

11-92

Linear and Telecom



# Linear & Telecom ICs

FOR ANALOG SIGNAL PROCESSING  
APPLICATIONS

 HARRIS

 **HARRIS**  
SEMICONDUCTOR

## NEW HIGH SPEED LINEAR PRODUCTS

### AMPLIFIERS

**HA-5020**  
**100MHz CURRENT FEEDBACK VIDEO**

(Page 3-368)

- UNITY GAIN BANDWIDTH ..... 100MHz
- DIFFERENTIAL GAIN ..... <0.02%
- DIFFERENTIAL PHASE ..... <0.03°
- SLEW RATE ..... 800V/μs
- GAIN FLATNESS ..... 0.1dB

**HA-2842**  
**WIDEBAND HIGH OUTPUT CURRENT VIDEO**

(Page 3-344)

- HIGH SLEW RATE ..... 375V/μs
- GAIN BANDWIDTH PRODUCT ..... 80MHz
- HIGH OUTPUT CURRENT ..... ±100mA
- DIFFERENTIAL GAIN/PHASE ..... 0.02%/0.03°
- LOW OFFSET VOLTAGE ..... 1mV

**HA-2839/40**  
**VERY HIGH SLEW RATE WIDEBAND**

(Page 3-335)

- HIGH SLEW RATE ..... 625V/μs
- WIDE GAIN BANDWIDTH ..... 600MHz
- DIFFERENTIAL GAIN/PHASE ..... 0.03%/0.03°
- LOW OFFSET VOLTAGE ..... 0.6mV
- FULL POWER BANDWIDTH ..... 10MHz

**HA-2841**  
**UNITY GAIN STABLE WIDEBAND VIDEO**

(Page 3-341)

- HIGH SLEW RATE ..... 240V/μs
- UNITY GAIN BANDWIDTH ..... 54MHz
- LOW OFFSET VOLTAGE ..... 1mV
- DIFFERENTIAL GAIN/PHASE ..... 0.03%/0.03°
- LOW DISTORTION ..... >83dB

**HA-2850**  
**LOW POWER HIGH SLEW RATE WIDEBAND**

(Page 3-347)

- LOW SUPPLY CURRENT ..... 8.0mA Max
- HIGH SLEW RATE ..... 340V/μs
- WIDE GAIN BANDWIDTH ..... 470MHz
- DIFFERENTIAL GAIN/PHASE ..... 0.04%/0.04°
- LOW OFFSET VOLTAGE ..... 0.6mV

**HA-5232/34**  
**DUAL/QUAD LOW COST PRECISION**

(Page 3-478)

- LOW OFFSET VOLTAGE ..... 300μV Max
- LOW OFFSET DRIFT ..... 2μV/°C
- LOW SUPPLY CURRENT ..... <1mA/A
- LOW BIAS CURRENT ..... 5nA
- HIGH CMRR/PSRR ..... 110dB

**HA-7712/13**  
**LOW POWER PRECISION**

(Page 3-481)

- VERY LOW POWER ..... 150μA (7712)  
15nA (7713)
- LOW OFFSET VOLTAGE ..... 250μV
- LOW INPUT BIAS CURRENT ..... 20pA
- WIDE OPERATING RANGE ..... 4V to 16V



## NEW HIGH SPEED LINEAR PRODUCTS

(Continued)

### MULTI-CHANNEL AMPLIFIERS

#### CA3256 VIDEO SWITCH AND AMPLIFIER

(Page 8-50)

- 5 MULTIPLEX VIDEO CHANNELS
  - ▶ 1 Independent Channel
  - ▶ 4 Channels With Enable
- UNITY GAIN BANDWIDTH ..... 25MHz
- PROGRAMMABLE VIDEO AMPLIFIER GAIN
- HIGH SIGNAL DRIVE CAPABILITY

#### HA-2444 SELECTABLE 4 CHANNEL VIDEO OP AMP

(Page 3-255)

- UNITY GAIN BANDWIDTH..... 45MHz
- DIFFERENTIAL GAIN ..... 0.03dB
- DIFFERENTIAL PHASE ..... 0.03°
- GAIN FLATNESS TO 10MHz ..... 0.1dB
- CROSSTALK REJECTION..... >60dB
- FAST CHANNEL SELECTION..... 60ns

### COMPARATORS

#### HFA-0003/3L ULTRA HIGH SPEED COMPARATOR

(Page 4-31)

- LOW PROPAGATION DELAY ..... 2.0/2.1ns
- LOW OFFSET VOLTAGE ..... 1mV
- WIDE COMMON MODE RANGE ..... +5.2/-2.8V
- USER PROGRAMMABLE HYSTERESIS
- WIDE TRACKING BANDWIDTH..... 270MHz

### MULTIPLIERS

#### HA-2556/2557 2 QUADRANT WIDEBAND ANALOG MULTIPLIER

(Pages 8-86 & 8-89)

- CHANNEL BANDWIDTH ..... 30/100MHz
- DIFFERENTIAL GAIN ..... 0.1%
- DIFFERENTIAL PHASE ..... 0.1°
- GAIN FLATNESS TO 10MHz ..... 0.1dB
- SLEW RATE ..... 350V/μs

### TELECOM SLICs

#### HC-5502B/HC-5504B/HC-5504DLC PBX SUBSCRIBER LINE INTERFACE CIRCUITS

(Page 9-75, 9-88 & 9-95)

- MEETS WORLDWIDE PBX REQUIREMENTS
- DIGITAL LOOP CARRIER MARKET (5504DLC)
- +5V AND +12V OPERATION

#### HC-5509B CENTRAL OFFICE SLIC

(Page 9-102)

- PROGRAMMABLE LOOP CURRENT
- THERMAL SHUTDOWN FEATURE
- TRANSMIT SIGNALS WHILE ON-HOOK

#### HC-5524 PBX AND DLC SLIC

(Page 9-111)

- PROGRAMMABLE LOOP CURRENT
- -24V BATTERY
- THERMAL SHUTDOWN FEATURE

## NEW POWER PROCESSING ICs

### DC/DC CONVERTERS AND REGULATORS

Produced on low power CMOS, these product offer superior performance over other second source devices while providing latch-free operation at very competitive prices.

#### ICL644/5/6/7 LOW VOLTAGE STEP-UP CONVERTERS

(Page 2-87)

- OUTPUT FROM A SINGLE CELL ..... +3V or +5V
- START-UP VOLTAGE ..... 0.9V
- I<sub>OUT</sub> ..... 200mA (INT. MOSFET)  
350mA (EXT. MOSFET)
- STANDBY CURRENT ..... 80µA

#### ICL7644/5/6/7 LOW VOLTAGE STEP-UP CONVERTERS

(Page 2-87)

- SAME AS ICL64X WITH SHUT DOWN FEATURE
- QUIESCENT CURRENT ..... 5µA
- AVAILABLE IN PDIP/SOIC

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### MOSFET DRIVERS

The "HV" family of MOSFET drivers utilize the benefits of Dielectric Isolation Technology to achieve cost effective SCR topologies with high voltage and high speed performance.

#### HV-350/355 HALF BRIDGE N-CHANNEL MOSFET DRIVER

(Page 2-54)

- +40V TO +450V, DC-30kHz (HV-350)
- +40V TO +450V, 10kHz-100kHz (HV-355)
- 2 AMPS PEAK
- RISE/FALL TIME ..... 75ns Max at 10000pF

#### HV-400 HIGH SPEED MOSFET DRIVER

(Page 2-62)

- PEAK SOURCE/SINK CURRENT ..... 6A/30A
- RISE TIME ..... 70ns
- FALL TIME ..... 30ns
- FREQUENCY RANGE ..... 300kHz

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### OFFLINE POWER SUPPLIES

Utilizing Harris Dielectric Isolation Technology and proprietary design, this product family provides direct offline to regulated DC conversion integrating the functions of rectifier, transformer, and 3 terminal regulator into a single cost saving IC.

#### HV-2405E SINGLE CHIP AC/DC POWER SUPPLY

(Page 2-76)

- INPUT RANGE ..... 18V to 264Vrms
- OUTPUT RANGE ..... 5V to 24VDC at 50mA
- 250mA OUTPUT WITH APP. NOTE AN9101
- UL RECOGNIZED (FILE # E130808)



## THE NEW HARRIS SEMICONDUCTOR

In December 1988, Harris Semiconductor acquired the General Electric Solid State division, thereby adding former GE, RCA, and Intersil devices to the Harris Semiconductor line.

This linear IC databook represents the full line of Harris Semiconductor linear products for commercial applications and supersedes previously published linear databooks under the Harris, GE, RCA or Intersil names. For a complete listing of all Harris Semiconductor products, please refer to the Product Selection Guide (SPG-201R; ordering information below).

For complete, current and detailed technical specifications on any Harris device please contact the nearest Harris sales, representative or distributor office; or direct literature requests to:

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See our  
specs in **CAPS**

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## LINEAR PRODUCT TECHNICAL ASSISTANCE

For technical assistance on the Harris products listed in this databook, please contact Field Applications Engineering staff available at one of the following Harris Sales Offices:

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### UNITED STATES

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|                      |                                       |
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### INTERNATIONAL

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|                |                                    |
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| <b>FRANCE</b>  | Paris . . . . . 33-1-346-54046     |
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| <b>KOREA</b>   | Seoul . . . . . 82-2-551-0931      |
| <b>U.K.</b>    | Camberley . . . . . 44-2-766-86886 |

For literature requests, please contact Harris Telemarketing at 407-724-3739.

# LINEAR

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GENERAL  
INFORMATION



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NOTE: Bold types designates a new product from Harris.



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## Obsolete Product Listing

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|---------------|------------------------------|
| CA 081        | NONE                         |
| CA 082        | NONE                         |
| CA 084        | NONE                         |
| CA 101        | LM 101                       |
| CA 201        | LM 201                       |
| CA 301        | LM 301                       |
| CA 307        | NONE                         |
| CA 311        | LM 311                       |
| CA 747        | LM 747                       |
| CA 748        | LM 748                       |
| CA 3000       | NONE                         |
| CA 3001       | CA 3100                      |
| CA 3002       | CA 3028                      |
| CA 3005       | CA 3100                      |
| CA 3006       | CA 3100                      |
| CA 3010/A     | CA 5420                      |
| CA 3015/A     | CA 3440/CA 3420              |
| CA 3029/A     | CA 5420                      |
| CA 3030/A     | CA 3440/CA 3420              |
| CA 3040       | NONE                         |
| CA 3250       | CA 3082                      |
| CA 3251       | CA 3081                      |
| CA 3401       | CA 5470                      |
| CA 3410       | NONE                         |
| CA 3493       | CA 3193                      |
| CA 3600       | CD 4002                      |
| CA 5422       | CA 5260/CA 5420              |
| CA 6078       | CA 3078                      |
| CA 6741       | CA 741                       |
| HA 2650/55    | CA 3440                      |
| HA 2720/25    | CA 3440                      |

| OBSOLETE PART | RECOMMENDED REPLACEMENT PART |
|---------------|------------------------------|
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| HA 5151       | HA 5142/CA 3440              |
| HA 5152       | HA 5142                      |
| HA 5154       | HA 5144                      |
| HA 5180       | CA 5420                      |
| HC 5512/12A   | NONE                         |
| ICH 8500      | CA 5420                      |
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| ICL 421       | ICL 7650S                    |
| ICL 422       | ICL 7650S                    |
| ICL 423       | ICL 7650S                    |
| ICL 7600      | NONE                         |
| ICL 7601      | NONE                         |
| ICL 7605      | NONE                         |
| ICL 7606      | NONE                         |
| ICL 7631      | ICL 7641/ICL 7642            |
| ICL 7652S     | ICL 7650S                    |
| ICL 7675      | HV 2405E                     |
| ICL 7676      | HV 2405E                     |
| ICL 7677      | ICL 7673                     |
| ICL 8007      | CA 5420                      |
| ICL 8021      | CA 3440                      |
| ICL 8023      | ICL 7641/ICL 7642            |
| ICM 7240      | ICL 7242                     |
| ICM 7250      | ICL 7242                     |
| LM 201        | LM 201                       |
| LM 301        | LM 301                       |
| LM 311        | LM 311                       |
| LM 747        | LM 747                       |
| LM 748        | LM 748                       |
| LM 4250       | CA 3440                      |

# Commercial Linear Product Cross Reference

| DEVICE                           | HARRIS REPLACEMENT                             | (Note 1)<br>PIN TO PIN | (Note 2)<br>EE | HARRIS ADVANTAGE OR COMMENTS   |
|----------------------------------|--|------------------------|----------------|--|
| 3507J                            | HA2-2525-5                                     | Yes                    | I              |  |
| 3508J                            | HA2-2625-5                                     | Yes                    | I              |  |
| 3551J<br>3551S                   | HA2-5162-5<br>HA2-5160-2                       | *<br>*                 | FE<br>FE       | Reduced Ibias/Greater Bandwidth<br>Reduced Ibias/Greater Bandwidth   |
| 3554AM<br>3554BM<br>3554SM       | HFA1-0001-9<br>HFA1-0001-9<br>HFA1-0001-9      | No<br>No<br>No         | FE<br>FE<br>FE | Greater Bandwidth/Faster Ts/Lower Cost<br>Greater Bandwidth/Faster Ts/Lower Cost<br>Greater Bandwidth/Faster Ts/Lower Cost |
| AD3554AM<br>AD3554BM<br>AD3554SM | HFA1-0001-9<br>HFA1-0001-9<br>HFA1-0001-9      | No<br>No<br>No         | FE<br>FE<br>FE | Greater Bandwidth/Faster Ts/Lower Cost<br>Greater Bandwidth/Faster Ts/Lower Cost<br>Greater Bandwidth/Faster Ts/Lower Cost |
| AD389BD<br>AD389KD               | HA1-5320-2<br>HA1-5320-5                       | No<br>No               | FE<br>FE       | Faster Acquisition/Reduced Droop<br>Faster Acquisition/Reduced Droop   |
| AD507JH<br>AD507KH               | HA2-2625-5<br>HA2-2625-5                       | Yes<br>Yes             | I<br>FE        |  |
| AD507SH                          | HA2-2620-2                                     | Yes                    | I              |  |
| AD509JH<br>AD509KH               | HA2-2525-5<br>HA2-2525-5                       | Yes<br>Yes             | I<br>FE        | Substitute HA2-2529-5<br>Substitute HA2-2529-5   |
| AD509SH                          | HA2-2520-2                                     | Yes                    | I              | Substitute HA2-2529-2  |
| AD518JH<br>AD518JN<br>AD518KH    | HA2-2515-5<br>HA3-2515-5<br>HA2-2515-5         | Yes<br>Yes<br>Yes      | I<br>I<br>FE   |  |
| AD518SH                          | HA2-2510-2                                     | Yes                    | I              |  |
| AD539JD<br>AD539KD<br>AD539SD    | HA1-2547-5<br>HA1-2547-5<br>HA1-2547-9         | No<br>No<br>No         | FE<br>FE<br>FE | Enhanced Bandwidth<br>Enhanced Bandwidth<br>Enhanced Bandwidth   |
| AD542JH                          | HA1-5170-5                                     | *                      | FE             | Enhanced ACs   |
| AD5539JN<br>AD5539JQ<br>AD5539SQ | HA3-2539-5<br>HA1-2539-5<br>HA1-2539-2         | *<br>*<br>*            | FE<br>FE<br>FE |  |
| AD582KD                          | HA1-2425-5                                     | No                     | FE             | Faster Acquisition/Enhanced ACs  |
| AD582SD                          | HA1-2420-2                                     | No                     | FE             | Faster Acquisition/Enhanced ACs  |
| AD583KD                          | HA1-2425-5                                     | Yes                    | FE             | Faster Acquisition/Greater Iout  |
| AD585AQ<br>AD585SQ               | HA1-5320-5<br>HA1-5320-2                       | No<br>No               | FE<br>FE       | Faster Acquisition/Reduced Droop<br>Faster Acquisition/Reduced Droop   |
| AD821AQ<br>AD821AS<br>AD821JN    | CA5160AE (PDIP)<br>CA5160AE (PDIP)<br>CA5160AE | *<br>*<br>*            | FE<br>FE<br>FE | Reduced Ibias/Enhanced ACs<br>Reduced Ibias/Enhanced ACs<br>Reduced Ibias/Enhanced ACs                                     |

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## Commercial Linear Product Cross Reference

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|--------------|--------------------|------------------------|----------------|---|
| AD840JN      | HA3B2840-5         | Yes                    | E              | Enhanced ACs/Lower Cost                 |
| AD840JQ      | HA1-2840-5         | Yes                    | E              | Enhanced ACs/Lower Cost                 |
| AD840KN      | HA3B2840-5         | Yes                    | E              | Enhanced ACs/Lower Cost                 |
| AD840KQ      | HA1-2840-5         | Yes                    | E              | Enhanced ACs/Lower Cost                 |
| AD840SQ      | HA1-2840/883       | Yes                    | E              | Enhanced ACs/Lower Cost                 |
| AD841JH      | HA2-2541-5         | Yes                    | FE             |   |
| AD841JN      | HA3B2841-5         | Yes                    | E              | Enhanced ACs/Lower Power                |
| AD841JQ      | HA1-2541-5         | Yes                    | FE             |   |
| AD841KH      | HA2-2541-5         | Yes                    | FE             |   |
| AD841KN      | HA3B2841-5         | Yes                    | E              | Enhanced ACs/Lower Power                |
| AD841KQ      | HA1-2841-5         | Yes                    | E              | Enhanced ACs/Lower Power                |
| AD841SH      | HA2-2841/883       | Yes                    | E              | Enhanced ACs/Lower Power                |
| AD841SQ      | HA1-2841/883       | Yes                    | E              | Enhanced ACs/Lower Power                |
| AD842JH      | HA2-2542-5         | Yes                    | FE             |   |
| AD842JN      | HA3B2842-5         | Yes                    | E              | Enhanced ACs/Lower Cost                 |
| AD842JQ      | HA1-2542-5         | Yes                    | FE             |   |
| AD842KH      | HA2-2542-5         | Yes                    | FE             |   |
| AD842KN      | HA3B2842-5         | Yes                    | E              | Enhanced ACs/Lower Cost                 |
| AD842KQ      | HA1-2542-5         | Yes                    | FE             |   |
| AD842SH      | HA2-2842/883       | Yes                    | E              | Enhanced ACs/Lower Cost                 |
| AD844AN      | HA3-5020-9         | Yes                    | FE             | Enhanced ACs and Video Performance      |
| AD844AQ      | HA7-5020-9         | Yes                    | FE             | Enhanced ACs and Video Performance      |
| AD844BQ      | HA7-5020-9         | Yes                    | FE             | Enhanced ACs and Video Performance      |
| AD844SQ/883B | HA7-5020/883       | Yes                    | FE             | Enhanced ACs and Video Performance      |
| AD846AN      | HA3-5020-9         | Yes                    | FE             | Enhanced ACs/Lower Cost                 |
| AD846AQ      | HA7-5020-9         | Yes                    | FE             | Enhanced ACs/Lower Cost                 |
| AD846BQ      | HA7-5020-9         | Yes                    | FE             | Enhanced ACs/Lower Cost                 |
| AD846SQ      | HA7-5020/883       | Yes                    | FE             | Enhanced ACs/Lower Cost                 |
| AD847JN      | HA3-2544C-5        | Yes                    | FE             |   |
| AD847SQ      | HA7-2544C-2        | Yes                    | FE             |   |
| AD9610BH     | HA1-5004-9         | No                     | FE             | Greater Bandwidth/Lower Cost Monolithic |
| AD9617JN     | HFA3-0001-5        | Yes                    | FE             | Greater Bandwidth/Lower Cost            |
| AD96685BH    | HFA2-0003L-9       | Yes                    | I              | Faster Propagation Delay/Lower Cost     |
| AD96685BQ    | HFA1-0003L-9       | Yes                    | I              | Faster Propagation Delay/Lower Cost     |
| AD96685BR    | HFA9P0003L-5       | Yes                    | I              | Faster Propagation Delay/Lower Cost     |
| ADLH0032CG   | HA2-2542-5         | *                      | FE             | Monolithic/Lower Cost                   |
| ADLH0032G    | HA2-2542-2         | *                      | FE             | Monolithic/Lower Cost                   |

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# Commercial Linear Product Cross Reference

| DEVICE   | HARRIS REPLACEMENT   | (Note 1)<br>PIN TO PIN                 | (Note 2)<br>EE             | HARRIS ADVANTAGE OR COMMENTS   |
|--|--|--|----------------------------|--|
| ADLH0033CG<br>ADLH0033G  | HA2-5033-5<br>HA2-5033-2   | *<br>*                                 | FE<br>FE                   | Enhanced ACs/Monolithic/Lower Cost<br>Enhanced ACs/Monolithic/Lower Cost   |
| ADOP27AH<br>ADOP27AQ   | HA2-5127A-2<br>HA7-5127A-2   | Yes<br>Yes                             | E<br>E                     | Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc   |
| ADOP27EH<br>ADOP27EQ<br>ADOP27GH<br>ADOP27GQ                         | HA2-5127A-5<br>HA7-5127A-5<br>HA2-5127-5<br>HA7-5127-5                               | Yes<br>Yes<br>Yes<br>Yes               | E<br>E<br>E<br>E           | Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc   |
| ADOP37AH<br>ADOP37AQ<br>ADOP37EH<br>ADOP37EQ<br>ADOP37GH<br>ADOP37GQ | HA2-5137A-2<br>HA7-5137A-2<br>HA2-5137A-5<br>HA7-5137A-5<br>HA2-5137-5<br>HA7-5137-5 | Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes | E<br>E<br>E<br>E<br>E<br>E | Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc |
| AM-450-2<br>AM-450-2M  | HA2-2505-5<br>HA2-2502-2   | Yes<br>Yes                             | E<br>E                     | Guaranteed DCs/ACs<br>Guaranteed DCs/ACs   |
| AM-452-2<br>AM-452-2M  | HA2-2525-5<br>HA2-2522-2   | Yes<br>Yes                             | E<br>E                     | Guaranteed DCs/ACs<br>Guaranteed DCs/ACs   |
| AM-460-2<br>AM-460-2M  | HA2-2605-5<br>HA2-2602-2   | Yes<br>Yes                             | E<br>E                     | Guaranteed DCs/ACs<br>Guaranteed DCs/ACs   |
| AM-462-2<br>AM-462-2M  | HA2-2625-5<br>HA2-2620-2   | Yes<br>Yes                             | E<br>E                     | Guaranteed DCs/ACs<br>Guaranteed DCs/ACs   |
| AM-7650-1<br>AM-7650-2   | ICL7650SCPD<br>ICL7650SCTV-1   | Yes<br>Yes                             | FE<br>FE                   | Almost Identical<br>Almost Identical   |
| BB3554AM<br>BB3554BM<br>BB3554SM                                     | HFA1-0001-9<br>HFA1-0001-9<br>HFA1-0001-9  | No<br>No<br>No                         | FE<br>FE<br>FE             | Greater Bandwidth/Faster Ts/Lower Cost<br>Greater Bandwidth/Faster Ts/Lower Cost<br>Greater Bandwidth/Faster Ts/Lower Cost   |
| CA3054   | CA3054   | Yes                                    | I                          | SOIC Version Available   |
| CA3059   | CA3059   | Yes                                    | I                          |  |
| CA3079   | CA3079   | Yes                                    | I                          |  |
| CA3146P  | CA3146E  | Yes                                    | I                          |  |
| CLC400AID<br>CLC400AJP   | HFA1-0001-9<br>HFA3-0001-9   | *<br>*                                 | FE<br>FE                   | Faster Transient Response<br>Faster Transient Response   |
| CLC401AID<br>CLC401AJP   | HFA1-0J05-9<br>HFA3-0005-9   | *<br>*                                 | FE<br>FE                   | Faster Transient Response<br>Faster Transient Response   |
| CLC430   | HA-5020  | Yes                                    | E                          | Enhanced AC and Video Performance  |
| CS-1524J   | CA1524F  | Yes                                    | I                          |  |

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## Commercial Linear Product Cross Reference

| DEVICE   | HARRIS REPLACEMENT                                   | (Note 1)<br>PIN TO PIN   | (Note 2)<br>EE       | HARRIS ADVANTAGE OR COMMENTS                             |
|--|--|--------------------------|----------------------|--|
| CS-2524J<br>CS-2524N                           | CA2524F<br>CA2524E                                   | Yes<br>Yes               | <br>                 |  |
| CS-3524J<br>CS-3524N                           | CA3524F<br>CA3524E                                   | Yes<br>Yes               | <br>                 |  |
| DS0026CJ-8<br>DS0026CN<br>DS0026H<br>DS0026J-8 | ICL7667CJA<br>ICL7667CPA<br>ICL7667MTV<br>ICL7667MJA | Yes<br>Yes<br>Yes<br>Yes | FE<br>FE<br>FE<br>FE | Reduced Icc<br>Reduced Icc<br>Reduced Icc<br>Reduced Icc |
| EHA1-2539-2<br>EHA1-2539-5                     | HA1-2539-2<br>HA1-2539-5                             | Yes<br>Yes               | <br>                 |  |
| EHA1-2540-2<br>EHA1-2540-5                     | HA1-2540-2<br>HA1-2540-5                             | Yes<br>Yes               | <br>                 |  |
| EHA1-5190-2<br>EHA1-5195-5                     | HA1-5190-2<br>HA1-5195-5                             | Yes<br>Yes               | <br>                 |  |
| EHA2-2500-2                                    | HA2-2500-2   | Yes                      |                      |  |
| EHA2-2502-2                                    | HA2-2502-2   | Yes                      |                      |  |
| EHA2-2505-5                                    | HA2-2505-5   | Yes                      |                      |  |
| EHA2-2510-2                                    | HA2-2510-2   | Yes                      |                      |  |
| EHA2-2512-2                                    | HA2-2512-2   | Yes                      |                      |  |
| EHA2-2515-5                                    | HA2-2515-5   | Yes                      |                      |  |
| EHA2-2520-2                                    | HA2-2520-2   | Yes                      |                      | Substitute HA2-2529-2                                    |
| EHA2-2522-2                                    | HA2-2522-2   | Yes                      |                      | Substitute HA2-2529-2                                    |
| EHA2-2525-5                                    | HA2-2525-5   | Yes                      |                      | Substitute HA2-2529-5                                    |
| EHA2-2600-2                                    | HA2-2600-2   | Yes                      |                      |  |
| EHA2-2602-2                                    | HA2-2602-2   | Yes                      |                      |  |
| EHA2-2605-5                                    | HA2-2605-5   | Yes                      |                      |  |
| EHA2-2620-2                                    | HA2-2620-2   | Yes                      |                      |  |
| EHA2-2622-2<br>EHA2-2625-5                     | HA2-2622-2<br>HA2-2625-5                             | Yes<br>Yes               | <br>                 |  |
| EHA2-5190-2<br>EHA2-5195-5                     | HA2-5190-2<br>HA2-5195-5                             | Yes<br>Yes               | <br>                 |  |
| EHA3-2539-5                                    | HA3-2539-5   | Yes                      |                      |  |
| EHA3-2540-5                                    | HA3-2540-5   | Yes                      |                      |  |
| EHA7-2500-2                                    | HA7-2500-2   | Yes                      |                      |  |

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|--------------|--------------------|------------------------|----------------|-------------------------------------|
| EHA7-2502-2  | HA7-2502-2         | Yes                    | I              |                                     |
| EHA7-2505-5  | HA7-2505-5         | Yes                    | I              |                                     |
| EHA7-2510-2  | HA7-2510-2         | Yes                    | I              |                                     |
| EHA7-2512-2  | HA7-2512-2         | Yes                    | I              |                                     |
| EHA7-2515-5  | HA7-2515-5         | Yes                    | I              |                                     |
| EHA7-2520-2  | HA7-2520-2         | Yes                    | I              |                                     |
| EHA7-2522-2  | HA7-2522-2         | Yes                    | I              |                                     |
| EHA7-2525-5  | HA7-2525-5         | Yes                    | I              |                                     |
| EHA7-2600-2  | HA7-2600-2         | Yes                    | I              |                                     |
| EHA7-2602-2  | HA7-2602-2         | Yes                    | I              |                                     |
| EHA7-2605-5  | HA7-2605-5         | Yes                    | I              |                                     |
| EHA7-2620-2  | HA7-2620-2         | Yes                    | I              |                                     |
| EHA7-2622-2  | HA7-2622-2         | Yes                    | I              |                                     |
| EHA7-2625-5  | HA7-2625-5         | Yes                    | I              |                                     |
| EL2003CH     | HA2-5002-5         | Yes                    | FE             | Greater Slew Rate/Reduced Icc       |
| EL2003CJ     | HA7-5002-5         | No                     | FE             | Greater Slew Rate/Reduced Icc       |
| EL2003CN     | HA3-5002-5         | No                     | FE             | Greater Slew Rate/Reduced Icc       |
| EL2003CPL    | HA9P5002-9         | No                     | FE             | Greater Slew Rate/Reduced Icc       |
| EL2003H      | HA2-5002-2         | Yes                    | FE             | Greater Slew Rate/Reduced Icc       |
| EL2003J      | HA7-5002-2         | No                     | FE             | Greater Slew Rate/Reduced Icc       |
| EL2005CG     | HA2-5033-5         | *                      | FE             | Greater Bandwidth                   |
| EL2005G      | HA2-5033-2         | *                      | FE             | Greater Bandwidth                   |
| EL2020CN     | HA3-5020-5         | Yes                    | E              | Enhanced ACs and DCs/Lower Cost     |
| EL2020CJ     | HA7-5020-5         | Yes                    | E              | Enhanced ACs and DCs/Lower Cost     |
| EL2020J      | HA7-5020/883       | Yes                    | E              | Enhanced ACs and DCs/Lower Cost     |
| EL2020J/883B | HA7-5020/883       | Yes                    | E              | Enhanced ACs and DCs/Lower Cost     |
| EL2020CM     | HA9P5020-5         | *                      | E              | Enhanced ACs and DCs/Lower Cost     |
| EL2030CN     | HA3-5020-5         | Yes                    | FE             | Enhanced DCs/Lower Cost             |
| EL2030CJ     | HA7-5020-5         | *                      | FE             | Enhanced DCs/Lower Cost             |
| EL2030J/883B | HA7-5020/883       | *                      | FE             | Enhanced DCs/Lower Cost             |
| EL2033CJ     | HA7-5002-5         | *                      | FE             | Greater Slew Rate/Reduced Icc       |
| EL2033CN     | HA3-5002-5         | *                      | FE             | Greater Slew Rate/Reduced Icc       |
| EL2033J      | HA7-5002-2         | *                      | FE             | Greater Slew Rate/Reduced Icc       |
| EL2039CJ     | HA1-2839-5         | Yes                    | FE             | Enhanced ACs/Lower Power/Lower Cost |
| EL2039CN     | HA3-2839-5         | Yes                    | FE             | Enhanced ACs/Lower Power/Lower Cost |
| EL2039J      | HA1-2839/883       | Yes                    | FE             | Enhanced ACs/Lower Power/Lower Cost |

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|--|--|--|--|--|
| EL2040CJ<br>EL2040CN<br>EL2040J  | HA1-2840-5<br>HA3-2840-5<br>HA1-2840/883   | Yes<br>Yes<br>Yes  | FE<br>FE<br>FE                               | Enhanced ACs/Lower Power/Lower Cost<br>Enhanced ACs/Lower Power/Lower Cost<br>Enhanced ACs/Lower Power/Lower Cost  |
| EL2041CG<br>EL2041CJ<br>EL2041G<br>EL2041J   | HA2-2541-5<br>HA1-2841-5<br>HA2-2841/883<br>HA1-2841/883   | Yes<br>Yes<br>Yes<br>Yes   | FE<br>FE<br>FE<br>FE                         | Enhanced ACs/Lower Power/Lower Cost<br>Enhanced ACs/Lower Power/Lower Cost<br>Enhanced ACs/Lower Power/Lower Cost<br>Enhanced ACs/Lower Power/Lower Cost |
| EL2190G<br>EL2190J   | HA2-5190-2<br>HA1-5190-2   | Yes<br>Yes   | FE<br>FE                                     |  |
| EL2195CG<br>EL2195CJ   | HA2-5195-5<br>HA1-5195-5   | Yes<br>Yes   | FE<br>FE                                     |  |
| ELH0032CG<br>ELH0032G  | HA2-2542-5<br>HA2-2542-2   | *<br>*   | FE<br>FE                                     |  |
| ELH0033CG<br>ELH0033G<br>HOS-100AH<br>HOS-100SH  | HA2-5033-5<br>HA2-5033-2<br>HA2-5033-2<br>HA2-5033-2   | *<br>*<br>*<br>*   | FE<br>FE<br>FE<br>FE                         | Greater Bandwidth<br>Greater Bandwidth<br>Greater Bandwidth/Lower Cost<br>Greater Bandwidth/Lower Cost   |
| HOS050<br>HOS050A<br>HOS050C   | HA2-2542-2<br>HA2-2542-2<br>HA2-2542-2   | *<br>*<br>*  | FE<br>FE<br>FE                               | Lower Cost<br>Lower Cost<br>Lower Cost   |
| ICL7611ACPA<br>ICL7611ACTV<br>ICL7611AMTV<br>ICL7611BCPA<br>ICL7611BCTV<br>ICL7611BMTV<br>ICL7611DCPA<br>ICL7611DCSA<br>ICL7611DCTV<br>ICL7611DMTV | ICL7611ACPA<br>ICL7611ACTV<br>ICL7611AMTV<br>ICL7611BCPA<br>ICL7611BCTV<br>ICL7611BMTV<br>ICL7611DCPA<br>ICL7611DCBA<br>ICL7611DCTV<br>ICL7611DMTV | Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes | <br> <br> <br> <br> <br> <br> <br> <br> <br> |  |
| ICL7612ACPA<br>ICL7612ACTV<br>ICL7612AMTV<br>ICL7612BCPA<br>ICL7612BCTV<br>ICL7612BMTV<br>ICL7612DCPA<br>ICL7612DCSA<br>ICL7612DCTV<br>ICL7612DMTV | ICL7612ACPA<br>ICL7612ACTV<br>ICL7612AMTV<br>ICL7612BCPA<br>ICL7612BCTV<br>ICL7612BMTV<br>ICL7612DCPA<br>ICL7612DCBA<br>ICL7612DCTV<br>ICL7612DMTV | Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes | <br> <br> <br> <br> <br> <br> <br> <br> <br> |  |

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| DEVICE   | HARRIS REPLACEMENT   | (Note 1)<br>PIN TO PIN   | (Note 2)<br>EE                               | HARRIS ADVANTAGE OR COMMENTS   |
|--|--|--|--|--|
| ICL7621ACPA<br>ICL7621ACTV<br>ICL7621AMTV<br>ICL7621BCPA<br>ICL7621BCTV<br>ICL7621BMTV<br>ICL7621DCPA<br>ICL7621DCSA<br>ICL7621DCTV<br>ICL7621DMTV | ICL7621ACPA<br>ICL7621ACTV<br>ICL7621AMTV<br>ICL7621BCPA<br>ICL7621BCTV<br>ICL7621BMTV<br>ICL7621DCPA<br>ICL7621DCBA<br>ICL7621DCTV<br>ICL7621DMTV | Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes | <br> <br> <br> <br> <br> <br> <br> <br> <br> |  |
| ICL7641CCPD<br>ICL7641ECPD   | ICL7641CCPD<br>ICL7641ECPD   | Yes<br>Yes   | <br>   |  |
| ICL7642CCJD<br>ICL7642CCPD<br>ICL7642CMJD<br>ICL7642ECJD<br>ICL7642ECPD<br>ICL7642EMJD   | ICL7642CCJD<br>ICL7642CCPD<br>ICL7642CMJD<br>ICL7642ECJD<br>ICL7642ECPD<br>ICL7642EMJD   | Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes                             | <br> <br> <br> <br> <br>                     |  |
| ICL7650BCPA-1<br>ICL7650BCPD<br>ICL7650BCTV-1  | ICL7650SCPA-1<br>ICL7650SCPD<br>ICL7650SCTV-1  | Yes<br>Yes<br>Yes  | FE<br>FE<br>FE                               | Reduced Vio/Ibias<br>Reduced Vio/Ibias<br>Reduced Vio/Ibias  |
| ICL7660CPA<br>ICL7660CSA<br>ICL7660CTV<br>ICL7660IJA<br>ICL7660ITV<br>ICL7660SMTV  | ICL7660SCPA<br>ICL7660SIBA<br>ICL7660SCTV<br>ICL7660SIPA (PDIP)<br>ICL7660SITV<br>ICL7660SMTV  | *<br>*<br>*<br>*<br>*<br>*   | E<br>E<br>E<br>E<br>E<br>E                   | Reduced Icc<br>Reduced Icc<br>Reduced Icc<br>Reduced Icc<br>Reduced Icc<br>Reduced Icc   |
| ICL7662CPA<br>ICL7662CTV   | ICL7662CPA<br>ICL7662CTV   | Yes<br>Yes   | E<br>E                                       | Reduced Vcc<br>Reduced Vcc   |
| ICL7663ACPA<br>ICL7663ACSA<br>ICL7663AIJA<br>ICL7663BCPA<br>ICL7663BIJA<br>ICL7663CPA<br>ICL7663CSA<br>ICL7663IJA                                  | ICL7663SACPA<br>ICL7663SCBA<br>ICL7663SACJA<br>ICL7663SCPA<br>ICL7663SIJA<br>ICL7663SCPA<br>ICL7663SCBA<br>ICL7663SIJA                             | Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes               | E<br>E<br>E<br>E<br>E<br>E<br>E<br>E         | Wider Voltage Range/Reduced Rsat<br>Wider Voltage Range/Reduced Rsat<br>Wider Voltage Range/Reduced Rsat<br>Wider Voltage Range/Reduced Rsat<br>Wider Voltage Range/Reduced Rsat<br>Wider Voltage Range/Reduced Rsat<br>Wider Voltage Range/Reduced Rsat<br>Wider Voltage Range/Reduced Rsat |
| ICL7665ACJA<br>ICL7665ACPA<br>ICL7665BCPA<br>ICL7665BCSA<br>ICL7665CJA<br>ICL7665CPA<br>ICL7665CSA   | ICL7665SACJA<br>ICL7665SACPA<br>ICL7665SCPA<br>ICL7665SCBA<br>ICL7665SCLA<br>ICL7665SCPA<br>ICL7665SCBA  | Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes                      | <br> <br>E<br>E<br> <br> <br>                | Enhanced Supply Range/Tempco<br>Enhanced Supply Range/Tempco   |

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GENERAL INFORMATION

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# Commercial Linear Product Cross Reference

| DEVICE  | HARRIS REPLACEMENT   | (Note 1)<br>PIN TO PIN                 | (Note 2)<br>EE                   | HARRIS ADVANTAGE OR COMMENTS   |
|---|--|--|----------------------------------|--|
| ICL7667CBA<br>ICL7667CJA<br>ICL7667CPA<br>ICL7667MJA                          | ICL7667CBA<br>ICL7667CJA<br>ICL7667CPA<br>ICL7667MJA                             | Yes<br>Yes<br>Yes<br>Yes               | FE<br>FE<br>FE<br>FE             |  |
| ICM7242IPA  | ICM7242IPA   | Yes                                    | FE                               |  |
| ICM7555CD<br>ICM7555CN<br>ICM7555IN<br>ICM7555IPA<br>ICM7555ITV<br>ICM7555MTV | ICM7555CBA<br>ICM7555IPA<br>ICM7555IPA<br>ICM7555IPA<br>ICM7555ITV<br>ICM7555MTV | Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes | FE<br>FE<br>FE<br>FE<br>FE<br>FE | Wider Operating Voltage Range<br>Wider Operating Voltage Range<br>Wider Operating Voltage Range  |
| ICM7556IPD<br>ICM7556MJD  | ICM7556IPD<br>ICM7556MJD   | Yes<br>Yes                             | FE<br>FE                         | Wider Operating Supply Range<br>Wider Operating Supply Range   |
| KF351N  | CA3140E  | Yes                                    | FE                               | Reduced I <sub>bias</sub> /I <sub>io</sub>   |
| KS272ACN<br>KS272AIN<br>KS272CN<br>KS272IN                                    | CA5260AE<br>CA5260AE<br>CA5260E<br>CA5260E                                       | Yes<br>Yes<br>Yes<br>Yes               | FE<br>FE<br>FE<br>FE             | Specified @ +5V Supply<br>Specified @ +5V Supply<br>Specified @ +5V Supply<br>Specified @ +5V Supply   |
| KS274CN<br>KS274IN  | CA5470E<br>CA5470E   | Yes<br>Yes                             | FE<br>FE                         | Greater Bandwidth/Spec. @ +5V Supply<br>Greater Bandwidth/Spec. @ +5V Supply   |
| LF157H  | CA3130AT   | Yes                                    | FE                               | Reduced I <sub>bias</sub>  |
| LF198AH<br>LF198H   | HA1-2420-2 (CDIP)<br>HA1-2420-2 (CDIP)   | No<br>No                               | FE<br>FE                         | Faster Acquisition<br>Faster Acquisition   |
| LF351D<br>LF351H<br>LF351M<br>LF351N<br>LF351P                                | CA3140M<br>CA3140T<br>CA3140M<br>CA3140E<br>CA3140E                              | Yes<br>Yes<br>Yes<br>Yes<br>Yes        | FE<br>FE<br>FE<br>FE<br>FE       | Reduced I <sub>bias</sub> /I <sub>io</sub><br>Reduced I <sub>bias</sub> /I <sub>io</sub><br>Reduced I <sub>bias</sub> /I <sub>io</sub><br>Reduced I <sub>bias</sub> /I <sub>io</sub><br>Reduced I <sub>bias</sub> /I <sub>io</sub> |
| LF353N<br>LF353P  | CA3240E<br>CA3240E   | Yes<br>Yes                             | FE<br>FE                         | Reduced I <sub>bias</sub> /I <sub>io</sub><br>Reduced I <sub>bias</sub> /I <sub>io</sub>   |
| LF357AH<br>LF357H<br>LF357M<br>LF357N   | CA3130AT<br>CA3130T<br>CA3130M<br>CA3130E  | Yes<br>Yes<br>Yes<br>Yes               | FE<br>FE<br>FE<br>FE             | Reduced I <sub>bias</sub><br>Reduced I <sub>bias</sub> /I <sub>io</sub><br>Reduced I <sub>bias</sub> /I <sub>io</sub><br>Reduced I <sub>bias</sub> /I <sub>io</sub>  |
| LF398AH<br>LF398AN<br>LF398H (CAN)<br>LF398N                                  | HA1-2425-5 (CDIP)<br>HA3-2425-5<br>HA1-2425-5 (CDIP)<br>HA3-2425-5               | No<br>No<br>No<br>No                   | FE<br>FE<br>FE<br>FE             | Faster Acquisition<br>Faster Acquisition<br>Faster Acquisition<br>Faster Acquisition   |
| LF400CH   | CA3100T  | *                                      | FE                               | Similar ACs  |

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# Commercial Linear Product Cross Reference

| DEVICE   | HARRIS REPLACEMENT   | (Note 1)<br>PIN TO PIN          | (Note 2)<br>EE             | HARRIS ADVANTAGE OR COMMENTS  |
|--|--|---------------------------------|----------------------------|---|
| LF411CD<br>LF411CH<br>LF411CN<br>LF411CP<br>LF411MH      | CA3140AM<br>CA3140AT<br>CA3140AE<br>CA3140AE<br>CA3140AT           | Yes<br>Yes<br>Yes<br>Yes<br>Yes | FE<br>FE<br>FE<br>FE<br>FE | Reduced Ibias/Iio<br>Reduced Ibias/Iio<br>Reduced Ibias/Iio<br>Reduced Ibias/Iio<br>Reduced Ibias/Iio   |
| LF412CD<br>LF412CN<br>LF412CP                            | CA3240AE<br>CA3140AE<br>CA3240AE                                   | Yes<br>Yes<br>Yes               | FE<br>FE<br>FE             | Reduced Ibias/Iio<br>Reduced Ibias/Iio<br>Reduced Ibias/Iio   |
| LH0002CH<br>LH0002CN<br>LH0002H                          | HA2-5002-5<br>HA3-5002-5<br>HA2-5002-2                             | *<br>No<br>*                    | E<br>E<br>E                | Enhanced ACs/DCs/Monolithic<br>Enhanced ACs/DCs/Monolithic<br>Enhanced ACs/DCs/Monolithic   |
| LH0022CD<br>LH0022CH                                     | CA3140AE (PDIP)<br>CA3140AT  | No<br>Yes                       | FE<br>FE                   | Greater Bandwidth/Slew Rate<br>Greater Bandwidth/Slew Rate  |
| LH0032ACG<br>LH0032AG<br>LH0032CG<br>LH0032G             | HA2-2542-S<br>HA2-2542-2<br>HA2-2542-5<br>HA2-2542-2               | Yes<br>Yes<br>Yes<br>Yes        | FE<br>FE<br>FE<br>FE       | Monolithic/Lower Cost<br>Monolithic/Lower Cost<br>Monolithic/Lower Cost<br>Monolithic/Lower Cost  |
| LH0033ACG<br>LH0033AG<br>LH0033CG<br>LH0033CJ<br>LH0033G | HA2-5033-5<br>HA2-5033-2<br>HA2-5033-5<br>HA3-5033-5<br>HA2-5033-2 | *<br>*<br>*<br>*<br>*           | FE<br>FE<br>FE<br>FE<br>FE | Greater Bandwidth/Monolithic/Lower Cost<br>Monolithic/Lower Cost<br>Greater Bandwidth/Monolithic/Lower Cost<br>Monolithic/Lower Cost<br>Monolithic/Lower Cost |
| LH0042CD<br>LH0042CH                                     | CA3140E (PDIP)<br>CA3140T  | No<br>Yes                       | FE<br>FE                   | Greater Bandwidth/Slew Rate<br>Greater Bandwidth/Slew Rate  |
| LH4004CD<br>LH4004D                                      | HA1-5004-5<br>HA1-5004-9   | No<br>No                        | FE<br>FE                   | Monolithic/Lower Cost<br>Monolithic/Lower Cost  |
| LH4161CH<br>LH4161CJ<br>LH4161H<br>LH4161J               | HA2-2544-5<br>HA7-2544-5<br>HA2-2544-2<br>HA7-2544-2               | No<br>No<br>No<br>No            | FE<br>FE<br>FE<br>FE       | PDIP Substitute is HA3-2544C-5  |
| LM143H   | HA2-2640-2   | *                               | FE                         | Enhanced ACs  |
| LM1524DJ   | CA1524F  | Yes                             | I                          |   |
| LM193H   | CA3290AT   | Yes                             | FE                         | MOSFET Input  |
| LM2524DN   | CA2524E  | Yes                             | I                          |   |
| LM2901N<br>LM2903N<br>LM293H                             | CA3290AE<br>CA3290AE<br>CA3290AT                                   | Yes<br>Yes<br>Yes               | FE<br>FE<br>FE             | MOSFET Input<br>MOSFET Input<br>MOSFET Input  |
| LM3045J  | CA3045F  | Yes                             | I                          |   |
| LM3046D<br>LM3046N                                       | CA3046M<br>CA3046E   | Yes<br>Yes                      | FE<br>I                    |   |

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|--|--|----------------------------|----------------------------|--|
| LM3080AN<br>LM3080N                                    | CA3080AE<br>CA3080E  | Yes<br>Yes                 | FE<br>FE                   |  |
| LM3086J<br>LM3086M<br>LM3086N                          | CA3086F<br>CA3086M<br>CA3086                                       | Yes<br>Yes<br>Yes          | I<br>I<br>I                |  |
| LM3146M<br>LM3146N                                     | CA3146M<br>CA3146E   | Yes<br>Yes                 | I<br>I                     | Enhanced "A" Version Offered<br>Enhanced "A" Version Offered                                       |
| LM3302N  | CA3290E/LM3302N  | Yes                        | I                          |  |
| LM3401N  | CA3401E  | Yes                        | E                          | Greater Bandwidth  |
| LM343H   | HA2-2645-5   | *                          | FE                         | Enhanced ACs   |
| LM3524DN<br>LM3524J<br>LM3524N                         | CA3524E<br>CA3524F<br>CA3524E                                      | Yes<br>Yes<br>Yes          | I<br>I<br>I                |  |
| LM393H<br>LM393N                                       | CA3290AT<br>CA3290AE   | Yes<br>Yes                 | FE<br>FE                   | MOSFET Input<br>MOSFET Input   |
| LM556CN  | ICM7556IPD   | Yes                        | FE                         | CMOS/Reduced Icc   |
| LM604ACM<br>LM604ACN<br>LM604AMJ<br>LM604CM<br>LM604CN | HA9P2406-5<br>HA3-2406-5<br>HA1-2400-2<br>HA9P2406-5<br>HA3-2406-5 | No<br>No<br>No<br>No<br>No | FE<br>FE<br>FE<br>FE<br>FE | Enhanced ACs<br>Enhanced ACs<br>Enhanced ACs<br>Enhanced ACs<br>Enhanced ACs                       |
| LM6118J  | HA7-5222-9   | Yes                        | FE                         | Lower Vio  |
| LM6161J  | HA7-2544-2   | *                          | FE                         | Guaranteed Differential Phase/Gain   |
| LM6164J  | HA1-5190-2   | No                         | FE                         | Reduced Voltage Noise  |
| LM6165J  | HA1-2540-2   | No                         | FE                         | Enhanced Slew Rate/Avol  |
| LM6218AH<br>LM6218AJ                                   | HA2-5222-9<br>HA7-5222-9   | No<br>Yes                  | FE<br>FE                   | Lower Vio<br>Lower Vio   |
| LM6361N  | HA3-2544C-5  | *                          | FE                         | Guaranteed Differential Phase/Gain   |
| LM6364N  | HA1-5195-5   | No                         | FE                         | Reduced Voltage Noise  |
| LM6365N  | HA3-2540C-5  | No                         | FE                         | Enhanced Slew Rate/Avol  |
| LM723CH<br>LM723CN<br>LM723H                           | CA0723CT<br>CA0723CE<br>CA0723T/LM723H                             | Yes<br>Yes<br>Yes          | I<br>I<br>I                |  |
| LMC555CH<br>LMC555CM<br>LMC555CN                       | ICM7555ITV<br>ICM7555CBA<br>ICM7555IPA                             | Yes<br>Yes<br>Yes          | FE<br>FE<br>FE             | Reduced Icc/Wider Supply Range<br>Reduced Icc/Wider Supply Range<br>Reduced Icc/Wider Supply Range |

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|--|--|--|--|--|
| LMC668ACJ<br>LMC668ACJ-8<br>LMC668ACN<br>MC668ACN-8  | ICL7650SIJD<br>ICL7650SIJA-1<br>ICL7650SIPD<br>ICL7650SCPA-1   | Yes<br>Yes<br>Yes<br>Yes                             | E<br>E<br>E<br>E                             | Enhanced DCs<br>Enhanced DCs<br>Enhanced DCs<br>Enhanced DCs   |
| LMC7660IN  | ICL7660SIPA  | *  | E  | Reduced Icc/Enhanced Efficiency  |
| LS204AT<br>LS204CB<br>LS204CM<br>LS204CT<br>LS204T   | HA2-5102-2<br>HA3-5102-5<br>HA9P-5102-5<br>HA2-5102-5<br>HA2-5102-2  | Yes<br>Yes<br>Yes<br>Yes<br>Yes                      | FE<br>FE<br>FE<br>FE<br>FE                   | Reduced Noise Voltage<br>Reduced Noise Voltage<br>Reduced Noise Voltage<br>Reduced Noise Voltage<br>Reduced Noise Voltage  |
| LS404CB<br>LS404CM<br>LS404M   | HA3-5104-5<br>HA9P-5104-5<br>HA9P-5104-9   | Yes  | FE<br>FE<br>FE                               | Reduced Noise Voltage<br>Reduced Noise Voltage<br>Reduced Noise Voltage  |
| LS776CB<br>LS776T  | CA3440AE<br>CA3440AT   | Yes<br>Yes   | FE<br>FE                                     | MOS Input<br>MOS Input   |
| LT1001CH<br>LT1001CJ8<br>LT1001MH<br>LT1001MJ8   | HA2-5177-5<br>HA7-5177-5<br>HA2-5177-2<br>HA7-5177-2   | Yes<br>Yes<br>Yes<br>Yes                             | FE<br>FE<br>FE<br>FE                         | Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc   |
| LT1014ACJ<br>LT1014AMJ<br>LT1014CJ<br>LT1014MJ   | HA1-5134A-5<br>HA1-5134A-2<br>HA1-5134-5<br>HA1-5134-2   | Yes<br>Yes<br>Yes<br>Yes                             | FE<br>FE<br>FE<br>FE                         | Reduced Vio/Enhanced ACs<br>Reduced Vio/Enhanced ACs<br>Reduced Vio/Enhanced ACs<br>Reduced Vio/Enhanced ACs   |
| LT1022CH<br>LT1022MH   | HA2-5160-5<br>HA2-5160-2   | *<br>*   | FE<br>FE                                     | Greater Bandwidth/Slew Rate<br>Greater Bandwidth/Slew Rate   |
| LT1037ACH<br>LT1037ACJ8<br>LT1037AMH<br>LT1037AMJ8<br>LT1037CH<br>LT1037CJ8<br>LT1037MH<br>LT1037MJ8 | HA2-5137A-5<br>HA7-5137A-5<br>HA2-5137A-2<br>HA7-5137A-2<br>HA2-5137-5<br>HA7-5137-5<br>HA2-5137-2<br>HA7-5137-2 | Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes | FE<br>FE<br>FE<br>FE<br>FE<br>FE<br>FE<br>FE | Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc |
| LT1073-5CN8<br>LT1073-5CS8   | ICL644CPD<br>ICL644CBD   | No<br>No   | FE<br>FE                                     |  |
| LT1223CJ8<br>LT1223CN8<br>LT1223CS8<br>LT1223MJ8   | HA7-5020-5<br>HA3-5020-5<br>HA9P5020-5<br>HA7-5020/883   | Yes<br>Yes<br>Yes<br>Yes                             | E<br>E<br>E<br>E                             | Enhanced ACs and Video Performance<br>Enhanced ACs and Video Performance<br>Enhanced ACs and Video Performance<br>Enhanced ACs and Video Performance   |
| LT1524J  | CA1524F  | Yes  | I  |  |
| LT3524J<br>LT3524N   | CA3524F<br>CA3524E   | Yes<br>Yes   | I<br>I                                       |  |

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|--|---|---------------------------------|--|--|
| LTC1044CH<br>LTC1044CN8<br>LTC1044MH   | ICL7660SITV<br>ICL7660SIPA<br>ICL7660SMTV   | Yes<br>Yes<br>Yes               | E<br>E<br>E                            | Reduced Icc/Wider Voltage Range<br>Reduced Icc/Wider Voltage Range<br>Reduced Icc/Wider Voltage Range  |
| LTC1050ACH<br>LTC1050ACN8<br>LTC1050AMH<br>LTC1050CH<br>LTC1050CN8<br>LTC1050CP<br>LTC1050MH | ICL7650SITV-1<br>ICL7650SIPA-1<br>ICL7650SMTV-1<br>ICL7650SITV-1<br>ICL7650SIPA-1<br>ICL7650SIPA-1<br>ICL7650SMTV-1 | *<br>*<br>*<br>*<br>*<br>*<br>* | FE<br>FE<br>FE<br>FE<br>FE<br>FE<br>FE | Reduced Ibias/Iio<br>Reduced Ibias/Iio<br>Reduced Ibias/Iio<br>Reduced Ibias/Iio/Greater Avol<br>Reduced Ibias/Iio/Greater Avol<br>Reduced Ibias/Iio<br>Reduced Ibias/Iio/Greater Avol |
| MA723CN  | CA0723CE  | Yes                             | I                                      |  |
| MAX460IGC<br>MAX460MGC   | HA2-5033-5<br>HA2-5033-2  | *<br>*                          | FE<br>FE                               | Greater Bandwidth<br>Greater Bandwidth   |
| MAX610CP<br>MAX611CP<br>MAX612CP   | HV3-1205/2405E-5<br>HV3-1205/2405E-5<br>HV3-1205/2405E-5  | No<br>No<br>No                  | FE<br>FE<br>FE                         | Guaranteed Surge Protection<br>Guaranteed Surge Protection<br>Guaranteed Surge Protection  |
| MAX626CPA<br>MAX626CSA<br>MAX626EJA<br>MAX626MJA   | ICL7667CPA<br>ICL7667CBA<br>ICL7667CJA<br>ICL7667MJA  | Yes<br>Yes<br>Yes<br>Yes        | FE<br>FE<br>FE<br>FE                   | Reduced T Delay/Icc<br>Reduced T Delay/Icc<br>Reduced T Delay/Icc<br>Reduced T Delay/Icc   |
| MAX654CPD<br>MAX654CSD<br>MAX654EPD<br>MAX654ESD   | ICL644CPD<br>ICL644CBD<br>ICL644IPD<br>ICL644IBD  | Yes<br>Yes<br>Yes<br>Yes        | FE<br>FE<br>FE<br>FE                   | Shutdown Feature With ICL7644 Version<br>Shutdown Feature With ICL7644<br>Shutdown Feature With ICL7644 Version<br>Shutdown Feature With ICL7644 Version                               |
| MAX655CPD<br>MAX655CSD<br>MAX655EPD<br>MAX655ESD   | ICL645CPD<br>ICL645CBD<br>ICL645IPD<br>ICL645IBD  | Yes<br>Yes<br>Yes<br>Yes        | FE<br>FE<br>FE<br>FE                   | Shutdown Feature With ICL7645 Version<br>Shutdown Feature With ICL7645 Version<br>Shutdown Feature With ICL7645 Version<br>Shutdown Feature With ICL7645 Version                       |
| MAX656CPD<br>MAX656CSD<br>MAX656EPD<br>MAX656ESD   | ICL646CPD<br>ICL646CBD<br>ICL646IPD<br>ICL646IBD  | Yes<br>Yes<br>Yes<br>Yes        | FE<br>FE<br>FE<br>FE                   | Shutdown Feature With ICL7646 Version<br>Shutdown Feature With ICL7646 Version<br>Shutdown Feature With ICL7646 Version<br>Shutdown Feature With ICL7646 Version                       |
| MAX657CPD<br>MAX657CSD<br>MAX657EPD<br>MAX657ESD   | ICL647CPD<br>ICL647CBD<br>ICL647IPD<br>ICL647IBD  | Yes<br>Yes<br>Yes<br>Yes        | FE<br>FE<br>FE<br>FE                   | Shutdown Feature With ICL7647 Version<br>Shutdown Feature With ICL7647 Version<br>Shutdown Feature With ICL7647 Version<br>Shutdown Feature With ICL7647 Version                       |
| MAX663CPA<br>MAX663CSA<br>MAX663EJA<br>MAX663EPA<br>MAX663ESA                                | ICL7663SACPA<br>ICL7663SCBA<br>ICL7663SAIJA<br>ICL7663SAIPA<br>ICL7663SIBA  | *<br>*<br>*<br>*<br>*           | FE<br>FE<br>FE<br>FE<br>FE             | Reduced Icc/Greater Voltage Range<br>Reduced Icc/Greater Voltage Range<br>Reduced Icc/Greater Voltage Range<br>Reduced Icc/Greater Voltage Range<br>Reduced Icc/Greater Voltage Range  |

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# Commercial Linear Product Cross Reference

| DEVICE  | HARRIS REPLACEMENT  | (Note 1)<br>PIN TO PIN                 | (Note 2)<br>EE             | HARRIS ADVANTAGE OR COMMENTS   |
|---|---|--|----------------------------|--|
| MAX8211CPA<br>MAX8211CPA-2<br>MAX8211CSA<br>MAX8211CTY                | ICL8211CPA<br>ICL8211CPA<br>ICL8211CBA<br>ICL8211CTY                  | Yes<br>Yes<br>Yes<br>Yes               | FE<br>FE<br>FE<br>FE       | Bipolar/Wider Supply Range<br>Bipolar/Wider Supply Range<br>Bipolar/Wider Supply Range<br>Bipolar/Wider Supply Range   |
| MAX8212CPA<br>MAX8212CSA<br>MAX8212CTY                                | ICL8212CPA<br>ICL8212CBA<br>ICL8212CTY                                | Yes<br>Yes<br>Yes                      | FE<br>FE<br>FE             | Bipolar/Wider Supply Range<br>Bipolar/Wider Supply Range<br>Bipolar/Wider Supply Range   |
| MAX9685CJE<br>MAX9685CPE<br>MAX9685CSE<br>MAX9685CTW                  | HFA1-0003L-5<br>HFA3-0003L-5<br>HFA9P0003L-5<br>HFA2-0003L-5          | Yes<br>Yes<br>Yes<br>Yes               | I<br>I<br>I<br>I           |  |
| MAX9690CJA<br>MAX9690CPA<br>MAX9690CSA                                | HFA1-0003-5<br>HFA3-0003-5<br>HFA9P0003-5                             | Yes<br>Yes<br>Yes                      | I<br>I<br>I                |  |
| MC1723CG<br>MC1723CGD<br>MC1723CP<br>MC1723CPD<br>MC1723G<br>MC1723GD | CA0723CT<br>CA0723CTX<br>CA0723CE<br>CA0723CEX<br>CA0723T<br>CA0723TX | Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes | I<br>I<br>I<br>I<br>I<br>I |  |
| MC1776CD<br>MC1776CG<br>MC1776CP1<br>MC1776G                          | ICL7611DCBA<br>ICL7611BCTV<br>ICL7611BCPA<br>ICL7611BMTV              | Yes<br>Yes<br>Yes<br>Yes               | FE<br>FE<br>FE<br>FE       | Lower Power Drain<br>Lower Power Drain<br>Lower Power Drain<br>Lower Power Drain   |
| MC3302N   | CA3290E   | Yes                                    | FE                         | MOSFET Input   |
| MC3303D<br>MC3303N  | CA5470M<br>CA5470E  | Yes<br>Yes                             | FE<br>FE                   | MOS Input/Enhanced ACs<br>FEMOS Input/Enhanced ACs   |
| MC33071P  | CA3140AE  | Yes                                    | FE                         | Reduced I <sub>bias</sub> /I <sub>io</sub>   |
| MC33072P  | CA3240AE  | Yes                                    | FE                         | Reduced I <sub>bias</sub> /I <sub>io</sub>   |
| MC3346D<br>MC3346P  | CA3046M<br>CA3046E  | Yes<br>Yes                             | I<br>I                     | Full -55 to 125 Degrees C Operation<br>Full -55 to 125 Degrees C Operation   |
| MC34001BG<br>MC34001BP<br>MC34001G<br>MC34001P                        | CA3140AT<br>CA3140AE<br>CA3140T<br>CA3140E                            | Yes<br>Yes<br>Yes<br>Yes               | FE<br>FE<br>FE<br>FE       | Reduced I <sub>bias</sub> /I <sub>io</sub><br>Reduced I <sub>bias</sub> /I <sub>io</sub><br>Reduced I <sub>bias</sub> /I <sub>io</sub><br>Reduced I <sub>bias</sub> /I <sub>io</sub> |
| MC34002BG<br>MC34002BP<br>MC34002G                                    | CA3240AT<br>CA3240AE<br>CA3240T                                       | Yes<br>Yes<br>Yes                      | FE<br>FE<br>FE             | Reduced I <sub>bias</sub> /I <sub>io</sub><br>Reduced I <sub>bias</sub> /I <sub>io</sub><br>Reduced I <sub>bias</sub> /I <sub>io</sub>   |
| MC34002P  | CA34002E  | Yes                                    | FE                         | Reduced I <sub>bias</sub> /I <sub>io</sub>   |
| MC3401P   | CA3401E   | Yes                                    | FE                         | Greater Bandwidth  |

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GENERAL INFORMATION

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# Commercial Linear Product Cross Reference

| DEVICE                                       | HARRIS REPLACEMENT                                   | (Note 1)<br>PIN TO PIN   | (Note 2)<br>EE       | HARRIS ADVANTAGE OR COMMENTS   |
|--|--|--------------------------|----------------------|--|
| MC3403D<br>MC3403N                           | CA5470M<br>CA5470E                                   | Yes<br>Yes               | FE<br>FE             | MOS Input/Enhanced ACs<br>MOS Input/Enhanced ACs   |
| MC34071P                                     | CA3140AE   | Yes                      | FE                   | Reduced Ibias/Iio  |
| MC34072P                                     | CA3240AE   | Yes                      | FE                   | Reduced Ibias/Iio  |
| MC34151D<br>MC34151P                         | ICL7667CBA<br>ICL7667CPA                             | Yes<br>Yes               | FE<br>FE             | CMOS/Reduced Icc/Faster Switching<br>CMOS/Reduced ICC/Faster Switching                                       |
| MC3456L<br>MC3456P<br>MC3556L                | ICM7556MJD<br>ICM7556IPD<br>ICM7556MJD               | Yes<br>Yes<br>Yes        | FE<br>FE<br>FE       | CMOS/Reduced Icc<br>CMOS/Reduced Icc<br>CMOS/Reduced Icc   |
| MIC426<br>MMH0026CP1<br>MMH0026G<br>MMH0026U | ICL7667CPA<br>ICL7667CPA<br>ICL7667MTV<br>ICL7667CJA | Yes<br>Yes<br>Yes<br>Yes | FE<br>FE<br>FE<br>FE | Reduced Icc<br>Reduced Icc<br>Reduced Icc  |
| NE5230N                                      | CA5160AE   | No                       | FE                   | MOS Input  |
| NE5517AN<br>NE5517D<br>NE5517N               | CA3280AE<br>CA3280M<br>CA3280E                       | No<br>No<br>No           | FE<br>FE<br>FE       | Reduced Vio<br>Reduced Vio<br>Reduced Vio  |
| NE5532AFE<br>NE5532AN<br>NE5532FE<br>NE5532N | HA7-5102-5<br>HA3-5102-5<br>HA7-5102-5<br>HA3-5102-5 | Yes<br>Yes<br>Yes<br>Yes | FE<br>FE<br>FE<br>FE | Enhanced DCs/Reduced Icc<br>Enhanced DCs/Reduced Icc<br>Enhanced DCs/Reduced Icc<br>Enhanced DCs/Reduced Icc |
| NE5534AFE<br>NE5534AN<br>NE5534FE<br>NE5534N | HA7-5101-5<br>HA3-5101-5<br>HA7-5101-5<br>HA3-5101-5 | *<br>*<br>*<br>*         | FE<br>FE<br>FE<br>FE | Enhanced DCs<br>Enhanced DCs<br>Enhanced DCs<br>Enhanced DCs   |
| NE5539D<br>NE5539F<br>NE5539N                | HA9P-2539-5<br>HA1-2539-5<br>HA3-2539-5              | *<br>*<br>*              | FE<br>FE<br>FE       | Specified @ +/- 15V Supplies<br>Specified @ +/- 15V Supplies<br>Specified @ +/- 15V Supplies                 |
| NE556-1N<br>NE556N                           | ICM7556IPD<br>ICM7556IPD                             | Yes<br>Yes               | FE<br>FE             | CMOS/Reduced Icc<br>CMOS/Reduced Icc   |
| OP-15CH<br>OP-15GN8                          | CA3140AT<br>CA3140AE                                 | Yes<br>Yes               | FE<br>FE             | Reduced Ibias/Iio<br>Reduced Ibias/Iio   |
| OP11AY<br>OP11EY                             | HA1-5134-2<br>HA1-5134-5                             | Yes                      | FE<br>FE             | Enhanced ACs<br>Enhanced ACs   |
| OP11FY                                       | HA1-5104-5   | Yes                      | FE                   | Enhanced ACs   |
| OP160GP<br>OP160GS                           | HA3-5020-9<br>HA9P5020-5                             | Yes<br>Yes               | E<br>E               |  |
| OP215GZ                                      | CA3240AE (PDIP)                                      | Yes                      | FE                   |  |

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| DEVICE  | HARRIS REPLACEMENT | (Note 1)<br>PIN TO PIN | (Note 2)<br>EE | HARRIS ADVANTAGE OR COMMENTS          |
|---------|--------------------|------------------------|----------------|---------------------------------------|
| OP220CJ | HA2-5142-2         | Yes                    | FE             | Enhanced ACs                          |
| OP220CZ | HA7-5142-2         | Yes                    | FE             | Enhanced ACs                          |
| OP220GJ | HA2-5142-5         | Yes                    | FE             | Enhanced ACs                          |
| OP220GZ | HA7-5142-5         | Yes                    | FE             | Enhanced ACs                          |
| OP271AZ | HA7-5102-2         | Yes                    | FE             | Lower Voltage Noise/Greater Bandwidth |
| OP271EZ | HA7-5102-5         | Yes                    | FE             | Lower Voltage Noise/Greater Bandwidth |
| OP271FZ | HA7-5102-5         | Yes                    | FE             | Lower Voltage Noise/Greater Bandwidth |
| OP271GP | HA3-5102-5         | Yes                    | FE             | Lower Voltage Noise/Greater Bandwidth |
| OP271GS | HA9P-5102-9        | Yes                    | FE             | Lower Voltage Noise/Greater Bandwidth |
| OP27AH  | HA2-5127A-2        | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP27AJ  | HA2-5127A-2        | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP27AJ8 | HA7-5127A-2        | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP27AZ  | HA7-5127A-2        | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP27CH  | HA2-5127-2         | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP27CJ  | HA2-5127-2         | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP27CJ8 | HA7-5127-2         | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP27CZ  | HA7-5127-2         | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP27EH  | HA2-5127A-5        | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP27EJ  | HA2-5127A-5        | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP27EJ8 | HA7-5127A-5        | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP27EZ  | HA7-5127A-5        | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP27GH  | HA2-5127-5         | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP27GJ  | HA2-5127-5         | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP27GJ8 | HA7-5127-5         | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP27GZ  | HA7-5127-5         | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP37AH  | HA2-5137A-2        | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP37AJ  | HA2-5137A-2        | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP37AJ8 | HA7-5137A-2        | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP37AZ  | HA7-5137A-2        | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP37CH  | HA2-5137-2         | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP37CJ  | HA2-5137-2         | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP37CJ8 | HA7-5137-2         | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP37CZ  | HA7-5137-2         | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP37EH  | HA2-5137A-5        | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP37EJ  | HA2-5137A-5        | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP37EJ8 | HA7-5137A-5        | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP37EZ  | HA7-5137A-5        | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP37GH  | HA2-5137-5         | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP37GJ  | HA2-5137-5         | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP37GJ8 | HA7-5137-5         | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP37GZ  | HA7-5137-5         | Yes                    | E              | Enhanced ACs/Reduced Icc              |
| OP400AY | HA1-5134A-2        | Yes                    | FE             |                                       |
| OP400EY | HA1-5134A-5        | Yes                    | FE             |                                       |
| OP400FY | HA1-5134-5         | Yes                    | FE             |                                       |
| OP41EJ  | CA3193AT           | Yes                    | FE             | Reduced Vio/Noise Voltage             |
| OP41FJ  | CA3193T            | Yes                    | FE             | Reduced Vio/Noise Voltage             |
| OP41GP  | CA3193E            | Yes                    | FE             | Reduced Vio/Noise Voltage             |

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|--|--|--|--|--|
| OP420BY<br>OP420CY<br>OP420HY  | HA1-5144-2<br>HA1-5144-2<br>HA1-5144-5   | Yes<br>Yes<br>Yes  | FE<br>FE<br>FE   | Enhanced ACs<br>Enhanced ACs<br>Enhanced ACs   |
| OP470AY<br>OP470EY<br>OP470FY<br>OP470GP<br>OP470GS  | HA1-5104-2<br>HA1-5104-5<br>HA1-5104-5<br>HA3-5104-5<br>HA9P5104-5   | Yes<br>Yes<br>Yes<br>Yes<br>Yes                          | FE<br>FE<br>FE<br>FE<br>FE   |  |
| OP47AD<br>OP47AT<br>OP47CD<br>OP47CT<br>OP47EN<br>OP47GN   | HA7-5147A-2<br>HA2-5147A-2<br>HA7-5147-2<br>HA2-5147-2<br>HA7-5147A-5 (CDIP)<br>HA7-5147-5 (CDIP)  | Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes                   | E<br>E<br>E<br>E<br>E<br>E   | Greater Bandwidth/Min Acl=10<br>Greater Bandwidth/Min Acl=10<br>Greater Bandwidth/Min Acl=10<br>Greater Bandwidth/Min Acl=10<br>Greater Bandwidth/Min Acl=10<br>Greater Bandwidth/Min Acl=10 |
| OP62AJ<br>OP62AZ<br>OP62EJ<br>OP62EZ<br>OP62FJ<br>OP62FZ   | HA2-5221-9<br>HA7-5221-9<br>HA2-5221-9<br>HA7-5221-9<br>HA2-5221-9<br>HA7-5221-9   | *<br>*<br>*<br>*<br>*<br>*                               | FE<br>FE<br>FE<br>FE<br>FE<br>FE                                     | Greater Slew Rate<br>Greater Slew Rate<br>Greater Slew Rate<br>Greater Slew Rate<br>Greater Slew Rate<br>Greater Slew Rate   |
| OP63AJ<br>OP63AZ<br>OP63EJ<br>OP63EZ<br>OP63FJ<br>OP63FZ<br>OP64AJ<br>OP64AZ<br>OP64EJ<br>OP64EZ<br>OP64FJ<br>OP64FZ | HA2-5221-9<br>HA7-5221-9<br>HA2-5221-9<br>HA7-5221-9<br>HA2-5221-9<br>HA7-5221-9<br>HA2-5221-9<br>HA7-5221-9<br>HA2-5221-9<br>HA7-5221-9<br>HA2-5221-9<br>HA7-5221-9 | *<br>*<br>*<br>*<br>*<br>*<br>*<br>*<br>*<br>*<br>*<br>* | FE<br>FE<br>FE<br>FE<br>FE<br>FE<br>FE<br>FE<br>FE<br>FE<br>FE<br>FE | Reduced Vio<br>Reduced Vio<br>Reduced Vio<br>Reduced Vio<br>Reduced Vio<br>Reduced Vio<br>Reduced Vio<br>Reduced Vio<br>Reduced Vio<br>Reduced Vio<br>Reduced Vio<br>Reduced Vio             |
| OP65AJ<br>OP65AZ<br>OP65EJ<br>OP65EZ<br>OP65FJ<br>OP65FZ   | HA2-2548-9<br>HA7-2548-9<br>HA2-2548-9<br>HA7-2548-9<br>HA2-2548-9<br>HA7-2548-9   | *<br>*<br>*<br>*<br>*<br>*                               | FE<br>FE<br>FE<br>FE<br>FE<br>FE                                     | Lower Vio/Guaranteed Ts<br>Lower Vio/Guaranteed Ts<br>Lower Vio/Guaranteed Ts<br>Lower Vio/Guaranteed Ts<br>Lower Vio/Guaranteed Ts<br>Lower Vio/Guaranteed Ts                               |
| OP65GP   | CA3450E  | No   | FE   | Greater Bandwidth /Slew Rate   |
| OP77BJ<br>OP77BZ<br>OP77FJ<br>OP77FZ   | HA2-5177-2<br>HA7-5177-2<br>HA2-5177-5<br>HA7-5177-5   | Yes<br>Yes<br>Yes<br>Yes                                 | FE<br>FE<br>FE<br>FE   | Greater Bandwidth/Reduced Icc<br>Greater Bandwidth/Reduced Icc<br>Greater Bandwidth/Reduced Icc<br>Greater Bandwidth/Reduced Icc   |

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| DEVICE   | HARRIS REPLACEMENT   | (Note 1)<br>PIN TO PIN                               | (Note 2)<br>EE                       | HARRIS ADVANTAGE OR COMMENTS   |
|--|--|--|--------------------------------------|--|
| OP80FJ<br>OP80GJ<br>OP80GP   | CA5420AT<br>CA5420T<br>CA5420E   | *<br>*<br>*  | FE<br>FE<br>FE                       | Single Supply Operation<br>Single Supply Operation<br>Single Supply Operation  |
| OPA121KP   | CA3140AE   | *  | FE                                   | MOS Input/Enhanced ACs   |
| OPA2111KM<br>OPA2111KP   | HA2-5102-5<br>HA3-5102-5   | Yes<br>Yes   | FE<br>FE                             | Greater Bandwidth<br>Greater Bandwidth   |
| OPA27AJ<br>OPA27AZ<br>OPA27CJ<br>OPA27CZ<br>OPA27EJ<br>OPA27EZ<br>OPA27GJ<br>OPA27GZ | HA2-5127A-2<br>HA7-5127A-2<br>HA2-5127-2<br>HA7-5127-2<br>HA2-5127A-5<br>HA7-5127A-5<br>HA2-5127-5<br>HA7-5127-5 | Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes | E<br>E<br>E<br>E<br>E<br>E<br>E<br>E | Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc |
| OPA37AJ<br>OPA37AZ<br>OPA37CJ<br>OPA37CZ<br>OPA37EJ<br>OPA37EZ<br>OPA37GJ<br>OPA37GZ | HA2-5137A-2<br>HA7-5137A-2<br>HA2-5137-2<br>HA7-5137-2<br>HA2-5137A-5<br>HA7-5137A-5<br>HA2-5137-5<br>HA7-5137-5 | Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes | E<br>E<br>E<br>E<br>E<br>E<br>E<br>E | Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc<br>Enhanced ACs/Reduced Icc |
| OPA404AG<br>OPA404BG<br>OPA404KP<br>OPA404KU<br>OPA404SG                             | HA1-5114-5<br>HA1-5114-5<br>HA3-5114-5<br>HA9P-5114-5<br>HA1-5114-2  | Yes<br>Yes<br>Yes<br>Yes<br>Yes                      | FE<br>FE<br>FE<br>FE<br>FE           | Lower Voltage Noise/Enhanced ACs<br>Lower Voltage Noise/Enhanced ACs<br>Lower Voltage Noise/Enhanced ACs<br>Lower Voltage Noise/Enhanced ACs<br>Lower Voltage Noise/Enhanced ACs   |
| OPA445AP<br>OPA445BM<br>OPA445SM   | HA7-2645-5<br>HA2-2640-2<br>HA2-2640-2   | Yes<br>Yes<br>Yes                                    | FE<br>FE<br>FE                       |  |
| OPA620KG<br>OPA620KP<br>OPA620LG<br>OPA620SG   | HFA7-0005-5<br>HFA3-0005-5<br>HFA7-0005-5<br>HFA7-0005-9   | *<br>*<br>*<br>*                                     | FE<br>FE<br>FE<br>FE                 | Enhanced ACs<br>Enhanced ACs<br>Enhanced ACs<br>Enhanced ACs   |
| OPA621KG<br>OPA621KP<br>OPA621LG<br>OPA621SG   | HFA7-0002-5<br>HFA3-0002-5<br>HFA7-0002-5<br>HFA7-0002-9   | *<br>*<br>*<br>*                                     | FE<br>FE<br>FE<br>FE                 | Lower Voltage Noise/Temco<br>Lower Voltage Noise/Temco<br>Lower Voltage Noise/Temco<br>Lower Voltage Noise/Temco   |
| OPA633AH<br>OPA633KP<br>OPA633SH   | HA2-5033-2<br>HA3-5033-5<br>HA2-5033-5   | Yes<br>Yes<br>Yes                                    | I<br>I<br>FE                         |  |
| RC3403AN   | CA5470E  | Yes  | FE                                   | MOS Input/Enhanced ACs   |

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GENERAL INFORMATION

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## Commercial Linear Product Cross Reference

| DEVICE                                     | HARRIS REPLACEMENT                                   | (Note 1)<br>PIN TO PIN   | (Note 2)<br>EE       | HARRIS ADVANTAGE OR COMMENTS  |
|--|--|--------------------------|----------------------|---|
| RC4741D<br>RC4741M                         | HA1-4741-2<br>HA9P-4741-5                            | Yes<br>Yes               | E<br>E               | Guaranteed ACs<br>Guaranteed ACs                                    |
| RC5532AN<br>RC5532N                        | HA3-5102-5<br>HA3-5102-5                             | Yes<br>Yes               | FE<br>FE             | Enhanced DCs/Reduced Icc<br>Enhanced DCs/Reduced Icc                |
| RC5534AN<br>RC5534N<br>RM5534T             | HA3-5101-5<br>HA3-5101-5<br>HA2-5101-2               | *<br>*<br>*              | FE<br>FE<br>FE       | Enhanced DCs/Reduced Icc<br>Enhanced DCs/Reduced Icc<br>Reduced Icc |
| RM5532AD<br>RM5532AT<br>RM5532D<br>RM5532T | HA7-5102-2<br>HA2-5102-2<br>HA7-5102-2<br>HA2-5102-2 | Yes<br>Yes<br>Yes<br>Yes | FE<br>FE<br>FE<br>FE | Reduced Icc<br>Reduced Icc<br>Reduced Icc<br>Reduced Icc            |
| RM5534AD<br>RM5534AT<br>RM5534D            | HA7-5101-2<br>HA2-5101-2<br>HA7-5101-2               | *<br>*<br>*              | FE<br>FE<br>FE       | Reduced Icc<br>Reduced Icc<br>Reduced Icc                           |
| SA5230N                                    | CA5160AE   | No                       | FE                   | MOS Input   |
| SA556-1N<br>SA556N                         | ICM7556IPD<br>ICM7556IPD                             | Yes<br>Yes               | FE<br>FE             | CMOS/Reduced Icc<br>CMOS/Reduced Icc                                |
| SA723CN                                    | CA0723CE   | Yes                      | I                    |   |
| SE5532AFE<br>SE5532FE                      | HA7-5102-2<br>HA7-5102-2                             | Yes<br>Yes               | FE<br>FE             | Reduced Icc<br>Reduced Icc  |
| SE5534AFE<br>SE5534FE                      | HA7-5101-2<br>HA7-5101-2                             | *<br>*                   | FE<br>FE             | Reduced Ibias/Iio<br>Reduced Ibias/Iio                              |
| SE5539F                                    | HA1-2539-2   | *                        | FE                   | Specified @ +/- 15V Supplies  |
| SE556-1CN<br>SE556-1F<br>SE556F            | ICM7556MJD<br>ICM7556MJD<br>ICM7556MJD               | Yes<br>Yes<br>Yes        | FE<br>FE<br>FE       | CMOS/Reduced Icc<br>CMOS/Reduced Icc<br>CMOS/Reduced Icc            |
| SG1524CF<br>SG1524CN<br>SG1524J            | CA1524F<br>CA1524E<br>CA1524F                        | Yes<br>Yes<br>Yes        | FE<br>FE<br>I        |   |
| SG1536T<br>SG1536Y                         | HA2-2640-2<br>HA7-2640-2                             | *<br>*                   | FE<br>FE             | Reduced Vio/Enhanced ACs<br>Reduced Vio/Enhanced ACs                |
| SG2524CF<br>SG2524CN<br>SG2524J            | CA2524F<br>CA2524E<br>CA2524F                        | Yes<br>Yes<br>Yes        | FE<br>FE<br>I        |   |
| SG3045J                                    | CA3045F  | Yes                      | FE                   |   |
| SG3049T                                    | CA3049T  | Yes                      | FE                   | Greater Bandwidth/Reduced Noise                                     |
| SG3083                                     | CA3083   | Yes                      | I                    |   |

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# Commercial Linear Product Cross Reference

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|--|---|--------------------------|-----------------------|---|
| SG3183D<br>SG3183N                                       | CA3183M<br>CA3183E  | Yes<br>Yes               | FE<br>FE              | Identical Specs @ 25 degrees C<br>Identical Specs @ 25 degrees C  |
| SG3524CF<br>SG3524CN<br>SG3524J<br>SG3524N               | CA3524F<br>CA3524E<br>CA3524F<br>CA3524E                                | Yes<br>Yes<br>Yes<br>Yes | FE<br>FE<br>I<br>I    |   |
| SG723CN<br>SG723CT<br>SG723N<br>SG723T                   | CA0723CE<br>CA0723CT<br>CA0723E<br>CA0723T                              | Yes<br>Yes<br>Yes<br>Yes | FE<br>FE<br>FE<br>FE  | Vin Slightly Different<br>Vin Slightly Different<br>Vin Slightly Different<br>Vin Slightly Different  |
| SHC5320KH<br>SHC5320SH                                   | HA1-5320-5<br>HA1-5320-2  | Yes<br>Yes               | I<br>I                |   |
| SHC85  | HA1-2425-5  | No                       | FE                    | Enhanced ACs  |
| SHC85ET  | HA1-2420-2  | No                       | FE                    | Enhanced ACs  |
| SHM-20C<br>SHM-20M                                       | HA1-5320-5<br>HA1-5320-2  | Yes<br>Yes               | FE<br>FE              | Guaranteed Acquisition Time<br>Guaranteed Acquisition Time  |
| SHM-IC-1   | HA1-2425-5  | Yes                      | FE                    | Almost Identical  |
| SHM-IC-1M  | HA1-2420-2  | Yes                      | FE                    | Almost Identical  |
| SI7660AA<br>SI7660BA<br>SI7660CA<br>SI7660CJ<br>SI7660DY | ICL7660SMTV<br>ICL7660SITV<br>ICL7660SCTV<br>ICL7660SCPA<br>ICL7660SIBA | *<br>*<br>*<br>*<br>*    | E<br>E<br>E<br>E<br>E | Greater Vout Efficiency/Reduced Icc<br>Greater Vout Efficiency/Reduced Icc<br>Greater Vout Efficiency/Reduced Icc<br>Greater Vout Efficiency/Reduced Icc<br>Greater Vout Efficiency/Reduced Icc |
| SI7661AA<br>SI7661CA<br>SI7661CJ                         | ICL7662MTV<br>ICL7662CTV<br>ICL7662CPA                                  | Yes<br>Yes<br>Yes        | E<br>E<br>E           | Reduced Supply Current<br>Reduced Supply Current<br>Reduced Supply Current  |
| SL3045C-DG   | CA3045F   | Yes                      | FE                    |   |
| SL3046C-DP   | CA3046E   | Yes                      | FE                    |   |
| SL3127C-DC<br>SL3127C-DP                                 | CA3127F<br>CA3127E  | Yes<br>Yes               | FE<br>FE              | SOIC Version Available  |
| SL3145C-DC<br>SL3145C-DP                                 | CA3045F<br>CA3046E  | Yes<br>Yes               | FE<br>FE              |   |
| SL3227-DP<br>SL3227-MP                                   | CA3227E<br>CA3227M  | Yes<br>Yes               | FE<br>FE              | Greater Breakdown Voltages<br>Greater Breakdown Voltages  |
| SL3245-DP<br>SL3245-MP                                   | CA3246E<br>CA3246M  | Yes<br>Yes               | FE<br>FE              | Greater Breakdown Voltages<br>Greater Breakdown Voltages  |
| SL6310C-DP   | CA3094E   | No                       | FE                    | Programmable Biasing Current  |

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GENERAL INFORMATION

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# Commercial Linear Product Cross Reference

| DEVICE                                   | HARRIS REPLACEMENT                                   | (Note 1)<br>PIN TO PIN | (Note 2)<br>EE       | HARRIS ADVANTAGE OR COMMENTS   |
|--|--|------------------------|----------------------|--|
| SMP10AY<br>SMP10BY<br>SMP10EY<br>SMP10FY | HA1-2420-2<br>HA1-2420-2<br>HA1-2425-5<br>HA1-2425-5 | *<br>*<br>*<br>*       | FE<br>FE<br>FE<br>FE | Faster Acquisition/Lower Droop<br>Faster Acquisition/Lower Droop<br>Faster Acquisition/Lower Droop<br>Faster Acquisition/Lower Droop |
| SMP11AY<br>SMP11BY<br>SMP11EY<br>SMP11FY | HA1-2420-2<br>HA1-2420-2<br>HA1-2425-5<br>HA1-2425-5 | *<br>*<br>*<br>*       | FE<br>FE<br>FE<br>FE | Faster Acquisition/Lower Droop<br>Faster Acquisition/Lower Droop<br>Faster Acquisition/Lower Droop<br>Faster Acquisition/Lower Droop |
| SP1-2541-2<br>SP1-2541-5                 | HA1-2541-2<br>HA1-2541-5                             | Yes<br>Yes             | I<br>I               |  |
| SP1-2542-2<br>SP1-2542-5                 | HA1-2542-2<br>HA1-2542-5                             | Yes<br>Yes             | I<br>I               |  |
| SP1-5330-2<br>SP1-5330-5                 | HA1-5330-2<br>HA1-5330-5                             | Yes<br>Yes             | I<br>I               |  |
| SP2-2500-2                               | HA2-2500-2   | Yes                    | I                    |  |
| SP2-2502-2                               | HA2-2502-2   | Yes                    | I                    |  |
| SP2-2505-5                               | HA2-2505-5   | Yes                    | I                    |  |
| SP2-2510-2                               | HA2-2510-2   | Yes                    | I                    |  |
| SP2-2512-2                               | HA2-2512-2   | Yes                    | I                    |  |
| SP2-2515-5                               | HA2-2515-5   | Yes                    | I                    |  |
| SP2-2520-2                               | HA2-2520-2   | Yes                    | I                    | Substitute HA2-2529-2  |
| SP2-2522-2                               | HA2-2522-2   | Yes                    | I                    | Substitute HA2-2529-2  |
| SP2-2525-5                               | HA2-2525-5   | Yes                    | I                    | Substitute HA2-2529-5  |
| SP2-2541-2<br>SP2-2541-5                 | HA2-2541-2<br>HA2-2541-5                             | Yes<br>Yes             | I<br>I               |  |
| SP2-2542-2<br>SP2-2542-5                 | HA2-2542-2<br>HA2-2542-5                             | Yes<br>Yes             | I<br>I               |  |
| SP2-2600-2                               | HA2-2600-2   | Yes                    | I                    |  |
| SP2-2602-2                               | HA2-2602-2   | Yes                    | I                    |  |
| SP2-2605-5                               | HA2-2605-5   | Yes                    | I                    |  |
| SP2-2620-2                               | HA2-2620-2   | Yes                    | I                    |  |
| SP2-2622-2                               | HA2-2622-2   | Yes                    | I                    |  |
| SP2-2625-5                               | HA2-2625-5   | Yes                    | I                    |  |
| SP3-2505-5                               | HA3-2505-5   | Yes                    | I                    |  |
| SP3-2515-5                               | HA3-2515-5   | Yes                    | I                    |  |

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# Commercial Linear Product Cross Reference

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|------------|--------------------|------------------------|----------------|---|
| SP3-2525-5 | HA3-2525-5         | Yes                    | I              | Substitute HA3-2529-5                                       |
| SP3-2542-5 | HA3-2542-5         | Yes                    | I              |   |
| SP3-2605-5 | HA3-2605-5         | Yes                    | I              |   |
| SP3-2625-5 | HA3-2625-5         | Yes                    | I              |   |
| SP7-2500-2 | HA7-2500-2         | Yes                    | I              |   |
| SP7-2502-2 | HA7-2502-2         | Yes                    | I              |   |
| SP7-2505-5 | HA7-2505-5         | Yes                    | I              |   |
| SP7-2510-2 | HA7-2510-2         | Yes                    | I              |   |
| SP7-2512-2 | HA7-2512-2         | Yes                    | I              |   |
| SP7-2515-5 | HA7-2515-5         | Yes                    | I              |   |
| SP7-2520-2 | HA7-2520-2         | Yes                    | I              | Substitute HA7-2529-2                                       |
| SP7-2522-2 | HA7-2522-2         | Yes                    | I              | Substitute HA7-2529-2                                       |
| SP7-2525-5 | HA7-2525-5         | Yes                    | I              | Substitute HA7-2529-5                                       |
| SP7-2600-2 | HA7-2600-2         | Yes                    | I              |   |
| SP7-2602-2 | HA7-2602-2         | Yes                    | I              |   |
| SP7-2605-5 | HA7-2605-5         | Yes                    | I              |   |
| SP7-2620-2 | HA7-2620-2         | Yes                    | I              |   |
| SP7-2622-2 | HA7-2622-2         | Yes                    | I              |   |
| SP7-2625-5 | HA7-2625-5         | Yes                    | I              |   |
| TA75393P   | CA3290AE/CA3290E   | Yes                    | FE             | Reduced I <sub>bias</sub> /I <sub>io</sub> /I <sub>cc</sub> |
| TA75557F   | HA9P5102-9         | No                     | FE             | Greater Bandwidth/Reduced Vnoise                            |
| TA75557P   | HA3-5102-5         | Yes                    | FE             | Greater Bandwidth/Reduced Vnoise                            |
| TA75559F   | HA9P5112-9         | No                     | FE             | Greater Bandwidth/Reduced Vnoise                            |
| TA75559P   | HA3-5112-5         | Yes                    | FE             | Greater Bandwidth/Reduced Vnoise                            |
| TA76524P   | CA3524E            | Yes                    | I              |   |
| TCA520BN   | CA5130AE           | *                      | FE             | MOS Input/Enhanced ACs                                      |
| TCA520TD   | CA5130M            | *                      | FE             | MOS Input/Enhanced ACs                                      |
| TCA971     | CA3146AE/CA3046E   | Yes                    | FE             | Greater V <sub>cb0</sub> With CA3146                        |
| TCA971G    | CA3146AM/CA3046M   | Yes                    | FE             | Greater V <sub>cb0</sub> With CA3146                        |
| TCA991     | CA3146E/CA3046E    | Yes                    | FE             | Greater V <sub>cb0</sub> With CA3146                        |
| TCA991G    | CA3146M/CA3046M    | Yes                    | FE             | Greater V <sub>cb0</sub> With CA3146                        |
| TD62507F   | CA3183AM           | No                     | FE             | Alt. Product Is CA3083                                      |
| TD62507P   | CA3183AE           | No                     | FE             | Alt. Product Is CA3083                                      |

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|--|--|---|--|--|
| TDB2046DP<br>TDB2046FP   | CA3046E<br>CA3046M   | Yes<br>Yes  | E<br>E   | Full -55 to 125 Degrees C Operation<br>Full -55 to 125 Degrees C Operation   |
| TLC251ACP<br>TLC251CP  | CA3440AE<br>CA3440E  | *<br>*  | FE<br>FE   |  |
| TLC252ACD<br>TLC252ACP<br>TLC252CD<br>TLC252CP   | CA5260AM<br>CA5260AE<br>CA5260M<br>CA5260E   | Yes<br>Yes<br>Yes<br>Yes                                    | FE<br>FE<br>FE<br>FE                               | Specified @ +5V Supply<br>Specified @ +5V Supply<br>Specified @ +5V Supply<br>Specified @ +5V Supply   |
| TLC254CD<br>TLC254CN   | CA5470M<br>CA5470E   | Yes<br>Yes  | FE<br>FE   | Specified @ +5V Supply<br>Specified @ +5V Supply   |
| TLC272ACD<br>TLC272ACP<br>TLC272AID<br>TLC272AIP<br>TLC272CD<br>TLC272CP<br>TLC272ID<br>TLC272IP<br>TLC272MJG          | CA5260AM<br>CA5260AE<br>CA5260AM<br>CA5260AE<br>CA5260M<br>CA5260E<br>CA5260M<br>CA5260E<br>CA5260E (PDIP) | Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes | FE<br>FE<br>FE<br>FE<br>FE<br>FE<br>FE<br>FE<br>FE | Greater Vout Range/Reduced Icc<br>Greater Vout Range/Reduced Icc<br>Greater Vout Range/Reduced Icc<br>Greater Vout Range/Reduced Icc<br>Greater Vout Range/Reduced Icc<br>Greater Vout Range/Reduced Icc<br>Greater Vout Range/Reduced Icc<br>Greater Vout Range/Reduced Icc<br>Greater Vout Range/Reduced Icc                   |
| TLC274CD<br>TLC274CN<br>TLC274ID<br>TLC274IN<br>TLC274MJ   | CA5470M<br>CA5470E<br>CA5470M<br>CA5470E<br>CA5470E (PDIP)   | Yes<br>Yes<br>Yes<br>Yes<br>Yes                             | FE<br>FE<br>FE<br>FE<br>FE                         | Greater Vout/Bandwidth/Slew Rate<br>Greater Vout/Bandwidth/Slew Rate<br>Greater Vout/Bandwidth/Slew Rate<br>Greater Vout/Bandwidth/Slew Rate<br>Greater Vout/Bandwidth/Slew Rate   |
| TLC27M2ACD<br>TLC27M2ACP<br>TLC27M2AID<br>TLC27M2AIP<br>TLC27M2CD<br>TLC27M2CP<br>TLC27M2ID<br>TLC27M2IP<br>TLC27M2MJG | CA5260AM<br>CA5260AE<br>CA5260AM<br>CA5260AE<br>CA5260M<br>CA5260E<br>CA5260M<br>CA5260E<br>CA5260E (PDIP) | Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes | FE<br>FE<br>FE<br>FE<br>FE<br>FE<br>FE<br>FE<br>FE | Greater Vout/Bandwidth/Slew Rate<br>Greater Vout/Bandwidth/Slew Rate<br>Greater Vout/Bandwidth/Slew Rate<br>Greater Vout/Bandwidth/Slew Rate<br>Greater Vout/Bandwidth/Slew Rate<br>Greater Vout/Bandwidth/Slew Rate<br>Greater Vout/Bandwidth/Slew Rate<br>Greater Vout/Bandwidth/Slew Rate<br>Greater Vout/Bandwidth/Slew Rate |
| TLC555CD<br>TLC555IP   | ICM7555CBA<br>ICM7555IPA   | Yes<br>Yes  | FE<br>FE   | Reduced Icc<br>Reduced Icc   |
| TLC556CN<br>TLC556IN<br>TLC556MJ   | ICM7556IPD<br>ICM7556IPD<br>ICM7556MJ  | Yes<br>Yes<br>Yes   | FE<br>FE<br>FE                                     | Reduced Icc<br>Reduced Icc<br>Reduced Icc  |
| TP1321   | HA-5195  | Yes   | FE   |  |
| TP1322   | HA-2520  | Yes   | FE   |  |
| TP1326   | HA-2600  | Yes   | FE   |  |
| TP1332   | HA-2645  | Yes   | FE   |  |

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**1**  
GENERAL  
INFORMATION

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|---|---|---|---|--|
| TP1339  | HA-2620   | No  | FE  |  |
| TP1341  | HA-2540   | Yes   | FE  |  |
| TP1342  | HA-2539   | Yes   | FE  |  |
| TP1344  | HA-5160   | Yes   | FE  |  |
| TP1345  | HA-5162   | Yes   | FE  |  |
| TP1346  | H1-5180   | Yes   |   |  |
| TP4856  | HA1-2420/25   | Yes   | I   | Guaranteed Acquisition Time  |
| TP4866  | HA1-5320  | Yes   | FE  | Guaranteed Acquisition Time  |
| TSC426CBA<br>TSC426CPA<br>TSC426IJA<br>TSC426MJA  | ICL7667CBA<br>ICL7667CPA<br>ICL7667CJA<br>ICL7667MJA  | Yes<br>Yes<br>Yes<br>Yes                                    | FE<br>FE<br>FE<br>FE                      | Reduced T Delay/Icc<br>Faster Switching<br>Reduced T Delay/Icc<br>Faster Switching   |
| TSC7650ACPA<br>TSC7650ACPD<br>TSC7650AIJA<br>TSC7650AIJD  | ICL7650SCPA-1<br>ICL7650SCPD<br>ICL7650SIJA-1<br>ICL7650SIJD  | Yes<br>Yes<br>Yes<br>Yes                                    | FE<br>FE<br>FE<br>FE                      | Reduced Tempco/Voltage Noise<br>Reduced Tempco/Voltage Noise<br>Reduced Tempco/Voltage Noise<br>Reduced Tempco/Voltage Noise |
| TSC7660CAA<br>TSC7660CPA  | ICL7660SCBA<br>ICL7660SCPA  | Yes<br>Yes  | E<br>E                                    | Greater Vout Efficiency/Reduced Icc<br>Greater Vout Efficiency/Reduced Icc   |
| TSC7662   | ICL7662   | *   | FE  |  |
| UA723CDP<br>UA723CH<br>uA723CN<br>uA723CN<br>UA723IDP<br>UA723IH<br>UA723MDP<br>UA723MH<br>uA723N | CA0723CE<br>CA0723CT<br>CA0723CE<br>CA0723CE<br>CA0723CE<br>CA0723CT<br>CA0723E<br>CA0723T<br>CA0723E | Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes<br>Yes | I<br>I<br>I<br>I<br>I<br>I<br>I<br>I<br>I |  |
| UC0P01CN<br>UC0P01GJ  | CA3140AE<br>CA3140AE (PDIP)   | Yes<br>Yes  | FE<br>FE                                  | MOSFET Input<br>MOSFET Input   |
| UC1524J   | CA1524F   | Yes   | I   |  |
| UC2524J<br>UC2524N  | CA2524F<br>CA2524E  | Yes<br>Yes  | I<br>I                                    |  |
| UC3524J<br>UC3524N  | CA3524F<br>CA3524E  | Yes<br>Yes  | I<br>I                                    |  |
| ULN2046A-1<br>ULN2046L-1  | CA3146E<br>CA3146M  | Yes<br>Yes  | FE<br>FE                                  | Full -40 to 85 Degree C Operation  |

NOTES: 1. A "\*" in this column indicates that primary pins are pin-to-pin, but secondary or optional function pins are not.  
 2. Electrical equivalency; denoted by the following: I = Identical, FE = Functional Equivalent, E = Enhanced Harris product meets all competitor specifications and exceeds several.

# Commercial Linear Product Cross Reference

| DEVICE  | HARRIS REPLACEMENT   | (Note 1)<br>PIN TO PIN     | (Note 2)<br>EE                   | HARRIS ADVANTAGE OR COMMENTS   |
|---|--|----------------------------|----------------------------------|--|
| ULN2083A<br>ULN2083A-1<br>ULN2083L  | CA3083<br>CA3183E<br>CA3083M   | Yes<br>Yes<br>Yes          | I<br>I<br>I                      | Full -55 to 125 Degree C Operation<br>Full -40 to 85 Degree C Operation<br>Full -55 to 125 Degree C Operation  |
| ULN2086A  | CA3086   | Yes                        | I                                | Full -55 to 125 Degree C Operation   |
| uPC357C   | CA3130E  | Yes                        | FE                               | Reduced I <sub>bias</sub>  |
| uPC4741C<br>uPC4741G2   | HA3-4741-5<br>HA9P4741-5   | Yes<br>*                   | E<br>E                           | Guaranteed Specs Over Temp<br>Guaranteed Specs Over Temp   |
| uPD5555C  | ICM7555CPA   | Yes                        | FE                               | Reduced I <sub>cc</sub>  |
| uPD5556C  | ICM7556CPD   | Yes                        | FE                               | Reduced I <sub>cc</sub>  |
| VI-7660-1<br>VI-7660-2  | ICL7660SCPA<br>ICL7660SCTV   | *<br>*                     | E<br>E                           | Greater V <sub>out</sub> Efficiency/Reduced I <sub>cc</sub><br>Greater V <sub>out</sub> Efficiency/Reduced I <sub>cc</sub>   |
| XR-13600AP<br>XR-13600CP  | CA3280AE<br>CA3280E  | No<br>No                   | FE<br>FE                         | Reduced V <sub>io</sub> /Enhanced ACs<br>Reduced V <sub>io</sub> /Enhanced ACs   |
| XR-1524M  | CA1524F  | Yes                        | I                                |  |
| XR-2242CP   | ICM7242IPA   | Yes                        | FE                               | Greatly Reduced I <sub>cc</sub>  |
| XR-2524N<br>XR-2524P  | CA2524F<br>CA2524E   | Yes<br>Yes                 | I<br>I                           |  |
| XR-3403CP   | CA5470E  | Yes                        | FE                               | MOS Input/Enhanced ACs   |
| XR-3524N<br>XR-3524P  | CA3524F<br>CA3524E   | Yes<br>Yes                 | I<br>I                           |  |
| XR-4739CN<br>XR-4739CP  | HA7-5102-5<br>HA3-5102-5   | No<br>No                   | FE<br>FE                         | Enhanced ACs/DCs<br>Enhanced ACs/DCs   |
| XR-4741CN<br>XR-4741CP<br>XR-4741M  | HA1-4741-5<br>HA3-4741-5<br>HA1-4741-2   | Yes<br>Yes<br>Yes          | E<br>E<br>E                      | Guaranteed Channel Separation<br>Guaranteed Channel Separation<br>Guaranteed Channel Separation  |
| XR-5532AN<br>XR-5532AP<br>XR-5532N<br>XR-5532P                              | HA7-5102-5<br>HA3-5102-5<br>HA7-5102-5<br>HA3-5102-5                             | Yes<br>Yes<br>Yes<br>Yes   | FE<br>FE<br>FE<br>FE             | Reduced V <sub>io</sub> /I <sub>bias</sub><br>Reduced V <sub>io</sub> /I <sub>bias</sub><br>Reduced V <sub>io</sub> /I <sub>bias</sub><br>Reduced V <sub>io</sub> /I <sub>bias</sub>   |
| XR-5534ACN<br>XR-5534ACP<br>XR-5534AM<br>XR-5534CN<br>XR-5534CP<br>XR-5534M | HA7-5101-5<br>HA3-5101-5<br>HA7-5101-2<br>HA7-5101-5<br>HA3-5101-5<br>HA7-5101-2 | *<br>*<br>*<br>*<br>*<br>* | FE<br>FE<br>FE<br>FE<br>FE<br>FE | Greater Av <sub>ol</sub> /Reduced V <sub>io</sub><br>Greater Av <sub>ol</sub> /Reduced V <sub>io</sub><br>Greater Av <sub>ol</sub><br>Greater Av <sub>ol</sub> /Reduced V <sub>io</sub><br>Greater Av <sub>ol</sub> /Reduced V <sub>io</sub><br>Greater Av <sub>ol</sub> |
| XR-8038CN<br>XR-8038CP<br>XR-8038M<br>XR-8038N                              | ICL8038CCJD<br>ICL8038CCPD<br>ICL8038AMJD<br>ICL8038BCJD                         | Yes<br>Yes<br>Yes<br>Yes   | FE<br>FE<br>FE<br>FE             | Reduced Supply Current<br>Reduced Supply Current<br>Reduced Supply Current<br>Reduced Supply Current   |

NOTES: 1. A "\*" in this column indicates that primary pins are pin-to-pin, but secondary or optional function pins are not.

2. Electrical equivalency; denoted by the following: I = Identical, FE = Functional Equivalent, E = Enhanced Harris product meets all competitor specifications and exceeds several.

# Data Acquisition Products

## A/D CONVERTERS DISPLAY

|                  |  |
|------------------|--|
| CA3162/CA3162A   | A/D Converter for 3½-Digit Display                   |
| ICL71C03/ICL8052 | Precision 4½-Digit A/D Converter                     |
| ICL71C03/ICL8068 | Precision 4½-Digit A/D Converter                     |
| ICL7106          | 3½-Digit LCD Single-Chip A/D Converter               |
| ICL7107          | 3½-Digit LED Single-Chip A/D Converter               |
| ICL7116          | 3½-Digit with Display Hold Single-Chip A/D Converter |
| ICL7117          | 3½-Digit with Display Hold Single-Chip A/D Converter |
| ICL7126          | 3½-Digit Low Power Single-Chip A/D Converter         |
| ICL7129          | 4½-Digit LCD Single-Chip A/D Converter               |
| ICL7136          | 3½-Digit LCD Low Power A/D Converter                 |
| ICL7137          | 3½-Digit LED Low Power Single-Chip A/D Converter     |
| ICL7139          | 3¾-Digit Autoranging Multimeter                      |
| ICL7149          | Low Cost 3¾-Digit Autoranging Multimeter             |
| ICL7182          | 101 Segment LCD Bargraph A/D Converter               |

## A/D CONVERTERS INTEGRATING

|                 |   |
|-----------------|---|
| HI-7159         | Microprocessor-Compatible 5½-Digit A/D Converter  |
| ICL7104/ICL8052 | 14/16-Bit $\mu$ P-Compatible 2-Chip A/D Converter |
| ICL7104/ICL8068 | 14/16-Bit $\mu$ P-Compatible 2-Chip A/D Converter |
| ICL7109         | 12-Bit $\mu$ P-Compatible A/D Converter           |
| ICL7135         | 4½-Digit BCD Output A/D Converter                 |

## A/D SUCCESSIVE APPROXIMATION

|                |   |
|----------------|---|
| ADC0802        | 8-Bit $\mu$ P-Compatible A/D Converter                                  |
| ADC0803        | 8-Bit $\mu$ P-Compatible A/D Converter                                  |
| ADC0804        | 8-Bit $\mu$ P-Compatible A/D Converter                                  |
| CA3310/CA3310A | CMOS 10-Bit A/D Converter with Internal Track and Hold                  |
| HI-574A        | Fast, Complete 12-Bit A/D Converter with Microprocessor Interface       |
| HI-674A        | 12 $\mu$ s, Complete 12-Bit A/D Converter with Microprocessor Interface |
| HI-774         | 8 $\mu$ s, Complete 12-Bit A/D Converter with Microprocessor Interface  |
| HI-7151        | 10-Bit High-Speed A/D Converter with Track and Hold                     |
| HI-7152        | 10-Bit High-Speed A/D Converter with Track and Hold                     |
| HI-7153        | 8-Channel 10-Bit High-Speed A/D Converter with Track and Hold           |
| ICL7112        | 12-Bit High-Speed CMOS $\mu$ P-Compatible A/D Converter                 |
| ICL7115        | 14-Bit High-Speed CMOS $\mu$ P-Compatible A/D Converter                 |

## A/D CONVERTERS FLASH

|         |  |
|---------|--|
| CA3304  | CMOS Video-Speed 4-Bit Flash A/D Converter |
| CA3306  | CMOS Video-Speed 6-Bit Flash A/D Converter |
| CA3318  | CMOS Video-Speed 8-Bit Flash A/D Converter |
| HI-5700 | 8-Bit, 20MSPS Flash A/D Converter          |

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## Data Acquisition Products (Continued)

### D/A CONVERTERS

|                  |  |
|------------------|--|
| AD7520           | 10/12-Bit Multiplying D/A Converter                        |
| AD7521           | 10/12-Bit Multiplying D/A Converter                        |
| AD7530           | 10/12-Bit Multiplying D/A Converter                        |
| AD7531           | 10/12-Bit Multiplying D/A Converter                        |
| AD7523           | 8-Bit Multiplying D/A Converter                            |
| AD7533           | 10-Bit Multiplying D/A Converter                           |
| AD7541           | 12-Bit Multiplying D/A Converter                           |
| AD7545           | 12-Bit Buffered Multiplying CMOS DAC                       |
| CA3338           | CMOS Video-Speed 8-Bit R-2R D/A Converter                  |
| HI-562A          | 12-Bit High-Speed Monolithic D/A Converter                 |
| HI-565A          | High-Speed Monolithic D/A Converter with Reference         |
| HI-DAC16B/DAC16C | 16-Bit D/A Converter                                       |
| HI-DAC80V        | 12-Bit, Low Cost, Monolithic D/A Converter                 |
| HI-DAC85V        | 12-Bit, Low Cost, Monolithic D/A Converter                 |
| ICL7121          | 16-Bit Multiplying Microprocessor-Compatible D/A Converter |
| ICL7134          | 14-Bit Multiplying $\mu$ P-Compatible D/A Converter        |

### ANALOG SWITCHES

|        |   |
|--------|---|
| DG180  | Dual SPST 10 Ohm High-Speed Driver with JFET Switch |
| DG181  | Dual SPST 30 Ohm High-Speed Driver with JFET Switch |
| DG182  | Dual SPST 75 Ohm High-Speed Driver with JFET Switch |
| DG183  | Dual DPST 10 Ohm High-Speed Driver with JFET Switch |
| DG184  | Dual DPST 30 Ohm High-Speed Driver with JFET Switch |
| DG185  | Dual DPST 75 Ohm High-Speed Driver with JFET Switch |
| DG186  | SPDT 10 Ohm High-Speed Driver with JFET Switch      |
| DG187  | SPDT 30 Ohm High-Speed Driver with JFET Switch      |
| DG188  | SPDT 75 Ohm High-Speed Driver with JFET Switch      |
| DG189  | Dual SPDT 10 Ohm High-Speed Driver with JFET Switch |
| DG190  | Dual SPDT 30 Ohm High-Speed Driver with JFET Switch |
| DG191  | Dual SPDT 75 Ohm High-Speed Driver with JFET Switch |
| DG200  | Dual SPST CMOS Analog Switch                        |
| DG201  | Quad SPST CMOS Analog Switch                        |
| DG201A | Quad Monolithic SPST CMOS Analog Switch             |
| DG202  | Quad Monolithic SPST CMOS Analog Switch             |
| DG211  | Quad Monolithic SPST CMOS Analog Switch             |
| DG212  | Quad Monolithic SPST CMOS Analog Switch             |
| DG300A | Dual SPST TTL Compatible CMOS Analog Switch         |
| DG301A | SPDT TTL Compatible CMOS Analog Switch              |
| DG302A | Dual DPST TTL Compatible CMOS Analog Switch         |
| DG303A | Dual SPDT TTL Compatible CMOS Analog Switch         |
| DG308A | Quad Monolithic SPST CMOS Analog Switch             |
| DG309  | Quad Monolithic SPST CMOS Analog Switch             |

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# Data Acquisition Products (Continued)

## ANALOG SWITCHES (Continued)

|          |   |
|----------|---|
| HI-200   | Dual SPST CMOS Analog Switch                |
| HI-201   | Quad SPST CMOS Analog Switch                |
| HI-201HS | High-Speed Quad SPST CMOS Analog Switch     |
| HI-222   | High Frequency Video Switch                 |
| HI-300   | Dual SPST CMOS Analog Switch                |
| HI-301   | SPDT CMOS Analog Switch                     |
| HI-302   | Dual DPST CMOS Analog Switch                |
| HI-303   | Dual SPDT CMOS Analog Switch                |
| HI-304   | Dual SPST CMOS Analog Switch                |
| HI-305   | SPDT CMOS Analog Switch                     |
| HI-306   | Dual DPST CMOS Analog Switch                |
| HI-307   | Dual SPDT CMOS Analog Switch                |
| HI-381   | Dual SPST CMOS Analog Switch                |
| HI-384   | Dual DPST CMOS Analog Switch                |
| HI-387   | SPDT CMOS Analog Switch                     |
| HI-390   | Dual SPDT CMOS Analog Switch                |
| HI-5040  | SPST CMOS Analog Switch                     |
| HI-5041  | Dual SPST CMOS Analog Switch                |
| HI-5042  | SPDT CMOS Analog Switch                     |
| HI-5043  | Dual SPDT CMOS Analog Switch                |
| HI-5044  | DPST CMOS Analog Switch                     |
| HI-5045  | Dual DPST CMOS Analog Switch                |
| HI-5046  | DPDT CMOS Analog Switch                     |
| HI-5046A | DPDT CMOS Analog Switch                     |
| HI-5047  | 4PST CMOS Analog Switch                     |
| HI-5047A | 4PST CMOS Analog Switch                     |
| HI-5048  | Dual SPST CMOS Analog Switch                |
| HI-5049  | Dual DPST CMOS Analog Switch                |
| HI-5050  | SPDT CMOS Analog Switch                     |
| HI-5051  | Dual SPDT CMOS Analog Switch                |
| IH401A   | Quad Varafet Analog Switch                  |
| IH5009   | Quad 100 Ohm Virtual Ground Analog Switch   |
| IH5010   | Quad 150 Ohm Virtual Ground Analog Switch   |
| IH5011   | Quad 100 Ohm Virtual Ground Analog Switch   |
| IH5012   | Quad 150 Ohm Virtual Ground Analog Switch   |
| IH5014   | Triple 150 Ohm Virtual Ground Analog Switch |
| IH5016   | Triple 150 Ohm Virtual Ground Analog Switch |
| IH5017   | Dual 100 Ohm Virtual Ground Analog Switch   |
| IH5018   | Dual 150 Ohm Virtual Ground Analog Switch   |
| IH5019   | Dual 100 Ohm Virtual Ground Analog Switch   |
| IH5020   | Dual 150 Ohm Virtual Ground Analog Switch   |
| IH5022   | Single 150 Ohm Virtual Ground Analog Switch |

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# Data Acquisition Products (Continued)

## ANALOG SWITCHES (Continued)

|        |  |
|--------|--|
| IH5024 | Single 150 Ohm Virtual Ground Analog Switch    |
| IH5040 | SPST 75 Ohm High-Level CMOS Analog Switch      |
| IH5041 | Dual SPST 75 Ohm High-Level CMOS Analog Switch |
| IH5042 | SPDT 75 Ohm High-Level CMOS Analog Switch      |
| IH5043 | Dual SPDT 75 Ohm High-Level CMOS Analog Switch |
| IH5044 | DPST 75 Ohm High-Level CMOS Analog Switch      |
| IH5045 | Dual DPST 75 Ohm High-Level CMOS Analog Switch |
| IH5046 | DPDT 75 Ohm High-Level CMOS Analog Switch      |
| IH5047 | 4PST 75 Ohm High-Level CMOS Analog Switch      |
| IH5052 | Quad SPST CMOS Analog Switch                   |
| IH5053 | Quad SPST CMOS Analog Switch                   |
| IH5140 | SPST High-Level CMOS Analog Switch             |
| IH5141 | Dual SPST High-Level CMOS Analog Switch        |
| IH5142 | SPDT High-Level CMOS Analog Switch             |
| IH5143 | Dual SPDT High-Level CMOS Analog Switch        |
| IH5144 | DPST High-Level CMOS Analog Switch             |
| IH5145 | Dual DPST High-Level CMOS Analog Switch        |
| IH5148 | Dual SPST High-Level CMOS Analog Switch        |
| IH5149 | Dual DPST High-Level CMOS Analog Switch        |
| IH5150 | SPDT High-Level CMOS Analog Switch             |
| IH5151 | Dual SPDT High-Level CMOS Analog Switch        |
| IH5341 | Dual SPST CMOS RF/Video Switch                 |
| IH5352 | Quad SPST CMOS RF/Video Switch                 |
| IH6201 | Dual CMOS Driver/Voltage Translator            |

## MULTIPLEXERS

|                |   |
|----------------|---|
| DG506A         | 16-Channel/Dual 8-Channel CMOS Analog Multiplexer   |
| DG507A         | 16-Channel/Dual 8-Channel CMOS Analog Multiplexer   |
| DG508A         | 8-Channel/Dual 4-Channel CMOS Analog Multiplexer  |
| DG509A         | 8-Channel/Dual 4-Channel CMOS Analog Multiplexer  |
| DG526          | 16-Channel/Dual 8-Channel CMOS Latchable Multiplexer  |
| DG527          | 16-Channel/Dual 8-Channel CMOS Latchable Multiplexer  |
| DG528          | 8-Channel/Dual 4-Channel Latchable Multiplexer  |
| DG529          | 8-Channel/Dual 4-Channel Latchable Multiplexer  |
| HI-1818A/1828A | Low Resistance Single 8/Differential 4-Channel CMOS Analog Multiplexers                     |
| HI-506         | Single 16/Differential 8-Channel CMOS Analog Multiplexer                                    |
| HI-507         | Single 16/Differential 8-Channel CMOS Analog Multiplexer                                    |
| HI-506A        | Single 16/Differential 8-Channel CMOS Analog Multiplexer with Active Overvoltage Protection |
| HI-507A        | Single 16/Differential 8-Channel CMOS Analog Multiplexer with Active Overvoltage Protection |

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# Data Acquisition Products (Continued)

## MULTIPLEXERS (Continued)

|         |   |
|---------|---|
| HI-508  | Single 8/Differential 4-Channel CMOS Analog Multiplexer                                     |
| HI-509  | Single 8/Differential 4-Channel CMOS Analog Multiplexer                                     |
| HI-508A | Single 8/Differential 4-Channel CMOS Analog Multiplexer with Active Overvoltage Protection  |
| HI-509A | Single 8/Differential 4-Channel CMOS Analog Multiplexer with Active Overvoltage Protection  |
| HI-516  | 16-Channel/Differential 8-Channel CMOS High-Speed Analog Multiplexer                        |
| HI-518  | 8-Channel/Differential 4-Channel CMOS High-Speed Analog Multiplexer                         |
| HI-524  | 4-Channel Wideband and Video Multiplexer  |
| HI-539  | Monolithic, 4-Channel, Low Level, Differential Multiplexer                                  |
| HI-546  | Single 16/Differential 8-Channel CMOS Analog Multiplexer with Active Overvoltage Protection |
| HI-547  | Single 16/Differential 8-Channel CMOS Analog Multiplexer with Active Overvoltage Protection |
| HI-548  | Single 8/Differential 4-Channel CMOS Analog Multiplexer with Active Overvoltage Protection  |
| HI-549  | Single 8/Differential 4-Channel CMOS Analog Multiplexer with Active Overvoltage Protection  |
| IH5108  | 8-Channel Fault Protected CMOS Analog Multiplexer   |
| IH5116  | 16-Channel Fault Protected CMOS Analog Multiplexer  |
| IH5208  | 4-Channel Differential Fault Protected CMOS Analog Multiplexer                              |
| IH5216  | 8-Channel Differential Fault Protected CMOS Analog Multiplexer                              |
| IH6108  | 8-Channel CMOS Analog Multiplexer   |
| IH6208  | 4-Channel Differential CMOS Analog Multiplexer  |

## DISPLAY DRIVERS

|         |   |
|---------|---|
| CA3161  | BCD to Seven Segment Decoder/Driver               |
| CA3168  | 2-Digit BCD to Seven Segment Decoder/Driver       |
| ICM7211 | 4-Digit LCD/LED Display Driver                    |
| ICM7212 | 4-Digit LCD/LED Display Driver                    |
| ICM7218 | 8-Digit LED Multiplexed Display Driver            |
| ICM7228 | 8-Digit LED Multiplexed Display Driver            |
| ICM7231 | Numeric/Alphanumeric Triplexed LCD Display Driver |
| ICM7232 | Numeric/Alphanumeric Triplexed LCD Display Driver |
| ICM7243 | 8-Character $\mu$ P-Compatible LED Display Driver |

## REAL-TIME CLOCK

|         |                                    |
|---------|------------------------------------|
| ICM7170 | $\mu$ P-Compatible Real-Time Clock |
|---------|------------------------------------|

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## Data Acquisition Products (Continued)

### COUNTERS WITH DISPLAY DRIVERS/TIMEBASE GENERATORS

|              |  |
|--------------|--|
| ICM7207/A    | CMOS Timebase Generator                          |
| ICM7208      | 7-Digit LED Display Counter                      |
| ICM7209      | Timebase Generator                               |
| ICM7213      | One Second/One Minute Timebase Generator         |
| ICM7216A/B/D | 8-Digit Multi-Function Frequency Counter/Timer   |
| ICM7217      | 4-Digit LED Display Programmable Up/Down Counter |
| ICM7224      | 4½-Digit LCD/LED Display Counter                 |
| ICM7225      | 4½-Digit LCD/LED Display Counter                 |
| ICM7226A/B   | 8-Digit Multi-Function Frequency Counter/Timer   |
| ICM7249      | 5½-Digit LCD $\mu$ -Power Event/Hour Meter       |

### SPECIAL PURPOSE

|         |  |
|---------|--|
| AD590   | 2-Wire Current Output Temperature Transducer |
| ICL8069 | Low Voltage Reference                        |

### DATA COMMUNICATIONS

|        |  |
|--------|--|
| ICL232 | +5 Volt Powered Dual RS-232 Transmitter/Receiver |
|--------|--|

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# Digital Signal Processing Products

## MULTIPLIERS

|             |  |
|-------------|--|
| HMA510      | 16 x 16-Bit CMOS Parallel Multiplier Accumulator |
| HMA510/883  | 16 x 16-Bit CMOS Parallel Multiplier Accumulator |
| HMU16/HMU17 | 16 x 16-Bit CMOS Parallel Multipliers            |
| HMU16/883   | 16 x 16-Bit CMOS Parallel Multiplier             |
| HMU17/883   | 16 x 16-Bit CMOS Parallel Multiplier             |

## ONE DIMENSIONAL FILTERS

|              |  |
|--------------|--|
| DECI • MATE  | Harris HSP43220 Decimating Digital Filter Development Software |
| HSP43168     | Dual FIR Filter  |
| HSP43220     | Decimating Digital Filter                                      |
| HSP43220/883 | Decimating Digital Filter                                      |
| HSP43481     | Digital Filter   |
| HSP43481/883 | Digital Filter   |
| HSP43881     | Digital Filter   |
| HSP43881/883 | Digital Filter   |
| HSP43891     | Digital Filter   |
| HSP43891/883 | Digital Filter   |

## TWO DIMENSIONAL FILTERS

|              |                           |
|--------------|---------------------------|
| HSP48901     | 3 x 3 Image Filter        |
| HSP48908     | Two Dimensional Convolver |
| HSP48908/833 | Two Dimensional Convolver |

## SIGNAL SYNTHESIZERS

|              |   |
|--------------|---|
| HSP45102     | 12 Bit Numerically Controlled Oscillator    |
| HSP45106     | 16 Bit Numerically Controlled Oscillator    |
| HSP45106/883 | 16 Bit Numerically Controlled Oscillator    |
| HSP45116     | Numerically Controlled Oscillator/Modulator |
| HSP45116/883 | Numerically Controlled Oscillator/Modulator |

## SPECIAL FUNCTION

|              |                          |
|--------------|--------------------------|
| HSP45240     | Address Sequencer        |
| HSP45240/883 | Address Sequencer        |
| HSP45256     | Binary Correlator        |
| HSP9501      | Programmable Data Buffer |
| HSP9520/9521 | Binary Correlator        |
| HSP9520/9521 | Binary Correlator        |

FOR MORE INFORMATION CONTACT YOUR  
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# Mixed Signal Products

## RADIO COMMUNICATION CIRCUITS

|         |                              |
|---------|------------------------------|
| CA 1523 | Vipur Switching Regulator    |
| CA 2111 | Radio FMIF                   |
| CA 3011 | Radio FMIF                   |
| CA 3012 | Radio FMIF                   |
| CA 3013 | Radio FMIF                   |
| CA 3014 | Radio FMIF                   |
| CA 3088 | AM Radio Multipurpose Array  |
| CA 3163 | Divide by 64/256 Prescaler   |
| CA 3209 | Radio FMIF                   |
| CA 3232 | Divide by 20                 |
| CA 3259 | Stereo Audio Tone/Volume     |
| CA 3263 | Op Amp Band Switch Amplifier |

## TRANSPORTATION AND INDUSTRIAL CIRCUITS

|         |  |
|---------|--|
| CA 3164 | Det/Alarm  |
| CA 3165 | Ignition Det/Switch                                    |
| CA 3169 | Half H Drive   |
| CA 3228 | Speed Control System                                   |
| CA 3242 | Quad Gated Inverting Power Driver                      |
| CA 3252 | Quad Gated Non-Inverting Power Driver                  |
| CA 3262 | Quad Gated Inverting Power Driver with Protection      |
| CA 3272 | Quad Gated Non-Inverting Power Driver with Diagnostics |
| CA 3273 | High Side Driver                                       |
| CA 3274 | Ignition Predriver                                     |
| CA 3275 | Dual H Driver  |
| CA 3276 | Dual Volt Regulator                                    |
| GS600   | Power Control/Motor Driver                             |
| GS601   | Power Control/Motor Driver                             |

## VIDEO/TV/CATV CIRCUITS

|         |  |
|---------|--|
| CA 3070 | Chroma Subcarrier Regen                          |
| CA 3154 | Horizontal Sync/AFC/Oscillator                   |
| CA 3202 | Horizontal/Vertical Count Down                   |
| CA 3210 | 525/625 Horizontal/Vertical Count Down           |
| CA 3218 | Horizontal/Vertical/Oscillator Count Down        |
| CA 3224 | Auto Line Bias Current                           |
| CA 3234 | Comp Video to RGB Chroma Luma Decoder            |
| CA 3236 | 525/625 Line, Horizontal/Vertical Count Down     |
| CA 3237 | IR Remote Control Amplifier                      |
| CA 3241 | Horizontal/Vertical Count Down                   |
| CA 3247 | Analog Interface Unit                            |
| CA 3253 | Camera Video Processor                           |
| CA 3254 | RS170 Synch Generator with Gen/Lock/Line/Lock    |
| CA 3255 | 625 Line Synch Generator with Gen/Lock/Line/Lock |
| CA 3261 | Horizontal Processor                             |

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## POWER PROCESSING CIRCUITS

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NOTE: Bold type designates a new product from Harris.

# Selection Guide

## POWER PROCESSING CIRCUITS

| TYPE  | FUNCTION  | DESCRIPTION  | PIN COUNT<br>PACKAGE                  |
|---|---|--|---------------------------------------|
| <b>CONVERTERS</b>                                     |   |  |                                       |
| ICL644/645/<br>646/647/<br>ICL7644/7645/<br>7646/7647 | Low Voltage Step-Up<br>Converters                           | Designed to provide 3V or 5V output from a single 1.5V battery (645 and 7645) use two cells. Low quiescent current coupled with low start up voltage, insure long battery life.  | 14/PDIP<br>14/SOIC                    |
| ICL7660S  | Voltage Converter   | Performs supply voltage conversion from positive to negative. Input range is +1.5V to +10V resulting in complementary output voltages of -1.5V to -12V. Can be connected as a voltage doubler to generate output voltage of -18.6V. T <sub>A</sub> Range: 0°C to +70°C, -55°C to +125°C. ICL7660S improved version of ICL7660. Has extended supply voltage range, lower supply current, and ESD protection (>2000V). | 8/SOIC,<br>8/PDIP<br>8/TO-99          |
| ICL7662S  | Voltage Converter   | Similar to the ICL7660S in its operation, except the output voltages are -4.5V to -20V. Doubler output 22.6V.  | 8/PDIP<br>8/TO-99                     |
| <b>MOSFET DRIVERS</b>                                 |   |  |                                       |
| HV-250/255  | Power CMOS FET<br>Driver                                    | Complementary power MOSFET driver. Wide supply range (20V to 450V). High peak output current of 2A. High switching speed 200ns. New product in development.  | 16/CDIP<br>16/PDIP                    |
| HV-350/355  | Totem Pole N-Channel<br>Power MOSFET Driver                 | Totem pole n-channel power MOSFET driver. Wide supply range (20V to 450V). High peak output current of 2A. High switching speed of 200ns. New product in development.  | 16/CDIP<br>16/PDIP<br>16/SOIC         |
| HV-400  | High Speed MOSFET<br>Driver                                 | Single, non-inverting high speed driver (up to 300kHz) designed to drive large capacitive loads in 5,000pF to 100,000pF range. Capable of sourcing 6A and sinking 10A.   | 8/PDIP<br>8/CDIP<br>8/SOIC            |
| ICL7667   | Dual Power<br>MOSFET Driver                                 | TTL-compatible high-speed CMOS driver designed to provide high output current (1.5A) and voltage (up to +15V) for driving the gates of power MOSFETs in high-frequency switched-mode power converters. T <sub>A</sub> Range: 0°C to +70°C, -55°C to +125°C.  | 8/SOIC<br>8/PDIP<br>8/CDIP<br>8/TO-99 |
| <b>OFFLINE POWER SUPPLIES</b>                         |   |  |                                       |
| HV-1205   | 120VAC Offline<br>Monolithic Power<br>Supply                | AC to DC converter designed for 120VAC input. Output is capable of 5VDC to 24VDC @ 0mA to 50mA of current. This part is UL recognized (File# 130808) and UL listed.  | 8/PDIP                                |
| HV-2405   | 240VAC Offline<br>Monolithic Power<br>Supply                | AC to DC converter designed for 240VAC input. Output is capable of 5VDC to 24VDC @ 0mA to 50mA of current. This part is UL recognized (File# 130808) and UL listed.  | 8/PDIP                                |
| <b>REGULATORS</b>                                     |   |  |                                       |
| ICL7663S  | Programmable Micro-<br>Power Positive<br>Voltage Regulator  | Low-power, high-efficiency device (I <sub>o</sub> = 4μA max.) that accepts an input of 1 to 16V and provides an adjustable output over the same range at up to 40mA load. T <sub>A</sub> Range: 0°C to +70°C, -25°C to +85°C. Line and load regulation and ESD protection (>2000V).  | 8/SOIC<br>8/CDIP<br>8/PDIP<br>8/TO-99 |
| <b>VOLTAGE MONITORING CIRCUITS</b>                    |   |  |                                       |
| ICL7665S<br>ICL7665                                   | Programmable Micro-<br>Power Under/Over<br>Voltage Detector | Contains two individually programmable voltage comparators and requires only 3μA supply current. Intended for battery-operated systems that require low or high voltage warnings, etc. Open drain outputs for interfacing. T <sub>A</sub> Range: 0°C to +70°C, -25°C to +85°C. ICL7665S improved ICL7665. For features, see ICL7663S.  | 8/SOIC<br>8/CDIP<br>8/PDIP<br>8/TO-99 |
| ICL7673   | Automatic Battery<br>Backup Switch                          | Automatically switches between a main power supply (eg., +5V) and a battery back-up supply, when the main supply is removed. Wide supply range: 2.5V to T <sub>A</sub> Range: 0°C to +70°C, -25°C to +85°C.  | 8/SOIC<br>8/PDIP                      |
| ICL8211   | Programmable Voltage<br>Level Detector                      | Contains a 1.15V reference, a comparator, a hysteresis output and a non-inverting main-output. Provides a 7mA current-limited output sink when voltage on threshold terminal is <1.15V. T <sub>A</sub> Range: 0°C to +70°C, -55°C to +125°C.   | 8/SOIC<br>8/CDIP<br>8/PDIP<br>8/TO-99 |
| ICL8212   | Programmable Voltage<br>Level Detector                      | Similar in operation to the ICL8211 except that its main output is inverting as opposed to non-inverting. Requires a voltage in excess of 1.15V to switch its output current limit. T <sub>A</sub> Range: Same as ICL8211.   | 8/SOIC<br>8/PDIP<br>8/TO-99           |

# Selection Guide

## POWER PROCESSING CIRCUITS

| TYPE   | DESCRIPTION                             | V <sub>I</sub><br>RANGE<br>V   | V <sub>O</sub><br>RANGE<br>V   | I <sub>O</sub><br>(MAX)<br>mA                | LOAD<br>REGULATION<br>% V <sub>O</sub> (MAX) | V <sub>I</sub> - V <sub>O</sub><br>V<br>(MIN)                         | SHORT-CIRCUIT<br>CURRENT LIMIT<br>mA (TYP) | PIN COUNT<br>AND PACKAGE<br>TYPE* |
|--|---|--|--------------------------------|--|--|---|--|-----------------------------------|
| CA3085   | Voltage regulators                      | 7.5 to 30  | 1.8 to 26                      | 12**   | 0.1  | 4   | 96   | 8E, 8S                            |
| CA3085A  |   | 7.5 to 40  | 1.7 to 36                      | 100  | 0.15   | 4   | 96   | 8E, 8S                            |
| CA3085B  |   | 7.5 to 50  | 1.7 to 46                      | 100  | 0.15   | 3.5   | 96   | 8E, 8S                            |
| CA723  |   | 9.5 to 40  | 2 to 37                        | 150  | 0.03   | 3   | 65   | 10T, 14E                          |
| CA723C   |   | 9.5 to 40  | 2 to 37                        | 150  | 0.03   | 3   | 65   | 10T, 14E                          |
|  |   | **This value may be extended to 100mA; however, regulation is not specified beyond 12mA. Operating temperature range (T <sub>A</sub> ): -55 to +125°C. Electrical characteristics at T <sub>A</sub> = 25°C |                                |  |  |   |  |                                   |
| TYPE   | DESCRIPTION                             | V <sup>+</sup><br>RANGE<br>V   | V <sub>O</sub><br>RANGE<br>V   | LOAD<br>REGULATION<br>% V <sub>O</sub> (TYP) | RIPPLE<br>REJECTION<br>dB (TYP)              | TOTAL STANDBY<br>CURRENT I <sub>S</sub> (mA)<br>(MAX)                 | V <sub>CE SAT</sub><br>V<br>(TYP)          |                                   |
| CA1524<br>CA2524<br>CA3524   | Regulating<br>pulse-width<br>modulators | 8 to 40  | 4.8 to 5.2                     | 0.2  | 66   | 10  | 0.8  |                                   |
|  |   | 8 to 40  | 4.8 to 5.2                     | 0.2  | 66   | 10  | 0.8  |                                   |
|  |   | 8 to 40  | 4.6 to 5.4                     | 0.2  | 66   | 10  | 0.8  |                                   |
| Electrical characteristics at V <sup>+</sup> = 20V, f = 20kHz.<br>T <sub>A</sub> = -55 to +125°C for CA1524; 0 to +70°C for CA2524, CA3524. 16-lead dual-in-line (E) & (F) packages.<br>Short-circuit current limit: 100mA typ. Temperature stability: 1% max. |   |  |                                |  |  |   |  |                                   |
| TYPE   | DESCRIPTION                             | AC INPUT VOLTS<br>@ 50-60 & 400Hz<br>(VAC)   | MAX. DC<br>SUPPLY<br>VOLTS (V) | MAX. INPUT<br>CURRENT<br>(μA)                | SENSOR<br>RANGE (R <sub>x</sub> )<br>kΩ      | CONTROL CURRENT TO<br>THYRISTOR GATE<br>(mA)                          |  |                                   |
| CA3059   | Zero voltage<br>switches                | 24   | 14                             | 1  | 2 to 100                                     | Up to 124 with internal supply; up<br>to 240 with one external supply |  |                                   |
| CA3079   |   | 120  |                                |  |  |   |  |                                   |
|  |   | 208/230<br>277   | 10                             | 2  | 2 to 50                                      |   |  |                                   |
| Electrical characteristics at T <sub>A</sub> = 25°C. 14-lead dual-in-line plastic package (no suffix).<br>Operating temperature range (T <sub>A</sub> ): -55 to +125°C.  |   |  |                                |  |  |   |  |                                   |

\*See Packaging and Ordering Information in Section 12.



## Voltage Regulators Adjustable from 2V to 37V at Output Currents Up to 150mA Without External Pass Transistors

August 1991

### Features

- Up to 150mA Output Current
- Positive and Negative Voltage Regulation
- Regulation in Excess of 10A with Suitable Pass Transistors
- Input and Output Short-Circuit Protection
- Load and Line Regulation ..... 0.03%
- Direct Replacement for 723 and 723C Industry Types
- Adjustable Output Voltage ..... 2V to 37V

### Applications

- Series and Shunt Voltage Regulator
- Floating Regulator
- Switching Voltage Regulator
- High-Current Voltage Regulator
- Temperature Controller

### Description

The CA723 and CA723C are silicon monolithic integrated circuits designed for service as voltage regulators at output voltages ranging from 2V to 37V at currents up to 150 milliamperes.

Each type includes a temperature-compensated reference amplifier, an error amplifier, a power series pass transistor, and a current-limiting circuit. They also provide independently accessible inputs for adjustable current limiting and remote shutdown and, in addition, feature low standby current drain, low temperature drift, and high ripple rejection.

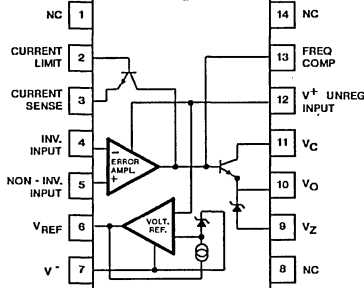
The CA723 and CA723C may be used with positive and negative power supplies in a wide variety of series, shunt, switching, and floating regulator applications. They can provide regulation at load currents greater than 150mA and in excess of 10A with the use of suitable n-p-n or p-n-p external pass transistors.

The CA723 and CA723C are supplied in the 10 lead TO-5 style package (T suffix), and the 14 lead dual-in-line plastic package (E suffix), and are direct replacements for industry types 723, 723C,  $\mu$ A723, and  $\mu$ A723C in packages with similar terminal arrangements. They are also available in chip form ("H" suffix).

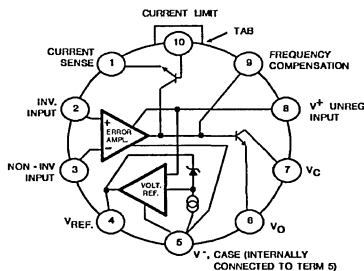
All types are rated for operation over the full military-temperature range of  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ .

### Pinouts

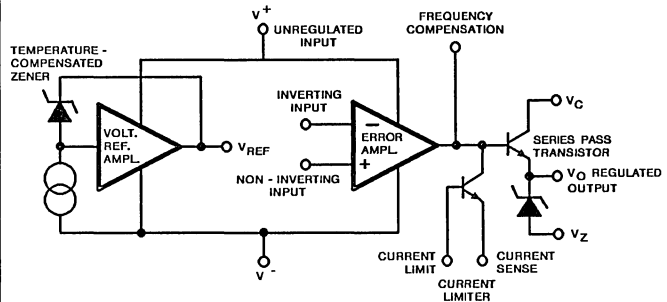
**E SUFFIX PACKAGE  
TOP VIEW**



**T SUFFIX PACKAGE  
TOP VIEW**



### Functional Block Diagram





# CA723, CA723C

## Absolute Maximum Ratings

|   |                 |
|---|-----------------|
| DC Supply Voltage (Between V+ and V- Terminals)                   | 40V             |
| Pulse Voltage for 50ms  |                 |
| Pulse Width (Between V+ and V- Terminals)                         | 50V             |
| Differential Input-Output Voltage                                 | 40V             |
| Differential Input Voltage  |                 |
| Between Inverting and Non-Inverting Inputs                        | ±5V             |
| Between Non-Inverting Input and V-                                | 8V              |
| Current From Zener Diode Terminal (V <sub>Z</sub> )               | 25mA            |
| Current From Voltage Reference Terminal (V <sub>REF</sub> )       | 15mA            |
| Device Dissipation  |                 |
| Up to T <sub>A</sub> = +25°C                                      |                 |
| CA723T, CA723CT   | 800mW           |
| CA723E, CA723CE   | 1000mW          |
| Above T <sub>A</sub> = +25°C                                      |                 |
| CA723T, CA723CT, Derate Linearly                                  | 6.3mW/°C        |
| CA723E, CA723CE, Derate Linearly                                  | 8.3mW/°C        |
| Ambient Temperature Range   |                 |
| Operating   | -55°C to +125°C |
| Storage   | -65°C to +150°C |
| Lead Temperature, During Soldering                                | +265°C          |
| At a distance 1/16" ± 1/32" (1.59 ± 0.79mm) from case for 10s max |                 |

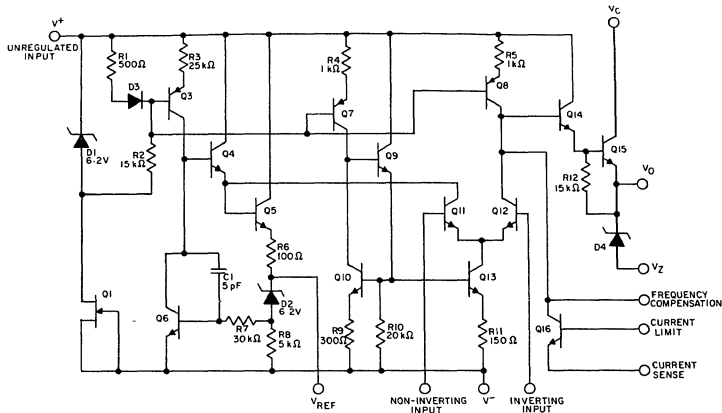


FIGURE 1. EQUIVALENT SCHEMATIC DIAGRAM OF THE CA723 AND CA723C

## CA723, CA723C

**ELECTRICAL CHARACTERISTICS** at  $T_A = 25\text{ C}$ ,  $V^+ = V_C = V_I = 12\text{ V}$ ,  $V^- = 0$ ,  $V_O = 5\text{ V}$ ,  
 $I_L = 1\text{ mA}$ ,  $C_1 = 100\text{ pF}$ ,  $C_{REF} = 0$ ,  $R_{SCP} = 0$ , unless otherwise specified. Divider  
impedance  $\frac{R_1 R_2}{R_1 + R_2}$  at non-inverting input, Term. 5, =  $10\text{ k}\Omega$  (See Figure 20)

| CHARACTERISTIC                                       | TEST CONDITIONS  | LIMITS |       |       |        |       |       | UNITS               |
|--|--|--------|-------|-------|--------|-------|-------|---------------------|
|  |  | CA723  |       |       | CA723C |       |       |                     |
|  |  | Min.   | Typ.  | Max.  | Min.   | Typ.  | Max.  |                     |
| Quiescent Regulator Current, $I_Q$                   | $I_L = 0$ ,<br>$V_I = 30\text{ V}$   | —      | 2.3   | 3.5   | —      | 2.3   | 4     | mA                  |
| Input Voltage Range, $V_I$                           |  | 9.5    | —     | 40    | 9.5    | —     | 40    | V                   |
| Output Voltage Range, $V_O$                          |  | 2      | —     | 37    | 2      | —     | 37    | V                   |
| Differential Input-Output Voltage, $V_I - V_O$       |  | 3      | —     | 38    | 3      | —     | 38    | V                   |
| Reference Voltage, $V_{REF}$                         |  | 6.95   | 7.15  | 7.35  | 6.8    | 7.15  | 7.5   | V                   |
| Line Regulation<br>(See Note 1)                      | $V_I = 12$<br>to $40\text{ V}$   | —      | 0.02  | 0.2   | —      | 0.1   | 0.5   | % $V_O$             |
|  | $V_I = 12$<br>to $15\text{ V}$   | —      | 0.01  | 0.1   | —      | 0.01  | 0.1   |                     |
|  | $V_I = 12$<br>to $15\text{ V}$ ,<br>$T_A = -55$ to<br>$+125^\circ\text{C}$     | —      | —     | 0.3   | —      | —     | —     |                     |
|  | $V_I = 12$<br>to $15\text{ V}$ ,<br>$T_A = 0$ to<br>$70^\circ\text{C}$         | —      | —     | —     | —      | —     | 0.3   |                     |
| Load Regulation<br>(See Note 1)                      | $I_L = 1$<br>to $50\text{ mA}$   | —      | 0.03  | 0.15  | —      | 0.03  | 0.2   | % $V_O$             |
|  | $I_L = 1$<br>to $50\text{ mA}$ ,<br>$T_A = -55$ to<br>$+125^\circ\text{C}$     | —      | —     | 0.6   | —      | —     | —     |                     |
|  | $I_L = 1$<br>to $50\text{ mA}$ ,<br>$T_A = 0$<br>to $70^\circ\text{C}$         | —      | —     | —     | —      | —     | 0.6   |                     |
| Output-Voltage<br>Temp. Coefficient,<br>$\Delta V_O$ | $T_A = -55$<br>to $+125^\circ\text{C}$   | —      | 0.002 | 0.015 | —      | —     | —     | %/ $^\circ\text{C}$ |
|  | $T_A = 0$<br>to $70^\circ\text{C}$   | —      | —     | —     | —      | 0.003 | 0.015 |                     |
| Ripple Rejection<br>(See Note 2)                     | $f = 50\text{ Hz}$<br>to $10\text{ kHz}$                                       | —      | 74    | —     | —      | 74    | —     | dB                  |
|  | $f = 50\text{ Hz}$ to<br>$10\text{ kHz}$ ,<br>$C_{REF} = 5\text{ }\mu\text{F}$ | —      | 86    | —     | —      | 86    | —     |                     |

# CA723, CA723C

## ELECTRICAL CHARACTERISTICS (Cont'd)

| CHARACTERISTIC   | TEST CONDITIONS                               | LIMITS |      |      |        |      |      | UNITS   |
|--|---|--------|------|------|--------|------|------|---------|
|  |   | CA723  |      |      | CA723C |      |      |         |
|  |   | Min.   | Typ. | Max. | Min.   | Typ. | Max. |         |
| Short-Circuit Limiting Current, $I_{LIM}$                  | $R_{SCP} = 10 \Omega$ ,<br>$V_O = 0$          | –      | 65   | –    | –      | 65   | –    | mA      |
| Equivalent Noise RMS Output Voltage, $V_N$<br>(See Note 2) | BW = 100 Hz to 10 kHz,<br>$C_{REF} = 0$       | –      | 20   | –    | –      | 20   | –    | $\mu V$ |
|  | BW = 100 Hz to 10 kHz,<br>$C_{REF} = 5 \mu F$ | –      | 2.5  | –    | –      | 2.5  | –    |         |

Note 1: Line and load regulation specifications are given for condition of a constant chip temperature. For high-dissipation condition, temperature drifts must be separately taken into account.

Note 2: For  $C_{REF}$  (See Figure 20).

## TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723

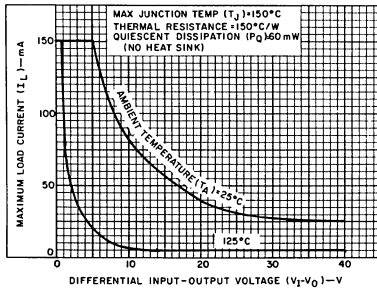


FIGURE 2. MAX LOAD CURRENT vs DIFFERENTIAL INPUT-OUTPUT VOLTAGE

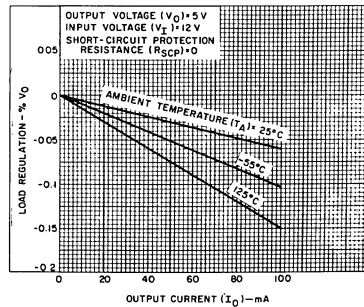


FIGURE 3. LOAD REGULATION WITHOUT CURRENT LIMITING

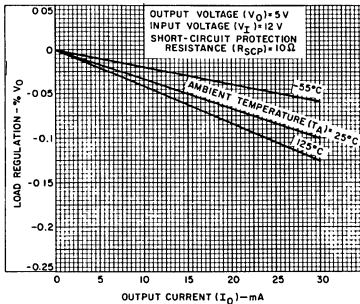


FIGURE 4. LOAD REGULATION WITH CURRENT LIMITING

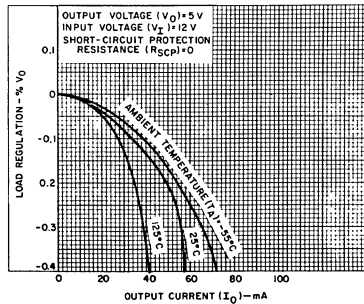


FIGURE 5. LOAD REGULATION WITH CURRENT LIMITING

# CA723, CA723C

## TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723 (Continued)

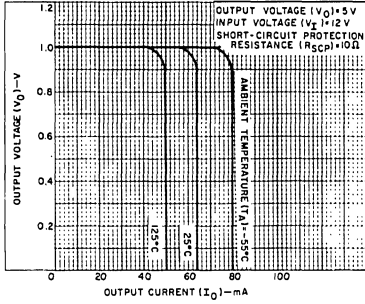


FIGURE 6. CURRENT LIMITING CHARACTERISTICS

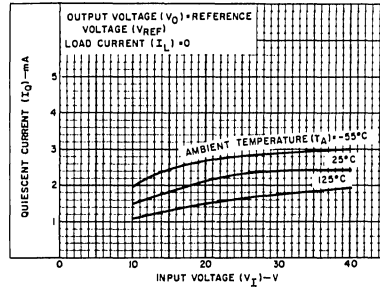


FIGURE 7. QUIESCENT CURRENT vs INPUT VOLTAGE

## TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723C

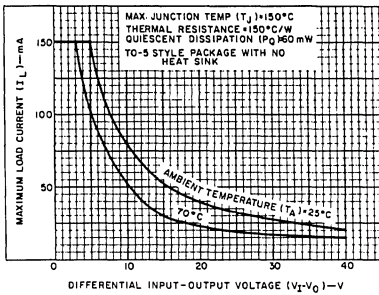


FIGURE 8. MAX LOAD CURRENT vs DIFFERENTIAL INPUT-OUTPUT VOLTAGE CA723CT

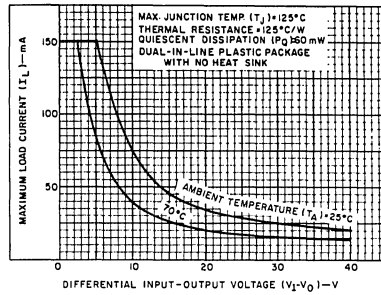


FIGURE 9. MAX LOAD CURRENT vs DIFFERENTIAL INPUT-OUTPUT VOLTAGE FOR CA723CE

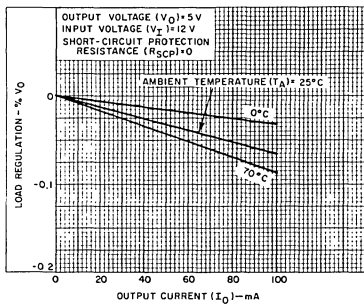


FIGURE 10. LOAD REGULATION WITHOUT CURRENT LIMITING

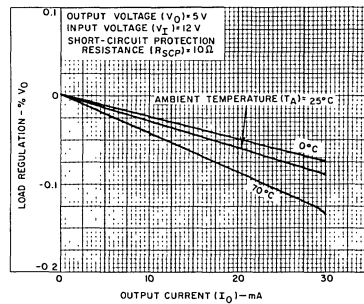


FIGURE 11. LOAD REGULATION WITH CURRENT LIMITING

# CA723, CA723C

## TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723C (Continued)

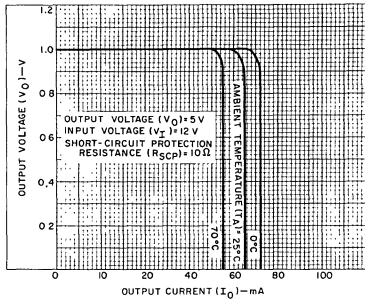


FIGURE 12. CURRENT LIMITING CHARACTERISTICS

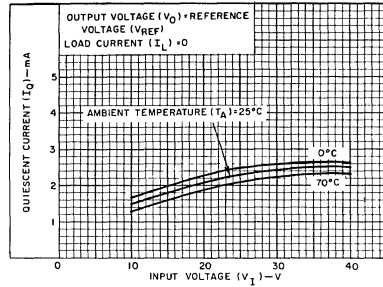


FIGURE 13. QUIESCIENT CURRENT vs INPUT VOLTAGE

## TYPICAL CHARACTERISTICS CURVES FOR TYPES CA723 AND CA723C

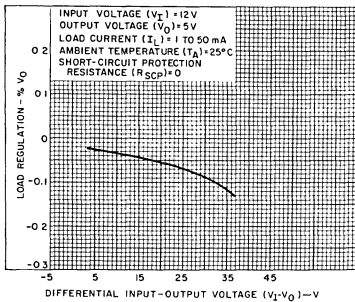


FIGURE 14. LOAD REGULATION vs DIFFERENTIAL INPUT-OUTPUT VOLTAGE

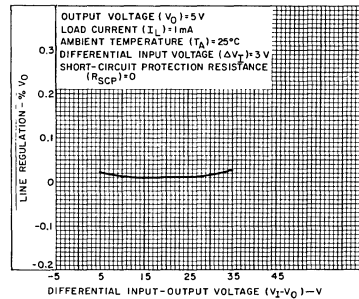


FIGURE 15. LINE REGULATION vs DIFFERENTIAL INPUT-OUTPUT VOLTAGE

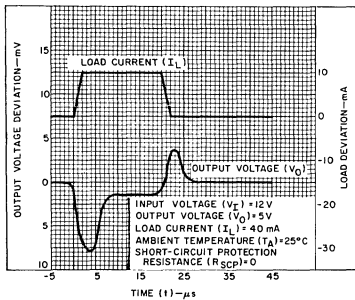


FIGURE 16. LINE TRANSIENT RESPONSE

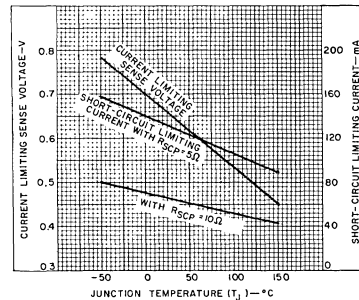


FIGURE 17. CURRENT LIMITING CHARACTERISTICS vs JUNCTION TEMPERATURE

# CA723, CA723C

## TYPICAL CHARACTERISTICS CURVES FOR TYPES CA723 AND CA723C (Continued)

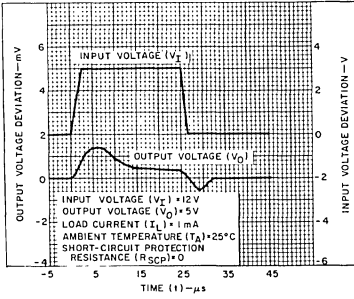


FIGURE 18. LOAD TRANSIENT RESPONSE

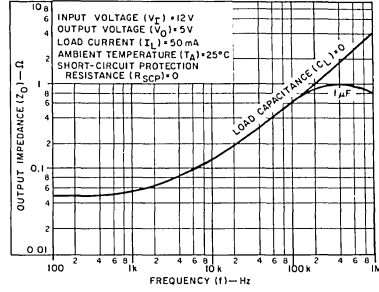


FIGURE 19. OUTPUT IMPEDANCE vs FREQUENCY

## TYPICAL APPLICATION CIRCUITS

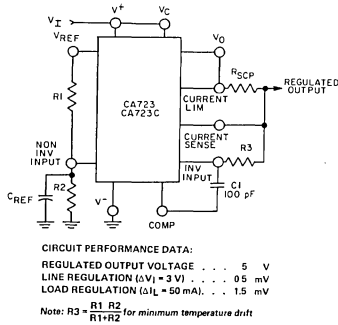


FIGURE 20. LOW VOLTAGE REGULATOR CIRCUIT ( $V_O = 2\text{V}$  TO  $7\text{V}$ )

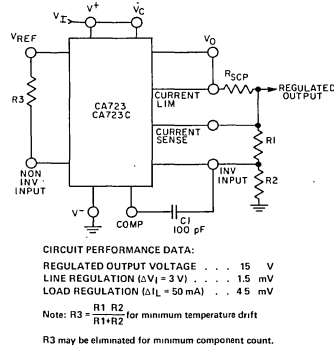


FIGURE 21. HIGH VOLTAGE REGULATOR CIRCUIT ( $V_O = 7\text{V}$  TO  $37\text{V}$ )

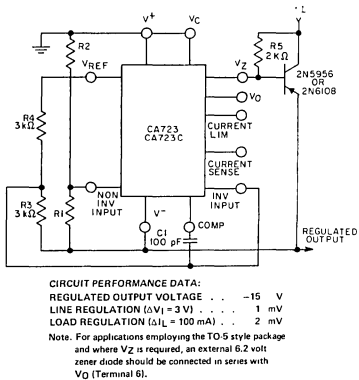


FIGURE 22. NEGATIVE VOLTAGE REGULATOR CIRCUIT

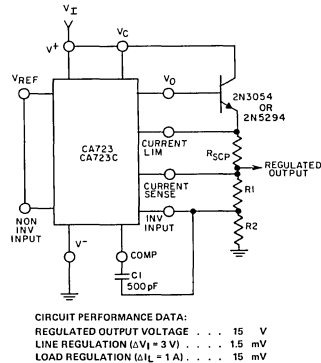
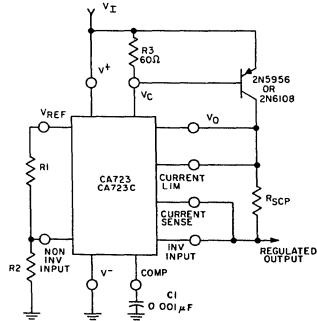


FIGURE 23. POSITIVE VOLTAGE REGULATOR CIRCUIT (WITH EXTERNAL n-p-n PASS TRANSISTOR)

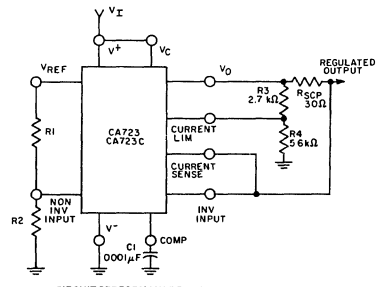
# CA723, CA723C

## TYPICAL APPLICATION CIRCUITS (Continued)



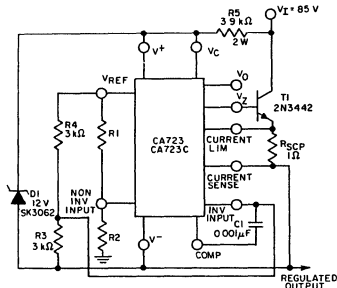
CIRCUIT PERFORMANCE DATA:  
 REGULATED OUTPUT VOLTAGE . . . . . 5 V  
 LINE REGULATION ( $\Delta V_I = 3$  V) . . . . . 0.5 mV  
 LOAD REGULATION ( $\Delta I_L = 1$  A) . . . . . 5 mV

FIGURE 24. POSITIVE VOLTAGE REGULATOR CIRCUIT (WITH EXTERNAL p-n-p PASS TRANSISTOR)



CIRCUIT PERFORMANCE DATA:  
 REGULATED OUTPUT VOLTAGE . . . . . 5 V  
 LINE REGULATION ( $\Delta V_I = 3$  V) . . . . . 0.5 mV  
 LOAD REGULATION ( $\Delta I_L = 10$  mA) . . . . . 1 mV  
 SHORT-CIRCUIT CURRENT . . . . . 20 mA

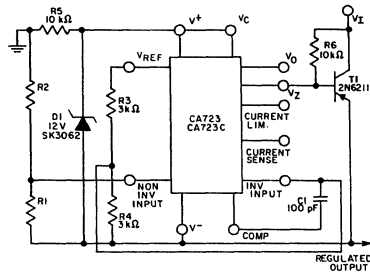
FIGURE 25. FOLDBACK CURRENT LIMITING CIRCUIT



Note: For applications employing the TO-5 style package and where  $V_Z$  is required, an external 6.2-volt zener diode should be connected in series with  $V_0$  (Terminal 6).

CIRCUIT PERFORMANCE DATA:  
 REGULATED OUTPUT VOLTAGE . . . . . 50 V  
 LINE REGULATION ( $\Delta V_I = 20$  V) . . . . . 15 mV  
 LOAD REGULATION ( $\Delta I_L = 50$  mA) . . . . . 20 mV

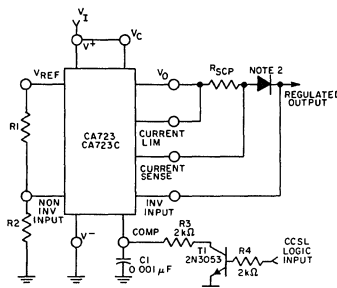
FIGURE 26. POSITIVE FLOATING REGULATOR CIRCUIT



CIRCUIT PERFORMANCE DATA:  
 REGULATED OUTPUT VOLTAGE . . . . . -100 V  
 LINE REGULATION ( $\Delta V_I = 20$  V) . . . . . 30 mV  
 LOAD REGULATION ( $\Delta I_L = 100$  mA) . . . . . 20 mV

Note: For applications employing the TO-5 style package and where  $V_Z$  is required, an external 6.2-volt zener diode should be connected in series with  $V_0$  (Terminal 6).

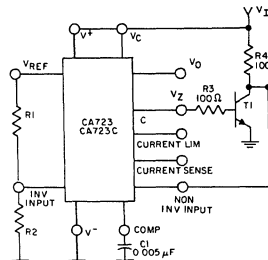
FIGURE 27. NEGATIVE FLOATING REGULATOR CIRCUIT



CIRCUIT PERFORMANCE DATA:  
 REGULATED OUTPUT VOLTAGE . . . . . 5 V  
 LINE REGULATION ( $\Delta V_I = 3$  V) . . . . . 0.5 mV  
 LOAD REGULATION ( $\Delta I_L = 50$  mA) . . . . . 1.5 mV

Note 1: A current limiting transistor may be used for shutdown if current limiting is not required.  
 Note 2: Add a diode if  $V_0 > 10$  V.

FIGURE 28. REMOTE SHUTDOWN REGULATOR CIRCUIT WITH CURRENT LIMITING



CIRCUIT PERFORMANCE DATA:  
 REGULATED OUTPUT VOLTAGE . . . . . 5 V  
 LINE REGULATION ( $\Delta V_I = 10$  V) . . . . . 0.5 mV  
 LOAD REGULATION ( $\Delta I_L = 100$  mA) . . . . . 1.5 mV

Note: For applications employing the TO-8 style package and where  $V_Z$  is required, an external 6.2-volt zener diode should be connected in series with  $V_0$  (Terminal 6).

FIGURE 29. SHUNT REGULATOR CIRCUIT

August 1991

### Features

- Complete PWM Power Control Circuitry
- Separate Outputs for Single-Ended or Push-Pull Operation
- Line and Load Regulation of 0.2% (Typ)
- Internal Reference Supply with 1% (Max) Oscillator and Reference Voltage Variation Over Full Temperature Range
- Standby Current of Less Than 10mA
- Frequency of Operation Beyond 100kHz
- Variable-Output Dead Time of 0.5 $\mu$ s to 5 $\mu$ s
- Low  $V_{CE(sat)}$  Over the Temperature Range

### Applications

- Positive and Negative Regulated Supplies
- Dual-Output Regulators
- Flyback Converters
- DC-DC Transformer-Coupled Regulating Converters
- Single-Ended DC-DC Converters
- Variable Power Supplies

### Description

The CA1524, CA2524, and CA3524 are silicon monolithic integrated circuits designed to provide all the control circuitry for use in a broad range of switching regulator circuits.

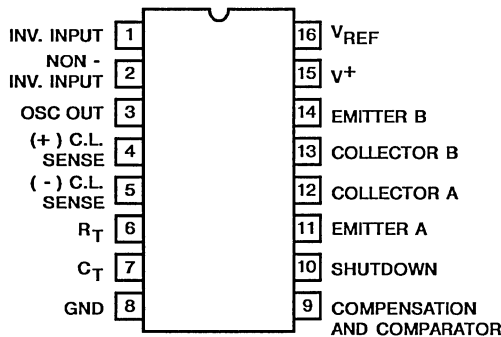
The CA1524, CA2524, and CA3524 have all the features of the industry types SG1524, SG2524, and SG3524, respectively. A block diagram of the CA1524 series is shown in Fig. 1. The circuit includes a zener voltage reference, transconductance error amplifier, precision R-C oscillator, pulse-width modulator, pulse-steering flip-flop, dual alternating output switches, and current-limiting and shutdown circuitry. This device can be used for switching regulators of either polarity, transformer-coupled dc-dc converter, transformerless voltage doublers, dc-ac power inverters, highly efficient variable power supplies, and polarity converter, as well as other power-control applications.

The CA1524 is specified for the military temperature range of -55°C to +125°C.

The CA2524 and CA3524 are specified for the commercial temperature range of 0°C to 70°C. All types operate over a supply voltage range of 8 to 40 V, have a rated operating temperature range of -55°C to +125°C, and are supplied in 16 lead, dual-in-line plastic packages (E suffix), and dual-in-line frit-seal hermetic packages (F suffix). The CA3524 is available in chip form (H suffix).

### Pinout

16 LEAD DUAL-IN-LINE PACKAGE  
TOP VIEW



### Maximum Rating, Absolute-Maximum Values

|   |                        |
|---|------------------------|
| Input Voltage (Between V <sub>IN</sub> and GND Terminals) | 40V                    |
| Operating Voltage Range (V <sub>IN</sub> to GND)          | 8 to 40V               |
| Output Current Each Output:                               |                        |
| (Terminal 11, 12 or 13, 14)                               | 100mA                  |
| Output Current (Reference Regulator)                      | 50mA                   |
| Oscillator Charging Current                               | 5mA                    |
| Device Dissipation:                                       |                        |
| Up to T <sub>A</sub> = 25°C                               | 1W                     |
| Above T <sub>A</sub> = 25°C                               | Derate linearly 8mW/°C |
| Operating Temperature Range                               | -55 to +125°C          |
| Storage Temperature Range                                 | -65 to +150°C          |



# CA1524, CA2524, CA3524

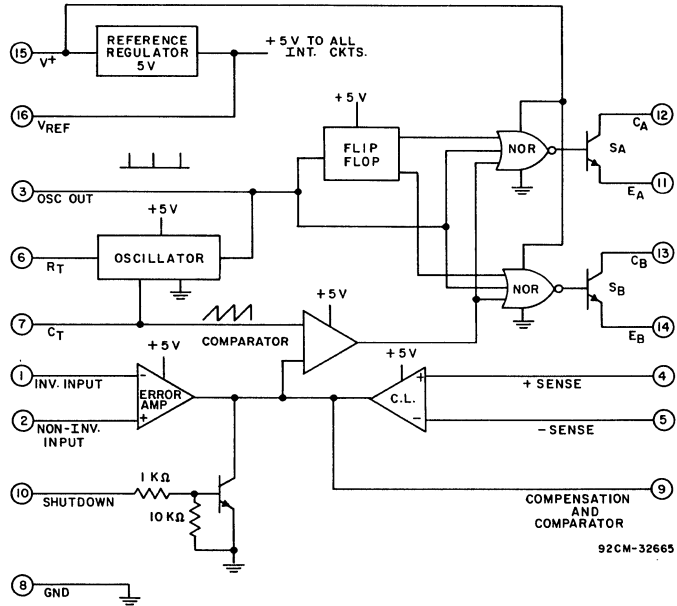


Fig. 1 - Functional block diagram of CA1524 series.

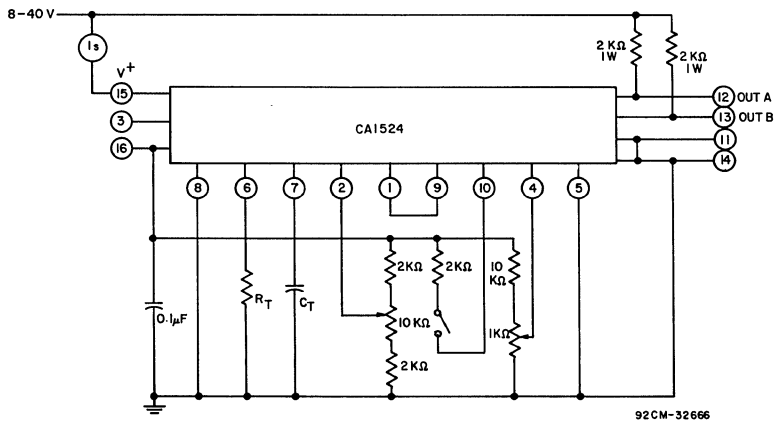
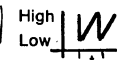


Fig. 2 - Open loop test circuit for CA1524 series.

## CA1524, CA2524, CA3524

**ELECTRICAL CHARACTERISTICS at  $T_A = -55$  to  $+125^\circ\text{C}$  for CA1524, 0 to  $+70^\circ\text{C}$  for the CA2524 and CA3524;  $V_+ = 20\text{ V}$  and  $f = 20\text{ kHz}$ , unless otherwise stated.**

| CHARACTERISTIC   | TEST CONDITIONS   | LIMITS         |      |      |        |      |      | UNITS                |
|--|---|----------------|------|------|--------|------|------|----------------------|
|  |   | CA1524, CA2524 |      |      | CA3524 |      |      |                      |
|  |   | Min.           | Typ. | Max. | Min.   | Typ. | Max. |                      |
| <b>Reference Section:</b>  |   |                |      |      |        |      |      |                      |
| Output Voltage   |   | 4.8            | 5    | 5.2  | 4.6    | 5    | 5.4  | V                    |
| Line Regulation  | $V_+ = 8$ to $40\text{ V}$  | —              | 10   | 20   | —      | 10   | 30   | mV                   |
| Load Regulation  | $I_L = 0$ to $20\text{ mA}$   | —              | 20   | 50   | —      | 20   | 50   | mV                   |
| Ripple Rejection   | $f = 120\text{ Hz}$ , $T_A = 25^\circ\text{C}$                                  | —              | 66   | —    | —      | 66   | —    | dB                   |
| Short Circuit Current Limit  | $V_{REF} = 0$ , $T_A = 25^\circ\text{C}$  | —              | 100  | —    | —      | 100  | —    | mA                   |
| Temperature Stability  | Over Operating Temperature Range  | —              | 0.3  | 1    | —      | 0.3  | 1    | %                    |
| Long Term Stability  | $T_A = 25^\circ\text{C}$  | —              | 20   | —    | —      | 20   | —    | mV/khr               |
| <b>Oscillator Section:</b>   |   |                |      |      |        |      |      |                      |
| Maximum Frequency  | $C_T = 0.001\ \mu\text{F}$ , $R_T = 2\text{ K}\Omega$                           | —              | 300  | —    | —      | 300  | —    | kHz                  |
| Initial Accuracy   | $R_T$ and $C_T$ constant  | —              | 5    | —    | —      | 5    | —    | %                    |
| Voltage Stability  | $V_+ = 8$ to $40\text{ V}$ , $T_A = 25^\circ\text{C}$                           | —              | —    | 1    | —      | —    | 1    | %                    |
| Temperature Stability  | Over Operating Temperature Range  | —              | —    | 2    | —      | —    | 2    | %                    |
| Output Amplitude   | Terminal 3, $T_A = 25^\circ\text{C}$  | —              | 3.5  | —    | —      | 3.5  | —    | V                    |
| Output Pulse Width (Pin 3)   | $C_T = 0.01\ \mu\text{F}$ , $T_A = 25^\circ\text{C}$                            | —              | 0.5  | —    | —      | 0.5  | —    | $\mu\text{s}$        |
| Ramp Voltage Low   | Pin 7   | —              | 0.6  | —    | —      | 0.6  | —    | V                    |
| Ramp Voltage High  | Pin 7   | —              | 3.5  | —    | —      | 3.5  | —    | V                    |
| Capacitor Charging Current   | Pin 7   | 0.03           | —    | 2    | 0.03   | —    | 2    | mA                   |
| Current Range  | $(5-2 V_{BE})/R_T$  |                |      |      |        |      |      |                      |
| Timing Resistance Range  | Pin 6   | 1.8            | —    | 120  | 1.8    | —    | 120  | $\text{K}\Omega$     |
| Charging Capacitor Range   | Pin 7   | 0.001          | —    | 0.1  | 0.001  | —    | 0.1  | $\mu\text{F}$        |
| Dead Time Expansion Capacitor on Pin 3 (when a small osc. cap is used) | Pin 3   | 100            | —    | 1000 | 100    | —    | 1000 | pF                   |
| <b>Error Amplifier Section:</b>  |   |                |      |      |        |      |      |                      |
| Input Offset Voltage   | $V_{CM} = 2.5\text{ V}$   | —              | 0.5  | 5    | —      | 2    | 10   | mV                   |
| Input Bias Current   | $V_{CM} = 2.5\text{ V}$   | —              | 1    | 10   | —      | 1    | 10   | $\mu\text{A}$        |
| Open Loop Voltage Gain   |   | 72             | 80   | —    | 60     | 80   | —    | dB                   |
| Common Mode Voltage  | $T_A = 25^\circ\text{C}$  | 1.8            | —    | 3.4  | 1.8    | —    | 3.4  | V                    |
| Common Mode Rejection Ratio  | $T_A = 25^\circ\text{C}$  | —              | 70   | —    | —      | 70   | —    | dB                   |
| Small Signal Bandwidth   | $A_V = 0\text{ dB}$ , $T_A = 25^\circ\text{C}$                                  | —              | 3    | —    | —      | 3    | —    | MHz                  |
| Output Voltage   | $T_A = 25^\circ\text{C}$  | 0.5            | —    | 3.8  | 0.5    | —    | 3.8  | V                    |
| Amplifier Pole   |   | —              | 250  | —    | —      | 250  | —    | Hz                   |
| Pin 9 Shutdown Current   | External Sink   | —              | 200  | —    | —      | 200  | —    | $\mu\text{A}$        |
| <b>Comparator Section:</b>   |   |                |      |      |        |      |      |                      |
| Duty Cycle   | % Each Output On  | 0              | —    | 45   | 0      | —    | 45   | %                    |
| Input Threshold  | Zero Duty Cycle   | —              | 1    | —    | —      | 1    | —    | V                    |
| Input Threshold  | Max. Duty Cycle   | —              | 3.5  | —    | —      | 3.5  | —    | V                    |
| Input Bias Current   |   | —              | 1    | —    | —      | 1    | —    | $\mu\text{A}$        |
| <b>Current Limiting Section:</b>                                       |   |                |      |      |        |      |      |                      |
| Sense Voltage For 25% Output Duty Cycle                                | Terminal 9 = 2 V with Error Amplifier Set for Max Out, $T_A = 25^\circ\text{C}$ | 190            | 200  | 210  | 180    | 200  | 220  | mV                   |
| Sense Voltage T.C.   |   | —              | 0.2  | —    | —      | 0.2  | —    | mV/ $^\circ\text{C}$ |
| Common Mode Voltage  |   | -1             | —    | +1   | -1     | —    | +1   | V                    |
| Rolloff Pole of R51 C3 + Q64   |   | —              | 300  | —    | —      | 300  | —    | Hz                   |

\*Ramp voltage at Pin 7  where  $t = \text{OSC period in microseconds}$   
 $t \cong R_T C_T$  with  $C_T$  in microfarads and  $R_T$  in ohms.

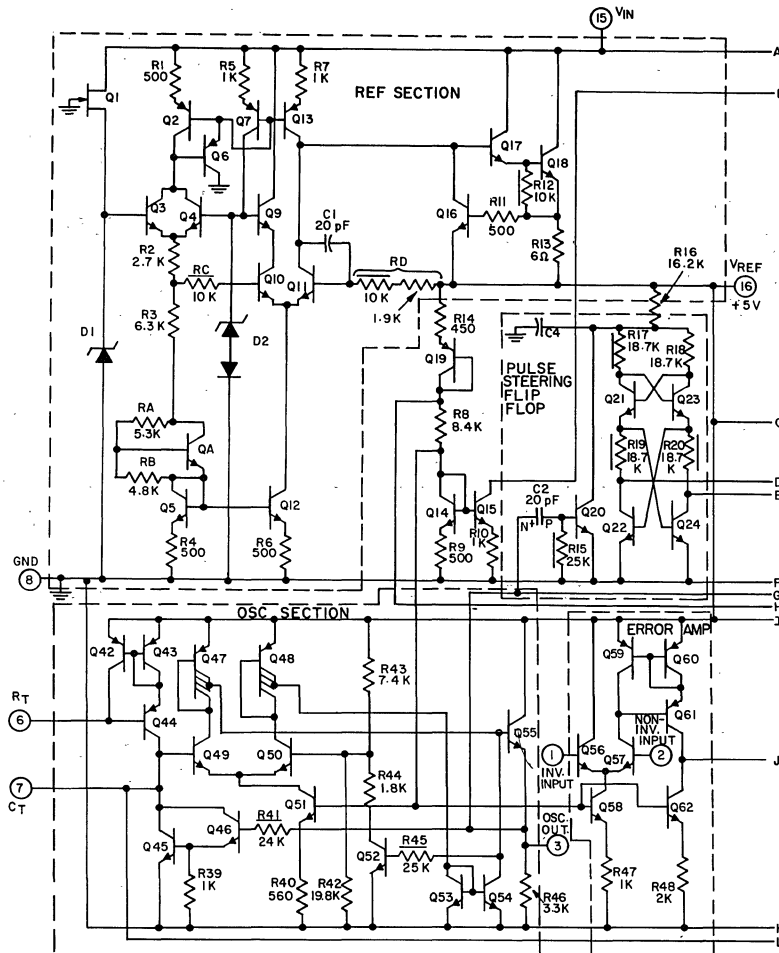
Output frequency at each output transistor is half OSC frequency when each output is used separately and is equal to the OSC frequency when each output is connected in parallel.

# CA1524, CA2524, CA3524

## ELECTRICAL CHARACTERISTICS (Cont'd)

| CHARACTERISTIC                       | TEST CONDITIONS                                | LIMITS         |      |      |        |      |      | UNITS         |
|--------------------------------------|--|----------------|------|------|--------|------|------|---------------|
|                                      |  | CA1524, CA2524 |      |      | CA3524 |      |      |               |
|                                      |  | Min.           | Typ. | Max. | Min.   | Typ. | Max. |               |
| <b>Output Section: (Each Output)</b> |  |                |      |      |        |      |      |               |
| Collector-Emitter Voltage            |  | 40             | —    | —    | 40     | —    | —    | V             |
| Collector Leakage Current            | $V_{CE}=40\text{ V}$                           | —              | 0.1  | 50   | —      | 0.1  | 50   | $\mu\text{A}$ |
| Saturation Voltage                   | $V_{+}=40\text{ V}, I_c=50\text{ mA}$          | —              | 0.8  | 2    | —      | 0.8  | 2    | V             |
| Emitter Output Voltage               | $V_{+}=20\text{ V}$                            | 17             | 18   | —    | 17     | 18   | —    | V             |
| Rise Time                            | $R_c=2\text{ K}\Omega, T_A=25^{\circ}\text{C}$ | —              | 0.2  | —    | —      | 0.2  | —    | $\mu\text{s}$ |
| Fall Time                            | $R_c=2\text{ K}\Omega, T_A=25^{\circ}\text{C}$ | —              | 0.1  | —    | —      | 0.1  | —    | $\mu\text{s}$ |
| Total Standby Current* $I_s$         | $V_{+}=40\text{ V}$                            | —              | 4    | 10   | —      | 4    | 10   | mA            |

\*Excluding oscillator charging current, error and current limit dividers, and with outputs open.



92CL-32686

Fig. 3 - Schematic diagram.

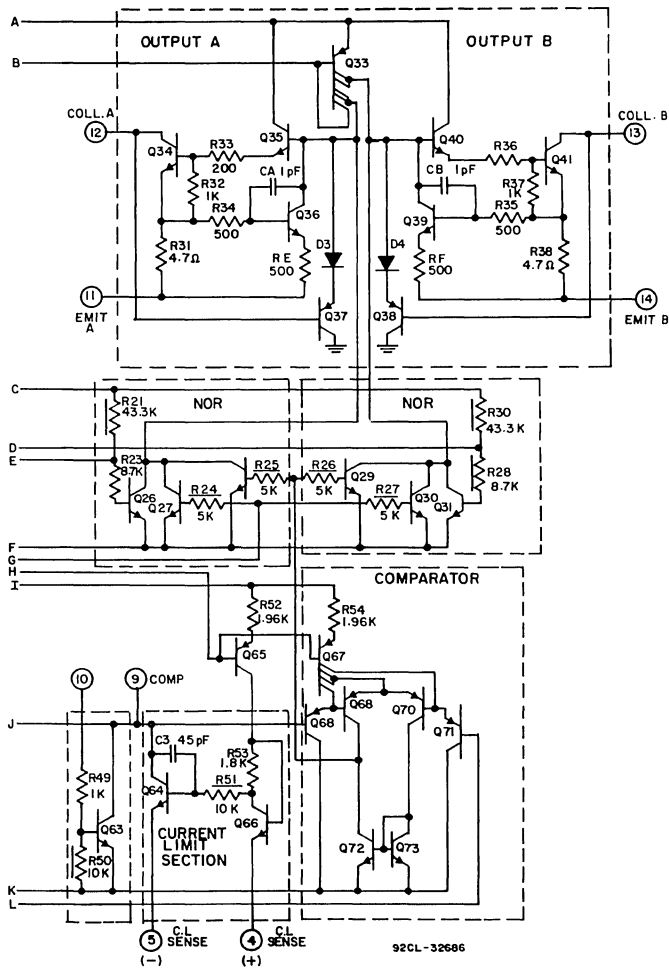


Fig. 3 - Schematic diagram (cont'd).

**CIRCUIT DESCRIPTION**  
**Voltage Reference Section**

The CA1524 series contains an internal series voltage regulator employing a zener reference to provide a nominal 5-volt output, which is used to bias all internal timing and control circuitry. The output of this regulator is available at terminal 16 and is capable of supplying up to 50-mA output current.

Fig. 4 shows the temperature variation of the reference voltage with supply voltages of 8 to 40 volts and load currents up to 20 mA. Load regulation and line regulation curves are shown in Figs. 5 and 6, respectively.

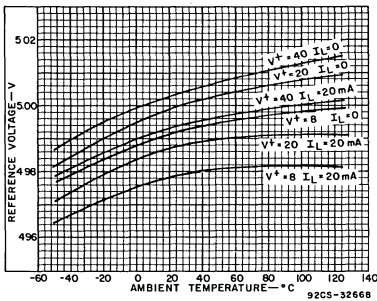


Fig. 4 - Typical reference voltage as a function of ambient temperature.

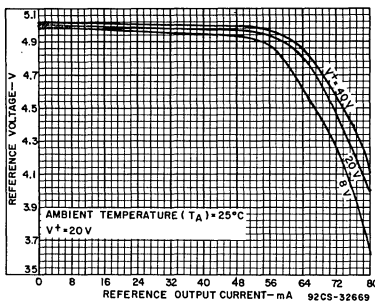


Fig. 5 - Typical reference voltage as a function of reference output current.

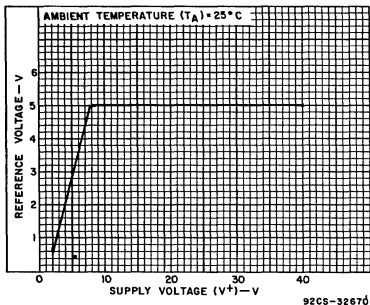


Fig. 6 - Typical reference voltage as a function of supply voltage.

**Oscillator Section**

Transistors Q42, Q43 and Q44, in conjunction with an external resistor R<sub>T</sub>, establishes a constant charging current into an external capacitor C<sub>T</sub> to provide a linear ramp voltage at terminal 7. The ramp voltage has a value that ranges from 0.6 to 3.5 volts and is used as the reference for the comparator in the device. The charging current is equal to (5-2V<sub>BE</sub>)/R<sub>T</sub> or approximately 3.6/R<sub>T</sub> and should be kept within the range of 30 μA to 2 mA by varying R<sub>T</sub>. The discharge time of C<sub>T</sub> determines the pulse width of the oscillator output pulse at terminal 3. This pulse has a practical range of 0.5 μs to 5 μs for a capacitor range of 0.001 to 0.1 μF. The pulse has two internal uses: as a dead-time control of blanking pulse to the output stages to assure that both outputs cannot be on simultaneously and as a trigger pulse to the internal flip-flop which controls the switching of the output between the two output channels. The output dead-time relationship is shown in Fig. 7. Pulse widths less than 0.5 μs may allow false triggering of one output by removing the blanking pulse prior to a stable state in the flip-flop.

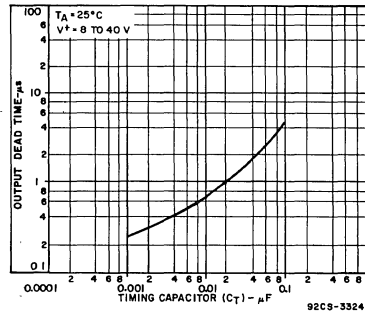


Fig. 7 - Typical output stage dead time as a function of timing capacitor value.

If a small value of C<sub>T</sub> must be used, the pulse width can be further expanded by the addition of a shunt capacitor in the order of 100 pF but no greater than 1000 pF, from terminal 3 to ground. When the oscillator output pulse is used as a sync input to an oscilloscope, the cable and input capacitances may increase the pulse width slightly. A 2-KΩ resistor at terminal 3 will usually provide sufficient decoupling of the cable. The upper limit of the pulse width is determined by the maximum duty cycle acceptable.

The oscillator period is determined by R<sub>T</sub> and C<sub>T</sub>, with an approximate value of t = R<sub>T</sub>C<sub>T</sub>, where R<sub>T</sub> is in ohms, C<sub>T</sub> is in μF, and t is in μs. Excess lead lengths, which produce stray capacitances, should be avoided in connecting R<sub>T</sub> and C<sub>T</sub> to their respective terminals. Fig. 8 provides curves for selecting these values for a wide range of oscillator periods. For series regulator applications, the two outputs can be connected in parallel for an effective 0-90% duty cycle with the output stage frequency the same as the oscillator frequency. Since the outputs are separate, push-pull and flyback applications are possible. The flip-flop divides the frequency such that the duty cycle of each output is 0-45% and the overall frequency is half that of the oscillator. Curves of the output duty cycle as a function of the voltage at terminal 9 are shown in Fig. 10. To synchronize two or more CA1524's, one must be designated as master, with

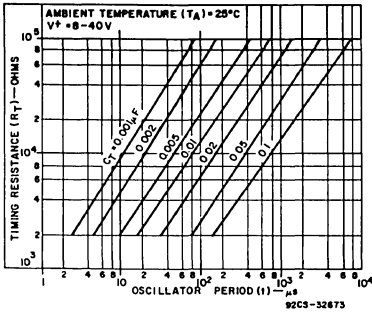


Fig. 8 - Typical oscillator period as a function of  $R_T$  and  $C_T$ .

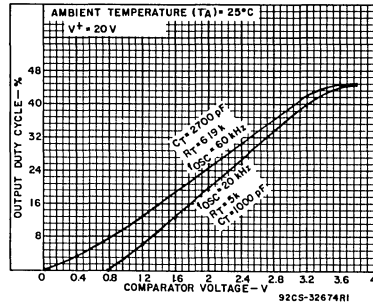


Fig. 10 - Typical duty cycle as a function of comparator voltage (at terminal 9).

$R_T C_T$  set for the correct period. Each of the remaining units (slaves) must have a  $C_T$  of  $\frac{1}{2}$  the value used in the master and approximately a 10% longer  $R_T C_T$  period than the master. Connecting terminal 3 together on all units assures that the master output pulse, which occurs first and has a wider pulse width, will reset the slave units.

**Error Amplifier Section**

The error amplifier consists of a differential pair (Q56, Q57) with an active load (Q61 and Q62) forming a differential transconductance amplifier. Since Q61 is driven by a constant current source, Q62, the output impedance  $R_{out}$ , terminal 9, is very high ( $\approx 5 M\Omega$ ).

The gain is:

$$A_v = g_m R = 8 I_c R / 2KT = 10^4,$$

where  $R = \frac{R_{out} R_L}{R_{out} + R_L}$ ,  $R_L = \infty$ ,  $A_v \propto 10^4$

Since  $R_{out}$  is extremely high, the gain can be easily reduced from a nominal  $10^4$  (80 dB) by the addition of an external shunt resistor from terminal 9 to ground as shown in Fig. 9.

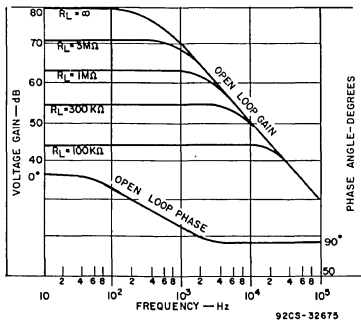


Fig. 9 - Open-loop error amplifier response characteristics.

phase shift curves are shown in Fig. 10. The uncompensated amplifier has a single pole at approximately 250 Hz and a unity gain cross-over at 3 MHz.

Since most output filter designs introduce one or more additional poles at a lower frequency, the best network to stabilize the system is a series RC combination at terminal 9 to ground. This network should be designed to introduce a zero to cancel out one of the output filter poles. A good starting point to determine the external poles is a 1000-pF capacitor and a variable series 50-K $\Omega$  potentiometer from terminal 9 to ground. The compensation point is also a convenient place to insert any programming signal to override the error amplifier. Internal shutdown and current limiting are also connected at terminal 9. Any external circuit that can sink 200  $\mu A$  can pull this point to ground and shut off both output drivers.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and will be stable in either the inverting or non-inverting mode. Input common-mode limits must be observed; if not, output signal inversion may result. The internal 5-volt reference can be used for conventional regulator applications if divided as shown in Fig. 11. If the error amplifier is connected as a unity gain amplifier, a fixed duty cycle application results.

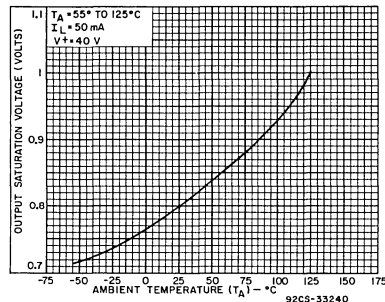


Fig. 11 - Typical output saturation voltage as a function of ambient temperature.

The output amplifier terminal is also used to compensate the system for ac stability. The frequency response and

## CA1524, CA2524, CA3524

### Output Section

The CA1524 series outputs are two identical n-p-n transistors with both collectors and emitters uncommitted. Each output transistor has antisaturation circuitry that enables a fast transient response for the wide range of oscillator frequencies. Current limiting of the output section is set at 100 mA for each output and 100 mA total if both outputs are paralleled. Having both emitters and collectors available provides the versatility to drive either n-p-n or p-n-p external transistors. Curves of the output saturation voltage as a function of temperature and output current are shown in Figs. 11 and 12, respectively.

There are a number of output configurations possible in the application of the CA1524 to voltage regulator circuits which fall into three basic classifications:

1. Capacitor-diode coupled voltage multipliers
2. Inductor-capacitor single-ended circuits
3. Transformer-coupled circuits

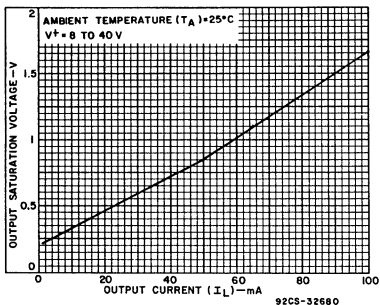


Fig. 12 - Typical output saturation voltage as a function of output current.

### Device Application Suggestions

For higher currents, the circuit of Fig. 13 may be used with an external p-n-p transistor and bias resistor. The internal regulator may be bypassed for operation from a fixed 5-volt supply by connecting both terminals 15 and 16 to the input voltage, which must not exceed 6 volts.

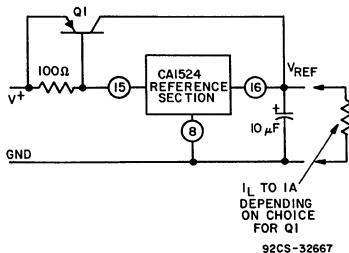


Fig. 13 - Circuit for expanding the reference current capability.

The internal 5-volt reference can be used for conventional regulator applications if divided as shown in Fig. 14. If the error amplifier is connected as a unity gain amplifier, a fixed duty cycle application results.

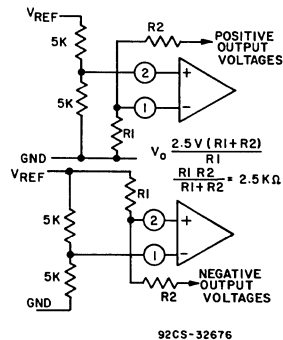


Fig. 14 - Error amplifier biasing circuits.

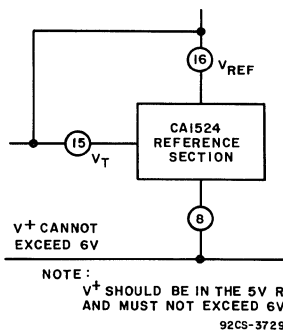


Fig. 15 - Circuit to allow external bypass of the reference regulation.

To provide an expansion of the dead time without loading the oscillator, the circuit of Fig. 16 may be used.

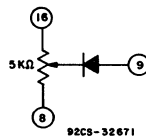


Fig. 16 - Circuit for expansion of dead time, without using a capacitor on pin 3 or when a low value oscillator capacitor is used.

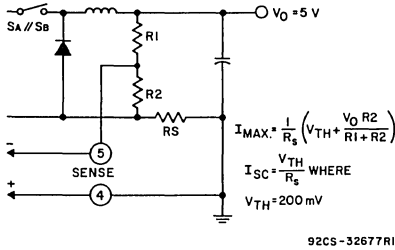


Fig. 17 - Foldback current-limiting circuit used to reduce power dissipation under shorted output conditions.

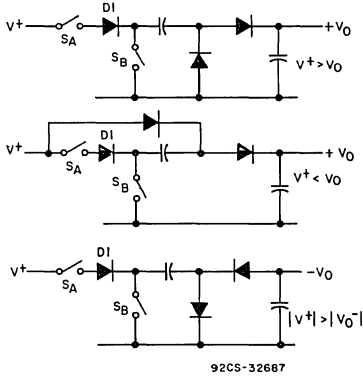


Fig. 18 - Capacitor-diode coupled voltage multiplier output stages. (Note: Diode D1 is necessary to prevent reverse emitter-base breakdown of transistor switch SA).

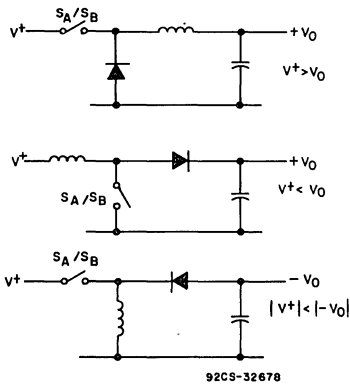


Fig. 19 - Single-ended inductor circuits where the two outputs of the 1524 are connected in parallel.

Table 1 - Input vs. Output voltage, and Feedback Resistor Values for IL=40 mA (For capacitor-diode output circuit in Fig. 21)

| VO (V) | R2 (KΩ) | V+ (Min.) (V) |
|--------|---------|---------------|
| -0.5   | 6       | 8             |
| -2.5   | 10      | 9             |
| -3     | 11      | 10            |
| -4     | 13      | 11            |
| -5     | 15      | 12            |
| -6     | 17      | 13            |
| -7     | 19      | 14            |
| -8     | 21      | 15            |
| -9     | 23      | 16            |
| -10    | 25      | 17            |
| -11    | 27      | 18            |
| -12    | 29      | 19            |
| -13    | 31      | 20            |
| -14    | 33      | 21            |
| -15    | 35      | 22            |
| -16    | 37      | 23            |
| -17    | 39      | 24            |
| -18    | 41      | 25            |
| -19    | 43      | 26            |
| -20    | 45      | 27            |

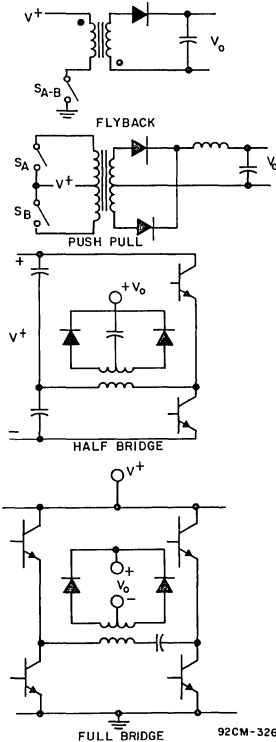


Fig. 20 - Transformer-coupled outputs.



## CA1524, CA2524, CA3524

### APPLICATIONS\*

A capacitor-diode output filter is used in Fig. 22 to convert +15 V dc to -5 V dc at output currents up to 50 mA. Since the output transistors have built-in current limiting, no additional current limiting is needed. Table I gives the required minimum input voltage and feedback resistor values, R2, for an output voltage.

### Capacitor-Diode Output Circuit

A capacitor-diode output filter is used in Fig. 21 to convert +15 V dc to -5 V dc at output currents up to 50 mA. Since the output transistors have built-in current limiting, no additional current limiting is needed. Table I gives the required minimum input voltage and feedback resistor values, R2, for an output voltage.

an output voltage range of -0.5 V to -20 V with an output current of 40 mA.

### Single-Ended Switching Regulator

The CA1524 in the circuit of Fig. 22 has both output stages connected in parallel to produce an effective 0-90% duty cycle. Transistor Q1 is pulsed on and off by these output stages. Regulation is achieved from the feedback provided by R1 and R2 to the error amplifier which adjusts the on-time of the output transistors according to the load current being drawn. Various output voltages can be obtained by adjusting R1 and R2. The use of an output inductor requires an R-C phase compensation network to stabilize the system. Current limiting is set at 1.9 amperes by the sense resistor R3.

\*For additional information on the application of this device and a further explanation of the circuits below, see RCA Application Note ICAN-6915 "Application of the CA1524 series PWM IC".

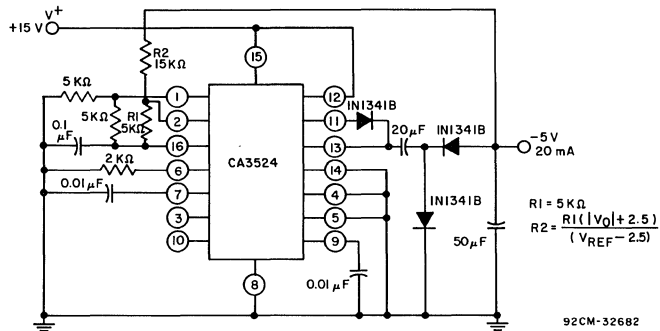


Fig. 21 - Capacitor-diode output circuit.

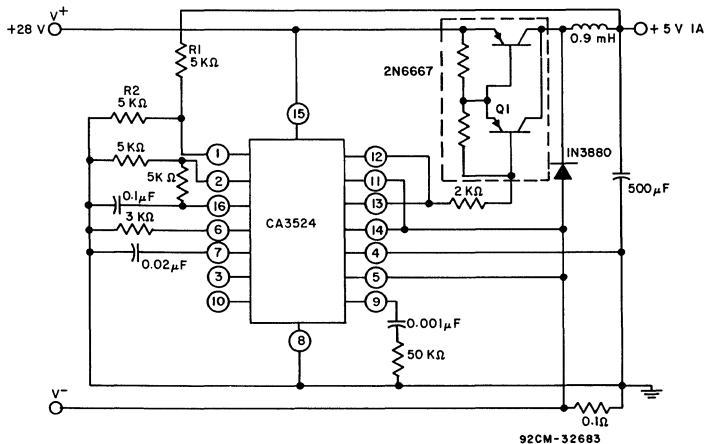


Fig. 22 - Single-ended LC switching regulator circuit.

## CA1524, CA2524, CA3524

### Flyback Converter

Fig. 23 shows a flyback converter circuit for generating a dual 15-volt output at 20 mA from a 5-volt regulated line. Reference voltage is provided by the input and the internal reference generator is unused. Current limiting in this circuit is accomplished by sensing current in the primary line and resetting the soft-start circuit.

### Push-Pull Converter

The output stages of the CA1524 provide the drive for transistors Q1 and Q2 in the push-pull application of Fig. 24. Since the internal flip-flop divides the oscillator frequency by two, the oscillator must be set at twice the output frequency. Current limiting for this circuit is done in the primary of transformer T1 so that the pulse width will be reduced if transformer saturation should occur.

### Low-Frequency Pulse Generator

Fig. 25 shows the CA1524 being used as a low-frequency pulse generator. Since all components (error amplifier, oscillator, oscillator reference regulator, output transistor drivers) are on the IC, a regulated 5-V (or 2.5-V) pulse of 0%-45% (or 0%-90%) on time is possible over a frequency range of 150 to 500 Hz. Switch S1 is used to go from a 5-V output pulse (S1 closed) to a 2.5-V output pulse (S1 open) with a duty cycle range of 0% to 45%. The output frequency will be roughly half of the oscillator frequency when the output transistors are not connected in parallel (75 Hz to 250 Hz, respectively). Switch S2 will allow both output stages to be paralleled for an effective duty cycle of 0%-90% with the output frequency range from 150 to 500 Hz. The frequency is adjusted by R1; R2 controls duty cycle.

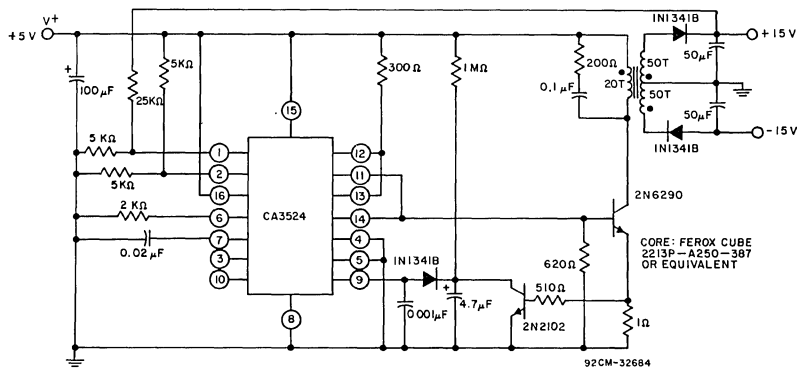


Fig. 23 - Flyback converter circuit.

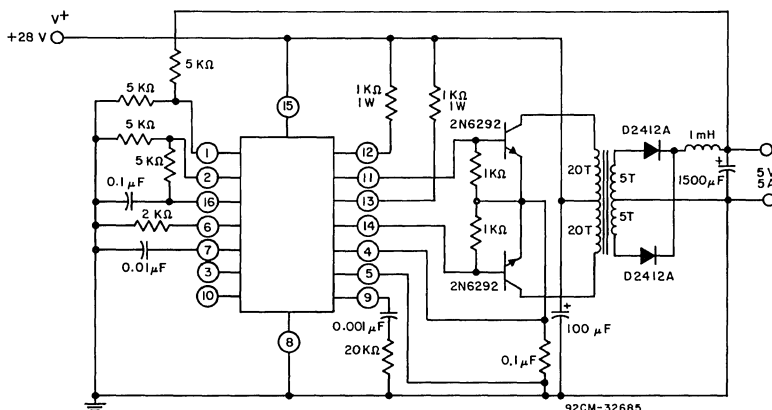


Fig. 24 - Push-pull transformer-coupled converter.

## CA1524, CA2524, CA3524

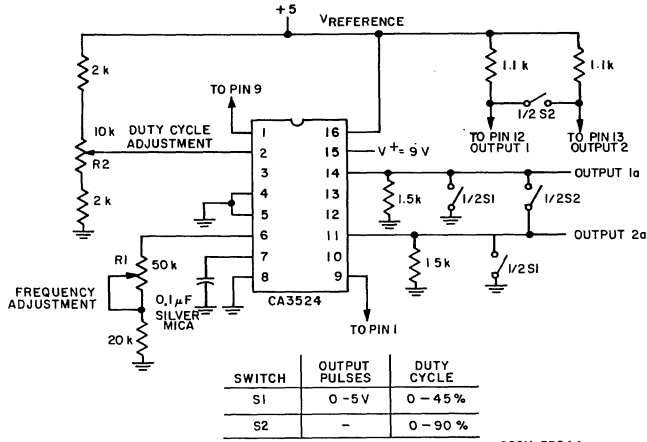


Fig. 25 - Low-frequency pulse generator.

### The Variable Switcher

The circuit diagram of the CA1524, used as a variable-output-voltage power supply is shown in Fig. 26. By connecting the two output transistors in parallel, the duty cycle is doubled, i.e., 0-90%.

As the reference voltage level is varied, the feedback voltage will track that level and cause the output voltage to change according to the change in reference voltage.

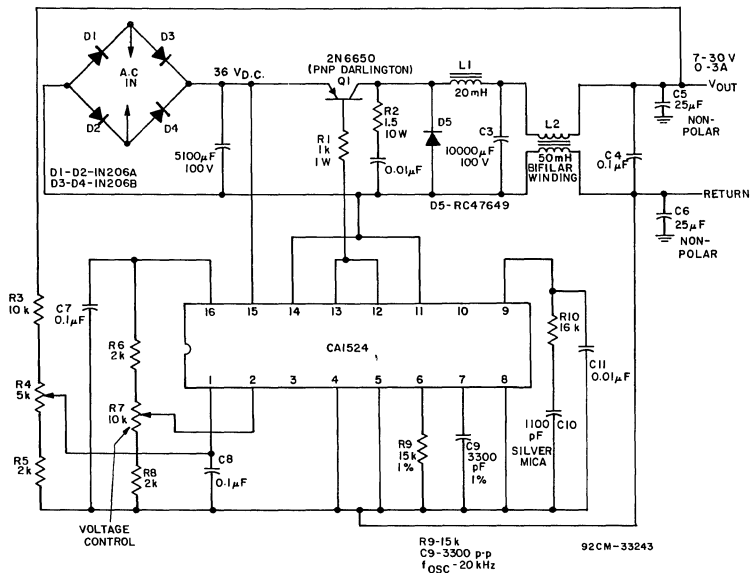


Fig. 26 - The CA1524 used as a 0.5 A, 7-30 V laboratory supply.

## CA1524, CA2524, CA3524

### Digital Readout Scale

The CA1524 can be used as the driving source for an electronic scale application. The circuit shown in Figs. 27 and 28 uses half (Q2) of the CA1524 output in a low-voltage switching regulator (2.2 V) application to drive the LED's displaying the weight. The remaining output stage (Q1) is used as a driver for the sampling plates PL1 and PL2. Since the CA1524 contains a 5-volt internal regulator and a wide operating range of 8 to 40 volts, a single 9-volt battery can power the total system. The two plates, PL1 and PL2, are driven with opposite phase signals (frequency held constant but duty cycle may change) from the pulse-width modulator IC (CA1524). The sensor, S, is located between the two plates. Plates PL1, S and PL2 form an effective capacitance

bridge-type divider network. As plate S is moved according to the object's weight, a change in capacitance is noted between PL1, S and PL2. This change is reflected as a voltage to the ac amplifier (CA3160). At the null position the signals from PL1 and PL2 as detected by S are equal in amplitude, but opposite in phase. As S is driven by the scale mechanism down toward PL2, the signal at S becomes greater. The CA3160 ac amplifier provides a buffer for the small signal change noted at S. The output of the CA3160 is converted to a dc voltage by a peak-to-peak detector. A peak-to-peak detector is needed, since the duty cycle of the sampled waveform is subject to change. The detector output is filtered further and displayed via the CA3161E and CA3162E digital readout system, indicating the weight on the scale.

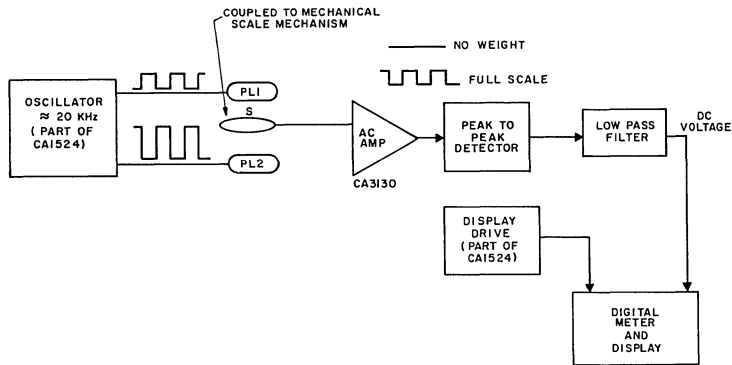


Fig. 27 - Basic digital readout scale.

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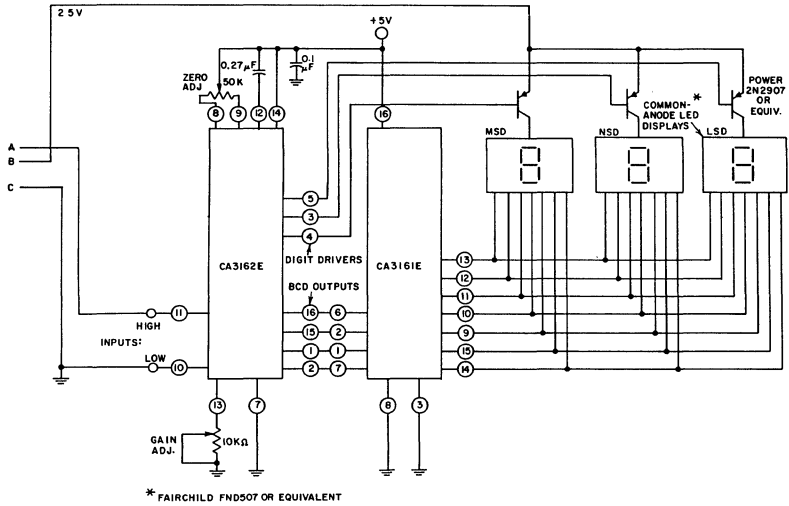


Fig. 28 - Schematic diagram of digital readout scale (cont'd).

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CA1524, CA2524, CA3524

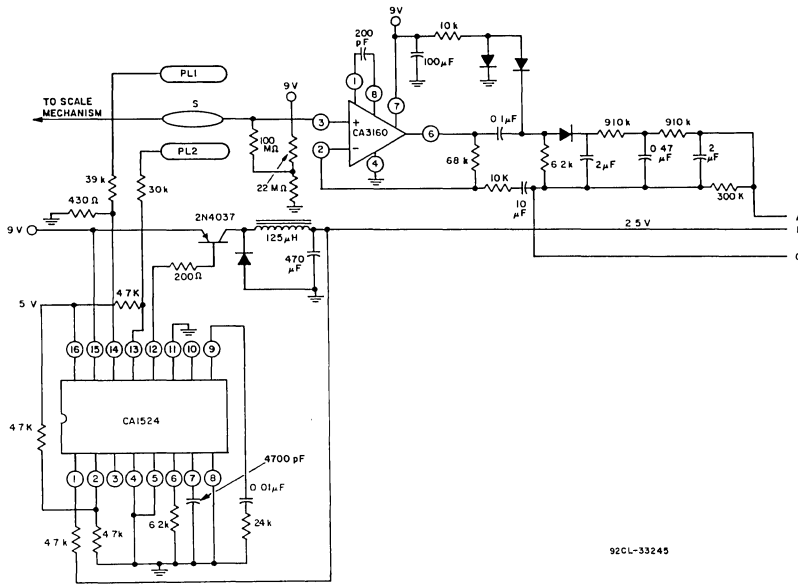
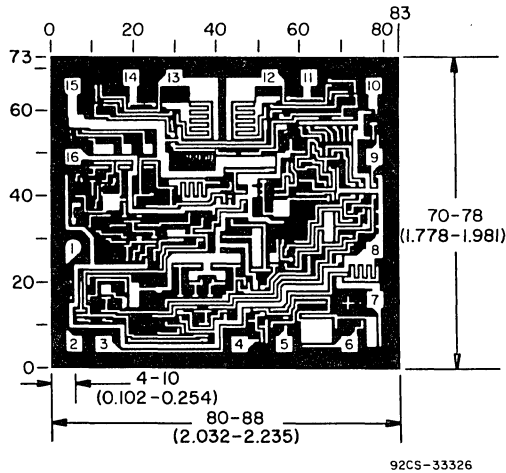


Fig. 29 - Schematic diagram of digital readout scale.



Dimensions and pad layout for CA3524H chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are  $57^\circ$  instead of  $90^\circ$  with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

August 1991

#### Features

- Relay Control
- Valve Control
- Synchronous Switching of Flashing Lights
- On-Off Motor Switching
- Differential Comparator with Self-Contained Power Supply for Industrial Applications
- Photosensitive Control
- Power One-Shot Control
- Heater Control
- Lamp Control

#### Type Features

|  | CA3059      | CA3079 |
|--|-------------|--------|
| • 24V, 120V, 208/230V, 277V at 50/60 or 400Hz Operation              | ✓           | ✓      |
| • Differential Input   | ✓           | ✓      |
| • Low Balance Input Current (Max) - $\mu$ A                          | 1           | 2      |
| • Built-In Protection Circuit for Opened or Shorted Sensor (Term 14) | ✓           | ✓      |
| • Sensor Range (Rx) - k $\Omega$                                     | 2 - 100     | 2 - 50 |
| • DC Mode (Term 12)  | ✓           |        |
| • External Trigger (Term 6)  | ✓           |        |
| • External Inhibit (Term 1)  | ✓           |        |
| • DC Supply Volts (Max)  | 14          | 10     |
| • Operating Temperature Range ( $^{\circ}$ C)                        | -55 to +125 |        |

#### Description

The CA3059 and CA3079 zero-voltage switches are monolithic silicon integrated circuits designed to control a thyristor in a variety of AC power switching applications for AC input voltages of 24V, 120V, 208/230V, and 277V at 50/60 and 400Hz. Each of the zero-voltage switches incorporates 4 functional blocks (see Fig. 1) as follows:

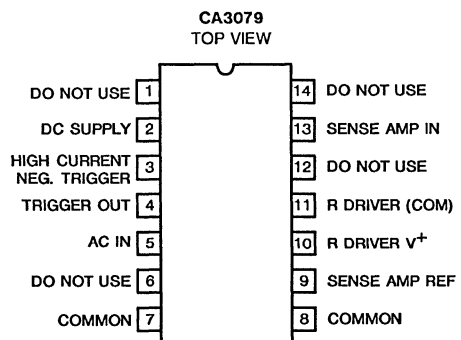
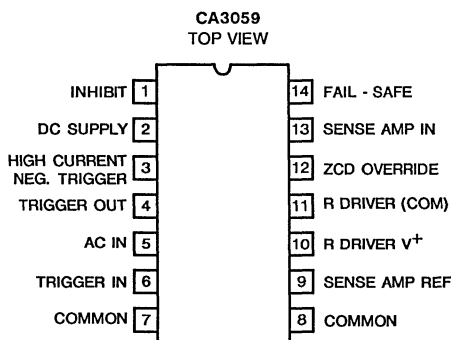
1. Limiter-Power Supply - Permits operation directly from an AC line.
2. Differential On/Off Sensing Amplifier - Tests the condition of external sensors or command signals. Hysteresis or proportional-control capability may easily be implemented in this section.
3. Zero-Crossing Detector - Synchronizes the output pulses of the circuit at the time when the AC cycle is at zero voltage point; thereby eliminating radio-frequency interference (RFI) when used with resistive loads.
4. Triac Gating Circuit - Provides high-current pulses to the gate of the power controlling thyristor.

In addition, the CA3059 provides the following important auxiliary functions (see Fig. 1).

1. A built-in protection circuit that may be actuated to remove drive from the triac if the sensor opens or shorts.
2. Thyristor firing may be inhibited through the action of an internal diode gate connected to Terminal 1.
3. High-power dc comparator operation is provided by overriding the action of the zero-crossing detector. This is accomplished by connecting Terminal 12 to Terminal 7. Gate current to the thyristor is continuous when Terminal 13 is positive with respect to Terminal 9.

The CA3059 and CA3079 are supplied in 14 lead dual-in-line plastic packages. They are also available in chip form (H suffix).

#### Pinouts



## CA3059, CA3079

### MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^\circ\text{C}$

DC SUPPLY VOLTAGE (BETWEEN TERMS. 2 AND 7):

|              |      |
|--------------|------|
| CA3059 ..... | 14 V |
| CA3079 ..... | 10 V |

DC SUPPLY VOLTAGE, (BETWEEN TERMS. 2 AND 8):

|              |      |
|--------------|------|
| CA3059 ..... | 14 V |
| CA3079 ..... | 10 V |

PEAK SUPPLY CURRENT (TERMS. 5 AND 7) .....

± 50 mA

OUTPUT PULSE CURRENT (TERM. 4) .....

150 mA

POWER DISSIPATIONS:

|   |   |
|---|---|
| Up to $T_A = 55^\circ\text{C}$ - CA3059, CA3079 ..... | 700 mW                                    |
| Above $T_A = 55^\circ\text{C}$ - CA3059, CA3079 ..... | Derate linearly 6.67 mW/ $^\circ\text{C}$ |

AMBIENT TEMPERATURE RANGE:

|                 |                              |
|-----------------|------------------------------|
| Operating ..... | -55 to +125 $^\circ\text{C}$ |
| Storage .....   | -65 to +150 $^\circ\text{C}$ |

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. .... +265 $^\circ\text{C}$

| MAXIMUM VOLTAGE RATINGS at $T_A = 25^\circ\text{C}$ |                            |          |          |          |                            |                            |                       |                       |          |          |                             |                             |                               | MAXIMUM CURRENT RATINGS       |                |                 |
|---|----------------------------|----------|----------|----------|----------------------------|----------------------------|-----------------------|-----------------------|----------|----------|-----------------------------|-----------------------------|-------------------------------|-------------------------------|----------------|-----------------|
| TERMINAL NO.  | 1<br><small>Note 3</small> | 2        | 3        | 4        | 5<br><small>Note 1</small> | 6<br><small>Note 3</small> | 7                     | 8                     | 9        | 10       | 11<br><small>Note 3</small> | 12<br><small>Note 3</small> | 13<br><small>Note 2,3</small> | 14<br><small>Note 2,3</small> | $I_{IN}$<br>mA | $I_{OUT}$<br>mA |
| 1<br><small>Note 3</small>                          | *                          | *        | *        | *        | 15<br>0                    | 10<br>-2                   | *                     | *                     | *        | *        | *                           | *                           | *                             | *                             | 10             | 0.1             |
| 2   |                            | 0<br>-15 | 0<br>-15 | 2<br>-14 | 0<br>-14                   | 0<br>-14                   | 0 <sup>▲</sup><br>-14 | 0 <sup>▲</sup><br>-14 | 0<br>-14 | 0<br>-14 | 0<br>-14                    | *                           | 0<br>-14                      | 0<br>-14                      | 150            | 10              |
| 3   |                            |          |          | 0<br>-15 | *                          | *                          | *                     | *                     | *        | *        | *                           | *                           | *                             | *                             | *              | *               |
| 4   |                            |          |          |          | 2<br>-10                   | *                          | *                     | *                     | *        | *        | *                           | *                           | *                             | *                             | 0.1            | 150             |
| 5<br><small>Note 1</small>                          |                            |          |          |          |                            | 7<br>-7                    | *                     | *                     | *        | *        | *                           | *                           | *                             | *                             | 50             | 10              |
| 6<br><small>Note 3</small>                          |                            |          |          |          |                            |                            | 14<br>0               | *                     | *        | *        | *                           | *                           | *                             | *                             | *              | *               |
| 7   |                            |          |          |          |                            |                            |                       | *                     | 14<br>0  | *        | 20<br>0                     | 2.5<br>-2.5                 | 14<br>0                       | 6<br>-6                       | *              | *               |
| 8   |                            |          |          |          |                            |                            |                       |                       |          | 10<br>0  | *                           | *                           | *                             | *                             | 0.1            | 2               |
| 9   |                            |          |          |          |                            |                            |                       |                       |          |          | *                           | *                           | *                             | *                             | *              | *               |
| 10  |                            |          |          |          |                            |                            |                       |                       |          |          | *                           | *                           | *                             | *                             | *              | *               |
| 11  |                            |          |          |          |                            |                            |                       |                       |          |          | *                           | *                           | *                             | *                             | *              | *               |
| 12<br><small>Note 3</small>                         |                            |          |          |          |                            |                            |                       |                       |          |          |                             | *                           | *                             | *                             | 50             | 50              |
| 13  |                            |          |          |          |                            |                            |                       |                       |          |          |                             |                             | *                             | *                             | *              | *               |
| 14<br><small>Note 3</small>                         |                            |          |          |          |                            |                            |                       |                       |          |          |                             |                             |                               | *                             | 2              | 2               |

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of horizontal Terminal 6 to vertical Terminal 4 is 2 to -10 volts.

**Note 1** – Resistance should be inserted between Terminal 5 and external supply or line voltage for limiting current into Terminal 5 to less than 50 mA.

**Note 2** – Resistance should be inserted between Terminal 14 and external supply for limiting current into Terminal 14 to less than 2 mA.

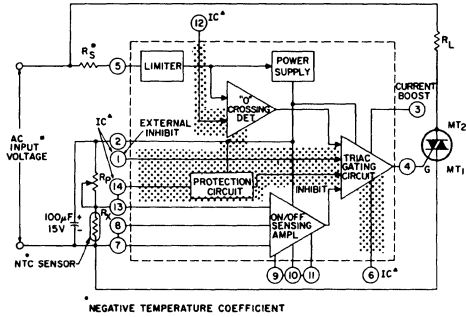
**Note 3** – For the CA3079 indicated terminal is internally connected and, therefore, should not be used.

<sup>▲</sup>For CA3079 (0 to -10 V).

\*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.



# CA3059, CA3079



| AC Input Voltage<br>(50/60 or 400 Hz)<br>V AC | Input Series<br>Resistor (RS)<br>k Ω | Dissipation Rating<br>for RS<br>W |
|---|--------------------------------------|-----------------------------------|
| 24  | 2                                    | 0.5                               |
| 120   | 10                                   | 2                                 |
| 208/230                                       | 20                                   | 4                                 |
| 277   | 25                                   | 5                                 |

**NOTE:**  
 Circuitry, within shaded areas, not included in CA3079  
 ■ See chart  
 ▲ IC = Internal Connection - DO NOT USE  
 (Terminal Restriction applies only to CA3079).

Fig. 1 - Functional block diagram of CA3059 and CA3079.

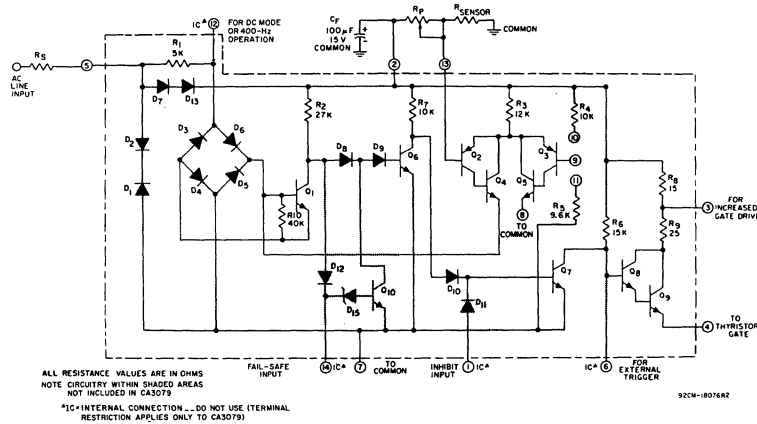


Fig. 2 - Schematic diagram of CA3059 and CA3079

## ELECTRICAL CHARACTERISTICS (For all types, unless indicated otherwise)

All voltages are measured with respect to Terminal 7.

| CHARACTERISTIC   | TEST CONDITIONS<br>T <sub>A</sub> = 25°C<br>(Unless Indicated Otherwise) | LIMITS |      |      | UNITS |
|--|--|--------|------|------|-------|
|  |  | Min.   | Typ. | Max. |       |
| <b>For Operating at 120 V rms, 50-60 Hz (AC Line Voltage)*</b> |  |        |      |      |       |
| DC Supply Voltage, V <sub>S</sub>                              |  |        |      |      |       |
| Inhibit Mode   |  |        |      |      |       |
| At 50/60 Hz  | R <sub>S</sub> = 8 kΩ, I <sub>L</sub> = 0                                | 6.1    | 6.5  | 7    | V     |
| At 400 Hz  | R <sub>S</sub> = 10 kΩ, I <sub>L</sub> = 0                               | —      | 6.8  | —    | V     |
| At 50/60 Hz  | R <sub>S</sub> = 5 kΩ, I <sub>L</sub> = 2 mA                             | —      | 6.4  | —    | V     |
| Pulse Mode   |  |        |      |      |       |
| At 50/60 Hz  | R <sub>S</sub> = 8 kΩ, I <sub>L</sub> = 0                                | 6      | 6.4  | 7    | V     |
| At 400 Hz  | R <sub>S</sub> = 10 kΩ, I <sub>L</sub> = 0                               | —      | 6.7  | —    | V     |
| At 50/60 Hz  | R <sub>S</sub> = 5 kΩ, I <sub>L</sub> = 2 mA                             | —      | 6.3  | —    | V     |
| At 50/60 Hz (CA3058)   | R <sub>S</sub> = 8 kΩ, I <sub>L</sub> = 0                                | 5.5    | —    | 7.5  | V     |
| See Fig. 3   | T <sub>A</sub> = -55 to +125°C   |        |      |      |       |

## CA3059, CA3079

### ELECTRICAL CHARACTERISTICS (For all types, unless indicated otherwise) (Cont'd)

All voltages are measured with respect to Terminal 7.

| CHARACTERISTIC   | TEST CONDITIONS<br>$T_A = 25^\circ\text{C}$<br>(Unless Indicated Otherwise) | LIMITS |          |       | UNITS         |
|--|---|--------|----------|-------|---------------|
|  |   | Min.   | Typ.     | Max.  |               |
| <b>For Operating at 120 V rms, 50-60 Hz (AC Line Voltage)<sup>•</sup></b>  |   |        |          |       |               |
| Gate Trigger Current, $I_{GT}^{(4)}$<br><i>See Figs. 4, 5(a)</i>   | Terms. 3 and 2 connected,<br>$V_{GT} = 1\text{ V}$                          | –      | 105      | –     | mA            |
| Peak Output Current (Pulsed),<br>$I_{OM}^{(4)}$<br>With Internal Power Supply  | Term. 3 open, Gate Trigger<br>Voltage ( $V_{GT}$ ) = 0                      | 50     | 84       | –     | mA            |
|  | Terms. 3 and 2 connected,<br>Gate Trigger Voltage ( $V_{GT}$ ) = 0          | 90     | 124      | –     | mA            |
| With External Power Supply<br><br><i>See Figs. 5, 6</i>  | Term. 3 open, $V^+ = 12\text{ V}$ , $V_{GT} = 0$                            | –      | 170      | –     | mA            |
|  | Terms. 3 and 2 connected,<br>$V^+ = 12\text{ V}$ , $V_{GT} = 0$             | –      | 240      | –     | mA            |
| Inhibit Input Ratio, $V_g/V_2$<br><i>See Fig. 7</i>  | Voltage Ratio of Term. 9 to 2   | 0.465  | 0.485    | 0.520 | –             |
| Total Gate Pulse Duration: <sup>*</sup><br>For positive dv/dt, $t_p$<br>50-60 Hz<br>400 Hz   | $C_{EXT} = 0$   | 70     | 100      | 140   | $\mu\text{s}$ |
|  | $C_{EXT} = 0$ , $R_{EXT} = \infty$  | –      | 12       | –     | $\mu\text{s}$ |
| For negative dv/dt, $t_N$<br>50-60 Hz<br>400 Hz<br><i>See Fig. 8</i>   | $C_{EXT} = 0$   | 70     | 100      | 140   | $\mu\text{s}$ |
|  | $C_{EXT} = 0$ , $R_{EXT} = \infty$  | –      | 10       | –     | $\mu\text{s}$ |
| Pulse Duration After Zero<br>Crossing (50-60 Hz):<br>For positive dv/dt, $t_{p1}$<br>For negative dv/dt, $t_{N1}$<br><i>See Fig. 8</i> | $C_{EXT} = 0$   | –      | 50       | –     | $\mu\text{s}$ |
|  | $R_{EXT} = \infty$  | –      | 60       | –     | $\mu\text{s}$ |
| Output Leakage Current, $I_4$<br>Inhibit Mode:<br><i>See Fig. 9</i>  |   | –      | 0.001    | 10    | $\mu\text{A}$ |
| Input Bias Current, $I_I$<br>CA3059<br>CA3079<br><i>See Fig. 10</i>  |   | –      | 220      | 1000  | nA            |
|  |   | –      | 220      | 2000  | nA            |
| Common-Mode Input<br>Voltage Range, $V_{CMR}$  | Terms. 9 and 13 connected   | –      | 1.5 to 5 | –     | V             |
| Sensitivity, $\Delta V_{13}^{\neq}$<br>(Pulse Mode)<br><i>See Figs. 5(a), 12</i>   | Term. 12 open   | –      | 6        | –     | mV            |

<sup>≠</sup> Required voltage change at Term. 13 to either turn OFF the triac when ON or turn ON the triac when OFF.

<sup>\*</sup> Pulse duration in 50 Hz applications is approximately 15% longer than shown in Fig. 8(b).

<sup>•</sup> The values given in the Electrical Characteristics Chart at 120 V also apply for operation at input voltages of 208/230 V, and 277 V, except for Pulse Duration. However, the series resistor (RS) must have the indicated value, shown in the chart in Fig. 1, for the specified input voltage.

# CA3059, CA3079

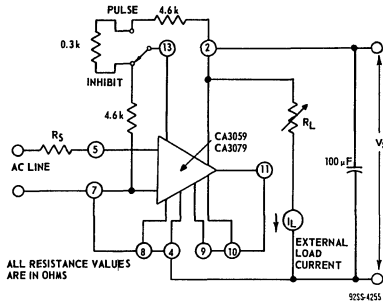


Fig. 3(a)—DC supply voltage test circuit for CA3059 and CA3079.

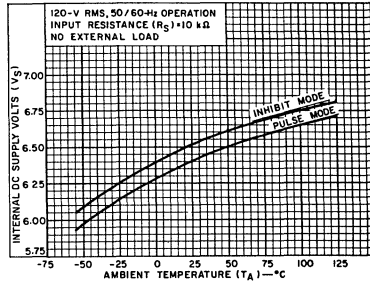


Fig. 3(b)—DC supply voltage vs. ambient temperature for CA3059 and CA3079.

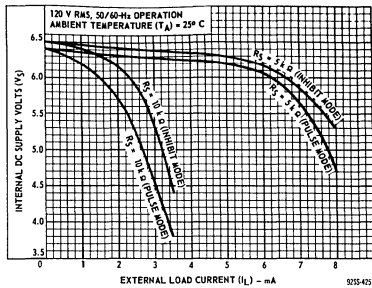


Fig. 3(c)—DC supply voltage vs. external load current for CA3059 and CA3079.

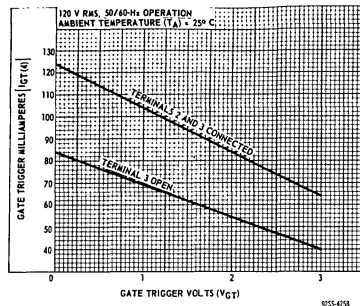


Fig. 4—Gate trigger current vs. gate trigger voltage for CA3059 and CA3079.

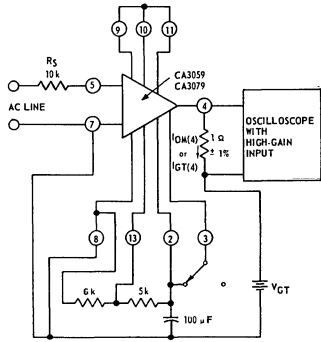


Fig. 5(a)—Peak output (pulsed) and gate trigger current with internal power supply test circuit for CA3059 and CA3079.

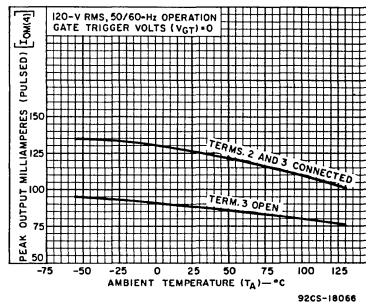


Fig. 5(b)—Peak output current (pulsed) vs. ambient temperature for CA3059 and CA3079.

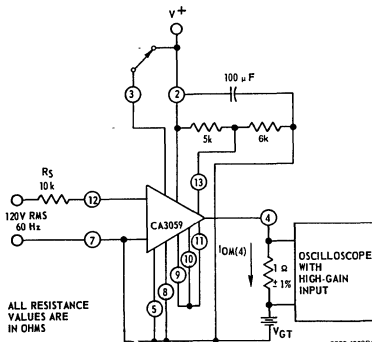


Fig. 6(a)—Peak output current (pulsed) with external power supply test circuit for CA3059.

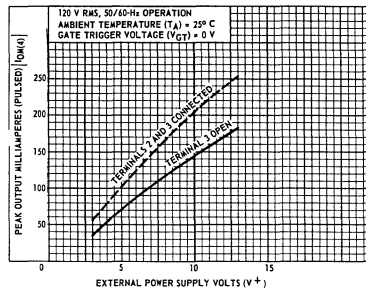


Fig. 6(b)—Peak output current (pulsed) vs. external power supply voltage for CA3059.

# CA3059, CA3079

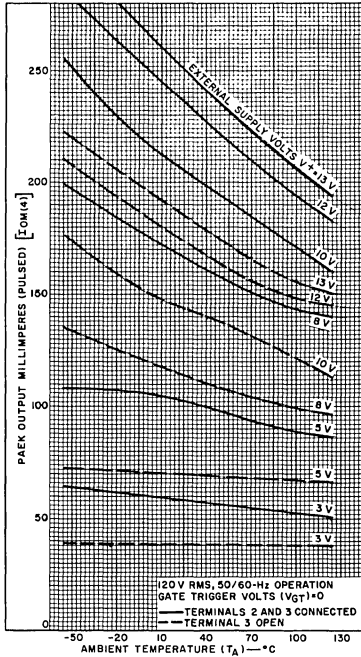


Fig. 6(c) - Peak output current (pulsed) vs ambient temperature for CA3059.

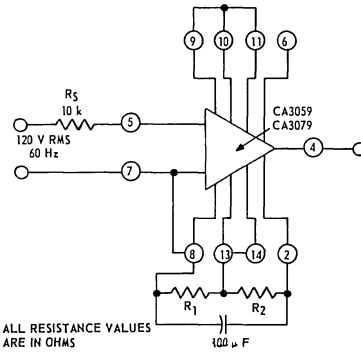


Fig. 7(a) - Input inhibit voltage ratio test circuit for CA3059 and CA3079.

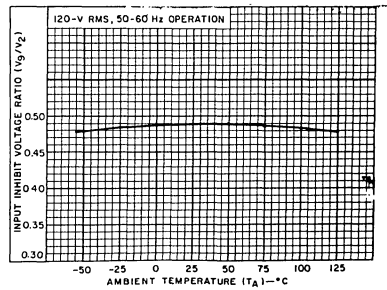


Fig. 7(b) - Input inhibit voltage ratio vs ambient temperature for CA3059 and CA3079.

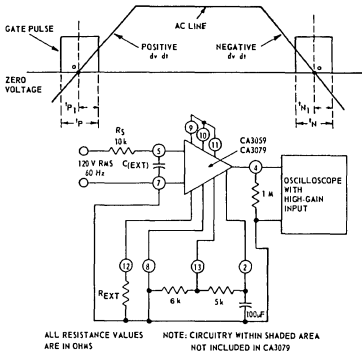


Fig. 8(a) - Gate pulse duration test circuit with associated waveform for CA3059 and CA3079.

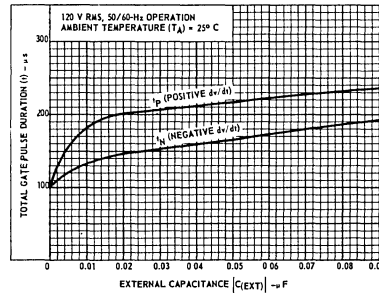


Fig. 8(b) - Total gate pulse duration vs external capacitance for CA3059 and CA3079.

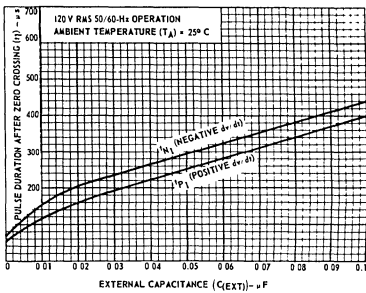


Fig. 8(c) - Pulse duration after zero crossing vs external capacitance for CA3059 and CA3079.

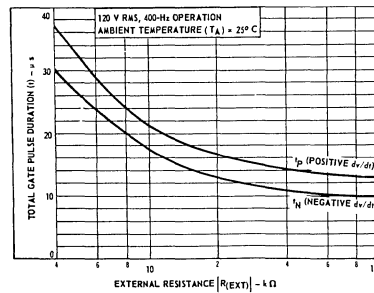


Fig. 8(d) - Total gate pulse duration vs external resistance for CA3059.

2  
POWER PROCESSING  
CIRCUITS

# CA3059, CA3079

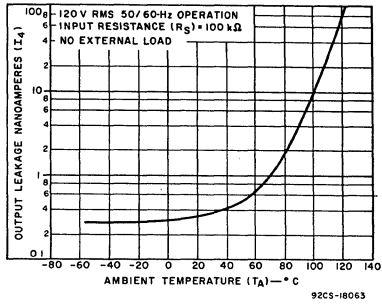


Fig. 9—Output leakage current (inhibit mode) vs. ambient temperature for CA3059 and CA3079.

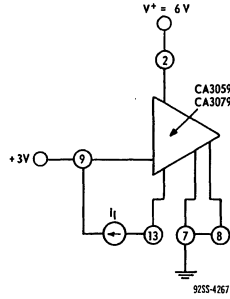
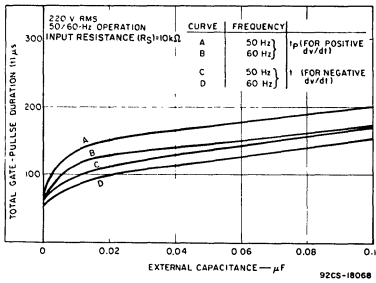
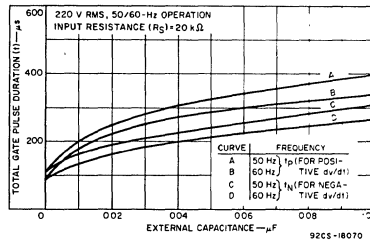


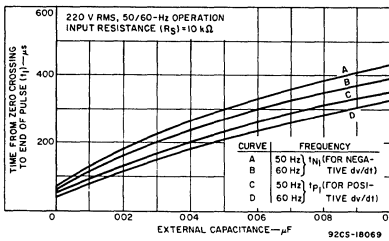
Fig. 10—Input bias current test circuit for CA3059 and CA3079.



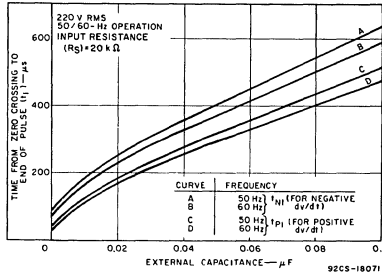
(a)



(b)



(c)



(d)

Fig. 11—Relative pulse width and location of zero crossing for 220-volt operation for CA3059 and CA3079.

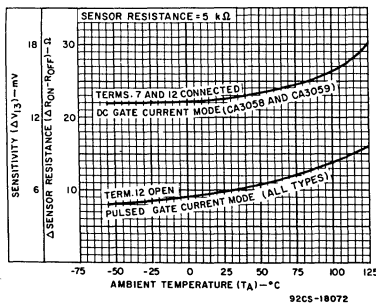


Fig. 12—Sensitivity vs. ambient temperature for CA3059 and CA3079.

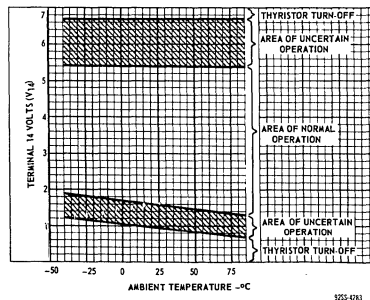


Fig. 13—Operating regions for built-in protection circuit for CA3059.

## CA3059, CA3079

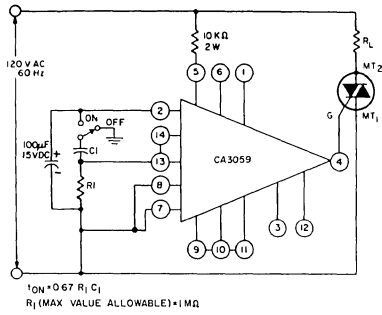


Fig. 14—Line-operated one-shot timer.

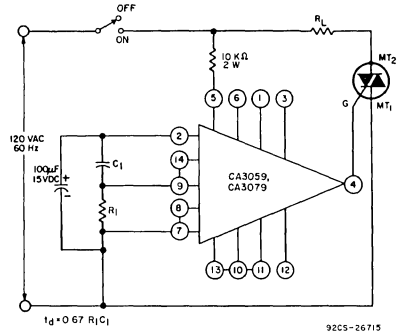


Fig. 15—Line-operated thyristor control time delay turn-on circuit.

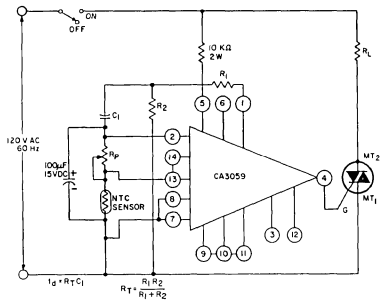


Fig. 16—On/off temperature control circuit with delayed turn-on.

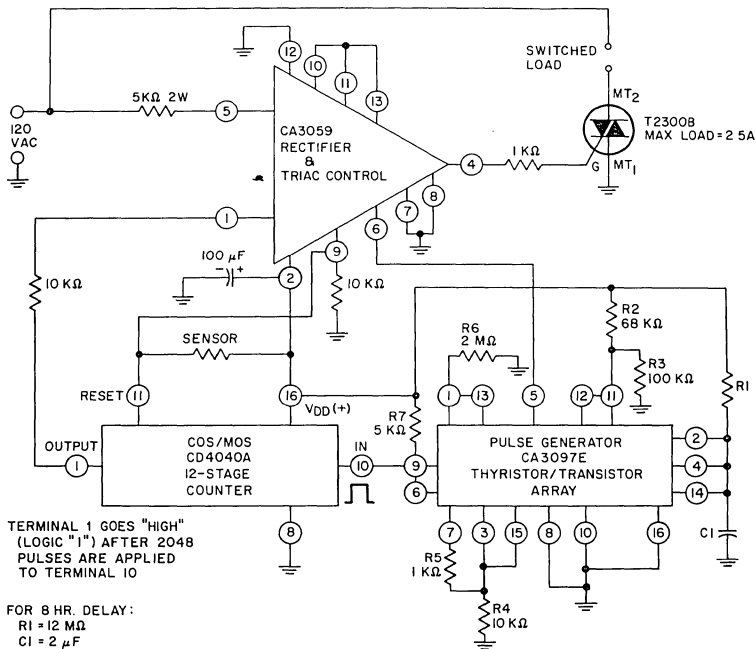


Fig. 17(a)—Line-operated IC timer for long time periods.

# CA3059, CA3079

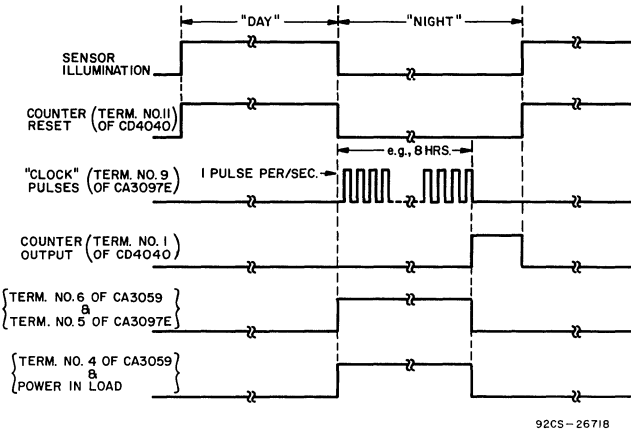


Fig. 17(b)—Timing diagram for Fig. 17(a).

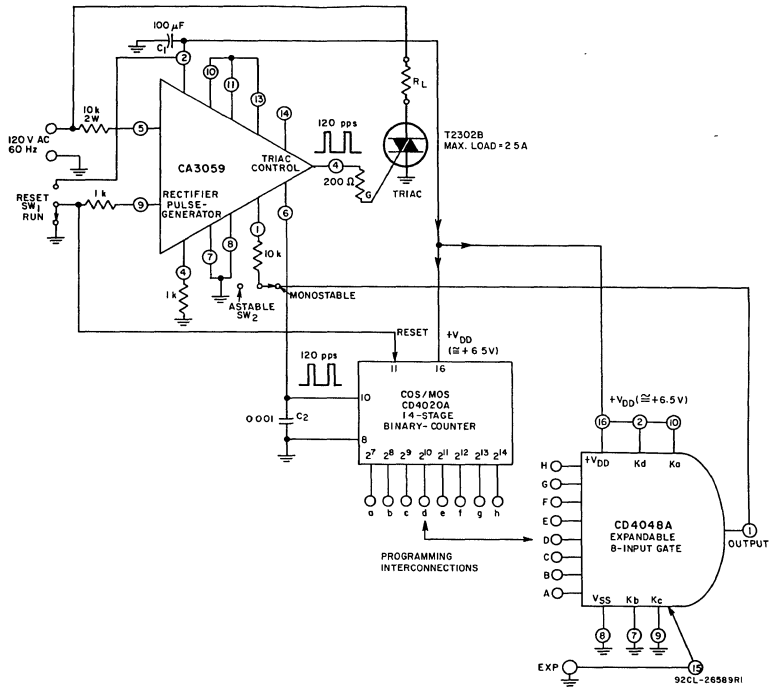


Fig. 18(a)—Programmable ultra-accurate line-operated timer.  
(Programmable over the range from 0.5333 seconds to 2 minutes, 16 seconds in 0.5333-second increments)

## CA3059, CA3079

| Time Periods<br>( $t = 0.5333 \text{ s}$ ) | 1 t | 2 t | 4 t | 8 t | 16 t | 32 t | 64 t | 128 t | $t_0$ |
|--|-----|-----|-----|-----|------|------|------|-------|-------|
| <b>Terminals</b>                           |     |     |     |     |      |      |      |       |       |
| CD4020A                                    | a   | b   | c   | d   | e    | f    | g    | h     |       |
| CD4048A                                    | A   | B   | C   | D   | E    | F    | G    | H     |       |
|  | C   | NC  | NC  | NC  | NC   | NC   | NC   | NC    | 1 t   |
|  | NC  | C   | NC  | NC  | NC   | NC   | NC   | NC    | 2 t   |
|  | C   | C   | NC  | NC  | NC   | NC   | NC   | NC    | 3 t   |
|  | NC  | NC  | C   | NC  | NC   | NC   | NC   | NC    | 4 t   |
|  | C   | NC  | C   | NC  | NC   | NC   | NC   | NC    | 5 t   |
|  | NC  | C   | C   | NC  | NC   | NC   | NC   | NC    | 6 t   |
|  | C   | C   | C   | NC  | NC   | NC   | NC   | NC    | 7 t   |
|  | NC  | NC  | NC  | C   | NC   | NC   | NC   | NC    | 8 t   |
|  | C   | NC  | NC  | C   | NC   | NC   | NC   | NC    | 9 t   |
|  | NC  | C   | NC  | C   | NC   | NC   | NC   | NC    | 10 t  |
|  | C   | C   | NC  | C   | NC   | NC   | NC   | NC    | 11 t  |
|  | NC  | NC  | C   | C   | NC   | NC   | NC   | NC    | 12 t  |
|  | C   | NC  | C   | C   | NC   | NC   | NC   | NC    | 13 t  |
|  | NC  | C   | C   | C   | NC   | NC   | NC   | NC    | 14 t  |
|  | C   | C   | C   | C   | NC   | NC   | NC   | NC    | 15 t  |
|  | C   | C   | C   | C   | NC   | C    | C    | NC    | 111 t |
|  | NC  | NC  | NC  | NC  | C    | C    | C    | NC    | 112 t |
|  | C   | NC  | NC  | NC  | C    | C    | C    | NC    | 113 t |
|  | C   | C   | C   | C   | C    | C    | C    | C     | 255 t |

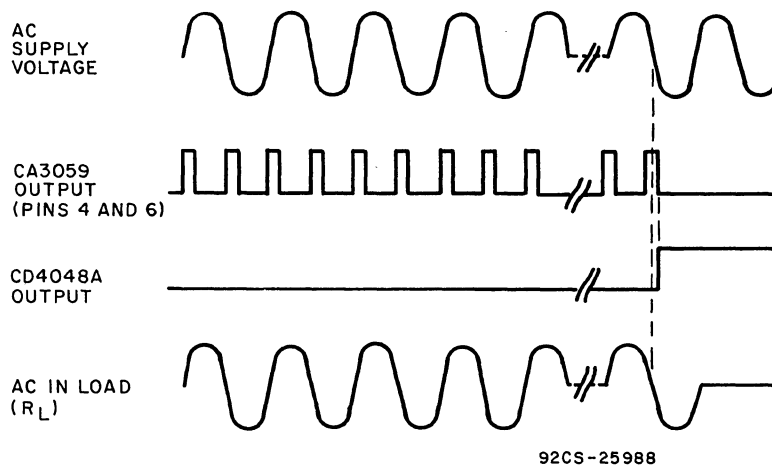
**Notes:**

$t_0$  = Total time delay =  $n_1 t + n_2 t + \dots + n_n t$ .

C = Connect. For example, interconnect terminal a of the CD4020A and terminal A of the CD4048A.

NC = No Connection. For example, terminal b of the CD4020A open and terminal B of the CD4048A connected to +V<sub>DD</sub> bus.

*Fig. 18(b) – "Programming" table for Fig. 18(a).*



*Fig. 18(c) – Timing diagram for Fig. 18(a).*



# CA3059, CA3079

## OPERATING CONSIDERATIONS

### Power Supply Considerations for CA3059 and CA3079

The CA3059 and CA3079 are intended for operation as self-powered circuits with the power supplied from an AC line through a dropping resistor. The internal supply is designed to allow for some current to be drawn by the auxiliary power circuits. Typical power supply characteristics are given in Figs. 3(b) and 3(c).

### Power Supply Considerations for CA3059

The output current available from the internal supply may not be adequate for higher power applications. In such applications an external power supply with a higher voltage should be used with a resulting increase in the output level. (See Fig. 5 for the peak output current characteristics). When an external power supply is used, Terminal 5 should be connected to Terminal 7 and the synchronizing voltage applied to Terminal 12 as illustrated in Fig. 5(a).

### Operation of Built-in Protection for the CA3059

A special feature of the CA3059 is the inclusion of a protection circuit which, when connected, removes power from the load if the sensor either shorts or opens. The protection circuit is activated by connecting Terminal 14 to Terminal 13 as shown in Fig. 1. To assure proper operation of the protection circuit the following conditions should be observed:

1. Use the internal supply and limit the external load current to 2 mA with a 5 k $\Omega$  dropping resistor.
2. Set the value of  $R_p$  and sensor resistance ( $R_X$ ) between 2 k $\Omega$  and 100 k $\Omega$ .
3. The ratio of  $R_X$  to  $R_p$ , typically, should be greater than 0.33 and less than 3. If either of these ratios is not met with an unmodified sensor over the entire anticipated temperature range, then either a series or shunt resistor must be added to avoid undesired activation of the circuit.

If operation of the protection circuit is desired under conditions other than those specified above, then apply the data given in Fig. 13.

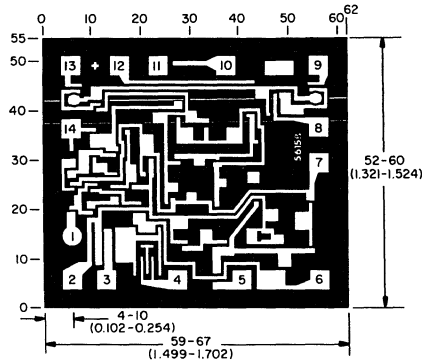
### External Inhibit Function for the CA3059

A priority inhibit command may be applied to Terminal 1. The presence of at least +1.2 V at 10  $\mu$ A will remove drive from the thyristor. This required level is compatible with DTL or T<sup>2</sup>L logic. A logical 1 activates the inhibit function.

### DC Gate Current Mode for the CA3059

Connecting Terminals 7 and 12 disables the zero-crossing detector and permits the flow of gate current on demand from the differential sensing amplifier. This mode of operation is useful when comparator operation is desired or when inductive loads are switched. Care must be exercised to avoid overloading the internal power supply when operating in this mode. A sensitive gate thyristor should be used with a resistor placed between Terminal 4 and the gate in order to limit the gate current.

For a list of RCA thyristors, see RCA Thyristor Data Bulletin, File No. 406, dated 5-75.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid gradations are in mils ( $10^{-3}$  inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and pad layout for CA3059H and CA3079H.

# CA3085, CA3085A CA3085B

Positive Voltage Regulators  
From 1.7V to 46V at Currents Up to 100mA

August 1991

### Features

- Up to 100 mA Output Current
- Input and Output Short-Circuit Protection
- Load and Line Regulation ..... 0.025%
- Pin Compatible with LM100 Series
- Adjustable Output Voltage

### Applications

- Shunt Voltage Regulator
- Current Regulator
- Switching Voltage Regulator
- High-Current Voltage Regulator
- Combination Positive and Negative Voltage Regulator
- Dual Tracking Regulator

### Description

The CA3085, CA3085A, and CA3085B are silicon monolithic integrated circuits designed specifically for service as voltage regulators at output voltages ranging from 1.7 to 46 volts at currents up to 100 milliamperes.

A block diagram of the CA3085 Series is shown in Fig. 1. The diagram shows the connecting terminals that provide access to the regulator circuit components. The voltage regulators provide important features such as: frequency compensation, short-circuit protection, temperature-compensated reference voltage, current limiting, and booster input. These devices are useful in a wide range of applications for regulating high-current, switching, shunt, and positive and negative voltages. They are also applicable for current and dual-tracking regulation.

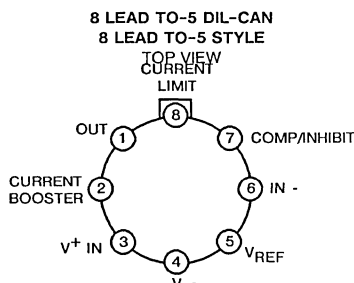
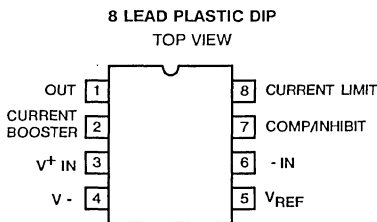
The CA3085A and CA3085B have output current capabilities up to 100 mA and the CA3085 up to 12 mA without the use of external pass transistors. However, all the devices can provide voltage regulation at load currents greater than 100 mA with the use of suitable external pass transistors. The CA3085 Series has an unregulated input voltage ranging from 7.5 to 30V (CA3085), 7.5 to 40V (CA3085A), and 7.5 to 50V (CA3085B) and a minimum regulated output voltage of 26V (CA3085), 36V (CA3085A), and 46V (CA3085B).

These types are supplied in the 8 lead TO-5 style package (CA3085, CA3085A, CA3085B, and the 8 lead TO-5 with dual-in-line formed leads ("DIL-CAN", CA3085S, CA3085AS, CA3085BS). The CA3085 is also supplied in the 8 lead dual-in-line plastic package ("MINI-DIP", CA3085E), and in chip form (CA3085H).

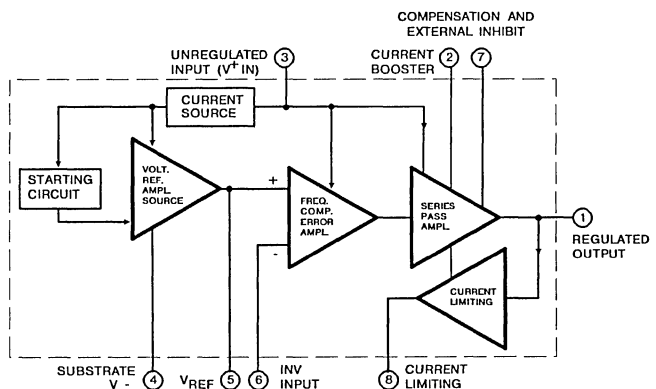
| TYPE    | V <sub>IN</sub> RANGE<br>V | V <sub>OUT</sub> RANGE<br>V | MAX I <sub>OUT</sub><br>mA | MAX LOAD REGULATION<br>% V <sub>OUT</sub> |
|---------|----------------------------|-----------------------------|----------------------------|---|
| CA3085  | 7.5 to 30                  | 1.8 to 26                   | 12*                        | 0.1                                       |
| CA3085A | 7.5 to 40                  | 1.7 to 36                   | 100                        | 0.15                                      |
| CA3085B | 7.5 to 50                  | 1.7 to 46                   | 100                        | 0.15                                      |

\*This value may be extended to 100 mA; however, regulation is not specified beyond 12 mA.

### Pinouts



### Functional Block Diagram



# CA3085, CA3085A, CA3085B

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES at  $T_A = 25^\circ\text{C}$

POWER DISSIPATION: WITHOUT HEAT SINK | WITH HEAT SINK (TO-5 ONLY)

|   |  |
|---|--|
| up to $T_A = 55^\circ\text{C}$ ..... 630 mW                                       | up to $T_C = 55^\circ\text{C}$ ..... 1.6 W   |
| above $T_A = 55^\circ\text{C}$ derate linearly @ $6.67 \text{ mW}/^\circ\text{C}$ | above $T_C = 55^\circ\text{C}$ ..... derate linearly at $16.7 \text{ mW}/^\circ\text{C}$ |

TEMPERATURE RANGE:

|                 |               |
|-----------------|---------------|
| Operating ..... | -55 to +125°C |
| Storage .....   | -65 to +150°C |

UNREGULATED INPUT VOLTAGE:

|               |      |
|---------------|------|
| CA3085 .....  | 30 V |
| CA3085A ..... | 40 V |
| CA3085B ..... | 50 V |

LEAD TEMPERATURE (DURING SOLDERING):

At distance  $1/16 \pm 1/32$  inch ( $1.59 \pm 0.79$ mm)  
from case for 10 seconds max. .... +265°C

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical Terminal No. 7 and horizontal Terminal No. 1 is +3 to -10 volts.

MAXIMUM VOLTAGE RATINGS

| TERMINAL No. | 5 | 6        | 7 | 8         | 1         | 2                      | 3                    | 4                    |
|--------------|---|----------|---|-----------|-----------|------------------------|----------------------|----------------------|
| 5            | - | +5<br>-5 | . | .         | .         | .                      | .                    | +10<br>0             |
| 6            | - | -        | . | .         | .         | .                      | .                    | .                    |
| 7            | - | -        | - | +3<br>-10 | +3<br>-10 | .                      | .                    | + $\frac{1}{2}$<br>0 |
| 8            | - | -        | - | -         | +5<br>-1  | .                      | .                    | .                    |
| 1            | - | -        | - | -         | -         | +10<br>- $\frac{1}{2}$ | 0<br>- $\frac{1}{2}$ | + $\frac{1}{2}$<br>0 |
| 2            | - | -        | - | -         | -         | -                      | 0                    | + $\frac{1}{2}$<br>0 |
| 3            | - | -        | - | -         | -         | -                      | -                    | + $\frac{1}{2}$<br>0 |
| 4            | - | -        | - | -         | -         | -                      | -                    | Substrate<br>& Case  |

\* Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

‡ 30 V for CA3085  
40 V for CA3085A  
50 V for CA3085B

MAXIMUM CURRENT RATINGS

| TERMINAL No. | $I_{IN}$ mA | $I_{OUT}$ mA |
|--------------|-------------|--------------|
| 5            | 10          | 1.0          |
| 6            | 1.0         | -0.1         |
| 7            | 1.0         | -1.0         |
| 8            | 0.1         | 10           |
| 1            | 20          | 150          |
| 2            | 150         | 60           |
| 3            | 150         | 60           |
| 4            | -           | -            |

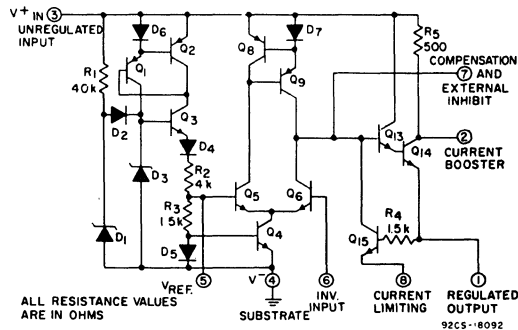


Fig.2—Schematic diagram of CA3085 Series.

# CA3085, CA3085A, CA3085B

## ELECTRICAL CHARACTERISTICS

| CHARACTERISTICS  | SYMBOL                              | Test Circuit Fig. No. | TEST CONDITIONS  |      |      | LIMITS |        |      |         |        |       | UNITS |         |      |                   |
|--|-------------------------------------|-----------------------|--|------|------|--------|--------|------|---------|--------|-------|-------|---------|------|-------------------|
|  |                                     |                       | T <sub>A</sub> = 25°C<br>(Unless indicated otherwise)  |      |      | CA3085 |        |      | CA3085A |        |       |       | CA3085B |      |                   |
|  |                                     |                       | MIN.   | TYP. | MAX. | MIN.   | TYP.   | MAX. | MIN.    | TYP.   | MAX.  |       |         |      |                   |
| Reference Voltage  | V <sub>REF</sub>                    | 4                     | V <sup>+</sup> <sub>IN</sub> = 15V   |      |      | 1.4    | 1.6    | 1.8  | 1.5     | 1.6    | 1.7   | 1.5   | 1.6     | 1.7  | V                 |
| Quiescent Regulator Current                              | I <sub>quiescent</sub>              | 4                     | V <sup>+</sup> <sub>IN</sub> = 30V   |      |      | —      | 3.3    | 4.5  | —       | —      | —     | —     | —       | —    | mA                |
|  |                                     |                       | V <sup>+</sup> <sub>IN</sub> = 40V   |      |      | —      | —      | —    | —       | 3.65   | 5     | —     | —       | —    |                   |
|  |                                     |                       | V <sup>+</sup> <sub>IN</sub> = 50V   |      |      | —      | —      | —    | —       | —      | —     | —     | —       | 4.05 |                   |
| Input Voltage Range                                      | V <sub>IN(range)</sub>              | —                     | —  |      |      | 7.5    | —      | 30   | 7.5     | —      | 40    | 7.5   | —       | 50   | V                 |
| Maximum Output Voltage                                   | V <sub>O(max.)</sub>                | 4                     | V <sup>+</sup> <sub>IN</sub> = 30, 40, 50V#; R <sub>L</sub> = 365Ω; Term. No. 6 to Gnd.            |      |      | 26     | 27     | —    | 36      | 37     | —     | 46    | 47      | —    | V                 |
| Minimum Output Voltage                                   | V <sub>O(min.)</sub>                | 4                     | V <sup>+</sup> <sub>IN</sub> = 30V   |      |      | —      | 1.6    | 1.8  | —       | 1.6    | 1.7   | —     | 1.6     | 1.7  | V                 |
| Input-Output Voltage Differential                        | V <sub>IN-VOUT</sub>                | —                     | —  |      |      | 4      | —      | 28   | 4       | —      | 38    | 3.5   | —       | 48   | V                 |
| Limiting Current   | I <sub>LIM</sub>                    | 7                     | V <sup>+</sup> <sub>IN</sub> = 16V, V <sup>+</sup> <sub>OUT</sub> = 10V<br>R <sub>SCP</sub> * = 6Ω |      |      | —      | 96     | 120  | —       | 96     | 120   | —     | 96      | 120  | mA                |
| Load Regulation*   | —                                   | —                     | I <sub>L</sub> = 1 to 100mA, R <sub>SCP</sub> = 0  |      |      | —      | —      | —    | —       | 0.025  | 0.15  | —     | 0.025   | 0.15 | %V <sub>OUT</sub> |
|  |                                     |                       | I <sub>L</sub> = 1 to 100mA, R <sub>SCP</sub> = 0<br>T <sub>A</sub> = 0°C to +70°C                 |      |      | —      | —      | —    | —       | 0.035  | 0.6   | —     | 0.035   | 0.6  |                   |
|  |                                     |                       | I <sub>L</sub> = 1 to 12mA, R <sub>SCP</sub> = 0   |      |      | —      | 0.003  | 0.1  | —       | —      | —     | —     | —       | —    |                   |
| Line Regulation <sup>▲</sup>                             | —                                   | —                     | I <sub>L</sub> = 1 mA, R <sub>SCP</sub> = 0  |      |      | —      | 0.025  | 0.1  | —       | 0.025  | 0.075 | —     | 0.025   | 0.04 | %V                |
|  |                                     |                       | I <sub>L</sub> = 1 mA, R <sub>SCP</sub> = 0<br>T <sub>A</sub> = 0°C to +70°C                       |      |      | —      | 0.04   | 0.15 | —       | 0.04   | 0.1   | —     | 0.04    | 0.08 |                   |
| Equivalent Noise Output Voltage                          | V <sub>NOISE</sub>                  | 11                    | V <sup>+</sup> <sub>IN</sub> = 25V   |      |      | —      | 0.5    | —    | —       | 0.5    | —     | —     | 0.5     | —    | mV p-p            |
|  |                                     |                       | C <sub>REF</sub> = 0   |      |      | —      | 0.3    | —    | —       | 0.3    | —     | —     | —       | 0.3  |                   |
| Ripple Rejection   | —                                   | 12                    | V <sup>+</sup> <sub>IN</sub> = 25V   |      |      | —      | 50     | —    | —       | 50     | —     | 45    | 50      | —    | dB                |
|  |                                     |                       | f = 1kHz   |      |      | —      | 56     | —    | —       | 56     | —     | 50    | 56      | —    |                   |
| Output Resistance  | r <sub>o</sub>                      | 12                    | V <sup>+</sup> <sub>IN</sub> = 25V, f = 1kHz   |      |      | —      | 0.075  | 1.1  | —       | 0.075  | 0.3   | —     | 0.075   | 0.3  | Ω                 |
| Temperature Coefficient of Reference and Output Voltages | ΔV <sub>REF</sub> , ΔV <sub>o</sub> | —                     | I <sub>L</sub> = 0, V <sub>REF</sub> = 1.6V  |      |      | —      | 0.0035 | —    | —       | 0.0035 | —     | —     | 0.0035  | —    | %°C               |
|  |                                     |                       | —  |      |      | —      | —      | —    | —       | —      | —     | —     | —       | —    |                   |
| Load Transient Recovery Time:                            | t <sub>ON</sub>                     | 16                    | V <sup>+</sup> <sub>IN</sub> = 25V, +50mA Step   |      |      | —      | 1      | —    | —       | 1      | —     | —     | 1       | —    | μs                |
|  |                                     |                       | Turn Off   |      |      | —      | 3      | —    | —       | 3      | —     | —     | —       | 3    |                   |
| Line Transient Recovery Time:                            | t <sub>ON</sub>                     | —                     | V <sup>+</sup> <sub>IN</sub> = 25V, f = 1kHz, 2V Step  |      |      | —      | 0.8    | —    | —       | 0.8    | —     | —     | 0.8     | —    | μs                |
|  |                                     |                       | Turn Off   |      |      | —      | 0.4    | —    | —       | 0.4    | —     | —     | —       | 0.4  |                   |

# 30V (CA3085), 40V(CA3085A), 50V(CA3085B)

\* R<sub>SCP</sub>: Short-circuit protection resistance

● Load Regulation =  $\frac{\Delta V_{OUT}}{V_{OUT(initial)}} \times 100\%$

▲ Line Regulation =  $\frac{(\Delta V_{OUT})}{[V_{OUT(initial)} (\Delta V_{IN})]} \times 100\%$

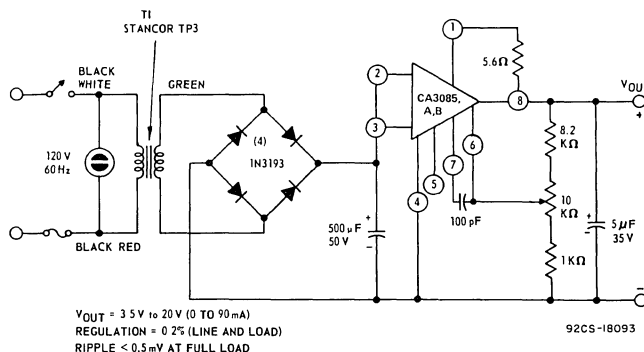


Fig.3—Application of the CA3085 Series in a typical power supply.

# CA3085, CA3085A, CA3085B

## TEST CIRCUITS AND TYPICAL CHARACTERISTICS CURVES FOR CA3085 SERIES

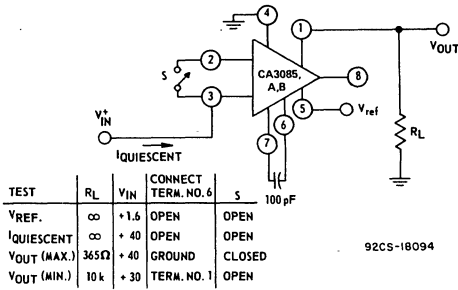


Fig. 4—Test circuit for \$V\_{REF}\$, \$I\_{quiescent}\$, \$V\_{OUT(max.)}\$, \$V\_{OUT(min.)}\$.

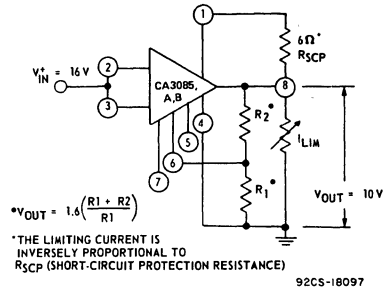


Fig. 7—Test circuit for limiting current

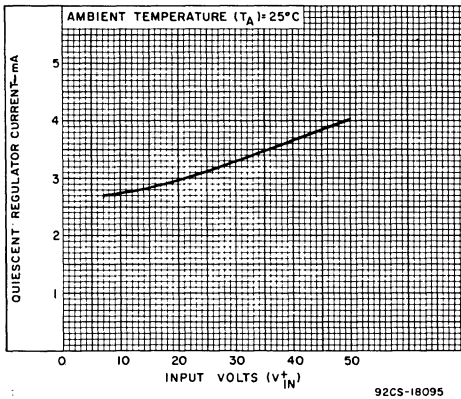


Fig. 5—\$I\_{quiescent}\$ vs. \$V\_{IN}^+\$.

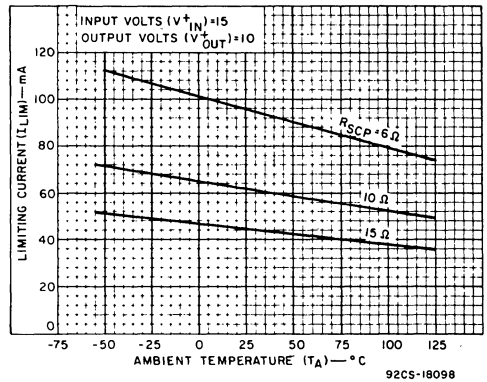


Fig. 8—\$I\_{LIM}\$ vs. \$T\_A\$.

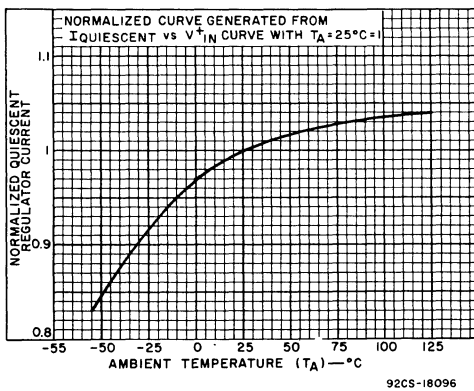


Fig. 6—Normalized \$I\_{quiescent}\$ vs. \$T\_A\$.

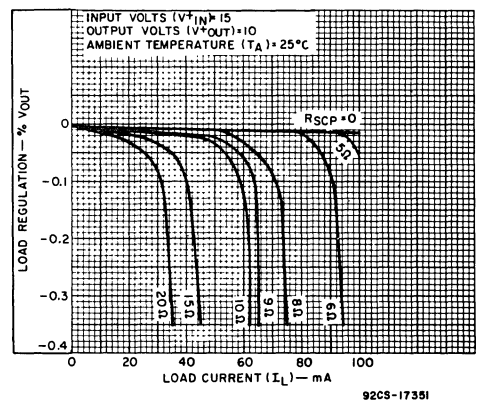


Fig. 9—Load regulation characteristics.

# CA3085, CA3085A, CA3085B

## TEST CIRCUITS AND TYPICAL CHARACTERISTICS CURVES FOR CA3085 SERIES

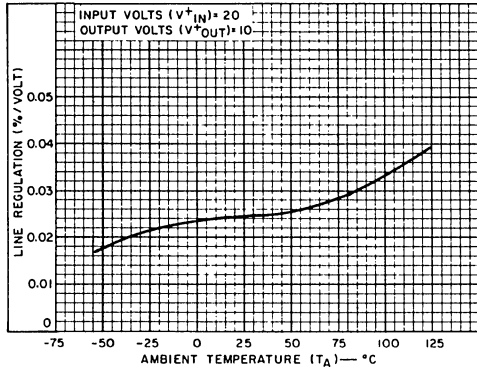


Fig.10—Line regulation temperature characteristics.

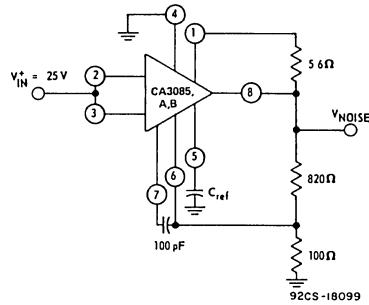


Fig.11—Test circuit for noise voltage.

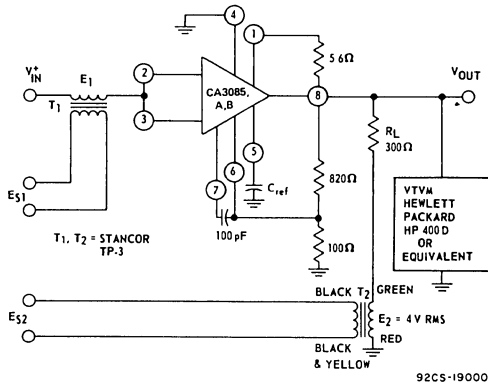


Fig.12—Test circuit for ripple rejection and output resistance.

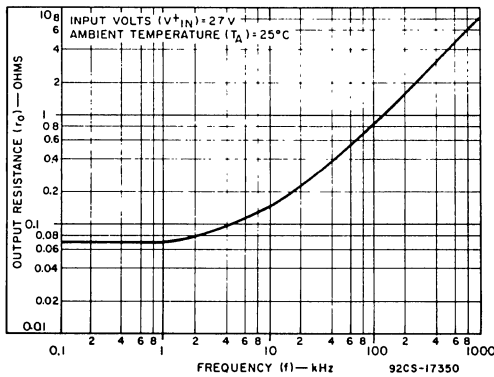


Fig.13— $r_O$  vs.  $f$ .

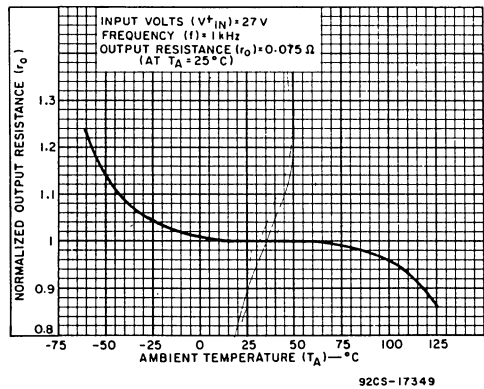


Fig.14—Normalized  $r_O$  vs.  $T_A$ .

### TEST PROCEDURES FOR TEST CIRCUIT FOR RIPPLE REJECTION AND OUTPUT RESISTANCE

#### Output Resistance

Conditions:

1.  $V_{IN} = +25V$ ,  $C_{REF} = 0$ , Short  $E_1$
2. Set  $E_{S2}$  at 1 kHz so that  $E_2 = 4V$  rms
3. Read  $V_{OUT}$  on a VTVM, such as a Hewlett-Packard, HP400D or equivalent
4. Calculate  $R_{OUT}$  from  $R_{OUT} = V_{OUT} (I_{RL}/E_2)$

#### Ripple Rejection — I

Conditions:

1.  $V_{IN} = +25V$ ,  $C_{REF} = 0$ , Short  $E_2$
2. Set  $E_{S1}$  at 1 kHz so that  $E_1 = 3V$  rms
3. Read  $V_{OUT}$  on a VTVM, such as a Hewlett-Packard, HP400D or equivalent
4. Calculate Ripple Rejection from  $20 \log (E_1/V_{OUT})$

#### Ripple Rejection — II

Conditions:

1. Repeat Ripple Rejection I with  $C_{REF} = 2 \mu F$

# CA3085, CA3085A, CA3085B

## TEST CIRCUIT AND TYPICAL CHARACTERISTICS CURVES FOR CA3085 SERIES

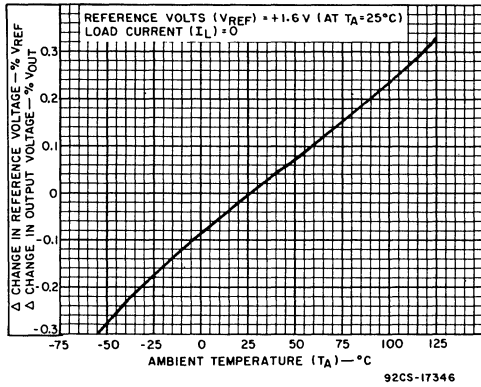


Fig.15—Temperature coefficient of  $V_{REF}$  and  $V_{OUT}$ .

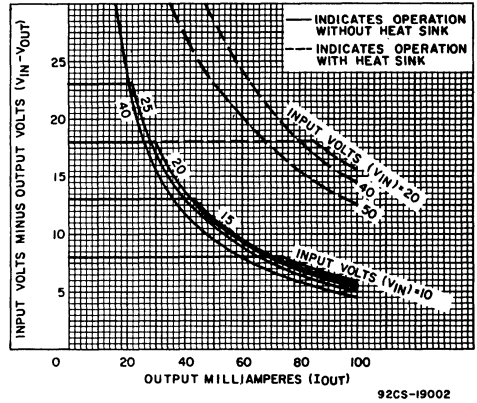


Fig.17—Dissipation limitation ( $V_{IN} - V_{OUT}$  vs.  $I_{OUT}$ ).

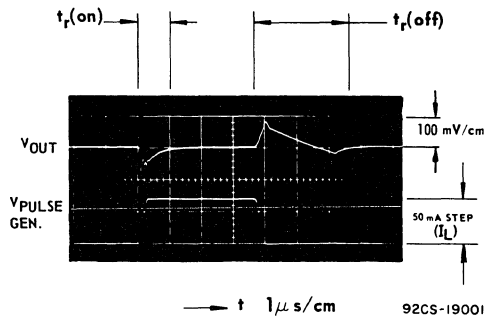
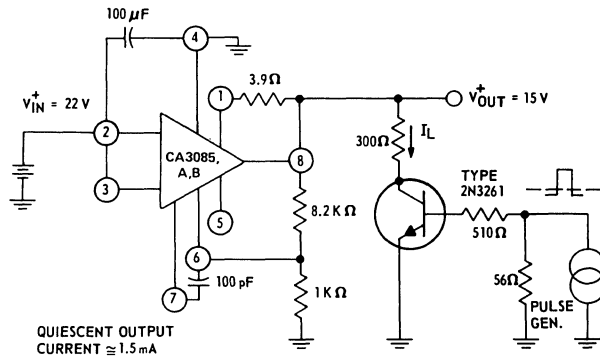


Fig.16—Turn-on and turn-off recovery time test circuit with associated waveforms.

# CA3085, CA3085A, CA3085B

## TYPICAL REGULATOR CIRCUITS USING THE CA3085 SERIES

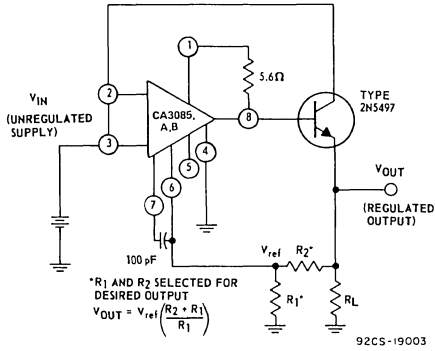


Fig.18—Typical high-current voltage regulator circuit.

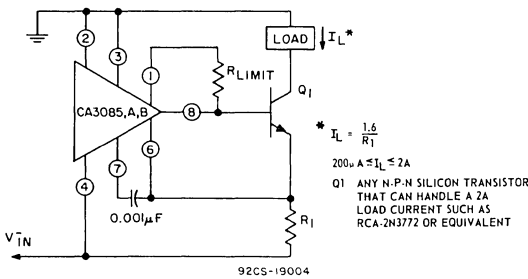
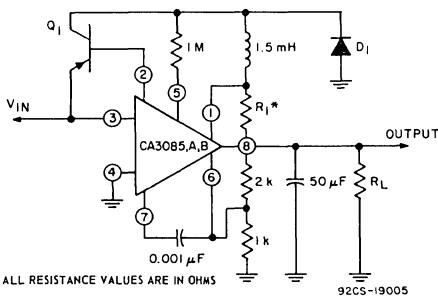
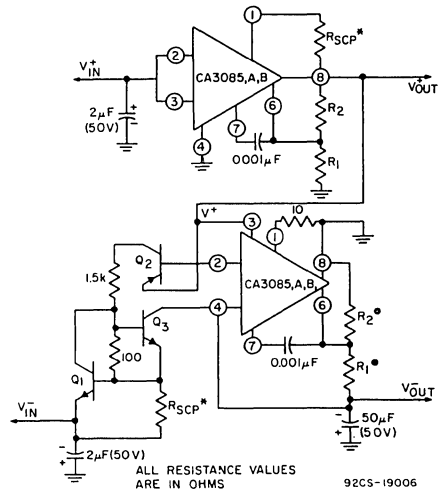


Fig.19—Typical current regulator circuit.



- D1 RCA-1N1763A OR EQUIVALENT
- Q1 RCA-2N5322 OR EQUIVALENT
- \*R<sub>1</sub> = 0.7 I<sub>L</sub> (MAX.)

Fig.20—Typical switching regulator circuit.



- ALL RESISTANCE VALUES ARE IN OHMS
- Q1 RCA-2N2102 OR EQUIVALENT
- Q2 ANY P-N-P SILICON TRANSISTOR (RCA-2N5322 OR EQUIVALENT)
- Q3 ANY N-P-N SILICON TRANSISTOR THAT CAN HANDLE THE DESIRED LOAD CURRENT (RCA-2N3772 OR EQUIVALENT)
- \*  $V_{OUT} = \left( \frac{R_1 + R_2}{R_1} \right)$
- \*R<sub>SCP</sub> SHORT-CIRCUIT PROTECTION RESISTANCE

Fig.21—Combination positive and negative voltage regulator circuit.



PRELIMINARY

May 1991

## Half Bridge Complementary MOSFET Driver

### Features

- Bipolar or Unipolar Supply Operation
- Wide Supply Range .....  $\pm 40V$  to  $+450V$ ,  $-100V$
- Complete MOSFET Protection
- High Output to Logic Supply Isolation
- High Peak Output Current .....  $2A$
- Fast Switching Times .....  $100ns$
- Frequency Range .....  $DC-30kHz$

### Applications

- High Switchmode Power Supplies
- PWM Servo Drives
- Stepper Motor Drives
- DC-DC Converters
- Uninterruptible Power Supplies

### Ordering Information

| PART NUMBER | TEMPERATURE RANGE                          | DESCRIPTION        |
|-------------|--|--------------------|
| HV250CP     | $0^{\circ}C \leq T_A \leq +75^{\circ}C$    | 16 Pin Plastic DIP |
| HV250IP     | $-40^{\circ}C \leq T_A \leq +85^{\circ}C$  | 16 Pin Plastic DIP |
| HV250MJ*    | $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ | 16 Pin Ceramic DIP |

### Description

The HV250 is a monolithic dielectrically isolated high voltage integrated circuit. The circuit provides an interface from digital signals to the gates of complementary power MOSFETs. The circuit has wide supply voltage range, from  $80VDC$  to  $450VDC$  in unipolar connection or  $\pm 40VDC$  to  $+450VDC$  and  $-100VDC$ . In addition the logic supply can float within the high voltage rails.

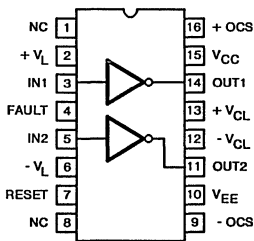
The inputs are TTL compatible when the logic supply is  $5V$ , but will operate up to  $15V$  logic supply.

The outputs provide up to  $2A$  current spikes to drive the gates of power MOSFETs. The actual voltage that the gates are driven to is set by the user, up to  $20V$  for  $V_{GS}$ .

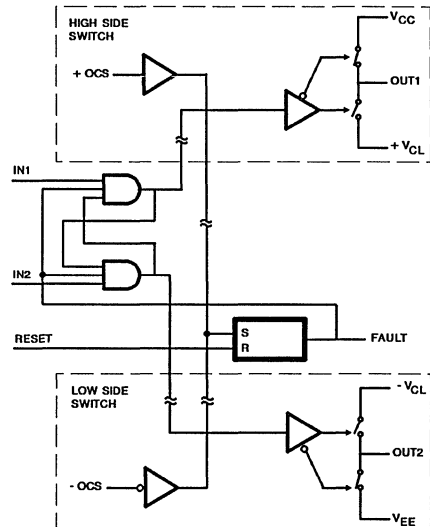
Also on board the chip is an overcurrent sense circuit, which independently sense overcurrent on the high side and the low side. An overcurrent condition sets a latch that disables both outputs. In order to enable the output the reset input must be toggled.

### Pinout

HV250CP (16 PIN PLASTIC DIP)  
TOP VIEW



### Functional Diagram



## Specifications HV250

### Absolute Maximum Ratings

|   |                 |
|---|-----------------|
| Voltage Between +V <sub>S</sub> and -V <sub>S</sub> ..... | 500V            |
| Voltage Between +V <sub>I</sub> and -V <sub>I</sub> ..... | 30V             |
| Voltage Between -V <sub>S</sub> and -V <sub>I</sub> ..... | 250V            |
| Peak Output Current .....                                 | 2A              |
| Logic Input Voltage .....                                 | +V <sub>L</sub> |
| Over Current Sense to  V <sub>S</sub>   .....             | 7V              |
| Fault Output Current .....                                | 1mA             |

### Operating Temperature Range

|                                    |                                 |
|------------------------------------|---------------------------------|
| HV250CP .....                      | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| HV250IP .....                      | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| HV250MJ* .....                     | -55°C ≤ T <sub>A</sub> ≤ +125°C |
| Storage Temperature Range .....    | -65°C ≤ T <sub>A</sub> ≤ +150°C |
| Maximum Junction Temperature ..... | +175°C                          |

\* Offered at a Later Date

### Electrical Specifications V<sub>CC</sub> = +40V, V<sub>EE</sub> = -40V, C<sub>L</sub> = 10nF, V<sub>L</sub> = 5V Unless Otherwise Specified

| PARAMETER  | TEMP  | HV250CP, HV250IP     |      |                      | UNITS |
|--|-------|----------------------|------|----------------------|-------|
|  |       | MIN                  | TYP  | MAX                  |       |
| <b>INPUT CHARACTERISTICS</b>                             |       |                      |      |                      |       |
| Input Voltage, High (V <sub>IH</sub> )                   | Full  | 2.4                  | -    | -                    | V     |
| Input Voltage, Low (V <sub>IL</sub> )                    | Full  | -                    | -    | 0.8                  | V     |
| Input Current (I <sub>IH</sub> )                         | +25°C | -                    | -    | 300                  | μA    |
|  | Full  | -                    | -    | 300                  | μA    |
| Input Current, Low (I <sub>IL</sub> )                    | +25°C | -150                 | -    | -                    | μA    |
|  | Full  | -150                 | -    | -                    | μA    |
| Overcurrent Input Threshold                              | +25°C | 80                   | 100  | 120                  | mV    |
|  | Full  | 75                   | 100  | 125                  | mV    |
| <b>TRANSFER CHARACTERISTICS</b>                          |       |                      |      |                      |       |
| Turn-On Delay (T <sub>D1</sub> , T <sub>D3</sub> )       | +25°C | -                    | -    | 1                    | μs    |
|  | Full  | -                    | -    | 1                    | μs    |
| Turn-On Delay Skew (T <sub>D1</sub> , T <sub>D3</sub> )  | +25°C | -                    | ±300 | -                    | ns    |
|  | Full  | -                    | ±300 | -                    | ns    |
| Turn-Off Delay (T <sub>D2</sub> , T <sub>D4</sub> )      | +25°C | -                    | -    | 1                    | μs    |
|  | Full  | -                    | -    | 1                    | μs    |
| Turn-Off Delay Skew (T <sub>D2</sub> , T <sub>D4</sub> ) | +25°C | -                    | ±100 | -                    | ns    |
|  | Full  | -                    | ±100 | -                    | ns    |
| Current Limit Sense to Output Turn-Off Delay             | +25°C | -                    | 500  | -                    | ns    |
|  | Full  | -                    | 500  | -                    | ns    |
| Current Limit Sense to Fault Output Turn-Off Delay       | +25°C | 50                   | -    | 150                  | ns    |
|  | Full  | 50                   | -    | 150                  | ns    |
| Reset Delay (T <sub>D6</sub> )                           | +25°C | -                    | 500  | -                    | ns    |
|  | Full  | -                    | 500  | -                    | ns    |
| <b>OUTPUT CHARACTERISTICS</b>                            |       |                      |      |                      |       |
| Output Rise Time   | Full  | -                    | 100  | 150                  | ns    |
| Output Fall Time   | Full  | -                    | 100  | 150                  | ns    |
| OUT1 Voltage (High)                                      | Full  | +V <sub>S</sub> -0.2 | -    | -                    | V     |
| OUT1 Voltage (Low)                                       | Full  | -                    | -    | +V <sub>S</sub> -19  | V     |
| OUT2 Voltage (High)                                      | Full  | -V <sub>S</sub> +19  | -    | -                    | V     |
| OUT2 Voltage (Low)                                       | Full  | -                    | -    | -V <sub>S</sub> +0.2 | V     |
| Fault Output (V <sub>OH</sub> )                          | Full  | 4.5                  | -    | -                    | V     |
| Fault Output (V <sub>OL</sub> )                          | Full  | -                    | -    | 0.8                  | V     |
| <b>POWER SUPPLY</b>                                      |       |                      |      |                      |       |
| I <sub>CC</sub>  | Full  | -                    | -    | 200                  | μA    |
| I <sub>EE</sub>  | Full  | -                    | -    | 200                  | μA    |
| I <sub>L</sub>   | Full  | -                    | -    | 4                    | mA    |

**2**  
POWER PROCESSING  
CIRCUITS

# HV250

## Parameter Definitions (Refer to Switching Waveforms)

| SYMBOL   | DEFINITIONS   |
|----------|---|
| $T_{D2}$ | Delay time as measured from the logic input high to low transition (1 to 0) at the 10% point, to the 10% point of the output transition for the high side switch. |
| $T_{D1}$ | Delay time as measured from the logic input low to high transition (0 to 1) at the 10% point, to the 10% point of the output transition for the high side switch. |
| $T_{D4}$ | Same as $T_{D0-1}$ for the low side switch.   |
| $T_{D3}$ | Same as $T_{D1-1}$ for the low side switch.   |
| $T_{R1}$ | Output rise time from the 10% - 90% points for the high side switch.  |
| $T_{R2}$ | Output rise time from the 10% - 90% points for the low side switch.   |
| $T_{F1}$ | Output fall time from the 10% - 90% points for the high side switch.  |
| $T_{F2}$ | Output fall time from the 10% - 90% points for the low side switch.   |
| $T_{D5}$ | Delay time as measured from the overcurrent input 10% point to the fault output high to low transition at the 10% point.  |
| $T_{D6}$ | Delay time as measured from the reset input 10% point to the fault output low to high transition at the 90% point.  |
| $T_{D7}$ | Delay time as measured from the overcurrent 1 input 10% point to output 1 low to high transition at the 90% point.  |
| $T_{D8}$ | Delay time as measured from the overcurrent 2 input 10% point to output 2 high to low transition at the 10% point.  |

## Switching Time Test Circuits

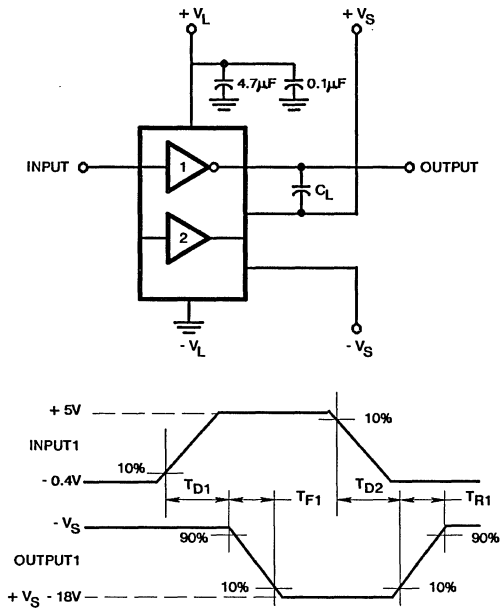


FIGURE 1. INVERTING DRIVE SWITCHING TIME (HIGH SIDE)

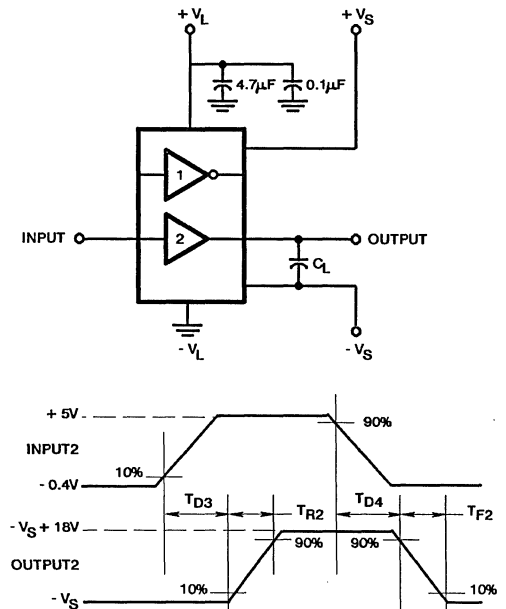
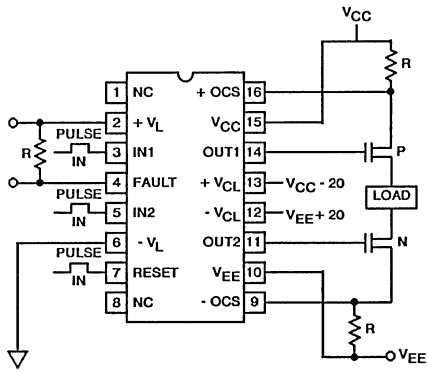


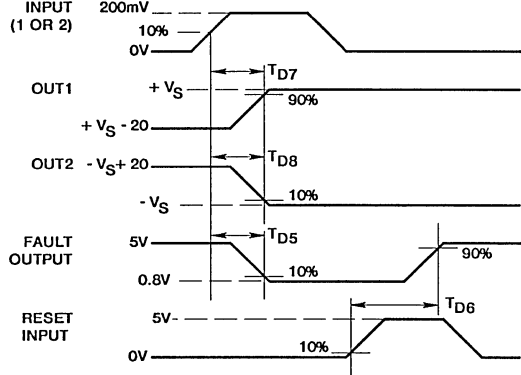
FIGURE 2. NON-INVERTING DRIVER SWITCHING TIME (LOW SIDE)

Overcurrent Test Waveforms

OVERCURRENT TEST CIRCUIT



OVERCURRENT



**PRELIMINARY**

May 1991

## Half Bridge Complementary MOSFET Driver

**Features**

- Bipolar or Unipolar Supply Operation
- Wide Supply Range .....  $\pm 40V$  to  $\pm 225V$
- Complete MOSFET Protection
- High Output to Logic Supply Isolation
- High Peak Output Current ..... **2A**
- Fast Switching Times ..... **100ns**
- Frequency Range ..... **10kHz** to **100kHz**

**Applications**

- High Switchmode Power Supplies
- PWM Servo Drives
- Stepper Motor Drives
- DC-DC Converters
- Uninterruptible Power Supplies

**Ordering Information**

| PART NUMBER | TEMPERATURE RANGE                          | DESCRIPTION        |
|-------------|--|--------------------|
| HV255CP     | $0^{\circ}C \leq T_A \leq +75^{\circ}C$    | 16 Pin Plastic DIP |
| HV255IP     | $-40^{\circ}C \leq T_A \leq +85^{\circ}C$  | 16 Pin Plastic DIP |
| HV255MJ*    | $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ | 16 Pin Ceramic DIP |

**Description**

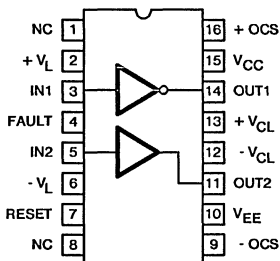
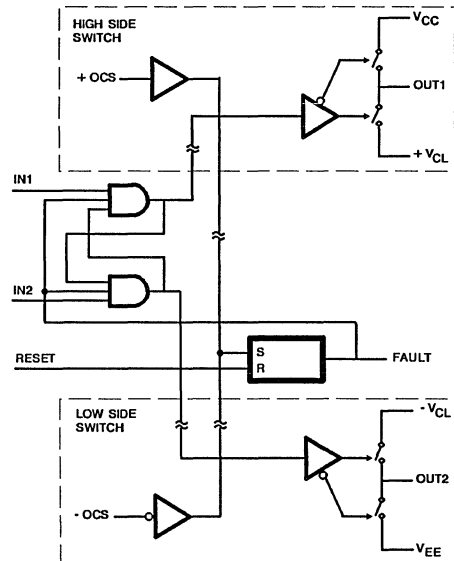
The HV255 is a monolithic dielectrically isolated high voltage integrated circuit. The circuit provides an interface from digital signals to the gates of complementary power MOSFETs or IGBTs. The circuit has wide supply voltage range, from 80VDC to 450VDC in unipolar connection or  $\pm 40VDC$  to  $\pm 225VDC$ . In addition the logic supply can float within the high voltage rails.

The inputs are TTL compatible when the logic supply is 5V, but will operate up to 15V logic supply.

The outputs provide up to 2A current spikes to drive the gates of power MOSFETs or IGBTs. The actual voltage that the gates are driven to is set by the user, up to 20V for  $V_{GS}$ .

Also on board the chip is an overcurrent sense circuit, which independently sense overcurrent on the high side and the low side. An overcurrent condition sets a latch that disables both outputs. In order to enable the output the reset input must be toggled.

**Pinout**

 HV255CP (16 PIN PLASTIC DIP)  
TOP VIEW

**Functional Diagram**


CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.  
Copyright © Harris Corporation 1991 \* Offered at a later date.

 File Number **2847**

## Specifications HV255

### Absolute Maximum Ratings

|   |                 |
|---|-----------------|
| Voltage Between +V <sub>S</sub> and -V <sub>S</sub> ..... | 500V            |
| Voltage Between +V <sub>I</sub> and -V <sub>I</sub> ..... | 30V             |
| Voltage Between -V <sub>S</sub> and -V <sub>I</sub> ..... | 250V            |
| Peak Output Current .....                                 | 2A              |
| Logic Input Voltage .....                                 | +V <sub>L</sub> |
| Over Current Sense to  V <sub>S</sub>   .....             | 7V              |
| Fault Output Current .....                                | 1mA             |

### Operating Temperature Range

|                                    |                                 |
|------------------------------------|---------------------------------|
| HV255CP .....                      | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| HV255IP .....                      | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| HV255MJ* .....                     | -55°C ≤ T <sub>A</sub> ≤ +125°C |
| Storage Temperature Range .....    | -65°C ≤ T <sub>A</sub> ≤ +150°C |
| Maximum Junction Temperature ..... | +175°C                          |

\* Offered at a Later Date

### Electrical Specifications V<sub>CC</sub> = +40V, V<sub>EE</sub> = -40V, C<sub>L</sub> = 10nF, V<sub>L</sub> = 5V Unless Otherwise Specified

| PARAMETER  | TEMP  | HV255CP, HV255IP     |      |                      | UNITS |
|--|-------|----------------------|------|----------------------|-------|
|  |       | MIN                  | TYP  | MAX                  |       |
| <b>INPUT CHARACTERISTICS</b>                             |       |                      |      |                      |       |
| Input Voltage, High (V <sub>IH</sub> )                   | Full  | 2.4                  | -    | -                    | V     |
| Input Voltage, Low (V <sub>IL</sub> )                    | Full  | -                    | -    | 0.8                  | V     |
| Input Current (I <sub>IH</sub> )                         | +25°C | -                    | -    | 300                  | μA    |
|  | Full  | -                    | -    | 300                  | μA    |
| Input Current, Low (I <sub>IL</sub> )                    | +25°C | 150                  | -    | -                    | μA    |
|  | Full  | 150                  | -    | -                    | μA    |
| Overcurrent Input Threshold                              | +25°C | 80                   | 100  | 120                  | mV    |
|  | Full  | 75                   | 100  | 125                  | mV    |
| <b>TRANSFER CHARACTERISTICS</b>                          |       |                      |      |                      |       |
| Turn-On Delay (T <sub>D1</sub> , T <sub>D3</sub> )       | +25°C | -                    | -    | 1                    | μs    |
|  | Full  | -                    | -    | 1                    | μs    |
| Turn-On Delay Skew (T <sub>D1</sub> , T <sub>D3</sub> )  | +25°C | -                    | ±300 | -                    | ns    |
|  | Full  | -                    | ±300 | -                    | ns    |
| Turn-Off Delay (T <sub>D2</sub> , T <sub>D4</sub> )      | +25°C | -                    | -    | 1                    | μs    |
|  | Full  | -                    | -    | 1                    | μs    |
| Turn-Off Delay Skew (T <sub>D2</sub> , T <sub>D4</sub> ) | +25°C | -                    | ±100 | -                    | ns    |
|  | Full  | -                    | ±100 | -                    | ns    |
| Current Limit Sense to Output Turn-Off Delay             | +25°C | -                    | 500  | -                    | ns    |
|  | Full  | -                    | 500  | -                    | ns    |
| Current Limit Sense to Fault Output Turn-Off Delay       | +25°C | 50                   | -    | 150                  | ns    |
|  | Full  | 50                   | -    | 150                  | ns    |
| Reset Delay (T <sub>D6</sub> )                           | +25°C | -                    | 500  | -                    | ns    |
|  | Full  | -                    | 500  | -                    | ns    |
| <b>OUTPUT CHARACTERISTICS</b>                            |       |                      |      |                      |       |
| Output Rise Time   | Full  | -                    | 100  | 150                  | ns    |
| Output Fall Time   | Full  | -                    | 100  | 150                  | ns    |
| OUT1 Voltage (High)                                      | Full  | +V <sub>S</sub> -0.2 | -    | -                    | V     |
| OUT1 Voltage (Low)                                       | Full  | -                    | -    | +V <sub>S</sub> -19  | V     |
| OUT2 Voltage (High)                                      | Full  | -V <sub>S</sub> +19  | -    | -                    | V     |
| OUT2 Voltage (Low)                                       | Full  | -                    | -    | -V <sub>S</sub> +0.2 | V     |
| Fault Output (V <sub>OH</sub> )                          | Full  | 4.5                  | -    | -                    | V     |
| Fault Output (V <sub>OL</sub> )                          | Full  | -                    | -    | 0.8                  | V     |
| <b>POWER SUPPLY</b>                                      |       |                      |      |                      |       |
| I <sub>CC</sub>  | Full  | -                    | -    | 200                  | μA    |
| I <sub>EE</sub>  | Full  | -                    | -    | 200                  | μA    |
| I <sub>L</sub>   | Full  | -                    | -    | 4                    | mA    |

**Parameter Definitions** (Refer to Switching Waveforms)

| SYMBOL   | DEFINITIONS   |
|----------|---|
| $T_{D2}$ | Delay time as measured from the logic input high to low transition (1 to 0) at the 10% point, to the 10% point of the output transition for the high side switch. |
| $T_{D1}$ | Delay time as measured from the logic input low to high transition (0 to 1) at the 10% point, to the 10% point of the output transition for the high side switch. |
| $T_{D4}$ | Same as $T_{D0-1}$ for the low side switch.   |
| $T_{D3}$ | Same as $T_{D1-1}$ for the low side switch.   |
| $T_{R1}$ | Output rise time from the 10% - 90% points for the high side switch.  |
| $T_{R2}$ | Output rise time from the 10% - 90% points for the low side switch.   |
| $T_{F1}$ | Output fall time from the 10% - 90% points for the high side switch.  |
| $T_{F2}$ | Output fall time from the 10% - 90% points for the low side switch.   |
| $T_{D5}$ | Delay time as measured from the overcurrent input 10% point to the fault output high to low transition at the 10% point.  |
| $T_{D6}$ | Delay time as measured from the reset input 10% point to the fault output low to high transition at the 90% point.  |
| $T_{D7}$ | Delay time as measured from the overcurrent 1 input 10% point to output 1 low to high transition at the 90% point.  |
| $T_{D8}$ | Delay time as measured from the overcurrent 2 input 10% point to output 2 high to low transition at the 10% point.  |

**Switching Time Test Circuits**

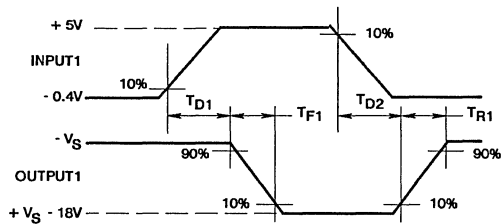
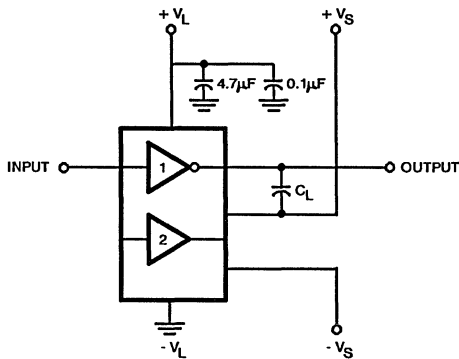


FIGURE 1. INVERTING DRIVE SWITCHING TIME (HIGH SIDE)

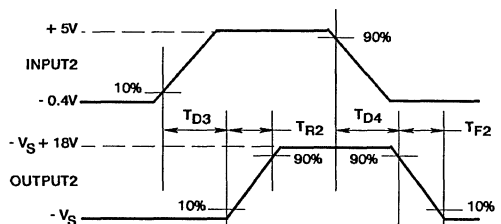
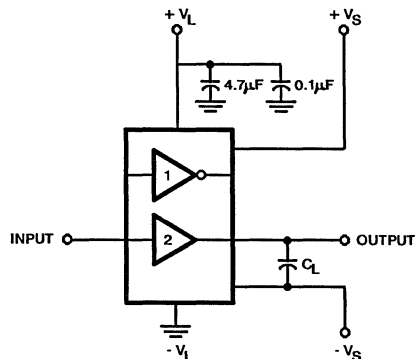
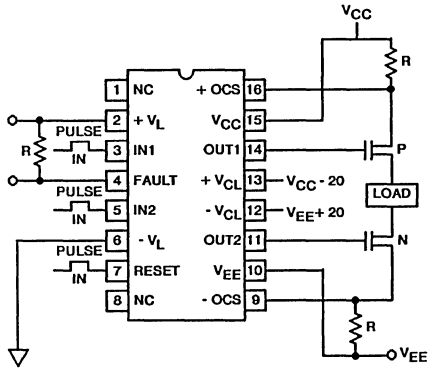


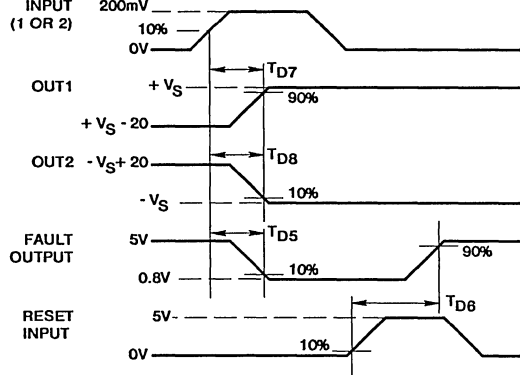
FIGURE 2. NON-INVERTING DRIVER SWITCHING TIME (LOW SIDE)

**Overcurrent Test Waveforms**

**OVERCURRENT TEST CIRCUIT**



**OVERCURRENT**





**PRELIMINARY**

May 1991

**Half Bridge  
N-Channel MOSFET Driver**
**Features**

- Unipolar Supply Operation
- Wide Supply Range ..... +40V to +450V
- Complete MOSFET Protection
- High Output to Logic Supply Isolation
- High Peak Output Current ..... 2A
- Fast Switching Times ..... 100ns
- Frequency Range ..... DC - 30kHz

**Applications**

- Switchmode Power Supplies
- PWM Servo Drives
- Stepper Motor Drives
- DC-DC Converters
- Uninterruptible Power Supplies

**Ordering Information**

| PART NUMBER | TEMPERATURE RANGE  | DESCRIPTION        |
|-------------|--|--------------------|
| HV350CP     | $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$    | 16 Pin Plastic DIP |
| HV350IP     | $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  | 16 Pin Plastic DIP |
| HV350MJ*    | $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | 16 Pin Ceramic DIP |

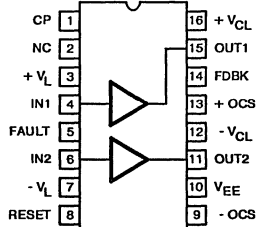
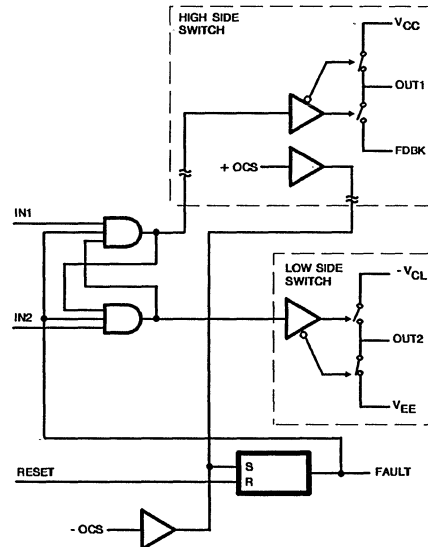
**Description**

The HV350 is a monolithic dielectrically isolated high voltage integrated circuit. The circuit provides an interface from digital signals to the gates of totem pole power MOSFETs or IGBTs. The circuit has wide supply voltage range, from 40VDC to 450VDC. In addition the logic supply can float within the high voltage rails.

The inputs are TTL compatible when the logic supply is 5V, but will operate up to 15V logic supply.

The outputs provide up to 2A current spikes to drive the gates of power MOSFETs or IGBTs. The actual voltage that the gates are driven to is set by the user, up to 20V for  $V_{GS}$ .

Also on board the chip is an overcurrent sense circuit, which independently sense overcurrent on the high side and the low side. An overcurrent condition sets a latch that disables both outputs. In order to enable the output the reset input must be toggled. An oscillator and charge pump current are integrated for high side operation.

**Pinout**
**HV350CP (16 PIN PLASTIC DIP)  
TOP VIEW**

**Functional Diagram**


## Specifications HV350

### Absolute Maximum Ratings

|   |                 |
|---|-----------------|
| Voltage Between +V <sub>S</sub> and -V <sub>S</sub> ..... | 500V            |
| Voltage Between +V <sub>I</sub> and -V <sub>I</sub> ..... | 30V             |
| Voltage Between -V <sub>S</sub> and -V <sub>I</sub> ..... | 0V              |
| Peak Output Current .....                                 | 2A              |
| Logic Input Voltage .....                                 | +V <sub>L</sub> |
| Over Current Sense to  V <sub>S</sub>   .....             | 7V              |
| Fault Output Current .....                                | 1mA             |

### Operating Temperature Range

|                                    |                                 |
|------------------------------------|---------------------------------|
| HV350CP .....                      | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| HV350IP .....                      | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| HV350MJ* .....                     | -55°C ≤ T <sub>A</sub> ≤ +125°C |
| Storage Temperature Range .....    | -65°C ≤ T <sub>A</sub> ≤ +150°C |
| Maximum Junction Temperature ..... | +175°C                          |

\* Offered at a Later Date

**Electrical Specifications** V<sub>CC</sub> = +40V, V<sub>EE</sub> = GND, C<sub>L</sub> = 10nF, V<sub>L</sub> = 5V Unless Otherwise Specified

| PARAMETER  | TEMP  | HV350CP, HV350IP    |      |     | UNITS |
|--|-------|---------------------|------|-----|-------|
|  |       | MIN                 | TYP  | MAX |       |
| <b>INPUT CHARACTERISTICS</b>                             |       |                     |      |     |       |
| Input Voltage, High (V <sub>IH</sub> )                   | Full  | 2.4                 | -    | -   | V     |
| Input Voltage, Low (V <sub>IL</sub> )                    | Full  | -                   | -    | 0.8 | V     |
| Input Current (I <sub>IH</sub> )                         | +25°C | -                   | -    | 300 | μA    |
|  | Full  | -                   | -    | 300 | μA    |
| Input Current, Low (I <sub>IL</sub> )                    | +25°C | -150                | -    | -   | μA    |
|  | Full  | -150                | -    | -   | μA    |
| Overcurrent Input Threshold                              | +25°C | 80                  | 100  | 120 | mV    |
|  | Full  | 75                  | 100  | 125 | mV    |
| <b>TRANSFER CHARACTERISTICS</b>                          |       |                     |      |     |       |
| Turn-On Delay (T <sub>D1</sub> , T <sub>D3</sub> )       | +25°C | -                   | -    | 1   | μs    |
|  | Full  | -                   | -    | 1   | μs    |
| Turn-On Delay Skew (T <sub>D1</sub> , T <sub>D3</sub> )  | +25°C | -                   | ±300 | -   | ns    |
|  | Full  | -                   | ±300 | -   | ns    |
| Turn-Off Delay (T <sub>D2</sub> , T <sub>D4</sub> )      | +25°C | -                   | -    | 1   | μs    |
|  | Full  | -                   | -    | 1   | μs    |
| Turn-Off Delay Skew (T <sub>D2</sub> , T <sub>D4</sub> ) | +25°C | -                   | ±100 | -   | ns    |
|  | Full  | -                   | ±100 | -   | ns    |
| Current Limit Sense to Output Turn-Off Delay             | +25°C | -                   | 500  | -   | ns    |
|  | Full  | -                   | 500  | -   | ns    |
| Current Limit Sense to Fault Output Turn-Off Delay       | +25°C | 50                  | -    | 150 | ns    |
|  | Full  | 50                  | -    | 150 | ns    |
| Reset Delay (T <sub>D6</sub> )                           | +25°C | -                   | 500  | -   | ns    |
|  | Full  | -                   | 500  | -   | ns    |
| <b>OUTPUT CHARACTERISTICS</b>                            |       |                     |      |     |       |
| Output Rise Time   | Full  | -                   | 100  | 150 | ns    |
| Output Fall Time   | Full  | -                   | 100  | 150 | ns    |
| OUT1 Voltage (High)                                      | Full  | +V <sub>S</sub> +19 | -    | -   | V     |
| OUT1 Voltage (Low)                                       | Full  | -                   | -    | 0.5 | V     |
| OUT2 Voltage (High)                                      | Full  | 19                  | -    | -   | V     |
| OUT2 Voltage (Low)                                       | Full  | -                   | -    | 0.5 | V     |
| Fault Output (V <sub>OH</sub> )                          | Full  | 4.5                 | -    | -   | V     |
| Fault Output (V <sub>OL</sub> )                          | Full  | -                   | -    | 0.8 | V     |
| <b>POWER SUPPLY</b>                                      |       |                     |      |     |       |
| I <sub>CC</sub>  | Full  | -                   | -    | 2   | mA    |
| I <sub>EE</sub>  | Full  | -                   | -    | 2   | mA    |
| I <sub>L</sub>   | Full  | -                   | -    | 4   | mA    |

2

POWER PROCESSING  
CIRCUITS

**Parameter Definitions** (Refer to Switching Waveforms)

| SYMBOL   | DEFINITIONS   |
|----------|---|
| $T_{D2}$ | Delay time as measured from the logic input high to low transition (1 to 0) at the 10% point, to the 10% point of the output transition for the high side switch. |
| $T_{D1}$ | Delay time as measured from the logic input low to high transition (0 to 1) at the 10% point, to the 10% point of the output transition for the high side switch. |
| $T_{D4}$ | Same as $T_{D0-1}$ for the low side switch.   |
| $T_{D3}$ | Same as $T_{D1-1}$ for the low side switch.   |
| $T_{R1}$ | Output rise time from the 10% - 90% points for the high side switch.  |
| $T_{R2}$ | Output rise time from the 10% - 90% points for the low side switch.   |
| $T_{F1}$ | Output fall time from the 10% - 90% points for the high side switch.  |
| $T_{F2}$ | Output fall time from the 10% - 90% points for the low side switch.   |
| $T_{D5}$ | Delay time as measured from the overcurrent input 10% point to the fault output high to low transition at the 10% point.  |
| $T_{D6}$ | Delay time as measured from the reset input 10% point to the fault output low to high transition at the 90% point.  |
| $T_{D7}$ | Delay time as measured from the overcurrent 1 input 10% point to output 1 low to high transition at the 90% point.  |
| $T_{D8}$ | Delay time as measured from the overcurrent 2 input 10% point to output 2 high to low transition at the 10% point.  |

**Switching Time Test Circuits**

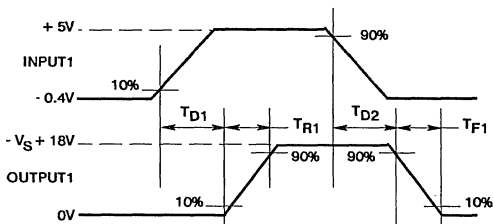
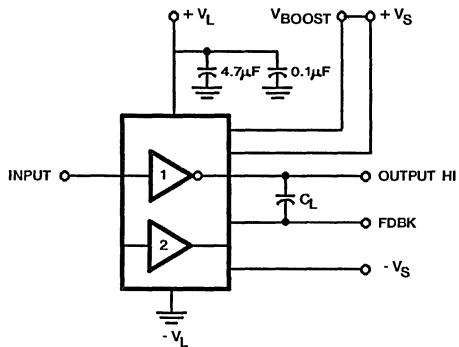


FIGURE 1. INVERTING DRIVE SWITCHING TIME (HIGH SIDE)

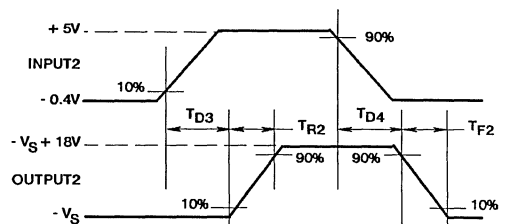
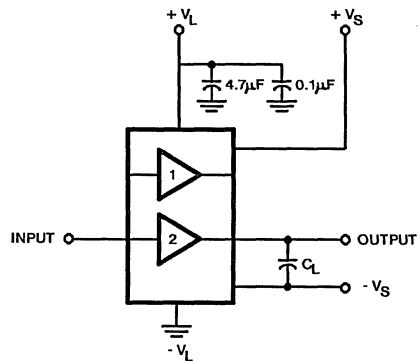
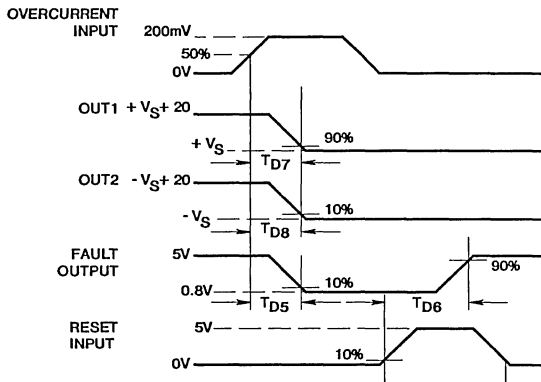
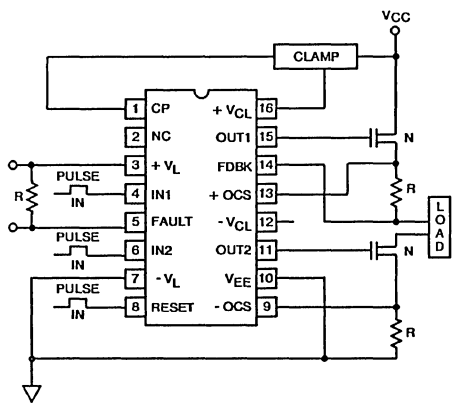


FIGURE 2. NON-INVERTING DRIVER SWITCHING TIME (LOW SIDE)

Overcurrent Test Waveforms

OVERCURRENT TEST CIRCUIT



**PRELIMINARY**

May 1991

**Half Bridge  
N-Channel MOSFET Driver**

### Features

- Unipolar Supply Operation
- Wide Supply Range ..... +40V to +450V
- Complete MOSFET Protection
- High Output to Logic Supply Isolation
- High Peak Output Current ..... 2A
- Fast Switching Times ..... 100ns
- Frequency Range ..... 10kHz to 100kHz

### Applications

- Switchmode Power Supplies
- PWM Servo Drives
- Stepper Motor Drives
- DC-DC Converters
- Uninterruptible Power Supplies

### Ordering Information

| PART NUMBER | TEMPERATURE RANGE  | DESCRIPTION        |
|-------------|--|--------------------|
| HV355CP     | $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$    | 16 Pin Plastic DIP |
| HV355IP     | $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  | 16 Pin Plastic DIP |
| HV355MJ*    | $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | 16 Pin Ceramic DIP |

### Description

The HV355 is a monolithic dielectrically isolated high voltage integrated circuit. The circuit provides an interface from digital signals to the gates of totem pole power MOSFETs or IGBTs. The circuit has wide supply voltage range, from 40VDC to 450VDC. In addition the logic supply can float within the high voltage rails.

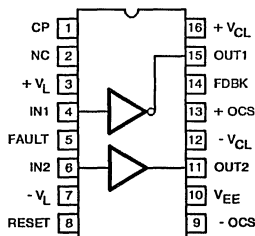
The inputs are TTL compatible when the logic supply is 5V, but will operate up to 15V logic supply.

The outputs provide up to 2A current spikes to drive the gates of power MOSFETs or IGBTs. The actual voltage that the gates are driven to is set by the user, up to 20V for  $V_{GS}$ .

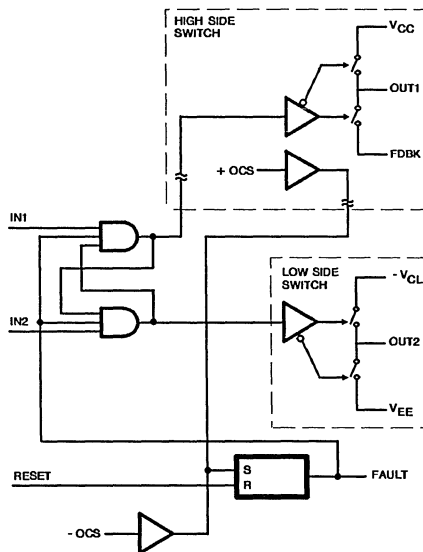
Also on board the chip is an overcurrent sense circuit, which independently sense overcurrent on the high side and the low side. An overcurrent condition sets a latch that disables both outputs. In order to enable the output the reset input must be toggled. An oscillator and charge pump current are integrated for high side operation.

### Pinout

**HV355CP (16 PIN PLASTIC DIP)  
TOP VIEW**



### Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.  
Copyright © Harris Corporation 1991 \* Offered at a later date.

## Specifications HV355

### Absolute Maximum Ratings

|   |                 |
|---|-----------------|
| Voltage Between +V <sub>S</sub> and -V <sub>S</sub> ..... | 500V            |
| Voltage Between +V <sub>I</sub> and -V <sub>I</sub> ..... | 30V             |
| Voltage Between -V <sub>S</sub> and -V <sub>I</sub> ..... | 0V              |
| Peak Output Current .....                                 | 2A              |
| Logic Input Voltage .....                                 | +V <sub>I</sub> |
| Over Current Sense to  V <sub>S</sub>   .....             | 7V              |
| Fault Output Current .....                                | 1mA             |

### Operating Temperature Range

|                                    |                                 |
|------------------------------------|---------------------------------|
| HV355CP .....                      | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| HV355IP .....                      | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| HV355MJ* .....                     | -55°C ≤ T <sub>A</sub> ≤ +125°C |
| Storage Temperature Range .....    | -65°C ≤ T <sub>A</sub> ≤ +150°C |
| Maximum Junction Temperature ..... | +175°C                          |

\* Offered at a Later Date

### Electrical Specifications V<sub>CC</sub> = +40V, V<sub>EE</sub> = GND, C<sub>L</sub> = 10nF, V<sub>L</sub> = 5V Unless Otherwise Specified

| PARAMETER  | TEMP  | HV355CP, HV355IP    |      |     | UNITS |
|--|-------|---------------------|------|-----|-------|
|  |       | MIN                 | TYP  | MAX |       |
| <b>INPUT CHARACTERISTICS</b>                             |       |                     |      |     |       |
| Input Voltage, High (V <sub>IH</sub> )                   | Full  | 2.4                 | -    | -   | V     |
| Input Voltage, Low (V <sub>IL</sub> )                    | Full  | -                   | -    | 0.8 | V     |
| Input Current (I <sub>IH</sub> )                         | +25°C | -                   | -    | 300 | μA    |
|  | Full  | -                   | -    | 300 | μA    |
| Input Current, Low (I <sub>IL</sub> )                    | +25°C | -150                | -    | -   | μA    |
|  | Full  | -150                | -    | -   | μA    |
| Overcurrent Input Threshold                              | +25°C | 80                  | 100  | 120 | mV    |
|  | Full  | 75                  | 100  | 125 | mV    |
| <b>TRANSFER CHARACTERISTICS</b>                          |       |                     |      |     |       |
| Turn-On Delay (T <sub>D1</sub> , T <sub>D3</sub> )       | +25°C | -                   | -    | 1   | μs    |
|  | Full  | -                   | -    | 1   | μs    |
| Turn-On Delay Skew (T <sub>D1</sub> , T <sub>D3</sub> )  | +25°C | -                   | ±300 | -   | ns    |
|  | Full  | -                   | ±300 | -   | ns    |
| Turn-Off Delay (T <sub>D2</sub> , T <sub>D4</sub> )      | +25°C | -                   | -    | 1   | μs    |
|  | Full  | -                   | -    | 1   | μs    |
| Turn-Off Delay Skew (T <sub>D2</sub> , T <sub>D4</sub> ) | +25°C | -                   | ±100 | -   | ns    |
|  | Full  | -                   | ±100 | -   | ns    |
| Current Limit Sense to Output Turn-Off Delay             | +25°C | -                   | 500  | -   | ns    |
|  | Full  | -                   | 500  | -   | ns    |
| Current Limit Sense to Fault Output Turn-Off Delay       | +25°C | 50                  | -    | 150 | ns    |
|  | Full  | 50                  | -    | 150 | ns    |
| Reset Delay (T <sub>D6</sub> )                           | +25°C | -                   | 500  | -   | ns    |
|  | Full  | -                   | 500  | -   | ns    |
| <b>OUTPUT CHARACTERISTICS</b>                            |       |                     |      |     |       |
| Output Rise Time   | Full  | -                   | 100  | 150 | ns    |
| Output Fall Time   | Full  | -                   | 100  | 150 | ns    |
| OUT1 Voltage (High)                                      | Full  | +V <sub>S</sub> +19 | -    | -   | V     |
| OUT1 Voltage (Low)                                       | Full  | -                   | -    | 0.5 | V     |
| OUT2 Voltage (High)                                      | Full  | 19                  | -    | -   | V     |
| OUT2 Voltage (Low)                                       | Full  | -                   | -    | 0.5 | V     |
| Fault Output (V <sub>OH</sub> )                          | Full  | 4.5                 | -    | -   | V     |
| Fault Output (V <sub>OL</sub> )                          | Full  | -                   | -    | 0.8 | V     |
| <b>POWER SUPPLY</b>                                      |       |                     |      |     |       |
| I <sub>CC</sub>  | Full  | -                   | -    | 200 | μA    |
| I <sub>EE</sub>  | Full  | -                   | -    | 200 | μA    |
| I <sub>L</sub>   | Full  | -                   | -    | 4   | mA    |

**Parameter Definitions** (Refer to Switching Waveforms)

| SYMBOL   | DEFINITIONS   |
|----------|---|
| $T_{D2}$ | Delay time as measured from the logic input high to low transition (1 to 0) at the 10% point, to the 10% point of the output transition for the high side switch. |
| $T_{D1}$ | Delay time as measured from the logic input low to high transition (0 to 1) at the 10% point, to the 10% point of the output transition for the high side switch. |
| $T_{D4}$ | Same as $T_{D0-1}$ for the low side switch.   |
| $T_{D3}$ | Same as $T_{D1-1}$ for the low side switch.   |
| $T_{R1}$ | Output rise time from the 10% - 90% points for the high side switch.  |
| $T_{R2}$ | Output rise time from the 10% - 90% points for the low side switch.   |
| $T_{F1}$ | Output fall time from the 10% - 90% points for the high side switch.  |
| $T_{F2}$ | Output fall time from the 10% - 90% points for the low side switch.   |
| $T_{D5}$ | Delay time as measured from the overcurrent input 10% point to the fault output high to low transition at the 10% point.  |
| $T_{D6}$ | Delay time as measured from the reset input 10% point to the fault output low to high transition at the 90% point.  |
| $T_{D7}$ | Delay time as measured from the overcurrent 1 input 10% point to output 1 low to high transition at the 90% point.  |
| $T_{D8}$ | Delay time as measured from the overcurrent 2 input 10% point to output 2 high to low transition at the 10% point.  |

**Switching Time Test Circuits**

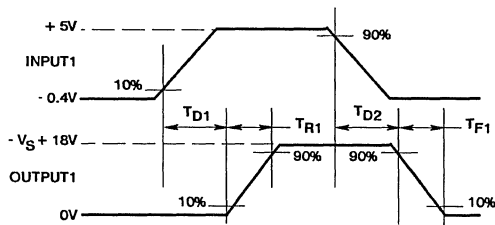
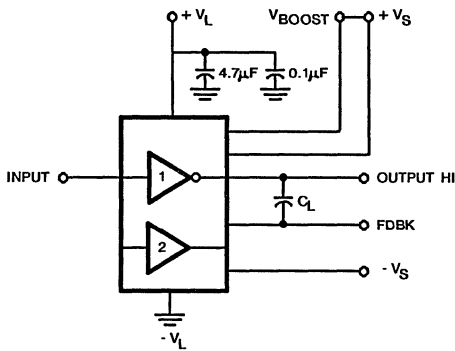


FIGURE 1. INVERTING DRIVE SWITCHING TIME (HIGH SIDE)

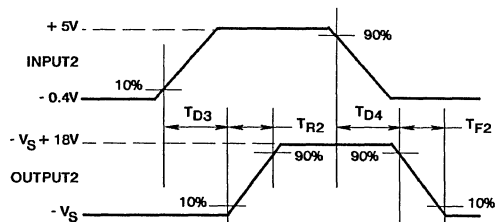
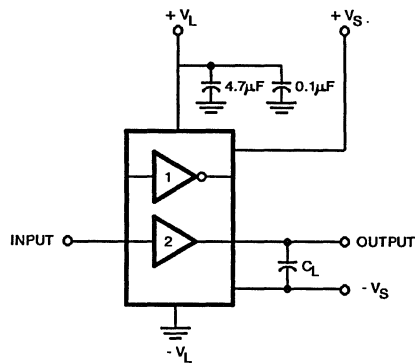
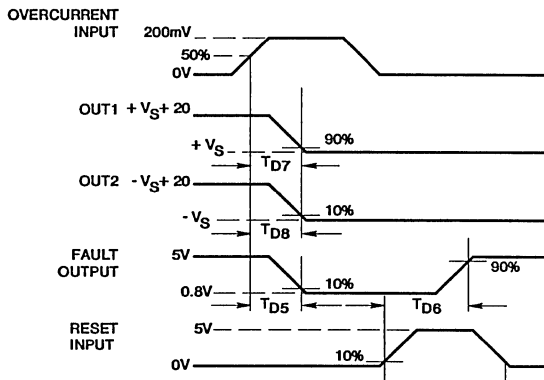
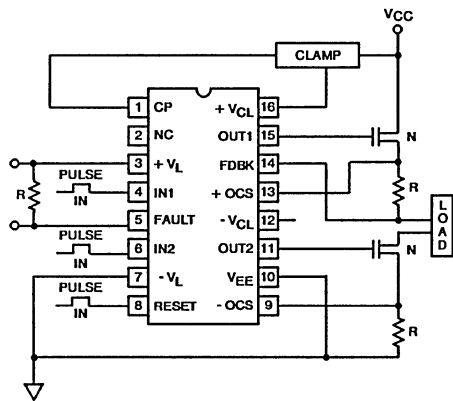


FIGURE 2. NON-INVERTING DRIVER SWITCHING TIME (LOW SIDE)

Overcurrent Test Waveforms

OVERCURRENT TEST CIRCUIT





## PRELIMINARY

May 1991

## High Speed MOSFET Driver

### Features

- Fast Fall Times ..... 22ns (10,000pF)
- No Supply Current in Quiescent State
- Peak Output Source Current ..... 6A
- Peak Output Sink Current ..... 30A
- High Frequency Capability ..... 300kHz

### Applications

- Switching Power Supplies
- DC/DC Converters
- Motor Controllers
- Uninterruptible Power Supplies

### Ordering Information

| PART NUMBER | TEMPERATURE RANGE | PACKAGE                |
|-------------|-------------------|------------------------|
| HV400CP     | 0°C to +75°C      | 8 Pin Plastic Mini-DIP |
| HV400CB     | 0°C to +75°C      | 8 Pin Plastic SOIC     |
| HV400IP     | -40°C to +85°C    | 8 Pin Plastic Mini-DIP |
| HV400IB     | -40°C to +85°C    | 8 Pin Plastic SOIC     |

### Description

The HV400 is a single monolithic, non-inverting high speed driver designed to drive large capacitive loads at high slew rates. The device is optimized for capacitive loads in the 5,000pF to 100,000pF range. It features an output stage capable of sourcing up to 6A through the high-side NPN switch and sinking up to 30A through the low-side SCR switch. Rise and fall times of 70ns and 30ns respectively are achieved driving a 20,000pF load. The output high and low side switches are pinned out separately allowing independent control of power MOSFET gate rise and fall times.

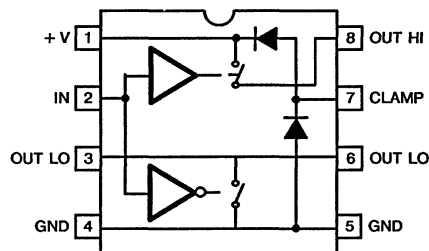
Special features are included in the device to provide a simple, high speed gate drive circuit for power MOSFET in application using pulse transformers. An optional on-chip diode works with an external storage capacitor to store energy from the pulse transformer after the gate drive pulse has completed its low to high transition. The storage capacitor supplies the gate drive current to turn on the MOSFET which overcomes the di/dt limitations of the pulse transformer. The high current drive capability of the HV400 using the floating supply provides a cost effective improvement over existing methods.

Another feature of the HV400 is the absence of quiescent current. When used with PWM control ICs, additional low voltage supply current to power the MOSFET driver during startup, is not needed.

The device is fabricated in the High Frequency Bipolar DI process which provides latchproof operation in the presence of transients on the power and signal lines. It is available in the 8 pin Plastic DIP and 8 pin SOIC (Commercial and Industrial grades).

### Pinout

HV400CP (PLASTIC DIP)  
HV400CB (SOIC)  
TOP VIEW



## Specifications HV400

### Absolute Maximum Ratings

|   |                  |
|---|------------------|
| Voltage Between V+ and GND Terminals .....        | 30V              |
| Input Voltage (Max) .....                         | +V + 1V          |
| Input Voltage (Min) .....                         | GND -1V          |
| Max Clamp Current (Pin 7) .....                   | TBD              |
| Peak Output Source Current .....                  | 6A               |
| Peak Output Sink Current .....                    | 30A              |
| Power Dissipation at T <sub>A</sub> = +25°C ..... | 1.2W Mini-DIP    |
| Derate Above 65°C .....                           | 15mW/°C Mini-DIP |

### Operating Temperature Range

|                                 |                                 |
|---------------------------------|---------------------------------|
| HV400CP/CB .....                | 0°C ≤ T <sub>A</sub> ≤ +70°C    |
| HV400IP/IB .....                | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| Storage Temperature Range ..... | -65°C ≤ T <sub>A</sub> ≤ +150°C |

### Electrical Specifications (Static) Test Conditions: +V = +20V at +25°C

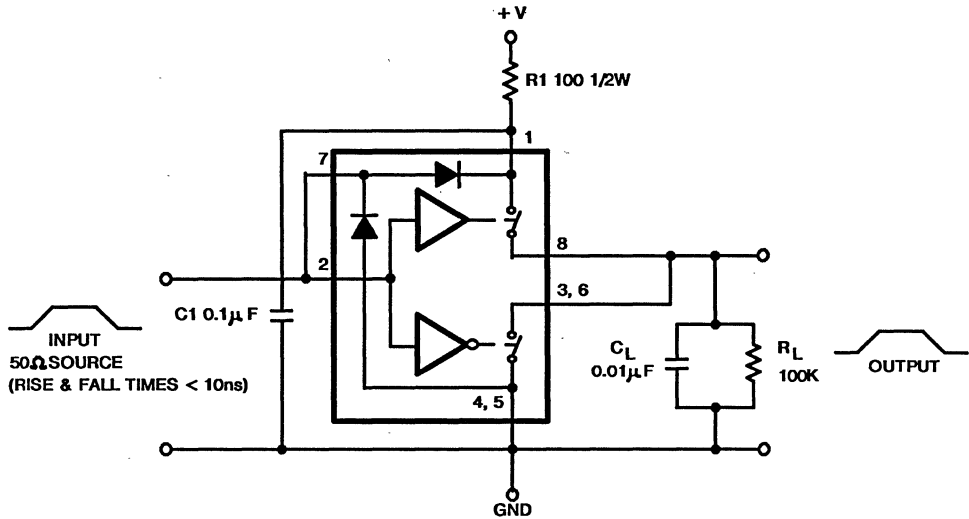
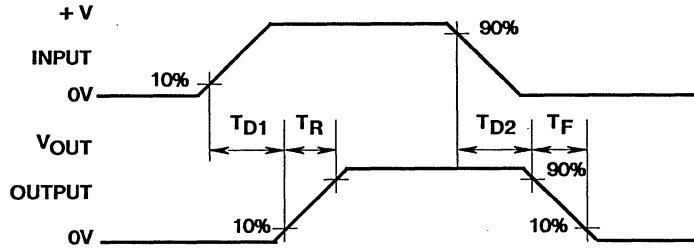
| SYMBOL          | PARAMETER                   | TEST CONDITIONS                                    | MINIMUM REQUIREMENT |      |      | UNITS |
|-----------------|-----------------------------|--|---------------------|------|------|-------|
|                 |                             |  | MIN                 | TYP  | MAX  |       |
| V <sub>IH</sub> | Input Voltage, High         | V <sub>OUT</sub> = 0V, I <sub>OUT HI</sub> = 1mA   | 1.5                 | 1.9  | 2.3  | V     |
| V <sub>IL</sub> | Input Voltage, Low          | V <sub>OUT</sub> = 18V, I <sub>OUT LO</sub> = -3mA | 16.8                | 17.1 | 17.3 | V     |
| I <sub>IH</sub> | Input Current, High (Pin 2) | V <sub>IN</sub> = +20V, I <sub>OUT HI</sub> = 0mA  | 11                  | 14.2 | 17   | mA    |
|                 |                             | I <sub>OUT HI</sub> = 150mA                        | 11.25               | 14.7 | 18   | mA    |
| I <sub>IL</sub> | Input Current, Low (Pin 2)  | V <sub>IN</sub> = 0V                               | 0                   | 0.7  | 1.0  | μA    |
| V <sub>OH</sub> | Output Voltage, High        | V <sub>IN</sub> = +V, I <sub>OUT</sub> = 150mA     | 16.7                | 16.9 | 17.1 | V     |
| V <sub>OL</sub> | Output Voltage, Low         | V <sub>IN</sub> = 0V, I <sub>OUT</sub> = -150mA    | 0.8                 | 0.88 | 1.0  | V     |
| V <sub>F</sub>  | Clamp Diode Forward Voltage | I <sub>D</sub> = 100mA                             | 0.9                 | 1.02 | 1.1  | V     |
| I <sub>R</sub>  | Reverse Leakage Current     | V <sub>R</sub> = 20V                               | -                   | 0.1  | 1.0  | μA    |
| I <sub>OL</sub> | Off Leakage Current (Pin 8) | V <sub>OUT</sub> = 0V, V <sub>IN</sub> = 0V        | 0                   | 10   | 50   | μA    |

### Electrical Specifications (Dynamic) Test Conditions: +V = 20V, C<sub>L</sub> = 10nF

| SYMBOL          | PARAMETER                  | TEST CONDITIONS | MINIMUM REQUIREMENT |      |      | UNITS |
|-----------------|----------------------------|-----------------|---------------------|------|------|-------|
|                 |                            |                 | MIN                 | TYP  | MAX  |       |
| T <sub>D1</sub> | Delay, Input to Output     | Figure 1        | -                   | 10   | -    | ns    |
| T <sub>D2</sub> | Delay, Input to Output     | Figure 1        | -                   | 10   | -    | ns    |
| T <sub>R</sub>  | Output Rise Time           | Figure 1        | -                   | 66   | -    | ns    |
| T <sub>F</sub>  | Output Fall Time           | Figure 1        | -                   | 22   | -    | ns    |
| T <sub>OR</sub> | Output, Recovery Time      | Figure 1        | -                   | 1000 | 1200 | ns    |
| T <sub>RR</sub> | Clamp Diode, Recovery Time |                 | -                   | TBD  | -    | ns    |

# HV400

## Timing Diagram



NOTE: Wiring Inductance Reduced to Absolute Minimum  
 FIGURE 1. HV400 TEST CIRCUIT

## Application Circuit

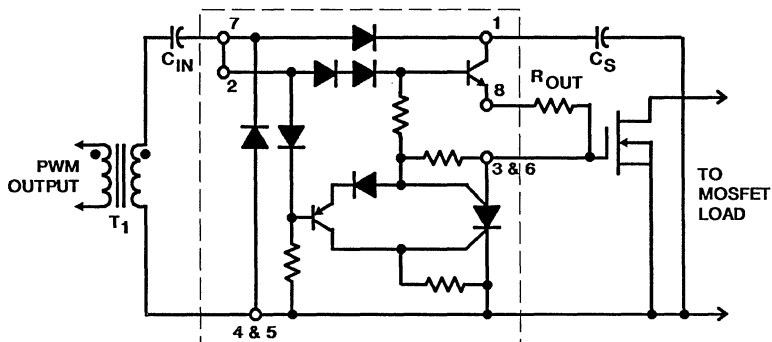


FIGURE 2. PRIMARY APPLICATION FOR HV400 IS WITH A PUSH-PULL DRIVEN PULSE TRANSFORMER

## UL RECOGNIZED

August 1991

## Single Chip Power Supply

### Features

- Direct AC to DC Conversion
- Wide Input Voltage Range ..... 18Vrms-132Vrms
- Multiple Output Voltages
- Guaranteed Output Current ..... 50mA
- Output Voltage ..... 5V to 24V
- Line and Load Regulation ..... <2%
- UL Recognition, File # E130808

### Applications

- Compact, Low Cost, Power Supply for Non-Isolated Applications
- Appliance Control
- Battery Back-Up Systems
- Dual Output Supply for OFF-LINE Motor Controls

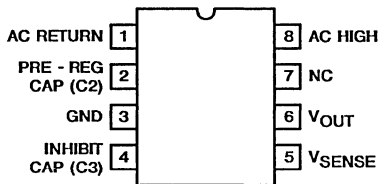
### Description

The HV-1205 is a single chip power supply that can supply 5V to 24V at 50mA output current. Just a few inexpensive external components are needed to provide a compact, light weight, cost effective power supply. The HV-1205 replaces a transformer, rectifier, and voltage regulator. This chip is made in the new Harris High Voltage Dielectric Isolation Process. This high breakdown process (400V) allows a patented switching circuit to draw current from the AC line only as necessary to supply the load. The HV-1205 operates from -40°C to +85°C (with no derating necessary due to package power dissipation). The HV-1205 is available in an 8 Pin Plastic Mini-DIP.

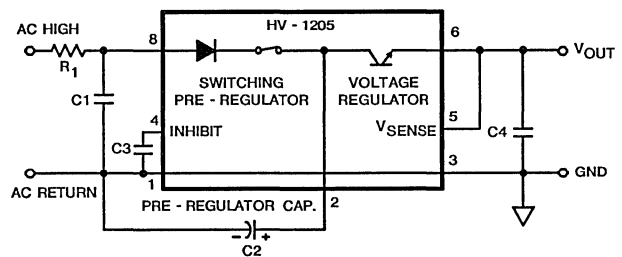
**CAUTION: This Product Does Not Provide Isolation From the AC Line**

### Pinout

HV3-1205 (PLASTIC MINI-DIP)  
TOP VIEW



### Functional Diagram



## Specifications HV-1205

### Absolute Maximum Ratings

|  |                         |
|--|-------------------------|
| Voltage Between Pin 1 and 8, Continuous Vrms | 132Vrms                 |
| Voltage Between Pin 1 and 8, Peak            | 400V                    |
| Voltage Between Pin 2 and 6                  | 15V                     |
| Input Current, Peak                          | 1.1A                    |
| Output Current                               | Short Circuit Protected |
| Output Voltage                               | 30V                     |
| Maximum Junction Temperature                 | +150°C                  |

### Operating Temperature Range

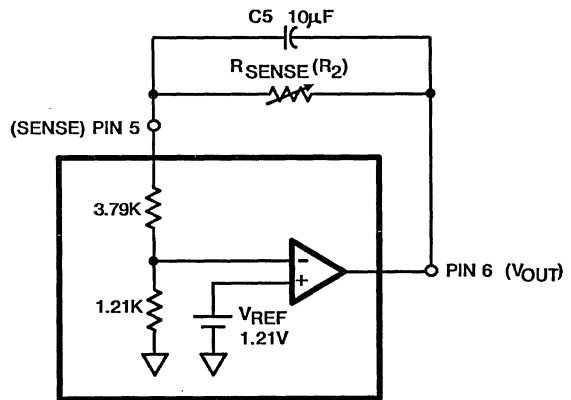
|                           |                             |
|---------------------------|-----------------------------|
| HV3-1205-9                | -40°C to +85°C              |
| HV3-1205-5                | 0°C to +75°C                |
| Storage Temperature Range | -65°C to +175°C             |
| Thermal Constants (°C/W)  | $\theta_{ja}$ $\theta_{jc}$ |
| Plastic DIP               | 82            16            |

**Electrical Specifications** Unless Otherwise Specified:  $V_{IN} = 120V_{rms}$  at 60Hz,  $C_1 = 0.05\mu F$ ,  $C_2 = 470\mu F$ ,  $C_3 = 150pF$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 50mA$ , Source Impedance,  $R_1 = 150\Omega$ . Parameters are Guaranteed at the Specific  $V_{IN}$  and Frequency Conditions, Unless Otherwise Specified. See Functional Diagrams for Component Location.

| PARAMETER  | $V_{IN}$   | TEMP  | HV-1205-9<br>-40°C to +85°C |      |      | HV-1205-5<br>0°C to +75°C |      |      | UNITS |
|--|--|-------|-----------------------------|------|------|---------------------------|------|------|-------|
|  |  |       | MIN                         | TYP  | MAX  | MIN                       | TYP  | MAX  |       |
| Output Voltage<br>(At Preset 5V)                               | 120V   | +25°C | 4.75                        | 5.0  | 5.25 | 4.75                      | 5.0  | 5.25 | V     |
|  | 120V   | Full  | 4.65                        | 5.0  | 5.35 | 4.65                      | 5.0  | 5.35 | V     |
| Output Voltage TC  | 120V   | Full  | -                           | 0.02 | -    | -                         | 0.02 | -    | %/°C  |
| Output Ripple ( $V_{p-p}$ )<br>( $C_4 = 1\mu F$ , $f = 60Hz$ ) | 120V   | +25°C | -                           | 10   | -    | -                         | 10   | -    | mV    |
|  | 120V   | Full  | -                           | 20   | -    | -                         | 20   | -    | mV    |
| Line Regulation  | 80Vrms to<br>132Vrms                               | +25°C | -                           | -    | 15   | -                         | -    | 20   | mV    |
|  |  | Full  | -                           | -    | 30   | -                         | -    | 40   | mV    |
| Load Regulation<br>( $I_{OUT} = 5mA$ to $50mA$ )               | 120V   | +25°C | -                           | -    | 15   | -                         | -    | 20   | mV    |
|  | 120V   | Full  | -                           | -    | 30   | -                         | -    | 40   | mV    |
| Output Current   | 120V   | Full  | 0                           | -    | 50   | 0                         | -    | 50   | mA    |
| Short Circuit Current Limit                                    | 120V   | Full  | 55                          | 95   | -    | 55                        | 95   | -    | mA    |
| Drop-Out Voltage   | Pin 2 - Pin 6                                      | +25°C | -                           | 2.2  | -    | -                         | 2.2  | -    | V     |
| Quiescent Current<br>Post Regulator                            | 11V <sub>DC</sub> to 30V <sub>DC</sub><br>On Pin 2 | +25°C | -                           | 2    | -    | -                         | 2    | -    | mA    |

### Equivalent Circuit For Output Voltage Adjustment

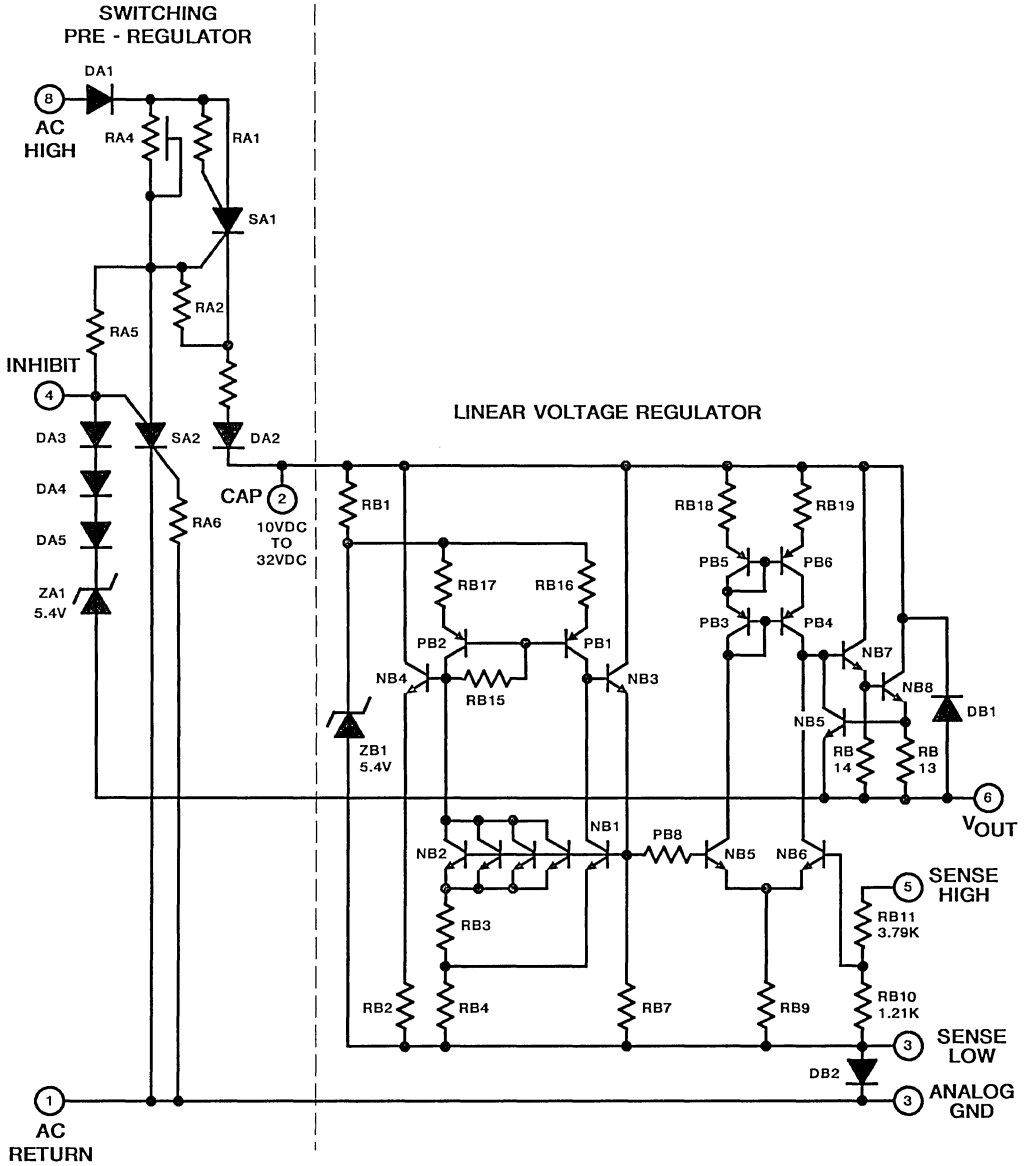
$R_2 = V_{OUT} - 5V$  Where  $R_2$  is the Approximate Value of Resistor Between Pin 5 and Pin 6 (in  $K\Omega$ ).  $V_{OUT}$  is the Desired Output Voltage. See Graph.



$R_{SENSE}$  IS ZERO OHMS FOR 5V<sub>OUT</sub>

FIGURE 1.

Schematic



## Application Information

### How The HV-1205 Works

The HV-1205 converts AC voltage into regulated DC voltage to power low voltage components such as integrated circuits. This is accomplished in two stages on the monolithic chip. First, the pre-regulator momentarily connects a large capacitor to the AC high line until it charges to about 6V above the selected output voltage. The pre-regulator then switches to a blocking mode and stays in that blocking mode until the next line cycle begins. The large capacitor supplies power to the series pass regulator, providing DC current to power the user's circuit. Providing current to the post regulator causes the large cap to discharge at a rate dependent on load current. Each line cycle refreshes the charge on the electrolytic capacitor. For a detailed explanation of HV-1205 operation see Application Note 558.

### Input Voltage

The HV-1205 operates over a wide range of input voltages. Most applications will use the 120Vrms line from the power grid. A standard circuit for this application is shown in Figure 2. Much smaller input voltages can be used. The size of the external components used will be determined by the output voltage and current required and the input voltage available. Several graphs have been provided to help choose component values for a specific application. The section below called Component Selection discusses trade-offs related to component sizing.

### Input Frequency

The HV-1205 is designed to operate from 48Hz to 380Hz. Higher operating frequency is possible. Keep in mind that the HV-1205 will refresh C2 once per line cycle.

### Setting Output Voltage

The HV-1205 can be set to provide a regulated output voltage anywhere from 5V to 24V<sub>DC</sub>. Refer to Figures 4, 5 and 6 for several ways of adjusting output voltage. Any time an output voltage greater than 5V is chosen, a 10 $\mu$ F capacitor between the output and the sense pin is required. That capacitor allows C2 to charge gradually.

As seen in Figure 1, output voltage is set by feedback to the sense pin. The output will rise to the voltage necessary to keep the sense pin at 5V. For a 5V output, pins 5 and 6 are shorted together. There are three ways to increase the output voltage beyond 5V. The simplest method is to increase the feedback resistor by adding an external resistor between pins 5 and 6. The disadvantage is that the internal circuit resistors have a tolerance of approximately  $\pm 15\%$  which limits the accuracy of the predicted output (see graph). The internal thin film resistors have low temperature coefficients.

An external voltage divider as shown in Figure 5 improves the accuracy as long as the external resistors are much lower in value than those of the internal divider. Approximately 1mA flows into pin 5. If a potentiometer is used as the divider, an additional resistor between the lower leg and ground will insure that the output never exceeds its maximum rated voltage.

A zener diode between pins 5 and 6, as shown in Figure 6, sets the output voltage above 5V by the zener's breakdown voltage at 1mA. This voltage has the accuracy and tolerance of the zener. An added advantage is that two outputs are now available, pin 5 at 5V and pin 6 at  $V_Z + 5V$ . All the current from the 5V supply flows through the reference diode. The sum of both output currents should not exceed 50mA.

### Output Current

Any current draw up to 50mA continuous is acceptable. More current can be drawn momentarily. Care should be taken to make sure C2 is not discharged below the dropout voltage and that the duty cycle of the excess current is low enough to not cause a package power dissipation problem. The output is current limited as shown in the graph to protect against shorted loads.

### Component Selection

One of the most powerful features of the HV-1205 is its flexibility. One standard configuration allows enormous variation in input voltage and output current while still maintaining a regulated output. For example, with  $R_1 = 150\Omega$ ,  $C_2 = 470\mu F$  and  $V_{OUT} = 5V$ , the HV-1205 will provide a regulated 50mA output when input voltage is anywhere from 132V<sub>AC</sub> down to about 28V<sub>AC</sub>. The designer can choose components tailored to his application in order to save cost, space, power dissipation etc.

Below is a list of external components, description of their purpose, and a recommended value. This is a full list of possible components all of which may not be required for an intended application. Most designs will use a subset of this list.

- F1: Fuse. Opens the connections to the power line should chip fail. Recommended value = 1/4A, 2AG similar to Littlefuse 225.250 $\oplus$ .
- R<sub>1</sub>: Source Resistance. Limits current into HV-1205. Needs to be large enough to limit inrush current when C2 is discharged fully.  $V_{PEAK}/R_1 = 1.1A$  Maximum. R<sub>1</sub> will dissipate power as shown in the graphs. The equation for Pd in R<sub>1</sub> is:  
 $P_d = 1.33 \sqrt{\pi R_1} V_{PEAK}(I_{OUT})^3$ . Low average output currents would allow for source resistors with lower Pd ratings. Similarly, lower V<sub>AC</sub> or smaller value R<sub>1</sub> will cause less dissipation in R<sub>1</sub>. Sizing of R<sub>1</sub> should be tailored to the intended application keeping in mind not to let the maximum inrush current be exceeded. Should an external method of limiting inrush current be used (such as NTC resistors) then the value of R<sub>1</sub> and its associated heat could be reduced. Recommended value = 150 $\Omega$ . To reduce Pd see App. Note AN9107.
- C1: Snubber Capacitor. R<sub>1</sub> and C1 form a low pass filter thereby limiting the rate of voltage rise at the input of the HV-1205. Recommended value = 0.05 $\mu$ F, AC rated.
- MOV: Surge suppressor. Metal Oxide Varistor clamps voltage to a level that the HV-1205 can handle. Recommended value = V130LA20 or equivalent.

**Application Information (Continued)**

- C2: Pre-Regulator capacitor. This capacitor is charged once each line cycle. The post-regulator portion of HV-1205 is powered by C2 for most of the line cycle. Normally the smallest C2 that will supply the load current (see graph) is used. Using a large C2 will supply temporary high load currents or normal load current during a short power loss. Using a larger C2 will reduce ripple at Pin 2, the input to the post regulator, which will reduce output ripple. C2 should have a ripple current rating consistent with the application. Small capacitors with high ESR may not store enough charge to maintain load current. See graph. Recommended value = 470µF, voltage rating should be about 10V greater than chosen V<sub>OUT</sub>.
- C3: Inhibit capacitor. Keeps the HV-1205 from turning on during input transients. If sized too large,

HV-1205 will never turn on. If sized too small, no protection from transients is offered. For 60Hz (or 50Hz) use the recommended value of 150pF, voltage rating should be at about 10V greater than V<sub>OUT</sub>. For 400Hz use 47pF.

- C4: Output filter capacitor. At least 1µF is required to maintain stability of the output stage. Larger values will not reduce ripple but will reduce spiking which may occur on the output coincident with the HV-1205 going into blocking mode. 100µF reduces the spike amplitude to about 25mVp-p.
- R2: Feedback component. A resistor or diode that causes a voltage drop between the SENSE and OUTPUT pins and thereby adjusting the output voltage. See voltage adjustment equivalent circuit. Also see graph for approximate resistor value.

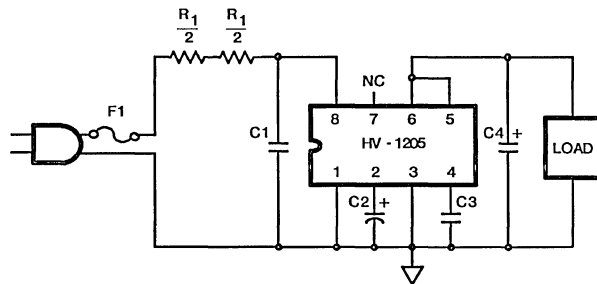


FIGURE 2. HV-1205 STANDARD +5V APPLICATION

**V<sub>OUT</sub> ADJUSTMENT**

| FIGURE 4 METHOD | FIGURE 5 METHOD | FIGURE 6 METHOD                |                |                  |                |
|-----------------|-----------------|--------------------------------|----------------|------------------|----------------|
| R <sub>2</sub>  | V <sub>O</sub>  | R <sub>A</sub> /R <sub>B</sub> | V <sub>O</sub> | V <sub>Z</sub> * | V <sub>O</sub> |
| 0               | 5V              | 0/00                           | 5V             | -                | 5V             |
| 1K              | 6V              | 160/1K                         | 6V             | 1V               | 6V             |
| 3K              | 8V              | 510/1K                         | 8V             | 3V               | 8V             |
| 5K              | 10V             | 820/1K                         | 10V            | 5V               | 10V            |
| 7K              | 12V             | 1.2K/1K                        | 12.2V          | 7V               | 12V            |
| 9K              | 14V             | 1.5K/1K                        | 14V            | 9V               | 14V            |
| 11K             | 16V             | 1.8K/1K                        | 15.8V          | 11V              | 16V            |
| 13K             | 18V             | 2.2K/1K                        | 18.2V          | 13V              | 18V            |
| 15K             | 20V             | 2.4K/1K                        | 19.4V          | 15V              | 20V            |
| 17K             | 22V             | 3.0K/1K                        | 23V            | 17V              | 22V            |
| 19K             | 24V             | 3.17K/1K                       | 24V            | 19V              | 24V            |

\*V<sub>Z</sub> @ 1mA

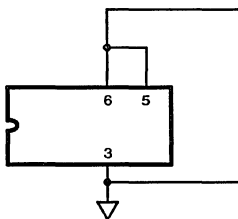


FIGURE 3. V<sub>OUT</sub> = +5V

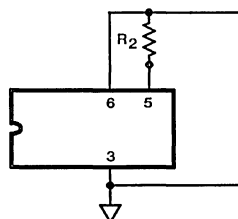


FIGURE 4. V<sub>OUT</sub> > +5V

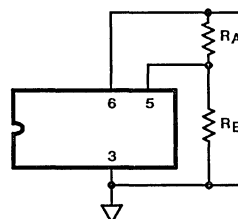


FIGURE 5. V<sub>OUT</sub> > +5V

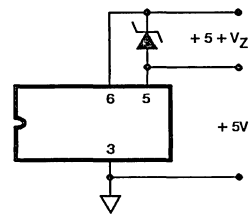
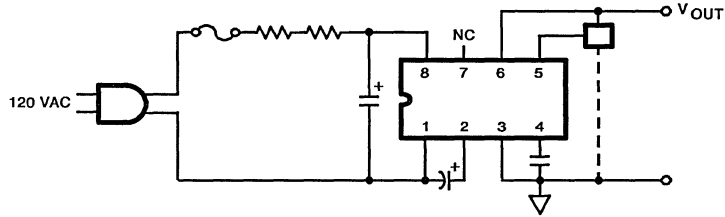


FIGURE 6. V<sub>OUT</sub> = +5V, +5 +V<sub>Z</sub>

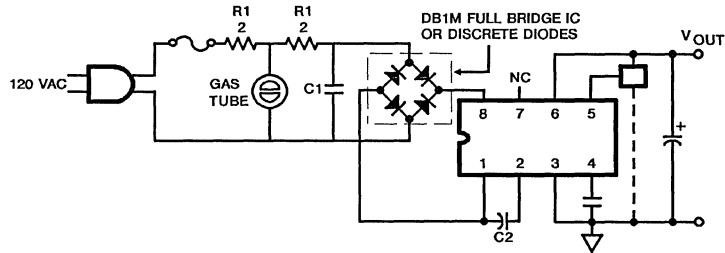


Application Information (Continued)

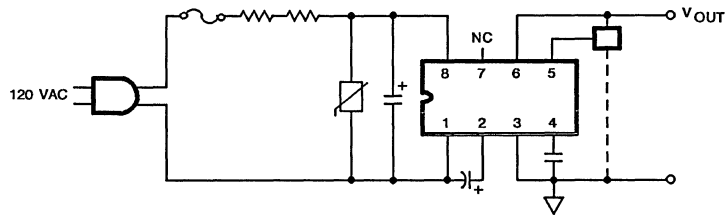
OPERATION WITH  $V_{OUT} > 5V$



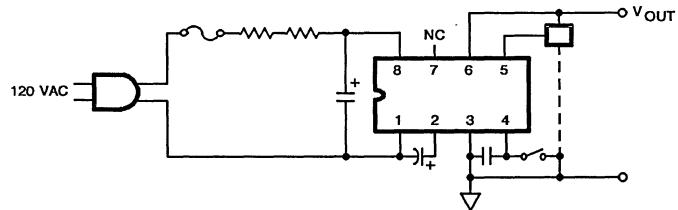
OPERATION FROM A BRIDGE RECTIFIER



SURGE PROTECTION USING MOV



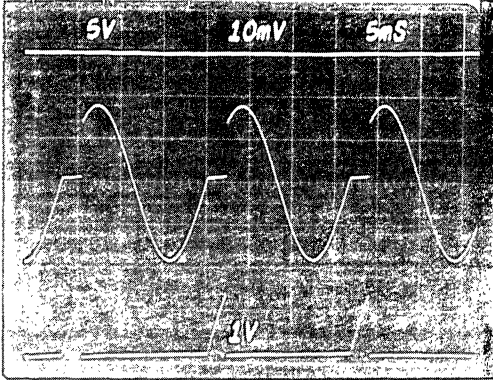
USING SWITCH TO TURN OFF OUTPUT



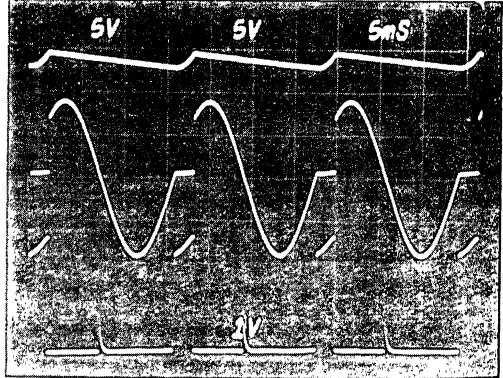
# HV-1205

**HV-1205 Waveforms** Unless Otherwise Specified:  $T_A = +25^\circ\text{C}$ ,  $V_{AC} = 120\text{Vrms}$ ,  $f = 60\text{Hz}$ ,  
 $R_1 = 150\Omega$ ,  $C_1 = 0.05\mu\text{F}$ ,  $C_2 = 470\mu\text{F}$ ,  $C_3 = 150\text{pF}$ ,  $C_4 = 1\mu\text{F}$ ,  $V_{OUT} = 5\text{V}$

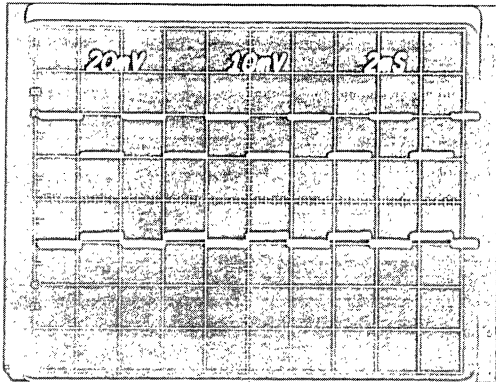
Top Trace: Regulated  $5V_{OUT}$   
 Middle Trace: Input Voltage at Pin 8, AC HIGH (100V/Div)  
 Bottom Trace: Current into Pin 8, (0.5A/Div)



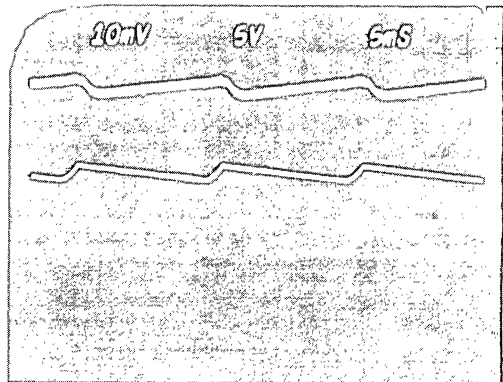
Top Trace: Pre-Regulator Capacitor Voltage,  $C_2$  (5V/Div) @ Approximately 11VDC  
 Middle Trace: Input Voltage at Pin 8, AC HIGH (100V/Div)  
 Bottom Trace: Inhibit Capacitor Voltage (5V/Div)



Top Trace: Load Current Step (50mA/Div)  
 Bottom Trace: Output Voltage (20mV/Div) @ 5VDC



Top Trace: Ripple on Regulated 5V Out with 50mA Out (10mV/Div)  
 Bottom Trace: Ripple on  $C_2$ , Input to Linear Regulator.  $C_2 = 470\mu\text{F}$  (5V/Div)



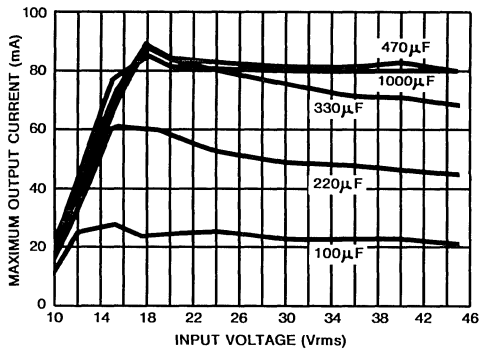
2  
 POWER PROCESSING  
 CIRCUITS

# HV-1205

**Typical Performance Curves** Unless Otherwise Specified:  $T_A = +25^\circ\text{C}$ ,  $V_{AC} = 120\text{Vrms}$ ,  $f = 60\text{Hz}$ ,  $R_1 = 150\Omega$ ,  $C_1 = 0.05\mu\text{F}$ ,  $C_2 = 470\mu\text{F}$ ,  $C_3 = 150\text{pF}$ ,  $C_4 = 1\mu\text{F}$ ,  $V_{OUT} = 5\text{V}$

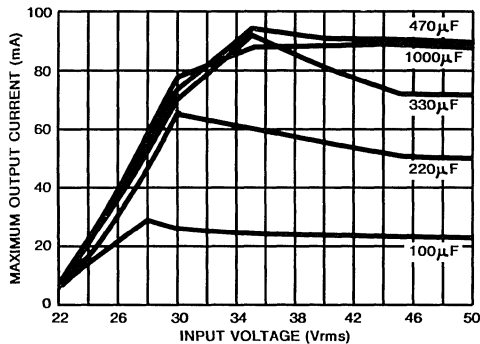
**MAXIMUM OUTPUT CURRENT FOR 5V REGULATED OUTPUT vs. INPUT VOLTAGE AND PRE-REGULATOR CAPACITOR SIZE (C2)**

$R_1 = 24\Omega$

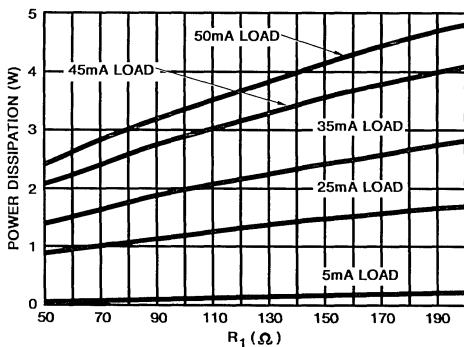


**MAXIMUM OUTPUT CURRENT FOR 24V REGULATED OUTPUT vs. INPUT VOLTAGE AND PRE-REGULATOR CAPACITOR SIZE (C2)**

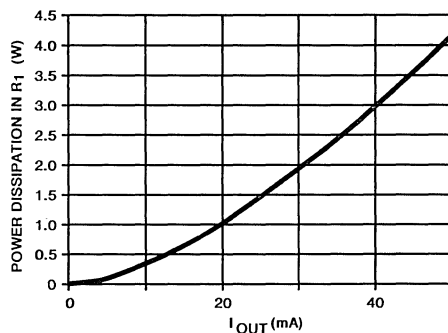
$R_1 = 24\Omega$



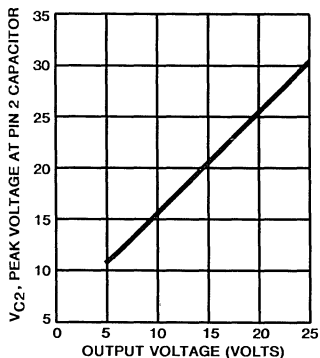
**Pd IN R1 vs. R1 VALUE**  
 $V_{rms} = 120\text{V}$



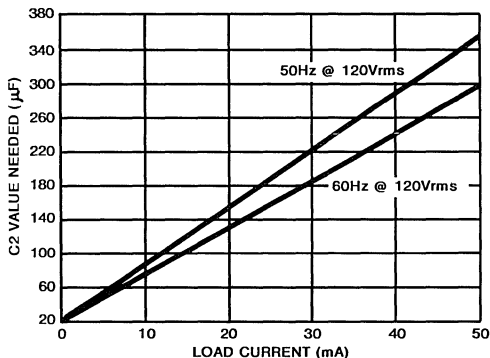
**Pd IN R1 vs. IOUT**  
 $120\text{Vrms}$ ,  $R_1 = 150\Omega$



**PEAK C2 VOLTAGE vs. OUTPUT VOLTAGE**



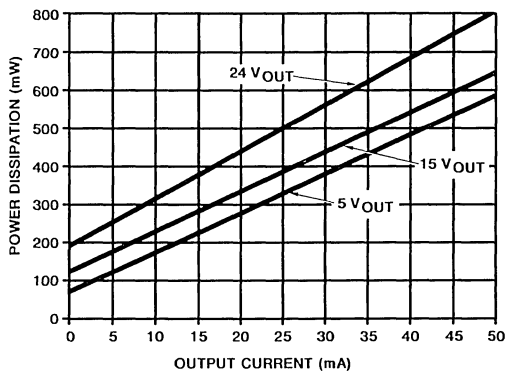
**MINIMUM C2 VALUE vs. LOAD CURRENT**



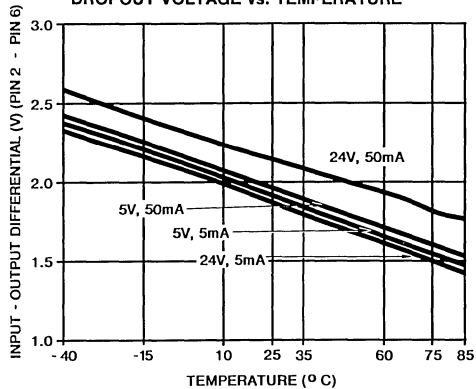
# HV-1205

**Typical Performance Curves** Unless Otherwise Specified:  $T_A = +25^\circ\text{C}$ ,  $V_{AC} = 120\text{Vrms}$ ,  $f = 60\text{Hz}$ ,  
 $R_1 = 150\Omega$ ,  $C_1 = 0.05\mu\text{F}$ ,  $C_2 = 470\mu\text{F}$ ,  $C_3 = 150\text{pF}$ ,  $C_4 = 1\mu\text{F}$ ,  $V_{OUT} = 5\text{V}$

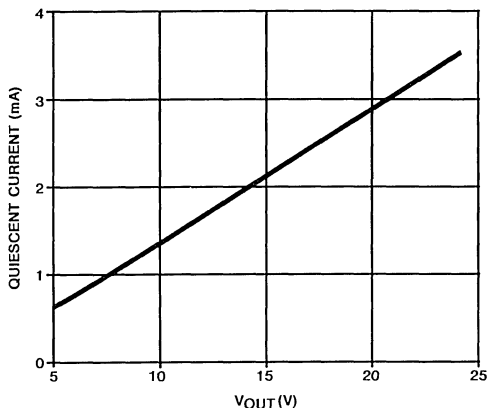
**CHIP POWER DISSIPATION vs. OUTPUT CURRENT**



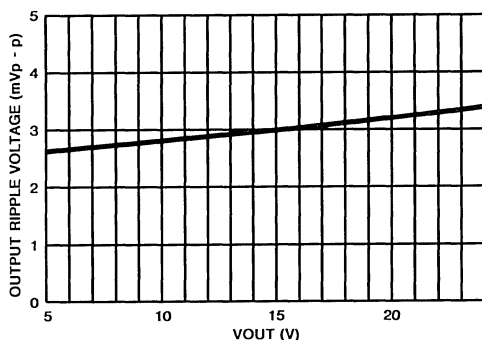
**DROPOUT VOLTAGE vs. TEMPERATURE**



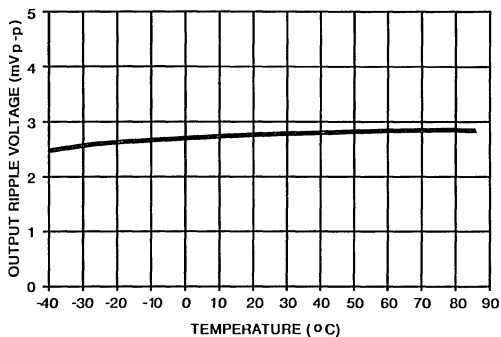
**QUIESCENT CURRENT vs. OUTPUT VOLTAGE @ +25°C**  
 $I_{OUT} = 5\text{mA to }50\text{mA}$



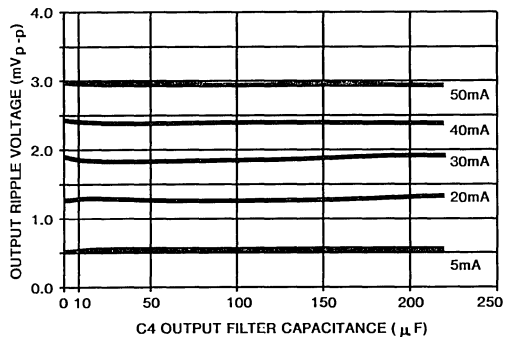
**OUTPUT RIPPLE VOLTAGE vs. OUTPUT VOLTAGE**  
 $I_{OUT} = 50\text{mA}$



**OUTPUT RIPPLE VOLTAGE vs. TEMPERATURE**  
 $C_4 = 1\mu\text{F}$



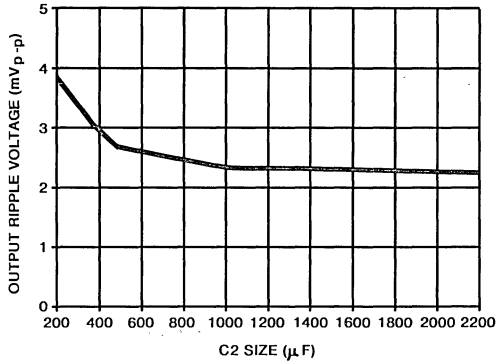
**OUTPUT RIPPLE VOLTAGE vs. LOAD CAPACITANCE AND OUTPUT CURRENT**



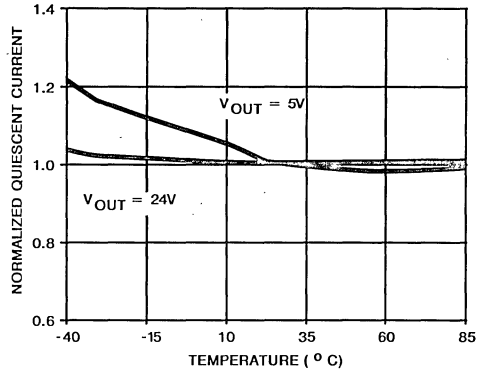
# HV-1205

**Typical Performance Curves** Unless Otherwise Specified:  $T_A = +25^\circ\text{C}$ ,  $V_{AC} = 120\text{Vrms}$ ,  $f = 60\text{Hz}$ ,  
 $R_1 = 150\Omega$ ,  $C_1 = 0.05\mu\text{F}$ ,  $C_2 = 470\mu\text{F}$ ,  $C_3 = 150\text{pF}$ ,  $C_4 = 1\mu\text{F}$ ,  $V_{OUT} = 5\text{V}$

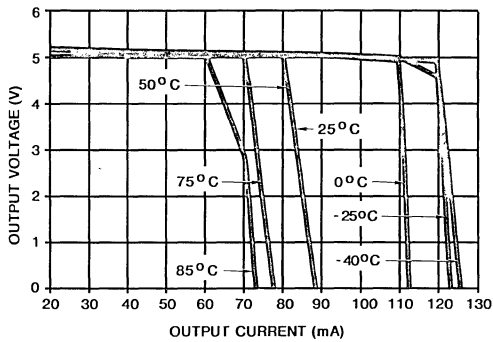
**OUTPUT RIPPLE VOLTAGE vs. C2 SIZE**  
 $I_{OUT} = 50\text{mA}$ ,  $V_{OUT} = 5\text{V}$



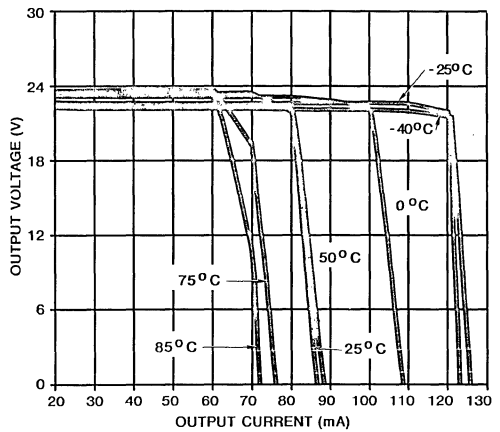
**NORMALIZED QUIESCENT CURRENT vs. TEMPERATURE**  
 Actual Quiescent Current at  $+25^\circ\text{C}$ :  $V_{OUT} = 24\text{V}$ : 3.42mA  
 $V_{OUT} = 5\text{V}$ : 0.41mA



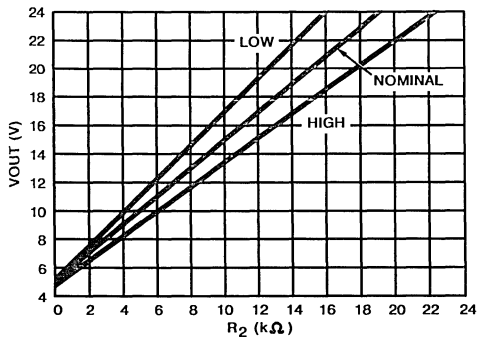
**OUTPUT CURRENT LIMIT (5V<sub>OUT</sub>)**  
 50mA is the Maximum Specified Output Current



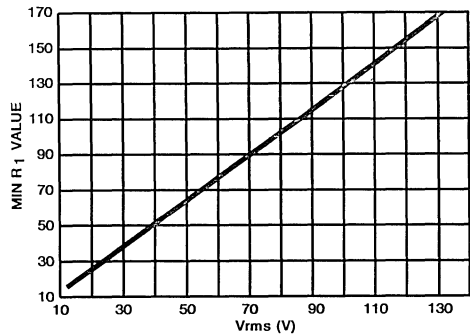
**OUTPUT CURRENT LIMIT (24V<sub>OUT</sub>)**  
 50mA is the Maximum Specified Output Current



**V<sub>OUT</sub> vs. R<sub>2</sub> WITH TOLERANCES**  
 Internal Resistors 15% High or Low

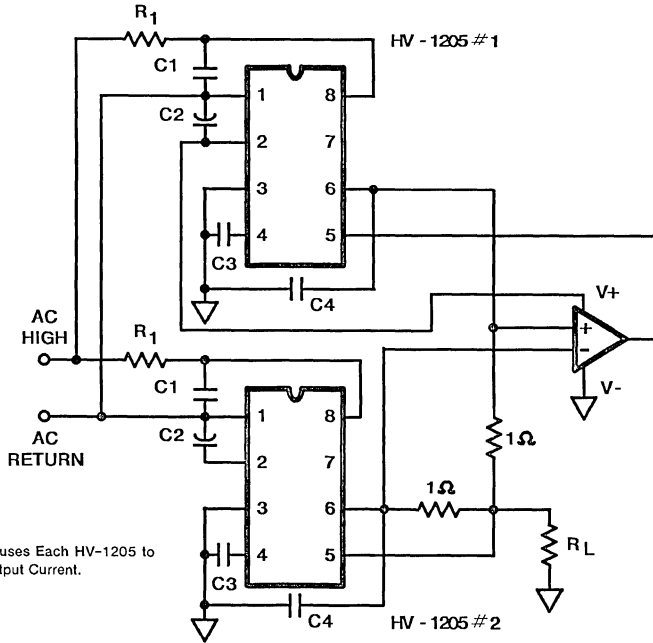


**MINIMUM ALLOWABLE R<sub>1</sub> FOR INPUT VOLTAGE**



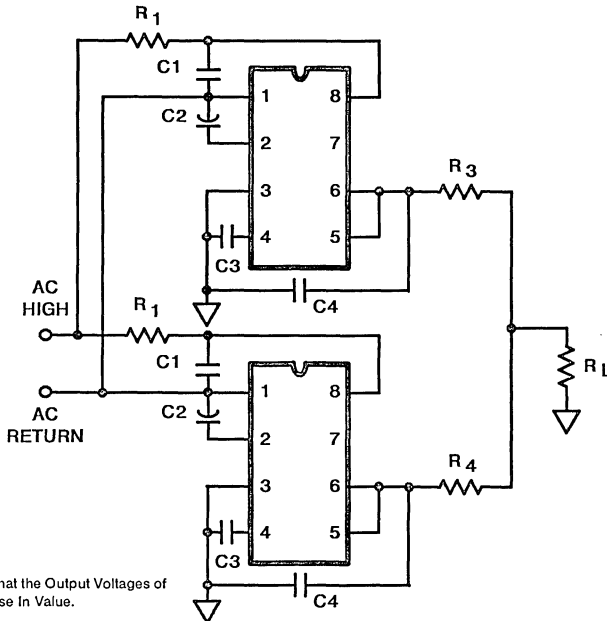
# HV-1205

## HV-1205 Parallel Operation (Method #1)



NOTE: Operational Amplifier Causes Each HV-1205 to Contribute Equally to Output Current.

## HV-1205 Parallel Operation (Method #2)



$$|I_{OUT}| = \frac{\Delta V_{OUT}}{R_3}$$

$$R_3 = R_4$$

NOTE: This Method Requires that the Output Voltages of Each HV-1205 are Close In Value.

## UL RECOGNIZED

August 1991

## World-Wide Single Chip Power Supply

### Features

- Direct AC to DC Conversion
- Wide Input Voltage Range ..... 18Vrms-264Vrms
- Multiple Output Voltages
- Guaranteed Output Current .....50mA\*
- Output Voltage ..... 5V to 24V
- Line and Load Regulation ..... <2%
- UL Recognition, File # E130808

### Applications

- Compact, Low Cost, Power Supply for Non-Isolated Applications
- Appliance Control
- Battery Back-Up Systems
- Dual Output Supply for OFF-LINE Motor Controls
- Housekeeping Supply for Switch-Mode Power Supplies

### Ordering Information

| PART NUMBER | OPERATING TEMPERATURE RANGE | PACKAGE DESCRIPTION     |
|-------------|-----------------------------|-------------------------|
| HV3-2405E-5 | 0°C to +75°C                | 8 Lead Plastic Mini-DIP |
| HV3-2405E-9 | -40°C to +85°C              | 8 Lead Plastic Mini-DIP |

**CAUTION:** This Product Does Not Provide Isolation From the AC Line

\*See App Note AN9101 for 250mA output.

### Description

The HV-2405E is a single chip power supply that can supply 5V to 24V at 50mA output current. Just a few inexpensive external components are needed to provide a compact, light weight, cost effective power supply. The HV-2405E replaces a transformer, rectifier, and voltage regulator. This chip is made in the new Harris High Voltage Dielectric Isolation Process. This high breakdown process (500V) allows a patented switching circuit to draw current from the AC line only as necessary to supply the load.

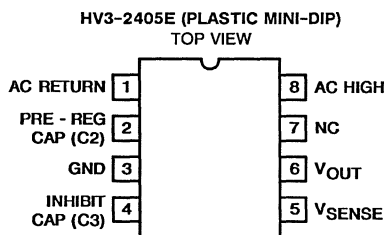
The wide input voltage range makes the HV-2405E an excellent choice for use in equipment which must operate from either 240V or 120V. Unlike competitive AC-DC convertors, the HV-2405E can use the same external components for operation from either voltage. In addition the HV-2405E can be connected across any two phases of a 3-phase system (208Vrms)\*. This great flexibility in input voltage allows a single design for worldwide use.

The HV-2405E is pin for pin compatible with the HV-1205 but allows twice the input voltage. Additionally, the output and sense pins are connected through a zener diode to limit output voltage should the sense pin to output connection become open.

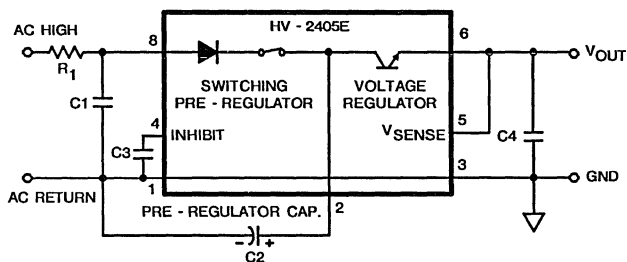
Further flexibility can be obtained from the HV-2405E by using it with other Harris chips. For example, the high efficiency ICL-7660S and ICL-7662 provide positive to negative voltage conversion. For automatic switch-over to battery back-up use the ICL 7673. Harris also offers a line of extremely low power op amps.

\* **CAUTION:** When used in this mode, GND and AC RETURN operate at high voltage with respect to earth ground.

### Pinout



### Functional Diagram



## Specifications HV-2405E

### Absolute Maximum Ratings

|   |                         |
|---|-------------------------|
| Voltage Between Pin 1 and 8, Continuous $V_{rms}$ ..... | 264Vrms                 |
| Voltage Between Pin 1 and 8, Peak .....                 | 500V                    |
| Voltage Between Pin 2 and 6 .....                       | 10V                     |
| Input Current, Peak .....                               | 2.5A                    |
| Output Current .....                                    | Short Circuit Protected |
| Output Voltage .....                                    | 30V                     |
| Maximum Junction Temperature.....                       | +150°C                  |

### Operating Temperature Range

|                                 |                             |
|---------------------------------|-----------------------------|
| HV3-2405E-9 .....               | -40°C to +85°C              |
| HV3-2405E-5 .....               | 0°C to +75°C                |
| Storage Temperature Range ..... | -65°C to +175°C             |
| Thermal Constants (°C/W)        | $\theta_{ja}$ $\theta_{jc}$ |
| Plastic DIP                     | 82            16            |

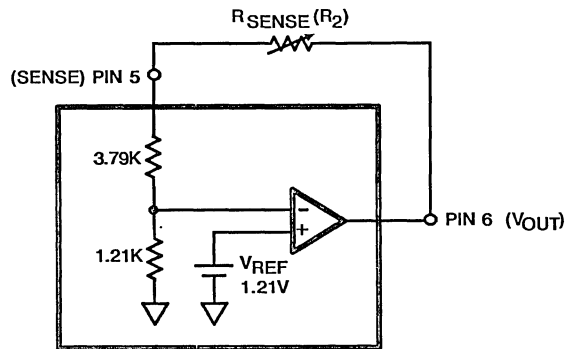
### Electrical Specifications

Unless Otherwise Specified:  $V_{IN} = 264V_{rms}$  at 50Hz,  $C1 = 0.05\mu F$ ,  $C2 = 470\mu F$ ,  $C3 = 150pF$ ,  $V_{OUT} = 5V$ ,  $I_{OUT} = 50mA$ , Source Impedance,  $R_1 = 150\Omega$ . Parameters are Guaranteed at the Specific  $V_{IN}$  and Frequency Conditions, Unless Otherwise Specified. See Functional Diagrams for Component Location.

| PARAMETER  | $V_{IN}$   | TEMP  | HV-2405E-9<br>-40°C to +85°C |      |      | HV-2405E-5<br>0°C to +75°C |      |      | UNITS |
|--|--|-------|------------------------------|------|------|----------------------------|------|------|-------|
|  |  |       | MIN                          | TYP  | MAX  | MIN                        | TYP  | MAX  |       |
| Output Voltage<br>(At Preset 5V)                       | 264V   | +25°C | 4.75                         | 5.0  | 5.25 | 4.75                       | 5.0  | 5.25 | V     |
|  | 264V   | Full  | 4.65                         | 5.0  | 5.35 | 4.65                       | 5.0  | 5.35 | V     |
| Output Voltage TC                                      | 264V   | Full  | -                            | 0.02 | -    | -                          | 0.02 | -    | %/°C  |
| Output Ripple (Vp-p)<br>( $C4 = 1\mu F$ , $f = 50Hz$ ) | 264V   | +25°C | -                            | 22   | -    | -                          | 22   | -    | mV    |
|  | 264V   | Full  | -                            | 24   | -    | -                          | 24   | -    | mV    |
| Line Regulation  | 80Vrms to<br>264Vrms                               | +25°C | -                            | 10   | 15   | -                          | 10   | 20   | mV    |
|  |  | Full  | -                            | 15   | 30   | -                          | 15   | 40   | mV    |
| Load Regulation<br>( $I_{OUT} = 5mA$ to $50mA$ )       | 264V   | +25°C | -                            | -    | 15   | -                          | -    | 20   | mV    |
|  | 264V   | Full  | -                            | -    | 30   | -                          | -    | 40   | mV    |
| Output Current   | 264V   | Full  | 0                            | -    | 50   | 0                          | -    | 50   | mA    |
| Short Circuit Current Limit                            | 264V   | Full  | 55                           | 95   | -    | 55                         | 95   | -    | mA    |
| Drop-Out Voltage                                       | Pin 2 - Pin 6                                      | +25°C | -                            | 2.2  | -    | -                          | 2.2  | -    | V     |
| Quiescent Current<br>Post Regulator                    | 11V <sub>DC</sub> to 30V <sub>DC</sub><br>On Pin 2 | +25°C | -                            | 2    | -    | -                          | 2    | -    | mA    |

### Equivalent Circuit For Output Voltage Adjustment

$R_2 = V_{OUT} - 5V$  Where  $R_2$  is the Approximate Value of Resistor Between Pin 5 and Pin 6 (in K $\Omega$ ).  $V_{OUT}$  is the Desired Output Voltage. See Graph.



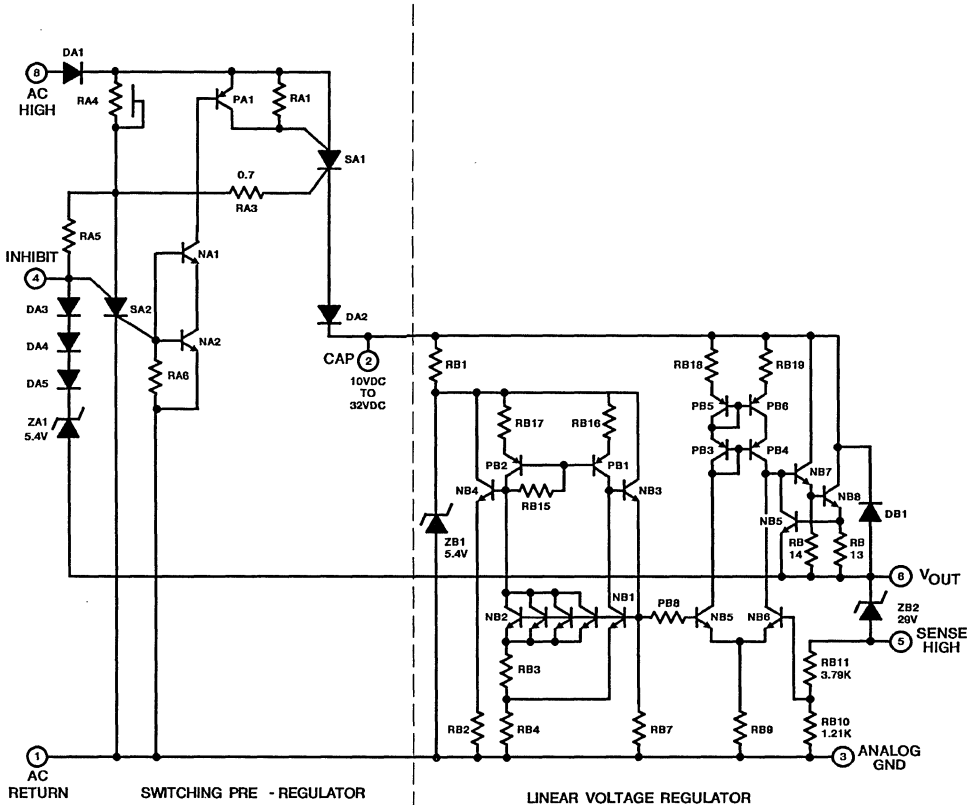
$R_{SENSE}$  IS ZERO OHMS FOR 5V OUTPUT

FIGURE 1.



# HV-2405E

## Schematic



Patent pending on the above circuit.

## Application Information

### How The HV-2405E Works

The HV-2405E converts AC voltage into regulated DC voltage to power low voltage components such as integrated circuits. This is accomplished in two stages on the monolithic chip. First, the pre-regulator momentarily connects a large capacitor to the AC high line until it charges to about 6V above the selected output voltage. The pre-regulator then switches to a blocking mode and stays in that blocking mode until the next line cycle begins. The large capacitor supplies power to the series pass regulator, providing DC current to power the user's circuit. Providing current to the post regulator causes the large cap to discharge at a rate dependent on load current. Each line cycle refreshes the charge on the electrolytic capacitor.

### Input Voltage

The HV-2405E operates over a wide range of input voltages. Most applications will use the 240Vrms or 120Vrms line from the power grid. A standard circuit for this application is shown in Figure 2. Much smaller input voltages can be used. The size of the external components used will be determined by the output voltage and current required and the input voltage available. Several graphs have been provided to help choose component values for a specific application. The section below called Component Selection discusses trade-offs related to component sizing.

### Input Frequency

The HV-2405E is designed to operate from 48Hz to 380Hz. Higher operating frequency is possible. Keep in mind that the HV-2405E will refresh C2 once per line cycle.

### Setting Output Voltage

The HV-2405E can be set to provide a regulated output voltage anywhere from 5V to 24V<sub>DC</sub>. Refer to Figures 4, 5 and 6 for several ways of adjusting output voltage.

As seen in Figure 1, output voltage is set by feedback to the sense pin. The output will rise to the voltage necessary to keep the sense pin at 5V. For a 5V output, pins 5 and 6 are shorted together. There are three ways to increase the output voltage beyond 5V. The simplest method is to increase the feedback resistor by adding an external resistor between pins 5 and 6. The disadvantage is that the internal circuit resistors have a tolerance of approximately ±15% which limits the accuracy of the predicted output (see graph). The internal thin film resistors have low temperature coefficients.

An external voltage divider as shown in Figure 5 improves the accuracy as long as the external resistors are much lower in value than those of the internal divider. Approximately 1mA flows into pin 5.

A zener diode between pins 5 and 6, as shown in Figure 6, sets the output voltage above 5V by the zener's breakdown voltage at 1mA. This voltage has the accuracy and tolerance of the zener. An added advantage is that two outputs are now available, pin 5 at 5V and pin 6 at V<sub>Z</sub> + 5V. All the current from the 5V supply flows through the reference diode. The sum of both output currents should not exceed 50mA.

The HV-2405E has an internal zener diode to clamp the output above the 24V maximum but below a damaging level.

### Output Current

Any current draw up to 50mA continuous is acceptable. More current can be drawn momentarily. Care should be taken to make sure C2 is not discharged below the dropout voltage and that the duty cycle of the excess current is low enough to not cause a package power dissipation problem. The output is current limited as shown in the graph to protect against shorted loads.

### Component Selection

One of the most powerful features of the HV-2405E is its flexibility. One standard configuration allows enormous variation in input voltage and output current while still maintaining a regulated output. For example, with R<sub>1</sub> = 150Ω, C2 = 470μF and V<sub>OUT</sub> = 5V, the HV-2405E will provide a regulated 50mA output when input voltage is anywhere from 264V<sub>AC</sub> down to about 28V<sub>AC</sub>. The designer can choose components tailored to his application in order to save cost, space, power dissipation etc.

Below is a list of external components, description of their purpose, and a recommended value. This is a full list of possible components all of which may not be required for an intended application. Most designs will use a subset of this list.

- F1:** Fuse. Opens the connections to the power line should chip or C2 fail. Recommended value = 1/2A, 2AG similar to Littlefuse 225.5000.
- R<sub>1</sub>:** Source Resistance. Limits current into HV-2405E. Needs to be large enough to limit inrush current when C2 is discharged fully. V<sub>PEAK</sub>/R<sub>1</sub> = 2.5A Maximum. R<sub>1</sub> will dissipate power as shown in the graphs. The equation for Pd in R<sub>1</sub> is:  

$$Pd = 1.33 \sqrt{\pi R_1} V_{PEAK}(I_{OUT})^3$$
 Low average output currents would allow for source resistors with lower Pd ratings. Similarly, lower V<sub>AC</sub> or smaller value R<sub>1</sub> will cause less dissipation in R<sub>1</sub>. Sizing of R<sub>1</sub> should be tailored to the intended application keeping in mind not to let the maximum inrush current be exceeded. Should an external method of limiting inrush current be used (such as NTC resistors) then the value of R<sub>1</sub> and its associated heat could be reduced. Recommended value = 150Ω. To reduce Pd see App Note AN9107.
- C1:** Snubber Capacitor. R<sub>1</sub> and C1 form a low pass filter thereby limiting the rate of voltage rise at the input of the HV-2405E. Recommended value = 0.05μF, AC rated.
- MOV:** Surge suppressor. Metal Oxide Varistor clamps voltage to a level that the HV-2405E can handle. Recommended value = V130LA20 or equivalent for 120V applications and gas tube which arcs over at less than 500V for 240V applicatons.

**Application Information (Continued)**

- C2: Pre-Regulator capacitor. This capacitor is charged once each line cycle. The post-regulator portion of HV-2405E is powered by C2 for most of the line cycle. Normally the smallest C2 that will supply the load current (see graph) is used. Using a large C2 will supply temporary high load currents or normal load current during a short power loss. Using a larger C2 will reduce ripple at Pin 2, the input to the post regulator, which will reduce output ripple. C2 should have a ripple current rating consistent with the application. Small capacitors with high ESR may not store enough charge to maintain load current. See graph. Recommended value = 470µF, voltage rating should be about 10V greater than chosen V<sub>OUT</sub>.
- C3: Inhibit capacitor. Keeps the HV-2405E from turning on during input transients. If sized too large, HV-2405E will never turn on. If sized too small, no

protection from transients is offered. For 50Hz or 60Hz use the recommended value of 150pF, voltage rating should be at about 10V greater than V<sub>OUT</sub>.

- C4: Output filter capacitor. At least 1µF is required to maintain stability of the output stage. Larger values will not reduce ripple but will reduce spiking which may occur on the output coincident with the HV-2405E going into blocking mode.
- R2: Feedback component. A resistor or zener diode that causes a voltage drop between the SENSE and OUTPUT pins and thereby adjusting the output voltage. See voltage adjustment equivalent circuit. Also see graph for approximate resistor value. About 1mA flows through this component.

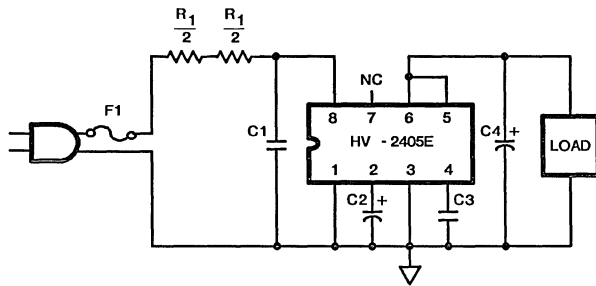


FIGURE 2. HV-2405E STANDARD +5V APPLICATION

**V<sub>OUT</sub> ADJUSTMENT**

| FIGURE 4 METHOD |                | FIGURE 5 METHOD                |                | FIGURE 6 METHOD  |                |
|-----------------|----------------|--------------------------------|----------------|------------------|----------------|
| R <sub>2</sub>  | V <sub>O</sub> | R <sub>A</sub> /R <sub>B</sub> | V <sub>O</sub> | V <sub>Z</sub> * | V <sub>O</sub> |
| 0               | 5V             | 0/Open                         | 5V             | -                | 5V             |
| 1K              | 6V             | 160/1K                         | 6V             | 1V               | 6V             |
| 3K              | 8V             | 510/1K                         | 8V             | 3V               | 8V             |
| 5K              | 10V            | 820/1K                         | 10V            | 5V               | 10V            |
| 7K              | 12V            | 1.2K/1K                        | 12.2V          | 7V               | 12V            |
| 9K              | 14V            | 1.5K/1K                        | 14V            | 9V               | 14V            |
| 11K             | 16V            | 1.8K/1K                        | 15.8V          | 11V              | 16V            |
| 13K             | 18V            | 2.2K/1K                        | 18.2V          | 13V              | 18V            |
| 15K             | 20V            | 2.4K/1K                        | 19.4V          | 15V              | 20V            |
| 17K             | 22V            | 3.0K/1K                        | 23V            | 17V              | 22V            |
| 19K             | 24V            | 3.17K/1K                       | 24V            | 19V              | 24V            |

\*V<sub>Z</sub> @ 1mA

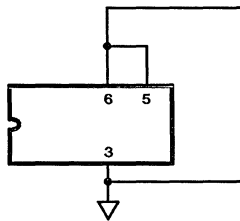


FIGURE 3. V<sub>OUT</sub> = +5V

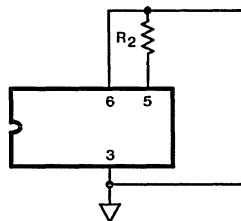


FIGURE 4. V<sub>OUT</sub> > +5V

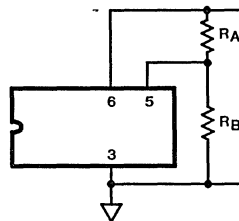


FIGURE 5. V<sub>OUT</sub> > +5V

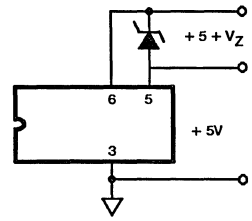
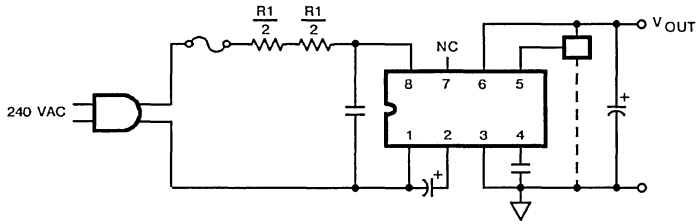


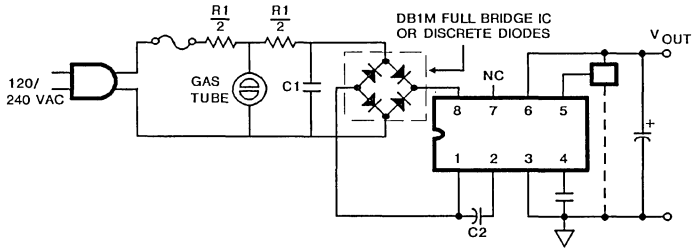
FIGURE 6. V<sub>OUT</sub> = +5V, +5 +V<sub>Z</sub>

Application Information (Continued)

OPERATION WITH  $V_{OUT} > 5V$

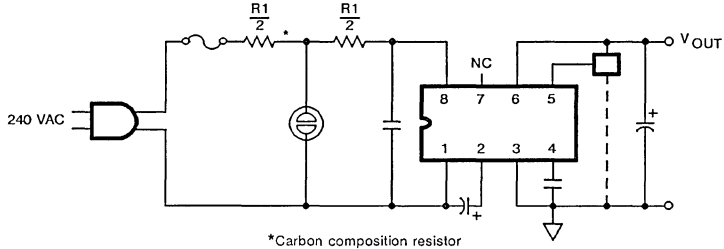


OPERATION FROM A BRIDGE RECTIFIER\*



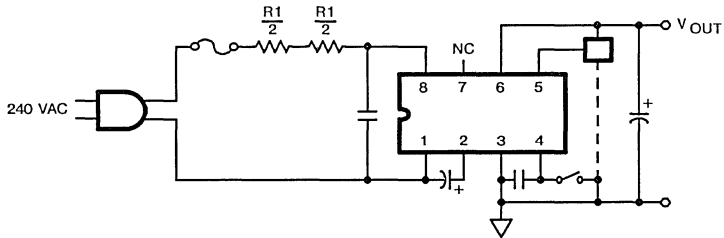
\*See App Note AN9006 for additional information.

SURGE PROTECTION USING GAS TUBE



\*Carbon composition resistor

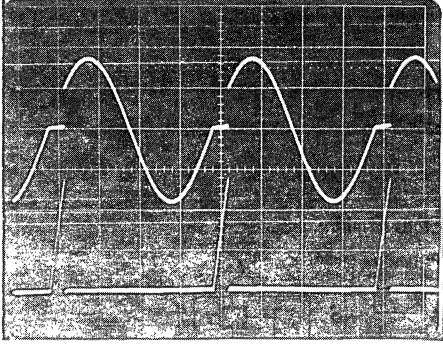
USING SWITCH TO TURN OFF OUTPUT



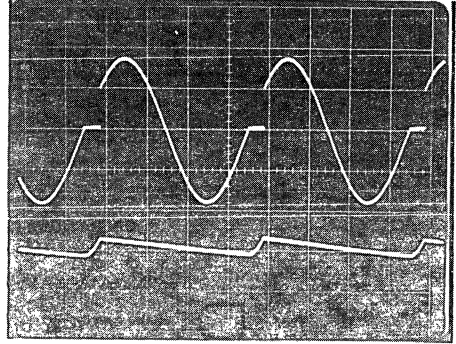
## HV-2405E

**HV-2405E Waveforms** Unless Otherwise Specified:  $T_A = +25^\circ\text{C}$ ,  $V_{AC} = 240\text{Vrms}$ ,  $f = 50\text{Hz}$ ,  
 $R_1 = 150\Omega$ ,  $C_1 = 0.05\mu\text{F}$ ,  $C_2 = 470\mu\text{F}$ ,  $C_3 = 150\text{pF}$ ,  $C_4 = 1\mu\text{F}$ ,  
 $V_{OUT} = 5\text{V @ } 50\text{mA}$ , 5ms/div

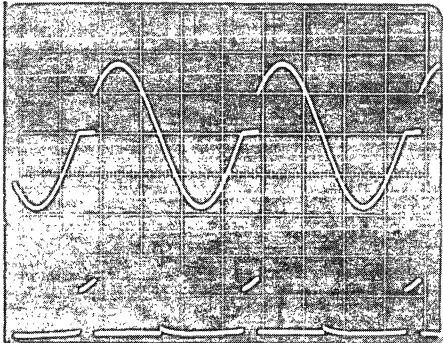
Top Trace: Input Voltage at Pin 8, AC High (200V/Div)  
 Bottom Trace: Current into Pin 8, (0.5A/Div)



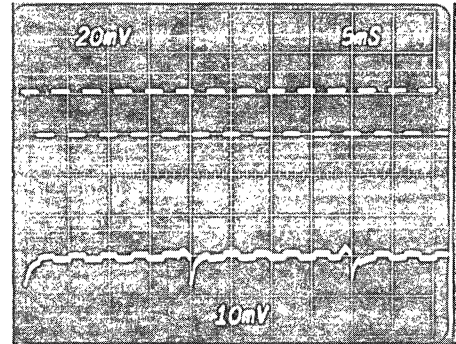
Top Trace: Input Voltage at Pin 8, AC High (200V/Div)  
 Bottom Trace: Pre-Regulator Capacitor Voltage, C2 (5V/Div)  
 @ Approximately 10V DC



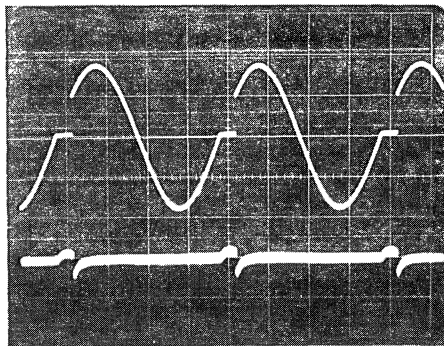
Top Trace: Input Voltage at Pin 8, AC High (200V/Div)  
 Bottom Trace: Inhibit Capacitor Voltage (10V/Div)



Top Trace: Load Current Step (50mA/Div)  
 Bottom Trace: Output Voltage (20mV/Div) @ 5VDC



Top Trace: Input Voltage at Pin 8, AC High (200V/Div)  
 Bottom Trace: Ripple or Switch Spike on Regulator 5V DC Output (50mV/Div)  
 This is Worst Case Ripple due to Worst Case Operating Conditions  
 (High Line Voltage, Minimum R1 Value, Maximum  $I_{OUT}$ )

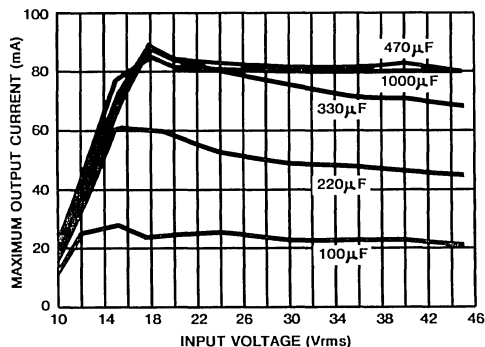


# HV-2405E

**Typical Performance Curves** Unless Otherwise Specified:  $T_A = +25^\circ\text{C}$ ,  $V_{AC} = 240\text{Vrms}$ ,  $f = 50\text{Hz}$ ,  $R_1 = 150\Omega$ ,  $C_1 = 0.05\mu\text{F}$ ,  $C_2 = 470\mu\text{F}$ ,  $C_3 = 150\text{pF}$ ,  $C_4 = 1\mu\text{F}$ ,  $V_{OUT} = 5\text{V}$

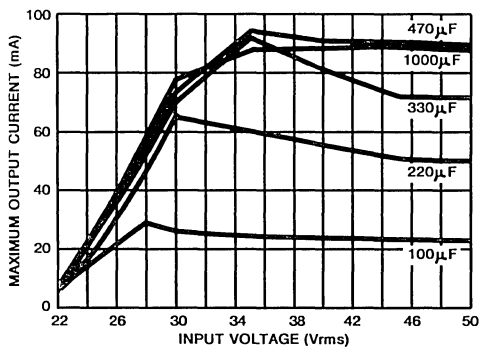
**MAXIMUM OUTPUT CURRENT FOR 5V REGULATED OUTPUT vs. INPUT VOLTAGE AND PRE-REGULATOR CAPACITOR SIZE (C2)**

$R_1 = 24\Omega$

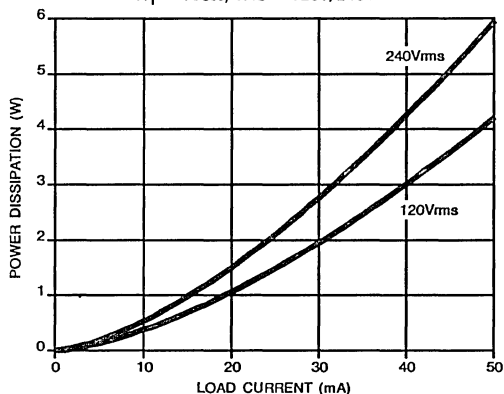


**MAXIMUM OUTPUT CURRENT FOR 24V REGULATED OUTPUT vs. INPUT VOLTAGE AND PRE-REGULATOR CAPACITOR SIZE (C2)**

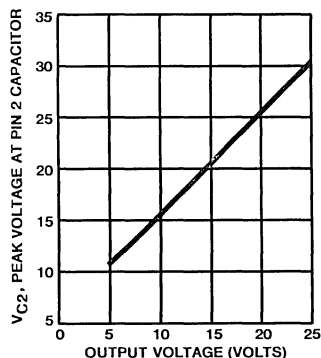
$R_1 = 24\Omega$



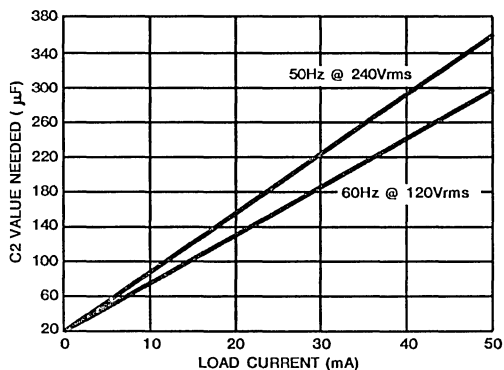
**Pd IN R1 vs. IOUT**  
 $R_1 = 150\Omega$ ,  $V_{AC} = 120\text{V}/240\text{V}$



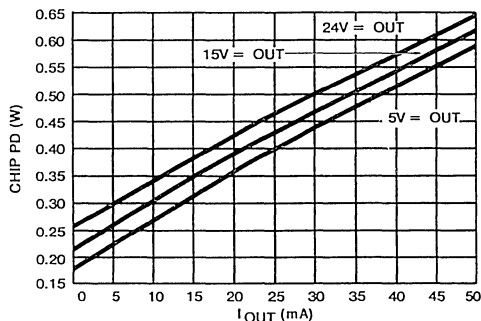
**PEAK C2 VOLTAGE vs. OUTPUT VOLTAGE**



**MINIMUM C2 VALUE vs. LOAD CURRENT**



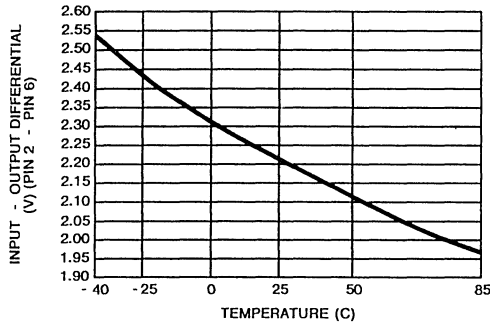
**CHIP POWER DISSIPATION vs. OUTPUT CURRENT**



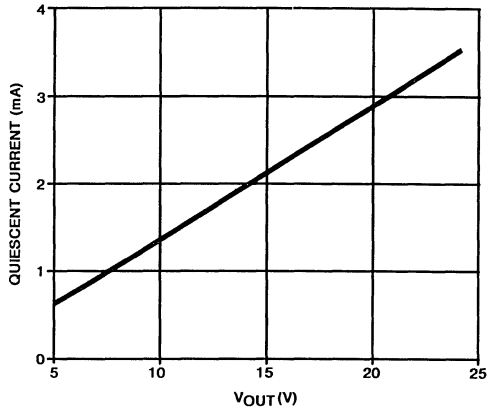
# HV-2405E

**Typical Performance Curves** Unless Otherwise Specified:  $T_A = +25^\circ\text{C}$ ,  $V_{AC} = 240\text{Vrms}$ ,  $f = 50\text{Hz}$ ,  
 $R_1 = 150\Omega$ ,  $C_1 = 0.05\mu\text{F}$ ,  $C_2 = 470\mu\text{F}$ ,  $C_3 = 150\text{pF}$ ,  $C_4 = 1\mu\text{F}$ ,  $V_{OUT} = 5\text{V}$

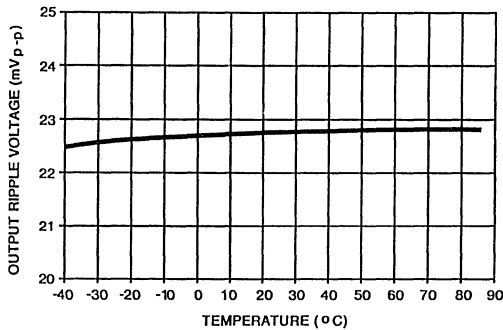
**DROPOUT VOLTAGE vs. TEMPERATURE**



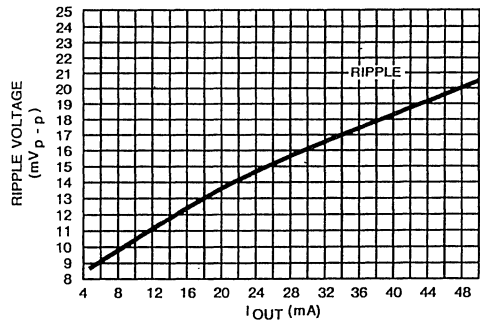
**QUIESCENT CURRENT vs. OUTPUT VOLTAGE @ +25°C**  
 $I_{OUT} = 5\text{mA to } 50\text{mA}$



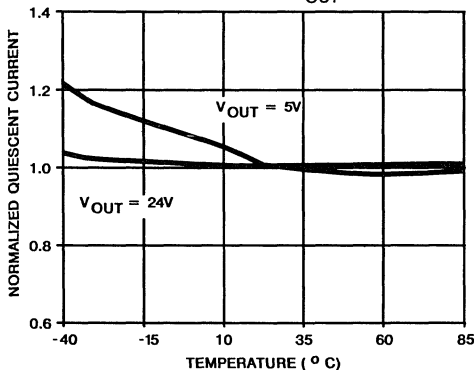
**OUTPUT RIPPLE VOLTAGE vs. TEMPERATURE**  
 $C_4 = 1\mu\text{F}$



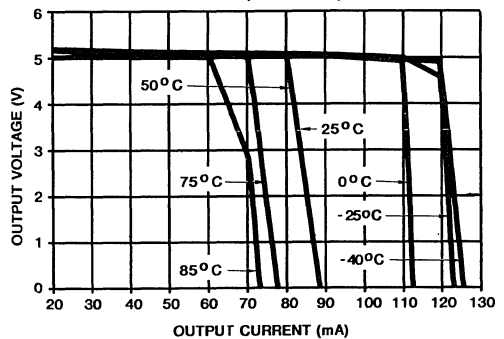
**OUTPUT RIPPLE VOLTAGE vs. LOAD CURRENT**



**NORMALIZED QUIESCENT CURRENT vs. TEMPERATURE**  
 Actual Quiescent Current at +25°C:  $V_{OUT} = 24\text{V}$ : 3.42mA  
 $V_{OUT} = 5\text{V}$ : 0.41mA

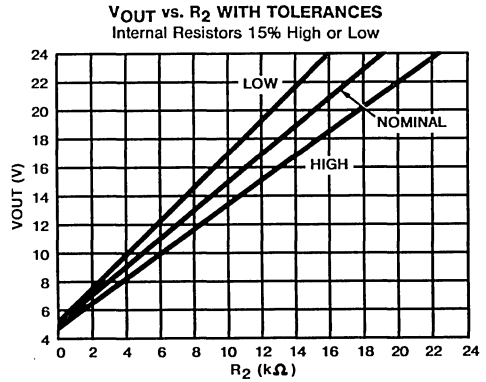
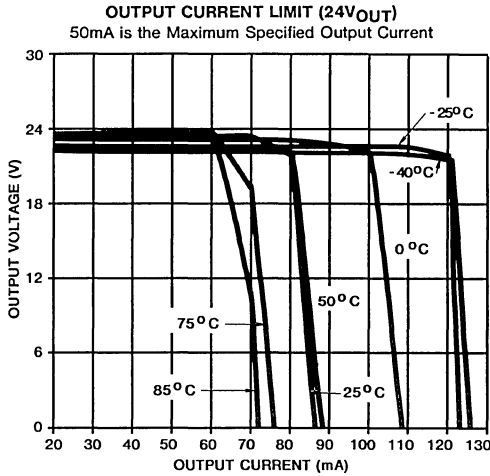


**OUTPUT CURRENT LIMIT (5V<sub>OUT</sub>)**  
 50mA is the Maximum Specified Output Current

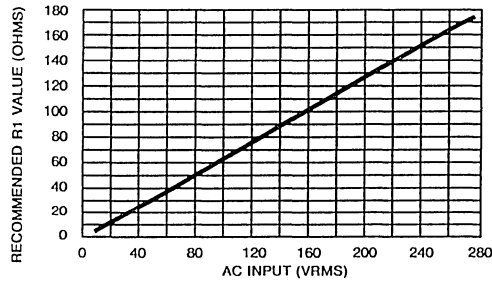


# HV-2405E

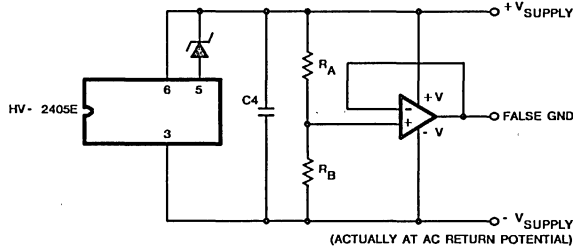
**Typical Performance Curves** Unless Otherwise Specified:  $T_A = +25^\circ\text{C}$ ,  $V_{AC} = 240\text{Vrms}$ ,  $f = 50\text{Hz}$ ,  
 $R_1 = 150\Omega$ ,  $C_1 = 0.05\mu\text{F}$ ,  $C_2 = 470\mu\text{F}$ ,  $C_3 = 150\text{pF}$ ,  $C_4 = 1\mu\text{F}$ ,  $V_{OUT} = 5\text{V}$



**MINIMUM RECOMMENDED  $R_1$  FOR NOMINAL INPUT VOLTAGE**



**CREATING SYNTHESIZED  $\pm$  SUPPLIES USING FALSE GROUND**



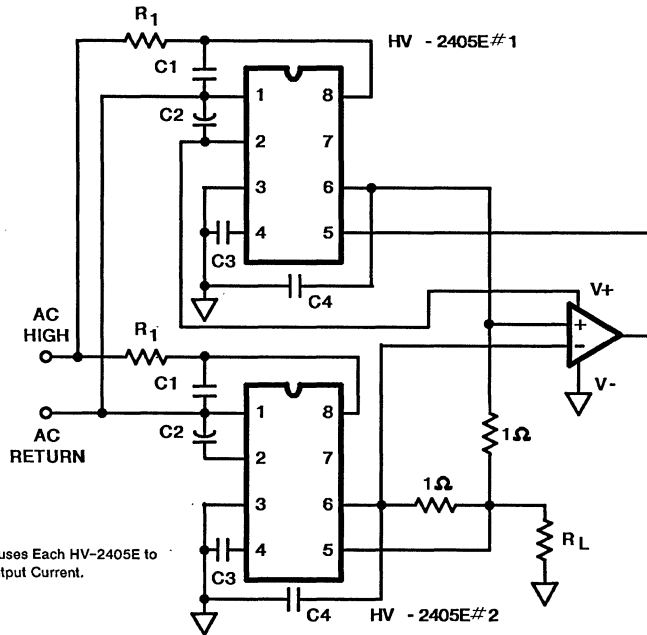
**NOTES:**

1.  $R_A$ ,  $R_B$  voltage divider sets voltage of false ground anywhere between  $V_{OUT}$  of HV-2405E and ground.
2.  $R_A$  and  $R_B$  should be large values (e.g. 470K)
3. Circuits powered with this method must ALL be referred to "False Gnd"
4. Op amp must be able to source/sink load current
5. Example:  $R_A = 470\text{K}$ ,  $R_B = 470\text{K}$ ,  $V_{OUT}$  set to 24V.  $+V_{SUPPLY}$  would be  $\approx +12\text{V}$   
 $-V_{SUPPLY}$  would be  $\approx -12\text{V}$



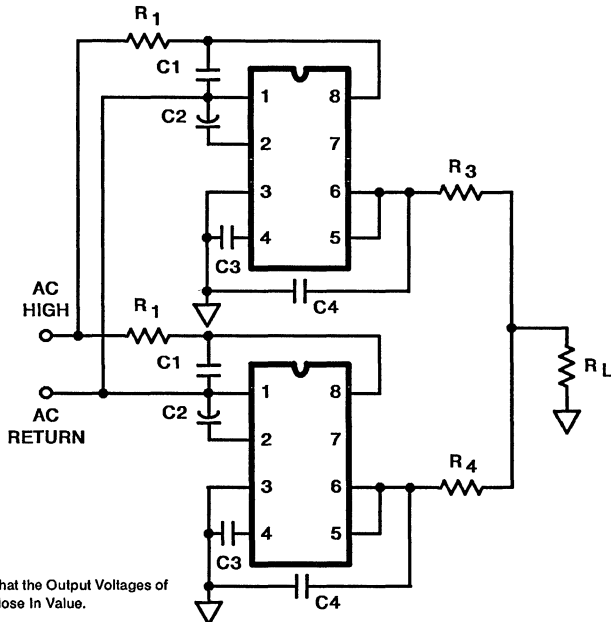
## HV-2405E

### HV-2405E Parallel Operation (Method #1)



NOTE: Operational Amplifier Causes Each HV-2405E to Contribute Equally to Output Current.

### HV-2405E Parallel Operation (Method #2)



$$\Delta I_{OUT} = \frac{\Delta V_{OUT}}{R_3}$$

$$R_3 = R_4$$

NOTE: This Method Requires that the Output Voltages of Each HV-2405E are Close In Value.



# HARRIS

# ICL644/645/646/647 ICL7644/7645/7646/7647

July 1991

## Low Voltage Step-Up Converters

### Features

- +5V @ 40mA from a Single Cell Battery. Note: Output Current can be Increased by Changing L2 (See Table 1)
- Guaranteed Start-up .....@1.15V  
Typ 0.9V
- Standby Mode ..... 80µA Quiescent Current
- Low Battery Indication
- Power Ready Function
- Shutdown Feature on  
764X Series ..... 5µA Max Quiescent
- Pin to Pin Compatible to MAX65X Series
- Efficiency ..... 75% @ 1.2V Input

### Applications

- Battery Powered Devices
- Single Cell Instruments
- Solar Powered Systems
- Pagers and Radio Controlled Receivers
- Portable Instruments
- 4-20mA Loop Powered Instruments

### Description

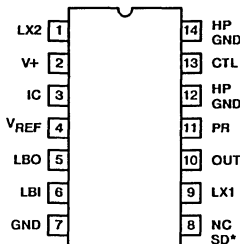
The ICL644, ICL645 and ICL646 are low power fixed +5V output step-up DC-DC converters designed for operation from very low input voltages. All control functions and a power FET are contained in the ICL644, ICL645 and ICL647, minimizing external components. The ICL646 contains an output pin to drive an external FET when higher output currents are required. A control pin changes between high power and low power standby modes. Standby mode allows operating for extended periods with minimum battery drain, and a power ready function is available for controlling external devices when the device is switched between standby and high power. In high power mode, the output current is approximately 40mA; in standby mode, it is about 500µA.

Minimum startup voltage is 1.15V, but once started the device will operate to lower voltages as the battery discharges. A separate low battery monitor is available; it can be used at its default value of 1.17V or may be adjusted by the designer to any higher voltage.

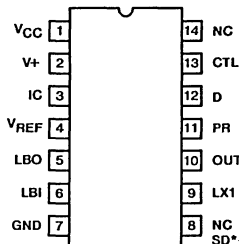
The ICL644, ICL646 and ICL647 are optimized for single cell (1.15V to 1.6V) battery operation and can also be used with input voltages up to 4.0V. The ICL645 is designed for two cell (or single lithium cell) operation with typical battery voltages of 2.0V to 3.6V. The ICL647 is identical to the ICL644 except its output voltage is preset to +3V. The ICL764X series of products offer the same features as the ICL64X with the addition of a shutdown feature. In the shutdown mode the quiescent current is less than 5µA.

### Pinouts

ICL644, ICL645 & ICL647  
ICL7644, ICL7645 & ICL7647  
TOP VIEW



ICL646  
ICL7646  
TOP VIEW



\* Pin 8 Used On 764X Series Only.

### Ordering Information

| PART NUMBER | TEMPERATURE RANGE | PACKAGE            |
|-------------|-------------------|--------------------|
| ICL64XCPD   | 0°C to +70°C      | 14 Pin Plastic DIP |
| ICL64XCBD   | 0°C to +70°C      | 14 Pin SOIC        |
| ICL64XIPD   | -40°C to +85°C    | 14 Pin Plastic DIP |
| ICL64XIBD   | -40°C to +85°C    | 14 Pin SOIC        |
| ICL764XCPD  | 0°C to +70°C      | 14 Pin Plastic DIP |
| ICL764XCBD  | 0°C to +70°C      | 14 Pin SOIC        |
| ICL764XIPD  | -40°C to +85°C    | 14 Pin Plastic DIP |
| ICL764XIBD  | -40°C to +85°C    | 14 Pin SOIC        |

X = 4, 5, 6 or 7

2  
POWER PROCESSING  
CIRCUITS

## Specifications ICL644/645/646/647 ICL7644/7645/7646/7647

### Absolute Maximum Ratings

|  |                                 |
|--|---------------------------------|
| Peak Voltage at LX1 Pin .....                    | +16V                            |
| Peak Voltage at LX2 or V <sub>CC</sub> Pin ..... | +6.6V                           |
| Supply Voltage to L1 .....                       | +15V                            |
| Supply Voltage to L2, V <sub>CC</sub> .....      | +5.6V                           |
| Peak Current, LX1 .....                          | 50mA                            |
| Peak Current, LX2 .....                          | 1.6A                            |
| LBO Output Current .....                         | 50mA                            |
| Input Voltage, CTL, LBI (See Note) .....         | -0.3V to (V <sup>+</sup> +0.3V) |

### Operating Temperature

|   |                 |
|---|-----------------|
| ICL64XCXX .....                               | 0°C to +70°C    |
| ICL64XIXX .....                               | -40°C to +85°C  |
| Storage Temperature .....                     | -65°C to +160°C |
| Lead Temperature (Soldering, 10 Sec) .....    | +300°C          |
| Power Dissipation                             |                 |
| Plastic DIP (derate 10mW/°C above 70°C) ..... | 800mW           |
| SOIC (derate 8.7mW/°C above 70°C) .....       | 695mW           |

NOTE: V<sup>+</sup> is generated at LX1. In low current mode, it is 4.5V to 5.6V (2.6V to 3.6V on ICL646 & ICL7646); in high current mode, it is 10V to 15V.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Electrical Specifications:** ICL644, ICL646, ICL647, ICL7644, ICL7646, ICL7647  
(GND = 0V, V<sub>BATT</sub> = 1.2V, T<sub>A</sub> = 25°C, Unless Otherwise Specified.)

| SYMBOL            | PARAMETER                           | TEST CONDITIONS  | LIMITS              |                          |      | UNITS |
|-------------------|-------------------------------------|--|---------------------|--------------------------|------|-------|
|                   |                                     |  | MIN                 | TYP                      | MAX  |       |
| V <sub>OUT</sub>  | Output Voltage                      | ICL644, ICL646 T <sub>A</sub> = Over Temp.*            | 4.5                 | 5.0                      | 5.5  | V     |
|                   |                                     | ICL647 T <sub>A</sub> = Over Temp.*                    | 2.7                 | 3.0                      | 3.3  | V     |
| V <sub>LX1</sub>  | Minimum Input Voltage to LX1        | I <sub>L</sub> = 0μA (Note 1)                          | -                   | 0.9                      | 1.0  | V     |
| V <sub>LX1</sub>  | Minimum Startup Voltage to LX1      | I <sub>L</sub> = 0μA                                   | -                   | 0.9                      | 1.15 | V     |
| V <sub>LX2</sub>  | Input Voltage to LX2                |  | 0.5                 | -                        | 5.6  | V     |
| I <sub>LX2</sub>  | Peak LX2 Switch Current             | ICL644, ICL647 (Note 1)                                | -                   | -                        | 1.5  | A     |
| I <sub>Q</sub>    | Standby Current                     | I <sub>L</sub> = 0μA, CTL = Open                       | -                   | 80                       | -    | μA    |
| f <sub>O</sub>    | Switching Frequency                 | V <sub>BATT</sub> = 1.0 to 1.6V                        | 15.5                | 18                       | 24   | kHz   |
| %ON               | LX2, D Switch Duty Cycle            | ICL644, ICL646   | 66                  | 75                       | 80   | %     |
|                   |                                     | ICL647   | 50                  | 66                       | 75   | %     |
| t <sub>ON</sub>   | LX2, D Switch On Time               | ICL644, ICL646   | 27                  | 36                       | 49   | μs    |
|                   |                                     | ICL647   | 20                  | 37                       | 47   | μs    |
| R <sub>DSON</sub> | LX2 On Resistance                   | ICL646, ICL647 (Note 1)                                | 0.40                | -                        | 0.67 | Ω     |
|                   |                                     | D Output Saturation Current<br>(Short Circuit Current) | ICL646, Source Sink | -                        | -25  | -     |
|                   |                                     |  | -                   | 100                      | -    | mA    |
| V <sub>LBI</sub>  | Low Battery Input Threshold Voltage |  | 1.12                |                          | 1.18 | V     |
|                   |                                     | Low Battery Input Threshold Tempco                     | -                   | -0.5                     | -    | mV/°C |
| I <sub>LBI</sub>  | Low Battery Input Bias Current      |  | -                   | 0.01                     | 10   | nA    |
| V <sub>LBO</sub>  | Low Battery Output                  | V <sub>LBI</sub> < 1.12V, I <sub>LBO</sub> = 1.6mA     | -                   | -                        | 0.4  | V     |
|                   |                                     | V <sub>LBI</sub> > 1.18V, I <sub>LBO</sub> = -1μA      | V <sup>+</sup> -1   | -                        | -    | V     |
| V <sub>PR</sub>   | Power Ready                         | PR High, I <sub>PR</sub> = -1μA                        | -                   | V <sub>OUT</sub><br>-0.2 | -    | V     |
|                   |                                     | PR Low, I <sub>PR</sub> = 1μA                          | -                   | 0.3                      | -    | V     |
| V <sub>CTL</sub>  | CTL Input Threshold                 |  | -                   | 0.07                     | -    | V     |
|                   | Efficiency                          | 5ma ≤ I <sub>LOAD</sub> ≤ 40ma                         | -                   | 75                       | -    | %     |

NOTE: 1. Not tested, guaranteed by design and characterization.

\* Commercial Temperature Range = 0°C to +70°C  
Industrial Temperature Range = -40°C to +85°C

**Specifications ICL644/645/646/647 ICL7644/7645/7646/7647**

**Electrical Specifications:** ICL645 & ICL7645 (GND = 0V, V<sub>BATT</sub> = 2.4V, T<sub>A</sub> = 25°C, Unless Otherwise Specified.)

| SYMBOL            | PARAMETER                           | TEST CONDITIONS                                    | LIMITS            |                       |      | UNITS |
|-------------------|-------------------------------------|--|-------------------|-----------------------|------|-------|
|                   |                                     |  | MIN               | TYP                   | MAX  |       |
| V <sub>OUT</sub>  | Output Voltage                      | T <sub>A</sub> = Over Temperature*                 | 4.5               | 5.0                   | 5.5  | V     |
| V <sub>LX1</sub>  | Minimum Input Voltage to LX1        | I <sub>L</sub> = 0μA                               | -                 | 0.9                   | 1.0  | V     |
| V <sub>LX1</sub>  | Minimum Startup Voltage to LX1      | I <sub>L</sub> = 0μA (Note 1)                      | -                 | 0.8                   | 1.15 | V     |
| V <sub>LX2</sub>  | Input Voltage to LX2                |  | -                 | -                     | 5.6  | V     |
| I <sub>LX2</sub>  | Peak LX2 Switch Current             | (Note 1)   | -                 | -                     | 1.5  | A     |
| I <sub>Q</sub>    | Standby Current                     | I <sub>L</sub> = 0μA, CTL = Open                   | -                 | 40                    | -    | μA    |
| f <sub>O</sub>    | Switching Frequency                 | V <sub>BATT</sub> = 2.0 to 3.2V                    | 15.5              | 18                    | 24   | kHz   |
| %ON               | Switch Duty Cycle                   |  | 40                | 50                    | 60   | %     |
| t <sub>ON</sub>   | Switch On Time                      |  | 15                | 28                    | 38   | μs    |
| R <sub>DSON</sub> | LX2 On Resistance                   | (Note 1)   | 0.40              | -                     | 0.67 | Ω     |
| V <sub>LBI</sub>  | Low Battery Input Threshold Voltage |  | 1.12              |                       | 1.18 | V     |
|                   | Low Battery Input Threshold Tempco  |  | -                 | -0.5                  | -    | mV/°C |
| I <sub>LBI</sub>  | Low Battery Input Bias Current      |  | -                 | 0.01                  | 10   | nA    |
| V <sub>LBO</sub>  | Low Battery Output                  | V <sub>LBI</sub> < 1.12V, I <sub>LBO</sub> = 1.6mA | -                 | -                     | 0.4  | V     |
|                   |                                     | V <sub>LBI</sub> > 1.18V, I <sub>LBO</sub> = -1μA  | V <sup>+</sup> -1 | -                     | -    | V     |
| V <sub>PR</sub>   | Power Ready                         | PR High, I <sub>PR</sub> = -1μA                    | -                 | V <sub>OUT</sub> -0.2 | -    | V     |
|                   |                                     | PR Low, I <sub>PR</sub> = 1mA                      | -                 | 0.3                   | -    | V     |
| V <sub>CTL</sub>  | Input Threshold                     |  | -                 | 0.7                   | -    | V     |
|                   | Efficiency                          | 5mA ≤ I <sub>LOAD</sub> ≤ 150mA                    | -                 | 75                    | -    | %     |

NOTE: 1. Not tested, Guaranteed by design and characterization.

\* Commercial Temperature Range = 0°C to +70°C  
Industrial Temperature Range = -40°C to +85°C

**Pin Description**

| ICL646,<br>ICL7646<br>PIN NUMBER | ICL644, ICL7644<br>ICL645, ICL7645<br>ICL647, ICL7647 | NAME      | FUNCTION   |
|----------------------------------|---|-----------|--|
| -                                | 1   | LX2       | Output drain of high power N-channel MOS FET.  |
| 1                                | -   | VCC       | Connect to battery positive terminal.  |
| -                                | 2   | V+        | Output of low power up converter; 10 to 15V in high power mode. 4.5V to 5.5V in standby mode.  |
| 2                                | -   | V+        | Output of low power up converter. 10 to 15V in high power mode. 2.6 to 3.6V in standby mode.   |
| 3                                | 3   | I/C       | Internal Connection. Leave this pin unconnec.ed. "Do not ground."  |
| -                                | 7   | GND       | Low power ground.  |
| 4                                | 4   | VREF      | 1.295V bandgap reference output; should be decoupled with a capacitor to pin 7. This terminal is high impedance and cannot source or sink current. |
| 5                                | 5   | LBO       | Low battery monitor output. Sinks 1.6mA when LBI is less than 1.17V, otherwise sources 1µA from V+.  |
| 6                                | 6   | LBI       | Low battery monitor input. Very high input impedance.  |
| 8*, 14                           | 8*  | NC<br>*SD | No connection. *Shutdown pin on ICL764X series and no connect pin on ICL64X series. Allows user to turn part off by grounding pin 8.               |
| 9                                | 9   | LX1       | Output (drain) of low power N-channel power driver.  |
| 10                               | 10  | OUT       | +5V (+3V on ICL647). Feedback (input) pin for high power operation; output pin in standby mode.  |
| 11                               | 11  | PR        | Power ready output; high (+5V on ICL644, 645, 646; +3V on ICL647) when high power converter is ready to supply power.                              |
| 7                                | 12, 14  | HP, GND   | High power ground.   |
| 13                               | 13  | CTL       | Control mode switch input; open circuit or high for standby mode, ground for high power mode.  |
| 12                               | -   | D         | Driver output to external FET. Output voltage swings from GND to VOUT.   |

**Low Voltage Step-Up Converters**

**Operating Principle**

The ICL644, ICL645, ICL646 and ICL647 are flyback, or boost converters: energy from the battery is first stored in a coil and then discharged to the load. Essentially, the circuit consists of a battery in series with a coil, a high power FET, rectifier, and filter, as shown in Figure 1. When the switch is closed, current builds up in the coil, creating a magnetic field. During the second half, or flyback part of the cycle, the power FET opens, the magnetic field collapses and the voltage across the inductor reverses polarity, adding to the voltage of the battery and discharging through the rectifier into the load.

The switch is controlled by a constant frequency oscillator whose output is gated on and off by a comparator that monitors the output voltage. When the output voltage is above the comparator threshold, the power FET skips an entire cycle of the oscillator. This pulse skipping technique varies the average duty cycle to achieve regulation, rather than varying the period or duty cycle of each cycle of the power FET; it eliminates a number of linear circuits that would otherwise add both circuit complexity and quiescent operating current.

The key to operating CMOS circuitry from a 1V supply depends on a technique called bootstrapping. A specially designed oscillator starts itself up on a very low voltage and builds up (or bootstraps) a higher voltage that in turn is used as the supply for further operation. This supply yields higher efficiency because the bootstrapped voltage drives the gate of the internal power FET transistor to lower on resistance.

When power is first applied, the circuit is very inefficient (for the first cycle) until a higher voltage is generated on the flyback half of the first cycle. This higher voltage is rectified and filtered, and powers the whole IC (and thus the oscillator) for the next cycle. Since each cycle generates a higher voltage for the next cycle, the voltage builds up very rapidly. An internal regulator limits the voltage to about 12V. The load for this supply is only the CMOS chip itself, so the requirements for the components, particularly the external inductor L1, are very broad. This voltage is brought out to the V+ pin and is connected to a tantalum capacitor for filtering.

This bootstrapped 12V drives an internal N-channel power FET that furnishes the switching power for the load. Since the gate of this FET is driven from a 12V supply, it has a very low on resistance and can efficiently switch high currents through a second inductor, L2. It is the power stored in this second inductor that is delivered to the 5V load via an external Schottky diode. The rectified and filtered 5V output is connected back to the OUT pin to provide feedback. The ICL644/645/646/647 thus has two separate switching circuits and uses two separate inductors.

**Circuit Details**

A typical application circuit is shown in Figure 2. The higher value inductor, L1, is typically 4.7mH, and may have fairly high losses. It is used for the low power section of the circuit and is rectified by an internal diode and routed to pin 2, V+, where it is filtered by an external capacitor, C1. The second inductor, L2, varies from 39µH to 500µH, depending on input voltage and load current. It must have low series resistance and sufficient core material to handle the load power without saturating. The inductor is connected to pin 1 (LX2), the drain of the Low Power FET, and is rectified by an external Schottky diode, D1, and filtered by an external capacitor, C2. This is the main +5V output (+3V on the ICL647), and it is connected to OUT, pin 10, which is the feedback input in high power mode. Figure 3 shows a similar circuit for the ICL646 using an external FET for higher power output.

**Low Power Standby Mode**

A control pin (CTL) is available for putting the device into standby mode to conserve power. When this pin is held low, the IC operates in the high power mode, if it is driven high or left open the following occurs: the POWER READY (PR) pin is driven low, the high power FET is gated off, the 12V (V+) switching supply is reduced to 5V (+3V on the ICL647) and is connected to the V<sub>OUT</sub> pin.

By lowering the internal 12V supply to 5V, the leakage currents of the CMOS circuits and the losses associated with its voltage reference and oscillator are reduced to a minimum. The internal low power 5V supply can furnish up to 500µA, and it is connected to the normal 5V output pin (OUT) to supply current to the load, keeping alive standby circuits.

**Power Ready Output Pin**

During initial start up (and when placed in standby mode), the ICL644/645/646/647 internal voltages are too low to drive the power FET efficiently. A separate comparator determines when this voltage has reached a high enough value to drive the FET. The output of this comparator gates the FET drive voltage. This scheme extends battery life in standby mode and prevents the power FET from stalling when switching to high power mode. The comparator output is also brought out to the POWER READY (PR) pin and can be used to control external circuits, further reducing battery drain.

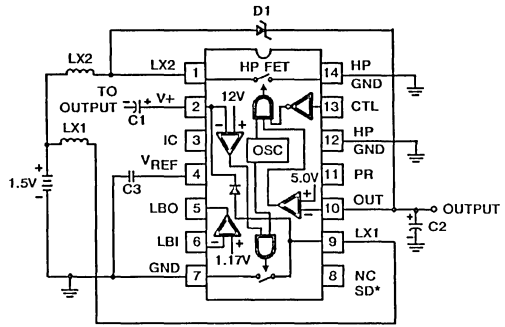


FIGURE 1. ICL644/645 BLOCK DIAGRAM

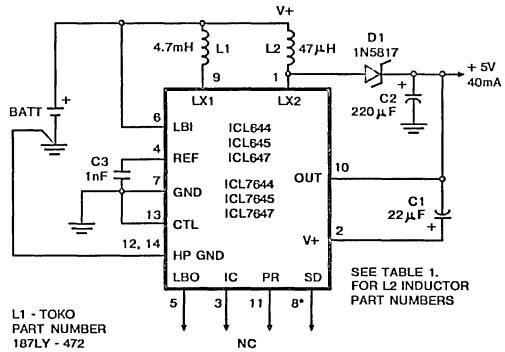


FIGURE 2. ICL64X/764X TYPICAL APPLICATION

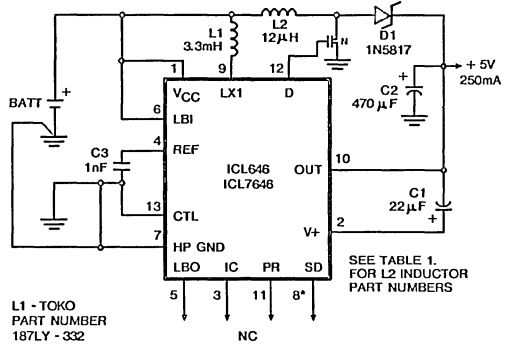


FIGURE 3. ICL646/7646 TYPICAL APPLICATION

POWER PROCESSING CIRCUITS

**Start Up and Mode Considerations**

The ICL644/645/646/647 may be started up in either the low power (standby) or high power mode. When starting in the high power mode, both the low power switch and the high power switch start immediately. Whether or not the load is connected, the output voltage will rise to 5V in the first few cycles. The OUT pin becomes an input for feedback to control regulation.

If the high power load (greater than about 500µA) is connected to the OUT pin and the device is placed in the low power mode (CTL pin driven high or left open), the low power oscillator will have to furnish all of the 5V power via the OUT pin, and the low power oscillator will stall. **It is, therefore, important to disconnect any load currents (greater than 500µA) whenever the low power or standby mode is selected.** The POWER READY (PR) pin may be used to disconnect the load via an external transistor. This way the mode and connection of the high power load are both controlled through the CTL input.

**Input Filtering**

It is important to limit the rate of rise of the battery voltage when the circuit is first turned on with a mechanical switch or the installation of the battery(ies). A simple R-C network made up of the battery internal resistance and a 10µF tantalum capacitor placed at the battery side of L2 input is sufficient for this purpose. This capacitor also helps to absorb the (relatively) high peak currents that are drawn from the battery in the high power mode.

**Output Filtering**

It is also important to limit the speed at which V+ decreases to 5V when the mode is switched from high power to standby. This is accomplished by putting a 22µF capacitor between the V+ and OUT pins. Also, a 220µF capacitor placed on the OUT pin provides both filtering and serves to hold up the 5V during the switchover period. Without these capacitors, the 5V may spike negatively during the switchover.

**Low Battery Function**

A completely independent low battery monitor is built into the ICL64X series and the ICL764X series. Its input (LBI) is the + input of a CMOS comparator whose - input is connected to the internal 1.17V band-gap reference. This input can be connected directly to the battery in single cell circuits or connected to a high resistance voltage divider for higher voltage monitoring. The output (LBO) can sink 1.6mA or source several microamperes from V+.

**Shutdown Function**

The ICL764X series is equipped with a shutdown feature. Pin 8, a no connect pin on ICL64X series, is used to power the part down. During shutdown the part draws less than 5µA quiescent current. The part can be shutdown by grounding pin 8. When pin 8 is left floating the part is identical to the ICL64X series.

**Inductor Selection**

**Low Power Coil**

The choice of the low power inductor, L1, is not critical. A 4.7mH coil with a DC resistance of less than 40Ω is adequate for most applications. In general, higher inductance values allow lower start up voltages, while lower resistances yield lower quiescent current in standby mode. If the inductance is made too high, the low power (V+) output voltage and current are reduced. This in turn reduces the efficiency of the power section, so the +5V output (in standby mode) supplied less current. Lower values of inductance raise the minimum start up voltage.

**High Power Coil**

The high power coil, L2, must store most of the energy that flows into the load. Accordingly, it should have a powdered iron or ferrite core and should have low resistance to minimize losses. It also must have an adequate current rating to prevent saturation.

Calculating the worst case inductor for the high power section (LX2) of the ICL644/645/646/647 is a two step process:

1. Determine the smallest inductor value that will not cause the circuit to exceed the peak current rating of the ICL644/645/647 with the highest expected input voltage (VINMAX), the longest on time (tONMAX), and the lowest total resistance (R(MIN)). R(MIN) is the sum of the minimum coil and FET resistances. Note that this peak current relates to the inductor and the FET switch and is several times the load current.

The following example assumes the minimum frequency fO(MIN) and the maximum %ON(MAX) for the calculation of tON(MAX). Although the calculated value for tON(MAX) is above that specified in the electrical characteristics table (49µs), the illustration is still a valid one that yields a worst case minimum inductor value.

NOTE: Units with both fO(MIN) and %ON(MAX) values near the ends of the allowed distributions will be rejected for tON(MAX).

From the Electrical Characteristics table:

- IPK LX2 = 1.5A
- RDSON(MIN) = 0.4Ω
- fO(MIN) = 15.500Hz
- Duty Cycle Maximum, %ON(MAX) = 0.8

then:

$$t_{ON(MAX)} = \%ON(MAX)/f_{O(MIN)} = 0.8/15500 = 51.6\mu s$$

Assume that the minimum coil resistance, RCOIL(MIN) is:

$$R_{COIL(MIN)} = 0.1\Omega$$

The minimum total resistance, R(MIN) is:

$$R(MIN) = R_{DS(on)(MIN)} + R_{COIL(MIN)} = 0.4 + 0.1 = 0.5\Omega$$

then:

$$I_{PK} = 1.5A = \frac{V_{IN(MAX)}}{R_{(MIN)}} \times \left[ 1 - e^{-R_{(MIN)} \times t_{ON(MAX)}/L_{(MIN)}} \right]$$

or:

$$L_{(MIN)} (\mu H) = \frac{-R_{(MIN)} t_{ON(MAX)}}{\ln \left[ \frac{1 - R_{(MIN)} \times I_{PK}/V_{IN(MAX)}}{1} \right]}$$

For a maximum input voltage of 1.56V (single alkaline cell), and a minimum coil resistance of 0.1Ω, the minimum permissible inductance for the ICL644/645/647 is 39.37μH.

2. Having determined the minimum inductance ( $L_{(MIN)}$ ) that keeps the peak current below the individual component ratings, we next calculate a new peak current ( $I'_{PK}$ ) using the highest resistance ( $R_{(MAX)}$ ), the lowest input voltage ( $V_{IN(MIN)}$ ) and the shortest on time ( $t_{ON(MIN)}$ ). Using these parameters, we will calculate the minimum available output (DC) current.

From the Electrical Characteristics table:

$$R_{DSON(MAX)} = 0.67\Omega$$

$$f_{O(MAX)} = 24kHz$$

$$\text{Duty Cycle Minimum, } \%ON_{(MIN)} = 0.66$$

then:

$$t_{ON(MIN)} = \%ON_{(MIN)}/f_{O(MAX)} = 0.66/24000 = 27.5\mu s$$

Assume that the maximum coil resistance,  $R_{COIL(MAX)}$  is:

$$R_{COIL(MAX)} = 0.15\Omega$$

The maximum total charging resistance,  $R_{(MAX)}$  is:

$$R_{(MAX)} = R_{DSON(MAX)} + R_{COIL(MAX)} = 0.82\Omega$$

At the end of the ON period:

$$I'_{PK} = \frac{V_{IN(MIN)}}{R_{(MAX)}} \times 1 - e^{-R_{(MAX)} \times t_{ON(MIN)}/L_{(MIN)}}$$

The energy stored in the coil is:

$$E_{COIL} = \frac{L_{(MIN)} \times I'_{PK}{}^2}{2}$$

And the power put into the coil is:

$$\begin{aligned} P_{COIL} &= f_{O(MAX)} \times E_{COIL} \\ &= \frac{L_{(MIN)} \times I'_{PK}{}^2 \times f_{O(MAX)}}{2} \end{aligned}$$

The minimum DC output current,  $I_{OUT}$ , is:

$$\begin{aligned} I_{OUT(MIN)} &= \frac{P_{LOAD}}{V_{LOAD}} = \frac{P_{COIL} - P_{LOSS}}{V_{OUT(MAX)} + V_{DIODE} - V_{IN(MIN)}} = \\ &= \frac{P_{COIL} - I'_{PK}{}^2 \times (R_{COIL(MAX)}/3) \times (1 - \%ON_{(MIN)})}{V_{OUT(MAX)} + V_{DIODE} - V_{IN(MIN)}} \end{aligned}$$

Using a  $47 \pm 10\%$  μH coil with a resistance of 0.15Ω, an input voltage of 1.1V, and the worst case highest output voltage of 5.5V. The calculated minimum DC output current is 32mA. This assumes a 0.3V forward drop in the 1N5818 diode.

When selecting a coil, care should be exercised to insure that the minimum inductance value, including all the manufacturing tolerances, is never lower than the calculated inductance, or the peak current rating of LX2 may be exceeded. In addition, the current rating of the coil should be greater than the peak current used in the calculation (1.5A, normally), to avoid saturating the core.

If the worst case output current is too small, then either the minimum input voltage must be increased or the maximum input voltage should be decreased. It is always desirable to decrease the ratio between maximum and minimum input voltages. The coil resistance also has a significant effect on the output current, so selecting a lower coil resistance will increase the output current and increase the overall efficiency.

If no satisfactory value of inductance can be found for the desired current, the ICL646 may be used with an external FET whose peak current exceeds 1.5A. The calculations are similar for the ICL644 except the external FETs  $R_{DSON}$  and current rating should be substituted in the above equations.

If the worst case output current is significantly higher than the required load current, a higher inductance value may be used. This will tend to reduce the peak current and the ripple voltage. Be sure to adjust the coil resistance and recalculate all the values.

When the maximum battery voltage exceeds 1.65V, the ICL645 should be used. Calculations for the ICL645 are identical to the ICL644 calculations, except that different values must be used for the maximum and minimum duty cycles.

In general, if a choice of batteries is available, higher input voltages are preferred for two reasons. First, as the input voltage approaches 1V, the load on the battery increases while the losses increase. The losses become so dominant that efficiency suffers and little output current can be maintained. Second, certain losses, such as the coil resistance and the FET on resistance are less significant with higher input voltages. This means not only higher efficiency, but a greater range of input voltages are tolerable; this in turn means that more of the chemical energy can be converted into electricity. For example, three NiCd cells, with a fully charged voltage of 4.05V, may still be used down to 1.1V (with about 5mA of 5V output current), far beyond the normal life expectancy.

The inductance values for commonly encountered battery operated power supplies are tabulated in Table 1.



TABLE 1. MINIMUM INDUCTANCE FOR COMMON BATTERIES

| BATTERY TYPE          | BATTERY VOLTAGE |       | OUTPUT |       | COIL SPECIFICATIONS (L2)<br>TOKO 8RBS 262LYF SERIES |       |          |
|-----------------------|-----------------|-------|--------|-------|---|-------|----------|
|                       | MIN             | MAX   |        |       | μH*   | OHMS  | PART NO. |
| 1 NiCads (ICL644)     | 1.15V           | 1.35V | 5V     | 43mA  | 39  | 0.09  | -0087K   |
| 1 Alkaline (ICL644)   | 1.20V           | 1.55V | 5V     | 43mA  | 47  | 0.10  | -0088K   |
| 1 Alkaline (ICL644)   | 2.5V            | 3.5V  | 5V     | 150mA | 33  | 0.80  | -0086K   |
| 2 NiCads (ICL645)     | 2.30V           | 2.70V | 5V     | 64mA  | 68  | 0.16  | -0090K   |
| 2 Alkalines (ICL645)  | 2.40V           | 3.10V | 5V     | 62mA  | 82  | 0.17  | -0091K   |
| 1 Lithium (ICL645)    | 2.60V           | 3.60V | 5V     | 64mA  | 100   | 0.22  | -0092K   |
| 1 NiCad (ICL646)**    | 1.15V           | 1.35V | 5V     | 250mA | 12  | 0.049 | -0081K   |
| 1 Alkaline (ICL646)** | 1.20V           | 1.55V | 5V     | 275mA | 6.8   | 0.037 | -0079M   |
| 1 Alkaline (ICL647)   | 1.20V           | 1.55V | 3V     | 60mA  | 39  | 0.09  | -0087K   |

\* Coils are from Toko. Inductance (μH) is the MINIMUM allowed for the listed battery voltage range (Battery Voltage: MIN, MAX). Lower values are not recommended, except when using the ICL646/7646 converters since they use an external MOSFET. If less current than listed in the Output column is needed, a higher inductance coil will reduce losses. The optimum induct-

ance varies inversely with required output current if all other conditions are unchanged. For example, refer to line 3 and the 10mA output. 120μH supplies this current more efficiently than the 39μH coil of line 2. L2 may also be calculated using the equations in the Inductor Selection Section.

\*\* These ICL646 circuits use an external current switch. Peak switch current is typically 3.5A.

**Capacitor Selection**

The high current fast rise-time pulses associated with switching power supplies demand good grounding and bypassing techniques. The ICL644/645/647 have 3 ground pins to improve grounding. In addition, the internal voltage reference is brought out for connection to an external 1nF capacitor, minimizing noise and modulation on the reference.

The two output voltages, V+ and +5V should be filtered with tantalum capacitors, or other capacitors with low effective series resistance, to minimize transients. If aluminum electrolytic capacitors are used, they should be paralleled with 0.1μF disc ceramics.

**Selecting Low Power Switching Diodes**

The ICL644/645/646/647 use one external diode, and this diode must be a Schottky. A common Schottky type that performs well is the 1N5818.

In applications where standby current must be minimized, the diode's reverse leakage characteristics are especially important. The ICL644/646/647 (40μA for the ICL645) standby current is typically 80μA, while the reverse current of some Schottky rectifiers can exceed this value, particularly at high temperature. If necessary, diode leakage can be reduced with higher voltage Schottky types such as 1N5817. If standby mode is not used or is used only for short periods, then diode leakage is not a significant additional loss compared to the normal load current and need not be considered.

**Rectifier Selection**

The ICL644 - 647 and ICL7644 - 7647 use one external rectifier. To achieve specified performance at low voltage, a Schottky type, such as the 1N5818, is recommended because it combines low forward voltage drop with fast switching speed. This maximizes power conversion efficiency and output current when the DC-DC converter is in high power mode. One drawback of Schottky rectifiers is relatively high reverse leakage current (at 5V reverse, 1N5818 leakage is typically 60μA at 25°C and 450μA at 75°C), which is quite large with respect to the circuit's quiescent current in standby mode (typical standby current ICL644/646/647 and ICL7644/7646/7647: 80μA, ICL645 and ICL7645: 40μA). If standby mode is not used or used only for short periods, reverse leakage is not a significant additional loss compared to the normal load current, and need not be considered.

If quiescent operating current is a primary concern, or if the ICL644 - 647 and ICL7644 - 7647 spends most of its time in standby mode, a silicon rectifier such as the 1N4933 or Unitorde UES1001 may be preferred. Silicon rectifiers have less reverse leakage current than do Schottky rectifiers (1N4933 leakage current is typically 1μA at 25°C and 50μA at 100°C). In circuits where the standby mode is the predominant mode of operation, battery life may be extended by trading conversion efficiency for lower standby quiescent current.

**Output Current vs. Input Voltage**

Figures 4 through 7 show output current versus input voltage using typical inductor values for each part in the ICL644 - 647 and ICL7644 - 7647 series. Where curves end in the middle of the graphs, the peak current limit of the internal LX2 switch has been reached. A higher input voltage than indicated by that line (for the given inductor) may damage the device. Figure 6 assumes that an IRF541 MOSFET is used (0.085Ω maximum on resistance).

Dashed lines indicate regions where the LX2 current limit hasn't been exceeded, but the current rating of the selected coil has. The actual voltages where lines end or become dashed are indicated by arrows on the graphs. The output currents indicated by dashed lines can be achieved only with inductors of higher current rating than the indicated coil. The coils used in Figures 4, 5 and 7 are as follows:

| INDUCTOR | TOKO PART NUMBER |
|----------|------------------|
| 33μH     | -0086K           |
| 47μH     | -0088K           |
| 100μH    | -0092K           |
| 150μH    | -0094K           |
| 220μH    | -0096K           |

The coils used in Figure 6 are the Toko series inductors.

The graphs in Figures 4 - 7 were calculated using worst case data, so individual circuits may supply more current than indicated. If the coils' current ratings are not exceeded, smaller, lower-cost coils than those indicated may be used in low-current applications. Use the equations in the text to calculate worst case peak coil/switch current to be sure that a particular coil's current rating is sufficient.

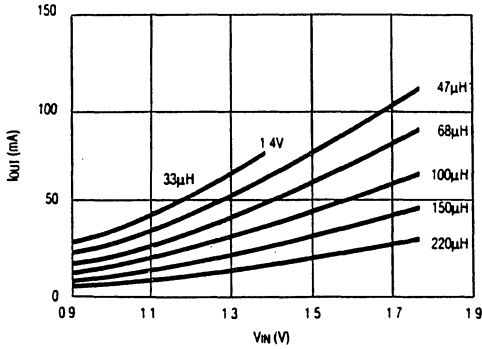


FIGURE 4. ICL644/7644, I<sub>OUT</sub> vs. V<sub>IN</sub> (V<sub>OUT</sub> = 5V)

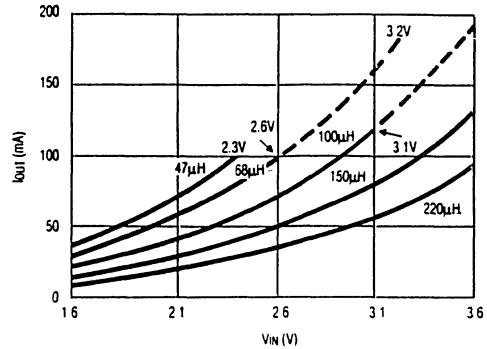


FIGURE 5. ICL645/7645, I<sub>OUT</sub> vs. V<sub>IN</sub> (V<sub>OUT</sub> = 5V)

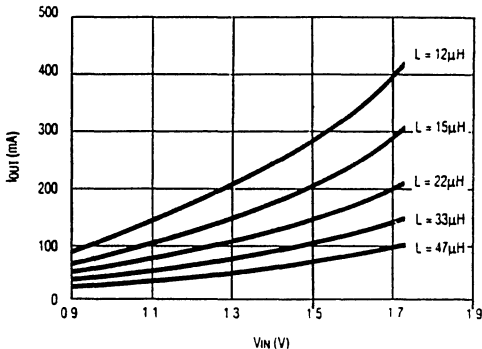


FIGURE 6. ICL646/7646, I<sub>OUT</sub> vs. V<sub>IN</sub> (V<sub>OUT</sub> = 5V)

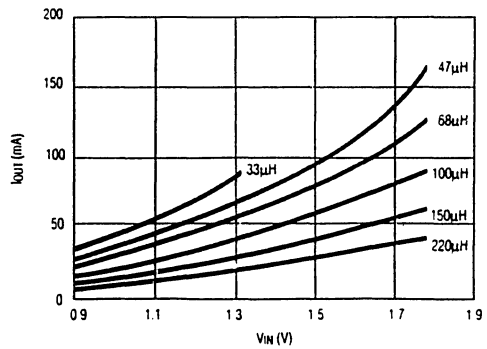


FIGURE 7. ICL647/7647, I<sub>OUT</sub> vs. V<sub>IN</sub> (V<sub>OUT</sub> = 3V)

# ICL7660

## CMOS Voltage Converter

### GENERAL DESCRIPTION

The Harris ICL7660 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The ICL7660 performs supply voltage conversion from positive to negative for an input range of +1.5V to +10.0V, resulting in complementary output voltages of -1.5V to -10.0V. Only 2 non-critical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7660 can also be connected to function as a voltage doubler and will generate output voltages up to +18.6V with a +10V input.

Contained on chip are a series DC power supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. A unique logic element senses the most negative voltage in the device and ensures that the output N-channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5 to +10.0 volts), the LV pin is left floating to prevent device latchup.

**An enhanced direct replacement for this part, the ICL7660S, is now available and should be used for all new designs.**

### FEATURES

- Simple Conversion of +5V Logic Supply to ±5V Supplies
- Simple Voltage Multiplication ( $V_{OUT} = (-) nV_{IN}$ )
- 99.9% Typical Open Circuit Voltage Conversion Efficiency
- 98% Typical Power Efficiency
- Wide Operating Voltage Range 1.5V to 10.0V
- Easy to Use — Requires Only 2 External Non-Critical Passive Components
- No External Diode Over Full Temperature and Voltage Range

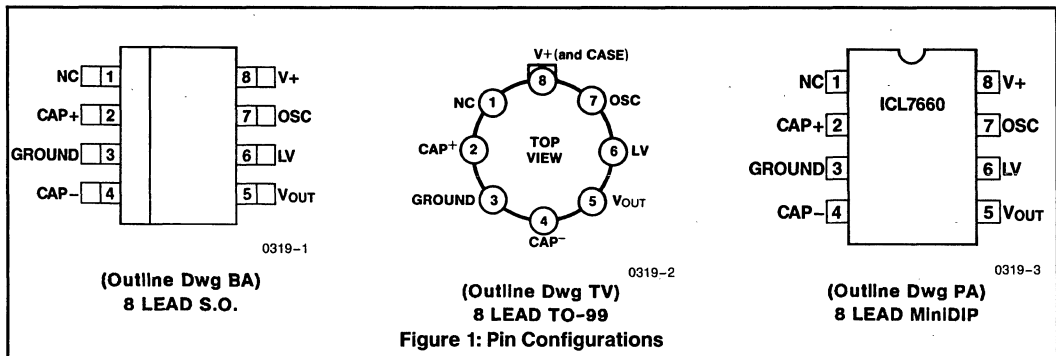
### APPLICATIONS

- On Board Negative Supply for Dynamic RAMs
- Localized  $\mu$ -Processor (8080 Type) Negative Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems

### ORDERING INFORMATION

| Part Number | Temp. Range    | Package        |
|-------------|----------------|----------------|
| ICL7660CTV  | 0° to +70°C    | TO-99          |
| ICL7660CBA  | 0°C to +70°C   | 8 PIN SOIC     |
| ICL7660CPA  | 0° to +70°C    | 8 PIN MINI DIP |
| ICL7660MTV* | -55° to +125°C | TO-99          |

\*Add /883B to part number if 883B processing is required.



# ICL7660

## ABSOLUTE MAXIMUM RATINGS

|   |  |
|---|--|
| Supply Voltage  | 10.5V                                    |
| LV and OSC Input Voltage                                |  |
| (Note 1)  | -0.3V to (V+ + 0.3V) for V+ < 5.5V       |
|   | (V+ - 5.5V) to (V+ + 0.3V) for V+ > 5.5V |
| Current into LV (Note 1)                                | 20 $\mu$ A for V+ > 3.5V                 |
| Output Short Duration (V <sub>SUPPLY</sub> $\leq$ 5.5V) | Continuous                               |
| Power Dissipation (Note 2)                              |  |
| ICL7660CTV  | 500mW                                    |
| ICL7660CPA  | 300mW                                    |
| ICL7660MTV  | 500mW                                    |

|                             |                 |
|-----------------------------|-----------------|
| Operating Temperature Range |                 |
| ICL7660M                    | -55°C to +125°C |
| ICL7660C                    | 0°C to +70°C    |
| Storage Temperature Range   | -65°C to +150°C |
| Lead Temperature            |                 |
| (Soldering, 10sec)          | 300°C           |

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

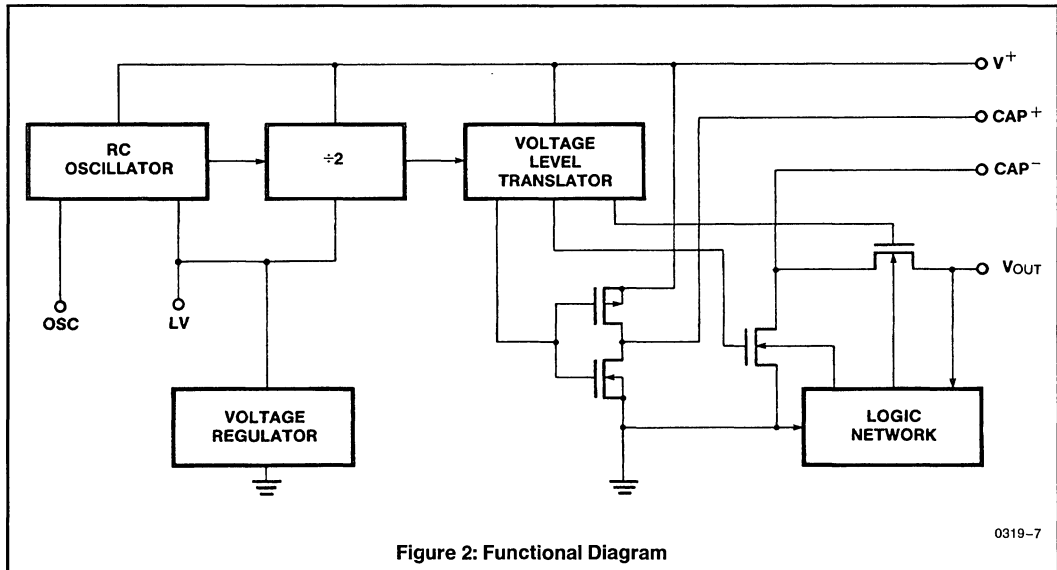


Figure 2: Functional Diagram

2  
POWER PROCESSING  
CIRCUITS

## ELECTRICAL CHARACTERISTICS

V+ = 5V, T<sub>A</sub> = 25°C, C<sub>OSC</sub> = 0, Test Circuit Figure 3 (unless otherwise specified)

| Symbol                      | Parameter                 | Test Conditions  | Limits |     |      | Units   |
|-----------------------------|---------------------------|--|--------|-----|------|---------|
|                             |                           |  | Min    | Typ | Max  |         |
| I+                          | Supply Current            | R <sub>L</sub> = $\infty$  |        | 170 | 500  | $\mu$ A |
| V <sub>L</sub> <sup>+</sup> | Supply Voltage Range - Lo | MIN $\leq$ T <sub>A</sub> $\leq$ MAX, R <sub>L</sub> = 10k $\Omega$ , LV to GROUND | 1.5    |     | 3.5  | V       |
| V <sub>H</sub> <sup>+</sup> | Supply Voltage Range - Hi | MIN $\leq$ T <sub>A</sub> $\leq$ MAX, R <sub>L</sub> = 10k $\Omega$ , LV Open      | 3.0    |     | 10.0 | V       |

NOTE: All typical values have been characterized but are not tested.

## ELECTRICAL CHARACTERISTICS

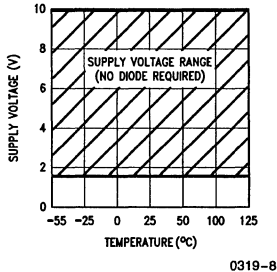
$V^+ = 5V$ ,  $T_A = 25^\circ C$ ,  $C_{OSC} = 0$ , Test Circuit Figure 3 (unless otherwise specified) (Continued)

| Symbol       | Parameter                     | Test Conditions  | Limits |      |     | Units     |
|--------------|-------------------------------|--|--------|------|-----|-----------|
|              |                               |  | Min    | Typ  | Max |           |
| $R_{OUT}$    | Output Source Resistance      | $I_{OUT} = 20mA$ , $T_A = 25^\circ C$  |        | 55   | 100 | $\Omega$  |
|              |                               | $I_{OUT} = 20mA$ , $0^\circ C \leq T_A \leq +70^\circ C$                                 |        |      | 120 | $\Omega$  |
|              |                               | $I_{OUT} = 20mA$ , $-55^\circ C \leq T_A \leq +125^\circ C$                              |        |      | 150 | $\Omega$  |
|              |                               | $V^+ = 2V$ , $I_{OUT} = 3mA$ , LV to GROUND<br>$0^\circ C \leq T_A \leq +70^\circ C$     |        |      | 300 | $\Omega$  |
|              |                               | $V^+ = 2V$ , $I_{OUT} = 3mA$ , LV to GROUND,<br>$-55^\circ C \leq T_A \leq +125^\circ C$ |        |      | 400 | $\Omega$  |
| $f_{OSC}$    | Oscillator Frequency          |  | 10     |      | kHz |           |
| $P_{Ef}$     | Power Efficiency              | $R_L = 5k\Omega$   | 95     | 98   |     | %         |
| $V_{OUT Ef}$ | Voltage Conversion Efficiency | $R_L = \infty$   | 97     | 99.9 |     | %         |
| $Z_{OSC}$    | Oscillator Impedance          | $V^+ = 2$ Volts  |        | 1.0  |     | $M\Omega$ |
|              |                               | $V = 5$ Volts  |        | 100  |     | $k\Omega$ |

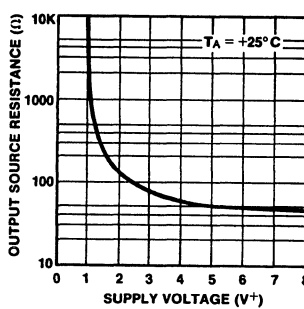
- Notes: 1. Connecting any input terminal to voltages greater than  $V^+$  or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the ICL7660.  
2. Derate linearly above  $50^\circ C$  by  $5.5mW/^\circ C$ .

## TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 3)

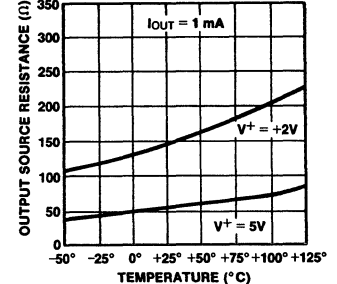
OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE



OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



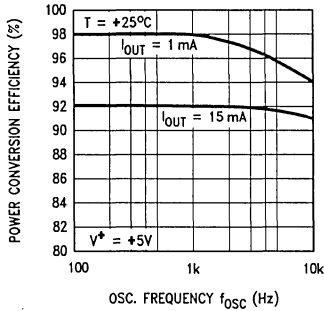
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE



NOTE: All typical values have been characterized but are not tested.

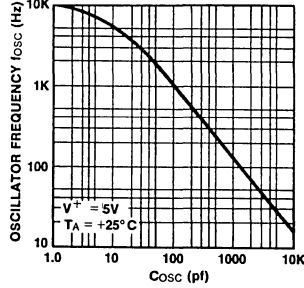
## TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 3) (Continued)

**POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSC. FREQUENCY**



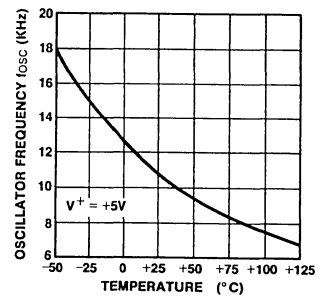
0319-11

**FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE**



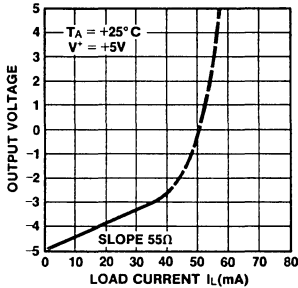
0319-12

**UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE**



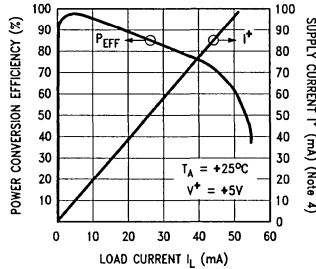
0319-13

**OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT**



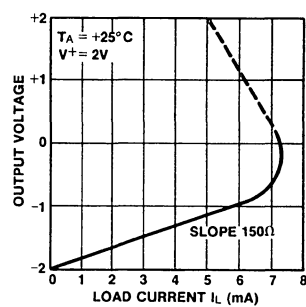
0319-14

**SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT**



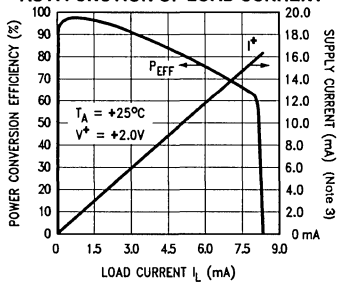
0319-15

**OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT**



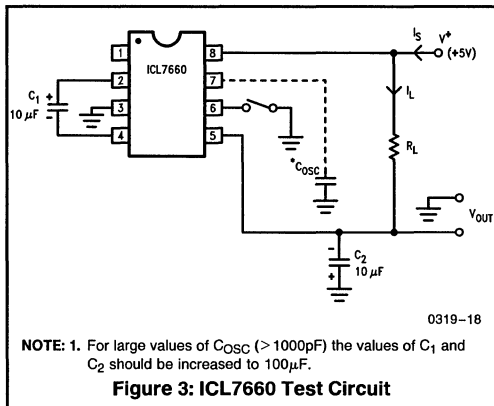
0319-16

**SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT**



0319-17

**NOTE 3.** These curves include in the supply current that current fed directly into the load  $R_L$  from  $V^+$  (See Figure 3). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7660, to the negative side of the load. Ideally,  $V_{OUT} \approx 2 V_{IN}$ ,  $I_S \approx 2 I_L$ , so  $V_{IN} \times I_S \approx V_{OUT} \times I_L$ .



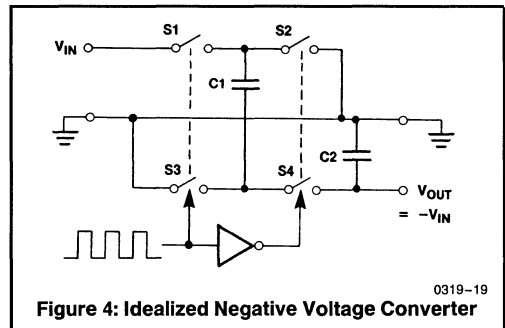
## DETAILED DESCRIPTION

The ICL7660 contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive  $10\mu\text{F}$  polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 4, which shows an idealized negative voltage converter. Capacitor  $C_1$  is charged to a voltage,  $V^+$ , for the half cycle when switches  $S_1$  and  $S_3$  are closed. (Note: Switches  $S_2$  and  $S_4$  are open during this half cycle.) During the second half cycle of operation, switches  $S_2$  and  $S_4$  are closed, with  $S_1$  and  $S_3$  open, thereby shifting capacitor  $C_1$  negatively by  $V^+$  volts. Charge is then transferred from  $C_1$  to  $C_2$  such that the voltage on  $C_2$  is exactly  $V^+$ , assuming ideal switches and no load on  $C_2$ . The ICL7660 approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7660, the 4 switches of Figure 4 are MOS power switches;  $S_1$  is a P-channel device and  $S_2$ ,  $S_3$  &  $S_4$  are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of  $S_3$  &  $S_4$  must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions ( $V_{OUT} = V^+$ ), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7660 by a logic network which senses the output voltage ( $V_{OUT}$ ) together with the level translators, and switches the substrates of  $S_3$  &  $S_4$  to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7660 is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.



## THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory a voltage converter can approach 100% efficiency if certain conditions are met:

- A The drive circuitry consumes minimal power.
- B The output switches have extremely low ON resistance and virtually no offset.
- C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660 approaches these conditions for negative voltage conversion if large values of  $C_1$  and  $C_2$  are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

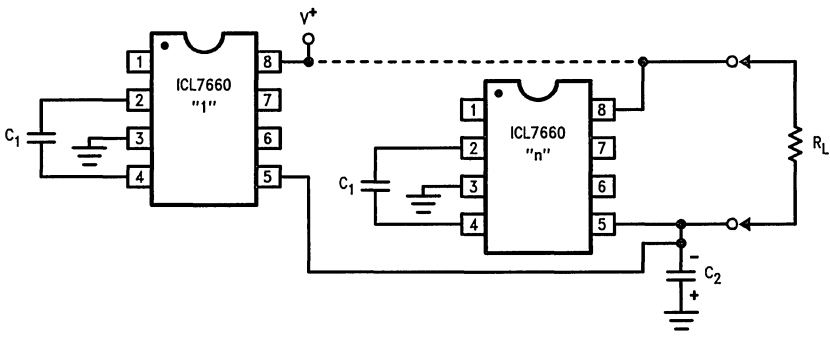
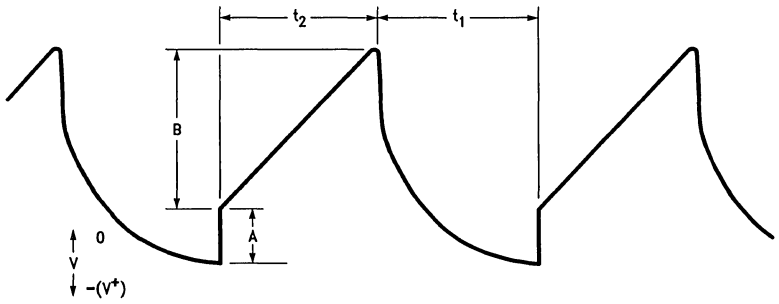
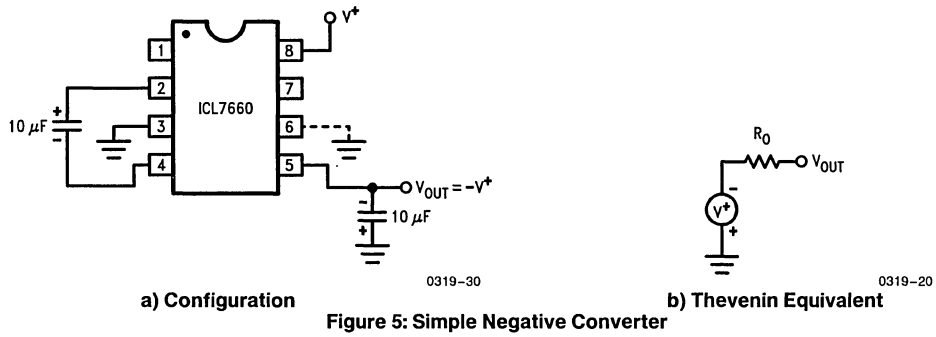
$$E = \frac{1}{2} C_1 (V_1^2 - V_2^2)$$

where  $V_1$  and  $V_2$  are the voltages on  $C_1$  during the pump and transfer cycles. If the impedances of  $C_1$  and  $C_2$  are relatively high at the pump frequency (refer to Figure 4) compared to the value of  $R_L$ , there will be a substantial difference in the voltages  $V_1$  and  $V_2$ . Therefore it is not only desirable to make  $C_2$  as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for  $C_1$  in order to achieve maximum efficiency of operation.

## DO'S AND DON'TS

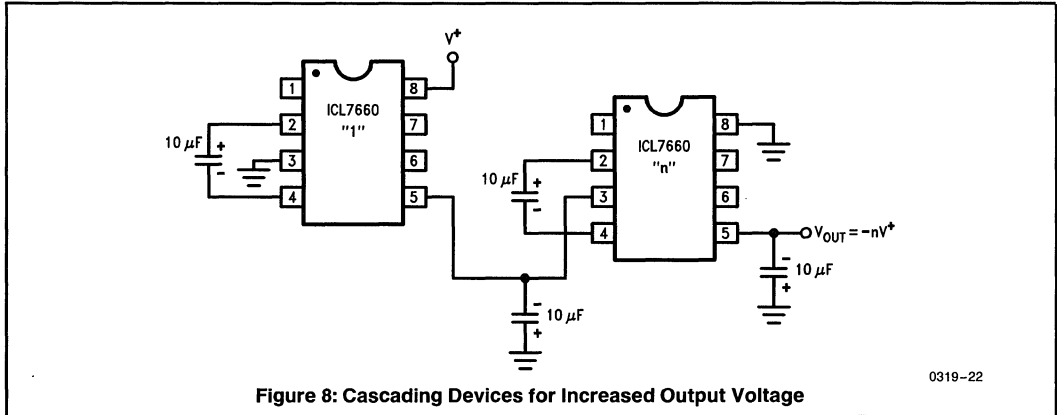
1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 3.5 volts.
3. Do not short circuit the output to  $V^+$  supply for supply voltages above 5.5 volts for extended periods, however, transient conditions including startup are okay.
4. When using polarized capacitors, the + terminal of  $C_1$  must be connected to pin 2 of the ICL7660 and the + terminal of  $C_2$  must be connected to GROUND.
5. If the voltage supply driving the 7660 has a large source impedance (25 - 30 ohms), then a  $2.2\mu\text{F}$  capacitor from pin 8 to ground may be required to limit rate of rise of input voltage to less than  $2V/\mu\text{s}$ .
6. User should insure that the output (pin 5) does not go more positive than GND (pin 3). Device latch up will occur under these conditions.

A 1N914 or similar diode placed in parallel with  $C_2$  will prevent the device from latching up under these conditions. (Anode pin 5, Cathode pin 6).



NOTE: All typical values have been characterized but are not tested.





**Figure 8: Cascading Devices for Increased Output Voltage**

0319-22

## TYPICAL APPLICATIONS

### Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7660 for generation of negative supply voltages. Figure 5 shows typical connections to provide a negative supply where a positive supply of +1.5V to +10.0 volts is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltages below 3.5 volts.

The output characteristics of the circuit in Figure 5a can be approximated by an ideal voltage source in series with a resistance as shown in Figure 5b. The voltage source has a value of  $-V^+$ . The output impedance ( $R_o$ ) is a function of the ON resistance of the internal MOS switches (shown in Figure 4), the switching frequency, the value of C1 and C2, and the ESR (equivalent series resistance) of C1 and C2. A good first order approximation for  $R_o$  is:

$$R_o \approx 2(R_{SW1} + R_{SW3} + ESR_{C1}) + \frac{2(R_{SW2} + R_{SW4} + ESR_{C1})}{(f_{PUMP} \cdot C1)} + ESR_{C2}$$

$$(f_{PUMP} = \frac{f_{OSC}}{2}, R_{SWX} = \text{MOSFET switch resistance})$$

Combining the four  $R_{SWX}$  terms as  $R_{SW}$ , we see that:

$$R_o \approx 2(R_{SW}) + \frac{1}{(f_{PUMP} \cdot C1)} + 4(ESR_{C1}) + ESR_{C2}$$

$R_{SW}$ , the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs), typically  $23\Omega$  @  $25^\circ\text{C}$  and 5V. Careful selection of C1 and C2 will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the  $1/(f_{PUMP} \cdot C1)$  component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the  $1/(f_{PUMP} \cdot C1)$  term, but may have the side effect of a net increase in output impedance when

$C1 > 10 \mu\text{F}$  and there is no longer enough time to fully charge the capacitors every cycle. In a typical application where  $f_{OSC} = 10 \text{ kHz}$  and  $C = C1 = C2 = 10 \mu\text{F}$ :

$$R_o \approx 2(23) + \frac{1}{(5 \cdot 10^3)(10^{-5})} + 4(ESR_{C1}) + ESR_{C2}$$

$$R_o \approx 46 + 20 + 5(ESR_C)$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low  $1/(f_{PUMP} \cdot C1)$  term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as  $10\Omega$ .

### Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by 2 voltages, A and B, as shown in Figure 101. Segment A is the voltage drop across the ESR of C2 at the instant it goes from being charged by C1 (current flow into C2) to being discharged through the load (current flowing out of C2). The magnitude of this current change is  $2 \cdot I_{out}$ , hence the total drop is  $2 \cdot I_{out} \cdot ESR_{C2}$  volts. Segment B is the voltage change across C2 during time  $t_2$ , the half of the cycle when C2 supplies current to the load. The drop at B is  $I_{out} \cdot t_2 / C2$  volts. The peak-to-peak ripple voltage is the sum of these voltage drops:

$$V_{ripple} \approx \left[ \frac{1}{2(f_{PUMP} \cdot C2)} + 2(ESR_{C2}) \right] I_{out}$$

Again, a low ESR capacitor will result in a higher performance output.

### Paralleling Devices

Any number of ICL7660 voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, C2, serves all devices while each device requires its own pump capacitor, C1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT} \text{ (of ICL7660)}}{n \text{ (number of devices)}}$$

NOTE: All typical values have been characterized but are not tested.

## Cascading Devices

The ICL7660 may be cascaded as shown to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n(V_{IN}),$$

where  $n$  is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660  $R_{OUT}$  values.

## Changing the ICL7660 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 9. In order to prevent possible device latchup, a 100k $\Omega$  resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10k $\Omega$  pullup resistor to  $V^+$  supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be  $1/2$  of the clock frequency. Output transitions occur on the positive-going edge of the clock.

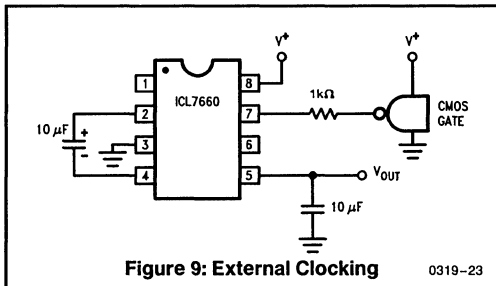


Figure 9: External Clocking

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It is also possible to increase the conversion efficiency of the ICL7660 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 10. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump ( $C_1$ ) and reservoir ( $C_2$ ) capacitors; this is overcome by increasing the values of  $C_1$  and  $C_2$  by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and  $V^+$  will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of  $C_1$  and  $C_2$  (from 10 $\mu$ F to 100 $\mu$ F).

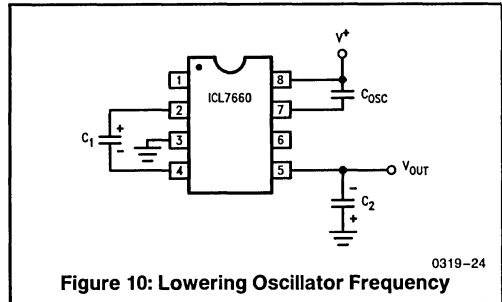


Figure 10: Lowering Oscillator Frequency

0319-24

## Positive Voltage Doubling

The ICL7660 may be employed to achieve positive voltage doubling using the circuit shown in Figure 11. In this application, the pump inverter switches of the ICL7660 are used to charge  $C_1$  to a voltage level of  $V^+ - V_F$  (where  $V^+$  is the supply voltage and  $V_F$  is the forward voltage drop of diode  $D_1$ ). On the transfer cycle, the voltage on  $C_1$  plus the supply voltage ( $V^+$ ) is applied through diode  $D_2$  to capacitor  $C_2$ . The voltage thus created on  $C_2$  becomes  $(2V^+) - (2V_F)$  or twice the supply voltage minus the combined forward voltage drops of diodes  $D_1$  and  $D_2$ .

The source impedance of the output ( $V_{OUT}$ ) will depend on the output current, but for  $V^+ = 5$  volts and an output current of 10mA it will be approximately 60 ohms.

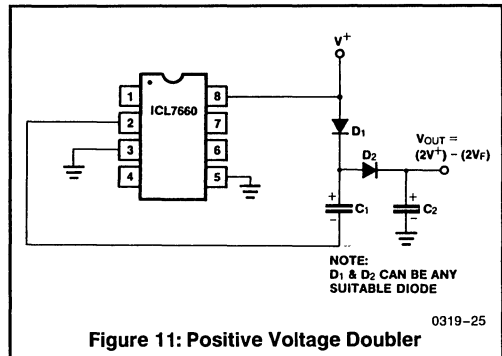


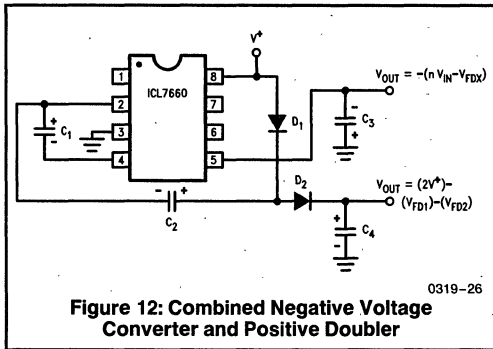
Figure 11: Positive Voltage Doubler

NOTE:  
D<sub>1</sub> & D<sub>2</sub> CAN BE ANY  
SUITABLE DIODE

0319-25

## Combined Negative Voltage Conversion and Positive Supply Doubling

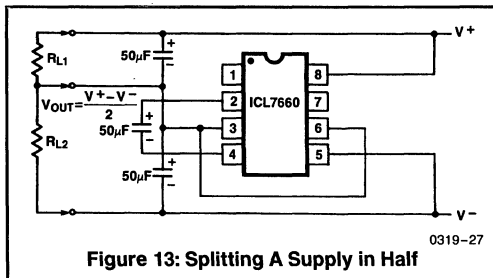
Figure 12 combines the functions shown in Figures 5 and 11 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9 volts and -5 volts from an existing +5 volt supply. In this instance capacitors  $C_1$  and  $C_3$  perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors  $C_2$  and  $C_4$  are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.



**Figure 12: Combined Negative Voltage Converter and Positive Doubler**

## Voltage Splitting

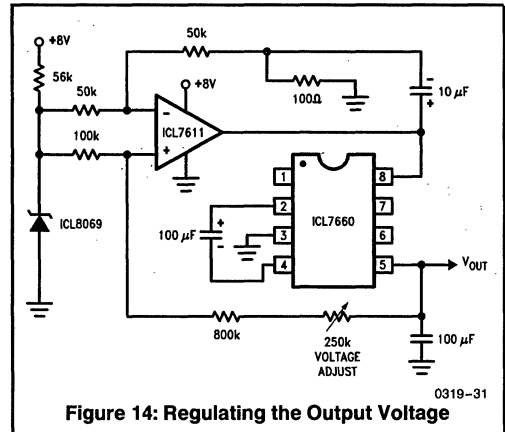
The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 13. The combined load will be evenly shared between the two sides. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 8, +15V can be converted (via +7.5, and -7.5) to a nominal -15V, although with rather high series output resistance ( $\sim 250\Omega$ ).



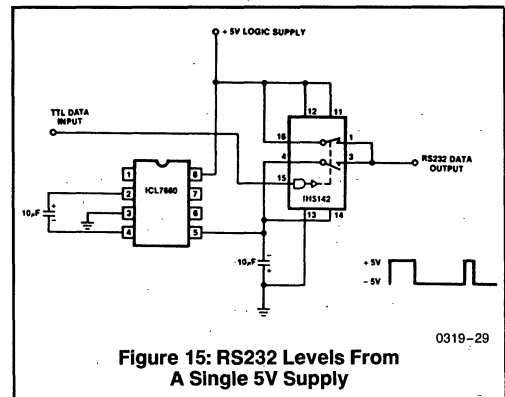
**Figure 13: Splitting A Supply in Half**

## Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7660 can be a problem, particularly if the load current varies substantially. The circuit of Figure 14 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7660's output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the 7660, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than  $5\Omega$  to a load of 10mA.



**Figure 14: Regulating the Output Voltage**



**Figure 15: RS232 Levels From A Single 5V Supply**

## OTHER APPLICATIONS

Further information on the operation and use of the ICL7660 may be found in A051 "Principals and Applications of the ICL7660 CMOS Voltage Converter".

# ICL7660S

## Super Voltage Converter

### GENERAL DESCRIPTION

The ICL7660S Super Voltage Converter is a monolithic CMOS voltage conversion IC that guarantees significant performance advantages over other similar devices. It is a direct replacement for the industry-standard ICL7660 offering an **extended** operating supply voltage range up to 12V, with **lower** supply current. **No external diode** is needed for the ICL7660S. In addition, a **Frequency Boost pin** has been incorporated to enable the user to achieve lower output impedance despite using smaller capacitors. All improvements are highlighted in **bold italics** in the Electrical Characteristics section. **Critical parameters are guaranteed over the entire commercial, industrial and military temperature ranges.**

The ICL7660S performs supply voltage conversion from positive to negative for an input range of 1.5V to 12V, resulting in complementary output voltages of -1.5V to -12V. Only 2 non-critical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7660S can be connected to function as a voltage doubler and will generate up to 22.8V with a 12V input. It can also be used as a voltage multiplier or voltage divider.

The chip contains a series DC power supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. The oscillator, when unloaded, oscillates at a nominal frequency of 10 kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be over-driven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (3.5V to 12V), the LV pin is left floating to prevent device latchup.

### FEATURES

- **Guaranteed Lower Max Supply Current for All Temperature Ranges**
- **Guaranteed Wider Operating Voltage Range —1.5V to 12V**
- **No External Diode Over Full Temperature and Voltage Range**
- **Boost Pin (Pin 1) for Higher Switching Frequency**
- **Guaranteed Minimum Power Efficiency of 96%**
- **Improved Minimum Open Circuit Voltage Conversion Efficiency of 99%**
- **Improved SCR Latchup Protection**
- **Simple Conversion of +5V Logic Supply to ±5V Supplies**
- **Simple Voltage Multiplication  $V_{OUT} = (-)nV_{IN}$**
- **Easy to Use—Requires Only 2 External Non-Critical Passive Components**
- **Improved Direct Replacement for Industry-Standard ICL7660 and Other Second-Source Devices**

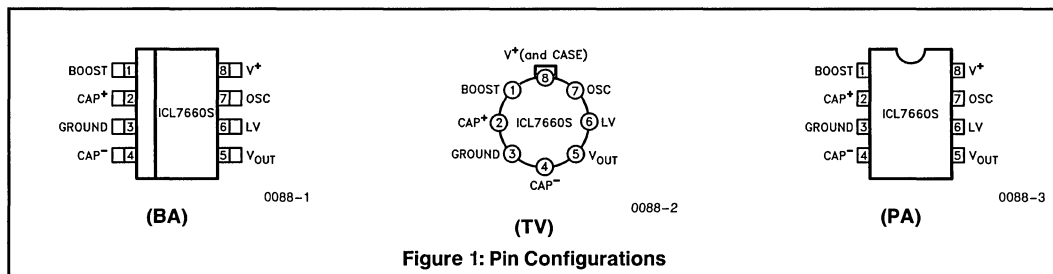
### APPLICATIONS

- **Simple Conversion of +5V to ±5V Supplies**
- **Voltage Multiplication  $V_{OUT} = \pm nV_{IN}$**
- **Negative Supplies for Data Acquisition Systems & Instrumentation**
- **RS232 Power Supplies**
- **Supply Splitter,  $V_{OUT} = \pm V_S/2$**

### ORDERING INFORMATION

| Part Number  | Temp. Range     | Package       |
|--------------|-----------------|---------------|
| ICL7660SCBA  | 0°C to +70°C    | 8-Pin SOIC    |
| ICL7660SCPA  | 0°C to +70°C    | 8-Pin Minidip |
| ICL7660SIBA  | -25°C to +85°C  | 8-Pin SOIC    |
| ICL7660SCTV  | 0°C to +70°C    | TO-99         |
| ICL7660SIPA  | -25°C to +85°C  | 8-Pin Minidip |
| ICL7660SITV  | -25°C to +85°C  | TO-99         |
| ICL7660SMTV* | -55°C to +125°C | TO-99         |

\*Add /883B to part number if 883B processing is required.

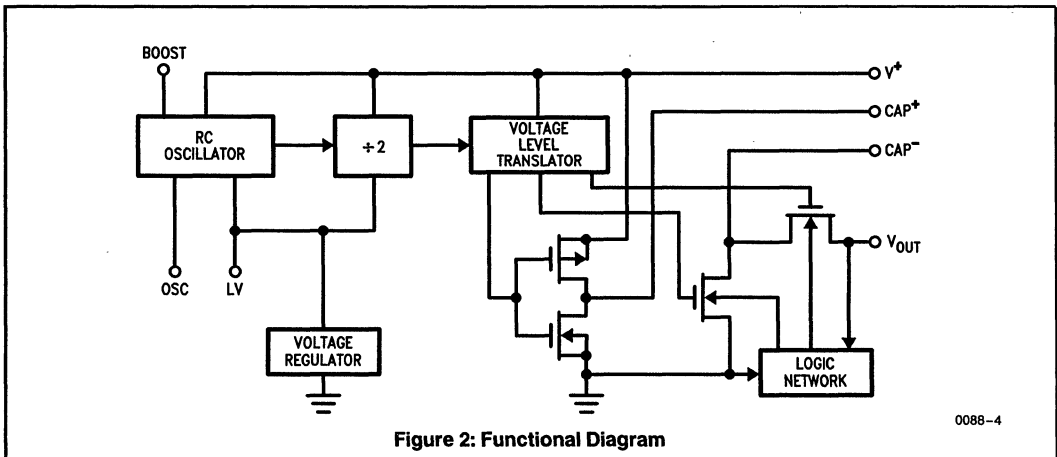


# ICL7660S

## ABSOLUTE MAXIMUM RATINGS

|   |  |
|---|--|
| Supply Voltage .....  | 13.0V  |
| LV and OSC Input Voltage                                      |  |
| (Note 1) .....  | -0.3V to (V <sup>+</sup> + 0.3V) for V <sup>+</sup> < 5.5V                   |
| .....   | (V <sup>+</sup> - 5.5V) to (V <sup>+</sup> + 0.3V) for V <sup>+</sup> > 5.5V |
| Current into LV (Note 1) .....                                | 20 $\mu$ A for V <sup>+</sup> > 3.5V   |
| Output Short Duration (V <sub>SUPPLY</sub> $\leq$ 5.5V) ..... | Continuous   |
| Power Dissipation (Note 2)                                    |  |
| ICL7660SCTV .....   | 500 mW   |
| ICL7660SCPA .....   | 300 mW   |
| ICL7660SCBA .....   | 300 mW   |
| ICL7660SITV .....   | 500 mW   |
| ICL7660SIPA .....   | 300 mW   |
| ICL7660SIBA .....   | 300 mW   |
| ICL7660SMTV .....   | 500 mW   |
| Operating Temperature Range                                   |  |
| ICL7660SM .....   | -55°C to +125°C  |
| ICL7660SI .....   | -25°C to +85°C   |
| ICL7660SC .....   | 0°C to +70°C   |
| Storage Temperature Range .....                               | -65°C to +150°C  |
| Lead Temperature  |  |
| (Soldering, 10 sec) .....                                     | 300°C  |

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



0088-4

*NOTE: All typical values have been characterized but are not tested.*

## ELECTRICAL CHARACTERISTICS

$V^+ = 5V$ ,  $T_A = 25^\circ\text{C}$ , OSC = Free running, Test Circuit Figure 3 (unless otherwise specified)

| Symbol              | Parameter                                  | Test Conditions   | Limits                 |                 |  | Units            |
|---------------------|--|---|------------------------|-----------------|--|------------------|
|                     |  |   | Min                    | Typ             | Max  |                  |
| $I^+$               | <b>Supply Current</b><br>(Note 3)          | $R_L = \infty$ , $25^\circ\text{C}$<br>$0^\circ\text{C} < T_A < +70^\circ\text{C}$<br>$-25^\circ\text{C} < T_A < +85^\circ\text{C}$<br>$-55^\circ\text{C} < T_A < +125^\circ\text{C}$ |                        | <b>80</b>       | <b>160</b><br><b>180</b><br><b>180</b><br><b>200</b> | $\mu\text{A}$    |
| $V_H^+$             | <b>Supply Voltage Range—Hi</b><br>(Note 4) | $R_L = 10\text{K}$ , LV Open<br>$T_{\min} < T_A < T_{\max}$   | 3.0                    |                 | <b>12</b>  | V                |
| $V_L^+$             | Supply Voltage Range—Lo                    | $R_L = 10\text{K}$ , LV to GROUND<br>$T_{\min} < T_A < T_{\max}$  | 1.5                    |                 | 3.5  | V                |
| $R_{OUT}$           | <b>Output Source Resistance</b>            | $I_{OUT} = 20\text{ mA}$ , $T_A = 25^\circ\text{C}$   |                        | 60              | 100  | $\Omega$         |
|                     |  | $I_{OUT} = 20\text{ mA}$ , $0^\circ\text{C} < T_A < +70^\circ\text{C}$  |                        |                 | 120  |                  |
|                     |  | $I_{OUT} = 20\text{ mA}$ , $-25^\circ\text{C} < T_A < +85^\circ\text{C}$  |                        |                 | 120  |                  |
|                     |  | $I_{OUT} = 20\text{ mA}$ , $-55^\circ\text{C} < T_A < +125^\circ\text{C}$   |                        |                 | 150  |                  |
|                     |  | $I_{OUT} = 3\text{ mA}$ , $V^+ = 2\text{V}$ , LV = GND,<br>$0^\circ\text{C} < T_A < +70^\circ\text{C}$  |                        |                 | <b>250</b>   |                  |
|                     |  | $I_{OUT} = 3\text{ mA}$ , $V^+ = 2\text{V}$ , LV = GND,<br>$-25^\circ\text{C} < T_A < +85^\circ\text{C}$  |                        |                 | <b>300</b>   |                  |
|                     |  | $I_{OUT} = 3\text{ mA}$ , $V^+ = 2\text{V}$ , LV = GND,<br>$-55^\circ\text{C} < T_A < +125^\circ\text{C}$   |                        |                 | 400  |                  |
| $f_{OSC}$           | <b>Oscillator Frequency</b>                | $C_{OSC} = 0$ , Pin 1 Open or GND<br>Pin 1 = $V^+$  | <b>5</b>               | 10<br><b>35</b> |  | kHz              |
| $PEff$              | <b>Power Efficiency</b>                    | $R_L = 5\text{ k}\Omega$<br>$T_{\min} < T_A < T_{\max}$   | <b>96</b><br><b>95</b> | 98<br><b>97</b> |  | %                |
| $V_{OUT\text{Eff}}$ | <b>Voltage Conversion Efficiency</b>       | $R_L = \infty$  | <b>99</b>              | 99.9            |  | %                |
| $Z_{OSC}$           | Oscillator Impedance                       | $V^+ = 2\text{V}$   |                        | 1               |  | $\text{M}\Omega$ |
|                     |  | $V^+ = 5\text{V}$   |                        | 100             |  | $\text{k}\Omega$ |

**NOTE 1:** Connecting any terminal to voltages greater than  $V^+$  or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of ICL7660s.

**2:** Derate linearly above  $50^\circ\text{C}$  by  $5.5\text{ mW}/^\circ\text{C}$ .

**3:** In the test circuit, there is no external capacitor applied to pin 7. However, when the device is plugged into a test socket, there is usually a very small but finite stray capacitance present, of the order of  $5\text{ pF}$ .

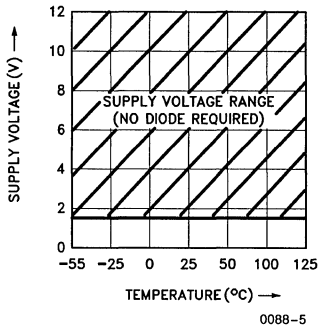
**4:** The Harris ICL7660S can operate without an external diode over the full temperature and voltage range. This device will function in existing designs which incorporate an external diode with no degradation in overall circuit performance.

**5:** All significant improvements over the industry-standard ICL7660 are highlighted in **bold italics**.

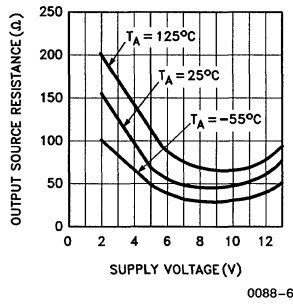
# ICL7660S

## TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 3)

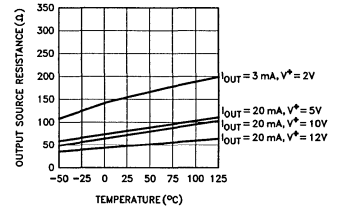
**OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE**



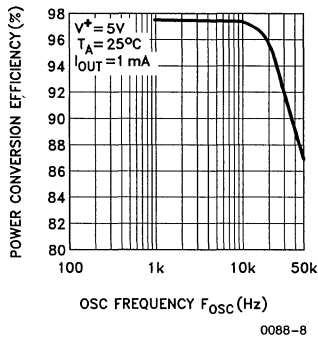
**OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE**



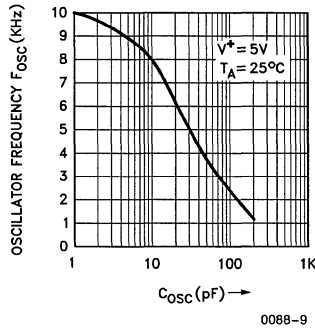
**OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE**



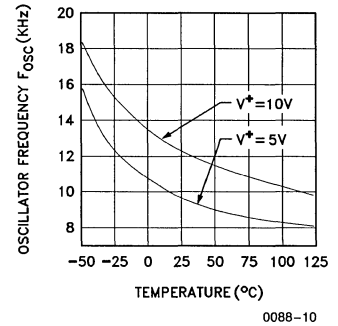
**POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSC. FREQUENCY**



**FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE**



**UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE**

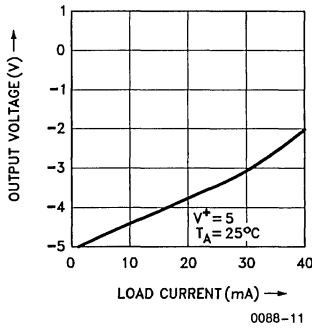


NOTE: All typical values have been characterized but are not tested.

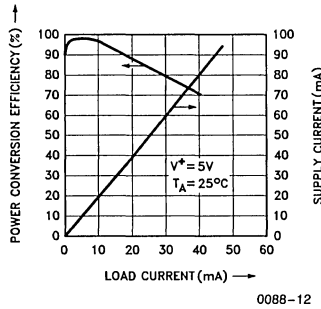
# ICL7660S

## TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 3) (Continued)

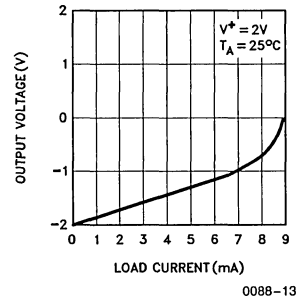
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



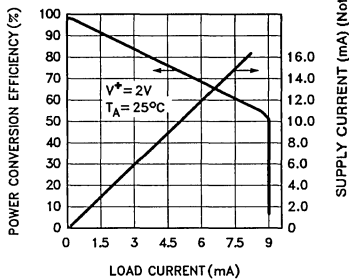
SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



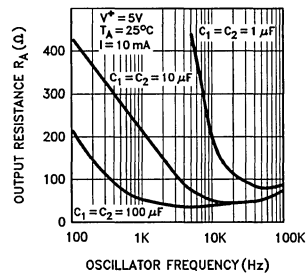
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



OUTPUT SOURCE RESISTANCE AS A FUNCTION OF OSCILLATOR FREQUENCY



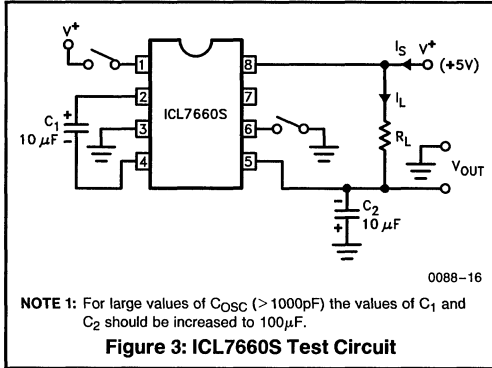
2  
POWER PROCESSING  
CIRCUITS

**NOTE 6:** These curves include in the supply current that current fed directly into the load  $R_L$  from  $V_+$  (see Figure 3). Thus approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7660S, to the negative side of the load. Ideally,  $V_{OUT} \approx 2 V_{IN}$ ,  $I_S \approx 2 I_L$ , so  $V_{IN} \times I_S \approx V_{OUT} \times I_L$ .

NOTE: All typical values have been characterized but are not tested.



# ICL7660S



## DETAILED DESCRIPTION

The ICL7660S contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10μF polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 4, which shows an idealized negative voltage converter. Capacitor C<sub>1</sub> is charged to a voltage, V<sup>+</sup>, for the half cycle when switches S<sub>1</sub> and S<sub>3</sub> are closed. (Note: Switches S<sub>2</sub> and S<sub>4</sub> are open during this half cycle.) During the second half cycle of operation, switches S<sub>2</sub> and S<sub>4</sub> are closed, with S<sub>1</sub> and S<sub>3</sub> open, thereby shifting capacitor C<sub>1</sub> negatively by V<sup>+</sup> volts. Charge is then transferred from C<sub>1</sub> to C<sub>2</sub> such that the voltage on C<sub>2</sub> is exactly V<sup>+</sup>, assuming ideal switches and no load on C<sub>2</sub>. The ICL7660S approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7660S, the 4 switches of Figure 4 are MOS power switches; S<sub>1</sub> is a P-channel device and S<sub>2</sub>, S<sub>3</sub> & S<sub>4</sub> are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S<sub>3</sub> & S<sub>4</sub> must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions (V<sub>OUT</sub> = V<sup>+</sup>), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7660S by a logic network which senses the output voltage (V<sub>OUT</sub>) together with the level translators, and switches the substrates of S<sub>3</sub> & S<sub>4</sub> to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7660S is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

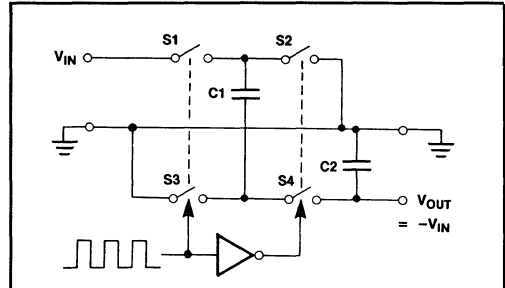


Figure 4: Idealized Negative Voltage Converter

## THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory a voltage converter can approach 100% efficiency if certain conditions are met:

- A The drive circuitry consumes minimal power.
- B The output switches have extremely low ON resistance and virtually no offset.
- C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660S approaches these conditions for negative voltage conversion if large values of C<sub>1</sub> and C<sub>2</sub> are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

$$E = \frac{1}{2} C_1 (V_1^2 - V_2^2)$$

where V<sub>1</sub> and V<sub>2</sub> are the voltages on C<sub>1</sub> during the pump and transfer cycles. If the impedances of C<sub>1</sub> and C<sub>2</sub> are relatively high at the pump frequency (refer to Figure 4) compared to the value of R<sub>L</sub>, there will be a substantial difference in the voltages V<sub>1</sub> and V<sub>2</sub>. Therefore it is not only desirable to make C<sub>2</sub> as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C<sub>1</sub> in order to achieve maximum efficiency of operation.

## DO'S AND DON'TS

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 3.5 volts.
3. Do not short circuit the output to V<sup>+</sup> supply for supply voltages above 5.5 volts for extended periods, however, transient conditions including startup are okay.
4. When using polarized capacitors, the + terminal of C<sub>1</sub> must be connected to pin 2 of the ICL7660 and the + terminal of C<sub>2</sub> must be connected to GROUND.
5. If the voltage supply driving the 7660S has a large source impedance (25 - 30 ohms), then a 2.2μF capacitor from pin 8 to ground may be required to limit rate of rise of input voltage to less than 2V/μs.
6. User should insure that the output (pin 5) does not go more positive than GND (pin 3). Device latch up will occur under these conditions.

A 1N914 or similar diode placed in parallel with C<sub>2</sub> will prevent the device from latching up under these conditions. (Anode pin 5, Cathode pin 6).

NOTE: All typical values have been characterized but are not tested.

# ICL7660S

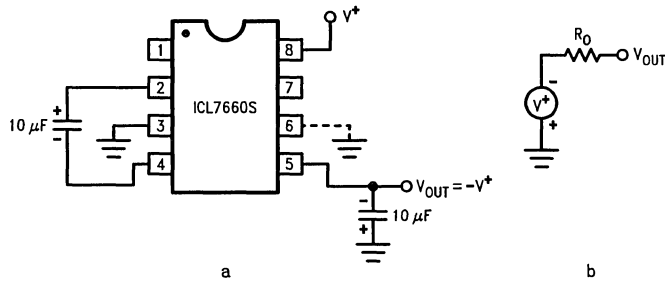


Figure 5: Simple Negative Converter and its Output Equivalent

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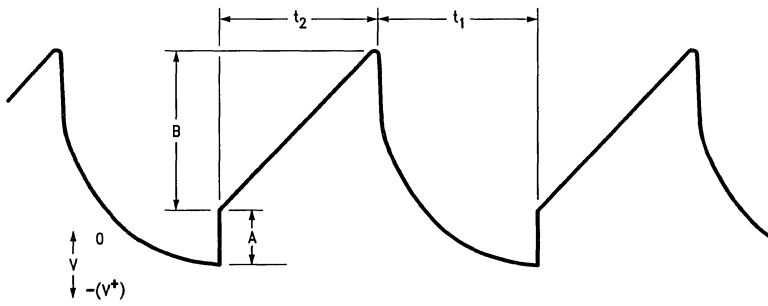


Figure 6: Output Ripple

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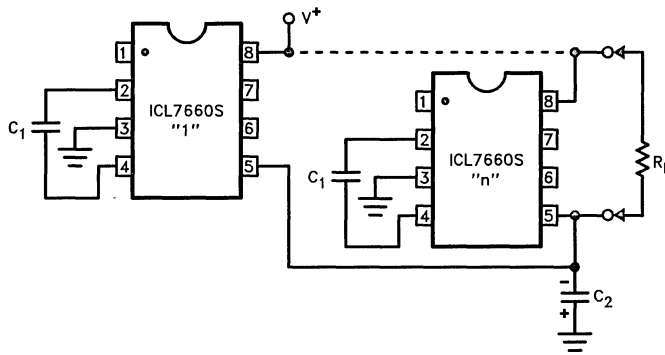
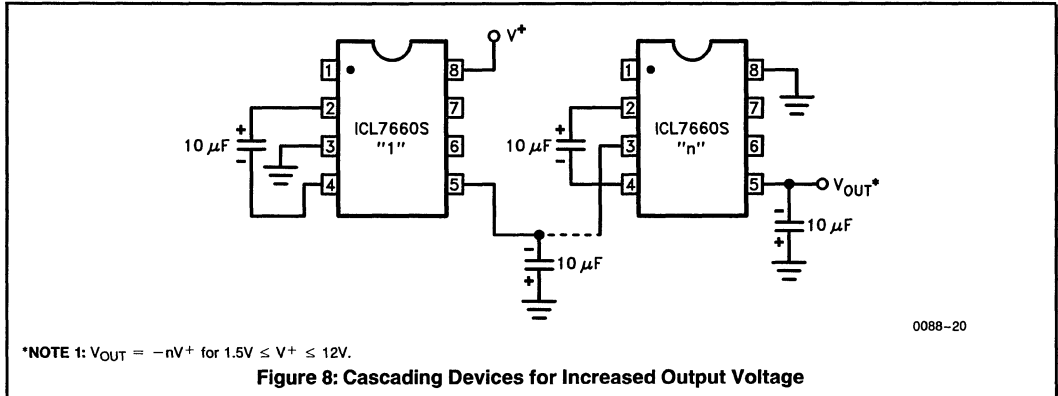


Figure 7: Paralleling Devices

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NOTE: All typical values have been characterized but are not tested.



**Figure 8: Cascading Devices for Increased Output Voltage**

## TYPICAL APPLICATIONS

### Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7660S for generation of negative supply voltages. Figure 5 shows typical connections to provide a negative supply where a positive supply of +1.5V to +12V is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltages below 3.5 volts.

The output characteristics of the circuit in Figure 5a can be approximated by an ideal voltage source in series with a resistance as shown in Figure 5b. The voltage source has a value of  $-(V^+)$ . The output impedance ( $R_o$ ) is a function of the ON resistance of the internal MOS switches (shown in Figure 4), the switching frequency, the value of  $C_1$  and  $C_2$ , and the ESR (equivalent series resistance) of  $C_1$  and  $C_2$ . A good first order approximation for  $R_o$  is:

$$R_o \approx 2(R_{SW1} + R_{SW3} + ESR_{C1}) + 2(R_{SW2} + R_{SW4} + ESR_{C1}) + \frac{1}{f_{PUMP} \times C_1} + ESR_{C2}$$

$$(f_{PUMP} = \frac{f_{OSC}}{2}, R_{SWX} = \text{MOSFET switch resistance})$$

Combining the four  $R_{SWX}$  terms as  $R_{SW}$ , we see that:

$$R_o \approx 2 \times R_{SW} + \frac{1}{f_{PUMP} \times C_1} + 4 \times ESR_{C1} + ESR_{C2} \Omega$$

$R_{SW}$ , the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs), typically  $23\Omega$  @  $25^\circ\text{C}$  and 5V. Careful selection of  $C_1$  and  $C_2$  will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the  $1/(f_{PUMP} \times C_1)$  component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the  $1/(f_{PUMP} \times C_1)$  term, but may have the side effect of a net increase in output impedance when  $C_1 > 10 \mu\text{F}$  and there is no longer enough time to fully charge the capacitors every cycle. In a typical application where  $f_{OSC} = 10 \text{ kHz}$  and  $C = C_1 = C_2 = 10 \mu\text{F}$ :

$$R_o \approx 2 \times 23 + \frac{1}{(5 \times 10^3 \times 10 \times 10^{-6})} + 4 \times ESR_{C1} + ESR_{C2}$$

$$R_o \approx 46 + 20 + 5 \times ESR_C \Omega$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low  $1/(f_{PUMP} \times C_1)$  term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as  $10\Omega$ .

### Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by 2 voltages, A and B, as shown in Figure 6. Segment A is the voltage drop across the ESR of  $C_2$  at the instant it goes from being charged by  $C_1$  (current flowing into  $C_2$ ) to being discharged through the load (current flowing out of  $C_2$ ). The magnitude of this current change is  $2 \times I_{OUT}$ , hence the total drop is  $2 \times I_{OUT} \times ESR_{C2}$  volts. Segment B is the voltage change across  $C_2$  during time  $t_2$ , the half of the cycle when  $C_2$  supplies current to the load. The drop at B is  $I_{OUT} \times t_2 / C_2$  volts. The peak-to-peak ripple voltage is the sum of these voltage drops:

$$V_{ripple} \approx \left( \frac{1}{2 \times f_{PUMP} \times C_2} + 2 \times ESR_{C2} \right) \times I_{OUT}$$

Again, a low ESR capacitor will result in a higher performance output.

### Paralleling Devices

Any number of ICL7660S voltage converters may be paralleled to reduce output resistance. The reservoir capacitor,  $C_2$ , serves all devices while each device requires its own pump capacitor,  $C_1$ . The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT} \text{ (of ICL7660S)}}{n \text{ (number of devices)}}$$

### Cascading Devices

The ICL7660S may be cascaded as shown to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n(V_{IN}),$$

# ICL7660S

where  $n$  is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660S  $R_{OUT}$  values.

## Changing the ICL7660S Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to alter the oscillator frequency. This can be achieved simply by one of several methods described below.

By connecting the Boost Pin (Pin 1) to  $V^+$ , the oscillator charge and discharge current is increased and, hence, the oscillator frequency is increased by approximately  $3\frac{1}{2}$  times. The result is a decrease in the output impedance and ripple. This is of major importance for surface-mount applications where capacitor size and cost are critical. Smaller capacitors, e.g.  $0.1 \mu\text{F}$ , can be used in conjunction with the Boost Pin in order to achieve similar output currents compared to the device free running with  $C_1 = C_2 = 10 \mu\text{F}$  or  $100 \mu\text{F}$ . (Refer to graph of Output Source Resistance as a Function of Oscillator Frequency).

Increasing the oscillator frequency can also be achieved by overdriving the oscillator from an external clock, as shown in Figure 9. In order to prevent device latchup, a  $100 \text{ k}\Omega$  resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a  $10 \text{ k}\Omega$  pullup resistor to  $V^+$  supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be  $\frac{1}{2}$  of the clock frequency. Output transitions occur on the positive-going edge of the clock.

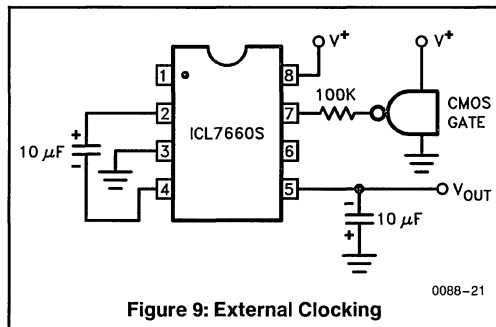


Figure 9: External Clocking

It is also possible to increase the conversion efficiency of the ICL7660S at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 10. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump ( $C_1$ ) and reservoir ( $C_2$ ) capacitors; this is overcome by increasing the values of  $C_1$  and  $C_2$  by the same factor that the frequency has been reduced. For example, the addition of a  $100 \text{ pF}$  capacitor between pin 7 (Osc) and  $V^+$  will lower the oscillator frequency to  $1 \text{ kHz}$  from its nominal frequency of  $10 \text{ kHz}$  (a multiple of 10), and thereby necessitate a corresponding increase in the value of  $C_1$  and  $C_2$  (from  $10 \mu\text{F}$  to  $100 \mu\text{F}$ ).

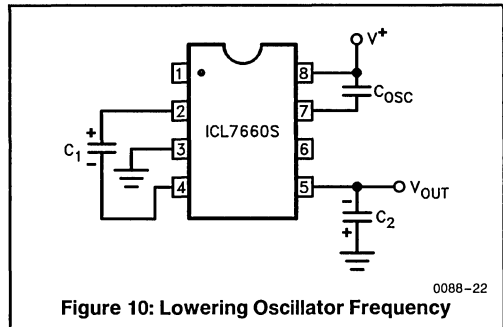
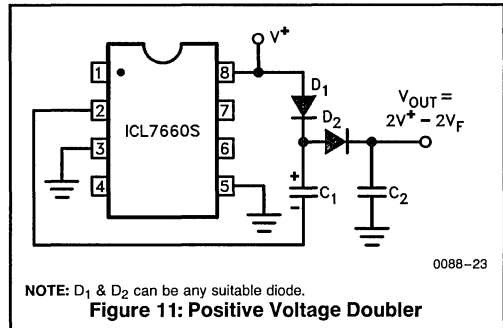


Figure 10: Lowering Oscillator Frequency



NOTE:  $D_1$  &  $D_2$  can be any suitable diode.

Figure 11: Positive Voltage Doubler

## Positive Voltage Doubling

The ICL7660S may be employed to achieve positive voltage doubling using the circuit shown in Figure 11. In this application, the pump inverter switches of the ICL7660S are used to charge  $C_1$  to a voltage level of  $V^+ - V_F$  (where  $V^+$  is the supply voltage and  $V_F$  is the forward voltage drop of diode  $D_1$ ). On the transfer cycle, the voltage on  $C_1$  plus the supply voltage ( $V^+$ ) is applied through diode  $D_2$  to capacitor  $C_2$ . The voltage thus created on  $C_2$  becomes  $(2V^+) - (2V_F)$  or twice the supply voltage minus the combined forward voltage drops of diodes  $D_1$  and  $D_2$ .

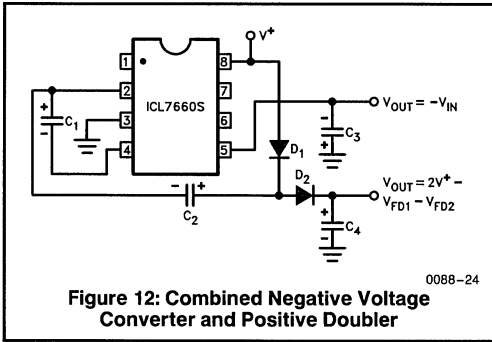
The source impedance of the output ( $V_{OUT}$ ) will depend on the output current, but for  $V^+ = 5 \text{ volts}$  and an output current of  $10 \text{ mA}$  it will be approximately  $60 \text{ ohms}$ .

## Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 12 combines the functions shown in Figures 5 and 11 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating  $+9 \text{ volts}$  and  $-5 \text{ volts}$  from an existing  $+5 \text{ volt}$  supply. In this instance capacitors  $C_1$  and  $C_3$  perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors  $C_2$  and  $C_4$  are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

NOTE: All typical values have been characterized but are not tested.

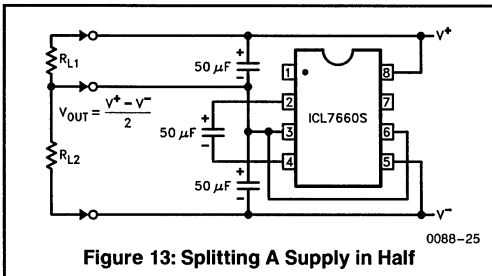
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**Figure 12: Combined Negative Voltage Converter and Positive Doubler**

## Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 13. The combined load will be evenly shared between the two sides, and a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 8, +15V can be converted (via +7.5, and -7.5) to a nominal -15V, although with rather high series output resistance (~250Ω).



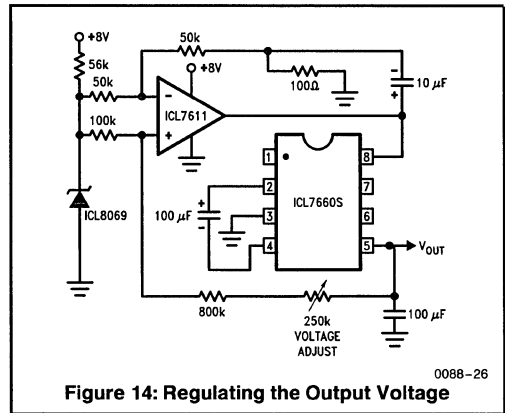
**Figure 13: Splitting A Supply in Half**

## Regulated Negative Voltage Supply

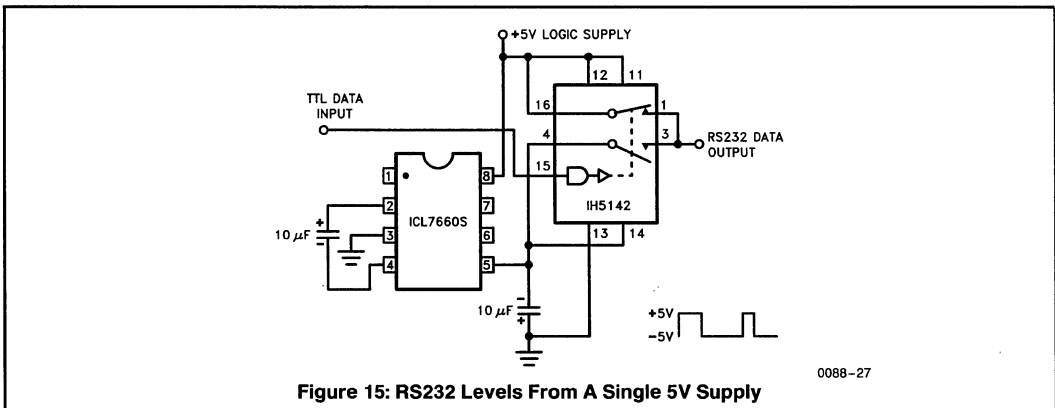
In some cases, the output impedance of the ICL7660S can be a problem, particularly if the load current varies substantially. The circuit of Figure 14 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7660S's output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the 7660S, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.

## OTHER APPLICATIONS

Further information on the operation and use of the ICL7660S may be found in A051 "Principals and Applications of the ICL7660 CMOS Voltage Converter".



**Figure 14: Regulating the Output Voltage**



**Figure 15: RS232 Levels From A Single 5V Supply**

### GENERAL DESCRIPTION

The Harris ICL7662 is a monolithic high-voltage CMOS power supply circuit which offers unique performance advantages over previously available devices. The ICL7662 performs supply voltage conversion from positive to negative for an input range of +4.5V to +20.0V, resulting in complementary output voltages of -4.5V to -20V. Only 2 non-critical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7662 can also function as a voltage doubler, and will generate output voltages up to +38.6V with a +20V input.

Contained on chip are a series DC power supply regulator, RC oscillator, voltage level translator, four output power MOS switches. A unique logic element senses the most negative voltage in the device and ensures that the output N-channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 15.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+10 to +20V), the LV pin is left floating to prevent device latchup.

### FEATURES

- No External Diode Needed Over Entire Temperature Range
- Pin Compatible With ICL7660
- Simple Conversion of +15V Supply to -15V Supply
- Simple Voltage Multiplication ( $V_{OUT} = (-) nV_{IN}$ )
- 99.9% Typical Open Circuit Voltage Conversion Efficiency
- 96% Typical Power Efficiency
- Wide Operating Voltage Range 4.5V to 20.0V
- Easy to Use — Requires Only 2 External Non-Critical Passive Components

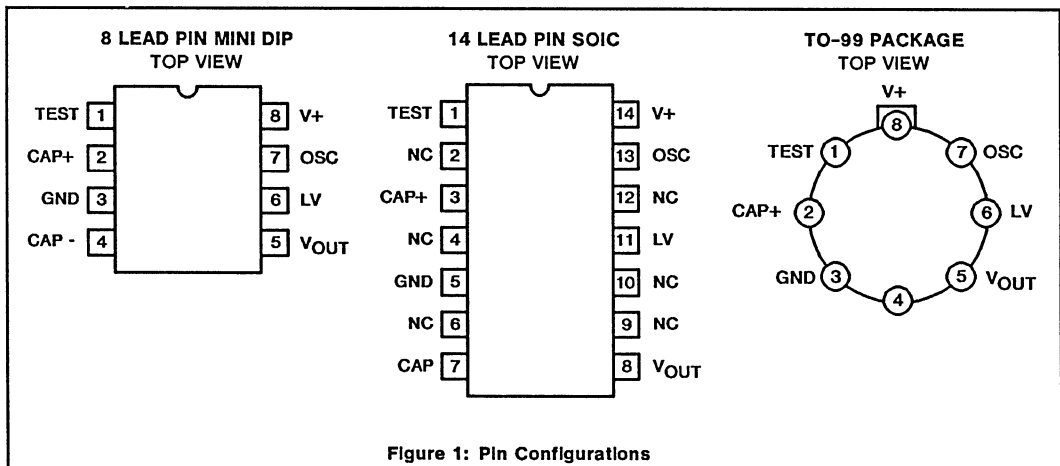
### APPLICATIONS

- On Board Negative Supply for Dynamic RAMs
- Localized  $\mu$ -Processor (8080 Type) Negative Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems
- Up to -20V for Op Amps

### ORDERING INFORMATION

| Part Number | Temperature Range | Package        |
|-------------|-------------------|----------------|
| ICL7662CTV  | 0°C to +70°C      | TO-99          |
| ICL7662CPA  | 0°C to +70°C      | 8 Pin Mini DIP |
| ICL7662CBD  | 0°C to +70°C      | 14 Pin SOIC    |
| ICL7662MTV* | -55°C to +125°C   | TO-99          |

\*Add /883B to Part Number for 883B Processing.



HARRIS SEMICONDUCTOR'S SOLE AND EXCLUSIVE WARRANTY OBLIGATION WITH RESPECT TO THIS PRODUCT SHALL BE THAT STATED IN THE WARRANTY ARTICLE OF THE CONDITION OF SALE. THE WARRANTY SHALL BE EXCLUSIVE AND SHALL BE IN LIEU OF ALL OTHER WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR USE.

NOTE: All typical values have been characterized but are not tested.

## ABSOLUTE MAXIMUM RATINGS

|   |   |
|---|---|
| Supply Voltage .....                    | 22V   |
| Oscillator Input Voltage (Note 1) ..... | -0.3V to (V <sup>+</sup> + 0.3V) for V <sup>+</sup> < 10V<br>(V <sup>+</sup> - 10V) to (V <sup>+</sup> + 0.3V) for V <sup>+</sup> > 10V |
| Current into LV (Note 1) .....          | 20μA for V <sup>+</sup> > 10V   |
| Output Short Duration .....             | Continuous  |

|   |       |
|---|-------|
| Power Dissipation (Note 2)                |       |
| ICL7662CTY .....                          | 500mW |
| ICL7662CPA .....                          | 300mW |
| ICL7662MTY .....                          | 500mW |
| Lead Temperature (Soldering, 10sec) ..... | 300°C |

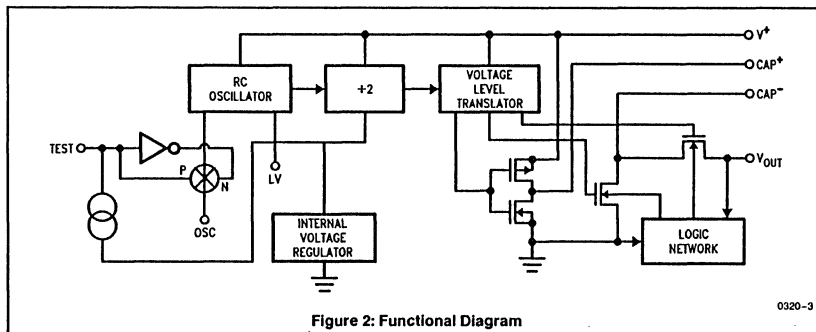
**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS V<sup>+</sup> = 15V, T<sub>A</sub> = 25°C, C<sub>OSC</sub> = 0, unless otherwise stated. Test Circuit

Figure 3.

| Symbol           | Parameter                         | Test Conditions  | Limits   |                   |                   | Units |
|------------------|-----------------------------------|--|----------|-------------------|-------------------|-------|
|                  |                                   |  | Min      | Typ               | Max               |       |
| V <sup>+</sup> L | Supply Voltage Range—Lo           | R <sub>L</sub> = 10kΩ, LV = GND  | 4.5      |                   | 11                | V     |
| V <sup>+</sup> H | Supply Voltage Range—Hi           | R <sub>L</sub> = 10kΩ, LV = Open   | 9        |                   | 20                | V     |
| I <sup>+</sup>   | Supply Current                    | R <sub>L</sub> = ∞, LV = Open<br>T <sub>A</sub> = 25°C<br>0°C < T <sub>A</sub> < +70°C<br>-55°C < T <sub>A</sub> < +125°C                          |          | .25<br>.30<br>.40 | .60<br>.85<br>1.0 | mA    |
| R <sub>O</sub>   | Output Source Resistance          | I <sub>o</sub> = 20mA, LV = Open<br>T <sub>A</sub> = 25°C<br>0°C < T <sub>A</sub> < +70°C<br>-55°C < T <sub>A</sub> < +125°C                       |          | 60<br>70<br>90    | 100<br>120<br>150 | Ω     |
| I <sup>+</sup>   | Supply Current                    | V <sup>+</sup> = 5V,<br>R <sub>L</sub> = ∞, LV = GND<br>T <sub>A</sub> = 25°C<br>0°C < T <sub>A</sub> < +70°C<br>-55°C < T <sub>A</sub> < +125°C   |          | 20<br>25<br>30    | 150<br>200<br>250 | μA    |
| R <sub>O</sub>   | Output Source Resistance          | V <sup>+</sup> = 5V,<br>I <sub>o</sub> = 3mA, LV = GND<br>T <sub>A</sub> = 25°C<br>0°C < T <sub>A</sub> < +70°C<br>-55°C < T <sub>A</sub> < +125°C |          | 125<br>150<br>200 | 200<br>250<br>350 | Ω     |
| F <sub>OSC</sub> | Oscillator Frequency              |  |          | 10                |                   | kHz   |
| P <sub>eff</sub> | Power Efficiency                  | R <sub>L</sub> = 2KΩ<br>T <sub>A</sub> = 25°C<br>Min < T <sub>A</sub> < Max  | 93<br>90 | 96<br>95          |                   | %     |
| V <sub>OEF</sub> | Voltage Conversion Effic.         | R <sub>L</sub> = ∞<br>Min < T <sub>A</sub> < Max   | 97       | 99.9              |                   | %     |
| I <sub>osc</sub> | Oscillator Sink or Source Current | V <sup>+</sup> = 5V (V <sub>osc</sub> = 0V to +5V)<br>V <sup>+</sup> = 15V (V <sub>osc</sub> = +5V to +15V)  |          | 0.5<br>4.0        |                   | μA    |

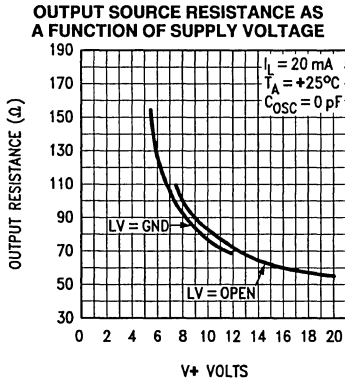
- NOTES:**
1. Connecting any terminal to voltages greater than V<sup>+</sup> or less than ground may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the ICL7662.
  2. Derate linearly above 50°C by 5.5mW/°C.
  3. Pin 1 is a Test pin and is not connected in normal use. When the TEST pin is connected to V<sup>+</sup>, an internal transmission gate disconnects any external parasitic capacitance from the oscillator which would otherwise reduce the oscillator frequency from its nominal value.



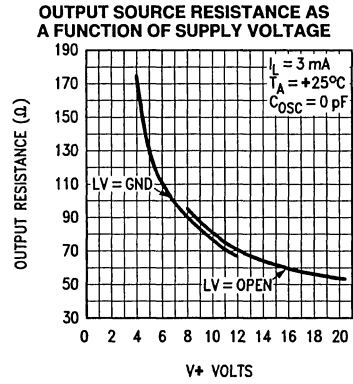
*NOTE: All typical values have been characterized but are not tested.*

## TYPICAL PERFORMANCE CHARACTERISTICS

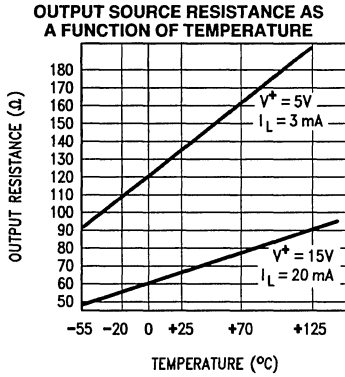
(See Test Circuit of Figure 3)



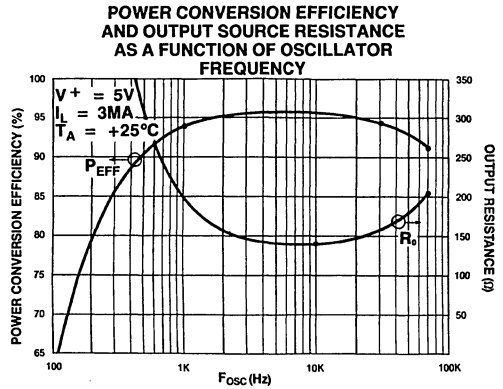
0320-4



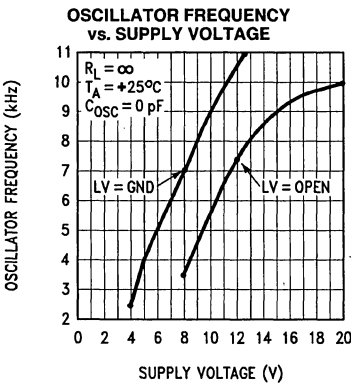
0320-5



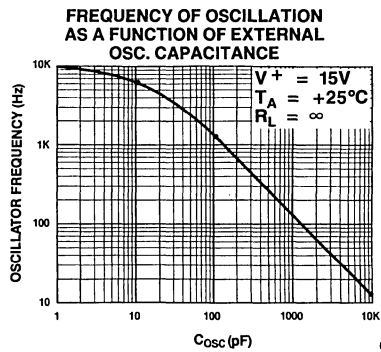
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0320-8



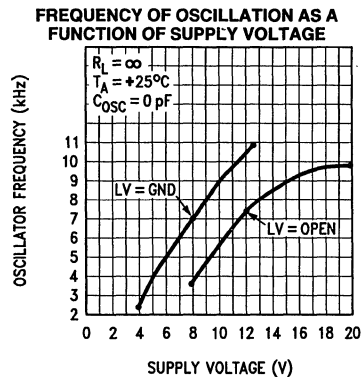
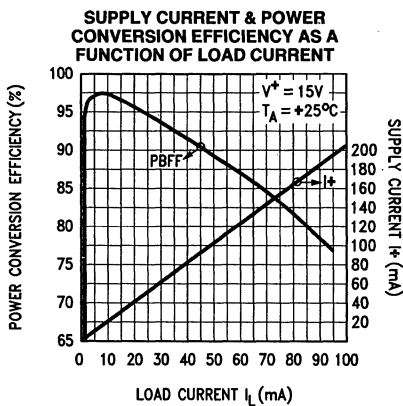
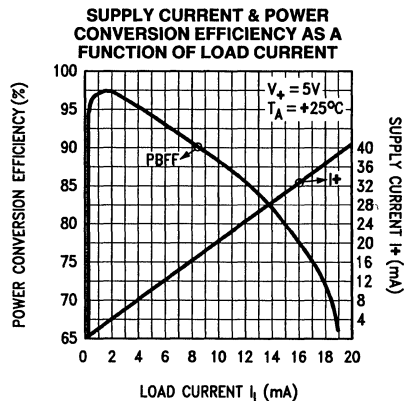
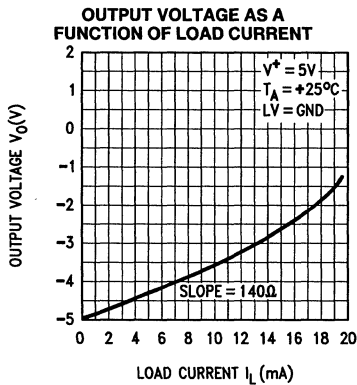
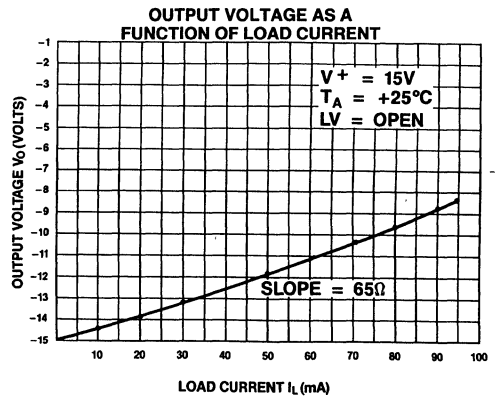
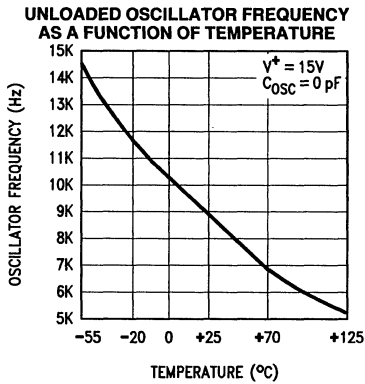
0320-9

NOTE: All typical values have been characterized but are not tested.



## TYPICAL PERFORMANCE CHARACTERISTICS

(See Test Circuit of Figure 3) (Continued)

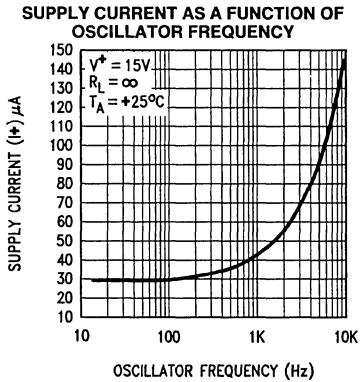


NOTE: All typical values have been characterized but are not tested.

# ICL7662

## TYPICAL PERFORMANCE CHARACTERISTICS

(See Test Circuit of Figure 3) (Continued)



0320-16

### NOTE 4.

Note that these curves include in the supply current that current fed directly into the load  $R_L$  from  $V^+$  (see Figure 3). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7662, to the negative side of the load. Ideally,  $V_{LOAD} \approx 2V_{IN}$ ,  $I_S \approx 2 I_L$ , so  $V_{IN} \cdot I_S \approx V_{LOAD} \cdot I_L$

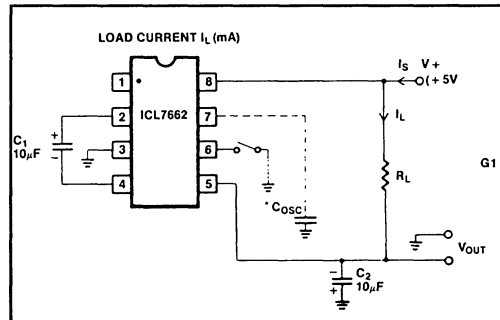
## CIRCUIT DESCRIPTION

The ICL7662 contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive  $10\mu F$  polarized electrolytic capacitors. The mode of operation of the device may be best understood by considering Figure 4, which shows an idealized negative voltage converter. Capacitor  $C_1$  is charged to a voltage,  $V^+$ , for the half cycle when switches  $S_1$  and  $S_3$  are closed. (Note: Switches  $S_2$  and  $S_4$  are open during this half cycle.) During the second half cycle of operation, switches  $S_2$  and  $S_4$  are closed, with  $S_1$  and  $S_3$  open, thereby shifting capacitor  $C_1$  negatively by  $V^+$  volts. Charge is then transferred from  $C_1$  to  $C_2$  such that the voltage on  $C_2$  is exactly  $V^+$ , assuming ideal switches and no load on  $C_2$ . The ICL7662 approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7662, the 4 switches of Figure 4 are MOS power switches;  $S_1$  is a P-channel device and  $S_2$ ,  $S_3$  &  $S_4$  are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of  $S_3$  &  $S_4$  must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions ( $V_{OUT} = V^+$ ), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7662 by a logic network which senses the output voltage ( $V_{OUT}$ ) together with the level translators, and switches the substrates of  $S_3$  &  $S_4$  to the correct level to maintain necessary reverse bias.

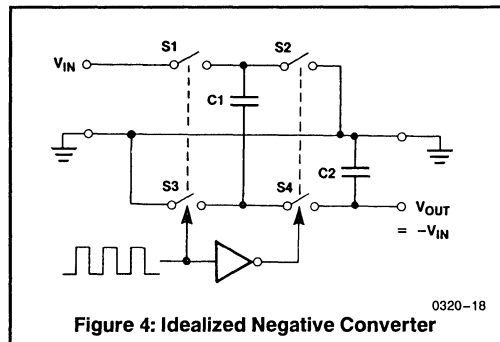
The voltage regulator portion of the ICL7662 is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 11 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.



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**NOTE:** For large value of  $C_{OSC}$  ( $> 1000\text{pF}$ ) the values of  $C_1$  and  $C_2$  should be increased to  $100\mu F$ .

**Figure 3: ICL7662 Test Circuit**



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**Figure 4: Idealized Negative Converter**

## THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory a voltage multiplier can approach 100% efficiency if certain conditions are met:

- A The drive circuitry consumes minimal power
- B The output switches have extremely low ON resistance and virtually no offset.
- C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7662 approaches these conditions for negative voltage multiplication if large values of  $C_1$  and  $C_2$  are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

$$E = \frac{1}{2} C_1 (V_1^2 - V_2^2)$$

where  $V_1$  and  $V_2$  are the voltages on  $C_1$  during the pump and transfer cycles. If the impedances of  $C_1$  and  $C_2$  are relatively high at the pump frequency (refer to Figure 4) compared to the value of  $R_L$ , there will be a substantial difference in the voltages  $V_1$  and  $V_2$ . Therefore it is not only desirable to make  $C_2$  as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for  $C_1$  in order to achieve maximum efficiency of operation.

## DO'S AND DON'TS

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 11 volts.
3. When using polarized capacitors, the + terminal of  $C_1$  must be connected to pin 2 of the ICL7662 and the + terminal of  $C_2$  must be connected to GROUND.
4. If the voltage supply driving the 7662 has a large source impedance (25 - 30 ohms), then a 2.2 $\mu$ F capacitor from pin 8 to ground may be required to limit rate of rise of input voltage to less than 2V/ $\mu$ s.
5. User should insure that the output (pin 5) does not go more positive than GND (pin 3). Device latch up will occur under these conditions.

A 1N914 or similar diode placed in parallel with  $C_2$  will prevent the device from latching up under these conditions. (Anode pin 5, Cathode pin 6).

## TYPICAL APPLICATIONS

### Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7662 for generation of negative supply voltages. Figure 5 shows typical connections to provide a negative supply where a positive supply of +4.5V to 20.0V is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltages below 11 volts.

The output characteristics of the circuit in Figure 5a can be approximated by an ideal voltage source in series with a resistance as shown in Figure 5b. The voltage source has a value of  $-(V^+)$ . The output impedance ( $R_o$ ) is a function of the ON resistance of the internal MOS switches (shown in Figure 4), the switching frequency, the value of  $C_1$  and  $C_2$ , and the ESR (equivalent series resistance) of  $C_1$  and  $C_2$ . A good first order approximation for  $R_o$  is:

$$R_o \approx 2(R_{SW1} + R_{SW3} + ESR_{C1}) + 2(R_{SW2} + R_{SW4} + ESR_{C1}) + \frac{1}{f_{PUMP} \times C1} + ESR_{C2}$$

$$(f_{PUMP} = \frac{f_{OSC}}{2}, R_{SWX} = \text{MOSFET switch resistance})$$

Combining the four  $R_{SWX}$  terms as  $R_{SW}$ , we see that:

$$R_o \approx 2 \times R_{SW} + \frac{1}{f_{PUMP} \times C1} + 4 \times ESR_{C1} + ESR_{C2} \Omega$$

$R_{SW}$ , the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs), typically 24 $\Omega$  @ 25°C and 15V, and 53 $\Omega$  @ 25°C and 5V. Careful selection of  $C_1$  and  $C_2$  will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the  $1/(f_{PUMP} \times C1)$  component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the  $1/(f_{PUMP} \times C1)$  term, but may have the side effect of a net increase in output impedance when  $C_1 > 10 \mu\text{F}$  and there is no longer enough time to fully charge the capacitors every cycle. In a typical application where  $f_{OSC} = 10 \text{ kHz}$  and  $C = C_1 = C_2 = 10 \mu\text{F}$ :

$$R_o \approx 2 \times 23 + \frac{1}{(5 \times 10^3 \times 10 \times 10^{-6})} + 4 \times ESR_{C1} + ESR_{C2}$$

$$R_o \approx 46 + 20 + 5 \times ESR_{C1} \Omega$$

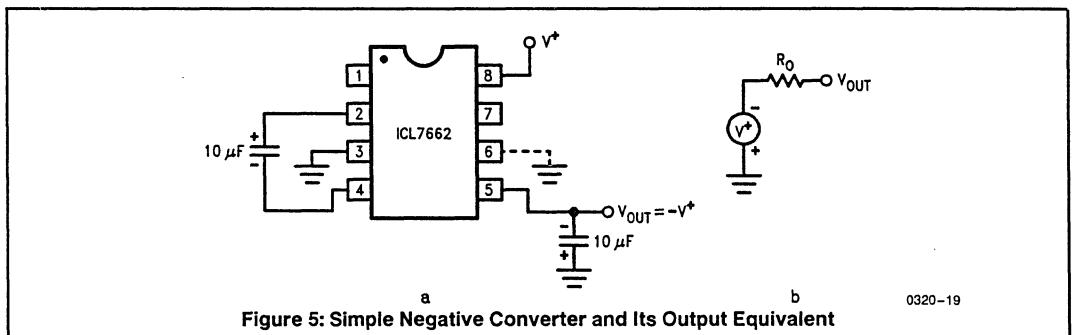


Figure 5: Simple Negative Converter and Its Output Equivalent

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Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low  $1/(f_{PUMP} \times C1)$  term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as  $10\Omega$ .

## Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by 2 voltages, A and B, as shown in Figure 6. Segment A is the voltage drop across the ESR of C2 at the instant it goes from being charged by C1 (current flowing into C2) to being discharged through the load (current flowing out of C2). The magnitude of this current change is  $2 \times I_{OUT}$ , hence the total drop is  $2 \times I_{OUT} \times ESR_{C2}$  volts. Segment B is the voltage change across C2 during time  $t_2$ , the half of the cycle when C2 supplies current to the load. The drop at B is  $I_{OUT} \times t_2/C2$  volts. The peak-to-peak ripple voltage is the sum of these voltage drops:

$$V_{ripple} \cong \left( \frac{1}{2 \times f_{PUMP} \times C2} + 2 \times ESR_{C2} \right) \times I_{OUT}$$

Again, a low ESR capacitor will result in a higher performance output.

## Paralleling Devices

Any number of ICL7662 voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, C2, serves all devices while each device requires its own pump capacitor, C1. The resultant output resistance would be approximately

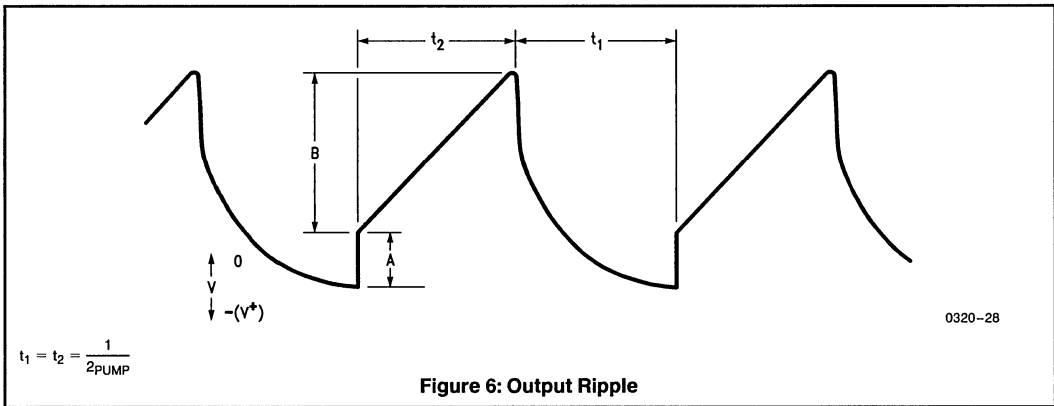
$$R_{OUT} = \frac{R_{OUT} \text{ (of ICL7662)}}{n \text{ (number of devices)}}$$

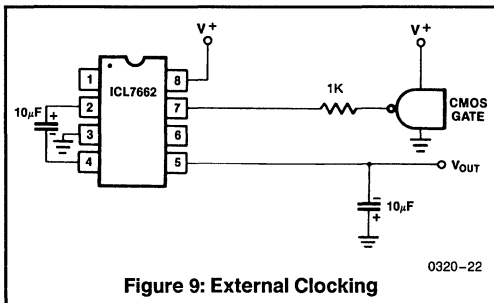
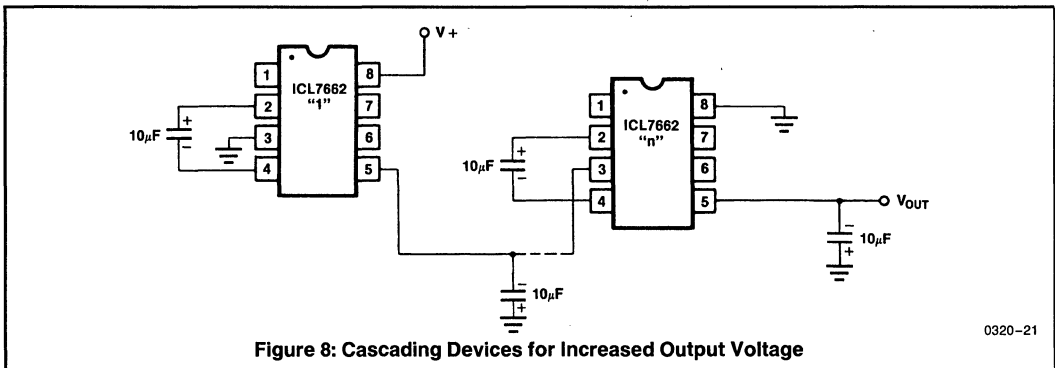
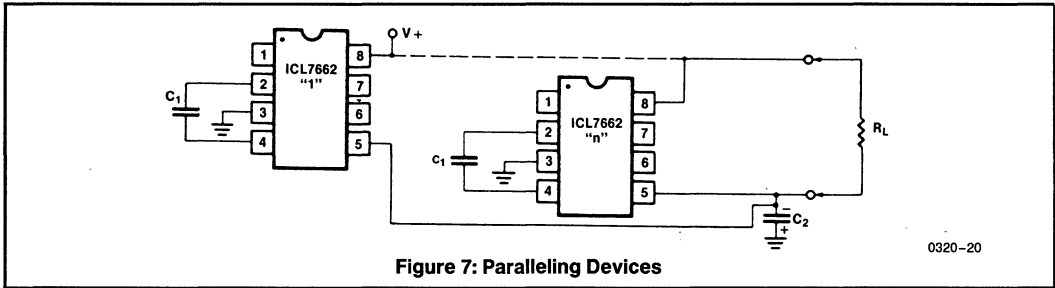
## Cascading Devices

The ICL7662 may be cascaded as shown to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n (V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7662  $R_{OUT}$  values.

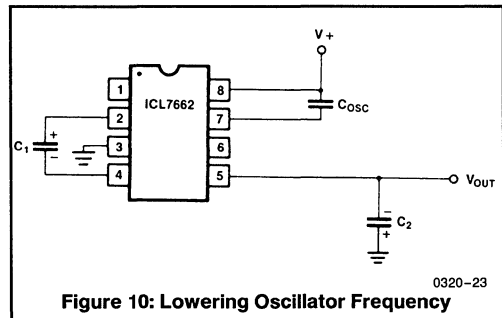




It is also possible to increase the conversion efficiency of the ICL7662 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor,  $C_{OSC}$ , as shown in Figure 10. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump ( $C_1$ ) and reservoir ( $C_2$ ) capacitors; this is overcome by increasing the values of  $C_1$  and  $C_2$  by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and  $V^+$  will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of  $C_1$  and  $C_2$  (from 10µF to 100µF).

## Changing the ICL7662 Oscillator Frequency

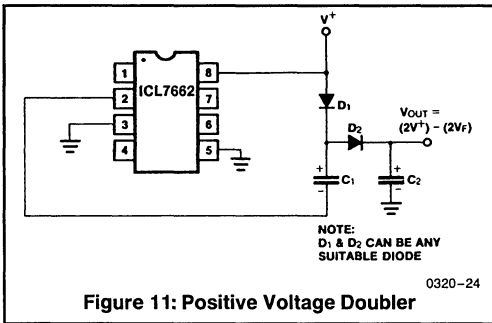
It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 9. In order to prevent possible device latchup, a 100kΩ resistor must be used in series with the clock output. In the situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pullup resistor to  $V^+$  supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be  $\frac{1}{2}$  of the clock frequency. Output transitions occur on the positive-going edge of the clock.



## Positive Voltage Doubling

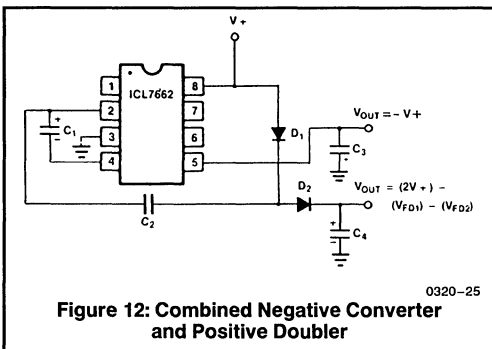
The ICL7662 may be employed to achieve positive voltage doubling using the circuit shown in Figure 11. In this application, the pump inverter switches of the ICL7662 are used to charge  $C_1$  to a voltage level of  $V^+ - V_F$  (where  $V^+$  is the supply voltage and  $V_F$  is the forward voltage drop of diode  $D_1$ ). On the transfer cycle, the voltage on  $C_1$  plus the supply voltage ( $V^+$ ) is applied through diode  $D_2$  to capacitor  $C_2$ . The voltage thus created on  $C_2$  becomes  $(2V^+) - (2V_F)$  or twice the supply voltage minus the combined forward voltage drops of diodes  $D_1$  and  $D_2$ .

The source impedance of the output ( $V_{OUT}$ ) will depend on the output current, but for  $V^+ = 15$  volts and an output current of 10mA it will be approximately 70 ohms.



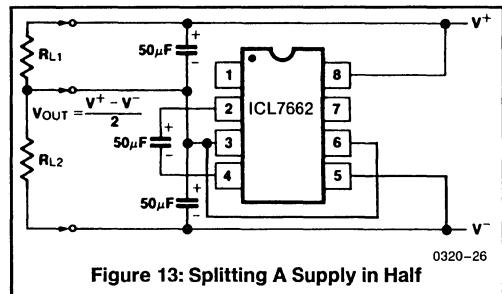
## Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 12 combines the functions shown in Figures 5 and 11 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9 volts and -5 volts from an existing +5 volt supply. In this instance capacitors  $C_1$  and  $C_3$  perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors  $C_2$  and  $C_4$  are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.



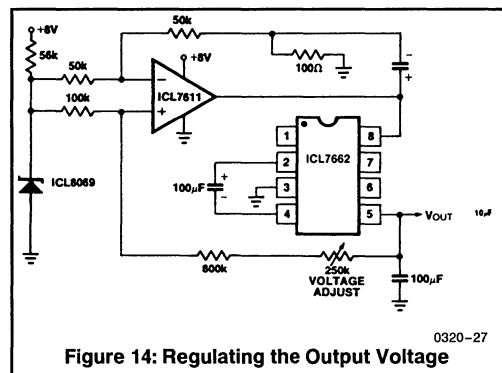
## Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 13. The combined load will be evenly shared between the two sides and, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 8, +30V can be converted (via +15V, and -15V) to a nominal -30V, although with rather high series output resistance ( $\sim 250\Omega$ ).



## Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7662 can be a problem, particularly if the load current varies substantially. The circuit of Figure 14 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7662's output does not respond instantaneously to a change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the 7662, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.



## OTHER APPLICATIONS

Further information on the operation and use of the ICL7662 may be found in A051 "Principals and Applications of the ICL7660 CMOS Voltage Converter".

# ICL7663S

## CMOS Programmable Micropower Positive Voltage Regulator

### GENERAL DESCRIPTION

The Harris ICL7663S Super Programmable Micropower Voltage Regulator is a low power, high efficiency positive voltage regulator which accepts 1.6V to 16V inputs and provides adjustable outputs from 1.3V to 16V at currents up to 40 mA.

It is a direct replacement for the industry standard ICL7663B offering *wider* operating voltage and temperature ranges, *improved* output accuracy (ICL7663SA), *better* temperature coefficient, *guaranteed* maximum supply current, and *guaranteed* line and load regulation. All improvements are highlighted in *bold italics* in the electrical characteristics section. *Critical parameters are guaranteed over the entire commercial and industrial temperature ranges.* The ICL7663S/SA programmable output voltage is set by two external resistors. The 1% reference accuracy of the ICL7663SA eliminates the need for trimming the output voltage in most applications.

The ICL7663S is well suited for battery powered supplies, featuring 4  $\mu$ A quiescent current, low  $V_{IN}$  to  $V_{OUT}$  differential, output current sensing and logic input level shutdown control. In addition, the ICL7663S has a negative temperature coefficient output suitable for generating a temperature compensated display drive voltage for LCD displays.

The ICL7663S is available in either an 8-pin plastic, CER-DIP, or SOIC package.

### FEATURES

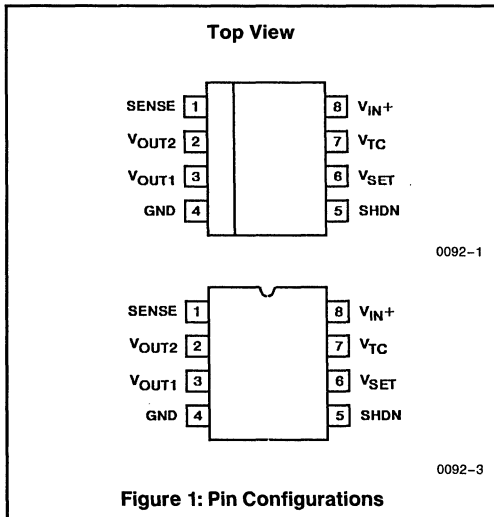
- **Guaranteed** 10  $\mu$ A Maximum Quiescent Current over *All Temperature Ranges*
- **Wider Operating Voltage Range**—1.6V to 16V
- **Guaranteed** Line and Load Regulation over *Entire Operating Temperature Range*
- **Optional**
- 1% Output Voltage Accuracy (ICL7663SA)
- Output Voltage Programmable from 1.3V to 16V
- **Improved** Temperature Coefficient of Output Voltage
- 40 mA Minimum Output Current with Current Limiting
- Output Voltages with Programmable Negative Temperature Coefficients
- Output Shutdown via Current-Limit Sensing or External Logic Level
- Low Input-to-Output Voltage Differential
- Improved Direct Replacement for Industry Standard ICL7663B and Other Second-Source Products

### APPLICATIONS

- Low-Power Portable Instrumentation
- **Pagers**
- Handheld Instruments
- LCD Display Modules
- Remote Data Loggers
- Battery-Powered Systems

### ORDERING INFORMATION

| Part Number   | Temperature Range | Package   |
|---|-------------------|---|
| ICL7663SCBA<br>ICL7663SCPA<br>ICL7663SCJA<br>ICL7663SACPA<br>ICL7663SACJA | 0°C to +70°C      | 8 Lead SOIC<br>8 Lead Minidip<br>8 Lead CERDIP<br>8 Lead Minidip<br>8 Lead CERDIP |
| ICL7663SIBA<br>ICL7663SIPA<br>ICL7663SIJA<br>ICL7663SAIPA<br>ICL7663SAIJA | -25°C to +85°C    | 8 Lead SOIC<br>8 Lead Minidip<br>8 Lead CERDIP<br>8 Lead Minidip<br>8 Lead CERDIP |



## ABSOLUTE MAXIMUM RATINGS

|                                       |                              |
|---------------------------------------|------------------------------|
| Input Supply Voltage                  | ..... +18V                   |
| Any Input or Output Voltage (Note 1)  | .....(V <sub>IN</sub> + 0.3) |
|                                       | to (GND - 0.3)V              |
| Output Source Current                 |                              |
| (Terminal 2)                          | ..... 50 mA                  |
| (Terminal 3)                          | ..... 25 mA                  |
| Output Sinking Current                |                              |
| (Terminal 7)                          | ..... -10 mA                 |
| Lead Temperature (Soldering, 10 sec.) | ..... 300°C                  |
| Storage Temperature Range             | ..... -65°C to +150°C        |
| Operating Temperature Range           |                              |
| ICL7663SC                             | ..... 0°C to +70°C           |
| ICL7663SI                             | ..... -25°C to +85°C         |
| Total Power Dissipation (Note 2)      |                              |
| SOIC                                  | ..... 200 mW                 |
| Minidip                               | ..... 200 mW                 |
| CERDIP                                | ..... 500 mW                 |

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**ELECTRICAL CHARACTERISTICS** Specifications below applicable to both ICL7663S and ICL7663SA unless otherwise stated. V<sup>+</sup><sub>IN</sub> = 9V, V<sub>OUT</sub> = 5V, T<sub>A</sub> = 25°C, unless otherwise stated. See Test Circuit, Figure 3.

| Symbol   | Parameter                            | Test Conditions  | Limits       |             |              | Units |
|--|--------------------------------------|--|--------------|-------------|--------------|-------|
|  |                                      |  | Min          | Typ         | Max          |       |
| V <sup>+</sup> <sub>IN</sub>                         | <b>Input Voltage</b>                 | <b>ICL7663S</b>  |              |             |              |       |
|  |                                      | T <sub>A</sub> = 25°C  | 1.5          |             | <b>16</b>    | V     |
|  |                                      | 0°C < T <sub>A</sub> < +70°C                                     | 1.6          |             | <b>16</b>    | V     |
|  |                                      | -25°C < T <sub>A</sub> < +85°C                                   | 1.6          |             | <b>16</b>    |       |
|  |                                      | <b>ICL7663SA</b>   |              |             |              |       |
|  |                                      | 0°C < T <sub>A</sub> < +70°C                                     | <b>1.6</b>   |             | <b>16</b>    | V     |
|  |                                      | -25°C < T <sub>A</sub> < +85°C                                   | <b>1.6</b>   |             | <b>16</b>    |       |
| I <sub>Q</sub>                                       | <b>Quiescent Current</b>             | 1.4V ≤ V <sub>OUT</sub> ≤ 8.5V, No Load                          |              |             |              |       |
|  |                                      | V <sup>+</sup> <sub>IN</sub> = 9V, 0°C < T <sub>A</sub> < 70°C   |              |             | <b>10</b>    | μA    |
|  |                                      | -25°C < T <sub>A</sub> < +85°C                                   |              |             | <b>10</b>    |       |
|  |                                      | V <sup>+</sup> <sub>IN</sub> = 16V, 0°C < T <sub>A</sub> < +70°C |              |             | <b>12</b>    | μA    |
|  |                                      | -25°C < T <sub>A</sub> < +85°C                                   |              |             | <b>12</b>    |       |
| V <sub>SET</sub>                                     | <b>Reference Voltage</b>             | I <sub>OUT1</sub> = 100 μA, V <sub>OUT</sub> = V <sub>SET</sub>  |              |             |              |       |
|  |                                      | <b>ICL7663S</b> T <sub>A</sub> = 25°C                            | 1.2          | 1.3         | 1.4          | V     |
|  |                                      | <b>ICL7663SA</b> T <sub>A</sub> = 25°C                           | <b>1.275</b> | <b>1.29</b> | <b>1.305</b> | V     |
| $\frac{\Delta V_{SET}}{\Delta T}$                    | <b>Temperature Coefficient</b>       | 0°C < T <sub>A</sub> < +70°C                                     |              | <b>100</b>  |              | ppm   |
|  |                                      | -25°C < T <sub>A</sub> < +85°C                                   |              | <b>100</b>  |              | ppm   |
| $\frac{\Delta V_{SET}}{V_{SET} \cdot \Delta V_{IN}}$ | <b>Line Regulation</b>               | 2V < V <sub>IN</sub> < 15V                                       |              |             |              |       |
|  |                                      | 0°C < T <sub>A</sub> < +70°C                                     |              | 0.03        |              | %/V   |
|  |                                      | -25°C < T <sub>A</sub> < +85°C                                   |              | 0.03        | <b>0.3</b>   | %/V   |
| I <sub>SET</sub>                                     | <b>V<sub>SET</sub> Input Current</b> | 0°C < T <sub>A</sub> < +70°C                                     |              | 0.01        | <b>10</b>    | nA    |
|  |                                      | -25°C < T <sub>A</sub> < +85°C                                   |              | 0.01        | <b>10</b>    | nA    |

**NOTE:** 1. Connecting any terminal to voltages greater than (V<sup>+</sup><sub>IN</sub> + 0.3V) or less than (GND - 0.3V) may cause destructive device latch-up. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7663S power-up.

2. Derate linearly above 50°C at 5 mW/°C for Plastic Minidip, 7.5 mW/°C for TO-99 can, and 10 mW/°C for CERDIP.

NOTE: All typical values have been characterized but are not tested.



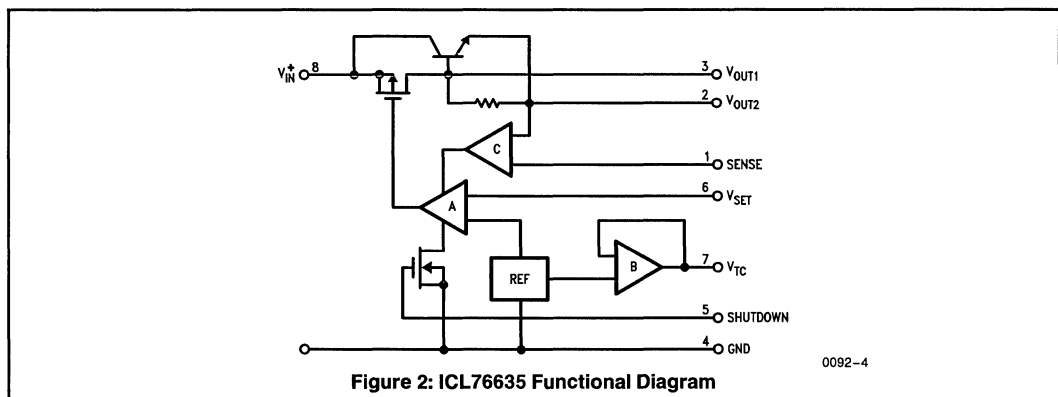
# ICL7663S

**ELECTRICAL CHARACTERISTICS** Specifications below applicable to both ICL7663S and ICL7663SA unless otherwise stated.  $V_{IN} = 9V$ ,  $V_{OUT} = 5V$ ,  $T_A = 25^\circ C$ , unless otherwise stated. See Test Circuit, Figure 3.

| Symbol                                  | Parameter  | Test Conditions   | Limits           |   |   | Units                            |
|---|--|---|------------------|---|---|----------------------------------|
|   |  |   | Min              | Typ   | Max   |                                  |
| $I_{SHDN}$                              | Shutdown Input Current   |   |                  | $\pm 0.01$  | 10  | nA                               |
| $V_{SHDN}$                              | Shutdown Input Voltage   | $V_{SHDN}$ HI: Both $V_{OUT}$ Disabled<br>$V_{SHDN}$ LO: Both $V_{OUT}$ Enable  | 1.4              |   | 0.3   | V<br>V                           |
| $I_{SENSE}$                             | Sense Pin Input Current  |   |                  | 0.01  | 10  | nA                               |
| $V_{CL}$                                | Sense Pin Input Threshold                                      |   |                  | 0.5   |   | V                                |
| $R_{SAT}$                               | <b><i>Input-Output Saturation Resistance (Note 3)</i></b>      | $V_{IN} = 2V$ , $I_{OUT1} = 1\text{ mA}$<br>$V_{IN} = 9V$ , $I_{OUT1} = 2\text{ mA}$<br>$V_{IN} = 15V$ , $I_{OUT1} = 5\text{ mA}$ |                  | <b><i>170</i></b><br><b><i>50</i></b><br><b><i>35</i></b> | <b><i>350</i></b><br><b><i>100</i></b><br><b><i>70</i></b>  | $\Omega$<br>$\Omega$<br>$\Omega$ |
| $\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$ | <b><i>Load Regulation</i></b>                                  | $1\text{ mA} < I_{OUT2} < 20\text{ mA}$<br>$50\ \mu A < I_{OUT1} < 5\text{ mA}$   |                  | 1<br>2  | <b><i>3</i></b><br><b><i>10</i></b>                         | $\Omega$<br>$\Omega$             |
| $I_{OUT2}$                              | <b><i>Available Output Current (<math>V_{OUT2}</math>)</i></b> | $3V \leq V_{IN} \leq 16V$ ,<br>$V_{IN} - V_{OUT2} = 1.5V$   | <b><i>40</i></b> |   |   | mA                               |
| $V_{TC}$                                | Negative Tempco Output (Note 4)                                | Open-Circuit Voltage  |                  | 0.9   |   | V                                |
| $I_{TC}$                                |  | Maximum Sink Current  | 0                | 8   | 2.0   | mA                               |
| $\frac{\Delta V_{TC}}{\Delta T}$        | Temperature Coefficient  | Open Circuit  |                  | +2.5  |   | mV/ $^\circ C$                   |
| $I_{L(MIN)}$                            | Minimum Load Current   | (Includes $V_{SET}$ Divider)<br>$T_A = 25^\circ C$<br>$0^\circ C < T_A < +70^\circ C$<br>$-25^\circ C < T_A < +85^\circ C$        |                  | 0.2<br>0.2  | <b><i>1.0</i></b><br><b><i>5.0</i></b><br><b><i>5.0</i></b> | $\mu A$<br>$\mu A$<br>$\mu A$    |

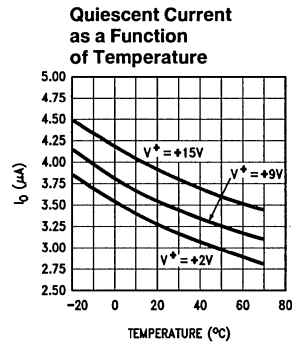
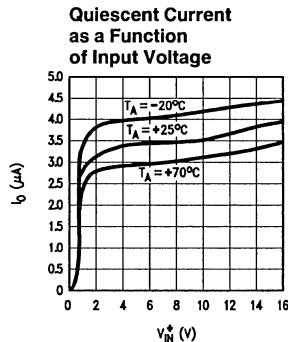
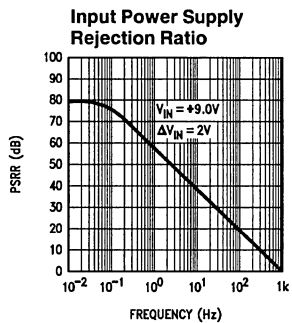
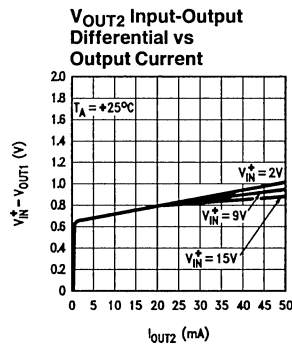
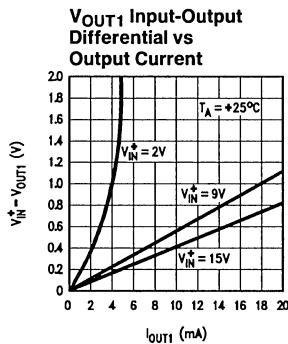
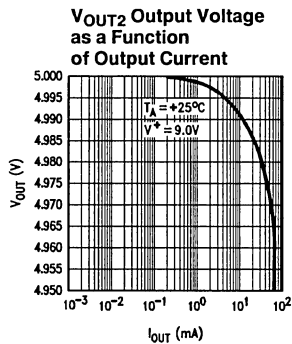
**NOTE: 3.** This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential at low current (under 5 mA), can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

- This output has a positive temperature coefficient. Using it in combination with the inverting input of the regulator at  $V_{SET}$ , a negative coefficient results in the output voltage. See Figure 5 for details. Pin will not source current.
- All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V.
- All significant improvements over the industry standard ICL7663 are highlighted in ***bold italics***.



NOTE: All typical values have been characterized but are not tested.

## TYPICAL PERFORMANCE CHARACTERISTICS



0092-5

## DETAILED DESCRIPTION

The ICL7663S is a CMOS integrated circuit incorporating all the functions of a voltage regulator plus protection circuitry on a single monolithic chip. Referring to the functional diagram (Figure 2), the main blocks are a bandgap-type voltage reference, an error amplifier, and an output driver with both PMOS and NPN pass transistors.

The bandgap output voltage, trimmed to  $1.29V \pm 15\text{ mV}$  for the ICL7663SA, and the input voltage at the  $V_{SET}$  terminal are compared in amplifier A. Error amplifier A drives a P-channel pass transistor which is sufficient for low (under about 5 mA) currents. The high current output is passed by an NPN bipolar transistor connected as a follower. This configuration gives more gain and lower output impedance.

Logic-controlled shutdown is implemented via a N-channel MOS transistor. Current-sensing is achieved with comparator C, which functions with the  $V_{OUT2}$  terminal. The ICL7663S has an output ( $V_{TC}$ ) from a buffer amplifier (B), which can be used in combination with amplifier A to generate programmable-temperature-coefficient output voltages.

The amplifier, reference and comparator circuitry all operate at bias levels well below  $1\ \mu\text{A}$  to achieve extremely low quiescent current. This does limit the dynamic response of

the circuits, however, and transients are best dealt with outside the regulator loop.

## BASIC OPERATION

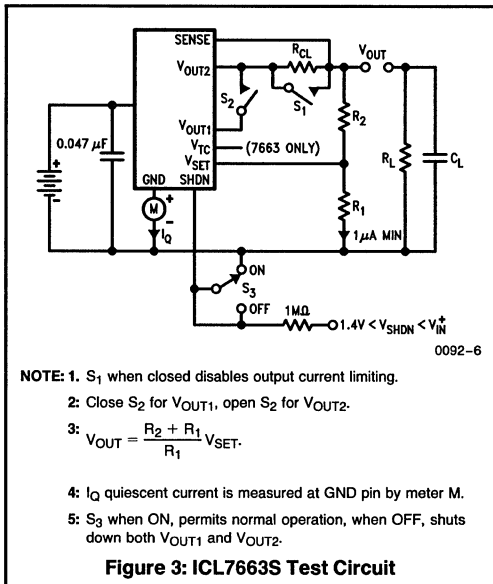
The ICL7663S is designed to regulate battery voltages in the 5V to 15V region at maximum load currents of about 5 mA to 30 mA. Although intended as low power devices, power dissipation limits must be observed. For example, the power dissipation in the case of a 10V supply regulated down to 2V with a load current of 30 mA clearly exceeds the power dissipation rating of the Minidip:

$$(10 - 2)(30)(10^{-3}) = 240\text{ mW}$$

The circuit of Figure 4 illustrates proper use of the device. CMOS devices generally require two precautions: every input pin must go somewhere, and maximum values of applied voltages and current limits must be rigorously observed. Neglecting these precautions may lead to, at the least, incorrect or nonoperation, and at worst, destructive device failure. To avoid the problem of latchup, do not apply inputs to any pins before supply voltage is applied.

NOTE: All typical values have been characterized but are not tested.

# ICL7663S



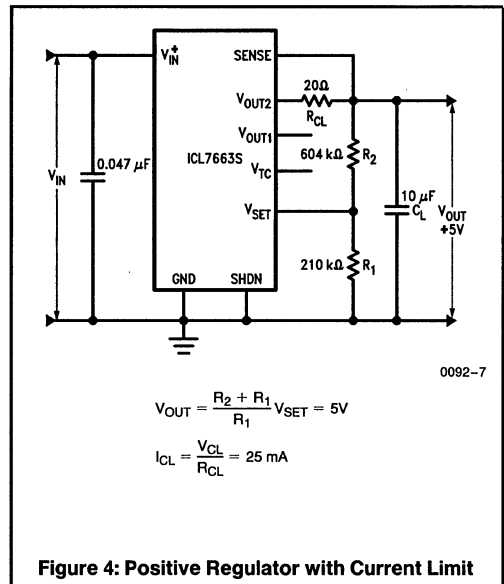
**Figure 3: ICL7663S Test Circuit**

**Input Voltages**—The ICL7663S accepts working inputs of 1.5V to 16V. When power is applied, the rate-of-rise of the input may be hundreds of volts per microsecond. This is potentially harmful to the regulators, where internal operating currents are in the nanoampere range. The 0.047  $\mu$ F capacitor on the device side of the switch will limit inputs to a safe level around 2 V/ $\mu$ s. Use of this capacitor is suggested in all applications. In severe rate-of-rise cases, it may be advisable to use an RC network on the SHutDown pin to delay output turn-on. Battery charging surges, transients, and assorted noise signals should be kept from the regulators by RC filtering, zener protection, or even fusing.

**Output Voltages**—The resistor divider  $R_2/R_1$  is used to scale the reference voltage,  $V_{SET}$ , to the desired output using the formula  $V_{OUT} = (1 + R_2/R_1) V_{SET}$ . Suitable arrangements of these resistors, using a potentiometer, enables exact values for  $V_{OUT}$  to be obtained. In most applications the potentiometer may be eliminated by using the ICL7663SA. The ICL7663SA has  $V_{SET}$  voltage guaranteed to be  $1.29V \pm 15$  mV and when used with  $\pm 1\%$  tolerance resistors for  $R_1$  and  $R_2$  the initial output voltage will be within  $\pm 2.7\%$  of ideal.

The low leakage current of the  $V_{SET}$  terminal allows  $R_1$  and  $R_2$  to be tens of megohms for minimum additional quiescent drain current. However, some load current is required for proper operation, so for extremely low-drain applications it is necessary to draw at least 1  $\mu$ A. This can include the current for  $R_2$  and  $R_1$ .

Output voltages up to nearly the  $V_{IN}$  supply may be obtained at low load currents, while the low limit is the reference voltage. The minimum input-output differential in each regulator is obtained using the  $V_{OUT1}$  terminal. The input-output differential increases to 1.5V when using  $V_{OUT2}$ .



**Figure 4: Positive Regulator with Current Limit**

**Output Currents**—Low output currents of less than 5 mA are obtained with the least input-output differential from the  $V_{OUT1}$  terminal (connect  $V_{OUT2}$  to  $V_{OUT1}$ ). Where higher currents are needed, use  $V_{OUT2}$  ( $V_{OUT1}$  should be left open in this case).

High output currents can be obtained only as far as package dissipation allows. It is strongly recommended that output current-limit sensing be used in such cases.

**Current-Limit Sensing**—The on-chip comparator (C in Figure 2) permits shutdown of the regulator output in the event of excessive current drain. As Figure 4 shows, a current-limiting resistor,  $R_{CL}$ , is placed in series with  $V_{OUT2}$  and the SENSE terminal is connected to the load side of  $R_{CL}$ . When the current through  $R_{CL}$  is high enough to produce a voltage drop equal to  $V_{CL}$  (0.5V) the voltage feedback is bypassed and the regulator output will be limited to this current. Therefore, when the maximum load current ( $I_{LOAD}$ ) is determined, simply divide  $V_{CL}$  by  $I_{LOAD}$  to obtain the value for  $R_{CL}$ .

**Logic-Controllable Shutdown**—When equipment is not needed continuously (e.g., in remote data-acquisition systems), it is desirable to eliminate its drain on the system until it is required. This usually means switches, with their unreliable contacts. Instead, the ICL7663S can be shut down by a logic signal, leaving only  $I_Q$  (under 4  $\mu$ A) as a drain on the power source. Since this pin must not be left open, it should be tied to ground if not needed. A voltage of less than 0.3V for the ICL7663S will keep the regulator ON, and a voltage level of more than 1.4V but less than  $V^+_{IN}$  will turn the outputs OFF. If there is a possibility that the control signal could exceed the regulator input ( $V^+_{IN}$ ) the current from this signal should be limited to 100  $\mu$ A maximum by a high-value (1 M $\Omega$ ) series resistor. This situation may occur when the logic signal originates from a system powered separately from that of the regulator.

**Additional Circuit Precautions**—This regulator has poor rejection of voltage fluctuations from AC sources above 10 Hz or so. To prevent the output from responding (where this might be a problem), a reservoir capacitor across the load is advised. The value of this capacitor is chosen so that the regulated output voltage reaches 90% of its final value in 20 ms. From

$$I = C \frac{\Delta V}{\Delta t}, C = I_{OUT} \frac{(20 \times 10^{-3})}{0.9 V_{OUT}} = 0.022 \frac{I_{OUT}}{V_{OUT}}$$

In addition, where such a capacitor is used, a current-limiting resistor is also suggested (see "Current-Limit Sensing").

**Producing Output Voltages with Negative Temperature Coefficients**—The ICL7663S has an additional output which is 0.9V relative to GND and has a tempco of +2.5 mV/°C. By applying this voltage to the inverting input of amplifier A (i.e., the V<sub>SET</sub> pin), output voltages having negative TC may be produced. The TC of the output voltage is controlled by the R<sub>2</sub>/R<sub>3</sub> ratio (see Figure 5 and its design equations).

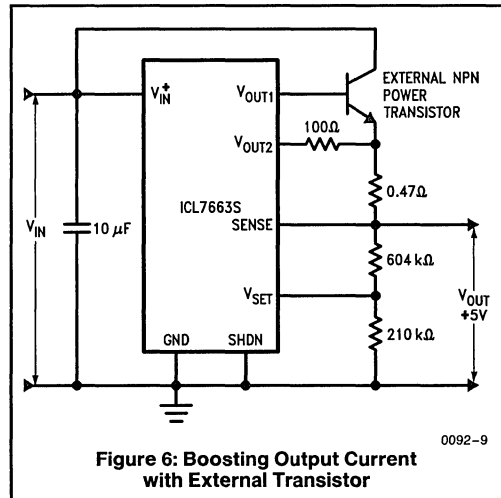
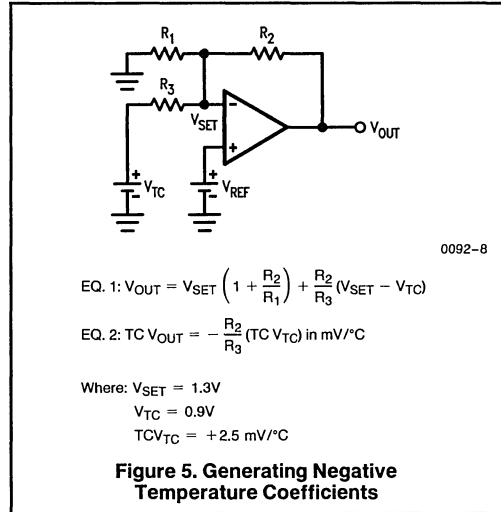
## APPLICATIONS

### Boosting Output Current with External Transistor

The maximum available output current from the ICL7663S is 40 mA. To obtain output currents greater than 40 mA, an external NPN transistor is used connected as shown in Figure 6.

### Generating a Temperature Compensated Display Drive Voltage

Temperature has an important effect in the variation of threshold voltage in multiplexed LCD displays. As temperature rises, the threshold voltage goes down. For applications where the display temperature varies widely, a temperature compensated display voltage, V<sub>DISP</sub>, can be generated using the ICL7663S. This is shown in Figure 7 for the ICM7233 triplexed LCD display driver.



NOTE: All typical values have been characterized but are not tested.

## APPLICATIONS

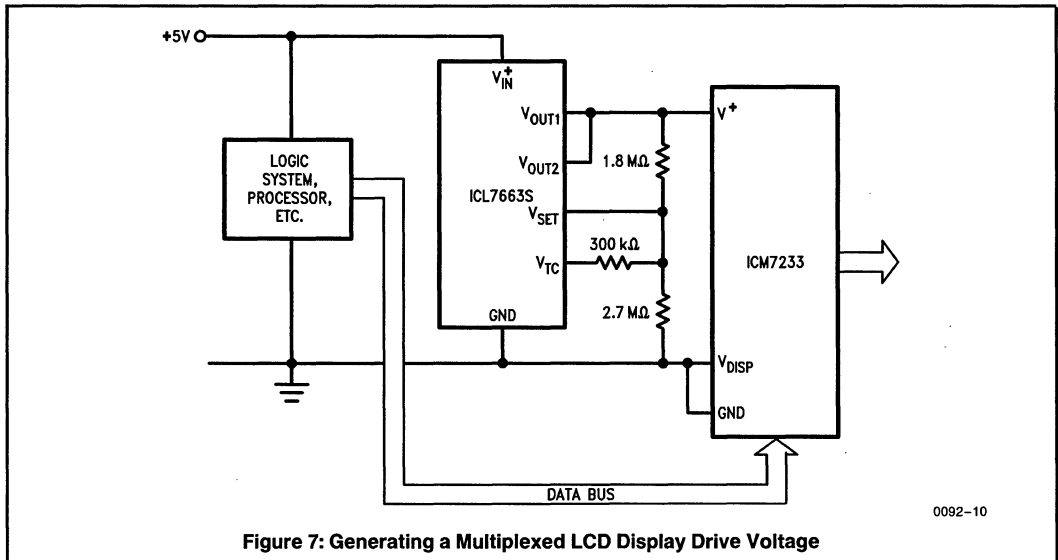


Figure 7: Generating a Multiplexed LCD Display Drive Voltage

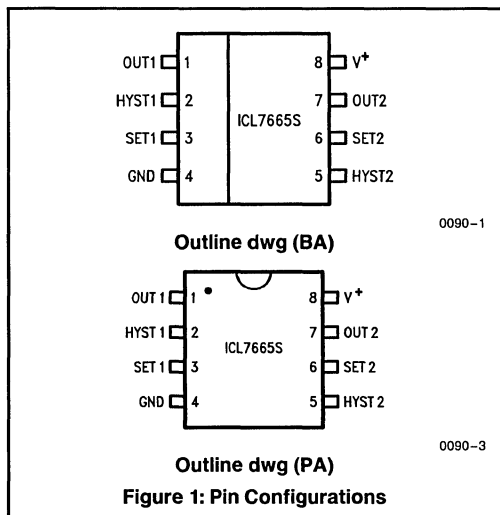
# ICL7665S

## CMOS Micropower Over/Under Voltage Detector

### GENERAL DESCRIPTION

The ICL7665S Super CMOS Micropower Over/Under Voltage Detector contains two low power, individually programmable voltage detectors on a single CMOS chip. Requiring typically 3  $\mu\text{A}$  for operation, the device is intended for battery-operated systems and instruments which require high or low voltage warnings, settable trip points, or fault monitoring and correction. The trip points and hysteresis of the two voltage detectors are individually programmed via external resistors. An internal bandgap-type reference provides an accurate threshold voltage while operating from any supply in the 1.6V to 16V range.

The Harris ICL7665S, Super Programmable Over/Under Voltage Detector is a direct replacement for the industry standard ICL7665B offering *wider* operating voltage and temperature ranges, *improved* threshold accuracy (ICL7665SA), and temperature coefficient, and *guaranteed* maximum supply current. All improvements are highlighted in bold italics in the electrical characteristics section. *All critical parameters are guaranteed over the entire commercial and industrial temperature ranges.*



### FEATURES

- **Guaranteed 10  $\mu\text{A}$  Maximum Quiescent Current over Temperature**
- **Guaranteed Wider Operating Voltage Range over Entire Operating Temperature Range**
- **2% Threshold Accuracy (ICL7665SA)**
- **Dual Comparator with Precision Internal Reference**
- **100 ppm/ $^{\circ}\text{C}$  Temperature Coefficient of Threshold Voltage**
- **Improved Direct Replacement for Industry-Standard ICL7665B and Other Second-Source Devices**
- **Up to 20 mA Output Current Sinking Ability**
- **Individually Programmable Upper and Lower Trip Voltages and Hysteresis Levels**

### APPLICATIONS

- **Pocket Pagers**
- **Portable Instrumentation**
- **Charging Systems**
- **Memory Power Back-Up**
- **Battery-Operated Systems**
- **Portable Computers**
- **Level Detectors**

### ORDERING INFORMATION

| Part Number  | Temperature Range                                | Package        |
|--------------|--|----------------|
| ICL7665SCBA  | 0 $^{\circ}\text{C}$ to +70 $^{\circ}\text{C}$   | 8 Lead SOIC    |
| ICL7665SCPA  | 0 $^{\circ}\text{C}$ to +70 $^{\circ}\text{C}$   | 8 Lead Minidip |
| ICL7665SCJA  | 0 $^{\circ}\text{C}$ to +70 $^{\circ}\text{C}$   | 8 Lead Cerdip  |
| ICL7665SACPA | 0 $^{\circ}\text{C}$ to +70 $^{\circ}\text{C}$   | 8 Lead Minidip |
| ICL7665SACJA | 0 $^{\circ}\text{C}$ to +70 $^{\circ}\text{C}$   | 8 Lead Cerdip  |
| ICL7665SIBA  | -25 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$ | 8 Lead SOIC    |
| ICL7665SIPA  | -25 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$ | 8 Lead Minidip |
| ICL7665SIJA  | -25 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$ | 8 Lead Cerdip  |
| ICL7665SAIPA | -25 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$ | 8 lead Minidip |
| ICL7665SAIJA | -25 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$ | 8 Lead Cerdip  |

HARRIS SEMICONDUCTOR'S SOLE AND EXCLUSIVE WARRANTY OBLIGATION WITH RESPECT TO THIS PRODUCT SHALL BE THAT STATED IN THE WARRANTY ARTICLE OF THE CONDITION OF SALE. THE WARRANTY SHALL BE EXCLUSIVE AND SHALL BE IN LIEU OF ALL OTHER WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR USE.

NOTE: All typical values have been characterized but are not tested.

# ICL7665S

## ABSOLUTE MAXIMUM RATINGS

|   |   |
|---|---|
| Supply Voltage (Note 2)   | -0.3V to +18V                           |
| Output Voltages OUT1 and OUT2 (with respect to GND)<br>(Note 2)               | -0.3V to +18V                           |
| Output Voltages HYST1 and HYST2 (with respect to V <sup>+</sup> )<br>(Note 2) | -0.3V to +18V                           |
| Input Voltages SET1 and SET2<br>(Note 2)                                      | (GND - 0.3V) to (V <sup>+</sup> + 0.3V) |
| Maximum Sink Output OUT1 and OUT2   | 25 mA                                   |
| Maximum Source Output Current<br>HYST1 and HYST2                              | -25 mA                                  |

|                                      |                |
|--------------------------------------|----------------|
| Lead Temperature (Soldering, 10 sec) | +300°C         |
| Storage Temperature Range            | -65°C to 150°C |
| Operating Temperature Range          |                |
| ICL7665SC                            | 0°C to +70°C   |
| ICL7665SI                            | -25°C to +85°C |
| Total Power Dissipation (Note 1)     |                |
| SOIC                                 | 200 mW         |
| Minidip                              | 200 mW         |
| CERDIP                               | 500 mW         |

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

The specifications below are applicable to both the ICL7665S and ICL7665SA unless otherwise stated. V<sup>+</sup> = 5V, T<sub>A</sub> = +25°C, Test Circuit Figure 3 unless otherwise stated.

| Symbol  | Parameter   | Test Conditions  | Limits       |             |              | Units |  |
|---|---|--|--------------|-------------|--------------|-------|--|
|   |   |  | Min          | Typ         | Max          |       |  |
| V <sup>+</sup>  | <b>Operating Supply Voltage</b>                                     | ICL7665S   |              |             |              |       |  |
|   |   | T <sub>A</sub> = 25°C  | 1.6          |             | 16           | V     |  |
|   |   | 0°C ≤ T <sub>A</sub> ≤ +70°C   | 1.8          |             | 16           | V     |  |
|   |   | -25°C ≤ T <sub>A</sub> ≤ +85°C   | 1.8          |             | 16           | V     |  |
|   |   | <b>ICL7665SA</b>   |              |             |              |       |  |
|   |   | 0°C ≤ T <sub>A</sub> ≤ +70°C   | <b>1.8</b>   |             | 16           | V     |  |
|   |   | -25°C ≤ T <sub>A</sub> ≤ +85°C   | <b>1.8</b>   |             | 16           | V     |  |
| I <sup>+</sup>  | <b>Supply Current</b>   | GND ≤ V <sub>SET1</sub> , V <sub>SET2</sub> ≤ V <sup>+</sup><br>All Outputs Open Circuit<br>0°C ≤ T <sub>A</sub> ≤ +70°C<br>V <sup>+</sup> = 2V<br>V <sup>+</sup> = 9V<br>V <sup>+</sup> = 15V<br>-25°C ≤ T <sub>A</sub> ≤ +85°C |              | 2.5         | 10           | μA    |  |
|   |   | V <sup>+</sup> = 2V  |              | 2.6         | 10           | μA    |  |
|   |   | V <sup>+</sup> = 9V  |              | 2.9         | <b>10</b>    | μA    |  |
|   |   | V <sup>+</sup> = 15V   |              |             |              |       |  |
|   |   | V <sup>+</sup> = 2V  |              | 2.5         | <b>10</b>    | μA    |  |
|   |   | V <sup>+</sup> = 9V  |              | 2.6         | <b>10</b>    | μA    |  |
|   | V <sup>+</sup> = 15V  |  | <b>2.9</b>   | <b>10</b>   | μA           |       |  |
| V <sub>SET1</sub><br>V <sub>SET2</sub>                      | <b>Input Trip Voltage</b>   | ICL7665S   | 1.15         | 1.3         | 1.45         | V     |  |
|   |   |  | 1.2          | 1.3         | 1.4          | V     |  |
|   |   | ICL7665SA  |              |             |              |       |  |
|   |   |  | <b>1.275</b> | <b>1.30</b> | <b>1.325</b> | V     |  |
|   |   |  |              |             |              |       |  |
|   |   |  | <b>1.225</b> | <b>1.30</b> | <b>1.375</b> | V     |  |
| $\frac{\Delta V_{SET}}{\Delta T}$                           | <b>Temperature Coefficient of V<sub>SET</sub></b>                   | ICL7665S   |              | <b>200</b>  |              | ppm   |  |
|   |   | <b>ICL7665SA</b>   |              | <b>100</b>  |              | ppm   |  |
| $\frac{\Delta V_{SET}}{\Delta V_S}$                         | Supply Voltage Sensitivity of V <sub>SET1</sub> , V <sub>SET2</sub> | R <sub>OUT1</sub> , R <sub>OUT2</sub> , R <sub>HYST1</sub> , R <sub>HYST2</sub> = 1 MΩ<br>2V ≤ V <sup>+</sup> ≤ 10V  |              | 0.03        |              | %/V   |  |
| I <sub>OLK</sub><br>I <sub>HLK</sub>                        | Output Leakage Currents of OUT and HYST                             | V <sub>SET</sub> = 0V or V <sub>SET</sub> ≥ 2V   |              | 10          | 200          | nA    |  |
|   |   |  |              | -10         | -100         | nA    |  |
|   |   | V <sup>+</sup> = 15V, T <sub>A</sub> = 70°C  |              |             | 2000         | nA    |  |
|   |   |  |              | -500        |              |       |  |
| V <sub>OUT1</sub><br>V <sub>OUT1</sub><br>V <sub>OUT1</sub> | Output Saturation Voltages  | V <sub>SET1</sub> = 2V, I <sub>OUT1</sub> = 2 mA   |              |             |              |       |  |
|   |   | V <sup>+</sup> = 2V  |              | 0.2         | 0.5          | V     |  |
|   |   | V <sup>+</sup> = 5V  |              | 0.1         | 0.3          | V     |  |
|   |   | V <sup>+</sup> = 15V   |              | 0.06        | 0.2          | V     |  |

NOTE: All typical values have been characterized but are not tested.

# ICL7665S

## ELECTRICAL CHARACTERISTICS

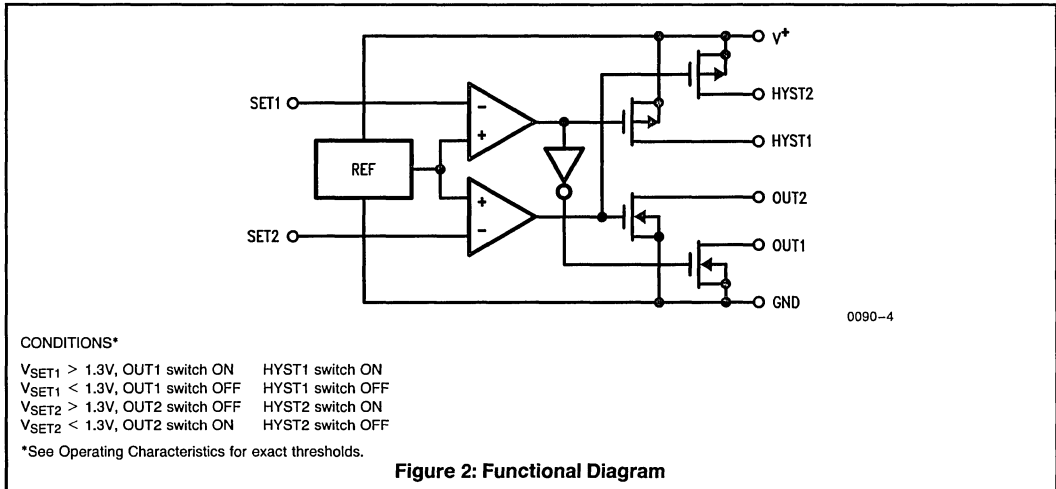
The specifications below are applicable to both the ICL7665S and ICL7665SA unless otherwise stated.  $V^+ = 5V$ ,  $T_A = +25^\circ\text{C}$ , Test Circuit Figure 3 unless otherwise stated. (Continued)

| Symbol                                    | Parameter                                 | Test Conditions  | Limits |                         |                         | Units       |
|---|---|--|--------|-------------------------|-------------------------|-------------|
|   |   |  | Min    | Typ                     | Max                     |             |
| $V_{HYST1}$<br>$V_{HYST1}$<br>$V_{HYST1}$ | Output Saturation Voltages                | $V_{SET1} = 2V, I_{HYST1} = -0.5\text{ mA}$<br>$V^+ = 2V$<br>$V^+ = 5V$<br>$V^+ = 15V$   |        | -0.15<br>-0.05<br>-0.02 | -0.30<br>-0.15<br>-0.10 | V<br>V<br>V |
| $V_{OUT2}$<br>$V_{OUT2}$<br>$V_{OUT2}$    | Output Saturation Voltages                | $V_{SET2} = 0V, I_{OUT2} = 2\text{ mA}$<br>$V^+ = 2V$<br>$V^+ = 5V$<br>$V^+ = 15V$   |        | 0.2<br>0.15<br>0.11     | 0.5<br>0.3<br>0.25      | V<br>V<br>V |
| $V_{HYST2}$<br>$V_{HYST2}$                | Output Saturation Voltages                | $V_{SET2} = 2V$<br>$V^+ = 2V, I_{HYST2} = -0.2\text{ mA}$<br>$V^+ = 5V, I_{HYST2} = -0.5\text{ mA}$<br>$V^+ = 15V, I_{HYST2} = -0.5\text{ mA}$     |        | -0.25<br>-0.43<br>-0.35 | -0.8<br>-1.0<br>-0.8    | V           |
| $I_{SET}$                                 | $V_{SET}$ Input Leakage Current           | $GND \leq V_{SET} \leq V^+$  |        | 0.01                    | 10                      | nA          |
| $\Delta V_{SET}$                          | $\Delta$ Input for Complete Output Change | $R_{OUT} = 4.7\text{ k}\Omega, R_{HYST} = 20\text{ k}\Omega$<br>$V_{OUTLO} = 1\% V^+, V_{OUTHI} = 99\% V^+$<br><i>ICL7665S</i><br><i>ICL7665SA</i> |        | 1.0<br>0.1              |                         | mV<br>mV    |
| $V_{SET1} - V_{SET2}$                     | Difference in Trip Voltages               | $R_{OUT}, R_{HYST} = 1\text{ M}\Omega$   |        | $\pm 5$                 | $\pm 50$                | mV          |
|   | <i>Output/Hysteresis Difference</i>       | $R_{OUT}, R_{HYST} = 1\text{ M}\Omega$<br><i>ICL7665S</i><br><i>ICL7665SA</i>  |        | $\pm 1$<br>$\pm 0.1$    |                         | mV<br>mV    |

**NOTE 1:** Derate above  $+25^\circ\text{C}$  ambient temperature at  $4\text{ mW}/^\circ\text{C}$ .

**2:** Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than  $(V^+ + 0.3V)$  or less than  $(GND - 0.3V)$  may cause destructive device latchup. For these reasons, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665S be turned on first. If this is not possible, currents into inputs and/or outputs must be limited to  $\pm 0.5\text{ mA}$  and voltages must not exceed those defined above.

**3:** All significant improvements over the industry-standard ICL7665 are highlighted in bold italics.





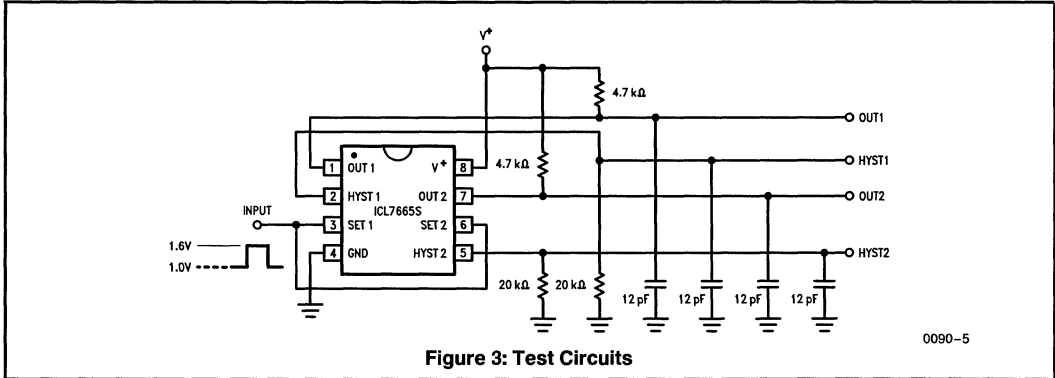


Figure 3: Test Circuits

0090-5

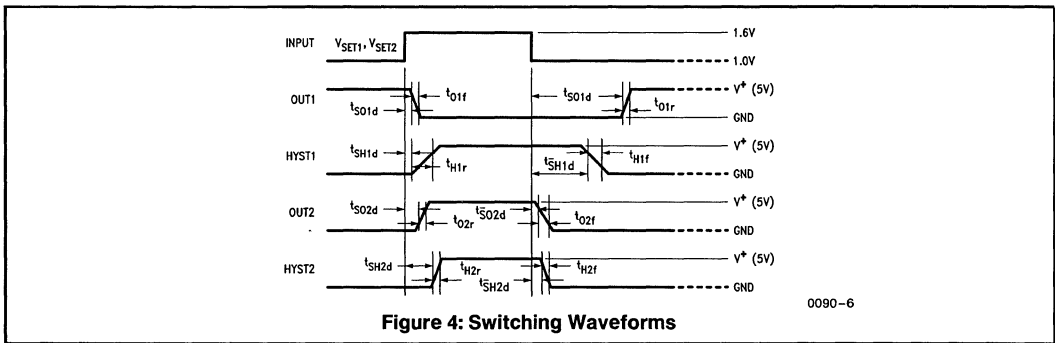


Figure 4: Switching Waveforms

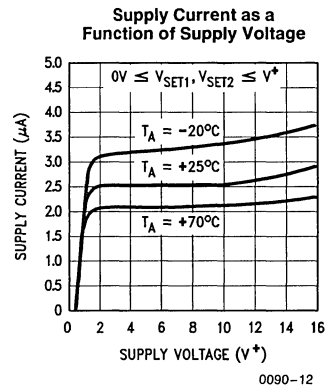
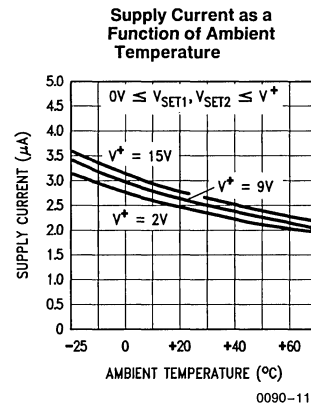
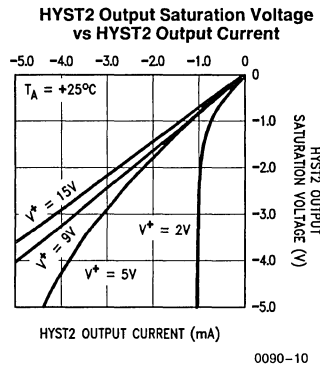
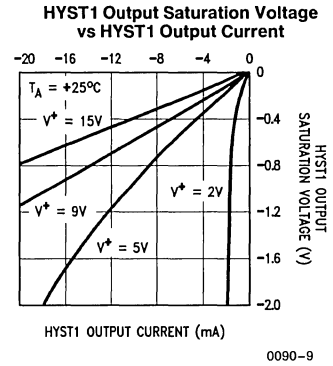
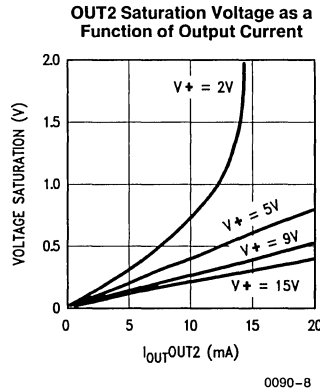
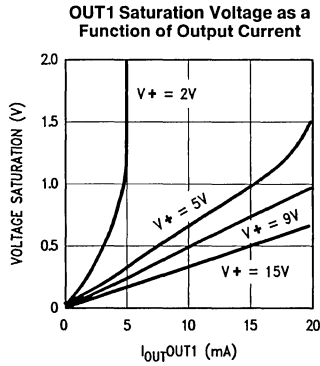
0090-6

## A.C. ELECTRICAL CHARACTERISTICS

| Symbol   | Parameter                            | Test Conditions   | Limits |                          |     | Units         |
|--|--------------------------------------|---|--------|--------------------------|-----|---------------|
|  |                                      |   | Min    | Typ                      | Max |               |
| $t_{SO1d}$<br>$t_{SH1d}$<br>$t_{SO2d}$<br>$t_{SH2d}$ | Output Delay Times<br>Input Going HI | $V_{SET}$ Switched between 1.0V to 1.6V<br>$R_{OUT} = 4.7\text{ k}\Omega$ , $C_L = 12\text{ pF}$<br>$R_{HYST} = 20\text{ k}\Omega$ , $C_L = 12\text{ pF}$ |        | 85<br>90<br>55<br>55     |     | $\mu\text{S}$ |
| $t_{SO1d}$<br>$t_{SH1d}$<br>$t_{SO2d}$<br>$t_{SH2d}$ | Input Going LO                       | $V_{SET}$ Switched between 1.6V to 1.0V<br>$R_{OUT} = 4.7\text{ k}\Omega$ , $C_L = 12\text{ pF}$<br>$R_{HYST} = 20\text{ k}\Omega$ , $C_L = 12\text{ pF}$ |        | 75<br>80<br>60<br>60     |     | $\mu\text{S}$ |
| $t_{O1r}$<br>$t_{O2r}$<br>$t_{H1r}$<br>$t_{H2r}$     | Output Rise Times                    | $V_{SET}$ Switched between 1.0V to 1.6V<br>$R_{OUT} = 4.7\text{ k}\Omega$ , $C_L = 12\text{ pF}$<br>$R_{HYST} = 20\text{ k}\Omega$ , $C_L = 12\text{ pF}$ |        | 0.6<br>0.8<br>7.5<br>0.7 |     | $\mu\text{S}$ |
| $t_{O1f}$<br>$t_{O2f}$<br>$t_{H1f}$<br>$t_{H2f}$     | Output Fall Times                    | $V_{SET}$ Switched between 1.0V to 1.6V<br>$R_{OUT} = 4.7\text{ k}\Omega$ , $C_L = 12\text{ pF}$<br>$R_{HYST} = 20\text{ k}\Omega$ , $C_L = 12\text{ pF}$ |        | 0.6<br>0.7<br>4<br>1.8   |     | $\mu\text{S}$ |

NOTE: All typical values have been characterized but are not tested.

## Typical Performance Characteristics



## DETAILED DESCRIPTION

As shown in the Functional Diagram, Figure 2, the ICL7665S consists of two comparators which compare input voltages on the SET1 and SET2 terminals to an internal 1.3V band-gap reference. The outputs from the two comparators drive open-drain N-channel transistors for OUT1 and OUT2, and open-drain P-channel transistors for HYST1 and HYST2 outputs. Each section, the Under-Voltage Detector and the Over-Voltage Detector, is independent of the other, although both use the internal 1.3V reference. The offset voltages of the two comparators will normally be unequal so  $V_{SET1}$  will generally not quite equal  $V_{SET2}$ .

The input impedances of the SET1 and SET2 pins are extremely high, and for most practical applications can be ignored. The four outputs are open-drain MOS transistors, and when ON behave as low resistance switches to their respective supply rails. This minimizes errors in setting-up the hysteresis, and maximizes the output flexibility. The operating currents of the bandgap reference and the comparators are around 100 nA each.

## PRECAUTIONS

Junction-isolated CMOS devices like the ICL7665S have an inherent SCR or 4-layer PNP structure distributed throughout the die. Under certain circumstances, this can be triggered into a potentially destructive high-current mode. This latchup can be triggered by forward-biasing an input or output with respect to the power supply, or by applying excessive supply voltages. In very-low current analog circuits, such as the ICL7665S, this SCR can also be triggered by applying the input power supply extremely rapidly ("instantaneously"), e.g. through a low impedance battery and an ON/OFF switch with short lead lengths. The rate-of-rise of the supply voltage can exceed  $100\text{ V}/\mu\text{s}$  in such a circuit. A low-impedance capacitor (e.g.,  $0.05\ \mu\text{F}$  disc ceramic) between the  $V^+$  and GROUND pins of the ICL7665S can be used to reduce the rate-of-rise of the supply voltage in battery applications. In line-operated systems, the rate-of-rise of the supply is limited by other considerations, and is normally not a problem.

# ICL7665S

If the SET voltages must be applied before the supply voltage  $V^+$ , the input current should be limited to less than 0.5 mA by appropriate external resistors, usually required for voltage setting anyway. A similar precaution should be taken with the outputs if it is likely that they will be driven by other circuits to levels outside the supplies at any time. See M011 for some other protection ideas.

## SIMPLE THRESHOLD DETECTOR

Figure 5 shows the simplest connection of the ICL7665S for threshold detection. From the graph (b), it can be seen that at low input voltages OUT1 is OFF, or high, while OUT2 is ON, or low. As the input rises (e.g., at power-on) toward  $V_{NOM}$  (usually the eventual operating voltage), OUT2 goes high on reaching  $V_{TR2}$ . If the voltage rises above  $V_{NOM}$  as much as  $V_{TR1}$ , OUT1 goes low. The equations giving  $V_{SET1}$  and  $V_{SET2}$  are from Figure 5(a):

$$V_{SET1} = V_{IN} \frac{R_{11}}{(R_{11} + R_{21})}; V_{SET2} = V_{IN} \frac{R_{12}}{(R_{12} + R_{22})}$$

Since the voltage to trip each comparator is nominally 1.3V, the value  $V_{IN}$  for each trip point can be found from

$$V_{TR1} = V_{SET1} \frac{(R_{11} + R_{21})}{R_{11}} = 1.3 \frac{(R_{11} + R_{21})}{R_{11}} \text{ for detector 1}$$

and

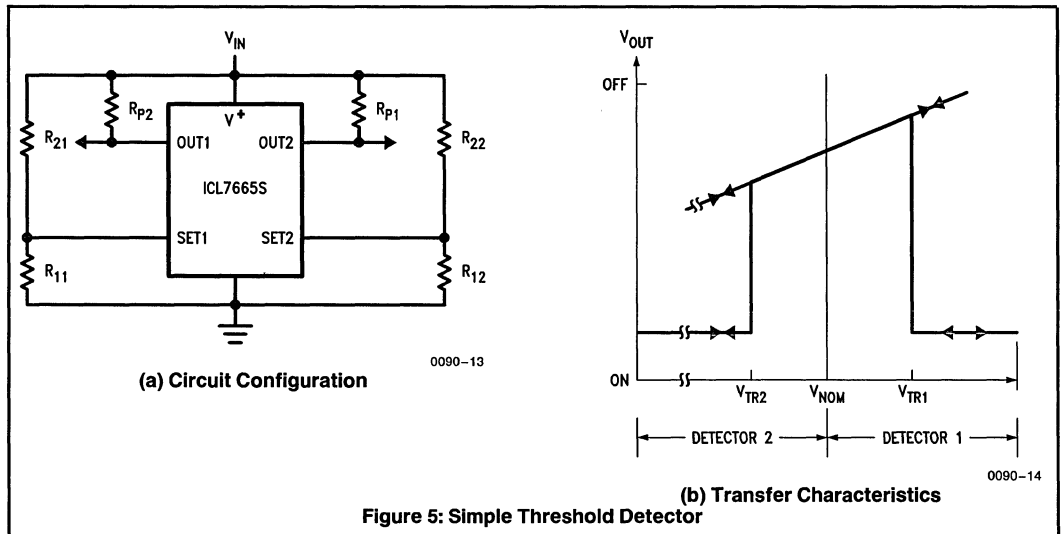
$$V_{TR2} = V_{SET2} \frac{(R_{12} + R_{22})}{R_{12}} = 1.3 \frac{(R_{12} + R_{22})}{R_{12}} \text{ for detector 2}$$

Either detector may be used alone, as well as both together, in any of the circuits shown here.

When  $V_{IN}$  is very close to one of the trip voltages, normal variations and noise may cause it to wander back and forth across this level, leading to erratic output ON and OFF conditions. The addition of hysteresis, making the trip points slightly different for rising and falling inputs, will avoid this condition.

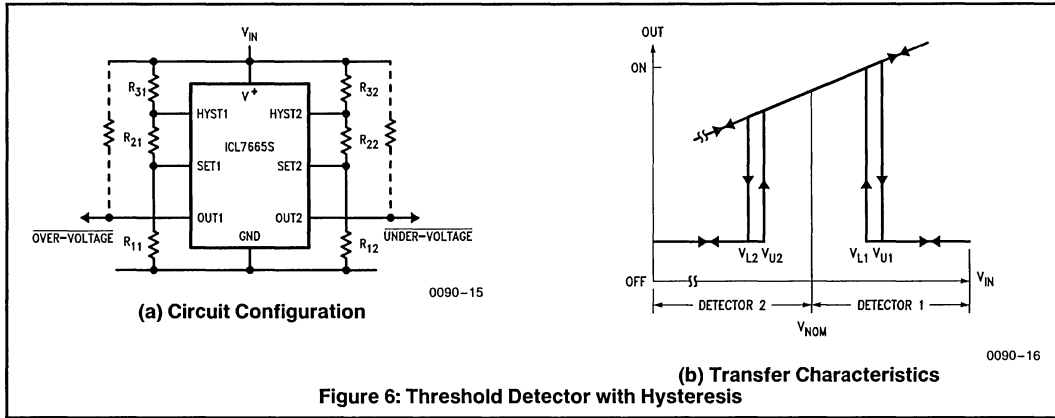
## THRESHOLD DETECTOR WITH HYSTERESIS

Figure 6(a) shows how to set up such hysteresis, while Figure 6(b) shows how the hysteresis around each trip point produces switching action at different points depending on whether  $V_{IN}$  is rising or falling (the arrows indicate direction of change). The HYST outputs are basically switches which short out  $R_{31}$  or  $R_{32}$  when  $V_{IN}$  is above the respective trip point. Thus if the input voltage rises from a low value, the trip point will be controlled by  $R_{1n}$ ,  $R_{2n}$ , and  $R_{3n}$ , until the trip point is reached. As this value is passed, the detector changes state,  $R_{3n}$  is shorted out, and the trip point becomes controlled by only  $R_{1n}$  and  $R_{2n}$ , a lower value. The input will then have to fall to this new point to restore the



NOTE: All typical values have been characterized but are not tested.

## APPLICATIONS



**Table 1: Set-Point Equations**

**a) NO HYSTERESIS**

$$\text{Over-Voltage } V_{TRIP} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$$

$$\text{Over-Voltage } V_{TRIP} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$$

**b) HYSTERESIS PER FIGURE 6A**

$$V_{U1} = \frac{R_{11} + R_{21} + R_{31}}{R_{11}} \times V_{SET1}$$

Over-Voltage  $V_{TRIP}$

$$V_{L1} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$$

$$V_{U2} = \frac{R_{12} + R_{22} + R_{32}}{R_{12}} \times V_{SET2}$$

Under-Voltage  $V_{TRIP}$

$$V_{L2} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$$

**c) HYSTERESIS PER FIGURE 7**

$$V_{U1} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$$

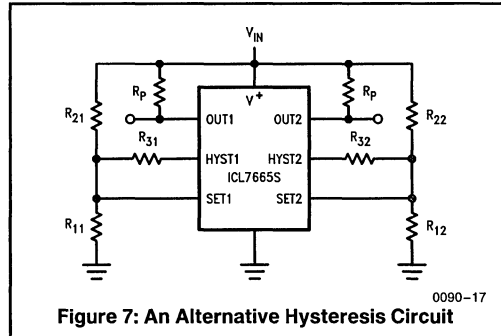
Over-Voltage  $V_{TRIP}$

$$V_{L1} = \frac{R_{11} + \frac{R_{21}R_{31}}{R_{21} + R_{31}}}{R_{11}} \times V_{SET1}$$

$$V_{U2} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$$

Over-Voltage  $V_{TRIP}$

$$V_{L2} = \frac{R_{12} + \frac{R_{22}R_{32}}{R_{22} + R_{32}}}{R_{12}} \times V_{SET2}$$



*NOTE: All typical values have been characterized but are not tested.*

## THRESHOLD DETECTOR WITH HYSTERESIS (Continued)

initial comparator state, but as soon as this occurs, the trip point will be raised again.

An alternative circuit for obtaining hysteresis is shown in Figure 7. In this configuration, the HYST pins put the extra resistor in parallel with the upper setting resistor. The values of the resistors differ, but the action is essentially the same. The governing equations are given in Table 1. These ignore the effects of the resistance of the HYST outputs, but these can normally be neglected if the resistor values are above about 100 k $\Omega$ .

## APPLICATIONS

### Single Supply Fault Monitor

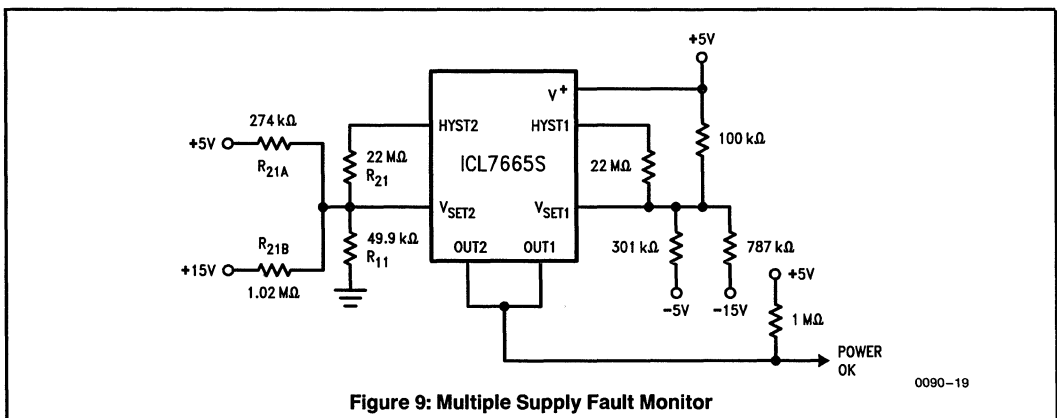
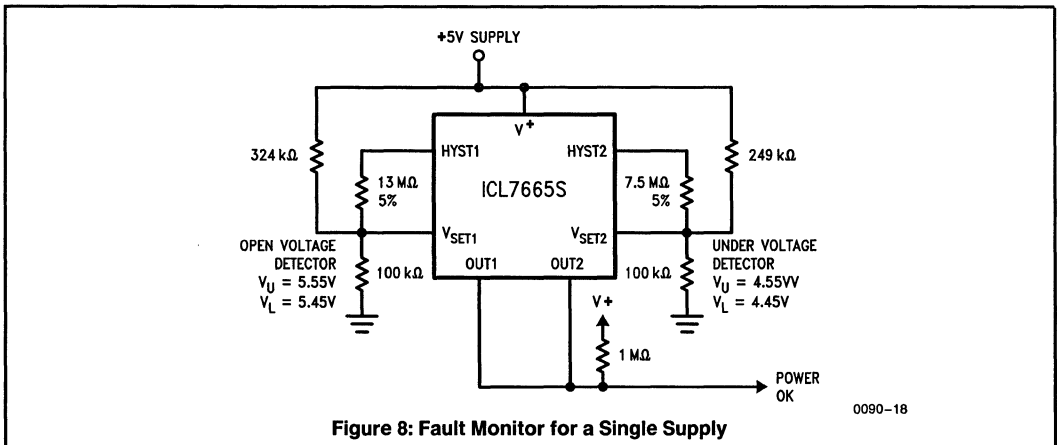
Figure 8 shows an over/under-voltage fault monitor for a single supply. The over-voltage trip point is centered around 5.5V and the under-voltage trip point is centered around 4.5V. Both have some hysteresis to prevent erratic output

ON and OFF conditions. The two outputs are connected in a wired OR configuration with a pullup resistor to generate a power OK signal.

### Multiple Supply Fault Monitor

The ICL7665S can simultaneously monitor several supplies when connected as shown in Figure 9. The resistors are chosen such that the sum of the currents through R<sub>21A</sub>, R<sub>21B</sub>, and R<sub>31</sub> is equal to the current through R<sub>11</sub> when the two input voltages are at the desired low voltage detection point. The current through R<sub>11</sub> at this point is equal to 1.3 V/R<sub>11</sub>. The voltage at the V<sub>SET</sub> input depends on the voltage of both supplies being monitored. The trip voltage of one supply while the other supply is at the nominal voltage will be different than the trip voltage when both supplies are below their nominal voltages.

The other side of the ICL7665S can be used to detect the absence of negative supplies. The trip points for OUT1 depend on both the negative supply voltages and the actual voltage of the +5V supply.



NOTE: All typical values have been characterized but are not tested.

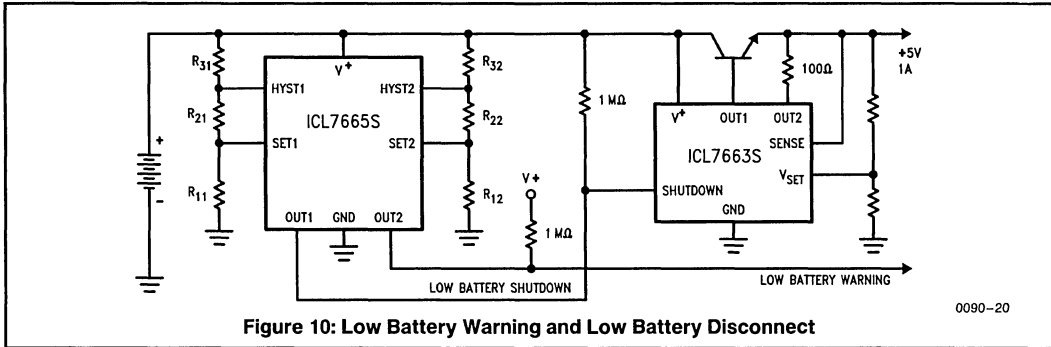


Figure 10: Low Battery Warning and Low Battery Disconnect

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## Combination Low Battery Warning and Low Battery Disconnect

When using rechargeable batteries in a system, it is important to keep the batteries from being overdischarged. The circuit shown in Figure 10 provides a low battery warning and also disconnects the low battery from the rest of the system to prevent damage to the battery. OUT1 is used to shutdown the ICL7663S when the battery voltage drops to the value where the load should be disconnected. As long as  $V_{SET1}$  is greater than 1.3V, OUT1 is low, but when  $V_{SET1}$  drops below 1.3V, OUT1 goes high, shutting off the ICL7663S. OUT2 is used for low battery warning. When  $V_{SET2}$  is greater than 1.3V, OUT2 is high and the low battery warning is on. When  $V_{SET2}$  drops below 1.3V, OUT2 is low and the low battery warning goes off. The trip voltage for low battery warning can be set higher than the trip voltage for shutdown to give advance low battery warning before the battery is disconnected.

## Power Fail Warning and Powerup/Powerdown Reset

Figure 11 shows a power fail warning circuit with powerup/powerdown reset. When the unregulated DC input is

above the trip point, OUT1 is low. When the DC input drops below the trip point, OUT1 shuts OFF and the power fail warning goes high. The voltage on the input of the 7805 decays at a rate of  $I_{OUT}/C$ . Since the 7805 will continue to provide 5V out at 1A until  $V_{IN}$  is less than 7.3V, this circuit will provide a certain amount of warning before the 5V output begins to drop.

The ICL7665S OUT2 is used to prevent a microprocessor from writing spurious data to a CMOS battery backup memory by causing OUT2 to go low when the 7805 5V output drops below the ICL7665S trip point.

## Simple High/Low Temperature Alarm

Figure 12 illustrates a simple high/low temperature alarm which uses the ICL7665S with an NPN transistor. The voltage at the top of  $R_1$  is determined by the  $V_{BE}$  of the transistor and the position of  $R_1$ 's wiper arm. This voltage has a negative temperature coefficient.  $R_1$  is adjusted so that  $V_{SET2}$  equals 1.3V when the NPN transistor's temperature reaches the temperature selected for the high temperature alarm. When this occurs, OUT2 goes low.  $R_2$  is adjusted

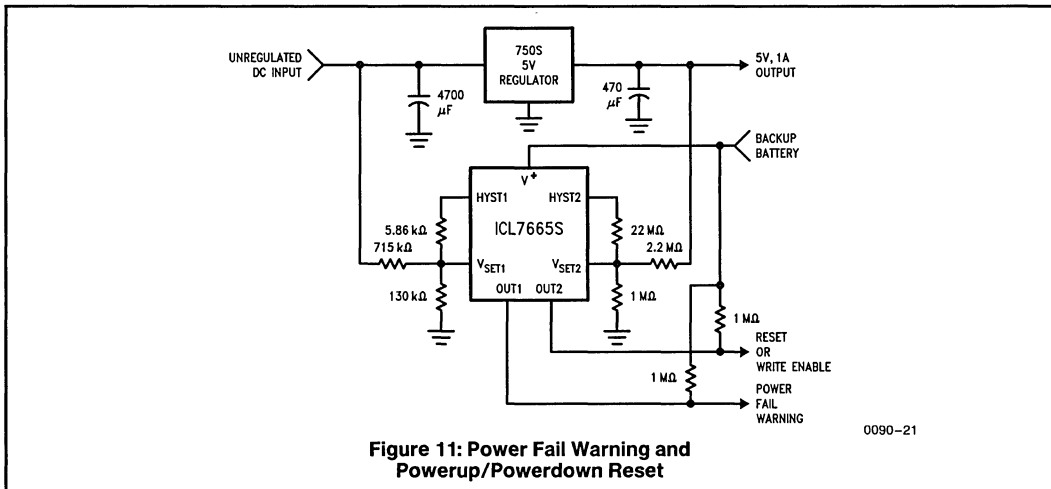
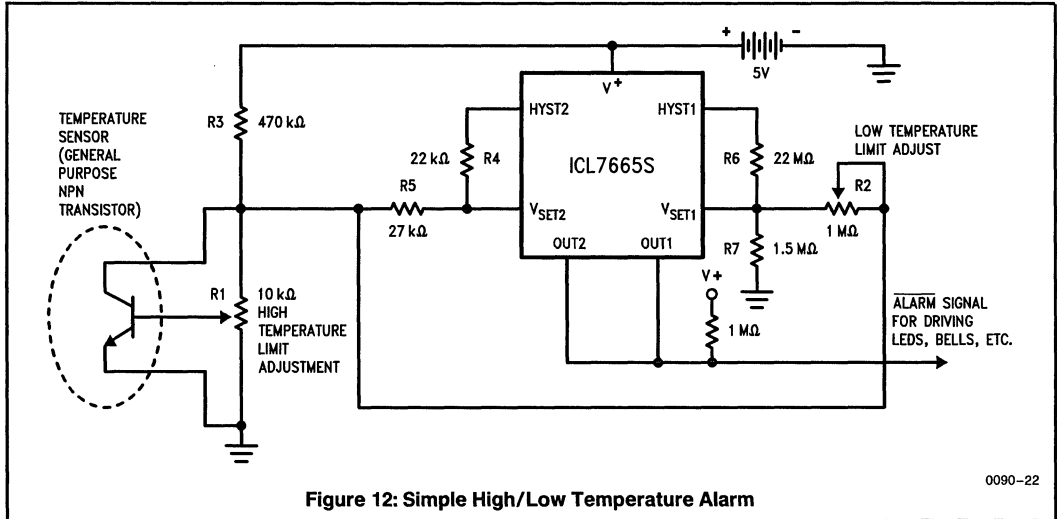


Figure 11: Power Fail Warning and Powerup/Powerdown Reset

0090-21

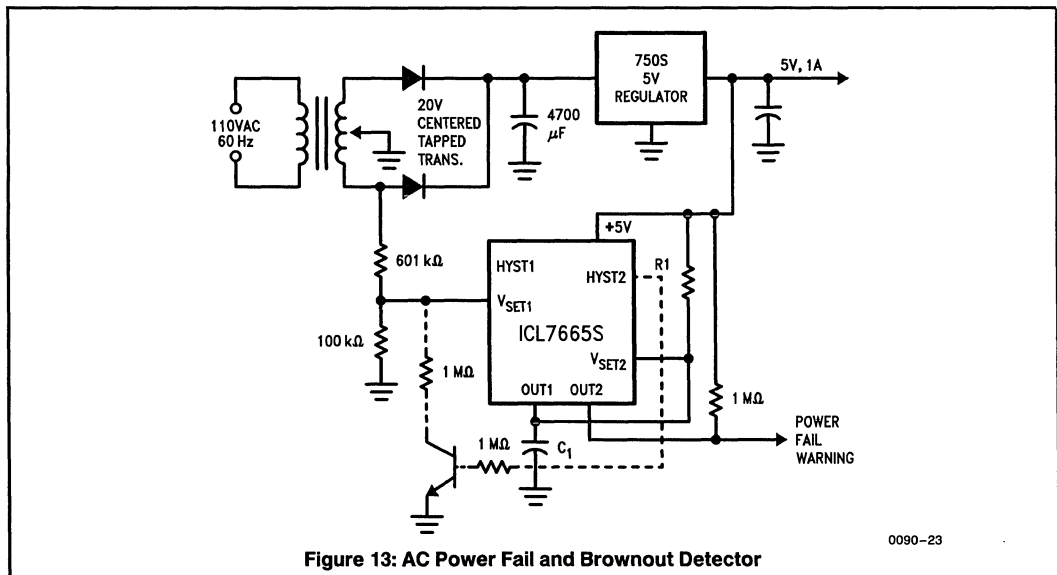


so that  $V_{SET1}$  equals 1.3V when the NPN transistor's temperature reaches the temperature selected for the low temperature alarm. When the temperature drops below this limit, OUT1 goes low.

### AC Power Fail and Brownout Detector

Figure 13 shows a circuit that detects AC undervoltage by monitoring the secondary side of the transformer. The capacitor,  $C_1$ , is charged through  $R_1$  when OUT1 is OFF. With a normal 110 VAC input to the transformer, OUT1 will dis-

charge  $C_1$  once every cycle, approximately every 16.7 ms. When the AC input voltage is reduced, OUT1 will stay OFF, so that  $C_1$  does not discharge. When the voltage on  $C_1$  reaches 1.3V, OUT2 turns OFF and the power fail warning goes high. The time constant,  $R_1C_1$ , is chosen such that it takes longer than 16.7 ms to charge  $C_1$  1.3V.



August 1991

### Features

- Fast Rise and Fall Times
  - ▶ 30ns with 1000pF Load
- Wide Supply Voltage Range
  - ▶  $V_{CC} = 4.5$  to 15V
- Low Power Consumption
  - ▶ 4mW with Inputs Low
  - ▶ 20mW with Inputs High
- TTL/CMOS Input Compatible Power Driver
  - ▶  $R_{OUT} = 7\Omega$  Typ
- Direct Interface with Common PWM Control ICs
- Pin Equivalent to DS0026/DS0056; TSC426

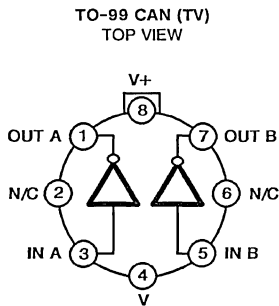
### Typical Applications

- Switching Power Supplies
- DC/DC Converters
- Motor Controllers

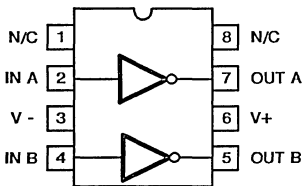
### Description

The ICL7667 is a dual monolithic high-speed driver designed to convert TTL level signals into high current outputs at voltages up to 15V. Its high speed and current output enable it to drive large capacitive loads with high slew rates and low propagation delays. With an output voltage swing only millivolts less than the supply voltage and a maximum supply voltage of 15V, the ICL7667 is well suited for driving power MOSFETs in high frequency switched-mode power converters. The ICL7667's high current outputs minimize power losses in the power MOSFETs by rapidly charging and discharging the gate capacitance. The ICL7667's inputs are TTL compatible and can be directly driven by common pulse-width modulation control ICs.

### Packages



8 LEAD DUAL-IN-LINE PACKAGE (PA, JA, BA)  
TOP VIEW

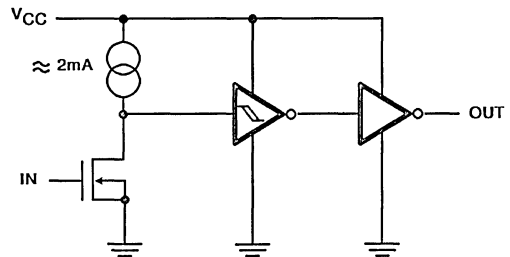


### Order Information

| PART NUMBER | TEMPERATURE RANGE | PACKAGE           |
|-------------|-------------------|-------------------|
| ICL7667CBA  | 0°C to +70°C      | 8 Pin SOIC        |
| ICL7667CPA  | 0°C to +70°C      | 8 Pin Plastic     |
| ICL7667CJA  | 0°C to +70°C      | 8 Pin Ceramic DIP |
| ICL7667CTV  | 0°C to +70°C      | TO-99 Can         |
| ICL7667MTV* | -55°C to +125°C   | TO-99 Can         |
| ICL7667MJA* | -55°C to +125°C   | 8 Pin Ceramic DIP |

\*Add /883B to Part Number for 883B Processing

### Functional Diagram





# ICL7667

## ABSOLUTE MAXIMUM RATINGS

|   |                                  |
|---|----------------------------------|
| Supply Voltage $V^+$ to $V^-$ .....                 | 15V                              |
| Input Voltage .....                                 | $(V^- - 0.3V)$ to $(V^+ + 0.3V)$ |
| Package Dissipation, $T_A = 25^\circ\text{C}$ ..... | 500mW                            |
| Linear Derating Factors                             |                                  |
| TO-99 .....   | Plastic .....                    |
| 6.7mW/ $^\circ\text{C}$ .....                       | 5.6mW/ $^\circ\text{C}$ .....    |
| above $50^\circ\text{C}$ .....                      | above $36^\circ\text{C}$ .....   |
| Cerdip .....  | 6.7mW/ $^\circ\text{C}$ .....    |
| above $50^\circ\text{C}$ .....                      | above $50^\circ\text{C}$ .....   |

|   |   |
|---|---|
| Storage Temperature .....                 | $-65^\circ\text{C}$ to $+150^\circ\text{C}$ |
| Operating Temperature Range               |   |
| ICL7667C .....                            | $0^\circ\text{C}$ to $+70^\circ\text{C}$    |
| ICL7667M .....                            | $-55^\circ\text{C}$ to $+125^\circ\text{C}$ |
| Lead Temperature (Soldering, 10sec) ..... | $300^\circ\text{C}$                         |

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

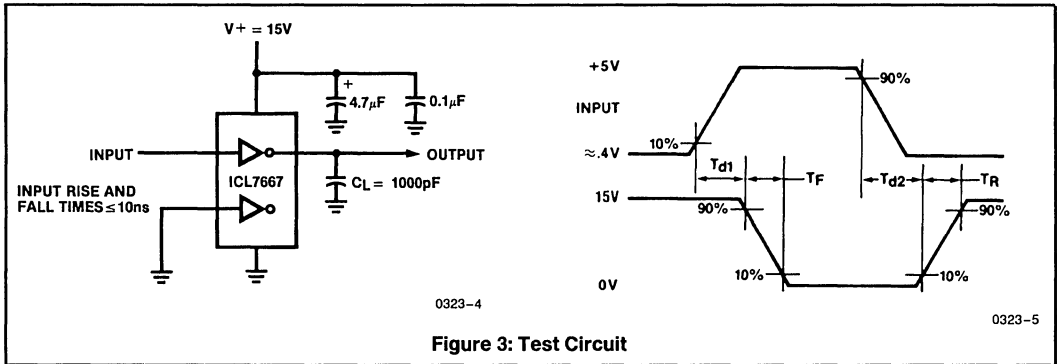
## ELECTRICAL CHARACTERISTICS (STATIC)

| Symbol    | Parameter             | Test Conditions   | ICL7667C,M               |          |      | ICL7667M   |     |     | Units         |
|-----------|-----------------------|---|--------------------------|----------|------|--|-----|-----|---------------|
|           |                       |   | $T_A = 25^\circ\text{C}$ |          |      | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ |     |     |               |
|           |                       |   | Min                      | Typ      | Max  | Min  | Typ | Max |               |
| $V_{IH}$  | Logic 1 Input Voltage | $V_{CC} = 4.5V$   | 2.0                      |          |      | 2.0  |     |     | V             |
| $V_{IH}$  | Logic 1 Input Voltage | $V_{CC} = 15V$  | 2.0                      |          |      | 2.0  |     |     | V             |
| $V_{IL}$  | Logic 0 Input Voltage | $V_{CC} = 4.5V$   |                          |          | 0.8  |  |     | 0.5 | V             |
| $V_{IL}$  | Logic 0 Input Voltage | $V_{CC} = 15V$  |                          |          | 0.8  |  |     | 0.8 | V             |
| $I_{IL}$  | Input Current         | $V_{CC} = 15V, V_{IN} = 0V$ and $15V$                   | -0.1                     |          | 0.1  | -0.1   |     | 0.1 | $\mu\text{A}$ |
| $V_{OH}$  | Output Voltage High   | $V_{CC} = 4.5V$ and $15V$                               | $V_{CC} - 0.05$          | $V_{CC}$ |      | $V_{CC} - 0.1$                                       |     |     | V             |
| $V_{OL}$  | Output Voltage Low    | $V_{CC} = 4.5V$ and $15V$                               |                          | 0        | 0.05 |  |     | 0.1 | V             |
| $R_{OUT}$ | Output Resistance     | $V_{IN} = V_{IL}, I_{OUT} = -10\text{mA}, V_{CC} = 15V$ |                          | 7        | 10   |  |     | 12  | $\Omega$      |
| $R_{OUT}$ | Output Resistance     | $V_{IN} = V_{IH}, I_{OUT} = 10\text{mA}, V_{CC} = 15V$  |                          | 8        | 12   |  |     | 13  | $\Omega$      |
| $I_{CC}$  | Power Supply Current  | $V_{CC} = 15V, V_{IN} = 3V$ both inputs                 |                          | 5        | 7    |  |     | 8   | mA            |
| $I_{CC}$  | Power Supply Current  | $V_{CC} = 15V, V_{IN} = 0V$ both inputs                 |                          | 150      | 400  |  |     | 400 | $\mu\text{A}$ |

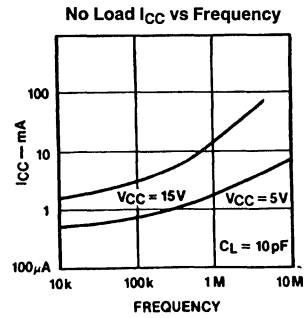
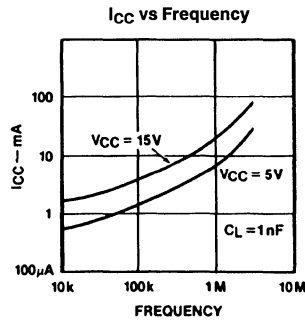
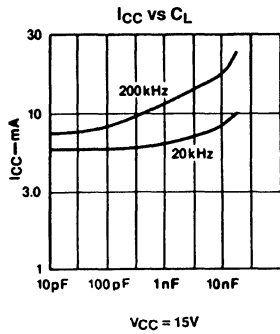
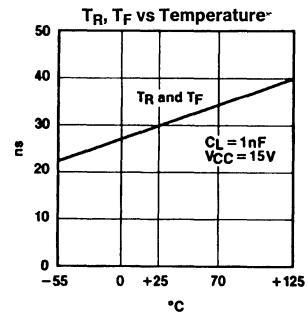
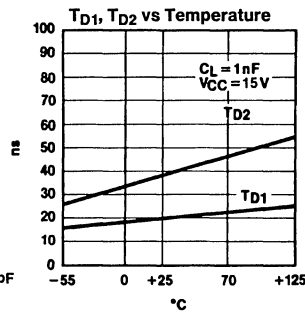
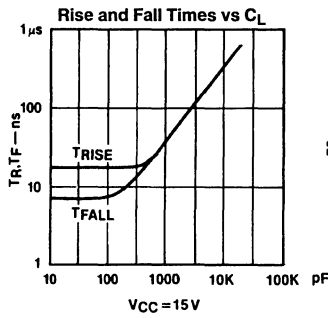
## ELECTRICAL CHARACTERISTICS (DYNAMIC)

| Symbol   | Parameter  | Test Conditions | ICL7667C,M               |     |     | ICL7667M   |     |     | Units |
|----------|------------|-----------------|--------------------------|-----|-----|--|-----|-----|-------|
|          |            |                 | $T_A = 25^\circ\text{C}$ |     |     | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ |     |     |       |
|          |            |                 | Min                      | Typ | Max | Min  | Typ | Max |       |
| $T_{D2}$ | Delay Time | Figure 3        |                          | 35  | 50  |  |     | 60  | ns    |
| $T_R$    | Rise Time  | Figure 3        |                          | 20  | 30  |  |     | 40  | ns    |
| $T_F$    | Fall Time  | Figure 3        |                          | 20  | 30  |  |     | 40  | ns    |
| $T_{D1}$ | Delay Time | Figure 3        |                          | 20  | 30  |  |     | 40  | ns    |

NOTE: All typical values have been characterized but are not tested.



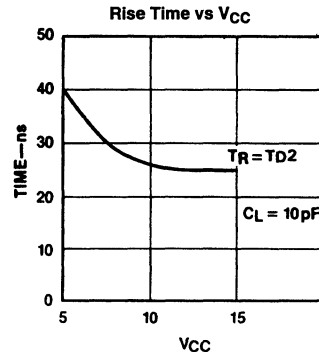
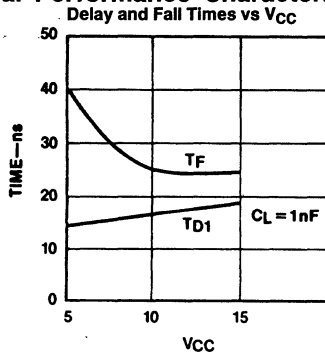
## Typical Performance Characteristics



0323-6

NOTE: All typical values have been characterized but are not tested.

## Typical Performance Characteristics (Continued)



0323-12

0323-13

## DETAILED DESCRIPTION

The ICL7667 is a dual high-power CMOS inverter whose inputs respond to TTL levels while the outputs can swing as high as 15V. Its high output current enables it to rapidly charge and discharge the gate capacitance of power MOS-FETs, minimizing the switching losses in switchmode power supplies. Since the output stage is CMOS, the output will swing to within millivolts of both ground and  $V_{CC}$  without any external parts or extra power supplies as required by the DS0026/56 family. Although most specifications are at  $V_{CC} = 15V$ , the propagation delays and specifications are almost independent of  $V_{CC}$ .

In addition to power MOS drivers, the ICL7667 is well suited for other applications such as bus, control signal, and clock drivers on large memory of microprocessor boards, where the load capacitance is large and low propagation delays are required. Other potential applications include peripheral power drivers and charge-pump voltage inverters.

### INPUT STAGE

The input stage is a large N-channel FET with a P-channel constant-current source. This circuit has a threshold of about 1.5V, relatively independent of the  $V_{CC}$  voltage. This means that the inputs will be directly compatible with TTL over the entire 4.5–15V  $V_{CC}$  range. Being CMOS, the inputs draw less than  $1\mu A$  of current over the entire input voltage range of ground to  $V_{CC}$ . The quiescent current or no load supply current of the ICL7667 is affected by the input voltage, going to nearly zero when the inputs are at the 0 logic level and rising to 7mA maximum when both inputs are at the 1 logic level. A small amount of hysteresis, about 50–100mV at the input, is generated by positive feedback around the second stage.

### OUTPUT STAGE

The ICL7667 output is a high-power CMOS inverter, swinging between ground and  $V_{CC}$ . At  $V_{CC} = 15V$ , the output impedance of the inverter is typically  $7\Omega$ . The high peak current capability of the ICL7667 enables it to drive a 1000pF load with a rise time of only 40ns. Because the output stage impedance is very low, up to 300mA will flow through the series N- and P-channel output devices (from  $V_{CC}$  to ground) during output transitions. This crossover current is responsible for a significant portion of the internal

power dissipation of the ICL7667 at high frequencies. It can be minimized by keeping the rise and fall times of the input to the ICL7667 below  $1\mu s$ .

## APPLICATION NOTES

Although the ICL7667 is simply a dual level-shifting inverter, there are several areas to which careful attention must be paid.

### GROUNDING

Since the input and the high current output current paths both include the ground pin, it is very important to minimize any common impedance in the ground return. Since the ICL7667 is an inverter, any common impedance will generate negative feedback, and will degrade the delay, rise and fall times. Use a ground plane if possible, or use separate ground returns for the input and output circuits. To minimize any common inductance in the ground return, separate the input and output circuit ground returns as close to the ICL7667 as is possible.

### BYPASSING

The rapid charging and discharging of the load capacitance requires very high current spikes from the power supplies. A parallel combination of capacitors that has a low impedance over a wide frequency range should be used. A  $4.7\mu F$  tantalum capacitor in parallel with a low inductance  $0.1\mu F$  capacitor is usually sufficient bypassing.

### OUTPUT DAMPING

Ringing is a common problem in any circuit with very fast rise or fall times. Such ringing will be aggravated by long inductive lines with capacitive loads. Techniques to reduce ringing include:

- 1) Reduce inductance by making printed circuit board traces as short as possible.
- 2) Reduce inductance by using a ground plane or by closely coupling the output lines to their return paths.
- 3) Use a 10 to  $30\Omega$  resistor in series with the output of the ICL7667. Although this reduces ringing, it will also slightly increase the rise and fall times.
- 4) Use good bypassing techniques to prevent supply voltage ringing.

NOTE: All typical values have been characterized but are not tested.

## POWER DISSIPATION

The power dissipation of the ICL7667 has three main components:

- 1) Input inverter current loss
- 2) Output stage crossover current loss
- 3) Output stage  $I^2R$  power loss

The sum of the above must stay within the specified limits for reliable operation.

As noted above, the input inverter current is input voltage dependent, with an  $I_{CC}$  of 0.2mA maximum with a logic 0 input and 6mA maximum with a logic 1 input.

The output stage crowbar current is the current that flows through the series N- and P-channel devices that form the output. This current, about 300mA, occurs only during output transitions. **Caution:** The inputs should never be allowed to remain between  $V_{IL}$  and  $V_{IH}$  since this could leave the output stage in a high current mode, rapidly leading to destruction of the device. If only one of the drivers is being used, be sure to tie the unused input to a ground. **NEVER** leave an input floating. The average supply current drawn by the output stage is frequency dependent, as can be seen in  $I_{CC}$  vs. Frequency graph in the Typical Characteristics Graphs.

The output stage  $I^2R$  power dissipation is nothing more than the product of the output current times the voltage drop across the output device. In addition to the current drawn by any resistive load, there will be an output current due to the charging and discharging of the load capacitance. In most high frequency circuits the current used to charge and discharge capacitance dominates, and the power dissipation is approximately

$$P_{AC} = CV_{CC}^2f$$

Where C = Load Capacitance

f = Frequency

In cases where the load is a power MOSFET and the gate drive requirements are described in terms of gate charge, the ICL7667 power dissipation will be

$$P_{AC} = Q_G V_{CC} f$$

Where  $Q_G$  = Charge required to switch the gate, in Coulombs.

f = Frequency

## POWER MOS DRIVER CIRCUITS

### POWER MOS DRIVER REQUIREMENTS

Because it has a very high peak current output, the ICL7667 excels at driving the gate of power MOS devices. The high current output is important since it minimizes the time the power MOS device is in the linear region. Figure 4 is a typical curve of charge vs. gate voltage for a power MOSFET. The flat region is caused by the Miller capacitance, where the drain-to-gate capacitance is multiplied by the voltage gain of the FET. This increase in capacitance occurs while the power MOSFET is in the linear region and

is dissipating significant amounts of power. The very high current output of the ICL7667 is able to rapidly overcome this high capacitance and quickly turns the MOSFET fully on or off.

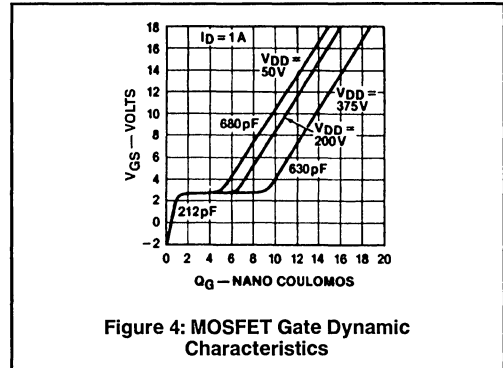


Figure 4: MOSFET Gate Dynamic Characteristics

## DIRECT DRIVE OF MOSFETS

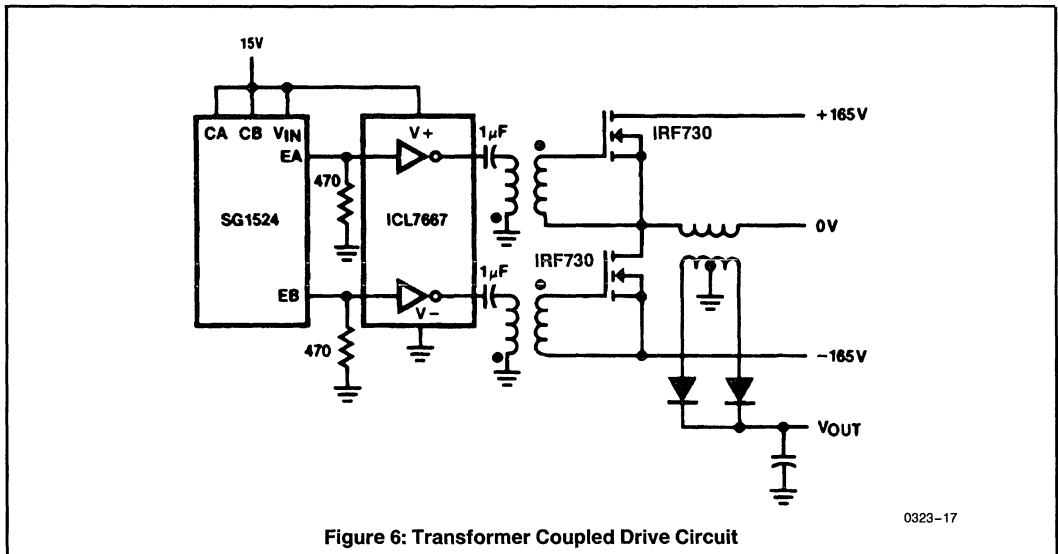
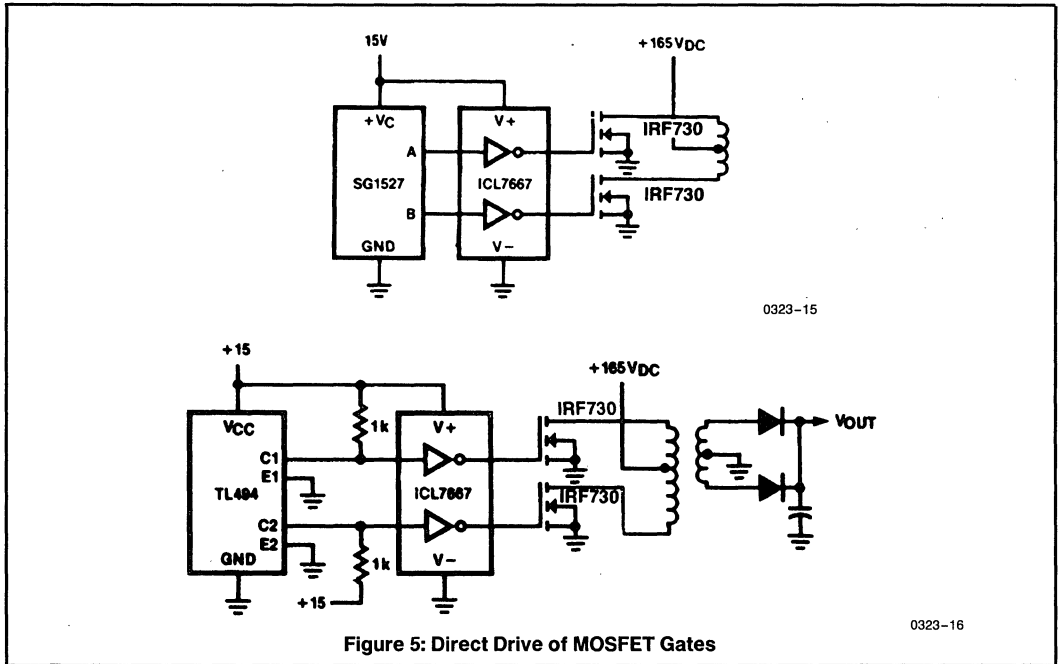
Figure 6 shows interfaces between the ICL7667 and typical switching regulator ICs. Note that unlike the DS0026, the ICL7667 does not need a dropping resistor and speed-up capacitor between it and the regulator IC. The ICL7667, with its high slew rate and high voltage drive can directly drive the gate of the MOSFET. The 1527 IC is the same as the 1525 IC, except that the outputs are inverted. This inversion is needed since ICL7667 is an inverting buffer.

## TRANSFORMER COUPLED DRIVE OF MOSFETS

Transformers are often used for isolation between the logic and control section and the power section of a switching regulator. The high output drive capability of the ICL7667 enables it to directly drive such transformers. Figure 6 shows a typical transformer coupled drive circuit. PWM ICs with either active high or active low outputs can be used in this circuit, since any inversion required can be obtained by reversing the windings on the secondaries.

## BUFFERED DRIVERS FOR MULTIPLE MOSFETS

In very high power applications which use a group of MOSFETs in parallel, the input capacitance may be very large and it can be difficult to charge and discharge quickly. Figure 8 shows a circuit which works very well with very large capacitance loads. When the input of the driver is zero, Q1 is held in conduction by the lower half of the ICL7667 and Q2 is clamped off by Q1. When the input goes positive, Q1 is turned off and a current pulse is applied to the gate of Q2 by the upper half of the ICL7667 through the transformer, T1. After about 20ns, T1 saturates and Q2 is held on by its own  $C_{GS}$  and the bootstrap circuit of C1, D1 and R1. This bootstrap circuit may not be needed at frequencies greater than 10kHz since the input capacitance of Q2 discharges slowly.



NOTE: All typical values have been characterized but are not tested.

# ICL7667

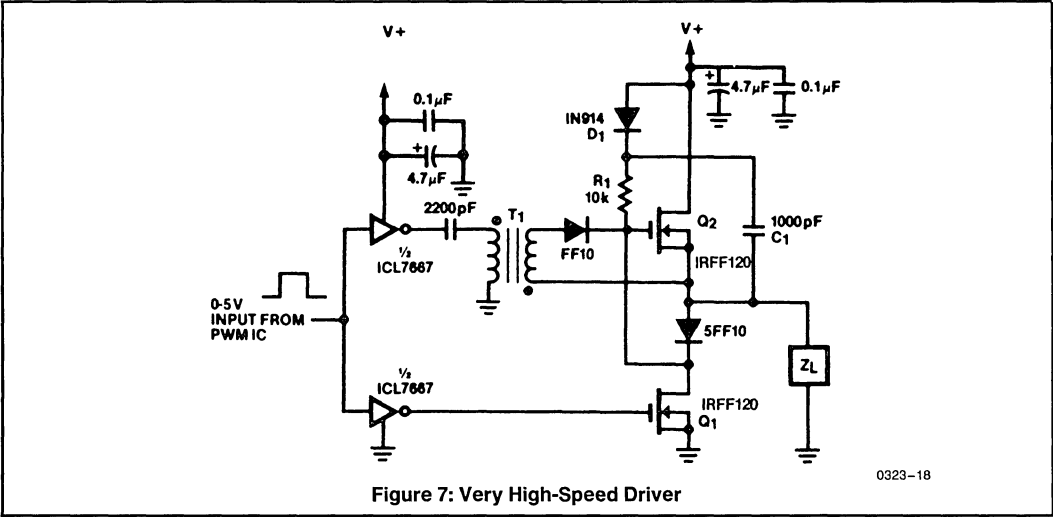


Figure 7: Very High-Speed Driver

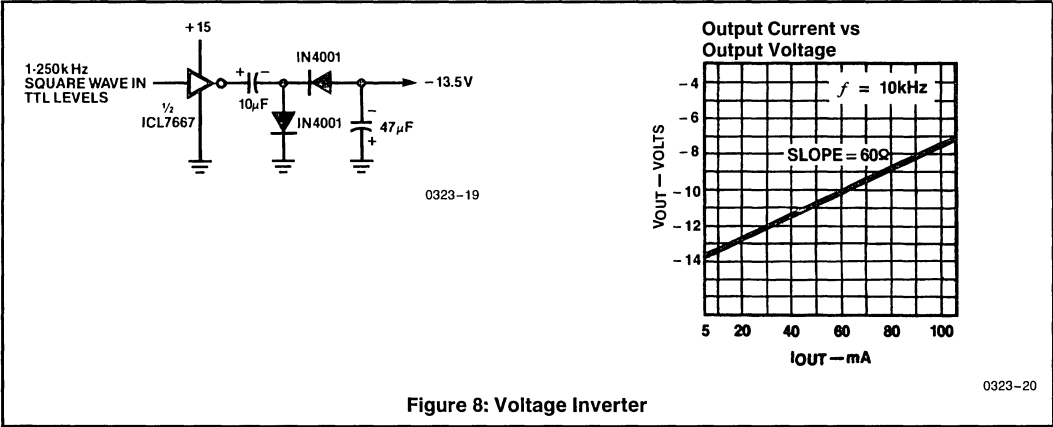
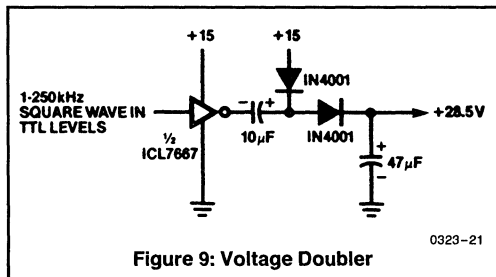


Figure 8: Voltage Inverter

NOTE: All typical values have been characterized but are not tested.



## OTHER APPLICATIONS

### RELAY AND LAMP DRIVERS

The ICL7667 is suitable for converting low power TTL or CMOS signals into high current, high voltage outputs for relays, lamps and other loads. Unlike many other level translator/driver ICs, the ICL7667 will both source and sink current. The continuous output current is limited to 200mA by the  $I^2R$  power dissipation in the output FETs.

### CHARGE PUMP OR VOLTAGE INVERTERS AND DOUBLERS

The low output impedance and wide  $V_{CC}$  range of the ICL7667 make it well suited for charge pump circuits. Figure

8 shows a typical charge pump voltage inverter circuit and a typical performance curve. A common use of this circuit is to provide a low current negative supply for analog circuitry or RS232 drivers. With an input voltage of +15V, this circuit will deliver 20mA at -12.6V. By increasing the size of the capacitors, the current capability can be increased and the voltage loss decreased. The practical range of the input frequency is 500Hz to 250kHz. As the frequency goes up, the charge pump capacitors can be made smaller, but the internal losses in the ICL7667 will rise, reducing the circuit efficiency.

Figure 9, a voltage doubler, is very similar in both circuitry and performance. A potential use of Figure 8 would be to supply the higher voltage needed for EEPROM or EPROM programming.

### CLOCK DRIVER

Some microprocessors (such as the 68XX and 65XX families) use a clock signal to control the various LSI peripherals of the family. The ICL7667's combination of low propagation delay, high current drive capability and wide voltage swing make it attractive for this application. Although the ICL7667 is primarily intended for driving power MOSFET gates at 15V, the ICL7667 also works well as a 5V high-speed buffer. Unlike standard 4000 series CMOS, the ICL7667 uses short channel length FETs and the ICL7667 is only slightly slower at 5V than at 15V.

# ICL7673

## Automatic Battery Back-up Switch

### GENERAL DESCRIPTION

The Harris ICL7673 is a monolithic CMOS battery backup circuit that offers unique performance advantages over conventional means of switching to a backup supply. The ICL7673 is intended as a low-cost solution for the switching of systems between two power supplies; main and battery backup. The main application is keep-alive-battery power switching for use in volatile CMOS RAM memory systems and real time clocks. In many applications this circuit will represent a low insertion voltage loss between the supplies and load. This circuit features low current consumption, wide operating voltage range, and exceptionally low leakage between inputs. Logic outputs are provided that can be used to indicate which supply is connected and can also be used to increase the power switching capability of the circuit by driving external PNP transistors.

### ORDERING INFORMATION

| Part Number | Temperature Range | Package        |
|-------------|-------------------|----------------|
| ICL7673CPA  | 0°C to +70°C      | 8 Pin Mini DIP |
| ICL7673CBA  | 0°C to +70°C      | 8 Pin SOIC     |
| ICL7673ITV  | -25°C to +85°C    | 8 Pin TO-99    |

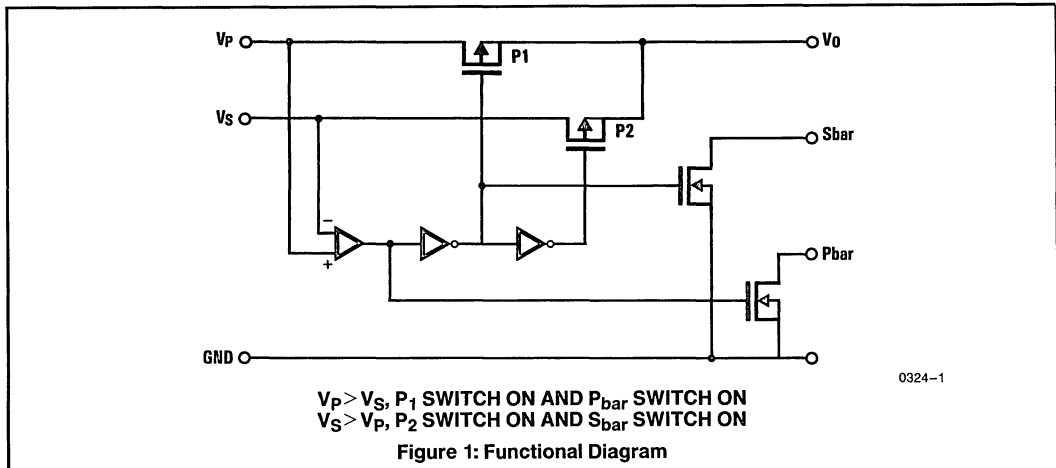
### FEATURES

- Automatically Connects Output to The Greater Of Either Input Supply Voltage
- If Main Power to External Equipment Is Lost, Circuit Will Automatically Connect Battery Backup
- Reconnects Main Power When Restored
- Logic Indicator Signaling Status Of Main Power
- Low Impedance Connection Switches
- Low Internal Power Consumption
- Wide Supply Range: 2.5 to 15 Volts
- Low Leakage Between Inputs
- External Transistors May Be Added If Very Large Currents Need to Be Switched

### APPLICATIONS

- On Board Battery Backup for Real-Time Clocks, Timers, or Volatile RAMs
- Over/Under Voltage Detector
- Peak Voltage Detector
- Other Uses:
  - Portable Instruments, Portable Telephones, Line Operated Equipment

2  
POWER PROCESSING  
CIRCUITS





# ICL7673

## ABSOLUTE MAXIMUM RATINGS

|   |                           |
|---|---------------------------|
| Input Supply ( $V_P$ or $V_S$ ) Voltage | ..... (GND - 0.3) to +18V |
| Output Voltages $P_{bar}$ and $S_{bar}$ | ..... (GND - 0.3) to +18V |
| Peak Current                            |                           |
| Input $V_P$ (@ $V_P=5V$ ) (note 1)      | ..... 38mA                |
| Input $V_S$ (@ $V_S=3V$ )               | ..... 30mA                |
| $P_{bar}$ or $S_{bar}$                  | ..... 150mA               |
| Continuous Current                      |                           |
| Input $V_P$ (@ $V_P=5V$ ) (note 1)      | ..... 38mA                |
| Input $V_S$ (@ $V_S=3V$ )               | ..... 30mA                |
| $P_{bar}$ or $S_{bar}$                  | ..... 50mA                |

|                                   |                       |
|-----------------------------------|-----------------------|
| Package Dissipation               | ..... 300mW           |
| Derate                            | ..... 6.1mW/°C        |
| Operating Temperature Range:      |                       |
| ICL7673C                          | ..... 0°C to +70°C    |
| ICL7673I                          | ..... -25°C to +85°C  |
| Storage Temperature               | ..... -65°C to +150°C |
| Lead Temperature (soldering, 10s) | ..... 300°C           |

Note 1. Derate above 25°C by 0.38mA/°C.

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

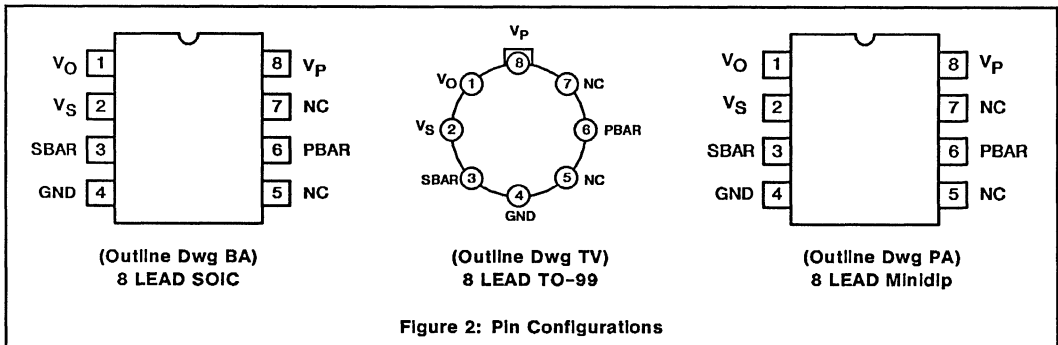


Figure 2: Pin Configurations

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

| Symbol         | Parameter                     | Test Conditions   | Min | Typ | Max | Units         |
|----------------|-------------------------------|---|-----|-----|-----|---------------|
| $V_P$          | INPUT VOLTAGE                 | $V_S = 0$ volts<br>$I_{load} = 0$ mA                      | 2.5 | -   | 15  | V             |
| $V_S$          |                               | $V_P = 0$ volts<br>$I_{load} = 0$ mA                      | 2.5 | -   | 15  |               |
| $I^+$          | QUIESCENT SUPPLY CURRENT      | $V_P = 0$ volts<br>$V_S = 3$ volts<br>$I_{load} = 0$ mA   | -   | 1.5 | 5   | $\mu\text{A}$ |
| $R_{ds(on)P1}$ | SWITCH RESISTANCE P1 (NOTE 2) | $V_P = 5$ volts<br>$V_S = 3$ volts<br>$I_{load} = 15$ mA  | -   | 8   | 15  | $\Omega$      |
|                |                               | @ $T_A = 85^\circ\text{C}$                                | -   | 16  | -   |               |
|                |                               | $V_P = 9$ volts<br>$V_S = 3$ volts<br>$I_{load} = 15$ mA  | -   | 6   | -   | $\Omega$      |
|                |                               | $V_P = 12$ volts<br>$V_S = 3$ volts<br>$I_{load} = 15$ mA | -   | 5   | -   | $\Omega$      |

NOTE: All typical values have been characterized but are not tested.

# ICL7673

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise specified) (Continued)

| Symbol                | Parameter   | Test Conditions   | Min | Typ  | Max | Units |
|-----------------------|---|---|-----|------|-----|-------|
| T <sub>C(P1)</sub>    | TEMPERATURE COEFFICIENT OF SWITCH RESISTANCE P1     | V <sub>P</sub> = 5 volts<br>V <sub>S</sub> = 3 volts<br>I load = 15mA                   | –   | 0.5  | –   | %/°C  |
| R <sub>ds(on)P2</sub> | SWITCH RESISTANCE P2 (NOTE 2)                       | V <sub>P</sub> = 0 volts<br>V <sub>S</sub> = 3 volts<br>I load = 1mA                    | –   | 40   | 100 | Ω     |
|                       |   | @ T <sub>A</sub> = 85°C   | –   | 60   | –   |       |
|                       |   | V <sub>P</sub> = 0 volts<br>V <sub>S</sub> = 5 volts<br>I load = 1mA                    | –   | 26   | –   | Ω     |
|                       |   | V <sub>P</sub> = 0 volts<br>V <sub>S</sub> = 9 volts<br>I load = 1mA                    | –   | 16   | –   | Ω     |
| T <sub>C(P2)</sub>    | TEMPERATURE COEFFICIENT OF SWITCH RESISTANCE P2     | V <sub>P</sub> = 0 volts<br>V <sub>S</sub> = 3 volts<br>I load = 1mA                    | –   | 0.7  | –   | %/°C  |
| I <sub>L(PS)</sub>    | LEAKAGE CURRENT (V <sub>P</sub> to V <sub>S</sub> ) | V <sub>P</sub> = 5 volts<br>V <sub>S</sub> = 3 volts<br>I load = 10mA                   | –   | 0.01 | 20  | nA    |
|                       |   | @ T <sub>A</sub> = 85°C   | –   | 35   | –   |       |
| I <sub>L(SP)</sub>    | LEAKAGE CURRENT (V <sub>S</sub> to V <sub>P</sub> ) | V <sub>P</sub> = 0 volts<br>V <sub>S</sub> = 3 volts<br>I load = 1mA                    | –   | 0.01 | 50  | nA    |
|                       |   | @ T <sub>A</sub> = 85°C   | –   | 120  | –   |       |
| V <sub>O Pbar</sub>   | OPEN DRAIN OUTPUT SATURATION VOLTAGES               | V <sub>P</sub> = 5 volts<br>V <sub>S</sub> = 3 volts<br>I sink = 3.2mA<br>I load = 0mA  | –   | 85   | 400 | mV    |
|                       |   | @ T <sub>A</sub> = 85°C   | –   | 120  | –   |       |
|                       |   | V <sub>P</sub> = 9 volts<br>V <sub>S</sub> = 3 volts<br>I sink = 3.2mA<br>I load = 0mA  | –   | 50   | –   | mV    |
|                       |   | V <sub>P</sub> = 12 volts<br>V <sub>S</sub> = 3 volts<br>I sink = 3.2mA<br>I load = 0mA | –   | 40   | –   | mV    |
| V <sub>O Sbar</sub>   | OPEN DRAIN OUTPUT SATURATION VOLTAGES               | V <sub>P</sub> = 0 volts<br>V <sub>S</sub> = 3 volts<br>I sink = 3.2mA<br>I load = 0mA  | –   | 150  | 400 | mV    |
|                       |   | @ T <sub>A</sub> = 85°C   | –   | 210  | –   |       |
|                       |   | V <sub>P</sub> = 0 volts<br>V <sub>S</sub> = 5 volts<br>I sink = 3.2mA<br>I load = 0mA  | –   | 85   | –   | mV    |
|                       |   | V <sub>P</sub> = 0 volts<br>V <sub>S</sub> = 9 volts<br>I sink = 3.2mA<br>I load = 0mA  | –   | 50   | –   | mV    |

NOTE: All typical values have been characterized but are not tested.

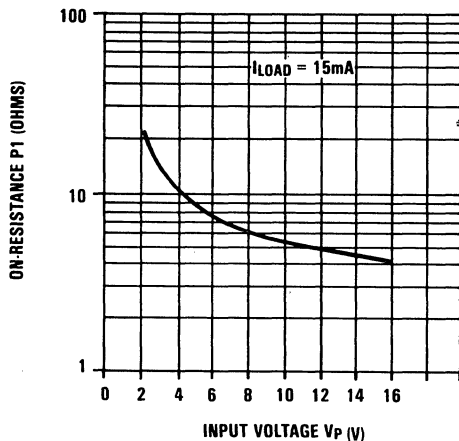
## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise specified) (Continued)

| Symbol                          | Parameter   | Test Conditions  | Min | Typ  | Max  | Units |
|---------------------------------|---|--|-----|------|------|-------|
| $I_{L Pbar}$                    | OUTPUT LEAKAGE CURRENTS OF Pbar AND Sbar  | V <sub>P</sub> = 0 volts<br>V <sub>S</sub> = 15 volts<br>I <sub>load</sub> = 0mA | -   | 50   | 500  | nA    |
|                                 |   | @ T <sub>A</sub> = 85°C  | -   | 900  | -    |       |
| $I_{L Sbar}$                    |   | V <sub>P</sub> = 15 volts<br>V <sub>S</sub> = 0 volts<br>I <sub>load</sub> = 0mA | -   | 50   | 500  | nA    |
|                                 |   | @ T <sub>A</sub> = 85°C  | -   | 900  | -    |       |
| V <sub>P</sub> - V <sub>S</sub> | SWITCHOVER UNCERTAINTY FOR COMPLETE SWITCHING OF INPUTS AND OPEN DRAIN OUTPUTS. | V <sub>S</sub> = 3 volts<br>I <sub>sink</sub> = 3.2mA<br>I <sub>load</sub> = 0mA | -   | ± 10 | ± 50 | mV    |

NOTE 2. The minimum input to output voltage can be determined by multiplying the load current by the switch resistance.

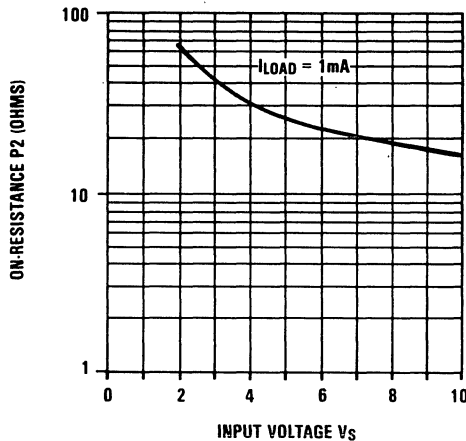
## TYPICAL PERFORMANCE CHARACTERISTICS

ON-RESISTANCE SWITCH P1 AS A FUNCTION OF INPUT VOLTAGE V<sub>P</sub>



0324-5

ON-RESISTANCE SWITCH P2 AS A FUNCTION OF INPUT VOLTAGE V<sub>S</sub>

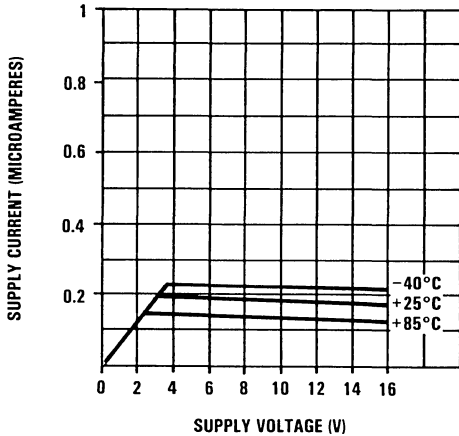


0324-6

NOTE: All typical values have been characterized but are not tested.

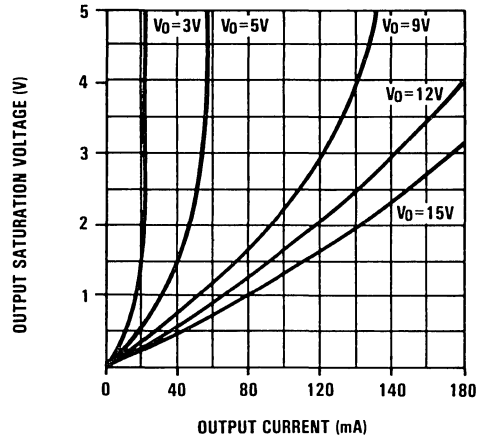
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



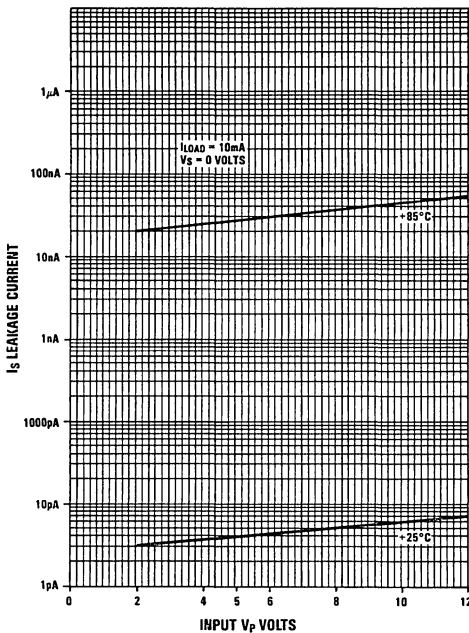
0324-7

Pbar OR Sbar SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



0324-8

I<sub>S</sub> LEAKAGE CURRENT V<sub>P</sub> to V<sub>S</sub> AS A FUNCTION OF INPUT VOLTAGE



0324-9

## DETAILED DESCRIPTION

As shown in the functional diagram (Figure 1), the ICL7673 includes a comparator which senses the input voltages V<sub>P</sub> and V<sub>S</sub>. The output of the comparator drives the first inverter and the open-drain N-channel transistor P<sub>bar</sub>. The first inverter drives a large P-channel switch, P1, a second inverter, and another open-drain N-channel transistor, S<sub>bar</sub>. The second inverter drives another large P-channel switch P2. The ICL7673, connected to a main and a backup power supply, will connect the supply of greater potential to its output. The circuit provides break-before-make switch action as it switches from main to backup power in the event of a main power supply failure. For proper operation, inputs V<sub>P</sub> and V<sub>S</sub> must not be allowed to float, and, the difference in the two supplies must be greater than 50 millivolts. The leakage current through the reverse biased parasitic diode of switch P2 is very low.

## OUTPUT VOLTAGE

The output operating voltage range is 2.5 to 15 volts. The insertion loss between either input and the output is a function of load current, input voltage, and temperature. This is due to the P-channels being operated in their triode region, and, the ON-resistance of the switches is a function of output voltage V<sub>O</sub>. The ON-resistance of the P-channels have positive temperature coefficients, and therefore as temperature increases the insertion loss also increases. At low load currents the output voltage is nearly equal to the greater of the two inputs. The maximum voltage drop across switch P1 or P2 is 0.5 volts, since above this voltage the body-drain parasitic diode will become forward biased. Complete switching of the inputs and open-drain outputs typically occurs in 50 microseconds.

# ICL7673

## INPUT VOLTAGE

The input operating voltage range for  $V_P$  or  $V_S$  is 2.5 to 15 volts. The input supply voltage ( $V_P$  or  $V_S$ ) slew rate should be limited to 2 volts per microsecond to avoid potential harm to the circuit. In line-operated systems, the rate-of-rise (or fall) of the supply is a function of power supply design. For battery applications it may be necessary to use a capacitor between the input and ground pins to limit the rate-of-rise of the supply voltage. A low-impedance capacitor such as a  $0.047\mu\text{F}$  disc ceramic can be used to reduce the rate-of-rise.

## STATUS INDICATOR OUTPUTS

The N-channel open drain output transistors can be used to indicate which supply is connected, or can be used to drive external PNP transistors to increase the power switching capability of the circuit. When using external PNP power transistors, the output current is limited by the beta and thermal characteristics of the power transistors. The application section details the use of external PNP transistors.

## APPLICATIONS

A typical discrete battery backup circuit is illustrated in Figure 3. This approach requires several components, substantial printed circuit board space, and high labor cost. It also consumes a fairly high quiescent current. The ICL7673 battery backup circuit, illustrated in Figure 4, will often replace such discrete designs and offer much better performance, higher reliability, and lower system manufacturing cost. A trickle charge system could be implemented with an additional resistor and diode as shown in Figure 5. A complete low power AC to regulated DC system can be implemented using the ICL7673 and ICL7663S micropower voltage regulator as shown in Figure 6.

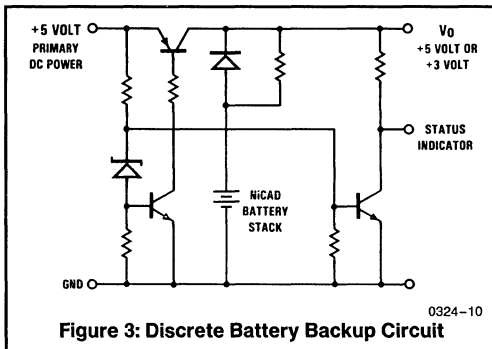


Figure 3: Discrete Battery Backup Circuit

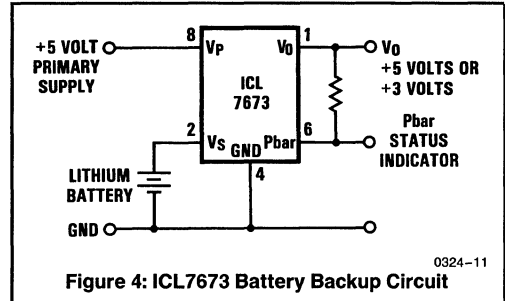


Figure 4: ICL7673 Battery Backup Circuit

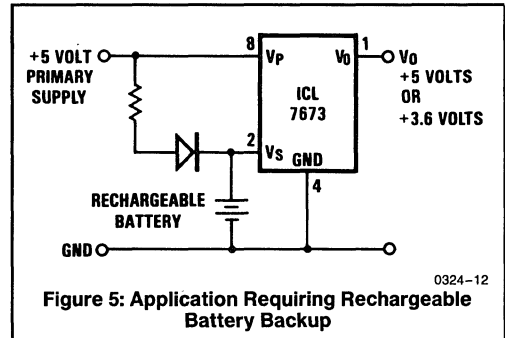


Figure 5: Application Requiring Rechargeable Battery Backup

Applications for the ICL7673 include volatile semiconductor memory storage systems, real-time clocks, timers, alarm systems, and over/under voltage detectors. Other systems requiring DC power when the master AC line supply fails can also use the ICL7673.

A typical application, as illustrated in Figure 7, would be a microprocessor system requiring a 5 volt supply. In the event of primary supply failure, the system is powered down, and a 3 volt battery is employed to maintain clock or volatile memory data. The main and backup supplies are connected to  $V_P$  and  $V_S$ , with the circuit output  $V_O$  supplying power to the clock or volatile memory. The ICL7673 will sense the main supply, when energized, to be of greater potential than  $V_S$  and connect, via its internal MOS switches,  $V_P$  to output  $V_O$ . The backup input,  $V_S$  will be disconnected internally. In the event of main supply failure, the circuit will sense that the backup supply is now the greater potential, disconnect  $V_P$  from  $V_O$ , and connect  $V_S$ .

Figure 8 illustrates the use of external PNP power transistors to increase the power switching capability of the circuit. In this application the output current is limited by the beta and thermal characteristics of the power transistors.

If hysteresis is desired for a particular low power application, positive feedback can be applied between the input  $V_P$  and open drain output  $S_{bar}$  through a resistor as illustrated in Figure 9. For high power applications hysteresis can be applied as shown in Figure 10.

The ICL7673 can also be used as a clipping circuit as illustrated in Figure 11. With high impedance loads the circuit output will be nearly equal to the greater of the two input signals.

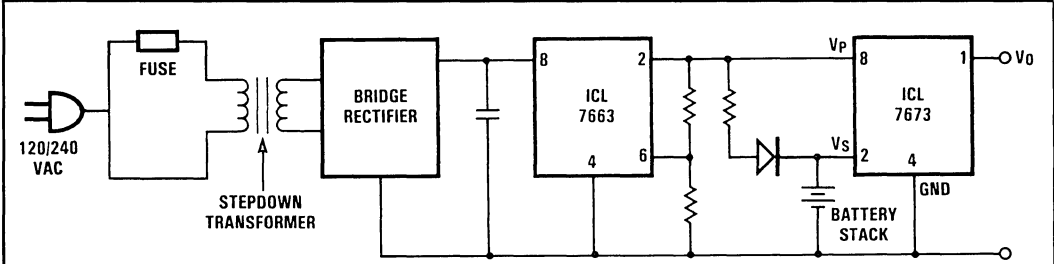


Figure 6: Power Supply for Low Power Portable AC to DC Systems

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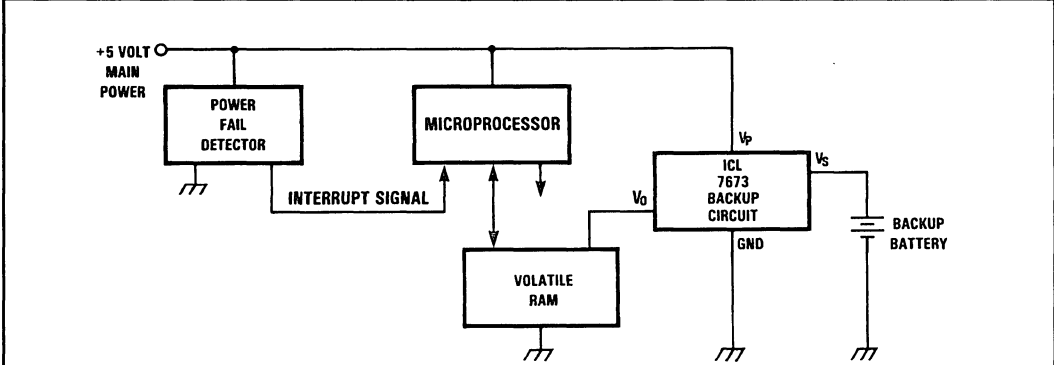


Figure 7: Typical Microprocessor Memory Application

0324-14

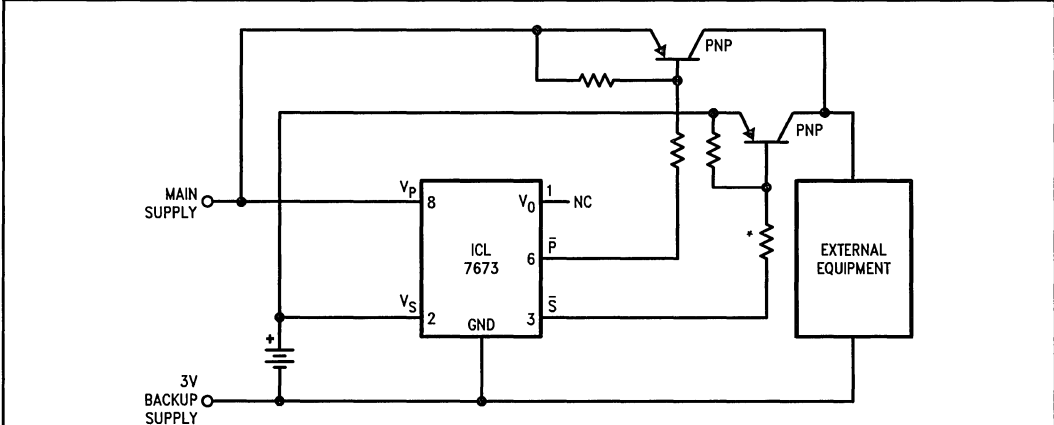


Figure 8: High Current Battery Backup System

\* > 1MΩ

0324-15

NOTE: All typical values have been characterized but are not tested.

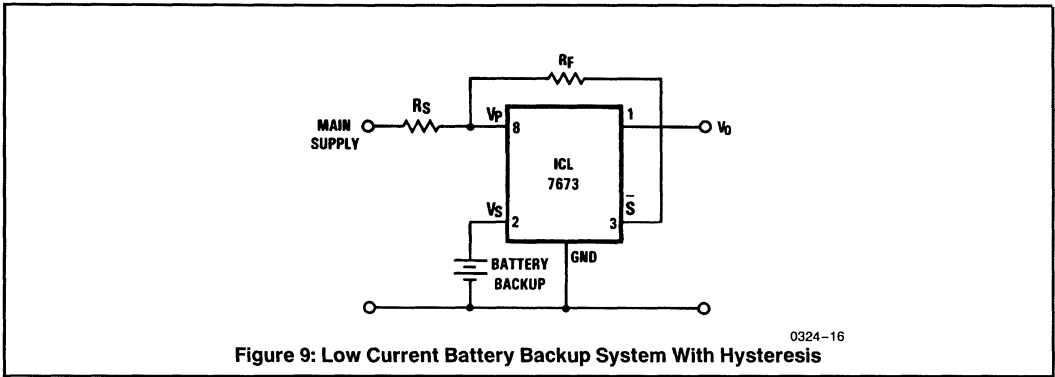


Figure 9: Low Current Battery Backup System With Hysteresis

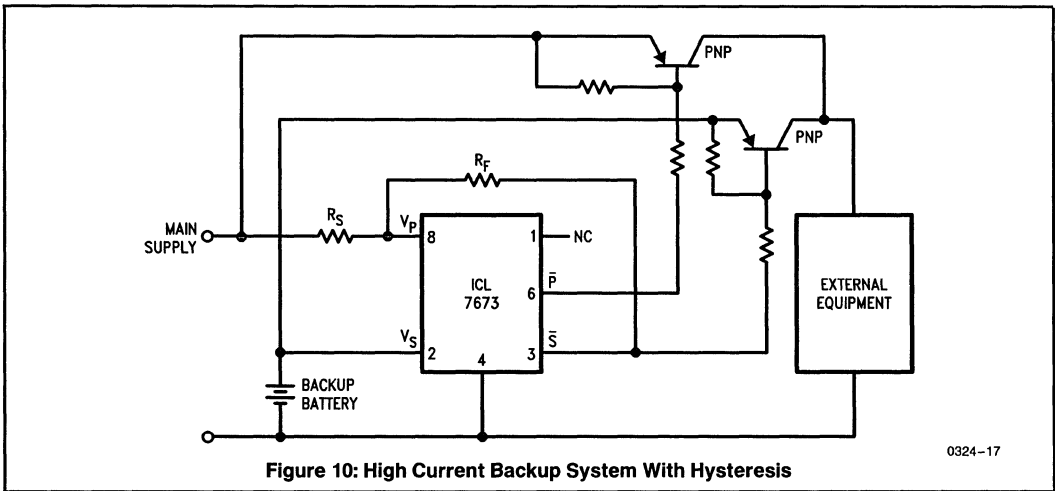


Figure 10: High Current Backup System With Hysteresis

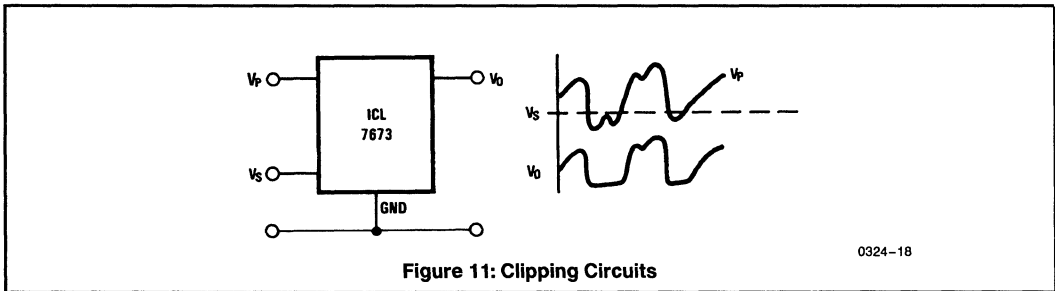


Figure 11: Clipping Circuits

# ICL8211/ICL8212 Programmable Voltage Detectors

## GENERAL DESCRIPTION

The Harris ICL8211/8212 are micropower bipolar monolithic integrated circuits intended primarily for precise voltage detection and generation. These circuits consist of an accurate voltage reference, a comparator and a pair of output buffer/drivers.

Specifically, the ICL8211 provides a 7mA current limited output sink when the voltage applied to the 'THRESHOLD' terminal is less than 1.15 volts (the internal reference). The ICL8212 requires a voltage in excess of 1.15 volts to switch its output on (no current limit). Both devices have a low current output (HYSTERESIS) which is switched on for input voltages in excess of 1.15V. The HYSTERESIS output may be used to provide positive and noise free output switching using a simple feedback network.

## ORDERING INFORMATION

| Part Number | Temperature Range | Package         |
|-------------|-------------------|-----------------|
| ICL8211CPA  | 0°C to +70°C      | 8 lead Mini DIP |
| ICL8211CBA  | 0°C to +70°C      | 8 lead SOIC     |
| ICL8211CTY  | 0°C to +70°C      | TO-99 Can       |
| ICL8211MTY* | -55°C to +125°C   | TO-99 Can       |
| ICL8212CPA  | 0°C to +70°C      | 8 lead Mini DIP |
| ICL8212CBA  | 0°C to +70°C      | 8 lead SOIC     |
| ICL8212CTY  | 0°C to +70°C      | TO-99 Can       |
| ICL8212MTY* | -55°C to +125°C   | TO-99 Can       |

\* Add /883B to part number if 883B processing is required.

## FEATURES

- High Accuracy Voltage Sensing and Generation: Internal Reference 1.15 Volts Typical
- Low Sensitivity to Supply Voltage and Temperature Variations
- Wide Supply Voltage Range: Typ. 1.8 to 30 Volts
- Essentially Constant Supply Current Over Full Supply Voltage Range
- Easy to Set Hysteresis Voltage Range
- Defined Output Current Limit — ICL8211  
High Output Current Capability — ICL8212

## APPLICATIONS

- Low Voltage Sensor/Indicator
- High Voltage Sensor/Indicator
- Non Volatile Out-of-Voltage Range Sensor/Indicator
- Programmable Voltage Reference or Zener Diode
- Series or Shunt Power Supply Regulator
- Fixed Value Constant Current Source

2  
POWER PROCESSING  
CIRCUITS

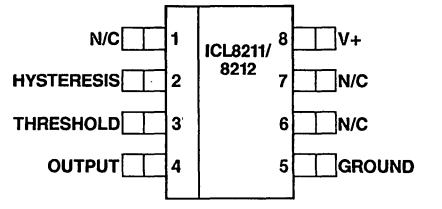
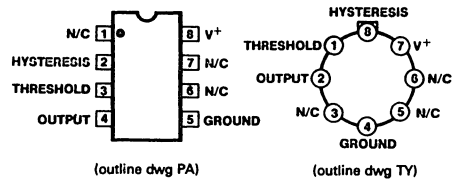
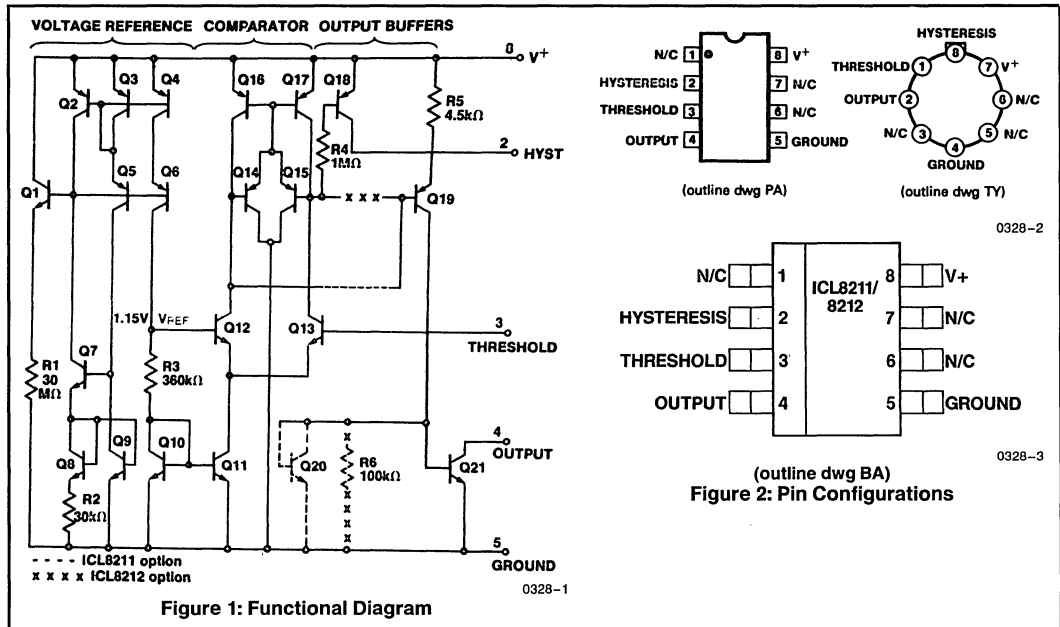


Figure 2: Pin Configurations

HARRIS SEMICONDUCTOR'S SOLE AND EXCLUSIVE WARRANTY OBLIGATION WITH RESPECT TO THIS PRODUCT SHALL BE THAT STATED IN THE WARRANTY ARTICLE OF THE CONDITION OF SALE. THE WARRANTY SHALL BE EXCLUSIVE AND SHALL BE IN LIEU OF ALL OTHER WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR USE.

NOTE: All typical values have been characterized but are not tested.



# ICL8211/ICL8212

## ABSOLUTE MAXIMUM RATINGS (Note 1)

|                           |  |
|---------------------------|--|
| Supply Voltage            | -0.5 to +30 volts  |
| Output Voltage            | -0.5 to +30 volts  |
| Hysteresis Voltage        | +0.5 to -10 volts  |
| Threshold Input Voltage   | +30 to -5 volts with respect to GROUND and<br>+0 to -30 volts with respect to V+ |
| Current into Any Terminal | ±30mA  |

|                                     |                 |
|-------------------------------------|-----------------|
| Power Dissipation (Note 1 & 2)      | 300mW           |
| Operating Temperature Range:        |                 |
| ICL8211M/8212M                      | -55°C to +125°C |
| ICL8211C/8212C                      | 0°C to +70°C    |
| Storage Temperature Range           | -65°C to +150°C |
| Lead Temperature (Soldering, 10sec) | 300°C           |

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**NOTE 1:** Rating applies for case temperatures to 125°C to ICL8211MTY/8212MTY products. Derate linearly at -10mW/°C for ambient temperatures above 100°C.

**NOTE 2:** Derate linearly above 50°C by -10mW/°C for ICL8211C/8212C products. The threshold input voltage may exceed +7 volts for short periods of time. However for continuous operation this voltage must be maintained at a value less than 7 volts.

## ELECTRICAL CHARACTERISTICS (V+ = 5V, TA = 25°C unless otherwise specified)

| Symbol                 | Parameter  | Test Conditions                                    | ICL8211              |                        |                      | ICL8212              |                        |                      | Units                |
|------------------------|--|--|----------------------|------------------------|----------------------|----------------------|------------------------|----------------------|----------------------|
|                        |  |  | Min                  | Typ                    | Max                  | Min                  | Typ                    | Max                  |                      |
| I+                     | Supply Current   | 2.0 < V+ < 30<br>VTH = 1.3V<br>VTH = 0.9V          | 10<br>50             | 22<br>140              | 40<br>250            | 50<br>10             | 110<br>20              | 250<br>40            | µA<br>µA             |
| VTH                    | Threshold Trip Voltage   | IOUT = 4mA<br>VOUT = 2V                            | 0.98<br>0.98<br>1.00 | 1.15<br>1.145<br>1.165 | 1.19<br>1.19<br>1.20 | 1.00<br>1.00<br>1.05 | 1.15<br>1.145<br>1.165 | 1.19<br>1.19<br>1.20 | V<br>V<br>V          |
| VTHP                   | Threshold Voltage Disparity Between Output & Hysteresis Output | IOUT = 4mA<br>IHYS = 7µA                           |                      | -8.0                   |                      |                      | -0.5                   |                      | mV                   |
| VSUPPLY                | Guaranteed Operating Supply Voltage Range (Note 5)             | +25°C<br>0 to +70°C                                | 2.0<br>2.2           |                        | 30<br>30             | 2.0<br>2.2           |                        | 30<br>30             | V<br>V               |
| VSUPPLY                | Minimum Operating Supply Voltage Range                         | +25°C<br>+125°C<br>-55°C                           |                      | 1.8<br>1.4<br>2.5      |                      |                      | 1.8<br>1.4<br>2.5      |                      | V<br>V<br>V          |
| ΔVTH/ΔT                | Threshold Voltage Temperature Coefficient                      | IOUT = 4mA<br>VOUT = 2V                            |                      | ±200                   |                      |                      | ±200                   |                      | ppm/°C               |
| ΔVTH/ΔV+               | Variation of Threshold Voltage with Supply Voltage             | ΔV+ = 10% at V+ = 5V                               |                      | 1.0                    |                      |                      | 1.0                    |                      | mV                   |
| I <sub>TH</sub>        | Threshold Input Current  | VTH = 1.15V<br>VTH = 1.00V                         |                      | 100<br>5               | 250                  |                      | 100<br>5               | 250                  | nA<br>nA             |
| I <sub>OLK</sub>       | Output Leakage Current   | VOUT = 30V<br>VOUT = 30V<br>VOUT = 5V<br>VOUT = 5V |                      |                        | 10<br>1              |                      |                        | 10<br>1              | µA<br>µA<br>µA<br>µA |
| VSAT                   | Output Saturation Voltage                                      | IOUT = 4mA   |                      | 0.17                   | 0.4                  |                      | 0.17                   | 0.4                  | V<br>V               |
| I <sub>OH</sub>        | Max Available Output Current                                   | (Note 3 & 4)<br>VOUT = 5V                          | 4                    | 7.0                    | 12                   | 15                   | 35                     |                      | mA<br>mA             |
| I <sub>LHYS</sub>      | Hysteresis Leakage Current                                     | V+ = 10V<br>VHYS = GROUND                          |                      |                        | 0.1                  |                      |                        | 0.1                  | µA                   |
| V <sub>HYS (max)</sub> | Hysteresis Sat Voltage   | IHYS = -7µA<br>measured with respect to V+         |                      | -0.1                   | -0.2                 |                      | -0.1                   | -0.2                 | V                    |
| I <sub>HYS (max)</sub> | Max Available Hysteresis Current                               |  |                      | -15                    | -21                  |                      | -15                    | -21                  | µA                   |

**NOTES:** 3. The maximum output current of the ICL8211 is limited by design to 15mA under any operating conditions. The output voltage may be sustained at any voltage up to +30V as long as the maximum power dissipation of the device is not exceeded.

4. The maximum output current of the ICL8212 is not defined, and systems using the ICL8212 must therefore ensure that the output current does not exceed 30mA and that the maximum power dissipation of the device is not exceeded.

5. Threshold Trip Voltage is 0.80V(min) to 1.30V(max). At I<sub>OUT</sub> = 3 mA.

NOTE: All typical values have been characterized but are not tested.

# ICL8211/ICL8212

## ELECTRICAL CHARACTERISTICS ICL8211MTY/8212MTY ( $V^+ = 5V$ , $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ )

| Symbol         | Parameter                                 | Test Conditions   | ICL8211      |     |              | ICL8212      |     |              | Units              |
|----------------|---|---|--------------|-----|--------------|--------------|-----|--------------|--------------------|
|                |   |   | Min          | Typ | Max          | Min          | Typ | Max          |                    |
| $I^+$          | Supply Current                            | $2.8 < V^+ < 30$<br>$V_T = 1.3V$<br>$V_T = 0.8V$                          |              |     | 100<br>350   |              |     | 350<br>100   | $\mu A$<br>$\mu A$ |
| $V_{TH}$       | Threshold Trip Voltage                    | $I_{OUT} = 2mA$<br>$V_{OUT} = 2V$<br>$V^+ = 2.8V$<br>$V^+ = 30V$          | 0.80<br>0.80 |     | 1.30<br>1.30 | 0.80<br>0.80 |     | 1.30<br>1.30 | V<br>V             |
| $V_{SUPPLY}$   | Guaranteed Operating Supply Voltage Range | (Note 5)  | 2.8          |     | 30           | 2.8          |     | 30           | V                  |
| $I_{TH}$       | Threshold Input Current                   | $V_{TH} = 1.15V$  |              |     | 400          |              |     | 400          | nA                 |
| $I_{OLK}$      | Output Leakage Current                    | $V_{OUT} = 30V$<br>$V_{TH} = 0.8V$<br>$V_{TH} = 1.3V$                     |              |     | 20           |              |     | 20           | $\mu A$<br>$\mu A$ |
| $V_{SAT}$      | Output Saturation Voltage                 | $I_{OUT} = 3mA$<br>$V_{TH} = 0.8V$<br>$V_{TH} = 1.3V$                     |              |     | 0.5          |              |     | 0.5          | V<br>V             |
| $I_{OH}$       | Max Available Output Current              | (Note 3 & 4)<br>$V_{OUT} = 5V$<br>$V_{TH} = 0.8V$<br>$V_{TH} = 1.3V$      | 3            |     | 15           | 9            |     |              | mA<br>mA           |
| $I_{LHYS}$     | Hysteresis Leakage Current                | $V^+ = 10V$<br>$V_{TH} = 0.8V$<br>$V_{HYST} = GROUND$                     |              |     | 0.2          |              |     | 0.2          | $\mu A$            |
| $V_{HYS(max)}$ | Hysteresis Saturation Voltage             | $I_{HYST} = -7\mu A$<br>$V_{TH} = 1.3V$<br>measured with respect to $V^+$ |              |     | 0.3          |              |     | 0.3          | V                  |
| $I_{HYS(max)}$ | Max Available Hysteresis Current          | $V_{TH} = 1.3V$   | 10           |     |              | 10           |     |              | $\mu A$            |

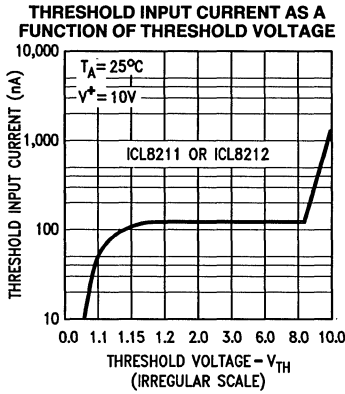
2

POWER PROCESSING  
CIRCUITS

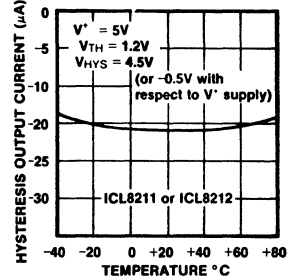
NOTE: All typical values have been characterized but are not tested.

# ICL8211/ICL8212

## TYPICAL PERFORMANCE CHARACTERISTICS COMMON TO ICL8211 AND ICL8212



HYSTERESIS OUTPUT SATURATION CURRENT AS A FUNCTION OF TEMPERATURE

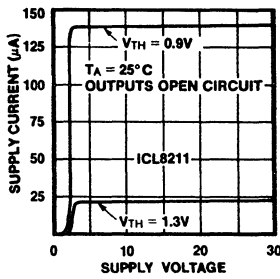


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0328-4

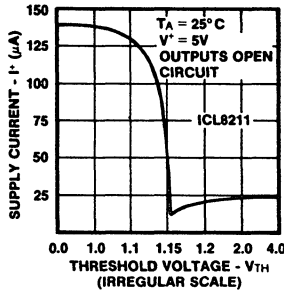
## TYPICAL PERFORMANCE CHARACTERISTICS ICL8211 ONLY

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



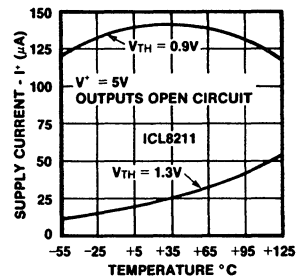
0328-6

SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



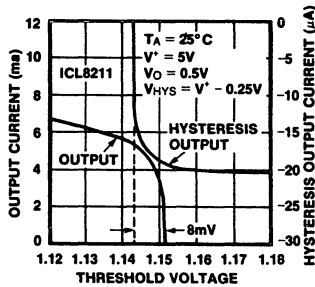
0328-7

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



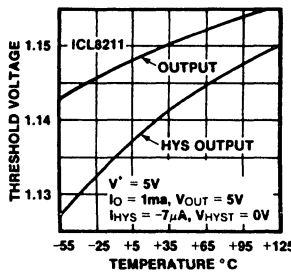
0328-8

OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE



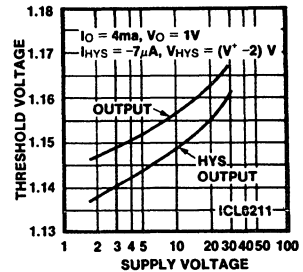
0328-9

THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE



0328-10

THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE



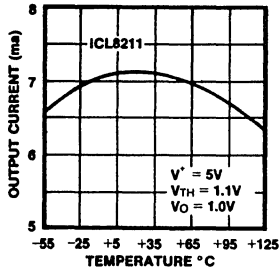
0328-11

NOTE: All typical values have been characterized but are not tested.

# ICL8211/ICL8212

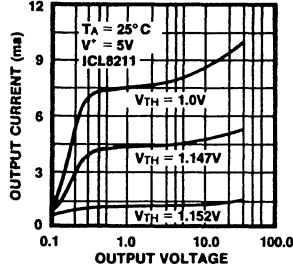
## TYPICAL PERFORMANCE CHARACTERISTICS ICL8211 ONLY (Continued)

OUTPUT SATURATION CURRENT AS A FUNCTION OF TEMPERATURE



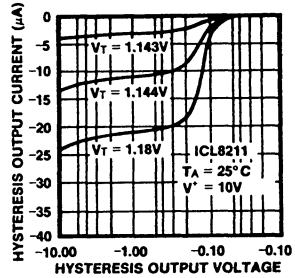
0328-12

OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



0328-13

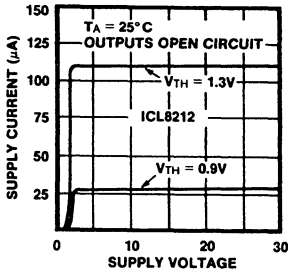
HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE



0328-23

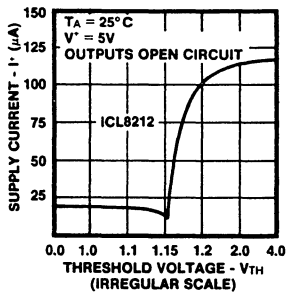
## TYPICAL PERFORMANCE CHARACTERISTICS ICL8212 ONLY

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



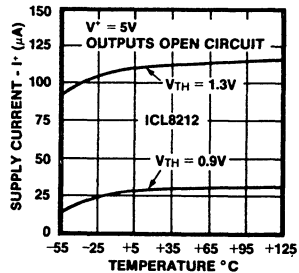
0328-15

SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



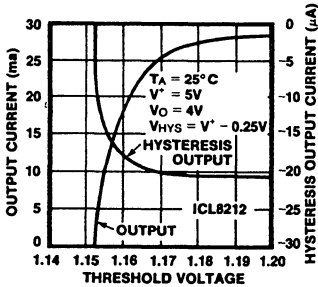
0328-16

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



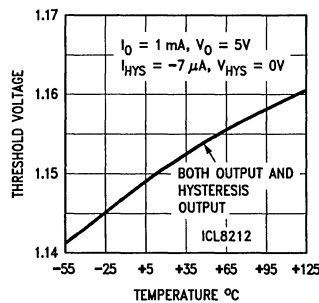
0328-17

OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE



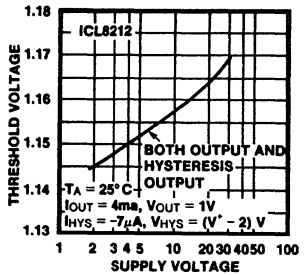
0328-18

THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE



0328-19

THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE



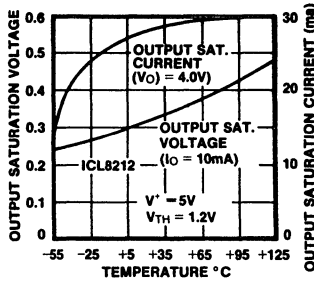
0328-20

NOTE: All typical values have been characterized but are not tested.

# ICL8211/ICL8212

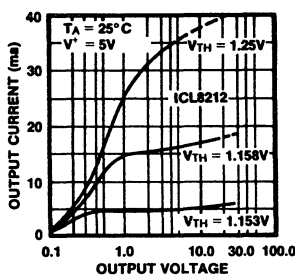
## TYPICAL PERFORMANCE CHARACTERISTICS ICL8212 ONLY (Continued)

OUTPUT SATURATION VOLTAGE AND CURRENT AS A FUNCTION OF TEMPERATURE



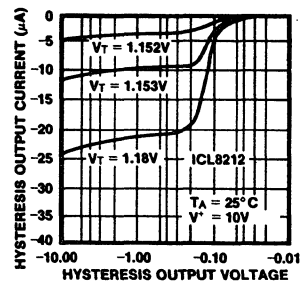
0328-21

OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



0328-22

HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE



0328-14

## DETAILED DESCRIPTION

The ICL8211 and ICL8212 use standard linear bipolar integrated circuit technology with high value thin film resistors which define extremely low value currents.

Components  $Q_1$  thru  $Q_{10}$  and  $R_1$ ,  $R_2$  and  $R_3$  set up an accurate voltage reference of 1.15 volts. This reference voltage is close to the value of the bandgap voltage for silicon and is highly stable with respect to both temperature and supply voltage. The deviation from the bandgap voltage is necessary due to the negative temperature coefficient of the thin film resistors ( $-5000$  ppm per  $^{\circ}\text{C}$ ).

Components  $Q_2$  thru  $Q_9$  and  $R_2$  make up a constant current source;  $Q_2$  and  $Q_3$  are identical and form a current mirror.  $Q_8$  has 7 times the emitter area of  $Q_9$ , and due to the current mirror, the collector currents of  $Q_8$  and  $Q_9$  are forced to be equal and it can be shown that the collector current in  $Q_8$  and  $Q_9$  is

$$I_C (Q_8 \text{ or } Q_9) = \frac{1}{R_2} \times \frac{kT}{q} \ln 7$$

or approximately  $1\mu\text{A}$  at  $25^{\circ}\text{C}$

Where  $k$  = Boltzman's constant

$q$  = charge on an electron

and  $T$  = absolute temperature in  $^{\circ}\text{K}$

Transistors  $Q_5$ ,  $Q_6$ , and  $Q_7$  assure that the  $V_{CE}$  of  $Q_3$ ,  $Q_4$ , and  $Q_9$  remain constant with supply voltage variations. This ensures a constant current supply free from variations.

The base current of  $Q_1$  provides sufficient start up current for the constant source; there being two stable states for this type of circuit — either ON as defined above, or OFF if no start up current is provided. Leakage current in the transistors is not sufficient in itself to guarantee reliable startup.

$Q_4$  is matched to  $Q_3$  and  $Q_2$ ;  $Q_{10}$  is matched to  $Q_9$ . Thus the  $I_C$  and  $V_{BE}$  of  $Q_{10}$  are identical to that of  $Q_9$  or  $Q_8$ . To generate the bandgap voltage, it is necessary to sum a voltage equal to the base emitter voltage of  $Q_9$  to a voltage proportional to the difference of the base emitter voltages of two transistors  $Q_8$  and  $Q_9$  operating at two current densities.

$$\text{Thus } 1.15 = V_{BE} (Q_9 \text{ or } Q_{10}) + \frac{R_3}{R_2} \times \frac{kT}{q} \ln 7$$

which provides  $\frac{R_3}{R_2} = 12$  (approx.)

The total supply current consumed by the voltage reference section is approximately  $6\mu\text{A}$  at room temperature. A voltage at the THRESHOLD input is compared to the reference 1.15 volts by the comparator consisting of transistors  $Q_{11}$  thru  $Q_{17}$ . The outputs from the comparator are limited to two diode drops less than  $V^+$  or approximately 1.1 volts. Thus the base current into the hysteresis output transistor is limited to about  $500\text{nA}$  and the collector current of  $Q_{19}$  to  $100\mu\text{A}$ .

In the case of the ICL8211,  $Q_{21}$  is proportioned to have 70 times the emitter area of  $Q_{20}$  thereby limiting the output current to approximately  $7\text{mA}$ , whereas for the ICL8212 almost all the collector current of  $Q_{19}$  is available for base drive to  $Q_{21}$ , resulting in a maximum available collector current of the order of  $30\text{mA}$ . It is advisable to externally limit this current to  $25\text{mA}$  or less.

## APPLICATIONS

The ICL8211 and ICL8212 are similar in many respects, especially with regard to the setup of the input trip conditions and hysteresis circuitry. The following discussion describes both devices, and where differences occur they are clearly noted.

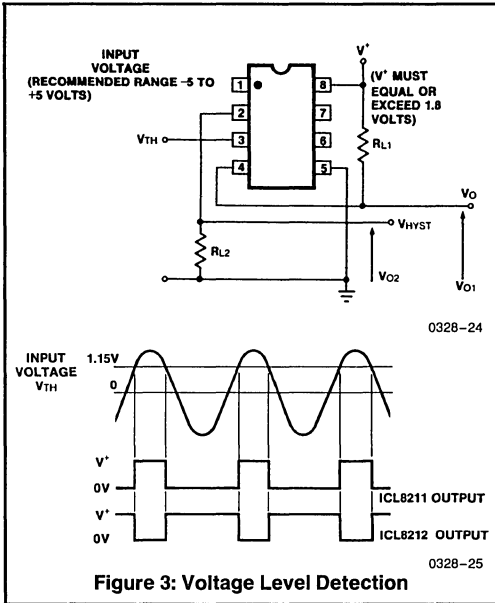
## General Information

### THRESHOLD INPUT CONSIDERATIONS

Although any voltage between  $-5\text{V}$  and  $V^+$  may be applied to the THRESHOLD terminal, it is recommended that the THRESHOLD voltage does not exceed about  $+6$  volts since above that voltage the threshold input current increases sharply. Also, prolonged operation above this voltage will lead to degradation of device characteristics.

NOTE: All typical values have been characterized but are not tested.

# ICL8211/ICL8212

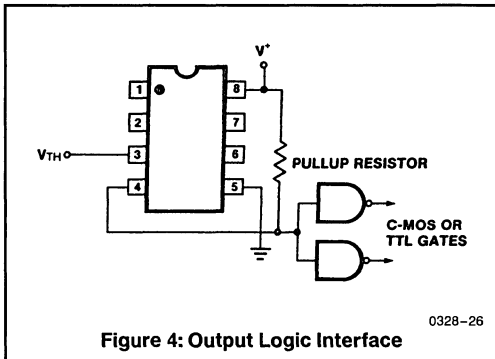


**Figure 3: Voltage Level Detection**

The outputs change states with an input THRESHOLD voltage of approximately 1.15 volts. Input and output waveforms are shown in Figure 3 for a simple 1.15 volt level detector.

The HYSTERESIS output is a low current output and is intended primarily for input threshold voltage hysteresis applications. If this output is used for other applications it is suggested that output currents be limited to  $10\mu\text{A}$  or less.

The regular OUTPUT's from either the ICL8211 or ICL8212 may be used to drive most of the common logic families such as TTL or C-MOS using a single pullup resistor. There is a guaranteed TTL fanout of 2 for the ICL8211 and 4 for the ICL8212.

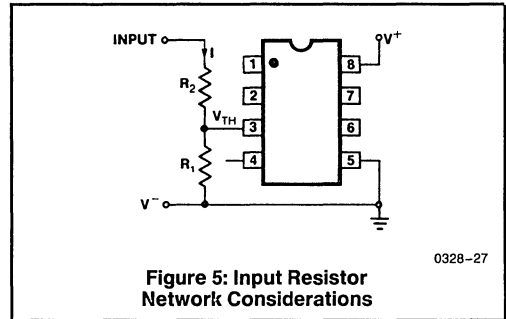


**Figure 4: Output Logic Interface**

A principal application of the ICL8211 is voltage level detection, and for that reason the OUTPUT current has been limited to typically 7mA to permit direct drive of an LED connected to the positive supply without a series current limiting resistor.

On the other hand the ICL8212 is intended for applications such as programmable zener references, and voltage regulators where output currents well in excess of 7mA are desirable. Therefore, the output of the ICL8212 is not current limited, and if the output is used to drive an LED, a series current limiting resistor must be used.

In most applications an input resistor divider network may be used to generate the 1.15V required for  $V_{TH}$ . For high accuracy, currents as large as  $50\mu\text{A}$  may be used, however for those applications where current limiting may be desirable, (such as when operating from a battery) currents as low as  $6\mu\text{A}$  may be considered without a great loss of accuracy.  $6\mu\text{A}$  represents a practical minimum, since it is about this level where the device's own input current becomes a significant percentage of that flowing in the divider network.



**Figure 5: Input Resistor Network Considerations**

Case 1. High accuracy required, current in resistor network unimportant Set  $I = 50\mu\text{A}$  for  $V_{TH} = 1.15$  volts  
 $\therefore R_1 \rightarrow 20\text{k}\Omega$ .

Case 2. Good accuracy required, current in resistor network important Set  $I = 7.5\mu\text{A}$  for  $V_{TH} = 1.15$  volts  
 $\therefore R_1 \rightarrow 150\text{k}\Omega$ .

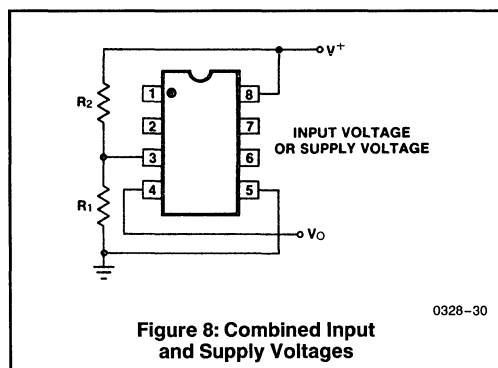
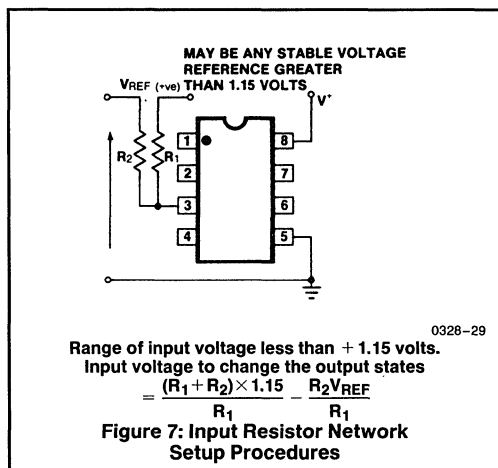
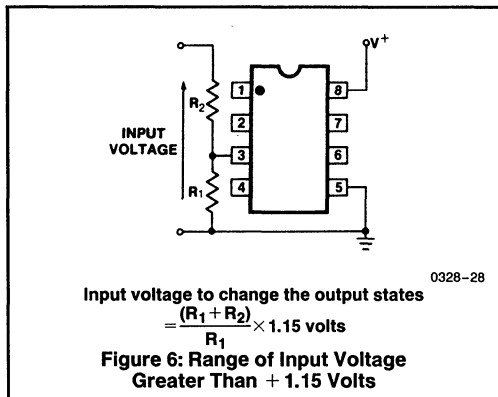
## SETUP PROCEDURES FOR VOLTAGE LEVEL DETECTION

Case 1. Simple voltage detection — no hysteresis

Unless an input voltage of approximately 1.15 volts is to be detected, resistor networks will be used to divide or multiply the unknown voltage to be sensed. Figure 7 shows procedures on how to set up resistor networks to detect INPUT VOLTAGES of any magnitude and polarity.

For supply voltage level detection applications the input resistor network is connected across the supply terminals as shown in Figure 8.

# ICL8211/ICL8212



## Case 2. Use of the HYSTERESIS function

The disadvantage of the simple detection circuits is that there is a small but finite input range where the outputs are neither totally 'ON' nor totally 'OFF'. The principle behind

hysteresis is to provide positive feedback to the input trip point such that there is a voltage difference between the input voltage necessary to turn the outputs ON and OFF.

The advantage of hysteresis is especially apparent in electrically noisy environments where simple but positive voltage detection is required. Hysteresis circuitry, however, is not limited to applications requiring better noise performance but may be expanded into highly complex systems with multiple voltage level detection and memory applications — refer to specific applications section.

There are two simple methods to apply hysteresis to a circuit for use in supply voltage level detection. These are shown in Figure 9.

The circuit (a) of Figure 9 requires that the full current flowing in the resistor network be sourced by the HYSTERESIS output, whereas for circuit (b) the current to be sourced by the HYSTERESIS output will be a function of the ratio of the two trip points and their values. For low values of hysteresis, circuit (b) is to be preferred due to the offset voltage of the hysteresis output transistor.

A third way to obtain hysteresis (ICL8211 only) is to connect a resistor between the OUTPUT and the THRESHOLD terminals thereby reducing the total external resistance between the THRESHOLD and GROUND when the OUTPUT is switched on.

## Practical Applications

### a) Low Voltage Battery Indicator (Figure 10)

This application is particularly suitable for portable or remote operated equipment which requires an indication of a depleted or discharged battery. The quiescent current taken by the system will be typically 35μA which will increase to 7mA when the lamp is turned on. R<sub>3</sub> will provide hysteresis if required.

### b) Non-Volatile Low Voltage Detector (Figure 11)

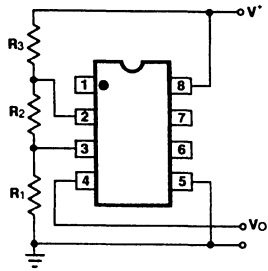
In this application the high trip voltage V<sub>TR2</sub> is set to be above the normal supply voltage range. On power up the initial condition is A. On momentarily closing switch S<sub>1</sub> the operating point changes to B and will remain at B until the supply voltage drops below V<sub>TR1</sub>, at which time the output will revert to condition A. Note that state A is always retained if the supply voltage is reduced below V<sub>TR1</sub> (even to zero volts) and then raised back to V<sub>NOM</sub>.

### c) Non-Volatile Power Supply Malfunction Recorder (Figures 12 and 13)

In many systems a transient or an extended abnormal (or absence of a) supply voltage will cause a system failure. This failure may take the form of information lost in a volatile semiconductor memory stack, a loss of time in a timer or even possible irreversible damage to components if a supply voltage exceeds a certain value.

It is, therefore, necessary to be able to detect and store the fact that an **out-of-operating range** supply voltage condition has occurred, even in the case where a supply voltage may have dropped to zero. Upon power up to the normal operating voltage this record must have been retained and easily interrogated. This could be important in the case of a transient power failure due to a faulty component or intermittent power supply, open circuit, etc., where direct observation of the failure is difficult.

# ICL8211/ICL8212



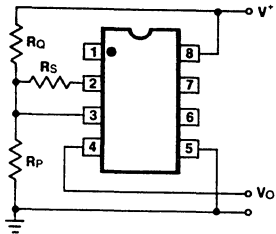
0328-31

Low trip voltage

$$V_{TR1} = \left[ \frac{(R_1 + R_2 \times 1.15)}{R_1} + 0.1 \right] \text{ volts}$$

High trip voltage

$$V_{TR2} = \frac{(R_1 + R_2 + R_3)}{R_1} \times 1.15 \text{ volts}$$



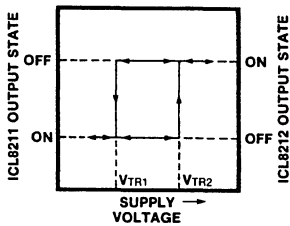
0328-32

Low trip voltage

$$V_{TR1} = \left[ \frac{R_Q R_S}{(R_Q + R_S)} + R_P \right] \times \frac{1}{R_P} \times 1.15 \text{ volts}$$

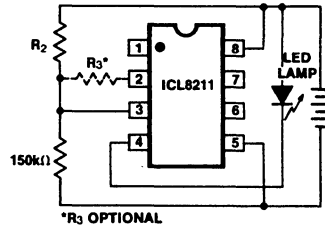
High trip voltage

$$V_{TR2} = \frac{(R_P + R_Q)}{R_P} \times 1.15 \text{ volts}$$



0328-33

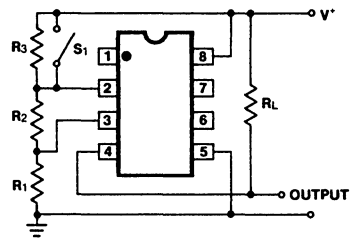
**Figure 9: Two alternative voltage detection circuits employing hysteresis to provide pairs of well defined trip voltages.**



\*R3 OPTIONAL

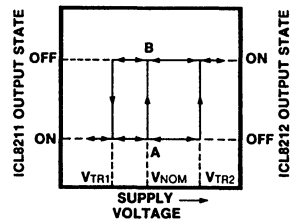
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**Figure 10: Low Voltage Battery Indicator**



0328-35

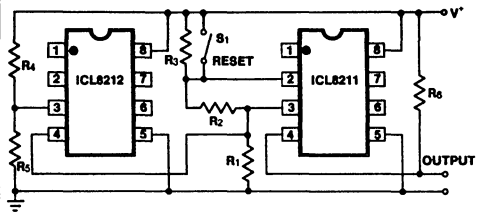
(a)



0328-36

(b)

**Figure 11: Non-Volatile Low Voltage Indicator**



0328-37

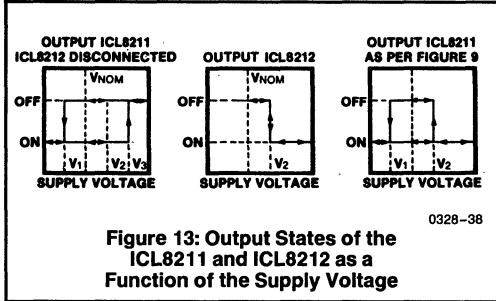
**Figure 12: Non-Volatile Power Supply Malfunction Recorder**

NOTE: All typical values have been characterized but are not tested.



# ICL8211/ICL8212

A simple circuit to record an out of range voltage excursion may be constructed using an ICL8211, an ICL8212 plus a few resistors. This circuit will operate to 30 volts without exceeding the maximum ratings of the I.C.'s. The two voltage limits defining the in range supply voltage may be set to any value between 2.0 and 30 volts.



**Figure 13: Output States of the ICL8211 and ICL8212 as a Function of the Supply Voltage**

The ICL8212 is used to detect a voltage, V<sub>2</sub>, which is the upper voltage limit to the operating voltage range. The ICL8211 detects the lower voltage limit of the operating voltage range, V<sub>1</sub>. Hysteresis is used with the ICL8211 so that the output can be stable in either state over the operating voltage range V<sub>1</sub> to V<sub>2</sub> by making V<sub>3</sub> — the upper trip point of the ICL8211 much higher in voltage than V<sub>2</sub>.

The output of the ICL8212 is used to force the output of the ICL8211 into the ON state above V<sub>2</sub>. Thus there is no value of the supply voltage that will result in the output of the ICL8211 changing from the ON state to the OFF state. This may be achieved only by shorting out R<sub>3</sub> for values of supply voltage between V<sub>1</sub> and V<sub>2</sub>.

d) Constant Current Sources (Figure 14)

The ICL8212 may be used as a constant current source of value of approximately 25μA by connecting the THRESHOLD terminal to GROUND. Similarly the ICL8211 will provide a 130μA constant current source. The equivalent parallel resistance is in the tens of megohms over the supply voltage range of 2 to 30 volts. These constant current sources may be used to provide biasing for various circuitry including differential amplifiers and comparators. See Typical Operating Characteristics for complete information.

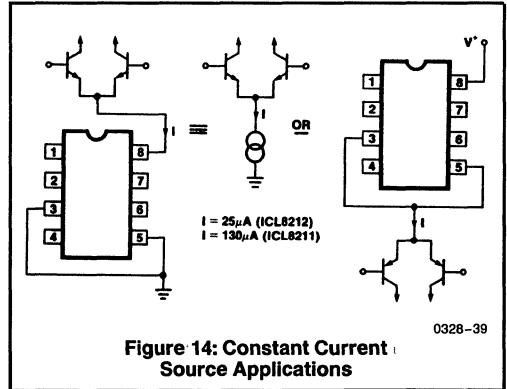
e) Programmable Zener Voltage Reference (Figure 15)

The ICL8212 may be used to simulate a zener diode by connecting the OUTPUT terminal to the V<sub>2</sub> output and using a resistor network connected to the THRESHOLD terminal to program the zener voltage

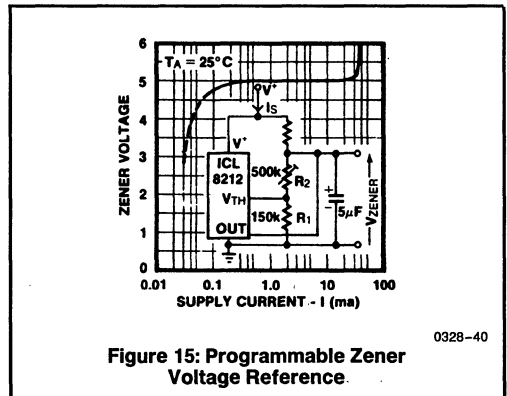
$$V_{\text{zener}} = \frac{(R_1 + R_2)}{R_1} \times 1.15 \text{ volts.}$$

Since there is no internal compensation in the ICL8212 it is necessary to use a large capacitor across the output to prevent oscillation.

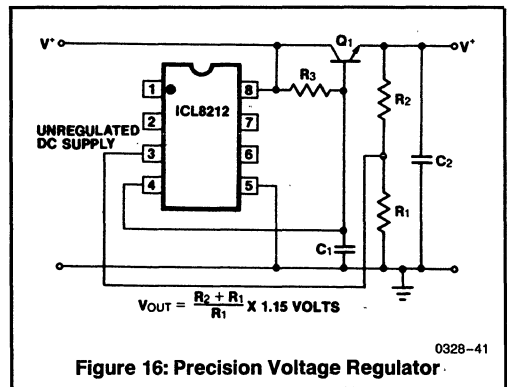
Zener voltages from 2 to 30 volts may be programmed and typical impedance values between 300μA and 25mA will range from 4 to 7Ω. The knee is sharper and occurs at a significantly lower current than other similar devices available.



**Figure 14: Constant Current Source Applications**



**Figure 15: Programmable Zener Voltage Reference**

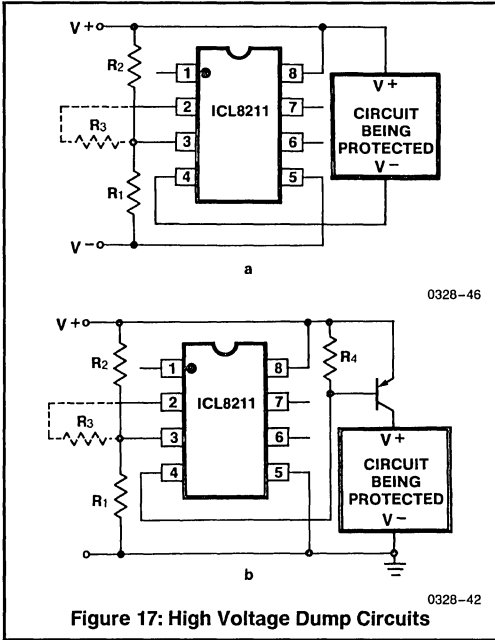


f) Precision Voltage Regulator (Figure 16)

The ICL8212 may be used as the controller for a highly stable series voltage regulator. The output voltage is simply programmed, using a resistor divider network R<sub>1</sub> and R<sub>2</sub>. Two capacitors C<sub>1</sub> and C<sub>2</sub> are required to ensure stability since the ICL8212 is uncompensated internally.

NOTE: All typical values have been characterized but are not tested.

# ICL8211/ICL8212



**Figure 17: High Voltage Dump Circuits**

This regulator may be used with lower input voltages than most other commercially available regulators and also consumes less power for a given output control current than

any commercial regulator. Applications would therefore include battery operated equipment especially those operating at low voltages.

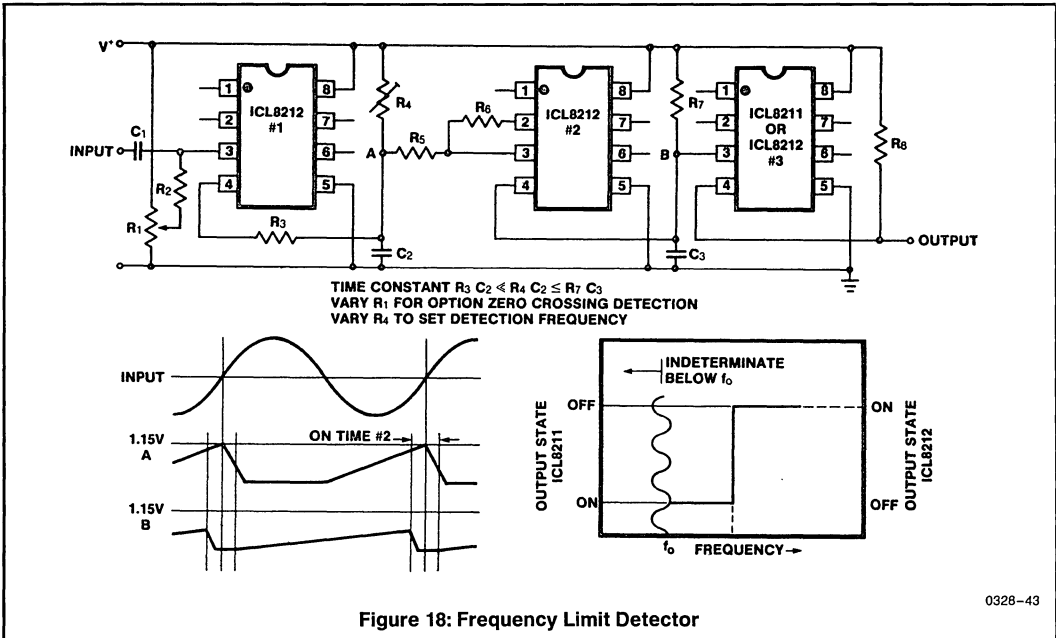
g) High Supply Voltage Dump Circuit (Figure 17)

In many circuit applications it is desirable to remove the power supply in the case of high voltage overload. For circuits consuming less than 5mA this may be achieved using an ICL8211 driving the load directly. For higher load currents it is necessary to use an external pnp transistor or darlington pair driven by the output of the ICL8211. Resistors  $R_1$  and  $R_2$  set up the disconnect voltage and  $R_3$  provides optional voltage hysteresis if so desired.

h) Frequency Limit Detector (Figure 18)

Simple frequency limit detectors providing a GO/NO-GO output for use with varying amplitude input signals may be conveniently implemented with the ICL8211/8212. In the application shown, the first ICL8212 is used as a zero crossing detector. The output circuit consisting of  $R_3$ ,  $R_4$  and  $C_2$  results in a slow output positive ramp. The negative range is much faster than the positive range.  $R_5$  and  $R_6$  provide hysteresis so that under all circumstances the second ICL8212 is turned on for sufficient time to discharge  $C_3$ . The time constant of  $R_7 C_3$  is much greater than  $R_4 C_2$ . Depending upon the desired output polarities for low and high input frequencies, either an ICL8211 or an ICL8212 may be used as the output driver.

This circuit is sensitive to supply voltage variations and should be used with a stabilized power supply. At very low frequencies the output will switch at the input frequency.



TIME CONSTANT  $R_3 C_2 \ll R_4 C_2 \leq R_7 C_3$   
 VARY  $R_1$  FOR OPTION ZERO CROSSING DETECTION  
 VARY  $R_4$  TO SET DETECTION FREQUENCY

**Figure 18: Frequency Limit Detector**

0328-43

NOTE: All typical values have been characterized but are not tested.

# ICL8211/ICL8212

## i) Switch Bounce Filter (Figure 19)

Single pole single throw (SPST) switches are less costly and more available than single pole double throw (SPDT) switches. SPST switches range from push button and slide types to calculator keyboards. A major problem with the use of switches is the mechanical bounce of the electrical contacts on closure. Contact bounce times can range from a fraction of a millisecond to several tens of milliseconds depending upon the switch type. During this contact bounce time the switch may make and break contact several times. The circuit shown in Figure 19 provides a rapid charge up of  $C_1$  to close to the positive supply voltage ( $V^+$ ) on a switch closure and a corresponding slow discharge of  $C_1$  on a switch break. By proportioning the time constant of  $R_1 C_1$  to approximately the manufacturer's bounce time the output as terminal #4 of the ICL8211/8212 will be a single transition of state per desired switch closure.

## j) Low Voltage Power Disconnect (Figure 20)

There are some classes of circuits that require the power supply to be disconnected if the power supply voltage falls below a certain value. As an example, the National LM199 precision reference has an on chip heater which malfunctions with supply voltages below 9 volts causing an excessive device temperature. The ICL8212 may be used to detect a power supply voltage of 9 volts and turn the power supply off to the LM199 heater section below that voltage.

For further applications, see A027 "Power Supply Design using the ICL8211 and ICL8212."

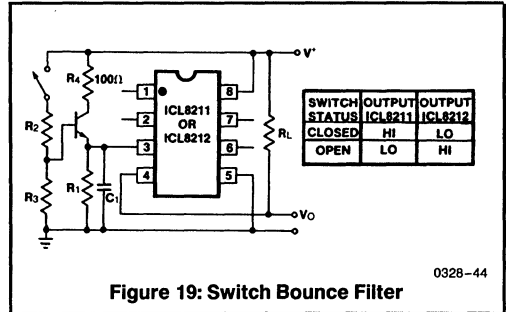


Figure 19: Switch Bounce Filter

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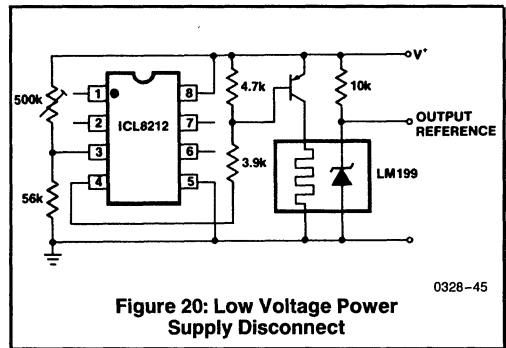


Figure 20: Low Voltage Power Supply Disconnect

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NOTE: Bold type designates a new product from Harris.

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NOTE: Bold type designates a new product from Harris.

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NOTE: Bold type designates a new product from Harris.

# Selection Guide

**SINGLE-SUPPLY:** Min/Max Limits @ +25°C, Unless Otherwise Specified

| DEVICE        | SUPPLY CURRENT<br>mA<br>(MAX) | INPUT OFFSET<br>VOLTAGE<br>mV<br>(MAX) | DOES<br>INPUT<br>INCLUDE<br>GROUND? | RAIL-TO<br>RAIL<br>OUTPUT? | INPUT<br>BIAS<br>CURRENT<br>nA<br>(MAX) | GAIN<br>BANDWIDTH<br>PRODUCT<br>MHz<br>(TYP) | SLEW<br>RATE<br>V/us<br>(TYP) | LARGE<br>SIGNAL<br>GAIN<br>dB<br>(MIN) | OUTPUT<br>CURRENT<br>mA<br>(MIN) |
|---------------|-------------------------------|--|-------------------------------------|----------------------------|---|--|-------------------------------|--|----------------------------------|
| <b>SINGLE</b> |                               |  |                                     |                            |   |  |                               |  |                                  |
| CA3440A       | 0.017                         | 5                                      | YES                                 | NO                         | 0.04                                    | 0.063  | 0.03                          | 80                                     | 15                               |
| CA3440        | 0.017                         | 10                                     | YES                                 | NO                         | 0.05                                    | 0.063  | 0.03                          | 80                                     | 15                               |
| ICL7612A      | 0.02                          | 2                                      | YES                                 | YES                        | 0.05                                    | 0.04   | 0.016                         | 86                                     | 8                                |
| ICL7611A      | 0.02                          | 2                                      | NO                                  | YES                        | 0.05                                    | 0.04   | 0.016                         | 86                                     | 8                                |
| ICL7612D      | 0.02                          | 15                                     | YES                                 | YES                        | 0.05                                    | 0.04   | 0.016                         | 80                                     | 8                                |
| ICL7611D      | 0.02                          | 15                                     | NO                                  | YES                        | 0.05                                    | 0.04   | 0.016                         | 80                                     | 8                                |
| CA5160A       | 0.1                           | 4                                      | YES                                 | YES                        | 0.01                                    | 4  | 10                            | 90                                     | 4                                |
| CA5130A       | 0.1                           | 4                                      | YES                                 | YES                        | 0.01                                    | 4  | 10                            | 90                                     | 4                                |
| CA5160        | 0.1                           | 10                                     | YES                                 | YES                        | 0.015                                   | 4  | 10                            | 85                                     | 4                                |
| CA5130        | 0.1                           | 10                                     | YES                                 | YES                        | 0.015                                   | 4  | 10                            | 85                                     | 4                                |
| CA3130A       | 0.3                           | 5                                      | YES                                 | YES                        | 0.03                                    | 15   | 10                            | 100                                    | 12                               |
| CA3130        | 0.3                           | 15                                     | YES                                 | YES                        | 0.05                                    | 15   | 10                            | 100                                    | 12                               |
| CA5420A       | 0.5                           | 5                                      | YES                                 | YES                        | 0.001                                   | 0.5  | 0.5                           | 85                                     | 1.2                              |
| CA5420        | 0.5                           | 10                                     | YES                                 | YES                        | 0.002                                   | 0.5  | 0.5                           | 85                                     | 1.2                              |
| CA3420A       | 0.65                          | 5                                      | YES                                 | YES                        | 0.005                                   | 0.5  | 0.5                           | 86                                     | 2.6                              |
| CA3420        | 0.65                          | 10                                     | YES                                 | YES                        | 0.005                                   | 0.5  | 0.5                           | 80                                     | 2.6                              |
| CA3140A       | 2.5                           | 5                                      | YES                                 | NO                         | 0.04                                    | 3.7  | 9                             | 86                                     | 12                               |
| CA3140        | 2.5                           | 15                                     | YES                                 | NO                         | 0.05                                    | 3.7  | 9                             | 86                                     | 12                               |
| CA3160A       | 15                            | 5                                      | YES                                 | YES                        | 0.03                                    | 4  | 10                            | 94                                     | 12                               |
| CA3160        | 15                            | 15                                     | YES                                 | YES                        | 0.05                                    | 4  | 10                            | 94                                     | 12                               |
| <b>DUALS</b>  |                               |  |                                     |                            |   |  |                               |  |                                  |
| HA-5142       | 0.16                          | 6                                      | YES                                 | NO                         | 100                                     | 0.4  | 1.5                           | 86                                     | 4.5                              |
| ICL7621A      | 0.25                          | 2                                      | NO                                  | YES                        | 0.05                                    | 0.5  | 0.16                          | 86                                     | 8                                |
| ICL7621D      | 0.25                          | 15                                     | NO                                  | YES                        | 0.05                                    | 0.5  | 0.16                          | 80                                     | 8                                |
| CA158A        | 1.2                           | 3                                      | YES                                 | NO                         | 100                                     | 1  | 0.5                           | 88                                     | 20                               |
| CA358         | 1.2                           | 7                                      | YES                                 | NO                         | 250                                     | 1  | 0.5                           | 88                                     | 20                               |
| CA5260A       | 2                             | 4                                      | YES                                 | YES                        | 0.015                                   | 3  | 5                             | 83                                     | 1.75                             |
| CA3260A       | 2                             | 5                                      | YES                                 | YES                        | 0.03                                    | 4  | 10                            | 94                                     | 12                               |
| CA5260        | 2                             | 15                                     | YES                                 | YES                        | 0.015                                   | 3  | 5                             | 80                                     | 1.75                             |
| CA3260        | 2                             | 15                                     | YES                                 | YES                        | 0.05                                    | 4  | 10                            | 94                                     | 12                               |
| CA3240A       | 2.5                           | 5                                      | YES                                 | NO                         | 0.04                                    | 3.7  | 9                             | 86                                     | 12                               |
| CA3240        | 2.5                           | 15                                     | YES                                 | NO                         | 0.05                                    | 3.7  | 9                             | 86                                     | 12                               |
| <b>QUADS</b>  |                               |  |                                     |                            |   |  |                               |  |                                  |
| ICL7642C      | 0.022                         | 10                                     | NO                                  | YES                        | 0.05                                    | 0.044  | 0.016                         | 80                                     | 8                                |
| ICL7642E      | 0.022                         | 20                                     | NO                                  | YES                        | 0.05                                    | 0.044  | 0.016                         | 80                                     | 8                                |
| HA-5144       | 0.32                          | 6                                      | YES                                 | NO                         | 100                                     | 0.4  | 1.5                           | 86                                     | 4.5                              |
| CA324         | 2                             | 7                                      | YES                                 | NO                         | 250                                     | 1  | 0.5                           | 86                                     | 10                               |
| CA124         | 2                             | 5                                      | YES                                 | NO                         | 150                                     | 1  | 0.5                           | 94                                     | 10                               |
| ICL7641C      | 2.5                           | 10                                     | NO                                  | YES                        | 0.05                                    | 1.4  | 1.6                           | 80                                     | 8                                |
| ICL7641E      | 2.5                           | 20                                     | NO                                  | YES                        | 0.05                                    | 1.4  | 1.6                           | 80                                     | 8                                |
| CA5470        | 10                            | 22                                     | YES                                 | NO                         | 0.01                                    | 14   | 5                             | 80                                     | 4                                |

# Selection Guide

**PRECISION:** Min/Max Limits @ +25°C, Unless Otherwise Specified

| DEVICE        | OFFSET VOLTAGE (mV) | V <sub>IO</sub> DRIFT (typ) ( $\mu\text{V}/^\circ\text{C}$ ) | BIAS CURRENT (nA) | OFFSET CURRENT (nA) | CMRR (dB) | PSRR (dB) | GBWP (MHz) | SLEW RATE (V/ $\mu\text{s}$ ) | A <sub>VOL</sub> (dB) | SUPPLY CURRENT (mA) |
|---------------|---------------------|--|-------------------|---------------------|-----------|-----------|------------|-------------------------------|-----------------------|---------------------|
| <b>SINGLE</b> |                     |  |                   |                     |           |           |            |                               |                       |                     |
| ICL7650S      | 0.005               | 0.02   | 0.01              | 0.005               | 120       | 120       | 2.0        | 2.5                           | 135                   | 3.0                 |
| HA-5127A      | 0.025               | 0.20   | 40.0              | 35.0                | 114       | 86        | 8.5        | 10.0                          | 120                   | 3.5                 |
| HA-5130       | 0.025               | 0.40   | 2.0               | 2.0                 | 110       | 100       | 2.5        | 0.8                           | 120                   | 1.3                 |
| HA-5137A      | 0.025               | 0.20   | 40.0              | 35.0                | 114       | 100       | 63.0       | 20.0                          | 120                   | 3.5                 |
| HA-5147A      | 0.025               | 0.20   | 40.0              | 35.0                | 114       | 100       | 120.0      | 35.0                          | 120                   | 3.5                 |
| HA-5177A      | 0.025               | 0.10   | 2.0               | 2.0                 | 120       | 110       | 2.0        | 0.8                           | 134                   | 1.7                 |
| HA-5177       | 0.060               | 0.20   | 6.0               | 6.0                 | 110       | 110       | 1.4        | 0.8                           | 126                   | 1.7                 |
| HA-5135       | 0.075               | 0.40   | 4.0               | 4.0                 | 106       | 94        | 2.5        | 0.8                           | 120                   | 1.7                 |
| HA-5137       | 0.100               | 0.40   | 80.0              | 75.0                | 100       | 96        | 63.0       | 20.0                          | 117                   | 3.5                 |
| HA-5147       | 0.100               | 0.40   | 80.0              | 75.0                | 100       | 96        | 140.0      | 35.0                          | 117                   | 3.5                 |
| CA3193A       | 0.200               | 1.00   | 20.0              | 5.0                 | 110       | 100       | 1.2        | 0.25                          | 110                   | 3.5                 |
| HA-7712A      | 0.250               | 2.00   | 0.02              | 0.01                | 90        | 90        | 1.0        | 0.45                          | 108                   | 0.200               |
| HA-7713A      | 0.250               | 2.00   | 0.02              | 0.01                | 90        | 90        | 0.12       | 0.04                          | 108                   | 0.030               |
| HA-5170       | 0.300               | 2.0  | 0.01              | 0.03                | 85        | 85        | 8.0        | 8.0                           | 109                   | 2.5                 |
| HA-7712B      | 0.500               | 2.0  | 0.02              | 0.01                | 80        | 80        | 1.0        | 0.45                          | 100                   | 0.200               |
| HA-7713B      | 0.500               | 2.0  | 0.02              | 0.01                | 80        | 80        | 0.12       | 0.04                          | 100                   | 0.030               |
| <b>DUAL</b>   |                     |  |                   |                     |           |           |            |                               |                       |                     |
| HA-5232       | 0.500               | 5.0  | 10                | 10                  | 100       | 100       | 0.5        | 0.15                          | 108                   | 1.45                |
| HA-5222       | 0.75                | 0.5  | 80                | 50                  | 86        | 86        | 100.0      | 25.0                          | 106                   | 8.00                |
| CA158A        | 2.0                 | 7.0  | 50                | 10                  | 70        | 65        | 1.0        | 0.5                           | 94                    | 1.20                |
| HA-5102       | 2.0                 | 3.0  | 200               | 75                  | 86        | 86        | 60.0       | 3.0                           | 100                   | 5.00                |
| HA-5112       | 2.0                 | 3.0  | 200               | 75                  | 86        | 86        | 60.0       | 20.0                          | 100                   | 5.00                |
| ICL7621       | 2.0                 | 10.0   | 0.05              | 0.03                | 76        | 80        | 1.4        | 1.6                           | 80                    | 2.50                |
| CA3280        | 3.0                 | 5.0  | 5000              | 700                 | 80        | 86        | 9.0        | 125.0                         | 94                    | 4.80                |
| CA258A        | 3.0                 | 7.0  | 80                | 15                  | 70        | 65        | 1.0        | 0.5                           | 94                    | 1.20                |
| CA358A        | 3.0                 | 7.0  | 100               | 30                  | 65        | 65        | 1.0        | 0.5                           | 88                    | 1.20                |
| <b>QUAD</b>   |                     |  |                   |                     |           |           |            |                               |                       |                     |
| HA-5134A      | 0.1                 | 0.3  | 25.0              | 25.0                | 115       | 110       | 4.0        | 0.75                          | 123                   | 8.00                |
| HA-5234       | 0.750               | 5.0  | 10                | 10                  | 100       | 100       | 0.5        | 0.15                          | 108                   | 2.9                 |
| HA-5114       | 2.5                 | 3.0  | 200.0             | 75.0                | 86        | 86        | 60.0       | 20.0                          | 100                   | 6.50                |
| HA-5104       | 2.5                 | 3.0  | 200.0             | 75.0                | 86        | 86        | 60.0       | 3.0                           | 100                   | 6.50                |
| HA-5144       | 6.0                 | 3.0  | 100.0             | 10.0                | 77        | 77        | 0.4        | 0.8                           | 86                    | 0.15                |
| CA224         | 7.0                 | 7.0  | 250.0             | 50.0                | 65        | 65        | 1.0        | 0.5                           | 88                    | 2.00                |
| CA324         | 7.0                 | 7.0  | 250.0             | 50.0                | 65        | 65        | 1.0        | 0.5                           | 86                    | 2.00                |
| CA2902        | 7.0                 | 7.0  | 250.0             | 50.0                | 65        | 65        | 1.0        | 0.5                           | 86                    | 2.00                |



# Selection Guide

**LOW BIAS CURRENT:** Min/Max Limits @ +25°C, Unless Otherwise Specified

| DEVICE        | BIAS CURRENT (nA) | OFFSET CURRENT (nA) | OFFSET VOLTAGE (mV) | CM RANGE ( $\pm$ V) | A <sub>VOL</sub> (dB) | GBWP (typ) (MHz) | SLEW RATE (typ) (V/ $\mu$ s) | CMRR (dB) | PSRR (dB) | CURRENT SUPPLY (mA) |
|---------------|-------------------|---------------------|---------------------|---------------------|-----------------------|------------------|------------------------------|-----------|-----------|---------------------|
| <b>SINGLE</b> |                   |                     |                     |                     |                       |                  |                              |           |           |                     |
| CA5420A       | 0.001             | 0.0005              | 5.0                 | 3.7                 | 85                    | 0.5              | 0.5                          | 75        | 75        | 0.50                |
| CA5420        | 0.002             | 0.0010              | 10.0                | 3.7                 | 85                    | 0.5              | 0.5                          | 70        | 70        | 0.50                |
| CA3420        | 0.005             | 0.004               | 10.0                | 1.0                 | 80                    | 0.5              | 0.5                          | 55        | 60        | 0.65                |
| CA3420A       | 0.005             | 0.004               | 5.0                 | 1.0                 | 86                    | 0.5              | 0.5                          | 60        | 70        | 0.65                |
| CA5130A       | 0.010             | 0.005               | 4.0                 | 2.5                 | 90                    | 4.0              | 10.0                         | 75        | 60        | 0.10                |
| CA5160A       | 0.010             | 0.005               | 4.0                 | 2.5                 | 90                    | 4.0              | 10.0                         | 75        | 60        | 0.10                |
| ICL7650S      | 0.010             | 0.005               | 0.005               | 3.5                 | 135                   | 2.0              | 2.5                          | 120       | 120       | 3.00                |
| CA5130        | 0.015             | 0.010               | 10.0                | 2.5                 | 85                    | 4.0              | 10.0                         | 70        | 55        | 0.10                |
| CA5160        | 0.015             | 0.010               | 10.0                | 2.5                 | 85                    | 4.0              | 10.0                         | 70        | 55        | 0.10                |
| HA-7712A      | 0.02              | 0.01                | 0.250               | 5.0                 | 108                   | 1.0              | 0.45                         | 90        | 90        | 0.200               |
| HA-7713A      | 0.02              | 0.01                | 0.25                | 5.0                 | 108                   | 0.12             | 0.04                         | 90        | 90        | 0.030               |
| HA-7712B      | 0.02              | 0.01                | 0.50                | 5.0                 | 100                   | 1.0              | 0.45                         | 80        | 0         | 0.200               |
| HA-7713B      | 0.02              | 0.01                | 0.50                | 5.0                 | 100                   | 0.12             | 0.04                         | 80        | 80        | 0.030               |
| CA3130A       | 0.030             | 0.020               | 5.0                 | 10.0                | 94                    | 15.0             | 9.0                          | 80        | 80        | 15.00               |
| <b>DUAL</b>   |                   |                     |                     |                     |                       |                  |                              |           |           |                     |
| CA5260        | 0.015             | 0.01                | 15.0                | 11.0                | 80                    | 3.0              | 5.0                          | 70        | 70        | 2.0                 |
| CA5260A       | 0.015             | 0.01                | 4.0                 | 2.5                 | 83                    | 3.0              | 5.0                          | 80        | 75        | 2.0                 |
| CA3260A       | 0.03              | 0.02                | 5.0                 | 13.0                | 94                    | 4.0              | 10.0                         | 80        | 76        | 15.5                |
| CA3240A       | 0.04              | 0.02                | 5.0                 | 13.0                | 86                    | 4.5              | 9.0                          | 70        | 76        | 12.0                |
| CA3240        | 0.05              | 0.03                | 15.0                | 12.0                | 86                    | 4.5              | 9.0                          | 70        | 76        | 12.0                |
| CA3260        | 0.05              | 0.03                | 15.0                | 10.0                | 94                    | 4.0              | 10.0                         | 70        | 70        | 15.5                |
| ICL7621       | 0.05              | 0.03                | 2.0                 | 12.0                | 80                    | 1.4              | 1.6                          | 76        | 80        | 2.5                 |
| HA-5232       | 10.0              | 10                  | 0.50                | 12.0                | 108                   | 0.5              | 0.15                         | 100       | 100       | 1.45                |
| CA158A        | 50.0              | 10.0                | 2.0                 | 13.0                | 94                    | 1.0              | 0.5                          | 70        | 65        | 1.2                 |
| <b>QUAD</b>   |                   |                     |                     |                     |                       |                  |                              |           |           |                     |
| CA5470        | 0.01              | 0.005               | 22.0                | 3.5                 | 80                    | 14.0             | 5.0                          | 55        | 60        | 10.0                |
| ICL7641       | 0.05              | 0.03                | 10.0                | 4.2                 | 80                    | 1.4              | 1.60                         | 70        | 80        | 2.5                 |
| ICL7642       | 0.05              | 0.03                | 10.0                | 4.2                 | 80                    | 1.4              | 1.60                         | 70        | 80        | 2.5                 |
| HA-5234       | 10.0              | 10                  | 0.750               | 12                  | 108                   | 0.5              | 0.15                         | 100       | 100       | 2.90                |
| HA-5134A      | 25.0              | 25.0                | 0.1                 | 10.0                | 123                   | 4.0              | 0.75                         | 115       | 110       | 8.0                 |

# Selection Guide

**WIDEBAND:** Min/Max Limits @ +25°C, Unless Otherwise Specified

| DEVICE        | GBWP<br>(typ)<br>(MHz) | FPBW<br>(MHz) | SLEW<br>RATE<br>(typ)<br>(V/μs) | A <sub>VL</sub><br>(dB)/<br>A <sub>ZOL</sub><br>(V/mA)* | MINIMUM<br>STABLE<br>GAIN | OFFSET<br>VOLTAGE<br>(mV) | BIAS<br>CURRENT<br>(nA) | CMRR<br>(dB) | PSRR<br>(dB) | SUPPLY<br>CURRENT<br>(mA) |
|---------------|------------------------|---------------|---------------------------------|---|---------------------------|---------------------------|-------------------------|--------------|--------------|---------------------------|
| <b>SINGLE</b> |                        |               |                                 |   |                           |                           |                         |              |              |                           |
| HFA-0002      | 1000                   | 4.50          | 250                             | 98  | 10                        | 0.7                       | 700                     | 105          | 90           | 15.0                      |
| HA-2539       | 600                    | 8.70          | 600                             | 80  | 10                        | 10.0                      | 20000                   | 60           | 60           | 25.0                      |
| HA-2839       | 500                    | 10.0          | 625                             | 86  | 10                        | 2.0                       | 14500                   | 75           | 75           | 15                        |
| HA-2840       | 500                    | 10.0          | 625                             | 86  | 10                        | 2.0                       | 14500                   | 75           | 75           | 15                        |
| HA-2850       | 400                    | 5.4           | 340                             | 86  | 10                        | 2.0                       | 14500                   | 75           | 75           | 7.5                       |
| HA-2540       | 400                    | 5.50          | 400                             | 80  | 10                        | 10.0                      | 20000                   | 60           | 60           | 25.0                      |
| HFA-0001      | 350                    | 53.00         | 1000                            | 43  | 1                         | 15.0                      | 50000                   | 45           | 35           | 75.0                      |
| HFA-0005      | 300                    | 22.00         | 420                             | 43  | 1                         | 15.0                      | 50000                   | 45           | 40           | 40.0                      |
| CA3450        | 170                    | 6.56          | 330                             | 60  | 1                         | 15.0                      | 350                     | 50           | 60           | 35.0                      |
| HA-2548       | 150                    | 1.91          | 120                             | 114   | 5                         | 0.9                       | 50                      | 80           | 86           | 18.0                      |
| HA-5190       | 150                    | 5.00          | 200                             | 83  | 5                         | 5.0                       | 15000                   | 74           | 70           | 28.0                      |
| HA-5195       | 150                    | 5.00          | 200                             | 83  | 5                         | 5.0                       | 15000                   | 74           | 70           | 28.0                      |
| HA-5147       | 140                    | 0.45          | 35                              | 117   | 10                        | 0.1                       | 80                      | 100          | 96           | 3.5                       |
| HA-5147A      | 120                    | 0.45          | 35                              | 120   | 10                        | 0.03                      | 40                      | 114          | 100          | 3.5                       |
| HA-5004       | 100                    | 100           | 1200                            | 100   | 1                         | 5.0                       | 5000                    | 58           | 50           | 16                        |
| HA-5020       | 100                    | 9.6           | 600                             | 3500  | 1                         | 8.0                       | 8000                    | 60           | 65           | 10                        |
| HA-2620       | 100                    | 0.40          | 35                              | 100   | 5                         | 4.0                       | 15                      | 80           | 80           | 3.7                       |
| HA-2622       | 100                    | 0.32          | 35                              | 98  | 5                         | 5.0                       | 25                      | 74           | 74           | 4.0                       |
| HA-2625       | 100                    | 0.32          | 35                              | 98  | 5                         | 5.0                       | 25                      | 74           | 74           | 4.0                       |
| HA-5101       | 100                    | 0.10          | 10                              | 120   | 1                         | 3.0                       | 200                     | 80           | 80           | 6.0                       |
| HA-5160       | 100                    | 1.60          | 120                             | 97  | 10                        | 3.0                       | 0.05                    | 74           | 74           | 8.0                       |
| HA-5162       | 100                    | 1.10          | 70                              | 90  | 10                        | 15.0                      | 0.065                   | 70           | 70           | 8.0                       |
| HA-5221       | 100                    | 0.24          | 25                              | 106   | 1                         | 0.75                      | 80                      | 86           | 86           | 8.0                       |
| HA-2842       | 80                     | 6.0           | 375                             | 94  | 2                         | 3.0                       | 10000                   | 85           | 70           | 14                        |
| HA-2841       | 50                     | 4.0           | 250                             | 90  | 1                         | 3.0                       | 10000                   | 80           | 70           | 11                        |
| <b>DUAL</b>   |                        |               |                                 |   |                           |                           |                         |              |              |                           |
| HA-5222       | 100.0                  | 0.24          | 25                              | 106   | 1                         | 0.8                       | 80.0                    | 86           | 86           | 8.0                       |
| HA-5102       | 60.0                   | 0.02          | 3                               | 100   | 1                         | 2.0                       | 200.0                   | 86           | 86           | 5.0                       |
| HA-5112       | 60.0                   | 0.19          | 20                              | 100   | 10                        | 2.0                       | 200.0                   | 86           | 86           | 5.0                       |
| CA3280        | 9.0                    | 1.99          | 125                             | 94  | 1                         | 3.0                       | 5000.0                  | 80           | 86           | 4.8                       |
| CA3280A       | 9.0                    | 1.99          | 125                             | 94  | 1                         | 0.5                       | 5000.0                  | 94           | 94           | 4.8                       |
| CA3240        | 4.5                    | 0.14          | 9                               | 86  | 1                         | 15.0                      | 0.05                    | 70           | 76           | 12.0                      |
| CA3240A       | 4.5                    | 0.14          | 9                               | 86  | 1                         | 5.0                       | 0.04                    | 70           | 76           | 12.0                      |
| CA3260        | 4.0                    | 0.16          | 10                              | 94  | 1                         | 15.0                      | 0.05                    | 70           | 70           | 15.5                      |
| CA3260A       | 4.0                    | 0.16          | 10                              | 94  | 1                         | 5.0                       | 0.03                    | 80           | 76           | 15.5                      |
| CA5260        | 3.0                    | 0.10          | 5                               | 80  | 1                         | 15.0                      | 0.02                    | 70           | 70           | 2.0                       |
| CA5260A       | 3.0                    | 0.10          | 5                               | 83  | 1                         | 4.0                       | 0.02                    | 80           | 75           | 2.0                       |
| <b>QUAD</b>   |                        |               |                                 |   |                           |                           |                         |              |              |                           |
| HA-5104       | 60.0                   | 0.02          | 3.0                             | 100   | 1                         | 2.5                       | 200.0                   | 86           | 86           | 6.5                       |
| HA-5114       | 60.0                   | 0.19          | 20.0                            | 100   | 10                        | 2.5                       | 200.0                   | 86           | 86           | 6.5                       |
| HA-2444       | 45.0                   | 5.1           | 160                             | 71  | 1                         | 7.0                       | 15000                   | 70           | 65           | 25                        |
| HA-2400       | 40.0                   | 0.20          | 30.0                            | 94  | 1                         | 9.0                       | 200.0                   | 80           | 74           | 6.0                       |
| HA-2404       | 40.0                   | 0.20          | 30.0                            | 94  | 1                         | 9.0                       | 200.0                   | 80           | 74           | 6.0                       |
| HA-2405       | 40.0                   | 0.20          | 30.0                            | 94  | 1                         | 9.0                       | 250.0                   | 74           | 74           | 6.0                       |
| HA-2406       | 30.0                   | 0.24          | 20.0                            | 92  | 1                         | 10.0                      | 250.0                   | 74           | 74           | 7.0                       |
| CA5470        | 14.0                   | 0.01          | 5.0                             | 80  | 1                         | 22.0                      | 0.01                    | 55           | 60           | 10.0                      |
| HA-5134A      | 4.0                    | 0.02          | 0.8                             | 123   | 1                         | 0.1                       | 25.0                    | 115          | 110          | 8.0                       |

\* A<sub>ZOL</sub> applies to current feedback amplifiers only (HA-5004, HA-5020)

# Selection Guide

**HIGH SLEW RATE:** Min/Max Limits @ +25°C, Unless Otherwise Specified

| DEVICE        | SLEW RATE (typ) (V/ $\mu$ s) | GBWP (typ) (MHz) | FPBW (MHz) | AVOL (dB)/AZOL (V/mA)* | MINIMUM STABLE GAIN | OFFSET VOLTAGE (mV) | BIAS CURRENT (nA) | CMRR (dB) | PSRR (dB) | SUPPLY CURRENT (mA) |
|---------------|------------------------------|------------------|------------|------------------------|---------------------|---------------------|-------------------|-----------|-----------|---------------------|
| <b>SINGLE</b> |                              |                  |            |                        |                     |                     |                   |           |           |                     |
| HA-5004       | 1200                         | 100              | 100        | 100                    | 1                   | 5.0                 | 5000              | 58        | 50        | 16                  |
| HFA-0001      | 1000                         | 350              | 4.5        | 43                     | 1                   | 15.0                | 50000             | 45        | 35        | 75.0                |
| HA-5020       | 800                          | 100              | 9.6        | 3500                   | 1                   | 8.0                 | 8000              | 60        | 64        | 10                  |
| HA-2839       | 625                          | 500              | 10.0       | 86                     | 10                  | 2.0                 | 14500             | 75        | 75        | 15                  |
| HA-2840       | 625                          | 500              | 10.0       | 86                     | 10                  | 2.0                 | 14500             | 75        | 75        | 15                  |
| HA-2539       | 600                          | 600              | 8.7        | 80                     | 10                  | 10.0                | 20000             | 60        | 60        | 25.0                |
| HFA-0005      | 420                          | 300              | 22.0       | 43                     | 1                   | 15.0                | 50000             | 45        | 40        | 40.0                |
| HA-2540       | 400                          | 400              | 5.5        | 80                     | 10                  | 10.0                | 20000             | 60        | 60        | 25.0                |
| HA-2842       | 375                          | 80               | 6.0        | 94                     | 2                   | 3.0                 | 10000             | 85        | 70        | 14                  |
| HA-2542       | 350                          | 70               | 4.7        | 80                     | 2                   | 10.0                | 35000             | 70        | 70        | 35.0                |
| HA-2850       | 340                          | 400              | 5.4        | 86                     | 10                  | 2.0                 | 14500             | 75        | 75        | 7.5                 |
| CA3450        | 330                          | 170              | 6.6        | 60                     | 1                   | 15.0                | 350               | 50        | 60        | 35.0                |
| HA-2841       | 250                          | 50               | 4.0        | 90                     | 1                   | 3.0                 | 10000             | 80        | 70        | 11                  |
| HA-2541       | 250                          | 40               | 3.0        | 80                     | 1                   | 2.0                 | 25000             | 70        | 70        | 40.0                |
| HFA-0002      | 250                          | 1000             | 4.5        | 98                     | 10                  | 0.7                 | 700               | 105       | 90        | 15.0                |
| HA-5190       | 200                          | 150              | 5.0        | 83                     | 5                   | 5.0                 | 15000             | 74        | 70        | 28.0                |
| HA-5195       | 200                          | 150              | 5.0        | 83                     | 5                   | 5.0                 | 15000             | 74        | 70        | 28.0                |
| HA-2529       | 150                          | 20               | 2.1        | 80                     | 3                   | 5.0                 | 200               | 80        | 80        | 6.0                 |
| HA-2544       | 150                          | 50               | 3.2        | 71                     | 1                   | 15.0                | 15000             | 75        | 70        | 12.0                |
| HA-2520       | 120                          | 20               | 1.5        | 80                     | 3                   | 8.0                 | 200               | 80        | 80        | 6.0                 |
| HA-2522       | 120                          | 20               | 1.2        | 78                     | 3                   | 10.0                | 250               | 74        | 74        | 6.0                 |
| HA-2525       | 120                          | 20               | 1.2        | 78                     | 3                   | 10.0                | 250               | 74        | 74        | 6.0                 |
| HA-2548       | 120                          | 150              | 1.91       | 114                    | 5                   | 0.9                 | 50                | 80        | 86        | 18.0                |
| HA-5160       | 120                          | 100              | 1.600      | 97                     | 10                  | 3                   | 0.05              | 74        | 74        | 8                   |
| <b>DUAL</b>   |                              |                  |            |                        |                     |                     |                   |           |           |                     |
| CA3280        | 125                          | 9.0              | 1.99       | 94                     | 1                   | 3.0                 | 5000              | 80        | 86        | 4.8                 |
| CA3280A       | 125                          | 9.0              | 1.99       | 94                     | 1                   | 0.5                 | 5000              | 94        | 94        | 4.8                 |
| HA-5222       | 25                           | 100              | 0.24       | 106                    | 1                   | 0.75                | 80                | 86        | 86        | 8.0                 |
| HA-5112       | 20                           | 60               | 0.19       | 100                    | 10                  | 2.0                 | 200               | 86        | 86        | 5.0                 |
| CA3260        | 10                           | 4.0              | 0.16       | 94                     | 1                   | 15.0                | 0.05              | 70        | 70        | 15.5                |
| CA3260A       | 10                           | 4.0              | 0.16       | 94                     | 1                   | 5.0                 | 0.03              | 80        | 76        | 15.5                |
| CA3240        | 9.0                          | 4.5              | 0.14       | 86                     | 1                   | 15.0                | 0.05              | 70        | 76        | 12.0                |
| CA3240A       | 9.0                          | 4.5              | 0.14       | 86                     | 1                   | 5.0                 | 0.04              | 70        | 76        | 12.0                |
| CA5260A       | 5.0                          | 3.0              | 0.10       | 83                     | 1                   | 4.0                 | 0.015             | 80        | 75        | 2.0                 |
| <b>QUAD</b>   |                              |                  |            |                        |                     |                     |                   |           |           |                     |
| HA-2444       | 160                          | 45               | 5.1        | 71                     | 1                   | 7.0                 | 15000             | 70        | 65        | 25                  |
| HA-2400       | 30                           | 40               | 0.20       | 94                     | 1                   | 9.0                 | 200               | 80        | 74        | 6                   |
| HA-2404       | 30                           | 40               | 0.20       | 94                     | 1                   | 9.0                 | 200               | 80        | 74        | 6                   |
| HA-2405       | 30                           | 40               | 0.20       | 94                     | 1                   | 9.0                 | 250               | 74        | 74        | 6                   |
| HA-2406       | 20                           | 30               | 0.24       | 92                     | 1                   | 10.0                | 250               | 74        | 74        | 7                   |
| HA-5114       | 20                           | 60               | 0.191      | 100                    | 10                  | 2.5                 | 200               | 86        | 86        | 6.5                 |
| CA5470        | 5.0                          | 14               | 0.01       | 80                     | 1                   | 22.0                | 0.01              | 55        | 60        | 10                  |

\* AZOL applies to current feedback amplifiers only (HA-5004, HA-5020)

# Selection Guide

**LOW POWER:** Min/Max Limits @ +25°C, Unless Otherwise Specified

| DEVICE        | SUPPLY CURRENT (mA) | MAX V+, V- (±V) | SLEW RATE (typ) (V/μs) | GBWP (typ) (MHz) | CM RANGE (±V) | OUTPUT VOLTAGE SWING (±V) | OUTPUT CURRENT (mA) | OFFSET VOLTAGE (mV) | BIAS CURRENT (nA) | PSRR (dB) |
|---------------|---------------------|-----------------|------------------------|------------------|---------------|---------------------------|---------------------|---------------------|-------------------|-----------|
| <b>SINGLE</b> |                     |                 |                        |                  |               |                           |                     |                     |                   |           |
| CA3440        | 0.017               | 12.5            | 0.03                   | 0.063            | 3.5           | 3.0                       | 15.0                | 10.0                | 0.050             | 70        |
| CA3440A       | 0.017               | 12.5            | 0.03                   | 0.063            | 3.5           | 3.0                       | 15.0                | 5.0                 | 0.040             | 70        |
| CA3078A       | 0.02                | 18.0            | 1.5                    | 0.002            | 5.5           | 5.1                       | 12.0                | 3.5                 | 12.0              | 70        |
| ICL7611A      | 0.02                | 9.0             | 0.02                   | 0.044            | 4.4           | 4.9                       | 8.0                 | 2.0                 | 0.05              | 80        |
| ICL7612A      | 0.02                | 9.0             | 0.02                   | 0.044            | 5.3           | 4.9                       | 8.0                 | 2.0                 | 0.05              | 80        |
| HA-7713A      | 0.03                | 9               | 0.04                   | 0.12             | 5             | 4.95                      | 10                  | 0.25                | 0.020             | 90        |
| HA-7713B      | 0.03                | 9               | 0.04                   | 0.12             | 5             | 4.95                      | 10                  | 0.500               | 0.020             | 80        |
| CA5130        | 0.10                | 8.0             | 10.0                   | 4.0              | 2.5           | 2.5                       | 4.0                 | 10.0                | 0.015             | 55        |
| CA5130A       | 0.10                | 8.0             | 10.0                   | 4.0              | 2.5           | 2.5                       | 4.0                 | 4.0                 | 0.010             | 60        |
| CA5160        | 0.10                | 8.0             | 10.0                   | 4.0              | 2.5           | 2.5                       | 4.0                 | 10.0                | 0.015             | 55        |
| CA5160A       | 0.10                | 8.0             | 10.0                   | 4.0              | 2.5           | 2.5                       | 4.0                 | 4.0                 | 0.010             | 60        |
| CA3078        | 0.13                | 7.0             | 1.5                    | 0.002            | 5.5           | 5.1                       | 12.0                | 4.5                 | 170.0             | 70        |
| HA-7712A      | 0.200               | 9               | 0.45                   | 1.0              | 5             | 4.95                      | 25                  | 0.250               | 0.02              | 90        |
| HA-7712B      | 0.200               | 9               | 0.45                   | 1.0              | 5             | 4.95                      | 25                  | 0.500               | 0.02              | 80        |
| CA3094        | 0.40                | 12.0            | 50.0                   | 30.0             | 12.0          | 14.9                      | 100.0               | 5.0                 | 5000.0            | 70        |
| CA3094A       | 0.40                | 18.0            | 50.0                   | 30.0             | 12.0          | 14.9                      | 100.0               | 5.0                 | 5000.0            | 70        |
| CA3094B       | 0.40                | 22.0            | 50.0                   | 30.0             | 12.0          | 14.9                      | 100.0               | 5.0                 | 5000.0            | 70        |
| <b>DUAL</b>   |                     |                 |                        |                  |               |                           |                     |                     |                   |           |
| ICL7621A      | 0.25                | 9.0             | 0.2                    | 0.5              | 4.2           | 4.9                       | 8.0                 | 2.0                 | 0.05              | 80        |
| HA-7712A      | 0.400               | 9               | 0.45                   | 1.0              | 5             | 4.95                      | 25                  | 0.250               | 0.02              | 90        |
| HA-7712B      | 0.400               | 9               | 0.45                   | 1.0              | 5             | 4.95                      | 25                  | 0.500               | 0.02              | 80        |
| CA158A        | 1.2                 | 13.0            | 0.5                    | 1.0              | 13.0          | 13.0                      | 20.0                | 2.0                 | 50.0              | 65        |
| CA258A        | 1.2                 | 6.5             | 0.5                    | 1.0              | 13.0          | 13.0                      | 20.0                | 3.0                 | 80.0              | 65        |
| CA2904        | 1.2                 | 6.5             | 0.5                    | 1.0              | 13.0          | 13.0                      | 20.0                | 7.0                 | 250.0             | 50        |
| CA258         | 1.2                 | 6.5             | 0.5                    | 1.0              | 13.0          | 13.0                      | 20.0                | 5.0                 | 150.0             | 65        |
| CA358         | 1.2                 | 13.0            | 0.5                    | 1.0              | 13.0          | 13.0                      | 20.0                | 7.0                 | 250.0             | 65        |
| CA158         | 1.2                 | 16.0            | 0.5                    | 1.0              | 13.0          | 13.0                      | 20.0                | 5.0                 | 150.0             | 65        |
| CA358A        | 1.2                 | 13.0            | 0.5                    | 1.0              | 13.0          | 13.0                      | 20.0                | 3.0                 | 100.0             | 65        |
| HA-5232       | 1.45                | 18              | 0.15                   | 0.5              | 12            | 12                        | 20                  | 0.500               | 10                | 100       |
| CA124         | 2.0                 | 16.0            | 0.5                    | 1.0              | 13.0          | 26.0                      | 10.0                | 5.0                 | 150.0             | 65        |
| CA5260        | 2.0                 | 8.0             | 5.0                    | 3.0              | 2.5           | 3.0                       | 1.75                | 15.0                | 0.015             | 70        |
| <b>QUAD</b>   |                     |                 |                        |                  |               |                           |                     |                     |                   |           |
| ICL7642       | 0.02                | 9.0             | 0.02                   | 0.04             | 4.2           | 4.5                       | 8.0                 | 10.0                | 0.05              | 80        |
| HA-5144       | 0.15                | 17.5            | 0.8                    | 0.4              | 10.0          | 10.0                      | 4.5                 | 6.0                 | 100.0             | 77        |
| CA224         | 2.00                | 16.0            | 0.5                    | 1.0              | 13.0          | 13.0                      | 10.0                | 7.0                 | 250.0             | 65        |
| CA324         | 2.00                | 16.0            | 0.5                    | 1.0              | 13.0          | 13.0                      | 10.0                | 7.0                 | 250.0             | 65        |
| ICL7641       | 2.50                | 9.0             | 1.6                    | 1.4              | 4.2           | 4.5                       | 8.0                 | 10.0                | 0.05              | 80        |
| HA-5234       | 2.90                | 18              | 0.15                   | 0.5              | 12            | 12                        | 20                  | 0.750               | 10                | 100       |

**3**  
OPERATIONAL AMPLIFIERS



**Quad Operational Amplifiers  
For Commercial, Industrial, and Military Applications**

August 1991

**Features**

- Operation from Single or Dual Supplies
- Unity-Gain Bandwidth ..... 1MHz (Typ.)
- DC Voltage Gain ..... 100dB (Typ.)
- Input Bias Current ..... 45nA (Typ.)
- Input Offset Voltage ..... 2mV (Typ.)
- Input Offset Current
  - ▶ CA224, CA324, CA2902, LM324, LM2902 ..... 5nA (Typ.)
  - ▶ CA124 ..... 3nA (Typ.)
- Replacement for Industry Types 124, 224, 324

**Applications**

- Summing Amplifiers
- Multivibrators
- Oscillators
- Transducer Amplifiers
- DC Gain Blocks

**Description**

The CA124, CA224, CA324, CA2902, LM324, and LM2902 consist of four independent, high-gain operational amplifiers on a single monolithic substrate. An on-chip capacitor in each of the amplifiers provides frequency compensation for unity gain. These devices are designed specially to operate from either single or dual supplies, and the differential voltage range is equal to the power-supply voltage. Low power drain and an input common-mode voltage range from 0 V to V+ -1.5 V (single-supply operation) make these devices suitable for battery operation.

The CA124, CA224, CA324, CA2902, LM324 and LM2902 are supplied in both 14-lead dual-in-line plastic (E suffix) and 14-lead (150 mil) small outline (M suffix) packages. The CA324 is available in chip form (H suffix).

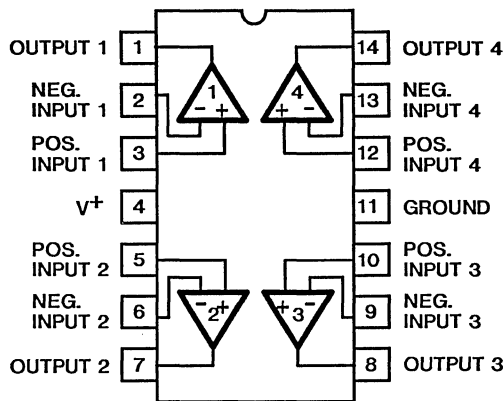
**Pinout**


FIGURE 1.

\* Technical Data on LM Branded types is identical to the corresponding CA Branded types.  
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.  
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# CA124, CA224, CA324, CA2902, LM324, LM2902

## MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^\circ\text{C}$

|   |  |
|---|--|
| SUPPLY VOLTAGE . . . . .  | 32 V or $\pm 16$ V                           |
| DIFFERENTIAL INPUT VOLTAGE . . . . .                            | $\pm 32$ V                                   |
| INPUT VOLTAGE . . . . .   | -0.3 V to +32 V                              |
| INPUT CURRENT ( $V_I < -0.3$ V) <sup>†</sup> . . . . .          | 50 mA  |
| OUTPUT SHORT CIRCUIT TO GROUND<br>( $V^+ \leq 15$ V)* . . . . . | Continuous                                   |
| DEVICE DISSIPATION:   |  |
| Up to $T_A = 55^\circ\text{C}$ . . . . .                        | 750 mW                                       |
| Above $T_A = 55^\circ\text{C}$ . . . . .                        | derate linearly at 6.67 mW/ $^\circ\text{C}$ |
| AMBIENT TEMPERATURE RANGE:                                      |  |
| Operating . . . . .   | -55 to +125 $^\circ\text{C}$                 |
| Storage . . . . .   | -65 to +150 $^\circ\text{C}$                 |
| LEAD TEMPERATURE (DURING SOLDERING):                            |  |
| At distance 1/16 $\pm$ 1/32 in. (1.59 $\pm$ 0.79 mm)            |  |
| from case for 10 seconds max. . . . .                           | +265 $^\circ\text{C}$                        |

\*The maximum output current is approximately 40 mA independent of the magnitude of  $V^+$ . Continuous short circuits at  $V^+ > 15$  V can cause excessive power dissipation and eventual destruction. Short circuits from the output to  $V^+$  can cause overheating and eventual destruction of the device.

†This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector-base junction of the input p-n-p transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral n-p-n parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the  $V^+$  voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3 V dc.

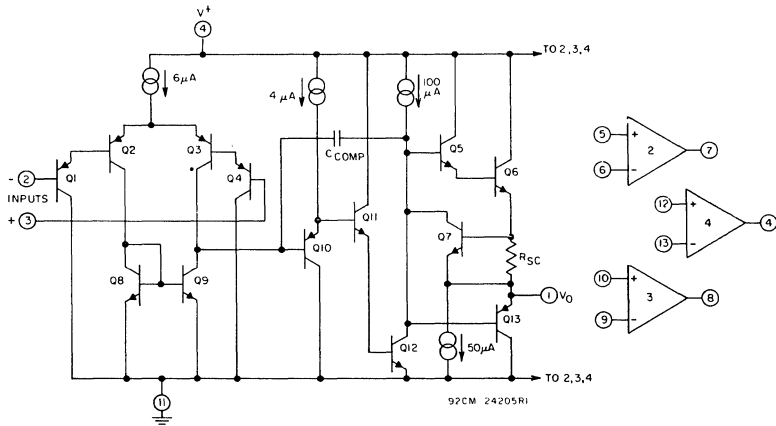


Fig. 2—Schematic diagram—one of four operational amplifiers.

CA124, CA224, CA324, CA2902, LM324, LM2902

ELECTRICAL CHARACTERISTICS (Values Apply For Each Operational Amplifier)

| CHARACTERISTIC   | TEST CONDITIONS<br>Supply Voltage ( $V^+$ ) = 5 V<br>Unless Otherwise Specified | CA124<br>LIMITS      |      |             | UNITS                        |    |
|--|---|----------------------|------|-------------|------------------------------|----|
|  |   | Min.                 | Typ. | Max.        |                              |    |
| $T_A = 25^\circ\text{C}$   |   |                      |      |             |                              |    |
| Input Offset Voltage, $V_{IO}$                                   | Note 3  | –                    | 2    | 5           | mV                           |    |
| Output Voltage Swing, $V_{OPP}$                                  | $R_L = 2\text{ k}\Omega$  | 0                    | –    | $V^+ - 1.5$ | V                            |    |
| Input Common-Mode Voltage Range, $V_{ICR}$                       | Note 2, $V^+ = 30\text{ V}$   | 0                    | –    | $V^+ - 1.5$ | V                            |    |
| Input Offset Current, $I_{IO}$                                   | $I_1^+ - I_1^-$   | –                    | 3    | 30          | nA                           |    |
| Input Bias Current, $I_{IB}$                                     | $I_1^+$ or $I_1^-$ , Note 1   | –                    | 45   | 150         | nA                           |    |
| Output Current (Source), $I_O$                                   | $V_1^+ = +1\text{ V}$ , $V_1^- = 0\text{ V}$ ,<br>$V^+ = 15\text{ V}$           | 20                   | 40   | –           | mA                           |    |
| Output Current (Sink), $I_O$                                     | $V_1^+ = 0\text{ V}$ , $V_1^- = 1\text{ V}$ , $V^+ = 15\text{ V}$               | 10                   | 20   | –           | mA                           |    |
|  | $V_1^+ = 0\text{ V}$ , $V_1^- = 1\text{ V}$ ,<br>$V_O = 200\text{ mV}$          | 12                   | 50   | –           | $\mu\text{A}$                |    |
| Large-Signal Voltage Gain, A                                     | $R_L \geq 2\text{ k}\Omega$ , $V^+ = 15\text{ V}$<br>(For large $V_O$ swing)    | 94                   | 100  | –           | dB                           |    |
| Common-Mode Rejection Ratio, CMRR                                | DC  | 70                   | 85   | –           | dB                           |    |
| Power Supply Rejection Ratio, PSRR                               | DC  | 65                   | 100  | –           | dB                           |    |
| Amplifier-to-Amplifier Coupling                                  | f = 1 to 20 kHz (Input referred)  | –                    | –120 | –           | dB                           |    |
| $T_A = -55\text{ to }+125^\circ\text{C}$                         |   |                      |      |             |                              |    |
| Input Offset Voltage, $V_{IO}$                                   | Note 3  | –                    | –    | 7           | mV                           |    |
| Temperature Coefficient of Input Offset Voltage, $\alpha V_{IO}$ | $R_S = 0$   | –                    | 7    | –           | $\mu\text{V}/^\circ\text{C}$ |    |
| Input Offset Current, $I_{IO}$                                   | $I_1^+ - I_1^-$   | –                    | –    | 100         | nA                           |    |
| Temperature Coefficient of Input Offset Current, $\alpha I_{IO}$ |   | –                    | 10   | –           | $\text{pA}/^\circ\text{C}$   |    |
| Input Bias Current, $I_{IB}$                                     | $I_1^+$ or $I_1^-$  | –                    | –    | 300         | nA                           |    |
| Total Supply Current, $I^+$                                      | $R_L = \infty$ On All Ampl.   | –                    | 0.8  | 2           | mA                           |    |
| Input Common-Mode Voltage Range, $V_{ICR}$                       | $V^+ = 30\text{ V}$   | 0                    | –    | $V^+ - 2$   | V                            |    |
| Large-Signal Voltage Gain, A                                     | $R_L \geq 2\text{ k}\Omega$ , $V^+ = 15\text{ V}$<br>(For large $V_O$ swing)    | 88                   | –    | –           | dB                           |    |
| Output Voltage Swing:  | $R_L = 2\text{ k}\Omega$ , $V^+ = 30\text{ V}$                                  | High-Level, $V_{OH}$ | 26   | –           | –                            | V  |
|  |   | Low-Level, $V_{OL}$  | 27   | 28          | –                            |    |
|  | $R_L = 10\text{ k}\Omega$   | –                    | 5    | 20          | mV                           |    |
| Output Current:  | $V_1^+ = 1\text{ V}_{DC}$ , $V_1^- = 0$ ,<br>$V^+ = 15\text{ V}$                | Source, $I_O$        | 10   | 20          | –                            | mA |
|  |   | Sink, $I_O$          | 5    | 8           | –                            | mA |
| Differential Input Voltage                                       | Note 2  | –                    | –    | $V^+$       | V                            |    |

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because the current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltage and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is  $V^+ - 1.5\text{ V}$ , but either or both inputs can go to  $+32\text{ V}$  without damage.

NOTE 3:  $V_O = 1.4\text{ V}_{DC}$ ,  $R_S = 0\ \Omega$  with  $V^+$  from 5 V to 30 V; and over the full input common-mode voltage range (0 V to  $V^+ - 1.5\text{ V}$ ).



**CA124, CA224, CA324, CA2902, LM324, LM2902**

**ELECTRICAL CHARACTERISTICS (Values apply for each operational amplifier)**

| CHARACTERISTIC  | TEST CONDITIONS<br>Supply Voltage ( $V^+$ ) = 5 V<br>Unless Otherwise Specified | CA224, CA324<br>LIMITS |      |             | UNITS                        |
|---|---|------------------------|------|-------------|------------------------------|
|   |   | Min.                   | Typ. | Max.        |                              |
| $T_A = 25^\circ\text{C}$  |   |                        |      |             |                              |
| Input Offset Voltage, $V_{IO}$  | Note 3  | –                      | 2    | 7           | mV                           |
| Output Voltage Swing, $V_{OPP}$   | $R_L = 2\text{ k}\Omega$  | 0                      | –    | $V^+ - 1.5$ | V                            |
| Input Common-Mode Voltage Range, $V_{ICR}$  | Note 2, $V^+ = 30\text{ V}$   | 0                      | –    | $V^+ - 1.5$ | V                            |
| Input Offset Current, $I_{IO}$  | $I_1^+ - I_1^-$   | –                      | 5    | 50          | nA                           |
| Input Bias Current, $I_{IB}$  | $I_1^+$ or $I_1^-$ , Note 1   | –                      | 45   | 250         | nA                           |
| Output Current (Source), $I_O$  | $V_1^+ = +1\text{ V}$ , $V_1^- = 0\text{ V}$ ,<br>$V^+ = 15\text{ V}$           | 20                     | 40   | –           | mA                           |
| Output Current (Sink), $I_O$  | $V_1^+ = 0\text{ V}$ , $V_1^- = 1\text{ V}$ , $V^+ = 15\text{ V}$               | 10                     | 20   | –           | mA                           |
|   | $V_1^+ = 0\text{ V}$ , $V_1^- = 1\text{ V}$ ,<br>$V_O = 200\text{ mV}$          | 12                     | 50   | –           | $\mu\text{A}$                |
| Large-Signal Voltage Gain, A  | $R_L \geq 2\text{ k}\Omega$ , $V^+ = 15\text{ V}$<br>(For large $V_O$ swing)    | 88                     | 100  | –           | dB                           |
| Common-Mode Rejection Ratio, CMRR   | DC  | 65                     | 70   | –           | dB                           |
| Power Supply Rejection Ratio, PSRR  | DC  | 65                     | 100  | –           | dB                           |
| Amplifier-to-Amplifier Coupling   | $f = 1\text{ to }20\text{ kHz}$<br>(Input referred)                             | –                      | –120 | –           | dB                           |
| $T_A = -40\text{ to }+85^\circ\text{C}$ (CA224), $T_A = 0\text{ to }70^\circ\text{C}$ (CA324) |   |                        |      |             |                              |
| Input Offset Voltage, $V_{IO}$  | Note 3  | –                      | –    | 9           | mV                           |
| Temperature Coefficient of Input Offset Voltage, $\alpha V_{IO}$                              | $R_S = 0$   | –                      | 7    | –           | $\mu\text{V}/^\circ\text{C}$ |
| Input Offset Current, $I_{IO}$  | $I_1^+ - I_1^-$   | –                      | –    | 150         | nA                           |
| Temperature Coefficient of Input Offset Current, $\alpha I_{IO}$                              |   | –                      | 10   | –           | $\text{pA}/^\circ\text{C}$   |
| Input Bias Current, $I_{IB}$  | $I_1^+$ or $I_1^-$  | –                      | –    | 500         | nA                           |
| Total Supply Current, $I^+$   | $R_L = \infty$ On All Ampl.   | –                      | 0.8  | 2           | mA                           |
| Input Common-Mode Voltage Range, $V_{ICR}$  | $V^+ = 30\text{ V}$   | 0                      | –    | $V^+ - 2$   | V                            |
| Large-Signal Voltage Gain, A  | $R_L \geq 2\text{ k}\Omega$ , $V^+ = 15\text{ V}$<br>(For large $V_O$ swing)    | 83                     | –    | –           | dB                           |
| Output Voltage Swing:   |   |                        |      |             |                              |
| High-Level, $V_{OH}$  | $R_L = 2\text{ k}\Omega$ , $V^+ = 30\text{ V}$                                  | 26                     | –    | –           | V                            |
|   | $R_L = 10\text{ k}\Omega$   | 27                     | 28   | –           |                              |
| Low-Level, $V_{OL}$   | $R_L = 10\text{ k}\Omega$   | –                      | 5    | 20          | mV                           |
| Output Current:   |   |                        |      |             |                              |
| Source, $I_O$   | $V_1^+ = 1\text{ V}_{DC}$ , $V_1^- = 0$ ,<br>$V^+ = 15\text{ V}$                | 10                     | 20   | –           | mA                           |
| Sink, $I_O$   | $V_1^- = 1\text{ V}_{DC}$ , $V_1^+ = 0$ ,<br>$V^+ = 15\text{ V}$                | 5                      | 8    | –           | mA                           |
| Differential Input Voltage  | Note 2  | –                      | –    | $V^+$       | V                            |

**NOTE 1:** Due to the p–n–p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because the current is essentially constant, independent of the state of the output.

**NOTE 2:** The input signal voltage and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is  $V^+ - 1.5\text{ V}$ , but either or both inputs can go to +32 V without damage.

**NOTE 3:**  $V_O = 1.4\text{ V}_{DC}$ ,  $R_S = 0\ \Omega$  with  $V^+$  from 5 V to 30 V; and over the full input common-mode voltage range (0 V to  $V^+ - 1.5\text{ V}$ ).

CA124, CA224, CA324, CA2902, LM324, LM2902

ELECTRICAL CHARACTERISTICS (Values apply for each operational amplifier)

| CHARACTERISTIC   | TEST CONDITIONS  | 2902 LIMITS |      |           | UNITS                        |
|--|--|-------------|------|-----------|------------------------------|
|  | Supply Voltage ( $V^+$ ) = 5 V<br>Unless Otherwise Specified   | Min.        | Typ. | Max.      |                              |
| $T_A = -40$ to $+85^\circ\text{C}$ (CA2902)                      |  |             |      |           |                              |
| Input Offset Voltage, $V_{IO}$                                   | Note 3   | -           | -    | 10        | mV                           |
| Temperature Coefficient of Input Offset Voltage, $\alpha V_{IO}$ | $R_S = 0$  | -           | 7    | -         | $\mu\text{V}/^\circ\text{C}$ |
| Input Offset Current, $I_{IO}$                                   | $I_1^+ - I_1^-$  | -           | 45   | 200       | nA                           |
| Temperature Coefficient of Input Offset Current, $\alpha I_{IO}$ |  | -           | 10   | -         | $\text{pA}/^\circ\text{C}$   |
| Input Bias Current, $I_{IB}$                                     | $I_1^+$ or $I_1^-$ , Note 1                                    | -           | 40   | 500       | nA                           |
| Input Common-Mode Voltage Range, $V_{ICR}$                       | $V^+ = 26$ V, Note 2   | 0           | -    | $V^+ - 2$ | V                            |
| Supply Current, $I^+$  | $R_L = \infty$ On All Ampl.                                    | -           | 0.7  | 1.2       | mA                           |
|  | $R_L = \infty, V^+ = 26$ V                                     | -           | 1.5  | 3         |                              |
| Large-Signal Voltage Gain, A                                     | $R_L > 2$ k $\Omega$ , $V^+ = 15$ V<br>(For large $V_O$ swing) | 83          | -    | -         | dB                           |
| Output Voltage Swing:<br>High-Level, $V_{OH}$                    | $R_L = 2$ k $\Omega$ , $V^+ = 26$ V                            | 22          | -    | -         | V                            |
|  | $R_L = 10$ k $\Omega$  | 23          | 28   | -         |                              |
| Low-Level, $V_{OL}$  | $R_L = 10$ k $\Omega$  | -           | 5    | 100       | mV                           |
| Output Current:<br>Source, $I_O$                                 | $V_1^+ = 1$ $V_{DC}$ , $V_1^- = 0$ ,<br>$V^+ = 15$ V           | 10          | 20   | -         | mA                           |
| Sink, $I_O$  | $V_1^- = 1$ $V_{DC}$ , $V_1^+ = 0$ ,<br>$V^+ = 15$ V           | 5           | 8    | -         | mA                           |
| Differential Input Voltage                                       | Note 2   | -           | -    | $V^+$     | V                            |

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because the current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltage and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is  $V^+ - 1.5$  V, but either or both inputs can go to +32 V without damage.

NOTE 3:  $V_O = 1.4$   $V_{DC}$ ,  $R_S = 0$   $\Omega$  with  $V^+$  from 5 V to 30 V; and over the full input common-mode voltage range (0 V to  $V^+ - 1.5$  V).

# CA124, CA224, CA324, CA2902, LM324, LM2902

## TYPICAL CHARACTERISTICS CURVES

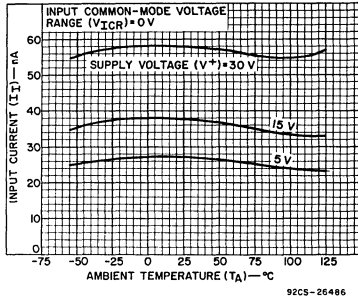


Fig. 3—Input current vs. ambient temperature.

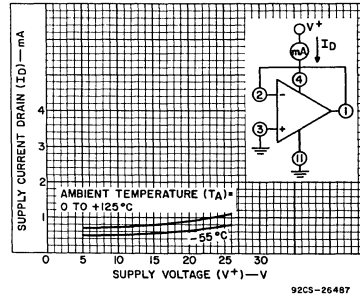


Fig. 4—Supply current drain vs. supply voltage.

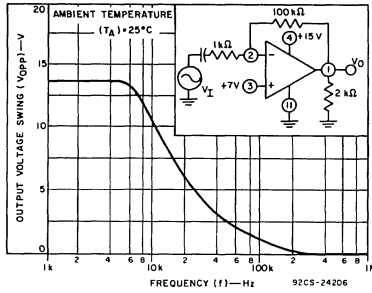


Fig. 5—Large-signal frequency response.

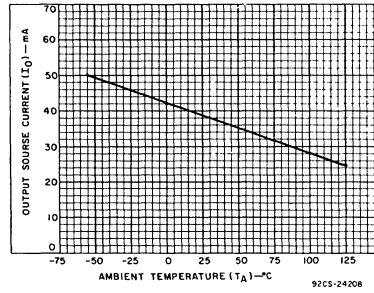


Fig. 6—Output current vs. ambient temperature.

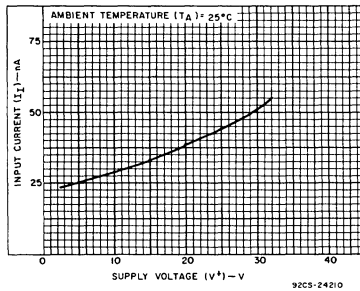


Fig. 7—Input current vs. supply voltage.

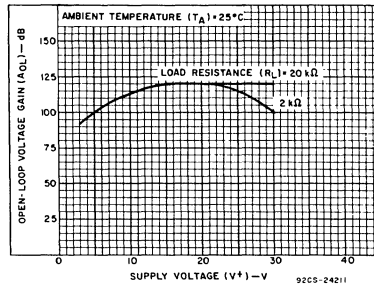


Fig. 8—Voltage gain vs. supply voltage.

TYPICAL CHARACTERISTICS CURVES (CONT'D)

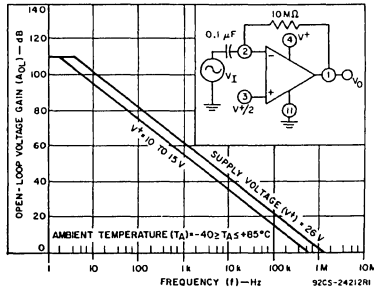


Fig. 9—Open-loop frequency response.

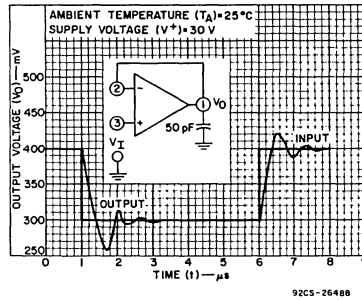


Fig. 10—Voltage follower pulse response (small signal).

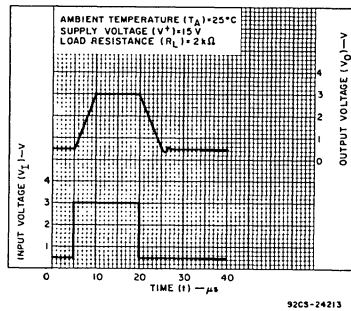


Fig. 11—Voltage follower pulse response.

# CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904, LM358\*, LM2904\*

## Dual Operational Amplifiers

### For Commercial, Industrial, and Military Applications

August 1991

#### Features

- Internal Frequency Compensation for Unity Gain
- High DC Voltage Gain ..... 100dB (Typ.)
- Wide Bandwidth at Unity Gain ..... 1MHz (Typ.)
- Wide Power Supply Range:
  - ▶ Single Supply ..... 3 to 30V
  - ▶ Dual Supplies .....  $\pm 1.5$  to  $\pm 15$ V
- Low Supply Current ..... 1.5 mA (Typ.)
- Low Input Bias Current
- Low Input Offset Voltage and Current
- Input Common-Mode Voltage Range Includes Ground
- Differential Input Voltage Range. Equal to  $V+$  Range
- Large Output Voltage Swing ..... 0 to  $V+ - 1.5$ V

#### Description

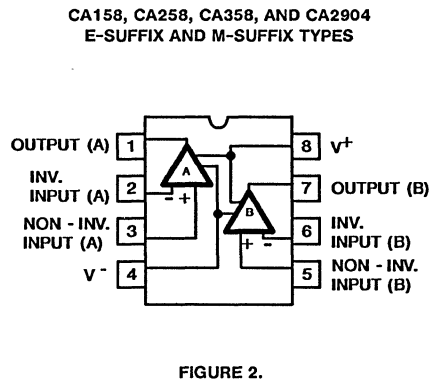
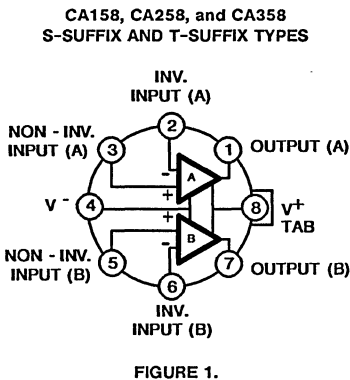
The CA158, CA158A, CA258, CA258A, CA358, CA358A and CA2904 types consist of two independent, high gain, internally frequency compensated operational amplifiers which are designed specifically to operate from a single power supply over a wide range of voltages. They may also be operated from split power supplies. The supply current is basically independent of the supply voltage over the recommended voltage range.

These devices are particularly useful in interface circuits with digital systems and can be operated from the single common 5 Vdc power supply. They are also intended for transducer amplifiers, dc gain blocks and many other conventional op amp circuits which can benefit from the single power supply capability.

The CA158, CA158A, CA258, CA258A, CA358, CA358A, and CA2904 types are supplied in 8-lead Small Outline packages (M suffix), 8-lead dual-in-line plastic packages (MINI-DIP, E suffix), 8-lead TO-5 style packages with standard leads (T suffix), and with dual-in-line formed leads (DIL-CAN, S suffix). The CA358 is also supplied in chip form (H suffix).

The CA158, CA158A, CA258, CA258A, CA358, CA358A, and CA2904 types are an equivalent to or a replacement for the industry types 158, 158A, 258, 258A, 358, 358A, and CA2904.

#### Pinouts



\* Technical Data on LM Branded types is identical to the corresponding CA Branded types.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.  
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# CA158, CA158A, CA258, CA258A, CA358 CA358A, CA2904, LM358, LM2904

## MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^\circ\text{C}$

|  |  |
|--|--|
| SUPPLY VOLTAGE, $V^+$ :                                |  |
| CA2904 . . . . .                                       | 26 V or $\pm 13$ V                           |
| Other Types . . . . .                                  | 32 V or $\pm 16$ V                           |
| DIFFERENTIAL INPUT VOLTAGE:                            |  |
| All Types . . . . .                                    | $\pm 32$ V                                   |
| INPUT VOLTAGE . . . . .                                | $-0.3$ V to $V^+$ V                          |
| INPUT CURRENT ( $V_I < -0.3$ V) <sup>†</sup> . . . . . | 50 mA  |
| OUTPUT SHORT CIRCUIT TO GROUND                         |  |
| ( $V^+ \leq 15$ V)* . . . . .                          | Continuous                                   |
| DEVICE DISSIPATION:                                    |  |
| Up to $T_A = 55^\circ\text{C}$ . . . . .               | 630 mW                                       |
| Above $T_A = 55^\circ\text{C}$ . . . . .               | derate linearly at 6.67 mW/ $^\circ\text{C}$ |
| AMBIENT TEMPERATURE RANGE:                             |  |
| Operating . . . . .                                    | $-55$ to $+125^\circ\text{C}$                |
| Storage . . . . .                                      | $-65$ to $+150^\circ\text{C}$                |
| LEAD TEMPERATURE (During Soldering):                   |  |
| At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm)  |  |
| from case for 10 seconds max. . . . .                  | $+300^\circ\text{C}$                         |

<sup>†</sup> This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector-base junction of the input p-n-p transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral n-p-n parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the  $V^+$  voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than  $-0.3$  V dc.

\* The maximum output current is approximately 40 mA independent of the magnitude of  $V^+$ . Continuous short circuits at  $V^+ > 15$  V can cause excessive power dissipation and eventual destruction. Short circuits from the output to  $V^+$  can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

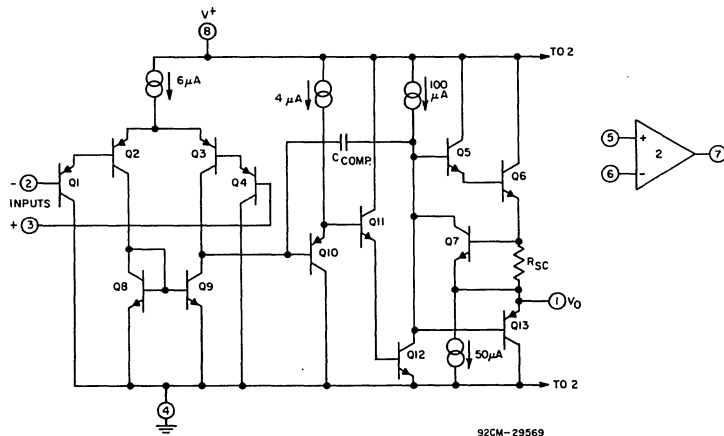


Fig.3 - Schematic diagram - one of two operational amplifiers.

**CA158, CA158A, CA258, CA258A, CA358  
CA358A, CA2904, LM358, LM2904**

**ELECTRICAL CHARACTERISTICS (Values Apply For Each Operational Amplifier)**

| CHARACTERISTIC  | TEST CONDITIONS  | LIMITS<br>CA158A (E, T, S)   |      |                      | UNITS |
|---|--|--|------|----------------------|-------|
|   |  | Supply Voltage (V <sup>+</sup> ) = 5 V<br>Unless Otherwise Specified | Min. | Typ.                 |       |
| <b>T<sub>A</sub> = 25°C</b>                                       |  |  |      |                      |       |
| Input Offset Voltage, V <sub>IO</sub>                             | Note 3   | –  | 1    | 2                    | mV    |
| Output Voltage Swing, V <sub>OPP</sub>                            | R <sub>L</sub> = 2 kΩ  | 0  | –    | V <sup>+</sup> – 1.5 | V     |
| Input Common-Mode Voltage Range, V <sub>ICR</sub>                 | Note 2, V <sup>+</sup> = 30 V  | 0  | –    | V <sup>+</sup> – 1.5 | V     |
| Input Offset Current, I <sub>IO</sub>                             | I <sub>1</sub> <sup>+</sup> – I <sub>1</sub> <sup>–</sup>  | –  | 2    | 10                   | nA    |
| Input Bias Current, I <sub>IB</sub>                               | I <sub>1</sub> <sup>+</sup> or I <sub>1</sub> <sup>–</sup> , Note 1                              | –  | 20   | 50                   | nA    |
| Output Current (Source), I <sub>O</sub>                           | V <sub>1</sub> <sup>+</sup> = +1 V, V <sub>1</sub> <sup>–</sup> = 0 V,<br>V <sup>+</sup> = 15 V  | 20   | 40   | –                    | mA    |
| Output Current (Sink), I <sub>O</sub>                             | V <sub>1</sub> <sup>+</sup> = 0 V, V <sub>1</sub> <sup>–</sup> = 1 V, V <sup>+</sup> = 15 V      | 10   | 20   | –                    | mA    |
|   | V <sub>1</sub> <sup>+</sup> = 0 V, V <sub>1</sub> <sup>–</sup> = 1 V,<br>V <sub>O</sub> = 200 mV | 12   | 50   | –                    | μA    |
| Short Circuit Output Current                                      | R <sub>L</sub> = 0 (to Ground) Note 4  | –  | 40   | 60                   | mA    |
| Large Signal Voltage Gain, A <sub>OL</sub>                        | R <sub>L</sub> ≥ 2 kΩ, V <sup>+</sup> = 15 V<br>(For large V <sub>O</sub> swing)                 | 50   | 100  | –                    | V/mV  |
| Common-Mode Rejection Ratio, CMRR                                 | DC   | 70   | 85   | –                    | dB    |
| Power Supply Rejection Ratio, PSRR                                | DC   | 65   | 100  | –                    | dB    |
| Amplifier-to-Amplifier Coupling                                   | f = 1 to 20 kHz (Input referred)   | –  | –120 | –                    | dB    |
| <b>T<sub>A</sub> = –55 to +125°C</b>                              |  |  |      |                      |       |
| Input Offset Voltage, V <sub>IO</sub>                             | Note 3   | –  | –    | 4                    | mV    |
| Temperature Coefficient of Input Offset Voltage, αV <sub>IO</sub> | R <sub>S</sub> = 0   | –  | 7    | 15                   | μV/°C |
| Input Offset Current, I <sub>IO</sub>                             | I <sub>1</sub> <sup>+</sup> – I <sub>1</sub> <sup>–</sup>  | –  | –    | 30                   | nA    |
| Temperature Coefficient of Input Offset Current, αI <sub>IO</sub> |  | –  | 10   | 200                  | pA/°C |
| Input Bias Current, I <sub>IB</sub>                               | I <sub>1</sub> <sup>+</sup> or I <sub>1</sub> <sup>–</sup>                                       | –  | 40   | 100                  | nA    |
| Input Common-Mode Voltage Range, V <sub>ICR</sub>                 | V <sup>+</sup> = 30 V, Note 2  | 0  | –    | V <sup>+</sup> – 2   | V     |
| Supply Current, I <sup>+</sup>                                    | R <sub>L</sub> = ∞ On All Ampl.  | –  | 0.7  | 1.2                  | mA    |
|   | R <sub>L</sub> = ∞, V <sup>+</sup> = 30 V  | –  | 1.5  | 3                    |       |

**NOTE 1:** Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

**NOTE 2:** The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V<sup>+</sup> – 1.5 V, but either or both inputs can go the + 32 V without damage.

**NOTE 3:** V<sub>O</sub> = 1.4 V<sub>DC</sub>, R<sub>S</sub> = 0 Ω with V<sup>+</sup> from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V<sup>+</sup> – 1.5 V).

**NOTE 4:** The maximum output current is approximately 40 mA independent of the magnitude of V<sup>+</sup>. Continuous short circuits at V<sup>+</sup> > 15 V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V<sup>+</sup> can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

**CA158, CA158A, CA258, CA258A, CA358  
CA358A, CA2904, LM358, LM2904**

**ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)**

| CHARACTERISTIC  | TEST CONDITIONS  | LIMITS<br>CA258A (E, T, S)   |      |                      | UNITS |
|---|--|--|------|----------------------|-------|
|   |  | Supply Voltage (V <sup>+</sup> ) = 5 V<br>Unless Otherwise Specified | Min. | Typ.                 |       |
| <b>T<sub>A</sub> = 25°C</b>                                       |  |  |      |                      |       |
| Input Offset Voltage, V <sub>IO</sub>                             | Note 3   | –  | 1    | 3                    | mV    |
| Output Voltage Swing, V <sub>OPP</sub>                            | R <sub>L</sub> = 2 kΩ  | 0  | –    | V <sup>+</sup> – 1.5 | V     |
| Input Common-Mode Voltage Range, V <sub>ICR</sub>                 | Note 2, V <sup>+</sup> = 30 V  | 0  | –    | V <sup>+</sup> – 1.5 | V     |
| Input Offset Current, I <sub>IO</sub>                             | I <sub>1</sub> <sup>+</sup> – I <sub>1</sub> <sup>–</sup>  | –  | 2    | 15                   | nA    |
| Input Bias Current, I <sub>IB</sub>                               | I <sub>1</sub> <sup>+</sup> or I <sub>1</sub> <sup>–</sup> , Note 1                              | –  | 40   | 80                   | nA    |
| Output Current (Source), I <sub>O</sub>                           | V <sub>1</sub> <sup>+</sup> = +1 V, V <sub>1</sub> <sup>–</sup> = 0 V,<br>V <sup>+</sup> = 15 V  | 20   | 40   | –                    | mA    |
| Output Current (Sink), I <sub>O</sub>                             | V <sub>1</sub> <sup>+</sup> = 0 V, V <sub>1</sub> <sup>–</sup> = 1 V, V <sup>+</sup> = 15 V      | 10   | 20   | –                    | mA    |
|   | V <sub>1</sub> <sup>+</sup> = 0 V, V <sub>1</sub> <sup>–</sup> = 1 V,<br>V <sub>O</sub> = 200 mV | 12   | 50   | –                    | μA    |
| Short Circuit Output Current                                      | R <sub>L</sub> = 0 (to Ground) Note 4  | –  | 40   | 60                   | mA    |
| Large Signal Voltage Gain, A <sub>OL</sub>                        | R <sub>L</sub> ≥ 2 kΩ, V <sup>+</sup> = 15 V<br>(For large V <sub>O</sub> swing)                 | 50   | 100  | –                    | V/mV  |
| Common-Mode Rejection Ratio, CMRR                                 | DC   | 70   | 85   | –                    | dB    |
| Power Supply Rejection Ratio, PSRR                                | DC   | 65   | 100  | –                    | dB    |
| Amplifier-to-Amplifier Coupling                                   | f = 1 to 20 kHz (Input referred)   | –  | –120 | –                    | dB    |
| <b>T<sub>A</sub> = –25 to +85°C</b>                               |  |  |      |                      |       |
| Input Offset Voltage, V <sub>IO</sub>                             | Note 3   | –  | –    | 4                    | mV    |
| Temperature Coefficient of Input Offset Voltage, αV <sub>IO</sub> | R <sub>S</sub> = 0   | –  | 7    | 15                   | μV/°C |
| Input Offset Current, I <sub>IO</sub>                             | I <sub>1</sub> <sup>+</sup> – I <sub>1</sub> <sup>–</sup>  | –  | –    | 30                   | nA    |
| Temperature Coefficient of Input Offset Current, αI <sub>IO</sub> |  | –  | 10   | 200                  | pA/°C |
| Input Bias Current, I <sub>IB</sub>                               | I <sub>1</sub> <sup>+</sup> or I <sub>1</sub> <sup>–</sup>                                       | –  | 40   | 100                  | nA    |
| Input Common-Mode Voltage Range, V <sub>ICR</sub>                 | V <sup>+</sup> = 30 V, Note 2  | 0  | –    | V <sup>+</sup> – 2   | V     |
| Supply Current, I <sup>+</sup>                                    | R <sub>L</sub> = ∞ On All Ampl.  | –  | 0.7  | 1.2                  | mA    |
|   | R <sub>L</sub> = ∞, V <sup>+</sup> = 30 V  | –  | 1.5  | 3                    |       |

**NOTE 1:** Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

**NOTE 2:** The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V<sup>+</sup> – 1.5 V, but either or both inputs can go the + 32 V without damage.

**NOTE 3:** V<sub>O</sub> = 1.4 V<sub>DC</sub>, R<sub>S</sub> = 0 Ω with V<sup>+</sup> from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V<sup>+</sup> – 1.5 V).

**NOTE 4:** The maximum output current is approximately 40 mA independent of the magnitude of V<sup>+</sup>. Continuous short circuits at V<sup>+</sup> > 15 V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V<sup>+</sup> can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.



**CA158, CA158A, CA258, CA258A, CA358  
CA358A, CA2904, LM358, LM2904**

**ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)**

| CHARACTERISTIC  | TEST CONDITIONS  | LIMITS<br>CA358A (E. T. S)   |      |                      | UNITS |
|---|--|--|------|----------------------|-------|
|   |  | Supply Voltage (V <sup>+</sup> ) = 5 V<br>Unless Otherwise Specified | Min. | Typ.                 |       |
| <b>T<sub>A</sub> = 25°C</b>                                       |  |  |      |                      |       |
| Input Offset Voltage, V <sub>IO</sub>                             | Note 3   | –  | 2    | 3                    | mV    |
| Output Voltage Swing, V <sub>O</sub> PP                           | R <sub>L</sub> = 2 kΩ  | 0  | –    | V <sup>+</sup> – 1.5 | V     |
| Input Common-Mode Voltage Range, V <sub>ICR</sub>                 | Note 2, V <sup>+</sup> = 30 V  | 0  | –    | V <sup>+</sup> – 1.5 | V     |
| Input Offset Current, I <sub>IO</sub>                             | I <sub>1</sub> <sup>+</sup> – I <sub>1</sub> <sup>–</sup>  | –  | 5    | 30                   | nA    |
| Input Bias Current, I <sub>IB</sub>                               | I <sub>1</sub> <sup>+</sup> or I <sub>1</sub> <sup>–</sup> , Note 1                              | –  | 45   | 100                  | nA    |
| Output Current (Source), I <sub>O</sub>                           | V <sub>1</sub> <sup>+</sup> = +1 V, V <sub>1</sub> <sup>–</sup> = 0 V,<br>V <sup>+</sup> = 15 V  | 20   | 40   | –                    | mA    |
| Output Current (Sink), I <sub>O</sub>                             | V <sub>1</sub> <sup>+</sup> = 0 V, V <sub>1</sub> <sup>–</sup> = 1 V, V <sup>+</sup> = 15 V      | 10   | 20   | –                    | mA    |
|   | V <sub>1</sub> <sup>+</sup> = 0 V, V <sub>1</sub> <sup>–</sup> = 1 V,<br>V <sub>O</sub> = 200 mV | 12   | 50   | –                    | μA    |
| Short Circuit Output Current                                      | R <sub>L</sub> = 0 (to Ground) Note 4  | –  | 40   | 60                   | mA    |
| Large Signal Voltage Gain, A <sub>OL</sub>                        | R <sub>L</sub> ≥ 2 kΩ, V <sup>+</sup> = 15 V<br>(For large V <sub>O</sub> swing)                 | 25   | 100  | –                    | V/mV  |
| Common-Mode Rejection Ratio, CMRR                                 | DC   | 65   | 85   | –                    | dB    |
| Power Supply Rejection Ratio, PSRR                                | DC   | 65   | 100  | –                    | dB    |
| Amplifier-to-Amplifier Coupling                                   | f = 1 to 20 kHz (Input referred)   | –  | –120 | –                    | dB    |
| <b>T<sub>A</sub> = 0 to +70°C</b>                                 |  |  |      |                      |       |
| Input Offset Voltage, V <sub>IO</sub>                             | Note 3   | –  | –    | 5                    | mV    |
| Temperature Coefficient of Input Offset Voltage, αV <sub>IO</sub> | R <sub>S</sub> = 0   | –  | 7    | 20                   | μV/°C |
| Input Offset Current, I <sub>IO</sub>                             | I <sub>1</sub> <sup>+</sup> – I <sub>1</sub> <sup>–</sup>  | –  | –    | 75                   | nA    |
| Temperature Coefficient of Input Offset Current, αI <sub>IO</sub> |  | –  | 10   | 300                  | pA/°C |
| Input Bias Current, I <sub>IB</sub>                               | I <sub>1</sub> <sup>+</sup> or I <sub>1</sub> <sup>–</sup>                                       | –  | 40   | 200                  | nA    |
| Input Common-Mode Voltage Range, V <sub>ICR</sub>                 | V <sup>+</sup> = 30 V, Note 2  | 0  | –    | V <sup>+</sup> – 2   | V     |
| Supply Current, I <sup>+</sup>                                    | R <sub>L</sub> = ∞ On All Ampl.  | –  | 0.7  | 1.2                  | mA    |
|   | R <sub>L</sub> = ∞, V <sup>+</sup> = 30 V  | –  | 1.5  | 3                    |       |

**NOTE 1:** Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

**NOTE 2:** The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V<sup>+</sup> – 1.5 V, but either or both inputs can go the + 32 V without damage.

**NOTE 3:** V<sub>O</sub> = 1.4 V<sub>DC</sub>, R<sub>S</sub> = 0 Ω with V<sup>+</sup> from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V<sup>+</sup> – 1.5 V).

**NOTE 4:** The maximum output current is approximately 40 mA independent of the magnitude of V<sup>+</sup>. Continuous short circuits at V<sup>+</sup> > 15 V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V<sup>+</sup> can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

**CA158, CA158A, CA258, CA258A, CA358  
CA358A, CA2904, LM358, LM2904**

**ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)**

| CHARACTERISTIC   | TEST CONDITIONS  | LIMITS<br>CA158 (E, T, S)<br>CA258 (E, T, S) |      |             | UNITS                        |
|--|--|--|------|-------------|------------------------------|
|  |  | Min.   | Typ. | Max.        |                              |
|  | Supply Voltage ( $V^+$ ) = 5 V<br>Unless Otherwise Specified                 |  |      |             |                              |
| <b><math>T_A = 25^\circ\text{C}</math></b>   |  |  |      |             |                              |
| Input Offset Voltage, $V_{IO}$   | Note 3   | –  | 2    | 5           | mV                           |
| Output Voltage Swing, $V_{OPP}$  | $R_L = 2\text{ k}\Omega$   | 0  | –    | $V^+ - 1.5$ | V                            |
| Input Common-Mode Voltage Range, $V_{ICR}$   | Note 2, $V^+ = 30\text{ V}$  | 0  | –    | $V^+ - 1.5$ | V                            |
| Input Offset Current, $I_{IO}$   | $I_1^+ - I_1^-$  | –  | 3    | 30          | nA                           |
| Input Bias Current, $I_{IB}$   | $I_1^+$ or $I_1^-$ , Note 1  | –  | 45   | 150         | nA                           |
| Output Current (Source), $I_O$   | $V_1^+ = +1\text{ V}$ , $V_1^- = 0\text{ V}$ ,<br>$V_O = 15\text{ V}$        | 20   | 40   | –           | mA                           |
| Output Current (Sink), $I_O$   | $V_1^+ = 0\text{ V}$ , $V_1^- = 1\text{ V}$ , $V^+ = 15\text{ V}$            | 10   | 20   | –           | mA                           |
|  | $V_1^+ = 0\text{ V}$ , $V_1^- = 1\text{ V}$ ,<br>$V_O = 200\text{ mV}$       | 12   | 50   | –           | $\mu\text{A}$                |
| Short Circuit Output Current   | $R_L = 0$ (to Ground) Note 4   | –  | 40   | 60          | mA                           |
| Large Signal Voltage Gain, $A_{OL}$  | $R_L \geq 2\text{ k}\Omega$ , $V^+ = 15\text{ V}$<br>(For large $V_O$ swing) | 50   | 100  | –           | V/mV                         |
| Common-Mode Rejection Ratio, CMRR  | DC   | 70   | 85   | –           | dB                           |
| Power Supply Rejection Ratio, PSRR   | DC   | 65   | 100  | –           | dB                           |
| Amplifier-to-Amplifier Coupling  | $f = 1$ to $20\text{ kHz}$ (Input referred)                                  | –  | –120 | –           | dB                           |
| <b><math>T_A = -55</math> to <math>+125^\circ\text{C}</math> (CA158); <math>T_A = -25</math> to <math>+85^\circ\text{C}</math> (CA258)</b> |  |  |      |             |                              |
| Input Offset Voltage, $V_{IO}$   | Note 3   | –  | –    | 7           | mV                           |
| Temperature Coefficient of Input Offset Voltage, $\alpha V_{IO}$   | $R_S = 0$  | –  | 7    | –           | $\mu\text{V}/^\circ\text{C}$ |
| Input Offset Current, $I_{IO}$   | $I_1^+ - I_1^-$  | –  | –    | 100         | nA                           |
| Temperature Coefficient of Input Offset Current, $\alpha I_{IO}$   |  | –  | 10   | –           | $\text{pA}/^\circ\text{C}$   |
| Input Bias Current, $I_{IB}$   | $I_1^+$ or $I_1^-$   | –  | 40   | 300         | nA                           |
| Input Common-Mode Voltage Range, $V_{ICR}$   | $V^+ = 30\text{ V}$ , Note 2   | 0  | –    | $V^+ - 2$   | V                            |
| Supply Current, $I^+$  | $R_L = \infty$ On All Ampl.  | –  | 0.7  | 1.2         | mA                           |
|  | $R_L = \infty$ , $V^+ = 30\text{ V}$   | –  | 1.5  | 3           |                              |

**NOTE 1:** Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

**NOTE 2:** The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is  $V^+ - 1.5\text{ V}$ , but either or both inputs can go the  $+32\text{ V}$  without damage.

**NOTE 3:**  $V_O = 1.4$ ,  $V_{DC}$ ,  $R_S = 0\ \Omega$  with  $V^+$  from 5 V to 30 V, and over the full input common-mode voltage range (0 V to  $V^+ - 1.5\text{ V}$ ).

**NOTE 4:** The maximum output current is approximately 40 mA independent of the magnitude of  $V^+$ . Continuous short circuits at  $V^+ > 15\text{ V}$  can cause excessive power dissipation and eventual destruction. Short circuits from the output to  $V^+$  can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

**CA158, CA158A, CA258, CA258A, CA358  
CA358A, CA2904, LM358, LM2904**

**ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)**

| CHARACTERISTIC  | TEST CONDITIONS  | LIMITS<br>CA358 (E, T, S)  |      |                      | UNITS |
|---|--|--|------|----------------------|-------|
|   |  | Supply Voltage (V <sup>+</sup> ) = 5 V<br>Unless Otherwise Specified | Min. | Typ.                 |       |
| <b>T<sub>A</sub> = 25°C</b>                                       |  |  |      |                      |       |
| Input Offset Voltage, V <sub>IO</sub>                             | Note 3   | –  | 2    | 7                    | mV    |
| Output Voltage Swing, V <sub>OPP</sub>                            | R <sub>L</sub> = 2 kΩ  | 0  | –    | V <sup>+</sup> – 1.5 | V     |
| Input Common-Mode Voltage Range, V <sub>ICR</sub>                 | Note 2, V <sup>+</sup> = 30 V  | 0  | –    | V <sup>+</sup> – 1.5 | V     |
| Input Offset Current, I <sub>IO</sub>                             | I <sub>1</sub> <sup>+</sup> – I <sub>1</sub> <sup>–</sup>  | –  | 5    | 50                   | nA    |
| Input Bias Current, I <sub>IB</sub>                               | I <sub>1</sub> <sup>+</sup> or I <sub>1</sub> <sup>–</sup> , Note 1                              | –  | 45   | 250                  | nA    |
| Output Current (Source), I <sub>O</sub>                           | V <sub>1</sub> <sup>+</sup> = +1 V, V <sub>1</sub> <sup>–</sup> = 0 V,<br>V <sup>+</sup> = 15 V  | 20   | 40   | –                    | mA    |
| Output Current (Sink), I <sub>O</sub>                             | V <sub>1</sub> <sup>+</sup> = 0 V, V <sub>1</sub> <sup>–</sup> = 1 V, V <sup>+</sup> = 15 V      | 10   | 20   | –                    | mA    |
|   | V <sub>1</sub> <sup>+</sup> = 0 V, V <sub>1</sub> <sup>–</sup> = 1 V,<br>V <sub>O</sub> = 200 mV | 12   | 50   | –                    | μA    |
| Short Circuit Output Current                                      | R <sub>L</sub> = 0 (to Ground) Note 4  | –  | 40   | 60                   | mA    |
| Large Signal Voltage Gain, A <sub>OL</sub>                        | R <sub>L</sub> ≥ 2 kΩ, V <sup>+</sup> = 15 V<br>(For large V <sub>O</sub> swing)                 | 25   | 100  | –                    | V/mV  |
| Common-Mode Rejection Ratio, CMRR                                 | DC   | 65   | 70   | –                    | dB    |
| Power Supply Rejection Ratio, PSRR                                | DC   | 65   | 100  | –                    | dB    |
| Amplifier-to-Amplifier Coupling                                   | f = 1 to 20 kHz (Input referred)   | –  | –120 | –                    | dB    |
| <b>T<sub>A</sub> = 0 to +70°C</b>                                 |  |  |      |                      |       |
| Input Offset Voltage, V <sub>IO</sub>                             | Note 3   | –  | –    | 9                    | mV    |
| Temperature Coefficient of Input Offset Voltage, αV <sub>IO</sub> | R <sub>S</sub> = 0   | –  | 7    | –                    | μV/°C |
| Input Offset Current, I <sub>IO</sub>                             | I <sub>1</sub> <sup>+</sup> – I <sub>1</sub> <sup>–</sup>  | –  | –    | 150                  | nA    |
| Temperature Coefficient of Input Offset Current, αI <sub>IO</sub> |  | –  | 10   | –                    | pA/°C |
| Input Bias Current, I <sub>IB</sub>                               | I <sub>1</sub> <sup>+</sup> or I <sub>1</sub> <sup>–</sup>                                       | –  | 40   | 500                  | nA    |
| Input Common-Mode Voltage Range, V <sub>ICR</sub>                 | V <sup>+</sup> = 30 V, Note 2  | 0  | –    | V <sup>+</sup> – 2   | V     |
| Supply Current, I <sup>+</sup>                                    | R <sub>L</sub> = ∞ On All Ampl.  | –  | 0.7  | 1.2                  | mA    |
|   | R <sub>L</sub> = ∞, V <sup>+</sup> = 30 V  | –  | 1.5  | 3                    |       |

**NOTE 1:** Due to the p–n–p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

**NOTE 2:** The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V<sup>+</sup> – 1.5 V, but either or both inputs can go the +32 V without damage.

**NOTE 3:** V<sub>O</sub> = 1.4, V<sub>DC</sub>, R<sub>S</sub> = 0 Ω with V<sup>+</sup> from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V<sup>+</sup> – 1.5 V).

**NOTE 4:** The maximum output current is approximately 40 mA independent of the magnitude of V<sup>+</sup>. Continuous short circuits at V<sup>+</sup> > 15 V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V<sup>+</sup> can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

**CA158, CA158A, CA258, CA258A, CA358  
CA358A, CA2904, LM358, LM2904**

**ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)**

| CHARACTERISTIC  | TEST CONDITIONS   | LIMITS<br>CA2904E  |      |                      | UNITS |
|---|---|--|------|----------------------|-------|
|   |   | Supply Voltage (V <sup>+</sup> ) = 5 V<br>Unless Otherwise Specified | Min. | Typ.                 |       |
| <b>T<sub>A</sub> = 25°C</b>                                       |   |  |      |                      |       |
| Input Offset Voltage, V <sub>IO</sub>                             | Note 3  | –  | 2    | 7                    | mV    |
| Output Voltage Swing, V <sub>OPP</sub>                            | R <sub>L</sub> = 10 kΩ  | 0  | –    | V <sup>+</sup> – 1.5 | V     |
| Input Common-Mode Voltage Range, V <sub>ICR</sub>                 | Note 2, V <sup>+</sup> = 30 V   | 0  | –    | V <sup>+</sup> – 1.5 | V     |
| Input Offset Current, I <sub>IO</sub>                             | I <sub>I</sub> <sup>+</sup> – I <sub>I</sub> <sup>–</sup>                                       | –  | 5    | 50                   | nA    |
| Input Bias Current, I <sub>IB</sub>                               | I <sub>I</sub> <sup>+</sup> or I <sub>I</sub> <sup>–</sup> , Note 1                             | –  | 45   | 250                  | nA    |
| Output Current (Source), I <sub>O</sub>                           | V <sub>I</sub> <sup>+</sup> = +1 V, V <sub>I</sub> <sup>–</sup> = 0 V,<br>V <sup>+</sup> = 15 V | 20   | 40   | –                    | mA    |
| Output Current (Sink), I <sub>O</sub>                             | V <sub>I</sub> <sup>+</sup> = 0 V, V <sub>I</sub> <sup>–</sup> = 1 V, V <sup>+</sup> = 15 V     | 10   | 20   | –                    | mA    |
| Short Circuit Output Current                                      | R <sub>L</sub> = 0 (to Ground) Note 4   | –  | 40   | 60                   | mA    |
| Large Signal Voltage Gain, A <sub>OL</sub>                        | R <sub>L</sub> ≥ 2 kΩ, V <sup>+</sup> = 15 V<br>(For large V <sub>O</sub> swing)                | –  | 100  | –                    | V/mV  |
| Common-Mode Rejection Ratio, CMRR                                 | DC  | 50   | 70   | –                    | dB    |
| Power Supply Rejection Ratio, PSRR                                | DC  | 50   | 100  | –                    | dB    |
| Amplifier-to-Amplifier Coupling                                   | f = 1 to 20 kHz (Input referred)  | –  | –120 | –                    | dB    |
| <b>T<sub>A</sub> = –40 to +85°C</b>                               |   |  |      |                      |       |
| Input Offset Voltage, V <sub>IO</sub>                             | Note 3  | –  | –    | 10                   | mV    |
| Temperature Coefficient of Input Offset Voltage, αV <sub>IO</sub> | R <sub>S</sub> = 0  | –  | 7    | –                    | μV/°C |
| Input Offset Current, I <sub>IO</sub>                             | I <sub>I</sub> <sup>+</sup> – I <sub>I</sub> <sup>–</sup>                                       | –  | 45   | 200                  | nA    |
| Temperature Coefficient of Input Offset Current, αI <sub>IO</sub> |   | –  | 10   | –                    | pA/°C |
| Input Bias Current, I <sub>IB</sub>                               | I <sub>I</sub> <sup>+</sup> or I <sub>I</sub> <sup>–</sup>                                      | –  | 40   | 500                  | nA    |
| Input Common-Mode Voltage Range, V <sub>ICR</sub>                 | V <sup>+</sup> = 30 V, Note 2   | 0  | –    | V <sup>+</sup> – 2   | V     |
| Supply Current, I <sup>+</sup>                                    | R <sub>L</sub> = ∞ On All Ampl.   | –  | 0.7  | 1.2                  | mA    |
|   | R <sub>L</sub> = ∞, V <sup>+</sup> = 30 V   | –  | 1.5  | 3                    |       |

**NOTE 1:** Due to the p–n–p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

**NOTE 2:** The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V<sup>+</sup> – 1.5 V, but either or both inputs can go the +32 V without damage.

**NOTE 3:** V<sub>O</sub> = 1.4, V<sub>DC</sub>, R<sub>S</sub> = 0 Ω with V<sup>+</sup> from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V<sup>+</sup> – 1.5 V).

**NOTE 4:** The maximum output current is approximately 40 mA independent of the magnitude of V<sup>+</sup>. Continuous short circuits at V<sup>+</sup> > 15 V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V<sup>+</sup> can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

CA158, CA158A, CA258, CA258A, CA358  
CA358A, CA2904, LM358, LM2904

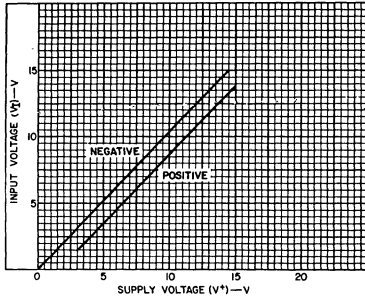


Fig. 4 - Input voltage range as a function of supply voltage.

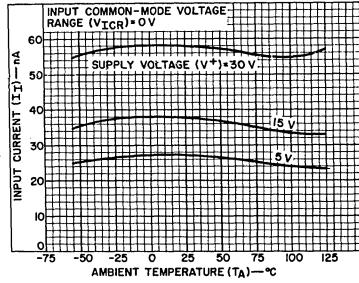


Fig. 5 - Input current as a function of ambient temperature.

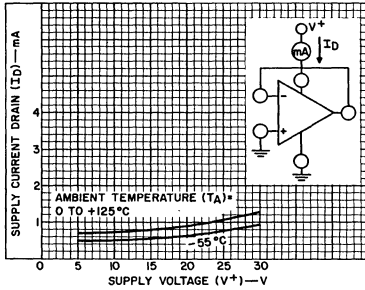


Fig. 6 - Supply current drain as a function of supply voltage.

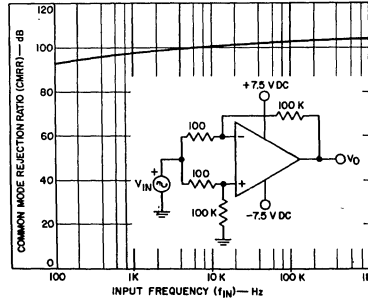


Fig. 7 - Common mode rejection ratio as a function of input frequency.

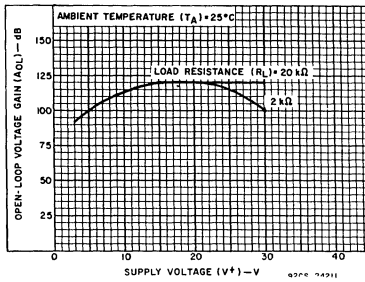


Fig. 8 - Voltage gain as a function of supply voltage.

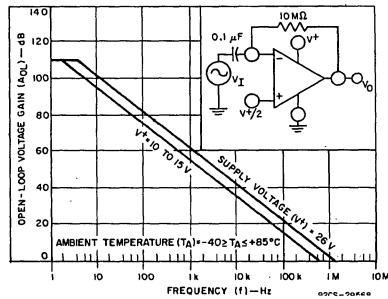


Fig. 9 - Open-loop frequency response.

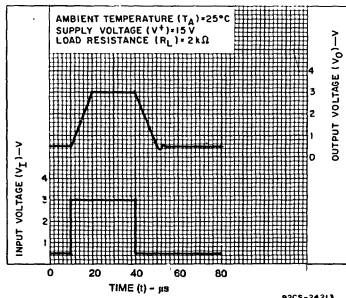


Fig. 10 - Voltage follower pulse response.

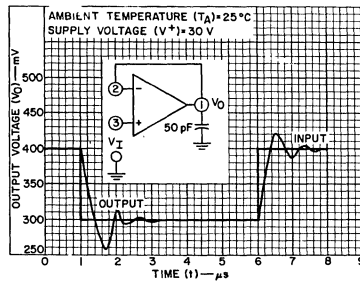
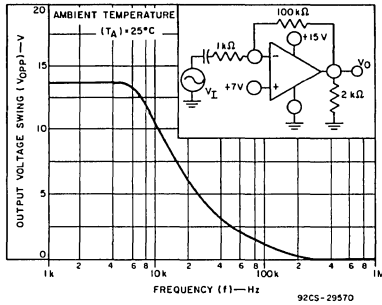
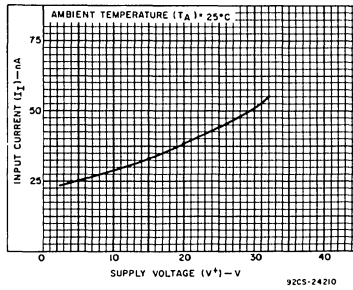


Fig. 11 - Voltage follower pulse response (small signal).

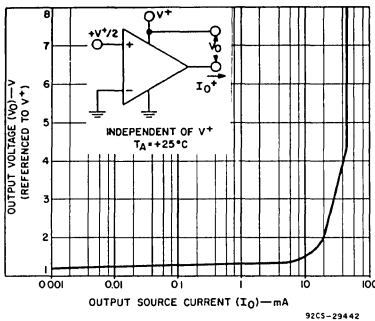
**CA158, CA158A, CA258, CA258A, CA358  
CA358A, CA2904, LM358, LM2904**



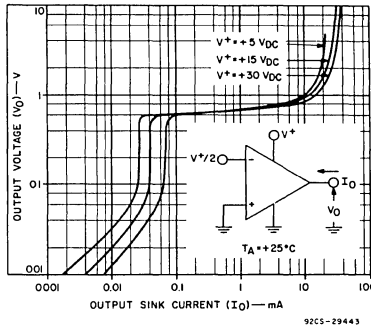
**Fig. 12 – Large-signal frequency response.**



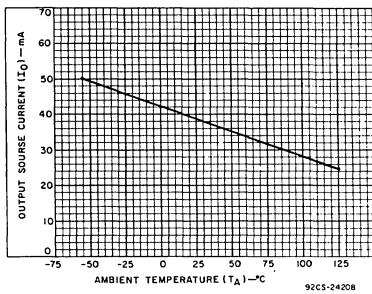
**Fig. 13 – Input current as a function of supply voltage.**



**Fig. 14 – Output source current characteristics.**



**Fig. 15 – Output sink current characteristics.**



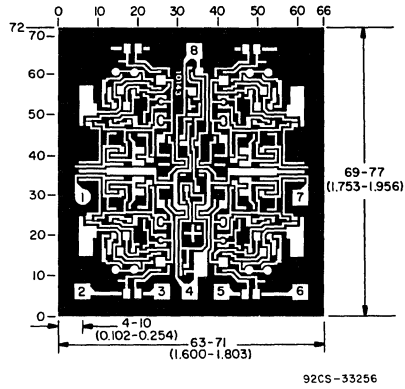
**Fig. 16 – Output current as a function of ambient temperature.**

**ORDERING INFORMATION**

These packages are identified by Suffix Letters indicated in the chart shown below. When ordering these devices, it is important that the appropriate suffix letter be affixed to the type number of the device required.

| PACKAGE  | SUFFIX LETTERS | TYPES                |
|--|----------------|----------------------|
| 8-Lead Dual-In-Line Plastic                        | E              | CA158, A<br>CA258, A |
| 8-Lead Small Outline                               | M              | CA358, A<br>CA2904   |
| 8-Lead TO-5 Style with Dual-In-Line Standard Leads | T              | CA158, A<br>CA258, A |
| 8-Lead TO-5 Style with Dual-In-Line Formed Leads   | S              | CA358, A             |

**CA158, CA158A, CA258, CA258A, CA358  
CA358A, CA2904, LM358, LM2904**



*Dimensions and pad layout for CA358H.*

*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).*

*The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are  $57^\circ$  instead of  $90^\circ$  with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.*



# CA741C, CA741, CA1458, CA1558, LM741\*, LM741C\*, LM1458\*, LM1558\*

## High-Gain Single and Dual Operational Amplifiers for Military, Industrial and Commercial Applications

August 1991

### Features

- Input Bias Current (All Types) ..... 500nA (Max.)
- Input Offset Current (All Types) ..... 200nA (Max.)

### Applications

- Comparator
- DC Amplifier
- Integrator or Differentiator
- Multivibrator
- Narrow-Band or Band-Pass Filter
- Summing Amplifier

### Description

The CA1458, CA1558 (dual types); CA741C, CA741 (single-types); high-gain operational amplifiers for use in military, industrial, and commercial applications.

These monolithic silicon integrated-circuit devices provide output short-circuit protection and latch-free operation. These types also feature wide common-mode and differential-mode signal ranges and have low-offset voltage nulling capability when used with an appropriately valued potentiometer. A 10-kilohm potentiometer is used for offset nulling types CA741C, CA741 (See Fig. 9); and types CA1458, CA1558, have no specific terminals for offset nulling. Each type consists of a differential-input amplifier that effectively drives a gain and level-shifting stage having a complementary emitter-follower output.

The manufacturing process make it possible to produce IC operational amplifiers with low-burst ("popcorn") noise characteristics. The CA741 gives limit specifications for burst noise in the data bulletin, File No. 530. Contact your Sales Representative for information pertinent to other operational amplifier types that meet low-burst noise specifications.

This operational amplifier line also offers the circuit designer the option of operation with internal or external phase compensation.

Unity gain with external phase compensation can be obtained with a single 30-pF capacitor. All the other types are internally phase-compensated.

| TYPE NO. | NO. OF AMPL. | PHASE COMP. | OFFSET VOLTAGE NULL | MINIMUM AOL | MAXIMUM VIO (mV) | OPERATING TEMPERATURE RANGE (°C) |
|----------|--------------|-------------|---------------------|-------------|------------------|----------------------------------|
| CA1458   | Dual         | Int.        | No                  | 20k         | 6                | 0 to 70 <sup>▲</sup>             |
| CA1558   | Dual         | Int.        | No                  | 50k         | 5                | -55 to 125                       |
| CA741C   | Single       | Int.        | Yes                 | 20k         | 6                | 0 to 70 <sup>▲</sup>             |
| CA741    | Single       | Int.        | Yes                 | 50k         | 5                | -55 to +125                      |

<sup>▲</sup> All types in any package style can be operated over the temperature range of -55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.

3  
OPERATIONAL AMPLIFIERS



## CA741C, CA741, CA1458, CA1558, LM741, LM741C, LM1458, LM1558

### Ordering Information

When ordering any of these types, it is important that the appropriate suffix letter for the package required be affixed to the type number. For example: If a CA1458 in a straight-lead TO-5 style package is desired, order CA1458T.

| TYPE NO. | PACKAGE TYPE AND SUFFIX LETTER |     |         |         |     |      |           | FIG. NO |
|----------|--------------------------------|-----|---------|---------|-----|------|-----------|---------|
|          | TO-5 STYLE                     |     |         | PLASTIC |     | CHIP | BEAM LEAD |         |
|          | 8L                             | 10L | DIL-CAN | 8L      | 14L |      |           |         |
| CA1458   | T                              | -   | S       | E       | -   | H    | -         | 1b, 1d  |
| CA1558   | T                              | -   | S       | E       | -   | -    | -         | 1b, 1d  |
| CA741C   | T                              | -   | S       | E       | -   | H    | -         | 1a, 1c  |
| CA741    | T                              | -   | S       | E       | -   | -    | L         | 1a, 1c  |

### Absolute Maximum Ratings $T_A = +25^\circ\text{C}$

DC Supply Voltage (Between V+ and V- Terminals):

CA741C, CA1458 (Note 2) ..... 36V

CA741, CA1558 (Note 2) ..... 44V

Differential Input Voltage .....  $\pm 30\text{V}$

DC Input Voltage (Note 1) .....  $\pm 15\text{V}$

Output Short-Circuit Duration ..... Indefinite

Device Dissipation:

Up to  $+70^\circ\text{C}$  (CA741C) ..... 500mW

Up to  $+75^\circ\text{C}$  (CA741) ..... 500mW

Up to  $+30^\circ\text{C}$  (CA1558) ..... 680mW

Up to  $+25^\circ\text{C}$  (CA1458) ..... 680mW

For Temperatures Exceeding Those Indicated Above ..... Derate Linearly 6.67mW/ $^\circ\text{C}$

Voltage Between Offset Null and V- (CA741C, CA741) .....  $\pm 0.5\text{V}$

Ambient Operating Temperature Range:

CA741, CA1558 .....  $-55$  to  $+125^\circ\text{C}$

CA741C, CA1458 ..... 0 to  $+70^\circ\text{C}$  (Note 3)

Ambient Storage Temperature Range .....  $-65$  to  $+150^\circ\text{C}$

Lead Temperature (During Soldering):

At Distance  $1/16 \pm 1/32$  Inch ( $1.59 \pm 0.79\text{mm}$ ) from Case for 10 Seconds Max .....  $+265^\circ\text{C}$

NOTES: 1. If Supply Voltage is Less than  $\pm 15$  Volts, the Absolute Maximum Input Voltage is Equal to the Supply Voltage.

2. Voltage Values Apply for Each of the Dual Operational Amplifiers.

3. All Types in any Package Style Can Be Operated Over the Temperature Range of  $-55$  to  $+125^\circ\text{C}$ , Although the Published Limits for Certain Electrical Specifications Apply Only Over the Temperature Range of 0 to  $+70^\circ\text{C}$

CA741C, CA741, CA1458, CA1558, LM741, LM741C, LM1458, LM1558

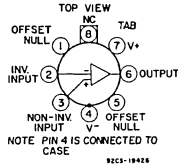


FIGURE 1a. CA741CS, CA741CT, CA741S, & CA741T WITH INTERNAL PHASE COMPENSATION.

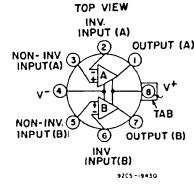


FIGURE 1b. CA1458S, CA1458T, CA1558S, & CA1558T AND INTERNAL PHASE COMPENSATION

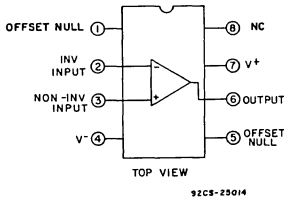


FIGURE 1c. CA741C AND CA741E WITH INTERNAL PHASE COMPENSATION

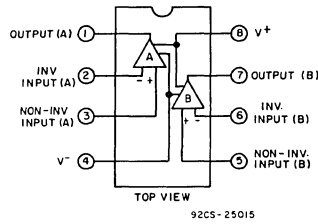


FIGURE 1d. CA1458E AND CA1558E WITH INTERNAL PHASE COMPENSATION

3  
OPERATIONAL AMPLIFIERS

FIGURE 1. FUNCTIONAL DIAGRAMS

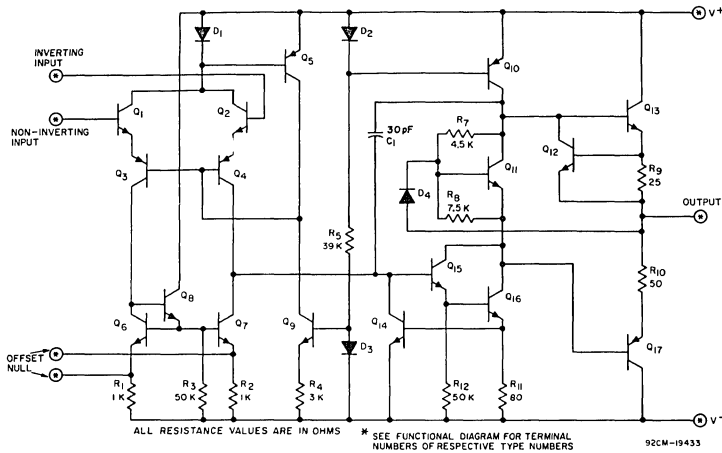


FIGURE 2. SCHEMATIC DIAGRAM OF OPERATIONAL AMPLIFIERS WITH INTERNAL PHASE COMPENSATION FOR CA741C, CA741, AND FOR EACH AMPLIFIER OF THE CA1458, AND CA1558

**CA741C, CA741, CA1458, CA1558, LM741, LM741C, LM1458, LM1558**

**ELECTRICAL CHARACTERISTICS**

Typical Values Intended Only for Design Guidance

| CHARACTERISTIC                    | TEST CONDITIONS<br>$V_{\pm} = \pm 15V$                          | TYPICAL VALUES<br>ALL TYPES | UNITS      |
|-----------------------------------|---|-----------------------------|------------|
| Input Capacitance, $C_I$          |   | 1.4                         | pF         |
| Offset Voltage Adjustment Range   |   | $\pm 15$                    | mV         |
| Output Resistance, $R_O$          |   | 75                          | $\Omega$   |
| Output Short-Circuit Current      |   | 25                          | mA         |
| Transient Response:               | Unity Gain<br>$V_I = 20mV, R_L = 2k\Omega,$<br>$C_L \leq 100pF$ |                             |            |
| Rise Time, $t_r$                  |   | 0.3                         | $\mu s$    |
| Overshoot                         |   | 5                           | %          |
| Slew Rate, $S_F$ :<br>Closed Loop | $R_L \geq 2k\Omega$   | 0.5                         | V/ $\mu s$ |

**ELECTRICAL CHARACTERISTICS**

For Equipment Design

| CHARACTERISTIC                                   | TEST CONDITIONS<br>Supply Voltage,<br>$V^+ = 15V,$<br>$V^- = -15V$ | Ambient<br>Temperature, $T_A$ | LIMITS            |          |      | UNITS      |
|--|--|-------------------------------|-------------------|----------|------|------------|
|  |  |                               | CA741C<br>CA1458* |          |      |            |
|  |  |                               | Min.              | Typ.     | Max. |            |
| Input Offset Voltage,<br>$V_{IO}$                | $R_S \leq 10k\Omega$   | 25 °C                         | –                 | 2        | 6    | mV         |
|  |  | 0 to 70 °C                    | –                 | –        | 7.5  |            |
| Input Offset Current,<br>$I_{IO}$                |  | 25 °C                         | –                 | 20       | 200  | nA         |
|  |  | 0 to 70 °C                    | –                 | –        | 300  |            |
| Input Bias Current,<br>$I_{IB}$                  |  | 25 °C                         | –                 | 80       | 500  | nA         |
|  |  | 0 to 70 °C                    | –                 | –        | 800  |            |
| Input Resistance, $R_I$                          |  |                               | 0.3               | 2        | –    | M $\Omega$ |
| Open-Loop Differential<br>Voltage Gain, $A_{OL}$ | $R_L \geq 2k\Omega$<br>$V_O = \pm 10V$                             | 25 °C                         | 20,000            | 200,000  | –    |            |
|  |  | 0 to 70 °C                    | 15,000            | –        | –    |            |
| Common-Mode Input<br>Voltage Range, $V_{ICR}$    |  | 25 °C                         | $\pm 12$          | $\pm 13$ | –    | V          |
| Common-Mode<br>Rejection Ratio, CMRR             | $R_S \leq 10k\Omega$   | 25 °C                         | 70                | 90       | –    | dB         |
| Supply-Voltage<br>Rejection Ratio, PSRR          | $R_S \leq 10k\Omega$   | 25 °C                         | –                 | 30       | 150  | $\mu V/V$  |
| Output Voltage Swing,<br>$V_{OPP}$               | $R_L \geq 10k\Omega$   | 25 °C                         | $\pm 12$          | $\pm 14$ | –    | V          |
|  |  | 25 °C                         | $\pm 10$          | $\pm 13$ | –    |            |
|  | $R_L \geq 2k\Omega$  | 0 to 70 °C                    | $\pm 10$          | $\pm 13$ | –    |            |
| Supply Current, $I^{\pm}$                        |  | 25 °C                         | –                 | 1.7      | 2.8  | mA         |
| Device Dissipation, $P_D$                        |  | 25 °C                         | –                 | 50       | 85   | mW         |

\* Values apply for each section of the dual amplifiers.

# CA741C, CA741, CA1458, CA1558, LM741, LM741C, LM1458, LM1558

## ELECTRICAL CHARACTERISTICS For Equipment Design

| CHARACTERISTIC                                   | TEST CONDITIONS<br>Supply Voltage,<br>$V^+ = 15\text{ V}$ ,<br>$V^- = -15\text{ V}$ |                | LIMITS           |          |      | UNITS           |
|--|---|----------------|------------------|----------|------|-----------------|
|  |   |                | CA741<br>CA1558* |          |      |                 |
|  | Ambient<br>Temperature, $T_A$   | Min.           | Typ.             | Max.     |      |                 |
| Input Offset Voltage, $V_{IO}$                   | $R_S \leq 10\text{ k}\Omega$  | 25 °C          | –                | 1        | 5    | mV              |
|  |   | –55 to +125 °C | –                | 1        | 6    |                 |
| Input Offset Current, $I_{IO}$                   |   | 25 °C          | –                | 20       | 200  | nA              |
|  |   | –55 °C         | –                | 85       | 500  |                 |
|  |   | +125 °C        | –                | 7        | 200  |                 |
| Input Bias Current, $I_{IB}$                     |   | 25 °C          | –                | 80       | 500  | nA              |
|  |   | –55 °C         | –                | 300      | 1500 |                 |
|  |   | +125 °C        | –                | 30       | 500  |                 |
| Input Resistance, $R_I$                          |   |                | 0.3              | 2        | –    | M $\Omega$      |
| Open-Loop Differential<br>Voltage Gain, $A_{OL}$ | $R_L \geq 2\text{ k}\Omega$<br>$V_O = \pm 10\text{ V}$                              | 25 °C          | 50,000           | 200,000  | –    |                 |
|  |   | –55 to +125 °C | 25,000           | –        | –    |                 |
| Common-Mode Input<br>Voltage Range, $V_{ICR}$    |   | –55 to +125 °C | $\pm 12$         | $\pm 13$ | –    | V               |
| Common-Mode<br>Rejection Ratio, $CMRR$           | $R_S \leq 10\text{ k}\Omega$  | –55 to +125 °C | 70               | 90       | –    | dB              |
| Supply Voltage<br>Rejection Ratio, $PSRR$        | $R_S \leq 10\text{ k}\Omega$  | –55 to +125 °C | –                | 30       | 150  | $\mu\text{V/V}$ |
| Output Voltage<br>Swing, $V_{OPP}$               | $R_L \geq 10\text{ k}\Omega$  | –55 to +125 °C | $\pm 12$         | $\pm 14$ | –    | V               |
|  | $R_L \geq 2\text{ k}\Omega$   | –55 to +125 °C | $\pm 10$         | $\pm 13$ | –    |                 |
| Supply Current, $I^{\pm}$                        |   | 25 °C          | –                | 1.7      | 2.8  | mA              |
|  |   | –55 °C         | –                | 2        | 3.3  |                 |
|  |   | +125 °C        | –                | 1.5      | 2.5  |                 |
| Device Dissipation, $P_D$                        |   | 25 °C          | –                | 50       | 85   | mW              |
|  |   | –55 °C         | –                | 60       | 100  |                 |
|  |   | +125 °C        | –                | 45       | 75   |                 |

\* Values apply for each section of the dual amplifiers.

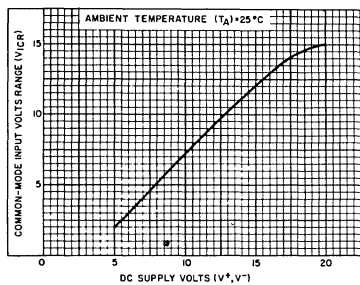


FIGURE 3. COMMON-MODE INPUT VOLTAGE RANGE vs. SUPPLY VOLTAGE FOR ALL TYPES.

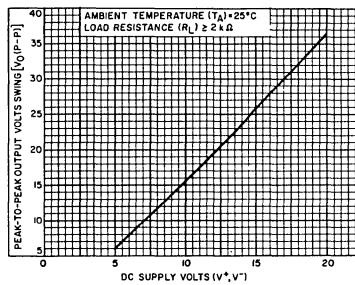


FIGURE 4. PEAK-TO-PEAK OUTPUT VOLTAGE vs. SUPPLY VOLTAGE FOR ALL TYPES

CA741C, CA741, CA1458, CA1558, LM741, LM741C, LM1458, LM1558

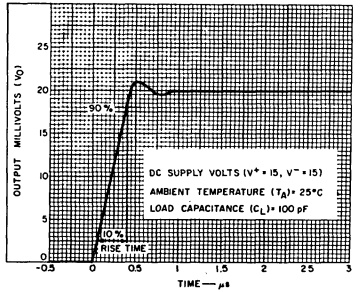


FIGURE 5. OUTPUT VOLTAGE vs. TRANSIENT RESPONSE TIME FOR CA741C AND CA741

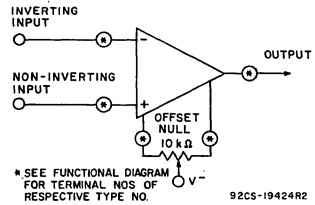


FIGURE 6. VOLTAGE OFFSET NULL CIRCUIT FOR CA741C AND CA741

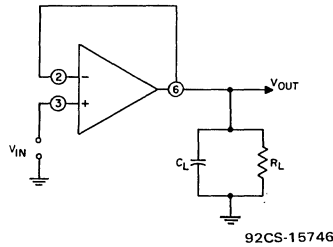
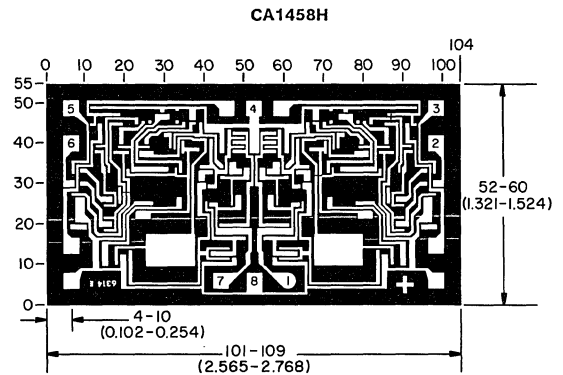
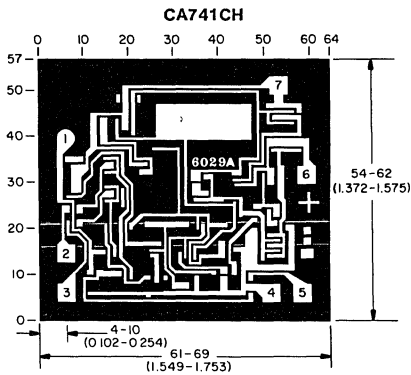


FIGURE 7. TRANSIENT RESPONSE TEST CIRCUIT FOR ALL TYPES

Chip Photos

DIMENSIONS AND PAD LAYOUTS



NOTE: Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

## Multipurpose Wide-Band Power Amplifiers Military, Industrial & Commercial Equip. @ Freq. Up to 8MHz

August 1991

### Features

- High Power Output Class B Amplifier
  - ▶ CA3020 ..... 0.5W Typ. at  $V_{CC} = +9V$
  - ▶ CA3020A ..... 1.0W Typ. at  $V_{CC} = +12V$
- Wide Frequency Range ..... Up to 8MHz With Resistive Loads
- High Power Gain ..... 75dB Typ.
- Single Power Supply For Class B Operation With Transformer
  - ▶ CA3020 ..... 3V to 9V
  - ▶ CA3020A ..... 3V to 12V
- Built-In Temperature-Tracking Voltage Regulator Provides Stable Operation Over - 55°C to +125°C Temperature Range

### Applications

- AF Power Amplifiers For Portable and Fixed Sound and Communications Systems
- Servo-Control Amplifiers
- Wide-Band Linear Mixers
- Video Power Amplifiers
- Transmission-Line Driver Amplifiers (Balanced and Unbalanced)
- Fan-In and Fan-Out Amplifiers For Computer Logic Circuits
- Lamp-Control Amplifiers
- Motor-Control Amplifiers
- Power Multivibrators
- Power Switches
- Companion Application Note, ICAN-5766, "Application of CA3020 and CA3020A Integrated Circuit Multipurpose Wide-Band Power Amplifiers"

### Description

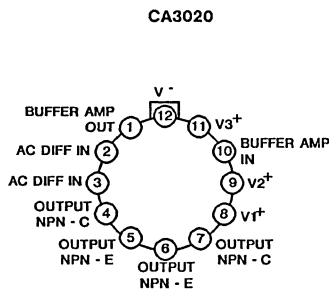
The CA3020 and CA3020A are integrated-circuit, multi-stage, multipurpose, wide-band power amplifiers on a single monolithic silicon chip. They employ a highly versatile and stable frequency-coupled circuit configuration featuring wide frequency range, high voltage and power gain, and high power output. These features plus inherent stability over a wide temperature range make the CA3020 and CA3020A extremely useful for a wide variety of applications in military, industrial, and commercial equipment.

The CA3020 and CA3020A are particularly suited for service as class B power amplifiers. The CA3020A can provide a maximum power output of 1 watt from a 12 volt dc supply with a typical power gain of 75dB. The CA3020 provides 0.5 watt power output from a 9 volt supply with the same power gain.

These types are supplied in hermetically sealed TO-5 style 12 lead packages.

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### Pinout



### Schematic Diagram

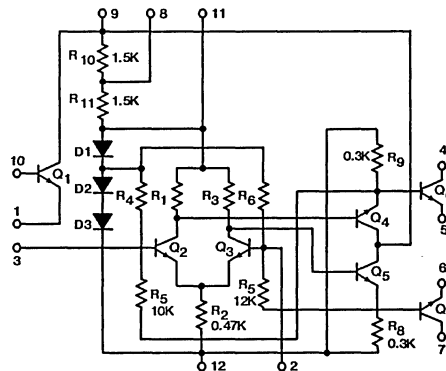


FIGURE1. DIAGRAM FOR CA3020 AND CA3020A

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as  $\pm 30\%$ .

Harris reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

# CA3020, CA3020A

## ABSOLUTE-MAXIMUM RATINGS:

| DISSIPATION:                             | WITHOUT HEAT SINK                        | WITH HEAT SINK   |
|--|--|--|
| At $T_A = 25^\circ\text{C}$ . . . . .    | 1 W                                      | At $T_C = 25^\circ\text{C}$ . . . . . 2 W  |
| Above $T_A = 25^\circ\text{C}$ . . . . . | derate linearly 6.7 mW/ $^\circ\text{C}$ | At $T_C = 25^\circ\text{C}$ to $T_C = 55^\circ\text{C}$ . . . . . 2 W              |
|  |  | Above $T_C = 55^\circ\text{C}$ . . . . . derate linearly 16.7 mW/ $^\circ\text{C}$ |

## TEMPERATURE RANGE:

|                     |   |
|---------------------|---|
| Operating . . . . . | -55 $^\circ\text{C}$ to +125 $^\circ\text{C}$ |
| Storage . . . . .   | -65 $^\circ\text{C}$ to +150 $^\circ\text{C}$ |

### MAXIMUM VOLTAGE RATINGS at $T_A = 25^\circ\text{C}$

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to terminal 12 is 0 to +10 volts.

| TERMINAL No. | 1 | 2 | 3 | 4                     | 5 | 6                     | 7 | 8      | 9                     | 10           | 11           | 12                    |
|--------------|---|---|---|-----------------------|---|-----------------------|---|--------|-----------------------|--------------|--------------|-----------------------|
| 1            | * | * | * | *                     | * | *                     | * | *      | $\Delta$ 0<br>-10/-12 | +3<br>Note 1 | *            | +10<br>0              |
| 2            |   | * | * | *                     | * | *                     | * | *      | *                     | *            | *            | +2<br>-2              |
| 3            |   |   | * | *                     | * | *                     | * | *      | *                     | *            | *            | +2<br>-2              |
| 4            |   |   |   | $\Delta$ +18/+25<br>0 | * | *                     | * | *      | *                     | *            | *            | $\Delta$ +18/+25<br>0 |
| 5            |   |   |   |                       | * | *                     | * | *      | *                     | *            | *            | +3<br>Note 2          |
| 6            |   |   |   |                       |   | $\Delta$ 0<br>-18/+25 | * | *      | *                     | *            | *            | +3<br>Note 2          |
| 7            |   |   |   |                       |   |                       | * | *      | *                     | *            | *            | $\Delta$ +18/+25<br>0 |
| 8            |   |   |   |                       |   |                       |   | Note 3 |                       | *            | *            | Note 3<br>0           |
| 9            |   |   |   |                       |   |                       |   |        | +10<br>0              | Note 1<br>0  | +10/+12<br>0 |                       |
| 10           |   |   |   |                       |   |                       |   |        |                       |              | *            | +10<br>0              |
| 11           |   |   |   |                       |   |                       |   |        |                       |              |              | *                     |
| 12           |   |   |   |                       |   |                       |   |        |                       |              |              | REF. SUB-STRATE       |

### MAXIMUM CURRENT RATINGS

| TERMINAL No. | $I_{IN}$<br>mA | $I_{OUT}$<br>mA |
|--------------|----------------|-----------------|
| 1            | -              | 20              |
| 2            | -              | -               |
| 3            | -              | -               |
| 4            | 300            | -               |
| 5            | -              | 300             |
| 6            | -              | 300             |
| 7            | 300            | -               |
| 8            | -              | -               |
| 9            | 20             | -               |
| 10           | 1              | -               |
| 11           | 20             | -               |
| 12           | -              | -               |

Note 1: This voltage is established by the maximum current rating.

Note 2: The emitters of  $Q_6$  and  $Q_7$  may be returned to a negative voltage supply through emitter resistors. Current into terminal No.9 should not be exceeded and the total device dissipation should not be exceeded.

Note 3: Terminal No.8 may be connected to terminals Nos.9, 11, or 12.

\* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

$\Delta$  Higher value is for CA3020A.

## CA3020, CA3020A

### ELECTRICAL CHARACTERISTICS AT $T_A = 25^\circ\text{C}$

| CHARACTERISTICS  | SYMBOLS                      | TEST CONDITIONS             |                         |           | LIMITS<br>CA3020 |                  |      | LIMITS<br>CA3020A |                   |      | UNITS              |
|--|------------------------------|-----------------------------|-------------------------|-----------|------------------|------------------|------|-------------------|-------------------|------|--------------------|
|  |                              | CIRCUIT<br>AND<br>PROCEDURE | DC<br>SUPPLY<br>VOLTAGE |           | MIN.             | TYP.             | MAX. | MIN.              | TYP.              | MAX. |                    |
|  |                              |                             | FIG.                    | $V_{CC1}$ |                  |                  |      |                   |                   |      |                    |
| Collector-to-Emitter<br>Breakdown Voltage, $Q_6$ & $Q_7$<br>at 10 mA | $V_{(BR)CER}$                | 2 <sub>a</sub>              | -                       | -         | 18               | -                | -    | 25                | -                 | -    | V                  |
| Collector-to-Emitter<br>Breakdown Voltage, $Q_1$<br>at 0.1 mA        | $V_{(BR)CEO}$                | -                           | -                       | -         | 10               | -                | -    | 10                | -                 | -    | V                  |
| Idle Currents, $Q_6$ & $Q_7$   | $I_4$ IDLE<br>$I_7$ IDLE     | 8                           | 9.0                     | 2.0       | -                | 5.5              | -    | -                 | 5.5               | -    | mA                 |
| Peak Output Currents,<br>$Q_6$ & $Q_7$                               | $I_4$ PK<br>$I_7$ PK         | 8                           | 9.0                     | 2.0       | 140              | -                | -    | 180               | -                 | -    | mA                 |
| Cutoff Currents,<br>$Q_6$ & $Q_7$                                    | $I_4$ CUTOFF<br>$I_7$ CUTOFF | 8                           | 9.0                     | 2.0       | -                | -                | 1.0  | -                 | -                 | 1.0  | mA                 |
| Differential Amplifier<br>Current Drain                              | $I_{CC1}$                    | 8                           | 9.0                     | 9.0       | 6.3              | 9.4              | 12.5 | 6.3               | 9.4               | 12.5 | mA                 |
| Total Current Drain  | $I_{CC1} + I_{CC2}$          | 8                           | 9.0                     | 9.0       | 8.0              | 21.5             | 35.0 | 14.0              | 21.5              | 30.0 | mA                 |
| Differential Amplifier<br>Input Terminal Voltages                    | $V_2$<br>$V_3$               | 8                           | 9.0                     | 2.0       | -                | 1.11             | -    | -                 | 1.11              | -    | V                  |
| Regulator Terminal Voltage   | $V_{11}$                     | 8                           | 9.0                     | 2.0       | -                | 2.35             | -    | -                 | 2.35              | -    | V                  |
| Q, Cutoff (Leakage) Currents:<br>Collector-to-Emitter                | $I_{CEO}$                    | -                           | 10.0                    | -         | -                | -                | 100  | -                 | -                 | 100  | $\mu\text{A}$      |
| Emitter-to-Base  | $I_{EBO}$                    | -                           | 3.0                     | -         | -                | -                | 0.1  | -                 | -                 | 0.1  |                    |
| Collector-to-Base  | $I_{CBO}$                    | -                           | 3.0                     | -         | -                | -                | 0.1  | -                 | -                 | 0.1  |                    |
| Forward Current Transfer<br>Ratio, $Q_1$ at 3 mA                     | $h_{FE1}$                    | -                           | 6.0                     | -         | 30               | 75               | -    | 30                | 75                | -    |                    |
| Bandwidth at -3 dB Point   | BW                           | 9                           | 6.0                     | 6.0       | -                | 8                | -    | -                 | 8                 | -    | MHz                |
| Maximum Power Output   | $P_{O(MAX)}$                 | 10                          | 6.0                     | 6.0       | 200              | 300 <sup>a</sup> | -    | 200               | 300 <sup>a</sup>  | -    | mW                 |
|  |                              |                             | 9.0                     | 9.0       | 400              | 550 <sup>a</sup> | -    | 400               | 550 <sup>a</sup>  | -    |                    |
|  |                              |                             | 9.0                     | 12.0      | -                | -                | -    | 800               | 1000 <sup>b</sup> | -    |                    |
| Sensitivity for $P_{OUT} = 400$ mW                                   | $e_{1N}$                     | 10                          | 9.0                     | 9.0       | -                | 35 <sup>a</sup>  | 55   | -                 | -                 | -    | mV                 |
| Sensitivity for $P_{OUT} = 800$ mW                                   | $e_{1N}$                     | 10                          | 9.0                     | 12.0      | -                | -                | -    | -                 | 50 <sup>b</sup>   | 100  | mV                 |
| Input Resistance---<br>Terminal 3 to Ground                          | $R_{IN3}$                    | 11                          | 6.0                     | 6.0       | -                | 1000             | -    | -                 | 1000              | -    | $\Omega$           |
| Junction-to-Case<br>Thermal Resistance                               | $\theta_{J-C}$               | -                           | -                       | -         | -                | -                | 60   | -                 | -                 | 60   | $^\circ\text{C/W}$ |

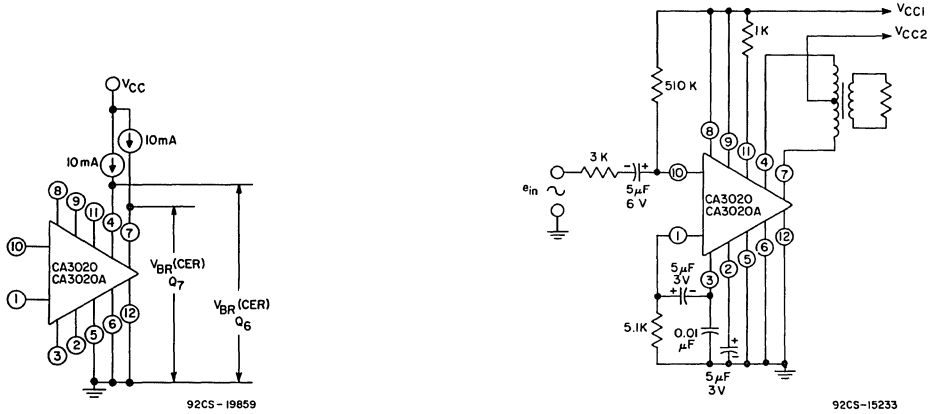
<sup>a</sup>  $R_{CC} = 130 \Omega$

<sup>b</sup>  $R_{CC} = 200 \Omega$

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# CA3020, CA3020A



a. Collector-to-Emitter Breakdown Voltage (Q<sub>6</sub> and Q<sub>7</sub>) Circuit

b. Typical Audio Amplifier Circuit Utilizing the CA3020 or CA3020A As An Audio Preamp and Class B Power Amplifier

Fig.2

## TYPICAL PERFORMANCE DATA\*

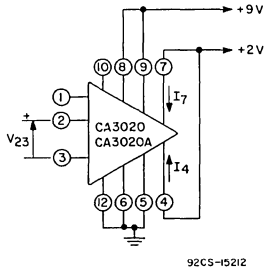
An External Radiator is Recommended for High Ambient Temperature Operation

| CHARACTERISTICS                                   | SYMBOLS                | CA3020 | CA3020A | UNITS      |
|---|------------------------|--------|---------|------------|
| Power Supply Voltage                              | $V_{CC1}$              | 9.0    | 9.0     | V          |
|   | $V_{CC2}$              | 9.0    | 12.0    |            |
| Zero Signal Current                               | Diff. Ampl. $I_{CC1}$  | 15     | 15      | mA         |
|   | Output Ampl. $I_{CC2}$ | 24     | 24      |            |
| Maximum Signal Current                            | Diff. Ampl. $I_{CC1}$  | 16     | 16.6    | mA         |
|   | Output Ampl. $I_{CC2}$ | 125    | 140     |            |
| Maximum Power Output at THD = 10%                 | $P_O$                  | 550    | 1000    | mW         |
| Sensitivity                                       | $e_{IN}$               | 35     | 45      | mV         |
| Power Gain  | $G_P$                  | 75     | 75      | dB         |
| Input Resistance                                  | $R_{IN}$               | 55     | 55      | k $\Omega$ |
| Efficiency  | $\eta$                 | 45     | 55      | %          |
| Signal-to-Noise Ratio                             | S/N                    | 70     | 66      | dB         |
| THD at 150 mW level                               |                        | 3.1    | 3.3     | %          |
| Test Signal Frequency from 600 $\Omega$ Generator |                        | 1000   | 1000    | Hz         |
| Equivalent Collector-to-Collector Load Resistance | $R_{CC}$               | 130    | 200     | $\Omega$   |

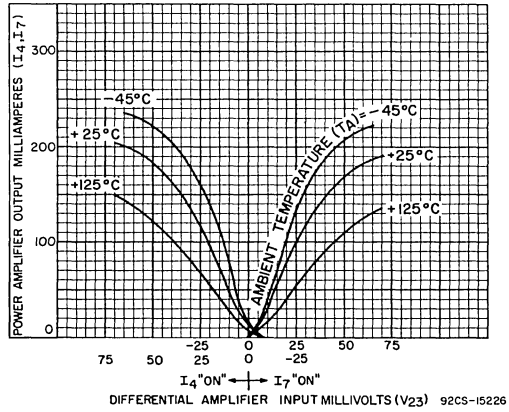
\* Refer to Figs.8 through 12 for Measurement and Symbol Information.

# CA3020, CA3020A

## TYPICAL TRANSFER CHARACTERISTICS

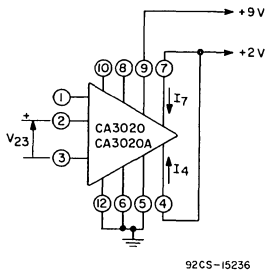


a. Test Setup

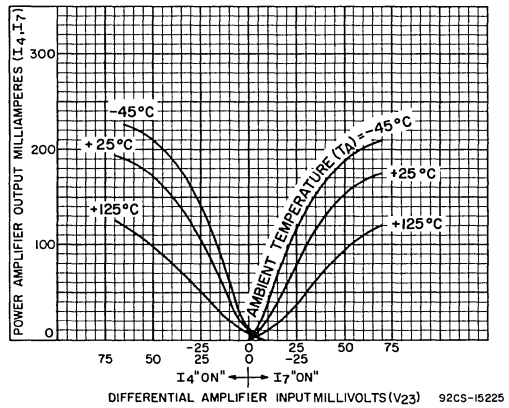


b. Characteristics with  $R_{10}$  shorted out

Fig.3



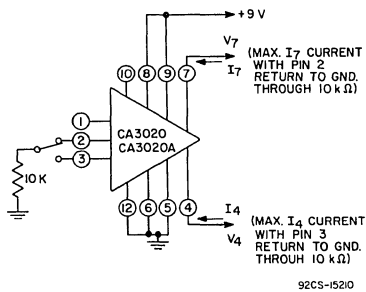
a. Test Setup



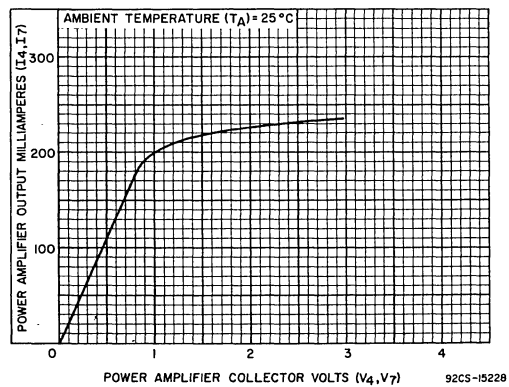
b. Characteristics with  $R_{10}$  in circuit

Fig.4

### "MINIMUM DRIVE" TYPICAL CURRENT-VOLTAGE SATURATION CURVE



a. Test Setup



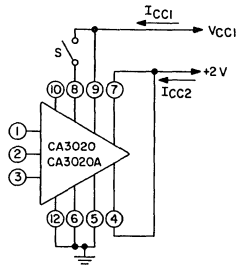
b. Characteristic

Fig.5

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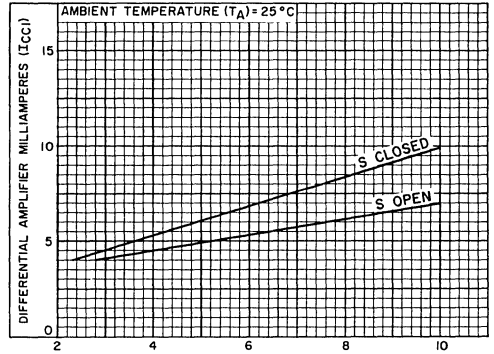
# CA3020, CA3020A

## ZERO SIGNAL AMPLIFIER CURRENT vs DIFFERENTIAL AMPLIFIER SUPPLY VOLTAGE



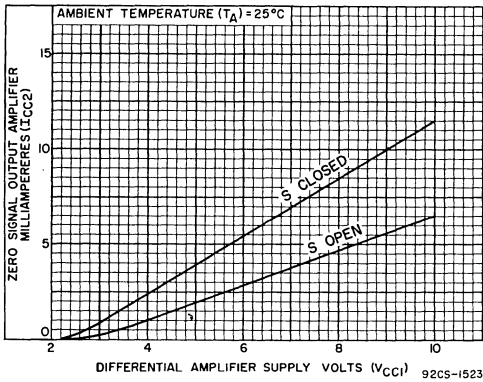
92CS-15211

a. Test Setup



DIFFERENTIAL AMPLIFIER SUPPLY VOLTS ( $V_{CC1}$ ) 92CS-15229

b. Differential Amplifier Characteristics

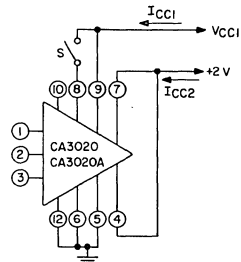


DIFFERENTIAL AMPLIFIER SUPPLY VOLTS ( $V_{CC1}$ ) 92CS-15231

c. Output Amplifier Characteristics

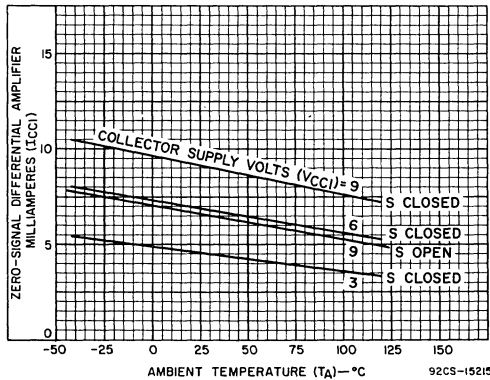
Fig. 6

## ZERO SIGNAL AMPLIFIER CURRENT vs AMBIENT TEMPERATURE



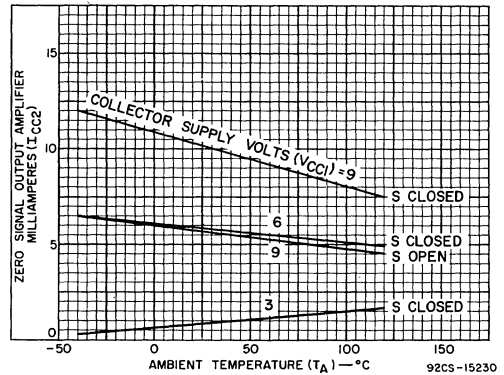
92CS-15213

a. Test Setup



AMBIENT TEMPERATURE ( $T_A$ ) — °C 92CS-15215

b. Differential Amplifier Characteristics



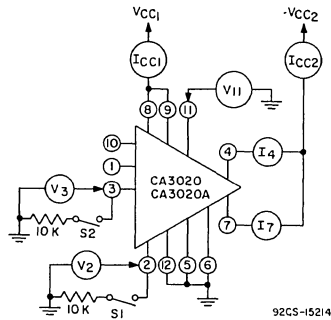
AMBIENT TEMPERATURE ( $T_A$ ) — °C 92CS-15230

c. Output Amplifier Characteristics

Fig. 7

# CA3020, CA3020A

## STATIC CURRENT AND VOLTAGE TEST CIRCUIT



| CURRENTS OR VOLTAGES  | S1    | S2    |
|-----------------------|-------|-------|
| I <sub>4-IDLE</sub>   | open  | open  |
| I <sub>7-IDLE</sub>   | open  | open  |
| I <sub>4-PEAK</sub>   | open  | close |
| I <sub>7-PEAK</sub>   | close | open  |
| I <sub>4-CUTOFF</sub> | close | open  |
| I <sub>7-CUTOFF</sub> | open  | close |

| CURRENTS OR VOLTAGES | S1   | S2   |
|----------------------|------|------|
| I <sub>CC1</sub>     | open | open |
| I <sub>CC2</sub>     | open | open |
| V <sub>2</sub>       | open | open |
| V <sub>3</sub>       | open | open |
| V <sub>11</sub>      | open | open |

Fig.8

## MEASUREMENT OF BANDWIDTH AT -3 dB POINTS

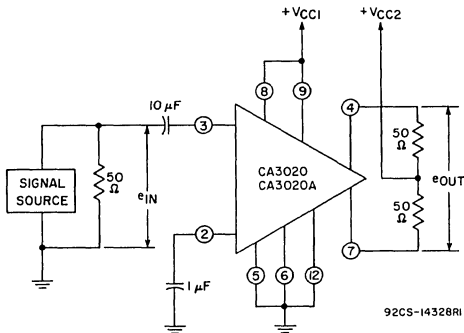
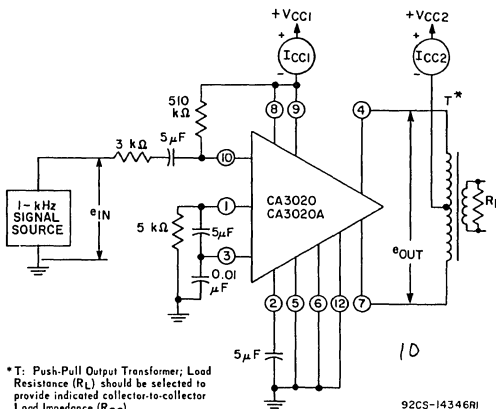


Fig.9

### PROCEDURES:

1. Apply desired value of  $V_{CC1}$  and  $V_{CC2}$ .
2. Apply 1 kHz input signal and adjust for  $e_{IN} = 5$  mV (rms)
3. Record the resulting value of  $e_{OUT}$  in dB (reference value)
4. Vary input-signal frequency, keeping  $e_{IN}$  constant at 5 mV, and record frequencies above and below 1 kHz at which  $e_{OUT}$  decreases 3 dB below reference value.
5. Record bandwidth as frequency range between -3 dB points.

## MEASUREMENTS OF ZERO-SIGNAL DC CURRENT DRAIN, MAXIMUM-SIGNAL DC CURRENT DRAIN, MAXIMUM POWER OUTPUT, CIRCUIT EFFICIENCY, SENSITIVITY, AND TRANSDUCER POWER GAIN



\*T: Push-Pull Output Transformer; Load Resistance ( $R_L$ ) should be selected to provide indicated collector-to-collector Load Impedance ( $R_{CL}$ )

### Maximum-Signal DC Current Drain, Maximum Power Output, Circuit Efficiency, Sensitivity, and Transducer Power Gain

1. Apply desired value of  $V_{CC1}$  and  $V_{CC2}$  and adjust  $e_{IN}$  to the value at which the  $e_{IN}$  Total Harmonic Distortion in the output of the amplifier = 10%
2. Record resulting value of  $I_{CC1}$  and  $I_{CC2}$  in mA as Maximum-Signal DC Current Drain
3. Determine resulting amplifier power output in watts and record as Maximum Power Output ( $P_{OUT}$ )
4. Calculate Circuit Efficiency ( $\eta$ ) in % as follows:

$$\eta = 100 \frac{P_{OUT}}{V_{CC1} I_{CC1} + V_{CC2} I_{CC2}}$$

where  $P_{OUT}$  is in watts,  $V_{CC1}$  and  $V_{CC2}$  are in volts, and  $I_{CC1}$  and  $I_{CC2}$  are in amperes.

5. Record value of  $e_{IN}$  in mV (rms) required in Step 1 as Sensitivity ( $e_{IN}$ )
6. Calculate Transducer Power Gain ( $G_p$ ) in dB as follows:

$$G_p = 10 \log_{10} \frac{P_{OUT}}{P_{IN}}$$

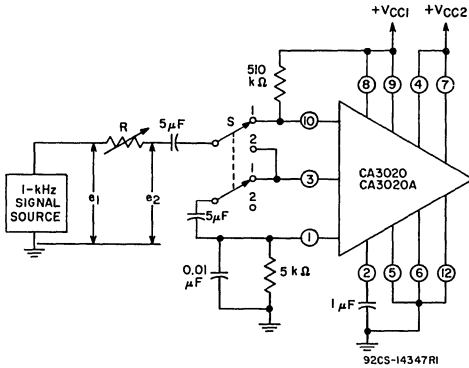
$$\text{where } P_{IN} \text{ (in mW)} = \frac{e_{IN}^2}{3000 + R_{IN(10)}}$$

Fig.10

3  
OPERATIONAL  
AMPLIFIERS

# CA3020, CA3020A

## MEASUREMENT OF INPUT RESISTANCE



### PROCEDURES:

Input Resistance Terminal 10 to Ground ( $R_{IN10}$ )

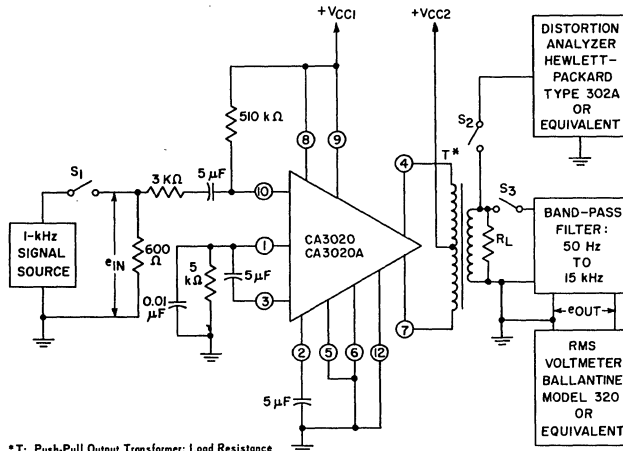
1. Apply desired value of  $V_{CC1}$  and  $V_{CC2}$  and set  $S$  in Position 1
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust  $R$  for  $e_2 = e_1/2$
4. Record resulting value of  $R$  as  $R_{IN10}$

Input Resistance Terminal 3 to Ground ( $R_{IN3}$ )

1. Apply desired value of  $V_{CC1}$  and  $V_{CC2}$  set  $S$  in Position 2
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust  $R$  for  $e_2 = e_1/2$
4. Record resulting value of  $R$  as  $R_{IN3}$

Fig.11

## MEASUREMENT OF SIGNAL-TO-NOISE RATIO AND TOTAL HARMONIC DISTORTION



\*T: Push-Pull Output Transformer; Load Resistance ( $R_L$ ) should be selected to provide indicated collector-to-collector Load Impedance ( $R_{CC}$ )

92CM-14329RI

### PROCEDURES:

#### Signal-to-Noise Ratio

1. Close  $S_1$  and  $S_3$ ; open  $S_2$
2. Apply desired values of  $V_{CC1}$  and  $V_{CC2}$
3. Adjust  $e_{IN}$  for an amplifier output of 150mW and record resulting value of  $E_{OUT}$  in dB as  $e_{OUT1}$  (reference value)
4. Open  $S_1$  and record resulting value of  $e_{OUT}$  in dB as  $e_{OUT2}$
5. Signal-to-Noise Ratio (S/N) =  $20 \log_{10} \frac{e_{OUT1}}{e_{OUT2}}$

#### Total Harmonic Distortion

1. Close  $S_1$  and  $S_2$ ; open  $S_3$
2. Apply desired values of  $V_{CC1}$  and  $V_{CC2}$
3. Adjust  $e_{IN}$  for desired level amplifier output power
4. Record Total Harmonic Distortion (THD) in %

Fig.12

August 1991

### Features

- Low Power Consumption as Low as 100mW Per Amplifier
- Independent Biasing for Each Amplifier
- High Forward Transconductance
- Programmable Range of Input Characteristics
- Low Input Bias and Input Offset Current
- High Input and Output Impedance
- No Effect on Device Under Output Short-Circuit Conditions
- Zener Diode Bias Regulator

### Applications

- For Low Power Conventional Operational Amplifier Applications
- Active Filters
- Comparators
- Gytrators
- Mixers
- Modulators
- Multiplexers
- Multipliers
- Strobing and Gating Functions
- Sample and Hold Functions

### Description

The CA3060 monolithic integrated circuit consists of an array of three independent Operational Transconductance Amplifiers.\* This type of amplifier has the generic characteristics of an operational voltage amplifier with the exception that the forward gain characteristic is best described by transconductance rather than voltage gain (open-loop voltage gain is the product of the transconductance and the load resistance,  $g_m R_L$ ). When operated into a suitable load resistor and with provisions for feedback, these amplifiers are well suited for a wide variety of operational-amplifier and related applications. In addition, the extremely high output impedance makes these types particularly well suited for service in active filter.

The three amplifiers in the CA3060 are identical push-pull Class A types which can be independently biased to achieve a wide range of characteristics for specific application. The electrical characteristics of each amplifier are a function of the amplifier bias current ( $I_{ABC}$ ). This feature offers the system designer maximum flexibility with regard to output current capability, noner consumption, slew rate, input resistance, input bias current, and input offset current. The linear variation of the parameters with respect to bias and the ability to maintain a constant dc level between input and output of each amplifier also makes the CA3060 suitable for a variety of non-linear applications such as mixers, multipliers, and modulators.

In addition, the CA3060 incorporates a unique Zener diode regulator system that permits current regulation below supply voltages normally associated with such systems.

The CA3060 is supplied in a 16-lead dual-in-line plastic package (E suffix) and in chip form (H suffix). This device is operational from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

### Block Diagram

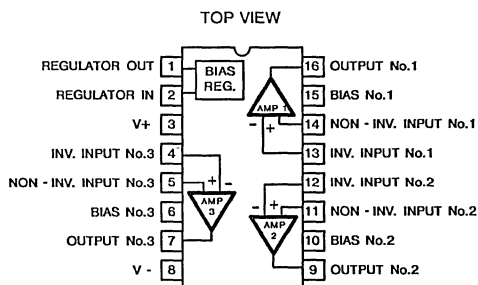


FIGURE 1 FUNCTIONAL BLOCK DIAGRAM FOR THE CA3060

\*Generic applications of the OTA are described in ICAN-6668. For improved input operating ranges, refer to CA3080 and CA3280 data bulletins (File Nos. 475 and 1174) and application notes ICAN-6668 and ICAN-6818.

# CA3060

## ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$ , $V_+ = 15\text{V}$ , $V_- = -15\text{V}$

| CHARACTERISTIC  | SYMBOL                     | TYPICAL CHARACTERISTICS CURVE Fig. | LIMITS                               |                                    |                                    |      |      | UNITS            |
|---|----------------------------|------------------------------------|--------------------------------------|------------------------------------|------------------------------------|------|------|------------------|
|   |                            |                                    | Amplifier Bias Current               |                                    |                                    |      |      |                  |
|   |                            |                                    | $I_{ABC} = 1\mu\text{A}$             | $I_{ABC} = 10\mu\text{A}$          | $I_{ABC} = 100\mu\text{A}$         | MIN. | TYP. |                  |
|   |                            |                                    | TYP.                                 | TYP.                               |                                    |      |      |                  |
| <b>STATIC CHARACTERISTICS</b>   |                            |                                    |                                      |                                    |                                    |      |      |                  |
| Input Offset Voltage  | $V_{IO}$                   | 3                                  | 1                                    | 1                                  | —                                  | 1    | 5    | mV               |
| Input Offset Current  | $I_{IO}$                   | 4                                  | 3                                    | 30                                 | —                                  | 250  | 1000 | nA               |
| Input Bias Current  | $I_{IB}$                   | 5a,b                               | 33                                   | 300                                | —                                  | 2500 | 5000 | nA               |
| Peak Output Current   | $I_{OM}$                   | 6a,b                               | 2.3                                  | 26                                 | 150                                | 240  | —    | $\mu\text{A}$    |
| Peak Output Voltage:  |                            |                                    |                                      |                                    |                                    |      |      |                  |
| Positive  | $V_{OM+}$                  | 7                                  | 13.6                                 | 13.6                               | 12                                 | 13.6 | —    | V                |
| Negative  | $V_{OM-}$                  |                                    | 14.7                                 | 14.7                               | 12                                 | 14.7 | —    |                  |
| Amplifier Supply Current (each amplifier)   | $I_A$                      | 8a,b                               | 8.5                                  | 85                                 | —                                  | 850  | 1200 | $\mu\text{A}$    |
| Power Consumption (each amplifier)  | P                          | —                                  | 0.26                                 | 2.6                                | —                                  | 26   | 36   | mW               |
| Input Offset-Voltage Sensitivity:   |                            |                                    |                                      |                                    |                                    |      |      |                  |
| Positive  | $\Delta V_{IO}/\Delta V_+$ | —                                  | 1.5                                  | 2                                  | —                                  | 2    | 150  | $\mu\text{V/V}$  |
| Negative  | $\Delta V_{IO}/\Delta V_-$ |                                    | 20                                   | 20                                 | —                                  | 30   | 150  |                  |
| Amplifier Bias Voltage*   | $V_{ABC}$                  | 9                                  | 0.54                                 | 0.60                               | —                                  | 0.66 | —    | V                |
| <b>DYNAMIC CHARACTERISTICS (at 1 kHz unless specified otherwise)</b>  |                            |                                    |                                      |                                    |                                    |      |      |                  |
| Forward Transconductance (large signal)   | $g_{21}$                   | 10a,b                              | 1.55                                 | 18                                 | 30                                 | 102  | —    | mmho             |
| Common-Mode Rejection Ratio   | CMRR                       | —                                  | 110                                  | 110                                | 70                                 | 90   | —    | dB               |
| Common-Mode Input Voltage Range   | $V_{ICR}$                  | —                                  | +12 to -12 min.<br>+13 to -14 typ.   | +12 to -12 min.<br>+13 to -14 typ. | +12 to -12 min.<br>+13 to -14 typ. |      |      | V                |
| Slew Rate (Test ckt., Fig. 13)  | SR                         | —                                  | 0.1                                  | 1                                  | —                                  | *    | —    | V/ $\mu\text{s}$ |
| Open-Loop ( $g_{21}$ ) Bandwidth  | $BW_{OL}$                  | 11                                 | 20                                   | 45                                 | —                                  | 110  | —    | kHz              |
| Input Impedance Components:   |                            |                                    |                                      |                                    |                                    |      |      |                  |
| Resistance  | $R_i$                      | 12                                 | 1600                                 | 170                                | 10                                 | 20   | —    | k $\Omega$       |
| Capacitance at 1 MHz  | $C_i$                      | —                                  | 2.7                                  | 2.7                                | —                                  | 2.7  | —    | pF               |
| Output Impedance Components:  |                            |                                    |                                      |                                    |                                    |      |      |                  |
| Resistance  | $R_o$                      | 14                                 | 200                                  | 20                                 | —                                  | 2    | —    | M $\Omega$       |
| Capacitance at 1 MHz  | $C_o$                      | —                                  | 4.5                                  | 4.5                                | —                                  | 4.5  | —    | pF               |
| <b>ZENER BIAS REGULATOR CHARACTERISTICS (at <math>T_A = 25^\circ\text{C}</math>, <math>I_z = 0.1\text{mA}</math>)</b> |                            |                                    |                                      |                                    |                                    |      |      |                  |
| Voltage   | $V_z$                      | 15                                 | Temp. Coeff. = 3mV/ $^\circ\text{C}$ | MIN.                               | TYP.                               | MAX. |      |                  |
|   |                            |                                    |                                      | 6.2                                | 6.7                                | 7.9  |      |                  |
| Impedance   | $Z_z$                      | —                                  |                                      | 200                                | 300                                |      |      | $\Omega$         |

\*Temperature-Coefficient; -2.2mV/ $^\circ\text{C}$  (at  $V_{ABC} = 0.54$ ,  $I_{ABC} = 1\mu\text{A}$ ); -2.1mV/ $^\circ\text{C}$  (at  $V_{ABC} = 0.60\text{V}$ ,  $I_{ABC} = 10\text{mA}$ ); -1.9mV/ $^\circ\text{C}$  (at  $V_{ABC} = 0.66\text{V}$ ,  $I_{ABC} = 100\text{mA}$ )

■ Conditions for Input Offset Voltage Sensitivity:

- (a) Bias current derived from the regulator with an appropriate resistor connected from terminal No. 1 to the bias terminal on the amplifier under test  
 $V_+$  is reduced to +13 volts for  $V_+$  sensitivity  
 $V_-$  is reduced to -13 volts for  $V_-$  sensitivity

(b)  $V_+$  sensitivity in  $\mu\text{V/V} = \frac{V_{\text{offset}} - V_{\text{offset}}}{1\text{ Volt}}$  for +13V and -15V supplies

$V_-$  sensitivity in  $\mu\text{V/V} = \frac{V_{\text{offset}} - V_{\text{offset}}}{1\text{ Volt}}$  for -13V and +15V supplies

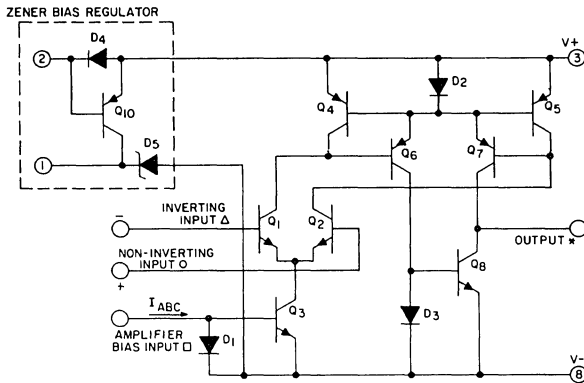
1 Volt

1 Volt

**MAXIMUM RATINGS, Absolute-Maximum Values at  $T_A = 25^\circ\text{C}$ :**

|  |  |
|--|--|
| DC SUPPLY VOLTAGE (BETWEEN $V^+$ and $V^-$ TERMINALS)                        | 36V ( $\pm 18\text{V}$ )                   |
| DIFFERENTIAL INPUT VOLTAGE (EACH AMPLIFIER)                                  | $\pm 5\text{V}$                            |
| DC INPUT VOLTAGE   | $V^+$ to $V^-$                             |
| INPUT SIGNAL CURRENT (EACH AMPLIFIER)  | $\pm 1\text{mA}$                           |
| AMPLIFIER BIAS CURRENT (EACH AMPLIFIER)                                      | 2 mA                                       |
| Bias Regulator Input Current   | -5mA                                       |
| OUTPUT SHORT-CIRCUIT DURATION*   | No limitation                              |
| DEVICE DISSIPATION   |  |
| Up to $T_A = 75^\circ\text{C}$   | 490mW                                      |
| Above $T_A = 75^\circ\text{C}$   | Derate linearly 6.67 mW/ $^\circ\text{C}$  |
| TEMPERATURE RANGE  |  |
| Operating  | $-40^\circ\text{C}$ to $+85^\circ\text{C}$ |
| Storage  | $-65$ to $+150^\circ\text{C}$              |
| LEAD TEMPERATURE (During Soldering)  |  |
| At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10s max. | $+300^\circ\text{C}$                       |

\*Short circuit may be applied to ground or to either supply



- Δ INVERTING INPUT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 13, 12 AND 4, RESPECTIVELY
- NON-INVERTING INPUT OF AMPLIFIERS 1, 2, AND 3 IS TERMINAL Nos. 14, 11, AND 5, RESPECTIVELY
- \* OUTPUT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 16, 9, AND 7, RESPECTIVELY
- AMPLIFIER BIAS CURRENT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 15, 10, AND 6, RESPECTIVELY

92CS-15860R1

Fig. 2 — Simplified schematic diagram showing bias regulator and one operational transconductance amplifier for the CA3060.

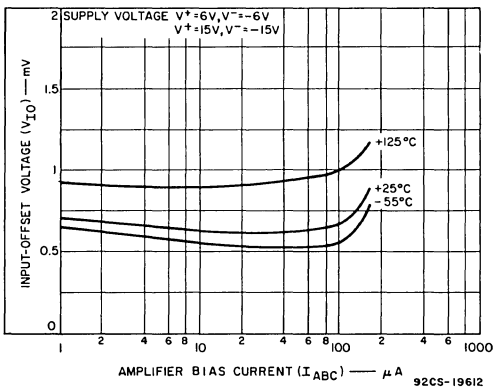


Fig.3—Input offset voltage vs. amplifier bias current.

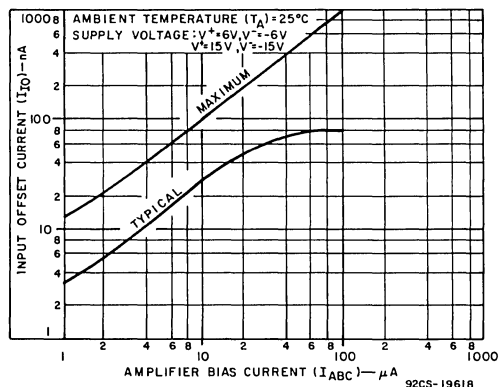


Fig.4—Input offset current vs. amplifier bias current.

3  
OPERATIONAL  
AMPLIFIERS



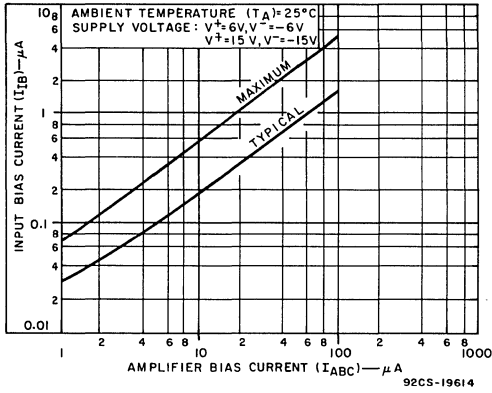


Fig. 5a—Input bias current vs. amplifier bias current

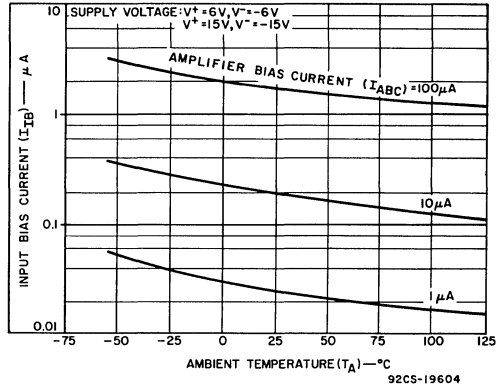


Fig. 5b—Input bias current vs. ambient temperature.

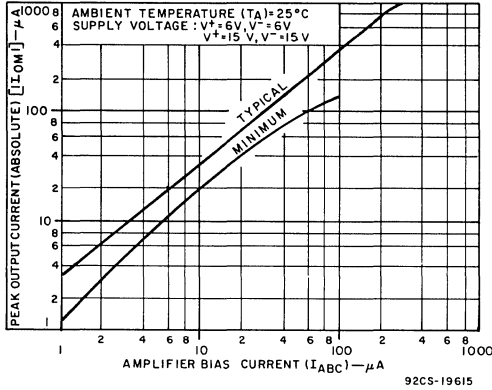


Fig. 6a—Peak output current vs. amplifier bias current.

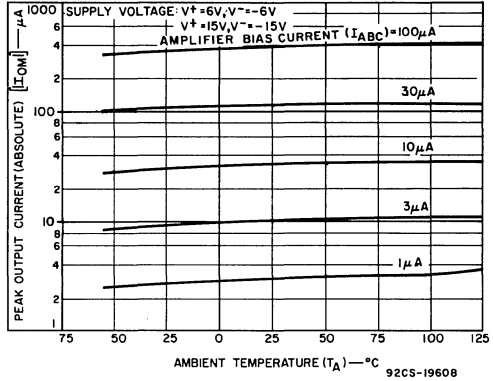


Fig. 6b—Peak output current vs. ambient temperature.

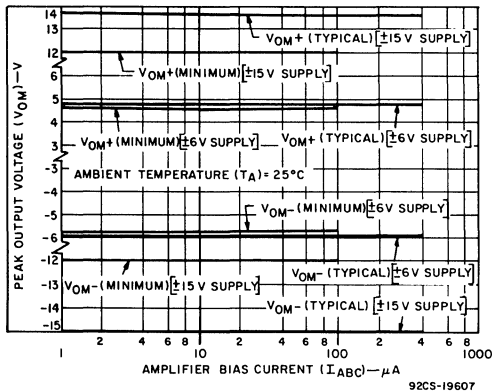


Fig. 7—Peak output voltage vs. amplifier bias current.

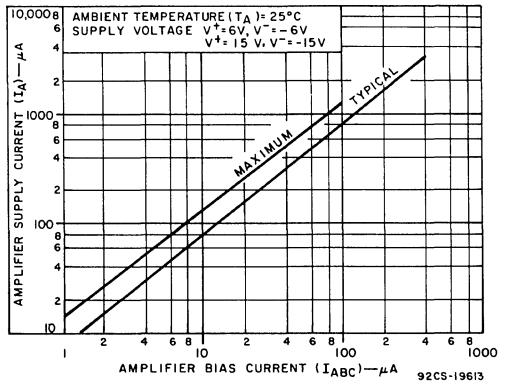


Fig. 8a—Amplifier supply current (each amplifier) vs. amplifier bias current.

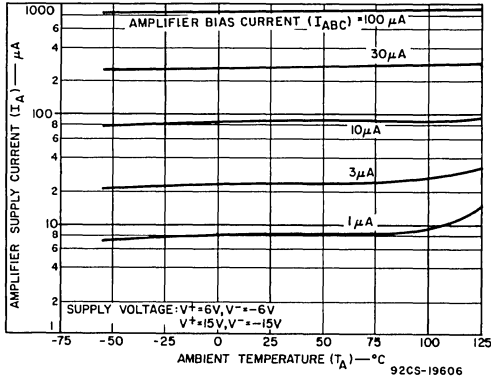


Fig.8b—Amplifier supply current (each amplifier) vs. ambient temperature.

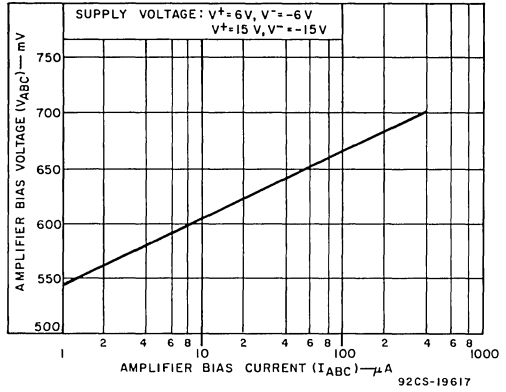


Fig.9—Amplifier bias voltage vs. amplifier bias current.

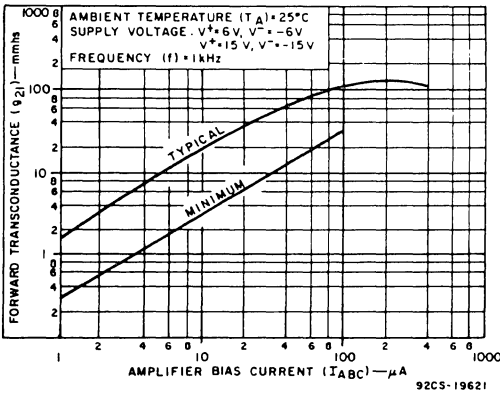


Fig.10a—Forward transconductance vs. amplifier bias current.

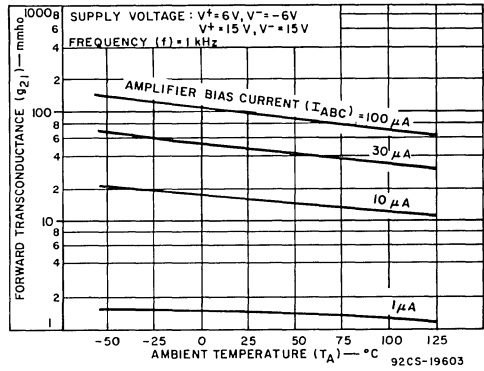


Fig.10b—Forward transconductance vs. ambient temperature.

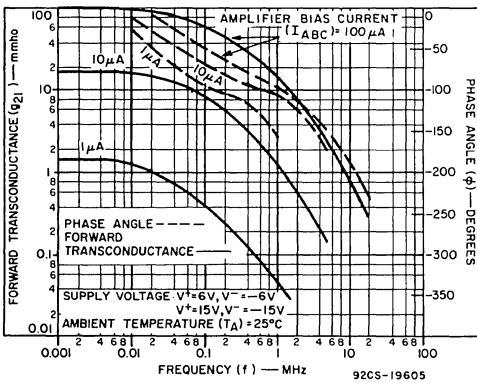


Fig.11—Forward transconductance vs. frequency.

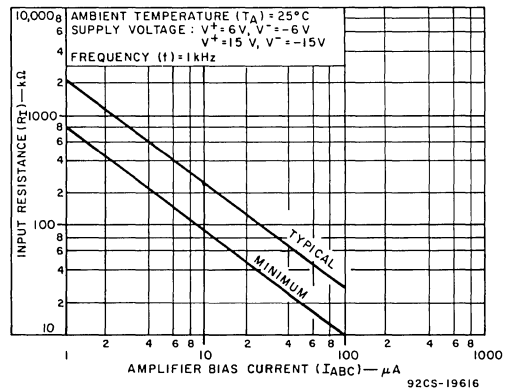
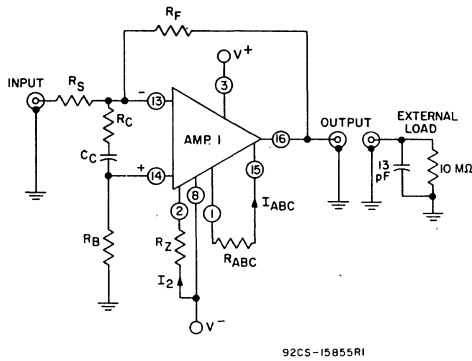


Fig.12—Input resistance vs. amplifier bias current.

# CA3060



92CS-15855RI

$V_Z$  is measured between terminals 1 and 8.

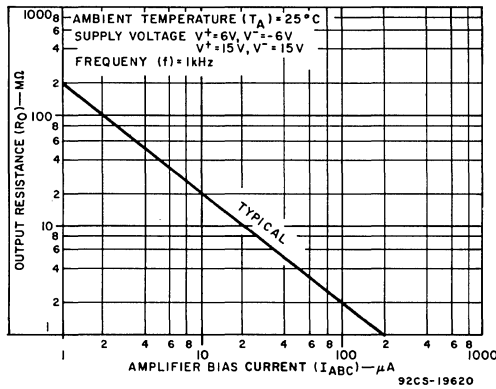
$V_{ABC}$  is measured between terminals 15 and 8.

$$R_Z = \frac{[(V^+) - (V^-) - 0.7]}{I_2}, \quad R_{ABC} = \frac{V_Z - V_{ABC}}{I_{ABC}}$$

Supply Voltage: for both  $\pm 6$  V and  $\pm 15$  V.

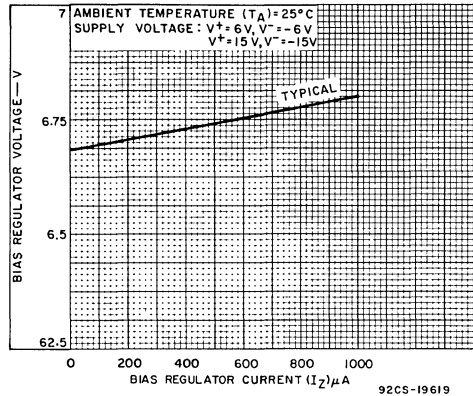
| TYPICAL SLEW RATE TEST CIRCUIT PARAMETERS |            |         |           |       |       |       |          |       |
|---|------------|---------|-----------|-------|-------|-------|----------|-------|
| $I_{ABC}$                                 | SLEW RATE  | $I_2$   | $R_{ABC}$ | $R_S$ | $R_F$ | $R_B$ | $R_C$    | $C_C$ |
| $\mu A$                                   | V/ $\mu s$ | $\mu A$ | ohms      |       |       |       | $\mu F$  |       |
| 100                                       | 8          | 200     | 62 k      | 100k  | 100k  | 51k   | 100      | 0.02  |
| 10  | 1          | 200     | 620k      | 1M    | 1M    | 510k  | 1k       | 0.005 |
| 1   | 0.1        | 2       | 6.2M      | 10M   | 10M   | 5.1M  | $\infty$ | 0     |

Fig. 13—Slew rate test circuit for amplifier No. 1 of CA3060.



92CS-19620

Fig. 14—Output resistance vs. amplifier bias current.



92CS-19619

Fig. 15—Bias regulator voltage vs. bias regulator current.

## OPERATING CONSIDERATIONS

The CA3060 consists of three operational amplifiers similar in form and application to conventional operational amplifiers but sufficiently different from the standard operational amplifier (op-amp) to justify some explanation of their characteristics. The amplifiers incorporated in the CA3060 are best described by the term Operational Transconductance Amplifier (OTA). The characteristics of an ideal OTA are similar to those of an ideal op-amp except that the OTA has an extremely high output impedance. Because of this inherent characteristic the output signal is best defined in terms of current which is proportional to the difference between the voltages of the two input terminals. Thus, the transfer characteristic is best described in terms of transconductance rather than voltage gain. Other than the difference given above, the characteristics tabulated on pages 3 and 4 of this data bulletin are similar to those of any typical op-amp.

The OTA circuitry incorporated in the CA3060 (See Fig. 16) provides the equipment designer with a wider variety of

circuit arrangements than does the standard op-amp; because as the curves in the data bulletin indicate, the user may select the optimum circuit conditions for a specific application simply by varying the bias conditions of each amplifier. If low power consumption, low bias, and low offset current, or high input impedance are primary design requirements, then low current operating conditions may be selected. On the other hand, if operation into a moderate load impedance is the primary consideration, then higher levels of bias may be used.

### Bias Considerations for Op-Amp Applications

The operational transconductance amplifiers allow the circuit designer to select and control the operating conditions of the circuit merely by the adjustment of the input bias current  $I_{ABC}$ . This enables the designer to have complete control over transconductance, peak output current and total power consumption independent of supply voltage.

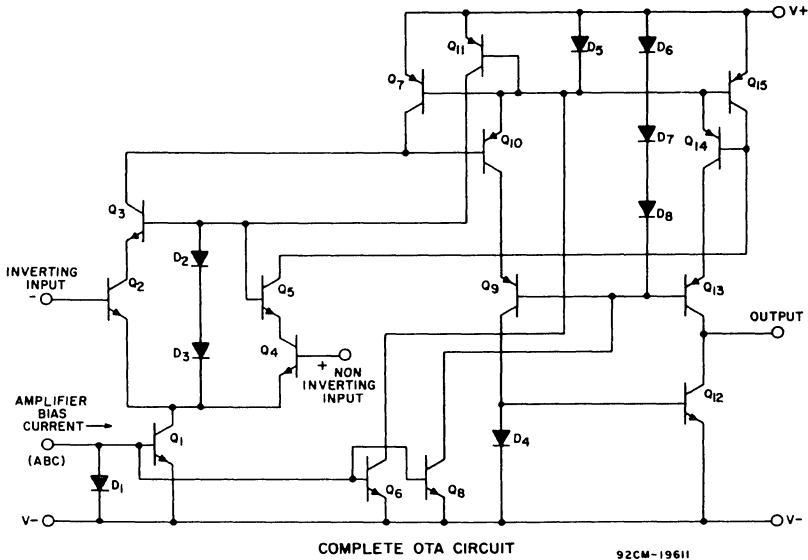


Fig.16—Complete schematic diagram showing bias regulator and one of the three operational transconductance amplifiers.

In addition, the high output impedance makes these amplifiers ideal for applications where current summing is involved.

The design of a typical operational amplifier circuit (See Fig. 17) would proceed as follows:

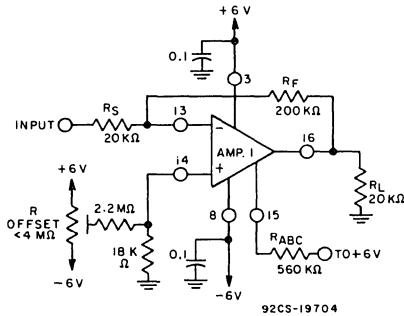


Fig.17—20-dB amplifier using the CA3060.

**Circuit Requirements**

- Closed loop voltage gain = 10 (20 dB)
- Offset voltage adjustable to zero
- Current drain as low as possible
- Supply voltage = ±6 V
- Maximum input voltage = ±50 mV
- Input resistance = 20 kΩ
- Load resistance = 20 kΩ
- Device: CA3060

**Calculation**

1. Required transconductance  $g_{21}$ .

Assume that the open loop gain  $A_{OL}$  must be at least ten times the closed loop gain. Therefore, the forward transconductance required is given by

$$g_{21} = A_{OL}/R_L$$

$$= 100/18 \text{ k}\Omega$$

$$\cong 5.5 \text{ mmho}$$

( $R_L = 20 \text{ k}\Omega$  in parallel with  $200 \text{ k}\Omega$ )

$$\cong 18 \text{ k}\Omega$$

2. Selection of suitable amplifier bias current.

The amplifier bias current is selected from the minimum value curve of transconductance (Fig. 10a) to assure that the amplifier will provide sufficient gain. For the required  $g_{21}$  of 5.5 mmho an amplifier bias current  $I_{ABC}$  of 20  $\mu\text{A}$  is suitable.

3. Determination of Output Swing Capability.

For a loop gain of 10 the output swing is  $\pm 0.5 \text{ V}$  and the peak load current 25  $\mu\text{A}$ . However, the amplifier must also supply the necessary current through the feedback resistor and for  $R_S = 20 \text{ k}\Omega$  than  $R_F = 200 \text{ k}\Omega$  if  $A_{OL} = 10$ . Therefore, the feedback loading =  $0.5/200 \text{ k}\Omega = 2.5 \mu\text{A}$ .

The total amplifier current output requirements are, therefore,  $\pm 27.5 \mu\text{A}$ . Referring to the data given in Fig. 6a we see that for an amplifier bias current of 20  $\mu\text{A}$  the amplifier output current is  $\pm 40 \mu\text{A}$ . This is obviously adequate and it is not necessary to change the amplifier bias current  $I_{ABC}$ .

4. Calculation of bias resistance.

For minimum supply current drain the amplifier bias current  $I_{ABC}$  should be fed directly from the supplies and not from the bias regulator. The value of the resistor  $R_{ABC}$  may be directly calculated using Ohm's law.

$$R_{ABC} = \frac{V_{SUP} - V_{ABC}}{I_{ABC}}$$

$$R_{ABC} = \frac{12 - 0.63}{20 \times 10^{-6}}$$

$$= 568.5 \text{ k}\Omega \text{ or } \cong 560 \text{ k}\Omega$$

5. Calculation of offset adjustment circuit.

In order to reduce the loading effect of the offset adjustment circuit on the power supply, the offset control should be arranged to provide the necessary offset current. The source resistance of the non-inverting input is made equal to the source resistance of the inverting input.

i.e.  $\frac{20 \times 200 \times 10^6 \text{ ohms}}{220 \times 10^3} \cong 18 \text{ k}\Omega$

Because the maximum offset voltage is 5 mV and an additional increment due to the offset current (Fig. 4) flowing through the source resistance

(i.e.  $200 \times 10^{-9} \times 18 \times 10^3 \text{ volts}$ ), therefore,

the Offset Voltage Range = 5 mV + 3.6 mV =  $\pm 8.6 \text{ mV}$

The current necessary to provide this offset is

$$\frac{8.6 \times 10^{-3}}{18 \times 10^3} \text{ or } 0.48 \mu\text{A}$$

With a supply voltage of  $\pm 6 \text{ V}$ , this current can be provided by a 10 M $\Omega$  resistor. However, the stability of such a resistor is often questionable and a more realistic value of 2.2 M $\Omega$  was used in the final circuit.

OTHER CONSIDERATIONS

Capacitance Effects

The CA3060 is designed to operate at such low power levels that high impedance circuits must be employed. In designing such circuits, particularly feedback amplifiers, stray circuit capacitance must always be considered because of its adverse effect on frequency response and stability. For example a 10-k $\Omega$  load with a stray capacitance of 15 pF has a time constant of 1 MHz. Fig. 18 illustrates how a 10-k $\Omega$  15-pF load modifies the frequency characteristic.

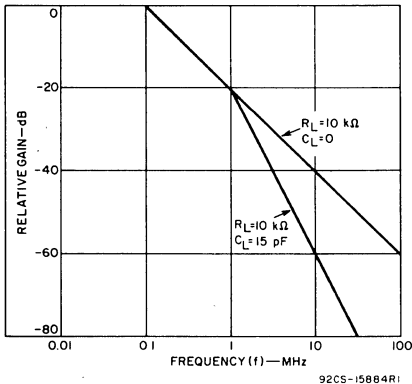


Fig. 18—Effect of capacitive loading on frequency response.

Capacitive loading also has an effect on slew rate; because the peak output current is established by the amplifier bias current,  $I_{ABC}$  (see Fig. 6a), the maximum slew rate is limited to the maximum rate at which the capacitance can be charged by the  $I_{OM}$ . Therefore,

$$SR = dV/dt = I_{OM}/C_L$$

where  $C_L$  is the total load capacitance including strays. This relationship is shown graphically in Fig. 19. When measuring slew rate for this data bulletin, care was taken to keep the total capacitive loading to 13 pF.

Phase Compensation

In many applications phase compensation will not be required for the amplifiers of the CA3060. When needed, compensation may easily be accomplished by a simple RC network at the input of the amplifier as shown in Fig. 13. The values given in Fig. 13 provide stable operation for the critical unity gain condition, assuming that capacitive loading on the output is 13 pF or less. Input phase compensation is recommended in order to maintain the highest possible slew rate.

In applications such as integrators, two OTAs may be cascaded to improve current gain. Compensation is best accomplished in this case with a shunt capacitor at the output of the first amplifier. The high gain following compensation assures a high slew rate.

APPLICATIONS

Having determined the operating points of the CA3060 amplifiers, they can now function in the same manner as conventional op-amps, and thus, are well suited for most op-amp applications, including inverting and non-inverting amplifiers, integrators, differentiators, summing amplifiers etc.

TRI-LEVEL COMPARATOR

Tri-level comparator circuits are an ideal application for the CA3060 since it contains the requisite three amplifiers. A tri-level comparator has three adjustable limits. If either the upper or lower limit is exceeded, the appropriate output is activated until the input signal returns to a selected intermediate limit. Tri-level comparators are particularly suited to many industrial control applications.

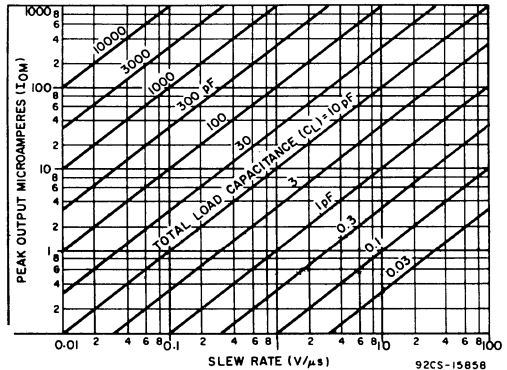


Fig. 19—Effect of load capacitance on slew rate.

# CA3060

## Circuit Description

Fig. 20 shows the block diagram of a tri-level comparator using the CA3060. Two of the three amplifiers are used to compare the input signal with the upper-limit and lower-

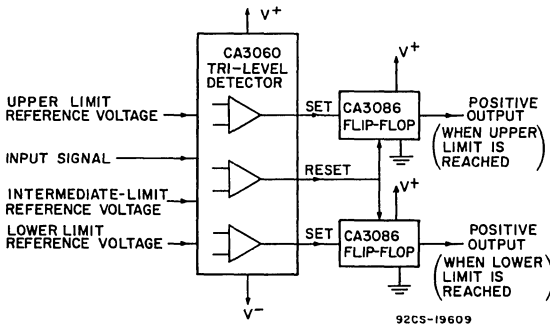


Fig.20—Functional block diagram of a tri-level comparator.

limit reference voltages. The third amplifier is used to compare the input signal with a selected value of intermediate-limit reference voltage. By appropriate selection or resistance ratios this intermediate-limit may be set to any voltage between the upper-limit and lower-limit values. The output of the upper-limit and lower-limit comparator sets the corresponding upper or lower-limit flip-flop. The activated flip-flop retains its state until the third comparator (intermediate-limit) in the CA3060 initiates a reset function, thereby indicating that the signal voltage has returned to the intermediate-limit selected. The flip-flops employ two CA3086 transistor-array IC's, with circuitry to provide separate "SET" and "POSITIVE OUTPUT" terminals.

The circuit diagram of a tri-level comparator appears in Fig. 21. Power is provided for the CA3060 via terminals 3 and 8 by  $\pm 6$ -volt supplies and the built-in regulator provides amplifier-bias-current ( $I_{ABC}$ ) to the three amplifiers via terminal 1. Lower-limit and upper-limit reference voltages are selected by appropriate adjustment of potentiometers R1 and R2, respectively. When resistors R3 and R4 are equal in value (as shown), the intermediate-limit reference voltage is automatically established at a value midway between the lower-limit and upper-limit values. Appropriate variation of resistors R3 and R4 permits selection of other values of intermediate-limit voltages. Input signal ( $E_S$ ) is applied to the three comparators via terminals 5, 12, and 14. The "SET" output lines trigger the appropriate flip-flop whenever the input signal reaches a limit value. When the input signal returns to an intermediate-value, the common flip-flop "RESET" line is energized. The loads in the circuits, shown in Fig. 21 are 5-V, 25-mA lamps.

## Active Filters — Using the CA3060 as a Gyrotor

The high output impedance of the OTAs makes the CA3060 ideally suited for use as a gyrotor in active filter applications. Fig. 22 shows two OTAs of the CA3060 connected as a gyrotor in an active filter circuit. The OTAs in this circuit can make a  $3\text{-}\mu\text{F}$  capacitor function as a floating 10-kilohm inductor across Terminals A and B. The measured Q of 13 (at a frequency of 1 Hz) of this inductor compares favorably with a calculated Q of 16. The 20-kilohm to 2-megohm attenuators in this circuit extend the dynamic range of the OTA by a factor of 100. The 100-kilohm potentiometer, across  $V^+$  and  $V^-$ , tunes the inductor by varying the  $g_{21}$  of the OTAs, thereby changing the gyration resistance.

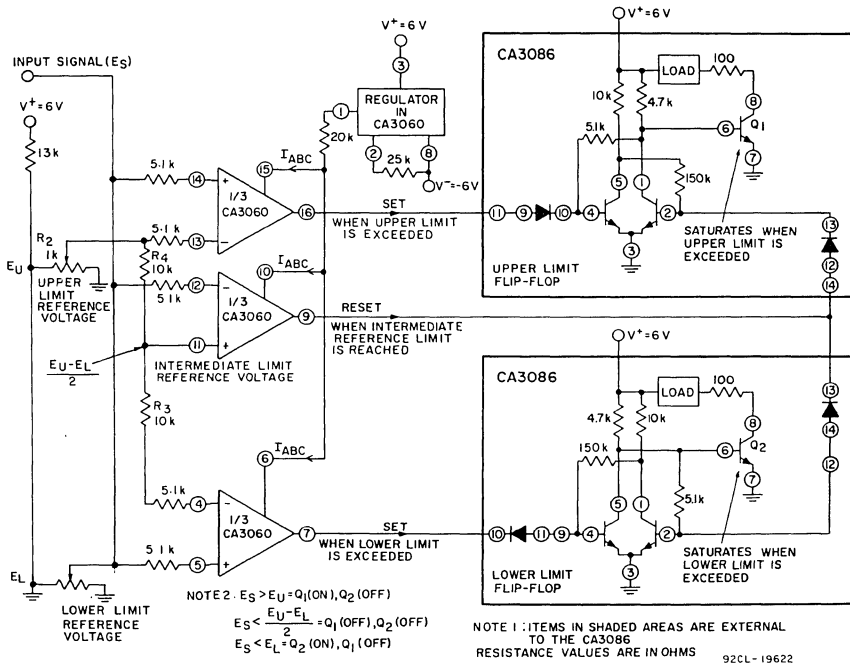


Fig.21—Tri-level comparator circuit.

## CA3060

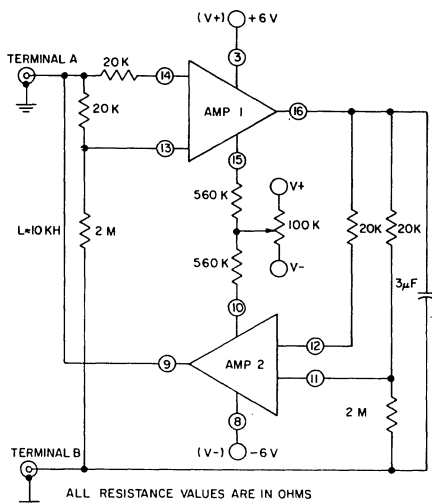


Fig.22—Two operational transconductance amplifiers of the CA3060 connected as a gyrator in an active filter circuit.

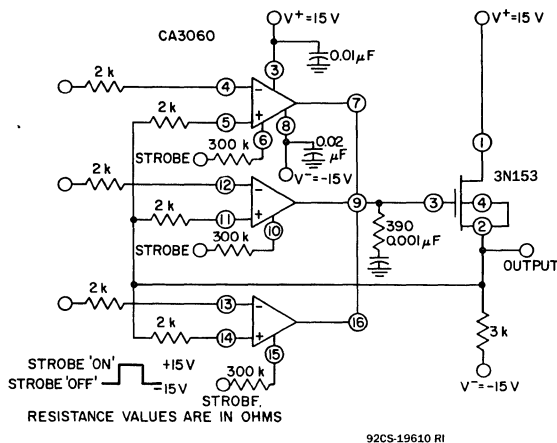


Fig.23—Three-channel multiplexer.

### THREE CHANNEL MULTIPLEXER

Fig. 23 shows a schematic of a three channel multiplexer using a single CA3060 and a 3N153 MOS/FET as a buffer and power amplifier.

When the CA3060 is connected as a high-input impedance voltage follower, and strobe "ON," each amplifier is activated and the output swings to the level of the input of that amplifier. The cascade arrangement of each CA3060 amplifier with the MOS/FET provides an open loop voltage gain in excess of 100 dB, thus assuring excellent accuracy in the voltage follower mode with 100% feedback.

Operation at  $\pm 6$  volts is also possible with several minor changes. First, the resistance in series with amplifier bias

current ( $I_{ABC}$ ) terminal of each amplifier should be decreased to maintain  $100 \mu A$  of strobe—"ON" current at this lower supply voltage. Second, the drain resistance for the MOS/FET should be decreased to maintain the same value of source current. The low cost dual-gate protected MOS/FET, RCA-40841, may be used when operating at the low supply voltage.

The phase compensation network consists of a single  $390\Omega$  resistor and a  $1000\text{-pF}$  capacitor, located at the interface of the CA3060 output and the MOS/FET gate. The bandwidth of the system is 1.5 MHz and the slew rate is  $0.3 \text{ volts}/\mu\text{sec}$ . The system slew rate is directly proportional to the value of the phase compensation capacitor. Thus, with higher gain settings where lower values of phase compensation capacitors are possible, the slew rate is proportionally increased.

### NON LINEAR APPLICATIONS

#### AM Modulator (Two-Quadrant Multiplier)

Fig. 24 shows Amplifier No. 3 of the CA3060 used in an AM modulator or 2-quadrant multiplier circuit. When modulation is applied to the amplifier bias input, Terminal B, and the carrier frequency to the differential input, Terminal A, the waveform, shown in Fig. 24, is obtained. Fig. 24 is a result of adjusting the input offset control to balance the circuit so that no modulation can occur at the output without a carrier input. The linearity of the modulator is indicated by the solid trace of the superimposed modulating frequency. The maximum depth of modulation is determined by the ratio of the peak input modulating voltage to  $V_{-}$ .

The two-quadrant multiplier characteristic of this modulator is easily seen if modulation and carrier are reversed as shown in Fig. 24. The polarity of the output must follow that of the differential input; therefore, the output is positive only during the positive half cycle of the modulation and negative only in the second half cycle. Note, that both the input and output signals are referenced to ground. The output signal is zero when either the differential input or  $I_{ABC}$  are zero.

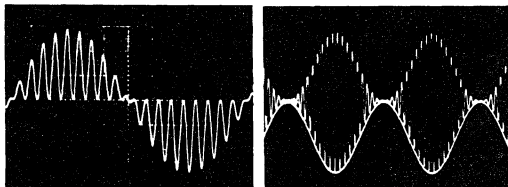
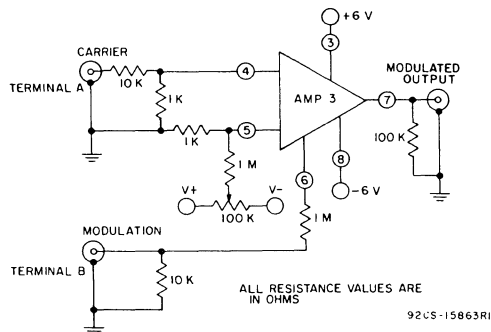


Fig.24—Two-quadrant multiplier circuit using the CA3060 with associated waveforms.

**Four-Quadrant Multiplier**

The CA3060 is also useful as a four-quadrant multiplier. A block diagram of such a multiplier, utilizing Amplifier Nos. 1, 2, and 3, is shown in Fig. 25 and a typical circuit is shown in Fig. 26. The multiplier consists of a single CA3060 and, as in the two-quadrant multiplier, exhibits no level shift between input and output. In Fig. 25, Amplifier No. 1 is connected as an inverting amplifier for the X-input signal. The output current of Amplifier No. 1 is calculated as follows:

$$I_{O(1)} = [-V_X] [g_{21}(1)] \tag{Eq. 3}$$

Ampl. No. 2 is a non-inverting amplifier so that

$$I_{O(2)} = [+V_X] [g_{21}(2)] \tag{Eq. 4}$$

Because the amplifier output impedances are high, the load current is the sum of the two output currents, for an output voltage

$$V_O = V_X R_L [g_{21}(2) \cdot g_{21}(1)] \tag{Eq. 5}$$

The transconductance is approximately proportional to the amplifier bias current; therefore, by varying the bias current the  $g_{21}$  is also controlled. Amplifier No. 2 bias current is proportional to the Y-input signal and is expressed as

$$I_{ABC(2)} \approx \frac{(V_-) + V_Y}{R_1} \tag{Eq. 6}$$

Hence,

$$g_{21}(2) \approx k [(V_-) + V_Y]. \tag{Eq. 7}$$

Bias for Amplifier No. 1 is derived from the output of Amplifier No. 3 which is connected as a unity-gain inverting amplifier.  $I_{ABC(1)}$ , therefore, varies inversely with  $V_Y$ . And by the same reasoning as above

$$g_{21}(1) \approx k [(V_-) \cdot V_Y]. \tag{Eq. 8}$$

Combining equation 5, 7, and 8 yields:

$$V_O \approx V_X \cdot k \cdot R_L \left\{ [(V_-) + V_Y] \cdot [(V_-) \cdot V_Y] \right\} \text{ or } V_O \approx 2k R_L V_X V_Y$$

Fig. 26 shows the actual circuit including all the adjustments associated with differential input and an adjustment for equalizing the gains of Amplifiers No. 1 and No. 2. Adjustment of the circuit is quite simple. With both the X and Y voltages at zero, connect Terminal 10 to Terminal 8. This procedure disables Amplifier No. 2 and permits adjusting the offset voltage of Amplifier No. 1 to zero by means of the 100-kΩ potentiometer. Next, remove the short between Terminals 10 and 8 and connect Terminal 15 to Terminal 8. This step disables Amplifier No. 1 and permits Amplifier No. 2 to be zeroed with the other potentiometer. With AC signals on both the X and Y input, R3 and R11 are adjusted for symmetrical output signals. Fig. 27 shows the output waveform with the multiplier adjusted. The voltage waveform in Fig. 27a shows suppressed carrier modulation of 1-kHz carrier with a triangular wave.

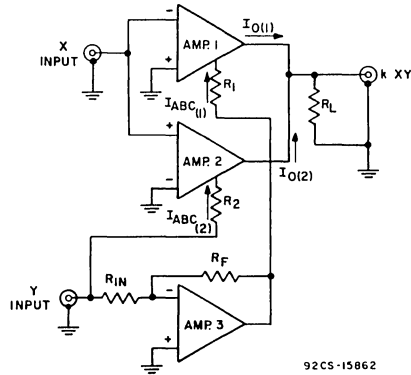


Fig. 25—Four-quadrant multiplier using the CA3060.

Figures 27b and 27c, respectively, show the squaring of a triangular wave and a sine wave. Notice that in both cases the outputs are always positive and return to zero after each cycle.

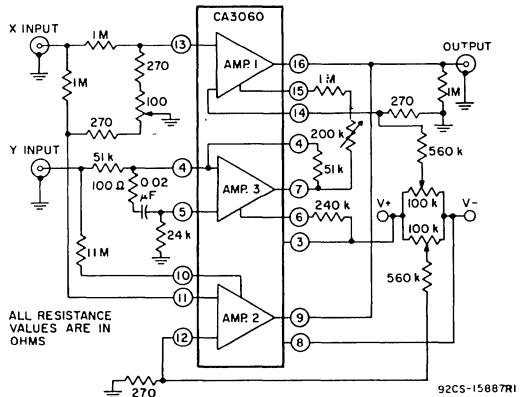


Fig. 26—Typical four-quadrant multiplier circuit.

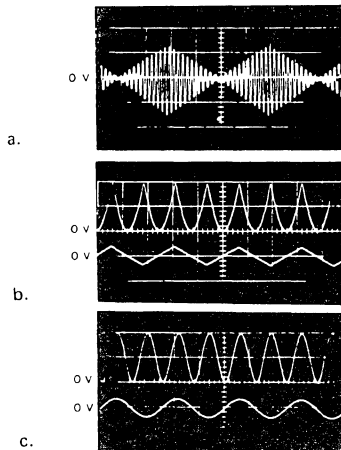


Fig. 27—Voltage waveforms of four-quadrant multiplier circuit.



August 1991

### Features

- Low Standby Power ..... As Low As 700nW
- Wide Supply Voltage Range .....  $\pm 0.75V$  to  $\pm 15V$
- High Peak Output Current ..... 6.5mA min.
- Adjustable Quiescent Current
- Output Short Circuit Protection

### Applications

- Portable Electronics
- Medical Electronics
- Instrumentation
- Telemetry
- Intrusion Alarms

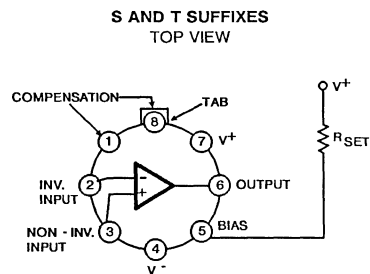
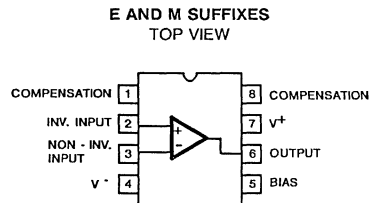
### Description

The CA3078 and CA3078A are high-gain monolithic operational amplifiers which can deliver milliamperes of current yet only consume microwatts of standby power. Their operating points are externally adjustable and frequency compensation may be accomplished with one external capacitor. The CA3078 and CA3078A provide the designer with the opportunity to tailor the frequency response and improve the slew rate without sacrificing power. Operation with a single 1.5 volt battery is a practical reality with these devices.

The CA3078A is a premium device having a supply voltage range of  $V_{\pm} = 0.75V$  to  $V_{\pm} = 15V$  and an operating temperature range of  $-55^{\circ}C$  to  $+125^{\circ}C$ . The CA3078 has the same lower supply voltage limit but the upper limit is  $V_{+} = +6V$  and  $V_{-} = -6V$ . The operating temperature range is from  $0^{\circ}C$  to  $+70^{\circ}C$ .

The CA3078 and CA3078A are supplied in the 8-lead Small Outline package (M suffix), the standard 8-lead TO-5 package ("T" suffix), the 8-lead dual-in-line formed-lead "DIL-CAN" package ("S" suffix), or the 8-lead dual-in-line plastic "MINI-DIP" package ("E" suffix).

### Pinouts



NOTE: Pin 4 is connected to case.

FIGURE 1

### Schematic Diagram

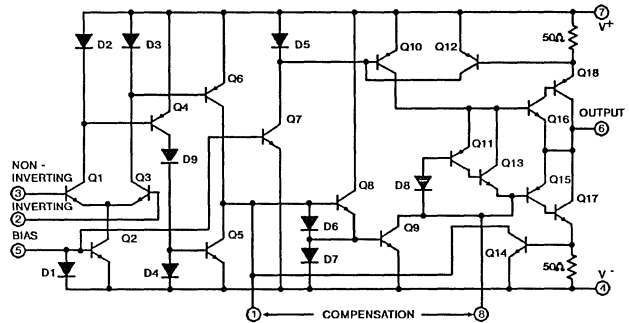


FIGURE 2 SCHEMATIC DIAGRAM OF THE CA3078 AND CA3078A

# CA3078, CA3078A

**MAXIMUM RATINGS, Absolute-Maximum Values at  $T_A = 25^\circ\text{C}$**

|  | CA3078A                             | CA3078                             |
|--|-------------------------------------|------------------------------------|
| DC Supply Voltage (between $V^+$ and $V^-$ terminal . . . . .)                       | 36 V                                | 14 V                               |
| Differential Input Voltage . . . . .   | $\pm 6$ V                           | $\pm 6$ V                          |
| DC Input Voltage . . . . .   | $V^+$ to $V^-$                      | $V^+$ to $V^-$                     |
| Input Signal Current . . . . .   | 0.1 mA                              | 0.1 mA                             |
| Output Short-Circuit Duration* . . . . .   | No Limitation                       | No Limitation                      |
| Device Dissipation . . . . .   | 150 mW (up to $125^\circ\text{C}$ ) | 500 mW (up to $70^\circ\text{C}$ ) |
| Temperature Range:   |                                     |                                    |
| Operating . . . . .  | $-55$ to $+125^\circ\text{C}$       | $0$ to $+70^\circ\text{C}$         |
| Storage . . . . .  | $-65$ to $+150^\circ\text{C}$       | $-65$ to $+150^\circ\text{C}$      |
| Lead Temperature (During Soldering):   |                                     |                                    |
| At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10s max. . . . . | $+300^\circ\text{C}$                | $+300^\circ\text{C}$               |

\* Short circuit may be applied to ground or to either supply.

## ELECTRICAL CHARACTERISTICS For Equipment Design

| CHARACTERISTICS SYMBOLS          | TEST CONDITIONS     |                     | CA3078A LIMITS                  |                          |                    |      |                                       |      | CA3078 LIMITS                 |                    |      |                                    | UNIT |                        |
|----------------------------------|---------------------|---------------------|---------------------------------|--------------------------|--------------------|------|---------------------------------------|------|-------------------------------|--------------------|------|------------------------------------|------|------------------------|
|                                  |                     |                     | $R_{SET} = 5.1 \text{ M}\Omega$ |                          |                    |      |                                       |      | $R_{SET} = 1 \text{ M}\Omega$ |                    |      |                                    |      |                        |
|                                  | $V^+$<br>&<br>$V^-$ | $R_S$<br>k $\Omega$ | $R_L$<br>k $\Omega$             | $T_A = 25^\circ\text{C}$ |                    |      | $T_A = -55$ to<br>$125^\circ\text{C}$ |      | $T_A = 25^\circ\text{C}$      |                    |      | $T_A = 0$ to<br>$70^\circ\text{C}$ |      |                        |
|                                  |                     |                     |                                 | MIN.                     | TYP.               | MAX. | MIN.                                  | MAX. | MIN.                          | TYP.               | MAX. | MIN.                               |      | MAX.                   |
| $V_{IO}$                         | 6                   | $\leq 10$           | —                               | —                        | 0.70               | 3.5  | —                                     | 4.5  | —                             | 1.3                | 4.5  | —                                  | 5    | mV                     |
| $I_{IO}$                         |                     | —                   | —                               | —                        | 0.50               | 2.5  | —                                     | 5.0  | —                             | 6                  | 32   | —                                  | 40   | nA                     |
| $I_{IB}$                         |                     | —                   | —                               | —                        | 7                  | 12   | —                                     | 50   | —                             | 60                 | 170  | —                                  | 200  | nA                     |
| $A_{OL}$                         |                     | —                   | $\geq 10$                       | 92                       | 100                | —    | 90                                    | —    | 88                            | 92                 | —    | 86                                 | —    | dB                     |
| $I_Q$                            |                     | —                   | —                               | —                        | 20                 | 25   | —                                     | 45   | —                             | 100                | 130  | —                                  | 150  | $\mu\text{A}$          |
| $P_D$                            |                     | —                   | —                               | —                        | 240                | 300  | —                                     | 540  | —                             | 1200               | 1560 | —                                  | 1800 | $\mu\text{W}$          |
| $V_{OM}$                         |                     | —                   | $\geq 10$                       | $\pm 5.1$                | $\pm 5.3$          | —    | $\pm 5$                               | —    | $\pm 5.1$                     | $\pm 5.3$          | —    | $\pm 5$                            | —    | V                      |
| $V_{ICR}$                        |                     | $\leq 10$           | —                               | —                        | -5.5<br>to<br>+5.8 | —    | -5<br>to<br>+5                        | —    | —                             | -5.5<br>to<br>+5.8 | —    | -5<br>to<br>+5                     | —    | V                      |
| CMRR                             |                     | $\leq 10$           | —                               | 80                       | 115                | —    | —                                     | —    | 80                            | 110                | —    | —                                  | —    | dB                     |
| $I_{OM}^+$ or $I_{OM}^-$         |                     | —                   | —                               | —                        | 12                 | —    | 6.5                                   | 30   | —                             | 12                 | —    | 6.5                                | 30   | mA                     |
| $\Delta V_{IO}/\Delta V^+$       |                     | $\leq 10$           | —                               | 76                       | 105                | —    | —                                     | —    | 76                            | 93                 | —    | —                                  | —    | $\mu\text{V}/\text{V}$ |
| $\Delta V_{IO}/\Delta V^-$       |                     |                     | —                               | 76                       | 105                | —    | —                                     | —    | 76                            | 93                 | —    | —                                  | —    |                        |
| $R_{SET} = 13 \text{ M}\Omega$ , |                     |                     |                                 |                          |                    |      |                                       |      |                               |                    |      |                                    |      |                        |
| $V_{IO}$                         |                     | 15                  | $\leq 10$                       | —                        | —                  | 1.4  | 3.5                                   | —    | 4.5                           | —                  | —    | —                                  | —    | —                      |
| $A_{OL}$                         | —                   |                     | $\geq 10$                       | 92                       | 100                | —    | 88                                    | —    | —                             | —                  | —    | —                                  | —    | dB                     |
| $I_Q$                            | —                   |                     | —                               | —                        | 20                 | 30   | —                                     | 50   | —                             | —                  | —    | —                                  | —    | $\mu\text{A}$          |
| $P_D$                            | —                   |                     | —                               | —                        | 600                | 750  | —                                     | 1350 | —                             | —                  | —    | —                                  | —    | $\mu\text{W}$          |
| $V_{OM}$                         | —                   |                     | $\geq 10$                       | $\pm 13.7$               | $\pm 14.1$         | —    | $\pm 13.5$                            | —    | —                             | —                  | —    | —                                  | —    | V                      |
| CMRR                             | $\leq 10$           |                     | —                               | 80                       | 106                | —    | —                                     | —    | —                             | —                  | —    | —                                  | —    | dB                     |
| $I_{IB}$                         | —                   |                     | —                               | —                        | 7                  | 14   | —                                     | 55   | —                             | —                  | —    | —                                  | —    | nA                     |
| $I_{IO}$                         | —                   |                     | —                               | —                        | 0.50               | 2.7  | —                                     | 5.5  | —                             | —                  | —    | —                                  | —    | nA                     |

3

OPERATIONAL AMPLIFIERS

## CA3078, CA3078A

ELECTRICAL CHARACTERISTICS, at  $T_A = 25^\circ\text{C}$

Typical Values Intended Only for Design Guidance

| CHARACTERISTICS SYMBOLS      | TYPICAL VALUES   |   |  |   | UNITS                  |
|------------------------------|--|---|--|---|------------------------|
|                              | CA3078A  |   | CA3078   |   |                        |
|                              | $V^+ = +1.3\text{ V}$ ,<br>$V^- = -1.3\text{ V}$<br>$R_{SET} = 2\text{ M}\Omega$ | $V^+ = +0.75\text{ V}$ ,<br>$V^- = -0.75\text{ V}$<br>$R_{SET} = 10\text{ M}\Omega$ | $V^+ = +1.3\text{ V}$ ,<br>$V^- = -1.3\text{ V}$<br>$R_{SET} = 2\text{ M}\Omega$ | $V^+ = +0.75\text{ V}$ ,<br>$V^- = -0.75\text{ V}$<br>$R_{SET} = 10\text{ M}\Omega$ |                        |
| $V_{IO}$                     | 0.7  | 0.9   | 1.3  | 1.5   | mV                     |
| $I_{IO}$                     | 0.3  | 0.054   | 1.7  | 0.5   | nA                     |
| $I_{IB}$                     | 3.7  | 0.45  | 9  | 1.3   | nA                     |
| $A_{OL}$                     | 84   | 65  | 80   | 60  | dB                     |
| $I_Q$                        | 10   | 1   | 10   | 1   | $\mu\text{A}$          |
| $P_D$                        | 26   | 1.5   | 26   | 1.5   | $\mu\text{W}$          |
| $V_{OPP}$                    | 1.4  | 0.3   | 1.4  | 0.3   | V                      |
| $V_{ICR}$                    | -0.8<br>to<br>+1.1   | -0.2<br>to<br>+0.5  | -0.8<br>to<br>+1.1   | -0.2<br>to<br>+0.5  | V                      |
| CMRR                         | 100  | 90  | 100  | 90  | dB                     |
| $I_{OM}^\pm$                 | 12   | 0.5   | 12   | 0.5   | mA                     |
| $\Delta V_{IO}/\Delta V^\pm$ | 20   | 50  | 20   | 50  | $\mu\text{V}/\text{V}$ |

Typical Values Intended Only for Design Guidance at  $T_A = 25^\circ\text{C}$  and  $V^+ = +6\text{ V}$ ,  $V^- = -6\text{ V}$

| CHARACTERISTICS SYMBOLS    | TEST CONDITIONS              | CA3078A                        |                              | CA3078                       | UNITS                        |
|----------------------------|------------------------------|--------------------------------|------------------------------|------------------------------|------------------------------|
|                            |                              | $R_{SET} = 5.1\text{ M}\Omega$ | $R_{SET} = 1\text{ M}\Omega$ | $R_{SET} = 1\text{ M}\Omega$ |                              |
| $\Delta V_{IO}/\Delta T_A$ | $R_S \leq 10\text{ k}\Omega$ | 5                              | 6                            | 6                            | $\mu\text{V}/^\circ\text{C}$ |
| $\Delta I_{IO}/\Delta T_A$ | $R_S \leq 10\text{ k}\Omega$ | 6.3                            | 70                           | 70                           | $\text{pA}/^\circ\text{C}$   |
| $BW_{OL}$                  | 3dB pt.                      | 0.3                            | 2                            | 2                            | kHz                          |
| SR                         | See Figs. 20, 21             | 0.027                          | 0.04                         | 0.04                         | V/ $\mu\text{s}$             |
|                            |                              | 0.5                            | 1.5                          | 1.5                          |                              |
| —                          | 10% to 90% Rise Time         | 3                              | 2.5                          | 2.5                          | $\mu\text{s}$                |
| $R_I$                      |                              | 7.4                            | 1.7                          | 0.87                         | $\text{M}\Omega$             |
| $R_O$                      |                              | 1                              | 0.8                          | 0.8                          | k $\Omega$                   |
| $e_N(10\text{ Hz})$        | $R_S = 0$                    | 40                             | —                            | 25                           | $\text{nV}/\sqrt{\text{Hz}}$ |
| $i_N(10\text{ Hz})$        | $R_S = 1\text{ M}\Omega$     | 0.25                           | —                            | 1                            | $\text{pA}/\sqrt{\text{Hz}}$ |

# CA3078, CA3078A

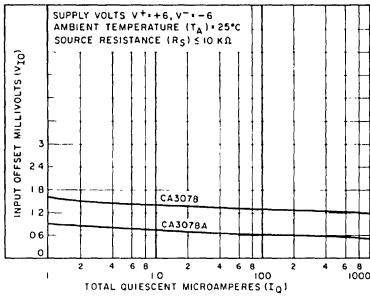


Fig. 3 - Input offset voltage vs. total quiescent current.

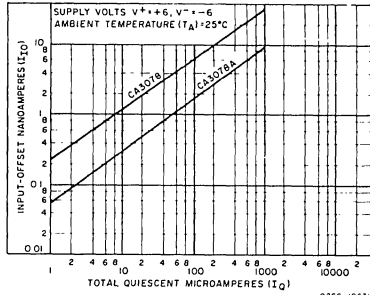


Fig. 4 - Input offset current vs. total quiescent current.

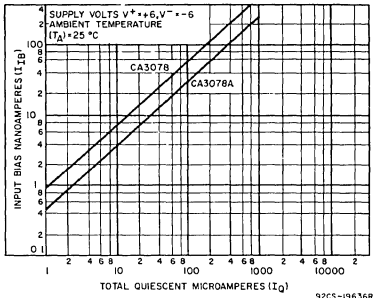


Fig. 5 - Input bias current vs. total quiescent current.

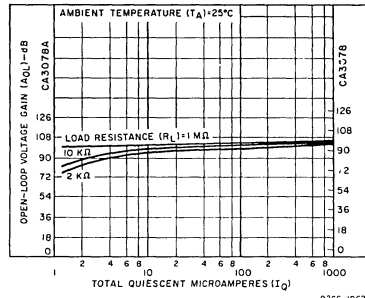


Fig. 6 - Open-loop voltage gain vs. total quiescent current.

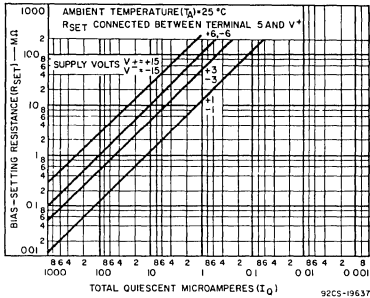


Fig. 7 - Bias-setting resistance vs. total quiescent current.

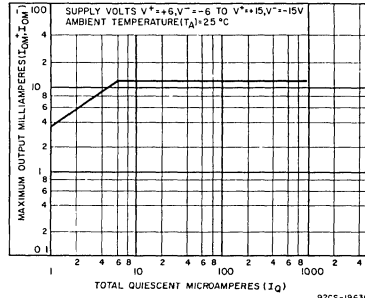


Fig. 8 - Maximum output current vs. total quiescent current.

# CA3078, CA3078A

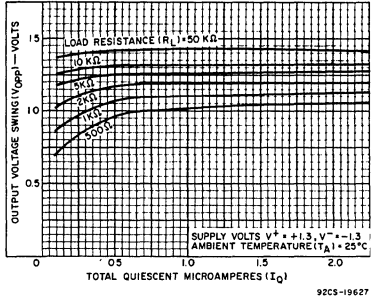


Fig. 9 - Output voltage swing vs. total quiescent current.

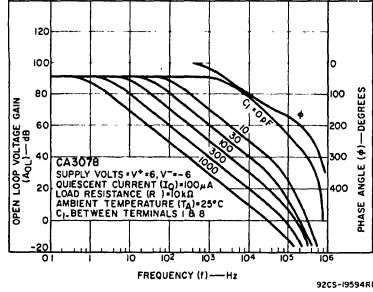


Fig. 10 - Open-loop voltage gain vs. frequency for  $I_Q = 100 \mu A$  - CA3078.

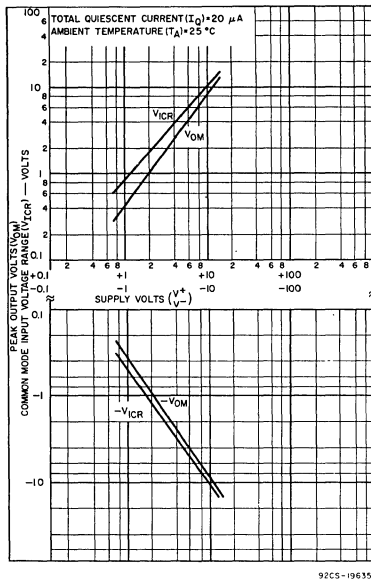


Fig. 11 - Output and common-mode voltage vs. supply voltage.

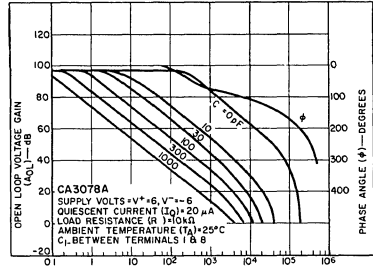


Fig. 12 - Open-loop voltage gain vs. frequency for  $I_Q = 20 \mu A$  - CA3078A.

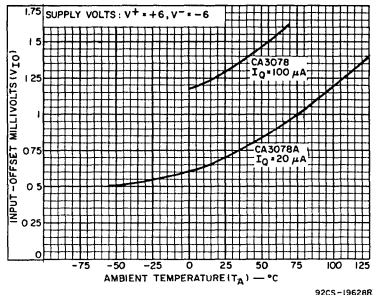


Fig. 13 - Input offset voltage vs. temperature.

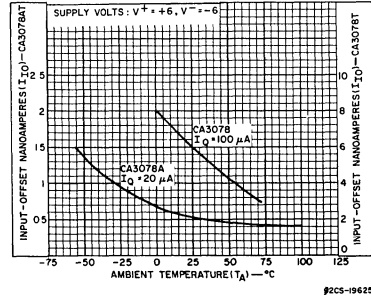


Fig. 14 - Input offset current vs. temperature.

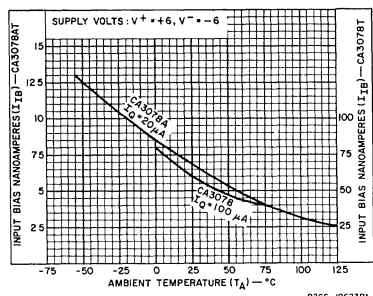


Fig. 15 - Input bias current vs. temperature.

# CA3078, CA3078A

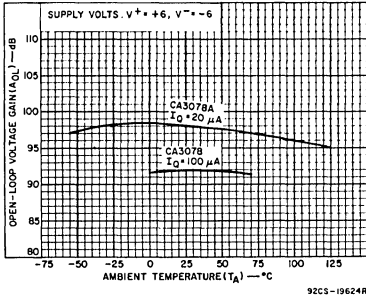


Fig. 16 - Open-loop voltage gain vs. temperature.

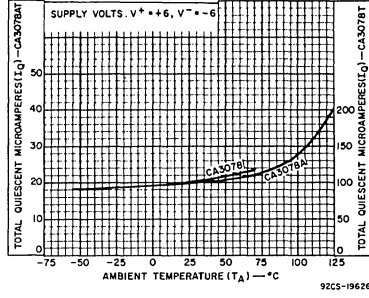


Fig. 17 - Total quiescent current vs. temperature.

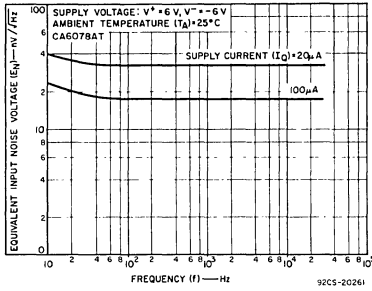


Fig. 18 - Equivalent input noise voltage vs. frequency.

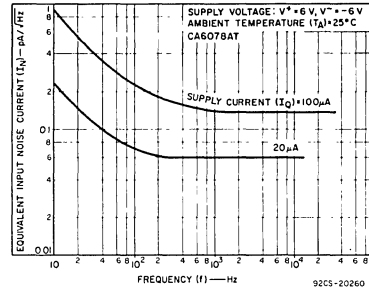


Fig. 19 - Equivalent input noise current vs. frequency.

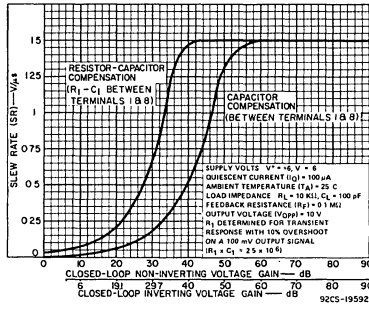


Fig. 20 - Slew rate vs. closed-loop gain for  $I_Q = 100 \mu A$  - CA3078.

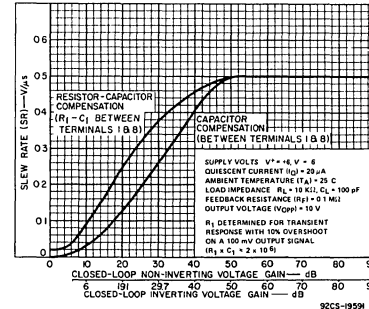


Fig. 21 - Slew rate vs. closed-loop gain for  $I_Q = 20 \mu A$  - CA3078.

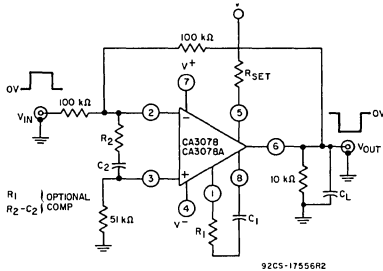


Fig. 22 - Transient response and slew-rate, unity gain (inverting) test circuit.

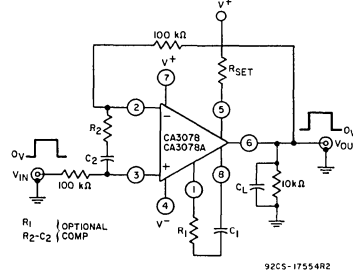


Fig. 23 - Slew-rate, unity gain (non-inverting) test circuit.

3  
OPERATIONAL AMPLIFIERS

## CA3078, CA3078A

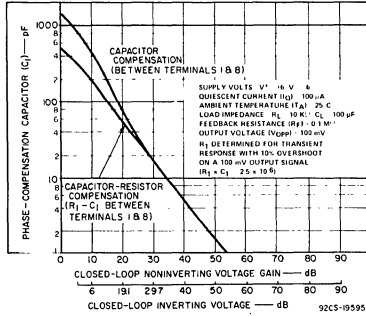


Fig. 24 — Phase compensation capacitance vs. closed-loop gain — CA3078.

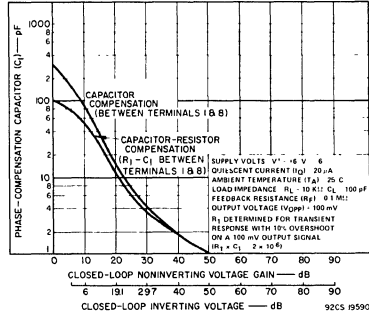


Fig. 25 — Phase compensation capacitance vs. closed-loop gain — CA3078A.

Table 1 — Unity-gain slew rate vs. compensation — CA3078 and CA3078A

| SUPPLY VOLTS: $V^+ = 6$ , $V^- = -6$      |                                   | TRANSIENT RESPONSE: 10% OVERSHOOT FOR AN OUTPUT VOLTAGE OF 100 mV |          |       |           |                                       | AMBIENT TEMPERATURE ( $T_A$ ) = 25°C |          |      |           |  |
|---|-----------------------------------|---|----------|-------|-----------|---------------------------------------|--------------------------------------|----------|------|-----------|--|
| OUTPUT VOLTAGE ( $V_O$ ) = $\pm 5$ V      |                                   |   |          |       |           |                                       |                                      |          |      |           |  |
| LOAD RESISTANCE ( $R_L$ ) = 10 k $\Omega$ |                                   |   |          |       |           |                                       |                                      |          |      |           |  |
| COMPENSATION TECHNIQUE                    | UNITY GAIN (INVERTING)<br>Fig. 22 |   |          |       |           | UNITY GAIN (NON-INVERTING)<br>Fig. 23 |                                      |          |      |           |  |
|   | R1                                | C1  | R2       | C2    | SLEW RATE | R1                                    | C1                                   | R2       | C2   | SLEW RATE |  |
| CA3078 — $I_Q = 100 \mu$ A                |                                   |   |          |       |           |                                       |                                      |          |      |           |  |
| Single Capacitor                          | 0                                 | 750   | $\infty$ | 0     | 0.0085    | 0                                     | 1500                                 | $\infty$ | 0    | 0.0095    |  |
| Resistor & Capacitor                      | 3.5                               | 350   | $\infty$ | 0     | 0.04      | 5.3                                   | 500                                  | $\infty$ | 0    | 0.024     |  |
| Input                                     | $\infty$                          | 0   | 0.25     | 0.306 | 0.67      | $\infty$                              | 0                                    | 0.311    | 0.45 | 0.67      |  |
| CA3078A — $I_Q = 20 \mu$ A                |                                   |   |          |       |           |                                       |                                      |          |      |           |  |
| Single Capacitor                          | 0                                 | 300   | $\infty$ | 0     | 0.0095    | 0                                     | 800                                  | $\infty$ | 0    | 0.003     |  |
| Resistor & Capacitor                      | 14                                | 100   | $\infty$ | 0     | 0.027     | 34                                    | 125                                  | $\infty$ | 0    | 0.02      |  |
| Input                                     | $\infty$                          | 0   | 0.644    | 0.156 | 0.29      | $\infty$                              | 0                                    | 0.77     | 0.4  | 0.4       |  |

### OPERATING CONSIDERATIONS

#### Compensation Techniques

The CA3078A and CA3078 can be phase-compensated with one or two external components depending upon the closed-loop gain, power consumption, and speed desired. The recommended compensation is a resistor in series with a capacitor connected from terminal 1 to terminal 8. Values of the resistor and capacitor required for compensation as a function of closed loop gain are shown in Figs. 24 and 25. These curves represent the compensation necessary at quiescent currents of 100  $\mu$ A and 20  $\mu$ A, respectively, for a transient response with 10% overshoot. Figs. 20 and 21 show the slew rates that can be obtained with the two different compensation tech-

niques. Higher speeds can be achieved with input compensation, but this increases noise output. Compensation can also be accomplished with a single capacitor connected from terminal 1 to terminal 8, with speed being sacrificed for simplicity. Table 1 gives an indication of slew rates that can be obtained with various compensation techniques at quiescent currents of 100  $\mu$ A and 20  $\mu$ A.

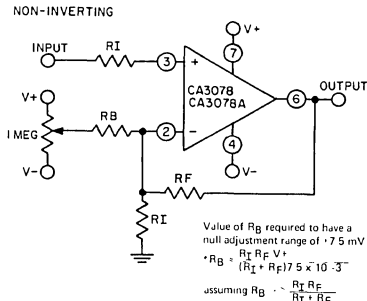
#### Single Supply Operation

The CA3078A and CA3078 can operate from a single supply with a minimum total supply voltage of 1.5 volts. Figs. 27 and 28 show the CA3078A or CA3078 in inverting the non-inverting 20-dB amplifier configurations utilizing a 1.5-volt type "AA" cell for a supply. The total power consumption for

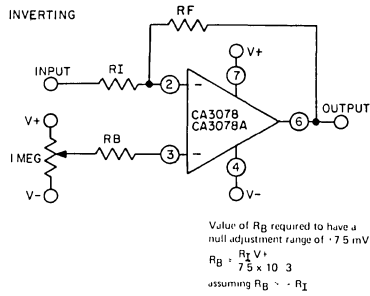
## CA3078, CA3078A

either circuit is approximately 675 nano-watts. The output voltage swing in this

configuration is 300 mV p-p with a 20 kΩ load.



92CS-20812R2



92CS-20813R2

Fig. 26 — Offset voltage null circuits.

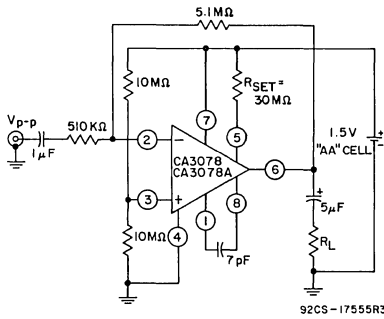


Fig. 27 — Inverting 20-dB amplifier circuit.

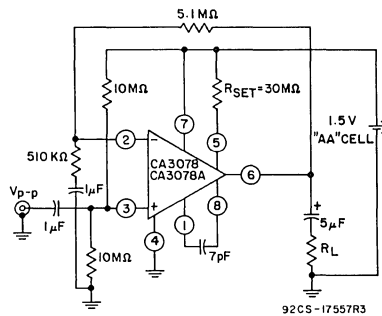


Fig. 28 — Non inverting 20-dB amplifier circuit.



August 1991

### Features

- Slow Rate (Unity Gain, Compensated) ..... 50V/μs
- Adjustable Power Consumption ... 10μW to 30mW
- Flexible Supply Voltage Range ..... ±2V to ±15V
- Fully Adjustable Gain ..... 0 to  $g_m R_L$  limit
- Tight  $g_m$  Spread
  - ▶ CA3080 ..... 2:1
  - ▶ CA3080A ..... 1.6:1
- Extended  $g_m$  Linearity ..... 3 decades

### Applications

- Sample and Hold
- Multiplex
- Voltage Follower
- Multiplier
- Comparator

### Description

The CA3080 and CA3080A types are Gatable-Gain Blocks which utilize the unique operational-transconductance-amplifier (OTA) concept described in Application Note ICAN-6668, "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

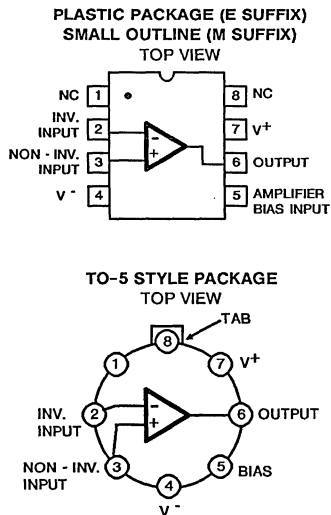
The CA3080 and CA3080A types have differential input and a single-ended, push-pull, class A output. In addition, these types have an amplifier bias input which may be used either for gating or for linear gain control. These types also have a high output impedance and their transconductance ( $g_m$ ) is directly proportional to the amplifier bias current ( $I_{ABC}$ ).

The CA3080 and CA3080A types are notable for their excellent slew rate (50V/μs), which makes them especially useful for multiplex and fast unity-gain voltage followers. These types are especially applicable for multiplex applications because power is consumed only when the devices are in the "ON" channel state.

The CA3080A is rated for operation over the full military-temperature range (-55 to +125°C) and its characteristics are specifically controlled for applications such as sample-and-hold, gain-control, multiplex, etc. Operational transconductance amplifiers are also useful in programmable power-switch applications, e.g., as described in Application Note ICAN-6048, "Some Applications of a Programmable Power Switch/Amplifier" (CA3094, CA3094A, CA3094B).

These types are supplied in the 8 lead Small Outline package (CA3080M, CA3080AM), the 8 lead TO-5-style package (CA3080, CA3080A), and in the 8 lead TO-5-style package with dual-in-line formed leads ("DIL-CAN", CA3080S, CA3080AS). The CA3080 is also supplied in the 8 lead dual-in-line plastic ("MINI-DIP") package (CA3080E, CA3080AE), and in chip form (CA3080H).

### Pinouts



NOTE: Pin 4 is connected to case.

FIGURE 1

### Schematic Diagram

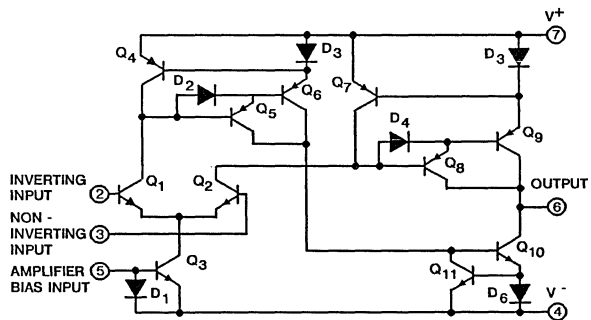


FIGURE 2 SCHEMATIC DIAGRAM FOR CA3080 AND CA3080A.

## CA3080, CA3080A

### ELECTRICAL CHARACTERISTICS For Equipment Design

| CHARACTERISTIC                             |                            | TEST CONDITIONS   | CA3080, CA3080E<br>CA3080M, CA3080S<br>LIMITS |               |       | UNITS            |
|--|----------------------------|---|---|---------------|-------|------------------|
|  |                            | $V^+ = 15\text{ V}, V^- = -15\text{ V}$<br>$I_{ABC} = 500\text{ }\mu\text{A}$<br>$T_A = 25^\circ\text{C}$<br>(unless indicated otherwise) | Min.  | Typ.          | Max.  |                  |
| Input Offset Voltage                       | $V_{IO}$                   | $T_A = 0\text{ to }70^\circ\text{C}$  | –   | 0.4           | 5     | mV               |
| Input Offset Current                       | $I_{IO}$                   |   | –   | 0.12          | 0.6   | $\mu\text{A}$    |
| Input Bias Current                         | $I_I$                      | $T_A = 0\text{ to }70^\circ\text{C}$  | –   | 2             | 5     | $\mu\text{A}$    |
| Forward Transconductance<br>(large signal) | $g_m$                      |   | 6700  | 9600          | 13000 | $\mu\text{mho}$  |
|  |                            | $T_A = 0\text{ to }70^\circ\text{C}$  | 5400  | –             | –     |                  |
| Peak Output Current                        | $ I_{OM} $                 | $R_L = 0$   | 350   | 500           | 650   | $\mu\text{A}$    |
|  |                            | $R_L = 0, T_A = 0\text{ to }70^\circ\text{C}$   | 300   | –             | –     |                  |
| Peak Output Voltage:                       |                            | $R_L = \infty$  |   |               |       | V                |
| Positive                                   | $V^{+OM}$                  |   | 12  | 13.5          | –     |                  |
| Negative                                   | $V^{-OM}$                  | –12   | –14.4   | –             |       |                  |
| Amplifier Supply Current                   | $I_A$                      |   | 0.8   | 1             | 1.2   | mA               |
| Device Dissipation                         | $P_D$                      |   | 24  | 30            | 36    | mW               |
| Input Offset Voltage Sensitivity:          |                            |   |   |               |       | $\mu\text{V/V}$  |
| Positive                                   | $\Delta V_{IO}/\Delta V^+$ |   | –   | –             | 150   |                  |
| Negative                                   | $\Delta V_{IO}/\Delta V^-$ |   | –   | –             | 150   |                  |
| Common-Mode Rejection Ratio                | CMRR                       |   | 80  | 110           | –     | dB               |
| Common-Mode Input-Voltage Range            | $V_{ICR}$                  |   | 12 to –12                                     | 13.6 to –14.6 | –     | V                |
| Input Resistance                           | $R_I$                      |   | 10  | 26            | –     | $\text{k}\Omega$ |

### ELECTRICAL CHARACTERISTICS Typical Values Intended Only for Design Guidance

CA3080, CA3080E  
CA3080M, CA3080S

|                              |                    |   |       |                        |
|------------------------------|--------------------|---|-------|------------------------|
| Input Offset Voltage         | $V_{IO}$           | $I_{ABC} = 5\text{ }\mu\text{A}$  | 0.3   | mV                     |
| Input Offset Voltage Change  | $ \Delta V_{IO} $  | $I_{ABC} = 500\text{ }\mu\text{A}$ to<br>$I_{ABC} = 5\text{ }\mu\text{A}$ | 0.2   | mV                     |
| Peak Output Current          | $I_{OM}$           | $I_{ABC} = 5\text{ }\mu\text{A}$  | 5     | $\mu\text{A}$          |
| Peak Output Voltage:         |                    | $I_{ABC} = 5\text{ }\mu\text{A}$  |       | V                      |
| Positive                     | $V^{+OM}$          |   | 13.8  |                        |
| Negative                     | $V^{-OM}$          | –14.5   |       |                        |
| Magnitude of Leakage Current |                    | $I_{ABC} = 0, V_{TP} = 0$   | 0.08  | nA                     |
|                              |                    | $I_{ABC} = 0, V_{TP} = 36\text{ V}$                                       | 0.3   |                        |
| Differential Input Current   |                    | $I_{ABC} = 0, V_{DIFF} = 4\text{ V}$                                      | 0.008 | nA                     |
| Amplifier Bias Voltage       | $V_{ABC}$          |   | 0.71  | V                      |
| Slew Rate:                   |                    |   |       | $\text{V}/\mu\text{s}$ |
| Maximum (uncompensated)      | $SR$               |   | 75    |                        |
| Unity Gain (compensated)     |                    |   | 50    |                        |
| Open-Loop Bandwidth          | $BW_{OL}$          |   | 2     | MHz                    |
| Input Capacitance            | $C_I$              | $f = 1\text{ MHz}$  | 3.6   | pF                     |
| Output Capacitance           | $C_O$              | $f = 1\text{ MHz}$  | 5.6   | pF                     |
| Output Resistance            | $R_O$              |   | 15    | $\text{M}\Omega$       |
| Input-to-Output Capacitance  | $C_{I-O}$          | $f = 1\text{ MHz}$  | 0.024 | pF                     |
| Propagation Delay            | $t_{PHL}, t_{PLH}$ | $I_{ABC} = 500\text{ }\mu\text{A}$  | 45    | ns                     |

## CA3080, CA3080A

### ELECTRICAL CHARACTERISTICS For Equipment Design

| CHARACTERISTIC                             |                             | TEST CONDITIONS   | CA3080, CA3080AE<br>CA3080AM,<br>CA3080AS<br>LIMITS |                  |       | UNITS           |
|--|-----------------------------|---|---|------------------|-------|-----------------|
|  |                             | $V^+ = 15\text{ V}, V^- = -15\text{ V}$<br>$I_{ABC} = 500\ \mu\text{A}$<br>$T_A = 25^\circ\text{C}$<br>(unless indicated otherwise) | Min.  | Typ.             | Max.  |                 |
| Input Offset Voltage                       | $V_{IO}$                    | $I_{ABC} = 5\ \mu\text{A}$  | —   | 0.3              | 2     | mV              |
|  |                             | $T_A = -55\text{ to }+125^\circ\text{C}$  | —   | 0.4              | 2     |                 |
| Input Offset Voltage Change                | $ \Delta V_{IO} $           | $I_{ABC} = 500\ \mu\text{A}$ to<br>$I_{ABC} = 5\ \mu\text{A}$   | —   | 0.1              | 3     | mV              |
| Input Offset Current                       | $I_{IO}$                    |   | —   | 0.12             | 0.6   | $\mu\text{A}$   |
| Input Bias Current                         | $I_I$                       |   | —   | 2                | 5     | $\mu\text{A}$   |
|  |                             | $T_A = -55\text{ to }+125^\circ\text{C}$  | —   | —                | 15    |                 |
| Forward Transconductance<br>(large signal) | $g_m$                       |   | 7700  | 9600             | 12000 | $\mu\text{mho}$ |
|  |                             | $T_A = -55\text{ to }+125^\circ\text{C}$  | 4000  | —                | —     |                 |
| Peak Output Current                        | $ I_{OM} $                  | $I_{ABC} = 5\ \mu\text{A}, R_L = 0$   | 3   | 5                | 7     | $\mu\text{A}$   |
|  |                             | $R_L = 0$   | 350   | 500              | 650   |                 |
|  |                             | $R_L = 0, T_A = -55\text{ to }+125^\circ\text{C}$   | 300   | —                | —     |                 |
| Peak Output Voltage:                       |                             |   |   |                  |       |                 |
| Positive                                   | $V_{OM}^+$                  | $I_{ABC} = 5\ \mu\text{A}$  | 12  | 13.8             | —     | V               |
| Negative                                   | $V_{OM}^-$                  | $R_L = \infty$  | -12   | -14.5            | —     |                 |
| Positive                                   | $V_{OM}^+$                  | $R_L = \infty$  | 12  | 13.5             | —     |                 |
| Negative                                   | $V_{OM}^-$                  |   | -12   | -14.4            | —     |                 |
| Amplifier Supply Current                   | $I_A$                       |   | 0.8   | 1                | 1.2   | mA              |
| Device Dissipation                         | $P_D$                       |   | 24  | 30               | 36    | mW              |
| Input Offset Voltage Sensitivity:          |                             |   |   |                  |       |                 |
| Positive                                   | $ \Delta V_{IO}/\Delta V^+$ |   | —   | —                | 150   | $\mu\text{V/V}$ |
| Negative                                   | $ \Delta V_{IO}/\Delta V^-$ |   | —   | —                | 150   |                 |
| Magnitude of Leakage Current               |                             | $I_{ABC} = 0, V_{TP} = 0$   | —   | 0.08             | 5     | nA              |
|  |                             | $I_{ABC} = 0, V_{TP} = 36\text{ V}$   | —   | 0.3              | 5     |                 |
| Differential Input Current                 |                             | $I_{ABC} = 0, V_{DIFF} = 4\text{ V}$  | —   | 0.008            | 5     | nA              |
| Common-Mode Rejection Ratio                | CMRR                        |   | 80  | 110              | —     | dB              |
| Common-Mode Input-Voltage Range            | $V_{ICR}$                   |   | 12 to<br>-12  | 13.6 to<br>-14.6 | —     | V               |
| Input Resistance                           | $R_I$                       |   | 10  | 26               | —     | k $\Omega$      |

### ELECTRICAL CHARACTERISTICS Typical Values Intended Only for Design Guidance

### CA3080, CA3080AE CA3080AM, CA3080AS

|   |                          |   |       |                              |
|---|--------------------------|---|-------|------------------------------|
| Amplifier Bias Voltage                    | $V_{ABC}$                |   | 0.71  | V                            |
| Slew Rate:                                |                          |   |       |                              |
| Maximum (uncompensated)                   | SR                       |   | 75    | V/ $\mu\text{s}$             |
| Unity Gain (compensated)                  |                          |   | 50    |                              |
| Open-Loop Bandwidth                       | BW <sub>OL</sub>         | —   | 2     | MHz                          |
| Input Capacitance                         | $C_I$                    | f = 1 MHz   | 3.6   | pF                           |
| Output Capacitance                        | $C_O$                    | f = 1 MHz   | 5.6   | pF                           |
| Output Resistance                         | $R_O$                    |   | .15   | M $\Omega$                   |
| Input-to-Output Capacitance               | $C_{I-O}$                | f = 1 MHz   | 0.024 | pF                           |
| Input Offset Voltage<br>Temperature Drift | $\Delta V_{IO}/\Delta T$ | $I_{ABC} = 100\ \mu\text{A},$<br>$T_A = -55\text{ to }+125^\circ\text{C}$ | 3     | $\mu\text{V}/^\circ\text{C}$ |
| Propagation Delay                         | $t_{PHL}, t_{PLH}$       | $I_{ABC} = 500\ \mu\text{A}$  | 45    | ns                           |

# CA3080, CA3080A

## MAXIMUM RATINGS, Absolute-Maximum Values:

|   |                |
|---|----------------|
| DC SUPPLY VOLTAGE (Between $V^+$ and $V^-$ terminals) | 36 V           |
| DIFFERENTIAL INPUT VOLTAGE                            | $\pm 5$ V      |
| DC INPUT VOLTAGE                                      | $V^+$ to $V^-$ |
| INPUT SIGNAL CURRENT                                  | 1 mA           |
| AMPLIFIER BIAS CURRENT                                | 2 mA           |
| OUTPUT SHORT-CIRCUIT DURATION*                        | Indefinite     |
| DEVICE DISSIPATION                                    | 125 mW         |
| TEMPERATURE RANGE:                                    |                |
| Operating   |                |
| CA3080, CA3080E, CA3080M, CA3080S                     | 0 to +70 °C    |
| CA3080A, CA3080AE, CA3080AM, CA3080AS                 | -55 to +125 °C |
| Storage   | -65 to +150 °C |
| LEAD TEMPERATURE (During Soldering):                  |                |
| At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm)          |                |
| from case for 10 s max.                               | +265 °C        |

\* Short circuit may be applied to ground or to either supply.

## TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS FOR THE CA3080 AND CA3080A

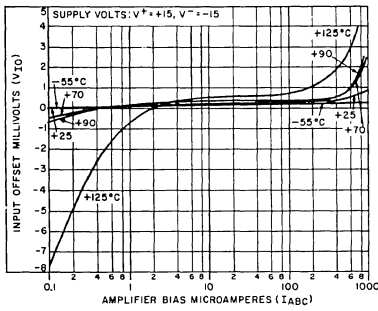


Fig. 3 - Input offset voltage as a function of amplifier bias current.

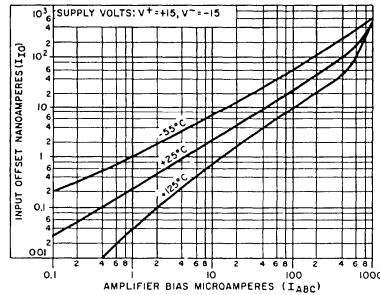


Fig. 4 - Input offset current as a function of amplifier bias current.

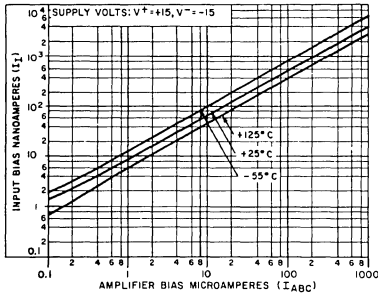


Fig. 5 - Input bias current as a function of amplifier bias current.

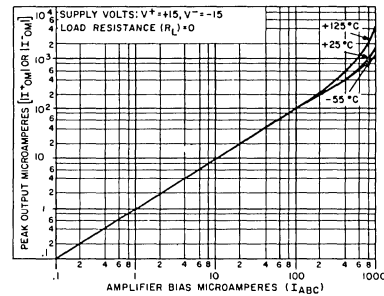


Fig. 6 - Peak output current as a function of amplifier bias current.

# CA3080, CA3080A

## TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS (Cont'd)

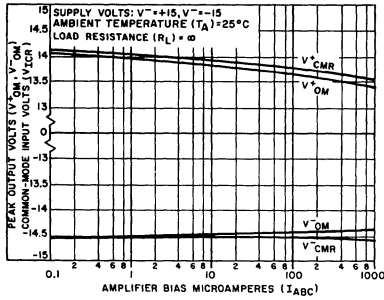


Fig. 7 - Peak output voltage as a function of amplifier bias current.

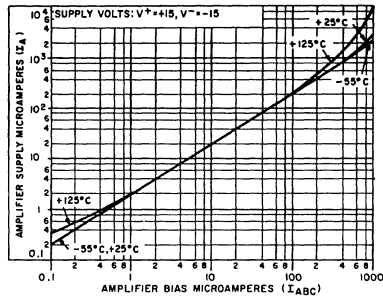


Fig. 8 - Amplifier supply current as a function of amplifier bias current.

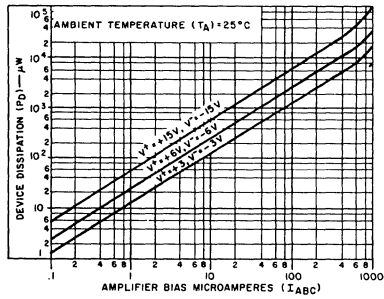


Fig. 9 - Total power dissipation as a function of amplifier bias current.

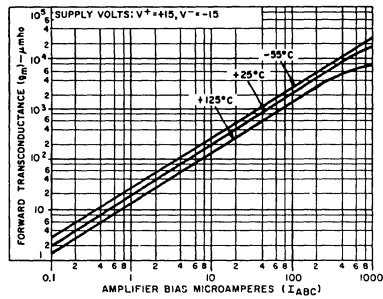


Fig. 10 - Transconductance as a function of amplifier bias current.

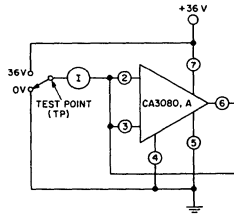


Fig. 11 - Leakage current test circuit.

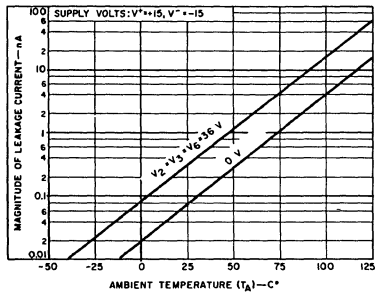


Fig. 12 - Leakage current as a function of temperature.

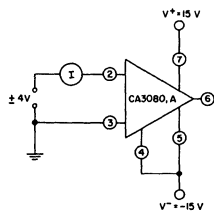


Fig. 13 - Differential input current test circuit.

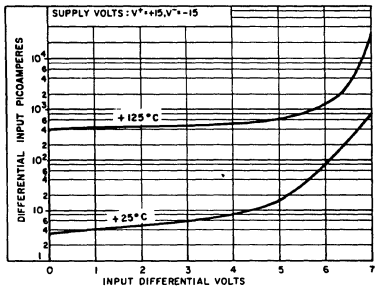


Fig. 14 - Input current as a function of input differential voltage.

# CA3080, CA3080A

## TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS (Cont'd)

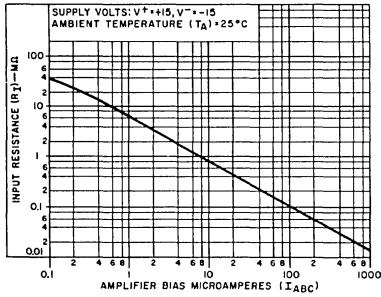


Fig. 15 - Input resistance as a function of amplifier bias current.

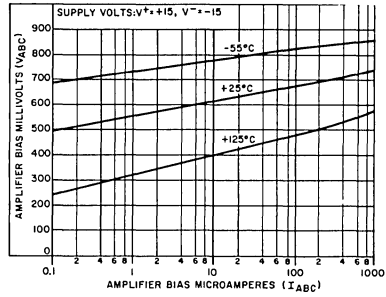


Fig. 16 - Amplifier bias voltage as a function of amplifier bias current.

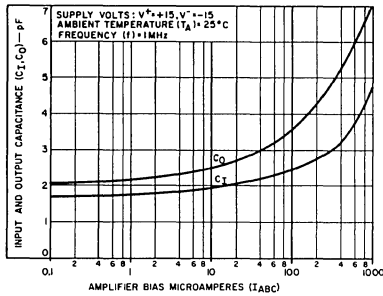


Fig. 17 - Input and output capacitance as a function of amplifier bias current.

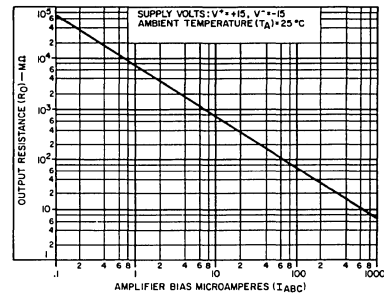


Fig. 18 - Output resistance as a function of amplifier bias current.

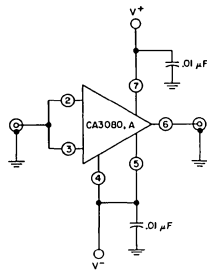


Fig. 19 - Input-to-output capacitance test circuit.

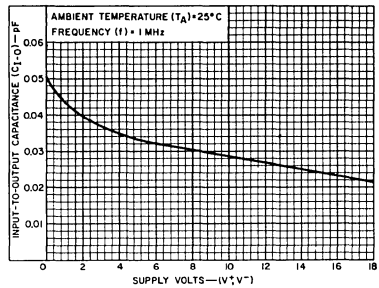


Fig. 20 - Input-to-output capacitance as a function of supply voltage.

## APPLICATIONS

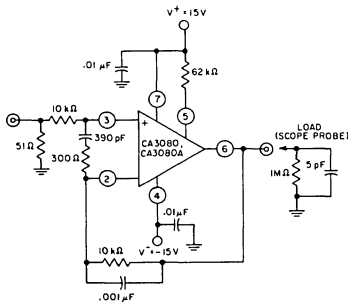
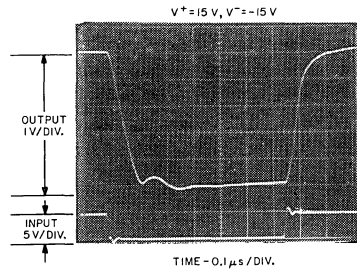


Fig. 21 - Schematic diagram of the CA3080 and CA3080A in a unity-gain voltage follower configuration and associated waveform.



3  
OPERATIONAL  
AMPLIFIERS

# CA3080, CA3080A

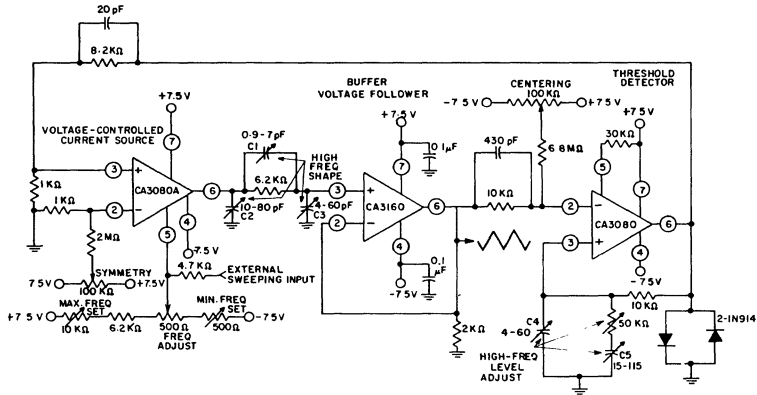
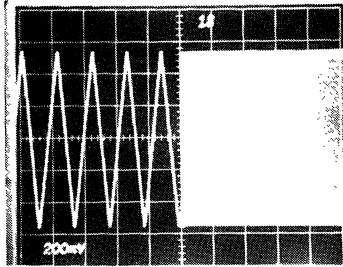
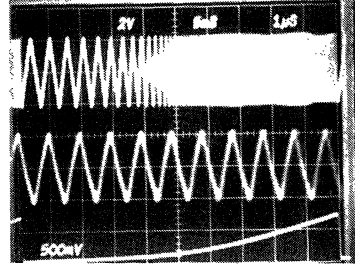


Fig.22 – 1,000,000/1 single-control function generator – 1 MHz to 1 Hz.



(a) – Two-tone output signal from the function generator. A square-wave signal modulates the external sweeping input to produce 1 Hz and 1 MHz, showing the 1,000,000/1 frequency range of the function generator.



(b) – Triple-trace of the function generator sweeping to 1 MHz. The bottom trace is the sweeping signal and the top trace is the actual generator output. The center trace displays the 1 MHz signal via delayed oscilloscope triggering of the upper swept output signal.

Fig.23 – Function generator dynamic characteristics waveforms.

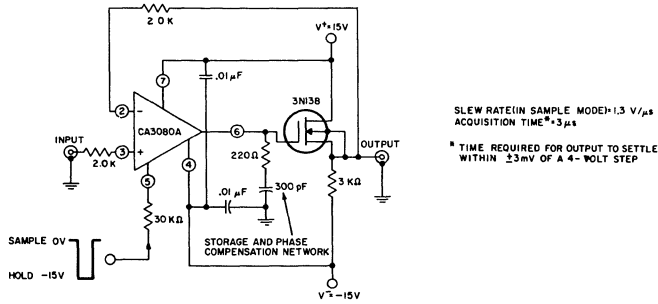


Fig.24 – Schematic diagram of the CA3080A in a sample-and-hold configuration.

# CA3080, CA3080A

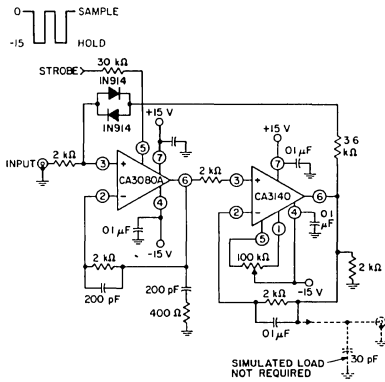
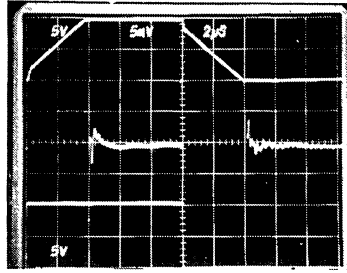
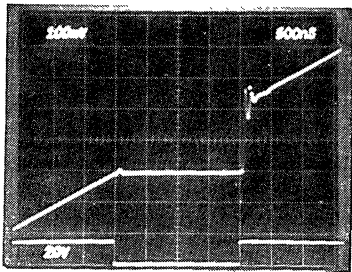


Fig.25 – Sample- and hold circuit.



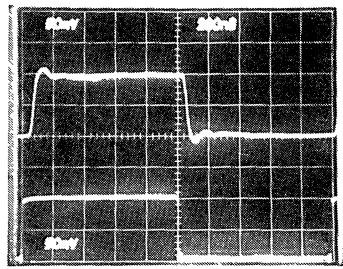
**LARGE-SIGNAL RESPONSE AND SETTLING TIME**  
 TOP TRACE: OUTPUT SIGNAL  
 (5 V/DIV AND 2 μs/DIV.)  
 BOTTOM TRACE: INPUT SIGNAL  
 (5 V/DIV. AND 2 μs/DIV.)  
 CENTER TRACE DIFFERENCE OF INPUT AND OUTPUT SIGNALS THROUGH TEKTRONIX AMPLIFIER 7A13  
 (5 mV/DIV AND 2 μs/DIV.)

Fig.26 – Large-signal response and settling time for circuit shown in Fig.25.



**SAMPLING RESPONSE**  
 TOP TRACE: SYSTEM OUTPUT  
 (100 mV/DIV AND 500 ns/DIV.)  
 BOTTOM TRACE: SAMPLING SIGNAL  
 (20 V/DIV AND 500 ns/DIV.)

Fig.27 – Sampling response for circuit shown in Fig. 25.



TOP TRACE: OUTPUT  
 (50 mV/DIV. AND 200 ns/DIV.)  
 BOTTOM TRACE: INPUT  
 (50 mV/DIV AND 200 ns/DIV.)

Fig.28 – Input and output response for circuit shown in Fig. 25.

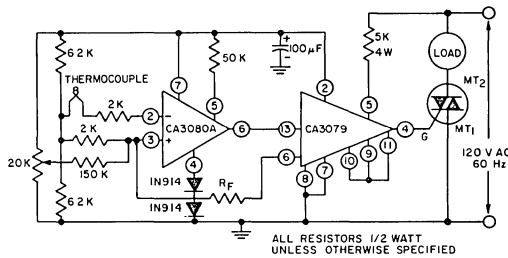


Fig.29 – Thermocouple temperature control with CA3079 zero voltage switch as the output amplifier.



# CA3080, CA3080A

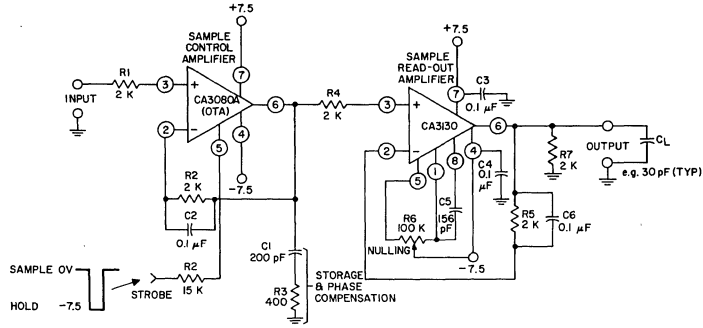
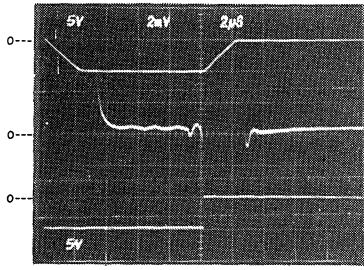
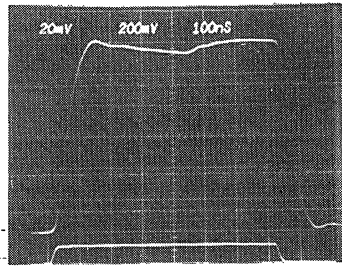


Fig.30 – Schematic diagram of the CA3080A in a sample-and-hold circuit with BiMOS output amplifier.



TOP TRACE: OUTPUT—5 V/DIV. & 2 μs/DIV.  
 CENTER TRACE: DIFFERENTIAL COMPARISON OF  
 INPUT & OUTPUT—2 mV/DIV. & 2 μs/DIV  
 BOTTOM TRACE: INPUT—5 V/DIV. & 2 μs/DIV

Fig.31 – Large-signal response for circuit shown in Fig. 30.



TOP TRACE: OUTPUT—20 mV/DIV. & 100 ns/DIV.  
 BOTTOM TRACE: INPUT—200 mV/DIV. & 100 ns/DIV.

Fig.32 – Small-signal response for circuit shown in Fig. 30.

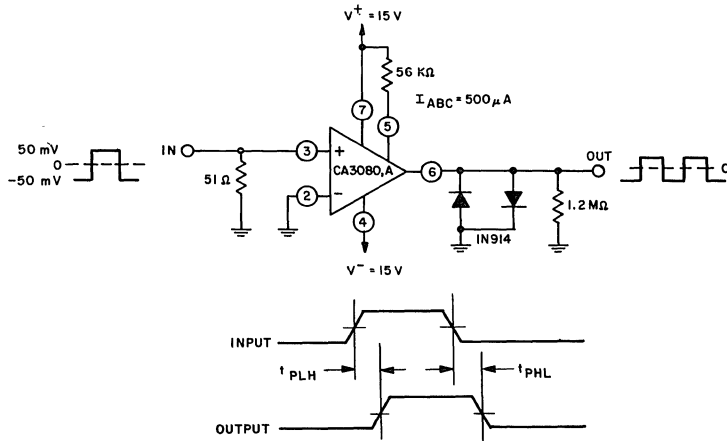


Fig. 33 – Propagation delay test circuit and associated waveforms.

# CA3094, CA3094A CA3094B

## Programmable Power Switch/Amplifier for Control & General-Purpose Applications

August 1991

### Features

- CA3094T, S, E, M ..... for Operation Up to 24V
- CA3094AT, S, E, M ..... for Operation Up to 36V
- CA3094BT, S, M ..... for Operation Up to 44V
- Designed for Single or Dual Power Supply
- Programmable: Strobing, Gating, Squelching, AGC Capabilities
- Can Deliver 3 Watts (Avg.) or 10W (Peak) to External Load (In Switching Mode)
- High-Power, Single-Ended Class A Amplifier Will Deliver Power Output of 0.6 Watt (1.6W Device Dissipation)
- Total Harmonic Distortion (THD) @ 0.6W In Class A Operation ..... 1.4% (Typ.)

### Applications

- Error-Signal Detector: Temperature Control with Thermistor Sensor; Speed Control for Shunt Wound DC Motor
- Over-Current, Over-Voltage, Over-Temperature Protectors
- Dual-Tracking Power Supply with CA3085
- Wide-Frequency-Range Oscillator
- Analog Timer
- Level Detector
- Alarm Systems
- Voltage Follower
- Ramp-Voltage Generator
- High-Power Comparator
- Ground-Fault Interrupter (GFI) Circuits

### Description

The CA3094 is a differential-input power-control switch/amplifier with auxiliary circuit features for ease of programmability. For example, an error or unbalance signal can be amplified by the CA3094 to provide an on-off signal or proportional-control output signal up to 100mA. This signal is sufficient to directly drive high-current thyristors, relays, dc loads, or power transistors. The CA3094 has the generic characteristics of the CA3080 operational amplifier directly coupled to an integral Darlington power transistor capable of sinking or driving currents up to 100mA.

The gain of the differential input stage is proportional to the amplifier bias current (I<sub>ABC</sub>), permitting programmable variation of the integrated circuit sensitivity with either digital and/or analog programming signals. For example, at an I<sub>ABC</sub> of 100 mA, a one-millivolt change at the input will change the output from 0 to 100 mA (typical).

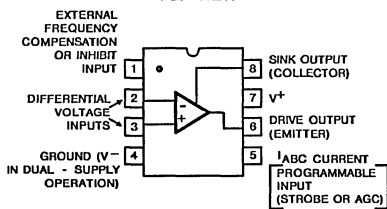
The CA3094 is intended for operation up to 24 volts and is especially useful for timing circuits, in automotive equipment, and in other applications where operation up to 24 volts is a primary design requirement (see Figs. 28, 29 and 30 in Applications Section). The CA3094A and CA3094B are like the CA3094 but are intended for operation up to 36 and 44 volts, respectively (single or dual supply).

These types are available in 8-lead TO-5 style packages with standard leads ("T" suffix) and with dual-in-line formed leads "DIL-CAN" ("S" suffix). Type CA3094 is also available in an 8-lead dual-in-line plastic package "MINI-DIP" ("E" suffix), Small Outline Package (M suffix), and in chip form ("H" suffix).

3  
OPERATIONAL AMPLIFIERS

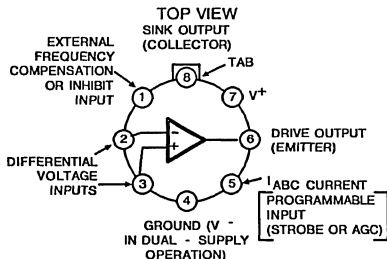
### Pinouts

#### PLASTIC AND SMALL OUTLINE PACKAGE TOP VIEW

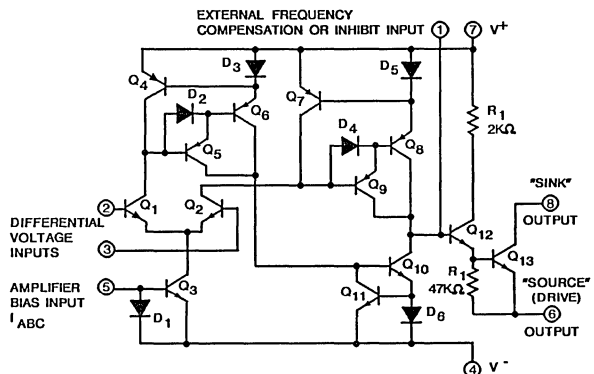


NOTE: Pin 4 is Connected to Case.

#### TO-5 STYLE PACKAGE TOP VIEW



### Schematic Diagram



| OUTPUT MODE | OUTPUT TERM | INPUTS |         |
|-------------|-------------|--------|---------|
|             |             | INV    | NON-INV |
| "Source"    | 6           | 2      | 3       |
| "Sink"      | 8           | 3      | 2       |

FIGURE 1. SCHEMATIC DIAGRAM OF CA3094

**CA3094, CA3094A, CA3094B**

**ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$  For Equipment Design**

| CHARACTERISTIC   | TEST CONDITIONS   |  | LIMITS |       |      | UNITS                           |
|--|---|--|--------|-------|------|---------------------------------|
|  | Single Supply $V^+ = 30\text{ V}$<br>Dual Supply $V^+ = 15\text{ V}$ ,<br>$V^- = 15\text{ V}$<br>$I_{ABC} = 100\ \mu\text{A}$<br>Unless Otherwise Specified |  | Min.   | Typ.  | Max. |                                 |
| <b>INPUT PARAMETERS</b>  |   |  |        |       |      |                                 |
| Input Offset Voltage $V_{IO}$  | $T_A = 25^\circ\text{C}$  |  | –      | 0.4   | 5    | mV                              |
|  | $T_A = 0\text{ to }70^\circ\text{C}$  |  | –      | –     | 7    | mV                              |
| Input-Offset-Voltage Change $ \Delta V_{IO} $                            | Change in $V_{IO}$<br>Between $I_{ABC} = 100\ \mu\text{A}$<br>and $I_{ABC} = 5\ \mu\text{A}$  |  | –      | 1     | 8    | mV                              |
| Input Offset Current $I_{IO}$  | $T_A = 25^\circ\text{C}$  |  | –      | 0.02  | 0.2  | $\mu\text{A}$                   |
|  | $T_A = 0\text{ to }70^\circ\text{C}$  |  | –      | –     | 0.3  | $\mu\text{A}$                   |
| Input Bias Current $I_I$   | $T_A = 25^\circ\text{C}$  |  | –      | 0.2   | 0.50 | $\mu\text{A}$                   |
|  | $T_A = 0\text{ to }70^\circ\text{C}$  |  | –      | –     | 0.70 | $\mu\text{A}$                   |
| Device Dissipation $P_D$   | $I_{out} = 0$   |  | 8      | 10    | 12   | mW                              |
| Common-Mode Rejection Ratio $CMRR$                                       |   |  | 70     | 110   | –    | dB                              |
| Common-Mode Input–<br>Voltage Range $V_{ICR}$                            | $V^+ = 30\text{ V}$ High  |  | 27     | 28.8  | –    | V                               |
|  | $V^+ = 30\text{ V}$ Low   |  | 1.0    | 0.5   | –    | V                               |
|  | $V^+ = 15\text{ V}$   |  | +12    | +13.8 | –    | V                               |
|  | $V^- = 15\text{ V}$   |  | –14    | –14.5 | –    | V                               |
| Unity Gain-Bandwidth   | $I_C = 7.5\text{ mA}$<br>$V_{CE} = 15\text{ V}$<br>$I_{ABC} = 500\ \mu\text{A}$   |  | –      | 30    | –    | MHz                             |
| Open-Loop Bandwidth<br>At –3 dB Point $BW_{OL}$                          | $I_C = 7.5\text{ mA}$<br>$V_{CE} = 15\text{ V}$<br>$I_{ABC} = 500\ \mu\text{A}$   |  | –      | 4     | –    | kHz                             |
| Total Harmonic Distortion<br>(Class A Operation) $THD$                   | $P_D = 220\text{ mW}$   |  | –      | 0.4   | –    | %                               |
|  | $P_D = 600\text{ mW}$   |  | –      | 1.4   | –    | %                               |
| Amplifier Bias Voltage $V_{ABC}$<br>(Terminal (No.5 to Terminal No.4))   |   |  | –      | 0.68  | –    | V                               |
| Input Offset Voltage<br>Temperature Coefficient $\Delta V_{IO}/\Delta T$ |   |  | –      | 4     | –    | $\mu\text{V}/^\circ\text{C}$    |
| Power-Supply Rejection $\Delta V_{IO}/\Delta V$                          |   |  | –      | 15    | 150  | $\mu\text{V}/\text{V}$          |
| 1/F Noise Voltage $E_N$  | $f = 10\text{ Hz}$  |  | –      | 18    | –    | $\eta\sqrt{\text{V}/\text{Hz}}$ |
|  | $I_{ABC} = 50\ \mu\text{A}$   |  | –      | –     | –    |                                 |
| 1/F Noise Current $I_N$  | $f = 10\text{ Hz}$  |  | –      | 1.8   | –    | $\rho\text{A}/\sqrt{\text{Hz}}$ |
|  | $I_{ABC} = 50\ \mu\text{A}$   |  | –      | –     | –    |                                 |
| Differential Input Resistance $R_I$                                      | $I_{ABC} = 20\ \mu\text{A}$   |  | 0.50   | 1     | –    | $\text{M}\Omega$                |
| Differential Input Capacitance $C_I$                                     | $f = 1\text{ MHz}$<br>$V^+ = 30\text{ V}$   |  | –      | 2.6   | –    | pF                              |

CA3094, CA3094A, CA3094B

ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$  For Equipment Design

| CHARACTERISTIC  | TEST CONDITIONS  | LIMITS       |                 |             | UNITS                                |
|---|--|--------------|-----------------|-------------|--------------------------------------|
|   | Single Supply $V^+ = 30\text{ V}$<br>Dual Supply $V^+ = 15\text{ V}$ ,<br>$V^- = -15\text{ V}$<br>$I_{ABC} = 100\ \mu\text{A}$<br>Unless Otherwise Specified | Min.         | Typ.            | Max.        |                                      |
| <i>OUTPUT PARAMETERS (Differential Input Voltage = 1V)</i>                                  |  |              |                 |             |                                      |
| Peak Output Voltage:<br>(Terminal No. 6)<br>With Q13 "ON" $V^+OM$<br>With Q13 "OFF" $V^-OM$ | $V^+ = 30\text{ V}$<br>$R_L = 2\text{ k}\Omega$ to ground  | 26<br>–      | 27<br>0.01      | –<br>0.05   | V<br>V                               |
| Peak Output Voltage:<br>(Terminal No. 6)<br>Positive $V^+OM$<br>Negative $V^-OM$            | $V^+ = +15\text{ V}$ , $V^- = -15\text{ V}$<br>$R_L = 2\text{ k}\Omega$ to $-15\text{ V}$  | +11<br>–     | +12<br>–14.99   | –<br>–14.95 | V<br>V                               |
| Peak Output Voltage:<br>(Terminal No. 8)<br>With Q13 "ON" $V^+OM$<br>With Q13 "OFF" $V^-OM$ | $V^+ = 30\text{ V}$<br>$R_L = 2\text{ k}\Omega$ to $30\text{ V}$   | 29.95<br>–   | 29.99<br>0.040  | –<br>–      | V<br>V                               |
| Peak Output Voltage:<br>(Terminal No. 8)<br>Positive $V^+OM$<br>Negative $V^-OM$            | $V^+ = 15\text{ V}$ , $V^- = -15\text{ V}$<br>$R_L = 2\text{ k}\Omega$ to $+15\text{ V}$   | +14.95<br>–  | +14.99<br>14.96 | –<br>–      | V<br>V                               |
| Collector-to-Emitter Saturation Voltage<br>(Terminal No. 8) $V_{CE(sat)}$                   | $V^+ = 30\text{ V}$<br>$I_C = 50\text{ mA}$<br>Terminal No. 6 grounded   | –            | 0.17            | 0.80        | V                                    |
| Output Leakage Current<br>(Terminal No. 6 to Terminal No. 4)                                | $V^+ = 30\text{ V}$  | –            | 2               | 10          | $\mu\text{A}$                        |
| Composite Small-Signal Current Transfer Ratio (Beta) ( $Q_{12}$ and $Q_{13}$ ) $h_{fe}$     | $V^+ = 30\text{ V}$<br>$V_{CE} = 5\text{ V}$<br>$I_C = 50\text{ mA}$   | 16,000       | 100,000         | –           |                                      |
| Output Capacitance:<br>Terminal No. 6 $C_O$<br>Terminal No. 8                               | $f = 1\text{ MHz}$<br>All Remaining Terminals Tied to Terminal No. 4   | –<br>–       | 5.5<br>17       | –<br>–      | pF<br>pF                             |
| <i>TRANSFER PARAMETERS</i>  |  |              |                 |             |                                      |
| Voltage Gain A  | $V^+ = 30\text{ V}$<br>$I_{ABC} = 100\ \mu\text{A}$<br>$\Delta V_{out} = 20\text{ V}$<br>$R_L = 2\text{ k}\Omega$  | 20,000<br>86 | 100,000<br>100  | –<br>–      | V/V<br>dB                            |
| Forward Transconductance To Terminal No. 1 $g_m$  |  | 1650         | 2200            | 2750        | $\mu\text{mhos}$                     |
| Slew Rate:<br>Open Loop:<br>Positive Slope<br>Negative Slope                                | $I_{ABC} = 500\ \mu\text{A}$<br>$R_L = 2\text{ k}\Omega$   | –<br>–       | 500<br>50       | –<br>–      | V/ $\mu\text{s}$<br>V/ $\mu\text{s}$ |
| Unity Gain (Non-Inverting, Compensated)   | $I_{ABC} = 500\ \mu\text{A}$<br>$R_L = 2\text{ k}\Omega$   | –            | 0.7             | –           | V/ $\mu\text{s}$                     |

3  
OPERATIONAL AMPLIFIERS

# CA3094, CA3094A, CA3094B

## MAXIMUM RATINGS, Absolute-Maximum Values:

|   | CA3094                          | CA3094A | CA3094B |       |
|---|---------------------------------|---------|---------|-------|
| <b>DC SUPPLY VOLTAGE:</b>   |                                 |         |         |       |
| Dual Supply   | ± 12 V                          | ± 18 V  | ± 22 V  | V     |
| Single Supply   | 24 V                            | 36 V    | 44 V    | V     |
| <b>DC DIFFERENTIAL INPUT VOLTAGE</b><br>(Terminals 2 and 3)             |                                 |         |         |       |
|   | ± 5*                            |         |         | V     |
| <b>DC COMMON-MODE INPUT VOLTAGE</b>                                     |                                 |         |         |       |
|   | Term. 4 ≤ Term. 2 & 3 ≤ Term. 7 |         |         |       |
| <b>PEAK INPUT SIGNAL CURRENT</b><br>(Terminals 2 and 3)                 |                                 |         |         |       |
|   | ± 1                             |         |         | mA    |
| <b>PEAK AMPLIFIER BIAS CURRENT</b><br>(Terminal 5)                      |                                 |         |         |       |
|   | 2                               |         |         | mA    |
| <b>OUTPUT CURRENT:</b>  |                                 |         |         |       |
| Peak  | 300                             |         |         | mA    |
| Average   | 100                             |         |         | mA    |
| <b>DEVICE DISSIPATION:</b>  |                                 |         |         |       |
| Up to T <sub>A</sub> = 55°C:  |                                 |         |         |       |
| Without heat sink   | 630                             |         |         | mW    |
| With heat sink  | 1.6                             |         |         | W     |
| Above T <sub>A</sub> = 55°C:  |                                 |         |         |       |
| Without heat sink derate linearly                                       | 6.67                            |         |         | mW/°C |
| With heat sink derate linearly  | 16.7                            |         |         | mW/°C |
| <b>THERMAL RESISTANCE</b><br>(Junction to Air)                          |                                 |         |         |       |
|   | 140                             |         |         | °C/W  |
| <b>AMBIENT TEMPERATURE RANGE:</b>                                       |                                 |         |         |       |
| Operating   | -55 to +125                     |         |         | °C    |
| Storage   | -65 to +150                     |         |         | °C    |
| <b>LEAD TEMPERATURE (DURING SOLDERING):</b>                             |                                 |         |         |       |
| At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm)<br>from case for 10 s max. | + 300                           |         |         | °C    |

\*Exceeding this voltage rating will not damage the device unless the peak input signal current (1 mA) is also exceeded.

## TYPICAL CHARACTERISTICS CURVES

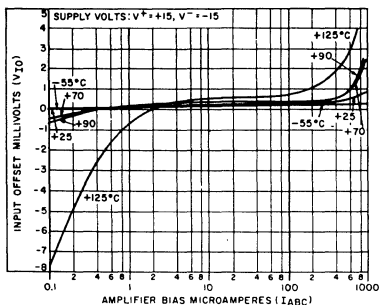


Fig.2 — Input offset voltage vs. amplifier bias current (I<sub>ABC</sub>, terminal No.5).

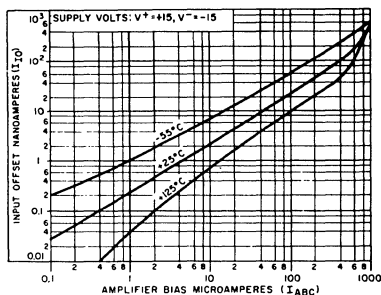


Fig.3 — Input offset current vs. amplifier bias current (I<sub>ABC</sub>, terminal No.5).

# CA3094, CA3094A, CA3094B

## TYPICAL CHARACTERISTICS CURVES (Cont'd)

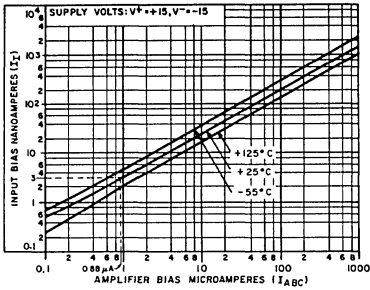


Fig. 4 - Input bias current vs. amplifier bias current ( $I_{ABC}$ , terminal No.5).

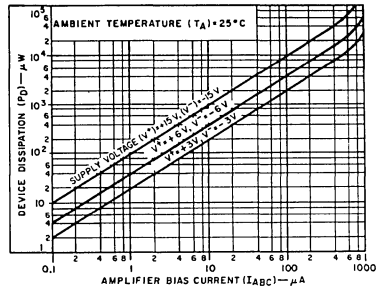


Fig. 5 - Device dissipation vs. amplifier bias current ( $I_{ABC}$ , terminal No.5).

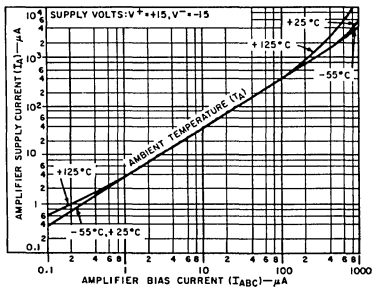


Fig. 6 - Amplifier supply current vs. amplifier bias current ( $I_{ABC}$ , terminal No.5).

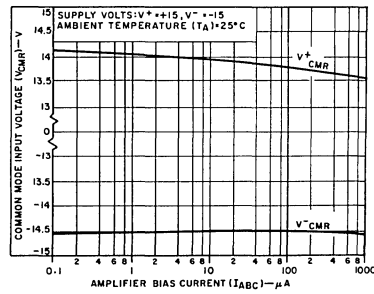


Fig. 7 - Common mode input voltage vs. amplifier bias current ( $I_{ABC}$ , terminal No.5).

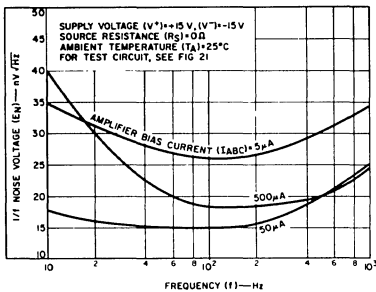


Fig. 8 - 1/F Noise voltage vs. frequency.

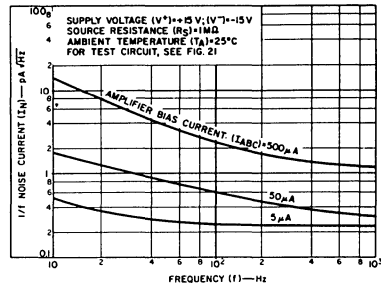


Fig. 9 - 1/F Noise current vs. frequency.

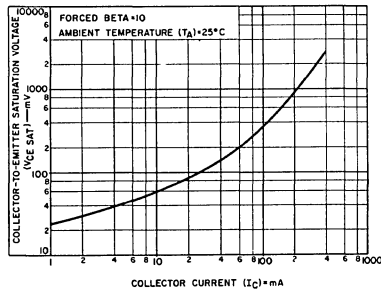


Fig. 10 - Collector-emitter saturation voltage vs. collector current of output transistor  $Q_{13}$ .

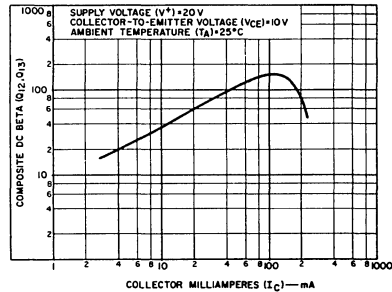


Fig. 11 - Composite dc beta vs. collector current of Darlington-connected output transistors ( $Q_{12}$ ,  $Q_{13}$ ).

# CA3094, CA3094A, CA3094B

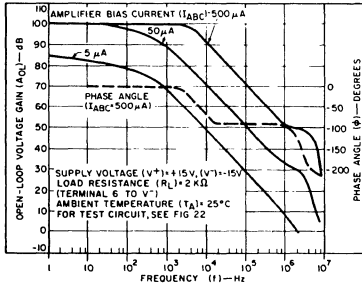


Fig. 12 - Open-loop voltage gain vs. frequency.

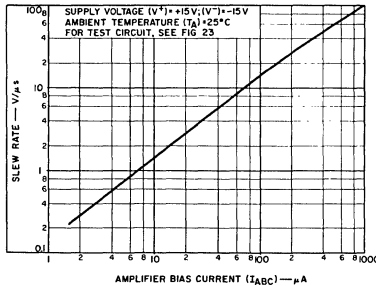


Fig. 14 - Slew rate vs amplifier bias current.

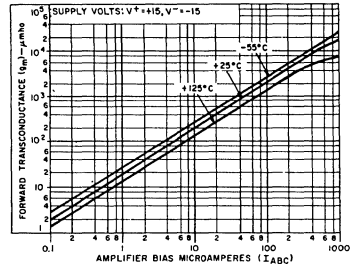


Fig. 13 - Forward transconductance vs amplifier bias current.

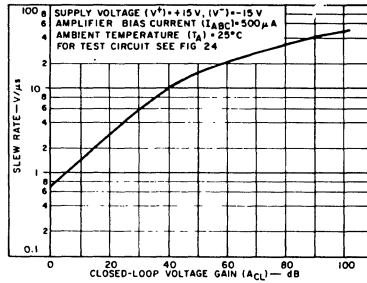


Fig. 15 - Slew rate vs closed-loop voltage gain.

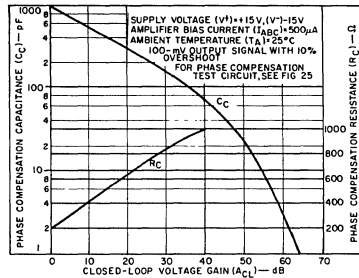


Fig. 16 - Phase compensation capacitance and resistance vs closed-loop voltage gain.

## OPERATING CONSIDERATIONS

The "Sink" Output (terminal No.8) and the "Drive" Output (terminal No.6) of the CA3094 are not inherently current (or power) limited. Therefore, if a load is connected between terminal No.6 and terminal No.4 ( $V^-$  or ground), it is important to connect a current-limiting resistor between terminal 8 and terminal No.7 ( $V^+$ ) to protect transistor Q13 under shorted load conditions. Similarly, if a load is connected between terminal No.8 and terminal No.7, the current-limiting resistor should be connected between terminal No.6 and terminal No.4 or ground. In circuit applications where the emitter of the output transistor is not connected to the most negative potential in the system, it is recommended that a 100-ohm current-limiting resistor be inserted between terminal No.7 and the  $V^+$  supply.

## TEST CIRCUITS

### I/F Noise Measurement Circuit

When using the CA3094, A, or B audio amplifier circuits, it is frequently necessary to consider the noise performance of the device. Noise measurements are made in the circuit shown in Fig.21. This circuit is a 30-dB, non-inverting amplifier with emitter-follower output and phase compensation from terminal No.2 to ground. Source resistors ( $R_s$ ) are set to  $0.\Omega$  or 1 M $\Omega$  for E noise and I noise measurements, respectively. These measurements are made at frequencies of 10, Hz, 100 Hz, and 1 kHz with a 1-Hz measurement bandwidth. Typical values for 1/f noise at 10 Hz and 50  $\mu A$   $I_{ABC}$  are  $E_n = 18 \text{ nV}/\sqrt{\text{HZ}}$  and  $I_n = 1.8 \text{ pA}/\sqrt{\text{HZ}}$ .

# CA3094, CA3094A, CA3094B

## TEST CIRCUITS

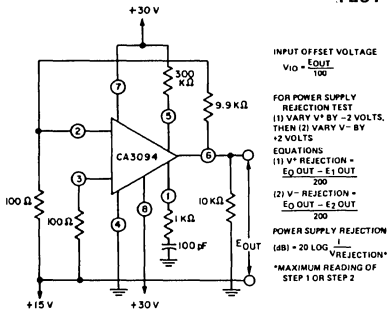


Fig. 17 - Input offset voltage and power-supply rejection test circuit.

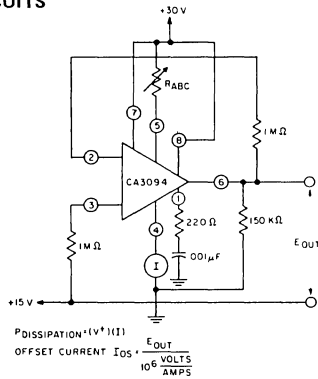


Fig. 18 - Input offset current test circuit.

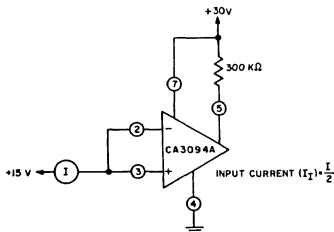


Fig. 19 - Input bias current test circuit.

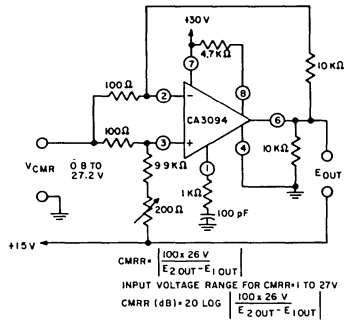


Fig. 20 - Common-mode range and rejection ratio test circuit.

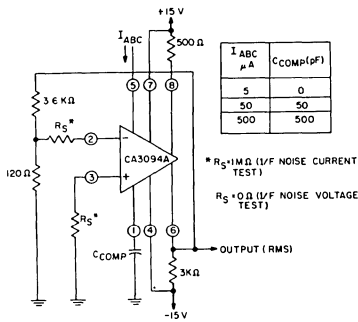


Fig. 21 - 1/f noise test circuit.

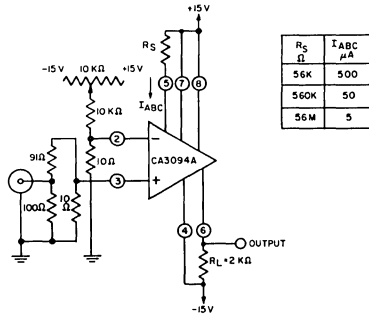


Fig. 22 - Open-loop gain vs frequency test circuit.

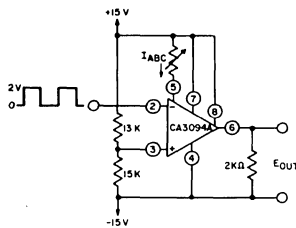


Fig. 23 - Open-loop slew rate vs  $I_{ABC}$  test circuit.

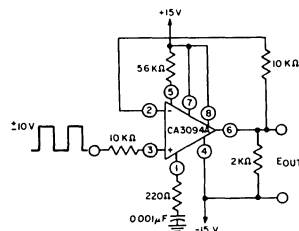


Fig. 24 - Slew rate vs. non-inverting unity gain test circuit.



# CA3094, CA3094A, CA3094B

## TEST CIRCUITS (Cont'd)

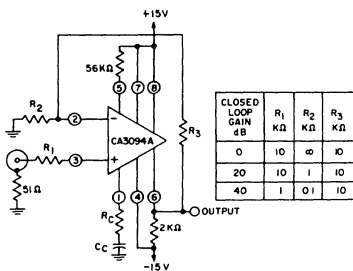
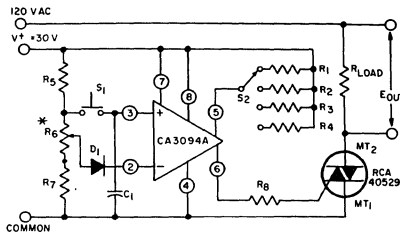
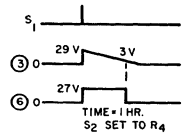


Fig.25 — Phase compensation test circuit.



- C<sub>1</sub> = 0.5 μF
- D<sub>1</sub> = 1N914
- R<sub>1</sub> = 0.51 MΩ ± 3 MIN.
- R<sub>2</sub> = 5.1 MΩ ± 30 MIN.
- R<sub>3</sub> = 22 MΩ ± 2 HRS.
- R<sub>4</sub> = 44 MΩ ± 4 HRS.
- R<sub>5</sub> = 1.5 KΩ
- R<sub>6</sub> = 50 KΩ
- R<sub>7</sub> = 5.1 KΩ
- R<sub>8</sub> = 1.5 KΩ



\* POTENTIOMETER REQUIRED FOR INITIAL TIME SET TO PERMIT DEVICE INTERCONNECTING TIME VARIATION WITH TEMPERATURE < 0.3 % / °C.

Fig.26 — Pre-settable analog timer.

### TYPICAL APPLICATIONS

For Additional Application Information, refer to Application Note ICAN-6048 "Some Applications of a Programmable Power/Switch Amplifier IC".

#### Design Considerations

The selection of the optimum amplifier bias current (I<sub>ABC</sub>) depends on —

1. The Desired Sensitivity — the higher the I<sub>ABC</sub>, the higher the sensitivity — i.e., a greater-drive current capability at the output for a specific voltage change at the input.

2. Required Input Resistance — the lower the I<sub>ABC</sub>, the higher the input resistance. If the desired sensitivity and required input resistance are not known and are to be experimentally determined, or the anticipated equipment design is sufficiently flexible to tolerate a wide range of these parameters, it is recommended that the equipment designer begin his calculations with an I<sub>ABC</sub> of 100 μA, since the CA3094 is characterized at this value of amplifier bias current.

The CA3094 is extremely versatile and can be used in a wide variety of applications.

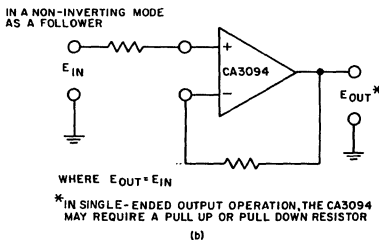
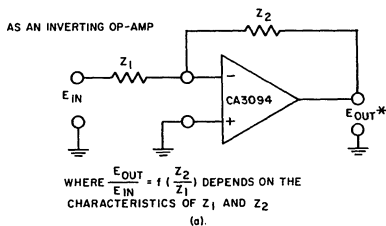
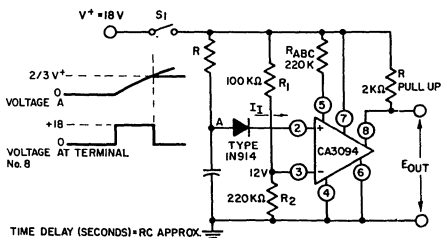


Fig.27 — Application of the CA3094: (a) as an inverting op-amp, and (b) in a non-inverting mode, as a follower.



Problem: To calculate the maximum value of R required to switch a 100-mA output current comparator

Given:  $I_{ABC} = 5 \mu A, R_{ABC} = 3.6 M\Omega \approx \frac{18 V}{5 \mu A}$

I<sub>1</sub> = 500 nA @ I<sub>ABC</sub> = 100 μA (from Fig.4)  
 I<sub>1</sub> = 5 μA can be determined by drawing a line on Fig.4 through I<sub>ABC</sub> = 100 μA and I<sub>B</sub> = 500 nA parallel to the typical T<sub>A</sub> = 25°C curve.

Then: I<sub>1</sub> = 33 nA @ I<sub>ABC</sub> = 5 μA

$$R_{max} = \frac{18 - 12 \text{ volts}}{33 nA} = 180 M\Omega @ T_A = 25^\circ C$$

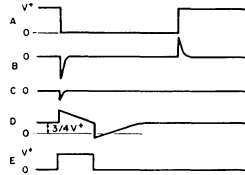
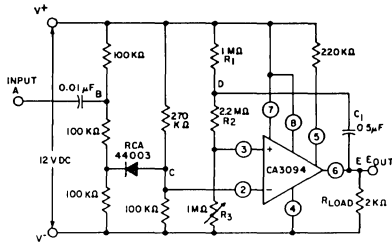
$$R_{max} = 180 M\Omega \times 2/3^* = 120 M\Omega @ T_A = -55^\circ C$$

\* Ratio of I<sub>1</sub> at T<sub>A</sub> = +25°C to I<sub>1</sub> at T<sub>A</sub> = -55°C for any given value of I<sub>ABC</sub>.

Fig.28 — RC timer.

# CA3094, CA3094A, CA3094B

## TYPICAL APPLICATIONS (Cont'd)



On a negative-going transient at input (A), a negative pulse at C will turn "on" the CA3094, and the output (E) will go from a low to a high level.

At the end of the time constant determined by  $C_1$ ,  $R_1$ ,  $R_2$ ,  $R_3$ , the CA3094 will return to the "off" state and the output will be pulled low by  $R_{LOAD}$ . This condition will be independent of the interval when input A returns to a high level.

Fig.29 — RC timer triggered by external negative pulse.

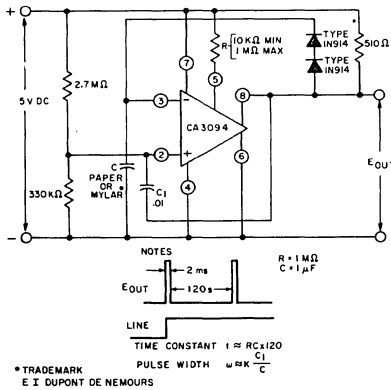


Fig.30 — Free-running pulse generator.

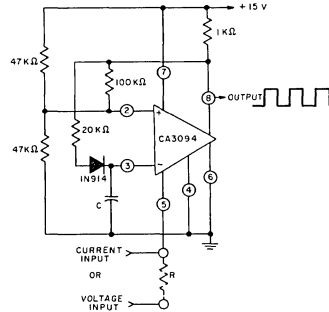


Fig.31 — Current or voltage-controlled oscillator.

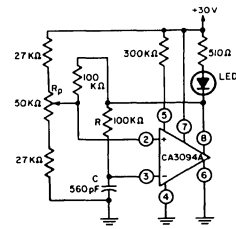


Fig.32 — Single-supply astable multivibrator.

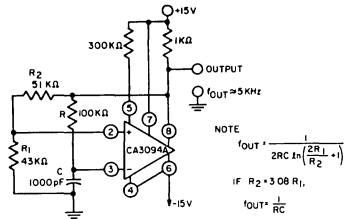


Fig.33 — Dual-supply astable multivibrator.

# CA3094, CA3094A, CA3094B

## TYPICAL APPLICATIONS (Cont'd)

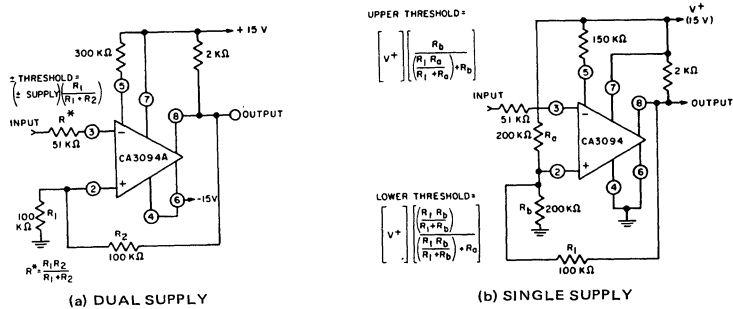


Fig. 34 - Comparators (threshold detectors) - dual- and single-supply types.

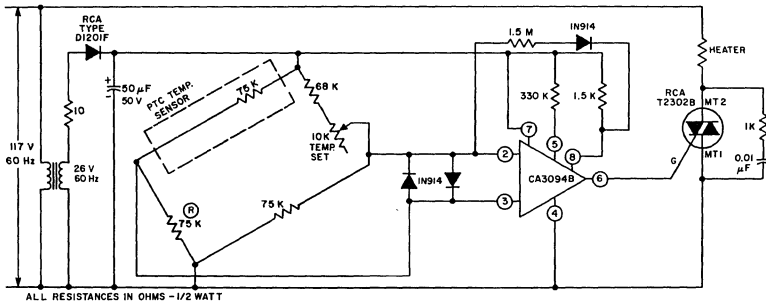


Fig. 35 - Temperature controller.

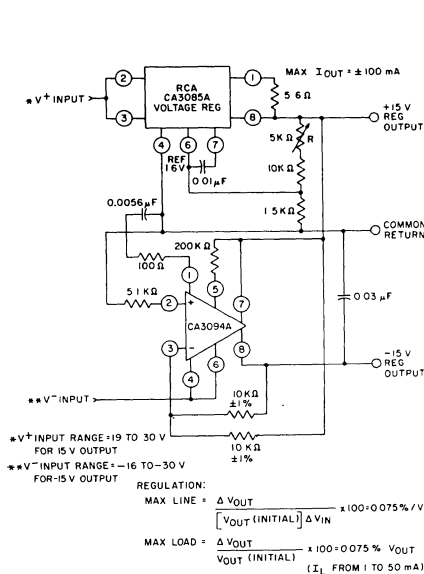


Fig. 36 - Dual-voltage tracking regulator.

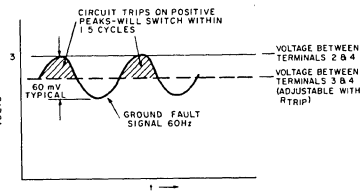
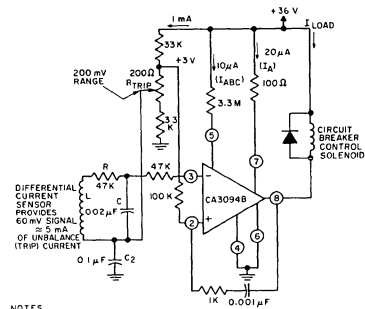
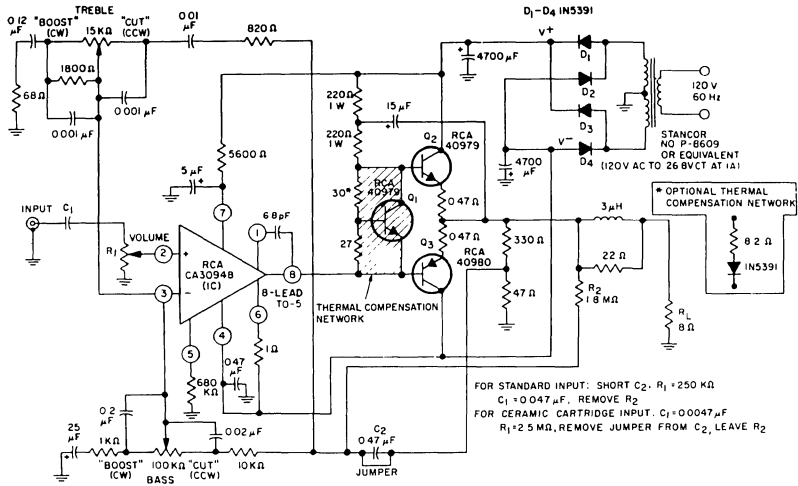


Fig. 37 - Ground fault interrupter (GFI) and waveform pertinent to ground fault detector.

# CA3094, CA3094A, CA3094B



FOR STANDARD INPUT: SHORT C<sub>2</sub>, R<sub>1</sub> = 250 kΩ  
 C<sub>1</sub> = 0.047 μF, REMOVE R<sub>2</sub>  
 FOR CERAMIC CARTRIDGE INPUT: C<sub>1</sub> = 0.0047 μF  
 R<sub>1</sub> = 2.5 MΩ, REMOVE JUMPER FROM C<sub>2</sub>, LEAVE R<sub>2</sub>

### TYPICAL PERFORMANCE DATA For 12-W Audio Amplifier Circuit

|   |                        |    |
|---|------------------------|----|
| Power Output (8Ω load, Tone Control set at "Flat")  |                        |    |
| Music (at 5% THD, regulated supply)   | 15                     | W  |
| Continuous (at 0.2% IMD, 60 Hz & 2 kHz mixed in a 4:1 ratio, unregulated supply) See Fig-8 in ICAN-6048 | 12                     | W  |
| Total Harmonic Distortion   |                        |    |
| At 1 W, unregulated supply  | 0.05                   | %  |
| At 12 W, unregulated supply   | 0.57                   | %  |
| Voltage Gain  | 40                     | dB |
| Hum and Noise (Below continuous Power Output)   | 83                     | dB |
| Input Resistance  | 250                    | kΩ |
| Tone Control Range  | See Fig 9 in ICAN-6048 |    |

Fig.38 — 12-watt amplifier circuit featuring true complementary-symmetry output stage with CA3094 in driver stage.

August 1991

## Wide-Band Operational Amplifier

### Features

- High Open-Loop Gain at Video Frequencies ..... 42dB (Typ.) @ 1MHz
- High Unity-Gain Crossover Frequency ( $f_T$ ) ..... 38MHz (Typ.)
- Wide Power Bandwidth  
 $V_O = 18Vp-p$  ..... 1.2MHz (Typ.)
- High Slew Rate
  - ▶ 20dB Amplifier ..... 70V/ $\mu s$  (Typ.)
  - ▶ Unity-Gain Amplifier ..... 25V/ $\mu s$  (Typ.)
- Fast Settling Time ..... 0.6 $\mu s$  (Typ.)
- High Output Current .....  $\pm 15mA$  Min.
- Single Capacitor Compensation
- Offset Null Terminals

### Applications

- Video Amplifiers
- Fast Peak Detectors
- Meter-Driver Amplifiers
- High-Frequency Feedback Amplifiers
- Video Pre-Drivers
- Oscillators
- Multivibrators
- Voltage-Controlled Oscillator
- Fast Comparators

### Description

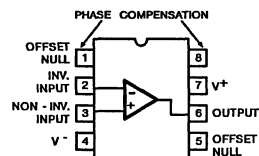
The CA3100 is a large-signal wideband, high-speed operational amplifier which has a unity gain cross-over frequency ( $f_T$ ) of approximately 38 MHz and an open-loop, 3 dB corner frequency of approximately 110 kHz. It can operate at a total supply voltage of from 14 to 36 volts ( $\pm 7$  to  $\pm 18$  volts when using split supplies) and can provide at least 18 Vp-p and 30 mA p-p at the output when operating from  $\pm 15$  volt supplies. The CA3100 can be compensated with a single external capacitor and has dc offset adjust terminals for those applications requiring offset null. (See Fig. 15).

The CA3100 circuit contains both bipolar and PMOS transistors on a single monolithic chip.

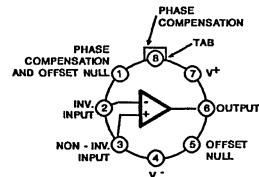
These devices are supplied in either the 8-lead Small Outline style package (M suffix), the standard 8-lead TO-5 style package (T suffix), 8-lead dual-in-line formed-lead TO-5 style "DIL-CAN" package (S suffix), or in the 8-lead dual-in-line plastic package "Mini-DIP" (E suffix). They are also available in chip form (H suffix).

### Pinouts

#### E AND M SUFFIXES TOP VIEW



#### S AND T SUFFIXES TOP VIEW



### Schematic Diagram

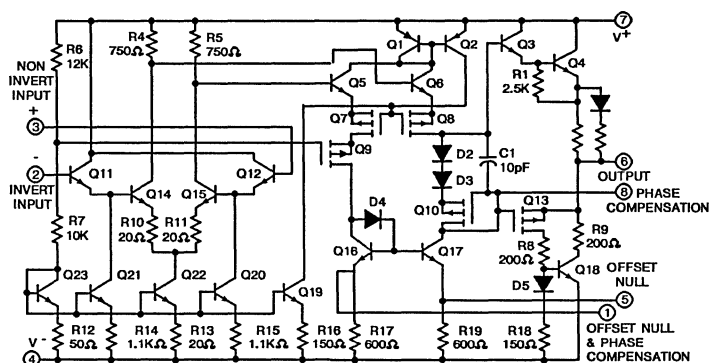


FIGURE 1. SCHEMATIC DIAGRAM FOR CA3100

# CA3100

ELECTRICAL CHARACTERISTICS, At  $T_A = 25^\circ\text{C}$ :

| CHARACTERISTICS  | TEST CONDITIONS<br>SUPPLY VOLTAGE ( $V^+, V^-$ )=15 V<br>UNLESS OTHERWISE SPECIFIED | LIMITS   |            |           | UNITS                      |
|--|---|----------|------------|-----------|----------------------------|
|  |   | MIN.     | TYP.       | MAX.      |                            |
| <b>STATIC</b>  |   |          |            |           |                            |
| Input Offset Voltage, $V_{IO}$   | $V_O = 0 \pm 0.1 \text{ V}$   | –        | $\pm 1$    | $\pm 5$   | mV                         |
| Input Bias Current, $I_{IB}$   | $V_O = 0 \pm 1 \text{ V}$   | –        | 0.7        | 2         | $\mu\text{A}$              |
| Input Offset Current, $I_{IO}$   |   | –        | $\pm 0.05$ | $\pm 0.4$ | $\mu\text{A}$              |
| Low-Frequency Open-Loop Voltage Gain, $A_{OL}^*$                               | $V_O = \pm 1 \text{ V Peak, } F = 1 \text{ kHz}$                                    | 56       | 61         | –         | dB                         |
| Common-Mode Input Voltage Range, $V_{ICR}$                                     | $\text{CMRR} \geq 76 \text{ dB}$  | $\pm 12$ | +14<br>–13 | –         | V                          |
| Common-Mode Rejection Ratio, CMRR  | $V_I \text{ Common Mode} = \pm 12 \text{ V}$  | 76       | 90         | –         | dB                         |
| Maximum Output Voltage:<br>Positive, $V_{OM}^+$<br>Negative, $V_{OM}^-$        | Differential Input Voltage = $0 \pm 0.1 \text{ V}$<br>$R_L = 2 \text{ K}\Omega$     | +9       | +11        | –         | V                          |
|  |   | –9       | –11        | –         |                            |
| Maximum Output Current:<br>Positive, $I_{OM}^+$<br>Negative, $I_{OM}^-$        | Differential Input Voltage = $0 \pm 0.1 \text{ V}$<br>$R_L = 250 \Omega$            | +15      | +30        | –         | mA                         |
|  |   | –15      | –30        | –         |                            |
| Supply Current, $I^+$  | $V_O = 0 \pm 0.1 \text{ V, } R_L \geq 10 \text{ K}\Omega$                           | –        | 8.5        | 10.5      | mA                         |
| Power-Supply Rejection Ratio, PSRR   | $\Delta V^+ = \pm 1 \text{ V, } \Delta V^- = \pm 1 \text{ V}$                       | 60       | 70         | –         | dB                         |
| <b>DYNAMIC</b>   |   |          |            |           |                            |
| Unity-Gain Crossover Frequency, $f_T$  | $C_C = 0, V_O = 0.3 \text{ V (P-P)}$  | –        | 38         | –         | MHz                        |
| 1-MHz Open-Loop Voltage Gain, $A_{OL}$   | $f = 1 \text{ MHz, } C_C = 0, V_O = 10 \text{ V (P-P)}$                             | 36       | 42         | –         | dB                         |
| Slew Rate, SR:<br>20-dB Amplifier  | $A_V = 10, C_C = 0, V_I = 1 \text{ V (Pulse)}$                                      | 50       | 70         | –         | V/ $\mu\text{s}$           |
|  | Follower Mode<br>$A_V = 1, C_C = 10 \text{ pF, } V_I = 10 \text{ V (Pulse)}$        | –        | 25         | –         |                            |
| Power Bandwidth, PBW <sup>▲</sup> :<br>20-dB Amplifier                         | $A_V = 10, C_C = 0, V_O = 18 \text{ V (P-P)}$                                       | 0.8      | 1.2        | –         | MHz                        |
|  | Follower Mode<br>$A_V = 1, C_C = 10 \text{ pF, } V_O = 18 \text{ V (P-P)}$          | –        | 0.4        | –         |                            |
| Open-Loop Differential Input Impedance, $Z_I$                                  | $F = 1 \text{ MHz}$   | –        | 30         | –         | $\text{K}\Omega$           |
| Open-Loop Output Impedance, $Z_O$  | $F = 1 \text{ MHz}$   | –        | 110        | –         | $\Omega$                   |
| Wideband Noise Voltage Referred to Input, $e_N$ (Total)                        | $\text{BW} = 1 \text{ MHz, } R_S = 1 \text{ K}\Omega$                               | –        | 8          | –         | $\mu\text{V}_{\text{RMS}}$ |
| Settling Time, $t_s$<br>[To Within $\pm 50 \text{ mV}$ of 9 V<br>Output Swing] | $R_L = 2 \text{ K}\Omega, C_L = 20 \text{ pF}$                                      | –        | 0.6        | –         | $\mu\text{s}$              |

▲ Power Bandwidth =  $\frac{\text{Slew Rate}}{\pi V_O \text{ (P-P)}}$

• Low-frequency dynamic characteristic

# CA3100

## MAXIMUM RATINGS, Absolute-Maximum Values:

|   |             |                      |
|---|-------------|----------------------|
| Supply Voltage (between V+ and V- terminals)                          | 36          | V                    |
| Differential Input Voltage  | ±12         | V                    |
| Input Voltage to Ground*  | ±15         | V                    |
| Offset Terminal to V- Terminal Voltage                                | ±0.5        | V                    |
| Output Current  | 50          | mA                   |
| Device Dissipation:   |             |                      |
| Up to $T_A = 55^\circ\text{C}$  | 630         | mW                   |
| Above $T_A = 55^\circ\text{C}$  | 6.67        | mW/ $^\circ\text{C}$ |
| Ambient Temperature Range:  |             |                      |
| Operating:  |             |                      |
| E and M Types   | -40 to +85  | $^\circ\text{C}$     |
| S and T Types   | -55 to +125 | $^\circ\text{C}$     |
| Storage   | -65 to +150 | $^\circ\text{C}$     |
| Lead Temperature (During Soldering):                                  |             |                      |
| At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. | +265        | $^\circ\text{C}$     |

\* If the supply voltage is less than ±15 volts, the maximum input voltage to ground is equal to the supply voltage.

• CA3100 does not contain circuitry to protect against short circuits in the output.

## TYPICAL CHARACTERISTIC CURVES

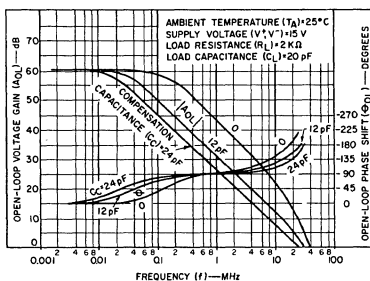


Fig. 2 - Open-loop gain, open-loop phase shift vs. frequency.

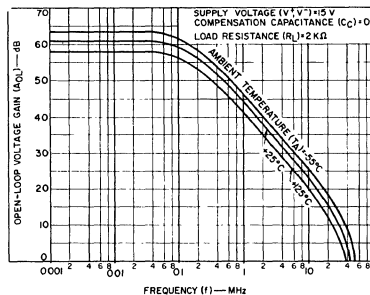


Fig. 3 - Open-loop gain vs. frequency and temperature.

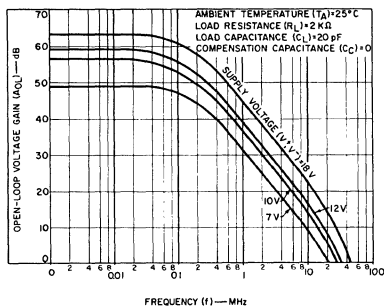


Fig. 4 - Open-loop gain vs. frequency and supply voltage.

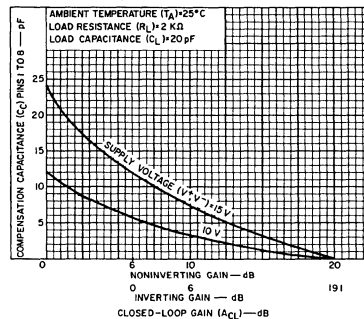


Fig. 5 - Required compensation capacitance vs. closed-loop gain.

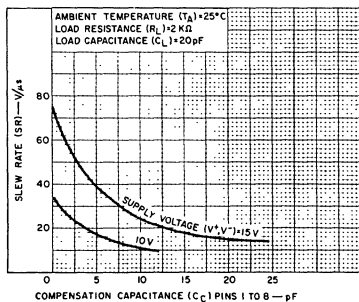


Fig. 6 - Slew rate vs. compensation capacitance.

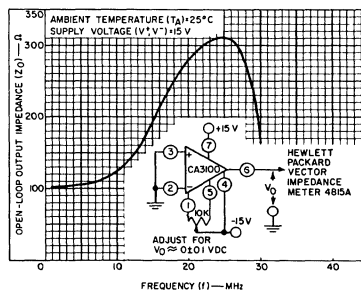


Fig. 7 - Typical open-loop output impedance vs. frequency.

TYPICAL CHARACTERISTIC CURVES (Cont'd)

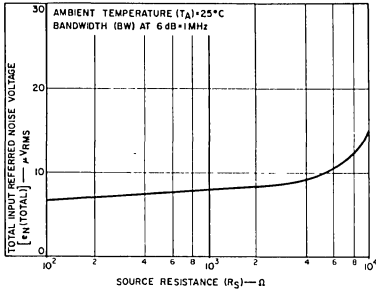


Fig. 8 — Wideband input noise voltage vs. source resistance.

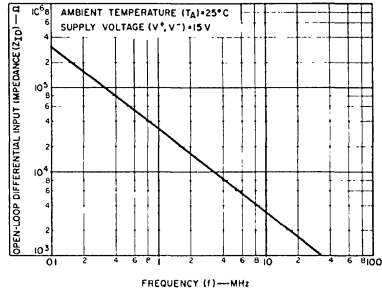


Fig. 9 — Typical open-loop differential input impedance vs. frequency.

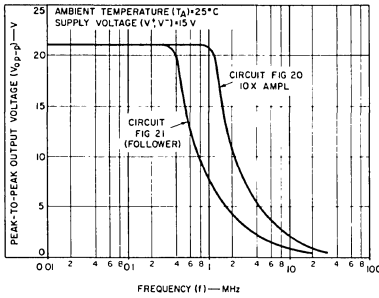


Fig. 10 — Maximum output voltage swing vs. frequency.

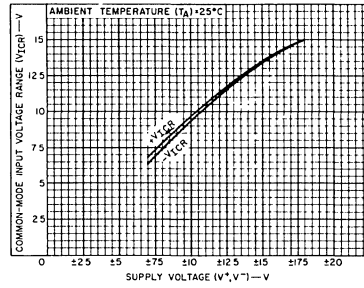


Fig. 11 — Common-mode input voltage range vs. supply voltage.

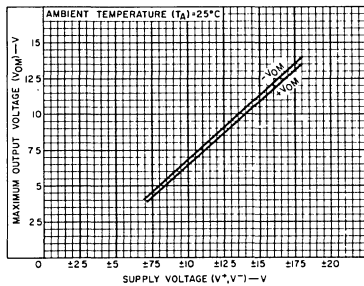


Fig. 12 — Maximum output voltage vs. supply voltage.

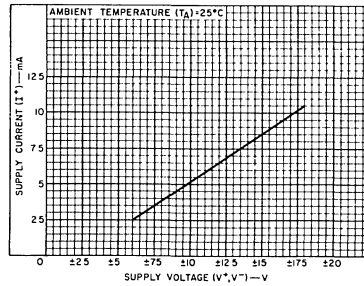


Fig. 13 — Supply current vs. supply voltage.

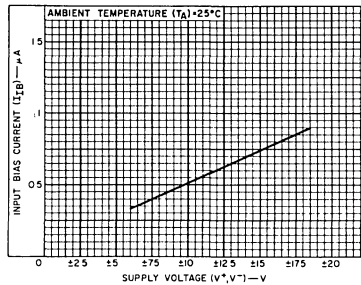


Fig. 14 — Input bias current vs. supply voltage.

3  
OPERATIONAL  
AMPLIFIERS



# CA3100

## TEST CIRCUITS

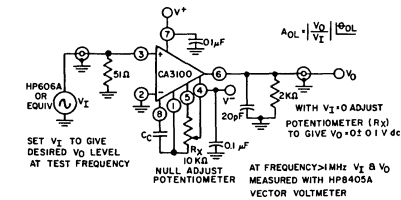


Fig. 15 - Open-loop voltage gain test circuit.

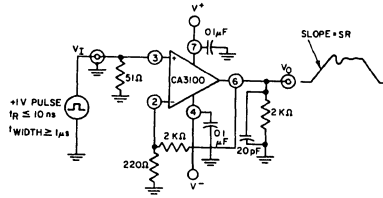


Fig. 16 - Slew rate in 10X amplifier test circuit.

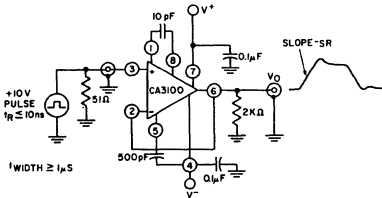


Fig. 17 - Follower slew rate test circuit.

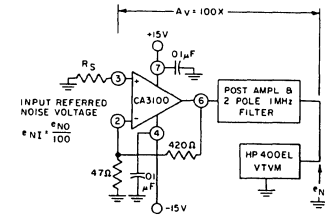


Fig. 18 - Wideband input noise voltage test circuit.

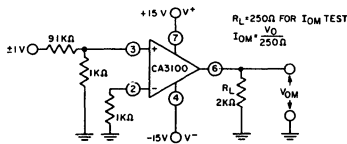


Fig. 19 - Output voltage swing ( $V_{OM}$ ), output current swing ( $I_{OM}$ ) test circuit.

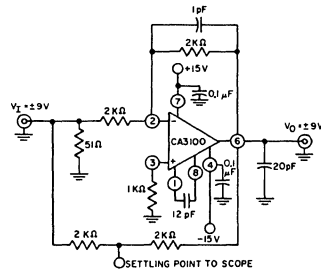


Fig. 20 - Settling time test circuit.

## TYPICAL APPLICATIONS

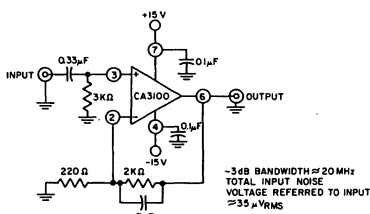


Fig. 21 - 20 dB video amplifier.

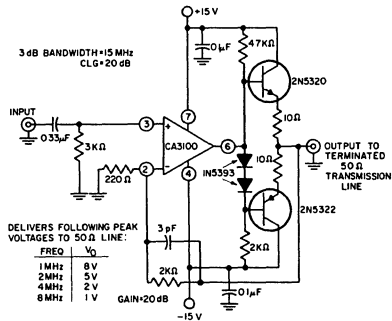


Fig. 22 - 20 dB video line driver.

# CA3100

## TYPICAL APPLICATIONS (Cont'd)

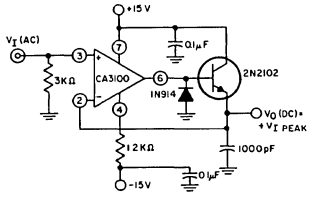


Fig. 23 – Fast positive peak detector.

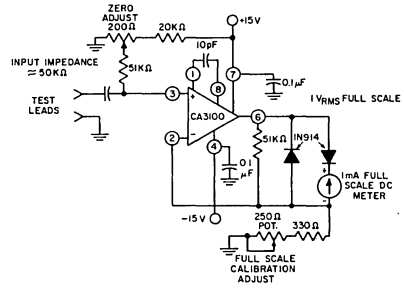


Fig. 24 – 1 MHz meter-driver amplifier.

August 1991

### Features

- MOSFET Input Stage Provides:
  - ▶ Very High  $Z_i = 1.5 T\Omega (1.5 \times 10^{12}\Omega)$  Typ.
  - ▶ Very Low  $I_i = 5\text{pA}$  Typ. @ 15V Operation  
= 2pA Typ. @ 5V Operation
- Ideal for Single-Supply Applications
- Common-Mode Input-Voltage Range Includes Negative Supply Rail; Input Terminals can be Swung 0.5V below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or both) Supply Rails

### Applications

- Ground-Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long-Duration Timers/Monostables
- High-Input-Impedance Comparators (Ideal Interface with Digital CMOS)
- High-Input-Impedance Wideband Amplifiers
- Voltage Followers (e.g. Follower for Single-Supply D/A Converter)
- Voltage Regulators (Permits Control of Output Voltage Down to Zero Volts)
- Peak Detectors
- Single-Supply Full-Wave Precision Rectifiers
- Photo-Diode Sensor Amplifiers

### Description

CA3130A and CA3130 are integrated-circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip.

Gate-protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3130 Series circuits operate at supply voltages ranging from 5 to 16 volts, or  $\pm 2.5$  to  $\pm 8$  volts when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA3130 Series is supplied in standard 8-lead TO-5 style packages (T suffix), 8-lead dual-in-line formed lead TO-5 style "DIL-CAN" packages (S suffix). The CA3130 is available in chip form (H suffix). The CA3130 and CA3130A are also available in the Mini-DIP 8-lead dual-in-line plastic package (E suffix), and in the 8-lead Small Outline package (M suffix). All types operate over the full military-temperature range of  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ . The CA3130A offers superior input characteristics over those of the CA3130.

### Pinouts

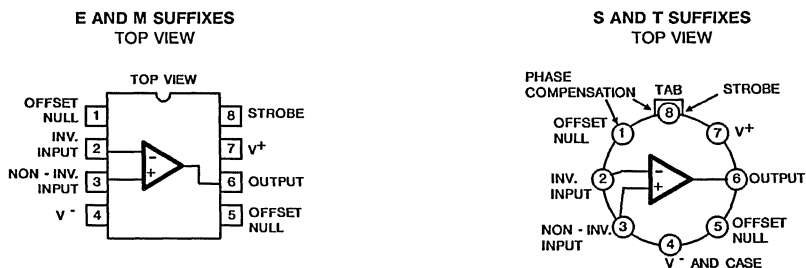


FIGURE 1.

## CA3130A, CA3130

**ELECTRICAL CHARACTERISTICS** at  $T_A=25^{\circ}\text{C}$ ,  $V^+=15\text{ V}$ ,  $V^- = 0\text{ V}$  (Unless otherwise specified)

| CHARACTERISTIC  | LIMITS               |                  |      |                     |                  |      | Units                          |
|---|----------------------|------------------|------|---------------------|------------------|------|--------------------------------|
|   | CA3130A (T, S, E, M) |                  |      | CA3130 (T, S, E, M) |                  |      |                                |
|   | Min.                 | Typ.             | Max. | Min.                | Typ.             | Max. |                                |
| Input Offset Voltage,<br>$ V_{IO} $ , $V^{\pm}=\pm 7.5\text{ V}$                              | –                    | 2                | 5    | –                   | 8                | 15   | mV                             |
| Input Offset Current,<br>$ I_{IO} $ , $V^{\pm}=\pm 7.5\text{ V}$                              | –                    | 0.5              | 20   | –                   | 0.5              | 30   | pA                             |
| Input Current, $I_I$<br>$V^{\pm}=\pm 7.5\text{ V}$  | –                    | 5                | 30   | –                   | 5                | 50   | pA                             |
| Large-Signal Voltage<br>Gain, $A_{OL}$<br>$V_O=10\text{ V}_{p-p}$ , $R_L=2\text{ k}\Omega$    | 50 k                 | 320 k            | –    | 50 k                | 320 k            | –    | V/V                            |
| Common-Mode<br>Rejection Ratio, CMRR  | 80                   | 90               | –    | 70                  | 90               | –    | dB                             |
| Common-Mode Input-<br>Voltage Range, $V_{ICR}$  | 0                    | –0.5<br>to<br>12 | 10   | 0                   | –0.5<br>to<br>12 | 10   | V                              |
| Power-Supply Rejection<br>Ratio, $\Delta V_{IO}/\Delta V^{\pm}$<br>$V^{\pm}=\pm 7.5\text{ V}$ | –                    | 32               | 150  | –                   | 32               | 320  | $\mu\text{V}/\text{V}$         |
| Maximum Output<br>Voltage:  |                      |                  |      |                     |                  |      | V                              |
| At $R_L=2\text{ k}\Omega$ $\frac{V_{OM}^+}{V_{OM}^-}$   | 12                   | 13.3             | –    | 12                  | 13.3             | –    |                                |
|   | –                    | 0.002            | 0.01 | –                   | 0.002            | 0.01 |                                |
| At $R_L=\infty$ $\frac{V_{OM}^+}{V_{OM}^-}$   | 14.99                | 15               | –    | 14.99               | 15               | –    |                                |
|   | –                    | 0                | 0.01 | –                   | 0                | 0.01 |                                |
| Maximum Output<br>Current:  |                      |                  |      |                     |                  |      | mA                             |
| $I_{OM}^+$ (Source) @<br>$V_O = 0\text{ V}$   | 12                   | 22               | 45   | 12                  | 22               | 45   |                                |
| $I_{OM}^-$ (Sink) @<br>$V_O = 15\text{ V}$  | 12                   | 20               | 45   | 12                  | 20               | 45   |                                |
| Supply Current, $I^+$ :<br>$V_O=7.5\text{ V}$ , $R_L=\infty$                                  | –                    | 10               | 15   | –                   | 10               | 15   | mA                             |
| $V_O = 0\text{ V}$ , $R_L = \infty$   | –                    | 2                | 3    | –                   | 2                | 3    |                                |
| Input Offset Voltage<br>Temp. Drift,<br>$\Delta V_{IO}/\Delta T^*$                            | –                    | 10               | –    | –                   | 10               | –    | $\mu\text{V}/^{\circ}\text{C}$ |

## CA3130A, CA3130

### TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

| CHARACTERISTIC                                    | TEST CONDITIONS  | CA3130A<br>CA3130<br>(T, S, E, M)              | UNITS         |
|---|--|--|---------------|
|   | $V^+ = +7.5\text{ V}$<br>$V^- = -7.5\text{ V}$<br>$T_A = 25^\circ\text{C}$<br>(Unless Otherwise Specified) |  |               |
| Input Offset Voltage Adjustment Range             | 10 k $\Omega$ across Terms. 4 and 5 or 4 and 1   | $\pm 22$                                       | mV            |
| Input Resistance, $R_I$                           |  | 1.5  | T $\Omega$    |
| Input Capacitance, $C_I$                          | f = 1 MHz  | 4.3  | pF            |
| Equivalent Input Noise Voltage, $e_n$             | BW = 0.2 MHz<br>$R_S = 1\text{ M}\Omega^*$   | 23   | $\mu\text{V}$ |
| Unity Gain Crossover Frequency, $f_T$             | $C_C = 0$  | 15   | MHz           |
|   | $C_C = 47\text{ pF}$   | 4  |               |
| Slew Rate, SR:                                    | Open Loop  | $C_C = 0$                                      | 30            |
|   | Closed Loop  | $C_C = 56\text{ pF}$                           | 10            |
| Transient Response:                               | Rise Time, $t_r$   | $C_C = 56\text{ pF}$<br>$C_L = 25\text{ pF}$   | 0.09          |
|   | Overshoot  | $R_L = 2\text{ k}\Omega$<br>(Voltage Follower) | 10            |
| Settling Time (4 V <sub>p-p</sub> Input to <0.1%) |  | 1.2  | $\mu\text{s}$ |

\* Although a 1-M $\Omega$  source is used for this test, the equivalent input noise remains constant for values of  $R_S$  up to 10 M $\Omega$ .

| CHARACTERISTIC   | TEST CONDITIONS  | CA3130A<br>(T, S, E, M) | CA3130<br>(T, S, E, M) | UNITS           |
|--|--|-------------------------|------------------------|-----------------|
|  | $V^+ = 5\text{ V}$<br>$V^- = 0\text{ V}$<br>$T_A = 25^\circ\text{C}$<br>(Unless Otherwise Specified) |                         |                        |                 |
| Input Offset Voltage, $V_{IO}$                           |  | 2                       | 8                      | mV              |
| Input Offset Current, $I_{IO}$                           |  | 0.1                     | 0.1                    | pA              |
| Input Current, $I_I$                                     |  | 2                       | 2                      | pA              |
| Common-Mode Rejection Ratio, CMRR                        |  | 90                      | 80                     | dB              |
| Large-Signal Voltage Gain, $A_{OL}$                      | $V_O = 4\text{ V}_{p-p}$   | 100 k                   | 100 k                  | V/V             |
|  | $R_L = 5\text{ k}\Omega$   | 100                     | 100                    | dB              |
| Common-Mode Input Voltage Range, $V_{ICR}$               |  | 0 to 2.8                | 0 to 2.8               | V               |
| Supply Current, $I^+$                                    | $V_O = 5\text{ V}$ ,<br>$R_L = \infty$   | 300                     | 300                    | $\mu\text{A}$   |
|  | $V_O = 2.5\text{ V}$ ,<br>$R_L = \infty$   | 500                     | 500                    |                 |
| Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^+$ |  | 200                     | 200                    | $\mu\text{V/V}$ |

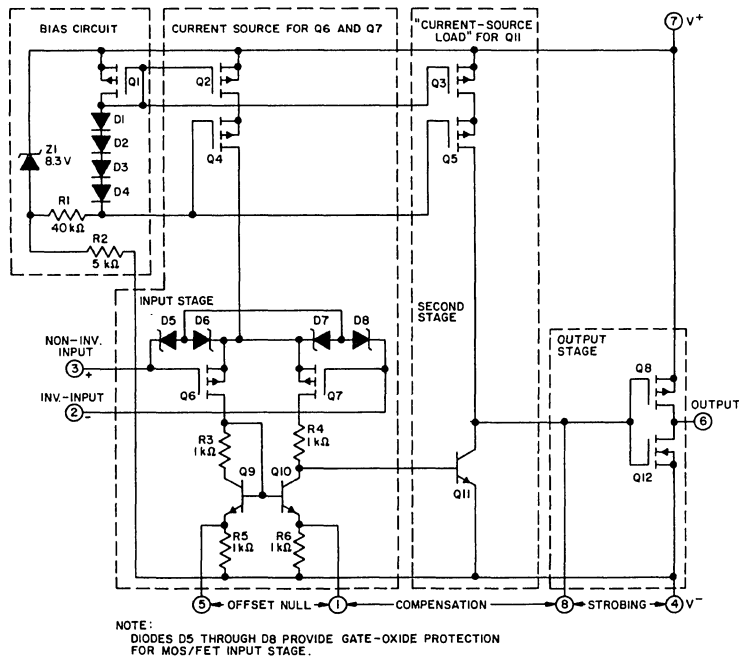
# CA3130A, CA3130

## MAXIMUM RATINGS, Absolute-Maximum Values

DC SUPPLY VOLTAGE  
(Between  $V^+$  and  $V^-$  Terminals) ..... 16 V  
DIFFERENTIAL-MODE INPUT VOLTAGE .....  $\pm 8$  V  
COMMON-MODE DC INPUT VOLTAGE ... ( $V^+ + 8$  V) to ( $V^- - 0.5$  V)  
INPUT-TERMINAL CURRENT ..... 1 mA  
DEVICE DISSIPATION:  
WITHOUT HEAT SINK —  
UP TO 55°C ..... 630 mW  
ABOVE 55°C ..... Derate linearly 6.67 mW/°C  
WITH HEAT SINK —  
UP TO 90°C ..... 1 W  
ABOVE 90°C ..... Derate linearly 16.7 mW/°C

TEMPERATURE RANGE:  
OPERATING (all types) ..... -55 to +125°C  
STORAGE (all types) ..... -65 to +150°C  
OUTPUT SHORT-CIRCUIT DURATION\* ..... INDEFINITE  
LEAD TEMPERATURE (DURING SOLDERING):  
AT DISTANCE 1/16  $\pm$  1/32 INCH  
(1.59  $\pm$  0.79 mm) FROM CASE ..... +265°C  
FOR 10 SECONDS MAX. ....

\*Short circuit may be applied to ground or to either supply.



92CM-24714R1

Fig. 2 — Schematic diagram of the CA3130 Series.

## CIRCUIT DESCRIPTION

Fig. 3 is a block diagram of the CA3130 Series CMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3130 Series circuits are ideal for single-supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in Fig. 3, provide the total gain of the CA3130. A biasing circuit provides two potentials for common use in the first and

second stages. Term. 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Term. 8 is tied to the negative supply rail (Term. 4) by mechanical or electrical means, the output potential at Term. 6 essentially rises to the positive supply-rail potential at Term. 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive CMOS digital circuits in comparator applications).

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OPERATIONAL AMPLIFIERS

## CA3130A, CA3130

**Input Stages**—The circuit of the CA3130 is shown in Fig. 2. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS transistors Q2, Q4 are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D8 provide gate-oxide protection against high-voltage transients, e.g., including static electricity during handling for Q6 and Q7.

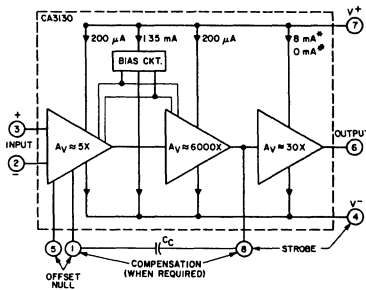
**Second-Stage**—Most of the voltage gain in the CA3130 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is subsequently described. Miller-Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terms. 1 and 8. A 47-picofarad capacitor provides sufficient compensation for stable unity-gain operation in most applications.

**Bias-Source Circuit**—At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Term. 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Term. 7 to provide gate bias for PMOS transistors Q2 and Q3. It

should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

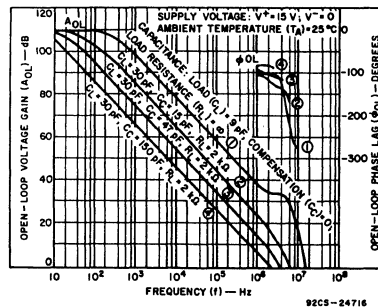
At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes non-conductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

**Output Stage**—The output stage consists of a drain-loaded inverting amplifier using CMOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig. 6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.



**Fig. 3 — Block diagram of the CA3130 Series.**

†For general information on the characteristics of CMOS transistor-pairs in linear-circuit applications, see File No. 619, data bulletin on CA3600E "CMOS Transistor Array".



**Fig. 4 — Open-loop voltage gain and phase shift vs. frequency for various values of  $C_L$ ,  $C_C$ , and  $R_L$ .**

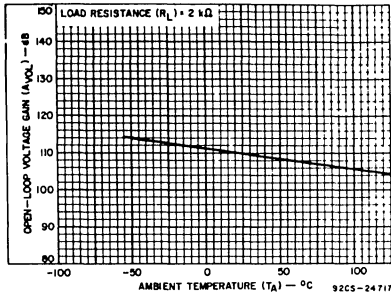


Fig. 5 - Open-loop gain vs. temperature.

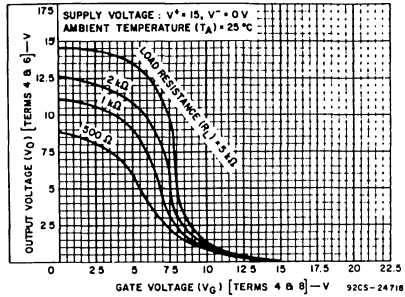


Fig. 6 - Voltage transfer characteristics of CMOS output stage.

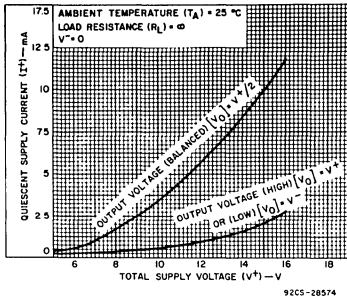


Fig. 7 - Quiescent supply current vs. supply voltage.

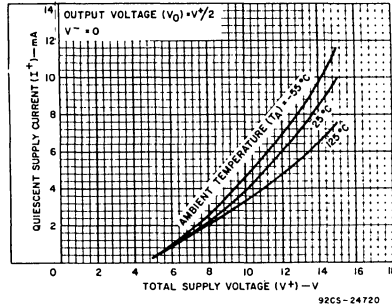


Fig. 8 - Quiescent supply current vs. supply voltage at several temperatures.

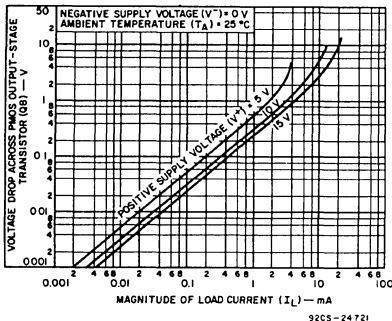


Fig. 9 - Voltage across PMOS output transistor (Q8) vs. load current.

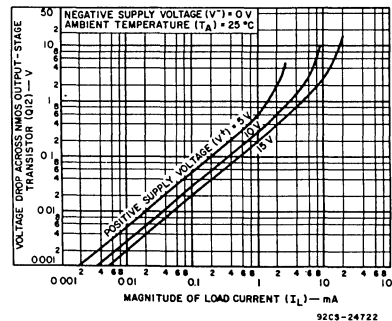


Fig. 10 - Voltage across NMOS output transistor (Q12) vs. load current.

**Input Current Variation with Common-Mode Input Voltage**

As shown in the Table of Electrical Characteristics, the input current for the CA3130 Series Op-Amps is typically 5 pA at  $T_A=25^\circ\text{C}$  when terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Fig.11 contains data showing the variation of input current as a function of common-mode input voltage at  $T_A = 25^\circ\text{C}$ . These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1 pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the

gate-protection diodes in the input circuit and, therefore, a function of the applied

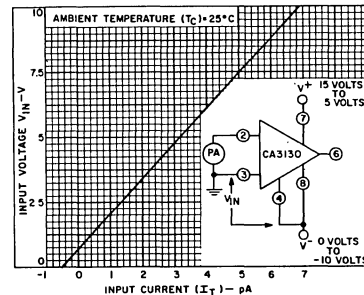


Fig.11 - Input current vs. common-mode voltage.



## CA3130A, CA3130

voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA3130 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

### Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terms. 1 and 5 and with the potentiometer slider arm connected to Term. 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

### Input-Current Variation with Temperature

The input current of the CA3130 Series circuits is typically 5 pA at 25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Fig.12 provides data on the typical variation of input bias current as a function of temperature in the CA3130.

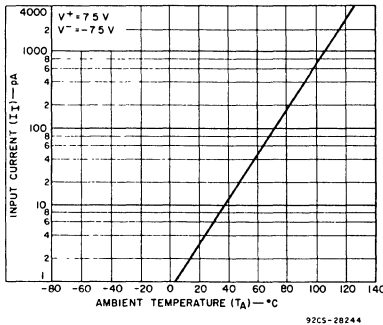


Fig.12 — Input current vs. ambient temperature.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3130. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

### Input-Offset-Voltage ( $V_{IO}$ ) Variation with DC Bias vs. Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magni-

tude of the change is increased at high temperatures. Users of the CA3130 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terms. 2 and 3. Fig.13 shows typical data pertinent to shifts in offset voltage encountered with CA3130 devices (TO-5 package) during life testing. At lower temperatures (TO-5 and plastic), for example at 85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output stage is "toggled", e.g., as in comparator applications.

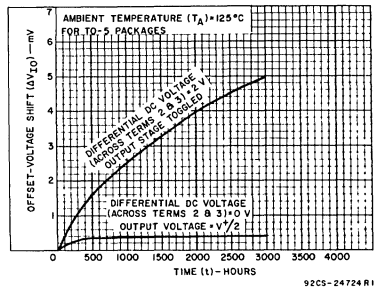


Fig.13 — Typical incremental offset-voltage shift vs. operating life.

### Power-Supply Considerations

Because the CA3130 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single- and dual-supply service. Figs. 14a and 14b show the CA3130 connected for both dual- and single-supply operation.

**Dual-supply operation:** When the output voltage at Term. 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

**Single-supply operation:** Initially, let it be assumed that the value of  $R_L$  is very high (or disconnected), and that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at  $V^+/2$ , i.e.,

## CA3130A, CA3130

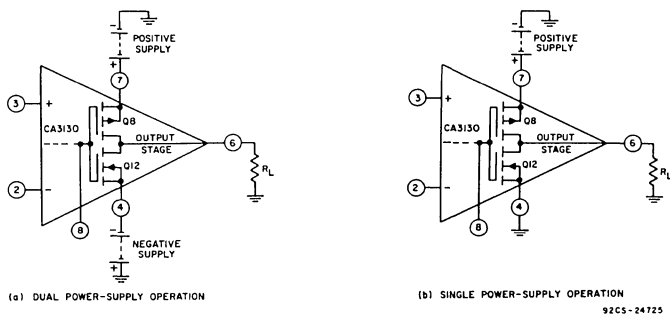


Fig. 14 — CA3130 output stage in dual and single power-supply operation.

the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA3130 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Term. 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA3130, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 14a shows a dual-supply arrangement for the output stage that can also be strobed off, assuming  $R_L = \infty$ , by pulling the potential of Term. 8 down to that of Term. 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Term. 6 and ground in the circuit of Fig. 14b. Let it further be assumed again that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is a  $V^+/2$ . Since PMOS transistor Q8 must now supply quiescent current to both  $R_L$  and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the  $R_L$  magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply-voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

### Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3130 is most advantageous in applications where in the source resistance of the input signal is

in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only  $23 \mu\text{V}$  when the test-circuit amplifier of Fig. 15 is operated at a total supply voltage of 15 volts. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

### TYPICAL APPLICATIONS

#### Voltage Followers

Operational amplifiers with very high input resistances, like the CA3130, are particularly suited to service as voltage followers. Fig. 16 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3130 in a split-supply configuration.

A voltage follower, operated from a single supply, is shown in Fig. 17, together with related waveforms. This follower circuit is

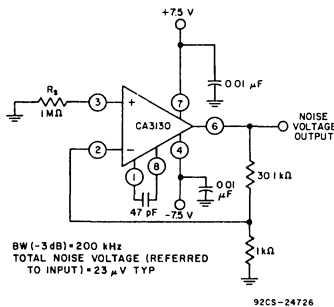
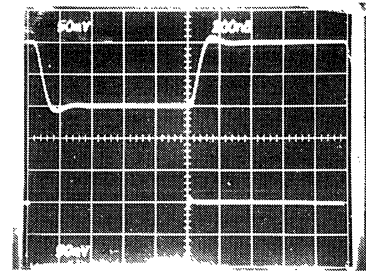
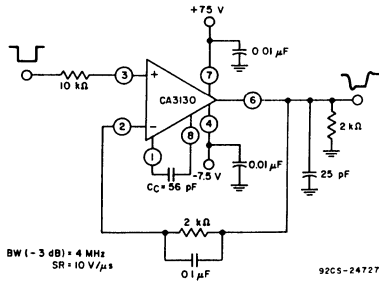
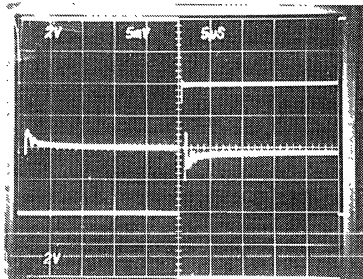


Fig. 15 — Test-circuit amplifier (30-dB gain) used for wideband noise measurements.

## CA3130A, CA3130



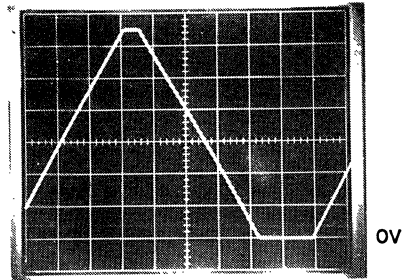
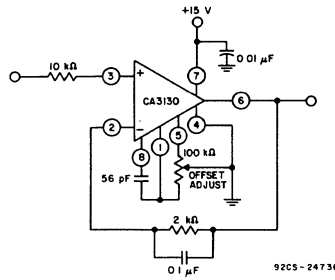
Top Trace: Output  
Bottom Trace: Input  
(a) Small-signal response (50 mV/div. and 200 ns/div.)



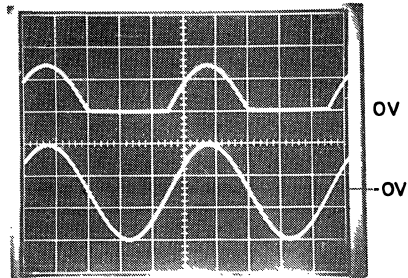
Top Trace: Output signal (2 V/div. and 5 μs/div.)  
Center Trace: Difference signal (5 mV/div. and 5 μs/div.)  
Bottom Trace: Input signal (2 V/div. and 5 μs/div.)  
(b) Input-output difference signal showing settling time (Measurement made with Tektronix 7A13 differential amplifier)

*Fig. 16 — Split-supply voltage follower with associated waveforms.*

linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig. 17a with input-signal ramping. The waveforms in Fig. 17b show that the follower does not lose its input-to-output phase-sense, even though the input is



(a) Output-waveform with input-signal ramping (2 V/div. and 500 μs/div.)



Top Trace: Output (5 V/div. and 200 μs/div.)  
Bottom Trace: Input (5 V/div. and 200 μs/div.)  
(b) Output-waveform with ground-reference sine-wave input

*Fig. 17 — Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig. 9 in ICAN-6080).*

being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig. 17b also shows the manner in which the CMOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3130 in a single-supply voltage-follower application.

## CA3130A, CA3130

### 9-Bit COS/MOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)\* is shown in Fig. 18. This system combines the concepts of multiple-switch CMOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3130 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig. 18.

of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA3130 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with varia-

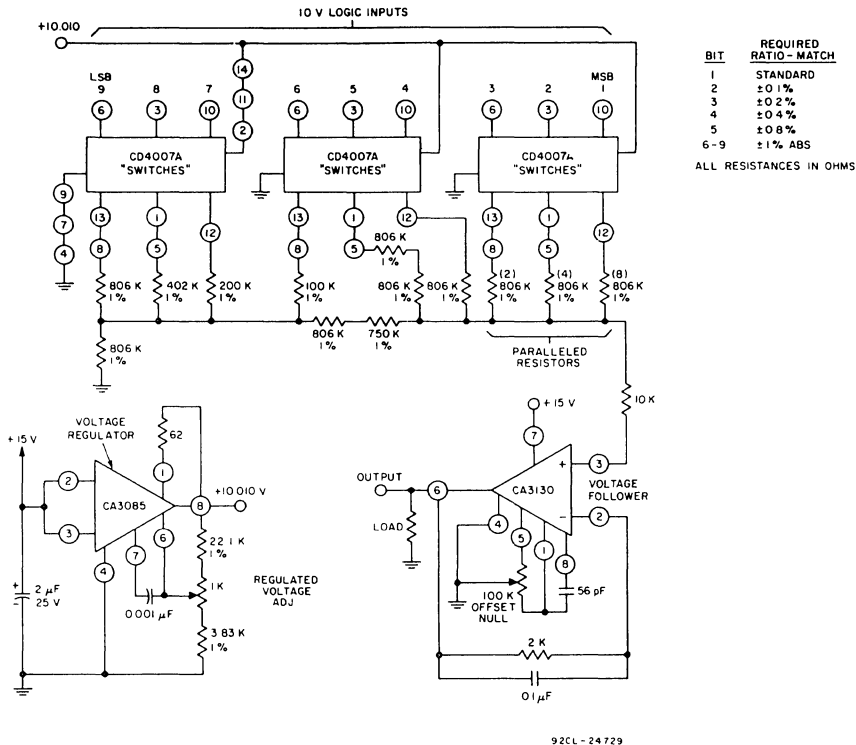


Fig. 18-9-bit DAC using CMOS digital switches and CA3130.

The circuit uses an R/2R voltage-ladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly

tions of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.

### Single-Supply, Absolute-Value, Ideal Full-Wave Rectifier

The absolute-value circuit using the CA3130 is shown in Fig. 19. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a

\* "Digital-to-Analog Conversion Using the Harris CD4007A COS/MOS IC", Application Note ICAN-6080.

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negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3130 functions as a normal inverting amplifier with a gain equal to  $-R2/R1$ . When the equality of the two equations shown in Fig. 19 is satisfied, the full-wave output is symmetrical.

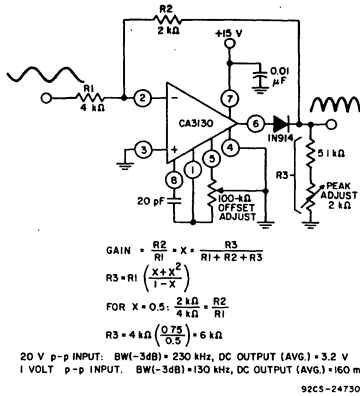
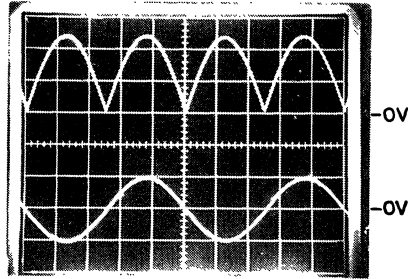


Fig. 19 — Single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.

### Error-Amplifier in Regulated-Power Supplies

The CA3130 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero. Fig. 21 shows the schematic diagram of a 40-mA power supply capable of providing regulated output volt-

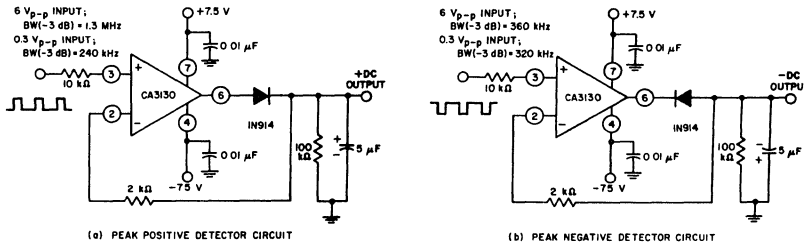


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Top Trace: Output signal (2 V/div.)  
 Bottom Trace: Input signal (10 V/div.)  
 Time base on both traces: 0.2 ms/div.

### Peak Detectors

Peak-detector circuits are easily implemented with the CA3130, as illustrated in Fig. 20 for both the peak-positive and the peak-negative circuit. It should be noted that with large-signal inputs, the bandwidth of the peak-negative circuit is much less than that of the peak-positive circuit. The second stage of the CA3130 limits the bandwidth in this case. Negative-going output-signal excursion requires a positive-going signal excursion at the collector of transistor Q11, which is loaded by the intrinsic capacitance of the associated circuitry in this mode. On the other hand, during a negative-going signal excursion at the collector of Q11, the transistor functions in an active "pull-down" mode so that the intrinsic capacitance can be discharged more expeditiously.



(a) PEAK POSITIVE DETECTOR CIRCUIT

(b) PEAK NEGATIVE DETECTOR CIRCUIT

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Fig. 20 — Peak-detector circuits.

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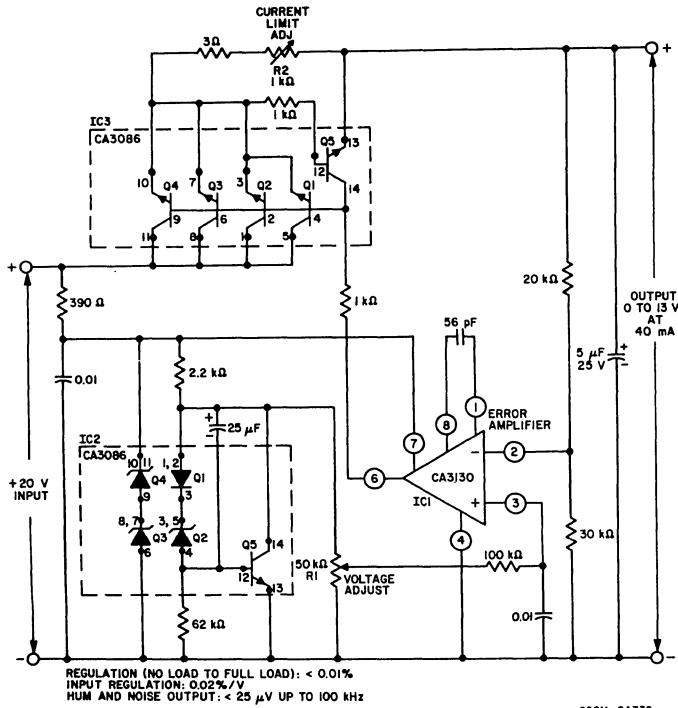


Fig. 21—Voltage regulator circuit (0 to 13 V at 40 mA).

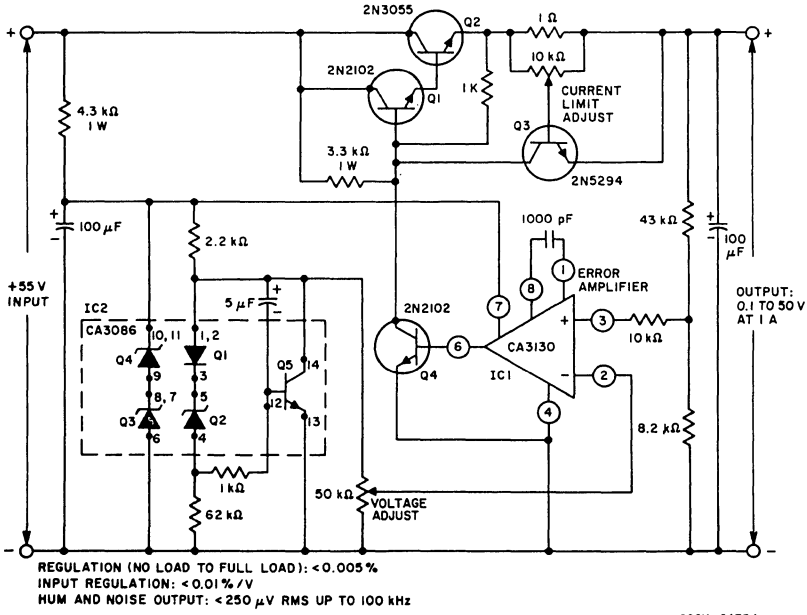


Fig. 22 — Voltage regulator circuit (0.1 to 50 V at 1 A).

## CA3130A, CA3130

justment over the range from 0.1 to 50 volts and currents up to 1 ampere. The error amplifier (IC1) and circuitry associated with IC2 function as previously described, although the output of IC1 is boosted by a discrete transistor (Q4) to provide adequate base drive for the Darlington-connected series-pass transistors Q1, Q2. Transistor Q3 functions in the previously described current-limiting circuit.

### Multivibrators

The exceptionally high input resistance presented by the CA3130 is an attractive feature for multivibrator circuit design because it permits the use of timing circuits with high R/C ratios. The circuit diagram of a pulse generator (astable multivibrator), with provisions for independent control of the "on" and "off" periods, is shown in Fig. 23. Resistors R1 and R2 are used to bias the CA3130 to the mid-point of the supply-voltage and R3 is the feedback resistor. The pulse repetition rate is selected by positioning S1 to the desired position and the rate remains essentially constant when the resistors which determine "on-period" and "off-period" are adjusted.

### Function Generator

Fig. 24 contains a schematic diagram of a function generator using the CA3130 in the integrator and threshold detector functions. This circuit generates a triangular or square-

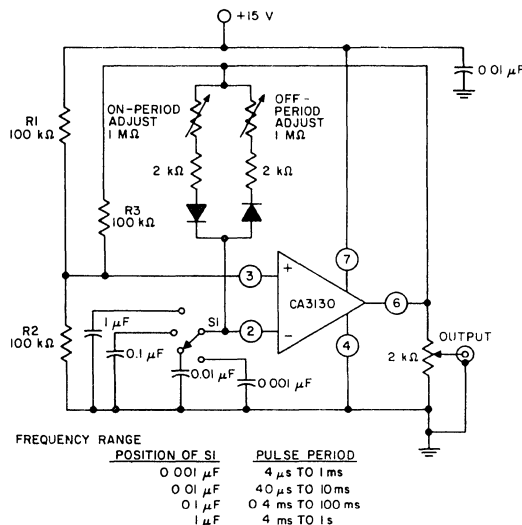
wave output that can be swept over a 1,000,000:1 range (0.1 Hz to 100 kHz) by means of a single control, R1. A voltage-control input is also available for remote sweep-control.

The heart of the frequency-determining system is an operational-transconductance-amplifier (OTA)\*, IC1, operated as a voltage-controlled current-source. The output,  $I_O$ , is a current applied directly to the integrating capacitor, C1, in the feedback loop of the integrator IC2, using a CA3130, to provide the triangular-wave output. Potentiometer R2 is used to adjust the circuit for slope symmetry of positive-going and negative-going signal excursions.

Another CA3130, IC3, is used as a controlled switch to set the excursion limits of the triangular output from the integrator circuit. Capacitor C2 is a "peaking adjustment" to optimize the high-frequency square-wave performance of the circuit.

Potentiometer R3 is adjustable to perfect the "amplitude symmetry" of the square-wave output signals. Output from the threshold detector is fed back via resistor R4 to the input of IC1 so as to toggle the current source from plus to minus in generating the linear triangular wave.

\*See File No. 475 and ICAN-6668.



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Fig. 23 — Pulse generator (astable multivibrator) with provisions for independent control of "ON" and "OFF" periods.

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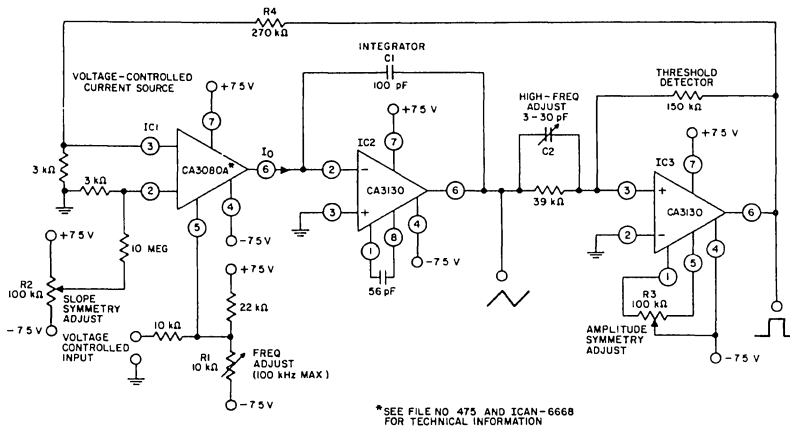


Fig. 24 - Function generator (frequency can be varied 1,000,000/1 with a single control).

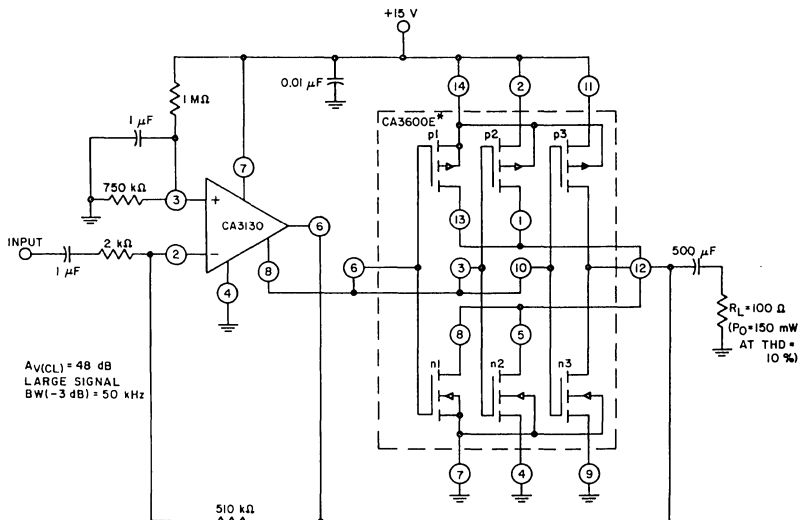
### Operation with Output-Stage Power-Booster

The current-sourcing and -sinking capability of the CA3130 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig. 25, three CMOS transistor-pairs in a single CA3600E IC array are shown parallel connected with the output stage in the CA3130. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of supply current at 15-V

operation. This arrangement boosts the current-handling capability of the CA3130 output stage by about 2.5X.

The amplifier circuit in Fig. 25 employs feedback to establish a closed-loop gain of 48 dB. The typical large-signal bandwidth (-3 dB) is 50 kHz.

\*See File No. 619 for technical information.



NOTE:  
TRANSISTORS p1, p2, p3 AND n1, n2, n3 ARE PARALLEL-CONNECTED WITH Q8 AND Q12, RESPECTIVELY, OF THE CA3130

Fig. 25 - CMOS transistor array (CA3600E) connected as power-booster in the output stage of the CA3130.

3  
OPERATIONAL AMPLIFIERS



August 1991

### Features

- MOSFET Input Stage
  - ▶ Very High Input Impedance ( $Z_{IN}$ )  $-1.5\text{ T}\Omega$  (Typ.)
  - ▶ Very Low Input Current ( $I_I$ )  $-10\text{ pA}$  (Typ.) @  $\pm 15\text{V}$
  - ▶ Wide Common-Mode Input-Voltage Range (VICR)
    - can be Swung 0.5 Volt Below Negative Supply-Voltage Rail
  - ▶ Output Swing Complements Input Common-Mode Range
- Directly Replaces Industry Type 741 in Most Applications

### Applications

- Ground-Referenced Single-Supply Amplifiers in Automobile and Portable Instrumentation
- Sample and Hold Amplifiers
- Long-Duration Timers/Multivibrators (Microseconds-Minutes-Hours)
- Photocurrent Instrumentation
- Peak Detectos
- Active Filters
- Comparators
- Interface in 5V TTL Systems and Other Low-Supply Voltage Systems
- All Standard Operational Amplifier Applications
- Function Generators
- Tone Controls
- Power Supplies
- Portable Instruments
- Intrusion Alarm Systems

### Description

The CA3140A and CA3140 are integrated-circuit operational amplifiers that combine the advantages of high-voltage PMOS transistors with high-voltage bipolar transistors on a single monolithic chip. Because of this unique combination of technologies, this device can now provide designers, for the first time, with the special performance features of the CA3130 CMOS operational amplifiers and the versatility of the 741 series of industry-standard operational amplifiers.

The CA3140A and CA3140 BiMOS operational amplifiers feature gate-protected MOSFET (PMOS) transistors in the input circuit to provide very-high-input impedance, very-low-input current, and high-speed performance. The CA3140A and CA3140 operate at supply voltage from 4 to 36 volts (either single or dual supply). These operational amplifiers are internally phase-compensated to achieve stable operation in unity-gain follower operation, and additionally, have access terminal for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset-voltage nulling. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute for single-supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load-terminal short-circuiting to either supply-rail or to ground.

The CA3140 Series has the same 8-lead terminal pin-out used for the "741" and other industry-standard operational amplifiers. They are supplied in either the standard 8-lead TO-5 style package (T suffix), or in the 8-lead dual-in-line formed-lead TO-5 style package "DIL-CAN" (S suffix). The CA3140 is available in chip form (H suffix). The CA3140A and CA3140 are also available in an 8-lead Small Outline package (M suffix) and in an 8-lead dual-in-line plastic package (MINI-DIP - E suffix). The CA3140A and CA3140 are intended for operation at supply voltage up to 36 volts ( $\pm 18$  volts). All types can be operated safely over the temperature range from  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .

### Pinouts

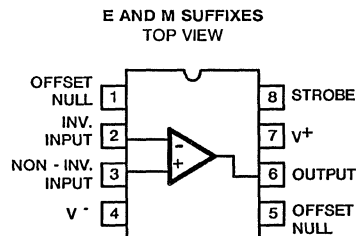
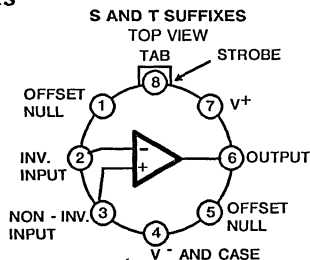


FIGURE 1.

## CA3140A, CA3140

### TYPICAL ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC   | TEST CONDITIONS   |   | CA3140A<br>(T, S, E, M) | CA3140<br>(T, S, E, M) | UNITS                        |
|--|---|---|-------------------------|------------------------|------------------------------|
|  | $V^+ = +15\text{ V}$<br>$V^- = -15\text{ V}$<br>$T_A = 25^\circ\text{C}$        |   |                         |                        |                              |
| Input Offset Voltage Adjustment Resistor                           | Typ. Value of Resistor Between Term. 4 and 5 or 4 and 1 to Adjust Max. $V_{IO}$ |   | 18                      | 4.7                    | $k\Omega$                    |
| Input Resistance $R_I$   |   |   | 1.5                     | 1.5                    | $T\Omega$                    |
| Input Capacitance $C_I$  |   |   | 4                       | 4                      | pF                           |
| Output Resistance $R_O$  |   |   | 60                      | 60                     | $\Omega$                     |
| Equivalent Wideband Input Noise Voltage (See Fig. 39)              | $e_n$   | BW = 140 kHz<br>$R_S = 1\text{ M}\Omega$                              | 48                      | 48                     | $\mu\text{V}$                |
| Equivalent Input Noise Voltage (See Fig. 10)                       | $e_n$   | $f = 1\text{ kHz}$ $R_S =$  | 40                      | 40                     | $n\text{V}/\sqrt{\text{Hz}}$ |
|  |   | $f = 10\text{ kHz}$ $100\ \Omega$                                     | 12                      | 12                     |                              |
| Short-Circuit Current to Opposite Supply Source<br>Sink $I_{OM}^-$ | $I_{OM}^+$  |   | 40                      | 40                     | mA                           |
|  | $I_{OM}^-$  |   | 18                      | 18                     | mA                           |
| Gain-Bandwidth Product, (See Figs. 5 & 18)                         | $f_T$   |   | 4.5                     | 4.5                    | MHz                          |
| Slew Rate, (See Fig. 6)  | SR  |   | 9                       | 9                      | $\text{V}/\mu\text{s}$       |
| Sink Current From Terminal 8 To Terminal 4 to Swing Output Low     |   |   | 220                     | 220                    | $\mu\text{A}$                |
| Transient Response:<br>Rise Time<br>Overshoot (See Fig. 37)        | $t_r$   | $R_L = 2\text{ k}\Omega$<br>$C_L = 100\text{ pF}$                     | 0.08                    | 0.08                   | $\mu\text{s}$                |
|  |   |   | 10                      | 10                     | %                            |
| Settling Time at $10\text{ V}_{p-p}$ , (See Fig. 17)               | $1\text{ mV}$   | $R_L = 2\text{ k}\Omega$<br>$C_L = 100\text{ pF}$<br>Voltage Follower | 4.5                     | 4.5                    | $\mu\text{s}$                |
|  | $10\text{ mV}$  |   | 1.4                     | 1.4                    |                              |

## CA3140A, CA3140

### ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At  $V^+ = 15\text{ V}$ ,  $V^- = 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$  Unless Otherwise Specified

| CHARACTERISTIC  | LIMITS     |                      |       |        |                      |       | UNITS                        |
|---|------------|----------------------|-------|--------|----------------------|-------|------------------------------|
|   | CA3140A    |                      |       | CA3140 |                      |       |                              |
|   | Min.       | Typ.                 | Max.  | Min.   | Typ.                 | Max.  |                              |
| Input Offset Voltage, $ V_{IO} $                                  | –          | 2                    | 5     | –      | 5                    | 15    | mV                           |
| Input Offset Current, $ I_{IO} $                                  | –          | 0.5                  | 20    | –      | 0.5                  | 30    | pA                           |
| Input Current, $I_I$  | –          | 10                   | 40    | –      | 10                   | 50    | pA                           |
| Large-Signal<br>Voltage Gain, $A_{OL}$ •<br>(See Figs. 4, 18)     | 20 k       | 100 k                | –     | 20 k   | 100 k                | –     | V/V                          |
|   | 86         | 100                  | –     | 86     | 100                  | –     | dB                           |
| Common-Mode<br>Rejection Ratio, CMRR<br>(See Fig. 9)              | –          | 32                   | 320   | –      | 32                   | 320   | $\mu\text{V/V}$              |
|   | 70         | 90                   | –     | 70     | 90                   | –     | dB                           |
| Common-Mode<br>Input-Voltage<br>Range, $V_{ICR}$<br>(See Fig. 20) | –15        | –15.5<br>to<br>+12.5 | 12    | –15    | –15.5<br>to<br>+12.5 | 11    | V                            |
| Power-Supply<br>Rejection<br>Ratio, PSRR<br>(See Fig. 11)         | –          | 100                  | 150   | –      | 100                  | 150   | $\mu\text{V/V}$              |
|   | 76         | 80                   | –     | 76     | 80                   | –     | dB                           |
| Max. Output<br>Voltage ■<br>(See Figs. 13, 20)                    | $V_{OM}^+$ | +12                  | 13    | –      | +12                  | 13    | V                            |
|   | $V_{OM}^-$ | –14                  | –14.4 | –      | –14                  | –14.4 |                              |
| Supply Current, $I^+$<br>(See Fig. 7)                             | –          | 4                    | 6     | –      | 4                    | 6     | mA                           |
| Device Dissipation, $P_D$   | –          | 120                  | 180   | –      | 120                  | 180   | mW                           |
| Input Offset Voltage<br>Temp. Drift, $\Delta V_{IO}/\Delta T$     | –          | 6                    | –     | –      | 8                    | –     | $\mu\text{V}/^\circ\text{C}$ |

• At  $V_O = 26V_{p-p}$ , +12V, –14V and  $R_L = 2\text{ k}\Omega$ .

■ At  $R_L = 2\text{ k}\Omega$ .

## CA3140A, CA3140

### MAXIMUM RATINGS, *Absolute-Maximum Values:*

CA3140, CA3140A

|  |  |
|--|--|
| DC SUPPLY VOLTAGE<br>(BETWEEN V <sup>+</sup> AND V <sup>-</sup> TERMINALS) ..... | 36 V   |
| DIFFERENTIAL-MODE INPUT VOLTAGE .....  | ± 8 V  |
| COMMON-MODE DC INPUT VOLTAGE .....   | (V <sup>+</sup> +8 V) to (V <sup>-</sup> -0.5 V) |
| INPUT-TERMINAL CURRENT .....   | 1 mA   |
| DEVICE DISSIPATION:  |  |
| WITHOUT HEAT SINK -  |  |
| UP TO 55°C .....   | 630 mW   |
| ABOVE 55°C .....   | Derate linearly 6.67 mW/°C                       |
| WITH HEAT SINK -   |  |
| UP TO 55°C .....   | 1 W  |
| ABOVE 55°C .....   | Derate linearly 16.7 mW/°C                       |
| TEMPERATURE RANGE:   |  |
| OPERATING (ALL TYPES) .....  | -55 to +125°C                                    |
| STORAGE (ALL TYPES) .....  | -65 to +150°C                                    |
| OUTPUT SHORT-CIRCUIT DURATION* .....   | INDEFINITE                                       |
| LEAD TEMPERATURE (DURING SOLDERING):   |  |
| AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM)                                    |  |
| FROM CASE FOR 10 SECONDS MAX. ....   | +265°C   |

\* Short circuit may be applied to ground or to either supply.

### TYPICAL ELECTRICAL CHARACTERISTICS FOR DESIGN GUIDANCE

At V<sup>+</sup> = 5 V, V<sup>-</sup> = 0 V, T<sub>A</sub> = 25°C

| CHARACTERISTIC   | CA3140A<br>(T, S, E, M)      | CA3140<br>(T, S, E, M) | UNITS |
|--|------------------------------|------------------------|-------|
| Input Offset Voltage  V <sub>IO</sub>                          | 2                            | 5                      | mV    |
| Input Offset Current  I <sub>IO</sub>                          | 0.1                          | 0.1                    | pA    |
| Input Current I <sub>I</sub>                                   | 2                            | 2                      | pA    |
| Input Resistance   | 1                            | 1                      | TΩ    |
| Large-Signal Voltage Gain<br>(See Figs.4,18)                   | A <sub>OL</sub>              | 100 k                  | 100 k |
|  |                              | 100                    | 100   |
| Common-Mode Rejection Ratio, CMRR                              |                              | 32                     | 32    |
|  |                              | 90                     | 90    |
| Common-Mode Input-Voltage Range<br>(See Fig.20)                | V <sub>ICR</sub>             | -0.5                   | -0.5  |
|  |                              | 2.6                    | 2.6   |
| Power-Supply Rejection Ratio ΔV <sub>IO</sub> /ΔV <sup>+</sup> |                              | 100                    | 100   |
|  |                              | 80                     | 80    |
| Maximum Output Voltage<br>(See Figs.13,20)                     | V <sub>OM</sub> <sup>+</sup> | 3                      | 3     |
|  | V <sub>OM</sub> <sup>-</sup> | 0.13                   | 0.13  |
| Maximum Output Current:<br>Source                              | I <sub>OM</sub> <sup>+</sup> | 10                     | 10    |
|  | I <sub>OM</sub> <sup>-</sup> | 1                      | 1     |
| Slew Rate (See Fig.6)  |                              | 7                      | 7     |
| Gain-Bandwidth Product (See Fig.5)                             | f <sub>T</sub>               | 3.7                    | 3.7   |
| Supply Current (See Fig.7)                                     | I <sup>+</sup>               | 1.6                    | 1.6   |
| Device Dissipation   | P <sub>D</sub>               | 8                      | 8     |
| Sink Current from Term. 8 to<br>Term. 4 to Swing Output Low    |                              | 200                    | 200   |

# CA3140A, CA3140

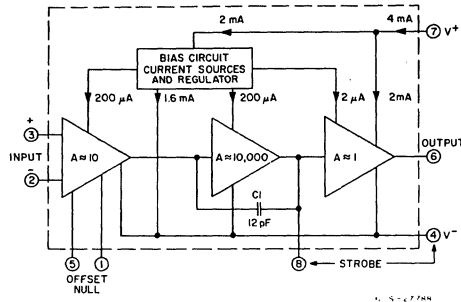


Fig.2 — Block diagram of CA3140 series.

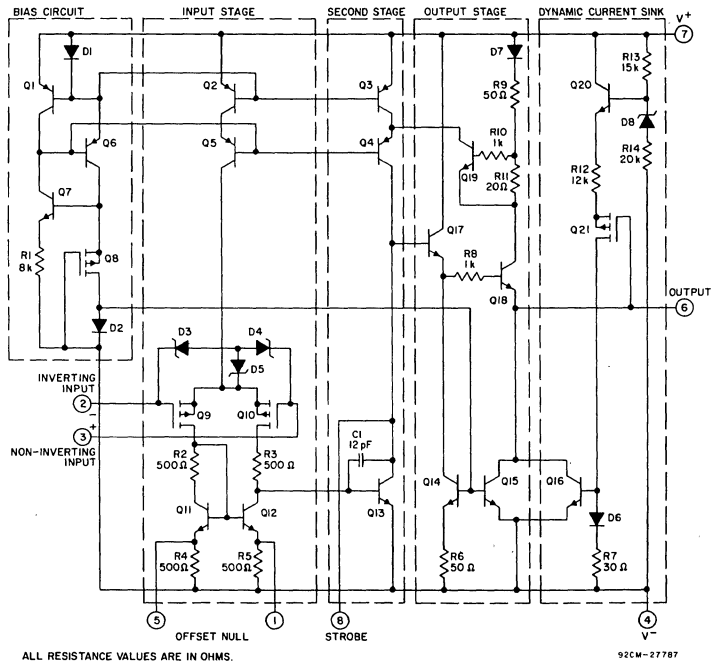


Fig.3 — Schematic diagram of CA3140 series.

## CIRCUIT DESCRIPTION

Fig.2 is a block diagram of the CA3140 Series PMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail. Two class A amplifier stages provide the voltage gain, and a unique class AB amplifier stage provides the current gain necessary to drive low-impedance loads.

A biasing circuit provides control of cascoded constant-current flow circuits in the first and second stages. The CA3140 includes an on-

chip phase-compensating capacitor that is sufficient for the unity gain voltage-follower configuration.

**Input Stages** — The schematic circuit diagram of the CA3140 is shown in Fig.3. It consists of a differential-input stage using PMOS field-effect transistors (Q9, Q10) working into a mirror pair of bipolar transistors (Q11, Q12) functioning as load resistors together with resistors R2 through R5. The mirror-pair transistors also function as a differen-

tial-to-single-ended converter to provide base-current drive to the second-stage bipolar transistor (Q13). Offset nulling, when desired, can be effected with a 10-k $\Omega$  potentiometer connected across terminals 1 and 5 and with its slider arm connected to terminal 4. Cascode-connected bipolar transistors Q2, Q5 are the constant-current source for the input stage. The base-biasing circuit for the constant-current source is described subsequently. The small diodes D3, D4, D5 provide gate-oxide protection against high-voltage transients, e.g., static electricity.

**Second Stage** — Most of the voltage gain in the CA3140 is provided by the second amplifier stage, consisting of bipolar transistor Q13 and its cascode-connected load resistance provided by bipolar transistors Q3, Q4. On-chip phase compensation, sufficient for a majority of the applications is provided by C1. Additional Miller-Effect compensation (roll-off) can be accomplished, when desired, by simply connecting a small capacitor between terminals 1 and 8. Terminal 8 is also used to strobe the output stage into quiescence. When terminal 8 is tied to the negative supply rail (terminal 4) by mechanical or electrical means, the output terminal 6 swings low, i.e., approximately to terminal 4 potential.

**Output Stage** — The CA3140 Series circuits employ a broadband output stage that can sink loads to the negative supply to complement the capability of the PMOS input stage when operating near the negative rail. Quiescent current in the emitter-follower cascode circuit (Q17, Q18) is established by transistors (Q14, Q15) whose base-currents are "mirrored" to current flowing through diode D2 in the bias circuit section. When the CA3140 is operating such that output terminal 6 is sourcing current, transistor Q18 functions as an emitter-follower to source current from the V+ bus (terminal 7), via D7, R9, and R11. Under these conditions, the collector potential of Q13 is sufficiently high to permit the necessary flow of base current to emitter follower Q17 which, in turn, drives Q18.

When the CA3140 is operating such that output terminal 6 is sinking current to the V- bus, transistor Q16 is the current-sinking

element. Transistor Q16 is mirror-connected to D6, R7, with current fed by way of Q21, R12, and Q20. Transistor Q20, in turn, is biased by current-flow through R13, zener D8, and R14. The dynamic current-sink is controlled by voltage-level sensing. For purposes of explanation, it is assumed that output terminal 6 is quiescently established at the potential mid-point between the V+ and V- supply rails. When output-current sinking-mode operation is required, the collector potential of transistor Q13 is driven below its quiescent level, thereby causing Q17, Q18 to decrease the output voltage at terminal 6. Thus, the gate terminal of PMOS transistor Q21 is displaced toward the V- bus, thereby reducing the channel resistance of Q21. As a consequence, there is an incremental increase in current flow through Q20, R12, Q21, D6, R7, and the base of Q16. As a result, Q16 sinks current from terminal 6 in direct response to the incremental change in output voltage caused by Q18. This sink current flows regardless of load; any excess current is internally supplied by the emitter-follower Q18. Short-circuit protection of the output circuit is provided by Q19, which is driven into conduction by the high voltage drop developed across R11 under output short-circuit conditions. Under these conditions, the collector of Q19 diverts current from Q4 so as to reduce the base-current drive from Q17, thereby limiting current flow in Q18 to the short-circuited load terminal.

**Bias Circuit** — Quiescent current in all stages (except the dynamic current sink) of the CA3140 is dependent upon bias current flow in R1. The function of the bias circuit is to establish and maintain constant-current flow through D1, Q6, Q8 and D2. D1 is a diode-connected transistor mirror-connected in parallel with the base-emitter junctions of Q1, Q2, and Q3. D1 may be considered as a current-sampling diode that senses the emitter current of Q6 and automatically adjusts the base current of Q6 (via Q1) to maintain a constant current through Q6, Q8, D2. The base-currents in Q2, Q3 are also determined by constant-current flow D1. Furthermore, current in diode-connected transistor D2 establishes the currents in transistors Q14 and Q15.

# CA3140A, CA3140

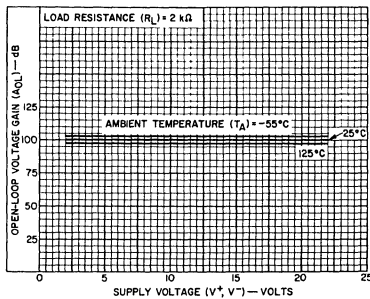


Fig. 4 - Open-loop voltage gain vs supply voltage and temperature.

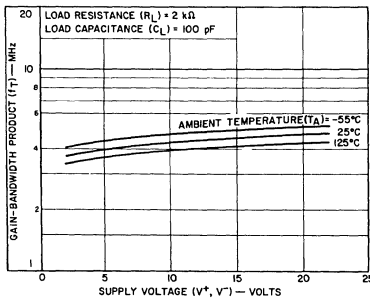


Fig. 5 - Gain-bandwidth product vs supply voltage and temperature.

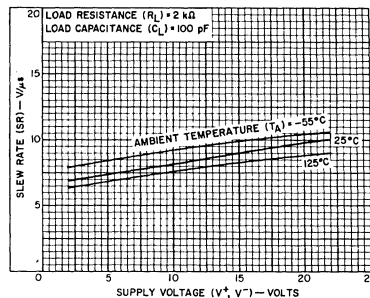


Fig. 6 - Slew rate vs supply voltage and temperature.

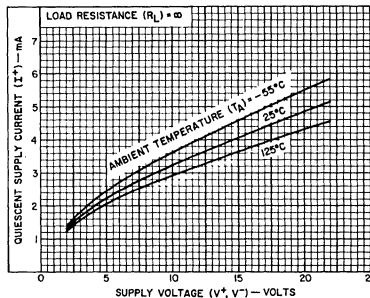


Fig. 7 - Quiescent supply current vs supply voltage and temperature.

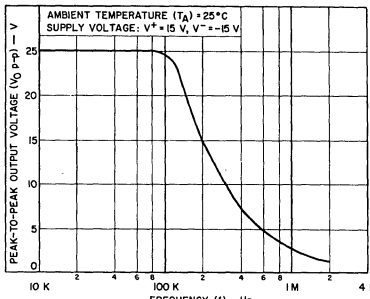


Fig. 8 - Maximum output voltage swing vs frequency.

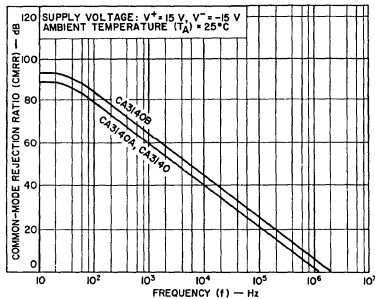


Fig. 9 - Common-mode rejection ratio vs frequency.

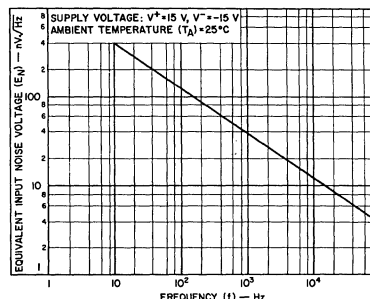


Fig. 10 - Equivalent input noise voltage vs frequency.

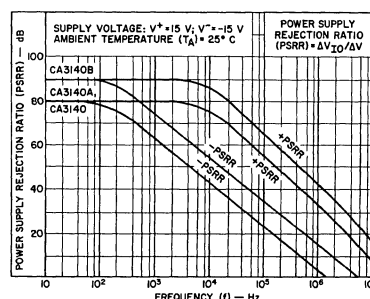


Fig. 11 - Power supply rejection ratio vs frequency.

## APPLICATIONS CONSIDERATIONS

Wide dynamic range of input and output characteristics with the most desirable high input-impedance characteristic is achieved in the CA3140 by the use of a unique design based upon the PMOS-Bipolar process. Input-common-mode voltage range and output-swing capabilities are complementary, allowing operation with the single supply down to four volts.

The wide dynamic range of these parameters also means that this device is suitable for many single-supply applications, such as, for example, where one input is driven below the potential of terminal 4 and the phase sense of the output signal must be maintained — a most important consideration in comparator applications.

### OUTPUT CIRCUIT CONSIDERATIONS

Excellent interfacing with TTL circuitry is easily achieved with a single 6.2-volt zener diode connected to terminal 8 as shown in Fig.12. This connection assures that the maximum output signal swing will not go more positive than the zener voltage minus two base-to-emitter voltage drops within the CA3140. These voltages are independent of the operating supply voltage.

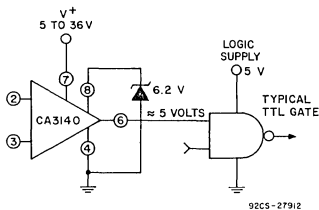


Fig.12 — Zener clamping diode connected to terminals 8 and 4 to limit CA3140 output swing to TTL levels.

Fig.13 shows output current-sinking capabilities of the CA3140 at various supply voltages. Output voltage swing to the negative supply rail permits this device to oper-

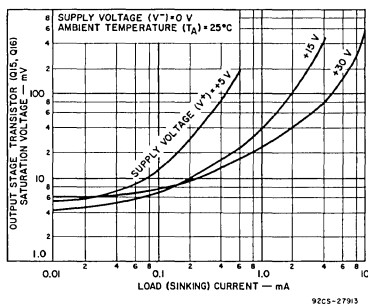


Fig.13 — Voltage across output transistors Q15 and Q16 vs load current.

ate both power transistors and thyristors directly without the need for level-shifting circuitry usually associated with the 741 series of operational amplifiers.

Fig.16 show some typical configurations. Note that a series resistor, R<sub>L</sub>, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

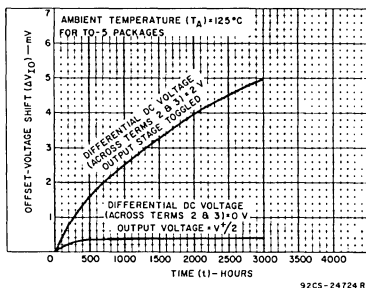


Fig.14 — Typical incremental offset-voltage shift vs operating life.

### OFFSET-VOLTAGE NULLING

The input-offset voltage can be nulled by connecting a 10-kΩ potentiometer between terminals 1 and 5 and returning its wiper arm to terminal 4, see Fig.15a. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors that may be placed at either end of the potentiometer, see Fig.15b, to optimize its utilization range are given in the table "Typical Electrical Characteristics" shown in this bulletin.

An alternate system is shown in Fig.15c. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to zero ohms at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

### LOW-VOLTAGE OPERATION

Operation at total supply voltages as low as 4 volts is possible with the CA3140. A current regulator based upon the PMOS threshold voltage maintains reasonable constant operating current and hence consistent performance down to these lower voltages.

The low-voltage limitation occurs when the upper extreme of the input common-mode voltage range extends down to the voltage at terminal 4. This limit is reached at a total



# CA3140A, CA3140

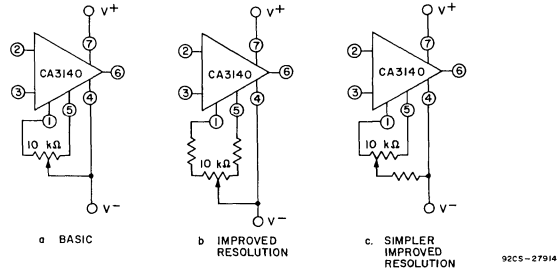


Fig.15 — Three offset-voltage nulling methods.

supply voltage just below 4 volts. The output voltage range also begins to extend down to the negative supply rail, but is slightly higher than that of the input. Fig.20 shows these characteristics and shows that with 2-volt dual supplies, the lower extreme of the input common-mode voltage range is below ground potential.

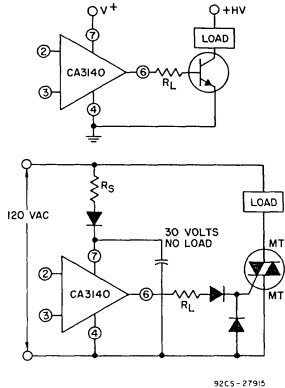


Fig.16 — Methods of utilizing the  $V_{CE(sat)}$  sinking-current capability of the CA3140 series.

## BANDWIDTH AND SLEW RATE

For those cases where bandwidth reduction is desired, for example, broadband noise reduction, an external capacitor connected between terminals 1 and 8 can reduce the open-loop  $-3$  dB bandwidth. The slew rate will, however, also be proportionally reduced by using this additional capacitor. Thus, a 20% reduction in bandwidth by this technique will also reduce the slew rate by about 20%.

Fig.17 shows the typical settling time required to reach 1 mV or 10 mV of the final value for various levels of large signal inputs for the voltage-follower and inverting unity-gain amplifiers. The exceptionally fast settling time characteristics are largely due to the high combination of high gain and wide bandwidth of the CA3140; as shown in Fig. 18.

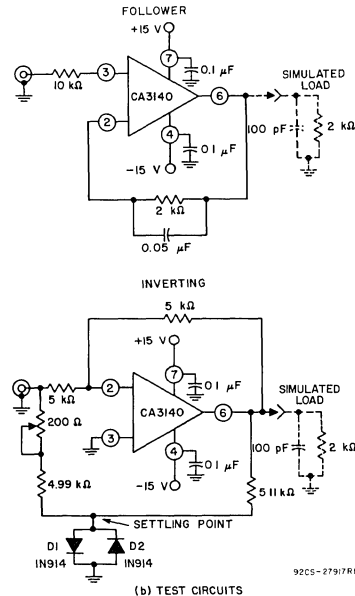
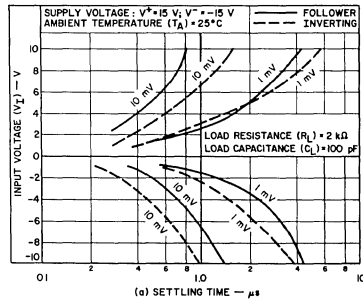


Fig.17 — Input voltage vs settling time.

## INPUT CIRCUIT CONSIDERATIONS

As mentioned previously, the amplifier inputs can be driven below the terminal 4 potential, but a series current-limiting re-

# CA3140A, CA3140

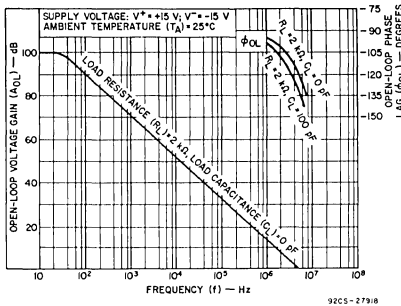


Fig. 18 — Open-loop voltage gain and phase lag vs frequency.

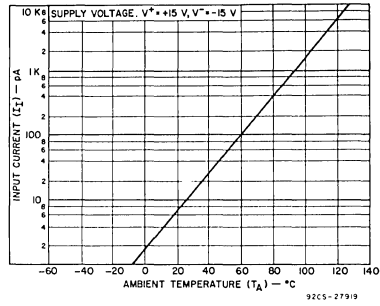


Fig. 19 — Input current vs ambient temperature.

sistor is recommended to limit the maximum input terminal current to less than 1 mA to prevent damage to the input protection circuitry.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3140 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9-kΩ resistor is sufficient.

The typical input current is in the order of 10 pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Fig. 19 shows typical input-terminal current versus ambient temperature for the CA3140.

It is well known that MOS/FET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. Fig. 14 shows the typical offset voltage change as a function of various stress voltages at the maximum rating of 125°C (for TO-5); at lower temperatures (TO-5 and plastic), for example, at 85°C, this change in voltage is considerably less. In typical linear applications, where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar a transistor input stage.

### SUPER SWEEP FUNCTION GENERATOR

A function generator having a wide tuning range is shown in Fig. 21. The 1,000,000/1

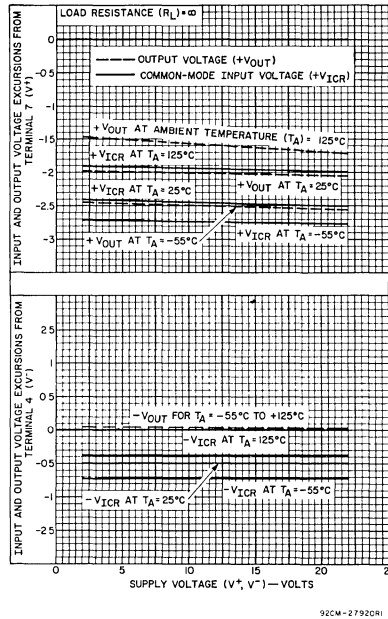


Fig. 20 — Output-voltage-swing capability and common-mode input-voltage range vs supply voltage and temperature.

adjustment range is accomplished by a single variable potentiometer or by an auxiliary sweeping signal. The CA3140 functions as a non-inverting read-out amplifier of the triangular signal developed across the integrating capacitor network connected to the output of the CA3080A current source.

Buffered triangular output signals are then applied to a second CA3080 functioning as a high-speed hysteresis switch. Output from the switch is returned directly back to the

## CA3140A, CA3140

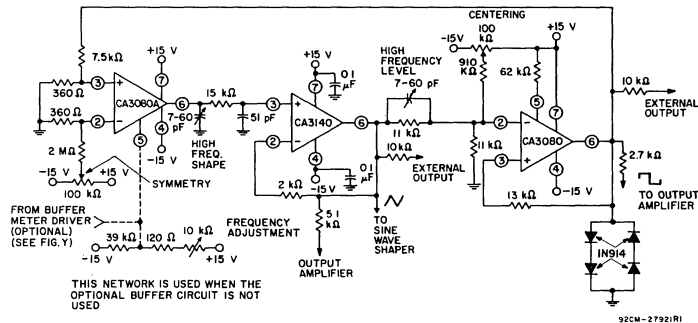
input of the CA3080A current source, thereby, completing the positive feedback loop.

The triangular output level is determined by the four 1N914 level-limiting diodes of the second CA3080 and the resistor-divider network connected to terminal No.2 (input) of the CA3080. These diodes establish the input trip level to this switching stage and, therefore, indirectly determine the amplitude of the output triangle.

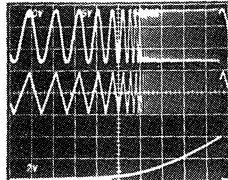
Compensation for propagation delays around the entire loop is provided by one adjust-

ment on the input of the CA3080. This adjustment, which provides for a constant generator amplitude output, is most easily made while the generator is sweeping. High-frequency ramp linearity is adjusted by the single 7-to-60 pF capacitor in the output of the CA3080A.

It must be emphasized that only the CA3080A is characterized for maximum output linearity in the current-generator function.



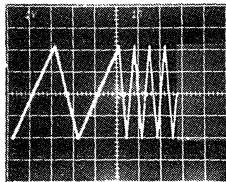
(a) Circuit



TOP TRACE: OUTPUT AT JUNCTION OF 2.7 kΩ AND 51 Ω RESISTORS  
5 V/DIV AND 500 ms/DIV  
CENTER TRACE: EXTERNAL OUTPUT OF TRIANGULAR FUNCTION GENERATOR  
2 V/DIV AND 500 ms/DIV  
BOTTOM TRACE: OUTPUT OF "LOG" GENERATOR  
10 V/DIV AND 500 ms/DIV

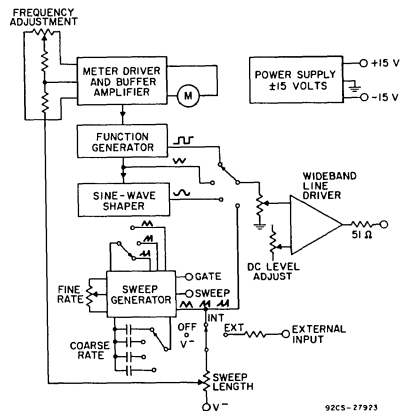
92CS-27922

(b1) Function generator sweeping



92CS-27937

(b2) Function generator with fixed frequencies



(c) Interconnections

1V/DIV and 1 sec/DIV

Three tone test signals, highest frequency  $\geq 0.5$  MHz. Note the slight asymmetry at the three-second/cycle signal. This asymmetry is due to slightly different positive and negative integration from the CA3080A and from the pc board and component leakages at the 100-pA level.

Fig.21 - Function generator.

## CA3140A, CA3140

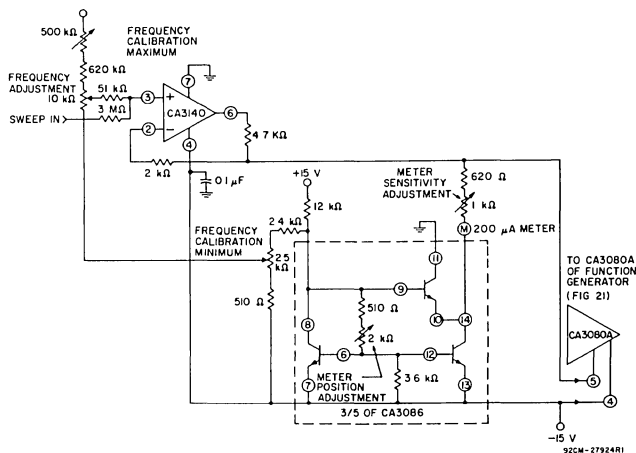


Fig. 22 — Meter driver and buffer amplifier.

### METER DRIVER AND BUFFER AMPLIFIER

Fig. 22 shows the CA3140 connected as a meter driver and buffer amplifier. Low driving impedance is required of the CA3080A current source to assure smooth operation of the Frequency Adjustment Control. This low-driving impedance requirement is easily met by using a CA3140 connected as a voltage follower. Moreover, a meter may be placed across the input to the CA3080A to give a logarithmic analog indication of the function generators frequency.

Analog frequency readout is readily accomplished by the means described above because the output current of the CA3080A varies approximately one decade for each 60-mV change in the applied voltage,  $V_{ABC}$  (voltage between terminals 5 and 4 of the CA3080A of the function generator). Therefore, six decades represent 360-mV change in  $V_{ABC}$ .

Now, only the reference voltage must be established to set the lower limit on the meter. The three remaining transistors from the CA3086 Array used in the sweep generator are used for this reference voltage. In addition, this reference generator arrangement tends to track ambient temperature variations, and thus compensates for the effects of the normal negative temperature coefficient of the CA3080A  $V_{ABC}$  terminal voltage.

Another output voltage from the reference generator is used to insure temperature tracking of the lower end of the Frequency Adjustment Potentiometer. A large series resistance simulates a current source, assuring similar temperature coefficients at both ends of the Frequency Adjustment Control.

To calibrate this circuit, set the Frequency Adjustment Potentiometer at its low end. Then adjust the Minimum Frequency Calibration Control for the lowest frequency. To establish the upper frequency limit, set the Frequency Adjustment Potentiometer to its upper end and then adjust the Maximum Frequency Calibration Control for the maximum frequency. Because there is interaction among these controls, repetition of the adjustment procedure may be necessary.

Two adjustments are used for the meter. The meter sensitivity control sets the meter-scale width of each decade, while the meter position control adjusts the pointer on the scale with negligible effect on the sensitivity adjustment. Thus, the meter sensitivity adjustment control calibrates the meter so that it deflects 1/6 of full scale for each decade change in frequency.

### SINE-WAVE SHAPER

The circuit shown in Fig. 23 uses a CA3140 as a voltage follower in combination with diodes from the CA3019 Array to convert the triangular signal from the function generator to a sine-wave output signal having typically less than 2% THD. The basic zero-crossing slope is established by the 10-k $\Omega$  potentiometer connected between terminals 2 and 6 of the CA3140 and the 9.1-k $\Omega$  resistor and 10-k $\Omega$  potentiometer from terminal 2 to ground. Two break points are established by diodes  $D_1$  through  $D_4$ . Positive feedback via  $D_5$  and  $D_6$  establishes the zero slope at the maximum and minimum levels of the sine wave. This technique is necessary because the voltage-follower configuration approaches unity gain rather than the zero gain required to shape the sine wave at the two extremes.

## CA3140A, CA3140

This circuit can be adjusted most easily with a distortion analyzer, but a good first approximation can be made by comparing the output signal with that of a sine-wave generator. The initial slope is adjusted with the potentiometer R1, followed by an adjustment of R2. The final slope is established by adjusting R3, thereby adding additional segments that are contributed by these diodes. Because there is some interaction among these controls, repetition of the adjustment procedure may be necessary.

### SWEEPING GENERATOR

Fig. 24 shows a sweeping generator. Three CA3140's are used in this circuit. One CA3140 is used as an integrator, a second device is used as a hysteresis switch that determines the starting and stopping points of the sweep. A third CA3140 is used as a logarithmic shaping network for the log function. Rates and slopes, as well as sawtooth, triangle, and logarithmic sweeps are generated by this circuit.

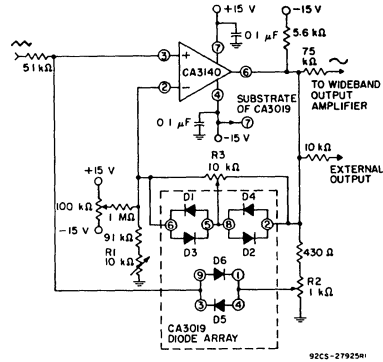


Fig. 23 — Sine-wave shaper.

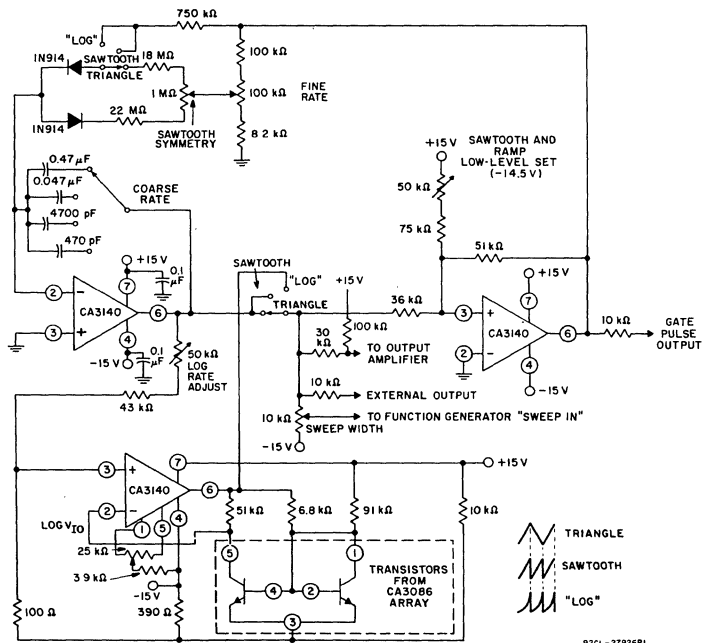


Fig. 24 — Sweeping generator.

## CA3140A, CA3140

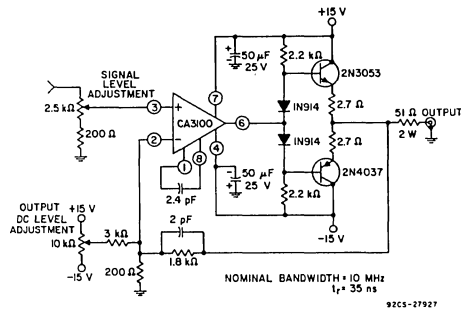


Fig. 25 — Wideband output amplifier.

### WIDEBAND OUTPUT AMPLIFIER

Fig. 25 shows a high-slew-rate, wideband amplifier suitable for use as a 50-ohm transmission-line driver. This circuit, when used in conjunction with the function generator and sine-wave shaper circuits shown in Figs. 21 and 23 provides 18 volts peak-to-peak output open-circuited, or 9 volts peak-to-peak output when terminated in 50 ohms. The slew rate required of this amplifier is 28 volts/ $\mu$ s (18 volts peak-to-peak  $\times \pi \times 0.5$  MHz).

### POWER SUPPLIES

High input-impedance, common-mode capability down to the negative supply and high output-drive current capability are key factors in the design of wide-range output-voltage supplies that use a single input voltage to provide a regulated output voltage that can be adjusted from essentially 0 to 24 volts. Unlike many regulator systems using comparators having a bipolar transistor-input stage, a high-impedance reference-voltage divider from a single supply can be used in connection with the CA3140 (see Fig. 26).

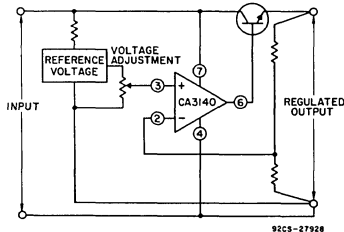


Fig. 26 — Basic single-supply voltage regulator showing voltage-follower configuration.

Essentially, the regulators, shown in Figs. 27 and 28, are connected as non-inverting power operational amplifiers with a gain of 3.2. An 8-volt reference input yields a maximum output voltage slightly greater than 25 volts. As a voltage follower, when the reference input goes to 0 volts the output will be 0 volts. Because the offset voltage is also multiplied by the 3.2 gain factor, a potentiometer is needed to null the offset voltage.

Series pass transistors with high  $I_{CBO}$  levels will also prevent the output voltage from reaching zero because there is a finite voltage drop ( $V_{CEsat}$ ) across the output of the CA3140 (see Fig. 13). This saturation voltage level may indeed set the lowest voltage obtainable.

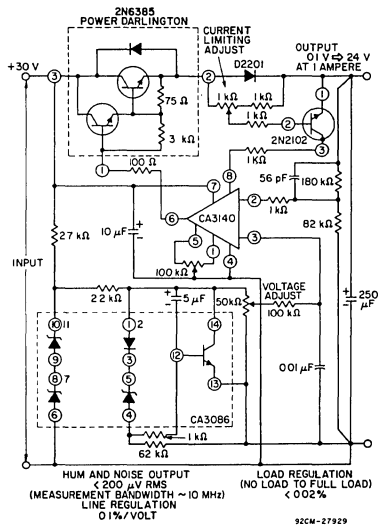


Fig. 27 — Regulated power supply.

## CA3140A, CA3140

The high impedance presented by terminal 8 is advantageous in effecting current limiting. Thus, only a small signal transistor is required for the current-limit sensing amplifier. Resistive decoupling is provided for this transistor to minimize damage to it or the CA3140 in the event of unusual input or output transients on the supply-rail.

Figs. 27 and 28, show circuits in which a D2201 high-speed diode is used for the current sensor. This diode was chosen for its slightly higher forward-voltage drop characteristic thus giving greater sensitivity. It must be emphasized that heat sinking of this diode is essential to minimize variation of the current trip point due to internal heating of the diode. That is, 1 ampere at 1 volt forward drop represents one watt which can result in significant regenerative changes in the current trip point as the diode temperature rises. Placing the small-signal reference amplifier in the proximity of the current-sensing diode also helps minimize the variability in the trip level due to the negative temperature coefficient of the diode. In spite of those limitations, the current limiting point can easily be adjusted over the range from 10 mA to 1 ampere with a single adjustment potentiometer. If the temperature stability of the current-limiting system is a serious consideration, the more usual current-sampling resistor-type of circuitry should be employed.

A power Darlington transistor (in a heat sink TO-3 case), is used as the series-pass element for the conventional current-limiting system, Fig. 27, because high-power Darlington dissipation will be encountered at low output voltage and high currents.

A small heat-sink VERSAWATT transistor is used as the series-pass element in the fold-back current system, Fig. 28, since dissipation levels will only approach 10 watts. In this system, the D2201 diode is used for current sampling. Foldback is provided by the 3 k $\Omega$  and 100 k $\Omega$  divider network connected to the base of the current-sensing transistor.

Both regulators, Figs. 27 and 28, provide better than 0.02% load regulation. Because there is constant loop gain at all voltage settings, the regulation also remains constant. Line regulation is 0.1% per volt. Hum and noise voltage is less than 200  $\mu$ V as read with a meter having a 10-MHz bandwidth.

Fig. 31 (a) shows the turn ON and turn OFF characteristics of both regulators. The slow turn-on rise is due to the slow rate of rise of the reference voltage. Fig. 29 (b) shows the transient response of the regulator with the switching of a 20- $\Omega$  load at 20 volts output.

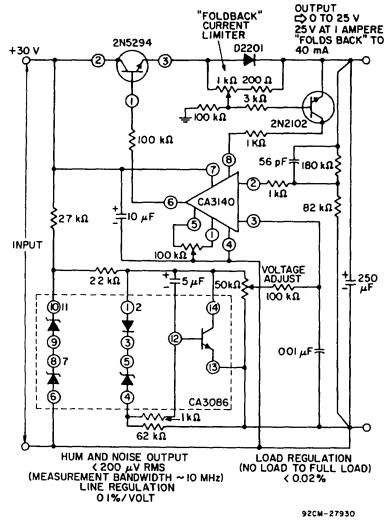
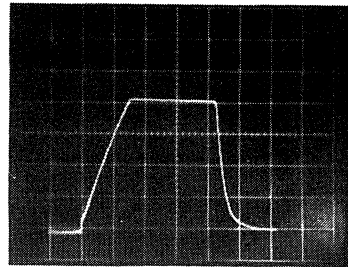
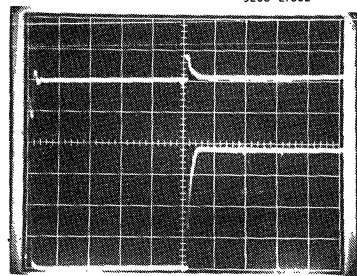


Fig. 28 — Regulated power supply with "foldback" current limiting.



(a)  
SUPPLY TURN-ON AND TURN-OFF CHARACTERISTICS  
(5 VOLTS / DIV AND -1 s / DIV.)



(b)  
TRANSIENT RESPONSE  
TOP TRACE: OUTPUT VOLTAGE  
(200 mV / DIV AND 5  $\mu$ s / DIV)  
BOTTOM TRACE: COLLECTOR OF LOAD SWITCHING TRANSISTOR,  
LOAD = 1 AMPERE  
(5 VOLTS / DIV AND 5  $\mu$ s / DIV)

Fig. 29 — Waveforms of dynamic characteristics of power supply currents shown in Figs. 29 and 30.

## CA3140A, CA3140

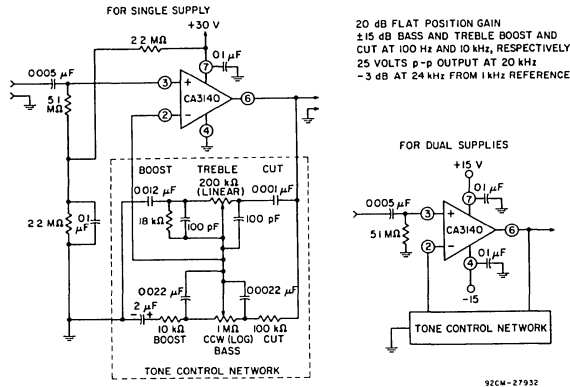


Fig. 30 — Tone control circuit using CA3130 series (20-dB midband gain).

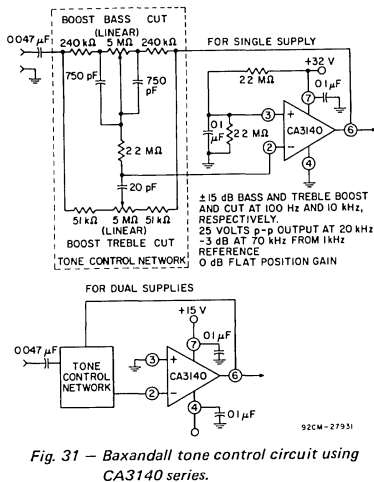


Fig. 31 — Baxandall tone control circuit using CA3140 series.

### TONE CONTROL CIRCUITS

High-slew-rate, wide-bandwidth, high-output voltage capability and high input impedance are all characteristics required of tone-control amplifiers. Two tone control circuits that exploit these characteristics of the CA3140 are shown in Figs. 30 and 31.

The first circuit, shown in Fig. 31, is the Baxandall tone-control circuit which provides unity gain at midband and uses standard linear potentiometers. The high input impedance of the CA3140 makes possible the use of low-cost, low-value, small-size capacitors, as well as reduced load of the driving stage.

Bass treble boost and cut are  $\pm 15$  dB at 100 Hz and 10 kHz, respectively. Full peak-to-peak output is available up to at least 20 kHz due to the high slew rate of the CA3140. The amplifier gain is  $-3$  dB down from its "flat" position at 70 kHz.

Fig. 30 shows another tone-control circuit with similar boost and cut specifications. The wideband gain of this circuit is equal to the ultimate boost or cut plus one, which in this case is a gain of eleven. For 20-dB boost and cut, the input loading of this circuit is essentially equal to the value of the resistance from terminal No.3 to ground. A detailed analysis of this circuit is given in "An IC Operational Transconductance Amplifier (OTA) With Power Capability" by L. Kaplan and H. Wittlinger, IEEE Transactions on Broadcast and Television Receivers, Vol. BTR-18, No.3, August, 1972.

### WIEN BRIDGE OSCILLATOR

Another application of the CA3140 that makes excellent use of its high input-impedance, high-slew-rate, and high-voltage qualities is the Wien Bridge sine-wave oscillator. A basic Wien Bridge oscillator is shown in Fig. 32. When  $R_1 = R_2 = R$  and  $C_1 = C_2 = C$ , the frequency equation reduces to the familiar  $f = 1/2\pi RC$  and the gain required for oscillation,  $A_{OSC}$  is equal to 3. Note that if  $C_2$  is increased by a factor of four and  $R_2$  is reduced by a factor of four, the gain required for oscillation becomes 1.5, thus per-



## CA3140A, CA3140

mitting a potentially higher operating frequency closer to the gain-bandwidth product of the CA3140.

Oscillator stabilization takes on many forms. It must be precisely set, otherwise the amplitude will either diminish or reach some form of limiting with high levels of distortion. The element,  $R_S$ , is commonly replaced with some variable resistance element. Thus, through some control means, the value of  $R_S$  is adjusted to maintain constant oscillator output. A FET channel resistance, a thermistor, a lamp bulb, or other device whose resistance is made to increase as the output amplitude is increased are a few of the elements often utilized.

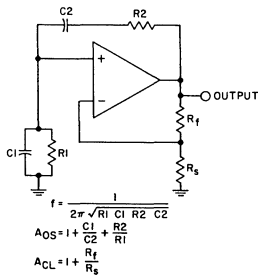


Fig. 32 — Basic Wien bridge oscillator circuit using an operational amplifier.

Fig. 33 shows another means of stabilizing the oscillator with a zener diode shunting the feedback resistor ( $R_f$  of Fig. 32). As the output signal amplitude increases, the zener diode impedance decreases resulting in more feedback with consequent reduction in gain; thus stabilizing the amplitude of the output signal. Furthermore, this combination of a monolithic zener diode and bridge rectifier circuit tends to provide a zero temperature coefficient for this regulating system. Because this bridge rectifier system has no time constant, i.e., thermal time constant for the lamp bulb, and RC time constant for filters often used in detector networks, there is no lower frequency limit. For example, with  $1\text{-}\mu\text{F}$  polycarbonate capacitors and  $22\text{ M}\Omega$  for the frequency determining network, the operating frequency is  $0.007\text{ Hz}$ .

As the frequency is increased, the output amplitude must be reduced to prevent the output signal from becoming slew-rate limited. An output frequency of  $180\text{ kHz}$  will reach a slew rate of approximately  $9\text{ volts}/\mu\text{s}$  when its amplitude is  $16\text{ volts peak-to-peak}$ .

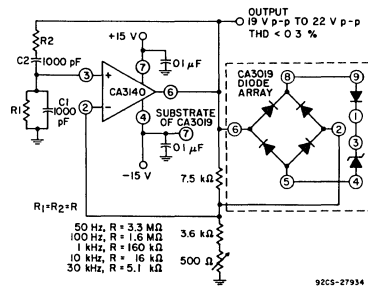


Fig. 33 — Wien bridge oscillator circuit using CA3140 series.

### SIMPLE SAMPLE-AND-HOLD SYSTEM

Fig. 34 shows a very simple sample-and-hold system using the CA3140 as the readout amplifier for the storage capacitor. The CA3080A serves as both input buffer amplifier and low feed-through transmission switch.\* System offset nulling is accom-

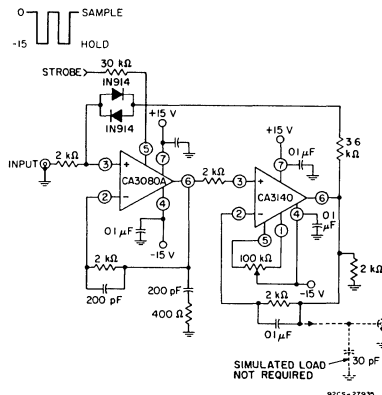


Fig. 34 — Sample-and-hold circuit.

plished with the CA3140 via its offset nulling terminals. A typical simulated load of  $2\text{ k}\Omega$  and  $30\text{ pF}$  is shown in the schematic.

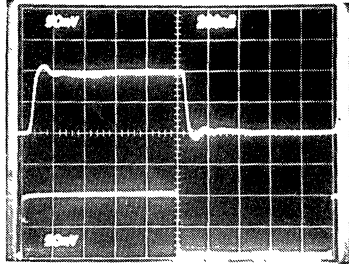
In this circuit, the storage compensation capacitance ( $C_1$ ) is only  $200\text{ pF}$ . Larger value capacitors provide longer "hold" periods but with slower slew rates. The slow rate

$$\frac{dv}{dt} = \frac{i}{c} = 0.5\text{ mA}/200\text{ pF} = 2.5\text{ V}/\mu\text{s}.$$

\* ICAN-6668 "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

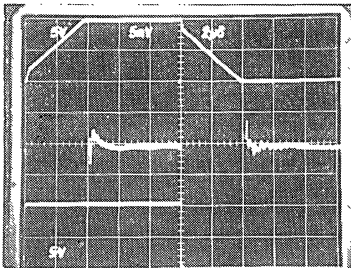
## CA3140A, CA3140

Pulse "droop" during the hold interval is  $170 \text{ pA}/200 \text{ pF}$  which is  $= 0.85 \text{ } \mu\text{V}/\mu\text{s}$ ; (i.e.,  $170 \text{ pA}/200 \text{ pF}$ ). In this case,  $170 \text{ pA}$  represents the typical leakage current of the CA3080A when strobed off. If  $C_1$  were increased to  $2000 \text{ pF}$ , the "hold-droop" rate will decrease to  $0.085 \text{ } \mu\text{V}/\mu\text{s}$ , but the slew rate would decrease to  $0.25 \text{ V}/\mu\text{s}$ . The parallel diode network connected between terminal



TOP TRACE: OUTPUT  
(50 mV/DIV AND 200 ns/DIV.)  
BOTTOM TRACE: INPUT  
(50 mV/DIV AND 200 ns/DIV.)

92CS-27883

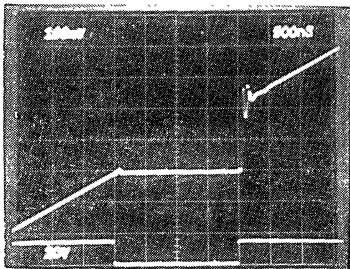


LARGE-SIGNAL RESPONSE AND  
SETTLING TIME

TOP TRACE: OUTPUT SIGNAL  
(5 V/DIV AND 2  $\mu\text{s}$ /DIV.)  
BOTTOM TRACE: INPUT SIGNAL  
(5 V/DIV AND 2  $\mu\text{s}$ /DIV.)

CENTER TRACE DIFFERENCE OF INPUT AND OUTPUT  
SIGNALS THROUGH TEKTRONIX  
AMPLIFIER 7A13  
(5 mV/DIV AND 2  $\mu\text{s}$ /DIV.)

92CS-27884



SAMPLING RESPONSE

TOP TRACE: SYSTEM OUTPUT  
(100 mV/DIV AND 500 ns/DIV.)  
BOTTOM TRACE: SAMPLING SIGNAL  
(20 V/DIV AND 500 ns/DIV.)

92CS-27885

Fig. 35 — Sample- and hold system dynamic characteristics waveforms.

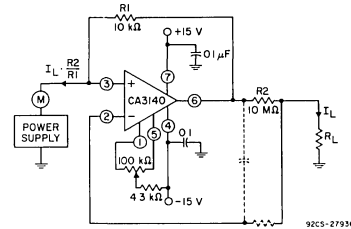
3 of the CA3080A and terminal 6 of the CA3140 prevents large input-signal feed-through across the input terminals of the CA3080A to the  $200 \text{ pF}$  storage capacitor when the CA3080A is strobed off. Fig. 35 shows dynamic characteristic waveforms of this sample-and-hold system.

### CURRENT AMPLIFIER

The low input-terminal current needed to drive the CA3140 makes it ideal for use in current-amplifier applications such as the one shown in Fig. 36. In this circuit, low current is supplied at the input potential as the power supply to load resistor  $R_L$ . This load current is increased by the multiplication factor  $R_2/R_1$ , when the load current is monitored by the power supply meter M. Thus, if the load current is  $100 \text{ nA}$ , with values shown, the load current presented to the supply will be  $100 \text{ } \mu\text{A}$ ; a much easier current to measure in many systems.

Note that the input and output voltages are transferred at the same potential and only the output current is multiplied by the scale factor.

The dotted components show a method of decoupling the circuit from the effects of high output-load capacitance and the potential oscillation in this situation. Essentially, the necessary high-frequency feedback is provided by the capacitor with the dotted series resistor providing load decoupling.



92CS-27936

Fig. 36 — Basic current amplifier for low-current measurement systems.

Fig. 37 shows a single-supply, absolute-value, ideal full-wave rectifier with associated waveforms. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3140 functions as a normal inverting amplifier with a gain equal to  $-R_2/R_1$ . When the equality of the two equations shown in Fig. 37 is satisfied, the full-wave output is symmetrical.

- "Operational Amplifiers Design and Applications", J. G. Graeme, McGraw-Hill Book Company, page 308 — "Negative Immittance Converter Circuits".

# CA3140A, CA3140

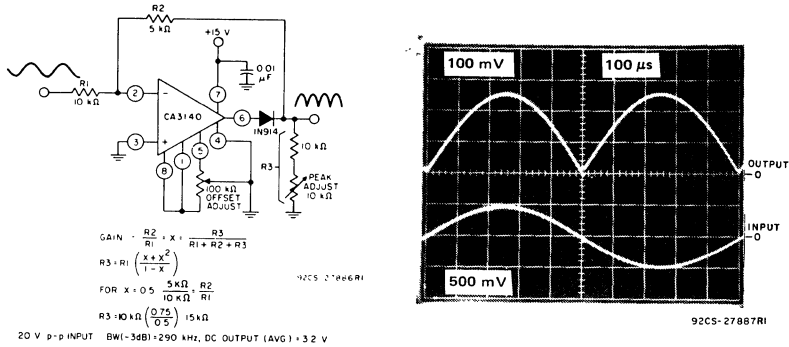
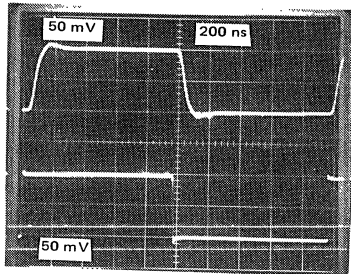
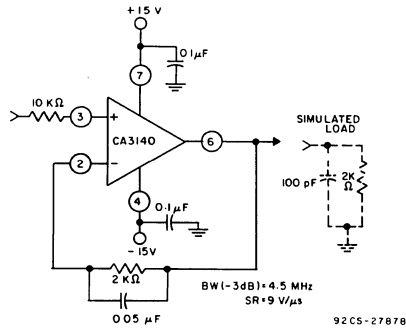
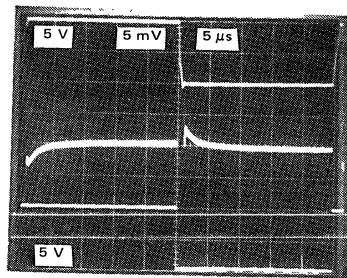


Fig. 37 — Single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.



(a) SMALL-SIGNAL RESPONSE (50 mV/DIV AND 200 ns/DIV) 92CS-27879



(b) INPUT-OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME (MEASUREMENT MADE WITH TEKTRONIX 7A13 DIFFERENTIAL AMPLIFIER) 92CS-27880

Fig. 38 — Split-supply voltage-follower test circuit and associated waveforms.

## CA3140A, CA3140

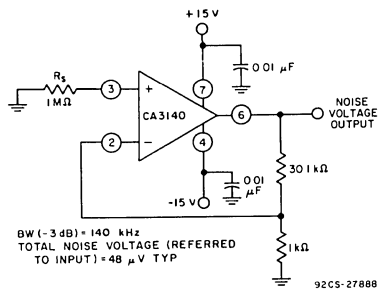
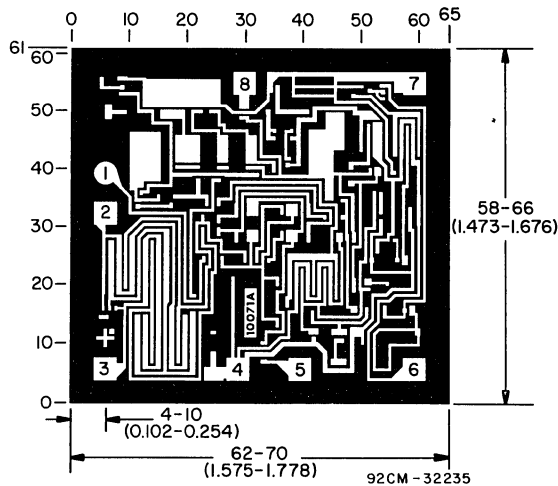


Fig. 39 — Test circuit amplifier (30-dB gain) used for wideband noise measurement.



Dimensions and pad layout for CA3140H.

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are  $57^\circ$  instead of  $90^\circ$  with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

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### Features

- MOSFET Input Stage Provides:
  - ▶ Very High  $Z_i = 1.5T\Omega$  ( $1.5 \times 10^{12}\Omega$ ) (Typ.)
  - ▶ Very Low  $I_i = 5\text{pA}$  Typ. @ 15V Operation  
= 2pA Typ. @ 5V Operation
- Common-Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can Be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or Both) Supply Rails

### Applications

- Ground Referenced Single Supply Amplifiers
- Fast Sample Hold Amplifiers
- Long Duration Timers/Monostables
- High Input Impedance Wideband Amplifiers
- Voltage Followers (e.g. Follower for Single Supply D/A Converter)
- Wien-Bridge Oscillators
- Voltage Controlled Oscillators
- Photo Diode Sensor Amplifiers

### Description

The CA3160A and CA3160 are integrated circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. The CA3160 series are frequency compensated versions of the popular CA3130 series.

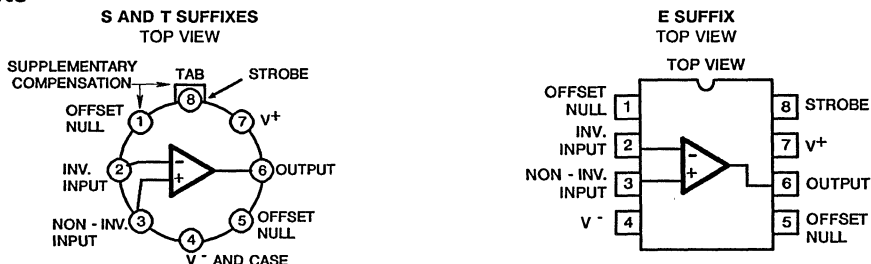
Gate-protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very high input impedance, very low input current, and exceptional speed performance. The use of PMOS field effect transistors in the input stage results in common-mode input voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3160 Series circuits operate at supply voltages ranging from 5 to 16 volts, or  $\pm 2.5$  to  $\pm 8$  volts when using split supplies, and have terminals for adjustment of offset voltage for applications requiring offset null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA3160 Series is supplied in standard 8-lead TO-5 style packages (T suffix), 8-lead dual-in-line formed lead TO-5 style "DIL-CAN" packages (S suffix). The CA3160 is available in chip form (H suffix). The CA3160 and CA3160A are also available in the Mini-DIP 8-lead dual-in-line plastic package (Mini-DIP-E suffix). All types operate over the full military temperature range of  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ . The CA3160A offers superior input characteristics over those of the CA3160.

### Pinouts



NOTE: CA3160 Series devices have an on-chip frequency-compensation network. Supplementary phase-compensation or frequency roll-off (if desired) can be connected externally between terminals 1 and 8.

FIGURE 1.

## CA3160A, CA3160

ELECTRICAL CHARACTERISTICS at  $T_A=25^{\circ}\text{C}$ ,  $V^+=15\text{ V}$ ,  $V^- = 0\text{ V}$  (Unless otherwise specified)

| CHARACTERISTIC  | LIMITS              |                  |      |                  |                  |      | Units                          |
|---|---------------------|------------------|------|------------------|------------------|------|--------------------------------|
|   | CA3160A (T, S, E)   |                  |      | CA3160 (T, S, E) |                  |      |                                |
|   | Min.                | Typ.             | Max. | Min.             | Typ.             | Max. |                                |
| Input Offset Voltage,<br>$ V_{IO} $ , $V^{\pm}=\pm 7.5\text{ V}$                                  | –                   | 2                | 5    | –                | 6                | 15   | mV                             |
| Input Offset Current,<br>$ I_{IO} $ , $V^{\pm}=\pm 7.5\text{ V}$                                  | –                   | 0.5              | 20   | –                | 0.5              | 30   | $\mu\text{A}$                  |
| Input Current, $I_I$<br>$V^{\pm}=\pm 7.5\text{ V}$  | –                   | 5                | 30   | –                | 5                | 50   | $\mu\text{A}$                  |
| Large-Signal Voltage<br>Gain, $A_{OL}$<br>$V_O=10\text{ V}_{\text{p-p}}$ , $R_L=2\text{ k}\Omega$ | 50 k                | 320 k            | –    | 50 k             | 320 k            | –    | V/V                            |
| Common-Mode<br>Rejection Ratio, CMRR  | 94                  | 110              | –    | 94               | 110              | –    | dB                             |
| Common-Mode Input-<br>Voltage Range, $V_{ICR}$  | 80                  | 95               | –    | 70               | 90               | –    | dB                             |
| Common-Mode Input-<br>Voltage Range, $V_{ICR}$  | 0                   | –0.5<br>to<br>12 | 10   | 0                | –0.5<br>to<br>12 | 10   | V                              |
| Power-Supply Rejection<br>Ratio, $\Delta V_{IO}/\Delta V^{\pm}$<br>$V^{\pm}=\pm 7.5\text{ V}$     | –                   | 32               | 150  | –                | 32               | 320  | $\mu\text{V}/\text{V}$         |
| Maximum Output<br>Voltage:  |                     |                  |      |                  |                  |      | V                              |
| At $R_L=2\text{ k}\Omega$   | $V_{OM}^+$<br>12    | 13.3             | –    | 12               | 13.3             | –    |                                |
|   | $V_{OM}^-$<br>–     | 0.002            | 0.01 | –                | 0.002            | 0.01 |                                |
| At $R_L=\infty$   | $V_{OM}^+$<br>14.99 | 15               | –    | 14.99            | 15               | –    | mA                             |
|   | $V_{OM}^-$<br>–     | 0                | 0.01 | –                | 0                | 0.01 |                                |
| Maximum Output<br>Current:  |                     |                  |      |                  |                  |      | mA                             |
| $I_{OM}^+$ (Source) @<br>$V_O = 0\text{ V}$   | 12                  | 22               | 45   | 12               | 22               | 45   |                                |
| $I_{OM}^-$ (Sink) @<br>$V_O = 15\text{ V}$  | 12                  | 20               | 45   | 12               | 20               | 45   |                                |
| Supply Current, $I^+$ :   |                     |                  |      |                  |                  |      | mA                             |
| $V_O=7.5\text{ V}$ , $R_L=\infty$   | –                   | 10               | 15   | –                | 10               | 15   |                                |
| $V_O = 0\text{ V}$ , $R_L = \infty$   | –                   | 2                | 3    | –                | 2                | 3    |                                |
| Input Offset Voltage<br>Temp. Drift,<br>$\Delta V_{IO}/\Delta T$                                  | –                   | 6                | –    | –                | 8                | –    | $\mu\text{V}/^{\circ}\text{C}$ |

## CA3160A, CA3160

### TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

| CHARACTERISTIC                                    | TEST CONDITIONS  |                           | CA3160/<br>CA3160A<br>(T, S, E) | UNITS                 |
|---|--|---------------------------|---------------------------------|-----------------------|
|   | $V^+ = +7.5\text{ V}$<br>$V^- = -7.5\text{ V}$<br>$T_A = 25^\circ\text{C}$<br>(Unless Otherwise Specified) |                           |                                 |                       |
| Input Offset Voltage Adjustment Range             | 10 k $\Omega$ across Terms. 4 and 5 or 4 and 1   |                           | $\pm 22$                        | mV                    |
| Input Resistance, $R_I$                           |  |                           | 1.5                             | T $\Omega$            |
| Input Capacitance, $C_I$                          | $f = 1\text{ MHz}$   |                           | 4.3                             | pF                    |
| Equivalent Input Noise Voltage, $e_n$             | BW=  | $R_S = 1\text{ M}\Omega$  | 40                              | $\mu\text{V}$         |
|   | 0.2 MHz  | $R_S = 10\text{ M}\Omega$ | 50                              |                       |
| Equivalent Input Noise Voltage, $e_n$             | $R_S =$  | 1 kHz                     | 72                              | nV $\sqrt{\text{Hz}}$ |
|   | 100 $\Omega$   | 10 kHz                    | 30                              |                       |
| Unity Gain Crossover Frequency, $f_T$             |  |                           | 4                               | MHz                   |
| Slew Rate, SR:                                    |  |                           | 10                              | V/ $\mu\text{s}$      |
| Transient Response:                               | $C_L = 25\text{ pF}$<br>$R_L = 2\text{ k}\Omega$<br>(Voltage Follower)                                     |                           | 0.09                            | $\mu\text{s}$         |
|   |  | Rise Time, $t_r$          |                                 |                       |
| Overshoot   |  |                           | 10                              | %                     |
| Settling Time (4 V <sub>p-p</sub> Input to <0.1%) |  |                           | 1.8                             | $\mu\text{s}$         |

| CHARACTERISTIC   | TEST CONDITIONS  |  | CA3160A<br>(T, S, E) | CA3160<br>(T, S, E) | UNITS           |
|--|--|--|----------------------|---------------------|-----------------|
|  | $V^+ = 5\text{ V}$<br>$V^- = 0\text{ V}$<br>$T_A = 25^\circ\text{C}$<br>(Unless Otherwise Specified) |  |                      |                     |                 |
| Input Offset Voltage, $V_{IO}$                           |  |  | 2                    | 6                   | mV              |
| Input Offset Current, $I_{IO}$                           |  |  | 0.1                  | 0.1                 | pA              |
| Input Current, $I_I$                                     |  |  | 2                    | 2                   | pA              |
| Common-Mode Rejection Ratio, CMRR                        |  |  | 90                   | 80                  | dB              |
| Large-Signal Voltage Gain, $A_{OL}$                      | $V_O = 4\text{ V}_{p-p}$<br>$R_L = 5\text{ k}\Omega$   |  | 100 k                | 100 k               | V/V             |
|  |  |  | 100                  | 100                 | dB              |
| Common-Mode Input Voltage Range, $V_{ICR}$               |  |  | 0 to 2.8             | 0 to 2.8            | V               |
| Supply Current, $I^+$                                    | $V_O = 5\text{ V}$<br>$R_L = \infty$   |  | 300                  | 300                 | $\mu\text{A}$   |
|  |  | $V_O = 2.5\text{ V}$<br>$R_L = \infty$ | 500                  | 700                 |                 |
| Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^+$ |  |  | 200                  | 200                 | $\mu\text{V/V}$ |

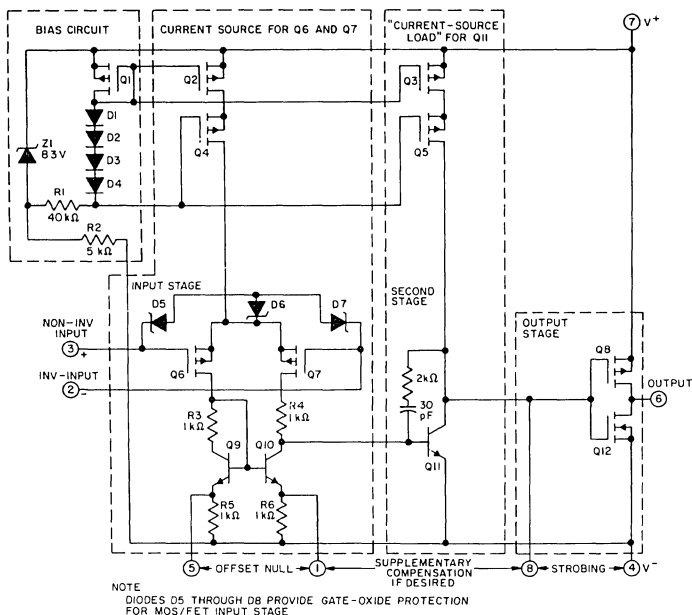
# CA3160A, CA3160

## MAXIMUM RATINGS, Absolute-Maximum Values

|   |                            |
|---|----------------------------|
| DC SUPPLY VOLTAGE<br>(Between $V^+$ and $V^-$ Terminals) .....        | 16 V                       |
| DIFFERENTIAL-MODE<br>INPUT VOLTAGE .....                              | $\pm 8$ V                  |
| COMMON-MODE DC<br>INPUT VOLTAGE... ( $V^+ + 8$ V) to ( $V^- - 0.5$ V) |                            |
| INPUT-TERMINAL CURRENT .....  | 1 mA                       |
| DEVICE DISSIPATION:   |                            |
| WITHOUT HEAT SINK —   |                            |
| UP TO 55°C .....  | 630 mW                     |
| ABOVE 55°C .....  | Derate linearly 6.67 mW/°C |
| WITH HEAT SINK —  |                            |
| UP TO 90°C .....  | 1 W                        |
| ABOVE 90°C .....  | Derate linearly 16.7 mW/°C |

|  |               |
|--|---------------|
| TEMPERATURE RANGE:   |               |
| OPERATING (All Types) .....  | -55 to +125°C |
| STORAGE (All Types) .....  | -65 to +150°C |
| OUTPUT SHORT-CIRCUIT<br>DURATION* .....                            | INDEFINITE    |
| LEAD TEMPERATURE<br>(DURING SOLDERING):                            |               |
| AT DISTANCE 1/16 $\pm$ 1/32 INCH<br>(1.59 $\pm$ 0.79 MM) FROM CASE |               |
| FOR 10 SECONDS MAX. ....   | +265°C        |

\*Short circuit may be applied to ground or to either supply.



92CM-28536

Fig. 2 — Schematic diagram of the CA3160 Series.

## CIRCUIT DESCRIPTION

Fig. 3 is a block diagram of the CA3160 series CMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3160 series circuits are ideal for single-supply operation. Three class A amplifier stages, having the individual gain capability and current consumption shown in Fig. 3, provide the total gain of the CA3160. A biasing circuit provides two potentials for common use in the first and second stages. Terminals 8 and 1 can be used to supplement the internal phase compensation network if

additional phase compensation or frequency roll-off is desired. Terminals 8 and 4 can also be used to strobe the output stage into a low quiescent current state. When Terminal 8 is tied to the negative supply rail (Terminal 4) by mechanical or electrical means, the output potential at Terminal 6 essentially rises to the positive supply-rail potential at Terminal 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive CMOS digital circuits in comparator applications).



## CA3160A, CA3160

**Input Stages** — The circuit of the CA3160 is shown in Fig.2. It consists of a differential input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS transistors Q2, Q4, are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D7 provide gate-oxide protection against high-voltage transients, e.g., including static electricity during handling for Q6 and Q7.

**Second-Stage** — Most of the voltage gain in the CA3160 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is described later. Miller Effect compensation (roll off) is accomplished by means of the 30-pF capacitor and 2-k $\Omega$  resistor connected between the base and collector of transistor Q11. These internal components provide sufficient compensation for unity gain operation in most applications. However, additional compensation, if desired, may be used between Terminals 1 and 8.

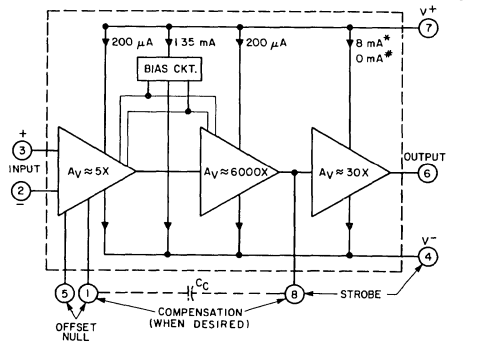
**Bias-Source Circuit** — At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Terminal 7. A potential of

about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Terminal 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes non-conductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

**Output Stage** — The output stage consists of a drain-loaded inverting amplifier using COS/MOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig.6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.

† For general information on the characteristics CMOS transistor-pairs in linear-circuit applications, see File No. 619, data bulletin on CA3600E "CMOS Transistor Array".



TOTAL SUPPLY VOLTAGE (FOR INDICATED VOLTAGE GAINS) = 15 V  
 \* WITH INPUT TERMINALS BIASED SO THAT TERM 6 POTENTIAL IS +7.5 V ABOVE TERM 4  
 \* WITH OUTPUT TERMINAL DRIVEN TO EITHER SUPPLY RAIL

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Fig. 3 — Block diagram of the CA3160 Series.

# CA3160A, CA3160

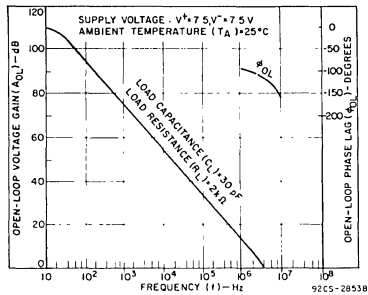


Fig. 4 - Open-loop voltage gain and phase shift vs. frequency.

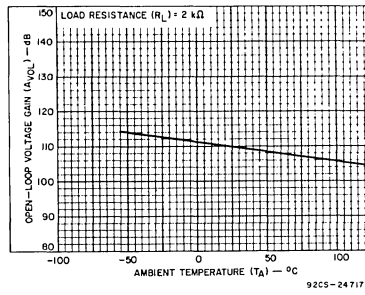


Fig. 5 - Open-loop gain vs. temperature.

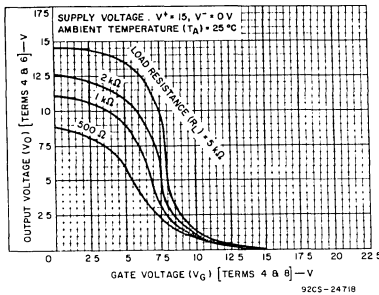


Fig. 6 - Voltage transfer characteristics of COS/MOS output stage.

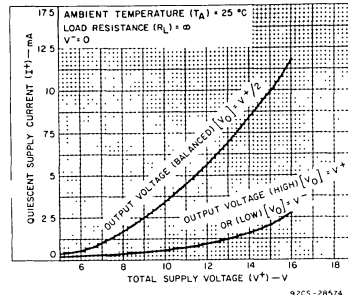


Fig. 7 - Quiescent supply current vs. supply voltage.

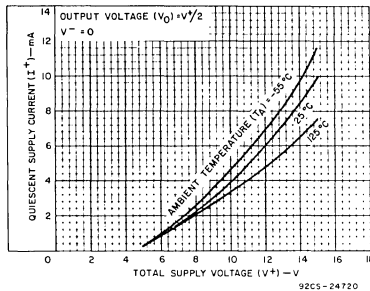


Fig. 8 - Quiescent supply current vs. supply voltage at several temperatures.

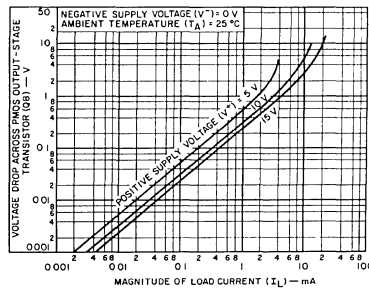


Fig. 9 - Voltage across PMOS output transistor (Q8) vs. load current.

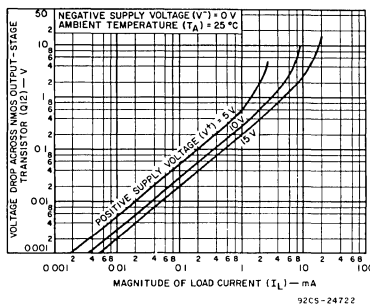


Fig. 10 - Voltage across NMOS output transistor (Q12) vs. load current.

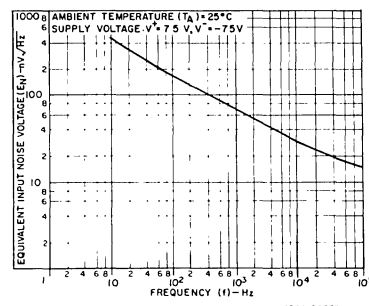


Fig. 11 - Equivalent noise voltage vs. frequency.

3  
OPERATIONAL  
AMPLIFIERS

**Offset Nulling**

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terminals 1 and 5 and with the potentiometer slider arm connected to Terminal 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

**Input Current Variation with Common-Mode Input Voltage**

As shown in the Table of Electrical Characteristics, the input current for the CA3160 Series Op-Amps is typically 5 pA at  $T_A=25^\circ\text{C}$  when Terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Fig. 12 contains

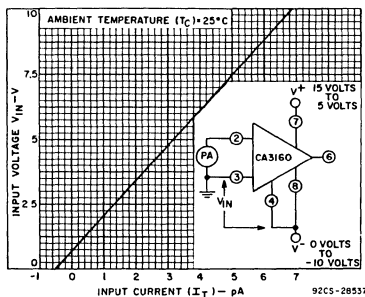


Fig. 12 – Input current vs. common-mode voltage.

data showing the variation of input current as a function of common-mode input voltage at  $T_A=25^\circ\text{C}$ . These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1 pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA3160 is also internally tied to Terminal 4, input terminal 3 is essentially “guarded” from spurious leakage currents.

**Input-Current Variation with Temperature**

The input current of the CA3160 Series circuits is typically 5 pA at  $25^\circ\text{C}$ . The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every  $10^\circ\text{C}$  increase in temperature. Fig. 13 provides data

on the typical variation of input bias current as a function of temperature in the CA3160.

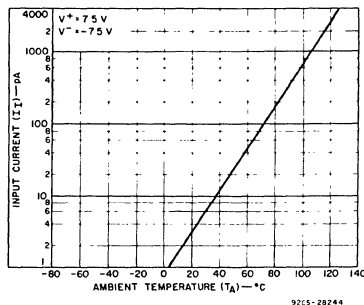


Fig. 13 – Input current vs. ambient temperature.

In applications requiring the lowest practical input current and incremental increases in current because of “warm-up” effects, it is suggested that an appropriate heat sink be used with the CA3160. In addition, when “sinking” or “sourcing” significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

**Input-Offset-Voltage ( $V_{IO}$ ) Variation with DC Bias vs. Device Operating Life**

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3160 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terminals 2 and 3. Fig. 14 shows typical data pertinent to shifts in offset voltage encountered with CA3160 devices in TO-5 packages during life testing. At lower temperatures (TO-5 and plastic) for example at  $85^\circ\text{C}$ , this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those en-

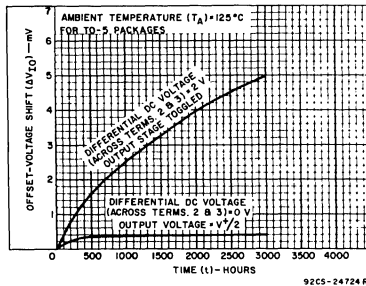


Fig. 14 – Typical incremental offset-voltage shift vs. operating life.

countered in an operational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output state is "toggled", e.g., as in comparator applications.

### Power-Supply Considerations

Because the CA3160 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single- and dual-supply service. Figs. 15(a) and 15(b) show the CA3160 connected for both dual- and single-supply operation.

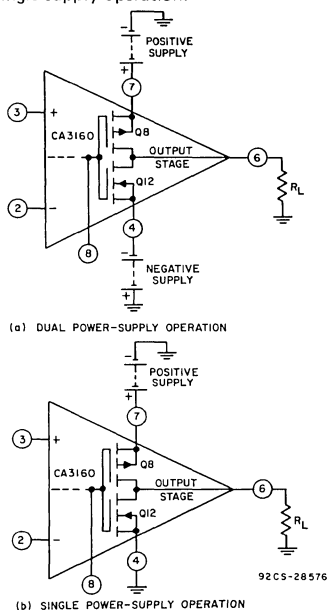


Fig. 15 — CA3160 output stage in dual and single power-supply operation.

**Dual-supply operation:** When the output voltage at Terminal 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

**Single-supply operation:** Initially, let it be assumed that the value of  $R_L$  is very high (or disconnected), and that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is at  $V^+/2$ , i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA3160 operated under these conditions.

Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Terminal 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA3160, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 15(a) shows a dual-supply arrangement for the output stage that can also be strobed off, assuming  $R_L = \infty$ , by pulling the potential of Terminal 8 down to that of Terminal 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Terminal 6 and ground in the circuit of Fig. 15(b). Let it further be assumed again that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is a  $V^+/2$ . Since PMOS transistor Q8 must now supply quiescent current to both  $R_L$  and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the  $R_L$  magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

### Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3160 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only  $40 \mu\text{V}$  when the test-circuit amplifier of Fig. 16 is operated at a total supply voltage of 15 volts. This value of

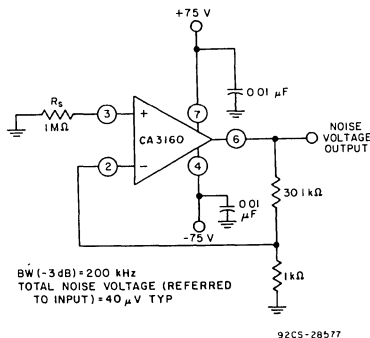
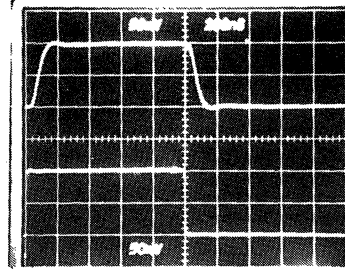
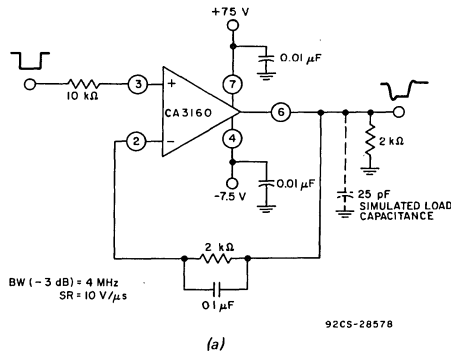


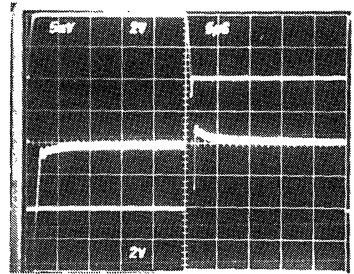
Fig. 16 — Test-circuit amplifier (30-dB gain) used for wideband noise measurements.

## CA3160A, CA3160

total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.



(b) Small Signal Response  
Top Trace: Output  
Bottom Trace: Input



(c) Input-Output Difference Signal Showing Settling Time  
Top Trace: Output Signal  
Center Trace: Difference Signal 5 mV/div  
Bottom Trace: Input Signal

Fig. 17 — Split-supply voltage follower with associated waveforms.

### TYPICAL APPLICATIONS

#### Voltage Followers

Operational amplifiers with very high input resistances, like the CA3160, are particularly suited to service as voltage followers. Fig. 17 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3160 in a split-supply configuration.

A voltage follower, operated from a single-supply, is shown in Fig. 18 together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig. 18b with input-signal ramping. The waveforms in Fig. 18c show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig. 18c also shows the manner in which the COS/MOS output stage permits the output signal to swing down

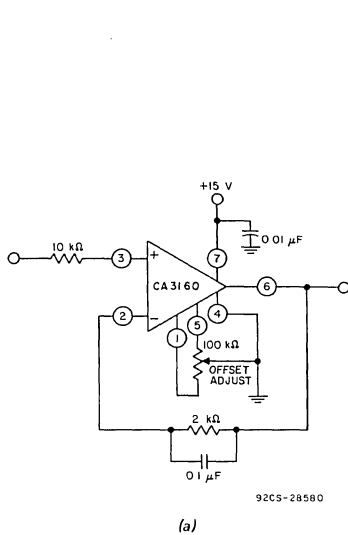
to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3160 in a single-supply voltage-follower application.

#### 9-Bit CMOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)\* is shown in Fig. 19. This system combines the concepts of multiple-switch CMOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3160 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig. 19.

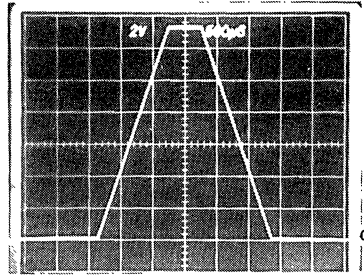
\* "Digital-to-Analog Conversion Using the Harris CD4007A COS/MOS IC", Application Note ICAN-6080.

# CA3160A, CA3160

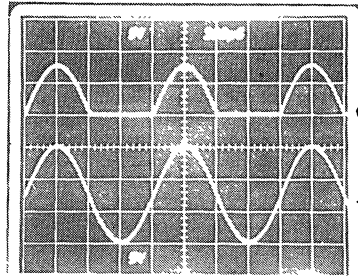


(a)

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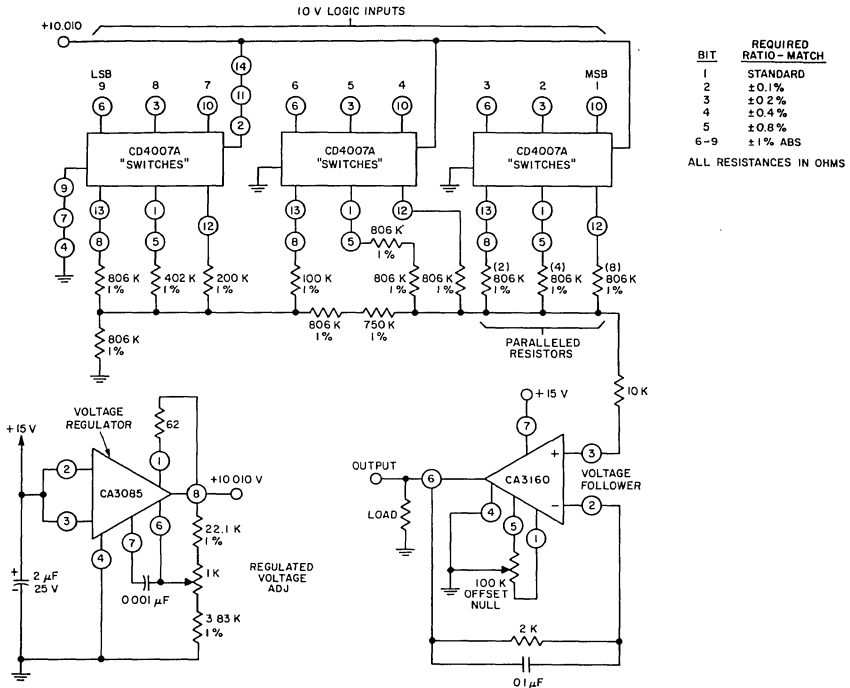
(b) Output signal with input-signal ramping.



(c) Output-Waveform with Ground-Reference Sine-Wave Input  
Top Trace: Output  
Bottom Trace: Input

92CS-28581R1

Fig. 18 - Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig.9 in ICAN-6080.)



| BIT | REQUIRED RATIO - MATCH |
|-----|------------------------|
| 1   | STANDARD               |
| 2   | ±0.1%                  |
| 3   | ±0.2%                  |
| 4   | ±0.4%                  |
| 5   | ±0.8%                  |
| 6-9 | ±1% ABS                |

ALL RESISTANCES IN OHMS

Fig. 19 - 9-bit DAC using CMOS digital switches and CA3160.

92CM-28582

## CA3160A, CA3160

The circuit uses an R/2R voltage-ladder network, with the output-potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA3160 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The

flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.

### Error-Amplifier in Regulated Power Supplies

The CA3160 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero.

The circuit shown in Fig.20 uses a CA3160 as an error amplifier in a continuously adjustable 1-ampere power supply. One of the key features of this circuit is its ability to regulate down to the vicinity of zero volts with only one dc power supply input.

An RC network, connected between the base of the output drive transistor and the input voltage, prevents "turn-on overshoot", a condition typical of many operational-amplifier regulator circuits. As the amplifier becomes operational, this RC network ceases to have any influence on the regulator performance.

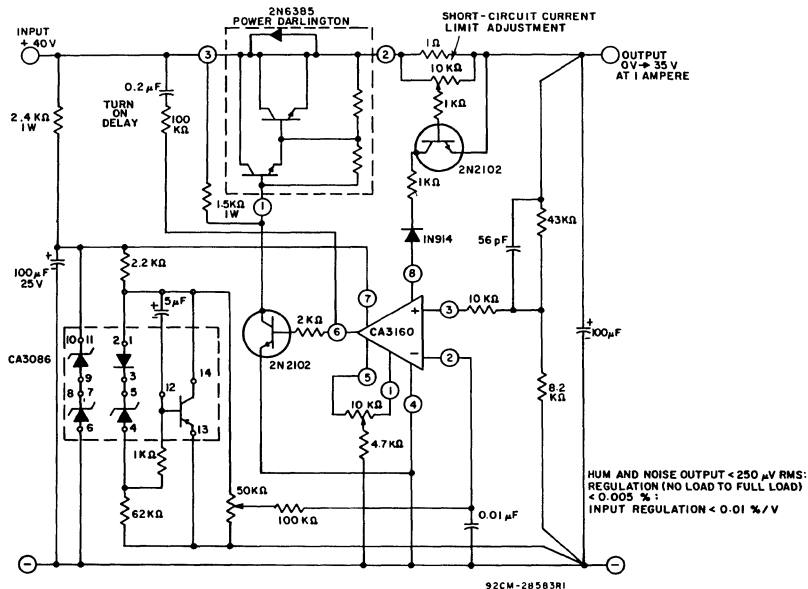


Fig.20 — Voltage regulator circuit (0.1 to 35 V at 1 A).

## CA3160A, CA3160

### Precision Voltage-Controlled Oscillator

The circuit diagram of a precision voltage-controlled oscillator is shown in Fig.21. The oscillator operates with a tracking error in the order of 0.02 percent and a temperature coefficient of 0.01%/°C. A multivibrator (A<sub>1</sub>) generates pulses of constant amplitude (V) and width (T<sub>2</sub>). Since the output (terminal 6) of A<sub>1</sub> (a CA3130) can swing within about 10 millivolts of either supply-rail, the output pulse amplitude (V) is essentially equal to V<sub>+</sub>. The average output voltage ( $E_{avg} = V T_2/T_1$ ) is applied to the non-inverting input terminal of comparator A<sub>2</sub> via an integrating network R<sub>3</sub>, C<sub>2</sub>. Comparator A<sub>2</sub> operates to establish circuit conditions such that  $E_{avg} = V_1$ . This circuit condition is accomplished by feeding an output signal from terminal 6 of A<sub>2</sub> through R<sub>4</sub>, D<sub>4</sub> to the inverting terminal (terminal 2)

of A<sub>1</sub>, thereby adjusting the multivibrator interval, T<sub>3</sub>.

### Voltmeter With High Input Resistance

The voltmeter circuit shown in Fig.22 illustrates an application in which a number of the CA3160 characteristics are exploited. Range-switch SW<sub>1</sub> is ganged between input and output circuitry to permit selection of the proper output voltage for feedback to Terminal 2 via 10 KΩ current-limiting resistor. The circuit is powered by a single 8.4-volt mercury battery. With zero input signal, the circuit consumes somewhat less than 500 microamperes plus the meter current required to indicate a given voltage. Thus, at full-scale input, the total supply current rises to slightly more than 1500 microamperes.

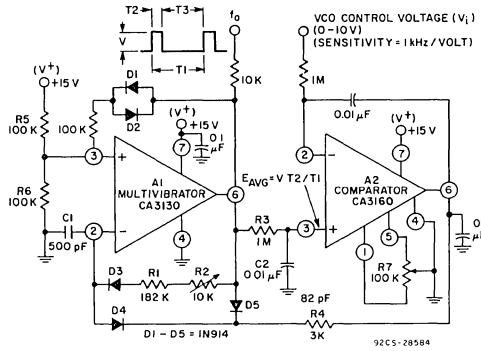


Fig.21 - Voltage-controlled oscillator.

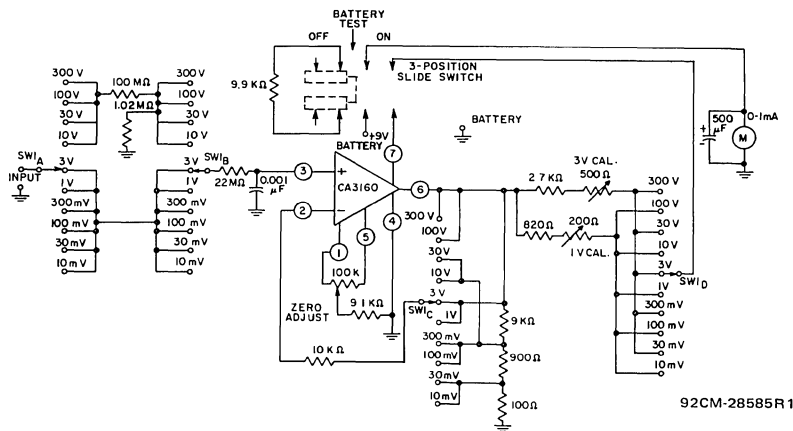


Fig.22 - High-input-resistance DC voltmeter.

3  
OPERATIONAL  
AMPLIFIERS



# CA3160A, CA3160

## Function Generator

A function generator having a wide tuning range is shown in Fig.23. The adjustment range, in excess of 1,000,000/1, is accomplished by a single potentiometer. Three operational amplifiers are utilized: a CA3160 as a voltage follower, a CA3080 as a high-speed comparator, and a second CA3080A

as a programmable current source. Three variable capacitors C1, C2, and C3 shape the triangular signal between 500 kHz and 1 MHz. Capacitors C4, C5, and the trimmer potentiometer in series with C5 maintain essentially constant ( $\pm 10\%$ ) amplitude up to 1 MHz.

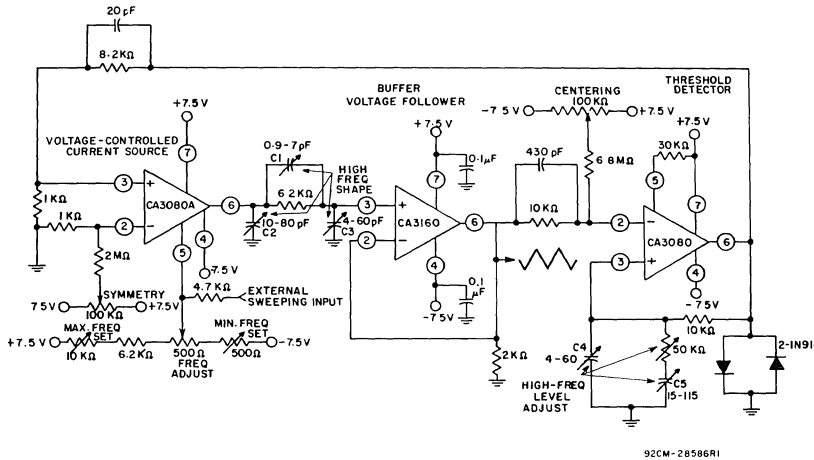
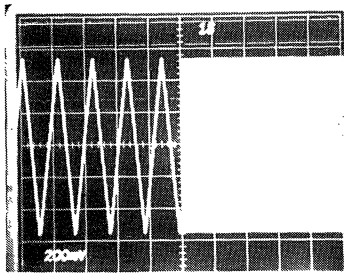
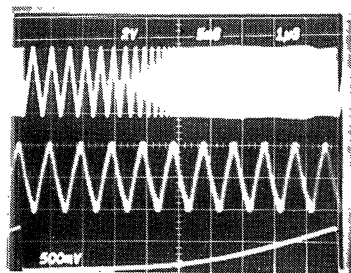


Fig.23(a) - 1,000,000/1 single-control function generator - 1 MHz to 1 Hz.



(b) - Two-tone output signal from the function generator. A square-wave signal modulates the external sweeping input to produce 1 Hz and 1 MHz, showing the 1,000,000/1 frequency range of the function generator.

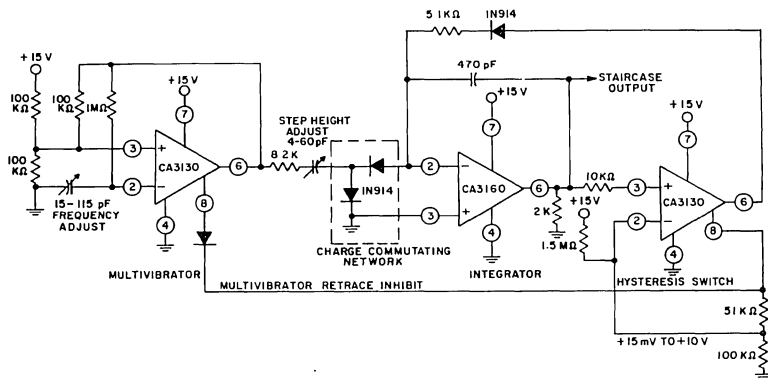


(c) - Triple-trace of the function generator sweeping to 1 MHz. The bottom trace is the sweeping signal and the top trace is the actual generator output. The center trace displays the 1 MHz signal via delayed oscilloscope triggering of the upper swept output signal.

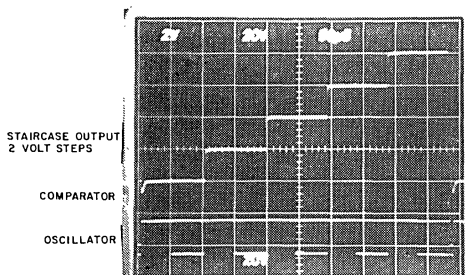
## CA3160A, CA3160

### Staircase Generator

Fig. 24 shows a staircase generator circuit utilizing three CMOS operational amplifiers. Two CA3130's are used; one as a multivibrator, the other as a hysteresis switch. The third amplifier, a CA3160, is used as a linear staircase generator.



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(b) — Staircase Generator Waveform  
 Top Trace: Staircase Output  
 2 Volt Steps  
 Center Trace: Comparator  
 Bottom Trace: Oscillator

### Picoammeter Circuit

Fig. 25 is a current-to-voltage converter configuration utilizing a CA3160 and CA3140 to provide a picoampere meter for  $\pm 3$  pA full-scale meter deflection. By placing Terminals 2 and 4 of the CA3160 at ground potential, the CA3160 input is operated in the "guarded mode". Under this operating condition, even slight leakage resistance present between Terminals 3 and 2 or between Terminals 3 and 4 would result in zero voltage across this leakage resistance, thus substantially reducing the leakage current.

If the CA3160 is operated with the same voltage on input Terminals 3 and 2 as on Terminal 4, a further reduction in the input current to the less than one picoampere level can be achieved as shown in Fig. 12.

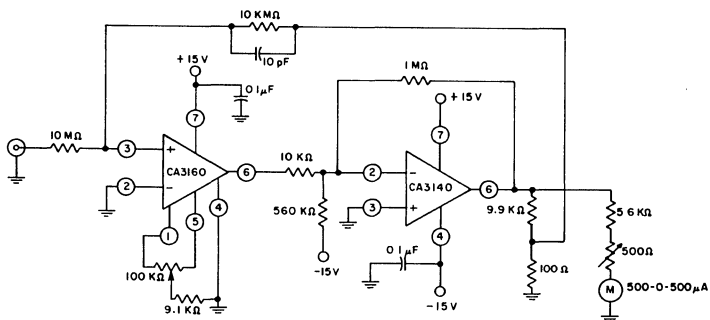
To further enhance the stability of this circuit, the CA3160 can be operated with its

output (Terminal 6) near ground, thus markedly reducing the dissipation by reducing the supply current to the device.

The CA3140 stage serves as a X100 gain stage to provide the required plus and minus output swing for the meter and feedback network. A 100-to-1 voltage divider network consisting of a 9.9-K $\Omega$  resistor in series with a 100-ohm resistor sets the voltage at the 10-KM $\Omega$  resistor (in series with Terminal 3) to  $\pm 30$  mV full-scale deflection. This 30-mV signal results from  $\pm 3$  volts appearing at the top of the voltage divider network which also drives the meter circuitry.

By utilizing a switching technique in the meter circuit and in the 9.9 K $\Omega$  and 100-ohm network similar to that used in voltmeter circuit shown in Fig. 22, a current range of 3 pA to 1 nA full scale can be handled with the single 10-KM $\Omega$  resistor.

## CA3160A, CA3160



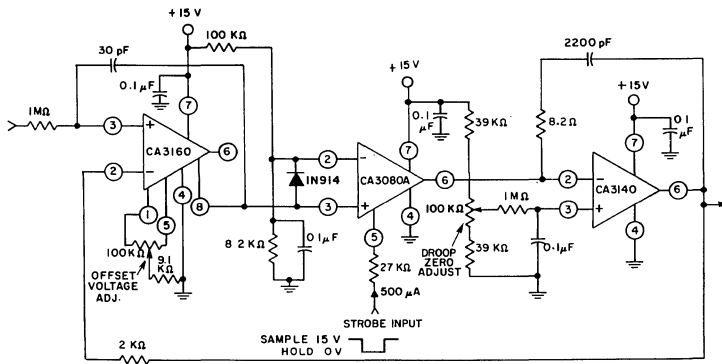
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Fig.25 — Current-to-voltage converter to provide a picoammeter with  $\pm 3 \mu\text{A}$  full-scale deflection.

### Single-Supply Sample-and-Hold System

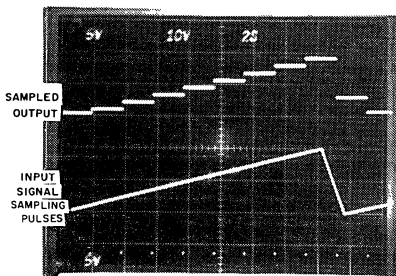
Fig. 26 shows a single-supply sample-and-hold system using a CA3160 to provide a high input impedance and an input-voltage range of 0 to 10 volts. The output from the input buffer integrator network is coupled to a CA3080A. The CA3080A functions as a strobeable current source for the CA3140 output integrator and storage capacitor. The CA3140 was chosen because of its low output impedance and constant gain-bandwidth

product. Pulse "droop" during the hold interval can be reduced to zero by adjusting the 100-K $\Omega$  bias-voltage potentiometer on the positive input of the CA3140. This zero adjustment sets the CA3080A output voltage at its zero current position. In this sample-and-hold circuit it is essential that the amplifier bias current be reduced to zero to minimize output signal current during the hold mode. Even with 320 mV at the amplifier bias circuit terminal (5) at least  $\pm 100 \mu\text{A}$  of output current will be available.

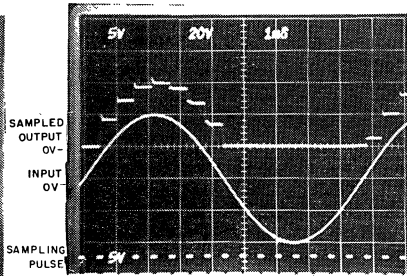


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Fig.26(a) — Single-supply sample-and-hold system— input 0-to-10 volts.



(b) — Sample-and-hold waveform.  
Top Trace: Sampled Output  
Center Trace: Input Signal  
Bottom Trace: Sampling Pulses



(c) — Sample-and-hold waveform.  
Top Trace: Sampled Output  
Center Trace: Input  
Bottom Trace: Sampling Pulse

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## CA3160A, CA3160

### Wien Bridge Oscillator

A simple, single-supply Wien Bridge oscillator using a CA3160 is shown in Fig. 27. A pair of parallel-connected 1N914 diodes comprise the gain-setting network which standardizes the output voltage at approximately 1.1 volts. The 500-ohm potentiometer is adjusted so that the oscillator will always start and the oscillation will be maintained. Increasing the amplitude of the voltage may lower the threshold level for starting and for sustaining the oscillation, but will introduce more distortion.

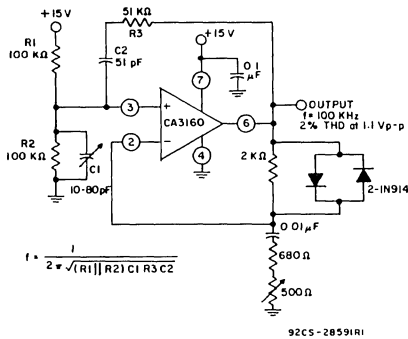


Fig. 27 — Single-supply Wien Bridge oscillator.

### Operation with Output-Stage Power-Booster

The current sourcing and sinking capability of the CA3160 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig. 28, three CMOS transistor-pairs in a single CA3600 IC array are shown parallel-connected with the output stage in the CA3160. In the Class A mode of CA3600E shown, a typical device consumes

20 mA of supply current at 15-V operation. This arrangement boosts the current-handling capability of the CA3160 output stage by about 2.5X.

The amplifier circuit in Fig. 28 employs feedback to establish a closed-loop gain of 20 dB. The typical large-signal-bandwidth (−3 dB) is 190 kHz.

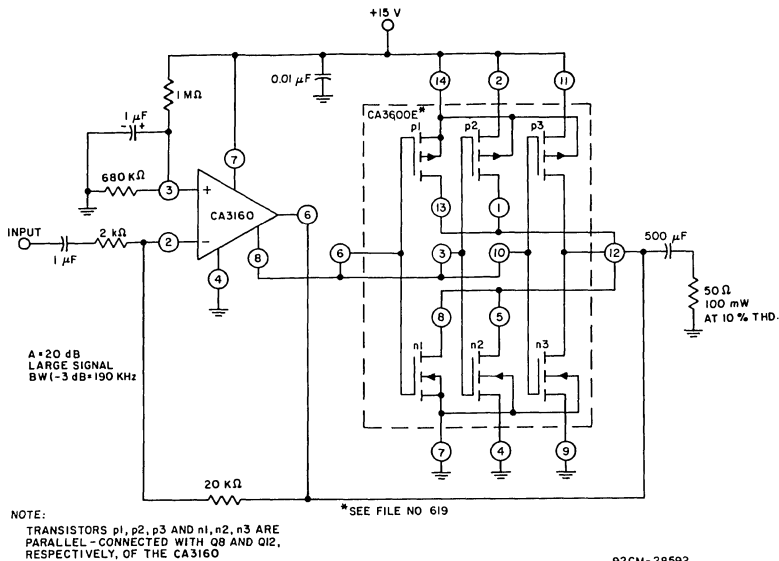


Fig. 28 — CMOS transistor array (CA3600E) connected as power booster in the output stage of the CA3160.

August 1991

## BICMOS Precision Operational Amplifiers

### Features

- Low  $V_{IO}$ :
  - ▶ CA3193A ..... 200 $\mu$ V (Max.)
  - ▶ CA3193 ..... 500 $\mu$ V (Max.)
- Low  $\Delta V_{IO}/\Delta T$ :
  - ▶ CA3193A ..... 3 $\mu$ V/ $^{\circ}$ C (Max.)
  - ▶ CA3193 ..... 5 $\mu$ V/ $^{\circ}$ C (Max.)
- Low  $I_{IO}$  and  $I_I$
- Low  $\Delta I_{IO}/\Delta T$ : CA3193 ..... 150pA/ $^{\circ}$ C (Max.)
- Low  $\Delta I_I/\Delta T$ : CA3193 ..... 3.7nA/ $^{\circ}$ C (Max.)

### Applications

- Thermocouple Preamplifiers
- Strain-Gauge Bridge Amplifiers
- Summing Amplifiers
- Differential Amplifiers
- Bilateral Current Sources
- Log Amplifiers
- Differential Voltmeters
- Precision Voltage References
- Active Filters
- Buffers
- Integrators
- Sample-and-Hold Circuits
- Low Frequency Filters

### Description

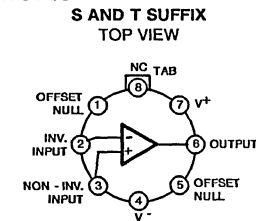
The CA3193A and CA3193 are ultra-stable, precision instrumentation, operational amplifiers that employ both PMOS and bipolar transistors on a single monolithic chip. The CA3193A and CA3193 amplifiers are internally phase compensated and provide a gain bandwidth product of 1.2MHz. They are pin compatible with the industry 741 series and many other IC op amps, and may be used as replacements for 741 series types in most applications.

The CA3193A and CA3193 can also be used as functional replacements for op-amp types 725, 108A, OP-5, OP-7, LM11 and LM714 in many applications where nulling is not employed. Because of their low offset voltage and low offset voltage-versus-temperature coefficient the CA3193A and CA3193 amplifiers have a wider range of applications than most op amps and are particularly well suited for use as thermocouple amplifiers, high gain filters, buffer, strain gauge bridge amplifiers and precision voltage references.

The two types in the CA3193 series are functionally identical. The CA3193A and CA3193 operate from supply voltages of  $\pm 3.5$ V to  $\pm 18$ V and have operating temperature ranges of  $-25^{\circ}$ C to  $+85^{\circ}$ C and  $0^{\circ}$ C to  $+70^{\circ}$ C, respectively.

The CA3193A and CA3193 types are supplied in standard 8-lead TO-5 style (T suffix), 8-lead dual-in-line formed lead TO-5 style (DIL-CAN-S suffix) and 8-lead dual-in-line plastic (Mini-DIP-E suffix) packages.

### Pinouts



NOTE: Pin 4 is Connected to Case on S and T Suffix.

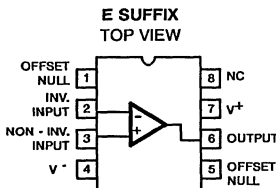


FIGURE 1.

### Block Diagram

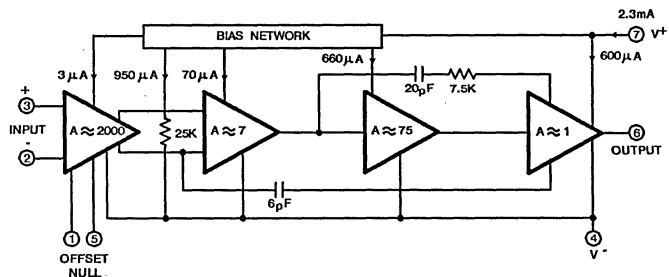


FIGURE 2. BLOCK DIAGRAM OF CA3193A AND CA3193

## CA3193A, CA3193

**Absolute-Maximum Ratings, Absolute-Maximum Values at  $T_A = 25^\circ\text{C}$**

|   | CA3193               | CA3193A          |
|---|----------------------|------------------|
| DC Supply Voltage .....   | $\pm 18$             | $\pm 18$         |
| Differential-Mode Input Voltage .....   | $\pm 5$              | $\pm 5$          |
| Common-Mode DC Input Voltage .....  | $(V^+ - 4), V^-$     | $(V^+ - 4), V^-$ |
| Input Terminal Current .....  | 1                    | 1                |
| Device Dissipation  |                      |                  |
| Without Heat Sink   |                      |                  |
| Up to $55^\circ\text{C}$ .....  | 630                  | 630              |
| Above $55^\circ\text{C}$ .....  | Derate Linearly 6.67 |                  |
| Temperature Range .....   | 0 to $70$            | -25 to 85        |
| Output Short-Circuit Duration* .....  | Indefinite           | Indefinite       |
| Lead Temperature (During Soldering) at distance of 1/16 in. $\pm$ 1/32 in.<br>(1.59 $\pm$ 0.79 mm) from case for 10 seconds max. .... | $\pm 265$            | $\pm 265$        |

\* Short circuit may be applied to ground or to either supply.

### Circuit Description

The block diagram of the CA3193 amplifier, Fig. 1 shows the voltage gain and supply current for each of its four amplifier stages. Simplified and complete schematic diagrams of the CA3193 amplifier are shown in Figs. 3 and 4, respectively.

A quad of physically cross-connected n-p-n transistors comprise the input-stage differential pair (Q1, Q2 in Figs. 3 and 4); this arrangement contributes to the low input offset-voltage characteristics of the amplifier. The ultra-high gain provided in the first stage ensures that subsequent stages cannot significantly influence the overall offset-voltage characteristics of the amplifier. High load impedances for the input-stage differential pair (Q1, Q2) are provided by the cascode-connected p-n-p transistors Q3, Q5 and Q4, Q6, thereby contributing to the high gain developed in the stage.

The second stage of the amplifier consists of a differential amplifier employing PMOS/FETs (Q7, Q8 in Figs. 3 and 4)

with appropriate drain loading. Since Q7 and Q8 are MOS/FETs, their loading on the first stage is quite low, thereby making an additional contribution to the high gain developed in the first stage. The second stage is also configured to convert its differential signal to a single-ended output signal by means of current mirror D9, Q30 (Figs. 3 and 4) to drive subsequent gain stage.

The third stage of the amplifier consists of Darlington-connected n-p-n transistors (Q17, Q19 in Figs. 3 and 4), driving the quasi-complementary Class AB output stage (Q14 and Q15, Q16 in Figs. 3 and 4). Output-stage short-circuit protection is activated by voltage drops developed across the 60-ohm resistors adjacent to the output terminal (R9 and R10, Fig. 4). When the voltage drop developed across either of these resistors reaches a potential equal to  $1 V_{BE}$ , the respective protective transistor (Q12 or Q13) is activated and shunts the base drive from the bases of the output stage transistors (Q14 and Q15, Q16).

Internal frequency compensation for the CA3193 amplifier is provided by two internal networks, a 6-pF capacitor connected between the input-stage transistor collectors and the node between the third and output stages and a second network, consisting of a 20-pF capacitor in series with a 7.5 k $\Omega$  resistor connected between the input and output nodes of the third stage.

## CA3193A, CA3193

**ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $V^+ = 15\text{ V}$  and  $V^- = 15\text{ V}$  unless otherwise specified.**

| CHARACTERISTIC  | LIMITS  |      |      |        |      |      | UNITS                                |
|---|---------|------|------|--------|------|------|--------------------------------------|
|   | CA3193A |      |      | CA3193 |      |      |                                      |
|   | Min.    | Typ. | Max. | Min.   | Typ. | Max. |                                      |
| Input Offset Voltage, $ V_{IO} $  | —       | 140  | 200  | —      | 300  | 500  | $\mu\text{V}$                        |
| $V_{IO}$ @ Max.Temp.  | —       | —    | 380  | —      | —    | 725  | $\mu\text{V}$                        |
| Input Offset Voltage Temp. Coefficient, $\Delta V_{IO}/\Delta T$ (Over specified temperature range for each device) | —       | 1    | 3    | —      | 1    | 5    | $\mu\text{V}/^\circ\text{C}$         |
| Input Offset Current, $I_{IO}$  | —       | 3    | 5    | —      | 5    | 10   | nA                                   |
| $ I_{IO} $ @ Max.Temp.  | —       | —    | 11   | —      | —    | 17   | nA                                   |
| Input Offset Current Temp. Coefficient, $\Delta I_{IO}/\Delta T$ (Over specified temperature range for each device) | —       | 0.03 | 0.10 | —      | 0.04 | 0.15 | $\text{nA}/^\circ\text{C}$           |
| Input Bias Current, $I_B$   | —       | 10   | 20   | —      | 20   | 40   | nA                                   |
| $ I_B $ @ Max.Temp.   | —       | —    | 83   | —      | —    | 207  | nA                                   |
| Input Bias Current Temp. Coefficient, $\Delta I_B/\Delta T$   | —       | 0.10 | 1.18 | —      | 0.15 | 3.70 | $\text{nA}/^\circ\text{C}$           |
| Input Noise Voltage, $e_n$ p-p (0.1 to 10 Hz)   | —       | 0.36 | —    | —      | 0.36 | —    | $\mu\text{V p-p}$                    |
| Input Noise Voltage Density, $e_n$  |         |      |      |        |      |      |                                      |
| $f_0 = 10\text{ Hz}$  | —       | 25   | —    | —      | 25   | —    | $\frac{\text{nV}}{\sqrt{\text{Hz}}}$ |
| $f_0 = 100\text{ Hz}$   | —       | 25   | —    | —      | 25   | —    |                                      |
| $f_0 = 1000\text{ Hz}$  | —       | 24   | —    | —      | 24   | —    |                                      |
| $f_0 = 10\text{ kHz}$   | —       | 24   | —    | —      | 24   | —    |                                      |
| $f_0 = 100\text{ kHz}$  | —       | 22   | —    | —      | 22   | —    |                                      |
| Input Noise Current, $i_n$ p-p (0.1 to 10 Hz)   | —       | 12   | 20   | —      | 12   | 20   | $\text{pA p-p}$                      |
| Input Noise Current Density, $i_n$  |         |      |      |        |      |      |                                      |
| $f_0 = 10\text{ Hz}$  | —       | 0.83 | —    | —      | 0.83 | —    | $\frac{\text{pA}}{\sqrt{\text{Hz}}}$ |
| $f_0 = 100\text{ Hz}$   | —       | 0.80 | —    | —      | 0.80 | —    |                                      |
| $f_0 = 1000\text{ Hz}$  | —       | 0.75 | —    | —      | 0.75 | —    |                                      |
| $f_0 = 10\text{ kHz}$   | —       | 0.72 | —    | —      | 0.72 | —    |                                      |
| $f_0 = 100\text{ kHz}$  | —       | 0.60 | —    | —      | 0.60 | —    |                                      |

## CA3193A, CA3193

**ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $V^+ = 15\text{ V}$  and  $V^- = 15\text{ V}$  (Cont'd)**  
 unless otherwise specified.

| CHARACTERISTIC  | LIMITS     |               |      |            |               |      | UNITS                  |
|---|------------|---------------|------|------------|---------------|------|------------------------|
|   | CA3193A    |               |      | CA3193     |               |      |                        |
|   | Min.       | Typ.          | Max. | Min.       | Typ.          | Max. |                        |
| Common-Mode Input Voltage Range, $V_{ICR}$  | -12        | -13.5 to 11.5 | 10   | -12        | -13.5 to 11.5 | 10   | V                      |
| Common-Mode Rejection Ratio, ( $V_{CM} = V_{ICR}$ )   | 110        | 115           | —    | 100        | 110           | —    | dB                     |
|   |            | 1.78          | 3.16 |            | 3.16          | 10   | $\mu\text{V/V}$        |
| Power Supply Rejection Ratio, PSRR, $\Delta V_{IO}/\Delta V \pm$  | 100        | 130           | —    | 100        | 130           | —    | dB                     |
|   |            | 0.316         | 10   |            | 0.316         | 10   | $\mu\text{V/V}$        |
| Maximum Output Voltage Swing ( $R_L \geq 2\text{ K}\Omega$ )  | $\pm 13.0$ | $\pm 13.5$    | —    | $\pm 13.0$ | $\pm 13.5$    | —    | V                      |
| Large-Signal Voltage Gain ( $V_O = \pm 10$ )<br>$R_L \geq 1\text{ K}\Omega$<br>$R_L \geq 2\text{ K}\Omega$<br>$R_L \geq 10\text{ K}\Omega$          | —          | —             | —    | —          | —             | —    | dB                     |
|   | 110        | 115           | —    | 100        | 110           | —    |                        |
|   | —          | 125           | —    | —          | 115           | —    |                        |
| Short-Circuit Output Current to the Opposite Rail, $I_{OM}^+$ , $I_{OM}^-$  | -25        | $\pm 7$       | 25   | -25        | $\pm 7$       | 25   | mA                     |
| Slew Rate, SR ( $R_L \geq 2\text{ K}\Omega$ ; Unity Gain Voltage Follower)  | —          | 0.25          | —    | —          | 0.25          | —    | $\text{V}/\mu\text{s}$ |
| Gain-Bandwidth Product, $f_t$<br>$A_{OL} = 0\text{ dB}$<br>$R_L = 2\text{ k}\Omega$<br>$C_L = 100\text{ pF}$<br>$V_{IN} = 20$<br>$f = 1\text{ kHz}$ | —          | 1.20          | —    | —          | 1.20          | —    | MHz                    |
| Small-Signal Transient Response, $t_r$ ( $V_{IN} = 20\text{ mV p-p}$ , $f = 1\text{ kHz}$ )   | —          | 0.29          | —    | —          | 0.29          | —    | $\mu\text{s}$          |
| Supply Current, $R_L = \infty$<br>$V^+ = 15, V^- = -15$   | —          | 2.3           | 3.5  | —          | 2.3           | 3.5  | mA                     |
| Temperature Range   | -25        | —             | 85   | 0          | —             | 70   | $^\circ\text{C}$       |



# CA3193A, CA3193

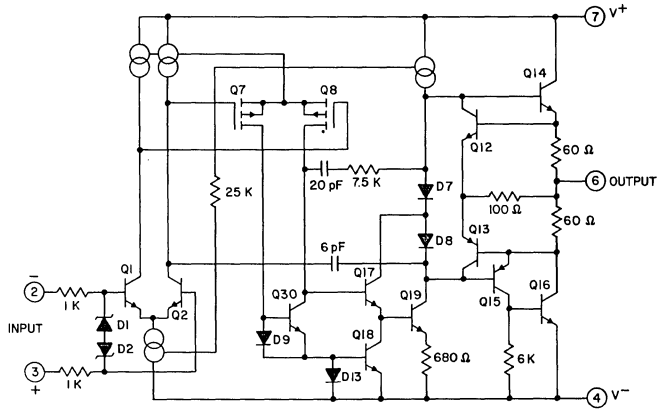


Fig. 3 - CA3193 simplified schematic diagram.

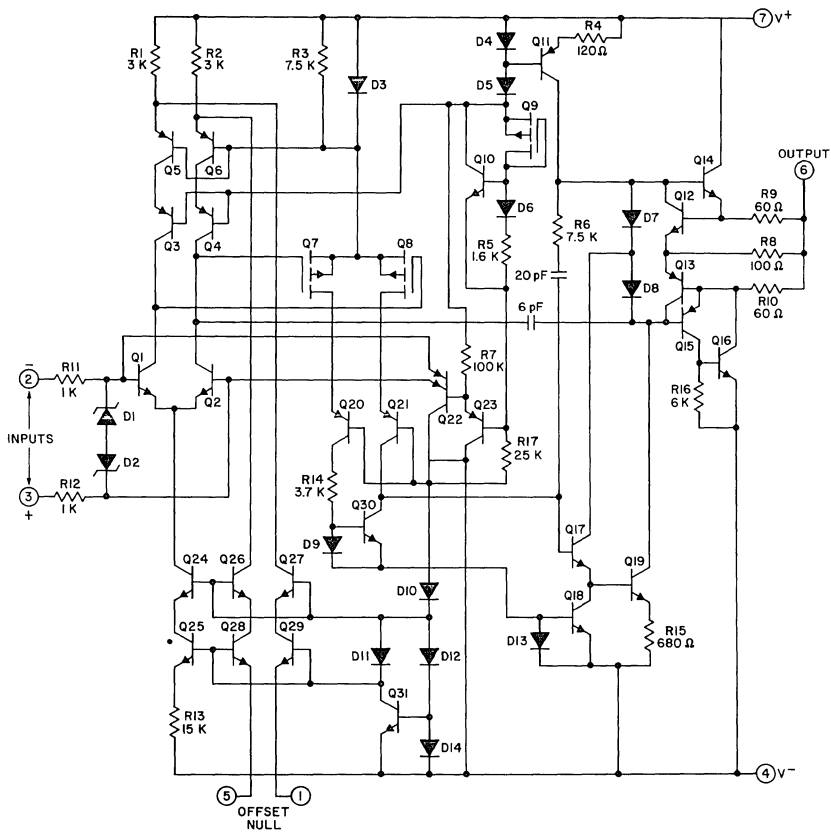


Fig. 4 - Schematic diagram of CA3193A and CA3193.

# CA3193A, CA3193

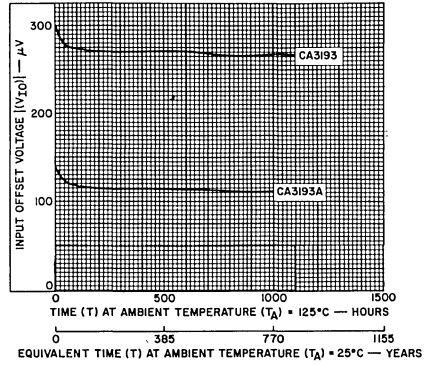
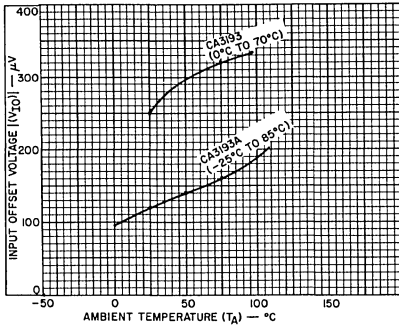


Fig. 5 - Typical input offset-voltage temperature characteristic for CA3193 series.

Fig. 6 - Input offset voltage vs. time.

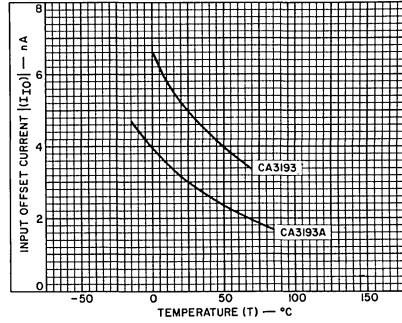
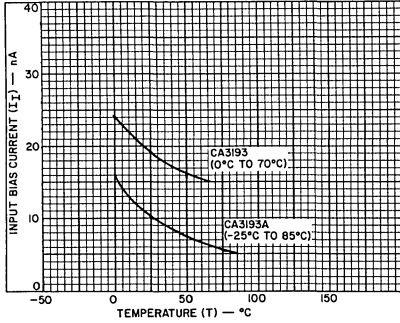


Fig. 7 - Typical input bias current vs. temperature.

Fig. 8 - Typical input offset current vs. temperature.

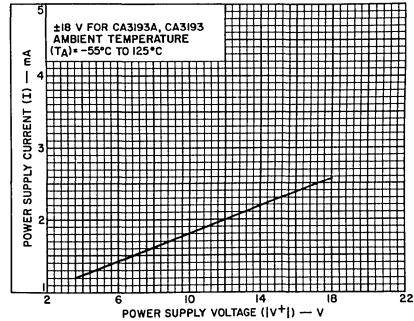
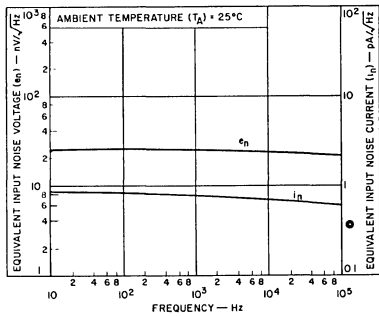


Fig. 9 - Input noise voltage and current density vs. frequency.

Fig. 10 - Power supply voltage ( $V^+$ ,  $V^-$ ) vs. supply current.

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OPERATIONAL  
AMPLIFIERS

# CA3193A, CA3193

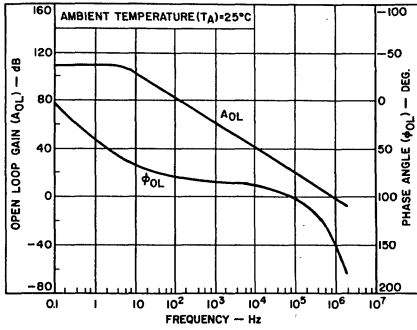


Fig. 11 - Open-loop gain and phase-shift response for CA3193B.

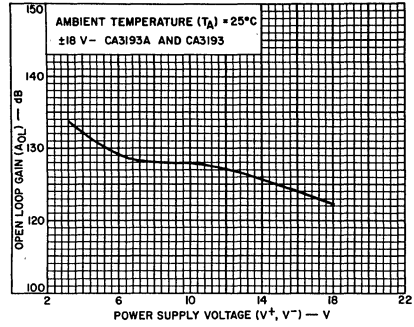


Fig. 12 - Open-loop gain vs. power-supply voltage.

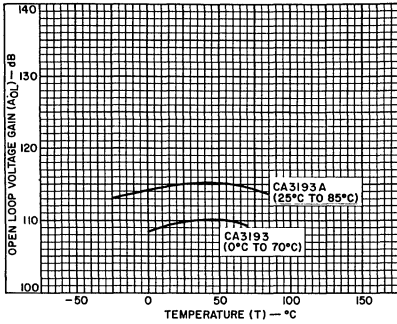


Fig. 13 - Open-loop gain vs. temperature for CA3193 series.

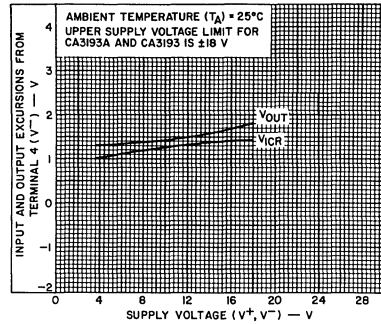


Fig. 14 - Maximum undistorted output voltage vs. frequency.

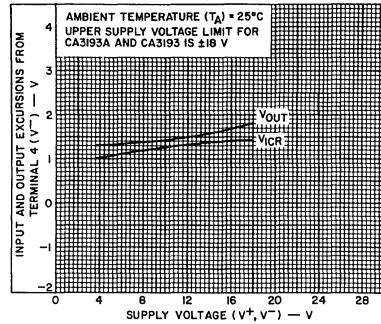


Fig. 15 - Output-voltage-swing capability and common-mode input-voltage vs. supply voltage.

## CA3193A, CA3193

### Offset Voltage Nulling

The input offset voltage can be nulled to zero by any of the three methods shown in the table below. A 10K potentiometer between terminals 1 and 5, with its wiper returned to  $V^-$ , will provide a gross nulling for all types. For finer nulling, either of the other two circuits shown below

may be used, thus providing simpler improved resolution for all types.

**CAUTION:** The CA3193 amplifiers will be damaged if they are plugged into op-amp circuits employing nulling with respect to the  $V^+$  supply bus.

### Offset Voltage Nulling

| Offset Nulling Circuits |                         |                          |                  |
|-------------------------|-------------------------|--------------------------|------------------|
| Type                    | Resistor R Value        | Resistor R Value         | Resistor R Value |
| CA3193A<br>CA3193       | 10K<br>10K              | 50K<br>20K               | 10K<br>5K        |
|                         | Gross Offset Adjustment | Finer Offset Adjustments |                  |

### TEST CIRCUITS

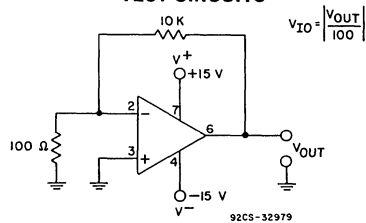
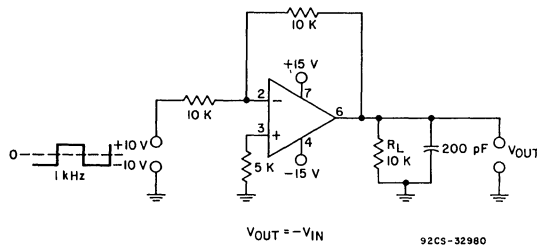
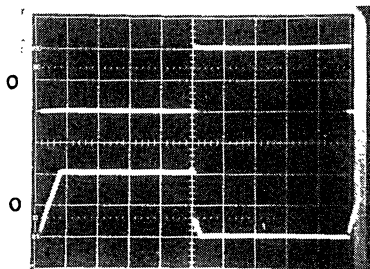


Fig. 16 - Input offset voltage test circuit.



a



b

TOP TRACE : INPUT VOLTAGE  
BOTTOM TRACE : OUTPUT VOLTAGE

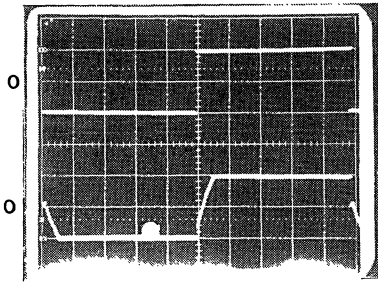
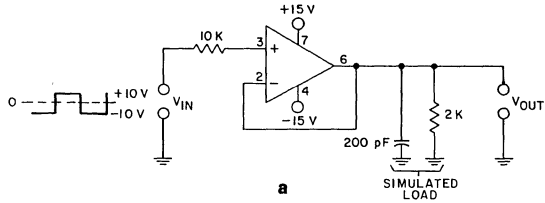
VERT.:  $\frac{10V}{DIV}$   $V^+ = 15V$   
 $V^- = -15V$

HOR.:  $\frac{.1ms}{DIV}$   $R_L = 10K$

92CS-32989

Fig. 17 - Inverting amplifier (a) test circuit (b) response to 1-kHz, 20-V p-p square wave.

# CA3193A, CA3193



TOP TRACE : INPUT VOLTAGE  
 BOTTOM TRACE : OUTPUT VOLTAGE

VERT: 10V  
 DIV

V+ = 15 V

V- = 15 V

HOR: .1ms  
 DIV

R<sub>L</sub> = 2K

Fig. 18 - Voltage follower (a) test circuit (b) response to 20-V p-p, 1-kHz square-wave input.

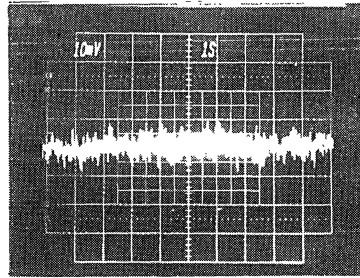
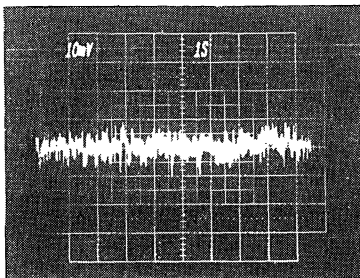
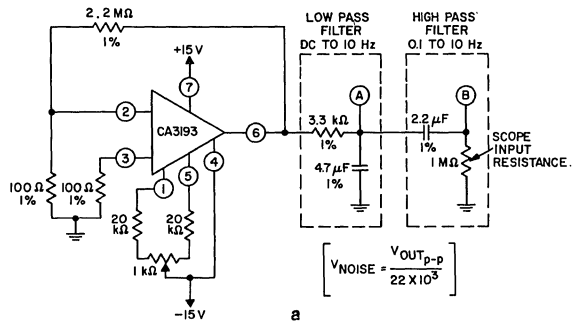
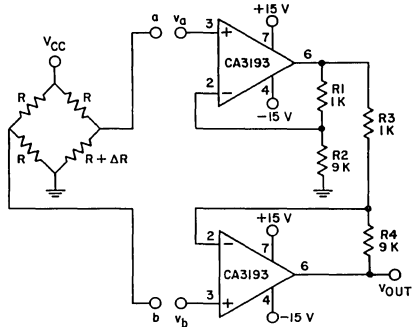


Fig. 19 - Low frequency noise (a) test circuit - 0.1 to 10 Hz (b) output A waveform - 0 to 10 Hz noise (c) output B waveform - 0 to 10 Hz noise.

# CA3193A, CA3193

## APPLICATION CIRCUITS



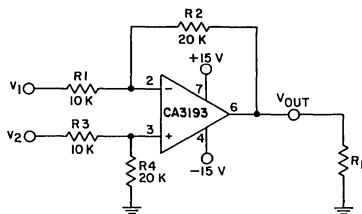
$$V_{OUT} = -V_a \left( \frac{R_2}{R_1} + 1 \right) \frac{R_4}{R_3} + V_b \left( \frac{R_4}{R_3} + 1 \right)$$

FOR IDEAL RESISTORS WITH  $\frac{R_1}{R_2} = \frac{R_3}{R_4}$

$$V_{OUT} = V_b - V_a \left( \frac{R_4}{R_3} + 1 \right)$$

$$A = \frac{V_{OUT}}{V_b - V_a} = \left( \frac{R_4}{R_3} + 1 \right)$$

FOR VALUES ABOVE  $V_{OUT} = (V_b - V_a) (10)$



ALL RESISTANCE VALUES ARE IN OHMS

$$V_{OUT} = V_2 \left( \frac{R_4}{R_3 + R_4} \right) \left( \frac{R_1 + R_2}{R_1} \right) - V_1 \left( \frac{R_2}{R_1} \right)$$

$$\text{IF } R_4 = R_2, R_3 = R_1 \text{ AND } \frac{R_2}{R_1} = \frac{R_4}{R_3}$$

$$\text{THEN } V_{OUT} = (V_2 - V_1) \left( \frac{R_2}{R_1} \right)$$

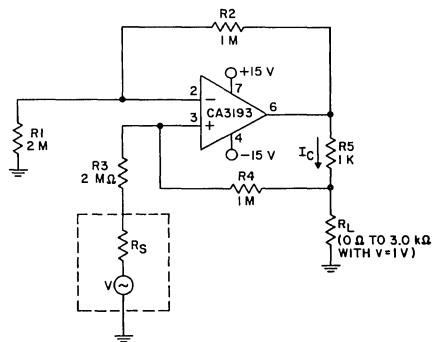
FOR VALUES ABOVE  $V_{OUT} = 2(V_2 - V_1)$

IF  $A_V$  IS TO BE MADE 1 AND IF  $R_1 = R_3 = R_4 = R$  WITH  $R_2 = 0.999R$  (0.1% MISMATCH IN  $R_2$ )

THEN  $V_{OCM} = 0.0005 V_{IN}$  OR  $CMRR = 66 \text{ dB}$   
 THUS, THE  $CMRR$  OF THIS CIRCUIT IS LIMITED BY THE MATCHING OR MISMATCHING OF THIS NETWORK RATHER THAN THE AMPLIFIER.

Fig. 20 - Typical two-op amp bridge-type differential amplifier.

Fig. 21 - Differential amplifier (simple subtractor) using CA3193.



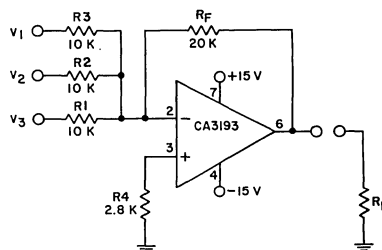
ALL RESISTORS ARE 1%

IF  $R_1 = R_3$  AND  $R_2 \approx R_4 + R_5$  THEN

$I_L$  IS INDEPENDENT OF VARIATIONS IN  $R_L$   
 FOR  $R_L$  VALUES OF  $0 \Omega$  TO  $3 \text{ k}\Omega$  WITH  $V = 1 \text{ V}$

$$I_L = \frac{V}{R_3} \frac{R_4}{R_5} = \frac{1 \text{ V}}{(2 \text{ M})} \frac{1 \text{ M}}{(1 \text{ K})} = \frac{1}{2} \mu\text{A} = 500 \mu\text{A}$$

Fig. 22 - Using CA3193 as a bilateral current source.



$$V_{OUT} = - \left( \frac{R_F}{R_1} V_1 + \frac{R_F}{R_2} V_2 + \frac{R_F}{R_3} V_3 \right)$$

$$V_{OUT} = - (2 V_1 + 2 V_2 + 2 V_3)$$

ALL RESISTANCE VALUES ARE IN OHMS

Fig. 23 - Typical summing amplifier application.

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OPERATIONAL AMPLIFIERS

## CA3193A, CA3193

The CA3193 is an excellent choice for use with thermocouples. In Fig. 24, the CA3193 amplifies the signal generated 500 times. The three 22-megohm resistors will provide full-scale output if the thermocouple opens.

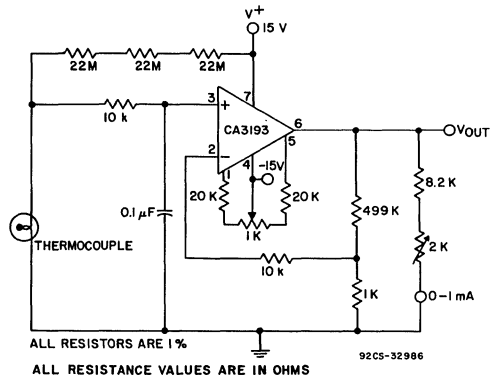


Fig. 24 - The CA3193 used in a thermocouple circuit.

# CA3240A CA3240

## Dual BiMOS Operational Amplifiers With MOSFET Input, Bipolar Output

August 1991

### Features

- Dual Version of CA3140
- Internally Compensated
- MOSFET Input Stage
  - (a) Very High Input Impedance ( $Z_{IN}$ ) ..... 1.5T $\Omega$  Typ.
  - (b) Very Low Input Current ( $I_I$ ) ..... 10pA Typ. at  $\pm 15V$
  - (c) Wide Common-Mode Input Voltage Range ( $V_{ICR}$ ): Can be Swung 0.5 Volt Below Negative Supply Voltage Rail
- Directly Replaces Industry Type 741 in Most Applications

### Applications

- Ground Referenced Single Supply Amplifiers in Automobile and Portable Instrumentation
- Sample and Hold Amplifiers
- Long Duration Timers/Multivibrators (Microseconds-Minutes-Hours)
- Photocurrent Instrumentation
- Active Filters
- Intrusion Alarm Systems
- Comparators
- Instrumentation Amplifiers
- Function Generators
- Power Supplies

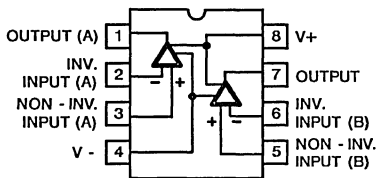
### Description

The CA3240A and CA3240 are dual versions of the popular CA3140 series integrated circuit operational amplifiers. They combine the advantages of MOS and bipolar transistors on the same monolithic chip. The gate-protected MOSFET (PMOS) input transistors provide high input impedance and a wide common-mode input voltage range (typically to 0.5V below the negative supply rail). The bipolar output transistors allow a wide output voltage swing and provide a high output current capability.

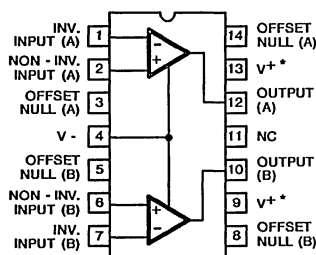
The CA3240A and CA3240 are supplied in the 8 lead dual-in-line plastic package (Mini-DIP, E suffix), and in the 14 lead dual-in-line plastic package (E1 suffix). The CA3240A and CA3240 are compatible with the industry standard 1458 operational amplifiers in similar packages. The CA3240A and CA3240 have an operating temperature range of  $-40^{\circ}C$  to  $+85^{\circ}C$ . The offset null feature is available only when these types are supplied in the 14 lead dual-in-line plastic package (E1 suffix). The CA3240 is also available in chip form (H suffix).

### Pinouts

**E SUFFIX**  
(Pin compatible with the industry standard 1458)  
TOP VIEW



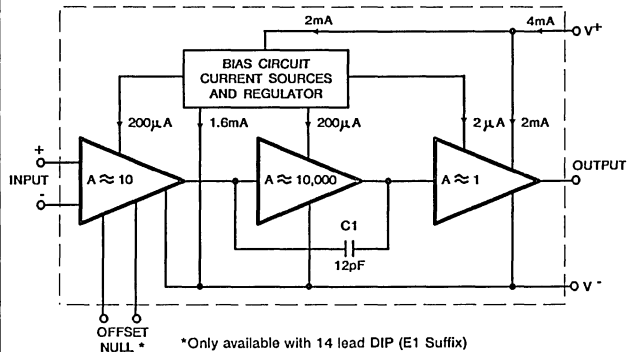
**E1 SUFFIX**  
TOP VIEW



\*Pins 9 & 13 internally connected through approximately 3 $\Omega$

FIGURE 1

### Block Diagram



\*Only available with 14 lead DIP (E1 Suffix)

FIGURE 2. BLOCK DIAGRAM OF ONE-HALF CA3240 SERIES



# CA3240A, CA3240

## MAXIMUM RATINGS, Absolute-Maximum Values:

|  |                                       |
|--|---------------------------------------|
| DC SUPPLY VOLTAGE<br>(BETWEEN $V^+$ AND $V^-$ TERMINALS) | 36 V                                  |
| OPERATING VOLTAGE RANGE                                  | 4 to 36 V<br>or $\pm 2$ to $\pm 18$ V |
| DIFFERENTIAL-MODE INPUT VOLTAGE                          | $\pm 8$ V                             |
| COMMON-MODE DC INPUT VOLTAGE                             | ( $V^+ + 8$ V) to ( $V^- - 0.5$ V)    |
| INPUT-TERMINAL CURRENT                                   | 1 mA                                  |
| DEVICE DISSIPATION:                                      |                                       |
| UP TO 55°C   | 630 mW                                |
| ABOVE 55°C   | Derate linearly 6.67 mW/°C            |
| TEMPERATURE RANGE:                                       |                                       |
| OPERATING  | -40 to +85°C                          |
| STORAGE  | -65 to +150°C                         |
| OUTPUT SHORT-CIRCUIT DURATION*                           | UNLIMITED                             |
| LEAD TEMPERATURE (DURING SOLDERING):                     |                                       |
| AT DISTANCE 1/16 $\pm$ 1/32 INCH (1.59 $\pm$ 0.79 MM)    |                                       |
| FROM CASE FOR 10 SECONDS MAX.                            | +265°C                                |

- \* Short circuit may be applied to ground or to either supply. Temperatures and/or supply voltages must be limited to keep dissipation within maximum rating.

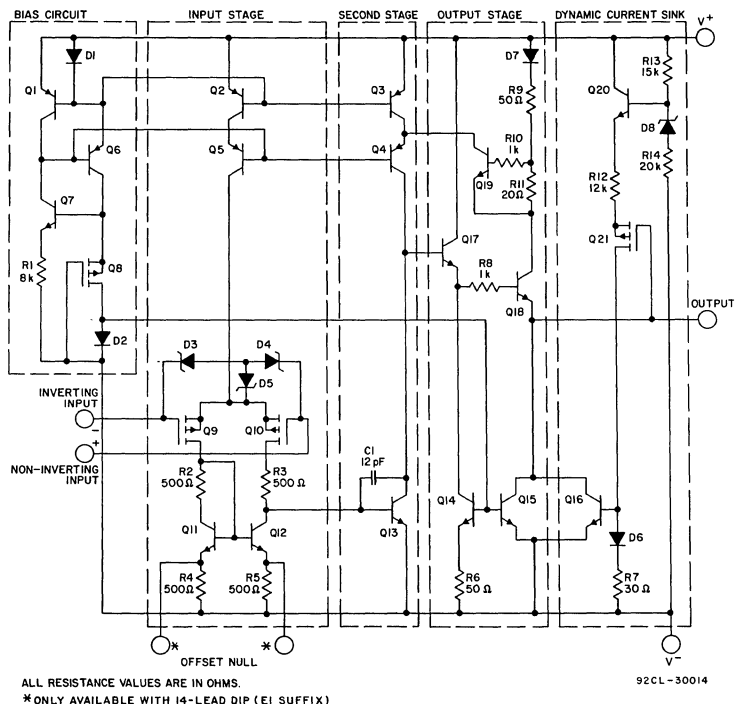


Fig. 2 - Schematic diagram of one-half CA3240 series.

### Circuit Description

The schematic diagram of one amplifier section of the CA3240 is shown in Fig. 2. It consists of a differential amplifier stage using PMOS transistors Q9 and Q10 with gate-to-source protection against static discharge damage provided by zener diodes D3, D4, and D5. Constant current bias is applied to the differential amplifier from transistors Q2

and Q5 connected as a constant-current source. This assures a high common-mode rejection ratio. The output of the differential amplifier is coupled to the base of gain stage transistor Q13 by means of an n-p-n current mirror that supplies the required differential-to-single-ended conversion. Provision for offset null for types in the 14-lead plastic package (E1 suffix) is provided through the use of this current mirror.

## CA3240A, CA3240

The gain stage transistor Q13 has a high-impedance active load (Q3 and Q4) to provide maximum open-loop gain. The collector of Q13 directly drives the base of the compound emitter-follower output stage. Pull-down for the output stage is provided by two independent circuits: (1) constant-current-connected transistors Q14 and Q15 and (2) dynamic current-sink transistor Q16 and its associated circuitry. *The level of pull-down current is constant at about 1 mA for Q15 and varies from 0 to 18 mA for Q16 depending on the magnitude of the voltage between the output terminal and  $V^+$ . The dynamic current sink becomes active whenever the output terminal is more negative*

than  $V^+$  by about 15 V. When this condition exists, transistors Q21 and Q16 are turned on causing Q16 to sink current from the output terminal to  $V^-$ . This current always flows when the output is in the linear region, either from the load resistor or from the emitter of Q18 if no load resistor is present. The purpose of this dynamic sink is to permit the output to go within 0.2 V ( $V_{CE(sat)}$ ) of  $V^-$  with a 2-k $\Omega$  load to ground. *When the load is returned to  $V^+$ , it may be necessary to supplement the 1 mA of current from Q15 in order to turn on the dynamic current sink (Q16). This may be accomplished by placing a resistor (approx. 2 k $\Omega$ ) between the output and  $V^-$ .*

### ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At  $V^+ = 15\text{ V}$ ,  $V^- = 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$  Unless Otherwise Specified

| CHARACTERISTIC   | LIMITS     |                |       |        |                |       | UNITS           |
|--|------------|----------------|-------|--------|----------------|-------|-----------------|
|  | CA3240A    |                |       | CA3240 |                |       |                 |
|  | Min.       | Typ.           | Max.  | Min.   | Typ.           | Max.  |                 |
| Input Offset Voltage, $ V_{IO} $   | –          | 2              | 5     | –      | 5              | 15    | mV              |
| Input Offset Current, $ I_{IO} $   | –          | 0.5            | 20    | –      | 0.5            | 30    | $\mu\text{A}$   |
| Input Current, $I_I$   | –          | 10             | 40    | –      | 10             | 50    | $\mu\text{A}$   |
| Large-Signal Voltage Gain, $A_{OL}$<br>(See Figs. 4, 19)                               | 20 k       | 100 k          | –     | 20 k   | 100 k          | –     | V/V             |
|  | 86         | 100            | –     | 86     | 100            | –     | dB              |
| Common-Mode Rejection Ratio, CMRR<br>(See Fig. 9)                                      | –          | 32             | 320   | –      | 32             | 320   | $\mu\text{V/V}$ |
|  | 70         | 90             | –     | 70     | 90             | –     | dB              |
| Common-Mode Input-Voltage Range, $V_{ICR}$<br>(See Fig. 16)                            | –15        | –15.5 to +12.5 | 12    | –15    | –15.5 to +12.5 | 11    | V               |
| Power-Supply Rejection Ratio, $\frac{\Delta V_{IO}}{\Delta V}$ , PSRR<br>(See Fig. 11) | –          | 100            | 150   | –      | 100            | 150   | $\mu\text{V/V}$ |
|  | 76         | 80             | –     | 76     | 80             | –     | dB              |
| Maximum Output Voltage, $V_{OM}$<br>(See Figs. 22, 16)                                 | $V_{OM}^+$ | +12            | 13    | –      | +12            | 13    | V               |
|  | $V_{OM}^-$ | –14            | –14.4 | –      | –14            | –14.4 |                 |
| Maximum Output Voltage, $V_{OM}^-$<br>$\dagger$  | 0.4        | 0.13           | –     | 0.4    | 0.13           | –     | V               |
| Supply Current, $I^+$<br>(See Fig. 7)<br>For Both Amps.                                | –          | 8              | 12    | –      | 8              | 12    | mA              |
| Total Device Dissipation, $P_D$  | –          | 240            | 360   | –      | 240            | 360   | mW              |

$\bullet$  At  $V_O = 26\text{ V}_{p-p}$ , +12 V, –14 V and  $R_L = 2\text{ k}\Omega$ .

$\blacksquare$  At  $R_L = 2\text{ k}\Omega$ .

$\dagger$  At  $V^+ = 5\text{ V}$ ,  $V^- = \text{GND}$ ,  $I_{\text{Sink}} = 200\ \mu\text{A}$ .

## CA3240A, CA3240

### TYPICAL ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC   | TEST CONDITIONS<br>$V^+ = +15\text{ V}$<br>$V^- = -15\text{ V}$<br>$T_A = 25^\circ\text{C}$     |  | TYPICAL VALUES     |         | UNITS                  |               |    |    |                              |
|--|---|--|--------------------|---------|------------------------|---------------|----|----|------------------------------|
|  |   |  | CA3240A            | CA3240  |                        |               |    |    |                              |
| Input Offset Voltage Adjustment Resistor (E1 Package Only) | Typ. Value of Resistor Between Terms. 4 and 3(5) or Between 4 and 14(8) to Adjust Max. $V_{IO}$ |  | 18                 | 4.7     | $k\Omega$              |               |    |    |                              |
| Input Resistance $R_I$                                     |   |  | 1.5                | 1.5     | $T\Omega$              |               |    |    |                              |
| Input Capacitance $C_I$                                    |   |  | 4                  | 4       | pF                     |               |    |    |                              |
| Output Resistance $R_O$                                    |   |  | 60                 | 60      | $\Omega$               |               |    |    |                              |
| Equivalent Wideband Input Noise Voltage (See Fig. 21)      | $e_n$   | BW=140 kHz<br>$R_S = 1\text{ M}\Omega$   | 48                 | 48      | $\mu\text{V}$          |               |    |    |                              |
| Equivalent Input Noise Voltage (See Fig. 10)               | $e_n$   | <table border="1" style="display: inline-table; border-collapse: collapse;"> <tr> <td style="padding: 2px;"><math>f = 1\text{ kHz}</math></td> <td style="padding: 2px;"><math>R_S =</math></td> </tr> <tr> <td style="padding: 2px;"><math>f = 10\text{ kHz}</math></td> <td style="padding: 2px;"><math>100\ \Omega</math></td> </tr> </table> | $f = 1\text{ kHz}$ | $R_S =$ | $f = 10\text{ kHz}$    | $100\ \Omega$ | 40 | 40 | $n\text{V}/\sqrt{\text{Hz}}$ |
| $f = 1\text{ kHz}$   | $R_S =$   |  |                    |         |                        |               |    |    |                              |
| $f = 10\text{ kHz}$  | $100\ \Omega$   |  |                    |         |                        |               |    |    |                              |
| Short-Circuit Current to Opposite Supply Source            | $I_{OM}^+$  |  | 40                 | 40      | mA                     |               |    |    |                              |
| Sink   | $I_{OM}^-$  |  | 11                 | 11      |                        |               |    |    |                              |
| Gain-Bandwidth Product (See Figs. 5 and 19)                | $f_T$   |  | 4.5                | 4.5     | MHz                    |               |    |    |                              |
| Slew Rate (See Fig. 6)                                     | SR  |  | 9                  | 9       | $\text{V}/\mu\text{s}$ |               |    |    |                              |
| Transient Response: Rise Time                              | $t_r$   | $R_L = 2\text{ k}\Omega$   | 0.08               | 0.08    | $\mu\text{s}$          |               |    |    |                              |
| Overshoot (See Fig. 20)                                    |   | $C_L = 100\text{ pF}$  | 10                 | 10      | %                      |               |    |    |                              |
| Settling Time at 10 V <sub>p-p</sub> (See Fig. 17)         | $t_s$   | $R_L = 2\text{ k}\Omega$<br>$C_L = 100\text{ pF}$  | 4.5                | 4.5     | $\mu\text{s}$          |               |    |    |                              |
|  |   | Voltage Follower   | 1.4                | 1.4     |                        |               |    |    |                              |
| Crosstalk  |   | $f = 1\text{ kHz}$   | 120                | 120     | dB                     |               |    |    |                              |

# CA3240A, CA3240

## ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At  $V^+ = 15\text{ V}$ ,  $V^- = 15\text{ V}$ ,  $T_A = -40$  to  $+85^\circ\text{C}$  Unless Otherwise Specified

| CHARACTERISTIC  | TYPICAL VALUES     |                    | UNITS                        |
|---|--------------------|--------------------|------------------------------|
|   | CA3240A            | CA3240             |                              |
| Input Offset Voltage, $ V_{IO} $  | 3                  | 10                 | mV                           |
| Input Offset Current, $ I_{IO} $  | 32                 | 32                 | pA                           |
| Input Current, $I_I$  | 640                | 640                | pA                           |
| Large-Signal Voltage Gain, $A_{OL}$<br>(See Figs. 4, 19)                                | 63 k               | 63 k               | V/V                          |
|   | 96                 | 96                 | dB                           |
| Common-Mode Rejection Ratio, CMRR<br>(See Fig. 9)                                       | 32                 | 32                 | $\mu\text{V/V}$              |
|   | 90                 | 90                 | dB                           |
| Common-Mode Input-Voltage Range, $V_{ICR}$<br>(See Fig. 16)                             | -15<br>to<br>+12.3 | -15<br>to<br>+12.3 | V                            |
| Power-Supply Rejection Ratio, $\frac{\Delta V_{IO}}{\Delta V}$<br>PSRR<br>(See Fig. 11) | 150                | 150                | $\mu\text{V/V}$              |
|   | 76                 | 76                 | dB                           |
| Maximum Output Voltage, $V_{OM}$<br>(See Figs. 16, 22)                                  | $V_{OM}^+$         | 12.4               | V                            |
|   | $V_{OM}^-$         | -14.2              |                              |
| Supply Current, $I^+$<br>(See Fig. 7) For Both Amps.                                    | 8.4                | 8.4                | mA                           |
| Total Device Dissipation, $P_D$   | 252                | 252                | mW                           |
| Temperature Coefficient of Input Offset Voltage, $\Delta V_{IO}/\Delta T$               | 15                 | 15                 | $\mu\text{V}/^\circ\text{C}$ |

● At  $V_O = 26\text{ V}_{\text{p-p}}$ ,  $+12\text{ V}$ ,  $-14\text{ V}$  and  $R_L = 2\text{ k}\Omega$ .

■ At  $R_L = 2\text{ k}\Omega$ .

◆ At  $T_A = 85^\circ\text{C}$

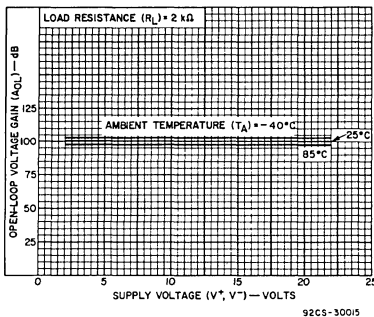


Fig. 4 — Open-loop voltage gain as a function of supply voltage and temperature.

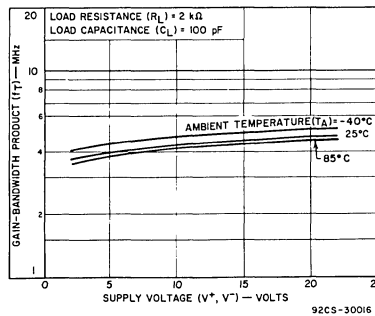


Fig. 5 — Gain-bandwidth product as a function of supply voltage and temperature.

## CA3240A, CA3240

**TYPICAL ELECTRICAL CHARACTERISTICS FOR DESIGN GUIDANCE**  
At  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$

| CHARACTERISTIC                                       |                             | TYPICAL VALUES |            | UNITS                  |
|--|-----------------------------|----------------|------------|------------------------|
|  |                             | CA3240A        | CA3240     |                        |
| Input Offset Voltage,                                | $ V_{IO} $                  | 2              | 5          | mV                     |
| Input Offset Current,                                | $ I_{IO} $                  | 0.1            | 0.1        | pA                     |
| Input Current,                                       | $I_I$                       | 2              | 2          | pA                     |
| Input Resistance                                     |                             | 1              | 1          | $\text{T}\Omega$       |
| Large-Signal Voltage Gain,<br>(See Figs. 4, 19)      | $A_{OL}$                    | 100 k          | 100 k      | V/V                    |
|  |                             | 100            | 100        | dB                     |
| Common-Mode Rejection Ratio, CMRR                    |                             | 32             | 32         | $\mu\text{V/V}$        |
|  |                             | 90             | 90         | dB                     |
| Common-Mode Input-Voltage<br>Range,<br>(See Fig. 22) | $V_{ICR}$                   | -0.5           | -0.5       | V                      |
|  |                             | 2.6            | 2.6        |                        |
| Power-Supply Rejection Ratio, PSRR                   |                             | 31.6           | 31.6       | $\mu\text{V/V}$        |
|  |                             | 90             | 90         | dB                     |
| Maximum Output Voltage,<br>(See Figs. 16, 22)        | $\frac{V_{OM}^+}{V_{OM}^-}$ | 3              | 3          | V                      |
|  |                             | 0.3            | 0.3        |                        |
| Maximum Output Current:<br>Source,                   | $I_{OM}^+$                  | 20             | 20         | mA                     |
|  |                             | Sink           | $I_{OM}^-$ |                        |
| Slew Rate (See Fig. 6)                               |                             | 7              | 7          | $\text{V}/\mu\text{s}$ |
| Gain-Bandwidth Product,<br>(See Fig. 5)              | $f_T$                       | 4.5            | 4.5        | MHz                    |
| Supply Current,<br>(See Fig. 7)                      | $I^+$                       | 4              | 4          | mA                     |
| Device Dissipation,                                  | $P_D$                       | 20             | 20         | mW                     |

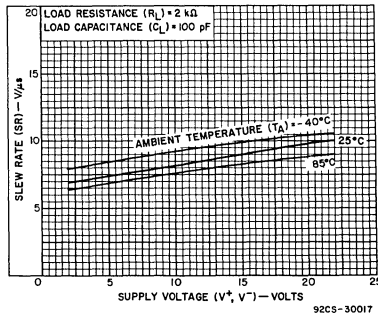


Fig. 6 — Slew rate as a function of supply voltage and temperature.

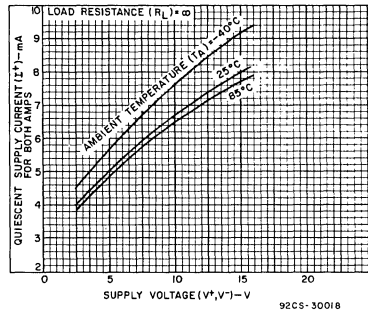


Fig. 7 — Quiescent supply current as a function of supply voltage and temperature.

# CA3240A, CA3240

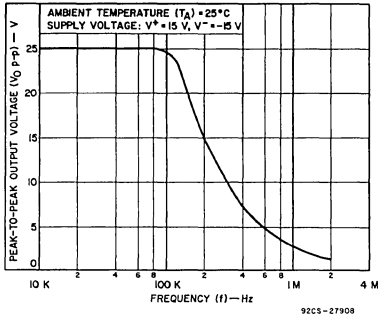


Fig. 8 — Maximum output voltage swing as a function of frequency.

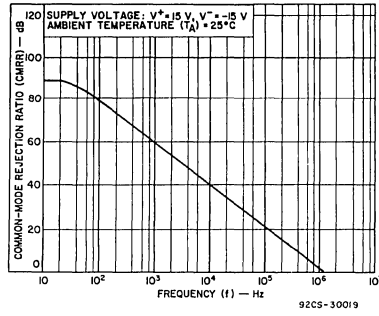


Fig. 9 — Common-mode rejection ratio as a function of frequency.

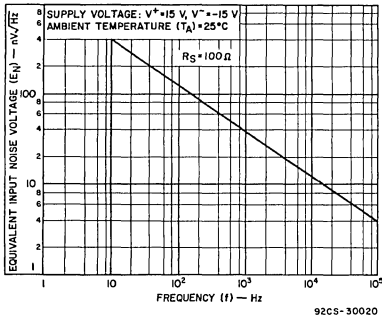


Fig. 10 — Equivalent input noise voltage as a function of frequency.

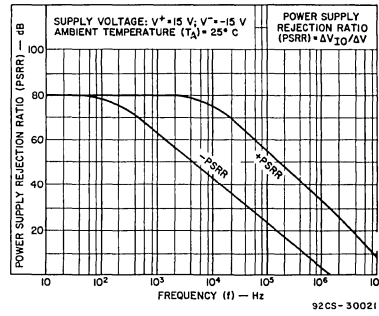


Fig. 11 — Power supply rejection ratio as a function of frequency.

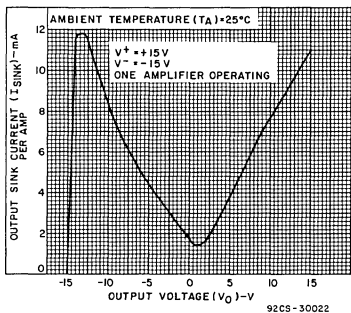


Fig. 12 — Output sink current as a function of output voltage.

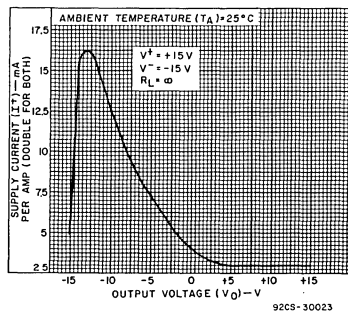


Fig. 13 — Supply current as a function of output voltage.

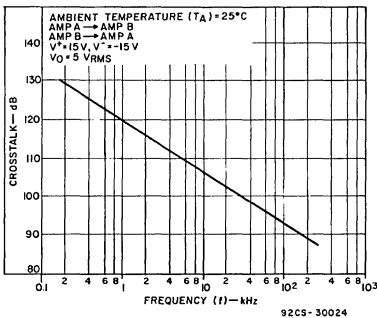


Fig. 14 — Crosstalk as a function of frequency.

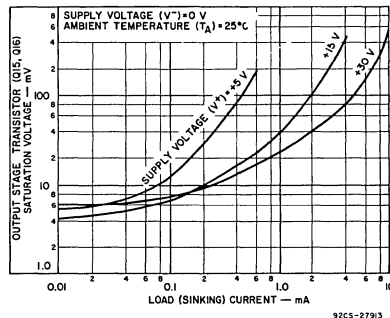


Fig. 15 — Voltage across output transistors Q15 and Q16 as a function of load current.

# CA3240A, CA3240

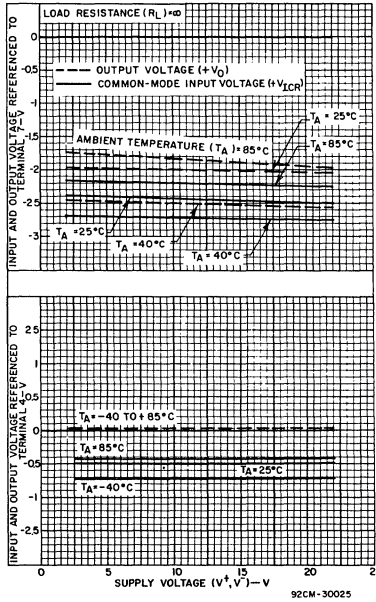


Fig. 16 - Output-voltage-swing capability and common-mode input-voltage range as a function of supply voltage and temperature.

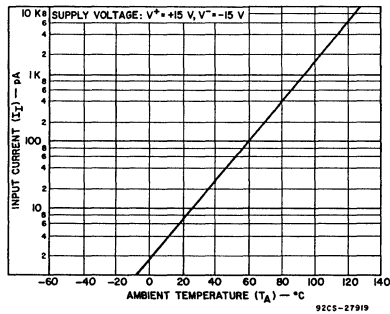


Fig. 18 - Input current as a function of ambient temperature.

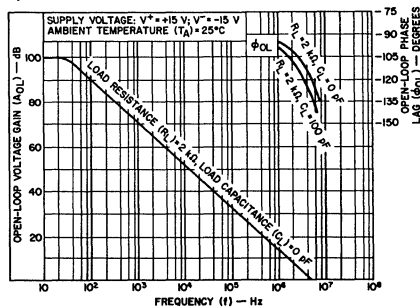
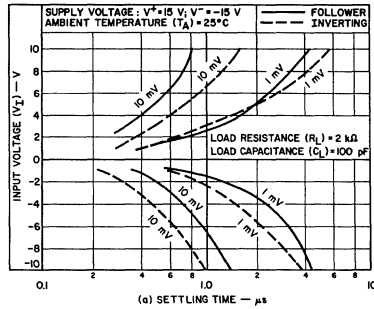
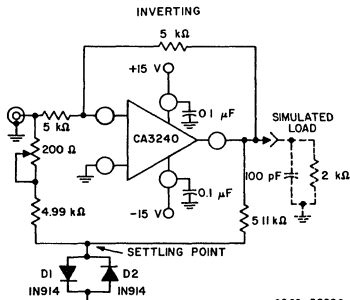
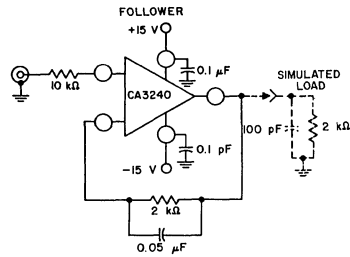


Fig. 19 - Open-loop voltage gain and phase lag as a function of frequency.



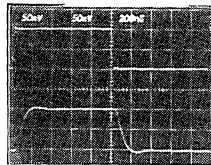
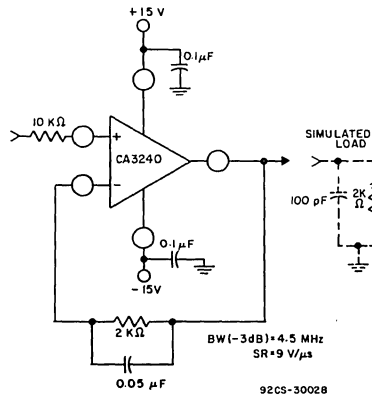
(a) SETTLING TIME - μs



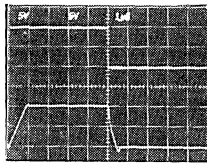
(b) TEST CIRCUITS

Fig. 17 - Input voltage as a function of settling time.

# CA3240A, CA3240



(a) SMALL SIGNAL RESPONSE

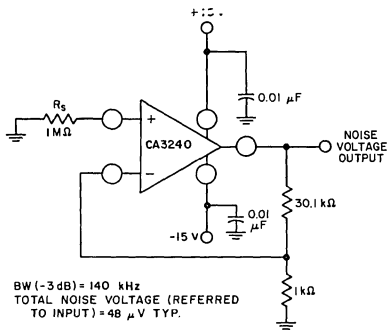


(b) LARGE SIGNAL RESPONSE

TOP TRACE: INPUT  
(50 mV/DIV; 200 ns/DIV)  
BOTTOM TRACE: OUTPUT  
(50 mV/DIV; 200 ns/DIV)

TOP TRACE: INPUT  
(5 V/DIV; 1 μs/DIV.)  
BOTTOM TRACE: OUTPUT  
(5 V/DIV; 1 ns/DIV)

Fig. 20 — Split-supply voltage-follower test circuit and associated waveforms.



92CS-30027  
BW (-3dB) = 140 kHz  
TOTAL NOISE VOLTAGE (REFERRED TO INPUT) = 48 μV TYP.

Fig. 21 — Test-circuit amplifier (30-dB gain) used for wideband noise measurement.

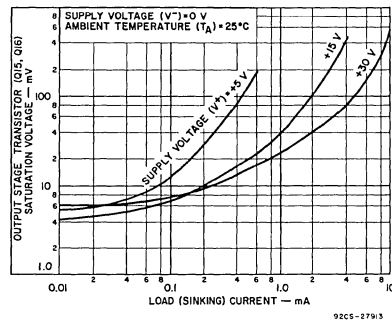


Fig. 22 — Voltage across output transistors Q15 and Q16 as a function of load current.



APPLICATIONS CONSIDERATIONS

Output Circuit Considerations

Fig. 22 shows output current-sinking capabilities of the CA3240 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level-shifting circuitry usually associated with the 741 series of operational amplifiers.

Fig. 23 shows some typical configurations. Note that a series resistor,  $R_L$ , is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

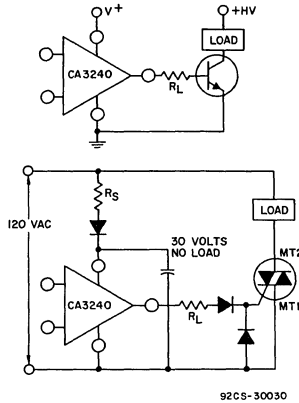


Fig. 23 — Methods of utilizing the  $V_{CE(sat)}$  sinking-current capability of the CA3240 series.

Input Circuit Considerations

As indicated by the typical VICR, this device will accept inputs as low as 0.5 V below  $V^-$ . However, a series current-limiting resistor is recommended to limit the maximum input terminal current to less than 1 mA to prevent damage to the input protection circuitry.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3240 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9-k $\Omega$  resistor is sufficient.

The typical input current is in the order of 10 pA when the inputs are centered at nominal device dissipation. As the output supplies

load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Fig. 24 shows typical input-terminal current versus ambient temperature for the CA3240.

It is well known that MOS/FET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. In typical linear applications, where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage.

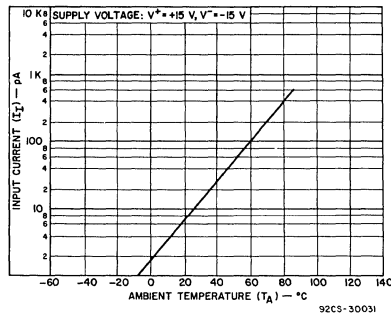


Fig. 24 — Input current as a function of ambient temperature.

Offset-Voltage Nulling

The input-offset voltage of the CA3240AE1 and CA3240E1 can be nulled by connecting a 10-k $\Omega$  potentiometer between Terminals 3 and 14 or 5 and 8 and returning its wiper arm to Terminal 4, see Fig. 25a. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors that may be placed at either end of the potentiometer, see Fig. 25b, to optimize its utilization range are given in the table "Electrical Characteristics For Design Guidance" shown in this bulletin.

An alternate system is shown in Fig. 25c. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to zero ohms at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

## CA3240A, CA3240

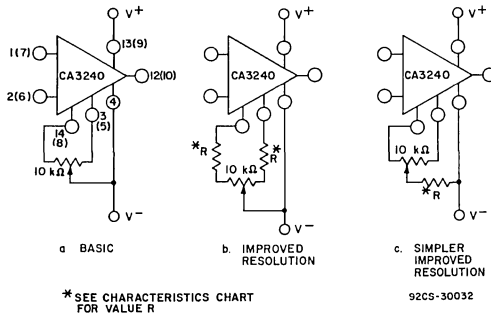


Fig. 25 — Three offset-voltage nulling methods.  
(CA3240AE1, CA3240E1 only.)

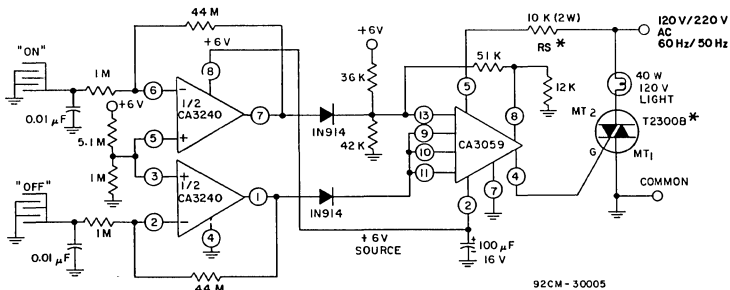
## TYPICAL APPLICATIONS

### On/Off Touch Switch

The on/off touch switch shown in Fig. 26 uses the CA3240E to sense small currents flowing between two contact points on a touch plate consisting of a PC board metallization "grid". When the "on" plate is touched, current flows between the two halves of the grid causing a positive shift in the output voltage (Term. 7) of the CA3240E. These positive transitions are fed into the CA3059, which is used as a latching circuit and zero-crossing triac driver. When a positive pulse occurs at Terminal 7 of the CA3240E,

the triac is turned on and held on by the CA3059 and its associated positive feedback circuitry (51-k $\Omega$  resistor and 36-k $\Omega$ /42-k $\Omega$  voltage divider). When the positive pulse occurs at Terminal 1 (CA3240E), the triac is turned off and held off in a similar manner. Note that power for the CA3240E is supplied by the CA3059 internal power supply.

The advantage of using the CA3240E in this circuit is that it can sense the small currents associated with skin conduction while allowing sufficiently high circuit impedance to provide protection against electrical shock.



\* AT 220 V OPERATION, TRIAC SHOULD BE T2300D,  
RS = 18 K, 5 W

Fig. 26 — On/off touch switch.

## CA3240A, CA3240

### Dual Level Detector (window comparator)

Fig. 27 illustrates a simple dual liquid level detector using the CA3240E as the sensing amplifier. This circuit operates on the principle that most liquids contain enough ions in solution to sustain a small amount of current flow between two electrodes submersed in the liquid. The current, induced by an 0.5-V potential across two halves of a

PC board grid, is converted to a voltage level by the CA3240E in a circuit similar to that of the on/off touch switch shown in Fig. 26. The changes in voltage for both the upper and lower level sensors are processed by the CA3140 to activate an LED whenever the liquid level is above the upper sensor or below the lower sensor.

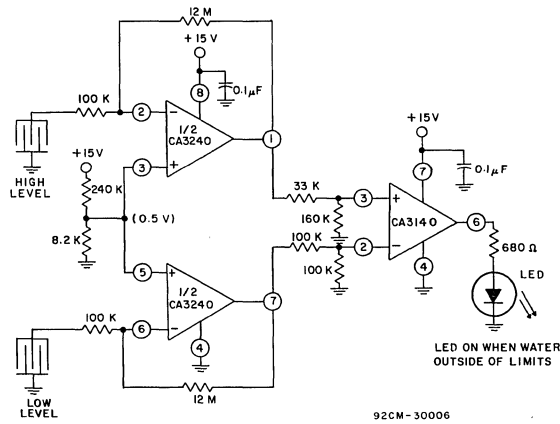


Fig. 27 — Dual level detector.

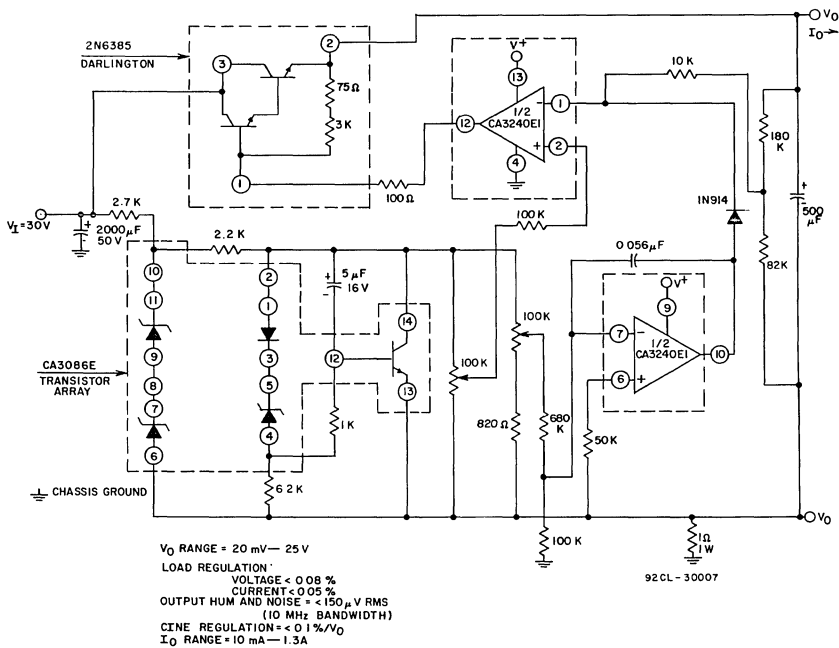


Fig. 28 — Constant-voltage/constant-current power supply.

## CA3240A, CA3240

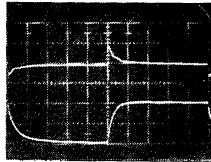
### Constant-Voltage/Constant-Current Power Supply

The constant-voltage/constant-current power supply shown in Fig. 28 uses the CA3240E as a voltage-error and current-sensing amplifier. The CA3240E is ideal for this application because its input common-mode voltage-range includes ground, allowing the supply to adjust from 20 mV to 25 V without requiring an additional negative input voltage. Also, the ground reference capability of the CA3240E allows it to sense the voltage across

29 shows the transient response of the supply during a 100-mA to 1-A load transition.

### Precision Differential Amplifier

Fig. 30 shows the CA3240E in the classical precision differential amplifier circuit. The CA3240E is ideally suited for biomedical applications because of its extremely high input impedance. To insure patient safety, an extremely high electrode series resistance is required to limit any current that might



TRANSIENT RESPONSE

TOP TRACE: OUTPUT VOLTAGE  
(500 mV/cm AND 5  $\mu$ s/cm)  
BOTTOM TRACE: COLLECTOR OF LOAD  
SWITCHING TRANSISTOR  
LOAD = 100 mA TO 1 A  
(5 V/cm AND 5  $\mu$ s/cm)

92CS-30034

Fig. 29 — Transient response.

the 1- $\Omega$  current-sensing resistor in the negative output lead of the power supply. The CA3086 transistor array functions as a reference for both constant-voltage and constant-current limiting. The 2N6385 power Darlington is used as the pass element and may be required to dissipate as much as 40 W. Fig.

result in patient discomfort in the event of a fault condition. In this case, 10-M $\Omega$  resistors have been used to limit the current to less than 2  $\mu$ A without affecting the performance of the circuit. Fig. 31 shows a typical electrocardiogram waveform obtained with this circuit.

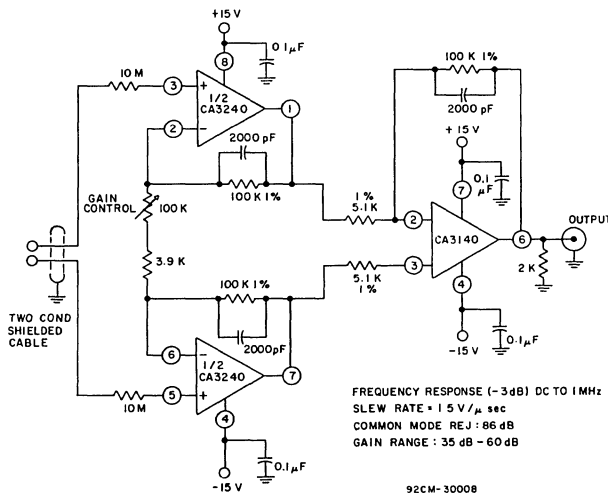
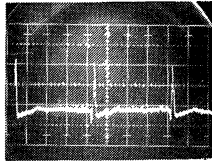


Fig. 30 — Precision differential amplifier.

## CA3240A, CA3240



TYPICAL ELECTROCARDIOGRAM WAVEFORM

VERTICAL : 1.0 mV/DIV  
 (AMPLIFIER GAIN = 100 X)  
 (SCOPE SENSITIVITY = 0.1V/DIV.)  
 HORIZONTAL : > 0.2 SEC/DIV (UNCAL)

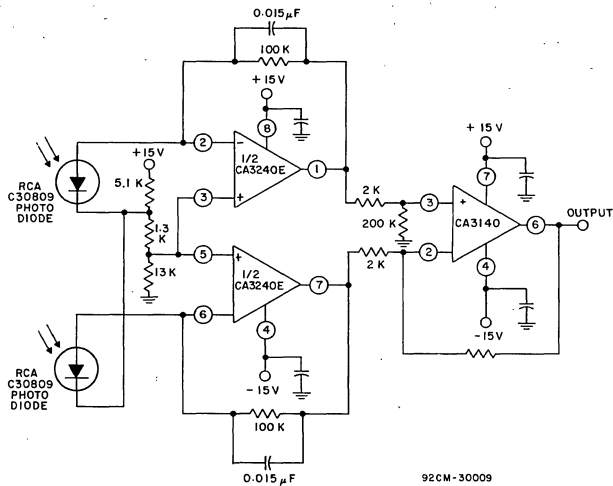
92CS-30033

Fig. 31 – Typical electrocardiogram waveform.

### Differential Light Detector

In the circuit shown in Fig. 32, the CA3240E converts the current from two photo diodes to voltage, and applies 1 V of reverse bias to the diodes. The voltages from the CA3240E outputs are subtracted in the second stage

(CA3140) so that only the difference is amplified. In this manner, the circuit can be used over a wide range of ambient light conditions without circuit component adjustment. Also, when used with a light source, the circuit will not be sensitive to changes in light level as the source ages.



92CM-30009

Fig. 32 – Differential light detector.

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### Features

- MOSFET Input Stage provides
  - ▶ Very High  $Z_i = 1.5T\Omega$  ( $1.5 \times 10^{12}\Omega$ ) Typ.
  - ▶ Very Low  $I_i = 5\text{pA}$  Typ. at 15V Operation  
= 2pA Typ. at 5V Operation
- Ideal for Single Supply Applications
- Common-Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (Or Both) Supply Rails

### Applications

- Ground Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long Duration Timers/Monostables
- Ideal Interface with Digital CMOS
- High Input Impedance Wide-band Amplifiers
- Voltage Followers (e.g. Follower for Single Supply D/A Converter)
- Voltage Regulators (Permits Control of Output Voltage Down to Zero Volts)
- Wien-Bridge Oscillators
- Voltage Controlled Oscillators
- Photo Diode Sensor Amplifiers

### Description

CA3260A and CA3260 are integrated circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. The CA3260 series circuits are dual versions of the popular CA3160 series.

Gate-protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very high input impedance, very low input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input voltage capability down to 0.5 volt below the negative supply terminal, an important attribute in single supply applications.

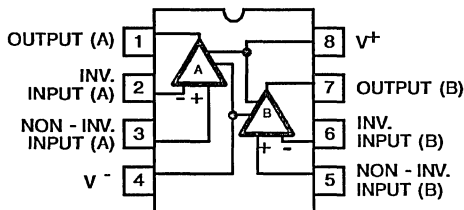
A complementary symmetry MOS (CMOS) transistor pair, capable of swinging the output voltage to within 10 millivolts of either supply voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3260 Series circuits operate at supply voltages ranging from 4 to 16 volts, or  $\pm 2$  to  $\pm 8$  volts when using split supplies. The CA3260 Series is supplied in standard 8 lead TO-5 style packages (T suffix) and 8 lead dual-in-line formed lead TO-5 style "DIL-CAN" packages (S suffix). The CA3260 is available in chip form (H suffix).

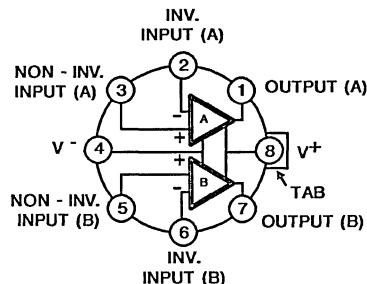
The CA3260 and CA3260A are also available in the 8 lead dual-in-line plastic package (Mini-DIP E suffix). All types operate over the full military temperature range of  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ . The CA3260A offers superior input characteristics over those of the CA3260.

### Pinouts

**E SUFFIX**  
(Pin compatible with the industry standard 1458)  
TOP VIEW



**S AND T SUFFIXES**  
(Pin compatible with the industry standard 1458)  
TOP VIEW



CA3260A, CA3260

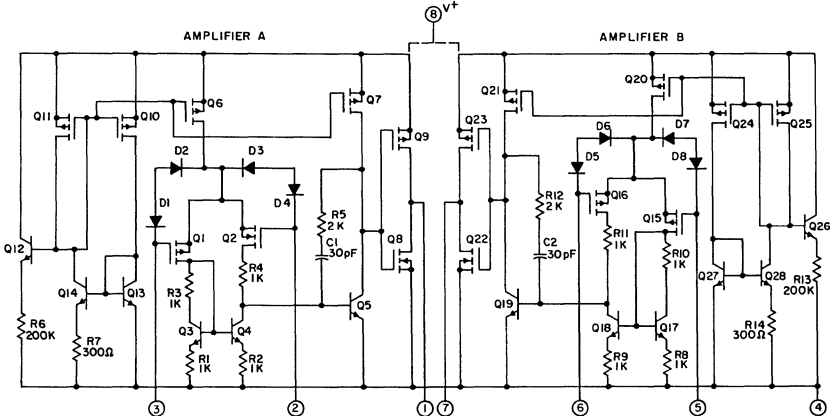


Fig. 1 - Schematic diagram of CA3260 series.

## CA3260A, CA3260

**ELECTRICAL CHARACTERISTICS** for Each Amplifier at  $T_A=25^\circ\text{C}$ ,  
 $V^+=15\text{ V}$ ,  $V^-=0\text{ V}$  (Unless otherwise specified)

| CHARACTERISTIC   | LIMITS                    |                  |       |                |                  |       | UNITS                        |
|--|---------------------------|------------------|-------|----------------|------------------|-------|------------------------------|
|  | CA3260A (T,S,E)           |                  |       | CA3260 (T,S,E) |                  |       |                              |
|  | Min.                      | Typ.             | Max.  | Min.           | Typ.             | Max.  |                              |
| Input Offset Voltage,<br>$ V_{IO} $ , $V^{\pm}=\pm 7.5\text{ V}$                                 | —                         | 2                | 5     | —              | 6                | 15    | mV                           |
| Input Offset Current,<br>$ I_{IO} $ , $V^{\pm}=\pm 7.5\text{ V}$                                 | —                         | 0.5              | 20    | —              | 0.5              | 30    | pA                           |
| Input Current, $I_I$<br>$V^{\pm}=\pm 7.5\text{ V}$   | —                         | 5                | 30    | —              | 5                | 50    | pA                           |
| Large-Signal Voltage<br>Gain, $A_{OL}$   | 50 k                      | 320 k            | —     | 50 k           | 320 k            | —     | V/V                          |
| $V_O=10\text{ V}_{p-p}$ , $R_L=10\text{ k}\Omega$  | 94                        | 110              | —     | 94             | 110              | —     | dB                           |
| Common-Mode<br>Rejection Ratio, CMRR   | 80                        | 95               | —     | 70             | 90               | —     | dB                           |
| Common-Mode Input<br>Voltage Range, $V_{ICR}$  | 0                         | -0.5<br>to<br>12 | 10    | 0              | -0.5<br>to<br>12 | 10    | V                            |
| Power-Supply Rejection<br>Ratio, $\Delta V_{IO}/\Delta V^{\pm}$<br>$V^{\pm}=\pm 7.5\text{ V}$    | —                         | 32               | 150   | —              | 32               | 320   | $\mu\text{V}/\text{V}$       |
| Maximum Output<br>Voltage:   |                           |                  |       |                |                  |       |                              |
| At $R_L=10\text{ k}\Omega$   | $\frac{V_{OM}^+}{V_{OM}}$ | 11               | 13.3  | —              | 11               | 13.3  | —                            |
|  | $\frac{V_{OM}^+}{V_{OM}}$ | —                | 0.002 | 0.01           | —                | 0.002 | 0.01                         |
| At $R_L=\infty$  | $\frac{V_{OM}^+}{V_{OM}}$ | 14.99            | 15    | —              | 14.99            | 15    | —                            |
|  | $\frac{V_{OM}^+}{V_{OM}}$ | —                | 0     | 0.01           | —                | 0     | 0.01                         |
| Maximum Output<br>Current,<br>$I_{OM}^+$ (Source) @<br>$V_O=7.5\text{ V}$                        | 12                        | 22               | 45    | 12             | 22               | 45    | mA                           |
| $I_{OM}$ (Sink) @<br>$V_O=7.5\text{ V}$  | 12                        | 20               | 45    | 12             | 20               | 45    |                              |
| Total<br>Supply Current, $I^+$<br>$R_L=\infty$<br>$V_O$ (Ampli.A)=7.5 V<br>$V_O$ (Ampli.B)=7.5 V | —                         | 9                | 15.5  | —              | 9                | 15.5  | mA                           |
| $V_O$ (Ampli.A)=0 V<br>$V_O$ (Ampli.B)=0 V   | —                         | 1.2              | 3     | —              | 1.2              | 3     |                              |
| $V_O$ (Ampli.A)=0 V<br>$V_O$ (Ampli.B)=7.5 V   | —                         | 5                | 8.5   | —              | 5                | 8.5   |                              |
| Input Offset Voltage<br>Temp.Drift, $\Delta V_{IO}/\Delta T$                                     | —                         | 6                | —     | —              | 8                | —     | $\mu\text{V}/^\circ\text{C}$ |
| Crosstalk $f=1\text{ kHz}$   | —                         | 120              | —     | —              | 120              | —     | dB                           |



## CA3260A, CA3260

### MAXIMUM RATINGS, Absolute-Maximum Values:

|   |   |
|---|---|
| DC SUPPLY VOLTAGE<br>(Between V <sup>+</sup> and V <sup>-</sup> Terminals)..... 16 V<br>DIFFERENTIAL-MODE<br>INPUT VOLTAGE..... ±8 V<br>COMMON-MODE DC<br>INPUT VOLTAGE..... (V <sup>+</sup> +8 V) to (V <sup>-</sup> -0.5 V)<br>INPUT-TERMINAL CURRENT ..... 1 mA<br>DEVICE DISSIPATION:<br>WITHOUT HEAT SINK —<br>UP TO 55°C..... 630 mW<br>ABOVE 55°C ... Derate linearly 6.67 mW/°C | WITH HEAT SINK —<br>UP TO 90°C..... 1 W<br>ABOVE 90°C ... Derate linearly 16.7 mW/°C<br>TEMPERATURE RANGE:<br>OPERATING (All Types) ..... -55 to +125°C<br>STORAGE (All Types) ..... -65 to +150°C<br>OUTPUT SHORT-CIRCUIT<br>DURATION* ..... INDEFINITE<br>LEAD TEMPERATURE<br>(DURING SOLDERING):<br>At distance 1/16 ± 1/32 in.<br>(1.59 ± 0.79 mm) from case<br>for 10 s max. .... +265°C |
|---|---|

\*Short circuit may be applied to ground or to either supply.

### TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

| CHARACTERISTIC  | TEST CONDITIONS  | CA3260A<br>(T, S, E) | CA3260<br>(T, S, E) | UNITS     |
|---|--|----------------------|---------------------|-----------|
| V <sup>+</sup> =+7.5 V, V <sup>-</sup> =-7.5 V, T <sub>A</sub> =25°C (Unless Otherwise Specified) |  |                      |                     |           |
| Input Resistance, R <sub>I</sub>  |  | 1.5                  | 1.5                 | TΩ        |
| Input Capacitance, C <sub>I</sub>   | f=1 MHz  | 4.3                  | 4.3                 | pF        |
| Unity Gain Crossover<br>Frequency, f <sub>T</sub>   |  | 4                    | 4                   | MHz       |
| Slew Rate, SR   |  | 10                   | 10                  | V/μs      |
| Transient Response:   | C <sub>L</sub> =25 pF<br>R <sub>L</sub> =2 kΩ<br>(Voltage<br>Follower) |                      |                     |           |
| Rise Time, t <sub>r</sub>   |  | 0.09                 | 0.09                | μs        |
| Overshoot   |  | 10                   | 10                  | %         |
| Settling Time (4 V <sub>p-p</sub><br>Input to < 0.1%)   |  | 1.8                  | 1.8                 | μs        |
| V <sup>+</sup> =5 V, V <sup>-</sup> =0 V, T <sub>A</sub> =25°C (Unless Otherwise Specified)       |  |                      |                     |           |
| Input Offset Voltage, V <sub>IO</sub>   |  | 2                    | 6                   | mV        |
| Input Offset Current, I <sub>IO</sub>   |  | 0.1                  | 0.1                 | pA        |
| Input Current, I <sub>I</sub>   |  | 2                    | 2                   | pA        |
| Common-Mode Rejection<br>Ratio, CMRR  |  | 70                   | 60                  | dB        |
| Large-Signal Voltage<br>Gain, A <sub>OL</sub>   | V <sub>O</sub> =4 V <sub>p-p</sub><br>R <sub>L</sub> =20 kΩ            | 100 k<br>100         | 100 k<br>100        | V/V<br>dB |
| Common-Mode Input<br>Voltage Range, V <sub>ICR</sub>  |  | 0 to 2.5             | 0 to 2.5            | V         |
| Supply Current, I <sup>+</sup>  | V <sub>O</sub> =5 V,<br>R <sub>L</sub> =∞                              | 1                    | 1                   | mA        |
|   | V <sub>O</sub> =2.5 V,<br>R <sub>L</sub> =∞                            | 1.2                  | 1.2                 |           |
| Power Supply Rejection<br>Ratio, ΔV <sub>IO</sub> /ΔV <sup>+</sup>                                |  | 200                  | 200                 | μV/V      |

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### Features

- Low Initial Input-Offset Voltage: 500 $\mu$ V Max. (CA3280A)
- Low Offset-Voltage Change vs  $I_{ABC}$ : <500 $\mu$ V Typ. for All Types
- Low Offset-Voltage Drift: 5 $\mu$ V/C Max. (CA3280A)
- Excellent Matching of the Two Amplifiers for All Characteristics
- Internal Current-Driven Linearizing Diodes Reduce the External Input Current to an Offset Component

### Applications

- Voltage-Controlled Amplifiers
- Voltage-Controlled Oscillators
- Multipliers
- Demodulators
- Sample and Hold
- Instrumentation Amplifiers
- Function Generators
- Triangle Wave-to-Sine Wave Converters
- Comparators
- Audio Preamplifiers

### Description

The CA3280 and CA3280A types consist of two variable operational amplifiers that are designed to substantially reduce the initial input offset voltage and the offset-voltage variation with respect to changes in programming current. This design results in reduced "AGC thump," an objectionable characteristic of many AGC systems. Inter-digitation, or crosscoupling, of critical portions of the circuit reduces the amplifier dependence upon thermal and processing variables.

The CA3280 has all the generic characteristics of an operational voltage amplifier except that the forward transfer characteristics is best described by transconductance rather than voltage gain, and the output is current, not voltage. The magnitude of the output current is equal to the product of transconductance and the input voltage. This type of operational transconductance amplifier was first introduced in 1969\*, and it has since gained wide acceptance as a gateable, gain-controlled building block for instrumentation and audio applications, such as linearization of transducer outputs, standardization of widely changing signals for data processing, multiplexing, instrumentation amplifiers operating from the nanopower range to high current and highspeed comparators.

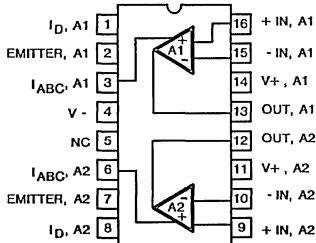
The operating-temperature ranges are -55 $^{\circ}$ C to +125 $^{\circ}$ C for the CA3280A, and 0 $^{\circ}$ C to +70 $^{\circ}$ C for the CA3280. The CA3280 and CA3280A are supplied in the 16 lead dual-in-line plastic package (E suffix), in the 16 lead dual-in-line frit-seal ceramic package (F suffix), and in chip form (H suffix).

For additional application information on this device and on OTAs in general, please refer to Application Notes: ICAN-6818, ICAN-6668, and ICAN-6077.

OPERATIONAL AMPLIFIERS

### Pinouts

E AND F SUFFIX  
TOP VIEW



### Functional Diagram

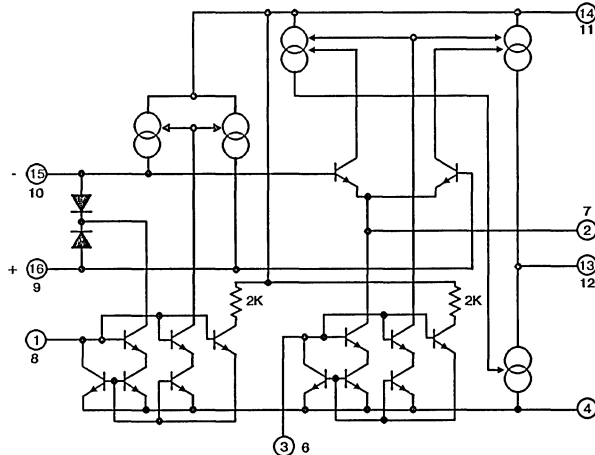


FIGURE 1. FUNCTIONAL DIAGRAM OF 1/2 CA3280

## CA3280A, CA3280

**MAXIMUM RATINGS, Absolute-Maximum Values:**

|   |                                |
|---|--------------------------------|
| DC SUPPLY VOLTAGE (BETWEEN V+ AND V- TERMINALS) | 36 V                           |
| DIFFERENTIAL INPUT VOLTAGE                      | ±5 V                           |
| DC INPUT VOLTAGE RANGE                          | V+ to V-                       |
| INPUT SIGNAL CURRENT AT $I_o = 0$               | 100 $\mu$ A                    |
| AMPLIFIER BIAS CURRENT                          | 10 mA                          |
| OUTPUT SHORT CIRCUIT DURATION*                  | Indefinite                     |
| LINEARIZING DIODE BIAS CURRENT, $I_b$           | 5 mA                           |
| PEAK INPUT CURRENT WITH LINEARIZING DIODE       | ± $I_b$                        |
| POWER DISSIPATION, $P_D$ :                      |                                |
| Either Amplifier                                | 600 mW                         |
| Total Package                                   | 750 mW                         |
| Above 55° C                                     | Derate linearly at 6.67 mW/° C |
| AMBIENT TEMPERATURE RANGE, $T_A$ :              |                                |
| Operating:                                      |                                |
| CA3280  | 0 to +70° C                    |
| CA3280A   | -55 to +125° C                 |
| Storage, All Types                              | -65 to +150° C                 |
| LEAD TEMPERATURE (DURING SOLDERING):            |                                |
| At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm)    |                                |
| from case for 10 sec. max                       | +265° C                        |

\*Short circuit may be applied to ground or to either supply.

## CA3280A, CA3280

**ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $V^\pm = 15\text{ V}$  (Unless Otherwise Stated)  
For Equipment Design**

| CHARACTERISTIC                                 | TEST CONDITIONS   | LIMITS  |                        |       |         |       |       | UNITS                        |                              |
|--|---|---|------------------------|-------|---------|-------|-------|------------------------------|------------------------------|
|  |   | CA3280  |                        |       | CA3280A |       |       |                              |                              |
|  |   | Min.  | Typ.                   | Max.  | Min.    | Typ.  | Max.  |                              |                              |
| Input Offset Voltage, $V_{IO}$                 | $I_{ABC}=1\text{ mA}$   | –   | –                      | 3     | –       | –     | 0.5   | mV                           |                              |
|  | $I_{ABC}=100\mu\text{A}$  | –   | 0.7                    | 3     | –       | 0.25  | 0.5   |                              |                              |
|  | $I_{ABC}=10\mu\text{A}$   | –   | –                      | 3     | –       | –     | 0.5   |                              |                              |
|  | $I_{ABC}=1\text{ mA to }10\mu\text{A}$<br>$T_A=\text{full temp. range}$ | –   | 0.8                    | 4     | –       | 0.8   | 1.5   |                              |                              |
| Input Offset Voltage Change, $ \Delta V_{IO} $ | $I_{ABC}=1\mu\text{A to }1\text{ mA}$                                   | –   | 0.5                    | 1     | –       | 0.5   | 1     | mV                           |                              |
|  | $I_{ABC}=100\mu\text{A}$<br>$T_A=\text{full temp. range}$               | –   | 5                      | –     | –       | 3     | 5     | $\mu\text{V}/^\circ\text{C}$ |                              |
| Amplifier Bias Voltage, $V_{ABC}$              | $I_{ABC}=100\mu\text{A}$  | –   | 1.2                    | –     | –       | 1.2   | –     | V                            |                              |
| Peak Output Voltage:                           | $I_{ABC}=500\mu\text{A}$  | Positive $V_{OM}^+$                                       | 12                     | 13.7  | –       | 12.5  | 13.7  | –                            | V                            |
|  |   | Negative $V_{OM}^-$                                       | 12                     | –14.3 | –       | –13.3 | –14.3 | –                            |                              |
|  | $I_{ABC}=5\mu\text{A}$  | Positive $V_{OM}^+$                                       | 12                     | 13.9  | –       | 12.5  | 13.9  | –                            |                              |
|  |   | Negative $V_{OM}^-$                                       | 12                     | –14.5 | –       | –13.5 | –14.5 | –                            |                              |
| Common-Mode Input Voltage Range, $V_{ICR}$     | $I_{ABC}=100\mu\text{A}$  | –13   | –                      | 13    | –13     | –     | 13    | V                            |                              |
| Noise Voltage, $e_N$ :                         | $I_{ABC}=500\mu\text{A}$  | 10 Hz   | –                      | 20    | –       | –     | 20    | –                            | $\text{nV}/\sqrt{\text{Hz}}$ |
|  |   | 1 kHz   | –                      | 8     | –       | –     | 8     | –                            | $\text{nV}/\sqrt{\text{Hz}}$ |
|  |   | 10 kHz  | –                      | 7     | –       | –     | 7     | –                            | $\text{nV}/\sqrt{\text{Hz}}$ |
| Input Offset Current, $I_{IO}$                 | $I_{ABC}=500\mu\text{A}$  | –   | 0.3                    | 0.7   | –       | 0.3   | 0.7   | $\mu\text{A}$                |                              |
|  | $I_{ABC}=500\mu\text{A}$  | –   | 1.8                    | 5     | –       | 1.8   | 5     | $\mu\text{A}$                |                              |
| Input Bias Current, $I_{IB}$                   | $I_{ABC}=500\mu\text{A}$<br>$T_A=\text{full temp. range}$               | –   | 3                      | 8     | –       | 3     | 8     |                              | $\mu\text{A}$                |
| Peak Output Current:                           | $I_{ABC}=500\mu\text{A}$  | Source $I_{OM}^+$   | 350                    | 410   | 650     | 350   | 410   | 650                          | $\mu\text{A}$                |
|  |   | Sink $I_{OM}^-$   | –350                   | –410  | –650    | –350  | –410  | –650                         |                              |
|  | $I_{ABC}=5\mu\text{A}$  | Source $I_{OM}^+$   | 3                      | 4.1   | 7       | 3     | 4.1   | 7                            |                              |
|  |   | Sink $I_{OM}^-$   | –3                     | –4.1  | –7      | –3    | –4.1  | –7                           |                              |
|  | Sink and Source, $I_{OM}^-$ , $I_{OM}^+$                                | $I_{ABC}=500\mu\text{A}$<br>$T_A=\text{full temp. range}$ | 350                    | 450   | 550     | 350   | 450   | 550                          |                              |
| Linearization Diodes:                          | $I_D = 100\mu\text{A}$  | Dynamic Impedance   | –                      | 700   | –       | –     | 700   | –                            | $\Omega$                     |
|  |   | Offset Current  | $I_D = 100\mu\text{A}$ | –     | 10      | –     | –     | 10                           | –                            |
|  | $I_D = 10\mu\text{A}$   |   | –                      | 0.5   | 1       | –     | 0.5   | 1                            |                              |

## CA3280A, CA3280

### ELECTRICAL CHARACTERISTICS (Cont'd)

| CHARACTERISTIC                                | TEST CONDITIONS  | LIMITS        |       |      |         |       |      | UNITS     |
|---|--|---------------|-------|------|---------|-------|------|-----------|
|   |  | CA3280        |       |      | CA3280A |       |      |           |
|   |  | Min.          | Typ.  | Max. | Min.    | Typ.  | Max. |           |
| Diode Network Supply Current                  | $I_{ABC}=100\mu A$                                       | 250           | 400   | 800  | 250     | 400   | 800  | $\mu A$   |
| Amplifier Supply Current (Per amplifier)      | $I_{ABC}=500\mu A$                                       | —             | 2     | 2.4  | —       | 2     | 2.4  | mA        |
| Amplifier Output Leakage Current, $I_{OL}$    | $I_{ABC}=0, V_O=0V$                                      | —             | 0.015 | 0.1  | —       | 0.015 | 0.1  | nA        |
|   | $I_{ABC}=0, V_O=30V$                                     | —             | 0.15  | 1    | —       | 0.15  | 1    |           |
| Common-Mode Rejection Ratio, CMRR             | $I_{ABC}=100\mu A$                                       | 80            | 100   | —    | 94      | 100   | —    | dB        |
| Power-Supply Rejection Ratio, PSRR            | $I_{ABC}=100\mu A$                                       | 86            | 105   | —    | 94      | 105   | —    | dB        |
| Open-Loop Voltage Gain, $A_{OL}$              | $I_{ABC}=100\mu A, R_L=\infty,$                          | 94            | 100   | —    | 94      | 100   | —    | dB        |
|   | $V_O=20 V_{p-p}$   | 50K           | 100K  | —    | 50K     | 100K  | —    |           |
| Forward Transconductance: Large Signal, $G_m$ | $I_{ABC}=50\mu A$  | —             | 0.8   | 1.2  | —       | 0.8   | 1.2  | mmho      |
|   | Small Signal, gm   | $I_{ABC}=1mA$ | —     | 16   | 22      | —     | 16   |           |
| Input Resistance, $R_I$                       | $I_{ABC}=10\mu A$  | 0.5           | —     | —    | 0.5     | —     | —    | $M\Omega$ |
| Channel Separation                            | $f=1 kHz$  | —             | 94    | —    | —       | 94    | —    | dB        |
| Open-Loop Total Harmonic Distortion           | $f=1 kHz, I_{ABC}=1.5 mA, R_L=15k\Omega, V_O=20 V_{p-p}$ | —             | 0.4   | —    | —       | 0.4   | —    | %         |
| Bandwidth                                     | $I_{ABC}=1mA, R_L=100\Omega$                             | —             | 9     | —    | —       | 9     | —    | MHz       |
| Slew Rate, SR: Open Loop                      | $I_{ABC}=1mA$  | —             | 125   | —    | —       | 125   | —    | $V/\mu s$ |
| Capacitance: Input, $C_I$                     | $I_{ABC}=100\mu A$                                       | —             | 4.5   | —    | —       | 4.5   | —    | pF        |
|   |  | Output, $C_O$ | —     | 7.5  | —       | —     | 7.5  |           |
| Output Resistance, $R_O$                      | $I_{ABC}=100\mu A$                                       | —             | 63    | —    | —       | 63    | —    | $M\Omega$ |

Figs. 2 and 3 show the equivalent circuits for the current source and linearization diodes in the CA3280. The current through the linearization network is approximately equal to the programming current. There are several advantages to driving these diodes with a current source. First, only the offset current from the biasing network flows through the input resistor. Second, another input is provided to extend the gain control dynamic range. And third, the input is truly differential and can accept signals within the common-mode range of the CA3280.

The structure of the variable operational amplifier eliminates the need for matched resistor networks in differential to single-ended converters, as shown in Fig. 4. A matched resistor network requires ratio matching of 0.01% or trimming for 80 dB of common-mode rejection. The CA3280, with its excellent common-mode rejection ratio, is capable of converting a small ( $\pm 25 mV$ ) differential input signal to a single-ended output without the need for a matched resistor network.

# CA3280A, CA3280

Fig. 5 shows the CA3280 in a typical gain-control application. The input-signal range as a function of distortion at various levels of linearization diode current is shown in Fig. 6. This curve shows only the AGC capability of the diode network, but gain control can also be performed with the amplifier bias current ( $I_{ABC}$ ). With no diode bias current, the gain is merely  $gmR_L$ . For example, with an  $I_{ABC}$  of 1 mA, the  $gm$  is approximately 16 mmhos. With the CA3280 operating into a 5 k $\Omega$  resistor, the gain is 80.

The need for external buffers can be eliminated by the use of low-value load resistors, but the resulting increase in the required amplifier bias current reduces the input impedance of the CA3280. The linearization diode impedance also decreases as the diode bias current increases, which further loads the input. The diodes, in addition to acting as a linearization network, also operate as an additional attenuation system to accommodate input signals in the volt range when they are applied through appropriate input resistors.

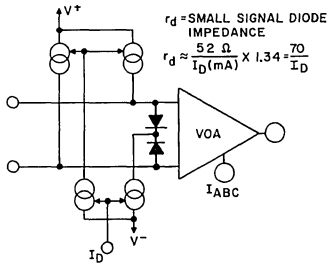


Fig. 2 - VOA showing linearization diodes and current drive.

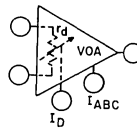


Fig. 3 - Block diagram of linearized VOA.

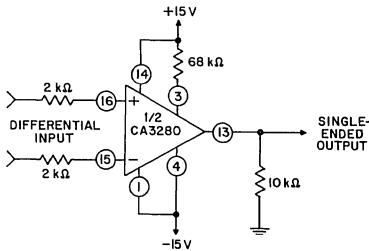


Fig. 4 - Differential to single-ended converter.

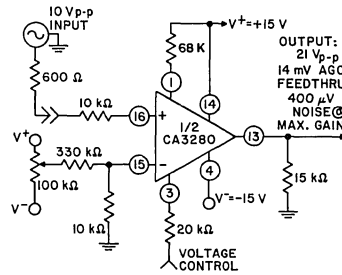


Fig. 5 - Typical gain control circuit.

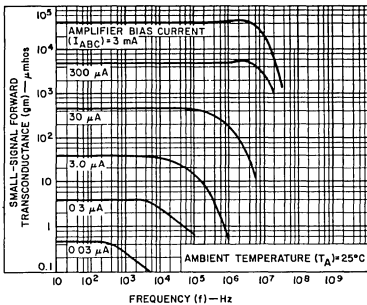


Fig. 6 - Amplifier gain as a function of frequency.

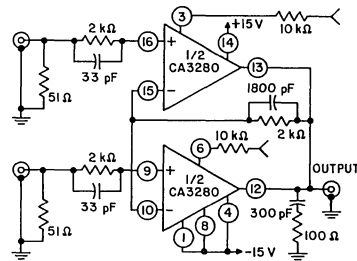
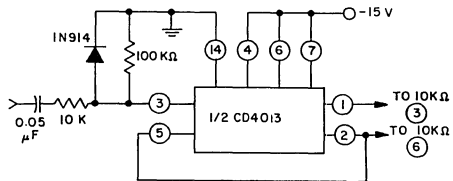
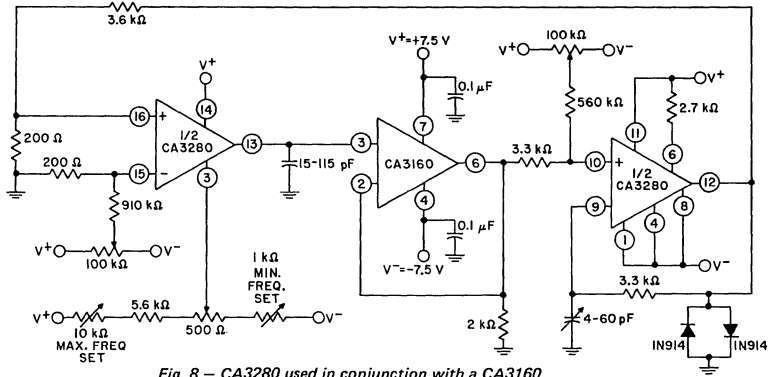


Fig. 7 - Two-channel linear multiplexer.



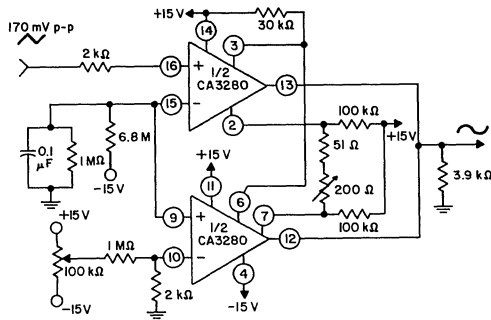
## CA3280A, CA3280



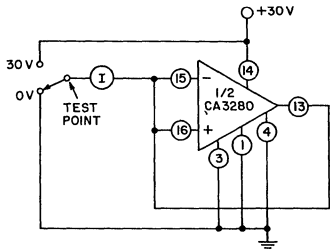
**Fig. 8** — CA3280 used in conjunction with a CA3160 to provide a function generator with a tunable range of from 2 Hz to 1 MHz.

Fig. 9 shows a triangle wave-to-sine wave converter using the CA3280. Two 100KΩ resistors are connected between the differential amplifier emitters and V+ to reduce the cur-

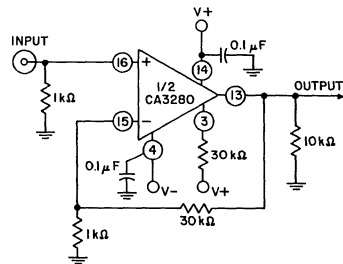
rent flow through the differential amplifier. This allows the amplifier to fully cut off during peak input signal excursions. THD is approximately 0.37% for this circuit.



**Fig. 9** — Triangle wave-to-sine wave converter.

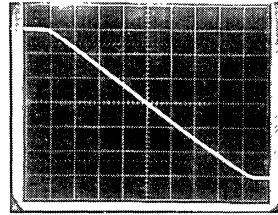
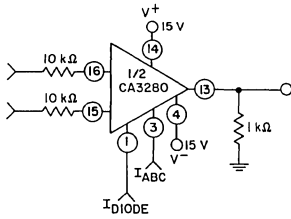


**Fig. 10** — Leakage current test circuit.



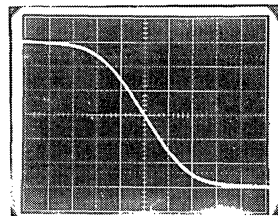
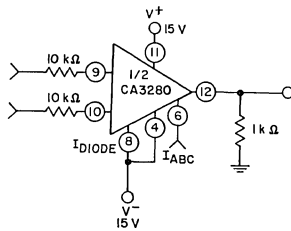
**Fig. 11** — Channel separation test circuit.

# CA3280A, CA3280



$I_{abc} = 650 \mu\text{A}$   
 $I_D = 200 \mu\text{A}$   
 VERT =  $200 \mu\text{A}/\text{DIV}$   
 HOR =  $1 \text{ V}/\text{DIV}$

a) With diode programming terminal active



$I_{abc} = 650 \mu\text{A}$   
 $I_D = 0$   
 VERT =  $200 \mu\text{A}/\text{DIV}$   
 HOR =  $25 \text{ mV}/\text{DIV}$

b) With diode programming terminal cut-off

Fig. 12 - CA3280 transfer characteristics.

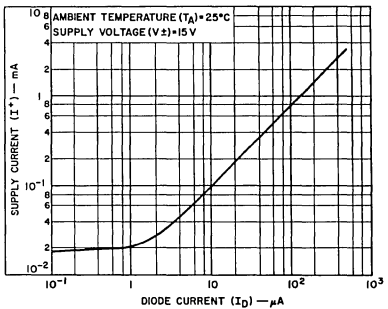


Fig. 13 - Supply current as a function of diode current.

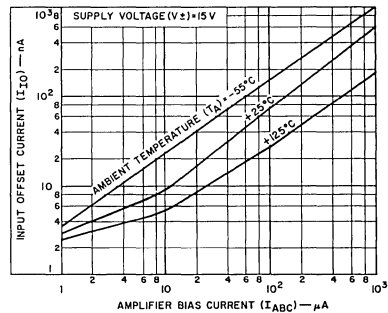


Fig. 14 - Input offset current as a function of amplifier bias current.

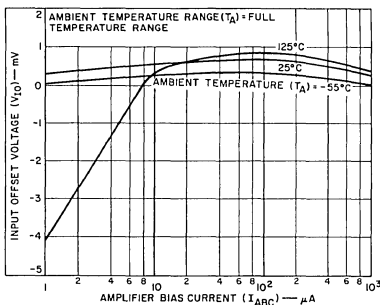


Fig. 15 - Input offset voltage as a function of amplifier bias current.

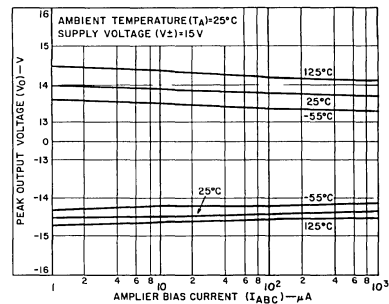


Fig. 16 - Peak output voltage as a function of amplifier bias current.



# CA3280A, CA3280

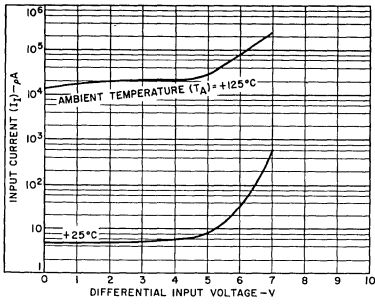


Fig. 17 – Input current as a function of input differential voltage.

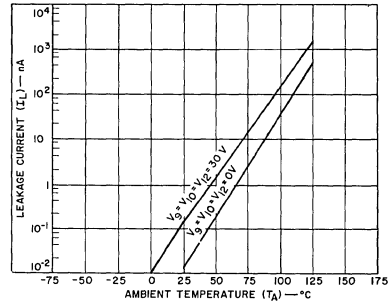


Fig. 18 – Leakage current as a function of temperature.

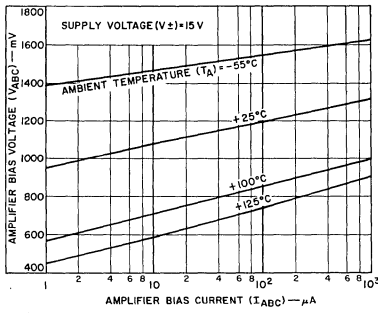


Fig. 19 – Amplifier bias voltage as a function of amplifier bias current.

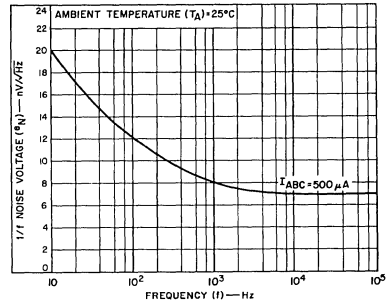


Fig. 20 –  $1/f$  noise as a function of frequency.

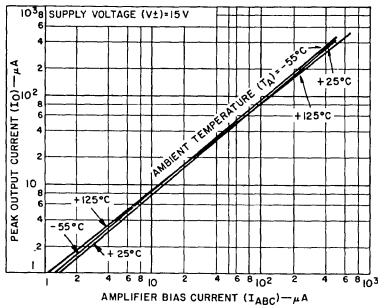


Fig. 21 – Peak output current as a function of amplifier bias current.

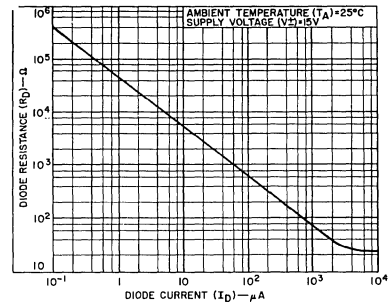


Fig. 22 – Diode resistance as a function of diode current.

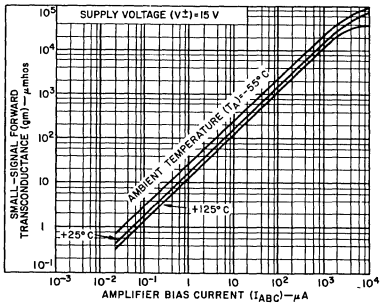


Fig. 23 – Amplifier gain as a function of amplifier bias current.

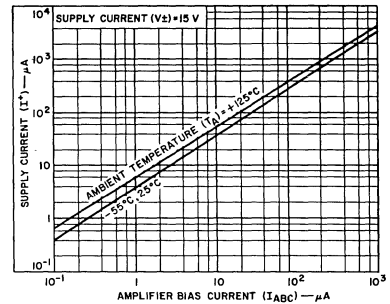


Fig. 24 – Supply current as a function of amplifier bias current.

# CA3280A, CA3280

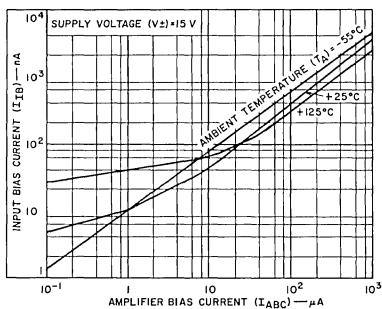

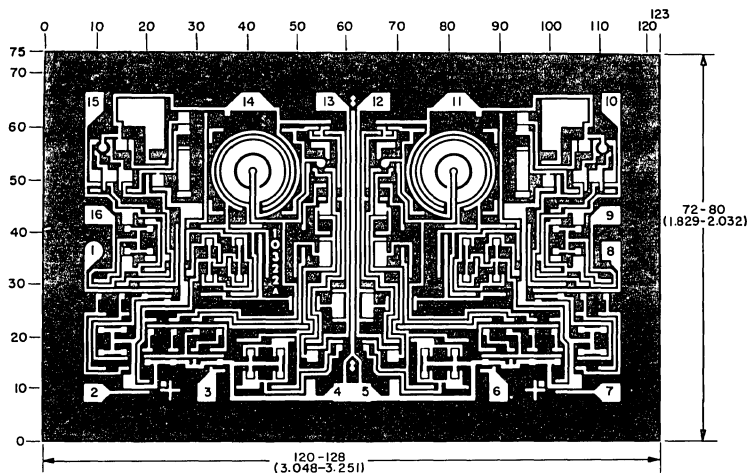


Fig. 25 – Input bias current as a function of amplifier bias current.

  
 OPERATIONAL AMPLIFIERS



Dimensions and pad layout for CA3280H.

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are  $57^\circ$  instead of  $90^\circ$  with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

August 1991

### Features

- 2V Supply at 300 $\mu$ A Supply Current
- 1pA (Typ.) Input Current (Essentially Constant to 85 $^{\circ}$ C)
- Rail-to-Rail Output Swing (Drive  $\pm$ 2mA into 1k $\Omega$  Load)
- Pin Compatible with 741 Operational Amplifiers

### Applications

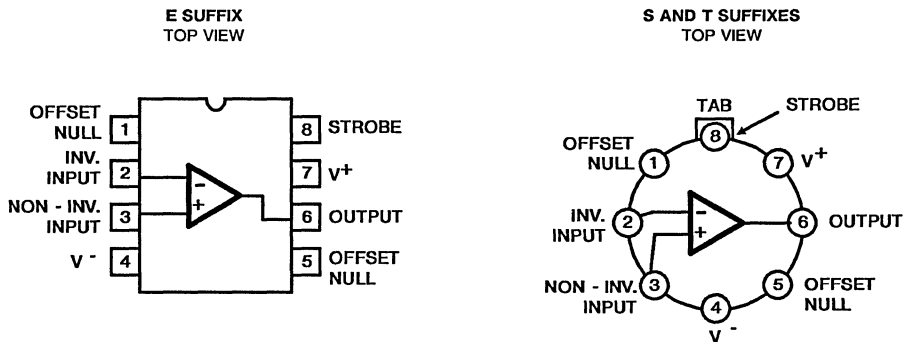
- pH Probe Amplifiers
- Picoammeters
- Electrometer (High Z) Instruments
- Portable Equipment
- Inaccessible Field Equipment
- Battery-Dependent Equipment (Medical and Military)

### Description

The CA3420A and CA3420\* are integrated-circuit operational amplifiers that combine PMOS transistors and bipolar transistors on a single monolithic chip. The CA3420A and CA3420 BIMOS operational amplifiers feature gate-protected PMOS transistors in the input circuit to provide very high input impedance, very low input currents (less than 1pA). The internal bootstrapping network features a unique guardbanding technique for reducing the doubling of leakage current for every 10 $^{\circ}$ C increase in temperature. The CA3420 series operates at total supply voltages from 2 to 20 volts either single or dual supply. These operational amplifiers are internally phase compensated to achieve stable operation in the unity gain follower configuration. Additionally, they have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS in the input stage results in common-mode input voltage capability down to 0.45 volt below the negative supply terminal, an important attribute for single-supply application. The output stage uses a feedback OTA type amplifier that can swing essentially from rail-to-rail. The output driving current of 1.5mA (min) is provided by using non-linear current mirrors.

The CA3420 series has the same 8 lead pin-out used for the industry standard 741. They are supplied in the standard 8 lead TO-5 style package (S suffix, and T suffix); in the standard 8 lead dual-in-line plastic package (Minidip - E suffix), and are also available in chip form (H suffix).

### Pinouts



\*Formerly Development Type No. TA10841

## CA3420A, CA3420

### MAXIMUM RATINGS, Absolute-Maximum Values ( $T_C=25^\circ\text{C}$ ):

|  |  |
|--|--|
| DC Supply Voltage<br>(Between $V^+$ and $V^-$ Terminals) ..... | 22 V   |
| Differential-Mode<br>Input Voltage .....                       | $\pm 15$ V                                     |
| Common-Mode DC<br>Input Voltage .....                          | $(V^+ + 8\text{ V})$ to $(V^- - 0.5\text{ V})$ |
| Input-Terminal Current .....                                   | 1 mA   |
| Device Dissipation:  |  |
| Without Heat Sink —  |  |
| Up to $55^\circ\text{C}$ .....                                 | 630 mW   |
| Above $55^\circ\text{C}$ .....                                 | Derate linearly 6.67 mW/ $^\circ\text{C}$      |
| With Heat Sink -   |  |
| Up to $110^\circ\text{C}$ .....                                | 630 mW   |
| Above $110^\circ\text{C}$ .....                                | Derate linearly 16.7 mW/ $^\circ\text{C}$      |

|   |                               |
|---|-------------------------------|
| Temperature Range:  |                               |
| Operating (All Types) .....   | $-55$ to $+125^\circ\text{C}$ |
| Storage (All Types) .....   | $-65$ to $+150^\circ\text{C}$ |
| Output Short-Circuit<br>Duration* .....                             | Indefinite                    |
| Lead Temperature<br>(During Soldering):                             |                               |
| At Distance $1/16 \pm 1/32$ Inch<br>( $1.59 \pm 0.79$ mm) from case |                               |
| For 10 seconds max. ....  | $+265^\circ\text{C}$          |

\*Short circuit may be applied to ground or to either supply.

### TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

| Characteristic                                | Test Conditions  |                     | CA3420A<br>(T,S,E) | CA3420<br>(T,S,E) | Units                        |
|---|--|---------------------|--------------------|-------------------|------------------------------|
|   | $V^+ = +10\text{V}; V^- = -10\text{V}$<br>$T_A = 25^\circ\text{C}$ |                     |                    |                   |                              |
| Input Resistance $R_I$                        |  |                     | 150                | 150               | $\text{T}\Omega$             |
| Input Capacitance $C_I$                       |  |                     | 4.9                | 4.9               | pF                           |
| Output Resistance $R_O$                       |  |                     | 300                | 300               | $\Omega$                     |
| Equivalent Input<br>Noise Voltage $e_n$       | $f = 1\text{ KHz}$   | $R_S = 100\ \Omega$ | 62                 | 62                | $\text{nV}/\sqrt{\text{Hz}}$ |
|   | $f = 10\text{ KHz}$  |                     | 38                 | 38                |                              |
| Short-Circuit Current Source<br>Source IOM+   |  |                     | 2.6                | 2.6               | mA                           |
| To Opposite Supply<br>Sink IOM-               |  |                     | 2.4                | 2.4               | mA                           |
| Gain-Bandwidth Product $f_T$                  |  |                     | 0.5                | 0.5               | MHz                          |
| Slew Rate SR                                  |  |                     | 0.5                | 0.5               | $\text{V}/\mu\text{s}$       |
| Transient Response                            |  |                     |                    |                   |                              |
| Rise Time $t_r$                               | $R_L = 2\text{ K}\Omega$<br>$C_L = 100\text{ pF}$                  |                     | 0.7                | 0.7               | $\mu\text{s}$                |
| Overshoot                                     |  |                     | 15                 | 15                | %                            |
| Current from Terminal 8<br>To $V^-$ $I_{g^+}$ |  |                     | 20                 | 20                | $\mu\text{A}$                |
| Current from Terminal 8<br>To $V^+$ $I_{g^-}$ |  |                     | 2                  | 2                 | mA                           |

## CA3420A, CA3420

### ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At  $V_+ = 1V$ ,  $V_- = -1V$ ,  $T_A = 25^\circ C$  unless otherwise specified

| Characteristic   | Limits  |       |      |        |       |      | Units            |
|--|---------|-------|------|--------|-------|------|------------------|
|  | CA3420A |       |      | CA3420 |       |      |                  |
|  | Min     | Typ   | Max  | Min    | Typ   | Max  |                  |
| Input Offset Voltage $ V_{IO} $                              | —       | 2     | 5    | —      | 5     | 10   | mV               |
| Input Offset Current $ I_{IO} ^*$                            | —       | 0.01  | 4    | —      | 0.01  | 4    | pA               |
| Input Current $ I_I ^*$                                      | —       | 0.02  | 5    | —      | 1     | 5    | pA               |
| Large-Signal Voltage Gain                                    | 20K     | 100K  | —    | 10K    | 100K  | —    | V/V              |
| AOL ( $R_L = 10\text{ K}\Omega$ )                            | 86      | 100   | —    | 80     | 100   | —    | dB               |
| Common-Mode  | —       | 560   | 1000 | —      | 560   | 1800 | $\mu V/V$        |
| Rejection Ratio CMRR   | 60      | 65    | —    | 55     | 65    | —    | dB               |
| Common-Mode Input VICR +                                     | +0.2    | +0.5  | —    | +0.2   | +0.5  | —    | V                |
| Voltage Range VICR -   | -1      | -1.3  | —    | —      | -1.3  | —    | V                |
| Power Supply Rejection                                       | —       | 32    | 320  | —      | 100   | 1000 | $\mu V/V$        |
| Ratio PSRR $\Delta V_{IO}/\Delta V$                          | 70      | 90    | —    | 60     | 80    | —    | dB               |
| Max Output Voltage VOM +                                     | +0.90   | +0.95 | —    | +0.90  | +0.95 | —    | V                |
| $R_L = 00$ VOM -   | -0.85   | -0.91 | —    | -0.85  | -0.91 | —    | V                |
| Supply Current $I_+$   | —       | 350   | 650  | —      | 350   | 650  | $\mu A$          |
| Device Dissipation $P_D$                                     | —       | 0.7   | 1.1  | —      | 0.7   | 1.1  | mW               |
| Input Offset Voltage<br>Temp. Drift $\Delta V_{IO}/\Delta T$ | —       | 4     | —    | —      | 4     | —    | $\mu V/^\circ C$ |

### ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At  $V_+ = 10V$ ,  $V_- = -10V$ ,  $T_A = 25^\circ C$  unless otherwise specified

| Characteristic   | Limits  |       |      |        |       |      | Units            |
|--|---------|-------|------|--------|-------|------|------------------|
|  | CA3420A |       |      | CA3420 |       |      |                  |
|  | Min     | Typ   | Max  | Min    | Typ   | Max  |                  |
| Input Offset Voltage $ V_{IO} $                              | —       | 2     | 5    | —      | 5     | 10   | mV               |
| Input Offset Current $ I_{IO} ^*$                            | —       | 0.03  | 4    | —      | 0.03  | 4    | pA               |
| Input Current $ I_I ^*$                                      | —       | 0.05  | 5    | —      | 0.05  | 5    | pA               |
| Large-Signal Voltage Gain                                    | 20K     | 100K  | —    | 10K    | 100K  | —    | V/V              |
| AOL ( $R_L = 10\text{ K}\Omega$ )                            | 86      | 100   | —    | 80     | 100   | —    | dB               |
| Common-Mode  | —       | 100   | 320  | —      | 100   | 320  | $\mu V/V$        |
| Rejection Ratio CMRR   | 70      | 80    | —    | 70     | 80    | —    | dB               |
| Common-Mode Input VICR +                                     | +9.0    | +9.3  | —    | +8.5   | +9.3  | —    | V                |
| Voltage Range VICR -   | -10     | -10.3 | —    | -10    | -10.3 | —    | V                |
| Power Supply Rejection                                       | —       | 32    | 320  | —      | 32    | 320  | $\mu V/V$        |
| Ratio PSRR $\Delta V_{IO}/\Delta V$                          | 70      | 90    | —    | 70     | 90    | —    | dB               |
| Max Output Voltage VOM +                                     | +9.7    | +9.9  | —    | +9.7   | +9.9  | —    | V                |
| $R_L = 00$ VOM -   | -9.7    | -9.85 | —    | -9.7   | -9.85 | —    | V                |
| Supply Current $I_+$   | —       | 450   | 1000 | —      | 450   | 1000 | $\mu A$          |
| Device Dissipation $P_D$                                     | —       | 9     | 14   | —      | 9     | 14   | mW               |
| Input Offset Voltage<br>Temp. Drift $\Delta V_{IO}/\Delta T$ | —       | 4     | —    | —      | 4     | —    | $\mu V/^\circ C$ |

\* The maximum limit represents the levels obtainable on high speed automatic test equipment. Typical values are obtained under laboratory conditions.

# CA3420A, CA3420

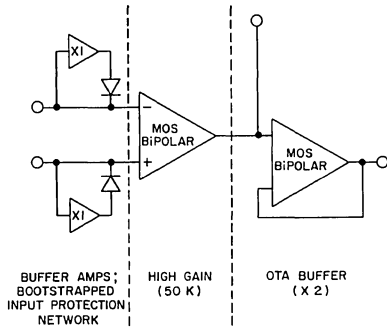


Fig. 1 - Functional diagram for CA3420.

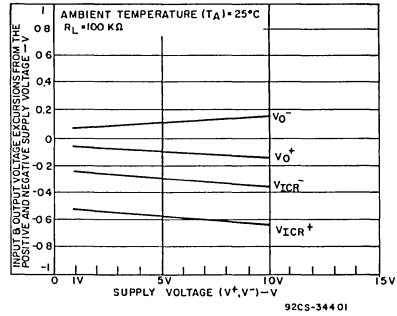


Fig. 2 - Output-voltage-swing and common-mode input-voltage range versus supply voltage.

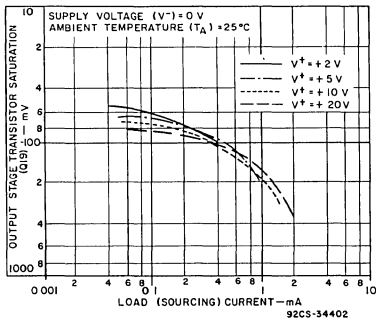


Fig. 3 - Output voltage versus load sourcing current.

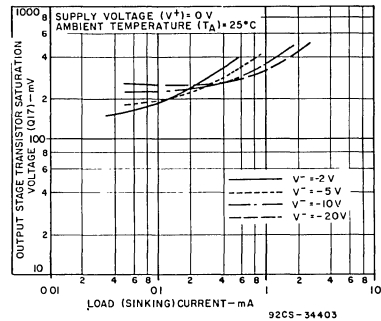


Fig. 4 - Output voltage versus load sinking current.

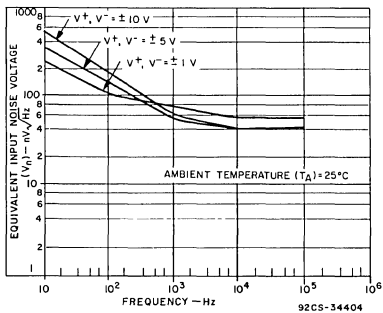


Fig. 5 - Input noise voltage versus frequency.

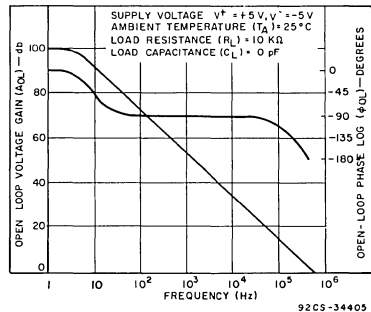


Fig. 6 - Open-loop gain and phase-shift response.

# CA3420A, CA3420

## Application Circuits

### Picoameter Circuit

The exceptionally low input current (typically 0.2 pA) makes the CA3420 highly suited for use in a picoameter circuit. With only a single 10K megohm resistor, this circuit covers the range from  $\pm 1.5$  pA. Higher current ranges are possible with suitable switching techniques and current scaling resistors. Input transient protection is provided by the 1-megohm resistor in series with the input. Higher current ranges require that this resistor be reduced. The 10-megohm resistor connected to pin 2 of the CA3420 decouples the potentially high input capacitance often associated with lower current circuits and reduces the tendency for the circuit to oscillate under these conditions.

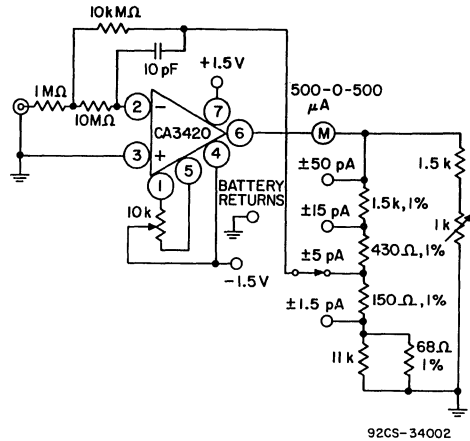


Fig. 7 - Picoameter circuit.

### High-Input-Resistance Voltmeter

Advantage is taken of the high input impedance of the CA3420 in a high-input-resistance dc voltmeter. Only two 1.5 V "AA" type penlite batteries power this exceedingly high-input resistance ( $>1,000,000$ -megohms) dc voltmeter. Full-scale deflection is  $\pm 500$  mV,  $\pm 150$  mV, and  $\pm 15$  mV. Higher voltage ranges are easily added with external input voltage attenuator networks.

The meter is placed in series with the gain network, thus eliminating the meter temperature coefficient error term.

Supply current in the standby position with the meter undeflected is  $300 \mu\text{A}$ . At full-scale deflection this current rises to  $800 \mu\text{A}$ . Carbon-zinc battery life should be in excess of 1,000 hours.

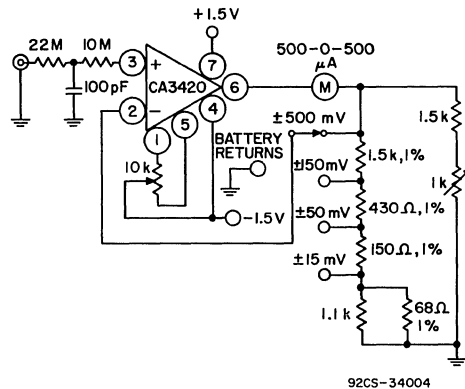


Fig. 8 - High input resistance voltmeter.

August 1991

## Nanopower BiMOS Operational Amp

### Features

- Standby Power at  $V+ = 5V$  ..... 300nW (Typ)
- Supply Current, BW, Slew Rate Programmable Using External Resistor
- Input Current ..... 10pA (Typ)
- 5V to 15V Supply
- Output Drives Typical Bipolar-Type Loads
- Low Cost 8-Lead Mini-DIP, TO-5

### Description

The CA3440A and CA3440\* are integrated circuit operational amplifiers that combine the advantages of MOS and bipolar transistors on a single monolithic chip.

The CA3440A and CA3440 BiMOS op amps feature gate-protected PMOS transistors in the input circuit to provide very high input impedance and very low input current (10pA). These devices operate at total supply voltage from 5V to 15V and can be operated over the temperature range from  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . Their virtues are programmability and very low standby power consumption (300nW). These operational amplifiers are internally phase compensated to achieve stable operation in the unity gain follower configuration. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS in the input stage results in common-mode input voltage capability down to 0.5V below the negative supply terminals, an important attribute for single supply applications. The output stage uses MOS complementary source follower form which permits moderate load driving capability ( $10\text{K}\Omega$ ) at very low total standby currents (50nA).

The CA3440A and CA3440 have the same 8-lead terminal pin-out used for "741" and other industry standard op amps with two exceptions: terminals one and five must be connected to the negative supply or to a potentiometer if nulling is required. Terminal 8 must be programmed through an external resistor returned to the negative supply.

These devices are supplied in either the standard 8-lead TO-5 style package (T suffix), 8-lead dual-in-line formed-lead TO-5 style "DIL-CAN" package (S suffix), or in the 8-lead dual-in-line plastic package "Mini-DIP" (E suffix).

\*Formerly Dev. Type No. TA10590.

### Pinouts

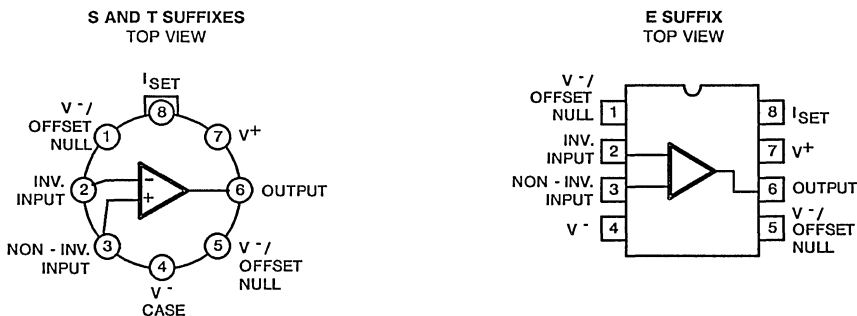


FIGURE 1.



# CA3440A, CA3440

## MAXIMUM RATINGS, Absolute-Maximum Values:

|   |                                    |
|---|------------------------------------|
| DC SUPPLY VOLTAGE<br>(BETWEEN $V^+$ AND $V^-$ TERMINALS) .....                          | 25 V                               |
| DIFFERENTIAL-MODE INPUT VOLTAGE .....   | $\pm 9$ V                          |
| COMMON-MODE DC INPUT VOLTAGE .....  | ( $V^+ + 8$ V) to ( $V^- - 0.5$ V) |
| INPUT-TERMINAL CURRENT .....  | 1 mA                               |
| DEVICE DISSIPATION:   |                                    |
| WITHOUT HEAT SINK —   |                                    |
| UP TO 55°C .....  | 630 mW                             |
| ABOVE 55°C .....  | Derate linearly 6.67 mW/°C         |
| WITH HEAT SINK —  |                                    |
| AT 125°C .....  | 418 mW                             |
| BELOW 125°C .....   | Derate linearly 16.7 mW/°C         |
| TEMPERATURE RANGE:  |                                    |
| OPERATING .....   | -55 to +125°C                      |
| STORAGE .....   | -65 to +150°C                      |
| OUTPUT SHORT-CIRCUIT DURATION .....   | INDEFINITE                         |
| LEAD TEMPERATURE (DURING SOLDERING):  |                                    |
| AT DISTANCE 1/16 $\pm$ 1/32 IN. (1.59 $\pm$ 0.79 MM) FROM CASE FOR 10 SECONDS MAX. .... | +265°C                             |

## TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

| CHARACTERISTIC  | TEST CONDITIONS<br>$V^+ = +5$ V; $V^- = -5$ V<br>$R_{SET} = 10$ M $\Omega$ ; $T_A = 25^\circ$ C |                       | CA3440A | CA3440 | UNITS                  |
|---|---|-----------------------|---------|--------|------------------------|
|   | Input Resistance, $R_I$   |                       |         | 2      |                        |
| Input Capacitance, $C_T$  |   |                       | 3.5     | 3.5    | pF                     |
| Output Resistance, $R_O$  |   |                       | 450     | 450    | $\Omega$               |
| Equivalent Input Noise Voltage, $e_n$   | $f = 1$ kHz   | $R_S = 100$ $\Omega$  | 110     | 110    | nV/ $\sqrt{\text{Hz}}$ |
|   | $f = 10$ kHz  |                       | 110     | 110    |                        |
| Short-Circuit Current<br>Source IOM $^+$<br>To Opposite Supply<br>Sink IOM $^-$ |   |                       | 15      | 15     | mA                     |
|   |   |                       | 4.5     | 4.5    |                        |
| Gain-Bandwidth Product, $f_T$   |   |                       | 63      | 63     | kHz                    |
| Slew Rate, SR   |   |                       | 0.03    | 0.03   | V/ $\mu$ s             |
| Transient Response  |   |                       |         |        |                        |
|   | Rise Time, $t_r$  | $R_L = 10$ k $\Omega$ | 5.6     | 5.6    | $\mu$ s                |
| Overshoot   | $C_L = 100$ pF  |                       | 10      | 10     | %                      |

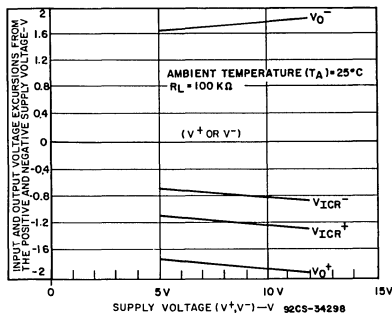


Fig. 1 - Output-voltage-swing and common-mode input-voltage range versus supply voltage.

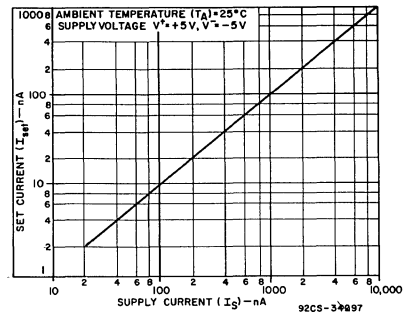


Fig. 2 - Set current versus supply current.

# CA3440A, CA3440

## ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At  $V^+ = +5\text{ V}$ ,  $V^- = -5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  Unless Otherwise Specified,  $R_{SET} = 10\text{ M}\Omega$

| CHARACTERISTIC   | LIMITS     |      |      |        |      |      | UNITS                        |
|--|------------|------|------|--------|------|------|------------------------------|
|  | CA3440A    |      |      | CA3440 |      |      |                              |
|  | Min.       | Typ. | Max. | Min.   | Typ. | Max. |                              |
| Input Offset Voltage, $ V_{IO} $                                 | —          | 2    | 5    | —      | 5    | 10   | mV                           |
| Input Offset Current, $ I_{IO} $                                 | —          | 2.5  | 20   | —      | 2.5  | 30   | pA                           |
| Input Current, $ I_I $   | —          | 10   | 40   | —      | 10   | 50   |                              |
| Large-Signal Voltage Gain, AOL<br>( $R_L = 10\text{ K}\Omega$ )  | 10K        | 100K | —    | 10K    | 100K | —    | V/V                          |
|  | 80         | 100  | —    | 80     | 100  | —    | dB                           |
| Common-Mode  | —          | 100  | 320  | —      | 100  | 320  | $\mu\text{V/V}$              |
| Rejection Ratio, CMRR  | 70         | 80   | —    | 70     | 80   | —    | dB                           |
| Common-Mode Input Voltage Range, $V_{ICR}^+$                     | +3.5       | +3.7 | —    | +3.5   | +3.7 | —    | V                            |
| $V_{ICR}^-$  | -5.0       | -5.3 | —    | -5.0   | -5.3 | —    |                              |
| Power Supply Rejection Ratio,<br>$\Delta V_{IO}/\Delta V$        | —          | 32   | 320  | —      | 32   | 320  | $\mu\text{V/V}$              |
|  | PSRR       | 70   | 90   | —      | 70   | 90   | dB                           |
| Maximum Output Voltage,<br>$V_{OM}^+$                            | +3         | +3.2 | —    | +3     | +3.2 | —    | V                            |
|  | $V_{OM}^-$ | -3   | -3.2 | —      | -3   | -3.2 |                              |
| Supply Current, $I^+$  | —          | 10   | 17   | —      | 10   | 17   | $\mu\text{A}$                |
| Device Dissipation, $P_D$  | —          | 100  | 170  | —      | 100  | 170  | $\mu\text{W}$                |
| Input Offset Voltage Temperature Drift, $\Delta V_{IO}/\Delta T$ | —          | 4    | —    | —      | 4    | —    | $\mu\text{V}/^\circ\text{C}$ |

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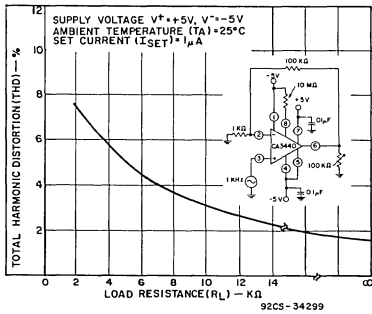


Fig. 3 - Total harmonic distortion percentage versus load resistance.

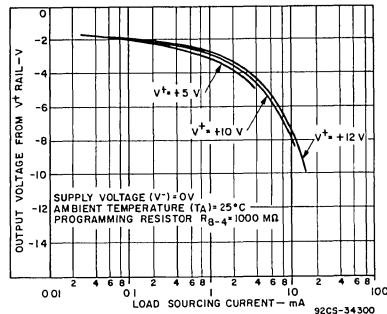


Fig. 4 - Output voltage versus sourcing load current.

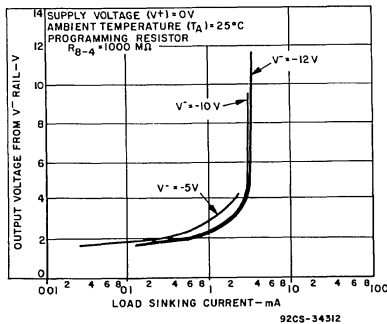


Fig. 5 - Output voltage versus sinking load current.

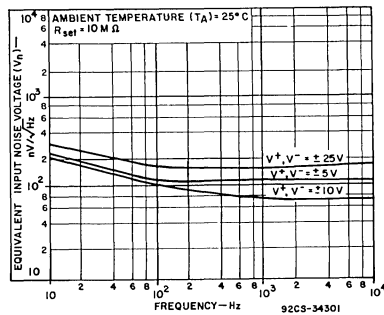


Fig. 6 - Input noise voltage versus frequency.

# CA3440A, CA3440

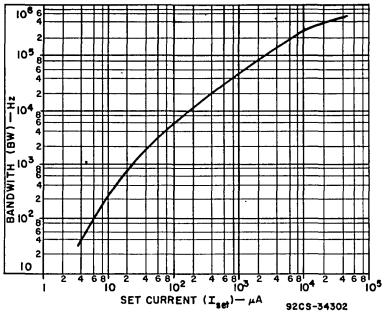


Fig. 7 - Bandwidth versus set current.

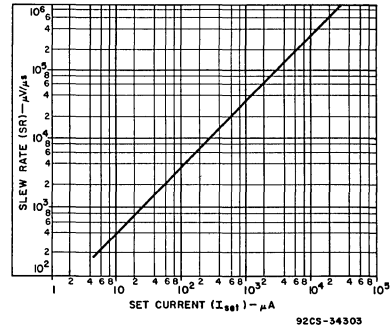


Fig. 8 - Slew rate versus set current.

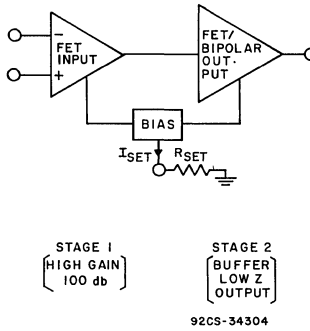


Fig. 9 - Nanopower op amp (supply current programmable using  $R_{SET}$ ) 1-pA typical input bias current, 4.0 to 15-volt supply.

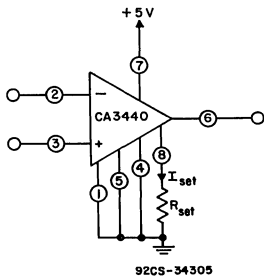


Fig. 10 - Nanopower op amp (usable standby power versus programming resistor  $R_{SET}$ ).

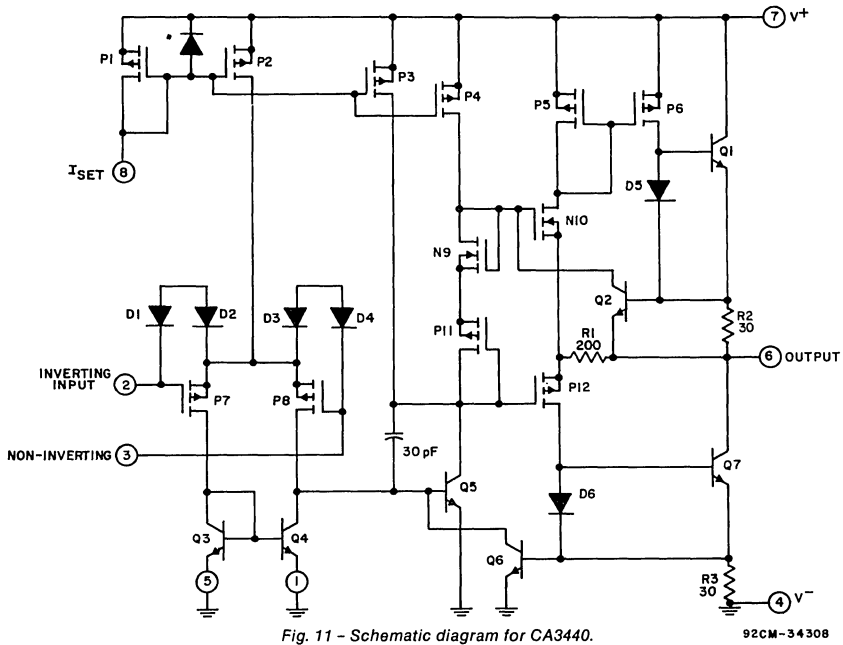
As  $R_{SET}$  is increased,  $I_{SET}$  and the standby power decrease while the BW/SR also decreases.

Operating at a +5 V single supply, the CA3440 exhibits the following characteristics:

| $R_{SET}$       | Standby Power | BW      | SR                 |
|-----------------|---------------|---------|--------------------|
| 1 M $\Omega$    | 250 $\mu$ W   | 164 kHz | 0.17 V/ $\mu$ s    |
| 10 M $\Omega$   | 25 $\mu$ W    | 27 kHz  | 0.017 V/ $\mu$ s   |
| 100 M $\Omega$  | 2.5 $\mu$ W   | 2.6 kHz | .0017 V/ $\mu$ s   |
| 1000 M $\Omega$ | 250 nW        | 78 Hz   | 0.00017 V/ $\mu$ s |

The CA3440 is pin-compatible with the 741 except that pins 1 and 5 (typical negative nulling pins) must be connected either directly to pin 4 or to a negative nulling potentiometer. In addition, pin 8, the  $I_{SET}$  terminal, must be returned to either ground or -V via  $R_{SET}$ .

# CA3440A, CA3440



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## APPLICATIONS CIRCUITS

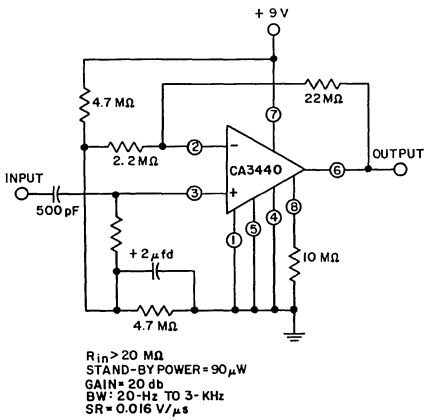


Fig. 12 - High-input impedance amplifier.

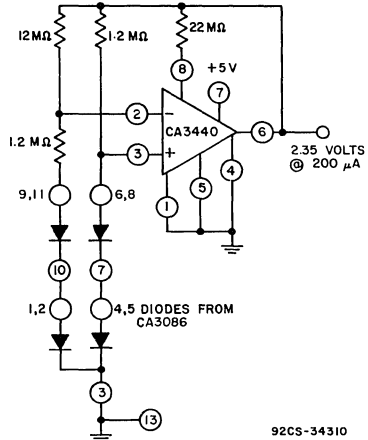


Fig. 13 - Micropower bandgap reference.

## Video Line Driver, High-Speed Operational Amplifier

August 1991

### Features

- High Open Loop Gain at Video Frequencies
  - $A_{OL}$  ..... > 40 dB at  $f = 5\text{MHz}$
- Power Bandwidth of 10MHz;  $A_{Closed\ Loop} = 5$ ;  $V_O = \pm 3.5V$
- Slew Rate at Full Load ..... 330V/ $\mu\text{sec}$  ( $A_V \geq 10$ )
- $f_T = 220\text{MHz}$ ;  $C_C = 0\text{pF}$  With a Load of  $50\Omega || 20\text{pF} || 1\text{M}\Omega$  (Scope Input)
- $V_{OUT} = \pm 4.1V$  Into  $75\Omega$
- Offset Null Terminals

### Applications

- Video Line Driver
- High-Frequency Unity Gain Buffer
- Pulse Amplifier
- High-Speed Comparator
- High-Frequency Oscillator and Video Amplifiers
- Driver for A/Ds in Video Applications ..... 10MHz BW

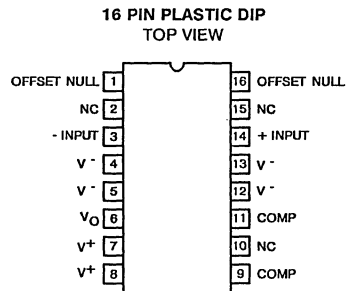
### Description

The CA3450\* is a large signal video line driver and high speed operational amplifier capable of driving  $50\Omega$  transmission lines and flash A/Ds. The uncompensated unity gain crossing occurs at 230MHz without load. It can operate dual or single supplies of  $\pm 7.25V$  or  $14.5V$ , respectively. The CA3450 can be compensated with a single capacitor network. It has output drive capability of 75mA SINK or SOURCE. The CA3450 is capable of driving Flash A/D's in video or high-speed instrumentation (accurate) applications with bandwidth up to 10MHz. Offset voltage nulling terminals are also available.

The CA3450 is available in a 16-lead dual-in-line plastic package (E suffix).

\*Formerly RCA Development Type No. TA11371A.

### Pinout



### Block Diagram

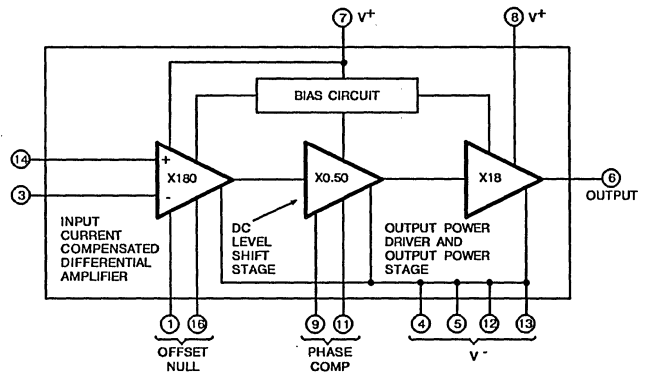


FIGURE 1.

# CA3450

## MAXIMUM RATINGS, Absolute-Maximum Values

|  |                               |
|--|-------------------------------|
| DC SUPPLY VOLTAGE (BETWEEN V+ AND V- TERMINAL) | 14.5 V                        |
| DIFFERENTIAL INPUT VOLTAGE                     | ±5 V                          |
| DEVICE DISSIPATION:                            |                               |
| Up to 55°C                                     | 1.5 W                         |
| Above 55°C                                     | Derate linearly at 16.6 mW/°C |
| OUTPUT CURRENT (SINK OR SOURCE)                | 100 mA                        |
| TEMPERATURE RANGE                              |                               |
| Operating                                      | -40°C to 85°C                 |
| Storage  | -65°C to 150°C                |
| MAXIMUM JUNCTION TEMPERATURE                   | 150°C                         |
| MAXIMUM THERMAL RESISTANCE                     |                               |
| Junction to Air (θ <sub>J-A</sub> )            | 60°C/W                        |
| Junction to Case (θ <sub>J-C</sub> )           | 12°C/W                        |
| To pins 4, 5, 12, 13 at seat                   |                               |

## ELECTRICAL CHARACTERISTICS, At T<sub>A</sub> = 25°C, C<sub>C</sub> = 5 pF, V<sub>+</sub>, V<sub>-</sub> = 6 V\*

| CHARACTERISTICS                                | CONDITIONS                                       | LIMITS        |      |      | UNITS |
|--|--|---------------|------|------|-------|
|  |  | MIN.          | TYP. | MAX. |       |
| <b>STATIC</b>                                  |  |               |      |      |       |
| Input Offset Voltage,  V <sub>IO</sub>         | T <sub>A</sub> = 25°C                            | —             | 8    | 20   | mV    |
|  | T <sub>A</sub> = -40°C to 85°C                   | —             | 10   | 35   |       |
| Input Bias Current,  I <sub>IB</sub>           | T <sub>A</sub> = 25°C                            | —             | 100  | 400  | nA    |
| Input Offset Current,  I <sub>IO</sub>         | T <sub>A</sub> = 25°C                            | —             | 50   | 200  |       |
| Open Loop DC Gain, A <sub>OL</sub>             | V <sub>OUT</sub> = ±2.5 V; R <sub>L</sub> = 50 Ω | -40°C to 85°C | 55   | —    | dB    |
|  |  | 25°C          | 60   | 70   |       |
| Power Supply Rejection Ratio, P <sub>SRR</sub> | ΔV = ±1 V  | 55            | 65   | —    | dB    |
| Common-Mode Rejection Ratio, C <sub>MRR</sub>  | V <sub>ICR</sub> ± = ±3.5 V                      | 50            | 60   | —    |       |
| Common-Mode Input Range, V <sub>ICR</sub>      | T <sub>A</sub> = -40°C to 85°C                   | ±3.0          | —    | —    | V     |
|  | T <sub>A</sub> = 25°C                            | ±3.5          | ±3.7 | —    |       |
| Supply current, I                              | T <sub>A</sub> = -40°C to 85°C                   | —             | —    | 50   | mA    |
|  | T <sub>A</sub> = 25°C                            | —             | 30   | 40   |       |

\*All test are performed with ± 6 volts at the terminals of the device.

A 10 ohm, ¼ watt supply decoupling resistor is shown in all application circuits of this device. The resistor serves two purpose, first provides a means of decoupling the IC directly at its terminal without introducing

additional supply resonance due to parallel connected capacitors. Secondly, it also provides protection for the device in event of a sustained short circuit applied directly to the output terminals.

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## CA3450

**ELECTRICAL CHARACTERISTICS, At  $T_A = 25^\circ\text{C}$ ,  $C_C = 5\text{ pF}$ ,  $V_+$ ,  $V_- = 6\text{ V}^*$**

| CHARACTERISTICS  | CONDITIONS  | LIMITS   |      |      | UNITS                  |                  |
|--|---|--|------|------|------------------------|------------------|
|  |   | MIN.   | TYP. | MAX. |                        |                  |
| <b>DYNAMIC</b>   |   |  |      |      |                        |                  |
| -3 dB Bandwidth<br>$A_V = 1$ (See Figure 3)<br>$C_C = 5\text{ pF}$   | No Load   | —  | 200  | —    | MHz                    |                  |
|  | $R_L = 1\text{ M}\Omega \parallel 20\text{ pF}$                                       | —  | 190  | —    |                        |                  |
|  | $R_L = 50\text{ Ohms} \parallel 20\text{ pF}$   | —  | 185  | —    |                        |                  |
| Bandwidth (Unity Gain Crossing)<br>$A_V = \text{Open Loop}$<br>$C_C = 0$ (See Figure 2)  | No Load   | 210  | 230  | —    |                        |                  |
|  | $R_L = 20\text{ pF} \parallel 1\text{ M}\Omega$                                       | 180  | 200  | —    |                        |                  |
|  | $R_L = 50\text{ Ohms} \parallel 20\text{ pF}$   | 180  | 220  | —    |                        |                  |
| Bandwidth (Unity Gain Crossing)<br>$A_V = 10$ , $C_C = 0\text{ pF}$<br>$R_{\text{Feedback}} = 450\text{ }\Omega$<br>$R_{\text{Pin 3-G}} = 50\text{ }\Omega$ (See Figure 3) | No Load   | 200  | 210  | —    |                        |                  |
|  | $50\text{ }\Omega$  | 175  | 190  | —    |                        |                  |
|  | $1\text{ M} \parallel 20\text{ pF}$   | 180  | 195  | —    |                        |                  |
|  | $50\text{ }\Omega \parallel 1\text{ M} \parallel 20\text{ pF}$                        | 170  | 188  | —    |                        |                  |
| Transient Response, Overshoot  | $A_V = 1$ , $C_C = 5\text{ pF}$   | $R_L = 50\text{ }\Omega \parallel 20\text{ pF}$  | —    | 30   | —                      | %                |
|  |   | No Load  | —    | 20   | —                      |                  |
|  | $A_V \geq 10$ , $C_C = 0\text{ pF}$ , $R_L = 50\text{ }\Omega \parallel 20\text{ pF}$ | —  | 10   | —    |                        |                  |
| Settling Time<br>(See Figure 6)  | 2 Volt Step<br>$R_L = 50\text{ }\Omega \parallel 20\text{ pF}$                        | $A_V = -1$ , $C_C = 5\text{ pF}$ , 0.1%, 10 Bits | —    | 35   | —                      | ns               |
|  |   | $A_V = 1$ , $C_C = 5\text{ pF}$ , 0.1%, 10 Bits  | —    | 50   | —                      |                  |
|  |   | $A_V = 10$ , $C_C = 0\text{ pF}$ , 0.1%, 10 Bits | —    | 35   | —                      |                  |
|  |   | $A_V = 10$ , $C_C = 0\text{ pF}$ , 1.0%, 7 Bits  | —    | 25   | —                      |                  |
| Slew Rate, SR<br>(See Figure 3)  | $A_V = 1$ , $C_C = 5\text{ pF}$   | No Load  | —    | 220  | —                      | V/ $\mu\text{s}$ |
|  |   | $R_L = 50\text{ }\Omega \parallel 20\text{ pF}$  | —    | 160  | —                      |                  |
|  | $A_V \geq 10$ , $C_C = 0\text{ pF}$   | No Load  | 370  | 440  | —                      |                  |
|  |   | $R_L = 50\text{ }\Omega \parallel 20\text{ pF}$  | 300  | 330  | —                      |                  |
| Power Bandwidth PBW (MHz)<br>$\text{PBW} = \text{SR}/\pi V_{\text{pp}}$  | $A_V = 5$ , $C_C = 5\text{ pF}$<br>$V_{\text{OUT}} = \pm 3.5\text{ V}$                | No Load  | —    | 10   | —                      | MHz              |
|  |   | $R_L = 50\text{ }\Omega \parallel 20\text{ pF}$  | —    | 7.2  | —                      |                  |
|  | $A_V \geq 10$ , $C_C = 0\text{ pF}$<br>$V_{\text{OUT}} = \pm 2.0\text{ V}$            | No Load  | 29   | 35   | —                      |                  |
|  |   | $R_L = 50\text{ }\Omega \parallel 20\text{ pF}$  | 24   | 26   | —                      |                  |
| Input Noise Voltage $e_n$  | $f = 1\text{ KHz}$  | —  | 12   | —    | nV/ $\sqrt{\text{Hz}}$ |                  |
| Differential Gain  | See Figure 15   | —  | 0.6  | —    | %                      |                  |
| Differential Phase   |   | —  | 0.3  | —    | Degrees                |                  |
| $I_{\text{OUT}}$   | Into +4 V or -4 V   | 60   | 75   | —    | mA                     |                  |
| Output Voltage Swing into 75 Ohms  | $V_{\text{OM}+}$  | 3.9  | +4.1 | —    | V                      |                  |
|  | $V_{\text{OM}-}$  | -3.9   | -4.1 | —    |                        |                  |
| Input Capacitance, $C_i$   | $f = 1\text{ MHz}$  | —  | 2.2  | —    | pF                     |                  |
| Input Resistance, $R_i$  |   | —  | 1    | —    | M $\Omega$             |                  |
| Output Resistance, $R_{\text{OUT}}$  | See Figure 13, $A = 1$ , 30 MHz   | —  | 4    | —    | $\Omega$               |                  |

\*All test are performed with  $\pm 6$  volts at the terminals of the device.

# CA3450

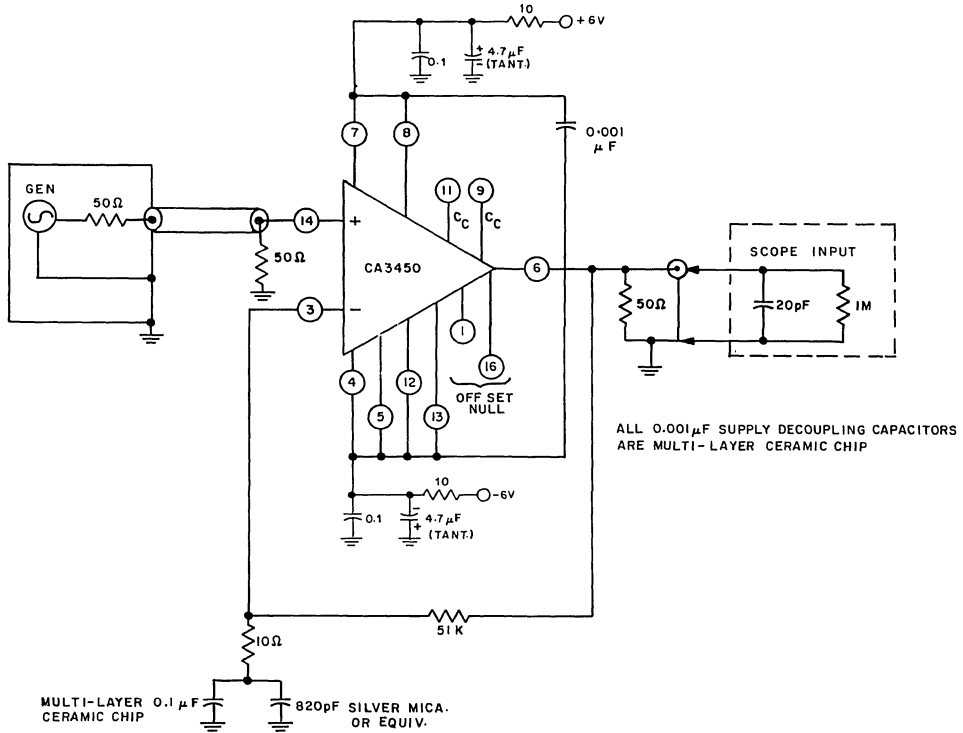


Fig. 2 - Open-loop gain versus frequency test circuit.

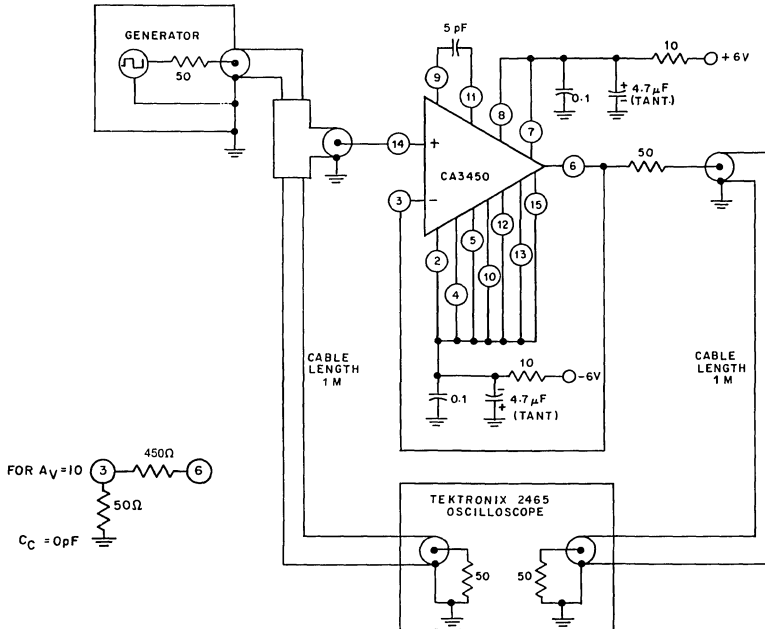


Fig. 3 - Unity-gain and X10 non-inverting amplifier/and slew rate test circuit.



Transient Response Waveforms

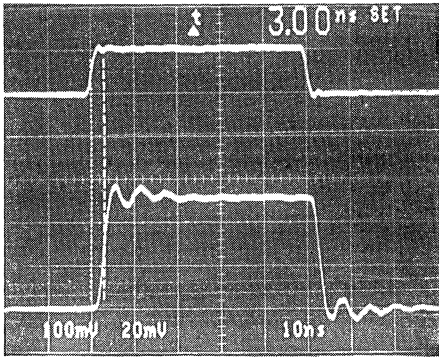


Figure 4 - Transient-response waveform.

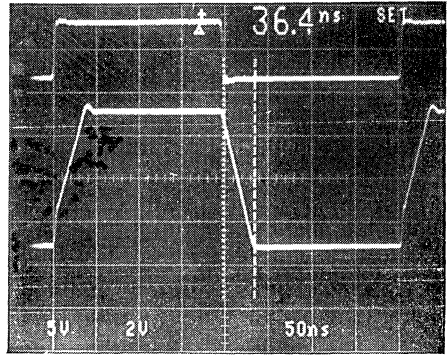


Figure 5 - Slew-rate waveform.

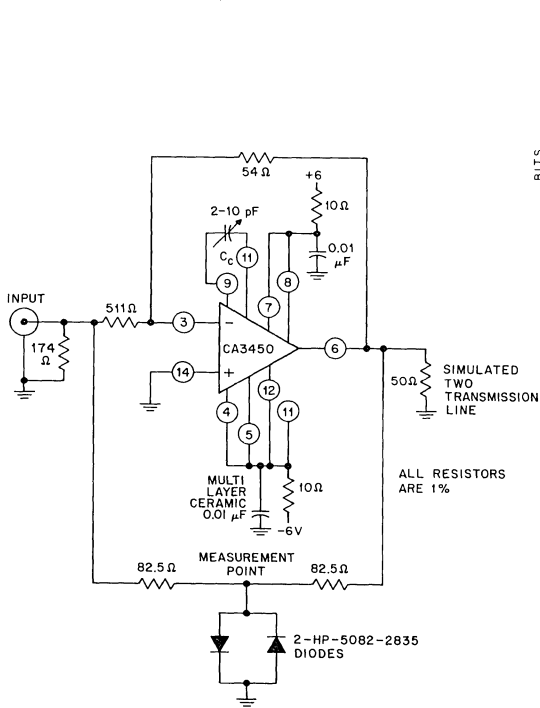


Figure 6 - Circuit used to measure settling time.

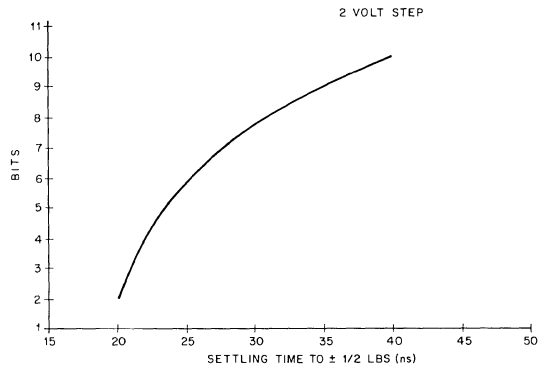


Figure 7 - Accuracy in bits as a function of settling time.

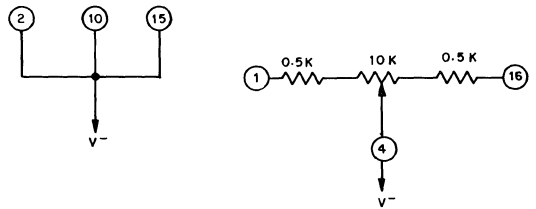


Figure 8 - Nulling circuit for the CA3450.

Typical Performance Curves

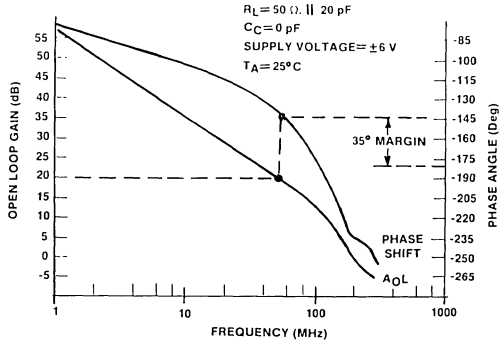


Figure 9 - Bode plot for the CA3450.

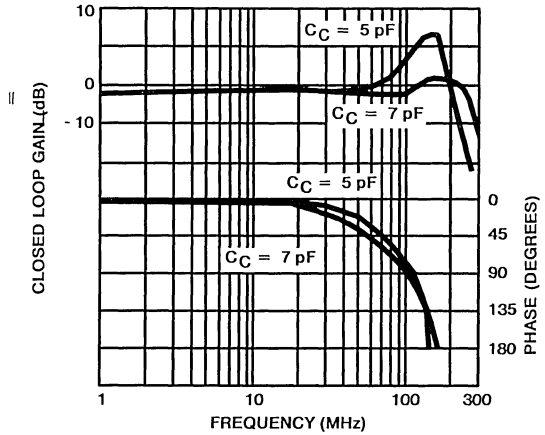


Figure 10 - Closed loop gain and phase vs frequency. ( $A_V = 1$ )

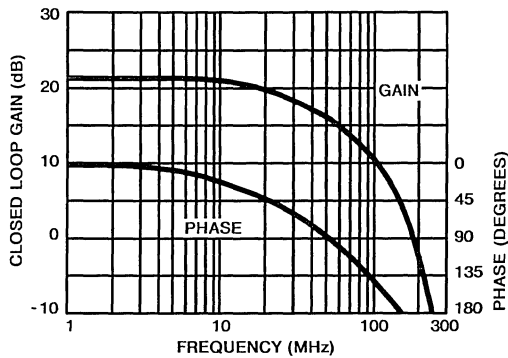


Figure 11 - Closed loop gain and phase vs frequency. ( $A_V = 10$ )

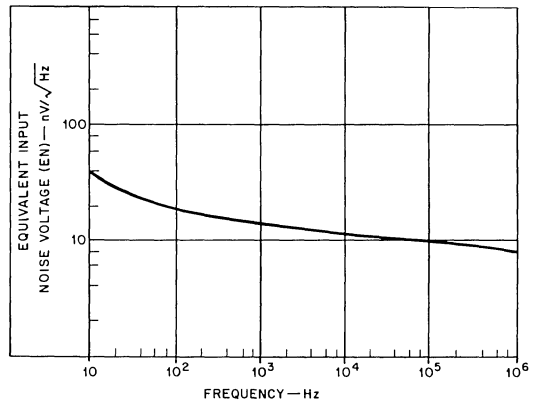


Figure 12 - Curve showing the equivalent input noise "e<sub>n</sub>" of the op amp.

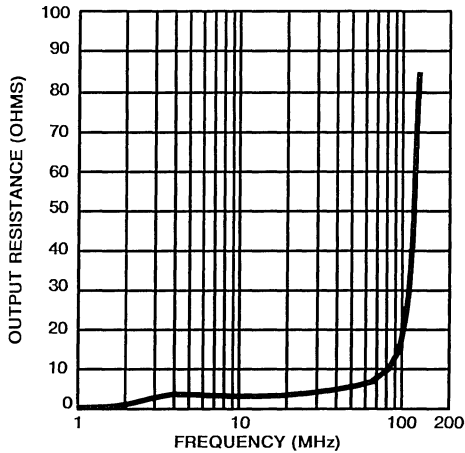


Figure 13 - Output resistance vs frequency.

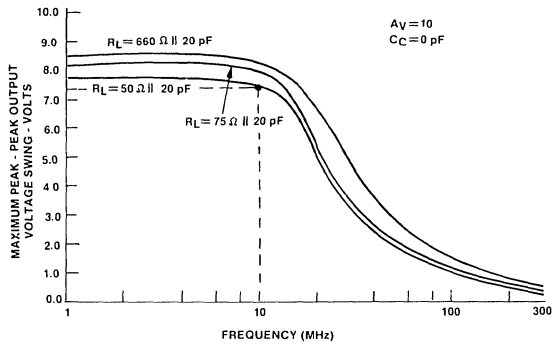


Figure 14 - Output voltage as a function of frequency for the CA3450 under various loads.

# CA3450

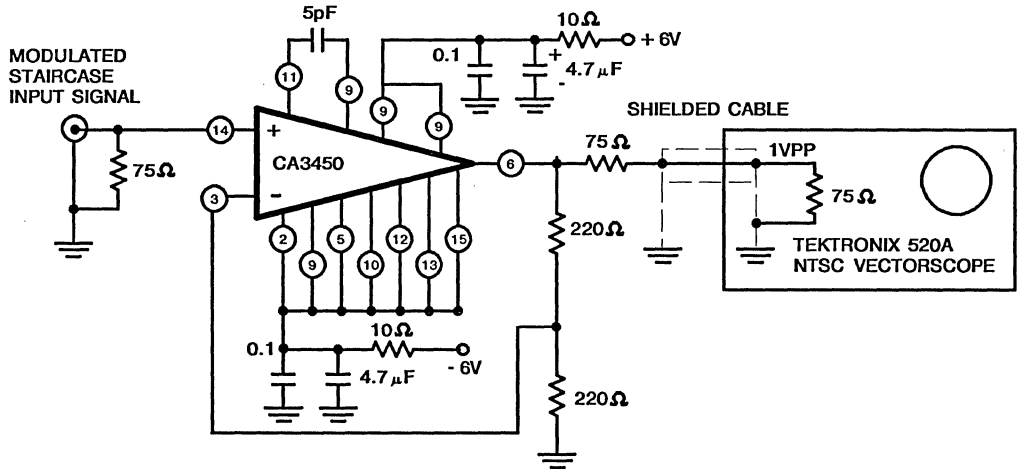


Figure 15 - Configuration used to measure differential gain and phase.

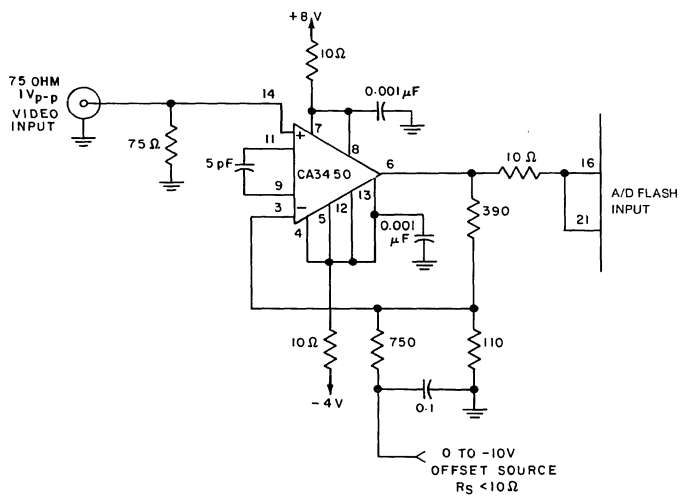


Figure 16 - Typical high-bandwidth X5 amplifier for driving the CA3318 Flash A/D.

# CA3450

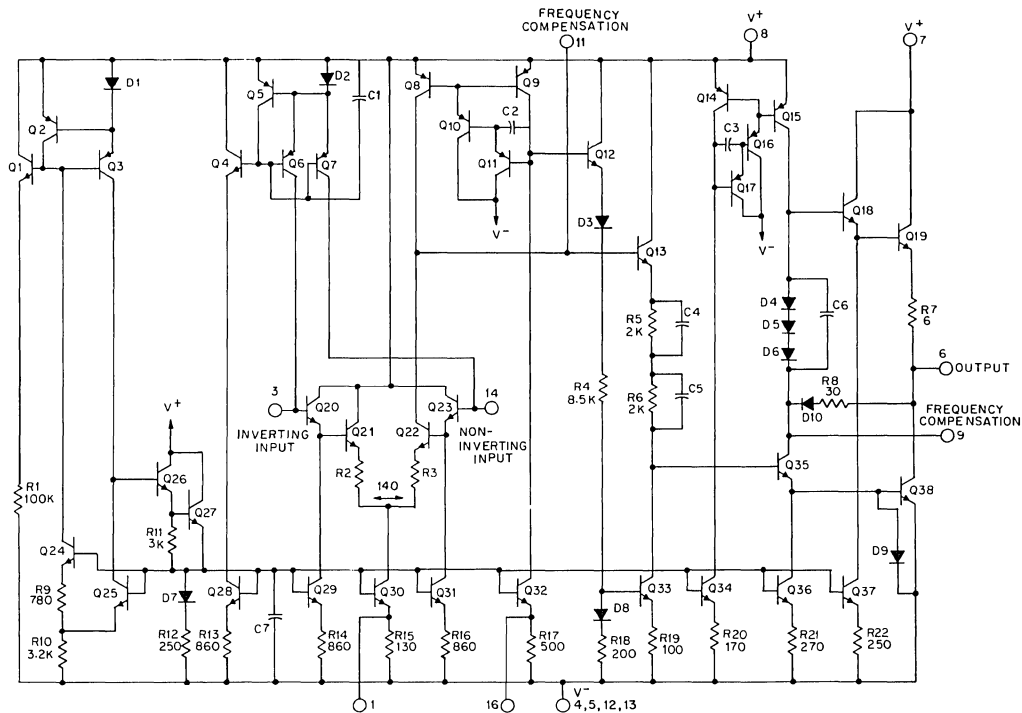
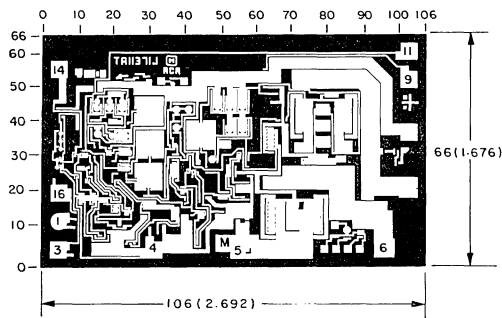


Figure 17 - Full schematic diagram of the CA3450.



M-Bonding wire to Chip Mounting Pad.  
Pins 12 and 13 Connected to Chip Mounting Pad.  
No Chip Pads for 2, 10, 12, 13, 15

Figure 18 - Dimensions and pad layout for CA3450H.

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should

consider a tolerance of -3 mils to +16 mils applicable to the nominal dimensions shown.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Scale graduations are in mils (10<sup>-3</sup> inch).

## BiMOS Microprocessor Operational Amplifiers With MOSFET Input/CMOS Output

August 1991

### Features

- MOSFET Input Stage
  - ▶ Very High  $Z_i$  ..... 1.5 T $\Omega$  (1.5 x 10<sup>12</sup> $\Omega$ ) Typ.
  - ▶ Very Low  $I_i$  ..... 5pA Typ. at 15V Operation  
2pA Typ. at 5V Operation
- Ideal for Single-Supply Applications
- Common-Mode Input-Voltage Range Includes Negative Supply Rail; Input Terminals Can Be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or Both) Supply Rails
- CA5130A, CA5130 Have Full Military Temperature Range Guaranteed Specifications for  $V_+ = 5V$
- CA5130A, CA5130 Are Guaranteed to Operate Down to  $V_+ = 4.5V$  for AQL
- CA5130A, CA5130 Are Guaranteed to Operate at  $\pm 7.5$  CA3130A, CA3130 Specifications

### Applications

- Ground-Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long-Duration Timers/Monostables
- High-Input-Impedance Comparators (Ideal Interface with Digital CMOS)
- High-Input-Impedance Wideband Amplifiers
- Voltage Followers (e.g. Follower for Single-Supply D/A Converter)
- Voltage Regulators (Permits Control of Output Voltage Down to Zero Volts)
- Peak Detectors
- Single-Supply Full-Wave Precision Rectifiers
- Photo-Diode Sensor Amplifiers
- 5V Logic Systems
- Microprocessor Interface

### Description

CA5130A and CA5130 are integrated-circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. They are designed and guaranteed to operate in microprocessors or logic systems that use +5V supplies.

Gate-protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5V below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10mV of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA5130 Series circuits operate at supply voltages ranging from 4 to 16 volts, or  $\pm 2$  to  $\pm 8$  volts when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA5130 Series is supplied in standard 8-lead TO-5 style packages (T suffix) and 8-lead dual-in-line formed lead TO-5 style "DIL-CAN" packages (S suffix). The CA5130 is available in chip form (H suffix). The CA5130 and CA5130A are also available in the 8-lead Small Outline package (M suffix) and in the 8-lead dual-in-line plastic package (Mini-DIP E suffix).

The CA5130A, CA5130 have guaranteed specifications for 5V operation over the full military-temperature range of -55°C to +125°C.

### Pinouts

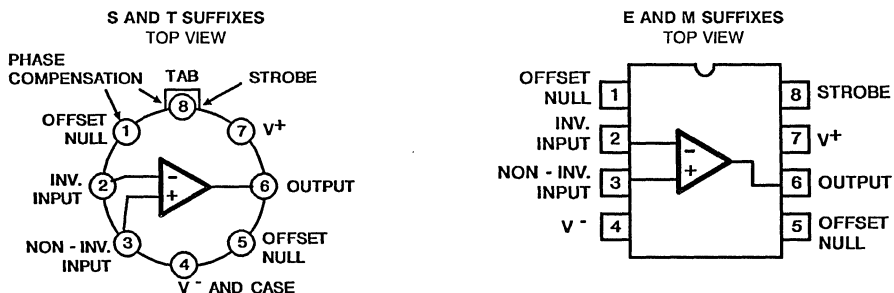


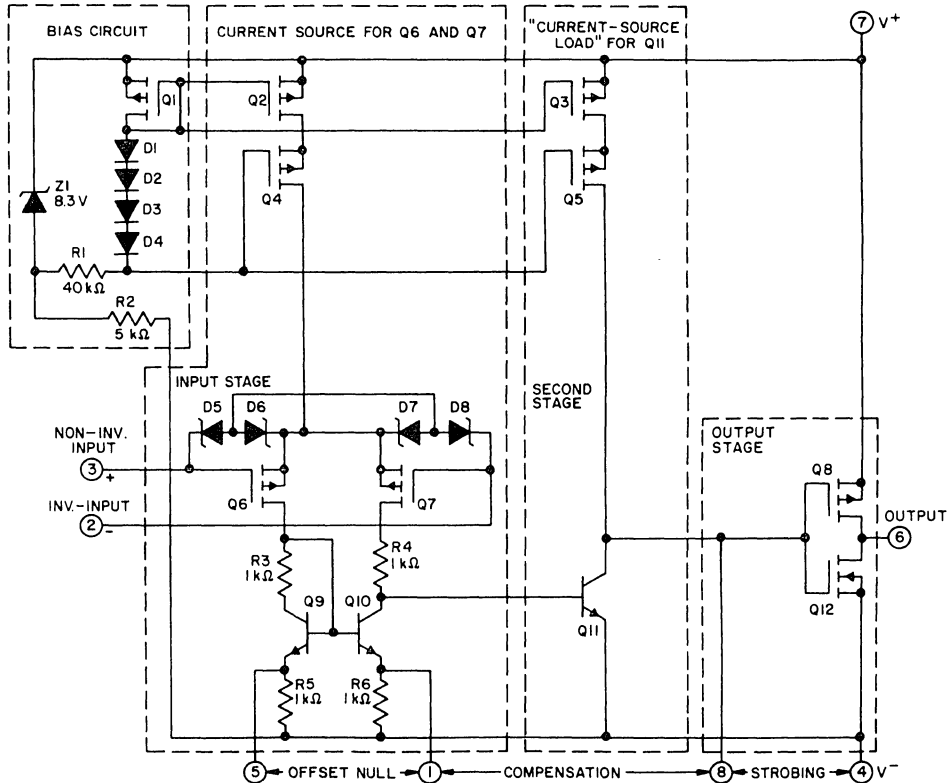
FIGURE 1.

# CA5130A, CA5130

## MAXIMUM RATINGS, Absolute-Maximum Values

|   |  |
|---|--|
| DC SUPPLY VOLTAGE<br>(Between V <sup>+</sup> and V <sup>-</sup> Terminals)  | 16 V   |
| DIFFERENTIAL-MODE INPUT VOLTAGE   | ±8 V   |
| COMMON-MODE DC INPUT VOLTAGE  | (V <sup>+</sup> +8V) to (V <sup>-</sup> -0.5V) |
| INPUT-TERMINAL CURRENT  | 1 mA   |
| DEVICE DISSIPATION:   |  |
| WITHOUT HEAT SINK -   |  |
| UP TO 55°C  | 630 mW   |
| ABOVE 55°C  | Derate Linearly 6.67 mW/°C                     |
| WITH HEAT SINK -  |  |
| UP TO 90°C  | 1 W  |
| ABOVE 90°C  | Derate Linearly 16.7 mW/°C                     |
| SMALL OUTLINE PACKAGE   | 250°/W   |
| TEMPERATURE RANGE:  |  |
| OPERATING (all types)   | -55 to +125°C                                  |
| STORAGE (all types)   | -65 to +150°C                                  |
| OUTPUT SHORT-CIRCUIT DURATION *   | INDEFINITE                                     |
| LEAD TEMPERATURE (DURING SOLDERING):  |  |
| At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. | +265°C   |

\* Short circuit may be applied to ground or to either supply.



NOTE:  
DIODES D5 THROUGH D8 PROVIDE GATE-OXIDE PROTECTION  
FOR MOS/FET INPUT STAGE.

Fig. 2 - Schematic diagram of the CA5130 series.

CA5130A, CA5130

ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$

| CHARACTERISTIC  |                     | LIMITS     |      |      |        |      |      | UNITS         |      |
|---|---------------------|------------|------|------|--------|------|------|---------------|------|
|   |                     | CA5130A    |      |      | CA5130 |      |      |               |      |
|   |                     | MIN.       | TYP. | MAX. | MIN.   | TYP. | MAX. |               |      |
| Input Offset Voltage<br>$V_o = 2.5\text{ V}$                                      | $V_{io}$            | —          | 1.5  | 4    | —      | 2    | 10   | mV            |      |
| Input Offset Current<br>$V_o = 2.5\text{ V}$                                      | $I_{io}$            | —          | 0.1  | 5    | —      | 0.1  | 10   | pA            |      |
| Input Current<br>$V_o = 2.5\text{ V}$   | $I_i$               | —          | 2    | 10   | —      | 2    | 15   |               |      |
| Common-Mode Rejection Ratio<br>$V_{CM} = 0\text{ to }1\text{ V}$                  | $C_{MRR}$           | 75         | 87   | —    | 70     | 85   | —    | dB            |      |
|   | $C_{MRR}$           | 60         | 69   | —    | 60     | 69   | —    |               |      |
| Input Common-Mode Voltage Range   | $V_{ICR}^+$         | 2.5        | 2.8  | —    | 2.5    | 2.8  | —    | V             |      |
|   | $V_{ICR}^-$         | —          | -0.5 | 0    | —      | -0.5 | 0    |               |      |
| Power-Supply Rejection Ratio<br>$\Delta^+ = 1\text{ V}$ ; $\Delta^- = 1\text{ V}$ | $P_{SRR}$           | 60         | 75   | —    | 55     | 73   | —    | dB            |      |
| Large-Signal Voltage Gain*<br>$V_o = 0.1\text{ to }4.1\text{ V}$                  | $A_{OL}$            |            |      |      |        |      |      |               |      |
|   | $R_L = \infty$      | 100        | 105  | —    | 95     | 105  | —    |               |      |
| $V_o = 0.1\text{ to }3.6\text{ V}$  | $R_L = 10\text{ k}$ | 90         | 97   | —    | 85     | 95   | —    |               |      |
| Source Current<br>$V_o = 0\text{ V}$  | $I_{SOURCE}$        | 1.0        | 3.1  | 4.0  | 1.0    | 2.6  | 4.0  | mA            |      |
| Sink Current<br>$V_o = 5\text{ V}$  | $I_{SINK}$          | 1.0        | 1.6  | 4.0  | 1.0    | 1.7  | 4.0  |               |      |
| Output Voltage<br>$R_L = \infty$  | $V_{OUT}$           |            |      |      |        |      |      | V             |      |
|   | $V_{OM}^+$          | 4.99       | 5    | —    | 4.99   | 5    | —    |               |      |
|   | $V_{OM}^-$          | —          | 0    | 0.01 | —      | 0    | 0.01 |               |      |
|   | $R_L = 10\text{ k}$ | $V_{OM}^+$ | 4.4  | 4.7  | —      | 4.4  | 4.7  |               | —    |
|   |                     | $V_{OM}^-$ | —    | 0    | 0.01   | —    | 0    |               | 0.01 |
|   | $R_L = 2\text{ k}$  | $V_{OM}^+$ | 2.5  | 3.5  | —      | 2.5  | 3.5  |               | —    |
| $V_{OM}^-$  |                     | —          | 0    | 0.01 | —      | 0    | 0.01 |               |      |
| Supply Current<br>$V_o = 0\text{ V}$  | $I_{SUPPLY}$        | —          | 50   | 100  | —      | 50   | 100  | $\mu\text{A}$ |      |
|   | $I_{SUPPLY}$        | —          | 260  | 400  | —      | 260  | 400  |               |      |

\*For  $V^+ = 4.5\text{ V}$  and  $V^- = \text{Gnd}$ ;  $V_{OUT} = 0.5\text{ V to }3.2\text{ V}$  at  $R_L = 10\text{ k}$ .

## CA5130A, CA5130

ELECTRICAL CHARACTERISTICS AT  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$

| CHARACTERISTIC  |                            | LIMITS  |      |      |        |      |      | UNITS         |
|---|----------------------------|---------|------|------|--------|------|------|---------------|
|   |                            | CA5130A |      |      | CA5130 |      |      |               |
|   |                            | MIN.    | TYP. | MAX. | MIN.   | TYP. | MAX. |               |
| Input Offset Voltage<br>$V_O = 2.5\text{ V}$                                      | $V_{IO}$                   | —       | 2    | 10   | —      | 3    | 15   | mV            |
| Input Offset Current<br>$V_O = 2.5\text{ V}$                                      | $I_{IO}$                   | —       | 0.1  | 5    | —      | 0.1  | 10   | nA            |
| Input Current<br>$V_O = 2.5\text{ V}$   | $I_I$                      | —       | 2    | 10   | —      | 2    | 15   |               |
| Common-Mode Rejection Ratio<br>$V_{CM} = 0$ to $1\text{ V}$                       | $C_{MRR}$                  | 60      | 80   | —    | 60     | 80   | —    | dB            |
| $V_{CM} = 0$ to $2.5\text{ V}$  | $C_{MRR}$                  | 55      | 80   | —    | 50     | 80   | —    |               |
| Input Common-Mode Voltage Range   | $V_{ICR}^+$                | 2.5     | 2.8  | —    | 2.5    | 2.8  | —    | V             |
|   | $V_{ICR}^-$                | —       | -0.5 | 0    | —      | -0.5 | 0    |               |
| Power-Supply Rejection Ratio<br>$\Delta^+ = 1\text{ V}$ ; $\Delta^- = 1\text{ V}$ | $P_{SRR}$                  | 45      | 70   | —    | 40     | 66   | —    | dB            |
| Large-Signal Voltage Gain*<br>$V_O = 0.1$ to $4.1\text{ V}$                       | $A_{OL}$<br>$R_L = \infty$ | 94      | 98   | —    | 90     | 98   | —    |               |
| $V_O = 0.1$ to $3.6\text{ V}$   | $R_L = 10\text{ k}$        | 80      | 88   | —    | 75     | 85   | —    |               |
| Source Current<br>$V_O = 0\text{ V}$  | $I_{SOURCE}$               | 0.6     | 2.2  | 5.0  | 0.6    | —    | 5.0  | mA            |
| Sink Current<br>$V_O = 5\text{ V}$  | $I_{SINK}$                 | 0.6     | 1.15 | 5.0  | 0.6    | —    | 5.0  |               |
| Output Voltage<br>$R_L = \infty$  | $V_{OUT}$<br>$V_{OM}^+$    | 4.99    | 5    | —    | 4.99   | 5    | —    | V             |
|   | $V_{OM}^-$                 | —       | 0    | 0.01 | —      | 0    | 0.01 |               |
| $R_L = 10\text{ k}$   | $V_{OM}^+$                 | 4.0     | 4.6  | —    | 4.0    | 4.6  | —    |               |
|   | $V_{OM}^-$                 | —       | 0    | 0.01 | —      | 0    | 0.01 |               |
| $R_L = 2\text{ k}$  | $V_{OM}^+$                 | 2.0     | 3.0  | —    | 2.0    | 3.0  | —    |               |
|   | $V_{OM}^-$                 | —       | 0    | 0.01 | —      | 0    | 0.01 |               |
| Supply Current<br>$V_O = 0\text{ V}$  | $I_{SUPPLY}$               | —       | 80   | 220  | —      | 80   | 220  | $\mu\text{A}$ |
| $V_O = 2.5\text{ V}$  | $I_{SUPPLY}$               | —       | 300  | 500  | —      | 300  | 500  |               |

\*For  $V^+ = 4.5\text{ V}$  and  $V^- = \text{Gnd}$ ;  $V_{OUT} = 0.5\text{ V}$  to  $3.2\text{ V}$  at  $R_L = 10\text{ k}$ .

**3**  
OPERATIONAL  
AMPLIFIERS



**CA5130A, CA5130**

**ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ ,  $V^+ = 15\text{ V}$ ,  $V^- = 0\text{ V}$  (Unless otherwise specified)**

| CHARACTERISTIC  |                   | LIMITS     |                  |      |        |                  |      | UNITS                        |      |
|---|-------------------|------------|------------------|------|--------|------------------|------|------------------------------|------|
|   |                   | CA5130A    |                  |      | CA5130 |                  |      |                              |      |
|   |                   | MIN.       | TYP.             | MAX. | MIN.   | TYP.             | MAX. |                              |      |
| Input Offset Voltage<br>$V_{IO}$<br>$V_{\pm} = \pm 7.5\text{ V}$  | $V_{IO}$          | —          | 2                | 5    | —      | 8                | 15   | mV                           |      |
| Input Offset Current<br>$I_{IO}$<br>$V_{\pm} = \pm 7.5\text{ V}$  | $I_{IO}$          | —          | 0.5              | 20   | —      | 0.5              | 30   | pA                           |      |
| Input Current<br>$I_I$<br>$V_{\pm} = \pm 7.5\text{ V}$  | $I_I$             | —          | 5                | 30   | —      | 5                | 50   | pA                           |      |
| Large-Signal Voltage Gain<br>$A_{OL}$<br>$V_O = 10\text{ V}_{p-p}$ , $R_L = 2\text{ k}\Omega$                 | $A_{OL}$          | 50 k       | 320 k            | —    | 50 k   | 320 k            | —    | V/V                          |      |
|   |                   | 94         | 110              | —    | 94     | 110              | —    | dB                           |      |
| Common-Mode Rejection Ratio<br>$C_{MRR}$  | $C_{MRR}$         | 80         | 90               | —    | 70     | 90               | —    | dB                           |      |
| Common-Mode Input-Voltage Range<br>$V_{ICR}$  | $V_{ICR}$         | 10         | -0.5<br>to<br>12 | 0    | 10     | -0.5<br>to<br>12 | 0    | V                            |      |
|   |                   | —          | 32               | 150  | —      | 32               | 320  | $\mu\text{V}/\text{V}$       |      |
| Power-Supply Rejection Ratio<br>$\Delta V_{IO}/\Delta V_{\pm}$<br>$V_{\pm} = \pm 7.5\text{ V}$                | $P_{SRR}$         | —          | 32               | 150  | —      | 32               | 320  | $\mu\text{V}/\text{V}$       |      |
| Maximum Output Voltage<br>At $R_L = 2\text{ k}$   | $V_{OM}^+$        | 12         | 13.3             | —    | 12     | 13.3             | —    | V                            |      |
|   | $V_{OM}^-$        | —          | 0.002            | 0.01 | —      | 0.002            | 0.01 |                              |      |
|   | At $R_L = \infty$ | $V_{OM}^+$ | 14.99            | 15   | —      | 14.99            | 15   |                              | —    |
|   |                   | $V_{OM}^-$ | —                | 0    | 0.01   | —                | 0    |                              | 0.01 |
| Maximum Output Current<br>$I_{OM}^+$ (Source) @ $V_O = 0\text{ V}$<br>$I_{OM}^-$ (Sink) @ $V_O = 15\text{ V}$ | $I_{OM}^+$        | 12         | 22               | 45   | 12     | 22               | 45   | mA                           |      |
|   | $I_{OM}^-$        | 12         | 20               | 45   | 12     | 20               | 45   |                              |      |
| Supply Current<br>$I^+$<br>$V_O = 7.5\text{ V}$ , $R_L = \infty$<br>$V_O = 0\text{ V}$ , $R_L = \infty$       | $I^+$             | —          | 10               | 15   | —      | 10               | 15   | mA                           |      |
|   |                   | —          | 2                | 3    | —      | 2                | 3    |                              |      |
| Input Offset Voltage Temp. Drift<br>$\Delta V_{IO}/\Delta T$  |                   | —          | 10               | —    | —      | 10               | —    | $\mu\text{V}/^\circ\text{C}$ |      |

## CA5130A, CA5130

### TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

| CHARACTERISTIC  | TEST CONDITIONS<br>V <sup>+</sup> = +7.5 V<br>V <sup>-</sup> = -7.5 V<br>T <sub>A</sub> = 25° C<br>(Unless otherwise specified) | TYPICAL VALUES |        | UNITS |
|---|---|----------------|--------|-------|
|   |   | CA5130A        | CA5130 |       |
| Input Offset Voltage<br>Adjustment Range              | 10 kΩ across<br>Terms. 4 and 5 or 4 and 1   | ±22            | ±22    | mV    |
| Input Resistance R <sub>I</sub>                       |   | 1.5            | 1.5    | TΩ    |
| Input Capacitance C <sub>I</sub>                      | f = 1 MHz   | 4.3            | 4.3    | pF    |
| Equivalent Input Noise<br>Voltage e <sub>n</sub>      | BW = 0.2 MHz<br>R <sub>S</sub> = 1 MΩ*  | 23             | 23     | μV    |
| Unity Gain Crossover<br>Frequency f <sub>r</sub>      | C <sub>C</sub> = 0  | 15             | 15     | MHz   |
|   | C <sub>C</sub> = 47 pF  | 4              | 4      |       |
| Slew Rate, SR:  |   |                |        | V/μs  |
|   |   |                |        |       |
| Closed Loop   | C <sub>C</sub> = 56 pF  | 10             | 10     |       |
| Transient Response:<br>Rise Time t <sub>r</sub>       | C <sub>C</sub> = 56 pF<br>C <sub>L</sub> = 25 pF<br>R <sub>L</sub> = 2 kΩ<br>(Voltage Follower)                                 |                |        | μs    |
|   |   |                |        |       |
| Settling Time (4 V <sub>p-p</sub> Input to<br>< 0.1%) |   | 10             | 10     | %     |
|   |   | 1.2            | 1.2    | μs    |

\* Although a 1-MΩ source is used for this test, the equivalent input noise remains constant for values of R<sub>S</sub> up to 10 MΩ.

**CIRCUIT DESCRIPTION**

Fig. 3 is a block diagram of the CA5130 Series CMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA5130 Series circuits are ideal for single-supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in Fig. 3, provide the total gain of the CA5130. A biasing circuit provides two potentials for common use in the first and second stages. Term. 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Term. 8 is tied to the negative supply rail (Term. 4) by mechanical or electrical means, the output potential at Term. 6 essentially rises to the positive supply-rail potential at Term. 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive CMOS digital circuits in comparator applications).

**Input Stages**

The circuit of the CA5130 is shown in Fig. 2. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS transistors Q2, Q4 are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D8 provide gate-oxide protection against high-voltage transients, e.g., including static electricity during handling for Q6 and Q7.

**Second-Stage**

Most of the voltage gain in the CA5130 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials

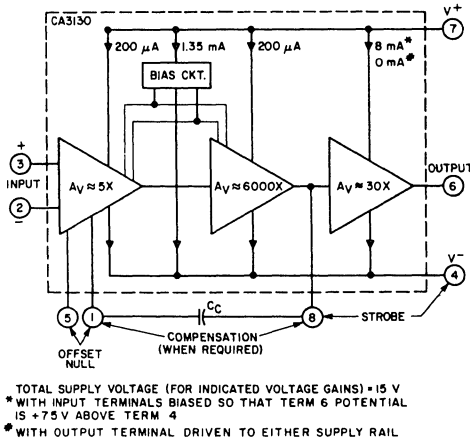


Fig. 3 - Block diagram of the CA5130 series.

for these PMOS transistors is subsequently described. Miller-Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terms. 1 and 8. A 47-picofarad capacitor provides sufficient compensation for stable unity-gain operation in most applications.

**Bias-Source Circuit**

At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Term. 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Term. 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected" to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes non-conductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

**Output Stage**

The output stage consists of a drain-loaded inverting amplifier using CMOS transistors operating in the Class A mode. When operating into very high resistance load, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig. 6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feed-back for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 percent accuracy levels, including the negative supply rail.

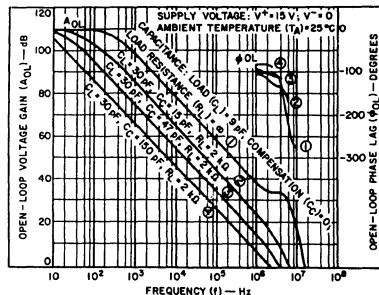


Fig. 4 - Open-loop voltage gain and phase shift vs. frequency for various values of  $C_L$ ,  $C_c$ , and  $R_L$ .

# CA5130A, CA5130

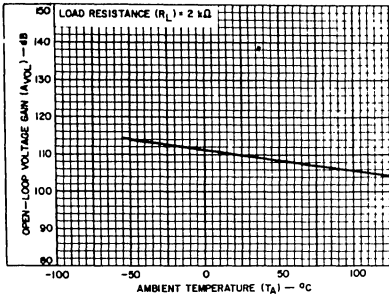


Fig. 5 - Open-loop gain vs. temperature.

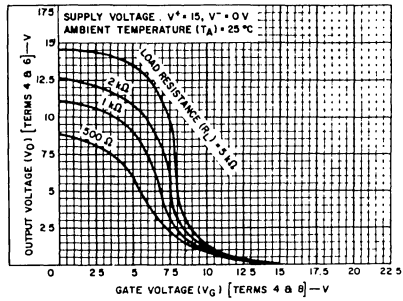


Fig. 6 - Voltage transfer characteristics of CMOS output stage.

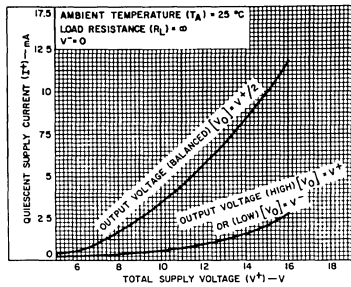


Fig. 7 - Quiescent supply current vs. supply voltage.

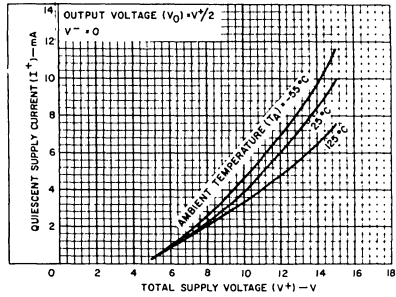


Fig. 8 - Quiescent supply current vs. supply voltage at several temperatures.

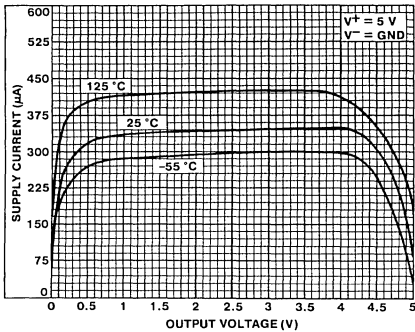


Fig. 9 - Supply current vs. output voltage.

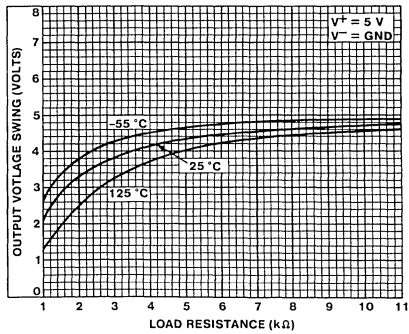


Fig. 10 - Output voltage swing vs. load resistance.

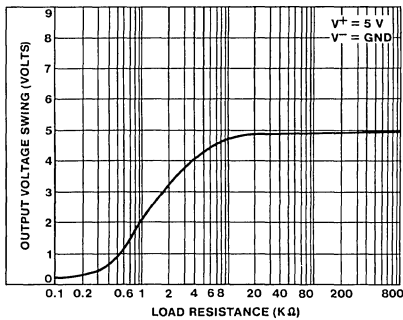


Fig. 11 - Output swing vs. load resistance.

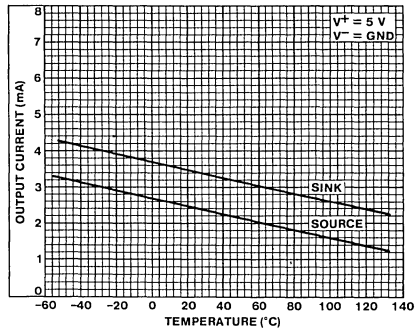


Fig. 12 - Output current vs. temperature.

**Input Current Variation with Common-Mode Input Voltage**

As shown in the Table of Electrical Characteristics, the input current for the CA5130 Series Op-Amps is typically 5 pA at  $T_A = 25^\circ\text{C}$  when terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Fig. 15 contains data showing the variation of input current as a function of common-mode input voltage at  $T_A = 25^\circ\text{C}$ . These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1 pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA5130 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

**Offset Nulling**

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terms. 1 and 5 and with the potentiometer slider arm connected to Term. 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

**Input-Current Variation with Temperature**

The input current of the CA5130 Series circuits is typically 5 pA at  $25^\circ\text{C}$ . The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every  $10^\circ\text{C}$  increase in temperature. Fig. 16 provides data on the typical variation of input bias current as a function of temperature in the CA5130.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA5130. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

**Input-Offset-Voltage ( $V_{IO}$ ) Variation with DC Bias vs. Device Operating Life**

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA5130 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across

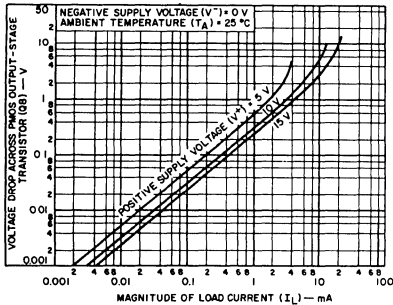


Fig. 13 - Voltage across PMOS output transistor (Q8) vs. load current.

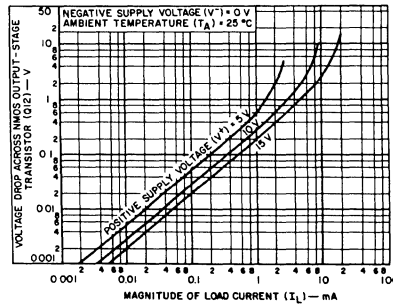


Fig. 14 - Voltage across NMOS output transistor (Q12) vs. load current.

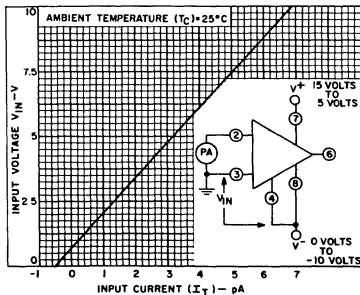


Fig. 15 - CA5130 input current vs. common-mode voltage.

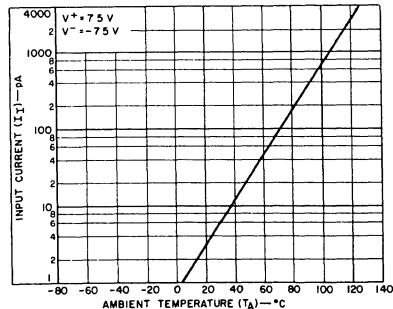


Fig. 16 - Input current vs. ambient temperature.

## CA5130A, CA5130

Terms. 2 and 3. Fig. 17 shows typical data pertinent to shifts in offset voltage encountered with CA5130 devices (TO-5 package) during life testing. At lower temperatures (TO-5 and plastic), for example at 85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output stage is "toggled", e.g., as in comparator applications.

### Power-Supply Considerations

Because the CA5130 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single- and dual-supply service. Figs. 18a and 18b show the CA5130 connected for both dual- and single-supply operation.

**Dual-supply operation:** When the output voltage at Term. 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

**Single-supply operation:** Initially, let it be assumed that the value of  $R_L$  is very high (or disconnected), and that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at  $V^+/2$ , i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA5130 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Term. 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA5130, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 14a shows a dual-supply arrangement for the output stage that can also be strobed off, assuming  $R_L = \infty$ , by pulling the potential of Term. 8 down to that of Term. 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Term. 6 and ground in the circuit of Fig. 18b. Let it further be assumed again that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is a  $V^+/2$ . Since PMOS transistor Q8 must now supply quiescent current to

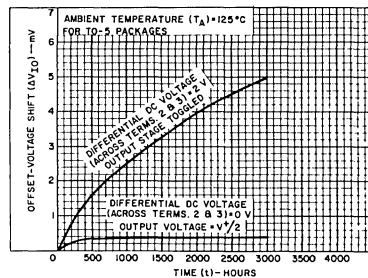


Fig. 17 - Typical incremental offset-voltage shift vs. operating life.

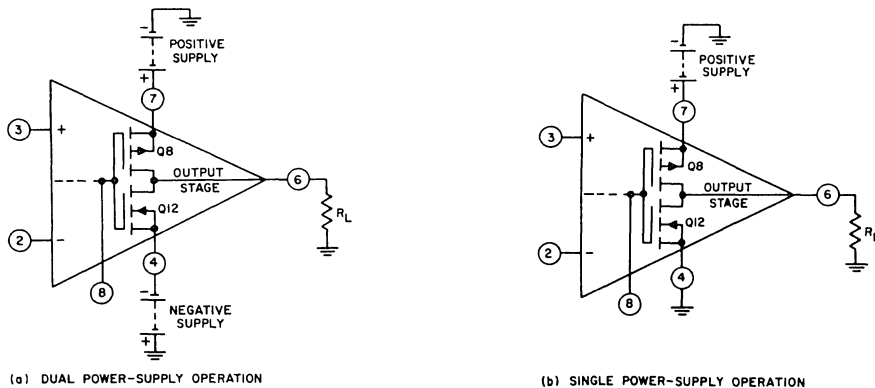


Fig. 18 - CA5130 output stage in dual and single power-supply operation.

## CA5130A, CA5130

both  $R_L$  and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the  $R_L$  magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply-voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

### Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA5130 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only  $23 \mu\text{V}$  when the test-circuit amplifier of Fig. 19 is operated at a total supply voltage of 15 volts. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

### TYPICAL APPLICATIONS

#### Voltage Followers

Operational amplifiers with very high input resistances, like the CA5130, are particularly suited to service as voltage followers. Fig. 20 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA5130 in a split-supply configuration.

A voltage follower, operated from a single supply, is shown in Fig. 21, together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig. 21a with input-signal ramping. The waveforms in Fig. 21b show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator

applications. Fig. 21b also shows the manner in which the CMOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA5130 in a single-supply voltage-follower application.

### 9-BIT CMOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)\* is shown in Fig. 22. This system combines the concepts of multiple-switch CMOS IC's a low-cost ladder network of discrete metal-oxide-film resistors, a CA5130 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig. 22.

The circuit uses an R/2R voltage-ladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one percent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA5130 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the CMOS building blocks simplifies the design of DAC systems tailored to particular needs.

\*"Digital-to-Analog Conversion Using the Harris CD4007A CMOS IC", Application Note ICAN-6080.

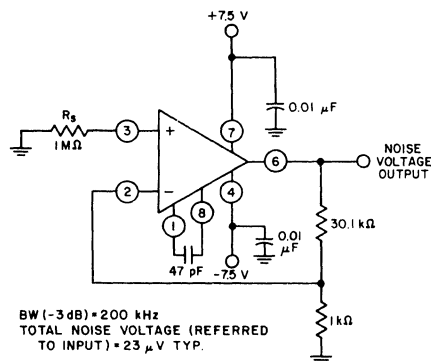
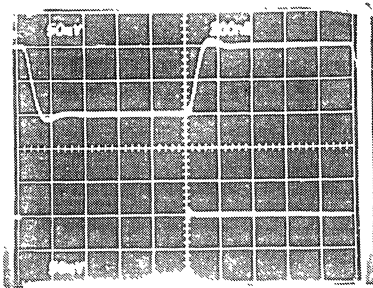
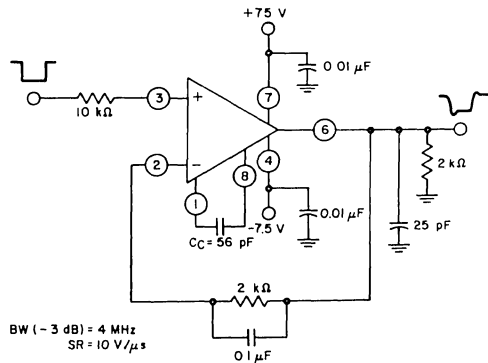


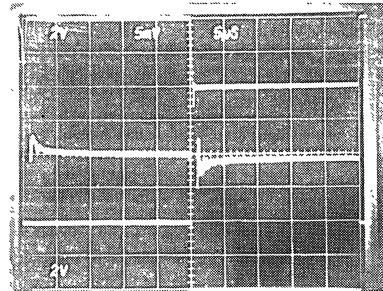
Fig. 19 - CA5130 test-circuit amplifier (30 -dB gain) used for wideband noise measurements.

## CA5130A, CA5130



Top Trace: Output  
Bottom Trace: Input

(a) Small-signal response (50 mV/div. and 200 ns/div.)



Top Trace: Output signal (2 V/div. and 5  $\mu$ s/div.)  
Center Trace: Difference signal (5 mV/div. and 5  $\mu$ s/div.)  
Bottom Trace: Input signal (2 V/div. and 5  $\mu$ s/div.)

(b) Input-output difference signal showing settling time  
(Measurement made with Tektronix 7A13 differential amplifier)

Fig. 20 - CA5130 split-supply voltage follower with associated waveforms.

### Single-Supply, Absolute-Value, Ideal Full-Wave Rectifier

The absolute-value circuit using the CA5130 is shown in Fig. 23. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA5130 functions as a normal inverting amplifier with a gain equal to  $-R_2/R_1$ . When the equality of the two equations shown in Fig. 23 is satisfied, the full-wave output is symmetrical.

### Peak Detectors

Peak-detector circuits are easily implemented with the CA5130, as illustrated in Fig. 24 for both the peak-positive and the peak-negative circuit. It should be noted that with large-signal inputs, the bandwidth of the peak-negative circuit is much less than that of the peak-positive circuit. The second stage of the CA5130 limits the bandwidth in this case. Negative-going output-signal excursion requires a positive-going signal excursion at the collector of transistor Q11, which is loaded by the intrinsic capacitance of the

associated circuitry in this mode. On the other hand, during a negative-going signal excursion at the collector of Q11, the transistor functions in active "pull-down" mode so that the intrinsic capacitance can be discharge more expeditiously.

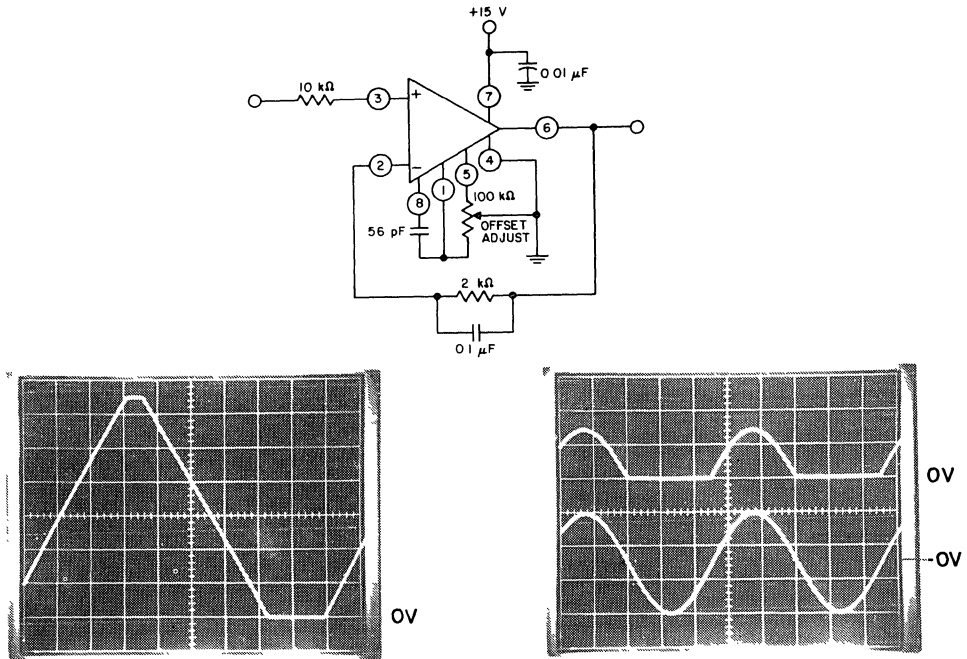
### Error-Amplifier in Regulated-Power Supplies

The CA5130 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero. Fig. 25 shows the schematic diagram of a 40-mA power supply capable of providing regulated output voltage by continuous adjustment over the range from 0 to 13 volts. Q3 and Q4 in IC2 (a CA3086 transistor-array IC) function as zeners to provide supply-voltage for the CA5130 comparator (IC1). Q1, Q2, and Q5 in IC2 are configured as a low impedance, temperature-compensated source of adjustable reference voltage for the error amplifier.

Transistors Q1, Q2, Q3, and Q4 in IC3 (another CA3086 transistor-array IC) are connected in parallel as the series-pass element. Transistor Q5 in IC3 functions as a current-limiting device by diverting base drive from the series-pass transistors, in accordance with the adjustment of resistor R2.



## CA5130A, CA5130



(a) Output-waveform with input-signal ramping (2 V/div. and 500  $\mu$ s/div.)

Top Trace: Output (5 V/div. and 200  $\mu$ s/div.)  
Bottom Trace: Input (5 V/div. and 200  $\mu$ s/div.)

(b) Output-waveform with ground-reference sine-wave input

Fig. 21 - Single-supply voltage-follower with associated waveforms.  
(e.g., for use in single-supply D/A converter; see Fig. 9 in ICAN-6080).

Fig. 26 contains the schematic diagram of a regulated power-supply capable of providing regulated output voltage by continuous adjustment over the range from 0.1 to 50 volts and currents up to 1 ampere. The error amplifier (IC1) and circuitry associated with IC2 function as previously described, although the output of IC1 is boosted by a discrete transistor (Q4) to provide adequate base drive for the Darlington-connected series-pass transistors Q1, Q2. Transistor Q3 functions in the previously described current-limiting circuit.

### Multivibrators

The exceptionally high input resistance presented by the CA5130 is an attractive feature for multivibrator circuit design because it permits the use of timing circuits with high R/C ratios. The circuit diagram of a pulse generator (astable multivibrator), with provisions for independent control of the "on" and "off" periods, is shown in Fig. 27. Resistors R1 and R2 are used to bias the CA5130 to the mid-point of the supply-voltage and R3 is the feedback resistor. The pulse repetition rate is selected by positioning S1 to the desired position and the rate remains essentially constant when the resistors which determine "on-period" and "off-period" are adjusted.

### Function Generator

Fig. 24 contains a schematic diagram of a function generator using the CA5130 in the integrator and threshold detector

functions. This circuit generates a triangular or square-wave output that can be swept over a 1,000,000:1 range (0.1 Hz to 100 kHz) by means of a single control, R1. A voltage-control input is also available for remote sweep-control.

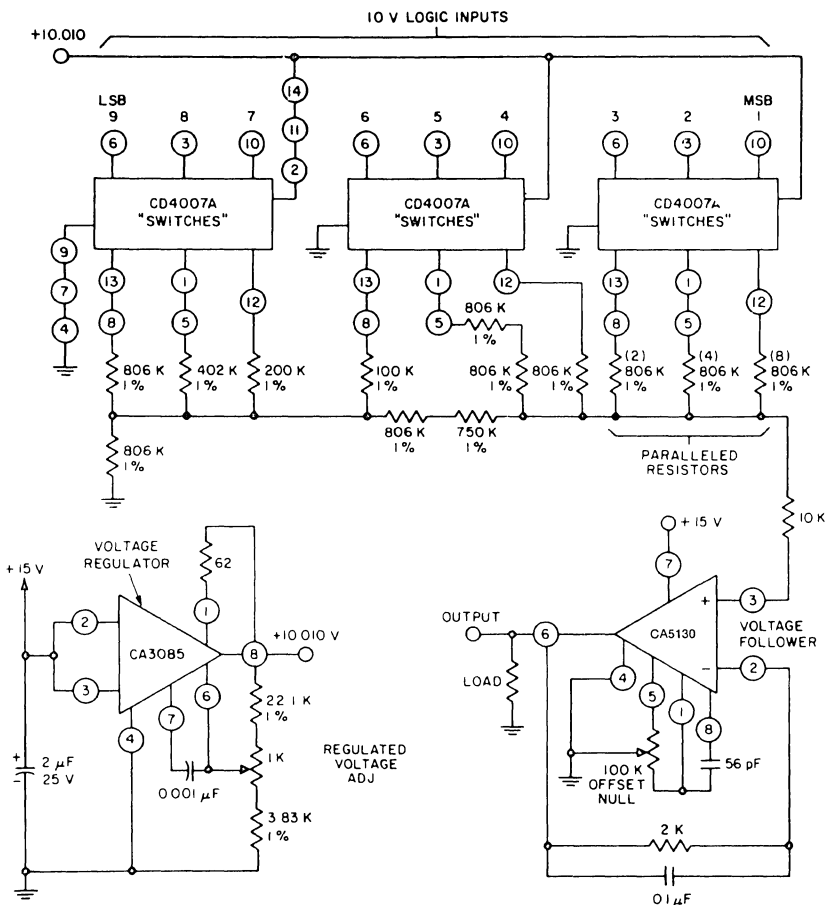
The heart of the frequency-determining system is an operational-transconductance-amplifier (OTA)\*, IC1, operated as a voltage-controlled current-source. The output,  $i_o$ , is a current applied directly to the integrating capacitor, C1, in the feedback loop of the integrator IC2, using a CA5130, to provide the triangular-wave output. Potentiometer R2 is used to adjust the circuit for slope symmetry of positive-going and negative-going signal excursions.

Another CA5130, IC3, is used as a controlled switch to set the excursion limits of the triangular output from the integrator circuit. Capacitor C2 is a "peaking adjustment" to optimize the high-frequency square-wave performance of the circuit.

Potentiometer R3 is adjustable to perfect the "amplitude symmetry" of the square-wave output signals. Output from the threshold detector is fed back via resistor R4 to the input of IC1 so as to toggle the current source from plus to minus in generating the linear triangular wave.

\*See File No. 475 and ICAN-6668.

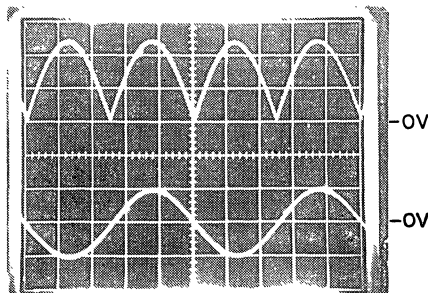
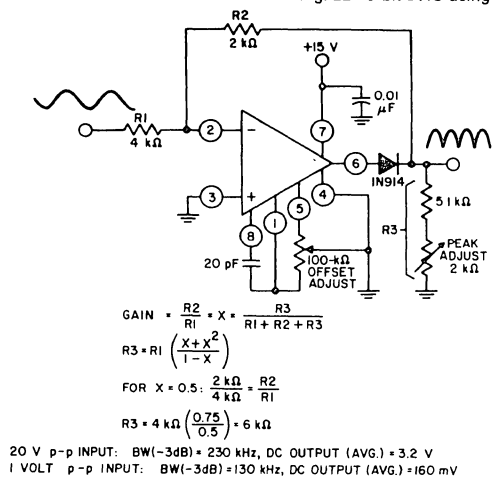
# CA5130A, CA5130



| BIT | REQUIRED RATIO - MATCH |
|-----|------------------------|
| 1   | STANDARD               |
| 2   | ±0.1%                  |
| 3   | ±0.2%                  |
| 4   | ±0.4%                  |
| 5   | ±0.8%                  |
| 6-9 | ±1% ABS                |

ALL RESISTANCES IN OHMS

Fig. 22 - 9-bit DAC using CMOS digital switches and CA5130.



Top Trace: Output signal (2 V/div.)  
 Bottom Trace: Input signal (10 V/div.)  
 Time base on both traces: 0.2 ms/div.

Fig. 23 - CA5130 single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.

OPERATIONAL AMPLIFIERS

## CA5130A, CA5130

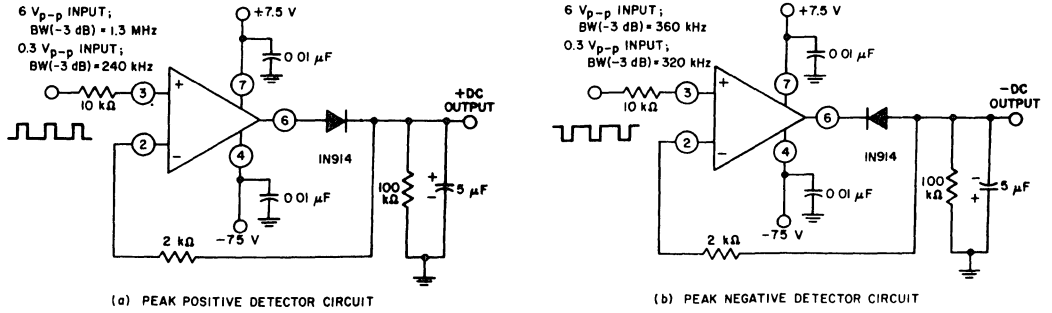


Fig. 24 - CA5130 peak-detector circuits.

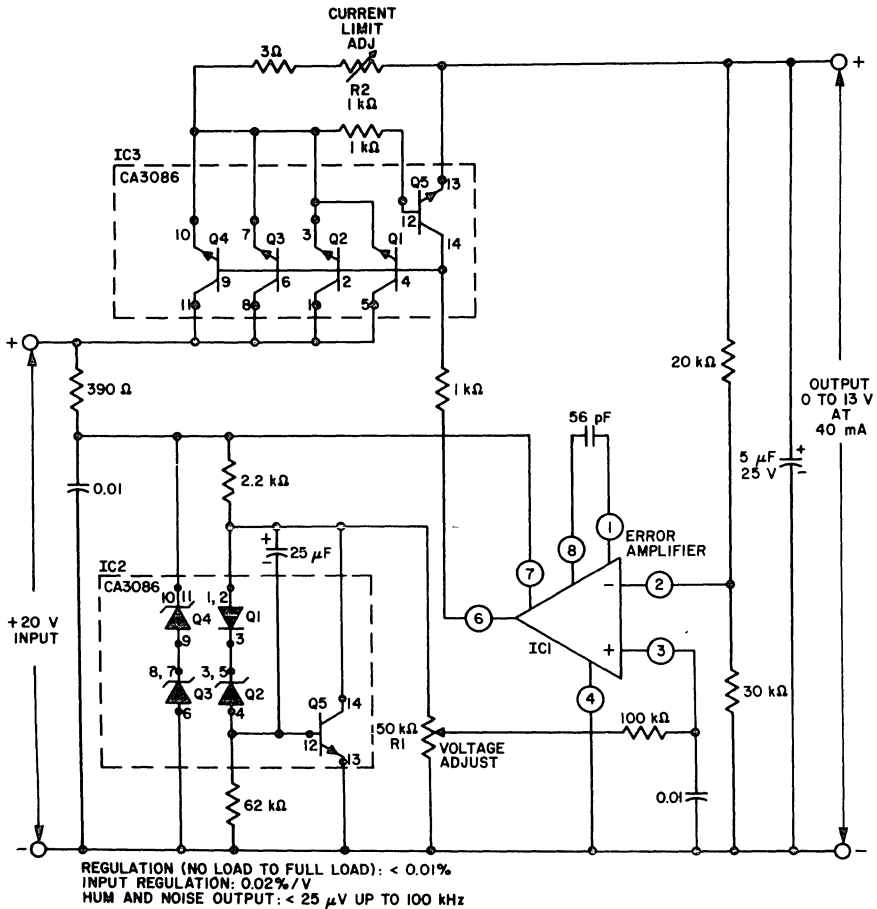
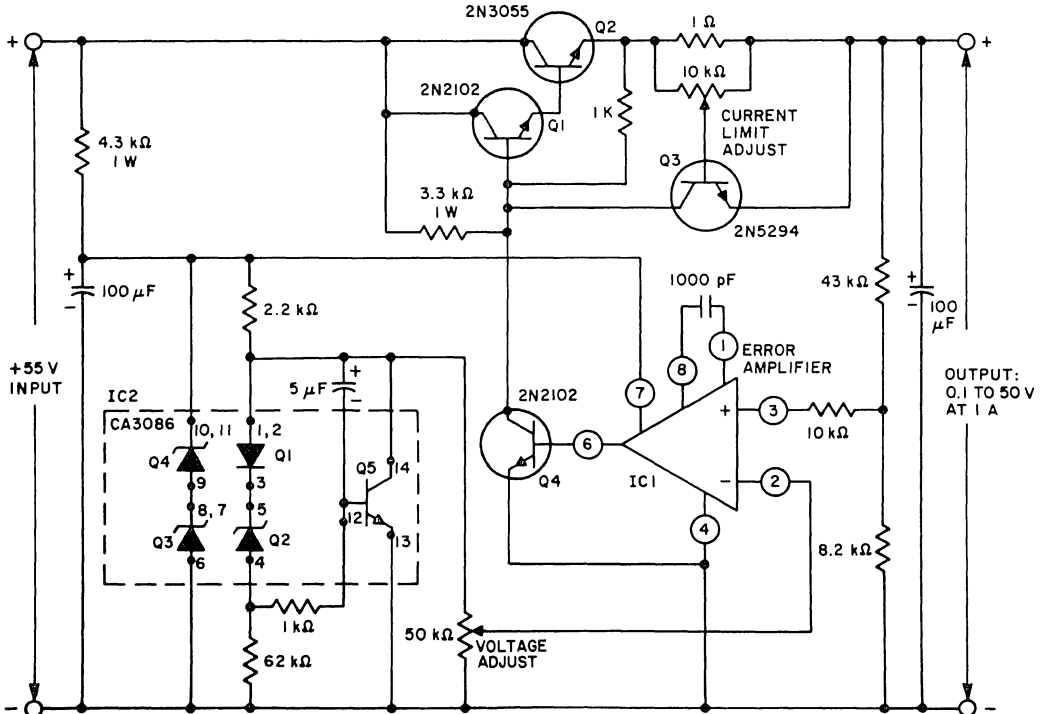


Fig. 25 - CA5130 voltage regulator circuit (0 to 13 V at 40 mA).

## CA5130A, CA5130



REGULATION (NO LOAD TO FULL LOAD): < 0.005 %  
 INPUT REGULATION: < 0.01 % / V  
 HUM AND NOISE OUTPUT: < 250 μV RMS UP TO 100 kHz

Fig. 26 - CA5130 voltage regulator circuit (0.1 to 50 V at 1 A).

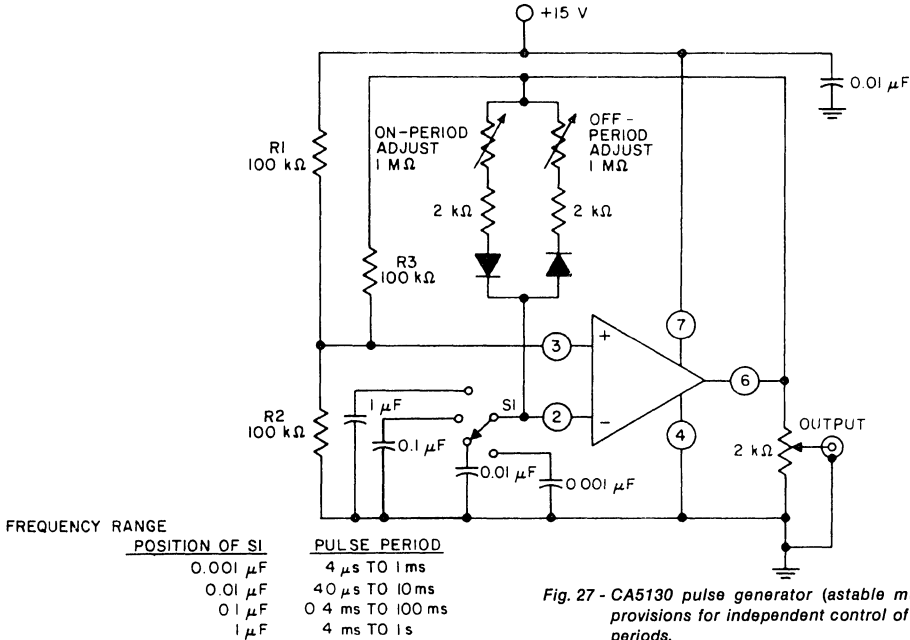
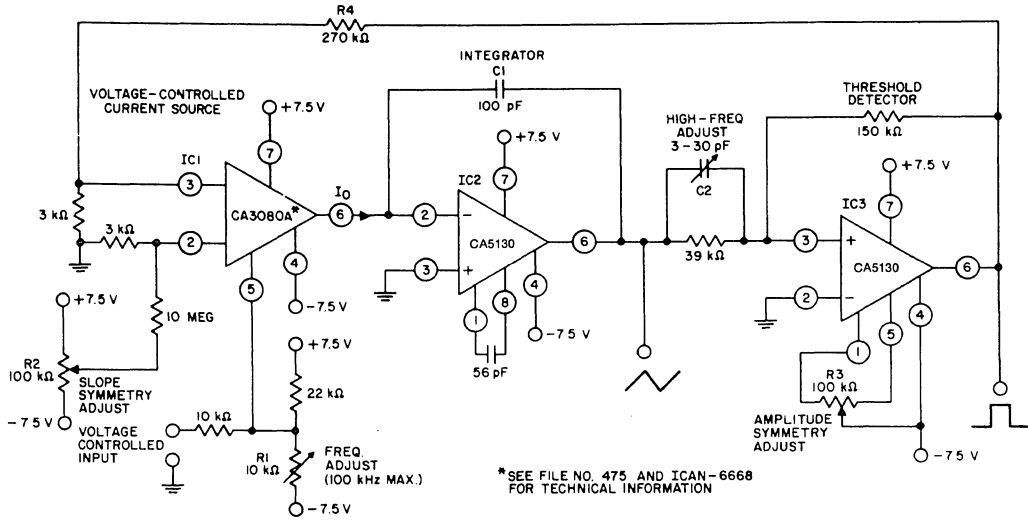


Fig. 27 - CA5130 pulse generator (astable multivibrator) with provisions for independent control of "ON" and "OFF" periods.

## CA5130A, CA5130



**Fig. 28 - Function generator (frequency can be varied 1,000,000/1 with a single control).**

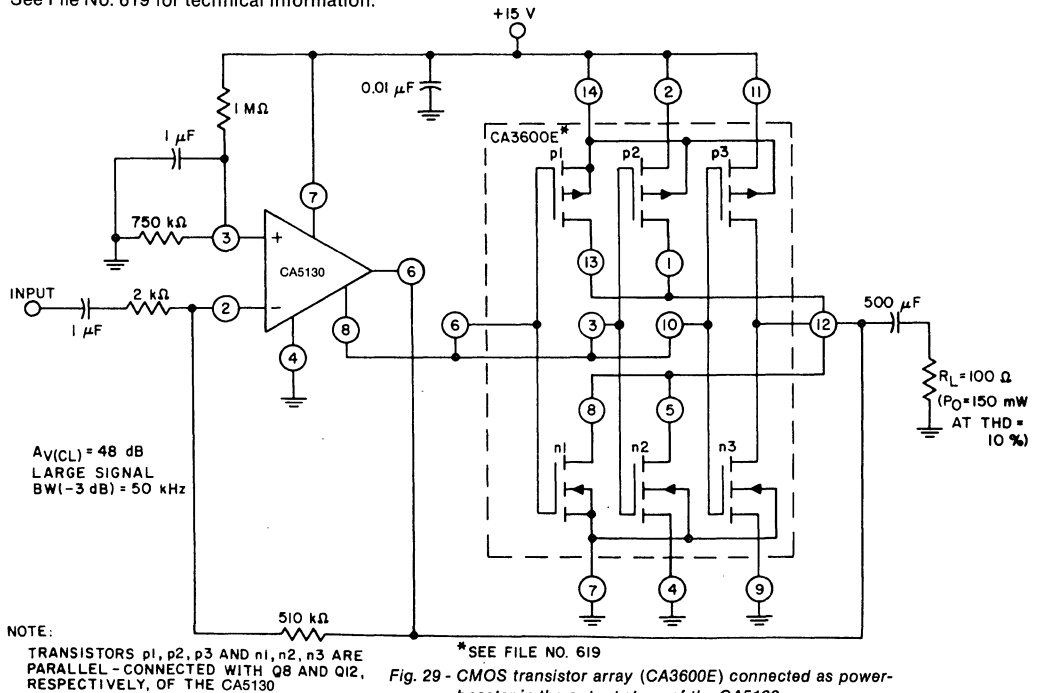
### Operation with Output-Stage Power-Booster

The current-sourcing and -sinking capability of the CA5130 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig. 29, three CMOS transistor-pairs in a single CA3600E\* IC array are shown parallel connected with the output stage in the CA5130. In the Class A mode of CA3600E shown, a typical device

consumes 20 mA of supply current at 15-V operation. This arrangement boosts the current-handling capability of the CA5130 output stage by about 2.5X.

The amplifier circuit in Fig. 29 employs feedback to establish a closed-loop gain of 48 dB. The typical large-signal bandwidth (-3 dB) is 50 kHz.

\*See File No. 619 for technical information.



NOTE:  
TRANSISTORS p1, p2, p3 AND n1, n2, n3 ARE PARALLEL-CONNECTED WITH Q8 AND Q12, RESPECTIVELY, OF THE CA5130

## BiMOS Microprocessor Operational Amplifiers With MOSFET Input/CMOS Output

August 1991

### Features

- MOSFET Input Stage
  - ▶ Very High  $Z_i$  .....  $1.5T\Omega$  ( $1.5 \times 10^{12}\Omega$ ) Typ.
  - ▶ Very Low  $I_i$  .....  $5pA$  Typ. at 15V Operation  
 $2pA$  Typ. at 5V Operation
- Common-Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can Be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or Both) Supply Rails
- CA5160A, CA5160 Have Full Military Temperature Range Guaranteed Specifications for  $V_+ = 5V$
- CA5160A, CA5160 Are Guaranteed to Operate Down to 4.5V for  $A_{OL}$
- CA5160A, CA5160 Are Guaranteed Up To +7.5

### Applications

- Ground Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long Duration Timers/Monostables
- Ideal Interface With Digital CMOS
- High Input Impedance Wideband Amplifiers
- Voltage Followers (e.g. Follower for Single Supply D/A Converter)
- Wien-Bridge Oscillators
- Voltage Controlled Oscillators
- Photo Diode Sensor Amplifiers
- 5V Logic Systems
- Microprocessor Interface

### Description

CA5160A and CA5160 are integrated circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. The CA5160 series circuits are frequency compensated versions of the popular CA5130 series. They are designed and guaranteed to operate in microprocessor or logic systems that use +5V supplies.

Gate-protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very high input impedance, very low input current, and exceptional speed performance. The use of PMOS field effect transistors in the input stage results in common-mode input voltage capability down to 0.5V below the negative supply terminal, an important attribute in single supply applications.

A complementary symmetry MOS (CMOS) transistor pair, capable of swinging the output voltage to within 10mV of either supply voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA5160 Series circuits operate at supply voltages ranging from 5V to 16V, or  $\pm 2.5V$  when using split supplies, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA5160 Series is supplied in standard 8-lead TO-5 style packages (T suffix), 8-lead dual-in-line formed lead TO-5 style "DIL-CAN" packages (S suffix), and 8-lead dual-in-line plastic package (Mini-DIP E suffix). The CA5160 is available in chip form (H suffix). They have guaranteed specifications for 5V operation over the full military temperature range of  $-55^\circ C$  to  $+125^\circ C$ .

 3  
OPERATIONAL AMPLIFIERS

### Pinouts

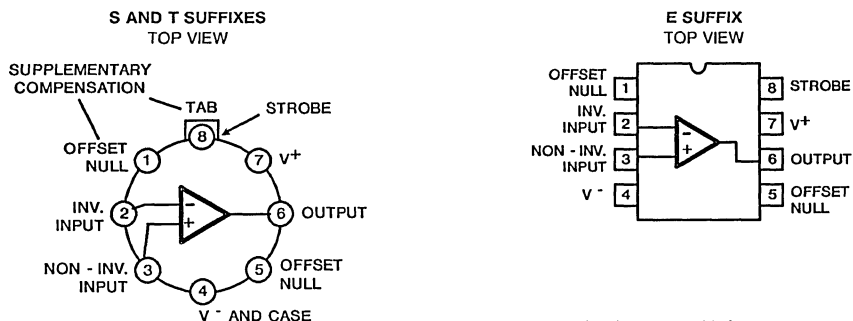


FIGURE 1.

CA5160 Series devices have an on-chip frequency-compensation network. Supplementary phase-compensation or frequency roll-off (if desired) can be connected externally between terminals 1 and 8.

# CA5160A, CA5160

## MAXIMUM RATINGS, Absolute-Maximum Values:

|  |                                    |
|--|------------------------------------|
| DC SUPPLY-VOLTAGE<br>(Between $V^+$ and $V^-$ Terminals) ..... | 16 V                               |
| DIFFERENTIAL-MODE<br>INPUT VOLTAGE .....                       | $\pm 8$ V                          |
| COMMON-MODE DC<br>INPUT VOLTAGE .....                          | ( $V^+ + 8$ V) to ( $V^- - 0.5$ V) |
| INPUT-TERMINAL CURRENT .....                                   | 1 mA                               |
| DEVICE DISSIPATION:  |                                    |
| WITHOUT HEAT SINK -  |                                    |
| UP TO 55°C .....   | 630 mW                             |
| ABOVE 55°C .....   | Derate linearly 6.67 mW/°C         |
| WITH HEAT SINK -   |                                    |
| UP TO 90°C .....   | 1 W                                |
| ABOVE 90°C .....   | Derate linearly 16.7 mW/°C         |

|  |               |
|--|---------------|
| TEMPERATURE RANGE:   |               |
| OPERATING (All Types) .....  | -55 to +125°C |
| STORAGE (All Types) .....  | -65 to +150°C |
| OUTPUT SHORT-CIRCUIT<br>DURATION* .....                            | INDEFINITE    |
| LEAD TEMPERATURE<br>(DURING SOLDERING):                            |               |
| AT DISTANCE $1/16 \pm 1/32$ INCH<br>(1.59 $\pm$ 0.79 MM) FROM CASE |               |
| FOR 10 SECONDS MAX .....   | +265°C        |

\*Short circuit may be applied to ground or to either supply.

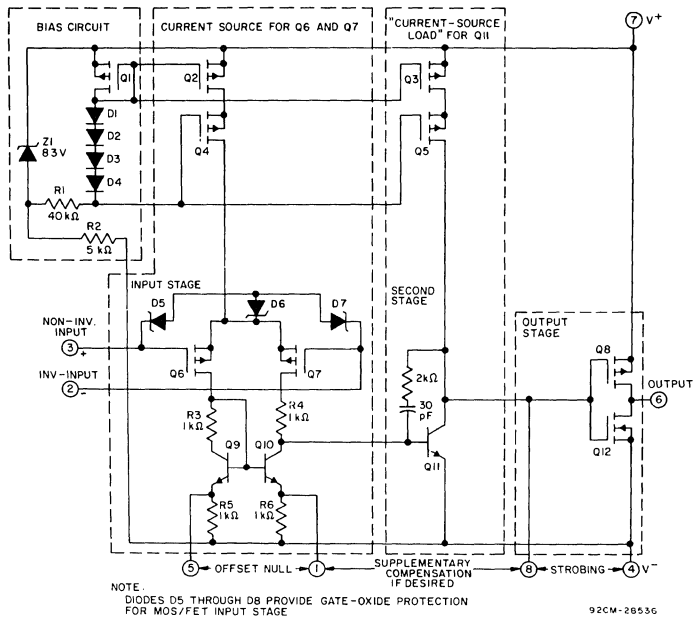


Fig. 2 — Schematic diagram of the CA5160 Series.

## CA5160A, CA5160

**ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$

| CHARACTERISTIC  |                     | LIMITS  |      |      |        |      |      | UNITS         |
|---|---------------------|---------|------|------|--------|------|------|---------------|
|   |                     | CA5160A |      |      | CA5160 |      |      |               |
|   |                     | Min.    | Typ. | Max. | Min.   | Typ. | Max. |               |
| Input Offset Voltage                                  | $V_{IO}$            | —       | 1.5  | 4    | —      | 2    | 10   | mV            |
| $V_O = 2.5\text{ V}$                                  |                     |         |      |      |        |      |      |               |
| Input Offset Current                                  | $I_{IO}$            | —       | 0.1  | 5    | —      | 0.1  | 10   | pA            |
| $V_O = 2.5\text{ V}$                                  |                     |         |      |      |        |      |      |               |
| Input Current   | $I_I$               | —       | 2    | 10   | —      | 2    | 15   |               |
| $V_O = 2.5\text{ V}$                                  |                     |         |      |      |        |      |      |               |
| Common-Mode Rejection Ratio                           | $C_{MRR}$           | 75      | 87   | —    | 70     | 80   | —    | dB            |
| $V_{CM} = 0\text{ to }1\text{ V}$                     |                     |         |      |      |        |      |      |               |
| $V_{CM} = 0\text{ to }2.5\text{ V}$                   | $C_{MRR}$           | 60      | 69   | —    | 60     | 69   | —    |               |
| Input Common-Mode Voltage Range                       | $V_{ICR}^+$         | 2.5     | 2.8  | —    | 2.5    | 2.8  | —    | V             |
|   | $V_{ICR}^-$         | —       | -0.5 | 0    | —      | -0.5 | 0    |               |
| Power-Supply Rejection Ratio                          | $PSRR$              | 60      | 75   | —    | 55     | 67   | —    | dB            |
| $\Delta V^+ = 1\text{ V}$ ; $\Delta V^- = 1\text{ V}$ |                     |         |      |      |        |      |      |               |
| Large-Signal Voltage Gain*                            | $A_{OL}$            |         |      |      |        |      |      |               |
| $V_O = 0.1\text{ to }4.1\text{ V}$                    | $R_L = \infty$      | 100     | 117  | —    | 95     | 117  | —    |               |
| $V_O = 0.1\text{ to }3.6\text{ V}$                    | $R_L = 10\text{ k}$ | 90      | 102  | —    | 85     | 102  | —    |               |
| Source Current  | $I_{SOURCE}$        | 1.0     | 3.1  | 4.0  | 1.0    | 2.2  | 4.0  | mA            |
| $V_O = 0\text{ V}$                                    |                     |         |      |      |        |      |      |               |
| Sink Current  | $I_{SINK}$          | 1.0     | 1.6  | 4.0  | 1.0    | 3.4  | 4.0  |               |
| $V_O = 5\text{ V}$                                    |                     |         |      |      |        |      |      |               |
| Output Voltage  | $V_{OUT}$           |         |      |      |        |      |      | V             |
| $R_L = \infty$  | $V_{OM}^+$          | 4.99    | 5    | —    | 4.99   | 5    | —    |               |
|   | $V_{OM}^-$          | —       | 0    | 0.01 | —      | 0    | 0.01 |               |
| $R_L = 10\text{ k}$                                   | $V_{OM}^+$          | 4.4     | 4.7  | —    | 4.4    | 4.7  | —    |               |
|   | $V_{OM}^-$          | —       | 0    | 0.01 | —      | 0    | 0.01 |               |
| $R_L = 2\text{ k}$                                    | $V_{OM}^+$          | 2.5     | 3.3  | —    | 2.5    | 3.3  | —    |               |
|   | $V_{OM}^-$          | —       | 0    | 0.01 | —      | 0    | 0.01 |               |
| Supply Current  | $I_{SUPPLY}$        | —       | 50   | 100  | —      | 50   | 100  | $\mu\text{A}$ |
| $V_O = 0\text{ V}$                                    |                     |         |      |      |        |      |      |               |
| $V_O = 2.5\text{ V}$                                  | $I_{SUPPLY}$        | —       | 320  | 400  | —      | 320  | 400  |               |

\*For  $V^+ = 4.5\text{ V}$  and  $V^- = \text{GND}$ ;  $V_{OUT} = 0.5\text{ V}$  to  $3.2\text{ V}$  at  $R_L = 10\text{ k}$

**3**  
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## CA5160A, CA5160

**ELECTRICAL CHARACTERISTICS** at  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$

| CHARACTERISTIC  | LIMITS              |      |      |        |      |      | UNITS |               |
|---|---------------------|------|------|--------|------|------|-------|---------------|
|   | CA5160A             |      |      | CA5160 |      |      |       |               |
|   | Min.                | Typ. | Max. | Min.   | Typ. | Max. |       |               |
| Input Offset Voltage<br>$V_O = 2.5\text{ V}$                  | $V_{IO}$            | —    | 2    | 10     | —    | 3    | 15    | mV            |
| Input Offset Current<br>$V_O = 2.5\text{ V}$                  | $I_{IO}$            | —    | 0.1  | 5      | —    | 0.1  | 10    | nA            |
| Input Current<br>$V_O = 2.5\text{ V}$                         | $I_I$               | —    | 2    | 10     | —    | 2    | 15    |               |
| Common-Mode Rejection Ratio<br>$V_{CM} = 0$ to $1\text{ V}$   | $C_{MRR}$           | 60   | 80   | —      | 60   | 80   | —     | dB            |
| $V_{CM} = 0$ to $2.5\text{ V}$                                | $C_{MRR}$           | 55   | 80   | —      | 50   | 75   | —     |               |
| Input Common-Mode Voltage Range                               |                     |      |      |        |      |      |       | V             |
|   | $V_{ICR}^+$         | 2.5  | 2.8  | —      | 2.5  | 2.8  | —     |               |
|   | $V_{ICR}^-$         | —    | -0.5 | 0      | —    | -0.5 | 0     |               |
| Power-Supply Rejection Ratio<br>$\Delta^+ = V^+ = 2\text{ V}$ | $P_{SRR}$           | 45   | 65   | —      | 40   | 60   | —     | dB            |
| Large-Signal Voltage Gain*<br>$V_O = 0.1$ to $4.1\text{ V}$   | $A_{OL}$            |      |      |        |      |      |       |               |
| $V_O = 0.1$ to $3.6\text{ V}$                                 | $R_L = \infty$      | 94   | 110  | —      | 90   | 110  | —     |               |
|   | $R_L = 10\text{ k}$ | 80   | 100  | —      | 75   | 100  | —     |               |
| Source Current<br>$V_O = 0\text{ V}$                          | $I_{SOURCE}$        | 0.6  | 2.2  | 5.0    | 0.6  | —    | 5.0   | mA            |
| Sink Current<br>$V_O = 5\text{ V}$                            | $I_{SINK}$          | 0.6  | 1.15 | 5.0    | 0.6  | —    | 5.0   |               |
| Output Voltage<br>$R_L = \infty$                              | $V_{OUT}$           |      |      |        |      |      |       | V             |
|   | $V_{OM}^+$          | 4.99 | 5    | —      | 4.99 | 5    | —     |               |
|   | $V_{OM}^-$          | —    | 0    | 0.01   | —    | 0    | 0.01  |               |
| $R_L = 10\text{ k}$   | $V_{OM}^+$          | 4.0  | 4.3  | —      | 4.0  | 4.3  | —     |               |
|   | $V_{OM}^-$          | —    | 0    | 0.01   | —    | 0    | 0.01  |               |
| $R_L = 2\text{ k}$  | $V_{OM}^+$          | 2.0  | 2.5  | —      | 2.0  | 2.5  | —     |               |
|   | $V_{OM}^-$          | —    | 0    | 0.01   | —    | 0    | 0.01  |               |
| Supply Current<br>$V_O = 0\text{ V}$                          | $I_{SUPPLY}$        | —    | 170  | 220    | —    | 170  | 220   | $\mu\text{A}$ |
| $V_O = 2.5\text{ V}$  | $I_{SUPPLY}$        | —    | 410  | 500    | —    | 410  | 500   |               |

\*For  $V^+ = 4.5\text{ V}$  and  $V^- = \text{GND}$ ;  $V_{OUT} = 0.5\text{ V}$  to  $3.2\text{ V}$  at  $R_L = 10\text{ k}$

## CA5160A, CA5160

**ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $V^+ = 15\text{V}$ ,  $V^- = 0\text{V}$  (Unless Otherwise Specified)**

| CHARACTERISTIC  |                | LIMITS         |            |       |        |            |       | UNITS                        |            |
|---|----------------|----------------|------------|-------|--------|------------|-------|------------------------------|------------|
|   |                | CA5160A        |            |       | CA5160 |            |       |                              |            |
|   |                | Min.           | Typ.       | Max.  | Min.   | Typ.       | Max.  |                              |            |
| Input Offset Voltage<br>$V^\pm = \pm 7.5\text{V}$                                       | $ V_{IO} $     | —              | 2          | 5     | —      | 6          | 15    | mV                           |            |
| Input Offset Current<br>$V^\pm = \pm 7.5\text{V}$                                       | $ I_{IO} $     | —              | 0.5        | 20    | —      | 0.5        | 30    | pA                           |            |
| Input Current<br>$V^\pm = \pm 7.5\text{V}$  | $I_I$          | —              | 5          | 30    | —      | 5          | 50    | pA                           |            |
| Large-Signal Voltage Gain<br>$V_O = 10 V_{p-p}$ , $R_L = 2\text{k}\Omega$               | $A_{OL}$       | 50k            | 320k       | —     | 50k    | 320k       | —     | V/V                          |            |
|   |                | 94             | 110        | —     | 94     | 110        | —     | dB                           |            |
| Common-Mode Rejection Ratio   | $C_{MRR}$      | 80             | 95         | —     | 70     | 90         | —     | dB                           |            |
| Common-Mode Input Voltage Range   | $V_{ICR}$      | 10             | -0.5 to 12 | 0     | 10     | -0.5 to 12 | 0     | V                            |            |
| Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^\pm$<br>$V^\pm = \pm 7.5\text{V}$ | $P_{SRR}$      | —              | 32         | 150   | —      | 32         | 320   | $\mu\text{V}/\text{V}$       |            |
| Maximum Output Voltage<br>$R_L = 2\text{k}\Omega$                                       | $V_{OM}^+$     | 12             | 13.3       | —     | 12     | 13.3       | —     | V                            |            |
|   |                | $V_{OM}^-$     | —          | 0.002 | 0.01   | —          | 0.002 |                              | 0.01       |
|   | $R_L = \infty$ | $V_{OM}^+$     | 14.99      | 15    | —      | 14.99      | 15    |                              | —          |
|   |                | $V_{OM}^-$     | —          | 0     | 0.01   | —          | 0     |                              | 0.1        |
| Maximum Output Current  | $I_{OM}^+$     | 12             | 22         | 45    | 12     | 22         | 45    | mA                           |            |
|   |                |                |            |       |        |            |       |                              | $I_{OM}^-$ |
| Supply Current<br>$V_O = 7.5\text{V}$   | $I^+$          | $R_L = \infty$ | —          | 10    | 15     | —          | 10    | 15                           | mA         |
|   |                |                |            |       |        |            |       |                              |            |
| Input Offset Voltage Temp. Drift,<br>$\Delta V_{IO}/\Delta T$                           |                | —              | 6          | —     | —      | 8          | —     | $\mu\text{V}/^\circ\text{C}$ |            |

## CA5160A, CA5160

### TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

| CHARACTERISTIC                            | TEST CONDITIONS   |  | CA5160/<br>CA5160A        | UNITS      |
|---|---|--|---------------------------|------------|
|   | $V^+ = +7.5\text{ V}$<br>$V^- = -7.5\text{ V}$<br>$T_A = 25^\circ\text{ C}$<br>(Unless Otherwise Specified) |  |                           |            |
| Input Offset Voltage Adjustment Range     | 10 k $\Omega$ across Terms 4 and 5 or 4 and 1   |  | $\pm 22$                  | mV         |
| Input Resistance                          | $R_i$   |  | 1.5                       | T $\Omega$ |
| Input Capacitance                         | $C_i$   | $f = 1\text{ MHz}$   | 4.3                       | pF         |
| Equivalent Input Noise Voltage            | $e_n$   | BW = 0.2 MHz   | $R_s = 1\text{ M}\Omega$  | 40         |
|   |   |  | $R_s = 10\text{ M}\Omega$ | 50         |
| Equivalent Input Noise Voltage            | $e_n$   | $R_s = 100\ \Omega$  | 1 kHz                     | 72         |
|   |   |  | 10 kHz                    | 30         |
| Unity Gain Crossover Frequency            | $f_T$   |  | 4                         | MHz        |
| Slew Rate                                 | SR:   |  | 10                        | V/ $\mu$ s |
| Transient Response:                       | $t_r$   | $C_L = 25\text{ pF}$<br>$R_L = 2\text{ k}\Omega$<br>(Voltage Follower) | 0.09                      | $\mu$ s    |
|   |   |  | 10                        | %          |
| Setting Time (4 $V_{p-p}$ Input to <0.1%) |   |  | 1.8                       | $\mu$ s    |

### CIRCUIT DESCRIPTION

Fig. 3 is a block diagram of the CA5160 series CMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA5160 series circuits are ideal for single-supply operation. Three class A amplifier stages, having the individual gain capability and current consumption shown in Fig. 3, provide the total gain of the CA5160. A biasing circuit provides two potentials for common use in the first and second stages. Terminals 8 and 1 can be used to supplement the internal phase compensation network if additional phase compensation or frequency roll-off is desired. Terminals 8 and 4 can also be used to strobe the output stage into a low quiescent current state. When Terminal 8 is tied to the negative supply rail (Terminal 4) by mechanical or electrical means, the output potential at Ter-

minal 6 essentially rises to the positive supply-rail potential at Terminal 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive CMOS digital circuits in comparator applications).

**Input Stages** — The circuit of the CA5160 is shown in Fig. 2. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terminals 1 and 5 and the potentiometer slider arm to Terminal 4.

## CA5160A, CA5160

Cascode-connected PMOS transistors Q2, Q4, are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D7 provide gate-oxide protection against high-voltage transients, e.g., including static electricity during handling for Q6 and Q7.

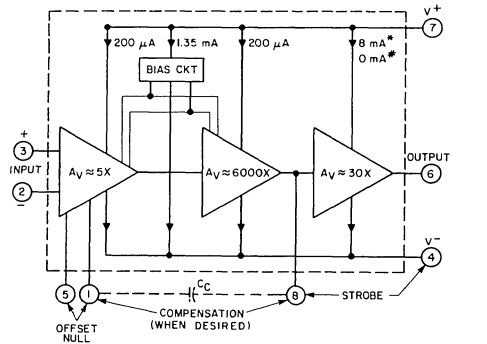
**Second-State** — Most of the voltage gain in the CA5160 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is described later. Miller Effect compensation (roll off) is accomplished by means of the 30-pf capacitor and 2-k $\Omega$  resistor connected between the base and collector of transistor Q11. These internal components provide sufficient compensation for unity gain operation in most applications. However, additional compensation, if desired, may be used between Terminals 1 and 8.

**Bias-Source Circuit** — At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Terminal 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Terminal 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected" to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes non-conductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply

voltages below about 4.5 volts results in seriously degraded performance.

**Output Stage** — The output stage consists of a drain-loaded inverting amplifier using CMOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig. 6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.



TOTAL SUPPLY VOLTAGE (FOR INDICATED VOLTAGE GAINS) +15 V  
 \* WITH INPUT TERMINALS BIASED SO THAT TERM 6 POTENTIAL IS +7.5 V ABOVE TERM 4  
 \* WITH OUTPUT TERMINAL DRIVEN TO EITHER SUPPLY RAIL

Fig. 3 — Block diagram of the CA5160 Series.

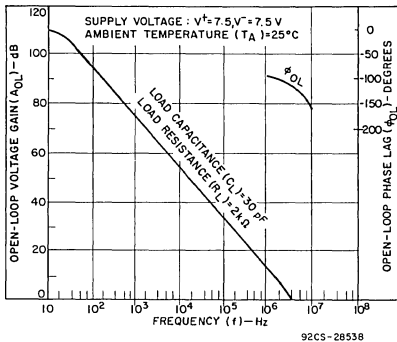


Fig. 4 — Open-loop voltage gain and phase shift vs. frequency.

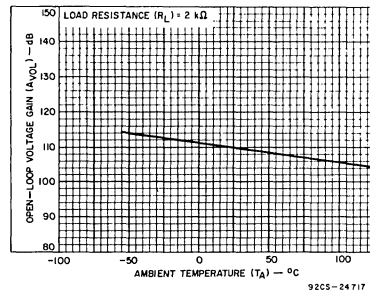


Fig. 5 — Open-loop gain vs. temperature.

# CA5160A, CA5160

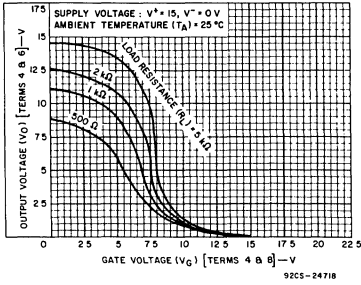


Fig. 6 — Voltage transfer characteristics of CMOS output stage.

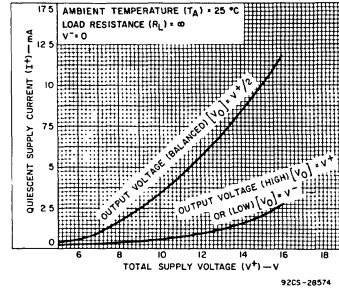


Fig. 7 — Quiescent supply current vs. supply voltage.

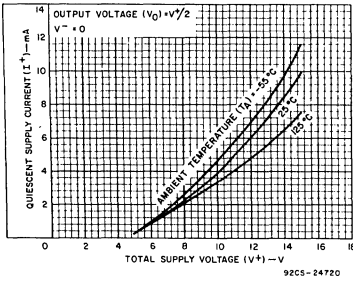


Fig. 8 — Quiescent supply current vs. supply voltage at several temperatures.

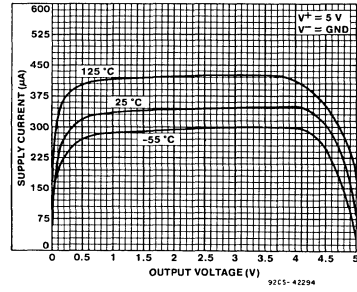


Fig. 9 — Supply current vs. output voltage.

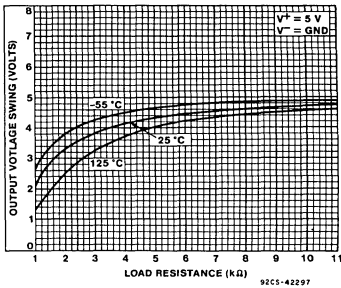


Fig. 10 — Output voltage swing vs. load resistance.

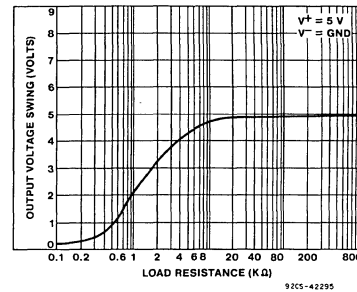


Fig. 11 — Output swing vs. load resistance.

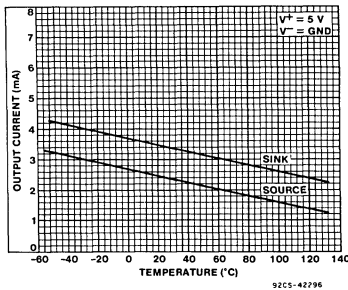


Fig. 12 — Output current vs. temperature.

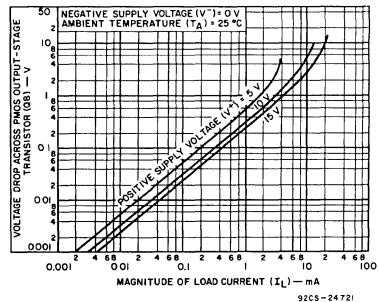


Fig. 13 — Voltage across PMOS output transistor (Q8) vs. load current.

# CA5160A, CA5160

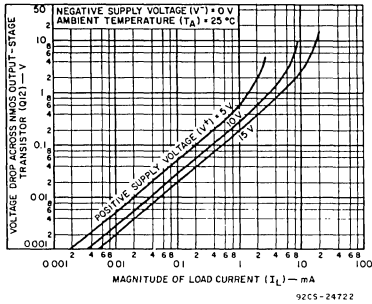


Fig. 14 — Voltage across NMOS output transistor (Q12) vs. load current.

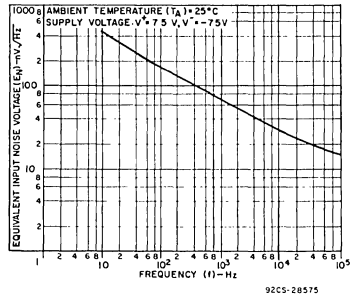


Fig. 15 — Equivalent noise voltage vs. frequency.

### Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terminals 1 and 5 and with the potentiometer slider arm connected to Terminal 4. A fine offset-null adjustment usually can be affected with the slider arm positioned in the mid-point of the potentiometer's total range.

### Input Current Variation with Common-Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA5160 Series Op-Amps is typically 5 pA at  $T_A = 25^\circ\text{C}$  when Terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Fig. 16 contains data showing the variation of input

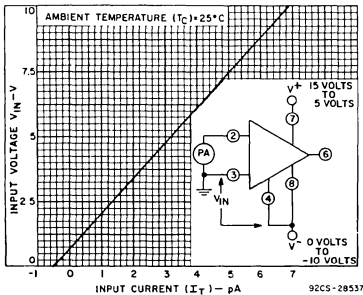


Fig. 16 — CA5160 input current vs. common-mode voltage.

current as a function of common-mode input voltage at  $T_A = 25^\circ\text{C}$ . These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1 pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA5160 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

### Input-Current Variation with Temperature

The input current of the CA5160 Series circuits is typically 5

pA at  $25^\circ\text{C}$ . The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every  $10^\circ\text{C}$  increase in temperature. Fig. 17 provides data on the typical variation of input bias current as a function of temperature in the CA5160.

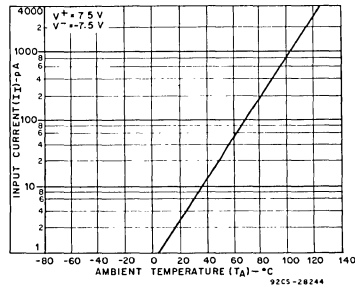


Fig. 17 — Input current vs. ambient temperature.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA5160. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

### Input-Offset-Voltage ( $V_{IO}$ ) Variation with DC Bias vs. Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA5160 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terminals 2 and 3. Fig. 18 shows typical data pertinent to shifts in offset voltage encountered with CA5160 devices in TO-5 packages during life testing. At lower temperatures (TO-5 and plastic) for example at  $85^\circ\text{C}$ , this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an oper-

3  
OPERATIONAL  
AMPLIFIERS

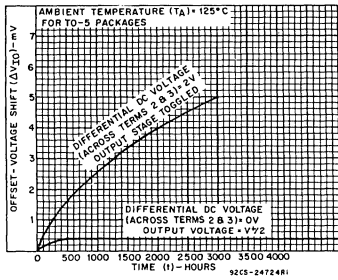


Fig. 18 — Typical incremental offset-voltage shift vs. operating life.

ational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output state is “toggled”, e.g., as in comparator applications.

**Power-Supply Considerations**

Because the CA5160, is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single- and dual-supply service. Figs. 19 (a) and 19 (b) show the CA5160 connected for both dual- and single-supply operation.

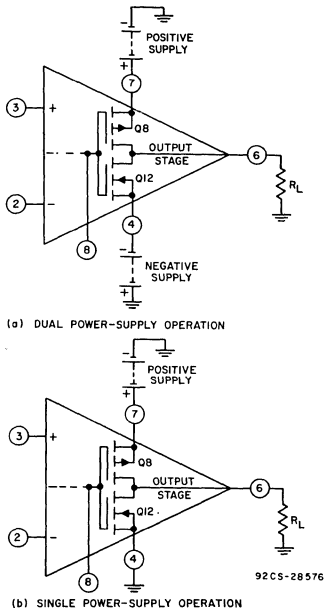


Fig. 19 — CA5160 output stage in dual and single power-supply operation

Dual-supply operation: When the output voltage at Terminal 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive

supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single-supply operation: Initially, let it be assumed that the value of  $R_L$  is very high (or disconnected), and that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is at  $V/2$ , i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA5160 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cutoff (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Terminal 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA5160, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 15(a) shows a dual-supply arrangement for the output stage that can also be strobed off, assuming  $R_L = \infty$ , by pulling the potential of Terminal 8 down to that of Terminal 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Terminal 6 and ground in the circuit of Fig. 19(b). Let it further be assumed again that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is  $V/2$ . Since PMOS transistor Q8 must now supply quiescent current to both  $R_L$  and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the  $R_L$  magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

**Wideband Noise**

From the standpoint of low-noise performance considerations, the use of the CA5160 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 40  $\mu V$  when the test-circuit amplifier of Fig. 20 is operated at a total supply

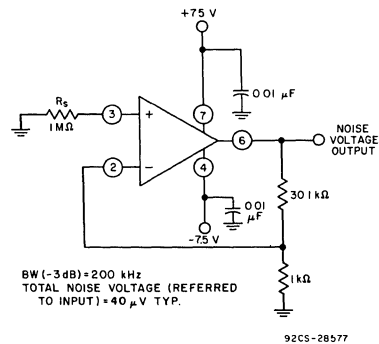


Fig. 20 — CA5160 Test-circuit amplifier (30-dB gain) used for wideband noise measurements.

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voltage of 15 volts. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

### TYPICAL APPLICATIONS

#### Voltage Followers

Operational amplifiers with very high input resistances, like the CA5160, are particularly suited to service as voltage followers. Fig. 21 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA5160 in a split-supply configuration.

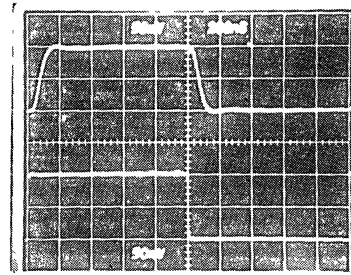
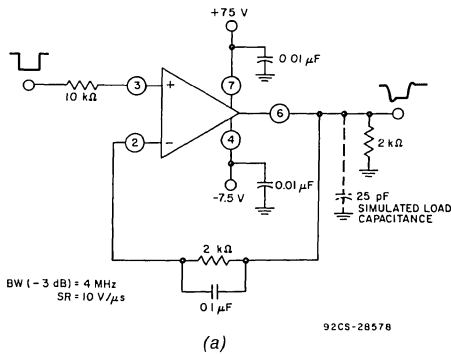
A voltage follower, operated from a single-supply, is shown in Fig. 22 together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig. 22b with input-signal ramping. The waveforms in Fig. 22c show that the fol-

lower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig. 22c also shows the manner in which the CMOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA5160 in a single-supply voltage-follower application.

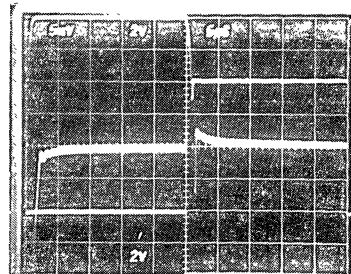
#### 9-Bit CMOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)\* is shown in Fig. 23. This system combines the concepts of multiple-switch CMOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA5160 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig. 23.

\*"Digital-to-Analog Conversion Using the Harris CD4007A CMOS IC", Application Note ICAN-6080.



(b) Small Signal Response  
Top Trace: Output  
Bottom Trace: Input

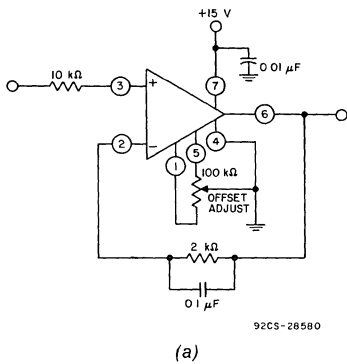


(c) Input-Output Difference Signal Showing  
Setting Time  
Top Trace: Output Signal  
Center Trace: Difference Signal 5 mV/div  
Bottom Trace: Input Signal

Fig. 21 — Split-supply voltage follower with associated waveforms for CA5160.

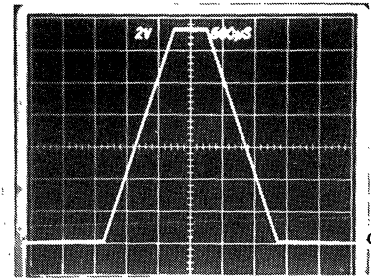


# CA5160A, CA5160

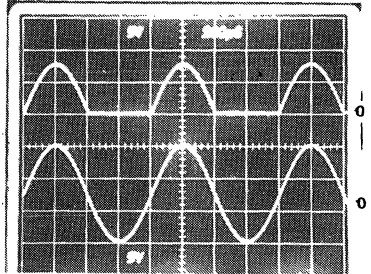


(a)

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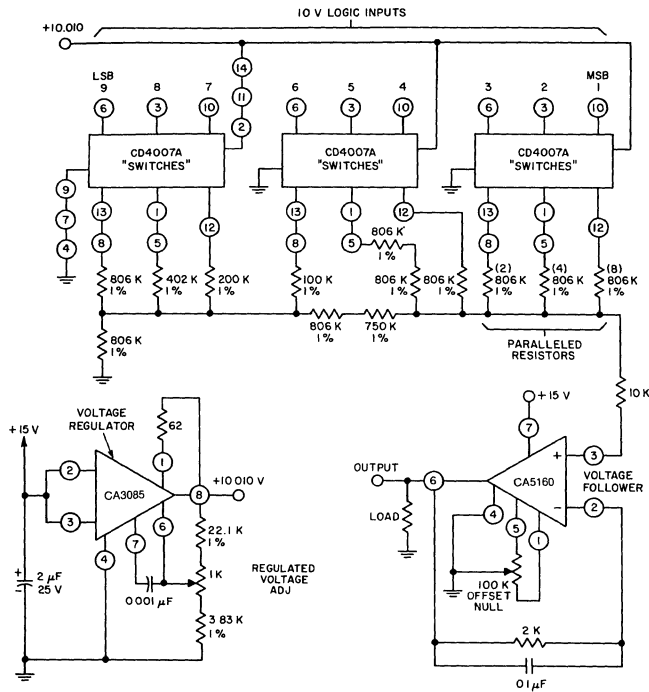
(b) Output signal with input-signal ramping.



(c) Output-Waveform with Ground-Reference Sine-Wave Input  
Top Trace: Output  
Bottom Trace: Input

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Fig. 22 — CA5160 Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig. 9 in ICAN-6080.)



92CM-28582

Fig. 23 — 9-bit DAC using CMOS digital switches and CA5160.

## CA5160A, CA5160

The circuit uses an R/2R voltage-ladder network, with the output-potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA5160 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the CMOS building blocks simplifies the design of DAC systems tai-

lored to particular needs.

### Error-Amplifier in Regulated Power Supplies

The CA5160 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero.

The circuit shown in Fig. 24 uses a CA5160 as an error amplifier in a continuously adjustable 1-ampere power supply. One of the key features of this circuit is its ability to regulate down to the vicinity of zero volts with only one dc power supply input.

An RC network, connected between the base of the output drive transistor and the input voltage, prevents "turn-on overshoot", a condition typical of many operational-amplifier regulator circuits. As the amplifier becomes operational, this RC network ceases to have any influence on the regulator performance.

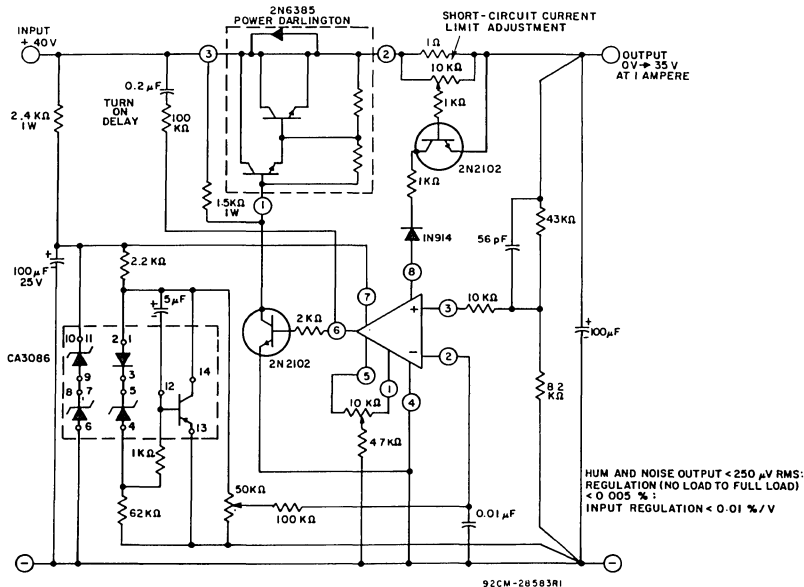


Fig. 24 — CA5160 Voltage regulator circuit (0.1 to 35 V at 1 A).

### Precision Voltage-Controlled Oscillator

The circuit diagram of a precision voltage-controlled oscillator is shown in Fig. 25. The oscillator operates with a tracking error in the order of 0.02 percent and a temperature coefficient of 0.01%/°C. A multivibrator ( $A_1$ ) generates pulses of constant amplitude ( $V$ ) and width ( $T_2$ ). Since the output (terminal 6) of  $A_1$  (a CA5130) can swing within about 10 millivolts of either supply-rail, the output pulse amplitude ( $V$ ) is essentially equal to  $V^+$ . The average output voltage ( $E_{avg} = V T_2/T_1$ ) is applied to the non-inverting input terminal of comparator  $A_2$  (a CA5160) via an integrating network  $R_3, C_2$ . Comparator  $A_2$  operates to establish circuit conditions such that  $E_{avg} = V_1$ . This circuit condition is accomplished by feeding an output signal from terminal 6 of  $A_2$  through  $R_4, D_4$  to the inverting terminal (terminal 2) of  $A_1$ , thereby adjusting

the multivibrator interval,  $T_3$ .

### Voltmeter With High Input Resistance

The voltmeter circuit shown in Fig. 26 illustrates an application in which a number of the CA5160 characteristics are exploited. Range-switch SW1 is ganged between input and output circuitry to permit selection of the proper output voltage for feedback to Terminal 2 via 10 K $\Omega$  current-limiting resistor. The circuit is powered by a single 8.4-volt mercury battery. With zero input signal, the circuit consumes somewhat less than 500 microamperes plus the meter current required to indicate a given voltage. Thus, at full-scale input, the total supply current rises to slightly more than 1500 microamperes.

# CA5160A, CA5160

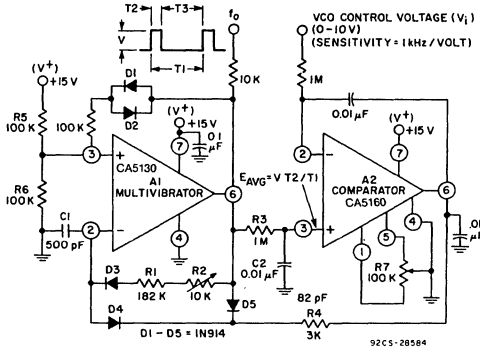


Fig. 25 — Voltage-controlled oscillator.

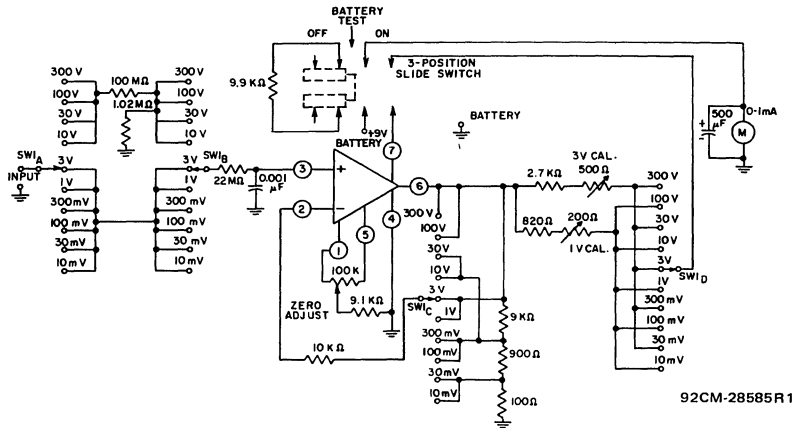


Fig. 26 — CA5160A high-input-resistance DC voltmeter

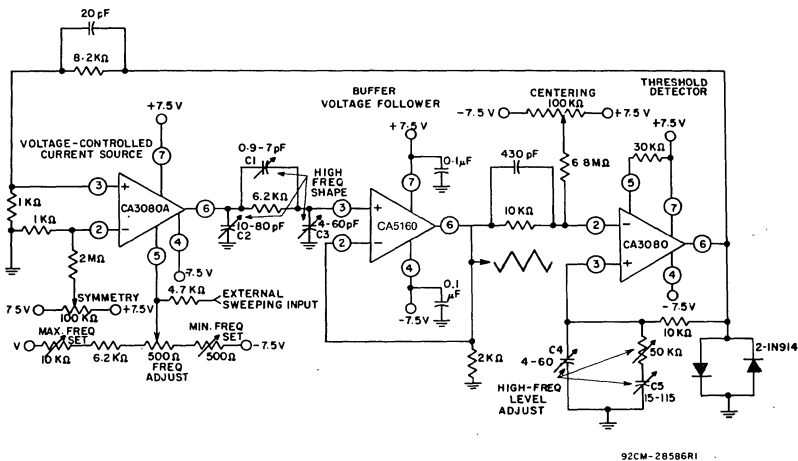


Fig. 27(a) — CA5160 1,000,000/1 single-control function generator — 1 MHz to 1 Hz.

## CA5160A, CA5160

### Function Generator

A function generator having a wide tuning range is shown in Fig. 27. The adjustment range, in excess of 1,000,000/1, is accomplished by a single potentiometer. Three operational amplifiers are utilized: a CA5160 as a voltage follower, a CA3080 as a high-speed comparator, and a second CA3080A

as a programmable current source. Three variable capacitors C1, C2, and C3 shape the triangular signal between 500 kHz and 1 MHz. Capacitors C4, C5 and the trimmer potentiometer in series with C5 maintain essentially constant ( $\pm 10\%$ ) amplitude up to 1 MHz.

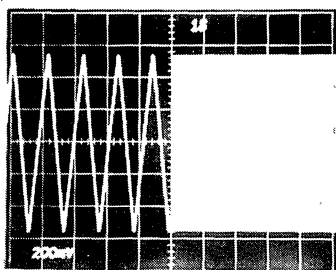
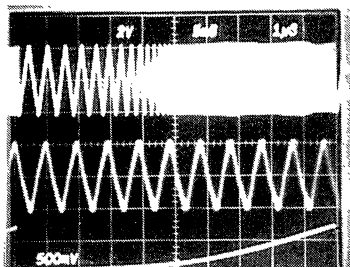


Fig. 27(b) — Two-tone output signal from the function generator. A square-wave signal modulates the external sweeping input to produce 1 Hz and 1 MHz, showing the 1,000,000/1 frequency range of the function generator.



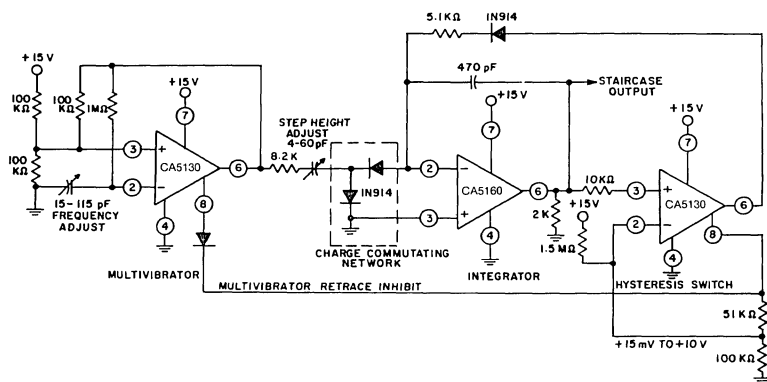
92CS-28588

Fig. 27(c) — Triple-trace of the function generator sweeping to 1 MHz. The bottom trace is the sweeping signal and the top trace is the actual generator output. The center trace displays the 1 MHz signal via delayed oscilloscope triggering of the upper swept output signal.

### Staircase Generator

Fig. 28 shows a staircase generator circuit utilizing three CMOS operational amplifiers. Two CA5130's are used; one

as a multivibrator, the other as a hysteresis switch. The third amplifier, a CA5160, is used as a linear staircase generator.



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Fig. 28(a) — Staircase generator circuit utilizing three CMOS operational amplifiers.

### Picoammeter Circuit

Fig. 29 is a current-to-voltage converter configuration utilizing a CA5160 and CA3140 to provide a picoampere meter for  $\pm 3$  pA full-scale meter deflection. By placing Terminals 2 and 4 of the CA5160 at ground potential, the CA5160 input is operated in the "guarded mode". Under this operating condition, even slight leakage resistance present between Terminals 3 and 2 or between Terminals 3 and 4 would result in zero voltage across this leakage resistance, thus substantially reducing the leakage current.

If the CA5160 is operated with the same voltage on input Terminals 3 and 2 as on Terminal 4, a further reduction in the input current to the less than one picoampere level can be achieved as shown in Fig. 16.

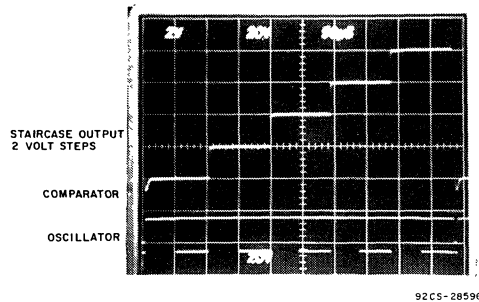
To further enhance the stability of this circuit, the CA5160 can be operated with its output (Terminal 6) near ground, thus markedly reducing the dissipation by reducing the supply current to the device.

The CA3140 stage serves as a X100 gain stage to provide the required plus and minus output swing for the meter and

## CA5160A, CA5160

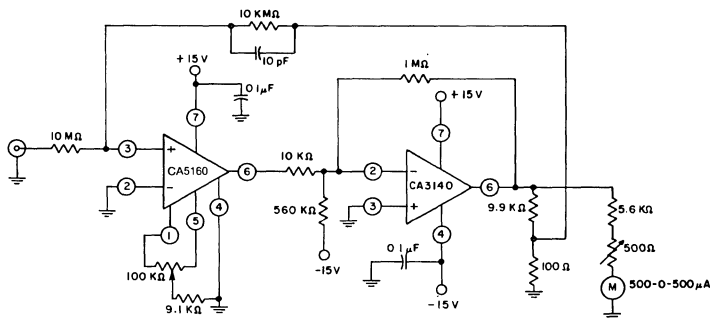
feedback network. A 100-to-1 voltage divider network consisting of a 9.9-K $\Omega$  resistor in series with a 100-ohm resistor sets the voltage at the 10-KM $\Omega$  resistor (in series with Terminal 3) to  $\pm 30$  mV full-scale deflection. This 30-mV signal results from  $\pm 3$  volts appearing at the top of the voltage divider network which also drives the meter circuitry.

By utilizing a switching technique in the meter circuit and in the 9.9 K $\Omega$  and 100-ohm network similar to that used in voltmeter circuit shown in Fig. 26, a current range of 3 pA to 1 nA full scale can be handled with the single 10-KM $\Omega$  resistor.



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Fig. 28 (b) — Staircase Generator Waveform  
Top Trace: Staircase Output  
2 Volt Steps  
Center Trace: Comparator  
Bottom Trace: Oscillator



92CM-28589R1

Fig. 29 — Current-to-voltage converter to provide a picoammeter with  $\pm 3$  pA full-scale deflection.

### Single-Supply Sample-and-Hold System

Fig. 30 shows a single-supply sample-and-hold system using a CA5160 to provide a high input impedance and an input-voltage range of 0 to 10 volts. The output from the input buffer integrator network is coupled to a CA3080A. The CA3080A functions as a strobeable current source for the CA3140 output integrator and storage capacitor. The CA3140 was chosen because of its low output impedance and constant gain-bandwidth product. Pulse "droop" during the hold

interval can be reduced to zero by adjusting the 100-K $\Omega$  bias-voltage potentiometer on the positive input of the CA3140. This zero adjustment sets the CA3080A output voltage at its zero current position. In this sample-and-hold circuit it is essential that the amplifier bias current be reduced to zero to minimize output signal current during the hold mode. Even with 320 mV at the amplifier bias circuit terminal (5) at least  $\pm 100$  pA of output current will be available.

## CA5160A, CA5160

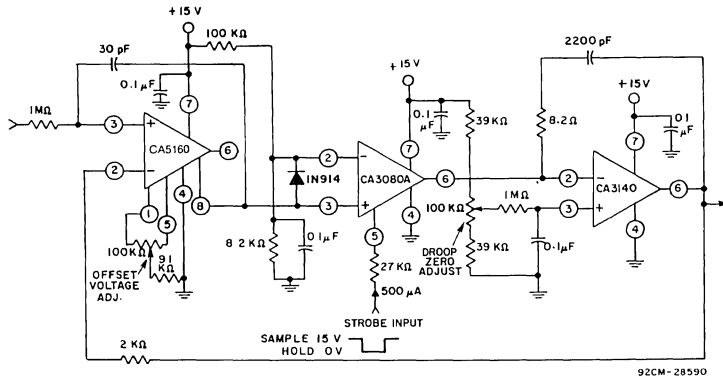
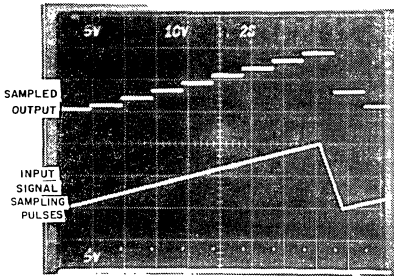
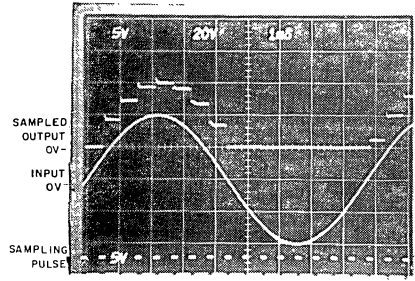


Fig. 30(a) — Single-supply sample-and-hold system—  
input 0-to-10 volts.



(b) — Sample-and-hold waveform.  
Top Trace: Sampled Output  
Center Trace: Input Signal  
Bottom Trace: Sampling Pulses



(c) — Sample-and-hold waveform.  
Top Trace: Sampled Output  
Center Trace: Input  
Bottom Trace: Sampling Pulse

### Wien Bridge Oscillator

A simple, single-supply Wien Bridge oscillator using a CA5160 is shown in Fig. 31. A pair of parallel-connected 1N914 diodes comprise the gain-setting network which standardizes the output voltage at approximately 1.1 volts.

The 500-ohm potentiometer is adjusted so that the oscillator will always start and the oscillation will be maintained. Increasing the amplitude of the voltage may lower the threshold level for starting and for sustaining the oscillation, but will introduce more distortion.

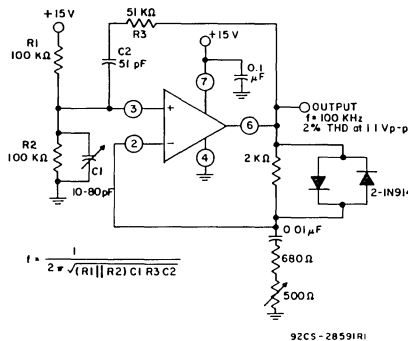


Fig. 31 — CA5160 Single-supply Wien Bridge oscillator.

## CA5160A, CA5160

### Operation with Output-Stage Power-Booster

The current sourcing and sinking capability of the CA5160 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig. 32, three CMOS transistor-pairs in a single CA3600 IC array are shown parallel-connected with the output stage in the CA5160. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of

supply current at 15-V operation. This arrangement boosts the current-handling capability of the CA5160 output stage by about 2.5X.

The amplifier circuit in Fig. 32 employs feedback to establish a closed-loop gain of 20 dB. The typical large-signal-bandwidth (-3 dB) is 190 kHz.

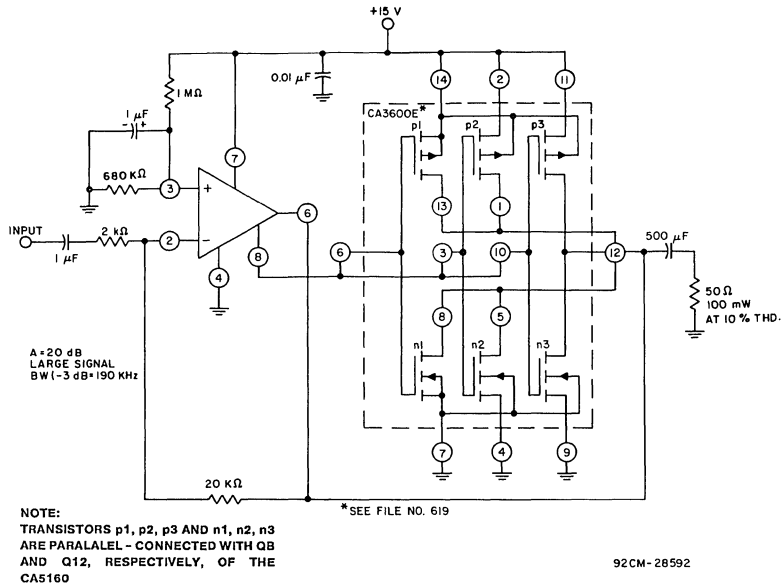


Fig. 32 — CMOS transistor array (CA3600E) connected as power booster in the output stage of the CA5160.

August 1991

### Features

- MOSFET Input Stage
  - ▶ Very High  $Z_i$  ..... 1.5T $\Omega$  (1.5 x 10<sup>12</sup> $\Omega$ ) Typ.
  - ▶ Very Low  $I_i$  ..... 5pA Typ. at 15V Operation  
2pA Typ. at 5V Operation
- Ideal for Single-Supply Applications
- Common-Mode Input Voltage Range Includes Negative Supply Rail; Input Terminals Can Be Swung 0.5V Below Negative Supply Rail
- CMOS Output Stage Permits Signal Swing to Either (or Both) Supply Rails
- CA5260A, CA5260 Have Full Military Temperature Range Guaranteed Specifications  $V_+ = 5V$
- CA5260A, CA5260 Are Guaranteed to Operate Down to 4.5V for AQL
- Fully guaranteed to operate at -55°C to +125°C at  $V_+ = 5V$ ,  $V_- = Gnd$

### Applications

- Ground Referenced Single Supply Amplifiers
- Fast Sample-Hold Amplifiers
- Long Duration Timers/Monostables
- Ideal Interface With Digital CMOS
- High Input Impedance Wideband Amplifiers
- Voltage Followers (e.g. Follower for Single Supply D/A Converter)
- Voltage Regulators (Permits Control of Output Voltage Down to Zero Volts)
- Wien-Bridge Oscillators
- Voltage Controlled Oscillators
- Photo Diode Sensor Amplifiers
- 5V Logic Systems
- Microprocessor Interface

### Description

The CA5260A and CA5260 are integrated-circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. The CA5260 series circuits are dual versions of the popular CA5160 series. They are designed and guaranteed to operate in microprocessor or logic systems that use +5V supplies.

Gate-protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5V below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10mV of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

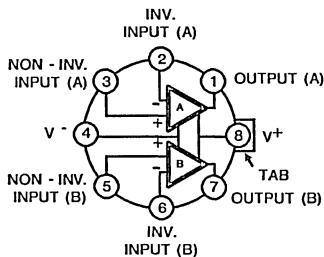
The CA5260 Series circuits operate at supply voltages ranging from 4.5V to 16V, or  $\pm 2.25V$  to  $\pm 8V$  when using split supplies.

The CA5260 Series is supplied in standard 8-lead TO-5 style packages (T suffix) and 8-lead dual-in-line formed lead TO-5 style "DIL-CAN" packages (S suffix). The CA5260 is available in chip form (H suffix). Both devices are also available in 8-lead Mini-DIP (E suffix) and 8-lead Small Outline (M suffix) packages.

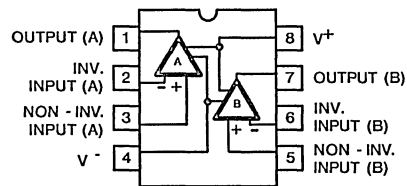
The CA5260A, CA5260 have guaranteed specifications for 5V operation over the full military-temperature range of -55°C to +125°C.

### Pinouts

S AND T SUFFIXES  
TOP VIEW



E AND M SUFFIXES  
TOP VIEW



NOTE: Pin compatible with the industry standard 1458

FIGURE 1.



## CA5260A, CA5260

### MAXIMUM RATINGS, Absolute-Maximum Values

|  |  |
|--|--|
| DC SUPPLY VOLTAGE<br>(Between V <sup>+</sup> and V <sup>-</sup> Terminals) ..... | 16 V   |
| DIFFERENTIAL-MODE INPUT VOLTAGE .....  | ±8 V   |
| COMMON-MODE DC INPUT VOLTAGE .....   | (V <sup>+</sup> +8V) to (V <sup>-</sup> -0.5V) |
| INPUT-TERMINAL CURRENT .....   | 1 mA   |
| DEVICE DISSIPATION:  |  |
| WITHOUT HEAT SINK -  |  |
| UP TO 55°C .....   | 630 mW   |
| ABOVE 55°C .....   | Derate Linearly 6.67 mW/°C                     |
| WITH HEAT SINK -   |  |
| UP TO 90°C .....   | 1 W  |
| ABOVE 90°C .....   | Derate Linearly 16.7 mW/°C                     |
| SMALL OUTLINE PACKAGE .....  | 250°/W   |
| TEMPERATURE RANGE:   |  |
| OPERATING (all types) .....  | -55 to +125°C                                  |
| STORAGE (all types) .....  | -65 to +150°C                                  |
| OUTPUT SHORT-CIRCUIT DURATION * .....  | INDEFINITE                                     |
| LEAD TEMPERATURE (DURING SOLDERING):   |  |
| At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. .... | +265°C   |

\* Short circuit may be applied to ground or to either supply.

### TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

V<sup>+</sup> = 5 V, V<sup>-</sup> = 0 V, T<sub>A</sub> = 25°C (Unless Otherwise Specified)

| CHARACTERISTIC                                     | TEST CONDITIONS | TYPICAL VALUES  |        | UNITS |      |
|--|-----------------|---|--------|-------|------|
|  |                 | CA5260A   | CA5260 |       |      |
| Input Resistance                                   | R <sub>i</sub>  | 1.5   | 1.5    | TΩ    |      |
| Input Capacitance                                  | C <sub>i</sub>  | f = 1 MHz   | 4.3    | 4.3   | pF   |
| Unity Gain Crossover Frequency                     | f <sub>t</sub>  | 3   | 3      | MHz   |      |
| Slew Rate  | SR              | V <sub>OUT</sub> = 2.5V <sub>P-P</sub>                                | 5      | 5     | V/μs |
| Transient Response:                                | t <sub>r</sub>  | C <sub>L</sub> = 25 pF<br>R <sub>L</sub> = 2 kΩ<br>(Voltage Follower) |        |       |      |
| Rise Time  |                 |   | 0.09   | 0.09  | μs   |
| Overshoot  |                 |   | 10     | 10    | %    |
| Settling Time (4 V <sub>P-P</sub> Input to < 0.1%) |                 |   | 1.8    | 1.8   | μs   |

## CA5260A, CA5260

**ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$**

| CHARACTERISTIC  |                                     | LIMITS       |      |      |        |      |      | UNITS |      |
|---|-------------------------------------|--------------|------|------|--------|------|------|-------|------|
|   |                                     | CA5260A      |      |      | CA5260 |      |      |       |      |
|   |                                     | MIN.         | TYP. | MAX. | MIN.   | TYP. | MAX. |       |      |
| Input Offset Voltage<br>$V_O = 2.5\text{ V}$                                      | $V_{IO}$                            | —            | 1.5  | 4    | —      | 2    | 15   | mV    |      |
| Input Offset Current<br>$V_O = 2.5\text{ V}$                                      | $I_{IO}$                            | —            | 1    | 10   | —      | 1    | 10   | pA    |      |
| Input Current<br>$V_O = 2.5\text{ V}$   | $I_I$                               | —            | 2    | 15   | —      | 2    | 15   |       |      |
| Common-Mode Rejection Ratio<br>$V_{CM} = 0\text{ to }1\text{ V}$                  | $C_{MRR}$                           | 80           | 85   | —    | 70     | 85   | —    | dB    |      |
|   | $V_{CM} = 0\text{ to }2.5\text{ V}$ | $C_{MRR}$    | 50   | 55   | —      | 50   | 55   |       | —    |
| Input Common-Mode Voltage Range   | $V_{ICR}^+$                         | 2.5          | 3    | —    | 2.5    | 3    | —    | V     |      |
|   | $V_{ICR}^-$                         | —            | -0.5 | 0    | —      | -0.5 | 0    |       |      |
| Power-Supply Rejection Ratio<br>$\Delta^+ = 1\text{ V}$ ; $\Delta^- = 1\text{ V}$ | $P_{SRR}$                           | 75           | 84   | —    | 70     | 84   | —    | dB    |      |
| Large-Signal Voltage Gain*<br>$V_O = 0.5\text{ to }4\text{ V}$                    | $A_{OL}$                            |              |      |      |        |      |      |       |      |
|   | $R_L = \infty$                      | 107          | 113  | —    | 105    | 111  | —    |       |      |
| $V_O = 0.5\text{ to }3.6\text{ V}$  | $R_L = 10\text{ k}$                 | 83           | 86   | —    | 80     | 86   | —    |       |      |
| Source Current<br>$V_O = 0\text{ V}$  | $I_{SOURCE}$                        | 1.75         | 2.2  | —    | 1.75   | 2.2  | —    | mA    |      |
| Sink Current<br>$V_O = 5\text{ V}$  | $I_{SINK}$                          | 1.70         | 2    | —    | 1.70   | 2    | —    |       |      |
| Output Voltage<br>$R_L = \infty$  | $V_{OUT}$                           |              |      |      |        |      |      | V     |      |
|   | $V_{OM}^+$                          | 4.99         | 5    | —    | 4.99   | 5    | —    |       |      |
|   | $V_{OM}^-$                          | —            | 0    | 0.01 | —      | 0    | 0.01 |       |      |
|   | $R_L = 10\text{ k}$                 | $V_{OM}^+$   | 4.4  | 4.7  | —      | 4.4  | 4.7  |       | —    |
|   |                                     | $V_{OM}^-$   | —    | 0    | 0.01   | —    | 0    |       | 0.01 |
|   | $R_L = 2\text{ k}$                  | $V_{OM}^+$   | 3    | 3.4  | —      | 3    | 3.4  |       | —    |
| $V_{OM}^-$  |                                     | —            | 0    | 0.01 | —      | 0    | 0.01 |       |      |
| Supply Current<br>$V_O = 0\text{ V}$  | $I_{SUPPLY}$                        | —            | 1.60 | 2.0  | —      | 1.60 | 2.0  | mA    |      |
|   | $V_O = 2.5\text{ V}$                | $I_{SUPPLY}$ | —    | 1.80 | 2.25   | —    | 1.80 |       | 2.25 |

\*For  $V^+ = 4.5\text{ V}$  and  $V^- = \text{Gnd}$ ;  $V_{OUT} = 0.5\text{ V to }3.2\text{ V}$  at  $R_L = 10\text{ k}$ .

**3**  
OPERATIONAL  
AMPLIFIERS

## CA5260A, CA5260

**ELECTRICAL CHARACTERISTICS AT  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$**

| CHARACTERISTIC  |                            | LIMITS  |      |      |        |      |      | UNITS |
|---|----------------------------|---------|------|------|--------|------|------|-------|
|   |                            | CA5260A |      |      | CA5260 |      |      |       |
|   |                            | MIN.    | TYP. | MAX. | MIN.   | TYP. | MAX. |       |
| Input Offset Voltage<br>$V_O = 2.5\text{ V}$                                      | $V_{IO}$                   | —       | 2    | 15   | —      | 3    | 20   | mV    |
| Input Offset Current<br>$V_O = 2.5\text{ V}$                                      | $I_{IO}$                   | —       | 1    | 10   | —      | 1    | 10   | nA    |
| Input Current<br>$V_O = 2.5\text{ V}$   | $I_I$                      | —       | 2    | 15   | —      | 2    | 15   |       |
| Common-Mode Rejection Ratio<br>$V_{CM} = 0$ to $1\text{ V}$                       | $C_{MRR}$                  | 65      | 78   | —    | 60     | 78   | —    | dB    |
| $V_{CM} = 0$ to $2.5\text{ V}$  | $C_{MRR}$                  | 50      | 60   | —    | 50     | 60   | —    |       |
| Input Common-Mode Voltage Range   | $V_{ICR}^+$                | 2.5     | 3    | —    | 2.5    | 3    | —    | V     |
|   | $V_{ICR}^-$                | —       | -0.5 | 0    | —      | -0.5 | 0    |       |
| Power-Supply Rejection Ratio<br>$\Delta^+ = 1\text{ V}$ ; $\Delta^- = 1\text{ V}$ | $P_{SRR}$                  | 62      | 65   | —    | 60     | 65   | —    | dB    |
| Large-Signal Voltage Gain*<br>$V_O = 0.5$ to $4\text{ V}$                         | $A_{OL}$<br>$R_L = \infty$ | 70      | 78   | —    | 70     | 78   | —    |       |
| $V_O = 0.5$ to $3.6\text{ V}$   | $R_L = 10\text{ k}$        | 60      | 65   | —    | 60     | 65   | —    |       |
| Source Current<br>$V_O = 0\text{ V}$  | $I_{SOURCE}$               | 1.3     | 1.6  | —    | 1.3    | 1.6  | —    | mA    |
| Sink Current<br>$V_O = 5\text{ V}$  | $I_{SINK}$                 | 1.2     | 1.4  | —    | 1.2    | 1.4  | —    |       |
| Output Voltage<br>$R_L = \infty$  | $V_{OUT}$<br>$V_{OM}^+$    | 4.99    | 5    | —    | 4.99   | 5    | —    | V     |
|   | $V_{OM}^-$                 | —       | 0    | 0.01 | —      | 0    | 0.01 |       |
| $R_L = 10\text{ k}$   | $V_{OM}^+$                 | 4.2     | 4.4  | —    | 4.2    | 4.4  | —    |       |
|   | $V_{OM}^-$                 | —       | 0    | 0.01 | —      | 0    | 0.01 |       |
| $R_L = 2\text{ k}$  | $V_{OM}^+$                 | 2.5     | 2.7  | —    | 2.5    | 2.7  | —    |       |
|   | $V_{OM}^-$                 | —       | 0    | 0.01 | —      | 0    | 0.01 |       |
| Supply Current<br>$V_O = 0\text{ V}$  | $I_{SUPPLY}$               | —       | 1.65 | 2.2  | —      | 1.65 | 2.2  | mA    |
| $V_O = 2.5\text{ V}$  | $I_{SUPPLY}$               | —       | 1.95 | 2.35 | —      | 1.95 | 2.35 |       |

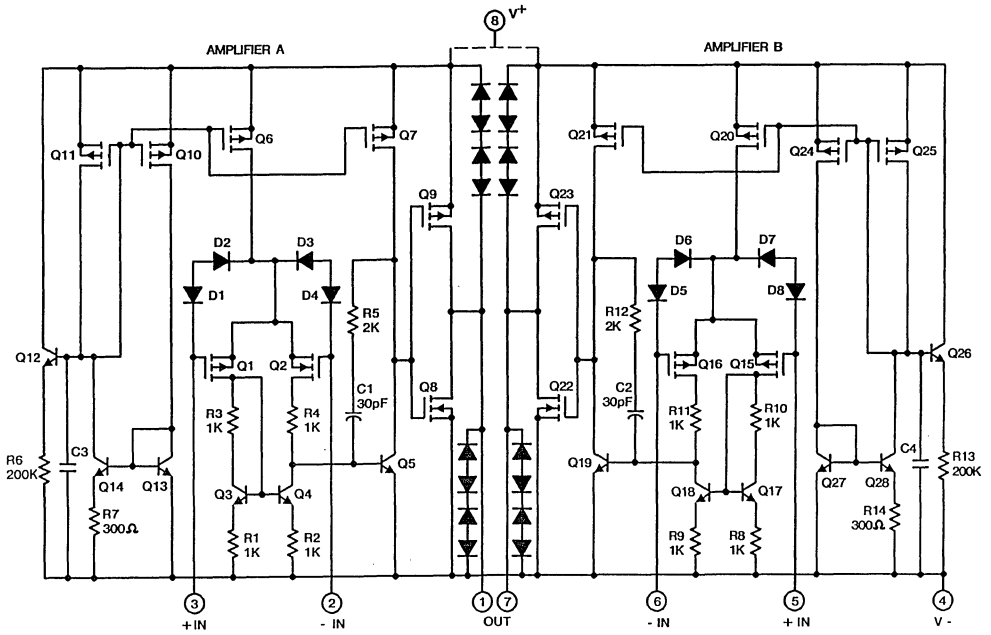
\*For  $V^+ = 4.5\text{ V}$  and  $V^- = \text{Gnd}$ ;  $V_{OUT} = 0.5\text{ V}$  to  $3.2\text{ V}$  at  $R_L = 10\text{ k}$ .

## CA5260A, CA5260

**ELECTRICAL CHARACTERISTICS for Each Amplifier at  $T_A = 25^\circ\text{C}$ ,  $V^+ = 15\text{ V}$ ,  $V^- = 0\text{ V}$  (Unless otherwise specified)**

| CHARACTERISTIC   |  | LIMITS                                   |  |       |        |       |       | UNITS                        |     |      |
|--|--|--|--|-------|--------|-------|-------|------------------------------|-----|------|
|  |  | CA5260A                                  |  |       | CA5260 |       |       |                              |     |      |
|  |  | MIN.                                     | TYP.   | MAX.  | MIN.   | TYP.  | MAX.  |                              |     |      |
| Input Offset Voltage   | $V_{IO}$                                   | —  | 2  | 5     | —      | 6     | 15    | mV                           |     |      |
| $V_{\pm} = \pm 7.5\text{ V}$                                 |  |  |  |       |        |       |       |                              |     |      |
| Input Offset Current   | $I_{IO}$                                   | —  | 0.5  | 20    | —      | 0.5   | 30    | pA                           |     |      |
| $V_{\pm} = \pm 7.5\text{ V}$                                 |  |  |  |       |        |       |       |                              |     |      |
| Input Current  | $I_I$                                      | —  | 5  | 30    | —      | 5     | 50    | pA                           |     |      |
| $V_{\pm} = \pm 7.5\text{ V}$                                 |  |  |  |       |        |       |       |                              |     |      |
| Large-Signal Voltage Gain                                    | $A_{OL}$                                   | 50 k                                     | 320 k  | —     | 50 k   | 320 k | —     | V/V                          |     |      |
|  |  | 94                                       | 110  | —     | 94     | 110   | —     | dB                           |     |      |
| $V_O = 10\text{ V}_{P-P}$ , $R_L = 10\text{ k}\Omega$        |  |  |  |       |        |       |       |                              |     |      |
| Common-Mode Rejection Ratio                                  | $C_{MRR}$                                  | 80                                       | 95   | —     | 70     | 90    | —     | dB                           |     |      |
| Common-Mode Input Voltage Range                              | $V_{ICR}$                                  | 10                                       | -0.5   | 0     | 10     | -0.5  | 0     | V                            |     |      |
|  |  |  | to   |       | to     |       | to    |                              |     |      |
| $V_{\pm} = \pm 7.5\text{ V}$                                 |  |  |  |       |        |       |       |                              |     |      |
| Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V_{\pm}$ | $P_{SRR}$                                  | —  | 32   | 150   | —      | 32    | 320   | $\mu\text{V/V}$              |     |      |
| $V_{\pm} = \pm 7.5\text{ V}$                                 |  |  |  |       |        |       |       |                              |     |      |
| Maximum Output Voltage:                                      | At $R_L = 10\text{ k}\Omega$               | $V_{OM}^+$                               | 11   | 13.3  | —      | 11    | 13.3  | —                            |     |      |
|  |  | $V_{OM}^-$                               | —  | 0.002 | 0.01   | —     | 0.002 | 0.01                         |     |      |
|  | At $R_L = \infty$                          | $V_{OM}^+$                               | 14.99  | 15    | —      | 14.99 | 15    | —                            |     |      |
|  |  | $V_{OM}^-$                               | —  | 0     | 0.01   | —     | 0     | 0.01                         |     |      |
|  |  |  |  |       |        |       |       | V                            |     |      |
| Maximum Output Current                                       | $I_{OM}^+$ (Source) @ $V_O = 7.5\text{ V}$ | 12                                       | 22   | 45    | 12     | 22    | 45    | mA                           |     |      |
|  |  | 12                                       | 20   | 45    | 12     | 20    | 45    |                              |     |      |
|  |  | $I_{OM}^-$ (Sink) @ $V_O = 7.5\text{ V}$ |  |       |        |       |       |                              |     |      |
| Total Supply Current   | $I^+$                                      | $R_L = \infty$                           | $V_O$ (Ampli. A) = $V_O$ (Ampli. B) = 7.5 V      |       | —      | 9     | 16.5  | —                            | 9   | 16.5 |
|  |  |  | $V_O$ (Ampli. A) = $V_O$ (Ampli. B) = 0 V        |       | —      | 1.2   | 4     | —                            | 1.2 | 4    |
|  |  |  | $V_O$ (Ampli. A) = 0 V, $V_O$ (Ampli. B) = 7.5 V |       | —      | 5     | 9.5   | —                            | 5   | 9.5  |
|  |  |  |  |       |        |       |       |                              |     |      |
| Input Offset Voltage Temp. Drift                             | $\Delta V_{IO}/\Delta T$                   | —  | 6  | —     | —      | 8     | —     | $\mu\text{V}/^\circ\text{C}$ |     |      |
| $V_{\pm} = \pm 7.5\text{ V}$                                 |  |  |  |       |        |       |       |                              |     |      |
| Crosstalk $f = 1\text{ kHz}$                                 |  | —  | 120  | —     | —      | 120   | —     | dB                           |     |      |

# CA5260A, CA5260



August 1991

**3**  
 OPERATIONAL  
 AMPLIFIERS

### Features

- CA5420A, CA5420 at 5V Supply Voltage With Full Military Temperature Range Guaranteed Specifications
- 5420A, CA5420 Guaranteed to Operate From  $\pm 1V$  to  $\pm 10V$  Supplies
- 2V Supply at 300 $\mu A$  Supply Current
- 1pA (Typ.) Input Current (Essentially Constant to +85°C)
- Rail-to-Rail Output Swing (Drive  $\pm 2mA$  Into 1k $\Omega$  Load)
- Pin Compatible With 741 Op Amp

### Applications

- pH Probe Amplifiers
- Picoammeters
- Electrometer (High Z) Instruments
- Portable Equipment
- Inaccessible Field Equipment
- Battery Dependent Equipment (Medical and Military)
- 5V Logic Systems
- Microprocessor Interface

### Description

The CA5420A and CA5420\* are integrated circuit operational amplifiers that combine PMOS transistors and bipolar transistors on a single monolithic chip. They are designed and guaranteed to operate in microprocessor logic systems that use  $V+ = 5V$ ,  $V- = Gnd$ , since they can operate down to  $\pm 1V$  supplies. They will also be suitable for 3.3V logic systems.

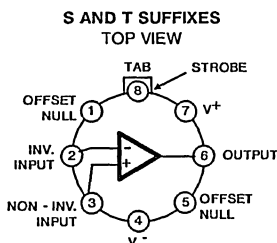
The CA5420A and CA5420 BiMOS operational amplifiers feature gate-protected PMOS transistors in the input circuit to provide very high input impedance, very low input currents (less than 1pA). The internal bootstrapping network features a unique guardbanding technique for reducing the doubling of leakage current for every 10°C increase in temperature. The CA5420 series operates at total supply voltages from 2V to 20V either single or dual supply. These operational amplifiers are internally phase compensated to achieve stable operation in the unity gain follower configuration. Additionally, they have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS in the input stage results in common-mode input voltage capability down to 0.45V below the negative supply terminal, an important attribute for single supply application. The output stage uses a feedback OTA-type amplifier that can swing essentially from rail-to-rail. The output driving current of 1.0mA (min) is provided by using non-linear current mirrors.

These devices have guaranteed specifications for 5V operation over the full military temperature range of -55°C to +125°C.

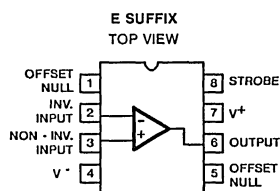
The CA5420 series has the same 8-lead pin-out used for the industry standard 741. They are supplied in the standard 8-lead TO-5 style package (S suffix, and T suffix); in the standard 8-lead dual-in-line plastic package (Mini-DIP - E suffix), and are also available in chip form (H suffix).

\*Formerly Dev. Type No. TA10841

### Pinouts



NOTE: Pin 4 is connected to Case



### Block Diagram

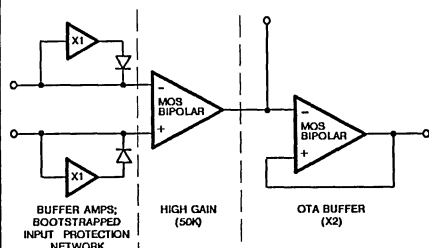


FIGURE 1.

## CA5420A, CA5420

### MAXIMUM RATINGS, Absolute-Maximum Values ( $T_c = 25^\circ\text{C}$ ):

|   |   |
|---|---|
| DC SUPPLY VOLTAGE (BETWEEN $V^+$ AND $V^-$ TERMINALS)                         | 22 V                                      |
| DIFFERENTIAL-MODE INPUT VOLTAGE   | $\pm 15$ V                                |
| COMMON-MODE DC INPUT VOLTAGE  | ( $V^+ + 8$ V) to ( $V^- - 0.5$ V)        |
| INPUT-TERMINAL CURRENT  | 1 mA                                      |
| DEVICE DISSIPATION:   |   |
| WITHOUT HEAT SINK   |   |
| Up to $55^\circ\text{C}$  | 630 mW                                    |
| Above $55^\circ\text{C}$  | Derate linearly 6.67 mW/ $^\circ\text{C}$ |
| WITH HEAT SINK  |   |
| Up to $110^\circ\text{C}$   | 630 mW                                    |
| Above $110^\circ\text{C}$   | Derate linearly 16.7 mW/ $^\circ\text{C}$ |
| TEMPERATURE RANGE:  |   |
| OPERATING (ALL TYPES)   | $-55$ to $+125^\circ\text{C}$             |
| STORAGE (ALL TYPES)   | $-65$ to $+150^\circ\text{C}$             |
| OUTPUT SHORT-CIRCUIT DURATION*  | Indefinite                                |
| LEAD TEMPERATURE (DURING SOLDERING):  |   |
| At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s max. | $+265^\circ\text{C}$                      |

\*Short circuit may be applied to ground or to either supply.

### TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

| CHARACTERISTIC               | TEST CONDITIONS  |                            | CA5420A<br>(T,S,E) | CA5420<br>(T,S,E) | UNITS                        |
|------------------------------|--|----------------------------|--------------------|-------------------|------------------------------|
|                              | $V^+ = +5\text{V}; V^- = \text{Gnd}$<br>$T_A = 25^\circ\text{C}$ |                            |                    |                   |                              |
| Input Resistance $R_i$       |  |                            | 150                | 150               | $\text{T}\Omega$             |
| Input Capacitance $C_i$      |  |                            | 4.9                | 4.9               | pF                           |
| Output Resistance $R_o$      |  |                            | 300                | 300               | $\Omega$                     |
| Equivalent Input             | $f = 1$ kHz  | $R_s = 100\Omega$          | 62                 | 62                | $\text{nV}/\sqrt{\text{Hz}}$ |
| Noise Voltage $e_n$          | $f = 10$ kHz   |                            | 38                 | 38                |                              |
| Short-Circuit Current Source |  |                            |                    |                   | mA                           |
| Source $I_{OM}^+$            |  |                            | 2.6                | 2.6               |                              |
| To Opposite Supply           |  |                            |                    |                   | mA                           |
| Sink $I_{OM}^-$              |  |                            | 2.4                | 2.4               |                              |
| Gain-Bandwidth Product $f_T$ |  |                            | 0.5                | 0.5               | MHz                          |
| Slew Rate SR                 |  |                            | 0.5                | 0.5               | V/ $\mu\text{s}$             |
| Transient Response           |  |                            |                    |                   |                              |
| Rise Time, $t_r$             | $R_L = 2$ k $\Omega$<br>$C_L = 100$ pF                           |                            | 0.7                | 0.7               | $\mu\text{s}$                |
| Overshoot                    |  |                            | 15                 | 15                | %                            |
| Current from Terminal 8      |  |                            |                    |                   |                              |
| To $V^-$ $I_{g^+}$           |  |                            | 20                 | 20                | $\mu\text{A}$                |
| Current from Terminal 8      |  |                            |                    |                   |                              |
| To $V^+$ $I_{g^-}$           |  |                            | 2                  | 2                 | mA                           |
| Settling Time                | .01%   | $A_V = 1$ $2V_{p-p}$ Input | 8                  | 8                 | $\mu\text{s}$                |
|                              | .10%   | $A_V = 1$ $2V_{p-p}$ Input | 4.5                | 4.5               | $\mu\text{s}$                |

# CA5420A, CA5420

ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$

| CHARACTERISTIC  |                     | LIMITS     |      |      |        |      |      | UNITS         |      |
|---|---------------------|------------|------|------|--------|------|------|---------------|------|
|   |                     | CA5420A    |      |      | CA5420 |      |      |               |      |
|   |                     | Min.       | Typ. | Max. | Min.   | Typ. | Max. |               |      |
| Input Offset Voltage<br>$V_O = 2.5\text{ V}$  | $V_{IO}$            | —          | 1    | 5    | —      | 1.5  | 10   | mV            |      |
| Input Offset Current<br>$V_O = 2.5\text{ V}$  | $I_{IO}$            | —          | 0.02 | 0.5  | —      | 0.02 | 1    | pA            |      |
| Input Current<br>$V_O = 2.5\text{ V}$   | $I_I$               | —          | 0.02 | 1    | —      | 0.02 | 2    |               |      |
| Common-Mode Rejection Ratio<br>$V_{CM} = 0\text{ to }3.7\text{ V}$ ; $V_O = 2.5\text{ V}$ | $C_{MRR}$           | 75         | 83   | —    | 70     | 80   | —    | dB            |      |
| Input Common-Mode Voltage Range<br>$V_O = 2.5\text{ V}$                                   | $V_{ICR}^+$         | 3.7        | 4    | —    | 3.7    | 4    | —    | V             |      |
|   | $V_{ICR}^-$         | —          | -0.3 | 0    | —      | -0.3 | 0    |               |      |
| Power-Supply Rejection Ratio<br>$\Delta^+ = 1\text{ V}$ ; $\Delta^- = 1\text{ V}$         | $P_{SRR}$           | 75         | 83   | —    | 70     | 80   | —    | dB            |      |
| Large-Signal Voltage Gain<br>$V_O = 0.5\text{ to }4\text{ V}$                             | $A_{OL}$            | —          | —    | —    | —      | —    | —    |               |      |
|   | $R_L = \infty$      | 85         | 87   | —    | 85     | 87   | —    |               |      |
|   | $R_L = 10\text{ k}$ | 85         | 87   | —    | 85     | 87   | —    |               |      |
|   | $R_L = 2\text{ k}$  | 80         | 85   | —    | 80     | 85   | —    |               |      |
| Source Current<br>$V_O = 0\text{ V}$  | $I_{SOURCE}$        | 1.2        | 2.7  | —    | 1.2    | 2.7  | —    | mA            |      |
| Sink Current<br>$V_O = 5\text{ V}$  | $I_{SINK}$          | 1.2        | 2.1  | —    | 1.2    | 2.1  | —    |               |      |
| Output Voltage<br>$R_L = \infty$  | $V_{OUT}$           | —          | —    | —    | —      | —    | —    | V             |      |
|   | $V_{OM}^+$          | 4.9        | 4.94 | —    | 4.9    | 4.94 | —    |               |      |
|   | $V_{OM}^-$          | —          | 0.13 | 0.15 | —      | 0.13 | 0.15 |               |      |
|   | $R_L = 10\text{ k}$ | $V_{OM}^+$ | 4.7  | 4.9  | —      | 4.7  | 4.9  |               | —    |
|   |                     | $V_{OM}^-$ | —    | 0.12 | 0.15   | —    | 0.12 |               | 0.15 |
|   | $R_L = 2\text{ k}$  | $V_{OM}^+$ | 3.5  | 4.6  | —      | 3.5  | 4.6  |               | —    |
|   | $V_{OM}^-$          | —          | 0.1  | 0.15 | —      | 0.1  | 0.15 |               |      |
| Supply Current<br>$V_O = 0\text{ V}$  | $I_{SUPPLY}$        | —          | 400  | 500  | —      | 400  | 500  | $\mu\text{A}$ |      |
| $V_O = 2.5\text{ V}$  | $I_{SUPPLY}$        | —          | 430  | 550  | —      | 430  | 550  |               |      |

3

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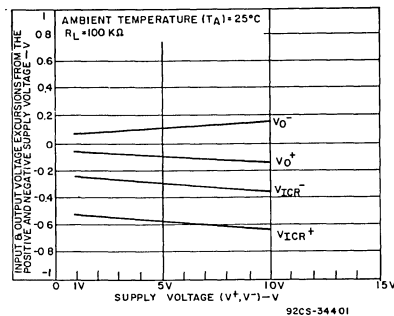


Fig. 2 - Output-voltage-swing and common-mode input-voltage range vs supply voltage.



# CA5420A, CA5420

**ELECTRICAL CHARACTERISTICS at  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V^+ = 5\text{ V}$ ,  $V^- = 0\text{ V}$**

| CHARACTERISTIC   |                    | LIMITS  |      |      |        |      |      | UNITS         |
|--|--------------------|---------|------|------|--------|------|------|---------------|
|  |                    | CA5420A |      |      | CA5420 |      |      |               |
|  |                    | Min.    | Typ. | Max. | Min.   | Typ. | Max. |               |
| Input Offset Voltage<br>$V_O = 2.5\text{ V}$   | $V_{IO}$           | —       | 2    | 10   | —      | 3    | 15   | mV            |
| Input Offset Current<br>$V_O = 2.5\text{ V}$ (Up to $T_A = 85^\circ\text{C}$ )   | $I_{IO}$           | —       | 1.5  | 3    | —      | 1.5  | 3    | nA            |
|  | $I_{IO}$           | —       | 2    | 10   | —      | 2    | 10   | pA            |
| Input Current<br>$V_O = 2.5\text{ V}$ (Up to $T_A = 85^\circ\text{C}$ )  | $ I_I $            | —       | 2    | 5    | —      | 2    | 5    | nA            |
|  | $ I_I $            | —       | 10   | 15   | —      | 15   | 25   | pA            |
| Common-Mode Rejection Ratio<br>$V_{CM} = 0$ to $3.7\text{ V}$ ; $V_O = 2.5\text{ V}$   | $C_{MRR}$          | 70      | 80   | —    | 65     | 75   | —    | dB            |
| Input Common-Mode Voltage Range<br>$V_O = 2.5\text{ V}$  | $V_{ICR}^+$        | 3.7     | 4    | —    | 3.7    | 4    | —    | V             |
|  | $V_{ICR}^-$        | —       | -0.3 | 0    | —      | -0.3 | 0    |               |
| Power-Supply Rejection Ratio<br>$\Delta^+ = 1\text{ V}$ ; $\Delta^- = 1\text{ V}$  | $P_{SRR}$          | 70      | 83   | —    | 65     | 80   | —    | dB            |
| Large-Signal Voltage Gain<br>$V_O = 0.5$ to $4\text{ V}$<br>$V_O = 0.7$ to $4\text{ V}$<br>$V_{OUT} = 0.7$ to $2.5\text{ V}$ | $A_{OL}$           | 85      | 87   | —    | 80     | 85   | —    | dB            |
|  | $R_L = \infty$     | 80      | 87   | —    | 80     | 85   | —    |               |
|  | $R_L = 10\text{k}$ | 75      | 80   | —    | 75     | 80   | —    |               |
|  | $R_L = 2\text{k}$  | 75      | 80   | —    | 75     | 80   | —    |               |
| Source Current<br>$V_O = 0\text{ V}$   | $I_{SOURCE}$       | 1       | 2.7  | —    | 1      | 2.7  | —    | mA            |
| Sink Current<br>$V_O = 5\text{ V}$   | $I_{SINK}$         | 1       | 2.1  | —    | 1      | 2.1  | —    | mA            |
| Output Voltage<br>$R_L = \infty$<br><br>$R_L = 10\text{k}$<br><br>$R_L = 2\text{k}$  | $V_{OUT}$          | 4.8     | 4.9  | —    | 4.8    | 4.9  | —    | V             |
|  | $V_{OM}^+$         | —       | 0.16 | 0.2  | —      | 0.16 | 0.2  |               |
|  | $V_{OM}^-$         | —       | 0.15 | 0.2  | —      | 0.15 | 0.20 |               |
|  | $V_{OM}^+$         | 3       | 4    | —    | 3      | 4    | —    |               |
|  | $V_{OM}^-$         | —       | 0.14 | 0.2  | —      | 0.14 | 0.2  |               |
|  | $V_{OM}^-$         | —       | 0.14 | 0.2  | —      | 0.14 | 0.2  |               |
| Supply Current<br>$V_O = 0\text{ V}$<br>$V_O = 2.5\text{ V}$   | $I_{SUPPLY}$       | —       | 430  | 550  | —      | 430  | 550  | $\mu\text{A}$ |
|  | $I_{SUPPLY}$       | —       | 480  | 600  | —      | 480  | 600  |               |

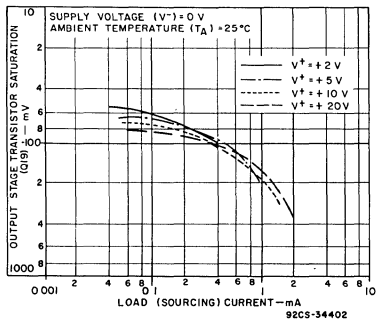


Fig. 3 - Output voltage vs load sourcing current.

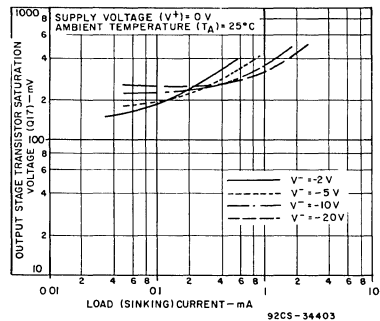


Fig. 4 - Output voltage vs load sinking current.

## CA5420A, CA5420

### ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At  $V^+ = 1\text{ V}$ ,  $V^- = -1\text{ V}$ ,  $T_A = 25^\circ\text{C}$  Unless Otherwise Specified

| CHARACTERISTIC   |                          | LIMITS  |       |      |        |       |      | UNITS                        |
|--|--------------------------|---------|-------|------|--------|-------|------|------------------------------|
|  |                          | CA5420A |       |      | CA5420 |       |      |                              |
|  |                          | Min.    | Typ.  | Max. | Min.   | Typ.  | Max. |                              |
| Input Offset Voltage                                     | $V_{IO}$                 | —       | 2     | 5    | —      | 5     | 10   | mV                           |
| Input Offset Current                                     | $ I_{IO} $               | —       | 0.01  | 4*   | —      | 0.01  | 4*   | pA                           |
| Input Current  | $ I_I $                  | —       | 0.02  | 5*   | —      | 0.02  | 5*   | pA                           |
| Large-Signal Voltage Gain<br>$R_L = 10\text{ k}\Omega$   | $A_{OL}$                 | 20k     | 100k  | —    | 10k    | 100k  | —    | V/V                          |
|  |                          | 86      | 100   | —    | 80     | 100   | —    | dB                           |
| Common-Mode Rejection Ratio                              | $C_{MRR}$                | —       | 560   | 1000 | —      | 560   | 1800 | $\mu\text{V/V}$              |
|  |                          | 60      | 65    | —    | 55     | 65    | —    | dB                           |
| Input Common-Mode Voltage Range                          | $V_{ICR}^+$              | 0.2     | 0.5   | —    | 0.2    | 0.5   | —    | V                            |
|  | $V_{ICR}^-$              | -1      | -1.3  | —    | —      | -1.3  | —    |                              |
| Power Supply Rejection Ratio<br>$\Delta V_{IO}/\Delta V$ | $P_{SRR}$                | —       | 32    | 320  | —      | 100   | 1000 | $\mu\text{V/V}$              |
|  |                          | 70      | 90    | —    | 60     | 80    | —    | dB                           |
| Maximum Output Voltage<br>$R_L = \infty$                 | $V_{OUT}$                | —       | —     | —    | —      | —     | —    | V                            |
|  | $V_{OM}^+$               | 0.9     | 0.95  | —    | 0.9    | 0.95  | —    |                              |
|  | $V_{OM}^-$               | -0.85   | -0.91 | —    | -0.85  | -0.91 | —    |                              |
| Supply Current   | $I_{SUPPLY}$             | —       | 350   | 650  | —      | 350   | 650  | $\mu\text{A}$                |
| Device Dissipation                                       | $P_D$                    | —       | 0.7   | 1.1  | —      | 0.7   | 1.1  | mW                           |
| Input Offset Voltage Temp. Drift                         | $\Delta V_{IO}/\Delta T$ | —       | 4     | —    | —      | 4     | —    | $\mu\text{V}/^\circ\text{C}$ |

\*The maximum limit represents the levels obtainable on high-speed automatic test equipment.

Typical values are obtained under laboratory conditions.

### ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At  $V^+ = 10\text{ V}$ ,  $V^- = -10\text{ V}$ ,  $T_A = 25^\circ\text{C}$  Unless Otherwise Specified

| CHARACTERISTIC   |                          | LIMITS  |       |      |        |       |      | UNITS                        |
|--|--------------------------|---------|-------|------|--------|-------|------|------------------------------|
|  |                          | CA5420A |       |      | CA5420 |       |      |                              |
|  |                          | Min.    | Typ.  | Max. | Min.   | Typ.  | Max. |                              |
| Input Offset Voltage                                     | $V_{IO}$                 | —       | 2     | 5    | —      | 5     | 10   | mV                           |
| Input Offset Current                                     | $ I_{IO} $               | —       | 0.03  | 4*   | —      | 0.03  | 4*   | pA                           |
| Input Current  | $ I_I $                  | —       | 0.05  | 5*   | —      | 0.05  | 5*   | pA                           |
| Large-Signal Voltage Gain<br>$R_L = 10\text{ k}\Omega$   | $A_{OL}$                 | 20k     | 100k  | —    | 10k    | 100k  | —    | V/V                          |
|  |                          | 86      | 100   | —    | 80     | 100   | —    | dB                           |
| Common-Mode Rejection Ratio                              | $C_{MRR}$                | —       | 100   | 320  | —      | 100   | 320  | $\mu\text{V/V}$              |
|  |                          | 70      | 80    | —    | 70     | 80    | —    | dB                           |
| Input Common-Mode Voltage Range                          | $V_{ICR}^+$              | 9       | 9.3   | —    | 8.5    | 9.3   | —    | V                            |
|  | $V_{ICR}^-$              | -10     | -10.3 | —    | -10    | -10.3 | —    |                              |
| Power Supply Rejection Ratio<br>$\Delta V_{IO}/\Delta V$ | $P_{SRR}$                | —       | 32    | 320  | —      | 32    | 320  | $\mu\text{V/V}$              |
|  |                          | 70      | 90    | —    | 70     | 90    | —    | dB                           |
| Maximum Output Voltage<br>$R_L = \infty$                 | $V_{OUT}$                | —       | —     | —    | —      | —     | —    | V                            |
|  | $V_{OM}^+$               | 9.7     | 9.9   | —    | 9.7    | 9.9   | —    |                              |
|  | $V_{OM}^-$               | -9.7    | -9.85 | —    | -9.7   | -9.85 | —    |                              |
| Supply Current   | $I_{SUPPLY}$             | —       | 450   | 1000 | —      | 450   | 1000 | $\mu\text{A}$                |
| Device Dissipation                                       | $P_D$                    | —       | 9     | 14   | —      | 9     | 14   | mW                           |
| Input Offset Voltage Temp. Drift                         | $\Delta V_{IO}/\Delta T$ | —       | 4     | —    | —      | 4     | —    | $\mu\text{V}/^\circ\text{C}$ |

\*The maximum limit represents the levels obtainable on high-speed automatic test equipment.

Typical values are obtained under laboratory conditions.

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# CA5420A, CA5420

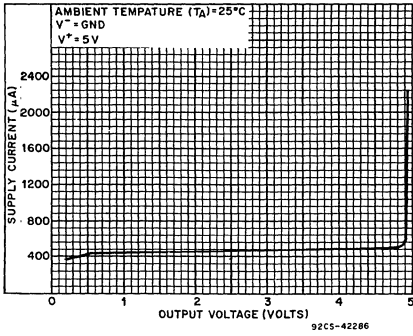


Fig. 5 - Supply current vs output voltage.

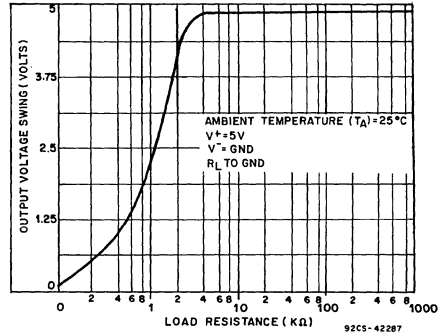


Fig. 6 - Output voltage swing vs load resistance.

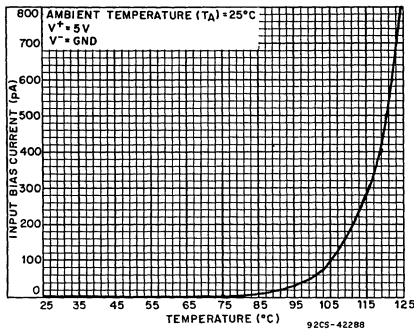


Fig. 7 - Input bias current drift ( $\Delta I_B/\Delta T$ ).

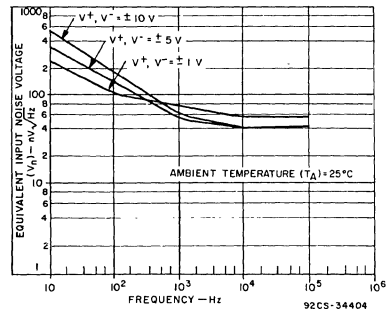


Fig. 8 - Input noise voltage vs frequency.

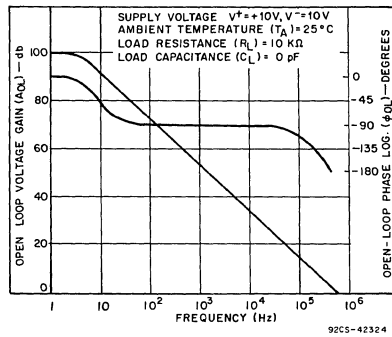


Fig. 9 - Open-loop gain and phase-shift response.

# CA5420A, CA5420

## APPLICATION CIRCUITS

### Picoammeter Circuit

The exceptionally low input current (typically 0.2 pA) makes the CA5420 highly suited for use in a picoammeter circuit. With only a single 10K-megohm resistor, this circuit covers the range from  $\pm 1.5$  pA. Higher current ranges are possible with suitable switching techniques and current scaling resistors. Input transient protection is provided by the 1-megohm resistor in series with the input. Higher current ranges require that this resistor be reduced. The 10-megohm resistor connected to pin 2 of the CA5420 decouples the potentially high input capacitance often associated with lower current circuits and reduces the tendency for the circuit to oscillate under these conditions.

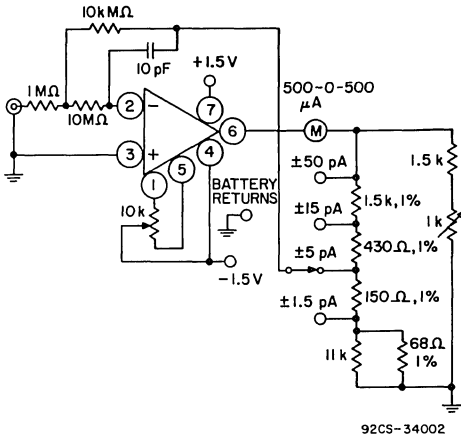


Fig. 10 - CA5420 picoammeter circuit.

### High-Input-Resistance Voltmeter

Advantage is taken of the high input impedance of the CA5420 in a high-input-resistance dc voltmeter. Only two 1.5-V "AA"-type penlite batteries power this exceedingly high-input-resistance ( $>1,000,000$  megohms) dc voltmeter. Full-scale deflection is  $\pm 500$  mV,  $\pm 150$  mV, and  $\pm 15$  mV. Higher voltage ranges are easily added with external input voltage attenuator networks.

The meter is placed in series with the gain network, thus eliminating the meter temperature coefficient error term.

Supply current in the standby position with the meter undeflected is  $300 \mu\text{A}$ . At full-scale deflection this current rises to  $800 \mu\text{A}$ . Carbon-zinc battery life should be in excess of 1,000 hours.

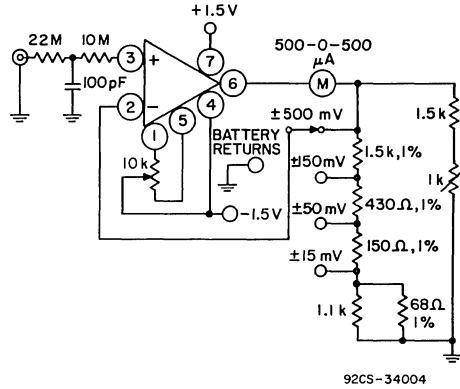


Fig. 11 - CA5420 high-input-resistance voltmeter.

August 1991

## Quad Microprocessor BiMOS-E Operational Amplifiers With MOSFET Input/Bipolar Output

### Features

- High-Speed CMOS Input Stage Provides
  - ▶ Very High  $Z_i$  .....  $5T\Omega$  ( $5 \times 10^{12}\Omega$ ) Typ.
  - ▶ Very Low  $I_j$  .....  $0.5\text{pA}$  (Typ) at 5V Operation
  - ▶ Very Low  $I_{IO}$  .....  $0.5\text{pA}$  (Typ) at 5V Operation
- ESD Protection to 2000V
- 3V to 16V Power Supply Operation
- Fully Guaranteed Specifications Over Full Military Range
- Wide BW (14MHz); High SR ( $5\text{V}/\mu\text{s}$ ) at 5V Supply
- Wide  $V_{ICR}$  Range From  $-0.5\text{V}$  to  $3.7\text{V}$  (Typ) at 5V Supply
- Ideally Suited for CMOS and HCMOS Applications
- +5V Characteristics for Microprocessor Applications

### Applications

- Bar Code Readers
- Photodiode Amplifiers (IR)
- Microprocessor Buffering
- Ground Reference Single Supply Amplifiers
- Fast Sample and Hold
- Timers
- Voltage Controlled Oscillators
- Voltage Followers
- V to I Converters
- Peak Detectors
- Precision Rectifiers
- 5V Logic Systems
- 3V Logic Systems

### Description

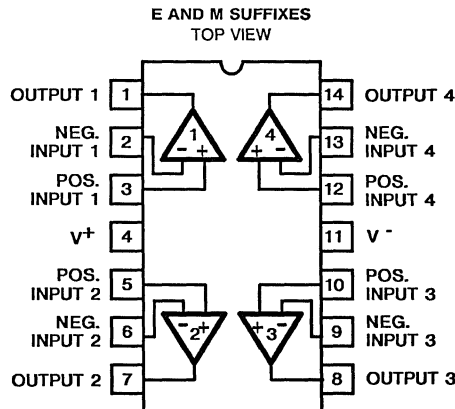
The CA5470 series are integrated circuit operational amplifiers that combine the advantages of both high-speed CMOS and bipolar transistors on a single monolithic chip. They are constructed in the BiMOS-E process which adds drain-extension implants to  $3\mu\text{m}$  polygate CMOS, enhancing both the voltage capability and providing vertical bipolar transistors for broadband analog/digital functions. This process lends itself easily to high-speed operational amplifiers, comparators, analog switches and interface peripherals, resulting in twice the speed of the conventional CMOS transistors having similar feature size.

BiMOS-E are broadbased bipolar transistors that have high transconductance, gains more constant with current level, stable "precision" base-emitter offset voltages and superior drive capability. Excellent interface with environmental potentials enable use in 5V logic systems and future 3.3V logic systems.

ESD capability exceeds the standard 2000 volt level. The CA5470 series can operate with single supply voltages from 3V to 16V or  $\pm 1.5\text{V}$  to  $\pm 8\text{V}$ . They have guaranteed specifications at both 5V and  $\pm 7.5\text{V}$  at room temperature as well as over the full  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  military range.

The CA5470 series is supplied in the standard 14 lead dual-in-line plastic package (E suffix) and the 14 lead small outline package (M suffix). The CA5470 is also available in chip form (H suffix).

### Pinout



# CA5470

## MAXIMUM RATINGS, Absolute-Maximum Values

### DC SUPPLY-VOLTAGE

(Between V+ and V- Terminals) ..... 16 V

DIFFERENTIAL MODE INPUT VOLTAGE .....  $\pm 8$  V

COMMON-MODE DC INPUT VOLTAGE ..... (V+ +8 V) to (V- -0.5V)

INPUT TERMINAL CURRENT ..... 1 mA

### DEVICE DISSIPATION:

#### WITHOUT HEAT SINK -

up to 55°C ..... 630 mW

above 55°C ..... Derate Linearly 6.67 mW/°C

#### WITH HEAT SINK -

up to 90°C ..... 1 W

above 90°C ..... Derate Linearly 16.7 mW/°C

#### SMALL OUTLINE PACKAGE -

up to 65°C ..... 500 mW

above 65°C ..... Derate Linearly at 5.9 mW/°C

### TEMPERATURE RANGE:

OPERATING (all types) ..... -55 to +125°C

STORAGE (all types) ..... -65 to +150°C

OUTPUT SHORT-CIRCUIT DURATION\* ..... INDEFINITE

### LEAD TEMPERATURE (DURING SOLDERING):

At distance  $1/16 \pm 1/32$  (1.59  $\pm$  0.79 mm) from case for 10 seconds max ..... +265°C

\*Short circuit may be applied to ground or to either supply.

## TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE $V_+ = 5$ V, $V_- = 0$ , $T_A = 25^\circ\text{C}$ (Unless Otherwise Specified)

| CHARACTERISTIC   | TEST CONDITIONS                   | TYPICAL VALUES | UNITS            |
|--|-----------------------------------|----------------|------------------|
| Input Resistance $R_i$   |                                   | 5              | $\text{T}\Omega$ |
| Input Capacitance $C_i$  | $f = 1$ MHz                       | 3.1            | $\mu\text{F}$    |
| Unity Gain Crossover Frequency $f_T$                                       |                                   | 14             | MHz              |
| Slew Rate SR   | $V_{OUT} = 3.65$ V <sub>p-p</sub> | 5              | v/ $\mu\text{s}$ |
| Transient Response:  | $C_L = 25$ pF                     |                |                  |
| Rise Time/Fall Time  | $R_L = 2$ k $\Omega$              | 27/25          | ns               |
| Overshoot  | (Voltage Follower)                | 20             | %                |
| Settling Time (4V <sub>p-p</sub> Input to < 0.1%)                          |                                   | 1              | $\mu\text{s}$    |
| Full Power BW ( $V_{OUT} = 3.65$ V <sub>p-p</sub> ) SR = 5V/ $\mu\text{s}$ | $A_V = 1$                         | 436            | kHz              |

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OPERATIONAL  
AMPLIFIERS

## CA5470

**ELECTRICAL CHARACTERISTICS** At  $T_A = 25^\circ\text{C}$ ,  $V_+ = 5\text{ V}$ ,  $V_- = \text{Gnd}$

| CHARACTERISTICS  |                     | LIMITS |             |      | UNITS            |
|--|---------------------|--------|-------------|------|------------------|
|  |                     | MIN.   | TYP         | MAX. |                  |
| Input Offset Voltage                                       | $ V_{IO} $          | —      | 6           | 22   | mV               |
| Input Offset Current                                       | $ I_{IO} $          | —      | 0.5         | 5    | pA               |
| Input Current  | $I_I$               | —      | 0.5         | 10   | pA               |
| Common-Mode Input Range                                    | $V_{ICR}$           | 3.5    | -0.5 to 3.7 | 0    | V                |
| Common-Mode Rejection Ratio<br>$V_{ICR} = 0$ to 3.5 V      | $C_{MRR}$           | 55     | 70          | —    | dB               |
| Power-Supply Rejection Ratio<br>$\Delta V = 2\text{ V}$    | $P_{SRR}$           | 60     | 75          | —    | dB               |
| Positive Output Voltage Swing<br>$R_L = 2\text{ k}$ to GND | $V_{OM+}$           | 4      | 4.4         | —    | V                |
| Negative Output Voltage Swing<br>$R_L = 2\text{ k}$ to GND | $V_{OM-}$           | —      | 0.06        | 0.10 | V                |
| Total Supply Current $V_{OUT} = 2.5\text{ V}$              | $I_{SUPPLY}$        | —      | 8           | 10   | mA               |
| Unity Gain Bandwidth Product                               | $f_T$               | 10     | 14          | —    | MHz              |
| Slew Rate  | SR                  | 4      | 5           | —    | V/ $\mu\text{s}$ |
| Output Current   |                     |        |             |      |                  |
| Source to opposite supply                                  | $I_{SOURCE}$        | 4      | 5.5         | —    | mA               |
| Sink to opposite supply                                    | $I_{SINK}$          | 0.8    | 1.2         | —    | mA               |
| Open Loop Gain $0.5\text{ V}$ to 3.5 V                     | $R_L = 10\text{ k}$ | 80     | 90          | —    | dB               |

**ELECTRICAL CHARACTERISTICS** At  $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_+ = 5\text{ V}$ ,  $V_- = \text{Gnd}$

| CHARACTERISTICS  |                     | LIMITS |             |       | UNITS            |
|--|---------------------|--------|-------------|-------|------------------|
|  |                     | MIN.   | TYP         | MAX.  |                  |
| Input Offset Voltage   | $ V_{IO} $          | —      | 6           | 25    | mV               |
| Input Offset Current   | $ I_{IO} $          | —      | 550         | 5500  | pA               |
| Input Current  | $I_I$               | —      | 550         | 11000 | pA               |
| Common-Mode Input Range                                      | $V_{ICR}$           | 3.5    | -0.5 to 3.7 | 0     | V                |
| Common-Mode Rejection Ratio<br>$V_{ICR} = 0$ to 3.5 V        | $C_{MRR}$           | 50     | 65          | —     | dB               |
| Power-Supply Rejection Ratio<br>$\Delta V = 2\text{ V}$      | $P_{SRR}$           | 58     | 75          | —     | dB               |
| Positive Output Voltage Swing<br>$R_L = 2\text{ k}$ to $V_-$ | $V_{OM+}$           | 3.8    | 4.2         | —     | V                |
| Negative Output Voltage Swing<br>$R_L = 2\text{ k}$ to $V_-$ | $V_{OM-}$           | —      | 0.08        | 0.11  | V                |
| Total Supply Current $V_{OUT} = 2.5\text{ V}$                | $I_{SUPPLY}$        | —      | 9           | 11    | mA               |
| Unity Gain Bandwidth Product                                 | $f_T$               | 8      | 12          | —     | MHz              |
| Slew Rate  | SR                  | 3      | 5           | —     | V/ $\mu\text{s}$ |
| Output Current   |                     |        |             |       |                  |
| Source to opposite supply                                    | $I_{SOURCE}$        | 4      | 5.5         | —     | mA               |
| Sink to opposite supply                                      | $I_{SINK}$          | 0.8    | 1.2         | —     | mA               |
| Open Loop Gain $0.5\text{ V}$ to 3.5 V                       | $R_L = 10\text{ k}$ | 80     | 90          | —     | dB               |

## CA5470

**ELECTRICAL CHARACTERISTICS** At  $T_A = 25^\circ\text{C}$ ,  $V_+ = 7.5\text{ V}$ ,  $V_- = -7.5\text{ V}$

| CHARACTERISTICS  |                     | LIMITS |             |       | UNITS            |
|--|---------------------|--------|-------------|-------|------------------|
|  |                     | MIN.   | TYP         | MAX.  |                  |
| Input Offset Voltage                                       | $ V_{IO} $          | —      | 5           | 25    | mV               |
| Input Offset Current                                       | $ I_{IO} $          | —      | 0.5         | 5     | pA               |
| Input Current  | $I_I$               | —      | 1           | 10    | pA               |
| Common-Mode Input Range                                    | $V_{ICR}$           | 5.8    | -7.8 to 6.0 | -7.5  | V                |
| Common-Mode Rejection Ratio<br>$V_{ICR} = 0$ to 3.5 V      | CMRR                | 60     | 70          | —     | dB               |
| Power-Supply Rejection Ratio<br>$\Delta V = 2\text{ V}$    | PSRR                | 65     | 76          | —     | dB               |
| Positive Output Voltage Swing<br>$R_L = 2\text{ k}$ to GND | $V_{OM+}$           | 6.3    | 6.5         | —     | V                |
| $R_L = 10\text{ k}$ to GND                                 |                     | 6.4    | 6.6         | —     |                  |
| Negative Output Voltage Swing<br>$R_L = 2\text{ k}$ to GND | $V_{OM-}$           | —      | -7.47       | -7.45 | V                |
| $R_L = 10\text{ k}$ to GND                                 |                     | —      | -7.3        | -7.1  |                  |
| Total Supply Current $V_{OUT} = \text{GND}$                | $I_{SUPPLY}$        | —      | 10          | 11    | mA               |
| Unity Gain Bandwidth Product                               | $f_T$               | 12     | 16          | —     | MHz              |
| Slew Rate  | SR                  | 4      | 7           | —     | V/ $\mu\text{s}$ |
| Output Current<br>Source to opposite supply                | $I_{SOURCE}$        | 6.2    | 6.8         | —     | mA               |
| Sink to opposite supply                                    | $I_{SINK}$          | 1      | 1.4         | —     | mA               |
| Open Loop Gain $-5\text{ V}$ to $+5\text{ V}$              | $R_L = 10\text{ k}$ | 80     | 90          | —     | dB               |

**ELECTRICAL CHARACTERISTICS** At  $T_A = 55^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_+ = 7.5\text{ V}$ ,  $V_- = -7.5\text{ V}$

| CHARACTERISTICS  |                     | LIMITS |             |       | UNITS            |
|--|---------------------|--------|-------------|-------|------------------|
|  |                     | MIN.   | TYP         | MAX.  |                  |
| Input Offset Voltage   | $ V_{IO} $          | —      | 5           | 30    | mV               |
| Input Offset Current   | $ I_{IO} $          | —      | 550         | 5500  | pA               |
| Input Current  | $I_I$               | —      | 1100        | 11000 | pA               |
| Common-Mode Input Range                                      | $V_{ICR}$           | 5.8    | -7.8 to 6.0 | -7.5  | V                |
| Common-Mode Rejection Ratio<br>$V_{ICR} = 0$ to 3.5 V        | CMRR                | 58     | 70          | —     | dB               |
| Power-Supply Rejection Ratio<br>$\Delta V = 2\text{ V}$      | PSRR                | 60     | 76          | —     | dB               |
| Positive Output Voltage Swing<br>$R_L = 2\text{ k}$ to $V_-$ | $V_{OM+}$           | 6      | 6.2         | —     | V                |
| $R_L = 10\text{ k}$ to GND                                   |                     | 6.1    | 6.4         | —     |                  |
| Negative Output Voltage Swing<br>$R_L = 2\text{ k}$ to $V_-$ | $V_{OM-}$           | —      | -7.47       | -7.45 | V                |
| $R_L = 10\text{ k}$ to GND                                   |                     | —      | -7.3        | -7.1  |                  |
| Total Supply Current $V_{OUT} = \text{GND}$                  | $I_{SUPPLY}$        | —      | 11          | 12    | mA               |
| Unity Gain Bandwidth Product                                 | $f_T$               | 10     | 15          | —     | MHz              |
| Slew Rate  | SR                  | 3      | 7           | —     | V/ $\mu\text{s}$ |
| Output Current<br>Source to opposite supply                  | $I_{SOURCE}$        | 6.2    | 6.8         | —     | mA               |
| Sink to opposite supply                                      | $I_{SINK}$          | 1      | 1.4         | —     | mA               |
| Open Loop Gain $-5\text{ V}$ to $+5\text{ V}$                | $R_L = 10\text{ k}$ | 80     | 90          | —     | dB               |



# CA5470

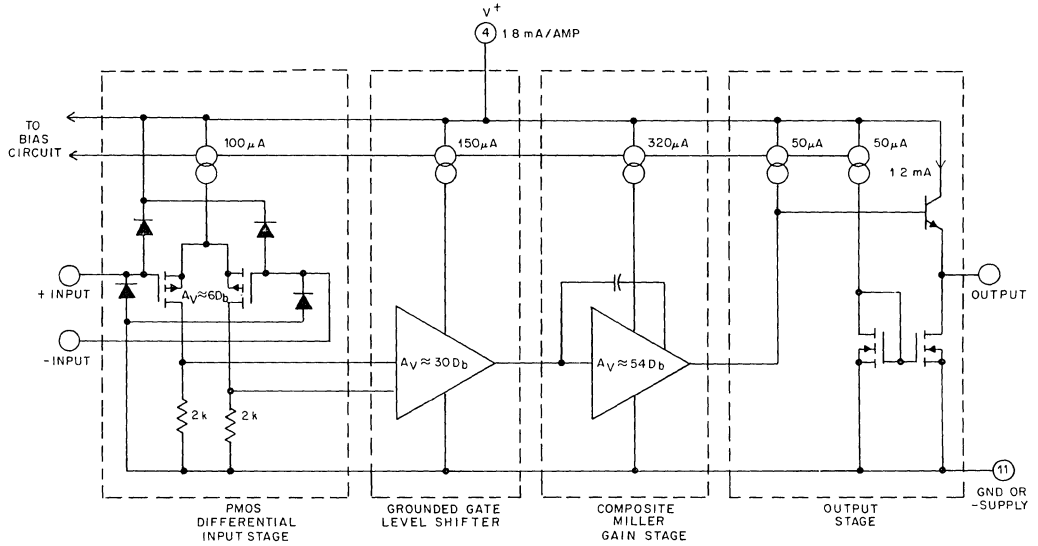
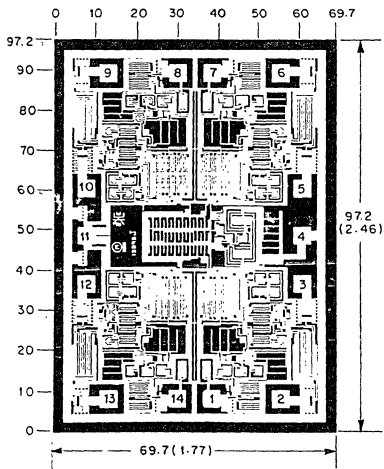


Figure 2 - Block diagram of the CA5470.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mills ( $10^{-3}$  inch). The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are  $57^\circ$  instead of  $90^\circ$  with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Figure 3 - Dimensions and pad layout for CA5470H.

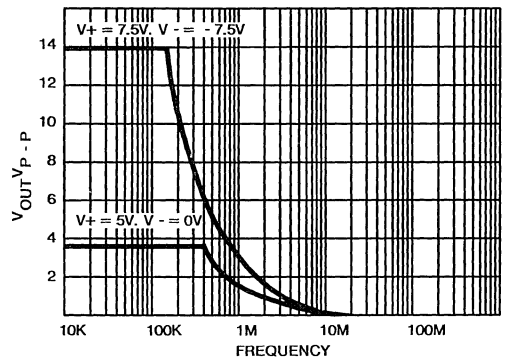


Figure 4 - Maximum output voltage swing vs frequency.

## PRAM Four Channel Programmable Amplifier

August 1991

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OPERATIONAL AMPLIFIERS

### Features

- Programmability
- High Rate Slew ..... 30V/ $\mu$ s
- Wide Gain Bandwidth ..... 40MHz
- High Gain ..... 150kV/V
- Low Offset Current ..... 5nA
- High Input Impedance ..... 30M $\Omega$
- Single Capacitor Compensation
- DTL/TTL Compatible Inputs

### Applications

- Thousands of Applications; Program:
  - ▶ Signal Selection/Multiplexing
  - ▶ Operational Amplifier Gain
  - ▶ Oscillator Frequency
  - ▶ Filter Characteristics
  - ▶ Add-Subtract Functions
  - ▶ Integrator Characteristics
  - ▶ Comparator Levels
- For Further Design Ideas, See App. Note 514.

### Description

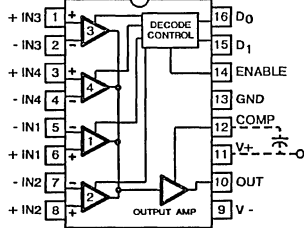
HA-2400/04/05 comprise a series of four-channel programmable amplifiers providing a level of versatility unsurpassed by any other monolithic operational amplifier. Versatility is achieved by employing four input amplifier channels, any one (or none) of which may be electronically selected and connected to a single output stage through DTL/TTL compatible address inputs. The device formed by the output and the selected pair of inputs is an op amp which delivers excellent slew rate, gain bandwidth and power bandwidth performance. Other advantageous features for these dielectrically isolated amplifiers include high voltage gain and input impedance coupled with low input offset voltage and offset current. External compensation is not required on this device at closed loop gains greater than 10.

Each channel of the HA-2400/04/05 can be controlled and operated with suitable feedback networks in any of the standard op amp configurations. This specialization makes these amplifiers excellent components for multiplexing signal selection and mathematical function designs. With 30V/ $\mu$ s slew rate, 40MHz gain bandwidth and 30M ohms input impedance these devices are ideal building blocks for signal generators, active filters and data acquisition designs. Programmability, coupled with 4mV typical offset voltage and 5nA offset current, makes these amplifiers outstanding components for signal conditioning circuits.

HA-2400/04/05 are available in a 16 pin Dual-In-Line package. HA-2400 is specified from  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . HA-2404 is specified over the  $-25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  range, while HA-2405 operates from  $0^{\circ}\text{C}$  to  $+75^{\circ}\text{C}$ .

### Pinout

HA1-2400/04/05 (CERAMIC DIP)  
TOP VIEW



TRUTH TABLE

| D <sub>1</sub> | D <sub>0</sub> | EN | SELECTED CHANNEL |
|----------------|----------------|----|------------------|
| L              | L              | H  | 1                |
| L              | H              | H  | 2                |
| H              | L              | H  | 3                |
| H              | H              | H  | 4                |
| X              | X              | L  | NONE             |

### Schematic

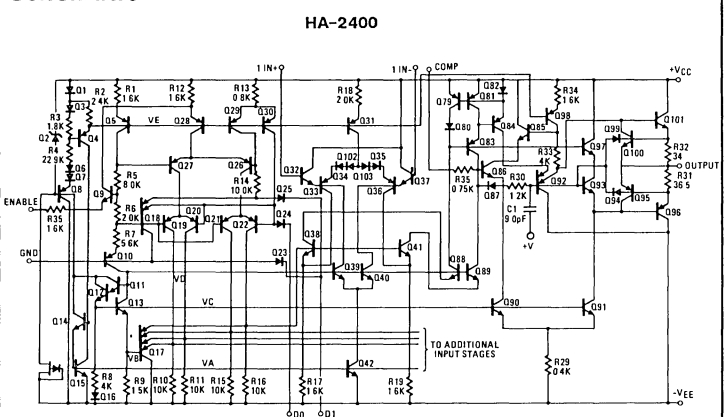


Diagram Includes: One Input Stage, Decode Control, Bias Network, and Output Stage.

## Specifications HA-2400/04/05

### Absolute Maximum Ratings

|  |  |
|--|--|
| Voltage between V+ and V- Terminals .....  | 45.0V  |
| Differential Input Voltage .....           | $\pm V_{SUPPLY}$                                   |
| Digital Input Voltage .....                | -0.76V to +10.0V                                   |
| Output Current .....                       | Short Circuit Protected<br>( $I_{SC} < \pm 33mA$ ) |
| Internal Power Dissipation (Note 13) ..... | 300mW  |

### Operating Temperature Ranges

|                                 |  |
|---------------------------------|--|
| HA-2400-2 .....                 | $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ |
| HA-2404-4 .....                 | $-25^{\circ}C \leq T_A \leq +85^{\circ}C$  |
| HA-2405-5 .....                 | $0^{\circ}C \leq T_A \leq +75^{\circ}C$    |
| Storage Temperature Range ..... | $-65^{\circ}C \leq T_A \leq +150^{\circ}C$ |

### Electrical Specifications

Test Conditions:  $V_{SUPPLY} = \pm 15.0V$ , Unless Otherwise Specified.

Digital Inputs:  $V_{IL} = +0.5V$ ,  $V_{IH} = +2.4$ . Limits apply to each of the four channels, when addressed.

| PARAMETER   | TEMP  | HA-2400/04<br>LIMITS |       |     | HA-2405<br>LIMITS |       |     | UNITS |
|---|-------|----------------------|-------|-----|-------------------|-------|-----|-------|
|   |       | MIN                  | TYP   | MAX | MIN               | TYP   | MAX |       |
| <b>INPUT CHARACTERISTICS</b>                              |       |                      |       |     |                   |       |     |       |
| Offset Voltage  | +25°C | -                    | 4     | 9   | -                 | 4     | 9   | mV    |
|   | Full  | -                    | -     | 11  | -                 | -     | 11  | mV    |
| Bias Current (Note 12)                                    | +25°C | -                    | 50    | 200 | -                 | 50    | 250 | nA    |
|   | Full  | -                    | -     | 400 | -                 | -     | 500 | nA    |
| Offset Current (Note 12)                                  | +25°C | -                    | 5     | 50  | -                 | 5     | 50  | nA    |
|   | Full  | -                    | -     | 100 | -                 | -     | 100 | nA    |
| Input Resistance (Note 12)                                | +25°C | -                    | 30    | -   | -                 | 30    | -   | MΩ    |
| Common Mode Range   | Full  | ±9.0                 | -     | -   | ±9.0              | -     | -   | V     |
| <b>TRANSFER CHARACTERISTICS</b>                           |       |                      |       |     |                   |       |     |       |
| Large Signal Voltage Gain (Notes 1, 5)                    | +25°C | 50k                  | 150k  | -   | 50k               | 150k  | -   | V/V   |
|   | Full  | 25K                  | -     | -   | 25K               | -     | -   | V/V   |
| Common Mode Rejection Ratio (Note 2)                      | Full  | 80                   | 100   | -   | 74                | 100   | -   | dB    |
| Gain Bandwidth (Notes 3, 14)<br>(Notes 4, 14)             | +25°C | 20                   | 40    | -   | 20                | 40    | -   | MHz   |
|   | +25°C | 4                    | 8     | -   | 4                 | 8     | -   | MHz   |
| <b>OUTPUT CHARACTERISTICS</b>                             |       |                      |       |     |                   |       |     |       |
| Output Voltage Swing (Note 1)                             | Full  | ±10.0                | ±12.0 | -   | ±10.0             | ±12.0 | -   | V     |
| Output Current  | +25°C | 10                   | 20    | -   | 10                | 20    | -   | mA    |
| Full Power Bandwidth (Notes 3, 5, 15)<br>(Notes 4, 5, 15) | +25°C | 640                  | 950   | -   | 640               | 950   | -   | kHz   |
|   | +25°C | 200                  | 250   | -   | 200               | 250   | -   | kHz   |
| <b>TRANSIENT RESPONSE</b>                                 |       |                      |       |     |                   |       |     |       |
| Rise Time (Notes 4, 6)                                    | +25°C | -                    | 20    | 45  | -                 | 20    | 50  | ns    |
| Overshoot (Notes 4, 6)                                    | +25°C | -                    | 25    | 40  | -                 | 25    | 40  | %     |
| Slew Rate (Notes 3, 7)<br>(Notes 4, 7, 14)                | +25°C | 20                   | 30    | -   | 20                | 30    | -   | V/μs  |
|   | +25°C | 6                    | 8     | -   | 6                 | 8     | -   | V/μs  |
| Settling Time (Notes 4, 7, 8, 14)                         | +25°C | -                    | 1.5   | 2.5 | -                 | 1.5   | 2.5 | μs    |
| <b>CHANNEL SELECT CHARACTERISTICS</b>                     |       |                      |       |     |                   |       |     |       |
| Digital Input Current ( $V_{IN} = 0V$ )                   | Full  | -                    | 1     | 1.5 | -                 | 1     | 1.5 | mA    |
| Digital Input Current ( $V_{IN} = +5.0V$ )                | Full  | -                    | 5     | -   | -                 | 5     | -   | nA    |
| Output Delay (Notes 9, 14)                                | +25°C | -                    | 100   | 250 | -                 | 100   | 250 | ns    |
| Crosstalk (Note 10)                                       | +25°C | -80                  | -110  | -   | -74               | -110  | -   | dB    |
| <b>POWER SUPPLY CHARACTERISTICS</b>                       |       |                      |       |     |                   |       |     |       |
| Supply Current  | +25°C | -                    | 4.8   | 6.0 | -                 | 4.8   | 6.0 | mA    |
| Power Supply Rejection Ratio (Note 11)                    | Full  | 74                   | 90    | -   | 74                | 90    | -   | dB    |

#### NOTES:

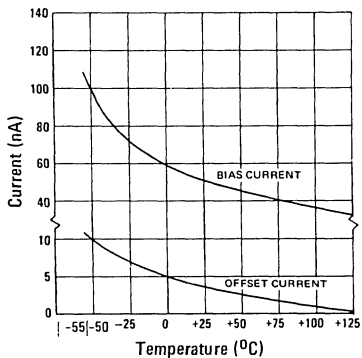
1.  $R_L = 2k\Omega$
2.  $V_{CM} = \pm 5VDC$
3.  $A_V = +10$ ,  $C_{COMP} = 0$ ,  $R_L = 2k\Omega$ ,  $C_L = 50pF$ .
4.  $A_V = +1$ ,  $C_{COMP} = 15pF$ ,  $R_L = 2k\Omega$ ,  $C_L = 50pF$ .
5.  $V_{OUT} = 20V$  peak to peak.
6.  $V_{OUT} = 200mV$  peak.
7.  $V_{OUT} = 10.0V$  peak to peak.
8. To 0.1% of final value.
9. To 10% of final value; output then slews at normal rate to final value.

10. Unselected input to output;  $V_{IN} = \pm 10VDC$
11.  $V_{SUPPLY} = \pm 10VDC$  to  $\pm 20VDC$
12. Unselected channels have approximately the same input parameters.
13. Derate by  $4.3mW/^{\circ}C$  above  $105^{\circ}C$ .
14. Guaranteed by design.
15. Full Power Bandwidth based on slew rate measurement using:

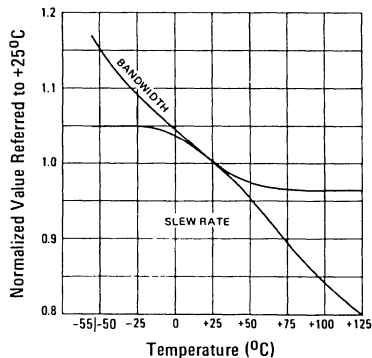
$$FPBW = \frac{S.R.}{2\pi V_{PEAK}}; V_{PEAK} = 5V$$

**Typical Performance Curves**  $V^+ = +15\text{VDC}$ ,  $V^- = -15\text{VDC}$ ,  $T_A = +25^\circ\text{C}$ , Unless Otherwise Specified.

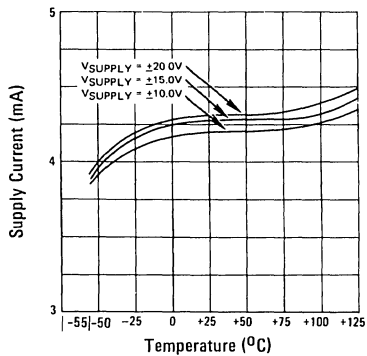
**INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE**



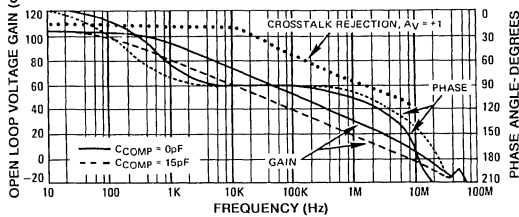
**NORMALIZED A.C. PARAMETERS vs. TEMPERATURE**



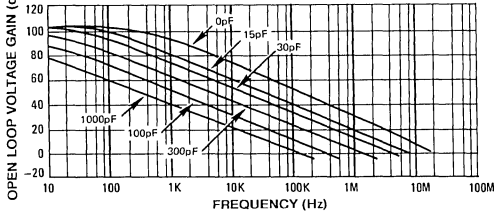
**POWER SUPPLY CURRENT DRAIN AS A FUNCTION OF TEMPERATURE**



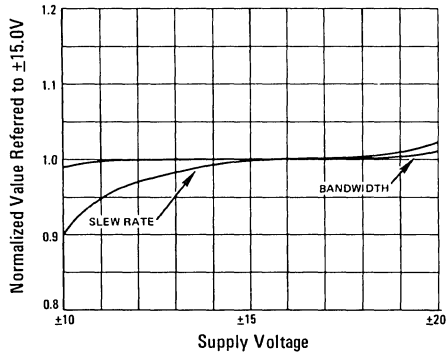
**OPEN LOOP FREQUENCY AND PHASE RESPONSE**



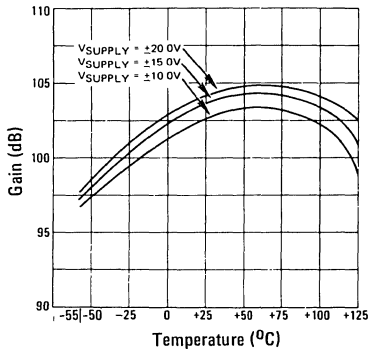
**FREQUENCY RESPONSE vs.  $C_{\text{COMP}}$**



**NORMALIZED A.C. PARAMETERS vs. SUPPLY VOLTAGE**



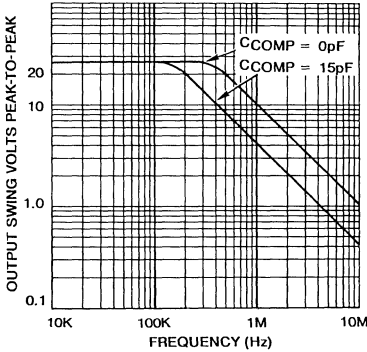
**OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE**



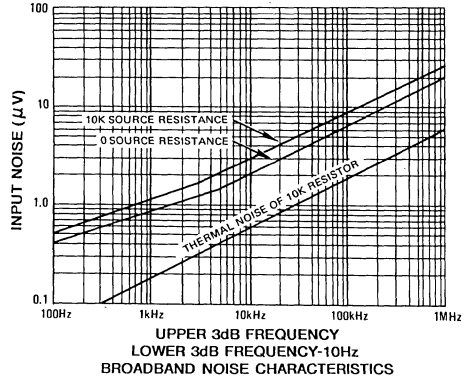
**3**  
OPERATIONAL AMPLIFIERS

Typical Performance Curves (Continued)

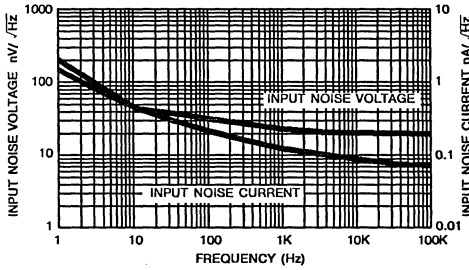
OUTPUT VOLTAGE SWING vs. FREQUENCY



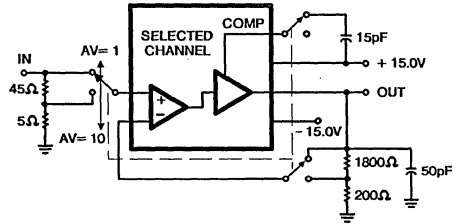
EQUIVALENT INPUT NOISE vs. BANDWIDTH



INPUT NOISE vs. FREQUENCY

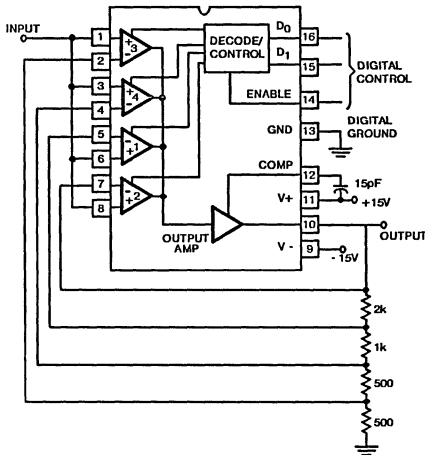


SLEW RATE AND TRANSIENT RESPONSE

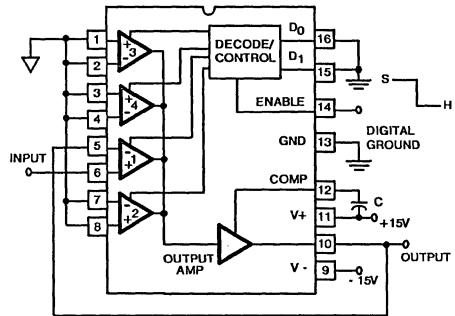


Typical Applications

HA-2400 AMPLIFIER, NONINVERTING PROGRAMMABLE GAIN



HA-2400 SAMPLE AND HOLD



Sample Charging Rate =  $\frac{I_1}{C}$  V/Sec.  $I_1 \approx 150 \times 10^{-6} \text{A}$   
 $I_2 \approx 200 \times 10^{-9} \text{A} @ +25^\circ\text{C}$   
 $\approx 600 \times 10^{-9} \text{A} @ -55^\circ\text{C}$   
 $\approx 100 \times 10^{-9} \text{A} @ +125^\circ\text{C}$

Hold Drift Rate =  $\frac{I_2}{C}$  V/Sec.

Switch Pedestal Error =  $\frac{Q}{C}$  Volts  $Q \approx 2 \times 10^{-12}$  Coulomb

For More Examples, See Harris Application Note 514

## Digitally Selectable Four Channel Operational Amplifier

August 1991

### Features

- TTL Compatible Inputs
- Single Capacitor Compensation
- Low Crosstalk ..... -110dB
- High Slew Rate ..... 20V/ $\mu$ s
- Low Offset Current ..... 5nA
- Offset Voltage ..... 7mV
- High Gain-Bandwidth ..... 30MHz
- High Input Impedance ..... 30M $\Omega$

### Description

The HA-2406 is a monolithic device consisting of four op amp input stages that can be individually connected to one output stage by decoding two TTL lines into four channel select signals. In addition to allowing each channel to be addressed, an enable control disconnects all input stages from the output stage when asserted low.

Each input-output combination of the HA-2406 is designed to be a 20V/ $\mu$ s, 30MHz gain-bandwidth amplifier that is stable at a gain of ten but by connecting one external 15pF capacitor all amplifiers are compensated for unity gain operation. The compensation pin may also be used to limit the output swing to TTL levels through suitable clamping diodes and divider networks (see Application Note 514).

### Applications

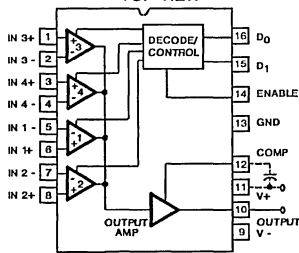
- Digital Control Of:
  - ▶ Analog Signal Multiplexing
  - ▶ Op Amp Gains
  - ▶ Oscillator Frequencies
  - ▶ Filter Characteristics
  - ▶ Comparator Levels
- For Further Design Ideas See Application Note 514

Dielectric isolation and short-circuit protected output stages contribute to the quality and durability of the HA-2406. When used as a simple amplifier, its dynamic performance is very good and when its added versatility is considered, the HA-2406 is unmatched in the analog world. It can replace a number of individual components in analog signal conditioning circuits for digital signal processing systems. Its advantages include saving board space and reducing power supply requirements.

The HA-2406 is available in a 16 pin dual-in-line package and is guaranteed for operation over the full commercial temperature range (0°C to +75°C). An SOIC package option is also available with -5 and -9 temperature grades.

### Pinout

HA9P2406-5, -9  
HA3-2406-5, HA1-2406-5  
TOP VIEW



### TRUTH TABLE

| D1 | D0 | EN | SELECTED CHANNEL |
|----|----|----|------------------|
| L  | L  | H  | 1                |
| L  | H  | H  | 2                |
| H  | L  | H  | 3                |
| H  | H  | H  | 4                |
| X  | X  | L  | NONE             |

### Schematic

HA-2406

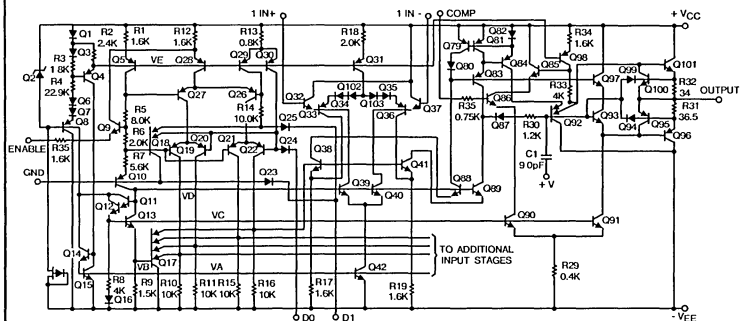


Diagram includes: One Input Stage, Decode Control, Bias Network and Output Stage.

## Specifications HA-2406

### Absolute Maximum Ratings

|   |   |                                  |  |
|---|---|----------------------------------|--|
| Voltage Between V+ and V- Terminals ..... | 45.0V   | Internal Power Dissipation ..... | 300mW  |
| Differential Input Voltage .....          | $\pm V_{SUPPLY}$  | Operating Temperature Range:     |  |
| Digital Input Voltage .....               | -0.76V to +10.0V  | HA-2406-5 .....                  | $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$    |
| Output Current .....                      | Short Circuit Protected<br>( $I_{SC} < \pm 33\text{mA}$ ) | HA-2406-9 .....                  | $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  |
|   |   | Storage Temperature Range .....  | $-65^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ |

**Electrical Specifications** Test Conditions:  $V_{SUPPLY} = \pm 15.0\text{V}$  Unless Otherwise Specified.  
 Digital Inputs:  $V_{IL} = +0.5\text{V}$ ,  $V_{IH} = +2.4\text{V}$ . Limits apply to each of the four channels, when addressed.

| PARAMETER   | TEMP  | HA-2406-5, -9<br>LIMITS |       |     | UNITS |
|---|-------|-------------------------|-------|-----|-------|
|   |       | MIN                     | TYP   | MAX |       |
| <b>INPUT CHARACTERISTICS</b>                      |       |                         |       |     |       |
| Offset Voltage                                    | +25°C | -                       | 7     | 10  | mV    |
|   | Full  | -                       | -     | 12  | mV    |
| Bias Current (Note 12)                            | +25°C | -                       | 50    | 250 | nA    |
|   | Full  | -                       | -     | 500 | nA    |
| Offset Current (Note 12)                          | +25°C | -                       | 5     | 50  | nA    |
|   | Full  | -                       | -     | 100 | nA    |
| Input Resistance (Note 12)                        | +25°C | -                       | 30    | -   | MΩ    |
|   | Full  | ±9.0                    | -     | -   | V     |
| <b>TRANSFER CHARACTERISTICS</b>                   |       |                         |       |     |       |
| Large Signal Voltage Gain (Notes 1, 5)            | +25°C | 40K                     | 150K  | -   | V/V   |
|   | Full  | 20K                     | -     | -   | V/V   |
| Common Mode Rejection Ratio (Note 2)              | Full  | 74                      | 80    | -   | dB    |
| Gain Bandwidth (Note 3, 15)                       | +25°C | 15                      | 30    | -   | MHz   |
| Gain Bandwidth (Note 4, 15)                       | +25°C | 3                       | 6     | -   | MHz   |
| <b>OUTPUT CHARACTERISTICS</b>                     |       |                         |       |     |       |
| Output Voltage Swing (Note 1)                     | Full  | ±10.0                   | ±12.0 | -   | V     |
| Output Current (Note 13)                          | +25°C | 10                      | 15    | -   | mA    |
| Full Power Bandwidth (Notes 3, 5, 14, 15)         | +25°C | 240                     | 320   | -   | kHz   |
| Full Power Bandwidth (Notes 4, 5, 14)             | +25°C | 64                      | 95    | -   | kHz   |
| <b>TRANSIENT RESPONSE</b>                         |       |                         |       |     |       |
| Rise Time (Notes 4, 6)                            | +25°C | -                       | 30    | 100 | ns    |
| Overshoot (Notes 4, 6)                            | +25°C | -                       | 25    | 40  | %     |
| Slew Rate (Notes 3, 7, 15)                        | +25°C | 15                      | 20    | -   | V/μs  |
| Slew Rate (Notes 4, 7)                            | +25°C | 4                       | 6     | -   | V/μs  |
| Settling Time (Notes 4, 7, 8, 15)                 | +25°C | -                       | 2.0   | 3.5 | μs    |
| <b>CHANNEL SELECT CHARACTERISTICS</b>             |       |                         |       |     |       |
| Digital Input Current ( $V_{IN} = 0\text{V}$ )    | Full  | -                       | 1     | 1.5 | mA    |
| Digital Input Current ( $V_{IN} = +5.0\text{V}$ ) | Full  | -                       | 15    | -   | nA    |
| Output Delay (Note 9, 15)                         | +25°C | -                       | 150   | 300 | ns    |
| Crosstalk (Note 10)                               | +25°C | -74                     | -110  | -   | dB    |
| <b>POWER SUPPLY CHARACTERISTICS</b>               |       |                         |       |     |       |
| Supply Current                                    | +25°C | -                       | 4.8   | 7.0 | mA    |
| Power Supply Rejection Ratio (Note 11)            | Full  | 74                      | 90    | -   | dB    |

**NOTES:**

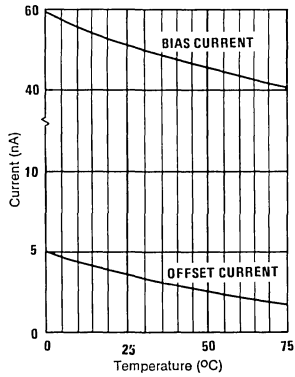
1.  $R_L = 2\text{k}\Omega$
2.  $V_{CM} = \pm 5\text{VDC}$
3.  $A_V = +10$ ,  $C_{COMP} = 0$ ,  $R_L = 2\text{k}\Omega$ ,  $C_L = 50\text{pF}$ .
4.  $A_V = +1$ ,  $C_{COMP} = 15\text{pF}$ ,  $R_L = 2\text{k}\Omega$ ,  $C_L = 50\text{pF}$ .
5.  $V_{OUT} = 20\text{V}$  peak to peak.
6.  $V_{OUT} = 200\text{mV}$  peak to peak.
7.  $V_{OUT} = 10.0\text{V}$  peak to peak.
8. To 0.1% of final value.
9. To 10% of final value; output then slews at normal rate to final value.

10. Unselected input to output;  $V_{IN} = \pm 10\text{VDC}$
11.  $V_{SUPPLY} = \pm 10\text{VDC}$  to  $\pm 20\text{VDC}$
12. Unselected channels have approximately the same input parameters.
13.  $V_{OUT} = \pm 10\text{V}$
14. Full power Bandwidth based on slew rate measurement using:  

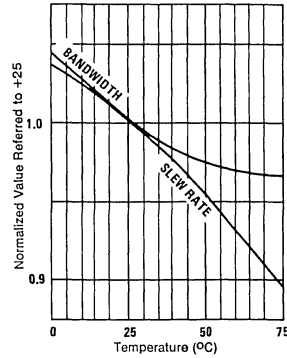
$$\text{FPBW} = \frac{\text{S.R.}}{2\pi V_{\text{peak}}}$$
15. Sample tested.

**Typical Performance Curves**  $V_+ = 15V$  D.C.,  $V_- = 15V$  D.C.,  $T_A = +25^\circ C$  Unless Otherwise Stated.

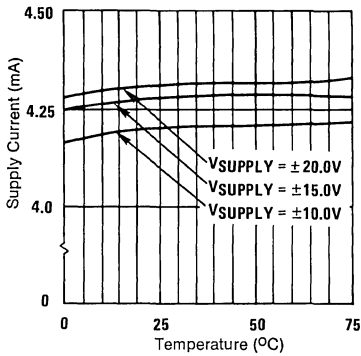
**INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE**



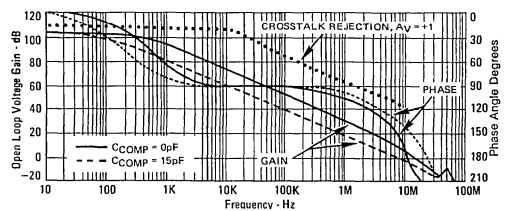
**NORMALIZED A. C. PARAMETERS vs TEMPERATURE**



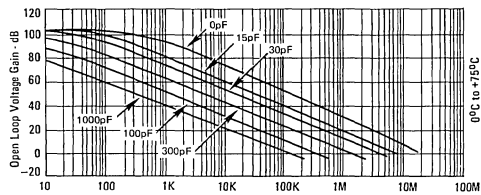
**POWER SUPPLY CURRENT DRAIN AS A FUNCTION OF TEMPERATURE**



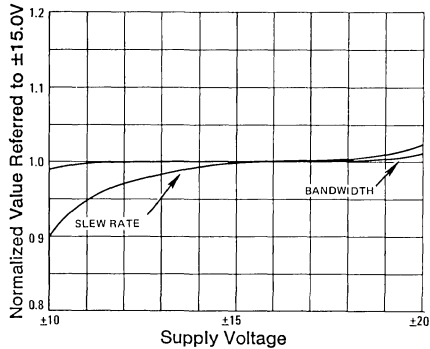
**OPEN LOOP FREQUENCY AND PHASE RESPONSE**



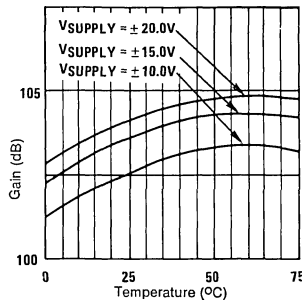
**FREQUENCY RESPONSE vs CCOMP**



**NORMALIZED A. C. PARAMETERS vs SUPPLY VOLTAGE**



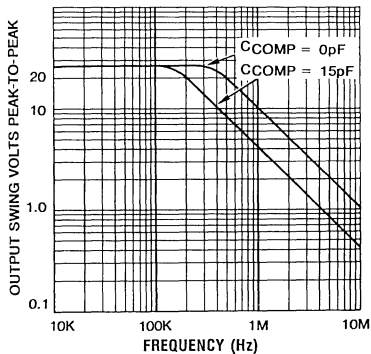
**OPEN LOOP VOLTAGE GAIN vs TEMPERATURE**



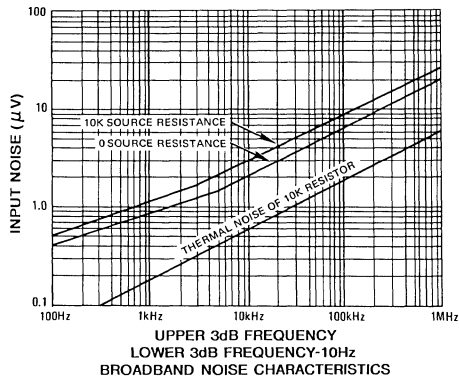


**Typical Performance Curves (Continued)**

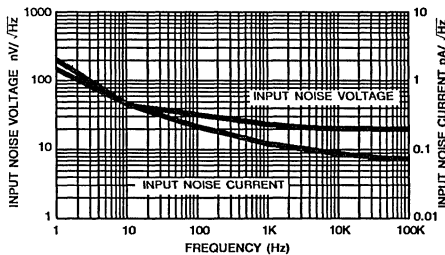
**OUTPUT VOLTAGE SWING vs FREQUENCY**



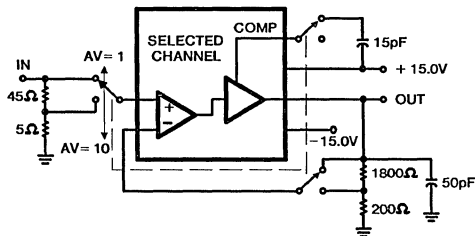
**EQUIVALENT INPUT NOISE vs BANDWIDTH**



**INPUT NOISE vs FREQUENCY**

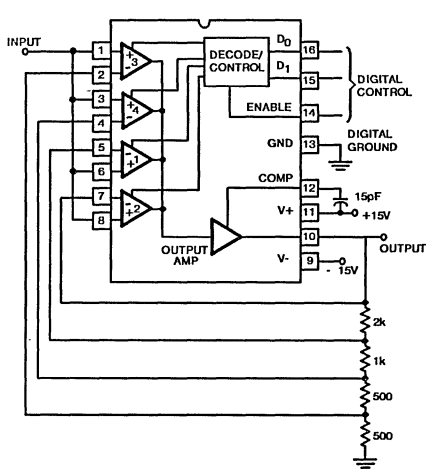


**SLEW RATE AND TRANSIENT RESPONSE**

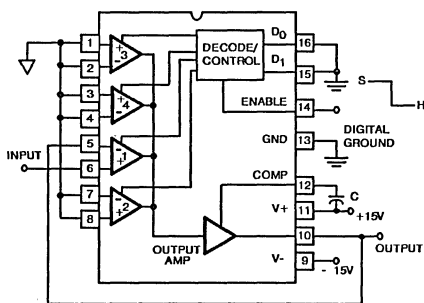


**Typical Applications**

**HA-2406  
AMPLIFIER, NON-INVERTING  
PROGRAMMABLE GAIN**



**HA-2406  
SAMPLE AND HOLD**



$$\begin{aligned} \text{Sample charging rate} &= \frac{I1}{C} \text{ V/sec.} & I1 &\approx 150 \times 10^{-6} \text{ A} \\ \text{Hold drift rate} &= \frac{I2}{C} \text{ V/sec.} & I2 &\approx 200 \times 10^{-9} \text{ A at } +25^\circ\text{C} \\ & & &\approx 600 \times 10^{-9} \text{ A at } -55^\circ\text{C} \\ & & &\approx 100 \times 10^{-9} \text{ A at } +125^\circ\text{C} \\ \text{Switch pedestal error} &= \frac{Q}{C} \text{ Volts} & Q &\approx 2 \times 10^{-12} \text{ Coul.} \end{aligned}$$

For more examples, see Harris Application Note 514.

August 1991

### Features

- Digital Selection of Input Channel
- Unity Gain Stability
- Gain Flatness @ 10MHz..... 0.1dB
- Differential Gain ..... 0.03%
- Differential Phase ..... 0.03°
- Fast Channel Selection ..... 60ns
- Crosstalk Rejection ..... 60dB

### Applications

- Video Multiplexer
- Programmable Gain Amplifier
- Special Effects Processors
- Video Distribution Systems
- Heads-up/Night Vision Displays
- Medical Imaging Systems
- Radar Video

### Description

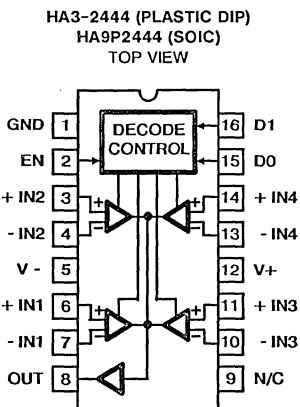
The HA-2444 is a channel-selectable video op amp consisting of four differential inputs, a single-ended output, and digital control circuitry allowing two digital inputs to activate one of the four differential inputs. The HA-2444 also includes a high impedance output state allowing the outputs of multiple HA-2444s to be wire-OR'd. Functionally, the HA-2444 is equivalent to four wideband video op amps and a wideband multiplexer.

Unlike similar competitor devices, the HA-2444 is not restricted to multiplexing. Any op amp configuration can be used with any of the inputs. Signal amplification, addition, integration, and more can be put under digital control with broadcast quality performance.

The key video parameters of the HA-2444 have been optimized without compromising dc performance. Gain Flatness, at 10MHz, is only 0.1dB. Differential gain and phase are typically 0.03% and 0.03 degrees, respectively. Laser trimming allows offset voltages in the 4.0mV range and a unique common current source design assures minimal channel-to-channel mismatch, while maintaining 60dB of crosstalk rejection at 5MHz. Open loop gain of 76dB and low input offset and bias currents enhance the performance of this versatile device.

For information about military grade devices, please refer to the HA-2444/883 data sheet. The HA-2444/883 devices are offered in Ceramic DIP and Ceramic Flatpack packages.

### Pinout



### Logic Operation

TRUTH TABLE

| EN | D1 | D0 | SELECTED CHANNEL                           |
|----|----|----|--|
| H  | L  | L  | 1  |
| H  | L  | H  | 2  |
| H  | H  | L  | 3  |
| H  | H  | H  | 4  |
| L  | X  | X  | NONE-OUT is set to a high impedance state. |

L = Low State (0.8V Max.)

H = High State (2.4V Min.)

X = Don't Care

## Specifications HA-2444

### Absolute Maximum Ratings (Note 1)

|   |                     |
|---|---------------------|
| Voltage Between V+ and V- Terminals .....             | 35V ( $\pm 17.5$ V) |
| Differential Input Voltage .....                      | $\pm 6$ V           |
| Peak (Short Duration) Output Current .....            | $\pm 40$ mA         |
| Maximum Junction Temperature .....                    | +175°C              |
| Maximum Junction Temperature (Plastic Packages) ..... | +150°C              |

### Operating Temperature Range

|                                 |  |
|---------------------------------|--|
| HA-2444-5 .....                 | $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$    |
| HA-2444-9 .....                 | $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  |
| Storage Temperature Range ..... | $-65^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ |
| Thermal Package Characteristics | $\theta_{jc}$ $\theta_{ja}$                              |
| 16 Pin Plastic DIP              | 27                      88                               |
| 16 Pin SOIC                     | 26                      96                               |

**Electrical Specifications** V+ = +15V, V- = -15V, R<sub>L</sub> = 1K, C<sub>L</sub> = 10pF, V<sub>IL</sub> = 0.8V, V<sub>IH</sub> = 2.4V. Unless Otherwise Specified. Specifications Apply to All Channels.

| PARAMETER  | TEMP  | HA-2444-5, -9 |            |     | UNITS                          |
|--|-------|---------------|------------|-----|--------------------------------|
|  |       | MIN           | TYP        | MAX |                                |
| <b>INPUT CHARACTERISTICS</b>                                   |       |               |            |     |                                |
| Input Offset Voltage   | +25°C | -             | 4          | 7   | mV                             |
|  | Full  | -             | -          | 15  | mV                             |
| Average Input Offset Voltage Drift                             | Full  | -             | 10         | -   | $\mu\text{V}/^{\circ}\text{C}$ |
| Channel to Channel Offset Voltage Mismatch                     | +25°C | -             | -          | 5   | mV                             |
|  | Full  | -             | -          | 8   | mV                             |
| Input Bias Current   | +25°C | -             | 9          | 15  | $\mu\text{A}$                  |
|  | Full  | -             | -          | 20  | $\mu\text{A}$                  |
| Average Input Bias Current Drift                               | Full  | -             | 0.04       | -   | $\mu\text{A}/^{\circ}\text{C}$ |
| Input Offset Current   | +25°C | -             | 2          | 4   | $\mu\text{A}$                  |
|  | Full  | -             | -          | 6   | $\mu\text{A}$                  |
| Average Input Offset Current Drift                             | Full  | -             | 10         | -   | $\text{nA}/^{\circ}\text{C}$   |
| Common Mode Range.   | Full  | -             | $\pm 11.5$ | -   | V                              |
| Differential Input Resistance (Note 16)                        | +25°C | 50            | 90         | -   | K $\Omega$                     |
| Differential Input Capacitance                                 | +25°C | -             | 3          | -   | pF                             |
| Input Noise Voltage Density    fo = 1000Hz                     | +25°C | -             | 26         | -   | $\text{nV}/\sqrt{\text{Hz}}$   |
| Input Noise Current Density    fo = 1000Hz                     | +25°C | -             | 4          | -   | $\text{pA}/\sqrt{\text{Hz}}$   |
| <b>TRANSFER CHARACTERISTICS</b>                                |       |               |            |     |                                |
| Large Signal Voltage Gain (Note 3)                             | +25°C | 71            | 76         | -   | dB                             |
|  | Full  | 68            | -          | -   | dB                             |
| Common Mode Rejection Ratio (Note 4)                           | Full  | 70            | 80         | -   | dB                             |
| Minimum Stable Gain  | +25°C | +1            | -          | -   | V/V                            |
| Unity Gain Bandwidth (Notes 2, 5)                              | +25°C | -             | 45         | -   | MHz                            |
| Gain Bandwidth Product (Note 5)                                | +25°C | -             | 50         | -   | MHz                            |
| Phase Margin (Note 2)  | +25°C | -             | 65         | -   | Degrees                        |
| Gain Margin (Note 2)   | +25°C | -             | 8.0        | -   | dB                             |
| <b>OUTPUT CHARACTERISTICS</b>                                  |       |               |            |     |                                |
| Output Voltage Swing (R <sub>L</sub> = 1K $\Omega$ )           | Full  | $\pm 10$      | $\pm 11$   | -   | V                              |
| Output Voltage Swing (R <sub>L</sub> = 75 $\Omega$ ) (Note 16) | +25°C | $\pm 2$       | -          | -   | V                              |
| Full Power Bandwidth (Note 6)                                  | Full  | 3.8           | 5.1        | -   | MHz                            |
| Output Current (Note 17)                                       | Full  | $\pm 25$      | -          | -   | mA                             |
| Disabled Output Current (Note 18)                              | Full  | -             | -          | 860 | $\mu\text{A}$                  |
| Output Resistance  | +25°C | -             | 20         | -   | $\Omega$                       |
| <b>TRANSIENT RESPONSE</b>                                      |       |               |            |     |                                |
| Rise Time (Notes 2, 7)   | +25°C | -             | 7          | -   | ns                             |
| Overshoot (Notes 2, 7)   | +25°C | -             | 10         | -   | %                              |
| Slew Rate (Notes 2, 9)   | Full  | 120           | 160        | -   | V/ $\mu\text{s}$               |
| Settling Time to 0.1% of $\pm 10$ V Output (Note 8)            | +25°C | -             | 120        | -   | ns                             |

## Specifications HA-2444

**Electrical Specifications**  $V_+ = +15V$ ,  $V_- = -15V$ ,  $R_L = 1K$ ,  $C_L = 10pF$ ,  $V_{IL} = 0.8V$ ,  $V_{IH} = 2.4V$ . Unless Otherwise Specified. Specifications Apply to All Channels.

| PARAMETER                                  | TEMP                | HA-2444-5, -9 |      |     | UNITS   |
|--|---------------------|---------------|------|-----|---------|
|  |                     | MIN           | TYP  | MAX |         |
| <b>SWITCHING CHARACTERISTICS</b>           |                     |               |      |     |         |
| Channel Select Time (Note 10)              | 0 to +85°C          | -             | 60   | 100 | ns      |
|  | -40 to 0°C          | -             | 80   | 125 | ns      |
| Output Enable Time (Note 11)               | Full                | -             | 40   | 100 | ns      |
| Digital Input Voltages                     | $V_{IH}$            | Full          | 2.4  | -   | V       |
|  | $V_{IL}$            | Full          | -    | 0.8 | V       |
| DO/D1 Input Current                        | ( $V_{IL} = 0.0V$ ) | Full          | -    | 0.7 | mA      |
|  | ( $V_{IH} = 5.0V$ ) | Full          | -    | 1.2 | μA      |
| EN Input Current                           | ( $V_{IL} = 0.0V$ ) | Full          | -    | 50  | μA      |
|  | ( $V_{IH} = 5.0V$ ) | Full          | -    | 1.2 | μA      |
| Crosstalk Rejection (Note 12)              | +25°C               | -             | 60   | -   | dB      |
| <b>VIDEO PARAMETERS</b>                    |                     |               |      |     |         |
| Differential Phase (Note 14)               | +25°C               | -             | 0.03 | -   | Degrees |
| Differential Gain (Note 14)                | +25°C               | -             | 0.03 | -   | %       |
| Gain Flatness (Notes 2, 13) (10MHz)        | +25°C               | -             | 0.1  | -   | dB      |
| Chrominance to Luminance Gain (Note 14)    | +25°C               | -             | 0.1  | -   | dB      |
| Chrominance to Luminance Delay (Note 14)   | +25°C               | -             | 7    | -   | ns      |
| <b>POWER SUPPLY</b>                        |                     |               |      |     |         |
| $I_{CC}$                                   | Full                | -             | 20   | 25  | mA      |
| $I_{EE}$                                   | Full                | -             | 20   | 25  | mA      |
| Supply Current (Output Disabled) (Note 19) | Full                | -             | -    | 10  | mA      |
| PSRR (Note 15)                             | Full                | 65            | 80   | -   | dB      |

**NOTES:**

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2.  $A_V = +1$ .
3.  $V_{OUT} = \pm 5V$ .
4.  $V_{CM} = \pm 5V$ .
5.  $V_{OUT} = \pm 100mV$ .
6. Full Power Bandwidth is calculated by:  

$$FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}} \quad V_{PEAK} = 5V$$
7.  $V_{OUT} = 0$  to  $\pm 200mV$ .
8. Settling time to 0.1% with a 10V step. Specified with the channel pre-selected and the output stage enabled.  $A_V = -1$ .
9.  $V_{OUT} = -5V$  to  $+5V$  or  $+5V$  to  $-5V$ .
10. The time required for an enabled HA-2444 to switch from one input channel to another. Measured from the 50% point of the digital input to 50% of the output.  $A_V = +1$  for all channels.  $V_{OUT}$  switches from 0V to 5V.
11. The time required to enable the output with a channel preselected. Measured from the 50% point of the Enable input to 4V on the output.  $A_V = +1$  for all channels.  $V_{IN} = 5V$  for the selected channel.
12.  $V_{IN} = 5V_p-p$ ,  $f_o = 5MHz$ , for one of the 3 unselected channels.  $V_{IN} = 0$  for the selected channel.  $A_V = +1$  for all channels.
13.  $V_{IN} = 200mV_{RMS}$ .
14. Tested with a VM700A video tester using a NTC-7 Composite input signal.
15.  $V_S = \pm 15V$  to  $\pm 20V$ .
16. These parameters are not tested. The limits are guaranteed based on lab characterization and reflect lot to lot variation.
17.  $V_{OUT} = \pm 10V$ ,  $V_{EN} = 2.4V$ , 50% Duty Cycle max.
18.  $V_{OUT} = \pm 5V$ ,  $V_{EN} = 0.8V$ .
19. Applies to  $I_{CC}$  and  $I_{EE}$ .  $V_{OUT} = 0V$ ,  $V_{EN} = 0.8V$ .

**3**  
OPERATIONAL AMPLIFIERS

## Precision High Slew Rate Operational Amplifiers

August 1991

### Features

- High Slew Rate ..... 30V/ $\mu$ s
- Fast Settling ..... 330ns
- Wide Power Bandwidth ..... 500KHz
- High Gain Bandwidth ..... 12MHz
- High Input Impedance ..... 50M $\Omega$
- Low Offset Current ..... 10nA
- Internally Compensated For Unity Gain Stability

### Description

HA-2500/2502/2505 comprises a series of monolithic operational amplifiers whose designs are optimized to deliver excellent slew rate, bandwidth, and settling time specifications. The outstanding dynamic features of this internally compensated device are complemented with low offset voltage and offset current.

These dielectrically isolated amplifiers are ideally suited for applications such as data acquisition, R.F., video, and pulse conditioning circuits. Slew rates of  $\pm 30\text{V}/\mu\text{s}$  and 330ns (0.1%) settling time make these devices excellent components in fast, accurate data acquisition and pulse amplification designs. 12MHz small signal bandwidth and 500kHz power bandwidth make these devices well suited to R.F. and video applications. With 2mV typical offset voltage plus offset trim capability and 10nA offset current,

### Applications

- Data Acquisition Systems
- R.F. Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

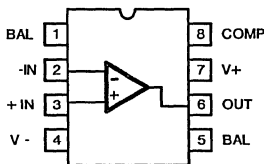
HA-2500/2502/2505 are particularly useful components in signal conditioning designs.

The gain and offset voltage figures of the HA-2500 series are optimized by internal component value changes while the similar design of the HA-2510 series is maximized for slew rate.

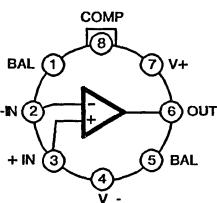
The HA-2500 and HA-2502 have guaranteed operation from  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  and are available in Hermetic Metal Can and Ceramic Mini-DIP packages. Both are offered as a /883 military grade part with the HA-2502 also available in LCC package. The HA-2505 has guaranteed operation from  $0^{\circ}\text{C}$  to  $+75^{\circ}\text{C}$  and is available in Plastic and Ceramic Mini-DIP and Metal Can packages. Mil-Std-883 product and data sheets are available upon request.

### Pinouts

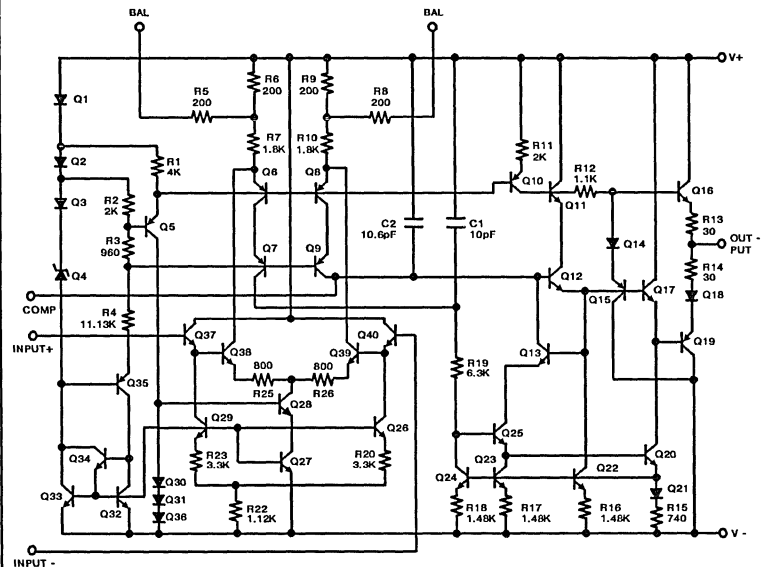
HA7-2500/02/05  
(CERAMIC MINI-DIP)  
HA3-2505 (PLASTIC MINI-DIP)  
TOP VIEW



HA2-2500/02/05  
(TO-99 METAL CAN)  
TOP VIEW



### Schematic



## Specifications HA-2500/2502/2505

### Absolute Maximum Ratings (Note 6)

|  |        |
|--|--------|
| Voltage Between V+ and V- Terminals .....  | 40.0V  |
| Differential Input Voltage .....           | ±15.0V |
| Peak Output Current .....                  | 50mA   |
| Internal Power Dissipation .....           | 300mW  |
| Lead Solder Temperature (10 Seconds) ..... | +275°C |

### Operating Temperature Range

|                                    |                                 |
|------------------------------------|---------------------------------|
| HA-2500/2502-2 .....               | -55°C ≤ T <sub>A</sub> ≤ +125°C |
| HA-2505-5 .....                    | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| HA-2505-9 .....                    | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| Storage Temperature Range .....    | -65°C ≤ T <sub>A</sub> ≤ +150°C |
| Maximum Junction Temperature ..... | +175°C                          |

### Electrical Specifications V+ = +15V DC, V- = -15V DC

| PARAMETER                                  | TEMP. | HA-2500-2 |       |     | HA-2502-2 |       |     | HA-2505-5, -9 |       |     | UNITS |
|--|-------|-----------|-------|-----|-----------|-------|-----|---------------|-------|-----|-------|
|  |       | MIN       | TYP   | MAX | MIN       | TYP   | MAX | MIN           | TYP   | MAX |       |
| <b>INPUT CHARACTERISTICS</b>               |       |           |       |     |           |       |     |               |       |     |       |
| Offset Voltage                             | +25°C | -         | 2     | 5   | -         | 4     | 8   | -             | 4     | 8   | mV    |
|  | Full  | -         | -     | 8   | -         | -     | 10  | -             | -     | 10  | mV    |
| Offset Voltage Average Drift               | Full  | -         | 20    | -   | -         | 20    | -   | -             | 20    | -   | μV/°C |
| Bias Current                               | +25°C | -         | 100   | 200 | -         | 125   | 250 | -             | 125   | 250 | nA    |
|  | Full  | -         | -     | 400 | -         | -     | 500 | -             | -     | 500 | nA    |
| Offset Current                             | +25°C | -         | 10    | 25  | -         | 20    | 50  | -             | 20    | 50  | nA    |
|  | Full  | -         | -     | 50  | -         | -     | 100 | -             | -     | 100 | nA    |
| Input Resistance (Note 10)                 | +25°C | 25        | 50    | -   | 20        | 50    | -   | 20            | 50    | -   | MΩ    |
| Common Mode Range                          | Full  | ±10.0     | -     | -   | ±10.0     | -     | -   | ±10.0         | -     | -   | V     |
| <b>TRANSFER CHARACTERISTICS</b>            |       |           |       |     |           |       |     |               |       |     |       |
| Large Signal Voltage Gain (Note 1, 4)      | +25°C | 20K       | 30K   | -   | 15K       | 25K   | -   | 15K           | 25K   | -   | V/V   |
|  | Full  | 15K       | -     | -   | 10K       | -     | -   | 10K           | -     | -   | V/V   |
| Common Mode Rejection Ratio (Note 2)       | Full  | 80        | 90    | -   | 74        | 90    | -   | 74            | 90    | -   | dB    |
| Gain Bandwidth Product (Note 3)            | +25°C | -         | 12    | -   | -         | 12    | -   | -             | 12    | -   | MHz   |
| <b>OUTPUT CHARACTERISTICS</b>              |       |           |       |     |           |       |     |               |       |     |       |
| Output Voltage Swing (Note 1)              | Full  | ±10.0     | ±12.0 | -   | ±10.0     | ±12.0 | -   | ±10.0         | ±12.0 | -   | V     |
| Output Current (Note 4)                    | +25°C | ±10       | ±20   | -   | ±10       | ±20   | -   | ±10           | ±20   | -   | mA    |
| Full Power Bandwidth (Notes 4, 11)         | +25°C | 350       | 500   | -   | 300       | 500   | -   | 300           | 500   | -   | KHz   |
| <b>TRANSIENT RESPONSE</b>                  |       |           |       |     |           |       |     |               |       |     |       |
| Rise Time (Notes 1, 5, 7 & 8)              | +25°C | -         | 25    | 50  | -         | 25    | 50  | -             | 25    | 50  | ns    |
| Overshoot (Notes 1, 5, 7 & 8)              | +25°C | -         | 25    | 40  | -         | 25    | 50  | -             | 25    | 50  | %     |
| Slew Rate (Notes 1, 5, 8 & 12)             | +25°C | ±25       | ±30   | -   | ±20       | ±30   | -   | ±20           | ±30   | -   | V/μs  |
| Settling Time to 0.1% (Notes 1, 5, 8 & 12) | +25°C | -         | 0.33  | -   | -         | 0.33  | -   | -             | 0.33  | -   | μs    |
| <b>POWER SUPPLY CHARACTERISTICS</b>        |       |           |       |     |           |       |     |               |       |     |       |
| Supply Current                             | +25°C | -         | 4     | 6   | -         | 4     | 6   | -             | 4     | 6   | mA    |
| Power Supply Rejection Ratio (Note 9)      | Full  | 80        | 90    | -   | 74        | 90    | -   | 74            | 90    | -   | dB    |

#### NOTES:

1. R<sub>L</sub> = 2KΩ
2. V<sub>CM</sub> = ±10V
3. A<sub>V</sub> > 10
4. V<sub>O</sub> = ±10.0V
5. C<sub>L</sub> = 50pF
6. Absolute Maximum Ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired.
7. V<sub>O</sub> = ±200mV
8. See Transient Response Test Circuits and Waveforms.
9. ΔV = ±5.0V
10. This parameter value is based on design calculations.
11. Full Power Bandwidth guaranteed based on slew rate measurement using:  
FPBW = S.R./2πV<sub>peak</sub>.
12. V<sub>OUT</sub> = ±5V.

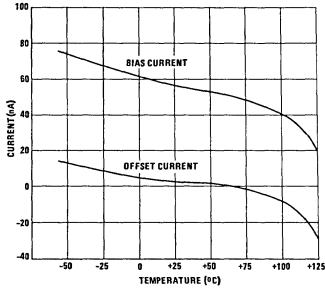
3

OPERATIONAL AMPLIFIERS

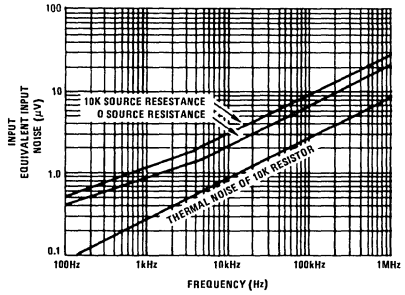
# HA-2500/2502/2505

**Performance Curves**  $V_{+} = +15\text{VDC}$ ,  $V_{-} = -15\text{VDC}$ ,  $T_A = +25^{\circ}\text{C}$ , Unless Otherwise Stated

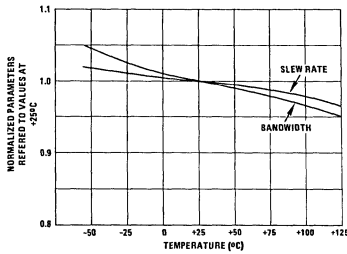
## INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



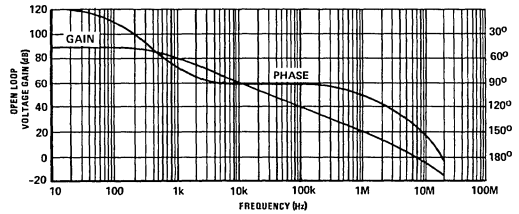
## EQUIVALENT INPUT NOISE vs. BANDWIDTH (With 10Hz High Pass Filter)



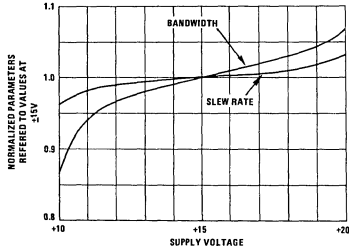
## NORMALIZED AC PARAMETERS vs. TEMPERATURE



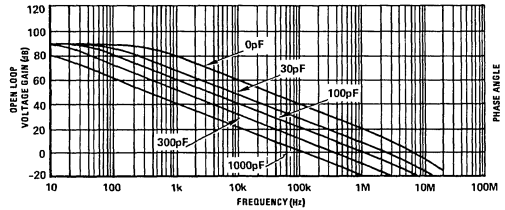
## OPEN-LOOP FREQUENCY AND PHASE RESPONSE



## NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE AT +25°C

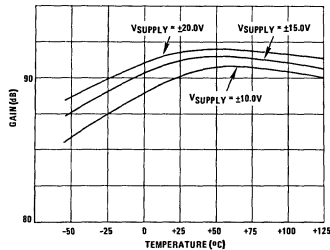


## OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

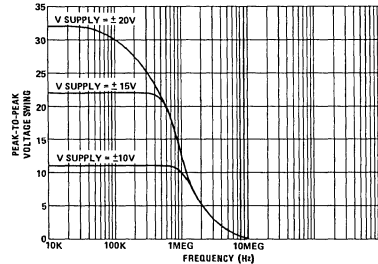


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

## OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE

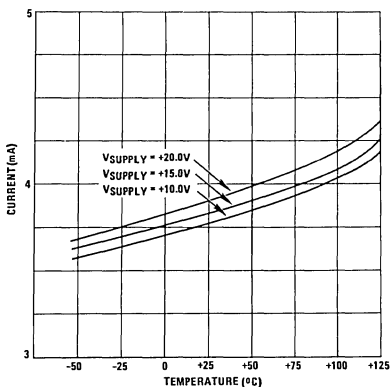


## OUTPUT VOLTAGE SWING vs. FREQUENCY AT +25°C

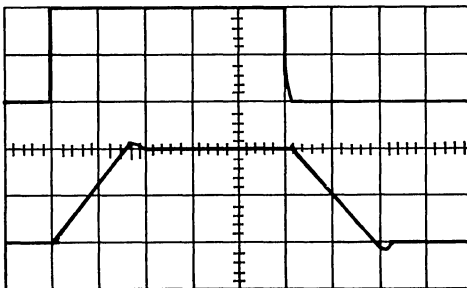


Typical Performance Curves (Continued)

POWER SUPPLY CURRENT vs TEMPERATURE



VOLTAGE FOLLOWER PULSE RESPONSE

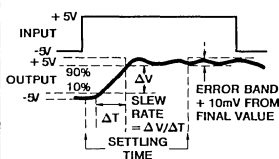


$R_L = 2K\Omega$ ,  $C_L = 50pF$   
Upper Trace: Input  
Lower Trace: Output

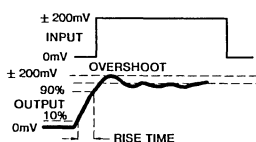
Vertical = 5V/Div.  
Horizontal = 200ns/Div.  
 $T_A = +25^\circ C$ ,  $V_S = \pm 15.0V$

Test Circuits

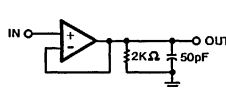
SLEW RATE AND SETTLING TIME



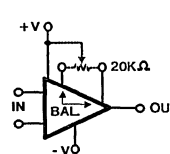
TRANSIENT RESPONSE



SLEW RATE AND TRANSIENT RESPONSE



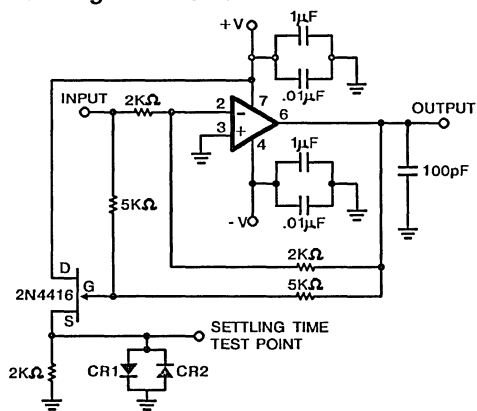
SUGGESTED  $V_{OS}$  ADJUSTMENT



NOTE: Measured on Both Positive and Negative Transitions from 0V to +200mV and 0V to -200mV at the output.

Tested Offset Adjustment Range is  $|V_{OS} + 1mV|$  minimum referred to output. Typical ranges are  $\pm 6mV$  with  $R_T = 20k\Omega$ .

Settling Time Circuit



- $A_V = -1$
- Feedback and Summing Resistor Ratios Should be 0.1% matched.
- Clipping Diodes CR1 and CR2 are Optional. HP5082-2810 Recommended.

Die Characteristics

|                                    |                   |               |
|------------------------------------|-------------------|---------------|
| Transistor Count                   | 40                |               |
| Die Dimensions                     | 57 x 65 x 19 mils |               |
| Substrate Potential                | Unbiased          |               |
| Process                            | Bipolar-DI        |               |
| Thermal Constants ( $^\circ C/W$ ) | $\theta_{ja}$     | $\theta_{jc}$ |
| HA2-Metal Can (-2, -5, -7)         | 202               | 56            |
| HA2-Metal Can (-8, /883)           | 168               | 52            |
| HA3-Plastic Mini-DIP (-5)          | 84                | 34            |
| HA4-Ceramic LCC (/883)             | 97                | 35            |
| HA7-Ceramic Mini-DIP (-8, /883)    | 138               | 63            |
| HA7-Ceramic Mini-DIP (-2, -5, -7)  | 204               | 112           |



August 1991

### Features

- High Slew Rate ..... 60V/ $\mu$ s
- Fast Settling ..... 250ns
- Wide Power Bandwidth ..... 1,000kHz
- High Gain Bandwidth ..... 12MHz
- High Input Impedance ..... 100M $\Omega$
- Low Offset Current ..... 10nA
- Internally Compensated For Unity Gain Stability

### Description

HA-2510/2512/2515 are a series of high performance operational amplifiers which set the standards for maximum slew rate, highest accuracy and widest bandwidths for internally compensated monolithic devices. In addition to excellent dynamic characteristics, these dielectrically isolated amplifiers also offer low offset current and high input impedance.

The  $\pm 60\text{V}/\mu\text{s}$  slew rate and 250ns (0.1%) settling time of these amplifiers is ideally suited for high speed D/A, A/D, and pulse amplification designs. HA-2510/2512/2515's superior 12MHz gain bandwidth and 1000kHz power-bandwidth is extremely useful in R.F. and video applications. For accurate

### Applications

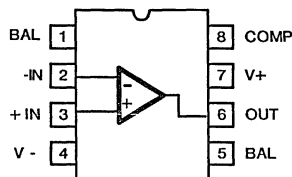
- Data Acquisition Systems
- R.F. Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

signal conditioning these amplifiers also provide 10nA offset current, coupled with 100M $\Omega$  input impedance, and offset trim capability.

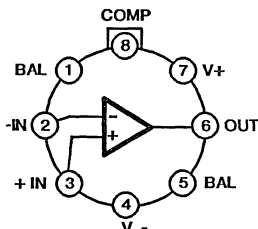
The HA-2510 and HA-2512 have guaranteed operation from  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  and are available in Metal Can and Ceramic Mini-DIP packages. Both are offered as a /883 military grade part with the HA-2512 also available in LCC package. The HA-2515 has guaranteed operation from  $0^{\circ}\text{C}$  to  $+75^{\circ}\text{C}$  and is available in Plastic and Ceramic Mini-DIP and Metal Can packages. Mil-Std-883 product and data sheets are available upon request.

### Pinouts

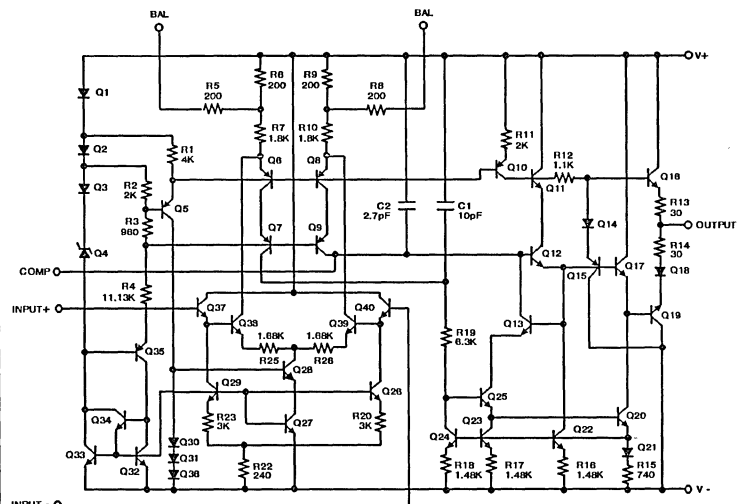
HA7-2510/12/15  
(CERAMIC MINI-DIP)  
HA3-2515 (PLASTIC MINI-DIP)  
TOP VIEW



HA2-2510/12/15  
(TO-99 METAL CAN)  
TOP VIEW



### Schematic



## Specifications HA-2510/2512/2515

### Absolute Maximum Ratings (Note 6)

|  |        |
|--|--------|
| Voltage Between V+ and V- Terminals .....  | 40.0V  |
| Differential Input Voltage .....           | ±15.0V |
| Peak Output Current .....                  | 50mA   |
| Internal Power Dissipation .....           | 300mW  |
| Lead Solder Temperature (10 Seconds) ..... | +275°C |

### Operating Temperature Range

|                                    |                                 |
|------------------------------------|---------------------------------|
| HA-2510/2512-2 .....               | -55°C ≤ T <sub>A</sub> ≤ +125°C |
| HA-2515-5 .....                    | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| HA-2515-9 .....                    | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| Storage Temperature Range .....    | -65°C ≤ T <sub>A</sub> ≤ +150°C |
| Maximum Junction Temperature ..... | +175°C                          |

### Electrical Specifications V+ = +15V DC, V- = -15V DC

| PARAMETER                                  | TEMP. | HA-2510-2 |       |     | HA-2512-2 |       |     | HA-2515-5, -9 |       |     | UNITS |
|--|-------|-----------|-------|-----|-----------|-------|-----|---------------|-------|-----|-------|
|  |       | MIN       | TYP   | MAX | MIN       | TYP   | MAX | MIN           | TYP   | MAX |       |
| <b>INPUT CHARACTERISTICS</b>               |       |           |       |     |           |       |     |               |       |     |       |
| Offset Voltage                             | +25°C | -         | 4     | 8   | -         | 5     | 10  | -             | 5     | 10  | mV    |
|  | Full  | -         | -     | 11  | -         | -     | 14  | -             | -     | 14  | mV    |
| Offset Voltage Average Drift               | Full  | -         | 20    | -   | -         | 25    | -   | -             | 30    | -   | μV/°C |
| Bias Current                               | +25°C | -         | 100   | 200 | -         | 125   | 250 | -             | 125   | 250 | nA    |
|  | Full  | -         | -     | 400 | -         | -     | 500 | -             | -     | 500 | nA    |
| Offset Current                             | +25°C | -         | 10    | 25  | -         | 20    | 50  | -             | 20    | 50  | nA    |
|  | Full  | -         | -     | 50  | -         | -     | 100 | -             | -     | 100 | nA    |
| Input Resistance (Note 10)                 | +25°C | 50        | 100   | -   | 40        | 100   | -   | 40            | 100   | -   | MΩ    |
| Common Mode Range                          | Full  | ±10.0     | -     | -   | ±10.0     | -     | -   | ±10.0         | -     | -   | V     |
| <b>TRANSFER CHARACTERISTICS</b>            |       |           |       |     |           |       |     |               |       |     |       |
| Large Signal Voltage Gain (Note 1, 4)      | +25°C | 10K       | 15K   | -   | 7.5K      | 15K   | -   | 7.5K          | 15K   | -   | V/V   |
|  | Full  | 7.5K      | -     | -   | 5K        | -     | -   | 5K            | -     | -   | V/V   |
| Common Mode Rejection Ratio (Note 2)       | Full  | 80        | 90    | -   | 74        | 90    | -   | 74            | 90    | -   | dB    |
| Gain Bandwidth Product (Note 3)            | +25°C | -         | 12    | -   | -         | 12    | -   | -             | 12    | -   | MHz   |
| <b>OUTPUT CHARACTERISTICS</b>              |       |           |       |     |           |       |     |               |       |     |       |
| Output Voltage Swing (Note 1)              | Full  | ±10.0     | ±12.0 | -   | ±10.0     | ±12.0 | -   | ±10.0         | ±12.0 | -   | V     |
| Output Current (Note 4)                    | +25°C | ±10       | ±20   | -   | ±10       | ±20   | -   | ±10           | ±20   | -   | mA    |
| Full Power Bandwidth (Notes 4, 11)         | +25°C | 750       | 1000  | -   | 600       | 1000  | -   | 600           | 1000  | -   | kHz   |
| <b>TRANSIENT RESPONSE</b>                  |       |           |       |     |           |       |     |               |       |     |       |
| Rise Time (Notes 1, 5, 7 & 8)              | +25°C | -         | 25    | 50  | -         | 25    | 50  | -             | 25    | 50  | ns    |
| Overshoot (Notes 1, 5, 7 & 8)              | +25°C | -         | 25    | 40  | -         | 25    | 50  | -             | 25    | 50  | %     |
| Slew Rate (Notes 1, 5, 8 & 12)             | +25°C | ±50       | ±65   | -   | ±40       | ±60   | -   | ±40           | ±60   | -   | V/μs  |
| Settling Time to 0.1% (Notes 1, 5, 8 & 12) | +25°C | -         | 0.25  | -   | -         | 0.25  | -   | -             | 0.25  | -   | μs    |
| <b>POWER SUPPLY CHARACTERISTICS</b>        |       |           |       |     |           |       |     |               |       |     |       |
| Supply Current                             | +25°C | -         | 4     | 6   | -         | 4     | 6   | -             | 4     | 6   | mA    |
| Power Supply Rejection Ratio (Note 9)      | Full  | 80        | 90    | -   | 74        | 90    | -   | 74            | 90    | -   | dB    |

#### NOTES:

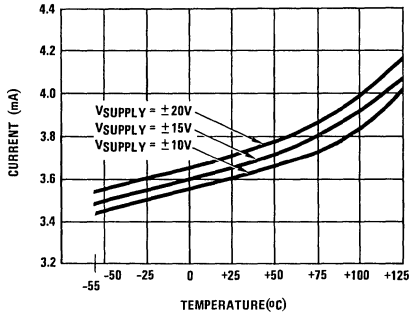
1. R<sub>L</sub> = 2KΩ
2. V<sub>CM</sub> = ±10V
3. A<sub>y</sub> > 10
4. V<sub>O</sub> = ±10.0V
5. C<sub>L</sub> = 50pF
6. Absolute Maximum Ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired.
7. V<sub>O</sub> = ±200mV
8. See Transient Response Test Circuits and Waveforms.
9. ΔV = ±5.0V
10. This parameter value is based on design calculations.
11. Full Power Bandwidth guaranteed based on slew rate measurement using: FPBW = S.R./2mVpeak.
12. V<sub>OUT</sub> = ±5V.

**3**

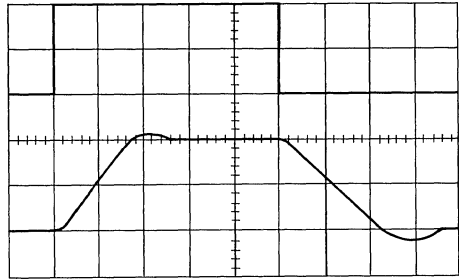
OPERATIONAL  
AMPLIFIERS

**Typical Performance Curves (Continued)**

**POWER SUPPLY CURRENT vs TEMPERATURE**



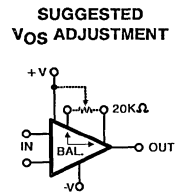
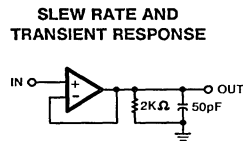
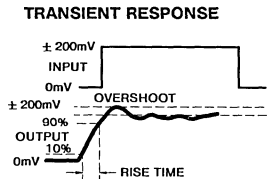
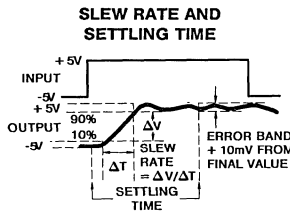
**VOLTAGE FOLLOWER PULSE RESPONSE**



$R_L = 2K\Omega$ ,  $C_L = 50pF$   
 Upper Trace: Input  
 Lower Trace: Output

Vertical = 5V/Div.  
 Horizontal = 200ns/Div.  
 $T_A = +25^\circ C$ ,  $V_S = \pm 15.0V$

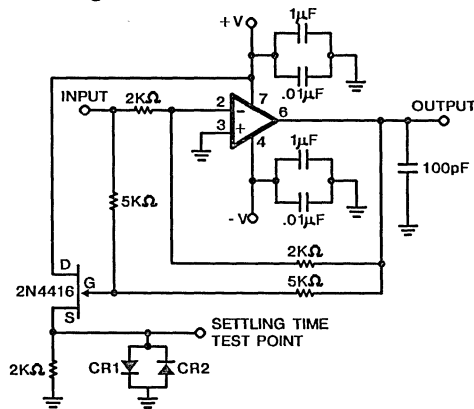
**Test Circuits**



NOTE: Measured on Both Positive and Negative Transitions from 0V to +200mV and 0V to -200mV at the output.

Tested Offset Adjustment Range is  $|V_{OS} + 1mV|$  minimum referred to output. Typical ranges are  $\pm 6mV$  with  $R_T = 20k\Omega$ .

**Settling Time Circuit**



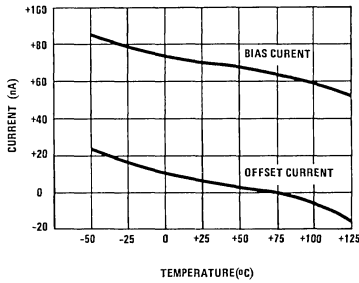
- $A_V = -1$
- Feedback and Summing Resistor Ratios Should be 0.1% matched.
- Clipping Diodes CR1 and CR2 are Optional. HP5082-2810 Recommended.

**Die Characteristics**

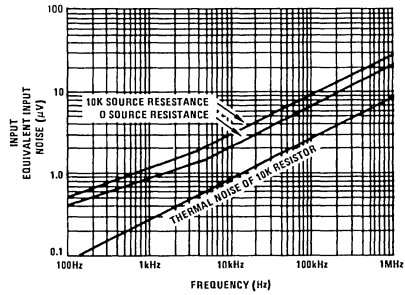
|                                   |                         |               |
|-----------------------------------|-------------------------|---------------|
| Transistor Count                  | ..... 40                |               |
| Die Dimensions                    | ..... 57 x 65 x 19 mils |               |
| Substrate Potential               | ..... Unbiased          |               |
| Process                           | ..... Bipolar-DI        |               |
| Thermal Constants (°C/W)          | $\theta_{ja}$           | $\theta_{jc}$ |
| HA2-Metal Can (-2, -5, -7)        | 202                     | 56            |
| HA2-Metal Can (-8, /883)          | 168                     | 52            |
| HA3-Plastic Mini-DIP (-5)         | 84                      | 34            |
| HA4-Ceramic LCC (/883)            | 97                      | 35            |
| HA7-Ceramic Mini-DIP (-8, /883)   | 138                     | 63            |
| HA7-Ceramic Mini-DIP (-2, -5, -7) | 204                     | 112           |

**Performance Curves**  $V_+ = +15VDC$ ,  $V_- = -15VDC$ ,  $T_A = +25^\circ C$ , Unless Otherwise Stated

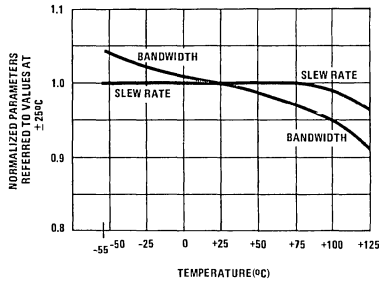
**INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE**



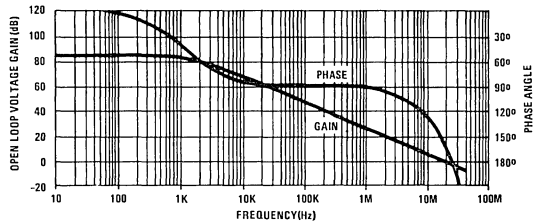
**EQUIVALENT INPUT NOISE vs. BANDWIDTH (With 10Hz High Pass Filter)**



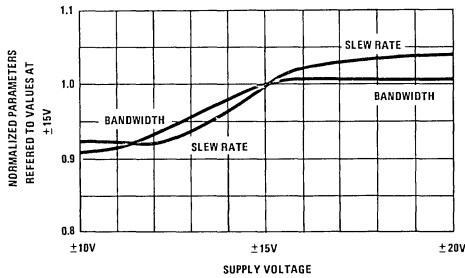
**NORMALIZED AC PARAMETERS vs. TEMPERATURE**



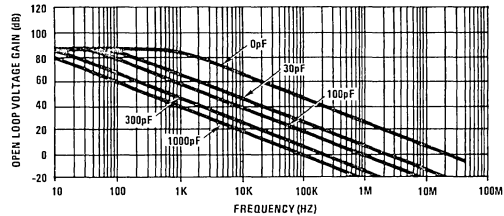
**OPEN-LOOP FREQUENCY AND PHASE RESPONSE**



**NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE AT +25°C**

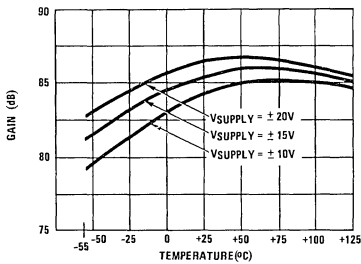


**OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND**

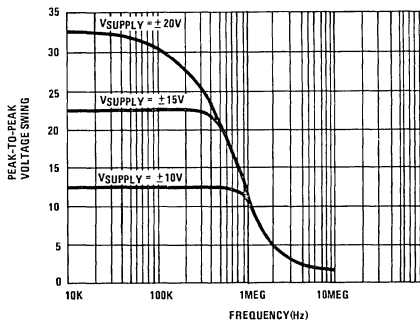


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

**OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE**



**OUTPUT VOLTAGE SWING vs. FREQUENCY AT +25°C**



## Uncompensated High Slew Rate Operational Amplifiers

August 1991

### Features

- High Slew Rate ..... 120V/ $\mu$ s
- Fast Settling ..... 200ns
- Wide Power Bandwidth ..... 2,000kHz
- High Gain Bandwidth ( $A_V \geq 3$ ) ..... 20MHz
- High Input Impedance ..... 100M $\Omega$
- Low Offset Current ..... 10nA

### Applications

- Data Acquisition Systems
- R.F. Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

### Description

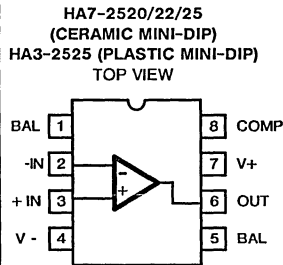
HA-2520/2522/2525 comprise a series of monolithic operational amplifiers delivering an unsurpassed combination of specifications for slew rate, bandwidth and settling time. These dielectrically isolated amplifiers are controlled at close loop gains greater than 3 without external compensation. In addition, these high performance components also provide low offset current and high input impedance.

120V/ $\mu$ s slew rate and 200ns (0.2%) settling time of these amplifiers make them ideal components for pulse amplification and data acquisition designs. These devices are valuable components for R.F. and video circuitry requiring up to 20MHz gain bandwidth and 2MHz power

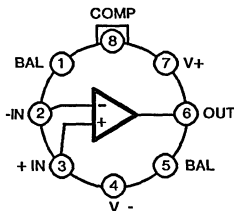
bandwidth. For accurate signal conditioning designs the HA-2520/2522/2525's superior dynamic specifications are complimented by 10nA offset current, 100M $\Omega$  input impedance and offset trim capability.

The HA-2520 and HA-2522 have guaranteed operation from  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  and are available in metal can and Ceramic Mini-DIP packages. Both are offered in /883 grade with the HA-2522 also available in LCC package. The HA-2525 has guaranteed operation from  $0^{\circ}\text{C}$  to  $+75^{\circ}\text{C}$  and is available in plastic and Ceramic Mini-DIP and metal can packages. Mil-Std-883 product and data sheets are available upon request.

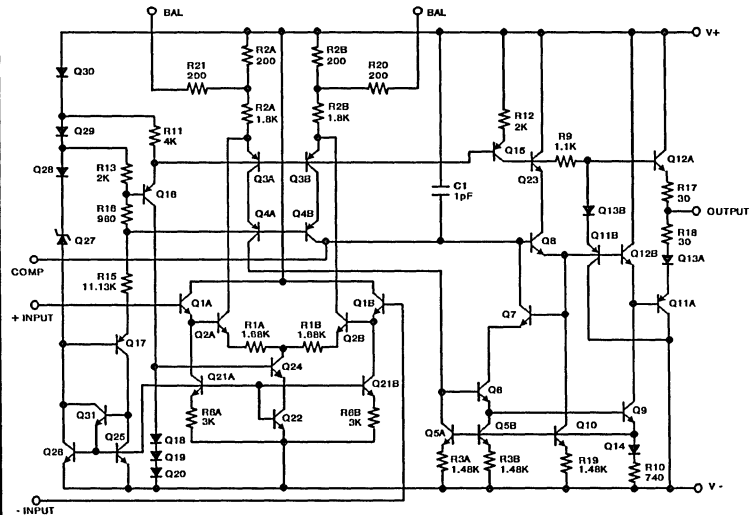
### Pinouts



HA2-2520/22/25  
(TO-99 METAL CAN)  
TOP VIEW



### Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.  
Copyright © Harris Corporation 1991

## Specifications HA-2520/2522/2525

### Absolute Maximum Ratings (Note 13)

|  |        |
|--|--------|
| Voltage Between V+ and V- Terminals .....  | 40.0V  |
| Differential Input Voltage .....           | ±15.0V |
| Peak Output Current .....                  | 50mA   |
| Internal Power Dissipation .....           | 300mW  |
| Lead Solder Temperature (10 Seconds) ..... | +275°C |

### Operating Temperature Range

|                                    |                                 |
|------------------------------------|---------------------------------|
| HA-2520/2522-2 .....               | -55°C ≤ T <sub>A</sub> ≤ +125°C |
| HA-2525-5 .....                    | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| HA-2525-9 .....                    | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| Storage Temperature Range .....    | -65°C ≤ T <sub>A</sub> ≤ +150°C |
| Maximum Junction Temperature ..... | +175°C                          |

### Electrical Specifications V+ = +15V DC, V- = -15V DC

| PARAMETER                                       | TEMP  | HA-2520-2 |       |     | HA-2522-2 |       |     | HA-2525-5, -9 |       |     | UNITS |
|---|-------|-----------|-------|-----|-----------|-------|-----|---------------|-------|-----|-------|
|   |       | MIN       | TYP   | MAX | MIN       | TYP   | MAX | MIN           | TYP   | MAX |       |
| <b>INPUT CHARACTERISTICS</b>                    |       |           |       |     |           |       |     |               |       |     |       |
| Offset Voltage                                  | +25°C | -         | 4     | 8   | -         | 5     | 10  | -             | 5     | 10  | mV    |
|   | Full  | -         | -     | 11  | -         | -     | 14  | -             | -     | 14  | mV    |
| Offset Voltage Drift                            | Full  | -         | 20    | -   | -         | 25    | -   | -             | 30    | -   | μV/°C |
| Bias Current                                    | +25°C | -         | 100   | 200 | -         | 125   | 250 | -             | 125   | 250 | nA    |
|   | Full  | -         | -     | 400 | -         | -     | 500 | -             | -     | 500 | nA    |
| Offset Current                                  | +25°C | -         | 10    | 25  | -         | 20    | 50  | -             | 20    | 50  | nA    |
|   | Full  | -         | -     | 50  | -         | -     | 100 | -             | -     | 100 | nA    |
| Input Resistance (Note 9)                       | +25°C | 50        | 100   | -   | 40        | 100   | -   | 40            | 100   | -   | MΩ    |
| Common Mode Range                               | Full  | ±10.0     | -     | -   | ±10.0     | -     | -   | ±10.0         | -     | -   | V     |
| <b>TRANSFER CHARACTERISTICS</b>                 |       |           |       |     |           |       |     |               |       |     |       |
| Large Signal Voltage Gain (Notes 1, 4)          | +25°C | 10K       | 15K   | -   | 7.5K      | 15K   | -   | 7.5K          | 15K   | -   | V/V   |
|   | Full  | 7.5K      | -     | -   | 5K        | -     | -   | 5K            | -     | -   | V/V   |
| Common Mode Rejection Ratio (Note 2)            | Full  | 80        | 90    | -   | 74        | 90    | -   | 74            | 90    | -   | dB    |
| Gain Bandwidth Product (Notes 3, 12)            | +25°C | 10        | 20    | -   | 10        | 20    | -   | 10            | 20    | -   | MHz   |
| <b>OUTPUT CHARACTERISTICS</b>                   |       |           |       |     |           |       |     |               |       |     |       |
| Output Voltage Swing (Note 1)                   | Full  | ±10.0     | ±12.0 | -   | ±10.0     | ±12.0 | -   | ±10.0         | ±12.0 | -   | V     |
| Output Current (Note 4)                         | +25°C | ±10       | ±20   | -   | ±10       | ±20   | -   | ±10           | ±20   | -   | mA    |
| Full Power Bandwidth (Notes 4, 10)              | +25°C | 1500      | 2000  | -   | 1200      | 2000  | -   | 1200          | 2000  | -   | kHz   |
| <b>TRANSIENT RESPONSE (A<sub>V</sub> = +3V)</b> |       |           |       |     |           |       |     |               |       |     |       |
| Rise Time (Notes 1, 5, 6 & 8)                   | +25°C | -         | 25    | 50  | -         | 25    | 50  | -             | 25    | 50  | ns    |
| Overshoot (Notes 1, 5, 6, & 8)                  | +25°C | -         | 25    | 40  | -         | 25    | 50  | -             | 25    | 50  | %     |
| Slew Rate (Notes 1, 5, 8 & 11)                  | +25°C | ±100      | ±120  | -   | ±80       | ±120  | -   | ±80           | ±120  | -   | V/μs  |
| Settling Time (Notes 1, 5, 8 & 11)              | +25°C | -         | 0.20  | -   | -         | 0.20  | -   | -             | 0.20  | -   | μs    |
| <b>POWER SUPPLY CHARACTERISTICS</b>             |       |           |       |     |           |       |     |               |       |     |       |
| Supply Current                                  | +25°C | -         | 4     | 6   | -         | 4     | 6   | -             | 4     | 6   | mA    |
| Power Supply Rejection Ratio (Note 7)           | Full  | 80        | 90    | -   | 74        | 90    | -   | 74            | 90    | -   | dB    |

#### NOTES:

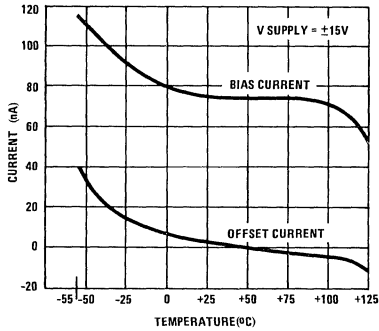
- |  |   |   |
|--|---|---|
| <p>1. R<sub>L</sub> = 2kΩ</p> <p>2. V<sub>CM</sub> = ±10V</p> <p>3. A<sub>V</sub> &gt; 10</p> <p>4. V<sub>O</sub> = ±10.0V</p> <p>5. C<sub>L</sub> = 50pF</p> <p>6. V<sub>O</sub> = ±200mV</p> | <p>7. ΔV = ±5.0V</p> <p>8. See Transient Response Test Circuits and Waveforms.</p> <p>9. This parameter value is based on design calculations.</p> <p>10. Full Power Bandwidth guaranteed based on slow rate measurement using: FPBW = S.R./2πV<sub>peak</sub>.</p> | <p>11. V<sub>OUT</sub> = ±5V</p> <p>12. Guaranteed by design.</p> <p>13. Absolute Maximum Ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.</p> |
|--|---|---|

3

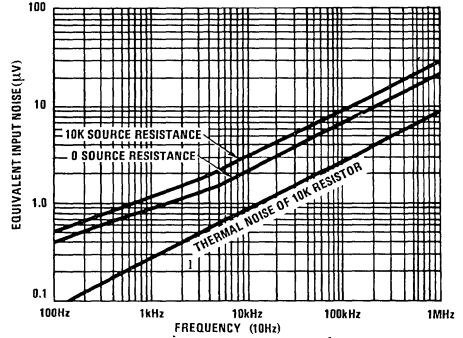
OPERATIONAL AMPLIFIERS

**Performance Curves**  $V_+ = +15VDC$ ,  $V_- = -15VDC$ ,  $T_A = +25^\circ C$ , Unless Otherwise Stated

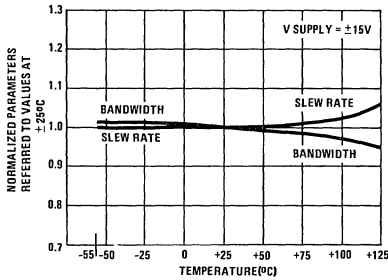
**INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE**



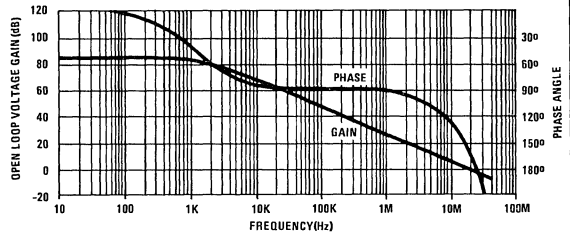
**EQUIVALENT INPUT NOISE vs. BANDWIDTH**  
(with 10 Hz High Pass Filter)



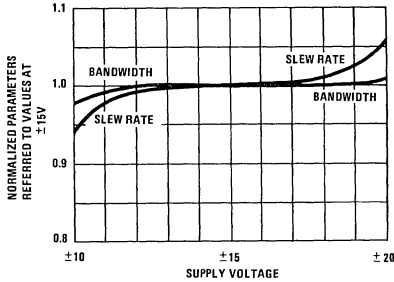
**NORMALIZED AC PARAMETERS vs. TEMPERATURE**



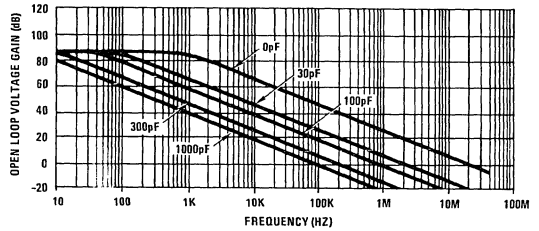
**OPEN-LOOP FREQUENCY AND PHASE RESPONSE**



**NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE AT +25°C**

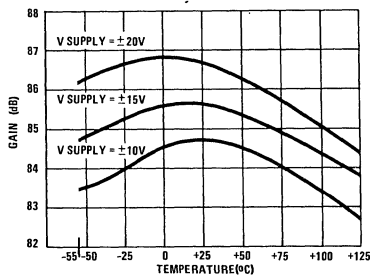


**OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND**

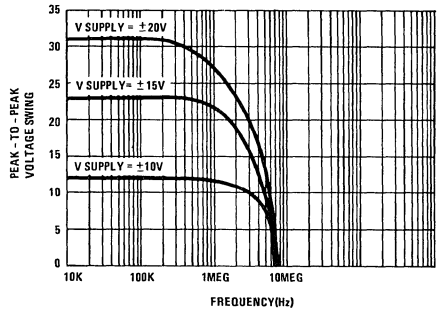


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

**OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE**

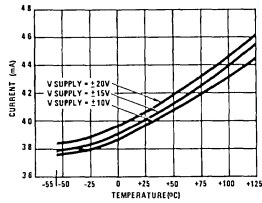


**OUTPUT VOLTAGE SWING vs. FREQUENCY AT +25°C**

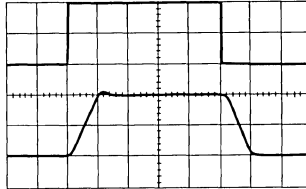


Performance Curves (Continued)

POWER SUPPLY CURRENT vs. TEMPERATURE

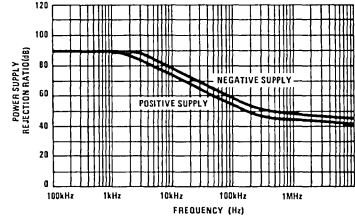


VOLTAGE FOLLOWER PULSE RESPONSE



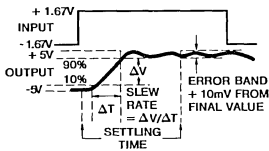
$R_L = 2K\Omega$ ,  $C_L = 50pF$  Horizontal = 100ns/Div.  
 Upper Trace: Input; 1.67V/Div.  $T_A = +25^\circ C$ ,  $V_S = \pm 15V$   
 Lower Trace: Output; 5V/Div.

POWER SUPPLY REJECTION RATIO vs. FREQUENCY

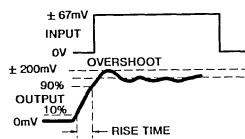


Test Circuits

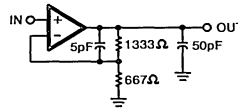
SLEW RATE AND SETTLING TIME



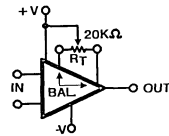
TRANSIENT RESPONSE



SLEW RATE AND TRANSIENT RESPONSE



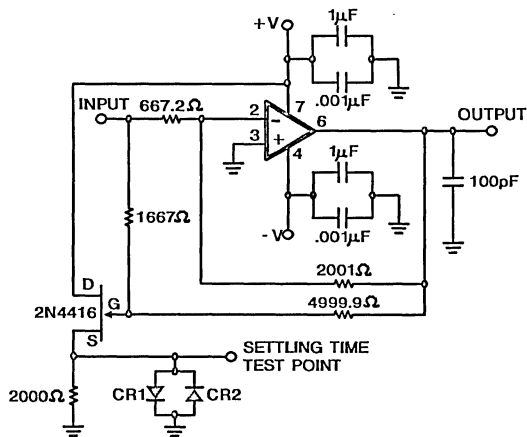
SUGGESTED  $V_{OS}$  ADJUSTMENT



NOTE: Measurement on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

Tested Offset Adjustment Range is  $|V_{OS} + 1mV|$  minimum referred to output. Typical range is +20mV to -18mV with  $R_T = 20k\Omega$ .

Settling Time Circuit

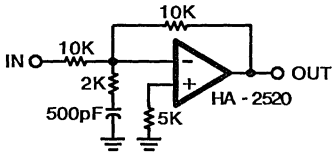


- $A_V = -3$
- Feedback and Summing Resistor Ratios Should be 0.1% matched.
- Clipping Diodes CR1 and CR2 are Optional. HP5082-2810 Recommended.



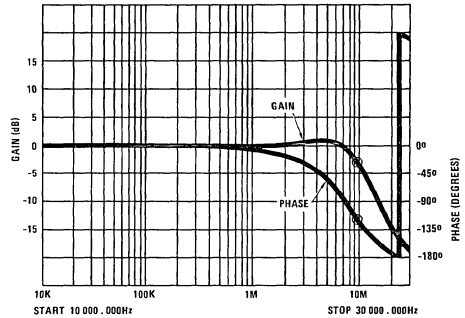
# HA-2520/2522/2525

## Typical Application



NOTE: Compensation Circuit for  $A_V = -1$   
 Slew Rate  $\approx 120V/\mu s$   
 Bandwidth  $\approx 10MHz$   
 Settling Time (0.1%)  $\approx 500ns$   
 Capacitance at pin 8 must be minimized for maximum bandwidth.  
 Tested and functional with supply voltages from  $\pm 4V$  to  $\pm 15V$ .

FREQUENCY RESPONSE FOR  
 INVERTING UNITY GAIN CIRCUIT



## Die Characteristics

|                                     |                   |               |
|-------------------------------------|-------------------|---------------|
| Transistor Count                    | 40                |               |
| Die Dimensions                      | 57 x 65 x 19 mils |               |
| Substrate Potential                 | Unbiased          |               |
| Process                             | Bipolar-DI        |               |
| Thermal Constants ( $^{\circ}C/W$ ) | $\theta_{ja}$     | $\theta_{jc}$ |
| HA2-Metal Can (-2, -5, -7)          | 206               | 56            |
| HA2-Metal Can (-8, /883)            | 168               | 52            |
| HA3-Plastic Mini-DIP (-5)           | 90                | 39            |
| HA4-Ceramic LCC (/883)              | 99                | 37            |
| HA7-Ceramic Mini-DIP (-8, /883)     | 100               | 28            |
| HA7-Ceramic Mini-DIP (-2, -5, -7)   | 204               | 112           |

## Uncompensated, High Slew Rate High Output Current, Operational Amplifier

August 1991

### Features

- High Slew Rate ..... 150V/ $\mu$ s
- Fast Settling ..... 200ns
- Wide Power Bandwidth ..... 2MHz
- Wide Gain Bandwidth ( $A_V \geq 3$ ) ..... 20MHz
- High Input Impedance ..... 130M $\Omega$
- Low Offset Current ..... 5nA
- High Output Current .....  $\pm 30$ mA

### Description

The HA-2529 is a monolithic operational amplifier which typifies excellence of design. With a design based on years of experience coupled with the reliable dielectric isolation process, these amplifiers provide an outstanding combination of DC and AC parameters at closed loop gains greater than 3.

The HA-2529 offers 150V/ $\mu$ s slew rate and fast settling time (200ns), while consuming a mere 6mA of quiescent current, making these amplifiers ideal components for video circuitry and data acquisition designs. With 20MHz gain-bandwidth combined with 7.5kV/V open loop gain, the HA-2529 is an ideal component for demanding signal conditioning designs. These devices provide  $\pm 30$ mA output

### Applications

- Data Acquisition Systems
- R.F. Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

current drive with an output voltage swing of  $\pm 10$ V making then suited for pulse amplifier and R.F. amplifier components.

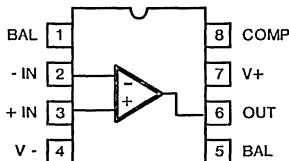
The HA-2529 will upgrade output current, slew rate, offset voltage drift and offset current drift in systems presently using the HA-2520/22/25 or EHA-2520/22/25.

The HA-2529-2 has guaranteed operation over the military temperature range ( $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ) and the HA-2529-5 has guaranteed operation over the commercial temperature range ( $0^{\circ}\text{C}$  to  $+75^{\circ}\text{C}$ ). MIL-STD-883 product and data sheets are available upon request.

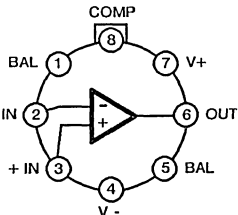
3  
OPERATIONAL AMPLIFIERS

### Pinouts

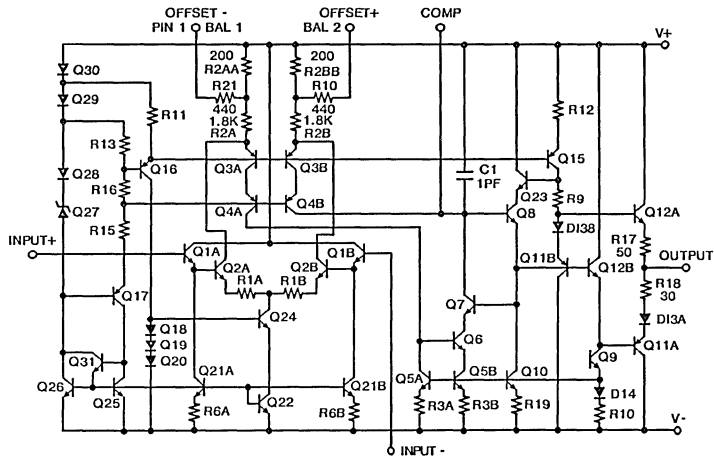
HA7-2529 (CERAMIC MINI-DIP)  
HA3-2529 (PLASTIC MINI-DIP)  
TOP VIEW



HA2-2529 (TO-99 METAL CAN)  
TOP VIEW



### Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.  
Copyright © Harris Corporation 1991

## Specifications HA-2529

### Absolute Maximum Ratings (Note 1)

|  |             |
|--|-------------|
| Voltage Between V+ and V- Terminals .....  | 40.0V       |
| Differential Input Voltage .....           | ±15V        |
| Output Current .....                       | 90mA (Peak) |
| Internal Power Dissipation (Note 10) ..... | 300mW       |
| Maximum Junction Temperature .....         | +175°C      |

### Operating Temperature Ranges

|                                 |  |
|---------------------------------|--|
| HA-2529-2 .....                 | $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ |
| HA-2529-5 .....                 | $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$    |
| Storage Temperature Range ..... | $-65^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ |

### Electrical Specifications $V_S = \pm 15\text{V}$ , $C_L = 50\text{pF}$ , $R_L = 2\text{k}\Omega$ , Unless Otherwise Specified

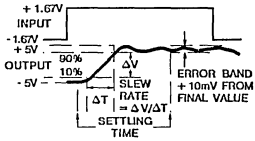
| PARAMETER   | TEMP  | HA-2529-2<br>-55°C to +125°C |      |     | HA-2529-5<br>0°C to +75°C |      |     | UNITS  |
|---|-------|------------------------------|------|-----|---------------------------|------|-----|--------|
|   |       | MIN                          | TYP  | MAX | MIN                       | TYP  | MAX |        |
| <b>INPUT CHARACTERISTICS</b>                      |       |                              |      |     |                           |      |     |        |
| Offset Voltage (Note 8)                           | +25°C | -                            | 2    | 5   | -                         | 2    | 10  | mV     |
|   | Full  | -                            | -    | 8   | -                         | -    | 14  | mV     |
| Average Offset Voltage Drift (Note 8)             | Full  | -                            | 10   | -   | -                         | 10   | -   | µV/°C  |
| Bias Current (Note 8)                             | +25°C | -                            | 50   | 200 | -                         | 50   | 250 | nA     |
|   | Full  | -                            | 80   | 400 | -                         | 80   | 400 | nA     |
| Average Bias Current Drift (Note 8)               | Full  | -                            | 0.2  | -   | -                         | 0.2  | -   | nA/°C  |
| Offset Current (Note 8)                           | +25°C | -                            | 5    | 25  | -                         | 5    | 50  | nA     |
|   | Full  | -                            | 10   | 50  | -                         | 10   | 100 | nA     |
| Average Offset Current Drift                      | Full  | -                            | 0.02 | -   | -                         | 0.02 | -   | nA/°C  |
| Common Mode Range                                 | Full  | ±10                          | ±13  | -   | ±10                       | ±13  | -   | V      |
| Differential Input Resistance (Note 11)           | +25°C | 50                           | 130  | -   | 50                        | 130  | -   | MΩ     |
| Differential Input Capacitance                    | +25°C | -                            | 3    | -   | -                         | 3    | -   | pF     |
| Input Noise Voltage (f = 1kHz)                    | +25°C | -                            | 20   | -   | -                         | 20   | -   | nV/√Hz |
| Input Noise Current (f = 1kHz)                    | +25°C | -                            | 1.8  | -   | -                         | 1.8  | -   | pA/√Hz |
| <b>TRANSFER CHARACTERISTICS</b>                   |       |                              |      |     |                           |      |     |        |
| Large Signal Voltage Gain (Note 3)                | +25°C | 10                           | 18   | -   | 7.5                       | 18   | -   | kV/V   |
|   | Full  | 7.5                          | 15   | -   | 5                         | 15   | -   | kV/V   |
| Common Mode Rejection Ratio (Note 5)              | Full  | 80                           | 100  | -   | 74                        | 100  | -   | dB     |
| Gain-Bandwidth Product (Note 2, 11)               | +25°C | 15                           | 20   | -   | 15                        | 20   | -   | MHz    |
| Minimum Stable Gain                               | +25°C | 3                            | -    | -   | 3                         | -    | -   | V/V    |
| <b>OUTPUT CHARACTERISTICS</b>                     |       |                              |      |     |                           |      |     |        |
| Output Voltage Swing                              | Full  | ±10                          | ±12  | -   | ±10                       | ±12  | -   | V      |
| Full Power Bandwidth (Notes 3 & 6)                | +25°C | 2.1                          | 2.6  | -   | 2.1                       | 2.6  | -   | MHz    |
| Output Current (Note 8)                           | +25°C | 30                           | 35   | -   | 30                        | 35   | -   | mA     |
|   | Full  | 25                           | 30   | -   | 25                        | 30   | -   | mA     |
| Output Resistance (Open Loop)                     | +25°C | -                            | 30   | -   | -                         | 30   | -   | Ω      |
| <b>TRANSIENT RESPONSE (<math>A_V = +3</math>)</b> |       |                              |      |     |                           |      |     |        |
| Rise Time (Note 2, 7)                             | +25°C | -                            | 20   | 45  | -                         | 20   | 50  | ns     |
| Overshoot (Note 2, 7)                             | +25°C | -                            | 10   | 30  | -                         | 10   | 30  | %      |
| Slew Rate (Note 3, 7)                             | +25°C | 135                          | 150  | -   | 135                       | 150  | -   | V/µs   |
| Settling Time (Note 4, 7)                         | +25°C | -                            | 200  | -   | -                         | 200  | -   | ns     |
| <b>POWER SUPPLY CHARACTERISTICS</b>               |       |                              |      |     |                           |      |     |        |
| Supply Current                                    | Full  | -                            | 4.5  | 6   | -                         | 4.5  | 6   | mA     |
| Power Supply Rejection Ratio (Note 12)            | Full  | 80                           | 90   | -   | 74                        | 90   | -   | dB     |

**NOTE:**

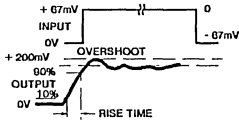
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2.  $V_{OUT} = \pm 200\text{mV}$ ,  $A_V \geq 3$ .
3.  $V_{OUT} = \pm 10\text{V}$ .
4. Settling Time is specified to 0.1% of final value for a 10V output step and  $A_V = -1$ .
5.  $\Delta V_{CM} = \pm 10\text{V}$ .
6. Full Power Bandwidth is guaranteed by equation:  $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$ .
7. See Transient Response and Settling Time Test Circuits.
8. Refer to typical performance curve in data sheet.
9.  $V_{OUT} = \pm 5\text{V}$ .
10. Refer to package thermal constants in Die Information section.
11. Parameter is guaranteed by design and characterization data.
12.  $\Delta V_S = \pm 10\text{V}$  to  $\pm 20\text{V}$ .

**Test Circuits**

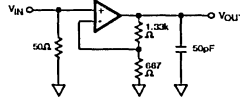
**SLEW RATE AND SETTLING TIME WAVEFORM**



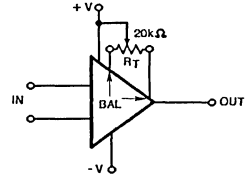
**TRANSIENT RESPONSE WAVEFORM**



**SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT**



**SUGGESTED V<sub>OS</sub> ADJUSTMENT**

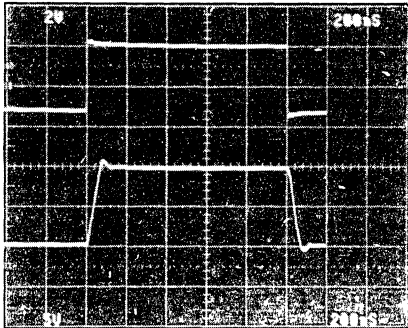


NOTE: Measured on both positive and negative transitions from 0 to +200mV and 0 to -200mV.

Tested Offset Adjustment is  $|V_{OS} + 1mV|$  minimum referred to output. Typical range is +28mV to -18mV with  $R_T = 20k\Omega$ .

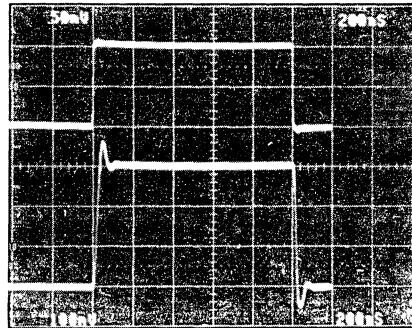
**LARGE SIGNAL RESPONSE**

Horizontal Scale: (200ns/Div.)  
Vertical Scale: (2V/Div. Input)  
(5V/Div. Output)

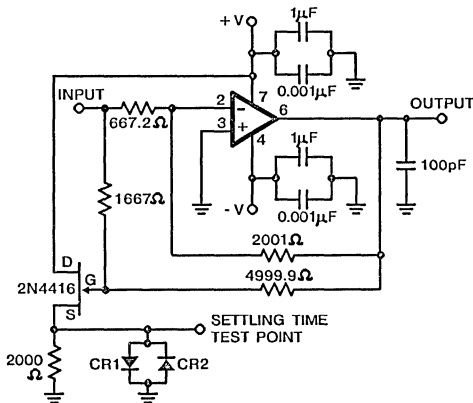


**SMALL SIGNAL RESPONSE**

Horizontal Scale: (200ns/Div.)  
Vertical Scale: (50mV/Div. Input)  
(100mV/Div. Output)



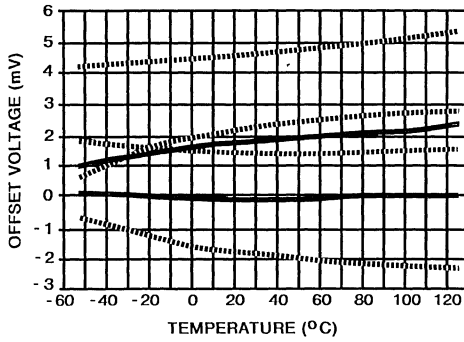
**Settling Time Circuit**



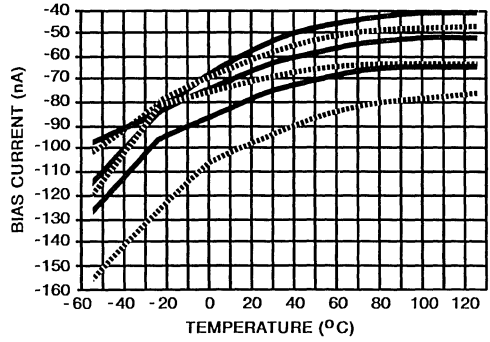
- $A_V = -3$
- Feedback and summing resistor ratios should be 0.1% matched.
- Clipping diodes CR1 and CR2 are optional. HP5082-2810 recommended.

**Typical Performance Curves**

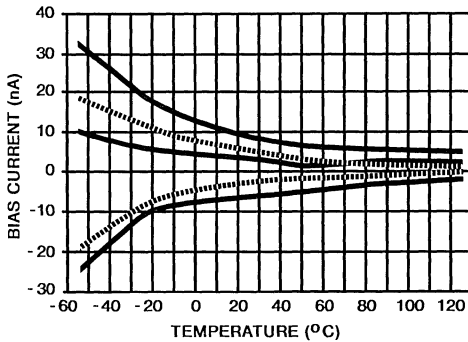
**OFFSET VOLTAGE vs. TEMPERATURE**  
6 Typical Units From 3 Lots @  $V_S = \pm 15V$



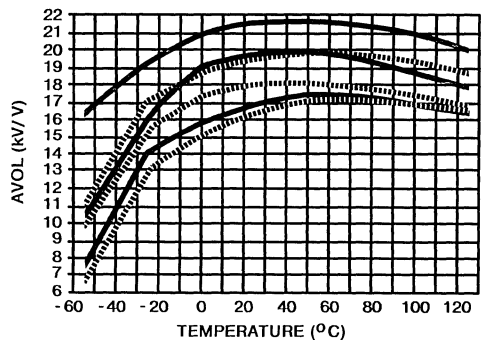
**BIAS CURRENT vs. TEMPERATURE**  
6 Typical Units From 3 Lots @  $V_S = \pm 15V$



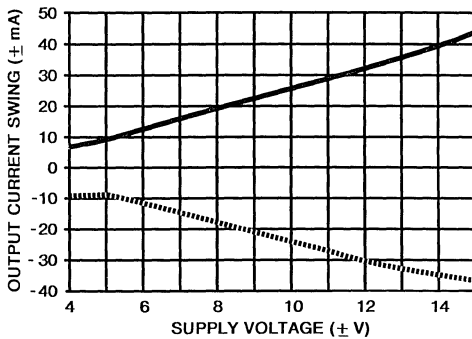
**OFFSET CURRENT vs. TEMPERATURE**  
5 Typical Units From 3 Lots @  $V_S = \pm 15V$



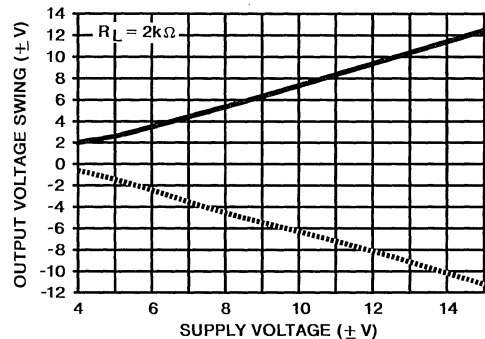
**OPEN LOOP GAIN vs. TEMPERATURE**  
6 Typical Units From 3 Lots @  $V_S = \pm 15V$



**OUTPUT CURRENT vs. SUPPLY VOLTAGE**

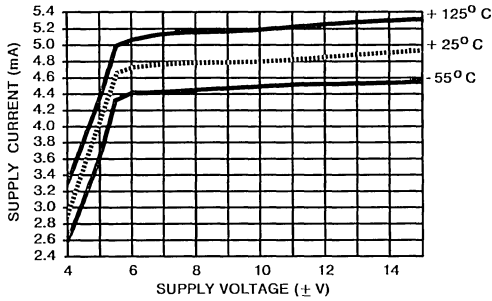


**OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE**

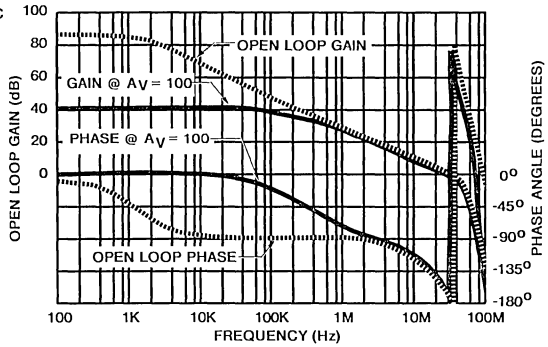


Typical Performance Curves (Continued)

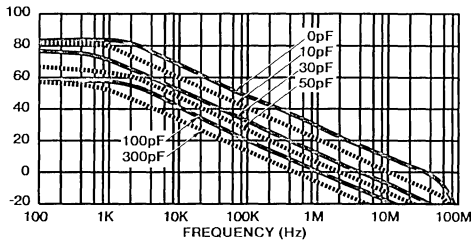
SUPPLY CURRENT vs. SUPPLY VOLTAGE  
Over Full Temperature



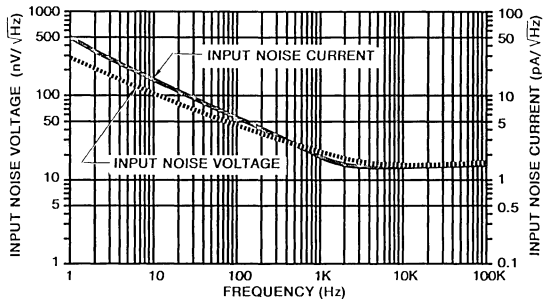
FREQUENCY RESPONSE AT VARIOUS GAINS



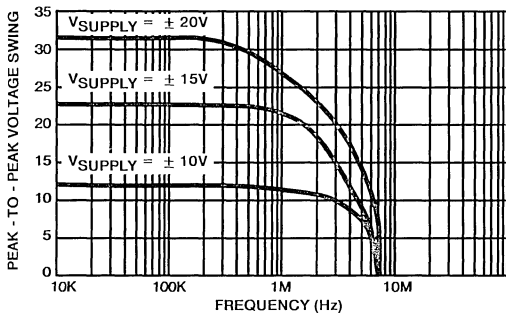
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



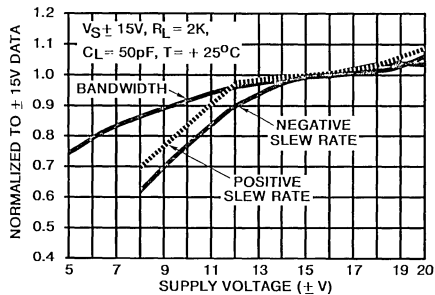
INPUT NOISE CHARACTERISTICS



OUTPUT VOLTAGE SWING vs. FREQUENCY



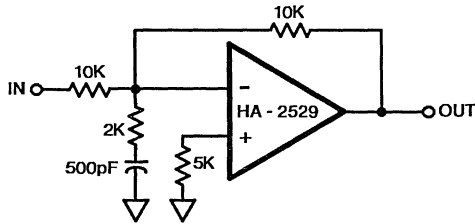
NORMALIZED A.C. PARAMETERS vs. SUPPLY VOLTAGE



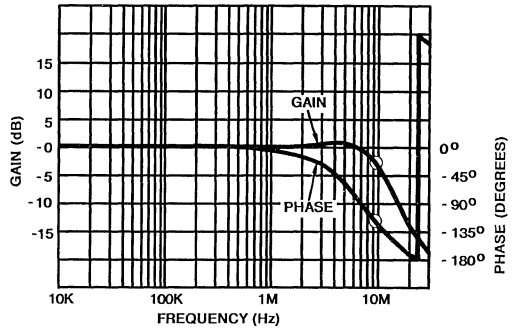
OPERATIONAL AMPLIFIERS

# HA-2529

## Typical Applications



FREQUENCY RESPONSE FOR  
INVERTING UNITY GAIN CIRCUIT



- NOTE:
- Compensation Circuit for  $A_v = -1$
  - Slew Rate  $\approx 120V/\mu s$
  - Bandwidth  $\approx 10MHz$
  - Settling Time (0.1%)  $\approx 500ns$
  - Capacitance at pin 8 must be minimized for maximum bandwidth.
  - Tested and functional with supply voltages from  $\pm 4V$  to  $\pm 15V$ .

## Die Characteristics

|   |  |
|---|--|
| Transistor Count .....                  | 40   |
| Die Dimensions .....                    | 1660 $\mu m$ x 1300 $\mu m$ x 485 $\mu m$<br>(65 mils x 51 mils x 19 mils) |
| Substrate Potential .....               | V-   |
| Process .....                           | Bipolar-DI   |
| Thermal Constants (°C/W) .....          | $\theta_{ja}$ $\theta_{jc}$  |
| HA2-Metal Can (-2, -5, -7) .....        | 206    56  |
| HA2-Metal Can (-8, /883) .....          | 168    52  |
| HA3-Plastic Mini-DIP (-5) .....         | 90    39   |
| HA4-Ceramic LCC (/883) .....            | 99    37   |
| HA7-Ceramic Mini-DIP (-8, /883) .....   | 140    65  |
| HA7-Ceramic Mini-DIP (-2, -5, -7) ..... | 204    112   |

## Very High Slew Rate Wideband Operational Amplifier

August 1991

### Features

- Very High Slew Rate ..... 600V/ $\mu$ s
- Open Loop Gain ..... 15kV/V
- Wide Gain-Bandwidth ( $A_V \geq 10$ ) ..... 600MHz
- Power Bandwidth ..... 9.5MHz
- Low Offset Voltage ..... 8mV
- Input Voltage Noise ..... 6nV/ $\sqrt{\text{Hz}}$
- Output Voltage Swing .....  $\pm 10\text{V}$
- Monolithic Bipolar Dielectric Isolation Construction

### Description

The Harris HA-2539 represents the ultimate in high slew rate, wideband, monolithic operational amplifiers. It has been designed and constructed with the Harris High Frequency Bipolar Dielectric Isolation process and features dynamic parameters never before available from a truly differential device.

With a 600V/ $\mu$ s slew rate and a 600MHz gain bandwidth product, the HA-2539 is ideally suited for use in video and RF amplifier designs, in closed loop gains of 10 or greater. Full  $\pm 10\text{V}$  swing coupled with outstanding A.C. parameters and complemented by high open loop gain makes the devices useful in high speed data acquisition systems.

### Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- RF Oscillators

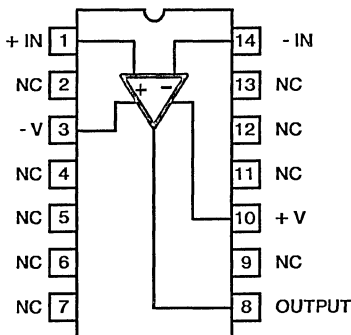
The HA-2539 is available in 14 pin ceramic and plastic DIP. The HA-2539-2 operates over  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  temperature range while the HA-2539-5 operates over the  $0^\circ\text{C}$  to  $+75^\circ\text{C}$  range. Additionally, SOIC packaging is available in  $-5$  and  $-9$  temperature grades.

For further design assistance please refer to Application Note 541 (Using The HA-2539 Very High Slew Rate Wideband Operational Amplifiers) and Application Note 556 (Thermal Safe-Operating-Areas For High Current Operational Amplifiers).

For military grade product information, the HA-2539/883 data sheet is available upon request.

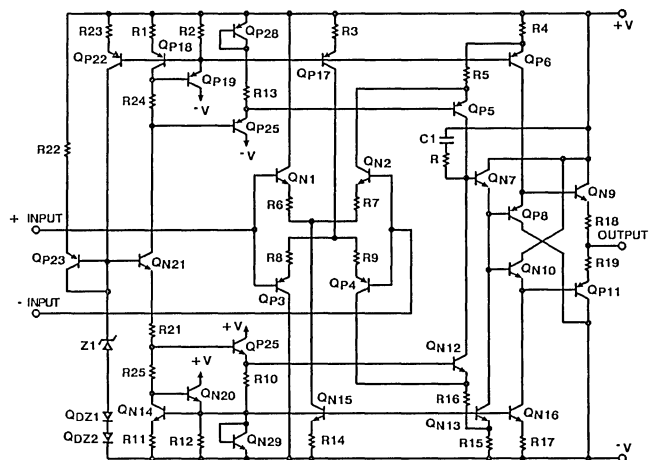
### Pinout

HA1-2539/2539C (CERAMIC DIP)  
 HA3-2539/2539C (PLASTIC DIP)  
 HA9P2539/2539C (SOIC)  
 TOP VIEW



(N.C.) No Connection pins may be tied to a ground plane for better isolation and heat dissipation.

### Schematic



3  
OPERATIONAL AMPLIFIERS



## Specifications HA-2539

### Absolute Maximum Ratings (Note 1)

|   |                        |
|---|------------------------|
| Voltage Between V+ and V- Terminals           | 35V                    |
| Differential Voltage                          | ±6V                    |
| Peak Output Current                           | 50mA                   |
| Continuous Output Current                     | 33mA <sub>rms</sub>    |
| Internal Quiescent Power Dissipation (Note 2) | 870mW<br>(Ceramic DIP) |

### Operating Temperature Range

|                              |                     |
|------------------------------|---------------------|
| HA-2539-2                    | -55°C ≤ TA ≤ +125°C |
| HA-2539/2539C-5              | 0°C ≤ TA ≤ +75°C    |
| HA-2539-9                    | -40°C ≤ TA ≤ +85°C  |
| Storage Temperature Range    | -65°C ≤ TA ≤ +150°C |
| Maximum Junction Temperature | +175°C              |

### Electrical Specifications V<sub>SUPPLY</sub> = ±15V, R<sub>L</sub> = 1kΩ, C<sub>L</sub> < 10pF, Unless Otherwise Specified.

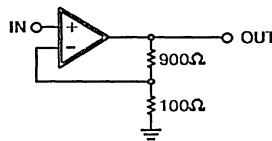
| PARAMETER  | TEMP  | HA-2539-2 |     |     | HA-2539-5, -9 |     |     | HA-2539C-5, -9 |     |     | UNITS  |
|--|-------|-----------|-----|-----|---------------|-----|-----|----------------|-----|-----|--------|
|  |       | MIN       | TYP | MAX | MIN           | TYP | MAX | MIN            | TYP | MAX |        |
| <b>INPUT CHARACTERISTICS</b>                                 |       |           |     |     |               |     |     |                |     |     |        |
| Offset Voltage   | +25°C | -         | 8   | 10  | -             | 8   | 15  | -              | 8   | 15  | mV     |
|  | Full  | -         | 13  | 15  | -             | 13  | 20  | -              | 13  | 20  | mV     |
| Average Offset Voltage Drift                                 | Full  | -         | 20  | -   | -             | 20  | -   | -              | 20  | -   | μV/°C  |
| Bias Current   | +25°C | -         | 5   | 20  | -             | 5   | 20  | -              | 5   | 20  | μA     |
|  | Full  | -         | -   | 25  | -             | -   | 25  | -              | -   | 25  | μA     |
| Offset Current   | +25°C | -         | 1   | 6   | -             | 1   | 6   | -              | 1   | 6   | μA     |
|  | Full  | -         | -   | 8   | -             | -   | 8   | -              | -   | 8   | μA     |
| Input Resistance   | +25°C | -         | 10  | -   | -             | 10  | -   | -              | 10  | -   | kΩ     |
| Input Capacitance  | +25°C | -         | 1   | -   | -             | 1   | -   | -              | 1   | -   | pF     |
| Common Mode Range  | Full  | ±10       | -   | -   | ±10           | -   | -   | ±10            | -   | -   | V      |
| Input Current Noise<br>(f = 1KHz, R <sub>SOURCE</sub> = 0Ω)  | +25°C | -         | 6   | -   | -             | 6   | -   | -              | 6   | -   | pA/√Hz |
| Input Voltage Noise<br>(f = 1KHz, R <sub>SOURCES</sub> = 0Ω) | +25°C | -         | 6   | -   | -             | 6   | -   | -              | 6   | -   | nV/√Hz |
| <b>TRANSFER CHARACTERISTICS</b>                              |       |           |     |     |               |     |     |                |     |     |        |
| Large Signal Voltage Gain<br>(Note 3)                        | +25°C | 10K       | 15K | -   | 10K           | 15K | -   | 7K             | 10K | -   | V/V    |
|  | Full  | 5K        | -   | -   | 5K            | -   | -   | 5K             | -   | -   | V/V    |
| Common-Mode Rejection Ratio<br>(Note 4)                      | Full  | 60        | 72  | -   | 60            | 72  | -   | 60             | 72  | -   | dB     |
| Minimum Stable Gain  | +25°C | 10        | -   | -   | 10            | -   | -   | 10             | -   | -   | V/V    |
| Gain Bandwidth Product<br>(Notes 5 & 6)                      | +25°C | -         | 600 | -   | -             | 600 | -   | -              | 600 | -   | MHz    |
| <b>OUTPUT CHARACTERISTICS</b>                                |       |           |     |     |               |     |     |                |     |     |        |
| Output Voltage Swing<br>(Note 3, 10)                         | Full  | ±10       | -   | -   | ±10           | -   | -   | ±10            | -   | -   | V      |
| Output Current (Note 3)                                      | +25°C | ±10       | ±20 | -   | ±10           | ±20 | -   | ±10            | ±20 | -   | mA     |
| Output Resistance  | +25°C | -         | 30  | -   | -             | 30  | -   | -              | 30  | -   | Ω      |
| Full Power Bandwidth<br>(Notes 3 & 7)                        | +25°C | 8.7       | 9.5 | -   | 8.7           | 9.5 | -   | 8.7            | 9.5 | -   | MHz    |
| <b>TRANSIENT RESPONSE (Note 8)</b>                           |       |           |     |     |               |     |     |                |     |     |        |
| Rise Time  | +25°C | -         | 7   | -   | -             | 7   | -   | -              | 7   | -   | ns     |
| Overshoot  | +25°C | -         | 15  | -   | -             | 15  | -   | -              | 15  | -   | %      |
| Slew Rate  | +25°C | 550       | 600 | -   | 550           | 600 | -   | 550            | 600 | -   | V/μs   |
| Settling Time: 10V Step to 0.1%                              | +25°C | -         | 180 | -   | -             | 180 | -   | -              | 200 | -   | ns     |
| <b>POWER REQUIREMENTS</b>                                    |       |           |     |     |               |     |     |                |     |     |        |
| Supply Current   | Full  | -         | 20  | 25  | -             | 20  | 25  | -              | 20  | 25  | mA     |
| Power Supply Rejection Ratio<br>(Note 9)                     | Full  | 60        | 70  | -   | 60            | 70  | -   | 60             | 70  | -   | dB     |

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. This value assumes a no load condition: Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below +175°C. By using Application Note 556 on Safe Operating Area equations, along with the packaging thermal resistances listed in the die information section, proper load conditions can be determined. Heat sinking is recommended above +75°C with suggested models:  
Thermalloy #6007 ( $\theta_{SA}=40^{\circ}\text{C/W}$ ) or AAVID #5602B ( $\theta_{SA}=16^{\circ}\text{C/W}$ ).
3.  $R_L = 1\text{k}\Omega$ ,  $V_O = \pm 10\text{V}$
4.  $V_{CM} = \pm 10\text{V}$
5.  $V_O = 90\text{mV}$
6.  $A_V = 10$ .
7. Full Power Bandwidth guaranteed based on slew rate measurement using 
$$\text{FPBW} = \frac{\text{Slew Rate}}{2nV_{\text{PEAK}}}$$
8. Refer to Test Circuits section of data sheet.
9.  $V_{\text{SUPPLY}} = \pm 5\text{VDC}$  to  $\pm 15\text{VDC}$
10. Guaranteed range for output voltage is  $\pm 10\text{V}$ . Functional operation outside of this range is not guaranteed.

Test Circuits

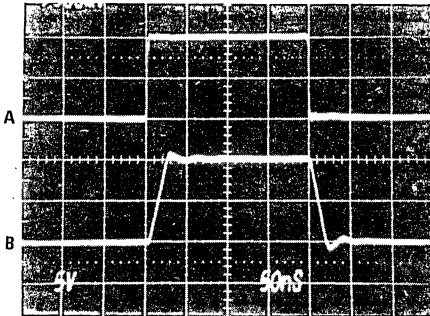
TEST CIRCUIT



$V_S = \pm 15\text{V}$   
 $A_V = +10$   
 $C_L \leq 10\text{pF}$

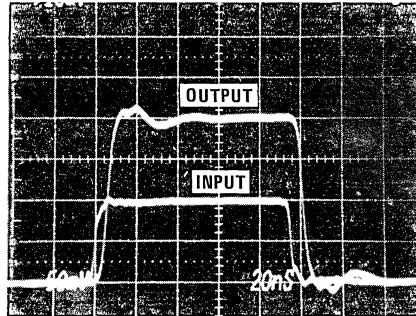
LARGE SIGNAL RESPONSE

Vertical Scale: A = 0.5V/Div., B = 5.0V/Div.  
 Horizontal Scale: Time: 50ns/Div.

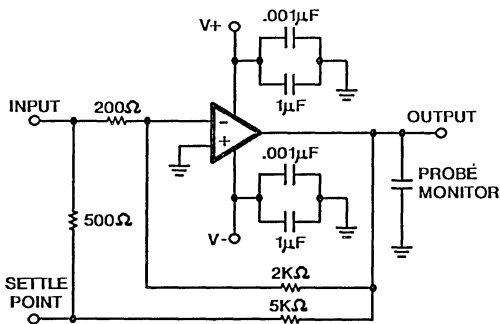


SMALL SIGNAL RESPONSE

Vertical Scale: Input = 10mV/Div., Output = 50mV/Div.  
 Horizontal Scale: 20ns/Div.



SETTLING TIME TEST CIRCUIT

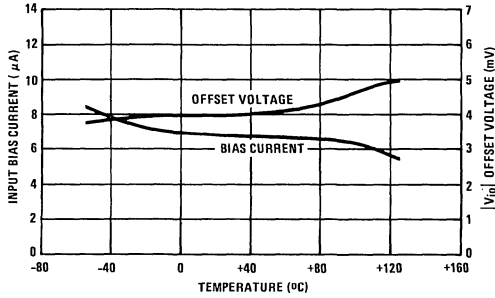


- $A_V = -10$
- Load Capacitance should be less than 10pF.
- It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
- SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

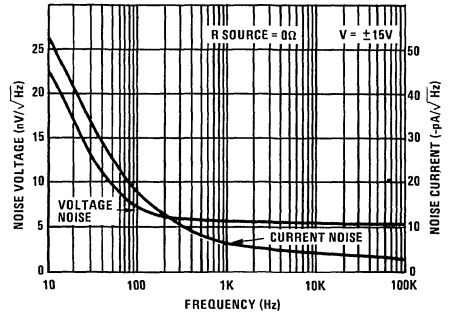
OPERATIONAL AMPLIFIERS

**Typical Performance Curves**

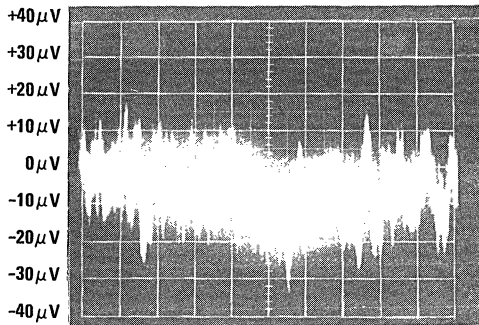
**INPUT OFFSET VOLTAGE AND BIAS CURRENT vs. TEMPERATURE**



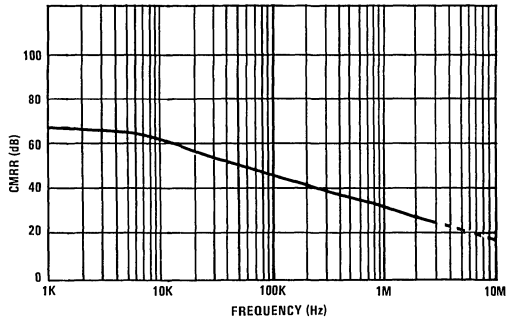
**INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY**



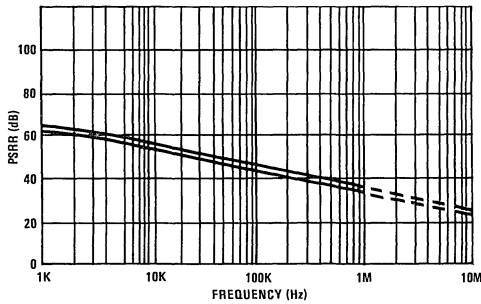
**BROADBAND NOISE (0.1Hz to 1MHz)**  
Vertical Scale:  $10\mu V/Div.$   
Horizontal Scale:  $50ms/Div.$



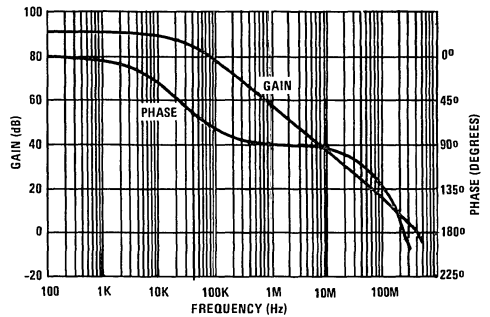
**COMMON MODE REJECTION RATIO vs. FREQUENCY**



**POWER SUPPLY REJECTION RATIO vs. FREQUENCY**

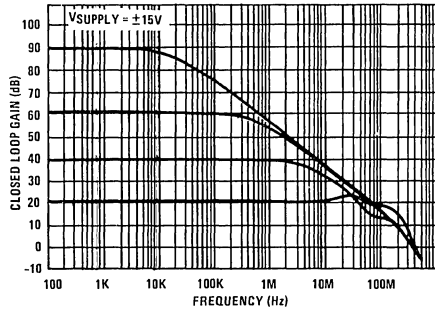


**OPEN LOOP GAIN/PHASE vs. FREQUENCY HA-2539**

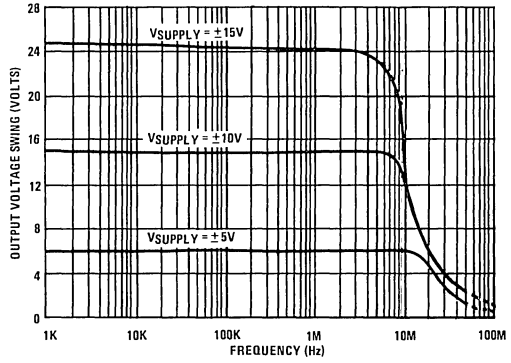


Typical Performance Curves (Continued)

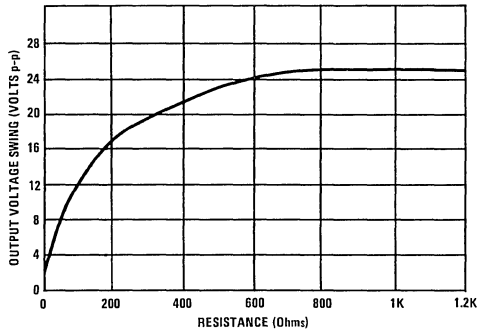
CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



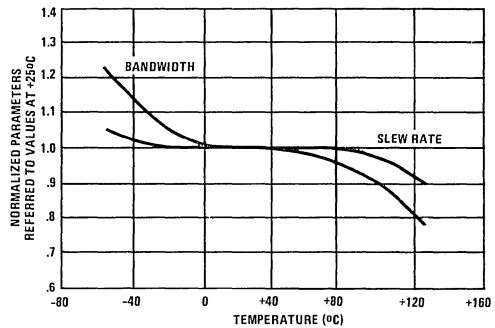
OUTPUT VOLTAGE SWING vs. FREQUENCY



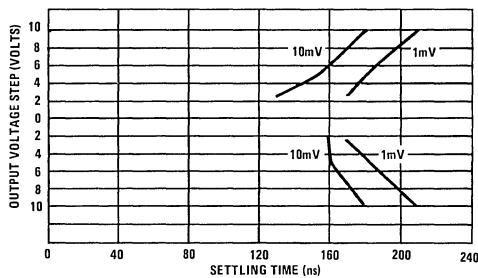
OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



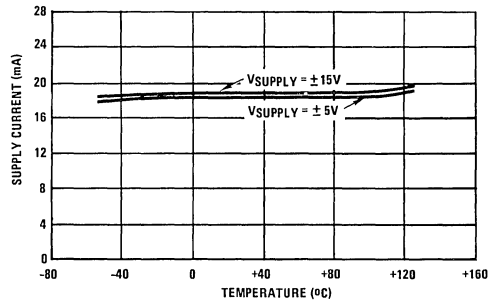
NORMALIZED AC PARAMETERS vs. TEMPERATURE



SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



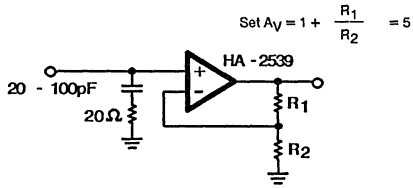
POWER SUPPLY CURRENT vs. TEMPERATURE AND SUPPLY VOLTAGE



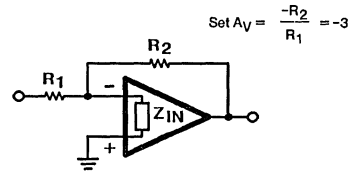
3  
OPERATIONAL  
AMPLIFIERS

**Applications**

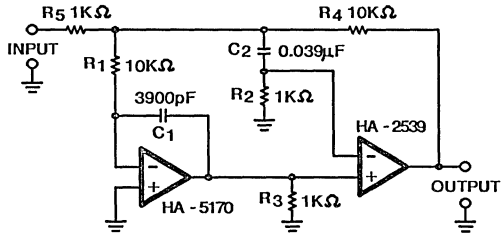
**FREQUENCY COMPENSATION BY OVERDAMPING**



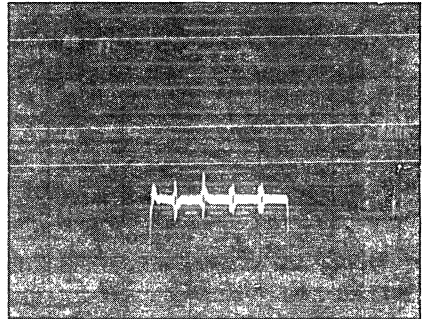
**STABILIZATION USING Z<sub>IN</sub>**



**REDUCING DC ERRORS  
COMPOSITE AMPLIFIER**



**DIFFERENTIAL GAIN ERROR (3%)  
HA-2539 20dB VIDEO GAIN BLOCK**



NOTE: No connect pins (NC) on the HA-2539 should be tied to a ground plane.  
Refer to Figure 4 in Application Note 541 for detailed Application suggestions.

**Die Characteristics**

|                                       |  |                 |
|---------------------------------------|--|-----------------|
| Transistor Count.....                 | 30   |                 |
| Die Dimensions .....                  | 75 x 61 x 19 mils<br>(1910μm x 1550μm x 483μm) |                 |
| Substrate Potential (Power Up)* ..... | V-   |                 |
| Process .....                         | High Frequency Bipolar-DI                      |                 |
| Passivation .....                     | Nitride  |                 |
| Thermal Constants (°C/W)              | θ <sub>ja</sub>                                | θ <sub>jc</sub> |
| HA1-2539/2539C Ceramic DIP            | 104  | 48              |
| HA3-2539/2539C Plastic DIP            | 95   | 46              |
| HA9P2539/2539C SOIC                   | 119  | 36              |

\*The substrate may be left floating (Insulating Die Mount) or it may be mounted on conductor at V- potential.

# HA-2540

## Wideband, Fast Settling Operational Amplifier

August 1991

### Features

- Very High Slew Rate ..... 400V/ $\mu$ s
- Fast Settling Time ..... 140ns
- Wide Gain-Bandwidth ( $A_V \geq 10$ ) ..... 400MHz
- Power Bandwidth ..... 6MHz
- Low Offset Voltage ..... 8mV
- Input Voltage Noise ..... 6nV/ $\sqrt{\text{Hz}}$
- Output Voltage Swing .....  $\pm 10\text{V}$
- Monolithic Bipolar Construction

### Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters

### Description

The Harris HA-2540 is a wideband, very high slew rate, monolithic operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction coupled with dielectric isolation allows this truly differential device to deliver outstanding performance in circuits where closed loop gain is 10 or greater. Additionally, the HA-2540 has a drive capability of  $\pm 10\text{V}$  into a  $1\text{K}\Omega$  load. Other desirable characteristics include low input voltage noise, low offset voltage, and fast settling time.

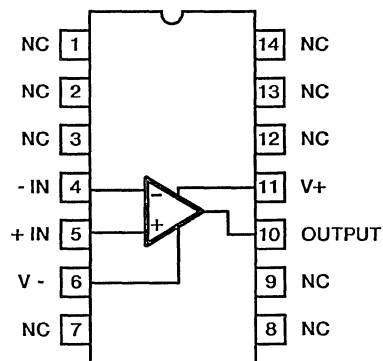
A 400V/ $\mu$ s slew rate ensures high performance in video and pulse amplification circuits, while the 400MHz gain-bandwidth-product is ideally suited for wideband signal amplification. A settling time of 140ns also makes the HA-2540 an excellent selection for high speed Data Acquisition Systems.

The HA-2540-2 is specified over the  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  range while the HA-2540-5 is specified from  $0^\circ\text{C}$  to  $+75^\circ\text{C}$ . The HA-2540 is available in the 14 pin Ceramic and Plastic DIP packages. A SOIC packaging option is also available in -5 and -9 temperature grades.

Refer to Application Note 541 and Application Note 556 for more information on High Speed Op-Amp applications. MIL-STD-883 data sheet is available on request.

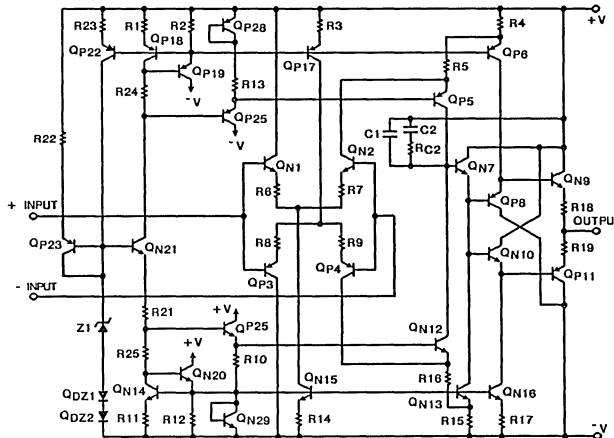
### Pinout

HA1-2540/2540C (CERAMIC DIP)  
HA3-2540/2540C (PLASTIC DIP)  
HA9P2540/2540C (SOIC)  
TOP VIEW



NC No Connection. These pins may be tied to a ground plane for added isolation and heat dissipation

### Schematic



3  
OPERATIONAL  
AMPLIFIERS

## HA-2540

### Absolute Maximum Ratings (Note 1)

|   |                                |
|---|--------------------------------|
| Voltage Between V+ and V- Terminals ..... | 35V                            |
| Differential Voltage .....                | ±6V                            |
| Output Current .....                      | 33mA (Continuous), 50mA (Peak) |
| Internal Power Dissipation (Note 2) ..... | 870mW (Cerdip)                 |

### Operating Temperature Ranges

|                                 |                                 |
|---------------------------------|---------------------------------|
| HA-2540-2 .....                 | -55°C ≤ T <sub>A</sub> ≤ +125°C |
| HA-2540/2540C-5 .....           | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| HA-2540/2540C-9 .....           | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| Storage Temperature Range ..... | -65°C ≤ T <sub>A</sub> ≤ +150°C |
| Junction Temperature .....      | +175°C                          |

**Electrical Specifications** V<sub>SUPPLY</sub> = ±15V, R<sub>L</sub> = 1kΩ, C<sub>L</sub> < 10pF, Unless Otherwise Specified.

| PARAMETER  | TEMP  | HA-2540-2 |     |     | HA-2540-5, -9 |     |     | HA-2540C-5, -9 |     |     | UNITS  |
|--|-------|-----------|-----|-----|---------------|-----|-----|----------------|-----|-----|--------|
|  |       | MIN       | TYP | MAX | MIN           | TYP | MAX | MIN            | TYP | MAX |        |
| <b>INPUT CHARACTERISTICS</b>                                 |       |           |     |     |               |     |     |                |     |     |        |
| Offset Voltage   | +25°C | -         | 8   | 10  | -             | 8   | 15  | -              | 8   | 15  | mV     |
|  | Full  | -         | 13  | 15  | -             | 13  | 20  | -              | 13  | 20  | mV     |
| Average Offset Voltage Drift                                 | Full  | -         | 20  | -   | -             | 20  | -   | -              | 20  | -   | μV/°C  |
| Bias Current   | +25°C | -         | 5   | 20  | -             | 5   | 20  | -              | 5   | 20  | μA     |
|  | Full  | -         | -   | 25  | -             | -   | 25  | -              | -   | 25  | μA     |
| Offset Current   | +25°C | -         | 1   | 6   | -             | 1   | 6   | -              | 1   | 6   | μA     |
|  | Full  | -         | -   | 8   | -             | -   | 8   | -              | -   | 8   | μA     |
| Input Resistance   | +25°C | -         | 10  | -   | -             | 10  | -   | -              | 10  | -   | kΩ     |
| Input Capacitance  | +25°C | -         | 1   | -   | -             | 1   | -   | -              | 1   | -   | pF     |
| Common Mode Range  | Full  | ±10       | -   | -   | ±10           | -   | -   | ±10            | -   | -   | V      |
| Input Noise Current<br>(f = 1kHz, R <sub>SOURCE</sub> = 0Ω)  | +25°C | -         | 6   | -   | -             | 6   | -   | -              | 6   | -   | pA/√Hz |
| Input Noise Voltage<br>(f = 1kHz, R <sub>SOURCES</sub> = 0Ω) | +25°C | -         | 6   | -   | -             | 6   | -   | -              | 6   | -   | nV/√Hz |
| <b>TRANSFER CHARACTERISTICS</b>                              |       |           |     |     |               |     |     |                |     |     |        |
| Large Signal Voltage Gain<br>(Note 3)                        | +25°C | 10K       | 15K | -   | 10K           | 15K | -   | 7K             | 10K | -   | V/V    |
|  | Full  | 5K        | -   | -   | 5K            | -   | -   | 5K             | -   | -   | V/V    |
| Common-Mode Rejection Ratio<br>(Note 4)                      | Full  | 60        | 72  | -   | 60            | 72  | -   | 60             | 72  | -   | dB     |
| Minimum Stable Gain  | +25°C | 10        | -   | -   | 10            | -   | -   | 10             | -   | -   | V/V    |
| Gain-Bandwidth-Product<br>(Notes 5 & 6)                      | +25°C | -         | 400 | -   | -             | 400 | -   | -              | 400 | -   | MHz    |
| <b>OUTPUT CHARACTERISTICS</b>                                |       |           |     |     |               |     |     |                |     |     |        |
| Output Voltage Swing (Note 3, 10)                            | Full  | ±10       | -   | -   | ±10           | -   | -   | ±10            | -   | -   | V      |
| Output Current (Note 3)                                      | +25°C | ±10       | ±20 | -   | ±10           | ±20 | -   | ±10            | ±20 | -   | mA     |
| Output Resistance  | +25°C | -         | 30  | -   | -             | 30  | -   | -              | 30  | -   | Ω      |
| Full Power Bandwidth<br>(Notes 3 & 7)                        | +25°C | 5.5       | 6   | -   | 5.5           | 6   | -   | 5.5            | 6   | -   | MHz    |
| <b>TRANSIENT RESPONSE (Note 8)</b>                           |       |           |     |     |               |     |     |                |     |     |        |
| Rise Time  | +25°C | -         | 14  | -   | -             | 14  | -   | -              | 14  | -   | ns     |
| Overshoot  | +25°C | -         | 5   | -   | -             | 5   | -   | -              | 5   | -   | %      |
| Slew Rate  | +25°C | 320       | 400 | -   | 320           | 400 | -   | 320            | 400 | -   | V/μs   |
| Settling Time: 10V Step to 0.1%                              | +25°C | -         | 140 | -   | -             | 140 | -   | -              | 140 | -   | ns     |
| <b>POWER REQUIREMENTS</b>                                    |       |           |     |     |               |     |     |                |     |     |        |
| Supply Current   | Full  | -         | 20  | 25  | -             | 20  | 25  | -              | 20  | 25  | mA     |
| Power Supply Rejection Ratio<br>(Note 9)                     | Full  | 60        | 70  | -   | 60            | 70  | -   | 60             | 70  | -   | dB     |

# HA-2540

## NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. This value assumes a no load condition: Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below +175°C. By using Application Note 556 on Safe Operating Area Equations, along with the packaging thermal resistances listed in the Die Information section, proper load conditions can be determined. Heat sinking is recommended above +75°C with suggested models:

Thermalloy #6007 ( $\theta_{SA} = 40^\circ\text{C/W}$ ) or AAVID #5602B ( $\theta_{SA} = 16^\circ\text{C/W}$ ).

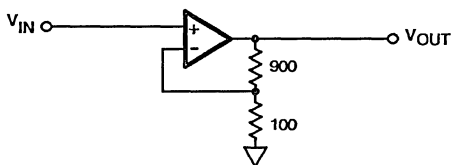
3.  $R_L = 1\text{k}\Omega$ ,  $V_O = \pm 10\text{V}$ .
4.  $V_{CM} = \pm 10\text{V}$ .
5.  $V_O = 90\text{mV}$ .
6.  $A_V = 10\text{V}$ .
7. Full power bandwidth guaranteed based on slow rate

measurement using:  $\text{FPBW} = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$

8. Refer to Test Circuits section of the data sheet.
9.  $V_{SUPPLY} = \pm 5\text{VDC}$  to  $\pm 15\text{VDC}$ .
10. Guaranteed range for output voltage is  $\pm 10\text{V}$ . Functional operation outside of this range is not guaranteed.

## Test Circuits

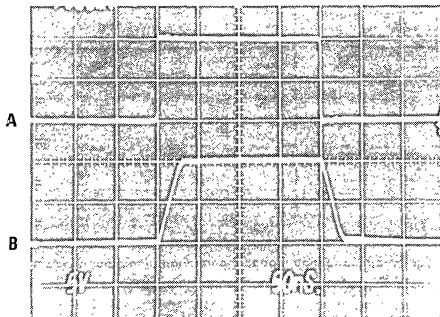
### LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



$A_V = +10$   
 $CL \leq 10\text{pF}$

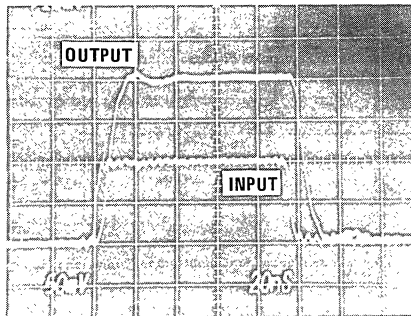
#### LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: A = 0.5V/Div., B = 5.0V/Div.)  
Horizontal Scale: (Time: 50ns/Div.)



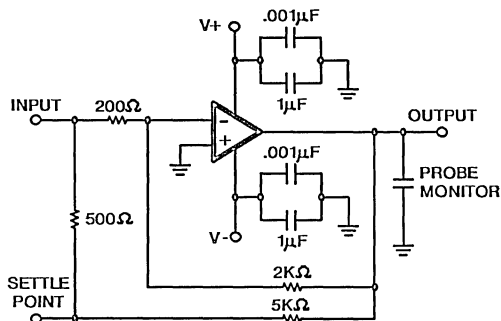
#### SMALL SIGNAL RESPONSE

Vertical Scale: Input = 10mV/Div.; Output = 50mV/Div.  
Horizontal Scale: 20ns/Div.



TURN-ON TIME DELAY TYPICALLY 4ns.

### SETTLING TIME TEST CIRCUIT

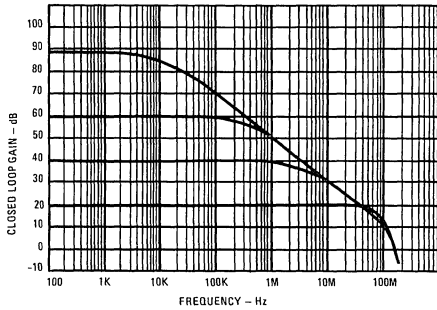


- $A_V = -10$ .
- Load Capacitance should be less than 10pF. Turn on time delay typically 4ns.
- It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
- SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

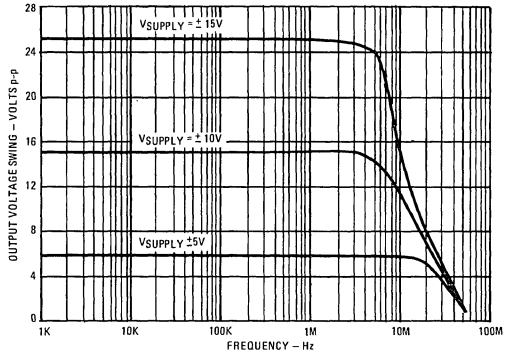


Performance Curves

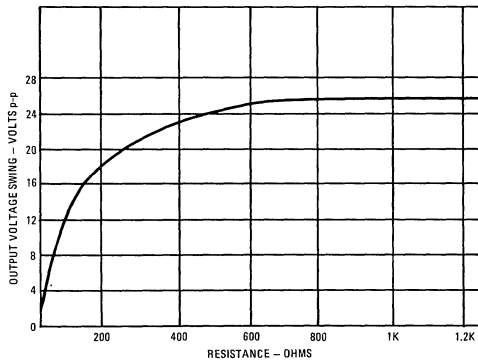
CLOSED LOOP FREQUENCY RESPONSE



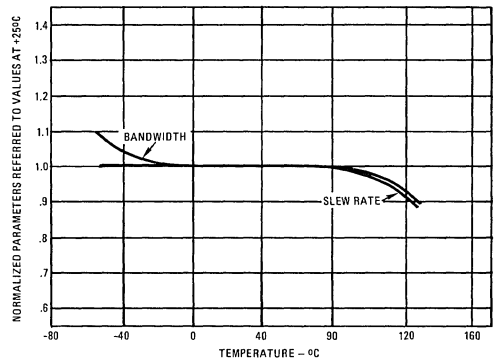
OUTPUT VOLTAGE SWING vs. FREQUENCY



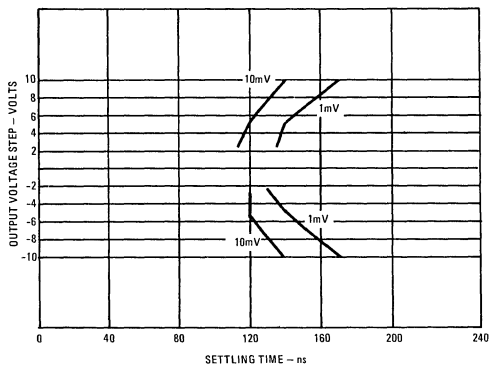
OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



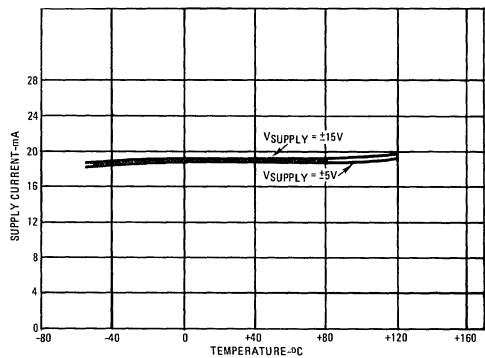
NORMALIZED AC PARAMETERS vs. TEMPERATURE



SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

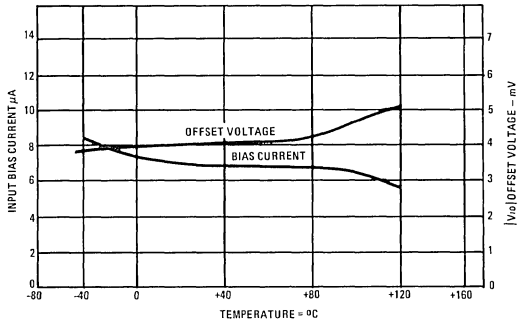


POWER SUPPLY CURRENT vs. TEMPERATURE AND SUPPLY VOLTAGE

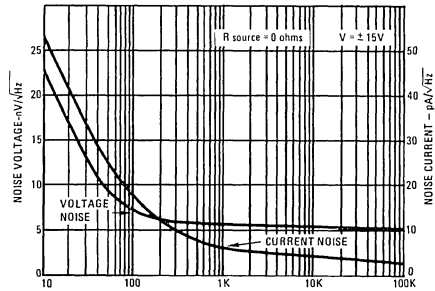


Performance Curves

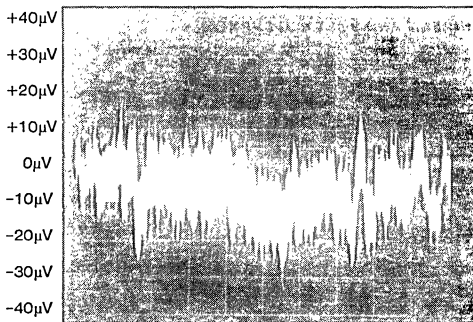
INPUT OFFSET VOLTAGE AND BIAS CURRENT vs. TEMPERATURE



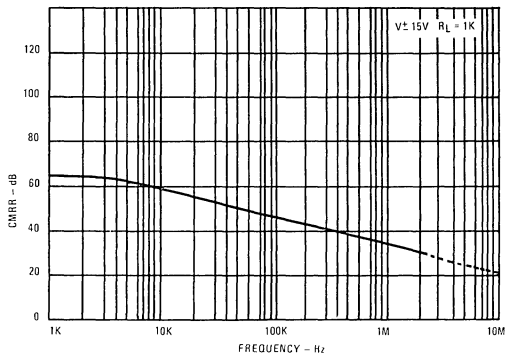
INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY



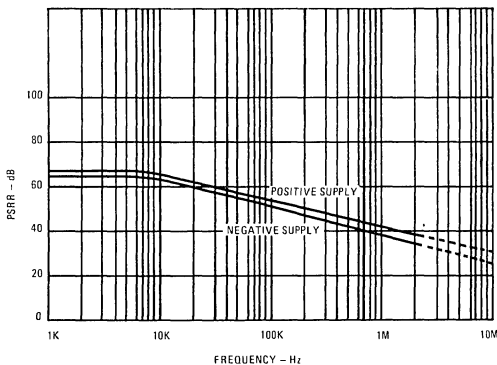
BROADBAND NOISE (0.1Hz to 1MHz)  
Vertical Scale: 10mV/Div.  
Horizontal Scale: 50ms/Div.



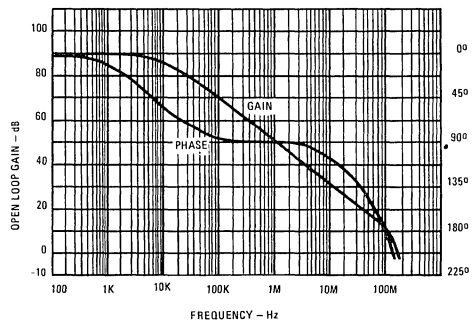
COMMON MODE REJECTION RATIO vs. FREQUENCY



POWER SUPPLY REJECTION RATIO vs. FREQUENCY



OPEN LOOP GAIN/PHASE vs. FREQUENCY HA-2540



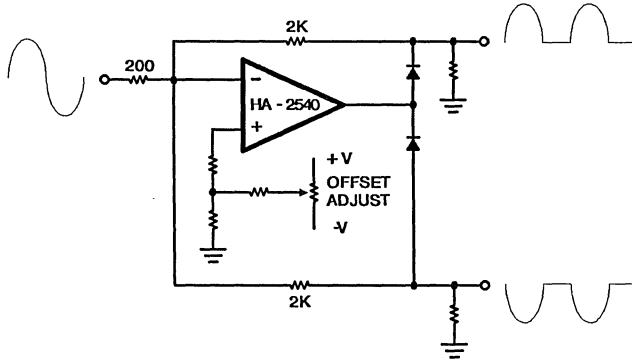
OPERATIONAL AMPLIFIERS

# HA-2540

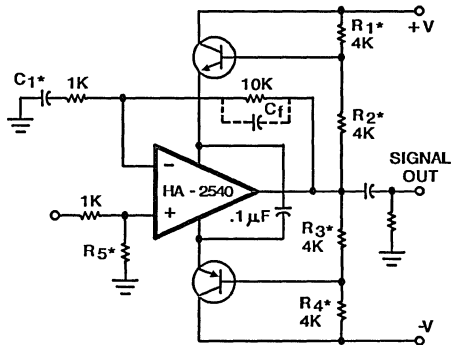
## Applications

### WIDEBAND SIGNAL SPLITTER

With one HA-2540 and two low capacitance switching diodes, signals exceeding 10MHz can be separated. This circuit is most useful for full wave rectification, AM detectors or sync generation.



### BOOTSTRAPPING FOR MORE OUTPUT CURRENT AND VOLTAGE SWING



#### NOTES:

1. Used for experimental purposes.  $C_f \approx 3pF$ .
2.  $C_1$  is optional ( $0.001\mu F \rightarrow 0.01\mu F$  ceramic)
3.  $R_5$  is optional and can be utilized to reduce input signal amplitude and/or balance input conditions.  $R_5 = 500\Omega$  to  $1k\Omega$ .

Refer to Application Note 541 For Further Applications Information.

## Die Characteristics

|                                       |   |                                     |               |               |
|---------------------------------------|---|-------------------------------------|---------------|---------------|
| Transistor Count .....                | 30  | Thermal Constants ( $^{\circ}C/W$ ) | $\theta_{ja}$ | $\theta_{jc}$ |
| Die Dimensions .....                  | 75 x 61 x 19 mils<br>(1910 $\mu m$ x 1550 $\mu m$ x 483 $\mu m$ ) | HA-2540/2540C Ceramic DIP           | 104           | 48            |
| Substrate Potential (Power Up)* ..... | V-  | HA-2540/2540C Plastic DIP           | 95            | 46            |
| Process .....                         | High Frequency Bipolar-DI   | HA-2540/2540C SOIC                  | 119           | 36            |
| Passivation .....                     | Nitride   |                                     |               |               |

\*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential. V- potential.

## Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier

August 1991

### Features

- Unity Gain Bandwidth ..... 40MHz
- High Slew Rate ..... 250V/ $\mu$ s
- Low Offset Voltage ..... 0.8mV
- Fast Settling Time (0.1%) ..... 90ns
- Power Bandwidth ..... 4MHz
- Output Voltage Swing (Min) .....  $\pm$ 10V
- Unity Gain Stability
- Monolithic Bipolar Dielectric Isolation Construction

### Description

The HA-2541 is the first unity gain stable monolithic operational amplifier to achieve 40MHz unity gain bandwidth. A major addition to the Harris series of high speed, wideband op amps, the HA-2541 is designed for video and pulse applications requiring stable amplifier response at low closed loop gains.

The uniqueness of the HA-2541 is that its slew rate and bandwidth characteristics are specified at unity gain. Historically, high slew rate, wide bandwidth and unity gain stability have been incompatible features for a monolithic operational amplifier. But features such as 250V/ $\mu$ s slew rate and 40MHz unity gain bandwidth clearly show that this is not the case for the HA-2541. These features, along with

### Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters
- High Speed A/D Input Buffer

90ns settling time to 0.1%, make this product an excellent choice for high speed data acquisition systems.

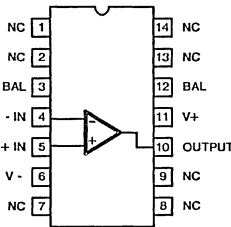
Packaged in a metal can (TO-8) or 14 pin ceramic DIP, the HA-2541 is pin compatible with the HA-2540 and HA-5190 op amps. The HA-2541-2 is specified over the temperature range of  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . The HA-2541-5 is specified over the temperature range of  $0^{\circ}\text{C}$  to  $+75^{\circ}\text{C}$ . For the military grade product, refer to the HA-2541 military data sheet.

For further application suggestions on the HA-2541, please refer to Application Note 550 (Using the HA-2541), and Application Note 556 (Thermal Safe-Operating-Areas For High Current Operational Amplifiers). Also see 'Applications' in this data sheet.

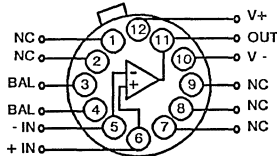
3  
OPERATIONAL AMPLIFIERS

### Pinouts

HA1-2541 CERAMIC DIP TOP VIEW

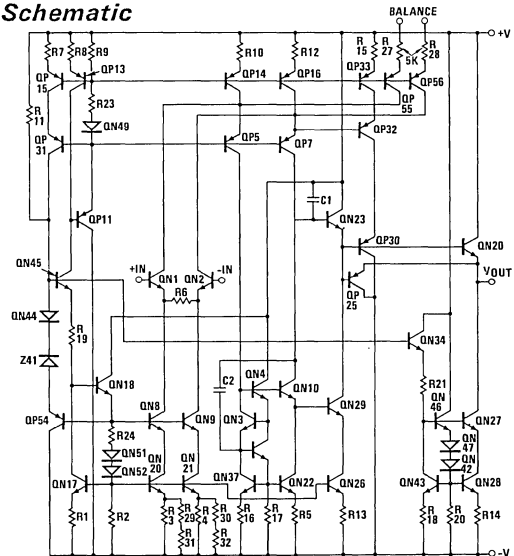


HA2-2541 METAL CAN (TO-8) TOP VIEW



VCASE = V-

### Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.  
Copyright © Harris Corporation 1991

## Specifications HA-2541

### Absolute Maximum Ratings (Note 1)

|                            |                     |
|----------------------------|---------------------|
| Voltage Between Vz and V-  | 35V                 |
| Differential Input Voltage | ±6V                 |
| Peak Output Current        | 50mA                |
| Continuous Output Current  | 28mA <sub>rms</sub> |

### Operating Temperature Range:

|  |                                 |
|--|---------------------------------|
| HA-2541-2                              | -55°C ≤ T <sub>A</sub> ≤ +125°C |
| HA-2541-5                              | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| Storage Temperature Range              | -65°C ≤ T <sub>A</sub> ≤ +150°C |
| Maximum Junction Temperature (Note 11) | +175°C                          |

### Electrical Specifications V<sub>SUPPLY</sub> = ±15 Volts; R<sub>L</sub> = 1kΩ, C<sub>L</sub> ≤ 10pF, Unless Otherwise Specified

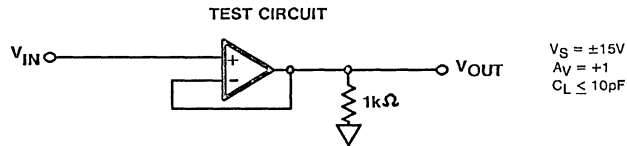
| PARAMETER   | TEMP  | HA-2541-2<br>-55°C to +125°C |       |     | HA-2541-5<br>0°C to +75°C |       |     | UNITS                  |
|---|-------|------------------------------|-------|-----|---------------------------|-------|-----|------------------------|
|   |       | MIN                          | TYP   | MAX | MIN                       | TYP   | MAX |                        |
| <b>INPUT CHARACTERISTICS</b>                        |       |                              |       |     |                           |       |     |                        |
| Offset Voltage                                      | +25°C | -                            | 0.8   | 2   | -                         | 1     | 2   | mV                     |
|   | Full  | -                            | -     | 6   | -                         | -     | 6   | mV                     |
| Average Offset Voltage Drift                        | Full  | -                            | 9     | -   | -                         | 9     | -   | μV/°C                  |
| Bias Current  | +25°C | -                            | 11    | 35  | -                         | 11    | 35  | μA                     |
|   | Full  | -                            | -     | 50  | -                         | -     | 50  | μA                     |
| Average Bias Current Drift                          | Full  | -                            | 85    | -   | -                         | 85    | -   | nA/°C                  |
| Offset Current                                      | +25°C | -                            | 1     | 7   | -                         | 1     | 7   | μA                     |
|   | Full  | -                            | -     | 9   | -                         | -     | 9   | μA                     |
| Input Resistance                                    | +25°C | -                            | 100   | -   | -                         | 100   | -   | kΩ                     |
| Input Capacitance                                   | +25°C | -                            | 1     | -   | -                         | 1     | -   | pF                     |
| Common Mode Range                                   | Full  | ±10                          | ±11   | -   | ±10                       | ±11   | -   | V                      |
| Input Noise Voltage (f = 1kHz, R <sub>g</sub> = 0Ω) | +25°C | -                            | 10    | -   | -                         | 10    | -   | nV <sub>rms</sub> /√Hz |
| Input Noise Current (f = 1kHz, R <sub>g</sub> = 0Ω) | +25°C | -                            | 4     | -   | -                         | 4     | -   | pA <sub>rms</sub> /√Hz |
| <b>TRANSFER CHARACTERISTICS</b>                     |       |                              |       |     |                           |       |     |                        |
| Large Signal Voltage Gain (Note 3)                  | +25°C | 10k                          | 16k   | -   | 10k                       | 16k   | -   | V/V                    |
|   | Full  | 5k                           | -     | -   | 5k                        | -     | -   | V/V                    |
| Common-Mode Rejection Ratio (Note 5)                | Full  | 70                           | 90    | -   | 70                        | 90    | -   | dB                     |
| Minimum Stable Gain                                 | +25°C | 1                            | -     | -   | 1                         | -     | -   | V/V                    |
| Unity Gain-Bandwidth (Note 6)                       | +25°C | -                            | 40    | -   | -                         | 40    | -   | MHz                    |
| <b>OUTPUT CHARACTERISTICS</b>                       |       |                              |       |     |                           |       |     |                        |
| Output Voltage Swing (Note 4)                       | Full  | ±10                          | ±11   | -   | ±10                       | ±11   | -   | V                      |
| Output Current (Note 4)                             | +25°C | ±10                          | ±15   | -   | ±10                       | ±15   | -   | mA                     |
| Output Resistance                                   | +25°C | -                            | 2     | -   | -                         | 2     | -   | Ω                      |
| Full Power Bandwidth (Note 3 & 7)                   | +25°C | 3                            | 4     | -   | 3                         | 4     | -   | MHz                    |
| Differential Gain (Note 2)                          | +25°C | -                            | 0.1   | -   | -                         | 0.1   | -   | %                      |
| Differential Phase (Note 2)                         | +25°C | -                            | 0.2   | -   | -                         | 0.2   | -   | Degree                 |
| Harmonic Distortion (Note 10)                       | +25°C | -                            | <0.01 | -   | -                         | <0.01 | -   | %                      |
| <b>TRANSIENT RESPONSE (Note 8)</b>                  |       |                              |       |     |                           |       |     |                        |
| Rise Time   | +25°C | -                            | 4     | -   | -                         | 4     | -   | ns                     |
| Overshoot   | +25°C | -                            | 40    | -   | -                         | 40    | -   | %                      |
| Slew Rate   | +25°C | 200                          | 250   | -   | 200                       | 250   | -   | V/μs                   |
| Settling Time: 10V Step to 0.1%                     | +25°C | -                            | 90    | -   | -                         | 90    | -   | ns                     |
|   | +25°C | -                            | 175   | -   | -                         | 175   | -   | ns                     |
| <b>POWER REQUIREMENTS</b>                           |       |                              |       |     |                           |       |     |                        |
| Supply Current                                      | +25°C | -                            | 29    | -   | -                         | 29    | -   | mA                     |
|   | Full  | -                            | -     | 40  | -                         | -     | 40  | mA                     |
| Power Supply Rejection Ratio (Note 9)               | Full  | 70                           | 80    | -   | 70                        | 78    | -   | dB                     |

# HA-2541

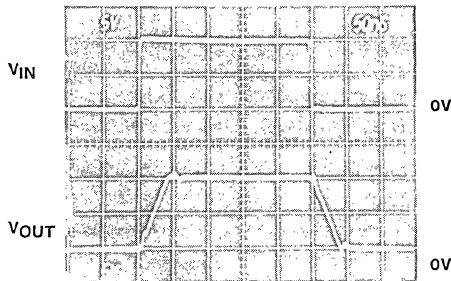
## NOTES:

- Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
- Differential Gain and Phase are measured with a 1 Volt differential voltage at 5MHz.
- $V_O = \pm 10V$
- $R_L = 1k\Omega$
- $V_{CM} = \pm 10V$
- $V_O = 90mV$ .
- Full Power Bandwidth guaranteed based on slew rate measurement  
using  $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
- Refer to Test Circuits section of this data sheet.
- $V_{SUPPLY} = \pm 5VDC$  to  $\pm 15VDC$
- $f = 10kHz$ ;  $A_V = 5$ ;  $V_O = 14Vp-p$
- This value assumes a no load condition: Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below  $+175^\circ C$ . By using Application Note 556 on Safe operating Area equations, along with the packaging thermal resistances listed in the Die Characteristics section, proper load conditions can be determined. Heat sinking is recommended above  $+75^\circ C$  with suggested models:
  - 14 Lead Ceramic DIP: Thermalloy #6007 or AAVID #5620B ( $\theta_{sa} = 16^\circ C/W$ ).
  - 12 Lead Metal Can (TO-8): Thermalloy #2240A ( $\theta_{sa} = 27^\circ C/W$ ) or #2268B ( $\theta_{sa} = 24^\circ C/W$ )

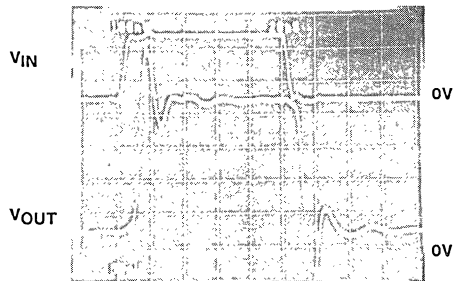
## Test Circuits



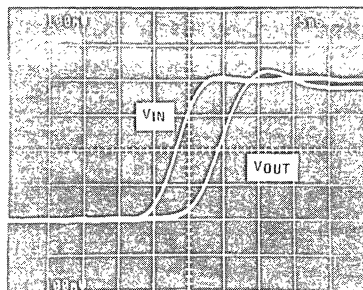
**LARGE SIGNAL RESPONSE**  
Vertical Scale (Volts: 5V/Div.)  
Horizontal Scale (Time: 50ns/Div.)



**SMALL SIGNAL RESPONSE**  
Vertical Scale ( $V_{IN} = 100mV/Div.$ ,  $V_{OUT} = 50mV/Div.$ )  
Horizontal Scale (Time: 20ns/Div.)



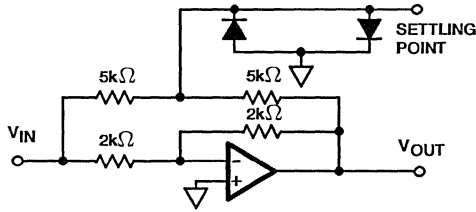
**PROPAGATION DELAY**  
Vertical Scale (Volts: 100mV/Div.)  
Horizontal Scale (Time: 5ns/Div.)



$V_S = \pm 15V$ ,  $R_L = 1k\Omega$   
 $T = +25^\circ C$   
Propagation delay variance is negligible over full temperature range.

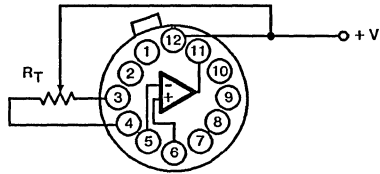
**Test Circuits (Continued)**

**SETTLING TIME TEST CIRCUIT**



- $A_V = -1$
- Feedback and Summing Resistors Must Be Matched (0.1%)
- HP5082-2810 Clipping Diodes Recommended
- Tektronix P6201 FET Probe Used At Settling Point.

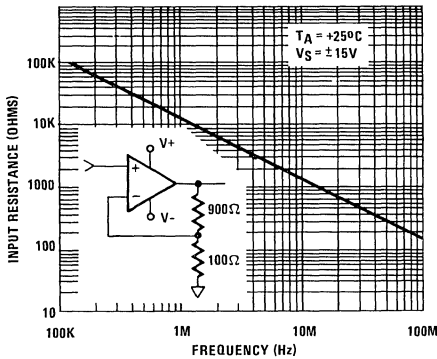
**Suggested Offset Voltage Adjustment**



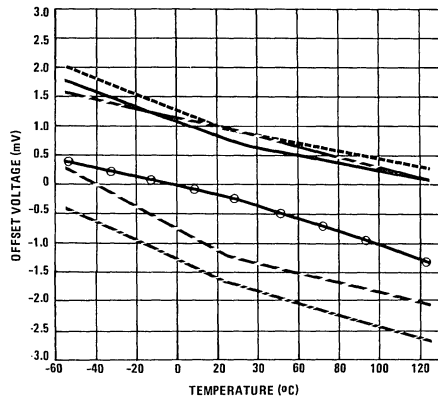
Tested Offset Adjustment Range is  $|V_{OS} + 1\text{mV}|$  minimum referred to output.  
Typical range is  $\pm 15\text{mV}$  for  $R_T = 5\text{k}\Omega$

**Typical Performance Curves**

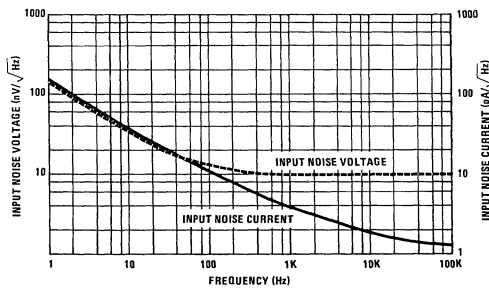
**INPUT RESISTANCE vs. FREQUENCY**



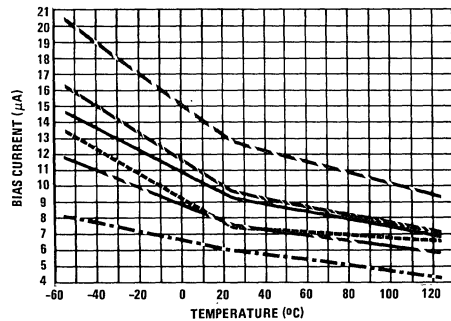
**OFFSET VOLTAGE DRIFT WITH TEMPERATURE**  
Of 6 Representative Units



**NOISE DENSITY vs. FREQUENCY**  
 $T_A = +25^\circ\text{C}$

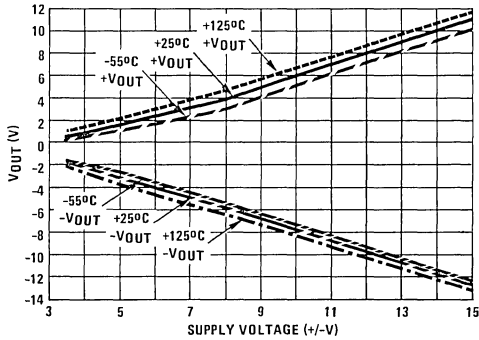


**BIAS CURRENT DRIFT WITH TEMPERATURE**  
Of 6 Representative Units

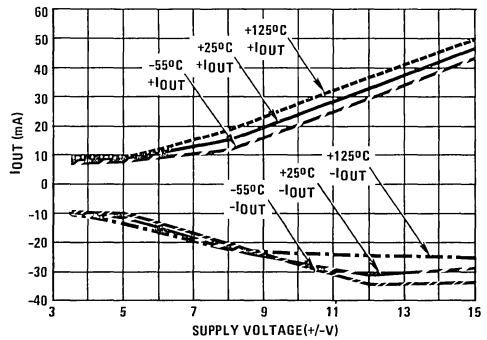


Typical Performance Curves (Continued)

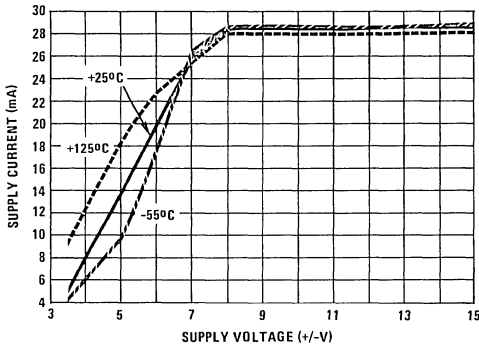
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE  
At Various Temperatures



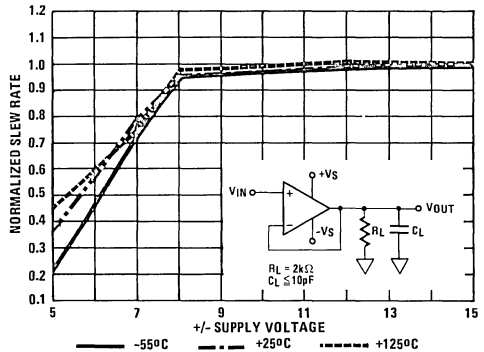
OUTPUT CURRENT vs. SUPPLY VOLTAGE  
At Various Temperatures



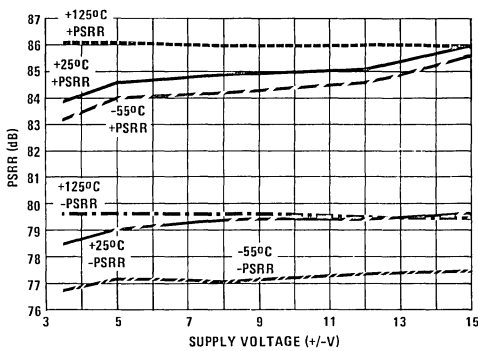
SUPPLY CURRENT vs. SUPPLY VOLTAGE  
At Various Temperatures



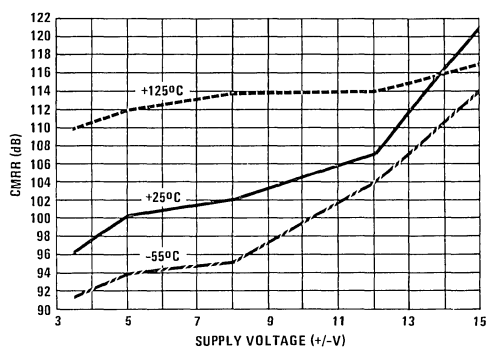
SLEW RATE vs. SUPPLY VOLTAGE  
Normalized With V<sub>S</sub> = ±15V at +25°C



PSRR vs. SUPPLY VOLTAGE  
Average of 3 Lots At Various Temperatures



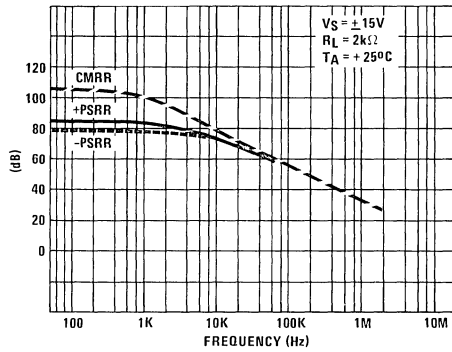
CMRR vs. SUPPLY VOLTAGE  
Average of 3 Lots At Various Temperatures



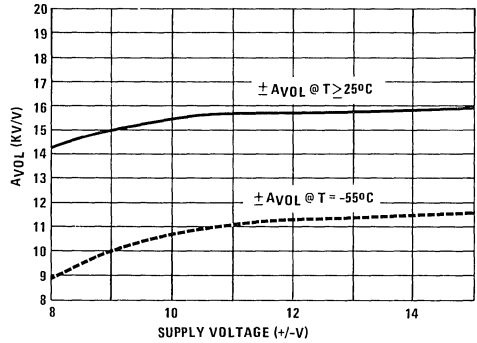


Typical Performance Curves (Continued)

REJECTION RATIOS vs. FREQUENCY

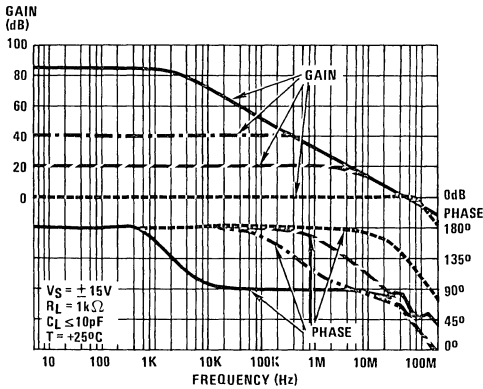


+/- OPEN LOOP GAIN vs. SUPPLY VOLTAGE  
Average of 3 Lots Over Temperature



GAIN AND PHASE FREQUENCY RESPONSE

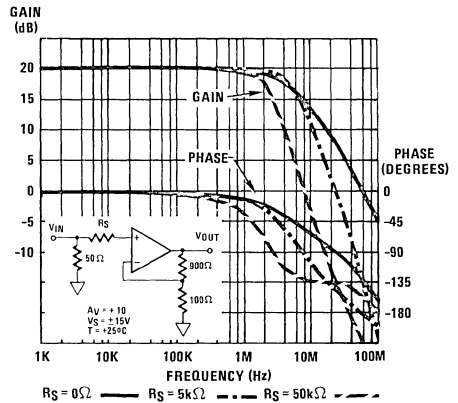
$V_S = \pm 15V, R_L = 1k, C_L \leq 10pF, T_A = +25^\circ C$



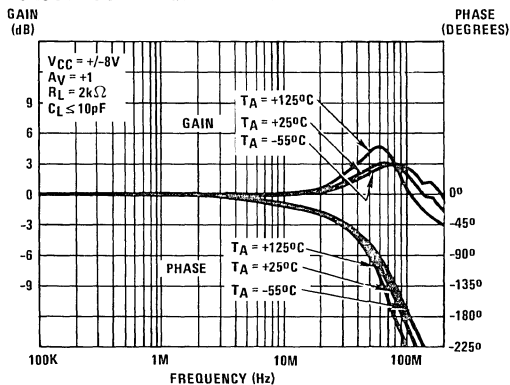
OPEN LOOP —  $A_V = -100$  - - -  $A_V = -10$  ···  $A_V = -1$

SMALL SIGNAL BANDWIDTH vs. SOURCE RESISTANCE

$V_S = \pm 15V, R_L = 1k\Omega$

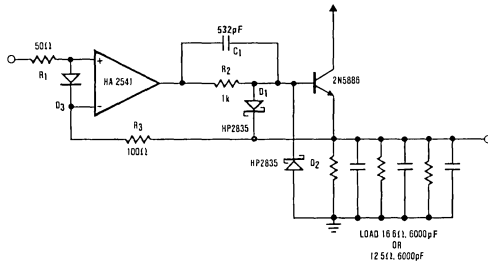


CLOSE LOOP FREQUENCY RESPONSE vs. TEMPERATURE



# HA-2541

## Applications (Also See Application Note 550)



APPLICATION 1. DRIVING POWER TRANSISTORS TO GAIN ADDITIONAL CURRENT BOOSTING

### APPLICATION 1

High power amplifiers and buffers are in use in a wide variety of applications. Many times the "high power" capability is needed to drive large capacitive loads as well as low value resistive loads. In both cases the final driver stage is usually a power transistor of some type, but because of their inherently low gain, several stages of pre-drivers are often required. The HA-2541, with its 10mA output rating, is powerful enough to drive a power transistor without additional stages of current amplification. This

capability is well demonstrated with the high power buffer circuit in Application 1.

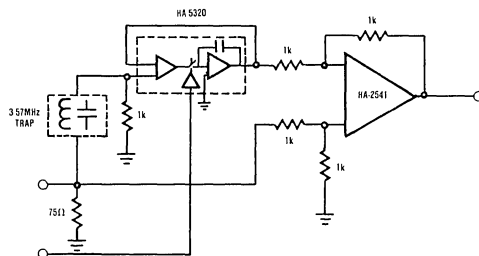
The HA-2541 acts as the pre-driver to the output power transistor. Together, they form a unity gain buffer with the ability to drive three 50 ohm coaxial cables in parallel, each with a capacitance of 2000pF. The total combined load is 16.6 ohms and 6000pF capacitance.

### APPLICATION 2

#### Video

One of the primary uses of the HA-2541 is in the area of video applications. These applications include signal construction, synchronization addition and removal, as well as signal modification. A wide bandwidth device such as the HA-2541 is well suited for use in this class of amplifier. This, however, is a more involved group of applications than ordinary amplifier applications since video signals contain precise DC levels which must be retained.

The addition of a clamping circuit restores D.C. levels at the output of an amplifier stage. The circuit shown in Application 2 utilizes the HA-5320 sample and hold amplifier as the D.C. clamp. Also shown is a 3.57MHz trap in series, which will block the color burst portion of the video signal and allow the D.C. level to be amplified and restored.



APPLICATION 2. VIDEO D.C. RESTORER

## Die Characteristics

|                                 |  |               |
|---------------------------------|--|---------------|
| Transistor Count                | 41   |               |
| Die Dimensions                  | 89 x 79 x 19 mils<br>(2250 $\mu$ m x 1990 $\mu$ m x 485 $\mu$ m) |               |
| Substrate Potential (Power Up)* | V-   |               |
| Process                         | High Frequency Bipolar   |               |
| Dielectric Isolation            |  |               |
| Passivation                     | Silox  |               |
| Thermal Constants (°C/W)        | $\theta_{ja}$  | $\theta_{jc}$ |
| Ceramic DIP                     | 91   | 35            |
| Metal Can                       | 66   | 30            |

\*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

OPERATIONAL AMPLIFIERS

## Wideband, High Slew Rate, High Output Current Operational Amplifier

August 1991

### Features

- Stable at Gains of 2 or Greater
- Gain Bandwidth ..... 70MHz
- High Slew Rate (Min.) ..... 300V/μs
- High Output Current (Min.) ..... 100mA
- Power Bandwidth (Typ.) ..... 5.5MHz
- Output Voltage Swing (Min.) ..... ±10V
- Monolithic Bipolar Dielectric Isolation Construction

### Description

The HA-2542 is a wideband, high slew rate, monolithic operational amplifier featuring an outstanding combination of speed, bandwidth, and output drive capability.

Utilizing the advantages of the Harris D. I. technology this amplifier offers 350V/μs slew rate, 70MHz gain bandwidth, and ±100mA output current. Application of this device is further enhanced through stable operation down to closed loop gains of 2.

For additional flexibility, offset null and frequency compensation controls are included in the HA-2542 pinout.

The capabilities of the HA-2542 are ideally suited for high speed coaxial cable driver circuits where low gain and high output drive requirements are necessary. With 5.5MHz full power bandwidth, this amplifier is most suitable for high

### Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- Coaxial Cable Drivers
- Fast Sample-Hold Circuits
- High Frequency Signal Conditioning Circuits

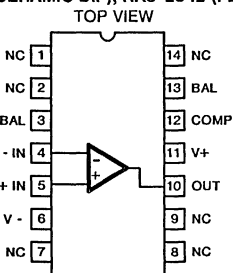
frequency signal conditioning circuits and pulse video amplifiers. Other applications utilizing the HA-2542 advantages include wideband amplifiers and fast sample-hold circuits.

The HA-2542 is available in ceramic or plastic 14 lead DIP packages, or a 12 lead metal can (TO-8) which is pin compatible with the HA-2541, HA-5190, LH0032 and HOS-050C. The HA-2542-2 is specified over the -55°C to +125°C temperature range and is also offered as a military part. The HA-2542-5 is specified over the commercial temperature range of 0°C to +75°C.

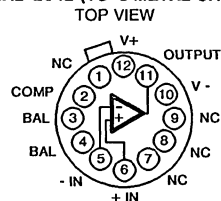
For more information on the HA-2542, please refer to Application Note 552 (Using The HA-2542), or Application Note 556 (Thermal Safe-Operating-Areas For High Current Op Amps).

### Pinouts

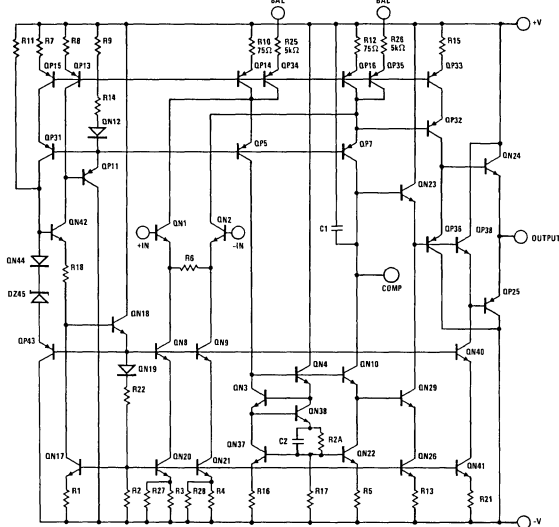
HA1-2542 (CERAMIC DIP), HA3-2542 (PLASTIC DIP)



HA2-2542 (TO-8 METAL CAN)



### Schematic



## Specifications HA-2542

### Absolute Maximum Ratings (Note 1)

|                                     |  |
|-------------------------------------|--|
| Voltage between V+ and V- Terminals | 35V                                    |
| Differential Input Voltage          | ±6V                                    |
| Output Current                      | 125mA (Peak)<br>107mA rms (Continuous) |

### Operating Temperature Range

|  |                                 |
|--|---------------------------------|
| HA-2542-2                              | -55°C ≤ T <sub>A</sub> ≤ +125°C |
| HA-2542-5                              | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| Storage Temperature Range              | -65°C ≤ T <sub>A</sub> ≤ +150°C |
| Maximum Junction Temperature (Note 11) | +175°C                          |

**Electrical Specifications** V<sub>SUPPLY</sub> = ±15 Volts; R<sub>L</sub> = 1kΩ, C<sub>L</sub> ≤ 10pF, Unless Otherwise Specified.

| PARAMETER  | TEMP              | HA-2542-2<br>-55°C to +125°C |       |      | HA-2542-5<br>0°C to +75°C |       |     | UNITS             |
|--|-------------------|------------------------------|-------|------|---------------------------|-------|-----|-------------------|
|  |                   | MIN                          | TYP   | MAX  | MIN                       | TYP   | MAX |                   |
| <b>INPUT CHARACTERISTICS</b>   |                   |                              |       |      |                           |       |     |                   |
| Offset Voltage   | +25°C             | -                            | 5     | 10   | -                         | 5     | 10  | mV                |
|  | Full              | -                            | 8     | 20   | -                         | 8     | 20  | mV                |
| Average Offset Voltage Drift   | Full              | -                            | 14    | -    | -                         | 14    | -   | μV/°C             |
| Bias Current   | +25°C             | -                            | 15    | 35   | -                         | 15    | 35  | μA                |
|  | Full              | -                            | 26    | 50   | -                         | 26    | 50  | μA                |
| Average Bias Current Drift   | Full              | -                            | 66    | -    | -                         | 45    | -   | nA/°C             |
| Offset Current   | +25°C             | -                            | 1     | 7    | -                         | 1     | 7   | μA                |
|  | Full              | -                            | -     | 9    | -                         | -     | 9   | μA                |
| Input Resistance   | +25°C             | -                            | 100   | -    | -                         | 100   | -   | kΩ                |
| Input Capacitance  | +25°C             | -                            | 1     | -    | -                         | 1     | -   | pF                |
| Common Mode Range  | Full              | ±10                          | -     | -    | ±10                       | -     | -   | V                 |
| Input Noise Voltage (0.1Hz to 100Hz)                                     | +25°C             | -                            | 2.2   | -    | -                         | 2.2   | -   | μV <sub>p-p</sub> |
| Input Noise Voltage Density (f <sub>o</sub> = 1kHz, R <sub>g</sub> = 0Ω) | +25°C             | -                            | 10    | -    | -                         | 10    | -   | nV/√Hz            |
| Input Noise Current Density (f <sub>o</sub> = 1kHz, R <sub>g</sub> = 0Ω) | +25°C             | -                            | 3     | -    | -                         | 3     | -   | pA/√Hz            |
| <b>TRANSFER CHARACTERISTICS</b>  |                   |                              |       |      |                           |       |     |                   |
| Large Signal Voltage Gain (Note 3)                                       | +25°C             | 10k                          | 30k   | -    | 10k                       | 30k   | -   | V/V               |
|  | Full              | 5k                           | 15k   | -    | 5k                        | 20k   | -   | V/V               |
| Common-Mode Rejection Ratio (Note 4)                                     | Full              | 70                           | 100   | -    | 70                        | 100   | -   | dB                |
| Minimum Stable Gain  | +25°C             | 2                            | -     | -    | 2                         | -     | -   | V/V               |
| Gain-Bandwidth-Product (Note 5)  | +25°C             | -                            | 70    | -    | -                         | 70    | -   | MHz               |
| <b>OUTPUT CHARACTERISTICS</b>  |                   |                              |       |      |                           |       |     |                   |
| Output Voltage Swing (Note 3)  | Full              | ±10                          | ±11   | -    | ±10                       | ±11   | -   | V                 |
| Output Current (Note 6)  | +25°C             | 100                          | -     | -    | 100                       | -     | -   | mA                |
| Output Resistance  | +25°C             | -                            | 5     | -    | -                         | 5     | -   | Ω                 |
| Full Power Bandwidth (Note 3 & 7)  | +25°C             | 4.7                          | 5.5   | -    | 4.7                       | 5.5   | -   | MHz               |
| Differential Gain (Note 2)   | +25°C             | -                            | 0.1   | -    | -                         | 0.1   | -   | %                 |
| Differential Phase (Note 2)  | +25°C             | -                            | 0.2   | -    | -                         | 0.2   | -   | Degrees           |
| Harmonic Distortion (Note 10)  | +25°C             | -                            | <0.04 | -    | -                         | <0.04 | -   | %                 |
| <b>TRANSIENT RESPONSE (Note 8)</b>                                       |                   |                              |       |      |                           |       |     |                   |
| Rise Time  | +25°C             | -                            | 4     | -    | -                         | 4     | -   | ns                |
| Overshoot  | +25°C             | -                            | 25    | -    | -                         | 25    | -   | %                 |
| Slew Rate  | +25°C             | 300                          | 350   | -    | 300                       | 350   | -   | V/μs              |
| Settling Time: 10V Step to 0.1%  | +25°C             | -                            | 100   | -    | -                         | 100   | -   | ns                |
|  | 10V Step to 0.01% | +25°C                        | -     | 200  | -                         | -     | 200 | -                 |
| <b>POWER REQUIREMENTS</b>  |                   |                              |       |      |                           |       |     |                   |
| Supply Current   | +25°C             | -                            | 30    | -    | -                         | 30    | -   | mA                |
|  | Full              | -                            | 31    | 34.5 | -                         | 31    | 40  | mA                |
| Power Supply Rejection Ratio (Note 9)                                    | Full              | 70                           | 79    | -    | 70                        | 79    | -   | dB                |

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 OPERATIONAL  
 AMPLIFIERS

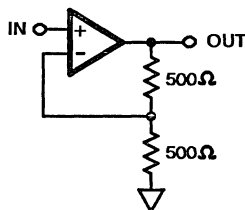
# HA-2542

## NOTES:

- Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
- Differential gain and phase are measured at 5MHz with a 1 Volt differential input voltage.
- $R_L = 1k\Omega$ ,  $V_O = \pm 10V$
- $V_{CM} = \pm 10V$
- $A_{VCL} = 100$
- $R_L = 50\Omega$ ,  $V_O = \pm 5V$
- Full Power Bandwidth guaranteed based on slew rate measurement using 
$$FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$$
- Refer to Test Circuits section of this data sheet.
- $V_{SUPPLY} = \pm 5VDC$  to  $\pm 15VDC$
- $V_{IN} = 1V_{RMS}$ ;  $f = 10kHz$ ;  $A_V = 10$ .
- This value assumes a no load condition: Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below  $+175^\circ C$ . By using Application Note 556 on Safe Operating Area equations, along with the packaging thermal resistances listed in the Die Characteristics section, proper load conditions can be determined. Heat sinking is recommended above  $+75^\circ C$  with suggested models:
  - 14 Lead Ceramic DIP: Thermalloy #6007 or AAVID #5602B ( $\theta_{sa} = 16^\circ C/W$ ).
  - 12 Lead Metal Can (TO-8): Thermalloy #2240A ( $\theta_{sa} = 27^\circ C/W$ ) or #2268B ( $\theta_{sa} = 24^\circ C/W$ )

## Test Circuits

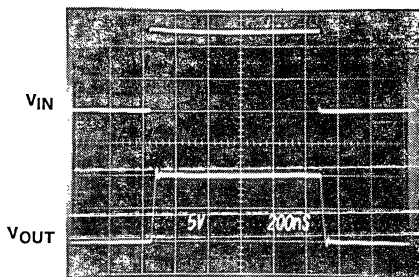
### TEST CIRCUIT



$V_S = \pm 15V$   
 $A_V = +2$   
 $C_L \leq 10pF$

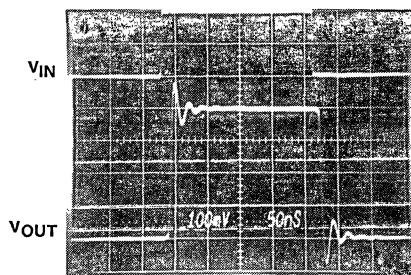
### LARGE SIGNAL RESPONSE

Vertical Scale (Volts:  $V_{IN} = 2.0V/Div.$ ,  $V_{OUT} = 5.0V/Div.$ )  
 Horizontal Scale (Time: 200ns/Div.)



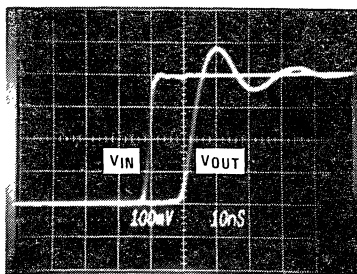
### SMALL SIGNAL RESPONSE

Vertical Scale (Volts: 100mV/Div.)  
 Horizontal Scale (Time: 50ns/Div.)



### TIME DELAY

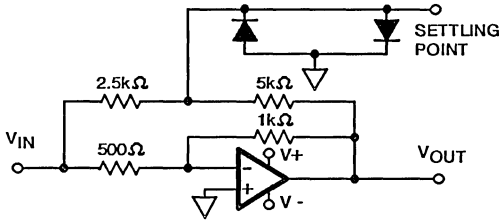
Vertical Scale (Volts: 100mV/Div.)  
 Horizontal Scale (Time: 10ns/Div.)



$V_S = \pm 15V$ ,  $R_L = 1k\Omega$   
 $T = +25^\circ C$   
 Propagation delay variance is negligible over full temperature range.

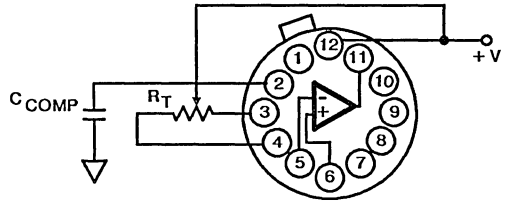
Test Circuits (Continued)

SETTLING TIME TEST CIRCUIT



- $A_V = -2$
- Feedback and summing resistors must be matched (0.1%)
- HP5082-2810 clipping diodes recommended
- Tektronix P6201 FET probe used at settling point
- For 0.01% settling time, heat sinking is suggested to reduce thermal effects and an analog ground plane with supply decoupling is suggested to minimize ground loop errors.

SUGGESTED OFFSET VOLTAGE ADJUSTMENT

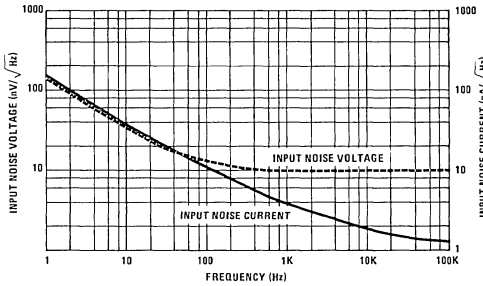


Suggested compensation scheme 5-20pF

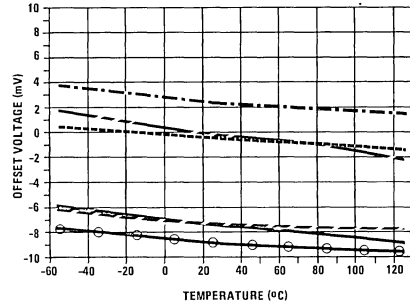
Tested Offset Adjustment Range is  $|V_{OS} + 1mV|$  minimum referred to output. Typical range is  $\pm 20mV$  with  $R_T = 5k\Omega$ .

Typical Performance Curves

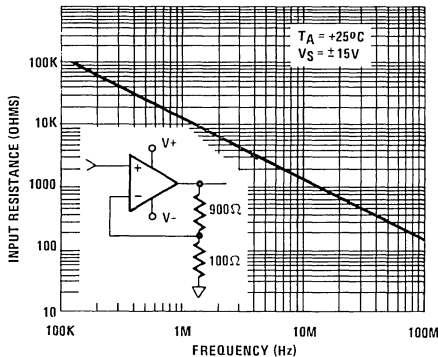
INPUT NOISE VOLTAGE AND INPUT NOISE CURRENT vs. FREQUENCY



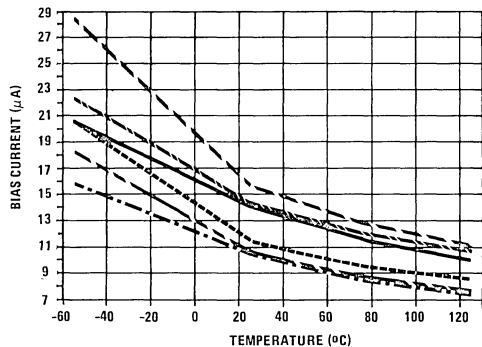
OFFSET VOLTAGE DRIFT WITH TEMPERATURE Of Six Representative Units,  $V_S = \pm 12V$



INPUT RESISTANCE vs. FREQUENCY



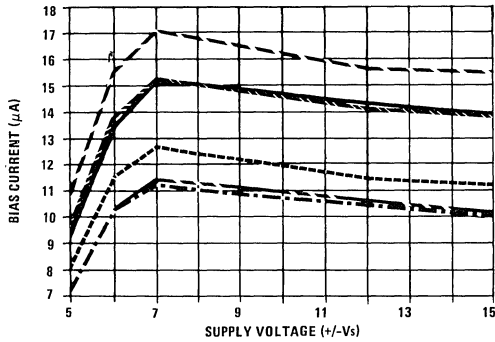
BIAS CURRENT DRIFT WITH TEMPERATURE Of Six Representative Units,  $V_S = \pm 12V$



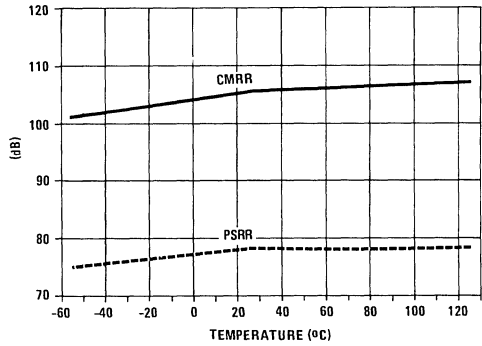
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**Typical Performance Curves (Continued)**

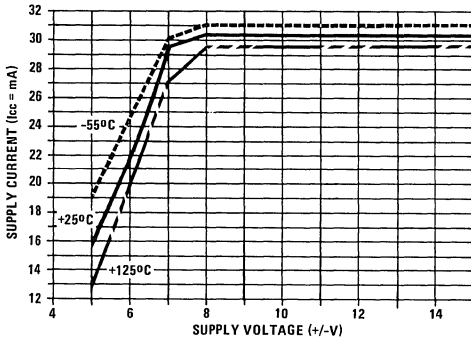
**BIAS CURRENT vs. POWER SUPPLY**  
Six Units At Various Supplies At +25°C



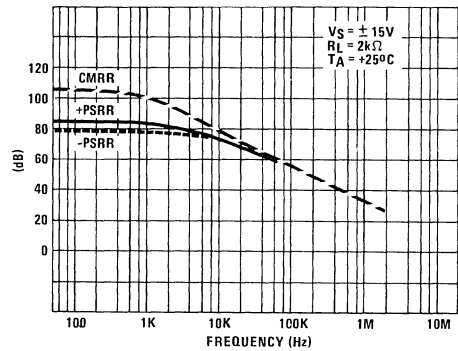
**PSRR AND CMRR vs. TEMPERATURE**  
 $V_S = \pm 15V$



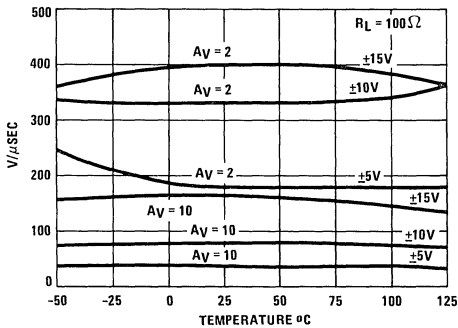
**SUPPLY CURRENT vs. SUPPLY VOLTAGE**  
At Various Temperatures



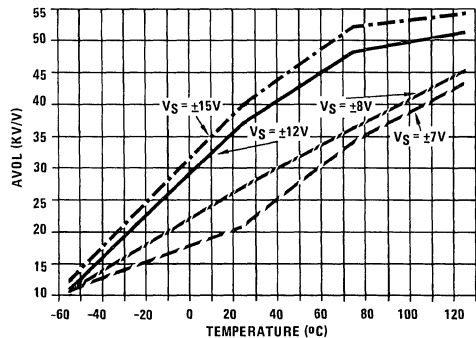
**PSRR AND CMRR vs. FREQUENCY**



**SLEW RATE vs. TEMPERATURE**  
At Various Supply Voltages With  $R_{Load} = 100\Omega$

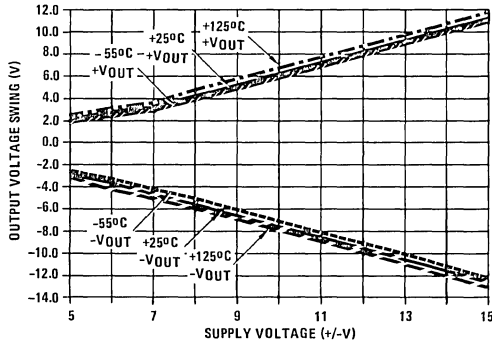


**OPEN LOOP GAIN vs. TEMPERATURE**  
At Various Supply Voltages

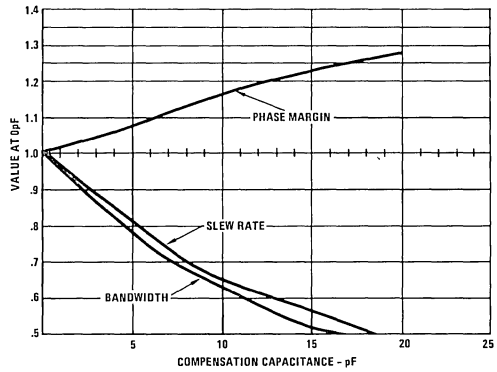


Typical Performance Curves (Continued)

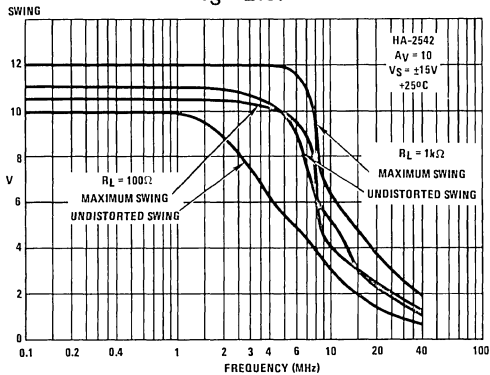
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE  
At Various Temperatures



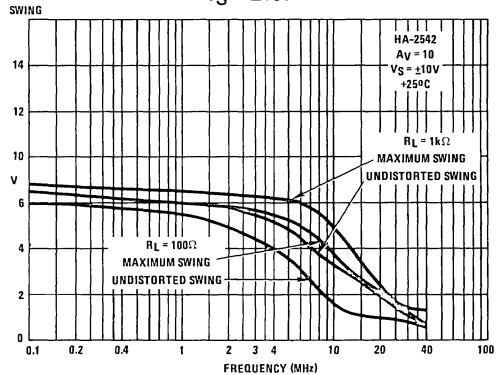
NORMALIZED AC PARAMETERS vs.  
COMPENSATION CAPACITANCE



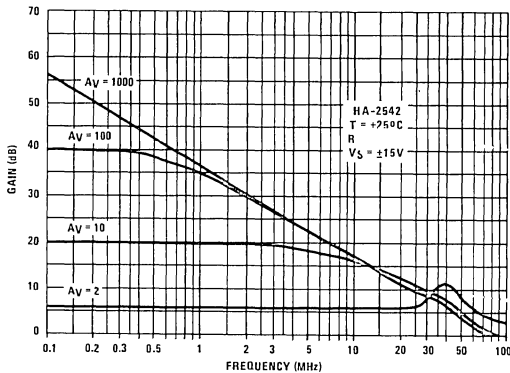
OUTPUT VOLTAGE SWING vs. FREQUENCY  
 $V_S = \pm 15V$



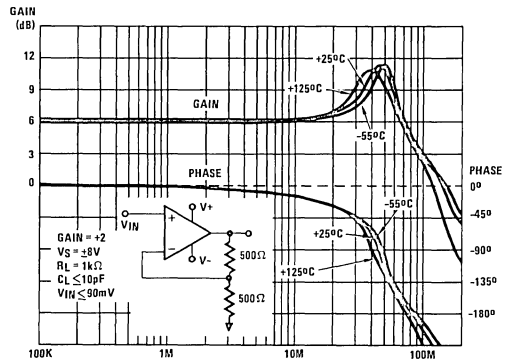
OUTPUT VOLTAGE SWING vs. FREQUENCY  
 $V_S = \pm 10V$



FREQUENCY RESPONSE CURVES



HA-2542 CLOSED LOOP GAIN vs. TEMPERATURE



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**Die Characteristics**

|                                     |   |               |
|-------------------------------------|---|---------------|
| Transistor Count .....              | 43  |               |
| Die Dimensions .....                | 72 x 105 x 19 mils<br>(1820 $\mu$ m x 2670 $\mu$ m x 485 $\mu$ m) |               |
| Substrate Potential* .....          | V-  |               |
| Process .....                       | High Frequency Bipolar-DI   |               |
| Passivation .....                   | Nitride   |               |
| Thermal Constants ( $^{\circ}$ C/W) | $\theta_{ja}$   | $\theta_{jc}$ |
| HA1-2542 Ceramic DIP                | 86.6  | 32.5          |
| HA3-2542 Plastic DIP                | 78.8  | 30.6          |
| HA2-2542 Metal Can                  | 58  | 29            |

\*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

**Typical Applications**

(Refer to Application Note 552 for Further Information)

The Harris HA-2542 is a state of the art monolithic device which also approaches the "ALL-IN-ONE" amplifier concept. This device features an outstanding set of AC parameters augmented by excellent output drive capability providing for suitable application in both high speed and high output drive circuits.

Primarily intended to be used in balanced 50 $\Omega$  and 75 $\Omega$  coaxial cable systems as a driver, the HA-2542 could also be used as a power booster in audio systems as well as a power amp in power supply circuits. This device would also be suitable as a small DC motor driver.

The applications shown on the following page demonstrate the HA-2542 at gains of +100 and +2 and as a video cable driver for small signals.

**Prototyping Guidelines**

For best overall performance in any application, it is recommended that high frequency layout techniques be used. This should include: 1) mounting the device through a ground plane; 2) connecting unused pins (N.C.) to the ground plane; 3) mounting feedback components on Teflon standoffs and or locating these components as close to the device as possible; 4) placing power supply decoupling capacitors from device supply pins to ground.

As a result of speed and bandwidth optimization, the HA-2542 can's case potential, when powered-up, is equal to the V- potential. Therefore, contact with other circuitry or ground should be avoided.

**Frequency Compensation**

The HA-2542 may be externally compensated with a single capacitor to ground. This provides the user the additional flexibility in tailoring the frequency response of the amplifier. A guideline to the response is demonstrated on the typical performance curve showing the normalized A.C. parameters versus compensation capacitance. It is suggested that the user check and tailor the accurate compensation value for each application. As shown additional phase margin is achieved at the loss of slew rate and bandwidth.

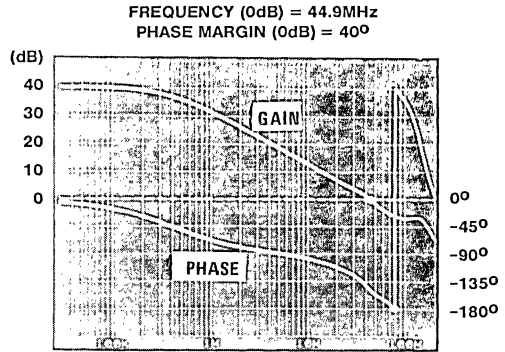
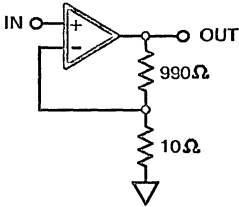
For example, for a voltage gain of +2 (or -1) and a load of 500pF/2k $\Omega$ , 20pF is needed for compensation to give a small signal bandwidth of 30MHz with 40 $^{\circ}$  of phase margin. If a full power output voltage of  $\pm$ 10V is needed, this same configuration will provide a bandwidth of 5MHz and a slew rate of 200V/ $\mu$ s.

If maximum bandwidth is desired and no compensation is needed, care must be given to minimize parasitic capacitance at the compensation pin. In some cases where minimum gain applications are desired, bending up or totally removing this pin may be the solution. In this case, care must also be given to minimize load capacitance.

For wideband positive unity gain applications, the HA-2542 can also be over-compensated with capacitance greater than 30pF to achieve bandwidths of around 25MHz. This over-compensation will also improve capacitive load handling or lower the noise bandwidth. This versatility along with the  $\pm$ 100mA output current makes the HA-2542 an excellent high speed driver for many power applications.

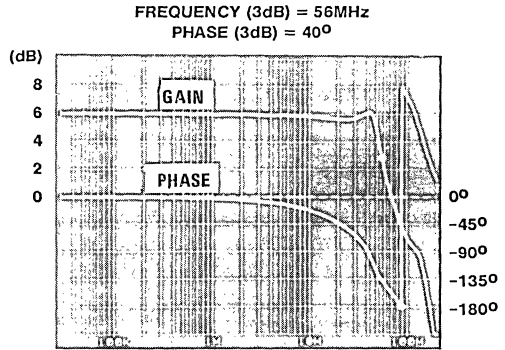
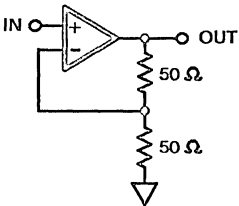
Typical Applications

NONINVERTING CIRCUIT ( $A_{VCL} = 100$ )



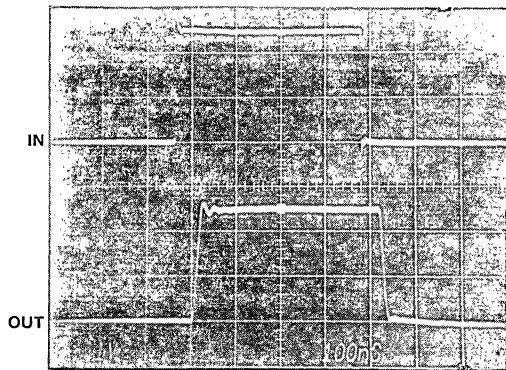
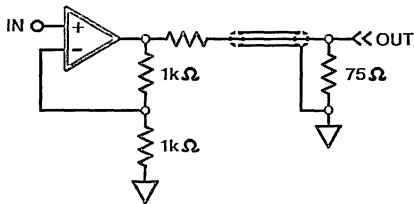
$A_{VCL} = 100$  PHASE AND GAIN

NONINVERTING CIRCUIT ( $A_{VCL} = 2$ )



$A_{VCL} = 2$  PHASE AND GAIN

VIDEO CABLE DRIVER ( $A_{VCL} = 2$ )



VIDEO CABLE DRIVER PULSE RESPONSE  
(1V/Div.; 100ns/Div.)

August 1990

## Video Operational Amplifier

### Features

- Gain Bandwidth ..... 50MHz
- High Slew Rate ..... 150V/ $\mu$ s
- Low Supply Current ..... 10mA
- Differential Gain Error ..... 0.03%
- Differential Phase Error ..... 0.03 degree
- Gain Flatness at 10MHz ..... 0.12dB

### Applications

- Video Systems
- Video Test Equipment
- Radar Displays
- Imaging Systems
- Pulse Amplifiers
- Signal Conditioning Circuits
- Data Acquisition Systems

### Description

The HA-2544 is a fast, unity gain stable, monolithic op amp designed to meet the needs required for accurate reproduction of video or high speed signals. It offers high voltage gain (6KV/V) and high phase margin (65 degrees) while maintaining tight gain flatness over the video bandwidth. Built from high quality Dielectric Isolation, the HA-2544 is another addition to the Harris series of high speed, wideband Op-Amps, and offers true video performance combined with the versatility of an op-amp.

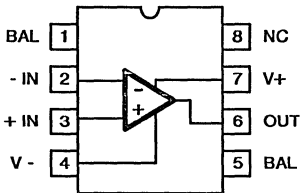
The primary features of the HA-2544 include 50MHz Gain Bandwidth, 150V/ $\mu$ s slew rate, 0.03% differential gain error and gain flatness of just 0.12dB at 10MHz. High performance and low power requirements are met with a supply current of only 10mA.

Uses of the HA-2544 range from video test equipment, guidance systems, radar displays and other precise imaging systems where stringent gain and phase requirements have previously been met with costly hybrids and discrete circuitry. The HA-2544 will also be used in non-video systems requiring high speed signal conditioning such as data acquisition systems, medical electronics, specialized instrumentation and communication systems.

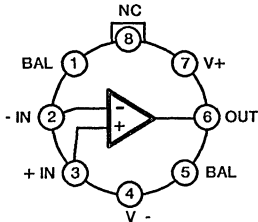
The HA-2544-2 is guaranteed over the military temperature range (-55°C to +125°C); the HA-2544/2544C-5 over the commercial range (0°C to +75°C) and the HA-2544/2544C-9 over the industrial range (-40°C to +85°C). The HA-2544 is available in TO-99 Metal Can, SOIC, and both Plastic and Ceramic Mini-DIP packages. Military (/883) product and data sheets are available upon request.

### Pinouts

HA9P2544/2544C (SOIC)  
HA7-2544 (CERAMIC MINI-DIP)  
HA3-2544/2544C (PLASTIC MINI-DIP)  
TOP VIEW

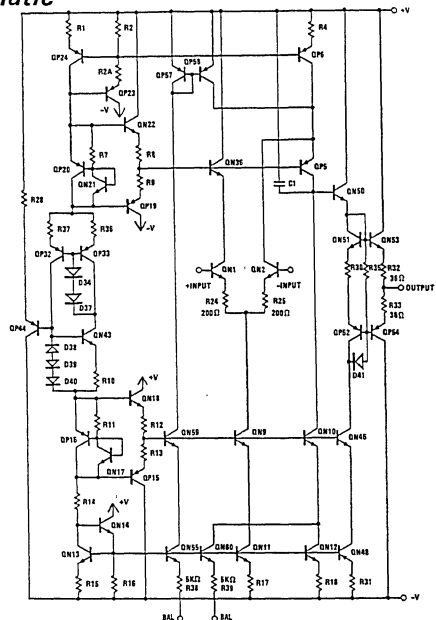


HA2-2544 (TO-99 METAL CAN)  
TOP VIEW



NOTE: V<sub>case</sub> = V-

### Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.  
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File Number 2900

## Specifications HA-2544

### Absolute Maximum Ratings (Note 1)

|  |       |
|--|-------|
| Voltage Between V+ and V- Terminals .....  | 35V   |
| Differential Input Voltage (Note 11) ..... | ±6V   |
| Output Current (Peak) .....                | ±40mA |
| Internal Power Dissipation .....           | 700mW |

### Operating Temperature Range

|                                    |  |
|------------------------------------|--|
| HA-2544/2544C-5 .....              | $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$    |
| HA-2544-9 .....                    | $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  |
| HA-2544-2 .....                    | $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ |
| Storage Temperature Range .....    | $-65^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ |
| Maximum Junction Temperature ..... | +175°C   |

**Electrical Specifications**  $V_S = \pm 15\text{V}$ ,  $C_L \leq 10\text{pF}$ ,  $R_L = 1\text{k}\Omega$ , Unless Otherwise Specified

| PARAMETER                                | TEMP   | HA-2544-2/-5 |       |     | HA-2544C-5 |       |     | UNITS                          |
|--|--------|--------------|-------|-----|------------|-------|-----|--------------------------------|
|  |        | MIN          | TYP   | MAX | MIN        | TYP   | MAX |                                |
| <b>INPUT CHARACTERISTICS</b>             |        |              |       |     |            |       |     |                                |
| Offset Voltage                           | +25°C  | -            | 6     | 15  | -          | 15    | 25  | mV                             |
|  | -2, -5 | -            | -     | 20  | -          | -     | 40  | mV                             |
|  | -9     | -            | -     | 25  | -          | -     | 40  | mV                             |
| Average Offset Voltage Drift (Note 9)    | Full   | -            | 10    | -   | -          | 10    | -   | $\mu\text{V}/^{\circ}\text{C}$ |
| Bias Current                             | +25°C  | -            | 7     | 15  | -          | 9     | 18  | $\mu\text{A}$                  |
|  | Full   | -            | -     | 20  | -          | -     | 30  | $\mu\text{A}$                  |
| Average Bias Current Drift (Note 9)      | Full   | -            | 0.04  | -   | -          | 0.04  | -   | $\mu\text{A}/^{\circ}\text{C}$ |
| Offset Current                           | +25°C  | -            | 0.2   | 2   | -          | 0.8   | 2   | $\mu\text{A}$                  |
|  | Full   | -            | -     | 3   | -          | -     | 3   | $\mu\text{A}$                  |
| Offset Current Drift                     | Full   | -            | 10    | -   | -          | 10    | -   | $\text{nA}/^{\circ}\text{C}$   |
| Common Mode Range                        | Full   | ±10          | ±11.5 | -   | ±10        | ±11.5 | -   | V                              |
| Differential Input Resistance            | +25°C  | 50           | 90    | -   | 50         | 90    | -   | k $\Omega$                     |
| Differential Input Capacitance           | +25°C  | -            | 3     | -   | -          | 3     | -   | pF                             |
| Input Noise Voltage (f = 1kHz)           | +25°C  | -            | 20    | -   | -          | 20    | -   | $\text{nV}/\sqrt{\text{Hz}}$   |
| Input Noise Current (f = 1kHz)           | +25°C  | -            | 2.4   | -   | -          | 2.4   | -   | $\text{pA}/\sqrt{\text{Hz}}$   |
| Input Noise Voltage                      |        |              |       |     |            |       |     |                                |
| 0.1Hz to 10Hz (Note 9)                   | +25°C  | -            | 1.5   | -   | -          | 1.5   | -   | $\mu\text{V p-p}$              |
| 0.1Hz to 1MHz                            | +25°C  | -            | 4.6   | -   | -          | 4.6   | -   | $\mu\text{V r.m.s.}$           |
| <b>TRANSFER CHARACTERISTICS</b>          |        |              |       |     |            |       |     |                                |
| Large Signal Voltage Gain (Notes 4, 9)   | +25°C  | 3.5          | 6     | -   | 3          | 6     | -   | kV/V                           |
|  | Full   | 2.5          | -     | -   | 2          | -     | -   | kV/V                           |
| Common Mode Rejection Ratio (Notes 6, 9) | -2, -5 | 75           | 89    | -   | 70         | 89    | -   | dB                             |
|  | -9     | 75           | 89    | -   | 65         | 89    | -   | dB                             |
| Minimum Stable Gain                      | +25°C  | +1           | -     | -   | +1         | -     | -   | V/V                            |
| Unity Gain Bandwidth (Notes 3, 9)        | +25°C  | -            | 45    | -   | -          | 45    | -   | MHz                            |
| Gain Bandwidth Product (Notes 3, 9)      | +25°C  | -            | 50    | -   | -          | 50    | -   | MHz                            |
| Phase Margin                             | +25°C  | -            | 65    | -   | -          | 65    | -   | Degrees                        |

3

OPERATIONAL  
AMPLIFIERS

## Specifications HA-2544

### Electrical Specifications (Continued)

| PARAMETER   | TEMP   | HA-2544-2/-5 |        |      | HA-2544C-5 |        |      | UNITS  |
|---|--------|--------------|--------|------|------------|--------|------|--------|
|   |        | MIN          | TYP    | MAX  | MIN        | TYP    | MAX  |        |
| <b>OUTPUT CHARACTERISTICS</b>                                 |        |              |        |      |            |        |      |        |
| Output Voltage Swing  | Full   | ±10          | ±11    | -    | ±10        | ±11    | -    | V      |
| Full Power Bandwidth (Note 7)                                 | +25°C  | 3.2          | 4.2    | -    | 3.2        | 4.2    | -    | MHz    |
| Peak Output Current (Note 9)                                  | +25°C  | ±25          | ±35    | -    | ±25        | ±35    | -    | mA     |
| Continuous Output Current (Note 9)                            | +25°C  | ±10          | -      | -    | ±10        | -      | -    | mA     |
| Output Resistance (Open Loop)                                 | +25°C  | -            | 20     | -    | -          | 20     | -    | Ω      |
| <b>TRANSIENT RESPONSE</b>                                     |        |              |        |      |            |        |      |        |
| Rise Time (Note 3)  | +25°C  | -            | 7      | -    | -          | 7      | -    | ns     |
| Overshoot (Note 3)  | +25°C  | -            | 10     | -    | -          | 10     | -    | %      |
| Slew Rate   | +25°C  | 100          | 150    | -    | 100        | 150    | -    | V/μs   |
| Settling Time (Note 5)  | +25°C  | -            | 120    | -    | -          | 120    | -    | ns     |
| <b>VIDEO PARAMETERS <math>R_L = 1k\Omega</math> (Note 10)</b> |        |              |        |      |            |        |      |        |
| Differential Phase (Note 12)                                  | +25°C  | -            | 0.03   | -    | -          | 0.03   | -    | Degree |
| Differential Gain (Notes 2, 12)                               | +25°C  | -            | 0.0026 | -    | -          | 0.0026 | -    | dB     |
|   | +25°C  | -            | 0.03   | -    | -          | 0.03   | -    | %      |
| Gain Flatness   |        |              |        |      |            |        |      |        |
|   | 5MHz   | +25°C        | -      | 0.10 | -          | -      | 0.10 | -      |
| 10MHz   | +25°C  | -            | 0.12   | -    | -          | 0.12   | -    | dB     |
| Chrominance to Luminance Gain (Note 13)                       | +25°C  | -            | 0.1    | -    | -          | 0.1    | -    | dB     |
| Chrominance to Luminance Delay (Note 13)                      | +25°C  | -            | 7      | -    | -          | 7      | -    | ns     |
| <b>POWER SUPPLY CHARACTERISTICS</b>                           |        |              |        |      |            |        |      |        |
| Supply Current  | Full   | -            | 10     | 12   | -          | 10     | 15   | mA     |
| Power Supply Rejection Ratio (Notes 8, 9)                     | -2, -5 | 70           | 80     | -    | 70         | 80     | -    | dB     |
|   | -9     | 65           | 80     | -    | 65         | 80     | -    | dB     |

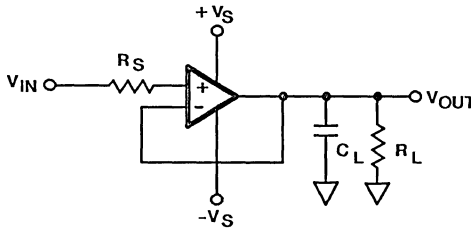
**NOTES:**

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2.  $A_D(\%) = \left[ 10^{\frac{A_D(\text{dB})}{20}} - 1 \right] \times 100$
3.  $V_{OUT} = \pm 100\text{mV}$ . For Rise Time and Overshoot testing,  $V_{OUT}$  is measured from 0 to +200mV and 0 to -200mV.
4.  $V_{OUT} = \pm 5\text{V}$
5. Settling Time is specified to 0.1% of final value for a 10V step and  $A_V = -1$
6.  $\Delta V_{CM} = \pm 10\text{V}$
7. Full Power Bandwidth is guaranteed by equation:  

$$\text{Full Power Bandwidth} = \frac{\text{Slew Rate}}{2\pi V_{\text{peak}}} \quad (V_{\text{peak used}} = 5\text{V})$$
8.  $\Delta V_S = \pm 10$  to  $\pm 20\text{V}$
9. Refer to typical performance curve in Data Sheet.
10. The video parameter specifications will degrade as the output load resistance decreases.
11. To achieve optimum AC performance, the input stage was designed without protective diode clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of the input transistors and probable degradation of the input parameters especially  $V_{OS}$ ,  $I_{OS}$  and Noise.
12. Tested with a VM700A video tester, using a NTC-7 Composite input signal. For adequate test repeatability, a minimum warm-up of 2 minutes is suggested.  $A_V = +1$ .
13. C-L Gain and C-L Delay was less than the resolution of the test equipment used which is 0.1dB and 7ns, respectively.

Test Circuits

TRANSIENT RESPONSE

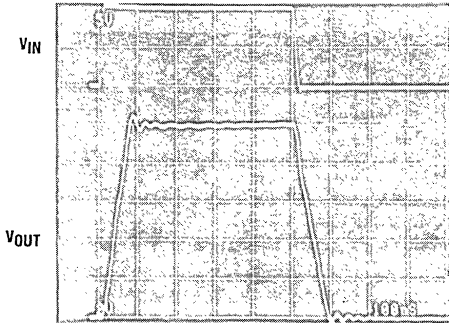


$V_S = \pm 15V$   
 $A_V = +1$   
 $R_S = 50$  or  $75\Omega$  (Optional)  
 $R_L = 1k\Omega$   
 $C_L < 10pF$

$V_{IN}$  for Large Signal =  $\pm 5V$   
 $V_{IN}$  for Small Signal = 0 to  $+200mV$   
 and 0 to  $-200mV$

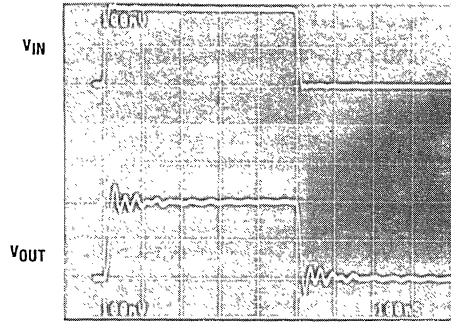
LARGE SIGNAL RESPONSE

$V_{OUT} = 0$  to  $+10V$   
 Vertical Scale: ( $V_{IN} = 5V/Div.$ ;  $V_{OUT} = 2V/Div.$ )  
 Horizontal Scale: (100ns/Div.)

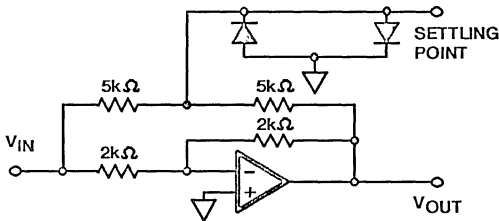


SMALL SIGNAL RESPONSE

$V_{OUT} = 0$  to  $+200mV$   
 Vertical Scale: ( $V_{IN} = 100mV/Div.$ ;  $V_{OUT} = 100mV/Div.$ )  
 Horizontal Scale: (100ns/Div.)

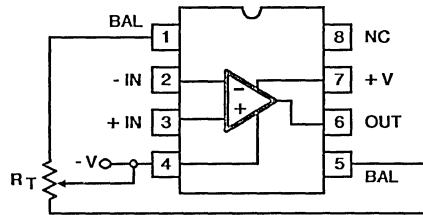


SETTLING TIME TEST CIRCUIT



- $A_V = -1$
- Feedback and Summing Resistors Must Be Matched (0.1%)
- HP5082-2810 Clipping Diodes Recommended.
- Tektronix P6201 FET Probe Used At Settling Point.

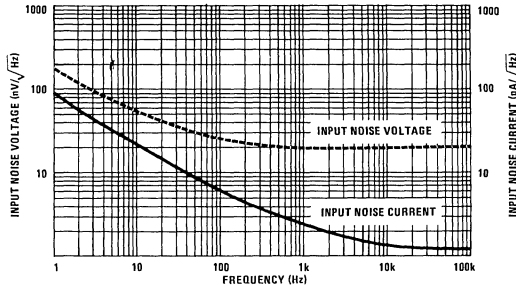
OFFSET VOLTAGE ADJUSTMENT



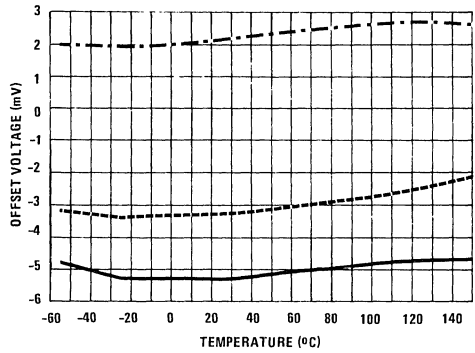
Tested Offset Adjustment Range Is  $|V_{OS} + 1mV|$  Minimum Referred To Output. Typical Range For  $R_T = 20k\Omega$  Is Approximately  $\pm 30mV$

Typical Performance Curves

INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY



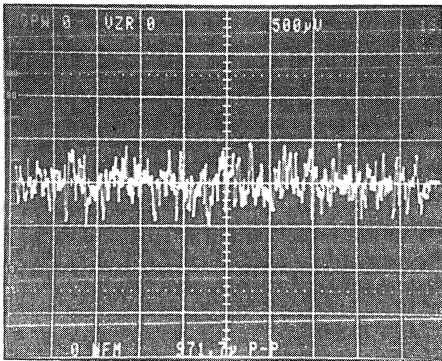
INPUT OFFSET VOLTAGE vs. TEMPERATURE  
3 Typical Units



NOISE VOLTAGE

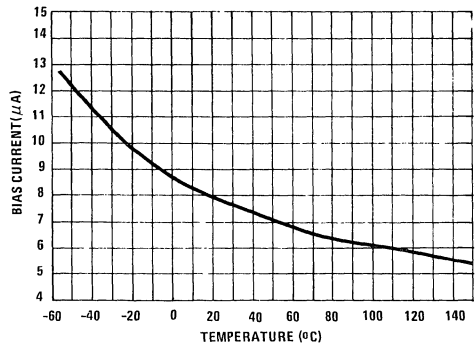
( $A_v = 1000$ )

0.1Hz to 10Hz, Noise Voltage =  $0.97 \mu\text{Vp-p}$



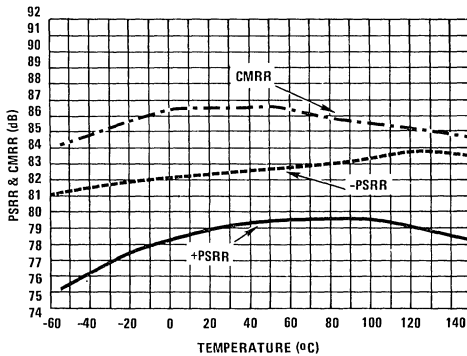
INPUT BIAS CURRENT vs. TEMPERATURE

$V_S = \pm 15\text{V}$ ,  $R_L = 1\text{k}\Omega$



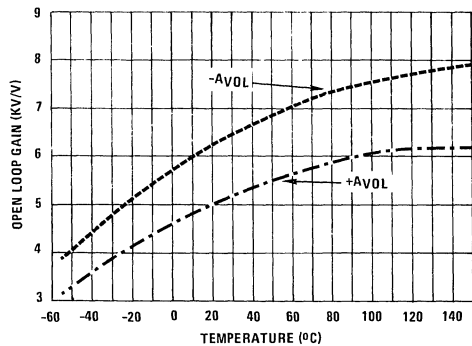
PSRR and CMRR vs. TEMPERATURE

$V_S = \pm 15\text{V}$ ,  $R_L = 1\text{k}\Omega$



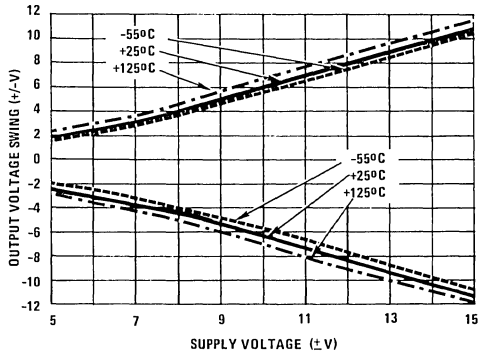
OPEN LOOP GAIN vs. TEMPERATURE

$V_S = \pm 15\text{V}$ ,  $R_L = 1\text{k}\Omega$

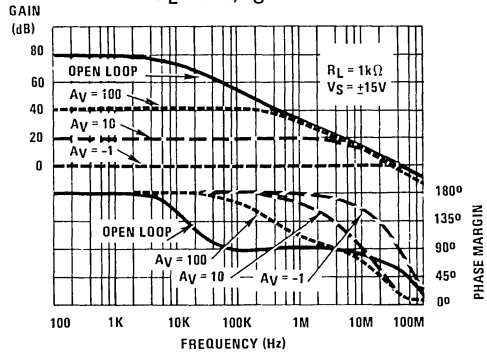


Typical Performance Curves (Continued)

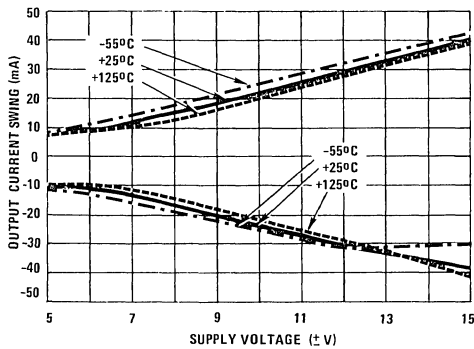
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE  
(Over Full Temperature)



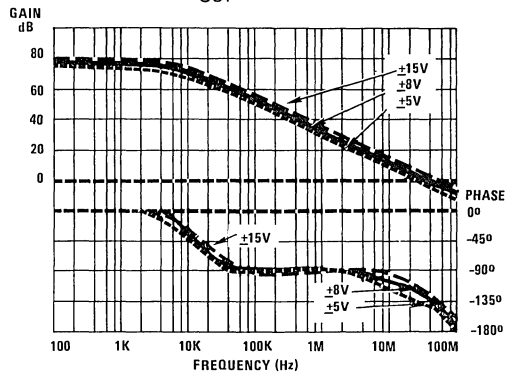
FREQUENCY RESPONSE AT VARIOUS GAINS  
 $R_L = 1k\Omega, V_S = \pm 15V$



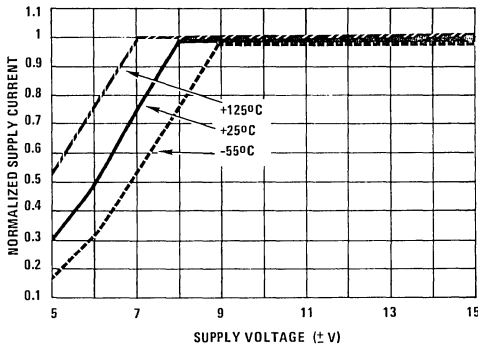
OUTPUT CURRENT vs. SUPPLY VOLTAGE  
(Over Full Temperature)



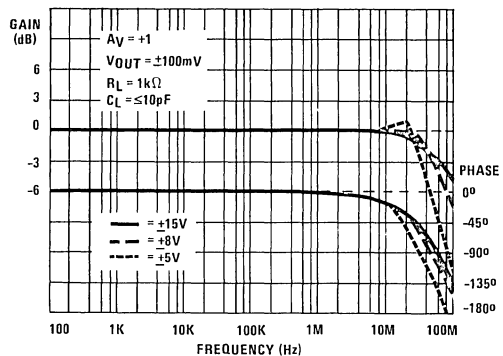
OPEN LOOP RESPONSE vs. SUPPLY VOLTAGE  
 $V_{OUT} = \pm 100mV$



SUPPLY CURRENT vs. SUPPLY VOLTAGE  
Normalized at  $V_S = \pm 15V$  at  $+25^\circ C$



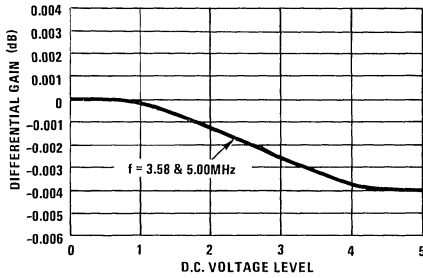
VOLTAGE FOLLOWER RESPONSE vs. SUPPLY VOLTAGE  
 $A_V = +1, R_L = 1K, C_L < 10pF$



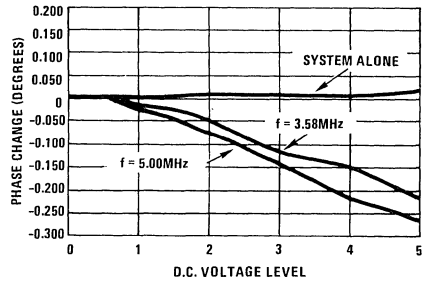


**Typical Video Performance**

**A.C. GAIN VARIATION vs. D.C. OFFSET LEVELS**  
(Differential Gain)

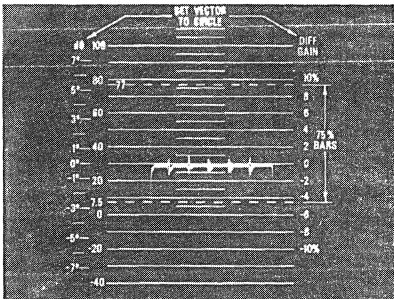


**A.C. PHASE VARIATION vs. D.C. OFFSET LEVELS**  
(Differential Phase)



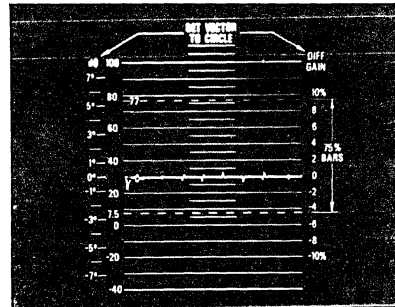
**DIFFERENTIAL GAIN**

NTSC Method,  $R_L = 1k\Omega$   
Differential Gain  $< 0.05\%$  at  $T_A = +75^\circ C$   
No Visual Difference at  $T_A = -55^\circ C$  or  $+125^\circ C$



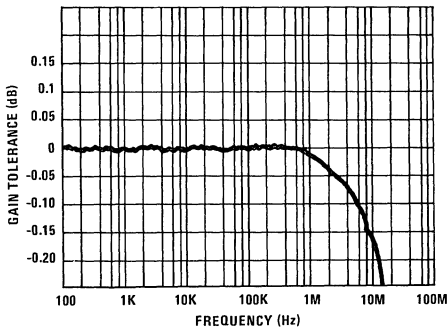
**DIFFERENTIAL PHASE**

NTSC Method,  $R_L = 1k\Omega$   
Differential Phase  $< 0.05$  Degree at  $T_A = +75^\circ C$   
No Visual Difference at  $T_A = -55^\circ C$  or  $+125^\circ C$



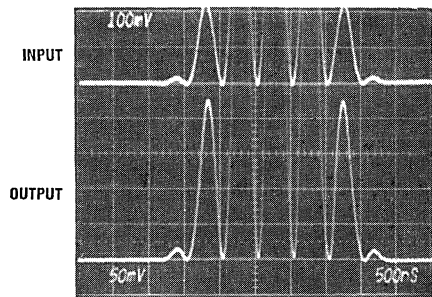
**GAIN FLATNESS**

$A_V = +1$ ,  $V_{IN} = \pm 100mV$   
 $R_L = 1K$ ,  $C_L < 10pF$



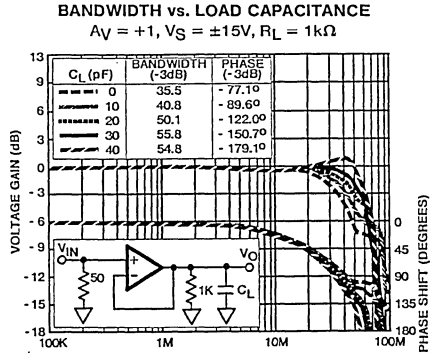
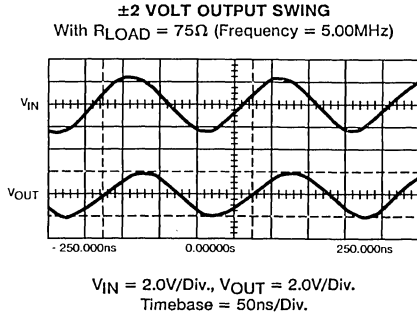
**CHROMINANCE TO LUMINANCE DELAY**

NTSC Method,  $R_L = 1k\Omega$   
C-L Delay  $< 7ns$  at  $T_A = +75^\circ C$   
No Visual Difference at  $T_A = -55^\circ C$  or  $+125^\circ C$



Vertical Scale: Input = 100mV/Div.  
Output = 50mV/Div.  
Horizontal Scale: 500ns/Div.

Typical Video Performance Curves (Continued)



Applications And Product Guidelines

The HA-2544 is a true differential op amp that is as versatile as any op amp but offers the advantages of high unity gain bandwidth, high speed and low supply current. More important than its' general purpose applications is that the HA-2544 was especially designed to meet the requirements found in a video amplifier system. These requirements include fine picture resolution and accurate color rendition, and must meet broadcast quality standards.

In a video signal, the video information is carried in the amplitude and phase as well as in the D.C. level. The amplifier must pass the 30Hz line rate luminance level and the 3.58MHz (NTSC) or 4.43MHz (PAL) color band without altering phase or gain. The HA-2544's key specifications aimed at meeting this include high bandwidth (50MHz), very low gain flatness (0.12dB at 10MHz), near unmeasurable differential gain and differential phase (0.03% and 0.03 degrees), and low noise (20nV/√Hz). The HA-2544 meets these guidelines and are sample tested for /883 grade product at 5 and/or 10MHz. If a customer wishes to 100% test these specifications, arrangement can be made.

The HA-2544 also offers the advantage of a full output voltage swing of ±10V into a 1K ohm load. This equates to a full power bandwidth of 2.4MHz for this ±10V signal. If video signal levels of ±2V maximum is used (with  $R_L = 1K\ \text{ohm}$ ), the full power bandwidth would be 11.9MHz without clipping distortion. Another usage might be required for a direct 50 ohm or 75 ohm load where the HA-2544 will still swing this ±2V signal as shown in the above display. One important note that must be realized is that as load resistance decreases the video parameters are also degraded. For optimal video performance a 1kΩ load is recommended.

If lower supply voltage are required, such as ±5V, many of the characterization curves indicate where the parameters vary. As shown the bandwidth, slew rate and supply current are still very well maintained.

Prototyping and PC Board Layout

When designing with the HA-2544 video op amp as with any high performance device, care should be taken to use

high frequency layout techniques to avoid unwanted parasitic effects. Short lead lengths, low source impedance and lower value feedback resistors help reduce unwanted poles or zeros. This layout would also include ground plane construction and power supply decoupling as close to the supply pins with suggested parallel capacitors of 0.1μF and 0.001μF ceramic to ground.

In the noninverting configuration, the amplifier is sensitive to stray capacitance (<40pF) to ground at the inverting input. Therefore, the inverting node connections should be kept to a minimum. Phase shift will also be introduced as load parasitic capacitance is increased. A small series resistor (20 ohm to 100 ohm) before the capacitance effectively decouples this effect.

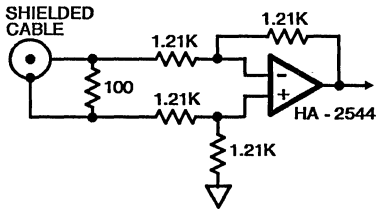
Stability/Phase Margin/Compensation

The HA-2544 has not sacrificed unity gain stability in achieving its superb AC performance. For this device, the phase margin exceeds 60 degrees at the unity crossing point of the open loop frequency response. Large phase margin is critical in order to reduce the differential phase and differential gain errors caused by most other op amps. Because this part is unity gain stable, no compensation pin is brought out. If compensation is desired to reduce the noise bandwidth, most standard methods may be used. One method suggested for an inverting scheme would be a series R-C from the inverting node to ground which will reduce bandwidth, but not effect slew rate. If the user wishes to achieve even higher bandwidth (>50MHz), and can tolerate some slight gain peaking and lower phase margin, experimenting with various load capacitance can be done.

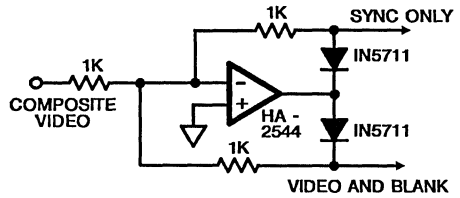
Shown in Application 1 is an excellent Differential Input, Unity Gain Buffer which also will terminate a cable to 75 ohm and reject common-mode voltages. Application 2 is a method of separating a video signal up into the Sync. only signal and the Video and Blanking signal. Application 3 shows the HA-2544 being used as a 100kHz High Pass 2-Pole Butterworth Filter. Also shown is the measured frequency response curves.

**Typical Application**

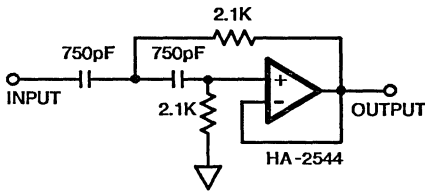
**APPLICATION 1**  
75Ω Differential Input Buffer



**APPLICATION 2**  
Composite Video Sync. Separator

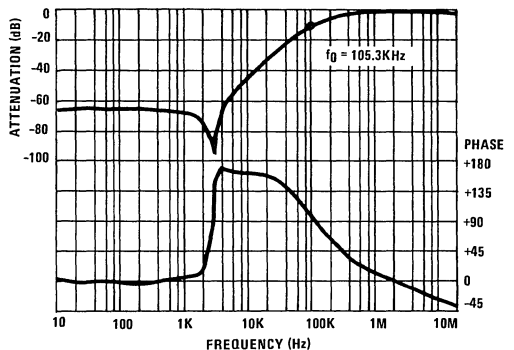


**APPLICATION 3**  
100kHz High Pass 2-Pole Butterworth Filter



$$f_0 = \frac{1}{2\pi(2.1K \cdot 750pF)}$$

**Measured Frequency Response of Application 3**



**Die Characteristics**

|                                  |  |                 |
|----------------------------------|--|-----------------|
| Transistor Count .....           | 44   |                 |
| Die Dimensions .....             | 80 x 65 x 19 mils<br>(2030 x 1630 x 485µm) |                 |
| Substrate Potential* .....       | V-   |                 |
| Process .....                    | High Frequency Bipolar D.I.                |                 |
| Passivation .....                | Nitride                                    |                 |
| Thermal Constants (°C/W)         | θ <sub>ja</sub>                            | θ <sub>jc</sub> |
| Metal Can TO-99, HA2-2544        | 186  | 50              |
| Plastic Mini-DIP, HA3-2544/2544C | 80   | 20              |
| Ceramic Mini-DIP, HA7-2544       | 185  | 98              |
| SOIC, HA9P2544                   | 160  | 42              |

\*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

August 1991

### Features

- High Slew Rate ..... 120V/ $\mu$ s
- Low Offset Voltage ..... 300 $\mu$ V
- High Open Loop Gain ..... 130dB
- Gain Bandwidth Product ..... 150MHz
- Low Voltage Noise @ 1kHz ..... 8.3nV/ $\sqrt{\text{Hz}}$
- Minimum Gain Stability .....  $\geq 5$

### Applications

- High Speed Instrumentation
- Data Acquisition Systems
- Analog Signal Conditioning
- Precision, Wideband Amplifiers
- Pulse/RF Amplifiers

### Description

The HA-2548 is a monolithic op amp that offers a unique combination of bandwidth, slew rate, and precision specifications. These features can eliminate the need for composite op amp designs and external calibration circuitry.

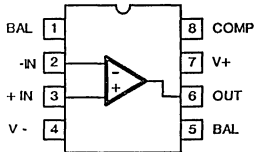
Optimized for gains  $\geq 5$ , the HA-2548 has a gain-bandwidth product of 150MHz and a slew rate of 120V/ $\mu$ s while maintaining extremely high open loop gain (130dB typ) and low offset voltage (300 $\mu$ V typ). These specifications are achieved through uniquely designed input circuitry and a single ultra-high gain stage that minimizes the AC signal path. Capable of delivering over 30mA of output current, the HA-2548 is ideal for precision, high speed applications such as signal conditioning, instrumentation, video/pulse amplifiers and buffers.

The HA-2548 is offered with a -5 temperature grade guaranteed between 0°C and +75°C and a -9 temperature grade guaranteed between -40°C and +85°C. Both grades are available in either a Ceramic Sidebraced DIP or a TO-99 Metal Can. The HA-2548 is also available in SOIC packaging with -5 temperature range. For information on the military version of this device please refer to the HA-2548/883 datasheet.

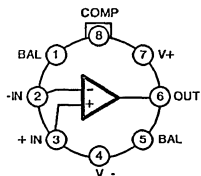
3  
OPERATIONAL  
AMPLIFIERS

### Pinouts

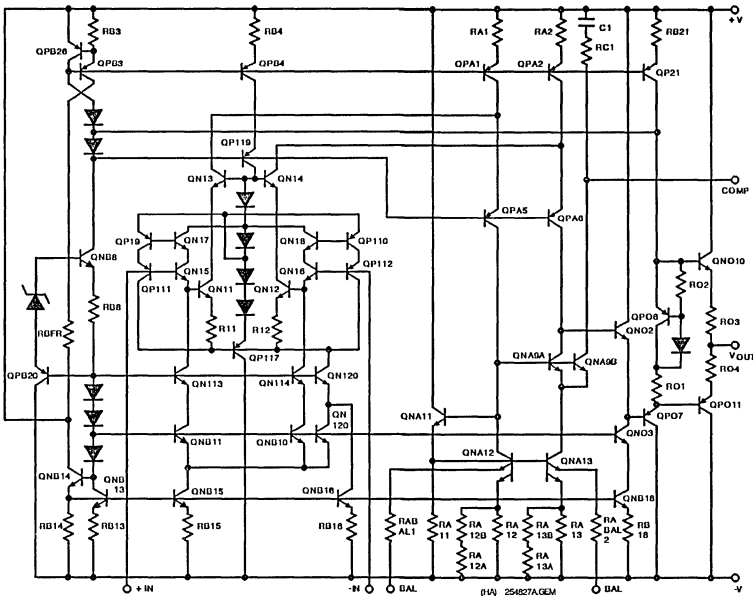
HA7-2548  
(CERAMIC SIDEBRAZED DIP)  
HA9P2548 (SOIC)  
TOP VIEW



HA2-2548  
(TO-99 METAL CAN)  
TOP VIEW



### Schematic (Simplified)



## Specifications HA-2548

### Absolute Maximum Ratings (Note 1)

|   |      |
|---|------|
| Voltage Between V+ and V- Terminals ..... | 40V  |
| Differential Input Voltage .....          | 5V   |
| Output Current .....                      | 40mA |

### Operating Temperature Range:

|                                    |  |
|------------------------------------|--|
| HA-2548-5 .....                    | $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$    |
| HA-2548-9 .....                    | $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  |
| Storage Temperature Range .....    | $-65^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ |
| Maximum Junction Temperature ..... | $+175^{\circ}\text{C}$                                   |

### Electrical Specifications V+ = +15V, V- = -15V, R<sub>L</sub> = 1K, C<sub>L</sub> = 10pF. (Unless Otherwise Specified)

| PARAMETER                              | TEMP                           | HA-2548-5, -9 |      |      | HA-2548A-5 |      |     | UNITS  |      |
|--|--------------------------------|---------------|------|------|------------|------|-----|--------|------|
|  |                                | MIN           | TYP  | MAX  | MIN        | TYP  | MAX |        |      |
| <b>INPUT CHARACTERISTICS</b>           |                                |               |      |      |            |      |     |        |      |
| Input Offset Voltage                   | +25°C                          | -             | 300  | 900  | -          | 100  | 300 | μV     |      |
|  | Full                           | -             | 400  | 1200 | -          | 200  | 600 | μV     |      |
| Average Offset Voltage Drift (Note 12) | Full                           | -             | 4    | 9    | -          | 3    | 7   | μV/°C  |      |
| Input Bias Current                     | +25°C                          | -             | 5    | 50   | -          | 5    | 50  | nA     |      |
|  | Full                           | -             | 20   | 100  | -          | 20   | 100 | nA     |      |
| Input Offset Current                   | +25°C                          | -             | 5    | 50   | -          | 5    | 50  | nA     |      |
|  | Full                           | -             | 20   | 100  | -          | 20   | 100 | nA     |      |
| Common Mode Range                      | +25°C                          | ±7            | ±10  | -    | ±7         | ±10  | -   | V      |      |
| Differential Input Resistance          | +25°C                          | -             | 1    | -    | -          | 1    | -   | MΩ     |      |
| Input Noise Voltage                    | f <sub>o</sub> = 0.1Hz to 10Hz | +25°C         | -    | 0.2  | -          | -    | 0.2 | μVrms  |      |
|  | f <sub>o</sub> = 0.1Hz to 1MHz | +25°C         | -    | 0.8  | -          | -    | 0.8 | μVrms  |      |
| Input Noise Voltage Density            | f <sub>o</sub> = 10Hz          | +25°C         | -    | 30   | -          | -    | 30  | nV/√Hz |      |
| (Note 2)                               | f <sub>o</sub> = 100Hz         | +25°C         | -    | 12   | -          | -    | 12  | nV/√Hz |      |
|  | f <sub>o</sub> = 1000Hz        | +25°C         | -    | 8.3  | -          | -    | 8.3 | nV/√Hz |      |
| Input Noise Current Density            | f <sub>o</sub> = 10Hz          | +25°C         | -    | 1.9  | -          | -    | 1.9 | pA/√Hz |      |
| (Note 2)                               | f <sub>o</sub> = 100Hz         | +25°C         | -    | 0.7  | -          | -    | 0.7 | pA/√Hz |      |
|  | f <sub>o</sub> = 1000Hz        | +25°C         | -    | 0.4  | -          | -    | 0.4 | pA/√Hz |      |
| <b>TRANSFER CHARACTERISTICS</b>        |                                |               |      |      |            |      |     |        |      |
| Large Signal Voltage Gain (Note 3)     | +25°C                          | 114           | 130  | -    | 120        | 130  | -   | dB     |      |
|  | Full                           | 108           | 125  | -    | 118        | 125  | -   | dB     |      |
| Common Mode Rejection Ratio (Note 4)   | Full                           | 80            | 90   | -    | 80         | 90   | -   | dB     |      |
| Gain Bandwidth Product (Note 5,12)     | +25°C                          | 130           | 150  | -    | 130        | 150  | -   | MHz    |      |
|  | Full                           | 110           | 125  | -    | 110        | 125  | -   | MHz    |      |
| Minimum Stable Gain                    | Full                           | 5             | -    | -    | 5          | -    | -   | V/V    |      |
| <b>OUTPUT CHARACTERISTICS</b>          |                                |               |      |      |            |      |     |        |      |
| Output Voltage Swing                   | Full                           | ±11           | ±12  | -    | ±11        | ±12  | -   | Volts  |      |
| Output Current (Note 6)                | Full                           | ±30           | ±33  | -    | ±30        | ±33  | -   | mA     |      |
| Output Resistance                      | +25°C                          | -             | 5    | -    | -          | 5    | -   | Ω      |      |
| Full Power Bandwidth (Note 7,12)       | +25°C                          | -             | 1.91 | -    | -          | 1.91 | -   | MHz    |      |
| <b>TRANSIENT RESPONSE</b>              |                                |               |      |      |            |      |     |        |      |
| Slew Rate (Note 8,12)                  | Positive                       | +25°C         | 80   | 120  | -          | 80   | 120 | -      | V/μs |
|  | Full                           | 70            | 105  | -    | 70         | 105  | -   | V/μs   |      |
|  | Negative                       | +25°C         | 70   | 110  | -          | 70   | 110 | -      | V/μs |
|  | Full                           | 60            | 105  | -    | 60         | 105  | -   | V/μs   |      |
| Rise Time (Note 9,12)                  | +25°C                          | -             | 16.5 | 20   | -          | 16.5 | 20  | ns     |      |
|  | Full                           | -             | 19   | 23   | -          | 19   | 23  | ns     |      |
| Fall Time (Notes 9,12)                 | +25°C                          | -             | 16   | 20   | -          | 16   | 20  | ns     |      |
|  | Full                           | -             | 18   | 23   | -          | 18   | 23  | ns     |      |
| Overshoot (Note 9,12)                  | Positive                       | +25°C         | -    | 15   | 25         | -    | 15  | 25     | %    |
|  | Full                           | -             | 25   | 35   | -          | 25   | 35  | %      |      |
|  | Negative                       | +25°C         | -    | 8    | 15         | -    | 8   | 15     | %    |
|  | Full                           | -             | 20   | 30   | -          | 20   | 30  | %      |      |
| Settling Time (Note 10,12)             | +25°C                          | -             | 200  | 260  | -          | 200  | 260 | ns     |      |
| <b>POWER SUPPLY</b>                    |                                |               |      |      |            |      |     |        |      |
| PSRR (Note 11)                         | Full                           | 86            | 95   | -    | 86         | 95   | -   | dB     |      |
| I <sub>CC</sub>                        | Full                           | -             | 12   | 18   | -          | 12   | 18  | mA     |      |

# HA-2548

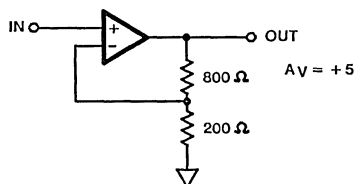
**NOTES:**

1. Absolute maximum ratings are limiting values, applied individually, beyond which the servability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Refer to typical performance curve in data sheet.
3.  $V_{OUT} = \pm 10V$ .
4.  $V_{CM} = \pm 2V$ .
5. Characterized in an  $A_V = -100$  configuration from 100kHz to 10MHz.
6.  $R_L = 1k\Omega$ ,  $V_{OUT} > 10V$ .
7. Full Power Bandwidth is calculated by:  

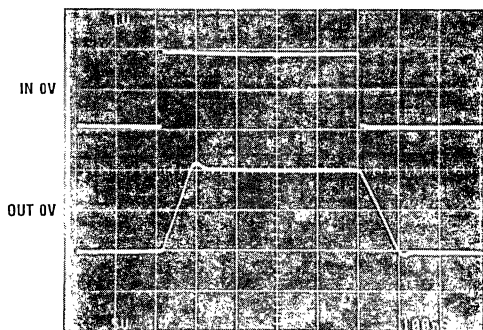
$$FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}}, V_{peak} = 10V$$
8.  $V_{OUT} = \pm 5V$ ,  $A_V = +5$ .
9.  $V_{OUT} = \pm 100mV$ ,  $A_V = +5$ .
- 10 Settling time is specified to 0.01% with a 10V step and  $A_V = -5$ .
11. Delta  $V_S = \pm 10V$  to  $\pm 20V$ .
12. These parameters are not tested. The limits are guaranteed based on lab characterization and reflect lot to lot variation.

## Test Circuits and Waveforms

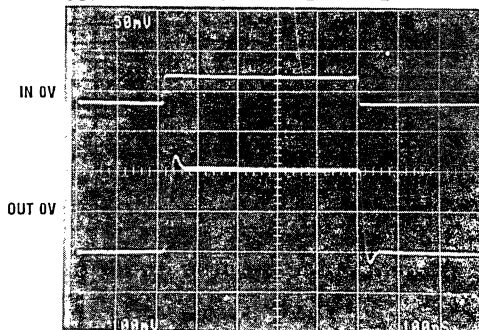
### LARGE AND SMALL SIGNAL RESPONSE CIRCUIT



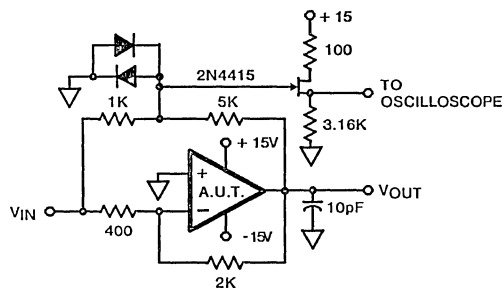
**LARGE SIGNAL RESPONSE**  
 $V_{OUT} = \pm 5V$ ,  $A_V = +5$ ,  $R_L = 1K$ ,  $C_L \leq 10pF$



**SMALL SIGNAL RESPONSE**  
 $V_{OUT} = \pm 100mV$ ,  $A_V = +5$ ,  $R_L = 1K$ ,  $C_L \leq 10pF$

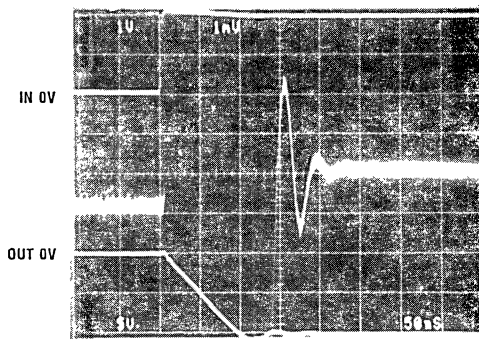


### SETTLING TIME TEST CIRCUIT



- $A_V = -5$
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

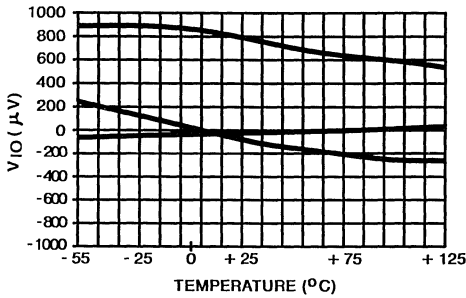
**HA-2548 SETTling TIME**  
 $A_V = -5$ , Output = -10V Output Scale Vertical: 1mV/Div  
 Horizontal: 50ns/Div



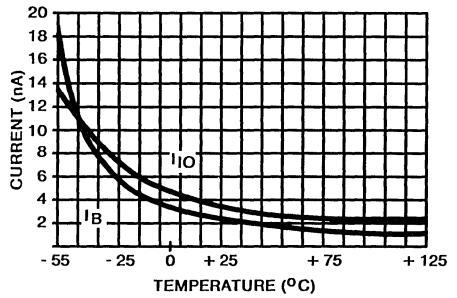
3  
OPERATIONAL AMPLIFIERS

**Typical Performance Curves**  $V_S = \pm 15V, T_A = +25^\circ C$

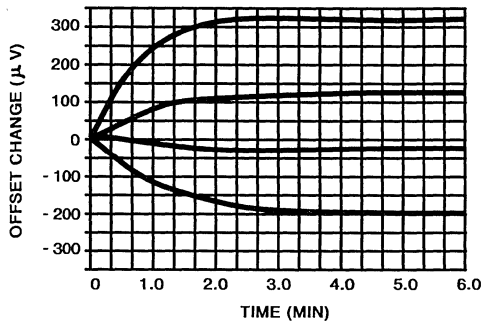
**$V_{IO}$  vs TEMPERATURE**  
(3 Representative Units)



**OFFSET CURRENT/BIAS CURRENT vs TEMPERATURE**

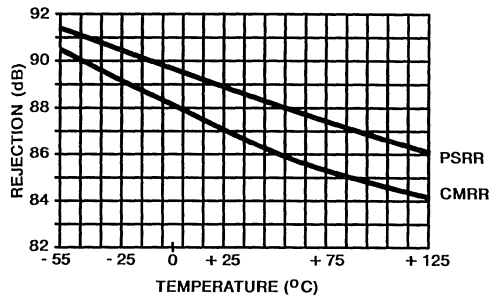


**$V_{IO}$  WARM-UP DRIFT (NORMALIZED FROM ZERO)**  
(4 Representative Units)

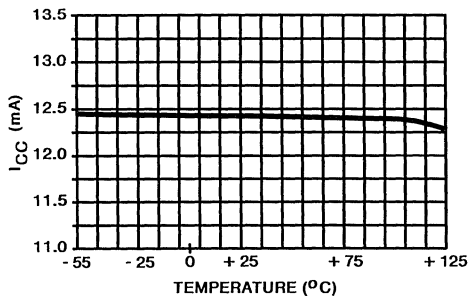


**PSRR/CMRR vs TEMPERATURE**

$V_{CC} = \pm 15V, V_{CM} = \pm 2V, V_S = \pm 10V$  to  $\pm 20V$

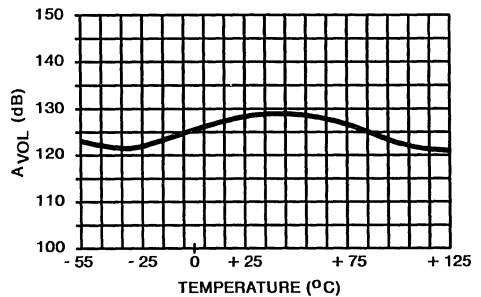


**$I_{CC}$  vs TEMPERATURE**



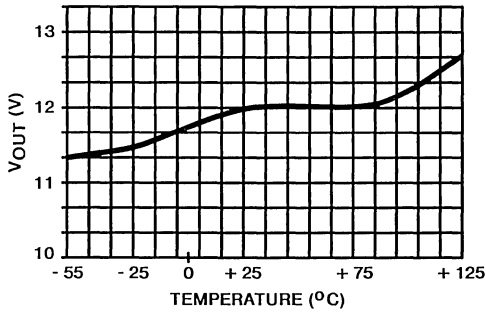
**$A_{VOL}$  vs TEMPERATURE**

$V_{CC} = \pm 15V, R_L = 1K\Omega$   
 $C_L \leq 10pF, V_{OUT} = \pm 10V$

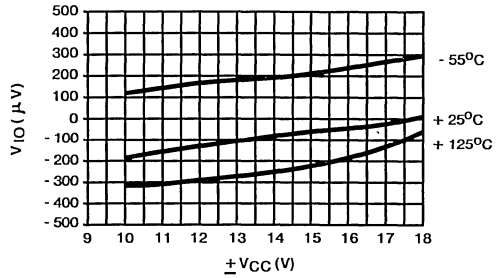


Typical Performance Curves (Continued)  $V_S = \pm 15V, T_A = +25^\circ C$

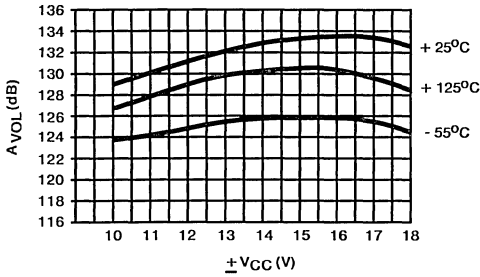
**$V_{OUT}$  vs TEMPERATURE**  
 $V_{CC} = \pm 15V, R_L = 1k\Omega, C_L = \leq 10pF$



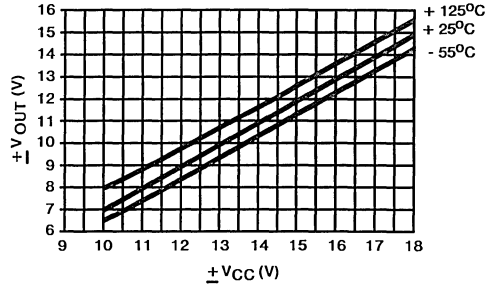
**$V_{IO}$  vs  $\pm V_{CC}$  vs TEMPERATURE**



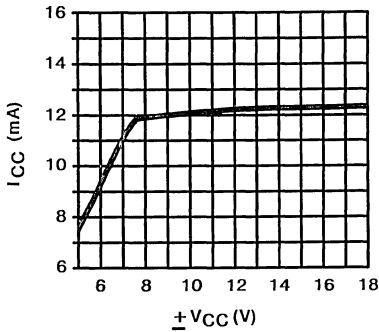
**$A_{VOL}$  vs  $\pm V_{CC}$  vs TEMPERATURE**  
 $V_{OUT} = \pm 5V @ V_{CC} = \pm 10V, V_{OUT} = \pm 10V @ V_{CC} = \pm 15V$   
 $V_{OUT} = \pm 12V @ V_{CC} = 18V$



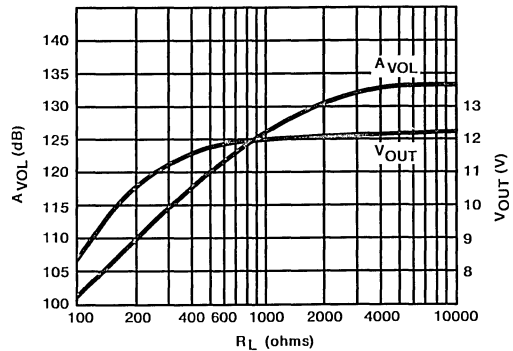
**$\pm V_{OUT}$  vs  $\pm V_{CC}$  vs TEMPERATURE**  
 $R_L = 1K$



**SUPPLY CURRENT vs  $\pm$ SUPPLY VOLTAGE**



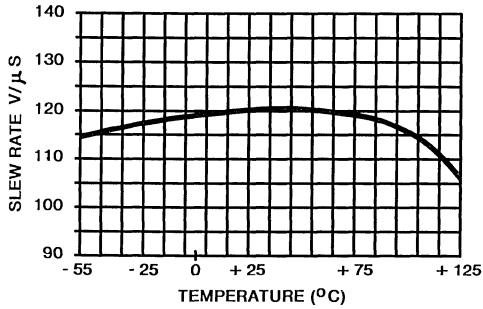
**$A_{VOL}/V_{OUT}$  vs  $R_L$**   
 $V_{IN} = \pm 3V$  For  $100\Omega, V_{IN} = \pm 5V$  For  $200\Omega$   
 $V_{IN} = \pm 10V$  For  $600\Omega$  to  $10k\Omega$



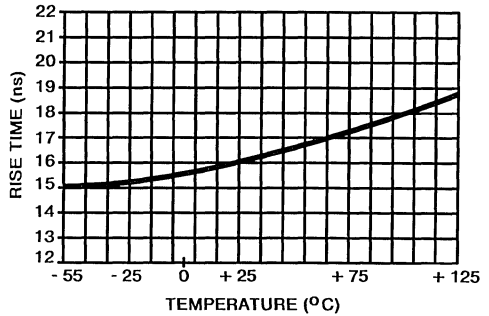


**Typical Performance Curves (Continued)**  $V_S = \pm 15V, T_A = +25^\circ C$

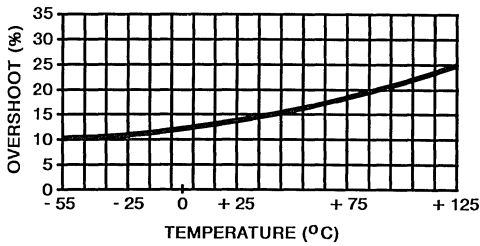
**SLEW RATE vs TEMPERATURE**  
 $V_{CC} = \pm 15V, R_L = 1k\Omega, C_L = \leq 10pF$   
 $A_V = \pm 5, V_{OUT} = \pm 5V(10Vp-p)$



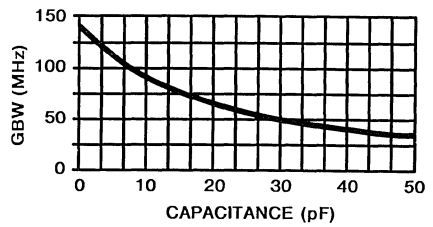
**RISE TIME vs TEMPERATURE**  
 $V_{CC} = \pm 15V, R_L = 1k\Omega, C_L = \leq 10pF$   
 $A_V = +5, V_{OUT} = \pm 100mV(200mVp-p)$



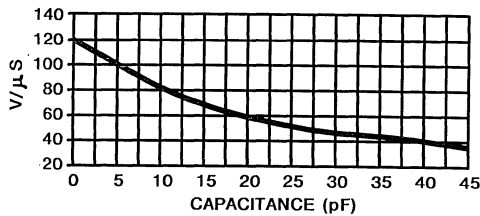
**% OVERSHOOT vs TEMPERATURE**  
 $A_V = +5, V_{OUT} = \pm 100mV(200mVp-p)$   
 $R_L = 1k\Omega, C_L \leq 10pF$



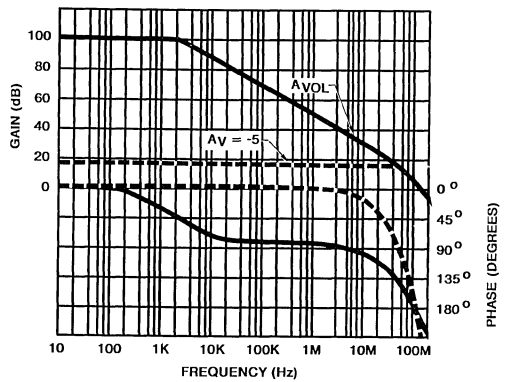
**GAIN BANDWIDTH PRODUCT vs COMPENSATION CAPACITANCE**



**SLEW RATE vs COMPENSATION CAPACITANCE**



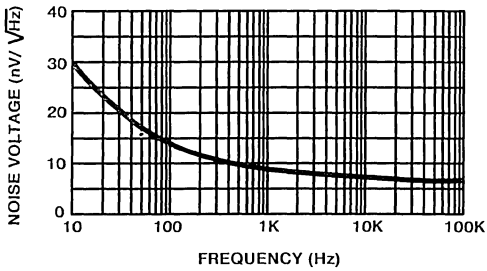
**GAIN AND PHASE vs FREQUENCY**  
 $R_L = 1k\Omega, C_L \leq 10pF$



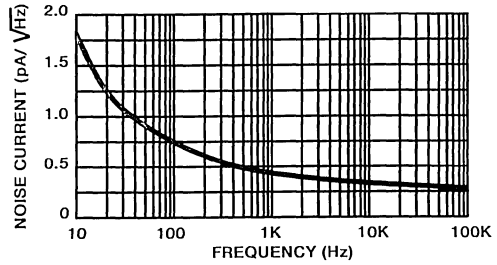
# HA-2548

## Typical Performance Curves (Continued) $V_S = \pm 15V, T_A = +25^\circ C$

INPUT NOISE VOLTAGE DENSITY

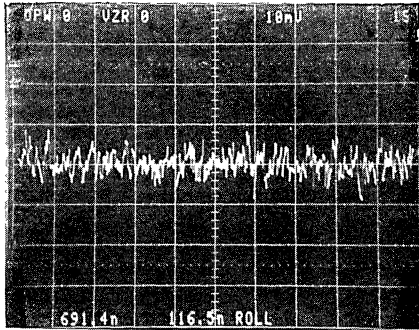


INPUT NOISE CURRENT DENSITY



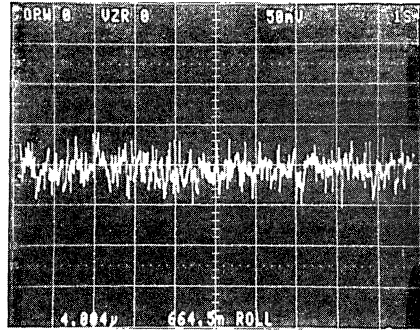
PEAK TO PEAK NOISE 0.1HZ TO 10HZ

p-p(RTI) = 691.4nV, rms(RTI) = 116.5nV,  $A_V = 25000$



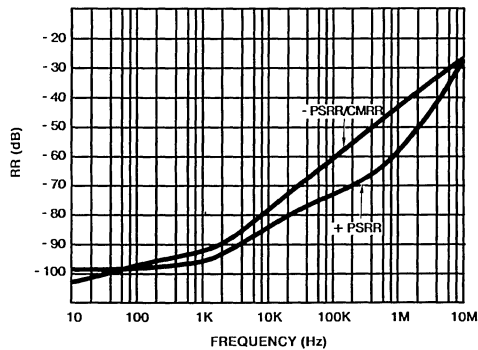
PEAK TO PEAK NOISE 0.1HZ TO 1MHZ

p-p(RTI) = 4.004μV, rms(RTI) = 664.5nV,  $A_V = 25000$



REJECTION RATIOS vs FREQUENCY

$A_V = \pm 10, V_{IN} = 300mV_{rms}$



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OPERATIONAL  
AMPLIFIERS

## Wideband, High Impedance Operational Amplifiers

August 1991

### Features

- Wide Bandwidth ..... 12MHz
- High Input Impedance ..... 500M $\Omega$
- Low Input Bias Current ..... 1nA
- Low Input Offset Current ..... 1nA
- Low Input Offset Voltage ..... 0.5mV
- High Gain ..... 150kV/V
- High Slew Rate ..... 7V/ $\mu$ s
- Output Short Circuit Protection
- Unity Gain Stable

### Description

HA-2600/2602/2605 are internally compensated bipolar operational amplifiers that feature very high input impedance (500M $\Omega$ , HA-2600) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2600) and low bias and offset current (1nA, HA-2600) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 12MHz unity gain-bandwidth, 7V/ $\mu$ s slew rate and 150kV/V open-loop gain enables HA-2600/2602/2605 to perform high-gain amplification of fast, wideband signals. These dynamic characteristics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

### Applications

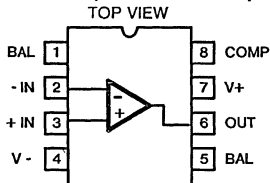
- Video Amplifier
- Pulse Amplifier
- Audio Amplifiers and Filters
- High-Q Active Filters
- High-Speed Comparators
- Low Distortion Oscillators

In addition to its application in pulse and video amplifier designs, HA-2600/2602/2605 are particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators. For more information, please refer to Application Note 515.

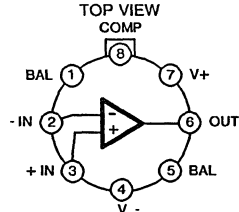
The HA-2600 and HA-2602 have guaranteed operation from -55 $^{\circ}$ C to +125 $^{\circ}$ C and are available in Metal Can and Ceramic Mini-DIP packages. Both are offered as /883 Military Grade; product and data sheets are available upon request. The HA-2605 has guaranteed operation from 0 $^{\circ}$ C to +75 $^{\circ}$ C and is available in Plastic and Ceramic Mini-DIP and Metal Can packages. SOIC packaging is also available for the HA-2605 with guaranteed operation from 0 $^{\circ}$ C to +70 $^{\circ}$ C (-5) and -40 $^{\circ}$ C to +85 $^{\circ}$ C (-9).

### Pinouts

HA9P2605 (SOIC)  
HA7-2600/02/05 (CERAMIC MINI-DIP)  
HA3-2605 (PLASTIC MINI-DIP)

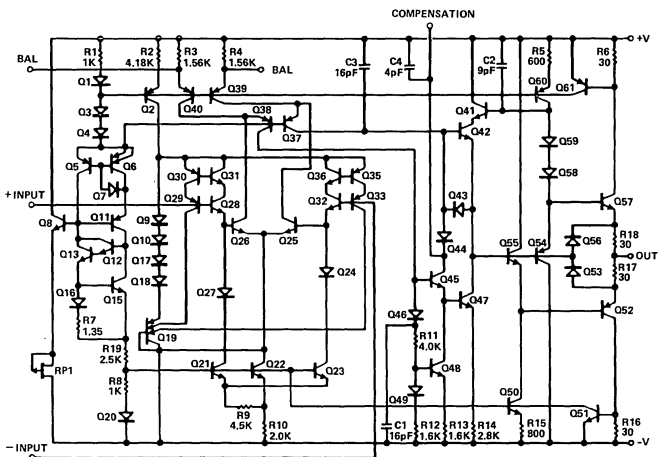


HA2-2600/02/05 (TO-99 METAL CAN)



NOTE: VCASE = V-

### Schematic



## Specifications HA-2600/02/05

### Absolute Maximum Ratings (Note 13)

|   |                               |
|---|-------------------------------|
| Voltage Between V+ and V- Terminals ..... | 45.0V                         |
| Differential Input Voltage .....          | ±12.0V                        |
| Peak Output Current .....                 | Full Short Circuit Protection |
| Internal Power Dissipation .....          | 300mW                         |
| Maximum Junction Temperature .....        | +175°C                        |

### Operating Temperature Ranges

|  |                                 |
|--|---------------------------------|
| HA-2600/HA-2602-2 .....                    | -55°C ≤ T <sub>A</sub> ≤ +125°C |
| HA-2605-5 .....                            | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| HA-2605-9 .....                            | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| Storage Temperature Range .....            | -65°C ≤ T <sub>A</sub> ≤ +150°C |
| Lead Solder Temperature (10 Seconds) ..... | +275°C                          |

### Electrical Specifications V<sub>S</sub> = ±15V D.C., Unless Otherwise Specified.

| PARAMETER  | TEMP  | HA-2600-2 |      |     | HA-2602-2 |      |     | HA-2605-5 |      |     | (NOTE 15)<br>HA-2605-9 | UNITS  |
|--|-------|-----------|------|-----|-----------|------|-----|-----------|------|-----|------------------------|--------|
|  |       | MIN       | TYP  | MAX | MIN       | TYP  | MAX | MIN       | TYP  | MAX | MAX                    |        |
| <b>INPUT CHARACTERISTICS</b>                         |       |           |      |     |           |      |     |           |      |     |                        |        |
| Offset Voltage                                       | +25°C | -         | 0.5  | 4   | -         | 3    | 5   | -         | 3    | 5   | 5                      | mV     |
|  | Full  | -         | 2    | 6   | -         | -    | 7   | -         | -    | 7   | 7                      | mV     |
| Average Offset Voltage Drift                         | Full  | -         | 5    | -   | -         | 5    | -   | -         | 5    | -   | -                      | µV/°C  |
| Bias Current   | +25°C | -         | 1    | 10  | -         | 15   | 25  | -         | 5    | 25  | 25                     | nA     |
|  | Full  | -         | 10   | 30  | -         | -    | 60  | -         | -    | 40  | 70                     | nA     |
| Offset Current                                       | +25°C | -         | 1    | 10  | -         | 5    | 25  | -         | 5    | 25  | 25                     | nA     |
|  | Full  | -         | 5    | 30  | -         | -    | 60  | -         | -    | 40  | 70                     | nA     |
| Differential Input Resistance (Note 10)              | +25°C | 100       | 500  | -   | 40        | 300  | -   | 40        | 300  | -   | -                      | MΩ     |
| Input Noise Voltage Density<br>f <sub>0</sub> = 1kHz | +25°C | -         | 11   | -   | -         | 11   | -   | -         | 11   | -   | -                      | nV/√Hz |
| Input Noise Current Density<br>f <sub>0</sub> = 1kHz | +25°C | -         | 0.16 | -   | -         | 0.16 | -   | -         | 0.16 | -   | -                      | pA/√Hz |
| Common Mode Range                                    | Full  | ±11       | ±12  | -   | ±11       | ±12  | -   | ±11       | ±12  | -   | -                      | V      |
| <b>TRANSFER CHARACTERISTICS</b>                      |       |           |      |     |           |      |     |           |      |     |                        |        |
| Large Signal Voltage Gain<br>(Notes 1, 4)            | +25°C | 100K      | 150K | -   | 80K       | 150K | -   | 80K       | 150K | -   | -                      | V/V    |
|  | Full  | 70K       | -    | -   | 60K       | -    | -   | 70K       | -    | -   | -                      | V/V    |
| Common Mode Rejection Ratio<br>(Note 2)              | Full  | 80        | 100  | -   | 74        | 100  | -   | 74        | 100  | -   | -                      | dB     |
| Minimum Stable Gain                                  | +25°C | 1         | -    | -   | 1         | -    | -   | 1         | -    | -   | -                      | V/V    |
| Gain Bandwidth Product (Note 3)                      | +25°C | -         | 12   | -   | -         | 12   | -   | -         | 12   | -   | -                      | MHz    |
| <b>OUTPUT CHARACTERISTICS</b>                        |       |           |      |     |           |      |     |           |      |     |                        |        |
| Output Voltage Swing (Note 1)                        | Full  | ±10       | ±12  | -   | ±10       | ±12  | -   | ±10       | ±12  | -   | -                      | V      |
| Output Current (Note 4)                              | +25°C | ±15       | ±22  | -   | ±10       | ±18  | -   | ±10       | ±18  | -   | -                      | mA     |
| Full Power Bandwidth (Notes 4, 11)                   | +25°C | 50        | 75   | -   | 50        | 75   | -   | 50        | 75   | -   | -                      | kHz    |
| <b>TRANSIENT RESPONSE (Note 8)</b>                   |       |           |      |     |           |      |     |           |      |     |                        |        |
| Rise Time (Notes 1, 5, 6 & 7)                        | +25°C | -         | 30   | 60  | -         | 30   | 60  | -         | 30   | 60  | 60                     | ns     |
| Overshoot (Notes 1, 5, 6 & 7)                        | +25°C | -         | 25   | 40  | -         | 25   | 40  | -         | 25   | 40  | 40                     | %      |
| Slew Rate (Notes 1, 5, 7 & 12)                       | +25°C | ±4        | ±7   | -   | ±4        | ±7   | -   | ±4        | ±7   | -   | -                      | V/µs   |
| Settling Time (Notes 1, 5 & 14)                      | +25°C | -         | 1.5  | -   | -         | 1.5  | -   | -         | 1.5  | -   | -                      | µs     |
| <b>POWER SUPPLY CHARACTERISTICS</b>                  |       |           |      |     |           |      |     |           |      |     |                        |        |
| Supply Current                                       | +25°C | -         | 3    | 3.7 | -         | 3    | 4   | -         | 3    | 4   | 4                      | mA     |
| Power Supply Rejection Ratio (Note 9)                | Full  | 80        | 90   | -   | 74        | 90   | -   | 74        | 90   | -   | -                      | dB     |

#### NOTES:

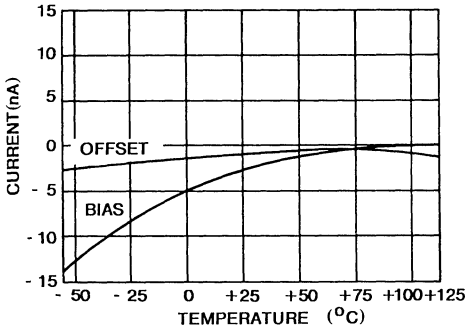
1. R<sub>L</sub> = 2kΩ
2. V<sub>CM</sub> = ±10V
3. V<sub>OUT</sub> < 90mV
4. V<sub>OUT</sub> = ±10V
5. C<sub>L</sub> = 100pF
6. V<sub>OUT</sub> = ±200mV
7. A<sub>V</sub> = +1
8. See Transient Response Test Circuits & Waveforms.
9. ΔV<sub>S</sub> = ±5V
10. This parameter value guaranteed by design calculations.
11. Full Power Bandwidth guaranteed by slew rate measurement:  
FPBW = S.R./2πV<sub>PEAK</sub>.
12. V<sub>OUT</sub> = ±5V
13. Absolute Maximum Ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
14. Settling time is characterized at A<sub>V</sub> = -1 to 0.1% of a 10 Volt step.
15. Typical and minimum specifications for -9 are identical to those of -5.

3

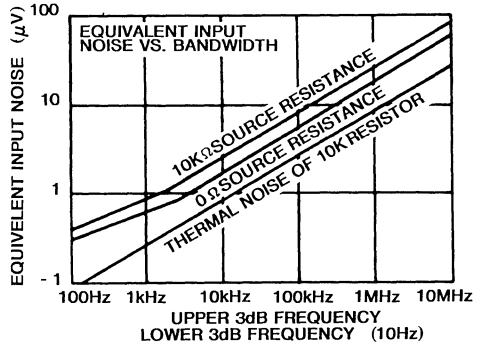
OPERATIONAL  
AMPLIFIERS

**Typical Performance Curves**  $V_S = \pm 15V$  D.C.,  $T_A = +25^\circ C$ , Unless Otherwise Specified.

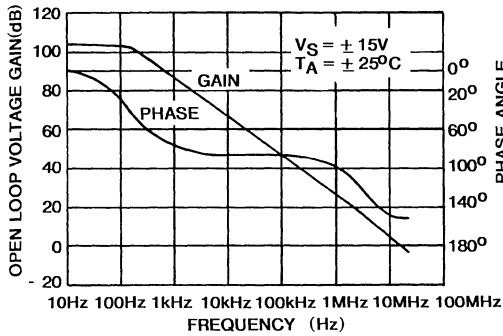
**INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE**



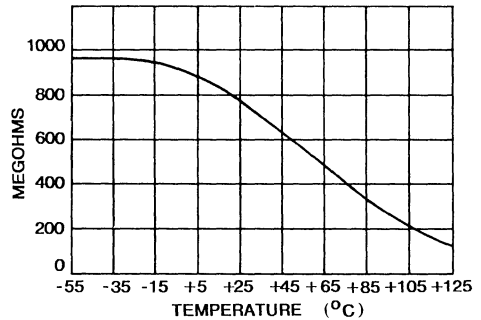
**BROADBAND NOISE CHARACTERISTICS**



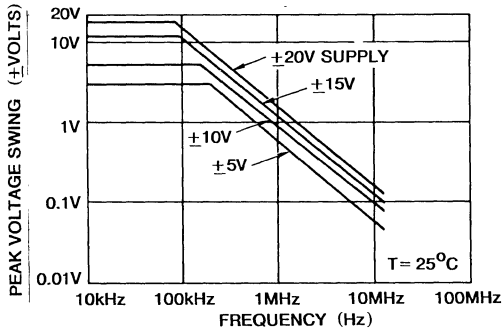
**OPEN LOOP FREQUENCY AND PHASE RESPONSE**



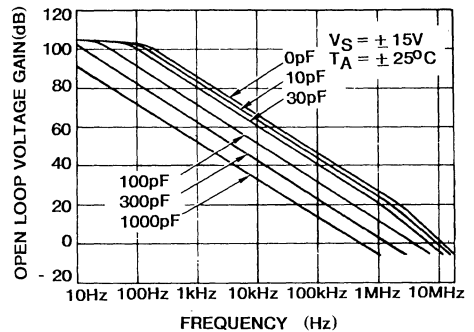
**INPUT IMPEDANCE vs. TEMPERATURE, 100Hz**



**OUTPUT VOLTAGE SWING vs. FREQUENCY**



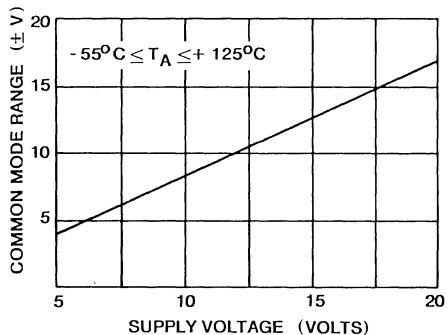
**OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND**



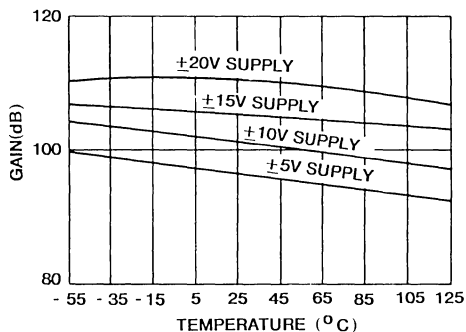
NOTE: External Compensation Components are not required for stability, but may be added to reduce bandwidth if desired. If External Compensation is used, also connect 100pF capacitor from output to ground.

**Typical Performance Curves (Continued)**

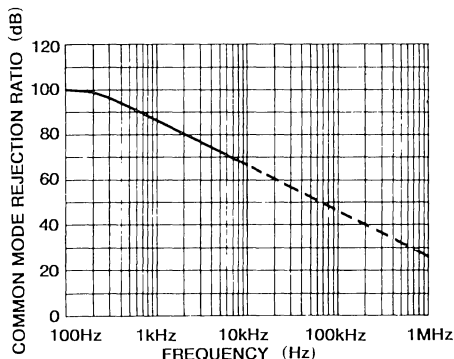
**COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE**



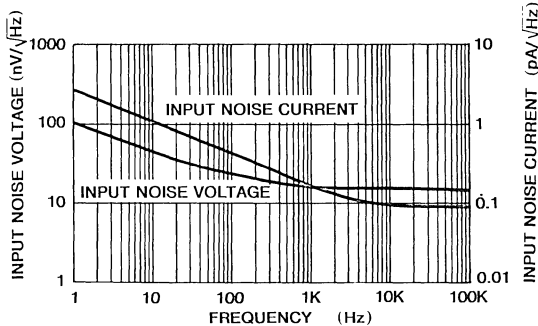
**OPEN - LOOP VOLTAGE GAIN vs. TEMPERATURE**



**COMMON MODE REJECTION RATIO vs. FREQUENCY**

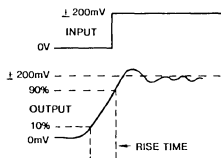


**NOISE DENSITY vs. FREQUENCY**

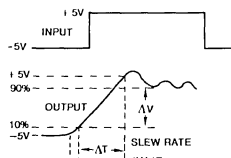


**Test Circuits**

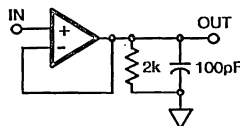
**TRANSIENT RESPONSE**



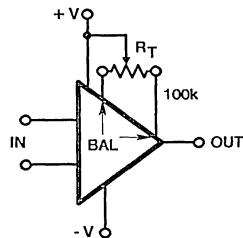
**SLEW RATE**



**SLEW RATE AND TRANSIENT RESPONSE**



**SUGGESTED V<sub>OS</sub> ADJUSTMENT AND COMPENSATION HOOK-UP**

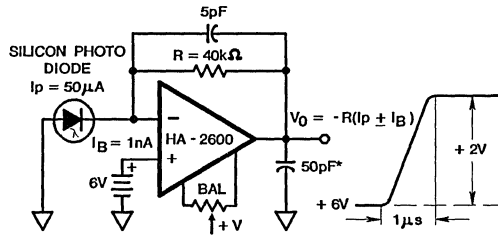


NOTE: Measured on both positive and negative transitions from 0 to +200mV and 0 to -200mV at output.

Tested Offset Adjustment is  $|V_{OS} + 1mV|$  minimum referred to output. Typical range is  $\pm 10mV$  with  $R_T = 100k\Omega$ .

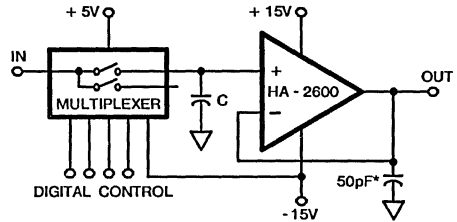
**Typical Applications**

**PHOTO-CURRENT TO VOLTAGE CONVERTER**



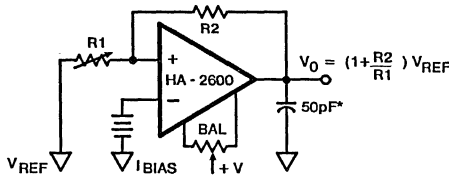
- FEATURES:**
1. Constant cell voltage
  2. Minimum bias current error

**SAMPLE-AND-HOLD**



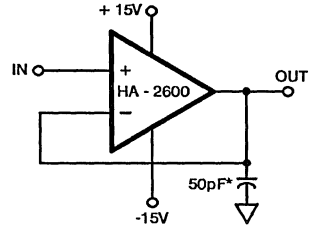
Drift rate  $\frac{I_{bias}}{C}$       If C = 1000pF  
 Drift = 0.01V/ms Max.

**REFERENCE VOLTAGE AMPLIFIER**



- FEATURES:**
1. Minimum bias current in reference cell
  2. Short circuit protection

**VOLTAGE FOLLOWER**



$Z_{IN} = 10^{12}$  Min.      B.W. = 12MHz Typ.  
 $Z_{OUT} = 0.01$  Max.      Slew Rate = 4V/μs Min.      Output Swing = ±10V Min. to 50kHz

\* A small load capacitance is recommended in all applications where practical to prevent possible high frequency oscillations resulting from external wiring parasitics. Capacitance up to 100pF has negligible effect on the bandwidth or slew rate.

**Die Characteristics**

|                              |                   |               |
|------------------------------|-------------------|---------------|
| Transistor Count .....       | 140               |               |
| Die Dimensions .....         | 73 x 52 x 19 mils |               |
| Substrate Potential .....    | Unbiased          |               |
| Thermal Constants (°C/W)     | $\theta_{ja}$     | $\theta_{jc}$ |
| HA2-Metal Can (-2, -5, -7)   | 202               | 55            |
| HA2-Metal Can (-8, /883)     | 161               | 48            |
| HA3-Plastic DIP (-5)         | 83                | 33            |
| HA4-Ceramic LCC (/883)       | 96                | 35            |
| HA7-Ceramic DIP (-2, -5, -7) | 204               | 112           |
| HA7-Ceramic DIP (-8, /883)   | 100               | 27            |
| HA9P-SOIC(-5, -9)            | 160               | 42            |

August 1991

### Features

- Gain Bandwidth Product ( $A_V \geq 5$ ) ..... 100MHz
- High Input Impedance ..... 500M $\Omega$
- Low Input Bias Current ..... 1nA
- Low Input Offset Current ..... 1nA
- Low Input Offset Voltage ..... 0.5mV
- High Gain ..... 150kV/V
- High Slew Rate ..... 35V/ $\mu$ s
- Output Short Circuit Protection

### Description

HA-2620/2622/2625 are bipolar operational amplifiers that feature very high input impedance (500M $\Omega$ , HA-2620) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2620) and low bias and offset current (1nA, HA-2620) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 100MHz gain-bandwidth product (HA-2620/2622/2625 are stable for closed loop gains greater than 5), 35V/ $\mu$ s slew rate and 150kV/V open-loop gain enables HA-2620/2622/2625 to perform high-gain amplification of very fast, wideband signals. These dynamic characteristics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact

### Applications

- Video and R.F. Amplifier
- Pulse Amplifier
- Audio Amplifiers and Filters
- High-Q Active Filters
- High-Speed Comparators
- Low Distortion Oscillators

design requirements by means of an external bandwidth control capacitor.

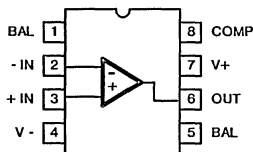
In addition to its application in pulse and video amplifier designs, HA-2620/2622/2625 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators. For more information, please refer to Application Notes 509, 519 and 546.

The HA-2620 and HA-2622 have guaranteed operation from -55 $^{\circ}$ C to +125 $^{\circ}$ C and are available in Metal Can and Ceramic Mini-DIP packages. Both are offered as /883 Military Grade with the HA-2622 also available in LCC packages. MIL-STD-883 data sheets are available upon request. The HA-2625 has guaranteed operation from 0 $^{\circ}$ C to +75 $^{\circ}$ C and is available in Plastic and Ceramic Mini-DIP and Metal Can packages. Additionally the HA-2625 is available in SOIC packaging with -5 and -9 temperature grades.

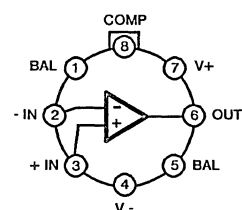
### Pinouts

HA9P2625 (SOIC)  
HA7-2620/22/25 (CERAMIC MINI-DIP)  
HA3-2625 (PLASTIC MINI-DIP)

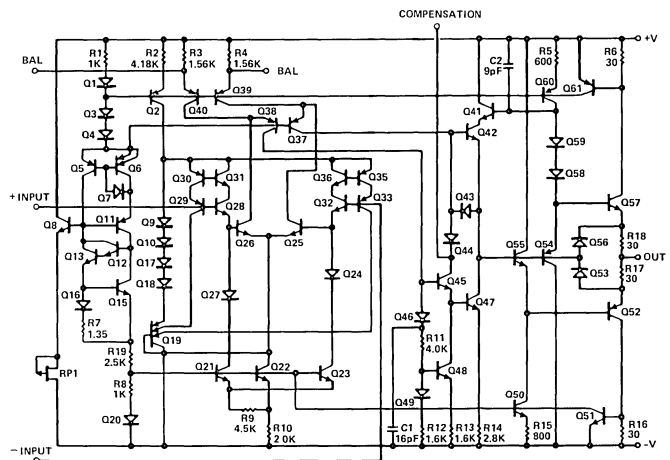
TOP VIEW



HA2-2620/22/25 (TO-99 METAL CAN)  
TOP VIEW



### Schematic





## Specifications HA-2620/22/25

### Absolute Maximum Ratings (Note 13)

|   |                               |
|---|-------------------------------|
| Voltage Between V+ and V- Terminals ..... | 45.0V                         |
| Differential Input Voltage .....          | ±12.0V                        |
| Peak Output Current .....                 | Full Short Circuit Protection |
| Internal Power Dissipation .....          | 300mW                         |
| Maximum Junction Temperature .....        | +175°C                        |

### Operating Temperature Ranges

|  |                                 |
|--|---------------------------------|
| HA-2620/HA-2622-2 .....                    | -55°C ≤ T <sub>A</sub> ≤ +125°C |
| HA-2625-5 .....                            | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| HA-2625-9 .....                            | -40°C ≤ T <sub>A</sub> ≤ +80°C  |
| Storage Temperature Range: .....           | -65°C ≤ T <sub>A</sub> ≤ +150°C |
| Lead Solder Temperature (10 Seconds) ..... | 275°C                           |

Electrical Specifications V<sub>S</sub> = ±15V D.C., Unless Otherwise Specified.

| PARAMETER   | TEMP  | HA-2620-2 |      |     | HA-2622-2 |      |     | HA-2625-5, -9 |      |     | UNITS  |
|---|-------|-----------|------|-----|-----------|------|-----|---------------|------|-----|--------|
|   |       | MIN       | TYP  | MAX | MIN       | TYP  | MAX | MIN           | TYP  | MAX |        |
| <b>INPUT CHARACTERISTICS</b>                      |       |           |      |     |           |      |     |               |      |     |        |
| Offset Voltage (Note 1)                           | +25°C | -         | 0.5  | 4   | -         | 3    | 5   | -             | 3    | 5   | mV     |
|   | Full  | -         | 2    | 6   | -         | -    | 7   | -             | -    | 7   | mV     |
| Average Offset Voltage Drift                      | Full  | -         | 5    | -   | -         | 5    | -   | -             | 5    | -   | µV/°C  |
| Bias Current                                      | +25°C | -         | 1    | 15  | -         | 5    | 25  | -             | 5    | 25  | nA     |
|   | Full  | -         | 10   | 35  | -         | -    | 60  | -             | -    | 40  | nA     |
| Offset Current                                    | +25°C | -         | 1    | 15  | -         | 5    | 25  | -             | 5    | 25  | nA     |
|   | Full  | -         | 5    | 35  | -         | -    | 60  | -             | -    | 40  | nA     |
| Differential Input Resistance (Note 11)           | +25°C | 65        | 500  | -   | 40        | 300  | -   | 40            | 300  | -   | MΩ     |
| Input Noise Voltage Density f <sub>O</sub> = 1kHz | +25°C | -         | 11   | -   | -         | 11   | -   | -             | 11   | -   | nV/√Hz |
| Input Noise Current Density f <sub>O</sub> = 1kHz | +25°C | -         | 0.16 | -   | -         | 0.16 | -   | -             | 0.16 | -   | pA/√Hz |
| Common Mode Range                                 | Full  | ±11       | ±12  | -   | ±11       | ±12  | -   | ±11           | ±12  | -   | V      |
| <b>TRANSFER CHARACTERISTICS</b>                   |       |           |      |     |           |      |     |               |      |     |        |
| Large Signal Voltage Gain (Notes 2 & 3)           | +25°C | 100K      | 150K | -   | 80K       | 150K | -   | 80K           | 150K | -   | V/V    |
|   | Full  | 70K       | -    | -   | 60K       | -    | -   | 70K           | -    | -   | V/V    |
| Common Mode Rejection Ratio (Note 4)              | Full  | 80        | 100  | -   | 74        | 100  | -   | 74            | 100  | -   | dB     |
| Minimum Stable Gain                               | +25°C | 5         | -    | -   | 5         | -    | -   | 5             | -    | -   | V/V    |
| Gain Bandwidth Product (Notes 2, 5 & 6)           | +25°C | -         | 100  | -   | -         | 100  | -   | -             | 100  | -   | MHz    |
| <b>OUTPUT CHARACTERISTICS</b>                     |       |           |      |     |           |      |     |               |      |     |        |
| Output Voltage Swing (Note 2)                     | Full  | ±10       | ±12  | -   | ±10       | ±12  | -   | ±10           | ±12  | -   | V      |
| Output Current (Note 3)                           | +25°C | ±15       | ±22  | -   | ±10       | ±18  | -   | ±10           | ±18  | -   | mA     |
| Full Power Bandwidth (Notes 2, 3, 7 & 12)         | +25°C | 400       | 600  | -   | 320       | 600  | -   | 320           | 600  | -   | kHz    |
| <b>TRANSIENT RESPONSE (Note 8)</b>                |       |           |      |     |           |      |     |               |      |     |        |
| Rise Time (Notes 2, 7 & 8)                        | +25°C | -         | 17   | 45  | -         | 17   | 45  | -             | 17   | 45  | ns     |
| Slew Rate (Notes 2, 7, 8 & 10)                    | +25°C | ±25       | ±35  | -   | ±20       | ±35  | -   | ±20           | ±35  | -   | V/µs   |
| <b>POWER SUPPLY CHARACTERISTICS</b>               |       |           |      |     |           |      |     |               |      |     |        |
| Supply Current                                    | +25°C | -         | 3    | 3.7 | -         | 3    | 4   | -             | 3    | 4   | mA     |
| Power Supply Rejection Ratio (Note 9)             | Full  | 80        | 90   | -   | 74        | 90   | -   | 74            | 90   | -   | dB     |

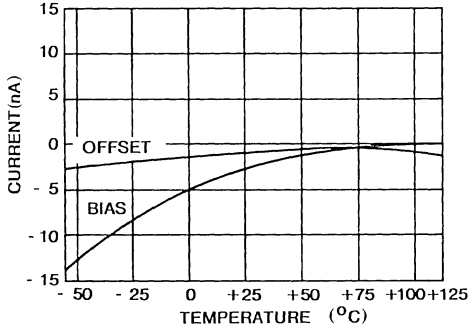
**NOTES:**

1. Offset may be externally adjusted to zero.
2. R<sub>L</sub> = 2kΩ
3. V<sub>OUT</sub> = ±10.0V
4. V<sub>CM</sub> = ±10V
5. V<sub>OUT</sub> < 90mV
6. 40dB Gain
7. See Transient Response Test Circuits & Waveforms.
8. A<sub>y</sub> = 5 (The HA-2620 family is not stable at unity gain without external compensation.)

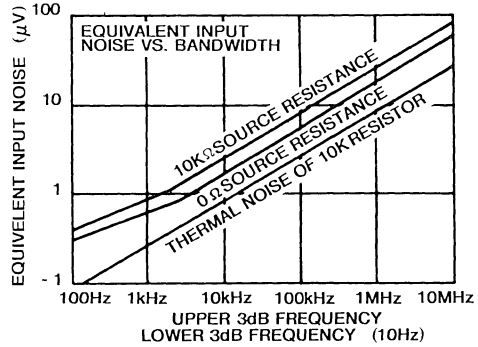
9. ΔV<sub>S</sub> = ±5V
10. V<sub>OUT</sub> = ±5V
11. This parameter value guaranteed by design calculations.
12. Full Power Bandwidth guaranteed by slew rate measurement:  
FPBW = S.R./2nV<sub>PEAK</sub>.
13. Absolute Maximum Ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

**Typical Performance Curves**  $V_S = \pm 15V$  D.C.,  $T_A = +25^\circ C$ , Unless Otherwise Specified.

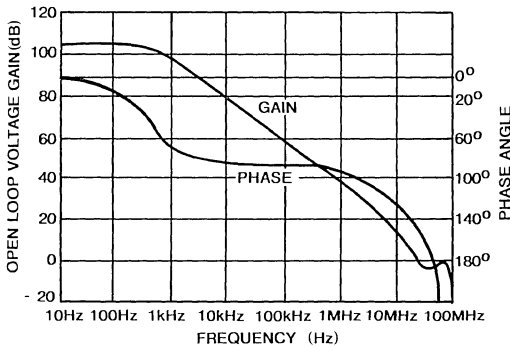
**INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE**



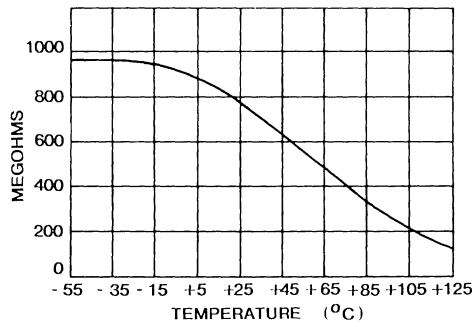
**BROADBAND NOISE CHARACTERISTICS**



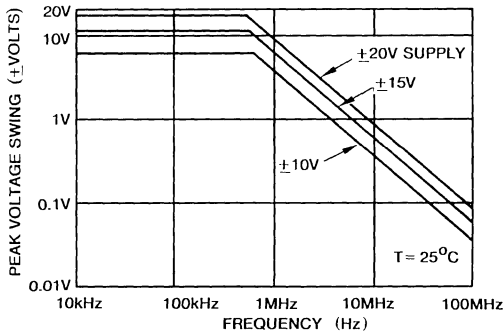
**OPEN LOOP FREQUENCY AND PHASE RESPONSE**



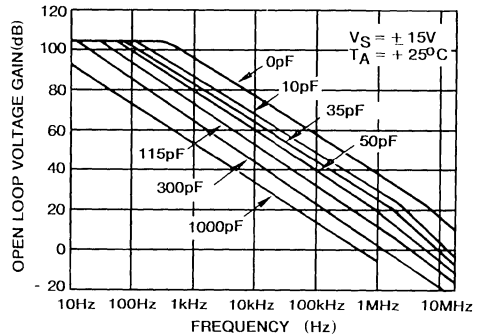
**INPUT IMPEDANCE vs. TEMPERATURE, 100Hz**



**OUTPUT VOLTAGE SWING vs. FREQUENCY**



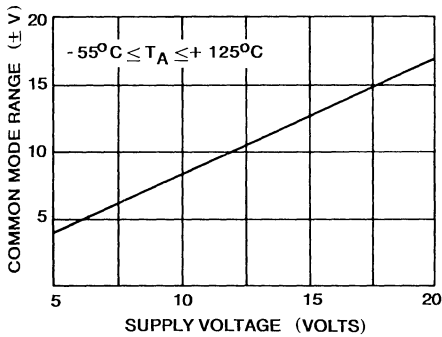
**OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND**



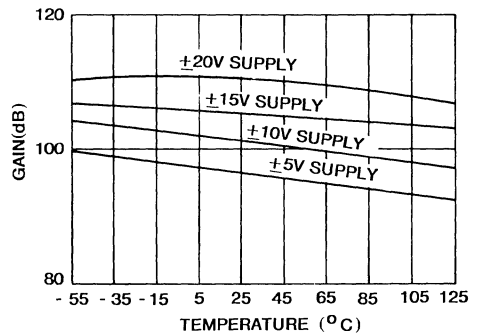
NOTE: External Compensation is required for closed loop gain < 5. If external compensation is used, also connect 100pF capacitor from output to ground.

**Typical Performance Curves (Continued)**

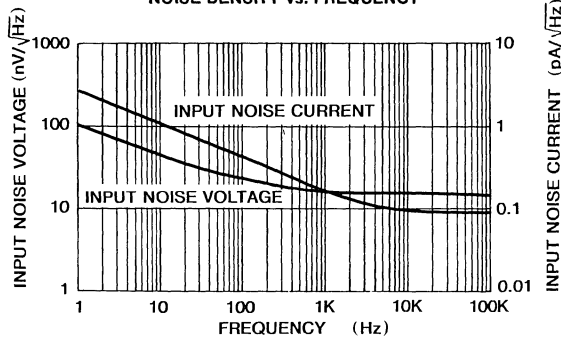
**COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE**



**OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE**

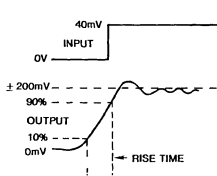


**NOISE DENSITY vs. FREQUENCY**

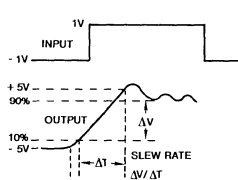


**Test Circuits**

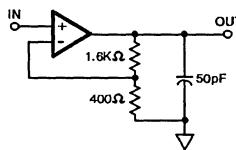
**TRANSIENT RESPONSE**



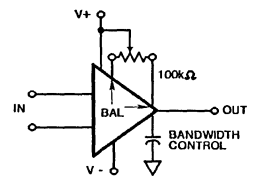
**SLEW RATE**



**SLEW RATE AND TRANSIENT RESPONSE**



**SUGGESTED V<sub>OS</sub> ADJUSTMENT AND COMPENSATION HOOK-UP**

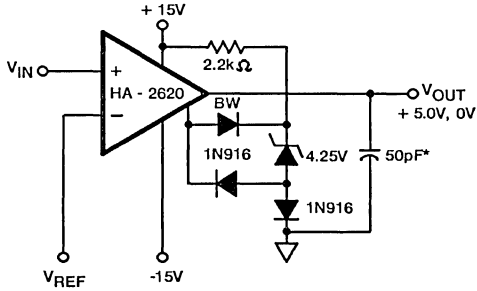


NOTE: Measured on both positive and negative transients from 0 to +200mV and 0 to -200mV at output.

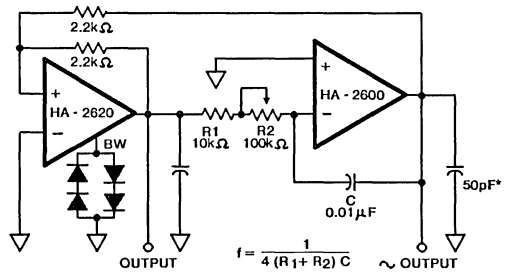
Tested Offset Adjustment is |V<sub>OS</sub> + 1mV| minimum referred to output. Typical range is ±10mV with R<sub>T</sub> = 100kΩ.

**Typical Applications**

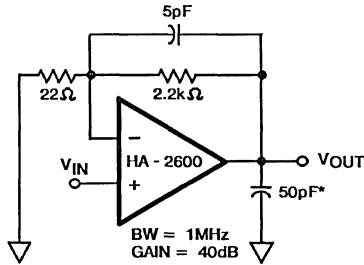
**HIGH IMPEDANCE COMPARATOR**



**FUNCTION GENERATOR**



**VIDEO AMPLIFIER**



\* A small load capacitance of at least 30pF (including stray capacitance) is recommended to prevent possible high frequency oscillations.

**Die Characteristics**

Transistor Count ..... 140  
 Die Dimensions ..... 73 x 52 x 19 mils  
 Substrate Potential ..... Unbiased

| Thermal Constants (°C/W)     | $\theta_{ja}$ | $\theta_{jc}$ |
|------------------------------|---------------|---------------|
| HA2-Metal Can (-2, -5, -7)   | 202           | 55            |
| HA2-Metal Can (-8, /883)     | 161           | 48            |
| HA3-Plastic DIP (-5)         | 83            | 33            |
| HA4-Ceramic LCC (/883)       | 96            | 35            |
| HA7-Ceramic DIP (-2, -5, -7) | 204           | 112           |
| HA7-Ceramic DIP (-8, /883)   | 81            | 32            |

August 1991

### Features

- Output Voltage Swing .....  $\pm 35V$
- Supply Voltage .....  $\pm 10V$  to  $\pm 40V$
- Offset Current ..... 5nA
- Bandwidth ..... 4MHz
- Slew Rate .....  $5V/\mu s$
- Common Mode Input Voltage Swing .....  $\pm 35V$
- Output Overload Protection

### Description

HA-2640 and HA-2645 are monolithic operational amplifiers which are designed to deliver unprecedented dynamic specifications for a high voltage internally compensated device. These dielectrically isolated devices offer very low values for offset voltage and offset current coupled with large output voltage swing and common mode input voltage.

For maximum reliability, these amplifiers offer unconditional output overload protection through current limiting and a chip temperature sensing circuit. This sensing device turns the amplifier "off", when the chip reaches a certain temperature level.

These amplifiers deliver  $\pm 35V$  common mode input voltage swing,  $\pm 35V$  output voltage swing, and up to  $\pm 40V$

### Applications

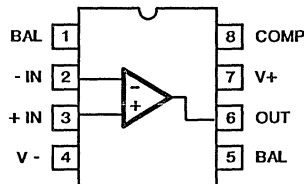
- Industrial Control Systems
- Power Supplies
- High Voltage Regulators
- Resolver Excitation
- Signal Conditioning

supply range for use in such designs as regulators, power supplies, and industrial control systems. 4MHz gain bandwidth and  $5V/\mu s$  slew rate make these devices excellent components for high performance signal conditioning applications. Outstanding input and output voltage swings coupled with a low 5nA offset current make these amplifiers excellent components for resolver excitation designs.

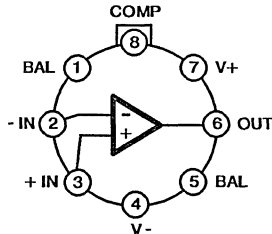
The HA-2640/2645 are available in Metal Can (TO-99) or Ceramic Mini-DIP and can be used as high performance pin-for-pin replacements for many general performance amplifiers. HA-2640 is specified from  $-55^{\circ}C$  to  $+125^{\circ}C$  and HA-2645 is specified over the  $0^{\circ}C$  to  $+75^{\circ}C$  range.

### Pinouts

HA7-2640/2645 (CERAMIC MINI-DIP)  
TOP VIEW

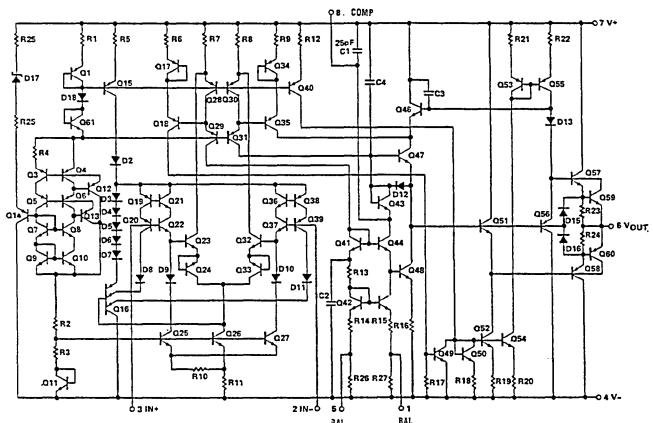


HA2-2640/2645 (TO-99 METAL CAN)  
TOP VIEW



(TO-99 Case Voltage = -V)

### Schematic



## Specifications HA-2640/2645

### Absolute Maximum Ratings (Note 12)

|   |                               |
|---|-------------------------------|
| Voltage Between V+ and V- Terminals ..... | 100V                          |
| Input Voltage Range .....                 | $\pm 10V$ to $\pm 37V$        |
| Output Current .....                      | Full Short Circuit Protection |
| Internal Power Dissipation .....          | 680mW *                       |
| Maximum Junction Temperature .....        | $+175^{\circ}C$               |

\* Derate by 4.6mW/°C above  $+25^{\circ}C$

### Operating Temperature Ranges

|                                 |  |
|---------------------------------|--|
| HA-2640-2 .....                 | $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ |
| HA-2645-5 .....                 | $0^{\circ}C \leq T_A \leq +75^{\circ}C$    |
| Storage Temperature Range ..... | $-65^{\circ}C \leq T_A \leq +150^{\circ}C$ |

**Electrical Specifications**  $V_{SUPPLY} = \pm 40V$ ,  $R_L = 5k\Omega$ , Unless Otherwise Specified.

| PARAMETER                             | TEMP  | HA-2640-2<br>-55°C to +125°C |          |          | HA-2645-5<br>0°C to +75°C |          |          | UNITS             |
|---------------------------------------|-------|------------------------------|----------|----------|---------------------------|----------|----------|-------------------|
|                                       |       | MIN                          | TYP      | MAX      | MIN                       | TYP      | MAX      |                   |
| <b>INPUT CHARACTERISTICS</b>          |       |                              |          |          |                           |          |          |                   |
| Offset Voltage                        | +25°C | -                            | 2        | 4        | -                         | 2        | 6        | mV                |
|                                       | Full  | -                            | -        | 6        | -                         | -        | 7        | mV                |
| Average Offset Voltage Drift          | Full  | -                            | 15       | -        | -                         | 15       | -        | $\mu V/^{\circ}C$ |
| Bias Current                          | +25°C | -                            | 10       | 25       | -                         | 12       | 30       | nA                |
|                                       | Full  | -                            | -        | 50       | -                         | -        | 50       | nA                |
| Offset Current                        | +25°C | -                            | 5        | 12       | -                         | 15       | 30       | nA                |
|                                       | Full  | -                            | -        | 35       | -                         | -        | 50       | nA                |
| Input Resistance (Note 10)            | +25°C | 50                           | 250      | -        | 40                        | 200      | -        | MΩ                |
| Common Mode Range                     | Full  | $\pm 35$                     | -        | -        | $\pm 35$                  | -        | -        | V                 |
| <b>TRANSFER CHARACTERISTICS</b>       |       |                              |          |          |                           |          |          |                   |
| Large Signal Voltage Gain (Notes 8)   | +25°C | 100K                         | 200K     | -        | 100K                      | 200K     | -        | V/V               |
|                                       | Full  | 75K                          | -        | -        | 75K                       | -        | -        | V/V               |
| Common Mode Rejection Ratio (Note 1)  | Full  | 80                           | 100      | -        | 74                        | 100      | -        | dB                |
| Minimum Stable Gain                   | +25°C | 1                            | -        | -        | 1                         | -        | -        | V/V               |
| Unity Gain Bandwidth (Note 2)         | +25°C | -                            | 4        | -        | -                         | 4        | -        | MHz               |
| <b>OUTPUT CHARACTERISTICS</b>         |       |                              |          |          |                           |          |          |                   |
| Output Voltage Swing                  | Full  | $\pm 35$                     | -        | -        | $\pm 35$                  | -        | -        | V                 |
| Output Current (Note 9)               | +25°C | $\pm 12$                     | $\pm 15$ | -        | $\pm 10$                  | $\pm 12$ | -        | mA                |
| Output Resistance                     | +25°C | -                            | 500      | -        | -                         | 500      | -        | Ω                 |
| Full Power Bandwidth (Notes 3 & 11)   | +25°C | -                            | 23       | -        | -                         | 23       | -        | kHz               |
| <b>TRANSIENT RESPONSE (Note 7)</b>    |       |                              |          |          |                           |          |          |                   |
| Rise Time (Notes 4 & 6)               | +25°C | -                            | 60       | 100      | -                         | 60       | 100      | ns                |
| Overshoot (Notes 4 & 6)               | +25°C | -                            | 15       | 30       | -                         | 15       | 40       | %                 |
| Slew Rate (Note 6)                    | +25°C | $\pm 3$                      | $\pm 5$  | -        | $\pm 2.5$                 | $\pm 5$  | -        | V/μs              |
| <b>POWER SUPPLY CHARACTERISTICS</b>   |       |                              |          |          |                           |          |          |                   |
| Supply Current                        | +25°C | -                            | 3.2      | 3.8      | -                         | 3.2      | 4.5      | mA                |
| Supply Voltage Range                  | Full  | $\pm 10$                     | -        | $\pm 40$ | $\pm 10$                  | -        | $\pm 40$ | V                 |
| Power Supply Rejection Ratio (Note 5) | Full  | 80                           | 90       | -        | 74                        | 90       | -        | dB                |

**NOTES:**

1.  $V_{CM} = \pm 20V$
2.  $V_{OUT} = 90mV$
3.  $V_{OUT} = \pm 35V$
4.  $V_{OUT} = \pm 200mV$
5.  $V_S = \pm 10V$  to  $\pm 40V$
6.  $A_V = +1$
7.  $C_L = 50pF$ ,  $R_L = 5k\Omega$
8.  $V_{OUT} = \pm 30V$
9.  $R_L = 1k\Omega$
10. This parameter based upon design calculations.
11. Full Power Bandwidth guaranteed based upon slew rate measurement:  
 $FPBW = S.R./2nV_{PEAK}$ ;  $V_{PEAK} = 35V$ .
12. Absolute Maximum Ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

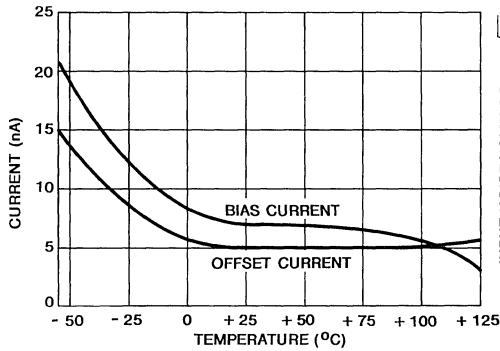
3

OPERATIONAL  
AMPLIFIERS

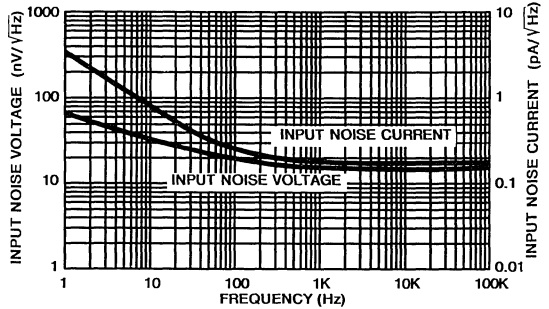
# HA-2640/2645

**Typical Performance Curves**  $V_+ = V_- = 40V$  D.C.,  $T_A = +25^\circ C$ , Unless Otherwise Specified.

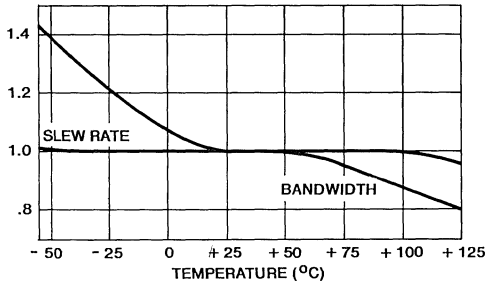
**INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE**



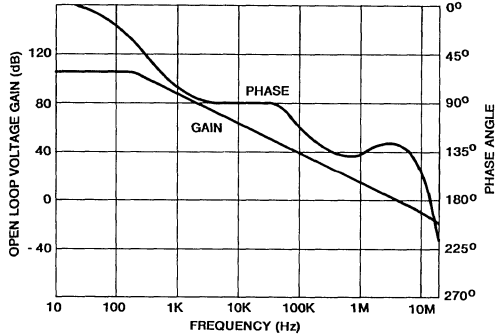
**INPUT NOISE CHARACTERISTICS**



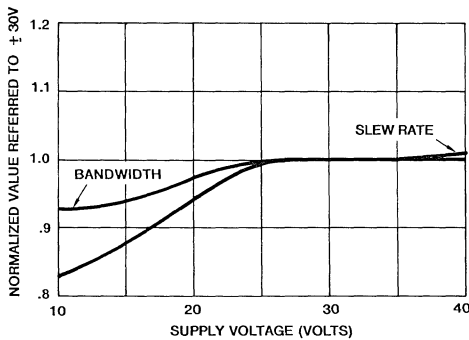
**NORMALIZED AC PARAMETERS vs. TEMPERATURE**



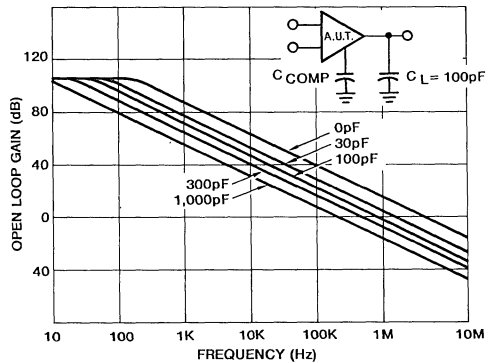
**OPEN LOOP FREQUENCY AND PHASE RESPONSE**



**NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE AT +25°C**



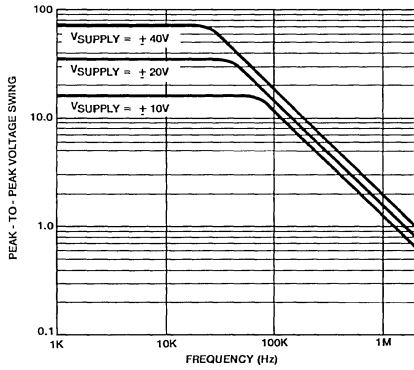
**OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND**



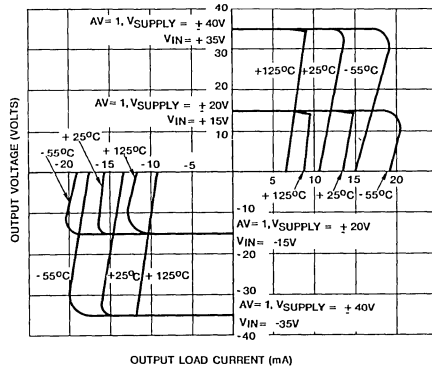
NOTE: External Compensation Components are not required for stability, but may be added to reduce bandwidth if desired. If External Compensation is used, also connect 100pF capacitor from output to ground.

Typical Performance Curves (Continued)

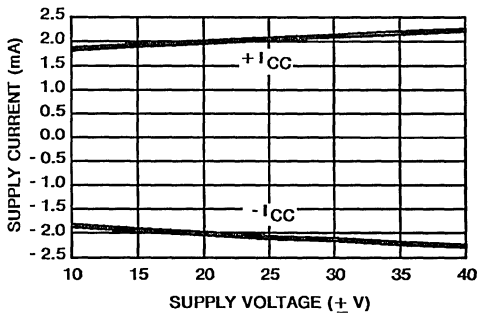
OUTPUT VOLTAGE SWING vs. FREQUENCY AT +25°C



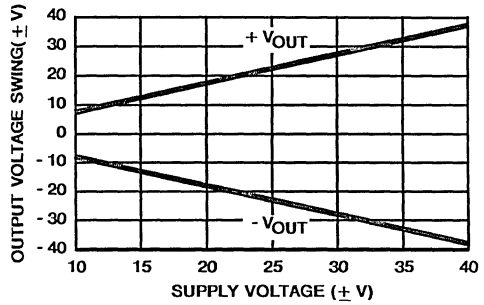
OUTPUT CURRENT CHARACTERISTIC



SUPPLY CURRENT vs. SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE

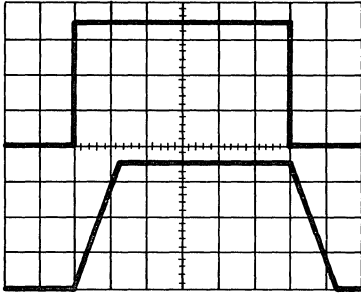




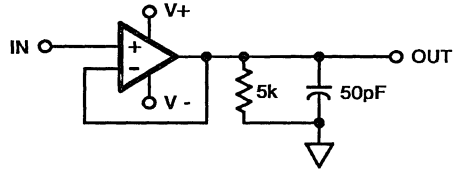
**Switching Waveform and Test Circuits**

**VOLTAGE FOLLOWER  
PULSE RESPONSE**

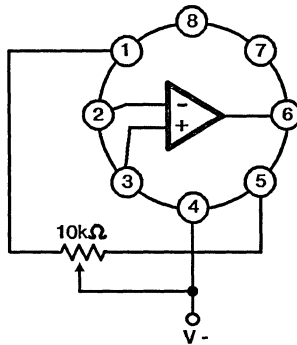
$R_L = 5K, C_L = 50pF$      $T_A = +25^{\circ}C$   
 Vertical = 10V/Div.     $V_S = \pm 40V$   
 Horizontal = 5 $\mu s$ /Div.



**SLEW RATE AND TRANSIENT  
RESPONSE TEST CIRCUIT**



**SUGGESTED  $V_{OS}$  ADJUSTMENT**



Tested Offset Adjustment Range is  $|V_{OS} + 1mV|$  minimum referred to output. Typical range is  $\pm 20mV$  with  $R_T = 10k\Omega$ .

**PRELIMINARY**

May 1991

**Very High Slew Rate Wideband Operational Amplifier**
**Features**

- Low Supply Current ..... 13mA
- Very High Slew Rate ..... 625V/ $\mu$ s
- Open Loop Gain ..... 25kV/V
- Wide Gain-Bandwidth ( $A_v \geq 10$ ) ..... 600MHz
- Full Power Bandwidth ..... 10MHz
- Low Offset Voltage ..... 0.6mV
- Differential Gain/Phase ..... 0.03%/0.03 $^\circ$
- Enhanced Replacement for EL2039

**Applications**

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- RF Oscillators

**Description**

The HA-2839 is a wideband, very high slew rate, operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction, coupled with dielectric isolation, delivers outstanding performance in circuits with a closed loop gain of 10 or greater.

A 625V/ $\mu$ s slew rate and a 600MHz gain bandwidth product ensure high performance in video and RF amplifier designs. Differential gain and phase are a low 0.03% and 0.03 degrees respectively, making the HA-2839 ideal for video

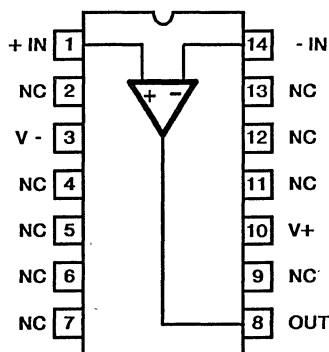
applications. A full  $\pm 10$ V output swing, high open loop gain, and outstanding A.C. parameters, make the HA-2839 an excellent choice for high speed Data Acquisition Systems.

The HA-2839 is available in commercial and industrial temperature ranges, and a choice of packages. See the "Ordering Information" section below for more information.

For military grade product, refer to the HA-2839/883 data sheet.

**Pinout**

HA1-2839 (CERAMIC DIP)  
HA3-2839 (PLASTIC DIP)  
TOP VIEW



(N.C.) No Connection pins may be tied to a ground plane for better isolation and heat dissipation.

**Ordering Information**

| PART NUMBER | TEMPERATURE RANGE                | PACKAGE            |
|-------------|----------------------------------|--------------------|
| HA1-2839-5  | 0 $^\circ$ C to +75 $^\circ$ C   | 14 Pin Ceramic DIP |
| HA3-2839-5  | 0 $^\circ$ C to +75 $^\circ$ C   | 14 Pin Plastic DIP |
| HA1-2839-9  | -40 $^\circ$ C to +85 $^\circ$ C | 14 Pin Ceramic DIP |
| HA3-2839-9  | -40 $^\circ$ C to +85 $^\circ$ C | 14 Pin Plastic DIP |

**3**  
OPERATIONAL AMPLIFIERS

## Specifications HA-2839

### Absolute Maximum Ratings (Note 1)

|   |           |
|---|-----------|
| Voltage Between V+ and V- Terminals             | 35V       |
| Differential Input Voltage                      | ±6V       |
| Peak Output Current                             | 50mA      |
| Continuous Output Current                       | 33mA Arms |
| Internal Quiescent Power Dissipation (Note 2)   | 525mW     |
| Maximum Junction Temperature (Note 2)           | +175°C    |
| Maximum Junction Temperature (Plastic Packages) | +150°C    |
|   | (Note 2)  |

### Operating Temperature Range

|                           |  |
|---------------------------|--|
| HA-2839-5                 | $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$    |
| HA-2839-9                 | $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  |
| Storage Temperature Range | $-65^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ |

### Electrical Specifications $V_{\text{SUPPLY}} = \pm 15\text{V}$ , $R_L = 1\text{k}\Omega$ , $C_L \leq 10\text{pF}$ , Unless Otherwise Specified.

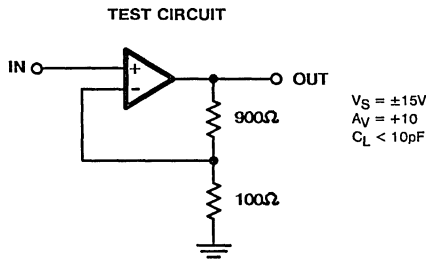
| PARAMETER  | TEMP  | HA-2839-5, -9 |      |      | UNITS                          |
|--|-------|---------------|------|------|--------------------------------|
|  |       | MIN           | TYP  | MAX  |                                |
| <b>INPUT CHARACTERISTICS</b>   |       |               |      |      |                                |
| Offset Voltage   | +25°C | -             | 0.6  | 2    | mV                             |
|  | Full  | -             | 2    | 6    | mV                             |
| Average Offset Voltage Drift   | Full  | -             | 20   | -    | $\mu\text{V}/^{\circ}\text{C}$ |
| Bias Current   | +25°C | -             | 5    | 14.5 | $\mu\text{A}$                  |
|  | Full  | -             | 8    | 20   | $\mu\text{A}$                  |
| Offset Current   | +25°C | -             | 1    | 4    | $\mu\text{A}$                  |
|  | Full  | -             | -    | 8    | $\mu\text{A}$                  |
| Input Resistance   | +25°C | -             | 10   | -    | k $\Omega$                     |
| Input Capacitance  | +25°C | -             | 1    | -    | pF                             |
| Common Mode Range  | Full  | ±10           | -    | -    | V                              |
| Input Noise Voltage<br>(f = 1kHz, $R_{\text{SOURCE}} = 0\Omega$ )          | +25°C | -             | 6    | -    | $\text{nV}/\sqrt{\text{Hz}}$   |
| Input Noise Current<br>(f = 1kHz, $R_{\text{SOURCE}} = 10\text{k}\Omega$ ) | +25°C | -             | 6    | -    | $\text{pA}/\sqrt{\text{Hz}}$   |
| <b>TRANSFER CHARACTERISTICS</b>  |       |               |      |      |                                |
| Large Signal Voltage Gain (Note 3)   | +25°C | 20K           | 25K  | -    | V/V                            |
|  | Full  | 15K           | 20K  | -    | V/V                            |
| Common-Mode Rejection Ratio (Note 4)                                       | Full  | 75            | 80   | -    | dB                             |
| Minimum Stable Gain  | +25°C | 10            | -    | -    | V/V                            |
| Gain Bandwidth Product (Notes 5 & 12)                                      | +25°C | -             | 600  | -    | MHz                            |
| <b>OUTPUT CHARACTERISTICS</b>  |       |               |      |      |                                |
| Output Voltage Swing (Note 3)  | Full  | ±10           | -    | -    | V                              |
| Output Current (Note 3)  | Full  | ±10           | ±20  | -    | mA                             |
| Output Resistance  | +25°C | -             | 30   | -    | $\Omega$                       |
| Full Power Bandwidth (Notes 3 & 7)   | +25°C | 8.7           | 10   | -    | MHz                            |
| Differential Gain (Notes 6 & 11)   | +25°C | -             | 0.03 | -    | %                              |
| Differential Phase (Notes 6 & 11)  | +25°C | -             | 0.03 | -    | Degrees                        |
| <b>TRANSIENT RESPONSE (Note 8)</b>   |       |               |      |      |                                |
| Rise Time  | +25°C | -             | 4    | -    | ns                             |
| Overshoot  | +25°C | -             | 20   | -    | %                              |
| Slew Rate (Notes 3 & 10)   | +25°C | 550           | 625  | -    | V/ $\mu\text{s}$               |
| Settling Time: 10V Step to 0.1%  | +25°C | -             | 180  | -    | ns                             |
| <b>POWER REQUIREMENTS</b>  |       |               |      |      |                                |
| Supply Current   | Full  | -             | 13   | 15   | mA                             |
| Power Supply Rejection Ratio (Note 9)                                      | Full  | 75            | 90   | -    | dB                             |

# HA-2839

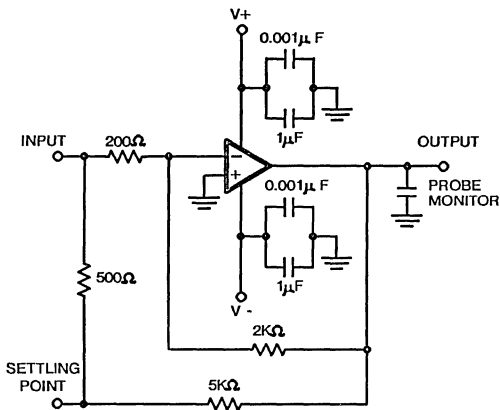
**NOTES:**

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. This value assumes a no load condition: Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below +175°C for ceramic packages and below +150°C for plastic packages.
3.  $R_L = 1k\Omega$ ,  $V_O = \pm 10V$ , 0 to  $\pm 10V$  for slew rate.
4.  $V_{CM} = \pm 10V$ .
5.  $V_O = 90mV$ .
6.  $A_V = +10$ .
7. Full Power Bandwidth guaranteed based on slew rate measurement using  $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$  ;  $V_{PEAK} = 10V$
8. Refer to Test Circuit section of data sheet.
9.  $V_{SUPPLY} = \pm 10VDC$  to  $\pm 20VDC$ .
10. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
11. Differential gain and phase are measured with a VM700A video tester, using a NTC-7 composite VITS.
12.  $A_V = +100$ .

## Test Circuits



## SETTLING TIME TEST CIRCUIT



- $A_V = -10$
- Load Capacitance should be less than 10pF.
- It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
- **SETTLING POINT** (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

**PRELIMINARY**

May 1991

**Very High Slew Rate Wideband Operational Amplifier**
**Features**

- Low Supply Current ..... 13mA
- Very High Slew Rate ..... 625V/ $\mu$ s
- Open Loop Gain ..... 25kV/V
- Wide Gain-Bandwidth ( $A_V \geq 10$ ) ..... 600MHz
- Full Power Bandwidth ..... 10MHz
- Low Offset Voltage ..... 0.6mV
- Differential Gain/Phase ..... 0.03%/0.03°
- Enhanced Replacement for AD840 and EL2040

**Applications**

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- RF Oscillators

**Description**

The HA-2840 is a wideband, very high slew rate, operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction, coupled with dielectric isolation, delivers outstanding performance in circuits with a closed loop gain of 10 or greater.

A 625V/ $\mu$ s slew rate and a 600MHz gain bandwidth product ensure high performance in video and RF amplifier designs. Differential gain and phase are a low 0.03% and 0.03 degrees respectively, making the HA-2840 ideal for video

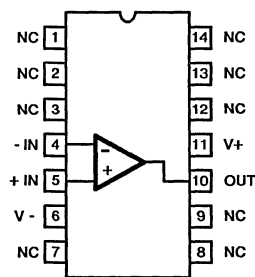
applications. A full  $\pm 10$ V output swing, high open loop gain, and outstanding A.C. parameters, make the HA-2840 an excellent choice for high speed Data Acquisition Systems.

The HA-2840 is available in commercial and industrial temperature ranges, and a choice of packages. See the "Ordering Information" section below for more information.

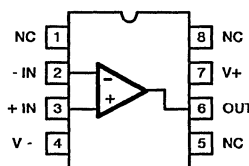
For military grade product, refer to the HA-2840/883 data sheet.

**Pinouts**

HA1-2840 (CERAMIC DIP)  
HA3B2840 (PLASTIC DIP)  
TOP VIEW



HA7-2840 (CERAMIC DIP)  
HA3-2840 (PLASTIC DIP)  
HA9P2840 (SOIC)  
TOP VIEW



(N.C.) No Connection pins may be tied to a ground plane for better isolation and heat dissipation.

**Ordering Information**

| PART NUMBER | TEMPERATURE RANGE | PACKAGE            |
|-------------|-------------------|--------------------|
| HA1-2840-5  | 0°C to +75°C      | 14 Pin Ceramic DIP |
| HA3B2840-5  | 0°C to +75°C      | 14 Pin Plastic DIP |
| HA7-2840-5  | 0°C to +75°C      | 8 Pin Ceramic DIP  |
| HA3-2840-5  | 0°C to +75°C      | 8 Pin Plastic DIP  |
| HA9P2840-5  | 0°C to +75°C      | 8 Pin SOIC         |
| HA1-2840-9  | -40°C to +85°C    | 14 Pin Ceramic DIP |
| HA3B2840-9  | -40°C to +85°C    | 14 Pin Plastic DIP |
| HA7-2840-9  | -40°C to +85°C    | 8 Pin Ceramic DIP  |
| HA3-2840-9  | -40°C to +85°C    | 8 Pin Plastic DIP  |
| HA9P2840-9  | -40°C to +85°C    | 8 Pin SOIC         |

## Specifications HA-2840

### Absolute Maximum Ratings (Note 1)

|   |        |
|---|--------|
| Voltage Between V+ and V- Terminals .....             | 35V    |
| Differential Input Voltage .....                      | ±6V    |
| Peak Output Current .....                             | 50mA   |
| Continuous Output Current .....                       | 33mA   |
| Internal Quiescent Power Dissipation (Note 2) .....   | 525mW  |
| Maximum Junction Temperature (Note 2) .....           | +175°C |
| Maximum Junction Temperature (Plastic Packages) ..... | +150°C |

(Note 2)

### Operating Temperature Range

|                                 |                                 |
|---------------------------------|---------------------------------|
| HA-2840-5 .....                 | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| HA-2840-9 .....                 | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| Storage Temperature Range ..... | -65°C ≤ T <sub>A</sub> ≤ +150°C |

**Electrical Specifications** V<sub>SUPPLY</sub> = ±15V, R<sub>L</sub> = 1kΩ, C<sub>L</sub> ≤ 10pF, Unless Otherwise Specified.

| PARAMETER   | TEMP  | HA-2840-5, -9 |      |      | UNITS   |
|---|-------|---------------|------|------|---------|
|   |       | MIN           | TYP  | MAX  |         |
| <b>INPUT CHARACTERISTICS</b>                                  |       |               |      |      |         |
| Offset Voltage  | +25°C | -             | 0.6  | 2    | mV      |
|   | Full  | -             | 2    | 6    | mV      |
| Average Offset Voltage Drift                                  | Full  | -             | 20   | -    | μV/°C   |
| Bias Current  | +25°C | -             | 5    | 14.5 | μA      |
|   | Full  | -             | 8    | 20   | μA      |
| Offset Current  | +25°C | -             | 1    | 4    | μA      |
|   | Full  | -             | -    | 8    | μA      |
| Input Resistance  | +25°C | -             | 10   | -    | kΩ      |
| Input Capacitance   | +25°C | -             | 1    | -    | pF      |
| Common Mode Range   | Full  | ±10           | -    | -    | V       |
| Input Noise Voltage<br>(f = 1kHz, R <sub>SOURCE</sub> = 0Ω)   | +25°C | -             | 6    | -    | nV/√Hz  |
| Input Noise Current<br>(f = 1kHz, R <sub>SOURCE</sub> = 10kΩ) | +25°C | -             | 6    | -    | pA/√Hz  |
| <b>TRANSFER CHARACTERISTICS</b>                               |       |               |      |      |         |
| Large Signal Voltage Gain (Note 3)                            | +25°C | 20K           | 25K  | -    | V/V     |
|   | Full  | 15K           | 20K  | -    | V/V     |
| Common-Mode Rejection Ratio (Note 4)                          | Full  | 75            | 80   | -    | dB      |
| Minimum Stable Gain   | +25°C | 10            | -    | -    | V/V     |
| Gain Bandwidth Product (Notes 5 & 12)                         | +25°C | -             | 600  | -    | MHz     |
| <b>OUTPUT CHARACTERISTICS</b>                                 |       |               |      |      |         |
| Output Voltage Swing (Note 3)                                 | Full  | ±10           | -    | -    | V       |
| Output Current (Note 3)                                       | Full  | ±10           | ±20  | -    | mA      |
| Output Resistance   | +25°C | -             | 30   | -    | Ω       |
| Full Power Bandwidth (Notes 3 & 7)                            | +25°C | 8.7           | 10   | -    | MHz     |
| Differential Gain (Notes 6 & 11)                              | +25°C | -             | 0.03 | -    | %       |
| Differential Phase (Notes 6 & 11)                             | +25°C | -             | 0.03 | -    | Degrees |
| <b>TRANSIENT RESPONSE (Note 8)</b>                            |       |               |      |      |         |
| Rise Time   | +25°C | -             | 4    | -    | ns      |
| Overshoot   | +25°C | -             | 20   | -    | %       |
| Slew Rate (Notes 3 & 10)                                      | +25°C | 550           | 625  | -    | V/μs    |
| Settling Time: 10V Step to 0.1%                               | +25°C | -             | 180  | -    | ns      |
| <b>POWER REQUIREMENTS</b>                                     |       |               |      |      |         |
| Supply Current  | Full  | -             | 13   | 15   | mA      |
| Power Supply Rejection Ratio (Note 9)                         | Full  | 75            | 90   | -    | dB      |

**3**  
OPERATIONAL  
AMPLIFIERS

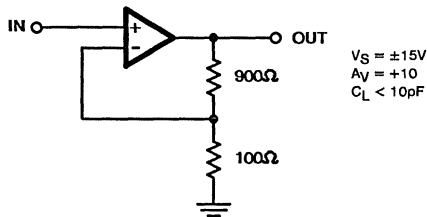
# HA-2840

## NOTES:

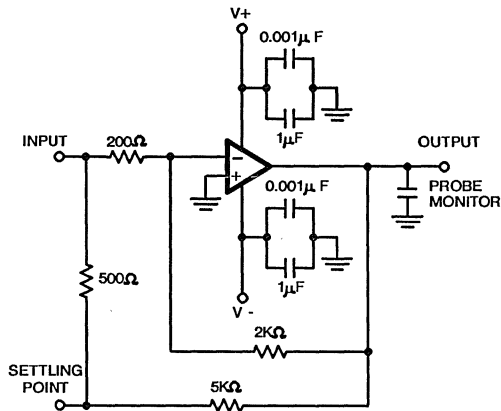
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. This value assumes a no load condition: Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below +175°C for ceramic packages and below +150°C for plastic packages.
3.  $R_L = 1k\Omega$ ,  $V_O = \pm 10V$ , 0 to  $\pm 10V$  for slew rate.
4.  $V_{CM} = \pm 10V$ .
5.  $V_O = 90mV$ .
6.  $A_V = +10$ .
7. Full Power Bandwidth guaranteed based on slew rate measurement using  $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$ ;  $V_{PEAK} = 10V$
8. Refer to Test Circuit section of data sheet.
9.  $V_{SUPPLY} = \pm 10VDC$  to  $\pm 20VDC$ .
10. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
11. Differential gain and phase are measured with a VM700A video tester, using a NTC-7 composite VITS.
12.  $A_V = +100$ .

## Test Circuits

### TEST CIRCUIT



### SETTLING TIME TEST CIRCUIT



- $A_V = -10$
- Load Capacitance should be less than 10pF.
- It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
- SETTLING POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

**PRELIMINARY**
**Wideband, Fast Settling, Unity Gain Stable,  
Video Operational Amplifier**

May 1991

**Features**

- Low Supply Current ..... 10mA
- Unity Gain Bandwidth ..... 54MHz
- High Slew Rate ..... 240V/ $\mu$ s
- Low Offset Voltage ..... 1mV
- Fast Settling Time (0.1%) ..... 90ns
- Full Power Bandwidth ..... 3.8MHz
- Differential Gain/Phase ..... 0.03%/0.03°
- Enhanced Replacement for AD841 and EL2041

**Applications**

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters
- High Speed A/D Input Buffer

**Description**

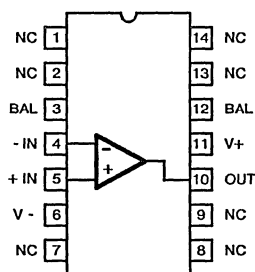
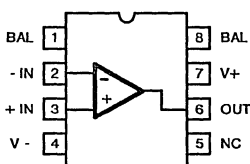
The HA-2841 is a wideband, unity gain stable, operational amplifier featuring a 54MHz unity gain bandwidth and excellent D.C. specifications.

The 240V/ $\mu$ s slew rate and 54MHz gain bandwidth product ensure high performance in video and pulse amplifier design. Differential gain and phase are a low 0.03% and 0.03 degrees respectively, making the HA-2841 an even better choice for video applications. A full  $\pm 10V$  output

swing, high open loop gain, rapid settling time, and outstanding A.C. parameters make the HA-2841 an excellent choice for high speed Data Acquisition Systems.

The HA-2841 is available in commercial and industrial temperature ranges, and a choice of packages. See the "Ordering Information" section below for more information.

For military grade product, refer to the HA-2841/883 data sheet.

**Pinouts**
**HA3B2841 (PLASTIC DIP)  
TOP VIEW**

**HA3-2841 (PLASTIC DIP)  
HA9P2841 (SOIC)  
TOP VIEW**


(N.C.) No Connection pins may be tied to a ground plane for better isolation and heat dissipation.

**Ordering Information**

| PART NUMBER | TEMPERATURE RANGE | PACKAGE            |
|-------------|-------------------|--------------------|
| HA3B2841-5  | 0°C to +75°C      | 14 Pin Plastic DIP |
| HA3-2841-5  | 0°C to +75°C      | 8 Pin Plastic DIP  |
| HA9P2841-5  | 0°C to +75°C      | 8 Pin SOIC         |
| HA3B2841-9  | -40°C to +85°C    | 14 Pin Plastic DIP |
| HA3-2841-9  | -40°C to +85°C    | 8 Pin Plastic DIP  |
| HA9P2841-9  | -40°C to +85°C    | 8 Pin SOIC         |



## Specifications HA-2841

### Absolute Maximum Ratings (Note 1)

|   |                       |
|---|-----------------------|
| Voltage Between V+ and V- Terminals .....             | 35V                   |
| Differential Input Voltage .....                      | ±6V                   |
| Peak Output Current .....                             | 50mA                  |
|   | 10mA (50% Duty Cycle) |
| Maximum Junction Temperature (Note 11) .....          | +175°C                |
| Maximum Junction Temperature (Plastic Packages) ..... | +150°C                |

### Operating Temperature Range

|                                 |                                 |
|---------------------------------|---------------------------------|
| HA-2841-5 .....                 | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| HA-2841-9 .....                 | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| Storage Temperature Range ..... | -65°C ≤ T <sub>A</sub> ≤ +150°C |

**Electrical Specifications** V<sub>SUPPLY</sub> = ±15V, R<sub>L</sub> = 1kΩ, C<sub>L</sub> ≤ 10pF, Unless Otherwise Specified.

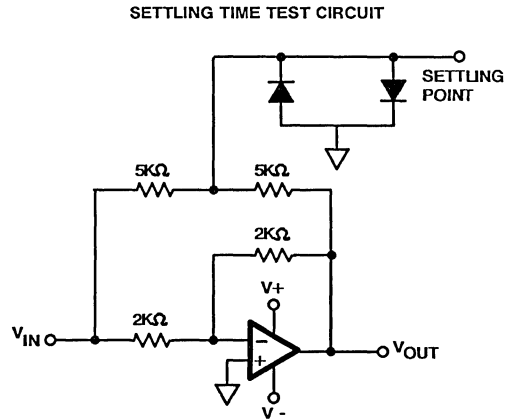
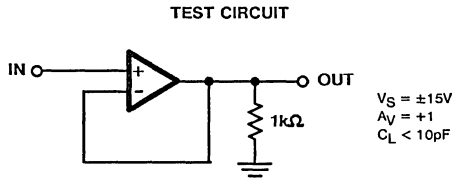
| PARAMETER   | TEMP  | HA-2841-5, -9 |       |     | UNITS   |
|---|-------|---------------|-------|-----|---------|
|   |       | MIN           | TYP   | MAX |         |
| <b>INPUT CHARACTERISTICS</b>  |       |               |       |     |         |
| Offset Voltage  | +25°C | -             | 1     | 3   | mV      |
|   | Full  | -             | -     | 6   | mV      |
| Average Offset Voltage Drift  | Full  | -             | 14    | -   | μV/°C   |
| Bias Current  | +25°C | -             | 5     | 10  | μA      |
|   | Full  | -             | 8     | 15  | μA      |
| Average Bias Current Drift  | Full  | -             | 45    | -   | nA/°C   |
| Offset Current  | +25°C | -             | 0.5   | 1.0 | μA      |
|   | Full  | -             | -     | 1.5 | μA      |
| Input Resistance  | +25°C | -             | 170   | -   | kΩ      |
| Input Capacitance   | +25°C | -             | 1     | -   | pF      |
| Common Mode Range   | Full  | ±10           | -     | -   | V       |
| Input Noise Voltage (10Hz to 1MHz)                                    | +25°C | -             | 16    | -   | μVrms   |
| Input Noise Voltage Density<br>(f = 1kHz, R <sub>SOURCE</sub> = 0Ω)   | +25°C | -             | 16    | -   | nV/√Hz  |
| Input Noise Current Density<br>(f = 1kHz, R <sub>SOURCE</sub> = 10kΩ) | +25°C | -             | 2     | -   | pA/√Hz  |
| <b>TRANSFER CHARACTERISTICS</b>                                       |       |               |       |     |         |
| Large Signal Voltage Gain (Note 3)                                    | +25°C | 25K           | 50K   | -   | V/V     |
|   | Full  | 10K           | 30K   | -   | V/V     |
| Common-Mode Rejection Ratio (Note 4)                                  | Full  | 80            | 95    | -   | dB      |
| Minimum Stable Gain   | +25°C | 1             | -     | -   | V/V     |
| Gain Bandwidth Product (Note 5)                                       | +25°C | -             | 54    | -   | MHz     |
| <b>OUTPUT CHARACTERISTICS</b>   |       |               |       |     |         |
| Output Voltage Swing  | Full  | ±10           | ±10.5 | -   | V       |
| Output Current (Note 6)   | Full  | 15            | 30    | -   | mA      |
| Output Resistance   | +25°C | -             | 8.5   | -   | Ω       |
| Full Power Bandwidth (Notes 3 & 7)                                    | +25°C | 3.2           | 3.8   | -   | MHz     |
| Differential Gain (Note 2)  | +25°C | -             | 0.03  | -   | %       |
| Differential Phase (Note 2)   | +25°C | -             | 0.03  | -   | Degrees |
| Harmonic Distortion (Note 10)   | +25°C | -             | >83   | -   | dB      |
| <b>TRANSIENT RESPONSE (Note 8)</b>                                    |       |               |       |     |         |
| Rise Time   | +25°C | -             | 3     | -   | ns      |
| Overshoot   | +25°C | -             | 33    | -   | %       |
| Slew Rate (Note 12)   | +25°C | 200           | 240   | -   | V/μs    |
| Settling Time: 10V Step to 0.1%                                       | +25°C | -             | 90    | -   | ns      |
| <b>POWER REQUIREMENTS</b>   |       |               |       |     |         |
| Supply Current  | +25°C | -             | 10    | -   | mA      |
|   | Full  | -             | 10    | 11  | mA      |
| Power Supply Rejection Ratio (Note 9)                                 | Full  | 70            | 80    | -   | dB      |

# HA-2841

**NOTES:**

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Differential gain and end phase are measured with a VM700A video tester, using a NTC-7 composite VITS.  $R_F = R_1 = 1K$ ,  $R_L = 700\Omega$ .
3.  $V_O = \pm 10V$ .
4.  $V_{CM} = \pm 10V$ .
5.  $A_{VCL} = 1000$ , Measured at unity gain crossing.
6.  $V_O = \pm 10$ ,  $R_L$  unconnected. Output duty cycle must be reduced if  $I_{OUT} > 10mA$ .
7. Full Power Bandwidth guaranteed based on slow rate measurement using  $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$ ;  $V_{PEAK} = 10V$
8. Refer to Test Circuit section of data sheet.
9.  $V_{SUPPLY} = \pm 10VDC$  to  $\pm 20VDC$ .
10.  $V_O = 2Vp-p$ ;  $f = 1MHz$ ;  $A_V = +1$ .
11. Maximum power dissipation, including output load, must be designed to maintain the maximum junction temperature below  $+175^\circ C$  for ceramic packages, and below  $+150^\circ C$  for the plastic packages.
12.  $A_V = +1$ . This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.

## Test Circuits



- $A_V = -1$
- Feedback and summing resistors must be matched (0.1%).
- HP5082-2810 clipping diodes recommended.
- Tektronix P6201 FET probe used at settling point.

## Die Characteristics

|                            |   |               |
|----------------------------|---|---------------|
| Transistor Count .....     | 43  |               |
| Die Dimensions .....       | 7.7 x 8.1 x 1.9 mils<br>(1960μm x 2060μm x 485μm) |               |
| Substrate Potential* ..... | V-  |               |
| Process .....              | High Frequency Bipolar-DI                         |               |
| Thermal Constants (°C/W)   | $\theta_{ja}$                                     | $\theta_{jc}$ |
| HA3B2841, Plastic DIP      | 89  | 28            |
| HA9P2841, SOIC             | 157   | 42            |
| HA3-2841, Plastic Mini-DIP | 92  | 30            |

\*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

**PRELIMINARY**
**Wideband, High Slew Rate, High Output Current,  
Video Operational Amplifier**

August 1991

**Features**

- Stable at Gains of 2 or Greater
- Gain Bandwidth ..... 80MHz
- High Slew Rate ..... 400V/ $\mu$ s
- High Output Current (Min) ..... 100mA
- Differential Gain/Phase ..... 0.02%/0.03 $^{\circ}$
- Low Supply Current (Max) ..... 15mA
- Low Input Offset Voltage ..... 1mV
- Enhanced Replacement for AD842

**Applications**

- Pulse and Video Amplifiers
- Wideband Amplifiers
- Coaxial Cable Drivers
- Fast Sample-Hold Circuits
- High Frequency Signal Conditioning Circuits

**Description**

The HA-2842 is a wideband, high slew rate, monolithic operational amplifier featuring an outstanding combination of speed, bandwidth, and output drive capability.

Utilizing the advantages of the Harris D. I. technology this amplifier offers 400V/ $\mu$ s slew rate, 80MHz gain bandwidth, and  $\pm$ 100mA output current. Application of this device is further enhanced through stable operation down to closed loop gains of 2.

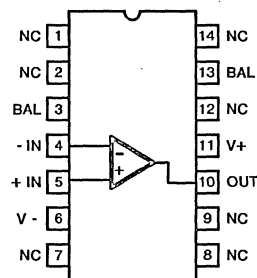
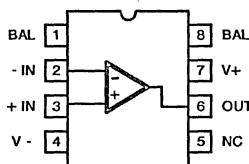
For additional flexibility, offset null controls are included in the HA-2842 pinout.

The capabilities of the HA-2842 are ideally suited for high speed coaxial cable driver circuits where low gain and high output drive requirements are necessary. With 6MHz full

power bandwidth, this amplifier is most suitable for high frequency signal conditioning circuits and pulse video amplifiers. Differential gain and phase are a low 0.02% and 0.03 degrees, respectively, making the HA-2842 ideal for video applications.

The HA-2842 is available in a Plastic 14 lead DIP package, which is pin compatible with the HA-2542 and AD842. The HA-2842 is also available in Plastic 8 Lead DIP and SOIC packages. See the "Ordering Information" section below for more information.

For information about using high output current operational amplifiers, please refer to Application Note 556 (Thermal Safe-Operating-Areas For High Current Op Amps). Please refer to the /883 data sheet for military compliant product.

**Pinouts**
**HA3B2842 (PLASTIC DIP)  
TOP VIEW**

**HA3-2842 (PLASTIC DIP)  
HA9P2842 (SOIC)  
TOP VIEW**

**Ordering Information**

| PART NUMBER | TEMPERATURE RANGE                    | PACKAGE            |
|-------------|--------------------------------------|--------------------|
| HA3B2842-5  | 0 $^{\circ}$ C to +75 $^{\circ}$ C   | 14 Pin Plastic DIP |
| HA3-2842-5  | 0 $^{\circ}$ C to +75 $^{\circ}$ C   | 8 Pin Plastic DIP  |
| HA9P2842-5  | 0 $^{\circ}$ C to +75 $^{\circ}$ C   | 8 Pin SOIC         |
| HA3B2842-9  | -40 $^{\circ}$ C to +85 $^{\circ}$ C | 14 Pin Plastic DIP |
| HA3-2842-9  | -40 $^{\circ}$ C to +85 $^{\circ}$ C | 8 Pin Plastic DIP  |
| HA9P2842-9  | -40 $^{\circ}$ C to +85 $^{\circ}$ C | 8 Pin SOIC         |

## Specifications HA-2842

### Absolute Maximum Ratings (Note 1)

|   |  |
|---|--|
| Voltage between V+ and V- Terminals             | 35V                                    |
| Differential Input Voltage                      | ±6V                                    |
| Output Current                                  | 125mA (Peak)<br>100mA (50% Duty Cycle) |
| Maximum Junction Temperature (Note 11)          | +175°C                                 |
| Maximum Junction Temperature (Plastic Packages) | +150°C                                 |

### Operating Temperature Range

|                           |                                 |
|---------------------------|---------------------------------|
| HA-2842-5                 | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| HA-2842-9                 | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| Storage Temperature Range | -65°C ≤ T <sub>A</sub> ≤ +150°C |

**Electrical Specifications** V<sub>SUPPLY</sub> = ±15 Volts; R<sub>L</sub> = 1kΩ, C<sub>L</sub> ≤ 10pF, Unless Otherwise Specified.

| PARAMETER   | TEMP  | HA-2842-5/-9 |      |     | UNITS   |
|---|-------|--------------|------|-----|---------|
|   |       | MIN          | TYP  | MAX |         |
| <b>INPUT CHARACTERISTICS</b>                                    |       |              |      |     |         |
| Offset Voltage  | +25°C | -            | 1    | 3   | mV      |
|   | Full  | -            | -    | 6   | mV      |
| Average Offset Voltage Drift                                    | Full  | -            | 13   | -   | μV/°C   |
| Bias Current  | +25°C | -            | 5    | 10  | μA      |
|   | Full  | -            | -    | 15  | μA      |
| Average Bias Current Drift                                      | Full  | -            | 20   | -   | nA/°C   |
| Offset Current  | +25°C | -            | 0.5  | 1.0 | μA      |
|   | Full  | -            | -    | 1.5 | μA      |
| Average Offset Current Drift                                    | Full  | -            | 1.3  | -   | nA/°C   |
| Input Resistance  | +25°C | -            | 170  | -   | kΩ      |
| Input Capacitance   | +25°C | -            | 1    | -   | pF      |
| Common Mode Range   | Full  | ±10          | -    | -   | V       |
| Input Noise Voltage (10Hz to 1MHz)                              | +25°C | -            | 16   | -   | μVrms   |
| Input Noise Voltage Density (fo = 1kHz, R <sub>S</sub> = 0Ω)    | +25°C | -            | 16   | -   | nV/√Hz  |
| Input Noise Current Density (fo = 1kHz, R <sub>S</sub> = 100kΩ) | +25°C | -            | 2    | -   | pA/√Hz  |
| <b>TRANSFER CHARACTERISTICS</b>                                 |       |              |      |     |         |
| Large Signal Voltage Gain (Note 3)                              | +25°C | 50k          | 100k | -   | V/V     |
|   | Full  | 30k          | 60k  | -   | V/V     |
| Common-Mode Rejection Ratio (Note 4)                            | Full  | 80           | 110  | -   | dB      |
| Minimum Stable Gain   | +25°C | 2            | -    | -   | V/V     |
| Gain-Bandwidth-Product (Note 5)                                 | +25°C | -            | 80   | -   | MHz     |
| <b>OUTPUT CHARACTERISTICS</b>                                   |       |              |      |     |         |
| Output Voltage Swing (Note 3)                                   | Full  | ±10          | ±11  | -   | V       |
| Output Current (Note 6)   | Full  | 100          | -    | -   | mA      |
| Output Resistance   | +25°C | -            | 8.5  | -   | Ω       |
| Full Power Bandwidth (Note 3 & 7)                               | +25°C | 5.2          | 6    | -   | MHz     |
| Differential Gain (Note 2)                                      | +25°C | -            | 0.02 | -   | %       |
| Differential Phase (Note 2)                                     | +25°C | -            | 0.03 | -   | Degrees |
| Harmonic Distortion (Note 10)                                   | +25°C | -            | >81  | -   | dB      |
| <b>TRANSIENT RESPONSE (Note 8)</b>                              |       |              |      |     |         |
| Rise Time   | +25°C | -            | 4    | -   | ns      |
| Overshoot   | +25°C | -            | 25   | -   | %       |
| Slew Rate (Note 12)   | +25°C | 325          | 400  | -   | V/μs    |
| Settling Time: 10V Step to 0.1%                                 | +25°C | -            | 100  | -   | ns      |
| <b>POWER REQUIREMENTS</b>                                       |       |              |      |     |         |
| Supply Current  | +25°C | -            | 14.2 | -   | mA      |
|   | Full  | -            | 14.3 | 15  | mA      |
| Power Supply Rejection Ratio (Note 9)                           | Full  | 70           | 80   | -   | dB      |

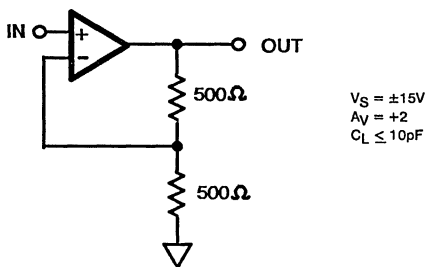
**3**  
OPERATIONAL  
AMPLIFIERS

NOTES:

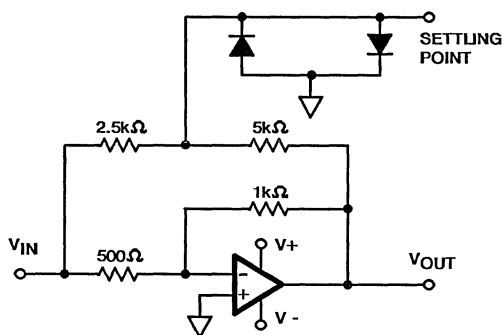
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Differential gain and phase are measured with a VM700A video tester, using a NTC-7 composite VITS.  $R_F = R_1 = 1K$ ,  $R_L = 700\Omega$ .
3.  $R_L = 1k\Omega$ ,  $V_O = \pm 10V$
4.  $V_{CM} = \pm 10V$
5.  $A_{VCL} = 100$
6.  $V_O = \pm 5V$ ,  $R_L$  Unconnected
7. Full Power Bandwidth guaranteed based on slew rate measurement using  $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$ ;  $V_{PEAK} = 10V$
8. Refer to Test Circuits section of this data sheet.
9.  $V_{SUPPLY} = \pm 10VDC$  to  $\pm 20VDC$
10.  $V_O = 2V_{p-p}$ ;  $f = 1MHz$ ;  $A_V = +2$ .
11. This value assumes a no load condition: Maximum power dissipation, including output load, must be designed to maintain the maximum junction temperature below  $+175^\circ C$  for ceramic packages, and below  $+150^\circ C$  for plastic packages. By using Application Note 556 on Safe Operating Area equations, along with the packaging thermal resistances listed in the Die Characteristics section, proper load conditions can be determined. Heat sinking is recommended above  $+75^\circ C$  with suggested models:  
 14 Lead Ceramic DIP:  
 Thermalloy #6007 or AAVID #5602B ( $\theta_{sa} = 16^\circ C/W$ ).  
 12 Lead Metal Can (TO-8):  
 Thermalloy #2240A ( $\theta_{sa} = 27^\circ C/W$ ) or #2268B ( $\theta_{sa} = 24^\circ C/W$ )
12.  $A_V = +2$ . This parameter is not tested. The limits are guaranteed based on fab characterization and reflect lot-to-lot variation.

Test Circuits

TEST CIRCUIT



SETTLING TIME TEST CIRCUIT



- $A_V = -2$
- Feedback and summing resistors must be matched (0.1%)
- HP5082-2810 clipping diodes recommended
- Tektronix P6201 FET probe used at settling point
- For 0.01% settling time, heat sinking is suggested to reduce thermal effects and an analog ground plane with supply decoupling is suggested to minimize ground loop errors.

Die Characteristics

|                            |  |               |
|----------------------------|--|---------------|
| Transistor Count .....     | 43   |               |
| Die Dimensions .....       | 77 x 81 x 19 mils<br>(1960μm x 2060μm x 485μm) |               |
| Substrate Potential* ..... | V-   |               |
| Process .....              | High Frequency Bipolar-DI                      |               |
| Passivation .....          | Nitride  |               |
| Thermal Constants (°C/W)   | $\theta_{ja}$                                  | $\theta_{jc}$ |
| HA3B2842 Plastic DIP       | 89   | 28            |
| HA3-2842 Plastic Mini-DIP  | 92   | 30            |
| HA9P2842 SOIC              | 157  | 42            |

\*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

Typical Applications

The Harris HA-2842 is a state of the art monolithic device which also approaches the "ALL-IN-ONE" amplifier concept. This device features an outstanding set of AC parameters augmented by excellent output drive capability providing for suitable application in both high speed and high output drive circuits.

Primarily intended to be used in balanced 50Ω and 75Ω coaxial cable systems as a driver, the HA-2842 could also be used as a power booster in audio systems as well as a power amp in power supply circuits. This device would also be suitable as a small DC motor driver.

Prototyping Guidelines

For best overall performance in any application, it is recommended that high frequency layout techniques be used. This should include: 1) mounting the device through a ground plane; 2) connecting unused pins (N.C.) to the ground plane; 3) mounting feedback components on Teflon standoffs and/or locating these components as close to the device as possible; 4) placing power supply decoupling capacitors from device supply pins to ground.

**PRELIMINARY**
**Low Power, High Slew Rate, Wideband Operational Amplifier**

August 1991

**Features**

- Low Supply Current ..... 7.5mA
- High Slew Rate ..... 340V/ $\mu$ s
- Open Loop Gain ..... 25kV/V
- Wide Gain-Bandwidth ( $A_V \geq 10$ ) ..... 470MHz
- Full Power Bandwidth ..... 5.4MHz
- Low Offset Voltage ..... 0.6mV
- Input Noise Voltage ..... 11.0nV/ $\sqrt{\text{Hz}}$
- Differential Gain/Phase ..... 0.04%/0.04 $^\circ$
- Lower Power Enhanced Replacement for AD840 and EL2040

**Applications**

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters

**Description**

The HA-2850 is a wideband, high slew rate, operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction, coupled with dielectric isolation, delivers outstanding performance in circuits with a closed loop gain of 10 or greater.

A 340V/ $\mu$ s slew rate and a 470MHz gain bandwidth product ensure high performance in video and wideband amplifier designs. Differential gain and phase are a low 0.04% and 0.04 degrees respectively, making the HA-2850 ideal for video applications. A full  $\pm 10\text{V}$  output swing, high open

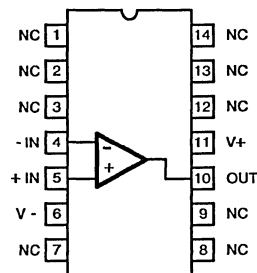
loop gain, and outstanding A.C. parameters, make the HA-2850 an excellent choice for high speed Data Acquisition Systems.

The HA-2850 is available in commercial and industrial temperature ranges, and a choice of packages. See the "Ordering Information" section below for more information.

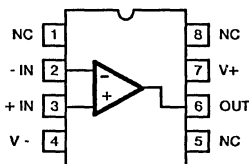
For military grade product, refer to the HA-2850/883 data sheet.

**Pinouts**

HA1-2850 (CERAMIC DIP)  
HA3B2850 (PLASTIC DIP)  
TOP VIEW



HA7-2850 (CERAMIC DIP)  
HA3-2850 (PLASTIC DIP)  
HA9P2850 (SOIC)  
TOP VIEW



(N.C.) No Connection pins may be tied to a ground plane for better isolation and heat dissipation.

**Ordering Information**

| PART NUMBER | TEMPERATURE RANGE                | PACKAGE            |
|-------------|----------------------------------|--------------------|
| HA1-2850-5  | 0 $^\circ$ C to +75 $^\circ$ C   | 14 Pin Ceramic DIP |
| HA3B2850-5  | 0 $^\circ$ C to +75 $^\circ$ C   | 14 Pin Plastic DIP |
| HA7-2850-5  | 0 $^\circ$ C to +75 $^\circ$ C   | 8 Pin Ceramic DIP  |
| HA3-2850-5  | 0 $^\circ$ C to +75 $^\circ$ C   | 8 Pin Plastic DIP  |
| HA9P2850-5  | 0 $^\circ$ C to +75 $^\circ$ C   | 8 Pin SOIC         |
| HA1-2850-9  | -40 $^\circ$ C to +85 $^\circ$ C | 14 Pin Ceramic DIP |
| HA3B2850-9  | -40 $^\circ$ C to +85 $^\circ$ C | 14 Pin Plastic DIP |
| HA7-2850-9  | -40 $^\circ$ C to +85 $^\circ$ C | 8 Pin Ceramic DIP  |
| HA3-2850-9  | -40 $^\circ$ C to +85 $^\circ$ C | 8 Pin Plastic DIP  |
| HA9P2850-9  | -40 $^\circ$ C to +85 $^\circ$ C | 8 Pin SOIC         |

**3**  
 OPERATIONAL AMPLIFIERS

## Specifications HA-2850

### Absolute Maximum Ratings (Note 1)

|   |        |
|---|--------|
| Voltage Between V+ and V- Terminals .....             | 35V    |
| Differential Input Voltage.....                       | ±6V    |
| Maximum Junction Temperature.....                     | +175°C |
| Maximum Junction Temperature (Plastic Packages) ..... | +150°C |

### Operating Temperature Range

|                                 |                                 |
|---------------------------------|---------------------------------|
| HA-2850-5 .....                 | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| HA-2850-9 .....                 | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| Storage Temperature Range ..... | -65°C ≤ T <sub>A</sub> ≤ +150°C |

### Electrical Specifications V<sub>SUPPLY</sub> = ±15V, R<sub>L</sub> = 1kΩ, C<sub>L</sub> ≤ 10pF, Unless Otherwise Specified.

| PARAMETER  | TEMP  | HA-2850-5, -9 |      |      | UNITS   |
|--|-------|---------------|------|------|---------|
|  |       | MIN           | TYP  | MAX  |         |
| <b>INPUT CHARACTERISTICS</b>   |       |               |      |      |         |
| Offset Voltage   | +25°C | -             | 0.6  | 2    | mV      |
|  | Full  | -             | 2    | 6    | mV      |
| Average Offset Voltage Drift   | Full  | -             | 20   | -    | μV/°C   |
| Bias Current   | +25°C | -             | 5    | 14.5 | μA      |
|  | Full  | -             | 8    | 20   | μA      |
| Offset Current   | +25°C | -             | 1    | 4    | μA      |
|  | Full  | -             | -    | 8    | μA      |
| Input Resistance   | +25°C | -             | 10   | -    | kΩ      |
| Input Capacitance  | +25°C | -             | 1    | -    | pF      |
| Common Mode Range  | Full  | ±10           | -    | -    | V       |
| Input Noise Voltage<br>(f <sub>o</sub> = 1kHz, R <sub>SOURCE</sub> = 0Ω)   | +25°C | -             | 11   | -    | nV/√Hz  |
| Input Noise Current<br>(f <sub>o</sub> = 1kHz, R <sub>SOURCE</sub> = 10kΩ) | +25°C | -             | 6    | -    | pA/√Hz  |
| <b>TRANSFER CHARACTERISTICS</b>  |       |               |      |      |         |
| Large Signal Voltage Gain (Note 3)   | +25°C | 20K           | 25K  | -    | V/V     |
|  | Full  | 15K           | 20K  | -    | V/V     |
| Common-Mode Rejection Ratio (Note 4)                                       | Full  | 75            | 80   | -    | dB      |
| Minimum Stable Gain  | +25°C | 10            | -    | -    | V/V     |
| Gain Bandwidth Product (Notes 5 & 11)                                      | +25°C | -             | 470  | -    | MHz     |
| <b>OUTPUT CHARACTERISTICS</b>  |       |               |      |      |         |
| Output Voltage Swing (Note 3)  | Full  | ±10           | ±11  | -    | V       |
| Output Current (Note 3)  | Full  | ±10           | ±20  | -    | mA      |
| Output Resistance  | +25°C | -             | 30   | -    | Ω       |
| Full Power Bandwidth (Notes 3 & 7)   | +25°C | 4.8           | 5.4  | -    | MHz     |
| Differential Gain (Notes 2 & 6)  | +25°C | -             | 0.04 | -    | %       |
| Differential Phase (Notes 2 & 6)   | +25°C | -             | 0.04 | -    | Degrees |
| <b>TRANSIENT RESPONSE (Note 8)</b>   |       |               |      |      |         |
| Rise Time  | +25°C | -             | 5    | -    | ns      |
| Overshoot  | +25°C | -             | 25   | -    | %       |
| Slew Rate (Notes 3 & 10)   | +25°C | 300           | 340  | -    | V/μs    |
| Settling Time: 10V Step to 0.1%  | +25°C | -             | 200  | -    | ns      |
| <b>POWER REQUIREMENTS</b>  |       |               |      |      |         |
| Supply Current   | Full  | -             | 7.5  | 8.0  | mA      |
| Power Supply Rejection Ratio (Note 9)                                      | Full  | 75            | 90   | -    | dB      |

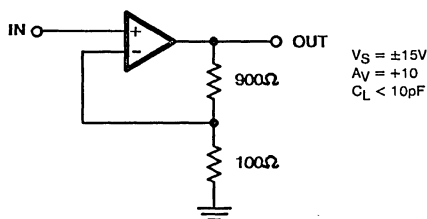
## HA-2850

### NOTES:

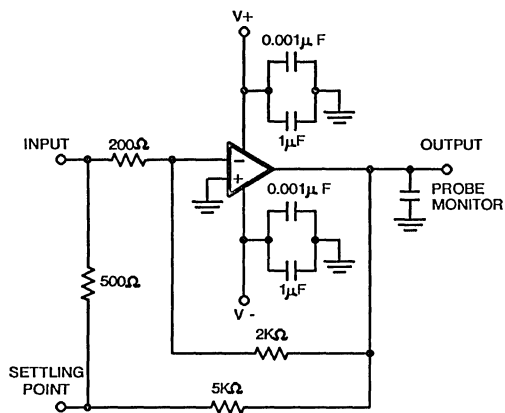
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Differential gain and end phase are measured with a VM700A video tester, using a NTC-7 composite VITS.
3.  $R_L = 1k\Omega$ ,  $V_O = \pm 10V$ , 0 to  $\pm 10V$  for slew rate.
4.  $V_{CM} = \pm 10V$ .
5.  $V_O = 90mV$ .
6.  $A_V = +10$ .
7. Full Power Bandwidth guaranteed based on slew rate measurement using  $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$ ;  $V_{PEAK} = 10V$
8. Refer to Test Circuit section of data sheet.
9.  $V_{SUPPLY} = \pm 10VDC$  to  $\pm 20VDC$ .
10. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
11.  $A_V = +100$ .

### Test Circuits

#### TEST CIRCUIT



#### SETTLING TIME TEST CIRCUIT



- $A_V = -10$
- Load Capacitance should be less than 10pF.
- It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
- SETTLING POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 588 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.



August 1991

## Quad Operational Amplifier

### Features

- Slew Rate ..... 1.6V/ $\mu$ s
- Bandwidth ..... 3.5MHz
- Input Voltage Noise ..... 9nV/ $\sqrt{\text{Hz}}$
- Input Offset Voltage ..... 0.5mV
- Input Bias Current ..... 60nA
- Supply Range .....  $\pm 2\text{V}$  to  $\pm 20\text{V}$
- No Crossover Distortion
- Standard Quad Pinout

### Description

HA-4741, which contains four amplifiers on a monolithic chip, provides a new measure of performance for general purpose operational amplifiers. Each amplifier in the HA-4741 has operating specifications that equal or exceed those of the 741-type amplifier in all categories of performance.

HA-4741 is well suited to applications requiring accurate signal processing by virtue of its low values of input offset voltage (0.5mV), input bias current (60nA) and input voltage noise (9nV/ $\sqrt{\text{Hz}}$  at 1kHz). 3.5MHz bandwidth, coupled with high open-loop gain, allow the HA-4741 to be used in designs requiring amplification of wide band signals, such as audio amplifiers. Audio application is further enhanced by the HA-4741's negligible output crossover distortion.

### Applications

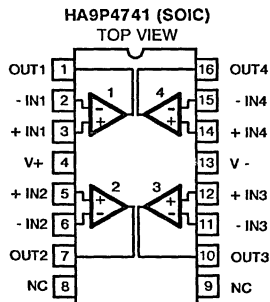
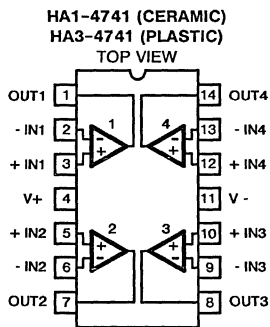
- Universal Active Filters
- D3 Communications Filters
- Audio Amplifiers
- Battery-Powered Equipment

These excellent dynamic characteristics also make the HA-4741 ideal for a wide range of active filter designs. Performance integrity of multi-channel designs is assured by a high level of amplifier-to-amplifier isolation (108dB at 10kHz).

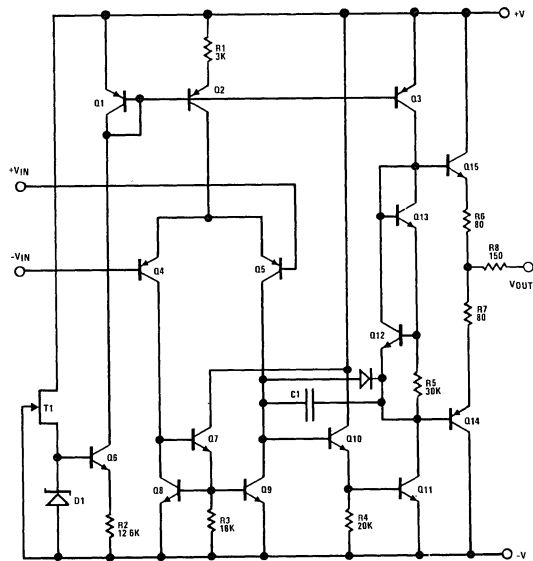
A wide range of supply voltages ( $\pm 2\text{V}$  to  $\pm 20\text{V}$ ) can be used to power the HA-4741, making it compatible with almost any system including battery-powered equipment.

The HA-4741 is available in plastic or ceramic 14 lead DIP packages. The HA-4741-2 operates from  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  and the HA-4741-5 operates over the  $0^\circ\text{C}$  to  $+75^\circ\text{C}$  temperature range. HA-4741/883 product and data sheets available upon request. This device is also offered in a 16 pin SOIC package with  $-5$  or  $-9$  temperature options.

### Pinouts



### Schematic



¼ HA-4741

## Specifications HA-4741

### Absolute Maximum Ratings (Note 13)

|   |                    |
|---|--------------------|
| $T_A = +25^\circ\text{C}$ Unless Otherwise Stated |                    |
| Voltage Between V+ and V- Terminals               | 40.0V              |
| Differential Input Voltage                        | $\pm 30.0\text{V}$ |
| Input Voltage (Note 1)                            | $\pm 15.0\text{V}$ |
| Output Short Circuit Duration (Note 2)            | Indefinite         |
| Power Dissipation For Plastic Package (Note 3)    | 880mW              |

### Operating Temperature Ranges

|                           |  |
|---------------------------|--|
| HA-4741-2                 | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ |
| HA-4741-5                 | $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$    |
| HA-4741-9                 | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$  |
| Storage Temperature Range | $-65^\circ\text{C} \leq T_A \leq +150^\circ\text{C}$ |

### Electrical Specifications $V_+ = +15\text{V}$ , $V_- = -15\text{V}$ , Unless Otherwise Specified.

| PARAMETER                                   | TEMP                  | HA-4741-2 |            |     | HA-4741-5 |            |     | (NOTE 14)<br>HA-4741-9 | UNITS                        |
|---|-----------------------|-----------|------------|-----|-----------|------------|-----|------------------------|------------------------------|
|   |                       | MIN       | TYP        | MAX | MIN       | TYP        | MAX | MAX                    |                              |
| <b>INPUT CHARACTERISTICS</b>                |                       |           |            |     |           |            |     |                        |                              |
| Offset Voltage                              | +25°C                 | -         | 0.5        | 3   | -         | 1          | 5   | 5                      | mV                           |
|   | Full                  | -         | 4          | 5   | -         | 4          | 6.5 | 8.5                    | mV                           |
| Average Offset Voltage Drift                | Full                  | -         | 5          | -   | -         | 5          | -   | -                      | $\mu\text{V}/^\circ\text{C}$ |
| Bias Current                                | +25°C                 | -         | 60         | 200 | -         | 60         | 300 | 300                    | nA                           |
|   | Full                  | -         | -          | 325 | -         | -          | 400 | 400                    | nA                           |
| Offset Current                              | +25°C                 | -         | 15         | 30  | -         | 30         | 50  | 50                     | nA                           |
|   | Full                  | -         | -          | 75  | -         | -          | 100 | 100                    | nA                           |
| Common Mode Range                           | Full                  | $\pm 12$  | -          | -   | $\pm 12$  | -          | -   | -                      | V                            |
| Differential Input Resistance               | +25°C                 | -         | 0.5        | -   | -         | 0.5        | -   | -                      | M $\Omega$                   |
| Input Voltage Noise (f = 1kHz)              | +25°C                 | -         | 9          | -   | -         | 9          | -   | -                      | $\text{nV}/\sqrt{\text{Hz}}$ |
| <b>TRANSFER CHARACTERISTICS</b>             |                       |           |            |     |           |            |     |                        |                              |
| Large Signal Voltage Gain (Notes 4)         | +25°C                 | 50K       | 100K       | -   | 25K       | 50K        | -   | -                      | V/V                          |
|   | Full                  | 25K       | -          | -   | 15K       | -          | -   | -                      | V/V                          |
| Common Mode Rejection Ratio                 | +25°C                 | 80        | 95         | -   | 80        | 95         | -   | -                      | dB                           |
|   | Full                  | 74        | -          | -   | 74        | -          | -   | -                      | dB                           |
| Channel Separation (Note 5)                 | +25°C                 | 90        | 108        | -   | 90        | 108        | -   | -                      | dB                           |
| Small Signal Bandwidth                      | +25°C                 | 2.5       | 3.5        | -   | 2.5       | 3.5        | -   | -                      | MHz                          |
| <b>OUTPUT CHARACTERISTICS</b>               |                       |           |            |     |           |            |     |                        |                              |
| Output Voltage Swing ( $R_L = 10\text{K}$ ) | Full                  | $\pm 12$  | $\pm 13.7$ | -   | $\pm 12$  | $\pm 13.7$ | -   | -                      | V                            |
|   | ( $R_L = 2\text{K}$ ) | $\pm 10$  | $\pm 12.5$ | -   | $\pm 10$  | $\pm 12.5$ | -   | -                      | V                            |
| Full Power Bandwidth (Notes 4 & 9)          | +25°C                 | 14        | 25         | -   | 14        | 25         | -   | -                      | kHz                          |
| Output Current (Note 6)                     | Full                  | $\pm 5$   | $\pm 15$   | -   | $\pm 5$   | $\pm 15$   | -   | -                      | mA                           |
| Output Resistance                           | +25°C                 | -         | 300        | -   | -         | 300        | -   | -                      | $\Omega$                     |
| <b>TRANSIENT RESPONSE (Note 7 &amp; 10)</b> |                       |           |            |     |           |            |     |                        |                              |
| Rise Time (Note 11)                         | +25°C                 | -         | 75         | 140 | -         | 75         | 140 | 140                    | ns                           |
| Overshoot (Note 11)                         | +25°C                 | -         | 25         | 40  | -         | 25         | 40  | 40                     | %                            |
| Slew Rate (Note 12)                         | +25°C                 | -         | $\pm 1.6$  | -   | -         | $\pm 1.6$  | -   | -                      | V/ $\mu\text{s}$             |
| <b>POWER SUPPLY CHARACTERISTICS</b>         |                       |           |            |     |           |            |     |                        |                              |
| Supply Current                              | +25°C                 | -         | 4.5        | 5   | -         | 5          | 7   | 7                      | mA                           |
| Power Supply Rejection Ratio (Note 8)       | Full                  | 80        | 95         | -   | 80        | 95         | -   | -                      | dB                           |

#### NOTES:

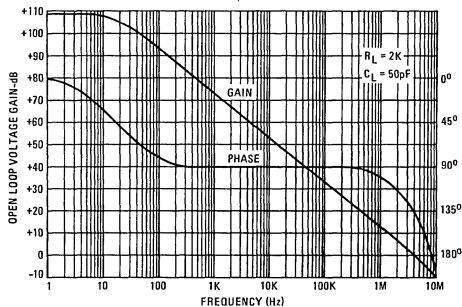
1. For supply voltages less than  $\pm 15\text{V}$ , the absolute maximum input voltage is equal to the supply voltage.
2. One amplifier may be shorted to ground indefinitely.
3. Derate  $5.8\text{mW}/^\circ\text{C}$  above  $T_A = +25^\circ\text{C}$ .
4.  $V_{\text{OUT}} = \pm 10$ ,  $R_L = 2\text{K}$ .
5. Referred to input;  $f = 10\text{kHz}$ ,  $R_S = 1\text{K}$ .
6.  $V_{\text{OUT}} = \pm 10$ .
7. See Pulse Response Characteristics.
8.  $\Delta V = \pm 5\text{V}$ .
9. Full power bandwidth guaranteed based upon slew rate measurement  $\text{FPBW} = \text{S.R.}/2\pi V_{\text{PEAK}}$ .
10.  $R_L = 2\text{K}$ ,  $C_L = 50\text{pF}$ .
11.  $V_{\text{OUT}} = \pm 200\text{mV}$ .
12.  $V_{\text{OUT}} = \pm 5\text{V}$ .
13. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
14. Typical and Minimum specifications for the -9 version are the same as those for the -5 version.

3

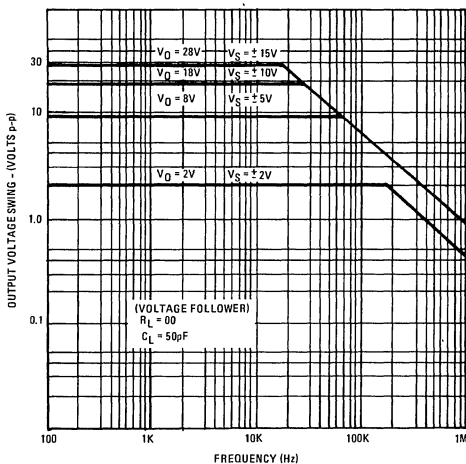
OPERATIONAL  
AMPLIFIERS

**Typical Performance Curves**  $V_+ = +15V$ ,  $V_- = -15V$ ,  $T_A = +25^\circ C$ , Unless Otherwise Specified.

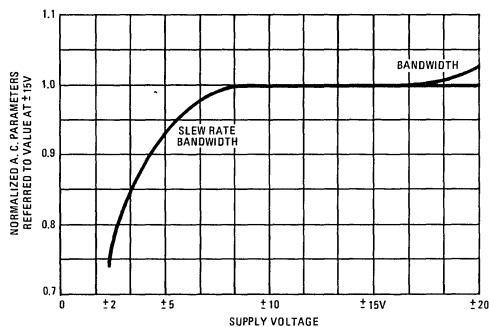
**OPEN LOOP FREQUENCY RESPONSE**



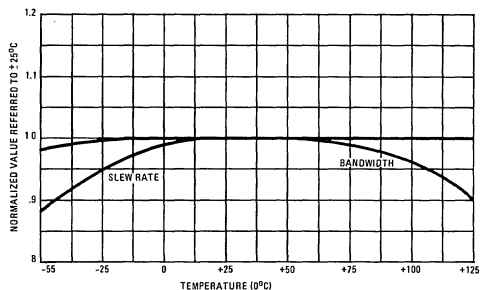
**OUTPUT VOLTAGE SWING vs. FREQUENCY**



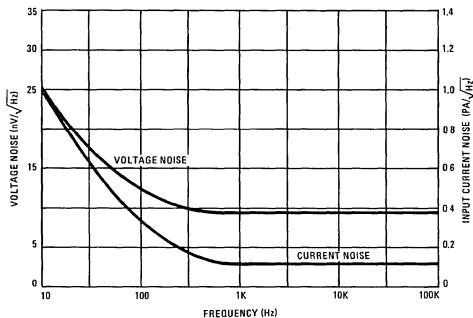
**NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE**



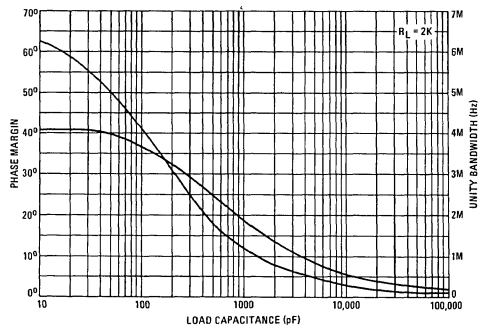
**NORMALIZED AC PARAMETERS vs. TEMPERATURE**



**INPUT NOISE vs. FREQUENCY**

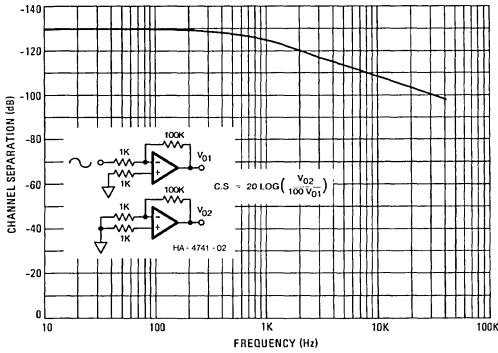


**SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE**

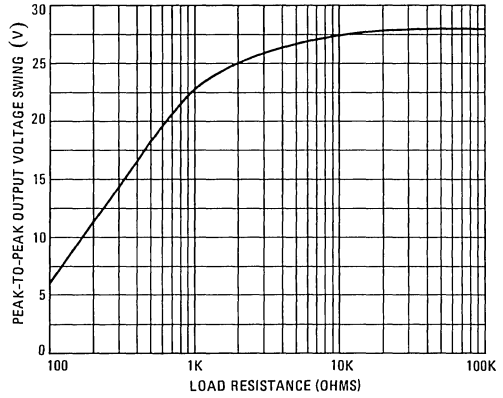


Typical Performance Curves (Continued)

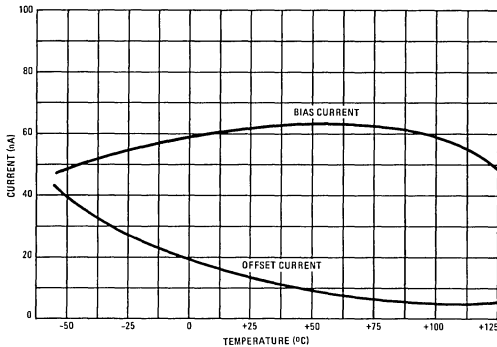
CHANNEL SEPARATION vs. FREQUENCY



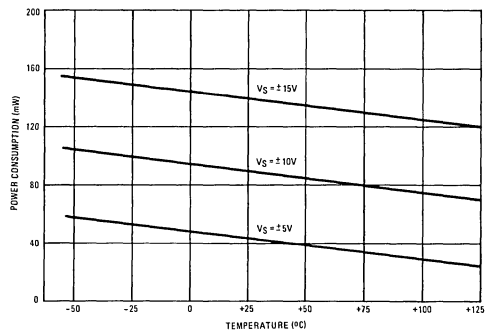
MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE

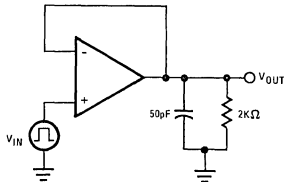


POWER CONSUMPTION vs. TEMPERATURE

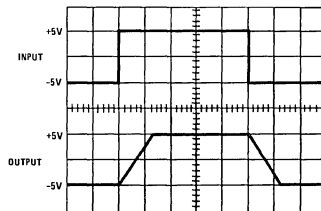


Pulse Response

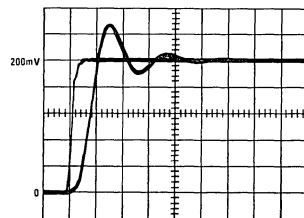
TRANSIENT RESPONSE/SLEW RATE CIRCUIT



SLEW RESPONSE (Volts: 5V/Div., Time: 5μs/Div.)



TRANSIENT RESPONSE (Volts: 40mV/Div., Time: 100ns/Div.)



3  
OPERATIONAL AMPLIFIERS

## Monolithic, Wideband, High Slew Rate, High Output Current Buffer

August 1991

### Features

- Voltage Gain ..... 0.995
- High Input Impedance ..... 3000k $\Omega$
- Low Output Impedance ..... 3 $\Omega$
- Very High Slew Rate ..... 1300V/ $\mu$ sec
- Very Wide Bandwidth ..... 110MHz
- High Output Current .....  $\pm$ 200mA
- Pulsed Output Current ..... 400mA
- Monolithic Construction

### Applications

- Line Driver
- Data Acquisition
- 110MHz Buffer
- High Power Current Booster
- High Power Current Source
- Sample and Holds
- Radar Cable Driver
- Video Products

### Description

The HA-5002 is a monolithic, wideband, high slew rate, high output current, buffer amplifier.

Utilizing the advantages of the Harris D.I. technologies, the HA-5002 current buffer offers 1300V/ $\mu$ sec slew rate with 110MHz of bandwidth. The  $\pm$ 200mA output current capability is enhanced by a 3 $\Omega$  output impedance.

The monolithic HA-5002 will replace the hybrid LH0002 with corresponding performance increases. These characteristics range from the 3000k $\Omega$  input impedance to the increased output voltage swing. Monolithic design technologies have

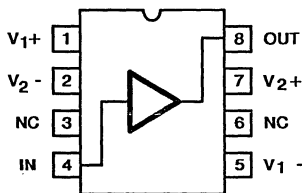
allowed a more precise buffer to be developed with more than an order of magnitude smaller gain error.

The HA-5002 will provide many present hybrid users with a higher degree of reliability and at the same time increase overall circuit performance.

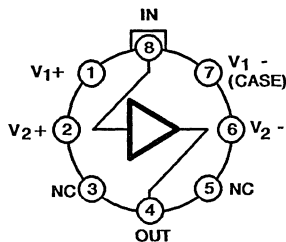
The HA-5002 is available in an 8 pin SOIC package, an 8 pin Metal Can, and 8 pin Ceramic and Plastic Mini-DIPs. For the military grade product, refer to the HA-5002/883 Data Sheet.

### Pinouts

HA9P5002 (SOIC)  
HA7-5002 (CERAMIC DIP)  
HA3-5002 (PLASTIC DIP)  
TOP VIEW

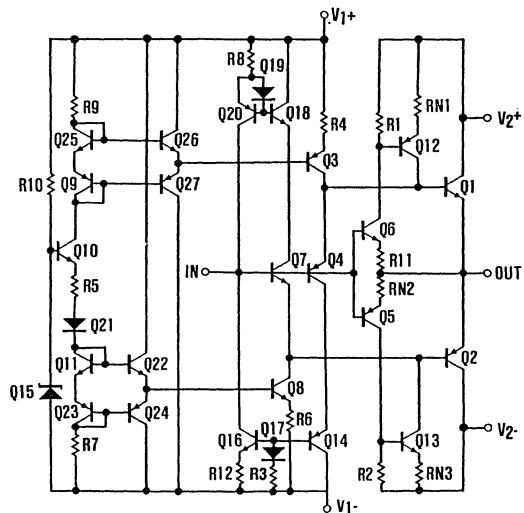


HA2-5002 TO-99 (METAL CAN)  
TOP VIEW



LCC Package Available for HA-5002/883.  
See HA-5002/883 Data Sheet

### Schematic



## Specifications HA-5002

### Absolute Maximum Ratings (Note 1)

|                                     |                                      |
|-------------------------------------|--------------------------------------|
| Voltage Between V+ and V- pins      | 44V                                  |
| Input Voltage                       | Equal to Supplies                    |
| Output Current                      | Continuous $\pm 200\text{mA}$        |
| Output Current                      | (50ms On, 1s Off) $\pm 400\text{mA}$ |
| Internal Power Dissipation (Note 2) |                                      |
| TO-99 (+25°C)                       | 1.13W                                |
| Mini-DIP (+25°C)                    | 1.22W                                |
| Plastic DIP (+25°C)                 | 1.88W                                |

### Operating Temperature Range

|                              |  |
|------------------------------|--|
| Maximum Junction Temperature | +150°C   |
| (Plastic Packages)           |  |
| Maximum Junction Temperature | +175°C   |
| HA-5002-2                    | $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ |
| HA-5002-5                    | $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$    |
| HA-5002-9                    | $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  |
| Storage Temperature Range    | $-65^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ |

### Electrical Specifications $V_{\text{SUPPLY}} = \pm 12\text{V}$ to $\pm 15\text{V}$ , $R_S = 50\Omega$ , $R_L = 1\text{k}\Omega$ , $C_L = 10\text{pF}$ , Unless Otherwise Specified.

| PARAMETER                             | TEMP                             | HA-5002-2 |          |            | HA-5002-5, -9 |          |            | UNITS                          |     |
|---------------------------------------|----------------------------------|-----------|----------|------------|---------------|----------|------------|--------------------------------|-----|
|                                       |                                  | MIN       | TYP      | MAX        | MIN           | TYP      | MAX        |                                |     |
| <b>INPUT CHARACTERISTICS</b>          |                                  |           |          |            |               |          |            |                                |     |
| Offset Voltage                        | +25°C                            | -         | 5        | 20         | -             | 5        | 20         | mV                             |     |
|                                       | Full                             | -         | 10       | 30         | -             | 10       | 30         | mV                             |     |
| Average Offset Voltage Drift          | Full                             | -         | 30       | -          | -             | 30       | -          | $\mu\text{V}/^{\circ}\text{C}$ |     |
| Bias Current                          | +25°C                            | -         | 2        | 7          | -             | 2        | 7          | $\mu\text{A}$                  |     |
|                                       | Full                             | -         | 3.4      | 10         | -             | 2.4      | 10         | $\mu\text{A}$                  |     |
| Input Resistance                      | Full                             | 1.5       | 3        | -          | 1.5           | 3        | -          | M $\Omega$                     |     |
| Input Noise Voltage (10Hz-1MHz)       | +25°C                            | -         | 4        | -          | -             | 4        | -          | $\mu\text{Vp-p}$               |     |
| <b>TRANSFER CHARACTERISTICS</b>       |                                  |           |          |            |               |          |            |                                |     |
| Voltage Gain (Note 7)                 | $R_L = 100\Omega$                | +25°C     | -        | 0.971      | -             | -        | 0.971      | -                              | V/V |
|                                       | $R_L = 1\text{k}\Omega$          | +25°C     | -        | 0.995      | -             | -        | 0.995      | -                              | V/V |
|                                       | $R_L = 1\text{k}\Omega$          | Full      | 0.990    | -          | -             | 0.980    | -          | -                              | V/V |
| -3dB Bandwidth (Note 4)               | +25°C                            | -         | 110      | -          | -             | 110      | -          | MHz                            |     |
| AC Current Gain                       | +25°C                            | -         | 40       | -          | -             | 40       | -          | A/mA                           |     |
| <b>OUTPUT CHARACTERISTICS</b>         |                                  |           |          |            |               |          |            |                                |     |
| Output Voltage Swing                  | $R_L = 100\Omega$                | +25°C     | $\pm 10$ | $\pm 10.7$ | -             | $\pm 10$ | $\pm 11.2$ | -                              | V   |
|                                       | $R_L = 1\text{k}\Omega$ (Note 3) | Full      | $\pm 10$ | $\pm 13.5$ | -             | $\pm 10$ | $\pm 13.9$ | -                              | V   |
|                                       | $R_L = 1\text{k}\Omega$ (Note 5) | Full      | $\pm 10$ | $\pm 10.5$ | -             | $\pm 10$ | $\pm 10.5$ | -                              | V   |
| Output Resistance                     | Full                             | -         | 3        | 10         | -             | 3        | 10         | $\Omega$                       |     |
| Harmonic Distortion (Note 6)          | +25°C                            | -         | <0.005   | -          | -             | <0.005   | -          | %                              |     |
| <b>TRANSIENT RESPONSE</b>             |                                  |           |          |            |               |          |            |                                |     |
| Full Power Bandwidth (Note 8)         | +25°C                            | -         | 41       | -          | -             | 41       | -          | MHz                            |     |
| Rise Time                             | +25°C                            | -         | 3.6      | -          | -             | 3.6      | -          | ns                             |     |
| Propagation Delay                     | +25°C                            | -         | 2        | -          | -             | 2        | -          | ns                             |     |
| Overshoot                             | +25°C                            | -         | 30       | -          | -             | 30       | -          | %                              |     |
| Slew Rate                             | +25°C                            | 1.0       | 1.3      | -          | 1.0           | 1.3      | -          | V/ns                           |     |
| Settling Time to 0.1%                 | +25°C                            | -         | 50       | -          | -             | 50       | -          | ns                             |     |
| <b>POWER REQUIREMENTS</b>             |                                  |           |          |            |               |          |            |                                |     |
| Supply Current                        | +25°C                            | -         | 8.3      | -          | -             | 8.3      | -          | mA                             |     |
|                                       | Full                             | -         | -        | 10         | -             | -        | 10         | mA                             |     |
| Power Supply Rejection Ratio (Note 9) | Full                             | 54        | 64       | -          | 54            | 64       | -          | dB                             |     |

#### NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. See thermal constants data in Die Characteristics section.
3.  $V_{\text{SUPPLY}} = \pm 15\text{V}$
4.  $V_{\text{IN}} = 1\text{V}_{\text{p-p}}$
5.  $V_{\text{SUPPLY}} = \pm 12\text{V}$
6.  $V_{\text{IN}} = 1\text{V}_{\text{RMS}}$ ;  $f = 10\text{kHz}$ .
7.  $V_{\text{OUT}} = \pm 10\text{V}$
8.  $\text{FPBW} = \frac{\text{Slew Rate}}{2\pi V_p}$   $V_p = 5\text{V}(10\text{Vp-p})$
9.  $\Delta V_{\text{SUPPLY}} = 10\text{V}$

### Operating Instructions

#### Layout Considerations

The wide bandwidth of the HA-5002 necessitates that high frequency circuit layout procedures be followed. Failure to follow these guidelines can result in marginal performance.

Probably the most crucial of the RF/video layout rules is the use of a ground plane. A ground plane provides isolation and minimizes distributed circuit capacitance and inductance which will degrade high frequency performance.

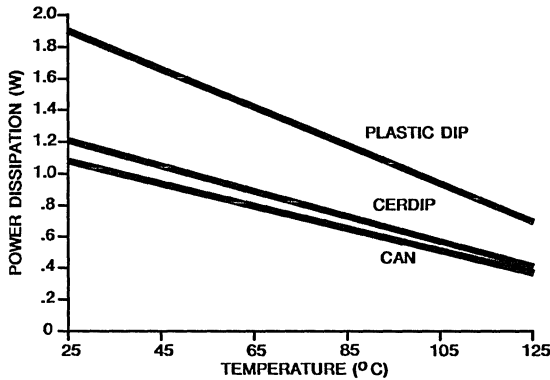
Other considerations are proper power supply bypassing and keeping the input and output connections as short as possible which minimizes distributed capacitance and reduces board space.

#### Power Supply Decoupling

For optimal device performance, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from 0.01 to 0.1  $\mu\text{F}$  will minimize high frequency variations in supply voltage, while low frequency bypassing requires larger valued capacitors since the impedance of the capacitor is dependent on frequency.

It is also recommended that the bypass capacitors be connected close to the HA-5002 (preferably directly to the supply pins).

#### FREE AIR POWER DISSIPATION



$$P_{dmax} = \frac{T_{jmax} - T_A}{\theta_{j-c} + \theta_{c-s} + \theta_{s-a}}$$

Where:  $T_{jmax}$  = Maximum Junction Temperature of the Device

$T_A$  = Ambient

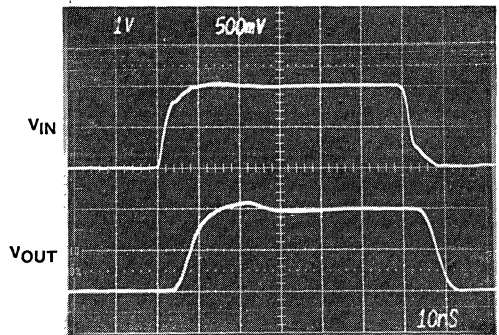
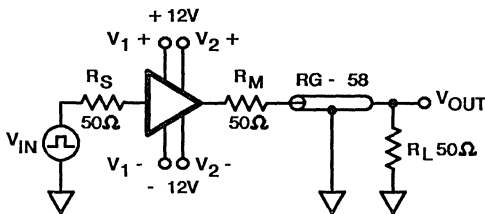
$\theta_{j-c}$  = Junction to Case Thermal Resistance

$\theta_{c-s}$  = Case to Heat Sink Thermal Resistance

$\theta_{s-a}$  = Heat Sink to Ambient Thermal Resistance

### Test Circuits

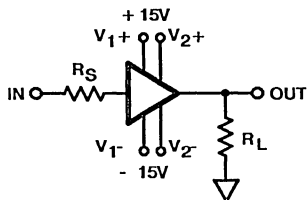
#### COAXIAL CABLE DRIVER - 50 $\Omega$ SYSTEM



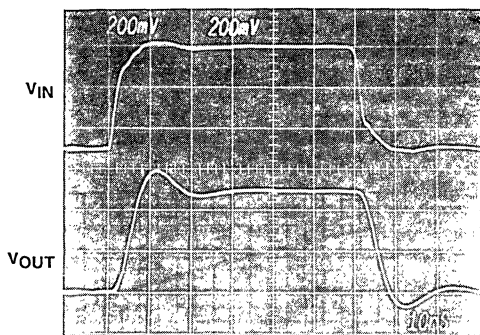
# HA-5002

## Test Circuits

### LARGE AND SMALL SIGNAL RESPONSE

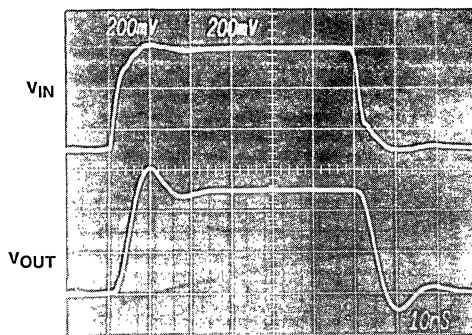


SMALL SIGNAL WAVEFORMS



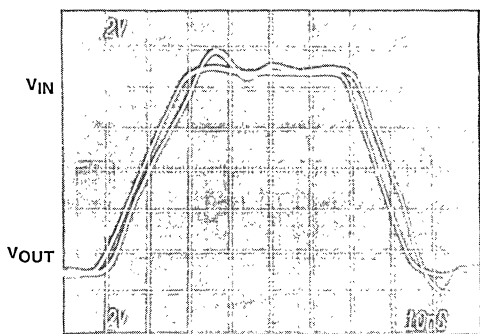
$R_S = 50\Omega$   
 $R_L = 100\Omega$

SMALL SIGNAL WAVEFORMS



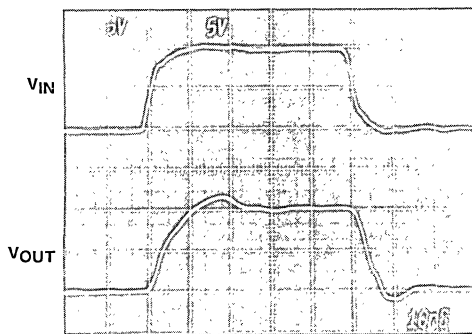
$R_S = 50\Omega$   
 $R_L = 1k\Omega$

LARGE SIGNAL WAVEFORMS



$R_S = 50\Omega$   
 $R_L = 1k\Omega$

LARGE SIGNAL WAVEFORMS



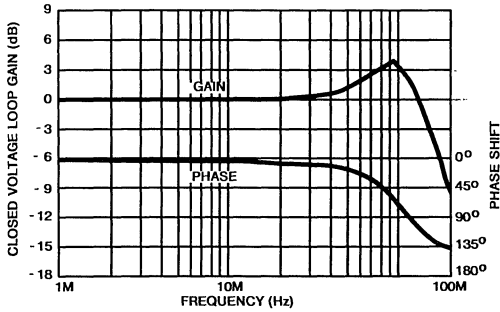
$R_S = 50\Omega$   
 $R_L = 1k\Omega$

3  
OPERATIONAL  
AMPLIFIERS

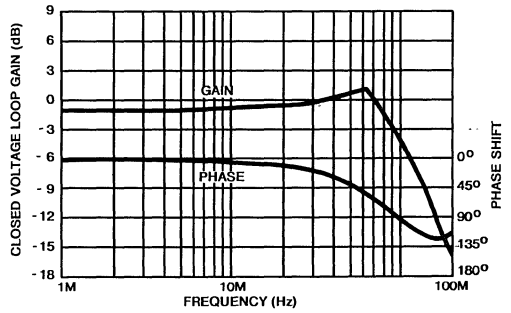


Typical Performance Curves

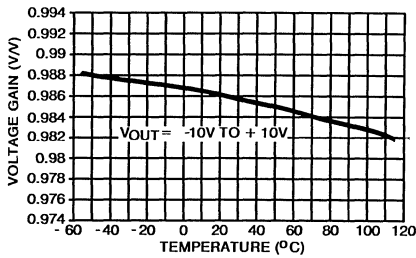
GAIN/PHASE vs. FREQUENCY  
 $V_{CC} = \pm 15V, R_L = 1K, R_S = 50\Omega$



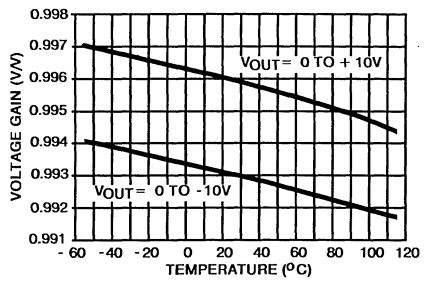
GAIN/PHASE vs. FREQUENCY  
 $V_{CC} = \pm 15V, R_L = 50\Omega, R_S = 50\Omega$



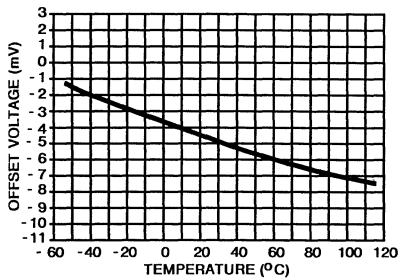
VOLTAGE GAIN vs. TEMPERATURE  
 $V_{CC} = \pm 15V, R_{LOAD} = 100\Omega$



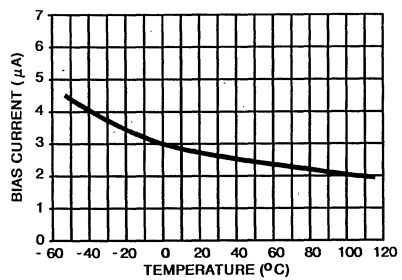
VOLTAGE GAIN vs. TEMPERATURE  
 $V_{CC} = \pm 15V, R_{LOAD} = 1k\Omega$



OFFSET VOLTAGE vs. TEMPERATURE  
 $V_{CC} = \pm 15V$

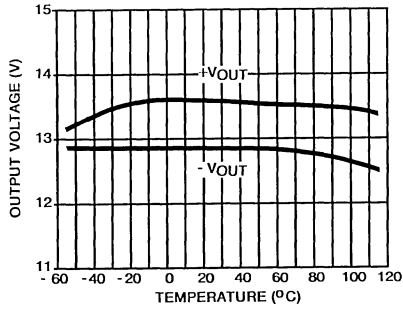


BIAS CURRENT vs. TEMPERATURE  
 $V_{CC} = \pm 15V$

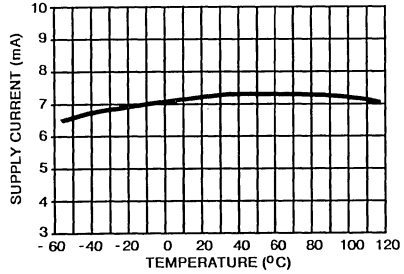


Typical Performance Curves (Continued)

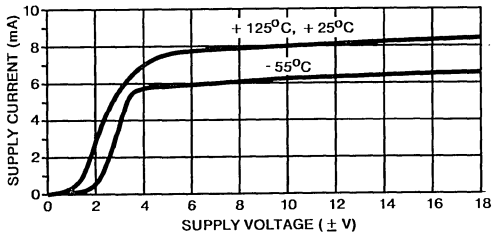
MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE  
 $V_{CC} = \pm 15V, R_{LOAD} = 100\Omega$



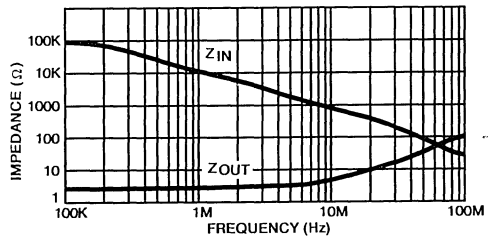
SUPPLY CURRENT vs. TEMPERATURE  
 $V_{CC} = \pm 15V, I_{OUT} = 0mA$



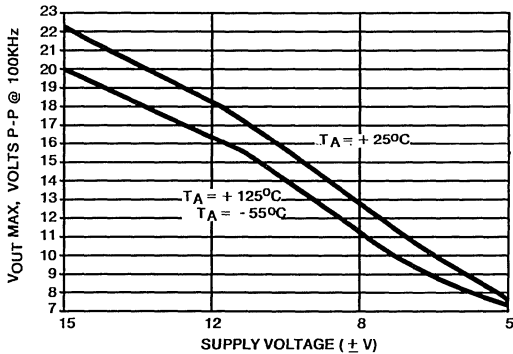
SUPPLY CURRENT vs. SUPPLY VOLTAGE  
 $I_{OUT} = 0mA$



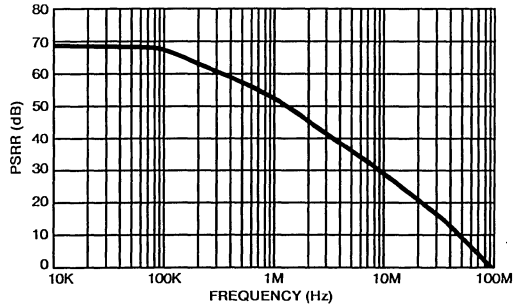
INPUT/OUTPUT IMPEDANCE vs. FREQUENCY  
 $V_{CC} = \pm 15V$



VOUT MAXIMUM vs. VSUPPLY  
 $R_{LOAD} = 100\Omega$

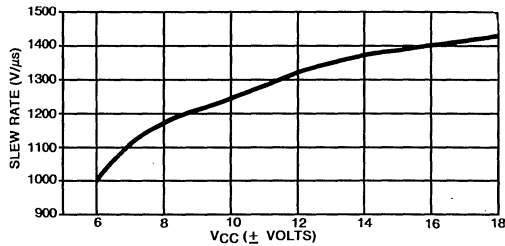


PSRR vs. FREQUENCY

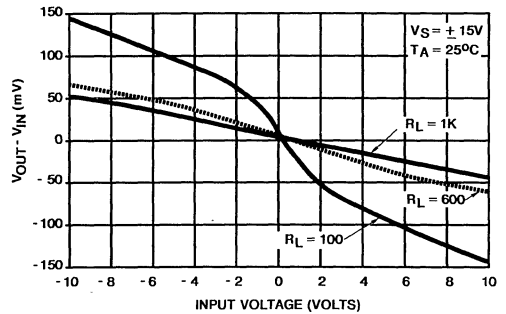


**Typical Performance Curves (Continued)**

**SLEW RATE vs. SUPPLY VOLTAGE**



**GAIN ERROR vs. INPUT VOLTAGE**



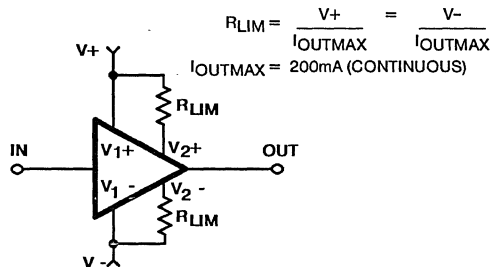
**Typical Applications**

**OPERATION AT REDUCED SUPPLY LEVELS**

The HA-5002 can operate at supply voltage levels as low as  $\pm 5V$  and lower. Output swing is directly affected as well as slight reductions in slew rate and bandwidth.

**SHORT CIRCUIT PROTECTION**

The Output current can be limited by using the following circuit:



**CAPACITIVE LOADING**

The HA-5002 will drive large capacitive loads without oscillation but peak current limits should not be exceeded. Following the formula  $I = C \frac{dv}{dt}$  implies that the slew rate or the capacitive load must be controlled to keep peak current below the maximum or use the current limiting approach as shown. The HA-5002 can become unstable with small capacitive loads (50pF) if certain precautions are not taken. Stability is enhanced by any one of the following: a source resistance in series with the input of 50Ω to 1K; increasing capacitive load to 150pF or greater; decreasing  $C_{LOAD}$  to 20pF or less; adding an output resistor of 10Ω to 50Ω; or adding feedback capacitance of 50pF or greater. Adding source resistance generally yields the best results.

**Die Characteristics**

|                            |  |               |
|----------------------------|--|---------------|
| Transistor Count .....     | 27   |               |
| Die Dimensions .....       | 80 x 81 x 19 mils<br>(2030μm x 2050μm x 480μm) |               |
| Substrate Potential* ..... | V1-  |               |
| Process .....              | Bipolar-DI                                     |               |
| Thermal Constants (°C/W)   | $\theta_{ja}$                                  | $\theta_{jc}$ |
| HA7-5002 Ceramic Mini-DIP  | 122  | 39            |
| HA3-5002 Plastic DIP       | 80   | 20            |
| HA2-5002 Metal Can         | 103  | 31            |
| HA9P5002 SOIC              | 160  | 42            |

\*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

August 1991

## 100MHz Current Feedback Amplifier

### Features

- Slew Rate ..... 1200V/ $\mu$ s
- Output Current.....  $\pm$ 100mA
- Drives .....  $\pm$ 9V into 100 $\Omega$
- $V_{SUPPLY}$  .....  $\pm$ 5V to  $\pm$ 18V
- Thermal Overload Protection and Output Flag
- Bandwidth Nearly Independent of Gain
- Output Enable/Disable

### Applications

- Unity Gain Video/Wideband Buffer
- Video Gain Block
- High Speed Peak Detector
- Fiber Optic Transmitters
- Zero Insertion Loss Transmission Line Drivers
- Current to Voltage Converter
- Radar Systems

### Description

The HA-5004 current feedback amplifier is a video/wideband amplifier optimized for low gain applications. The design is based on current-mode feedback which allows the amplifier to achieve higher closed loop bandwidth than voltage-mode feedback operational amplifiers. Since feedback is employed, the HA-5004 can offer better gain accuracy and lower distortion than open loop buffers. Unlike conventional op amps, the bandwidth and rise time of the HA-5004 are nearly independent of closed loop gain. The 100MHz bandwidth at unity gain reduces to only 65MHz at a gain of 10. The HA-5004 may be used in place of a conventional op amp with a significant improvement in speed power product.

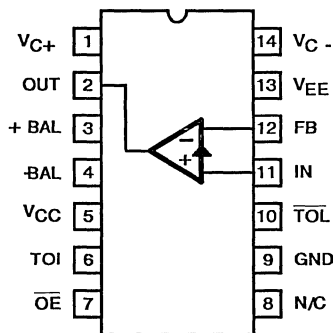
Several features have been designed in for added value. A thermal overload feature protects the part against excessive junction temperature by shutting down the output. If this feature is not needed, it can be inhibited via a TTL input (TOI). A TTL chip enable/disable ( $\overline{OE}$ ) input is also provided; when the chip is disabled its output is high impedance. Finally, an open collector output flag ( $\overline{TOL}$ ) is provided to indicate the status of the chip. The status flag goes low to indicate when the chip is disabled due to either the internal Thermal Overload shutdown or the external disable.

In order to maximize bandwidth and output drive capacity, internal current limiting is not provided. However, current limiting may be applied via the  $V_{C+}$  and  $V_{C-}$  pins which provide power separately to the output stage.

The HA-5004 is available in a 14-pin Ceramic DIP and is specified for operation from 0 $^{\circ}$ C to +75 $^{\circ}$ C (HA1-5004-5) and -40 $^{\circ}$ C to +85 $^{\circ}$ C (HA1-5004-9). For Military grade product refer to the HA-5004/883 data sheet.

### Pinouts

HA1-5004 (CERAMIC DIP)  
TOP VIEW



| INPUTS          |     | TEMP   | $\overline{TOL}$ OUTPUT<br>(OPEN COLLECTOR) | OPERATION                 |
|-----------------|-----|--------|---|---------------------------|
| $\overline{OE}$ | TOI | $T_J$  |   |                           |
| 0               | 0   | Normal | 1   | Normal                    |
| 0               | 0   | High*  | 0   | Auto Shutdown, Hi-Z OUT   |
| 0               | 1   | X      | 1   | Normal                    |
| 1               | X   | X      | 0   | Manual Shutdown, Hi-Z OUT |

\* $>$ 180 $^{\circ}$ C Typical

## Specifications HA-5004

### Absolute Maximum Ratings (Note 1)

|                                  |                      |
|----------------------------------|----------------------|
| Supply Voltage .....             | ±20V                 |
| Differential Input Voltage ..... | 5V                   |
| Common Mode Input Voltage .....  | ±V <sub>SUPPLY</sub> |
| Output Current .....             | ±120mA               |

### Operating Temperature Range

|                                    |                                 |
|------------------------------------|---------------------------------|
| HA-5004-9 .....                    | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| HA-5004-5 .....                    | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| Storage Temperature .....          | -65°C ≤ T <sub>A</sub> ≤ +150°C |
| Maximum Junction Temperature ..... | +175°C                          |

**Electrical Specifications** V<sub>CC</sub> = V<sub>C+</sub> = +15V, V<sub>EE</sub> = V<sub>C-</sub> = -15V, R<sub>S</sub> = 50Ω, R<sub>L</sub> = 100Ω, A<sub>V</sub> = +1, R<sub>F</sub> = 250Ω,  $\overline{OE}$  = 0.8V, TOI = 0.8V or 2.0V Unless Otherwise Specified.

| PARAMETER  | TEMP                                      | HA-5004-5, -9 |     |       | UNITS             |        |
|--|---|---------------|-----|-------|-------------------|--------|
|  |   | MIN           | TYP | MAX   |                   |        |
| <b>INPUT CHARACTERISTICS</b>                         |   |               |     |       |                   |        |
| Offset Voltage                                       | +25°C                                     | -             | 1   | 5     | mV                |        |
|  | Full                                      | -             | -   | 20    | mV                |        |
| Average Offset Voltage Drift                         | Full                                      | -             | 10  | -     | μV/°C             |        |
| Bias Current (+Input Only) (Note 2)                  | +25°C                                     | -             | 2   | 5     | μA                |        |
|  | Full                                      | -             | -   | 20    | μA                |        |
| Input Resistance (+Input Only) (Note 2)              | +25°C                                     | -             | 3   | -     | MΩ                |        |
| Input Capacitance                                    | +25°C                                     | -             | 3   | -     | pF                |        |
| Common Mode Range                                    | Full                                      | ±10           | -   | -     | V                 |        |
| <b>DISTORTION AND NOISE</b>                          |   |               |     |       |                   |        |
| Total Harmonic Distortion 2V <sub>p-p</sub> , 200kHz | A <sub>VCL</sub> = +1                     | -             | -72 | -     | dBc               |        |
|  | A <sub>VCL</sub> = +2                     | -             | -70 | -     | dBc               |        |
|  | A <sub>VCL</sub> = +5                     | -             | -68 | -     | dBc               |        |
| Input Noise Voltage 10Hz to 1MHz                     | +25°C                                     | -             | 15  | -     | μV <sub>p-p</sub> |        |
| Input Noise Voltage Density (Note 3)                 | f <sub>o</sub> = 10kHz                    | +25°C         | -   | 2.2   | nV/√Hz            |        |
|  | f <sub>o</sub> = 100kHz                   | +25°C         | -   | 2.2   | nV/√Hz            |        |
| Input Noise Current Density (Note 3)                 | f <sub>o</sub> = 10kHz                    | +25°C         | -   | 6     | pA/√Hz            |        |
|  | f <sub>o</sub> = 100kHz                   | +25°C         | -   | 4     | pA/√Hz            |        |
| <b>DIGITAL I/O CHARACTERISTICS</b>                   |   |               |     |       |                   |        |
| Logic Inputs (OE and TOI)                            | V <sub>IH</sub>                           | Full          | 2.0 | -     | V                 |        |
|  | V <sub>IL</sub>                           | Full          | -   | -     | 0.8               | V      |
|  | I <sub>IH</sub> @ V <sub>I</sub> = 2.4V   | Full          | -   | -     | 1                 | μA     |
|  | I <sub>IL</sub> @ V <sub>I</sub> = 0.4V   | Full          | -   | -     | 10                | μA     |
| Logic Output (TOL) (Open Collector)                  | V <sub>OL</sub> @ 800μA                   | Full          | -   | 0.05  | 0.4               | V      |
| <b>TRANSFER CHARACTERISTICS</b>                      |   |               |     |       |                   |        |
| DC Gain Error  | Small Signal (±100mV)                     | +25°C         | -   | 0.25  | 0.43              | %      |
|  |   | Full          | -   | 0.25  | 0.75              | %      |
|  | Large Signal (±10V) (R <sub>L</sub> = 1K) | +25°C         | -   | 0.25  | 0.43              | %      |
|  |   | Full          | -   | 0.25  | 0.75              | %      |
| DC Voltage Gain (Note 4)                             | +25°C                                     | 233           | 400 | -     | V/V               |        |
|  | Full                                      | 133           | 400 | -     | V/V               |        |
| DC Transimpedance (Note 5)                           | +25°C                                     | -             | 100 | -     | V/mA              |        |
|  | Full                                      | 33            | 100 | -     | V/mA              |        |
| -3dB Bandwidth A <sub>V</sub> = +1 (Note 6)          | +25°C                                     | -             | 100 | -     | MHz               |        |
| Gain Flatness  | DC to 5MHz                                | +25°C         | -   | 0.03  | -                 | dB     |
|  | DC to 10MHz                               | +25°C         | -   | 0.05  | -                 | dB     |
| Differential Gain (Notes 6, 7, 8) 3.58MHz            | A <sub>VCL</sub> = +1                     | +25°C         | -   | 0.035 | -                 | %      |
|  | A <sub>VCL</sub> = +2                     | +25°C         | -   | 0.058 | -                 | %      |
| Differential Gain (Notes 6, 7, 8) 4.43MHz            | A <sub>VCL</sub> = +1                     | +25°C         | -   | 0.035 | -                 | %      |
|  | A <sub>VCL</sub> = +2                     | +25°C         | -   | 0.058 | -                 | %      |
| Differential Phase (Note 6, 7) 3.58MHz               | A <sub>VCL</sub> = +1                     | +25°C         | -   | 0.15  | -                 | Degree |
|  | A <sub>VCL</sub> = +2                     | +25°C         | -   | 0.23  | -                 | Degree |
| Differential Phase (Note 6, 7) 4.43MHz               | A <sub>VCL</sub> = +1                     | +25°C         | -   | 0.17  | -                 | Degree |
|  | A <sub>VCL</sub> = +2                     | +25°C         | -   | 0.24  | -                 | Degree |
| Common Mode Rejection Ratio (Note 9)                 | Full                                      | -             | 58  | -     | dB                |        |
| Minimum Stable Gain                                  | Full                                      | 1             | -   | -     | V/V               |        |

## Specifications HA-5004

**Electrical Specifications (Continued)**  $V_{CC} = V_{C+} = +15V$ ,  $V_{EE} = V_{C-} = -15V$ ,  $R_S = 50\Omega$ ,  $R_L = 100\Omega$ ,  $A_V = +1$ ,  $R_F = 250\Omega$ ,  $\overline{OE} = 0.8V$ ,  $TOI = 0.8V$  or  $2.0V$  Unless Otherwise Specified.

| PARAMETER                                     | TEMP                  | HA-5004-5, -9 |       |       | UNITS |            |
|---|-----------------------|---------------|-------|-------|-------|------------|
|   |                       | MIN           | TYP   | MAX   |       |            |
| <b>OUTPUT CHARACTERISTICS</b>                 |                       |               |       |       |       |            |
| Output Voltage Swing                          | ( $R_L = 100\Omega$ ) | +25°C         | ±9.0  | ±9.5  | -     | V          |
|   | ( $R_L = 1k\Omega$ )  | +25°C         | ±11.5 | ±11.8 | -     | V          |
|   | ( $R_L = 100\Omega$ ) | Full          | ±8.0  | ±9.5  | -     | V          |
|   | ( $R_L = 1k\Omega$ )  | Full          | ±10.5 | ±11.8 | -     | V          |
| Full Power Bandwidth ( $A_V = +1$ ) (Note 10) |                       | +25°C         | -     | 100   | -     | MHz        |
| Output Resistance, Open Loop                  |                       | +25°C         | -     | 5     | -     | $\Omega$   |
| Output Current                                |                       | +25°C         | ±90   | ±100  | -     | mA         |
|   |                       | Full          | ±80   | ±100  | -     | mA         |
| Output Enable time (Hi Z to ±2V)              |                       | Full          | -     | 100   | -     | ns         |
| Output Disable time (±2V to Hi Z)             |                       | Full          | -     | 3     | -     | $\mu s$    |
| Output Leakage (Disabled)                     |                       | Full          | -     | -     | 1     | $\mu A$    |
| <b>TRANSIENT RESPONSE</b>                     |                       |               |       |       |       |            |
| Rise Time/Fall Time                           |                       | +25°C         | -     | 6.3   | -     | ns         |
| Propagation Delay (10V Step)                  |                       | +25°C         | -     | 7     | -     | ns         |
| Slew Rate                                     |                       | +25°C         | -     | 1200  | -     | V/ $\mu s$ |
| Settling Time (0.1%, 10V Step)                |                       | +25°C         | -     | 50    | -     | ns         |
| Overshoot                                     |                       | +25°C         | -     | 10    | -     | %          |
| <b>POWER SUPPLY CHARACTERISTICS</b>           |                       |               |       |       |       |            |
| Supply Current                                | (Enabled)             | +25°C         | -     | 12    | 16    | mA         |
|   |                       | Full          | -     | -     | 22    | mA         |
|   | (Disabled)            | +25°C         | -     | 7     | -     | mA         |
| Power Supply Rejection Ratio                  |                       | Full          | 50    | 60    | -     | dB         |

NOTES: 1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

2. Inverting (FB) input is a low impedance point; Bias Current, Offset Current, and Input Resistance are not specified for this terminal.

3. See typical performance curves.

4. DC Voltage Gain =  $\frac{1}{\text{Gain Error}}$

5. DC Transimpedance =  $\frac{R_F}{\text{Gain Error}}$ ,  $R_F = 250\Omega$

6.  $V_{IN} = 300mV_{p-p}$

7.  $V_{OFFSET} = 1.0V$

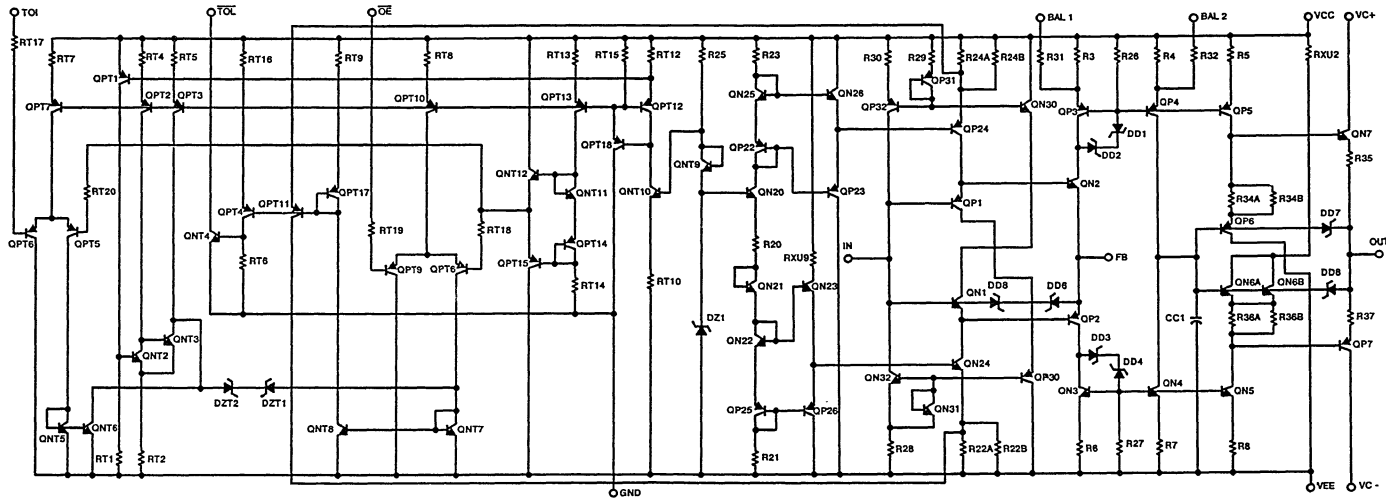
8. Differential Gain (dB) = 0.0869 Differential Gain (%)

9.  $V_{CM} = \pm 10V$

10. Full power bandwidth guaranteed by equation: Full Power Bandwidth =  $\frac{\text{Slew Rate}}{2\pi V_{peak}}$ ,  $V_{peak} = 2V$

Schematic

HA-5004

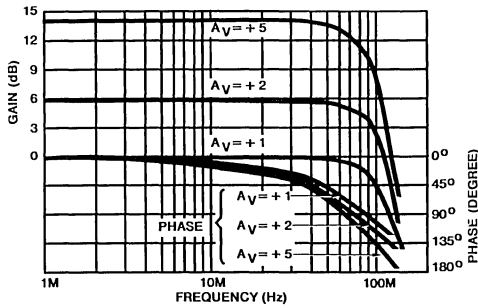


3-364

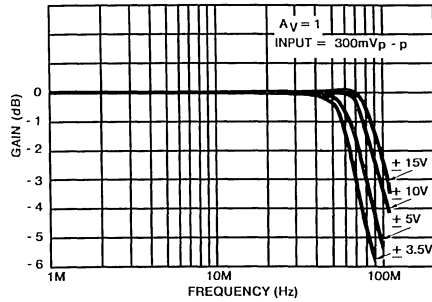
# HA-5004

**Typical Performance Curves**  $V_{SUPPLY} = \pm 15V$ ,  $T_A = 25^\circ C$ , Unless Otherwise Specified.

**GAIN AND PHASE vs. FREQUENCY**

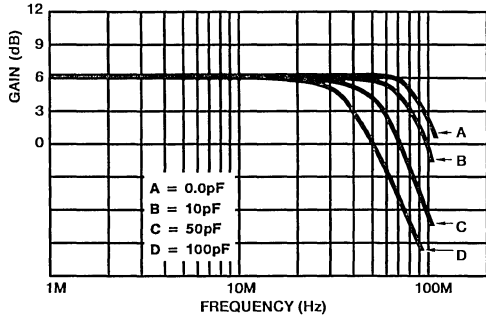


**FREQUENCY RESPONSE vs. SUPPLY VOLTAGE**



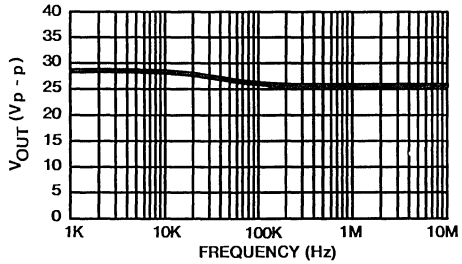
**FREQUENCY RESPONSE vs.  $C_L$**

$V_{CC} = \pm 15V$ ,  $A_V = +2$ ,  $R_L = 1k\Omega$ , Input = 10mV

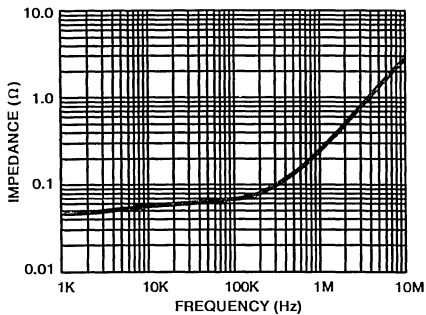


**MAX. UNDISTORTED SINEWAVE OUTPUT vs. FREQUENCY**

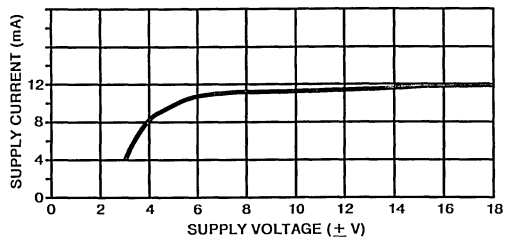
$V_{CC} = \pm 15V$ ,  $A_V = +1$ , Sinewave Input



**CLOSED LOOP OUTPUT IMPEDANCE vs. FREQUENCY**



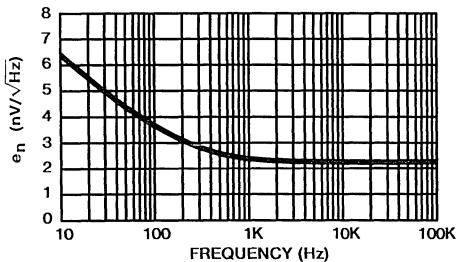
**SUPPLY CURRENT vs. SUPPLY VOLTAGE**



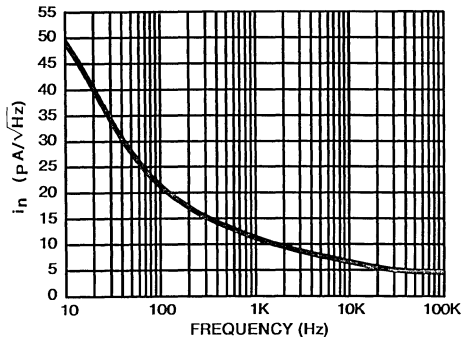
**3**  
OPERATIONAL  
AMPLIFIERS



**Typical Performance Curves (Continued)**  $V_{SUPPLY} = \pm 15V$ ,  $T_A = 25^\circ C$ , Unless Otherwise Specified.  
**VOLTAGE NOISE vs. FREQUENCY**  $V_{CC} = \pm 15V$

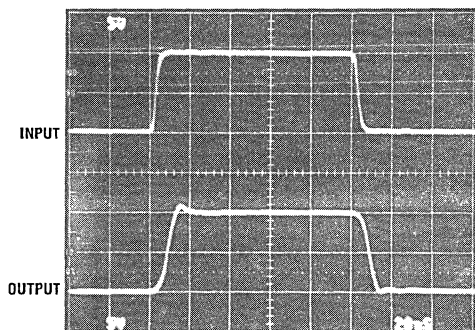


**CURRENT NOISE vs. FREQUENCY**  $V_{CC} = \pm 15V$



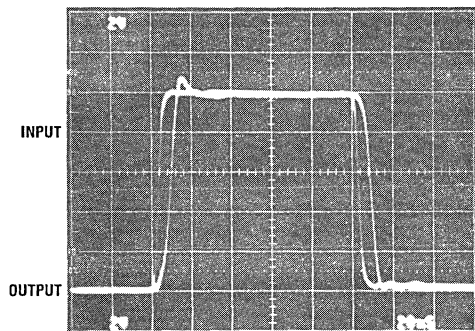
**Switching Waveforms**

**LARGE SIGNAL RESPONSE,  $A_v = +1$**   
 Vertical Scale: 5V/Div.  
 Horizontal Scale: 20ns/Div.



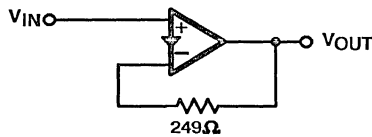
$A_v = +1$ ,  $V_{SUPPLY} = \pm 15V$

**PROPAGATION DELAY**  
 Vertical Scale: 2V/Div.  
 Horizontal Scale: 20ns/Div.

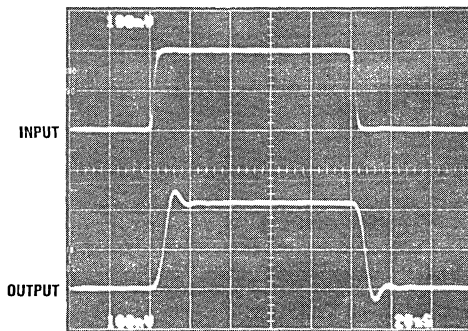


$A_v = +1$ ,  $V_{SUPPLY} = \pm 15V$

**TEST CIRCUIT**



**SMALL SIGNAL RESPONSE**  
 Vertical Scale: 100mV/Div.  
 Horizontal Scale: 20ns/Div.



$A_v = +1$ ,  $V_{SUPPLY} = \pm 15V$

**Applications Information**

**Theory of Operation**

The HA-5004 is a high performance amplifier that uses current feedback to achieve its outstanding performance. Although it is externally configured like an ordinary op amp in most applications, its internal operation is significantly different.

Inside the HA-5004, there is a unity gain buffer from the non-inverting (+) input to the inverting (FB) input (as suggested by the circuit symbol), and the inverting terminal is a low impedance point. Error currents are sensed at the inverting input and amplified; a small change in input current produces a large change in output voltage. The ratio of output voltage delta due to input current delta is the transimpedance of the device.

Steady state current at the inverting input is very small because the transimpedance is large. The voltage across the input terminals is nearly zero due to the buffer amplifier. These two properties are similar to standard op amps and likewise simplify circuit analysis.

**Resistor Selection**

The HA-5004 is optimized for a feedback resistor of 250Ω, regardless of gain configuration. It is important to note that this resistor is required even for unity gain applications; higher gain settings use a second resistor like regular op amp circuits as shown in Figure 1 below.

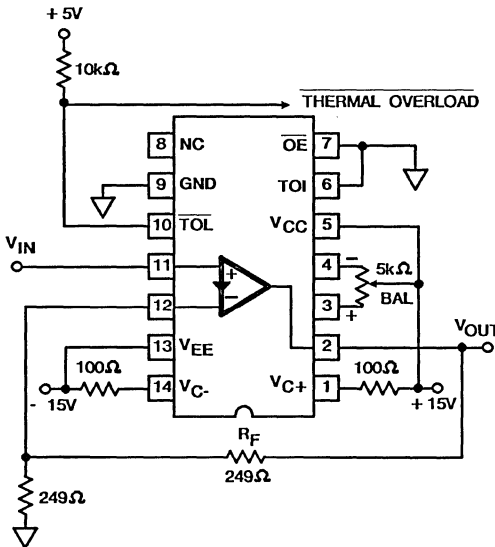


FIGURE 1: TYPICAL APPLICATION CIRCUIT,  $A_V = +2$

**Power Supplies**

The HA-5004 will operate over a wide range of supply voltages with excellent performance. Supplies may be either single-ended or split, ranging from 6V ( $\pm 3V$ ) to 36V ( $\pm 18V$ ). Appropriate reduction in input and output signal excursion is necessary for operation at lower supply voltages. Bypass capacitors from each supply to ground are recommended, typically a 0.01μF ceramic in parallel with a 4.7μF electrolytic.

**Current Limit**

No internal current limiting is provided for the HA-5004 in order to maximize bandwidth and slew rate. However, power is supplied separately to the output stage via pins 1 ( $V_{C+}$ ) and 14 ( $V_{C-}$ ) so that external current limiting resistors may be used. If required, 100Ω resistors to each supply rail are recommended.

**Enable/Disable and Thermal Overload Operation**

The HA-5004 operates normally with a TTL low state on pin 7 ( $\overline{OE}$ ) but it may be disabled manually by a TTL high state at this input. When disabled, the output and inverting (FB) input go to a high impedance state and the circuit is electrically debiased, reducing supply current by about 5mA. It is important to keep the differential input voltage below the absolute maximum rating of 5V when the device is disabled.

If the power dissipation becomes excessive and chip temperature exceeds approximately 180°C, the HA-5004 will automatically disable itself. The thermal overload condition will be indicated by a low state at the  $\overline{TOL}$  output on pin 10. ( $\overline{TOL}$  is also low for manual shutdown via pin 7). Automatic thermal shutdown can be bypassed by a TTL high state on Thermal Overload Inhibit (TOI) pin 6. See the truth table for a summary of operation.

**Offset Adjustment**

Offset voltage may be nulled with a 5KΩ potentiometer between pins 3 and 4, center tapped to the positive supply. Setting the slider towards pin 3 (+BAL) increases output voltage; towards pin 4 (-BAL) decreases output voltage. Offset can be adjusted by about  $\pm 10mV$  with a 5K pot; this range is extended with a lower resistance potentiometer.

**Die Characteristics**

|                           |   |               |
|---------------------------|---|---------------|
| Transistor Count .....    | 64  |               |
| Die Dimensions .....      | 93 x 63 x 19mils<br>(2370 x 1600 x 480μm) |               |
| Substrate Potential ..... | $V_{EE}$                                  |               |
| Process .....             | Bipolar DI                                |               |
| Thermal Constants (°C/W)  | $\theta_{ja}$                             | $\theta_{jc}$ |
| HA1-Ceramic DIP           | 107                                       | 25            |

August 1991

### Features

- Wide Unity Gain Bandwidth ..... 100MHz
- Slew Rate ..... 800V/ $\mu$ s
- Output Current .....  $\pm 30$ mA (Min)
- Drives ..... 3.5V into 75 $\Omega$
- Differential Gain ..... <0.02%
- Differential Phase ..... <0.03%
- Low Voltage Noise ..... 4.5nV/ $\sqrt{\text{Hz}}$
- Low Supply Current ..... 10mA (Max)
- Wide Supply Range .....  $\pm 5$ V to  $\pm 15$ V
- Output Enable/Disable
- High Performance Replacement for EL2020

### Description

The HA-5020 is a wide bandwidth, high slew rate amplifier optimized for video applications and gains between 1 and 10. Manufactured on Harris' Reduced Feature Complementary Bipolar DI process, this amplifier uses current mode feedback to maintain higher bandwidth at a given gain than conventional voltage feedback amplifiers. Since it is a closed loop device, the HA-5020 offers better gain accuracy and lower distortion than open loop buffers.

The HA-5020 features low differential gain and phase and will drive two double terminated 75 $\Omega$  coax cables to video levels with low distortion. Adding a gain flatness performance of 0.1dB makes this amplifier ideal for demanding video applications. The bandwidth and slew rate of the HA-5020 are relatively independent of closed loop gain. The 100MHz unity gain bandwidth only decreases to 60MHz at a gain of 10. The HA-5020 used in place of a conventional op amp will yield a significant improvement in

### Applications

- Unity Gain Video/Wideband Buffer
- Video Gain Block
- Video Distribution Amp/Coax Cable Driver
- Flash A/D Driver
- Waveform Generator Output Driver
- Current to Voltage Converter; D/A Output Buffer
- Radar Systems
- Imaging Systems

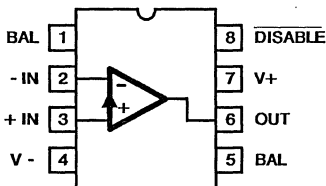
the speed power product. To further reduce power, the HA-5020 has a disable function which significantly reduces supply current, while forcing the output to a true high impedance state. This allows the outputs of multiple amplifiers to be wire-OR'd into multiplexer configurations. The device also includes output short circuit protection and output offset voltage adjustment.

The HA-5020 offers significant enhancements over competing amplifiers, such as the EL2020. Improvements include unity gain bandwidth, slew rate, video performance, lower supply current, and superior DC specifications.

The HA-5020 is available in commercial and industrial temperature ranges, and a choice of packages. See the "Ordering Information" section below for more information. For military grade product, please refer to the HA-5020/883 data sheet.

### Pinout

HA3-5020 (PLASTIC DIP)  
HA9P5020 (SOIC)  
TOP VIEW



### Ordering Information

| PART NUMBER | TEMPERATURE RANGE | PACKAGE           |
|-------------|-------------------|-------------------|
| HA3-5020-5  | 0°C to +75°C      | 8 Pin Plastic DIP |
| HA9P5020-5  | 0°C to +75°C      | 8 Pin SOIC        |
| HA3-5020-9  | -40°C to +85°C    | 8 Pin Plastic DIP |

## Specifications HA-5020

### Absolute Maximum Ratings (Note 1)

|   |              |
|---|--------------|
| Voltage Between V+ and V- Terminals             | 36V          |
| Common Mode Voltage                             | $V_{SUPPLY}$ |
| Differential Input Voltage                      | $\pm 10V$    |
| Output Current Short Circuit                    | Protected    |
| Maximum Junction Temperature (Note 19)          | +175°C       |
| Maximum Junction Temperature (Plastic Packages) | +150°C       |

### Operating Temperature Range

|                                 |  |               |
|---------------------------------|--|---------------|
| HA-5020-5                       | $0^{\circ}C \leq T_A \leq +75^{\circ}C$    |               |
| HA-5020-9                       | $-40^{\circ}C \leq T_A \leq +85^{\circ}C$  |               |
| Storage Temperature Range       | $-65^{\circ}C \leq T_A \leq +150^{\circ}C$ |               |
| Thermal Package Characteristics | $\theta_{jc}$                              | $\theta_{ja}$ |
| 8 Pin Plastic DIP               | 32   | 94            |
| Pin SOIC                        | 43   | 161           |

### Electrical Specifications $V_+ = +15V, V_- = -15V, R_F = 1k\Omega, A_V = +1, R_L = 400\Omega, C_L \leq 10pF$ , Unless Otherwise Specified.

| PARAMETER                                      | TEMP           | HA-5020-5, -9 |            |      | UNITS             |
|--|----------------|---------------|------------|------|-------------------|
|  |                | MIN           | TYP        | MAX  |                   |
| <b>INPUT CHARACTERISTICS</b>                   |                |               |            |      |                   |
| Input Offset Voltage (Note 2)                  | +25°C          | -             | 2          | 8    | mV                |
|  | Full           | -             | -          | 10   | mV                |
| Average Input Offset Voltage Drift             | Full           | -             | 20         | -    | $\mu V/^{\circ}C$ |
| $V_{IO}$ Common Mode Rejection Ratio (Note 3)  | Full           | 50            | 58         | -    | dB                |
| $V_{IO}$ Power Supply Rejection Ratio (Note 4) | +25°C          | 64            | -          | -    | dB                |
|  | Full           | 60            | -          | -    | dB                |
| Non-Inverting Input (+IN) Current              | +25°C          | -             | 3          | 8    | $\mu A$           |
|  | Full           | -             | -          | 20   | $\mu A$           |
| +IN Common Mode Rejection (Note 3)             | Full           | -             | -          | 0.5  | $\mu A/V$         |
| +IN Power Supply Rejection (Note 4)            | +25°C          | -             | -          | 0.06 | $\mu A/V$         |
|  | Full           | -             | -          | 0.2  | $\mu A/V$         |
| Inverting Input (-IN) Current                  | +25°C          | -             | 12         | 20   | $\mu A$           |
|  | Full           | -             | 25         | 50   | $\mu A$           |
| -IN Common Mode Rejection (Note 3)             | +25°C          | -             | -          | 0.4  | $\mu A/V$         |
|  | Full           | -             | -          | 0.5  | $\mu A/V$         |
| -IN Power Supply Rejection (Note 4)            | +25°C          | -             | -          | 0.2  | $\mu A/V$         |
|  | Full           | -             | -          | 0.5  | $\mu A/V$         |
| <b>TRANSFER CHARACTERISTICS</b>                |                |               |            |      |                   |
| Transimpedance                                 | +25°C          | 3500          | -          | -    | V/mA              |
|  | Full           | 1000          | -          | -    | V/mA              |
| Open Loop DC Voltage Gain                      | +25°C          | 70            | -          | -    | dB                |
| $R_L = 400\Omega, V_{OUT} = \pm 10V$           | Full           | 65            | -          | -    | dB                |
| Open Loop DC Voltage Gain                      | +25°C          | 60            | -          | -    | dB                |
| $R_L = 100\Omega, V_{OUT} = \pm 2.5V$          | Full           | 55            | -          | -    | dB                |
| <b>OUTPUT CHARACTERISTICS</b>                  |                |               |            |      |                   |
| Output Voltage Swing                           | +25°C to +85°C | $\pm 12$      | $\pm 12.7$ | -    | V                 |
|  | -40°C to 0°C   | $\pm 11$      | $\pm 11.8$ | -    | V                 |
| Output Current                                 | +25°C          | $\pm 30$      | $\pm 31.7$ | -    | mA                |
| (Guaranteed by Output Voltage Test)            | Full           | $\pm 27.5$    | -          | -    | mA                |
| <b>POWER SUPPLY CHARACTERISTICS</b>            |                |               |            |      |                   |
| Quiescent Supply Current                       | Full           | -             | 7.5        | 10   | mA                |
| Supply Current, Disabled (Note 5)              | Full           | -             | 5          | 7.5  | mA                |
| Disable Pin Input Current (Note 5)             | Full           | -             | 1.0        | 1.5  | mA                |
| Minimum Pin 8 Current to Disable (Note 6)      | Full           | 350           | -          | -    | $\mu A$           |
| Maximum Pin 8 Current to Enable (Note 7)       | Full           | -             | -          | 20   | $\mu A$           |

## Specifications HA-5020

**Electrical Specifications (Continued)**  $V_+ = +15V$ ,  $V_- = -15V$ ,  $R_F = 1k\Omega$ ,  $A_V = +1$ ,  $R_L = 400\Omega$ ,  $C_L \leq 10pF$ ,  
Unless Otherwise Specified.

| PARAMETER  | TEMP  | HA-5020-5, -9 |          |     | UNITS          |
|--|-------|---------------|----------|-----|----------------|
|  |       | MIN           | TYP      | MAX |                |
| <b>A.C. CHARACTERISTICS (<math>A_V = +1</math>)</b>                                |       |               |          |     |                |
| Slew Rate (Note 8)   | +25°C | 600           | 800      | -   | V/ $\mu$ s     |
|  | Full  | 500           | 700      | -   | V/ $\mu$ s     |
| Full Power Bandwidth (Note 9)<br>(Guaranteed by Slew Rate Test)                    | +25°C | 9.6           | 12.7     | -   | MHz            |
|  | Full  | 8.0           | 11.1     | -   | MHz            |
| Rise Time (Note 10)  | +25°C | -             | 5        | -   | ns             |
| Fall Time (Note 10)  | +25°C | -             | 5        | -   | ns             |
| Propagation Delay (Note 10)  | +25°C | -             | 6        | -   | ns             |
| 3-dB Bandwidth (Note 11)   | +25°C | -             | 100      | -   | MHz            |
| Settling Time to 1%, 10V Output Step   | +25°C | -             | 45       | -   | ns             |
| Settling Time to 0.25%, 10V Output Step  | +25°C | -             | 100      | -   | ns             |
| <b>A.C. CHARACTERISTICS (<math>A_V = +10</math>, <math>R_F = 383\Omega</math>)</b> |       |               |          |     |                |
| Slew Rate (Notes 8, 12)  | +25°C | 900           | 1100     | -   | V/ $\mu$ s     |
|  | Full  | 750           | -        | -   | V/ $\mu$ s     |
| Full Power Bandwidth (Note 9)<br>(Guaranteed by Slew Rate Test)                    | +25°C | 14.3          | 17.5     | -   | MHz            |
|  | Full  | 11.9          | -        | -   | MHz            |
| Rise Time (Note 10)  | +25°C | -             | 8        | -   | ns             |
| Fall Time (Note 10)  | +25°C | -             | 8        | -   | ns             |
| Propagation Delay (Note 10)  | +25°C | -             | 9        | -   | ns             |
| 3-dB Bandwidth (Note 11)   | +25°C | -             | 60       | -   | MHz            |
| Settling Time to 1%, 10V Output Step   | +25°C | -             | 55       | -   | ns             |
| Settling Time to 0.25%, 10V Output Step  | +25°C | -             | 90       | -   | ns             |
| <b>HARRIS VALUE ADDED SPECIFICATIONS</b>   |       |               |          |     |                |
| Input Noise Voltage ( $f = 1kHz$ )   | +25°C | -             | 4.5      | -   | $nV/\sqrt{Hz}$ |
| +Input Noise Current ( $f = 1kHz$ )  | +25°C | -             | 2.5      | -   | $pA/\sqrt{Hz}$ |
| -Input Noise Current ( $f = 1kHz$ )  | +25°C | -             | 25       | -   | $pA/\sqrt{Hz}$ |
| Input Common Mode Range  | Full  | $\pm 10$      | $\pm 12$ | -   | V              |
| -Ibias Adjust Range (Note 2)   | Full  | $\pm 25$      | $\pm 40$ | -   | $\mu A$        |
| Overshoot  | +25°C | -             | 30       | -   | %              |
| Output Current (Short Circuit, Note 13)  | Full  | $\pm 50$      | $\pm 65$ | -   | mA             |
| Output Current (Disabled, Notes 5, 14)   | Full  | -             | -        | 1   | $\mu A$        |
| Output Disable Time (Note 15)  | +25°C | -             | 10       | -   | $\mu s$        |
| Output Enable Time (Note 16)   | +25°C | -             | 1        | -   | $\mu s$        |
| Supply Voltage Range   | +25°C | 5             | -        | 15  | V              |
| Output Capacitance (Disabled, Notes 5,17)  | +25°C | -             | 15       | -   | pF             |
| <b>VIDEO CHARACTERISTICS</b>   |       |               |          |     |                |
| Differential Gain (Note 18)  | +25°C | -             | 0.02     | -   | %              |
| Differential Phase (Note 18)   | +25°C | -             | 0.03     | -   | Degrees        |
| Gain Flatness to 5MHz  | +25°C | -             | 0.1      | -   | dB             |
| Chrominance to Luminance Gain (Note 18)  | +25°C | -             | 0.02     | -   | dB             |
| Chrominance to Luminance Delay (Note 18)   | +25°C | -             | 0.3      | -   | ns             |

## HA-5020

### NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the servability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The inverting input current (-I<sub>bias</sub>) can be adjusted with an external 10kΩ pot between pins 1 and 5, wiper connected to V+. Since -I<sub>bias</sub> flows through the feedback resistor (R<sub>F</sub>), the result is an adjustment in offset voltage. The amount of offset voltage adjustment is determined by the value of R<sub>F</sub> ( $\Delta V_{OS} = \Delta I_{bias} \cdot R_F$ ).
3. V<sub>CM</sub> = ±10V.
4.  $\pm 4.5V \leq V_S \leq \pm 18V$ .
5. Disable = 0V.
6. R<sub>L</sub> = 100Ω, V<sub>IN</sub> = 10V. This is the minimum current which must be pulled out of the Disable pin in order to disable the output. The output is considered disabled when  $-10mV \leq V_{OUT} \leq +10mV$ .
7. V<sub>IN</sub> = 0V. This is the maximum current that can be pulled out of the Disable pin with the HA-5020 remaining enabled. The HA-5020 is considered disabled when the supply current has decreased by at least 0.5mA.
8. V<sub>OUT</sub> switches from -10V to +10V, or from +10V to -10V. Specification is from the 25% to 75% points.
9.  $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$ ; V<sub>PEAK</sub> = 10V.
10. R<sub>L</sub> = 100Ω, V<sub>OUT</sub> = 1V. Measured from 10% to 90% points for rise/fall times; from 50% points of input and output for propagation delay.
11. R<sub>L</sub> = 400Ω, V<sub>OUT</sub> = 100mV.
12. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
13. V<sub>IN</sub> = ±10V, V<sub>OUT</sub> = 0V.
14. V<sub>OUT</sub> = ±10V.
15. V<sub>IN</sub> = +10V, Disable = +15V to 0V. Measured from the 50% point of Disable to V<sub>OUT</sub> = 0V.
16. V<sub>IN</sub> = +10V, Disable = 0V to +15V. Measured from the 50% point of Disable to V<sub>OUT</sub> = 10V.
17. V<sub>IN</sub> = 0V, Force V<sub>OUT</sub> from 0V to ±10V, t<sub>r</sub>/t<sub>f</sub> = 50ns.
18. Measured with a VM700A video tester using a NTC-7 composite VITS.
19. Maximum power dissipation, including output load, must be designed to maintain junction temperature below +175°C for ceramic packages, and below +150°C for plastic packages.

August 1991

**Video Buffer**

### Features

- Differential Phase Error ..... 0.1 Degree
- Differential Gain Error ..... 0.1%
- High Slew Rate ..... 1300V/ $\mu$ s
- Wide Bandwidth (Small Signal) ..... 250MHz
- Wide Power Bandwidth ..... DC to 65MHz
- Fast Rise Time ..... 3ns
- High Output Drive .....  $\pm 8V$  With 100 $\Omega$  Load
- Wide Power Supply Range .....  $\pm 5V$  to  $\pm 16V$
- Replace Costly Hybrids

### Applications

- Video Buffer
- High Frequency Buffer
- Isolation Buffer
- High Speed Line Driver
- Impedance Matching
- Current Boosters
- High Speed A/D Input Buffers
- For Further Application Ideas, See App. Note 548

### Description

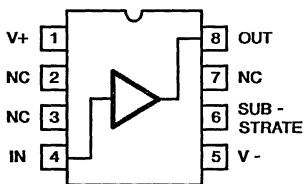
The HA-5033 is a unity gain monolithic I.C. designed for any application requiring a fast, wideband buffer. Featuring a bandwidth of 250MHz and outstanding differential phase/gain characteristics, this high performance voltage follower is an excellent choice for video circuit design. Other features, which include a minimum slew rate of 1000V/ $\mu$ s and high output drive capability, make the HA-5033 applicable for line driver and high speed data conversion circuits.

The high performance of this product is a result of the Harris Dielectric Isolation process. A major feature of this process is that it produces both PNP and NPN high frequency transistors which makes wide bandwidth designs, such as the HA-5033, practical. Alternative process methods typically produce a lower AC performance.

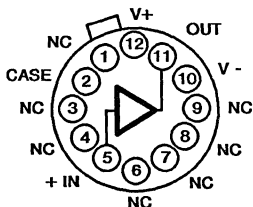
The HA-5033 is available in a 12 pin (TO-8) Metal Can or in 8 pin Plastic Mini-DIP and SOIC packages.

### Pinouts

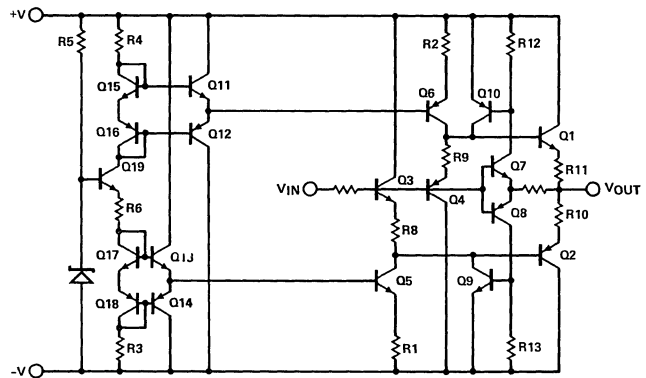
HA3-5033-5 (PLASTIC MINI-DIP)  
HA9P5033-5/-9 (SOIC)  
TOP VIEW



HA2-5033-2/-5 (TO-8 METAL CAN)  
TOP VIEW



### Schematic



## Specifications HA-5033

### Absolute Maximum Ratings (Note 1)

|  |                   |
|--|-------------------|
| Voltage Between V+ and V- Pins               | 40V               |
| Input Voltage                                | Equal to Supplies |
| Output Current (Peak) (50ms On/1 Second Off) | ±200mA            |
| Internal Power Dissipation (Note 2)          |                   |
| TO-8 (+25°C)                                 | 1.75W             |
| Mini-DIP (+25°C)                             | 1.95W             |

### Operating Temperature Ranges

|   |                                 |
|---|---------------------------------|
| HA-5033-2                                       | -55°C ≤ T <sub>A</sub> ≤ +125°C |
| HA-5033-5                                       | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| HA-5033-9                                       | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| Storage Temperature Range                       | -65°C ≤ T <sub>A</sub> ≤ +150°C |
| Maximum Junction Temperature                    | +175°C                          |
| Maximum Junction Temperature (Plastic Packages) | +150°C                          |

**Electrical Specifications** V<sub>SUPPLY</sub> = ±12V, R<sub>S</sub> = 50Ω, R<sub>L</sub> = 100Ω, C<sub>L</sub> = 10pF, Unless Otherwise Specified.

| PARAMETER                           | TEMP                          | HA-5033-2 |      |      | HA-5033-5 |      |      | NOTE 10<br>HA-5033-9 | UNITS  |
|-------------------------------------|-------------------------------|-----------|------|------|-----------|------|------|----------------------|--------|
|                                     |                               | MIN       | TYP  | MAX  | MIN       | TYP  | MAX  | MAX                  |        |
| <b>INPUT CHARACTERISTICS</b>        |                               |           |      |      |           |      |      |                      |        |
| Offset Voltage                      | +25°C                         | -         | 5    | 15   | -         | 5    | 15   | 15                   | mV     |
|                                     | Full                          | -         | 6    | 25   | -         | 6    | 25   | 30                   | mV     |
| Average Offset Voltage Drift        | Full                          | -         | 33   | -    | -         | 33   | -    | -                    | μV/°C  |
| Bias Current                        | +25°C                         | -         | 20   | 35   | -         | 20   | 35   | 35                   | μA     |
|                                     | Full                          | -         | 30   | 50   | -         | 30   | 50   | 50                   | μA     |
| Input Resistance                    | +25°C                         | -         | 1.5  | -    | -         | 1.5  | -    | -                    | MΩ     |
| Input Capacitance                   | +25°C                         | -         | 1.6  | -    | -         | 1.6  | -    | -                    | pF     |
| Input Noise Voltage (Note 3)        | +25°C                         | -         | 20   | -    | -         | 20   | -    | -                    | μVp-p  |
| <b>TRANSFER CHARACTERISTICS</b>     |                               |           |      |      |           |      |      |                      |        |
| Voltage Gain                        | R <sub>L</sub> = 100Ω         | +25°C     | 0.93 | -    | -         | 0.93 | -    | -                    | V/V    |
|                                     | R <sub>L</sub> = 1kΩ          | +25°C     | 0.93 | 0.99 | -         | 0.93 | 0.99 | -                    | V/V    |
| -3dB Bandwidth                      | R <sub>L</sub> = 100Ω         | Full      | 0.92 | -    | -         | 0.92 | -    | -                    | V/V    |
|                                     | +25°C                         | -         | 250  | -    | -         | 250  | -    | -                    | MHz    |
| <b>OUTPUT CHARACTERISTICS</b>       |                               |           |      |      |           |      |      |                      |        |
| Output Voltage Swing                | R <sub>L</sub> = 100Ω         | Full      | ±8   | ±10  | -         | ±8   | ±10  | -                    | V      |
|                                     | R <sub>L</sub> = 1kΩ (Note 4) | Full      | ±11  | ±12  | -         | ±11  | ±12  | -                    | V      |
| Output Current                      | +25°C                         | ±80       | ±100 | -    | ±80       | ±100 | -    | -                    | mA     |
| Output Resistance                   | +25°C                         | -         | 5    | -    | -         | 5    | -    | -                    | Ω      |
| Full Power Bandwidth (Note 5)       | +25°C                         | -         | 146  | -    | -         | 146  | -    | -                    | MHz    |
|                                     | (Note 7)                      | +25°C     | 15.9 | -    | -         | 15.9 | -    | -                    | MHz    |
| <b>TRANSIENT RESPONSE</b>           |                               |           |      |      |           |      |      |                      |        |
| Rise Time (Note 6)                  | +25°C                         | -         | 3    | -    | -         | 3    | -    | -                    | ns     |
| Propagation Delay                   | +25°C                         | -         | 1    | -    | -         | 1    | -    | -                    | ns     |
| Overshoot                           | +25°C                         | -         | 10   | -    | -         | 10   | -    | -                    | %      |
| Slew Rate (Note 7)                  | +25°C                         | 1         | 1.3  | -    | 1         | 1.3  | -    | -                    | V/ns   |
| Settling Time to 0.1%               | +25°C                         | -         | 50   | -    | -         | 50   | -    | -                    | ns     |
| Differential Phase Error (Note 8)   | +25°C                         | -         | 0.1  | -    | -         | 0.1  | -    | -                    | Degree |
| Differential Gain Error (Note 8)    | +25°C                         | -         | 0.1  | -    | -         | 0.1  | -    | -                    | %      |
| <b>POWER SUPPLY CHARACTERISTICS</b> |                               |           |      |      |           |      |      |                      |        |
| Supply Current                      | +25°C                         | -         | 21   | 25   | -         | 21   | 25   | 25                   | mA     |
|                                     | Full                          | -         | 21   | 30   | -         | 21   | 30   | 30                   | mA     |
| Power Supply Rejection Ratio        | Full                          | 54        | -    | -    | 54        | -    | -    | -                    | dB     |
| Harmonic Distortion (Note 9)        | +25°C                         | -         | <0.1 | -    | -         | <0.1 | -    | -                    | %      |

#### NOTES:

- Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
- TO-8: θ<sub>ja</sub> = 101°C/W, θ<sub>jc</sub> = 33°C/W Recommended heat sinks for the TO-8: Thermalloy 2240A, θ<sub>sa</sub> = 27°C/W, IERC Up-TO-8-48CB, θ<sub>sa</sub> = 10°C/W. Mini-DIP: θ<sub>ja</sub> = 91°C/W, θ<sub>sa</sub> = 40°C/W.
- 10Hz to 1MHz
- ±V<sub>SUPPLY</sub> = ±15V
- V<sub>OUT</sub> = 1V<sub>RMS</sub>, R<sub>L</sub> = 1kΩ
- V<sub>OUT</sub> = 500mV
- ±V<sub>SUPPLY</sub> = ±15V, V<sub>OUT</sub> = ±10V, R<sub>L</sub> = 1kΩ.
- Differential gain and phase error are non-linear signal distortions found in video systems and are defined as follows: Differential gain error is defined as the change in amplitude at the color subcarrier frequency as the picture signal is varied from blanking to white level. Differential phase error is defined as the change in the phase of the color subcarrier as the picture signal is varied from blanking to white level. Differential gain and phase error were too small to be measured with a Tektronix 520A NTSC Vector Scope.
- V<sub>IN</sub> = 1V<sub>RMS</sub>
- Typical and minimum specification for the -9 version are the same as those for the -5 version.

3  
OPERATIONAL  
AMPLIFIERS



## Operating Instructions

### Layout Considerations

The wide bandwidth of the HA-5033 necessitates that high frequency circuit layout procedures be followed. Failure to follow these guidelines can result in marginal performance.

Probably the most crucial of the RF/video layout rules is the use of a ground plane. A ground plane provides isolation and minimizes distributed circuit capacitance and inductance which will degrade high frequency performance. This ground plane shielding can also incorporate the metal case of the HA-5033 since pin #2 is internally tied to the package. This feature allows the user to make metal to metal contact between the ground plane and the package, which extends shielding, provides additional heat sinking and eliminates the use of a socket, IC sockets contribute inter-lead capacitance which limits device bandwidth and should be avoided.

For the plastic Mini-DIP, pin 6 can be tied to either supply, grounded, or simply not used. But to optimize device

performance and improve isolation, it is recommended that this pin be grounded.

Other considerations are proper power supply bypassing and keeping the input and output connections as short as possible which minimizes distributed capacitance and reduces board space.

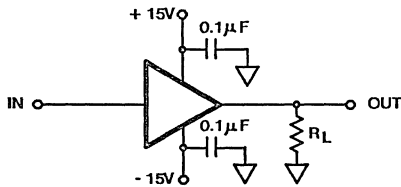
### Power Supply Decoupling

For optimum device performance, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from 0.01 to 0.1  $\mu\text{F}$  will minimize high frequency variations in supply voltage. Solid tantalum capacitors 1  $\mu\text{F}$  or larger will optimize low frequency performance.

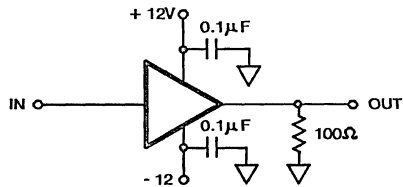
It is also recommended that the bypass capacitors be connected close to the HA-5033 (preferably directly to the supply pins).

## Test Circuits

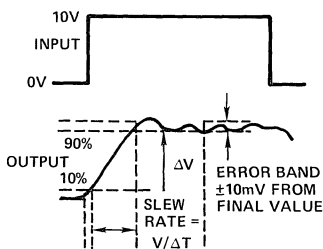
SLEW RATE AND SETTLING TIME



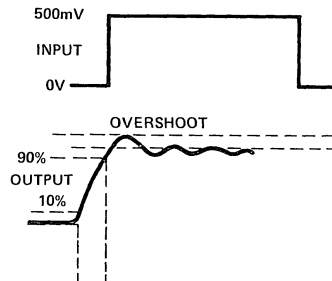
TRANSIENT RESPONSE



SETTLING TIME



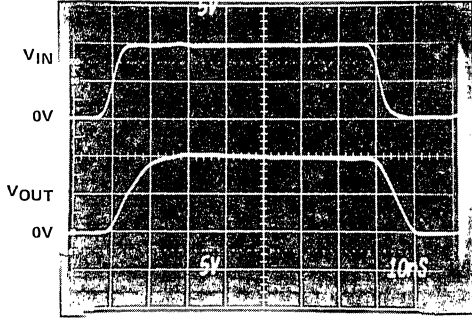
RISE TIME



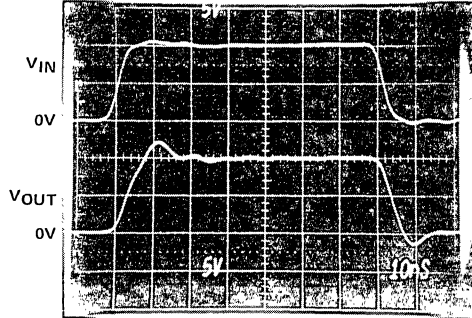
NOTE: Measured on both positive and negative transitions.

Test Circuits (Continued)

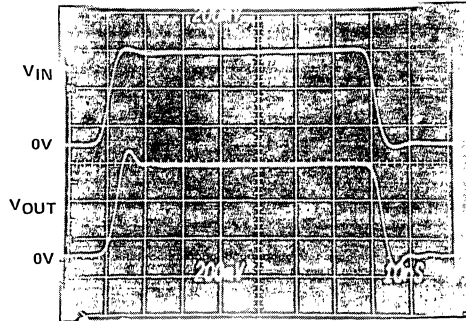
**+10V RESPONSE**  
 $T_A = +25^\circ\text{C}$ ,  $R_S = 50\Omega$ ,  $R_L = 100\Omega$



**+10V RESPONSE**  
 $T_A = +25^\circ\text{C}$ ,  $R_S = 50\Omega$ ,  $R_L = 1\text{k}\Omega$



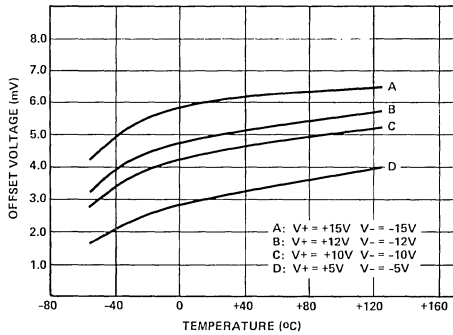
**+0.5V PULSE RESPONSE**  
 $T_A = +25^\circ\text{C}$ ,  $R_S = 50\Omega$ ,  $R_L = 100\Omega$



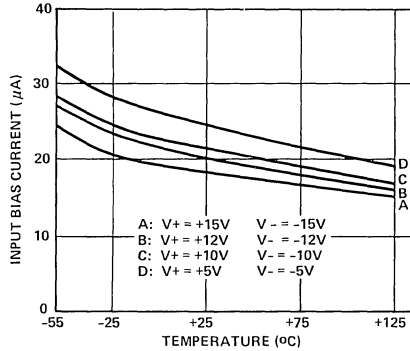
  
 OPERATIONAL AMPLIFIERS

Typical Performance Curves

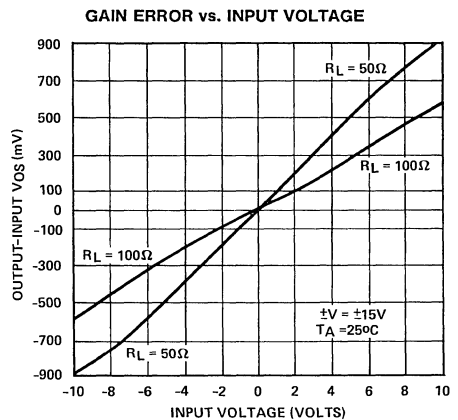
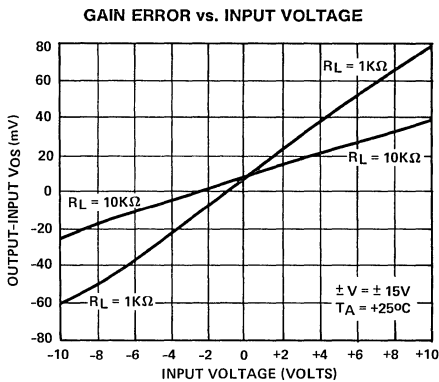
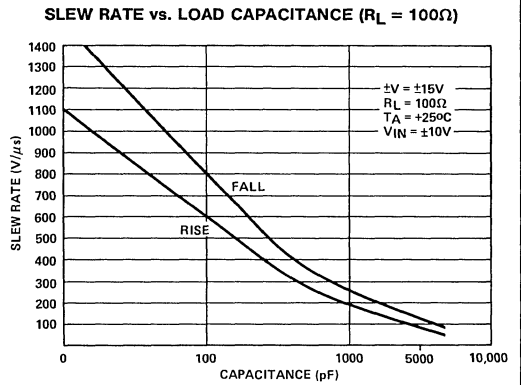
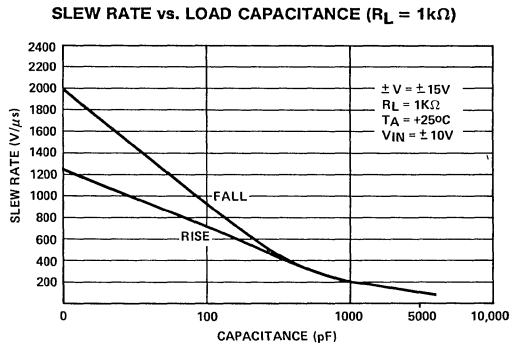
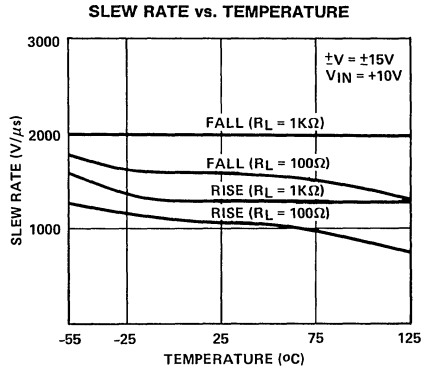
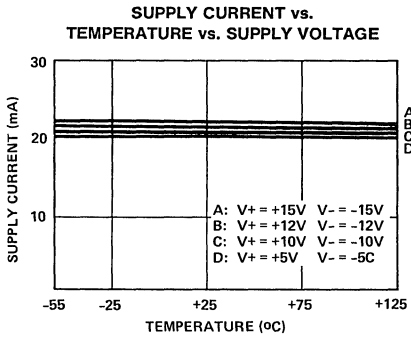
INPUT OFFSET VOLTAGE vs.  
 TEMPERATURE vs. SUPPLY VOLTAGE



INPUT BIAS CURRENT vs.  
 TEMPERATURE vs. SUPPLY VOLTAGE

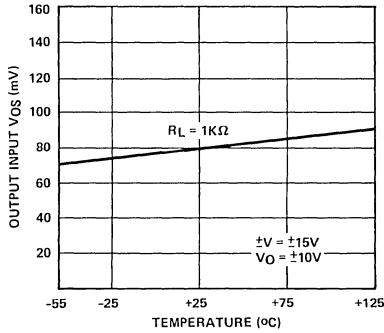


Typical Performance Curves (Continued)

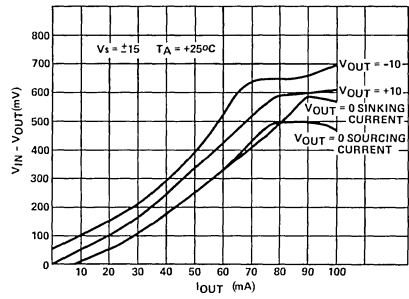


Typical Performance Curves (Continued)

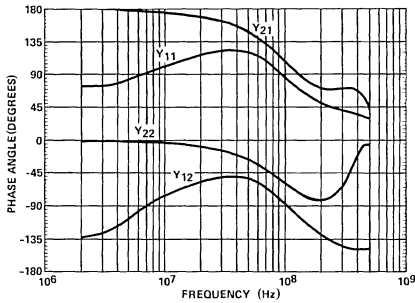
GAIN ERROR vs. TEMPERATURE



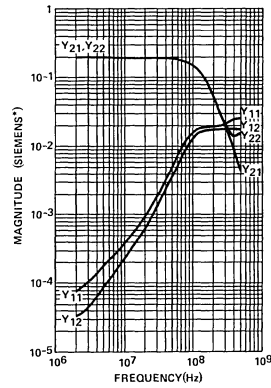
$V_{IN} - V_{OUT}$  vs.  $I_{OUT}$



Y - PARAMETERS PHASE vs. FREQUENCY

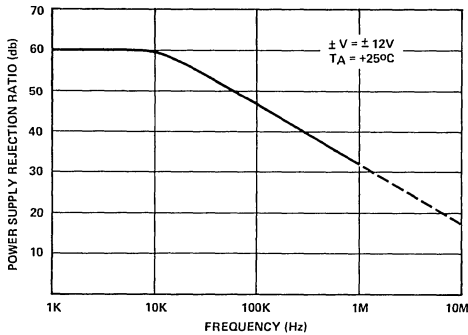


Y - PARAMETER MAGNITUDE vs. FREQUENCY

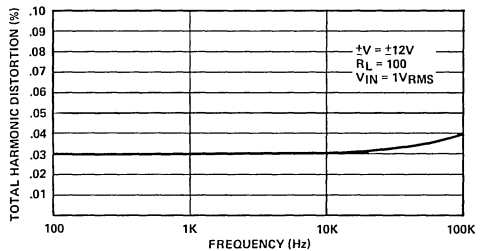


\* Siemens =  $\Omega^{-1}$

POWER SUPPLY REJECTION RATIO vs. FREQUENCY



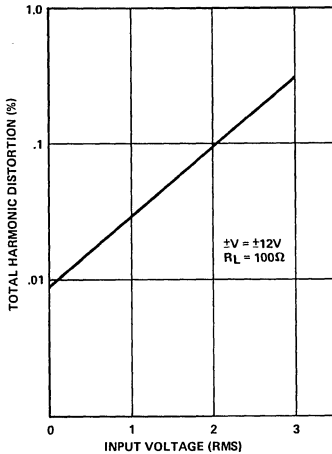
TOTAL HARMONIC DISTORTION vs. FREQUENCY



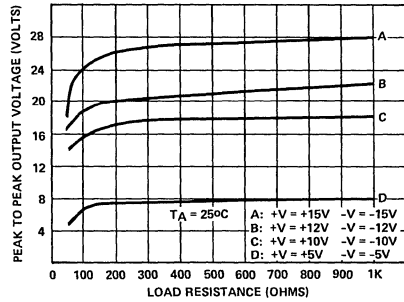
# HA-5033

## Typical Performance Curves (Continued)

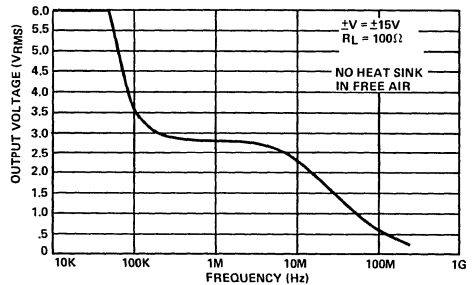
TOTAL HARMONIC DISTORTION vs. RMS INPUT VOLTAGE



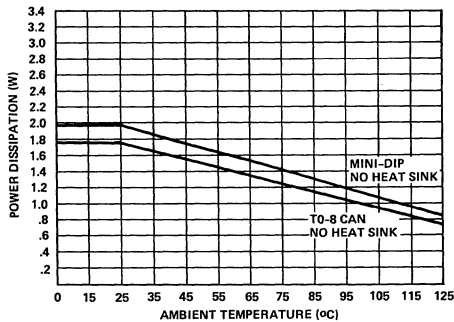
OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE vs. SUPPLY VOLTAGE



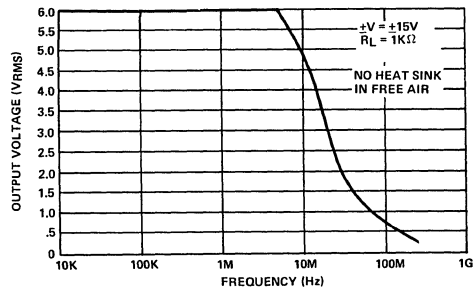
OUTPUT SWING vs. FREQUENCY\*



MAXIMUM POWER DISSIPATION vs. AMBIENT TEMPERATURE



OUTPUT SWING vs. FREQUENCY\*



\* This curve was obtained by noting the output voltage necessary to produce an observable distortion for a given frequency. If higher distortion is acceptable, then a higher output voltage for a given frequency can be obtained.

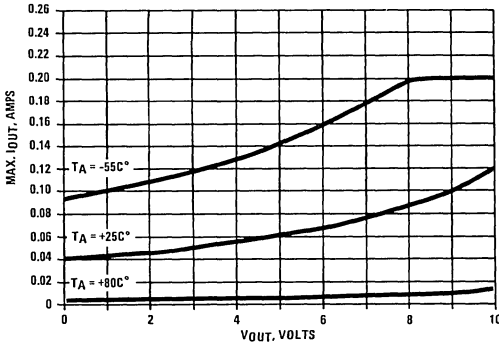
However, operating the HA-5033 with increased distortion (to the right of curve shown), will also be accompanied by an increase in supply current. The resulting increase in chip temperature must be considered and heat sinking will be necessary to prevent thermal runaway.

This characteristic is the result of the output transistor operation. If the signal amplitude or signal frequency or both are increased beyond the curve shown, the NPN, PNP output transistors will approach a condition of being simultaneously on. Under this condition, thermal runaway can occur.

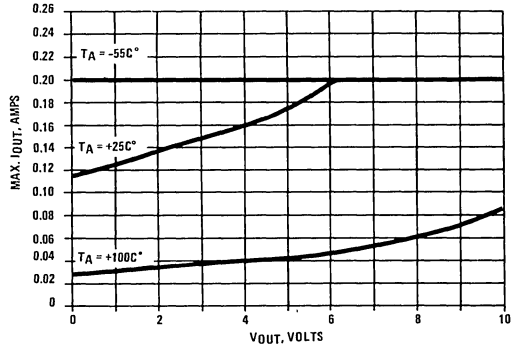
# HA-5033

## Typical Performance Curves (Continued)

HA-5033 SOA, TO-8, NO SINK  
 $T_J = +175, I_{CC} = 30\text{mA}, V_{CC} = \pm 15, \theta_{ja} = 101^\circ\text{C/W}$

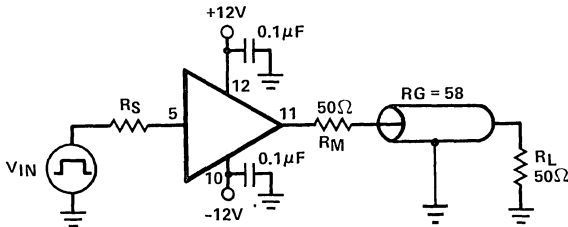


HA-5033, TO-8, AAVID 5792  $\theta_{sa} = 25^\circ\text{C/W}$   
 $T_J = +175, I_{CC} = 30\text{mA}, V_{CC} = \pm 15, \theta_{jc} = 33^\circ\text{C/W}$



## Typical Applications (Also See Application Note 548)

### VIDEO COAXIAL LINE DRIVER - 50V SYSTEM

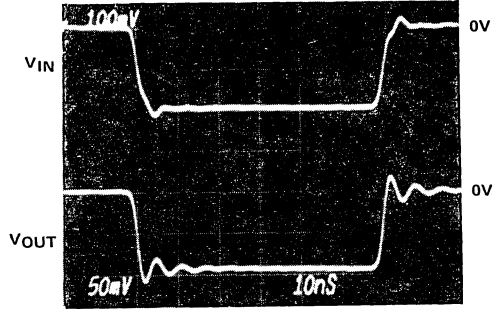
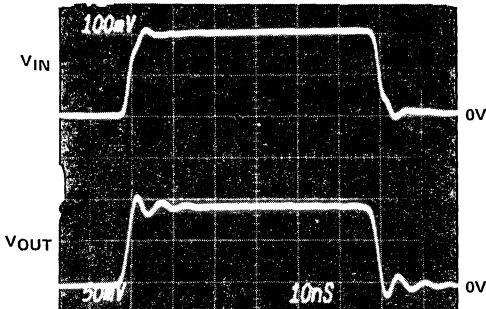


**POSITIVE PULSE RESPONSE**  
 $T_A = +25^\circ\text{C}, R_S = 50\Omega, R_M = R_L = 50\Omega$   

$$V_O = V_{IN} \left( \frac{R_L}{R_L + R_M} \right) = \frac{1}{2} V_{IN}$$

**NEGATIVE PULSE RESPONSE**  
 $T_A = +25^\circ\text{C}, R_S = 50\Omega, R_M = R_L = 50\Omega$   

$$V_O = V_{IN} \left( \frac{R_L}{R_L + R_M} \right) = \frac{1}{2} V_{IN}$$

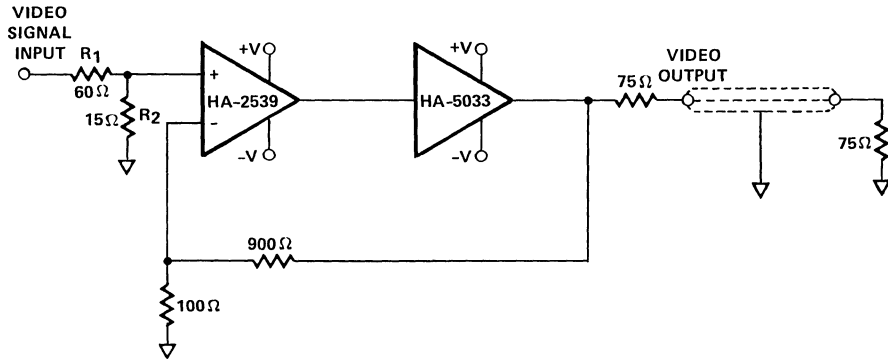


3  
OPERATIONAL AMPLIFIERS

# HA-5033

## Typical Applications (Continued)

### VIDEO GAIN BLOCK



### Die Characteristics

|                            |   |
|----------------------------|---|
| Transistor Count .....     | 20  |
| Die Dimensions .....       | 50 x 66 x 19mils<br>(1270 x 1660 x 480μm) |
| Substrate Potential* ..... | V-  |
| Process .....              | High Frequency Bipolar-DI                 |
| Passivation .....          | Nitride                                   |

\*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.



HARRIS

# HA-5101/5111

## Low Noise, High Performance Operational Amplifiers

August 1991

### Features

- Low Noise ..... 3.3nV/ $\sqrt{\text{Hz}}$  at 1kHz
- Wide Bandwidth ..... 10MHz (Compensated)  
100MHz (Uncompensated)
- High Slew Rate ..... 10V/ $\mu\text{s}$  (Compensated)  
50V/ $\mu\text{s}$  (Uncompensated)
- Low Offset Voltage Drift ..... 3 $\mu\text{V}/^\circ\text{C}$
- High Gain ..... 1 x 10<sup>6</sup>V/V
- High CMRR/PSRR ..... 100dB
- High Output Drive Capability ..... 30mA

### Description

The HA-5101/5111 are dielectrically isolated operational amplifiers featuring low noise and high performance. Both amplifiers have an excellent noise voltage density of 3.3nV/ $\sqrt{\text{Hz}}$  at 1kHz. The uncompensated HA-5111 is stable at a minimum gain of 10 and has the same DC specifications as the unity gain stable HA-5101. The difference in compensation yields a 100MHz gain-bandwidth product and a 50V/ $\mu\text{s}$  slew rate for the HA-5111 versus a 10MHz unity gain bandwidth and a 10V/ $\mu\text{s}$  slew rate for the HA-5101.

DC characteristics of the HA-5101/5111 assure accurate performance. The 0.5mV offset voltage is externally adjustable and offset voltage drift is just 3 $\mu\text{V}/^\circ\text{C}$ . An offset current of only 30nA reduces input current errors and an open loop voltage gain of 1 x 10<sup>6</sup>V/V increases loop gain for low distortion amplification.

### Applications

- High Quality Audio Preamplifiers
- High Q Active Filters
- Low Noise Function Generators
- Low Distortion Oscillators
- Low Noise Comparators
- For Further Design Ideas, See App. Note 554

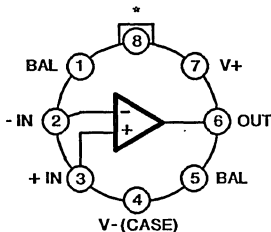
The HA-5101/5111 are ideal for audio applications, especially low-level signal amplifiers such as microphone, tape head and phono cartridge preamplifiers. Additionally, it is well suited for low distortion oscillators, low noise function generators and high Q filters.

The HA-5101/5111-2 has guaranteed operation from -55 $^\circ\text{C}$  to +125 $^\circ\text{C}$  and can be ordered as a military grade part. The HA-5101/5111-5 has guaranteed operation from 0 $^\circ\text{C}$  to +75 $^\circ\text{C}$ . All devices are available in Ceramic Mini-DIP and TO-99 Can packages. Additionally, the HA-5101/5111-5 is available in a Plastic Mini-DIP package.

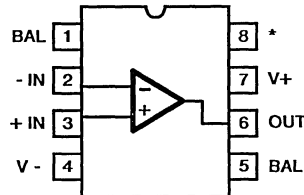
These devices are also available in SOIC packages in both -5 and -9 temperature grades.

### Pinouts

HA2-5101/5111 (TO-99 METAL CAN)  
TOP VIEW



HA3-5101/5111 (PLASTIC MINI-DIP)  
HA7-5101/5111 (CERAMIC MINI-DIP)  
HA9P5101/5111 (SOIC)  
TOP VIEW



\*HA-5101 No Connect  
HA-5111 Compensation

3  
OPERATIONAL AMPLIFIERS



## Specifications HA-5101/5111

### Absolute Maximum Ratings (Note 1)

|   |                               |
|---|-------------------------------|
| $T_A = +25^\circ\text{C}$ Unless Otherwise Stated |                               |
| Voltage Between V+ and V- Terminals               | 40.0V                         |
| Differential Input Voltage                        | $\pm 7\text{V}$               |
| Voltage (at any pin)                              | $\pm V_{\text{SUPPLY}}$       |
| Output Current                                    | Full Short Circuit Protection |
| Junction Temperature                              | $+175^\circ\text{C}$          |

### Operating Temperature

|  |   |
|--|---|
| HA-5101/5111-2   | $-55^\circ\text{C}$ to $+125^\circ\text{C}$ |
| HA-5101/5111-5   | $0^\circ\text{C}$ to $+75^\circ\text{C}$    |
| HA-5101/5111-9   | $-40^\circ\text{C}$ to $+85^\circ\text{C}$  |
| Storage Temperature  | $-65^\circ\text{C}$ to $+150^\circ\text{C}$ |
| Internal Power Dissipation   | 560mW                                       |
| (Derate at 5.3mW/ $^\circ\text{C}$ Above $70^\circ\text{C}$ Ambient) |   |

### Electrical Specifications $V_+ = +15\text{V}$ , $V_- = -15\text{V}$ , $R_S = 100\Omega$ , $R_L = 2\text{k}\Omega$ , $C_L = 50\text{pF}$ , Unless Otherwise Specified.

| PARAMETER  | TEMP                | HA-5101-2, -5<br>HA-5111-2, -5 |          |     | HA-5101-9<br>HA-5111-9 |          |     | UNITS                        |
|--|---------------------|--------------------------------|----------|-----|------------------------|----------|-----|------------------------------|
|  |                     | MIN                            | TYP      | MAX | MIN                    | TYP      | MAX |                              |
| <b>INPUT CHARACTERISTICS</b>   |                     |                                |          |     |                        |          |     |                              |
| Offset Voltage   | $+25^\circ\text{C}$ | -                              | 0.5      | 3   | -                      | 0.5      | 3   | mV                           |
|  | Full                | -                              | -        | 4   | -                      | -        | 4   | mV                           |
| Offset Voltage Drift   | Full                | -                              | 3        | -   | -                      | 3        | -   | $\mu\text{V}/^\circ\text{C}$ |
| Bias Current   | $+25^\circ\text{C}$ | -                              | 100      | 200 | -                      | 100      | 200 | nA                           |
|  | Full                | -                              | -        | 325 | -                      | -        | 325 | nA                           |
| Offset Current   | $+25^\circ\text{C}$ | -                              | 30       | 75  | -                      | 30       | 75  | nA                           |
|  | Full                | -                              | -        | 125 | -                      | -        | 125 | nA                           |
| Input Resistance   | $+25^\circ\text{C}$ | -                              | 500      | -   | -                      | 500      | -   | $\text{k}\Omega$             |
| Common Mode Range  | Full                | $\pm 12$                       | -        | -   | $\pm 12$               | -        | -   | V                            |
| <b>TRANSFER CHARACTERISTICS</b>  |                     |                                |          |     |                        |          |     |                              |
| Large Signal Voltage Gain (Note 2)   | $+25^\circ\text{C}$ | -                              | 1000K    | -   | -                      | 1000K    | -   | V/V                          |
|  | Full                | 100K                           | 250K     | -   | 100K                   | 250K     | -   | V/V                          |
| Common Mode Rejection Ratio (Note 3)   | Full                | 80                             | 100      | -   | 80                     | 100      | -   | dB                           |
| Small Signal Bandwidth<br>HA-5101 ( $A_V = 1$ )  | $+25^\circ\text{C}$ | -                              | 10       | -   | -                      | 10       | -   | MHz                          |
| Minimum Stable Gain  | Full                | 1                              | -        | -   | 1                      | -        | -   | V/V                          |
|  | Full                | 10                             | -        | -   | 10                     | -        | -   | V/V                          |
| Gain Bandwidth Product HA-5111 ( $A_V = 10$ )  | $+25^\circ\text{C}$ | -                              | 100      | -   | -                      | 100      | -   | MHz                          |
| <b>OUTPUT CHARACTERISTICS</b>  |                     |                                |          |     |                        |          |     |                              |
| Output Voltage Swing<br>$R_L = 10\text{K}$<br>$R_L = 2\text{K}$<br>( $V_{PS} = \pm 18$ , $R_L = 600$ ) | Full                | $\pm 12$                       | $\pm 13$ | -   | $\pm 12$               | $\pm 13$ | -   | V                            |
|  | Full                | $\pm 12$                       | $\pm 13$ | -   | $\pm 12$               | $\pm 13$ | -   | V                            |
|  | $+25^\circ\text{C}$ | $\pm 15$                       | -        | -   | $\pm 15$               | -        | -   | V                            |
| Output Current (Note 4)  | $+25^\circ\text{C}$ | 25                             | 30       | -   | 25                     | 30       | -   | mA                           |
| Full Power Bandwidth (Note 5)  | $+25^\circ\text{C}$ | 95                             | 160      | -   | 95                     | 160      | -   | kHz                          |
|  | $+25^\circ\text{C}$ | 630                            | 790      | -   | 630                    | 790      | -   | kHz                          |
| Output Resistance  | $+25^\circ\text{C}$ | -                              | 110      | -   | -                      | 110      | -   | $\Omega$                     |
| Maximum Load Capacitance   | $+25^\circ\text{C}$ | -                              | 800      | -   | -                      | 800      | -   | pF                           |

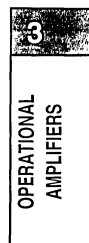
## Specifications HA-5101/5111

**Electrical Specifications (Continued)**  $V_+ = 15V$ ,  $V_- = -15V$ ,  $R_S = 100$ ,  $R_L = 2K$ ,  $C_L = 50pF$   
Unless Otherwise Specified.

| PARAMETER                               | TEMP  | HA-5101-2, -5<br>HA-5111-2, -5 |       |     | HA-5101-9<br>HA-5111-9 |       |     | UNITS  |
|---|-------|--------------------------------|-------|-----|------------------------|-------|-----|--------|
|   |       | MIN                            | TYP   | MAX | MIN                    | TYP   | MAX |        |
| <b>TRANSIENT RESPONSE (Note 6)</b>      |       |                                |       |     |                        |       |     |        |
| Rise Time                               |       |                                |       |     |                        |       |     |        |
| HA-5101                                 | +25°C | -                              | 50    | 100 | -                      | 50    | 100 | ns     |
| HA-5111                                 | +25°C | -                              | 30    | 60  | -                      | 30    | 60  | ns     |
| Overshoot                               |       |                                |       |     |                        |       |     |        |
| HA-5101                                 | +25°C | -                              | 20    | 35  | -                      | 20    | 35  | %      |
| HA-5111                                 | +25°C | -                              | 20    | 40  | -                      | 20    | 40  | %      |
| Slew Rate                               |       |                                |       |     |                        |       |     |        |
| HA-5101                                 | +25°C | 6                              | 10    | -   | 6                      | 10    | -   | V/μs   |
| HA-5111                                 | +25°C | 40                             | 50    | -   | 40                     | 50    | -   | V/μs   |
| Settling Time (Note 7)                  |       |                                |       |     |                        |       |     |        |
| HA-5101 0.01%                           | -     | -                              | 2.6   | -   | -                      | 2.6   | -   | μs     |
| HA-5111 0.01%                           | -     | -                              | 0.5   | -   | -                      | 0.5   | -   | μs     |
| <b>NOISE CHARACTERISTICS (Note 8)</b>   |       |                                |       |     |                        |       |     |        |
| Input Noise Voltage                     |       |                                |       |     |                        |       |     |        |
| f = 10Hz                                | +25°C | -                              | 7     | 17  | -                      | 7     | 17  | nV/√Hz |
| f = 1kHz                                | +25°C | -                              | 3.3   | 4.5 | -                      | 3.3   | 4.5 | nV/√Hz |
| Input Noise Current                     |       |                                |       |     |                        |       |     |        |
| f = 10Hz                                | +25°C | -                              | 5.1   | 28  | -                      | 5.1   | 28  | pA/√Hz |
| f = 1kHz                                | +25°C | -                              | 1.1   | 3   | -                      | 1.1   | 3   | pA/√Hz |
| Broadband Noise Voltage f = DC to 30kHz | +25°C | -                              | 0.870 | -   | -                      | 0.870 | -   | μVrms  |
| <b>POWER SUPPLY CHARACTERISTICS</b>     |       |                                |       |     |                        |       |     |        |
| Supply Current HA-5101/5111             | Full  | -                              | 4     | 6   | -                      | 4     | 7   | mA     |
| Power Supply Rejection Ratio (Note 9)   | Full  | 80                             | 100   | -   | 80                     | 100   | -   | dB     |

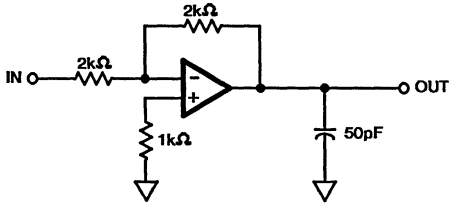
**NOTES:**

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2.  $V_{OUT} = \pm 10V$ ,  $R_L = 2K$ .
3.  $V_{CM} = \pm 10V$ .
4. Output current is measured with  $V_{OUT} = \pm 15V$  with  $V_{SUPPLY} = \pm 18V$ .
5. Full power bandwidth is guaranteed by equation:  
Full power bandwidth =  $\frac{\text{Slew Rate}}{2\pi V_{Peak}}$ ,  $V_{Peak} = 10V$ .
6. Refer to Test Circuits section of the data sheet.
7. Settling time is measured to 0.01% of final value for a 10V output step, and  $A_V = -10$  for HA-5111 and 0.01% of final value for a 10V output step,  $A_V = -1$  for HA-5101.
8. Sample Tested.
9. Delta  $V_{SUPPLY} = \pm 5V$ .

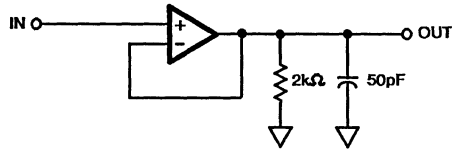


**Test Circuits**

**HA-5101 LARGE SIGNAL RESPONSE CIRCUIT**

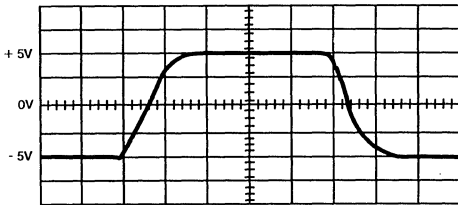


**HA-5101 SMALL SIGNAL RESPONSE CIRCUIT**



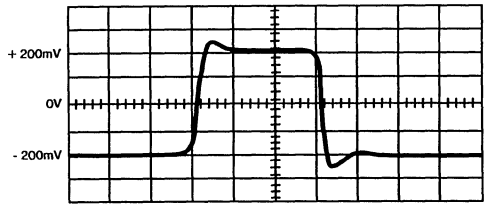
**HA-5111 LARGE SIGNAL TRANSIENT RESPONSE**

Ch. 1 = 2.5V/Div.  
Timebase = 200ns/Div.



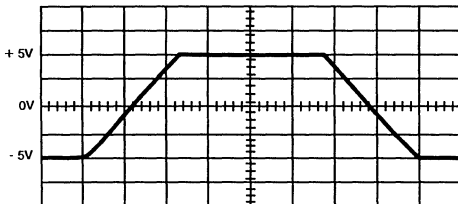
**HA-5111 SMALL SIGNAL TRANSIENT RESPONSE**

Ch. 1 = 100mV/Div.  
Timebase = 100ns/Div.



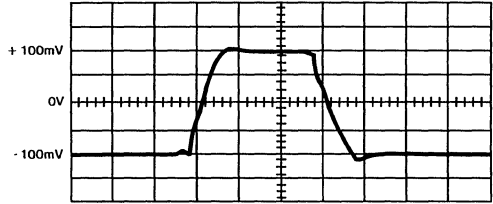
**HA-5101 LARGE SIGNAL TRANSIENT RESPONSE**

Ch. 1 = 2.5V/Div.  
Timebase = 1.00μs/Div.

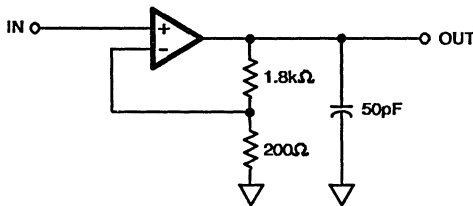


**HA-5101 SMALL SIGNAL TRANSIENT RESPONSE**

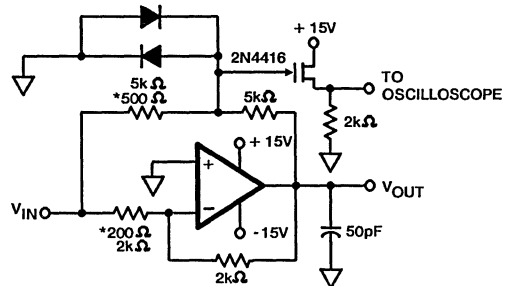
Ch. 1 = 50mV/Div.  
Timebase = 100ns/Div.



**HA-5111 LARGE AND SMALL SIGNAL RESPONSE CIRCUIT**



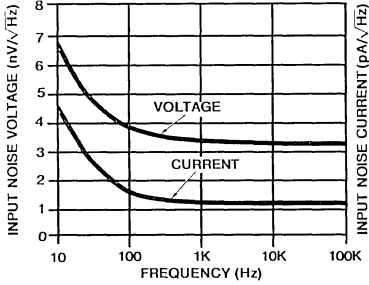
**SETTLING TIME CIRCUIT**



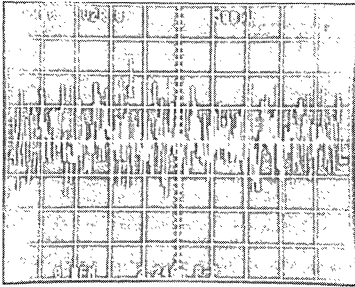
- $A_V = -1$  (HA-5101),  $*A_V = -10$  (HA-5111)
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional, HP5082-2810 recommended.

Typical Performance Curves

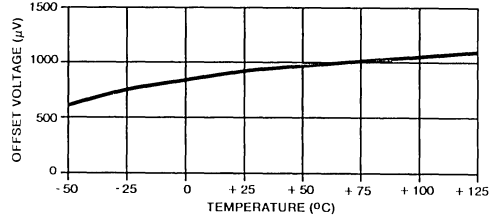
HA-5101/11 NOISE SPECTRUM



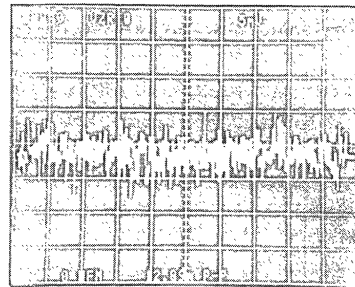
PEAK-TO-PEAK NOISE 0.1Hz to 10Hz  
 $A_V = 25000$ ,  $V_{CC} = \pm 15V$   
 (2.25 $\mu$ Vp-p RTO)



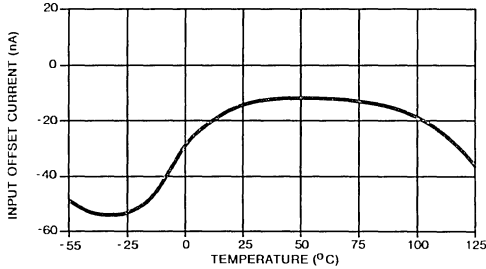
OFFSET VOLTAGE vs. TEMPERATURE



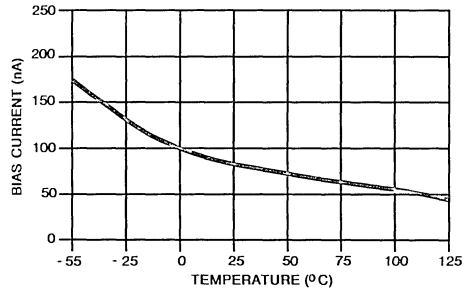
PEAK-TO-PEAK TOTAL NOISE 0.1Hz to 1MHz  
 $A_V = 25000$ ,  $V_{CC} = \pm 15V$   
 (12.89mVp-p RTO)



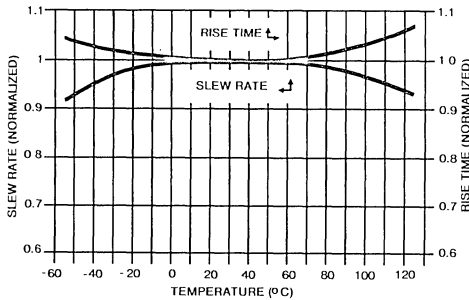
INPUT OFFSET CURRENT vs. TEMPERATURE



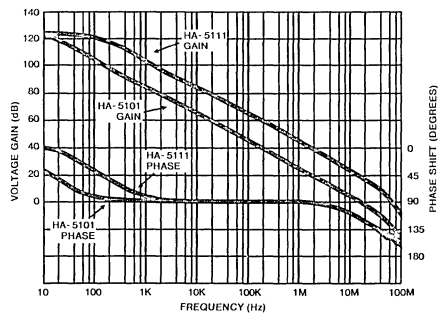
INPUT BIAS CURRENT vs. TEMPERATURE



SLEW RATE/RISE TIME vs. TEMPERATURE  
 $R_L = 2K$ ,  $C_L = 50pF$ ,  $V_{CC} = \pm 15V$



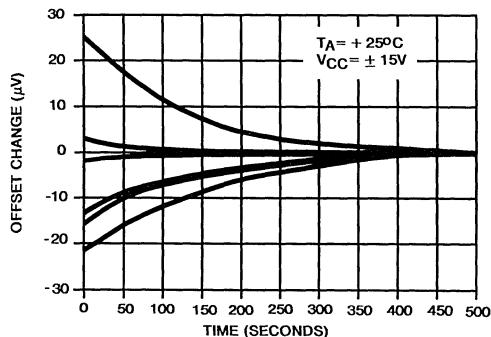
OPEN-LOOP GAIN/PHASE VS. FREQUENCY



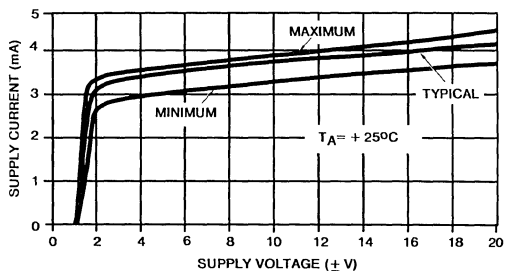
  
 OPERATIONAL AMPLIFIERS

**Typical Performance Curves (Continued)**

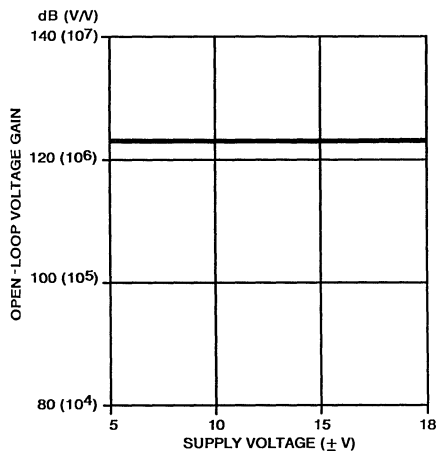
**INPUT OFFSET WARMUP DRIFT vs. TIME**  
(Normalized To Zero Final Value)  
(Six Representative Units)



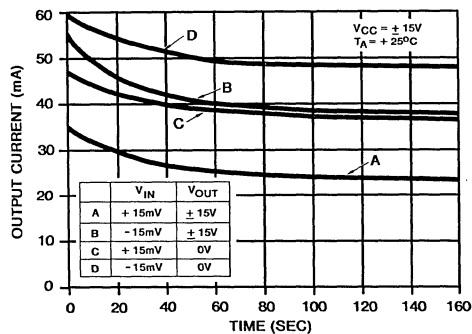
**SUPPLY CURRENT vs. SUPPLY VOLTAGE**



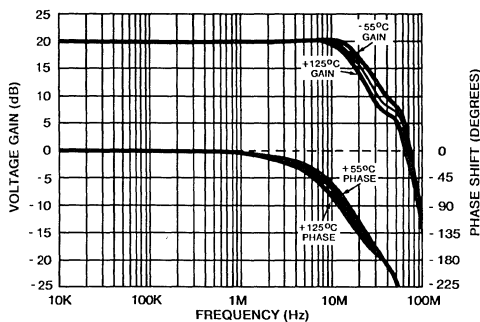
**DC OPEN-LOOP VOLTAGE GAIN vs. SUPPLY VOLTAGE**



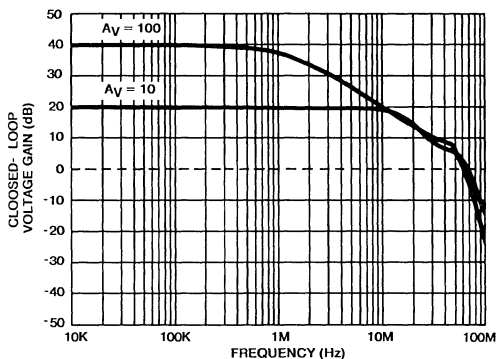
**SHORT CIRCUIT CURRENT vs. TIME**



**HA-5111 CLOSED-LOOP GAIN AND PHASE AT HIGH AND LOW TEMPERATURE**  
AT HIGH AND LOW TEMPERATURE  
(Typical Response Of One Amplifier)  
 $V_{CC} = \pm 15\text{V}$ ,  $A_V = 10\text{V/V}$ ,  $R_L = 2\text{K}$ ,  $C_L = 50\text{pF}$



**HA-5111 CLOSED-LOOP VOLTAGE GAIN FREQUENCY AT DIFFERENT CLOSED-LOOP GAINS**  
AT DIFFERENT CLOSED-LOOP GAINS  
 $T_A = +25^\circ\text{C}$ ,  $V_{CC} = \pm 15\text{V}$ ,  $A_V = 100$ ,  
 $10\text{V/V}$ ,  $R_L = 2\text{K}$ ,  $C_L = 50\text{pF}$

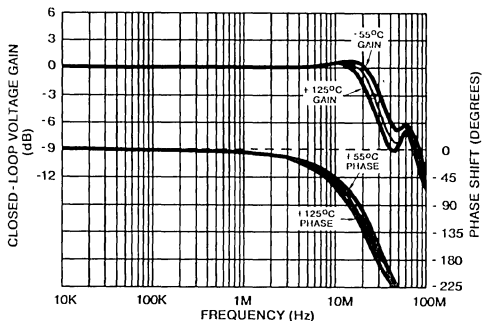


Typical Performance Curves (Continued)

HA-5101 CLOSED-LOOP GAIN AND PHASE AT HIGH AND LOW TEMPERATURE

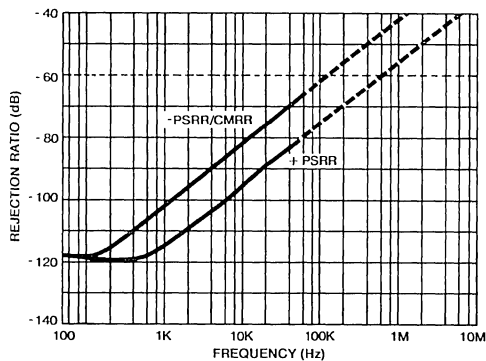
(Typical Response Of One Amplifier)

$V_{CC} = \pm 15V$ ,  $A_V = 1V/V$ ,  $R_L = 2K$ ,  $C_L = 50pF$



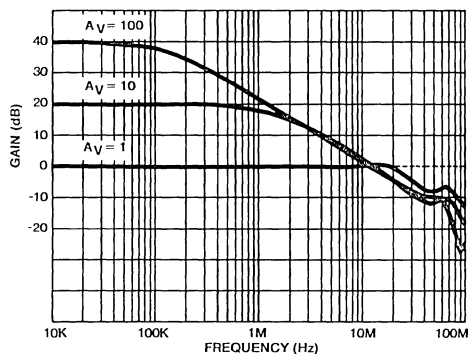
HA-5111 REJECTION RATIOS vs. FREQUENCY

$T_A = +25^\circ C$ ,  $V_{CC} = \pm 15V$



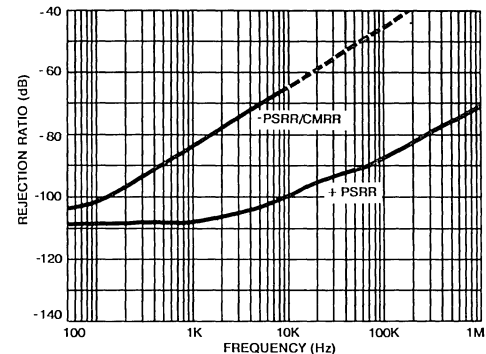
HA-5101 CLOSED-LOOP VOLTAGE GAIN vs. FREQUENCY AT DIFFERENT CLOSED-LOOP GAINS

$T_A = +25^\circ C$ ,  $V_{CC} = \pm 15V$ ,  $R_L = 2K$ ,  $C_L = 50pF$

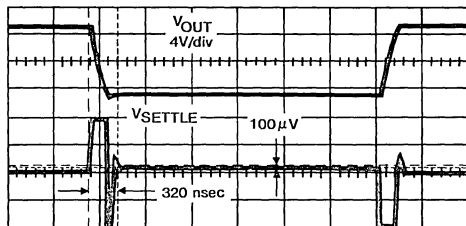


HA-5101 REJECTION RATIOS vs. FREQUENCY

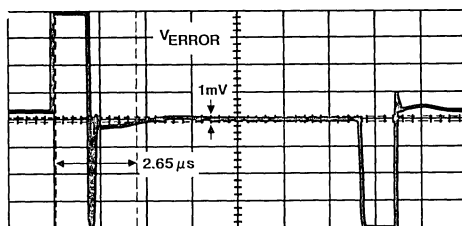
$T_A = +25^\circ C$ ,  $V_{CC} = \pm 15V$



HA-5111 SETTLING WAVEFORM 500ns/DIV.



HA-5101 SETTLING WAVEFORM 1.5μs/DIV.



**Applications Information**

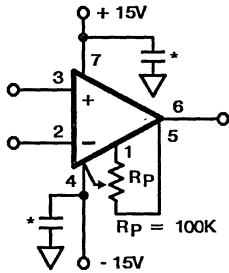
**Operation At ±5V Supply**

The HA-5101/11 performs well at  $V_{CC} = \pm 5V$  exhibiting typical characteristics as listed below:

|   |     |            |
|---|-----|------------|
| $I_{CC}$ .....                            | 3.7 | mA         |
| $V_{IO}$ .....                            | 0.5 | mA         |
| $I_{BIAS}$ .....                          | 56  | nA         |
| $AVOL (V_O = \pm 3V)$ .....               | 106 | KV/V       |
| $V_{OUT}$ .....                           | 3.7 | V          |
| $I_{OUT}$ .....                           | 13  | mA         |
| CMRR ( $\Delta V_{CM} = \pm 2.5V$ ) ..... | 90  | dB         |
| PSRR ( $\Delta V_{CC} = 0.5V$ ) .....     | 90  | dB         |
| Unity Bandwidth (5101) .....              | 10  | MHz        |
| GBW (5111) .....                          | 100 | MHz        |
| Slew Rate (5101) .....                    | 7   | V/ $\mu$ s |
| Slew Rate (5111) .....                    | 40  | V/ $\mu$ s |

**Offset Adjustment**

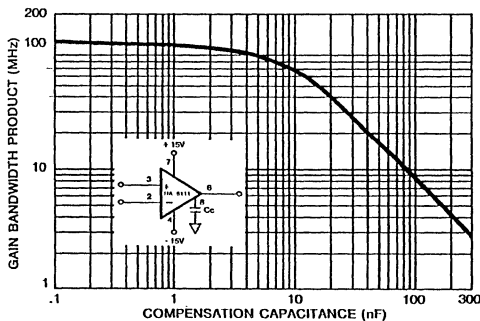
The following is the recommended  $V_{IO}$  adjust configuration:



\* Proper decoupling is always recommended, 0.1 $\mu$ F high quality capacitor should be at or very near the device's supply pins.

**Compensation**

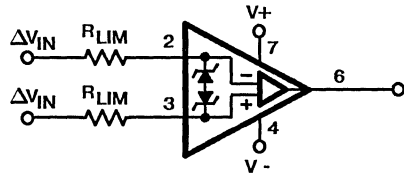
An external compensation capacitor can be used with the HA-5111 connected between pin 8 and ground (or  $V-$ ,  $V+$  not Recommended). A plot of gain bandwidth product vs. compensation capacitor has been included as a design aid. The capacitor should be a high frequency type mounted near the device leads to minimize parasitics.



**Input Protection**

The HA-5101/11 has built-in back-to-back protection diodes which will limit the differential input voltage to approximately 7V. If the 5101/11 will be used in conditions where that voltage may be exceeded, then current limiting resistors must be used. No more than 25mA should be allowed to flow in the HA-5101/11's input.

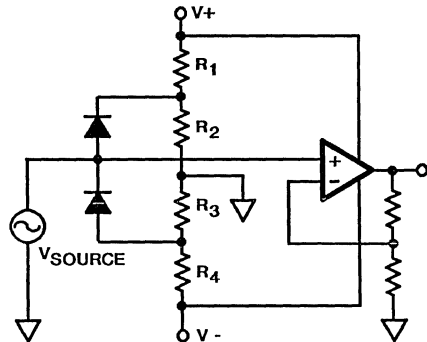
**Comparator Circuit**



Choose  $R_{LIM}$  Such That:  $\frac{(\Delta V_{INMAX} - 7V)}{25mA} < 2R_{LIM}$

**Output Saturation**

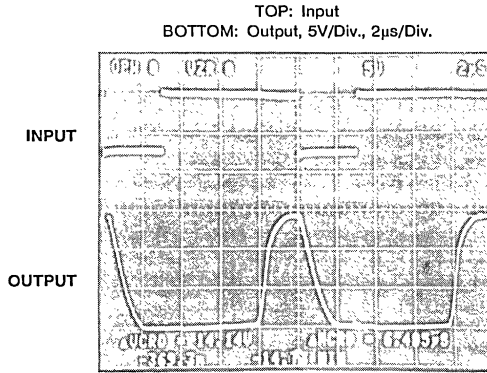
When an op amp is overdriven, output devices can saturate and sometimes take a long time to recover. Saturation can be avoided (sometimes) by using circuits such as:



If saturation cannot be avoided the HA-5101/11 recovers from a 25% overdrive in about 6.5 $\mu$ s (see photos).

# HA-5101/5111

## Applications Information (Continued)



Output is overdriven negative and recovers in 6μs.

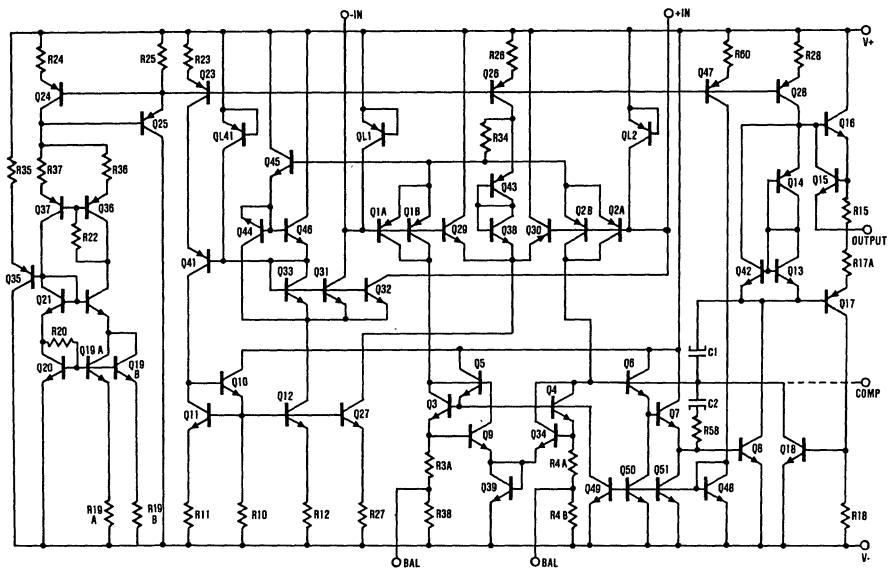
## Die Characteristics

|                            |  |               |
|----------------------------|--|---------------|
| Transistor Count .....     | 54   |               |
| Die Dimensions .....       | 69 x 69 x 19 mils<br>(1800 x 1800 x 480μm) |               |
| Substrate Potential* ..... | V- or Float                                |               |
| Process .....              | Bipolar DI                                 |               |
| Thermal Constants (°C/W)   | $\theta_{ja}$                              | $\theta_{jc}$ |
| HA2-5101/5111 (-2/-5/-7)   | 192  | 52            |
| HA2-5101/5111 (/883)       | 158  | 48            |
| HA3-5101/5111 (-5)         | 80   | 29            |
| HA7-5101/5111 (-2/-5/-7)   | 190  | 102           |
| HA7-5101/5111 (/883)       | 136  | 61            |
| HA9P5101/5111 (-5/-9)      | 160  | 42            |

\* The Substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.



Schematic



## Low Noise High Performance Operational Amplifiers

August 1991

### Features

- Low Noise .....  $4.3nV/\sqrt{Hz}$
- Wide Bandwidth ..... 8MHz (Compensated)  
60MHz (Uncompensated)
- High Slew Rate .....  $3V/\mu s$  (Compensated)  
 $20V/\mu s$  (Uncompensated)
- Low Offset Voltage ..... 0.5mV
- Available in Duals or Quads

### Applications

- High Q, Active Filters
- Audio Amplifiers
- Instrumentation Amplifiers
- Integrators
- Signal Generators
- For Further Design Ideas, See App. Note 554.

### Description

Low noise and high performance are key words describing HA-5102/04/12/14. These general purpose amplifiers offer an array of dynamic specifications ranging from a  $3V/\mu s$  slew rate and 8MHz bandwidth (5102/04) to  $20V/\mu s$  slew rate and 60MHz gain-bandwidth-product (HA-5112/14). Complementing these outstanding parameters is a very low noise specification of  $4.3nV/\sqrt{Hz}$  at 1kHz.

Fabricated using the Harris high frequency DI process, these operational amplifiers also offer excellent input specifications such as a 0.5mV offset voltage and 30nA offset current. Complementing these specifications are 108dB open loop gain and 108dB channel separation. Consuming a very modest amount of power (90mW/package for duals and 150mW/package for quads), HA-5102/04/12/14 also provide 15mA of output current.

This impressive combination of features make this series of amplifiers ideally suited for designs ranging from audio amplifiers and active filters to the most demanding signal conditioning and instrumentation circuits.

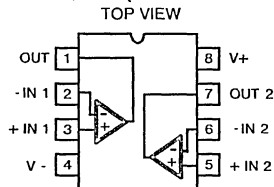
These operational amplifiers are available in dual or quad form with industry standard pinouts allowing for immediate inter-changeability with most other dual and quad operational amplifiers.

HA-5102 Dual, Comp.                      HA-5104 Quad, Comp.  
HA-5112 Dual, Uncomp.                HA-5114 Quad, Uncomp.

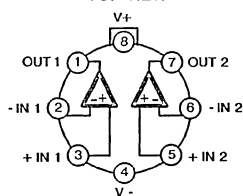
Each of these products are available in -2 (-55°C to +125°C), -5 (0°C to +75°C), -9 (-40°C to +85°C) or /883 grades. Refer to the /883 data sheet for military product.

### Pinouts

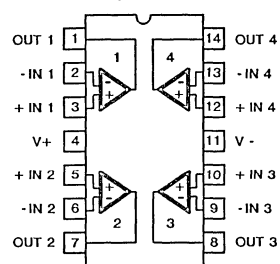
HA3-5102/5112 (PLASTIC MINI-DIP)  
HA7-5102/5112 (CERAMIC MINI-DIP)



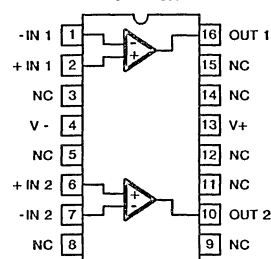
HA2-5102/5112 (TO-99 METAL CAN)



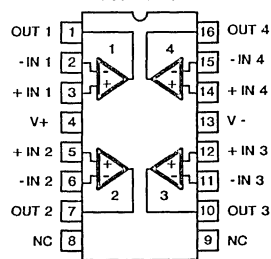
HA1-5104/5114 (CERAMIC DIP)  
HA3-5104/5114 (PLASTIC DIP)



HA9P5102/5112 (SOIC)



HA9P5104/5114 (SOIC)



## Specifications HA-5102/04/12/14

### Absolute Maximum Ratings (Note 1)

|   |                    |
|---|--------------------|
| $T_A = +25^\circ\text{C}$ Unless Otherwise Stated |                    |
| Voltage Between V+ and V- Terminals               | 40.0V              |
| Differential Input Voltage                        | $\pm 7\text{V}$    |
| Input Voltage (Note 2)                            | $\pm 15.0\text{V}$ |
| Output Short Circuit Duration (Note 3)            | Indefinite         |
| Power Dissipation (Note 4)                        | 880mW              |

### Operating Temperature Ranges

|                           |  |
|---------------------------|--|
| HA-5102/5104/5112/5114-2  | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ |
| HA-5102/5104/5112/5114-5  | $-0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$   |
| HA-5102/5104/5112/5114-9  | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$  |
| Storage Temperature Range | $-65^\circ\text{C} \leq T_A \leq +150^\circ\text{C}$ |

### Electrical Specifications V+ = 15V D.C., V- = -15V D.C., Unless Otherwise Specified

| PARAMETER   | TEMP         | HA-5102-2, -5<br>HA-5112-2, -5 |          |     | HA-5104-2, -5<br>HA-5114-2, -5 |          |     | HA-5102-9<br>HA-5112-9 |          |     | HA-5104-9<br>HA-5114-9 |          |     | UNITS                        |     |
|---|--------------|--------------------------------|----------|-----|--------------------------------|----------|-----|------------------------|----------|-----|------------------------|----------|-----|------------------------------|-----|
|   |              | MIN                            | TYP      | MAX | MIN                            | TYP      | MAX | MIN                    | TYP      | MAX | MIN                    | TYP      | MAX |                              |     |
| <b>INPUT CHARACTERISTICS</b>                          |              |                                |          |     |                                |          |     |                        |          |     |                        |          |     |                              |     |
| Offset Voltage  | +25°C        | -                              | 0.5      | 2.0 | -                              | 0.5      | 2.5 | -                      | 0.5      | 2.0 | -                      | 0.5      | 2.5 | mV                           |     |
|   | Full         | -                              | -        | 2.5 | -                              | -        | 3.0 | -                      | -        | 2.5 | -                      | -        | 3.0 | mV                           |     |
| Offset Voltage Average Drift                          | Full         | -                              | 3        | -   | -                              | 3        | -   | -                      | 3        | -   | -                      | 3        | -   | $\mu\text{V}/^\circ\text{C}$ |     |
| Bias Current  | +25°C        | -                              | 130      | 200 | -                              | 130      | 200 | -                      | 130      | 200 | -                      | 130      | 200 | nA                           |     |
|   | Full         | -                              | -        | 325 | -                              | -        | 325 | -                      | -        | 500 | -                      | -        | 500 | nA                           |     |
| Offset Current  | +25°C        | -                              | 30       | 75  | -                              | 30       | 75  | -                      | 30       | 75  | -                      | 30       | 75  | nA                           |     |
|   | Full         | -                              | -        | 125 | -                              | -        | 125 | -                      | -        | 125 | -                      | -        | 125 | nA                           |     |
| Input Resistance                                      | +25°C        | -                              | 500      | -   | -                              | 500      | -   | -                      | 500      | -   | -                      | 500      | -   | k $\Omega$                   |     |
| Common Mode Range                                     | Full         | $\pm 12$                       | -        | -   | $\pm 12$                       | -        | -   | $\pm 12$               | -        | -   | $\pm 12$               | -        | -   | V                            |     |
| <b>TRANSFER CHARACTERISTICS</b>                       |              |                                |          |     |                                |          |     |                        |          |     |                        |          |     |                              |     |
| Large Signal Voltage Gain<br>(Note 5)                 | +25°C        | 100                            | 250      | -   | 100                            | 250      | -   | 80                     | 250      | -   | 80                     | 250      | -   | kV/V                         |     |
|   | Full         | 100                            | -        | -   | 100                            | -        | -   | 80                     | -        | -   | 80                     | -        | -   | kV/V                         |     |
| Common Mode Rejection Ratio<br>(Note 6)               | Full         | 86                             | 95       | -   | 86                             | 95       | -   | 80                     | 95       | -   | 80                     | 95       | -   | dB                           |     |
| Small Signal Bandwidth<br>HA-5102/5104 ( $A_V = 1$ )  | +25°C        | -                              | 8        | -   | -                              | 8        | -   | -                      | 8        | -   | -                      | 8        | -   | MHz                          |     |
| Gain Bandwidth Product<br>HA-5112/5114 ( $A_V = 10$ ) | +25°C        | -                              | 60       | -   | -                              | 60       | -   | -                      | 60       | -   | -                      | 60       | -   | MHz                          |     |
| Channel Separation (Note 7)                           | +25°C        | -                              | 108      | -   | -                              | 108      | -   | -                      | 108      | -   | -                      | 108      | -   | dB                           |     |
| <b>OUTPUT CHARACTERISTICS</b>                         |              |                                |          |     |                                |          |     |                        |          |     |                        |          |     |                              |     |
| Output Voltage Swing<br>( $R_L = 10\text{K}$ )        | Full         | $\pm 12$                       | $\pm 13$ | -   | $\pm 12$                       | $\pm 13$ | -   | $\pm 12$               | $\pm 13$ | -   | $\pm 12$               | $\pm 13$ | -   | V                            |     |
|   | Full         | $\pm 10$                       | $\pm 12$ | -   | $\pm 10$                       | $\pm 12$ | -   | $\pm 10$               | $\pm 12$ | -   | $\pm 10$               | $\pm 12$ | -   | V                            |     |
| Output Current (Note 8)                               | Full         | $\pm 10$                       | $\pm 15$ | -   | $\pm 10$                       | $\pm 15$ | -   | $\pm 7$                | $\pm 15$ | -   | $\pm 7$                | $\pm 15$ | -   | mA                           |     |
| Full Power Bandwidth (Note 9)                         | HA-5102/5104 | +25°C                          | 16       | 47  | -                              | 16       | 47  | -                      | 16       | 47  | -                      | 16       | 47  | -                            | kHz |
|   | HA-5112/5114 | +25°C                          | 191      | 318 | -                              | 191      | 318 | -                      | 191      | 318 | -                      | 191      | 318 | -                            | kHz |
| Output Resistance                                     | +25°C        | -                              | 110      | -   | -                              | 110      | -   | -                      | 110      | -   | -                      | 110      | -   | $\Omega$                     |     |
| <b>STABILITY</b>                                      |              |                                |          |     |                                |          |     |                        |          |     |                        |          |     |                              |     |
| Minimum Stable Closed Loop Gain<br>HA-5102/5104       | Full         | 1                              | -        | -   | 1                              | -        | -   | 1                      | -        | -   | 1                      | -        | -   | V/V                          |     |
|   | Full         | 10                             | -        | -   | 10                             | -        | -   | 10                     | -        | -   | 10                     | -        | -   | V/V                          |     |

## Specifications HA-5102/04/12/14

**Electrical Specifications (Continued)**  $V_+ = 15V$  D.C.,  $V_- = -15V$  D.C., Unless Otherwise Specified

| PARAMETER                                    | TEMP  | HA-5102-2, -5<br>HA-5112-2, -5 |      |     | HA-5104-2, -5<br>HA-5114-2, -5 |      |     | HA-5102-9<br>HA-5112-9 |      |     | HA-5104-9<br>HA-5114-9 |      |     | UNITS          |
|--|-------|--------------------------------|------|-----|--------------------------------|------|-----|------------------------|------|-----|------------------------|------|-----|----------------|
|  |       | MIN                            | TYP  | MAX | MIN                            | TYP  | MAX | MIN                    | TYP  | MAX | MIN                    | TYP  | MAX |                |
| <b>TRANSIENT RESPONSE (Note 10)</b>          |       |                                |      |     |                                |      |     |                        |      |     |                        |      |     |                |
| <b>Rise Time</b>                             |       |                                |      |     |                                |      |     |                        |      |     |                        |      |     |                |
| HA-5102/5104                                 | +25°C | -                              | 108  | 200 | -                              | 108  | 200 | -                      | 108  | 200 | -                      | 108  | 200 | ns             |
| HA-5112/5114                                 | +25°C | -                              | 48   | 100 | -                              | 48   | 100 | -                      | 48   | 100 | -                      | 48   | 100 | ns             |
| <b>Overshoot</b>                             |       |                                |      |     |                                |      |     |                        |      |     |                        |      |     |                |
| HA-5102/5104                                 | +25°C | -                              | 20   | 35  | -                              | 20   | 35  | -                      | 20   | 35  | -                      | 20   | 35  | %              |
| HA-5112/5114                                 | +25°C | -                              | 30   | 40  | -                              | 30   | 40  | -                      | 30   | 40  | -                      | 30   | 40  | %              |
| <b>Slew Rate</b>                             |       |                                |      |     |                                |      |     |                        |      |     |                        |      |     |                |
| HA-5102/5104                                 | +25°C | ±1                             | ±3   | -   | ±1                             | ±3   | -   | ±1                     | ±3   | -   | ±1                     | ±3   | -   | V/μs           |
| HA-5112/5114                                 | +25°C | ±12                            | ±20  | -   | ±12                            | ±20  | -   | ±12                    | ±20  | -   | ±12                    | ±20  | -   | V/μs           |
| <b>Settling Time (Note 11)</b>               |       |                                |      |     |                                |      |     |                        |      |     |                        |      |     |                |
| HA-5102/5104                                 | +25°C | -                              | 4.5  | -   | -                              | 4.5  | -   | -                      | 4.5  | -   | -                      | 4.5  | -   | μs             |
| HA-5112/5114                                 | +25°C | -                              | 0.6  | -   | -                              | 0.6  | -   | -                      | 0.6  | -   | -                      | 0.6  | -   | μs             |
| <b>NOISE CHARACTERISTICS</b>                 |       |                                |      |     |                                |      |     |                        |      |     |                        |      |     |                |
| <b>Input Noise Voltage (Note 12)</b>         |       |                                |      |     |                                |      |     |                        |      |     |                        |      |     |                |
| f = 10Hz                                     | +25°C | -                              | 9    | 17  | -                              | 9    | 17  | -                      | 9    | 17  | -                      | 9    | 17  | $nV/\sqrt{Hz}$ |
| f = 1kHz                                     | +25°C | -                              | 4.3  | 6.0 | -                              | 4.3  | 6.0 | -                      | 4.3  | 6.0 | -                      | 4.3  | 6.0 | $nV/\sqrt{Hz}$ |
| <b>Input Noise Current (Note 12)</b>         |       |                                |      |     |                                |      |     |                        |      |     |                        |      |     |                |
| f = 10Hz                                     | +25°C | -                              | 5.1  | 12  | -                              | 5.1  | 12  | -                      | 5.1  | 12  | -                      | 5.1  | 12  | $pA/\sqrt{Hz}$ |
| f = 1kHz                                     | +25°C | -                              | 0.57 | 3   | -                              | 0.57 | 3   | -                      | 0.57 | 3   | -                      | 0.57 | 3   | $pA/\sqrt{Hz}$ |
| <b>Broadband Noise Voltage</b>               |       |                                |      |     |                                |      |     |                        |      |     |                        |      |     |                |
| f = DC to 30kHz                              | +25°C | -                              | 870  | -   | -                              | 870  | -   | -                      | 870  | -   | -                      | 870  | -   | nVrms          |
| <b>POWER SUPPLY CHARACTERISTICS</b>          |       |                                |      |     |                                |      |     |                        |      |     |                        |      |     |                |
| <b>Supply Current</b>                        |       |                                |      |     |                                |      |     |                        |      |     |                        |      |     |                |
| HA-5102/5112                                 | +25°C | -                              | 3.0  | 5.0 | -                              | 3.0  | 5.0 | -                      | 3.0  | 5.0 | -                      | 3.0  | 5.0 | mA             |
| HA-5104/5114                                 | +25°C | -                              | 5.0  | 6.5 | -                              | 5.0  | 6.5 | -                      | 5.0  | 6.5 | -                      | 5.0  | 6.5 | mA             |
| <b>Power Supply Rejection Ratio (Note 6)</b> |       |                                |      |     |                                |      |     |                        |      |     |                        |      |     |                |
| Full   | Full  | 86                             | 100  | -   | 86                             | 100  | -   | 80                     | 100  | -   | 80                     | 100  | -   | dB             |

**NOTES:**

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages  $< \pm 15V$ , the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 9.6mW/°C above  $T_A = +25°C$ .
5.  $V_{OUT} = \pm 10V$ ,  $R_L = 2K$
6.  $V_{CM} = \pm 5.0V$
7. Channel separation value is referred to the input of the amplifier. Input test conditions are:  $f = 10kHz$ ;  $V_{IN} = 200mV$  peak to peak;  $R_S = 1k\Omega$ . (Refer to Channel Separation vs. Frequency Curve for test circuits.)
8. Output current is measured with  $V_{OUT} = \pm 5V$ .
9. Full power bandwidth is guaranteed by equation:  

$$\text{Full power bandwidth} = \frac{\text{Slew Rate}}{2\pi V_{peak}}$$
10. Refer to Test Circuits section of the data sheet.
11. Settling time is measured to 0.1% of final value for a 1 volt input step, and  $A_V = -10$  for HA-5112/5114, and a 10 volt input step,  $A_V = -1$  for HA-5102/5104.
12. Sample tested.

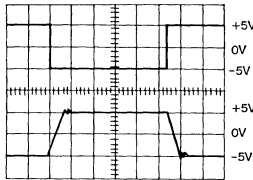
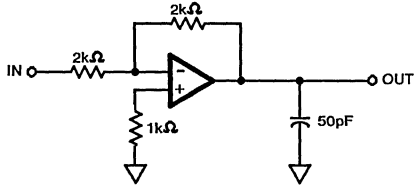
3

OPERATIONAL  
AMPLIFIERS

**Test Circuits**

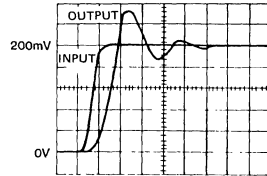
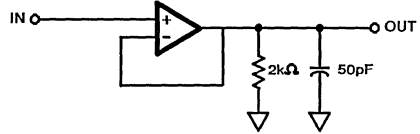
**LARGE SIGNAL RESPONSE CIRCUIT**

Volts: 5V/Div., Time: 5 $\mu$ s/Div. ( $A_V = -1$ )  
HA-5102/5104



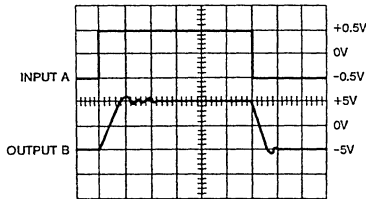
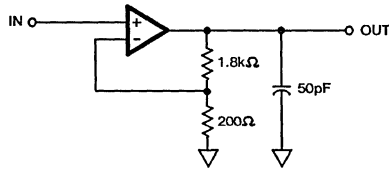
**SMALL SIGNAL RESPONSE CIRCUIT**

Volts: 40mV/Div., Time: 50ns/Div. ( $A_V = +1$ )  
HA-5102/5104

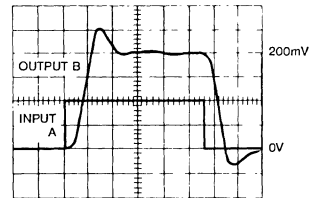


**LARGE AND SMALL SIGNAL RESPONSE CIRCUIT**

HA-5112/5114 ( $A_V = +10$ )

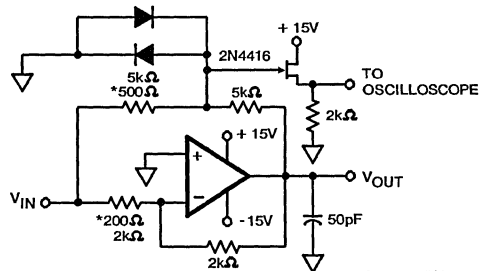


Volts: Input A: 0.5V/Div., Output B: 5V/Div.  
Time: 50ns/Div.



Volts: Input A: 0.01V/Div., Output B: 50mV/Div.  
Time: 50ns/Div.

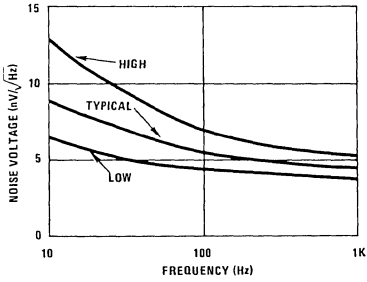
**SETTLING TIME CIRCUIT**



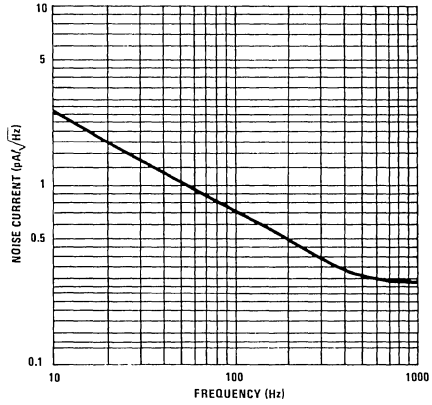
- $A_V = -1$  (HA-5102/5104),  $A_V = -10$  (HA-5112/5114)
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional, HP5082-2810 recommended.

**Typical Performance Curves**

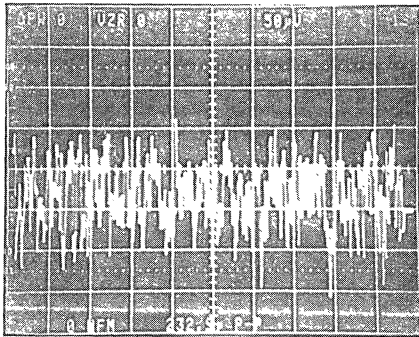
**INPUT NOISE VOLTAGE DENSITY**  
 $V_{CC} = \pm 15V, T_A = +25^\circ C$



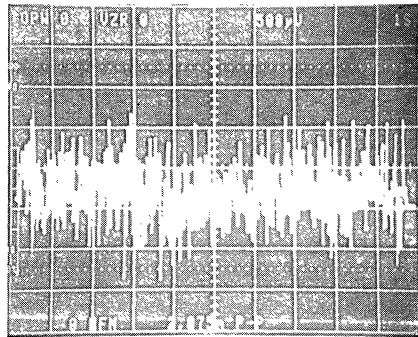
**INPUT NOISE CURRENT DENSITY**  
 $V_{CC} = \pm 15V, T_A = +25^\circ C$



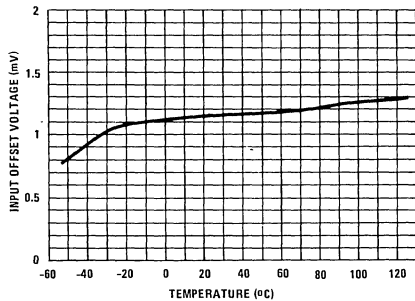
**0.1Hz TO 10Hz NOISE**  
 $V_{CC} = \pm 15V, T_A = +25^\circ C$   
 50 $\mu V/Div.$ , 1s/Div.,  $A_V = 1000 V/V$   
 Input Noise = 0.232 $\mu Vp-p$



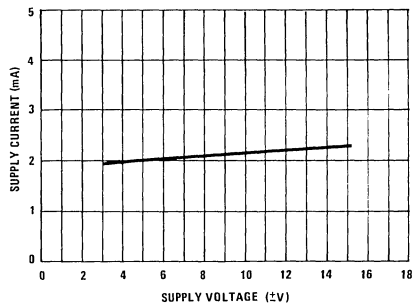
**0.1Hz TO 1MHz NOISE**  
 $V_{CC} = \pm 15V, T_A = +25^\circ C$   
 500 $\mu V/Div.$ , 1s/Div.,  $A_V = 1000 V/V$   
 Total Output Noise = 2.075 $\mu Vp-p$



**$V_{IO}$  vs. TEMPERATURE**  
 $V_{CC} = \pm 15V$

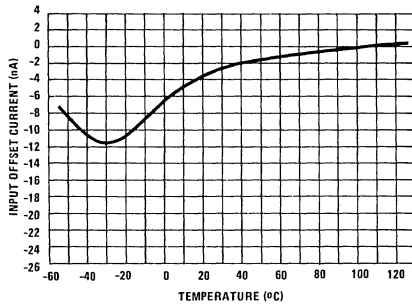


**$V_{IO}$  vs.  $V_{CC}$**   
 $T_A = +25^\circ C$

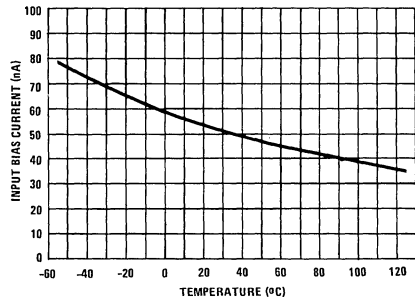


**Typical Performance Curves (Continued)**

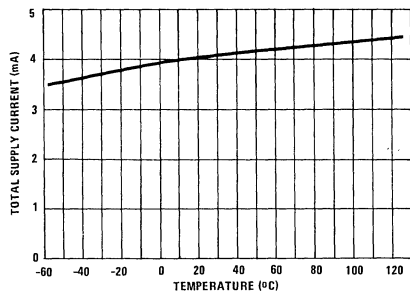
**$I_{IO}$  vs. TEMPERATURE**  
 $V_{CC} = \pm 15V$



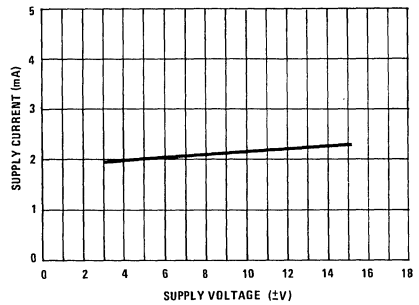
**IBIAS vs. TEMPERATURE**  
 $V_{CC} = \pm 15V$



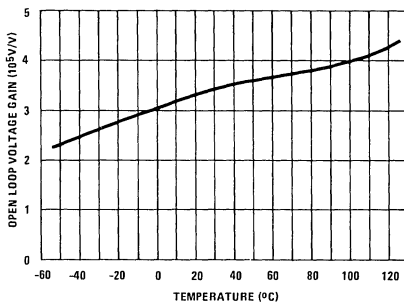
**$I_{CC}$  vs. TEMPERATURE**  
 $V_{CC} = \pm 15V, I_{OUT} = 0$



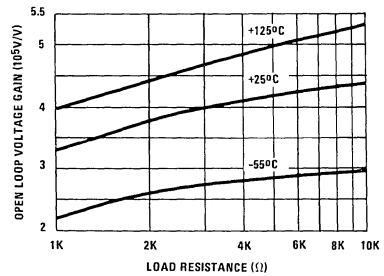
**$I_{CC}$  vs.  $V_{CC}$**   
 $T_A = +25^\circ C, I_{OUT} = 0$



**$A_{VOL}$  vs. TEMPERATURE**  
 $V_{CC} = \pm 15V, \Delta V_O = \pm 10V, R_L = 2K$

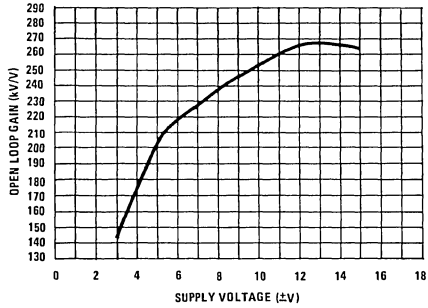


**$A_{VOL}$  vs. LOAD RESISTANCE**  
 $V_O = \pm 10V, V_{CC} = \pm 15V, T_A = +25^\circ C$

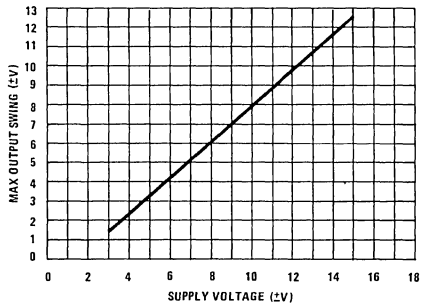


Typical Performance Curves (Continued)

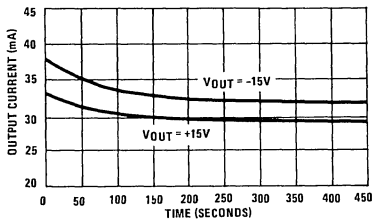
**AVOL vs. VCC**  
 $T_A = +25^\circ\text{C}$ ,  $R_L = 2\text{K}$



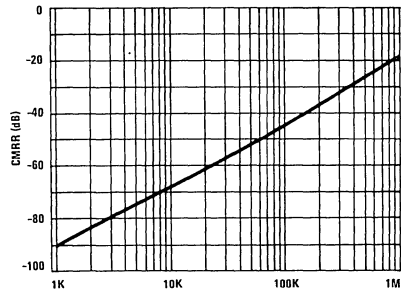
**VOUT vs. VCC**  
 $T_A = +25^\circ\text{C}$ ,  $R_L = 2\text{K}$



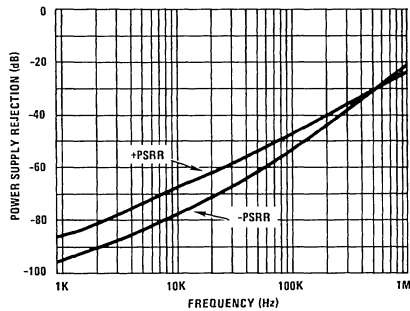
**OUTPUT SHORT-CIRCUIT CURRENT vs. TIME**  
 $V_{CC} = \pm 15\text{V}$ ,  $T_A = +25^\circ\text{C}$



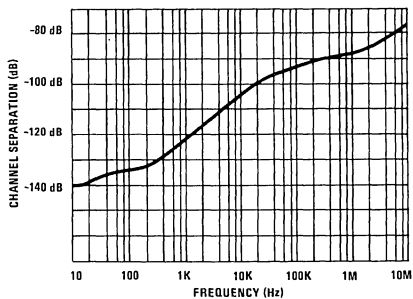
**CMRR vs. FREQUENCY**



**PSRR vs. FREQUENCY**



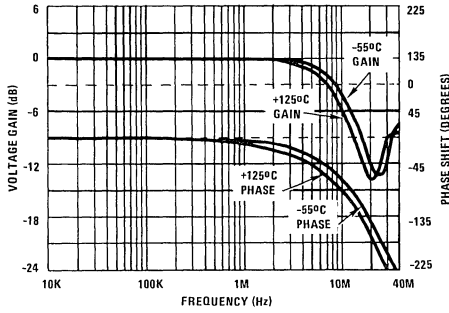
**HA-5104 CHANNEL SEPARATION vs. FREQUENCY**  
 $10\text{Hz} \leq f \leq 10\text{MHz}$



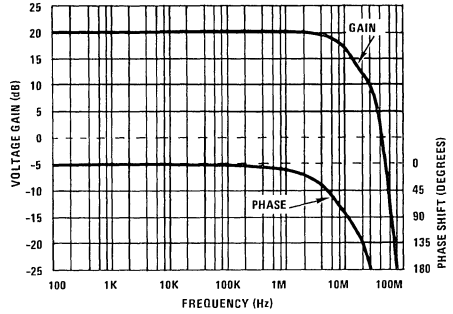


Typical Performance Curves (Continued)

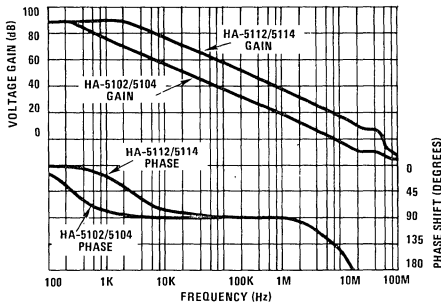
HA-5104/02 UNITY GAIN FREQUENCY RESPONSE  
 $V_{CC} = \pm 15V, R_L = 2K, C_L = 50pF$



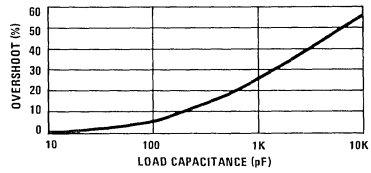
HA-5112/14 FREQUENCY RESPONSE  
 $A_{VCL} = 10, T_A = +25^\circ C, R_L = 2K, C_L = 50pF$



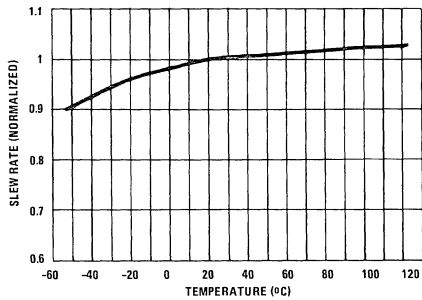
OPEN LOOP GAIN vs. FREQUENCY  
 $V_{CC} = \pm 15V, R_L = 2K, C_L = 50pF, T_A = +25^\circ C$



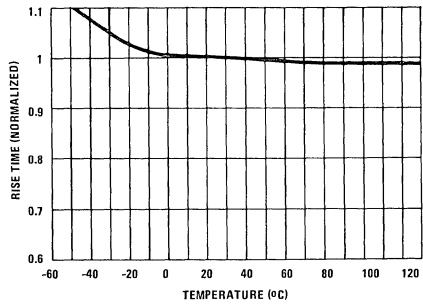
SMALL SIGNAL OVERSHOOT vs. CLOAD  
 $V_{CC} = \pm 15V, T_A = +25^\circ C, R_L = 2K$



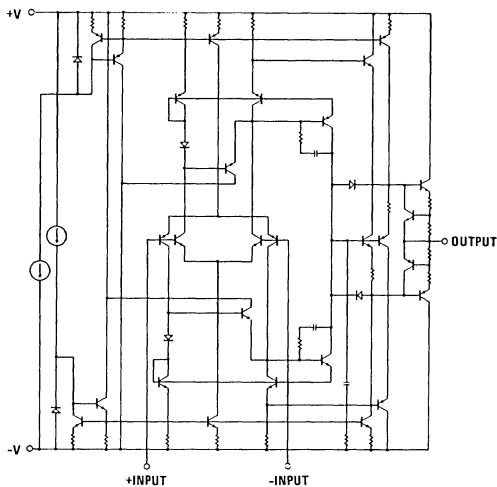
SLEW RATE vs. TEMPERATURE  
 $R_L = 2K, C_L = 50pF, V_{CC} = \pm 15V$



RISE TIME vs. TEMPERATURE  
 $R_L = 2K, C_L = 50pF, V_{CC} = \pm 15V$



**Simplified Schematic**



**Die Characteristics**

| Transistor Count  | Thermal Constants (°C/W)   | $\theta_{ja}$ | $\theta_{jc}$ |
|---|----------------------------|---------------|---------------|
| HA-5102/5112 ..... 93   | HA1-5104 (-2, -5, -7)      | 103           | 35            |
| HA-5104/5114 ..... 175  | HA1-5104 (/883)            | 78            | 25            |
| Die Dimensions  | HA2-5102/5112 (-2, -5, -7) | 174           | 48            |
| HA-5102/5112 ..... 98.4 x 67.3 x 19 mils<br>(2500 x 1710 x 480 $\mu$ m) | HA2-5102/5112 (/883)       | 134           | 40            |
| HA-5104/5114 ..... 99.6 x 95.3 x 19 mils<br>(2530 x 2420 x 480 $\mu$ m) | HA3-5102/5112 (-5)         | 80            | 20            |
| Substrate Potential* ..... V-   | HA3-5104/5114 (-5)         | 75            | 23            |
| Process ..... Bipolar-DI  | HA7-5102/5112 (-2, -5, -7) | 163           | 82            |
| Passivation ..... Nitride   | HA7-5102/5112 (/883)       | 124           | 47            |
|   | HA9P5102/5112              | 160           | 42            |
|   | HA9P5104/5114              | 94            | 26            |

\*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

August 1991

### Features

- High Speed ..... 10V/ $\mu$ s
- Wide Unity Gain Bandwidth ..... 8.5MHz
- Low Noise ..... 3nV/ $\sqrt{\text{Hz}}$  at 1KHz
- Low VOS ..... 10 $\mu$ V
- High CMRR ..... 126dB
- High Gain ..... 1800V/mV

### Description

The HA-5127 monolithic operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Harris D. I. technology and advanced processing techniques, this unique design unites low noise (3nV/ $\sqrt{\text{Hz}}$ ) precision instrumentation performance with high speed (10V/ $\mu$ s) wideband capability.

This amplifier's impressive list of features include low VOS (10 $\mu$ V), wide unity gain-bandwidth (8.5MHz), high open loop gain (1800V/mV), and high CMRR (126dB). Additionally, this flexible device operates over a wide supply range ( $\pm 5\text{V}$  to  $\pm 20\text{V}$ ) while consuming only 140mW of power.

### Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers

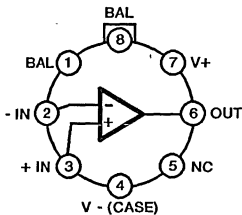
Using the HA-5127 allows designers to minimize errors while maximizing speed and bandwidth.

This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5127's qualities include instrumentation amplifiers, pulse amplifiers, audio preamplifiers, and signal conditioning circuits.

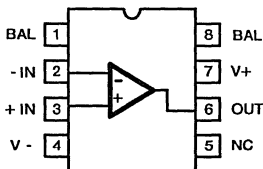
This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37. The HA-5127 is available in TO-99 Metal Can and Ceramic 8 pin Mini-DIPs. For the military grade product, refer to the HA-5127/883 data sheet.

### Pinouts

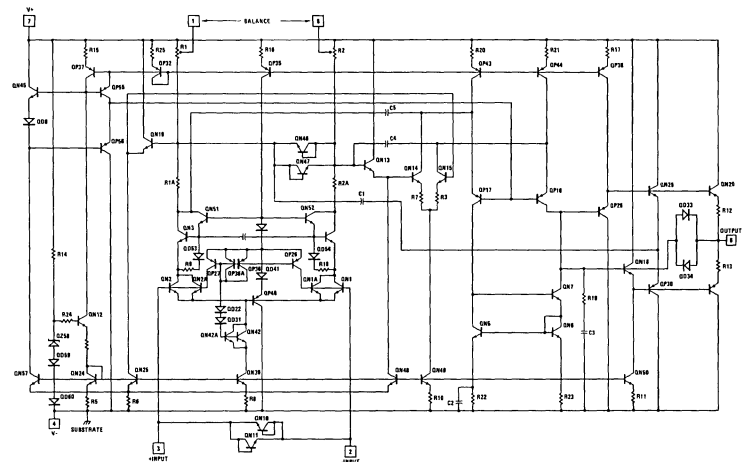
HA2-5127 (TO-99 METAL CAN)  
TOP VIEW



HA7-5127 (CERAMIC MINI-DIP)  
TOP VIEW



### Schematic



## Specifications HA-5127

### Absolute Maximum Ratings (Note 1)

|  |
|--|
| $T_A = +25^\circ\text{C}$ Unless Otherwise Stated                |
| Voltage Between $V_+$ and $V_-$ Terminals ..... $\pm 22\text{V}$ |
| Differential Input Voltage (Note 2) ..... $\pm 0.7\text{V}$      |
| Internal Power Dissipation ..... 500mW                           |
| Output Current ..... Full Short Circuit Protection               |

### Operating Temperature Ranges

|                                    |  |
|------------------------------------|--|
| HA-5127/27A-2 .....                | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ |
| HA-5127/27A-5 .....                | $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$    |
| Storage Temperature Range .....    | $-65^\circ\text{C} \leq T_A \leq +150^\circ\text{C}$ |
| Maximum Junction Temperature ..... | $\leq +175^\circ\text{C}$                            |

### Electrical Specifications $V_+ = 15\text{V}$ , $V_- = -15\text{V}$ , $C_L < 50\text{pF}$ , $R_S < 100\Omega$

| PARAMETER                                  | TEMP                  | HA-5127A            |            |            | HA-5127    |            |            | UNITS                        |   |
|--|-----------------------|---------------------|------------|------------|------------|------------|------------|------------------------------|---|
|  |                       | MIN                 | TYP        | MAX        | MIN        | TYP        | MAX        |                              |   |
| <b>INPUT CHARACTERISTICS</b>               |                       |                     |            |            |            |            |            |                              |   |
| Offset Voltage                             | $+25^\circ\text{C}$   | -                   | 10         | 25         | -          | 30         | 100        | $\mu\text{V}$                |   |
|  | Full                  | -                   | 30         | 60         | -          | 70         | 300        | $\mu\text{V}$                |   |
| Average Offset Voltage Drift               | Full                  | -                   | 0.2        | 0.6        | -          | 0.4        | 1.8        | $\mu\text{V}/^\circ\text{C}$ |   |
| Bias Current                               | $+25^\circ\text{C}$   | -                   | $\pm 10$   | $\pm 40$   | -          | $\pm 15$   | $\pm 80$   | nA                           |   |
|  | Full                  | -                   | $\pm 20$   | $\pm 60$   | -          | $\pm 35$   | $\pm 150$  | nA                           |   |
| Offset Current                             | $+25^\circ\text{C}$   | -                   | 7          | 35         | -          | 12         | 75         | nA                           |   |
|  | Full                  | -                   | 15         | 50         | -          | 30         | 135        | nA                           |   |
| Common Mode Range                          | Full                  | $\pm 10.3$          | $\pm 11.5$ | -          | $\pm 10.3$ | $\pm 11.5$ | -          | V                            |   |
| Differential Input Resistance (Note 3)     | $+25^\circ\text{C}$   | 1.5                 | 6          | -          | 0.8        | 4          | -          | M $\Omega$                   |   |
| Input Noise Voltage 0.1Hz to 10Hz (Note 4) | $+25^\circ\text{C}$   | -                   | 0.08       | 0.18       | -          | 0.09       | 0.25       | $\mu\text{Vp-p}$             |   |
| Input Noise Voltage Density (Note 5)       | $f_0 = 10\text{Hz}$   | -                   | 3.5        | 5.5        | -          | 3.8        | 8.0        | $\text{nV}/\sqrt{\text{Hz}}$ |   |
|  | $f_0 = 30\text{Hz}$   | -                   | 3.1        | 4.5        | -          | 3.3        | 5.6        | $\text{nV}/\sqrt{\text{Hz}}$ |   |
|  | $f_0 = 1000\text{Hz}$ | -                   | 3.0        | 3.8        | -          | 3.2        | 4.5        | $\text{nV}/\sqrt{\text{Hz}}$ |   |
|  | $f_0 = 10\text{Hz}$   | $+25^\circ\text{C}$ | -          | 1.7        | 4.0        | -          | 1.7        | $\text{pA}/\sqrt{\text{Hz}}$ |   |
| Input Noise Current Density (Note 5)       | $f_0 = 30\text{Hz}$   | -                   | 1.0        | 2.3        | -          | 1.0        | -          | $\text{pA}/\sqrt{\text{Hz}}$ |   |
|  | $f_0 = 1000\text{Hz}$ | -                   | 0.4        | 0.6        | -          | 0.4        | 0.6        | $\text{pA}/\sqrt{\text{Hz}}$ |   |
|  |                       |                     |            |            |            |            |            |                              |   |
| <b>TRANSFER CHARACTERISTICS</b>            |                       |                     |            |            |            |            |            |                              |   |
| Large Signal Voltage Gain (Note 7)         | $+25^\circ\text{C}$   | 1000                | 1800       | -          | 700        | 1500       | -          | V/mV                         |   |
|  | Full                  | 600                 | 1200       | -          | 300        | 800        | -          | V/mV                         |   |
| Common Mode Rejection Ratio (Note 7)       | Full                  | 114                 | 126        | -          | 100        | 120        | -          | dB                           |   |
| Minimum Stable Gain                        | $+25^\circ\text{C}$   | 1                   | -          | -          | 1          | -          | -          | V/V                          |   |
| Unity-Gain-Bandwidth                       | $+25^\circ\text{C}$   | 5                   | 8.5        | -          | 5          | 8.5        | -          | MHz                          |   |
| <b>OUTPUT CHARACTERISTICS</b>              |                       |                     |            |            |            |            |            |                              |   |
| Output Voltage Swing                       | $R_L = 600\Omega$     | $+25^\circ\text{C}$ | $\pm 10.0$ | $\pm 11.5$ | -          | $\pm 10.0$ | $\pm 11.5$ | -                            | V |
|  | $R_L = 2K\Omega$      | Full                | $\pm 11.7$ | $\pm 13.8$ | -          | $\pm 11.4$ | $\pm 13.5$ | -                            | V |
| Full Power Bandwidth (Note 8)              | $+25^\circ\text{C}$   | 111                 | 160        | -          | 111        | 160        | -          | kHz                          |   |
| Output Resistance, Open Loop               | $+25^\circ\text{C}$   | -                   | 70         | -          | -          | 70         | -          | $\Omega$                     |   |
| Output Current                             | $+25^\circ\text{C}$   | 16.5                | 25         | -          | 16.5       | 25         | -          | mA                           |   |
| <b>TRANSIENT RESPONSE (Note 9)</b>         |                       |                     |            |            |            |            |            |                              |   |
| Rise Time                                  | $+25^\circ\text{C}$   | -                   | -          | 150        | -          | -          | 150        | ns                           |   |
| Slew Rate (Note 11)                        | $+25^\circ\text{C}$   | 7                   | 10         | -          | 7          | 10         | -          | V/ $\mu\text{s}$             |   |
| Settling Time (Note 10)                    | $+25^\circ\text{C}$   | -                   | 1.5        | -          | -          | 1.5        | -          | $\mu\text{s}$                |   |
| Overshoot                                  | $+25^\circ\text{C}$   | -                   | 20         | 40         | -          | 20         | 40         | %                            |   |
| <b>POWER SUPPLY CHARACTERISTICS</b>        |                       |                     |            |            |            |            |            |                              |   |
| Supply Current                             | $+25^\circ\text{C}$   | -                   | 3.5        | -          | -          | 3.5        | -          | mA                           |   |
|  | Full                  | -                   | -          | 4.0        | -          | -          | 4.0        | mA                           |   |
| Power Supply Rejection Ratio (Note 12)     | Full                  | -                   | 2          | 4          | -          | 16         | 51         | $\mu\text{V}/\text{V}$       |   |

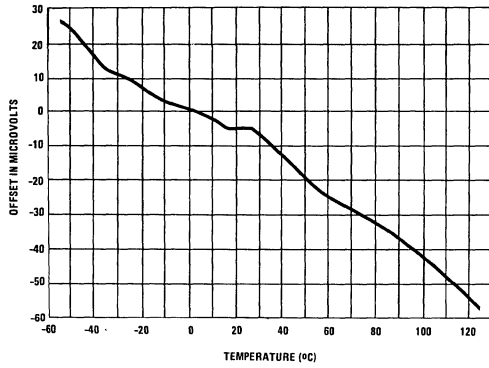
#### NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.
3. This parameter value is based upon design calculations.
4. Refer to Typical Performance section of the data sheet.
5. Sample tested.
6.  $V_{\text{OUT}} = \pm 10\text{V}$ ,  $R_L = 2K\Omega$
7.  $V_{\text{CM}} = \pm 10\text{V}$
8. Full power bandwidth guaranteed based on slew rate measurement using:  $\text{FPBW} = \frac{\text{Slew Rate}}{2\pi V_{\text{PEAK}}}$
9. Refer to Test Circuits section of the data sheet.
10. Settling time is specified to 0.1% of final value for a 10V output step and  $A_V = -1$ .
11.  $V_{\text{OUT}} = 10\text{V}$  Step
12.  $V_S = \pm 4\text{V}$  to  $\pm 18\text{V}$

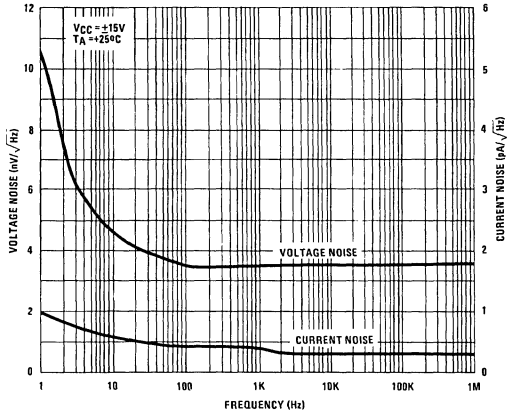
# HA-5127

**Typical Performance Curves** Unless Otherwise Specified:  $T_A = +25^\circ\text{C}$ ,  $V_{\text{SUPPLY}} = \pm 15\text{V}$

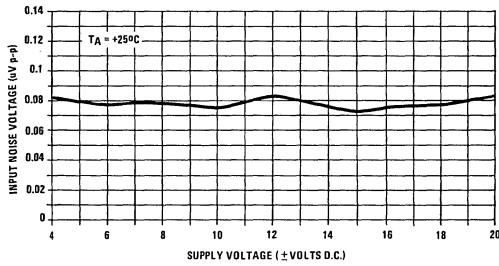
**OFFSET VOLTAGE TYPICAL DRIFT vs. TEMPERATURE**



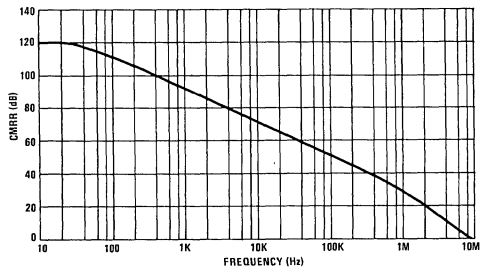
**NOISE CHARACTERISTICS**



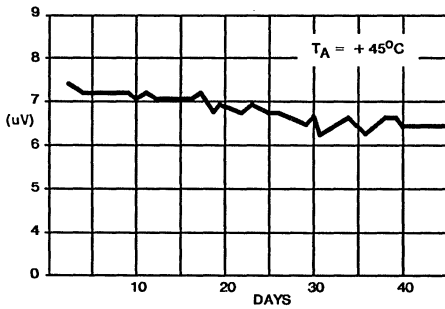
**NOISE vs. SUPPLY VOLTAGE**



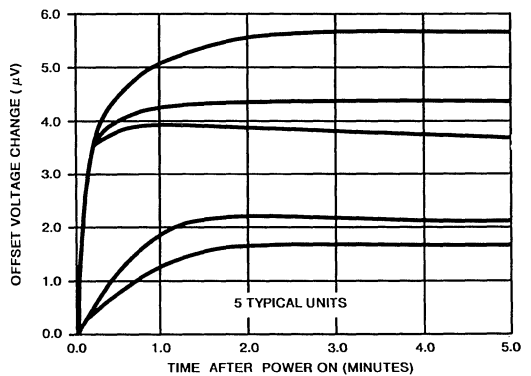
**CMRR vs. FREQUENCY**



**OFFSET VOLTAGE DRIFT vs. TIME**

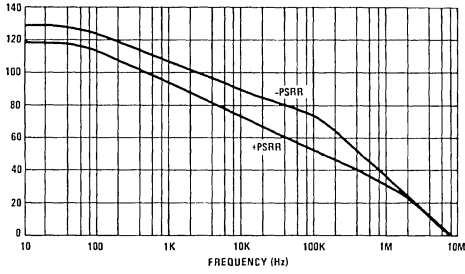


**OFFSET VOLTAGE WARM UP DRIFT**

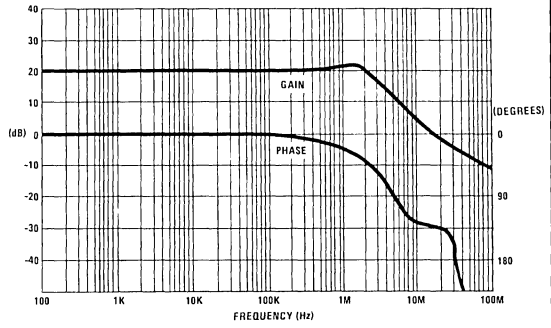


**Typical Performance Curves** Unless Otherwise Specified:  $T_A = +25^\circ\text{C}$ ,  $V_{\text{SUPPLY}} = \pm 15\text{V}$

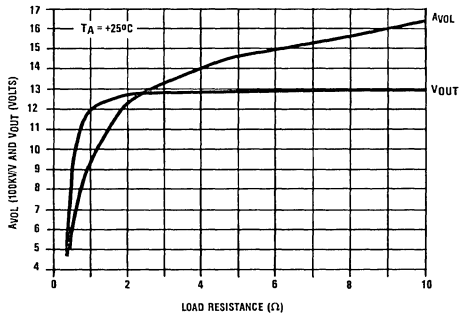
**PSRR vs. FREQUENCY**



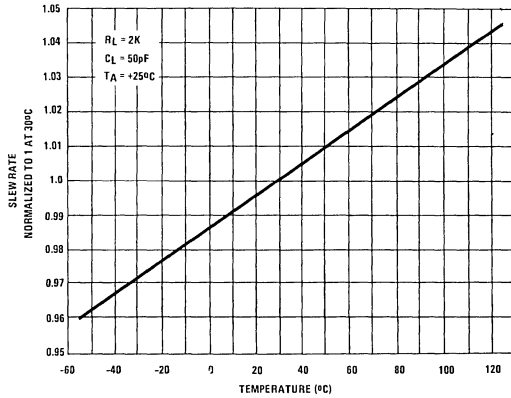
**CLOSED LOOP GAIN AND PHASE vs. FREQUENCY**



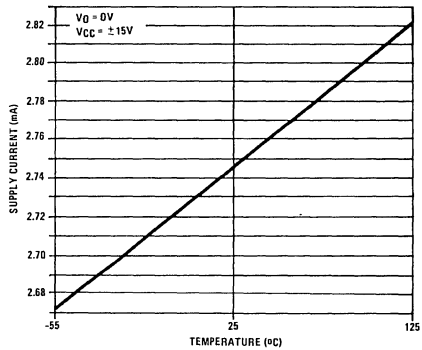
**AVOL AND  $V_{\text{OUT}}$  vs. LOAD RESISTANCE**



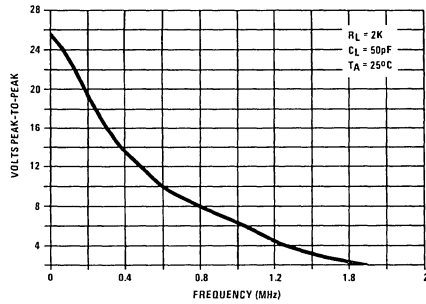
**NORMALIZED SLEW RATE vs. TEMPERATURE**



**SUPPLY CURRENT vs. TEMPERATURE**

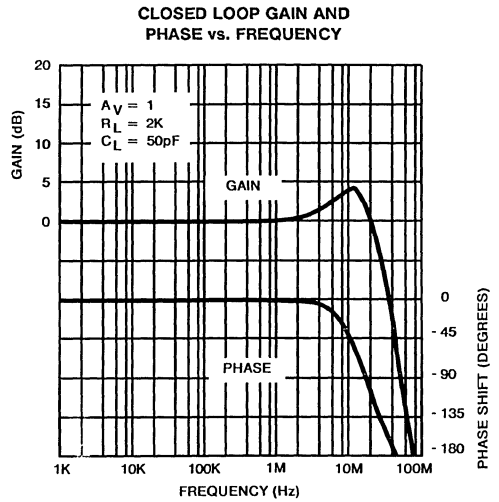
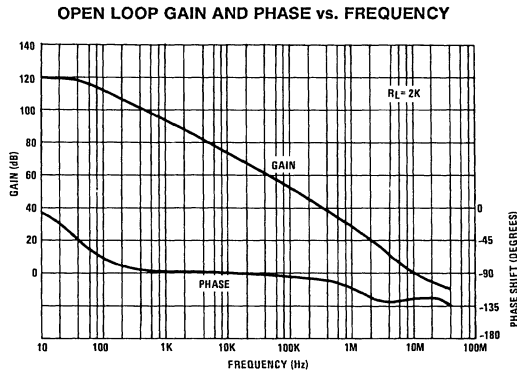
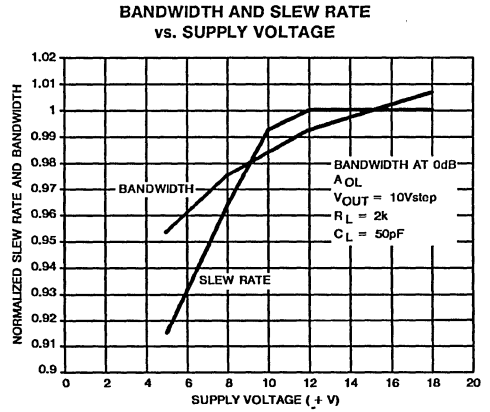
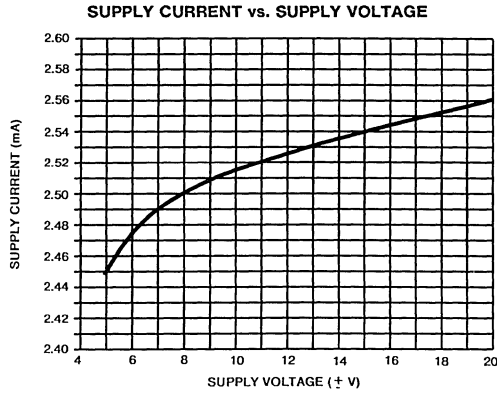


**$V_{\text{OUT MAX}}$  vs. FREQUENCY  
UNDISTORTED SINEWAVE OUTPUT**



# HA-5127

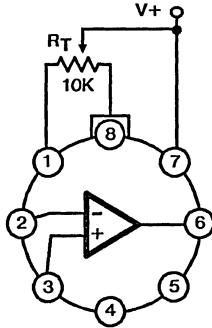
**Typical Performance Curves** Unless Otherwise Specified:  $T_A = +25^\circ\text{C}$ ,  $V_{\text{SUPPLY}} = \pm 15\text{V}$



# HA-5127

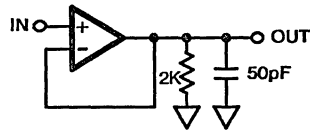
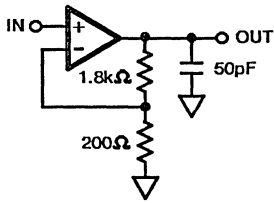
**Typical Performance Curves** Unless Otherwise Specified:  $T_A = +25^\circ\text{C}$ ,  $V_{\text{SUPPLY}} = \pm 15\text{V}$

## SUGGESTED OFFSET VOLTAGE ADJUSTMENT

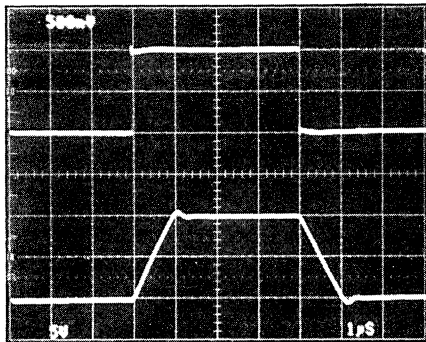


Tested Offset Adjustment Range is  $|V_{\text{OS}} + 1\text{mV}|$  minimum referred to output. Typical range is  $\pm 4\text{mV}$  with  $R_T = 10\text{k}\Omega$ .

## LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUITS

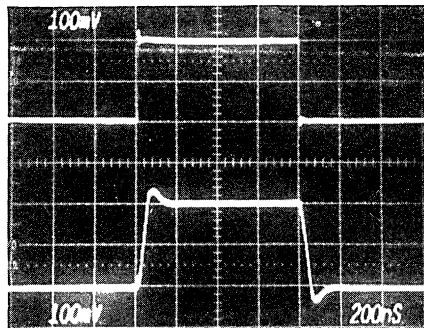


### LARGE SIGNAL RESPONSE



Vertical Scale: (Volts: Input = 0.5V/Div.)  
(Output = 5V/Div.)  
Horizontal Scale: (Time = 1μs/Div.)

### SMALL SIGNAL RESPONSE



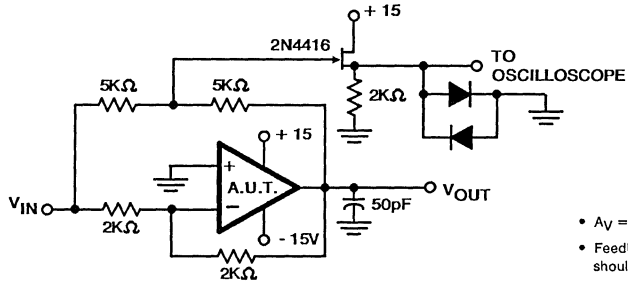
Vertical Scale: (Volts: 100mV/Div.)  
Horizontal Scale: (200ns/Div.)



# HA-5127

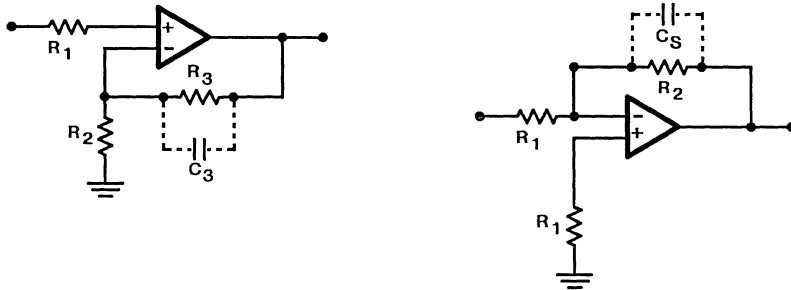
**Typical Performance Curves** Unless Otherwise Specified:  $T_A = +25^\circ\text{C}$ ,  $V_{\text{SUPPLY}} = \pm 15\text{V}$

## SETTLING TIME TEST CIRCUIT



- $A_v = -1$
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended

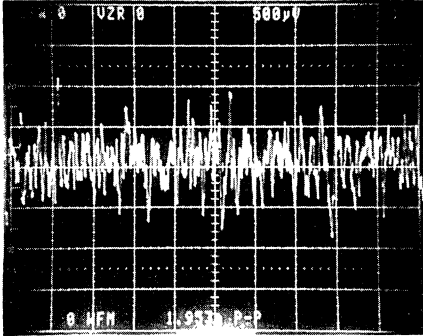
## SUGGESTED STABILITY CIRCUITS



Low resistances are preferred for low noise applications as a  $1\text{k}\Omega$  resistor has  $4\text{nV}/\sqrt{\text{Hz}}$  of thermal noise. Total resistances of greater than  $10\text{k}\Omega$  on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

## HA-5127

0.1Hz TO 10Hz NOISE WITH  $A_{CL} = 25,000V/V$



Horizontal Scale = 1sec/Div.  
Vertical Scale = 0.002 $\mu$ V/Div.  
0.08 $\mu$ Vp-p

### Die Characteristics

|                                     |   |               |
|-------------------------------------|---|---------------|
| Transistor Count                    | 63  |               |
| Die Dimensions                      | 65 x 104.3 x 19 mils<br>(1700 $\mu$ m x 2600 $\mu$ m x 480 $\mu$ m) |               |
| Substrate Potential*                | V-  |               |
| Process                             | Bipolar-DI  |               |
| Thermal Constants ( $^{\circ}C/W$ ) | $\theta_{ja}$   | $\theta_{jc}$ |
| HA7-5127 Ceramic Mini-DIP           | 160   | 79            |
| HA2-5127 TO-99 Metal Can            | 172   | 48            |

\*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

3

OPERATIONAL  
AMPLIFIERS

August 1991

## Precision Operational Amplifier

### Features

- Low Offset Voltage ..... 10 $\mu$ V
- Low Offset Voltage Drift ..... 0.4 $\mu$ V/ $^{\circ}$ C
- Low Noise ..... 9nV/ $\sqrt{\text{Hz}}$
- Open Loop Gain ..... 140dB
- Unity Gain Bandwidth ..... 2.5MHz
- All Bipolar Construction

### Description

The Harris HA-5130/5135 are precision operational amplifiers manufactured using a combination of key technological advancements to provide outstanding input characteristics.

A Super Beta input stage is combined with laser trimming, dielectric isolation and matching techniques to produce 25 $\mu$ V (Maximum) input offset voltage and 0.4 $\mu$ V/ $^{\circ}$ C input offset voltage average drift. Other features enhanced by this process include 9nV/ $\sqrt{\text{Hz}}$  (Typ.) Input Noise Voltage, 1nA Input Bias Current and 140dB Open Loop Gain.

These features coupled with 120dB CMRR and PSRR make HA-5130/5135 an ideal device for precision DC

### Applications

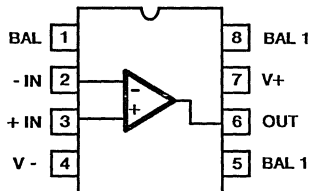
- High Gain Instrumentation
- Precision Data Acquisition
- Precision Integrators
- Biomedical Amplifiers
- Precision Threshold Detectors

instrumentation amplifiers. Excellent input characteristics in conjunction with 2.5MHz bandwidth and 0.8V/ $\mu$ s slew rate, make this amplifier extremely useful for precision integrator and biomedical amplifier designs. These amplifiers are also well suited for precision data acquisition and for accurate threshold detector applications.

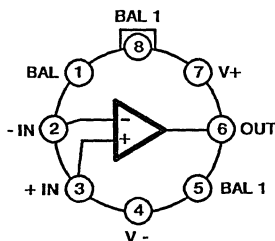
HA-5130/5135 is packaged in an 8 pin (TO-99) Metal Can and an 8 lead Cerdip and is pin compatible with many existing op amp configurations. It offers added features over the industry standard OP-07 in regards to bandwidth and slew rate specifications. For the military grade product, refer to the HA-5135/883 data sheet.

### Pinouts

HA7-5130/5135 (CERAMIC MINI-DIP)  
TOP VIEW

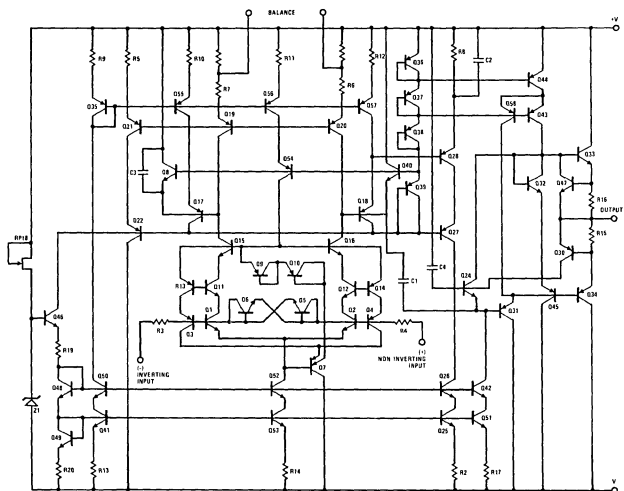


HA2-5130/5135 (TO-99 METAL CAN)  
TOP VIEW



(Both BAL 1 Pins are Connected Together Internally)

### Schematic



## Specifications HA-5130/5135

### Absolute Maximum Ratings (Note 1)

|   |                    |
|---|--------------------|
| $T_A = +25^\circ\text{C}$ Unless Otherwise Stated |                    |
| Voltage Between V+ and V- Terminals               | 40.0V              |
| Differential Input Voltage                        | $\pm 15.0\text{V}$ |
| Output Short Circuit Duration                     | Indefinite         |
| Power Dissipation (Note 2)                        | 300mW              |

### Operating Temperature Ranges

|                           |  |
|---------------------------|--|
| HA-5130/5135-2            | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ |
| HA-5130/5135-5            | $0^\circ\text{C} < T_A \leq +75^\circ\text{C}$       |
| Storage Temperature Range | $-65^\circ\text{C} \leq T_A \leq +150^\circ\text{C}$ |

### Electrical Specifications $V_+ = +15\text{V}$ , $V_- = -15\text{V}$

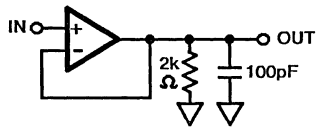
| PARAMETER                                  | TEMP  | HA-5130-2/-5 |          |         | HA-5135-2/-5 |          |         | UNITS                        |
|--|-------|--------------|----------|---------|--------------|----------|---------|------------------------------|
|  |       | MIN          | TYP      | MAX     | MIN          | TYP      | MAX     |                              |
| <b>INPUT CHARACTERISTICS</b>               |       |              |          |         |              |          |         |                              |
| Offset Voltage                             | +25°C | -            | 10       | 25      | -            | 10       | 75      | $\mu\text{V}$                |
|  | Full  | -            | 50       | 60      | -            | 50       | 130     | $\mu\text{V}$                |
| Average Offset Voltage Drift               | Full  | -            | 0.4      | 0.6     | -            | 0.4      | 1.3     | $\mu\text{V}/^\circ\text{C}$ |
| Bias Current                               | +25°C | -            | $\pm 1$  | $\pm 2$ | -            | $\pm 1$  | $\pm 4$ | nA                           |
|  | Full  | -            | -        | $\pm 4$ | -            | -        | $\pm 6$ | nA                           |
| Bias Current Average Drift                 | Full  | -            | 0.02     | 0.04    | -            | 0.02     | 0.04    | $\text{nA}/^\circ\text{C}$   |
| Offset Current                             | +25°C | -            | -        | 2       | -            | -        | 4       | nA                           |
|  | Full  | -            | -        | 4       | -            | -        | 5.5     | nA                           |
| Offset Current Average Drift               | Full  | -            | 0.02     | 0.04    | -            | 0.02     | 0.04    | $\text{nA}/^\circ\text{C}$   |
| Common Mode Range                          | Full  | $\pm 12$     | -        | -       | $\pm 12$     | -        | -       | V                            |
| Differential Input Resistance              | +25°C | 20           | 30       | -       | 20           | 30       | -       | $\text{M}\Omega$             |
| Input Noise Voltage 0.1Hz to 10Hz (Note 3) | +25°C | -            | -        | 0.6     | -            | -        | 0.6     | $\mu\text{Vp-p}$             |
| Input Noise Voltage Density (Note 3)       | +25°C | -            | -        | -       | -            | -        | -       | $\text{nV}/\sqrt{\text{Hz}}$ |
| $f_0 = 10\text{Hz}$                        |       | -            | 13.0     | 18.0    | -            | 13.0     | 18.0    | $\text{nV}/\sqrt{\text{Hz}}$ |
| $f_0 = 100\text{Hz}$                       |       | -            | 10.0     | 13.0    | -            | 10.0     | 13.0    | $\text{nV}/\sqrt{\text{Hz}}$ |
| $f_0 = 1000\text{Hz}$                      |       | -            | 9.0      | 11.0    | -            | 9.0      | 11.0    | $\text{nV}/\sqrt{\text{Hz}}$ |
| Input Noise Current 0.1Hz to 10Hz (Note 3) | +25°C | -            | 15       | 30      | -            | 15       | 30      | $\text{pAp-p}$               |
| Input Noise Current Density (Note 3)       | +25°C | -            | -        | -       | -            | -        | -       | $\text{pA}/\sqrt{\text{Hz}}$ |
| $f_0 = 10\text{Hz}$                        |       | -            | 0.4      | 0.8     | -            | 0.4      | 0.8     | $\text{pA}/\sqrt{\text{Hz}}$ |
| $f_0 = 100\text{Hz}$                       |       | -            | 0.17     | 0.23    | -            | 0.17     | 0.23    | $\text{pA}/\sqrt{\text{Hz}}$ |
| $f_0 = 1000\text{Hz}$                      |       | -            | 0.14     | 0.17    | -            | 0.14     | 0.17    | $\text{pA}/\sqrt{\text{Hz}}$ |
| <b>TRANSFER CHARACTERISTICS</b>            |       |              |          |         |              |          |         |                              |
| Large Signal Voltage Gain (Note 4)         | +25°C | 120          | 140      | -       | 120          | 140      | -       | dB                           |
|  | Full  | 120          | -        | -       | 120          | -        | -       | dB                           |
| Common Mode Rejection Ratio (Note 5)       | Full  | 110          | 120      | -       | 106          | 120      | -       | dB                           |
| Closed Loop Bandwidth ( $A_{VCL} = +1$ )   | +25°C | 0.6          | 2.5      | -       | 0.6          | 2.5      | -       | MHz                          |
| <b>OUTPUT CHARACTERISTICS</b>              |       |              |          |         |              |          |         |                              |
| Output Voltage Swing (Note 6)              | +25°C | $\pm 10$     | $\pm 12$ | -       | $\pm 10$     | $\pm 12$ | -       | V                            |
|  | Full  | $\pm 10$     | -        | -       | $\pm 10$     | -        | -       | V                            |
| Full Power Bandwidth (Note 7)              | +25°C | 8            | 10       | -       | 8            | 10       | -       | kHz                          |
| Output Current (Note 8)                    | +25°C | $\pm 15$     | $\pm 20$ | -       | $\pm 15$     | $\pm 20$ | -       | mA                           |
| Output Resistance (Note 8)                 | +25°C | -            | 45       | -       | -            | 45       | -       | $\Omega$                     |
| <b>TRANSIENT RESPONSE (Note 10)</b>        |       |              |          |         |              |          |         |                              |
| Rise Time                                  | +25°C | -            | 340      | -       | -            | 340      | -       | ns                           |
| Slew Rate                                  | +25°C | 0.5          | 0.8      | -       | 0.5          | 0.8      | -       | $\text{V}/\mu\text{s}$       |
| Settling Time (Note 11)                    | +25°C | -            | 11       | -       | -            | 11       | -       | $\mu\text{s}$                |
| <b>POWER SUPPLY CHARACTERISTICS</b>        |       |              |          |         |              |          |         |                              |
| Supply Current                             | Full  | -            | 1.0      | 1.3     | -            | 1.0      | 1.7     | mA                           |
| Power Supply Rejection Ratio (Note 12)     | Full  | 100          | 130      | -       | 94           | 130      | -       | dB                           |

#### NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at  $6.8\text{mW}/^\circ\text{C}$  for operation at ambient temperatures above  $+75^\circ\text{C}$ .
3. Not tested, 90% of units meet or exceed these specifications.
4.  $V_{OUT} = \pm 10\text{V}$ ;  $R_L = 2\text{K}$ .  
 Gain  $\text{dB} = 20 \log_{10} A_v$   
 $\therefore 120\text{dB} = 1\text{MV}/\text{V}$   
 $140\text{dB} = 10\text{MV}/\text{V}$
5.  $V_{CM} = \pm 10\text{V DC}$
6.  $R_L = 600\Omega$ .
7.  $R_L = 2\text{K}$ ; Full power bandwidth guaranteed based on slew rate measurement using  $\text{FPBW} = \frac{\text{SLEW RATE}}{2\pi V_{PEAK}}$
8.  $V_{OUT} = 10\text{V}$
9. Output resistance measured under open loop conditions ( $f = 100\text{Hz}$ ).
10. Refer to test circuits section of the data sheet.
11. Settling time is measured to 0.1% of final value for a 10V output step and  $A_v = -1$ .
12.  $V_{SUPPLY} = \pm 5\text{V DC}$  to  $\pm 20\text{V DC}$ .

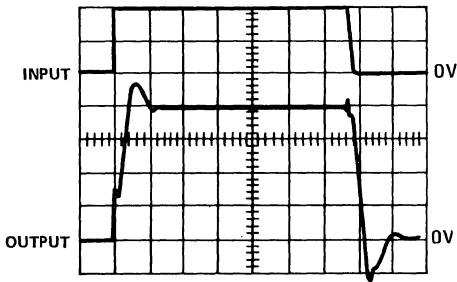
Test Circuits

SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



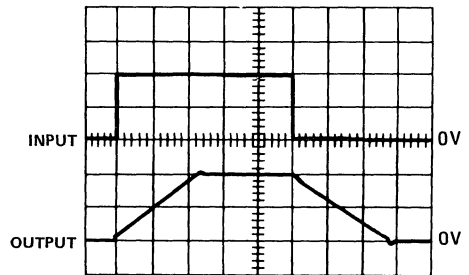
SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: 50mV/Div. Output)  
 (Volts: 100mV/Div. Input)  
 Horizontal Scale: (Time: 1μs/Div.)

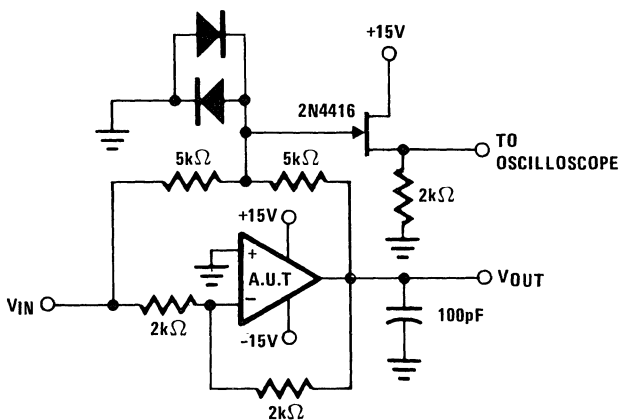


LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: 5V/Div.)  
 Horizontal Scale: (Time: 5μs/Div.)



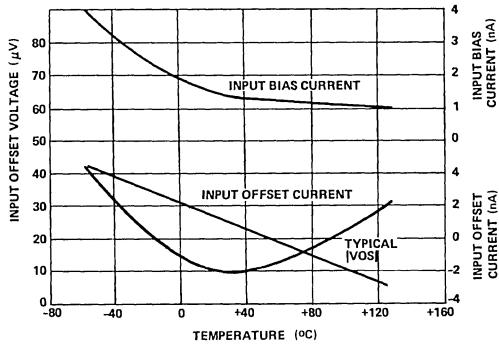
SETTLING TIME CIRCUIT



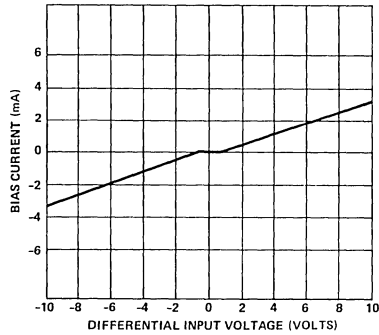
- $A_V = -1$ .
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

Typical Performance Curves

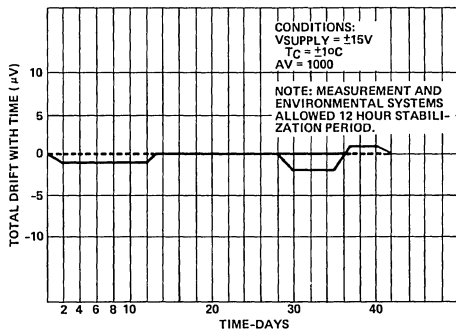
INPUT OFFSET VOLTAGE, INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



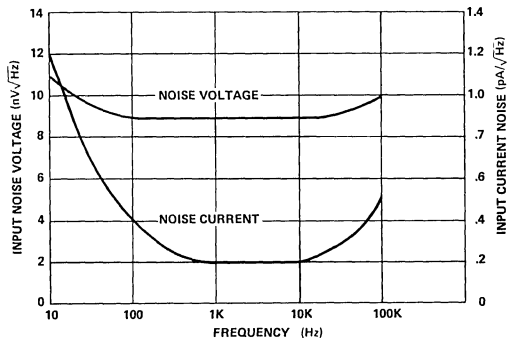
INPUT BIAS CURRENT vs. DIFFERENTIAL INPUT VOLTAGE



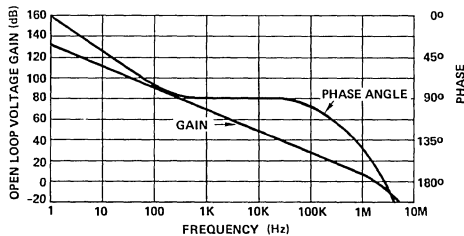
HA-5130 OFFSET VOLTAGE STABILITY vs. TIME



INPUT NOISE vs. FREQUENCY

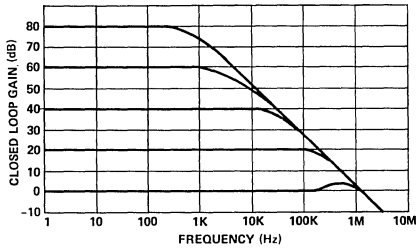


OPEN LOOP FREQUENCY RESPONSE

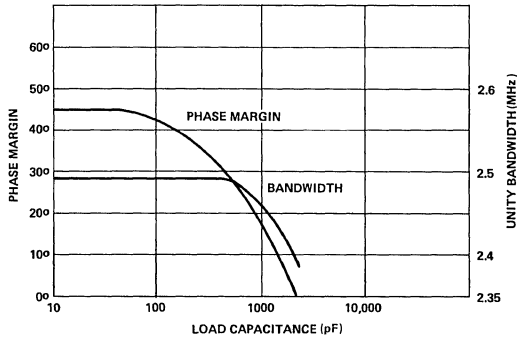


**Typical Performance Curves (Continued)**

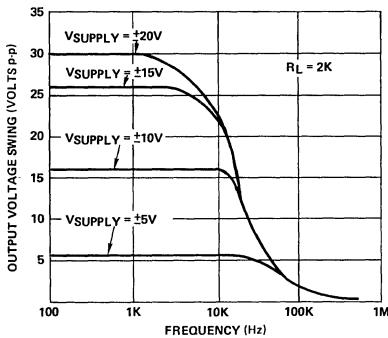
**CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS**



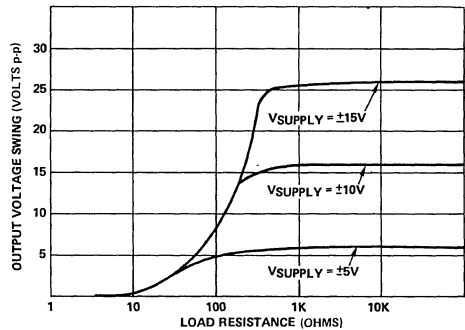
**SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE**



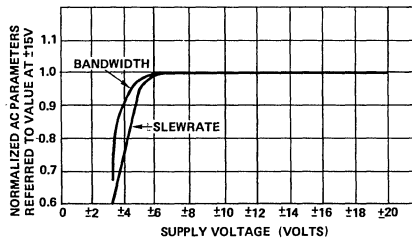
**OUTPUT VOLTAGE SWING vs. FREQUENCY AND SUPPLY VOLTAGE**



**MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE AND SUPPLY VOLTAGE**

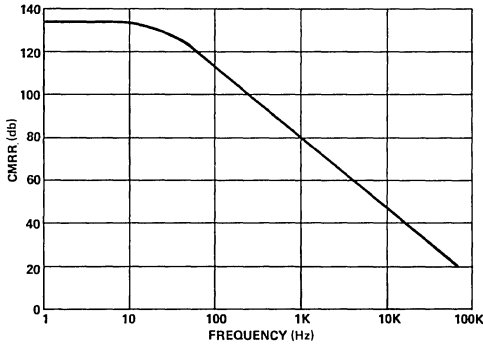


**NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE**

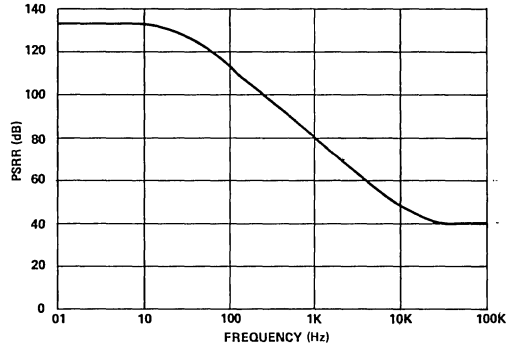


Typical Performance Curves (Continued)

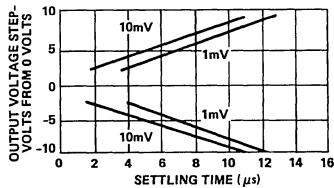
CMRR vs. FREQUENCY



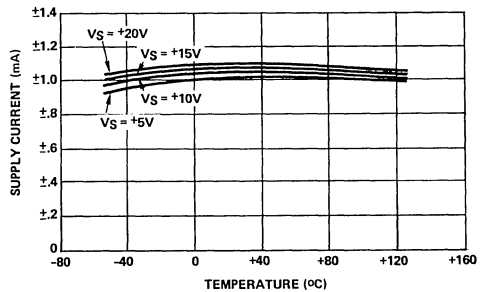
PSRR vs. FREQUENCY



SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



POWER SUPPLY CURRENT vs. TEMPERATURE AND SUPPLY VOLTAGE



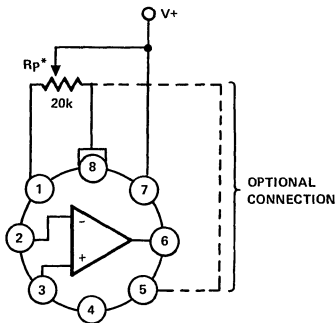
Applying the HA-5130/5135 Operational Amplifiers

- POWER SUPPLY DECOUPLING:** Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01 μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
- CONSIDERATIONS FOR PROTOTYPING:** The following list of recommendations are suggested for prototyping.
  - Resolving low level signals requires minimizing leakage currents caused by external circuitry. Use of quality insulating materials, thorough cleaning of insulating surfaces and implementation of moisture barriers when required is suggested.
  - Error voltages generated by thermocouples formed between dissimilar metals in the presence of temperature gradients should be minimized. Isolation of low level circuitry from heat generating components is recommended.
  - Shielded cable input leads, guard rings and shield drivers are recommended for the most critical applications.
- When driving large capacitive loads (> 500pF), a small value resistor (≈ 50Ω) should be connected in series with the output and inside the feedback loop.
- OFFSET VOLTAGE ADJUSTMENT:** A 20kΩ balance potentiometer is recommended if offset nulling is required. However, other potentiometer values such as 10kΩ, 50kΩ and 100kΩ may be used. The minimum adjustment range for given values is ±2mV.
- SATURATION RECOVERY:** Input and output saturation recovery time is negligible in most applications. However, care should be exercised to avoid exceeding the absolute maximum ratings of the device.
- DIFFERENTIAL INPUT VOLTAGES:** Inputs are shunted with back-to-back diodes for overvoltage protection. In applications where differential input voltages in excess of 1V are applied between the inputs, the use of limiting resistors at the inputs is recommended.



**Applications**

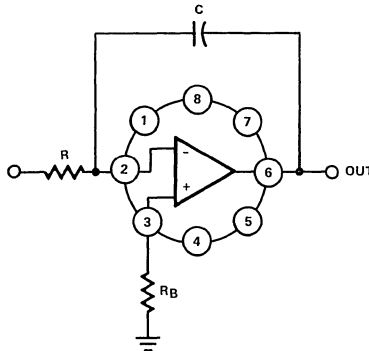
**OFFSET NULLING CONNECTIONS**



\* Although  $R_p$  is shown equal to 20K, other values such as 50K, 100K and 1M may be used. Range of adjustment is approximately  $\pm 2.5mV$ .  $V_{OS}$  TC of the amplifier is optimized at minimal  $V_{OS}$ .

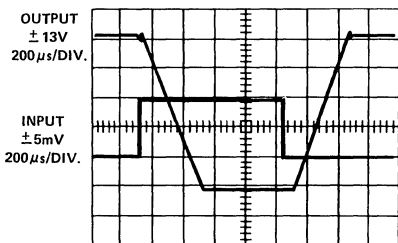
Tested Offset Adjustment is  $|V_{OS} + 1mV|$  minimum referred to output.

**PRECISION INTEGRATOR**

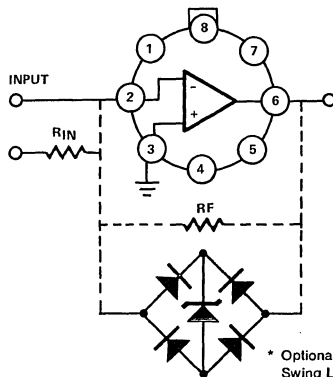


The excellent input and gain characteristics of HA-5130 are well suited for precision integrator applications. Accurate integration over seven decades of frequency using HA-5130, virtually nullifies the need for more expensive chopper-type amplifiers.

**ZERO CROSSING DETECTOR**

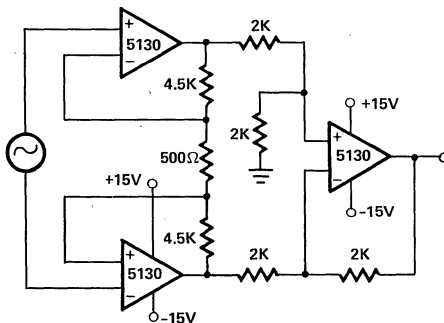


Low  $V_{OS}$  coupled with high open loop Gain, high CMRR and high PSRR make HA-5130 ideally suited for precision detector applications.



\* Optional for Output Swing Limiting

**PRECISION INSTRUMENTATION AMPLIFIER ( $A_v = 100$ )**



August 1991

## Precision Quad Operational Amplifier

### Features

- Low Offset Voltage ..... Max 200 $\mu$ V
- Low Offset Voltage Drift ..... Max 2 $\mu$ V/ $^{\circ}$ C
- Offset Voltage Match (5134A) .. Full Temp. Max 250 $\mu$ V
- High Channel Separation ..... 120dB
- Low Noise ..... 7nV/ $\sqrt{\text{Hz}}$
- Wide Unity Gain Bandwidth ..... 4MHz
- High CMRR/PSRR (Typ)..... 120dB
- Dielectric Isolation

### Description

The HA-5134 is a precision quad operational amplifier that is pin compatible with the OP-400, LT1014, OP11, RM4156, and LM148 as well as the HA-4741. Each amplifier features guaranteed maximum values for offset voltage of 200 $\mu$ V, offset voltage drift of 2 $\mu$ V/ $^{\circ}$ C, and offset current of 75nA over the full military temperature range while CMRR/PSRR is guaranteed greater than 94dB and AVOL is guaranteed above 750kV/V from -55 $^{\circ}$ C to +125 $^{\circ}$ C.

Precision performance of the HA-5134 is enhanced by a noise voltage density of 7nV/ $\sqrt{\text{Hz}}$  at 1kHz, noise current density of 1pA/ $\sqrt{\text{Hz}}$  at 1kHz and channel separation of 120dB. Each unity-gain stable quad amplifier is fabricated

### Applications

- Instrumentation Amplifiers
- State-Variable Filters
- Precision Integrators
- Threshold Detectors
- Precision Data Acquisition Systems
- Low-Level Transducer Amplifiers

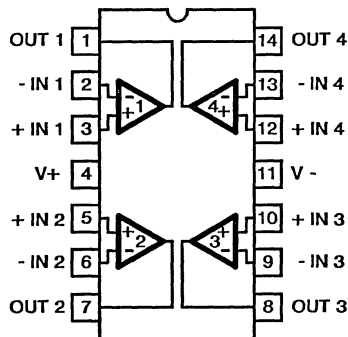
using the dielectric isolation process to assure performance in the most demanding applications.

The HA-5134 is ideal for compact circuits such as instrumentation amplifiers, state-variable filters, and low-level transducer amplifiers. Other applications include precision data acquisition, precision integrators, and accurate threshold detectors in designs where board space is a limitation.

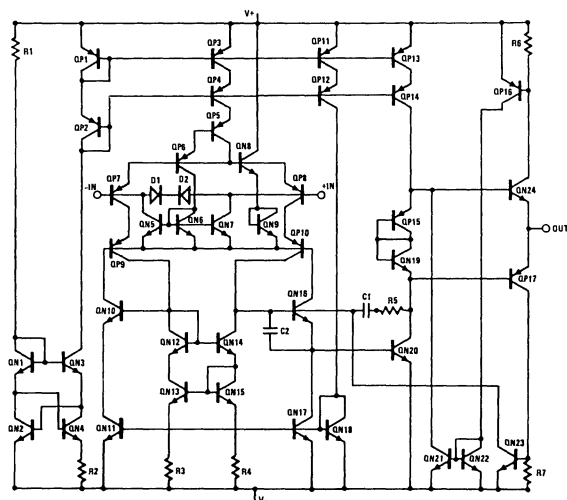
The HA-5134-2 has guaranteed operation from -55 $^{\circ}$ C to +125 $^{\circ}$ C and can be ordered as a military grade part. The HA-5134-5 is guaranteed from 0 $^{\circ}$ C to +75 $^{\circ}$ C and all devices are available in ceramic dual-in-line packages. For military grade product, refer to the HA-5134/883 Data Sheet.

### Pinout

HA1-5134 (CERAMIC DIP)  
TOP VIEW



### Schematic (Each Amplifier)



## Specifications HA-5134

### Absolute Maximum Ratings (Note 1)

|                                     |                               |
|-------------------------------------|-------------------------------|
| TA = +25°C Unless Otherwise Stated  |                               |
| Voltage Between V+ and V- Terminals | 40.0V                         |
| Differential Input Voltage (Note 2) | ±6.0V                         |
| Internal Power Dissipation (Note 3) | 800mW                         |
| Output Current                      | Full Short Circuit Protection |
| Voltage at any Op Amp Terminal      | V+, V-                        |
| Maximum Junction Temperature        | +175°C                        |

### Operating Temperature Ranges

|                           |                     |
|---------------------------|---------------------|
| HA-5134A/5134-2           | -55°C ≤ TA ≤ +125°C |
| HA-5134A/5134-5           | 0°C ≤ TA ≤ +75°C    |
| Storage Temperature Range | -65°C ≤ TA ≤ +150°C |

### Electrical Specifications VCC = ±15V, RLOAD = 2K, CLOAD = 50pF, RS ≤ 100Ω Unless Otherwise Specified

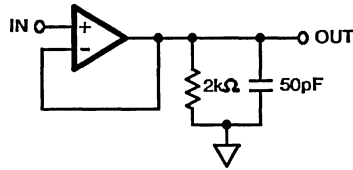
| PARAMETER                                   | TEMP  | HA-5134A-2/-5 |      |     | HA-5134-2/-5 |      |     | UNITS  |
|---|-------|---------------|------|-----|--------------|------|-----|--------|
|   |       | MIN           | TYP  | MAX | MIN          | TYP  | MAX |        |
| <b>INPUT CHARACTERISTICS</b>                |       |               |      |     |              |      |     |        |
| Offset Voltage                              | +25°C | -             | 50   | 100 | -            | 50   | 200 | μV     |
|   | Full  | -             | 75   | 250 | -            | 75   | 350 | μV     |
| Average Offset Voltage Drift                | Full  | -             | 0.3  | 1.2 | -            | 0.3  | 2   | μV/°C  |
| Offset Voltage Match                        | Full  | -             | -    | 250 | -            | -    | -   | μV     |
| Bias Current                                | +25°C | -             | ±10  | ±25 | -            | ±10  | ±50 | nA     |
|   | Full  | -             | ±20  | ±50 | -            | ±20  | ±75 | nA     |
| Offset Current                              | +25°C | -             | 10   | 25  | -            | 10   | 50  | nA     |
|   | Full  | -             | 15   | 50  | -            | 15   | 75  | nA     |
| Average Offset Current Drift                | Full  | -             | 0.05 | -   | -            | 0.05 | -   | nA/°C  |
| Common Mode Range                           | Full  | ±10           | -    | -   | ±10          | -    | -   | V      |
| Differential Input Resistance               | +25°C | -             | 30   | -   | -            | 30   | -   | MΩ     |
| Input Noise Voltage (0.1Hz to 10Hz)         | +25°C | -             | 0.2  | -   | -            | 0.2  | -   | μVp-p  |
| Input Noise Voltage Density                 | +25°C | f0 = 10Hz     | -    | 10  | -            | -    | 10  | nV/√Hz |
|   |       | f0 = 100Hz    | -    | 7.5 | -            | -    | 7.5 | nV/√Hz |
|   |       | f0 = 1kHz     | -    | 7   | -            | -    | 7   | nV/√Hz |
| Input Noise Current Density                 | +25°C | f0 = 10Hz     | -    | 3   | -            | -    | 3   | pA/√Hz |
|   |       | f0 = 100Hz    | -    | 1.5 | -            | -    | 1.5 | pA/√Hz |
|   |       | f0 = 1kHz     | -    | 1   | -            | -    | 1   | pA/√Hz |
| <b>TRANSFER CHARACTERISTICS</b>             |       |               |      |     |              |      |     |        |
| Large Signal Voltage Gain<br>(VOU = ±10V)   | +25°C | 1500          | 3000 | -   | 1200         | 3000 | -   | V/mV   |
|   | Full  | 1000          | 2000 | -   | 750          | 2000 | -   | V/mV   |
| Common Mode Rejection Ratio<br>(VCM = ±10V) | +25°C | 115           | 120  | -   | 100          | 120  | -   | dB     |
|   | Full  | 110           | 115  | -   | 94           | 115  | -   | dB     |
| Minimum Stable Gain                         | +25°C | 1             | -    | -   | 1            | -    | -   | V/V    |
| Unity-Gain Bandwidth                        | +25°C | -             | 4    | -   | -            | 4    | -   | MHz    |
| <b>OUTPUT CHARACTERISTICS</b>               |       |               |      |     |              |      |     |        |
| Output Voltage Swing                        | Full  | 12            | 13.5 | -   | 12           | 13.5 | -   | V      |
| Output Current                              | +25°C | -             | 20   | -   | -            | 20   | -   | mA     |
| Full Power Bandwidth (Note 4)               | +25°C | 12            | 16   | -   | 12           | 16   | -   | kHz    |
| Channel Separation (VOU = ±10V)             | +25°C | 120           | 136  | -   | 120          | 136  | -   | dB     |
| <b>TRANSIENT RESPONSE (Note 5)</b>          |       |               |      |     |              |      |     |        |
| Rise Time (Note 6)                          | +25°C | -             | 200  | 400 | -            | 200  | 400 | ns     |
| Slew Rate                                   | +25°C | 0.75          | 1.0  | -   | 0.75         | 1.0  | -   | V/μs   |
| Overshoot                                   | +25°C | -             | 20   | 40  | -            | 20   | 40  | %      |
| Settling Time (Note 7)                      | +25°C | -             | 13   | -   | -            | 13   | -   | μs     |
| <b>POWER SUPPLY CHARACTERISTICS</b>         |       |               |      |     |              |      |     |        |
| Supply Current (All Amps)                   | Full  | -             | 6.5  | 8   | -            | 6.5  | 8   | mA     |
| Power Supply Rejection Ratio (Note 8)       | +25°C | 110           | 120  | -   | 100          | 120  | -   | dB     |
|   | Full  | 100           | 115  | -   | 94           | 115  | -   | dB     |

#### NOTES:

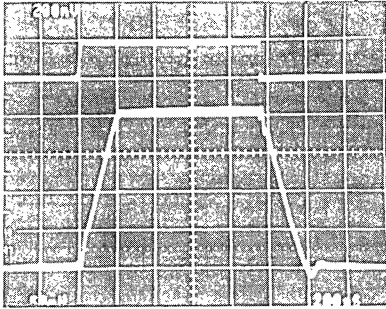
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For differential input voltages greater than 6V, the input current must be limited to 25mA to protect the back-to-back input diodes.
3. Derate at 10mW/°C for ambient temperatures greater than +95°C.
4. Full power bandwidth guaranteed based on slew rate measurement using  $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$ ;  $V_{peak} = 10V$
5. Refer to Test Circuits section of the data sheet.
6. Time from 10% to 90% of 200mV output step,  $A_V = 1$ .
7. Specified to 0.01% of a 10V step,  $A_V = -1$ .
8.  $V_S = \pm 5V$  to  $\pm 18V$ .

Test Circuits

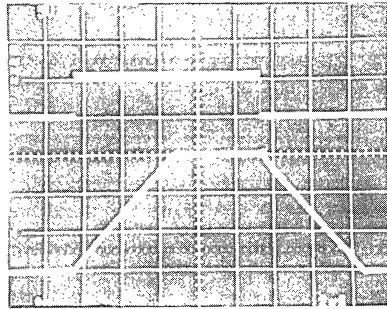
SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



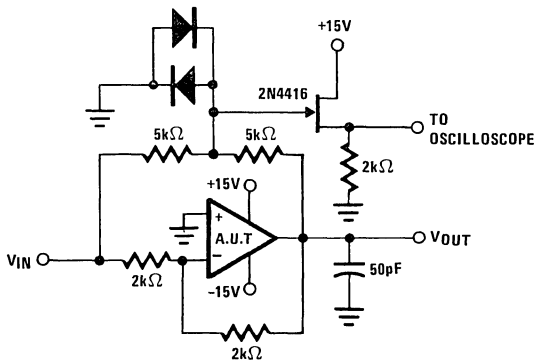
**SMALL SIGNAL RESPONSE**  
 Vertical: 50mV/Div. Horizontal: 200ns/Div.  
 $T_A = +25^\circ\text{C}$ ,  $V_{CC} = \pm 15\text{V}$   
 $A_V = +1$ ,  $R_L = 2\text{k}\Omega$ ,  $C_L = 50\text{pF}$



**LARGE SIGNAL RESPONSE**  
 Vertical: 2V/Div. Horizontal: 2μs/Div.  
 $T_A = +25^\circ\text{C}$ ,  $V_{CC} = \pm 15\text{V}$   
 $A_V = +1$ ,  $R_L = 2\text{k}\Omega$ ,  $C_L = 50\text{pF}$

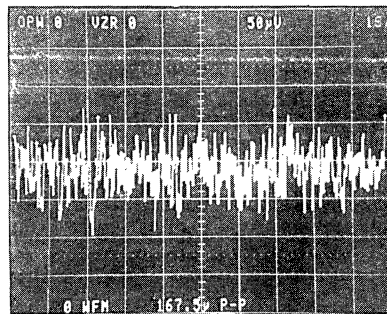


SETTLING TIME CIRCUIT



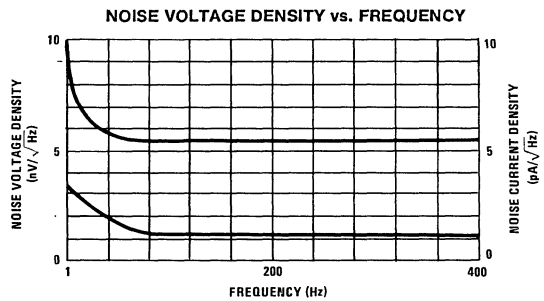
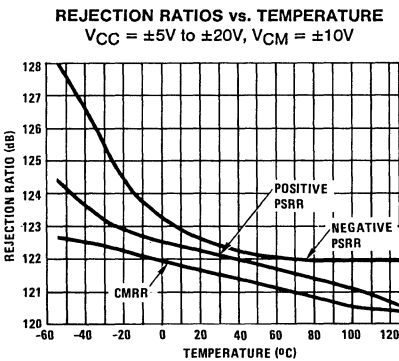
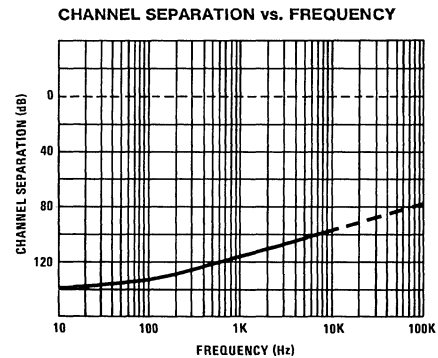
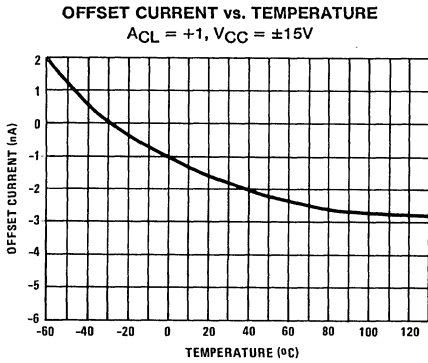
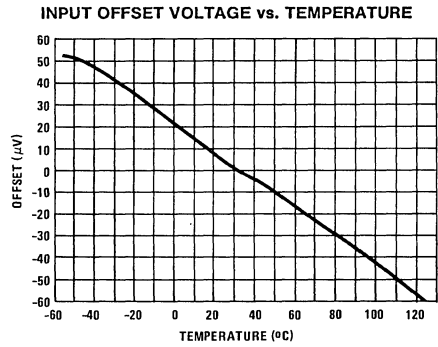
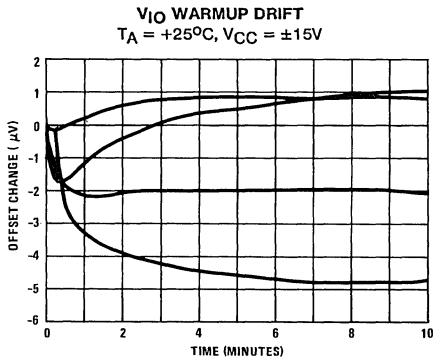
- $A_V = -1$ .
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

PEAK-TO-PEAK NOISE 0.1Hz TO 10Hz  
 $T_A = +25^\circ\text{C}$ ,  $V_{CC} = \pm 15\text{V}$ ,  $A_V = 1000$



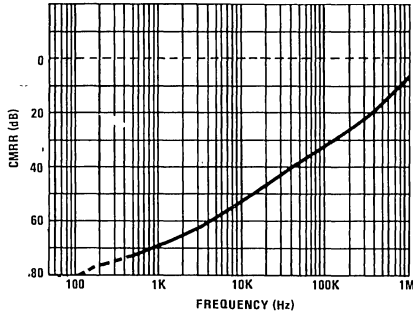
$e_{n-p-p} = 0.167\mu\text{V}_{p-p}$   
 0.05μV/Div., 1s/Div.

Performance Curves

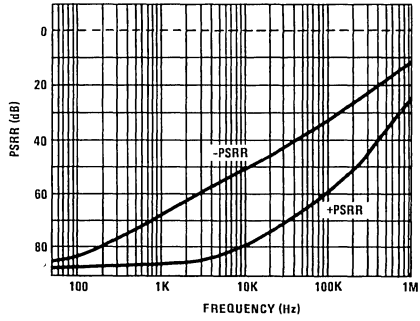


Performance Curves (Continued)

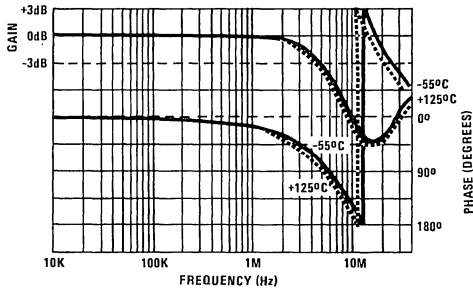
CMRR vs. FREQUENCY



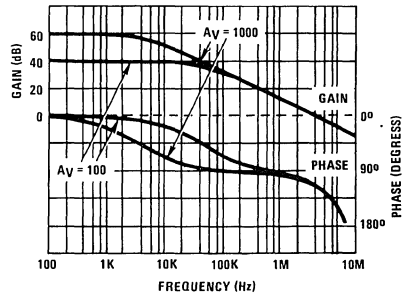
PSRR vs. FREQUENCY



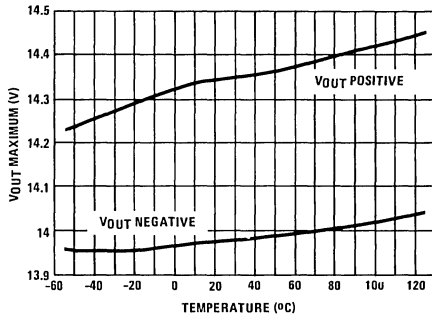
CLOSED-LOOP FREQUENCY RESPONSE vs. TEMPERATURE



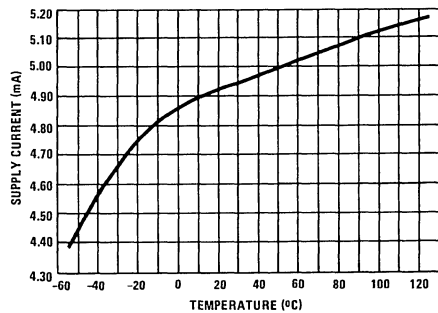
CLOSED-LOOP GAIN/PHASE vs. FREQUENCY  
T<sub>A</sub> = +25°C, V<sub>CC</sub> = ±15V



MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE  
R<sub>LOAD</sub> = 2K, A<sub>v</sub> = 1000, V<sub>IN</sub> = ±2V

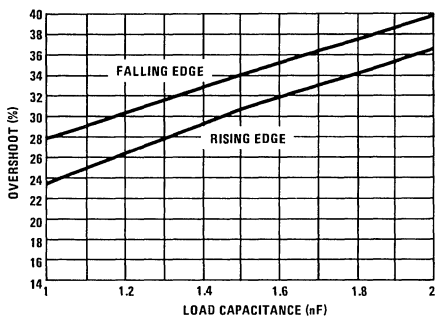


SUPPLY CURRENT vs. TEMPERATURE  
V<sub>CC</sub> = ±15V

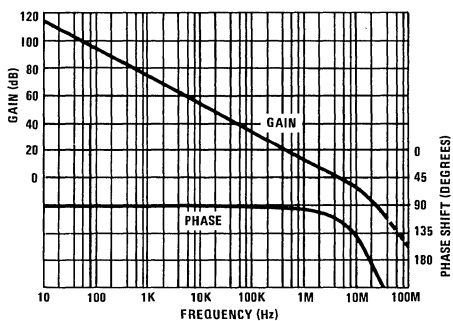


**Performance Curves (Continued)**

**OVERSHOOT vs. C<sub>LOAD</sub>**  
 $V_{CC} = \pm 15V, T_A = +25^\circ C, A_V = 1, V_{OUT} = 200mV$



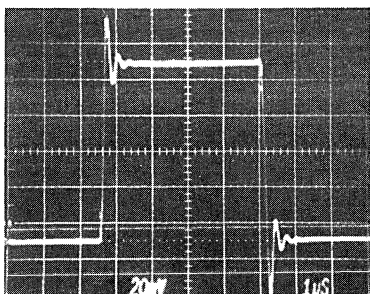
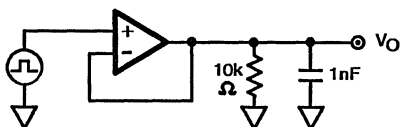
**OPEN LOOP GAIN & PHASE vs. FREQUENCY**



**Applications Information**

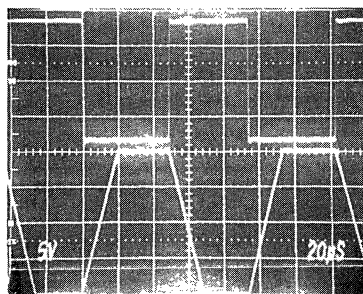
**SMALL SIGNAL TRANSIENT RESPONSE**

$C_{LOAD} = 1nF$



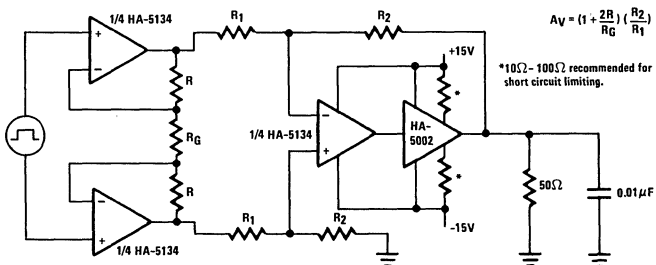
$T_A = +25^\circ C, V_{CC} = \pm 15V,$   
 $A_V = 1, R_L = 10K$   
 20mV/Div, 1μs/Div.

**TRANSIENT RESPONSE OF APPLICATION CIRCUIT #1**



$V_{OUT} = \pm 10V, R_{LOAD} = 50V$   
 $C_{LOAD} = 0.01mF, A_V = 3, V_{CC} = \pm 15V$   
 Top: Input, 2V/Div, 20μs/Div. Bottom: Output, 5V/Div, 20μs/Div.

**APPLICATION CIRCUIT #1:  
 INSTRUMENTATION AMPLIFIER WITH POWER OUTPUT**



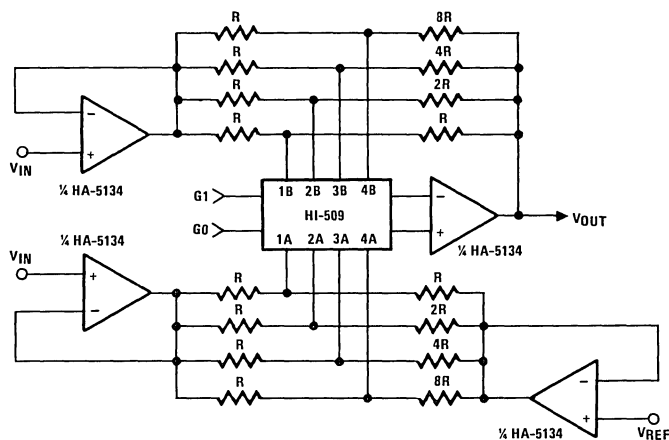
\*100Ω - 100Ω recommended for short circuit limiting.

**NOTE:** When driving heavy loads the HA-5002 may contribute to thermal errors. Proper thermal shielding is recommended.

# HA-5134

## Applications Information (Continued)

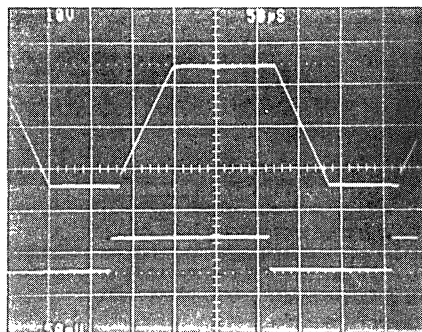
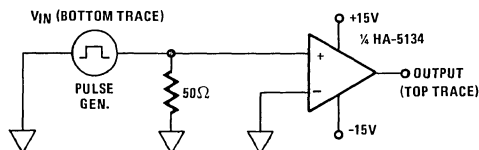
### APPLICATION CIRCUIT #2: PROGRAMMABLE GAIN AMPLIFIER



| G <sub>1</sub> | G <sub>0</sub> | A <sub>v</sub> |
|----------------|----------------|----------------|
| 0              | 0              | -1             |
| 0              | 1              | -2             |
| 1              | 0              | -4             |
| 1              | 1              | -8             |

High  $A_{VOL}$  of HA-5134 reduces gain error.  
Gain Error  $\approx 0.004\%$  @  $A_v = 8$

### APPLICATION CIRCUIT #3: PRECISION COMPARATOR



Horizontal: 50μs/Div.  
 $V_{IN} = \pm 25mV$ ,  $V_{OUT} = \pm 14V$

NOTE: If differential input voltages greater than 6V are present, input current must be limited to less than 25mA.

## General Considerations

- POWER SUPPLY DECOUPLING:** Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
- CONSIDERATIONS FOR PROTOTYPING:** The following list of recommendations are suggested for prototyping.
  - Resolving low level signals requires minimizing leakage currents caused by external circuitry. Use of quality insulating materials, thorough cleaning of insulating surfaces and implementation of moisture barriers when required is suggested.
  - Error voltages generated by thermocouples formed between dissimilar metals in the presence of temperature gradients should be minimized. Isolation of low level circuitry from heat generating components is recommended.
  - Shielded cable input leads, guard rings and shield drivers are recommended for the most critical applications.



## Ultra-Low Noise Precision Wideband Operational Amplifier

August 1991

### Features

- High Speed ..... 20V/ $\mu$ s
- Wide Gain Bandwidth ( $A_V \geq 5$ ) ..... 63MHz
- Low Noise ..... 3nV/ $\sqrt{\text{Hz}}$  at 1KHz
- Low VOS ..... 10 $\mu$ V
- High CMRR ..... 126dB
- High Gain ..... 1800V/mV

### Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers
- For Further Design Ideas See Application Note 553

### Description

The HA-5137 monolithic operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Harris D. I. technology and advanced processing techniques, this unique design unites low noise (3nV/ $\sqrt{\text{Hz}}$ ) precision instrumentation performance with high speed (20V/ $\mu$ s) wideband capability.

This amplifier's impressive list of features include low  $V_{OS}$  (10 $\mu$ V), wide gain-bandwidth (63MHz), high open loop gain (1800V/mV), and high CMRR (126dB). Additionally, this flexible device operates over a wide supply range ( $\pm 5$ V to  $\pm 20$ V) while consuming only 140mW of power.

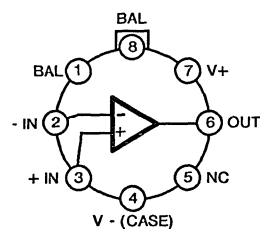
Using the HA-5137 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than five.

This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5137's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits.

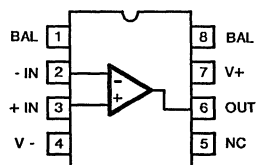
This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37 where gains are greater than five. The HA-5137 is available in TO-99 Metal Can and Ceramic 8 pin Mini- DIPs. For the military grade product, refer to the HA-5137/883 data sheet.

### Pinouts

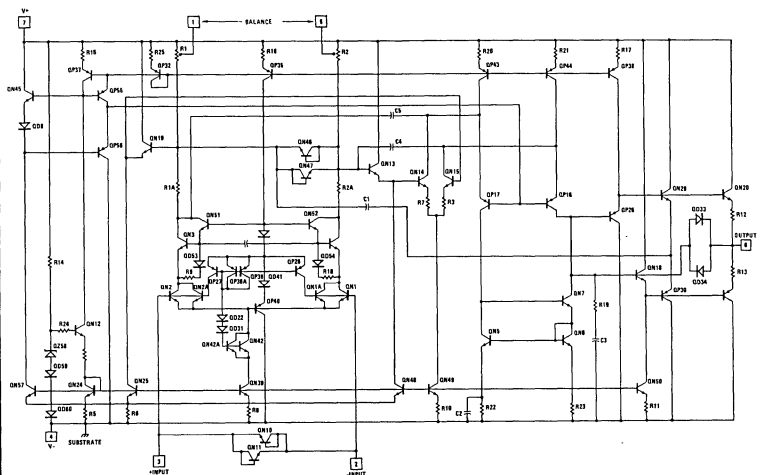
HA2-5137 (TO-99 METAL CAN)  
TOP VIEW



HA7-5137 (CERAMIC MINI-DIP)  
TOP VIEW



### Schematic



## Specifications HA-5137

### Absolute Maximum Ratings (Note 1)

|   |                               |
|---|-------------------------------|
| $T_A = +25^\circ\text{C}$ Unless Otherwise Stated |                               |
| Voltage Between V+ and V- Terminals               | $\pm 22\text{V}$              |
| Differential Input Voltage (Note 2)               | $\pm 0.7\text{V}$             |
| Internal Power Dissipation                        | 500mW                         |
| Output Current                                    | Full Short Circuit Protection |

### Operating Temperature Ranges

|                              |  |
|------------------------------|--|
| HA-5137/37A-2                | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ |
| HA-5137/37A-5                | $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$    |
| Storage Temperature Range    | $-65^\circ\text{C} \leq T_A \leq +150^\circ\text{C}$ |
| Maximum Junction Temperature | $+175^\circ\text{C}$                                 |

### Electrical Specifications $V_+ = 15\text{V}$ , $V_- = -15\text{V}$ , $C_L \leq 50\text{pF}$ , $R_S \leq 100\Omega$

| PARAMETER                                    | TEMP                    | HA-5137A   |            |            | HA-5137    |            |            | UNITS                        |   |
|--|-------------------------|------------|------------|------------|------------|------------|------------|------------------------------|---|
|  |                         | MIN        | TYP        | MAX        | MIN        | TYP        | MAX        |                              |   |
| <b>INPUT CHARACTERISTICS</b>                 |                         |            |            |            |            |            |            |                              |   |
| Offset Voltage                               | +25°C                   | -          | 10         | 25         | -          | 30         | 100        | $\mu\text{V}$                |   |
|  | Full                    | -          | 30         | 60         | -          | 70         | 300        | $\mu\text{V}$                |   |
| Average Offset Voltage Drift                 | Full                    | -          | 0.2        | 0.6        | -          | 0.4        | 1.8        | $\mu\text{V}/^\circ\text{C}$ |   |
| Bias Current                                 | +25°C                   | -          | $\pm 10$   | $\pm 40$   | -          | $\pm 15$   | $\pm 80$   | nA                           |   |
|  | Full                    | -          | $\pm 20$   | $\pm 60$   | -          | $\pm 35$   | $\pm 150$  | nA                           |   |
| Offset Current                               | +25°C                   | -          | 7          | 35         | -          | 12         | 75         | nA                           |   |
|  | Full                    | -          | 15         | 50         | -          | 30         | 135        | nA                           |   |
| Common Mode Range                            | Full                    | $\pm 10.3$ | $\pm 11.5$ | -          | $\pm 10.3$ | $\pm 11.5$ | -          | V                            |   |
| Differential Input Resistance (Note 3)       | +25°C                   | 1.5        | 6          | -          | 0.8        | 4          | -          | M $\Omega$                   |   |
| Input Noise Voltage 0.1 Hz to 10 Hz (Note 4) | +25°C                   | -          | 0.08       | 0.18       | -          | 0.09       | 0.25       | $\mu\text{Vp-p}$             |   |
| Input Noise Voltage Density (Note 5)         | +25°C                   | -          | 3.5        | 5.5        | -          | 3.8        | 8.0        | $\text{nV}/\sqrt{\text{Hz}}$ |   |
|  | $f_0 = 30\text{Hz}$     | -          | 3.1        | 4.5        | -          | 3.3        | 5.6        | $\text{nV}/\sqrt{\text{Hz}}$ |   |
|  | $f_0 = 1000\text{Hz}$   | -          | 3.0        | 3.8        | -          | 3.2        | 4.5        | $\text{nV}/\sqrt{\text{Hz}}$ |   |
| Input Noise Current Density (Note 5)         | +25°C                   | -          | 1.7        | 4.0        | -          | 1.7        | -          | $\text{pA}/\sqrt{\text{Hz}}$ |   |
|  | $f_0 = 30\text{Hz}$     | -          | 1.0        | 2.3        | -          | 1.0        | -          | $\text{nV}/\sqrt{\text{Hz}}$ |   |
|  | $f_0 = 1000\text{Hz}$   | -          | 0.4        | 0.6        | -          | 0.4        | 0.6        | $\text{nV}/\sqrt{\text{Hz}}$ |   |
| <b>TRANSFER CHARACTERISTICS</b>              |                         |            |            |            |            |            |            |                              |   |
| Large Signal Voltage Gain (Note 6)           | +25°C                   | 1000       | 1800       | -          | 700        | 1500       | -          | V/mV                         |   |
|  | Full                    | 600        | 1200       | -          | 300        | 800        | -          | V/mV                         |   |
| Common Mode Rejection Ratio (Note 7)         | Full                    | 114        | 126        | -          | 100        | 120        | -          | dB                           |   |
| Minimum Stable Gain                          | +25°C                   | 5          | -          | -          | 5          | -          | -          | V/V                          |   |
| Gain-Bandwidth-Product                       | +25°C                   | 60         | 80         | -          | 60         | 80         | -          | MHz                          |   |
|  | $f_0 = 1\text{MHz}$     | -          | 63         | -          | -          | 63         | -          | MHz                          |   |
| <b>OUTPUT CHARACTERISTICS</b>                |                         |            |            |            |            |            |            |                              |   |
| Output Voltage Swing                         | $R_L = 600\Omega$       | +25°C      | $\pm 10.0$ | $\pm 11.5$ | -          | $\pm 10.0$ | $\pm 11.5$ | -                            | V |
|  | $R_L = 2\text{K}\Omega$ | Full       | $\pm 11.7$ | $\pm 13.8$ | -          | $\pm 11.4$ | $\pm 13.5$ | -                            | V |
| Full Power Bandwidth (Note 8)                | +25°C                   | 220        | 320        | -          | 220        | 320        | -          | KHz                          |   |
| Output Resistance, Open Loop                 | +25°C                   | -          | 70         | -          | -          | 70         | -          | $\Omega$                     |   |
| Output Current                               | +25°C                   | 16.5       | 25         | -          | 16.5       | 25         | -          | mA                           |   |
| <b>TRANSIENT RESPONSE (Note 9)</b>           |                         |            |            |            |            |            |            |                              |   |
| Rise Time                                    | +25°C                   | -          | -          | 100        | -          | -          | 100        | ns                           |   |
| Slew Rate (Note 11)                          | +25°C                   | 14         | 20         | -          | 14         | 20         | -          | V/ $\mu\text{s}$             |   |
| Settling Time (Note 10)                      | +25°C                   | -          | 1.0        | -          | -          | 1.0        | -          | $\mu\text{s}$                |   |
| Overshoot                                    | +25°C                   | -          | 20         | 40         | -          | 20         | 40         | %                            |   |
| <b>POWER SUPPLY CHARACTERISTICS</b>          |                         |            |            |            |            |            |            |                              |   |
| Supply Current                               | +25°C                   | -          | 3.5        | -          | -          | 3.5        | -          | mA                           |   |
|  | Full                    | -          | -          | 4.0        | -          | -          | 4.0        | mA                           |   |
| Power Supply Rejection Ratio (Note 12)       | Full                    | -          | 2          | 4          | -          | 16         | 51         | $\mu\text{V}/\text{V}$       |   |

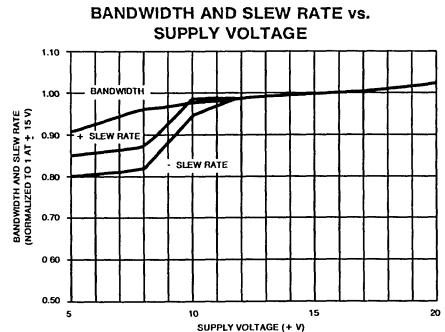
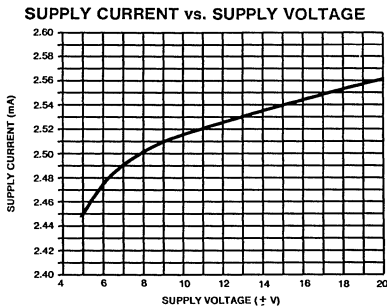
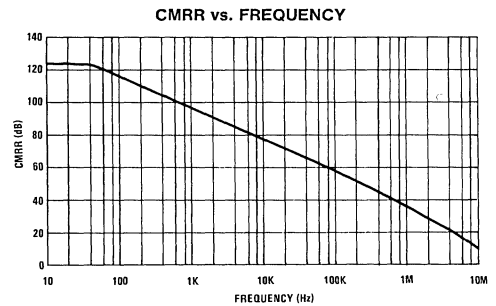
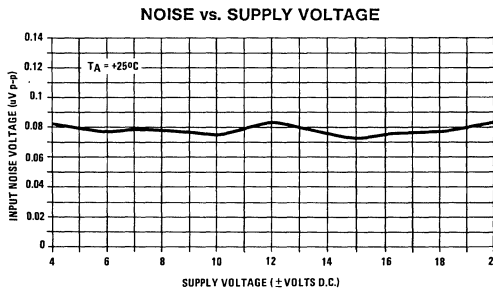
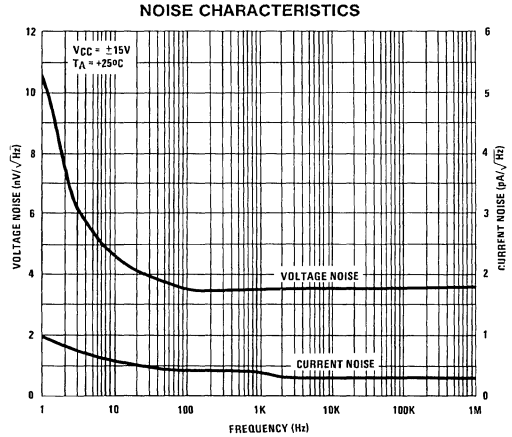
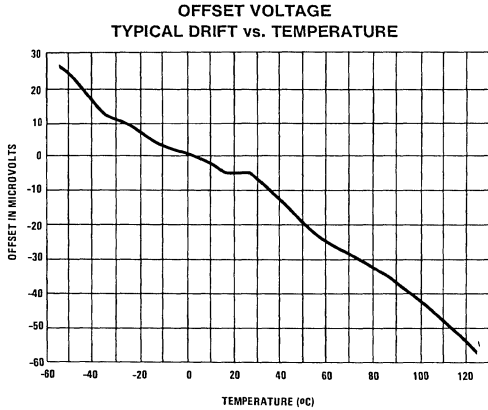
3  
OPERATIONAL  
AMPLIFIERS

# HA-5137

## NOTES:

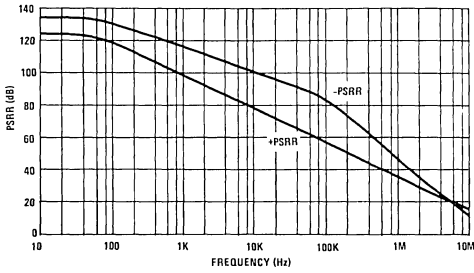
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.
3. This parameter value is based upon design calculations.
4. Refer to Typical Performance section of the data sheet.
5. Sample tested.
6.  $V_{OUT} = \pm 10V$ ,  $R_L = 2k\Omega$
7.  $V_{CM} = \pm 10V$
8. Full power bandwidth guaranteed based on slew rate measurement using:  $FPBW = \frac{\text{Slew Rate}}{2\pi V_{Peak}}$
9. Refer to Test Circuits section of the data sheet.
10. Settling time is specified to 0.1% of final value for a 10V output step and  $A_V = -5$ .
11.  $V_{OUT} = 10V$  Step
12.  $V_S = \pm 4V$  to  $\pm 18V$

## Typical Performance Unless Otherwise Specified: $T_A = +25^\circ C$ , $V_{SUPPLY} = \pm 15V$

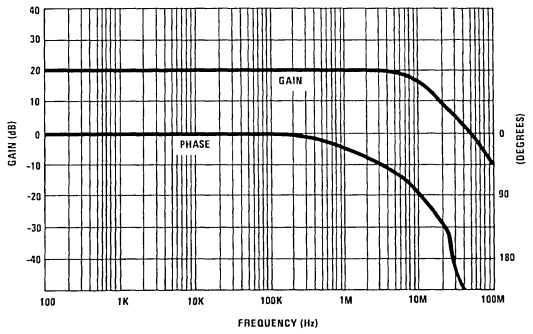


**Typical Performance Curves** Unless Otherwise Specified:  $T_A = +25^\circ\text{C}$ ,  $V_{\text{SUPPLY}} = \pm 15\text{V}$

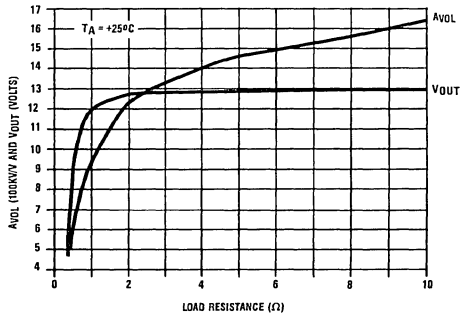
**PSRR vs. FREQUENCY**



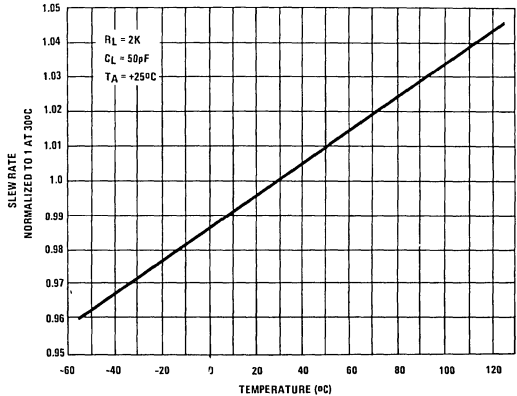
**CLOSED LOOP GAIN AND PHASE vs. FREQUENCY**



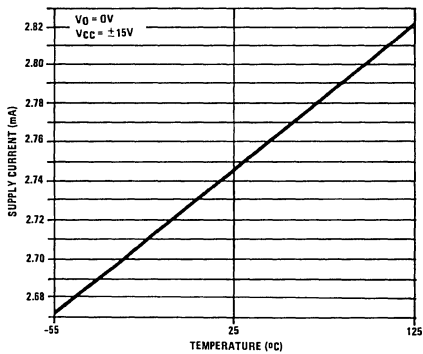
**AVOL AND VOUT vs. LOAD RESISTANCE**



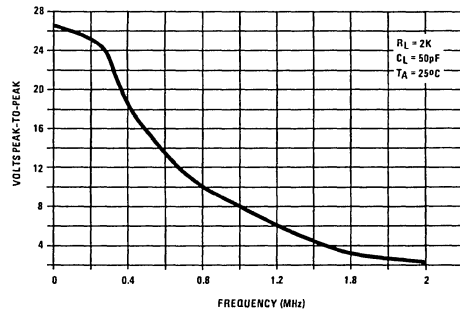
**NORMALIZED SLEW RATE vs. TEMPERATURE**



**SUPPLY CURRENT vs. TEMPERATURE**

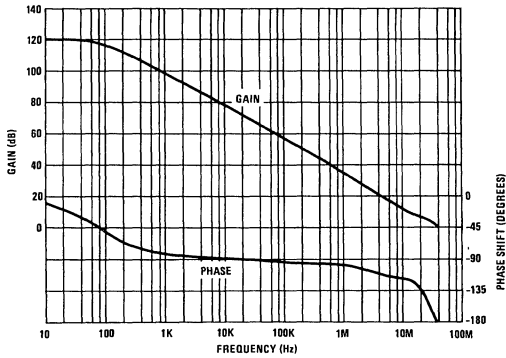


**VOUT MAX vs. FREQUENCY  
UNDISTORTED SINEWAVE OUTPUT**

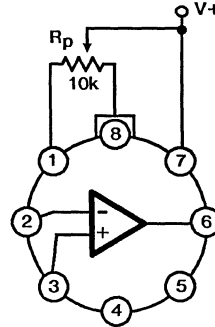


**Typical Performance Curves** Unless Otherwise Specified:  $T_A = +25^\circ\text{C}$ ,  $V_{\text{SUPPLY}} = \pm 15\text{V}$

OPEN LOOP GAIN AND PHASE vs. FREQUENCY

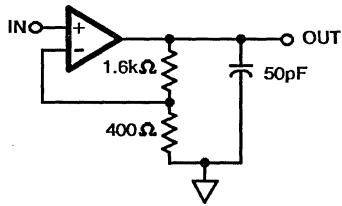


SUGGESTED OFFSET VOLTAGE ADJUSTMENT

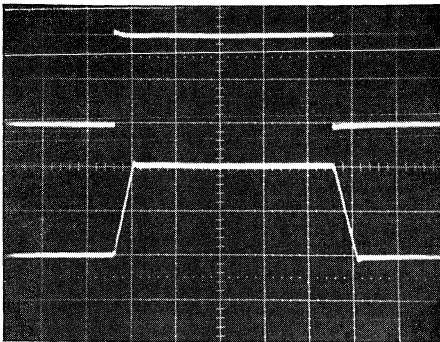


Test Offset Adjustment Range is  $|V_{OS} + 1\text{mV}|$  minimum referred to output.  
Typical range is  $\pm 4\text{mV}$  with  $R_p = 10\text{k}\Omega$ .

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT

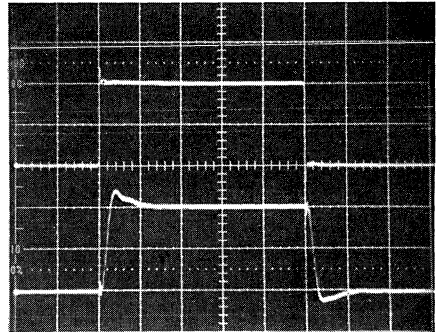


LARGE SIGNAL RESPONSE



Vertical Scale: (Volts: Input = 1V/Div.)  
(Volts: Output = 5V/Div.)  
Horizontal Scale: (Time = 1μs/Div.)

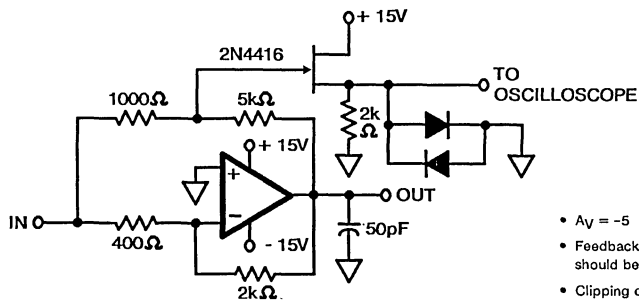
SMALL SIGNAL RESPONSE



Vertical Scale: (Volts: Input = 20mV/Div.)  
(Volts: Output = 100mV/Div.)  
Horizontal Scale: (Time = 100ns/Div.)

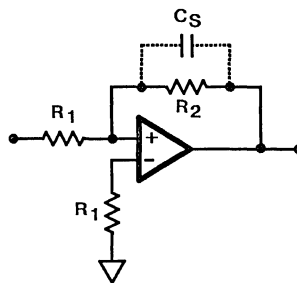
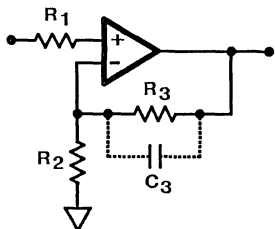
**Typical Performance Curves (Continued)** Unless Otherwise Specified:  $T_A = +25^\circ\text{C}$ ,  $V_{\text{SUPPLY}} = \pm 15\text{V}$

**SETTLING TIME TEST CIRCUIT**



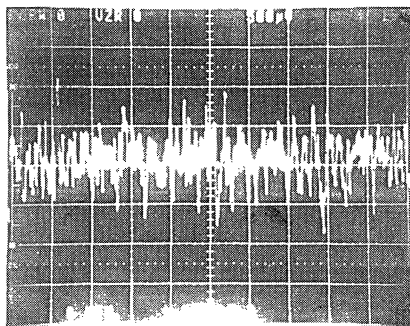
- $A_v = -5$
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

**SUGGESTED STABILITY CIRCUITS**



Low resistances are preferred for low noise applications as a 1KΩ resistor has  $4nV\sqrt{\text{Hz}}$  of thermal noise. Total resistances of greater than 10KΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

**0.1Hz TO 10Hz NOISE WITH  $A_{CL} = 25,000\text{V/V}$**



Horizontal Scale = 1 sec/Div.  
Vertical Scale = 0.002μV/Div.  
0.08μVp-p

**Die Characteristics**

|                            |   |               |
|----------------------------|---|---------------|
| Transistor Count .....     | 63  |               |
| Die Dimensions .....       | 65 x 104.3 x 19 mils<br>(1700μm x 2600μm x 480μm) |               |
| Substrate Potential* ..... | V-  |               |
| Process .....              | Bipolar-DI  |               |
| Thermal Constants (°C/W)   | $\theta_{ja}$                                     | $\theta_{jc}$ |
| HA7-5137 Ceramic Mini-DIP  | 160   | 79            |
| HA2-5137 TO-99 Metal Can   | 172   | 48            |

\*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

August 1991

### Features

- Low Supply Current ..... 45 $\mu$ A/Amp
- Wide Supply Voltage Range ..... Single 3V to 30V or Dual  $\pm$ 1.5V to  $\pm$ 15V
- High Slew Rate ..... 1.5V/ $\mu$ s
- High Gain ..... 100kV/V
- Unity Gain Stable
- Available in Duals and Quads

### Applications

- Portable Instruments
- Meter Amplifiers
- Telephone Headsets
- Microphone Amplifiers
- Instrumentation
- For Further Design Ideas See Application Note 544

### Description

The HA-5142/44 ultra-low power operational amplifiers provide AC and DC performance characteristics similar to or better than most general purpose amplifiers while only drawing 1/30 of the supply current of most general purpose amplifiers. In applications which require low power dissipation and good A.C. electrical characteristics, this family offers the industry's best speed/power ratio.

The HA-5142/44 provides accurate signal processing by virtue of their low input offset voltage (2mV), low input bias current (45nA), high open loop gain (100kV/V) and low noise, for low power operational amplifiers (20nV/ $\sqrt$ Hz). These characteristics coupled with a 1.5V/ $\mu$ s slew rate and

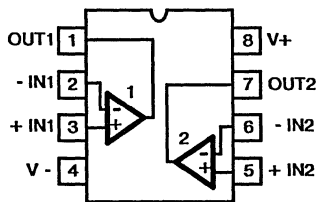
a 400kHz bandwidth make the HA-5142/44 ideal for use in low power instrumentation, audio amplifier and active filter designs. The wide range of supply voltages (3V to 30V) also allow these amplifiers to be very useful in low voltage battery powered equipment. These parts are also tested and guaranteed at both  $\pm$ 15V and single ended +5V supplies.

These amplifiers are available in duals (HA-5142, SOIC, Can or Mini-DIP) or quads (HA-5144, SOIC or DIP) with industry standard pinouts which allow the HA-5142/5144's to be interchangeable with most other operational amplifiers. For military grade product refer to the 5142, 5144/883 data sheet.

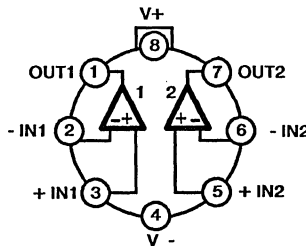
### Pinouts

#### TOP VIEWS

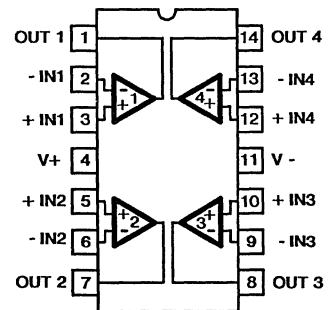
HA3-5142 (PLASTIC MINI-DIP)  
HA7-5142 (CERAMIC DIP)



HA2-5142 (TO-99 METAL CAN)



HA1-5144 (CERAMIC DIP)  
HA3-5144 (PLASTIC DIP)



## Specifications HA-5142/44

### Absolute Maximum Ratings (Note 1)

|   |               |
|---|---------------|
| Voltage Between V+ and V- Terminals ..... | 35V           |
| Differential Input Voltage .....          | ±7V           |
| Output Current .....                      | S/C Protected |
| Internal Power Dissipation .....          | 500mW         |

### Operating Temperature Range

|                                    |  |
|------------------------------------|--|
| HA-5142/44-5 .....                 | $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$    |
| HA-5142/44-2 .....                 | $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ |
| HA-5142/44-9 .....                 | $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  |
| Storage Temperature Range .....    | $-65^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ |
| Maximum Junction Temperature ..... | +175°C   |

**Electrical Specifications**  $R_S = 100\Omega$ ,  $C_L \leq 10\text{pF}$  Unless Otherwise Specified.

| PARAMETER                              | TEMP  | -2, -5<br>V+ = +5V, V- = 0V |            |     | -2, -5<br>V+ = +15V, V- = -15V |      |     | UNITS                          |
|--|-------|-----------------------------|------------|-----|--------------------------------|------|-----|--------------------------------|
|  |       | MIN                         | TYP        | MAX | MIN                            | TYP  | MAX |                                |
| <b>INPUT CHARACTERISTICS</b>           |       |                             |            |     |                                |      |     |                                |
| Offset Voltage (Note 11)               | +25°C | -                           | 2          | 6   | -                              | 2    | 6   | mV                             |
|  | Full  | -                           | -          | 8   | -                              | -    | 8   | mV                             |
| Average Offset Voltage Drift           | Full  | -                           | 3          | -   | -                              | 3    | -   | $\mu\text{V}/^{\circ}\text{C}$ |
| Bias Current (Note 11)                 | +25°C | -                           | 45         | 100 | -                              | 45   | 100 | nA                             |
|  | Full  | -                           | -          | 125 | -                              | -    | 125 | nA                             |
| Offset Current (Note 11)               | +25°C | -                           | 0.3        | 10  | -                              | 0.3  | 10  | nA                             |
|  | Full  | -                           | -          | 20  | -                              | -    | 20  | nA                             |
| Common Mode Range                      | Full  | 0 to 3                      | -          | -   | ±10                            | -    | -   | V                              |
| Differential Input Resistance          | +25°C | -                           | 0.6        | -   | -                              | 0.6  | -   | MΩ                             |
| Input Noise Voltage (f = 1kHz)         | +25°C | -                           | 20         | -   | -                              | 20   | -   | $\text{nV}/\sqrt{\text{Hz}}$   |
| Input Noise Current (f = 1kHz)         | +25°C | -                           | 0.25       | -   | -                              | 0.25 | -   | $\text{pA}/\sqrt{\text{Hz}}$   |
| <b>TRANSFER CHARACTERISTICS</b>        |       |                             |            |     |                                |      |     |                                |
| Large Signal Voltage Gain (Notes 2, 4) | +25°C | 20k                         | 100k       | -   | 20k                            | 100k | -   | V/V                            |
|  | Full  | 15k                         | -          | -   | 15k                            | -    | -   | V/V                            |
| Common Mode Rejection Ratio (Note 7)   | Full  | 77                          | 105        | -   | 77                             | 105  | -   | dB                             |
| Bandwidth (Notes 2, 3)                 | +25°C | -                           | 0.4        | -   | -                              | 0.4  | -   | MHz                            |
| <b>OUTPUT CHARACTERISTICS</b>          |       |                             |            |     |                                |      |     |                                |
| Output Voltage Swing (Notes 2, 10)     | +25°C | 1.0 to 3.8                  | 0.7 to 4.2 | -   | ±10                            | ±13  | -   | V                              |
|  | Full  | 1.2 to 3.5                  | 0.9 to 4.0 | -   | ±10                            | ±13  | -   | V                              |
| Full Power Bandwidth (Notes 2, 4, 8)   | +25°C | -                           | 240        | -   | -                              | 24   | -   | kHz                            |
| <b>TRANSIENT RESPONSE (Notes 2, 3)</b> |       |                             |            |     |                                |      |     |                                |
| Rise Time                              | +25°C | -                           | 600        | -   | -                              | 600  | -   | ns                             |
| Slew Rate (Note 6)                     | +25°C | 0.8                         | 1.5        | -   | 0.8                            | 1.5  | -   | V/μs                           |
| Settling Time (Note 5)                 | +25°C | -                           | 10         | -   | -                              | 10   | -   | μs                             |
| <b>POWER SUPPLY CHARACTERISTICS</b>    |       |                             |            |     |                                |      |     |                                |
| Supply Current                         | +25°C | -                           | 45         | 80  | -                              | 100  | 150 | μA/Amp                         |
|  | Full  | -                           | -          | 100 | -                              | -    | 200 | μA/Amp                         |
| Power Supply Rejection Ratio (Note 9)  | Full  | 77                          | 105        | -   | 77                             | 105  | -   | dB                             |

#### NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2.  $R_L = 50\text{k}\Omega$
3.  $C_L = 50\text{pF}$
4.  $V_O = 1.4$  to  $2.5\text{V}$  for  $V_{CC} = +5, 0\text{V}$ ;  $V_O = \pm 10\text{V}$  for  $V_{CC} = \pm 15\text{V}$ .
5. Settling Time is specified to 0.1% of final value for a 3V output step and  $A_V = -1$  for  $V_{CC} = +5\text{V}, 0\text{V}$ . Output step = 10V for  $V_{CC} = \pm 15\text{V}$ .
6. Maximum input slew rate =  $10\text{V}/\mu\text{s}$ .
7.  $V_{CM} = 0$  to  $3\text{V}$  for  $V_{CC} = +5, 0\text{V}$ ;  $V_{CM} = \pm 10\text{V}$  for  $V_{CC} = \pm 15\text{V}$ .
8. Full Power Bandwidth is guaranteed by equation:  

$$\text{Full Power Bandwidth} = \frac{\text{Slew Rate}}{2\text{nV Peak}}$$
9.  $\Delta V_S = +10\text{V}$  for  $V_{CC} = +5, 0\text{V}$ ;  $\Delta V_S = \pm 5\text{V}$  for  $V_{CC} = \pm 15\text{V}$ .
10. For  $V_{CC} = +5, 0\text{V}$  terminate  $R_L$  at  $+2.5\text{V}$ . Typical output current is  $\pm 3\text{mA}$ .
11.  $V_O = 1.4\text{V}$  for  $V_{CC} = +5\text{V}, 0\text{V}$ .

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OPERATIONAL  
AMPLIFIERS



## Specifications HA-5142/44

**Electrical Specifications**  $R_S = 100\Omega$ ,  $C_L \leq 10pF$  Unless Otherwise Specified.

| PARAMETER                              | TEMP  | -9<br>V+ = +5V, V- = 0V      |            |     | -9<br>V+ = +15V, V- = -15V |          |     | UNITS            |
|--|-------|------------------------------|------------|-----|----------------------------|----------|-----|------------------|
|  |       | MIN                          | TYP        | MAX | MIN                        | TYP      | MAX |                  |
|  |       | <b>INPUT CHARACTERISTICS</b> |            |     |                            |          |     |                  |
| Offset Voltage (Note 11)               | +25°C | -                            | 2          | 6   | -                          | 2        | 6   | mV               |
|  | Full  | -                            | -          | 8   | -                          | -        | 8   | mV               |
| Average Offset Voltage Drift           | Full  | -                            | 3          | -   | -                          | 3        | -   | $\mu V/^\circ C$ |
| Bias Current (Note 11)                 | +25°C | -                            | 45         | 100 | -                          | 45       | 100 | nA               |
|  | Full  | -                            | -          | 125 | -                          | -        | 125 | nA               |
| Offset Current (Note 11)               | +25°C | -                            | 0.3        | 10  | -                          | 0.3      | 10  | nA               |
|  | Full  | -                            | -          | 20  | -                          | -        | 20  | nA               |
| Common Mode Range                      | Full  | 0 to 3                       | -          | -   | $\pm 10$                   | -        | -   | V                |
| Differential Input Resistance          | +25°C | -                            | 0.6        | -   | -                          | 0.6      | -   | $M\Omega$        |
| Input Noise Voltage (f = 1kHz)         | +25°C | -                            | 20         | -   | -                          | 20       | -   | $nV/\sqrt{Hz}$   |
| Input Noise Current (f = 1kHz)         | +25°C | -                            | 0.25       | -   | -                          | 0.25     | -   | $pA/\sqrt{Hz}$   |
| <b>TRANSFER CHARACTERISTICS</b>        |       |                              |            |     |                            |          |     |                  |
| Large Signal Voltage Gain (Notes 2, 4) | +25°C | 20k                          | 100k       | -   | 20k                        | 100k     | -   | V/V              |
|  | Full  | 12k                          | -          | -   | 12k                        | -        | -   | V/V              |
| Common Mode Rejection Ratio (Note 7)   | Full  | 70                           | 105        | -   | 70                         | 105      | -   | dB               |
| Bandwidth (Notes 2, 3)                 | +25°C | -                            | 0.4        | -   | -                          | 0.4      | -   | MHz              |
| <b>OUTPUT CHARACTERISTICS</b>          |       |                              |            |     |                            |          |     |                  |
| Output Voltage Swing (Notes 2, 10)     | +25°C | 1.0 to 3.8                   | 0.7 to 4.2 | -   | $\pm 10$                   | $\pm 13$ | -   | V                |
|  | Full  | 1.2 to 3.5                   | 0.9 to 4.0 | -   | $\pm 10$                   | $\pm 13$ | -   | V                |
| Full Power Bandwidth (Notes 2, 4, 8)   | +25°C | -                            | 240        | -   | -                          | 24       | -   | kHz              |
| <b>TRANSIENT RESPONSE (Notes 2, 3)</b> |       |                              |            |     |                            |          |     |                  |
| Rise Time                              | +25°C | -                            | 600        | -   | -                          | 600      | -   | ns               |
| Slew Rate (Note 6)                     | +25°C | 0.8                          | 1.5        | -   | 0.8                        | 1.5      | -   | V/ $\mu s$       |
| Settling Time (Note 5)                 | +25°C | -                            | 10         | -   | -                          | 10       | -   | $\mu s$          |
| <b>POWER SUPPLY CHARACTERISTICS</b>    |       |                              |            |     |                            |          |     |                  |
| Supply Current                         | +25°C | -                            | 45         | 80  | -                          | 100      | 150 | $\mu A/Amp$      |
|  | Full  | -                            | -          | 100 | -                          | -        | 200 | $\mu A/Amp$      |
| Power Supply Rejection Ratio (Note 9)  | Full  | 70                           | 105        | -   | 70                         | 105      | -   | dB               |

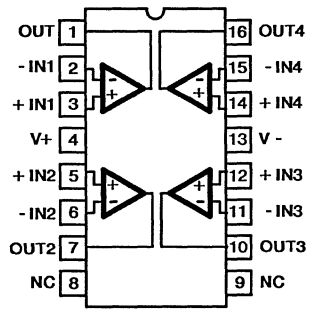
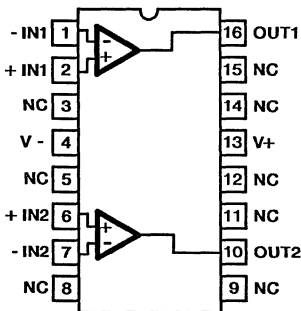
NOTE: The notes from the -2, -5 table apply to this -9 table. Absolute maximum ratings and the operating temperature ranges also apply.

### SOIC Pinouts

TOP VIEWS

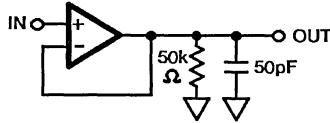
HA9P5142 (SOIC)

HA9P5144 (SOIC)



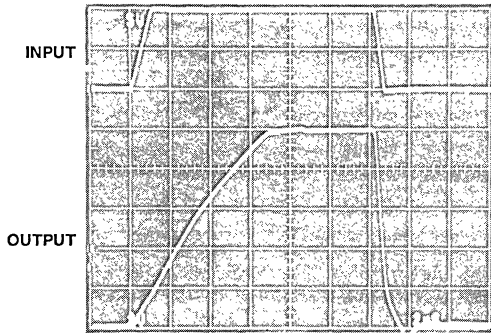
Test Circuits

SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



LARGE SIGNAL RESPONSE

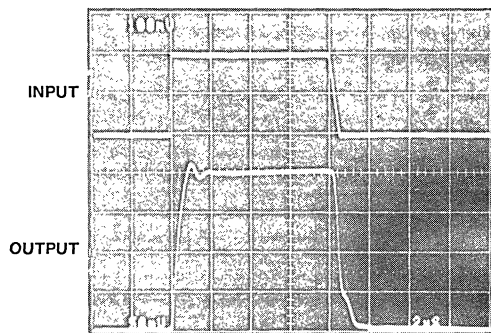
Vertical Scale: (Volts: Input = 5V/Div.; Output = 2V/Div.)  
Horizontal Scale: (Time: 2μs/Div.)



+VSUPPLY = +15V, -VSUPPLY = -15V

SMALL SIGNAL RESPONSE

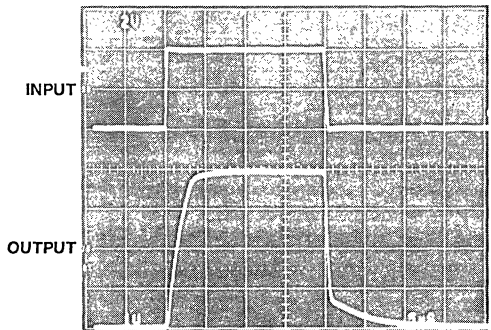
Vertical Scale: (Volts: Input = 100mV/Div.; Output = 50mV/Div.)  
Horizontal Scale: (Time: 2μs/Div.)



+VSUPPLY = +15V, -VSUPPLY = -15V

LARGE SIGNAL RESPONSE

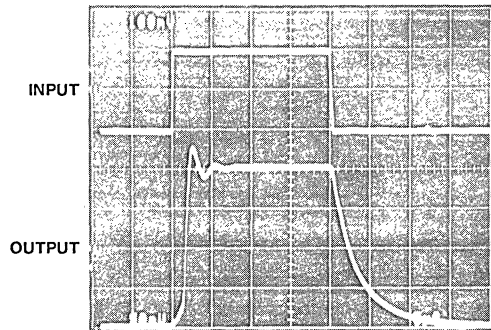
Vertical Scale: (Volts: Input = 2V/Div.; Output = 1V/Div.)  
Horizontal Scale: (Time: 5μs/Div.)



+VSUPPLY = +5V, -VSUPPLY = 0V

SMALL SIGNAL RESPONSE

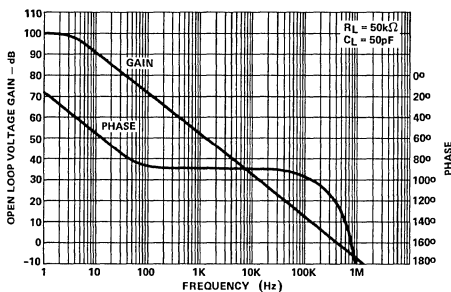
Vertical Scale: (Volts: Input = 100mV/Div.; Output = 50mV/Div.)  
Horizontal Scale: (Time: 5μs/Div.)



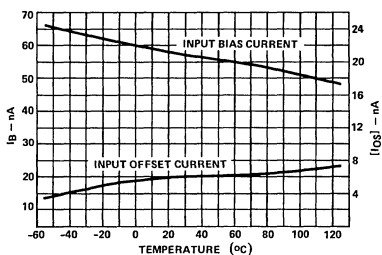
+VSUPPLY = +5V, -VSUPPLY = 0V

**Performance Curves**  $V_S = \pm 2.5V$ ,  $T_A = +25^\circ C$  Unless Otherwise Specified

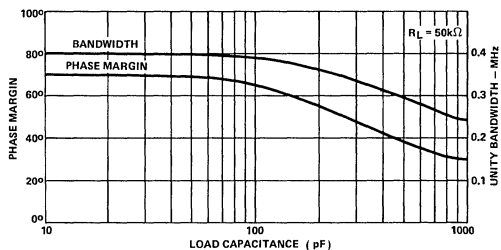
**OPEN LOOP FREQUENCY RESPONSE**



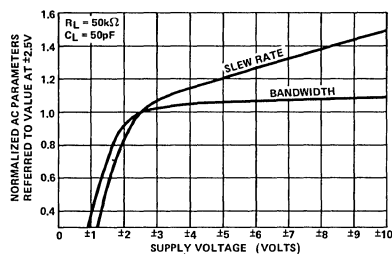
**INPUT OFFSET CURRENT AND BIAS CURRENT vs. TEMPERATURE**



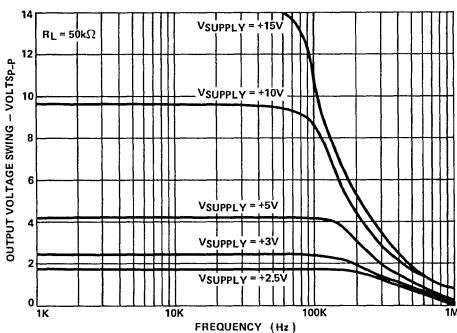
**BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE**



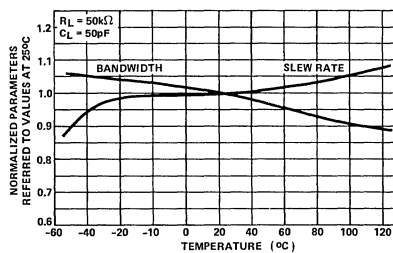
**NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE**



**OUTPUT VOLTAGE SWING vs. FREQUENCY AND SINGLE SUPPLY VOLTAGE**

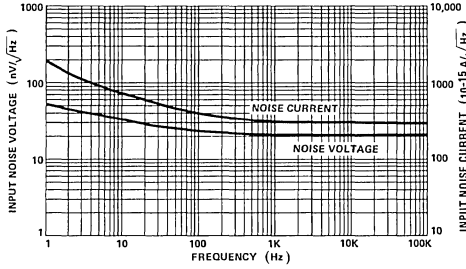


**NORMALIZED AC PARAMETERS vs. TEMPERATURE**

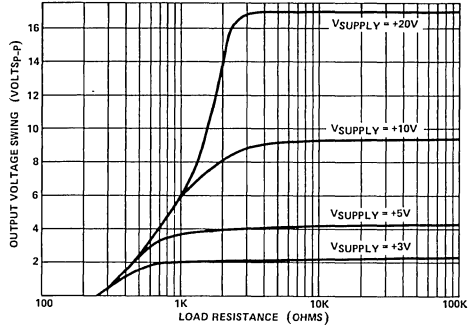


Performance Curves (Continued)  $V_S = \pm 2.5V$ ,  $T_A = +25^\circ C$  Unless Otherwise Specified

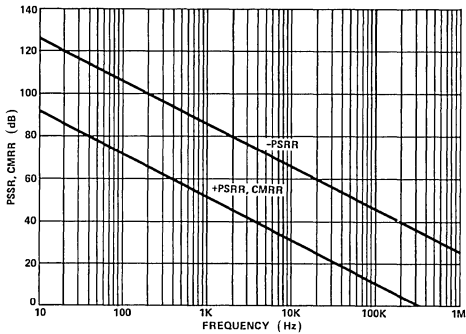
INPUT NOISE vs. FREQUENCY



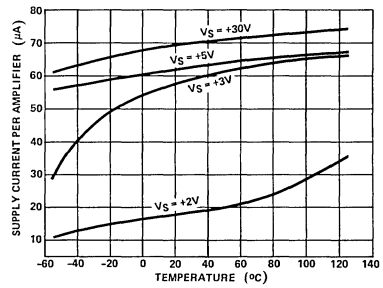
MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE AND SINGLE SUPPLY VOLTAGE



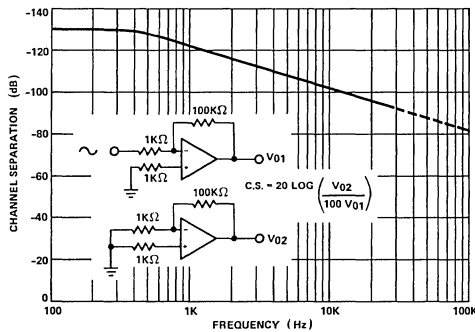
PSRR AND CMRR vs. FREQUENCY



POWER SUPPLY CURRENT vs. TEMPERATURE AND SINGLE SUPPLY VOLTAGE



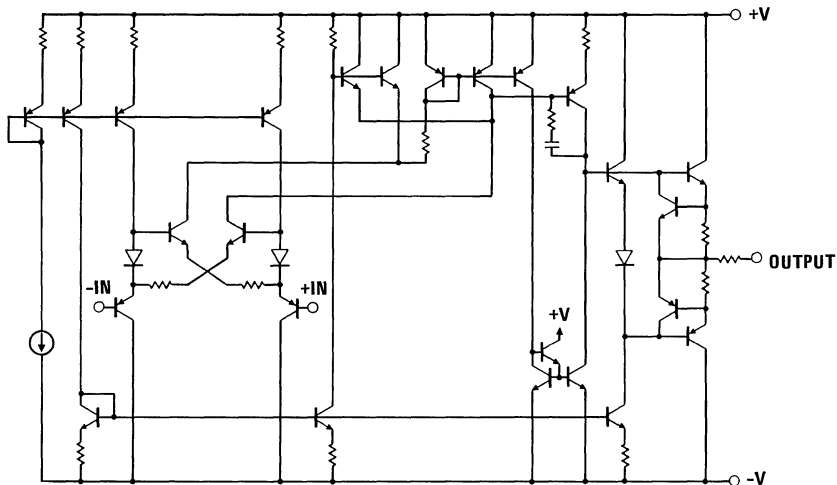
CHANNEL SEPARATION vs. FREQUENCY



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OPERATIONAL  
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# HA-5142/44

## Schematic



## Die Characteristics

### Transistor Count

|               |     |
|---------------|-----|
| HA-5142 ..... | 66  |
| HA-5144 ..... | 132 |

Substrate Potential\* ..... V-  
 Process ..... Bipolar-DI

### Thermal Constants (°C/W)

|                       | $\theta_{ja}$ | $\theta_{jc}$ |
|-----------------------|---------------|---------------|
| HA1-5144 (-2, -5, -7) | 101           | 33            |
| HA1-5144 (/883)       | 75            | 22            |
| HA2-5144 (-2, -5, -7) | 206           | 56            |
| HA2-5142 (-2, -5, -7) | 184           | 50            |
| HA2-5142 (/883)       | 143           | 43            |
| HA3-5142 (-5)         | 80            | 20            |
| HA3-5144 (-5)         | 75            | 20            |
| HA7-5142 (-2, -5, -7) | 177           | 92            |
| HA7-5142 (/883)       | 80            | 20            |
| HA9P5142 (-5, -9)     | 94            | 26            |
| HA9P5144 (-5, -9)     | 90            | 26            |

\*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

NOTE: Consult Harris for LCC/PLCC information.

## Ultra-Low Noise Precision High Slew Rate Wideband Operational Amplifier

August 1991

### Features

- High Speed ..... 35V/ $\mu$ s
- Wide Gain Bandwidth ( $A_V \geq 10$ ) ..... 120MHz
- Low Noise ..... 3nV/ $\sqrt{\text{Hz}}$  at 1 KHz
- Low VOS ..... 10 $\mu$ V
- High CMRR ..... 126dB
- High Gain ..... 1800V/mV

### Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers

### Description

The HA-5147 monolithic operational amplifier features an unparallelled combination of precision DC and wideband high speed characteristics. Utilizing the Harris D. I. technology and advanced processing techniques, this unique design unites low noise (3nV/ $\sqrt{\text{Hz}}$ ) precision instrumentation performance with high speed (35V/ $\mu$ s) wideband capability.

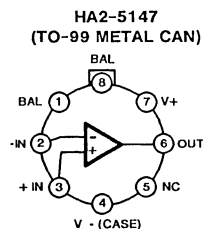
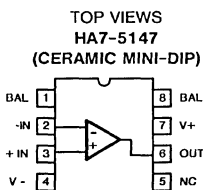
This amplifier's impressive list of features include low  $V_{OS}$  (10 $\mu$ V), wide gain-bandwidth (120MHz), high open loop gain (1800V/mV), and high CMRR (126dB). Additionally, this flexible device operates over a wide supply range ( $\pm 5V$  to  $\pm 20V$ ) while consuming only 140mW of power.

Using the HA-5147 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than ten.

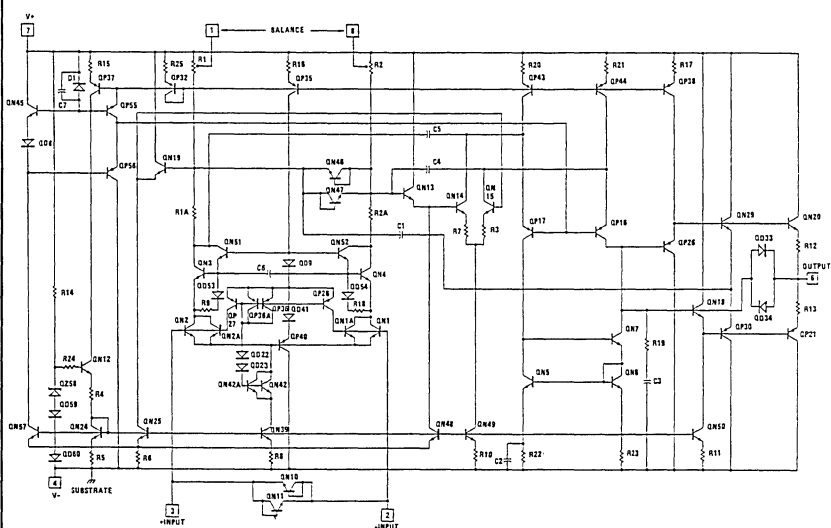
This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5147's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits. Further application ideas are given in Application Note 553.

This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37 where gains are greater than ten. The HA-5147 is available in TO-99 Metal Can and Ceramic 8 pin Mini-DIPs. For military grade product, refer to the HA-5147/883 data sheet.

### Pinouts



### Schematic



## Specifications HA-5147

### Absolute Maximum Ratings (Note 1)

|   |                               |
|---|-------------------------------|
| $T_A = +25^\circ\text{C}$ Unless Otherwise Stated |                               |
| Voltage Between V+ and V- Terminals               | $\pm 22\text{V}$              |
| Differential Input Voltage (Note 2)               | $\pm 0.7\text{V}$             |
| Internal Power Dissipation                        | 500mW                         |
| Output Current                                    | Full Short Circuit Protection |

### Operating Temperature Ranges

|                              |  |
|------------------------------|--|
| HA-5147/47A-2                | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ |
| HA-5147/47A-5                | $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$    |
| Storage Temperature Range    | $-65^\circ\text{C} \leq T_A \leq +150^\circ\text{C}$ |
| Maximum Junction Temperature | $+175^\circ\text{C}$                                 |

### Electrical Specifications $V_+ = 15\text{V}$ , $V_- = -15\text{V}$ , $C_L \leq 50\text{pF}$ , $R_S \leq 100\Omega$

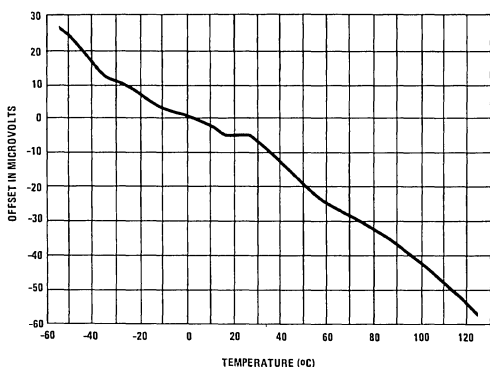
| PARAMETER                                  | TEMP                    | HA-5147A            |            |            | HA-5147    |            |            | UNITS                        |
|--|-------------------------|---------------------|------------|------------|------------|------------|------------|------------------------------|
|  |                         | MIN                 | TYP        | MAX        | MIN        | TYP        | MAX        |                              |
| <b>INPUT CHARACTERISTICS</b>               |                         |                     |            |            |            |            |            |                              |
| Offset Voltage                             | $+25^\circ\text{C}$     | -                   | 10         | 25         | -          | 30         | 100        | $\mu\text{V}$                |
|  | Full                    | -                   | 30         | 60         | -          | 70         | 300        | $\mu\text{V}$                |
| Average Offset Voltage Drift               | Full                    | -                   | 0.2        | 0.6        | -          | 0.4        | 1.8        | $\mu\text{V}/^\circ\text{C}$ |
| Bias Current                               | $+25^\circ\text{C}$     | -                   | $\pm 10$   | $\pm 40$   | -          | $\pm 15$   | $\pm 80$   | nA                           |
|  | Full                    | -                   | $\pm 20$   | $\pm 60$   | -          | $\pm 35$   | $\pm 150$  | nA                           |
| Offset Current                             | $+25^\circ\text{C}$     | -                   | 7          | 35         | -          | 12         | 75         | nA                           |
|  | Full                    | -                   | 15         | 50         | -          | 30         | 135        | nA                           |
| Common Mode Range                          |                         | $\pm 10.3$          | $\pm 11.5$ | -          | $\pm 10.3$ | $\pm 11.5$ | -          | V                            |
| Differential Input Resistance (Note 3)     | $+25^\circ\text{C}$     | 1.5                 | 6          | -          | 0.8        | 4          | -          | M $\Omega$                   |
| Input Noise Voltage 0.1Hz to 10Hz (Note 4) | $+25^\circ\text{C}$     | -                   | 0.08       | 0.18       | -          | 0.09       | 0.25       | $\mu\text{Vp-p}$             |
| Input Noise Voltage Density (Note 5)       | $+25^\circ\text{C}$     | -                   | 3.5        | 5.5        | -          | 3.8        | 8.0        | $\text{nV}/\sqrt{\text{Hz}}$ |
|  | $f_0 = 10\text{Hz}$     | -                   | -          | -          | -          | -          | -          | -                            |
|  | $f_0 = 30\text{Hz}$     | -                   | 3.1        | 4.5        | -          | 3.3        | 5.6        | $\text{nV}/\sqrt{\text{Hz}}$ |
|  | $f_0 = 1000\text{Hz}$   | -                   | 3.0        | 3.8        | -          | 3.2        | 4.5        | $\text{nV}/\sqrt{\text{Hz}}$ |
| Input Noise Current Density (Note 5)       | $+25^\circ\text{C}$     | -                   | 1.7        | 4.0        | -          | 1.7        | -          | $\text{pA}/\sqrt{\text{Hz}}$ |
|  | $f_0 = 10\text{Hz}$     | -                   | -          | -          | -          | -          | -          | -                            |
|  | $f_0 = 30\text{Hz}$     | -                   | 1.0        | 2.3        | -          | 1.0        | -          | $\text{pA}/\sqrt{\text{Hz}}$ |
|  | $f_0 = 1000\text{Hz}$   | -                   | 0.4        | 0.6        | -          | 0.4        | 0.6        | $\text{pA}/\sqrt{\text{Hz}}$ |
| <b>TRANSFER CHARACTERISTICS</b>            |                         |                     |            |            |            |            |            |                              |
| Minimum Stable Gain                        | $+25^\circ\text{C}$     | 10                  | -          | -          | 10         | -          | -          | V/V                          |
| Large Signal Voltage Gain (Note 6)         | $+25^\circ\text{C}$     | 1000                | 1800       | -          | 700        | 1500       | -          | V/mV                         |
|  | Full                    | 600                 | 1200       | -          | 300        | 800        | -          | V/mV                         |
| Common Mode Rejection Ratio (Note 7)       | Full                    | 114                 | 126        | -          | 100        | 120        | -          | dB                           |
| Gain-Bandwidth-Product                     | $f_0 = 10\text{kHz}$    | $+25^\circ\text{C}$ | 120        | 140        | -          | 120        | 140        | MHz                          |
|  | $f_0 = 1\text{MHz}$     | $+25^\circ\text{C}$ | -          | 120        | -          | -          | 120        | MHz                          |
| <b>OUTPUT CHARACTERISTICS</b>              |                         |                     |            |            |            |            |            |                              |
| Output Voltage Swing                       | $R_L = 600\Omega$       | $+25^\circ\text{C}$ | $\pm 10.0$ | $\pm 11.5$ | -          | $\pm 10.0$ | $\pm 11.5$ | V                            |
|  | $R_L = 2\text{K}\Omega$ | Full                | $\pm 11.7$ | $\pm 13.8$ | -          | $\pm 11.4$ | $\pm 13.5$ | V                            |
| Full Power Bandwidth (Note 8)              |                         | $+25^\circ\text{C}$ | 445        | 500        | -          | 445        | 500        | KHz                          |
| Output Resistance, Open Loop               |                         | $+25^\circ\text{C}$ | -          | 70         | -          | -          | 70         | $\Omega$                     |
| Output Current                             |                         | $+25^\circ\text{C}$ | 16.5       | 25         | -          | 16.5       | 25         | mA                           |
| <b>TRANSIENT RESPONSE (Note 9)</b>         |                         |                     |            |            |            |            |            |                              |
| Rise Time                                  | $+25^\circ\text{C}$     | -                   | 22         | 50         | -          | 22         | 50         | ns                           |
| Slew Rate (Note 11)                        | $+25^\circ\text{C}$     | 28                  | 35         | -          | 28         | 35         | -          | V/ $\mu\text{s}$             |
| Settling Time (Note 10)                    | $+25^\circ\text{C}$     | -                   | 400        | -          | -          | 400        | -          | ns                           |
| Overshoot                                  | $+25^\circ\text{C}$     | -                   | 20         | 40         | -          | 20         | 40         | %                            |
| <b>POWER SUPPLY CHARACTERISTICS</b>        |                         |                     |            |            |            |            |            |                              |
| Supply Current                             | $+25^\circ\text{C}$     | -                   | 3.5        | -          | -          | 3.5        | -          | mA                           |
|  | Full                    | -                   | -          | 4.0        | -          | -          | 4.0        | mA                           |
| Power Supply Rejection Ratio (Note 12)     | Full                    | -                   | 2          | 4          | -          | 16         | 51         | $\mu\text{V}/\text{V}$       |

NOTES:

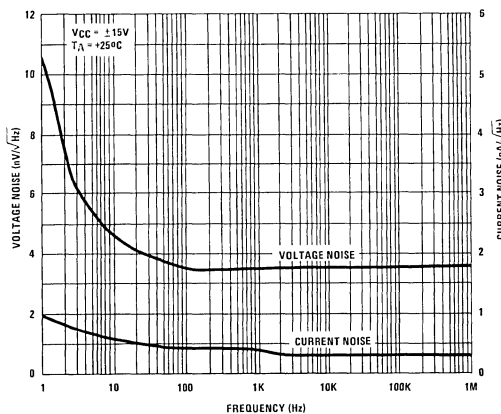
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.
3. This parameter value is based upon design calculations.
4. Refer to Typical Performance section of the data sheet.
5. Sample tested.
6.  $V_{OUT} = \pm 10V, R_L = 2K\Omega$
7.  $V_{CM} = \pm 10V$
8. Full power bandwidth guaranteed based on slew rate measurement using:  $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
9. Refer to Test Circuits section of the data sheet.
10. Settling time is specified to 0.1% of final value for a 10V output step and  $A_V = -10$ .
11.  $V_{OUT} = 10V$  Step
12.  $V_S = \pm 4V$  to  $\pm 16V$

**Typical Performance Curves** Unless Otherwise Specified:  $T_A = +25^\circ C, V_{SUPPLY} = \pm 15V$

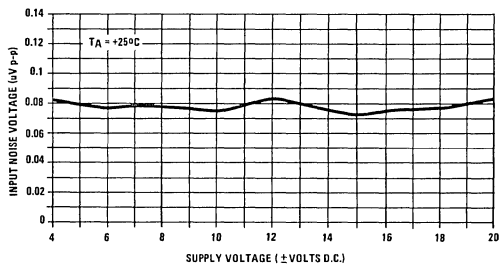
OFFSET VOLTAGE TYPICAL DRIFT vs. TEMPERATURE



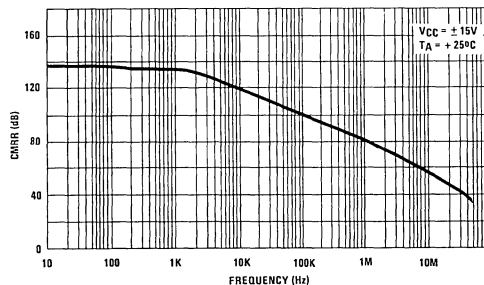
NOISE CHARACTERISTICS



NOISE vs. SUPPLY VOLTAGE



CMRR vs. FREQUENCY

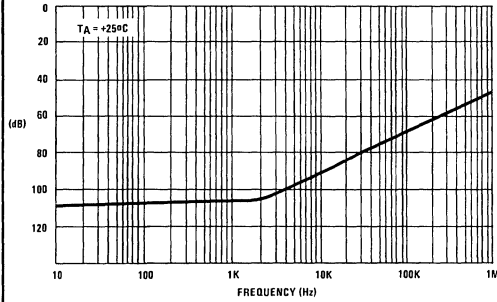


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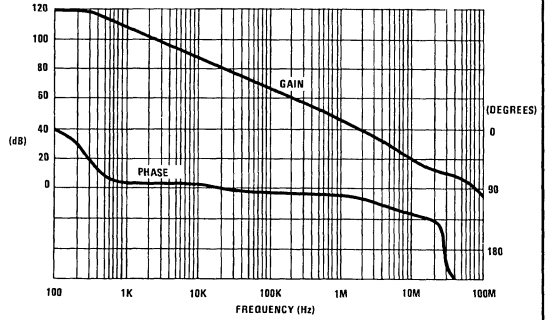


**Typical Performance Curves (Continued)** Unless Otherwise Specified:  $T_A = +25^\circ\text{C}$ ,  $V_{\text{SUPPLY}} = \pm 15\text{V}$

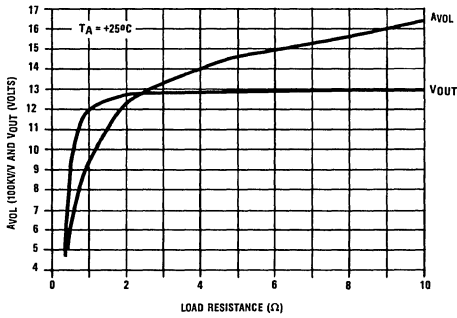
**PSRR vs. FREQUENCY**



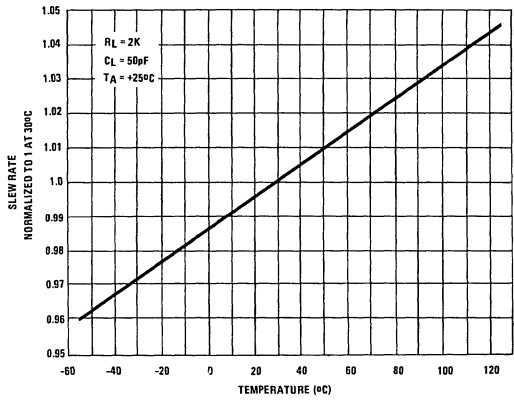
**OPEN LOOP GAIN AND PHASE vs. FREQUENCY**



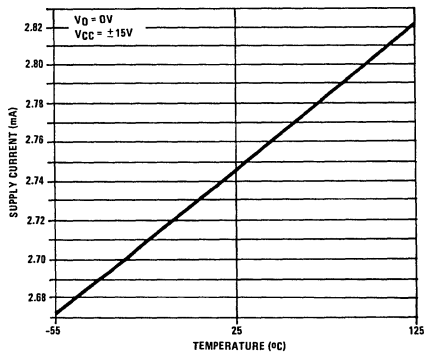
**$A_{\text{VOL}}$  AND  $V_{\text{OUT}}$  vs. LOAD RESISTANCE**



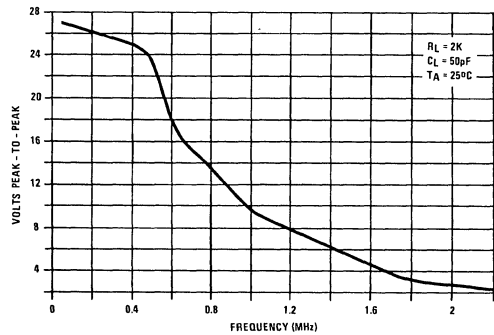
**NORMALIZED SLEW RATE vs. TEMPERATURE**



**SUPPLY CURRENT vs. TEMPERATURE**

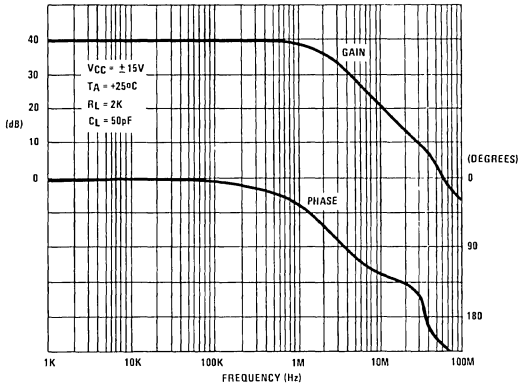


**$V_{\text{OUT MAX}}$  vs. FREQUENCY  
UNDISTORTED SINEWAVE OUTPUT**

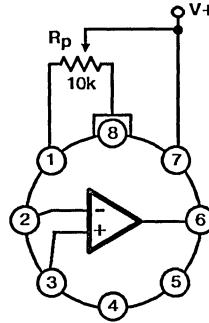


**Typical Performance Curves (Continued)** Unless Otherwise Specified:  $T_A = +25^\circ\text{C}$ ,  $V_{\text{SUPPLY}} = \pm 15\text{V}$

**CLOSED LOOP GAIN AND PHASE vs. FREQUENCY**

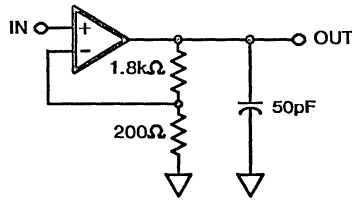


**SUGGESTED OFFSET VOLTAGE ADJUSTMENT**

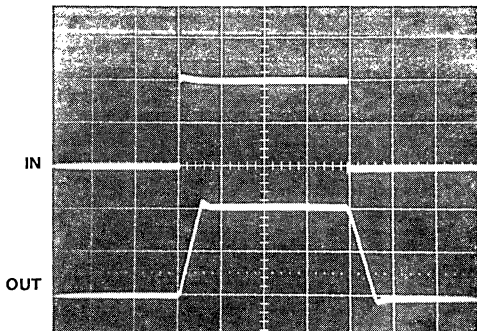


Tested Offset Adjustment Range is  $|V_{OS} + 1\text{mV}|$  minimum referred to output.  
 Typical range is  $\pm 4\text{mV}$  with  $R_T = 10\text{k}\Omega$ .

**LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT**

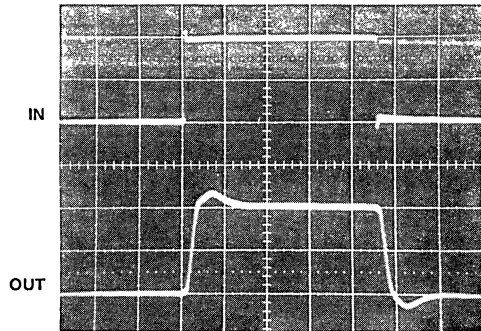


**LARGE SIGNAL RESPONSE**



Vertical Scale: (Volts: Input = 0.5V/Div.)  
 (Volts: Output = 5V/Div.)  
 Horizontal Scale: (Time: 500ns/Div)

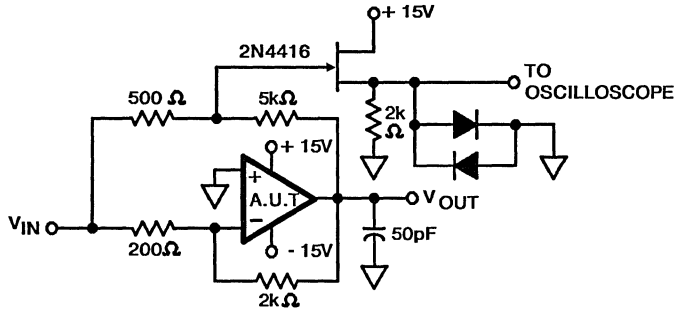
**SMALL SIGNAL RESPONSE**



Vertical Scale: (Volts: Input = 10mV/Div)  
 (Volts: Output = 100mV/Div)  
 Horizontal Scale: (Time: 100ns/Div)

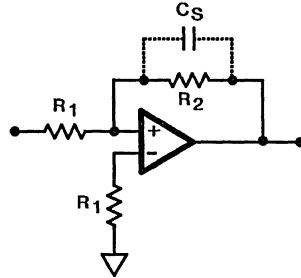
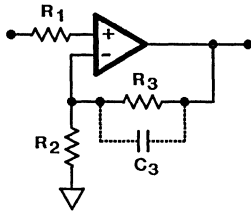
**Typical Performance Curves (Continued)** Unless Otherwise Specified:  $T_A = +25^\circ\text{C}$ ,  $V_{\text{SUPPLY}} = \pm 15\text{V}$

**SETTLING TIME TEST CIRCUIT**



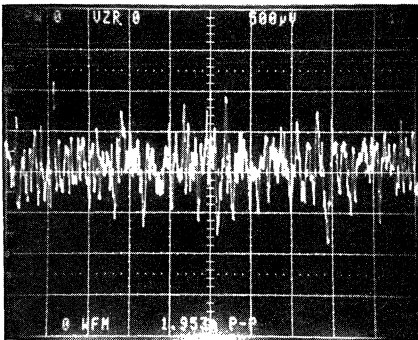
- $A_V = -10$
- Feedback and summing resistors should be 0.1%
- Clipping diodes are optional. HP5082-2810 recommended

**SUGGESTED STABILITY CIRCUITS**



Low resistances are preferred for low noise applications as a  $1\text{k}\Omega$  resistor has  $4\text{nV}/\sqrt{\text{Hz}}$  of thermal noise. Total resistances of greater than  $10\text{k}\Omega$  on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

**0.1Hz TO 10Hz NOISE WITH  $A_{\text{CL}} = 25,000\text{V/V}$**



Horizontal Scale = 1sec/Div.  
Vertical Scale = 0.002μV/Div.  
0.08μVp-p

**Die Characteristics**

|  |                      |               |
|--|----------------------|---------------|
| Transistor Count .....                   | 63                   |               |
| Die Dimensions .....                     | 65 x 104.3 x 19 mils |               |
| Substrate Potential* .....               | V-                   |               |
| V-Process .....                          | Bipolar-DI           |               |
| Thermal Constants ( $^\circ\text{C/W}$ ) | $\theta_{ja}$        | $\theta_{jc}$ |
| HA7-5147 Ceramic Mini-DIP                | 160                  | 79            |
| HA2-5147 TO-99 Metal Can                 | 172                  | 48            |

\*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

# HA-5160/62

Wideband, JFET Input High Slew Rate, Uncompensated, Operational Amplifier

August 1991

### Features

- Wide Gain Bandwidth ( $A_V \geq 10$ ) ..... 100MHz
- High Slew Rate ..... 120V/ $\mu$ s
- Settling Time ..... 280ns
- Power Bandwidth ..... 1.9MHz
- Offset Voltage ..... 1.0mV
- Bias Current ..... 20pA

### Description

The HA-5160 is a wideband, uncompensated, operational amplifier with FET/Bipolar technologies and Dielectric Isolation. This monolithic amplifier features superior high frequency capabilities further enhanced by precision laser trimming of the input stage to provide excellent input characteristics. This device has excellent phase margin at a closed loop gain of 10 without external compensation.

The HA-5160/5162 offers a number of important advantages over similar FET input op amps from other manufacturers. In addition to superior bandwidth and settling characteristics, the Harris devices have nearly constant slew rate, bandwidth, and settling characteristics over the operating temperature range. This provides the user predictable performance in applications where settling time, full power bandwidth, closed loop bandwidth, or phase shift is critical. Note also that Harris specifies all parameters at ambient (rather than junction) temperature to

### Applications

- Video and RF Amplifiers
- Data Acquisition
- Pulse Amplifiers
- Precision Signal Generation

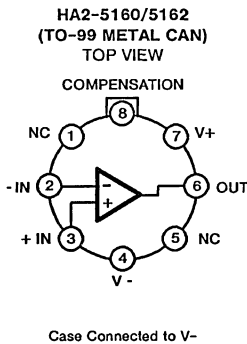
provide the designer meaningful data to predict actual operating performance.

Complementing the HA-5160/5162's predictable and excellent dynamic characteristics are very low input offset voltage, very low input bias current, and a very high input impedance. This ideal combination of features make these amplifiers most suitable for precision, high speed, data acquisition system designs and for a wide variety of signal conditioning applications. The HA-5160 provides excellent performance for applications which require both precision and high speed performance. The HA-5162 meets or exceeds the performance specifications of National's hybrid op amp, the LH0062.

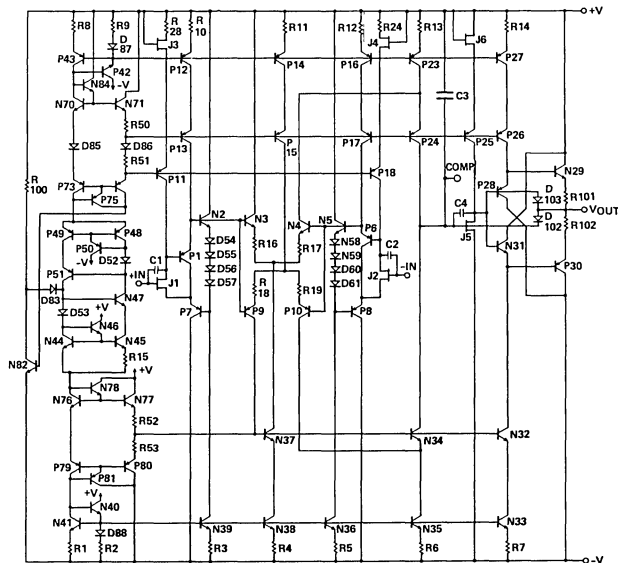
The HA2-5160-2 denotes a temperature range of -55°C to +125°C and the HA2-5160/62-5 denotes a 0°C to +75°C range. Military version (/883) data sheets are available upon request.

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OPERATIONAL AMPLIFIERS

### Pinout



### Schematic



## Specifications HA-5160/5162

### Absolute Maximum Ratings

|   |                               |
|---|-------------------------------|
| Voltage Between V+ and V- .....           | 40V                           |
| Differential Input Voltage .....          | ±40V                          |
| Peak Output Current .....                 | Full Short Circuit Protection |
| Internal Power Dissipation (Note 2) ..... | 675mW                         |

### Operating Temperature Ranges:

|   |                                 |
|---|---------------------------------|
| HA-5160-2 .....                             | -55°C ≤ T <sub>A</sub> ≤ +125°C |
| HA-5160-5 .....                             | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| HA-5162-5 .....                             | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| Storage Temperature Range .....             | -65°C ≤ T <sub>A</sub> ≤ +150°C |
| Maximum Junction Temperature (Note 2) ..... | +175°C                          |

### Electrical Specifications V+ = +15V, V- = -15V, Unless Otherwise Specified.

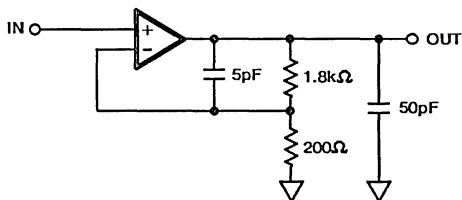
| PARAMETER                                    | TEMP  | HA-5160-2<br>-55°C to 125°C |                  |     | HA-5160-5<br>0°C to +75°C |                  |     | HA-5162-5<br>0°C to +75°C |                  |     | UNITS |
|--|-------|-----------------------------|------------------|-----|---------------------------|------------------|-----|---------------------------|------------------|-----|-------|
|  |       | MIN                         | TYP              | MAX | MIN                       | TYP              | MAX | MIN                       | TYP              | MAX |       |
| <b>INPUT CHARACTERISTICS</b>                 |       |                             |                  |     |                           |                  |     |                           |                  |     |       |
| Offset Voltage                               | +25°C | -                           | 1                | 3   | -                         | 1                | 3   | -                         | 3                | 15  | mV    |
|  | Full  | -                           | 3                | 5   | -                         | 3                | 5   | -                         | 5                | 20  | mV    |
| Offset Voltage Average Drift                 | Full  | -                           | 10               | -   | -                         | 20               | -   | -                         | 20               | 35  | μV/°C |
| Bias Current                                 | +25°C | -                           | 20               | 50  | -                         | 20               | 50  | -                         | 20               | 65  | pA    |
|  | Full  | -                           | 5                | 10  | -                         | 5                | 10  | -                         | 5                | 10  | nA    |
| Offset Current                               | +25°C | -                           | 2                | 10  | -                         | 2                | 10  | -                         | 2                | 10  | pA    |
|  | Full  | -                           | 2                | 5   | -                         | 2                | 5   | -                         | 2                | 5   | nA    |
| Input Capacitance                            | +25°C | -                           | 5                | -   | -                         | 5                | -   | -                         | 5                | -   | pF    |
| Input Resistance                             | +25°C | -                           | 10 <sup>12</sup> | -   | -                         | 10 <sup>12</sup> | -   | -                         | 10 <sup>12</sup> | -   | Ω     |
| Common Mode Range                            | Full  | ±10                         | ±11              | -   | ±10                       | ±11              | -   | ±10                       | ±11              | -   | V     |
| <b>TRANSFER CHARACTERISTICS</b>              |       |                             |                  |     |                           |                  |     |                           |                  |     |       |
| Large Signal Voltage Gain (Note 3)           | +25°C | 75K                         | 150K             | -   | 75K                       | 150K             | -   | 25K                       | 100K             | -   | V/V   |
|  | Full  | 60K                         | 100K             | -   | 60K                       | 100K             | -   | 25K                       | 75K              | -   | V/V   |
| Common Mode Rejection Ratio (Note 4)         | Full  | 74                          | 80               | -   | 74                        | 80               | -   | 70                        | 80               | -   | dB    |
| Minimum Stable Gain                          | +25°C | 10                          | -                | -   | 10                        | -                | -   | 10                        | -                | -   | V/V   |
| Gain Bandwidth Product (A <sub>v</sub> ≥ 10) | Full  | -                           | 100              | -   | -                         | 100              | -   | -                         | 100              | -   | MHz   |
| <b>OUTPUT CHARACTERISTICS</b>                |       |                             |                  |     |                           |                  |     |                           |                  |     |       |
| Output Voltage Swing (Note 5)                | +25°C | ±10                         | ±11              | -   | ±10                       | ±11              | -   | ±10                       | ±11              | -   | V     |
|  | Full  | ±10                         | ±11              | -   | ±10                       | ±11              | -   | ±10                       | ±11              | -   | V     |
| Output Current (Note 6)                      | +25°C | ±10                         | ±20              | -   | ±10                       | ±20              | -   | ±10                       | ±20              | -   | mA    |
| Output Short Circuit Current                 | +25°C | -                           | ±35              | -   | -                         | ±35              | -   | -                         | ±35              | -   | mA    |
| Full Power Bandwidth (Note 3, 7)             | +25°C | 1.6                         | 1.9              | -   | 1.6                       | 1.9              | -   | 0.8                       | 1.1              | -   | MHz   |
| Output Resistance (Note 8)                   | +25°C | -                           | 50               | -   | -                         | 50               | -   | -                         | 50               | -   | Ω     |
| <b>TRANSIENT RESPONSE (Note 9)</b>           |       |                             |                  |     |                           |                  |     |                           |                  |     |       |
| Rise Time                                    | +25°C | -                           | 20               | -   | -                         | 20               | -   | -                         | 20               | -   | ns    |
| Slew Rate                                    | +25°C | 100                         | 120              | -   | 100                       | 120              | -   | 50                        | 70               | -   | V/μs  |
| Settling Time (Note 10)                      | +25°C | -                           | 280              | -   | -                         | 280              | -   | -                         | 400              | -   | ns    |
| <b>POWER SUPPLY CHARACTERISTICS</b>          |       |                             |                  |     |                           |                  |     |                           |                  |     |       |
| Supply Current                               | Full  | -                           | 8                | 10  | -                         | 8                | 10  | -                         | 8                | 12  | mA    |
| Power Supply Rejection Ratio (Note 11)       | +25°C | 74                          | 86               | -   | 74                        | 86               | -   | 70                        | 86               | -   | dB    |

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at  $6.8\text{mW}/^\circ\text{C}$  for operation at ambient temperatures above  $+75^\circ\text{C}$ .
3.  $V_{\text{OUT}} = \pm 10\text{V}$ ,  $R_L = 2\text{K}$
4.  $V_{\text{CM}} = \pm 10\text{V DC}$
5.  $R_L = 2\text{K}$
6.  $V_{\text{OUT}} = \pm 10\text{V}$
7. Full Power Bandwidth guaranteed, based on slew rate measurement using  $\text{FPWB} = \frac{\text{Slew Rate}}{2\pi V_{\text{peak}}}$
8. Output resistance measured under open loop conditions.
9. Refer to Test circuits section of the data sheet, where  $A_V = +10$ .
10. Settling Time is measured to 0.2% of final value for a 10 volt output step and  $A_V = 10$ .
11.  $V_{\text{SUPPLY}} = \pm 10\text{V DC}$  to  $\pm 20\text{V DC}$

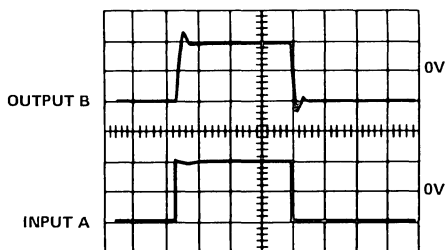
Test Circuits

LARGE AND SMALL SIGNAL RESPONSE CIRCUIT



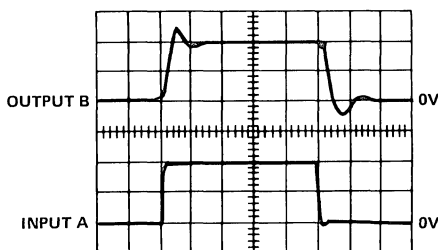
LARGE SIGNAL RESPONSE

Vertical Scale: A = 0.5V/Div., B = 5V/Div.  
Horizontal Scale: Time = 500ns/Div.

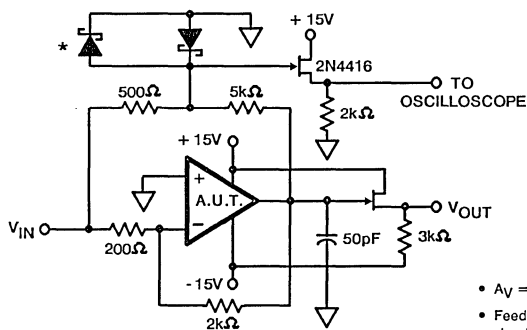


SMALL SIGNAL RESPONSE

Vertical Scale: A = 10mV/Div., B = 100mV/Div.  
Horizontal Scale: Time = 100ns/Div.



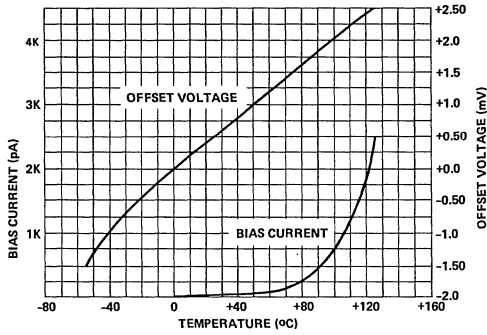
SETTLING TIME CIRCUIT



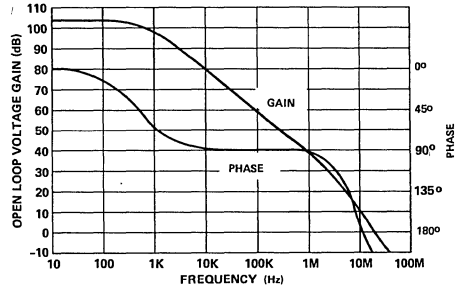
- $A_V = -10$
- Feedback and summing resistors should be 0.1% matched.
- \* Clipping Diodes are optional.  
HP5082-2810 recommended.

**Typical Performance Curves**

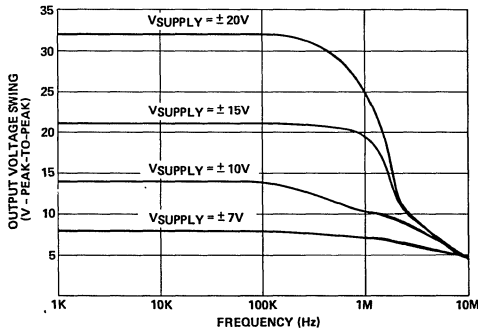
**INPUT OFFSET VOLTAGE AND BIAS CURRENT vs. TEMPERATURE**



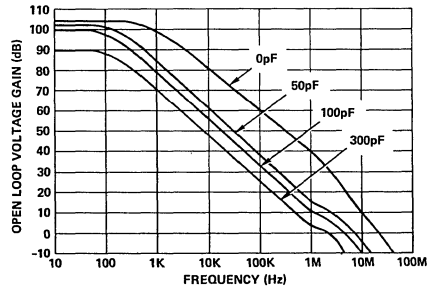
**OPEN LOOP FREQUENCY RESPONSE**



**OUTPUT VOLTAGE SWING vs. FREQUENCY**

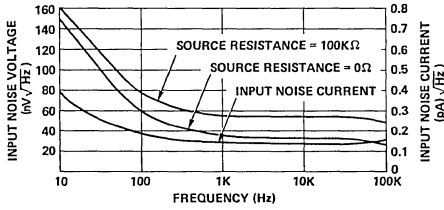


**OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS BANDWIDTH CONTROL CAPACITANCES**

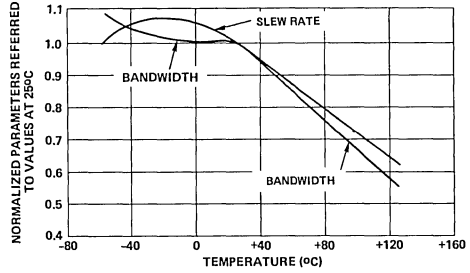


Typical Performance Curves (Continued)

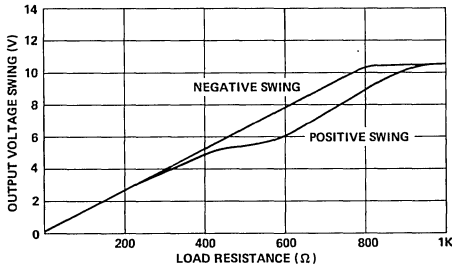
INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY



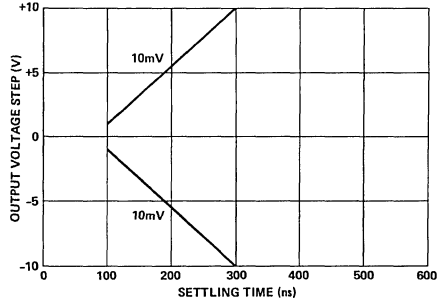
NORMALIZED AC PARAMETERS vs. TEMPERATURE



OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

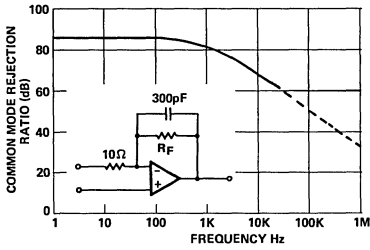




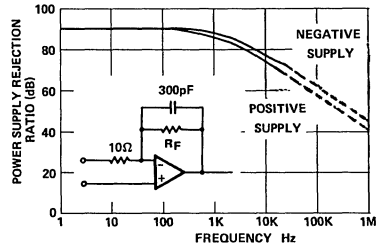
# HA-5160/5162

## Typical Performance Curves (Continued)

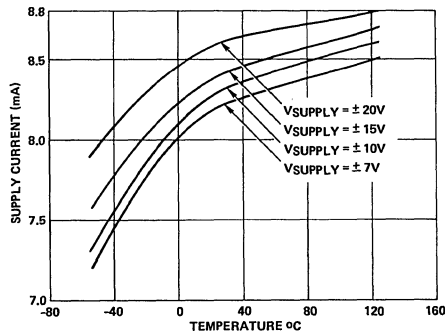
**COMMON MODE REJECTION RATIO vs. FREQUENCY**



**POWER SUPPLY REJECTION RATIO vs. FREQUENCY**



**POWER SUPPLY CURRENT vs. TEMPERATURE**



### Die Characteristics

|   |   |
|---|---|
| Transistor Count .....                            | 82  |
| Die Dimensions .....                              | 131 x 72 x 19 mils<br>(3330 x 1830 x 483μm) |
| Substrate Potential (Powered Up) .....            | None  |
| Process .....                                     | Bipolar/JFET DI                             |
| Thermal Constants (°C/W)                          | $\theta_{ja}$ $\theta_{jc}$                 |
| HA2-5160 (-8, /883)<br>(Gold Eutectic Die Attach) | 103      31                                 |
| HA2-5160/5162 (-2, -5, -7)<br>(Glass Die Attach)  | 146      38                                 |

**Applying the HA-5160/5162**

1. **POWER SUPPLY DECOUPLING:** Although not absolutely necessary, it is recommended that all power supply lines be decoupled with  $0.01\mu\text{F}$  ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
2. **STABILITY:** The phase margin of the HA-5160/5162 will be improved by connecting a small capacitor ( $>10\text{pF}$ ) between the output and the inverting input of

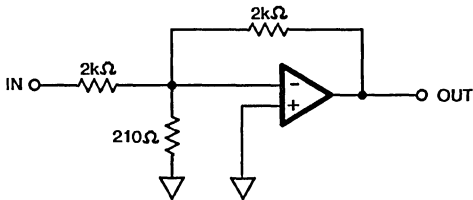
the device. This small capacitor compensated for the input capacitance of the FET.

3. **CAPACITIVE LOADS:** When driving large capacitive loads ( $>100\text{pF}$ ), it is suggested that a small resistor ( $\approx 100\Omega$ ) be connected in series with the output of the device and inside the feedback loop.
4. **POWER SUPPLY MINIMUM:** The absolute supply minimum is  $\pm 6\text{V}$  and the safe level is  $\pm 7\text{V}$ .

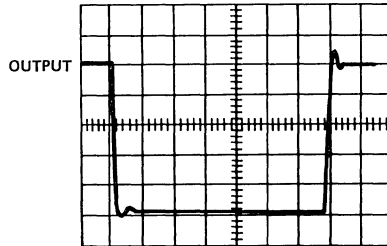
**Applications**

**Suggested Compensation For Unity Gain Stability\***

**INVERTING UNITY GAIN CIRCUIT**

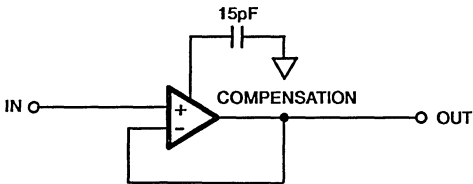


**INVERTING UNITY GAIN PULSE RESPONSE**

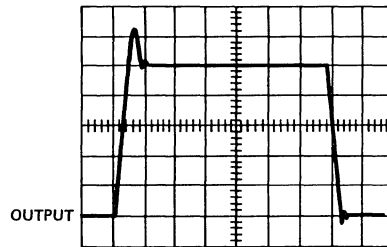


Vertical Scale: (Volts: 2V/Div.)  
Horizontal Scale: (Time: 500ns/Div.)

**NONINVERTING UNITY GAIN CIRCUIT**



**NONINVERTING UNITY GAIN PULSE RESPONSE**



Vertical Scale: (Volts: 2V/Div.)  
Horizontal Scale: (Time: 500ns/Div.)

\* Values Were Determined Experimentally  
For Optimum Speed and Settling Time.

## Precision JFET Input Operational Amplifier

August 1991

### Features

- Low Offset Voltage ..... 100 $\mu$ V
- Low Offset Voltage Drift ..... 2 $\mu$ V/ $^{\circ}$ C
- Low Noise ..... 10nV/ $\sqrt{\text{Hz}}$
- High Open Loop Gain ..... 600K V/V
- Wide Bandwidth ..... 8MHz
- Unity Gain Stable

### Description

The Harris HA-5170 is a precision, JFET input, operational amplifier which features low noise, low offset voltage and low offset voltage drift. Constructed using FET/Bipolar technology, the Harris Dielectric Isolation (DI) process, and laser trimming this amplifier offers low input bias and offset currents. This operational amplifier design also completely eliminates the troublesome errors due to warm-up drift.

Complementing these excellent input characteristics are dynamic performance characteristics never before available from precision operational amplifiers. An 8V/ $\mu$ s slew rate and 8MHz bandwidth allow the designer to extend precision instrumentation applications in both speed and

### Applications

- High Gain Instrumentation Amplifiers
- Precision Data Acquisition
- Precision Integrators
- Precision Threshold Detectors
- For Further Design Ideas, Refer to App. Note 540.

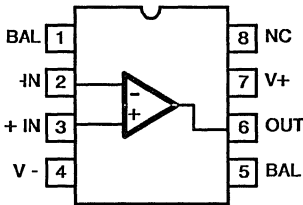
bandwidth. These characteristics make the HA-5170 well suited for precision integrator amplifier designs.

The superior input characteristics also make the HA-5170 ideally suited for transducer signal amplifiers, precision voltage followers and precision data acquisition systems. For application assistance, please refer to Application Note 540 addressing specifically this device.

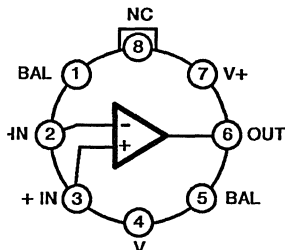
The HA-5170 is available in Metal Can (TO-99) and Ceramic Mini-DIP packages. HA-5170-2 denotes a  $-55^{\circ}$ C to  $+125^{\circ}$ C temperature range and HA-5170-5 denotes the  $0^{\circ}$ C to  $+75^{\circ}$ C range. Military version (/883) product and data sheets available upon request.

### Pinouts

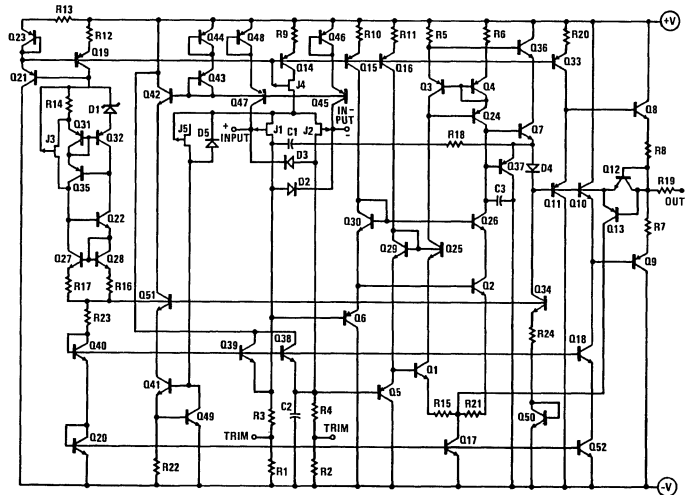
HA7-5170 (CERAMIC MINI-DIP)  
TOP VIEW



HA2-5170 (TO-99 METAL CAN)  
TOP VIEW



### Schematic



## Specifications HA-5170

### Absolute Maximum Ratings (Note)

$T_A = +25^\circ\text{C}$ , Unless Otherwise Specified.

|   |                      |
|---|----------------------|
| Voltage Between V+ and V- Terminals ..... | 44.0V                |
| Differential Input Voltage .....          | $\pm 30.0\text{V}$   |
| Output Short Circuit Duration .....       | Indefinite           |
| Power Dissipation (Note 2) .....          | 675mW                |
| Maximum Junction Temperature .....        | $+175^\circ\text{C}$ |

### Operating Temperature Ranges

|                                 |  |
|---------------------------------|--|
| HA-5170-2 .....                 | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ |
| HA-5170-5 .....                 | $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$    |
| Storage Temperature Range ..... | $-65^\circ\text{C} \leq T_A \leq +150^\circ\text{C}$ |

### Electrical Specifications V+ = +15V, V- = -15V, Unless Otherwise Specified.

| PARAMETER                                       | TEMP  | HA-5170-2<br>-55°C to +125°C |                    |     | HA-5170-5<br>0°C to +75°C |                    |     | UNITS                        |
|---|-------|------------------------------|--------------------|-----|---------------------------|--------------------|-----|------------------------------|
|   |       | MIN                          | TYP                | MAX | MIN                       | TYP                | MAX |                              |
| <b>INPUT CHARACTERISTICS</b>                    |       |                              |                    |     |                           |                    |     |                              |
| Offset Voltage                                  | +25°C | -                            | 0.1                | 0.3 | -                         | 0.1                | 0.3 | mV                           |
|   | Full  | -                            | -                  | 0.5 | -                         | -                  | 0.5 | mV                           |
| Average Offset Voltage Drift (Note 3)           | Full  | -                            | 2                  | 5   | -                         | 2                  | 5   | $\mu\text{V}/^\circ\text{C}$ |
| Bias Current                                    | +25°C | -                            | 20                 | 100 | -                         | 20                 | 100 | pA                           |
|   | Full  | -                            | 3                  | 30  | -                         | 0.1                | 2   | nA                           |
| Bias Current Average Drift                      | Full  | -                            | 3                  | -   | -                         | 3                  | -   | $\text{pA}/^\circ\text{C}$   |
| Offset Current                                  | +25°C | -                            | 3                  | 30  | -                         | 3                  | 60  | pA                           |
|   | Full  | -                            | -                  | 5   | -                         | -                  | 0.1 | nA                           |
| Offset Current Average Drift (Note 3)           | Full  | -                            | 0.3                | 1   | -                         | 0.3                | 1   | $\text{pA}/^\circ\text{C}$   |
| Common Mode Range                               | Full  | $\pm 10$                     | +15.1              | -   | $\pm 10$                  | +15.1              | -   | V                            |
|   |       |                              | -12                |     |                           | -12                |     | V                            |
| Differential Input Capacitance                  | +25°C | -                            | 80                 | 100 | -                         | 80                 | 100 | pF                           |
| Differential Input Resistance (Note 3)          | +25°C | $1 \times 10^{10}$           | $6 \times 10^{10}$ | -   | $1 \times 10^{10}$        | $6 \times 10^{10}$ | -   | $\Omega$                     |
| Input Capacitance (Single Ended)                | +25°C | -                            | 12                 | -   | -                         | 12                 | -   | pF                           |
| Input Noise Voltage                             | +25°C | -                            | 0.5                | 5   | -                         | 0.5                | 5   | $\mu\text{V}_{\text{p-p}}$   |
| 0.1Hz to 10Hz (Note 3)                          |       |                              |                    |     |                           |                    |     |                              |
| Input Noise Voltage Density (Note 3)            |       |                              |                    |     |                           |                    |     |                              |
| $f_0 = 10\text{Hz}$                             | +25°C | -                            | 20                 | 150 | -                         | 20                 | 150 | $\text{nV}/\sqrt{\text{Hz}}$ |
| $f_0 = 100\text{Hz}$                            | +25°C | -                            | 12                 | 50  | -                         | 12                 | 50  | $\text{nV}/\sqrt{\text{Hz}}$ |
| $f_0 = 1000\text{Hz}$                           | +25°C | -                            | 10                 | 25  | -                         | 10                 | 25  | $\text{nV}/\sqrt{\text{Hz}}$ |
| Input Noise Current Density (Note 3)            |       |                              |                    |     |                           |                    |     |                              |
| $f_0 = 10\text{Hz}$                             | +25°C | -                            | 0.05               | -   | -                         | 0.05               | -   | $\text{pA}/\sqrt{\text{Hz}}$ |
| $f_0 = 100\text{Hz}$                            | +25°C | -                            | 0.01               | -   | -                         | 0.01               | -   | $\text{pA}/\sqrt{\text{Hz}}$ |
| $f_0 = 1000\text{Hz}$                           | +25°C | -                            | 0.01               | 0.1 | -                         | 0.01               | 0.1 | $\text{pA}/\sqrt{\text{Hz}}$ |
| <b>TRANSFER CHARACTERISTICS</b>                 |       |                              |                    |     |                           |                    |     |                              |
| Large Signal Voltage Gain (Notes 4)             | +25°C | 300K                         | 600K               | -   | 300K                      | 600K               | -   | V/V                          |
|   | Full  | 200K                         | -                  | -   | 250K                      | -                  | -   | V/V                          |
| Common Mode Rejection Ratio (Note 5)            | Full  | 85                           | 100                | -   | 90                        | 100                | -   | dB                           |
| Minimum Stable Gain                             | +25°C | 1                            | -                  | -   | 1                         | -                  | -   | V/V                          |
| Closed Loop Bandwidth ( $A_{\text{VCL}} = +1$ ) | +25°C | 4                            | 8                  | -   | 4                         | 8                  | -   | MHz                          |
| <b>OUTPUT CHARACTERISTICS</b>                   |       |                              |                    |     |                           |                    |     |                              |
| Output Voltage Swing (Note 6)                   | +25°C | $\pm 10$                     | $\pm 12$           | -   | $\pm 10$                  | $\pm 12$           | -   | V                            |
| Full Power Bandwidth (Note 7)                   | +25°C | 80                           | 120                | -   | 80                        | 120                | -   | kHz                          |
| Output Current (Note 8)                         | +25°C | $\pm 10$                     | $\pm 15$           | -   | $\pm 10$                  | $\pm 15$           | -   | mA                           |
| Output Resistance (Note 3 & 9)                  | +25°C | -                            | 45                 | 100 | -                         | 45                 | 100 | $\Omega$                     |
| <b>TRANSIENT RESPONSE</b>                       |       |                              |                    |     |                           |                    |     |                              |
| Rise Time                                       | +25°C | -                            | 45                 | 100 | -                         | 45                 | 100 | ns                           |
| Slew Rate                                       | +25°C | 5                            | 8                  | -   | 5                         | 8                  | -   | V/ $\mu\text{s}$             |
| Settling Time (Notes 3 & 10)                    | +25°C | -                            | 1                  | 5   | -                         | 1                  | 5   | $\mu\text{s}$                |
| <b>POWER SUPPLY CHARACTERISTICS</b>             |       |                              |                    |     |                           |                    |     |                              |
| Supply Current                                  | Full  | -                            | 1.9                | 2.5 | -                         | 1.9                | 2.5 | mA                           |
| Power Supply Rejection Ratio (Note 11)          | Full  | 85                           | 105                | -   | 90                        | 105                | -   | dB                           |

#### NOTES:

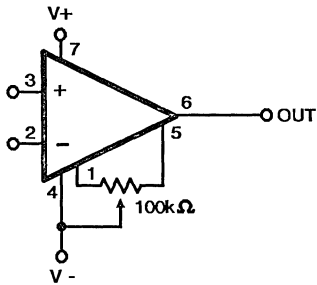
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8 mW/ $^\circ\text{C}$  for operation at ambient temperatures above  $+75^\circ\text{C}$ .
3. Parameter is not 100% tested. 90% of all units meet or exceed these specifications.
4.  $V_{\text{OUT}} = \pm 10$ ,  $R_L = 2\text{k}\Omega$ .
5.  $\Delta V_{\text{CM}} = \pm 10\text{V D.C.}$
6.  $R_L = 2\text{k}\Omega$ .
7.  $R_L = 2\text{k}\Omega$ ; Full power bandwidth guaranteed based on slew rate measurement using  $\text{FPBW} = \frac{\text{SLEW RATE}}{2\pi V_{\text{PEAK}}}$ .
8.  $V_{\text{OUT}} = \pm 10\text{V}$ .  $I_{\text{SC}}$  turns on at  $\approx 23\text{mA}$ .
9. Output resistance measured under open loop conditions ( $f = 100\text{Hz}$ ).
10. Settling time is measured to 0.1% of final value for a 10V output step and  $A_V = -1$ .
11.  $\Delta V_{\text{SUPPLY}} = \pm 10\text{V D.C. to } \pm 20\text{V D.C.}$

3

OPERATIONAL  
AMPLIFIERS

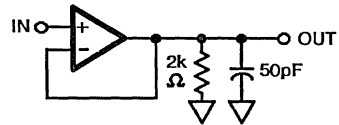
**Test Circuits**

**V<sub>OS</sub> ADJUSTMENT**



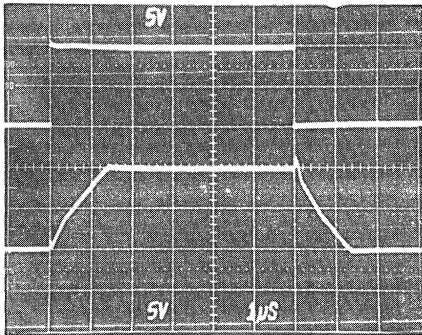
Tested Offset Adjustment Range is  $|V_{OS} + 1\text{mV}|$  minimum referred to output. Typical range is  $\pm 5\text{mV}$  with  $R_T = 1\text{k}\Omega$  and  $\pm 15\text{mV}$  with  $R_T = 100\text{k}\Omega$ .

**LARGE AND SMALL SIGNAL RESPONSE CIRCUIT**



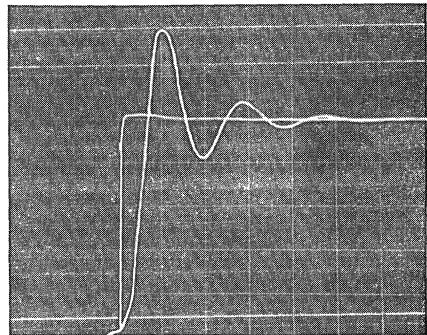
**LARGE SIGNAL RESPONSE**

Vertical Scale: 5V/Div.  
Horizontal Scale: 1μs/Div.

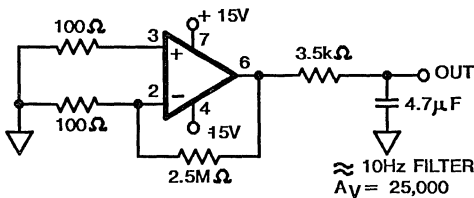


**SMALL SIGNAL RESPONSE**

Vertical Scale: 10mV/Div.  
Horizontal Scale: 100ns/Div.

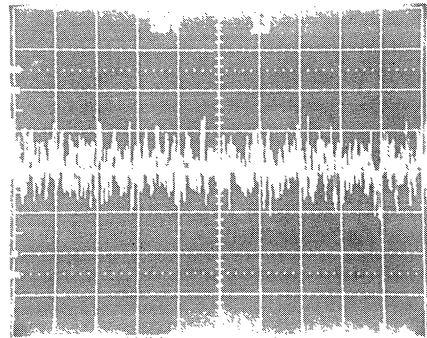


**LOW FREQUENCY NOISE TEST CIRCUIT**



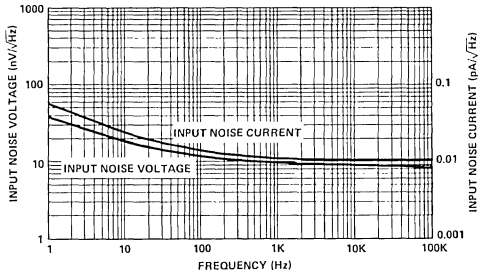
**HA-5170 LOW FREQUENCY NOISE (0.1Hz TO 10Hz)**

Vertical Scale: 200nV/Div. (Noise Referred to Input)  
5mV/Div. at Output,  $A_{VCL} = 25,000$ .  
Horizontal Scale: 1 Sec./Div.

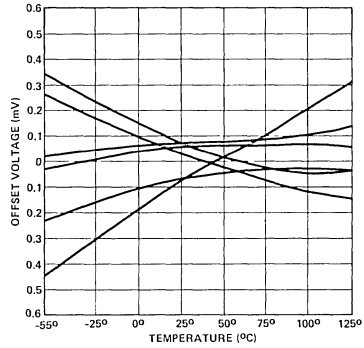


Typical Performance Curves

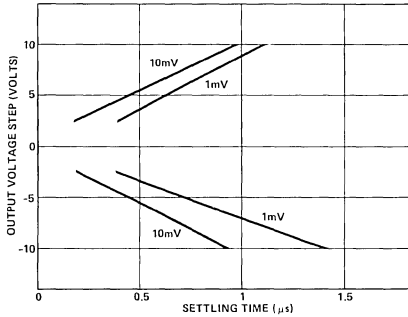
INPUT VOLTAGE NOISE vs. FREQUENCY



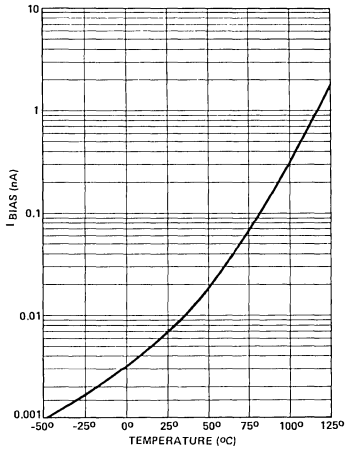
OFFSET VOLTAGE vs. TEMPERATURE DRIFT OF REPRESENTATIVE UNITS



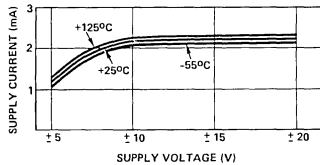
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



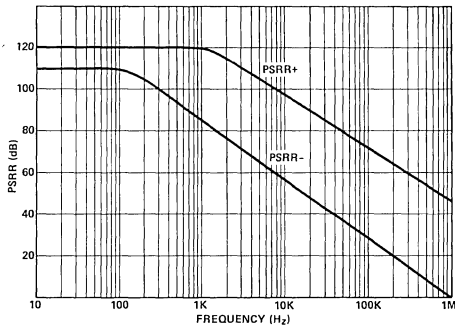
BIAS CURRENT vs. TEMPERATURE



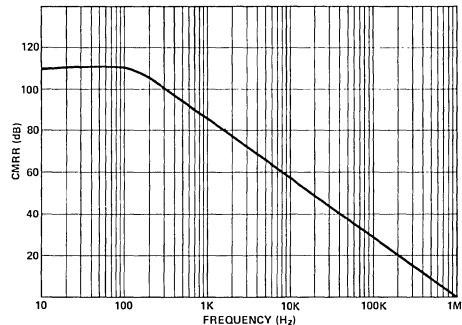
POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE AND TEMPERATURE



POWER SUPPLY REJECTION RATIO vs. FREQUENCY



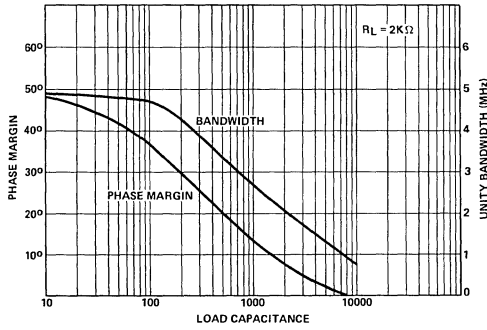
COMMON MODE REJECTION RATIO vs. FREQUENCY



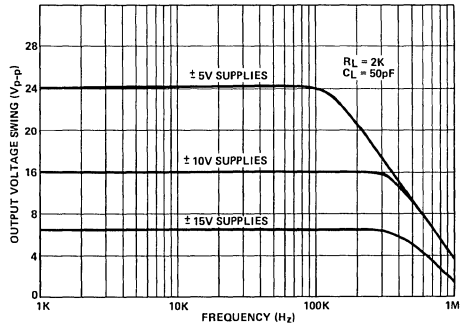

  
 OPERATIONAL AMPLIFIERS

**Typical Performance Curves (Continued)**

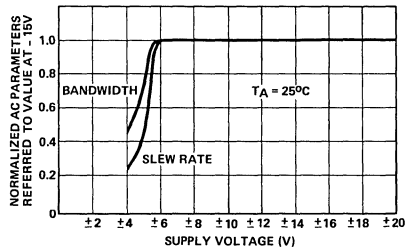
**SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE**



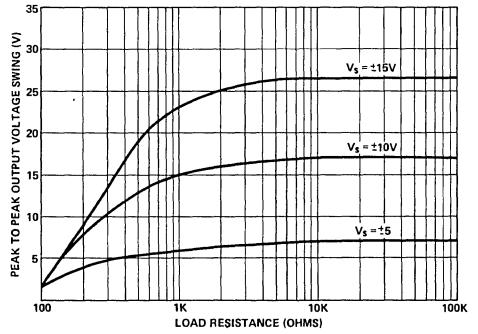
**OUTPUT VOLTAGE SWING vs. FREQUENCY AND SUPPLY VOLTAGE**



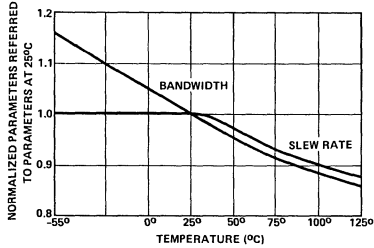
**NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE**



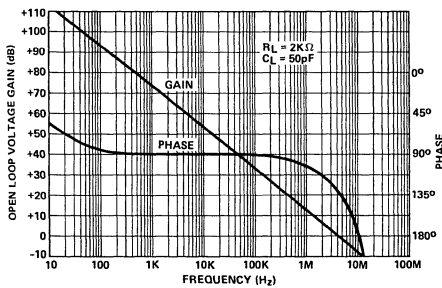
**MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE**



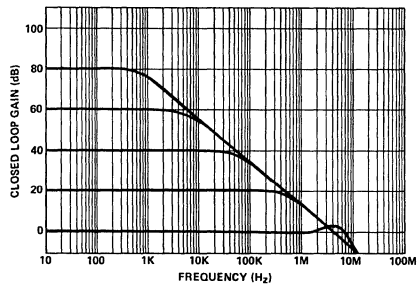
**NORMALIZED AC PARAMETERS vs. TEMPERATURE**



**OPEN LOOP FREQUENCY RESPONSE**



**CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS**



## Ultra-Low Offset Voltage Operational Amplifier

August 1991

### Features

- Low Offset Voltage ..... 10 $\mu$ V
- Low Offset Voltage Drift ..... 0.1 $\mu$ V/ $^{\circ}$ C
- High Voltage Gain ..... 150dB
- High CMRR ..... 140dB
- High PSRR ..... 135dB
- Low Noise ..... 8.8nV/ $\sqrt{\text{Hz}}$
- Low Power Consumption ..... 51mW Max.

### Applications

- High Gain Instrumentation Amplifiers
- Precision Control Systems
- Precision Integrators
- High Resolution Data Converters
- Precision Threshold Detectors
- Low Level Transducer Amplifiers

### Description

The HA-5177 is a monolithic, all bipolar, precision operational amplifier, utilizing Harris dielectric isolation and advance processing techniques. This design features a combination of precision input characteristics, wide bandwidth (2MHz) and high speed (0.8V/ $\mu$ s).

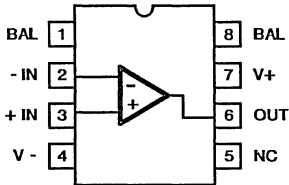
The HA-5177 uses advanced matching techniques and laser trimming to produce low offset voltage (10 $\mu$ V) and low offset voltage drift (0.1 $\mu$ V/ $^{\circ}$ C). This design also features low voltage noise (8.8nV/ $\sqrt{\text{Hz}}$ ), low current noise (0.32pA/ $\sqrt{\text{Hz}}$ ), nanoamp input currents, and 120dB minimum gain.

These outstanding features along with high CMRR (140dB) and high PSRR (135dB) make this unity gain stable amplifier ideal for high resolution data acquisition systems, precision integrators, and low level transducer amplifiers.

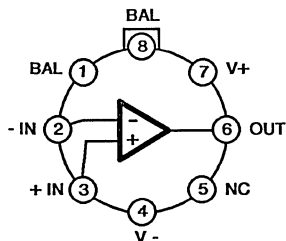
The HA-5177 can be used as a direct replacement for the OP05, OP07, and OP77 while offering higher bandwidth and slew rate. The HA-5177 is packaged in an 8 pin (TO-99) Metal Can and Ceramic 8 pin Mini-DIP and is pin compatible with many existing op amps. See the HA-5177/883 data sheet for military grade parts and LCC package.

### Pinouts

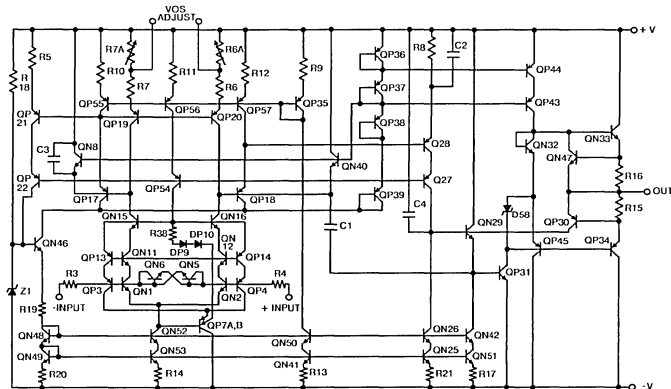
HA7-5177 (CERAMIC MINI-DIP)  
TOP VIEW



HA2-5177 (TO-99 METAL CAN)  
TOP VIEW



### Schematic





## Specifications HA-5177

### Absolute Maximum Ratings (Note 1)

|   |                         |
|---|-------------------------|
| Voltage Between V+ and V- Terminals ..... | 44V                     |
| Differential Input Voltage .....          | ±15V                    |
| Output Current .....                      | Short Circuit Protected |

### Operating Temperature Ranges

|                                    |                                 |
|------------------------------------|---------------------------------|
| HA-5177A/5177-2 .....              | -55°C ≤ T <sub>A</sub> ≤ +125°C |
| HA-5177A/5177-5 .....              | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| Storage Temperature Range .....    | -65°C ≤ T <sub>A</sub> ≤ +150°C |
| Maximum Junction Temperature ..... | +175°C                          |

### Electrical Specifications V+ = +15V, V- = -15V, Unless Otherwise Specified

| PARAMETER                                     | TEMP                  | HA-5177A |      |       | HA-5177 |      |       | UNITS             |      |
|---|-----------------------|----------|------|-------|---------|------|-------|-------------------|------|
|   |                       | MIN      | TYP  | MAX   | MIN     | TYP  | MAX   |                   |      |
| <b>INPUT CHARACTERISTICS</b>                  |                       |          |      |       |         |      |       |                   |      |
| Offset Voltage                                | +25°C                 | -        | 10   | 25    | -       | 20   | 60    | μV                |      |
|   | Full                  | -        | 25   | 60    | -       | 40   | 100   | μV                |      |
| Average Offset Voltage Drift                  | Full                  | -        | 0.1  | 0.3   | -       | 0.2  | 0.6   | μV/°C             |      |
| Bias Current                                  | +25°C                 | -        | 1.2  | 2     | -       | 1.2  | 6     | nA                |      |
|   | Full                  | -        | 2.4  | 4     | -       | 2.4  | 8     | nA                |      |
| Bias Current Average Drift                    | Full                  | -        | 8    | 25    | -       | 15   | 35    | pA/°C             |      |
| Offset Current                                | +25°C                 | -        | 0.6  | 2     | -       | 0.6  | 6     | nA                |      |
|   | Full                  | -        | 1.0  | 4     | -       | 1.0  | 8     | nA                |      |
| Offset Current Average Drift                  | Full                  | -        | 1.5  | 25    | -       | 1.5  | 50    | pA/°C             |      |
| Common Mode Range                             | Full                  | ±12      | -    | -     | ±12     | -    | -     | V                 |      |
| Differential Input Resistance                 | +25°C                 | -        | 47   | -     | -       | 47   | -     | MΩ                |      |
| Input Noise Voltage 0.1 Hz to 10 Hz           | +25°C                 | -        | 0.35 | 0.6   | -       | 0.35 | 0.6   | μV <sub>p-p</sub> |      |
| Input Noise Voltage Density                   |                       |          |      |       |         |      |       |                   |      |
| f <sub>o</sub> = 10 Hz                        | +25°C                 | -        | 13   | 18    | -       | 13   | 18    | nV/√Hz            |      |
| f <sub>o</sub> = 100 Hz                       | +25°C                 | -        | 10   | 13    | -       | 10   | 13    | nV/√Hz            |      |
| f <sub>o</sub> = 1000 Hz                      | +25°C                 | -        | 8.8  | 11    | -       | 8.8  | 11    | nV/√Hz            |      |
| Input Noise Current 0.1 Hz to 10 Hz           | +25°C                 | -        | 14   | 45    | -       | 14   | 45    | pA <sub>p-p</sub> |      |
| Input Noise Current Density                   |                       |          |      |       |         |      |       |                   |      |
| f <sub>o</sub> = 10 Hz                        | +25°C                 | -        | 1.1  | 4     | -       | 7.1  | 10    | pA/√Hz            |      |
| f <sub>o</sub> = 100 Hz                       | +25°C                 | -        | 0.55 | 2.3   | -       | 3.3  | 5     | pA/√Hz            |      |
| f <sub>o</sub> = 1000 Hz                      | +25°C                 | -        | 0.32 | 1     | -       | 1.2  | 2     | pA/√Hz            |      |
| <b>TRANSFER CHARACTERISTICS</b>               |                       |          |      |       |         |      |       |                   |      |
| Large Signal Voltage Gain (Note 2)            | +25°C                 | 134      | 150  | -     | 126     | 150  | -     | dB                |      |
|   | Full                  | 126      | 140  | -     | 120     | 140  | -     | dB                |      |
| Common Mode Rejection Ratio (Note 3)          | Full                  | 120      | 140  | -     | 110     | 140  | -     | dB                |      |
| Closed Loop Bandwidth (A <sub>VCL</sub> = +1) | +25°C                 | 0.6      | 2    | -     | 0.6     | 2    | -     | MHz               |      |
| <b>OUTPUT CHARACTERISTICS</b>                 |                       |          |      |       |         |      |       |                   |      |
| Output Voltage Swing                          | R <sub>L</sub> = 600Ω | +25°C    | ±10  | ±12.5 | -       | ±10  | ±12.5 | -                 | V    |
|   | R <sub>L</sub> = 2K   | +25°C    | ±12  | ±13   | -       | ±12  | ±13   | -                 | V    |
|   | R <sub>L</sub> = 2K   | Full     | ±12  | ±12.5 | -       | ±12  | ±12.5 | -                 | V    |
| Full Power Bandwidth (Note 5)                 |                       | +25°C    | 8    | 10    | -       | 8    | 10    | -                 | kHz  |
| Output Current (Note 6)                       |                       | +25°C    | 15   | 20    | -       | 15   | 20    | -                 | mA   |
| Output Resistance                             |                       | +25°C    | -    | 60    | -       | -    | 60    | -                 | Ω    |
| <b>TRANSIENT RESPONSE</b>                     |                       |          |      |       |         |      |       |                   |      |
| Rise Time (Note 10)                           | +25°C                 | -        | 310  | 420   | -       | 310  | 420   | -                 | ns   |
| Stew Rate (Note 11)                           | +25°C                 | 0.5      | 0.8  | -     | 0.5     | 0.8  | -     | -                 | V/μs |
| Settling Time (Notes 7, 8)                    | +25°C                 | -        | 14   | -     | -       | 14   | -     | -                 | μs   |
| Overshoot (Note 10)                           | +25°C                 | -        | 10   | 40    | -       | 10   | 40    | -                 | %    |
| <b>POWER SUPPLY CHARACTERISTICS</b>           |                       |          |      |       |         |      |       |                   |      |
| Supply Current                                | Full                  | -        | 1.2  | 1.7   | -       | 1.2  | 1.7   | -                 | mA   |
| Power Supply Rejection Ratio (Note 9)         | Full                  | 110      | 135  | -     | 110     | 135  | -     | -                 | dB   |

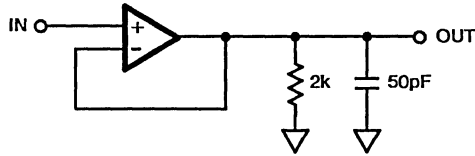
#### NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. V<sub>OUT</sub> = ±10V, R<sub>L</sub> = 2kΩ
3. ΔV<sub>CM</sub> = ±10V D.C.
4. R<sub>L</sub> = 2K

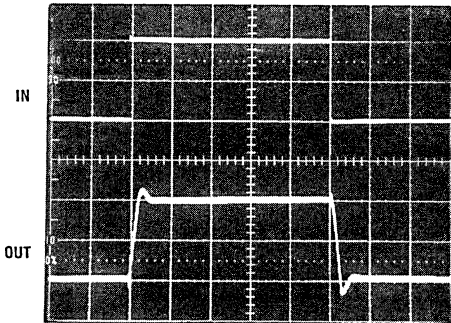
5. Full power bandwidth guaranteed based on slew rate measurement using  $FBW = \frac{\text{Slew Rate}}{2nV_{PEAK}}$ , V<sub>PEAK</sub> = 10V.
6. V<sub>OUT</sub> = ±10.
7. Refer to test circuits section of the data sheet.
8. Settling time is measured to 0.1% of final value for a 10V output step and A<sub>V</sub> = +1.
9. ΔV<sub>SUPPLY</sub> = ±10V D.C. to ±20V D.C.
10. A<sub>V</sub> = 1, R<sub>L</sub> = 2K, V<sub>OUT</sub> = ±200mV
11. A<sub>V</sub> = 1, R<sub>L</sub> = 2K, V<sub>OUT</sub> = 0 to ±3V

Test Circuits

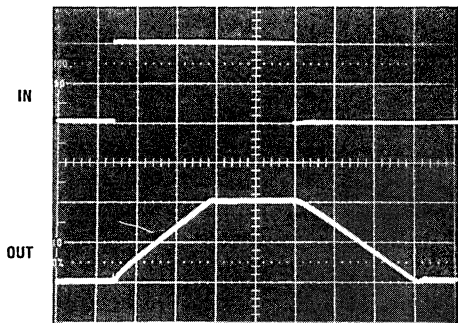
SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



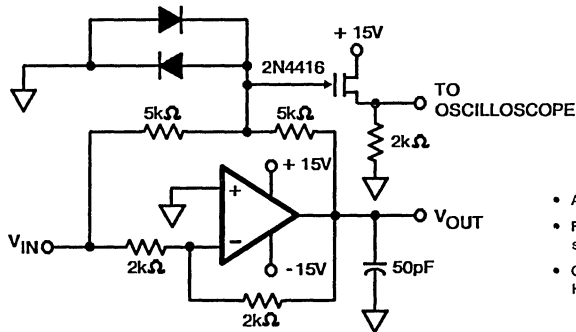
**SMALL SIGNAL RESPONSE**  
Vertical Scale: (Volts: 100mV/Div.)  
Horizontal Scale: (Time: 2μs/Div.)



**LARGE SIGNAL RESPONSE**  
Vertical Scale: (Volts: 5V/Div.)  
Horizontal Scale: (Time: 5μs/Div.)



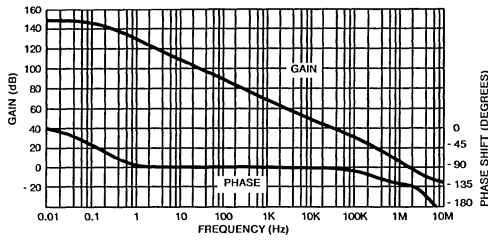
SETTLING TIME CIRCUIT



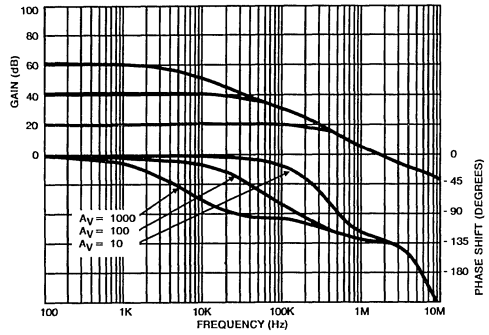
- $A_v = -1$
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

Typical Performance Curves  $V_S = \pm 15V, T_A = +25^\circ C$

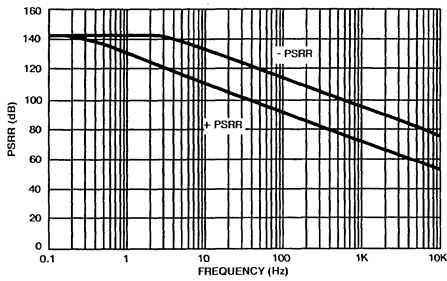
OPEN LOOP GAIN AND PHASE vs. FREQUENCY



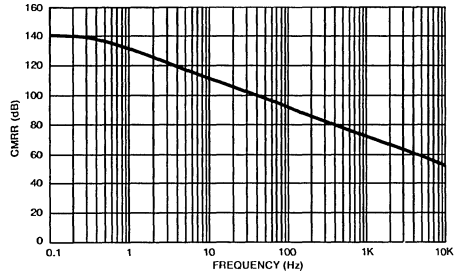
VARIOUS CLOSED LOOP GAINS vs. FREQUENCY  
 $R_L = 2K, C_L = 50pF$



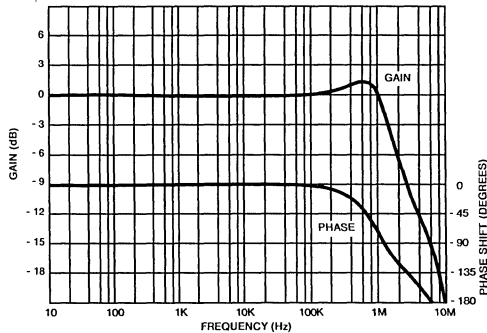
PSRR vs. FREQUENCY



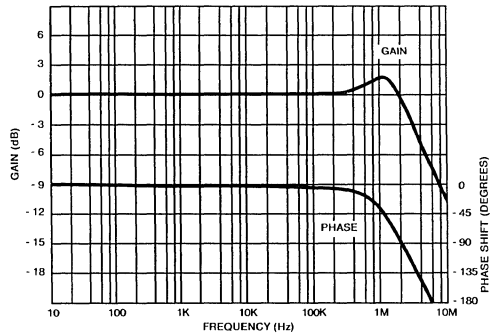
CMRR vs. FREQUENCY



CLOSED LOOP GAIN AND PHASE vs. FREQUENCY  
 $A_V = -1, R_L = 2K, C_L = 50pF$

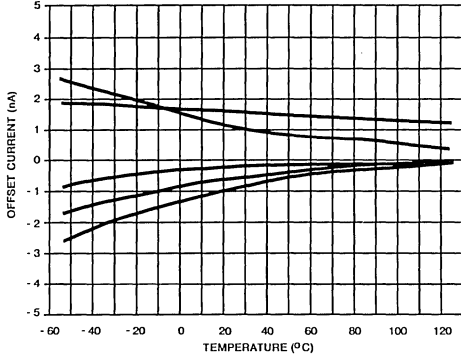


CLOSED LOOP GAIN AND PHASE vs. FREQUENCY  
 $A_V = +1, R_L = 2K, C_L = 50pF$

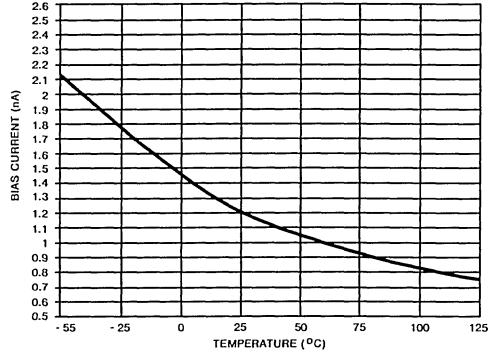


**Typical Performance Curves**  $V_S = \pm 15V, T_A = +25^\circ C$

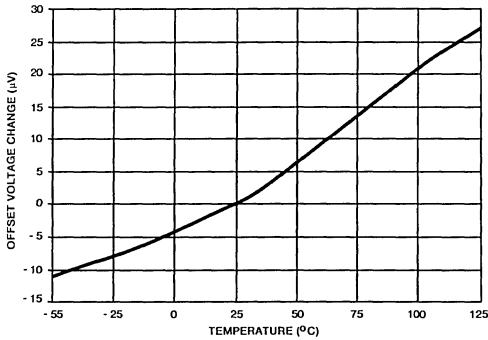
**OFFSET CURRENT vs. TEMPERATURE**  
Five Representative Units



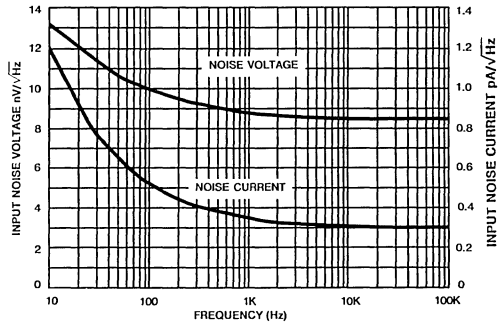
**BIAS CURRENT vs. TEMPERATURE**



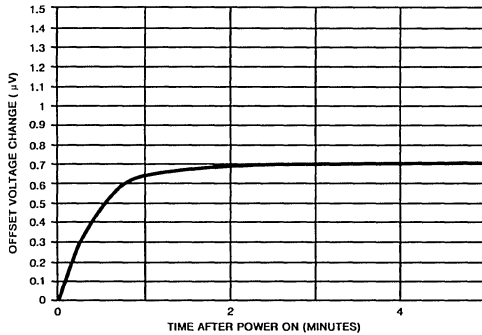
**OFFSET VOLTAGE vs. TEMPERATURE**



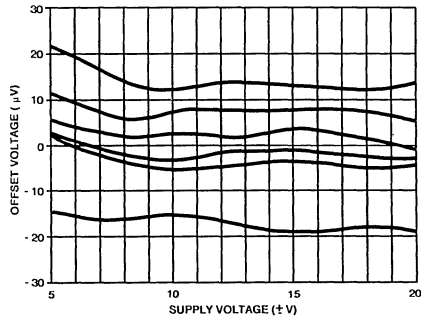
**INPUT NOISE vs. FREQUENCY**



**OFFSET VOLTAGE WARM-UP DRIFT**



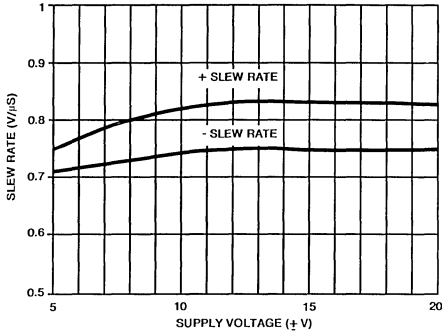
**OFFSET VOLTAGE vs. SUPPLY VOLTAGE**  
Six Representative Units



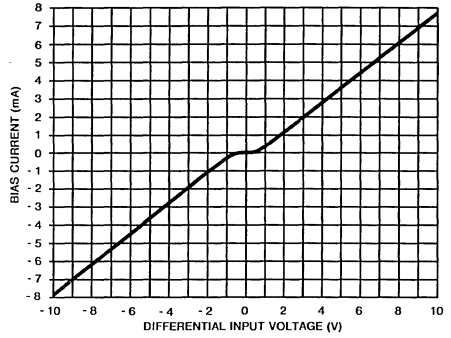
# HA-5177

## Typical Performance Curves $V_S = \pm 15V, T_A = +25^\circ C$

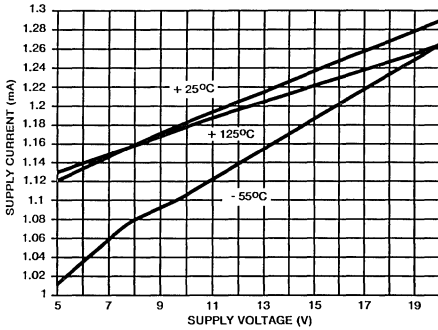
**SLEW RATE vs. SUPPLY VOLTAGE**  
 $A_V = -1, R_L = 2K, C_L = 50pF$



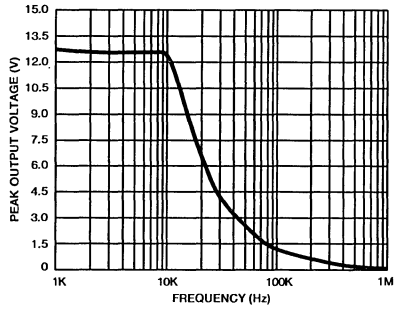
**BIAS CURRENT vs. DIFFERENTIAL INPUT VOLTAGE**



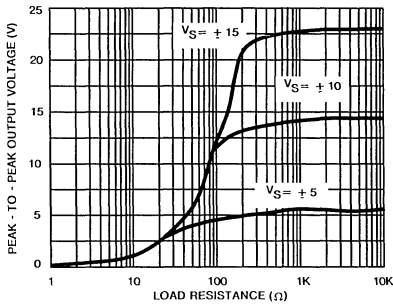
**SUPPLY CURRENT vs. SUPPLY VOLTAGE**



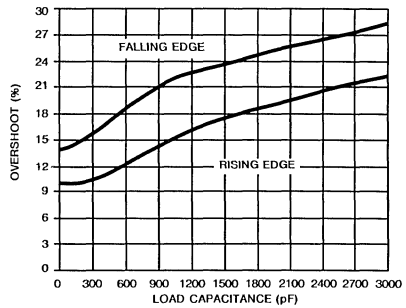
**OUTPUT VOLTAGE vs. FREQUENCY**  
 $A_V = -1, R_L = 2K, C_L = 50pF$



**OUTPUT VOLTAGE vs. LOAD RESISTANCE**  
 $A_V = -1, V_{IN} = 100Hz, C_L = 50pF$



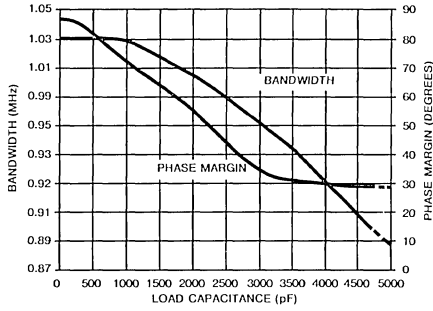
**OVERSHOOT vs. LOAD CAPACITANCE**  
 $V_S = \pm 15V, A_V = +1, V_{OUT} = \pm 200mV$



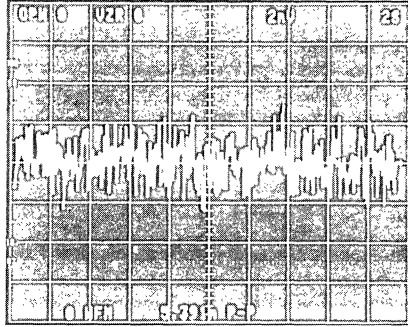
# HA-5177

## Typical Performance Curves $V_S = \pm 15V, T_A = +25^\circ C$

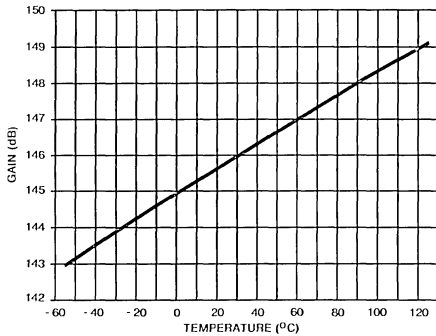
**SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE**  
 $A_V = +1$



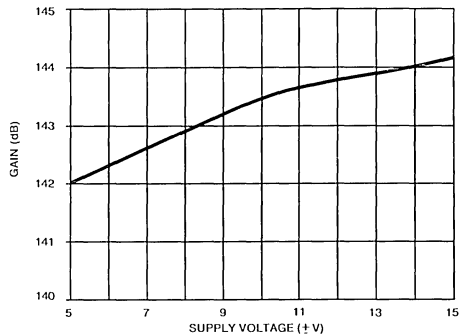
**PEAK-TO-PEAK NOISE 0.1Hz TO 10Hz**  
 $A_V = 25,000, 0.22\mu V_{p-p} RTI$



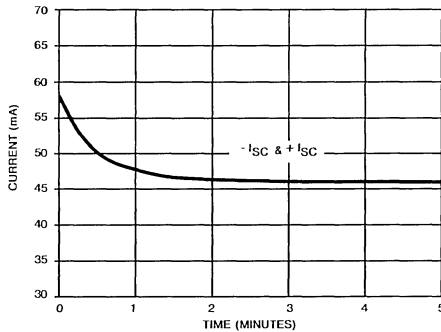
**OPEN LOOP GAIN vs. TEMPERATURE**



**OPEN LOOP GAIN vs. SUPPLY VOLTAGE**



**OUTPUT SHORT CIRCUIT CURRENT vs. TIME**  
 $V_{IN} = \pm 10V, A_V = -1$



  
**OPERATIONAL AMPLIFIERS**

# HA-5177

## Applications Information

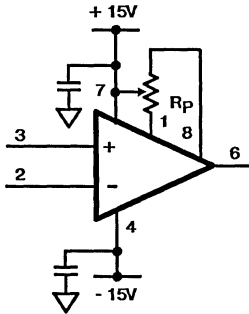
### Operation Below $\pm 5V$ Supply

The HA-5177 performs well down to  $\pm 5V$  supplies.

At  $\pm 5V$  supplies there is a slight degradation of slew rate and open loop gain. There is very little change in bias currents and offset voltage.

### Offset Adjustment

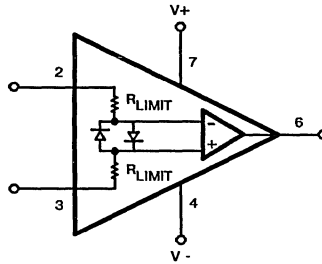
The following is the recommended  $V_{IO}$  adjust configuration:



Setting  $R_p = 20K$  will give an adjustment range of  $\pm 2.6mV$ .

### Input Protection

The HA-5177 input stage has built in back-to-back protection diodes with series current limiting resistors.



The Bias currents will increase when a differential voltage of 0.7 volts is exceeded.

The internal current limiting resistors sufficiently limit current therefore, no external resistors are required.

Refer to the "Bias Current vs. Differential Input Voltage" curve in the Typical Performance Curves section.

## Die Characteristics

|                                     |   |
|-------------------------------------|---|
| Transistor Count .....              | 71  |
| Die Dimensions .....                | 102 x 71.7 x 19 mils<br>(2590 x 1820 x 485 $\mu$ m) |
| Substrate Potential* .....          | V-  |
| Process .....                       | High Frequency Bipolar DI                           |
| Passivation .....                   | Silox   |
| Thermal Constants ( $^{\circ}C/W$ ) | $\theta_{ja}$ $\theta_{jc}$                         |
| Ceramic Mini-DIP, HA7-5177          | 154    74   |
| Metal Can TO-99, HA2-5177           | 124    38   |

\* The substrate may be left floating (insulating Die Mount) or it may be mounted on a conductor at V- potential.

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### Features

- Fast Settling Time (0.1%) ..... 70ns
- Very High Slew Rate ..... 200V/ $\mu$ s
- Wide Gain-Bandwidth ( $A_V \geq 5$ ) ..... 150MHz
- Power Bandwidth ..... 6.5MHz
- Low Offset Voltage ..... 3mV
- Input Noise Voltage ..... 6nV/ $\sqrt{\text{Hz}}$
- Monolithic Bipolar D.I. Construction

### Description

HA-5190/5195 are monolithic operational amplifiers featuring an ultimate combination of speed, precision, and bandwidth. Employing monolithic bipolar construction coupled with Dielectric Isolation, these devices are capable of delivering an unparalleled 200V/ $\mu$ s slew rate with a settling time of 70ns (0.1%, 5V output step). These truly differential amplifiers are designed to operate at gains  $\geq 5$  without the need for external compensation. Other outstanding HA-5190/5195 features are 150MHz gain-bandwidth-product and 6.5MHz full power bandwidth. In addition to these dynamic characteristics, these amplifiers also have excellent input characteristics such as 3mV offset voltage and 6.0nV/ $\sqrt{\text{Hz}}$  input voltage noise at 1kHz.

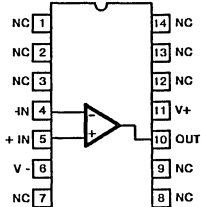
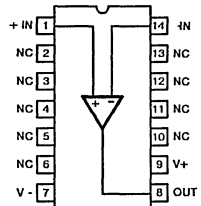
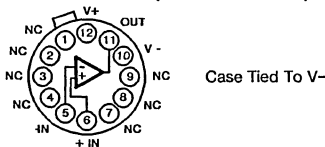
### Applications

- Fast, Precise D/A Converters
- High Speed Sample-Hold Circuits
- Pulse and Video Amplifiers
- WideBand Amplifiers
- Replace Costly Hybrids

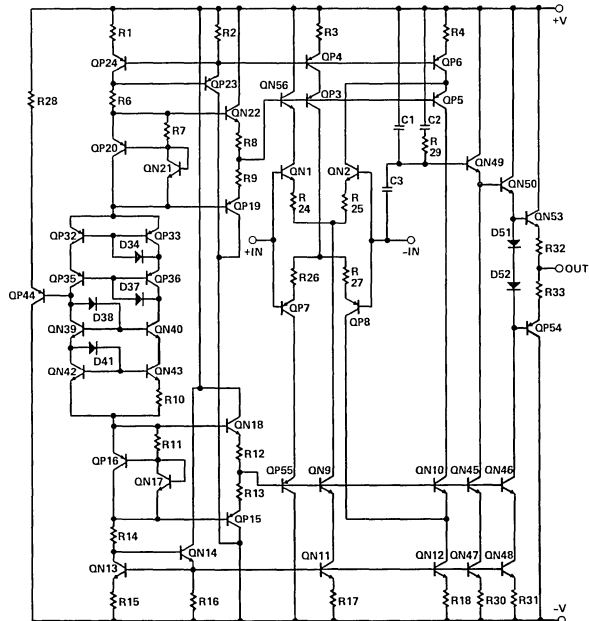
With 200V/ $\mu$ s slew rate and 70ns settling time, these devices make ideal output amplifiers for accurate, high speed D/A converters or the main components in high speed sample/hold circuits. The 5190/5195 are also ideally suited for a variety of pulse and wideband video amplifiers. Please refer to Application Notes 525 and 526 for some of these application designs.

The HA-5190 is specified over the  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  range while the HA-5195 is specified from  $0^\circ\text{C}$  to  $+75^\circ\text{C}$ . The HA-5190/5195 are available in 12 pin Metal Can (TO-8) and 14 pin Ceramic DIP packages. The HA-5195 is also available in SOIC packaging. At temperatures above  $+75^\circ\text{C}$  a heat sink is required for the HA-5190 (see Note 2 and Application Note 556). For military versions, please request the HA-5190/833 data sheet.

### Pinouts TOP VIEWS

**HA1-5190/5195 (CERAMIC DIP)**

**HA9P5195 (SOIC)**

**HA2-5190/5195 (TO-8 METAL CAN)**


### Schematic





## Specifications HA-5190/5195

### Absolute Maximum Ratings (Note 1)

|   |                                       |
|---|---------------------------------------|
| Voltage Between V+ and V- Terminals .....   | 35V                                   |
| Differential Input Voltage .....            | ±6V                                   |
| Output Current .....                        | 50mA (Peak)                           |
| Internal Power Dissipation (Note 2) .....   | 870mW (Cerdip);<br>1W (TO-8) Free Air |
| Maximum Junction Temperature (Note 2) ..... | +175°C                                |

### Operating Temperature Ranges

|                                 |                                 |
|---------------------------------|---------------------------------|
| HA-5190-2 .....                 | -55°C ≤ T <sub>A</sub> ≤ +125°C |
| HA-5195-5 .....                 | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| Storage Temperature Range ..... | -65°C ≤ T <sub>A</sub> ≤ +150°C |

### Electrical Specifications V<sub>SUPPLY</sub> = ±15V; R<sub>L</sub> = 200Ω, Unless Otherwise Specified.

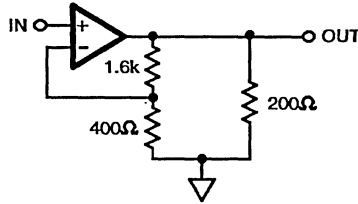
| PARAMETER   | TEMP  | HA-5190-2 |     |     | HA-5195-5 |     |     | UNITS  |
|---|-------|-----------|-----|-----|-----------|-----|-----|--------|
|   |       | MIN       | TYP | MAX | MIN       | TYP | MAX |        |
| <b>INPUT CHARACTERISTICS</b>                        |       |           |     |     |           |     |     |        |
| Offset Voltage                                      | +25°C | -         | 3   | 5   | -         | 3   | 6   | mV     |
|   | Full  | -         | -   | 10  | -         | -   | 10  | mV     |
| Average Offset Voltage Drift                        | Full  | -         | 20  | -   | -         | 20  | -   | μV/°C  |
| Bias Current  | +25°C | -         | 5   | 15  | -         | 5   | 15  | μA     |
|   | Full  | -         | -   | 20  | -         | -   | 20  | μA     |
| Offset Current                                      | +25°C | -         | 1   | 4   | -         | 1   | 4   | μA     |
|   | Full  | -         | -   | 6   | -         | -   | 6   | μA     |
| Input Resistance                                    | +25°C | -         | 10  | -   | -         | 10  | -   | kΩ     |
| Input Capacitance                                   | +25°C | -         | 1   | -   | -         | 1   | -   | pF     |
| Common Mode Range                                   | Full  | ±5        | -   | -   | ±5        | -   | -   | V      |
| Input Noise Current (f = 1kHz, R <sub>g</sub> = 0Ω) | +25°C | -         | 5   | -   | -         | 5   | -   | pA/√Hz |
| Input Noise Voltage (f = 1kHz, R <sub>g</sub> = 0Ω) | +25°C | -         | 6   | -   | -         | 6   | -   | nV/√Hz |
| <b>TRANSFER CHARACTERISTICS</b>                     |       |           |     |     |           |     |     |        |
| Large Signal Voltage Gain (Notes 3)                 | +25°C | 15K       | 30K | -   | 10K       | 30K | -   | V/V    |
|   | Full  | 5K        | -   | -   | 5K        | -   | -   | V/V    |
| Common Mode Rejection Ratio (Note 4)                | Full  | 74        | 95  | -   | 74        | 95  | -   | dB     |
| Minimum Stable Gain                                 | +25°C | 5         | -   | -   | 5         | -   | -   | V/V    |
| Gain-Bandwidth-Product (Notes 5 & 6)                | +25°C | -         | 150 | -   | -         | 150 | -   | MHz    |
| <b>OUTPUT CHARACTERISTICS</b>                       |       |           |     |     |           |     |     |        |
| Output Voltage Swing (Note 3)                       | Full  | ±5        | ±8  | -   | ±5        | ±8  | -   | V      |
| Output Current (Note 3)                             | +25°C | ±25       | ±30 | -   | ±25       | ±30 | -   | mA     |
| Output Resistance                                   | +25°C | -         | 30  | -   | -         | 30  | -   | Ω      |
| Full Power Bandwidth (Note 3 & 7)                   | +25°C | 5         | 6.5 | -   | 5         | 6.5 | -   | MHz    |
| <b>TRANSIENT RESPONSE (Note 8)</b>                  |       |           |     |     |           |     |     |        |
| Rise Time   | +25°C | -         | 13  | 18  | -         | 13  | 18  | ns     |
| Overshoot   | +25°C | -         | 8   | -   | -         | 8   | -   | %      |
| Slew Rate   | +25°C | 160       | 200 | -   | 160       | 200 | -   | V/μs   |
| Settling Time:                                      |       |           |     |     |           |     |     |        |
| 5V Step to 0.1%                                     | +25°C | -         | 70  | -   | -         | 70  | -   | ns     |
| 5V Step to 0.01%                                    | +25°C | -         | 100 | -   | -         | 100 | -   | ns     |
| 2.5V Step to 0.1%                                   | +25°C | -         | 50  | -   | -         | 50  | -   | ns     |
| 2.5V Step to 0.01%                                  | +25°C | -         | 80  | -   | -         | 80  | -   | ns     |
| <b>POWER SUPPLY CHARACTERISTICS</b>                 |       |           |     |     |           |     |     |        |
| Supply Current                                      | Full  | -         | 19  | 28  | -         | 19  | 28  | mA     |
| Power Supply Rejection Ratio (Note 9)               | Full  | 70        | 90  | -   | 70        | 90  | -   | dB     |

#### NOTES:

1. Absolute Maximum Ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Recommended heat sinks: For TO-8 Metal Can, Thermalloy #2240A (θ<sub>SA</sub> = 27°C/W) or #2268B (θ<sub>SA</sub> = 24°C/W). For 14 pin Ceramic DIP: AAVID #5602B (θ<sub>SA</sub> = 16°C/W). See Die Characteristics Section for θ<sub>JA</sub>/θ<sub>JC</sub> values.
3. R<sub>L</sub> = 200Ω, C<sub>L</sub> < 10pF, V<sub>OUT</sub> = ±5V.
4. ΔV<sub>CM</sub> = ±5V.
5. V<sub>OUT</sub> = 90mV.
6. A<sub>V</sub> = 10.
7. Full power bandwidth guaranteed based on slew rate measurement using  $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
8. Refer to Test Circuits section of data sheet.
9. ΔV<sub>SUPPLY</sub> = ±10V D.C. to ±20V D.C.

Test Circuits

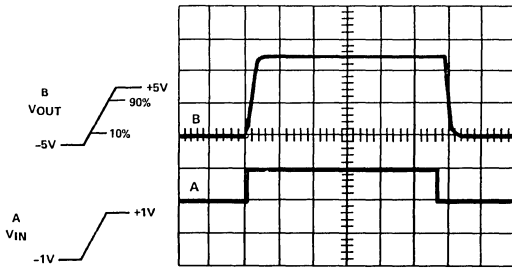
LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT\*



$A_V = 5$   
\*  $C_L < 10\text{pF}$

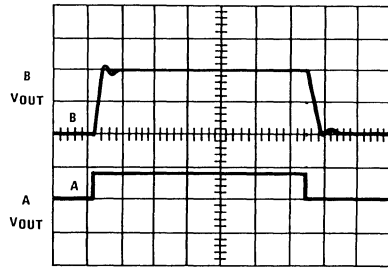
LARGE SIGNAL RESPONSE

Vertical Scale: (Volts: A = 2.0V/Div., B = 4.0/Div.)  
Horizontal Scale: (Time: 100ns/Div.)

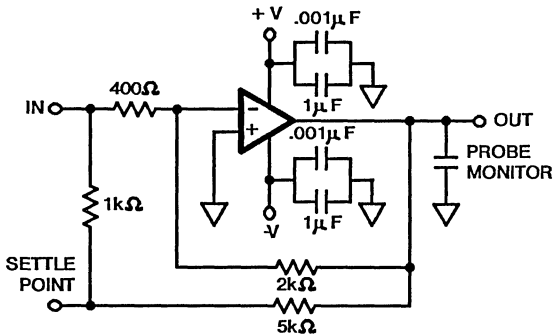


SMALL SIGNAL RESPONSE

Vertical Scale: (Volts: A = 50mV/Div., B = 100mV/Div.)  
Horizontal Scale: (Time: 100ns/Div.)



SETTLING TIME TEST CIRCUIT

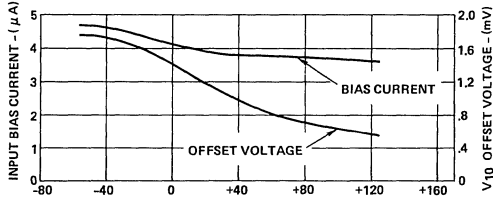


- $A_V = -5$
- Load Capacitance should be less than 10pF.
- It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
- Settle Point (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

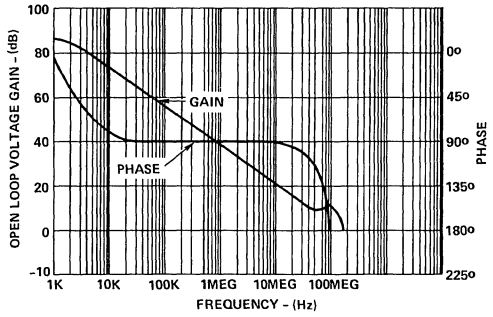
# HA-5190/5195

**Typical Performance Curves**  $V_+ = +15V$ ,  $V_- = -15V$ ,  $T_A = +25^\circ C$ , Unless Otherwise Specified.

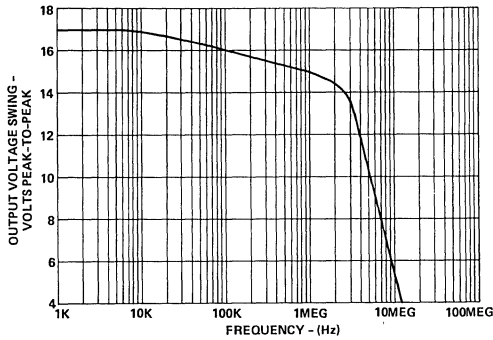
**INPUT OFFSET VOLTAGE AND BIAS CURRENT vs. TEMPERATURE**



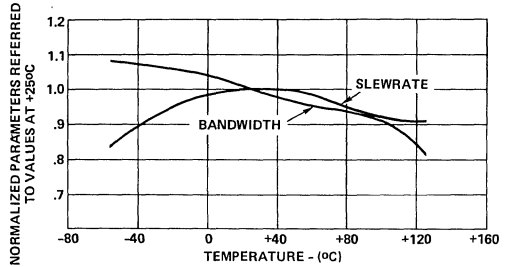
**OPEN LOOP FREQUENCY RESPONSE**



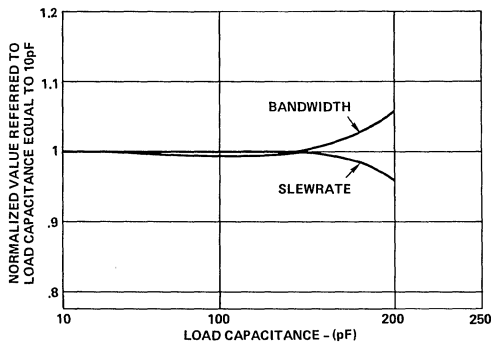
**OUTPUT VOLTAGE SWING vs. FREQUENCY**



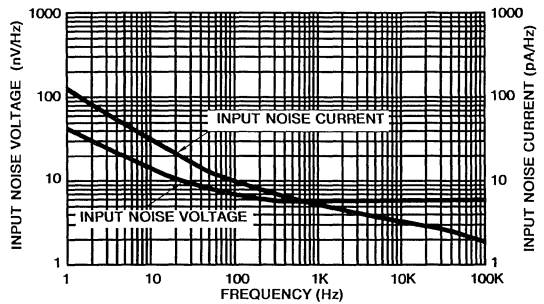
**NORMALIZED AC PARAMETERS vs. TEMPERATURE**



**NORMALIZED AC PARAMETERS vs. LOAD CAPACITANCE**

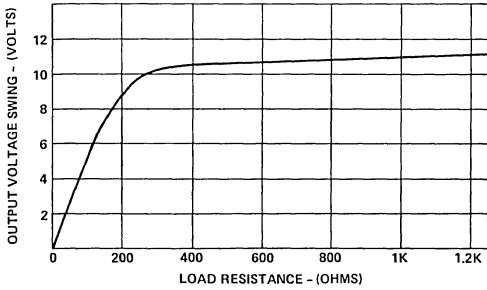


**INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY**

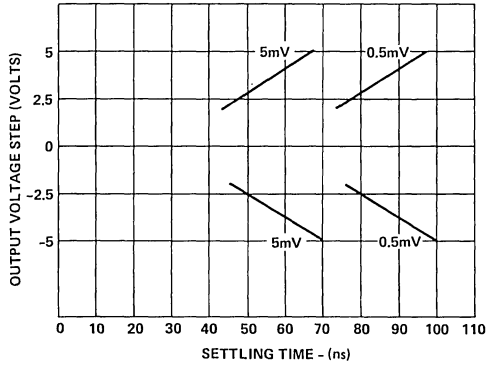


Typical Performance Curves (Continued)

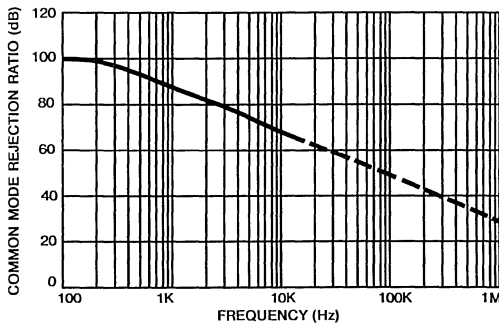
OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



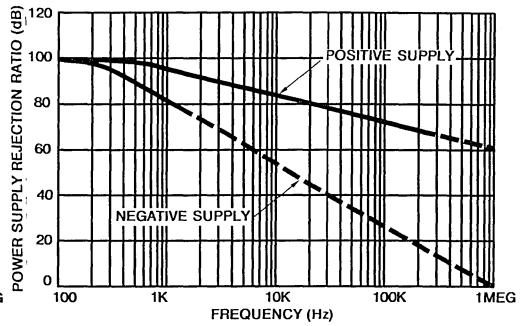
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



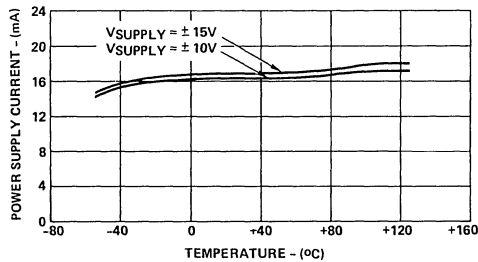
COMMON MODE REJECTION RATIO vs. FREQUENCY



POWER SUPPLY REJECTION RATIO vs. FREQUENCY



POWER SUPPLY CURRENT vs. TEMPERATURE

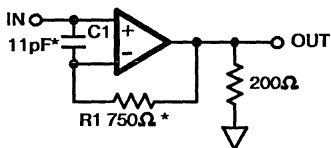


**Applying the HA-5190/5195**

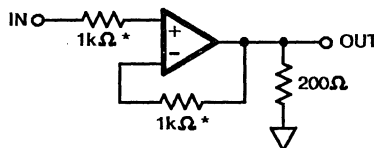
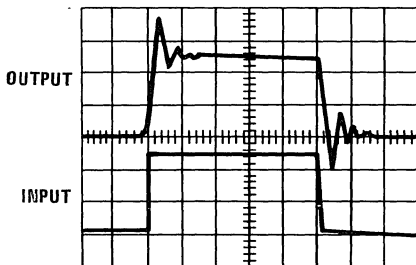
1. **POWER SUPPLY DECOUPLING:** Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01 $\mu$ F ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
2. **STABILITY CONSIDERATIONS:** HA-5190/5195 is stable at gains > 5. Gains < 5 are covered elsewhere in this data sheet. Feedback resistors should be of carbon composition located as near to the input terminals as possible.
3. **WIRING CONSIDERATIONS:** Video pulse circuits should be built on a ground plane. Minimum point to point connections directly to the amplifier terminals should be used. When ground planes cannot be used, good single point grounding techniques should be applied.
4. **OUTPUT SHORT CIRCUIT:** HA-5190/5195 does not have output short circuit protection. Short circuits to ground can be tolerated for approximately 10 seconds. Short circuits to either supply will result in immediate destruction of the device.
5. **HEAVY CAPACITIVE LOADS:** When driving heavy capacitive loads (> 100pF) a small resistor (< 100 $\Omega$ ) should be connected in series with the output and inside the feedback loop.

**Typical Applications** (Also see Application Notes 525 and 526)

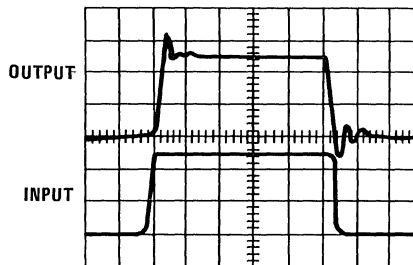
**SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY: NONINVERTING**



Vertical Scale: (Volts: 2V/Div.)  
Horizontal Scale: (Time: 100ns/Div.)

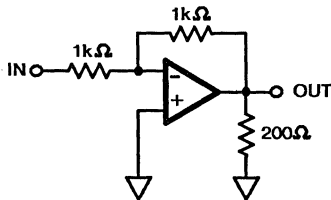


Vertical Scale: (Volts: 2V/Div.)  
Horizontal Scale: (Time: 100ns/Div.)

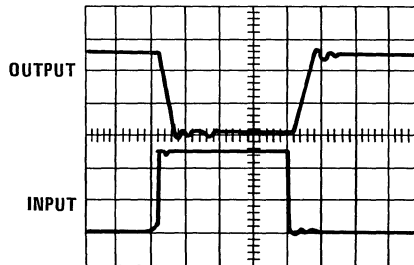


\* Values were determined experimentally for optimum speed and settling time. R1 and C1 should be optimized for each particular application to ensure best overall frequency response.

**INVERTING**

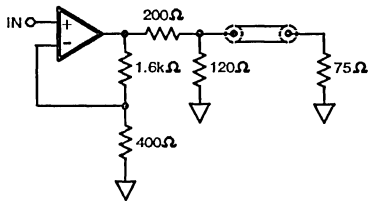


Vertical Scale: (Volts: 2V/Div.)  
Horizontal Scale: (50ns/Div.)

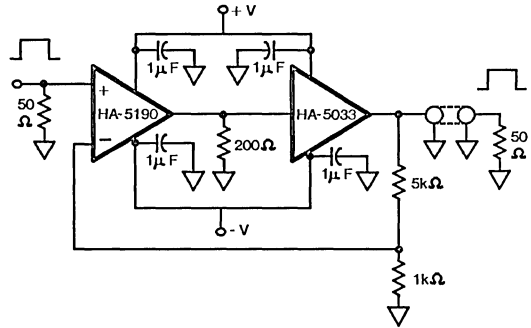


**Typical Applications** (Continued)

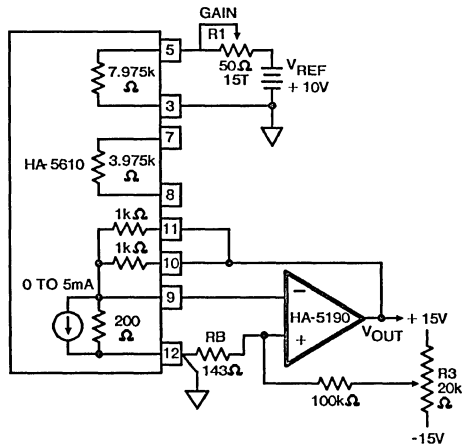
**VIDEO PULSE AMPLIFIER/75Ω COAXIAL DRIVER**



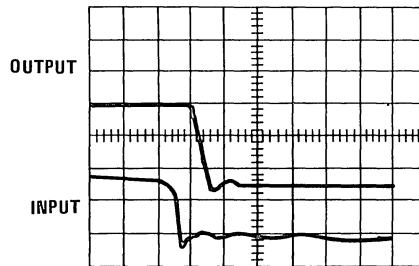
**VIDEO PULSE AMPLIFIER COAXIAL LINE DRIVER**



**FAST DAC OUTPUT BUFFER**



Vertical Scale: (Volts: 2V/Div.)  
 Horizontal Scale: (Time: 50ns/Div.)  
 B = V<sub>OUT</sub> C = Digital Input



\* Time delay between B and C represents total time delay for 0V to +5V full scale coded change.

**Die Characteristics**

|                                   |   |                 |
|-----------------------------------|---|-----------------|
| Transistor Count                  | 49  |                 |
| Die Dimensions                    | 0.087 x 0.052 x 0.019 inches<br>(2210 x 1320 x 483 μm)  |                 |
| Substrate Potential (Powered Up)* | V-  |                 |
| Process                           | High Frequency Bipolar Dielectric Isolation Passivation |                 |
| Passivation                       | Nitride   |                 |
| Thermal Constants (°C/W)          | θ <sub>ja</sub>   | θ <sub>jc</sub> |
| Ceramic DIP                       | 104   | 48              |
| Metal Can                         | 87  | 32              |

\*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

August 1991

### Features

- Gain Bandwidth Product ..... 100MHz
- Unity Gain Bandwidth ..... 35MHz
- High Slew Rate ..... 25V/ $\mu$ s
- Low Offset Voltage ..... 0.3mV
- High Open Loop Gain ..... 128dB
- Channel Separation @ 10kHz ..... 110dB
- Low Noise Voltage @ 1kHz ..... 3.4nV/ $\sqrt{\text{Hz}}$
- High Output Current ..... 56mA
- Low Supply Current per Amplifier ..... 8mA

### Applications

- Precision Test Systems
- Active Filtering
- Small Signal Video
- Accurate Signal Processing
- RF Signal Conditioning

### Description

The HA-5221/5222 are single and dual high performance dielectrically isolated, monolithic op amps, featuring precision DC characteristics while providing excellent AC characteristics. Designed for audio, video, and other demanding applications, noise (3.4nV/ $\sqrt{\text{Hz}}$  @ 1kHz), total harmonic distortion (<0.005%), and DC errors are kept to a minimum.

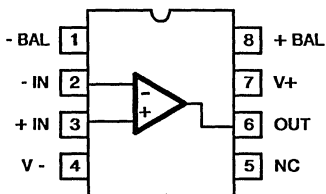
The precision performance is shown by low offset voltage (0.3mV), low bias currents (40nA), low offset currents (15nA), and high open loop gain (128dB). The combination of these excellent DC characteristics with the fast settling time (0.4 $\mu$ s) make the HA-5221/5222 ideally suited for precision signal conditioning.

The unique design of the HA-5221/5222 gives them outstanding AC characteristics not normally associated with precision op amps, high unity gain bandwidth (35MHz) and high slew rate (25V/ $\mu$ s). Other key specifications include high CMRR (95dB) and high PSRR (100dB). The combination of these specifications will allow the HA-5221/5222 to be used in RF signal conditioning as well as video amplifiers.

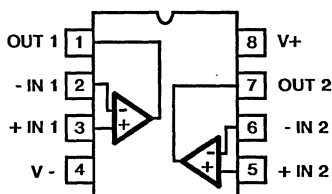
The performance of the HA-5221/5222-9 is guaranteed from -40°C to +85°C, while the HA-5221/5222-5 is guaranteed from 0°C to +75°C. The HA-5221 is available in 8 pin Ceramic Mini-DIP and 8 pin Metal Can (TO-99) and the HA-5222 is available in the 8 pin Ceramic Mini-DIP. For MIL-STD-883C compliant product and Ceramic LCC packaging, consult the HA-5221/5222/883C data sheet.

### Pinouts

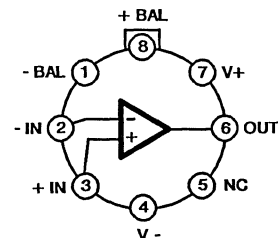
HA7-5221 (CERAMIC MINI-DIP)  
TOP VIEW



HA7-5222 (CERAMIC MINI-DIP)  
TOP VIEW



HA2-5221 (TO-99 METAL CAN)  
TOP VIEW



## Specifications HA-5221/22

### Absolute Maximum Ratings (Note 1)

|   |            |
|---|------------|
| Voltage Between V+ and V- Terminals .....   | 35V        |
| Differential Input Voltage (Note 14) .....  | 5V         |
| Output Current Short Circuit Duration ..... | Indefinite |

### Operating Temperature Ranges

|                                    |  |
|------------------------------------|--|
| HA-5221/5222-9 .....               | $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  |
| HA-5221/5222-5 .....               | $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$    |
| Storage Temperature Range .....    | $-65^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ |
| Maximum Junction Temperature ..... | +175°C   |

### Electrical Specifications V+ = 15V, V- = -15V, Unless Otherwise Specified

| PARAMETER                                | TEMP                                | HA-5221-9 & HA-5222-9 |            |            | HA-5221-5 & HA-5222-5 |            |            | UNITS                          |                              |
|--|-------------------------------------|-----------------------|------------|------------|-----------------------|------------|------------|--------------------------------|------------------------------|
|  |                                     | MIN                   | TYP        | MAX        | MIN                   | TYP        | MAX        |                                |                              |
| <b>INPUT CHARACTERISTICS</b>             |                                     |                       |            |            |                       |            |            |                                |                              |
| Input Offset Voltage                     | +25°C                               | -                     | 0.30       | 0.75       | -                     | 0.30       | 0.75       | mV                             |                              |
|  | Full                                | -                     | 0.35       | 1.5        | -                     | 0.35       | 1.5        | mV                             |                              |
| Average Offset Voltage Drift             | Full                                | -                     | 0.5        | -          | -                     | 0.5        | -          | $\mu\text{V}/^{\circ}\text{C}$ |                              |
| Input Bias Current                       | +25°C                               | -                     | 40         | 80         | -                     | 40         | 100        | nA                             |                              |
|  | Full                                | -                     | 70         | 200        | -                     | 70         | 200        | nA                             |                              |
| Input Offset Current                     | +25°C                               | -                     | 15         | 50         | -                     | 15         | 100        | nA                             |                              |
|  | Full                                | -                     | 30         | 150        | -                     | 30         | 150        | nA                             |                              |
| Input Offset Voltage Match               | +25°C                               | -                     | 400        | 750        | -                     | 400        | 750        | $\mu\text{V}$                  |                              |
|  | Full                                | -                     | -          | 1500       | -                     | -          | 1500       | $\mu\text{V}$                  |                              |
| Common Mode Range                        | +25°C                               | $\pm 12$              | -          | -          | $\pm 12$              | -          | -          | V                              |                              |
| Differential Input Resistance            | +25°C                               | -                     | 70         | -          | -                     | 70         | -          | k $\Omega$                     |                              |
| Input Noise Voltage                      | $f_o = 0.1\text{Hz to }10\text{Hz}$ | -                     | 0.25       | -          | -                     | 0.25       | -          | $\mu\text{Vp-p}$               |                              |
| Input Noise Voltage Density (Note 2, 15) | $f_o = 10\text{Hz}$                 | +25°C                 | -          | 6.2        | 10                    | -          | 6.2        | 10                             | $\text{nV}/\sqrt{\text{Hz}}$ |
|  | $f_o = 100\text{Hz}$                | +25°C                 | -          | 3.6        | 6                     | -          | 3.6        | 6                              | $\text{nV}/\sqrt{\text{Hz}}$ |
|  | $f_o = 1000\text{Hz}$               | +25°C                 | -          | 3.4        | 4.0                   | -          | 3.4        | 4.0                            | $\text{nV}/\sqrt{\text{Hz}}$ |
| Input Noise Current Density (Note 2, 15) | $f_o = 10\text{Hz}$                 | +25°C                 | -          | 4.7        | 8.0                   | -          | 4.7        | 8.0                            | $\text{pA}/\sqrt{\text{Hz}}$ |
|  | $f_o = 100\text{Hz}$                | +25°C                 | -          | 1.8        | 2.8                   | -          | 1.8        | 2.8                            | $\text{pA}/\sqrt{\text{Hz}}$ |
|  | $f_o = 1000\text{Hz}$               | +25°C                 | -          | 0.97       | 1.8                   | -          | 0.97       | 1.8                            | $\text{pA}/\sqrt{\text{Hz}}$ |
| THD+N (Note 3)                           | +25°C                               | -                     | <0.005     | -          | -                     | <0.005     | -          | %                              |                              |
| <b>TRANSFER CHARACTERISTICS</b>          |                                     |                       |            |            |                       |            |            |                                |                              |
| Large Signal Voltage Gain (Note 4)       | +25°C                               | 106                   | 128        | -          | 106                   | 128        | -          | dB                             |                              |
|  | Full                                | 100                   | 120        | -          | 100                   | 120        | -          | dB                             |                              |
| Common Mode Rejection Ratio (Note 5)     | Full                                | 86                    | 95         | -          | 86                    | 95         | -          | dB                             |                              |
| Unity Gain Bandwidth (-3dB)              | +25°C                               | -                     | 35         | -          | -                     | 35         | -          | MHz                            |                              |
| Gain Bandwidth Product (1kHz to 400kHz)  | +25°C                               | -                     | 100        | -          | -                     | 100        | -          | MHz                            |                              |
| Minimum Stable Gain                      | Full                                | 1                     | -          | -          | 1                     | -          | -          | V/V                            |                              |
| <b>OUTPUT CHARACTERISTICS</b>            |                                     |                       |            |            |                       |            |            |                                |                              |
| Output Voltage Swing                     | $R_L = 333\Omega$                   | Full                  | $\pm 10$   | -          | -                     | $\pm 10$   | -          | V                              |                              |
|  | $R_L = 1\text{K}$                   | +25°C                 | $\pm 12$   | $\pm 12.5$ | -                     | $\pm 12$   | $\pm 12.5$ | V                              |                              |
|  | $R_L = 1\text{K}$                   | Full                  | $\pm 11.5$ | $\pm 12.1$ | -                     | $\pm 11.5$ | $\pm 12.1$ | V                              |                              |
| Output Current (Note 6)                  | Full                                | $\pm 30$              | $\pm 56$   | -          | $\pm 30$              | $\pm 56$   | -          | mA                             |                              |
| Output Resistance                        | +25°C                               | -                     | 10         | -          | -                     | 10         | -          | $\Omega$                       |                              |
| Full Power Bandwidth (Note 7)            | +25°C                               | 238                   | 398        | -          | 238                   | 398        | -          | kHz                            |                              |
| Channel Separation (Note 8)              | +25°C                               | -                     | 110        | -          | -                     | 110        | -          | dB                             |                              |
| <b>TRANSIENT RESPONSE (Note 13)</b>      |                                     |                       |            |            |                       |            |            |                                |                              |
| Slew Rate (Note 9, 15)                   | Full                                | 15                    | 25         | -          | 15                    | 25         | -          | V/ $\mu\text{s}$               |                              |
| Rise Time (Note 10, 15)                  | Full                                | -                     | 13         | 20         | -                     | 13         | 20         | ns                             |                              |
| Overshoot (Note 10, 15)                  | Full                                | -                     | 28         | 50         | -                     | 28         | 50         | %                              |                              |
| Settling Time (Note 11)                  | 0.1%                                | +25°C                 | -          | 0.4        | -                     | 0.4        | -          | $\mu\text{s}$                  |                              |
|  | 0.01%                               | +25°C                 | -          | 1.5        | -                     | 1.5        | -          | $\mu\text{s}$                  |                              |
| <b>POWER SUPPLY</b>                      |                                     |                       |            |            |                       |            |            |                                |                              |
| PSRR (Note 12)                           | Full                                | 86                    | 100        | -          | 86                    | 100        | -          | dB                             |                              |
| Supply Current                           | Full                                | -                     | 8          | 11         | -                     | 8          | 11         | mA/Op Amp                      |                              |

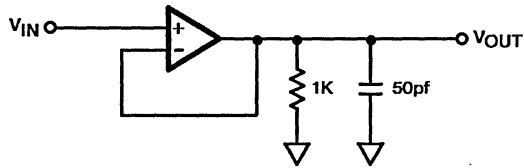
#### NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Refer to typical performance curve in data sheet.
3.  $A_{VCL} = 10$ ,  $f_o = 1\text{kHz}$ ,  $V_O = 5V_{rms}$ ,  $R_L = 600\Omega$ , 10Hz to 100kHz, Minimum resolution of test equipment is 0.005%.
4.  $V_{OUT} = 0$  to  $\pm 10V$ ,  $R_L = 1\text{K}$ ,  $C_L = 50\text{pF}$ .
5.  $V_{CM} = \pm 10V$ .
6.  $V_{OUT} = \pm 10V$ .
7. Full Power Bandwidth is calculated by:  $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}} = 10V$ .
8. HA-5222 only,  $f_o = 10\text{kHz}$ ,  $R_L = 1\text{K}$ ,  $C_L = 50\text{pF}$ .
9.  $V_{OUT} = \pm 2.5V$ ,  $R_L = 1\text{K}$ ,  $C_L = 50\text{pF}$ .
10.  $V_{OUT} = \pm 100\text{mV}$ ,  $R_L = 1\text{K}$ ,  $C_L = 50\text{pF}$ .
11. Settling time is specified for a 10V step and  $A_V = -1$ .
12.  $V_S = \pm 10V$  to  $\pm 20V$ .
13. See Test Circuits.
14. Input is protected by back-to-back zener diodes. See applications section.
15. Guaranteed by characterization.



Test Circuits

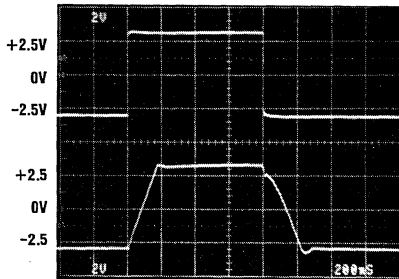
TRANSIENT RESPONSE TEST CIRCUIT



LARGE SIGNAL RESPONSE

$$V_{OUT} = \pm 2.5V$$

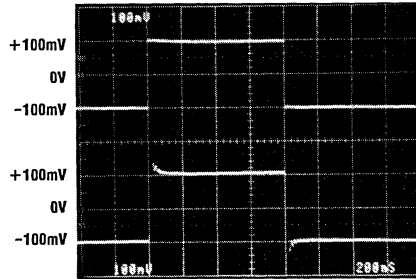
Vertical Scale: 2V/div Horizontal Scale: 200ns/div



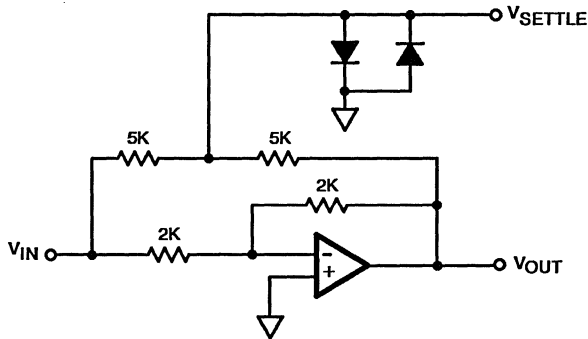
SMALL SIGNAL RESPONSE

$$V_{OUT} = \pm 100mV$$

Vertical Scale: 100mV/div Horizontal Scale: 200ns/div



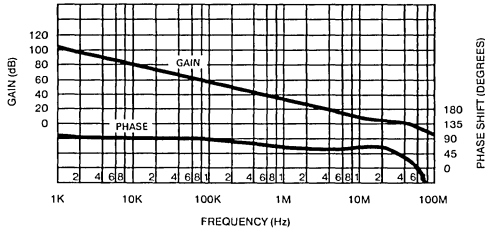
SETTLING TIME TEST CIRCUIT



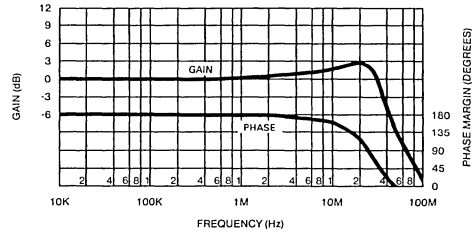
- $A_v = -1$
- Feedback and summing resistors must be matched (0.1%).
- HP5082-2810 clipping diodes recommended.
- Tektronix P6201 FET probe used at settling point.

Typical Performance Curves  $V_S = \pm 15V, T_A = 25^\circ C$

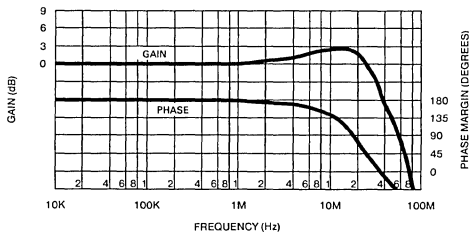
OPEN LOOP GAIN AND PHASE vs FREQUENCY  
 $R_L = 1K, C_L = 50pF$



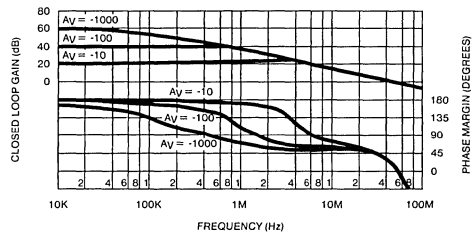
CLOSED LOOP GAIN vs FREQUENCY  
 $A_V = +1, R_L = 1K, C_L = 50pF$



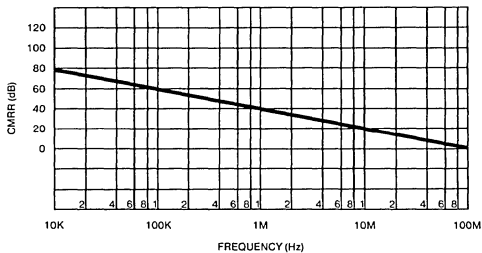
CLOSED LOOP GAIN vs FREQUENCY  
 $A_V = -1, R_L = 1K, C_L = 50pF$



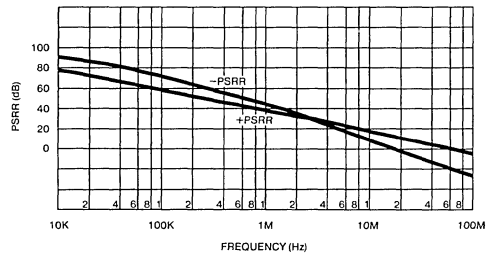
VARIOUS CLOSED LOOP GAINS vs FREQUENCY  
 $R_L = 1K, C_L = 50pF$



CMRR vs FREQUENCY  
 $A_V = +1, R_L = 1K$



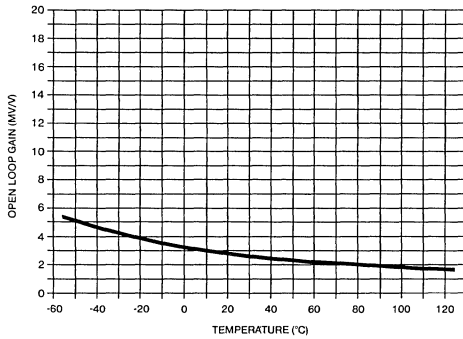
PSRR vs FREQUENCY  
 $A_V = +1, R_L = 1K$



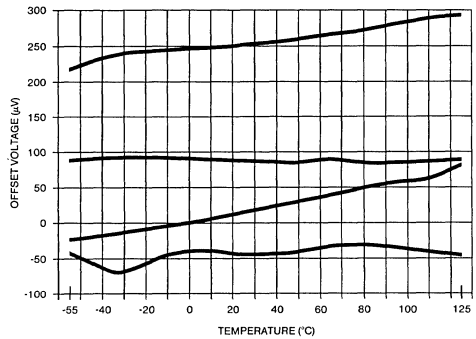
# HA-5221/22

## Typical Performance Curves $V_S = \pm 15V, T_A = 25^\circ C$

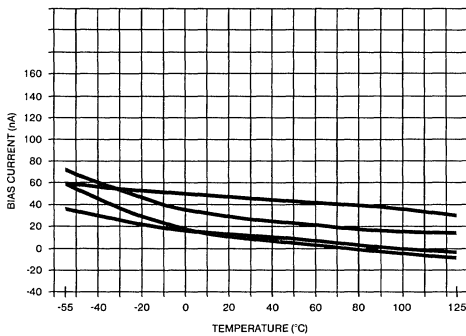
**OPEN LOOP GAIN vs TEMPERATURE**  
 $R_L = 1K$



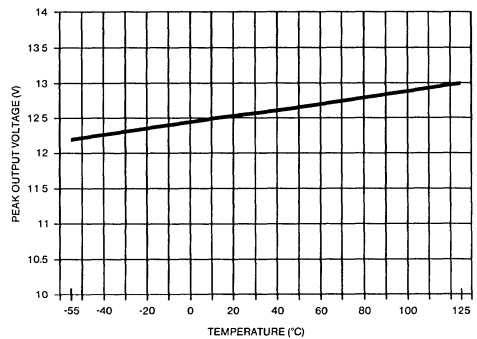
**OFFSET VOLTAGE vs TEMPERATURE**  
4 Representative Units



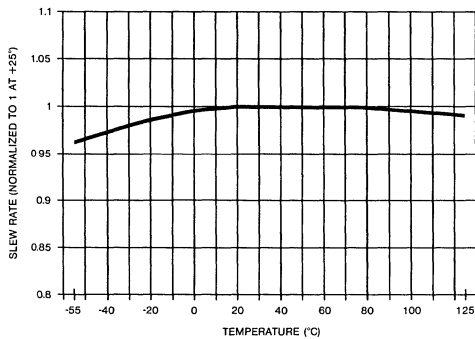
**BIAS CURRENT vs TEMPERATURE**  
4 Representative Units



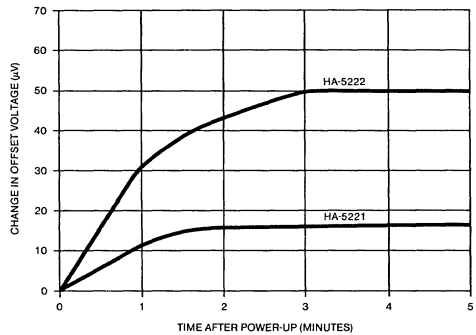
**OUTPUT VOLTAGE SWING vs TEMPERATURE**  
 $R_L = 600\Omega$



**SLEW RATE vs TEMPERATURE**  
 $A_V = +1, R_L = 1K, C_L = 50pF$



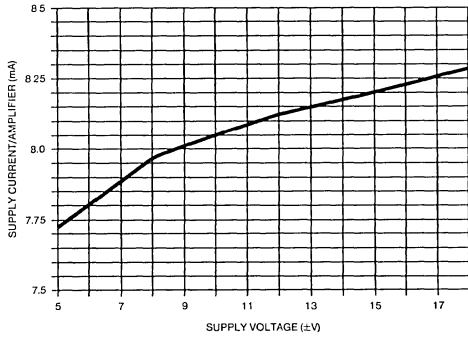
**OFFSET VOLTAGE WARM-UP DRIFT**  
Ceramic DIP Packages



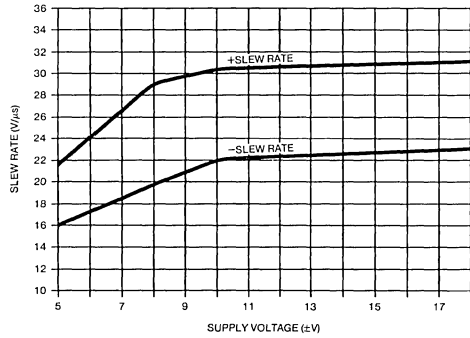
# HA-5221/22

## Typical Performance Curves $V_S = \pm 15V, T_A = 25^\circ C$

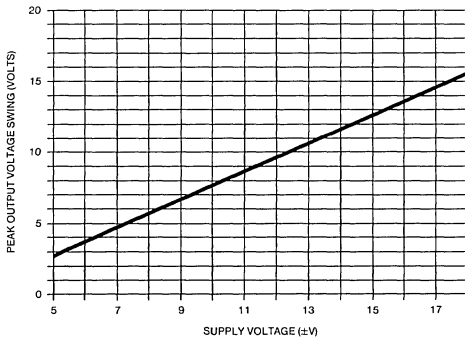
**SUPPLY CURRENT vs SUPPLY VOLTAGE**



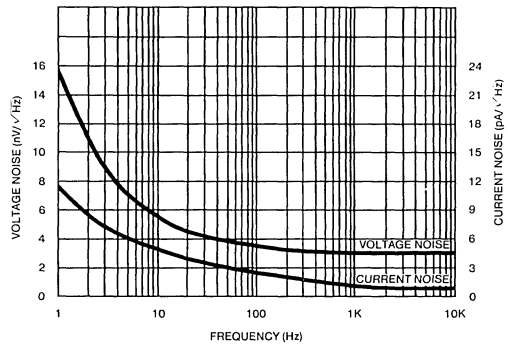
**SLEW RATE vs SUPPLY VOLTAGE**  
 $A_V = +1, R_L = 2K, C_L = 50pF$



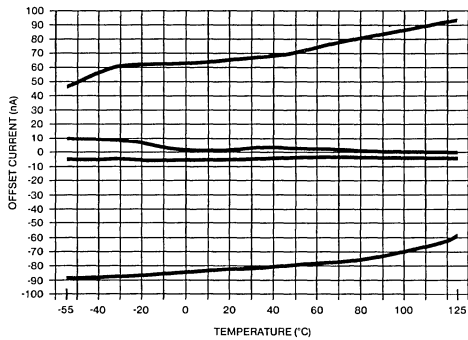
**OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE**  
 $R_L = 600\Omega$



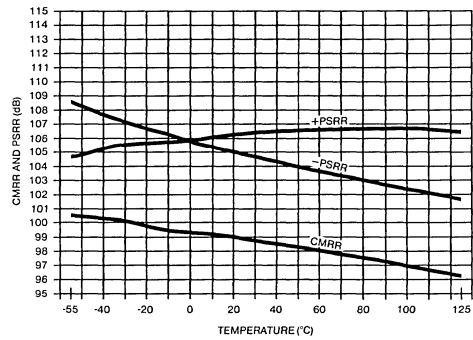
**NOISE CHARACTERISTICS**



**OFFSET CURRENT vs TEMPERATURE**  
 4 Representative Units



**CMRR AND PSRR vs TEMPERATURE**

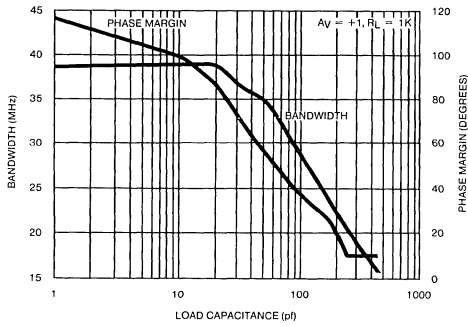


3  
OPERATIONAL AMPLIFIERS

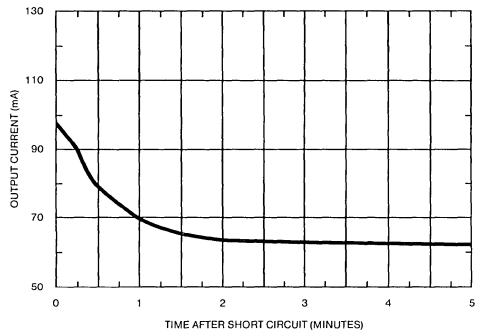
# HA-5221/22

Typical Performance Curves  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$

**BANDWIDTH AND PHASE MARGIN vs LOAD CAPACITANCE**

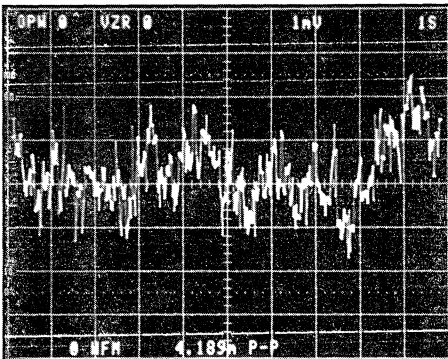


**SHORT CIRCUIT OUTPUT CURRENT vs TIME**



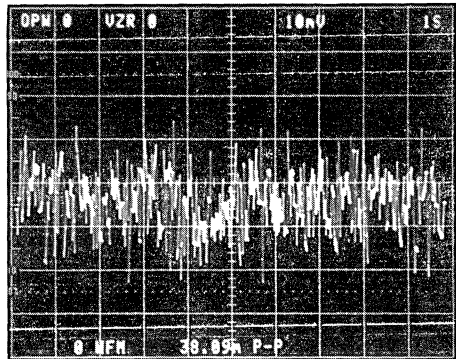
**0.1Hz TO 10Hz NOISE**

Vertical Scale: 1mV/div Horizontal Scale: 1 S/div  
 $A_V = +25,000$  (0.168 $\mu$ Vp-p RTI)



**0.1Hz TO 1Hz 1MHz**

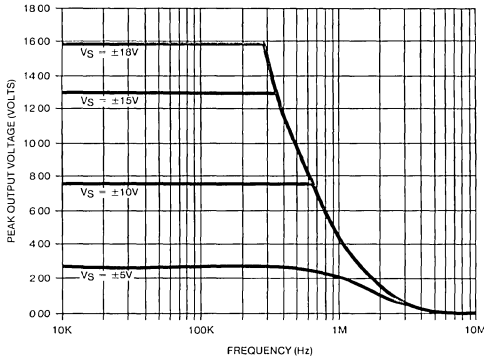
Vertical Scale: 10mV/div Horizontal Scale: 1 S/div  
 $A_V = +25,000$  (1.5 $\mu$ Vp-p RTI)



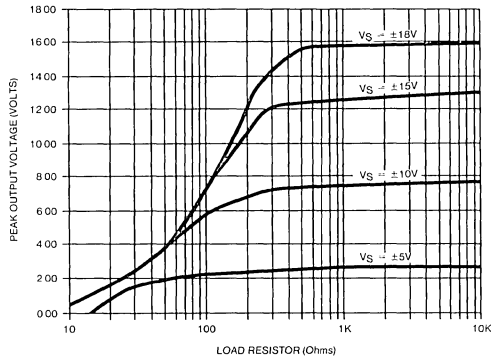
# HA-5221/22

## Typical Performance Curves $V_S = \pm 15V, T_A = 25^\circ C$

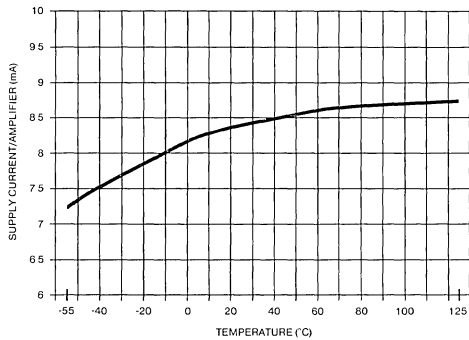
**OUTPUT VOLTAGE SWING vs FREQUENCY**  
 $A_V = +1, R_L = 1K, C_L = 15\mu F, THD \leq 0.01\%$



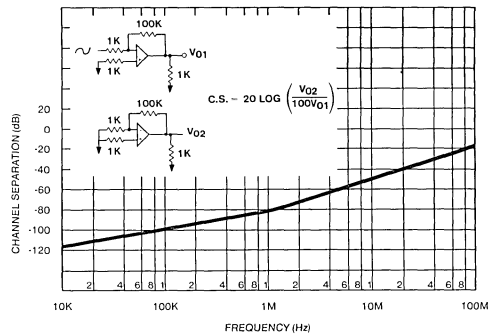
**OUTPUT VOLTAGE SWING vs LOAD RESISTANCE**  
 $A_V = +1, THD \leq 0.01\%, f = 1kHz$



**SUPPLY CURRENT/AMPLIFIER vs TEMPERATURE**



**CHANNEL SEPARATION vs FREQUENCY**  
 (HA-5222 only)



  
**OPERATIONAL AMPLIFIERS**

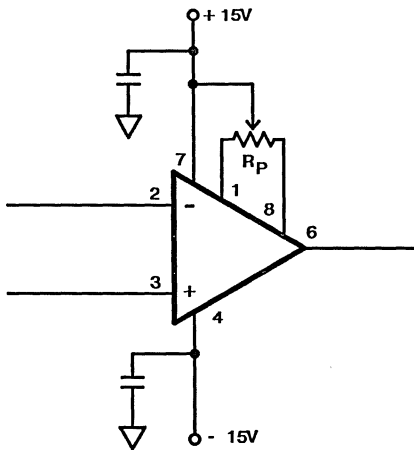
**Applications Information**

**Operation at Various Supply Voltages**

The HA-5221/5222 operates over a wide range of supply voltages with little variation in performance. The supplies may be varied from  $\pm 5$  volts to  $\pm 15$  volts. See typical performance curves for variations in supply current, slew rate and output voltage swing.

**Offset Adjustment**

The following diagram shows the offset voltage adjustment configuration for the HA-5221. By moving the potentiometer wiper towards pin 8 (+BAL), the op amp's output voltage will increase; towards pin 1 (-BAL) decreases the output voltage.



A 20k $\Omega$  trim pot will allow an offset voltage adjustment of about 10mV.

**Capacitive Loading Considerations**

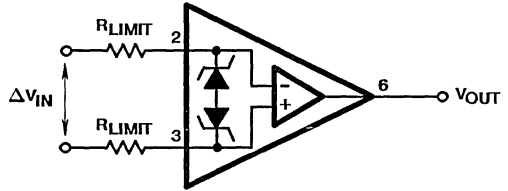
When driving capacitive loads  $>80$ pF, a small resistor, 50 to 100 $\Omega$ , should be connected in series with the output and inside the feedback loop.

**Saturation Recovery**

When an op amp is over driven, output devices can saturate and sometimes take a long time to recover. By clamping the input, output saturation can be avoided. If output saturation can not be avoided, the maximum recovery time when overdriven into the positive rail is 10.6 $\mu$ s. When driven into the negative rail the maximum recovery time is 3.8 $\mu$ s.

**Input Protection**

The HA-5221/5222 has built in back-to-back protection diodes which limit the maximum allowable differential input voltage to approximately 5 volts. If the HA-5221/5222 will be used in circuits where the maximum differential voltage may be exceeded, then current limiting resistors must be used. The input current should be limited to a maximum of 10mA.



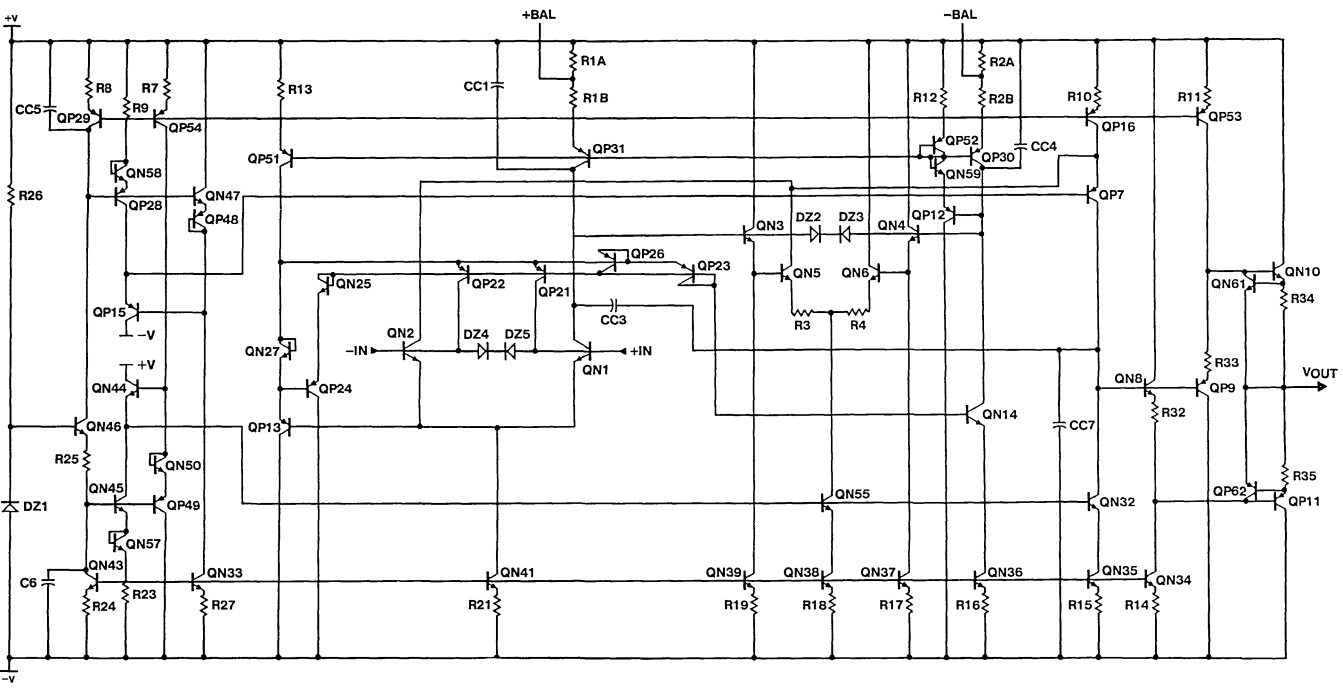
**PC Board Layout Guidelines**

When designing with the HA-5221 or the HA-5222, good high frequency (RF) techniques should be used when building a p.c. board. Use of ground plane is recommended. Power supply decoupling is very important. A 0.01 $\mu$ f to 0.1 $\mu$ f high quality ceramic capacitor at each power supply pin with a 2.2 $\mu$ f to 10 $\mu$ f tantalum close by will provide excellent decoupling. Chip capacitors produce the best results due to ease of placement next to the op amp and basically no lead inductance. If leaded capacitors are used, the leads should be kept as short as possible to minimize lead inductance.

**Die Characteristics**

|                                     |                             |                             |
|-------------------------------------|-----------------------------|-----------------------------|
| Transistor Count                    |                             |                             |
| HA-5221 .....                       |                             | 64                          |
| HA-5222 .....                       |                             | 128                         |
| Die Dimensions                      |                             |                             |
| HA-5221 .....                       | 94 x 72 x 19mils            |                             |
|                                     | (2400 x 1840 x 480 $\mu$ m) |                             |
| HA-5222 .....                       | 185 x 78 x 19mils           |                             |
|                                     | (4690 x 1980 x 480 $\mu$ m) |                             |
| Substrate Potential* .....          | V-                          |                             |
| Process .....                       | High Frequency, Bipolar, DI |                             |
| Passivation .....                   | Silox                       |                             |
| Thermal Constants ( $^{\circ}$ C/W) |                             | $\theta_{ja}$ $\theta_{jc}$ |
| HA2-5221 .....                      | 163                         | 36                          |
| HA7-5221 .....                      | 152                         | 76                          |
| HA7-5222 .....                      | 134                         | 59                          |

\*The substrate may be left floating (Insulating Die Mount) or it may be on a conductor at V- potential.



3-477



## PRELIMINARY

August 1991

### Features

- Low Offset Voltage ..... 300 $\mu$ V (Max)
- Low Offset Drift ..... 2 $\mu$ V/ $^{\circ}$ C
- Low Supply Current ..... <1mA/Amp
- High Gain, CMRR and PSRR

### Applications

- Audio Amplifiers
- Low Impedance Sensors
- Universal Active Filters
- Process Control Equipment

### Description

The HA-5232 and HA-5234 are dual and quad precision bipolar-input op amps. They are intended for use in multi-channel data acquisition systems where moderate-to-high level of accuracy is required. This relatively high level of accuracy is maintained across temperature with an Average Offset Drift of 2 $\mu$ V/ $^{\circ}$ C for the high grade parts.

The HA-5232 and HA-5234 were designed to offer a solution between the lower performance parts like the HA-4741 or CA324 and the higher priced precision multiple op amps like the OP-400. These parts will allow the designer to get a relatively high level of precision in his transducer preamp without having to worry about offset trimming.

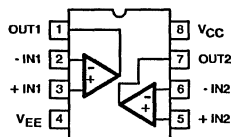
Large volume applications will be in process control and environment monitoring where many low impedance sensors such as thermocouples, thermistors, strain gauges, and pressure transducers are used to assess the state of the system. Other systems with similar requirements include mainframe computers, aircraft, and semiconductor fab and test equipment.

The HA-5232 and HA-5234 are available in commercial and industrial temperature ranges, and a choice of packages. See the "Ordering Information" section below for more information.

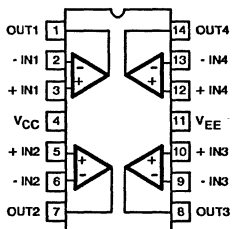
For military grade product, refer to the HA-5232/883 and HA-5234/883 data sheet.

### Pinouts

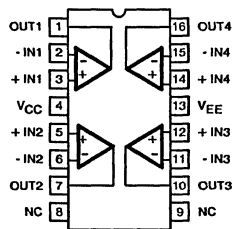
HA9P5232 (8 PIN SOIC)  
HA3-5232 (8 PIN PLASTIC DIP)  
TOP VIEW



HA3-5234 (14 PIN PLASTIC DIP)  
TOP VIEW



HA9P5234 (16 PIN SOIC)  
TOP VIEW



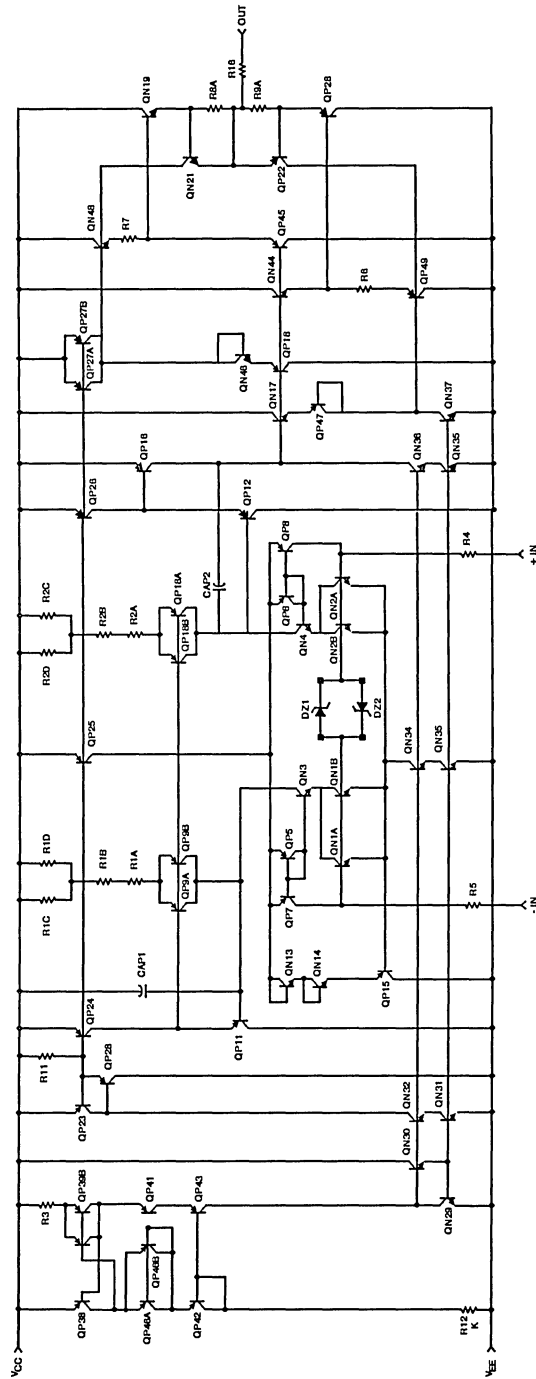
The functional pinouts will comply to the JEDEC standards for dual and quad op amps as shown above.

### Ordering Information

| PART NUMBER    | TEMPERATURE RANGE                    | PACKAGE            |
|----------------|--------------------------------------|--------------------|
| HA3-5232-5/A-5 | 0 $^{\circ}$ C to +70 $^{\circ}$ C   | 8 Pin Plastic DIP  |
| HA9P5232-5/A-5 | 0 $^{\circ}$ C to +70 $^{\circ}$ C   | 8 Pin SOIC         |
| HA3-5234-5/A-5 | 0 $^{\circ}$ C to +70 $^{\circ}$ C   | 14 Pin Plastic DIP |
| HA9P5234-5/A-5 | 0 $^{\circ}$ C to +70 $^{\circ}$ C   | 16 Pin SOIC        |
| HA3-5232-9/A-9 | -40 $^{\circ}$ C to +85 $^{\circ}$ C | 8 Pin Plastic DIP  |
| HA9P5232-9/A-9 | -40 $^{\circ}$ C to +85 $^{\circ}$ C | 8 Pin SOIC         |
| HA3-5234-9/A-9 | -40 $^{\circ}$ C to +85 $^{\circ}$ C | 14 Pin Plastic DIP |
| HA9P5234-9/A-9 | -40 $^{\circ}$ C to +85 $^{\circ}$ C | 16 Pin SOIC        |

HA-5232 HA-5234

Schematic



## Specifications HA-5232 HA-5234

### Absolute Maximum Ratings

Voltage Between V+ and V- ..... 36V  
 Common Mode Voltage .....  $V_{SUPPLY}$   
 Differential Input Voltage .....  $V_{SUPPLY}$   
 Output Current Short Circuit ..... Protected

### Operating Temperature Ranges

HA-5232-5, HA-5234-5 .....  $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$   
 HA-5232-9, HA-5234-9 .....  $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$   
 Storage Temperature Range .....  $-65^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$   
 Maximum Junction Temperature .....  $+175^{\circ}\text{C}$

**Electrical Specifications**  $V_{SUPPLY} = \pm 15\text{V}$ ,  $R_L = 100\text{k}\Omega$ ,  $C_L = 20\text{pF}$  Unless Otherwise Specified

| PARAMETER                        | TEMP                | HA-5232A-5 or A-9<br>HA-5234A-5 or A-9 |      |     | HA-5232-5 or -9<br>HA-5234-5 or -9 |      |     | UNITS                          |    |
|----------------------------------|---------------------|--|------|-----|------------------------------------|------|-----|--------------------------------|----|
|                                  |                     | MIN                                    | TYP  | MAX | MIN                                | TYP  | MAX |                                |    |
| Offset Voltage                   | +25°C               | -                                      | 100  | 200 | -                                  | 100  | 500 | $\mu\text{V}$                  |    |
|                                  | Full                | -                                      | -    | 300 | -                                  | -    | 725 | $\mu\text{V}$                  |    |
| Average Offset Drift             | Full                | -                                      | -    | 2   | -                                  | -    | 5   | $\mu\text{V}/^{\circ}\text{C}$ |    |
| Input Bias Current               | +25°C               | -                                      | -    | 5   | -                                  | -    | 10  | nA                             |    |
|                                  | Full                | -                                      | -    | 10  | -                                  | -    | 15  | nA                             |    |
| Input Offset Current             | +25°C               | -                                      | -    | 3.5 | -                                  | -    | 10  | nA                             |    |
|                                  | Full                | -                                      | -    | 6   | -                                  | -    | 15  | nA                             |    |
| Common Mode Range                | Full                | 12                                     | -    | -   | 12                                 | -    | -   | V                              |    |
| CMRR (Note 1)                    | +25°C               | 110                                    | -    | -   | 100                                | -    | -   | dB                             |    |
|                                  | Full                | 105                                    | -    | -   | 100                                | -    | -   | dB                             |    |
| Input Capacitance                | +25°C               | -                                      | 3    | -   | -                                  | 3    | -   | pF                             |    |
| Input Noise Voltage 0.1Hz - 10Hz | +25°C               | -                                      | 0.5  | -   | -                                  | 0.5  | -   | $\mu\text{V}_{p-p}$            |    |
|                                  | $f_o = 1\text{kHz}$ | -                                      | 11   | -   | -                                  | 11   | -   | $\text{nV}/\sqrt{\text{Hz}}$   |    |
| Input Noise Current 0.1Hz - 10Hz | +25°C               | -                                      | 15   | -   | -                                  | 15   | -   | $\text{pA}_{p-p}$              |    |
|                                  | $f_o = 1\text{kHz}$ | -                                      | 0.4  | -   | -                                  | 0.4  | -   | $\text{pA}/\sqrt{\text{Hz}}$   |    |
| Large Signal Gain (Note 2)       | +25°C               | 1000                                   | -    | -   | 250                                | -    | -   | KV/V                           |    |
|                                  | Full                | 1000                                   | -    | -   | 250                                | -    | -   | KV/V                           |    |
| Unity Gain Bandwidth             | +25°C               | -                                      | 0.5  | -   | -                                  | 0.5  | -   | MHz                            |    |
| Minimum Stable Gain              | Full                | 1                                      | -    | -   | 1                                  | -    | -   | V/V                            |    |
| Output Swing (Note 2)            | +25°C               | 12                                     | -    | -   | 12                                 | -    | -   | V                              |    |
|                                  | Full                | 12                                     | -    | -   | 12                                 | -    | -   | V                              |    |
| Short Circuit Current            | Full                | -                                      | -    | 50  | -                                  | -    | 50  | mA                             |    |
| Slew Rate (Note 3)               | +25°C               | -                                      | 0.15 | -   | -                                  | 0.15 | -   | V/ $\mu\text{s}$               |    |
| PSRR (Note 4)                    | +25°C               | 105                                    | -    | -   | 100                                | -    | -   | dB                             |    |
|                                  | Full                | 100                                    | -    | -   | 100                                | -    | -   | dB                             |    |
| $I_{CC}$                         | HA-5232             | +25°C                                  | -    | -   | 1.45                               | -    | -   | 1.45                           | mA |
|                                  |                     | Full                                   | -    | -   | 1.55                               | -    | -   | 1.55                           | mA |
|                                  | HA-5234             | +25°C                                  | -    | -   | 2.9                                | -    | -   | 2.9                            | mA |
|                                  |                     | Full                                   | -    | -   | 3.1                                | -    | -   | 3.1                            | mA |

**NOTES:**

1.  $V_{CM} = \pm 10\text{V}$
2.  $R_L = 2\text{K}$
3.  $R_L = 2\text{K}$ ,  $C_L = 100\text{pF}$ ,  $V_{OUT} = \pm 10\text{V}$ ,  $A_V = +1$
4.  $|V_G| = 3\text{V to } 18\text{V}$

**PRELIMINARY**

**Low Power Precision BiMOS  
Operational Amplifiers**

August 1991

**Features**

- Low Power: HA-7712 ..... 150 $\mu$ A  
                  HA-7713 ..... 15 $\mu$ A
- Low Offset Voltage: A Grade ..... 250 $\mu$ V  
                                  B Grade ..... 500 $\mu$ V
- Wide Operating Voltage Range..... 4V to 16V
- Low Input Bias Current
- Common Mode Range Includes the Negative Rail
- Output Voltage Swing to  $\pm$ 100mV of Supplies
- High Input Impedance ..... 1012
- High Gain, CMRR and PSRR

**Applications**

- Portable Instruments
- Telephone Headsets
- Hearing Aid/Microphone Amplifiers
- Medical Instrumentation
- Meter Amplifiers
- High Performance Buffers
- Hand-Held Instrumentation

**Description**

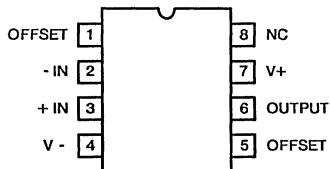
The HA-7712/13 are monolithic single operational amplifiers which use Harris' new BiMOS process. They offer precision performance and low power consumption, with quiescent currents of 150 $\mu$ A for the HA-7712 and 15 $\mu$ A for the HA-7713. These op amps have an input offset voltage of less than 250 $\mu$ V, an input offset current below 10pA, and an open-loop gain of 115dB.

The HA-7712/13 will operate at supply voltages ranging from  $\pm$ 2V to  $\pm$ 8V. The wide common mode voltage range, which includes the negative supply, allows for amplification of signals including ground in a single supply application.

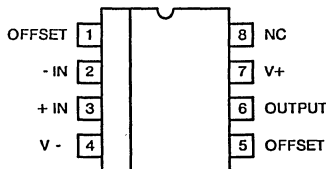
The HA-7712/13 are available in commercial and industrial temperature ranges. The high performance and low power consumption make the HA-7712/13 ideal for industrial applications.

**Pinouts**

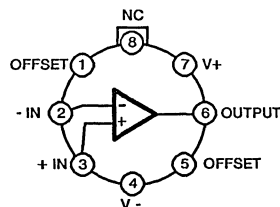
OUTLINE DRAWING  
8-PIN MINIDIP  
TOP VIEW



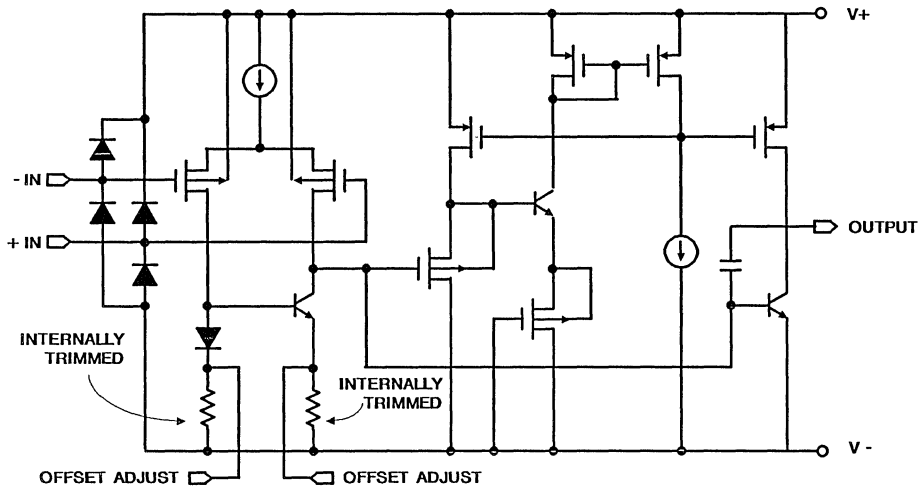
OUTLINE DRAWING  
8-PIN SOIC  
TOP VIEW



OUTLINE DRAWING  
8-PIN TO-99  
TOP VIEW



**3**  
OPERATIONAL  
AMPLIFIERS

**Block Diagram****Detailed Description****Overview**

The HA-7712/13 BiMOS op amps are pin compatible with the ICL-7611 CMOS op amp, however pin 8 on the HA-7712/13 is not connected (pin 8 on the ICL-7611 is the I<sub>Q</sub> set pin, which is not required for the HA-7712/13). The HA-7712 has a quiescent current of 150μA, and the HA-7713 has a quiescent current of 15μA.

These op amps operate with supply voltages of ±2V to ±8V. They have very low offset voltages: 250μV for the A grade and 500μV for the B grade. The HA-7712/13 op amps offer high open-loop gain, CMRR, PSRR, slew rate and unity-gain bandwidth. They also have excellent noise performance due to p-channel inputs and NPN loads. The common mode voltage range of the HA-7712/13 op amps include the negative supply rail which allows for amplification of signals including ground in a single supply application.

**Static Protection**

All devices are static protected by the use of input protection diodes. However, strong static fields should be avoided, as it is possible for the strong fields to cause degraded diode junction characteristics, which may result in increased input leakage currents.

**Latchup Avoidance**

Junction-isolated BiMOS circuits employ configurations which produce a parasitic 4-layer (p-n-p-n) structure. The 4-layer structure has characteristics similar to an SCR and under certain circumstances may be triggered into a low impedance state resulting in excessive supply current. To

avoid this condition, no voltage greater than 0.3V beyond the supply rails may be applied to any pin. In general, the op amp supplies must be established simultaneously with, or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to 2mA to prevent latchup.

**Output Stage and Load Driving Considerations**

The HA-7712/13 op amps consist of three gain stages: input stage, intermediate stage and output stage. The quiescent current flows primarily in the intermediate and output stages. The intermediate stage is for level shifting and the output stage consists of a common source p-channel device for sourcing current and a common emitter NPN for sinking current. The outputs swing to almost the supply rails for output loads of 1MΩ for the HA-7713 and 100kΩ for the HA-7712. The gain of the op amp is directly proportional to the load impedance.

**Input Offset Nulling**

Offset nulling may be achieved by connecting a 20kΩ pot between the OFFSET terminals with the wiper connected to V-. If offset nulling is not required, the OFFSET terminals should be left open.

**Frequency Compensation**

The HA-7712/13 are internally compensated and are stable for closed loop gains as low as unity with capacitive loads up to 100pF.

## Specifications HA-7712 HA-7713

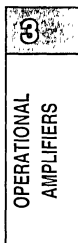
### Absolute Maximum Ratings

|   |   |
|---|---|
| Total Supply Voltage (V+ to V-) ..... 18V<br>Input Voltage ..... (V+ +0.3V) to (V- -0.3V)<br>Differential Input Voltage ..... ±[(V+ +0.3V) - (V- -0.3V)]<br>Duration of Output Short Circuit ..... Indefinite<br>Current Into Any Pin ..... 10mA<br>Continuous Total Power Dissipation (T <sub>A</sub> = +25°C)<br>Plastic Package ..... 250mW<br>SOIC Package ..... 200mW<br>TO-99 ..... 250mW | Storage Temperature Range ..... -65°C to +150°C<br>Lead Temperature (Soldering, 10 sec) ..... +300°C<br>Operating Temperature Range<br>HA-7712/13-5 (Commercial) ..... 0°C to +70°C<br>HA-7712/13-9 (Industrial) ..... -40°C to +85°C |
|---|---|

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

### Electrical Specifications Test Conditions: V+ = +5V, V- = -5V, T<sub>A</sub> = +25°C Unless Otherwise Specified.

| PARAMETER   | SYMBOL               | TEST CONDITIONS  | HA-7712/13A |                  |     | HA-7712/13B |                  |     | UNITS    |
|---|----------------------|--|-------------|------------------|-----|-------------|------------------|-----|----------|
|   |                      |  | MIN         | TYP              | MAX | MIN         | TYP              | MAX |          |
| Input Offset Voltage  | V <sub>OS</sub>      | HA-7712 R <sub>L</sub> = 100kΩ<br>HA-7713 R <sub>L</sub> = 1MΩ |             |                  |     |             |                  |     |          |
|   |                      | T <sub>A</sub> = +25°C   | -           | -                | 250 | -           | -                | 500 | μV       |
|   |                      | 0°C ≤ T <sub>A</sub> ≤ +70°C                                   | -           | -                | 350 | -           | -                | 650 | μV       |
|   |                      | -40°C ≤ T <sub>A</sub> ≤ +85°C                                 | -           | -                | 400 | -           | -                | 700 | μV       |
| Average Temperature Coefficient of Input Offset Voltage                   | ΔV <sub>OS</sub> /ΔT | HA-7712 R <sub>L</sub> = 100kΩ<br>HA-7713 R <sub>L</sub> = 1MΩ | -           | 2                | -   | -           | 2                | -   | μV/°C    |
| Change in Input Offset With Time (Note 3)                                 | ΔV <sub>OS</sub> /Δt | HA-7712 R <sub>L</sub> = 100kΩ<br>HA-7713 R <sub>L</sub> = 1MΩ | -           | 2                | -   | -           | 2                | -   | μV/month |
| Input Offset Current<br> I <sub>I(-)</sub> - I <sub>I(+)</sub>   (Note 1) | I <sub>OS</sub>      | T <sub>A</sub> = +25°C   | -           | -                | 10  | -           | -                | 10  | pA       |
|   |                      | 0°C ≤ T <sub>A</sub> ≤ +70°C                                   | -           | -                | 25  | -           | -                | 25  | pA       |
|   |                      | -40°C ≤ T <sub>A</sub> ≤ +85°C                                 | -           | -                | 40  | -           | -                | 40  | pA       |
| Input Bias Current<br> I <sub>I(+)</sub> , I <sub>I(-)</sub>   (Note 1)   | I <sub>BIAS</sub>    | T <sub>A</sub> = +25°C   | -           | -                | 20  | -           | -                | 20  | pA       |
|   |                      | 0°C ≤ T <sub>A</sub> ≤ +70°C                                   | -           | -                | 50  | -           | -                | 50  | pA       |
|   |                      | -40°C ≤ T <sub>A</sub> ≤ +85°C                                 | -           | -                | 80  | -           | -                | 80  | pA       |
| Output Voltage Swing  | V <sub>OUT</sub>     | HA-7712 R <sub>L</sub> = 100kΩ<br>HA-7713 R <sub>L</sub> = 1MΩ |             |                  |     |             |                  |     |          |
|   |                      | T <sub>A</sub> = +25°C   | ±4.95       | -                | -   | ±4.95       | -                | -   | V        |
|   |                      | T <sub>MIN</sub> ≤ T <sub>A</sub> ≤ T <sub>MAX</sub>           | ±4.9        | -                | -   | ±4.9        | -                | -   | V        |
| Input Resistance  | R <sub>IN</sub>      |  | -           | 10 <sup>12</sup> | -   | -           | 10 <sup>12</sup> | -   | Ω        |
| Large Signal Voltage Gain   | A <sub>VOL</sub>     | HA-7712 R <sub>L</sub> = 100kΩ<br>HA-7713 R <sub>L</sub> = 1MΩ |             |                  |     |             |                  |     |          |
|   |                      | T <sub>A</sub> = +25°C   | 108         | 115              | -   | 100         | 110              | -   | dB       |
|   |                      | 0°C ≤ T <sub>A</sub> ≤ +70°C                                   | 103         | -                | -   | 95          | -                | -   | dB       |
|   |                      | -40°C ≤ T <sub>A</sub> ≤ +85°C                                 | 98          | -                | -   | 90          | -                | -   | dB       |
| Unity Gain Bandwidth  | GBW                  | HA-7712 R <sub>L</sub> = 100kΩ                                 | -           | 1000             | -   | -           | 1000             | -   | kHz      |
|   |                      | HA-7713 R <sub>L</sub> = 1MΩ                                   | -           | 120              | -   | -           | 120              | -   | kHz      |



## Specifications HA-7712 HA-7713

**Electrical Specifications (Continued)** Test Conditions:  $V+ = +5V$ ,  $V- = -5V$ ,  $T_A = +25^\circ C$ , Unless Otherwise Specified.

| PARAMETER                             | SYMBOL   | TEST CONDITIONS  | HA-7712/13A |       |     | HA-7712/13B |       |     | UNITS          |
|---------------------------------------|----------|--|-------------|-------|-----|-------------|-------|-----|----------------|
|                                       |          |  | MIN         | TYP   | MAX | MIN         | TYP   | MAX |                |
| Common Mode Voltage Range             | CMVR     | HA-7712 $R_L = 100k\Omega$<br>HA-7713 $R_L = 1M\Omega$ | -5          | -     | 4   | -5          | -     | 4   | V              |
| Common Mode Rejection Ratio           | CMRR     | HA-7712 $R_L = 100k\Omega$                             | 90          | 105   | -   | 80          | 100   | -   | dB             |
|                                       |          | HA-7713 $R_L = 1M\Omega$                               | 90          | 105   | -   | 80          | 100   | -   | dB             |
| Power Supply Rejection Ratio          | PSRR     | HA-7712 $R_L = 100k\Omega$                             | 90          | 105   | -   | 80          | 100   | -   | dB             |
|                                       |          | HA-7713 $R_L = 1M\Omega$                               | 90          | 105   | -   | 80          | 100   | -   | dB             |
| Positive Short Circuit Output Current | +IOSC    | HA-7712  | -           | 25    | -   | -           | 25    | -   | mA             |
|                                       |          | HA-7713  | -           | 10    | -   | -           | 10    | -   | mA             |
| Negative Short Circuit Output Current | -IOSC    | HA-7712  | -           | 25    | -   | -           | 25    | -   | mA             |
|                                       |          | HA-7713  | -           | 10    | -   | -           | 10    | -   | mA             |
| Input Noise Voltage                   | $e_N$    | $R_S = 100\Omega$ , $f = 1kHz$                         |             |       |     |             |       |     |                |
|                                       |          | HA-7712 $R_L = 100k\Omega$                             | -           | 30    | -   | -           | 30    | -   | $nV/\sqrt{Hz}$ |
|                                       |          | HA-7713 $R_L = 1M\Omega$                               | -           | 60    | -   | -           | 60    | -   | $nV/\sqrt{Hz}$ |
| Input Noise Current                   | $I_N$    | $R_S = 100\Omega$ , $f = 10kHz$                        | -           | 0.001 | -   | -           | 0.001 | -   | $pA/\sqrt{Hz}$ |
| Slew Rate                             | SR       | HA-7712 $R_L = 100k\Omega$                             | -           | 0.45  | -   | -           | 0.45  | -   | $V/\mu s$      |
|                                       |          | HA-7713 $R_L = 1M\Omega$                               | -           | 0.04  | -   | -           | 0.04  | -   | $V/\mu s$      |
| Rise Time                             | $t_R$    | HA-7712 $R_L = 100k\Omega$                             | -           | 0.35  | -   | -           | 0.35  | -   | $\mu s$        |
|                                       |          | HA-7713 $R_L = 1M\Omega$                               | -           | 2.5   | -   | -           | 2.5   | -   | $\mu s$        |
| Over Shoot                            |          | HA-7712 $R_L = 100k\Omega$                             | -           | 7     | -   | -           | 7     | -   | %              |
|                                       |          | HA-7713 $R_L = 1M\Omega$                               | -           | 17    | -   | -           | 17    | -   | %              |
| Operating Supply Range                | V+ to V- |  | 4           | -     | 16  | 4           | -     | 16  | V              |
| Supply Current                        | $I_S$    | HA-7712 $R_L = 100k\Omega$                             | -           | 150   | 200 | -           | 150   | 200 | $\mu A$        |
|                                       |          | HA-7713 $R_L = 1M\Omega$                               | -           | 15    | 30  | -           | 15    | 30  | $\mu A$        |

**NOTES:**

- Parameter guaranteed by design and characterization, and is not production tested.
- Typical values are guaranteed by design and characterization, and are not production tested.
- Long term input offset voltage stability refers to the average trend line of  $V_{OS}$  vs time over extended periods after the first 24 hours of operation.

### Ordering Information

| PART        | TEMPERATURE RANGE | PACKAGE           | PART        | TEMPERATURE RANGE | PACKAGE           |
|-------------|-------------------|-------------------|-------------|-------------------|-------------------|
| HA3-7712A-5 | 0°C to +70°C      | 8-Pin Plastic DIP | HA3-7713A-5 | 0°C to +70°C      | 8-Pin Plastic DIP |
| HA3-7712B-5 |                   | 8-Pin Plastic DIP | HA3-7713B-5 |                   | 8-Pin Plastic DIP |
| HA9P7712B-5 |                   | 8-Pin SOIC        | HA9P7713B-5 |                   | 8-Pin SOIC        |
| HA2-7712A-5 |                   | 8-Pin TO-99       | HA2-7713A-5 |                   | 8-Pin TO-99       |
| HA2-7712B-5 |                   | 8-Pin TO-99       | HA2-7713B-5 |                   | 8-Pin TO-99       |
| HA3-7712A-9 | -40°C to +85°C    | 8-Pin Plastic DIP | HA3-7713A-9 | -40°C to +85°C    | 8-Pin Plastic DIP |
| HA3-7712B-9 |                   | 8-Pin Plastic DIP | HA3-7713B-9 |                   | 8-Pin Plastic DIP |
| HA9P7712B-9 |                   | 8-Pin SOIC        | HA9P7713B-9 |                   | 8-Pin SOIC        |
| HA2-7712A-9 |                   | 8-Pin TO-99       | HA2-7713A-9 |                   | 8-Pin TO-99       |
| HA2-7712B-9 |                   | 8-Pin TO-99       | HA2-7713B-9 |                   | 8-Pin TO-99       |

## Ultra High Slew Rate Operational Amplifier

August 1991

### Features

- Unity Gain Bandwidth ..... 350MHz
- Full Power Bandwidth ..... 53MHz
- High Slew Rate ..... 1000V/ $\mu$ s
- High Output Drive .....  $\pm 50$ mA
- Monolithic Construction

### Applications

- RF/IF Processors
- Video Amplifiers
- High Speed Cable Drivers
- Pulse Amplifiers
- High Speed Communications
- Fast Data Acquisition Systems

### Description

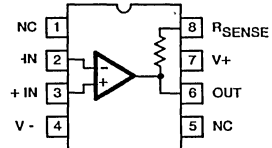
The HFA-0001 is an all bipolar op amp featuring high slew rate (1000V/ $\mu$ s), and high unity gain bandwidth (350MHz). These features combined with fast settling time (25ns) make this product very useful in high speed data acquisition systems as well as RF, video, and pulse amplifier designs. Other outstanding characteristics include low bias currents (15 $\mu$ A), low offset current (18 $\mu$ A), and low offset voltage (6mV).

The HFA-0001 offers high performance at low cost. It can replace hybrids and RF transistor amplifiers, simplifying designs while providing increased reliability due to monolithic construction. To enhance the ease of design, the HFA-0001 has a 50 $\Omega$   $\pm 20\%$  resistor connected from the output of the op amp to a separate pin. This can be used when driving 50 $\Omega$  strip line, microstrip, or coax cable.

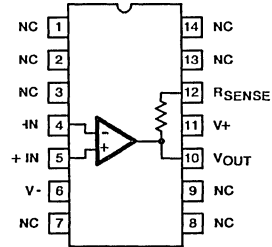
The performance of the HFA-0001-9 is guaranteed from -40 $^{\circ}$ C to +85 $^{\circ}$ C, while the HFA-0001-5 is guaranteed from 0 $^{\circ}$ C to +75 $^{\circ}$ C. The HFA-0001 is available in 16 pin SOIC, 8 pin Plastic Mini-Dip and 14 pin Sidebraze packages. For MIL-STD-883 compliant product and Ceramic LCC package consult the HFA-0001/883 datasheet.

### Pinouts

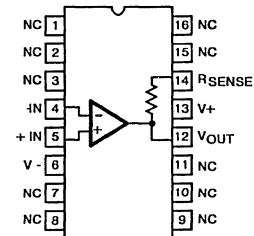
HFA3-0001-5 (PLASTIC MINI-DIP)  
TOP VIEW



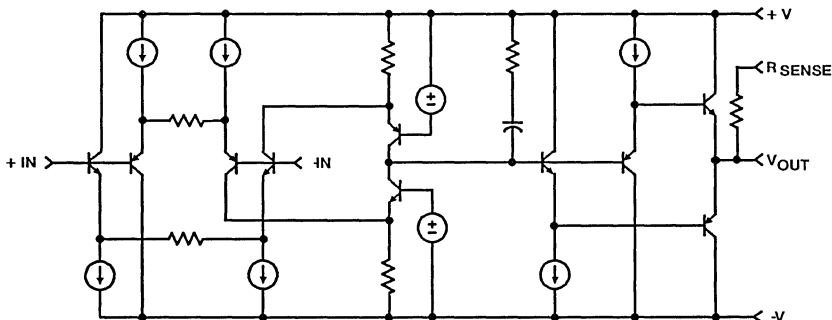
HFA1-0001-5/-9 (CERAMIC SIDEBRAZE DIP)  
TOP VIEW



HFA9P0001-5 (WIDE BODY SOIC)  
TOP VIEW



### Simplified Schematic





## Specifications HFA-0001

### Absolute Maximum Ratings (Note 1)

|   |      |
|---|------|
| Voltage Between V+ and V- Terminals ..... | 12V  |
| Differential Input Voltage .....          | 5V   |
| Common Mode Input Voltage .....           | ±4V  |
| Output Current .....                      | 60mA |

### Operating Temperature Range

|                                    |                                 |
|------------------------------------|---------------------------------|
| HFA-0001-9 .....                   | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| HFA-0001-5 .....                   | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| Storage Temperature .....          | -65°C ≤ T <sub>A</sub> ≤ +150°C |
| Maximum Junction Temperature ..... | +175°C                          |

### Electrical Specifications V+ = +5V, V- = -5V, Unless Otherwise Specified

| PARAMETER                            | TEMP                    | HFA-0001-9 |      |      | HFA-0001-5 |      |      | UNITS  |   |
|--------------------------------------|-------------------------|------------|------|------|------------|------|------|--------|---|
|                                      |                         | MIN        | TYP  | MAX  | MIN        | TYP  | MAX  |        |   |
| <b>INPUT CHARACTERISTICS</b>         |                         |            |      |      |            |      |      |        |   |
| Offset Voltage                       | +25°C                   | -          | 6    | 30   | -          | 6    | 30   | mV     |   |
|                                      | High                    | -          | 4.5  | 30   | -          | 4.5  | 30   | mV     |   |
|                                      | Low                     | -          | 12.5 | 50   | -          | 12.5 | 35   | mV     |   |
| Average Offset Voltage Drift         | High                    | -          | 50   | -    | -          | 50   | -    | μV/°C  |   |
|                                      | Low                     | -          | 100  | -    | -          | 100  | -    | μV/°C  |   |
| Bias Current                         | +25°C                   | -          | 15   | 100  | -          | 15   | 100  | μA     |   |
|                                      | Full                    | -          | 20   | 100  | -          | 20   | 100  | μA     |   |
| Offset Current                       | +25°C                   | -          | 18   | 50   | -          | 18   | 50   | μA     |   |
|                                      | Full                    | -          | 22   | 50   | -          | 22   | 50   | μA     |   |
| Common Mode Range                    | +25°C                   | ±3         | -    | -    | ±3         | -    | -    | V      |   |
| Differential Input Resistance        | +25°C                   | -          | 10   | -    | -          | 10   | -    | KΩ     |   |
| Input Capacitance                    | +25°C                   | -          | 2    | -    | -          | 2    | -    | pF     |   |
| Input Noise Voltage                  | 0.1Hz to 10Hz           | +25°C      | -    | 3.5  | -          | 3.5  | -    | μVrms  |   |
|                                      | 10Hz to 1MHz            | +25°C      | -    | 6.7  | -          | 6.7  | -    | μVrms  |   |
| Input Noise Voltage                  | f <sub>0</sub> = 10Hz   | +25°C      | -    | 640  | -          | 640  | -    | nV/√Hz |   |
|                                      | f <sub>0</sub> = 100Hz  | +25°C      | -    | 170  | -          | 170  | -    | nV/√Hz |   |
|                                      | f <sub>0</sub> = 1000Hz | +25°C      | -    | 43   | -          | 43   | -    | nV/√Hz |   |
| Input Noise Current                  | f <sub>0</sub> = 10Hz   | +25°C      | -    | 2.35 | -          | 2.35 | -    | nA/√Hz |   |
|                                      | f <sub>0</sub> = 100Hz  | +25°C      | -    | 0.57 | -          | 0.57 | -    | nA/√Hz |   |
|                                      | f <sub>0</sub> = 1000Hz | +25°C      | -    | 0.16 | -          | 0.16 | -    | nA/√Hz |   |
| <b>TRANSFER CHARACTERISTICS</b>      |                         |            |      |      |            |      |      |        |   |
| Large Signal Voltage Gain (Note 2)   | +25°C                   | 150        | 200  | -    | 150        | 200  | -    | V/V    |   |
|                                      | High                    | 150        | 170  | -    | 100        | 170  | -    | V/V    |   |
|                                      | Low                     | 150        | 220  | -    | 150        | 220  | -    | V/V    |   |
| Common Mode Rejection Ratio (Note 3) | +25°C                   | 45         | 47   | -    | 42         | 47   | -    | dB     |   |
|                                      | High                    | 40         | 45   | -    | 40         | 45   | -    | dB     |   |
|                                      | Low                     | 45         | 48   | -    | 42         | 48   | -    | dB     |   |
| Unity Gain Bandwidth                 | +25°C                   | -          | 350  | -    | -          | 350  | -    | MHz    |   |
| Minimum Stable Gain                  | Full                    | 1          | -    | -    | 1          | -    | -    | V/V    |   |
| <b>OUTPUT CHARACTERISTICS</b>        |                         |            |      |      |            |      |      |        |   |
| Output Voltage Swing                 | R <sub>L</sub> = 100Ω   | +25°C      | -    | ±3.5 | -          | -    | ±3.5 | -      | V |
|                                      | R <sub>L</sub> = 1k     | +25°C      | ±3.5 | ±3.7 | -          | ±3.5 | ±3.7 | -      | V |
|                                      | High                    | ±3.0       | ±3.6 | -    | ±3.0       | ±3.6 | -    | V      |   |
|                                      | Low                     | ±3.5       | ±3.7 | -    | ±3.5       | ±3.7 | -    | V      |   |
| Full Power Bandwidth (Note 5)        | +25°C                   | -          | 53   | -    | -          | 53   | -    | MHz    |   |
| Output Resistance, Open Loop         | +25°C                   | -          | 3    | -    | -          | 3    | -    | Ω      |   |
| Output Current                       | Full                    | ±30        | ±50  | -    | ±30        | ±50  | -    | mA     |   |

## Specifications HFA-0001

### Electrical Specifications (Continued) $V_+ = +5V, V_- = -5V$ , Unless Otherwise Specified

| PARAMETER                             | TEMP  | HFA-0001-9 |      |     | HFA-0001-5 |      |     | UNITS      |
|---------------------------------------|-------|------------|------|-----|------------|------|-----|------------|
|                                       |       | MIN        | TYP  | MAX | MIN        | TYP  | MAX |            |
| <b>TRANSIENT RESPONSE</b>             |       |            |      |     |            |      |     |            |
| Rise Time (Note 4, 6)                 | +25°C | -          | 480  | -   | -          | 480  | -   | ps         |
| Slew Rate (Note 4, 7)                 | +25°C | -          | 1000 | -   | -          | 1000 | -   | V/ $\mu$ s |
|                                       |       |            |      |     |            |      |     |            |
|                                       |       |            |      |     |            |      |     |            |
| Settling Time (3V Step)               | +25°C | -          | 875  | -   | -          | 875  | -   | V/ $\mu$ s |
|                                       |       |            |      |     |            |      |     |            |
|                                       |       |            |      |     |            |      |     |            |
| Overshoot (Note 4, 6)                 | +25°C | -          | 36   | -   | -          | 36   | -   | %          |
| <b>POWER SUPPLY CHARACTERISTICS</b>   |       |            |      |     |            |      |     |            |
| Supply Current                        | Full  | -          | 65   | 75  | -          | 65   | 75  | mA         |
| Power Supply Rejection Ratio (Note 8) | +25°C | 40         | 42   | -   | 37         | 42   | -   | dB         |
|                                       | High  | 35         | 41   | -   | 35         | 41   | -   | dB         |
|                                       | Low   | 40         | 42   | -   | 37         | 42   | -   | dB         |

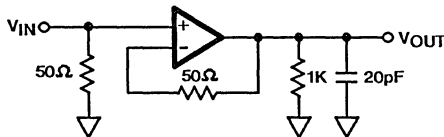
**NOTES:**

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2.  $V_{OUT} = 0$  to  $\pm 2V$ ,  $R_L = 1K$
3.  $\Delta V_{CM} = \pm 2V$
4.  $R_L = 100\Omega$
5. Full Power Bandwidth is calculated by equation:  

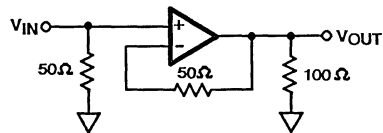
$$FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}}, V_{peak} = 3.0V$$
6.  $V_{OUT} = \pm 200mV, A_V = +1$
7.  $V_{OUT} = \pm 3V, A_V = +1$
8.  $\Delta V_S = \pm 4V$  to  $\pm 6V$

### Test Circuits

**LARGE SIGNAL RESPONSE TEST CIRCUIT**



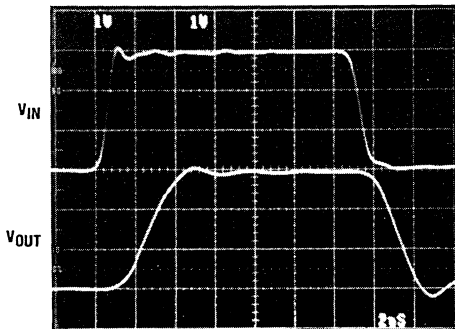
**SMALL SIGNAL RESPONSE TEST CIRCUIT**



**LARGE SIGNAL RESPONSE**

$V_{OUT} = 0$  to  $3V$

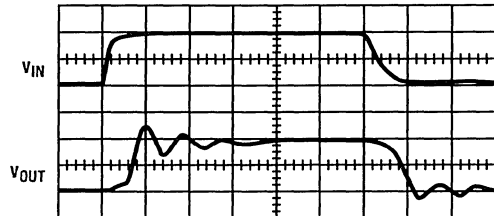
Vertical Scale: 1V/Div. Horizontal Scale: 2ns/Div.



**SMALL SIGNAL RESPONSE**

$V_{OUT} = 0$  to  $200mV$

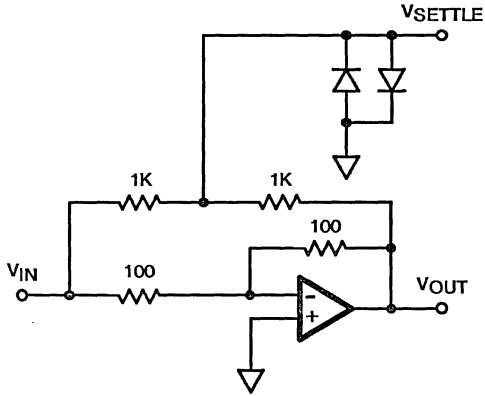
Vertical Scale: 100mV/Div. Horizontal Scale: 2ns/Div.



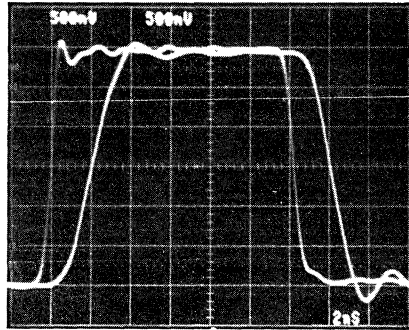
NOTE: Initial step in output is due to fixture feedthrough

Test Circuits (Continued)

SETTLING TIME SCHEMATIC



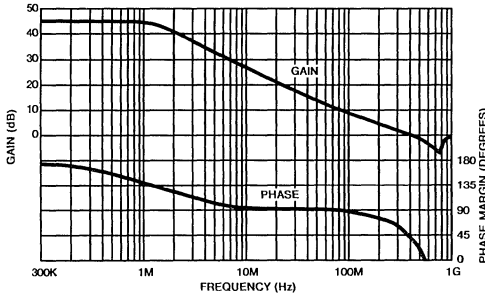
PROPAGATION DELAY  
Vertical Scale: 500mV/Div. Horizontal Scale: 2ns/Div.  
 $A_V = +1$ ,  $R_L = 100\Omega$ ,  $V_{OUT} = 0$  to  $3V$



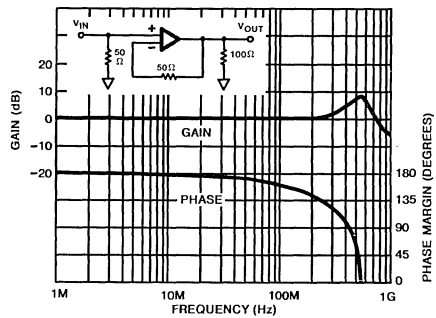
NOTE: Test Fixture delay of 450ps is included

Typical Performance Curves  $V_S = \pm 5V$ ,  $T_A = +25^\circ C$ , Unless Otherwise Specified

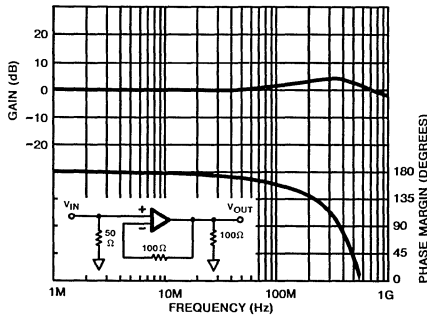
OPEN LOOP GAIN AND PHASE vs FREQUENCY  
 $R_L = 100\Omega$



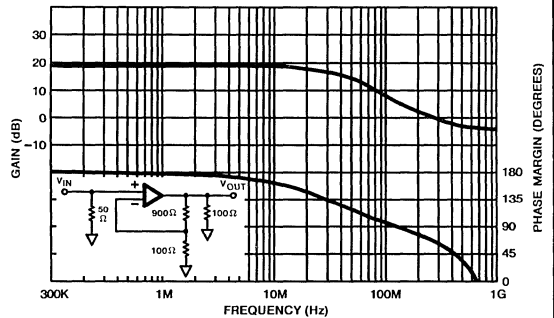
CLOSED LOOP GAIN vs FREQUENCY  
 $A_V = +1$ ,  $R_L = 100\Omega$ ,  $R_F = 50\Omega$



CLOSED LOOP GAIN vs FREQUENCY

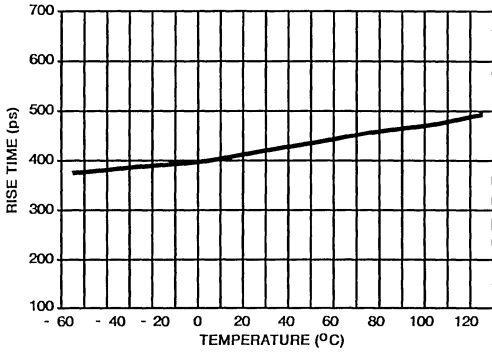


CLOSED LOOP GAIN vs FREQUENCY  
 $A_V = +10$ ,  $R_L = 100\Omega$

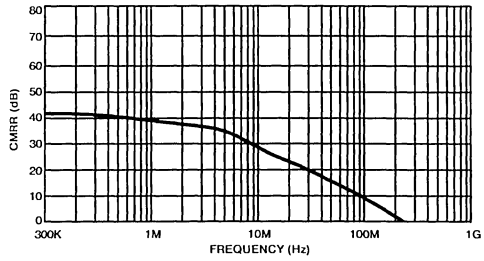


Typical Performance Curves (Continued)  $V_S = \pm 5V$ ,  $T_A = +25^\circ C$ , Unless Otherwise Specified

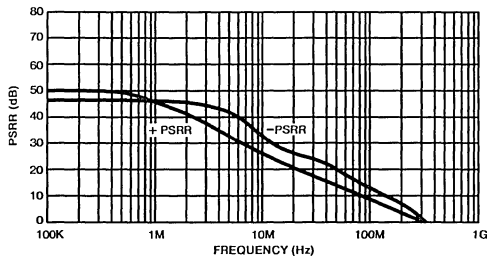
RISE TIME vs TEMPERATURE  
 $A_V = +1$ ,  $R_L = 100\Omega$ ,  $V_{OUT} = 0$  to  $200mV$



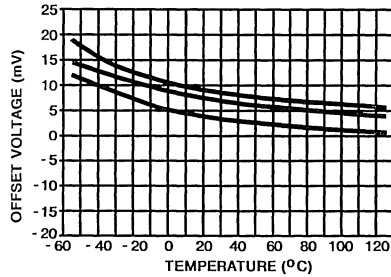
CMRR vs FREQUENCY



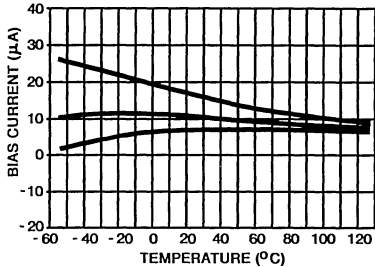
PSRR vs FREQUENCY



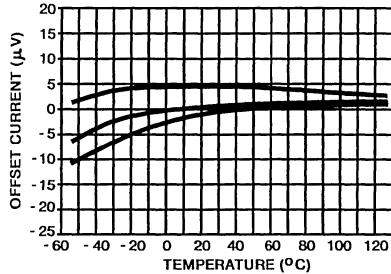
OFFSET VOLTAGE vs TEMPERATURE  
 3 Representative Units



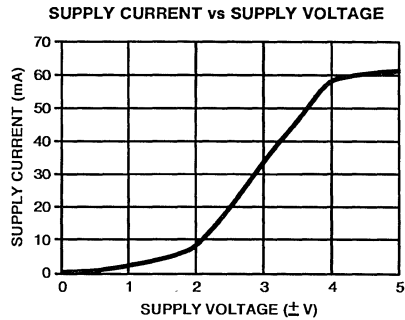
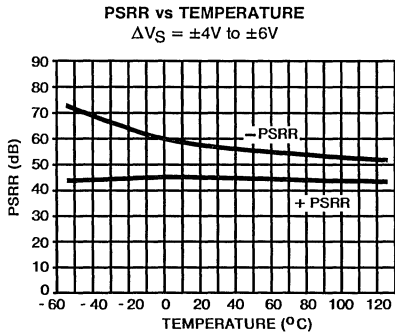
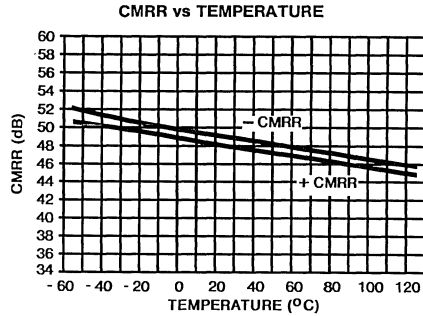
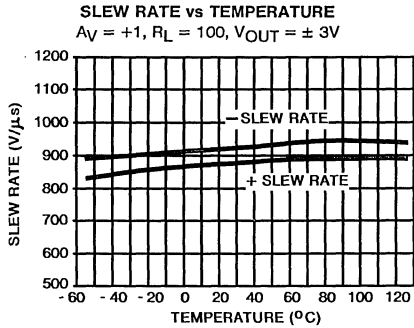
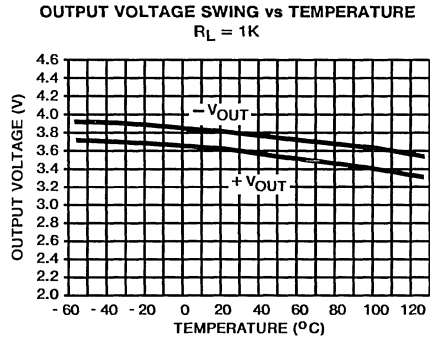
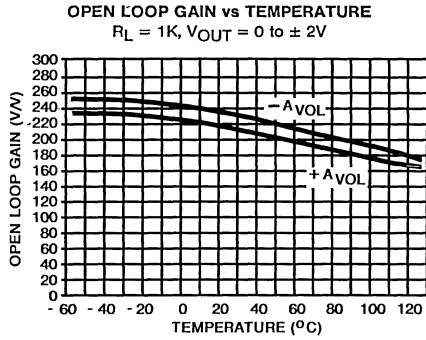
BIAS CURRENT vs TEMPERATURE  
 3 Representative Units



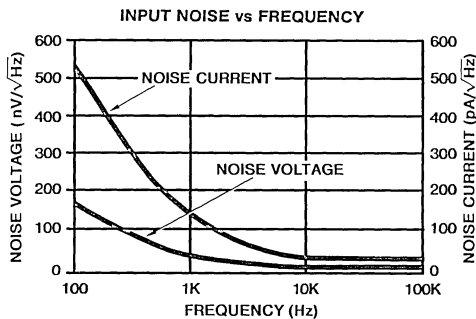
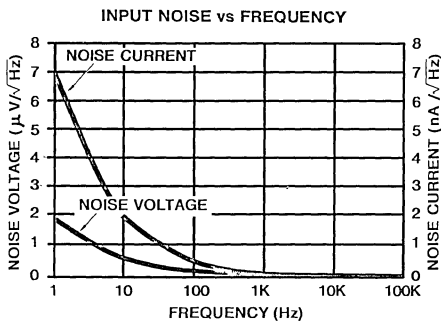
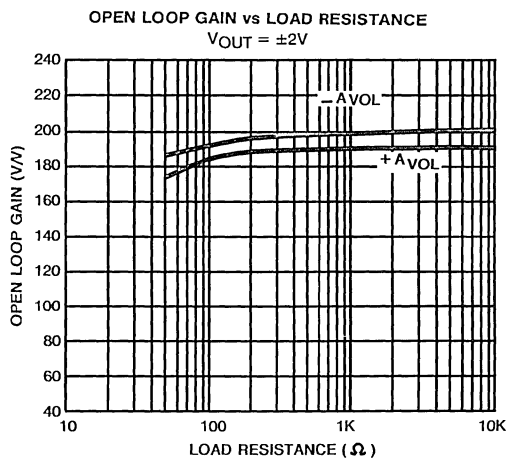
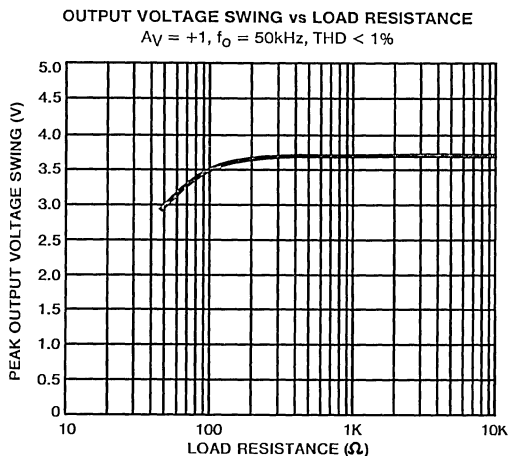
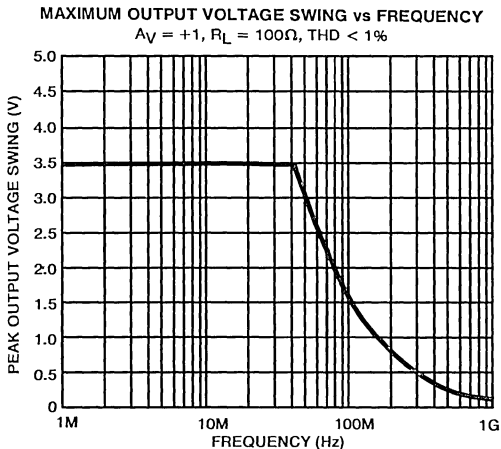
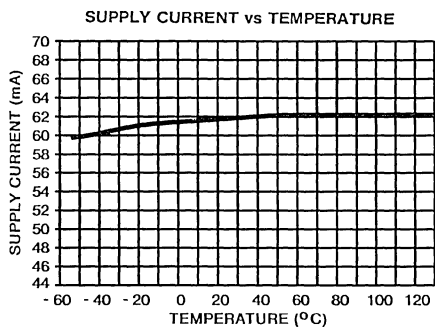
OFFSET CURRENT vs TEMPERATURE  
 3 Representative Units




Typical Performance Curves (Continued)  $V_S = \pm 5V$ ,  $T_A = +25^\circ C$ , Unless Otherwise Specified



Typical Performance Curves (Continued)  $V_S = \pm 5V$ ,  $T_A = +25^\circ C$ , Unless Otherwise Specified



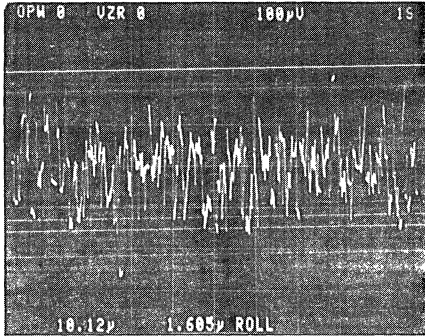
  
 OPERATIONAL AMPLIFIERS

**Typical Performance Curves (Continued)**  $V_S = \pm 5V$ ,  $T_A = +25^\circ C$ , Unless Otherwise Specified

**INPUT VOLTAGE NOISE**

0.1Hz to 10Hz

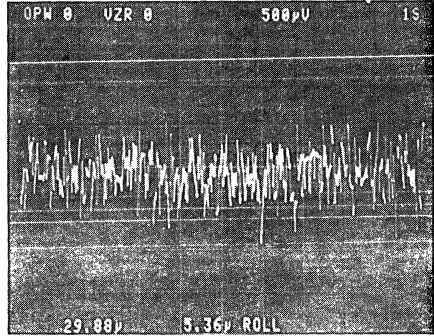
$A_V = 50$ , Noise Voltage =  $1.605\mu V_{rms}$  (RTI)  
Noise Voltage =  $10.12\mu V_{p-p}$



**INPUT NOISE VOLTAGE**

10Hz to 1MHz

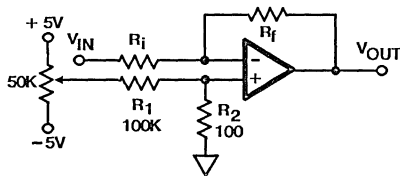
$A_V = 50$ , Noise Voltage =  $5.36\mu V_{rms}$  (RTI)  
Noise Voltage =  $29.88\mu V_{p-p}$



**Applications Information**

**Offset Adjustment**

When applications require the offset voltage to be as low as possible, the figure below shows two possible schemes for adjusting offset voltage.

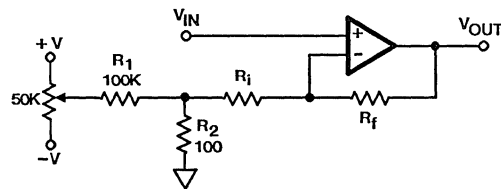


Adjustment  
Range  $\approx \pm V$

$$\frac{R_2}{R_1}$$

**FIGURE 1. INVERTING GAIN**

For a voltage follower application, use the circuit in Figure 2 without  $R_2$  and with  $R_i$  shorted.  $R_1$  should be  $1M\Omega$  to  $10M\Omega$ . the adjustment resistors will cause only a very small gain error.



Adjustment  
Range  $\approx \pm V$

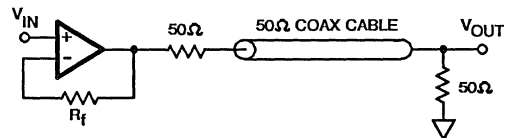
$$\text{Gain} \approx 1 + \frac{R_f}{R_i + R_2}$$

**FIGURE 2. NON-INVERTING GAIN**

**PC Board Layout Guidelines**

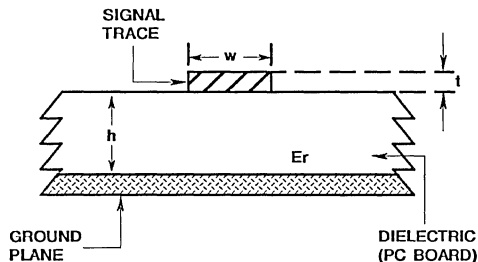
When designing with the HFA-0001, good high frequency (RF) techniques should be used when making a PC board. A massive ground plane should be used to maintain a low impedance ground. Proper shielding and use of short interconnection leads are also very important.

To achieve maximum high frequency performance, the use of low impedance transmission lines with impedance matching is recommended:  $50\Omega$  lines are common in communications and  $75\Omega$  lines in video systems. Impedance matching is important to minimize reflected energy therefore minimizing transmitted signal distortion. This is accomplished by using a series matching resistor ( $50\Omega$  or  $75\Omega$ ), matched transmission line ( $50\Omega$  or  $75\Omega$ ), and a matched terminating resistor, as shown in the figure below. Note that there will be a 6dB loss from input to output. The HFA-0001 has an integral  $50\Omega \pm 20\%$  resistor connected to the op amps output with the other end of the resistor pinned out. This  $50\Omega$  resistor can be used as the series resistor instead of an external resistor.



**Applications Information (Continued)**

PC board traces can be made to look like a 50Ω or 75Ω transmission line, called microstrip. Microstrip is a PC board trace with a ground plane directly beneath, on the opposite side of the board, as shown below.



When manufacturing pc boards, the trace width can be calculated based on a number of variables. The following equation is reasonably accurate for calculating the proper trace width for a 50Ω transmission line.

$$Z_0 = \frac{87}{\sqrt{E_r + 1.41}} \ln \left( \frac{5.98h}{0.8w + t} \right) \Omega$$

Power supply decoupling is essential for high frequency op amps. A 0.01μf high quality ceramic capacitor at each supply pin in parallel with a 1μf tantalum capacitor will provide excellent decoupling as shown in Figure 3. Chip capacitors produce the best results due to ease of placement next to the op amp and they have negligible lead inductance. If leaded capacitors are used, the leads should be kept as short as possible to minimize lead inductance. The figures below illustrate two different decoupling schemes. Figure 4 improves the PSRR because the resistor and capacitors create low pass filters. Note that the supply current will create a voltage drop across the resistor.

**Saturation Recovery**

When an op amp is over driven output devices can saturate and sometimes take a long time to recover. By clamping the

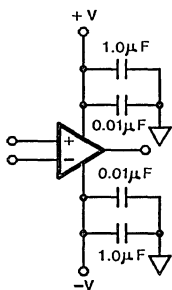
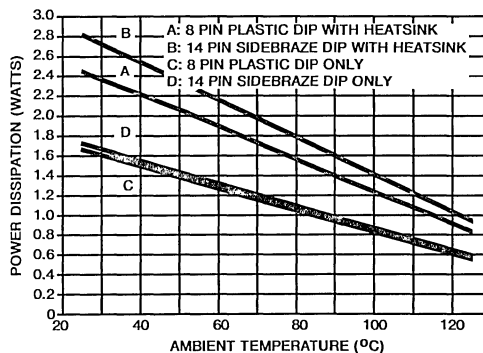


FIGURE 3. POWER SUPPLY DECOUPLING

input to safe levels, output saturation can be avoided. If output saturation cannot be avoided, the recovery time from 25% over-drive is 20ns and 30ns from 50% over-drive.

**Thermal Management**

The HFA-0001 can sink and source a large amount of current making it very useful in many applications. Care must be taken not to exceed the power handling capability of the part to insure proper performance and maintain high reliability. The following graph shows the maximum power handling capability of the HFA-0001 without exceeding the maximum allowable junction temperature of 175°C. The curves also show the improved power handling capability when heatsinks are used based on AVVID heatsink #5801B for the 8 pin Plastic DIP and IERC heatsink #PEP50AB for the 14 pin Sidebraze DIP. These curves are based on natural convection. Forced air will greatly improve the power dissipation capabilities of a heatsink.



| Thermal Constants (°C/W) | θ <sub>ja</sub> | θ <sub>jc</sub> |
|--------------------------|-----------------|-----------------|
| HFA1-0001-5/-9           | 75              | 13              |
| HFA3-0001-5              | 98              | 36              |
| HFA9P-0001-5/-9          | 96              | 27              |

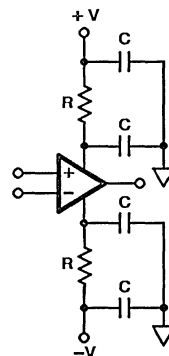


FIGURE 4. IMPROVED DECOUPLING/CURRENT LIMITING

3  
OPERATIONAL AMPLIFIERS



August 1991

### Features

- Wide Gain Bandwidth Product ..... 1GHz
- High Slew Rate ..... 250V/ $\mu$ s
- High Open Loop Gain ..... 105V/mV
- Low Offset Voltage ..... 0.6mV
- Low Power Consumption ..... 143mW
- Low Input Voltage Noise @ 1KHz ..... 2.7nV/ $\sqrt{\text{Hz}}$
- Monolithic Construction

### Applications

- RF/IF Processors
- Video Amplifiers
- Radar Systems
- Pulse Amplifiers
- High Speed Communications
- Fast Data Acquisition Systems

### Description

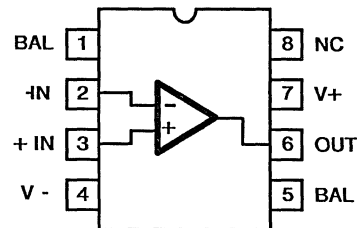
The HFA-0002 is a very wideband, high slew rate, op amp, featuring precision DC characteristics. Stable in gains of 10 or greater this all bipolar op amp offers a combination of AC and DC performance never seen before in monolithic form.

The high gain bandwidth product (1GHz) and high slew rate (250V/ $\mu$ s) make this op amp ideal for use in video and RF circuits. The low offset voltage (0.6mV), low bias current (0.23 $\mu$ A), and low voltage noise (2.7nV/ $\sqrt{\text{Hz}}$ ) specifications combined with the excellent AC characteristics make this op amp ideal for high speed data acquisition systems with high accuracy.

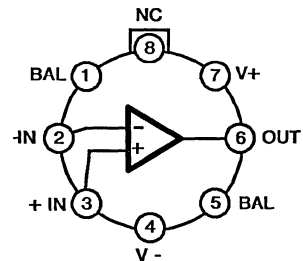
The HFA-0002-9 operates over the -40°C to +85°C temperature range, while the HFA-0002-5 operates over 0°C to +75°C. The HFA-0002 is available in 8 pin SOIC, 8 pin Ceramic Sidebraze DIP, 8 pin Plastic DIP, and 8 pin TO-99 Metal Can packages. For MIL-STD-883 compliant product and Ceramic LCC package consult the HFA-0002/883 datasheet.

### Pinouts

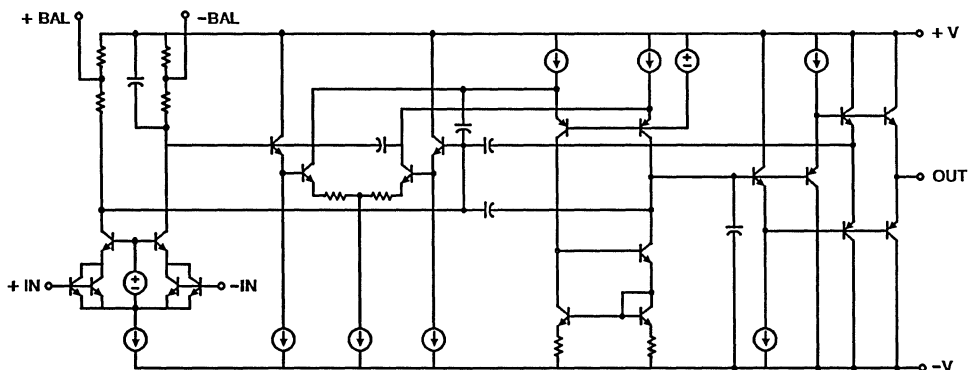
HFA9P0002-5/-9 (SOIC)  
 HFA7-0002-5/-9  
 (CERAMIC SIDEBRAZE DIP)  
 HFA3-0002-5/-9 (PLASTIC MINI-DIP)  
 TOP VIEW



HFA2-0002-5/-9 (TO-99 METAL CAN)  
 TOP VIEW



### Simplified Schematic



## Specifications HFA-0002

### Absolute Maximum Ratings (Note 1)

|   |       |
|---|-------|
| Voltage Between V+ and V- Terminals ..... | 12V   |
| Differential Input Voltage .....          | 5V    |
| Common Mode Input Voltage .....           | ±5V   |
| Output Current .....                      | ±20mA |

### Operating Temperature Range

|                                    |  |
|------------------------------------|--|
| HFA-0002-9 .....                   | $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  |
| HFA-0002-5 .....                   | $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$    |
| Storage Temperature .....          | $-65^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ |
| Maximum Junction Temperature ..... | +175°C   |

### Electrical Specifications +V = +5V, -V = -5V, Unless Otherwise Specified

| PARAMETER                             | TEMP                    | HFA-0002-5/-9 |      |     | UNITS  |
|---------------------------------------|-------------------------|---------------|------|-----|--------|
|                                       |                         | MIN           | TYP  | MAX |        |
| <b>INPUT CHARACTERISTICS</b>          |                         |               |      |     |        |
| Offset Voltage                        | +25°C                   | -             | 0.6  | 1   | mV     |
|                                       | Full                    | -             | 1.2  | 2   | mV     |
| Average Offset Voltage Drift          | Full                    | -             | 2.0  | -   | μV/°C  |
| Bias Current                          | +25°C                   | -             | 0.23 | 1.0 | μA     |
|                                       | High                    | -             | 0.1  | 1.0 | μA     |
|                                       | Low                     | -             | 0.32 | 2.0 | μA     |
| Offset Current                        | +25°C                   | -             | 0.12 | 1.0 | μA     |
|                                       | Full                    | -             | 0.16 | 1.0 | μA     |
| Common Mode Range                     | Full                    | ±2.5          | -    | -   | V      |
| Differential Input Resistance         | +25°C                   | -             | 1    | -   | MΩ     |
| Input Capacitance                     | +25°C                   | -             | 2    | -   | pF     |
| Input Noise Voltage                   | 0.1Hz to 10Hz           | +25°C         | -    | 5.1 | nVrms  |
|                                       | 10Hz to 1MHz            | +25°C         | -    | 375 | nVrms  |
| Input Noise Voltage                   | f <sub>o</sub> = 10Hz   | +25°C         | -    | 8.9 | nV/√Hz |
|                                       | f <sub>o</sub> = 100Hz  | +25°C         | -    | 3.7 | nV/√Hz |
|                                       | f <sub>o</sub> = 1000Hz | +25°C         | -    | 2.7 | nV/√Hz |
| Input Noise Current                   | f <sub>o</sub> = 10Hz   | +25°C         | -    | 25  | pA/√Hz |
|                                       | f <sub>o</sub> = 100Hz  | +25°C         | -    | 8.4 | pA/√Hz |
|                                       | f <sub>o</sub> = 1000Hz | +25°C         | -    | 4.5 | pA/√Hz |
| <b>TRANSFER CHARACTERISTICS</b>       |                         |               |      |     |        |
| Large Signal Voltage Gain (Note 2, 4) | Full                    | 80            | 105  | -   | V/mV   |
| Common Mode Rejection Ratio (Note 3)  | +25°C                   | 100           | 110  | -   | dB     |
|                                       | Full                    | 90            | 108  | -   | dB     |
| Gain Bandwidth Product                | f <sub>o</sub> = 1MHz   | +25°C         | -    | 1   | GHz    |
| Minimum Stable Gain                   | Full                    | 10            | -    | -   | V/V    |
| <b>OUTPUT CHARACTERISTICS</b>         |                         |               |      |     |        |
| Output Voltage Swing (Note 4)         | Full                    | ±3.5          | ±3.9 | -   | V      |
| Full Power Bandwidth (Note 5)         | +25°C                   | 10.6          | 13.3 | -   | MHz    |
| Output Resistance, Open Loop          | +25°C                   | -             | 5    | -   | Ω      |
| Output Current                        | Full                    | ±10           | ±12  | -   | mA     |
| <b>TRANSIENT RESPONSE</b>             |                         |               |      |     |        |
| Rise Time (Note 4, 6)                 | +25°C                   | -             | 3.2  | -   | ns     |
| Slew Rate (Note 4, 7, 10)             | +25°C                   | 200           | 250  | -   | V/μs   |
| Settling Time (Note 4, 7)             | +25°C                   | -             | 50   | -   | ns     |
| Overshoot (Note 4, 6)                 | +25°C                   | -             | 30   | -   | %      |
| <b>POWER SUPPLY CHARACTERISTICS</b>   |                         |               |      |     |        |
| Supply Current                        | Full                    | -             | 14   | 20  | mA     |
| Power Supply Rejection Ratio (Note 8) | Full                    | 90            | 99   | -   | dB     |

## Specifications HFA-0002

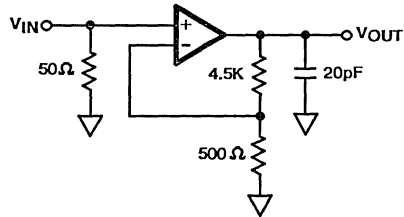
**NOTES:**

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2.  $V_{OUT} = \pm 3V$
3.  $\Delta V_{CM} = \pm 2V$
4.  $R_L = 5K, C_L = 20pF$
5. Full Power Bandwidth is guaranteed by equation:  

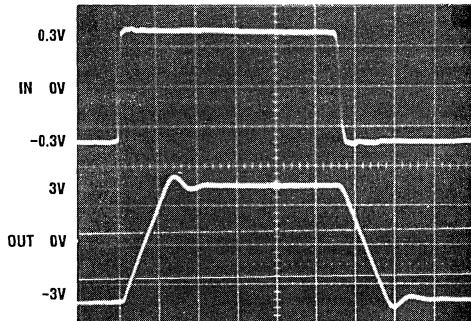
$$FPB = \frac{\text{Slew Rate}}{2\pi V_{peak}}, V_{peak} = 3.0V$$
6.  $V_{OUT} = \pm 100mV, A_V = +10$
7.  $V_{OUT} = \pm 3V, A_V = +10$
8.  $\Delta V_S = \pm 4V \text{ to } \pm 6V$
9.  $V_{OUT} = \pm 3.5V$
10. This parameter is not tested. This limit is guaranteed based on lot characterization and reflects lot to lot variation.

### Test Circuits

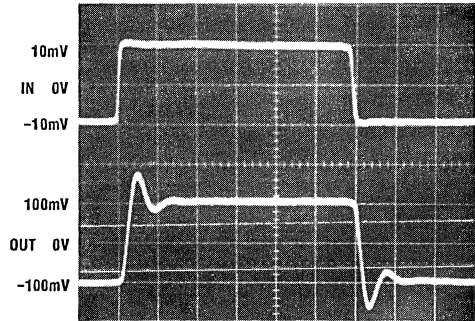
**LARGE & SMALL SIGNAL RESPONSE TEST CIRCUIT**



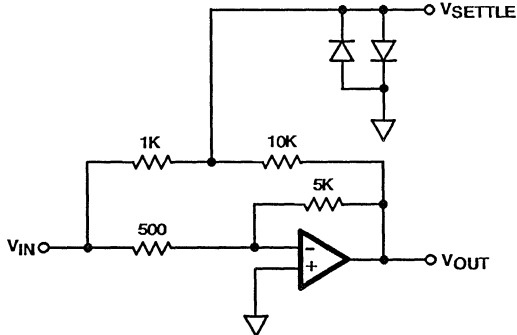
**LARGE SIGNAL RESPONSE**  
 Input: 0.2V/Div. Output: 2V/Div.  
 Horizontal Scale: 20ns/Div.



**SMALL SIGNAL RESPONSE**  
 Input: 10mV/Div. Output: 100mV/Div.



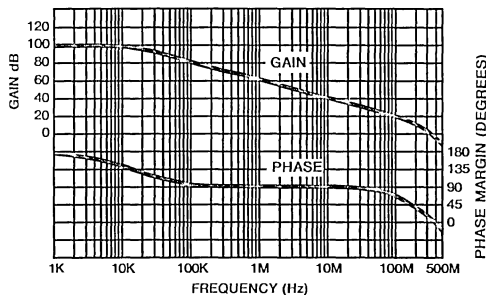
**SETTLING TIME SCHEMATIC**



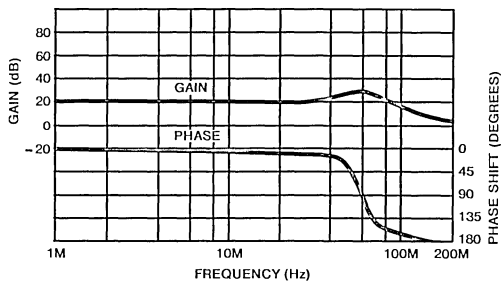
- $A_V = -1$
- Feedback and summing resistors must be matched (0.1%)
- HP5082-2810 clipping diodes recommended
- Tektronix P6201 FET probe used at settling point

Typical Performance Curves  $V_S = \pm 5V$ ,  $T_A = +25^\circ C$ , Unless Otherwise Specified

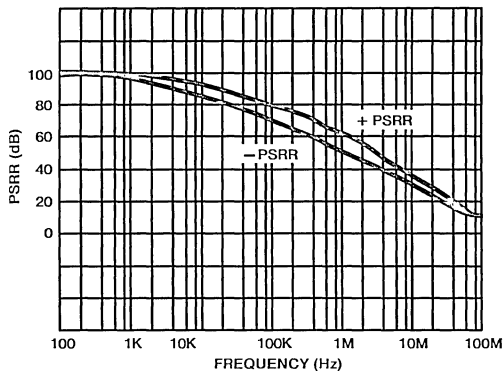
OPEN LOOP GAIN AND PHASE vs FREQUENCY



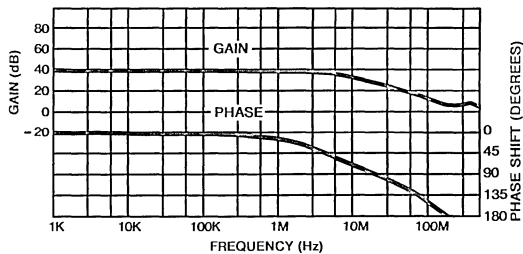
CLOSED LOOP GAIN vs FREQUENCY  
 $A_V = +10$ ,  $R_L = 5K$ ,  $C_L = 20pF$



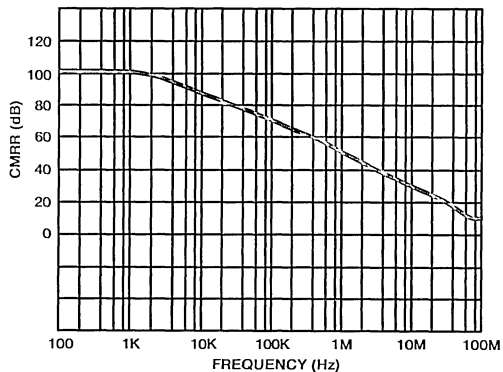
PSRR vs FREQUENCY



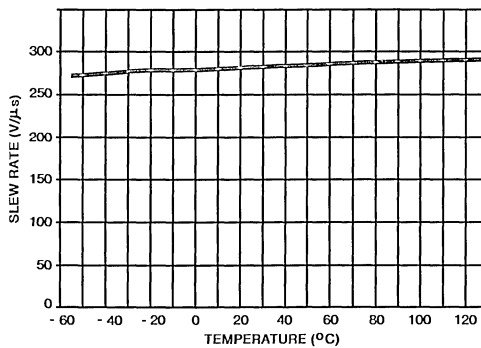
CLOSED LOOP GAIN vs FREQUENCY  
 $A_V = +100$ ,  $R_L = 5K$ ,  $C_L = 20pF$



CMRR vs FREQUENCY

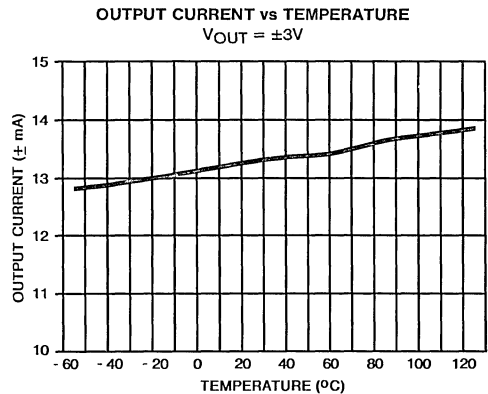
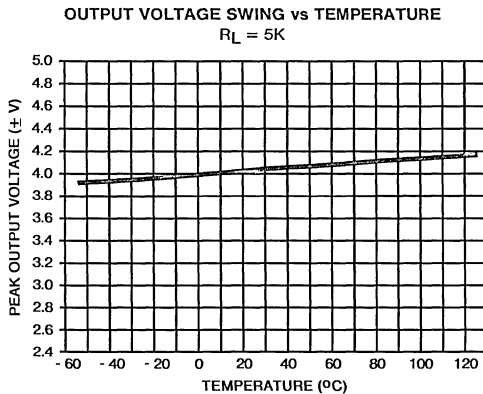
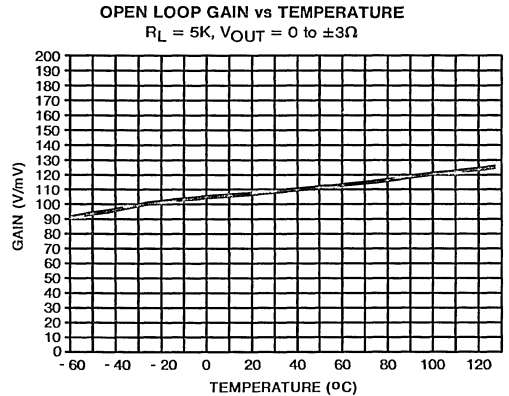
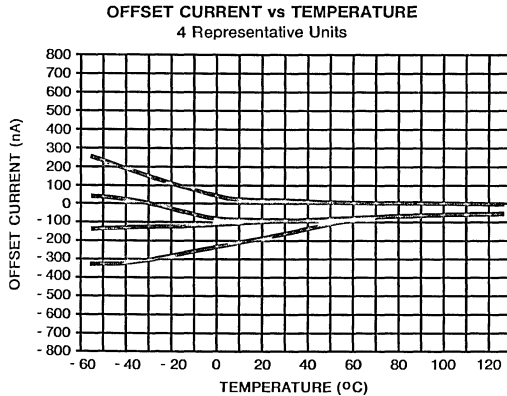
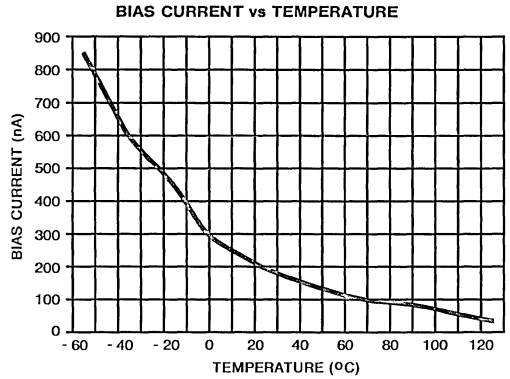
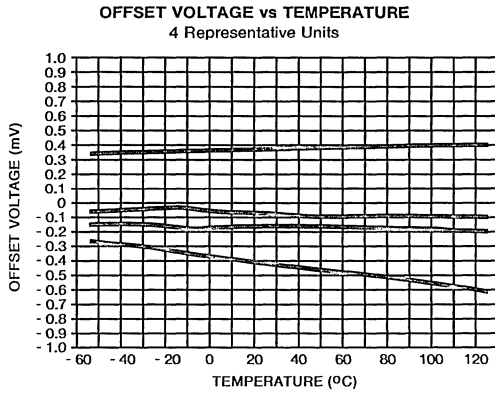


SLEW RATE vs TEMPERATURE  
 $V_{OUT} = 3V$ ,  $R_L = 5K$ ,  $C_L = 20pF$



  
 OPERATIONAL AMPLIFIERS

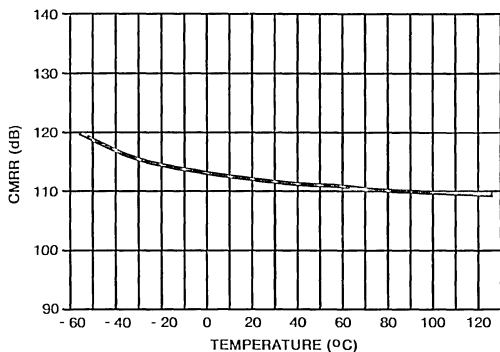
Typical Performance Curves (Continued)  $V_S = \pm 5V$ ,  $T_A = +25^\circ C$ , Unless Otherwise Specified



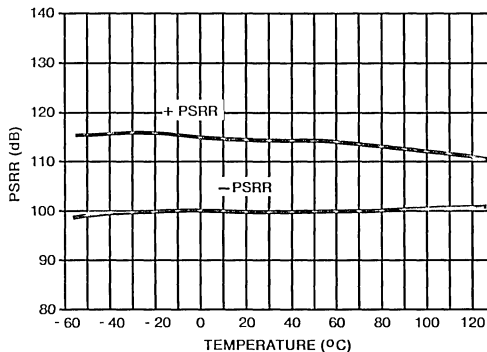
# HFA-0002

Typical Performance Curves (Continued)  $V_S = \pm 5V$ ,  $T_A = +25^\circ C$ , Unless Otherwise Specified

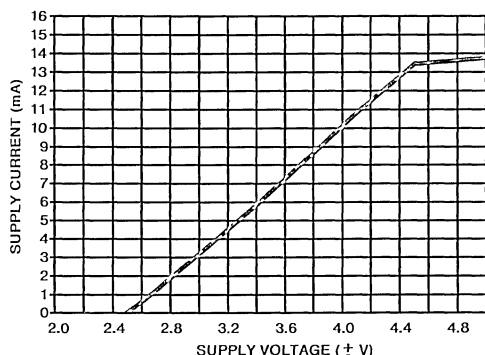
**CMRR vs TEMPERATURE**  
 $V_{CM} = 0$  to  $\pm 3V$



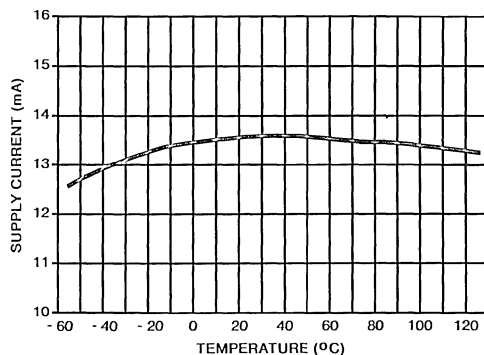
**PSRR vs TEMPERATURE**  
 $\Delta V_S = \pm 4V$  to  $\pm 6V$



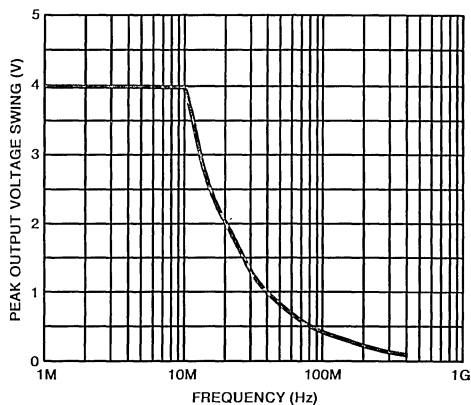
**SUPPLY CURRENT vs SUPPLY VOLTAGE**



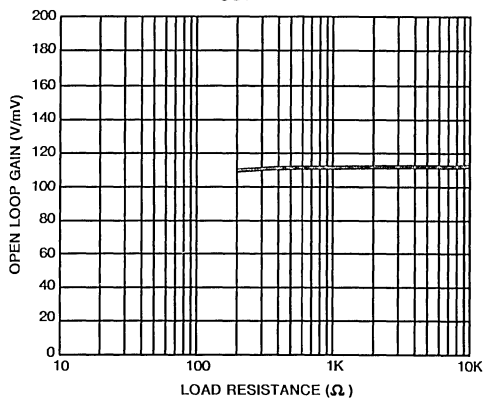
**SUPPLY CURRENT vs TEMPERATURE**



**OUTPUT VOLTAGE SWING vs FREQUENCY**  
 $A_V = +10$ ,  $R_L = 5K$



**OPEN LOOP GAIN vs LOAD RESISTANCE**  
 $V_{OUT} = \pm 3V$

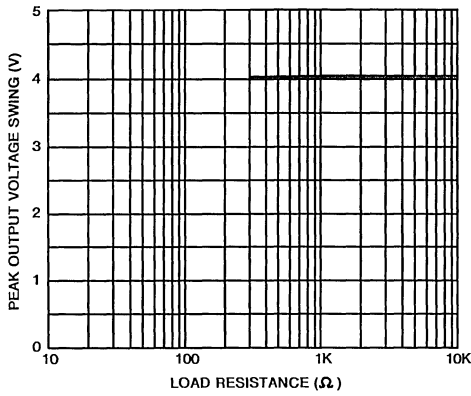


OPERATIONAL AMPLIFIERS

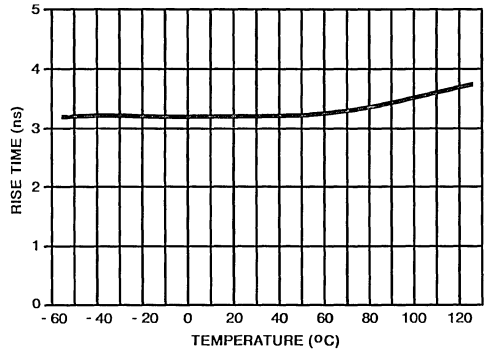
# HFA-0002

**Typical Performance Curves (Continued)**  $V_S = \pm 5V$ ,  $T_A = +25^\circ C$ , Unless Otherwise Specified

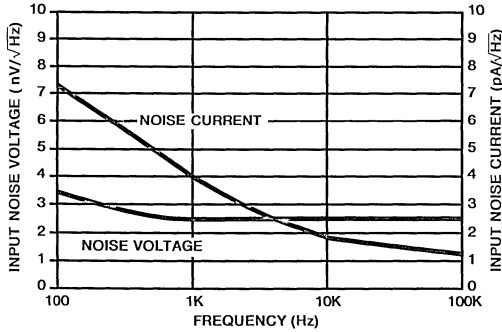
**OUTPUT VOLTAGE SWING vs LOAD RESISTANCE**



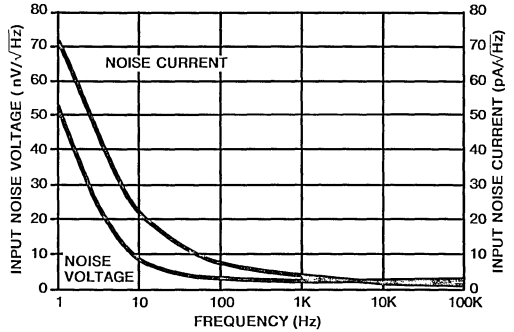
**RISE TIME vs TEMPERATURE**



**INPUT NOISE vs FREQUENCY**



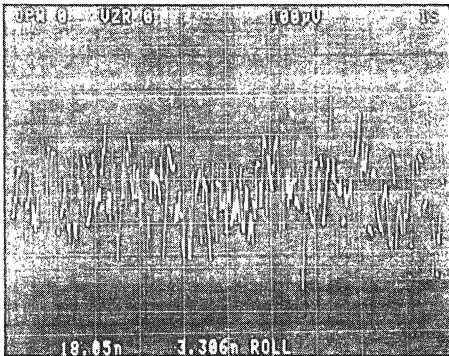
**INPUT NOISE vs FREQUENCY**



**INPUT NOISE VOLTAGE**

0.1Hz to 10Hz

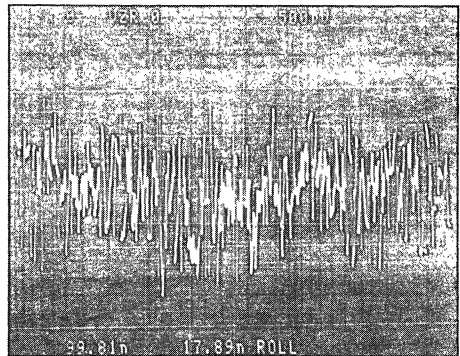
$A_V = 25,000$ , Noise Voltage =  $3.31nV_{rms}$  (RTI)



**INPUT NOISE VOLTAGE**

10Hz to 1MHz

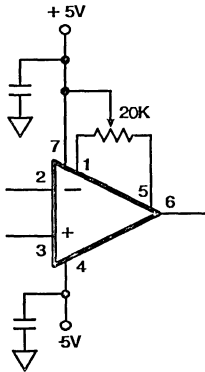
$A_V = 25,000$ , Noise Voltage =  $17.89nV_{rms}$  (RTI)



**Applications Information**

**Offset Voltage Adjustment**

The HFA-0002, due to its low offset voltage, will typically not require any external offset adjustment. If certain applications do require lower offset, the following diagram shows one possible configuration.



The power supply lines must be well decoupled to filter any power supply noise. A 20K trim pot will allow an offset adjustment of about 3mV, referred to input.

**PC Board Layout Guidelines**

When designing with the HFA-0002, good high frequency (RF) techniques should be used when doing pc board layouts. A massive ground plane should be used to maintain a low impedance ground. PC board traces should be kept as short as possible and kept wide to minimize trace inductance and impedance. Stray capacitance at the op amps

output and at the high impedance inputs should be kept to a minimum, to prevent any unwanted phase shift and bandwidth limiting.

When breadboarding remember to keep feedback resistor values low ( $\leq 5k\Omega$ ) for optimum performance. The use of metal film resistors for values over 200 $\Omega$  and carbon film resistors under 200 $\Omega$  typically gives the best performance. Remember to keep all lead lengths as short as possible to minimize lead inductance.

Sockets will add parasitic capacitance and inductance and therefore can limit AC performance as well as reduce stability. If sockets must be used, a low profile socket with minimum pin to pin capacitance will minimize any performance degradation.

Power supply decoupling is essential for high frequency op amps. A 0.01 $\mu$ F high quality ceramic capacitor at each supply pin in parallel with a 1 $\mu$ F tantalum capacitor will provide excellent decoupling. Chip capacitors produce the best results due to the ease of placement next to the op amp and they have negligible lead inductance. If leaded capacitors are used, again the lead lengths should be kept to a minimum.

**Saturation Recovery**

When an op amp is over driven output devices can saturate and sometime take a long time to recover. By clamping the input to safe levels, output saturation can be avoided. If output saturation cannot be avoided, the recovery time for an input sine wave at 25% overdrive is 100ns.

| Thermal Constants ( $^{\circ}\text{C}/\text{W}$ ) | $\theta_{ja}$ | $\theta_{jc}$ |
|---|---------------|---------------|
| HFA2-0002-5/-9 .....                              | 117           | 36            |
| HFA3-0002-5/-9 .....                              | 96            | 34            |
| HFA7-0002-5/-9 .....                              | 75            | 13            |
| HFA9P-0002-5/-9 .....                             | 158           | 43            |



August 1991

### Features

- Unity Gain Bandwidth .....300MHz
- Full Power Bandwidth ..... 22MHz
- High Slew Rate ..... 420V/ $\mu$ s
- High Output Drive .....  $\pm$ 50mA
- Monolithic Bipolar Construction

### Applications

- RF/IF Processors
- Video Amplifiers
- Radar Systems
- Pulse Amplifiers
- High Speed Communications
- Fast Data Acquisition Systems

### Description

The HFA-0005 is an all bipolar op amp featuring high slew rate (420V/ $\mu$ s), and high unity gain bandwidth (300MHz). These features combined with fast settling time (20ns) make this product very useful in high speed data acquisition systems as well as RF, video, and pulse amplifier designs.

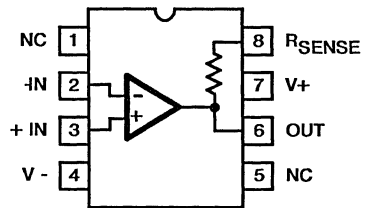
Other outstanding characteristics include low bias currents (15 $\mu$ A), low offset current (6 $\mu$ A), and low offset voltage (6mV). These high performance characteristics are achieved with only 40mA of supply current.

The HFA-0005 offers high performance at low cost. It can replace hybrids and RF transistor amplifiers, simplifying designs while providing increased reliability due to monolithic construction. To enhance the ease of design, the HFA-0005 has a 50 $\Omega$   $\pm$ 20% resistor connected from the output of the op amp to a separate pin. This can be used when driving 50 $\Omega$  strip line, microstrip, or coax cable.

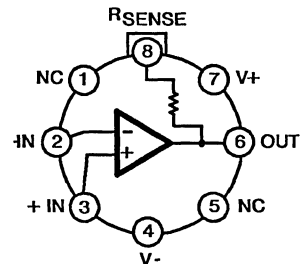
The performance of the HFA-0005-9 is guaranteed from -40 $^{\circ}$ C to +85 $^{\circ}$ C, while the HFA-0005-5 is guaranteed from 0 $^{\circ}$ C to +75 $^{\circ}$ C. The HFA-0005 is available in 8 pin SOIC, 8 pin Sidebraze, 8 pin Plastic Mini-Dip, and 8 pin TO-99 Metal Can packages. For MIL-STD-883 compliant product and Ceramic LCC package consult the HFA-0005/883 datasheet.

### Pinouts

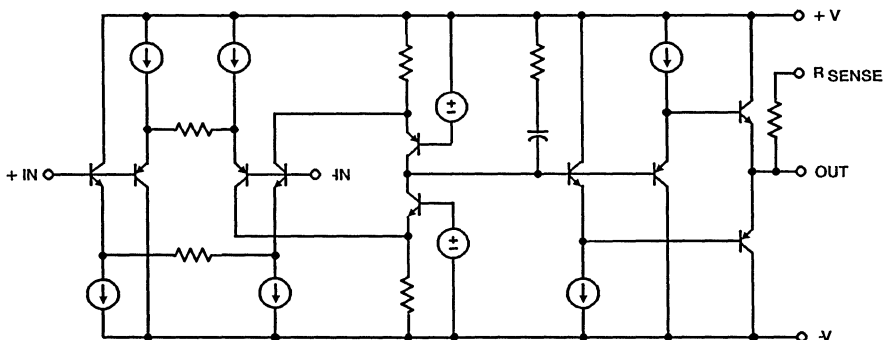
HFA9P0005-5/-9 (SOIC)  
HFA7-0005-5/-9  
(CERAMIC SIDEBRAZE DIP)  
HFA3-0005-5/-9 (PLASTIC MINI-DIP)  
TOP VIEW



HFA2-0005 (TO-99 METAL CAN)  
TOP VIEW



### Simplified Schematic



## Specifications HFA-0005

### Absolute Maximum Ratings (Note 1)

|   |       |
|---|-------|
| Voltage Between V+ and V- Terminals ..... | 12V   |
| Differential Input Voltage .....          | 5V    |
| Common Mode Input Voltage .....           | ±4V   |
| Output Current .....                      | ±60mA |

### Operating Temperature Range

|                                    |                                 |
|------------------------------------|---------------------------------|
| HFA-0005-9 .....                   | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| HFA-0005-5 .....                   | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| Storage Temperature .....          | -65°C ≤ T <sub>A</sub> ≤ +150°C |
| Maximum Junction Temperature ..... | +175°C                          |

### Electrical Specifications V+ = +5V, V- = -5V, Unless Otherwise Specified

| PARAMETER                             | TEMP                    | HFA-0005-9 |      |      | HFA-0005-5 |      |      | UNITS  |   |
|---------------------------------------|-------------------------|------------|------|------|------------|------|------|--------|---|
|                                       |                         | MIN        | TYP  | MAX  | MIN        | TYP  | MAX  |        |   |
| <b>INPUT CHARACTERISTICS</b>          |                         |            |      |      |            |      |      |        |   |
| Offset Voltage                        | +25°C                   | -          | 6    | 15   | -          | 6    | 30   | mV     |   |
|                                       | Full                    | -          | 11   | 45   | -          | 11   | 35   | mV     |   |
| Average Offset Voltage Drift          | Full                    | -          | 100  | -    | -          | 100  | -    | μV/°C  |   |
| Bias Current                          | +25°C                   | -          | 15   | 50   | -          | 15   | 100  | μA     |   |
|                                       | Full                    | -          | 20   | 50   | -          | 20   | 100  | μA     |   |
| Offset Current                        | +25°C                   | -          | 6    | 25   | -          | 6    | 50   | μA     |   |
|                                       | Full                    | -          | 12   | 50   | -          | 12   | 50   | μA     |   |
| Common Mode Range                     | Full                    | ±3         | -    | -    | ±3         | -    | -    | V      |   |
| Differential Input Resistance         | +25°C                   | -          | 10   | -    | -          | 10   | -    | KΩ     |   |
| Input Capacitance                     | +25°C                   | -          | 2    | -    | -          | 2    | -    | pF     |   |
| Input Noise Voltage                   | 0.1Hz to 10Hz           | +25°C      | -    | 2.5  | -          | -    | 2.5  | μVrms  |   |
|                                       | 10Hz to 1MHz            | +25°C      | -    | 5.8  | -          | -    | 5.8  | μVrms  |   |
| Input Noise Voltage                   | f <sub>o</sub> = 10Hz   | +25°C      | -    | 450  | -          | -    | 450  | nV/√Hz |   |
|                                       | f <sub>o</sub> = 100Hz  | +25°C      | -    | 160  | -          | -    | 160  | nV/√Hz |   |
|                                       | f <sub>o</sub> = 1000Hz | +25°C      | -    | 40   | -          | -    | 40   | nV/√Hz |   |
| Input Noise Current                   | f <sub>o</sub> = 10Hz   | +25°C      | -    | 2.0  | -          | -    | 2.0  | nA/√Hz |   |
|                                       | f <sub>o</sub> = 100Hz  | +25°C      | -    | 0.57 | -          | -    | 0.57 | nA/√Hz |   |
|                                       | f <sub>o</sub> = 1000Hz | +25°C      | -    | 0.11 | -          | -    | 0.11 | nA/√Hz |   |
| <b>TRANSFER CHARACTERISTICS</b>       |                         |            |      |      |            |      |      |        |   |
| Large Signal Voltage Gain (Note 2)    | +25°C                   | 150        | 230  | -    | 150        | 230  | -    | V/V    |   |
|                                       | High                    | 150        | 180  | -    | 150        | 180  | -    | V/V    |   |
|                                       | Low                     | 150        | 250  | -    | 150        | 250  | -    | V/V    |   |
| Common Mode Rejection Ratio (Note 3)  | Full                    | 45         | 47   | -    | 42         | 45   | -    | dB     |   |
| Unity Gain Bandwidth                  | +25°C                   | -          | 300  | -    | -          | 300  | -    | MHz    |   |
| Minimum Stable Gain                   | Full                    | 1          | -    | -    | 1          | -    | -    | V/V    |   |
| <b>OUTPUT CHARACTERISTICS</b>         |                         |            |      |      |            |      |      |        |   |
| Output Voltage Swing                  | R <sub>L</sub> = 100Ω   | +25°C      | -    | ±3.5 | -          | -    | ±3.5 | -      | V |
|                                       | R <sub>L</sub> = 1K     | Full       | ±3.5 | ±4.0 | -          | ±3.5 | ±4.0 | -      | V |
| Full Power Bandwidth (Note 5)         | +25°C                   | -          | 22   | -    | -          | 22   | -    | MHz    |   |
| Output Resistance, Open Loop          | +25°C                   | -          | 3.0  | -    | -          | 3.0  | -    | Ω      |   |
| Output Current                        | Full                    | ±25        | ±50  | -    | ±25        | ±50  | -    | mA     |   |
| <b>TRANSIENT RESPONSE</b>             |                         |            |      |      |            |      |      |        |   |
| Rise Time (Note 4, 6)                 | +25°C                   | -          | 480  | -    | -          | 480  | -    | ps     |   |
| Slew Rate (Note 7)                    | +25°C                   | -          | 420  | -    | -          | 420  | -    | V/μs   |   |
| Settling Time (3V Step) 0.1%          | +25°C                   | -          | 20   | -    | -          | 20   | -    | ns     |   |
| Overshoot (Note 4, 6)                 | +25°C                   | -          | 30   | -    | -          | 30   | -    | %      |   |
| <b>POWER SUPPLY CHARACTERISTICS</b>   |                         |            |      |      |            |      |      |        |   |
| Supply Current                        | +25°C                   | -          | 35   | 40   | -          | 35   | 40   | mA     |   |
|                                       | Full                    | -          | 37   | 40   | -          | 37   | 45   | mA     |   |
| Power Supply Rejection Ratio (Note 8) | +25°C                   | 40         | 42   | -    | 37         | 40   | -    | dB     |   |

# Specifications HFA-0005

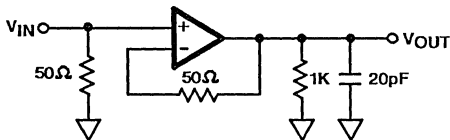
**NOTES:**

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2.  $V_{OUT} = 0$  to  $\pm 2V$ ,  $R_L = 1K$
3.  $\Delta V_{CM} = \pm 2V$
4.  $R_L = 100\Omega$
5. Full Power Bandwidth is calculated by equation:  

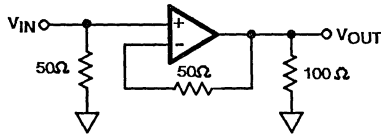
$$FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}} \quad V_{peak} = 3.0V$$
6.  $V_{OUT} = \pm 200mV$ ,  $A_V = +1$
7.  $V_{OUT} = \pm 3V$ ,  $A_V = +1$
8.  $\Delta V_S = \pm 4V$  to  $\pm 6V$

## Test Circuits

**LARGE SIGNAL RESPONSE TEST CIRCUIT**



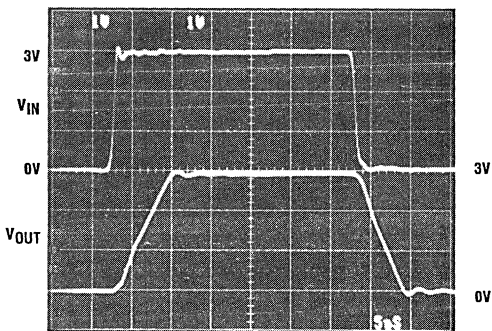
**SMALL SIGNAL RESPONSE TEST CIRCUIT**



**LARGE SIGNAL RESPONSE**

$V_{OUT} = 0$  to  $3V$

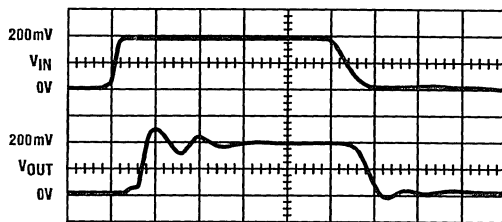
Vertical Scale:  $1V/Div$ . Horizontal Scale:  $5ns/Div$ .



**SMALL SIGNAL RESPONSE**

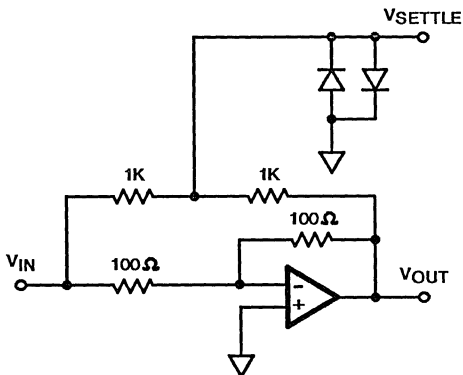
$V_{OUT} = 0$  to  $200mV$

Vertical Scale:  $100mV/Div$ . Horizontal Scale:  $2ns/Div$ .



NOTE: Initial step in output is due to fixture feedthrough

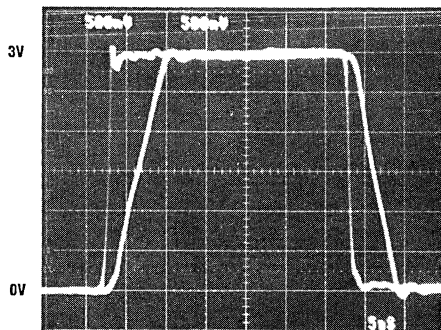
**SETTLING TIME SCHEMATIC**



**PROPAGATION DELAY**

Vertical Scale:  $500mV/Div$ . Horizontal Scale:  $5ns/Div$ .

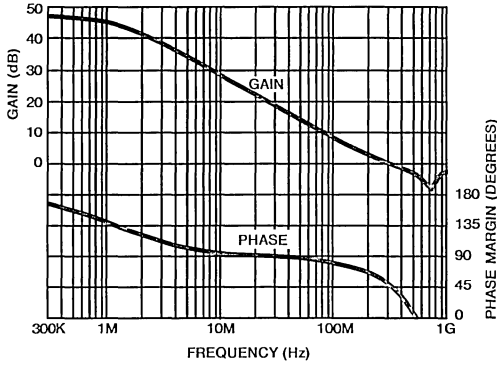
$A_V = +1$ ,  $R_L = 1K$ ,  $V_{OUT} = 0$  to  $3V$



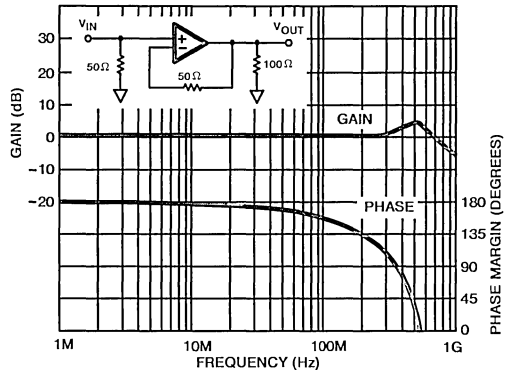
\*NOTE: Test fixture delay of 450ps is included.

Typical Performance Curves  $V_S = \pm 5V$ ,  $T_A = +25^\circ C$ , Unless Otherwise Specified

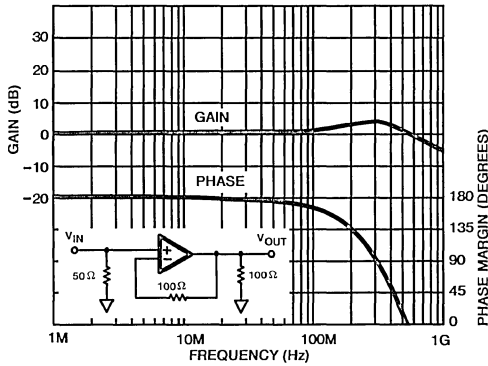
OPEN LOOP GAIN AND PHASE vs FREQUENCY  
 $R_L = 100\Omega$



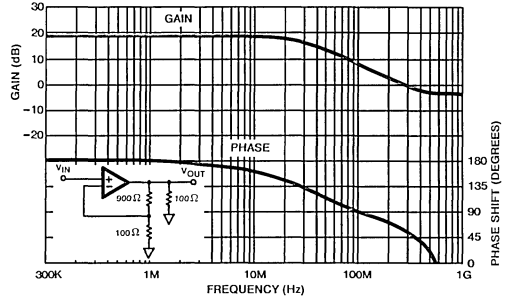
CLOSED LOOP GAIN vs FREQUENCY  
 $A_V = +1$ ,  $R_L = 100$ ,  $R_F = 50\Omega$ ,  $V_{IN} = 70.7mV_{rms}$



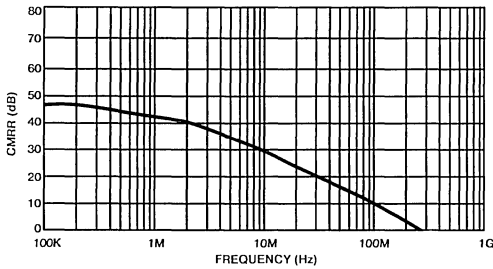
CLOSED LOOP GAIN vs FREQUENCY



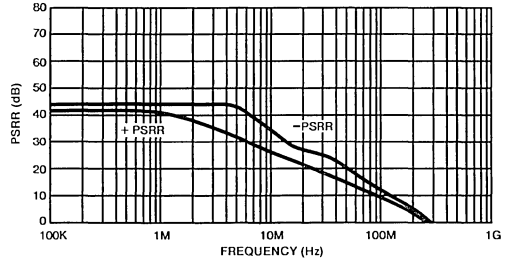
CLOSED LOOP GAIN vs FREQUENCY  
 $A_V = +10$ ,  $R_L = 100\Omega$



CMRR vs FREQUENCY



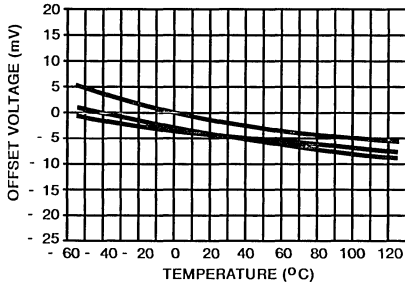
PSRR vs FREQUENCY



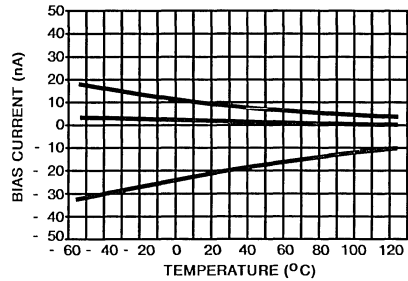

  
 OPERATIONAL AMPLIFIERS

Typical Performance Curves (Continued)  $V_S = \pm 5V$ ,  $T_A = +25^\circ C$ , Unless Otherwise Specified

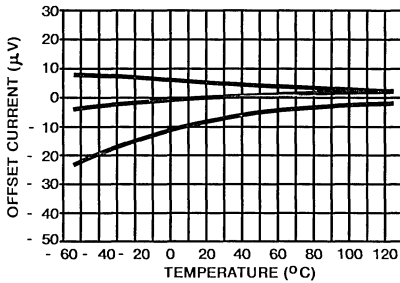
OFFSET VOLTAGE vs TEMPERATURE  
3 Representative Units



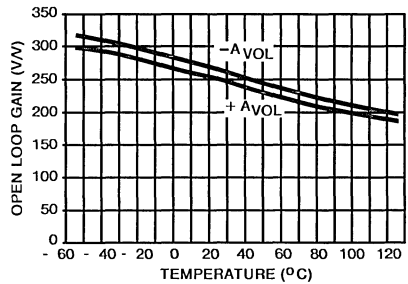
BIAS CURRENT vs TEMPERATURE  
3 Representative Units



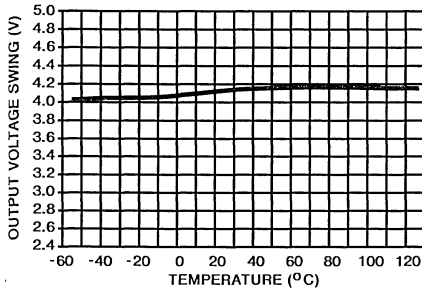
OFFSET CURRENT vs TEMPERATURE  
3 Representative Units



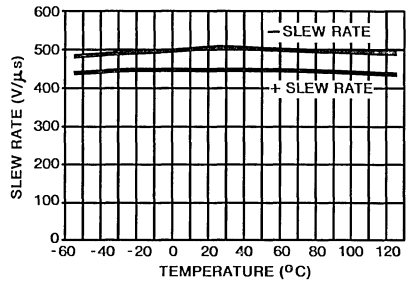
OPEN LOOP GAIN vs TEMPERATURE  
 $R_L = 1K$ ,  $V_{OUT} = 0$  to  $\pm 2V$



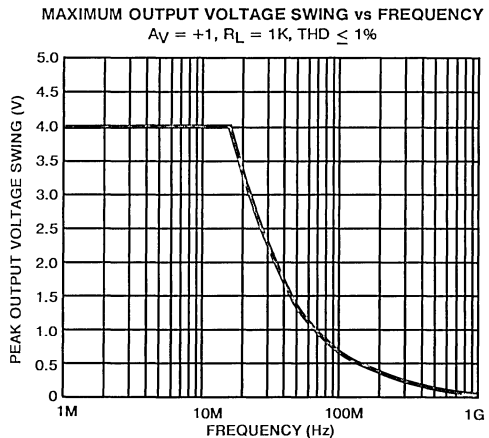
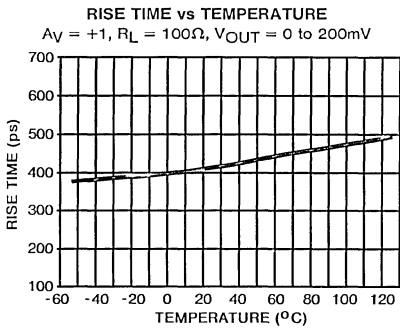
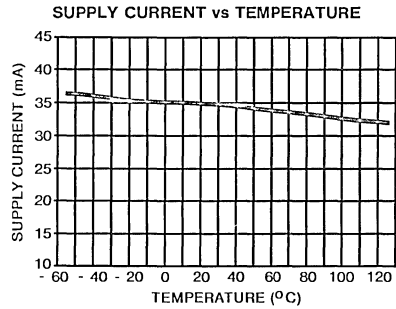
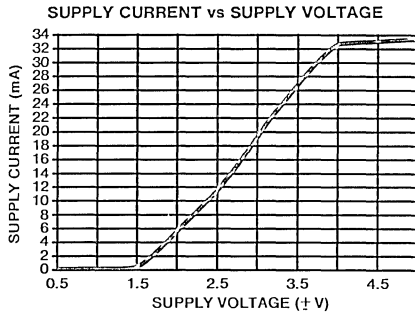
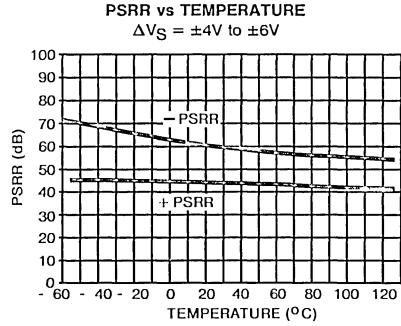
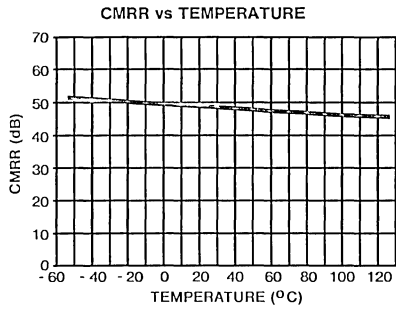
OUTPUT VOLTAGE SWING vs TEMPERATURE  
 $R_L = 1K$



SLEW RATE vs TEMPERATURE  
 $A_V = +1$ ,  $R_L = 100\Omega$ ,  $V_{OUT} = 3V$

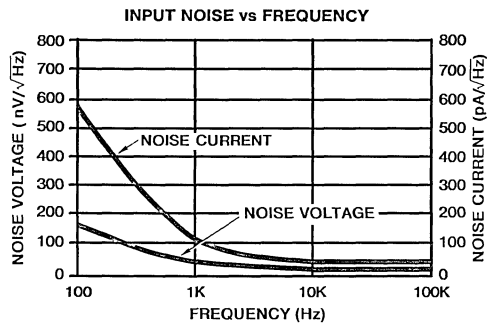
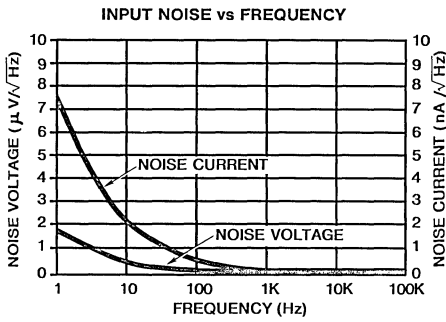
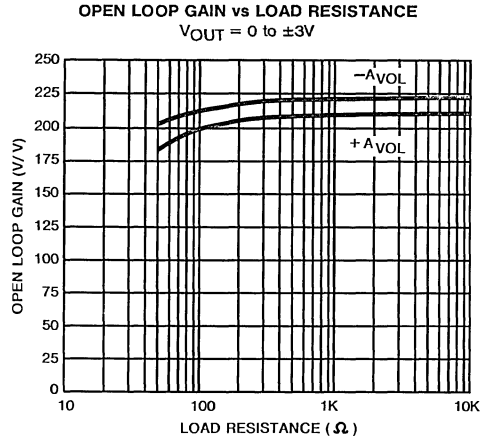
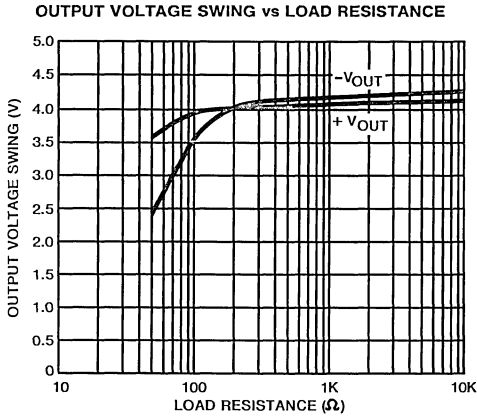


Typical Performance Curves (Continued)  $V_S = \pm 5V$ ,  $T_A = 25^\circ C$ , Unless Otherwise Specified

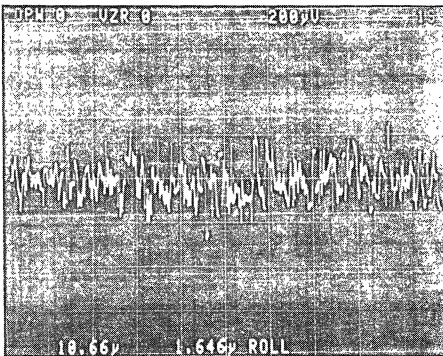


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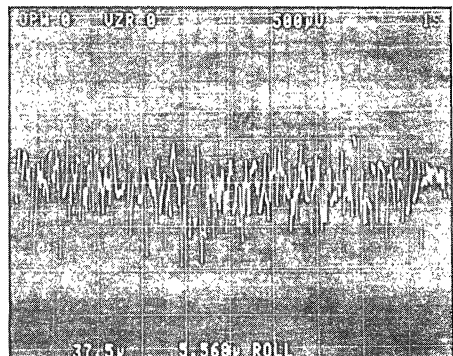
Typical Performance Curves (Continued)  $V_S = \pm 5V$ ,  $T_A = +25^\circ C$ , Unless Otherwise Specified



**INPUT NOISE VOLTAGE**  
 $A_V = 50$ , Noise Voltage =  $1.646\mu V_{rms}$  (RTI)



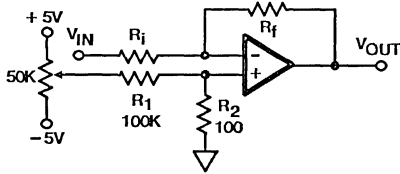
**INPUT NOISE VOLTAGE**  
 $A_V = 50$ , Noise Voltage =  $5.568\mu V_{rms}$  (RTI)



**Applications Information**

**Offset Adjustment**

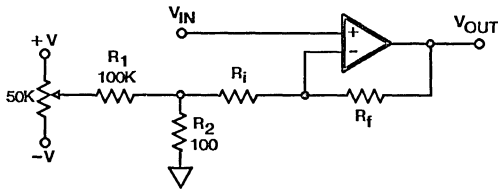
When applications require the offset voltage to be as low as possible, the figure below shows two possible schemes for adjusting offset voltage.



Adjustment Range  $\approx \pm V \left( \frac{R_2}{R_1} \right)$

**FIGURE 1. INVERTING GAIN**

For a voltage follower application, use the circuit in Figure 2 without R2 and with Ri shorted. R1 should be 1MV to 10MV. the adjustment resistors will cause only a very small gain error.



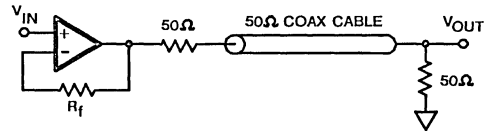
Adjustment Range  $\approx \pm V \left( \frac{R_2}{R_1} \right)$       Gain  $\approx 1 + \left( \frac{R_f}{R_1 + R_2} \right)$

**FIGURE 2. NON-INVERTING GAIN**

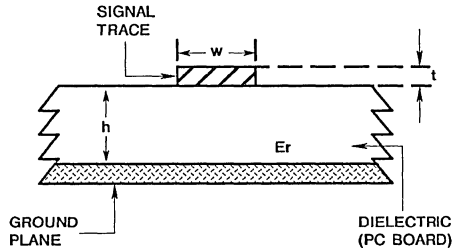
**PC Board Layout Guidelines**

When designing with the HFA-0005, good high frequency (RF) techniques should be used when making a PC board. A massive ground plane should be used to maintain a low impedance ground. Proper shielding and use of short interconnection leads are also very important.

To achieve maximum high frequency performance, the use of low impedance transmission lines with impedance matching is recommended: 50Ω lines are common in communications and 75Ω lines in video systems. Impedance matching is important to minimize reflected energy therefore minimizing transmitted signal distortion. This is accomplished by using a series matching resistor (50 or 75Ω), matched transmission line (50 or 75Ω), and a matched terminating resistor, as shown in the figure below. Note that there will be a 6dB loss from input to output. The HFA-0005 has an integral 50Ω resistor connected to the op amps output with the other end of the resistor pinned out. This 50Ω resistor can be used as the series resistor instead of an external resistor.



PC board traces can be made to look like a 50 or 75Ω transmission line, called microstrip. Microstrip is a PC board trace with a ground plane directly beneath, on the opposite side of the board, as shown below.





**Applications Information (Continued)**

When manufacturing pc boards the trace width can be calculated based on a number of variables.

The following equation is reasonably accurate for calculating the proper trace width for a 50Ω transmission line.

$$Z_0 = \frac{87}{\sqrt{E_r + 1.41}} \ln \left( \frac{5.98h}{0.8w + t} \right) \Omega$$

Power supply decoupling is essential for high frequency op amps. A 0.01μf high quality ceramic capacitor at each supply pin in parallel with a 1μf tantalum capacitor will provide excellent decoupling. Chip capacitors produce the best results due to ease of placement next to the op amp and they have negligible lead inductance. If leaded capacitors are used, the leads should be kept as short as possible to minimize lead inductance. The figures below illustrate two different decoupling schemes. Figure 4 improves the PSRR because the resistor and capacitors create low pass filters. Note that the supply current will create a voltage drop across the resistor.

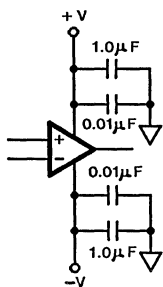


FIGURE 3.

**Saturation Recovery**

When an op amp is over driven output devices can saturate and sometimes take a long time to recover. By clamping the input to safe levels, output saturation can be avoided. If output saturation cannot be avoided, the recovery time from 25% over-drive is 20ns and 30ns from 50% over-drive.

**Thermal Constants (°C/W)**

|                       | θ <sub>ja</sub> | θ <sub>jc</sub> |
|-----------------------|-----------------|-----------------|
| HFA2-0005-5/-9 .....  | 120             | 37              |
| HFA3-0005-5 .....     | 98              | 36              |
| HFA7-0005-5/-9 .....  | 75              | 13              |
| HFA9P-0005-5/-9 ..... | 158             | 43              |

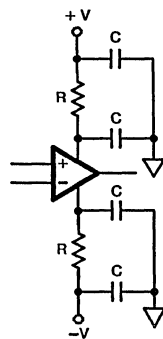


FIGURE 4.

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### Features

- Wide Operating Voltage Range  $\pm 1V$  to  $\pm 8V$
- High Input Impedance -  $10^{12}\Omega$
- Programmable Power Consumption - Low as  $20\mu W$
- Input Current Lower Than BIFETs - Typ  $1pA$
- Available as Singles, Duals, and Quads
- Output Voltage Swings to Within Millivolts of  $V_-$  and  $V_+$
- Low Power Replacement for Many Standard Op Amps
- Compensated and Uncompensated Versions
- Input Common Mode Voltage Range Greater Than Supply Rails (ICL7612)

### Description

The ICL761X/762X/764X series is a family of monolithic CMOS operational amplifiers. These devices provide the designer with high performance operation at low supply voltages and selectable quiescent currents, and are an ideal design tool when ultra low input current and low power dissipation are desired.

The basic amplifier will operate at supply voltages ranging from  $\pm 1V$  to  $\pm 8V$ , and may be operated from a single Lithium cell.

A unique quiescent current programming pin allows setting of standby current to  $1mA$ ,  $100\mu A$ , or  $10\mu A$ , with no external components. This results in power consumption as low as  $20\mu W$ . Output swings range to within a few millivolts of the supply voltages.

### Applications

- Portable Instruments
- Telephone Headsets
- Hearing Aid/Microphone Amplifiers
- Meter Amplifiers
- Medical Instruments
- High Impedance Buffers

Of particular significance is the extremely low ( $1pA$ ) input current, input noise current of  $.01pA/\sqrt{Hz}$ , and  $10^{12}\Omega$  input impedance. These features optimize performance in very high source impedance applications.

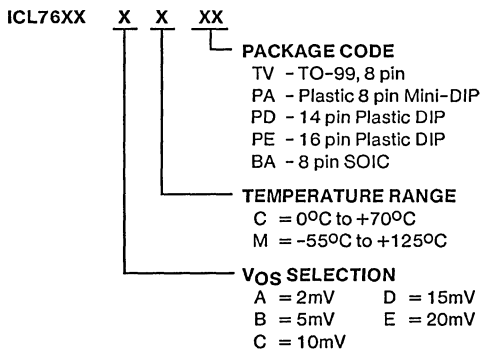
The inputs are internally protected. Outputs are fully protected against short circuits to ground or to either supply.

AC performance is excellent, with a slew rate of  $1.6V/\mu s$ , and unity gain bandwidth of  $1MHz$  at  $I_Q = 1mA$ .

Because of the low power dissipation, operating temperatures and drift are quite low. Applications utilizing these features may include stable instruments, extended life designs, or high density packages.

### Selection Guide

#### DEVICE NOMENCLATURE



#### SPECIAL FEATURE CODES

- C = Internally Compensated
- H = High Quiescent Current ( $1mA$ )
- L = Low Quiescent Current ( $10\mu A$ )
- M = Medium Quiescent Current ( $100\mu A$ )
- O = Offset Null Capability
- P = Programmable Quiescent Current
- V = Extended CMVR

3  
OPERATIONAL  
AMPLIFIERS

## ORDERING INFORMATION

| Basic Part Number  | Number of OP-AMPS in Package, and Special Features (SEE CODES) | Package Type and Suffix |                      |                      |                |                 |
|--------------------|--|-------------------------|----------------------|----------------------|----------------|-----------------|
|                    |  | 8-Lead TO-99            |                      | 8-Pin MINIDIP        | 8-Pin SOIC     | Plastic DIP (1) |
|                    |  | 0°C to +70°C            | -55°C to +125°C      | 0°C to +70°C         | 0°C to +70°C   | 0°C to +70°C    |
| ICL7611<br>ICL7612 | SINGLE OP-AMP:<br>C, O, P<br>C, O, P, V                        | ACTV<br>BCTV<br>DCTV    | AMTV<br>BMTV<br>DMTV | ACPA<br>BCPA<br>DCPA | DCBA-T<br>DCBA |                 |
| ICL7621            | DUAL OP-AMP:<br>C, M   | ACTV<br>BCTV<br>DCTV    | AMTV<br>BMTV<br>DMTV | ACPA<br>BCPA<br>DCPA | DCBA<br>DCBA-T |                 |
| ICL7641<br>ICL7642 | QUAD OP-AMP:<br>C, H<br>C, L                                   |                         |                      |                      |                | CCPD<br>ECPD    |

NOTES: 1. Quads are only available in 14 pin DIP package.  
2. Ordering code must consist of basic part number and package suffix, e.g., ICL7611BCPA.

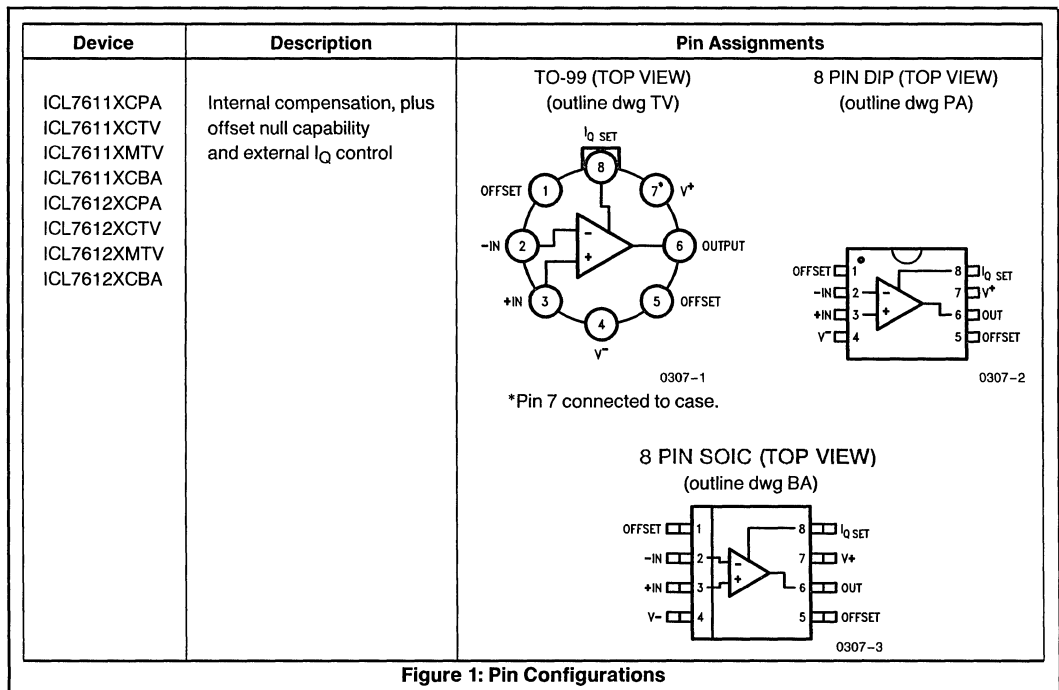


Figure 1: Pin Configurations

NOTE: All typical values have been characterized but are not tested.

# ICL76XX

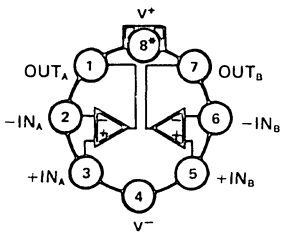
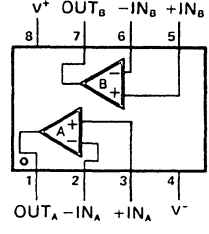
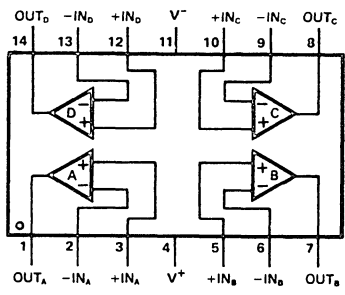
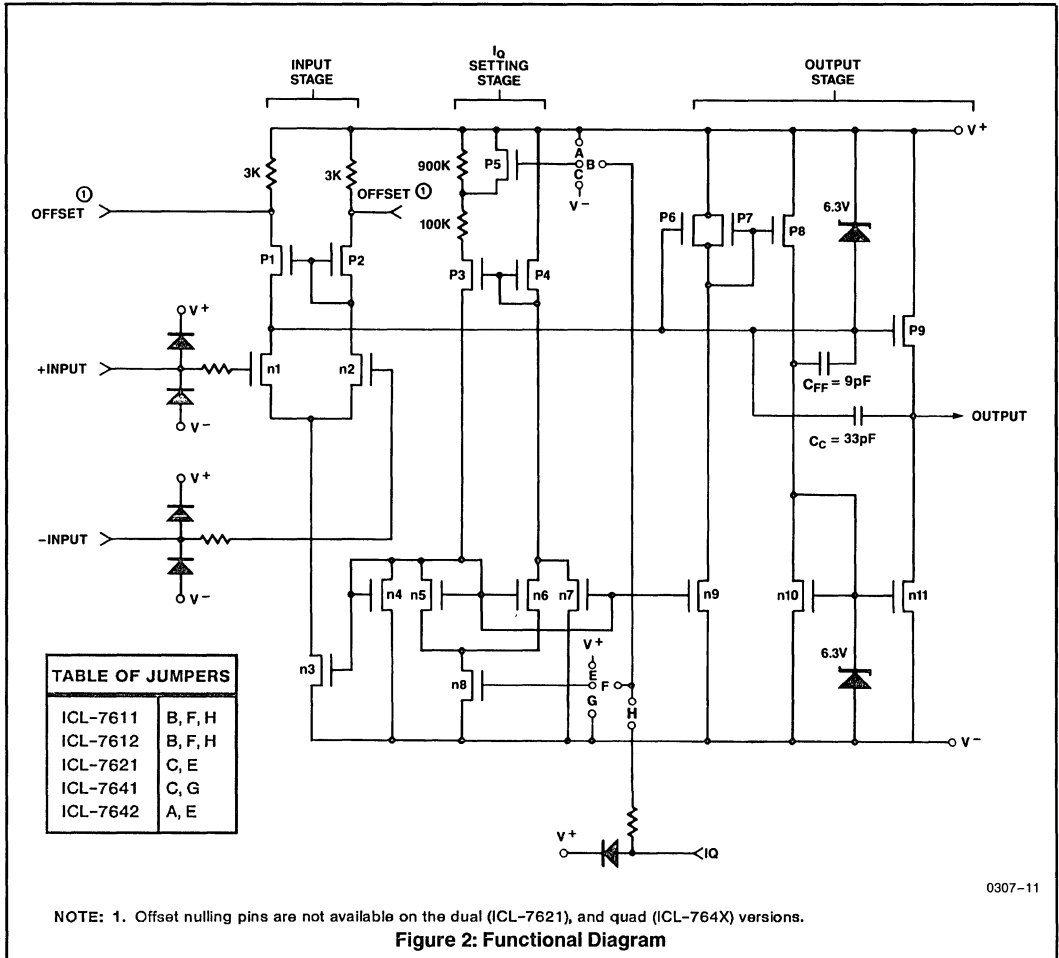
| Device   | Description   | Pin Assignments   |   |
|--|---|---|---|
| ICL7621XCPA<br>ICL7621XCTV<br>ICL7621XMTV<br>ICL7621XCBA | Dual op amps with internal compensation; $I_Q$ fixed at $100\mu A$<br>Pin compatible with Texas Inst. TL082<br>Motorola MC1458<br>Raytheon RC4558   | <p>TO-99 (TOP VIEW)<br/>(outline dwg TV)</p>  <p>0307-6</p> <p>*Pin 8 connected to case.</p> | <p>8 PIN DIP (TOP VIEW)<br/>(outline dwg PA)</p>  <p>0307-7</p> |
| ICL7641XCPD<br>ICL7642XCPD                               | Quad op amps with internal compensation.<br>$I_Q$ fixed at 1mA (ICL7641)<br>$I_Q$ fixed at $10\mu A$ (ICL7642)<br>Pin compatible with Texas Instr. TL084<br>National LM324<br>Harris HA4741 | <p>14 PIN DIP (TOP VIEW)<br/>(outline dwg PD)</p>  <p>0307-10</p>                            |   |

Figure 1: Pin Configurations (Cont.)

  
 OPERATIONAL AMPLIFIERS

NOTE: All typical values have been characterized but are not tested.

# ICL76XX



NOTE: All typical values have been characterized but are not tested.

# ICL76XX

## ABSOLUTE MAXIMUM RATINGS

|   |                                    |
|---|------------------------------------|
| Total Supply Voltage $V^+$ to $V^-$ .....             | 18V                                |
| Input Voltage .....                                   | $V^- - 0.3$ to $V^+ + 0.3$ V       |
| Differential Input Voltage <sup>[1]</sup> .....       | $\pm[(V^+ + 0.3) - (V^- - 0.3)]$ V |
| Duration of Output Short Circuit <sup>[2]</sup> ..... | Unlimited                          |

## Continuous Power Dissipation

|                 |       |                  |
|-----------------|-------|------------------|
|                 | @25°C | Above 25°C       |
|                 |       | derate as below: |
| TO-99           | 250mW | 2mW/°C           |
| 8 Lead Minidip  | 250mW | 2mW/°C           |
| 14 Lead Plastic | 375mW | 3mW/°C           |
| 14 Lead Cerdip  | 500mW | 4mW/°C           |

|   |                 |
|---|-----------------|
| Storage Temperature Range .....           | -65°C to +150°C |
| Operating Temperature Range               |                 |
| ICL76XXM .....                            | -55°C to +125°C |
| ICL76XXC .....                            | 0°C to +70°C    |
| Lead Temperature (Soldering, 10sec) ..... | 300°C           |

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

- NOTE 1.** Long term offset voltage stability will be degraded if large input differential voltages are applied for long periods of time.  
**NOTE 2.** The outputs may be shorted to ground or to either supply, for  $V_{SUPP} \leq 10$ V. Care must be taken to insure that the dissipation rating is not exceeded.

## ELECTRICAL CHARACTERISTICS (7611/12 and 7621 ONLY)

( $V_{SUPPLY} = \pm 5.0$ V,  $T_A = 25^\circ$ C, unless otherwise specified.)

| Symbol                   | Parameter   | Test Conditions  | 76XXA   |     |                   | 76XXB   |     |                   | 76XXD   |     |                   | Units      |
|--------------------------|---|--|---|-----|-------------------|---|-----|-------------------|---|-----|-------------------|------------|
|                          |   |  | Min   | Typ | Max               | Min   | Typ | Max               | Min   | Typ | Max               |            |
| $V_{OS}$                 | Input Offset Voltage                                    | $R_S \leq 100k\Omega$ , $T_A = 25^\circ$ C<br>$T_{MIN} \leq T_A \leq T_{MAX}$  |   |     | 2<br>3            |   |     | 5<br>7            |   |     | 15<br>20          | mV         |
| $\Delta V_{OS}/\Delta T$ | Temperature Coefficient of $V_{OS}$                     | $R_S \leq 100k\Omega$  |   | 10  |                   |   | 15  |                   |   | 25  |                   | $\mu$ V/°C |
| $I_{OS}$                 | Input Offset Current                                    | $T_A = 25^\circ$ C<br>$\Delta T_A = C_{(2)}$<br>$\Delta T_A = M_{(2)}$   |   | 0.5 | 30<br>300<br>800  |   | 0.5 | 30<br>300<br>800  |   | 0.5 | 30<br>300<br>800  | pA         |
| $I_{BIAS}$               | Input Bias Current                                      | $T_A = 25^\circ$ C<br>$\Delta T_A = C$<br>$\Delta T_A = M$   |   | 1.0 | 50<br>400<br>4000 |   | 1.0 | 50<br>400<br>4000 |   | 1.0 | 50<br>400<br>4000 | pA         |
| $V_{CMR}$                | Common Mode Voltage Range<br>(Except ICL7612)           | $I_Q = 10\mu$ A <sup>(1)</sup><br>$I_Q = 100\mu$ A<br>$I_Q = 1$ mA <sup>(1)</sup>  | $\pm 4.4$<br>$\pm 4.2$<br>$\pm 3.7$   |     |                   | $\pm 4.4$<br>$\pm 4.2$<br>$\pm 3.7$   |     |                   | $\pm 4.4$<br>$\pm 4.2$<br>$\pm 3.7$   |     |                   | V          |
| $V_{CMR}$                | Extended Common Mode<br>Voltage Range<br>(ICL7612 Only) | $I_Q = 10\mu$ A<br>$I_Q = 100\mu$ A<br>$I_Q = 1$ mA  | $\pm 5.3$<br>$+ 5.3$<br>$- 5.1$<br>$+ 5.3$<br>$- 4.5$   |     |                   | $\pm 5.3$<br>$+ 5.3$<br>$- 5.1$<br>$+ 5.3$<br>$- 4.5$   |     |                   | $\pm 5.3$<br>$+ 5.3$<br>$- 5.1$<br>$+ 5.3$<br>$- 4.5$   |     |                   | V          |
| $V_{OUT}$                | Output Voltage Swing                                    | (1) $I_Q = 10\mu$ A, $R_L = 1M\Omega$<br>$T_A = 25^\circ$ C<br>$\Delta T_A = C$<br>$\Delta T_A = M$<br>$I_Q = 100\mu$ A, $R_L = 100k\Omega$<br>$T_A = 25^\circ$ C<br>$\Delta T_A = C$<br>$\Delta T_A = M$<br>(1) $I_Q = 1$ mA, $R_L = 10k\Omega$<br>$T_A = 25^\circ$ C<br>$\Delta T_A = C$<br>$\Delta T_A = M$ | $\pm 4.9$<br>$\pm 4.8$<br>$\pm 4.7$<br>$\pm 4.9$<br>$\pm 4.8$<br>$\pm 4.5$<br>$\pm 4.5$<br>$\pm 4.3$<br>$\pm 4.0$ |     |                   | $\pm 4.9$<br>$\pm 4.8$<br>$\pm 4.7$<br>$\pm 4.9$<br>$\pm 4.8$<br>$\pm 4.5$<br>$\pm 4.5$<br>$\pm 4.3$<br>$\pm 4.0$ |     |                   | $\pm 4.9$<br>$\pm 4.8$<br>$\pm 4.7$<br>$\pm 4.9$<br>$\pm 4.8$<br>$\pm 4.5$<br>$\pm 4.5$<br>$\pm 4.3$<br>$\pm 4.0$ |     |                   | V          |

NOTE: All typical values have been characterized but are not tested.

# ICL76XX

## ELECTRICAL CHARACTERISTICS (7611/12 and 7621 ONLY) (Continued)

( $V_{SUPPLY} = \pm 5.0V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.)

| Symbol                           | Parameter   | Test Conditions   | 76XXA              |                      |     | 76XXB                |                     |                      | 76XXD              |                     |                 | Units      |
|----------------------------------|---|---|--------------------|----------------------|-----|----------------------|---------------------|----------------------|--------------------|---------------------|-----------------|------------|
|                                  |   |   | Min                | Typ                  | Max | Min                  | Typ                 | Max                  | Min                | Typ                 | Max             |            |
| A <sub>VOL</sub>                 | Large Signal Voltage Gain   | $V_O = \pm 4.0V$ , $R_L = 1M\Omega$<br>$I_Q = 10\mu A^{(1)}$ , $T_A = 25^\circ C$<br>$\Delta T_A = C$<br>$\Delta T_A = M$               | 86<br>80<br>74     | 104                  |     | 80<br>75<br>68       | 104                 |                      | 80<br>75<br>68     | 104                 |                 | dB         |
|                                  |   | $V_O = \pm 4.0V$ , $R_L = 100k\Omega$<br>$I_Q = 100\mu A$ , $T_A = 25^\circ C$<br>$\Delta T_A = C$<br>$\Delta T_A = M$                  | 86<br>80<br>74     | 102                  |     | 80<br>75<br>68       | 102                 |                      | 80<br>75<br>68     | 102                 |                 |            |
|                                  |   | $V_O = \pm 4.0V$ , $R_L = 10k\Omega$<br>$I_Q = 1mA^{(1)}$ , $T_A = 25^\circ C$<br>$\Delta T_A = C$<br>$\Delta T_A = M$                  | 80<br>76<br>72     | 83                   |     | 76<br>72<br>68       | 83                  |                      | 76<br>72<br>68     | 83                  |                 |            |
| GBW                              | Unity Gain Bandwidth  | $I_Q = 10\mu A^{(1)}$<br>$I_Q = 100\mu A$<br>$I_Q = 1mA^{(1)}$  |                    | 0.044<br>0.48<br>1.4 |     | 0.044<br>0.48<br>1.4 |                     | 0.044<br>0.48<br>1.4 |                    |                     | MHz             |            |
| R <sub>IN</sub>                  | Input Resistance  |   |                    | 10 <sup>12</sup>     |     | 10 <sup>12</sup>     |                     | 10 <sup>12</sup>     |                    |                     | $\Omega$        |            |
| CMRR                             | Common Mode Rejection Ratio                                       | $R_S \leq 100k\Omega$ , $I_Q = 10\mu A^{(1)}$   | 76                 | 96                   |     | 70                   | 96                  |                      | 70                 | 96                  |                 | dB         |
|                                  |   | $R_S \leq 100k\Omega$ , $I_Q = 100\mu A$  | 76                 | 91                   |     | 70                   | 91                  |                      | 70                 | 91                  |                 |            |
|                                  |   | $R_S \leq 100k\Omega$ , $I_Q = 1mA^{(1)}$   | 66                 | 87                   |     | 60                   | 87                  |                      | 60                 | 87                  |                 |            |
| PSRR                             | Power Supply Rejection Ratio<br>$V_{SUPPLY} = \pm 8V$ to $\pm 2V$ | $R_S \leq 100k\Omega$ , $I_Q = 10\mu A^{(1)}$   | 80                 | 94                   |     | 80                   | 94                  |                      | 80                 | 94                  |                 | dB         |
|                                  |   | $R_S \leq 100k\Omega$ , $I_Q = 100\mu A$  | 80                 | 86                   |     | 80                   | 86                  |                      | 80                 | 86                  |                 |            |
|                                  |   | $R_S \leq 100k\Omega$ , $I_Q = 1mA^{(1)}$   | 70                 | 77                   |     | 70                   | 77                  |                      | 70                 | 77                  |                 |            |
| e <sub>n</sub>                   | Input Referred Noise Voltage                                      | $R_S = 100\Omega$ , $f = 1kHz$  |                    | 100                  |     | 100                  |                     | 100                  |                    |                     | nV/ $\sqrt{Hz}$ |            |
| i <sub>n</sub>                   | Input Referred Noise Current                                      | $R_S = 100\Omega$ , $f = 1kHz$  |                    | 0.01                 |     | 0.01                 |                     | 0.01                 |                    |                     | pA/ $\sqrt{Hz}$ |            |
| I <sub>SUPPLY</sub>              | Supply Current<br>(Per Amplifier)                                 | No Signal, No Load<br>$I_Q$ SET = +5V <sup>(1)</sup> Low Bias<br>$I_Q$ SET = 0V Medium Bias<br>$I_Q$ SET = -5V <sup>(1)</sup> High Bias | 0.01<br>0.1<br>1.0 | 0.02<br>0.25<br>2.5  |     | 0.01<br>0.1<br>1.0   | 0.02<br>0.25<br>2.5 |                      | 0.01<br>0.1<br>1.0 | 0.02<br>0.25<br>2.5 | mA              |            |
| V <sub>O1</sub> /V <sub>O2</sub> | Channel Separation  | $A_V = 100$   |                    | 120                  |     | 120                  |                     | 120                  |                    |                     | dB              |            |
| SR                               | Slew Rate   | $A_V = 1$ , $C_L = 100pF$<br>$V_{IN} = 8V_{p-p}$<br>$I_Q = 10\mu A^{(1)}$ , $R_L = 1M\Omega$  |                    | 0.016                |     |                      | 0.016               |                      |                    | 0.016               |                 | V/ $\mu s$ |
|                                  |   | $I_Q = 100\mu A$ , $R_L = 100k\Omega$   |                    | 0.16                 |     |                      | 0.16                |                      |                    | 0.16                |                 |            |
|                                  |   | $I_Q = 1mA^{(1)}$ , $R_L = 10k\Omega$   |                    | 1.6                  |     |                      | 1.6                 |                      |                    | 1.6                 |                 |            |
| t <sub>r</sub>                   | Rise Time   | $V_{IN} = 50mV$ , $C_L = 100pF$<br>$I_Q = 10\mu A^{(1)}$ , $R_L = 1M\Omega$   |                    | 20                   |     |                      | 20                  |                      |                    | 20                  |                 | $\mu s$    |
|                                  |   | $I_Q = 100\mu A$ , $R_L = 100k\Omega$   |                    | 2                    |     |                      | 2                   |                      |                    | 2                   |                 |            |
|                                  |   | $I_Q = 1mA^{(1)}$ , $R_L = 10k\Omega$   |                    | 0.9                  |     |                      | 0.9                 |                      |                    | 0.9                 |                 |            |
|                                  | Overshoot Factor  | $V_{IN} = 50mV$ , $C_L = 100pF$<br>$I_Q = 10\mu A^1$ , $R_L = 1M\Omega$   |                    | 5                    |     |                      | 5                   |                      |                    | 5                   |                 | %          |
|                                  |   | $I_Q = 100\mu A$ , $R_L = 100k\Omega$   |                    | 10                   |     |                      | 10                  |                      |                    | 10                  |                 |            |
|                                  |   | $I_Q = 1mA^1$ , $R_L = 10k\Omega$   |                    | 40                   |     |                      | 40                  |                      |                    | 40                  |                 |            |

NOTES: 1. ICL7611, 7612 only.

2. C = Commercial Temperature Range: 0°C to +70°C  
M = Military Temperature Range: -55°C to +125°C

NOTE: All typical values have been characterized but are not tested.

# ICL76XX

## ELECTRICAL CHARACTERISTICS (7611/12 A AND B GRADES ONLY)

( $V_{SUPPLY} = \pm 1.0V$ ,  $I_Q = 10\mu A$ ,  $T_A = 25^\circ C$ , unless otherwise specified.)

| Symbol                   | Parameter   | Test Conditions   | 76XXA              |                          |           | 76XXB              |                          |           | Units            |
|--------------------------|---|---|--------------------|--------------------------|-----------|--------------------|--------------------------|-----------|------------------|
|                          |   |   | Min                | Typ                      | Max       | Min                | Typ                      | Max       |                  |
| $V_{OS}$                 | Input Offset Voltage                              | $R_S \leq 100k\Omega$ , $T_A = 25^\circ C$<br>$T_{MIN} \leq T_A \leq T_{MAX}$ |                    |                          | 2<br>3    |                    |                          | 5<br>7    | mV               |
| $\Delta V_{OS}/\Delta T$ | Temperature Coefficient of $V_{OS}$               | $R_S \leq 100k\Omega$   |                    | 10                       |           |                    | 15                       |           | $\mu V/^\circ C$ |
| $I_{OS}$                 | Input Offset Current                              | $T_A = 25^\circ C$<br>$\Delta T_A = C$  |                    | 0.5                      | 30<br>300 |                    | 0.5                      | 30<br>300 | pA               |
| $I_{BIAS}$               | Input Bias Current                                | $T_A = 25^\circ C$<br>$\Delta T_A = C$  |                    | 1.0                      | 50<br>500 |                    | 1.0                      | 50<br>500 | pA               |
| $V_{CMR}$                | Common Mode Voltage Range<br>(Except ICL7612)     |   | $\pm 0.6$          |                          |           | $\pm 0.6$          |                          |           | V                |
| $V_{CMR}$                | Extended Common Mode Voltage Range (ICL7612 Only) |   | +0.6<br>to<br>-1.1 |                          |           | +0.6<br>to<br>-1.1 |                          |           | V                |
| $V_{OUT}$                | Output Voltage Swing                              | $R_L = 1M\Omega$ , $T_A = 25^\circ C$<br>$\Delta T_A = C$                     |                    | $\pm 0.98$<br>$\pm 0.96$ |           |                    | $\pm 0.98$<br>$\pm 0.96$ |           | V                |
| $A_{VOL}$                | Large Signal Voltage Gain                         | $V_O = \pm 0.1V$ , $R_L = 1M\Omega$<br>$T_A = 25^\circ C$<br>$\Delta T_A = C$ |                    | 90<br>80                 |           |                    | 90<br>80                 |           | dB               |
| GBW                      | Unity Gain Bandwidth                              |   |                    | 0.044                    |           |                    |                          |           | MHz              |
| $R_{IN}$                 | Input Resistance                                  |   |                    | $10^{12}$                |           |                    | $10^{12}$                |           | $\Omega$         |
| CMRR                     | Common Mode Rejection Ratio                       | $R_S \leq 100k\Omega$   |                    | 80                       |           |                    | 80                       |           | dB               |
| PSRR                     | Power Supply Rejection Ratio                      | $R_S \leq 100k\Omega$   |                    | 80                       |           |                    | 80                       |           | dB               |
| $e_n$                    | Input Referred Noise Voltage                      | $R_S = 100\Omega$ , $f = 1kHz$  |                    | 100                      |           |                    | 100                      |           | $nV/\sqrt{Hz}$   |
| $i_n$                    | Input Referred Noise Current                      | $R_S = 100\Omega$ , $f = 1kHz$  |                    | 0.01                     |           |                    | 0.01                     |           | $pA/\sqrt{Hz}$   |
| $I_{SUPPLY}$             | Supply Current<br>(Per Amplifier)                 | No Signal, No Load  |                    | 6                        | 15        |                    | 6                        | 15        | $\mu A$          |
| SR                       | Slew Rate   | $A_V = 1$ , $C_L = 100pF$<br>$V_{IN} = 0.2V_{p-p}$<br>$R_L = 1M\Omega$        |                    | 0.016                    |           |                    | 0.016                    |           | $V/\mu s$        |
| $t_r$                    | Rise Time   | $V_{IN} = 50mV$ , $C_L = 100pF$<br>$R_L = 1M\Omega$                           |                    | 20                       |           |                    | 20                       |           | $\mu s$          |
|                          | Overshoot Factor                                  | $V_{IN} = 50mV$ , $C_L = 100pF$<br>$R_L = 1M\Omega$                           |                    | 5                        |           |                    | 5                        |           | %                |

NOTE: C= Commercial Temperature Range (0°C to +70°C) M= Military Temperature Range (-55°C to +125°C).

NOTE: All typical values have been characterized but are not tested.



## ELECTRICAL CHARACTERISTICS (7641/42 ONLY)

(V<sub>SUPPLY</sub> = ±5.0V, T<sub>A</sub> = 25°C, unless otherwise specified.)

| Symbol               | Parameter                                  | Test Conditions  | 76XXC (6)            |                      |                   | 76XXE (6)            |                      |                   | Units |
|----------------------|--|--|----------------------|----------------------|-------------------|----------------------|----------------------|-------------------|-------|
|                      |  |  | Min                  | Typ                  | Max               | Min                  | Typ                  | Max               |       |
| V <sub>OS</sub>      | Input Offset Voltage                       | R <sub>S</sub> ≤ 100kΩ, T <sub>A</sub> = 25°C<br>T <sub>MIN</sub> ≤ T <sub>A</sub> ≤ T <sub>MAX</sub>  |                      |                      | 10<br>15          |                      |                      | 20<br>25          | mV    |
| ΔV <sub>OS</sub> /ΔT | Temperature Coefficient of V <sub>OS</sub> | R <sub>S</sub> ≤ 100kΩ (Note 5)  |                      | 20                   |                   |                      | 30                   |                   | μV/°C |
| I <sub>OS</sub>      | Input Offset Current                       | T <sub>A</sub> = 25°C<br>ΔT <sub>A</sub> = C<br>ΔT <sub>A</sub> = M  |                      | 0.5                  | 30<br>300<br>800  |                      | 0.5                  | 30<br>300<br>800  | pA    |
| I <sub>BIAS</sub>    | Input Bias Current                         | T <sub>A</sub> = 25°C<br>ΔT <sub>A</sub> = C<br>ΔT <sub>A</sub> = M  |                      | 1.0                  | 50<br>500<br>4000 |                      | 1.0                  | 50<br>500<br>4000 | pA    |
| V <sub>CMR</sub>     | Common Mode Voltage Range                  | I <sub>Q</sub> = 10μA <sup>(1)</sup><br>I <sub>Q</sub> = 100μA <sup>(3)</sup><br>I <sub>Q</sub> = 1mA <sup>(2)</sup>   | ±4.4<br>±4.2<br>±3.7 |                      |                   | ±4.4<br>±4.2<br>±3.7 |                      |                   | V     |
| V <sub>OUT</sub>     | Output Voltage Swing                       | I <sub>Q</sub> = 10μA <sup>(1)</sup> , R <sub>L</sub> = 1MΩ<br>T <sub>A</sub> = 25°C<br>ΔT <sub>A</sub> = C<br>ΔT <sub>A</sub> = M   | ±4.9<br>±4.8<br>±4.7 |                      |                   | ±4.9<br>±4.8<br>±4.7 |                      |                   | V     |
|                      |  | I <sub>Q</sub> = 100μA <sup>(3)</sup> , R <sub>L</sub> = 100kΩ<br>T <sub>A</sub> = 25°C<br>ΔT <sub>A</sub> = C<br>ΔT <sub>A</sub> = M  | ±4.9<br>±4.8<br>±4.5 |                      |                   | ±4.9<br>±4.8<br>±4.5 |                      |                   |       |
|                      |  | I <sub>Q</sub> = 1mA <sup>(2)</sup> , R <sub>L</sub> = 10kΩ<br>T <sub>A</sub> = 25°C<br>ΔT <sub>A</sub> = C<br>ΔT <sub>A</sub> = M   | ±4.5<br>±4.3<br>±4.0 |                      |                   | ±4.5<br>±4.3<br>±4.0 |                      |                   |       |
| A <sub>VOL</sub>     | Large Signal Voltage Gain                  | V <sub>O</sub> = ±4.0V, R <sub>L</sub> = 1MΩ <sup>(1)</sup><br>I <sub>Q</sub> = 10μA <sup>(1)</sup> , T <sub>A</sub> = 25°C<br>ΔT <sub>A</sub> = C<br>ΔT <sub>A</sub> = M    | 80<br>75<br>68       | 104                  |                   | 80<br>75<br>68       | 104                  |                   | dB    |
|                      |  | V <sub>O</sub> = ±4.0V, R <sub>L</sub> = 100kΩ <sup>(3)</sup><br>I <sub>Q</sub> = 100μA <sup>(3)</sup> , T <sub>A</sub> = 25°C<br>ΔT <sub>A</sub> = C<br>ΔT <sub>A</sub> = M | 80<br>75<br>68       | 102                  |                   | 80<br>75<br>68       | 102                  |                   |       |
|                      |  | V <sub>O</sub> = ±4.0V, R <sub>L</sub> = 10kΩ <sup>(2)</sup><br>I <sub>Q</sub> = 1mA <sup>(2)</sup> , T <sub>A</sub> = 25°C<br>ΔT <sub>A</sub> = C<br>ΔT <sub>A</sub> = M    | 76<br>72<br>68       | 98                   |                   | 76<br>72<br>68       | 98                   |                   |       |
| GBW                  | Unity Gain Bandwidth                       | I <sub>Q</sub> = 10μA <sup>(1)</sup><br>I <sub>Q</sub> = 100μA <sup>(3)</sup><br>I <sub>Q</sub> = 1mA <sup>(2)</sup>   |                      | 0.044<br>0.48<br>1.4 |                   |                      | 0.044<br>0.48<br>1.4 |                   | MHz   |
| R <sub>IN</sub>      | Input Resistance                           |  |                      | 10 <sup>12</sup>     |                   |                      | 10 <sup>12</sup>     |                   | Ω     |
| CMRR                 | Common Mode Rejection Ratio                | R <sub>S</sub> ≤ 100kΩ, I <sub>Q</sub> = 10μA <sup>(1)</sup>   | 70                   | 96                   |                   | 70                   | 96                   |                   | dB    |
|                      |  | R <sub>S</sub> ≤ 100kΩ, I <sub>Q</sub> = 100μA   | 70                   | 91                   |                   | 70                   | 91                   |                   |       |
|                      |  | R <sub>S</sub> ≤ 100kΩ, I <sub>Q</sub> = 1mA <sup>(2)</sup>  | 60                   | 87                   |                   | 60                   | 87                   |                   |       |

NOTE: All typical values have been characterized but are not tested.

# ICL76XX

## ELECTRICAL CHARACTERISTICS (7641/42 ONLY) (Continued)

( $V_{SUPPLY} = \pm 5.0V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.)

| Symbol          | Parameter   | Test Conditions  | 76XXC (6) |       |       | 76XXE (6) |       |       | Units           |
|-----------------|---|--|-----------|-------|-------|-----------|-------|-------|-----------------|
|                 |   |  | Min       | Typ   | Max   | Min       | Typ   | Max   |                 |
| PSRR            | Power Supply Rejection Ratio<br>$V_{SUPPLY} = \pm 8V$ to $\pm 2V$ | $R_S \leq 100k\Omega$ , $I_Q = 10\mu A^{(1)}$                                  | 80        | 94    |       | 80        | 94    |       | dB              |
|                 |   | $R_S \leq 100k\Omega$ , $I_Q = 100\mu A$                                       | 80        | 86    |       | 80        | 86    |       |                 |
|                 |   | $R_S \leq 100k\Omega$ , $I_Q = 1mA^{(2)}$                                      | 70        | 77    |       | 70        | 77    |       |                 |
| $e_n$           | Input Referred Noise Voltage                                      | $R_S = 100\Omega$ , $f = 1kHz$   |           | 100   |       |           | 100   |       | nV/ $\sqrt{Hz}$ |
| $I_n$           | Input Referred Noise Current                                      | $R_S = 100\Omega$ , $f = 1kHz$   |           | 0.01  |       |           | 0.01  |       | pA/ $\sqrt{Hz}$ |
| $I_{SUPPLY}$    | Supply Current<br>(Per Amplifier)                                 | No Signal, No Load<br>7642 ONLY  |           | 0.01  | 0.03  |           | 0.01  | 0.03  | mA              |
|                 |   | $I_Q = 10\mu A^{(1)}$ Low Bias   |           | 0.01  | 0.022 |           | 0.01  | 0.022 |                 |
|                 |   | $I_Q = 100\mu A$ Medium Bias   |           | 0.1   | 0.25  |           | 0.1   | 0.25  |                 |
|                 |   | $I_Q = 1mA^{(2)}$ High Bias  |           | 1.0   | 2.5   |           | 1.0   | 2.5   |                 |
| $V_{O1}/V_{O2}$ | Channel Separation  | $A_V = 100$  |           | 120   |       |           | 120   |       | dB              |
| SR              | Slew Rate   | $A_V = 1$ , $C_L = 100pF$<br>$V_{IN} = 8Vp-p$                                  |           |       |       |           |       |       | V/ $\mu s$      |
|                 |   | $I_Q = 10\mu A^{(1)}$ , $R_L = 1M\Omega$                                       |           | 0.016 |       |           | 0.016 |       |                 |
|                 |   | $I_Q = 100\mu A$ , $R_L = 100k\Omega$<br>$I_Q = 1mA^{(2)}$ , $R_L = 10k\Omega$ |           | 0.16  |       |           | 0.16  |       |                 |
| $t_r$           | Rise Time   | $V_{IN} = 50mV$ , $C_L = 100pF$<br>$I_Q = 10\mu A^{(1)}$ , $R_L = 1M\Omega$    |           | 20    |       |           | 20    |       | $\mu s$         |
|                 |   | $I_Q = 100\mu A$ , $R_L = 100k\Omega$  |           | 2     |       |           | 2     |       |                 |
|                 |   | $I_Q = 1mA^{(2)}$ , $R_L = 10k\Omega$  |           | 0.9   |       |           | 0.9   |       |                 |
|                 | Overshoot Factor  | $V_{IN} = 50mV$ , $C_L = 100pF$<br>$I_Q = 10\mu A^{(1)}$ , $R_L = 1M\Omega$    |           | 5     |       |           | 5     |       | %               |
|                 |   | $I_Q = 100\mu A$ , $R_L = 100k\Omega$  |           | 10    |       |           | 10    |       |                 |
|                 |   | $I_Q = 1mA^{(2)}$ , $R_L = 10k\Omega$  |           | 40    |       |           | 40    |       |                 |

NOTES: 1. Does not apply to 7641.  
2. Does not apply to 7642.

For Test Conditions:  
C = Commercial Temperature Range:  $0^\circ C$  to  $+70^\circ C$   
M = Military Temperature Range:  $-55^\circ C$  to  $+125^\circ C$

## ELECTRICAL CHARACTERISTICS (7642 ONLY)

( $V_{SUPPLY} = \pm 1.0V$ ,  $I_Q = 10\mu A$ ,  $T_A = 25^\circ C$ , unless otherwise specified.)

| Symbol                   | Parameter                           | Test Conditions   | 76XXC     |     |           | Units            |
|--------------------------|-------------------------------------|---|-----------|-----|-----------|------------------|
|                          |                                     |   | Min       | Typ | Max       |                  |
| $V_{OS}$                 | Input Offset Voltage                | $R_S \leq 100k\Omega$ , $T_A = 25^\circ C$<br>$T_{MIN} \leq T_A \leq T_{MAX}$ |           |     | 10<br>12  | mV               |
| $\Delta V_{OS}/\Delta T$ | Temperature Coefficient of $V_{OS}$ | $R_S \leq 100k\Omega$   |           | 20  |           | $\mu V/^\circ C$ |
| $I_{OS}$                 | Input Offset Current                | $T_A = 25^\circ C$<br>$\Delta T_A = C$  |           | 0.5 | 30<br>300 | pA               |
| $I_{BIAS}$               | Input Bias Current                  | $T_A = 25^\circ C$<br>$\Delta T_A = C$  |           | 1.0 | 50<br>500 | pA               |
| $V_{CMR}$                | Common Mode Voltage Range           |   | $\pm 0.6$ |     |           | V                |

NOTE: All typical values have been characterized but are not tested.

# ICL76XX

## ELECTRICAL CHARACTERISTICS (7642 ONLY) (Continued)

( $V_{SUPPLY} = \pm 1.0V$ ,  $I_Q = 10\mu A$ ,  $T_A = 25^\circ C$ , unless otherwise specified.)

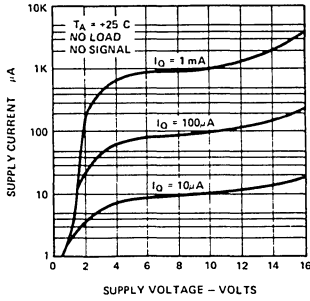
| Symbol          | Parameter                         | Test Conditions   | 76XXC |                          |     | Units          |
|-----------------|-----------------------------------|---|-------|--------------------------|-----|----------------|
|                 |                                   |   | Min   | Typ                      | Max |                |
| $V_{OUT}$       | Output Voltage Swing              | $R_L = 1M\Omega$ , $T_A = 25^\circ C$<br>$\Delta T_A = C$                     |       | $\pm 0.98$<br>$\pm 0.96$ |     | V              |
| $A_{VOL}$       | Large Signal Voltage Gain         | $V_O = \pm 0.1V$ , $R_L = 1M\Omega$<br>$T_A = 25^\circ C$<br>$\Delta T_A = C$ |       | 90<br>80                 |     | dB             |
| GBW             | Unity Gain Bandwidth              |   |       | 0.044                    |     | MHz            |
| $R_{IN}$        | Input Resistance                  |   |       | $10^{12}$                |     | $\Omega$       |
| CMRR            | Common Mode Rejection Ratio       | $R_S \leq 100k\Omega$   |       | 80                       |     | dB             |
| PSRR            | Power Supply Rejection Ratio      |   |       | 80                       |     | dB             |
| $e_n$           | Input Referred Noise Voltage      | $R_S = 100\Omega$ , $f = 1kHz$  |       | 100                      |     | $nV/\sqrt{Hz}$ |
| $i_n$           | Input Referred Noise Current      | $R_S = 100\Omega$ , $f = 1kHz$  |       | 0.01                     |     | $pA/\sqrt{Hz}$ |
| $I_{SUPPLY}$    | Supply Current<br>(Per Amplifier) | No Signal, No Load  |       | 6                        | 15  | $\mu A$        |
| $V_{O1}/V_{O2}$ | Channel Separation                | $A_V = 100$   |       | 120                      |     | dB             |
| SR              | Slew Rate                         | $A_V = 1$ , $C_L = 100pF$<br>$V_{IN} = 0.2V_{p-p}$<br>$R_L = 1M\Omega$        |       | 0.016                    |     | $V/\mu s$      |
| $t_r$           | Rise Time                         | $V_{IN} = 50mV$ , $C_L = 100pF$<br>$R_L = 1M\Omega$                           |       | 20                       |     | $\mu s$        |
|                 | Overshoot Factor                  | $V_{IN} = 50mV$ , $C_L = 100pF$<br>$R_L = 1M\Omega$                           |       | 5                        |     | %              |

NOTE: C=Commercial Temperature Range (0°C to +70°C)

NOTE: All typical values have been characterized but are not tested.

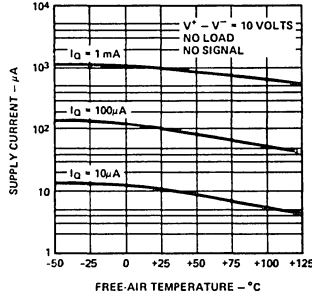
## TYPICAL PERFORMANCE CHARACTERISTICS

**SUPPLY CURRENT PER AMPLIFIER AS A FUNCTION OF SUPPLY VOLTAGE**



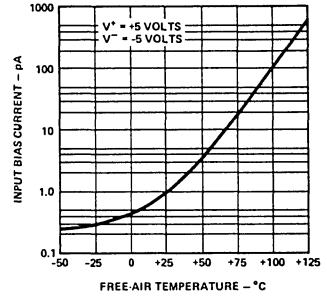
0307-12

**SUPPLY CURRENT PER AMPLIFIER AS A FUNCTION OF FREE-AIR TEMPERATURE**



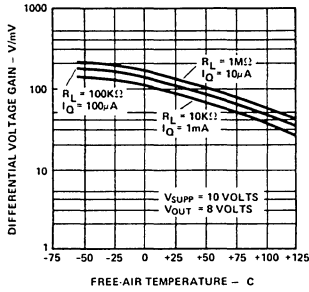
0307-13

**INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE**



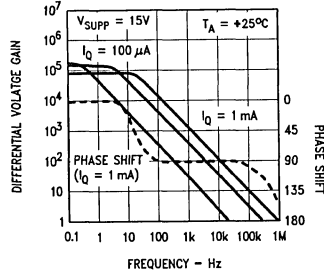
0307-14

**LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF FREE-AIR TEMPERATURE**



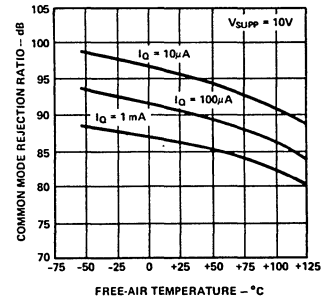
0307-15

**LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN AND PHASE SHIFT AS A FUNCTION OF FREQUENCY**



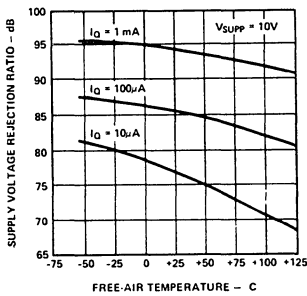
0307-16

**COMMON MODE REJECTION RATIO AS A FUNCTION OF FREE-AIR TEMPERATURE**



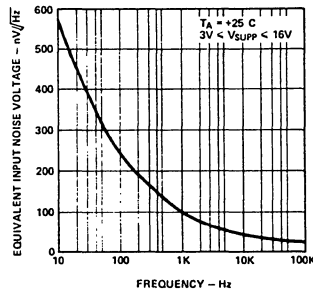
0307-17

**POWER SUPPLY REJECTION RATIO AS A FUNCTION OF FREE-AIR TEMPERATURE**



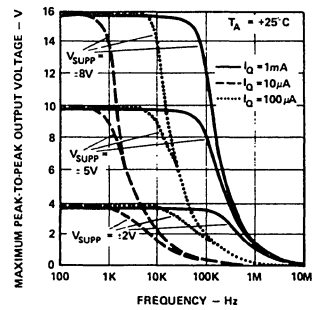
0307-18

**EQUIVALENT INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY**



0307-19

**PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY**



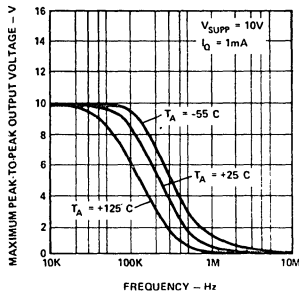
0307-20

3  
OPERATIONAL AMPLIFIERS

NOTE: All typical values have been characterized but are not tested.

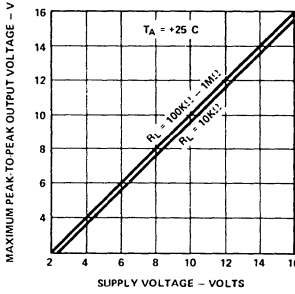
## TYPICAL PERFORMANCE CHARACTERISTICS

**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY**



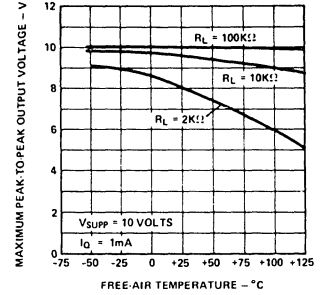
0307-21

**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE**



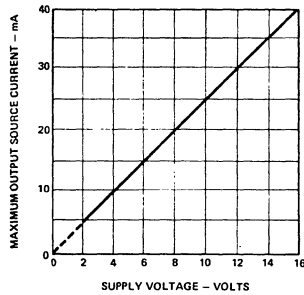
0307-22

**MAXIMUM PEAK-TO-PEAK VOLTAGE AS A FUNCTION OF FREE-AIR TEMPERATURE**



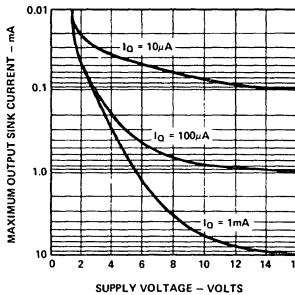
0307-23

**MAXIMUM OUTPUT SOURCE CURRENT AS A FUNCTION OF SUPPLY VOLTAGE**



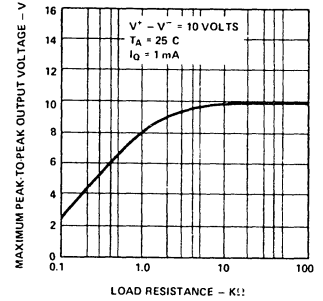
0307-24

**MAXIMUM OUTPUT SINK CURRENT AS A FUNCTION OF SUPPLY VOLTAGE**



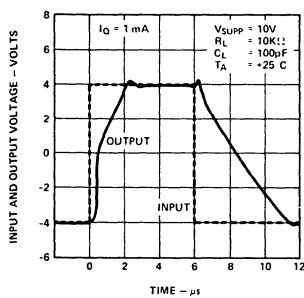
0307-25

**MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF LOAD RESISTANCE**



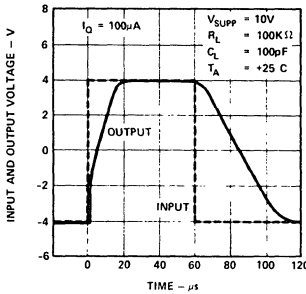
0307-26

**VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE**



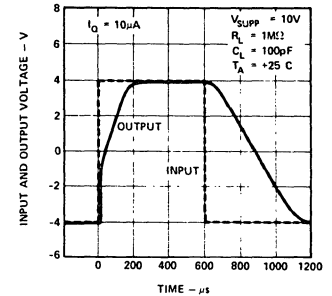
0307-27

**VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE**



0307-28

**VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE**



0307-29

NOTE: All typical values have been characterized but are not tested.

## DETAILED DESCRIPTION

### Static Protection

All devices are static protected by the use of input diodes. However, strong static fields should be avoided, as it is possible for the strong fields to cause degraded diode junction characteristics, which may result in increased input leakage currents.

### Latchup Avoidance

Junction-isolated CMOS circuits employ configurations which produce a parasitic 4-layer (p-n-p-n) structure. The 4-layer structure has characteristics similar to an SCR, and under certain circumstances may be triggered into a low impedance state resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails may be applied to any pin. In general, the op-amp supplies must be established simultaneously with, or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to 2mA to prevent latchup.

### Choosing the Proper $I_Q$

Each device in the ICL76XX family has a similar  $I_Q$  set-up scheme, which allows the amplifier to be set to nominal quiescent currents of  $10\mu\text{A}$ ,  $100\mu\text{A}$  or  $1\text{mA}$ . These current settings change only very slightly over the entire supply voltage range. The ICL7611/12 have an external  $I_Q$  control terminal, permitting user selection of each amplifiers' quiescent current. (The 7621 and 7641/42 have fixed  $I_Q$  settings - refer to selector guide for details.) To set the  $I_Q$  of programmable versions, connect the  $I_Q$  terminal as follows:

$I_Q = 10\mu\text{A}$  —  $I_Q$  pin to  $V^+$

$I_Q = 100\mu\text{A}$  —  $I_Q$  pin to ground. If this is not possible, any voltage from  $V^+ - 0.8$  to  $V^- + 0.8$  can be used.

$I_Q = 1\text{mA}$  —  $I_Q$  pin to  $V^-$

NOTE: The output current available is a function of the quiescent current setting. For maximum p-p output voltage swings into low impedance loads,  $I_Q$  of  $1\text{mA}$  should be selected.

### Output Stage and Load Driving Considerations

Each amplifiers' quiescent current flows primarily in the output stage. This is approximately 70% of the  $I_Q$  settings.

This allows output swings to almost the supply rails for output loads of  $1\text{M}\Omega$ ,  $100\text{k}\Omega$ , and  $10\text{k}\Omega$ , using the output stage in a highly linear class A mode. In this mode, crossover distortion is avoided and the voltage gain is maximized. However, the output stage can also be operated in Class AB for higher output currents. (See graphs under Typical Operating Characteristics). During the transition from Class A to Class B operation, the output transfer characteristic is non-linear and the voltage gain decreases.

### Input Offset Nulling

For those models provided with OFFSET NULLING pins, nulling may be achieved by connecting a 25K pot between the OFFSET terminals with the wiper connected to  $V^+$ . At quiescent currents of  $1\text{mA}$  and  $100\mu\text{A}$ , the nulling range provided is adequate for all  $V_{OS}$  selections; however with  $I_Q = 10\mu\text{A}$ , nulling may not be possible with higher values of  $V_{OS}$ .

### Frequency Compensation

The ICL76XX are internally compensated, and are stable for closed loop gains as low as unity with capacitive loads up to  $100\text{pF}$

### Extended Common Mode Input Range

The ICL7612 incorporates additional processing which allows the input CMVR to exceed each power supply rail by 0.1 volt for applications where  $V_{SUPP} \geq \pm 1.5\text{V}$ . For those applications where  $V_{SUPP} \leq \pm 1.5\text{V}$ , the input CMVR is limited in the positive direction, but may exceed the negative supply rail by 0.1 volt in the negative direction (eg. for  $V_{SUPP} = \pm 1.0\text{V}$ , the input CMVR would be  $+0.6$  volts to  $-1.1$  volts).

### OPERATION AT $V_{SUPP} = \pm 1.0$ VOLTS

Operation at  $V_{SUPP} = \pm 1.0\text{V}$  is guaranteed at  $I_Q = 10\mu\text{A}$  for A and B grades only. This applies to those devices with selectable  $I_Q$ , and devices that are set internally to  $I_Q = 10\mu\text{A}$  (i.e., ICL7611, 7612, 7642).

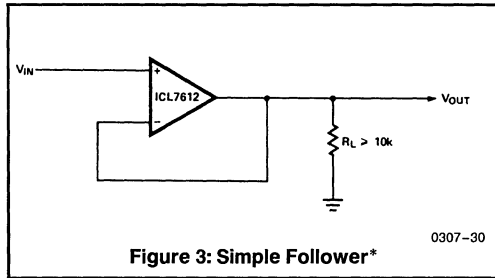
Output swings to within a few millivolts of the supply rails are achievable for  $R_L \geq 1\text{M}\Omega$ . Guaranteed input CMVR is  $\pm 0.6\text{V}$  minimum and typically  $+0.9\text{V}$  to  $-0.7\text{V}$  at  $V_{SUPP} = \pm 1.0\text{V}$ . For applications where greater common mode range is desirable, refer to the description of ICL7612 above.



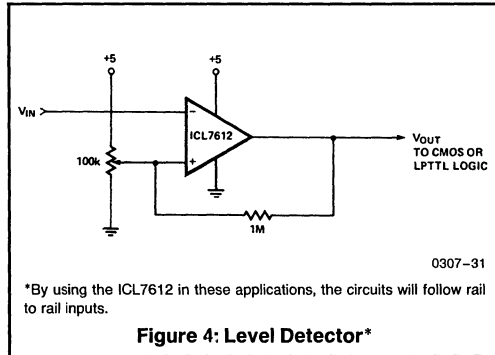
The user is cautioned that, due to extremely high input impedances, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup.

## APPLICATIONS

Note that in no case is  $I_Q$  shown. The value of  $I_Q$  must be chosen by the designer with regard to frequency response and power dissipation.

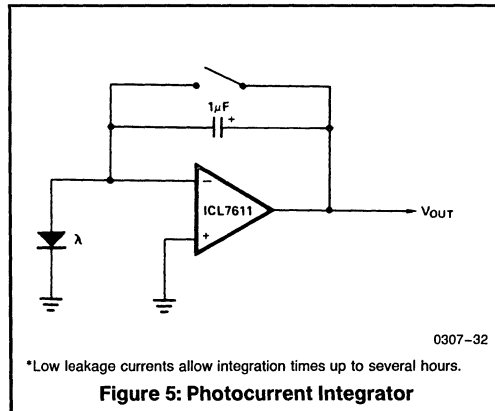


**Figure 3: Simple Follower\***



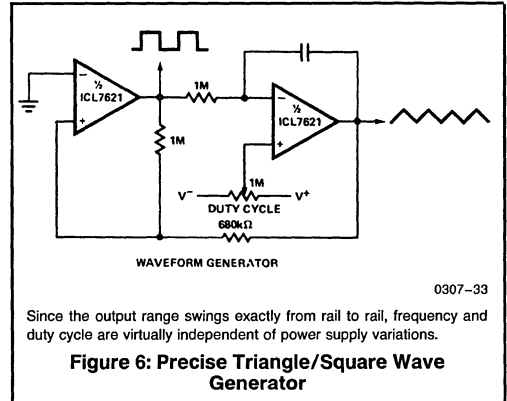
\*By using the ICL7612 in these applications, the circuits will follow rail to rail inputs.

**Figure 4: Level Detector\***



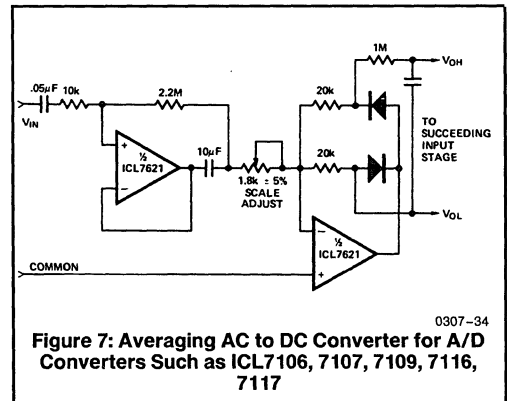
\*Low leakage currents allow integration times up to several hours.

**Figure 5: Photocurrent Integrator**

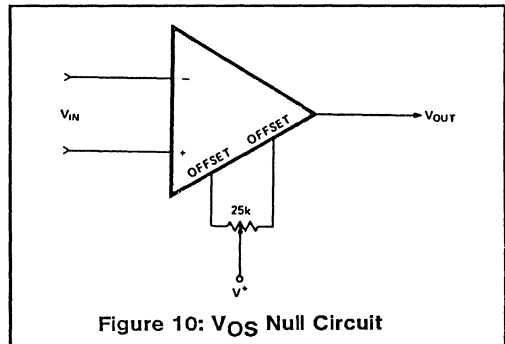
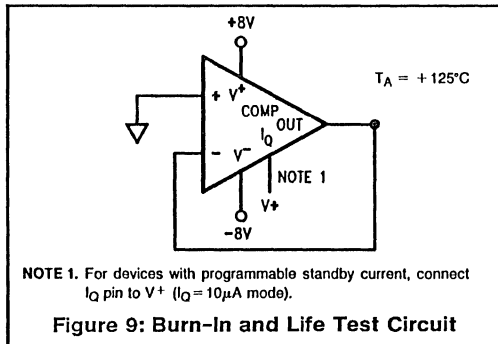
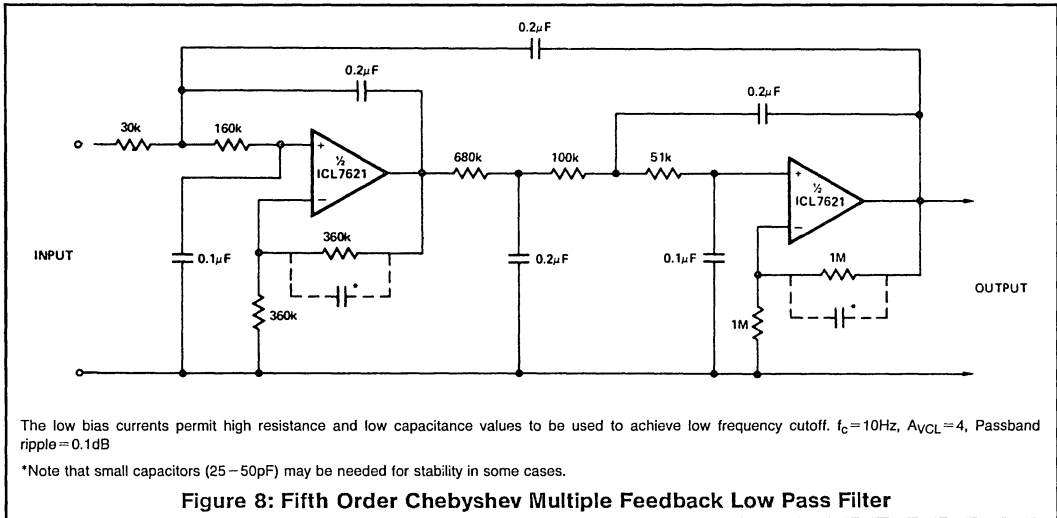


Since the output range swings exactly from rail to rail, frequency and duty cycle are virtually independent of power supply variations.

**Figure 6: Precise Triangle/Square Wave Generator**



**Figure 7: Averaging AC to DC Converter for A/D Converters Such as ICL7106, 7107, 7109, 7116, 7117**





# ICL7650S

## Super Chopper-Stabilized Operational Amplifier

### GENERAL DESCRIPTION

The ICL7650S Super Chopper-Stabilized Amplifier offers exceptionally low input offset voltage and is extremely stable with respect to time and temperature. It is a direct replacement for the industry-standard ICL7650 offering *improved* input offset voltage, *lower* input offset voltage temperature coefficient, *reduced* input bias current, and *wider* common mode voltage range. All improvements are highlighted in *bold italics* in the Electrical Characteristics section. *Critical parameters are guaranteed over the entire commercial, industrial and military temperature ranges.*

Harris' unique CMOS chopper-stabilized amplifier circuitry is user-transparent, virtually eliminating the traditional chopper amplifier problems of intermodulation effects, chopping spikes, and overrange lock-up.

The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs; these are the only external components necessary.

The clock oscillator and all the other control circuitry is entirely self-contained. However the 14-lead version includes a provision for the use of an external clock, if required for a particular application. In addition, the ICL7650S is internally compensated for unity-gain operation.

### FEATURES

- **Guaranteed Max Input Offset Voltage for All Temperature Ranges**
- **Low Long-Term and Temperature Drifts of Input Offset Voltage**
- **Guaranteed Max Input Bias Current—10 pA**
- **Extremely Wide Common Mode Voltage Range—+3.5 to -5V**
- **Reduced Supply Current—2 mA**
- **Guaranteed Minimum Output Source/Sink Current**
- **Extremely High Gain—150 dB**
- **Extremely High CMRR and PSRR—140 dB**
- **High Slew Rate—2.5V/ $\mu$ s**
- **Wide Bandwidth—2 MHz**
- **Unity-gain Compensated**
- **Clamp Circuit to Avoid Overload Recovery Problems and Allow Comparator Use**
- **Extremely Low Chopping Spikes at Input and Output**
- **Characterized Fully Over All Temperature Ranges**
- **Improved, Direct Replacement for Industry-Standard ICL7650 and other Second-Source Parts**

### ORDERING INFORMATION

| Part          | Temperature Range | Package        |
|---------------|-------------------|----------------|
| ICL7650SCPA-1 | 0°C to +70°C      | 8-Pin Plastic  |
| ICL7650SCPD   |                   | 14-Pin Plastic |
| ICL7650SCTV-1 |                   | 8-Pin TO-99    |
| ICL7650SIPA-1 | -25°C to +85°C    | 8-Pin Plastic  |
| ICL7650SIPD   |                   | 14-Pin Plastic |
| ICL7650SIJD   |                   | 14-Pin CERDIP  |
| ICL7650SITV-1 |                   | 8-Pin TO-99    |
| ICL7650SMJD   | -55°C to +125°C   | 14-Pin CERDIP  |
| ICL7650SMTV-1 |                   | 8-Pin TO-99    |

# ICL7650S

## ABSOLUTE MAXIMUM RATINGS

|   |                                    |
|---|------------------------------------|
| Total Supply Voltage ( $V^+$ to $V^-$ )                         | 18V                                |
| Input Voltage   | ( $V^+ + 0.3$ ) to ( $V^- - 0.3$ ) |
| Voltage on Oscillator Control Pins                              | $V^+$ to $V^-$                     |
| Duration of Output Short Circuit                                | Indefinite                         |
| Current into Any Pin  | 10 mA                              |
| —while operating (Note 1)                                       | 100 $\mu$ A                        |
| Continuous Total Power Dissipation ( $T_A = 25^\circ\text{C}$ ) |                                    |
| CERDIP Package  | 500 mW                             |
| Plastic Package   | 375 mW                             |
| TO-99   | 250 mW                             |

|                                      |   |
|--------------------------------------|---|
| Storage Temperature Range            | $-55^\circ\text{C}$ to $150^\circ\text{C}$  |
| Lead Temperature (Soldering, 10 sec) | $+300^\circ\text{C}$                        |
| Operating Temperature Range          |   |
| ICL7650SC                            | $0^\circ\text{C}$ to $+70^\circ\text{C}$    |
| ICL7650SI                            | $-25^\circ\text{C}$ to $+85^\circ\text{C}$  |
| ICL7650SM                            | $-55^\circ\text{C}$ to $+125^\circ\text{C}$ |

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

Test Conditions: ( $V^+ = +5\text{V}$ ,  $V^- = -5\text{V}$ ,  $T_A = +25^\circ\text{C}$ , Test Circuit as in Fig. 3 (unless otherwise specified))

| Symbol                   | Parameter  | Test Conditions   | Limits    |                  |          | Units                           |
|--------------------------|--|---|-----------|------------------|----------|---------------------------------|
|                          |  |   | Min       | Typ              | Max      |                                 |
| $V_{OS}$                 | Input Offset Voltage<br>(Note 2)                                       | $T_A = +25^\circ\text{C}$   |           | $\pm 0.7$        | $\pm 5$  | $\mu\text{V}$                   |
|                          |  | $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$                       |           | $\pm 1$          | $\pm 8$  |                                 |
|                          |  | $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$                     |           | $\pm 2$          | $\pm 10$ |                                 |
|                          |  | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$                    |           | $\pm 4$          | $\pm 20$ |                                 |
| $\Delta V_{OS}/\Delta T$ | Average Temperature<br>Coefficient of Input Offset<br>Voltage (Note 2) | $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$                       |           | 0.02             |          | $\mu\text{V}/^\circ\text{C}$    |
|                          |  | $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$                     |           | 0.02             |          |                                 |
|                          |  | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$                    |           | 0.03             | 0.1      |                                 |
| $\Delta V_{OS}/\Delta t$ | Change in Input<br>Offset with Time                                    |   |           | 100              |          | $\text{nV}/\sqrt{\text{month}}$ |
| $I_{bias}$               | Input Bias Current<br>$ I(+) ,  I(-) $                                 | $T_A = 25^\circ\text{C}$  |           | 4                | 10       | $\text{pA}$                     |
|                          |  | $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$                       |           | 5                | 20       |                                 |
|                          |  | $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$                     |           | 20               | 50       |                                 |
|                          |  | $-55^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$                     |           | 20               | 50       |                                 |
|                          |  | $+85^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$                    |           | 100              | 500      |                                 |
| $I_{OS}$                 | Input Offset Current<br>$ I(-) - I(+) $                                | $T_A = 25^\circ\text{C}$  |           | 8                | 20       | $\text{pA}$                     |
|                          |  | $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$                       |           | 10               | 40       |                                 |
|                          |  | $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$                     |           | 20               | 40       |                                 |
|                          |  | $-55^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$                     |           | 20               | 40       |                                 |
|                          |  | $+85^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$                    |           | 20               | 50       |                                 |
| $R_{IN}$                 | Input Resistance   |   |           | 10 <sup>12</sup> |          | $\Omega$                        |
| $A_{VOL}$                | Large Signal Voltage Gain<br>(Note 2)                                  | $R_L = 10 \text{ k}\Omega, V_O = \pm 4\text{V}, T_A = 25^\circ\text{C}$ | 135       | 150              |          | dB                              |
|                          |  | $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$                       | 130       |                  |          |                                 |
|                          |  | $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$                     | 130       |                  |          |                                 |
|                          |  | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$                    | 120       |                  |          |                                 |
| $V_{OUT}$                | Output Voltage Swing<br>(Note 3)                                       | $R_L = 10 \text{ k}\Omega$  | $\pm 4.7$ | $\pm 4.85$       |          | V                               |
|                          |  | $R_L = 100 \text{ k}\Omega$   |           | $\pm 4.95$       |          |                                 |

NOTE: All typical values have been characterized but are not tested.

## ELECTRICAL CHARACTERISTICS (Continued)

Test Conditions: ( $V^+ = +5V$ ,  $V^- = -5V$ ,  $T_A = +25^\circ\text{C}$ , Test Circuit as in Fig. 3 (unless otherwise specified))

| Symbol                         | Parameter                                      | Test Conditions   | Limits     |                   |             | Units                        |
|--------------------------------|--|---|------------|-------------------|-------------|------------------------------|
|                                |  |   | Min        | Typ               | Max         |                              |
| <b>CMVR</b>                    | <b>Common Mode Voltage Range</b><br>(Note 2)   | $T_A = 25^\circ\text{C}$                                      | -5         | <b>-5.2 to +4</b> | <b>+3.5</b> | V                            |
|                                |  | $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$             | -5         |                   | <b>+3.5</b> |                              |
|                                |  | $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$           | -5         |                   | <b>+3.5</b> |                              |
|                                |  | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$          | -5         |                   | <b>+3.5</b> |                              |
| <b>CMRR</b>                    | <b>Common Mode Rejection Ratio</b><br>(Note 2) | $\text{CMVR} = -5V \text{ to } +3.5V, T_A = 25^\circ\text{C}$ | <b>120</b> | <b>140</b>        |             | dB                           |
|                                |  | $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$             | <b>120</b> |                   |             |                              |
|                                |  | $25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$            | <b>115</b> |                   |             |                              |
|                                |  | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$          | <b>110</b> |                   |             |                              |
| <b>PSRR</b>                    | <b>Power Supply Rejection Ratio</b>            | $V^+, V^- = \pm 3V \text{ to } \pm 8V$                        | 120        | <b>140</b>        |             | dB                           |
| en                             | Input Noise Voltage                            | $R_S = 100\Omega, f = \text{DC to } 10 \text{ Hz}$            |            | 2                 |             | $\mu\text{Vp-p}$             |
| in                             | Input Noise Current                            | $f = 10 \text{ Hz}$   |            | 0.01              |             | $\text{pA}/\sqrt{\text{Hz}}$ |
| GBW                            | Gain Bandwidth Product                         |   |            | 2                 |             | MHz                          |
| SR                             | Slew Rate                                      | $C_L = 50 \text{ pF}, R_L = 10 \text{ k}\Omega$               |            | 2.5               |             | $\text{V}/\mu\text{s}$       |
| $t_r$                          | Rise Time                                      |   |            | 0.2               |             | $\mu\text{s}$                |
|                                | Overshoot                                      |   |            | 20                |             | %                            |
| $V^+ \text{ to } V^-$          | Operating Supply Range                         |   | 4.5        |                   | 16          | V                            |
| <b><i>I<sub>supp</sub></i></b> | <b>Supply Current</b>                          | No Load, $T_A = 25^\circ\text{C}$                             |            | 2                 | <b>3</b>    | mA                           |
|                                |  | $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$             |            |                   | <b>3.2</b>  |                              |
|                                |  | $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$           |            |                   | <b>3.5</b>  |                              |
|                                |  | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$          |            |                   | <b>4</b>    |                              |
| $I_{O \text{ source}}$         | Output Source Current                          | $T_A = 25^\circ\text{C}$                                      | 2.9        | 4.5               |             | mA                           |
|                                |  | $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$             | 2.3        |                   |             |                              |
|                                |  | $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$           | 2.2        |                   |             |                              |
|                                |  | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$          | 2          |                   |             |                              |
| $I_{O \text{ sink}}$           | Output Sink Current                            | $T_A = 25^\circ\text{C}$                                      | 25         | 30                |             | mA                           |
|                                |  | $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$             | 20         |                   |             |                              |
|                                |  | $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$           | 19         |                   |             |                              |
|                                |  | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$          | 17         |                   |             |                              |
| $f_{\text{ch}}$                | Internal Chopping Frequency                    | Pins 12 & 14 Open   | 120        | 250               | 375         | Hz                           |
|                                | Clamp ON Current (Note 4)                      | $R_L = 100 \text{ k}\Omega, T_A = 25^\circ\text{C}$           | 25         | 70                |             | $\mu\text{A}$                |
|                                | <b>Clamp OFF Current</b><br>(Note 4)           | $-4V \leq V_{\text{out}} \leq +4V, T_A = 25^\circ\text{C}$    |            | <b>0.001</b>      | <b>5</b>    | nA                           |
|                                |  | $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$             |            |                   | <b>10</b>   |                              |
|                                |  | $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$           |            |                   | <b>10</b>   |                              |
|                                |  | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$          |            |                   | <b>15</b>   |                              |

**NOTE 1:** Limiting input current to  $100 \mu\text{A}$  is recommended to avoid latchup problems. Typically  $1 \text{ mA}$  is safe, however this is not guaranteed.

**2:** These parameters are guaranteed by design and characterization, but not tested at temperature extremes because thermocouple effects prevent precise measurement of these voltages in automatic test equipment.

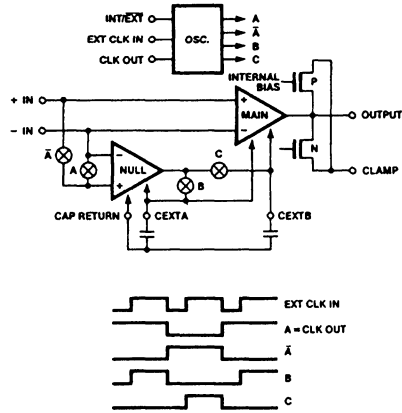
**3:** OUTPUT CLAMP not connected. See typical characteristic curves for output swing vs. clamp current characteristics.

**4:** See OUTPUT CLAMP under detailed description.

**5:** All significant improvements over the industry-standard ICL7650 are highlighted in **bold italics**.

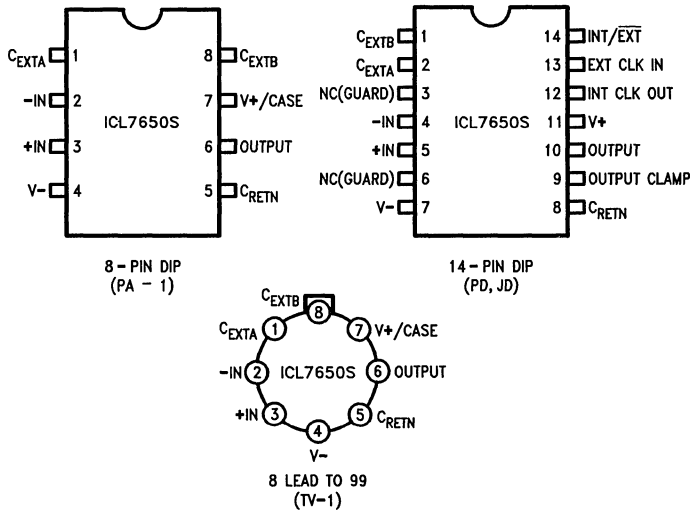
*NOTE: All typical values have been characterized but are not tested.*

# ICL7650S



0089-1

Figure 1: Functional Diagram

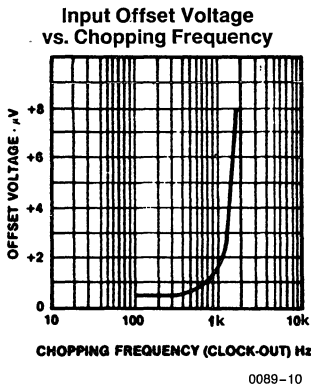
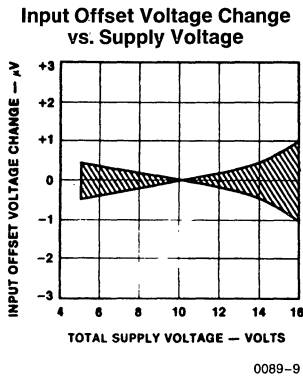
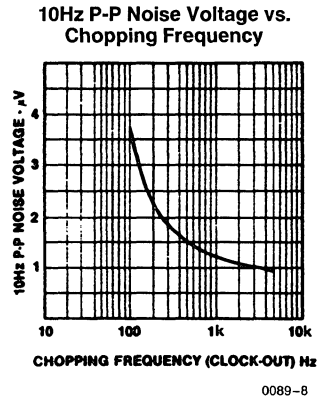
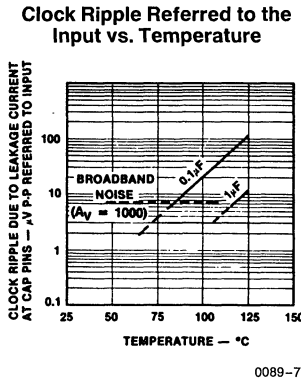
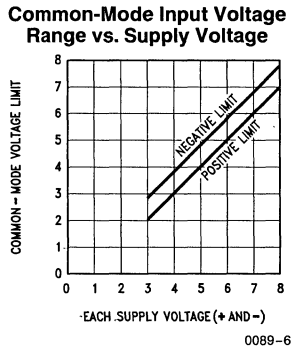
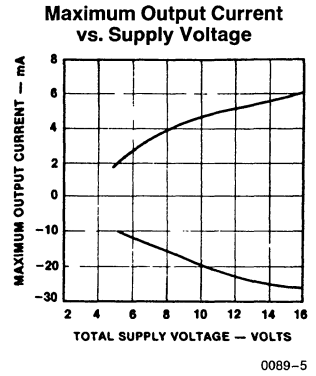
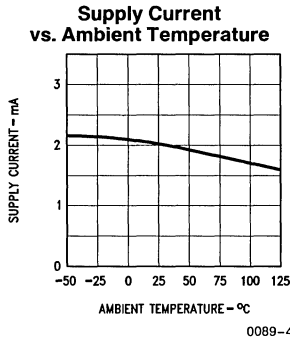
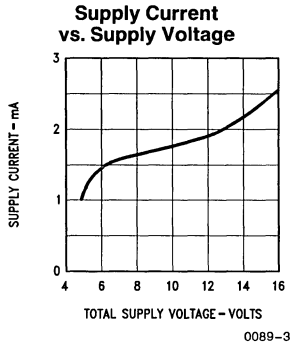


0089-2

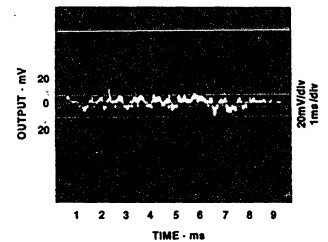
Figure 2: Pin Configurations

# ICL7650S

## TYPICAL PERFORMANCE CHARACTERISTICS



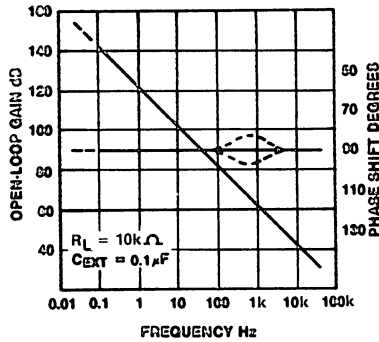
**Output with Zero Input; Gain = 1000; Balanced Source Impedance = 10 kΩ**



NOTE: All typical values have been characterized but are not tested.

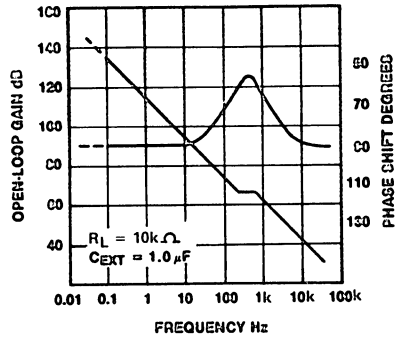
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Open Loop Gain and Phase Shift vs. Frequency



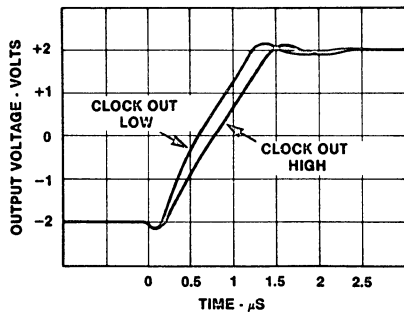
0089-12

Open Loop Gain and Phase Shift vs. Frequency



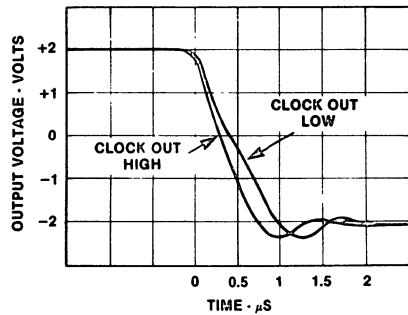
0089-13

Voltage Follower Large Signal Pulse Response\*



0089-14

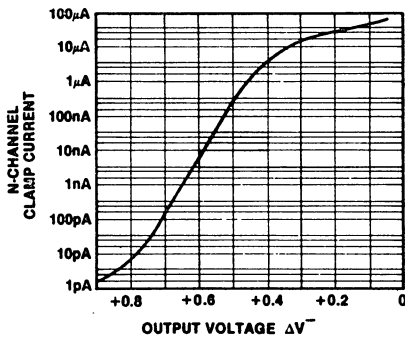
Voltage Follower Large Signal Pulse Response\*



0089-15

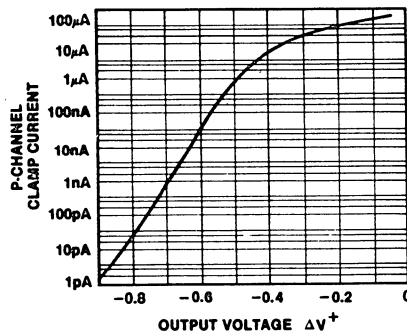
\*THE TWO DIFFERENT RESPONSES CORRESPOND TO THE TWO PHASES OF THE CLOCK.

N-Channel Clamp Current vs. Output Voltage



0089-16

P-Channel Clamp Current vs. Output Voltage



0089-17

NOTE: All typical values have been characterized but are not tested.

# ICL7650S

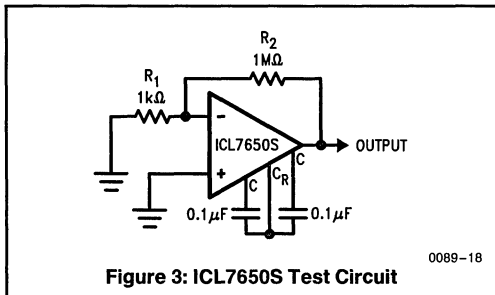


Figure 3: ICL7650S Test Circuit

## DETAILED DESCRIPTION

### Amplifier

The functional diagram shows the major elements of the ICL7650S. There are two amplifiers, the main amplifier, and the nulling amplifier. Both have offset-null capability. The main amplifier is connected continuously from the input to the output, while the nulling amplifier, under the control of the chopping oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET gates, are inherently high impedance, and two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power-supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and  $A_{VOL}$ .

Careful balancing of the input switches, and the inherent balance of the input circuit, minimizes chopper frequency charge injection at the input terminals, and also the feedforward-type injection into the compensation capacitor, which is the main cause of output spikes in this type of circuit.

### Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs. frequency characteristics near the chopping frequency. These effects are substantially reduced in the ICL7650S by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7650S, the intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

### Capacitor Connection

The null/storage capacitors should be connected to the  $C_{EXTA}$  and  $C_{EXTB}$  pins, with a common connection to the  $C_{RETN}$  pin. This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to  $C_{RETN}$ .

NOTE: All typical values have been characterized but are not tested.

### Output Clamp

The OUTPUT CLAMP pin allows reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled input differential inputs are avoided, together with the consequent charge build-up on the correction-storage capacitors. The output swing is slightly reduced.

### Clock

The ICL7650S has an internal oscillator, giving a chopping frequency of 200 Hz, available at the CLOCK OUT pin on the 14-pin devices. Provision has also been made for the use of an external clock in these parts. The INT/EXT pin has an internal pull-up and may be left open for normal operation, but to utilize an external clock this pin must be tied to  $V^-$  to disable the internal clock. The external clock signal may then be applied to the EXT CLOCK IN pin. An internal divide-by-two provides the desired 50% input switching duty cycle. Since the capacitors are charged only when EXT CLOCK IN is high, a 50%–80% positive duty cycle is recommended, especially for higher frequencies. The external clock can swing between  $V^+$  and  $V^-$ . The logic threshold will be at about 2.5V below  $V^+$ . Note also that a signal of about 400 Hz, with a 70% duty cycle, will be present at the EXT CLOCK IN pin with INT/EXT high or open. This is the internal clock signal before being fed to the divider.

In those applications where a strobe signal is available, an alternate approach to avoid capacitor misbalancing during overload can be used. If a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier, neither capacitor will be charged. Since the leakage at the capacitor pins is quite low at room temperature, the typical amplifier will drift less than 10  $\mu$ V/sec, and relatively long measurements can be made with little change in offset.

## BRIEF APPLICATION NOTES

### Component Selection

The two required capacitors,  $C_{EXTA}$  and  $C_{EXTB}$ , have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1  $\mu$ F, and to maintain the same relationship between the chopping frequency and the nulling time constant this value should be scaled approximately in proportion if an external clock is used. A high-quality film-type capacitor such as mylar is preferred, although a ceramic or other lower-grade capacitor may prove suitable in many applications. For quickest setting on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1  $\mu$ V.

### Static Protection

All device pins are static-protected by the use of input diodes. However, strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics, which may result in increased input-leakage currents.

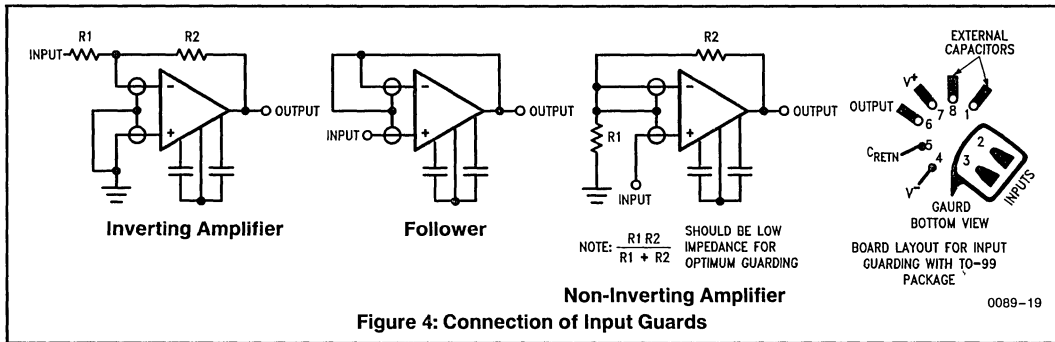


Figure 4: Connection of Input Guards

## Latchup Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1 mA to avoid latchup, even under fault conditions.

## Output Stage/Load Driving

The output circuit is a high-impedance type (approximately 18 kΩ), and therefore with loads less than this value, the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17 dB lower with a 1 kΩ load than with a 10 kΩ load. If the amplifier is used strictly for DC, this lower gain is of little consequence, since the DC gain is typically greater than 120 dB even with a 1 kΩ load. However, for wideband applications, the best frequency response will be achieved with a load resistor of 10 kΩ or higher. This will result in a smooth 6 dB/octave response from 0.1 Hz to 2 MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier.

## Thermo-Electric Effects

The ultimate limitations to ultra-high precision DC amplifiers are the thermo-electric or Peltier effects arising in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermo-electric voltages typically around 0.1 μV/°C, but up to tens of μV/°C for some materials, will be generated. In order to

realize the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermoelectric-efficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

## Guarding

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the ICL7650S. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the 14-pin dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration, but corresponds to that of the LM108).

NOTE: All typical values have been characterized but are not tested.



## Pin Compatibility

The basic pinout of the 8-pin device corresponds, where possible, to that of the industry-standard 8-pin devices, the LM741, LM101, etc. The null-storing external capacitors are connected to pins 1 and 8, usually used for offset null or compensation capacitors, or simply not connected. In the case of the OP-05 and OP-07 devices, the replacement of the offset-null pot, connected between pins 1 and 8 and  $V+$ , by two capacitors from those pins to pin 5, will provide easy compatibility. As for the LM108, replacement of the compensation capacitor between pins 1 and 8 by the two capacitors to pin 5 is all that is necessary. The same operation, with the removal of any connection to pin 5, will suffice for the LM101,  $\mu$ A748, and similar parts.

The 14-pin device pinout corresponds most closely to that of the LM108 device, owing to the provision of "NC" pins for guarding between the input and all other pins. Since this device does not use any of the extra pins, and has no provision for offset-nulling, but requires a compensation capacitor, some changes will be required in layout to convert it to the ICL7650S.

## TYPICAL APPLICATIONS

Clearly the applications of the ICL7650S will mirror those of other op amps. Anywhere that the performance of a circuit can be significantly improved by a reduction of input-offset voltage and bias current, the ICL7650S is the logical choice. Basic non-inverting and inverting amplifier circuits are shown in Figures 5 and 6. Both circuits can use the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op amps by the ICL7650S are the supply voltage ( $\pm 8V$  max.) and the output drive capability (10 k $\Omega$  load for full swing). Even these limitations can be overcome using a simple booster circuit, as shown in Figure 7, to enable the full output capabilities of the LM741 (or any other standard device) to be combined with the input capabilities of the ICL7650S. The pair form a composite device, so loop gain stability, when the feedback network is added, should be watched carefully.

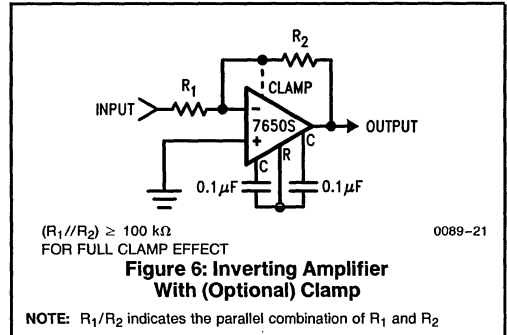
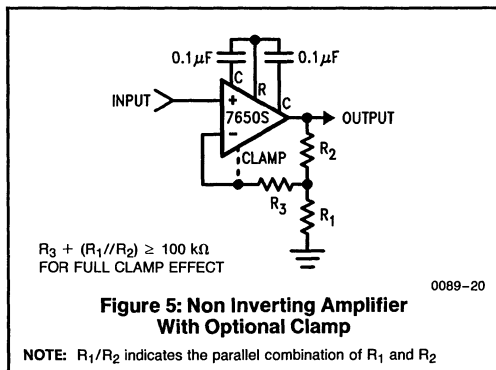
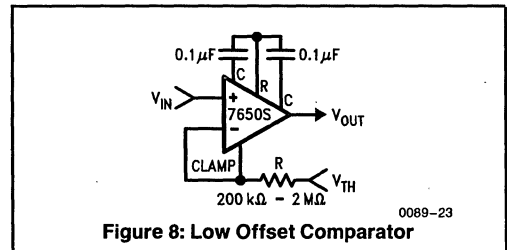
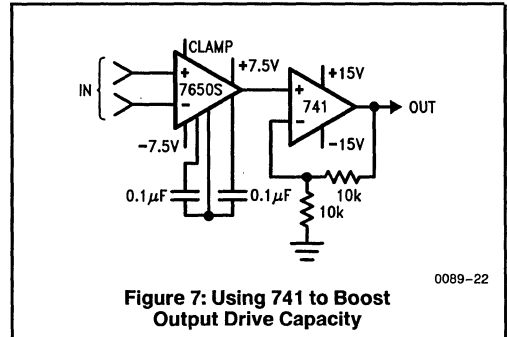
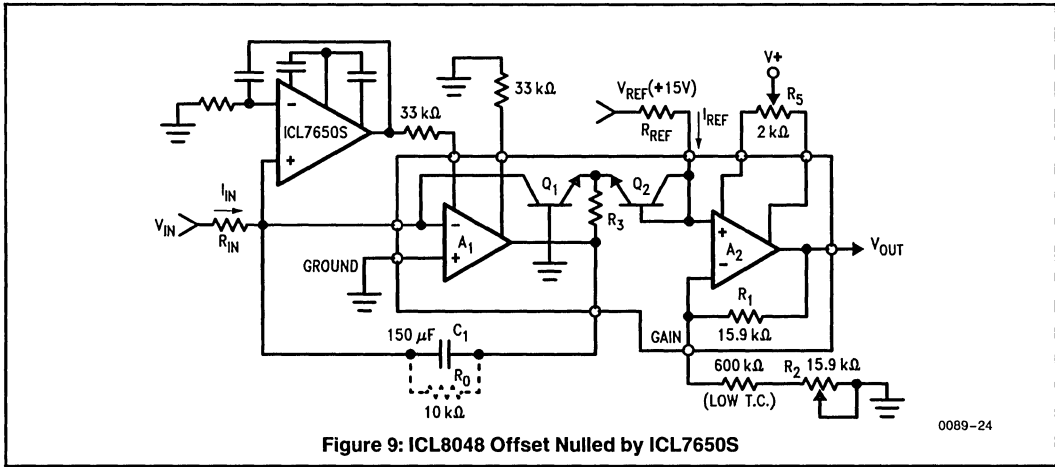


Figure 8 shows the use of the clamp circuit to advantage in a zero-offset comparator. The usual problems in using a chopper stabilized amplifier in this application are avoided, since the clamp circuit forces the inverting input to follow the input signal. The threshold input must tolerate the output clamp current  $\approx V_{IN}/R$  without disturbing other portions of the system.



Normal logarithmic amplifiers are limited in dynamic range in the voltage-input mode by their input-offset voltage. The built-in temperature compensation and convenience features of the ICL8048 can be extended to a voltage-input dynamic range of close to 6 decades by using the ICL7650S to offset-null the ICL8048, as shown in Figure 9. The same concept can also be used with such devices as the HA2500 or HA2600 families of op amps to add very low offset voltage capability to their very high slew rates and bandwidths. Note that these circuits will also have their DC gains, CMRR, and PSRR enhanced.

# ICL7650S



FOR FURTHER APPLICATIONS ASSISTANCE, SEE A053 AND R017

NOTE: All typical values have been characterized but are not tested.

# Operational Amplifiers Glossary of Terms

**AVERAGE INPUT OFFSET CURRENT DRIFT** - The average change in offset current between room (+25°C) and high temperature (+125°C, +85°C or +75°C) or between room temperature and low temperature (0°C, -25°C or -55°C) divided by the temperature difference.

**AVERAGE OFFSET VOLTAGE DRIFT** - The average change in offset voltage between room (+25°C) and high temperature (+125°C, +85°C or +75°C) or between room temperature and low temperature (0°C, -25°C or -55°C) divided by the temperature difference.

**CHANNEL SEPARATION** - The ratio of the output of a driven amplifier to the output (referred to input) of an adjacent undriven amplifier.

**COMMON MODE INPUT VOLTAGE ( $V_{IC}$ )** - The average of the voltages present at the differential input terminals.

**COMMON MODE INPUT VOLTAGE RANGE ( $V_{ICR}$ )** - The range of voltage that if exceeded at either input terminal will cause the amplifier to cease operating properly.

**COMMON MODE REJECTION RATIO (CMRR)** - The ratio of change in input offset voltage to change in input common-mode voltage, expressed in dB.

$$CMRR = 20 \times \log_{10} \frac{V_{IO}}{V_{CM}}$$

**COMMON MODE RESISTANCE ( $r_{IC}$ )** - The ratio of change in input common-mode voltage to the resulting change in input current.

**DIFFERENTIAL INPUT RESISTANCE ( $r_{ID}$ )** - The ratio of change in input differential voltage (small-signal, assumes amplifier operating linearly) to the resulting change in differential input current.

**FULL POWER BANDWIDTH (FPBW)** - The maximum frequency at which a full scale undistorted (THD < 1%) sine wave can be obtained at the output of the amplifier.

**GAIN BANDWIDTH (GBW)** - The open-loop gain of an op amp (in V/V) at a mid-band, linear-region frequency (usually between 1KHz and 10KHz) times that frequency (in Hz).  $GBW = [A_{VOL}] \cdot f$

**INPUT BIAS CURRENT ( $I_{BIAS}$ )** - The average of the currents flowing into or out of the input terminals when the output is at zero volts.

**INPUT CAPACITANCE ( $C_{IN}$ )** - The equivalent capacitance seen looking into either input terminal.

**INPUT NOISE CURRENT ( $I_n$ )** - The input noise current that would reproduce the noise seen at the output if all amplifier noise sources were set to zero and the source impedances were large compared to the optimum source impedance.

**INPUT OFFSET CURRENT ( $I_{OS}$ )** - The difference in the currents flowing into the two input terminals when the output is at zero volts.

**INPUT OFFSET VOLTAGE ( $V_{OS}$ )** - The differential D.C. voltage required to zero the output voltage with no input signal or load. Input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

**INPUT NOISE VOLTAGE ( $e_n$ )** - The input noise voltage that would reproduce the noise seen at the output if all the amplifier noise sources and source resistances were set to zero.

**LARGE SIGNAL VOLTAGE GAIN ( $A_V$ )** - The ratio of the peak to peak output voltage swing (over a specified range) to the change in input voltage required to drive the output.

**OUTPUT CURRENT ( $I_{OUT}$ )** - The output current available from the amplifier at some specified output voltage.

**OUTPUT RESISTANCE ( $R_O$ )** - The ratio of the change in output voltage to the change in output current.

**OUTPUT SHORT CIRCUIT CURRENT ( $I_{SC}$ )** - The output current available from the amplifier with the output shorted to ground (or other specified potential).

**OUTPUT VOLTAGE SWING ( $V_{OUT}$ )** - The maximum output voltage swing, referred to ground, that can be obtained under specified loading conditions.

**OVERSHOOT** - Peak excursion above final value of an output step response.

**POWER SUPPLY REJECTION RATIO (PSRR)** - The ratio of the change in input offset voltage to the change in power supply voltage producing it.

**RISE TIME ( $t_r$ )** - The time required for an output voltage step to change from 10% to 90% of its final value, when the input is subjected to a small-signal voltage pulse.

**SETTLING TIME ( $t_{set.}$ )** - The time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

**SLEW RATE (SR)** - The rate of change of the output under large-signal conditions. Slew rate may be specified separately for both positive and negative going changes.

**SUPPLY CURRENT ( $I_S$ )** - The current required from the power supply to operate the amplifier with no load and the output at zero volts.

**SUPPLY VOLTAGE RANGE** - The range of power supply voltage over which the amplifier may be safely operated.

**UNITY GAIN BANDWIDTH** - The frequency range from D.C. to that frequency where the amplifiers open loop gain is unity.

## COMPARATORS

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**NOTE:** Bold type designates a new product from Harris.

# Selection Guide

## COMPARATORS

General Purpose Electrical Characteristics,  $T_A = +25^\circ\text{C}$

| TYPE                   | $V_{IO}$<br>MAX<br>mV | $I_I$<br>MAX<br>nA | $I^+$<br>MAX<br>Ma | MAX<br>$V^+$ ,<br>$V^-$ | AOL<br>(MIN)<br>dB | RESPONSE<br>TIME | PIN<br>COUNT<br>AND<br>PKG<br>TYPE |
|------------------------|-----------------------|--------------------|--------------------|-------------------------|--------------------|------------------|------------------------------------|
| <b>Dual-Unit Types</b> |                       |                    |                    |                         |                    |                  |                                    |
| CA3290                 | 20                    | 50pA               | 3                  | $\pm 18$                | 88                 | (1)              | 8E, S, T<br>14E1                   |
| CA3290A                | 10                    | 40pA               | 3                  | $\pm 18$                | 88                 |                  |                                    |
| <b>Quad-Unit Types</b> |                       |                    |                    |                         |                    |                  |                                    |
| CA139                  | 5                     | 100                | 8                  | $\pm 18$                | -                  | (2)              | 14E                                |
| CA139A                 | 2                     | 100                | 8                  | $\pm 18$                | 94                 |                  | 14E                                |
| CA239                  | 5                     | 250                | 2                  | $\pm 18$                | -                  |                  | 14E                                |
| CA239A                 | 2                     | 250                | 2                  | $\pm 18$                | 94                 |                  | 14E                                |
| CA339                  | 5                     | 250                | 2                  | $\pm 18$                | 94                 |                  | 14E                                |
| CA339A                 | 2                     | 250                | 2                  | $\pm 18$                | 94                 |                  | 14E                                |

| TYPE    | $V_{IO}$<br>mV | $I_{IO}$<br>nA | COMMENTS   | RE-<br>SPONSE<br>TIME | PIN<br>CT<br>AND<br>PKG<br>TYPE |
|---------|----------------|----------------|--|-----------------------|---------------------------------|
| HA-4900 | 2              | 10             | Single or dual supply.<br>Analog and logic<br>supplies separated for<br>easier interface and<br>noise immunity | 130ns                 | 16                              |
| HA-4902 | 2              | 10             |  | 130ns                 | 16                              |
| HA-4905 | 4              | 25             |  | 130ns                 | 16                              |

\*See Packaging and Ordering Information in Section 12.

Response Time:

- (1) -  $t_r = 1.2 \mu\text{s}$ ,  $t_f = 200 \text{ ns}$   
 (2) -  $t_r = 1.3 \mu\text{s}$ ,  $t_f = 300 \text{ ns}$

## Ultra High Speed Comparators

| TYPE      | PROPAGATION<br>DELAY<br>ns | TRACKING<br>BANDWIDTH<br>MHz | $V_{IO}$<br>mV | LARGE SIGNAL<br>VOLTAGE GAIN<br>V/V | COMMENTS  |
|-----------|----------------------------|------------------------------|----------------|-------------------------------------|---|
| HFA-0003  | 2.0                        | 270                          | 1              | 3100                                | Direct Output Version   |
| HFA-0003L | 2.1                        | 270                          | 1              | 3100                                | Latched Output Version with User Programmable<br>Hysteresis Control |

# CA139, CA139A, CA239, CA239A, CA339, CA339A, LM339\*, LM339A\*

## Quad Voltage Comparators

For Industrial, Commercial and Military Applications

August 1991

### Features

- Operation from Single or Dual Supplies
- Common Mode Input Voltage Range to GND
- Output Voltage Compatible with TTL, DTL, ECL, MOS and CMOS
- Differential Input Voltage Range Equal to the Supply Voltage
- Maximum Input Offset Voltage ( $V_{IO}$ ):
  - ▶ CA139A, CA239A, CA339A ..... 2mV
  - ▶ CA139, CA239, CA339 ..... 5mV
- Replacement for Industry Types 139, 239, 339, 139A, 239A, and 339A

### Applications

- Square Wave Generators
- Time Delay Generators
- Pulse Generators
- Multivibrators
- High Voltage Digital Logic Gates
- A/D Converters
- MOS Clock Timers

### Description

The CA139, CA239, CA339, CA139A, CA239A, and CA339A types consist of four independent single or dual supply voltage comparators on a single monolithic substrate. The common mode input voltage range includes ground even when operated from a single supply, and the low power supply current drain makes these comparators suitable for battery operation. These types were designed to directly interface with TTL and CMOS.

Types CA139A, CA239A, and CA339A have all the features and characteristics of their prototype counterparts CA139, CA239, and CA339 plus an even lower input offset voltage characteristic. These devices are supplied in a 14-lead Small Outline package (M suffix), in a 14-lead dual-in-line plastic package (E suffix) and in a 14-lead dual-in-line hermetic (frit-seal) ceramic package (F suffix). The CA339 is also available in chip form (H suffix).

4  
COMPARATORS

### Functional Diagram

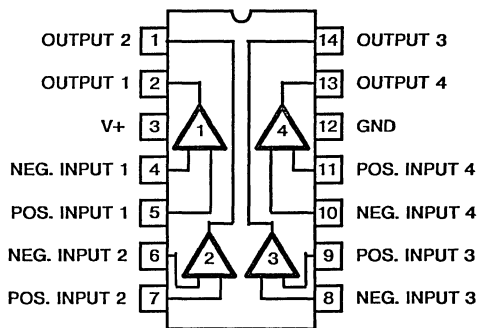


FIGURE 1.

\* Technical Data on LM Branded types is identical to the corresponding CA Branded types

**CA139, CA139A, CA239, CA239A,  
CA339, CA339A, LM339, LM339A**

**MAXIMUM RATINGS, Absolute-Maximum Values at  $T_A = 25^\circ\text{C}$ :**

|  |  |
|--|--|
| DC SUPPLY VOLTAGE .....  | 36 V or $\pm 18$ V                           |
| DC DIFFERENTIAL INPUT VOLTAGE .....  | $\pm 36$ V                                   |
| INPUT VOLTAGE .....  | -0.3 V to +36 V                              |
| INPUT CURRENT ( $V_I < -0.3$ V)* .....   | 50 mA  |
| OUTPUT SHORT CIRCUIT TO GROUND <sup>▲</sup><br>(Single Supply) .....   | Continuous                                   |
| DEVICE DISSIPATION:<br>Up to $T_A = 55^\circ\text{C}$ .....  | 750 mW                                       |
| Above $T_A = 55^\circ\text{C}$ .....   | derate linearly at 6.67 mW/ $^\circ\text{C}$ |
| AMBIENT TEMPERATURE RANGE:<br>Operating .....  | -55 to +125 $^\circ\text{C}$                 |
| Storage .....  | -65 to +150 $^\circ\text{C}$                 |
| LEAD TEMPERATURE (DURING SOLDERING):<br>At distance 1/16 $\pm$ 1/32 in. (1.59 $\pm$ 0.79 mm)<br>from case for 10 seconds max. .... | +265 $^\circ\text{C}$ .                      |

\* Inputs must not go more negative than -0.3 V.

<sup>▲</sup> Short circuits from the output to  $V^+$  can cause excessive heating and eventual destruction. The maximum output current independent of  $V^+$  is approximately 20 mA.

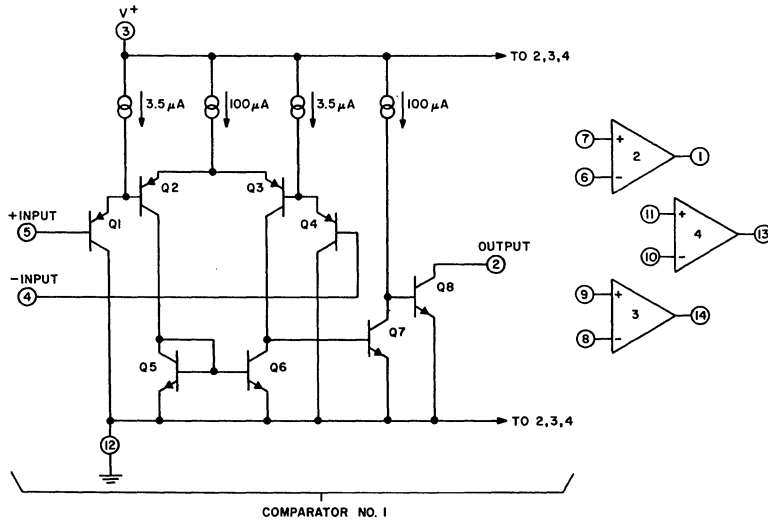


Fig. 2—Schematic diagram.

**CA139, CA139A, CA239, CA239A,  
CA339, CA339A, LM339, LM339A**

**ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC   | TEST CONDITIONS  |        | LIMITS |      |             |        |     |             | UNITS         |
|--|--|--------|--------|------|-------------|--------|-----|-------------|---------------|
|  | $V^+ = 5\text{ V}$<br>Unless otherwise indicated   |        | CA139  |      |             | CA139A |     |             |               |
|  | Min.   | Typ.   | Max.   | Min. | Typ.        | Max.   |     |             |               |
| Input Offset Voltage ( $V_{IO}$ )<br>At Output Switch Point $V \cong 1.4\text{ V}$ | $V_{REF} = 1.4\text{ V}, R_S = 0$  | 25°C   | –      | 2    | 5           | –      | 1   | 2           | mV            |
|  |  | Note 1 | –      | –    | 9           | –      | –   | 4           |               |
| Differential Input Voltage ( $V_{ID}$ )  | Keep all inputs $\geq 0\text{ V}$ for $V^-$ (If used),<br>Notes 1, 2   |        | –      | –    | 36          | –      | –   | 36          | V             |
| Saturation Voltage ( $V_{sat}$ )   | $V_I^- = 1\text{ V}, V_I^+ = 0\text{ V}, I_{SINK} \leq 4\text{ mA}$  | 25°C   | –      | 250  | 400         | –      | 250 | 400         | mV            |
|  |  | Note 1 | –      | –    | 700         | –      | –   | 700         |               |
| Common-Mode Input Voltage Range ( $V_{ICR}$ )                                      | Note 3   | 25°C   | 0      | –    | $V^+ - 1.5$ | 0      | –   | $V^+ - 1.5$ | V             |
|  |  | Note 1 | 0      | –    | $V^+ - 2$   | 0      | –   | $V^+ - 2$   |               |
| Input Offset Current ( $I_{IO}$ )  | $I_I^+ - I_I^-$  | 25°C   | –      | 3    | 25          | –      | 3   | 25          | nA            |
|  |  | Note 1 | –      | –    | 100         | –      | –   | 100         |               |
| Input Bias Current ( $I_{IB}$ )  | $I_I^+$ or $I_I^-$ with Output in Linear Range   | 25°C   | –      | 25   | 100         | –      | 25  | 100         | nA            |
|  |  | Note 1 | –      | –    | 300         | –      | –   | 300         |               |
| Total Supply Current ( $I^+$ )   | $R_L = \infty$ on all comparators, $T_A = 25^\circ\text{C}$  |        | –      | 0.8  | 2           | –      | 0.8 | 2           | mA            |
| Output Leakage Current   | $V_I^+ \geq 1\text{ V}, V_I^- = 0, V_O = 5\text{ V}$<br>$V_I^+ \geq 1\text{ V}, V_I^- = 0, V_O = 30\text{ V}$                    | 25°C   | –      | 0.1  | –           | –      | 0.1 | –           | nA            |
|  |  | Note 1 | –      | –    | 1           | –      | –   | 1           | $\mu\text{A}$ |
| Output Sink Current  | $V_I^- \geq 1\text{ V}, V_I^+ = 0, V_O \leq +1.5\text{ V}, T_A = 25^\circ\text{C}$   |        | 6      | 16   | –           | 6      | 16  | –           | mA            |
| Voltage Gain ( $A_{OL}$ )  | $R_L \geq 15\text{ k}\Omega, V^+ = 15\text{ V}, T_A = 25^\circ\text{C}$  |        | –      | 200  | –           | 50     | 200 | –           | V/mV          |
| Large Signal Response Time   | $V_I = \text{TTL Logic Swing}, V_{REF} = +1.4\text{ V}, V_{RL} = 5.0\text{ V}, R_L = 5.1\text{ k}\Omega, T_A = 25^\circ\text{C}$ |        | –      | 300  | –           | –      | 300 | –           | ns            |
| Response Time<br>See Figs. 5 & 6   | $V_{RL} = 5\text{ V}, R_L = 5.1\text{ k}\Omega, T_A = 25^\circ\text{C}$  |        | –      | 1.3  | –           | –      | 1.3 | –           | $\mu\text{s}$ |

Note 1: Ambient Temperature ( $T_A$ ) applicable over operating temperature range as shown below.

CA139 (–55 to +125°C) | CA239 (–25 to +85°C) | CA339 (0 to +70°C)  
CA139A | CA239A | CA339A

Note 2: The comparator will provide a proper output state even if the positive swing of the inputs exceeds the power supply voltage level, if the other input remains within the common-mode voltage range. The low input voltage state must not be less than –0.3 V (or 0.3 V below the magnitude of the negative power supply, if used).

Note 3: The upper end of the common-mode voltage range is ( $V^+$ ) – 1.5 V, but either or both inputs can go to +30 V without damage.



**CA139, CA139A, CA239, CA239A,  
CA339, CA339A, LM339, LM339A**

**ELECTRICAL CHARACTERISTICS**

| CHARACTERISTIC   | TEST CONDITIONS  |        | LIMITS       |      |                     |                |      |                     | UNITS |
|--|--|--------|--------------|------|---------------------|----------------|------|---------------------|-------|
|  | V <sup>+</sup> = 5 V   |        | CA239, CA339 |      |                     | CA239A, CA339A |      |                     |       |
|  | Unless otherwise indicated   |        | Min.         | Typ. | Max.                | Min.           | Typ. | Max.                |       |
| Input Offset Voltage (V <sub>IO</sub> )<br>At Output Switch Point V ≅ 1.4 V. | V <sub>REF</sub> = 1.4 V, R <sub>S</sub> = 0   | 25°C   | –            | 2    | 5                   | –              | 1    | 2                   | mV    |
|  |  | Note 1 | –            | –    | 9                   | –              | –    | 4                   |       |
| Differential Input Voltage (V <sub>ID</sub> )                                | Keep all inputs ≥ 0 V for V <sup>–</sup> (If used), Notes 1, 2   |        | –            | –    | 36                  | –              | –    | 36                  | V     |
| Saturation Voltage (V <sub>sat</sub> )                                       | V <sub>I<sup>–</sup></sub> = 1 V,<br>V <sub>I<sup>+</sup></sub> = 0 V,<br>I <sub>SINK</sub> ≤ 4 mA   | 25°C   | –            | 250  | 400                 | –              | 250  | 400                 | mV    |
|  |  | Note 1 | –            | –    | 700                 | –              | –    | 700                 |       |
| Common-Mode Input Voltage Range (V <sub>ICR</sub> )                          | Note 3   | 25°C   | 0            | –    | V <sup>+</sup> –1.5 | 0              | –    | V <sup>+</sup> –1.5 | V     |
|  |  | Note 1 | 0            | –    | V <sup>+</sup> –2   | 0              | –    | V <sup>+</sup> –2   |       |
| Input Offset Current (I <sub>IO</sub> )                                      | I <sub>I<sup>+</sup></sub> – I <sub>I<sup>–</sup></sub>  | 25°C   | –            | 5    | 50                  | –              | 5    | 50                  | nA    |
|  |  | Note 1 | –            | –    | 150                 | –              | –    | 150                 |       |
| Input Bias Current (I <sub>IB</sub> )  | I <sub>I<sup>+</sup></sub> or I <sub>I<sup>–</sup></sub> with Output in Linear Range   | 25°C   | –            | 25   | 250                 | –              | 25   | 250                 | nA    |
|  |  | Note 1 | –            | –    | 400                 | –              | –    | 400                 |       |
| Total Supply Current (I <sup>+</sup> )                                       | R <sub>L</sub> = ∞ on all comparators, T <sub>A</sub> = 25°C   |        | –            | 0.8  | 2                   | –              | 0.8  | 2                   | mA    |
| Output Leakage Current   | V <sub>I<sup>+</sup></sub> ≥ 1 V,<br>V <sub>I<sup>–</sup></sub> = 0,<br>V <sub>O</sub> = 5 V   | 25°C   | –            | 0.1  | –                   | –              | 0.1  | –                   | nA    |
|  | V <sub>I<sup>+</sup></sub> ≥ 1 V,<br>V <sub>I<sup>–</sup></sub> = 0,<br>V <sub>O</sub> = 30 V  | Note 1 | –            | –    | 1                   | –              | –    | 1                   | μA    |
| Output Sink Current  | V <sub>I<sup>–</sup></sub> ≥ 1 V,<br>V <sub>I<sup>+</sup></sub> = 0,<br>V <sub>O</sub> ≤ +1.5 V,<br>T <sub>A</sub> = 25°C                  |        | 6            | 16   | –                   | 6              | 16   | –                   | mA    |
| Voltage Gain (A <sub>OL</sub> )  | R <sub>L</sub> ≥ 15 kΩ, V <sup>+</sup> = 15 V,<br>T <sub>A</sub> = 25°C  |        | –            | 200  | –                   | 50             | 200  | –                   | V/mV  |
| Large Signal Response Time   | V <sub>I</sub> = TTL Logic Swing, V <sub>REF</sub> = +1.4 V, V <sub>RL</sub> = 5.0 V,<br>R <sub>L</sub> = 5.1 kΩ,<br>T <sub>A</sub> = 25°C |        | –            | 300  | –                   | –              | 300  | –                   | ns    |
| Response Time<br>See Figs. 5 & 6   | V <sub>RL</sub> = 5 V,<br>R <sub>L</sub> = 5.1 kΩ,<br>T <sub>A</sub> = 25°C  |        | –            | 1.3  | –                   | –              | 1.3  | –                   | μs    |

Note 1: Ambient Temperature (T<sub>A</sub>) applicable over operating temperature range as shown below.

CA139 (–55 to +125°C) CA239 (–25 to +85°C) CA339 (0 to +70°C)  
CA139A (–55 to +125°C) CA239A (–25 to +85°C) CA339A (0 to +70°C)

Note 2: The comparator will provide a proper output state even if the positive swing of the inputs exceeds the power supply voltage level, if the other input remains within the common-mode voltage range. The low input voltage state must not be less than –0.3 V (or 0.3 V below the magnitude of the negative power supply, if used).

Note 3: The upper end of the common-mode voltage range is (V<sup>+</sup>) – 1.5 V, but either or both inputs can go to +30 V without damage.

# CA139, CA139A, CA239, CA239A, CA339, CA339A, LM339, LM339A

## TYPICAL CHARACTERISTICS

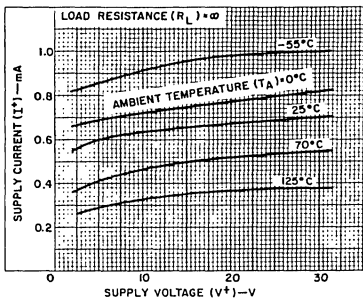


Fig. 3—Supply current vs. supply voltage.

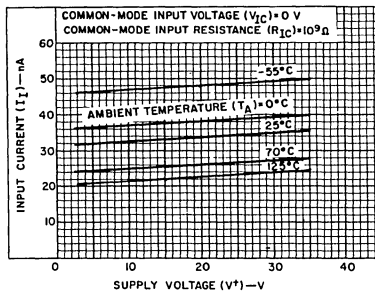


Fig. 4—Input current vs. supply voltage.

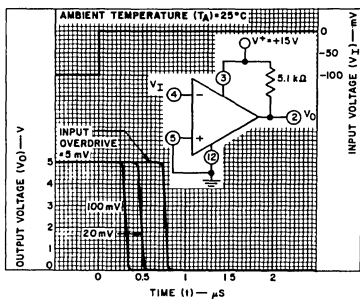


Fig. 5—Response time for various input overdrives—negative transition.

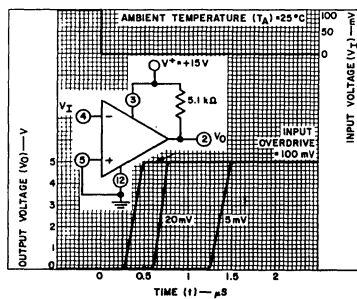


Fig. 6—Response time for various input overdrives—positive transition.

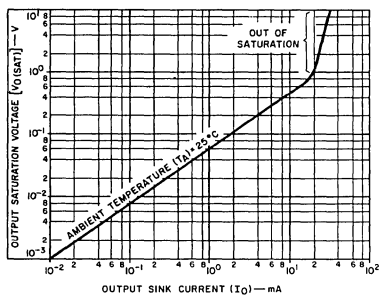
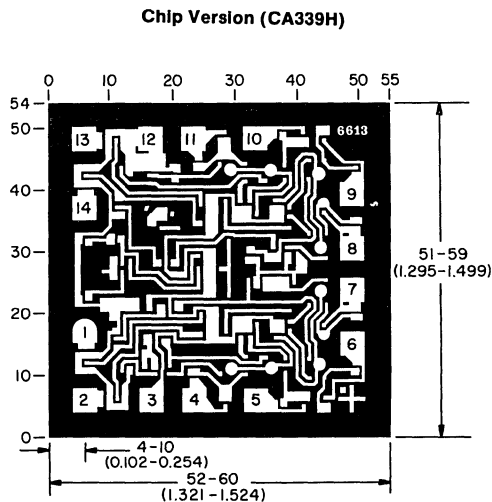


Fig. 7—Output saturation voltage vs. output sink current.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

## Programmable Schmitt Trigger - With Memory Dual-Input Precision Level Detectors

August 1991

### Features

- Programmable Operating Current
- Micropower Standby Dissipation
- Direct Control of Currents Up to ..... 150mA
- Low Input On/Off Current of Less Than 1nA for Programmable Bias Current of 1 $\mu$ A
- Built-in Hysteresis..... 20mV (Max)

### Applications

- Control of Relays, Heaters, LEDs, Lamps, Photosensitive Devices, Thyristors, Solenoids, etc.
- Signal Reconditioning
- Phase and Frequency Modulators
- On/Off Motor Switching
- Schmitt Triggers, Level Detectors
- Time Delays
- Overvoltage, Overcurrent, Overtemperature Protection
- Battery-Operated Equipment
- Square and Triangular-Wave Generators

### Description

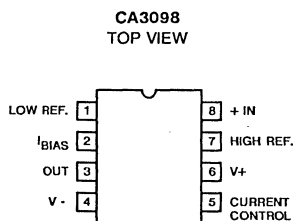
The CA3098 Programmable Schmitt Trigger is a monolithic silicon integrated circuit designed to control high-operating-current loads such as thyristors, lamps, relays, etc. The CA3098 can be operated with either a single power supply with maximum operating voltage of 16V, or a dual power supply with maximum operating voltage of  $\pm 8V$ . It can directly control currents up to 150mA and operates with microwatt standby power dissipation when the current to be controlled is less than 30mA. The CA3098 contains the following major circuit-function features (see Figure 1):

1. Differential amplifiers and summer: the circuit uses two differential amplifiers, one to compare the input voltage with the "high" reference, and the other to compare the input with the "low" reference. The resultant output of the differential amplifiers actuates a summer circuit which delivers a trigger that initiates a change in state of a flip-flop.
2. Flip-flop: the flip-flop functions as a bistable "memory" element that changes state in response to each trigger command.
3. Driver and output stages: these stages permit the circuit to "sink" maximum peak load currents up to 150mA at terminal 3.
4. Programmable operating current: the circuit incorporates access at terminal 2 to permit programming the desired quiescent operating current and performance parameters.

The CA3098 is supplied in the 8 lead dual-in-line plastic package ("Mini-DIP", E suffix), and in chip form (H suffix).

For information on another Harris Dual-Input Precision Level Detector, see the data bulletin for the Harris CA3099E, File No. 620.

### Pinout



### Block Diagram

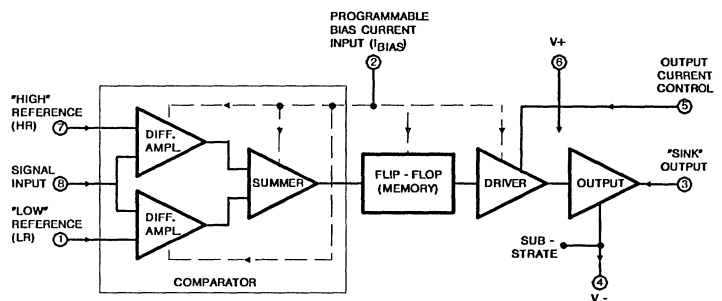


FIGURE 1. BLOCK DIAGRAM OF CA3098 PROGRAMMABLE SCHMITT TRIGGER

# CA3098

## ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$ Unless Otherwise Specified

| CHARACTERISTIC                                    | TEST CONDITIONS   | Fig. No. | LIMITS |           |      | UNITS                        |
|---|---|----------|--------|-----------|------|------------------------------|
|   |   |          | Min.   | Typ.      | Max. |                              |
| Input Offset Voltage:<br>"Low" Ref., $V_{IO(LR)}$ | $V_{LR} = \text{Gnd}, V_{HR} = 3\text{ V}$<br>$I_{BIAS} = 100\ \mu\text{A}$                   | 5        | -15    | -3        | 6    | mV                           |
| "High" Ref., $V_{IO(HR)}$                         | $V_{HR} = \text{Gnd}, V_{LR} = -3\text{ V}$<br>$I_{BIAS} = 100\ \mu\text{A}$                  | 6        | -10    | $\pm 10$  | 10   |                              |
| Temp. Coeff:<br>"Low" Ref.                        | $-55^\circ\text{C}$ to $+125^\circ\text{C}$   | 7        | -      | 4.5       | -    | $\mu\text{V}/^\circ\text{C}$ |
| "High" Ref.                                       | $-55^\circ\text{C}$ to $+125^\circ\text{C}$   | 8        | -      | $\pm 8.2$ | -    |                              |
| Min. Hysteresis<br>Voltage $V_{IO(HR-LR)}$ :      | $V_{REG} = 6\text{ V}, V^+ = 12\text{ V}$<br>$I_{BIAS} = 100\ \mu\text{A}$                    | 9        | -      | 3         | 20   | mV                           |
| Temp. Coeff.                                      | $-55^\circ\text{C}$ to $+125^\circ\text{C}$   | 10       | -      | 6.7       | -    | $\mu\text{V}/^\circ\text{C}$ |
| Output Saturation Voltage,<br>$V_{CE(SAT)}$       | $V_I = 4\text{ V}, V_{REG} = 6\text{ V},$<br>$V^+ = 12\text{ V}, I_{BIAS} = 100\ \mu\text{A}$ | 11,12    | -      | 0.72      | 1.2  | V                            |
| Total Supply Current,<br>$I_{TOTAL}$ :            |   | 13,14    |        |           |      |                              |
| "ON"  | $V_I = 4\text{ V}, V_{REG} = 6\text{ V};$<br>$V^+ = 12\text{ V}, I_{BIAS} = 100\ \mu\text{A}$ |          | 500    | 710       | 800  | $\mu\text{A}$                |
| "OFF"   | $V_I = 8\text{ V}, V_{REG} = 6\text{ V}$<br>$V^+ = 12\text{ V}, I_{BIAS} = 100\ \mu\text{A}$  |          | 400    | 560       | 750  | $\mu\text{A}$                |
| Input Bias Current, $I_{IB}$ :                    |   | 15       |        |           |      |                              |
| $I_{B(p-n-p)}$                                    | $V_I = 4\text{ V}, V_{REG} = 6\text{ V}$<br>$V^+ = 12\text{ V}, I_{BIAS} = 100\ \mu\text{A}$  |          | -      | 42        | 100  | nA                           |
| $I_{B(n-p-n)}$                                    | $V_I = 8\text{ V}, V_{REG} = 6\text{ V}$<br>$V^+ = 12\text{ V}, I_{BIAS} = 100\ \mu\text{A}$  |          | -      | 28        | 100  | nA                           |
| Output Leakage Current,<br>$I_{CE(OFF)}$          | Current from Term. 3 when<br>Q46 is "OFF"   | -        | -      | -         | 10   | $\mu\text{A}$                |
| Switching Times:                                  |   | 18       |        |           |      |                              |
| Delay, $t_d$                                      | $I_C = 100\ \mu\text{A}$  |          | -      | 600       | -    | ns                           |
| Fall, $t_f$                                       | $I_{BIAS} = 100\ \mu\text{A}$   |          | -      | 50        | -    | ns                           |
| Rise, $t_r$                                       | $V^+ = 5\text{ V}$  |          | -      | 500       | -    | ns                           |
| Storage, $t_s$                                    | $V_{REG} = 2.5\text{ V}$  |          | -      | 4.5       | -    | $\mu\text{s}$                |
| Output Current, $I_O$                             | $V^+ = 12\text{ V}, I_{BIAS} = 50\ \mu\text{A}$   | -        | 100    | -         | -    | mA                           |

# CA3098

Maximum Ratings, Absolute-Maximum Values at  $T_A = 25^\circ\text{C}$ :

|  |   |                      |
|--|---|----------------------|
| Supply Voltage Between Terminals 6 and 4, .....  | 16  | V                    |
| Output Voltage Between Terminals 7 and 4, and 3 and 4 .....                                  | 16  | V                    |
| Differential Input Voltage Between Terminals 8 and 1, and<br>Terminals 7 and 8 .....         | 10  | V                    |
| Operating Voltage Range:   |   |                      |
| Term. 8 .....  | $V^-$ to $V^+$                                  |                      |
| Term. 7 .....  | $(V^- \text{ plus } 2.0 \text{ V})$ to $V^+$    |                      |
| Term. 1 .....  | $(V^-)$ to $(V^+ \text{ minus } 2.0 \text{ V})$ |                      |
| Load Current (Term. 3) .....   | 150   | mA                   |
| Input Current to Voltage Regulator (Term. 5) .....   | 25  | mA                   |
| Programmable Bias Current (Term. 2) .....  | 1   | mA                   |
| Output Current Control (Term. 5) .....   | 15  | mA                   |
| Power Dissipation:   |   |                      |
| Up to $T_A = 55^\circ\text{C}$ .....   | 630   | mW                   |
| Above $T_A = 55^\circ\text{C}$ Derate linearly at .....                                      | 6.67  | mW/ $^\circ\text{C}$ |
| Ambient Temperature Range (All Packages):  |   |                      |
| Operating .....  | -55 to +125                                     | $^\circ\text{C}$     |
| Storage .....  | -65 to +150                                     | $^\circ\text{C}$     |
| Lead Temperature (During Soldering):   |   |                      |
| At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79$ mm)<br>from case for 10 seconds max. .... | 265   | $^\circ\text{C}$     |

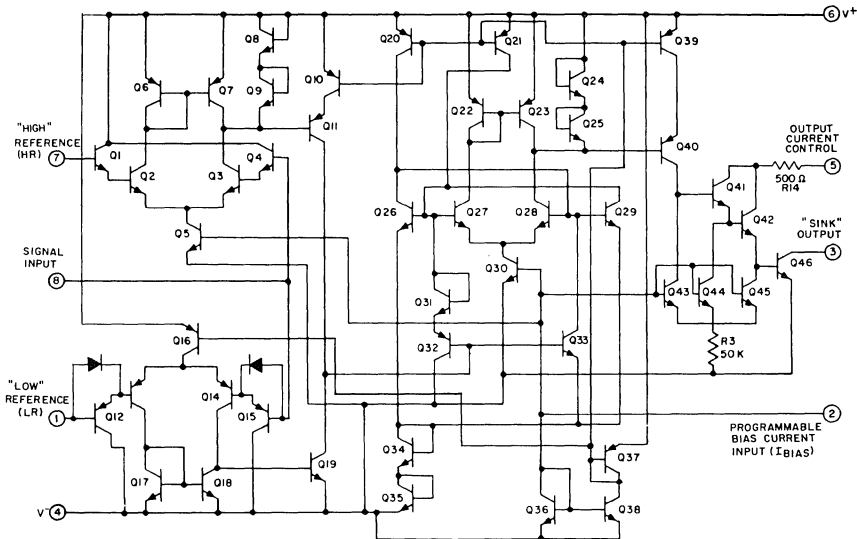


Fig. 2 - Schematic diagram of CA3098.

**General Description of Circuit Operation**  
(Refer to Figs. 2, 3, 4)

When the signal-input voltage of the CA3098 is equal to or less than the "low" reference voltage (LR), current flows from an external power supply through a load connected to terminal 3 ("sink" output). This condition is maintained until the signal-input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop (memory) such that the output stage interrupts current flow in the external load. This condition, in turn, is maintained until such time as the signal again becomes equal to or less than the "low" reference voltage (VR).

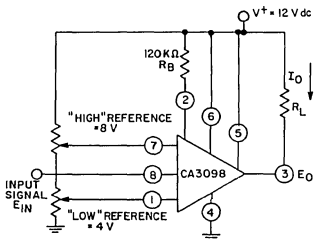


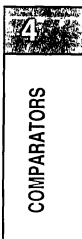
Fig. 3 - Basic hysteresis switch (Schmitt trigger).

The CA3098 comparator is unique in that it contains circuit provisions to permit programmability. This feature provides flexibility to the designer to optimize quiescent power consumption, input-circuit characteristics, hysteresis, and additionally permits independent control of the comparator, namely, pulsing, strobing, keying, squelching, etc. Programmability is accomplished by means of the bias current ( $I_{bias}$ ) supplied to terminal 2.

An auxiliary means of controlling the magnitude of load-current flow at terminal 3 is provided by "sinking" current into terminal 5. Figs 3 and 4 highlight the operation of the CA3098 when connected as a simple hysteresis switch (Schmitt trigger).

| Sequence | Input Signal Level  | Output Voltage (V)<br>(Term. 3) |
|----------|---------------------|---------------------------------|
| 1        | $4 \geq E_{IN} > 0$ | 0                               |
| 2        | $8 \geq E_{IN} > 4$ | 0                               |
| 3        | $E_{IN} > 8$        | 12                              |
| 2        | $8 \geq E_{IN} > 4$ | 12                              |
| 1        | $4 \geq E_{IN} > 0$ | 0                               |

Fig. 4 - Resultant output states of the CA3098, shown in Fig. 3 as a function of various input signal levels.



**TYPICAL CHARACTERISTIC CURVES**

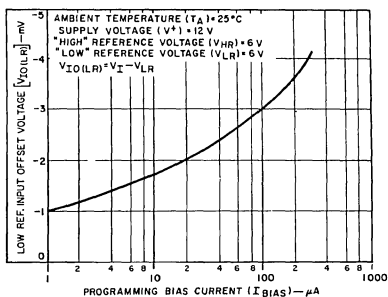


Fig. 5 - Input-offset voltage ("low" reference) vs. programming bias current.

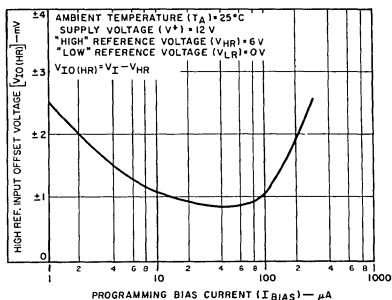


Fig. 6 - Input-offset voltage ("high" reference) vs. programming bias current.

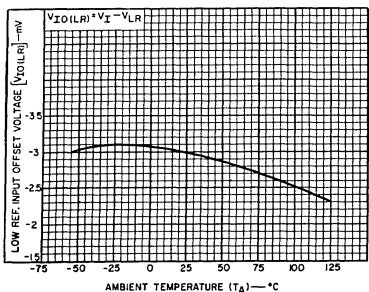


Fig. 7 - Input-offset voltage ("low" reference) vs. ambient temperature.

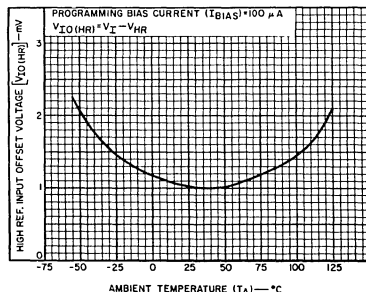


Fig. 8 - Input-offset voltage ("high" reference) vs. ambient temperature.

TYPICAL CHARACTERISTIC CURVES (Cont'd)

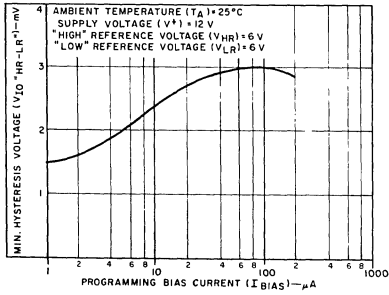


Fig. 9 - Min. hysteresis voltage vs. programming bias current.

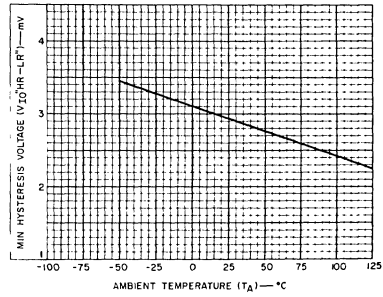


Fig. 10 - Min. hysteresis voltage vs. ambient temperature.

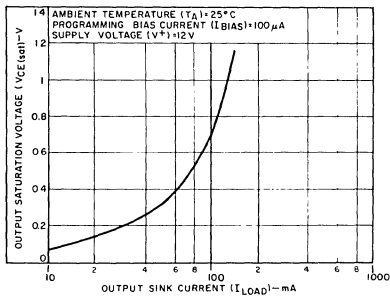


Fig. 11 - Output saturation voltage vs. output sink current.

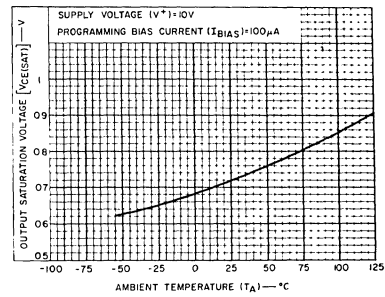


Fig. 12 - Output saturation voltage vs. ambient temperature.

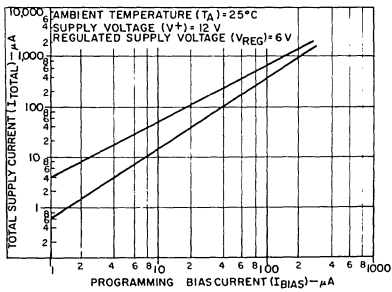


Fig. 13 - Total supply current vs. programming bias current.

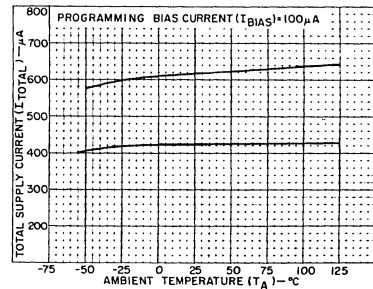


Fig. 14 - Total supply current vs. ambient temperature.

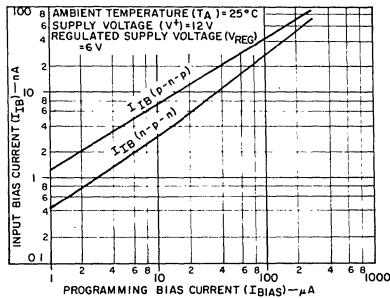


Fig. 15 - Input bias current vs. programming bias current.

# CA3098

## TEST CIRCUITS

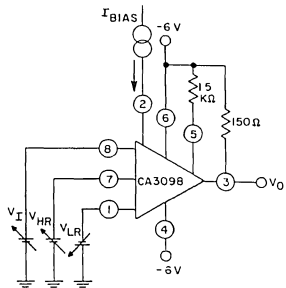
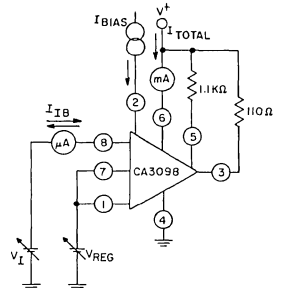


Fig. 16 - Input-offset voltage test circuit.



HYSTERESIS VOLTAGE =  $V_I$  "OFF" -  $V_I$  "ON"

Fig. 17 - Min. hysteresis voltage, total supply current, and input-bias-current test circuit.

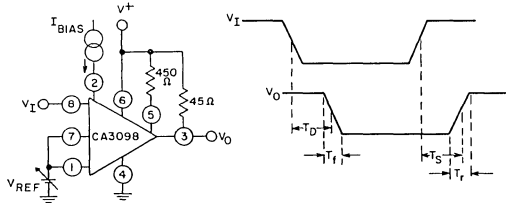


Fig. 18 - Switching time test circuit.

## TYPICAL APPLICATIONS

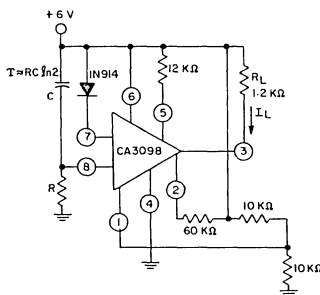


Fig. 19 - Time delay circuit: Terminal 3 "sinks" after  $\tau$  seconds.

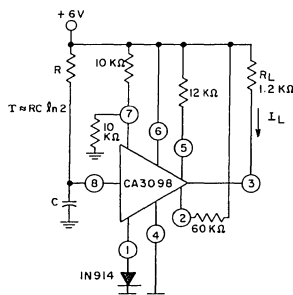


Fig. 20 - Time delay circuit: "sink" current interrupted after  $\tau$  seconds.

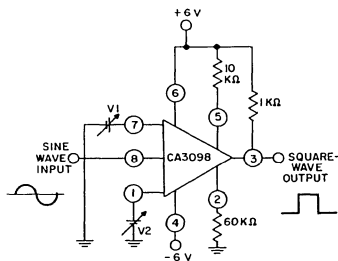
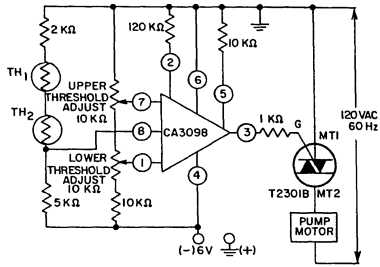


Fig. 21 - Sine-wave to square-wave converter with duty-cycle adjustment ( $V_1$  and  $V_2$ ).



# CA3098

## TYPICAL APPLICATIONS (Cont'd)



- Notes**
- (a) Motor pump is "ON" when water level rises above thermistor TH<sub>2</sub>.
  - (b) Motor pump remains "ON" until water level falls below thermistor TH<sub>1</sub>.
  - (c) Thermistors, operate in self-heating mode.

Fig. 22(a) - Water-level control.

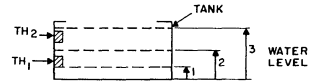


Fig. 22(b) - Water level diagram for circuit of Fig. 22(a).

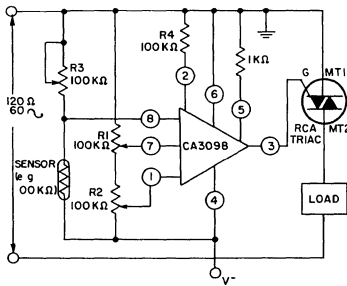


Fig. 23 - OFF/ON control of triac with programmable hysteresis.

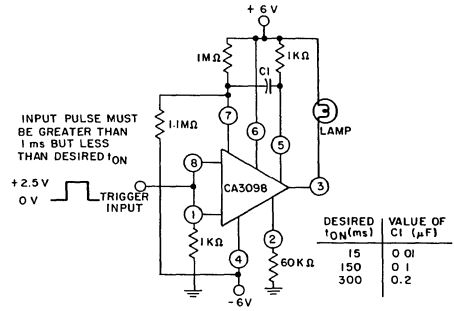
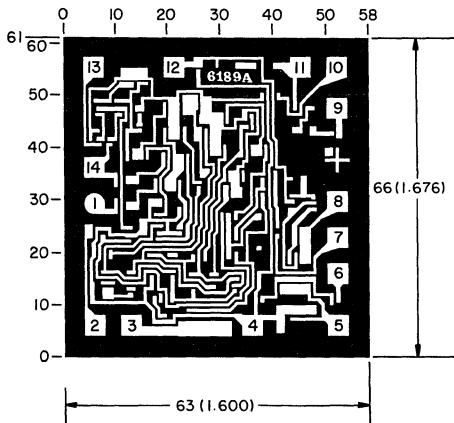


Fig. 24 - One-shot multivibrator.



Dimensions and pad layout for the CA3098H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are  $57^\circ$  instead of  $90^\circ$  with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

# CA3290A CA3290

## BiMOS Dual Voltage Comparator With MOSFET Input, Bipolar Output

August 1991

### Features

- MOSFET Input Stage
  - ▶ Very High Input Impedance ( $Z_{IN}$ ) . . . . . 1.7 T $\Omega$  (Typ)
  - ▶ Very Low Input Current @  $V_+ = +5V$  . . . . . 3.5pA (Typ)
  - ▶ Wide Common Mode Input Voltage Range ( $V_{ICR}$ ) - can be Swung 1.5V (Typ) Below Negative Supply - Voltage Rail
  - ▶ Virtually Eliminates Errors Due to Flow of Input Currents
- Output Voltage Compatible with TTL, DTL, ECL, MOS, and CMOS Logic Systems in Most Applications

### Applications

- High Source Impedance Voltage Comparators
- Long Time Delay Circuits
- Square Wave Generators
- A/D Converters
- Window Comparators

### Description

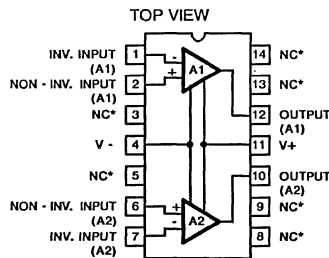
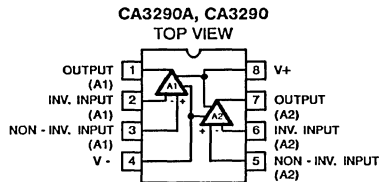
The CA3290A and CA3290 types consist of a dual voltage comparator on a single monolithic chip. The common mode input voltage range includes ground even when operated from a single supply. The low supply current drain makes these comparators suitable for battery operation; their extremely low input currents allow their use in applications that employ sensors with extremely high source impedances. Package options are shown in the table below.

### Selection Chart

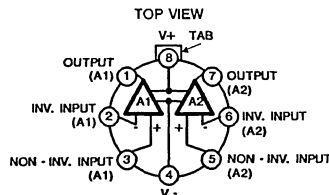
| SELECTION | CHARACTERISTIC    |                |              |           | PACKAGE AND SUFFIX |         |         |         |
|-----------|-------------------|----------------|--------------|-----------|--------------------|---------|---------|---------|
|           | MAX $V_{IO}$ (mV) | MAX $I_j$ (pA) | MIN $A_{OL}$ | $V_+$ (V) | TO-5               |         | PLASTIC |         |
|           |                   |                |              |           | STD                | DIL-CAN | 8-LEAD  | 14-LEAD |
| CA3290A   | 10                | 40             | 25K          | 36        | T                  | S       | E       | E1      |
| CA3290    | 20                | 50             | 25K          | 36        | T                  | S       | E       | E1      |

The CA3290 is also available in chip form (H suffix)

### Pinouts



\* Tie to GND or  $V_+$  for best Input/Output isolation



### Basic CA3290 Comparator

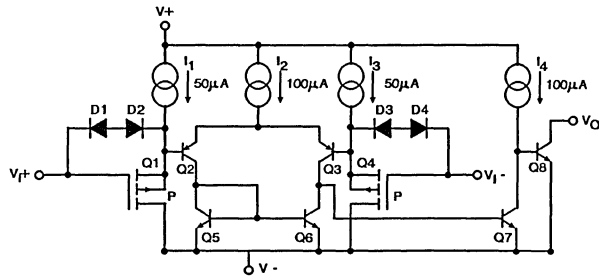


FIGURE 1.

# CA3290A, CA3290

## MAXIMUM RATINGS, *Absolute-Maximum Values:*

|  |  |
|--|--|
| DC SUPPLY VOLTAGE:                               |  |
| Single Supply:                                   |  |
| CA3290A, CA3290                                  | ..... +36 V  |
| Dual Supply:                                     |  |
| CA3290A, CA3290                                  | ..... ±18 V  |
| DIFFERENTIAL INPUT VOLTAGE                       | ..... ±36 V or ±[(V <sup>+</sup> -V <sup>-</sup> )+5 V]<br>(whichever is less) |
| COMMON-MODE INPUT VOLTAGE                        | ..... V <sup>+</sup> +5 V to V <sup>-</sup> -5 V                               |
| DEVICE DISSIPATION:                              |  |
| Up to 55°C                                       | ..... 630 mW   |
| Above 55°C                                       | ..... Derate linearly at 6.67 mW/°C  |
| OUTPUT-TO-V <sup>-</sup> SHORT CIRCUIT DURATION* | ..... CONTINUOUS   |
| TEMPERATURE RANGE, ALL TYPES:                    |  |
| Operating  | ..... -55 to +125°C  |
| Storage  | ..... -65 to +150°C  |
| INPUT TERMINAL CURRENT                           |  |
| LEAD TEMPERATURE (DURING SOLDERING):             |  |
| AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM)    |  |
| FROM CASE FOR 10 SECONDS MAX.                    | ..... 265°C  |

\*Short circuits from the output to V<sup>-</sup> can cause excessive heating and eventual destruction of the device.

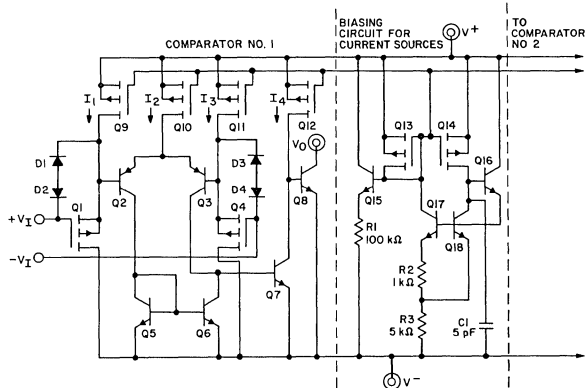


Fig. 2 — Schematic diagram of CA3290 (only one is shown).

## CIRCUIT DESCRIPTION

### The Basic Comparator

Fig. 1 shows the basic circuit diagram for one of the two comparators in the CA3290. It is generically similar to the industry-type "139" comparators, with PMOS transistors replacing p-n-p transistors as input stage elements. Transistors Q1 through Q4 comprise the differential input stage, with Q5 and Q6 serving as a mirror-connected active load and differential-to-single-ended converter. The differential input at Q1 and Q4 is amplified so as to toggle Q6 in accordance with the input-signal polarity. For example, if +V<sub>IN</sub> is greater than -V<sub>IN</sub>, Q1, Q2, and current mirror transistors Q5 and Q6 will be turned off; transistors Q3, Q4, and Q7 will be turned on, causing Q8 to be turned off.

The output is pulled positive when a load resistor is connected between the output and V<sup>+</sup>.

In essence, Q1 and Q4 function as source-followers to drive Q2 and Q3, respectively, with zener diodes D1 through D4 providing gate-oxide protection against input voltage transients (e.g., static electricity). The current flow in Q1 and Q2 is established at approximately 50 microamperes by constant-current sources I1 and I3, respectively. Since Q1 and Q4 are operated with a constant current load, their gate-to-source voltage drops will be effectively constant as long as the input voltages are within the common-mode range.

## CA3290A, CA3290

As a result, the input offset voltage ( $V_{GS(Q11)} + V_{BE(Q2)} - V_{BE(Q3)} - V_{GS(Q4)}$ ) will not be degraded when a large differential dc voltage is applied to the device for extended periods of time at high temperatures.

Additional voltage gain following the first stage is provided by transistors Q7 and Q8. The collector of Q8 is open, offering the user a wide variety of options in applications. An additional discrete transistor can be added if it becomes necessary to boost the output sink-current capability.

The detailed schematic diagram for one comparator and the common current-source biasing is shown in Fig. 2. PMOS transistors Q9 through Q12 are the current-source elements identified in Fig. 1 as I<sub>1</sub> through I<sub>4</sub>, respectively. Their gate-source potentials ( $V_{GS}$ ) are supplied by a common bus from the biasing circuit shown in the right-hand portion of the Fig. 2. The currents supplied by Q10 and Q12 are twice those supplied by Q9 and Q11. The transistor geometries are appropriately scaled to provide the requisite currents with common  $V_{GS}$  applied to Q9 through Q12.

ELECTRICAL CHARACTERISTICS at  $T_A = -55$  to  $+125^\circ\text{C}$

| CHARACTERISTIC  | TEST CONDITIONS  |                      | VALUES  |      |        |      | UNITS                        |
|---|--|----------------------|---------|------|--------|------|------------------------------|
|   |  |                      | CA3290A |      | CA3290 |      |                              |
|   |  | V <sup>+</sup>       | Typ.    | Max. | Typ.   | Max. |                              |
| Input Offset Voltage, $V_{IO}$                                      | $V_{CM}=1.4\text{ V}$ ,<br>$V_O=1.4\text{ V}$                  | 5 V                  | 4.5     | —    | 8.5    | —    | mV                           |
|   | $V_{CM}=0\text{ V}$ ,<br>$V_O=0\text{ V}$                      | $\pm 15\text{ V}$    | 8.5     | —    | 8.5    | —    |                              |
| Temp. Coefficient of Input Offset Voltage, $\Delta V_{IO}/\Delta T$ |  |                      | 8       | —    | 8      | —    | $\mu\text{V}/^\circ\text{C}$ |
| Input Offset Current, $I_{IO}$                                      | $V_{CM}=1.4\text{ V}$  | 5 V                  | 2       | 28   | 2      | 32   | nA                           |
|   | $V_{CM}=0\text{ V}$  | $\pm 15\text{ V}$    | 7       | 28   | 7      | 32   |                              |
| Input Current, $I_I^\Delta$   | $V_{CM}=1.4\text{ V}$  | 5 V                  | 2.8     | 45   | 2.8    | 55   | nA                           |
|   | $V_{CM}=0\text{ V}$  | $\pm 15\text{ V}$    | 13      | 45   | 13     | 55   |                              |
| Supply Current, $I^{+*}$  | $R_L = \infty$   | 5 V                  | 0.85    | 1    | 0.85   | 1.6  | mA                           |
|   |  | 30 V                 | 1.62    | 3    | 1.62   | 3.5  |                              |
| Voltage Gain, $A_{OL}$  | $R_L = 15\text{ k}\Omega$                                      | $\pm 15\text{ V}$    | 150     | —    | 150    | —    | V/mV                         |
|   |  |                      | 103     | —    | 103    | —    | dB                           |
| Saturation Voltage<br>$I_{SINK} = 4\text{ mA}$                      | $V^+=5\text{ V}$ ,<br>$+V_I=0\text{ V}$ ,<br>$-V_I=1\text{ V}$ | $+125^\circ\text{C}$ | 0.22    | 0.7  | 0.22   | 0.7  | V                            |
|   |  | $-55^\circ\text{C}$  | 0.1     | —    | 0.1    | —    |                              |
| Output Leakage Current, $I_{OL}$                                    |  | 15 V                 | 65      | —    | 65     | —    | nA                           |
|   |  | 36 V                 | 130     | 1k   | 130    | 1k   |                              |

$^\Delta$  At  $T_A = +125^\circ\text{C}$

\* At  $T_A = -55^\circ\text{C}$

**CA3290A, CA3290**

**ELECTRICAL CHARACTERISTICS AT  $T_A = 25^\circ\text{C}$**

| CHARACTERISTIC   | TEST COND.<br>$V^+$                     | LIMITS               |                            |                            |                      |                            |                            | UNITS           |
|--|---|----------------------|----------------------------|----------------------------|----------------------|----------------------------|----------------------------|-----------------|
|  |   | CA3290A              |                            |                            | CA3290               |                            |                            |                 |
|  |   | Min.                 | Typ.                       | Max.                       | Min.                 | Typ.                       | Max.                       |                 |
| Input Offset Voltage, $V_{IO}$<br>$V_{CM}=1.4\text{ V}$<br>$V_O=1.4\text{ V}$                | 5 V                                     | –                    | 4                          | 10                         | –                    | 7.5                        | 20                         | mV              |
|  | $V_{CM}=0\text{ V}$<br>$V_O=0\text{ V}$ | $\pm 15\text{ V}$    | –                          | 4                          | 10                   | –                          | 7.5                        |                 |
| Input Current, $I_I$<br>$V_{CM}=1.4\text{ V}$  | 5 V                                     | –                    | 3.5                        | 40                         | –                    | 3.5                        | 50                         | pA              |
|  | $V_{CM}=0\text{ V}$                     | $\pm 15\text{ V}$    | –                          | 12                         | 40                   | –                          | 12                         |                 |
| Input Offset Current, $I_{IO}$<br>$V_{CM}=1.4\text{ V}$                                      | 5 V                                     | –                    | 2                          | 25                         | –                    | 2                          | 30                         | pA              |
|  | $V_{CM}=0\text{ V}$                     | $\pm 15\text{ V}$    | –                          | 7                          | 25                   | –                          | 7                          |                 |
| Common-Mode Input-Voltage Range, $V_{ICR}$<br>$V_O=1.4\text{ V}$                             | 5 V                                     | $V^+ - 3.5$<br>$V^-$ | $V^+ - 3.1$<br>$V^- - 1.5$ | –                          | $V^+ - 3.5$<br>$V^-$ | $V^+ - 3.1$<br>$V^- - 1.5$ | –                          | V               |
|  | $V_O=0\text{ V}$                        | $\pm 15\text{ V}$    | $V^+ - 3.8$<br>$V^-$       | $V^+ - 3.4$<br>$V^- - 1.6$ | –                    | $V^+ - 3.8$<br>$V^-$       | $V^+ - 3.4$<br>$V^- - 1.6$ |                 |
| Supply Current, $I^+$<br>$R_L = \infty$  | 30 V                                    | –                    | 1.35                       | 3                          | –                    | 1.35                       | 3                          | mA              |
|  | 5 V                                     | –                    | 0.8                        | 1.4                        | –                    | 0.8                        | 1.4                        |                 |
| Voltage Gain, $A_{OL}$<br>$R_L = 15\text{ k}\Omega$  | $\pm 15\text{ V}$                       | 25                   | 800                        | –                          | 25                   | 800                        | –                          | V/mV            |
|  |   | 88                   | 118                        | –                          | 88                   | 118                        | –                          | dB              |
| Output Sink Current<br>$V_O=1.4\text{ V}$  | 5 V                                     | 6                    | 30                         | –                          | 6                    | 30                         | –                          | mA              |
| Saturation Voltage<br>$+V_I=0\text{ V}$ ,<br>$-V_I=1\text{ V}$ ,<br>$I_{SINK} = 4\text{ mA}$ | 5 V                                     | –                    | 0.12                       | 0.4                        | –                    | 0.12                       | 0.4                        | V               |
| Output Leakage Current, $I_{OL}$   | 15 V                                    | –                    | 100                        | –                          | –                    | 100                        | –                          | pA              |
|  | 36 V                                    | –                    | 500                        | –                          | –                    | 500                        | –                          |                 |
| Response Time<br>$R_L=5.1\text{ k}\Omega$<br>Rising Edge                                     | 15 V                                    | –                    | 1.2                        | –                          | –                    | 1.2                        | –                          | $\mu\text{s}$   |
|  |   | Falling Edge         | –                          | 200                        | –                    | –                          | 200                        | –               |
| Common-Mode Rejection Ratio, CMRR  | $\pm 15\text{ V}$                       | –                    | 44                         | 562                        | –                    | 44                         | 562                        | $\mu\text{V/V}$ |
|  | 5 V                                     | –                    | 100                        | 562                        | –                    | 100                        | 562                        |                 |
| Power-Supply Rejection Ratio, PSRR   | $\pm 15\text{ V}$                       | –                    | 15                         | 316                        | –                    | 15                         | 316                        | $\mu\text{V/V}$ |
| Large-Signal Response Time<br>$R_L=5.1\text{ k}\Omega$                                       | 15 V                                    | –                    | 500                        | –                          | –                    | 500                        | –                          | ns              |
|  | 5 V                                     | –                    | 400                        | –                          | –                    | 400                        | –                          |                 |

# CA3290A, CA3290

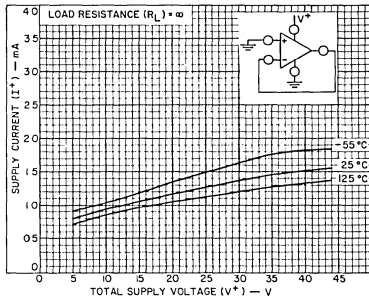


Fig. 3 — Supply current as a function of supply voltage (both amplifiers).

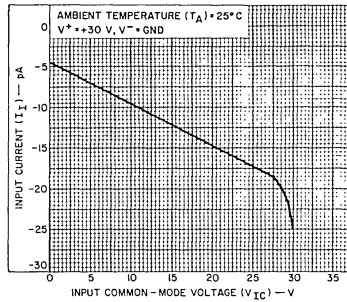


Fig. 4 — Input current as a function of input common-mode voltage.

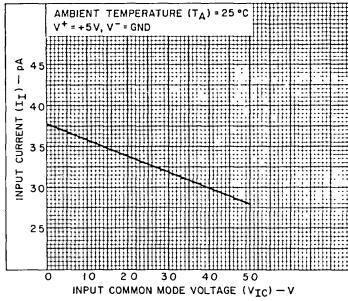


Fig. 5 — Input current as a function of input common-mode voltage.

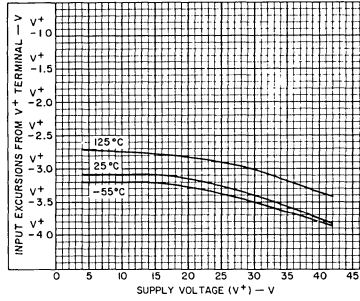


Fig. 6 — Positive common-mode input voltage range as a function of supply voltage.

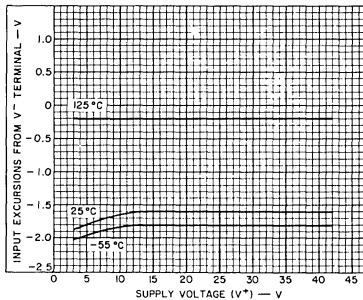


Fig. 7 — Negative common-mode input voltage range as a function of supply voltage.

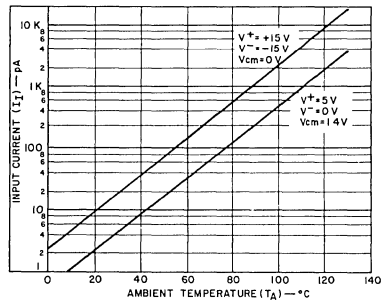


Fig. 8 — Input current as a function of ambient temperature.

# CA3290A, CA3290

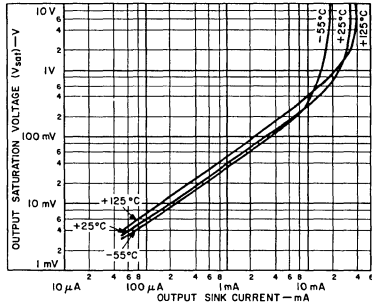
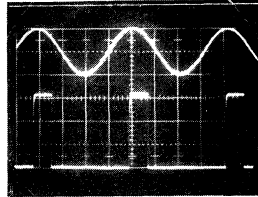
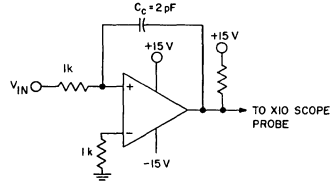


Fig. 9 — Output saturation voltage as a function of output sink current.



WITH C<sub>c</sub>  
 TOP TRACE ≈ 4.5 mV/DIV = V<sub>IN</sub>  
 BOTTOM TRACE = 10 V/DIV = V<sub>OUT</sub>  
 H = 5 μs/DIV

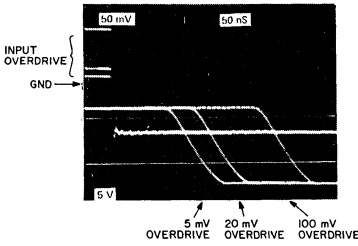
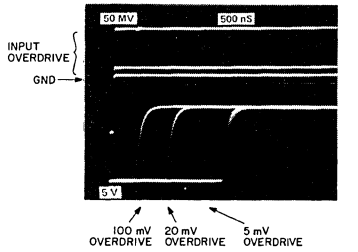
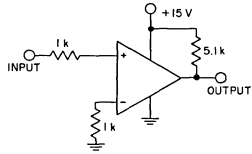
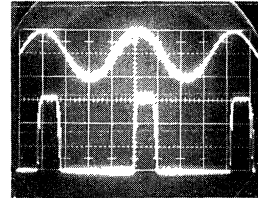


Fig. 11 — Non-inverting comparator response-time test circuit and waveforms.



WITHOUT C<sub>c</sub>  
 TOP TRACE ≈ 4.5 mV/DIV  
 BOTTOM TRACE = 10 V/DIV  
 H = 5 μs/DIV

Fig. 10 — Parasitic-oscillations test circuit and associated waveforms.

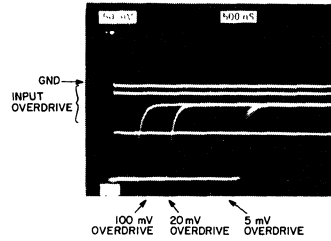
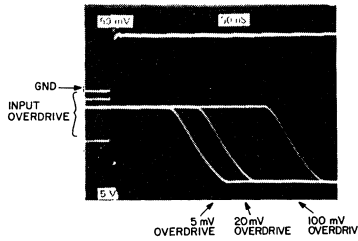
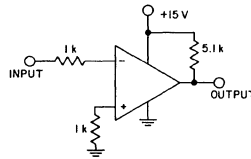


Fig. 12 — Inverting comparator response-time test circuit and waveforms.

## CA3290A, CA3290

### OPERATING CONSIDERATIONS

#### Input Circuit

The use of MOS transistors in the input stage of the CA3290 series circuits provides the user with the following features for comparator applications:

1. Ultra-high input impedance ( $\cong 1.7 \text{ T}\Omega$ );
2. The availability of common-mode rejection for input signals at potentials below that of the negative power-supply rail;
3. Retention of the in-phase relationship of the input and output signals for input signals below the negative rail.

Although the CA3290 employs rugged bipolar (zener) diodes for protection of the input circuit, the input-terminal currents should not exceed 1 mA. Appropriate series-connected limiting resistors should be used in circuits where greater current flows might exist, allowing the signal input voltage to be greater than the supply voltage without damaging the circuit.

#### Output Circuit

The output of the CA3290 is the open collector of an n-p-n transistor, a feature providing flexibility in a broad range of comparator applications. An output ORing function can be implemented by parallel-connection of the open collectors. An output pull-up resistor can be connected to a power supply having a voltage range within the rating of the particular CA3290 in use; the magnitude of this voltage may be set at a value which is independent of that applied to the  $V^+$  terminal of the CA3290.

#### Parasitic Oscillations

The ideal comparator has, among other features, ultra-high input impedance, high gain, and wide bandwidth. These desirable characteristics may, however, produce parasitic oscillations unless certain precautions are observed to minimize the stray capacitive

coupling between the input and output terminals. Parasitic oscillations manifest themselves during the output voltage transition intervals as the comparator switches states. For high source impedances, stray capacitance can induce parasitic oscillations. The addition of a small amount (1 to 10 mV) of positive feedback (hysteresis) produces a faster transition, thereby reducing the likelihood of parasitic oscillations. Furthermore, if the input signal is a pulse waveform, with relatively rapid rise and fall times, parasitic tendencies are reduced.

When dual comparators, like the CA3290, are packaged in an 8-lead configuration, the output terminal of each comparator is adjacent to an input terminal. The lead-to-lead capacitance is approximately 1 pF, which may be sufficient to cause undesirable feedback effects in certain applications. Circuit factors such as impedance levels, supply voltage, toggling rate, etc., may increase the possibility of parasitic oscillations. To minimize this potential oscillatory condition, it is recommended that for source impedances greater than 1 k $\Omega$  a capacitor ( $\cong 1\text{-}2 \text{ pF}$ ) be connected between the appropriate input terminal and the output terminal. (See Fig. 10.)

The CA3290A and CA3290 are also supplied in a 14-lead dual-in-line plastic package. To minimize the possibility of parasitic oscillations the input and output terminals are positioned on opposite sides of the package. In addition, there are two leads between the output terminal of each comparator and its corresponding inverting input terminal, reducing the input/output coupling significantly. These leads (8, 9, 13, 14) should be tied to either the  $V^+$  or  $V^-$  supply rail. If either comparator is unused, its input terminals should also be tied to either the  $V^+$  or  $V^-$  supply rail.

### TYPICAL APPLICATIONS

#### Light-Controlled One-Shot Timer

In Fig. 13 one comparator (A1) of the CA3290 is used to sense a change in photo diode current. The other comparator (A2) is configured as a one-shot timer and is triggered by the output of A1. The output of the circuit will switch to a low state for approximately 60 seconds after the light source to the photo diode has been interrupted. The circuit operates at normal room lighting levels. The sensitivity of the circuit may be adjusted by changing the values of R1 and R2. The ratio of R1 to R2 should be

constant to insure constant reverse voltage bias on the photo diode.

#### Low-Frequency Multivibrator

In this application, one-half of the CA3290 is used as a conventional multivibrator circuit. Because of the extremely high input impedance of this device, large values of timing resistor (R1) may be used for long time delays with relatively small leakage timing capacitors. The second half of the CA3290 is used as an output buffer to insure that the multivibrator frequency will not be affected by output loading.



## CA3290A, CA3290

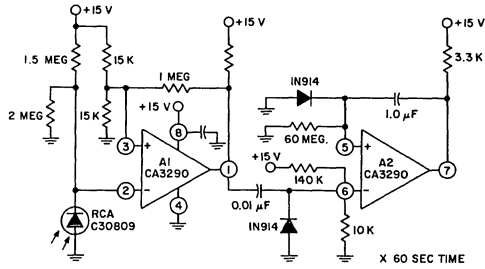


Fig. 13 – Light-controlled one-shot timer.

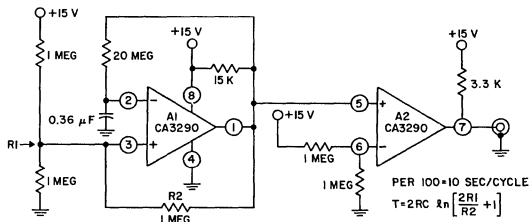


Fig. 14 – Low-frequency multivibrator.

### Window Comparator

Both halves of the CA3290 can be used in a high input-impedance window comparator as shown in Fig. 15. The LED will be

turned "on" whenever the input signal is above the lower limit ( $V_L$ ) but below the upper limit ( $V_U$ ), as determined by the  $R_1/R_2/R_3$  resistor divider.

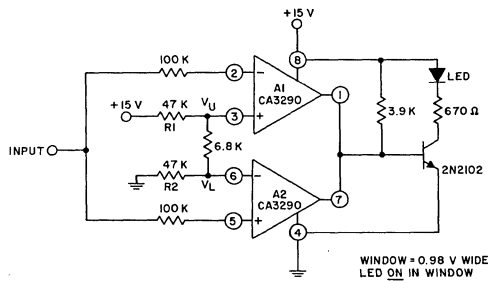


Fig. 15 – Window comparator.

# CA3290A, CA3290

## LED Bar Graph Driver

The circuit in Fig. 16 demonstrates the use of the CA3290 in a bar graph display. The non-inverting inputs of both comparators are tied to the voltage divider reference and the input signal is applied to both of the

inverting inputs. The LED for a particular comparator will be turned "on" when the input voltage reaches the voltage on the resistor divider reference. The CA3290 is ideal for this application where input-signal loading is critical even though many comparator inputs are driven in parallel.

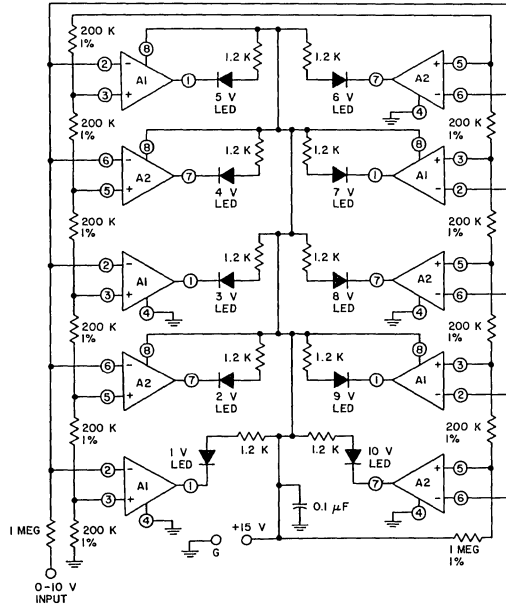
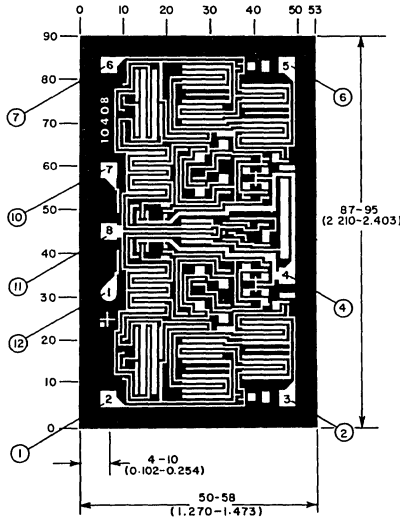


Fig. 16 — LED bar-graph driver.



NOTE: NOS. IN PADS ARE FOR 8-LEAD DIP AND TO-5 NOS. OUTSIDE OF CHIP ARE FOR 14-LEAD DIP

92CM-30091

Dimensions and pad layout for the CA3290H.

The photographs and dimensions of each chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10<sup>-3</sup> inch).

May 1990

## Precision Quad Comparator

### Features

- Fast Response Time ..... 130ns
- Low Offset Voltage ..... 2.0mV
- Low Offset Current ..... 10nA
- Single or Dual-Voltage Supply Operation
- Selectable Output Logic Levels
- Active Pull-Up/Pull-Down Output Circuit-No External Resistors Required

### Applications

- Threshold Detector
- Zero-Crossing Detector
- Window Detector
- Analog Interfaces for Microprocessors
- High Stability Oscillators
- Logic System Interfaces

### Description

The HA-4900 series are monolithic, quad, precision comparators offering fast response time, low offset voltage, low offset current and virtually no channel-to-channel crosstalk for applications requiring accurate, high speed, signal level detection. These comparators can sense signals at ground level while being operated from either a single +5 volt supply (digital systems) or from dual supplies (analog networks) up to  $\pm 15$ volts. The HA-4900 series contains a unique current driven output stage which can be connected to logic system supplies ( $V_{Logic+}$  and  $V_{Logic-}$ ) to make the output levels directly compatible (no external components needed) with any standard logic or special system logic levels. In combination analog/digital systems,

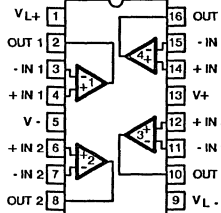
the design employed in the HA-4900 series input and output stages prevents troublesome ground coupling of signals between analog and digital portions of the system.

These comparators' combination of features makes them ideal components for signal detection and processing in data acquisition systems, test equipment and microprocessor/analog signal interface networks.

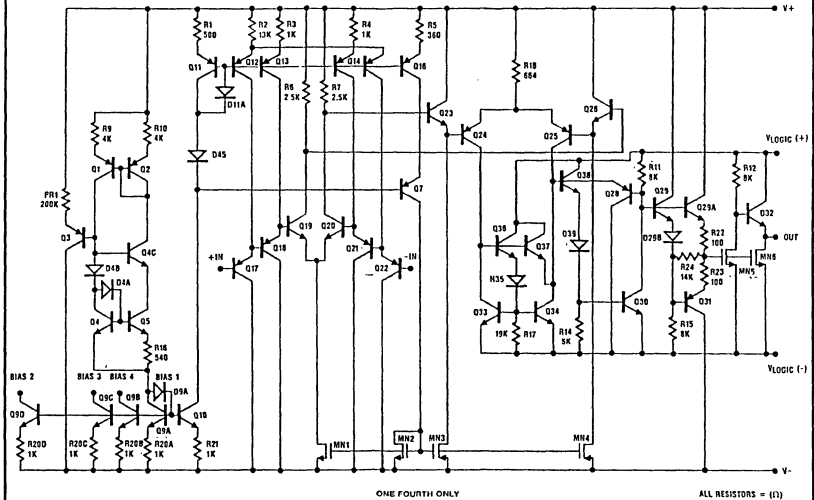
All devices are available in 16 pin dual-in-line ceramic packages. The HA-4900/4902-2 operates from  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  and the HA-4905-5 operates over a  $0^{\circ}\text{C}$  to  $+75^{\circ}\text{C}$  temperature range. For military grade product, refer to the HA-4902/883 data sheet.

### Pinouts

HA1-4900/02/05  
(CERAMIC DIP)  
TOP VIEW



### Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.  
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File Number **2855**

**Absolute Maximum Ratings** (Note 1)

Voltage Between V+ and V- Terminals ..... 33V  
 Differential Input Voltage ..... ±15V  
 Voltage Between V<sub>Logic</sub> (+) and V<sub>Logic</sub> (-) ..... 18V  
 Peak Output Current ..... ±50mA  
 Internal Power Dissipation (Note 7, 8) ..... 2.0W

**Operating Temperature Ranges**

HA-4900-2 ..... -55°C ≤ T<sub>A</sub> ≤ +125°C  
 HA-4902-2 ..... -55°C ≤ T<sub>A</sub> ≤ +125°C  
 HA-4905-5 ..... 0°C ≤ T<sub>A</sub> ≤ +75°C  
 Storage Temperature Range: ..... -65°C ≤ T<sub>A</sub> ≤ +150°C

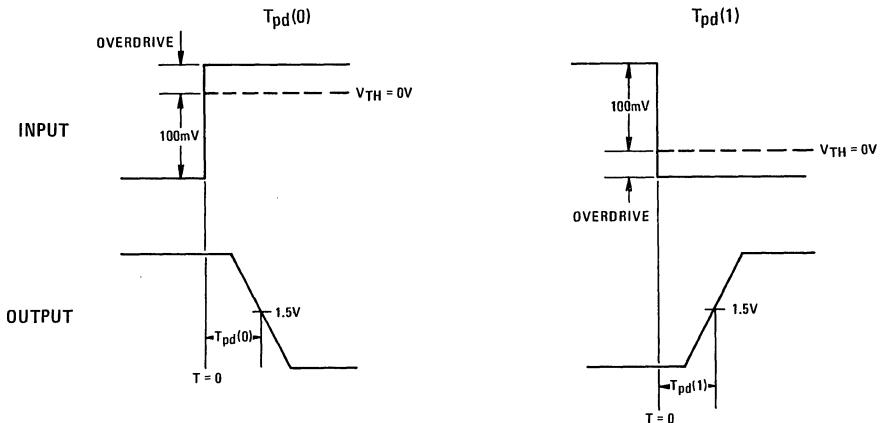
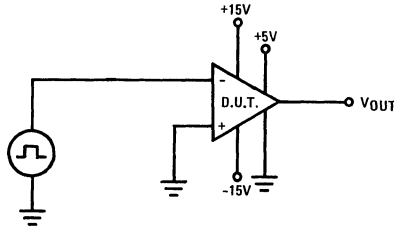
**Electrical Specifications** V+ = +15V, V- = -15V, V<sub>Logic</sub> (+) = 5V, V<sub>Logic</sub> (-) = GND.

| PARAMETER                                      | TEMP  | HA-4900-2<br>-55°C to +125°C |      |                     | HA-4902-2<br>-55°C to +125°C |      |                     | HA-4905-5<br>0°C to +75°C |      |                     | UNITS |
|--|-------|------------------------------|------|---------------------|------------------------------|------|---------------------|---------------------------|------|---------------------|-------|
|  |       | MIN                          | TYP  | MAX                 | MIN                          | TYP  | MAX                 | MIN                       | TYP  | MAX                 |       |
| <b>INPUT CHARACTERISTICS</b>                   |       |                              |      |                     |                              |      |                     |                           |      |                     |       |
| Offset Voltage (Note 2)                        | +25°C |                              | 2    | 3                   |                              | 2    | 5                   |                           | 4    | 7.5                 | mV    |
|  | Full  |                              |      | 4                   |                              |      | 8                   |                           |      | 10                  | mV    |
| Offset Current                                 | +25°C |                              | 10   | 25                  |                              | 10   | 35                  |                           | 25   | 50                  | nA    |
|  | Full  |                              |      | 35                  |                              |      | 45                  |                           |      | 70                  | nA    |
| Bias Current (Note 3)                          | +25°C |                              | 50   | 75                  |                              | 50   | 150                 |                           | 100  | 150                 | nA    |
|  | Full  |                              |      | 150                 |                              |      | 200                 |                           |      | 300                 | nA    |
| Input Sensitivity (Note 4)                     | +25°C |                              |      | V <sub>IO</sub> +.3 |                              |      | V <sub>IO</sub> +.5 |                           |      | V <sub>IO</sub> +.5 | mV    |
|  | Full  |                              |      | V <sub>IO</sub> +.4 |                              |      | V <sub>IO</sub> +.6 |                           |      | V <sub>IO</sub> +.7 | mV    |
| Common Mode Range                              | Full  | V-                           |      | (V+)-2.4            | V-                           |      | (V+)-2.6            | V-                        |      | (V+)-2.4            | V     |
| Differential Input Resistance                  | +25°C |                              | 250  |                     |                              | 250  |                     |                           | 250  |                     | MΩ    |
| <b>TRANSFER CHARACTERISTICS</b>                |       |                              |      |                     |                              |      |                     |                           |      |                     |       |
| Large Signal Voltage Gain                      | +25°C |                              | 400K |                     |                              | 400K |                     |                           | 400K |                     | V/V   |
| Response Time (T <sub>pd0</sub> ) (Note 5)     | +25°C |                              | 130  | 200                 |                              | 130  | 200                 |                           | 130  | 200                 | ns    |
| Response Time (T <sub>pd1</sub> ) (Note 5)     | +25°C |                              | 180  | 215                 |                              | 180  | 215                 |                           | 180  | 215                 | ns    |
| <b>OUTPUT CHARACTERISTICS</b>                  |       |                              |      |                     |                              |      |                     |                           |      |                     |       |
| Output Voltage Level                           |       |                              |      |                     |                              |      |                     |                           |      |                     |       |
| Logic "Low State" (V <sub>OL</sub> ) (Note 6)  | Full  |                              | 0.2  | 0.4                 |                              | 0.2  | 0.4                 |                           | 0.2  | 0.4                 | V     |
| Logic "High State" (V <sub>OH</sub> ) (Note 6) | Full  | 3.5                          | 4.2  |                     | 3.5                          | 4.2  |                     | 3.5                       | 4.2  |                     | V     |
| Output Current                                 |       |                              |      |                     |                              |      |                     |                           |      |                     |       |
| I <sub>Sink</sub>                              | Full  |                              | 3.0  |                     | 3.0                          |      |                     | 3.0                       |      |                     | mA    |
| I <sub>Source</sub>                            | Full  |                              | 3.0  |                     | 3.0                          |      |                     | 3.0                       |      |                     | mA    |
| <b>POWER SUPPLY CHARACTERISTICS</b>            |       |                              |      |                     |                              |      |                     |                           |      |                     |       |
| Supply Current, I <sub>PS</sub> (+)            | +25°C |                              | 6.5  | 20                  |                              | 6.5  | 20                  |                           | 7    | 20                  | mA    |
| Supply Current, I <sub>PS</sub> (-)            | +25°C |                              | 4    | 8                   |                              | 4    | 8                   |                           | 5    | 8                   | mA    |
| Supply Current, I <sub>PS</sub> (Logic)        | +25°C |                              | 3.5  | 4                   |                              | 3.5  | 4                   |                           | 3.5  | 4                   | mA    |
| Supply Voltage Range                           |       |                              |      |                     |                              |      |                     |                           |      |                     |       |
| V <sub>Logic</sub> (+) (Note 7)                | Full  | 0                            |      | +15.0               | 0                            |      | +15.0               | 0                         |      | +15.0               | V     |
| V <sub>Logic</sub> (-) (Note 7)                | Full  | -15.0                        |      | 0                   | -15.0                        |      | 0                   | -15.0                     |      | 0                   | V     |

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Minimum differential input voltage required to ensure a defined output state.
3. Input bias currents are essentially constant with differential input voltages up to  $\pm 9$  volts. With differential input voltages from  $\pm 9$  to  $\pm 15$  volts, bias current on the more negative input can rise to approximately  $500\mu\text{A}$ . This will also cause higher supply currents.
4.  $R_S \leq 200\Omega$   $V_{IN} \leq$  Common Mode Range. Input sensitivity is the worst case minimum differential input voltage required to guarantee a given output logic state. This parameter includes the effects of offset voltage, offset current, common mode rejection, and voltage gain.
5. For  $T_{pd}(1)$ ; 100mV input step, -10mV overdrive. For  $T_{pd}(0)$ ; -100mV input step, 10mV overdrive. Frequency  $\approx 100\text{Hz}$ ; Duty Cycle  $\approx 50\%$ ; Inverting input driven. See Test Circuit below. All unused inverting inputs tie to +5V.
6. For  $V_{OH}$  and  $V_{OL}$ :  $I_{Sink} = I_{Source} = 3.0\text{mA}$ . For other values of  $V_{Logic}$ :  $V_{OH}(\text{min.}) = V_{Logic} + -1.5\text{V}$ .
7. Total Power Dissipation (T.P.D.) is the sum of individual dissipation contributions of  $V+$ ,  $V-$  and  $V_{Logic}$  shown in curves of Power Dissipation vs. Supply Voltages (see Performance Curves). The calculated T.P.D. is then located on the graph of Maximum Allowable Package Dissipation vs. Ambient Temperature to determine ambient temperature operating limits imposed by the calculated T.P.D. (See Performance Curves). For instance, the combination of +15V, -15V, +5V, 0V ( $V+$ ,  $V-$ ,  $V_{Logic+}$ ,  $V_{Logic-}$ ) gives a T.P.D. of 350mW, the combination +15V, -15V, 0V gives a T.P.D. of 450mW.
8. Derate By  $5.8\text{mW}/^\circ\text{C}$  above  $T_A = +75^\circ\text{C}$ .  $\theta_{ja} = 75^\circ\text{C}/\text{W}$ ,  $\theta_{jc} = 20^\circ\text{C}/\text{W}$ .

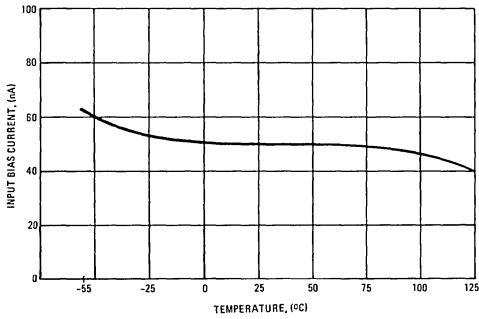
Test Circuits



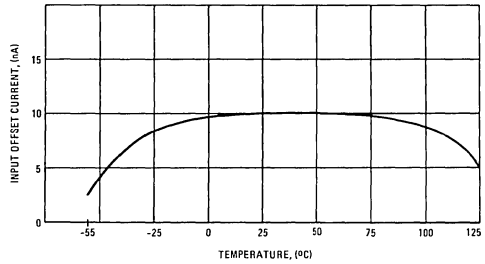
For input and output voltage waveforms for various input overdrives see Performance Curves.

**Typical Performance Curves**  $V_+ = 15V$ ,  $V_{Logic (+)} = 5V$ ,  $V_{Logic (-)} = 0V$ ,  $T_A = +25^\circ C$ ,  
Unless Otherwise Specified.

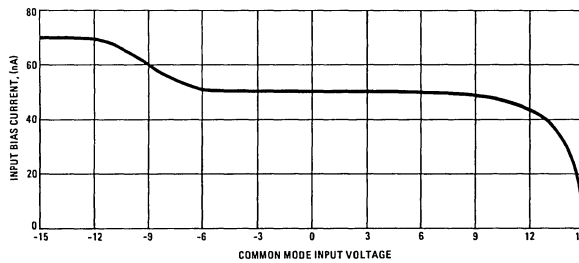
**INPUT BIAS CURRENT vs. TEMPERATURE**



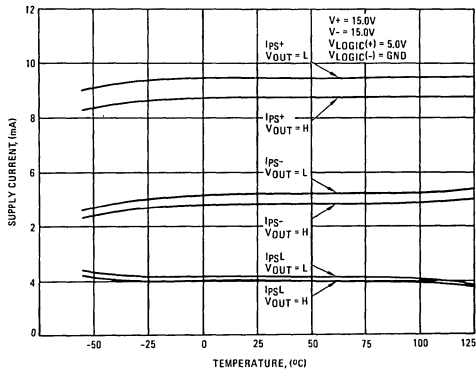
**INPUT OFFSET CURRENT vs. TEMPERATURE**



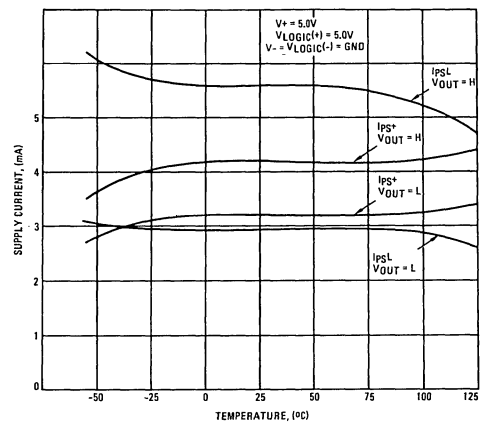
**INPUT BIAS CURRENT vs. COMMON MODE INPUT VOLTAGE**  
( $V_{DIFF.} = 0V$ )



**SUPPLY CURRENT vs. TEMPERATURE**  
FOR  $\pm 15V$  SUPPLIES AND  $\pm 5V$  LOGIC SUPPLY

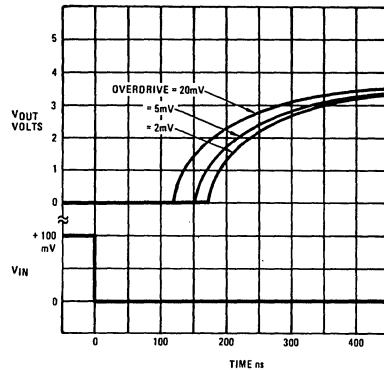
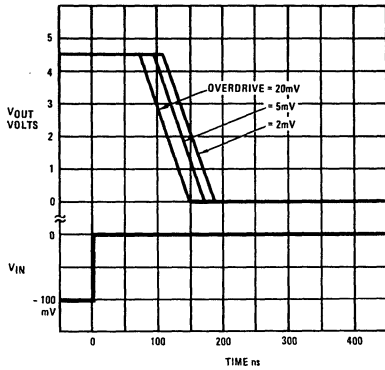


**SUPPLY CURRENT vs. TEMPERATURE**  
FOR SINGLE +5V OPERATION

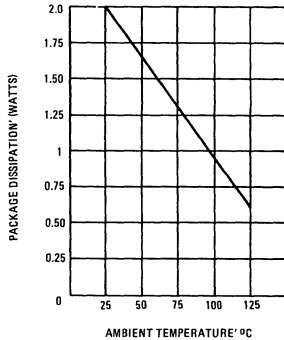


**Typical Performance Curves (Continued)**  $V_+ = 15V$ ,  $V_{Logic (+)} = 5V$ ,  $V_{Logic (-)} = 0V$ ,  $T_A = +25^\circ C$ , Unless Otherwise Specified.

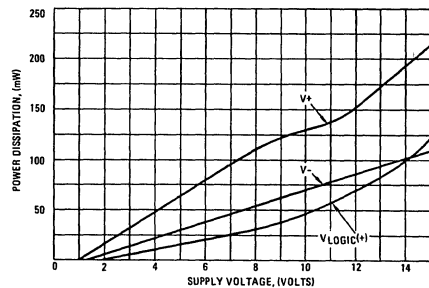
**RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES**



**MAXIMUM PACKAGE DISSIPATION vs.  $T_{AMBIENT}$**



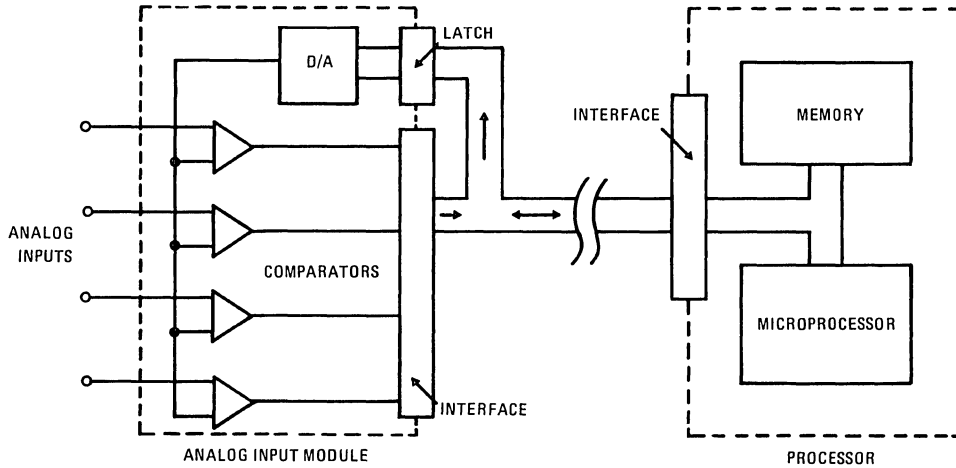
**MAXIMUM POWER DISSIPATION vs. SUPPLY VOLTAGE (NO LOAD CONDITION)**



**Applying the HA-4900 Series Comparators**

- SUPPLY CONNECTIONS:** This device is exceptionally versatile in working with most available power supplies. The voltage applied to the  $V_+$  and  $V_-$  terminals determines the allowable input signal range; while the voltage applied to the  $V_{L+}$  and  $V_{L-}$  determines the output swing. In systems where dual analog supplies are available, these would be connected to  $V_+$  and  $V_-$ , while the logic supply and return would be connected to  $V_{Logic+}$  and  $V_{Logic-}$ . The analog and logic supply commons can be connected together at one point in the system, since the comparator is immune to noise on the logic supply ground. A negative output swing may be obtained by connecting  $V_{L+}$  to ground and  $V_{L-}$  to a negative supply. Bipolar output swings (15V P-P, max.) may be obtained using dual supplies. In systems where only a single logic supply is available (+5V to 15V),  $V_+$  and  $V_{Logic+}$  may be connected together to the positive supply while  $V_-$  and  $V_{Logic-}$  are grounded. If an input signal could swing negative with respect to the  $V_-$  terminal, a resistor should be connected in series with the input to limit input current to  $< 5mA$  since the C-B junction of the input transistor would be forward biased.
- UNUSED INPUTS:** Inputs of unused comparator sections should be tied to a differential voltage source to prevent output "chatter".
- CROSSTALK:** Simultaneous high frequency operation of all other channels in the package will not affect the output logic state of a given channel, provided that its differential input voltage is sufficient to define a given logic state ( $\Delta V_{IN} \geq \pm V_{OS}$ ). Low level or high impedance input lines should be shielded from other signal sources to reduce crosstalk and interference.
- POWER SUPPLY DECOUPLING:** Decouple all power supply lines with .01 $\mu F$  ceramic capacitors to ground line located near the package to reduce coupling between channels or from external sources.
- RESPONSE TIME:** Fast rise time ( $< 200ns$ ) input pulses of several volts amplitude may result in delay times somewhat longer than those illustrated for 100mV steps. Operating speed is optimized by limiting the maximum differential input voltage applied, with resistor-diode clamping networks.

**Typical Applications**

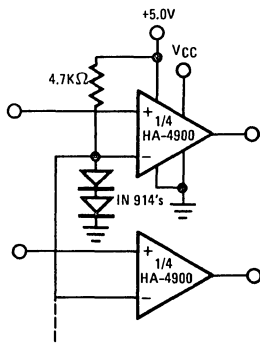


**Data Acquisition System**

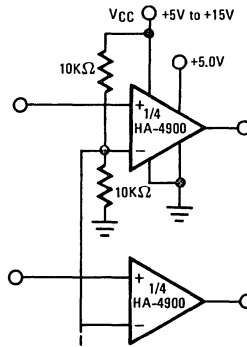
In this circuit the HA-4900 series is used in conjunction with a D to A converter to form a simple, versatile, multi-channel analog input for a data acquisition system. In operation the processor first sends an address to the D to A, then the processor reads the digital word generated by the comparator outputs.

To perform a simple comparison, the processor sets the D to A to a given reference level, then examines one or more

comparator outputs to determine if their inputs are above or below the reference. A window comparison consists of two such cycles with 2 reference levels set by the D to A. One way to digitize the inputs would be for the processor to increment the D to A in steps. The D to A address, as each comparator switches, is the digitized level of the input. While stairstepping the D to A is slower than successive approximation, all channels are digitized during one staircase ramp.



TTL TO CMOS



CMOS TO TTL

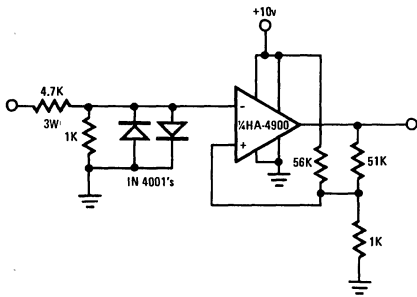
**Logic Level Translators**

The HA-4900 series comparators can be used as versatile logic interface devices as shown in the circuits above. Negative logic devices may also be interfaced with appropriate supply connections.

If separate supplies are used for  $V^-$  and  $V_{Logic-}$ , these logic level translators will tolerate several volts of ground line differential noise.

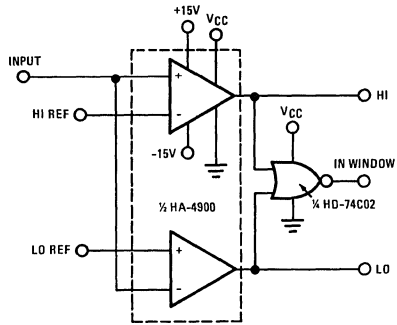


**Typical Applications (Continued)**



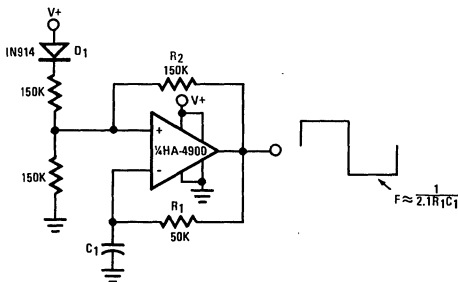
**RS-232 To CMOS Line Receiver**

This RS-232 type line receiver to drive CMOS logic uses a Schmitt trigger feedback network to give about 1 volt input hysteresis for added noise immunity. A possible problem in an interface which connects two equipments, each plugged into a different AC receptacle, is that the power line voltage may appear at the receiver input when the interface connection is made or broken. The two diodes and a 3 watt input resistor will protect the inputs under these conditions.



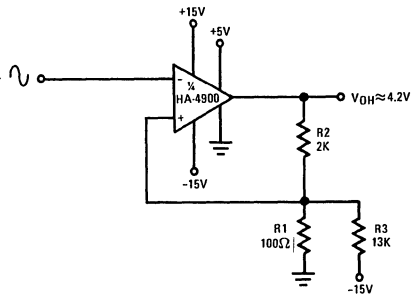
**Window Detector**

The high switching speed, low offset current and low offset voltage of the HA-4900 series makes this window detector circuit extremely well suited to applications requiring fast, accurate, decision-making. The circuit above is ideal for industrial process system feedback controllers or "out-of-limit" alarm indicators.



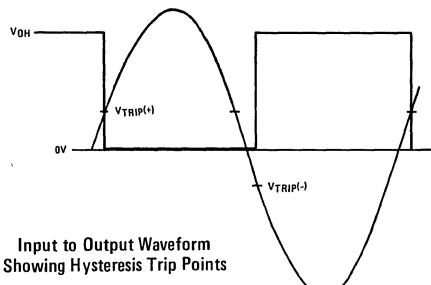
**Oscillator/Clock Generator**

This self-starting fixed frequency oscillator circuit gives excellent frequency stability. R<sub>1</sub> and C<sub>1</sub> comprise the frequency determining network while R<sub>2</sub> provides the regenerative feedback. Diode D<sub>1</sub> enhances the stability by compensating for the difference between V<sub>OH</sub> and V<sub>Supply</sub>. In applications where a precision clock generator up to 100kHz is required, such as in automatic test equipment, C<sub>1</sub> may be replaced by a crystal.



**Schmitt Trigger (Zero Crossing Detector With Hysteresis)**

This Circuit has a 100mV hysteresis which can be used in applications where very fast transition times are required at the output even though the signal input is very slow. The hysteresis loop also reduces false triggering due to noise on the input. The waveforms below show the trip points developed by the hysteresis loop.



Input to Output Waveform Showing Hysteresis Trip Points

PRELIMINARY

August 1991

Ultra-High Speed Comparator

### Features

- Low Propagation Delay (0003/0003L) ..... 2.0/2.1ns
- Low Latch Set-up Time ..... 0.8ns
- Low Offset Voltage, Drift Coefficient ..... 1.0mV, 4 $\mu$ V/ $^{\circ}$ C
- Wide Common Mode Range ..... +5.2/-2.8V
- Low Power Dissipation ..... 200mW
- Large Differential Input Resistance ..... 1M $\Omega$
- Complementary ECL Outputs; 50 $\Omega$  Driving Capability
- Resistor Programmable Hysteresis with '0003L
- Pin Compatible with MAX9690/9685 & AD96685
- Available in SOIC

### Applications

- Window Detector
- High Speed Peak Detector
- High Speed Threshold Detector
- High Speed Data Acquisition Systems
- Fiber Optic Decision Circuits
- High Speed Phase Detector
- Frequency Counter

### Description

The HFA-0003/0003L are monolithic, ultra high speed, voltage comparators. These comparators combine a low input offset voltage (1.0mV) with a low propagation delay (2.0ns) to achieve a large dynamic input range. The low offset voltage also makes these comparators ideally suited for high speed, precision analog-to-digital processing applications. The circuits have differential analog inputs, and provide complementary, ECL compatible (10K and 100K) logic outputs. The outputs are capable of supplying the current required by terminated 50 $\Omega$  transmission lines. Both outputs are open emitter structures, requiring external pull-down resistors. The recommended circuit is 50 $\Omega$  connected to -2.0V, but any equivalent ECL termination circuit may be used.

The HFA-0003L is a latched version of the HFA-0003. The latch function allows the HFA-0003L to operate in sample-hold or track-hold modes, when synchronous detection is required. The Latch Enable (LE) input can be driven by a standard ECL gate. See the Applications section on page 4 for more information on this feature.

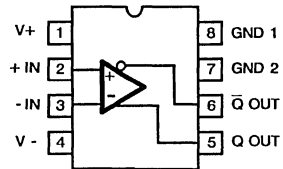
The HFA-0003L also has an additional feature, user programmable hysteresis. By connecting a resistor from the HYS pin to GND the user can select up to 20mV of input hysteresis. See the Applications section on page 4 for more information on this feature.

The HFA-0003 is pin compatible with the MAX9690, and SP9680 while providing improved performance. The HFA-0003L is pin compatible with the MAX9685, AD96685, SP9685, HCMP96850, and the VC7695 while providing improved performance.

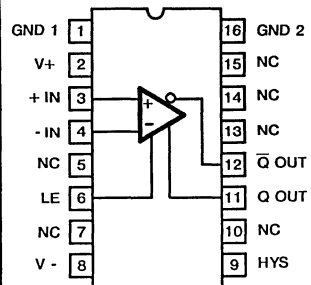
The performance of the HFA-0003/0003L-5 is guaranteed from -40 $^{\circ}$ C to +85 $^{\circ}$ C, while the HFA-0003/0003L-5 is guaranteed from 0 $^{\circ}$ C to +75 $^{\circ}$ C. The HFA-0003 is available in 8 pin Plastic DIP, Ceramic Sidebraze DIP, and SOIC. The HFA-0003L is available in 16 pin Plastic DIP, Ceramic Sidebraze DIP, SOIC, and a TO-100 Metal Can package. Refer to the /883 datasheets for military compliant product.

### Pinouts

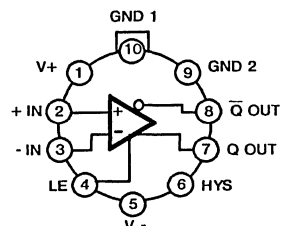
HFA7-0003-5/-9  
(CERAMIC SIDEBRAZE DIP)  
HFA3-0003-5/-9 (PLASTIC MINI-DIP)  
HFA9P0003-5/-9 (SOIC)  
TOP VIEW



HFA1-0003L-5/-9  
(CERAMIC SIDEBRAZE DIP)  
HFA3-0003L-5/-9 (PLASTIC DIP)  
HFA9P0003L-5/-9 (SOIC)  
TOP VIEW



HFA2-0003L-5/-9  
(TO-100 METAL CAN)  
TOP VIEW



4  
COMPARATORS

## Specifications HFA-0003/HFA-0003L

### Absolute Maximum Ratings (Note 1)

|   |        |
|---|--------|
| Voltage Between V+ and V- Terminals .....             | 20V    |
| Supply Voltage (GND to V+) .....                      | 8V     |
| Supply Voltage (GND to V-) .....                      | 18V    |
| Differential Input Voltage .....                      | 5.5V   |
| Common Mode Voltage .....                             | ±5V    |
| Differential Ground Voltage (GND1 to GND2) .....      | ±1V    |
| Peak (Short Duration) Output Current (Note 2) .....   | -35mA  |
| Maximum Junction Temperature .....                    | +175°C |
| Maximum Junction Temperature (Plastic Packages) ..... | +150°C |

### Operating Temperature Range

|                                     |                                 |
|-------------------------------------|---------------------------------|
| HFA-0003/HFA-0003L-9 .....          | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| HFA-0003/HFA-0003L-5 .....          | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| Storage Temperature Range .....     | -65°C ≤ T <sub>A</sub> ≤ +150°C |
| Thermal Package Characteristics     |                                 |
|                                     | θ <sub>jc</sub> θ <sub>ja</sub> |
| 8 Pin Ceramic Sidebraced DIP .....  | 39      95                      |
| 8 Pin Plastic DIP .....             | 34      96                      |
| 8 Pin SOIC .....                    | 42      161                     |
| 16 Pin Ceramic Sidebraced DIP ..... | 34      79                      |
| 16 Pin Plastic DIP .....            | 32      92                      |
| 16 Pin SOIC .....                   | 35      114                     |
| TO-100 Metal Can .....              | 32      108                     |

### Electrical Specifications V+ = 5V, V- = -5.2V, R<sub>L</sub> = 50Ω to -2V, Unless Otherwise Specified

| PARAMETER   | TEMP  | HFA-0003-5/-9 |       |       | HFA-0003L-5/-9 |       |       | UNITS |
|---|-------|---------------|-------|-------|----------------|-------|-------|-------|
|   |       | MIN           | TYP   | MAX   | MIN            | TYP   | MAX   |       |
| <b>INPUT CHARACTERISTICS</b>  |       |               |       |       |                |       |       |       |
| Input Offset Voltage (V <sub>OS</sub> )                                 | +25°C | -             | 1     | 3     | -              | 1     | 3     | mV    |
|   | Full  | -             | -     | 4     | -              | -     | 4     | mV    |
| Average Offset Voltage Drift (Note 8)                                   | Full  | -             | -     | 4     | -              | -     | 4     | μV/°C |
| Input Bias Current  | +25°C | -             | 5     | 8     | -              | 5     | 8     | μA    |
|   | Full  | -             | 8     | 13    | -              | 8     | 13    | μA    |
| Input Offset Current  | +25°C | -             | 0.15  | 0.2   | -              | 0.15  | 0.2   | μA    |
|   | Full  | -             | -     | 0.3   | -              | -     | 0.3   | μA    |
| Common Mode Range   | Full  | -2.8          | -     | +5.2  | -2.8           | -     | +5.2  | V     |
| Differential Input Resistance   | +25°C | -             | 1     | -     | -              | 1     | -     | MΩ    |
| Common Mode Input Resistance  | +25°C | -             | 9.5   | -     | -              | 9.5   | -     | MΩ    |
| Input Capacitance   | +25°C | -             | 1     | -     | -              | 1     | -     | pF    |
| <b>TRANSFER CHARACTERISTICS</b>   |       |               |       |       |                |       |       |       |
| Large Signal Voltage Gain   | +25°C | -             | 3100  | -     | -              | 3100  | -     | V/V   |
|   | Full  | -             | 1200  | -     | -              | 1200  | -     | V/V   |
| Common Mode Rejection Ratio (Note 3)                                    | +25°C | 70            | 75    | -     | 70             | 75    | -     | dB    |
|   | Full  | 70            | -     | -     | 70             | -     | -     | dB    |
| Tracking Bandwidth (Note 4)   | +25°C | -             | 270   | -     | -              | 270   | -     | MHz   |
| <b>SWITCHING CHARACTERISTICS</b>  |       |               |       |       |                |       |       |       |
| Propagation Delay Input to Output (t <sub>pd</sub> )<br>(Notes 5, 8, 9) | +25°C | -             | 2.0   | 2.4   | -              | 2.1   | 2.6   | ns    |
|   | Full  | -             | -     | 2.8   | -              | -     | 3.0   | ns    |
| Maximum Dispersion (Notes 6, 8)   | Full  | -             | -     | 200   | -              | -     | 200   | ps    |
| <b>OUTPUT CHARACTERISTICS</b>   |       |               |       |       |                |       |       |       |
| Output Voltage Level<br>Logic Low (V <sub>OL</sub> )                    | +25°C | -             | -1.83 | -1.65 | -              | -1.83 | -1.65 | V     |
|   | Full  | -             | -1.83 | -1.57 | -              | -1.83 | -1.57 | V     |
| Logic High (V <sub>OH</sub> )   | +25°C | -0.938        | -0.85 | -     | -0.938         | -0.85 | -     | V     |
|   | Full  | -1.05         | -0.96 | -     | -1.05          | -0.96 | -     | V     |
| Continuous Output Current (Note 2)                                      | Full  | -30           | -     | -     | -30            | -     | -     | mA    |

## Specifications HFA-0003/HFA-0003L

**Electrical Specifications (Continued)**  $V_+ = 5V$ ,  $V_- = -5.2V$ ,  $R_L = 50\Omega$  to  $-2V$ , Unless Otherwise Specified

| PARAMETER   | TEMP  | HFA-0003-5/-9 |     |     | HFA-0003L-5/-9 |      |        | UNITS   |
|---|-------|---------------|-----|-----|----------------|------|--------|---------|
|   |       | MIN           | TYP | MAX | MIN            | TYP  | MAX    |         |
| <b>LATCH CHARACTERISTICS (HFA-0003L ONLY)</b>     |       |               |     |     |                |      |        |         |
| LE Input Voltage Level                            |       |               |     |     |                |      |        |         |
| Logic Low ( $V_{IL}$ )                            | Full  | -             | -   | -   | -              | -    | -1.475 | V       |
| Logic High ( $V_{IH}$ )                           | Full  | -             | -   | -   | -1.105         | -    | -      | V       |
| LE Input Current Level                            |       |               |     |     |                |      |        |         |
| Logic Low ( $V_{IL} = -1.85V$ )                   | Full  | -             | -   | -   | -              | 0.06 | 0.5    | $\mu A$ |
| Logic High ( $V_{IH} = -0.81V$ )                  | Full  | -             | -   | -   | -              | 11   | 20     | $\mu A$ |
| Propagation Delay from LE to Output ( $t_{pdL}$ ) | +25°C | -             | -   | -   | -              | 2.2  | 2.7    | ns      |
| (Notes 5, 8, 9)                                   | Full  | -             | -   | -   | -              | 2.6  | 3.1    | ns      |
| Minimum Set-Up Time ( $t_s$ ) (Notes 8, 9)        | +25°C | -             | -   | -   | -              | 0.8  | 1.2    | ns      |
|   | Full  | -             | -   | -   | -              | -    | 1.5    | ns      |
| Minimum Hold Time ( $t_h$ ) (Notes 8, 9)          | Full  | -             | -   | -   | -              | 0.5  | 1.0    | ns      |
| Minimum LE Pulse Width ( $t_{pw}$ ) (Notes 8, 9)  | +25°C | -             | -   | -   | -              | 0.9  | 0.95   | ns      |
|   | Full  | -             | -   | -   | -              | -    | 1.1    | ns      |
| <b>POWER SUPPLY</b>                               |       |               |     |     |                |      |        |         |
| PSRR (Note 7)                                     | +25°C | 70            | 80  | -   | 70             | 80   | -      | dB      |
|   | Full  | 65            | -   | -   | 65             | -    | -      | dB      |
| $I_{CC}$  | Full  | -             | 11  | 13  | -              | 11   | 13     | mA      |
| $I_{EE}$  | Full  | -             | 19  | 22  | -              | 19   | 22     | mA      |
| Power Dissipation                                 | Full  | -             | -   | 200 | -              | -    | 200    | mW      |

**NOTES:**

1. Absolute maximum ratings are limiting values, applied individually, beyond which the servicability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions may affect device reliability.
2. Outputs have no sink current (+I) capability, since they are open emitter NPN transistors.
3.  $-2.0V \leq V_{CM} \leq +4.0V$ .
4. Tracking Bandwidth (TBW) is defined as the maximum input frequency at which the outputs still switch between  $V_{OL}$  and  $V_{OH}$ .  $V_{IN} = 15mV_{p-p}$  sinewave centered on OV.
5.  $V_{IN} = 100mV$ .  $V_{OD}$  is the amount of input overdrive.
6. Dispersion is defined as the change in propagation delay for input overdrives between 0.1V and 1.0V.
7.  $+4.0V \leq V_+ \leq +5.5V$  or  $-6.2V \leq V_- \leq -4.7V$ .
8. This parameter is not tested. It is guaranteed by design, and by device characterization.
9.  $V_{OD} = 10mV$ .

**Applications Information**

**HFA-0003L Latch Functionality**

The Latch Enable (LE) pin of the '0003L controls the function of the on chip latch. When the LE input is at an ECL Logic 1, the latch is open (transparent) and the comparator functions normally. When the LE input switches to a Logic 0, the outputs are latched in unambiguous states dependant on the current input state, providing the set-up and hold times are met. If the latch function is not utilized, the LE input must be connected to an ECL Logic 1 (e.g. GND).

**HFA-0003L Hysteresis Functionality**

To improve performance in systems with slow transition times, and/or high noise levels, the HFA-0003L allows the user to easily set the amount of input hysteresis. The hysteresis level is set by the current flowing into the HYS input; the larger the current the larger the level of hysteresis. This current is provided by connecting a resistor (R<sub>H</sub>) between the HYS pin and GND, and it is recommended that the input

current not exceed 1mA. The input current can be approximated from the following formula:

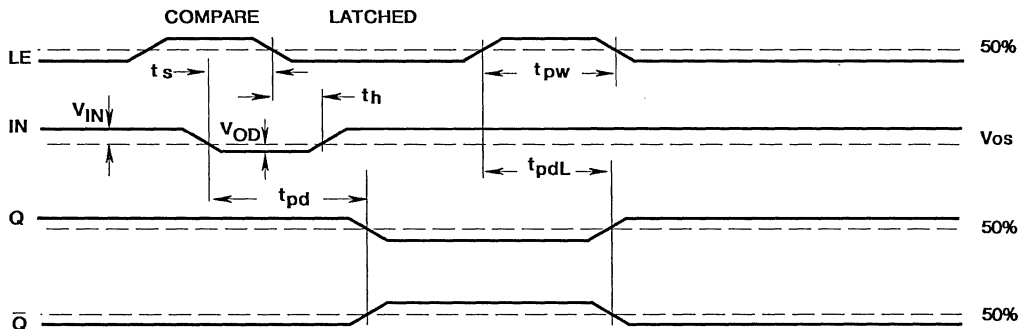
$$I_H = \frac{GND-(V-)-0.7V}{R_H}$$

The table below gives approximate levels of hysteresis for some values of I<sub>H</sub>, at T<sub>A</sub> = +25°C.

|                     |     |     |     |     |     |
|---------------------|-----|-----|-----|-----|-----|
| I <sub>H</sub> (mA) | 0.2 | 0.4 | 0.6 | 0.8 | 1.0 |
| HYS (mV)            | 1   | 4   | 8   | 13  | 22  |

If the hysteresis function isn't used, the HYS input may be left floating, or may be connected to V-. The HYS input **MUST NEVER BE CONNECTED** directly to GND or V+, as device damage will occur. **Before inserting an HFA-0003L into a competitor socket**, the user must ensure that the corresponding socket pin is a true no-connect (i.e. is floating).

**Timing Diagram**



## SAMPLE AND HOLD AMPLIFIERS

|   | PAGE |
|---|------|
| SELECTION GUIDE .....   | 5-2  |
| <b>SAMPLE AND HOLD DATA SHEETS</b>                                    |      |
| HA 2420, 25    Fast Sample and Hold Amplifier .....                   | 5-3  |
| HA 5320        High Speed Precision Monolithic Amplifier .....        | 5-10 |
| HA 5330        Very High Speed Monolithic Amplifier .....             | 5-17 |
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# Selection Guide

## SAMPLE-AND-HOLD AMPLIFIERS

| TYPE   | SAMPLE/HOLD TYPE  | TEMPERATURE RANGE   | PACKAGE*  | ACQUISITION TIME (TO 0.01%) TYP, +25°C                  | CHARGE TRANSFER TYP, +25°C | APERTURE TIME TYP, +25°C | GAIN BANDWIDTH PRODUCT TYP, +25°C                    |
|--|---|---|---|---|----------------------------|--------------------------|--|
| HA1-2420-2<br>HA1-2420-8<br>HA1-2425-5<br>HA1-2425-7<br>HA3-2425-5<br>HA4-2420/883<br>HA4P2425-5 | Low Droop Rate  | -55°C to +125°C<br>-55°C to +125°C<br>0°C to +75°C<br>0°C to +75°C<br>0°C to +75°C<br>-55°C to +125°C<br>0°C to +75°C | 14-Pin Cerdip<br>14-Pin Cerdip<br>14-Pin Cerdip<br>14-Pin Cerdip<br>14-Pin Epoxy<br>20-Pin LCC Ceramic<br>20-Pin PLCC Epoxy | 3.2µs<br><br><br><br><br><br>(C <sub>H</sub> = 1,000pF) | 10pC                       | 30ns                     | 2.5MHz   |
| HA1-5320-2<br>HA1-5320-5<br>HA1-5320-7<br>HA1-5320-8<br>HA3-5320-5<br>HA4-5320-8                 | High Speed<br>Low Charge<br>Transfer Precision<br>Complete-Includes<br>Hold Capacitor | -55°C to +125°C<br>0°C to +75°C<br>0°C to +75°C<br>-55°C to +125°C<br>0°C to +75°C<br>-55°C to +125°C                 | 14-Pin Cerdip<br>14-Pin Cerdip<br>14-Pin Cerdip<br>14-Pin Cerdip<br>14-Pin Plastic DIP<br>20-Pin LCC Ceramic                | 1µs<br><br><br><br><br><br>(C <sub>H</sub> = Internal)  | 0.1pC                      | 25ns                     | 2.0MHz<br><br><br><br><br><br>C <sub>H</sub> = 100pF |
| HA1-5330-5<br>HA1-5330-4<br>HA1-5330-2<br>HA1-5330/883<br>HA4-5330/883                           | Very High Speed<br>Precision<br>Monolithic<br>Complete-Includes<br>Hold Capacitor     | 0°C to +75°C<br>-25°C to +85°C<br>-55°C to +125°C<br>-55°C to +125°C<br>-55°C to +125°C                               | 14-Pin Cerdip<br>14-Pin Cerdip<br>14-Pin Cerdip<br>14-Pin Cerdip<br>20-Pin LCC Ceramic                                      | 500ns   | 0.05pC                     | 20ns                     | 4.5MHz   |
| HA1-5340-5<br>HA1-5340-9   | High Speed<br>Low Distortion-<br>Includes Hold<br>Capacitor                           | 0°C to +75°C<br>-40°C to +85°C  | 14-Pin Cerdip<br>14-Pin Cerdip  | 700ns   | 0.5pC                      | 15ns                     | 10MHz  |

\* See Packaging and Ordering Information in Section 12

August 1991

## Fast Sample and Hold

### Features

- Maximum Acquisition Time (10V Step to 0.1%) ... 4 $\mu$ s (10V Step to 0.01%) ..... 6 $\mu$ s
- Low Droop Rate ( $C_H = 1000\text{pF}$ ) ..... 5 $\mu\text{V/ms}$  (Typ.)
- Gain Bandwidth Product ..... 2.5MHz (Typ.)
- Low Effective Aperture Delay Time ..... 30ns (Typ.)
- TTL Compatible Control Input
- $\pm 12\text{V}$  to  $\pm 15\text{V}$  Operation

### Description

The HA-2420/2425 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and MOSFET input unity gain amplifier.

With an external holding capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over

### Applications

- 12-Bit Data Acquisition
- Digital to Analog Deglitcher
- Auto Zero Systems
- Peak Detector
- Gated Operational Amplifier

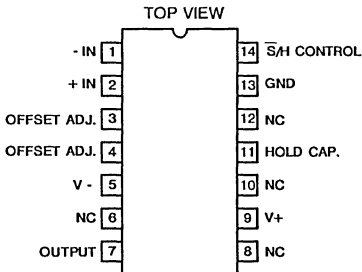
the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc. For more information, please see Application Note 517.

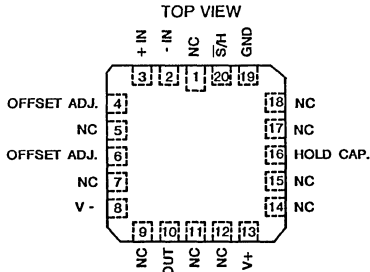
The HA-2420/25 is offered in a 14 pin Ceramic or Plastic DIP and a 20 pad Ceramic LCC or 20 pad PLCC. The MIL-STD-883 data sheet for this device is available on request.

**SAMPLE AND HOLD AMPLIFIERS**

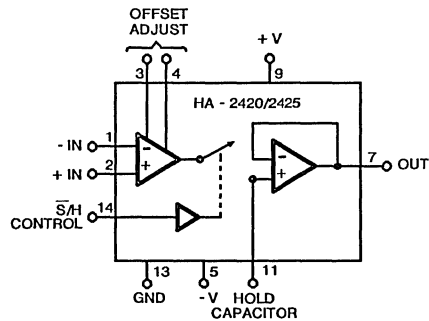
### Pinouts 14 PIN CERAMIC/PLASTIC DIP



### 20 PAD LCC/PLCC



### Functional Diagram





## Specifications HA-2420/2425

### Absolute Maximum Ratings

|   |                         |
|---|-------------------------|
| Voltage Between V+ and V- Terminals .....         | 40V                     |
| Differential Input Voltage .....                  | ±24V                    |
| Digital Input Voltage (Sample and Hold Pin) ..... | +8V, -15V               |
| Output Current .....                              | Short Circuit Protected |
| Junction Temperature .....                        | +175°C                  |

### Operating Temperature Range

|                                 |                                 |
|---------------------------------|---------------------------------|
| HA-2420-2/-8 .....              | -55°C ≤ T <sub>A</sub> ≤ +125°C |
| HA-2425-5/-7 .....              | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| Storage Temperature Range ..... | -65°C ≤ T <sub>A</sub> ≤ +150°C |

**Electrical Specifications** Test Conditions (Unless Otherwise Specified) V<sub>SUPPLY</sub> = ±15.0V; C<sub>H</sub> = 1000pF;  
 Digital Input: V<sub>IL</sub> = +0.8V (Sample), V<sub>IH</sub> = +2.0V (Hold),  
 Unity Gain Configuration (Output tied to -Input)

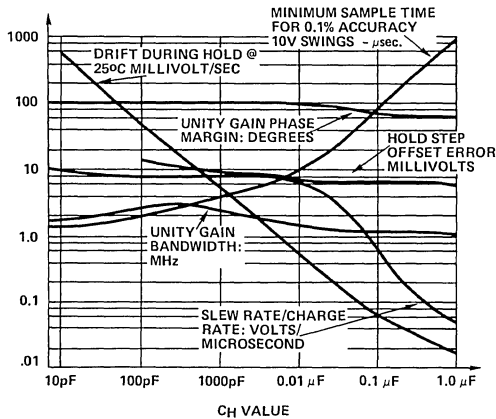
| PARAMETER                                       | TEMP  | HA-2420-2/-8 |      |      | HA-2425-5/-7 |      |      | UNITS |
|---|-------|--------------|------|------|--------------|------|------|-------|
|   |       | MIN          | TYP  | MAX  | MIN          | TYP  | MAX  |       |
| <b>INPUT CHARACTERISTICS</b>                    |       |              |      |      |              |      |      |       |
| Input Voltage Range                             | Full  | ±10          | -    | -    | ±10          | -    | -    | V     |
| Offset Voltage                                  | +25°C | -            | 2    | 4    | -            | 3    | 6    | mV    |
|   | Full  | -            | 3    | 6    | -            | 4    | 8    | mV    |
| Bias Current                                    | +25°C | -            | 40   | 200  | -            | 40   | 200  | nA    |
|   | Full  | -            | -    | 400  | -            | -    | 400  | nA    |
| Offset Current                                  | +25°C | -            | 10   | 50   | -            | 10   | 50   | nA    |
|   | Full  | -            | -    | 100  | -            | -    | 100  | nA    |
| Input Resistance                                | +25°C | 5            | 10   | -    | 5            | 10   | -    | MΩ    |
| Common Mode Range                               | Full  | ±10          | -    | -    | ±10          | -    | -    | V     |
| <b>TRANSFER CHARACTERISTICS</b>                 |       |              |      |      |              |      |      |       |
| Large Signal Voltage Gain (Notes 1, 4)          | Full  | 25K          | 50K  | -    | 25K          | 50K  | -    | V/V   |
| Common Mode Rejection (Note 2)                  | Full  | -80          | -90  | -    | -74          | -90  | -    | dB    |
| Hold Mode Feedthrough Attenuation (Note 3)      | Full  | -            | -76  | -    | -            | -76  | -    | dB    |
| Gain Bandwidth Product (Note 3)                 | +25°C | -            | 2.5  | -    | -            | 2.5  | -    | MHz   |
| <b>OUTPUT CHARACTERISTICS</b>                   |       |              |      |      |              |      |      |       |
| Output Voltage Swing (Note 1)                   | Full  | ±10          | -    | -    | ±10          | -    | -    | V     |
| Output Current                                  | +25°C | ±15          | -    | -    | ±15          | -    | -    | mA    |
| Full Power Bandwidth (Notes 3, 4)               | +25°C | -            | 100  | -    | -            | 100  | -    | kHz   |
| Output Resistance (D.C.)                        | +25°C | -            | 0.15 | -    | -            | 0.15 | -    | Ω     |
| <b>TRANSIENT RESPONSE</b>                       |       |              |      |      |              |      |      |       |
| Rise Time (Notes 3, 5)                          | +25°C | -            | 75   | 100  | -            | 75   | 100  | ns    |
| Overshoot (Notes 3, 5)                          | +25°C | -            | 25   | 40   | -            | 25   | 40   | %     |
| Slew Rate (Notes 3, 6)                          | +25°C | 3.5          | 5    | -    | 3.5          | 5    | -    | V/μs  |
| <b>DIGITAL INPUT CHARACTERISTICS</b>            |       |              |      |      |              |      |      |       |
| Digital Input Current (V <sub>IN</sub> = 0V)    | Full  | -            | -    | -0.8 | -            | -    | -0.8 | mA    |
| Digital Input Current (V <sub>IN</sub> = +5.0V) | Full  | -            | -    | 20   | -            | -    | 20   | μA    |
| Digital Input Voltage (Low)                     | Full  | -            | -    | 0.8  | -            | -    | 0.8  | V     |
| Digital Input Voltage (High)                    | Full  | 2.0          | -    | -    | 2.0          | -    | -    | V     |
| <b>SAMPLE AND HOLD CHARACTERISTICS</b>          |       |              |      |      |              |      |      |       |
| Acquisition Time to 0.1% 10V Step (Note 3)      | +25°C | -            | 2.3  | 4    | -            | 2.3  | 4    | μs    |
| Acquisition Time to 0.01% 10V Step (Note 3)     | +25°C | -            | 3.2  | 6    | -            | 3.2  | 6    | μs    |
| Aperture Time (Note 9)                          | +25°C | -            | 30   | -    | -            | 30   | -    | ns    |
| Effective Aperture Delay Time                   | +25°C | -            | 30   | -    | -            | 30   | -    | ns    |
| Aperture Uncertainty                            | +25°C | -            | 5    | -    | -            | 5    | -    | ns    |
| Drift Current (Notes 3, 7)                      | +25°C | -            | 5    | -    | -            | 5    | -    | pA    |
| HA1-2420, HA4-2420                              | Full  | -            | 1.8  | 10   | -            | -    | -    | nA    |
| HA1-2425  | Full  | -            | -    | -    | -            | 0.1  | 1.0  | nA    |
| HA3-2425, HA4P2425                              | Full  | -            | -    | -    | -            | 7.5  | 10.0 | nA    |
| Hold Step Error (Note 7)                        | +25°C | -            | 10   | 20   | -            | 10   | 20   | mV    |
| <b>POWER SUPPLY CHARACTERISTICS</b>             |       |              |      |      |              |      |      |       |
| Supply Current (+)                              | +25°C | -            | 3.5  | 5.5  | -            | 3.5  | 5.5  | mA    |
| Supply Current (-)                              | +25°C | -            | 2.5  | 3.5  | -            | 2.5  | 3.5  | mA    |
| Power Supply Rejection                          | Full  | -80          | -90  | -    | -74          | -90  | -    | dB    |

- NOTES: 1. R<sub>L</sub> = 2kΩ. 2. V<sub>CM</sub> = ±10VDC. 3. A<sub>v</sub> = ±1, R<sub>L</sub> = 2kΩ, C<sub>L</sub> = 50pF. 4. V<sub>OUT</sub> = 20V peak-to-peak. 5. V<sub>OUT</sub> = 200mV peak-to-peak. 6. V<sub>OUT</sub> = 10.0V peak-to-peak. 7. V<sub>IN</sub> = 0V. 8. f<sub>IN</sub> ≤ 100kHz. 9. Derived from computer simulation only; not tested.

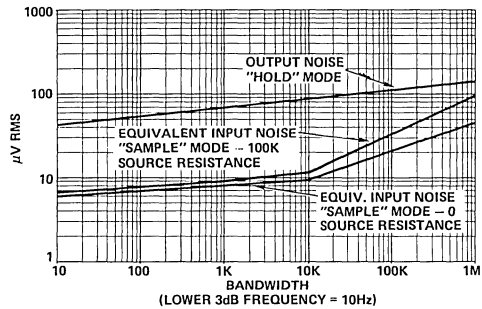
# HA-2420/2425

**Performance Curves**  $V_{SUPPLY} = \pm 15VDC$ ,  $T_A = +25^\circ C$ ,  $C_H = 1000pF$  Unless Otherwise Specified

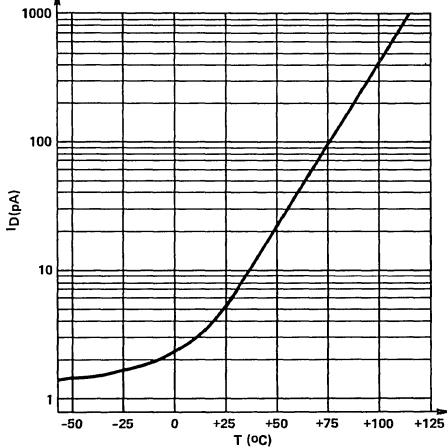
## TYPICAL SAMPLE AND HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITOR



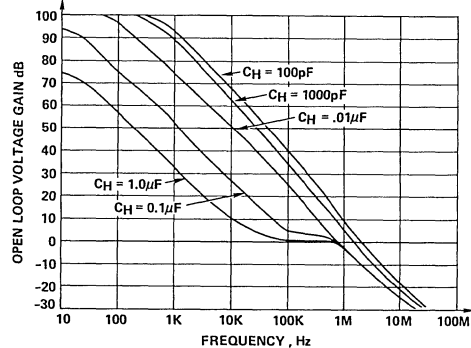
## BROADBAND NOISE CHARACTERISTICS



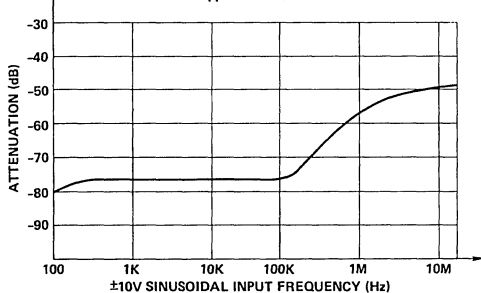
## DRIFT CURRENT vs. TEMPERATURE



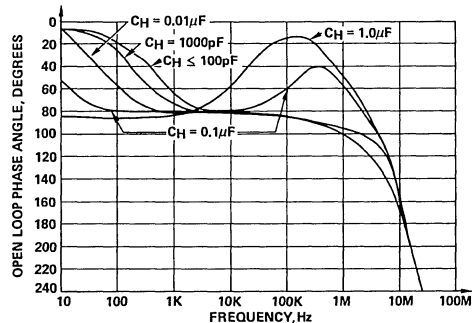
## OPEN LOOP FREQUENCY RESPONSE



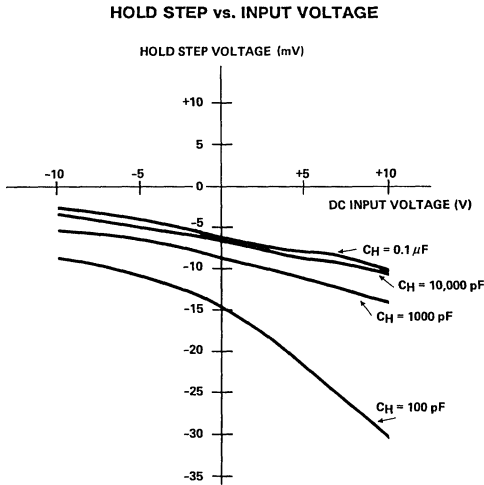
## HOLD MODE FEED THROUGH ATTENUATION $C_H = 1000pF$



## OPEN LOOP PHASE RESPONSE



**Offset and Gain Adjustment**



**GAIN ADJUSTMENT**

The linear variation in pedestal voltage with sample-and-hold input voltage causes a  $-0.06\%$  gain error ( $C_H = 1000\text{pF}$ ). In some applications (D/A deglitcher, A/D converter) the gain error can be adjusted elsewhere in the system, while in other applications it must be adjusted at the sample-and-hold. The two circuits shown below demonstrate how to adjust gain error at the sample-and-hold.

The recommended procedure for adjusting gain error is:

1. Perform offset adjustment.
2. Apply the nominal input voltage that should produce a +10V output.
3. Adjust the trim pot for +10V output in the hold mode.
4. Apply the nominal input voltage that should produce a -10V output.
5. Measure the output hold voltage ( $V_{-10 \text{ NOMINAL}}$ ). Adjust the trim pot for an output hold voltage of

$$\frac{(V_{-10 \text{ NOMINAL}}) + (-10V)}{2}$$

**OFFSET ADJUSTMENT**

The offset voltage of the HA-2420/2425 may be adjusted using a  $100\text{k}\Omega$  trim pot, as shown in Figure 6. The recommended adjustment procedure is:

1. Apply zero volts to the sample-and-hold input, and a square wave to the  $\overline{\text{S/H}}$  control.
2. Adjust the trim pot for zero volts output in the hold mode.

**INVERTING CONFIGURATION**

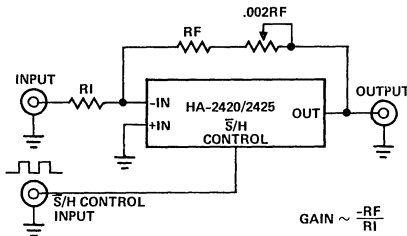


FIGURE 2.

**NONINVERTING CONFIGURATION**

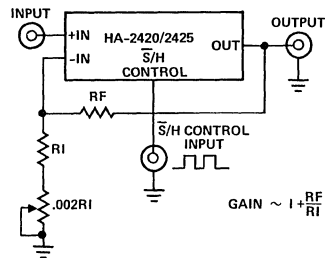


FIGURE 3.

# HA-2420/2425

## Test Circuits

### HOLD STEP ERROR AND DRIFT CURRENT

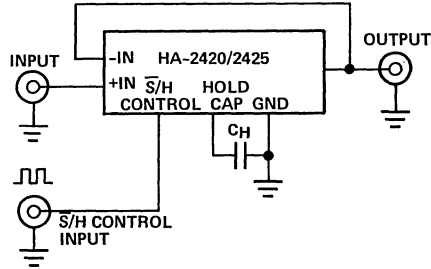
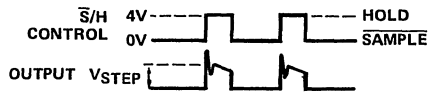


FIGURE 4.

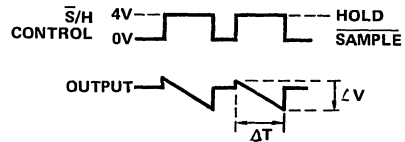
#### HOLD STEP ERROR TEST

1. With a D.C. input voltage, observe the following waveforms:



#### DRIFT CURRENT TEST

1. With a D.C. input voltage, observe the following waveforms:



2. Set rise/fall times of  $\bar{S}/H$  Control to approximately 20ns.

2. Measure the slope of the output during hold,  $\Delta V/\Delta t$ , and compute drift current from:  $I_D = C_H \Delta V/\Delta t$ .

### HOLD MODE FEEDTHROUGH ATTENUATION

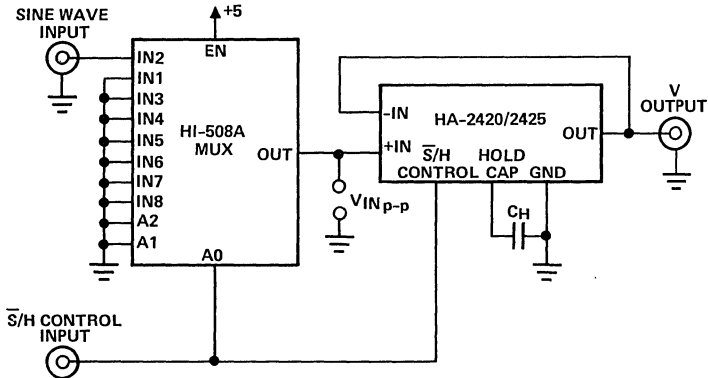


FIGURE 5.

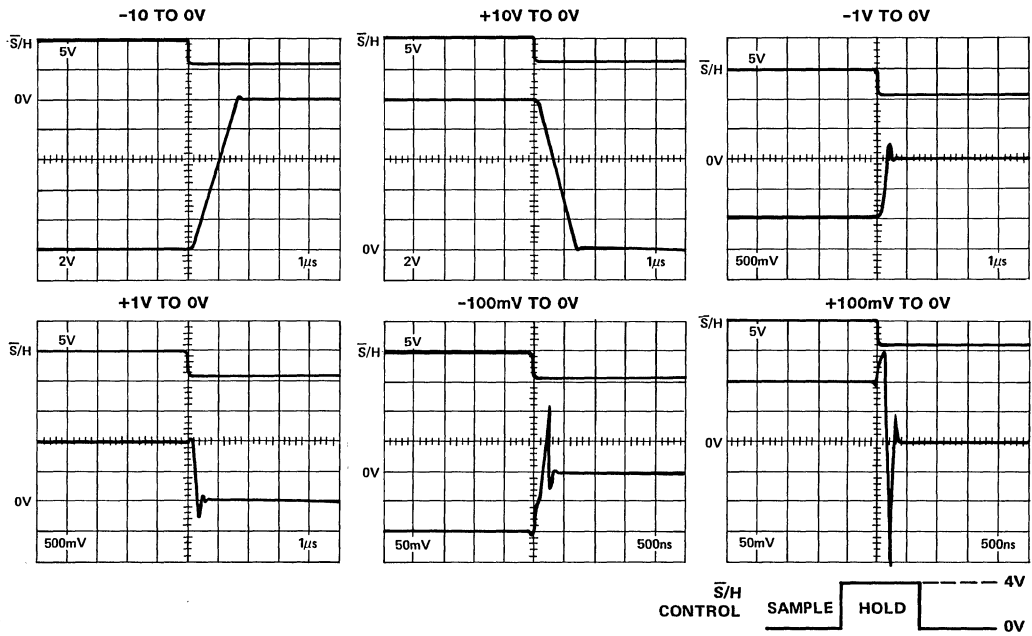
NOTE: Compute hold mode feedthrough attenuation from the formula:

$$\text{Feedthrough Attenuation} = 20 \text{ Log } \frac{V_{\text{OUT HOLD}}}{V_{\text{IN HOLD}}}$$

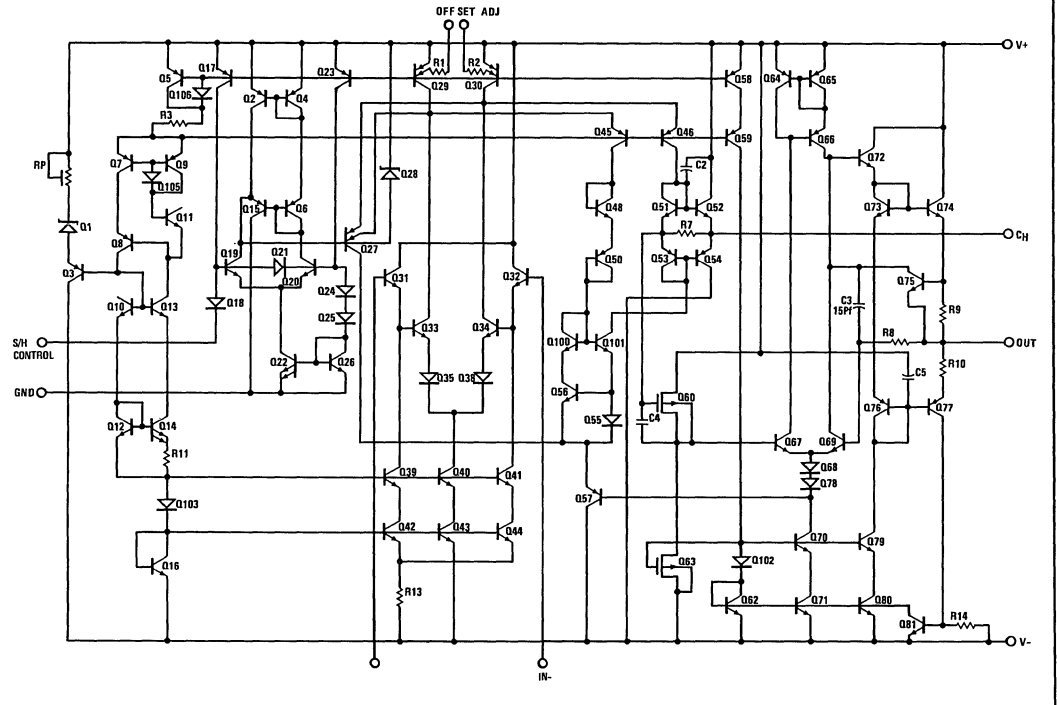
Where  $V_{\text{OUT HOLD}}$  = Peak-to-Peak value of output sinewave during the hold mode.

# HA-2420/2425

## Acquisition Times ( $C_H = 1000\text{pF}$ )



## Schematic



**Applications**

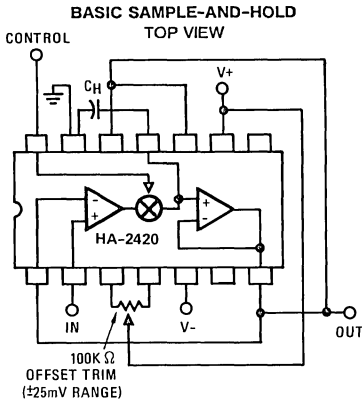


FIGURE 6.

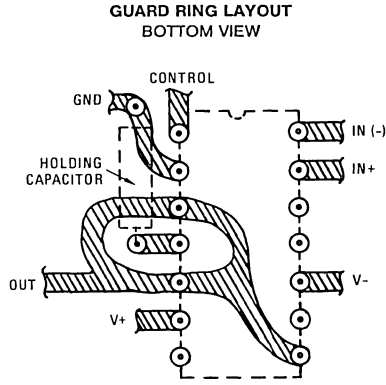


FIGURE 7.

**NOTES:**

- Figure 6 shows a typical unity gain circuit, with Offset Zeroing. All of the other normal op amp feedback configurations may be used with the HA-2420/2425. The input amplifier may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.
- The method used to reduce leakage paths on the P.C. board and the device package is shown in Figure 7. This guard ring is recommended to minimize the drift during hold mode.

- The holding capacitor should have extremely high insulation resistance and low dielectric absorption. Polystyrene (below +85°C), Teflon, or Parlene types are recommended.

For more applications, consult Harris Application Note 517, or factory applications group.

**Glossary of Terms:**

**ACQUISITION TIME:**

The time required following a "sample" command, for the output to reach its final value within  $\pm 0.1\%$  or  $\pm 0.01\%$ . This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

**APERTURE TIME:**

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

**EFFECTIVE APERTURE DELAY TIME (EADT):**

The difference between the digital delay time from the Hold command to the opening of the S/H switch, and the propagation time from the analog input to the switch.

EADT may be positive, negative or zero. If zero, the S/H amplifier will output a voltage equal to  $V_{IN}$  at the instant the Hold command was received. For negative EADT, the

output in Hold (exclusive of pedestal and droop errors) will correspond to a value of  $V_{IN}$  that occurred before the Hold command.

**APERTURE UNCERTAINTY:**

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

**DRIFT CURRENT:**

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D \text{ (pA)} = C_H \text{ (pF)} \times \frac{\Delta V}{\Delta T} \text{ (Volts/sec)}$$

**Die Characteristics**

|                     |                      |
|---------------------|----------------------|
| Transistor Count    | 78                   |
| Die Dimensions      | 97 x 61 x 19 mils    |
| Substrate Potential | -V <sub>SUPPLY</sub> |
| Process             | Bipolar DI           |

|                          |               |               |
|--------------------------|---------------|---------------|
| Thermal Constants (°C/W) | $\theta_{ja}$ | $\theta_{jc}$ |
| Ceramic DIP              | 94            | 39            |
| Ceramic LCC              | 88            | 28            |

## High Speed Precision Monolithic Sample and Hold Amplifier

August 1991

### Features

- Gain, D.C. ....  $2 \times 10^6$  V/V
- Acquisition Time .....  $1.0 \mu\text{s}$  (0.01%)
- Droop Rate .....  $0.08 \mu\text{V}/\mu\text{s}$  (+25°C)  
 $17 \mu\text{V}/\mu\text{s}$  (Full Temperature)
- Aperture Time ..... 25ns
- Hold Step Error (See Glossary) ..... 1.0mV
- Internal Hold Capacitor
- Fully Differential Input
- TTL Compatible

### Description

The HA-5320 was designed for use in precision, high speed data acquisition systems.

The circuit consists of an input transconductance amplifier capable of providing large amounts of charging current, a low leakage analog switch, and an output integrating amplifier. The analog switch sees virtual ground as its load; therefore, charge injection on the hold capacitor is constant over the entire input/output voltage range. The pedestal voltage resulting from this charge injection can be adjusted to zero by use of the offset adjust inputs. The device includes a hold capacitor. However, if improved droop rate is

### Applications

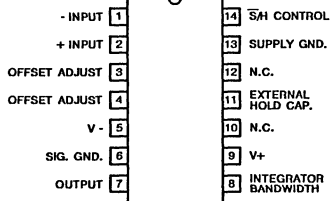
- Precision Data Acquisition Systems
- Digital to Analog Converter Deglitcher
- Auto Zero Circuits
- Peak Detector

required at the expense of acquisition time, additional hold capacitance may be added externally.

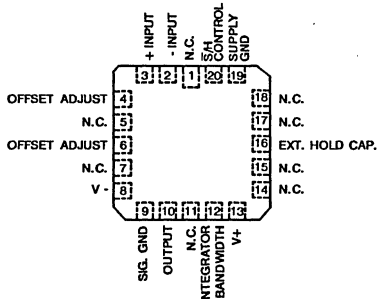
This monolithic device is manufactured using the Harris Dielectric Isolation Process, minimizing stray capacitance and eliminating SCR's. This allows higher speed and latch-free operation. The HA-5320 is available in a Ceramic 14-pin DIP, a Plastic 14-pin DIP, and a Ceramic 20-pin LCC package. For further information, please see Application Note 538. The Mil-Std-883 data sheet for this device is available on request.

### Pinouts

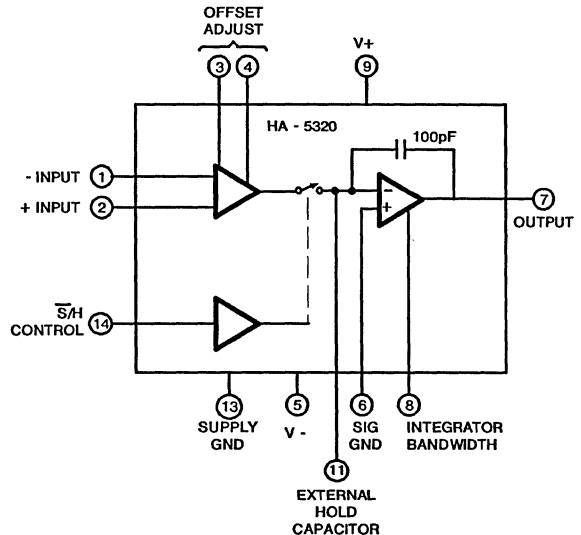
14 PIN PLASTIC DIP  
14 PIN CERAMIC DIP  
TOP VIEW



20 PIN CERAMIC LCC  
TOP VIEW



### Functional Diagram



## Specifications HA-5320

### Absolute Maximum Ratings (Note 1)

|   |                |
|---|----------------|
| Voltage Between V+ and V- Terminals ..... | 40V            |
| Differential Input Voltage .....          | ±24V           |
| Digital Input Voltage .....               | +8V, -15V      |
| Output Current, Continuous .....          | ±20mA (Note 2) |
| Junction Temperature .....                | +175°C         |

### Operating Temperature Range

|                                 |                                 |
|---------------------------------|---------------------------------|
| HA-5320-2/-8 .....              | -55°C ≤ T <sub>A</sub> ≤ +125°C |
| HA-5320-5/-7 .....              | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| Storage Temperature Range ..... | -65°C ≤ T <sub>A</sub> ≤ +150°C |

### Electrical Specifications

Test Conditions (Unless Otherwise Specified) V<sub>SUPPLY</sub> = ±15.0V; C<sub>H</sub> = Internal;  
 Digital Input: V<sub>IL</sub> = +0.8V (Sample), V<sub>IH</sub> = +2.0V (Hold), Unity Gain Configuration  
 (Output tied to -Input)

| PARAMETER  | TEMP  | HA-5320-2/-8    |                   |     | HA-5320-5/-7      |                   |     | UNITS             |
|--|-------|-----------------|-------------------|-----|-------------------|-------------------|-----|-------------------|
|  |       | MIN             | TYP               | MAX | MIN               | TYP               | MAX |                   |
| <b>INPUT CHARACTERISTICS</b>                             |       |                 |                   |     |                   |                   |     |                   |
| Input Voltage Range                                      | Full  | ±10             | -                 | -   | ±10               | -                 | -   | V                 |
| Input Resistance   | +25°C | 1               | 5                 | -   | 1                 | 5                 | -   | MΩ                |
| Input Capacitance  | +25°C | -               | -                 | 3   | -                 | -                 | 3   | pF                |
| Offset Voltage   | +25°C | -               | 0.2               | -   | -                 | 0.5               | -   | mV                |
|  | Full  | -               | -                 | 2.0 | -                 | -                 | 1.5 | mV                |
| Bias Current   | +25°C | -               | 70                | 200 | -                 | 100               | 300 | nA                |
|  | Full  | -               | -                 | 200 | -                 | -                 | 300 | nA                |
| Offset Current   | +25°C | -               | 30                | 100 | -                 | 30                | 300 | nA                |
|  | Full  | -               | -                 | 100 | -                 | -                 | 300 | nA                |
| Common Mode Range  | Full  | ±10             | -                 | -   | ±10               | -                 | -   | V                 |
| CMRR (Note 3)  | +25°C | 80              | 90                | -   | 72                | 90                | -   | dB                |
| Offset Voltage T.C.                                      | Full  | -               | 5                 | 15  | -                 | 5                 | 20  | μV/°C             |
| <b>TRANSFER CHARACTERISTICS</b>                          |       |                 |                   |     |                   |                   |     |                   |
| Gain, D.C. (Note 12)                                     | +25°C | 10 <sup>6</sup> | 2x10 <sup>6</sup> | -   | 3x10 <sup>5</sup> | 2x10 <sup>6</sup> | -   | V/V               |
| Gain Bandwidth Product (A <sub>v</sub> = +1)<br>(Note 5) | +25°C | -               | 2.0               | -   | -                 | 2.0               | -   | MHz               |
|  |       | -               | 0.18              | -   | -                 | 0.18              | -   | MHz               |
| <b>OUTPUT CHARACTERISTICS</b>                            |       |                 |                   |     |                   |                   |     |                   |
| Output Voltage   | Full  | ±10             | -                 | -   | ±10               | -                 | -   | V                 |
| Output Current   | +25°C | ±10             | -                 | -   | ±10               | -                 | -   | mA                |
| Full Power Bandwidth (Note 4)                            | +25°C | -               | 600               | -   | -                 | 600               | -   | kHz               |
| Output Resistance (Hold Mode)                            | +25°C | -               | 1.0               | -   | -                 | 1.0               | -   | Ω                 |
| Total Output Noise, D.C. to 10MHz                        |       |                 |                   |     |                   |                   |     |                   |
| Sample   | +25°C | -               | 125               | 200 | -                 | 125               | 200 | μV <sub>RMS</sub> |
| Hold   | +25°C | -               | 125               | 200 | -                 | 125               | 200 | μV <sub>RMS</sub> |
| <b>TRANSIENT RESPONSE</b>                                |       |                 |                   |     |                   |                   |     |                   |
| Rise Time (Note 5)                                       | +25°C | -               | 100               | -   | -                 | 100               | -   | ns                |
| Overshoot (Note 5)                                       | +25°C | -               | 15                | -   | -                 | 15                | -   | %                 |
| Slew Rate (Note 6)                                       | +25°C | -               | 45                | -   | -                 | 45                | -   | V/μs              |
| <b>DIGITAL INPUT CHARACTERISTICS</b>                     |       |                 |                   |     |                   |                   |     |                   |
| Input Voltage (High), V <sub>IH</sub>                    | Full  | 2.0             | -                 | -   | 2.0               | -                 | -   | V                 |
| Input Voltage (Low), V <sub>IL</sub>                     | Full  | -               | -                 | 0.8 | -                 | -                 | 0.8 | V                 |
| Input Current (V <sub>IL</sub> = 0V)                     | Full  | -               | -                 | 4   | -                 | -                 | 4   | μA                |
| Input Current (V <sub>IH</sub> = +5V)                    | Full  | -               | -                 | 0.1 | -                 | -                 | 0.1 | μA                |

  
**SAMPLE AND HOLD  
 AMPLIFIERS**



## Specifications HA-5320

### Electrical Specifications (Continued)

| PARAMETER   | TEMP  | HA-5320-2/-8 |      |     | HA-5320-5/-7 |      |     | UNITS |
|---|-------|--------------|------|-----|--------------|------|-----|-------|
|   |       | MIN          | TYP  | MAX | MIN          | TYP  | MAX |       |
| <b>SAMPLE AND HOLD CHARACTERISTICS</b>              |       |              |      |     |              |      |     |       |
| Acquisition Time to 0.1% (Note 7)                   | +25°C | -            | 0.8  | 1.2 | -            | 0.8  | 1.2 | μs    |
| Acquisition Time to 0.01% (Note 7)                  | +25°C | -            | 1.0  | 1.5 | -            | 1.0  | 1.5 | μs    |
| Aperture Time (Note 8)                              | +25°C | -            | 25   | -   | -            | 25   | -   | ns    |
| Effective Aperture Delay Time (See Glossary)        | +25°C | -50          | -25  | 0   | -50          | -25  | 0   | ns    |
| Aperture Uncertainty                                | +25°C | -            | 0.3  | -   | -            | 0.3  | -   | ns    |
| Droop Rate  | +25°C | -            | 0.08 | 0.5 | -            | 0.08 | 0.5 | μV/μs |
| Drift Current (Note 9)                              | Full  | -            | 17   | 100 | -            | 1.2  | 100 | μV/μs |
|   | +25°C | -            | 8    | 50  | -            | 8    | 50  | pA    |
| Charge Transfer (Note 9)                            | Full  | -            | 1.7  | 10  | -            | 0.12 | 10  | nA    |
|   | +25°C | -            | 0.1  | 0.5 | -            | 0.1  | 0.5 | pC    |
| Hold Mode Settling Time 0.01%                       | Full  | -            | 165  | 350 | -            | 165  | 350 | ns    |
| Hold Mode Feedthrough (10V <sub>p-p</sub> , 100kHz) | Full  | -            | 2    | -   | -            | 2    | -   | mV    |
| <b>POWER SUPPLY CHARACTERISTICS</b>                 |       |              |      |     |              |      |     |       |
| Positive Supply Current (Note 10)                   | +25°C | -            | 11   | 13  | -            | 11   | 13  | mA    |
| Negative Supply Current (Note 10)                   | +25°C | -            | -11  | -13 | -            | -11  | -13 | mA    |
| Power Supply Rejection                              | V+    | Full         | 80   | -   | 80           | -    | -   | dB    |
|   | V-    | Full         | 65   | -   | 65           | -    | -   | dB    |

**NOTES**

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Internal Power Dissipation may limit Output Current below 20mA.
3.  $V_{CM} = \pm 5V$  D.C.
4.  $V_O = 20V_{p-p}$ ;  $R_L = 2k\Omega$ ;  $C_L = 50pF$ ; unattenuated output.
5.  $V_O = 200mV_{p-p}$ ;  $R_L = 2k\Omega$ ;  $C_L = 50pF$ .
6.  $V_O = 20V$  Step;  $R_L = 2k\Omega$ ;  $C_L = 50pF$ .
7.  $V_O = 10V$  Step;  $R_L = 2k\Omega$ ;  $C_L = 50pF$ .
8. Derived from computer simulation only; not tested.
9.  $V_{IN} = 0V$ ,  $V_{IH} = +3.5V$ ,  $t_r < 20ns$  ( $V_{IL}$  to  $V_{IH}$ ).
10. Specified for a zero differential input voltage between +IN and -IN. Supply current will increase with differential input (as may occur in the Hold mode) to approximately  $\pm 46mA$  at 20V.
11. Based on a one volt delta in each supply, i.e.  $15V \pm 0.5V$  D.C.
12.  $R_L = 1K$ ,  $C_L = 30pF$

## HA-5320

### Applying the HA-5320

The HA-5320 has the uncommitted differential inputs of an op amp, allowing the Sample and Hold function to be combined with many conventional op amp circuits. See the Harris Application Note 517 for a collection of circuit ideas.

#### LAYOUT

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01 to 0.1 $\mu$ F, ceramic) should be provided from each power supply terminal to the Supply Ground terminal on pin 13.

The ideal ground connections are pin 6 (SIG. Ground) directly to the system Signal Ground, and pin 13 (Supply Ground) directly to the system Supply Common.

#### HOLD CAPACITOR

The HA-5320 includes a 100pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Specifications section is based on this internal capacitor).

Additional capacitance may be added between pins 7 and 11. This external hold capacitance will reduce droop rate at the expense of acquisition time, and provide other trade-offs as shown in the Performance Curves.

If an external hold capacitor  $C_{HEXT}$  is used, then a noise bandwidth capacitor of value  $0.1 C_{HEXT}$  should be connected from pin 8 to ground. Exact value and type are not critical.

The hold capacitor  $C_{HEXT}$  should have high insulation resistance and low dielectric absorption, to minimize droop errors. Polystyrene dielectric is a good choice for operating temperatures up to +85°C. Teflon® and glass dielectrics offer good performance to +125°C and above.

The hold capacitor terminal (pin 11) remains at virtual ground potential. Any PC connection to this terminal should be kept short and "guarded" by the ground plane, since nearby signal lines or power supply voltages will introduce errors due to drift current.

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### Applications

Figure 1 shows the HA-5320 connected as a unity gain noninverting amplifier — its most widely used configuration. As an input device for a fast successive — approximation A/D converter, it offers very high throughput rate for a monolithic IC sample/hold amplifier. Also, the HA-5320's hold step error is adjustable to zero using the Offset Adjust potentiometer, to deliver a 12-bit accurate output from the converter.

The application may call for an external hold capacitor  $C_{HEXT}$  as shown. As mentioned earlier,  $0.1 C_{HEXT}$  is then

recommended at pin 8 to reduce output noise in the Hold mode.

The HA-5320 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the S/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

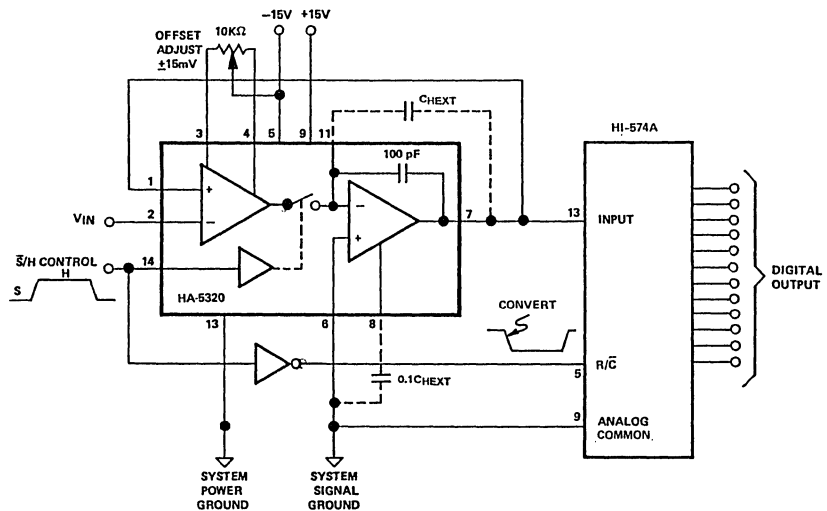
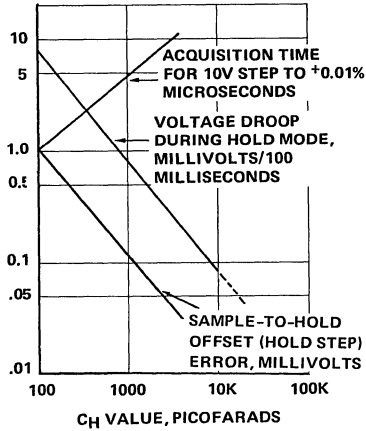


FIGURE 1.  
TYPICAL HA-5320 CONNECTIONS; NONINVERTING UNITY GAIN MODE

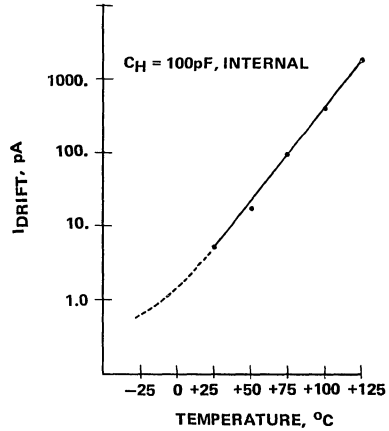
NOTE: Pin Numbers Refer to DIP Package Only.

**Performance Curves**  $V_{SUPPLY} = \pm 15VDC$

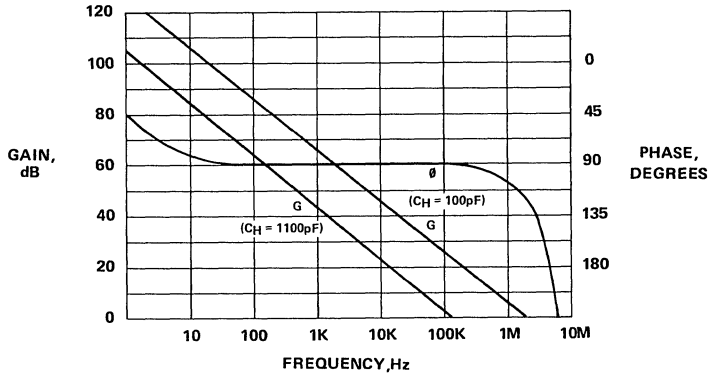
**TYPICAL SAMPLE AND HOLD PERFORMANCE AS FUNCTION OF HOLDING CAPACITOR**



**DRIFT CURRENT vs. TEMPERATURE**

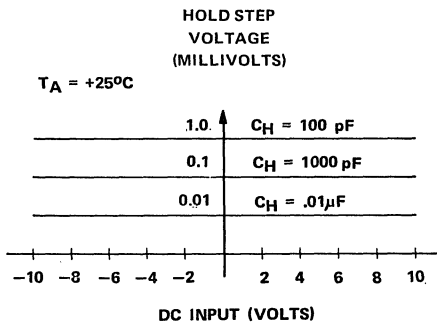


**OPEN LOOP GAIN AND PHASE RESPONSE**

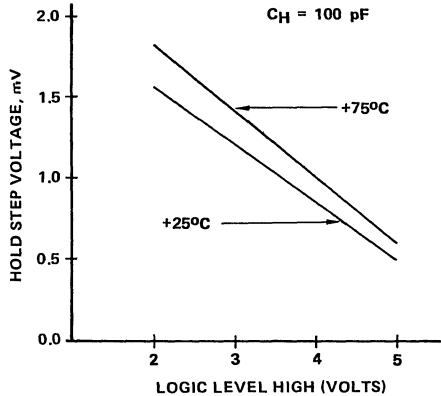


**TYPICAL SAMPLE-TO-HOLD OFFSET (HOLD STEP) ERROR**

**HOLD STEP vs. INPUT VOLTAGE**

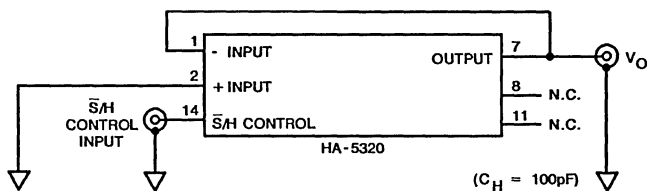


**HOLD STEP vs. LOGIC ( $V_{IH}$ ) VOLTAGE**



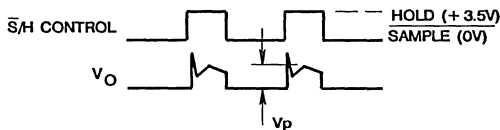
Test Circuits

CHARGE TRANSFER AND DRIFT CURRENT



CHARGE TRANSFER TEST

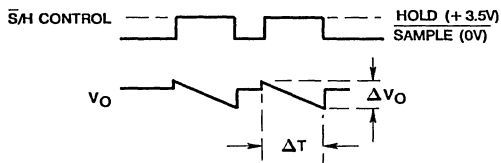
1. Observe the "hold step" voltage  $V_p$ :



2. Compute charge transfer:  $Q = V_p C_H$

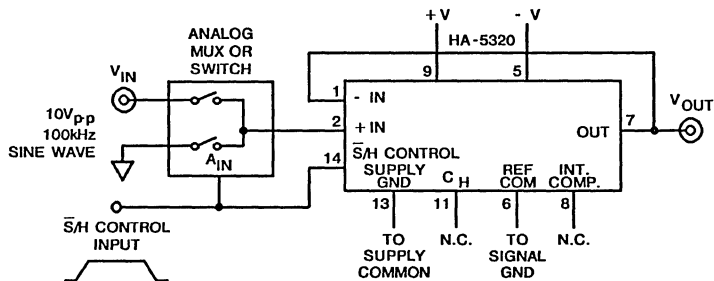
DRIFT CURRENT TEST

1. Observe the voltage "droop",  $\Delta V_O / \Delta T$ :



2. Measure the slope of the output during hold,  $\Delta V_O / \Delta T$ , and compute drift current:  $I_D = C_H \Delta V_O / \Delta T$ .

HOLD MODE FEED THROUGH ATTENUATION



Feedthrough in dB =  $20 \text{ Log } \frac{V_{OUT}}{V_{IN}}$  where:

$V_{OUT}$  = Volts<sub>p-p</sub>, Hold Mode,

$V_{IN}$  = Volts<sub>p-p</sub>.

**Glossary of Terms**

**ACQUISITION TIME:**

The time required following a "sample" command, for the output to reach its final value within  $\pm 0.1\%$  or  $\pm 0.01\%$ . This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

**CHARGE TRANSFER:**

The small charge transferred to the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the HOLD mode. Charge transfer is directly proportional to sample-to-hold offset pedestal error, where:

$$\text{Charge Transfer (pC)} = C_H (\text{pF}) \times \text{Offset Error (V)}$$

**APERTURE TIME:**

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is the interval between the conditions of 10% open and 90% open.

**HOLD STEP ERROR:**

Hold Step Error is the output error due to Charge Transfer (see above). It may be calculated from the specified parameter, Charge Transfer, using the following relationship:

$$\text{HOLD STEP (V)} = \frac{\text{CHARGE TRANSFER (pC)}}{\text{HOLD CAPACITANCE (pF)}}$$

See Performance Curves.

**EFFECTIVE APERTURE DELAY TIME (EADT):**

The difference between the digital delay time from the Hold command to the opening of the S/H switch, and the propagation time from the analog input to the switch.

EADT may be positive, negative or zero. If zero, the  $\bar{S}/H$  amplifier will output a voltage equal to  $V_{IN}$  at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of  $V_{IN}$  that occurred before the Hold command.

**APERTURE UNCERTAINTY:**

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

**DRIFT CURRENT:**

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D (\text{pA}) = C_H (\text{pF}) \times \frac{\Delta V}{\Delta T} (\text{Volts/sec})$$

**Die Characteristics**

|                           |                        |
|---------------------------|------------------------|
| Transistor Count .....    | 175                    |
| Die Dimensions .....      | 90.2 x 143.7 x 19 mils |
| Substrate Potential ..... | -V <sub>SUPPLY</sub>   |
| Process .....             | Bipolar DI             |

|                         |               |               |
|-------------------------|---------------|---------------|
| Thermal Constants (C/W) | $\theta_{ja}$ | $\theta_{jc}$ |
| Ceramic DIP             | 75            | 15            |
| Ceramic LCC             | 76            | 19            |

August 1991

### Features

- Very Fast Acquisition ..... 350ns (0.1%)  
500ns (0.01%)
- Low Droop Rate ..... 0.01 $\mu$ V/ $\mu$ s
- Very Low Offset ..... 0.2mV
- High Slew Rate ..... 90V/ $\mu$ s
- Wide Supply Range .....  $\pm$ 11V to  $\pm$ 18V
- Internal Hold Capacitor
- Fully Differential Input
- TTL/CMOS Compatible

### Description

The HA-5330 is a very fast sample and hold amplifier designed primarily for use with high speed A/D converters. It utilizes the Harris Dielectric Isolation process to achieve a 500ns acquisition time to 12-bit accuracy and a droop rate of 0.01 $\mu$ V/ $\mu$ s. The circuit consists of an input transconductance amplifier capable of producing large amounts of charging current, a low leakage analog switch, and an integrating output stage which includes a 90pF hold capacitor.

The analog switch operates into a virtual ground, so charge injection on the hold capacitor is constant and independent of

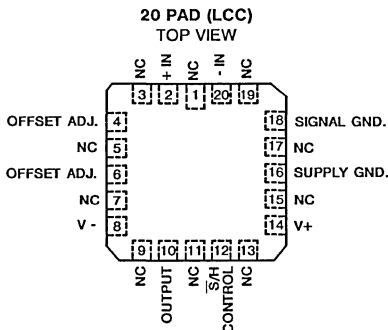
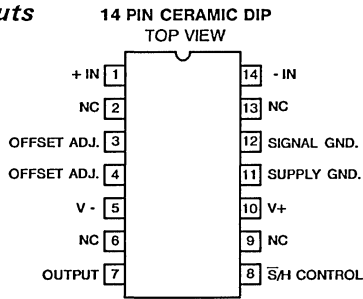
### Applications

- Precision Data Acquisition Systems
- D/A Converter Deglitching
- Auto-Zero Circuits
- Peak Detectors

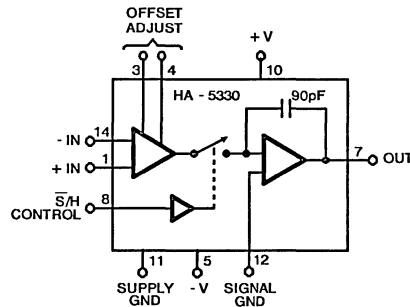
$V_{IN}$ . Charge injection is held to a low value by compensation circuits and, if necessary, the resulting 0.5mV hold step error can be adjusted to zero via the Offset Adjust terminals. Compensation is also used to minimize leakage currents which cause voltage droop in the Hold mode.

The HA-5330 will operate at reduced supply voltages (to  $\pm$ 11V) with a reduced signal range. This monolithic device is available in a 14 pin Ceramic DIP and a 20 pad LCC package. The MIL-STD-883 data sheet for this device is available on request.

### Pinouts



### Functional Diagram



## Specifications HA-5330

### Absolute Maximum Ratings (Note 1)

|  |                |
|--|----------------|
| Voltage between V+ and SUPPLY/SIG GND .....        | +20V           |
| Voltage between V- and SUPPLY/SIG GND .....        | -20V           |
| Voltage between SUPPLY GND and SIG GND .....       | ±2.0V          |
| Differential Input Voltage .....                   | ±24V           |
| Voltage between S/H Control and SUPPLY/SIG GND ... | +8V, -6V       |
| Output Current, Continuous .....                   | ±17mA (Note 2) |
| Junction Temperature .....                         | +175°C         |

### Operating Temperature Range

|                                 |                 |
|---------------------------------|-----------------|
| HA-5330-2 .....                 | -55°C to +125°C |
| HA-5330-4 .....                 | -25°C to +85°C  |
| HA-5330-5 .....                 | 0°C to +75°C    |
| Storage Temperature Range ..... | -65°C to +150°C |

### Electrical Specifications

Test Conditions Unless Otherwise Specified:  $V_{SUPPLY} = \pm 15V$ ;  
 S/H Control  $V_{IH} = +0.8V$  (Sample);  $V_{IH} = +2.0V$  (Hold); SIG GND = SUPPLY GND,  
 Unity Gain Configuration (Output tied to -Input)

| PARAMETER                              | TEMP        | HA-5330-2, -4   |                 |           | HA-5330-5       |                 |           | UNITS  |   |
|--|-------------|-----------------|-----------------|-----------|-----------------|-----------------|-----------|--------|---|
|  |             | MIN             | TYP             | MAX       | MIN             | TYP             | MAX       |        |   |
| <b>INPUT CHARACTERISTICS</b>           |             |                 |                 |           |                 |                 |           |        |   |
| Input Voltage Range                    | Full        | ±10             | -               | -         | ±10             | -               | -         | V      |   |
| Input Resistance (Note 3)              | +25°C       | 5               | 15              | -         | 5               | 15              | -         | MΩ     |   |
| Input Capacitance                      | +25°C       | -               | 3               | -         | -               | 3               | -         | pF     |   |
| Offset Voltage                         | +25°C       | -               | 0.2             | -         | -               | 0.2             | -         | mV     |   |
|  | Full        | -               | -               | 2.0       | -               | -               | 1.5       | mV     |   |
| Offset Voltage Temperature Coefficient | Full        | -               | 1               | 10        | -               | 1               | 10        | μV/°C  |   |
| Bias Current                           | +25°C       | -               | ±20             | -         | -               | ±20             | -         | nA     |   |
|  | Full        | -               | -               | ±500      | -               | -               | ±300      | nA     |   |
| Offset Current                         | +25°C       | -               | 20              | -         | -               | 20              | -         | nA     |   |
|  | Full        | -               | -               | 500       | -               | -               | 300       | nA     |   |
| Common Mode Range                      | Full        | ±10             | -               | -         | ±10             | -               | -         | V      |   |
| CMRR (Note 4)                          | Full        | 86              | 100             | -         | 86              | 100             | -         | dB     |   |
| <b>TRANSFER CHARACTERISTICS</b>        |             |                 |                 |           |                 |                 |           |        |   |
| Gain, DC                               | Full        | $2 \times 10^6$ | $2 \times 10^7$ | -         | $2 \times 10^6$ | $2 \times 10^7$ | -         | V/V    |   |
| Gain Bandwidth Product (Note 12)       | +25°C       | -               | 4.5             | -         | -               | 4.5             | -         | MHz    |   |
| <b>OUTPUT CHARACTERISTICS</b>          |             |                 |                 |           |                 |                 |           |        |   |
| Output Voltage                         | Full        | ±10             | -               | -         | ±10             | -               | -         | V      |   |
| Output Current                         | Full        | ±10             | -               | -         | ±10             | -               | -         | mA     |   |
| Full Power Bandwidth (Note 6)          | +25°C       | -               | 1.4             | -         | -               | 1.4             | -         | MHz    |   |
| Output Resistance                      | Hold Mode   | +25°C           | -               | 0.2       | -               | 0.2             | -         | Ω      |   |
|  | Sample Mode | +25°C           | -               | $10^{-5}$ | 0.001           | -               | $10^{-5}$ | 0.001  | Ω |
| Total Output Noise, DC to 4.0MHz       | Sample Mode | +25°C           | -               | 230       | -               | 230             | -         | μV RMS |   |
|  | Hold Mode   | +25°C           | -               | 190       | -               | 190             | -         | μV RMS |   |

### Die Characteristics

|                           |                    |               |
|---------------------------|--------------------|---------------|
| Transistor Count .....    | 205                |               |
| Die Dimensions .....      | 99 x 166 x 19 mils |               |
| Substrate Potential ..... | SIG. GND           |               |
| Process .....             | Bipolar-DI         |               |
| Thermal Constants (°C/W)  | $\theta_{ja}$      | $\theta_{jc}$ |
| Ceramic DIP               | 75                 | 15            |
| Ceramic LCC               | 76                 | 19            |

## Specifications HA-5330

### Electrical Specifications (Continued)

| PARAMETER                                      | TEMP    | HA-5330-2, -4 |      |     | HA-5330-5 |      |     | UNITS |    |
|--|---------|---------------|------|-----|-----------|------|-----|-------|----|
|  |         | MIN           | TYP  | MAX | MIN       | TYP  | MAX |       |    |
| <b>TRANSIENT RESPONSE</b>                      |         |               |      |     |           |      |     |       |    |
| Rise Time (Note 5)                             | +25°C   | -             | 70   | -   | -         | 70   | -   | ns    |    |
| Overshoot (Note 5)                             | +25°C   | -             | 10   | -   | -         | 10   | -   | %     |    |
| Slew Rate (Note 7)                             | +25°C   | -             | 90   | -   | -         | 90   | -   | V/μs  |    |
| <b>DIGITAL INPUT CHARACTERISTICS</b>           |         |               |      |     |           |      |     |       |    |
| Input Voltage (High), V <sub>IH</sub>          | Full    | 2.0           | -    | -   | 2.0       | -    | -   | V     |    |
| Input Voltage (Low), V <sub>IL</sub>           | Full    | -             | -    | 0.8 | -         | -    | 0.8 | V     |    |
| Input Current (V <sub>IL</sub> = 0V)           | Full    | -             | 10   | 40  | -         | 10   | 40  | μA    |    |
| Input Current (V <sub>IH</sub> = +5V)          | Full    | -             | 10   | 40  | -         | 10   | 40  | μA    |    |
| <b>SAMPLE/HOLD CHARACTERISTICS</b>             |         |               |      |     |           |      |     |       |    |
| Acquisition Time (Note 8)                      | (0.1%)  | +25°C         | -    | 350 | -         | -    | 350 | -     | ns |
|  |         | Full          | -    | -   | 500       | -    | -   | 500   | ns |
|  | (0.01%) | +25°C         | -    | 500 | -         | -    | 500 | -     | ns |
|  |         | Full          | -    | -   | 900       | -    | -   | 900   | ns |
| Aperture Time (Note 3)                         | +25°C   | -             | 20   | -   | -         | 20   | -   | ns    |    |
| Effective Aperture Delay Time (See Glossary)   | +25°C   | -50           | -25  | 0   | -50       | -25  | 0   | ns    |    |
| Aperture Uncertainty                           | +25°C   | -             | 0.1  | -   | -         | 0.1  | -   | ns    |    |
| Droop Rate (Note 9)                            | +25°C   | -             | 0.01 | -   | -         | 0.01 | -   | μV/μs |    |
|  | Full    | -             | -    | 100 | -         | -    | 10  | μV/μs |    |
| Hold Step Error (Note 10)                      | +25°C   | -             | 0.5  | -   | -         | 0.5  | -   | mV    |    |
| Hold Mode Settling Time (0.01%)                | +25°C   | -             | 100  | 200 | -         | 100  | 200 | ns    |    |
| Hold Mode Feedthru 20V <sub>p-p</sub> , 100kHz | Full    | -             | -88  | -   | -         | -88  | -   | dB    |    |
| <b>POWER SUPPLY CHARACTERISTICS</b>            |         |               |      |     |           |      |     |       |    |
| Positive Supply Current                        | Full    | -             | 18   | 22  | -         | 18   | 24  | mA    |    |
| Negative Supply Current                        | Full    | -             | 19   | 23  | -         | 19   | 25  | mA    |    |
| Power Supply Rejection, V+, V- (Note 11)       | Full    | 86            | 100  | -   | 86        | 100  | -   | dB    |    |

**NOTES:**

1. Absolute maximum ratings are limiting values, applied individually, beyond which serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Internal Power Dissipation may limit Output Current below ±17mA.
3. Derived from computer simulation only; not tested.
4. +V<sub>CM</sub> = ±10V DC.
5. V<sub>i</sub> = 200mV Step; R<sub>L</sub> = 2K; C<sub>L</sub> = 50pF
6. Full power bandwidth based on slew rate measurement using 
$$FPBW = \frac{SLEW\ RATE}{2\pi V_{peak}}$$
7. V<sub>O</sub> = 20V Step; R<sub>L</sub> = 2K; C<sub>L</sub> = 50pF.
8. V<sub>O</sub> = 10V Step; R<sub>L</sub> = 2K; C<sub>L</sub> = 50pF.
9. This parameter is measured at ambient temperature extremes in a high speed test environment. Consequently, steady state heating effects from internal power dissipation are not included.
10. V<sub>IN</sub> = 0V; V<sub>IH</sub> = +3.5V; t<sub>r</sub> = 22ns (V<sub>IL</sub> to V<sub>IH</sub>). See graph.
11. Based on a three volt delta in each supply, i.e. 15V = ±1.5V DC.
12. V<sub>OUT</sub> = 200mV<sub>p-p</sub>, R<sub>L</sub> = 2K, C<sub>L</sub> = 50pF.

Distortion of wave shape occurs beyond 100KHz due to slew rate enhancement circuitry



### Applying the HA-5330

The HA-5330 has the uncommitted differential inputs of an op amp, allowing the Sample/Hold function to be combined with many conventional op amp circuit ideas. See the Harris Application Note 517 for a collection of circuit ideas.

### Layout

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01 to 0.1 $\mu$ F, ceramic) should be provided from each power supply terminal to the Supply GND Terminal on pin 11.

### Applications

The HA-5330 is configured as a unity gain noninverting amplifier by simply connecting the output (pin 7) to the inverting input (pin 14). As an input device for a fast successive - approximation A/D converter, it offers an extremely high throughput rate. Also, the HA-5330's pedestal error is adjustable to zero by using an Offset Adjust potentiometer (10K to 50K) center tapped to V-.

The ideal ground connections are pin 11 (Supply Ground) directly to the system Supply Common, and pin 12 (Signal Ground) directly to the system Signal Ground (Analog Ground).

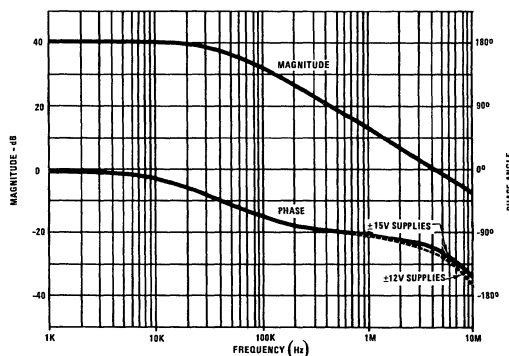
### Hold Capacitor

The HA-5330 includes a 90pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Specifications section is based on the internal capacitor).

### Output Stage

The HA-5330 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the  $\bar{S}/H$  output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

MAGNITUDE AND PHASE RESPONSE  
(Closed Loop Gain = 100)



### Glossary of Terms

#### Acquisition Time:

The time required following a "sample" command, for the output to reach its final value within  $\pm 0.1\%$  or  $\pm 0.01\%$ . This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

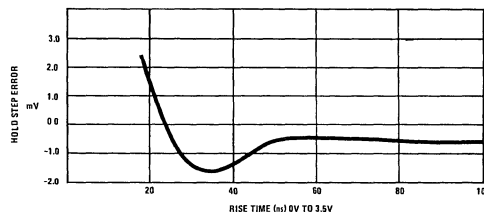
#### Aperture Time:

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

#### Hold Step Error:

Hold step error is the output shift due to charge transfer from the sample to the hold mode. It is also referred to as "offset step" or "pedestal error".

HOLD STEP ERROR vs.  $\bar{S}/H$  CONTROL RISE TIME



#### Effective Aperture Delay Time (EADT):

The difference between the digital delay time from the Hold command to the opening of the  $\bar{S}/H$  switch, and the propagation time from the analog input to the switch.

EADT may be positive, negative or zero. If zero, the  $\bar{S}/H$  amplifier will output a voltage equal to  $V_{IN}$  at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of  $V_{IN}$  that occurred before the Hold command.

#### Aperture Uncertainty:

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

## High Speed, Low Distortion, Precision Monolithic Sample and Hold Amplifier

August 1991

### Features

- Fast Acquisition Time (0.01%) ..... 700ns
- Fast Hold Mode Settling Time (0.01%) ..... 200ns
- Low Distortion (Hold Mode) ..... -72dBc  
( $V_{IN} = 200\text{kHz}$ ,  $F_s = 450\text{kHz}$ ,  $5V_{p-p}$ )
- Bandwidth Minimally Affected By External  $C_H$
- Fully Differential Analog Inputs
- Built-in 135pF Hold Capacitor
- Pin Compatible with HA-5320

### Applications

- High Bandwidth Precision Data Acquisition Systems
- Inertial Navigation and Guidance Systems
- Ultrasonics
- SONAR
- RADAR

### Ordering Information

| MODEL NUMBER | OPERATING TEMPERATURE RANGE | PRODUCT DESCRIPTION |
|--------------|-----------------------------|---------------------|
| HA1-5340-5   | 0°C to +75°C                | 14 Pin Ceramic DIP  |
| HA1-5340-9   | -40°C to +85°C              | 14 Pin Ceramic DIP  |

### Description

The HA-5340 combines the advantages of two sample/hold architectures to create a new generation of monolithic sample/hold. High amplitude, high frequency signals can be sampled with very low distortion being introduced. The combination of exceptionally fast acquisition time and specified/characterized hold mode distortion is an industry first. Additionally, the AC performance is only minimally affected by additional hold capacitance.

To achieve this level of performance, the benefits of an integrating output stage have been combined with the advantages of a buffered hold capacitor. To the user this translates to a front-end stage that has high bandwidth due

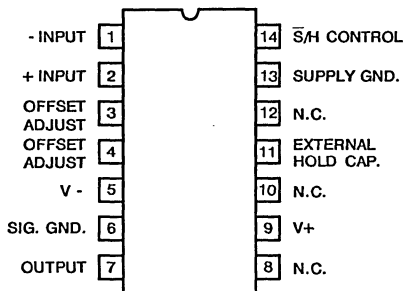
to charging only a small capacitive load and an output stage with constant pedestal error which can be nulled out using the offset adjust pins. Since the performance penalty for additional hold capacitance is low, the designer can further minimize pedestal error and droop rate without sacrificing speed.

Low distortion, fast acquisition, and low droop rate are the result, making the HA-5340 the obvious choice for high speed, high accuracy sampling systems.

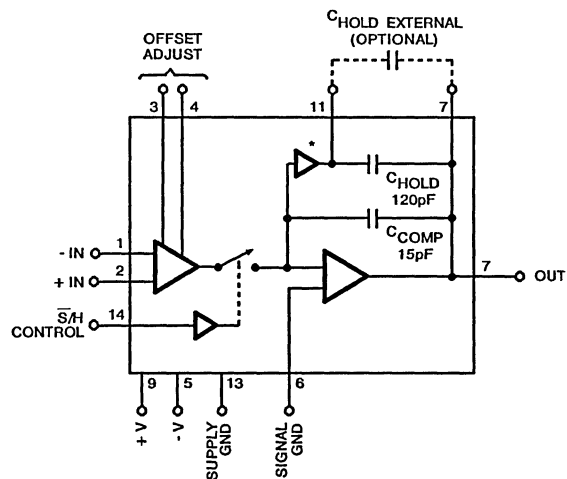
For a Military temperature range version request the HA-5340/883 data sheet.

### Pinout

HA1-5340 (CERAMIC DIP)  
TOP VIEW



### Functional Diagram



\* Buffer acts as a buffer in sample mode, acts as a closed switch in hold mode.

## Specifications HA-5340

### Absolute Maximum Ratings (Note 1)

|   |          |
|---|----------|
| Voltage Between V+ and V- Terminals ..... | 36V      |
| Differential Input Voltage .....          | 24V      |
| Digital Input Voltage .....               | +8V, -6V |
| Output Current, Continuous .....          | ±20mA    |
| Junction Temperature .....                | +175°C   |

### Operating Temperature Range

|                                 |  |
|---------------------------------|--|
| HA-5340-9 .....                 | $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  |
| HA-5340-5 .....                 | $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$    |
| Storage Temperature Range ..... | $-65^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ |

**Electrical Specifications** Test Conditions (Unless Otherwise Specified)  $V_{\text{SUPPLY}} = \pm 15.0\text{V}$ ;  $C_H = \text{Internal} = 135\text{pF}$ ; Digital Input:  $V_{\text{IL}} = +0.8\text{V}$  (Sample),  $V_{\text{IH}} = +2.0\text{V}$  (Hold). Non-Inverting Unity Gain Configuration (Output tied to -Input),  $R_L = 2\text{K}$ ,  $C_L = 60\text{pF}$

| PARAMETER   | TEMP  | HA-5340-9<br>HA-5340-5 |      |      | UNITS |
|---|-------|------------------------|------|------|-------|
|   |       | MIN                    | TYP  | MAX  |       |
| <b>INPUT CHARACTERISTICS</b>                              |       |                        |      |      |       |
| Input Voltage Range                                       | Full  | -10                    | -    | +10  | V     |
| Input Resistance (Note 2)                                 | +25°C | -                      | 1    | -    | MΩ    |
| Input Capacitance   | +25°C | -                      | -    | 3    | pF    |
| Input Offset Voltage                                      | +25°C | -                      | -    | 1.5  | mV    |
|   | Full  | -                      | -    | 3.0  | mV    |
| Offset Voltage Temperature Coefficient                    | Full  | -                      | -    | 30   | μV/°C |
| Bias Current  | +25°C | -                      | ±70  | -    | nA    |
|   | Full  | -                      | -    | ±350 | nA    |
| Offset Current  | +25°C | -                      | ±50  | -    | nA    |
|   | Full  | -                      | -    | ±350 | nA    |
| Common Mode Range   | Full  | -10                    | -    | +10  | V     |
| CMRR (±10 Vdc) (Note 3)                                   | +25°C | -                      | 83   | -    | dB    |
|   | Full  | 72                     | -    | -    | dB    |
| <b>TRANSFER CHARACTERISTICS</b>                           |       |                        |      |      |       |
| Gain, DC  | +25°C | 110                    | 140  | -    | dB    |
| Gain Bandwidth Product $C_H$ External = 0pF               | Full  | -                      | 10   | -    | MHz   |
| $C_H$ External = 100pF                                    | Full  | -                      | 9.6  | -    | MHz   |
| $C_H$ External = 1000pF                                   | Full  | -                      | 6.7  | -    | MHz   |
| <b>TRANSIENT RESPONSE</b>                                 |       |                        |      |      |       |
| Rise Time (200mV step)                                    | +25°C | -                      | 20   | 30   | ns    |
| Overshoot (200mV step)                                    | +25°C | -                      | 35   | 50   | %     |
| Slew Rate (10V step)                                      | +25°C | 40                     | 60   | -    | V/μs  |
| <b>DIGITAL INPUT CHARACTERISTICS</b>                      |       |                        |      |      |       |
| Input Voltage (High), $V_{\text{IH}}$                     | Full  | 2.0                    | -    | -    | V     |
| Input Voltage (Low), $V_{\text{IL}}$                      | Full  | -                      | -    | 0.8  | V     |
| Input Current $V_{\text{IL}} = 0\text{V}$ $I_{\text{IL}}$ | Full  | -                      | 7    | 40   | μA    |
| Input Current $V_{\text{IH}} = 5\text{V}$ $I_{\text{IH}}$ | Full  | -                      | 4    | 40   | μA    |
| <b>OUTPUT CHARACTERISTICS</b>                             |       |                        |      |      |       |
| Output Voltage  | Full  | -10                    | -    | +10  | V     |
| Output Current  | Full  | -10                    | -    | +10  | mA    |
| Full Power Bandwidth (Slew Rate Limited) (Note 4)         | Full  | 0.6                    | 0.9  | -    | MHz   |
| Output Resistance - Hold Mode                             | +25°C | -                      | 0.05 | 0.1  | Ω     |
|   | Full  | -                      | 0.07 | 0.15 | Ω     |
| <b>TOTAL OUTPUT NOISE, D.C. TO 10MHz</b>                  |       |                        |      |      |       |
| Sample Mode   | +25°C | -                      | 325  | 400  | μVrms |
| Hold Mode   | +25°C | -                      | 325  | 400  | μVrms |

## Specifications HA-5340

**Electrical Specifications** Test Conditions (Unless Otherwise Specified)  $V_{SUPPLY} = \pm 15.0V$ ;  $C_H = \text{Internal} = 135pF$ ; Digital Input:  $V_{IL} = +0.8V$  (Sample),  $V_{IH} = +2.0V$  (Hold). Non-Inverting Unity Gain Configuration (Output tied to -Input),  $R_L = 2K$ ,  $C_L = 60pF$

| PARAMETER   | TEMP  | HA-5340-9<br>HA-5340-5 |     |      | UNITS |               |
|---|---|------------------------|-----|------|-------|---------------|
|   |   | MIN                    | TYP | MAX  |       |               |
| <b>DISTORTION CHARACTERISTICS</b>                                 |   |                        |     |      |       |               |
| <b>SAMPLE MODE</b>  |   |                        |     |      |       |               |
| Signal to Noise Ratio<br>(RMS Signal to RMS noise)                | $V_{IN} = 200kHz$ (20Vp-p)  | Full                   | -   | 115  | -     | dB            |
| Total Harmonic Distortion   | $V_{IN} = 200kHz$ , 5Vp-p   | Full                   | -90 | -100 | -     | dBc           |
|   | $V_{IN} = 200kHz$ , 10Vp-p  | Full                   | -76 | -82  | -     | dBc           |
|   | $V_{IN} = 200kHz$ , 20Vp-p  | Full                   | -70 | -74  | -     | dBc           |
|   | $V_{IN} = 500kHz$ , 5Vp-p   | Full                   | -66 | -75  | -     | dBc           |
|   | Intermodulation Distortion<br>$V_{IN} = 10Vp-p$ ( $f_1 = 20kHz$ , $f_2 = 21kHz$ ) | Full                   | -78 | -83  | -     | dBc           |
| <b>HOLD MODE (50% Duty Cycle <math>\bar{S}/H</math>)</b>          |   |                        |     |      |       |               |
| Signal to Noise Ratio<br>(RMS Signal to RMS noise)                |   |                        |     |      |       |               |
| Fs = 450kHz   | $V_{IN} = 200kHz$ , 5Vp-p   | +25°C                  | -   | 76   | -     | dB            |
|   | $V_{IN} = 200kHz$ , 10Vp-p  | +25°C                  | -   | 76   | -     | dB            |
| Total Harmonic Distortion<br>Fs = 450kHz                          | $V_{IN} = 200kHz$ , 5Vp-p   | +25°C                  | -   | -72  | -     | dBc           |
|   | $V_{IN} = 200kHz$ , 10Vp-p  | +25°C                  | -   | -66  | -     | dBc           |
|   | $V_{IN} = 200kHz$ , 20Vp-p  | +25°C                  | -   | -56  | -     | dBc           |
| Fs = 450kHz   | $V_{IN} = 100kHz$ , 5Vp-p   | +25°C                  | -   | -84  | -     | dBc           |
|   | $V_{IN} = 100kHz$ , 10Vp-p  | +25°C                  | -   | -71  | -     | dBc           |
|   | $V_{IN} = 100kHz$ , 20Vp-p  | +25°C                  | -   | -61  | -     | dBc           |
| Fs = 2f <sub>IN</sub> (Nyquist)                                   | $V_{IN} = 20kHz$ , 5Vp-p  | +25°C                  | -   | -95  | -     | dBc           |
|   | $V_{IN} = 50kHz$ , 5Vp-p  | +25°C                  | -   | -91  | -     | dBc           |
|   | $V_{IN} = 100kHz$ , 5Vp-p   | +25°C                  | -   | -82  | -     | dBc           |
| Intermodulation Distortion<br>Fs = 450kHz                         | $V_{IN} = 10Vp-p$<br>( $f_1 = 20kHz$ , $f_2 = 21kHz$ )                            | +25°C                  | -   | -79  | -     | dBc           |
| <b>SAMPLE/HOLD CHARACTERISTICS</b>                                |   |                        |     |      |       |               |
| Acquisition Time  | 10V Step to 0.01%   | +25°C                  | -   | 700  | -     | ns            |
|   |   | Full                   | -   | -    | 900   | ns            |
|   | 10V Step to 0.1%  | +25°C                  | -   | 430  | 600   | ns            |
| Drop Rate ( $C_H = \text{Internal}$ )                             |   | +25°C                  | -   | 0.1  | -     | $\mu V/\mu s$ |
|   |   | Full                   | -   | -    | 95    | $\mu V/\mu s$ |
| Hold Step Error ( $V_{IL} = 0V$ , $V_{IH} = 4.0V$ , $t_r = 5ns$ ) |   | +25°C                  | -   | 15   | -     | mV            |
| Hold Mode Settling Time (to $\pm 1mV$ )                           |   | Full                   |     | 200  | 300   | ns            |
| Hold Mode Feedthrough (20Vp-p, 200kHz, sine)                      |   | Full                   | -   | -76  | -     | dB            |
| EADT (Effective Aperture Delay Time)                              |   | +25°C                  | -   | -15  | -     | ns            |
| Aperture Uncertainty  |   | +25°C                  | -   | 0.2  | -     | ns            |
| <b>POWER SUPPLY CHARACTERISTICS</b>                               |   |                        |     |      |       |               |
| Positive Supply Current   |   | Full                   | -   | 19   | 25    | mA            |
| Negative Supply Current   |   | Full                   | -   | 19   | 25    | mA            |
| PSRR (V or -V, 10% delta)   |   | Full                   | 75  | 82   | -     | dB            |

- NOTES: 1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Derived from Computer Simulation only, not tested.
3. +CMRR is measured from 0V to +10V, -CMRR is measured from 0V to -10V
4. Based on the calculation  $FPBW = \text{Slew Rate}/2\pi V_{peak}$  ( $V_{peak} = 10V$ ).

5  
SAMPLE AND HOLD  
AMPLIFIERS

## HA-5340

### Applying the HA-5340

The HA-5340 has the uncommitted differential inputs of an op amp, allowing the Sample and Hold function to be combined with many conventional op amp circuits. See the Harris Application Note 517 for a collection of circuit ideas.

#### LAYOUT

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01 to 0.1 $\mu$ F, ceramic) should be provided from each power supply terminal to the Supply Ground terminal on pin 13.

The ideal ground connections are pin 6 (SIG. Ground) directly to the system Signal Ground, and pin 13 (Supply Ground) directly to the system Supply Common.

#### HOLD CAPACITOR

The HA-5340 includes a 135pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Specifications section is based on this internal capacitor).

Additional capacitance may be added between pins 7 and 11. This external hold capacitance will reduce droop rate at the expense of acquisition time, and provide other trade-offs as shown in the Performance Curves.

The hold capacitor  $C_H$  should have high insulation resistance and low dielectric absorption, to minimize droop errors. Teflon<sup>®</sup>, polystyrene and polypropylene dielectric capacitor types offer good performance over the specified operating temperature range.

The hold capacitor terminal (pin 11) remains at virtual ground potential. Any PC connection to this terminal should be kept short and "guarded" by the ground plane, since nearby signal lines or power supply voltages will introduce errors due to drift current.

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### Applications

Figure 1 shows the HA-5340 connected as a unity gain noninverting amplifier — its most widely used configuration. As an input device for a fast successive — approximation A/D converter, it offers very high throughput rate for a monolithic IC sample/hold amplifier. Also, the HA-5340's hold step error is adjustable to zero using the Offset Adjust potentiometer, to deliver a 12-bit accurate output from the converter.

The HA-5340 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the S/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

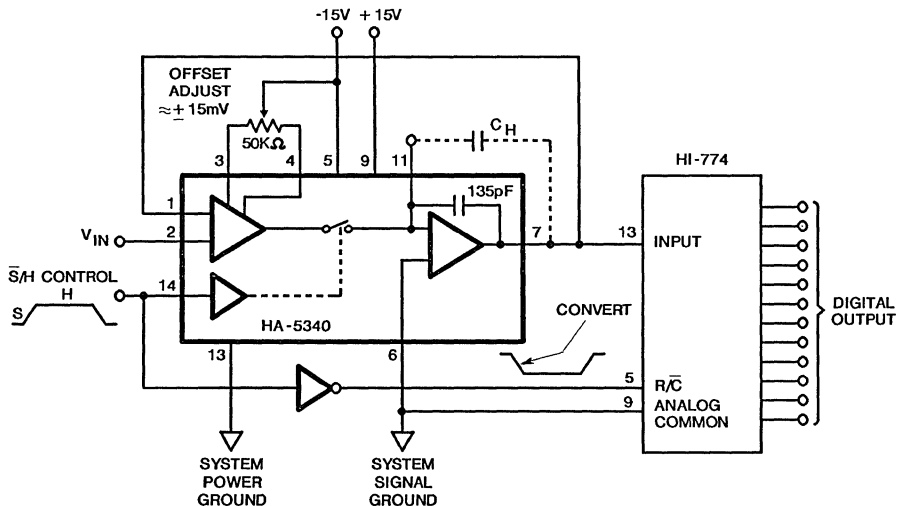
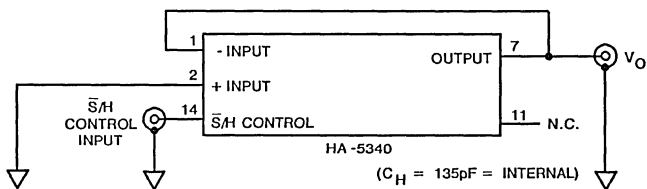


FIGURE 1.  
TYPICAL HA-5340 CONNECTIONS; NONINVERTING UNITY GAIN MODE

NOTE: Pin Numbers Refer to DIP Package Only.

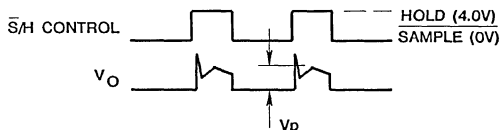
Test Circuits

HOLD STEP ERROR AND DROOP RATE



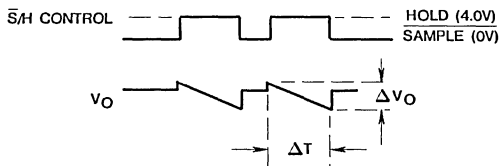
HOLD STEP ERROR

1. Observe the "hold step" voltage  $V_p$ :



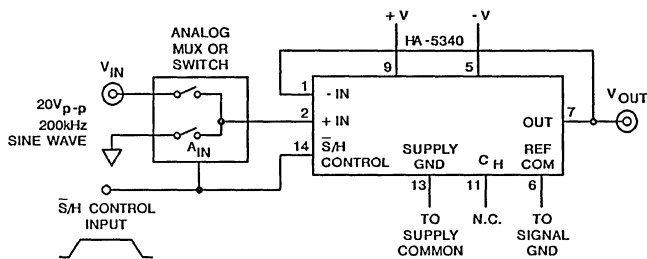
DROOP RATE TEST

1. Observe the voltage "droop",  $\Delta V_O / \Delta T$ :



2. Measure the slope of the output during hold,  $\Delta V_O / \Delta T$ .
3. Droop can be positive or negative - usually to one rail or the other not to GND.

HOLD MODE FEED THROUGH ATTENUATION



Feedthrough in dB =  $20 \text{ Log } \frac{V_{OUT}}{V_{IN}}$  where:

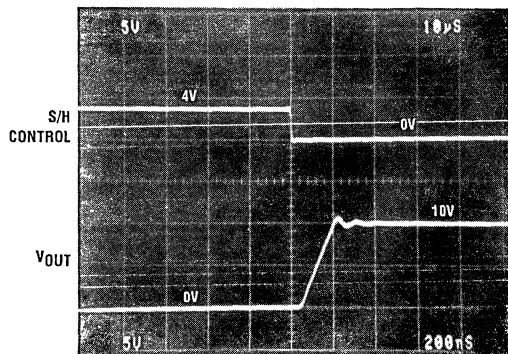
$V_{OUT}$  = Volts<sub>p-p</sub>, Hold Mode,

$V_{IN}$  = Volts<sub>p-p</sub>.

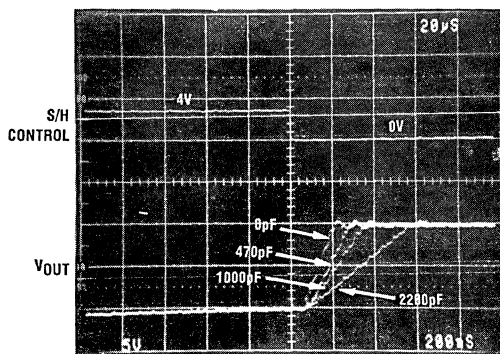
# HA-5340

**Performance Curves**  $V_S = \pm 15V$ ,  $T_A = +25^\circ C$ , unless otherwise specified.

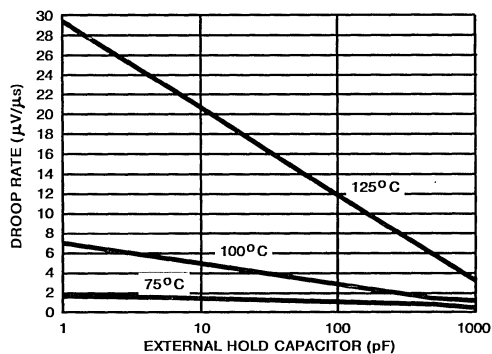
TACQ POS 0 TO +10 STEP



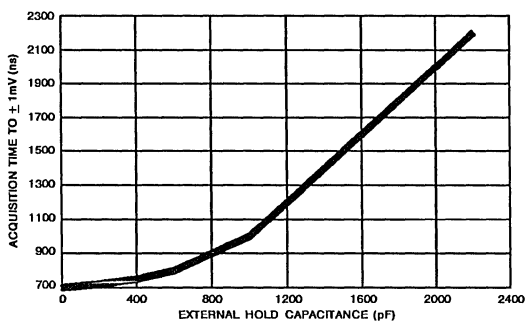
TACQ vs. ADDITIONAL  $C_H$



DROOP RATE vs. HOLD CAPACITOR SIZE



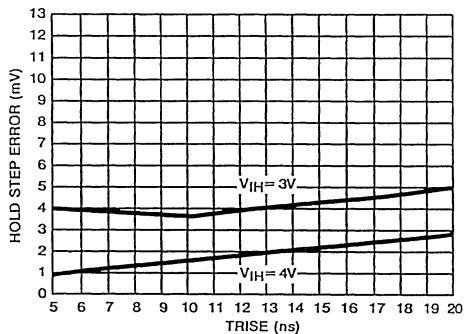
ACQUISITION TIME (0.01%) vs. HOLD CAPACITANCE



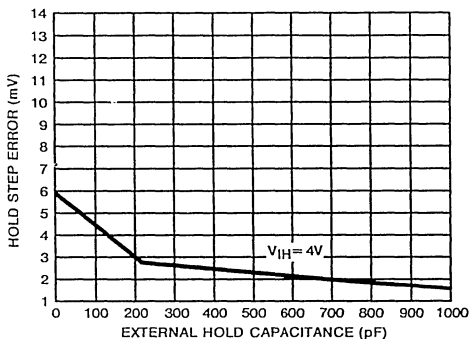
# HA-5340

**Performance Curves (Continued)**  $V_S = \pm 15V$ ,  $T_A = +25^\circ C$ , unless otherwise specified.

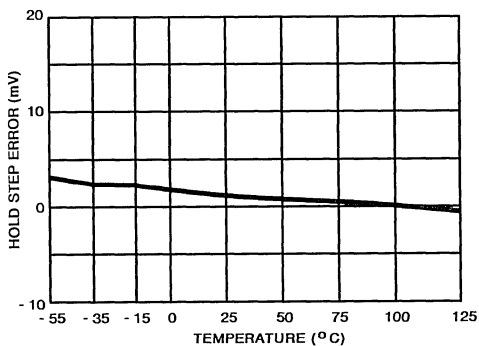
**HOLD STEP ERROR vs.  $T_{RISE}$**   
 $C_H = \text{Internal}$ ; Temperature =  $+25^\circ C$



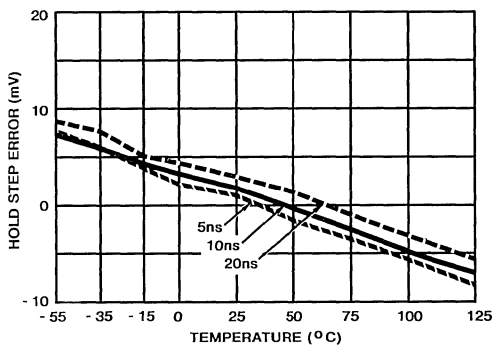
**HOLD STEP ERROR vs. HOLD CAPACITANCE**  
 $T_{RISE} = 5ns$ ; Temperature =  $+25^\circ C$



**HOLD STEP ERROR vs. TEMPERATURE**  
 $V_{IH} = 4V$ ,  $C_H = 470pF$



**HOLD STEP ERROR vs. TEMPERATURE**  
 $V_{IH} = 4V$ ,  $C_H = \text{Internal}$   
 $t_r = 5ns, 10ns, 20ns$

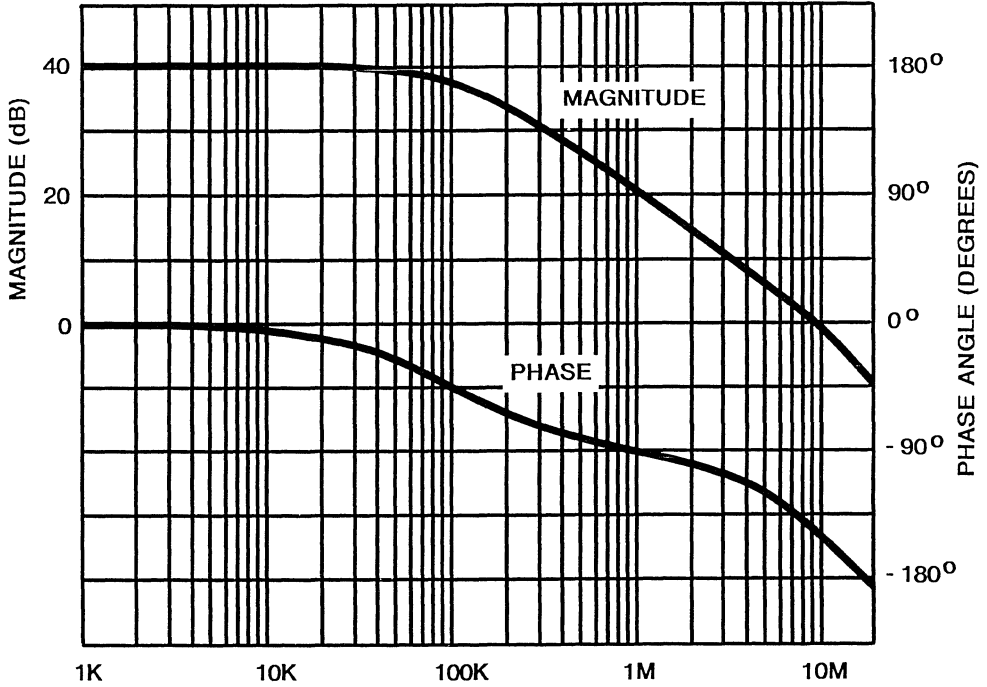




# HA-5340

**Performance Curves** (Continued)  $V_S = \pm 15V$ ,  $T_A = +25^\circ C$ , unless otherwise specified.

**CLOSED LOOP PHASE/GAIN**  
 $A_V = +100, \pm 15V$  and  $\pm 12V$  Supplies\*

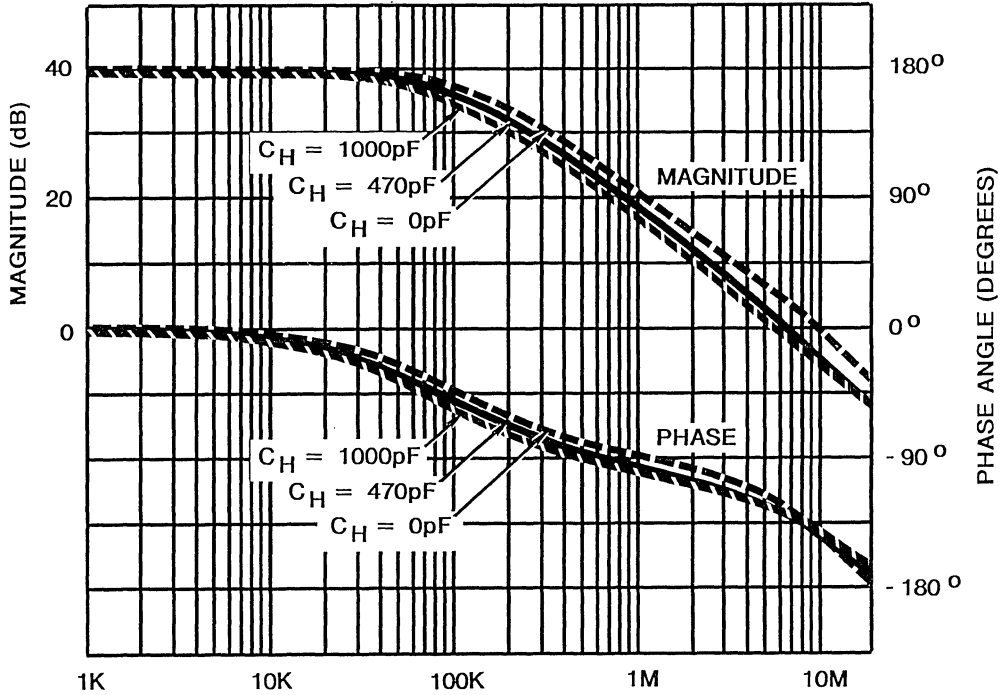


\*  $\pm 15V$  and  $\pm 12V$  supplies trace the same line within the width of the line, therefore only one line is shown.

# HA-5340

**Performance Curves** (Continued)  $V_S = \pm 15V$ ,  $T_A = +25^\circ C$ , unless otherwise specified.

CLOSED LOOP PHASE/GAIN  
 $A_V = +100$



## Die Characteristics

|                         |                    |
|-------------------------|--------------------|
| Transistor Count .....  | 196                |
| Die Size .....          | 139 x 84 x 19 mils |
| Thermal Impedance:      |                    |
| $\theta_{ja}$ .....     | 75°C/W             |
| $\theta_{jc}$ .....     | 15°C/W             |
| Tie Substrate to: ..... | -V                 |
| Process .....           | Bipolar-DI         |



## DIFFERENTIAL AMPLIFIERS

|   | PAGE |
|---|------|
| <b>SELECTION GUIDE</b> .....                                      | 6-2  |
| <b>DIFFERENTIAL AMPLIFIERS DATA SHEETS</b>                        |      |
| CA 3028A, B    Differential/Cascode Amplifier .....               | 6-3  |
| CA 3049        Dual High-Frequency Differential Amplifier .....   | 6-14 |
| CA 3053        Differential/Cascode Amplifier .....               | 6-3  |
| CA 3054        Transistor Array-Dual Differential Amplifier ..... | 6-19 |
| CA 3102        Dual High-Frequency Differential Amplifier .....   | 6-14 |

# Selection Guide

## DIFFERENTIAL AMPLIFIERS

| TYPE    | DESCRIPTION                      | FEATURES  | FREQ. RANGE DC TO MHz | A (TYP) dB | BW (3dB POINT) (TYP) MHz                  | 1/F NF (TYP) dB | AGC RANGE (TYP) dB | PIN CT AND PKG TYPE* |
|---------|----------------------------------|---|-----------------------|------------|---|-----------------|--------------------|----------------------|
| CA3028A | Differential /Cascode Amplifiers | <ul style="list-style-type: none"> <li>• Balanced differential-amplifier configuration with controlled constant-current source</li> <li>• RF, IF, and video frequency capability</li> <li>• Balanced agc capability</li> <li>• Operation from DC to 500MHz</li> <li>• CA3028B is controlled for input offset voltage, current, and input bias current, and is intended for "balance" requirements</li> <li>• Push-pull inputs and outputs</li> <li>• CA3028 and CA3053 are identical except for 100MHz noise specification</li> </ul> | 120                   | 40□        | -   | 7.2             | 62                 | 8E, M, S, T          |
| CA3028B |                                  |   | 120                   | 40         | 8   | 7.2             | 62                 |                      |
| CA3049  | Dual High Frequency              |   | 500                   | 22         | 1.35▲                                     | 53              | 75                 | 12T                  |
| CA3053  | Differential /Cascode Amplifier  |   | 120                   | 40         | Recommended for IF Amplifier Applications |                 |                    | 8E, M, S, T          |
| CA3054  | Dual Independent                 |   | 120                   | 32         | 550†                                      | 3.25            | 75                 | 14E, M               |
| CA3102  | Dual High-Frequency              |   | 500                   | 22         | 1.35▲                                     | 1.5             | 7.5                | 14E, M               |

\*See Packaging and Ordering Information in Section 12 ▲ GHz †f<sub>T</sub> (MHz) □G<sub>p</sub> Min. at 100MHz: Cascode = 16dB; Diff Ampl. = 14dB.

CA3028B: V<sub>OUT</sub> = 11.5V<sub>p-p</sub>. T<sub>A</sub> Range: -55 to +125°C except for type CA3054 (0 to +85°C)



HARRIS

# CA3028A, CA3028B CA3053

Differential/Cascode Amplifiers

For Commercial & Industrial Equipment from DC to 120MHz

August 1991

### Features

- Controlled for Input Offset Voltage, Input Offset Current and Input Bias Current (CA3028 Series Only)
- Balanced Differential Amplifier Configuration with Controlled Constant-Current Source
- Single-Ended and Dual-Ended Operation

### Applications

- RF and IF Amplifiers (Differential or Cascode)
- DC, Audio and Sense Amplifiers
- Converter in the Commercial FM Band
- Oscillator
- Mixer
- Limiter
- Companion Application Note, ICAN 5337 "Application of the CA3028 Integrated Circuit Amplifier in the HF and VHF Ranges." This note covers characteristics of different operating modes, noise performance, mixer, limiter, and amplifier design considerations.

### Description

The CA3028A and CA3028B are differential/cascode amplifiers designed for use in communications and industrial equipment operating at frequencies from DC to 120MHz.

The CA3028B is like the CA3028A but is capable of premium performance particularly in critical DC and differential amplifier applications requiring tight controls for input offset voltage, input offset current, and input bias current.

The CA3053 is similar to the CA3028A and CA3028B but is recommended for IF amplifier applications.

The CA3028A, CA3028B, and CA3053 are available in 8-lead packages as shown below. When ordering these devices, it is important to add the appropriate suffix letter to the device.

### Package/Lead Options

| SMALL OUTLINE (150 MIL) | STRAIGHT LEAD TO-5 | DUAL-IN-LINE FORMED-LEAD TO-5 | DUAL-IN-LINE PLASTIC (MINI-DIP) |
|-------------------------|--------------------|-------------------------------|---------------------------------|
| CA3028AM                | CA3028A*           | CA3028AS                      | CA3028AE                        |
| CA3028BM                | CA3028B*           | CA3028BS                      | CA3028BE                        |
| CA3053M                 | CA3053*            | CA3053S                       | CA3053E                         |

\*Most types in a straight-lead TO-5 package carry a "T" suffix. This one does not. Order type number as shown.

### Schematic Diagram

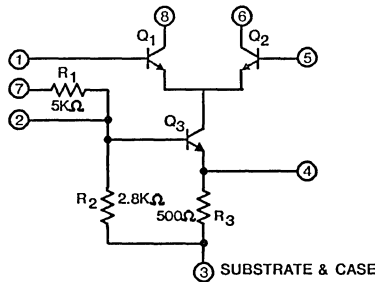


FIGURE 1. CA3028A, CA3028B AND CA3053

6  
DIFFERENTIAL AMPLIFIERS

## CA3028A, CA3028B, CA3053

### ABSOLUTE MAXIMUM RATINGS at T<sub>A</sub> = 25°C

#### DISSIPATION

At T<sub>A</sub> Up to 85°C (CA3028A, CA3028B, CA3053) ..... 450 mW

At T<sub>A</sub> 85°C (CA3028A, CA3028B, CA3053) ..... Derate linearly 5 mW/°C

#### AMBIENT-TEMPERATURE RANGE

Operating ..... -55°C to +125°C

Storage ..... -65°C to +150°C

#### LEAD TEMPERATURE (DURING SOLDERING)

At distance 1/16 + 1/32 (1.59 + 0.79 mm) from case for 10 seconds max ..... +265°C

### MAXIMUM VOLTAGE RATINGS at T<sub>A</sub> = 25°C

| TERMINAL No.   | 1 | 2                     | 3                     | 4                     | 5                     | 6                     | 7                     | 8                     |
|----------------|---|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| -1             |   | 0 to -15 <sup>▲</sup> | 0 to -15 <sup>▲</sup> | 0 to -15 <sup>▲</sup> | +5 to -5              | *                     | *                     | +20 <sup>⊕</sup> to 0 |
| 2              |   |                       | +5 to -11             | +5 to -1              | +15 <sup>⊕</sup> to 0 | *                     | +15 <sup>⊕</sup> to 0 | *                     |
| 3 <sup>‡</sup> |   |                       |                       | +10 to 0              | +15 <sup>⊕</sup> to 0 | +30 <sup>●</sup> to 0 | +15 <sup>⊕</sup> to 0 | +30 <sup>●</sup> to 0 |
| 4              |   |                       |                       |                       | +15 <sup>⊕</sup> to 0 | *                     | *                     | *                     |
| 5              |   |                       |                       |                       |                       | +20 <sup>⊕</sup> to 0 | *                     | *                     |
| 6              |   |                       |                       |                       |                       |                       | *                     | *                     |
| 7              |   |                       |                       |                       |                       |                       |                       | *                     |
| 8              |   |                       |                       |                       |                       |                       |                       |                       |

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of the horizontal terminal 4 with respect to terminal 2 is -1 to +5 volts.

‡ Terminal #3 is connected to the substrate and case.

\* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe, if the specified voltage limits between all other terminals are not exceeded.

▲ Limit is -12V for CA3053.

⊕ Limit is +15V for CA3053.

⊕ Limit is +12V for CA3053.

● Limit is +24V for CA3028A and +18V for CA3053.

### MAXIMUM CURRENT RATINGS

| TERMINAL No. | I <sub>IN</sub> mA | I <sub>OUT</sub> mA |
|--------------|--------------------|---------------------|
| 1            | 0.6                | 0.1                 |
| 2            | 4                  | 0.1                 |
| 3            | 0.1                | 23                  |
| 4            | 20                 | 0.1                 |
| 5            | 0.6                | 0.1                 |
| 6            | 20                 | 0.1                 |
| 7            | 4                  | 0.1                 |
| 8            | 20                 | 0.1                 |

### ELECTRICAL CHARACTERISTICS at T<sub>A</sub> = 25°C

| CHARACTERISTIC  | SYMBOL                                 | TEST CIRCUIT Fig. | SPECIAL TEST CONDITIONS | LIMITS TYPE CA3028A |   |           | LIMITS TYPE CA3028B |           |              | LIMITS TYPE CA3053 |           |            | UNITS        | TYPICAL CHARACTERISTIC CURVES Fig. |            |
|---|--|-------------------|-------------------------|---------------------|---|-----------|---------------------|-----------|--------------|--------------------|-----------|------------|--------------|------------------------------------|------------|
|   |  |                   |                         | Min.                | Typ.  | Max.      | Min.                | Typ.      | Max.         | Min.               | Typ.      | Max.       |              |                                    |            |
| <b>STATIC CHARACTERISTICS</b>                                 |  |                   |                         |                     |   |           |                     |           |              |                    |           |            |              |                                    |            |
|   |  |                   |                         | +V <sub>CC</sub>    | -V <sub>EE</sub>                                |           |                     |           |              |                    |           |            |              |                                    |            |
| Input Offset Voltage  | V <sub>IO</sub>                        | 2                 |                         | 6V<br>12V           | 6V<br>12V                                       | -         | -                   | -         | 0.98<br>5    | 5                  | -         | -          | mV           | 4                                  |            |
| Input Offset Current  | I <sub>IO</sub>                        | 3a                |                         | 6V<br>12V           | 6V<br>12V                                       | -         | -                   | -         | 0.56<br>1.06 | 5<br>6             | -         | -          | μA           | 4                                  |            |
| Input Bias Current  | I <sub>I</sub>                         | 3a                |                         | 6V<br>12V           | 6V<br>12V                                       | -         | 16.6<br>36          | 70<br>106 | -            | 16.6<br>36         | 40<br>80  | -          | -            | μA                                 | 5a         |
|   |  | 3b                |                         | 9V<br>12V           | -   | -         | -                   | -         | -            | -                  | -         | 29<br>36   | 85<br>125    |                                    | 5b         |
| Quiescent Operating Current                                   | I <sub>6</sub><br>or<br>I <sub>8</sub> | 3a                |                         | 6V<br>12V           | 6V<br>12V                                       | 0.8<br>2  | 1.25<br>3.3         | 2<br>5    | 1<br>2.5     | 1.25<br>3.3        | 1.5<br>4  | -          | -            | mA                                 | 6a<br>7    |
|   |  | 3b                |                         | 9V<br>12V           | -   | -         | -                   | -         | -            | -                  | -         | 1.2<br>2.0 | 2.2<br>3.3   |                                    | 3.5<br>5.0 |
| AGC Bias Current (Into Constant-Current Source Terminal No.7) | I <sub>7</sub>                         | 8a                |                         | 12V<br>12V          | V <sub>AGC</sub> = +9<br>V <sub>AGC</sub> = +12 | -         | 1.28<br>1.65        | -         | -            | 1.28<br>1.65       | -         | -          | -            | mA                                 | 8b         |
|   |  | -                 |                         | 9V<br>12V           | -   | -         | -                   | -         | -            | -                  | -         | -          | 1.15<br>1.55 |                                    | -          |
| Input Current (Terminal No.7)                                 | I <sub>7</sub>                         | -                 |                         | 6V<br>12V           | 6V<br>12V                                       | 0.5<br>1  | 0.85<br>1.65        | 1<br>2.1  | 0.5<br>1     | 0.85<br>1.65       | 1<br>2.1  | -          | -            | mA                                 | -          |
| Device Dissipation  | P <sub>T</sub>                         | 3a                |                         | 6V<br>12V           | 6V<br>12V                                       | 24<br>120 | 36<br>175           | 54<br>260 | 24<br>120    | 36<br>175          | 42<br>220 | -          | -            | mW                                 | 9          |
|   |  | 3b                |                         | 9V<br>12V           | -   | -         | -                   | -         | -            | -                  | -         | -          | 50<br>100    |                                    | 80<br>150  |

CA3028A, CA3028B, CA3053

ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$  (cont'd)

| CHARACTERISTIC                                | SYMBOL                          | TEST CIRCUIT<br>Fig. | SPECIAL TEST CONDITIONS   | LIMITS<br>TYPE CA3028A  |                 |     | LIMITS<br>TYPE CA3028B |            |                          | LIMITS<br>TYPE CA3053 |      |     | UNITS            | TYPICAL CHARACTERISTIC CURVE |       |
|---|---------------------------------|----------------------|---|---|-----------------|-----|------------------------|------------|--------------------------|-----------------------|------|-----|------------------|------------------------------|-------|
|   |                                 |                      |   | Min   | Typ.            | Max | Min                    | Typ.       | Max                      | Min                   | Typ. | Max |                  |                              |       |
| DYNAMIC CHARACTERISTICS                       |                                 |                      |   |   |                 |     |                        |            |                          |                       |      |     |                  |                              |       |
| Power Gain                                    | G <sub>P</sub>                  | 10a                  | f = 100 MHz   | Cascode   | 16              | 20  | -                      | 16         | 20                       | -                     | -    | -   | -                | dB                           | 10b   |
|   |                                 | 11a.d                | V <sub>CC</sub> = +9V   | Diff.-Ampl  | 14              | 17  | -                      | 14         | 17                       | -                     | -    | -   | -                | -                            | dB    |
| Noise Figure                                  | NF                              | 10a                  | f = 10.7 MHz  | Cascode   | 35              | 39  | -                      | 35         | 39                       | -                     | 35   | 39  | -                | dB                           | 10b * |
|   |                                 | 11a                  | V <sub>CC</sub> = +9V   | Diff.-Ampl  | 28              | 32  | -                      | 28         | 32                       | -                     | 28   | 32  | -                | dB                           | 11b * |
| Input Admittance                              | Y <sub>11</sub>                 | 10a                  | f = 100 MHz   | Cascode   | -               | 7.2 | 9                      | -          | 7.2                      | 9                     | -    | -   | -                | mmho                         | 10c   |
|   |                                 | 11a.d                | V <sub>CC</sub> = +9V   | Diff.-Ampl  | -               | 6.7 | 9                      | -          | 6.7                      | 9                     | -    | -   | -                | mmho                         | 11c,e |
| Reverse Transfer Admittance                   | Y <sub>12</sub>                 | -                    | f = 10.7 MHz  | V <sub>CC</sub> = +9V   | Cascode         |     |                        |            | 0.6 + j 1.6              |                       |      |     | mmho             | 12                           |       |
|   |                                 |                      |   |   | Diff.-Ampl      |     |                        |            | 0.5 + j 0.5              |                       |      |     | mmho             | 13                           |       |
| Cascode                                       |                                 |                      |   |   | 0.0003 - j 0    |     |                        |            | mmho                     | 14                    |      |     |                  |                              |       |
| Diff.-Ampl                                    |                                 |                      |   |   | 0.01 - j 0.0002 |     |                        |            | mmho                     | 15                    |      |     |                  |                              |       |
| Forward Transfer Admittance                   | Y <sub>21</sub>                 | -                    | f = 10.7 MHz  | V <sub>CC</sub> = +9V   | Cascode         |     |                        |            | 99 - j 18                |                       |      |     | mmho             | 16                           |       |
|   |                                 |                      |   |   | Diff.-Ampl      |     |                        |            | -37 + j 0.5              |                       |      |     | mmho             | 17                           |       |
| Cascode                                       |                                 |                      |   |   | 0 + j 0.08      |     |                        |            | mmho                     | 18                    |      |     |                  |                              |       |
| Diff.-Ampl                                    |                                 |                      |   |   | 0.04 + j 0.23   |     |                        |            | mmho                     | 19                    |      |     |                  |                              |       |
| Power Output (Untuned)                        | P <sub>o</sub>                  | 20a                  | f = 10.7 MHz  | Diff.-Ampl<br>50 Ω Input-Output   | -               | 5.7 | -                      | -          | 5.7                      | -                     | -    | -   | μW               | 20b                          |       |
| AGC Range (Max. Power Gain to Full Cutoff)    | AGC                             | 21a                  | V <sub>CC</sub> = +9V   | Diff.-Ampl.   | -               | 62  | -                      | -          | 62                       | -                     | -    | -   | dB               | 21b                          |       |
| Voltage Gain                                  | at<br>f = 10.7 MHz              | A                    | 22a   | f = 10.7 MHz  | Cascode         | -   | 40                     | -          | 40                       | -                     | -    | 40  | -                | dB                           | 22b   |
|   |                                 |                      | 22c   | V <sub>CC</sub> = +0V<br>R <sub>L</sub> = 1 kΩ  | Diff.-Ampl.     | -   | 30                     | -          | -                        | 30                    | -    | -   | 30               | -                            | dB    |
|   | Differential<br>at<br>f = 1 kHz |                      | 23  | V <sub>CC</sub> = +6V,<br>R <sub>L</sub> = 2 kΩ<br>V <sub>EE</sub> = -6V,<br>V <sub>CC</sub> = +12V,<br>R <sub>L</sub> = 1.6 kΩ<br>V <sub>EE</sub> = -12V |                 | -   | -                      | -          | 35                       | 38                    | 42   | -   | -                | -                            | dB    |
| Max. Peak-to-Peak Output Voltage at f = 1 kHz | V <sub>o</sub> (P-P)            | 23                   | V <sub>CC</sub> = +6V,<br>R <sub>L</sub> = 2 kΩ<br>V <sub>CC</sub> = +12V,<br>R <sub>L</sub> = 1.6 kΩ | V <sub>EE</sub> = -6V,<br>V <sub>EE</sub> = -12V  | -               | -   | -                      | 7          | 11.5                     | -                     | -    | -   | V <sub>P-P</sub> | -                            |       |
| Bandwidth at -3 dB point                      | BW                              | 23                   | V <sub>CC</sub> = +6V,<br>R <sub>L</sub> = 2 kΩ   | V <sub>EE</sub> = -6V,  | -               | -   | -                      | -          | 7.3                      | -                     | -    | -   | MHz              | -                            |       |
|   |                                 |                      | V <sub>CC</sub> = +12V,<br>R <sub>L</sub> = 1.6 kΩ  | V <sub>EE</sub> = -12V,   | -               | -   | -                      | -          | -                        | 8                     | -    | -   | -                | -                            | -     |
| Common-Mode Input-Voltage Range               | V <sub>CMR</sub>                | 24                   | V <sub>CC</sub> = +6V,<br>V <sub>CC</sub> = +12V  | V <sub>EE</sub> = -6V,<br>V <sub>EE</sub> = -12V  | -               | -   | -                      | -2.5<br>-5 | (-3.2 - 4.5)<br>(-7 - 9) | 4<br>7                | -    | -   | -                | V                            |       |
| Common-Mode Rejection Ratio                   | CMR                             | 24                   | V <sub>CC</sub> = +6V,<br>V <sub>CC</sub> = +12V  | V <sub>EE</sub> = -6V,<br>V <sub>EE</sub> = -12V  | -               | -   | -                      | 60<br>60   | 110<br>90                | -                     | -    | -   | -                | dB                           |       |
| Input Impedance at f = 1 kHz                  | Z <sub>IN</sub>                 | -                    | V <sub>CC</sub> = +6V,<br>V <sub>CC</sub> = +12V  | V <sub>EE</sub> = -6V,<br>V <sub>EE</sub> = -12V  | -               | -   | -                      | -          | 5.5<br>3                 | -                     | -    | -   | -                | kΩ                           |       |
| Peak-to-Peak Output Current                   | I <sub>P-P</sub>                | -                    | V <sub>CC</sub> = +9V   | f = 10.7 MHz  | 2               | 4   | 7                      | 2.5        | 4                        | 6                     | 2    | 4   | 7                | mA                           | -     |
|   |                                 |                      | V <sub>CC</sub> = +12V  | e <sub>in</sub> = 400 mV<br>Diff.-Ampl.   | 3.5             | 6   | 10                     | 4.5        | 6                        | 8                     | 3.5  | 6   | 10               | -                            |       |

\* Does not apply to CA3053

6  
DIFFERENTIAL AMPLIFIERS



**DEFINITION OF TERMS**

**AGC Bias Current**

The current drawn by the device from the AGC-voltage source, at maximum AGC voltage.

**AGC Range**

The total change in voltage gain (from maximum gain to complete cutoff) which may be achieved by application of the specified range of dc voltage to the AGC input terminal of the device.

**Common-Mode Rejection Ratio**

The ratio of the full differential voltage gain to the common-mode voltage gain.

**Device Dissipation**

The total power drain of the device with no signal applied and no external load current.

**Input Bias Current**

The average value (one-half the sum) of the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

**Input Offset Current**

The difference in the currents at the two input terminals when the quiescent operating voltages at the two output

terminals are equal.

**Input Offset Voltage**

The difference in the dc voltages which must be applied to the input terminals to obtain equal quiescent operating voltages (zero output offset voltage) at the output terminals.

**Noise Figure**

The ratio of the total noise power of the device and a resistive signal source to the noise power of the signal source alone, the signal source representing a generator of zero impedance in series with the source resistance.

**Power Gain**

The ratio of the signal power developed at the output of the device to the signal power applied to the input, expressed in dB.

**Quiescent Operating Current**

The average (dc) value of the current in either output terminal.

**Voltage Gain**

The ratio of the change in output voltage at either output terminal with respect to ground, to a change in input voltage at either input terminal with respect to ground, with the other input terminal at ac ground.

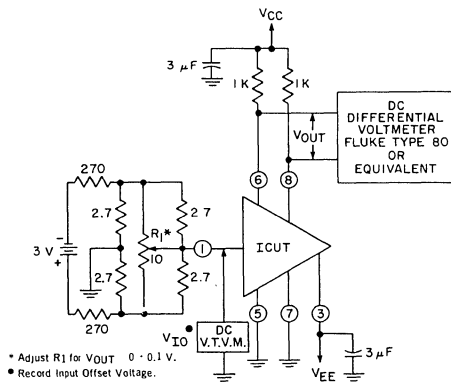


Fig. 2 - Input offset voltage test circuit for CA3028B.

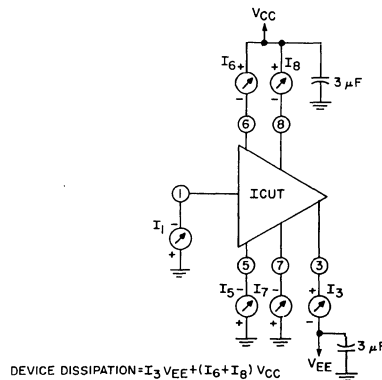


Fig. 3a - Input offset current, input bias current, device dissipation, and quiescent operating current test circuit for CA3028A and CA3028B.

# CA3028A, CA3028B, CA3053

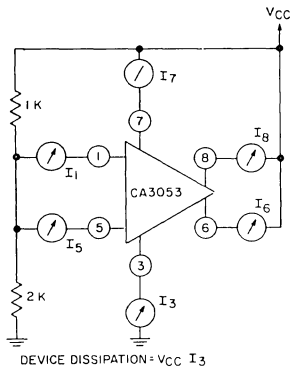


Fig. 3b - Input bias current, device dissipation and quiescent operating current test circuit for CA3053.

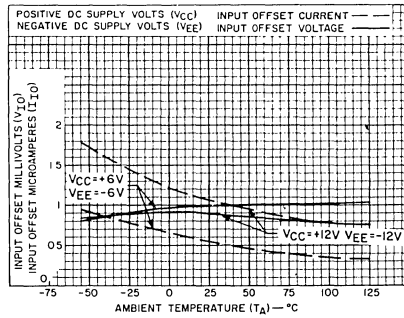


Fig. 4 - Input offset voltage and input offset current for CA3028B.

## TYPICAL CHARACTERISTICS

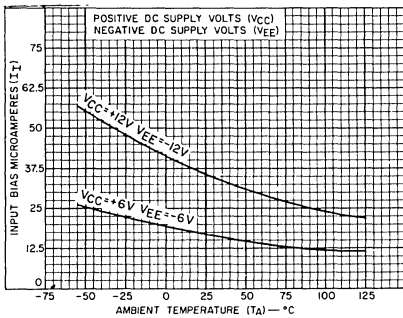


Fig. 5a - Input bias current vs. ambient temperature for CA3028A and CA3028B.

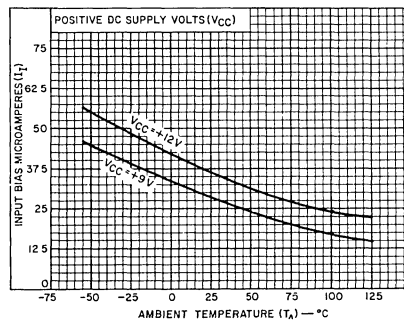


Fig. 5b - Input bias current vs. ambient temperature for CA3053.

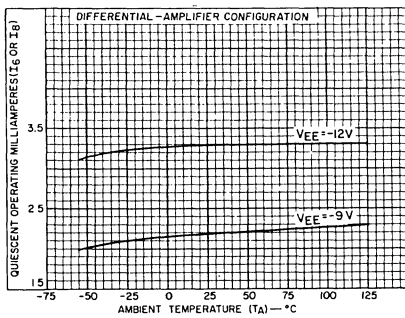


Fig. 6a - Quiescent operating current vs. ambient temperature for CA3028A and CA3028B.

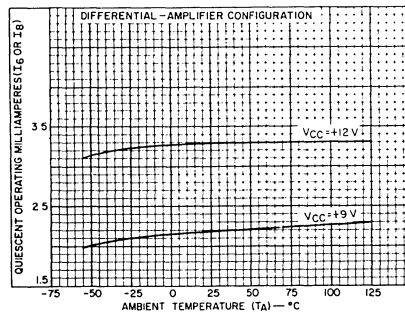


Fig. 6b - Quiescent operating current vs. ambient temperature for CA3053.

6  
DIFFERENTIAL AMPLIFIERS

# CA3028A, CA3028B, CA3053

## TYPICAL CHARACTERISTICS (Continued)

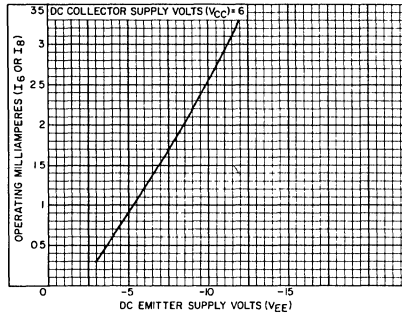


Fig. 7 - Operating current vs.  $V_{EE}$  voltage for CA3028A and CA3028B.

## TYPICAL CHARACTERISTICS AND TEST CIRCUITS

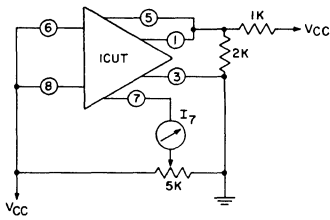


Fig. 8a - AGC bias current test circuit (differential-amplifier configuration) for CA3028A and CA3028B.

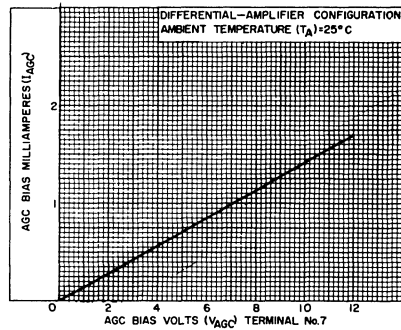


Fig. 8b - AGC bias current vs. bias volts (terminal No. 7) for CA3028A and CA3028B.

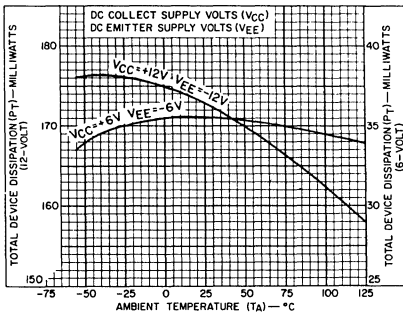


Fig. 9 - Device dissipation vs. temperature for CA3028A and CA3028B.

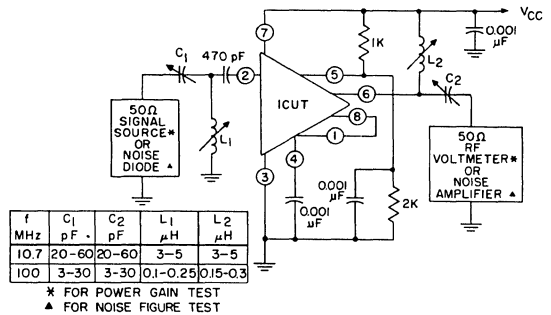


Fig. 10a - Power gain and noise figure test circuit (cascode configuration) for CA3028A, CA3028B and CA3053\*

\* 10.7 MHz Power Gain Test Only.

# CA3028A, CA3028B, CA3053

## TYPICAL CHARACTERISTICS AND TEST CIRCUITS (Continued)

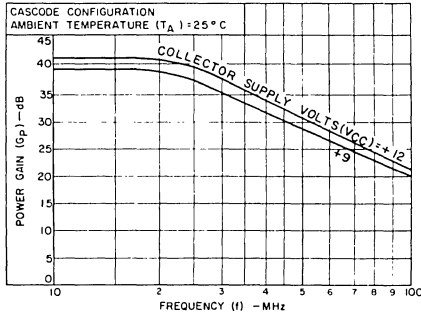


Fig. 10b - Power gain vs. frequency (cascode configuration) for CA3028A and CA3028B.

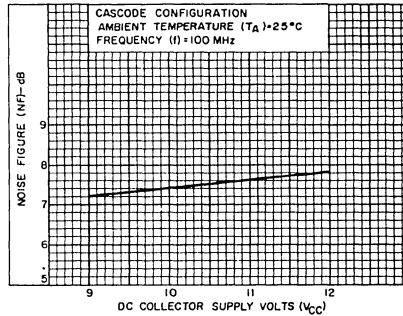
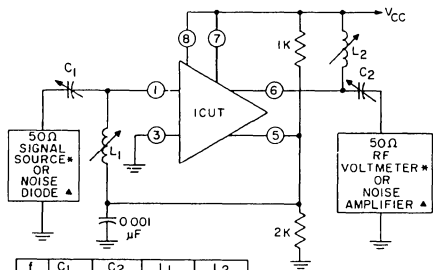


Fig. 10c - 100 MHz noise figure vs. collector supply volts (cascode configuration) for CA3028A and CA3028B

## TYPICAL NOISE FIGURE AND POWER GAIN TEST CIRCUITS AND CHARACTERISTICS



| f<br>MHz | C <sub>1</sub><br>pF | C <sub>2</sub><br>pF | L <sub>1</sub><br>μH | L <sub>2</sub><br>μH |
|----------|----------------------|----------------------|----------------------|----------------------|
| 10.7     | 30-60                | 20-50                | 3-6                  | 3-6                  |
| 100      | 2-15                 | 2-15                 | 0.2-0.5              | 0.2-0.5              |

\* FOR POWER GAIN TEST  
▲ FOR NOISE FIGURE TEST

Fig. 11a - Power gain and noise figure test circuit (differential-amplifier configuration and terminal No. 7 connected to V<sub>CC</sub>) for CA3028A, CA3028B and CA3053\*.

\* 10.7 MHz Power Gain Test Only.

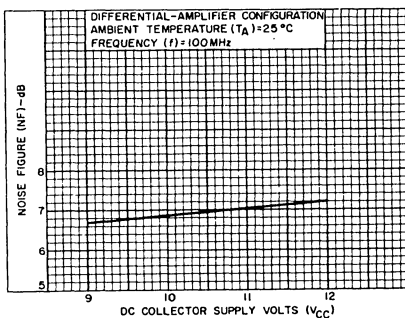


Fig. 11c - 100 MHz noise figure vs. collector supply voltage (differential-amplifier configuration) for CA3028A and CA3028B

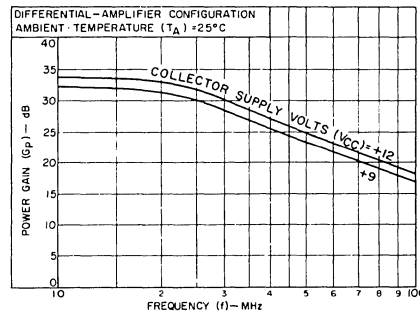
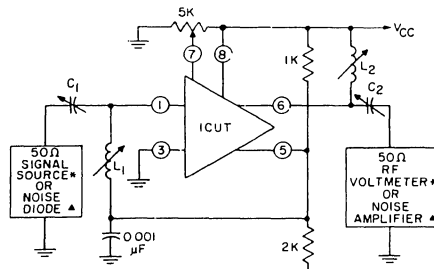


Fig. 11b - Power gain vs. frequency (differential-amplifier configuration) for CA3028A and CA3028B.



| f<br>MHz | C <sub>1</sub><br>pF | C <sub>2</sub><br>pF | L <sub>1</sub><br>μH | L <sub>2</sub><br>μH |
|----------|----------------------|----------------------|----------------------|----------------------|
| 10.7     | 30-60                | 20-50                | 3-6                  | 3-6                  |
| 100      | 2-15                 | 2-15                 | 0.2-0.5              | 0.2-0.5              |

\* FOR POWER GAIN TEST  
▲ FOR NOISE FIGURE TEST

Fig. 11d - Power gain and noise figure test circuit (differential-amplifier configuration) for CA3028A and CA3028B.

# CA3028A, CA3028B, CA3053

## TYPICAL NOISE FIGURE AND POWER GAIN TEST CIRCUITS AND CHARACTERISTICS (Continued)

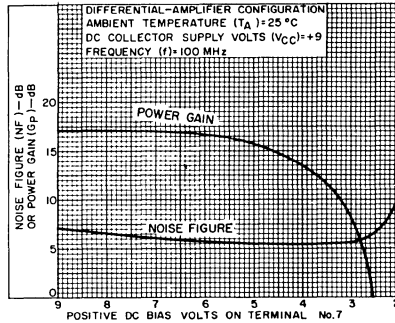


Fig. 11e - 100 MHz noise figure and power gain vs. base-to-emitter bias (terminal No. 7) for CA3028A and CA3028B.

## TYPICAL ADMITTANCE PARAMETERS

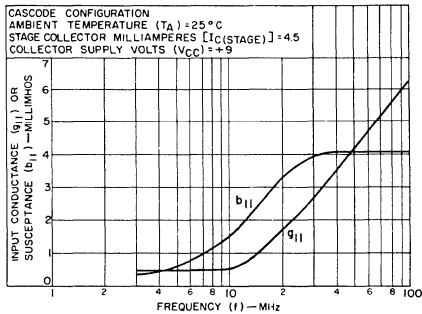


Fig. 12 - Input admittance ( $Y_{11}$ ) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

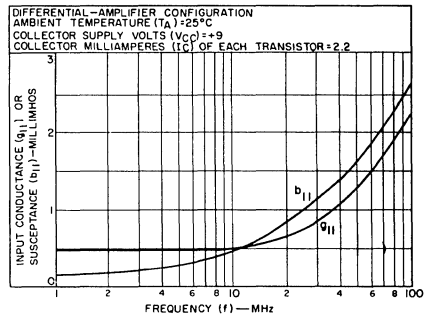


Fig. 13 - Input admittance ( $Y_{11}$ ) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

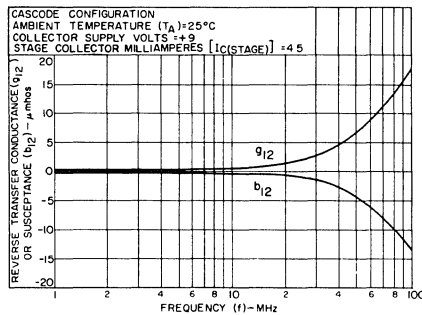


Fig. 14 - Reverse transadmittance ( $Y_{12}$ ) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

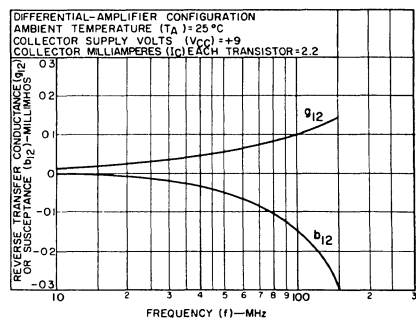


Fig. 15 - Reverse transadmittance ( $Y_{12}$ ) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

# CA3028A, CA3028B, CA3053

## TYPICAL ADMITTANCE PARAMETERS (Continued)

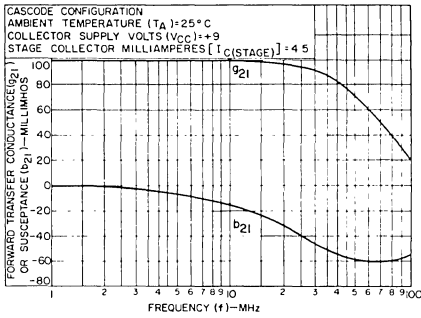


Fig. 16 - Forward transadmittance ( $Y_{21}$ ) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

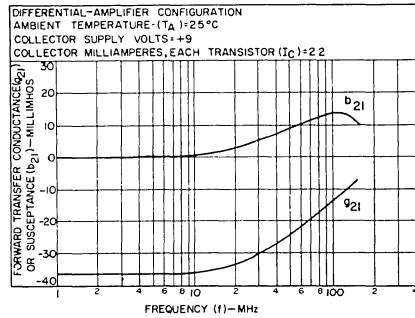


Fig. 17 - Forward transadmittance ( $Y_{21}$ ) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

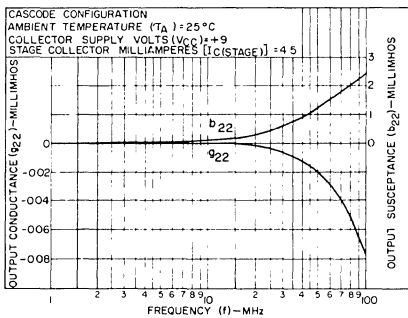


Fig. 18 - Output admittance ( $Y_{22}$ ) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

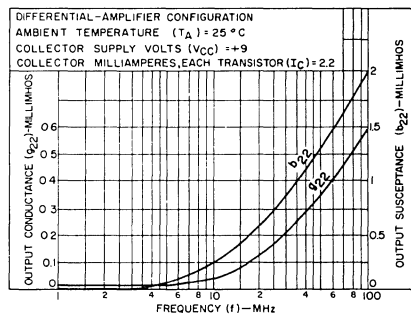


Fig. 19 - Output admittance ( $Y_{22}$ ) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

## TYPICAL TEST CIRCUITS AND CHARACTERISTICS

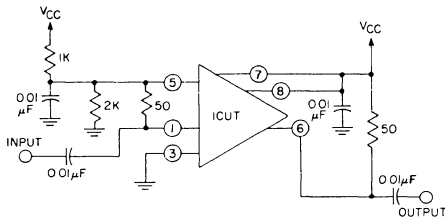


Fig. 20a - Output power test circuit for CA3028A and CA3028B.

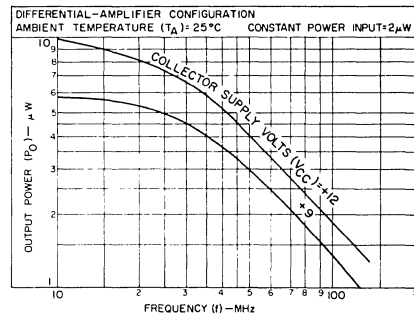


Fig. 20b - Output power vs. frequency - 50  $\Omega$  input and 50  $\Omega$  output (differential-amplifier configuration) for CA3028A and CA3028B.

# CA3028A, CA3028B, CA3053

## TYPICAL TEST CIRCUITS AND CHARACTERISTICS (Continued)

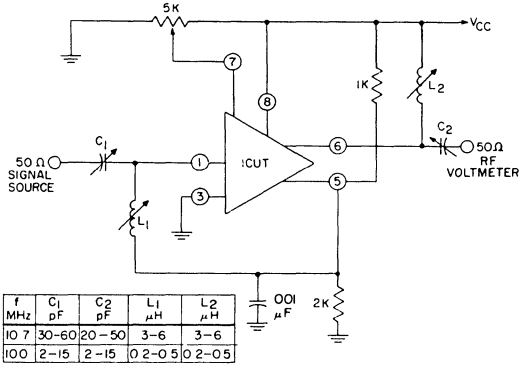


Fig. 21a - AGC range test circuit (differential amplifier) for CA3028A and CA3028B.

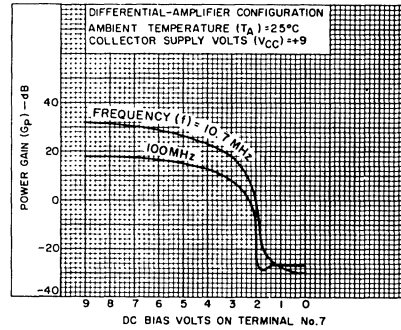


Fig. 21b - AGC characteristics for CA3028A and CA3028B.

## TEST CIRCUITS AND TYPICAL CHARACTERISTICS

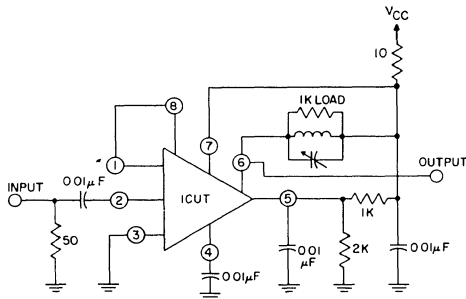


Fig. 22a - Transfer characteristic (voltage gain) test circuit (10.7 MHz) cascode configuration for CA3028A, CA3028B and CA3053.

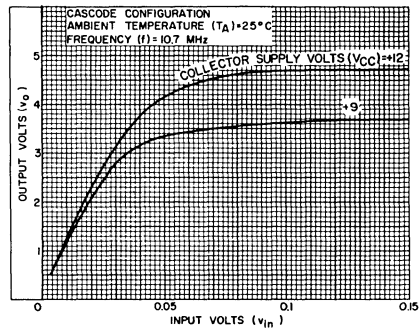


Fig. 22b - Transfer characteristics (cascode configuration) for CA3028A, CA3028B and CA3053.

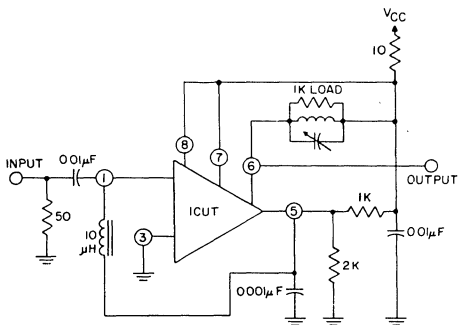


Fig. 22c - Transfer characteristic (voltage gain) test circuit (10.7 MHz) differential-amplifier configuration for CA3028A, CA3028B and CA3053.

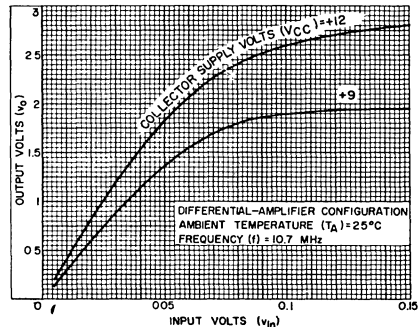
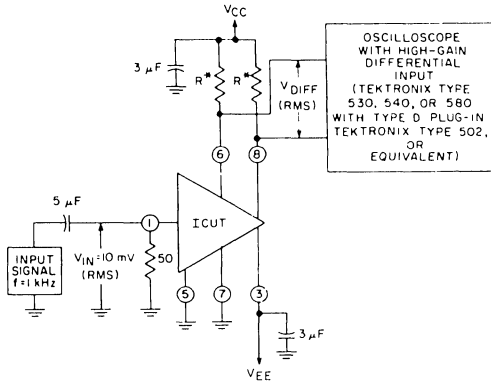


Fig. 22d - Transfer characteristics (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

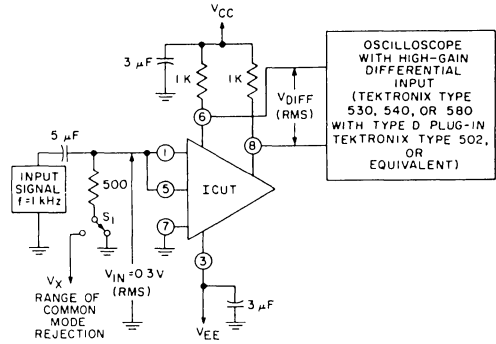
## CA3028A, CA3028B, CA3053

### TEST CIRCUITS AND TYPICAL CHARACTERISTICS (Continued)



- \* For  $R = 1.6 \text{ k}\Omega$  - ( $V_{CC} = 12\text{V}$ ,  $V_{EE} = -12\text{V}$ )
- For  $R = 2 \text{ k}\Omega$  - ( $V_{CC} = 6\text{V}$ ,  $V_{EE} = -6\text{V}$ )

Fig. 23 - Differential voltage gain, maximum peak-to-peak output voltage, and bandwidth test circuit for CA3028B.



- For CMR test:  $S_1$  to ground
- For input common-mode voltage range test:  $S_1$  to  $V_X$

$$\text{Common mode rejection ratio} = 20 \log_{10} \frac{(A^*) (2) (0.3)}{V_{\text{DIFF}} (\text{RMS})}$$

- \*  $A$  = Single-ended voltage gain.

Fig. 24 - Common-mode rejection ratio and common-mode input-voltage range test circuit for CA3028B.



## Dual High-Frequency Differential Amplifiers For Low-Power Applications Up to 500MHz

August 1991

### Features

- Power Gain 23dB (Typ) ..... 200MHz
- Noise Figure 4.6dB (Typ) ..... 200MHz
- Two Differential Amplifiers on a Common Substrate
- Independently Accessible Inputs and Outputs
- Full Military Temperature Range... -55°C to +125°C

### Applications

- VHF Amplifiers
- VHF Mixers
- Multifunction Combinations - RF/Mixer/Oscillator;  
Converter/IF
- IF Amplifiers (Differential and/or Cascode)
- Product Detectors
- Doubly Balanced Modulators and Demodulators
- Balanced Quadrature Detectors
- Cascade Limiters
- Synchronous Detectors
- Balanced Mixers
- Synthesizers
- Balanced (Push-Pull) Cascode Amplifiers
- Sense Amplifiers

### Description

The CA3049T and CA3102\* consist of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six transistors which comprise the amplifiers are general-purpose devices which exhibit low  $1/f$  noise and a value of  $f_T$  in excess of 1GHz. These features make the CA3049T and CA3102 useful from DC to 500MHz. Bias and load registers have been omitted to provide maximum application flexibility.

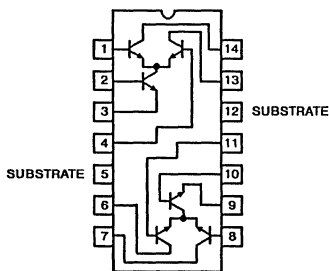
The monolithic construction of the CA3049T and CA3102 provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual-channel applications where matched performance of the two channels is required.

The CA3102 is like the CA3049T except that it has a separate substrate connection for greater design flexibility. The CA3049T is supplied in the 12-lead TO-5 package; the CA3102, in the 14-lead plastic dual-in-line package (E suffix) and in the 14-lead Small Outline package (M suffix).

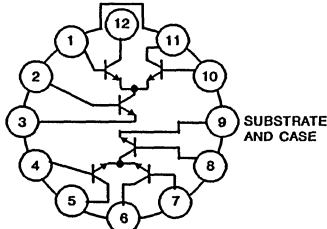
\* Formerly Developmental No. TA6228.

### Pinouts

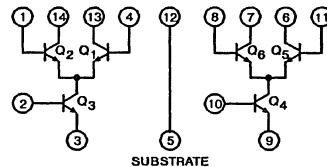
CA3102E, CA3102M  
TOP VIEW



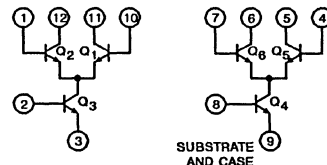
CA3049T  
TOP VIEW



### Schematic Diagrams



CA3102E, CA3102M



CA3049T

## CA3049, CA3102

**MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES,**  
AT  $T_A = 25^\circ\text{C}$

| Power Dissipation, P:                   | CA3049T     | CA3102E                      |
|---|-------------|------------------------------|
| Any one transistor                      | 300         | 300 mW                       |
| Total package                           | 600         | 750 mW                       |
| For $T_A > 55^\circ\text{C}$ Derate at: | 5           | 6.67 mW/ $^\circ\text{C}$    |
| Temperature Range:                      |             |                              |
| Operating                               | -55 to +125 | -55 to +125 $^\circ\text{C}$ |
| Storage                                 | -65 to +150 | -65 to +150 $^\circ\text{C}$ |

The following ratings apply for each transistor in the devices

|   |    |    |
|---|----|----|
| Collector-to-Emitter Voltage, $V_{CEO}$     | 15 | V  |
| Collector-to-Base Voltage, $V_{CBO}$        | 20 | V  |
| Collector-to-Substrate Voltage, $V_{CIO}^*$ | 20 | V  |
| Emitter-to-Base Voltage, $V_{EBO}$          | 5  | V  |
| Collector Current, $I_C$                    | 50 | mA |

\*The collector of each transistor of the CA3049T and CA3102 is isolated from the substrate by an integral diode. The substrate (terminal 9) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

### ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$

| CHARACTERISTICS   | SYMBOLS                          | TEST CONDITIONS  | TEST CIRCUIT | CA3102 LIMITS |                  |      | CA3049T LIMITS |                  |      | TYPICAL CHARACTERISTICS CURVES |            |
|---|----------------------------------|--|--------------|---------------|------------------|------|----------------|------------------|------|--------------------------------|------------|
|   |                                  |  |              | FIG.          | MIN.             | TYP. | MAX.           | MIN.             | TYP. |                                | MAX.       |
| <b>STATIC CHARACTERISTICS</b>                             |                                  |  |              |               |                  |      |                |                  |      |                                |            |
| For Each Differential Amplifier                           |                                  |  |              |               |                  |      |                |                  |      |                                |            |
| Input Offset Voltage                                      | $V_{IO}$                         |  | 1            | ---           | 0.25             | 5    | ---            | 0.25             | ---  | mV                             | -4         |
| Input Offset Current                                      | $I_{IO}$                         | $I_3 = I_9 = 2 \text{ mA}$   | 1            | ---           | 0.3              | 3    | ---            | 0.3              | ---  | $\mu\text{A}$                  | ---        |
| Input Bias Current  | $I_{IB}$                         |  | 1            | ---           | 13.5             | 33   | ---            | 13.5             | 33   | $\mu\text{A}$                  | 5          |
| Temperature Coefficient Magnitude of Input-Offset Voltage | $\frac{ dV_{IO} }{dT}$           |  | 1            | ---           | 1.1              | ---  | ---            | 1.1              | ---  | $\mu\text{V}/^\circ\text{C}$   | 4          |
| For Each Transistor                                       |                                  |  |              |               |                  |      |                |                  |      |                                |            |
| DC Forward Base-to-Emitter Voltage                        | $V_{BE}$                         | $V_{CE} = 6 \text{ V}$<br>$I_C = 1 \text{ mA}$                                     | ---          | 674           | 774              | 874  | ---            | 774              | ---  | mV                             | 6          |
| Temperature Coefficient of Base-to-Emitter Voltage        | $\frac{\Delta V_{BE}}{\Delta T}$ | $V_{CE} = 6 \text{ V}$ , $I_C = 1 \text{ mA}$                                      | ---          | ---           | -0.9             | ---  | ---            | -0.9             | ---  | $\text{mV}/^\circ\text{C}$     | 6          |
| Collector-Cutoff Current                                  | $I_{CBO}$                        | $V_{CB} = 10 \text{ V}$ , $I_E = 0$  | ---          | ---           | 0.0013           | 100  | ---            | 0.0013           | 100  | nA                             | 7          |
| Collector-to-Emitter Breakdown Voltage                    | $V_{(BR)CEO}$                    | $I_C = 1 \text{ mA}$ , $I_B = 0$   | ---          | 15            | 24               | ---  | 15             | 24               | ---  | V                              | ---        |
| Collector-to-Base Breakdown Voltage                       | $V_{(BR)CBO}$                    | $I_C = 10 \mu\text{A}$ , $I_E = 0$   | ---          | 20            | 60               | ---  | 20             | 60               | ---  | V                              | ---        |
| Collector-to-Substrate Breakdown Voltage                  | $V_{(BR)CISO}$                   | $I_C = 10 \mu\text{A}$ , $I_B = 0$ , $I_E = 0$                                     | ---          | 20            | 60               | ---  | 20             | 60               | ---  | V                              | ---        |
| Emitter-to-Base Breakdown Voltage                         | $V_{(BR)EBO}$                    | $I_E = 10 \mu\text{A}$ , $I_C = 0$   | ---          | 5             | 7                | ---  | 5              | 7                | ---  | V                              | ---        |
| <b>DYNAMIC CHARACTERISTICS</b>                            |                                  |  |              |               |                  |      |                |                  |      |                                |            |
| 1/f Noise Figure (For Single Transistor)                  | NF                               | $f = 100 \text{ KHz}$ , $R_S = 500 \Omega$<br>$I_C = 1 \text{ mA}$                 | ---          | ---           | 1.5              | ---  | ---            | 1.5              | ---  | dB                             | 12         |
| Gain Bandwidth Product (For Single Transistor)            | $f_T$                            | $V_{CE} = 6 \text{ V}$ , $I_C = 5 \text{ mA}$                                      | ---          | ---           | 1.35             | ---  | ---            | 1.35             | ---  | $\text{GHz}$                   | 11         |
| Collector-Base Capacitance                                | $C_{CB}$                         | $I_C = 0$ $V_{CB} = 5 \text{ V}$   | *            | ---           | 0.28             | ---  | ---            | 0.28             | ---  | pF                             | 8          |
| Collector-Substrate Capacitance                           | $C_{CI}$                         | $I_C = 0$ $V_{CI} = 5 \text{ V}$   | **           | ---           | 0.15             | ---  | ---            | 0.28             | ---  | pF                             | 8          |
| For Each Differential Amplifier                           |                                  |  |              |               |                  |      |                |                  |      |                                |            |
| Common-Mode Rejection Ratio                               | CMR                              | $I_3 = I_9 = 2 \text{ mA}$   | ---          | ---           | 100              | ---  | ---            | 100              | ---  | dB                             | ---        |
| AGC Range, One Stage                                      | AGC                              | Bias Voltage = -6V   | 2            | ---           | 75               | ---  | ---            | 75               | ---  | dB                             | ---        |
| Voltage Gain, Single-Ended Output                         | A                                | Bias Voltage = -4.2V<br>$f = 10 \text{ MHz}$                                       | 2            | 18            | 22               | ---  | ---            | 22               | ---  | dB                             | 9, 10      |
| Insertion Power Gain                                      | $G_p$                            | $f = 200 \text{ MHz}$  | Cascade      | 3             | ---              | 23   | ---            | 23               | ---  | dB                             | ---        |
| Noise Figure  | NF                               | $V_{CC} = 12 \text{ V}$<br>For Cascade Configuration<br>$I_3 = I_9 = 2 \text{ mA}$ | Cascade      | 3             | ---              | 4.6  | ---            | 4.6              | ---  | dB                             | ---        |
| Input Admittance  | $Y_{11}$                         | For Diff. Amplifier Configuration<br>$I_3 = I_9 = 4 \text{ mA}$                    | Cascade      | ---           | $1.5 + j 2.45$   | ---  | ---            | $1.5 + j 2.45$   | ---  | mmho                           | 14, 16, 18 |
|   |                                  |  | Diff.Amp.    | ---           | $0.878 + j 1.3$  | ---  | ---            | $0.878 + j 1.3$  | ---  | mmho                           | 15, 17, 19 |
| Reverse Transfer Admittance                               | $Y_{12}$                         | (each collector $I_C \approx 2 \text{ mA}$ )                                       | Cascade      | ---           | $0 - j 0.008$    | ---  | ---            | $0 - j 0.008$    | ---  | mmho                           | ---        |
|   |                                  |  | Diff.Amp.    | ---           | $0 - j 0.013$    | ---  | ---            | $0 - j 0.013$    | ---  | mmho                           | ---        |
| Forward Transfer Admittance                               | $Y_{21}$                         |  | Cascade      | ---           | $17.9 - j 30.7$  | ---  | ---            | $17.9 - j 30.7$  | ---  | mmho                           | 26, 28, 30 |
|   |                                  |  | Diff. Amp.   | ---           | $-10.5 + j 13$   | ---  | ---            | $-10.5 + j 13$   | ---  | mmho                           | 27, 29, 31 |
| Output Admittance   | $Y_{22}$                         |  | Cascade      | ---           | $-0.503 - j 15$  | ---  | ---            | $-0.503 - j 15$  | ---  | mmho                           | 20, 22, 24 |
|   |                                  |  | Diff.Amp.    | ---           | $0.071 + j 0.62$ | ---  | ---            | $0.071 + j 0.62$ | ---  | mmho                           | 21, 23, 25 |

\* Terminals 1 & 14 or 7 & 8. (CA3102) 1 & 12 or 6 & 7 (CA3049T)

\*\* Terminals 13 & 4, or 6 & 11. (CA3102) 10 & 11 or 4 & 5 (CA3049T)

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DIFFERENTIAL AMPLIFIERS

# CA3049, CA3102

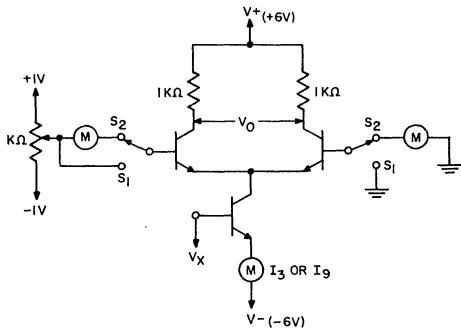


Fig. 1—Static characteristics test circuit for CA3102

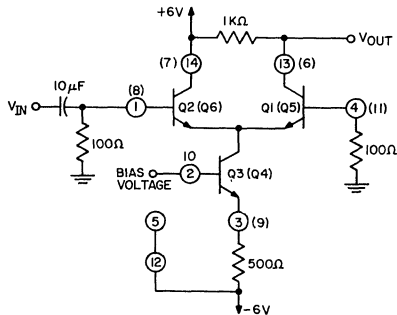
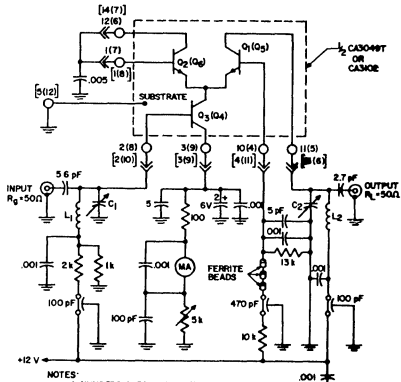


Fig. 2—AGC range and voltage gain test circuit for CA3102



L<sub>1</sub>, L<sub>2</sub> – Approx. 1/2 Turn #18 Tinned Copper Wire, 5/8" Dia.  
 C<sub>1</sub>, C<sub>2</sub> – 15 pF Variable Capacitors (Hammarlund, MAC-15; or Equivalent)  
 All Capacitors in μF Unless Otherwise Indicated  
 All Resistors in Ohms Unless Otherwise Indicated

Fig. 3—200 MHz cascode power gain and noise figure test circuit.

## Typical Characteristics for CA3049T and CA3102

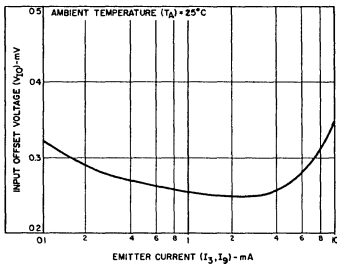


Fig. 4—Input offset voltage vs. emitter current.

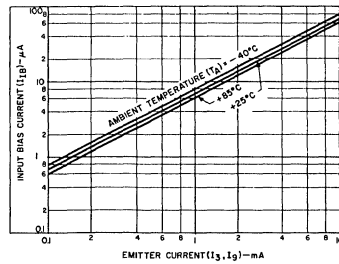


Fig. 5—Input bias current vs. emitter current.

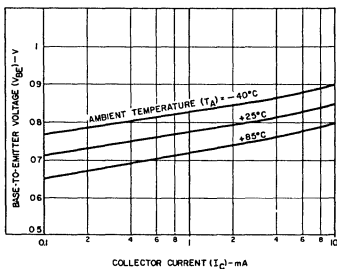


Fig. 6—Base-to-emitter voltage vs. collector current.

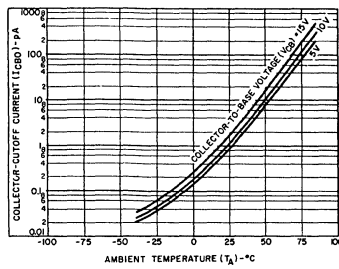


Fig. 7—Collector-cutoff current vs. temperature.

# CA3049, CA3102

## Typical Characteristics for CA3049T and CA3102 (cont'd)

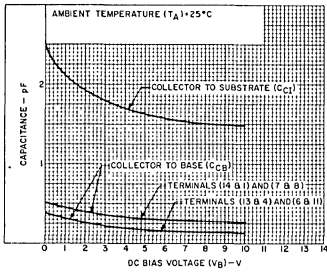


Fig. 8—Capacitance vs. dc bias voltage.

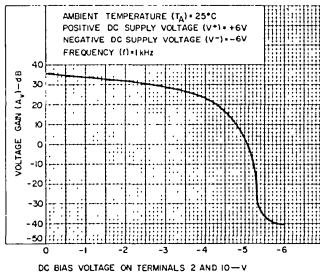


Fig. 9—Voltage gain vs. dc bias voltage.

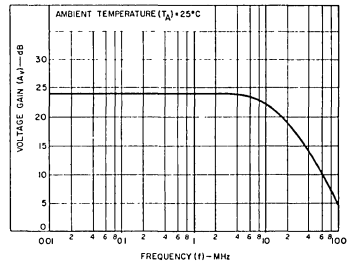


Fig. 10—Voltage gain vs. frequency.

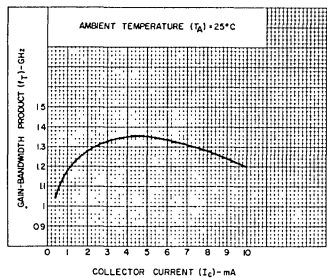


Fig. 11—Gain-bandwidth product vs. collector current.

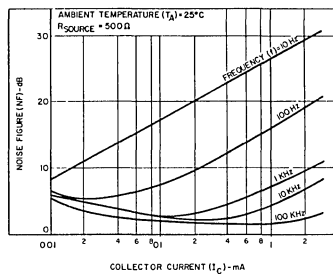


Fig. 12—1/f noise figure vs. collector current.

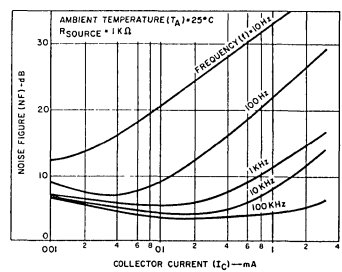


Fig. 13—1/f noise figure vs. collector current.

## Typical Input Admittance Characteristics for CA3049T and CA3102

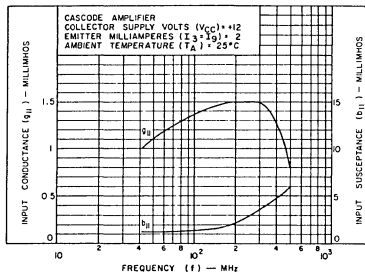


Fig. 14—Input admittance ( $Y_{11}$ ) vs. frequency.

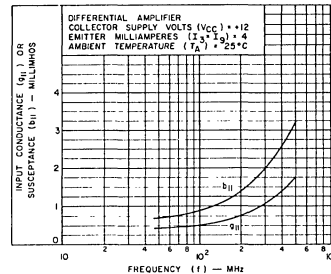


Fig. 15—Input admittance ( $Y_{11}$ ) vs. frequency.

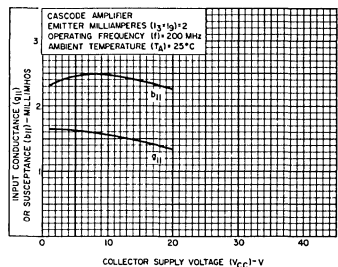


Fig. 16—Input admittance ( $Y_{11}$ ) vs. collector supply voltage.

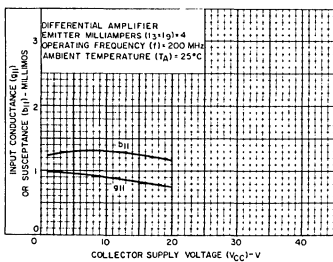


Fig. 17—Input admittance ( $Y_{11}$ ) vs. collector supply voltage.

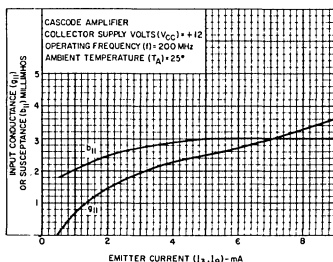


Fig. 18—Input admittance ( $Y_{11}$ ) vs. emitter current.

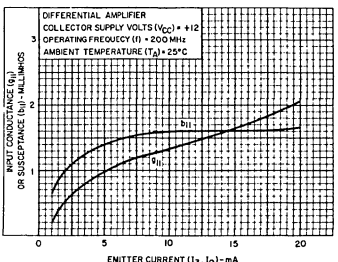


Fig. 19—Input admittance ( $Y_{11}$ ) vs. emitter current.

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DIFFERENTIAL AMPLIFIERS

# CA3049, CA3102

## Typical Output Admittance Characteristics for CA3049T and CA3102

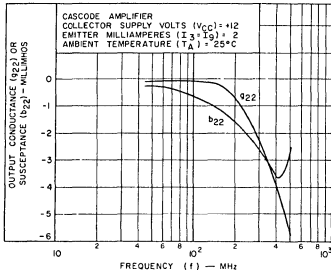


Fig. 20—Output admittance ( $Y_{22}$ ) vs. frequency.

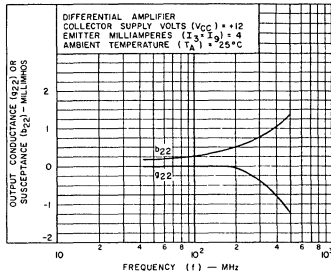


Fig. 21—Output admittance ( $Y_{22}$ ) vs. frequency.

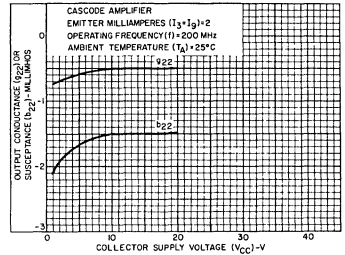


Fig. 22—Output admittance ( $Y_{22}$ ) vs. collector supply voltage.

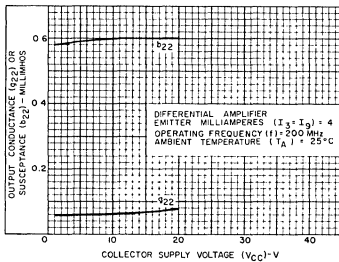


Fig. 23—Output admittance ( $Y_{22}$ ) vs. collector supply voltage.

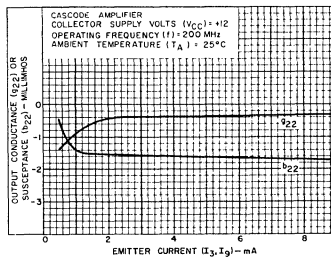


Fig. 24—Output admittance ( $Y_{22}$ ) vs. emitter current.

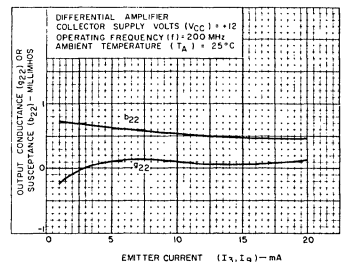


Fig. 25—Output admittance ( $Y_{22}$ ) vs. emitter current.

## Typical Forward Transfer Characteristics for CA3049T and CA3102

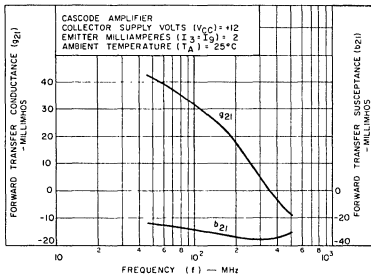


Fig. 26—Forward transfer admittance ( $Y_{21}$ ) vs. frequency.

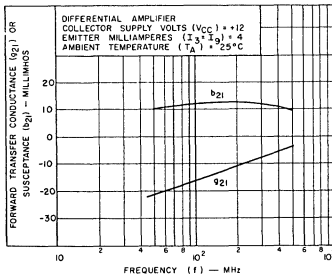


Fig. 27—Forward transfer admittance ( $Y_{21}$ ) vs. frequency.

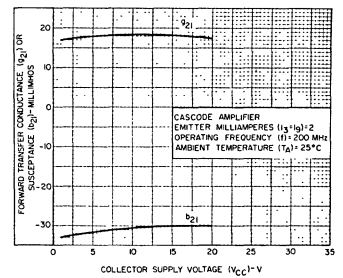


Fig. 28—Forward transfer admittance ( $Y_{21}$ ) vs. collector supply voltage.

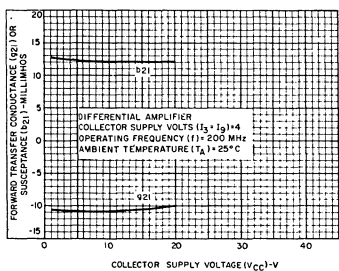


Fig. 29—Forward transfer admittance ( $Y_{21}$ ) vs. collector supply voltage.

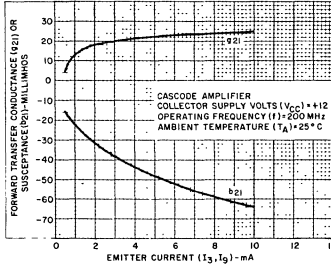


Fig. 30—Forward transfer admittance ( $Y_{21}$ ) vs. emitter current.

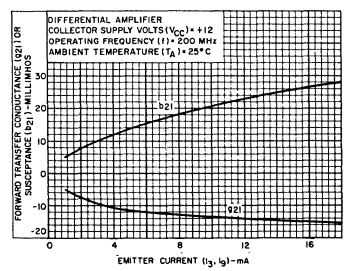


Fig. 31—Forward transfer admittance ( $Y_{21}$ ) vs. emitter current.

## Transistor Array - Dual Independent Differential Amplifier For Low Power Applications from DC to 120MHz

August 1991

### Features

- Two Differential Amplifiers on a Common Substrate
- Independently Accessible Inputs and Outputs
- Maximum Input Offset Voltage .....  $\pm 5\text{mV}$
- Temperature Range .....  $0^\circ\text{C}$  to  $+85^\circ\text{C}$

### Applications

- Dual Sense Amplifiers
- Dual Schmitt Triggers
- Multifunction Combinations - RF/Mixer/Oscillator; Converter/IF
- IF Amplifiers (Differential and/or Cascode)
- Product Detectors
- Doubly Balanced Modulators and Demodulators
- Balanced Quadrature Detectors
- Cascade Limiters
- Synchronous Detectors
- Pairs of Balanced Mixers
- Synthesizer Mixers
- Balanced (Push-Pull) Cascode Amplifiers

### Description

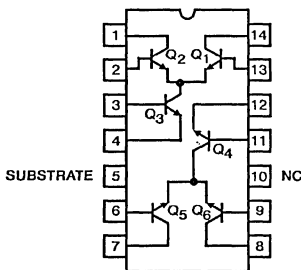
The CA3054 consists of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six n-p-n transistors which comprise the amplifiers are general-purpose devices which exhibit low  $1/f$  noise and a value of  $f_T$  in excess of 300MHz. These features make the CA3054 useful from DC to 120MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3054 provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual-channel applications where matched performance of the two channels is required.

The CA3054 is supplied in a 14-lead plastic dual-in-line package and a 14-lead small outline package (M suffix) with a limited temperature range. The availability of extra terminals allows the introduction of an independent substrate connection for maximum flexibility.

### Pinout

CA3054, CA3054M  
TOP VIEW



### Schematic Diagram

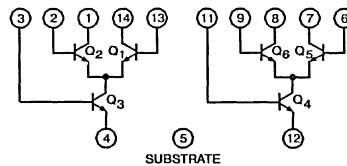


FIGURE 1.

**CAUTION:** Substrate MUST be maintained negative with respect to all collector terminals of this device. See Maximum Voltage Ratings chart.

# CA3054

## MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES, AT $T_A = 25^\circ\text{C}$

|                                    |               |                      |  |
|------------------------------------|---------------|----------------------|--|
| <b>POWER DISSIPATION, P:</b>       | <b>CA3054</b> |                      | The following ratings apply for each transistor in the device: |
| Any one transistor .....           | 300           | mW                   | COLLECTOR-TO-EMITTER VOLTAGE, $V_{CE0}$ ...                    |
| Total package .....                | 750           | mW                   | COLLECTOR-TO-BASE VOLTAGE, $V_{CB0}$ .....                     |
| For $T_A > 55^\circ\text{C}$ ..... | 6.67          | mW/ $^\circ\text{C}$ | COLLECTOR-TO-SUBSTRATE VOLTAGE, $V_{C10}^*$ .....              |
| <b>TEMPERATURE RANGE:</b>          |               |                      | EMITTER-TO-BASE VOLTAGE, $V_{EB0}$ .....                       |
| Operating .....                    | 0 to +85      | $^\circ\text{C}$     | COLLECTOR CURRENT, $I_C$ .....                                 |
| Storage .....                      | -65 to +150   | $^\circ\text{C}$     |  |

### LEAD TEMPERATURE (During Soldering)

At distance  $1/16 \pm 1/32$  inch ( $1.59 \pm 0.79$  mm) from case for 10 seconds max. .... +265 $^\circ\text{C}$

\*The collector of each transistor of the CA3054 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide for normal transistor action. The substrate should be maintained at signal (AC) ground by means of a suitable grounding capacitor, to avoid undesired coupling between transistors.

### Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 4 is +15 to -5 volts.

| CA3054 →<br>Terminal No.<br>↓ | 13 | 14       | 1      | 2        | 3      | 4         | 6        | 7      | 8        | 9      | 11        | 12        | 5                     |
|-------------------------------|----|----------|--------|----------|--------|-----------|----------|--------|----------|--------|-----------|-----------|-----------------------|
| 13                            |    | 0<br>-20 | *<br>* | +5<br>-5 | *<br>* | +15<br>-5 | *<br>*   | *<br>* | *<br>*   | *<br>* | *<br>*    | *<br>*    | *<br>*                |
| 14                            |    |          | *<br>* | *<br>*   | *<br>* | +20<br>0  | *<br>*   | *<br>* | *<br>*   | *<br>* | *<br>*    | *<br>*    | +20<br>0              |
| 1                             |    |          |        | +20<br>0 | *<br>* | +20<br>0  | *<br>*   | *<br>* | *<br>*   | *<br>* | *<br>*    | *<br>*    | +20<br>0              |
| 2                             |    |          |        |          | *<br>* | +15<br>-5 | *<br>*   | *<br>* | *<br>*   | *<br>* | *<br>*    | *<br>*    | *<br>*                |
| 3                             |    |          |        |          |        | +1<br>-5  | *<br>*   | *<br>* | *<br>*   | *<br>* | *<br>*    | *<br>*    | *<br>*                |
| 4                             |    |          |        |          |        |           | *<br>*   | *<br>* | *<br>*   | *<br>* | *<br>*    | *<br>*    | *<br>*                |
| 6                             |    |          |        |          |        |           | 0<br>-20 | *<br>* | +5<br>-5 | *<br>* | +15<br>-5 | *<br>*    | *<br>*                |
| 7                             |    |          |        |          |        |           |          | *<br>* | *<br>*   | *<br>* | *<br>*    | *<br>*    | +20<br>0              |
| 8                             |    |          |        |          |        |           |          |        | +20<br>0 | *<br>* | *<br>*    | +20<br>0  | *<br>*                |
| 9                             |    |          |        |          |        |           |          |        |          |        | *<br>*    | +15<br>-5 | *<br>*                |
| 11                            |    |          |        |          |        |           |          |        |          |        |           | -1<br>-5  | *<br>*                |
| 12                            |    |          |        |          |        |           |          |        |          |        |           |           | *<br>*                |
| 5                             |    |          |        |          |        |           |          |        |          |        |           |           | Ref<br>Sub-<br>strate |

\*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

### Maximum Current Ratings

| CA3054<br>Terminal<br>No.* | $I_{IN}$<br>mA | $I_{OUT}$<br>mA |
|----------------------------|----------------|-----------------|
| 13                         | 5              | 0.1             |
| 14                         | 50             | 0.1             |
| 1                          | 50             | 0.1             |
| 2                          | 5              | 0.1             |
| 3                          | 5              | 0.1             |
| 4                          | 0.1            | 50              |
| 6                          | 5              | 0.1             |
| 7                          | 50             | 0.1             |
| 8                          | 50             | 0.1             |
| 9                          | 5              | 0.1             |
| 11                         | 5              | 0.1             |
| 12                         | 0.1            | 50              |

\* Terminal No. 10 of CA3054 is not used.

CA3054

ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$

| CHARACTERISTICS   | SYMBOLS   | TEST CONDITIONS  | TEST CIRCUIT |      | CA3054 LIMITS                    |                                  |                              | UNITS | TYPICAL CHARAC-<br>TERISTICS<br>CURVES |
|---|---|--|--------------|------|----------------------------------|----------------------------------|------------------------------|-------|--|
|   |   |  | FIG.         | MIN. | TYP.                             | MAX.                             | FIG.                         |       |  |
| STATIC CHARACTERISTICS  |   |  |              |      |                                  |                                  |                              |       |  |
| For Each Differential Amplifier   |   |  |              |      |                                  |                                  |                              |       |  |
| Input Offset Voltage  | $V_{IO}$  | $V_{CB} = 3\text{ V}$<br>$I_{E(Q3)} = I_{E(Q4)} = 2\text{ mA}$   | -            | -    | 0.45                             | 5                                | mV                           | 6     |  |
| Input Offset Current  | $I_{IO}$  |  | -            | -    | 0.3                              | 2                                | $\mu\text{A}$                | 7     |  |
| Input Bias Current  | $I_I$   |  | -            | -    | 10                               | 24                               | $\mu\text{A}$                | 3     |  |
| Quiescent Operating Current Ratio   | $\frac{I_{C(Q1)} \text{ or } I_{C(Q5)}}{I_{C(Q2)} \text{ or } I_{C(Q6)}}$ |  | -            | -    | 0.98 to 1.02                     | -                                | -                            | 3     |  |
| Temperature Coefficient Magnitude of Input-Offset Voltage                               | $\frac{ \Delta V_{IO} }{\Delta T}$  |  | -            | -    | 1.1                              | -                                | $\mu\text{V}/^\circ\text{C}$ | 5     |  |
| For Each Transistor   |   |  |              |      |                                  |                                  |                              |       |  |
| DC Forward Base-to-Emitter Voltage  | $V_{BE}$  | $V_{CB} = 3\text{ V}$ $\left\{ \begin{array}{l} I_C = 50\text{ }\mu\text{A} \\ 1\text{ mA} \\ 3\text{ mA} \\ 10\text{ mA} \end{array} \right.$ | -            | -    | 0.630<br>0.715<br>0.750<br>0.800 | 0.700<br>0.800<br>0.850<br>0.900 | V                            | 6     |  |
| Temperature Coefficient of Base-to-Emitter Voltage                                      | $\frac{\Delta V_{BE}}{\Delta T}$  | $V_{CB} = 3\text{ V}, I_C = 1\text{ mA}$   | -            | -    | -1.9                             | -                                | $\mu\text{V}/^\circ\text{C}$ | 4     |  |
| Collector-Cutoff Current  | $I_{CBO}$   | $V_{CB} = 10\text{ V}, I_E = 0$  | -            | -    | 0.002                            | 100                              | nA                           | 2     |  |
| Collector-to-Emitter Breakdown Voltage  | $V_{(BR)CEO}$   | $I_C = 1\text{ mA}, I_B = 0$   | -            | 15   | 24                               | -                                | V                            | -     |  |
| Collector-to-Base Breakdown Voltage   | $V_{(BR)CBO}$   | $I_C = 10\text{ }\mu\text{A}, I_E = 0$   | -            | 20   | 60                               | -                                | V                            | -     |  |
| Collector-to-Substrate Breakdown Voltage  | $V_{(BR)C10}$   | $I_C = 10\text{ }\mu\text{A}, I_{C1} = 0$  | -            | 20   | 60                               | -                                | V                            | -     |  |
| Emitter-to-Base Breakdown Voltage   | $V_{(BR)EBO}$   | $I_E = 10\text{ }\mu\text{A}, I_C = 0$   | -            | 5    | 7                                | -                                | V                            | -     |  |
| DYNAMIC CHARACTERISTICS   |   |  |              |      |                                  |                                  |                              |       |  |
| Common-Mode Rejection Ratio For Each Amplifier  | CMR   | $V_{CC} = 12\text{ V}$<br>$V_{EE} = -6\text{ V}$<br>$V_x = -3.3\text{ V}$<br>$f = 1\text{ kHz}$  | 8a           | -    | 100                              | -                                | dB                           | 8b    |  |
| AGC Range, One Stage  | AGC   |  | 9a           | -    | 75                               | -                                | dB                           | 9b    |  |
| Voltage Gain, Single Stage Double-Ended Output  | A   |  | 9a           | -    | 32                               | -                                | dB                           | 9b    |  |
| AGC Range, Two Stage  | AGC   |  | 10a          | -    | 105                              | -                                | dB                           | 10b   |  |
| Voltage Gain, Two Stage Double-Ended Output   | A   |  | 10a          | -    | 60                               | -                                | dB                           | 10b   |  |
| Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: (For Single Transistor) |   |  |              |      |                                  |                                  |                              |       |  |
| Forward Current-Transfer Ratio  | $h_{fe}$  | $f = 1\text{ kHz}, V_{CE} = 3\text{ V}, I_C = 1\text{ mA}$   | -            | -    | 110                              | -                                | -                            | 11    |  |
| Short-Circuit Input Impedance   | $h_{ie}$  |  | -            | -    | 3.5                              | -                                | $\text{k}\Omega$             | 11    |  |
| Open-Circuit Output Impedance   | $h_{oe}$  |  | -            | -    | 15.6                             | -                                | $\mu\text{mho}$              | 11    |  |
| Open-Circuit Reverse Voltage-Transfer Ratio   | $h_{re}$  |  | -            | -    | $1.8 \times 10^{-4}$             | -                                | -                            | 11    |  |

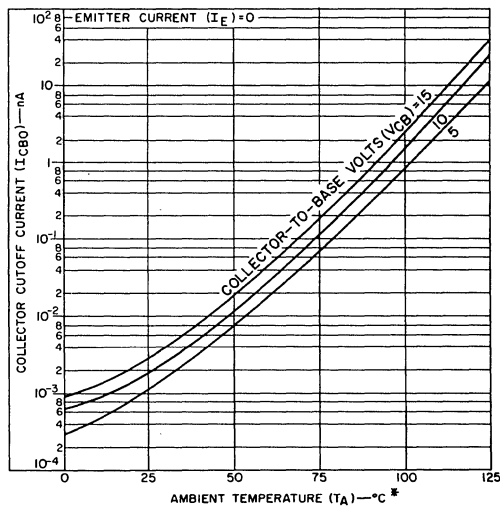
6  
DIFFERENTIAL AMPLIFIERS



# CA3054

| DYNAMIC CHARACTERISTICS CONT'D.  |          |  |   |   |                  |   |                 |     |
|--|----------|--|---|---|------------------|---|-----------------|-----|
| 1/f Noise Figure<br>(For Single Transistor)  | NF       | $f = 1 \text{ kHz}, V_{CE} = 3 \text{ V}$  | - | - | 3.25             | - | dB              | -   |
| Gain-Bandwidth Product<br>(For Single Transistor)  | $f_T$    | $V_{CE} = 3 \text{ V}, I_C = 3 \text{ mA}$   | - | - | 550              | - | MHz             | 12  |
| Admittance Characteristics;<br>Differential Circuit Configuration:<br>(For Each Amplifier) |          |  |   |   |                  |   |                 |     |
| Forward Transfer Admittance  | $y_{21}$ | $V_{CB} = 3 \text{ V}$<br>Each Collector<br>$I_C \approx 1.25 \text{ mA}$<br>$f = 1 \text{ MHz}$ | - | - | $-20 + j0$       | - | mmho            | 13a |
| Input Admittance   | $y_{11}$ |  | - | - | $0.22 + j0.1$    | - | mmho            | 13b |
| Output Admittance  | $y_{22}$ |  | - | - | $0.01 + j0$      | - | mmho            | 13c |
| Reverse Transfer Admittance  | $y_{12}$ |  | - | - | $-0.003 + j0$    | - | mmho            | 13d |
| Admittance Characteristics;<br>Cascode Circuit Configuration:<br>(For Each Amplifier)      |          |  |   |   |                  |   |                 |     |
| Forward Transfer Admittance  | $y_{21}$ | $V_{CB} = 3 \text{ V}$<br>Total Stage<br>$I_C \approx 2.5 \text{ mA}$<br>$f = 1 \text{ MHz}$     | - | - | $68 - j0$        | - | mmho            | 14a |
| Input Admittance   | $y_{11}$ |  | - | - | $0.55 + j0$      | - | mmho            | 14b |
| Output Admittance  | $y_{22}$ |  | - | - | $0 + j0.02$      | - | mmho            | 14c |
| Reverse Transfer Admittance  | $y_{12}$ |  | - | - | $0.004 - j0.005$ | - | $\mu\text{mho}$ | 14d |
| Noise Figure   | NF       | $f = 100 \text{ MHz}$  | - | - | 8                | - | dB              | -   |

## TYPICAL STATIC CHARACTERISTICS



\* For CA3054: use data from 0°C to 85°C only

Fig.2 - Collector-to-base cutoff current vs ambient temperature for each transistor.

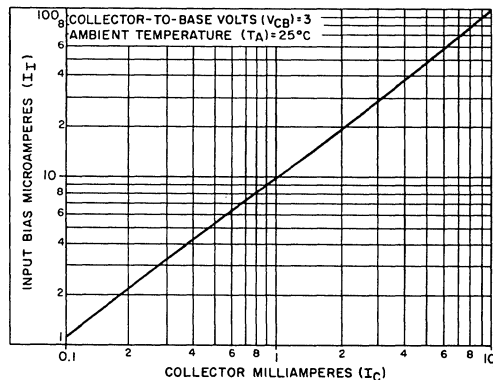


Fig.3 - Input bias current characteristic vs collector current for each transistor.

TYPICAL STATIC CHARACTERISTICS

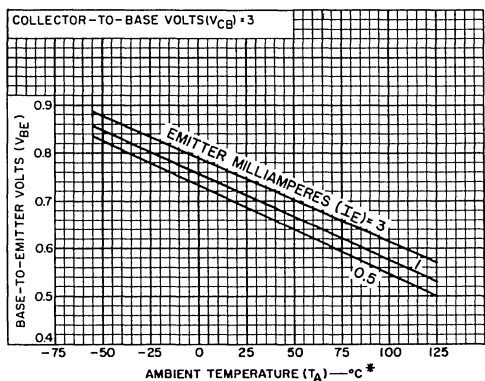


Fig.4 - Base-to-emitter voltage characteristic for each transistor vs ambient temperature.

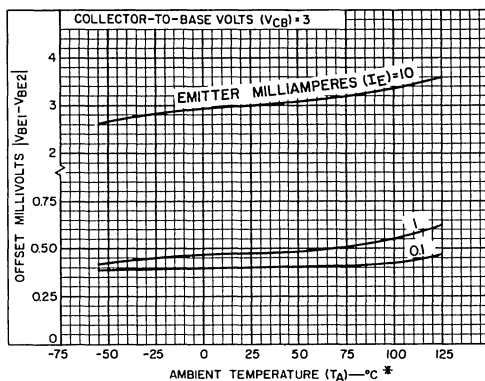


Fig.5 - Offset voltage characteristic vs ambient temperature for differential pairs.

\* For CA3054: use data from 0°C to 85°C only

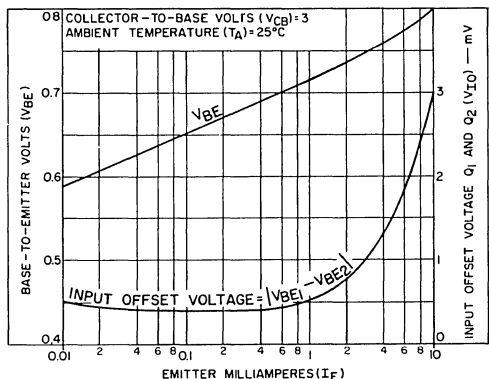


Fig.6 - Static base-to-emitter voltage characteristic and input offset voltage for differential pairs vs emitter current.

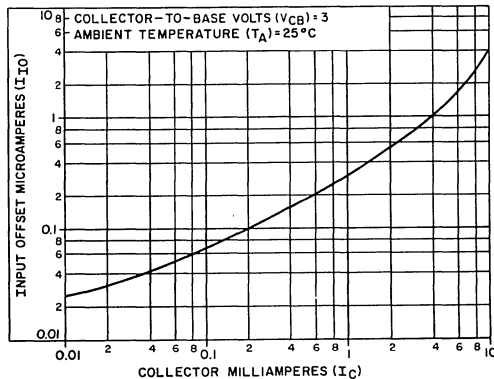


Fig.7 - Input offset current for matched differential pairs vs collector current.

TYPICAL DYNAMIC CHARACTERISTICS

COMMON MODE REJECTION RATIO

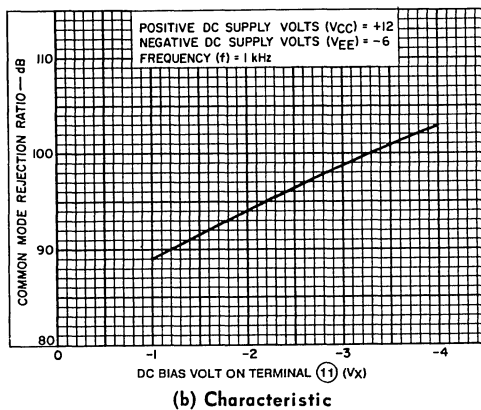
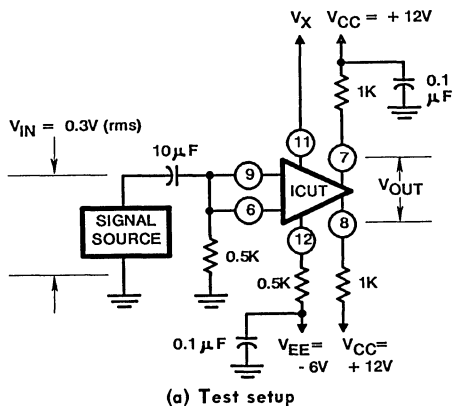
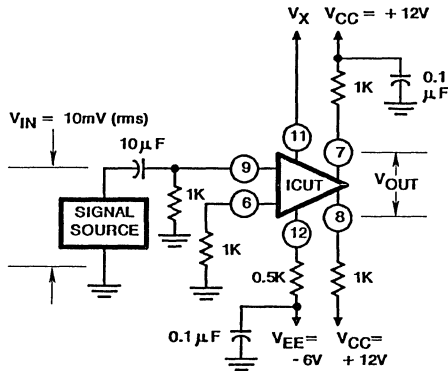


Fig.8

TYPICAL DYNAMIC CHARACTERISTICS (cont'd)  
SINGLE-STAGE VOLTAGE GAIN



(a) Test setup

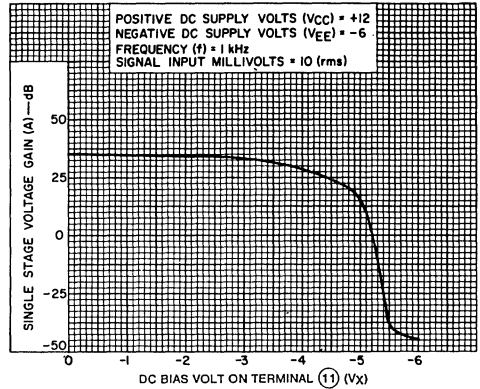
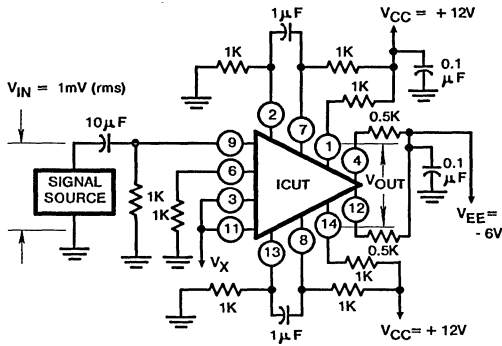


Fig.9

(b) Characteristic

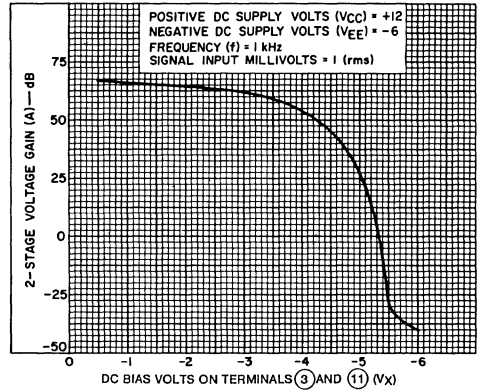
TWO-STAGE VOLTAGE GAIN



(a) Test setup

Fig.10

(b) Characteristic



TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

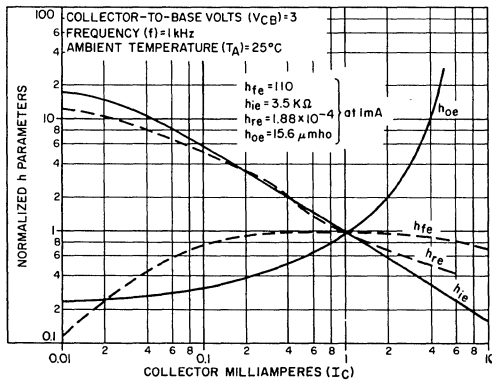


Fig.11 - Forward current-transfer ratio ( $h_{fe}$ ), short-circuit input impedance ( $h_{ie}$ ), open-circuit output impedance ( $h_{oe}$ ), and open-circuit reverse voltage-transfer ratio ( $h_{re}$ ) vs collector current for each transistor.

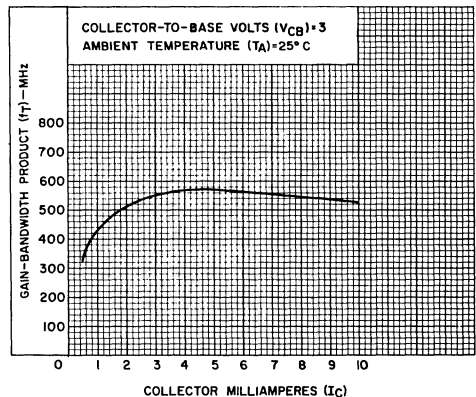


Fig.12 - Gain-bandwidth product ( $f_T$ ) vs collector current.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER

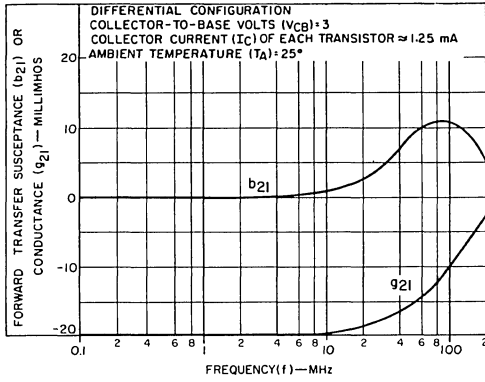


Fig.13(a) - Forward transfer admittance ( $Y_{21}$ ) vs frequency.

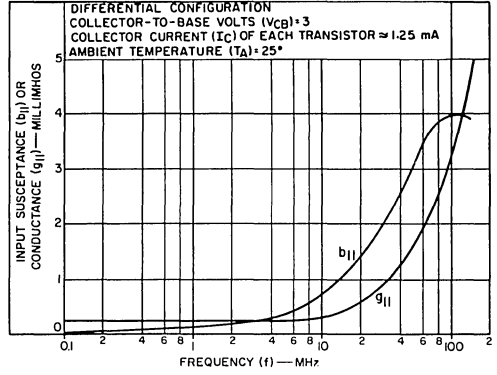


Fig.13(b) - Input admittance ( $Y_{11}$ ).

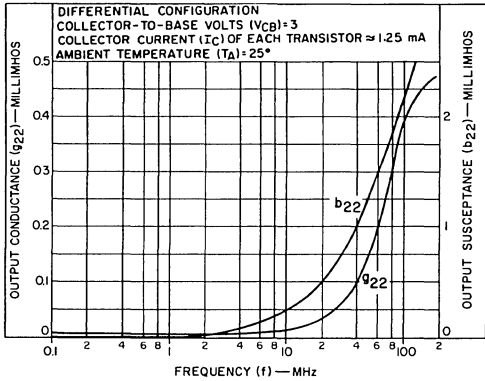


Fig.13(c) - Output admittance ( $Y_{22}$ ) vs frequency.

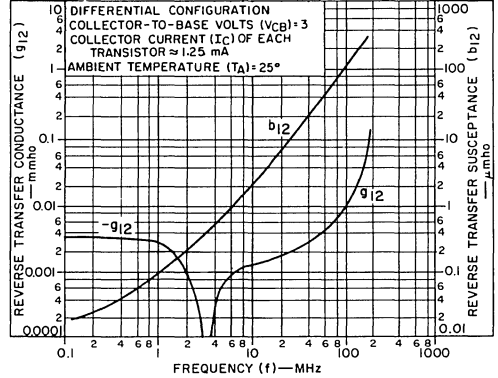


Fig.13(d) - Reverse transfer admittance ( $Y_{12}$ ) vs frequency.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH CASCODE AMPLIFIER

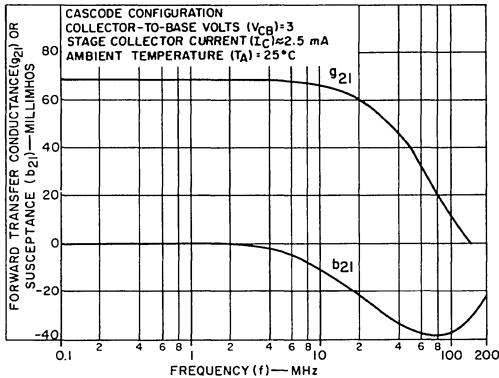


Fig.14(a) - Forward transfer admittance ( $Y_{21}$ ) vs frequency.

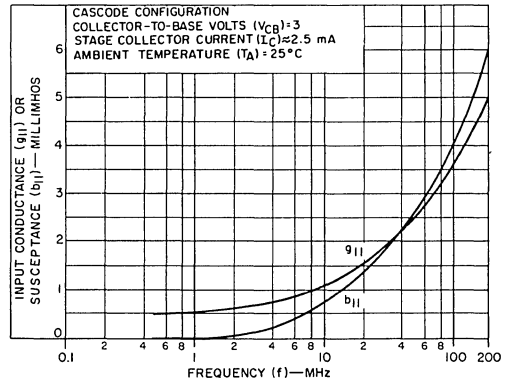


Fig.14(b) - Input admittance ( $Y_{11}$ ) vs frequency.

# CA3054

## TYPICAL CHARACTERISTICS FOR EACH CASCODE AMPLIFIER (cont'd)

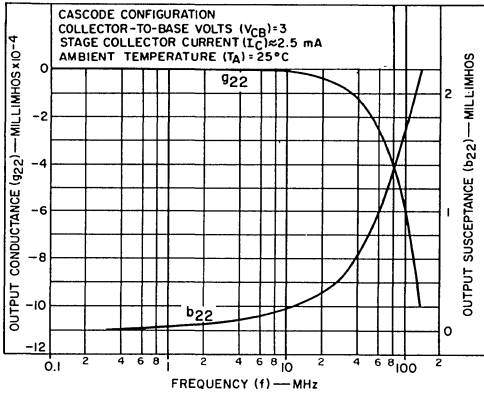


Fig.14(c) - Output admittance ( $Y_{22}$ ) vs frequency.

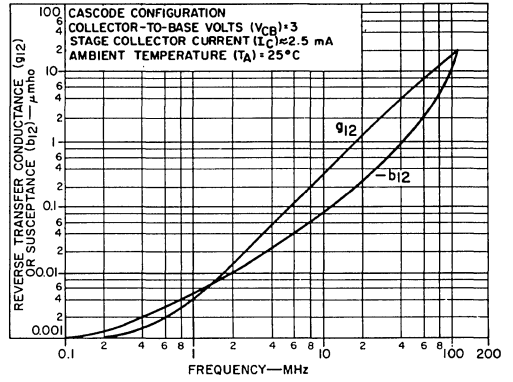


Fig.14(d) - Reverse transfer admittance ( $Y_{12}$ ) vs frequency.

## ARRAYS

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# Selection Guide

## TRANSISTOR ARRAYS

Electrical Characteristics at  $T_A = 25^\circ\text{C}$

| Type    | Description  | $V_{(BR)}^{CEO}$<br>(Min.) V  | $V_{(BR)}^{CBO}$<br>(Min.) V | $h_{FE}$<br>(Min.) | $I_C$<br>(Max.)<br>mA | Pin Count<br>& Package<br>Type* |
|---------|--|---|------------------------------|--------------------|-----------------------|---------------------------------|
| CA3018  | Two Isolated Transistors plus a Darlington Pair        | 15  | 20                           | 30                 | 50                    | 12T                             |
| CA3018A |  | 15  | 30                           | 60                 | 50                    |                                 |
|         |  | $h_{FE}$ matched $\pm 10\%$ . $V_{BE}$ matched $\pm 2\text{mV}$ and $\pm 5\text{mV}$ max.<br>Operation from DC to 120MHz. |                              |                    |                       |                                 |
| CA3045  | Three Transistors plus a Differential Pair             | 15  | 20                           | 40                 | 50                    | 14D, 14F                        |
| CA3046  |  | 15  | 20                           | 40                 | 50                    | 14E, 14M                        |
|         |  | $f_T > 300\text{MHz}$ . 2 matched pairs $\pm 5\text{mV}$  |                              |                    |                       |                                 |
| CA3081  | General-Purpose n-p-n High-Current Transistors         | 16  | 20                           | 40                 | 100                   | 16E, 16F,<br>16M                |
|         |  | Seven Common-Emitter  |                              |                    |                       |                                 |
| CA3082  |  | 16  | 20                           | 40                 | 100                   | 16E, 16F<br>16M                 |
|         |  | Seven Common-Collector  |                              |                    |                       |                                 |
| CA3083  | 15   | 20  | 40                           | 100                | 16E, 16F,<br>16M      |                                 |
|         |  | Five independent transistors.<br>$Q_1$ and $Q_2$ matched: $I_{O}$ (at 1mA) 2.5 $\mu\text{A}$ maximum.                     |                              |                    |                       |                                 |
| CA3086  | Three Isolated Transistors plus a Differential Pair    | 15  | 20                           | 40                 | 50                    | 14E, 14F,<br>14M                |
|         |  | $f_T > 550\text{MHz}$ typ. Operation from DC to 120MHz  |                              |                    |                       |                                 |
| CA3127  | Five Independent Transistors                           | 15  | 20                           | 40                 | 20                    | 16E, 16F,<br>16M                |
|         |  | $f_T > 1\text{GHz}$ . Operation from DC to 500MHz.  |                              |                    |                       |                                 |
| CA3146  | Three Transistors plus a Differential Pair             | 30  | 40                           | 30                 | 50                    | 14E, 14M                        |
| CA3146A |  | 40  | 50                           | 30                 | 50                    |                                 |
|         |  | $f_T > 500\text{MHz}$ typ. Operation from DC to 120MHz.   |                              |                    |                       |                                 |
| CA3183  | Five High-Current Transistors                          | 30  | 40                           | 40                 | 75                    | 16E, 16M                        |
| CA3183A |  | 40  | 50                           | 40                 | 75                    |                                 |
|         |  | High-voltage versions of CA3083 Transistors<br>$Q_1$ and $Q_2$ matched at 1mA.  |                              |                    |                       |                                 |
| CA3227  | Five Independent Transistors                           | 8   | 12                           | 40                 | 20                    | 16E, 16M                        |
|         |  | $f_T = 3\text{GHz}$ typ. Operation from DC to 1.5GHz.   |                              |                    |                       |                                 |
| CA3246  | Three Independent Transistors plus a Differential Pair | 8   | 12                           | 40                 | 20                    | 14E, 14M                        |
|         |  | $f_T = 3\text{GHz}$ typ. Operation from DC to 1.5GHz.   |                              |                    |                       |                                 |

\* See Packaging and Ordering Information in Section 12.

# Selection Guide

## TRANSISTOR ARRAYS (Continued)

Electrical Characteristics at  $T_A = 25^\circ\text{C}$

| Type    | Description                                    | $V_{(BR)CEO}$<br>(Min.) V<br>n-p-n/p-n-p | $V_{(BR)CBO}$<br>(Min.) V<br>n-p-n/p-n-p | $h_{FE}$<br>(Min.)<br>n-p-n/p-n-p | $I_C$<br>(Max.)<br>n-p-n/p-n-p | Pin Count<br>and<br>Package<br>Type* |
|---------|--|--|--|-----------------------------------|--------------------------------|--------------------------------------|
| CA3096  | Five Independent Transistors, 3 n-p-n, 2 p-n-p | 35/-40                                   | 45/-40                                   | 150/20                            | 50/-10                         | 16E, 16M                             |
| CA3096A |  | 35/-40                                   | 45/-40                                   | 150/20                            | 50/-10                         |                                      |
| CA3096C |  | 24/-24                                   | 30/-24                                   | 100/15                            | 50/-10                         |                                      |
|         |  | n-p-n                                    |  | p-n-p                             |                                |                                      |
|         |  | $ V_{IO}  = 5\text{mV max.}$             |  | 5mV max.                          |                                |                                      |
|         |  | $ I_{IO}  = 0.6\ \mu\text{A max.}$       |  | 0.25 $\mu\text{A max.}$           |                                |                                      |

## DIODE ARRAYS

Electrical Characteristics at  $T_A = 25^\circ\text{C}$ . Apply for each Diode

| Type   | Description   | $V_{(BR)R}$<br>(Min.) V | $I_R$<br>(Max.) $\mu\text{A}$ | $C_D$<br>(Typ.) pF | $V_{F1} - V_{F2}$<br>(Max.) mV | Pin Count<br>& Package<br>Type* |
|--------|---|-------------------------|-------------------------------|--------------------|--------------------------------|---------------------------------|
| CA3039 | 6 Individual  | 5                       | 0.1                           | 0.65               | 5 ( $I_F = 1\ \text{mA}$ )     | 12T, 14M                        |
|        | • Ultra-fast low-capacitance matched diodes               |                         |                               |                    |                                |                                 |
| CA3141 | 10 High Reverse Breakdown Voltage Diodes $\square\square$ | 30                      | 0.1                           | 0.3                | 0.55 (typ.<br>ea. diode pr.)   | 16E                             |
|        | • Low-noise performance<br>• Low-leakage current          |                         |                               |                    |                                |                                 |

$\square\square$  Six connected to form 3 common-cathode diode pairs.  
Four connected to form 2 common-anode diode pairs.

\* See Packaging and Ordering Information in Section 12.





August 1991

## General-Purpose Transistor Arrays Range

### Features

- Matched Monolithic General Purpose Transistors
- $H_{FE}$  Matched .....  $\pm 10\%$
- $V_{BE}$  Matched CA3018A .....  $\pm 2mV$   
CA3018 .....  $\pm 5mV$
- Operation From DC to 120MHz
- Wide Operating Current Range
- CA3018A Performance Characteristics Controlled from  $10\mu A$  to 10mA
- Low Noise Figure ..... 3.2dB Typical at 1KHz
- Full Military Temperature Range...  $-55^{\circ}C$  to  $+125^{\circ}C$

### Applications

- Two Isolated Transistors and a Darlington-Connected Transistor Pair for Low-Power Applications at Frequencies from DC Through the VHF Range
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers
- See Application Note, ICAN-5296 "Application of the CA3018 Integrated-Circuit Transistor Array" for Suggested Applications

### Description

The CA3018 and CA3018A consist of four general purpose silicon n-p-n transistors on a common monolithic substrate.

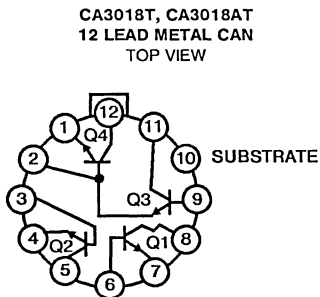
Two of the four transistors are connected in the Darlington configuration. The substrate is connected to a separate terminal for maximum flexibility.

The transistors of the CA3018 and the CA3018A are well suited to a wide variety of applications in low-power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits but in addition they provide the advantages of close electrical and thermal matching inherent in integrated circuit construction.

The CA3018A is similar to the CA3018 but features tighter control of current gain, leakage, and offset parameters making it suitable for more critical applications requiring premium performance.

Both devices are supplied in a 12-lead TO-5 style can package (T suffix).

### Pinout



### Schematic

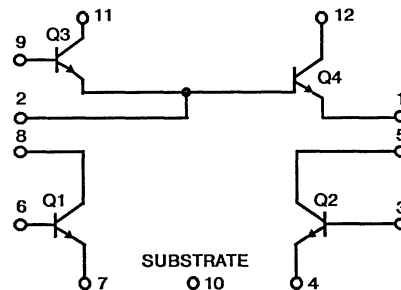


FIGURE 1. SCHEMATIC FOR CA3018 AND CA3018A

# CA3018, CA3018A

## Maximum Ratings, Absolute-Maximum Values, at TA=25°C

|                                 | CA3018      | CA3018A     |    |
|---------------------------------|-------------|-------------|----|
| Power Dissipation, P:           |             |             |    |
| Any one transistor . . . . .    | 300         | 300         | mW |
| Total package . . . . .         | 450         | 450         | mW |
| Derate at 5 mW/°C for TA > 85°C |             |             |    |
| Temperature Range:              |             |             |    |
| Operating . . . . .             | -55 to +125 | -55 to +125 | °C |
| Storage . . . . .               | -65 to +150 | -65 to +150 | °C |

The following ratings apply for each transistor in the device:

|  | CA3018 | CA3018A |    |
|--|--------|---------|----|
| Collector-to-Emitter Voltage, V <sub>CEO</sub> . . . . .     | 15     | 15      | V  |
| Collector-to-Base Voltage, V <sub>CBO</sub> . . . . .        | 20     | 30      | V  |
| Collector-to-Substrate Voltage, V <sub>CIO</sub> * . . . . . | 20     | 40      | V  |
| Emitter-to-Base Voltage, V <sub>EBO</sub> . . . . .          | 5      | 5       | V  |
| Collector Current, I <sub>C</sub> . . . . .                  | 50     | 50      | mA |

\*The collector of each transistor of the CA3018 and CA3018A is isolated from the substrate by an integral diode. The substrate (terminal 10) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

### LEAD TEMPERATURE (During Soldering)

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)

from case for 10 seconds max. . . . . +265°C

Characteristics apply for each transistor in the CA3018 and CA3018A as specified.

| ELECTRICAL CHARACTERISTICS at TA = 25°C  | SYMBOLS   | SPECIAL TEST CONDITIONS  | CA3018 LIMITS |                 |      | CA3018A LIMITS |                  |                | Units       | CHARACTERISTICS CURVES |
|--|---|--|---------------|-----------------|------|----------------|------------------|----------------|-------------|------------------------|
|  |   |  | Min.          | Typ.            | Max. | Min.           | Typ.             | Max.           |             |                        |
| STATIC CHARACTERISTICS   |   |  |               |                 |      |                |                  |                |             |                        |
| Collector-Cutoff Current   | I <sub>CBO</sub>                                    | V <sub>CB</sub> =10V, I <sub>E</sub> =0  | -             | 0.002           | 100  | -              | 0.002            | 40             | nA          | 2                      |
| Collector-Cutoff Current   | I <sub>CEO</sub>                                    | V <sub>CE</sub> =10V, I <sub>B</sub> =0  | -             | See Curve       | 5    | -              | See Curve        | 0.5            | μA          | 3                      |
| Collector-Cutoff Current Darlington Pair   | I <sub>CEOD</sub>                                   | V <sub>CE</sub> =10V, I <sub>B</sub> =0  | -             | -               | -    | -              | -                | 5              | μA          | -                      |
| Collector-to-Emitter Breakdown Voltage   | V <sub>(BR)CEO</sub>                                | I <sub>C</sub> =1mA, I <sub>B</sub> =0   | 15            | 24              | -    | 15             | 24               | -              | V           | -                      |
| Collector-to-Base Breakdown Voltage  | V <sub>(BR)CBO</sub>                                | I <sub>C</sub> =10μA, I <sub>E</sub> =0  | 20            | 60              | -    | 30             | 60               | -              | V           | -                      |
| Emitter-to-Base Breakdown Voltage  | V <sub>(BR)EBO</sub>                                | I <sub>E</sub> =10μA, I <sub>C</sub> =0  | 5             | 7               | -    | 5              | 7                | -              | V           | -                      |
| Collector-to-Substrate Breakdown Voltage   | V <sub>(BR)CIO</sub>                                | I <sub>C</sub> =10μA, I <sub>C1</sub> =0   | 20            | 60              | -    | 40             | 60               | -              | V           | -                      |
| Collector-to-Emitter Saturation Voltage  | V <sub>CE(S)</sub>                                  | I <sub>B</sub> =1mA, I <sub>C</sub> =10mA  | -             | 0.23            | -    | -              | 0.23             | 0.5            | V           | -                      |
| Static Forward Current Transfer Ratio (Note 1)   | h <sub>FE</sub>                                     | V <sub>CE</sub> =3V, $\begin{cases} I_C=10mA \\ I_C=1mA \\ I_C=10μA \end{cases}$ | -             | 100<br>30<br>54 | -    | 50<br>60<br>30 | 100<br>100<br>54 | 200            | -<br>-<br>- | 4                      |
| Magnitude of Static Beta Ratio (Isolated Transistors Q <sub>1</sub> and Q <sub>2</sub> )         |   | V <sub>CE</sub> =3V, I <sub>C1</sub> =I <sub>C2</sub> =1mA                       | 0.9           | 0.97            | -    | 0.9            | 0.97             | -              | -           | 4                      |
| Static Forward Current Transfer Ratio Darlington Pair (Q <sub>3</sub> & Q <sub>4</sub> )         | h <sub>FED</sub>                                    | V <sub>CE</sub> =3V, $\begin{cases} I_C=1mA \\ I_C=100μA \end{cases}$            | 1500<br>-     | 5400<br>-       | -    | 2000<br>1000   | 5400<br>2800     | -              | -           | 5                      |
| Base-to-Emitter Voltage  | V <sub>BE</sub>                                     | V <sub>CE</sub> =3V, $\begin{cases} I_E=1mA \\ I_E=10mA \end{cases}$             | -             | 0.715<br>0.800  | -    | 0.600<br>-     | 0.715<br>0.800   | 0.800<br>0.900 | V           | 6                      |
| Input Offset Voltage   | $\begin{Bmatrix} V_{BE1} \\ -V_{BE2} \end{Bmatrix}$ | V <sub>CE</sub> =3V, I <sub>E</sub> =1mA   | -             | 0.48            | 5    | -              | 0.48             | 2              | mV          | 6,8                    |
| Temperature Coefficient: Base-to-Emitter Voltage Q <sub>1</sub> , Q <sub>2</sub>                 | $\frac{\Delta V_{BE}}{\Delta T}$                    | V <sub>CE</sub> =3V, I <sub>E</sub> =1mA   | -             | -1.9            | -    | -              | -1.9             | -              | mV/°C       | 7                      |
| Base (Q <sub>3</sub> )-to-Emitter (Q <sub>4</sub> ) Voltage-Darlington Pair                      | V <sub>BED</sub> (V <sub>9-1</sub> )                | V <sub>CE</sub> =3V, $\begin{cases} I_E=10mA \\ I_E=1mA \end{cases}$             | -             | 1.46<br>1.32    | -    | -              | 1.46<br>1.32     | 1.60<br>1.50   | V           | 9                      |
| Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair-Q <sub>3</sub> , Q <sub>4</sub> | $\frac{\Delta V_{BED}}{\Delta T}$                   | V <sub>CE</sub> =3V, I <sub>E</sub> =1mA   | -             | 4.4             | -    | -              | 4.4              | -              | mV/°C       | 10                     |
| Temperature Coefficient: Magnitude of Input-Offset Voltage                                       | $\frac{ V_{BE1}-V_{BE2} }{\Delta T}$                | V <sub>CE</sub> =6V, V <sub>EE</sub> =-6V, I <sub>C1</sub> =I <sub>C2</sub> =1mA | -             | 10              | -    | -              | 10               | -              | μV/°C       | -                      |

# CA3018, CA3018A

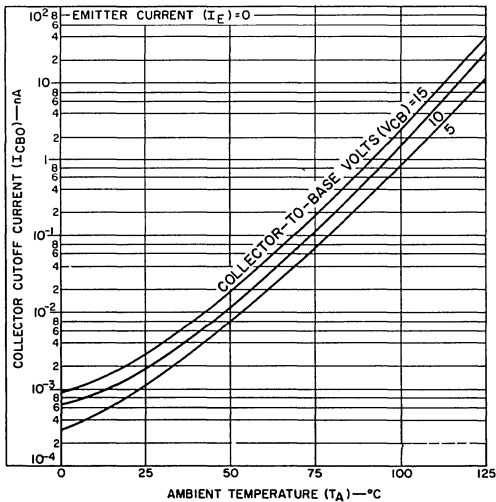
## ELECTRICAL CHARACTERISTICS, (CONT'D)

| DYNAMIC CHARACTERISTICS   |          |  |           |                      |           |     |                      |   |                 |       |
|---|----------|--|-----------|----------------------|-----------|-----|----------------------|---|-----------------|-------|
| Low Frequency Noise Figure                                      | NF       | $f=1\text{ KHz}, V_{CE}=3\text{V}, I_C=100\mu\text{A}$<br>Source resistance=1 K $\Omega$ | -         | 3.25                 | -         | -   | 3.25                 | - | dB              | 11(b) |
| Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: |          |  |           |                      |           |     |                      |   |                 |       |
| Forward Current-Transfer Ratio                                  | $h_{fe}$ | $f=1\text{KHz}, V_{CE}=3\text{V}, I_C=1\text{mA}$  | -         | 110                  | -         | -   | 110                  | - | -               | 12    |
| Short-Circuit Input Impedance                                   | $h_{ie}$ |  | -         | 3.5                  | -         | -   | 3.5                  | - | K $\Omega$      | 12    |
| Open-Circuit Output Impedance                                   | $h_{oe}$ |  | -         | 15.6                 | -         | -   | 15.6                 | - | $\mu\text{mho}$ | 12    |
| Open-Circuit Reverse Voltage-Transfer Ratio                     | $h_{re}$ |  | -         | $1.8 \times 10^{-4}$ | -         | -   | $1.8 \times 10^{-4}$ | - | -               | 12    |
| Admittance Characteristics:                                     |          |  |           |                      |           |     |                      |   |                 |       |
| Forward Transfer Admittance                                     | $Y_{fe}$ | $f=1\text{MHz}, V_{CE}=3\text{V}, I_C=1\text{mA}$  | -         | $31-j1.5$            | -         | -   | $31-j1.5$            | - | mho             | 13    |
| Input Admittance  | $Y_{ie}$ |  | -         | $0.3+j0.04$          | -         | -   | $0.3+j0.04$          | - | mho             | 14    |
| Output Admittance   | $Y_{oe}$ |  | -         | $0.001+j0.03$        | -         | -   | $0.001+j0.03$        | - | mho             | 15    |
| Reverse Transfer Admittance                                     | $Y_{re}$ |  | See Curve |                      | See Curve |     | mho                  |   | 16              |       |
| Gain-Bandwidth Product  | $f_T$    | $V_{CE}=3\text{V}, I_C=3\text{mA}$   | 300       | 500                  | -         | 300 | 500                  | - | MHz             | 17    |
| Emitter-to-Base Capacitance                                     | $C_{EB}$ | $V_{EB}=3\text{V}, I_E=0$  | -         | 0.6                  | -         | -   | 0.6                  | - | pF              | -     |
| Collector-to-Base Capacitance                                   | $C_{CB}$ | $V_{CB}=3\text{V}, I_C=0$  | -         | 0.58                 | -         | -   | 0.58                 | - | pF              | -     |
| Collector-to-Substrate Capacitance                              | $C_{Cl}$ | $V_C=3\text{V}, I_C=0$   | -         | 2.8                  | -         | -   | 2.8                  | - | pF              | -     |

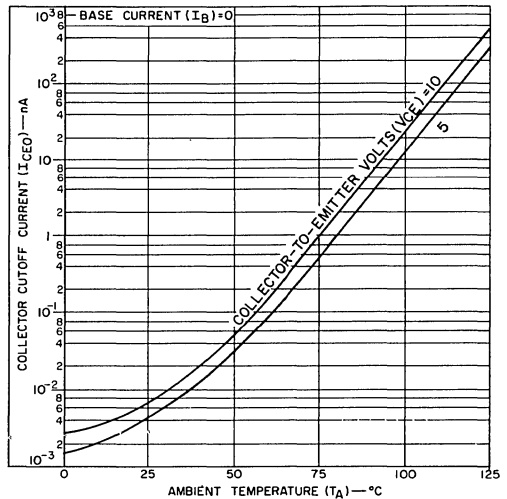
**NOTES:**

- Actual forcing current is via the emitter for this test.

## STATIC CHARACTERISTICS



**Fig.2 - Typical Collector-To-Base Cutoff Current vs Ambient Temperature for Each Transistor.**



**Fig.3 - Typical Collector-To-Emmitter Cutoff Current vs Ambient Temperature for Each Transistor.**

CA3018, CA3018A

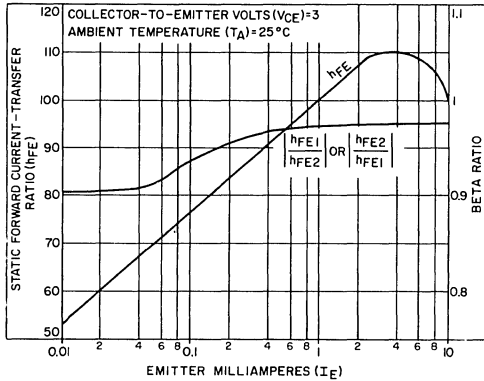


Fig.4 - Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors  $Q_1$  and  $Q_2$  vs Emitter Current.

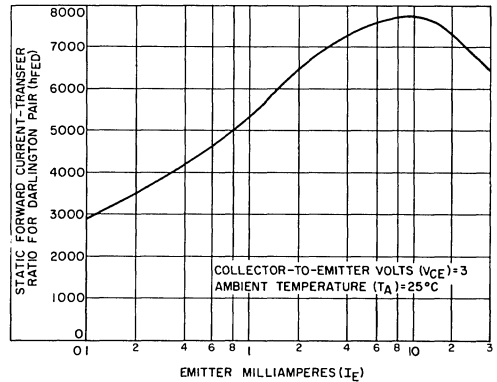


Fig.5 - Typical Static Forward Current - Transfer Ratio for Darlington-connected Transistors  $Q_3$  and  $Q_4$  vs Emitter Current.

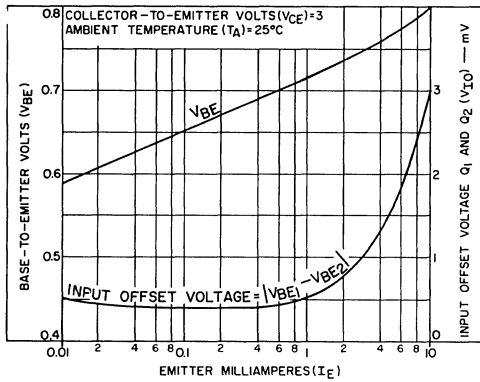


Fig.6 - Typical Static Base-to-Emitter Voltage Characteristic and Input Offset Voltage for  $Q_1$  and  $Q_2$  vs Emitter Current.

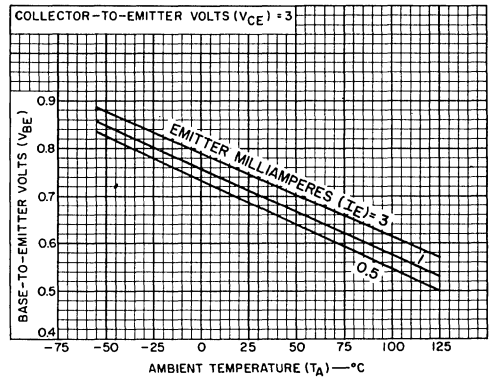


Fig.7 - Typical Base-To-Emitter Voltage Characteristic for Each Transistor vs Ambient Temperature

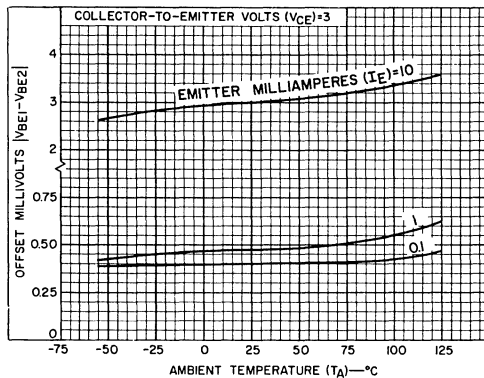


Fig.8 - Typical Offset Voltage Characteristic vs Ambient Temperature

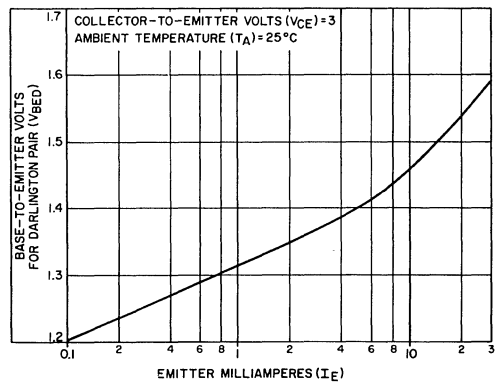


Fig.9 - Typical Static Input Voltage Characteristic for Darlington Pair ( $Q_3$  and  $Q_4$ ) vs Emitter Current

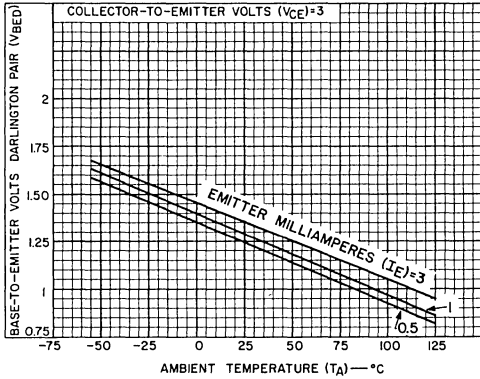


Fig. 10 - Typical Static Input Voltage Characteristic for Darlington Pair ( $Q_3$  and  $Q_4$ ) vs Ambient Temperature.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

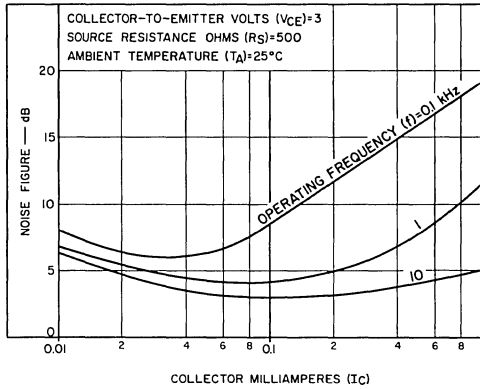


Fig. 11(a) - Noise Figure vs Collector Current,  $R_S = 500 \Omega$ .

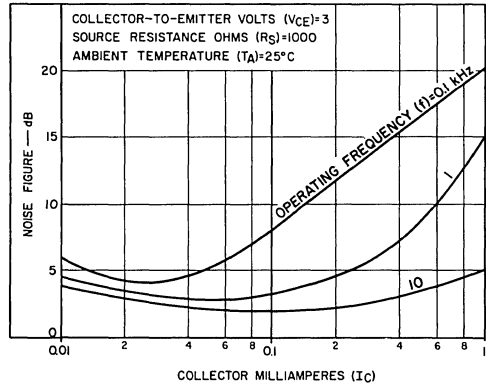


Fig. 11(b) - Noise Figure vs Collector Current,  $R_S = 1 K\Omega$ .

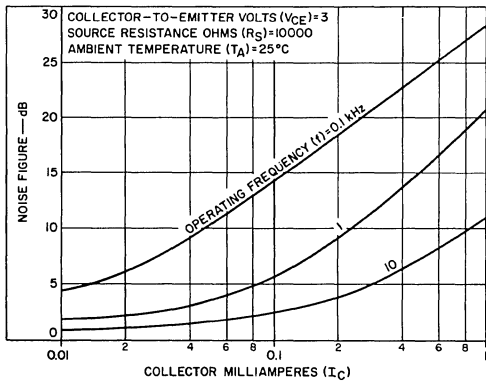


Fig. 11(c) - Noise Figure vs Collector Current,  $R_S = 10 K\Omega$ .

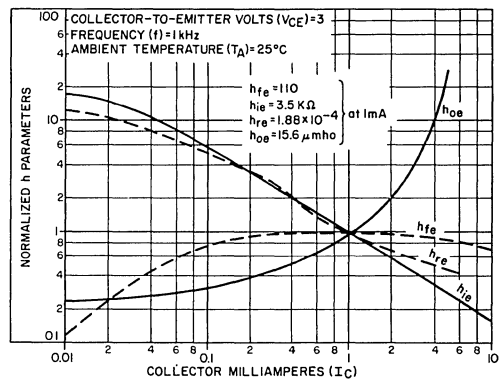


Fig. 12 - Forward Current-Transfer Ratio ( $h_{fe}$ ), Short-Circuit Input Impedance ( $h_{ie}$ ), Open-Circuit Output Impedance ( $h_{oe}$ ), and Open-Circuit Reverse Voltage-Transfer Ratio ( $h_{re}$ ) vs Collector Current

7  
ARRAYS

# CA3018, CA3018A

## TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

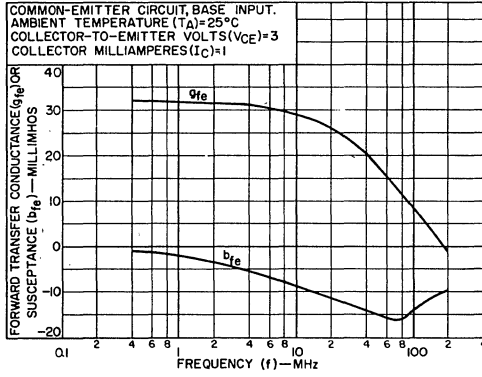


Fig.13 - Forward Transfer Admittance ( $Y_{fe}$ )

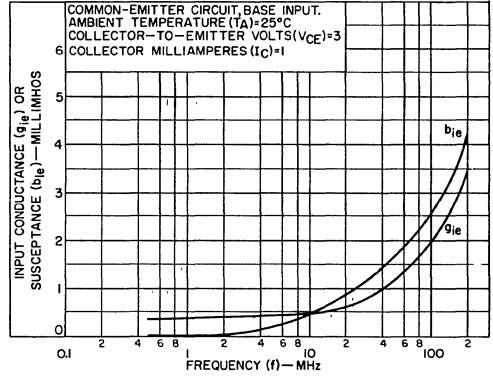


Fig.14 - Input Admittance ( $Y_{ie}$ )

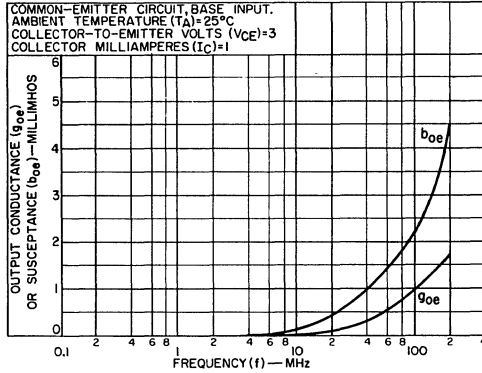


Fig.15 - Output Admittance ( $Y_{oe}$ )

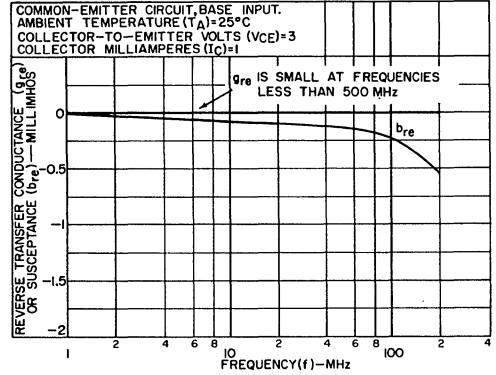


Fig.16 - Reverse Transfer Admittance ( $Y_{re}$ )

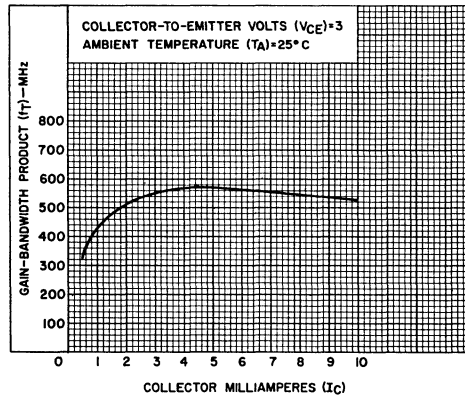


Fig.17 - Typical Gain-Bandwidth Product ( $f_T$ ) vs Collector Current

August 1991

Diode Array

### Features

- Six Matched Diodes on a Common Substrate
- Excellent Reverse Recovery Time ..... 1ns Typical
- Matched Monolithic Construction -  $V_F$  Matched Within 5mV
- Low Diode Capacitance -  $C_D = 0.65\text{pF}$  Typical at  $V_R = -2\text{V}$

### Applications

- Ultra-Fast Low-Capacitance Matched Diodes for Applications in Communications and Switching Systems
- Balanced Modulators or Demodulators
- Ring Modulators
- High Speed Diode Gates
- Analog Switches

### Description

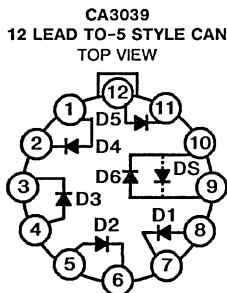
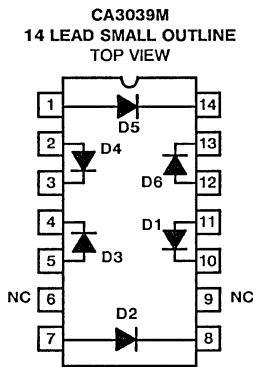
The CA3039 consists of six ultra-fast, low capacitance diodes on a common monolithic substrate. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the array extremely useful for a wide variety of applications in communication and switching systems.

Five of the diodes are independently accessible, the sixth shares a common terminal with the substrate.

For applications such as balanced modulators or ring modulators where capacitive balance is important, the substrate should be returned to a DC potential which is significantly more negative (with respect to the active diodes) than the peak signal applied.

The CA3039 is available in a 12-lead TO-5 style can package and in a 14-lead Small Outline package (M suffix).

### Pinouts



### Schematic

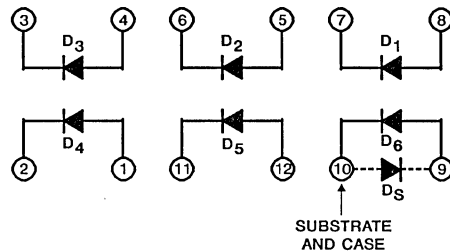


FIGURE 1. SCHEMATIC DIAGRAM FOR CA3039



## CA3039

### ABSOLUTE MAXIMUM RATINGS at $T_A = 25^\circ\text{C}$

|  |  |
|--|--|
| Dissipation:<br>Any one diode unit. . . . . 100 mW<br>Total for device . . . . . 600 mW<br>For $T_A > 55^\circ\text{C}$ . . . . . derate linearly 5.7 mW/ $^\circ\text{C}$ | Peak Inverse Voltage, PIV for: $D_1$ - $D_5$ . . . . . 5 V<br>$D_6$ . . . . . 0.5 V<br>Peak Diode-to-Substrate Voltage, $V_{DI}$<br>for $D_1$ - $D_5$ (term. 1,4,5,8 or 12 to term. 10) +20, -1 V<br>DC Forward Current, $I_F$ . . . . . 25 mA<br>Peak Recurrent Forward Current, $I_F$ . . . . . 100 mA<br>Peak Forward Surge Current, $I_F$ (surge) . . . . . 100 mA |
| Temperature Range:<br>Operating . . . . . $-55$ to $+125^\circ\text{C}$<br>Storage . . . . . $-65$ to $+150^\circ\text{C}$   |  |

#### LEAD TEMPERATURE (During Soldering)

At distance  $1/16 \pm 1/32$  inch ( $1.59 \pm 0.79\text{mm}$ )  
 from case for 10 seconds max. . . . .  $+265^\circ\text{C}$

### ELECTRICAL CHARACTERISTICS, at $T_A = 25^\circ\text{C}$

*Characteristics apply for each diode unit, unless otherwise specified.*

| CHARACTERISTICS   | SYMBOLS                                    | SPECIAL TEST CONDITIONS      | LIMITS |       |      | UNITS                        | CHARACTERISTIC CURVES<br>FIG. |
|---|--|------------------------------|--------|-------|------|------------------------------|-------------------------------|
|   |  |                              | MIN.   | TYP.  | MAX. |                              |                               |
| DC Forward Voltage Drop   | $V_F$                                      | $I_F = 50 \mu\text{A}$       | -      | 0.65  | 0.69 | V                            | 2                             |
|   |  |                              | -      | 0.73  | 0.78 | V                            |                               |
|   |  |                              | -      | 0.76  | 0.80 | V                            |                               |
|   |  |                              | -      | 0.81  | 0.90 | V                            |                               |
| DC Reverse Breakdown Voltage  | $V_{(BR)R}$                                | $I_R = -10 \mu\text{A}$      | 5      | 7     | -    | V                            | -                             |
| DC Reverse Breakdown Voltage<br>Between any Diode Unit and Substrate                                    | $V_{(BR)R}$                                | $I_R = -10 \mu\text{A}$      | 20     | -     | -    | V                            | -                             |
| DC Reverse (Leakage) Current  | $I_R$                                      | $V_R = -4$ V                 | -      | 0.016 | 100  | nA                           | 3                             |
| DC Reverse (Leakage) Current<br>Between any Diode Unit and Substrate                                    | $I_R$                                      | $V_R = -10$ V                | -      | 0.022 | 100  | nA                           | 4                             |
| Magnitude of Diode Offset Voltage<br>(Difference in DC Forward Voltage<br>Drops of any Two Diode Units) | $ V_{F1} - V_{F2} $                        | $I_F = 1$ mA                 | -      | 0.5   | 5    | mV                           | 2                             |
| Temperature Coefficient of $ V_{F1} - V_{F2} $  | $\frac{\Delta V_{F1} - V_{F2} }{\Delta T}$ | $I_F = 1$ mA                 | -      | 1     | -    | $\mu\text{V}/^\circ\text{C}$ | 5                             |
| Temperature Coefficient of Forward Drop   | $\frac{\Delta V_F}{\Delta T}$              | $I_F = 1$ mA                 | -      | -1.9  | -    | $\text{mV}/^\circ\text{C}$   | 6                             |
| DC Forward Voltage Drop for<br>Anode-to-Substrate Diode ( $D_5$ )                                       | $V_F$                                      | $I_F = 1$ mA                 | -      | 0.65  | -    | V                            | -                             |
| Reverse Recovery Time   | $t_{rr}$                                   | $I_F = 10$ mA, $I_R = 10$ mA | -      | 1     | -    | ns                           | -                             |
| Diode Resistance  | $R_D$                                      | $f = 1$ kHz, $I_F = 1$ mA    | 25     | 30    | 45   | $\Omega$                     | 7                             |
| Diode Capacitance   | $C_D$                                      | $V_R = -2$ V, $I_F = 0$      | -      | 0.65  | -    | pF                           | 8                             |
| Diode-to-Substrate Capacitance  | $C_{DI}$                                   | $V_{DI} = +4$ V, $I_F = 0$   | -      | 3.2   | -    | pF                           | 9                             |

TYPICAL CHARACTERISTICS

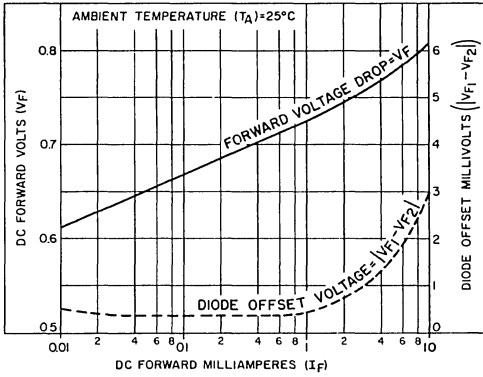


Fig. 2 - DC forward voltage drop (any diode) and diode offset voltage vs DC forward current

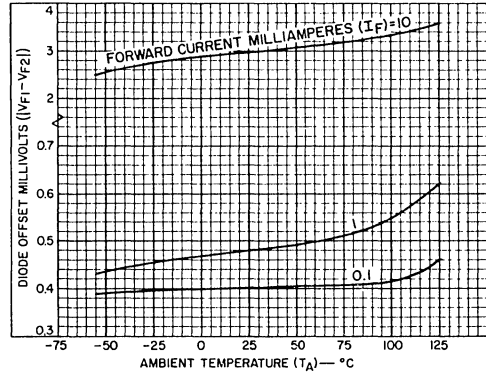


Fig. 5 - Diode offset voltage (any diode) vs temperature

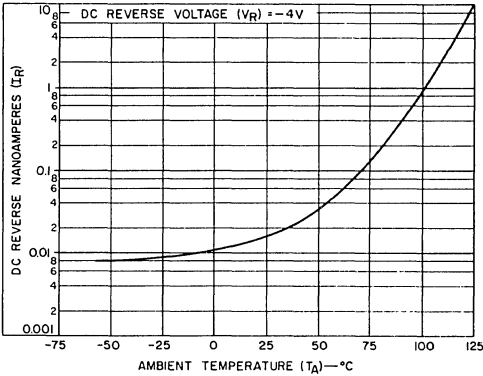


Fig. 3 - DC reverse (leakage) current (diodes 1,2,3,4,5) vs temperature

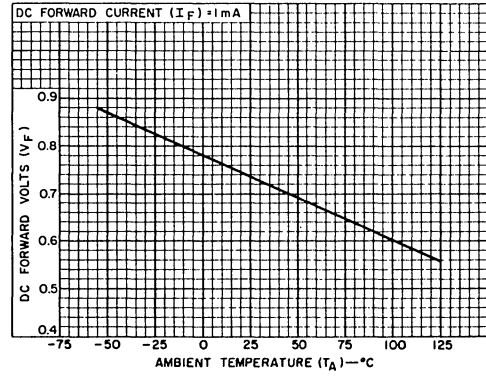


Fig. 6 - DC forward voltage drop (any diode) vs temperature

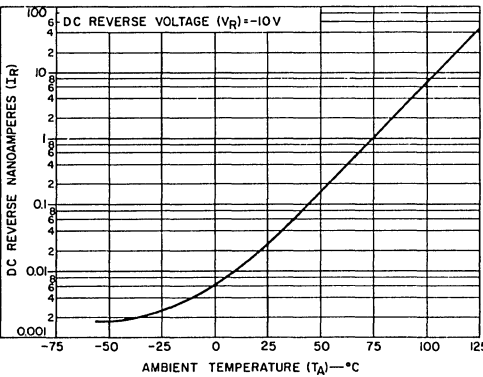


Fig. 4 - DC reverse (leakage) current between diodes (1,2,3,4,5) and substrate vs temperature

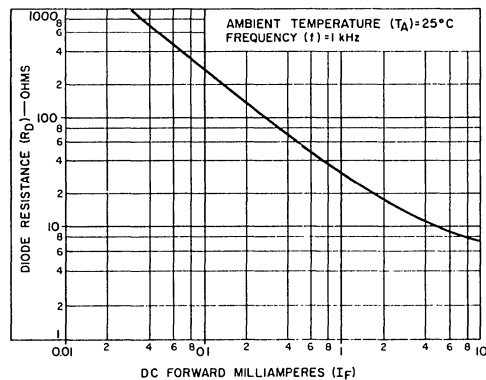


Fig. 7 - Diode resistance (any diode) vs DC forward current

TYPICAL CHARACTERISTICS

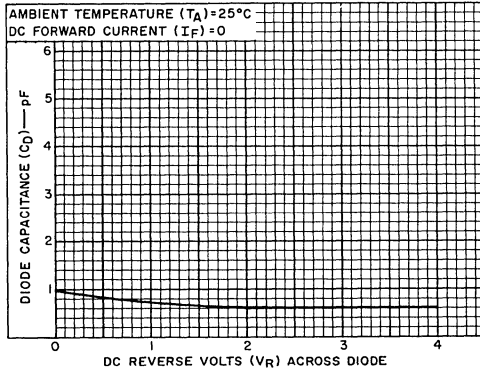


Fig. 8 - Diode capacitance (diodes 1,2,3,4,5) vs reverse voltage

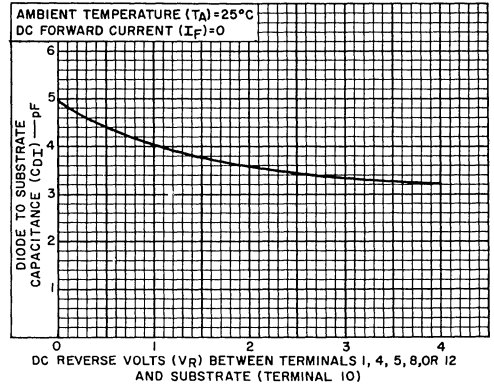


Fig. 9 - Diode-to-substrate capacitance vs reverse voltage

# CA3045 CA3046

## General Purpose N-P-N Transistor Arrays

August 1991

### Features

- Two Matched Transistors:  $V_{BE}$  Matched  $\pm 5mV$ ; Input Offset Current  $2\mu A$  Max at  $I_C = 1mA$
- 5 General Purpose Monolithic Transistors
- Operation From DC to 120MHz
- Wide Operating Current Range
- Low Noise Figure ..... 3.2dB Typical at 1KHz
- Full Military Temperature Range ...  $-55^{\circ}C$  to  $+125^{\circ}C$

### Applications

- Three Isolated Transistors and One Differentially Connected Transistor Pair for Low-Power Applications at Frequencies from DC through the VHF Range
- Custom Designed Differential Amplifiers
- Temperature compensated amplifiers
- See Application Note, ICAN-5296 "Application of the CA3018 Integrated-Circuit Transistor Array" for Suggested Applications

### Description

The CA3045 and CA3046 each consist of five general purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3045 and CA3046 are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits. However, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

The CA3045 is supplied in a 14-lead dual-in-line hermetic (welded-seal) ceramic package and the CA3045F in a 14-lead dual-in-line hermetic (frit-seal) ceramic package.

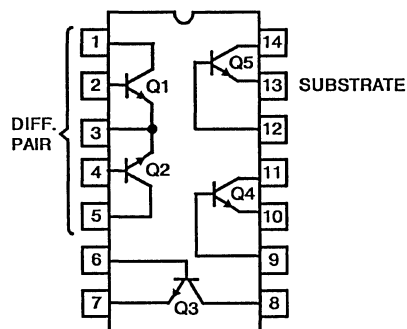
The CA3046 is electrically identical to the CA3045 but is supplied in a 14-lead dual-in-line plastic package (no suffix) and in 14-lead Small Outline package (M suffix).

### Packaging Information

| PACKAGE                                | SUFFIX | CA3045 | CA3046 |
|--|--------|--------|--------|
| 14-Lead Dual-In-Line Plastic           | None   |        | ✓      |
| 14-Lead Dual-In-Line Ceramic           | None   | ✓      |        |
| 14-Lead Dual-In-Line Frit-Seal Ceramic | F      | ✓      |        |
| Chip                                   | H      |        | ✓      |
| 14-Lead Small Outline                  | M      |        | ✓      |

### Pinout

CA3045, CA3046  
14 PIN PACKAGES  
TOP VIEW



### Schematic Diagram

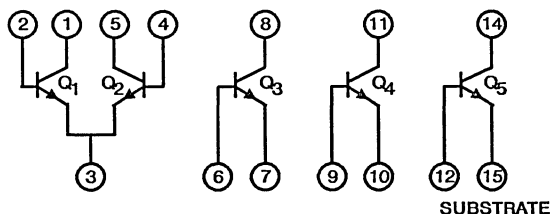


FIGURE 1.

## CA3045, CA3046

### ABSOLUTE MAXIMUM RATINGS AT $T_A = 25^\circ\text{C}$

|   | CA3045          |               | CA3046, CA3045F |               |                      |
|---|-----------------|---------------|-----------------|---------------|----------------------|
|   | Each Transistor | Total Package | Each Transistor | Total Package |                      |
| Power Dissipation:                                  |                 |               |                 |               |                      |
| $T_A$ up to $55^\circ\text{C}$ .....                | —               | —             | 300             | 750           | mW                   |
| $T_A > 55^\circ\text{C}$ .....                      | —               | —             | Derate at 6.67  |               | mW/ $^\circ\text{C}$ |
| $T_A$ up to $75^\circ\text{C}$ .....                | 300             | 750           | —               | —             | mW                   |
| $T_A > 75^\circ\text{C}$ .....                      | Derate at 8     |               | —               | —             | mW/ $^\circ\text{C}$ |
| Collector-to-Emitter Voltage, $V_{CEO}$ .....       | 15              | —             | 15              | —             | V                    |
| Collector-to-Base Voltage, $V_{CBO}$ .....          | 20              | —             | 20              | —             | V                    |
| Collector-to-Substrate Voltage, $V_{C1O}^*$ .....   | 20              | —             | 20              | —             | V                    |
| Emitter-to-Base Voltage, $V_{EBO}$ .....            | 5               | —             | 5               | —             | V                    |
| Collector Current .....                             | 50              | —             | 50              | —             | mA                   |
| Temperature Range:                                  |                 |               |                 |               |                      |
| Operating .....                                     | —55 to +125     |               | —55 to +125     |               | $^\circ\text{C}$     |
| Storage .....                                       | —65 to +150     |               | —65 to +150     |               | $^\circ\text{C}$     |
| Lead Temperature (During Soldering):                |                 |               |                 |               |                      |
| At distance $1/16 \pm 1/32''$ ( $1.59 \pm 0.79$ mm) |                 |               |                 |               |                      |
| from case for 10 seconds max. ....                  | +265            |               | +265            |               | $^\circ\text{C}$     |

\* The collector of each transistor of the CA3045 and CA3046 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

### ELECTRICAL CHARACTERISTICS, at $T_A = 25^\circ\text{C}$

Characteristics apply for each transistor in the CA3045 and CA3046 as specified.

| CHARACTERISTICS   | SYMBOLS                            | SPECIAL TEST CONDITIONS  | LIMITS                     |                  |             | UNITS                        | CHARACTERISTIC CURVES |
|---|------------------------------------|--|----------------------------|------------------|-------------|------------------------------|-----------------------|
|   |                                    |  | Type CA3045<br>Type CA3046 |                  |             |                              |                       |
|   |                                    |  | MIN.                       | TYP.             | MAX.        |                              |                       |
| STATIC CHARACTERISTICS  |                                    |  |                            |                  |             |                              |                       |
| Collector-to-Base Breakdown Voltage   | $V_{(BR)CBO}$                      | $I_C = 10 \mu\text{A}, I_E = 0$  | 20                         | 60               | —           | V                            | —                     |
| Collector-to-Emitter Breakdown Voltage  | $V_{(BR)CEO}$                      | $I_C = 1 \text{ mA}, I_B = 0$  | 15                         | 24               | —           | V                            | —                     |
| Collector-to-Substrate Breakdown Voltage  | $V_{(BR)C1O}$                      | $I_C = 10 \mu\text{A}, I_{C1} = 0$   | 20                         | 60               | —           | V                            | —                     |
| Emitter-to-Base Breakdown Voltage   | $V_{(BR)EBO}$                      | $I_E = 10 \mu\text{A}, I_C = 0$  | 5                          | 7                | —           | V                            | —                     |
| Collector-Cutoff Current  | $I_{CBO}$                          | $V_{CE} = 10 \text{ V}, I_E = 0$   | —                          | 0.002            | 40          | nA                           | 2                     |
| Collector-Cutoff Current  | $I_{CEO}$                          | $V_{CE} = 10 \text{ V}, I_B = 0$   | —                          | See curve        | 0.5         | $\mu\text{A}$                | 3                     |
| Static Forward Current-Transfer Ratio (Static Beta) (Note 1)  | $h_{FE}$                           | $V_{CE} = 3 \text{ V} \begin{cases} I_C = 10 \text{ mA} \\ I_C = 1 \text{ mA} \\ I_C = 10 \mu\text{A} \end{cases}$ | —<br>40<br>—               | 100<br>100<br>54 | —<br>—<br>— | —<br>—<br>—                  | 4                     |
| Input Offset Current for Matched Pair $Q_1$ and $Q_2$ . $ I_{101} - I_{102} $ (Note 1)  |                                    | $V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$   | —                          | 0.3              | 2           | $\mu\text{A}$                | 5                     |
| Base-to-Emitter Voltage (Note 1)  | $V_{BE}$                           | $V_{CE} = 3 \text{ V} \begin{cases} I_E = 1 \text{ mA} \\ I_E = 10 \text{ mA} \end{cases}$                         | —<br>—                     | 0.715<br>0.800   | —           | V                            | 6                     |
| Magnitude of Input Offset Voltage for Differential Pair $ V_{BE1} - V_{BE2} $ (Note 1)  |                                    | $V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$   | —                          | 0.45             | 5           | mV                           | 6,8                   |
| Magnitude of Input Offset Voltage for Isolated Transistors $ V_{BE3} - V_{BE4} $ , $ V_{BE4} - V_{BE5} $ , $ V_{BE5} - V_{BE3} $ (Note 1) |                                    | $V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$   | —                          | 0.45             | 5           | mV                           | 6,8                   |
| Temperature Coefficient of Base-to-Emitter Voltage  | $\frac{\Delta V_{BE}}{\Delta T}$   | $V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$   | —                          | —1.9             | —           | mV/ $^\circ\text{C}$         | 7                     |
| Collector-to-Emitter Saturation Voltage   | $V_{CES}$                          | $I_B = 1 \text{ mA}, I_C = 10 \text{ mA}$  | —                          | 0.23             | —           | V                            | —                     |
| Temperature Coefficient: Magnitude of Input-Offset Voltage  | $\frac{ \Delta V_{10} }{\Delta T}$ | $V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$   | —                          | 1.1              | —           | $\mu\text{V}/^\circ\text{C}$ | 8                     |

# CA3045, CA3046

## ELECTRICAL CHARACTERISTICS (Cont'd.)

| DYNAMIC CHARACTERISTICS   |          |   |     |                      |   |                  |      |
|---|----------|---|-----|----------------------|---|------------------|------|
| Low-Frequency Noise Figure                                      | NF       | $f = 1 \text{ kHz}, V_{CE} = 3 \text{ V}, I_C = 100 \mu\text{A}$<br>Source Resistance = $1 \text{ k}\Omega$ | -   | 3.25                 | - | dB               | 9(b) |
| Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: |          |   |     |                      |   |                  |      |
| Forward Current-Transfer Ratio                                  | $h_{fe}$ | $f = 1 \text{ kHz}, V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$   | -   | 110                  | - | -                | 10   |
| Short-Circuit Input Impedance                                   | $h_{ie}$ |   | -   | 3.5                  | - | $\text{k}\Omega$ |      |
| Open-Circuit Output Impedance                                   | $h_{oe}$ |   | -   | 15.6                 | - | $\mu\text{mho}$  |      |
| Open-Circuit Reverse Voltage-Transfer Ratio                     | $h_{re}$ |   | -   | $1.8 \times 10^{-4}$ | - | -                |      |
| Admittance Characteristics:                                     |          |   |     |                      |   |                  |      |
| Forward Transfer Admittance                                     | $Y_{fe}$ | $f = 1 \text{ MHz}, V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$   | -   | $31-j1.5$            | - | -                | 11   |
| Input Admittance  | $Y_{ie}$ |   | -   | $0.3+j0.04$          | - | -                | 12   |
| Output Admittance   | $Y_{oe}$ |   | -   | $0.001+j0.03$        | - | -                | 13   |
| Reverse Transfer Admittance                                     | $Y_{re}$ |   | -   | See curve            | - | -                | 14   |
| Gain-Bandwidth Product  | $f_T$    | $V_{CE} = 3 \text{ V}, I_C = 3 \text{ mA}$  | 300 | 550                  | - | MHz              | 15   |
| Emitter-to-Base Capacitance                                     | $C_{EB}$ | $V_{EB} = 3 \text{ V}, I_E = 0$   | -   | 0.6                  | - | pF               | -    |
| Collector-to-Base Capacitance                                   | $C_{CB}$ | $V_{CB} = 3 \text{ V}, I_C = 0$   | -   | 0.58                 | - | pF               | -    |
| Collector-to-Substrate Capacitance                              | $C_{CI}$ | $V_{CS} = 3 \text{ V}, I_C = 0$   | -   | 2.8                  | - | pF               | -    |

### NOTES:

1. Actual forcing current is via the emitter for this test.

## STATIC CHARACTERISTICS

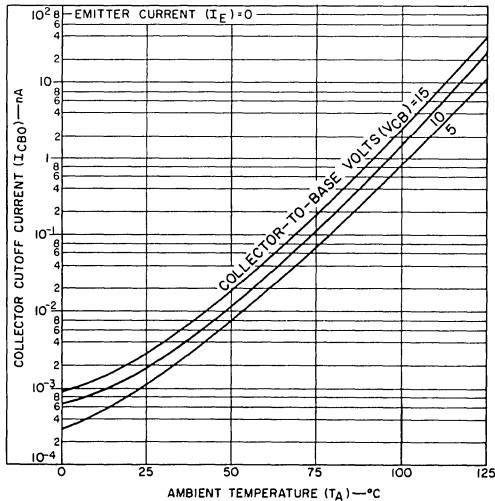


Fig. 2 - Typical collector-to-base cutoff current vs ambient temperature for each transistor.

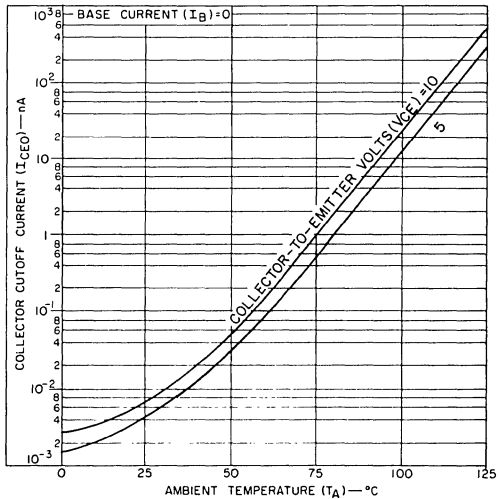


Fig. 3 - Typical collector-to-emitter cutoff current vs ambient temperature for each transistor.

STATIC CHARACTERISTICS

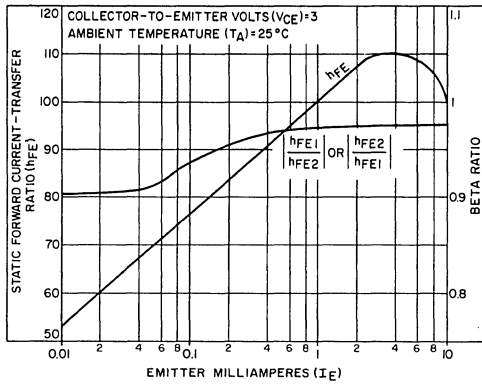


Fig.4 - Typical static forward current-transfer ratio and beta ratio for transistors Q<sub>1</sub> and Q<sub>2</sub> vs emitter current.

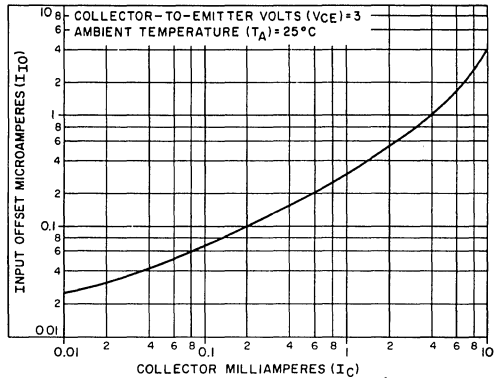


Fig.5 - Typical input offset current for matched transistor pair Q<sub>1</sub>Q<sub>2</sub> vs collector current.

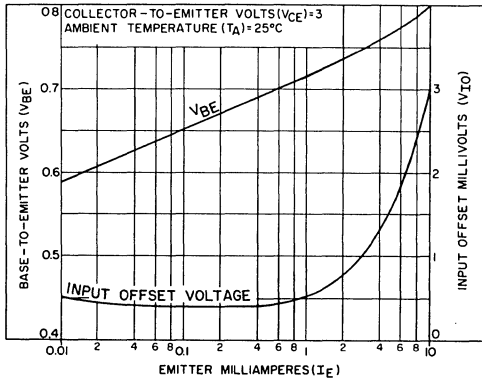


Fig.6 - Typical static base-to-emitter voltage characteristic and input offset voltage for differential pair and paired isolated transistors vs emitter current.

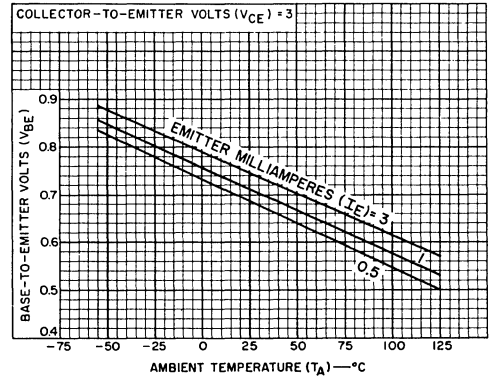


Fig.7 - Typical base-to-emitter voltage characteristic vs ambient temperature for each transistor.

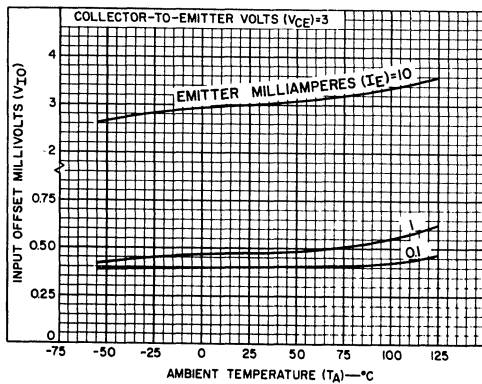


Fig.8 - Typical input offset voltage characteristics for differential pair and paired isolated transistors vs ambient temperature.

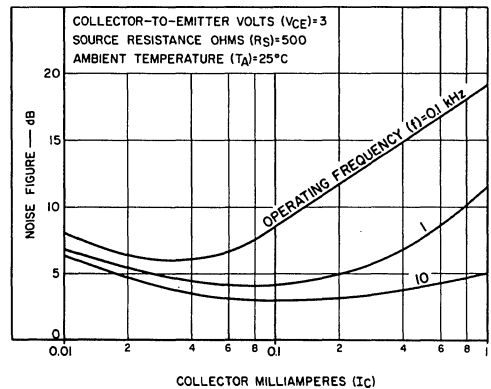


Fig.9(a) - Typical noise figure vs collector current.

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

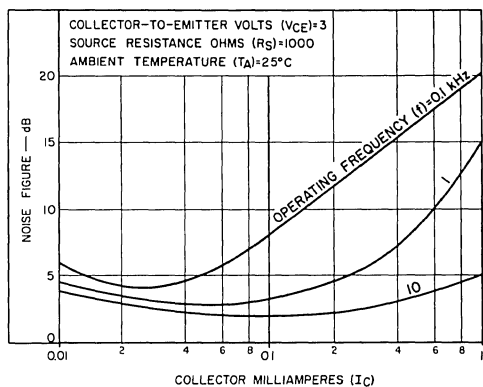


Fig.9(b) - Typical noise figure vs collector current.

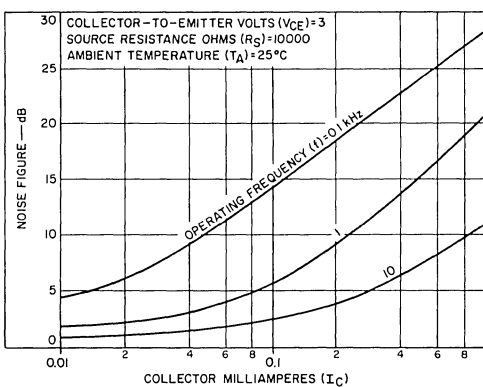


Fig.9(c) - Typical noise figure vs collector current.

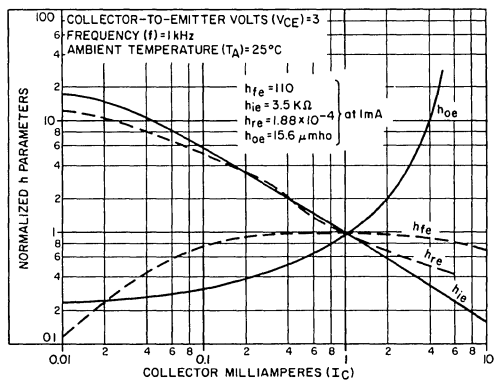


Fig.10 - Typical normalized forward current-transfer ratio, short-circuit input impedance, open-circuit output impedance, and open-circuit reverse voltage-transfer ratio vs collector current.

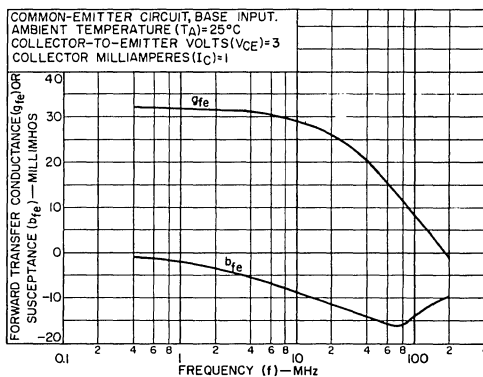


Fig.11 - Typical forward transfer admittance vs frequency.

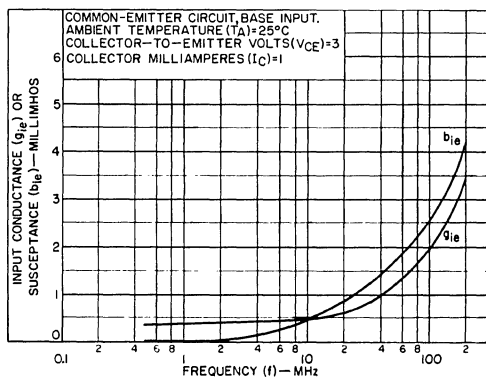


Fig.12 - Typical input admittance vs frequency.

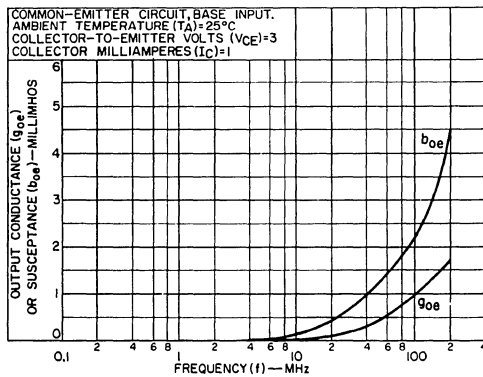


Fig.13 - Typical output admittance vs frequency.



CA3045, CA3046

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

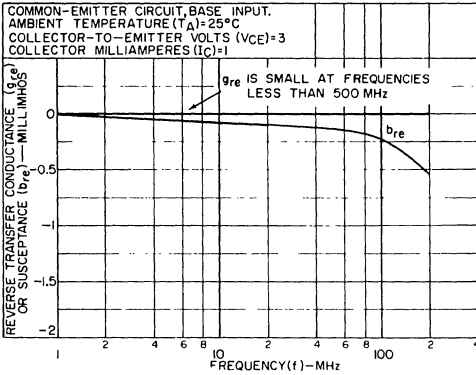


Fig.14 - Typical reverse transfer admittance vs frequency.

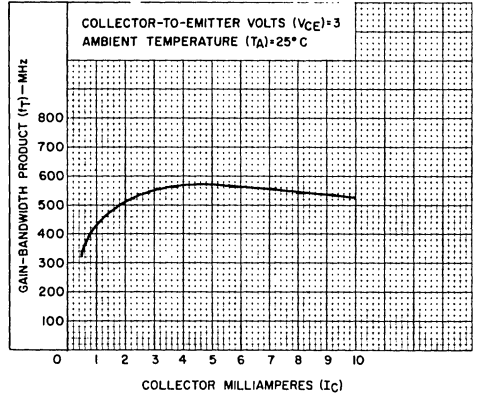


Fig.15 - Typical gain-bandwidth product vs collector current.

August 1991

### Features

- CA3081 - Common-Emitter Array
- CA3082 - Common-Collector Array
- Directly Drive 7-Segment Incandescent Displays and Light-Emitting-Diode (LED) Display
- 7 Transistors Permit a Wide Range of Applications in Either a Common-Emitter (CA3081) or Common-Collector (CA3082) Configuration
- High  $I_C$  ..... 100mA Max
- Low  $V_{CE}$  Sat (at 50mA) ..... 0.4V Typ

### Applications

- Drivers for
  - ▶ Incandescent Display Devices
  - ▶ LED Displays
  - ▶ Relay Control
  - ▶ Thyristor Firing

### Description

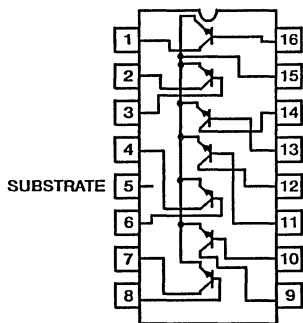
CA3081 and CA3082 consist of seven high-current (to 100mA) silicon n-p-n transistors on a common monolithic substrate. The CA3081 is connected in a common-emitter configuration and the CA3082 is connected in a common-collector configuration.

The CA3081 and CA3082 are capable of directly driving seven-segment displays, and light-emitting diode (LED) displays. These types are also well-suited for a variety of other drive applications, including relay control and thyristor firing.

The CA3081 and CA3082 are supplied in a 16-lead Small Outline package (M suffix), in a 16-lead dual-in-line plastic package (no suffix), and in a 16-lead dual-in-line frit-seal ceramic package (F suffix), which include a separate substrate connection for maximum flexibility in circuit design. Both types are also available in chip form.

### Functional Diagrams

CA3081  
COMMON-EMITTER CONFIGURATION



CA3082  
COMMON-COLLECTOR CONFIGURATION

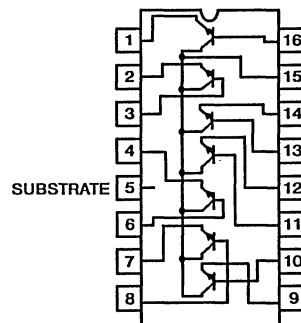


FIGURE 1. FUNCTIONAL DIAGRAMS OF TYPES CA3081 AND CA3082

## CA3081, CA3082

### MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^\circ\text{C}$

**Power Dissipation:**

|                                |                      |                            |
|--------------------------------|----------------------|----------------------------|
| Any one transistor .....       | 500                  | mW                         |
| Total package .....            | 750                  | mW                         |
| Above $55^\circ\text{C}$ ..... | Derate linearly 6.67 | $\text{mW}/^\circ\text{C}$ |

**Ambient Temperature Range:**

|                 |                 |                  |
|-----------------|-----------------|------------------|
| Operating ..... | $-55$ to $+125$ | $^\circ\text{C}$ |
| Storage .....   | $-65$ to $+150$ | $^\circ\text{C}$ |

**Lead Temperature (During Soldering):**

|   |     |                  |
|---|-----|------------------|
| At distance $1/16'' \pm 1/32''$ ( $1.59 \text{ mm} \pm 0.79 \text{ mm}$ ) |     |                  |
| from case for 10 seconds max. ....  | 265 | $^\circ\text{C}$ |

The following ratings apply for each transistor in the device:

|   |     |    |
|---|-----|----|
| Collector-to-Emitter Voltage ( $V_{\text{CEO}}$ ) .....     | 16  | V  |
| Collector-to-Base Voltage ( $V_{\text{CBO}}$ ) .....        | 20  | V  |
| Collector-to-Substrate Voltage ( $V_{\text{CIO}}$ ) * ..... | 20  | V  |
| Emitter-to-Base Voltage ( $V_{\text{EBO}}$ ) .....          | 5   | V  |
| Collector Current ( $I_{\text{C}}$ ) .....                  | 100 | mA |
| Base Current ( $I_{\text{B}}$ ) .....                       | 20  | mA |

\* The collector of each transistor of the CA3081 and CA3082 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and

provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

### ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$

**For Equipment Design**

| CHARACTERISTIC   | SYMBOL                      | TEST CONDITIONS   |                              | LIMITS |      |      | UNITS         |
|--|-----------------------------|---|------------------------------|--------|------|------|---------------|
|  |                             |   | Typ. Char. Curve<br>Fig. No. | Min.   | Typ. | Max. |               |
|  |                             |   |                              |        |      |      |               |
| Collector-to-Base Breakdown Voltage                        | $V_{(\text{BR})\text{CBO}}$ | $I_{\text{C}} = 500 \mu\text{A}, I_{\text{E}} = 0$                    | —                            | 20     | 60   | —    | V             |
| Collector-to-Substrate Breakdown Voltage                   | $V_{(\text{BR})\text{CIO}}$ | $ I_{\text{C}}  = 500 \mu\text{A}, I_{\text{B}} = 0$                  | —                            | 20     | 60   | —    | V             |
| Collector-to-Emitter Breakdown Voltage                     | $V_{(\text{BR})\text{CEO}}$ | $I_{\text{C}} = 1 \text{ mA}, I_{\text{B}} = 0$                       | —                            | 16     | 24   | —    | V             |
| Emitter-to-Base Breakdown Voltage                          | $V_{(\text{BR})\text{EBO}}$ | $I_{\text{C}} = 500 \mu\text{A}$                                      | —                            | 5      | 6.9  | —    | V             |
| DC Forward-Current Transfer Ratio                          | $h_{\text{FE}}$             | $V_{\text{CE}} = 0.5 \text{ V}, I_{\text{C}} = 30 \text{ mA}$         | —                            | 30     | 68   | —    |               |
|  |                             | $V_{\text{CE}} = 0.8 \text{ V}, I_{\text{C}} = 50 \text{ mA}$         | —                            | 40     | 70   | —    |               |
| Base-to-Emitter Saturation Voltage                         | $V_{\text{BE sat}}$         | $I_{\text{C}} = 30 \text{ mA}, I_{\text{B}} = 1 \text{ mA}$           | 3                            | —      | 0.87 | 1.2  | V             |
| Collector-to-Emitter Saturation Voltage:<br>CA3081, CA3082 | $V_{\text{CE sat}}$         | $I_{\text{C}} = 30 \text{ mA}, I_{\text{B}} = 1 \text{ mA}$           | —                            | —      | 0.27 | 0.5  | V             |
|  |                             | CA3081<br>$I_{\text{C}} = 50 \text{ mA}, I_{\text{B}} = 5 \text{ mA}$ | 4                            | —      | 0.4  | 0.7  |               |
|  |                             | CA3082<br>$I_{\text{C}} = 50 \text{ mA}, I_{\text{B}} = 5 \text{ mA}$ | 4                            | —      | 0.4  | 0.8  |               |
| Collector-Cutoff Current                                   | $I_{\text{CEO}}$            | $V_{\text{CE}} = 10 \text{ V}, I_{\text{B}} = 0$                      | —                            | —      | —    | 10   | $\mu\text{A}$ |
| Collector-Cutoff Current                                   | $I_{\text{CBO}}$            | $V_{\text{CB}} = 10 \text{ V}, I_{\text{E}} = 0$                      | —                            | —      | —    | 1    | $\mu\text{A}$ |

# CA3081, CA3082

## TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR OF TYPES CA3081 AND CA3082

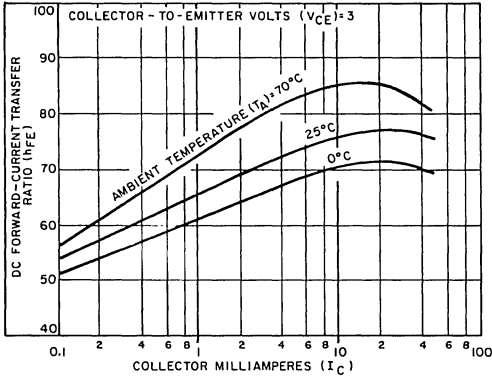


Fig. 2- $h_{FE}$  vs.  $I_C$

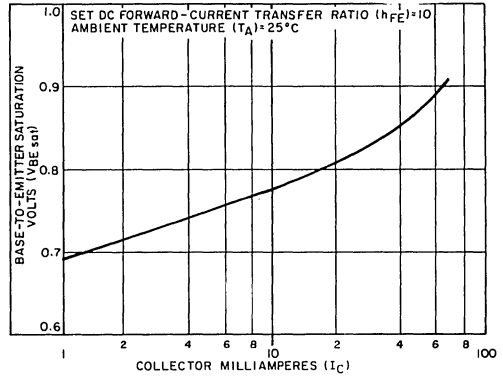


Fig. 3- $V_{BEsat}$  vs.  $I_C$

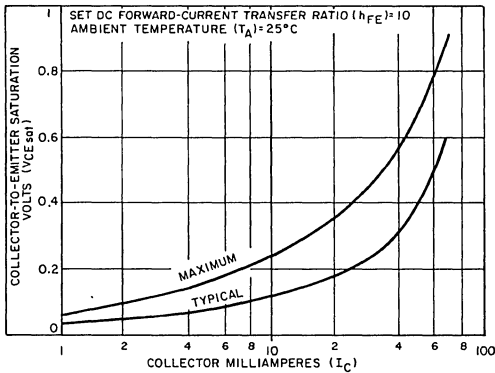


Fig. 4- $V_{CEsat}$  vs.  $I_C$  at  $T_A = 25^\circ C$

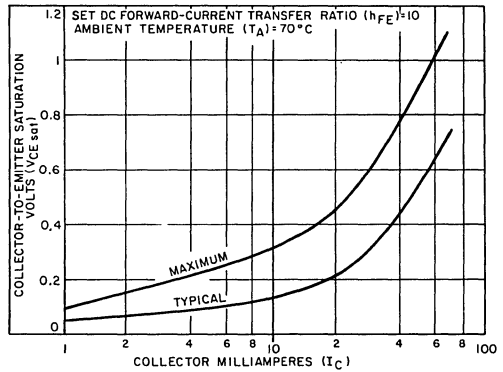


Fig. 5- $V_{CEsat}$  vs.  $I_C$  at  $T_A = 70^\circ C$

### TYPICAL READ-OUT DRIVER APPLICATIONS

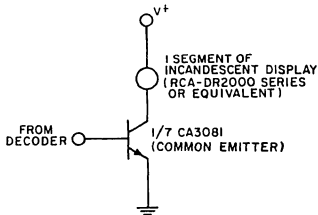
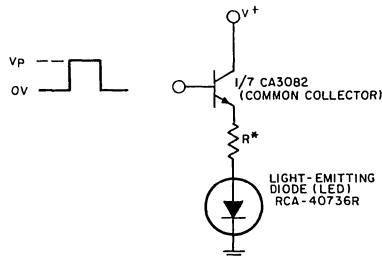


Fig. 6—Schematic diagram showing one transistor of the CA3081 driving one segment of an incandescent display.



\*THE RESISTANCE FOR R IS DETERMINED BY THE RELATIONSHIP

$$R = \frac{V_P - V_{BE} - V_F(LED)}{I(LED)}$$

$$R = 0 \text{ FOR } V_P = V_{BE} + V_F(LED)$$

WHERE:  $V_P$  = INPUT PULSE VOLTAGE

$V_F$  = FORWARD VOLTAGE DROP ACROSS THE DIODE

Fig. 7—Schematic diagram showing one transistor of the CA3082 driving a light-emitting diode (LED).

## General-Purpose High-Current N-P-N Transistor Array

August 1991

### Features

- High  $I_C$  ..... 100mA Max
- Low  $V_{CEsat}$  (at 50mA) ..... 0.7V Max
- Matched Pair (Q1 and Q2)  
 $V_{IO}$  ( $V_{BE}$  Matched) .....  $\pm 5mV$  Max  
 $I_{IO}$  (at 1mA) ..... 2.5 $\mu A$  Max
- 5 Independent Transistors Plus Separate Substrate Connection

### Applications

- Signal Processing and Switching Systems Operating from DC to VHF
- Lamp and Relay Driver
- Differential Amplifier
- Temperature-Compensated Amplifier
- Thyristor Firing
- See Application Note, ICAN-5296 "Application of the CA3018 Circuit Transistor Array" for Suggested Applications

### Description

The CA3083 is a versatile array of five high-current (to 100mA) n-p-n transistors on a common monolithic substrate. In addition, two of these transistors (Q1 and Q2) are matched at low currents (i.e. 1mA) for applications in which offset parameters are of special importance.

Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design. The CA3083 is supplied in a 16-lead dual-in-line frit-seal ceramic package (F suffix), a 16-lead Small Outline package (M suffix), and a 16-lead dual-in-line plastic package (no suffix). The CA3083 is also available in chip form.

### Functional Diagram

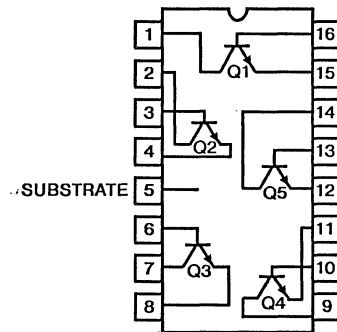


FIGURE 1.

# CA3083

## MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^\circ\text{C}$

### Power Dissipation:

|                                |                      |                            |
|--------------------------------|----------------------|----------------------------|
| Any one transistor .....       | 500                  | mW                         |
| Total package .....            | 750                  | mW                         |
| Above $55^\circ\text{C}$ ..... | Derate linearly 6.67 | $\text{mW}/^\circ\text{C}$ |

### Ambient Temperature Range:

|                 |                 |                  |
|-----------------|-----------------|------------------|
| Operating ..... | $-55$ to $+125$ | $^\circ\text{C}$ |
| Storage .....   | $-65$ to $+150$ | $^\circ\text{C}$ |

### Lead Temperature (During Soldering):

|   |     |                  |
|---|-----|------------------|
| At distance $1/16'' \pm 1/32''$ ( $1.59 \text{ mm} \pm 0.79 \text{ mm}$ )<br>from case for 10 seconds max. .... | 265 | $^\circ\text{C}$ |
|---|-----|------------------|

The following ratings apply for each transistor in the device:

|  |     |    |
|--|-----|----|
| Collector-to-Emitter Voltage ( $V_{\text{CEO}}$ ) .....                | 15  | V  |
| Collector-to-Base Voltage ( $V_{\text{CBO}}$ ) .....                   | 20  | V  |
| Collector-to-Substrate Voltage ( $V_{\text{CIO}}$ ) <sup>■</sup> ..... | 20  | V  |
| Emitter-to-Base Voltage ( $V_{\text{EBO}}$ ) .....                     | 5   | V  |
| Collector Current ( $I_{\text{C}}$ ) .....                             | 100 | mA |
| Base Current ( $I_{\text{B}}$ ) .....                                  | 20  | mA |

■ The collector of each transistor of the CA3083 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

## ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$

### For Equipment Design

| CHARACTERISTICS   | SYMBOL                      | TEST CONDITIONS   | LIMITS |      |      | UNITS         |               |
|---|-----------------------------|---|--------|------|------|---------------|---------------|
|   |                             |   | Min.   | Typ. | Max. |               |               |
| <b>For Each Transistor:</b>                                     |                             |   |        |      |      |               |               |
| Collector-to-Base Breakdown Voltage                             | $V_{(\text{BR})\text{CBO}}$ | $I_{\text{C}} = 100\mu\text{A}, I_{\text{E}} = 0$   | 20     | 60   | —    | V             |               |
| Collector-to-Emitter Breakdown Voltage                          | $V_{(\text{BR})\text{CEO}}$ | $I_{\text{C}} = 1\text{mA}, I_{\text{B}} = 0$   | 15     | 24   | —    | V             |               |
| Collector-to-Substrate Breakdown Voltage                        | $V_{(\text{BR})\text{CIO}}$ | $I_{\text{CI}} = 100\mu\text{A}, I_{\text{B}} = 0, I_{\text{E}} = 0$                        | 20     | 60   | —    | V             |               |
| Emitter-to-Base Breakdown Voltage                               | $V_{(\text{BR})\text{EBO}}$ | $I_{\text{E}} = 500\mu\text{A}, I_{\text{C}} = 0$   | 5      | 6.9  | —    | V             |               |
| Collector-Cutoff Current  | $I_{\text{CEO}}$            | $V_{\text{CE}} = 10\text{V}, I_{\text{B}} = 0$  | —      | —    | 10   | $\mu\text{A}$ |               |
| Collector-Cutoff Current  | $I_{\text{CBO}}$            | $V_{\text{CB}} = 10\text{V}, I_{\text{E}} = 0$  | —      | —    | 1    | $\mu\text{A}$ |               |
| DC Forward Current Transfer Ratio (Note 1)                      | $h_{\text{FE}}$             | $V_{\text{CE}} = 3\text{V}$<br>$I_{\text{C}} = 10\text{mA}$<br>$I_{\text{C}} = 50\text{mA}$ | 2      | 40   | 76   | —             |               |
| Base-to-Emitter Voltage   | $V_{\text{BE}}$             | $V_{\text{CE}} = 3\text{V}, I_{\text{C}} = 10\text{mA}$                                     | 3      | 0.65 | 0.74 | 0.85          | V             |
| Collector-to-Emitter Saturation Voltage                         | $V_{\text{CEsat}}$          | $I_{\text{C}} = 50\text{mA}, I_{\text{B}} = 5\text{mA}$                                     | 4, 5   | —    | 0.40 | 0.70          | V             |
| Gain-Bandwidth Product  | $f_{\text{T}}$              | $V_{\text{CE}} = 3\text{V}$<br>$I_{\text{C}} = 10\text{mA}$                                 | —      | 450  | —    | MHz           |               |
| <b>For Transistors Q1 and Q2 (As a Differential Amplifier):</b> |                             |   |        |      |      |               |               |
| Absolute Input Offset Voltage                                   | $ V_{\text{IO}} $           | $V_{\text{CE}} = 3\text{V}, I_{\text{C}} = 1\text{mA}$                                      | 7      | —    | 1.2  | 5             | mV            |
| Absolute Input Offset Current                                   | $ I_{\text{IO}} $           |   | 8      | —    | 0.7  | 2.5           | $\mu\text{A}$ |

### NOTES:

1. Actual forcing current is via the emitter for this test.

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

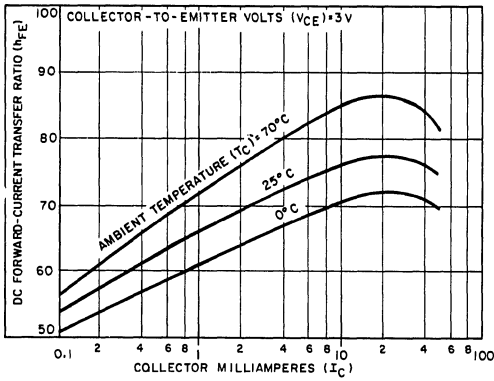


Fig.2 -  $h_{FE}$  vs  $I_C$

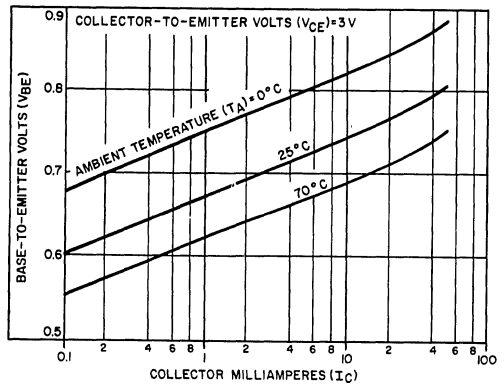


Fig.3 -  $V_{BE}$  vs  $I_C$

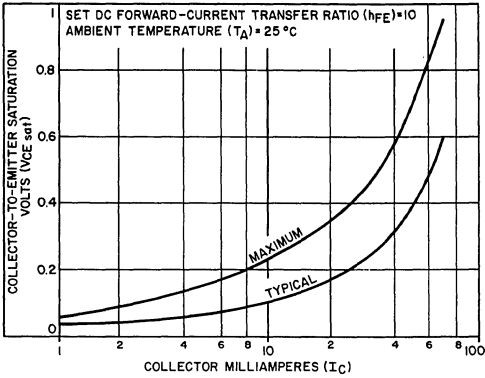


Fig.4 -  $V_{CE\ sat}$  vs  $I_C$  at 25°C

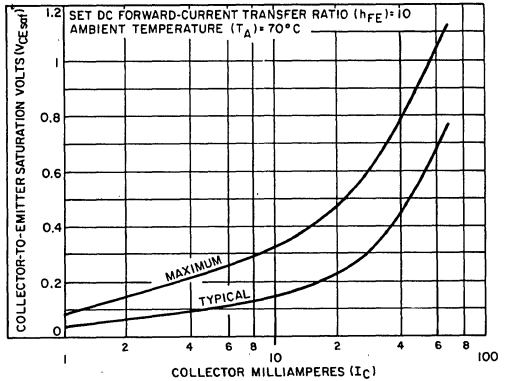


Fig.5 -  $V_{CE\ sat}$  vs  $I_C$  at 70°C

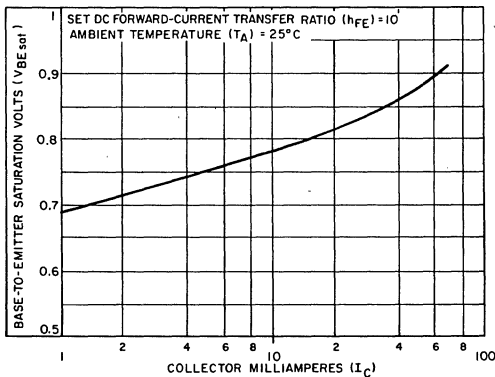


Fig.6 -  $V_{BE\ sat}$  vs  $I_C$

TYPICAL STATIC CHARACTERISTICS FOR DIFFERENTIAL AMPLIFIER

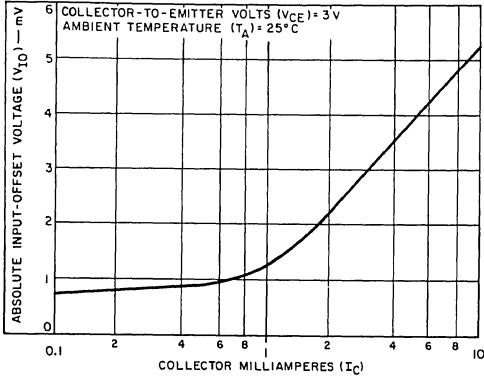


Fig.7 —  $V_{IO}$  vs  $I_C$  (transistors Q1 and Q2 as a differential amplifier).

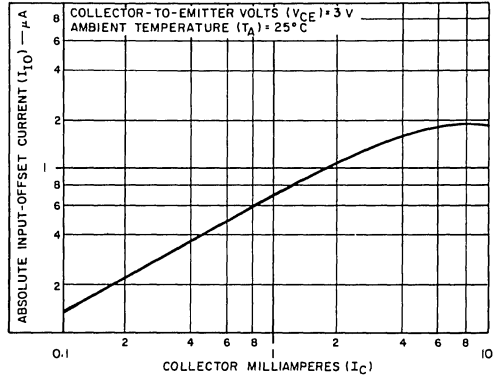


Fig.8 —  $I_{IO}$  vs  $I_C$  (transistors Q1 and Q2 as a differential amplifier).



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### Applications

- Three Isolated Transistors and One Differentially Connected Transistor Pair For Low-Power Applications from DC to 120MHz
- General-Purpose Use in Signal Processing Systems Operating in the DC to 190MHz Range
- Temperature Compensated Amplifiers
- See Application Note, ICAN-5296 "Application of the CA3018 Integrated-Circuit Transistor Array" for Suggested Applications

### Description

The CA3086 consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3086 are well suited to a wide variety of applications in low-power systems at frequencies from DC to 120 MHz. They may be used as discrete transistors in conventional circuits. However, they also provide the very significant inherent advantages unique to integrated circuits, such as compactness, ease of physical handling and thermal matching.

The CA3086 is supplied in a 14-lead dual-in-line plastic package. The CA3086F is supplied in a 14-lead dual-in-line hermetic (frit-seal) ceramic package. The CA3086M is supplied in a 14-lead Small Outline package.

### Functional Diagram

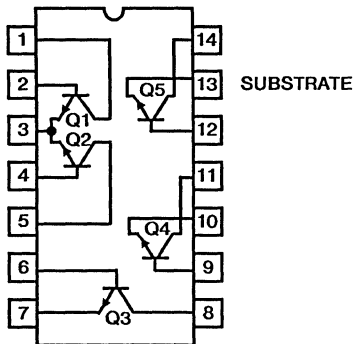


FIGURE 1.

### MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^\circ\text{C}$

#### DISSIPATION:

|  |   |
|--|---|
| Any one transistor .....                           | 300 mW                                    |
| Total package up to $T_A = 55^\circ\text{C}$ ..... | 750 mW                                    |
| Above $T_A = 55^\circ\text{C}$ .....               | Derate linearly 6.67 mW/ $^\circ\text{C}$ |

#### AMBIENT TEMPERATURE RANGE:

|                 |                                  |
|-----------------|----------------------------------|
| Operating ..... | $-55$ to $+125$ $^\circ\text{C}$ |
| Storage .....   | $-65$ to $+150$ $^\circ\text{C}$ |

#### LEAD TEMPERATURE (DURING SOLDERING):

|  |                         |
|--|-------------------------|
| At distance 1/16 $\pm$ 1/32 inch ( $1.59 \pm 0.79$ mm) ..... | $+265$ $^\circ\text{C}$ |
|--|-------------------------|

The following ratings apply for each transistor in the device:

|   |       |
|---|-------|
| COLLECTOR-TO-EMITTER VOLTAGE, $V_{CEO}$ .....     | 15 V  |
| COLLECTOR-TO-BASE VOLTAGE, $V_{CBO}$ .....        | 20 V  |
| COLLECTOR-TO-SUBSTRATE VOLTAGE, $V_{C10}^*$ ..... | 20V   |
| EMITTER-TO-BASE VOLTAGE, $V_{EBO}$ .....          | .5 V  |
| COLLECTOR CURRENT, $I_C$ .....                    | 50 mA |

\*The collector of each transistor in the CA3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action. To avoid undesirable coupling between transistors, the substrate (terminal 13) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

# CA3086

ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$   
For Equipment Design

| CHARACTERISTICS                          | SYMBOLS       | TEST CONDITIONS                         |                                     | LIMITS |           |      | UNITS         |
|--|---------------|---|-------------------------------------|--------|-----------|------|---------------|
|  |               |   | Typ. Characteristic Curves Fig. No. | Min.   | Typ.      | Max. |               |
|  |               |   |                                     |        |           |      |               |
| Collector-to-Base Breakdown Voltage      | $V_{(BR)CBO}$ | $I_C = 10 \mu\text{A}, I_E = 0$         | —                                   | 20     | 60        | —    | V             |
| Collector-to-Emitter Breakdown Voltage   | $V_{(BR)CEO}$ | $I_C = 1 \text{mA}, I_B = 0$            | —                                   | 15     | 24        | —    | V             |
| Collector-to-Substrate Breakdown Voltage | $V_{(BR)CIO}$ | $I_C = 10 \mu\text{A}, I_{CI} = 0$      | —                                   | 20     | 60        | —    | V             |
| Emitter-to-Base Breakdown Voltage        | $V_{(BR)EBO}$ | $I_E = 10 \mu\text{A}, I_C = 0$         | —                                   | 5      | 7         | —    | V             |
| Collector-Cutoff Current                 | $I_{CBO}$     | $V_{CB} = 10\text{V}, I_E = 0$          | 2                                   | —      | 0.002     | 100  | nA            |
| Collector-Cutoff Current                 | $I_{CEO}$     | $V_{CE} = 10\text{V}, I_B = 0$          | 3                                   | —      | See Curve | 5    | $\mu\text{A}$ |
| DC Forward-Current Transfer Ratio        | $h_{FE}$      | $V_{CE} = 3\text{V}, I_C = 1 \text{mA}$ | 4                                   | 40     | 100       | —    |               |

## TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

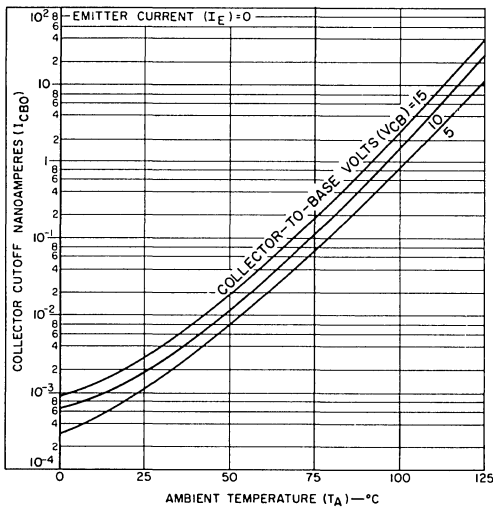


Fig.2—  $I_{CBO}$  vs  $T_A$ .

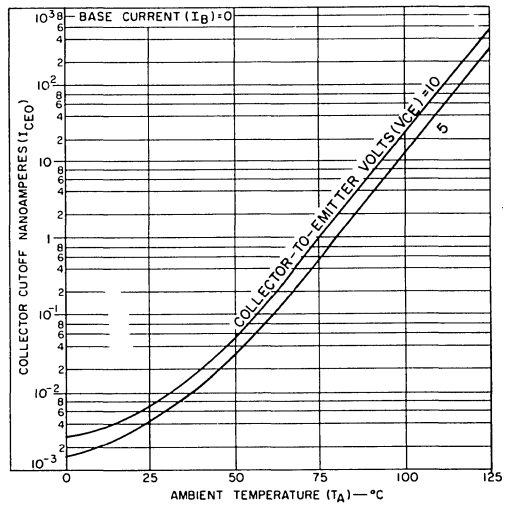


Fig.3—  $I_{CEO}$  vs  $T_A$ .

CA3086

**ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$**   
**Typical Values Intended Only for Design Guidance**

| CHARACTERISTICS   | SYMBOL                   | TEST CONDITIONS  |                       |                                      | TYPICAL VALUES       | UNITS                |
|---|--------------------------|--|-----------------------|--------------------------------------|----------------------|----------------------|
|   |                          |  |                       | Typ. Characteristics Curves Fig. No. |                      |                      |
| DC Forward-Current Transfer Ratio                               | $h_{FE}$                 | $V_{CE} = 3\text{V}$   | $I_C = 10\text{mA}$   | 4                                    | 100                  |                      |
|   |                          |  | $I_C = 10\mu\text{A}$ | 4                                    | 54                   |                      |
| Base-to-Emitter Voltage   | $V_{BE}$                 | $V_{CE} = 3\text{V}$   | $I_E = 1\text{mA}$    | 5                                    | 0.715                | V                    |
|   |                          |  | $I_E = 10\text{mA}$   | 5                                    | 0.800                | V                    |
| $V_{BE}$ Temperature Coefficient                                | $\Delta V_{BE}/\Delta T$ | $V_{CE} = 3\text{V}, I_C = 1\text{mA}$   |                       | 6                                    | -1.9                 | mV/ $^\circ\text{C}$ |
| Collector-to-Emitter Saturation Voltage                         | $V_{CEsat}$              | $I_B = 1\text{mA}, I_C = 10\text{mA}$  |                       | -                                    | 0.23                 | V                    |
| Noise Figure (low frequency)                                    | NF                       | $f = 1\text{kHz}, V_{CE} = 3\text{V}, I_C = 100\mu\text{A}, R_S = 1\text{k}\Omega$ |                       | -                                    | 3.25                 | dB                   |
| Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: |                          |  |                       |                                      |                      |                      |
| Forward Current-Transfer Ratio                                  | $h_{fe}$                 | $f = 1\text{kHz}, V_{CE} = 3\text{V}, I_C = 1\text{mA}$                            |                       | 7                                    | 100                  | -                    |
| Short-Circuit Input Impedance                                   | $h_{ie}$                 |  |                       | 7                                    | 3.5                  | k $\Omega$           |
| Open-Circuit Output Impedance                                   | $h_{oe}$                 |  |                       | 7                                    | 15.6                 | $\mu\text{mho}$      |
| Open-Circuit Reverse-Voltage Transfer Ratio                     | $h_{re}$                 |  |                       | 7                                    | $1.8 \times 10^{-4}$ | -                    |
| Admittance Characteristics:                                     |                          |  |                       |                                      |                      |                      |
| Forward Transfer Admittance                                     | $Y_{fe}$                 | $f = 1\text{MHz}, V_{CE} = 3\text{V}, I_C = 1\text{mA}$                            |                       | 8                                    | $31 - j1.5$          | mmho                 |
| Input Admittance  | $Y_{ie}$                 |  |                       | 9                                    | $0.3 + j0.04$        | mmho                 |
| Output Admittance   | $Y_{oe}$                 |  |                       | 10                                   | $0.001 + j0.03$      | mmho                 |
| Reverse Transfer Admittance                                     | $Y_{re}$                 |  |                       | 11                                   | See Curve            | -                    |
| Gain-Bandwidth Product  | $f_T$                    | $V_{CE} = 3\text{V}, I_C = 3\text{mA}$   |                       | 12                                   | 550                  | MHz                  |
| Emitter-to-Base Capacitance                                     | $C_{EBO}$                | $V_{EB} = 3\text{V}, I_E = 0$  |                       | -                                    | 0.6                  | pF                   |
| Collector-to-Base Capacitance                                   | $C_{CBO}$                | $V_{CB} = 3\text{V}, I_C = 0$  |                       | -                                    | 0.58                 | pF                   |
| Collector-to-Substrate Capacitance                              | $C_{CIO}$                | $V_{CI} = 3\text{V}, I_C = 0$  |                       | -                                    | 2.8                  | pF                   |

# CA3086

## TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

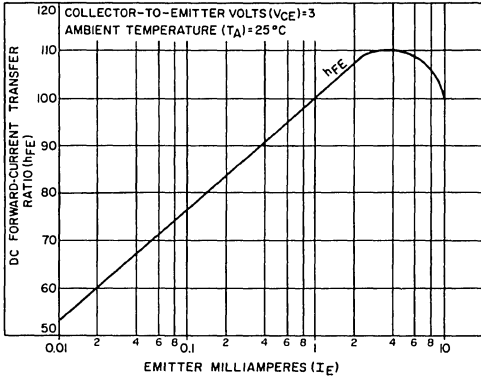


Fig.4 -  $h_{FE}$  vs  $I_E$

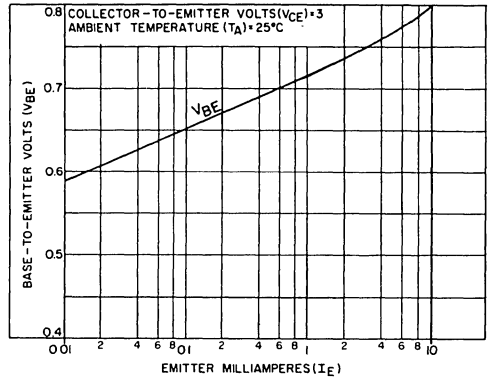


Fig.5 -  $V_{BE}$  vs  $I_E$

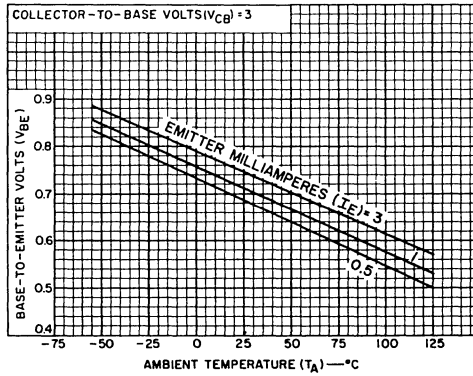


Fig.6 -  $V_{BE}$  vs  $T_A$

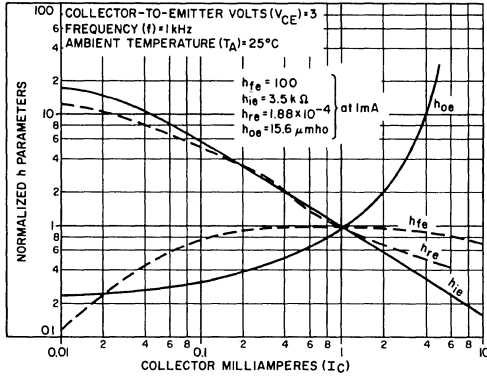


Fig. 7 - Normalized  $h_{fe}$ ,  $h_{ie}$ ,  $h_{oe}$ ,  $h_{re}$  vs  $I_C$ .

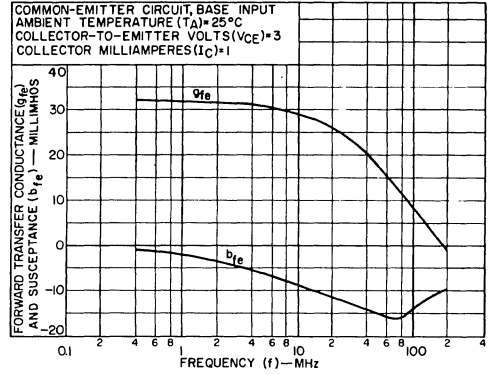


Fig. 8 -  $y_{fe}$  vs  $f$ .

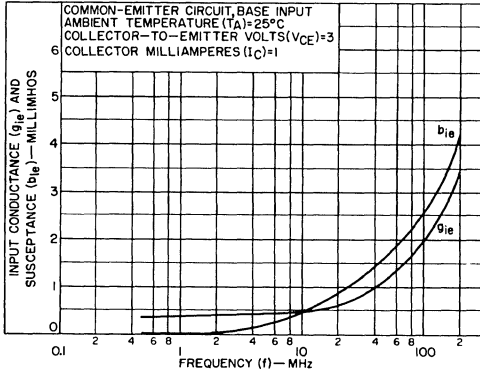


Fig. 9 -  $y_{ie}$  vs  $f$ .

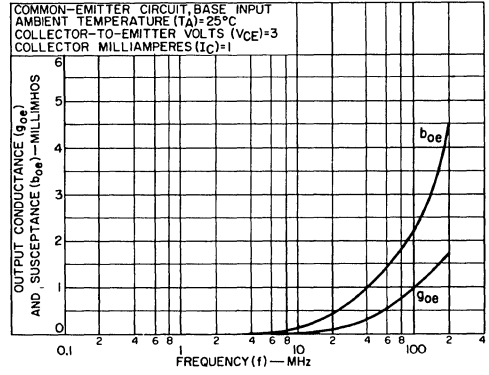


Fig. 10 -  $y_{oe}$  vs  $f$ .

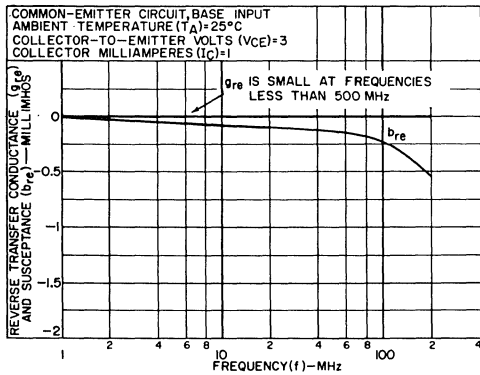


Fig. 11 -  $y_{re}$  vs  $f$ .

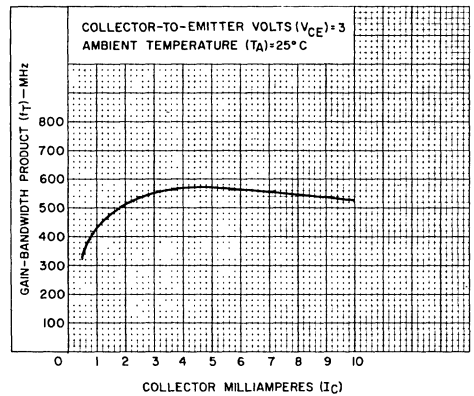


Fig. 12 -  $f_T$  vs  $I_C$ .

August 1991

N-P-N/P-N-P Transistor Arrays

### Applications

- Five-Independent Transistors
  - ▶ Three N-P-N and
  - ▶ Two P-N-P
- Differential Amplifiers
- DC Amplifiers
- Sense Amplifiers
- Level Shifters
- Timers
- Lamp and Relay Drivers
- Thyristor Firing Circuits
- Temperature-Compensated Amplifiers
- Operational Amplifiers

### Description

The CA3096C, CA3096, and CA3096A are general purpose high-voltage silicon transistor arrays. Each array consists of five independent transistors (two p-n-p and three n-p-n types) on a common substrate, which has a separate connection. Independent connections for each transistor permit maximum flexibility in circuit design.

Types CA3096A, CA3096, and CA3096C are identical, except that the CA3096A specifications include parameter matching and greater stringency in  $I_{CBO}$ ,  $I_{CEO}$ , and  $V_{CE(SAT)}$ . The CA3096C is a relaxed version of the CA3096.

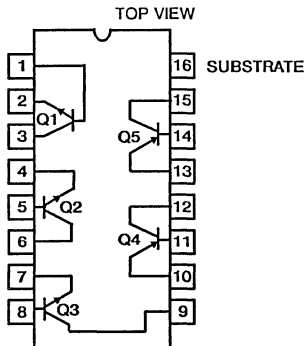
The CA3096C, CA3096, and CA3096A are supplied in 16-lead dual-in-line plastic packages (E-suffix), and in 16-lead Small Outline packages (M suffix). The CA3096 is also available in chip form (H suffix).

### CA3096A, CA3096, CA3096C Essential Differences

| CHARACTERISTIC           | CA3096A | CA3096  | CA3096C |
|--------------------------|---------|---------|---------|
| $V_{(BR)CEO}$ (V) Min.   | n-p-n   | 35      | 35      |
|                          | p-n-p   | -40     | -40     |
| $V_{(BR)CBO}$ (V) Min.   | n-p-n   | 45      | 45      |
|                          | p-n-p   | -40     | -40     |
| $h_{FE}$ @ 1 mA          | n-p-n   | 150-500 | 150-500 |
|                          | p-n-p   | 20-200  | 20-200  |
| $h_{FE}$ @ 100 $\mu$ A   | n-p-n   | 40-250  | 40-250  |
|                          | p-n-p   | 40-250  | 30-300  |
| $I_{CBO}$ (nA) Max.      | n-p-n   | 40      | 100     |
|                          | p-n-p   | -40     | -100    |
| $I_{CEO}$ (nA) Max.      | n-p-n   | 100     | 1000    |
|                          | p-n-p   | -100    | -1000   |
| $V_{CE(SAT)}$ (V) Max.   | n-p-n   | 0.5     | 0.7     |
| $ V_{IO} $ (mV) Max.     | n-p-n   | 5       | -       |
|                          | p-n-p   | 5       | -       |
| $I_{IO}$ ( $\mu$ A) Max. | n-p-n   | 0.6     | -       |
|                          | p-n-p   | 0.25    | -       |

### Pinout

CA3096, CA3096A, CA3096C  
16 PIN PACKAGES



### Schematic Diagram

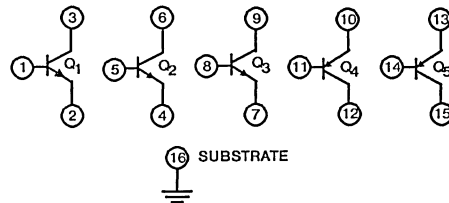


FIGURE 1.

# CA3096, CA3096A, CA3096C

## MAXIMUM RATINGS, Absolute-Maximum Values:

|  | EACH<br>N-P-N | EACH<br>P-N-P |                      |
|--|---------------|---------------|----------------------|
| COLLECTOR-TO-EMITTER VOLTAGE, $V_{CE0}$ :              |               |               |                      |
| CA3096A, CA3096  | 35            | -40           | V                    |
| CA3096C  | 24            | -24           | V                    |
| COLLECTOR-TO-BASE VOLTAGE, $V_{CBO}$ :                 |               |               |                      |
| CA3096A, CA3096  | 45            | -40           | V                    |
| CA3096C  | 30            | -24           | V                    |
| COLLECTOR-TO-SUBSTRATE VOLTAGE, $V_{C10}$ :            |               |               |                      |
| CA3096A, CA3096  | 45            | -             | V                    |
| CA3096C  | 30            | -             | V                    |
| EMITTER-TO-SUBSTRATE VOLTAGE, $V_{E10}$ :              |               |               |                      |
| CA3096A, CA3096  | -             | -40           | V                    |
| CA3096C  | -             | -24           | V                    |
| EMITTER-TO-BASE VOLTAGE, $V_{EBO}$ :                   |               |               |                      |
| CA3096A, CA3096  | 6             | -40           | V                    |
| CA3096C  | 6             | -24           | V                    |
| COLLECTOR CURRENT, $I_C$ (All Types)                   | 50            | -10           | mA                   |
| POWER DISSIPATION, $P_D$ :                             |               |               |                      |
| Up to $T_A = 55^\circ\text{C}$ :                       |               |               |                      |
| Device (Total)   | 750           |               | mW                   |
| Each Transistor  | 200           |               | mW                   |
| Above $T_A = 55^\circ\text{C}$ derate linearly at      | 6.67          |               | mW/ $^\circ\text{C}$ |
| AMBIENT-TEMPERATURE RANGE, $T_A$ :                     |               |               |                      |
| Operating  |               | -55 to +125   | $^\circ\text{C}$     |
| Storage  |               | -65 to +150   | $^\circ\text{C}$     |
| LEAD TEMPERATURE (DURING SOLDERING):                   |               |               |                      |
| At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79$ mm) |               |               |                      |
| from case for 10 s max.                                |               |               | 265                  |

## STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$

For Equipment Design

| CHARACTERISTIC                         | TEST CONDITIONS                                 | LIMITS  |       |      |        |       |      |         |       |      | UNITS                |
|--|---|---------|-------|------|--------|-------|------|---------|-------|------|----------------------|
|  |   | CA3096A |       |      | CA3096 |       |      | CA3096C |       |      |                      |
|  |   | Min.    | Typ.  | Max. | Min.   | Typ.  | Max. | Min.    | Typ.  | Max. |                      |
| For Each n-p-n Transistor              |   |         |       |      |        |       |      |         |       |      |                      |
| $I_{CBO}$                              | $V_{CB} = 10\text{ V}$ ,<br>$I_E = 0$           | -       | 0.001 | 40   | -      | 0.001 | 100  | -       | 0.001 | 100  | nA                   |
| $I_{CEO}$                              | $V_{CE} = 10\text{ V}$ ,<br>$I_B = 0$           | -       | 0.006 | 100  | -      | 0.006 | 1000 | -       | 0.006 | 1000 | nA                   |
| $V_{(BR)CEO}$                          | $I_C = 1\text{ mA}$ ,<br>$I_B = 0$              | 35      | 50    | -    | 35     | 50    | -    | 24      | 35    | -    | V                    |
| $V_{(BR)CBO}$                          | $I_C = 10\ \mu\text{A}$ ,<br>$I_E = 0$          | 45      | 100   | -    | 45     | 100   | -    | 30      | 80    | -    | V                    |
| $V_{(BR)C10}$                          | $I_{C1} = 10\ \mu\text{A}$ ,<br>$I_B = I_E = 0$ | 45      | 100   | -    | 45     | 100   | -    | 30      | 80    | -    | V                    |
| $V_{(BR)EBO}$                          | $I_E = 10\ \mu\text{A}$ ,<br>$I_C = 0$          | 6       | 8     | -    | 6      | 8     | -    | 6       | 8     | -    | V                    |
| $V_Z$                                  | $I_Z = 10\ \mu\text{A}$                         | 6       | 7.9   | 9.8  | 6      | 7.9   | 9.8  | 6       | 7.9   | 9.8  | V                    |
| $V_{CE(SAT)}$                          | $I_C = 10\text{ mA}$ ,<br>$I_B = 1\text{ mA}$   | -       | 0.24  | 0.5  | -      | 0.24  | 0.7  | -       | 0.24  | 0.7  | V                    |
| $V_{BE(\text{Note 1})}$                | $I_C = 1\text{ mA}$ ,                           | 0.6     | 0.69  | 0.78 | 0.6    | 0.69  | 0.78 | 0.6     | 0.69  | 0.78 | V                    |
| $h_{FE(\text{Note 1})}$                | $V_{CE} = 5\text{ V}$                           | 150     | 390   | 500  | 150    | 390   | 500  | 100     | 390   | 670  |                      |
| $ \Delta V_{RF}/\Delta T $<br>(Note 1) | $I_C = 1\text{ mA}$ ,<br>$V_{CE} = 5\text{ V}$  | -       | 1.9   | -    | -      | 1.9   | -    | -       | 1.9   | -    | mV/ $^\circ\text{C}$ |

**CA3096, CA3096A, CA3096C**

**STATIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$  (Cont'd)**  
For Equipment Design

| CHARACTERISTIC                         | TEST CONDITIONS  | LIMITS  |        |      |        |       |       |         |       |       | UNITS                      |
|--|--|---------|--------|------|--------|-------|-------|---------|-------|-------|----------------------------|
|  |  | CA3096A |        |      | CA3096 |       |       | CA3096C |       |       |                            |
|  |  | Min.    | Typ.   | Max. | Min.   | Typ.  | Max.  | Min.    | Typ.  | Max.  |                            |
| For Each p-n-p Transistor              |  |         |        |      |        |       |       |         |       |       |                            |
| $I_{CBO}$                              | $V_{CB} = -10\text{ V}$ ,<br>$I_E = 0$                 | -       | -0.006 | -40  | -      | -0.06 | -100  | -       | -0.06 | -100  | nA                         |
| $I_{CEO}$                              | $V_{CE} = -10\text{ V}$ ,<br>$I_B = 0$                 | -       | -0.12  | -100 | -      | -0.12 | -1000 | -       | -0.12 | -1000 | nA                         |
| $V_{(BR)CEO}$                          | $I_C = -100\ \mu\text{A}$ ,<br>$I_B = 0$               | -40     | -75    | -    | -40    | -75   | -     | -24     | -30   | -     | V                          |
| $V_{(BR)CBO}$                          | $I_C = -10\ \mu\text{A}$ ,<br>$I_E = 0$                | -40     | -80    | -    | -40    | -80   | -     | -24     | -60   | -     | V                          |
| $V_{(BR)EBO}$                          | $I_E = -10\ \mu\text{A}$ ,<br>$I_C = 0$                | -40     | -100   | -    | -40    | -100  | -     | -24     | -80   | -     | V                          |
| $V_{(BR)EIO}$                          | $ I_E  = 10\ \mu\text{A}$ ,<br>$I_B = I_C = 0$         | -40     | -100   | -    | -40    | -100  | -     | -24     | -80   | -     | V                          |
| $V_{CE(SAT)}$                          | $I_C = -1\ \text{mA}$ ,<br>$I_B = -100\ \mu\text{A}$   | -       | -0.16  | -0.4 | -      | -0.16 | -0.4  | -       | -0.16 | -0.4  | V                          |
| $V_{BE}$<br>(Note 1)                   | $I_C = -100\ \mu\text{A}$ ,<br>$V_{CE} = -5\ \text{V}$ | -0.5    | -0.6   | -0.7 | -0.5   | -0.6  | -0.7  | -0.5    | -0.6  | -0.7  | V                          |
| $h_{FE}$<br>(Note 1)                   | $I_C = -100\ \mu\text{A}$ ,<br>$V_{CE} = -5\ \text{V}$ | 40      | 85     | 250  | 40     | 85    | 250   | 30      | 85    | 300   |                            |
|  | $I_C = -1\ \text{mA}$ ,<br>$V_{CE} = -5\ \text{V}$     | 20      | 47     | 200  | 20     | 47    | 200   | 15      | 47    | 200   |                            |
| $ \Delta V_{BE}/\Delta T $<br>(Note 1) | $I_C = -100\ \mu\text{A}$ ,<br>$V_{CE} = -5\ \text{V}$ | -       | 2.2    | -    | -      | 2.2   | -     | -       | 2.2   | -     | $\text{mV}/^\circ\text{C}$ |

$I_{CBO}$  Collector-Cutoff Current

$I_{CEO}$  Collector-Cutoff Current

$V_{(BR)CEO}$  Collector-to-Emitter Breakdown Voltage

$V_{(BR)CBO}$  Collector-to-Base Breakdown Voltage

$V_{(BR)CIO}$  Collector-to-Substrate Breakdown Voltage

$V_{(BR)EBO}$  Emitter-to-Base Breakdown Voltage

$V_Z$  Emitter-to-Base Zener Voltage

$V_{CE(SAT)}$  Collector-to-Emitter Saturation Voltage

$V_{BE}$  Base-to-Emitter Voltage

$h_{FE}$  DC Forward-Current Transfer Ratio

$|\Delta V_{BE}/\Delta T|$  Magnitude of Temperature Coefficient: (for each transistor)

**NOTES:**

1. Actual forcing current is via the emitter for this test.

**7**

ARRAYS



# CA3096, CA3096A, CA3096C

**STATIC ELECTRICAL CHARACTERISTICS at  $T_A = 25^\circ\text{C}$  (CA3096A Only)**  
For Equipment Design

| CHARACTERISTIC  | TEST CONDITIONS  | LIMITS  |      |      | UNITS                        |
|---|--|---------|------|------|------------------------------|
|   |  | CA3096A |      |      |                              |
|   |  | Min.    | Typ. | Max. |                              |
| <b>For Transistors Q1 and Q2 (as a Differential Amplifier)</b>                            |  |         |      |      |                              |
| Absolute Input Offset Voltage, $ V_{IO} $   | $V_{CE} = 5\text{ V}, I_C = 1\text{ mA}$                   | -       | 0.3  | 5    | mV                           |
| Absolute Input Offset Current, $ I_{IO} $   |  | -       | 0.07 | 0.6  | $\mu\text{A}$                |
| Absolute Input Offset Voltage Temperature Coefficient, $\frac{ \Delta V_{IO} }{\Delta T}$ |  | -       | 1.1  | -    | $\mu\text{V}/^\circ\text{C}$ |
| <b>For Transistors Q4 and Q5 (As a Differential Amplifier)</b>                            |  |         |      |      |                              |
| Absolute Input Offset Voltage, $ V_{IO} $   | $V_{CE} = -5\text{ V}, I_C = -100\mu\text{A}$<br>$R_S = 0$ | -       | 0.15 | 5    | mV                           |
| Absolute Input Offset Current, $ I_{IO} $   |  | -       | 2    | 250  | nA                           |
| Absolute Input Offset Voltage Temperature Coefficient, $\frac{ \Delta V_{IO} }{\Delta T}$ |  | -       | 0.54 | -    | $\mu\text{V}/^\circ\text{C}$ |

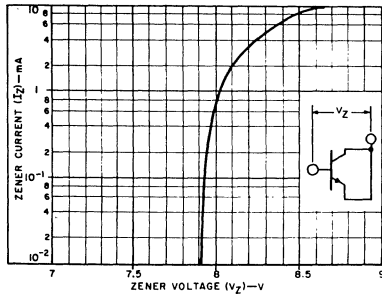


Fig. 1 – Base-to-emitter zener characteristic (n-p-n).

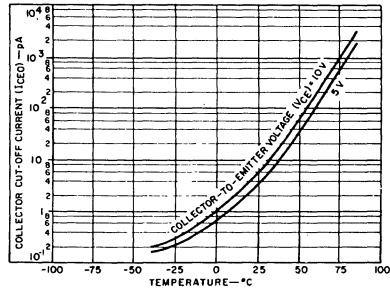


Fig. 2 – Collector cut-off current ( $I_{CEO}$ ) as a function of temperature (n-p-n).

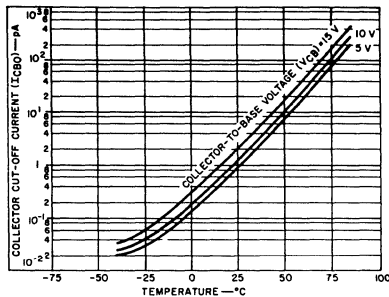


Fig. 3 – Collector cut-off current ( $I_{CBO}$ ) as a function of temperature (n-p-n).

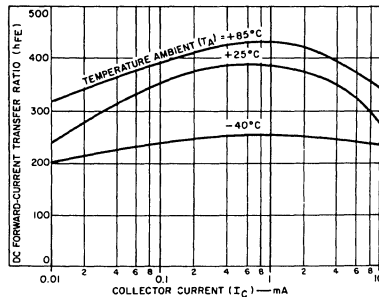


Fig. 4 – Transistor (n-p-n)  $h_{FE}$  as a function of collector current.

# CA3096, CA3096A, CA3096C

## DYNAMIC

### ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$

Typical Values Intended Only for Design Guidance

| CHARACTERISTICS   | TEST CONDITIONS  | TYPICAL VALUES | UNITS            |
|---|--|----------------|------------------|
| <b>For Each n-p-n Transistor</b>                            |  |                |                  |
| Noise Figure (low frequency), NF                            | $f = 1\text{ kHz}, V_{CE} = 5\text{ V}, I_C = 1\text{ mA}, R_S = 1\text{ k}\Omega$ | 2.2            | dB               |
| Low-Frequency Input Resistance, $R_i$                       | $f = 1.0\text{ kHz}, V_{CE} = 5\text{ V}, I_C = 1\text{ mA}$                       | 10             | $\text{k}\Omega$ |
| Low-Frequency Output Resistance, $R_o$                      |  | 80             | $\text{k}\Omega$ |
| <b>Admittance Characteristics:</b>                          |  |                |                  |
| Forward Transfer Admittance, $\frac{g_{fe}}{y_{fe} b_{fe}}$ | $f = 1\text{ MHz}, V_{CE} = 5\text{ V}, I_C = 1\text{ mA}$                         | 7.5            | mmho             |
|   |  | -j13           |                  |
| Input Admittance, $\frac{g_{ie}}{y_{ie} b_{ie}}$            |  | 2.2            | mmho             |
|   |  | j3.1           |                  |
| Output Admittance, $\frac{g_{oe}}{y_{oe} b_{oe}}$           | 0.76   | mmho           |                  |
|   | j2.4   |                |                  |
| Gain-Bandwidth Product, $f_T$                               | $V_{CE} = 5\text{ V}, I_C = 1.0\text{ mA}$   | 280            | MHz              |
|   | $V_{CE} = 5\text{ V}, I_C = 5\text{ mA}$   | 335            |                  |
| Emitter-to-Base Capacitance, $C_{EB}$                       | $V_{EB} = 3\text{ V}$  | 0.75           | $\mu\text{F}$    |
| Collector-to-Base Capacitance, $C_{CB}$                     | $V_{CB} = 3\text{ V}$  | 0.46           | $\mu\text{F}$    |
| Collector-to-Substrate Capacitance, $C_{CI}$                | $V_{CI} = 3\text{ V}$  | 3.2            | $\mu\text{F}$    |
| <b>For Each p-n-p Transistor</b>                            |  |                |                  |
| Noise Figure (low frequency), NF                            | $f = 1\text{ kHz}, I_C = 100\text{ }\mu\text{A}, R_S = 1\text{ k}\Omega$           | 3              | dB               |
| Low-Frequency Input Resistance, $R_i$                       | $f = 1\text{ kHz}, V_{CE} = 5\text{ V}, I_C = 100\text{ }\mu\text{A}$              | 27             | $\text{k}\Omega$ |
| Low-Frequency Output Resistance, $R_o$                      |  | 680            | $\text{k}\Omega$ |
| Gain-Bandwidth Product, $f_T$                               | $V_{CE} = 5\text{ V}, I_C = 100\text{ }\mu\text{A}$                                | 6.8            | MHz              |
| Emitter-to-Base Capacitance, $C_{EB}$                       | $V_{EB} = -3\text{ V}$   | 0.85           | $\mu\text{F}$    |
| Collector-to-Base Capacitance, $C_{CB}$                     | $V_{CB} = -3\text{ V}$   | 2.25           | $\mu\text{F}$    |
| Base-to-Substrate Capacitance, $C_{BI}$                     | $V_{BI} = 3\text{ V}$  | 3.05           | $\mu\text{F}$    |

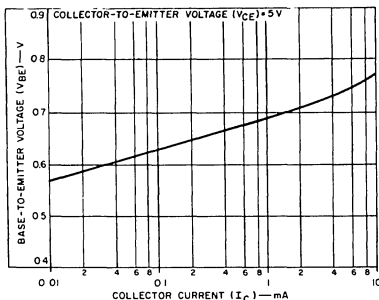


Fig. 5 -  $V_{BE}$  (n-p-n) as a function of collector current.

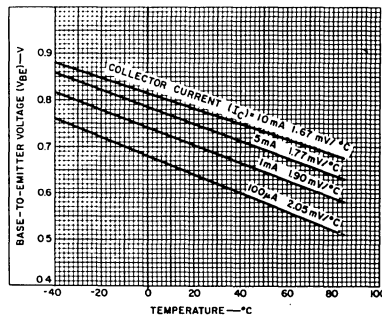


Fig. 6 -  $V_{BE}$  (n-p-n) as a function of temperature.

# CA3096, CA3096A, CA3096C

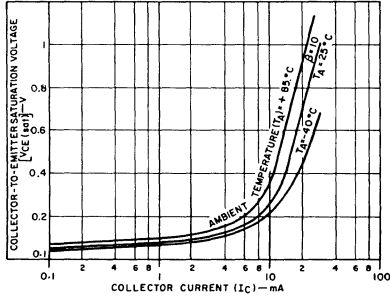


Fig. 7 —  $V_{CE(SAT)}$  (n-p-n) as a function of collector current.

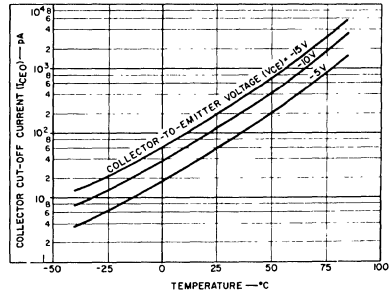


Fig. 8 — Collector cut-off current ( $I_{CEO}$ ) as a function of temperature (p-n-p).

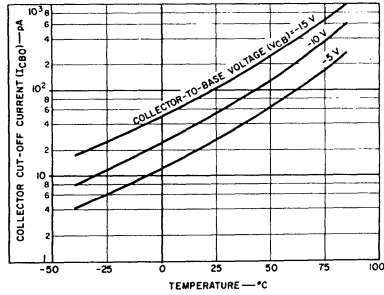


Fig. 9 — Collector cut-off current ( $I_{CBO}$ ) as a function of temperature (p-n-p).

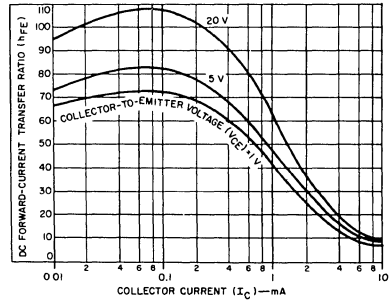


Fig. 10 — Transistor (p-n-p)  $h_{FE}$  as a function of collector current.

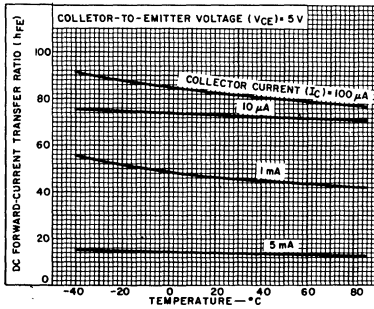


Fig. 11 — Transistor (p-n-p)  $h_{FE}$  as a function of temperature.

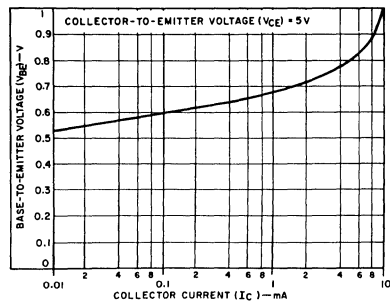


Fig. 12 —  $V_{BE}$  (p-n-p) as a function of collector current.

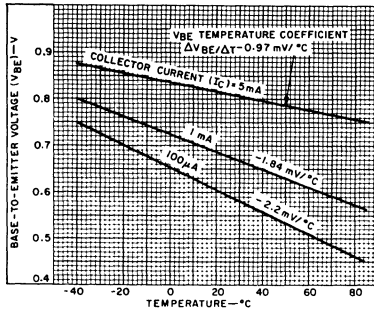


Fig. 13 —  $V_{BE}$  (p-n-p) as a function of temperature.

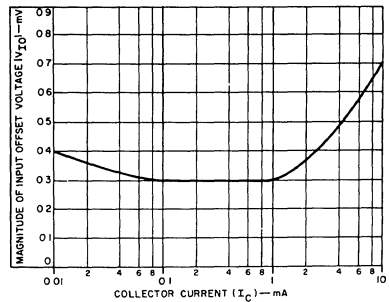


Fig. 14 — Magnitude of input offset voltage  $|V_{IO}|$  as a function of collector current for n-p-n transistor  $Q_1-Q_2$ .

CA3096, CA3096A, CA3096C

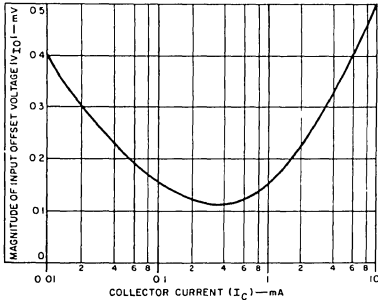


Fig. 15 - Magnitude of input offset voltage  $|V_{IO}|$  as a function of collector current for p-n-p transistor  $Q_4-Q_5$

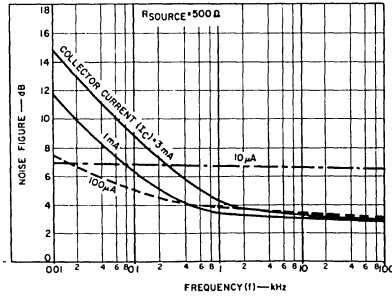


Fig. 16 - Noise figure as a function of frequency for n-p-n transistors.

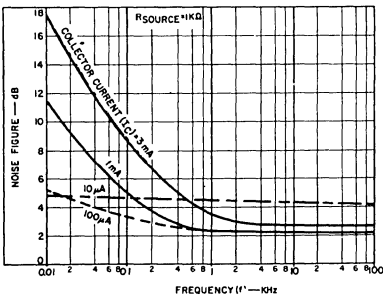


Fig. 17 - Noise figure as a function of frequency for n-p-n transistors.

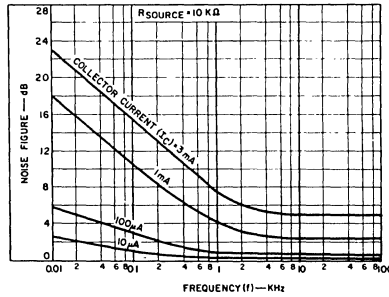


Fig. 18 - Noise as a function of frequency for n-p-n transistors.

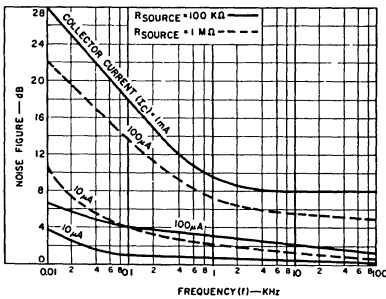


Fig. 19 - Noise figure as a function of frequency for n-p-n transistors.

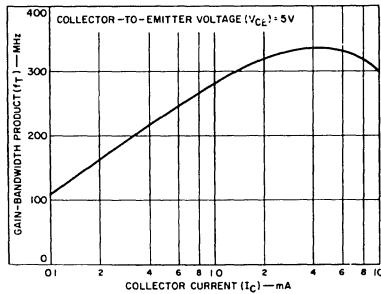


Fig. 20 - Gain-bandwidth product as a function of collector current (n-p-n).

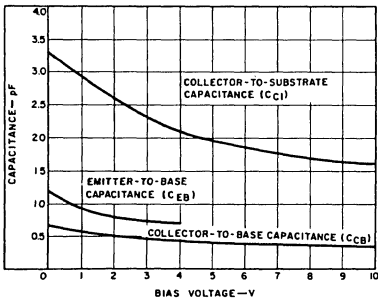


Fig. 21 - Capacitance as a function of bias voltage (n-p-n).

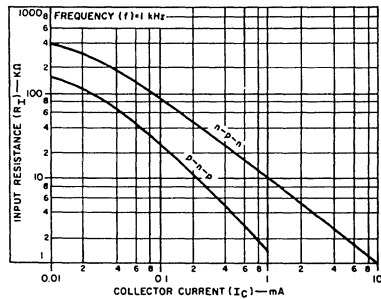


Fig. 22 - Input resistance as a function of collector current.

CA3096, CA3096A, CA3096C

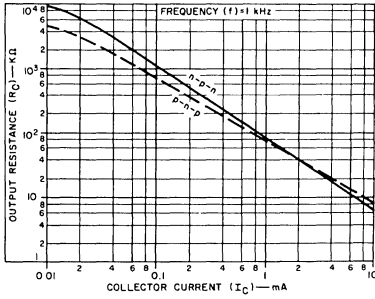


Fig. 23 - Output resistance as a function of collector current.

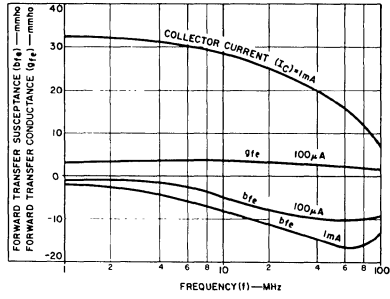


Fig. 24 - Forward transconductance as a function of frequency.

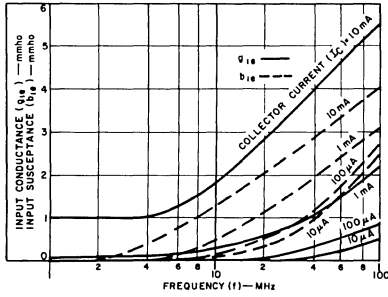


Fig. 25 - Input admittance as a function of frequency.

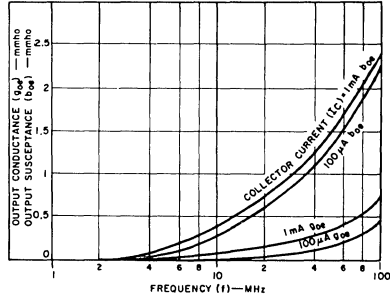


Fig. 26 - Output admittance as a function of frequency.

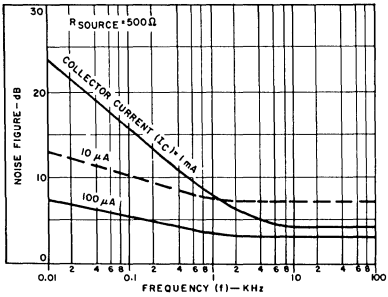


Fig. 27 - Noise figure as a function of frequency (p-n-p).

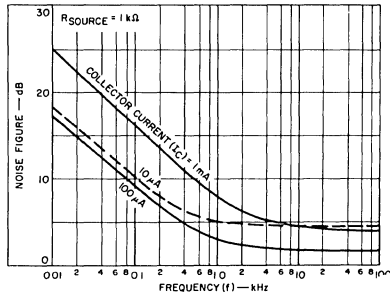


Fig. 28 - Noise figure as a function of frequency (p-n-p).

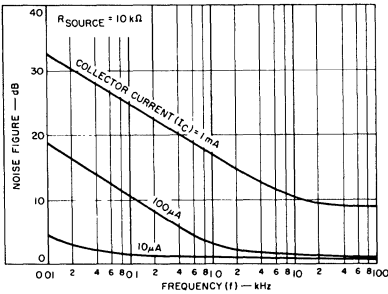


Fig. 29 - Noise figure as a function of frequency (p-n-p).

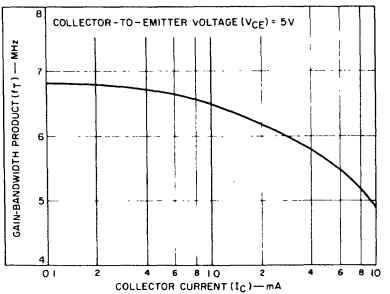


Fig. 30 - Gain-bandwidth product as a function of collector current (p-n-p).

# CA3096, CA3096A, CA3096C

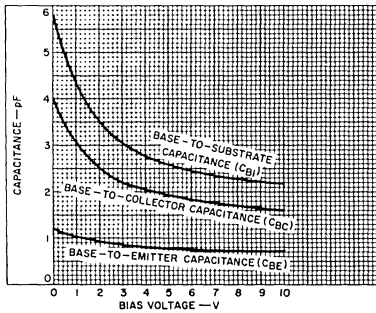


Fig. 31 - Capacitance as a function of bias voltage (p-n-p).

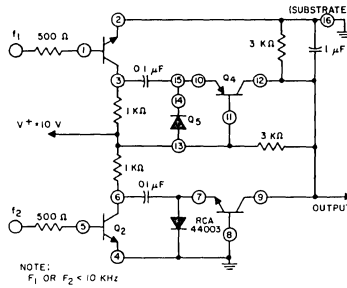


Fig. 32 - Frequency comparator using CA3096

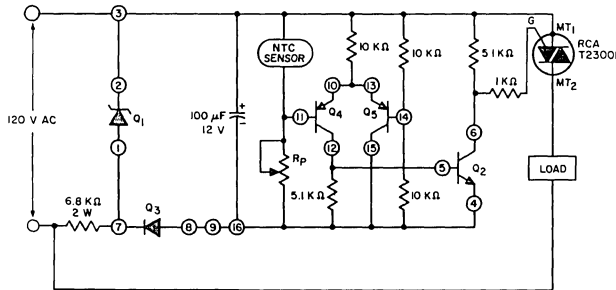


Fig. 33 - Line-operated level switch using CA3096A or CA3096

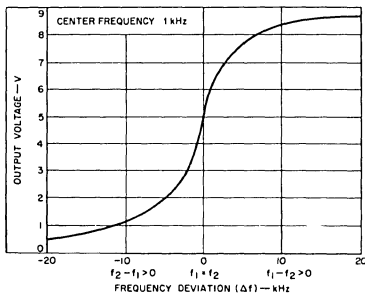


Fig. 34 - Frequency comparator characteristics.

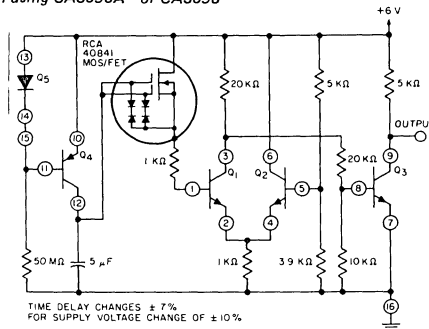


Fig. 35 - One-minute timer using CA3096A and a MOS/FET.

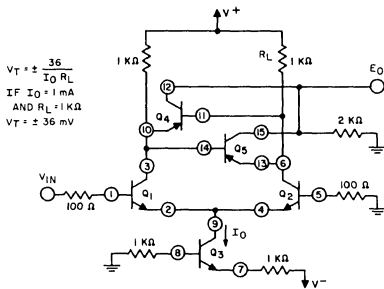
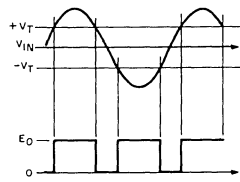


Fig. 36 - CA3096A small-signal zero-voltage detector having noise immunity.



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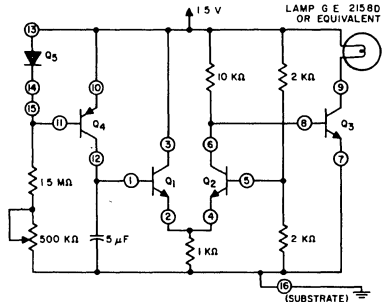


Fig. 37 — Ten-second timer operated from 1.5-volt supply using CA3096

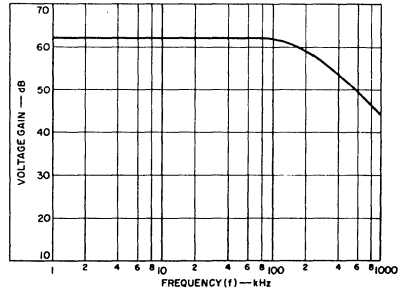


Fig. 38 — Gain-frequency characteristics.

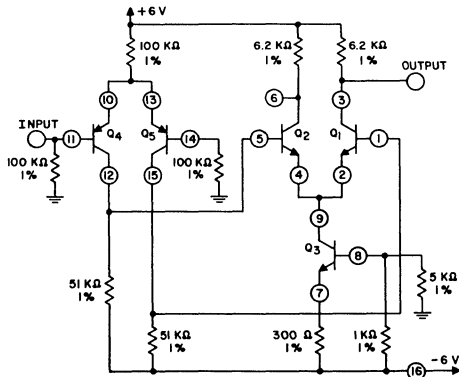
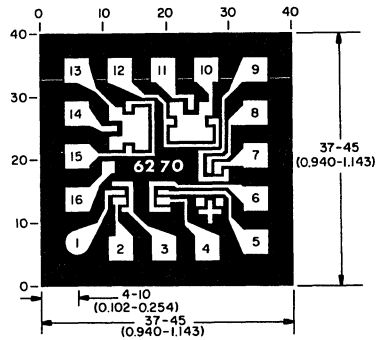


Fig. 39 — Cascade of differential amplifiers using CA3096A

### Features:

1. Can be operated with either dual supply or single supply.
2. Wide-input common-mode range +5 V to -5 V.
3. Low bias current:  $< 1 \mu\text{A}$ .



### CA3096H

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are  $57^\circ$  instead of  $90^\circ$  with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

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### Features

- Gain-Bandwidth Product ( $f_T$ ) ..... >1GHz
- Power Gain ..... 30dB (Typ) at 100MHz
- Noise Figure ..... 3.5dB (Typ) at 100MHz
- Five Independent Transistors on a Common Substrate

### Applications

- VHF Amplifiers
- Multifunction Combinations - RF/Mixer/Oscillator
- Sense Amplifiers
- Synchronous Detectors
- VHF Mixers
- IF Converter
- IF Amplifiers
- Synthesizers
- Cascade Amplifiers

### Description

The CA3127\* consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Each of the completely isolated transistors exhibits low  $1/f$  noise and a value of  $f_T$  in excess of 1GHz, making the CA3127 useful from DC to 500MHz. Access is provided to each of the terminals for the individual transistors and a separate substrate connection has been provided for maximum application flexibility. The monolithic construction of the CA3127 provides close electrical and thermal matching of the five transistors.

The CA3127 is supplied in the 16-lead Small Outline package (M suffix), 16-lead dual-in-line plastic package (E suffix), 16-lead dual-in-line frit-seal ceramic package (F suffix), and is also available in clip form (H suffix). It operates over the full military temperature range of  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .

\* Formerly RCA Dev. No. TA6206.

### Schematic Diagram

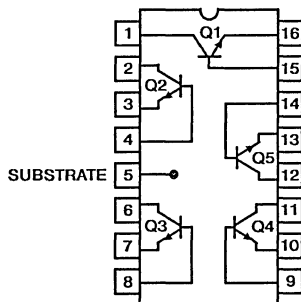


FIGURE 1.

### MAXIMUM RATINGS, Absolute-Maximum Values:

|   |  |
|---|--|
| <b>POWER DISSIPATION, <math>P_D</math>:</b>   |  |
| Any one transistor .....  | 85 mW  |
| Total Package:  |  |
| For $T_A$ up to $75^\circ\text{C}$ .....  | 425 mW                                       |
| For $T_A > 75^\circ\text{C}$ .....  | Derate Linearly at 6.67 mW/ $^\circ\text{C}$ |
| <b>AMBIENT TEMPERATURE RANGE:</b>   |  |
| Operating .....   | $-55^\circ\text{C}$ to $+125^\circ\text{C}$  |
| Storage .....   | $-65^\circ\text{C}$ to $+150^\circ\text{C}$  |
| <b>LEAD TEMPERATURE (DURING SOLDERING):</b>   |  |
| At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79$ mm) from case for 10 seconds max. .... | $+265^\circ\text{C}$                         |
| The following ratings apply for each transistor in the device:                            |  |
| COLLECTOR-TO-EMITTER VOLTAGE, $V_{CE0}$ .....   | 15 V   |
| COLLECTOR-TO-BASE VOLTAGE, $V_{CB0}$ .....  | 20 V   |
| COLLECTOR-TO-SUBSTRATE VOLTAGE, $V_{C10}^\dagger$ .....                                   | 20 V   |
| COLLECTOR CURRENT, $I_C$ .....  | 20 mA  |

$^\dagger$  The collector of each transistor of the CA3127 is isolated from the substrate by an integral diode. The substrate (terminal 5) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.



### CA3127

#### STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$

| CHARACTERISTICS                          | TEST CONDITIONS                             | LIMITS                 |      |      | UNITS         |   |
|--|---|------------------------|------|------|---------------|---|
|  |   | Min.                   | Typ. | Max. |               |   |
| <b>For Each Transistor:</b>              |   |                        |      |      |               |   |
| Collector-to-Base Breakdown Voltage      | $I_C = 10 \mu\text{A}, I_E = 0$             | 20                     | 32   | –    | V             |   |
| Collector-to-Emitter Breakdown Voltage   | $I_C = 1 \text{ mA}, I_B = 0$               | 15                     | 24   | –    | V             |   |
| Collector-to-Substrate Breakdown Voltage | $I_{C1} = 10 \mu\text{A}, I_B = 0, I_E = 0$ | 20                     | 60   | –    | V             |   |
| Emitter-to-Base Breakdown Voltage*       | $I_E = 10 \mu\text{A}, I_C = 0$             | 4                      | 5.7  | –    | V             |   |
| Collector-Cutoff-Current                 | $V_{CE} = 10 \text{ V}, I_B = 0$            | –                      | –    | 0.5  | $\mu\text{A}$ |   |
| Collector-Cutoff-Current                 | $V_{CB} = 10 \text{ V}, I_E = 0$            | –                      | –    | 40   | nA            |   |
| DC Forward-Current Transfer Ratio        | $V_{CE} = 6 \text{ V}$                      | $I_C = 5 \text{ mA}$   | 35   | 88   | –             |   |
|  |   | $I_C = 1 \text{ mA}$   | 40   | 90   | –             |   |
|  |   | $I_C = 0.1 \text{ mA}$ | 35   | 85   | –             |   |
| Base-to-Emitter Voltage                  | $V_{CE} = 6 \text{ V}$                      | $I_C = 5 \text{ mA}$   | 0.71 | 0.81 | 0.91          | V |
|  |   | $I_C = 1 \text{ mA}$   | 0.66 | 0.76 | 0.86          |   |
|  |   | $I_C = 0.1 \text{ mA}$ | 0.60 | 0.70 | 0.80          |   |
| Collector-to-Emitter Saturation Voltage  | $I_C = 10 \text{ mA}, I_B = 1 \text{ mA}$   | –                      | 0.26 | 0.50 | V             |   |
| Magnitude of Difference in $V_{BE}$      | $Q_1 \& Q_2$ Matched                        | –                      | 0.5  | 5    | mV            |   |
| Magnitude of Difference in $I_B$         | $V_{CE} = 6 \text{ V}, I_C = 1 \text{ mA}$  | –                      | 0.2  | 3    | $\mu\text{A}$ |   |

\*When used as a zener for reference voltage, the device must not be subjected to more than 0.1 millijoule of energy from any possible capacitance or electrostatic discharge in order to prevent degradation of the junction. Maximum operating zener current should be less than 10 mA.

#### DYNAMIC CHARACTERISTICS at $T_A = 25^\circ\text{C}$

| CHARACTERISTICS                      | TEST CONDITIONS   | LIMITS |      |      | UNITS      |
|--------------------------------------|---|--------|------|------|------------|
|                                      |   | Min.   | Typ. | Max. |            |
| I/F Noise Figure                     | $f = 100 \text{ kHz}, R_S = 500 \Omega, I_C = 1 \text{ mA}$   | –      | 1.8  | –    | dB         |
| Gain-Bandwidth Product               | $V_{CE} = 6 \text{ V}, I_C = 5 \text{ mA}$  | –      | 1.15 | –    | GHz        |
| Collector-to-Base Capacitance        | $V_{CB} = 6 \text{ V}, f = 1 \text{ MHz}$   | –      | See  | –    | pF         |
| Collector-to-Substrate Capacitance   | $V_{C1} = 6 \text{ V}, f = 1 \text{ MHz}$   | –      | Fig. | –    | pF         |
| Emitter-to-Base Capacitance          | $V_{BE} = 4 \text{ V}, f = 1 \text{ MHz}$   | –      | 5    | –    | pF         |
| Voltage Gain                         | $V_{CE} = 6 \text{ V}, f = 10 \text{ MHz}$<br>$R_L = 1 \text{ k}\Omega, I_C = 1 \text{ mA}$             | –      | 28   | –    | dB         |
| Power Gain                           | Cascode Configuration<br>$f = 100 \text{ MHz}, V^+ = 12 \text{ V}$                                      | 27     | 30   | –    | dB         |
| Noise Figure                         | $I_C = 1 \text{ mA}$  | –      | 3.5  | –    | dB         |
| Input Resistance                     | Common-Emitter Configuration<br>$V_{CE} = 6 \text{ V}$<br>$I_C = 1 \text{ mA}$<br>$f = 200 \text{ MHz}$ | –      | 400  | –    | $\Omega$   |
| Output Resistance                    |   | –      | 4.6  | –    | k $\Omega$ |
| Input Capacitance                    |   | –      | 3.7  | –    | pF         |
| Output Capacitance                   |   | –      | 2    | –    | pF         |
| Magnitude of Forward Transadmittance |   | –      | 24   | –    | mmho       |

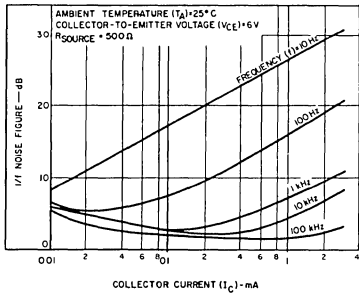


Fig. 2 - 1/f noise figure as a function of collector current at  $R_{SOURCE} = 500 \Omega$ .

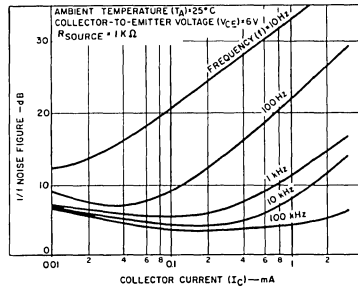


Fig. 3 - 1/f noise figure as a function of collector current at  $R_{SOURCE} = 1 k\Omega$ .

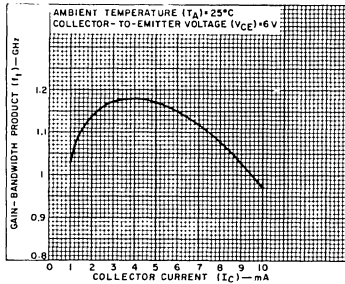


Fig. 4 - Gain-bandwidth product as a function of collector current.

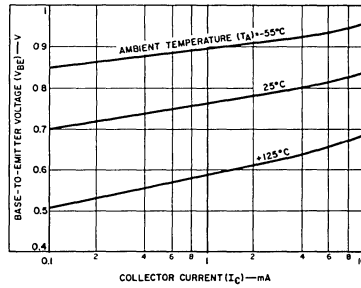


Fig. 5 - Base-to-emitter voltage as a function of collector current.

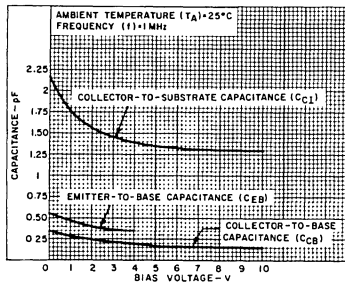


Fig. 6(a) - Capacitance as a function of bias voltage for  $Q_2$ .

| Transistor   | Capacitance (pF) |       |          |       |          |       |       |
|--------------|------------------|-------|----------|-------|----------|-------|-------|
|              | $C_{CB}$         |       | $C_{CE}$ |       | $C_{CB}$ |       |       |
| Bias Voltage | Pkg.             | Total | Pkg.     | Total | Pkg.     | Total |       |
| 01           | 0.025            | 0.190 | 0.090    | 0.125 | 0.365    | 0.610 | 0.475 |
| 02           | 0.015            | 0.170 | 0.225    | 0.265 | 0.130    | 0.360 | 0.085 |
| 03           | 0.040            | 0.200 | 0.215    | 0.240 | 0.360    | 0.625 | 0.210 |
| 04           | 0.040            | 0.190 | 0.225    | 0.270 | 0.365    | 0.610 | 0.085 |
| 05           | 0.010            | 0.165 | 0.095    | 0.115 | 0.140    | 0.355 | 0.090 |

Fig. 6(b) - Typical capacitance values at  $f = 1 \text{ MHz}$ . Three terminal measurement. Guard all terminals except those under test.

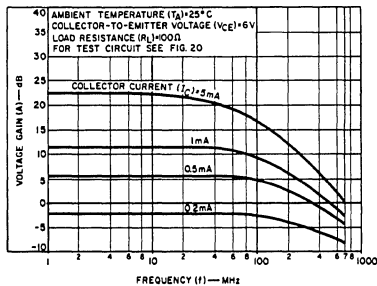


Fig. 7 - Voltage gain as a function of frequency at  $R_L = 100 \Omega$ .

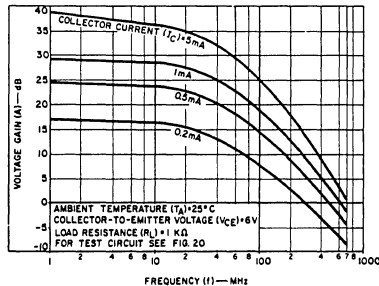


Fig. 8 - Voltage gain as a function of frequency at  $R_L = 1 k\Omega$ .

7  
ARRAYS

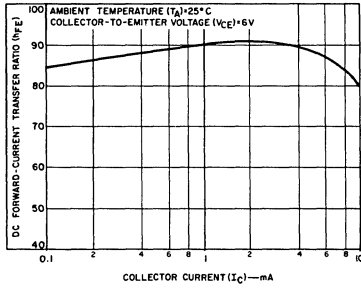


Fig. 9 - DC forward-current transfer ratio as a function of collector current.

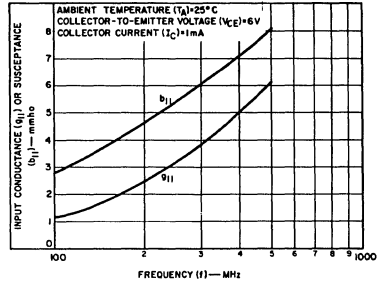


Fig. 10 - Input admittance ( $Y_{11}$ ) as a function of frequency.

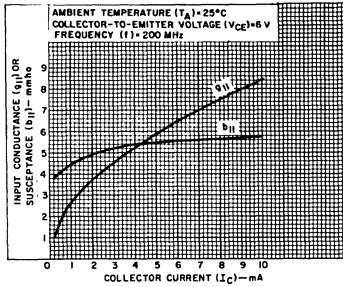


Fig. 11 - Input admittance ( $Y_{11}$ ) as a function of collector current.

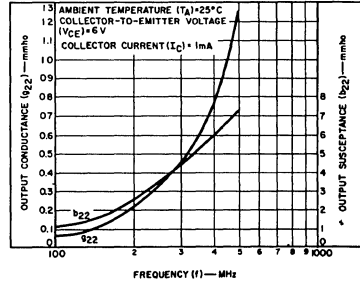


Fig. 12 - Output admittance ( $Y_{22}$ ) as a function of frequency.

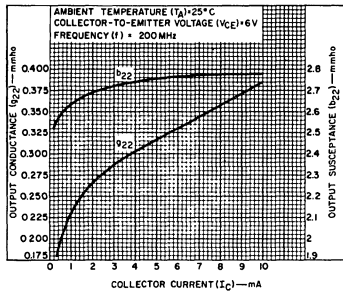


Fig. 13 - Output admittance ( $Y_{22}$ ) as a function of collector current.

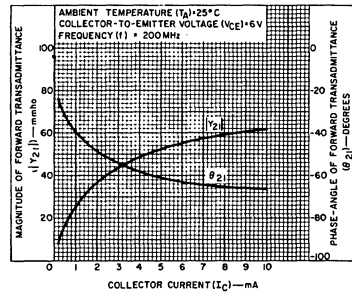


Fig. 14 - Forward transmittance ( $Y_{21}$ ) as a function of collector current.

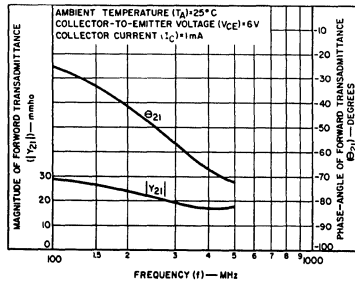


Fig. 15 - Forward transmittance ( $Y_{21}$ ) as a function of frequency.

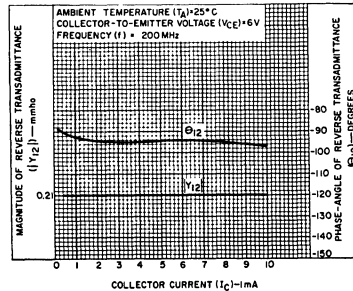


Fig. 16 - Reverse transmittance ( $Y_{12}$ ) as a function of collector current.

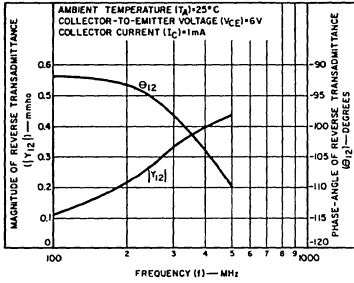


Fig. 17 - Reverse transmittance ( $Y_{12}$ ) as a function of frequency.

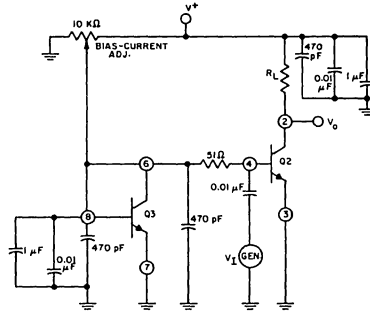


Fig. 18 - Voltage-gain test circuit using current-mirror biasing for  $Q_2$ .

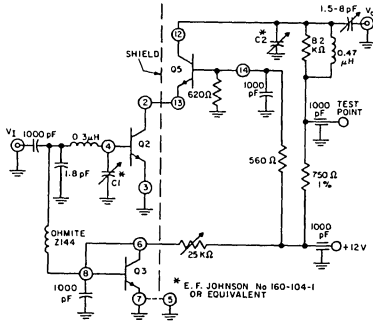


Fig. 19 - 100-MHz power-gain and noise-figure test circuit.

This circuit was chosen because it conveniently represents a close approximation in performance to a properly unilateralized single transistor of this type. The use of  $Q_3$  in a current-mirror configuration facilitates simplified biasing. The use of the cascode circuit in no way implies that the transistors cannot be used individually.

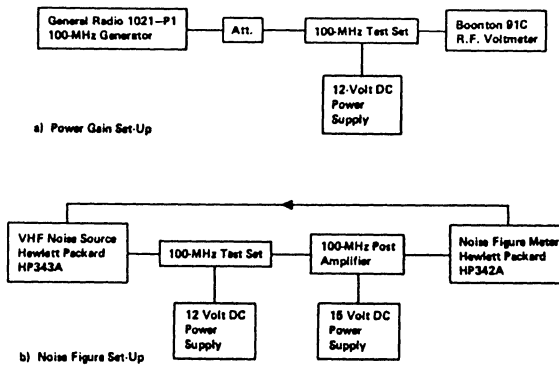


Fig. 20 - Block diagrams of power-gain and noise-figure test set-ups.

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## High-Voltage Diode Array For Commercial, Industrial & Military Applications

### Features

- Matched Monolithic Construction -  $V_F$  for Each Diode Pair Matched to Within 0.55mV (Typ) at  $I_F = 1\text{mA}$
- Low Diode Capacitance - 0.3pF (Typ) at  $V_R = 2\text{V}$
- High Diode-to-Substrate Breakdown Voltage... 30V (Min)
- Low Reverse (Leakage) Current ..... 100nA (Max)

### Applications

- Balanced Modulators of Demodulators
- Analog Switches
- High-Voltage Diode Gates
- Current Ratio Detectors

### Description

The CA3141E High Voltage Diode Array Consists of ten general purpose high reverse breakdown diodes. Six diodes are internally connected to form three common cathode diode pairs, and the remaining four diodes are internally connected to form two common anode diode pairs. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the CA3141 extremely useful for a wide variety of applications in communications and switching systems.

The CA3141 is supplied in the 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).

### Pinout

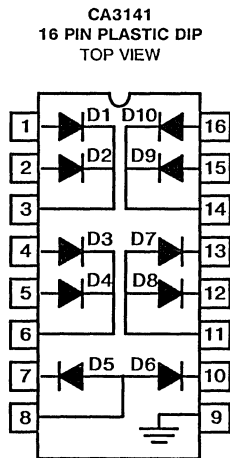


FIGURE 1.

### MAXIMUM RATINGS, Absolute-Maximum Values:

|  |                              |
|--|------------------------------|
| PEAK INVERSE VOLTAGE (PIV) .....   | 30V                          |
| PEAK DIODE-TO-SUBSTRATE VOLTAGE .....                                    | 30V                          |
| PEAK FORWARD SURGE CURRENT [ $I_F$ (SURGE)] .....                        | 100mA                        |
| DC FORWARD CURRENT ( $I_F$ ) .....                                       | 25mA                         |
| DISSIPATION:   |                              |
| Any one diode unit .....   | 50mW                         |
| Total Package:   |                              |
| Up to 55°C .....   | 650mW                        |
| For $T_A > 55^\circ\text{C}$ .....                                       | Derate linearly at 6.67mW/°C |
| AMBIENT TEMPERATURE RANGE:   |                              |
| Operating .....  | -55°C to +125°C              |
| Storage .....  | -65°C to +150°C              |
| LEAD TEMPERATURE (During Soldering):                                     |                              |
| At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... | +265°C                       |

# CA3141

## ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$

| CHARACTERISTIC   | TEST CONDITIONS                                    | LIMITS            |      |      | UNIT                       |   |
|--|--|-------------------|------|------|----------------------------|---|
|  |  | Min.              | Typ. | Max. |                            |   |
| DC Forward Voltage Drop, $V_F$   | $I_F$ (Anode)                                      | 100 $\mu\text{A}$ | —    | 0.7  | 0.9                        | V |
|  |  | 1 mA              | —    | 0.78 | 1                          |   |
|  |  | 10 mA             | —    | 0.93 | 1.2                        |   |
| DC Reverse Breakdown Voltage, $V_{(BR)R}$                                | $I_F = -10 \mu\text{A}$                            | 30                | 50   | —    | V                          |   |
| DC Breakdown Voltage Between Any Diode and Substrate, $V_{(BR)DI}$       | $I_{DI} = 10 \mu\text{A}$                          | 30                | 50   | —    | V                          |   |
| DC Reverse (Leakage) Current, $I_R$                                      | $V_F = -20 \text{ V}$                              | —                 | —    | 100  | nA                         |   |
| DC Reverse (Leakage) Current Between Any Diode and Substrate, $I_{DI}$   | $V_{DI} = 20 \text{ V}$                            | —                 | —    | 100  | nA                         |   |
| Magnitude of Diode Offset Voltage Between Diode Pairs                    | $V_{DI} = 20 \text{ V}$<br>$I_{FA} = 1 \text{ mA}$ | —                 | 0.55 | —    | mV                         |   |
| Temperature Coefficient of Forward Voltage Drop, $\Delta V_F / \Delta T$ | $I_F = 1 \text{ mA}$                               | —                 | -1.5 | —    | $\text{mV}/^\circ\text{C}$ |   |
| Reverse Recovery Time, $t_{rr}$  | $I_F = 2 \text{ mA}$ , $I_R = 2 \text{ mA}$        | —                 | 50   | —    | ns                         |   |
| Diode Capacitance, $C_D$   |  | See Fig. 5        |      |      | pF                         |   |
| Diode Anode-to-Substrate Capacitance, $C_{DAI}$                          |  | See Fig. 6        |      |      | pF                         |   |
| Diode Cathode-to-Substrate Capacitance, $C_{DCI}$                        |  | See Fig. 7        |      |      | pF                         |   |
| Magnitude of Cathode-to-Anode Current Ratio, $ I_{FC}/I_{FA} $           | $I_{FA} = 1 \text{ mA}$ , $V_{DS} = 10 \text{ V}$  | 0.9               | 0.96 | —    |                            |   |

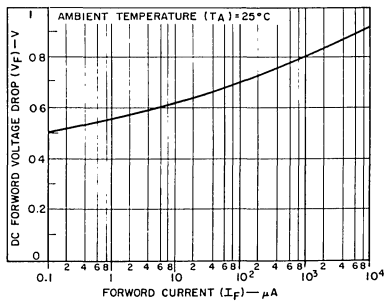


Fig. 2 — DC forward voltage drop vs. forward current.

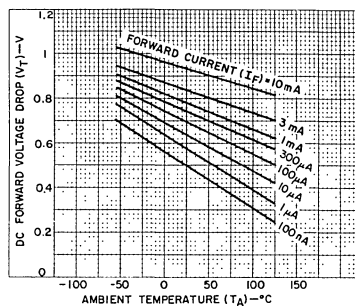


Fig. 3 — DC forward voltage drop vs. ambient temperature.

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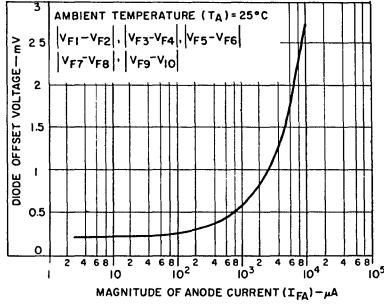


Fig. 4 - Diode offset voltage vs. magnitude of anode current.

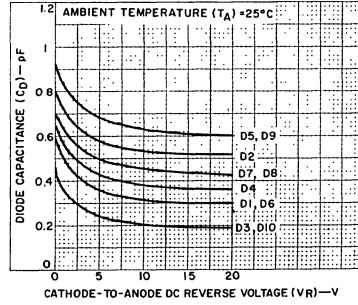


Fig. 5 - Diode capacitance vs. cathode-to-anode reverse voltage.

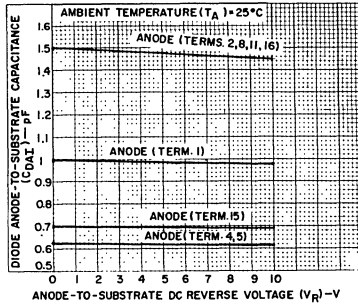


Fig. 6 - Diode anode-to-substrate capacitance vs. reverse voltage.

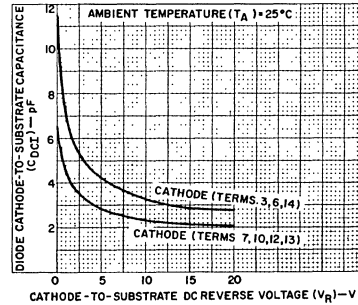


Fig. 7 - Diode cathode-to-substrate capacitance vs. cathode-to-substrate DC reverse voltage.

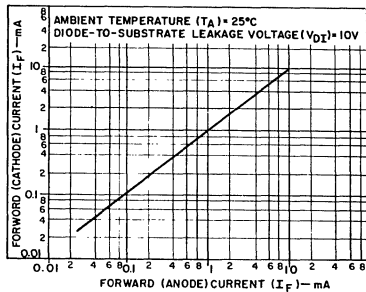


Fig. 8 - Forward (cathode) current vs. forward (anode) current.

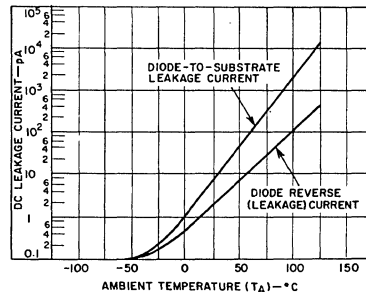


Fig. 9 - DC leakage current vs. ambient temperature.

# CA3146, CA3146A CA3183, CA3183A

August 1991

High-Voltage Transistor Arrays

## Features

- Matched General-Purpose Transistors
- $V_{BE}$  Matched  $\pm 5\text{mV}$  Max
- Operation from DC to 120MHz (CA3146, A)
- Low-Noise Figure: 3.2dB Typ at 1 kHz (CA3146, A)
- High  $I_C$ : 75mA Max (CA3183, A)

## Applications

- General Use in Signal Processing Systems in DC Through VHF Range
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers
- Lamp and Relay Drivers (CA3183, A)
- Thyristor Firing (CA3183, A)

## Description

The CA3146A, CA3146, CA3183A, and CA3183\* are general-purpose high-voltage silicon n-p-n transistor arrays on a common monolithic substrate.

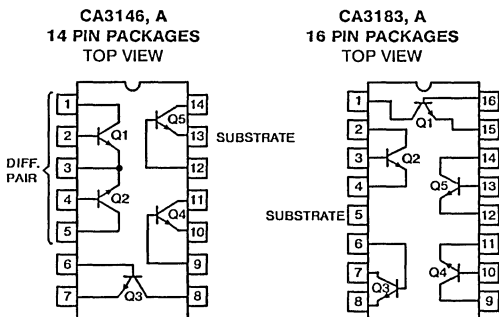
Types CA3146A and CA3146 consist of five transistors with two of the transistors connected to form a differentially-connected pair. These types are recommended for low-power applications in the DC through VHF range. Both types are supplied in 14-lead dual-in-line plastic (E suffix) and 14-lead small outline (M suffix) packages and operate over the ambient temperature range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ . (CA3146A and CA3146 are high-voltage versions of the popular predecessor type CA3046.)

Types CA3183A and CA3183 consist of five high-current transistors with independent connections for each transistor. In addition two of these transistors (Q1 and Q2) are matched at low-current (i.e. 1 mA) for applications where offset parameters are of special importance. A special substrate terminal is also included for greater flexibility in circuit design. Both types are supplied in 16-lead dual-in-line plastic (E suffix) and 16-lead small outline (M suffix) packages and operate over the ambient temperature range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ . (CA3183A and CA3183 are high-voltage versions of the popular predecessor type CA3083.)

The types with an "A" suffix are premium versions of their non-"A" counterparts and feature tighter control of breakdown voltages making them more suitable for higher voltage applications.

For detailed application information, see companion Application Note, ICAN-5296 "Application of the CA3018 Integrated Circuit Transistor Array."

## Pinouts



\*Formerly Developmental Types Nos.

CA3146A - TA6084                      CA3183A - TA6094  
CA3146 - TA6181                      CA3183 - TA6183

| TYPE                             | $P_T^*$<br>MAX.<br>mW | $I_C$<br>MAX.<br>mA | $V_{CE0}$<br>MAX.<br>V | $V_{CBO}$<br>MAX.<br>V | $V_{CE}$ sat.<br>at 10 mA<br>TYP.<br>V | $h_{FE}$<br>at 1 mA,<br>& $V_{CE} = 5\text{V}$<br>TYP. | DIFF. PAIR AT 1mA      |                                   | $T_A$ Range<br>(OPERATING)<br>$^\circ\text{C}$ |
|----------------------------------|-----------------------|---------------------|------------------------|------------------------|--|--|------------------------|-----------------------------------|--|
|                                  |                       |                     |                        |                        |  |  | $V_{I0}$<br>MAX.<br>mV | $I_{I0}$<br>MAX.<br>$\mu\text{A}$ |  |
| VALUES APPLY FOR EACH TRANSISTOR |                       |                     |                        |                        |  |  |                        |                                   |  |
| CA3146A                          | 300                   | 50                  | 40                     | 50                     | 0.33                                   | 100  | $\pm 5$                | 2                                 | $-40 - +85$                                    |
| CA3146                           | 300                   | 50                  | 30                     | 40                     | 0.33                                   | 100  | $\pm 5$                | 2                                 | $-40 - +85$                                    |
| CA3183A                          | 500                   | 75                  | 40                     | 50                     | 0.16                                   | 75   | $\pm 5$                | 2.5                               | $-40 - +85$                                    |
| CA3183                           | 500                   | 75                  | 30                     | 40                     | 0.16                                   | 75   | $\pm 5$                | 2.5                               | $-40 - +85$                                    |

\* Caution on Total Package Power Dissipation: The maximum total package dissipation rating for the CA3146 and CA3183 Series circuits is 750 mW at temperatures up to  $+55^\circ\text{C}$ , then derate linearly at 6.67mW/ $^\circ\text{C}$ .



## CA3146, CA3146A, CA3183, CA3183A

### MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^\circ\text{C}$

#### POWER DISSIPATION:

|  |   |
|--|---|
| Any one transistor -   |   |
| CA3146A, CA3146  | 300 mW                                    |
| CA3183A, CA3183  | 500 mW                                    |
| Total package -  |   |
| Up to $55^\circ\text{C}$ (CA3146A, CA3146, CA3183A, CA3183)    | 750 mW                                    |
| Above to $55^\circ\text{C}$ (CA3146A, CA3146, CA3183A, CA3183) | Derate linearly 6.67 mW/ $^\circ\text{C}$ |

#### AMBIENT TEMPERATURE RANGE:

|                                  |                               |
|----------------------------------|-------------------------------|
| Operating -                      |                               |
| CA3146A, CA3146, CA3183A, CA3183 | $-40$ to $+85^\circ\text{C}$  |
| Storage (all types)              | $-65$ to $+150^\circ\text{C}$ |

The following ratings apply for each transistor in the device:

#### COLLECTOR-TO-EMITTER VOLTAGE ( $V_{CEO}$ ):

|                  |      |
|------------------|------|
| CA3146A, CA3183A | 40 V |
| CA3146, CA3183   | 30 V |

#### COLLECTOR-TO-BASE VOLTAGE ( $V_{CBO}$ ):

|                  |      |
|------------------|------|
| CA3146A, CA3183A | 50 V |
| CA3146, CA3183   | 40 V |

#### COLLECTOR-TO-SUBSTRATE VOLTAGE ( $V_{CISO}$ ):<sup>■</sup>

|                  |      |
|------------------|------|
| CA3146A, CA3183A | 50 V |
| CA3146, CA3183   | 40 V |

#### EMITTER-TO-BASE VOLTAGE ( $V_{EB0}$ ) all types

|  |     |
|--|-----|
|  | 5 V |
|--|-----|

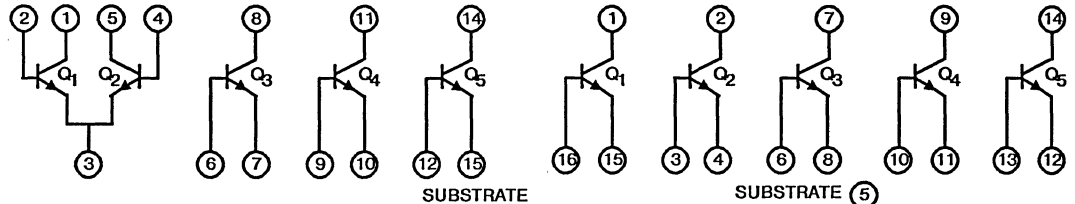
#### COLLECTOR CURRENT -

|                 |       |
|-----------------|-------|
| CA3146A, CA3146 | 50 mA |
| CA3183          | 75 mA |

#### BASE CURRENT ( $I_B$ ) - CA3183A, CA3183

|  |       |
|--|-------|
|  | 20 mA |
|--|-------|

<sup>■</sup> The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.



CA3146A, CA3146

CA3183A, CA3183

Figure 1 - Schematic diagrams of high-voltage arrays.

### COMPARISON OF RELATED PREDECESSOR TYPE WITH TYPES IN THIS DATA BULLETIN

|         | DATA FILE NO. | $V_{CE0}$ MIN. | $V_{CBO}$ MIN. | $V_{CE}$ sat. TYP. V |              | $I_C$ MAX. mA | $C_{CB}$ TYP. pF | $C_{CI}$ TYP. pF | $C_{CE}$ TYP. pF |
|---------|---------------|----------------|----------------|----------------------|--------------|---------------|------------------|------------------|------------------|
|         |               |                |                | $I_C = 10$ mA        | $I_C = 1$ mA |               |                  |                  |                  |
| CA3046  | 341           | 15             | 20             | 0.23                 | 0.715        | 50            | 0.58             | 2.8              | 0.6              |
| CA3146A |               | 40             | 50             | 0.33                 | 0.730        | 50            | 0.37             | 2.2              | 0.7              |
| CA3146  |               | 30             | 40             | 0.33                 | 0.730        | 50            | 0.37             | 2.2              | 0.7              |
| CA3083  | 481           | 15             | 20             | $I_C = 50$ mA        |              | 100           | —                | —                | —                |
| CA3183A |               | 40             | 50             | 0.4                  | 0.74         |               |                  |                  |                  |
| CA3183  |               | 30             | 40             | 1.7                  | 0.75         |               |                  |                  |                  |

## CA3146, CA3146A, CA3183, CA3183A

### STATIC ELECTRICAL CHARACTERISTICS – CA3146 Series

| CHARACTERISTICS   | SYMBOL  | TEST CONDITIONS  |                           | LIMITS  |           |      |        |           |      | UNITS                        |   |
|---|---|--|---------------------------|---------|-----------|------|--------|-----------|------|------------------------------|---|
|   |   | $T_A = 25^\circ\text{C}$                               | Typ. Char. Curve Fig. No. | CA3146A |           |      | CA3146 |           |      |                              |   |
|   |   |  |                           | Min.    | Typ.      | Max. | Min.   | Typ.      | Max. |                              |   |
| <b>For Each Transistor :</b>  |   |  |                           |         |           |      |        |           |      |                              |   |
| Collector-to-Base Breakdown Voltage                                   | $V_{(BR)CBO}$                                   | $I_C = 10\ \mu\text{A}, I_E = 0$                       | –                         | 50      | 72        | –    | 40     | 72        | –    | V                            |   |
| Collector-to-Emitter Breakdown Voltage                                | $V_{(BR)CEO}$                                   | $I_C = 1\ \text{mA}, I_B = 0$                          | –                         | 40      | 56        | –    | 30     | 56        | –    | V                            |   |
| Collector-to-Substrate Breakdown Voltage                              | $V_{(BR)CIO}$                                   | $I_{C1} = 10\ \mu\text{A}, I_B = 0, I_E = 0$           | –                         | 50      | 72        | –    | 40     | 72        | –    | V                            |   |
| Emitter-to-Base Breakdown Voltage                                     | $V_{(BR)EBO}$                                   | $I_E = 10\ \mu\text{A}, I_C = 0$                       | –                         | 5       | 7         | –    | 5      | 7         | –    | V                            |   |
| Collector-Cutoff Current  | $I_{CEO}$                                       | $V_{CE} = 10\ \text{V}, I_B = 0$                       | 2                         | –       | see curve | 5    | –      | see curve | 5    | $\mu\text{A}$                |   |
| Collector-Cutoff Current  | $I_{CBO}$                                       | $V_{CB} = 10\ \text{V}, I_E = 0$                       | 3                         | –       | 0.002     | 100  | –      | 0.002     | 100  | nA                           |   |
| DC Forward-Current Transfer Ratio                                     | $h_{FE}$  | $V_{CE} = 5\ \text{V}$                                 | $I_C = 10\ \text{mA}$     | 4       | –         | 85   | –      | –         | 85   | –                            | – |
|   |   |  | $I_C = 1\ \text{mA}$      | 4       | 30        | 100  | –      | 30        | 100  | –                            |   |
|   |   |  | $I_C = 10\ \mu\text{A}$   | 4       | –         | 90   | –      | –         | 90   | –                            |   |
| Base-to-Emitter Voltage   | $V_{BE}$  | $V_{CE} = 3\ \text{V}, I_C = 1\ \text{mA}$             | 5                         | 0.63    | 0.73      | 0.83 | 0.63   | 0.73      | 0.83 | V                            |   |
| Collector-to-Emitter Saturation Voltage                               | $V_{CEsat}$                                     | $I_C = 10\ \text{mA}, I_B = 1\ \text{mA}$              | 6                         | –       | 0.33      | –    | –      | 0.33      | –    | V                            |   |
| <b>For transistors Q3 and Q4 (Darlington Configuration):</b>          |   |  |                           |         |           |      |        |           |      |                              |   |
| Base-to-Emitter (Q3 to Q4)  | $V_{BE}$  | $V_{CE} = 5\ \text{V}$                                 | $I_E = 10\ \text{mA}$     | 8       | –         | 1.46 | –      | –         | 1.46 | –                            | V |
|   |   |  | $I_E = 1\ \text{mA}$      | 8,9     | –         | 1.32 | –      | –         | 1.32 | –                            |   |
| Magnitude of Base-to-Emitter Temperature Coefficient                  | $\left  \frac{\Delta V_{BE}}{\Delta T} \right $ | $V_{CE} = 5\ \text{V}, I_E = 1\ \text{mA}$             | –                         | –       | 4.4       | –    | –      | 4.4       | –    | $\text{mV}/^\circ\text{C}$   |   |
| <b>For transistors Q1 and Q2 (AS a Differential Amplifier):</b>       |   |  |                           |         |           |      |        |           |      |                              |   |
| Magnitude of Input Offset Voltage<br>$ V_{BE1} - V_{BE2} $            | $ V_{IO} $                                      | $V_{CE} = 5\ \text{V}, I_E = 1\ \text{mA}$             | 10, 11                    | –       | 0.48      | 5    | –      | 0.48      | 5    | mV                           |   |
| Magnitude of Base-to-Emitter Temperature Coefficient                  | $\left  \frac{\Delta V_{BE}}{\Delta T} \right $ | $V_{CE} = 5\ \text{V}, I_E = 1\ \text{mA}$             | –                         | –       | 1.9       | –    | –      | 1.9       | –    | $\text{mV}/^\circ\text{C}$   |   |
| Magnitude of $V_{IO}$ ( $V_{BE1} - V_{BE2}$ ) Temperature Coefficient | $\left  \frac{\Delta V_{IO}}{\Delta T} \right $ | $V_{CE} = 5\ \text{V}, I_{C1} = I_{C2} = 1\ \text{mA}$ | –                         | –       | 1.1       | –    | –      | 1.1       | –    | $\mu\text{V}/^\circ\text{C}$ |   |
| Magnitude of Input Offset Current<br>$ I_{O1} - I_{O2} $              | CA3146AE and CA3146E only<br>$I_{IO}$           | $V_{CE} = 5\ \text{V}, I_{C1} = I_{C2} = 1\ \text{mA}$ | 12                        | –       | 0.3       | 2    | –      | 0.3       | 2    | $\mu\text{A}$                |   |

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## CA3146, CA3146A, CA3183, CA3183A

### DYNAMIC ELECTRICAL CHARACTERISTICS – CA3146 Series

| CHARACTERISTICS   | SYMBOL   | TEST CONDITIONS  |                          | CA3146A |                      |      | CA3146 |                      |      | UNITS            |
|---|----------|--|--------------------------|---------|----------------------|------|--------|----------------------|------|------------------|
|   |          | $T_A = 25^\circ\text{C}$   | Typ. Char. Curve Fig.No. | Min.    | Typ.                 | Max. | Min.   | Typ.                 | Max. |                  |
|   |          |  |                          |         |                      |      |        |                      |      |                  |
| Low Frequency Noise Figure                                      | NF       | $f = 1\text{kHz}, V_{CE} = 5\text{V}, I_C = 100\mu\text{A},$ Source resistance = $1\text{k}\Omega$ | 14                       | –       | 3.25                 | –    | –      | 3.25                 | –    | dB               |
| Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: |          |  |                          |         |                      |      |        |                      |      |                  |
| Forward-Current Transfer Ratio                                  | $h_{fe}$ | $f = 1\text{kHz}, V_{CE} = 5\text{V}, I_C = 1\text{mA}$  | 16                       | –       | 100                  | –    | –      | 100                  | –    | –                |
| Short-Circuit Input Impedance                                   | $h_{ie}$ |  | 16                       | –       | 2.7                  | –    | –      | 3.5                  | –    | $\text{k}\Omega$ |
| Open-Circuit Output Impedance                                   | $h_{oe}$ |  | 16                       | –       | 15.6                 | –    | –      | 15.6                 | –    | $\mu\text{mho}$  |
| Open-Circuit Reverse-Voltage Transfer Ratio                     | $h_{re}$ |  | 16                       | –       | $1.8 \times 10^{-4}$ | –    | –      | $1.8 \times 10^{-4}$ | –    | –                |
| Admittance Characteristics:                                     |          |  |                          |         |                      |      |        |                      |      |                  |
| Forward Transfer Admittance                                     | $Y_{fe}$ | $f = 1\text{MHz}, V_{CE} = 5\text{V}, I_C = 1\text{mA}$  | 17                       | –       | $31-j1.5$            | –    | –      | $31-j1.5$            | –    | $\text{mmho}$    |
| Input Admittance  | $Y_{ie}$ |  | 18                       | –       | $0.35+j0.04$         | –    | –      | $0.3+j0.04$          | –    | $\text{mmho}$    |
| Output Admittance   | $Y_{oe}$ |  | 19                       | –       | $0.001+j0.03$        | –    | –      | $0.001+j0.03$        | –    | $\text{mmho}$    |
| Reverse Transfer Admittance                                     | $Y_{re}$ |  | 20                       | –       | See curve            | –    | –      | See curve            | –    | $\text{mmho}$    |
| Gain-Bandwidth Product  | $f_T$    | $V_{CE} = 5\text{V}, I_C = 3\text{mA}$   | 21                       | 300     | 500                  | –    | 300    | 500                  | –    | MHz              |
| Emitter-to-Base Capacitance                                     | $C_{EB}$ | $V_{EB} = 5\text{V}, I_E = 0$  | 22                       | –       | 0.70                 | –    | –      | 0.70                 | –    | pF               |
| Collector-to-Base Capacitance                                   | $C_{CB}$ | $V_{CB} = 5\text{V}, I_C = 0$  | 22                       | –       | 0.37                 | –    | –      | 0.37                 | –    | pF               |
| Collector-to-Substrate Capacitance                              | $C_{Cl}$ | $V_{Cl} = 5\text{V}, I_C = 0$  | 22                       | –       | 2.2                  | –    | –      | 2.2                  | –    | pF               |

### STATIC ELECTRICAL CHARACTERISTICS – CA3183 Series

| CHARACTERISTICS   | SYMBOL        | TEST CONDITIONS                             |                           | LIMITS  |      |      |        |      |      | UNITS         |
|---|---------------|---|---------------------------|---------|------|------|--------|------|------|---------------|
|   |               | $T_A = 25^\circ\text{C}$                    | Typ. Char. Curve Fig. No. | CA3183A |      |      | CA3183 |      |      |               |
|   |               |   |                           | Min.    | Typ. | Max. | Min.   | Typ. | Max. |               |
| <b>For Each Transistor:</b>                                     |               |   |                           |         |      |      |        |      |      |               |
| Collector-to-Base Breakdown Voltage                             | $V_{(BR)CBO}$ | $I_C = 100\mu\text{A}, I_E = 0$             | –                         | 50      | –    | –    | 40     | –    | –    | V             |
| Collector-to-Emitter Breakdown Voltage                          | $V_{(BR)CEO}$ | $I_C = 1\text{mA}, I_B = 0$                 | –                         | 40      | –    | –    | 30     | –    | –    | V             |
| Collector-to-Substrate Breakdown Voltage                        | $V_{(BR)ClO}$ | $I_{Cl} = 100\mu\text{A}, I_B = 0, I_E = 0$ | –                         | 50      | –    | –    | 40     | –    | –    | V             |
| Emitter-to-Base Breakdown Voltage                               | $V_{(BR)EBO}$ | $I_E = 500\mu\text{A}, I_C = 0$             | –                         | 5       | –    | –    | 5      | –    | –    | V             |
| Collector-Cutoff Current  | $I_{CEO}$     | $V_{CE} = 10\text{V}, I_B = 0$              | 23                        | –       | –    | 10   | –      | –    | 10   | $\mu\text{A}$ |
| Collector-Cutoff Current  | $I_{CBO}$     | $V_{CB} = 10\text{V}, I_E = 0$              | 24                        | –       | –    | 1    | –      | –    | 1    | $\mu\text{A}$ |
| DC Forward-Current Transfer Ratio                               | $h_{FE}$      | $V_{CE} = 3\text{V}, I_C = 10\text{mA}$     | 25, 26                    | 40      | –    | –    | 40     | –    | –    | –             |
|   |               | $V_{CE} = 5\text{V}, I_C = 50\text{mA}$     | –                         | 40      | –    | –    | 40     | –    | –    | –             |
| Base-to-Emitter Voltage   | $V_{BE}$      | $V_{CE} = 3\text{V}, I_C = 10\text{mA}$     | 27                        | 0.65    | 0.75 | 0.85 | 0.65   | 0.75 | 0.85 | V             |
| Collector-to-Emitter Saturation Voltage                         | $*V_{CEsat}$  | $I_C = 50\text{mA}, I_B = 5\text{mA}$       | 28                        | –       | 1.7  | 3.0  | –      | 1.7  | 3.0  | V             |
| <b>For Transistors Q1 and Q2 (As a Differential Amplifier):</b> |               |   |                           |         |      |      |        |      |      |               |
| Absolute Input Offset Voltage                                   | $ V_{IO} $    | $V_{CE} = 3\text{V}, I_C = 1\text{mA}$      | 29                        | –       | 0.47 | 5    | –      | 0.47 | 5    | mV            |
| Absolute Input Offset Current                                   | $ I_{IO} $    |   | 30                        | –       | 0.78 | 2.5  | –      | 0.78 | 2.5  | $\mu\text{A}$ |

\* A maximum dissipation of 5 transistors x 150mW = 750mW is possible for a particular application.

# CA3146, CA3146A, CA3183, CA3183A

## TYPICAL STATIC CHARACTERISTICS CURVES — CA3146 SERIES

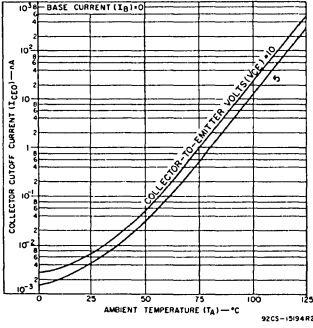


Fig. 2 —  $I_{CEO}$  vs.  $T_A$  for any transistor.

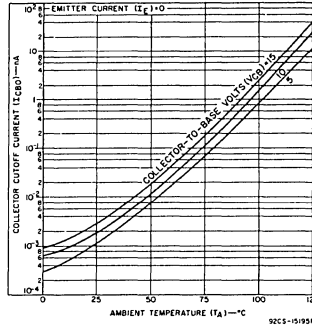


Fig. 3 —  $I_{CBO}$  vs.  $T_A$  for any transistor.

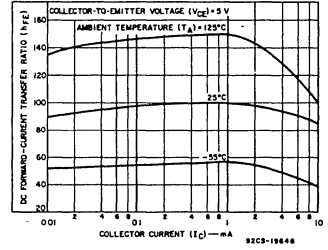


Fig. 4 —  $h_{FE}$  vs.  $I_C$  for any transistor.

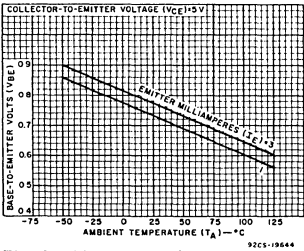


Fig. 5 —  $V_{BE}$  vs.  $T_A$  for any transistor.

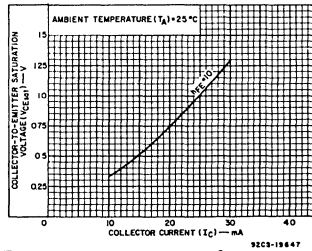


Fig. 6 —  $V_{CE\ sat}$  vs.  $I_C$  for any transistor.

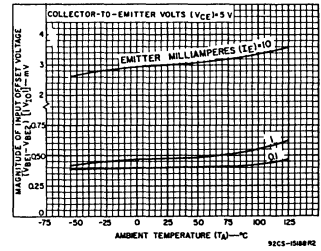


Fig. 10 —  $V_{I0}$  vs.  $T_A$  for Q1 and Q2.

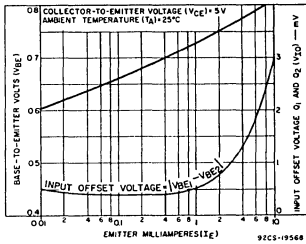


Fig. 11 —  $V_{BE}$  and  $V_{I0}$  vs.  $I_E$  for Q1 and Q2.

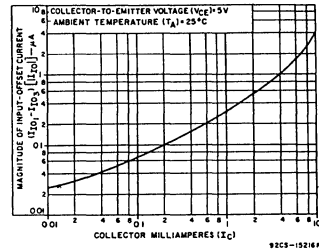


Fig. 12 —  $I_{I0}$  vs.  $I_C$  (Q1 and Q2) for types CA3146A and CA3146

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ARRAYS

# CA3146, CA3146A, CA3183, CA3183A

## TYPICAL DYNAMIC CHARACTERISTICS CURVES (FOR ANY TRANSISTOR) – CA3146 SERIES

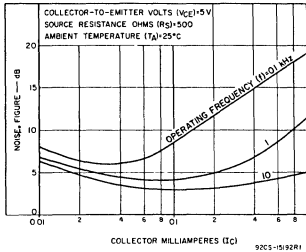


Fig. 13 – NF vs.  $I_C$  @  $R_S = 500\Omega$ .

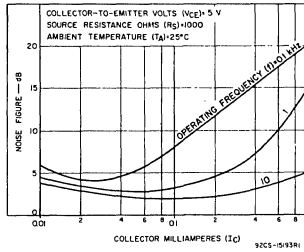


Fig. 14 – NF vs.  $I_C$  @  $R_S = 1k\Omega$ .

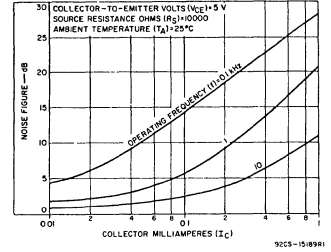


Fig. 15 – NF vs.  $I_C$  @  $R_S = 10k\Omega$ .

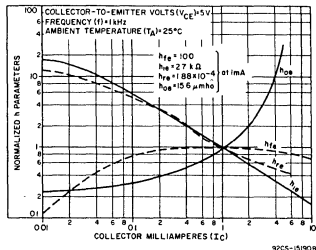


Fig. 16 –  $h_{fe}$ ,  $h_{ie}$ ,  $h_{oe}$ ,  $h_{re}$  vs.  $I_C$ .

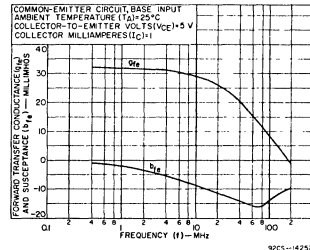


Fig. 17 –  $y_{fe}$  vs.  $f$ .

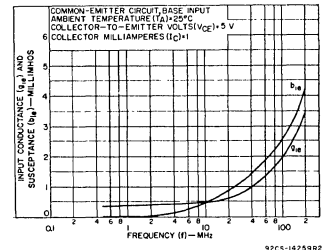


Fig. 18 –  $y_{re}$  vs.  $f$ .

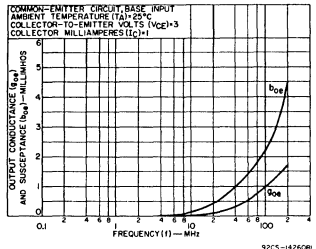


Fig. 19 –  $y_{oe}$  vs.  $f$ .

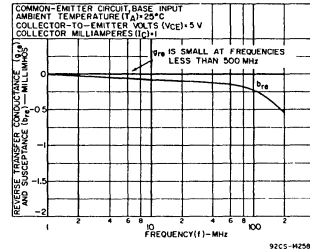


Fig. 20 –  $y_{re}$  vs.  $f$ .

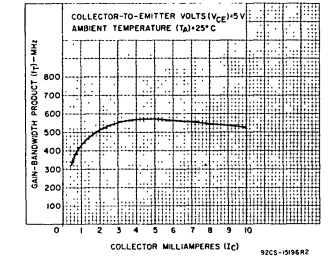


Fig. 21 –  $f_T$  vs.  $I_C$ .

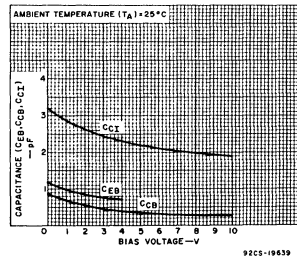


Fig. 22 –  $C_{EB}$ ,  $C_{CB}$ ,  $C_{cI}$  vs. bias voltage

# CA3146, CA3146A, CA3183, CA3183A

## TYPICAL STATIC CHARACTERISTICS CURVES – CA3183 SERIES

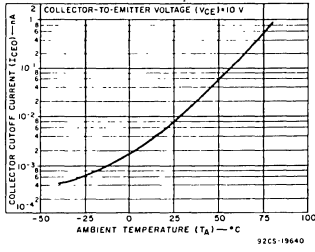


Fig. 23 –  $I_{CEO}$  vs.  $T_A$  for any transistor.

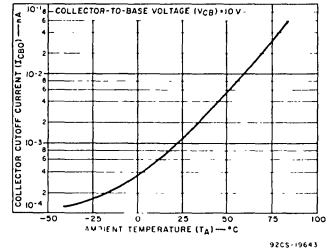


Fig. 24 –  $I_{CBO}$  vs.  $T_A$  for any transistor.

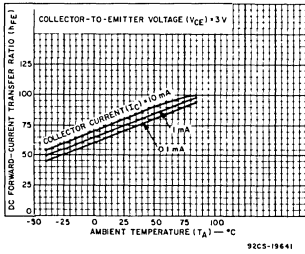


Fig. 25 –  $h_{FE}$  vs.  $T_A$  for any transistor.

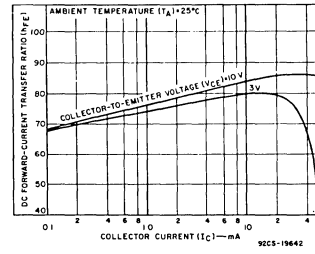


Fig. 26 –  $h_{FE}$  vs.  $I_C$  for any transistor.

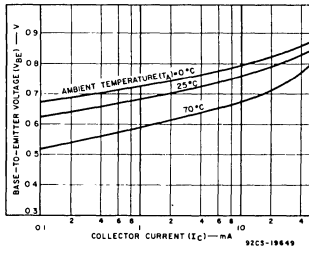


Fig. 27 –  $V_{BE}$  vs.  $I_C$  for any transistor.

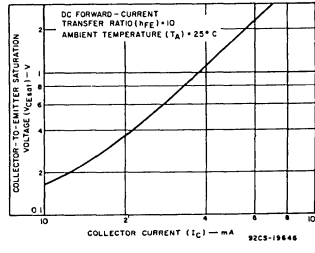


Fig. 28 –  $V_{CE sat}$  vs.  $I_C$  for any transistor.

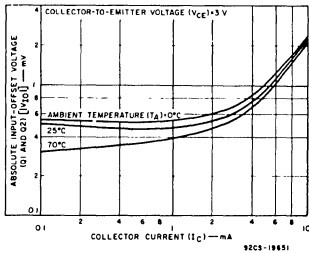


Fig. 29 –  $|V_{IO}|$  vs.  $I_C$  for differential amplifier (Q1 and Q2).

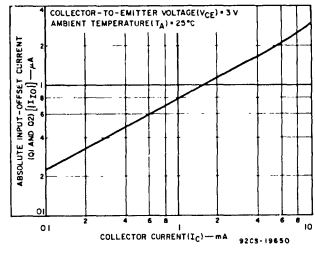


Fig. 30 –  $|I_{IO}|$  vs.  $I_C$  for differential amplifier (Q1 and Q2).

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ARRAYS

August 1991

## High-Frequency N-P-N Transistor Arrays For Low-Power Applications at Frequencies Up to 1.5GHz

### Features

- Gain-Bandwidth Product ( $f_T$ ) ..... >3GHz
- Five Transistors on a Common Substrate

### Applications

- VHF Amplifiers
- VHF Mixers
- Multifunction Combinations-RF/Mixer/Oscillator
- IF Converter
- IF Amplifiers
- Sense Amplifiers
- Synthesizers
- Synchronous Detectors
- Cascade Amplifiers

### Description

The CA3227 and CA3246\* consist of five general purpose silicon n-p-n transistors on a common monolithic substrate. Each of the transistors exhibits a value of  $f_T$  in excess of 3GHz, making them useful from DC to 1.5GHz. The monolithic construction of these devices provides close electrical and thermal matching of the five transistors.

The CA3227 is supplied in a 16-lead Small Outline package (M suffix) and in 16-lead dual-in-line plastic package (E suffix). The CA3246 is supplied in a 14-lead Small Outline package (M suffix) and in a 14-lead dual-in-line plastic package (E suffix).

\*Formerly RCA Development Nos. TA10854 and TA10855, respectively.

### Schematic Diagrams

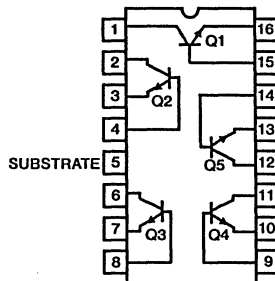


FIGURE 1. SCHEMATIC DIAGRAM OF CA3227

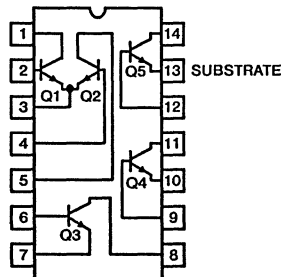


FIGURE 2. SCHEMATIC DIAGRAM OF CA3246

### MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^\circ\text{C}$

#### POWER DISSIPATION, $P_D$ :

- Any one transistor ..... 85mW
- Total Package:
- For  $T_A$  up to  $75^\circ\text{C}$  ..... 425mW
- For  $T_A > 75^\circ\text{C}$  ..... Derate Linearly at 6.67mW/ $^\circ\text{C}$

#### AMBIENT TEMPERATURE RANGE:

- Operating .....  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$
- Storage .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$

#### LEAD TEMPERATURE (DURING SOLDERING):

- At distance  $1/16 \pm 1/32$  in. ( $1.59 \pm 0.79$  mm) from case for 10 seconds max. ....  $+265^\circ\text{C}$

The following ratings apply for each transistor in the device:

- COLLECTOR-TO-EMITTER VOLTAGE,  $V_{CEO}$  ..... 8V
- COLLECTOR-TO-BASE VOLTAGE,  $V_{CBO}$  ..... 12V
- COLLECTOR-TO-SUBSTRATE VOLTAGE,  $V_{CISO}$  § ..... 20V
- COLLECTOR CURRENT,  $I_C$  ..... 20mA

§ The collector of each transistor of these devices is isolated from the substrate by an integral diode. The substrate (terminal 5/CA3227E and terminal 13/CA3246E) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

CA3227, CA3246

STATIC ELECTRICAL CHARACTERISTICS at  $T_A=25^\circ\text{C}$

| CHARACTERISTIC                           | SYMBOL        | TEST CONDITIONS                        | LIMITS               |      |      | UNITS         |  |
|--|---------------|--|----------------------|------|------|---------------|--|
|  |               |  | Min.                 | Typ. | Max. |               |  |
| <b>For Each Transistor:</b>              |               |  |                      |      |      |               |  |
| Collector-to-Base Breakdown Voltage      | $V_{(BR)CBO}$ | $I_C=10\ \mu\text{A}, I_E=0$           | 12                   | 20   | —    | V             |  |
| Collector-to-Emitter Breakdown Voltage   | $V_{(BR)CEO}$ | $I_C=1\ \text{mA}, I_B=0$              | 8                    | 10   | —    | V             |  |
| Collector-to-Substrate Breakdown Voltage | $V_{(BR)CIO}$ | $I_{C1}=10\ \mu\text{A}, I_B=0, I_E=0$ | 20                   | —    | —    | V             |  |
| Emitter-Cutoff-Current*                  | $I_{EBO}$     | $V_{EB}=4.5\ \text{V}, I_C=0$          | —                    | —    | 10   | $\mu\text{A}$ |  |
| Collector-Cutoff-Current                 | $I_{CEO}$     | $V_{CE}=5\ \text{V}, I_B=0$            | —                    | —    | 1    | $\mu\text{A}$ |  |
| Collector-Cutoff-Current                 | $I_{CBO}$     | $V_{CB}=8\ \text{V}, I_E=0$            | —                    | —    | 100  | nA            |  |
| DC Forward-Current Transfer Ratio        | $h_{FE}$      | $V_{CE}=6\ \text{V}$                   | $I_C=10\ \text{mA}$  | —    | 110  | —             |  |
|  |               |  | $I_C=1\ \text{mA}$   | 40   | 150  | —             |  |
|  |               |  | $I_C=0.1\ \text{mA}$ | —    | 150  | —             |  |
| Base-to-Emitter Voltage                  | $V_{BE}$      | $V_{CE}=6\ \text{V}, I_C=1\ \text{mA}$ | 0.62                 | 0.71 | 0.82 | V             |  |
| Collector-to-Emitter Saturation Voltage  | $V_{CE(sat)}$ | $I_C=10\ \text{mA}, I_B=1\ \text{mA}$  | —                    | 0.13 | 0.50 | V             |  |
| Base-to-Emitter Saturation Voltage       | $V_{BE(sat)}$ | $I_C=10\ \text{mA}, I_B=1\ \text{mA}$  | 0.74                 | —    | 0.94 | V             |  |

\*On small-geometry, high-frequency transistors, it is very good practice never to take the Emitter Base Junction into reverse breakdown. To do so may permanently degrade the  $h_{FE}$ . Hence, the use of  $I_{EBO}$  rather than  $V_{(BR)EBO}$ . These devices are also susceptible to damage by electrostatic discharge and transients in the circuits in which they are used. Moreover, CMOS handling procedures should be employed.



CA3227, CA3246

**DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A=25^\circ\text{C}$ , 200 MHz, Common Emitter**  
**Typical Values Intended Only for Design Guidance**

| CHARACTERISTIC  | TEST CONDITIONS              | TYPICAL VALUES                             | UNITS |         |
|---|------------------------------|--|-------|---------|
| <b>For Each Transistor</b>                                    |                              |  |       |         |
| Input Admittance, $Y_{11}$                                    | $\frac{b_{11}}{g_{11}}$      | $I_C=1\text{ mA},$<br>$V_{CE}=5\text{ V}$  | 4     | mmho    |
|   |                              |  | 0.75  |         |
| Output Admittance, $Y_{22}$                                   | $\frac{b_{22}}{g_{22}}$      | $I_C=1\text{ mA},$<br>$V_{CE}=5\text{ V}$  | 2.7   | mmho    |
|   |                              |  | 0.13  |         |
| Forward Transfer Admittance, $Y_{21}$                         | $\frac{Y_{21}}{\theta_{21}}$ | $I_C=1\text{ mA},$<br>$V_{CE}=5\text{ V}$  | 29.3  | mmho    |
|   |                              |  | -33   | degrees |
| Reverse Transfer Admittance, $Y_{12}$                         | $\frac{Y_{12}}{\theta_{12}}$ | $I_C=1\text{ mA},$<br>$V_{CE}=5\text{ V}$  | 0.38  | mmho    |
|   |                              |  | -97   | degrees |
| Input Admittance, $Y_{11}$                                    | $\frac{b_{11}}{g_{11}}$      | $I_C=10\text{ mA},$<br>$V_{CE}=5\text{ V}$ | 4.8   | mmho    |
|   |                              |  | 2.85  |         |
| Output Admittance, $Y_{22}$                                   | $\frac{b_{22}}{g_{22}}$      | $I_C=10\text{ mA},$<br>$V_{CE}=5\text{ V}$ | 2.75  | mmho    |
|   |                              |  | 0.9   |         |
| Forward Transfer Admittance, $Y_{21}$                         | $\frac{Y_{21}}{\theta_{21}}$ | $I_C=10\text{ mA},$<br>$V_{CE}=5\text{ V}$ | 95    | mmho    |
|   |                              |  | -62   | degrees |
| Reverse Transfer Admittance, $Y_{12}$                         | $\frac{Y_{12}}{\theta_{12}}$ | $I_C=10\text{ mA},$<br>$V_{CE}=5\text{ V}$ | 0.39  | mmho    |
|   |                              |  | -97   | degrees |
| Small-Signal Forward Current Transfer Ratio                   | $h_{21}$                     | $I_C=1\text{ mA},$<br>$V_{CE}=5\text{ V}$  | 7.1   |         |
|   |                              | $I_C=10\text{ mA},$<br>$V_{CE}=5\text{ V}$ | 17    |         |
| <b>Typical Capacities @ 1 MHz, Three-Terminal Measurement</b> |                              |  |       |         |
| Collector-to-Base Capacitance, $C_{CB}$                       | $V_{CB}=6\text{ V}$          | 0.3  | pF    |         |
| Collector-to-Substrate Capacitance, $C_{CI}$                  | $V_{CI}=6\text{ V}$          | 1.6  | pF    |         |
| Collector-to-Emitter Capacitance, $C_{CE}$                    | $V_{CE}=6\text{ V}$          | 0.4  | pF    |         |
| Emitter-to-Base Capacitance, $C_{EB}$                         | $V_{EB}=3\text{ V}$          | 0.75                                       | pF    |         |

## SPECIAL ANALOG CIRCUITS

|  | PAGE  |
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| <b>SPECIAL ANALOG CIRCUITS DATA SHEETS</b> |   |
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| ICL 8049                                   | Antilog Amplifier ..... 8-110   |
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| ICM 7556                                   | Dual General Purpose Timer ..... 8-126                                    |
| LM 555C                                    | Timer ..... 8-3   |

NOTE: Bold type designates a new product from Harris.



# CA555, CA555C, LM555C\*

## Timers For Timing Delays & Oscillator Applications in Commercial, Industrial & Military Equipment

August 1991

### Features

- Accurate Timing from Microseconds Through Hours
- Astable and Monostable Operation
- Adjustable Duty Cycle
- Output Capable of Sourcing or Sinking up to 200mA
- Output Capable of Driving TTL Devices
- Normally ON and OFF Outputs
- High-Temperature Stability ..... 0.005%/°C
- Directly Interchangeable with SE555, NE555, MC1555, and MC1455

### Applications

- Precision Timing
- Sequential Timing
- Time-Delay Generation
- Pulse Generation
- Pulse-Width and Position Modulation
- Pulse Detector

### Description

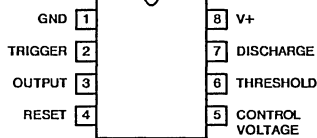
The CA555 and CA555C are highly stable timers for use in precision timing and oscillator applications. As timers, these monolithic integrated circuits are capable of producing accurate time delays for periods ranging from microseconds through hours. These devices are also useful for astable oscillator operation and can maintain an accurately controlled free-running frequency and duty cycle with only two external resistors and one capacitor.

The circuits of the CA555 and CA555C may be triggered by the falling edge of the wave-form signal, and the output of these circuits can source or sink up to a 200-milliamperere current or drive TTL circuits.

The CA555 and CA555C are supplied in standard 8-lead TO-5 style packages (T suffix), 8-lead TO-5 style packages with dual-in-line formed leads (DIL-CAN, S suffix), 8-lead Small Outline package (M suffix), 8-lead dual-in-line plastic packages (MINI-DIP, E suffix), and in chip form (H suffix). These types are direct replacement for industry types in packages with similar terminal arrangements e.g. SE555 and NE555, MC1555 and MC1455, respectively. The CA555 type circuits are intended for applications requiring premium electrical performance. The CA555C type circuits are intended for applications requiring less stringent electrical characteristics.

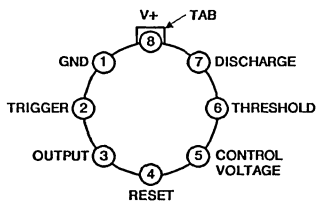
### Pinouts

CA555, CA555C, LM555C  
8 PIN MINI-DIP  
TOP VIEW



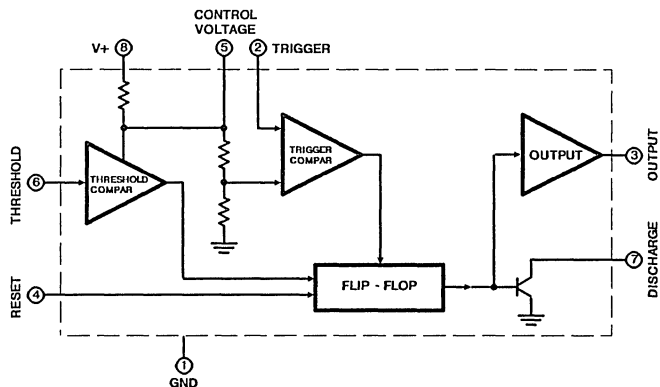
TO-5 Style Package with Formed Leads

CA555, CA555C, LM555C  
8 LEAD METAL CAN  
TOP VIEW



TO-5 Style Package

### Functional Diagram



\*Technical Data on LM Branded types is identical to the corresponding CA Branded types.  
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.  
Copyright © Harris Corporation 1991

## Specifications CA555, CA555C, LM555C

### Absolute Maximum Ratings Absolute-Maximum Values

|                                 |                                       |
|---------------------------------|---------------------------------------|
| DC Supply Voltage               | 18V                                   |
| Device Dissipation:             |                                       |
| Up to $T_A = +55^\circ\text{C}$ | 600mW                                 |
| Above $T_A = +55^\circ\text{C}$ | Derate Linearly 5mW/ $^\circ\text{C}$ |

### Ambient Temperature Range:

|   |   |
|---|---|
| Operating CA555   | $-55^\circ\text{C}$ to $+125^\circ\text{C}$ |
| CA555C  | $0^\circ\text{C}$ to $+70^\circ\text{C}$    |
| Storage Temperature Range   | $-65^\circ\text{C}$ to $+150^\circ\text{C}$ |
| Lead Temperature (During Soldering): At distance 1/16 $\pm$ 1/32in. (1.59 $\pm$ 0.79mm) from case for 10s max | $+265^\circ\text{C}$                        |

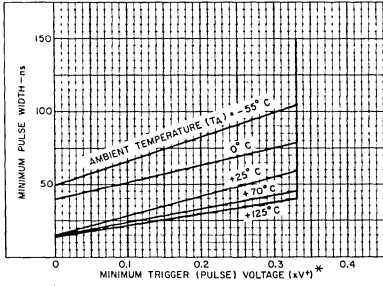
### Electrical Characteristics $T_A = +25^\circ\text{C}$ , $V_+ = 5\text{V}$ to $15\text{V}$ Unless Otherwise Specified

| CHARACTERISTICS                              | TEST CONDITIONS   | LIMITS |             |      |        |             |      | UNITS                 |
|--|---|--------|-------------|------|--------|-------------|------|-----------------------|
|  |   | CA555  |             |      | CA555C |             |      |                       |
|  |   | MIN    | TYP         | MAX  | MIN    | TYP         | MAX  |                       |
| DC Supply Voltage, $V_+$                     |   | 4.5    | -           | 18   | 4.5    | -           | 16   | V                     |
| DC Supply Current (Low State), Note 1, $I_+$ | $V_+ = 5\text{V}$ , $R_L = \infty$  | -      | 3           | 5    | -      | 3           | 6    | mA                    |
|  | $V_+ = 15\text{V}$ , $R_L = \infty$   | -      | 10          | 12   | -      | 10          | 15   | mA                    |
| Threshold Voltage, $V_{TH}$                  |   | -      | (2/3) $V_+$ | -    | -      | (2/3) $V_+$ | -    | V                     |
| Trigger Voltage                              | $V_+ = 5\text{V}$   | 1.45   | 1.67        | 1.9  | -      | 1.67        | -    | V                     |
|  | $V_+ = 15\text{V}$  | 4.8    | 5           | 5.2  | -      | 5           | -    | V                     |
| Trigger Current                              |   | -      | 0.5         | -    | -      | 0.5         | -    | $\mu\text{A}$         |
| Threshold Current, Note 2, $I_{TH}$          |   | -      | 0.1         | 0.25 | -      | 0.1         | 0.25 | $\mu\text{A}$         |
| Reset Voltage                                |   | 0.4    | 0.7         | 1.0  | 0.4    | 0.7         | 1.0  | V                     |
| Reset Current                                |   | -      | 0.1         | -    | -      | 0.1         | -    | mA                    |
| Control Voltage Level                        | $V_+ - 5\text{V}$   | 2.9    | 3.33        | 3.8  | 2.6    | 3.33        | 4    | V                     |
|  | $V_+ = 15\text{V}$  | 9.6    | 10          | 10.4 | 9      | 10          | 11   | V                     |
| Output Voltage Drop: Low State, $V_{OL}$     | $V_+ = 5\text{V}$ , $I_{SINK} = 5\text{mA}$   | -      | -           | -    | -      | 0.25        | 0.35 | V                     |
|  | $I_{SINK} = 8\text{mA}$   | -      | 0.1         | 0.25 | -      | -           | -    | V                     |
|  | $V_+ = 15\text{V}$ , $I_{SINK} = 10\text{mA}$   | -      | 0.1         | 0.15 | -      | 0.1         | 0.25 | V                     |
|  | $I_{SINK} = 50\text{mA}$  | -      | 0.4         | 0.5  | -      | 0.4         | 0.75 | V                     |
|  | $I_{SINK} = 100\text{mA}$   | -      | 2.0         | 2.2  | -      | 2.0         | 0.5  | V                     |
| Output Voltage Droop: High State, $V_{OH}$   | $V_+ = 5\text{V}$ , $I_{SOURCE} = 100\text{mA}$   | 3.0    | 3.3         | -    | 2.75   | 3.3         | -    | V                     |
|  | $V_+ = 15\text{V}$ , $I_{SOURCE} = 100\text{mA}$  | 13.0   | 13.3        | -    | 12.75  | 13.3        | -    | V                     |
|  | $I_{SOURCE} = 200\text{mA}$   | -      | 12.5        | -    | -      | 12.5        | -    | V                     |
| Timing Error (Monostable):                   | $R_1, R_2 = 1\text{k}\Omega$ to $100\text{k}\Omega$ ,<br>$C = 0.1\mu\text{F}$ Tested at | -      | 0.5         | 2    | -      | 1           | -    | %                     |
| Frequency Drift with Temperature             | $V_+ = 5\text{V}$ ,<br>$V_+ = 15\text{V}$   | -      | 30          | 100  | -      | 50          | -    | p/m/ $^\circ\text{C}$ |
| Drift with Supply Voltage                    |   | -      | 0.05        | 0.2  | -      | 0.1         | -    | %/V                   |
| Output Rise Time, $t_r$                      |   | -      | 100         | -    | -      | 100         | -    | ns                    |
| Output Fall Time, $t_f$                      |   | -      | 100         | -    | -      | 100         | -    | ns                    |

#### NOTES:

- When the output is in a high state, the DC supply current is typically 1 mA less than the low-state value.
- The threshold current will determine the sum of the values of  $R_1$  and  $R_2$  to be used in Figure 15 (astable operation); the maximum total  $R_1 + R_2 = 20\text{M}\Omega$ .

# CA555, CA555C, LM555C



\* WHERE x IS THE DECIMAL MULTIPLIER OF THE SUPPLY VOLTAGE

FIGURE 1. MINIMUM PULSE WIDTH vs MINIMUM TRIGGER VOLTAGE

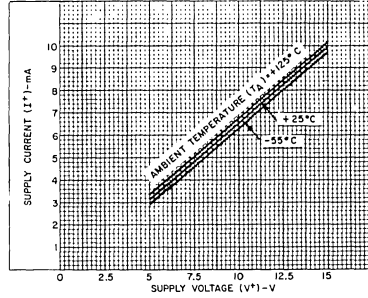


FIGURE 2. SUPPLY CURRENT vs SUPPLY VOLTAGE

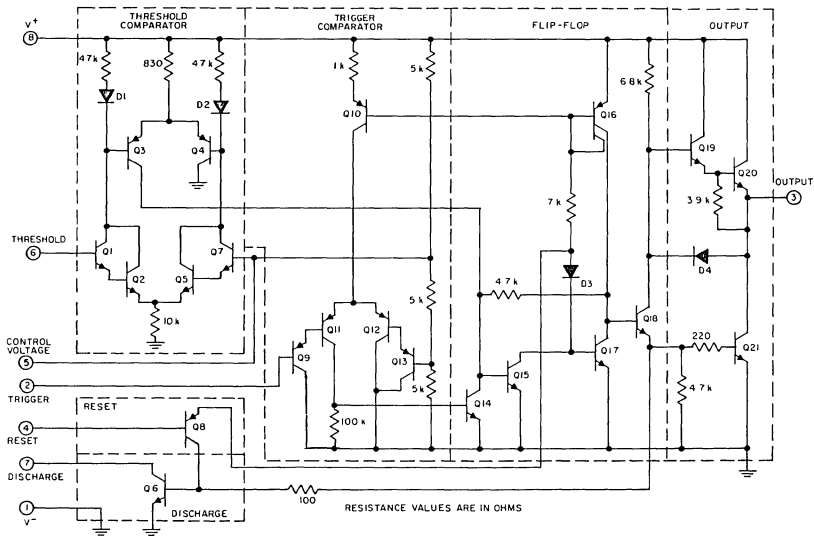


FIGURE 3. SCHEMATIC DIAGRAM OF THE CA555 AND CA555C

CA555, CA555C, LM555C

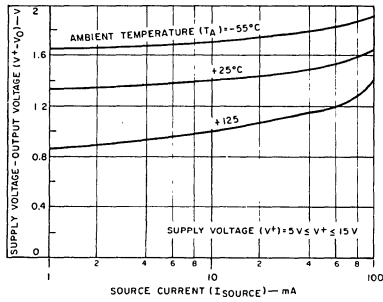


FIGURE 4. OUTPUT VOLTAGE DROP (HIGH STATE) vs SOURCE CURRENT

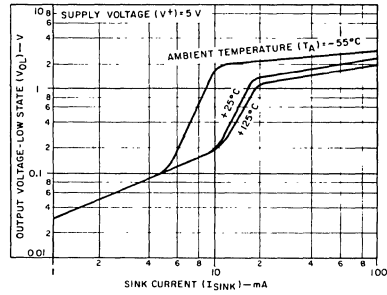


FIGURE 5. OUTPUT VOLTAGE-LOW STATE vs SINK CURRENT AT  $V^+ = 5V$

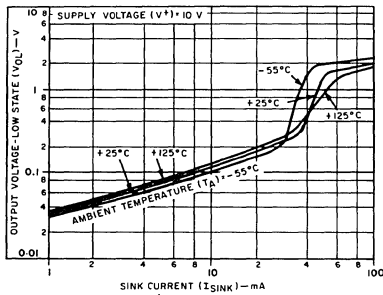


FIGURE 6. OUTPUT VOLTAGE-LOW STATE vs SINK CURRENT AT  $V^+ = 10V$

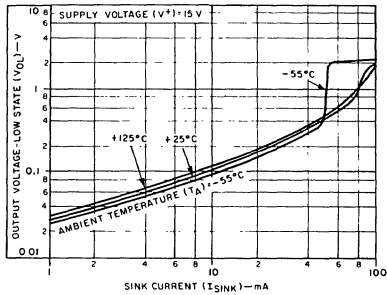


FIGURE 7. OUTPUT VOLTAGE-LOW STATE vs SINK CURRENT AT  $V^+ = 15V$

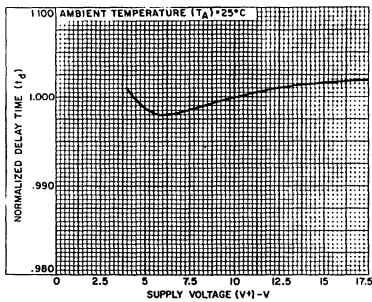


FIGURE 8. DELAY TIME vs SUPPLY VOLTAGE

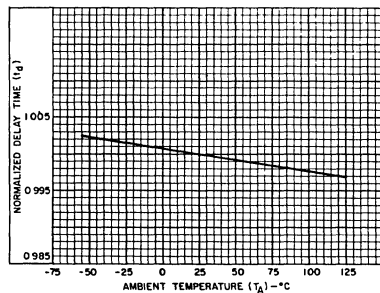
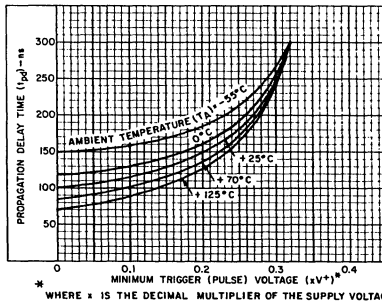


FIGURE 9. DELAY TIME vs TEMPERATURE



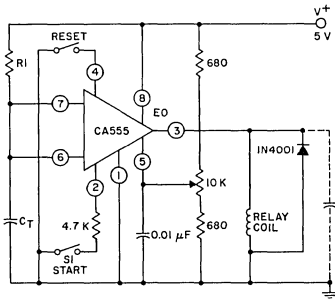
\* WHERE x IS THE DECIMAL MULTIPLIER OF THE SUPPLY VOLTAGE

FIGURE 10. PROPAGATION DELAY TIME vs TRIGGER VOLTAGE

**Typical Applications**

**Reset Timer (Monostable Operation)**

Figure 11 shows the CA555 connected as a reset timer. In this mode of operation capacitor  $C_T$  is initially held discharged by a transistor on the integrated circuit. Upon closing the "start" switch, or applying a negative trigger pulse to terminal 2, the integral timer flip-flop is "set" and releases the short circuit across  $C_T$  which drives the output voltage "high" (relay energized). The action allows the voltage across the capacitor to increase exponentially with the constant  $t = R_1 C_T$ . When the voltage across the capacitor equals  $2/3 V+$ , the comparator resets the flip-flop which in turn discharges the capacitor rapidly and drives the output to its low state.



ALL RESISTANCE VALUES ARE IN OHMS

FIGURE 11. RESET TIMER (MONOSTABLE OPERATION)

Since the charge rate and threshold level of the are both directly proportional to  $V+$ , the timing interval is relatively independent of supply voltage variations. Typically, the timing varies only 0.05% for a 1V change in  $V+$ .

Applying a negative pulse simultaneously to the reset terminal (4) and the trigger terminal (2) during the timing cycle discharges  $C_T$  and causes the timing cycle to restart. Momentarily closing only the reset switch during the timing interval discharges  $C_T$ , but the timing cycle does not restart.

Figure 12 shows the typical waveforms generated during this mode of operation, and Figure 13 gives the family of time delay curves with variations in  $R_1$  and  $C_T$ .

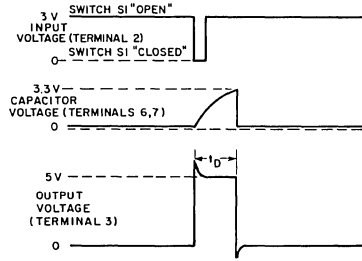


FIGURE 12. TYPICAL WAVEFORMS FOR RESET TIMER

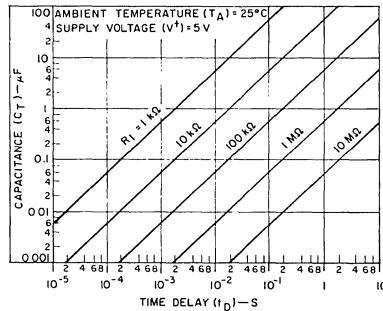


FIGURE 13. TIME DELAY vs RESISTANCE AND CAPACITANCE

**Repeat Cycle Timer (Astable Operation)**

Figure 14 shows the CA555 connected as a repeat cycle timer. In this mode of operation, the total period is a function of both  $R_1$  and  $R_2$ .

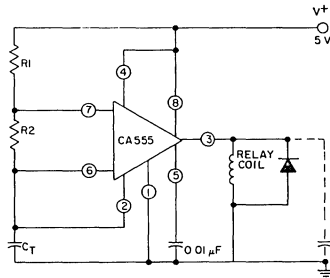


FIGURE 14. REPEAT CYCLE TIMER (ASTABLE OPERATIONAL)

$$T = 0.693 (R_1 + 2R_2) C_T = t_1 + t_2$$

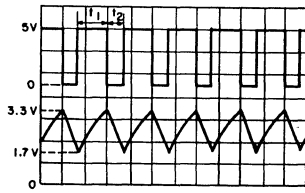
where  $t_1 = 0.693 (R_1 + R_2) C_T$   
 and  $t_2 = 0.693 (R_2) C_T$   
 the duty cycle is:

$$\frac{t_2}{t_1 + t_2} = \frac{R_2}{R_1 + 2R_2}$$

Typical waveforms generated during this mode of operation are shown in Figure 15. Figure 16 give the family of curves of free running frequency with variations in the value of  $(R_1 + 2R_2)$  and  $C_T$ .



CA555, CA555C, LM555C



Top Trace: Output voltage (2V/div. and 0.5 ms/div.)  
 Bottom Trace: Capacitor voltage (1 V/div. and 0.5 ms/div.)

FIGURE 15. TYPICAL WAVEFORMS FOR REPEAT CYCLE TIMER

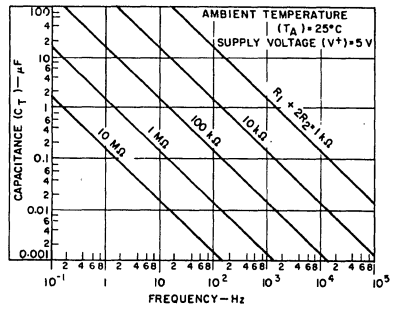


FIGURE 16. FREE RUNNING FREQUENCY OF REPEAT CYCLE TIMER WITH VARIATION IN CAPACITANCE AND RESISTANCE

August 1991

## TV Horizontal Processors

### Features

- CA1391E - Positive Horizontal Sawtooth Input
- CA1394E - Negative Horizontal Sawtooth Input
- Internal Shunt Regulator
- Linear Balanced Phase Detector
- Preset Hold Control Capability
- Pull-In .....  $\pm 300\text{Hz}$  (Typ.)
- Low Thermal Frequency Drift
- Small Static Phase Error
- Variable Output Duty Cycle
- Adjustable DC Loop Gain

### Description

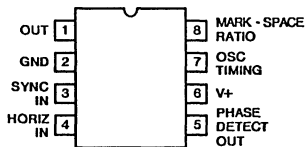
The Harris CA1391E and CA1394E are monolithic integrated circuits designed for use in the low-level horizontal section of monochrome or color television receivers. Functions include a phase detector, an oscillator, a regulator, and a pre-driver.

The CA1391E and CA1394E are electrically equivalent and pin compatible with industry types 1391 and 1394 in similar packages.

These types are supplied in an 8-lead dual-in-line plastic (Mini-DIP) package, and operate over an ambient temperature range of 0 to +85°C.

### Pinout

CA1391E, CA1394E  
(PLASTIC MINI-DIP)  
TOP VIEW



### Functional Block Diagram

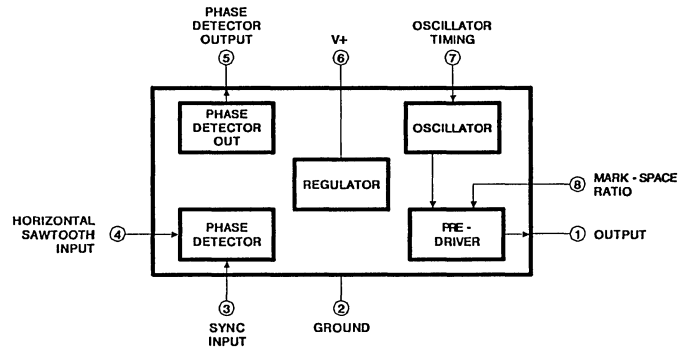


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM OF THE CA1391E, CA1394E

# CA1391, CA1394

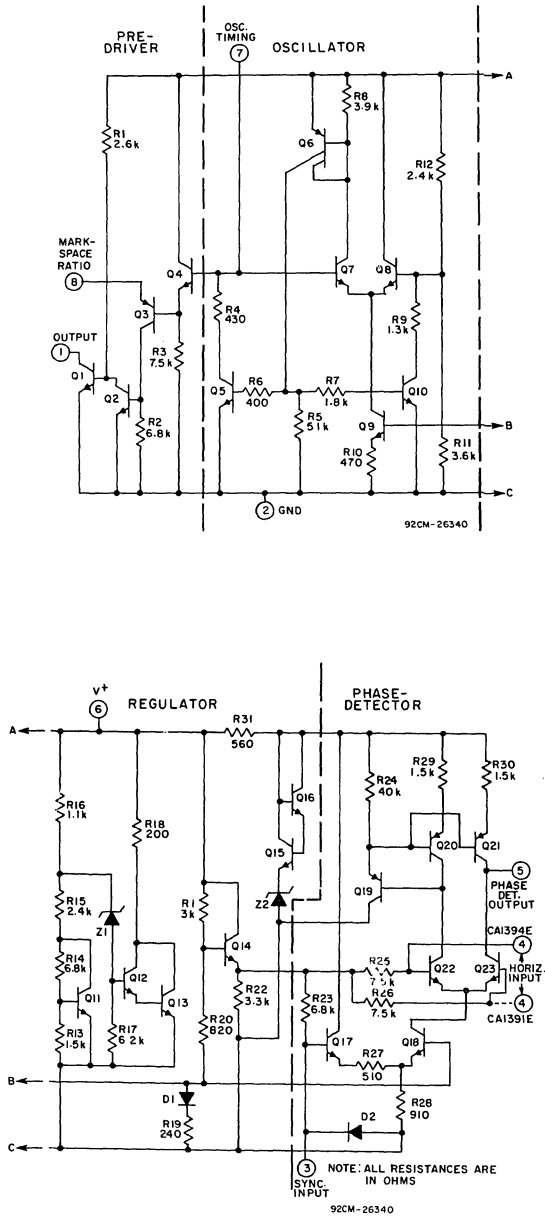


Fig.2 - Schematic diagram of CA1391E, CA1394E.

# CA1391, CA1394

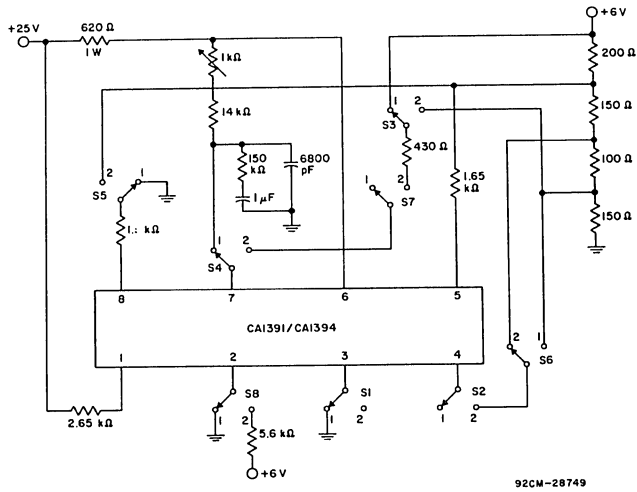


Fig.3 - DC test circuit.

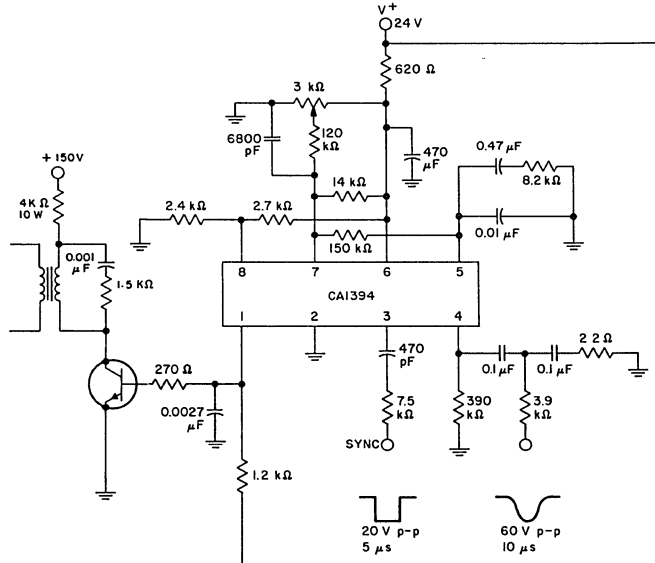


Fig.4 - Typical circuit application.

## Specifications CA1391, CA1394

### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ , Unless Otherwise Specified.

|  |                               |
|--|-------------------------------|
| DC Supply Current .....  | 40mA                          |
| DC Output Voltage .....  | 40V                           |
| DC Output Current .....  | 30mA                          |
| Sync Input Voltage .....   | 5V <sub>p-p</sub>             |
| Sawtooth Input Voltage .....   | 5V <sub>p-p</sub>             |
| Device Dissipation:  |                               |
| Up to $T_A = 25^\circ\text{C}$ .....   | 625mW                         |
| Above $T_A = 25^\circ\text{C}$ Derate Linearly .....                                   | 5mW/ $^\circ\text{C}$         |
| Ambient Temperature Range:   |                               |
| Operating .....  | 0 to +85 $^\circ\text{C}$     |
| Storage .....  | -65 to +150 $^\circ\text{C}$  |
| Lead Temperature (During Soldering):   |                               |
| At Distance 1/16 $\pm$ 1/32 in. (1.59 $\pm$ 0.79mm) from Case for 10 Seconds Max. .... | +260 $^\circ\text{C}$         |
| Thermal Resistance .....   | 200 $^\circ\text{C}/\text{W}$ |

### ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$ (See Fig.3)

| CHARACTERISTIC           | TEST CONDITIONS   | LIMITS |           |       | UNITS         |
|--------------------------|---|--------|-----------|-------|---------------|
|                          |   | Min.   | Typ.      | Max.  |               |
| Supply Voltage           | S1, S5, S6 = 2<br>S2, S3, S4, S7, S8 = 1<br>Measure term. 6 to Gnd  | 8      | —         | 9     | V             |
| Free-Running Frequency   | S1, S5, S6 = 2<br>S2, S3, S4, S7, S8 = 1<br>Counter to term. 1      | 14734  | —         | 16734 | Hz            |
| Output Leakage           | S2, S3, S6, S8 = 1<br>S1, S4, S5, S7 = 2<br>Measure term. 1 to 25 V | —      | 10        | —     | mV            |
| Output Saturation        | S2, S3, S5, S6, S8 = 1<br>S1, S4, S7 = 2<br>Measure term. 1 to Gnd  | —      | 60        | —     | mV            |
| Phase Detector Bias      | S2, S5, S6, S8 = 1<br>S1, S3, S4, S7 = 2<br>Measure term. 3 to Gnd  | —      | 1.9       | —     | V             |
| Phase Detector Leak      | S5, S8 = 1<br>S1, S2, S3, S4, S6, S7 = 2<br>Measure term. 5 to +4 V | -2     | —         | +2    | mV            |
| Phase Detector Low       | S1, S5, S8 = 1<br>S2, S3, S4, S6, S7 = 2<br>Measure term. 5 to +4 V | -0.55* | —         | —     | V             |
| Phase Detector High      | S1, S5, S6, S8 = 1<br>S2, S3, S4, S7 = 2<br>Measure term. 5 to +4 V | +0.55* | —         | —     | V             |
| Phase Detector Balance   | $V_{DET2} + V_{DET3}$   | -100   | —         | +100  | mV            |
| Sync Diode               | S1, S2, S3, S4, S6, S7 = 1<br>S5, S8 = 2                            | 0.3    | —         | 1.2   | V             |
| Static Phase Error       | See Fig.4   | —      | 0.5       | —     | $\mu\text{s}$ |
| Oscillator Pull-in Range |   | —      | $\pm 300$ | —     | Hz            |
| Oscillator Hold-in Range |   | —      | $\pm 900$ | —     | Hz            |

\* Polarity reversed in the CA1391.

## CA1391, CA1394

### CIRCUIT OPERATION

(See schematic diagram, Fig.2)

The CA1391 and CA1394 contain the oscillator, phase detector, and predriver sections necessary for the television horizontal oscillator and AFC loop.

The oscillator is an RC type with terminal 7 used to control the timing. If it is assumed that Q7 is initially off, then an external capacitor connected from terminal 7 to ground charges through an external resistance connected between terminals 6 and 7. As soon as the voltage at terminal 7 exceeds the potential set at the base of Q8 by resistors R11 and R12, Q7 turns on, and Q6 supplies base current to Q5 and Q10. Transistor Q5 discharges the capacitor through R4 until the base bias of Q7 falls below that of Q8, at which time, Q7 turns off, and the cycle repeats.

The sawtooth generated at the base of Q4 appears across R3 and turn off Q3 whenever the sawtooth voltage rises to a value that exceeds the bias set at terminal 8. By adjusting the potential at terminal 8, the duty cycle at the pre-drive output (terminal 1) may be changed.

The phase detector is isolated from the remainder of the circuit by R31, Z2, Q15 and Q16. The phase detector consists of the comparator Q22 and Q23, and the gated current source Q18. Negative-going sync pulses at terminal 3 turn off Q17, and the current division between Q22 and Q23 is then determined by the phase relationship of the sync and the sawtooth waveform at terminal 4, which is derived from the horizontal flyback pulse. If there is no phase difference between the sync and sawtooth, equal currents flow in the collectors of Q22 and Q23 during each half of the sync pulse period. The current in Q22 is turned around by current mirror Q20 and Q21 so that there is no net output current at terminal 5 for balanced conditions. When a phase offset occurs, current flows either in or out of terminal 5. In circuit applications, this terminal is connected to terminal 7 through an external low-pass filter, thereby controlling the oscillator.

Shunt regulation for the circuit is obtained by using a  $V_{BE}$  and zener multiplier. Resistors R13 and R14 multiply the  $V_{BE}$  of Q11, and the ratio of R15 and R16 multiplies the voltage of the zener diode Z1.

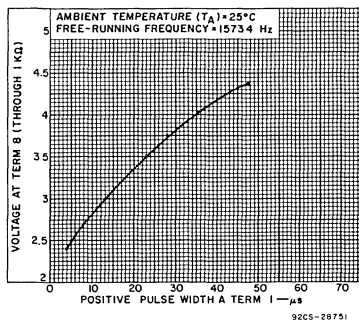


Fig.5 — Duty cycle at the pre-drive output (term.1) as it is affected by the input at term. 8.

August 1991

FM IF System

### Features

- For FM IF Amplifier Applications in High-Fidelity, Automotive, and Communications Receivers
- Includes: IF Amplifier, Quadrature Detector, AF Pre-amplifier, and Specific Circuits for AGC, AFC, Muting (Squelch), and Tuning Meter
- Exceptional Limiting Sensitivity ..... 12 $\mu$ V (Typ.) @ -3dB Point
- Low Distortion: (with Double-Tuned Coil) ..... 0.1% (Typ.)
- Single-Coil Tuning Capability
- High Recovered Audio ..... 400mV (Typ.)
- Provides Specific Signal for Control of Interchannel Muting (Squelch)
- Provides Specific Signal for Direct Drive of a Tuning Meter
- Provides Delayed AGC Voltage for RF Amplifier
- Provides a Specific Circuit for Flexible AFC
- Internal Supply-Voltage Regulators

### Description

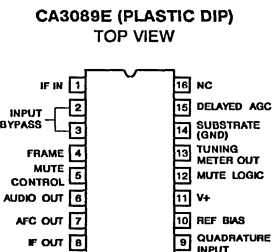
Harris CA3089E is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. Figure 1 is a block diagram showing the CA3089E features, which include a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as delayed AGC for the RF tuner, and AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5 to +16 volts.

The CA3089E is ideal for high-fidelity operation. Distortion in a CA3089E FM-IF System is primarily a function of the phase linearity characteristic of the outboard detector coil.

The CA3089E utilizes the 16-lead dual-in-line plastic package and can operate over the ambient temperature range of -40°C to +85°C.

### Pinout



### Block Diagram

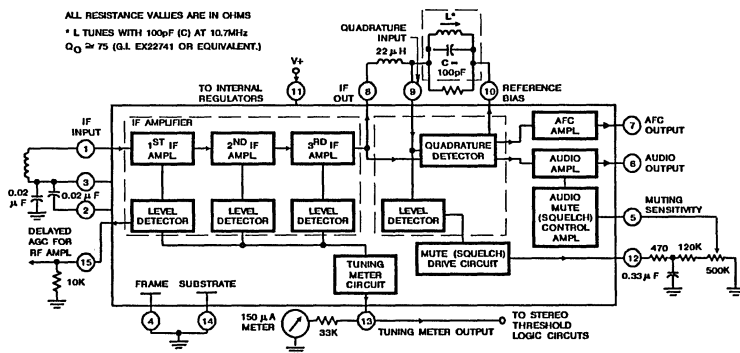


FIGURE 1. BLOCK DIAGRAM OF THE CA3089E

# CA3089

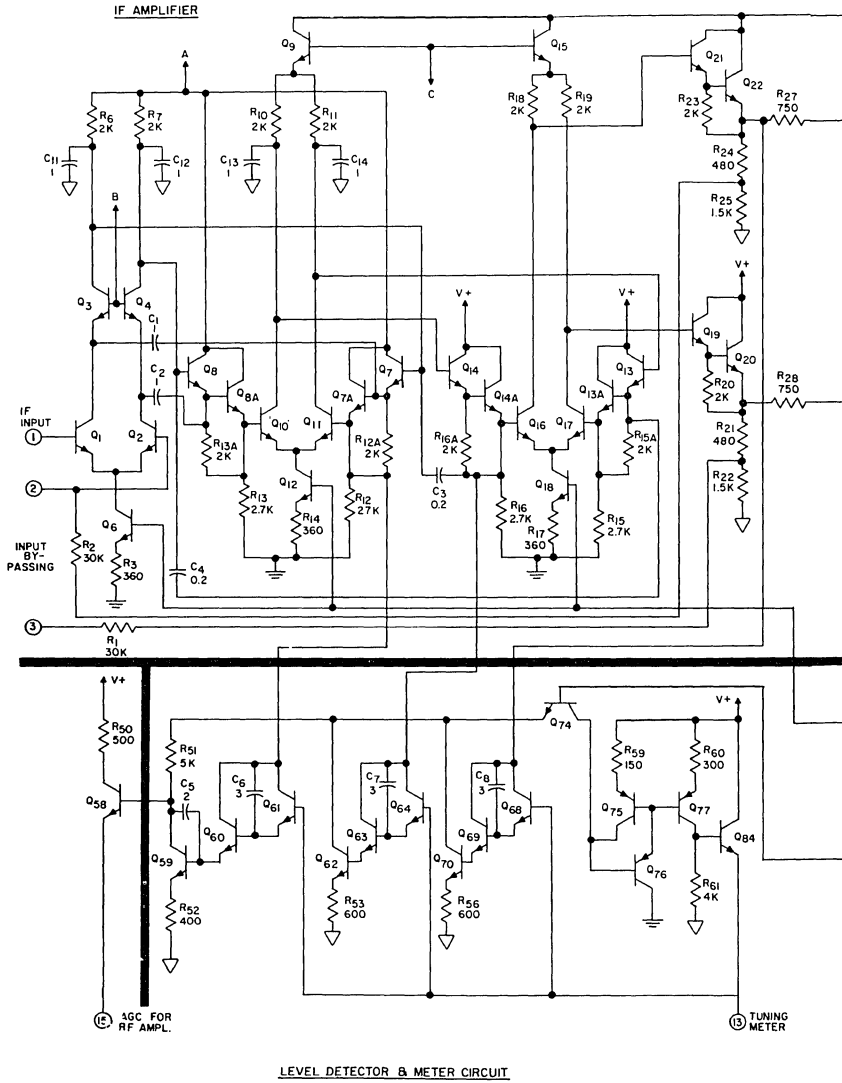


Fig. 2 - Schematic diagram of the CA3089E (cont'd on next page).



# CA3089

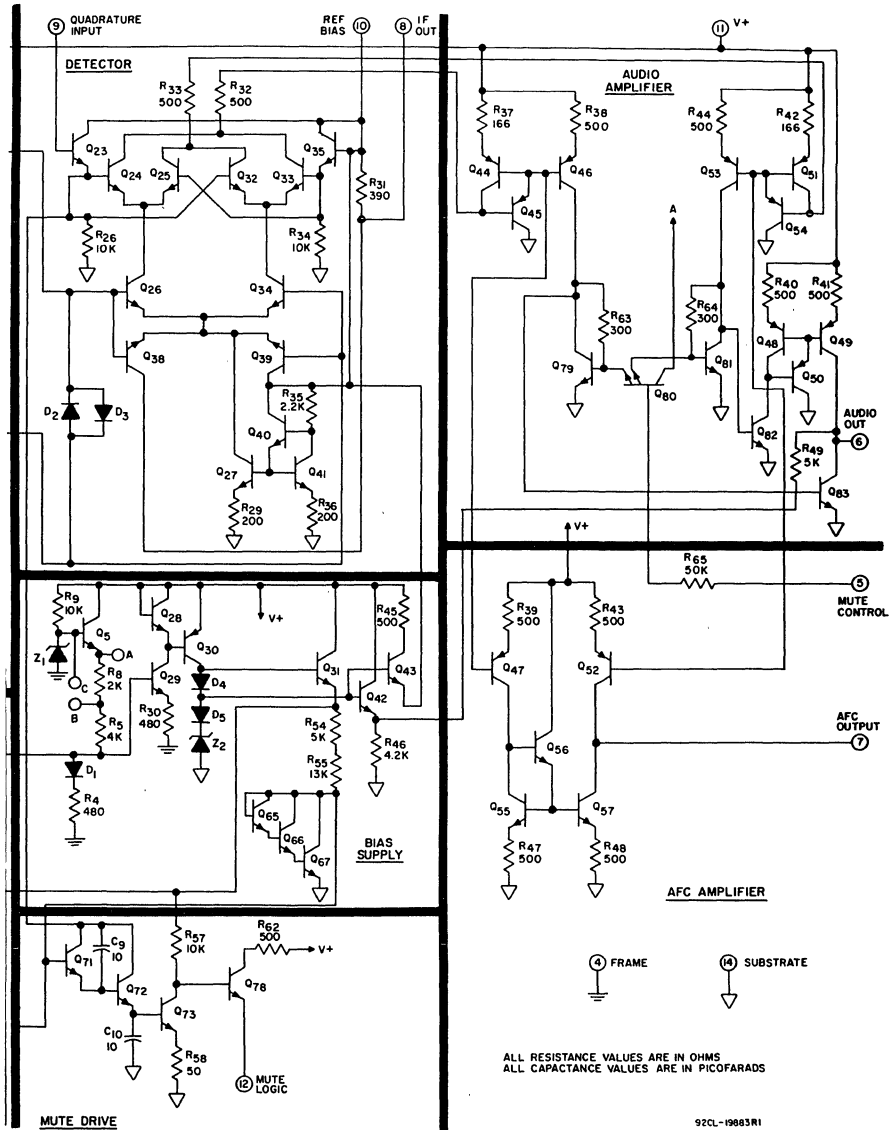


Fig. 2 - Schematic diagram of the CA3089E (cont'd from previous page).

# Specifications CA3089

## MAXIMUM RATINGS, Absolute Maximum Values

|  |                 |             |                      |
|--|-----------------|-------------|----------------------|
| DC Supply Voltage:   |                 |             |                      |
| Between Terminals 11 and 4   |                 | 16          | V                    |
| Between Terminals 11 and 14  |                 | 16          | V                    |
| DC Current (out of Terminal 15)  |                 | 2           | mA                   |
| Device Dissipation:  |                 |             |                      |
| Up to $T_A = 60^\circ\text{C}$   |                 | 600         | mW                   |
| Above $T_A = 60^\circ\text{C}$   | derate linearly | 6.7         | mW/ $^\circ\text{C}$ |
| Ambient Temperature Range:   |                 |             |                      |
| Operating  |                 | -40 to + 85 | $^\circ\text{C}$     |
| Storage  |                 | -65 to +150 | $^\circ\text{C}$     |
| Lead Temperature (During Soldering):                                   |                 |             |                      |
| At distance not less than 1/32" (0.79mm) from case for 10 seconds max. |                 | +265        | $^\circ\text{C}$     |

## ELECTRICAL CHARACTERISTICS, at $T_A = 25^\circ\text{C}$ , $V_+ = 12$ Volts (See Figs. 5 and 6)

| CHARACTERISTIC   | TEST CONDITIONS                           | LIMITS                      |      |      | UNITS         |   |
|--|---|-----------------------------|------|------|---------------|---|
|  |   | Min.                        | Typ. | Max. |               |   |
| <b>Static (DC) Characteristics</b>                         |   |                             |      |      |               |   |
| Quiescent Circuit Current                                  | No signal input,<br>Non muted             | 16                          | 23   | 30   | mA            |   |
| DC Voltages:   |   |                             |      |      |               |   |
| Terminal 1 (IF Input)                                      |   | 1.2                         | 1.9  | 2.4  | V             |   |
| Terminal 2 (AC Return to Input)                            |   | 1.2                         | 1.9  | 2.4  | V             |   |
| Terminal 3 (DC Bias to Input)                              |   | 1.2                         | 1.9  | 2.4  | V             |   |
| Terminal 6 (Audio Output)                                  |   | 5.0                         | 5.6  | 6.0  | V             |   |
| Terminal 10 (DC Reference)                                 | 5.0                                       | 5.6                         | 6.0  | V    |               |   |
| <b>Dynamic Characteristics</b>                             |   |                             |      |      |               |   |
| Input Limiting Voltage ( $-3$ dB point), $V_1$ (lim)       | —   | —                           | 12   | 25   | $\mu\text{V}$ |   |
| AM Rejection (Term. 6), AMR                                | $V_{IN} = 0.1\text{V}$ ,<br>AM Mod. = 30% | 45                          | 55   | —    | dB            |   |
| Recovered AF Voltage (Term. 6)<br>$V_O$ (AF)               | $f_O = 10.7\text{ MHz}$ ,                 | 300                         | 400  | 500  | mV            |   |
| Total Harmonic Distortion, THD:*<br>Single Tuned (Term. 6) | $V_{IN} = 0.1\text{ V}$                   | $f_{mod} = 400\text{ Hz}$ , | —    | 0.5  | 1.0           | % |
| Double Tuned (Term. 6)                                     |   |                             | —    | 0.1  | —             | % |
| Signal plus Noise to Noise Ratio (Term. 6)                 | Deviation = $\pm 75\text{ kHz}$           | 60                          | 67   | —    | dB            |   |

\*THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8,9, and 10.

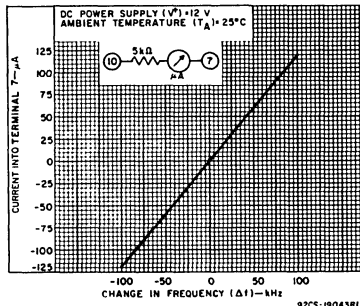


Fig. 3 — AFC characteristics (current at Term.7) as a function of change in frequency. (See test circuit Fig. 5.)

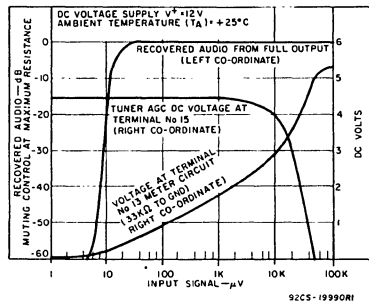
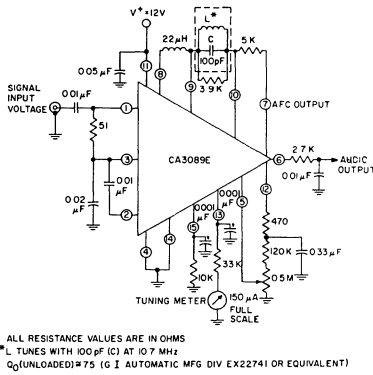


Fig. 4 — Muting action, tuner AGC, and tuning meter output as a function of input signal voltage. (See test circuit Fig.5.)

8  
SPECIAL  
ANALOG CIRCUITS

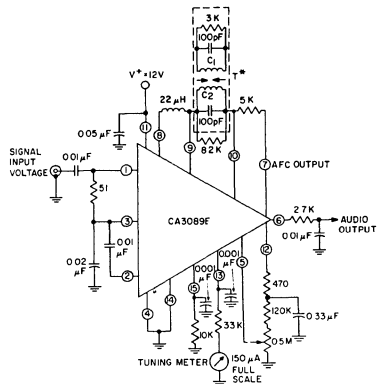
# CA3089



ALL RESISTANCE VALUES ARE IN OHMS  
 \* T TUNES WITH 100 pF (C) AT 10.7 MHz  
 Q<sub>1</sub>(UNLOADED) ≥ 75 (G I AUTOMATIC MFG DIV EX22741 OR EQUIVALENT)

92CM 104-411

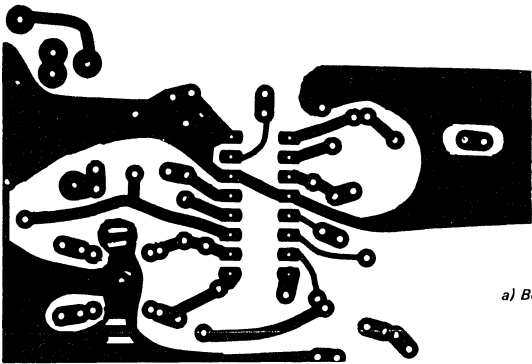
Fig. 5 — Test circuit for CA3089E using a single-tuned detector coil.



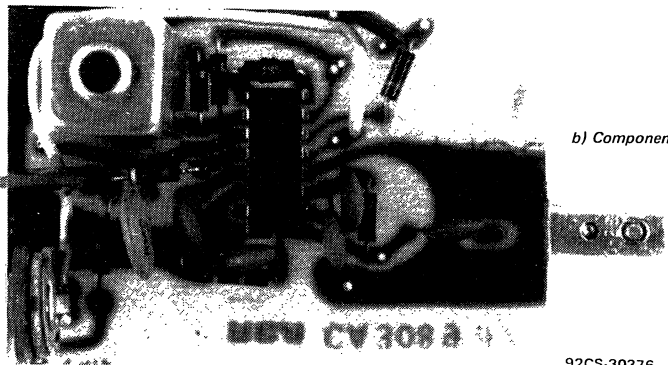
ALL RESISTANCE VALUES ARE IN OHMS  
 \* T PRI - Q<sub>1</sub>(UNLOADED) ≥ 75 (TUNES WITH 100 pF (C1) 201 of 34+ ON 7/32" DIA FORM SEC - Q<sub>2</sub>(UNLOADED) ≥ 75 (TUNES WITH 100 pF (C2) 201 of 34+ ON 7/32" DIA FORM 1% (PERCENT OF CRITICAL COUPLING) ≥ 70% (ADJUSTED FOR COIL VOLTAGE V<sub>C</sub>) = 150 mV  
 ABOVE VALUES PERMIT PROPER OPERATION OF MUTE (SQUELCH) CIRCUIT  
 \* E TYPE SLUGS, SPACING 4 mm

92CM 104-411

Fig. 6 — Test circuit for CA3089E using a double-tuned detector coil.



a) Bottom view of printed-circuit board.

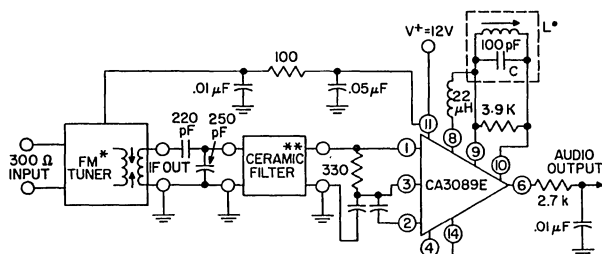


b) Component side — top view.

92CS-30376

Fig. 7 — Actual size photographs of the CA3089E and outboard components mounted on a printed-circuit board.

## CA3089



ALL RESISTANCE VALUES ARE IN OHMS

\* WALLER 4SN3FC OR EQUIVALENT

\*\* MURATA SFG 10.7 MA OR EQUIVALENT

• L TUNES WITH 100pF (C) AT 10.7 MHz  
 $Q_0$  UNLOADED=75 (G.I EX22741 OR EQUIVALENT)

92CS-19045

Performance data at  $f_0 = 98$  MHz,  $f_{MOD} = 400$  Hz,  
 Deviation =  $\pm 75$  kHz:

-3dB Limiting Sensitivity . . . . . 2 $\mu$ V (Antenna Level)  
 20dB Quieting Sensitivity . . . . . 1 $\mu$ V (Antenna Level)  
 30dB Quieting Sensitivity . . . . . 15 $\mu$ V (Antenna Level)

Fig. 8 - Typical FM tuner using the CA3089E  
 with a single-tuned detector coil.

August 1991

TV Chroma Processor

### Features

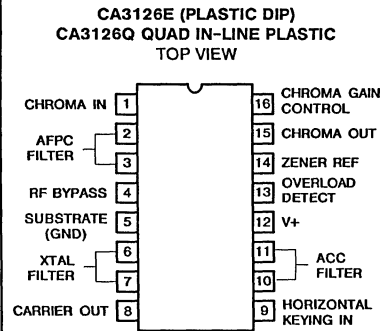
- Phase-Locked Subcarrier Regeneration Utilizes Sample-and-Hold Techniques
- Automatic Chrominance Control (ACC)/Killer Detector Employs Sample-and-Hold Techniques
- Supplementary ACC with an Overload Detector to Prevent Oversaturation of this Picture Tube
- Sinusoidal Subcarrier Output
- Keyed Chroma Output
- Emitter-Follower Buffered Outputs for Low Output Impedance
- Linear DC Saturation Control

### Description

Harris CA3126 is a monolithic silicon integrated circuit designed for chroma processing applications in color TV receivers. It is compatible with the CA3067 chroma demodulator as well as other chroma demodulators.

The CA3126 is supplied in a 16-lead dual-in-line plastic package (E Suffix) and in a 16-lead quad-in-line plastic package (Q Suffix).

### Pinout



### Block Diagram

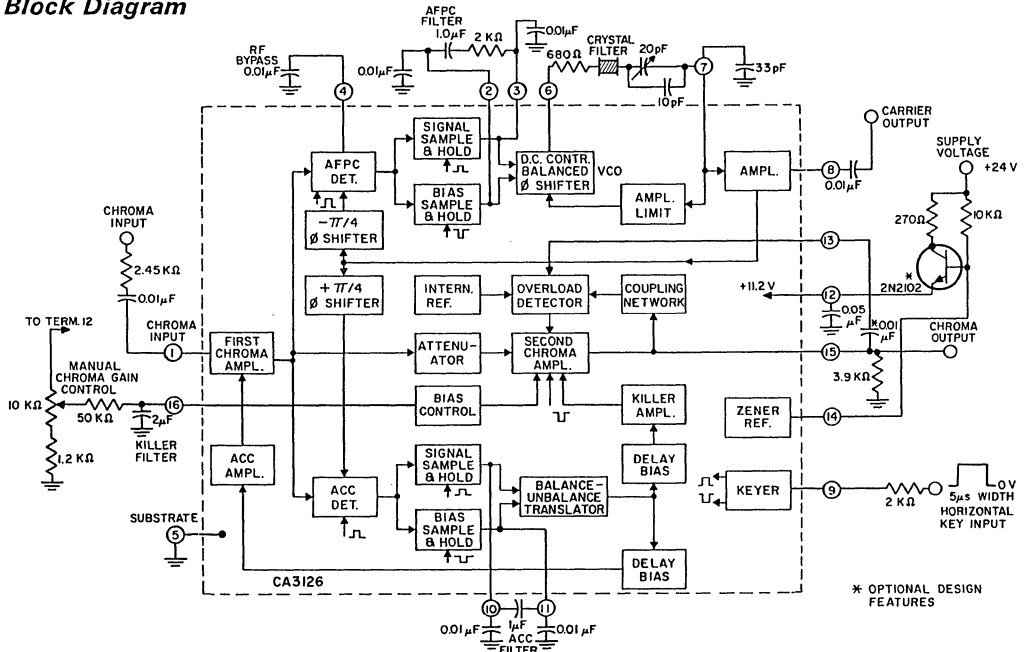


FIGURE 1. BLOCK DIAGRAM OF CA3126 TV CHROMA PROCESSOR

## Specifications CA3126

### MAXIMUM RATINGS, Absolute-Maximum Values at $T_A = 25^\circ\text{C}$

#### DEVICE DISSIPATION:

Up to  $T_A = 55^\circ\text{C}$  ..... 750 mW  
 Above  $T_A = 55^\circ\text{C}$  ..... derate linearly 7.9 mW/ $^\circ\text{C}$

DC SUPPLY VOLTAGE (Across Terms. 5 and 12)<sup>▲</sup> ..... 13.2 V

#### DC CURRENT:

Into Term. 12 ..... 38 mA  
 Into Term. 14 ..... 20 mA

#### DC VOLTAGE (Terminal 9):

Negative Rating ..... -5 V  
 Positive Rating ..... 3 V

#### AMBIENT TEMPERATURE RANGE:

Operating ..... -40 to +85 $^\circ\text{C}$   
 Storage ..... -65 to +150 $^\circ\text{C}$

#### LEAD TEMPERATURE (During Soldering):

At a distance not less than 1/32 in. (0.79 mm)  
 from case for seconds max. .... +265 $^\circ\text{C}$

<sup>▲</sup>This rating does not apply when using the internal zener reference in conjunction with an external pass transistor.

### ELECTRICAL CHARACTERISTICS

Test Conditions:  $T_A = 25^\circ\text{C}$ , chroma control at maximum position for all characteristics tests except for chroma output test.

For this test, control should be set at minimum position. Electrical characteristics referenced to test circuit, Fig.2.

| CHARACTERISTIC                              | TERMINAL, MEASUREMENT, AND SYMBOL | SWITCH POS. |    | CHROMA INPUT TP1 | LIMITS    |      |      | UNITS             |
|---|-----------------------------------|-------------|----|------------------|-----------|------|------|-------------------|
|   |                                   | S1          | S2 |                  | Min.      | Typ. | Max. |                   |
| <b>Static Characteristics</b>               |                                   |             |    |                  |           |      |      |                   |
| Voltage Regulator                           | $V_{12}$                          | 2           | 2  | 0                | 10.1      | 11.2 | 12.1 | V                 |
| Supply Current                              | $I_{12}$                          | 2           | 2  | 0                | 16        | 25   | 38   | mA                |
| <b>Dynamic Characteristics (See Note 1)</b> |                                   |             |    |                  |           |      |      |                   |
| Pull-in Range*                              | $V_8$                             | *           | 2  | 0.5 $V_{p-p}$    | $\pm 250$ | —    | —    | Hz                |
| Oscillator Output                           | $V_8$                             | 2           | 2  | 0                | 0.6       | 1.0  | —    | $V_{p-p}$         |
| 100% Chroma Output                          | $V_{15}$                          | 1           | 2  | 0.5 $V_{p-p}$    | 1.4       | 2.7  | —    | $V_{p-p}$         |
| Overload Detector                           | $V_{15}$                          | 1           | 1  | 0.5 $V_{p-p}$    | 0.4       | —    | 0.7  | $V_{p-p}$         |
| Minimum Chroma Output                       | $V_{15}$                          | 1           | 2  | 0.5 $V_{p-p}$    | —         | —    | 20   | $mV_{p-p}$        |
| 200% Chroma Output                          | $V_{15}$                          | 1           | 2  | 1 $V_{p-p}$      | 70        | 100  | 140  | % of 100% reading |
| 20% Chroma Output                           | $V_{15}$                          | 1           | 2  | 0.1 $V_{p-p}$    | 40        | —    | 105  |                   |
| Kill Level                                  | $V_{TP1}$                         | 1           | 2  | vary             | 5         | —    | 60   | $mV_{p-p}$        |

Note 1: Except for pull-in range testing, tune oscillator trimmer capacitor for free-running frequency of 3.579545 MHz  $\pm 10$  Hz.

\*Set Switch 1 to Position 2, detune oscillator  $\pm 250$  Hz, set Switch 1 to Position 1, and check for oscillator pull-in.

# CA3126

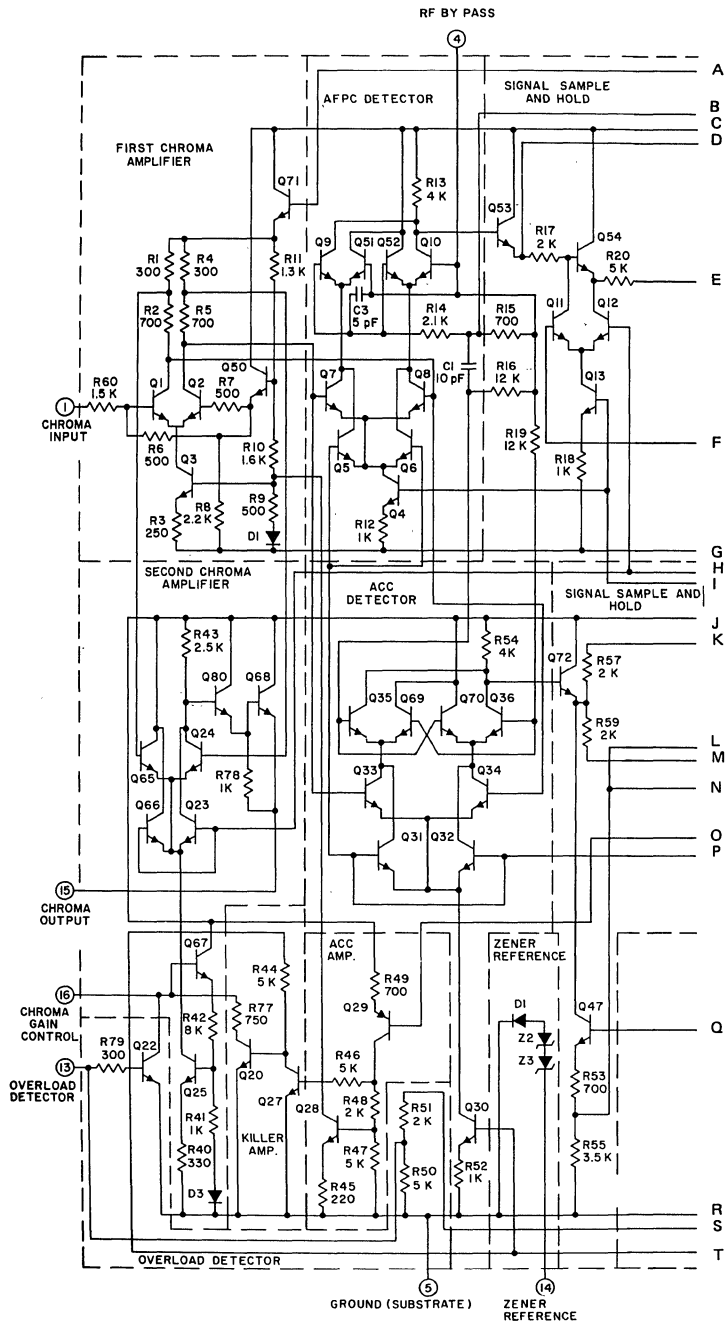


Fig. 2- Schematic diagram of the CA3126.

# CA3126

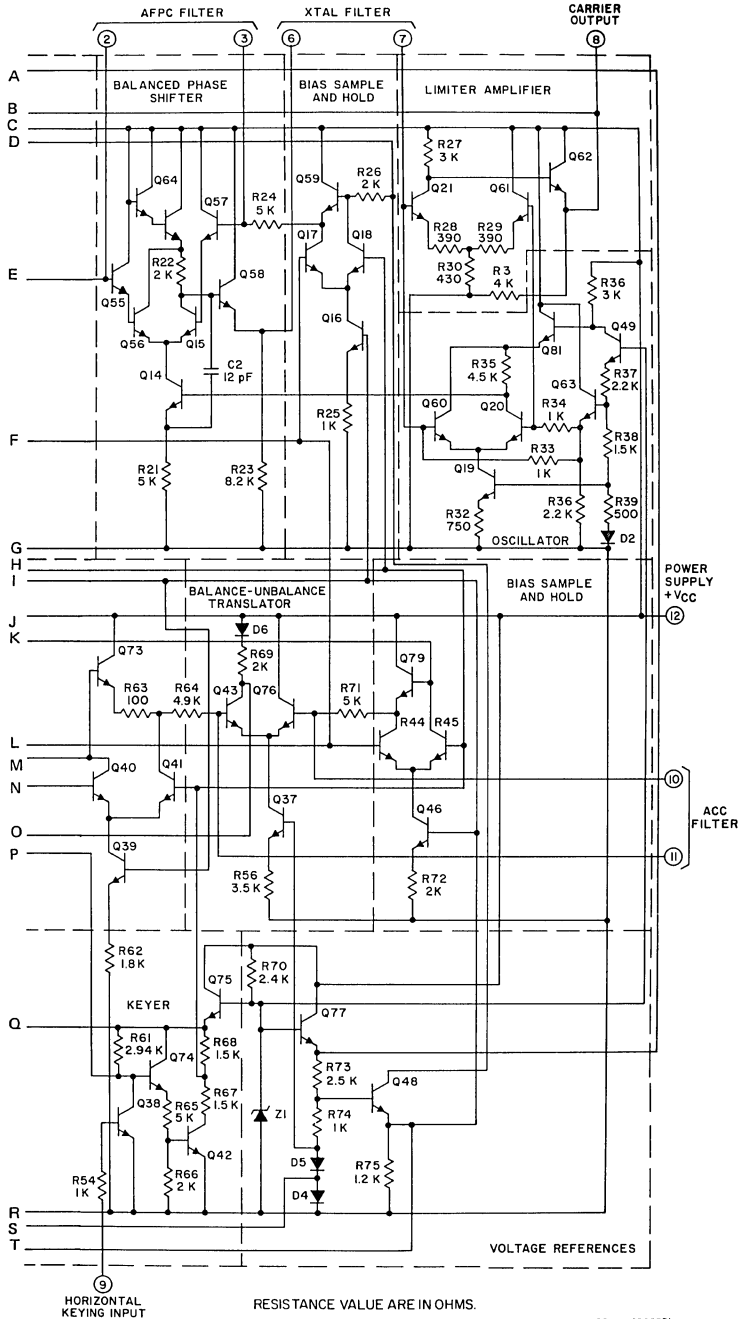


Fig. 2 — Schematic diagram of the CA3126 (cont'd).



# CA3126

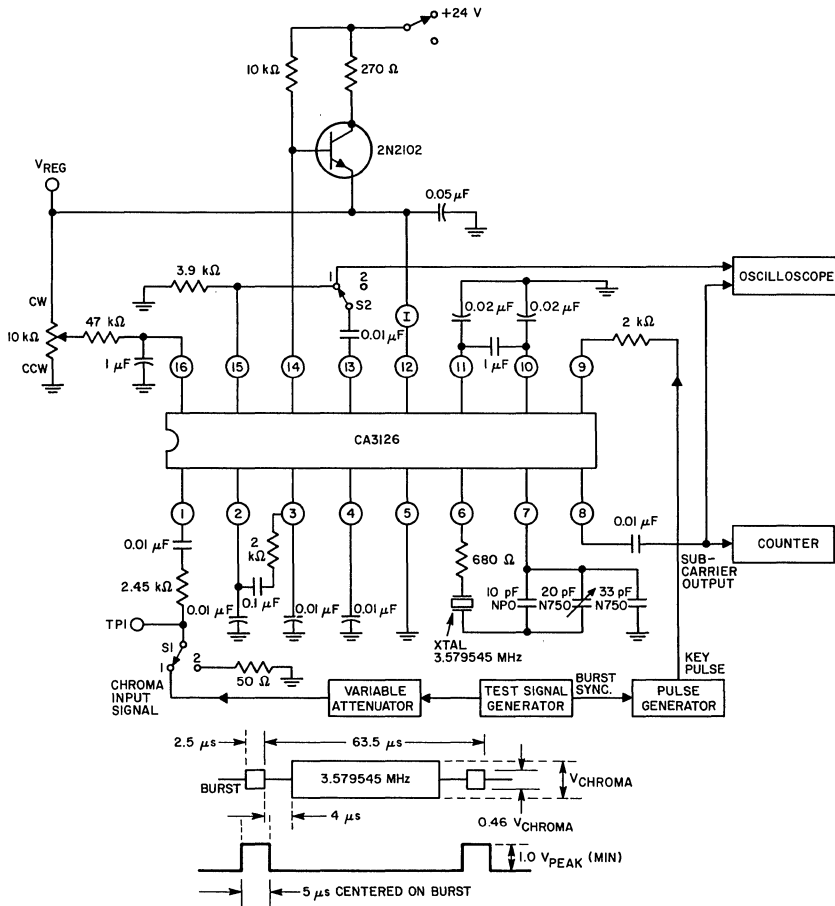


Fig. 3 — Test circuit for CA3126.

## CIRCUIT DESCRIPTION

The following paragraphs briefly describe the circuit operation of the CA3126 (shown in Figs. 1 and 2). A detailed description of the operation of various portions of the CA3126 is given in ICAN-6247, "Application of the CA3126 Chroma-Processing IC Using Sample-and-Hold Techniques".

The chroma input is applied to Terminal 1 through the desired band-shaping network. A 2,450-ohm resistor should be placed in series with Terminal 1 to minimize oscillator pickup in the first chroma amplifier. This amplifier supplies signals to the second chroma amplifier and to the ACC and AFPC detectors. The first chroma amplifier is gain-controlled by the ACC amplifier.

A horizontal keying pulse is applied to Terminal 9. This pulse must be present to ensure proper operation of the oscillator circuit. The subcarrier burst is sampled during the keying interval in the AFPC detector. The error voltage, produced at Terminal 2 and proportional to the burst phase, is compared to the quiescent bias voltage at Terminal 3 by the sample-and-hold circuitry. This "compared" voltage controls the phase-shifting network in the phase-locked loop. The operation of the AFPC loop is independent of any external adjustments or voltages except for an initial capacitor adjustment to set the free-running frequency.

## CA3126

The regenerated oscillator signal at Terminal 8 is applied internally to the AFPC and ACC detectors through +45- and -45-degree phase-shifter networks to establish the proper phase relationship for these detectors. The ACC detector, which also samples the burst during the keying interval, produces a correction voltage proportional to the burst amplitude. The correction voltage is compared to the quiescent bias level using sample-and-hold circuitry similar to that used in the AFPC portion of the circuit. The "compared" voltage is applied internally to the ACC amplifier and killer amplifier. Because the amplifier gains and killer threshold are determined by the ratios of the internal resistors, these functions are independent of external voltages or controls.

The attenuated chroma signal is fed to the second chroma amplifier, where the burst is removed by keyer action. The killer amplifier, the chroma gain control, and the overload detector control the action of the second chroma amplifier, whose gain is proportional to the dc voltage at Terminal 16. The overload detector (Terminal 13) receives a sample of the chroma output (Terminal 15) and detects the peak of the signal. The detected voltage is stored in an external capacitor connected to Terminal 16. This stored voltage on Terminal 16 affects the gain of the second chroma in the same manner as the chroma gain control.

### APPLICATIONS INFORMATION

#### General Considerations

The block diagram shown in Fig. 1 is typical of the type of circuit used in the practical application of the CA3126. Several items are critical for proper operation of the circuit.

1. A series resistor of approximately 2,450 ohms (or high source impedance) must be used at the chroma input. This high impedance minimizes pickup of unbalanced currents, particularly of the subcarrier oscillator signal.
2. When the overload detector is used, a large resistor (nominally 47,000 ohms) must be placed in series with Terminal 16 to set the required RC time constant. The same RC network series serves to set the killer time constant.
3. The setting of the free-running oscillator frequency requires the presence of the keying pulse. The free-running frequency will be erroneous if Terminal 1 is dc shorted during the setting operation because of the dc offset voltage introduced to the AFPC detector.
4. Care must be taken in PC board designs to provide reasonable isolation between the oscillator portion of the circuit (Terminals 6, 7, and 8) and the chroma input (Terminal 1).

#### Overload Detector

The overload detector accomplishes two purposes:

1. It prevents oversaturation due to low burst-to-chroma ratios.
2. It prevents overload conditions due to noise.

Both of these conditions are discussed in more detail in ICAN-6247. The extent to which the overload detector is used depends upon the individual receiver design goals. If greater than 0.5-volt peak-to-peak output is desired, the chroma output at Terminal 15 can be tapped to yield any desired degree of overload detector action.

#### Chroma Gain Control

The chroma gain control operates by varying the base bias on current source transistor Q25. To ensure proper temperature tracking of the chroma gain control, it is essential that the control be operated from a supply source derived from the reference voltage at Terminal 12. Because the control operates from a current source, chroma gain is much more predictable and far less temperature sensitive than controls that steer current by means of a differential amplifier. The typical chroma gain characteristic for the CA3126 is shown in Fig. 4.

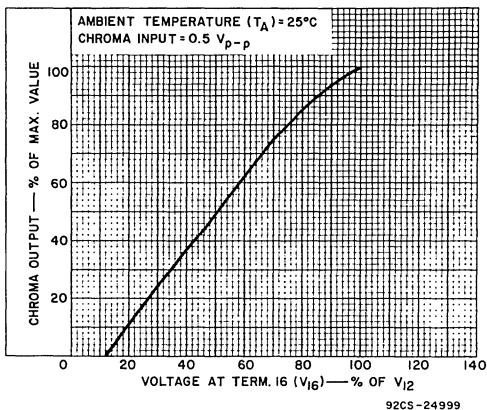


Fig. 4—Chroma gain control.

#### Subcarrier Regenerator Oscillator

The oscillator filter consists of a 3.579545-MHz crystal, a 680-ohm resistor, and a 10-pF capacitor connected in series across Terminals 6 and 7. A 33-pF capacitor, shunt connected from Terminal 7 to ground, rolls off higher-order harmonics, thereby preventing oscillation at the crystal third-harmonic frequency. A curve of the typical static phase error as a function of the free-running oscillator frequency is shown in Fig. 5. It should be noted that the slope of the curve determines the dc gain of the phase-locked loop, i.e., 40 Hz per degree.

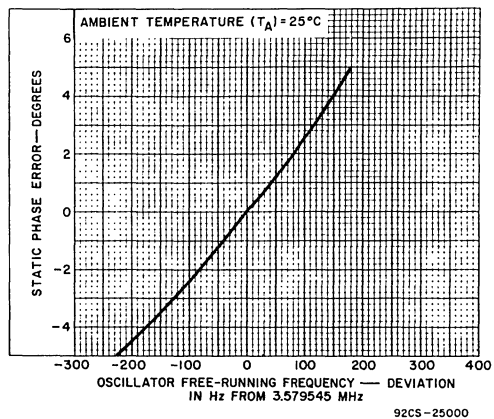


Fig. 5—Static phase error.

# CA3126

## Thermal Considerations

The circuit of the CA3126 is thermally compensated to achieve the optimal operating characteristics over the normal operating temperature range of TV receivers. Figs. 6 and 7 show the oscillator- and chroma-output amplitudes and phases as a function of temperature (Terminals 8 and 15), respectively.

Both the oscillator- and chroma-output amplitudes and phases are measured relative to the chroma-input phase. The performance of the oscillator free-running frequency as a function of temperature is shown in Fig. 8. All the temperature plots are characteristic of the test circuit with the indicated component types and values given in Fig. 3.

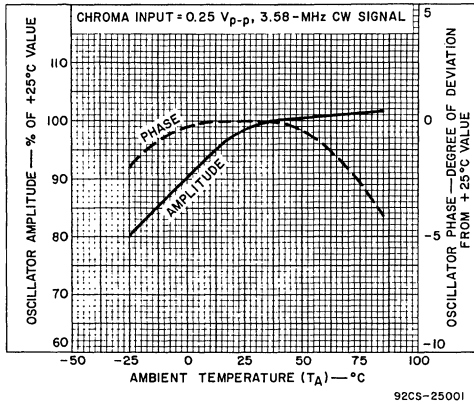


Fig. 6—Amplitude and phase variations of oscillator output vs. temperature.

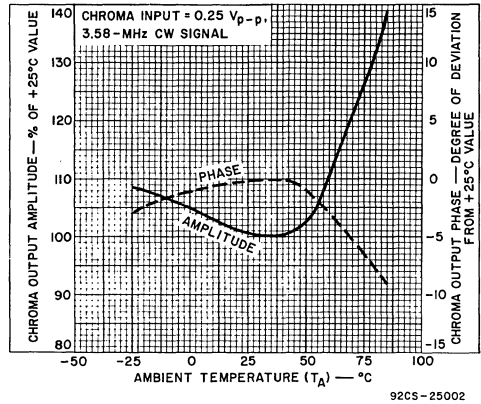


Fig. 7—Amplitude and phase variations of chroma output vs. temperature.

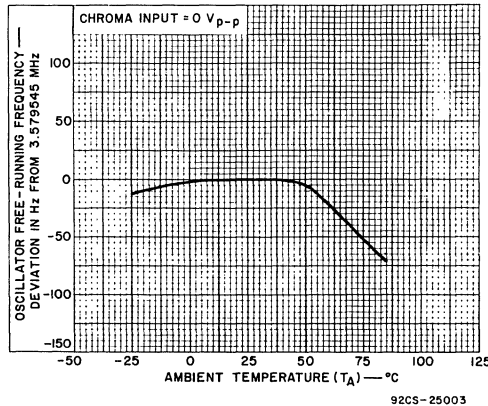


Fig. 8—Variation of oscillator free-running frequency vs. temperature.

### Features

- Includes IF Amplifier, Quadrature Detector, AF Pre-amplifier, and Specific Circuits for AGC, AFC, Tuning Meter, Deviation-Noise Muting, and ON Channel Detector
- For FM IF Amplifier Applications in High-Fidelity, Automotive, and Communications Receivers
- Exceptional Limiting Sensitivity ..... 12 $\mu$ V (Typ.) @-3dB Point
- Low Distortion ..... 0.1% (Typ.) (with Double-Tuned Coil)
- Single-Coil Tuning Capability
- Improved S + N/N Ratio
- Externally Programmable Recovered Audio Level
- Provides Specific Signal for Control of Interchannel Muting (Squelch)
- Provides Specific Signal for Direct Drive of a Tuning Meter
- On Channel Step for Search Control
- Provides Programmable AGC Voltage for RF Amplifier
- Provides a Specific Circuit for Flexible Audio Output
- Internal Supply-Voltage Regulators
- Externally Programmable "On" Channel Step Width, and Deviation at Which Muting Occurs

### Description

The Harris CA3189E\* is a monolithic integrated circuit that provides all the functions of a comprehensive FM-IF system. Figure 1 shows a block diagram of the CA3189E, which includes a three-stage FM-IF amplifier/limiter configuration with level detectors for each stage, a doubly-balanced quadrature FM detector and an audio amplifier that features the optional use of a muting (squelch) circuit.

The advanced circuit design of the IF system includes desirable deluxe features such as programmable delayed AGC for the RF tuner, an AFC drive circuit, and an output signal to drive a tuning meter and/or provide stereo switching logic. In addition, internal power-supply regulators maintain a nearly constant current drain over the voltage supply range of +8.5 to +16 Volts.

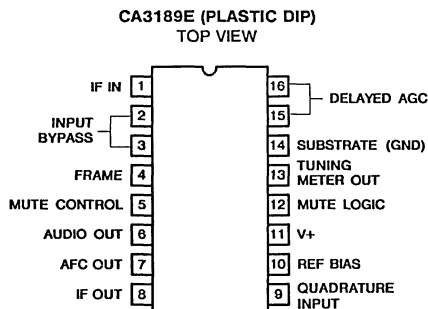
The CA3189E is ideal for high-fidelity operation. Distortion in a CA3189E FM-IF System is primarily a function of the phase linearity characteristic of the onboard detector coil.

The CA3189E has all the features of the CA3089E plus additions. See CA3189E features compared to the CA3089E in Table 1.

The CA3189E utilizes the 16-lead dual-in-line plastic package and can operate over the ambient temperature range of -40°C to +85°C.

\*Formerly Developmental Type No. TA10038.

### Pinout



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$

|  |                             |
|--|-----------------------------|
| DC Supply Voltage                            | 16V                         |
| (Between Terms. 11 and 4).....               | 16V                         |
| (Between Terms. 11 and 14) .....             | 2mA                         |
| DC Current (Out of Term. 15).....            | 640mW                       |
| Device Dissipation:                          | Derate Linearly at 9.9mW/°C |
| Up to $T_A = 85^\circ\text{C}$ .....         | -40 to +85°C                |
| Above $T_A = 85^\circ\text{C}$ .....         | -65 to +150°C               |
| Ambient Temperature Range                    |                             |
| Operating .....                              |                             |
| Storage .....                                |                             |
| Lead Temperature (During Soldering):         |                             |
| At Distance Not Less Than 1/32 Inch (0.79mm) |                             |
| from Case for 10s Max.....                   | +265°C                      |

**8**  
 SPECIAL  
 ANALOG CIRCUITS

## Specifications CA3189

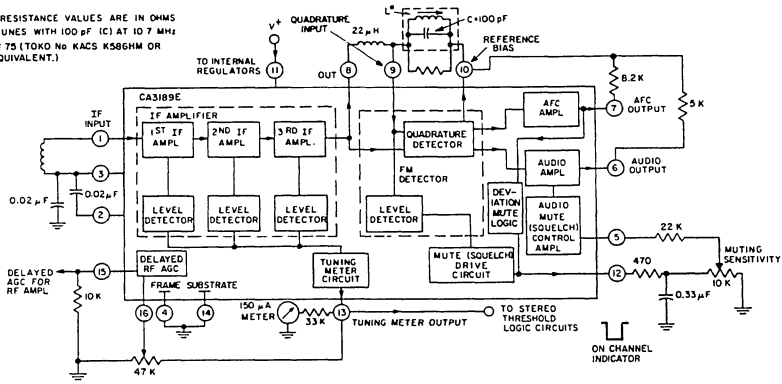
ELECTRICAL CHARACTERISTICS, at  $T_A = 25^\circ\text{C}$ ,  $V^+ = 12$  Volts

| CHARACTERISTIC  | SYMBOL            | TEST CONDITIONS                             |  | LIMITS |  |          | UNITS         |     |
|---|-------------------|---|--|--------|--|----------|---------------|-----|
|   |                   |   | Circuit or Fig. No.  | Min.   | Typ.                                   | Max.     |               |     |
| <b>Static (DC) Characteristics</b>                    |                   |   |  |        |  |          |               |     |
| Quiescent Circuit Current                             | $I_{11}$          | No signal input,<br>Non muted               | 3,4  | 20     | 31                                     | 40       | mA            |     |
| DC Voltages:<br>Terminal 1 (IF Input)                 | $V_1$             |   |  | 1.2    | 1.9                                    | 2.4      | V             |     |
| Terminal 2 (AC Return to Input)                       | $V_2$             |   |  | 1.2    | 1.9                                    | 2.4      | V             |     |
| Terminal 3 (DC Bias to Input)                         | $V_3$             |   |  | 1.2    | 1.9                                    | 2.4      | V             |     |
| Terminal 15 (RF AGC)                                  | $V_{15}$          |   |  | 7.5    | 9.5                                    | 11       | V             |     |
| Terminal 10 (DC Reference)                            | $V_{10}$          |   |  | 5      | 5.6                                    | 6        | V             |     |
| <b>Dynamic Characteristics</b>                        |                   |   |  |        |  |          |               |     |
| Input Limiting Voltage (-3 dB point)                  | $V_I(\text{lim})$ |   |  | -      | 12                                     | 25       | $\mu\text{V}$ |     |
| AM Rejection (Term. 6)                                | AMR               | $V_{IN} = 0.1 \text{ V}$ ,<br>AM Mod. = 30% | $f_0 = 10.7 \text{ MHz}$ ,   | 3,4    | 45                                     | 55       | -             | dB  |
| Recovered AF Voltage (Term. 6)                        | $V_O(\text{AF})$  |   |  |        | 325                                    | 500      | 650           | mV  |
| Total Harmonic Distortion:*<br>Single Tuned (Term. 6) | THD               | $V_{IN} = 0.1 \text{ V}$                    | $f_{\text{mod.}} = 400 \text{ Hz}$ ,<br>Deviation $\pm 75 \text{ kHz}$ | 3      | -                                      | 0.5      | 1             | %   |
| Double Tuned (Term. 6)                                | THD               |   |  |        | -                                      | 0.1      | -             | %   |
| Signal plus Noise to Noise Ratio (Term. 6)            | S + N/N           |   |  |        | 3,4                                    | 65       | 72            | -   |
| Deviation Mute Frequency                              | $f_{\text{DEV.}}$ |   | $f_{\text{mod.}} = 0$  | 3,6,7  | -                                      | $\pm 40$ | -             | kHz |
| RF AGC Threshold                                      | $V_{16}$          |   |  | 3,4    | -                                      | 1.25     | -             | V   |
| On Channel Step                                       | $V_{12}$          | $V_{IN} = 0.1 \text{ V}$                    | $f_{\text{DEV.}} < \pm 40 \text{ kHz}$                                 | 3      | -                                      | 0        | -             | V   |
|   |                   |   |  |        | $f_{\text{DEV.}} > \pm 40 \text{ kHz}$ | -        | 5.6           | -   |

\*THD characteristics are essentially a function of the phase characteristics of the network connected between terminals 8, 9, and 10.

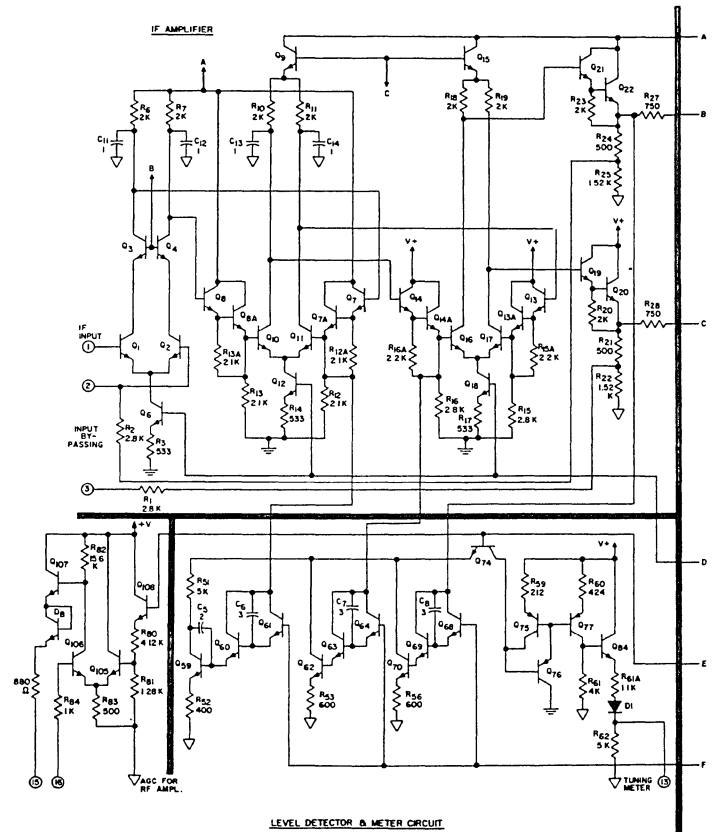
# CA3189

ALL RESISTANCE VALUES ARE IN OHMS  
 \* L TUNES WITH 100 pF ICT AT 10.7 MHz  
 Q<sub>D</sub> = 75 (10K) NO KACS K586HM OR  
 EQUIVALENT.)



92CM-29951

Fig. 1 - Block diagram of the CA3189E.



92CL-29952

Fig. 2 - Schematic diagram of the CA3189E (cont'd on next page).

8  
 SPECIAL  
 ANALOG CIRCUITS

# CA3189

TABLE I – CA3189E Features Compared to CA3089E

| FEATURES  | CA3189E | CA3089E |
|---|---------|---------|
| Low Limiting Sensitivity (12 $\mu$ V typ.)              | Yes     | Yes     |
| Low Distortion  | Yes     | Yes     |
| Single-coil Tuning Capability                           | Yes     | Yes     |
| Programmable Audio Level                                | Yes     | No      |
| S/N Mute  | Yes     | Yes     |
| Deviation Mute  | Yes     | No      |
| Flexible AFC  | Yes     | Yes     |
| Programmable AGC Threshold and Voltage                  | Yes     | No      |
| Typical S + N/N > 70 dB                                 | Yes     | No      |
| Meter Drive Voltage Depressed at Very-Low Signal Levels | Yes     | No      |
| On-Channel Step Control Voltage                         | Yes     | No      |

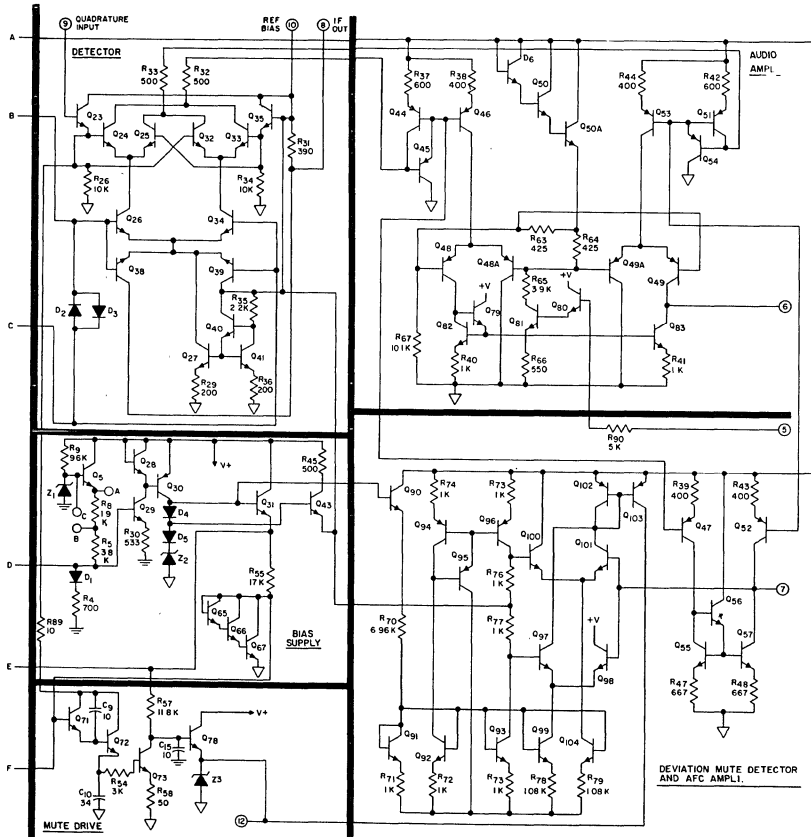
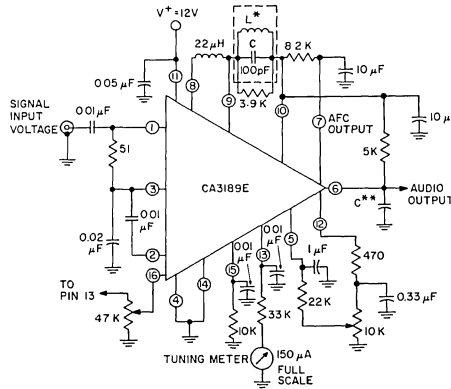


Fig. 2 - Schematic diagram of the CA3189E (cont'd from previous page).

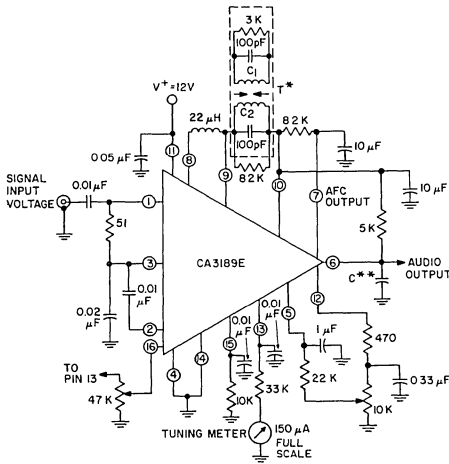
# CA3189



ALL RESISTANCE VALUES ARE IN OHMS  
 \*L TUNES WITH 100 pF (C) AT 10.7 MHz  
 $Q_0$ (UNLOADED)  $\approx$  75 (TOKO No KACS K56HM OR EQUIVALENT)  
 \*C = 0.01  $\mu$ F FOR 50  $\mu$ S DEEMPHASIS (EUROPE)  
 = 0.015  $\mu$ F FOR 75  $\mu$ S DEEMPHASIS (USA)

92CM-29953

Fig. 3 - Test circuit for CA3189E using a single-tuned detector coil.



ALL RESISTANCE VALUES ARE IN OHMS  
 \*T: PRI. -  $Q_0$ (UNLOADED)  $\approx$  75 (TUNES WITH 100 pF (C1) 201 OF 34e ON 7/32" DIA. FORM)  
 SEC. -  $Q_0$ (UNLOADED)  $\approx$  75 (TUNES WITH 100 pF (C2) 201 OF 34e ON 7/32" DIA. FORM)  
 k (PERCENT OF CRITICAL COUPLING)  $\approx$  70%  
 (ADJUSTED FOR COIL VOLTAGE  $V_C$ ) = 150 mV  
 ABOVE VALUES PERMIT PROPER OPERATION OF MUTE (SQUELCH) CIRCUIT  
 \*E" TYPE SLUGS, SPACING 4mm  
 \*C = 0.01  $\mu$ F FOR 50  $\mu$ S DEEMPHASIS (EUROPE)  
 = 0.015  $\mu$ F FOR 75  $\mu$ S DEEMPHASIS (USA)

Fig. 4 - Test circuit for CA3189E using a double-tuned detector coil.

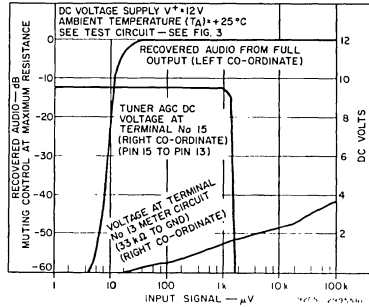


Fig. 5 - Muting action, tuner AGC, and tuning meter output as a function of input signal voltage.

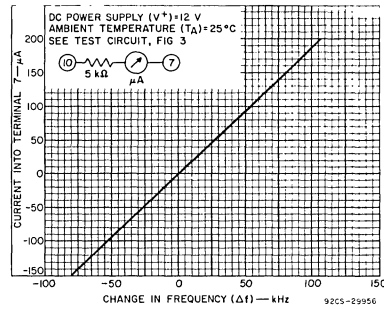


Fig. 6 - AFC characteristics (current at Term. 7 as a function of change in frequency).

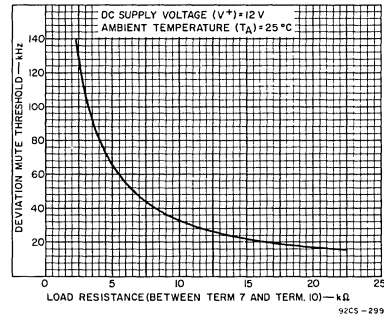


Fig. 7 - Deviation mute threshold as a function of load resistance (between Term. 7 and Term. 10).

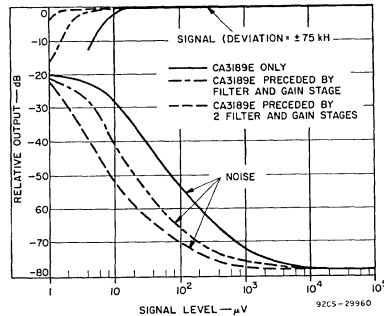
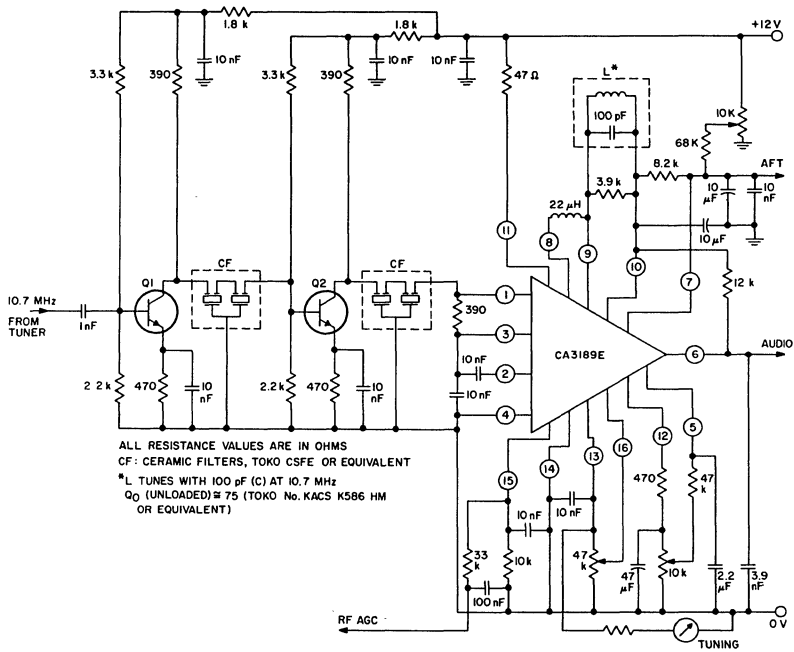


Fig. 8 - Typical limiting and noise characteristics.



# CA3189



ALL RESISTANCE VALUES ARE IN OHMS  
 CF: CERAMIC FILTERS, TOKO CSFE OR EQUIVALENT  
 \*L TUNES WITH 100 pF (C) AT 10.7 MHz  
 Q<sub>0</sub> (UNLOADED) ≈ 75 (TOKO No. KACS K586 HM  
 OR EQUIVALENT)

Fig. 9 – Complete FM IF system for high-quality receivers.

92CL-29958B1

## Single Chip PAL Luminance/Chroma Processor

August 1991

### Features

- All PAL Luminance and Chrominance Processing Circuitry on a Single Chip in a 24-Lead Plastic Package
- Phase-Locked Subcarrier Regeneration Utilizing Sample-and-Hold
- DC Controls for Brightness, Contrast, and Color-Saturation Functions
- Input for Average Beam-Current Limiting
- Contrast Control Having Excellent Tracking of Luma and Chroma Channels
- Low-Impedance RGB Outputs with Excellent Tracking for Direct Coupling to Video Driver Circuitry

### Description

The Harris CA3194E\* is a silicon monolithic integrated circuit designed to perform all of the signal processing functions for both the chroma and luminance signals of PAL color television receivers.

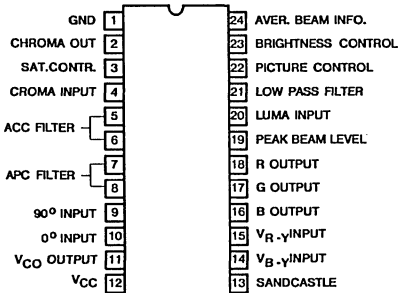
This circuit performs all the functions needed between the video detector and the video RGB output stages. DC contrast, brightness, and saturation controls and average beam limiting functions are included. The RGB buffer stages are capable of delivering 5mA of current into the video output stages.

The CA3194E is supplied in the 24-lead dual-in-line plastic package.

\* Formerly RCA Dev. No. TA10313.

### Pinout

CA3194E (PLASTIC DIP)  
TOP VIEW



TERMINAL VOLTAGE AND CURRENT RATINGS

| TERMINAL | VOLTAGE* - V |      | CURRENT - mA    |                  |
|----------|--------------|------|-----------------|------------------|
|          | MIN.         | MAX. | I <sub>IN</sub> | I <sub>OUT</sub> |
| 1        | -            | -    | -               | -                |
| 2        | 0            | 13   | 0               | 30               |
| 3        | 0            | 8    | 10              | -                |
| 4        | 0            | 5    | -               | -                |
| 5        | 0            | Note | -               | -                |
| 6        | -            | -    | 0.1             | 0.5              |
| 7        | 0            | Note | -               | -                |
| 8        | 0            | Note | -               | -                |
| 9        | 0            | 8    | -               | -                |
| 10       | 0            | 8    | -               | 0.7              |
| 11       | 0            | 13   | -               | 10               |
| 12       | 0            | 13   | -               | -                |
| 13       | 0            | 12   | -               | -                |
| 14       | 0            | 5    | -               | 1.5              |
| 15       | 0            | 5    | -               | 1.5              |
| 16       | 0            | 13   | -               | 10               |
| 17       | 0            | 13   | -               | 10               |
| 18       | 0            | 13   | -               | 10               |
| 19       | 0            | Note | -               | -                |
| 20       | 0            | 5    | -               | -                |
| 21       | 0            | Note | -               | -                |
| 22       | 0            | 8    | -               | -                |
| 23       | 0            | 5    | -               | -                |
| 24       | 0            | 12   | -               | -                |

NOTE: The maximum should not exceed the V<sub>CC</sub> voltage. Voltage with respect to Terminal 1 for V<sub>CC</sub> (Terminal 12) of 12V ±10%.

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SPECIAL  
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**Circuit Description** (See Figures 1 and 6)

The chroma signal is externally separated from the video signal by means of a bandpass or high-pass filter and applied to pin 4. The burst is separated in the first chroma stage and applied to the synchronous detector which provides information to sample-and-hold circuits for APC (phase-locked loop), ACC (automatic chroma gain control) and identification and killing. The 4.43-MHz crystal oscillator is phase-locked to the burst and provides 0° and 90° (via an external phase shifter) carriers to the chroma demodulators. The burst and chroma amplitude at the output of the first chroma amplifier is kept constant by the automatic gain control.

The second chroma stage provides saturation control (pin 3) which tracks the contrast control in the luminance channel. This stage is also used for color killing.

A buffer stage drives the external PAL delay line. The separated U and V signals are applied to pins 14 and 15, respectively, and demodulated. A standard G-Y matrix is included on the chip.

The luminance signal passes through the subcarrier trap and through the luminance delay line and enters the chip at pin 20. Contrast and brightness control is provided before the luminance signal is combined with the color difference signals in the Y matrix. Average and peak beam limiting circuits are controlled from pins 24 and 19.

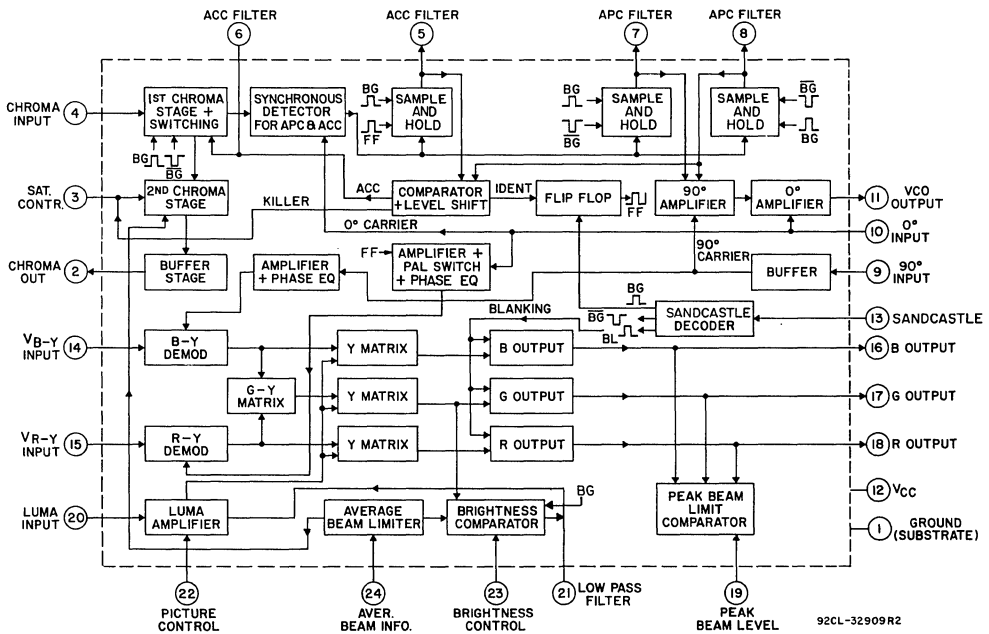


Fig. 1 - Block diagram.

## Specifications CA3194

### Absolute Maximum Ratings

#### DC Supply Voltage and Current:

|                            |                         |
|----------------------------|-------------------------|
| Pin 12 Voltage Range ..... | 11 Min. to 13 Max. V    |
| Pin 12 Current Range ..... | 44 (Typ.) to 60 Max. mA |

#### Device Dissipation:

|  |   |
|--|---|
| Up to $T_A = 25^\circ\text{C}$ .....   | 825mW                                     |
| Above $T_A = 25^\circ\text{C}$ .....   | Derate Linearly @ 8.7mW/ $^\circ\text{C}$ |
| $\theta_{JC}$ Max. = 115 $^\circ\text{C}/\text{W}$ , $T_J$ Max. = 150 $^\circ\text{C}$ |   |

#### Ambient Temperature Range:

|                 |                              |
|-----------------|------------------------------|
| Operating ..... | -40 to +85 $^\circ\text{C}$  |
| Storage .....   | -65 to +150 $^\circ\text{C}$ |

#### Lead Temperature (During Soldering):

|  |                       |
|--|-----------------------|
| At Distance 1/16 ± 1/32 in. (1.59 ± 0.79mm) from Case for 10 Seconds Max. .... | +265 $^\circ\text{C}$ |
|--|-----------------------|

**Electrical Characteristics**  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 12\text{V}$ ,  $V_S = 2.85\text{V}$ ,  $V_C = 2.85\text{V}$ ,  $V_{AB} = V_{PB} = V_{CC}$ ,  $V_B$  adjusted for  $V_{18} = 6.3\text{V}$ ,  $C_X$  adjusted for  $F_{OSC} = 4.43361875\text{MHz}$ , Sandcastle:  $V_{BG} = 8.0\text{V}$ ,  $V_{BLANK} = 3.5\text{V}$ —Burst Gate centered on Burst. These conditions exist except as otherwise noted. See Figure 5 for test circuit.

| CHARACTERISTIC                         | TEST CONDITIONS   | TYPICAL VALUE         | UNITS            |
|--|---|-----------------------|------------------|
| <b>LUMINANCE SECTION</b>               |   |                       |                  |
| Input Impedance—Term. 20               |   | 6<br>5                | k $\Omega$<br>pF |
| Luminance Channel Input Voltage        | Luma Input Signal=30% Sync  | 0.5                   | $V_{p-p}$        |
| Bandwidth of Luminance Channel         | Luma Input Signal: 0.5 $V_{p-p}$ (30% Sync) modulated CW<br>Adj. modulation frequency for -3 dB at color outputs  | 8                     | MHz              |
| Brightness Control Range—Term. 23      | For control characteristics, See Fig. A   | 0 - 3.5               | V dc             |
| Output Black Level:<br>Range<br>Offset | Luma Input Signal: 0.5 $V_{p-p}$ (30% Sync)<br>$V_B$ 0 - 5 V<br>Measured at Pin 18 black level. See Fig. A.   | 5.9 - 9.7<br>0.6 Max. | V dc             |
| Contrast Control Range—Term. 22        | Luminance input: 0.5 $V_{p-p}$ (30% Sync), for control characteristics. See Fig. B.   | 0 - 5                 | V dc             |
| Luminance Gain Control Range           | Luminance Input: 0.5 $V_{p-p}$ (30% Sync),<br>$V_C=0.5 - 5$ V measure Pin 18 black level to maximum white level. See Fig. C.  | 32                    | dB               |
| RGB Output Swing                       | Luminance Input: 0.5 $V_{p-p}$ (30% Sync), $V_C=5$ V, read black level to peak white. See Fig. D.   | 4                     | $V_{p-p}$        |
| <b>CHROMINANCE SECTION</b>             |   |                       |                  |
| Input Impedance—Term. 4                | See Fig. E.   | 4.5<br>5              | k $\Omega$<br>pF |
| Chroma Channel Input Voltage           | Chroma  | 220                   | m $V_{p-p}$      |
|  | Burst   | 100                   | m $V_{p-p}$      |
| ACC Range                              |   | +6 - -20              | dB               |
| Input Burst Level for Kill             | Adjust chroma input Pin 4 until Pin 2 $\leq 25$ m $V_{p-p}$ .<br>Measure Burst level at Pin 4.  | 10*                   | m $V_{p-p}$      |
| Contrast Control Chroma/Luma Tracking  | Chroma Input: Burst=100 m $V_{p-p}$<br>Chroma=220 m $V_{p-p}$<br>Luminance Input: 0.35 $V_{p-p}$<br>$V_S$ adjusted for Chroma at Pin 18=2 $V_{p-p}$<br>$V_C$ is adjusted for luminance at Pin 18=2 $V_{p-p}$ .<br>$V_C$ is again adjusted for luminance of +6 and -9 dB.<br>Then read chroma percentage difference. See Fig. F. | ±5                    | %                |
| Saturation Control Range—Term. 3       | For control characteristic, see Fig. G.   | 0 - 5                 | V dc             |
| Max. Chroma Output Voltage—Term. 2     | Chroma Input: Burst=100 m $V_{p-p}$<br>Chroma=220 m $V_{p-p}$ . Adjust $V_C$ and $V_S$ for max. Pin 2 output.   | 2.5                   | $V_{p-p}$        |

\*If a different value is desired, see the Threshold Adjustment Circuit of Fig. 3.

## Specifications CA3194

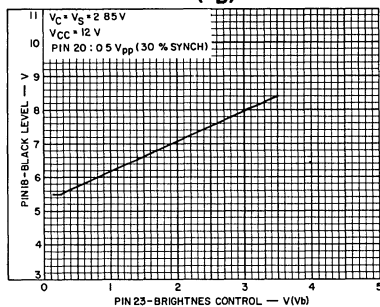
| CHARACTERISTIC                              | TEST CONDITIONS   | TYPICAL VALUE         | UNITS             |
|---|---|-----------------------|-------------------|
| <b>OSCILLATOR SECTION</b>                   |   |                       |                   |
| Pull-In Range                               | Chroma Input: Burst=100 mV <sub>p-p</sub><br>Chroma=220 mV <sub>p-p</sub> . Adjust C <sub>X</sub> for HI/LO f <sub>OSC</sub> without Chroma signal. Apply signal to lock. | ±500                  | Hz                |
| Static Phase Error                          |   | 2                     | DEG/100 Hz        |
| <b>DEMODULATOR SECTION</b>                  |   |                       |                   |
| R-Y Demodulator Conversion Gain             | Chroma Input: Burst=100 mV<br>Chroma=220 mV <sub>p-p</sub> , V <sub>φ</sub> . Adjust V <sub>C</sub> for V18=1 V. Read V15. Calculate V18/V15.                             | 10                    | Ratio             |
| B-Y Demodulator Conversion Gain             | Chroma Input: Burst=100 mV <sub>p-p</sub> , U <sub>φ</sub> . Read V16 and V14. Calculate V16/V14. V <sub>C</sub> remains as for R-Y gain                                  | 18                    | Ratio             |
| G-Y/B-Y Matrix Ratio                        | Chroma Input: Burst=100 mV <sub>p-p</sub> , Chroma=220 mV <sub>p-p</sub> , U <sub>φ</sub> read V17 and V16. Calculate V17/16. V <sub>C</sub> remains as above.            | 0.2                   | Ratio             |
| G-Y/R-Y Matrix Ratio                        | Chroma Input: Burst=100 mV <sub>p-p</sub> , Chroma=220 mV <sub>p-p</sub> , V <sub>φ</sub> . Read V17 and V18. Calculate V17/18. V <sub>C</sub> remains as above.          | 0.5                   | Ratio             |
| Sub-Carrier and Harmonic Content at Outputs | No Chroma or Luma Input.<br>Read residual carrier at outputs.   | 30                    | mV <sub>p-p</sub> |
| <b>SANDCASTLE PULSE</b>                     |   |                       |                   |
| Horizontal and Vertical Blanking Pedestal   |   | 2 - 5                 | V                 |
| Burst Gate Pulse                            |   | 6.5 - V <sub>CC</sub> | V                 |

**NOTE:**

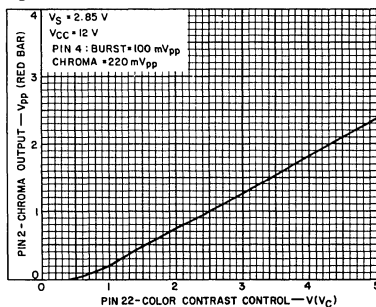
Use of the circuit of Fig. 4 is suggested to prevent increased color saturation at low level RF signals. The reference voltage can be adjusted by changing the values of the voltage divider.

### TYPICAL CHARACTERISTICS (Refer to Fig. 5 for Test Circuit)

**A. BRIGHTNESS CONTROL (V<sub>B</sub>)**



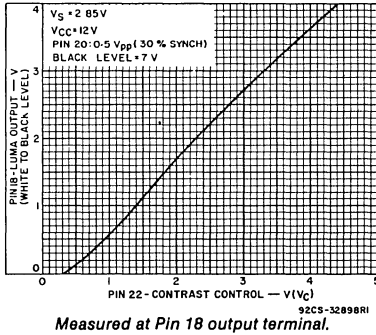
Measured at Pin 18 output terminal.



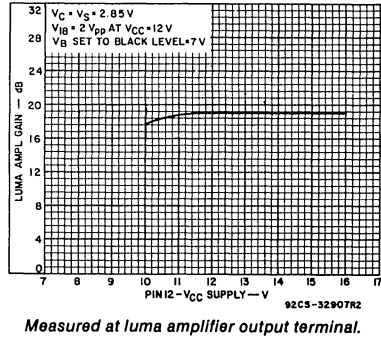
Measured at 2nd chroma amplifier output terminal.

TYPICAL CHARACTERISTICS (Cont'd)

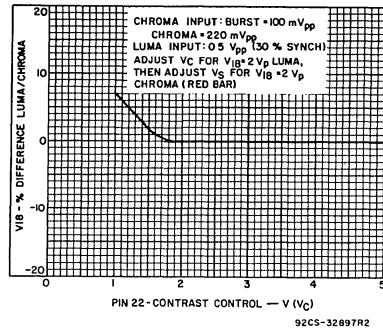
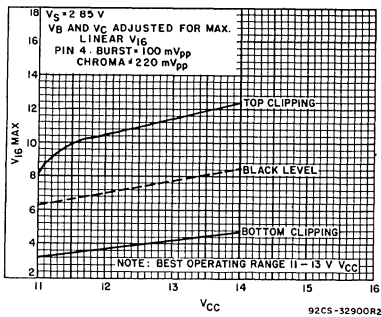
B. CONTRAST CONTROL ( $V_C$ )



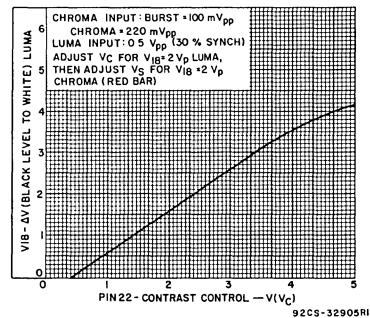
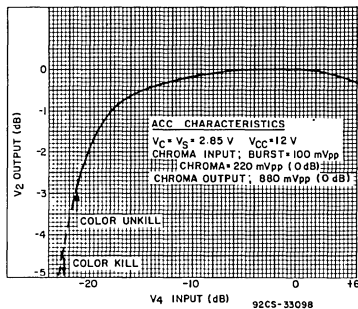
C. LUMA GAIN VS. SUPPLY VOLTAGE ( $V_{CC}$ )



D. LINEAR OPERATING RANGE AS A FUNCTION OF  $V_{CC}$

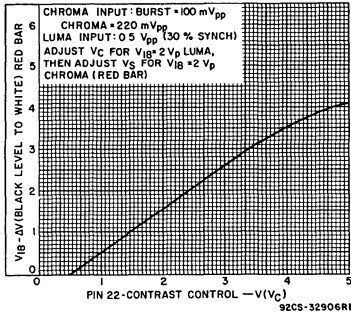


E. ACC CHARACTERISTICS



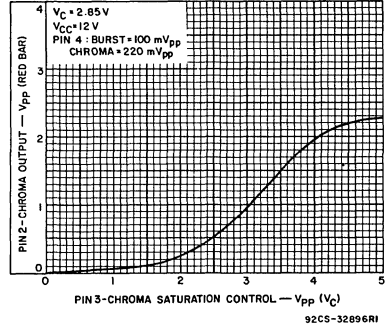
TYPICAL CHARACTERISTICS (Cont'd)

F. LUMA/CHROMA TRACKING WITH CONTRAST CONTROL



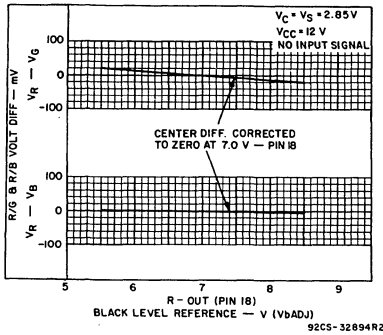
Measured at Pin 18 output terminal.

G. SATURATION CONTROL ( $V_S$ )



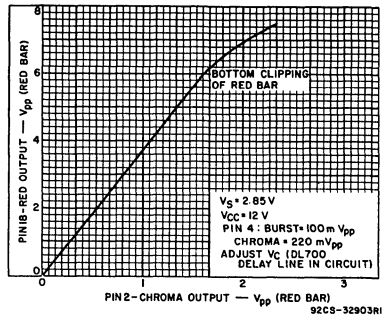
Measured at chroma amplifier output terminal Pin 2.

H. DIFFERENTIAL BLACK-LEVEL TRACKING



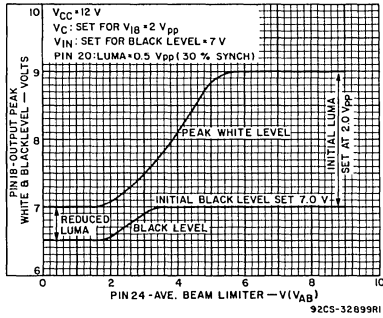
Measured at RGB output terminals.

I. PIN 18 OUTPUT VS. PIN 2 VOLTAGE

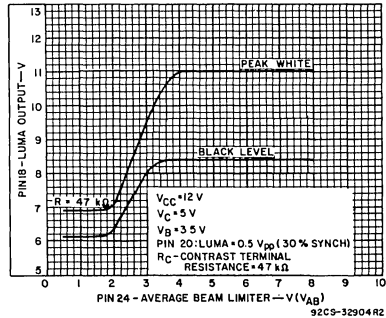


Measured at chroma output terminals and R output.

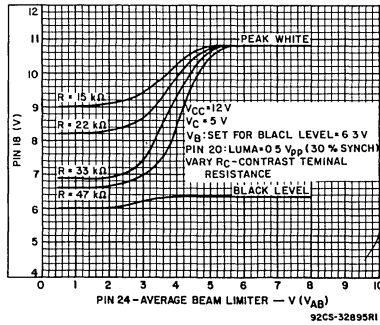
J. AVERAGE BEAM LIMITER (V<sub>AB</sub>)



Measured at Pin 18 output.



Measured at Pin 18 output.



Measured at Pin 18 output.

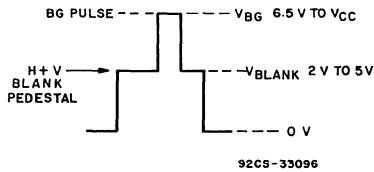
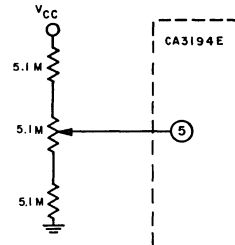


Fig. 2 - Sandcastle input waveform.



KILLER THRESHOLD LEVEL CONTROL  
92CS-34516

Fig. 3 - Killer-threshold level control.

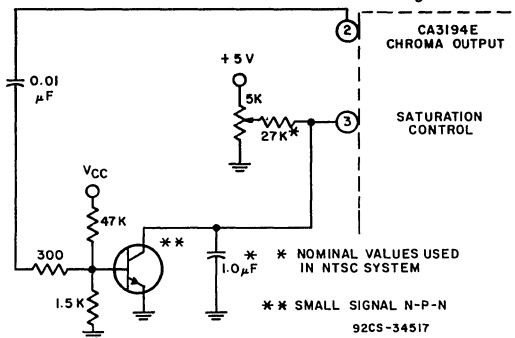


Fig. 4 - External overload detector.

8  
SPECIAL  
ANALOG CIRCUITS



### CA3194

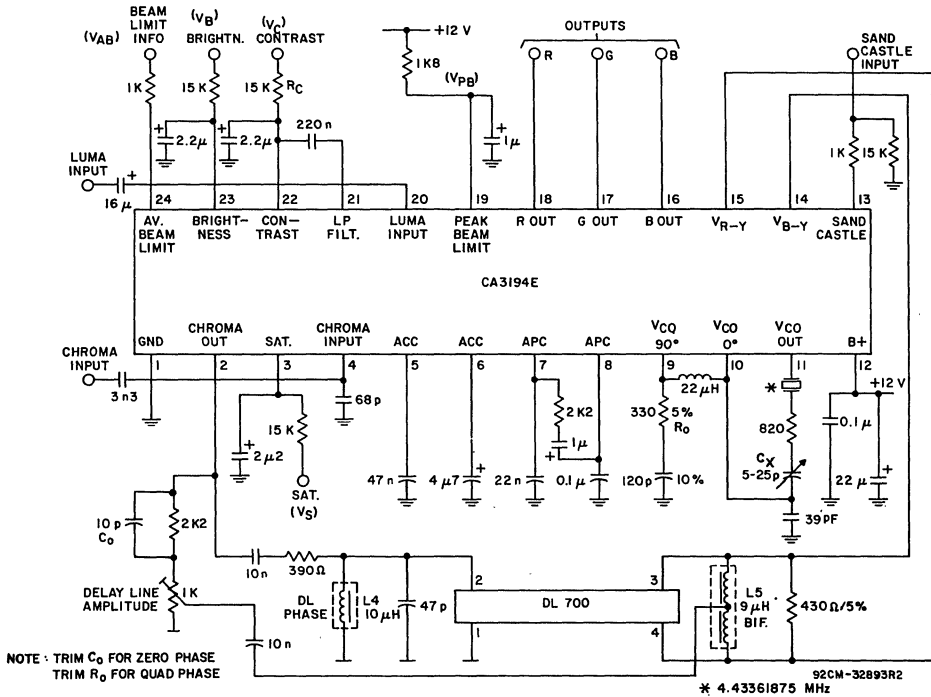


Fig. 5 - Test circuit.

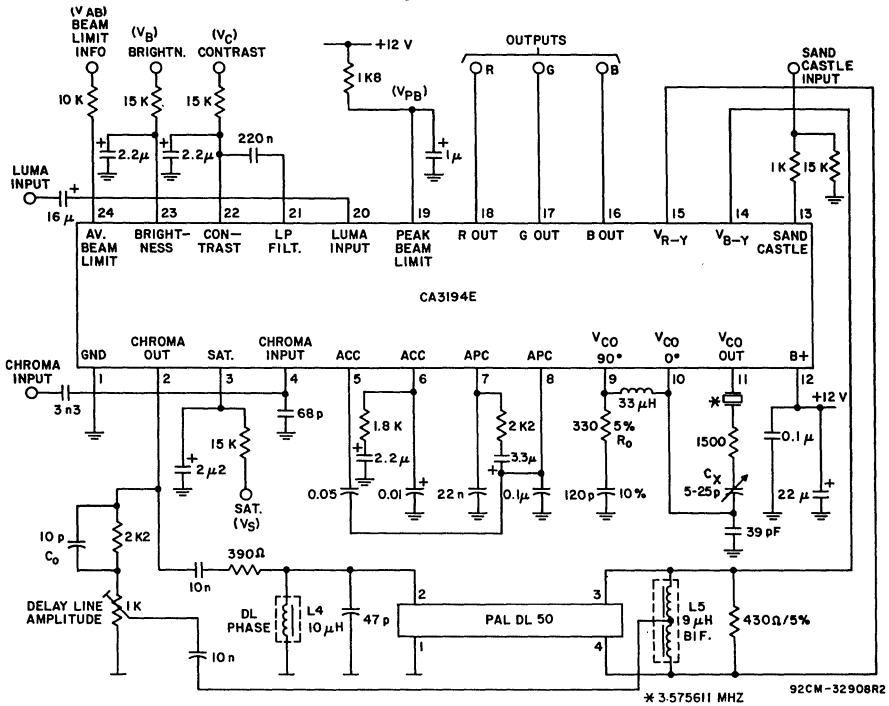


Fig. 6 - Application circuit for PAL M.

August 1991

### Features

- All Chroma Processing and Demodulating Circuitry on a Single Chip in a 28-Lead Plastic Package
- Phase-Locked Subcarrier Regeneration Utilizing Sample-and-Hold Techniques
- Supplementary ACC with Overload Detector to Prevent Over Saturation of the Picture Tube
- Linear DC Controls for Chroma Gain and Tint
- Dynamic "Flesh Correction" - Corrects Purple and Green Flesh Colors without Affecting Primary Colors
- Balanced Chroma Demodulators with Low Output Impedance for Direct Coupling
- Internal RF Filtering
- Requires Few External Components
- Automatic Beam Limiter
- Chroma Luminance Tracking Picture Control

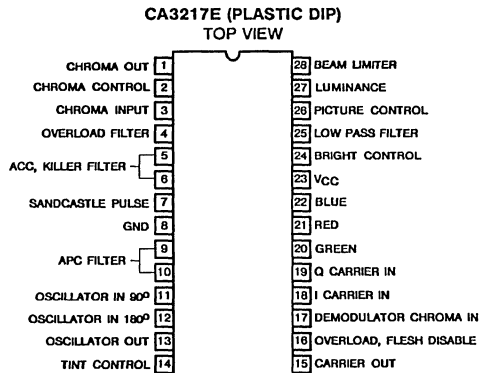
### Description

The Harris CA3217E\* is a monolithic silicon integrated circuit. It contains all the required circuit functions between the video detector and the picture tube RGB driver stages of a color television receiver. The CA3217E decodes the chrominance signals and then produces three different color signals that are internally combined with the luminance to develop the RGB signals. The picture saturation, hue and brightness DC controls are externally adjustable by the viewers. The AFPC, ACC, Dynamic flesh control, Beam limiting and Gate black level (Brightness) control are servo loops used to stabilize the RGB output and reduce frequent manual adjustment. The automatic beam limiter circuit reduces picture contrast and brightness to prevent excessive drive output at the picture tube.

The CA3217E is supplied in a 28-lead dual-in-line plastic package.

\* Formerly RCA Dev. Type No. TA10806.

### Pinout



### Absolute Maximum Ratings

|  |                              |
|--|------------------------------|
| DC Supply Voltage                            |                              |
| Between Terms 23 and 8                       | 14.0V                        |
| Device Dissipation:                          |                              |
| Up to $T_A = 55^\circ\text{C}$               | 1.27W                        |
| Above $T_A = 55^\circ\text{C}$               | Derate Linearly at 13.3mW/°C |
| Ambient Temperature Range:                   |                              |
| Operating                                    | -40 to +85°C                 |
| Storage                                      | -65 to +150°C                |
| Lead Temperature (During Soldering):         |                              |
| At Distance 1/16 ± 1/32 Inch (1.59 ± 0.79mm) |                              |
| from Case for 10 Seconds Max.                | +265°C                       |

**8**
**SPECIAL  
ANALOG CIRCUITS**

## Specifications CA3217

### ELECTRICAL CHARACTERISTICS at T<sub>A</sub> = 25° C

| CHARACTERISTIC             | TEST CONDITIONS |                |                |                |                |                |                          |                            |                        |                  |      | LIMITS |      |      | UNITS             |
|----------------------------|-----------------|----------------|----------------|----------------|----------------|----------------|--------------------------|----------------------------|------------------------|------------------|------|--------|------|------|-------------------|
|                            | Test            | S <sub>2</sub> | S <sub>3</sub> | S <sub>4</sub> | S <sub>5</sub> | S <sub>6</sub> | mV <sub>p-p</sub> Chroma | mV <sub>p-p</sub> Burst In | mV <sub>p-p</sub> Luma | Relays Energized | Note | Min.   | Typ. | Max. |                   |
| <b>STATIC</b> (Test 1-5)   |                 |                |                |                |                |                |                          |                            |                        |                  |      |        |      |      |                   |
| Dissipation                | Pin 23          | 6.3 V          | 11.2 V         | 4.0 V          | 6.3 V          | 11.2 V         |                          |                            |                        |                  |      | 30     | 48   | 66   | mA                |
| Pin 1 Bal                  | XPT1            | 1.2 V          | 11.2 V         | 4.0 V          | 6.3 V          | 11.2 V         |                          |                            |                        |                  |      |        | 10.5 |      | Vdc               |
| Pin 3 Bal                  | XPT1            | 1.2 V          | 11.2 V         | 4.0 V          | 6.3 V          | 11.2 V         |                          |                            |                        |                  |      |        | 2.2  |      |                   |
| Pin 17 Bal                 | XPT9            | 1.2 V          | 11.2 V         | 4.0 V          | 6.3 V          | 11.2 V         |                          |                            |                        |                  |      |        | 3.0  |      |                   |
| Pin 13 Bal                 | XPT13           | 1.2 V          | 11.2 V         | 4.0 V          | 6.3 V          | 11.2 V         |                          |                            |                        |                  |      |        | 7.5  |      |                   |
| <b>DYNAMIC</b> (Test 6-26) |                 |                |                |                |                |                |                          |                            |                        |                  |      |        |      |      |                   |
| Oscillator Pull-In         | "D"             | 6.3 V          | 11.2 V         | 4.0 V          | 6.3 V          | 11.2 V         | 25                       | 25                         |                        | K4, K7           | 1    | -350   |      | +350 | Hz                |
| Oscillator Level           | "D"             | 6.3 V          | 11.2 V         | 4.0 V          | 6.3 V          | 11.2 V         | 0                        | 0                          |                        | K7               |      |        | 0.7  |      | V <sub>p-p</sub>  |
| 100% Acc                   | P21             | Vary           | 11.2 V         | 4.0 V          | 6.3 V          | 11.2 V         | 125                      | 125                        |                        | K4, K7           | 2    |        | 1.5  |      |                   |
| 200% Acc                   | P21             | T8             | 11.2 V         | 4.0 V          | 6.3 V          | 11.2 V         | 250                      | 250                        |                        | K4, K7           | 3    |        | 100  |      | %                 |
| 20% Acc                    | P21             | T8             | 11.2 V         | 4.0 V          | 6.3 V          | 11.2 V         | 25                       | 25                         |                        | K4, K7           | 3    |        | 90   |      | Vdc               |
| Tint Center                | S5              | Vary           | 11.2 V         | 4.0 V          | Vary           | 11.2 V         | 250                      | 125                        |                        | K4, K7           | 4    |        | 6.5  |      |                   |
| R-Y Maximum                | P21             | 11.2 V         | 11.2 V         | 6.0 V          | T11            | 11.2 V         | 250                      | 125                        |                        | K1, K4, K7       |      |        | 6.0  |      | V <sub>p-p</sub>  |
| Unkill                     | P21             | 11.2 V         | 11.2 V         | 4.0 V          | T11            | 11.2 V         | 25                       | 12.5                       |                        | K4, K7           |      |        | 4.5  |      |                   |
| Kill                       | P21             | 11.2 V         | 11.2 V         | 4.0 V          | T11            | 11.2 V         | 25                       | 2.5                        |                        | K4, K7           |      |        |      | 150  | mV <sub>p-p</sub> |
| Chroma Reserver            | P21             | 11.2 V         | 11.2 V         | 4.0 V          | T11            | 11.2 V         | 12.5                     | 125                        |                        | K2, K4, K7       |      |        | 2.0  |      | V <sub>p-p</sub>  |
| Maximum Luma               | P21             | 11.2 V         | 11.2 V         | 4.0 V          | T11            | 11.2 V         |                          |                            | 125                    | K1, K3, K7       | 5    |        | 2.2  |      |                   |
| Luma Ratio                 | P21             | 11.2 V         | 6.3 V          | 4.0 V          | T11            | 11.2 V         |                          |                            | 125                    | K1, K3, K7       | 6    |        | 50   |      | %                 |
| Linearity                  | P21             | 11.2 V         | Vary           | 3.0            | T11            | 11.2 V         |                          |                            | 425                    | K3, K7           | 7    |        | 4    |      | V <sub>p-p</sub>  |
| T19 = T19/T18              | P21             | 11.2 V         | T18            | 3.0            | T11            | 11.2 V         |                          |                            | 212.5                  | K3, K7           |      |        | 50   |      | %                 |
| 4.78 MHz Response          | P21             | 11.2 V         | 11.2 V         | 4.0 V          | T11            | 11.2 V         |                          |                            | 125                    | K3, K6, K7       | 8    | -3     |      | 3    | dB                |
| Contrast Limit 1           | P24             | 11.2 V         | 11.2 V         | 4.0 V          | T11            | 11.2 V         |                          |                            | 250                    | K3, K5, K7       | 9    |        | 3.9  |      | Vdc               |
| Contrast Limit 2           | P26             | 11.2 V         | 11.2 V         | 4.0 V          | T11            | 11.2 V         |                          |                            | 250                    | K3, K5, K7       | 9    |        | 8.2  |      |                   |
| Bright Limit 1             | P24             | 11.2 V         | 11.2 V         | 4.0 V          | T11            | 11.2 V         |                          |                            | 250                    | K3, K5, K7       | 10   |        | 3.1  |      |                   |
| Bright Limit 2             | P26             | 11.2 V         | 11.2 V         | 4.0 V          | T11            | 11.2 V         |                          |                            | 250                    | K3, K5, K7       | 10   |        | 5.6  |      |                   |
| G-Y Ratio                  | P20             | Vary           | 11.2 V         | 4.0 V          | T11            | 11.2 V         | 250                      | 125                        |                        |                  | 11   |        | 0.33 |      | R                 |
| B-Y Ratio                  | P22             | T25            | 11.2 V         | 4.0 V          | T11            | 11.2 V         | 250                      | 125                        |                        |                  | 11   |        | 1.20 |      |                   |

#### Notes:

- With K7 energized and frequency counter at D vary C1 for 3.579175 MHz. Then with K4 energized, check for pull-in. Repeat for frequency tuned to 3.579875 MHz. For all other tests tune to 3.579545 MHz ±10 Hz.
- Vary S2 for 1.5 V<sub>p-p</sub> at Pin 21.
- % of 100% ACC.
- Adjust C1 for 3.579545 MHz ±10 Hz. Adjust S2 for 1.6V V<sub>p-p</sub> at Pin 22 and 0 reference; then adjust S5 for minimum at P21. Read and record S5 voltage
- Black to White.
- T17 = T17/T16.
- Adjust S3 for 4.0 V<sub>p-p</sub>.
- AC amplitude = 50 mV<sub>p-p</sub> reference 15 kHz.
- Adjust beam limiter to 10.7 V.
- Adjust beam limiter to 9.8 V.
- Adjust S2 for 1.5 V<sub>p-p</sub> at Pin 21, then calculate P20/P21 and P22/P21.

## CA3217

### TYPICAL PERFORMANCE OF THE CA3217E

| Function  | Typical Data                            |              |
|---|---|--------------|
| Nominal Supply  | 11.2V                                   |              |
| Nominal Dissipation   | 500 mW                                  |              |
| Oscillator Stability  | 5 Hz                                    |              |
| Supply Variation 10-14 V  |   |              |
| Variation with Temperature<br>( $\Delta T = 50^\circ\text{C}$ ) | 25 Hz                                   |              |
| AFPC Characteristics  |   |              |
| dc Loop Gain  | 33 Hz/degree                            |              |
| Pull-in Range   | $\pm 500$ Hz                            |              |
| ACC Characteristic  |   |              |
| 100% Chroma Input Level   | 250 mV <sub>p-p</sub> on red bar        |              |
| 3-dB Point  | at 20% nominal input level              |              |
| Hue-Control Range   | 100°                                    |              |
| Saturation-Control Range  | 40 dB min                               |              |
| <b>Demodulator Characteristics:</b>                             | <b>Relative Amplitude</b>               | <b>Angle</b> |
| R — Y   | 1.0                                     | 93°          |
| B — Y   | 1.2                                     | 2°           |
| G — Y   | 0.3                                     | 258°         |
| Bandwidth (Chroma)  | 900 kHz                                 |              |
| Flesh Control   | Primary control in the +1 half-plane    |              |
| Chroma Overload Control   | Two levels                              |              |
| Picture Control   | 40 dB                                   |              |
| Brightness Control  | Black level clamped on 3 V to 5 V level |              |
| Beam Limiting   | On picture and brightness controls      |              |
| Luma Bandwidth  | 5 MHz min                               |              |
| Sandcastle Input  |   |              |
| 1.2 — 2.3 V   | Blanking                                |              |
| >3.3 V  | Burst gate                              |              |
| Maximum Linear Output   |   |              |
| R   | 5 V                                     |              |
| G   | 3 V                                     |              |
| B   | 3.7 V                                   |              |

# CA3217

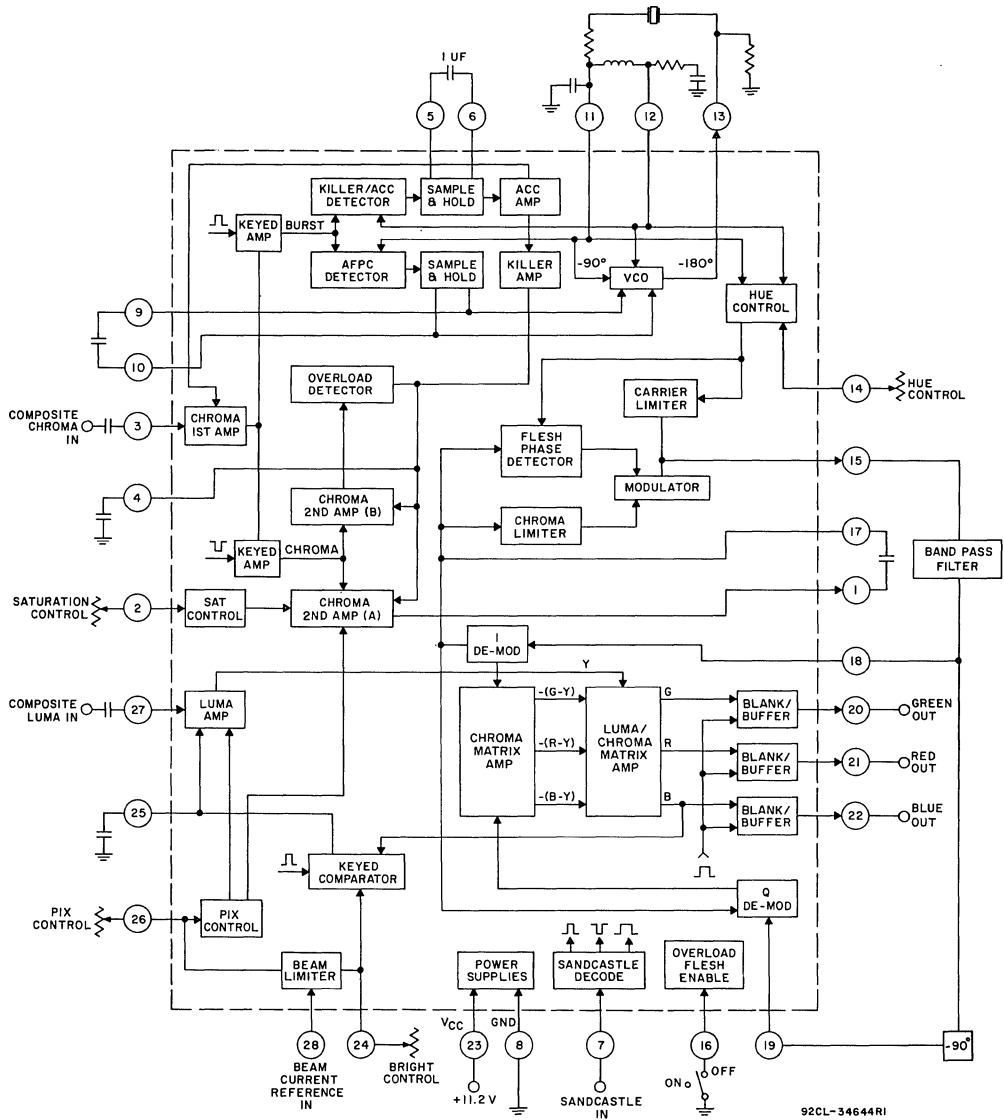


Fig. 1 - Functional block diagram of the CA3217E.

# CA3217

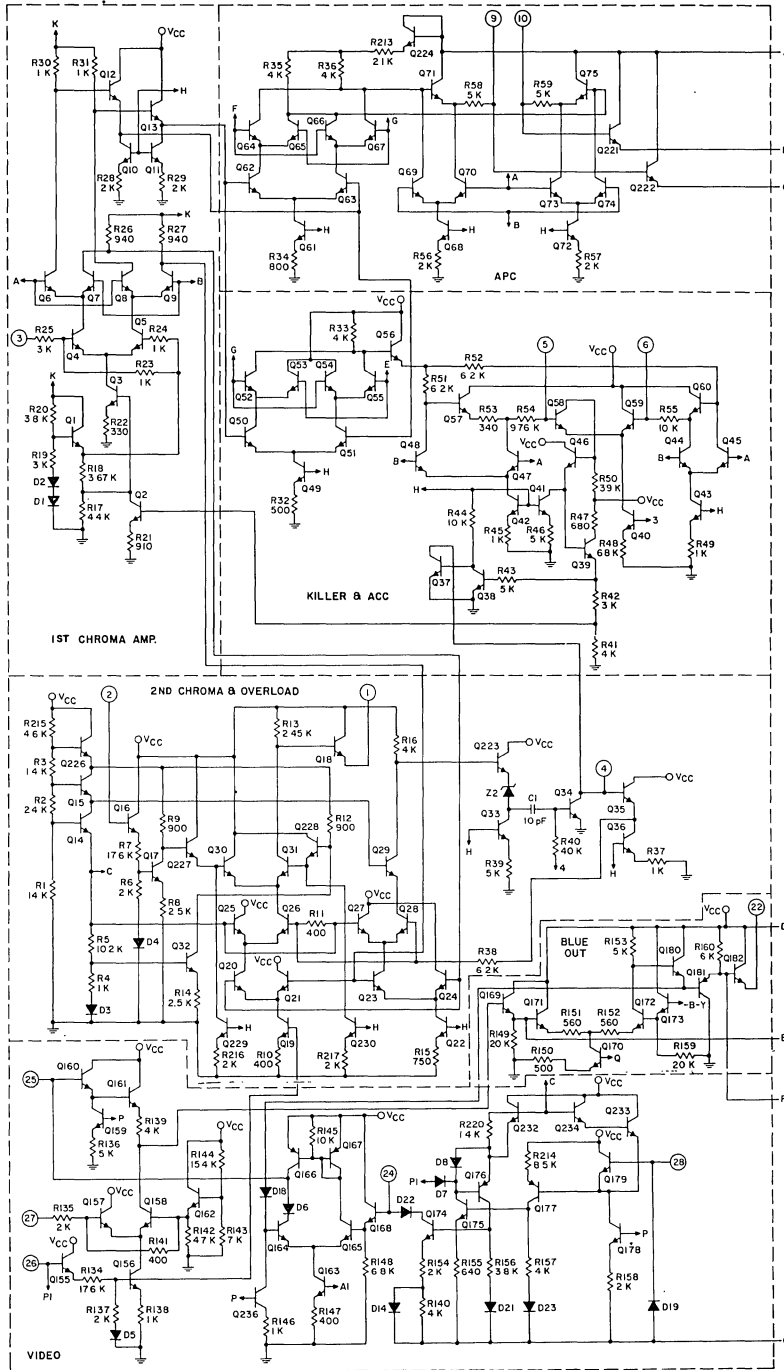


Fig. 2 - Schematic diagram of the CA3217E.  
(Cont'd on next page).

# CA3217

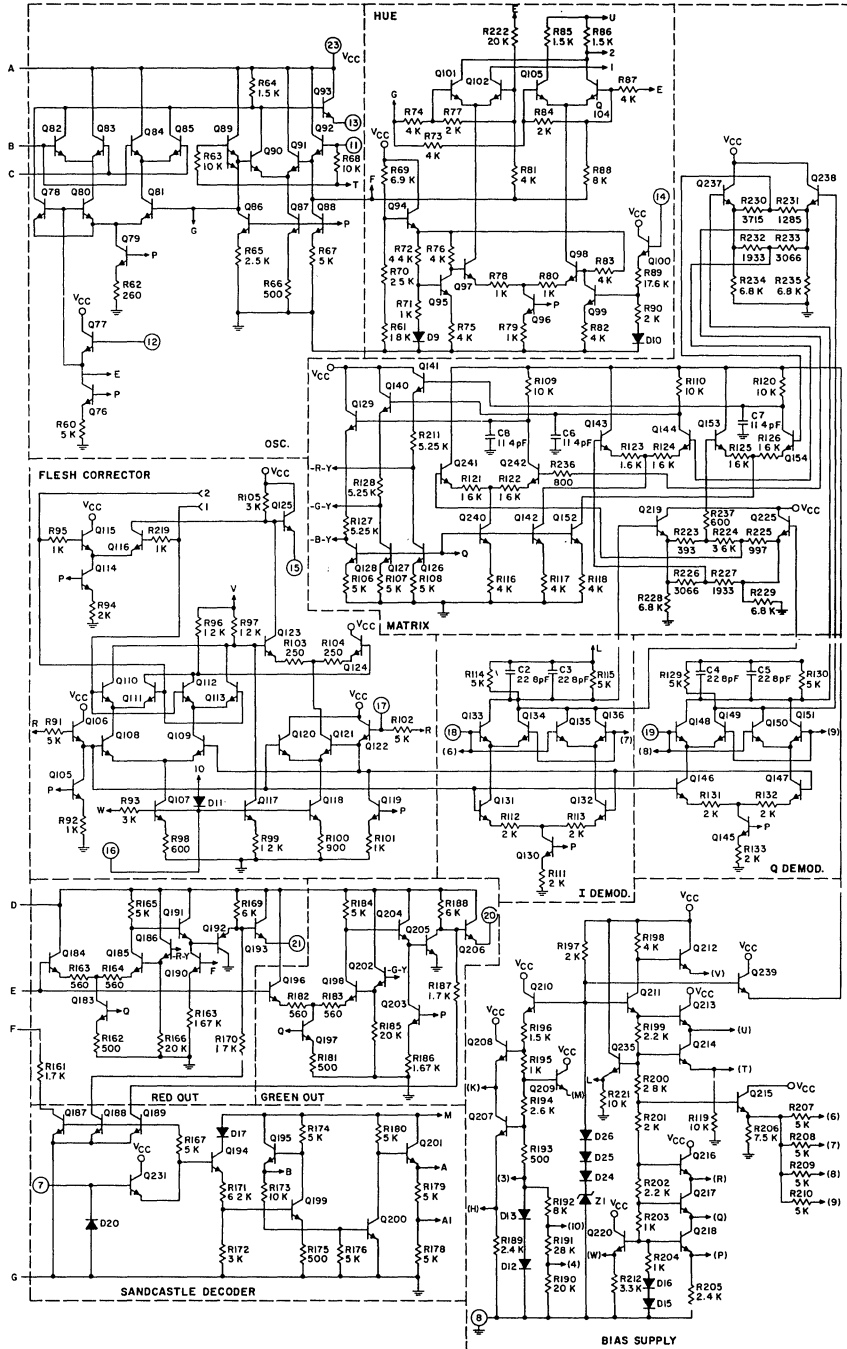


Fig. 2 - Schematic diagram of the CA3217E.  
(Cont'd from previous page).

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# CA3217

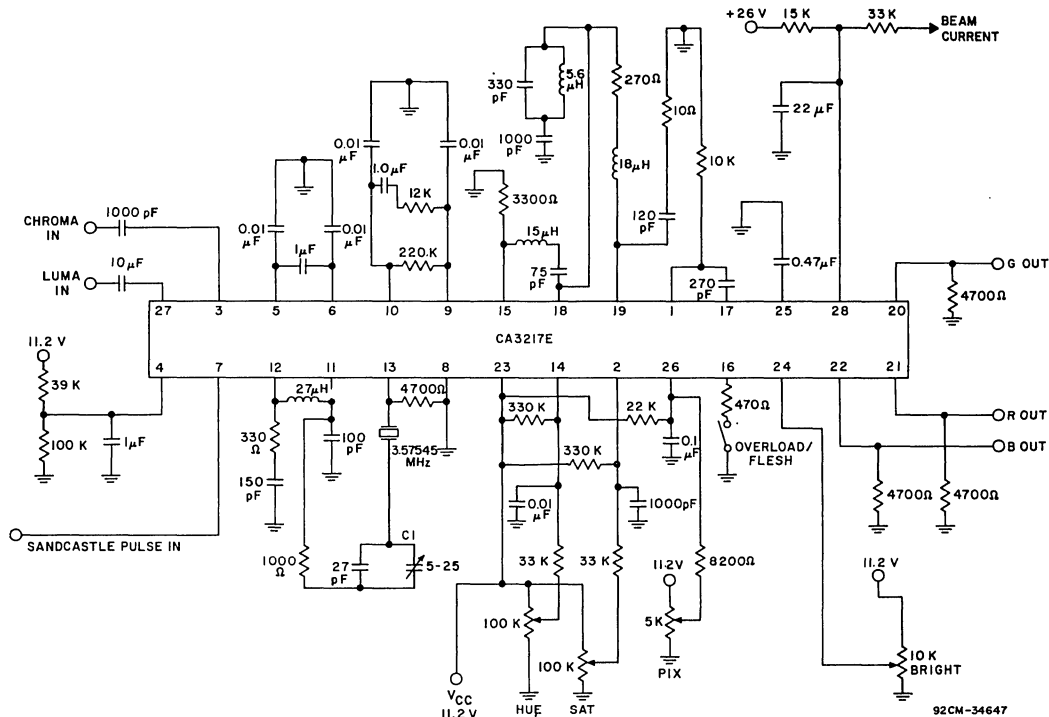


Fig. 3 - Typical application circuit.

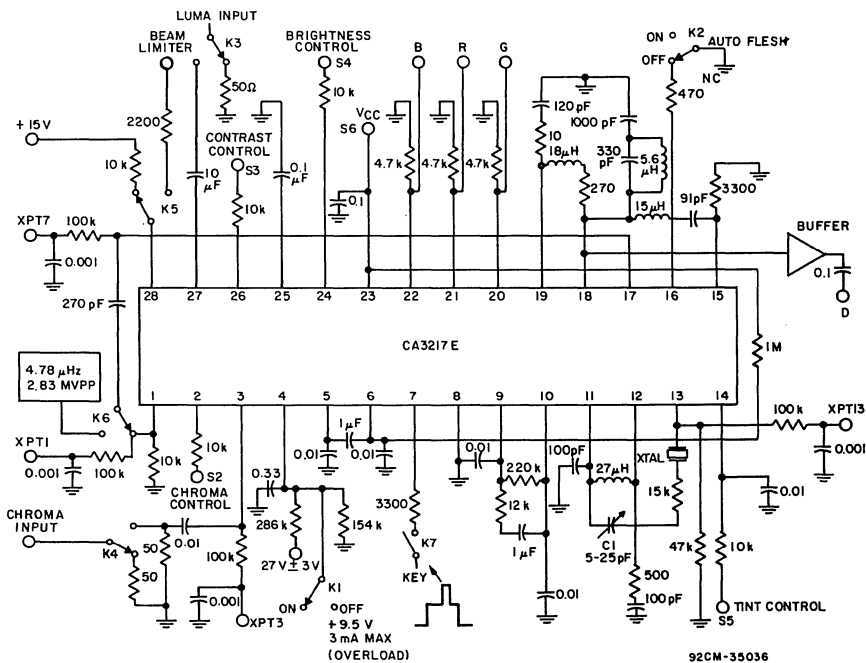


Fig. 4 - Test circuit for the CA3217E.

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# CA3217

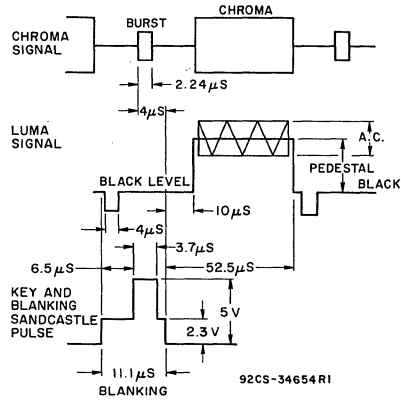


Fig. 5 - Test signals for the CA3217E.

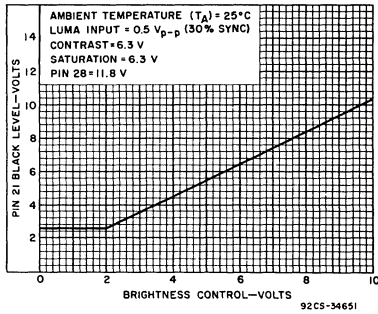


Fig. 6 - Typical P21 black level versus brightness control.

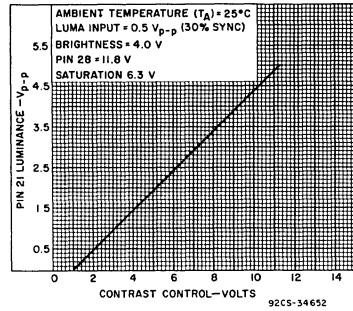


Fig. 7 - Typical P21 luminance output versus contrast control.

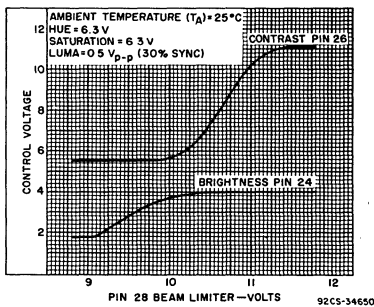


Fig. 8 - Typical beam limiter versus contrast and brightness.

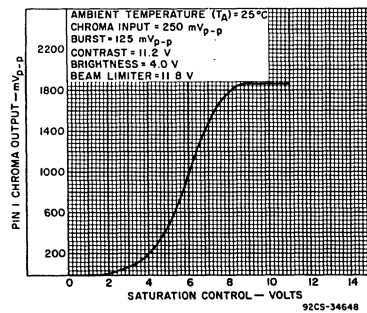


Fig. 9 - Typical P1 chroma output versus saturation control.

# CA3217

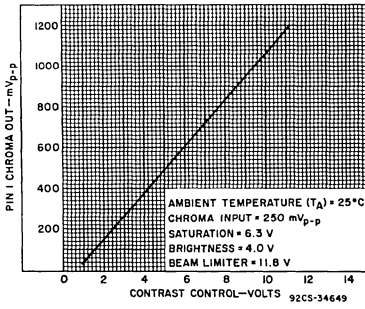


Fig. 10 - Typical P1 chroma output versus contrast control.

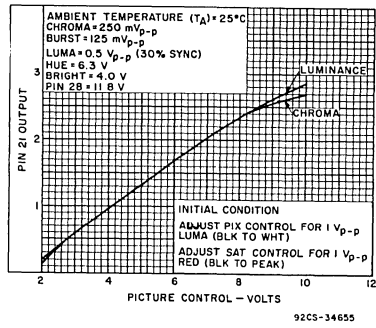


Fig. 11 - Typical luma/chroma track.

March 1991

### Features

- 5 Multiplex Video Channels
  - ▶ 1 Independent Channel
  - ▶ 4 Channels with Enable
- 4 LED Channel Indicator Outputs
- Wideband Video Amplifier ..... 25MHz Unity Gain
- Adjustable Video Amplifier Gain
- High Signal-Drive Capability

### Applications

- Video Multiplex Switch
- 75Ω Video Amplifier/Line Driver
- Video Signal-Level Control
- Monitor Switching Control
- TV/CATV Audio/Video Switch
- Video Signal Adder/Fader Control

### Description

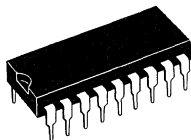
The CA3256 BiMOS analog video switch has five channels of CMOS multiplex switching for general-purpose video-signal control. One of four CMOS channels may be selected in parallel with channel 5. The CMOS switches are inputs to the video amplifier but may be used in bilateral switching between channels 1 to 4 and channel 5. The analog switches of channels 1 to 4 are digitally controlled with logic-level conversion and binary decoding to select 1 of 4 channels. The enable function controls channels 1 to 4 but does not affect channel 5. LED output drivers are selected with the channel 1-to-4 switch selection to indicate the ON-channel. Channel 5 may be used as a monitor output for data or signal information on channels 1 to 4. The transmission gate switches shown in the block diagram of the CA3256 are configured in a "T" design to minimize feedthrough. When the switch is off, the shunt or center of the "T" is grounded.

The amplifier has high input impedance to minimize the  $R_{ON}$  transmission gate insertion loss. The amplifier output impedance is typically 5Ω in a complementary symmetry output. The amplifier can directly drive a nominal 75Ω coaxial cable to provide line-to-line video switching. The gain of the amplifier is programmable by different feedback resistor values between pins 8 and 9. Compensation may also be used between these pins for an optimally flat frequency response. An internal regulated 5V DC bias reference with temperature compensation permits stable direct-coupled output drive and minimizes DC offset during signal switching.

The CA3256 device is available in an 18-lead Dual-In-Line Plastic Package (E Suffix).

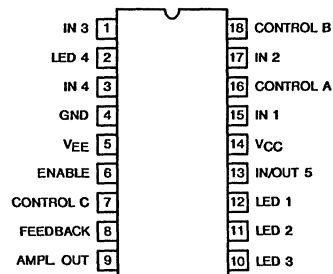
### Package

18-LEAD DUAL-IN-LINE  
PLASTIC PACKAGE  
E SUFFIX



### Pinout

18-LEAD DIP  
TOP VIEW



Block Diagram

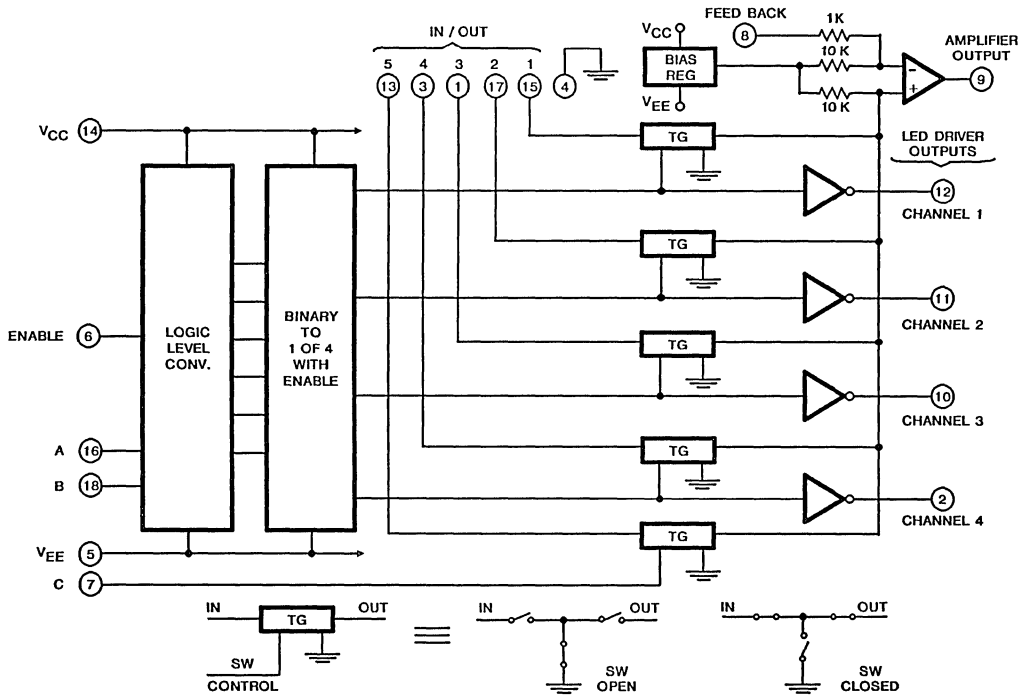


FIGURE 1.

Switch Control Logic

| CHANNEL NUMBER | C | A              | B | ENABLE |
|----------------|---|----------------|---|--------|
| 1              | O | O              | O | I      |
| 2              | O | O              | I | I      |
| 3              | O | I              | O | I      |
| 4              | O | I              | I | I      |
| 5 + (1-4)*     | I | Channel 1-4    |   | I      |
| 5              | I | Channel 5 Only |   | O      |
| None           | O | X              | X | O      |

\* For Maximum Video Bandwidth, Use Single Channel Selections

## Specifications CA3256

### Absolute Maximum Ratings

DC Supply Voltage Range,  $V_{CC}$  (Referenced to  $V_{EE}$ ) ..... 18V  
 Control Input Voltage Range, All Inputs .....  $V_{EE}$  to  $V_{CC}$   
 Signal Input Voltage Range, Channel 1-5 ..... 3Vp-p  
 Amplifier Output Current ..... 30mA  
 DC LED Sink Current ..... 30mA

### Device Dissipation:

Up to  $T_A = 55^\circ\text{C}$  ..... 630mW  
 Above  $T_A = 55^\circ\text{C}$  ..... Derate Linearly at 6.67mW/ $^\circ\text{C}$   
 Operating Temperature Range .....  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$   
 Storage Temperature Range .....  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Lead Temperature (During Soldering) at Distance 1/16  $\pm$  1/32 in.  
 (1.59  $\pm$  0.79 mm) from case for 10sec max. ....  $+265^\circ\text{C}$

### Performance Data $T_A = +25^\circ\text{C}$ , Nominal Data for $(V_{CC} - V_{EE}) = 12\text{V}$

| CHARACTERISTICS  | SYMBOL          | TYPICAL VALUES |               | UNITS         |
|--|-----------------|----------------|---------------|---------------|
| Power Supply Voltage $V_{CC} - V_{EE}$                 |                 | 10 to 18       |               | VDC           |
| Power Supply Current $V_{CC} - V_{EE} = 12\text{V}$    |                 | 20             |               | mA            |
|  |                 | SWITCH         | AMPLIFIER     |               |
| Open Loop Gain   | $A_{OL}$        | -              | 35            | dB            |
| Programmable Gain, FB Adjustment Range                 |                 | -              | $-0.8 A_{OL}$ | dB            |
| Power Bandwidth  |                 | -              | 10            | MHz           |
| Unity Gain Bandwidth, 1k $\Omega$ , 7pF Compensation   |                 | -              | 25            | MHz           |
| Insertion Loss   |                 | -0.8           | -             | dB            |
| Signal Feedthrough, 5MHz                               |                 | -66            | -             | dB            |
| Input Impedance  | $Z_{IN}$        | -              | 10            | k $\Omega$    |
| Output Impedance                                       | $Z_{OUT}$       | -              | 5             | $\Omega$      |
| Maximum Input Voltage                                  | $V_{I(max)}$    | 3              | 2.5           | Vp-p          |
| Maximum Output Voltage, Clipped                        | $V_{O(max)}$    | -              | 7             | Vp-p          |
| Reference Bias Output Voltage ( $V_B - V_{EE}$ )       |                 | -              | 5             | VDC           |
| Differential Gain                                      |                 | -              | 1             | %             |
| Differential Phase                                     |                 | -              | 1             | Degree        |
| Off Isolation, Channel to Channel, $Z_{IN} = 75\Omega$ |                 | -66            | -             | dB            |
| LCC Switch Turn On/Off Time Delay                      |                 | -              | 0.5           | $\mu\text{s}$ |
| Maximum LED Sink Current                               |                 | -              | 30            | mA            |
| Typical Output Source Current                          |                 | -              | 16            | mA            |
| Channel Control Switch A, B, C                         | $E_N$ Threshold | 6              | -             | V             |

CAUTION: Connect the  $V_{EE}$  power supply voltage before or during the  $V_{CC}$  turn-on.

## Specifications CA3256

**Electrical Specifications**  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = +12$ ,  $V_{LED} = +12$ ,  $V_{EE} = \text{GND}$ , Pin 4 = GND, Feedback Switch Closed,  $V_{HIGH} = 9\text{V}$ ,  $V_{LOW} = 3\text{V}$  (See Figure 3) Unless Otherwise Specified.

| CHARACTERISTICS  | INPUTS   |        |       |       |        | CHANNEL SWITCH CONTROL  |        |       |        |                  | MIN   | TYP   | MAX  | UNITS      |   |
|--|--|--------|-------|-------|--------|---|--------|-------|--------|------------------|-------|-------|------|------------|---|
|  | CH 1   | CH 2   | CH 3  | CH 4  | CH 5   | A   | B      | C     | ENABLE | TEST PIN #       |       |       |      |            |   |
|  | PIN 15   | PIN 17 | PIN 1 | PIN 3 | PIN 13 | PIN 16  | PIN 18 | PIN 7 | PIN 6  |                  |       |       |      |            |   |
| Supply Current, $I_{CC}$<br>$V_{LED} = 0\text{V}$                                    | 0V   | 0V     | 0V    | 0V    | 0V     | 3V  | 3V     | 3V    | 3V     | 14               | 10    | 16    | 22   | mA         |   |
| Dual Supply Current<br>$V_S = \pm 5\text{V}$   | 0V   | 0V     | 0V    | 0V    | 0V     | 0V  | 0V     | 0V    | 5V     | 14/5             | 10    | 20    | 26   | mA         |   |
| Amplifier Output,<br>Open Loop<br>$V_{B(OL)}, V_{LED} = 0\text{V}$                   | 0V   | 0V     | 0V    | 0V    | 0V     | 3V  | 3V     | 3V    | 3V     | 9                | 6     | 8.5   | 10   | V          |   |
| Amplifier Output,<br>Closed Loop, $V_{LED} = 0\text{V}$                              | 0V   | 0V     | 0V    | 0V    | 0V     | 3V  | 3V     | 3V    | 3V     | 9                | 4.8   | 5.1   | 5.4  | V          |   |
| $I_{OUT}$ MAX. (Source)<br>Open Loop   | 0V   | 0V     | 0V    | 0V    | 0V     | 3V  | 3V     | 3V    | 3V     | 9<br>Note 1      | -     | -70   | -25  | mA         |   |
| $I_{OUT}$ MAX. (Sink)<br>Open Loop   | 0V   | 0V     | 0V    | 0V    | 0V     | 3V  | 3V     | 3V    | 3V     | 9<br>Note 2      | 10    | 16    | -    | mA         |   |
| Input Leakage<br>Channel 1-5   | 3V   | 3V     | 3V    | 3V    | 3V     | 3V  | 3V     | 3V    | 3V     | 1, 3,<br>15, 17  | -15   | 5     | +15  | nA         |   |
| Channel Control Input<br>A, B, C, Enable Leakage                                     | 0V   | 0V     | 0V    | 0V    | 0V     | Measure at 3V, 9V each;<br>Enable and Channel<br>Switching Control Inputs |        |       |        | 6, 7,<br>16, 18  | -20   | 10    | +20  | nA         |   |
| LED Off, $V_{OFF}$   | 0V   | 0V     | 0V    | 0V    | 0V     | Select Channel 0-5  |        |       |        | 2, 10,<br>11, 12 | 11.97 | 11.99 | -    | V          |   |
| LED On, $V_{ON}$   | 0V   | 0V     | 0V    | 0V    | 0V     | Select Channel 0-5  |        |       |        | 2, 10,<br>11, 12 | -     | 0.1   | 0.3  | V          |   |
| Switch Resistance, $R_{DS}$  | $\pm 100\mu\text{A}$ Input Each Switch,<br>Channel 1-4 + 5 |        |       |       |        | Select<br>Channel 1-4   | 9V     | 9V    |        |                  | 0.8   | 1.1   | 1.4  | k $\Omega$ |   |
| $R_{DS}$ Match   | Calculation: (Max $R_{DS}$ - Min $R_{DS}$ )/Min $R_{DS}$   |        |       |       |        |   |        |       |        |                  | -     | -     | 3.6  | 5          | % |
| Amplifier Output Offset<br>$V_O$ Feedback Switch<br>Closed $V_{SUP} = \pm 5\text{V}$ | 0V   | 0V     | 0V    | 0V    | 0V     | 0V  | 0V     | 0V    | +5V    | 9                | -100  | 45    | +100 | mV         |   |
| Closed Loop Unity Gain   | 3V   | 0V     | 0V    | 0V    | 0V     | 3V  | 3V     | 3V    | 9V     | 9                | -0.5  | -0.1  | +0.5 | dB         |   |

**NOTES:**

1.  $V_{OUT} = +3\text{V}$ .
2.  $V_{OUT} = +7\text{V}$ .

CA3256

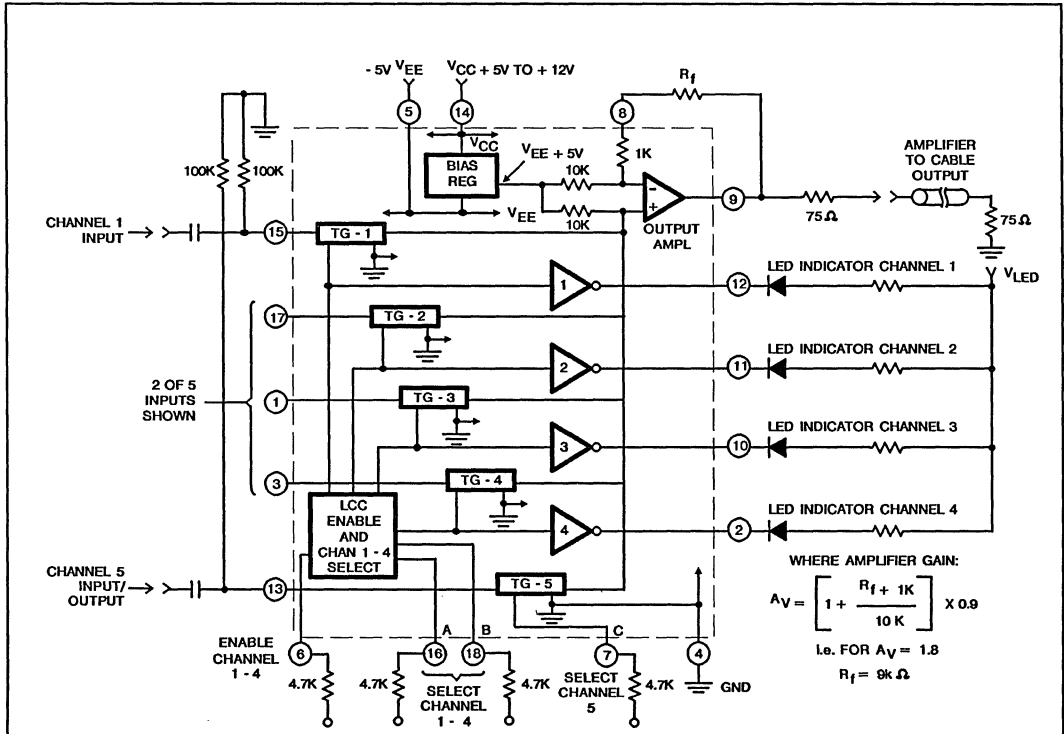


FIGURE 2(a). TYPICAL APPLICATION BIAS CIRCUIT DIRECT-COUPLED OUTPUT WITH  $V_{EE} = -5V$

# CA3256

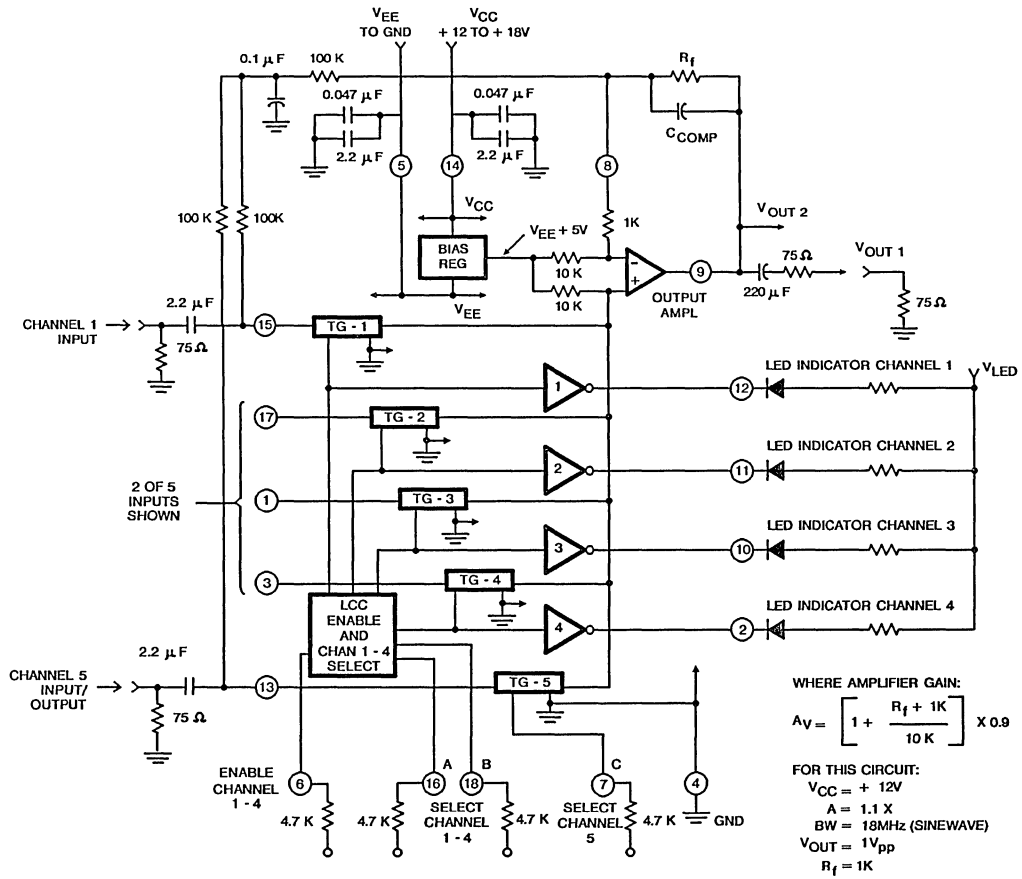
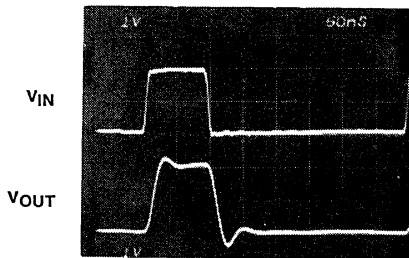


FIGURE 2(b). TYPICAL APPLICATION BIAS CIRCUIT AC-COUPLED INPUT WITH  $V_{EE} = GND$



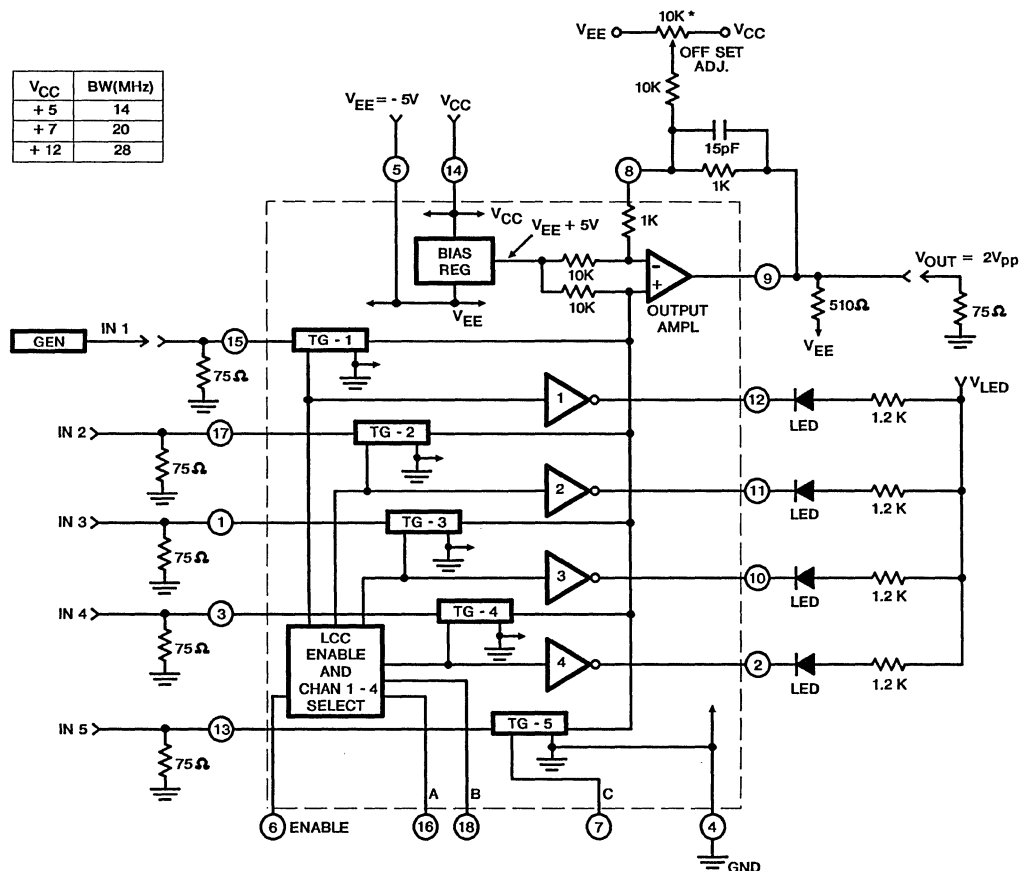
Waveform Display (Figure 2b) Pulse Performance = 20ns  $t_r$  for 0 to 2V Pulse

$V_{CC} = +12V, R_f = 1k\Omega, C_{COMP} = 6pF, Pin 9$  at  $V_{EE}(GND)$ .



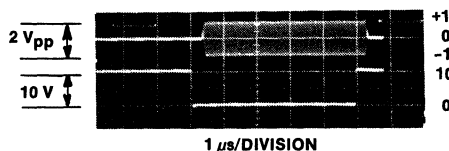
# CA3256

| V <sub>CC</sub> | BW(MHz) |
|-----------------|---------|
| + 5             | 14      |
| + 7             | 20      |
| + 12            | 28      |

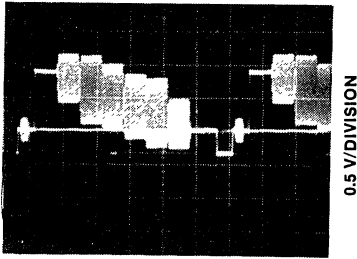


\* Adjust offset for V<sub>DC</sub> at pin 9 equal to zero volts with no AC signal and one channel "ON". Dynamic clamping may be accomplished by error current feedback to pin 8.

**FIGURE 2(c). TYPICAL APPLICATION BIAS CIRCUIT DC-COUPLED INPUT AND OUTPUT. THE V<sub>p-p</sub> OUTPUT CAPABILITY IS FIXED BY THE V<sub>CC</sub> AND V<sub>EE</sub> RANGE AND IS APPROXIMATELY +3.6V, -2.5V (CLIPPED) FOR V<sub>CC</sub> = +5V, V<sub>EE</sub> = 5V. THE LOW P.S. FUNCTIONAL RANGE FOR 2V<sub>p-p</sub> OUTPUT IS V<sub>CC</sub> = +4V, V<sub>EE</sub> = -4V; BW ≈ 10MHz.**

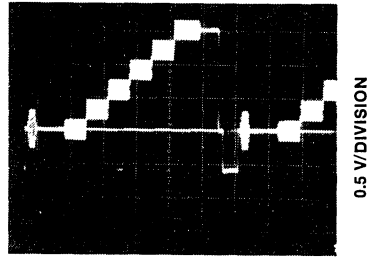


**PHOTO 1. WAVEFORM DISPLAY (FIGURE 2c) GATED OUTPUT FOR V<sub>CC</sub> = +12V ENABLE = HIGH, CONTROL B = C = LOW, CONTROL A = 10V PULSE. THE BURST OUTPUT IS DELAYED ~ 400ns at t<sub>ON</sub>, t<sub>OFF</sub>.**



10 μs/DIVISION

PHOTO 2. STANDARD NTS COLOR BAR



10 μs/DIVISION

PHOTO 3. UNIFORM STEP SIGNAL WITH 3.58MHz MODULATION. CIRCUIT CONDITIONS,  $V_{CC} = +5V$ ,  $V_{EE} = -5V$ ,  $I_{CC} \approx 25mA$ .

PHOTOS 2 & 3. WAVEFORM DISPLAY (FIGURE 2c) OF DC COUPLED PERFORMANCE CHARACTERISTIC.

Test Circuit

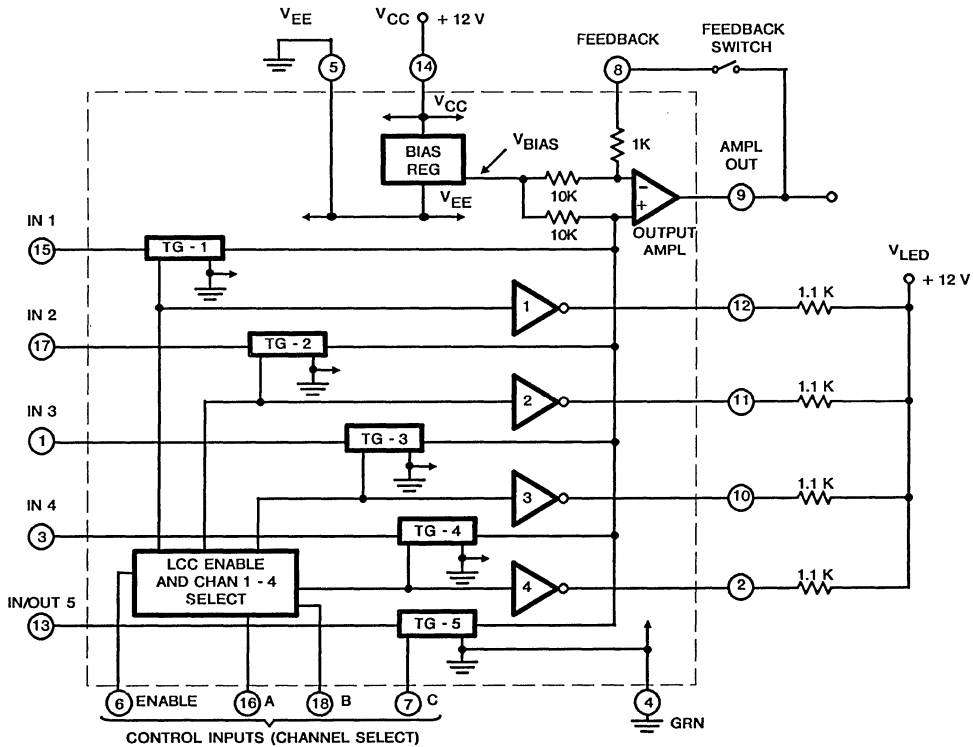


FIGURE 3. CA3256 TEST CIRCUIT

Test Circuits (Continued)

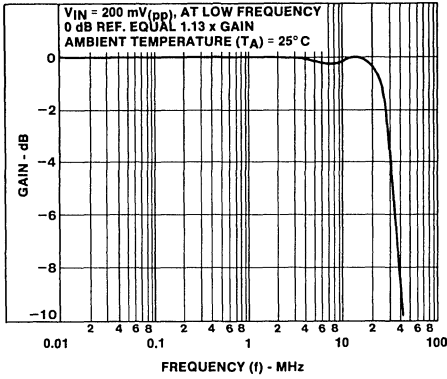


FIGURE 4(a). GAIN-BANDWIDTH CHARACTERISTICS OF FIGURE 2b WITH COMPENSATION CAPACITOR,  $C_{COMP}$ , AND  $R_f$ , SEE FIGURE 4b AND FIGURE 6(1).

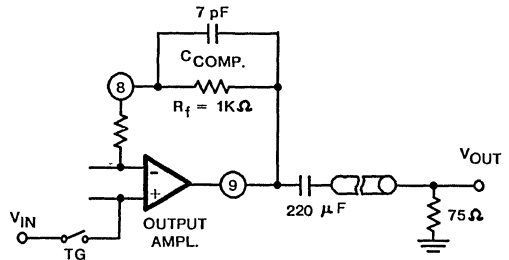


FIGURE 4(b). TEST CIRCUIT.

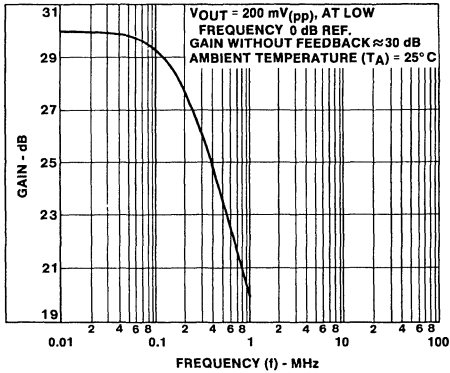


FIGURE 5(a). OPEN LOOP GAIN-BANDWIDTH CHARACTERISTIC OF FIGURE 2b WITH NO FEEDBACK, SEE FIGURE 5b AND FIGURE 6(5).

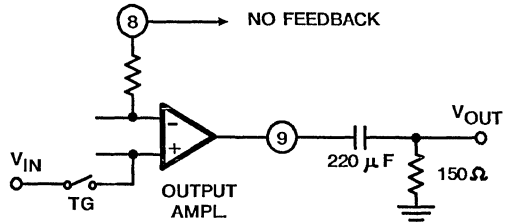


FIGURE 5(b). TEST CIRCUIT.

Test Circuits (Continued)

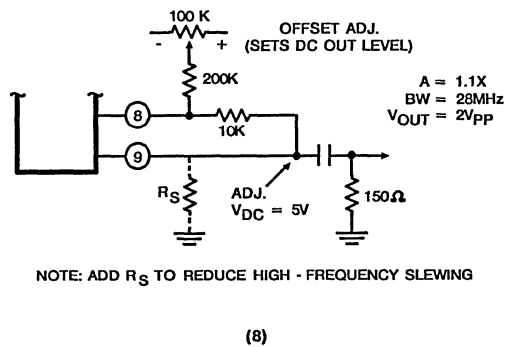
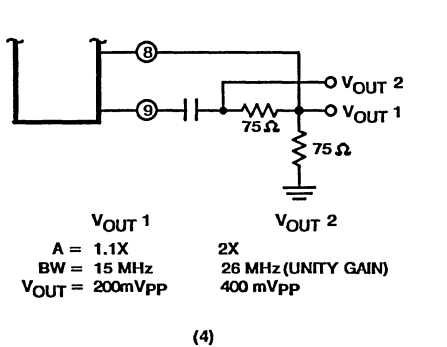
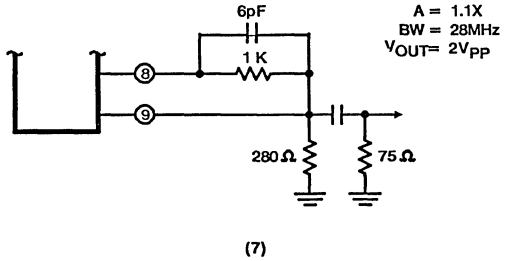
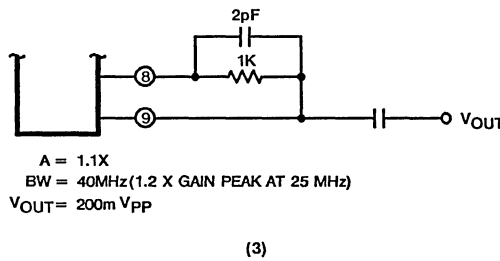
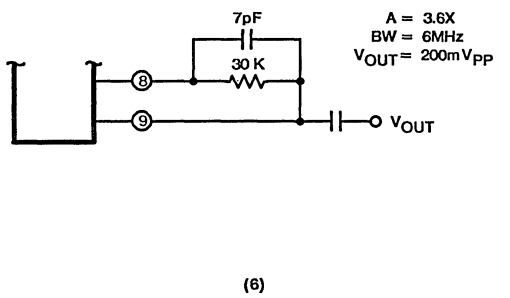
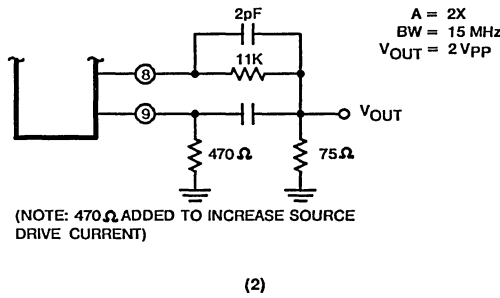
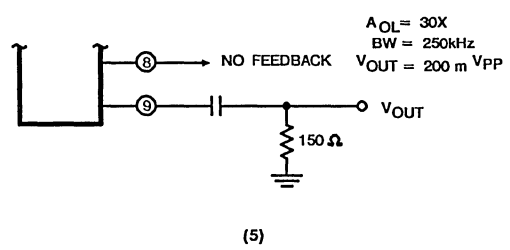
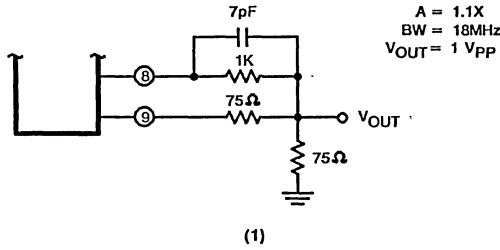


FIGURE 6. OTHER TABULATED RESULTS FOR VARIATIONS OF LOAD AND FEEDBACK FOR CIRCUIT, FIGURE 2b;  $V_{CC} = +12V$ .

## ***Application of High Speed CMOS Analog Switches***

CMOS analog switches are available in a wide variety of forms, and have been known and used for some time. There are a number of advantages to using the CMOS transmission gate as a switch:

- Ideal suitability to series cascade arrangements.
- Simple multiple parallel input switching arrangements.
- No bipolar junctions and, hence, no offset.
- Very low power consumption.
- Wide signal-swing capability.
- Fast multiplexing and video switching in high-speed CMOS.
- Wide bandwidth in high-speed CMOS.
- Low  $R_{ON}$  channel resistance in high-speed CMOS.
- Bidirectional signal handling.

### ***An Integrated Video-Switch Amplifier***

Commonly, integrated video-switch amplifiers have been fabricated in the bipolar technology using differential amplifiers in a current-switching mode. In this form, two differential pairs are needed for two input-signal sources. The handling of multiple sources is very much more complex. The advantages of the CMOS video-switch amplifier have already been noted. While the bipolar video switch has high output drive and switching speed as advantages, the price is high in voltage offset and current drain. The integrated device solution that is offered here is in the use of the BiMOS technology, where both the CMOS and bipolar processes complement each other to provide CMOS switching with bipolar amplifiers. The BiMOS process allows several CMOS switches to be coupled to a bipolar drive-amplifier in the same process to exploit the best of two technologies.

Other advantages are gained when the BiMOS process is used for an IC video-switch amplifier design. The BiMOS process calls for a p-substrate and, therefore, isolated n-epitaxial layers can be built for both n and p channel parts. The layers provide for better isolation of the n and p channels. The n and p wells in a transmission-gate cell can be switched between source and rail; therefore, they have a smaller body effect on both n and p devices, which results in better gain linearity. Where desired, oxide capacitors are available for bipolar amplifier compensation.

### **CA3256 Video-Switch Amplifier**

The block diagram of Figure 1 shows the functional diagram of the CA3256, which consists of five MOS channels, each comprising a three-element T-switch. The output of the five switches is made common and fed into the input of a bipolar buffer amplifier. The T-switch, together with the input impedance of the buffer, is typically  $10k\Omega$ , and has an insertion loss of approximately 0.8dB. The T-switch was designed to handle up to 3Vpp input signal with low distortion. The T-switches of the CA3256 conform to a break-before-make format; hence, shorting to ground is eliminated.

The amplifier is programmable for gain and, typically, can provide a gain of 1 times into a  $75\Omega$  load or a gain of 5 times into a  $1k\Omega$  load. The maximum output signal swing with linearity is greater than 5Vpp for ( $V_{CC} - V_{EE}$ ) greater than or equal to 12 volts, while the maximum output current is approximately 20mA. The amplifier has base-current compensation to reduce offset and a temperature compensated 5-volt zener referenced bias. Other features include LED-selector indicators for channels 1 through 4. The fifth channel is independently selectable for use as a separate input or output in parallel with any on channel, and may be used as a monitor, or for pass-through, signal summing, or parallel distribution.

In the application, the user has the option to specify  $-5$  volts  $V_{EE}$  for the switch and a ground reference for the amplifier input and output. Alternatively, the CA3256 may be used with a single +12 volt supply. The logic select for channels 1 through 4 is controlled by the A, B and Inhibit lines with ground to  $V_{CC}$  logic switching. The logic threshold is approximately  $V_{CC}/2$  independent of the  $-V_{EE}$  voltage level. DC coupling may also be used at the output (when  $V_{EE}$  is returned to a  $-5$  volt supply). For the circuit of Figure 2(b), AC coupling is used at the output and input. The switching bias arrangement shown provides for stable bias across each switch when in the off position to minimize transients when the input is switched.

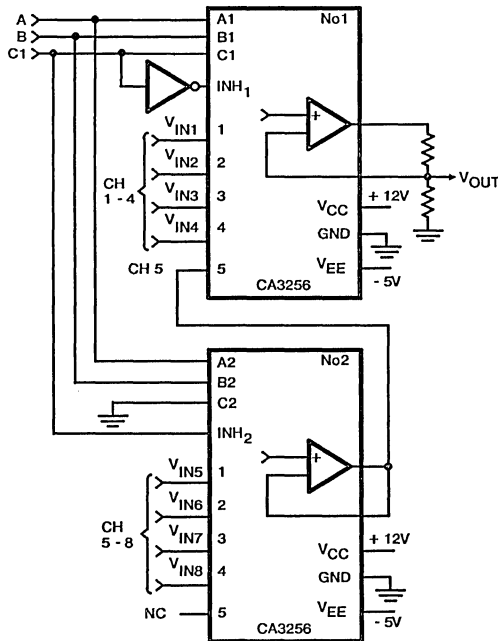
Any combination of switch input circuits can be configured with multiple, parallel, line-drive outputs. The video-switch amplifier circuit of Figure 7 illustrates how the CA3256 may be configured in pairs to provide an 8-to-1 video-switch amplifier using a 3-bit address to select the input. It is also possible to use the fifth channel input to tie signals to a common bus line for distribution from the selected amplifier; however, distributed capacitance loading will result in reduced bandwidth. The 4 plus 1 combination of input-signal switching provides for a wide assortment of video-switch circuit configurations.

## CA3256

While the BiMOS process does provide some compromises for both the switch and the amplifier, the combined system is capable of the performance needed in most high-quality, switching applications. As an integrated system, many of the problems in pc-board layout are simplified, and there is a reduction in component count. In its simplest form, with +12 and -5 volt supplies, the CA3256 may be DC connected at the input and output; the LED indicators need not be connected. A DC level translator resolves the channel switch control at the  $-V_{EE}$  voltage level. Under these conditions, the circuit may be as simple as the one in Figure 7.

### Summary

While each video-switch amplifier is designed for a specific application and, to that end, is tailored as far as performance to a given set of specifications, the circuit-designer's goal is generally the same in every case: to make the best possible switch for the lowest cost. In this respect, the CA3256 IC switch and amplifier discussed provide an excellent choice for a cost-effective high-performance video-switch amplifier, by taking advantage of the complementary features of both high-speed CMOS and bipolar integrated circuits.



TRUTH TABLE

| CH | C1 | A | B |
|----|----|---|---|
| 1  | 0  | 0 | 0 |
| 2  | 0  | 0 | 1 |
| 3  | 0  | 1 | 0 |
| 4  | 0  | 1 | 1 |
| 5  | 1  | 0 | 0 |
| 6  | 1  | 0 | 1 |
| 7  | 1  | 1 | 0 |
| 8  | 1  | 1 | 1 |

FIGURE 7. AN 8-TO-1 VIDEO-SWITCH AMPLIFIER USING TWO CA3256 DEVICES.

## Sync Generator for TV Applications and Video Processing Systems

August 1991

### Features

- Interlaced Composite Sync Output
- Automatic Genlock Capability
- Crystal Oscillator Operation
- 525 or 625 Line Operation
- Vertical Reset Option
- Wide Power Supply Operating Voltage .... 4-15V

### Applications

- Cameras
- Monitors and Displays
- CATV
- Teletext
- Video Games
- Sync Restorer
- Video Service Instruments

### Description

The Harris CD22402\* is a CMOS LSI sync generator that produces all the timing signals required to drive a fully 2-to-1 interlaced 525-line 30-frame/second, or 625-line 25-frame/second TV camera or video processing system. A complete sync waveform is produced which begins each field with six serrated vertical sync pulses, preceded and followed by six half-width double frequency equalizing pulses. The sync output is gated by the master clock to preserve horizontal phase continuity during the vertical interval.

The CD22402 can be operated either in "genlock" mode, in which it is synchronized with a reference sync pulse train from another TV camera, or in "stand-alone" mode, in which it is synchronized with a local on-chip crystal oscillator (the crystal and two passive components are off chip). Also, the circuit can sense the presence or absence of a reference sync pulse train and automatically select the "genlock" or "stand-alone" mode.

A frame sync pulse is produced at the beginning of every odd field. The vertical counter can be reset to either the first equalizing pulse or the first vertical sync pulse of the vertical interval.

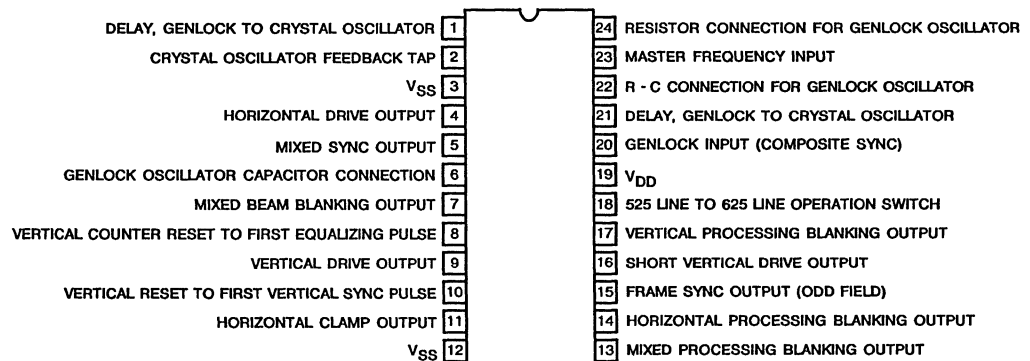
The interlaced sync provided by the CD22402 differs from RS-170 by having slightly narrower sync and equalizing pulses. The clock frequency of 32 times horizontal rate allows for approximately 4 $\mu$ s horizontal pulse widths and 2 $\mu$ s equalizing pulses. Otherwise operation can be phase locked to a color sub-carrier for a full interlaced operating system.

The CD22402 is operable with a single supply over a voltage range of from 4 to 15 volts. It is supplied in a 24-lead dual-in-line ceramic package (D suffix) or a 24-lead dual-in-line plastic package (E suffix).

\* Formerly RCA Developmental Type No. TA6993.

### Pinout

CD22402D CERAMIC PACKAGE AND CD22402E PLASTIC PACKAGE  
TOP VIEW



# Specifications CD22402

## MAXIMUM RATINGS, Absolute-Maximum Values:

|   |  |
|---|--|
| DC SUPPLY-VOLTAGE ( $V_{DD}$ )<br>(Voltage referenced to $V_{SS}$ terminal)   | 15 V   |
| INPUT VOLTAGE RANGE, ALL INPUTS   | $V_{SS} \leq V_i \leq V_{DD}$                        |
| DC INPUT CURRENT, ANY ONE INPUT   | $\pm 10$ mA  |
| POWER DISSIPATION PER PACKAGE ( $P_D$ ):                                      |  |
| For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)                       | 500 mW   |
| For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)                       | Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW |
| For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE D)                      | 500 mW   |
| For $T_A = +100$ to $125^\circ\text{C}$ (PACKAGE TYPE D)                      | Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR                                      |  |
| For $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$         | 100 mW   |
| OPERATING-TEMPERATURE RANGE ( $T_A$ ):  |  |
| PACKAGE TYPE D  | $-55$ to $+125^\circ\text{C}$                        |
| PACKAGE TYPE E  | $-40$ to $+85^\circ\text{C}$                         |
| STORAGE-TEMPERATURE RANGE ( $T_{stg}$ )                                       | $-65$ to $+150^\circ\text{C}$                        |
| LEAD TEMPERATURE (DURING SOLDERING):  |  |
| At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s max. | $+265^\circ\text{C}$                                 |

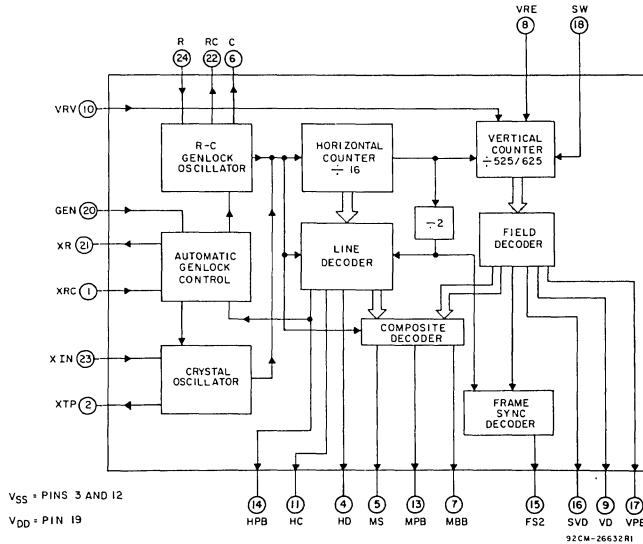


Fig. 1 - Block diagram of CD22402 monochrome TV sync generator with automatic genlock.

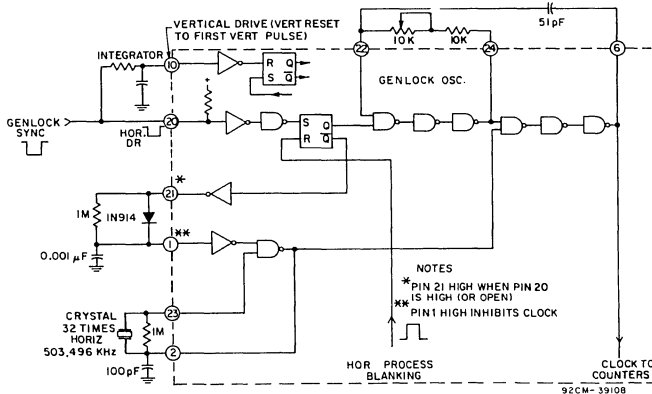


Fig. 1a - Logic detail of the oscillator/genlock portion of the CD22402.

8  
SPECIAL  
ANALOG CIRCUITS



## CD22402

### TERMINAL DEFINITIONS FOR RCA CD22402 SYNC GENERATOR

| Terminal No. | Symbol          | Function   |
|--------------|-----------------|--|
| 1            | XRC             | <b>Delay, Genlock to Crystal Oscillator.</b> Resistor, diode and capacitor connection for delay that automatically turns on the crystal oscillator when the genlock input is removed. When the signal on terminal 1 is high the crystal oscillator is inhibited. Typical values for R and C are 1 M $\Omega$ and 0.001 $\mu$ F. For operation as a crystal-controlled stand-alone sync generator without genlock, terminal 1 should be hard-wired to V <sub>SS</sub> .   |
| 2            | XTP             | <b>Crystal Oscillator Feedback Tap.</b> Feedback connection (tap) for crystal oscillator. When a crystal (shunted by a 1 M $\Omega$ resistor) is connected between this terminal and terminal 23, and a 100-pF capacitor is connected from this terminal to V <sub>SS</sub> , the sync generator creates its own master frequency. For a 525-line, 30-frame/second raster, the crystal frequency is 504.000 kHz*; and for a 625-line, 25-frame/second raster, the crystal frequency is 500.000 kHz*.   |
| 3            | V <sub>SS</sub> | <b>Negative Power Supply Voltage.</b> This terminal must be hard-wired to terminal 12 (V <sub>SS</sub> ).  |
| 4            | HD              | <b>Horizontal Drive Output.</b>  |
| 5            | MS              | <b>Mixed Sync Output.</b>  |
| 6            | C               | <b>Capacitor Connection for R-C Genlock Oscillator.</b>  |
| 7            | MBB             | <b>Mixed Beam Blanking Output.</b>   |
| 8            | VRE             | <b>Vertical Counter Reset to First Equalizing Pulse.</b> A low-level signal on this terminal resets the vertical counter to the first equalizing pulse of a field. When not in use this terminal should be connected to V <sub>DD</sub> .  |
| 9            | VD              | <b>Vertical Drive Output.</b>  |
| 10           | VRV             | <b>Vertical Counter Reset to First Vertical Sync Pulse.</b> A low-level signal on this terminal resets the sync generator to the first vertical sync pulse of a field. For genlock operation, terminal 10 is used as a resistor and capacitor connection for an integrator network that detects vertical sync pulses in a master sync waveform to which the sync generator is to be genlocked. R is 22 K $\Omega$ , and C is 0.001 pF. When not in use this terminal should be connected to V <sub>DD</sub> .  |
| 11           | HC              | <b>Horizontal Clamp Output.</b>  |
| 12           | V <sub>SS</sub> | <b>Negative Power Supply Voltage.</b>  |
| 13           | MPB             | <b>Mixed Processing Blanking Output.</b>   |
| 14           | HPB             | <b>Horizontal Processing Blanking Output.</b>  |
| 15           | FS2             | <b>Frame Sync Output (Odd Field).</b> A pulse coinciding with the first equalizing pulse is produced at the beginning of every odd field.  |
| 16           | SVD             | <b>Short Vertical Drive Output.</b>  |
| 17           | VPB             | <b>Vertical Processing Blanking Output.</b>  |
| 18           | SW              | <b>Operation Switch for 525-Line or 625-Line Raster.</b> A high-level signal on terminal 18 causes the sync generator to generate a 625-line raster. An internal pull-down resistor is connected to terminal 18, so in the absence of an applied input to this terminal, a 525-line raster is produced.  |
| 19           | V <sub>DD</sub> | <b>Positive Power Supply Voltage.</b> V <sub>DD</sub> can be any voltage between +4 and +15 relative to V <sub>SS</sub> .  |
| 20           | GEN             | <b>Genlock Input Composite Sync.</b> A negative-going reference mixed sync waveform applied to terminal 20 disables the crystal oscillator and locks the R-C genlock oscillator to the horizontal pulses of the reference sync waveform. Vertical sync detection is achieved by an R-C integrator connected from terminal 20 to terminal 10 (vertical reset to first vertical sync pulse). An internal pull-up resistor is connected to terminal 20 so that in the absence of an applied input the crystal oscillator is enabled and the R-C genlock oscillator is disabled. |
| 21           | XR              | <b>Delay, Genlock to Crystal Oscillator, Resistor and Diode Connection for Delay, Genlock to Crystal Oscillator.</b> Automatically turns on the crystal oscillator when the input to terminal 20 is removed.   |
| 22           | RC              | <b>Resistor and Capacitor Connection for Genlock Oscillator.</b> If the genlock oscillator is not used this terminal should be connected to V <sub>SS</sub> . C should be 100 pF, and R should be a 10-K $\Omega$ potentiometer.   |
| 23           | XIN             | <b>Master Frequency Input.</b>   |
| 24           | R               | <b>Resistor Connection for Genlock Oscillator.</b>   |

\*32 times horizontal frequency.

# CD22402

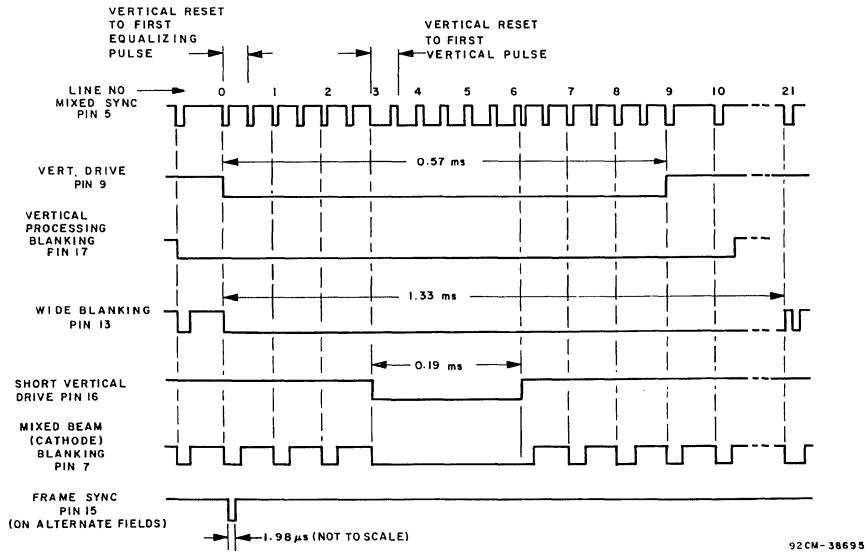
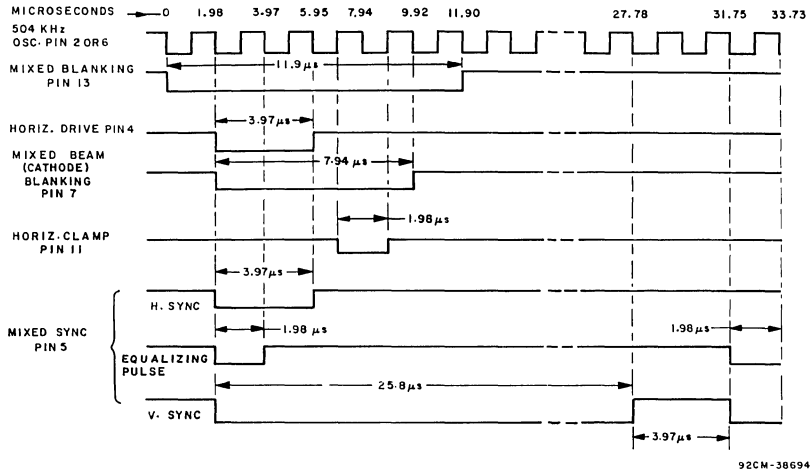


Fig. 2 - Sync generator timing - 525/60 Hz.

# CD22402

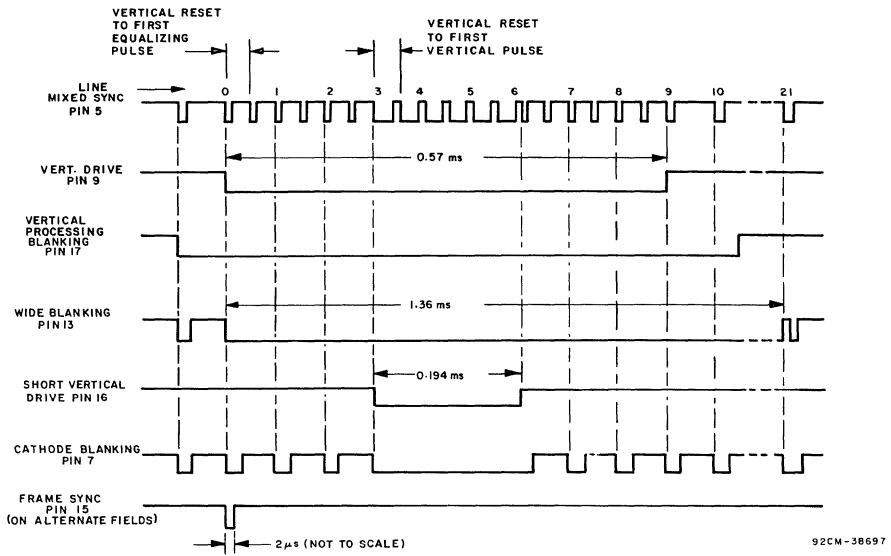
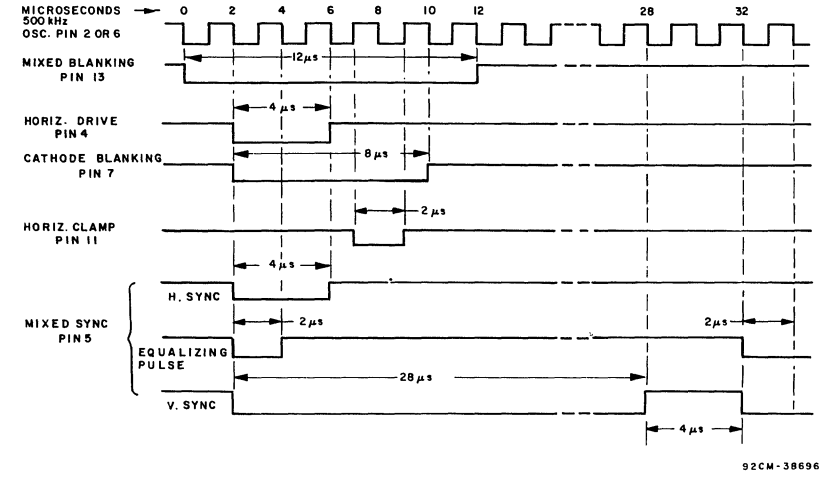


Fig. 3 - Sync generator timing - 625/50 Hz.

# CD22402

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC  | TEST CONDITIONS         |                     | LIMITS |      |      |       |      |      |        |      |      | UNITS |
|---|-------------------------|---------------------|--------|------|------|-------|------|------|--------|------|------|-------|
|   |                         |                     | -55°C  |      |      | +25°C |      |      | +125°C |      |      |       |
|   | V <sub>O</sub> (V)      | V <sub>DD</sub> (V) | Min.   | Typ. | Max. | Min.  | Typ. | Max. | Min.   | Typ. | Max. |       |
| Quiescent Device Current<br>I <sub>DD</sub>                         |                         | 5                   | —      | —    | —    | 0.5   | 0.75 | 1    | —      | —    | —    | mA    |
|   |                         | 10                  | —      | —    | —    | 1.5   | 2    | 2.5  | —      | —    | —    |       |
|   |                         | 15                  | —      | —    | —    | 3     | 4    | 5    | —      | —    | —    |       |
| Output Voltage<br>Low-Level<br>V <sub>OL</sub>                      |                         | 5                   | —      | —    | 0.01 | —     | —    | 0.01 | —      | —    | 0.05 | V     |
|   |                         | 10                  | —      | —    | 0.01 | —     | —    | 0.01 | —      | —    | 0.05 |       |
| High-Level<br>V <sub>OH</sub>                                       |                         | 5                   | 4.99   | —    | —    | 4.99  | —    | —    | 4.95   | —    | —    |       |
|   |                         | 10                  | 9.99   | —    | —    | 9.99  | —    | —    | 9.95   | —    | —    |       |
| Threshold Voltage<br>(N-Channel)<br>V <sub>THN</sub>                | I <sub>D</sub> = 10 μA  |                     | —      | 1.7  | —    | 1     | 1.5  | 2.6  | —      | 1.3  | —    |       |
| (P-Channel)<br>V <sub>THP</sub>                                     | I <sub>D</sub> = -10 μA |                     | —      | -1.7 | —    | -1    | -1.5 | -2.6 | —      | -1.3 | —    |       |
| Noise Immunity<br>(Any Input)<br>V <sub>NL</sub><br>V <sub>NH</sub> |                         | 5                   | 1.5    | —    | —    | 1.5   | 2.25 | —    | 1.4    | —    | —    |       |
|   |                         | 10                  | 3      | —    | —    | 3     | 4.5  | —    | 2.9    | —    | —    |       |
|   |                         | 5                   | 1.4    | —    | —    | 1.5   | 2.25 | —    | 1.5    | —    | —    |       |
|   |                         | 10                  | 2.9    | —    | —    | 3     | 4.5  | —    | 3      | —    | —    |       |
| Output SINK Current<br>(N-Channel)<br>I <sub>DN</sub>               | 0.5                     | 5                   | 100    | —    | —    | 80    | 160  | —    | 56     | —    | —    | μA    |
|   | 5                       |                     | 1200   | —    | —    | 960   | 1920 | —    | 672    | —    | —    |       |
|   | 0.5                     | 10                  | 248    | —    | —    | 200   | 400  | —    | 140    | —    | —    |       |
|   | 10                      |                     | 3000   | —    | —    | 2400  | 4800 | —    | 1680   | —    | —    |       |
| Output SOURCE Current<br>(P-Channel)<br>I <sub>DP</sub>             | 4.5                     | 5                   | 200    | —    | —    | 80    | 160  | —    | 56     | —    | —    |       |
|   | 0                       |                     | 1200   | —    | —    | 960   | 1920 | —    | 672    | —    | —    |       |
|   | 9.5                     | 10                  | 248    | —    | —    | 200   | 400  | —    | 140    | —    | —    |       |
|   | 0                       |                     | 3000   | —    | —    | 2400  | 4800 | —    | 1680   | —    | —    |       |
| Input Current<br>(Each Input)<br>I <sub>I</sub>                     |                         | —                   | —      | —    | —    | 10    | —    | —    | —      | —    | pA   |       |

## DYNAMIC ELECTRICAL CHARACTERISTICS at T<sub>A</sub> = 25°C and C<sub>L</sub> = 15 pF Typical Temperature Coefficient for All Values of V<sub>DD</sub> = 0.3%/°C

| CHARACTERISTIC   | TEST CONDITIONS | LIMITS              |      |      | UNITS |                                       |    |   |    |    |
|--|-----------------|---------------------|------|------|-------|---------------------------------------|----|---|----|----|
|  |                 | V <sub>DD</sub> (V) | MIN. | TYP. |       | MAX.                                  |    |   |    |    |
| Output State<br>Propagation Delay Time<br>(50% to 50%) |                 |                     |      |      | ns    |                                       |    |   |    |    |
|  |                 |                     |      |      |       | Low-to-High Level<br>t <sub>PLH</sub> | 5  | — | 40 | 80 |
|  |                 |                     |      |      |       | High-to-Low Level<br>t <sub>PHL</sub> | 10 | — | 20 | 40 |
| Transition Time<br>(10% to 90%)                        |                 |                     |      |      | ns    |                                       |    |   |    |    |
|  |                 |                     |      |      |       | Low-to-High<br>t <sub>TLH</sub>       | 5  | — | 45 | 90 |
|  |                 |                     |      |      |       | High-to-Low<br>t <sub>THL</sub>       | 10 | — | 30 | 60 |
| Input Capacity (Per Input)<br>C <sub>I</sub>           |                 |                     |      |      | pF    |                                       |    |   |    |    |

# CD22402

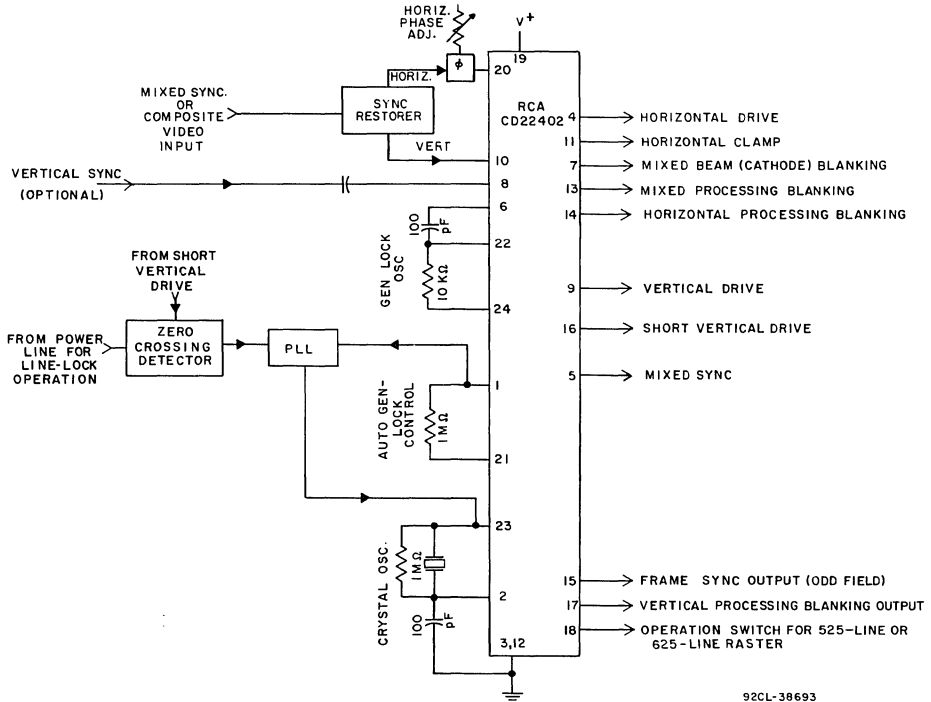


Fig. 4 - Typical application in a TV camera.

## Wideband Two Quadrant Analog Multiplier

August 1991

### Features

- High Speed Voltage Output ..... 300V/μs
- Low Multiplication Error ..... 1.6%
- Input Bias Currents ..... 1.2μA
- Signal Input Feedthrough ..... -52dB
- Wide Signal Bandwidth ..... 30MHz
- Wide Control Bandwidth ..... 17MHz
- Gain Flatness to 5 MHz ..... 0.10dB

### Applications

- Military Avionics
- Missile Guidance Systems
- Medical Imaging Displays
- Video Mixers
- Sonar AGC Processors
- Radar Signal Conditioning
- Voltage Controlled Amplifier
- Vector Generator

### Description

The HA-2546 is a monolithic, high speed, two quadrant, analog multiplier constructed in the Harris Dielectrically Isolated High Frequency Process. The high frequency performance of the HA-2546 rivals the best analog multipliers currently available including hybrids.

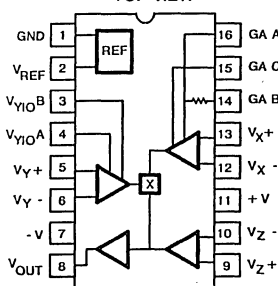
The HA-2546 has a voltage output with a 30MHz signal bandwidth, 300V/μs slew rate and a 17MHz control input bandwidth. High bandwidth and slew rate make this part an ideal component for use in video systems. The suitability for precision video applications is demonstrated further by the 0.1dB gain flatness to 5MHz, 1.6% multiplication error, -52dB feedthrough and differential inputs with 1.2μA bias currents. The HA-2546 also has low differential gain (0.1%) and phase (0.1°) errors.

The HA-2546 is well suited for AGC circuits as well as mixer applications for sonar, radar, and medical imaging equipment. The voltage output of the HA-2546 simplifies many designs by eliminating the current-to-voltage conversion stage required for current output multipliers.

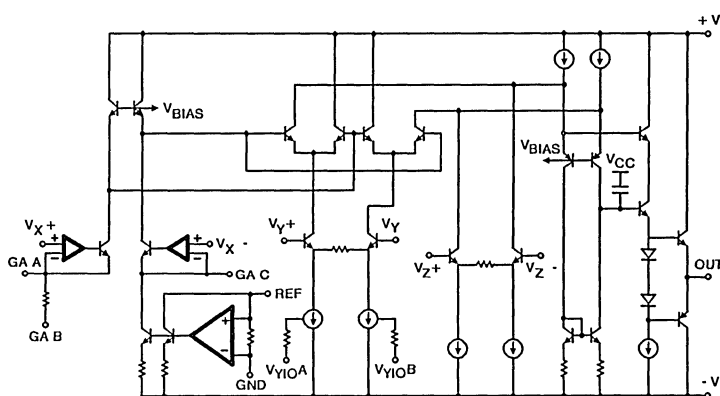
The HA-2546-9 has guaranteed operation from -40°C to +85°C. The HA-2546-5 has guaranteed operation from 0°C to +75°C. The HA-2546 is available in a 16 pin Ceramic DIP. For MIL-STD-883 compliant product and LCC packages consult the HA-2546/883 datasheet.

### Pinout

HA1-2546 (CERAMIC DIP)  
TOP VIEW



### Simplified Schematic



## Specifications HA-2546

### Absolute Maximum Ratings (Note 1)

|   |        |
|---|--------|
| Voltage Between V+ and V- Terminals ..... | 35V    |
| Differential Input Voltage .....          | 6V     |
| Output Current .....                      | ±60mA  |
| Maximum Junction Temperature .....        | +175°C |

### Operating Temperature Range

|                                 |                                 |
|---------------------------------|---------------------------------|
| HA-2546-9 .....                 | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| HA-2546-5 .....                 | 0°C ≤ T <sub>A</sub> ≤ +75°C    |
| Storage Temperature Range ..... | -65°C ≤ T <sub>A</sub> ≤ +150°C |

### Electrical Specifications V+ = 15V, V- = -15V, R<sub>L</sub> = 1K, C<sub>L</sub> = 50pF, Unless Otherwise Specified

| PARAMETER   | TEMP  | HA-2546-9 |       |     | HA-2546-5 |       |     | UNITS  |
|---|-------|-----------|-------|-----|-----------|-------|-----|--------|
|   |       | MIN       | TYP   | MAX | MIN       | TYP   | MAX |        |
| <b>MULTIPLIER PERFORMANCE</b>                     |       |           |       |     |           |       |     |        |
| Multiplication Error (Note 2)                     | +25°C | -         | 1.6   | 3   | -         | 1.6   | 3   | %      |
|   | Full  | -         | 3.0   | 7   | -         | 3.0   | 7   | %      |
| Multiplication Error Drift                        | Full  | -         | 0.003 | -   | -         | 0.003 | -   | %/°C   |
| Differential Gain (Note 3,11)                     | +25°C | -         | 0.1   | 0.2 | -         | 0.1   | 0.2 | %      |
| Differential Phase (Note 3,11)                    | +25°C | -         | 0.1   | 0.3 | -         | 0.1   | 0.3 | Deg.   |
| Gain Flatness (Note 6,11)                         |       |           |       |     |           |       |     |        |
| DC to 5 MHz                                       | +25°C | -         | 0.1   | 0.2 | -         | 0.1   | 0.2 | dB     |
| 5 MHz to 8 MHz                                    | +25°C | -         | 0.18  | 0.3 | -         | 0.18  | 0.3 | dB     |
| Scale Factor Error                                | Full  | -         | 0.7   | 5.0 | -         | 0.7   | 5.0 | %      |
| 1% Amplitude Bandwidth Error                      | +25°C | -         | 6     | -   | -         | 6     | -   | MHz    |
| 1% Vector Bandwidth Error                         | +25°C | -         | 260   | -   | -         | 260   | -   | kHz    |
| THD + N (Note 4)                                  | +25°C | -         | 0.03  | -   | -         | 0.03  | -   | %      |
| Voltage Noise (Note 17)                           |       |           |       |     |           |       |     |        |
| f <sub>o</sub> =10Hz                              | +25°C | -         | 400   | -   | -         | 400   | -   | nV/√Hz |
| f <sub>o</sub> =100Hz                             | +25°C | -         | 150   | -   | -         | 150   | -   | nV/√Hz |
| f <sub>o</sub> =1kHz                              | +25°C | -         | 75    | -   | -         | 75    | -   | nV/√Hz |
| Common Mode Range                                 | +25°C | -         | ±9    | -   | -         | ±9    | -   | Volts  |
| <b>SIGNAL INPUT, V<sub>Y</sub></b>                |       |           |       |     |           |       |     |        |
| Input Offset Voltage                              | +25°C | -         | 3     | 10  | -         | 3     | 10  | mV     |
|   | Full  | -         | 8     | 20  | -         | 8     | 20  | mV     |
| Average Offset Voltage Drift                      | Full  | -         | 45    | -   | -         | 45    | -   | μV/°C  |
| Input Bias Current                                | +25°C | -         | 7     | 15  | -         | 7     | 15  | μA     |
|   | Full  | -         | 10    | 15  | -         | 10    | 15  | μA     |
| Input Offset Current                              | +25°C | -         | 0.7   | 2   | -         | 0.7   | 2   | μA     |
|   | Full  | -         | 1.0   | 3   | -         | 1.0   | 3   | μA     |
| Differential Input Resistance                     | +25°C | -         | 720   | -   | -         | 720   | -   | kΩ     |
| Small Signal Bandwidth (-3dB) (Note 6)            | +25°C | -         | 30    | -   | -         | 30    | -   | MHz    |
| Full Power Bandwidth (Note 5)                     | +25°C | -         | 9.5   | -   | -         | 9.5   | -   | MHz    |
| Feedthrough (Note 15)                             | +25°C | -         | -52   | -   | -         | -52   | -   | dB     |
| CMRR (Note 7)                                     | Full  | 60        | 78    | -   | 60        | 78    | -   | dB     |
| <b>V<sub>Y</sub> TRANSIENT RESPONSE (Note 12)</b> |       |           |       |     |           |       |     |        |
| Slew Rate (Note 8)                                | +25°C | -         | 300   | -   | -         | 300   | -   | V/μs   |
| Rise Time (Note 9)                                | +25°C | -         | 11    | -   | -         | 11    | -   | ns     |
| Overshoot (Note 9)                                | +25°C | -         | 17    | -   | -         | 17    | -   | %      |
| Propagation Delay                                 | +25°C | -         | 25    | -   | -         | 25    | -   | ns     |
| Settling Time (Note 8) 0.1%                       | +25°C | -         | 200   | -   | -         | 200   | -   | ns     |

## Specifications HA-2546

**Electrical Specifications (Continued)**  $V_+ = 15V, V_- = -15V, R_L = 1K, C_L = 50pF$ , Unless Otherwise Specified

| PARAMETER  | TEMP  | HA-2546-9 |            |     | HA-2546-5 |            |     | UNITS            |
|--|-------|-----------|------------|-----|-----------|------------|-----|------------------|
|  |       | MIN       | TYP        | MAX | MIN       | TYP        | MAX |                  |
| <b>CONTROL INPUT, <math>V_X</math></b>               |       |           |            |     |           |            |     |                  |
| Input Offset Voltage                                 | +25°C | -         | 0.3        | 2   | -         | 0.3        | 2   | mV               |
|  | Full  | -         | 3          | 20  | -         | 3          | 20  | mV               |
| Average Offset Voltage Drift                         | Full  | -         | 10         | -   | -         | 10         | -   | $\mu V/^\circ C$ |
| Input Bias Current                                   | +25°C | -         | 1.2        | 2   | -         | 1.2        | 2   | $\mu A$          |
|  | Full  | -         | 1.8        | 5   | -         | 1.8        | 5   | $\mu A$          |
| Input Offset Current                                 | +25°C | -         | 0.3        | 2   | -         | 0.3        | 2   | $\mu A$          |
|  | Full  | -         | 0.4        | 3   | -         | 0.4        | 3   | $\mu A$          |
| Differential Input Resistance                        | +25°C | -         | 360        | -   | -         | 360        | -   | k $\Omega$       |
| Small Signal Bandwidth (-3dB) (Note 13)              | +25°C | -         | 17         | -   | -         | 17         | -   | MHz              |
| Feedthrough (Note 16)                                | +25°C | -         | -40        | -   | -         | -40        | -   | dB               |
| Common Mode Rejection Ratio (Note 19)                | +25°C | -         | 80         | -   | -         | 80         | -   | dB               |
| <b><math>V_X</math> TRANSIENT RESPONSE (Note 12)</b> |       |           |            |     |           |            |     |                  |
| Slew Rate (Note 19)                                  | +25°C | -         | 95         | -   | -         | 95         | -   | V/ $\mu s$       |
| Rise Time (Note 20)                                  | +25°C | -         | 20         | -   | -         | 20         | -   | ns               |
| Overshoot (Note 20)                                  | +25°C | -         | 17         | -   | -         | 17         | -   | %                |
| Propagation Delay                                    | +25°C | -         | 50         | -   | -         | 50         | -   | ns               |
| Settling Time (Note 19) 0.1%                         | +25°C | -         | 200        | -   | -         | 200        | -   | ns               |
| <b><math>V_Z</math> CHARACTERISTICS</b>              |       |           |            |     |           |            |     |                  |
| Input Offset Voltage (Note 17)                       | +25°C | -         | 4          | 15  | -         | 4          | 15  | mV               |
|  | Full  | -         | 8          | 20  | -         | 8          | 20  | mV               |
| Open Loop Gain                                       | +25°C | -         | 70         | -   | -         | 70         | -   | dB               |
| Differential Input Resistance                        | +25°C | -         | 900        | -   | -         | 900        | -   | k $\Omega$       |
| <b>OUTPUT CHARACTERISTICS</b>                        |       |           |            |     |           |            |     |                  |
| Output Voltage Swing (Note 18)                       | Full  | -         | $\pm 6.25$ | -   | -         | $\pm 6.25$ | -   | Volts            |
| Output Current                                       | Full  | $\pm 20$  | $\pm 45$   | -   | $\pm 20$  | $\pm 45$   | -   | mA               |
| Output Resistance                                    | +25°C | -         | 1          | -   | 1         | -          | -   | $\Omega$         |
| <b>POWER SUPPLY</b>                                  |       |           |            |     |           |            |     |                  |
| PSRR (Note 10)                                       | Full  | 58        | 63         | -   | 58        | 63         | -   | dB               |
| Supply Current                                       | Full  | -         | 23         | 29  | -         | 23         | 29  | mA               |

**NOTES:**

1. Absolute maximum ratings are limiting values, applied individually, beyond which the servability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Error is percent of full scale, 1% = 50mV.
3.  $f_o = 3.58MHz/4.43MHz, V_Y = 300mVp-p, 0$  to 1Vdc offset,  $V_X = 2V$ .
4.  $f_o = 10kHz, V_Y = 1Vrms, V_X = 2V$ .
5.  $V_X = 2V$ , Full Power Bandwidth calculated by equation:  

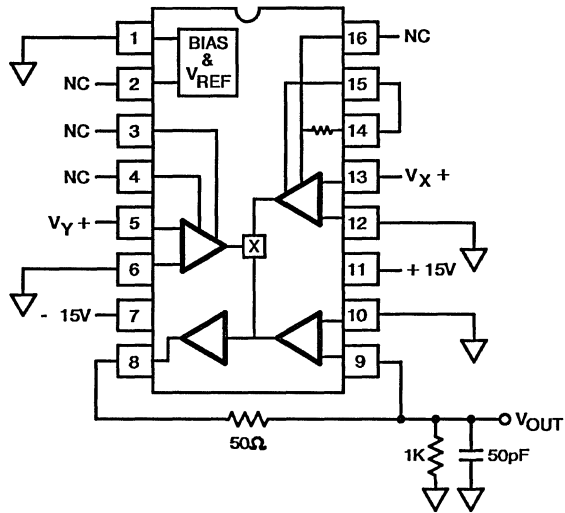
$$FPBW = \frac{\text{Slew Rate}}{2\pi V_{\text{peak}}}, V_{\text{peak}} = 5V.$$
6.  $V_X = 2V$ .
7.  $V_Y = 0$  to  $\pm 5V, V_X = 2V$ .
8.  $V_{OUT} = \pm 5V, V_X = 2V$ .
9.  $V_{OUT} = 0$  to  $\pm 100mV, V_X = 2V$ .
10.  $V_S = \pm 12V$  to  $\pm 15V, V_Y = 5V, V_X = 2V$ .
11. Guaranteed by characterization and not 100% tested.
12. See Test Circuit.
13.  $V_Y = 5V, V_{X-} = -1V$ .
15.  $f_o = 5MHz, V_X = 0, V_Y = 200mVrms$ .
16.  $f_o = 100kHz, V_Y = 0, V_{X+} = 200mVrms, V_{X-} = -0.5V$ .
17.  $V_X = V_Y = 0$ .
18.  $V_X = 2.5V, V_Y = \pm 5V$ .
19.  $V_X = 0$  to 2V,  $V_Y = 5V$ .
20.  $V_X = 0$  to 200mV,  $V_Y = 5V$ .

**8**  
 SPECIAL  
 ANALOG CIRCUITS



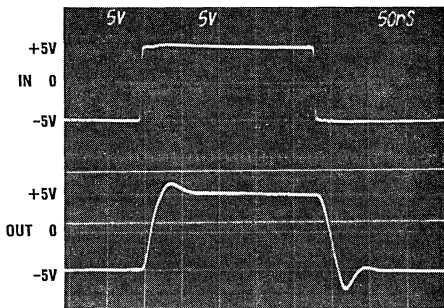
Test Circuits

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



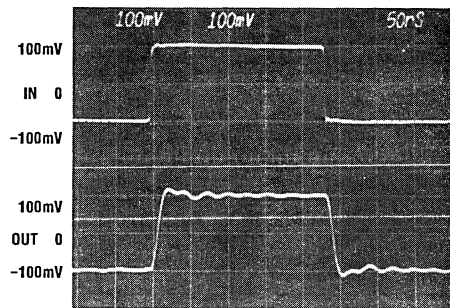
V<sub>Y</sub> LARGE SIGNAL RESPONSE

Vertical Scale: 5V/Div. Horizontal Scale: 50ns/Div.



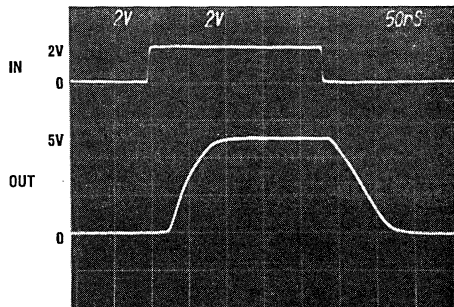
V<sub>Y</sub> SMALL SIGNAL RESPONSE

Vertical Scale: 100mV/Div. Horizontal Scale: 50ns/Div.



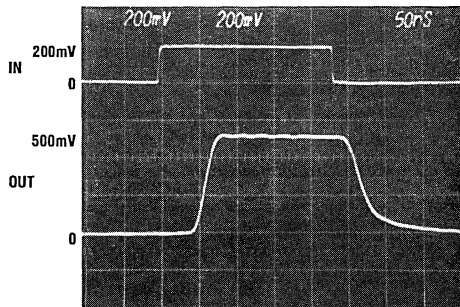
V<sub>X</sub> LARGE SIGNAL RESPONSE

Vertical Scale: 2V/Div. Horizontal Scale: 50ns/Div.



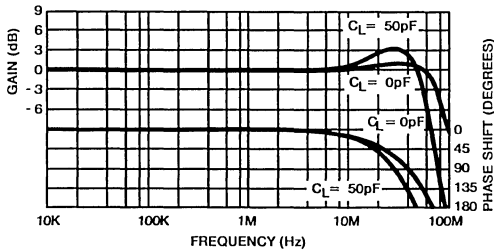
V<sub>X</sub> SMALL SIGNAL RESPONSE

Vertical Scale: 200mV/Div. Horizontal Scale: 50ns/Div.

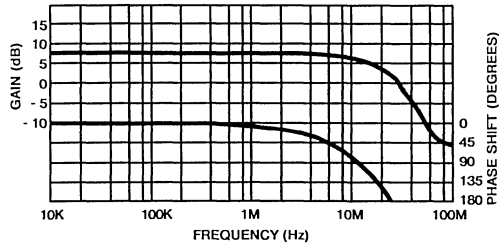


**Typical Performance Curves**  $V_S = \pm 15V$ ,  $T_A = +25^\circ C$ , See test circuit for multiplier configuration

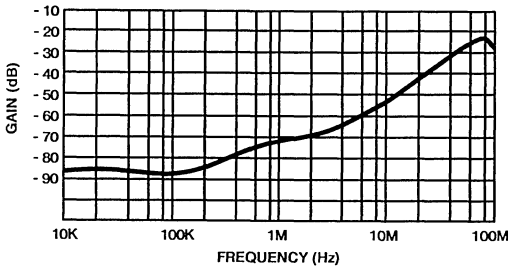
**$V_Y$  GAIN AND PHASE vs FREQUENCY**  
 $R_L = 1K$ ,  $V_X = 2V_{dc}$ ,  $V_Y = 200mV_{rms}$



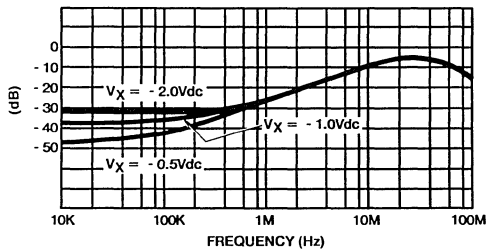
**$V_X$  GAIN AND PHASE vs FREQUENCY**  
 $R_L = 1K$ ,  $V_{X+} = 200mV_{rms}$ ,  $V_Y = 5V_{dc}$ ,  $V_{X-} = -1V_{dc}$



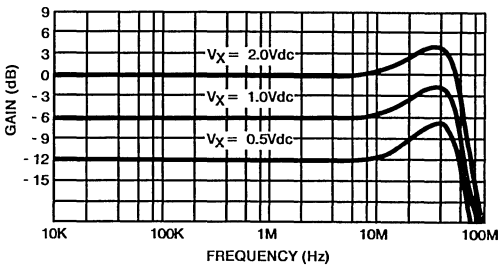
**$V_Y$  FEEDTHROUGH vs FREQUENCY**  
 $V_X = 0V$ ,  $R_L = 1K$ ,  $V_Y = 200mV_{rms}$



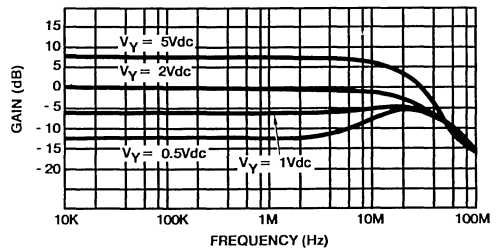
**$V_X$  FEEDTHROUGH vs FREQUENCY**  
 $R_L = 1K$ ,  $V_{X+} = 200mV_{rms}$ ,  $V_Y = 0V$



**VARIOUS  $V_Y$  FREQUENCY RESPONSES**  
 $R_L = 1K$ ,  $C_L = 50pF$ ,  $V_Y = 200mV_{rms}$

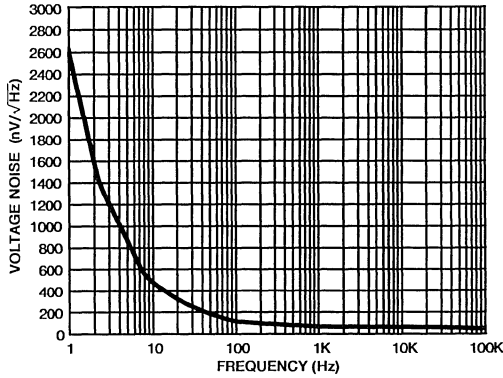


**VARIOUS  $V_X$  FREQUENCY RESPONSES**  
 $V_{X+} = 200mV_{rms}$ ,  $R_L = 1K$ ,  $V_{X-} = -1V_{dc}$

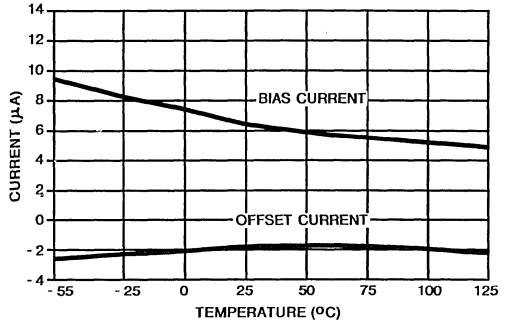


**Typical Performance Curves (Continued)**  $V_S = \pm 15V$ ,  $T_A = +25^\circ C$ , See test circuit for multiplier configuration

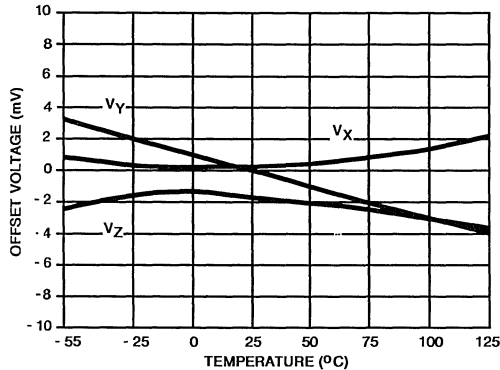
**NOISE CHARACTERISTICS**  
 $V_X = 0V$ ,  $V_Y = 0V$



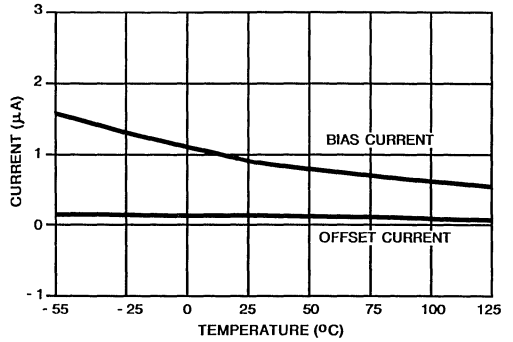
**$V_Y$  OFFSET AND BIAS CURRENT vs TEMPERATURE**



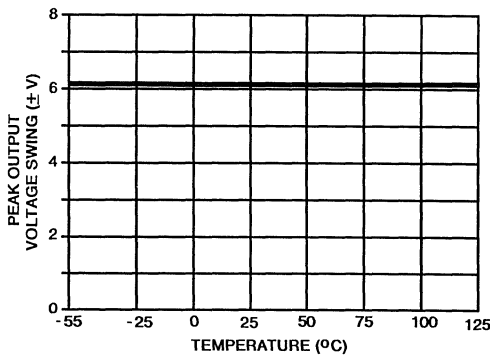
**OFFSET VOLTAGE vs TEMPERATURE**



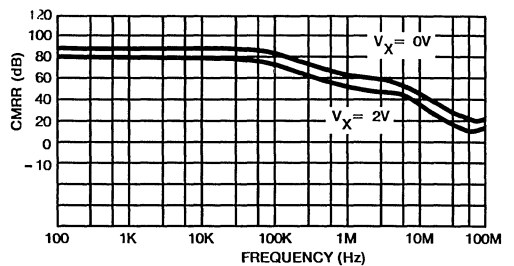
**$V_X$  OFFSET AND BIAS CURRENT vs TEMPERATURE**



**OUTPUT VOLTAGE SWING vs TEMPERATURE**

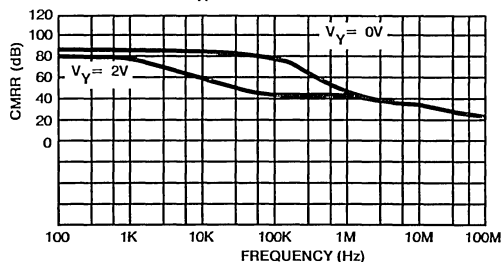


**$V_Y$  CMRR vs FREQUENCY**  
 $V_{Ycm} = 200mV_{rms}$

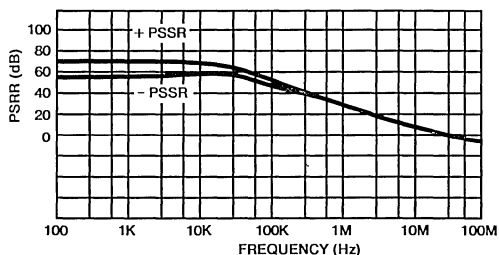


**Typical Performance Curves (Continued)**  $V_S = \pm 15V$ ,  $T_A = +25^\circ C$ , See test circuit for multiplier configuration

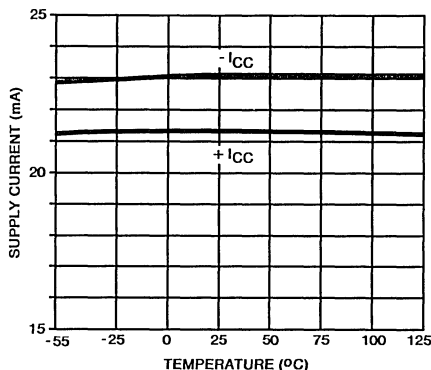
**$V_X$  COMMON MODE REJECTION RATIO vs FREQUENCY**  
 $V_Y = 200mV_{rms}$



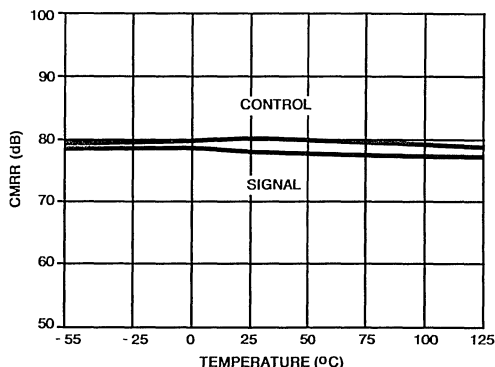
**PSRR vs FREQUENCY**  
 $V_Y = V_X = 0V$



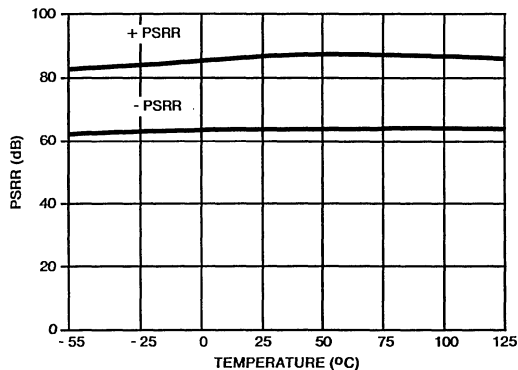
**SUPPLY CURRENT vs TEMPERATURE**



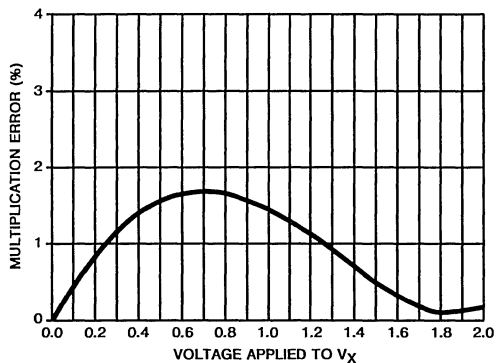
**SIGNAL/CONTROL CMRR vs TEMPERATURE**



**PSRR vs TEMPERATURE**

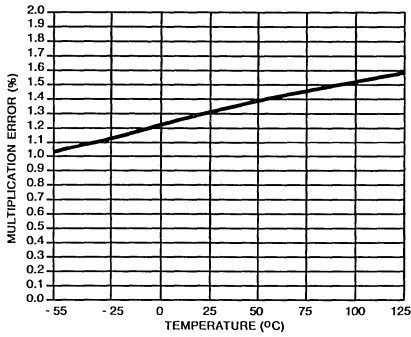


**MULTIPLICATION ERROR vs  $V_X$**



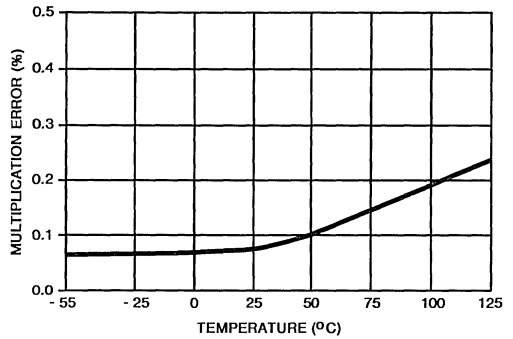
**Typical Performance Curves (Continued)**  $V_S = \pm 15V$ ,  $T_A = +25^\circ C$ , See test circuit for multiplier configuration

**WORST CASE MULTIPLICATION ERROR vs TEMPERATURE**



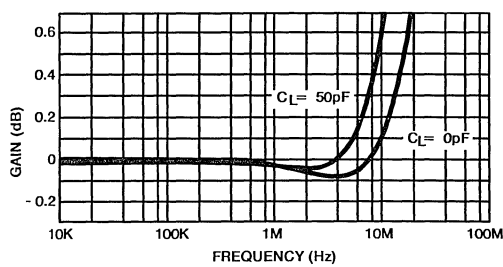
**MULTIPLICATION ERROR vs TEMPERATURE**

$V_Y = 5V$ ,  $V_X = 2V$

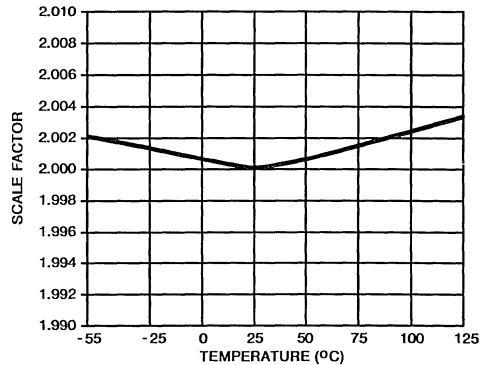


**GAIN VARIATION vs FREQUENCY**

$R_L = 1K$ ,  $V_X = 2V_{dc}$ ,  $V_Y = 200mV_{rms}$

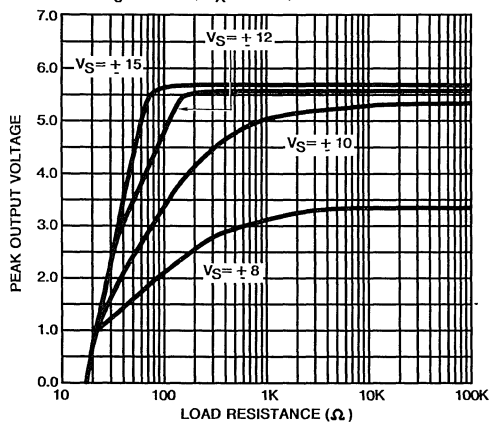


**SCALE FACTOR vs TEMPERATURE**

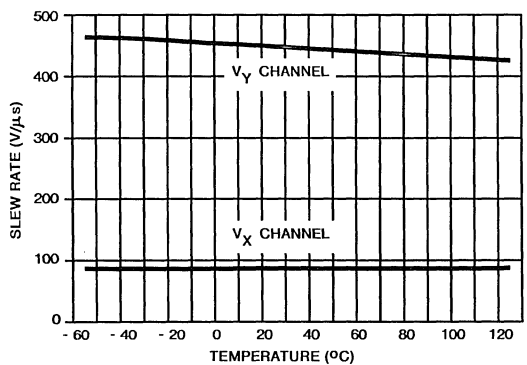


**OUTPUT VOLTAGE SWING vs LOAD RESISTANCE**

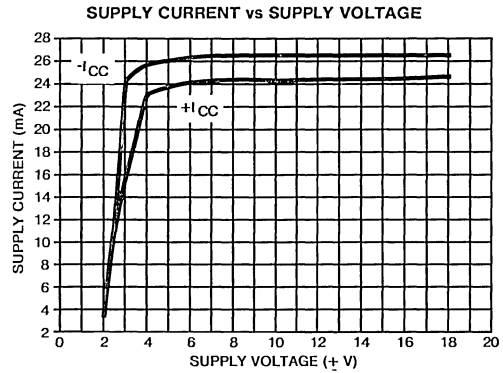
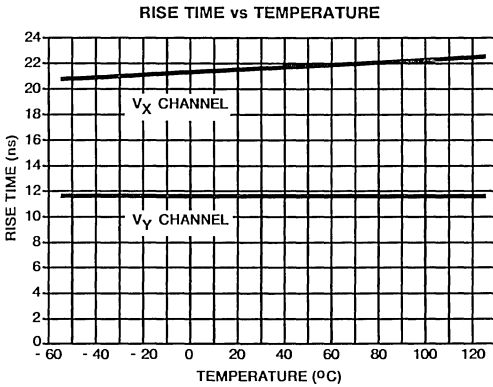
$f_o = 10kHz$ ,  $V_X = 2V_{dc}$ , THD < 0.1%



**SLEW RATE vs TEMPERATURE**



**Typical Performance Curves (Continued)**  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ , See test circuit for multiplier configuration



**Applications Information**

**Theory of Operation**

The HA-2546 is a two quadrant multiplier with one differential signal channel,  $V_{Y+}$  and  $V_{Y-}$ , one differential control channel,  $V_{X+}$  and  $V_{X-}$ , and one differential input,  $V_{Z+}$  and  $V_{Z-}$ , to complete the feedback of the output amplifier. Figure 1 shows a detailed functional block diagram of the HA-2546. The differential voltages of channels  $V_X$  and  $V_Y$  are converted to differential currents. These currents are then multiplied in a circuit similar to a Gilbert Cell multiplier, producing a differential current product. The differential voltage of  $V_Z$  is converted to a differential current which sums with the product currents. The differential "product/sum" currents are converted to a single-ended current then converted to a voltage output by a transimpedance amplifier.

The open loop transfer equation for the HA-2546 is:

$$V_{OUT} = A \left[ \frac{(V_{X+} - V_{X-})(V_{Y+} - V_{Y-}) - (V_{Z+} - V_{Z-})}{SF} \right], \text{ where}$$

A = Output Amplifier Open Loop Gain

SF = Scale Factor

$V_X, V_Y, V_Z$  = Differential Inputs

The scale factor is used to maintain the output of the multiplier within the normal operating range of  $\pm 5V$ . The scale factor can be defined by the user by way of an optional external resistor,  $R_{EXT}$ , and the Gain Adjust pins, Gain Adjust A (GA A), Gain Adjust B (GA B), and Gain Adjust C (GA C). The scale factor is determined as follows:

SF = 2, when GA B is shorted to GA C

SF  $\approx 1.2 * R_{EXT}$ , when  $R_{EXT}$  is connected between GA A and GA C ( $R_{EXT}$  is in  $k\Omega$ )

SF  $\approx 1.2 * (R_{EXT} + 1.667k\Omega)$ , when  $R_{EXT}$  is connected to GA B and GA C ( $R_{EXT}$  is in  $k\Omega$ )

The scale factor can be adjusted from 2 to 5. It should be noted that any adjustments to the scale factor will affect the AC performance of the control channel,  $V_X$ . The normal input operating range of  $V_X$  is equal to the scale factor voltage.

The typical multiplier configuration is shown in Figure 2. The ideal transfer function for this configuration is:

$$V_{OUT} = \begin{cases} \frac{(V_{X+} - V_{X-})(V_{Y+} - V_{Y-})}{2} + V_{Z-}, & \text{when } (V_{X+} - V_{X-}) \geq 0 \\ 0, & \text{when } (V_{X+} - V_{X-}) < 0 \end{cases}$$

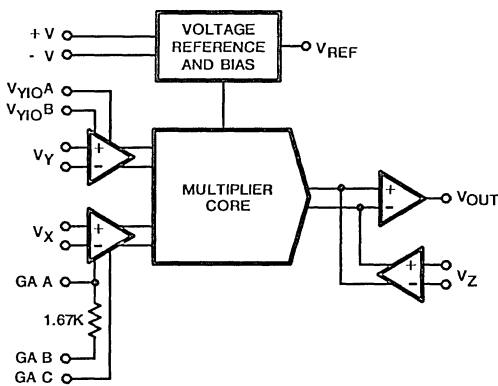


FIGURE 1.

8  
SPECIAL  
ANALOG CIRCUITS

**Applications Information (Continued)**

The  $V_{X-}$  pin is usually connected to ground so that when  $V_{X+}$  is negative there is no signal at the output, i.e. two quadrant operation. If the  $V_X$  input is a negative going signal the  $V_{X+}$  pin maybe grounded and the  $V_{X-}$  pin used as the input.

The  $V_{Y-}$  terminal is usually grounded allowing  $V_{Y+}$  to swing  $\pm 5$  volts. The  $V_{Z+}$  terminal is usually connected directly to  $V_{OUT}$  to complete the feedback loop of the output amplifier while  $V_{Z-}$  is grounded. The scale factor is normally set to 2 by connecting GA B to GA C. Therefore the transfer function becomes:

$$V_{OUT} = \frac{(V_{X+})(V_{Y-})}{2}$$

The multiplication error is trimmed to be minimum at full scale,  $V_X = 2V$  and  $V_Y = 5V$ . When  $V_Y = 5V$ , the worst case multiplication error occurs when  $V_X \approx 0.65V$ . See Typical Performance Curves.

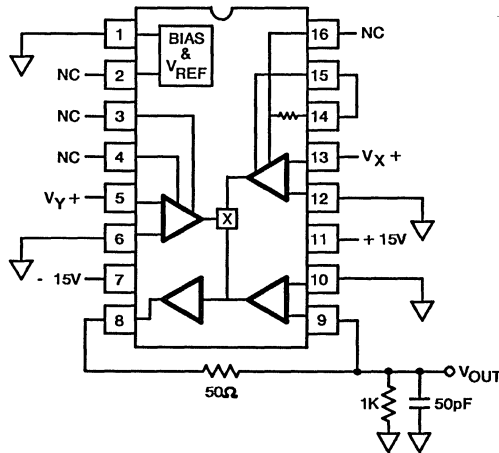


FIGURE 2.

**Operation At Reduced Supply Voltages**

The HA-2546 will operate over a range of supply voltages,  $\pm 8$  to  $\pm 15$  volts. Use of supply voltages below  $\pm 12$  volts will cause degradation of electrical parameters.

**Offset Adjustment**

The signal channel offset voltage may be nulled by using a 20K potentiometer between  $V_{YIO}$  Adjust pins A and B and connecting the wiper to  $-V_S$ . Reducing the signal channel offset voltage will reduce  $V_X$  AC feedthrough and improve the multiplication error. Output offset voltage can also be nulled by connecting  $V_{Z-}$  to the wiper of a potentiometer which is tied between  $+V$  and  $-V$ .

**Capacitive Drive Capability**

When driving capacitive loads  $>20pF$  a  $50\Omega$  resistor should be connected between  $V_{OUT}$  and  $V_{Z-}$ , using  $V_{Z-}$  as the output (see Figure 2). This will prevent the multiplier from going unstable due to the pole created by the load capacitor and reduce gain peaking at higher frequencies.

**Die Characteristics**

|                                     |   |
|-------------------------------------|---|
| Transistor Count .....              | 87  |
| Die Dimensions .....                | 79.9 x 119.7 x 19 mils<br>(2030 x 3040 x 480 $\mu$ m) |
| Substrate Potential* .....          | $V-$  |
| Process .....                       | High Frequency, Bipolar, DI                           |
| Passivation .....                   | Nitride   |
| Thermal Constants ( $^{\circ}C/W$ ) | $\theta_{ja}$ $\theta_{jc}$                           |
| HA1-2546 .....                      | 76      17  |

\* The substrate maybe left floating (Insulating Die Mount) or it may be on a conductor at  $V-$  potential.

August 1991

### Features

- Low Multiplication Error ..... 1.6%
- Input Bias Currents ..... 1.2 $\mu$ A
- Signal Input Feedthrough @ 5MHz ..... -50dB
- Wide Signal Bandwidth ..... 100MHz
- Wide Control Bandwidth ..... 22MHz

### Applications

- Military Avionics
- Missile Guidance Systems
- Medical Imaging Displays
- Video Mixers
- Sonar AGC Processors
- Radar Signal Conditioning
- Voltage Controlled Amplifier
- Vector Generator

### Description

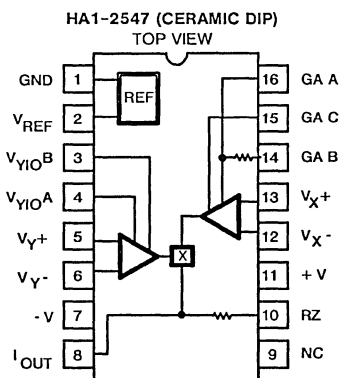
The HA-2547 is a monolithic, high speed, two quadrant, analog multiplier constructed in Harris' Dielectrically Isolated High Frequency Process. The high frequency performance of the HA-2547 rivals the best analog multipliers currently available including hybrids.

The single-ended current output of the HA-2547 has a 100MHz signal bandwidth ( $R_L = 50\Omega$ ) and a 22MHz control input bandwidth. High bandwidth and low distortion make this part an ideal component in video systems. The suitability for precision video applications is demonstrated further by low multiplication error (1.6%), low feedthrough (-50dB), and differential inputs with low bias currents (1.2 $\mu$ A). The HA-2547 is also well suited for mixer circuits as well as AGC applications for sonar, radar, and medical imaging equipment.

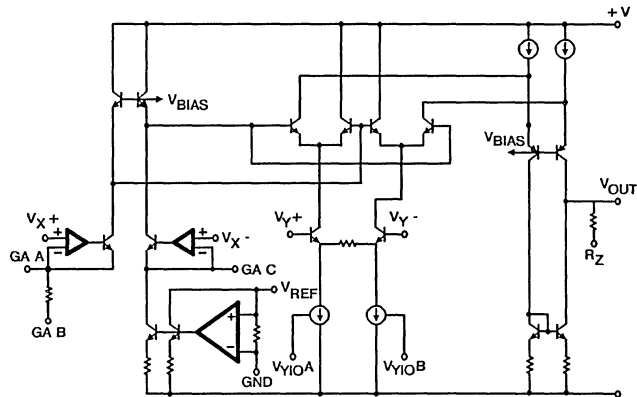
The current output of the HA-2547 allows it to achieve higher bandwidths than voltage output multipliers. An internal feedback resistor is provided to give an accurate current-to-voltage conversion and is trimmed to give a full scale output voltage of  $\pm 5$  volts. The HA-2547 is not limited to multiplication applications only; frequency doubling and power detection are also possible.

The HA-2547-9 has guaranteed operation from -40 $^{\circ}$ C to +85 $^{\circ}$ C, while the HA-2547-5 has guaranteed operation from 0 $^{\circ}$ C to +75 $^{\circ}$ C. The HA-2547 is available in a 16 pin Ceramic DIP. For MIL-STD-883 compliant product and LCC packages consult the HA-2547/883 datasheet.

### Pinout



### Schematic





## Specifications HA-2547

### Absolute Maximum Ratings (Note 1)

|   |        |
|---|--------|
| Voltage Between V+ and V- Terminals ..... | 35V    |
| Differential Input Voltage .....          | 6V     |
| Output Current .....                      | 3mA    |
| Maximum Junction Temperature .....        | +175°C |

### Operating Temperature Range

|                                 |  |
|---------------------------------|--|
| HA-2547-9 .....                 | $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  |
| HA-2547-5 .....                 | $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$    |
| Storage Temperature Range ..... | $-65^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ |

### Electrical Specifications +V = +15V, -V = -15V, R<sub>Z</sub> (Pin 10) Grounded, Unless Otherwise Specified

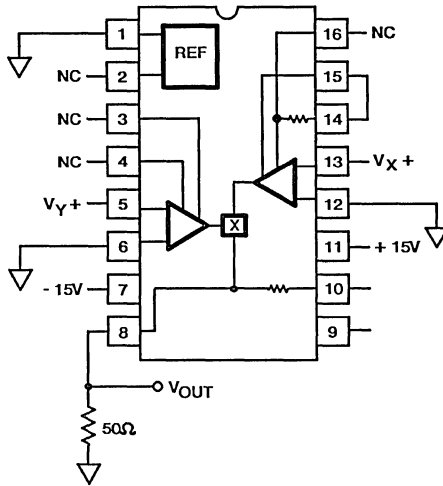
| PARAMETER                                   | TEMP  | HA-2547-9 |       |     | HA-2547-5 |       |     | UNITS |
|---|-------|-----------|-------|-----|-----------|-------|-----|-------|
|   |       | MIN       | TYP   | MAX | MIN       | TYP   | MAX |       |
| <b>MULTIPLIER PERFORMANCE</b>               |       |           |       |     |           |       |     |       |
| Multiplication Error (Note 2)               | +25°C | -         | 1.6   | 3   | -         | 1.6   | 3   | %FS   |
|   | Full  | -         | 3.0   | 7   | -         | 3.0   | 7   | %FS   |
| Multiplication Error Drift                  | Full  | -         | 0.003 | -   | -         | 0.003 | -   | %/°C  |
| Scale Factor Error                          | Full  | -         | 0.7   | 5   | -         | 0.7   | 5   | %     |
| THD+N (Note 3)                              | +25°C | -         | 0.03  | -   | -         | 0.03  | -   | %     |
| Output Offset Voltage (Note 4)              | +25°C | -         | 6     | 15  | -         | 6     | 15  | mV    |
|   | Full  | -         | 14    | 20  | -         | 14    | 20  | mV    |
| Average Offset Voltage Drift                | Full  | -         | -     | -   | -         | -     | -   | μV/°C |
| <b>SIGNAL INPUT, V<sub>Y</sub></b>          |       |           |       |     |           |       |     |       |
| Input Offset Voltage                        | +25°C | -         | 4     | 10  | -         | 4     | 10  | mV    |
|   | Full  | -         | 8     | 20  | -         | 8     | 20  | mV    |
| Average Offset Voltage Drift                | Full  | -         | 35    | -   | -         | 35    | -   | μV/°C |
| Input Bias Current                          | +25°C | -         | 7     | 15  | -         | 7     | 15  | μA    |
|   | Full  | -         | 10    | 15  | -         | 10    | 15  | μA    |
| Input Offset Current                        | +25°C | -         | 0.7   | 2   | -         | 0.7   | 2   | μA    |
|   | Full  | -         | 1.0   | 3   | -         | 1.0   | 3   | μA    |
| Input Differential Resistance               | +25°C | -         | 720   | -   | -         | 720   | -   | kΩ    |
| Small Signal Bandwidth (-3dB) (Notes 5, 10) | +25°C | -         | 100   | -   | -         | 100   | -   | MHz   |
| Feedthrough (Note 13)                       | +25°C | -         | -50   | -   | -         | -50   | -   | dB    |
| Differential Input Range                    | +25°C | ±5        | -     | -   | ±5        | -     | -   | Volts |
| Common Mode Range                           | +25°C | -         | ±9    | -   | -         | ±9    | -   | Volts |
| CMRR (Note 6)                               | Full  | 60        | 78    | -   | 60        | 78    | -   | dB    |
| <b>V<sub>Y</sub> TRANSIENT RESPONSE</b>     |       |           |       |     |           |       |     |       |
| Rise Time (Note 15)                         | +25°C | -         | 5     | -   | -         | 5     | -   | ns    |
| Propagation Delay                           | +25°C | -         | 3     | -   | -         | 3     | -   | ns    |
| <b>CONTROL INPUT, V<sub>X</sub></b>         |       |           |       |     |           |       |     |       |
| Input Offset Voltage                        | +25°C | -         | 1     | 2   | -         | 1     | 2   | mV    |
|   | Full  | -         | 2     | 20  | -         | 2     | 20  | mV    |
| Average Offset Voltage Drift                | Full  | -         | 12    | -   | -         | 12    | -   | μV/°C |
| Input Bias Current                          | +25°C | -         | 1.2   | 2   | -         | 1.2   | 2   | μA    |
|   | Full  | -         | 1.8   | 5   | -         | 1.8   | 5   | μA    |
| Input Offset Current                        | +25°C | -         | 0.3   | 2   | -         | 0.3   | 2   | μA    |
|   | Full  | -         | 0.4   | 3   | -         | 0.4   | 3   | μA    |
| Input Differential Resistance               | +25°C | -         | 360   | -   | -         | 360   | -   | kΩ    |
| Small Signal Bandwidth (-3dB) (Notes 5, 10) | +25°C | -         | 22    | -   | -         | 22    | -   | MHz   |
| Feedthrough (Note 14)                       | +25°C | -         | -40   | -   | -         | -40   | -   | dB    |
| Input Range (Note 12)                       | Full  | +2        | -     | -   | +2        | -     | -   | Volts |
| Common Mode Range                           | +25°C | -         | ±9    | -   | -         | ±9    | -   | Volts |
| CMMR (Note 7)                               | +25°C | -         | 75    | -   | -         | 75    | -   | dB    |
| <b>V<sub>X</sub> TRANSIENT RESPONSE</b>     |       |           |       |     |           |       |     |       |
| Rise Time (Note 16)                         | +25°C | -         | 15    | -   | -         | 15    | -   | ns    |
| Propagation Delay                           | +25°C | -         | 25    | -   | -         | 25    | -   | ns    |
| <b>OUTPUT CHARACTERISTICS</b>               |       |           |       |     |           |       |     |       |
| Full Scale Output Voltage (Note 8)          | Full  | -         | ±6.25 | -   | -         | ±6.25 | -   | Volts |
| Full Scale Output Current (Note 11)         | +25°C | -         | 2     | -   | -         | 2     | -   | mA    |
| Output Resistance                           | +25°C | -         | 4     | -   | -         | 4     | -   | MΩ    |
| <b>POWER SUPPLY</b>                         |       |           |       |     |           |       |     |       |
| PSRR (Note 9)                               | Full  | 58        | 63    | -   | 58        | 63    | -   | dB    |
| I <sub>CC</sub>                             | Full  | -         | 20    | 29  | -         | 20    | 29  | mA    |

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the servability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied
2. Error is percent of full scale, 1% = 50mV.
3.  $f_o = 10\text{kHz}$ ,  $V_Y = 1\text{Vrms}$ ,  $V_X = 2\text{V}$ .
4.  $V_X = 0\text{V}$ ,  $V_Y = 0\text{V}$ .
5.  $R_L = 50\Omega$ .
6.  $V_Y = 0$  to  $\pm 5\text{V}$ ,  $V_X = 2\text{V}$ .
7.  $V_X = 0$  to  $2\text{V}$ ,  $V_Y = 5\text{V}$ .
8.  $V_Y = \pm 5$ ,  $V_X = 2.5\text{V}$ .
9.  $V_S = \pm 12\text{V}$  to  $\pm 15\text{V}$ ,  $V_Y = 5\text{V}$ ,  $V_X = 2\text{V}$ .
10. Guaranteed by sample test and not 100% tested.
11. Output current tolerance is  $\pm 20\%$ .
12. Scale Factor = 2. See Applications Information.
13.  $f_o = 5\text{MHz}$ ,  $V_X = 0$ ,  $V_Y = 200\text{mVrms}$ . Relative to full scale output.
14.  $f_o = 5\text{MHz}$ ,  $V_Y = 0$ ,  $V_{X+} = 200\text{mVrms}$ ,  $V_{X-} = -0.5\text{V}$ . Relative to full scale output.
15.  $V_Y = \pm 5\text{V}$ ,  $V_X = 2\text{V}$ ,  $R_L = 50\Omega$ .
16.  $V_X = 0$  to  $2\text{V}$ ,  $V_Y = 5\text{V}$ ,  $R_L = 50\Omega$ .

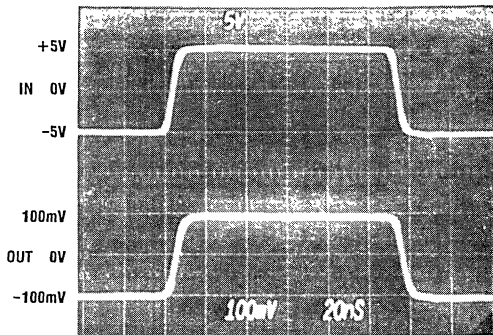
Test Circuits

AC AND TRANSIENT RESPONSE TEST CIRCUIT



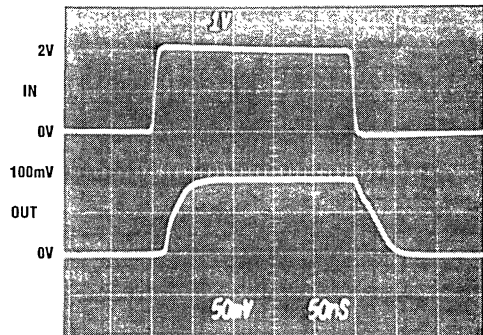
$V_Y$  TRANSIENT RESPONSE

Vertical Scale: Top: 5V/Div Bottom: 100mV/Div  
Horizontal Scale: 20ns/Div

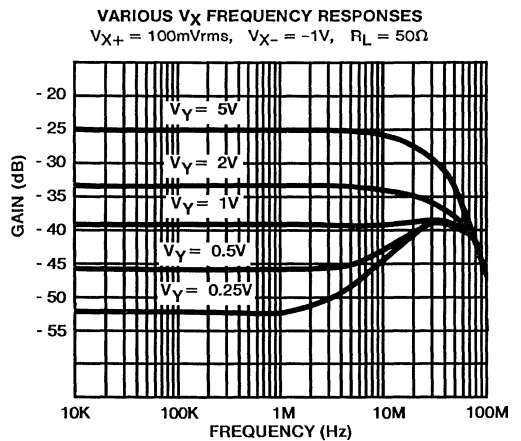
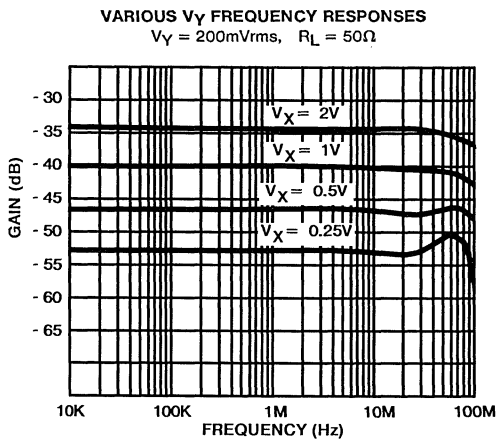
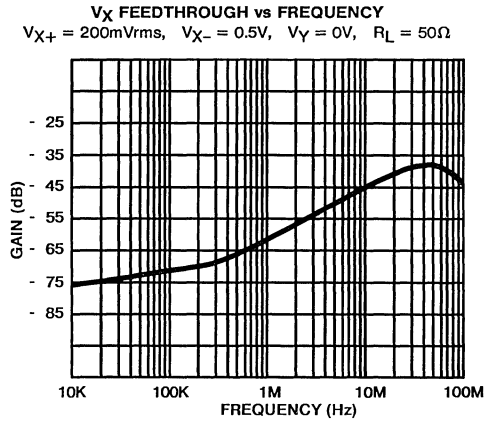
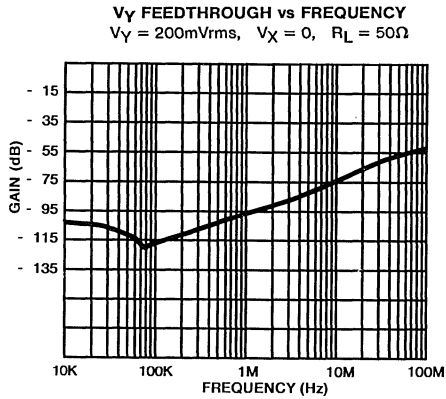
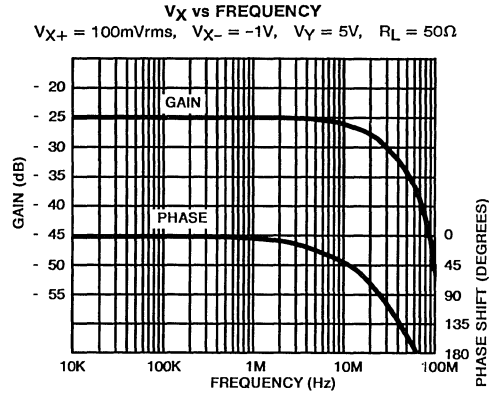
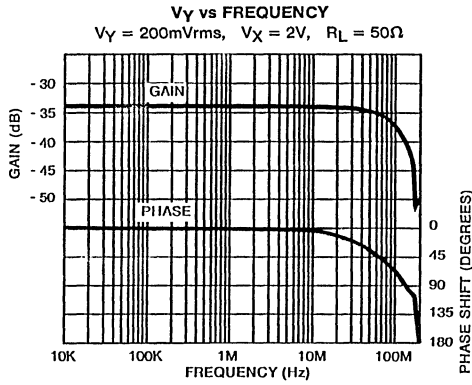


$V_X$  TRANSIENT RESPONSE

Vertical Scale: Top: 1V/Div Bottom: 50mV/Div  
Horizontal Scale: 50ns/Div

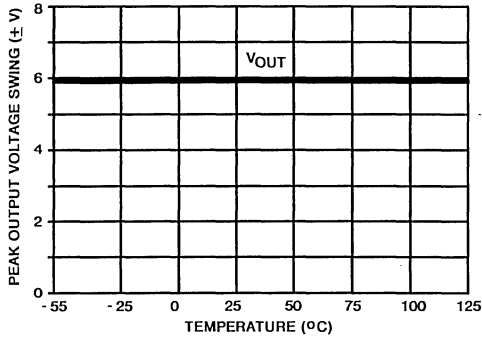


**Typical Performance Curves**  $V_S = \pm 15V, T_A = +25^\circ C$

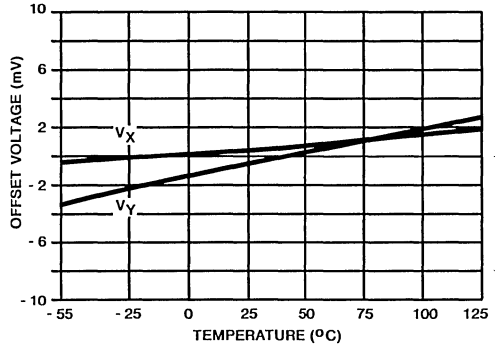


Typical Performance Curves (Continued)  $V_S = \pm 15V, T_A = +25^\circ C$

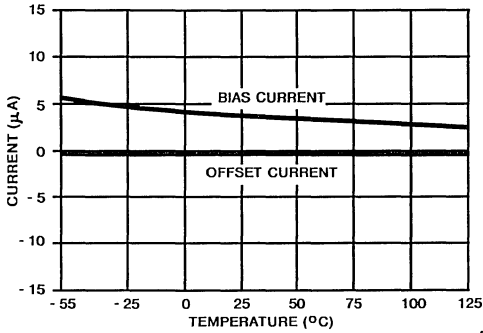
OUTPUT VOLTAGE SWING vs TEMPERATURE



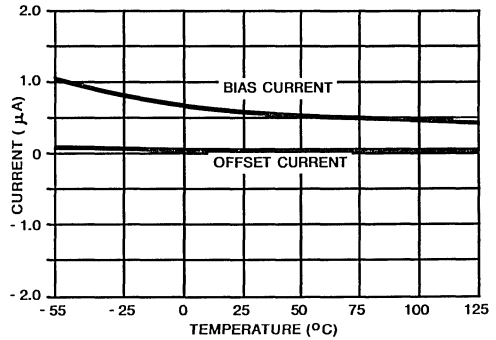
OFFSET VOLTAGE vs TEMPERATURE



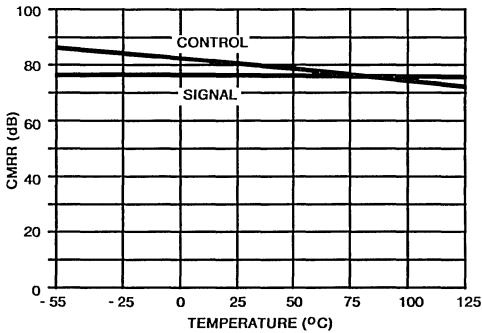
$V_Y$  OFFSET/BIAS CURRENT vs TEMPERATURE



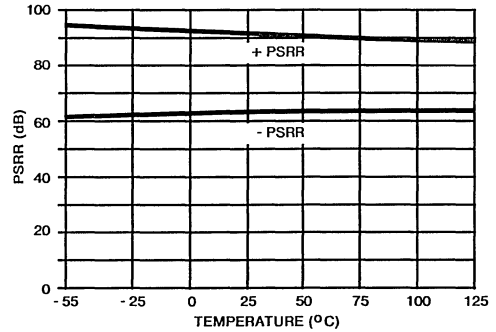
$V_X$  OFFSET/BIAS CURRENT vs TEMPERATURE



SIGNAL/CONTROL CMRR vs TEMPERATURE



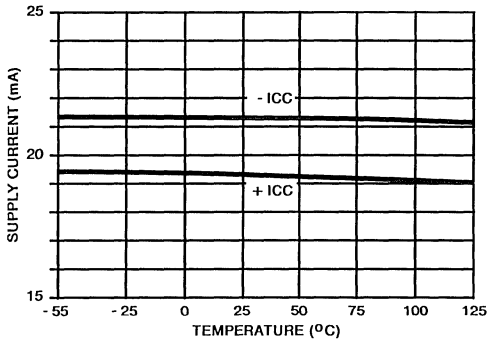
PSRR vs TEMPERATURE



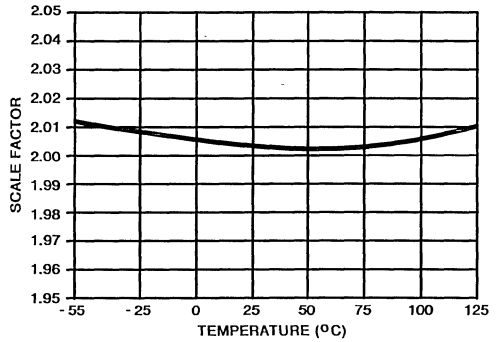
# HA-2547

Typical Performance Curves (Continued)  $V_S = \pm 15V$ ,  $T_A = +25^\circ C$

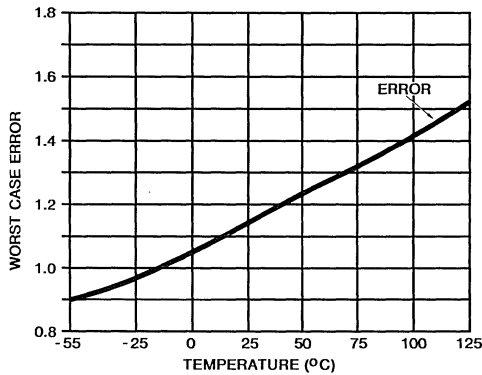
**$I_{CC}$  vs TEMPERATURE**



**SCALE FACTOR vs TEMPERATURE**

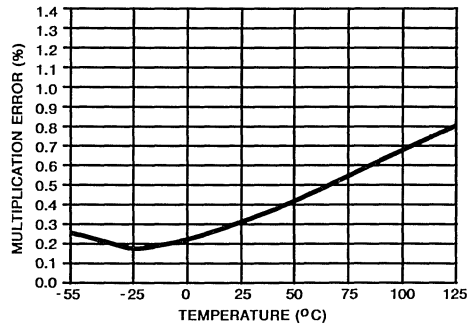


**WORST CASE MULTIPLICATION ERROR vs TEMPERATURE**



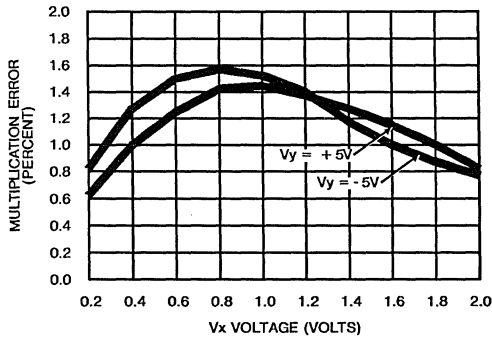
**MULTIPLICATION ERROR vs TEMPERATURE**

$V_X = 2V$ ,  $V_Y = 5V$



**MULTIPLICATION ERROR vs  $V_X$**

$V_Y = +5V$  and  $-5V$



## Die Characteristics

|                                    |   |
|------------------------------------|---|
| Transistor Count .....             | 75  |
| Die Dimensions .....               | 79.9 x 119.7 x 19 mils<br>(2030 x 3040 x 480 $\mu$ m) |
| Substrate Potential* .....         | $V^-$   |
| Process .....                      | High Frequency, Bipolar, DI                           |
| Passivation .....                  | Nitride   |
| Thermal Constants ( $^\circ C/W$ ) | $\theta_{ja}$ $\theta_{jc}$                           |
| HA1 -2547 .....                    | 76          17.3                                      |

\* The substrate may be left floating (Insulating Die Mount) or it may be on a conductor at  $V^-$  potential.

**Applications Information**

**Theory of Operation**

The HA-2547 is a current output, two quadrant multiplier with one differential signal channel,  $V_{Y+}$  and  $V_{Y-}$ , and one differential control channel,  $V_{X+}$  and  $V_{X-}$ . Figure 1 shows a detailed functional block diagram of the HA-2547. The differential voltages of channels  $V_X$  and  $V_Y$  are converted to differential currents. These differential currents are then multiplied in a circuit similar to a Gilbert Cell multiplier, producing a differential current product. The differential product currents are then converted to a single-ended output current which is typically 2mA,  $\pm 20\%$  at full scale ( $V_X = 2V$ ,  $V_Y = \pm 5V$ ). A trimmed internal scaling resistor,  $R_Z$ , is designed to convert the output current to an accurate voltage by grounding  $R_Z$  (pin 10).  $R_Z$  is trimmed such that at full scale output current the voltage drop across  $R_Z$  will be  $\pm 5.0$  volts.

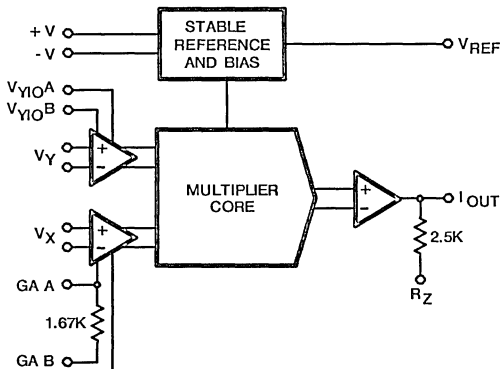


FIGURE 1.

The transfer equation for the HA-2547 is:

$$I_{OUT} = \frac{V_{OUT}}{R_Z} = \frac{(V_{X+} - V_{X-})(V_{Y+} - V_{Y-})}{SF \cdot R_Z}, \text{ where}$$

SF = Scale Factor

$R_Z = 2.5k\Omega$  (Internal)

$V_X, V_Y$  = Differential Inputs

The scale factor is used to maintain the output of the multiplier within the normal operating range of  $\pm 5V$ . The scale factor can be defined by the user by way of an optional external resistor,  $R_{EXT}$ , and the Gain Adjust pins: Gain Adjust A (GA A), Gain Adjust B (GA B), and Gain Adjust C (GA C). The scale factor is determined as follows:

SF = 2, when GA B is shorted to GA C

$SF \approx (1.2)(R_{EXT})$ , when  $R_{EXT}$  is connected between GA A and GA C ( $R_{EXT}$  is in  $k\Omega$ )

$SF \approx (1.2)(R_{EXT} + 1.667k\Omega)$ , when  $R_{EXT}$  is connected to GA B and GA C ( $R_{EXT}$  is in  $k\Omega$ ).

The scale factor can be adjusted from 2 to 5. It should be noted that any adjustments to the scale factor will affect the AC performance of the control channel,  $V_X$ . The normal input operating range of  $V_X$  is equal to the scale factor value.

A typical multiplier configuration is shown in Figure 2. The ideal transfer function for this configuration is shown below, illustrating two quadrant operation:

$$V_{OUT} = \frac{(V_{X+} - V_{X-})(V_{Y+} - V_{Y-})}{2}, \text{ when } (V_{X+} - V_{X-}) \geq 0$$

$$0, \text{ when } (V_{X+} - V_{X-}) < 0$$

The  $V_{X-}$  pin is usually connected to ground so that when  $V_{X+}$  is negative there is no signal at the output, i.e. two quadrant operation. If the  $V_X$  input is a negative going signal the  $V_{X+}$  pin maybe grounded and the  $V_{X-}$  pin used as the input. The  $V_{Y-}$  terminal is usually grounded allowing  $V_{Y+}$  to swing  $\pm 5$  volts.  $R_Z$  is normally used as a feedback resistor for an external op amp to provide an accurate current-to-voltage conversion. The scale factor is normally set to 2 by connecting GA B to GA C. Therefore, the transfer function becomes:

$$V_{OUT} = \frac{(V_{X+})(V_{Y+})}{2}$$

The multiplication error is trimmed to be minimum at full scale,  $V_X = 2V$  and  $V_Y = \pm 5V$ . When  $V_Y = \pm 5V$ , the worst case multiplication error occurs when  $V_X \approx 0.8V$  (Refer to typical performance curves).

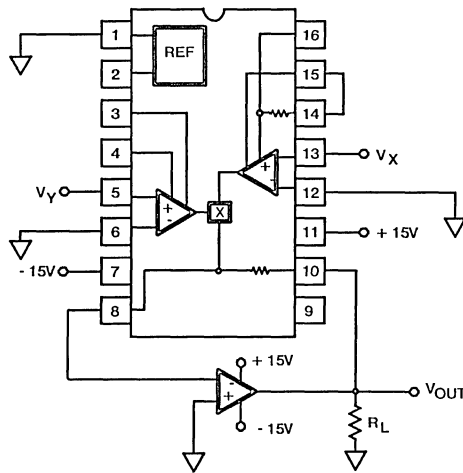


FIGURE 2.

**Operation At Various Supply Voltages**

The HA-2547 will operate over a range of supply voltages,  $\pm 8$  to  $\pm 15$  volts. Use of supply voltages below  $\pm 12$  volts will cause degradation of electrical parameters.

**Offset Adjustment**

The signal channel offset voltage may be nulled by using a 20K potentiometer between  $V_{YIO}$  Adjust pins A and B and connecting the wiper to  $-V_S$ . Reducing the signal channel offset voltage will reduce  $V_X$  AC feedthrough and improve the multiplication error. Output offset voltage can also be nulled by connecting  $V_{Z-}$  to the wiper of a potentiometer which is tied between  $+V$  and  $-V$ .

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SPECIAL  
ANALOG CIRCUITS

**PRELIMINARY**

August 1991

## Wideband Four Quadrant Voltage Output Analog Multiplier

### Features

- High Speed Voltage Output ..... 350V/ $\mu$ s
- Low Multiplication Error ..... 1.5%
- Input Bias Currents ..... 5 $\mu$ A
- Y Input Feedthrough ..... -60dB
- Wide X and Y Channel Bandwidth ..... 30MHz
- Gain Flatness to 10 MHz ..... 0.10dB

### Applications

- Military Avionics
- Missile Guidance Systems
- Medical Imaging Displays
- Video Mixers
- Sonar AGC Processors
- Radar Signal Conditioning
- Voltage Controlled Amplifier
- Vector Generator

### Description

The HA-2556 is a monolithic, high speed, four quadrant, analog multiplier constructed in the Harris Dielectrically Isolated High Frequency Process. The high frequency performance of the HA-2556 rivals the best analog multipliers currently available including hybrids.

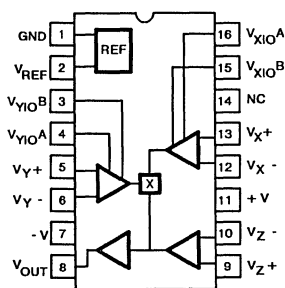
The HA-2556 has a voltage output X and Y channel bandwidth of 30MHz, and a 350V/ $\mu$ s slew rate. High bandwidth and slew rate make this part an ideal component for use in video systems. The suitability for precision video applications is demonstrated further by the 0.1dB gain flatness to 10MHz, 1.5% multiplication error, -60dB feedthrough and differential inputs with 5 $\mu$ A bias currents. The HA-2556 also has low differential gain (0.1%) and phase (0.1 $^\circ$ ) errors.

The HA-2556 is well suited for AGC circuits as well as mixer applications for sonar, radar, and medical imaging equipment. The voltage output of the HA-2556 simplifies many designs by eliminating the current-to-voltage conversion stage required for current output multipliers.

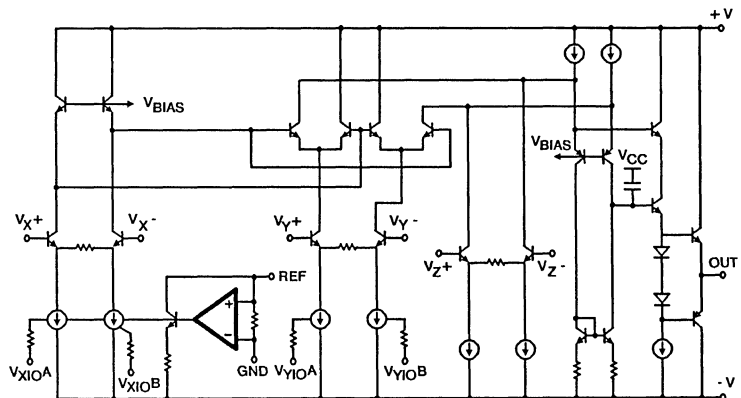
The HA-2556-9 has guaranteed operation from -40 $^\circ$ C to +85 $^\circ$ C. The HA-2556-5 has guaranteed operation from 0 $^\circ$ C to +70 $^\circ$ C. The HA-2556 is available in a 16 pin Ceramic DIP. For MIL-STD-883 compliant product and LCC packages consult the HA-2556/883 datasheet.

### Pinout

HA1-2556 (CERAMIC DIP)  
TOP VIEW



### Simplified Schematic



## Specifications HA-2556

### Absolute Maximum Ratings (Note 1)

|   |        |
|---|--------|
| Voltage Between V+ and V- Terminals ..... | 35V    |
| Differential Input Voltage .....          | 6V     |
| Output Current .....                      | ±60mA  |
| Maximum Junction Temperature .....        | +175°C |

### Operating Temperature Range

|                                 |                                 |
|---------------------------------|---------------------------------|
| HA-2556-9 .....                 | -40°C ≤ T <sub>A</sub> ≤ +85°C  |
| HA-2556-5 .....                 | 0°C ≤ T <sub>A</sub> ≤ +70°C    |
| Storage Temperature Range ..... | -65°C ≤ T <sub>A</sub> ≤ +150°C |

### Electrical Specifications V+ = 15V, V- = -15V, R<sub>L</sub> = 1K, C<sub>L</sub> = 50pF, Unless Otherwise Specified

| PARAMETER  | TEMP  | HA-2556-9 |       |     | HA-2556-5 |       |     | UNITS  |
|--|-------|-----------|-------|-----|-----------|-------|-----|--------|
|  |       | MIN       | TYP   | MAX | MIN       | TYP   | MAX |        |
| <b>MULTIPLIER PERFORMANCE</b>                                    |       |           |       |     |           |       |     |        |
| Multiplication Error (Note 2)                                    | +25°C | -         | 1.5   | 3   | -         | 1.5   | 3   | %      |
|  | Full  | -         | 3.0   | 6   | -         | 3.0   | 6   | %      |
| Multiplication Error Drift                                       | Full  | -         | 0.003 | -   | -         | 0.003 | -   | %/°C   |
| Differential Gain (Note 3,10)                                    | +25°C | -         | 0.1   | 0.2 | -         | 0.1   | 0.2 | %      |
| Differential Phase (Note 3,10)                                   | +25°C | -         | 0.1   | 0.3 | -         | 0.1   | 0.3 | Deg.   |
| Gain Flatness (Note 6,10)  |       |           |       |     |           |       |     |        |
| DC to 10 MHz   | +25°C | -         | 0.1   | 0.2 | -         | 0.1   | 0.2 | dB     |
| Scale Factor   | +25°C | -         | 5     | -   | -         | 5     | -   | V      |
| 1% Vector Bandwidth Error  | +25°C | -         | 260   | -   | -         | 260   | -   | kHz    |
| THD + N (Note 4)   | +25°C | -         | 0.03  | -   | -         | 0.03  | -   | %      |
| Voltage Noise (Note 12)  |       |           |       |     |           |       |     |        |
| f <sub>0</sub> =10Hz   | +25°C | -         | 400   | -   | -         | 400   | -   | nV/√Hz |
| f <sub>0</sub> =100Hz  | +25°C | -         | 150   | -   | -         | 150   | -   | nV/√Hz |
| f <sub>0</sub> =1kHz   | +25°C | -         | 75    | -   | -         | 75    | -   | nV/√Hz |
| <b>SIGNAL INPUT, V<sub>X</sub>, V<sub>Y</sub>, V<sub>Z</sub></b> |       |           |       |     |           |       |     |        |
| Input Offset Voltage   | +25°C | -         | 3     | 10  | -         | 3     | 10  | mV     |
|  | Full  | -         | 8     | 20  | -         | 8     | 20  | mV     |
| Average Offset Voltage Drift                                     | Full  | -         | 45    | -   | -         | 45    | -   | μV/°C  |
| Input Bias Current   | +25°C | -         | 5     | 10  | -         | 5     | 10  | μA     |
|  | Full  | -         | 10    | 15  | -         | 10    | 15  | μA     |
| Input Offset Current   | +25°C | -         | 0.5   | 1   | -         | 0.5   | 1   | μA     |
|  | Full  | -         | 1.0   | 1.5 | -         | 1.0   | 1.5 | μA     |
| Differential Input Resistance                                    | +25°C | -         | 720   | -   | -         | 720   | -   | kΩ     |
| Small Signal Bandwidth (-3dB)                                    | +25°C | -         | 30    | -   | -         | 30    | -   | MHz    |
| Full Power Bandwidth (Note 5)                                    | +25°C | -         | 9.5   | -   | -         | 9.5   | -   | MHz    |
| Y Input Feedthrough (Note 11)                                    | +25°C | -         | -60   | -   | -         | -60   | -   | dB     |
| Differential Input Range   | +25°C | ±5        | -     | -   | ±5        | -     | -   | V      |
| Common Mode Range  | +25°C | -         | ±9    | -   | -         | ±9    | -   | Volts  |
| CMRR (Note 6)  | Full  | 60        | 78    | -   | 60        | 78    | -   | dB     |
| <b>V<sub>X</sub>, V<sub>Y</sub> TRANSIENT RESPONSE</b>           |       |           |       |     |           |       |     |        |
| Slew Rate (Note 7)   | +25°C | -         | 350   | -   | -         | 350   | -   | V/μs   |
| Rise Time (Note 8)   | +25°C | -         | 11    | -   | -         | 11    | -   | ns     |
| Overshoot (Note 8)   | +25°C | -         | 17    | -   | -         | 17    | -   | %      |
| Propagation Delay  | +25°C | -         | 25    | -   | -         | 25    | -   | ns     |
| Settling Time (Note 7) 0.1%                                      | +25°C | -         | 200   | -   | -         | 200   | -   | ns     |



## Specifications HA-2556

**Electrical Specifications (Continued)**  $V_+ = 15V$ ,  $V_- = -15V$ ,  $R_L = 1K$ ,  $C_L = 50pF$ , Unless Otherwise Specified

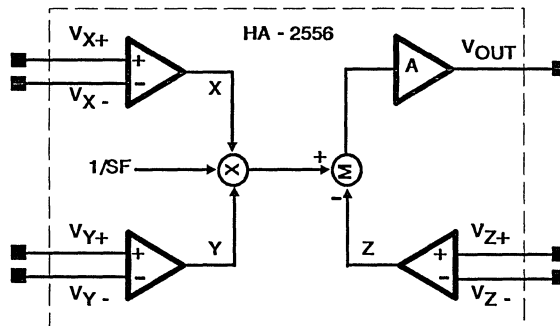
| PARAMETER                               | TEMP  | HA-2556-9 |       |     | HA-2556-5 |       |     | UNITS |
|---|-------|-----------|-------|-----|-----------|-------|-----|-------|
|   |       | MIN       | TYP   | MAX | MIN       | TYP   | MAX |       |
| <b>V<sub>Z</sub> TRANSIENT RESPONSE</b> |       |           |       |     |           |       |     |       |
| Slew Rate (Note 7)                      | +25°C | -         | 350   | -   | -         | 350   | -   | V/μs  |
| Rise Time (Note 8)                      | +25°C | -         | 11    | -   | -         | 11    | -   | ns    |
| Overshoot (Note 8)                      | +25°C | -         | 17    | -   | -         | 17    | -   | %     |
| Propagation Delay                       | +25°C | -         | 25    | -   | -         | 25    | -   | ns    |
| Settling Time (Note 7) 0.1%             | +25°C | -         | 200   | -   | -         | 200   | -   | ns    |
| <b>OUTPUT CHARACTERISTICS</b>           |       |           |       |     |           |       |     |       |
| Output Voltage Swing (Note 13)          | Full  | -         | ±6.05 | -   | -         | ±6.05 | -   | Volts |
| Output Current                          | Full  | ±20       | ±45   | -   | ±20       | ±45   | -   | mA    |
| Output Resistance                       | +25°C | -         | 1     | -   | 1         | -     | -   | Ω     |
| <b>POWER SUPPLY</b>                     |       |           |       |     |           |       |     |       |
| PSRR (Note 9)                           | Full  | -         | 63    | -   | -         | 63    | -   | dB    |
| Supply Current                          | Full  | -         | 18    | 20  | -         | 18    | 20  | mA    |

**NOTES:**

1. Absolute maximum ratings are limiting values, applied individually, beyond which the servability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Error is percent of full scale, 1% = 50mV.
3.  $f_o = 4.43MHz$ ,  $V_Y = 300mVp-p$ , 0 to 1Vdc offset,  $V_X = 5V$ .
4.  $f_o = 10kHz$ ,  $V_Y = 1Vrms$ ,  $V_X = 5V$ .
5. Full Power Bandwidth calculated by equation:  

$$FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}}, V_{peak} = 5V.$$
6.  $V_{IN} = 0$  to  $\pm 10$ .
7.  $V_{OUT} = 0$  to  $\pm 5V$ .
8.  $V_{OUT} = 0$  to  $\pm 100mV$ .
9.  $V_S = \pm 12V$  to  $\pm 15V$ .
10. Guaranteed by characterization and not 100% tested.
11.  $f_o = 5MHz$ .
12.  $V_X = V_Y = 0$ .
13.  $V_X = 5.5V$ ,  $V_Y = \pm 5.5$ .

### Functional Block Diagram



The transfer equation for the HA-2556 is:  
 $(V_{X+} - V_{X-})(V_{Y+} - V_{Y-}) = SF(V_{Z+} - V_{Z-})$ ,  
 where SF = Scale Factor = 5V  
 $V_X, V_Y, V_Z$  = Differential Inputs.

**PRELIMINARY**

August 1991

## Wideband Four Quadrant Current Output Analog Multiplier

### Features

- Low Multiplication Error ..... 1.5%
- Input Bias Currents ..... 5 $\mu$ A
- Y Input Feedthrough @ 5MHz ..... -60dB
- Wide X and Y Channel Bandwidth ..... 100MHz

### Applications

- Military Avionics
- Missile Guidance Systems
- Medical Imaging Displays
- Video Mixers
- Sonar AGC Processors
- Radar Signal Conditioning
- Voltage Controlled Amplifier
- Vector Generator

### Description

The HA-2557 is a monolithic, high speed, four quadrant, analog multiplier constructed in Harris' Dielectrically Isolated High Frequency Process. The high frequency performance of the HA-2557 rivals the best analog multipliers currently available including hybrids.

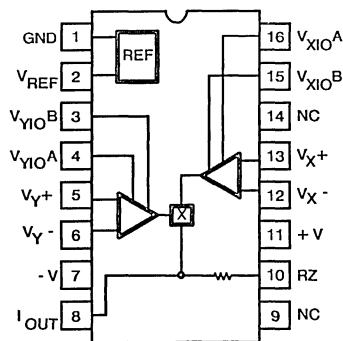
The single-ended current output of the HA-2557 has a 100MHz signal bandwidth ( $R_L = 50\Omega$ ). High bandwidth and low distortion make this part an ideal component in video systems. The suitability for precision video applications is demonstrated further by low multiplication error (1.5%), low feedthrough (-60dB), and differential inputs with low bias currents (5 $\mu$ A). The HA-2557 is also well suited for mixer circuits as well as AGC applications for sonar, radar, and medical imaging equipment.

The current output of the HA-2557 allows it to achieve higher bandwidths than voltage output multipliers. Full scale output current is trimmed to 1.6mA. An internal 2500 $\Omega$  feedback resistor is also provided to accurately convert the current, if desired, to a full scale output voltage of  $\pm 4V$ . The HA-2557 is not limited to multiplication applications only; frequency doubling and power detection are also possible.

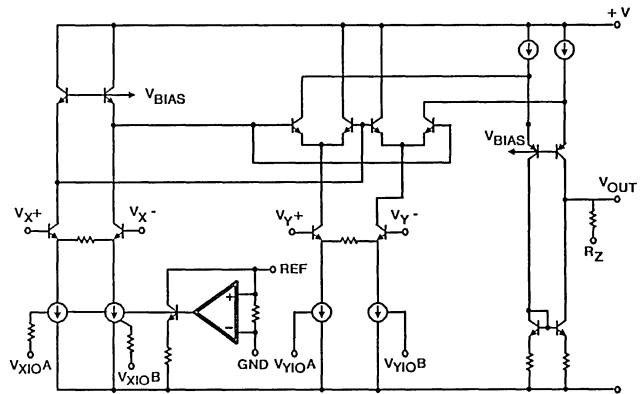
The HA-2557-9 has guaranteed operation from -40 $^{\circ}C$  to +85 $^{\circ}C$ , while the HA-2557-5 has guaranteed operation from 0 $^{\circ}C$  to +70 $^{\circ}C$ . The HA-2557 is available in a 16 pin Ceramic DIP. For MIL-STD-883 compliant product and LCC packages consult the HA-2557/883 datasheet.

### Pinout

HA1-2557 (CERAMIC DIP)  
TOP VIEW



### Schematic



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SPECIAL  
ANALOG CIRCUITS

## Specifications HA-2557

### Absolute Maximum Ratings (Note 1)

|   |        |
|---|--------|
| Voltage Between V+ and V- Terminals ..... | 35V    |
| Differential Input Voltage .....          | 6V     |
| Output Current .....                      | 3mA    |
| Maximum Junction Temperature .....        | +175°C |

### Operating Temperature Range

|                                 |  |
|---------------------------------|--|
| HA-2557-9 .....                 | $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$  |
| HA-2557-5 .....                 | $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$    |
| Storage Temperature Range ..... | $-65^{\circ}\text{C} \leq T_A \leq +150^{\circ}\text{C}$ |

### Electrical Specifications +V = +15V, -V = -15V, Unless Otherwise Specified

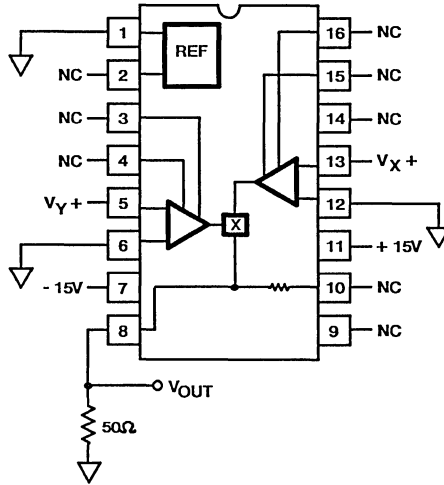
| PARAMETER   | TEMP  | HA-2557-9 |       |     | HA-2557-5 |       |     | UNITS |
|---|-------|-----------|-------|-----|-----------|-------|-----|-------|
|   |       | MIN       | TYP   | MAX | MIN       | TYP   | MAX |       |
| <b>MULTIPLIER PERFORMANCE</b>                                   |       |           |       |     |           |       |     |       |
| Multiplication Error (Note 2)                                   | +25°C | -         | 1.5   | 3   | -         | 1.5   | 3   | %FS   |
|   | Full  | -         | 3.0   | 6   | -         | 3.0   | 6   | %FS   |
| Multiplication Error Drift                                      | Full  | -         | 0.003 | -   | -         | 0.003 | -   | %/°C  |
| Scale Factor  | +25°C | -         | 10    | -   | -         | 10    | -   | kV-Ω  |
| THD+N (Note 3)  | +25°C | -         | 0.03  | -   | -         | 0.03  | -   | %     |
| Output Offset Voltage (Note 4)                                  | +25°C | -         | 6     | 15  | -         | 6     | 15  | mV    |
|   | Full  | -         | 14    | 20  | -         | 14    | 20  | mV    |
| Average Offset Voltage Drift                                    | Full  | -         | -     | -   | -         | -     | -   | μV/°C |
| <b>V<sub>X</sub>, V<sub>Y</sub>, V<sub>Z</sub></b>              |       |           |       |     |           |       |     |       |
| Input Offset Voltage  | +25°C | -         | 4     | 10  | -         | 4     | 10  | mV    |
|   | Full  | -         | 8     | 20  | -         | 8     | 20  | mV    |
| Average Offset Voltage Drift                                    | Full  | -         | 35    | -   | -         | 35    | -   | μV/°C |
| Input Bias Current  | +25°C | -         | 5     | 10  | -         | 5     | 10  | μA    |
|   | Full  | -         | 10    | 15  | -         | 10    | 15  | μA    |
| Input Offset Current  | +25°C | -         | 0.5   | 1   | -         | 0.5   | 1   | μA    |
|   | Full  | -         | 1.0   | 1.5 | -         | 1.0   | 1.5 | μA    |
| Differential Input Resistance                                   | +25°C | -         | 720   | -   | -         | 720   | -   | kΩ    |
| Small Signal Bandwidth (-3dB) (Note 5)                          | +25°C | -         | 100   | -   | -         | 100   | -   | MHz   |
| Y Input Feedthrough (Note 8)                                    | +25°C | -         | -60   | -   | -         | -60   | -   | dB    |
| Differential Input Range  | +25°C | ±4        | -     | -   | ±4        | -     | -   | Volts |
| Common Mode Range   | +25°C | -         | ±9    | -   | -         | ±9    | -   | Volts |
| CMRR (Note 6)   | Full  | 60        | 78    | -   | 60        | 78    | -   | dB    |
| <b>V<sub>X</sub>, V<sub>Y</sub> TRANSIENT RESPONSE (Note 5)</b> |       |           |       |     |           |       |     |       |
| Rise Time   | +25°C | -         | 5     | -   | -         | 5     | -   | ns    |
| Propagation Delay   | +25°C | -         | 3     | -   | -         | 3     | -   | ns    |
| <b>OUTPUT CHARACTERISTICS</b>                                   |       |           |       |     |           |       |     |       |
| Full Scale Output Compliance Voltage                            | Full  | -         | 4     | -   | -         | 4     | -   | Volts |
| Full Scale Output Current                                       | +25°C | -         | 1.6   | -   | -         | 1.6   | -   | mA    |
| Internal Feedback Resistor (R <sub>Z</sub> )                    | +25°C | -         | 2500  | -   | -         | 2500  | -   | Ω     |
| Output Resistance   | +25°C | -         | 1.5   | -   | -         | 1.5   | -   | MΩ    |
| <b>POWER SUPPLY</b>   |       |           |       |     |           |       |     |       |
| PSRR (Note 7)   | Full  | -         | 63    | -   | -         | 63    | -   | dB    |
| I <sub>CC</sub>   | Full  | -         | 18    | 20  | -         | 18    | 20  | mA    |

#### NOTES:

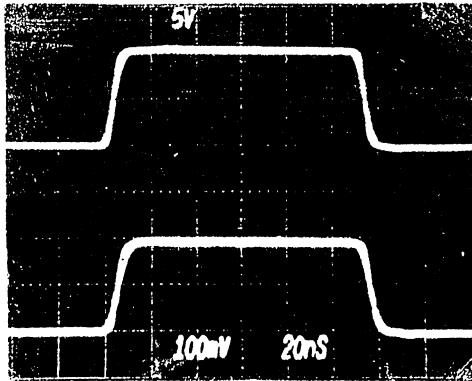
1. Absolute maximum ratings are limiting values, applied individually, beyond which the servability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Error is percent of full scale, 1% = 50mV.
3. f<sub>0</sub> = 10kHz, V<sub>Y</sub> = 1Vrms, V<sub>X</sub> = 4V.
4. V<sub>X</sub> = 0V, V<sub>Y</sub> = 0V.
5. R<sub>L</sub> = 50Ω.
6. V<sub>CM</sub> = 0 to ±9V.
7. V<sub>S</sub> = ±12V to ±15V.
8. f<sub>0</sub> = 5MHz. Relative to full scale output.

Test Circuits

AC AND TRANSIENT RESPONSE TEST CIRCUIT



**V<sub>y</sub> TRANSIENT RESPONSE**  
 Vertical Scale: Top 5V/Div Bottom: 100mV/Div  
 Horizontal Scale: 20ns/Div



# ICL8013

## Four Quadrant Analog Multiplier

### GENERAL DESCRIPTION

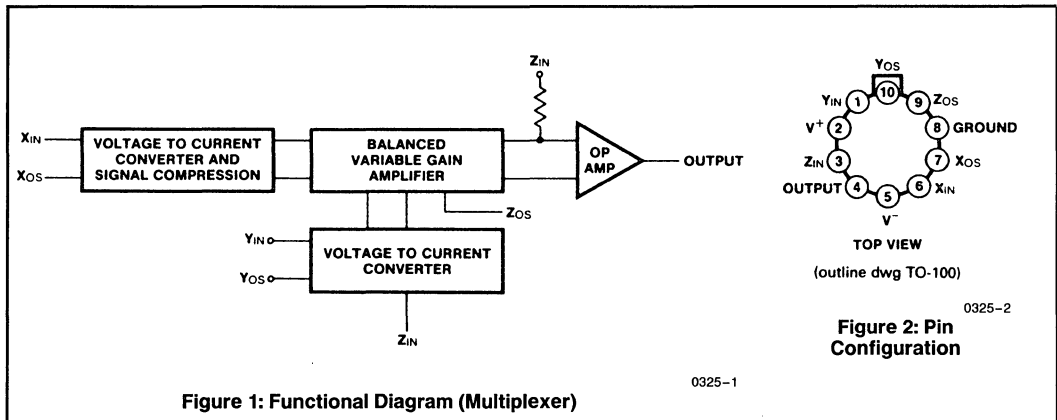
The ICL8013 is a four quadrant analog multiplier whose output is proportional to the algebraic product of two input signals. Feedback around an internal op-amp provides level shifting and can be used to generate division and square root functions. A simple arrangement of potentiometers may be used to trim gain accuracy, offset voltage and feed-through performance. The high accuracy, wide bandwidth, and increased versatility of the ICL8013 make it ideal for all multiplier applications in control and instrumentation systems. Applications include RMS measuring equipment, frequency doublers, balanced modulators and demodulators, function generators, and voltage controlled amplifiers.

### FEATURES

- Accuracy of  $\pm 0.5\%$  ("A" Version)
- Full  $\pm 10V$  Input Voltage Range
- 1MHz Bandwidth
- Uses Standard  $\pm 15V$  Supplies
- Built-in Op Amp Provides Level Shifting, Division and Square Root Functions

### ORDERING INFORMATION

| Part Number  | Multiplication Error | Temperature Range                 | Package           |
|--------------|----------------------|-----------------------------------|-------------------|
| ICL8013AM TX | $\pm 0.5\%$          | $-55^{\circ}C$ to $+125^{\circ}C$ | 10-LEAD<br>TO-100 |
| ICL8013BM TX | $\pm 1\%$            | $-55^{\circ}C$ to $+125^{\circ}C$ |                   |
| ICL8013CM TX | $\pm 2\%$            | $-55^{\circ}C$ to $+125^{\circ}C$ |                   |
| ICL8013AC TX | $\pm 5\%$            | $0^{\circ}C$ to $+70^{\circ}C$    |                   |
| ICL8013BC TX | $\pm 1\%$            | $0^{\circ}C$ to $+70^{\circ}C$    |                   |
| ICL8013CC TX | $\pm 2\%$            | $0^{\circ}C$ to $+70^{\circ}C$    |                   |



# ICL8013

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V  
 Power Dissipation (Note 1) ..... 500mW  
 Input Voltages  
 (X<sub>IN</sub>, Y<sub>IN</sub>, Z<sub>IN</sub>, X<sub>OS</sub>, Y<sub>OS</sub>, Z<sub>OS</sub>) ..... V<sub>SUPPLY</sub>

Operating Temperature Range:  
 ICL8013XC ..... 0°C to +70°C  
 ICL8013XM ..... -55°C to +125°C  
 Storage Temperature Range ..... -65°C to +150°C  
 Lead Temperature (Soldering, 10sec) ..... 300°C

**NOTE 1:** Derate at 6.8mW/°C for operation at ambient temperature above 75°C.

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS (Unless otherwise specified T<sub>A</sub> = 25°C, V<sub>SUPPLY</sub> = ±15V, Gain and Offset Potentiometers Externally Trimmed)

| Parameter   | Test Conditions                    | ICL8013A             |                 |          | ICL8013B |                 |            | ICL8013C |                 |            | Units                        |
|---|------------------------------------|----------------------|-----------------|----------|----------|-----------------|------------|----------|-----------------|------------|------------------------------|
|   |                                    | Min                  | Typ             | Max      | Min      | Typ             | Max        | Min      | Typ             | Max        |                              |
| Multiplier Function                                 |                                    |                      | $\frac{XY}{10}$ |          |          | $\frac{XY}{10}$ |            |          | $\frac{XY}{10}$ |            |                              |
| Multiplication Error                                | -10 < X < 10<br>-10 < Y < 10       |                      |                 | 0.5      |          |                 | 1.0        |          |                 | 2.0        | % Full Scale                 |
| Divider Function                                    |                                    |                      | $\frac{10Z}{X}$ |          |          | $\frac{10Z}{X}$ |            |          | $\frac{10Z}{X}$ |            |                              |
| Division Error                                      | X = -10<br>X = -1                  |                      | 0.3<br>1.5      |          |          | 0.3<br>1.5      |            |          | 0.3<br>1.5      |            | % Full Scale<br>% Full Scale |
| Feedthrough   | X = 0, Y = ±10V<br>Y = 0, X = ±10V |                      |                 | 50<br>50 |          |                 | 100<br>100 |          |                 | 200<br>150 | mV<br>mV                     |
| Non-Linearity                                       | X Input                            |                      | ±0.5            |          |          | ±0.5            |            |          | ±0.8            |            | %                            |
|   | Y Input                            |                      | ±0.2            |          |          | ±0.2            |            |          | ±0.3            |            | %                            |
| Frequency Response<br>Small Signal Bandwidth (-3dB) |                                    |                      | 1.0             |          |          | 1.0             |            |          | 1.0             |            | MHz                          |
| Full Power Bandwidth                                |                                    |                      | 750             |          |          | 750             |            |          | 750             |            | kHz                          |
| Slew Rate   |                                    |                      | 45              |          |          | 45              |            |          | 45              |            | V/μs                         |
| 1% Amplitude Error                                  |                                    |                      | 75              |          |          | 75              |            |          | 75              |            | kHz                          |
| 1% Vector Error<br>(0.5° Phase Shift)               |                                    |                      | 5               |          |          | 5               |            |          | 5               |            | kHz                          |
| Settling Time<br>(to ±2% of Final Value)            | V <sub>IN</sub> = ±10V             |                      | 1               |          |          | 1               |            |          | 1               |            | μs                           |
| Overload Recovery<br>(to ±2% of Final Value)        |                                    |                      | 1               |          |          | 1               |            |          | 1               |            | μs                           |
| Output Noise  | 5 Hz to 10 kHz<br>5 Hz to 5 MHz    |                      | 0.6<br>3        |          |          | 0.6<br>3        |            |          | 0.6<br>3        |            | mV rms<br>mV rms             |
| Input Resistance                                    | X Input                            | V <sub>IN</sub> = 0V | 10              |          |          | 10              |            |          | 10              |            | MΩ                           |
|   | Y Input                            |                      | 6               |          |          | 6               |            |          | 6               |            | MΩ                           |
|   | Z Input                            |                      | 36              |          |          | 36              |            |          | 36              |            | kΩ                           |
| Input Bias Current                                  | X or Y Input                       | V <sub>IN</sub> = 0V | 2               | 5        |          | 7.5             |            |          | 10              |            | μA                           |
|   | Z Input                            |                      | 25              |          |          | 25              |            |          | 25              |            | μA                           |
| Power Supply Variation                              | Multiplication Error               |                      | 0.2             |          |          | 0.2             |            |          | 0.2             |            | % / %                        |
|   | Output Offset                      |                      |                 | 50       |          |                 | 75         |          |                 | 100        | mV/V                         |
|   | Scale Factor                       |                      | 0.1             |          |          | 0.1             |            |          | 0.1             |            | % / %                        |
| Quiescent Current                                   |                                    |                      | 3.5             | 6.0      |          | 3.5             | 6.0        |          | 3.5             | 6.0        | mA                           |

NOTE: All typical values have been characterized but are not tested.

## ELECTRICAL CHARACTERISTICS

(Unless otherwise specified  $T_A = 25^\circ\text{C}$ ,  $V_{\text{SUPPLY}} = \pm 15\text{V}$ , Gain and Offset Potentiometers Externally Trimmed) (Continued)

| Parameter   | Test Conditions  | ICL8013A                    |          |     | ICL8013B |          |     | ICL8013C |          |     | Units         |
|---|--|-----------------------------|----------|-----|----------|----------|-----|----------|----------|-----|---------------|
|   |  | Min                         | Typ      | Max | Min      | Typ      | Max | Min      | Typ      | Max |               |
| <b>The Following Specifications Apply Over the Operating Temperature Ranges</b> |  |                             |          |     |          |          |     |          |          |     |               |
| Multiplication Error  | $-10\text{V} < X_{\text{IN}} < 10\text{V}$ ,<br>$-10\text{V} < Y_{\text{IN}} < 10\text{V}$ |                             | 1.5      |     |          | 2        |     |          | 3        |     | % Full Scale  |
| Average Temperature Coefficients  | Accuracy   |                             | 0.06     |     |          | 0.06     |     |          | 0.06     |     | %/°C          |
|   | Output Offset  |                             | 0.2      |     |          | 0.2      |     |          | 0.2      |     | mV/°C         |
|   | Scale Factor   |                             | 0.04     |     |          | 0.04     |     |          | 0.04     |     | %/°C          |
| Input Bias Current  | X or Y Input   | $V_{\text{IN}} = 0\text{V}$ |          | 5   |          | 5        |     |          | 10       |     | $\mu\text{A}$ |
|   | Z Input  |                             |          | 25  |          | 25       |     |          | 35       |     | $\mu\text{A}$ |
| Input Voltage (X, Y, or Z)  |  |                             | $\pm 10$ |     |          | $\pm 10$ |     |          | $\pm 10$ |     | V             |
| Output Voltage Swing  | $R_L \geq 2\text{k}\Omega$<br>$C_L < 1000\text{pF}$  |                             | $\pm 10$ |     |          | $\pm 10$ |     |          | $\pm 10$ |     | V             |

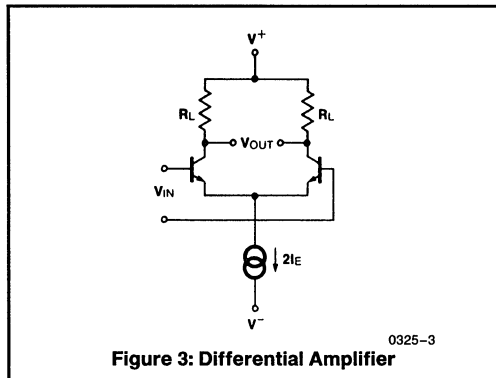


Figure 3: Differential Amplifier

## DETAILED DESCRIPTION

The fundamental element of the ICL8013 multiplier is the bipolar differential amplifier of Figure 3.

The small signal differential voltage gain of this circuit is given by

$$A_V = \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{R_L}{r_e}$$

Substituting  $r_e = \frac{1}{g_m} = \frac{kT}{qI_E}$

$$V_{\text{OUT}} = V_{\text{IN}} \frac{R_L}{r_e} = V_{\text{IN}} \cdot \frac{qI_E R_L}{kT}$$

The output voltage is thus proportional to the product of the input voltage  $V_{\text{IN}}$  and the emitter current  $I_E$ . In the simple transconductance multiplier of Figure 4, a current source comprising  $Q_3$ ,  $D_1$ , and  $R_Y$  is used. If  $V_Y$  is large compared with the drop across  $D_1$ , then

$$I_D \sim \frac{V_Y}{R_Y} = 2I_E \text{ and}$$

$$V_{\text{OUT}} = \frac{qR_L}{kTR_Y} (V_X \cdot V_Y)$$

There are several difficulties with this simple modulator:

- 1:  $V_Y$  must be positive and greater than  $V_D$ .
- 2: Some portion of the signal at  $V_X$  will appear at the output unless  $I_E = 0$ .
- 3:  $V_X$  must be a small signal for the differential pair to be linear.
- 4: The output voltage is not centered around ground.

The first problem relates to the method of converting the  $V_Y$  voltage to a current to vary the gain of the  $V_X$  differential pair. A better method, Figure 5, uses another differential pair but with considerable emitter degeneration. In this cir-

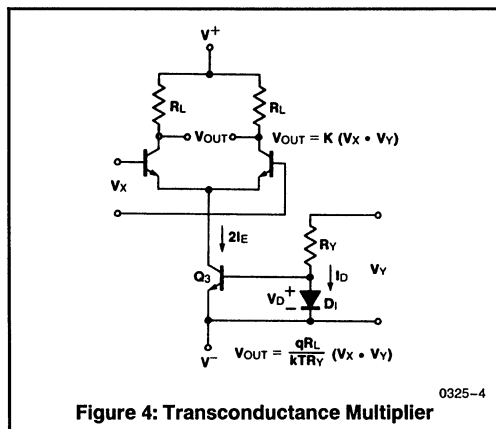
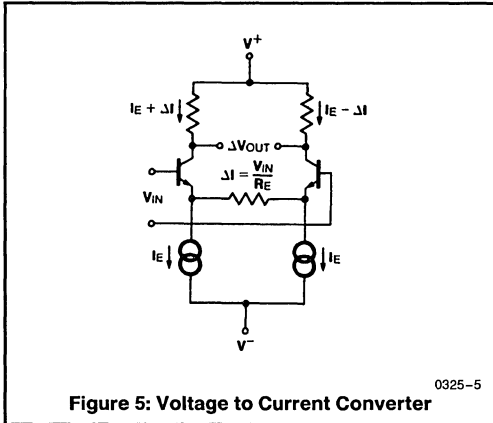


Figure 4: Transconductance Multiplier

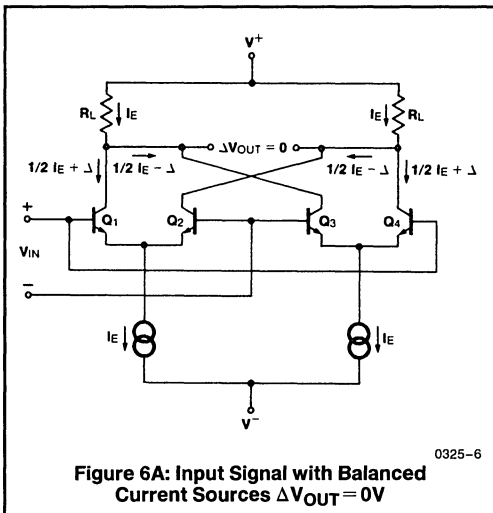
cuit the differential input voltage appears across the common emitter resistor, producing a current which adds or subtracts from the quiescent current in either collector. This type of voltage to current converter handles signals from 0 volts to  $\pm 10$  volts with excellent linearity.



**Figure 5: Voltage to Current Converter**

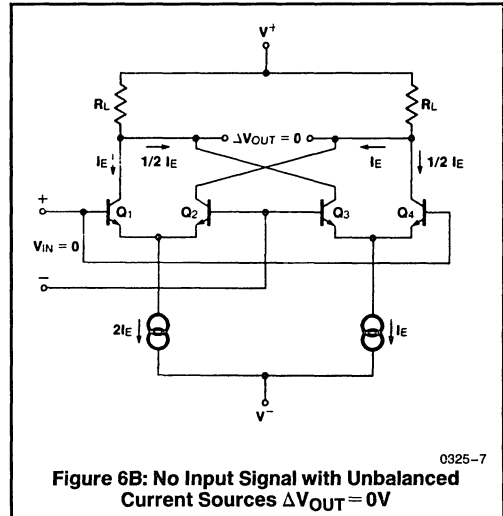
The second problem is called feedthrough; i.e. the product of zero and some finite input signal does not produce zero output voltage. The circuit whose operation is illustrated by Figures 6A, B, and C overcomes this problem and forms the heart of many multiplier circuits in use today.

This circuit is basically two matched differential pairs with cross coupled collectors. Consider the case shown in 6A of exactly equal current sources biasing the two pairs. With a small positive signal at  $V_{IN}$ , the collector current of  $Q_1$  and  $Q_4$  will increase but the collector currents of  $Q_2$  and  $Q_3$  will decrease by the same amount. Since the collectors are cross coupled the current through the load resistors remains unchanged and independent of the  $V_{IN}$  input voltage.

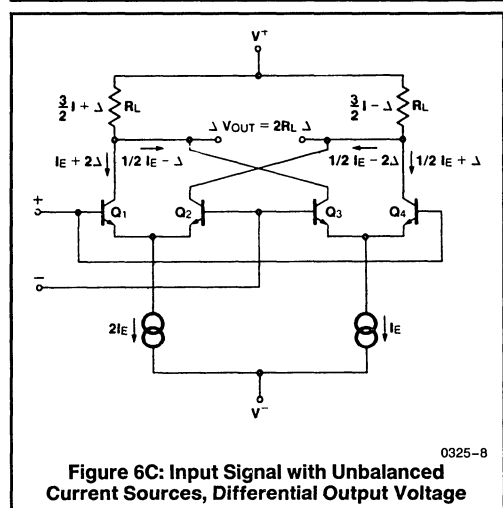


**Figure 6A: Input Signal with Balanced Current Sources  $\Delta V_{OUT} = 0V$**

In Figure 6B, notice that with  $V_{IN} = 0$  any variation in the ratio of biasing current sources will produce a common mode voltage across the load resistors. The differential output voltage will remain zero. In Figure 6C we apply a differential input voltage with unbalanced current sources. If  $I_{E1}$  is twice  $I_{E2}$ , the gain of differential pair  $Q_1$  and  $Q_2$  is twice the gain of pair  $Q_3$  and  $Q_4$ . Therefore, the change in cross coupled collector currents will be unequal and a differential output voltage will result. By replacing the separate biasing current sources with the voltage to current converter of Figure 5 we have a balanced multiplier circuit capable of four quadrant operation (Figure 7).



**Figure 6B: No Input Signal with Unbalanced Current Sources  $\Delta V_{OUT} = 0V$**

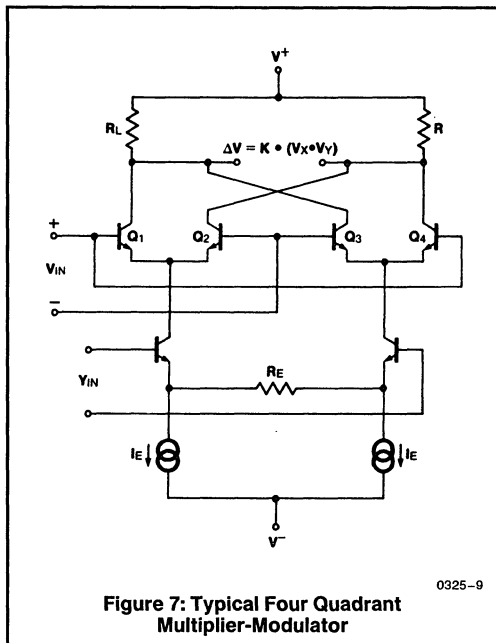


**Figure 6C: Input Signal with Unbalanced Current Sources, Differential Output Voltage**

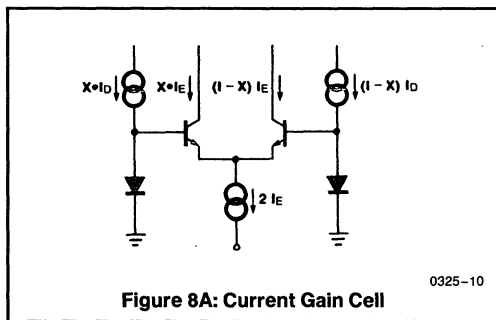
NOTE: All typical values have been characterized but are not tested.



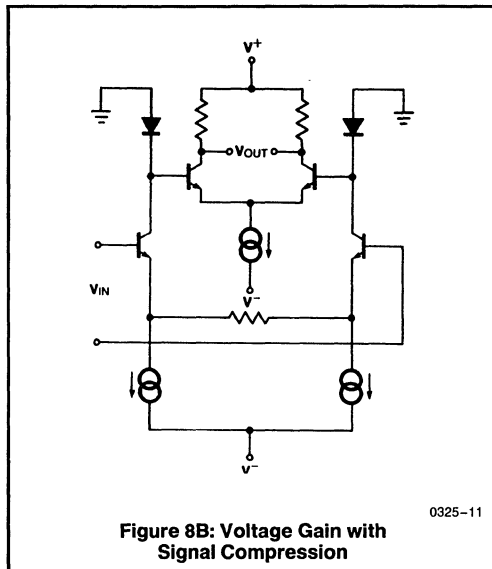
This circuit of Figure 7 still has the problem that the input voltage  $V_{IN}$  must be small to keep the differential amplifier in the linear region. To be able to handle large signals, we need an amplitude compression circuit.



**Figure 7: Typical Four Quadrant Multiplier-Modulator**



**Figure 8A: Current Gain Cell**



**Figure 8B: Voltage Gain with Signal Compression**

Figure 4 showed a current source formed by relying on the matching characteristics of a diode and the emitter base junction of a transistor. Extension of this idea to a differential circuit is shown in Figure 8A. In a differential pair, the input voltage splits the biasing current in a logarithmic ratio. (The usual assumption of linearity is useful only for small signals.) Since the input to the differential pair in Figure 8A is the difference in voltage across the two diodes, which in turn is proportional to the log of the ratio of drive currents, it follows that the ratio of diode currents and the ratio of collector currents are linearly related and independent of amplitude. If we combine this circuit with the voltage to current converter of Figure 5, we have Figure 8B. The output of the differential amplifier is now proportional to the input voltage over a large dynamic range, thereby improving linearity while minimizing drift and noise factors.

The complete schematic is shown in Figure 9. The differential pair  $Q_3$  and  $Q_4$  form a voltage to current converter whose output is compressed in collector diodes  $Q_1$  and  $Q_2$ . These diodes drive the balanced cross-coupled differential amplifier  $Q_7/Q_8$   $Q_{14}/Q_{15}$ . The gain of these amplifiers is modulated by the voltage to current converter  $Q_9$  and  $Q_{10}$ . Transistors  $Q_5$ ,  $Q_6$ ,  $Q_{11}$ , and  $Q_{12}$  are constant current sources which bias the voltage to current converter. The output amplifier comprises transistors  $Q_{16}$  through  $Q_{27}$ .

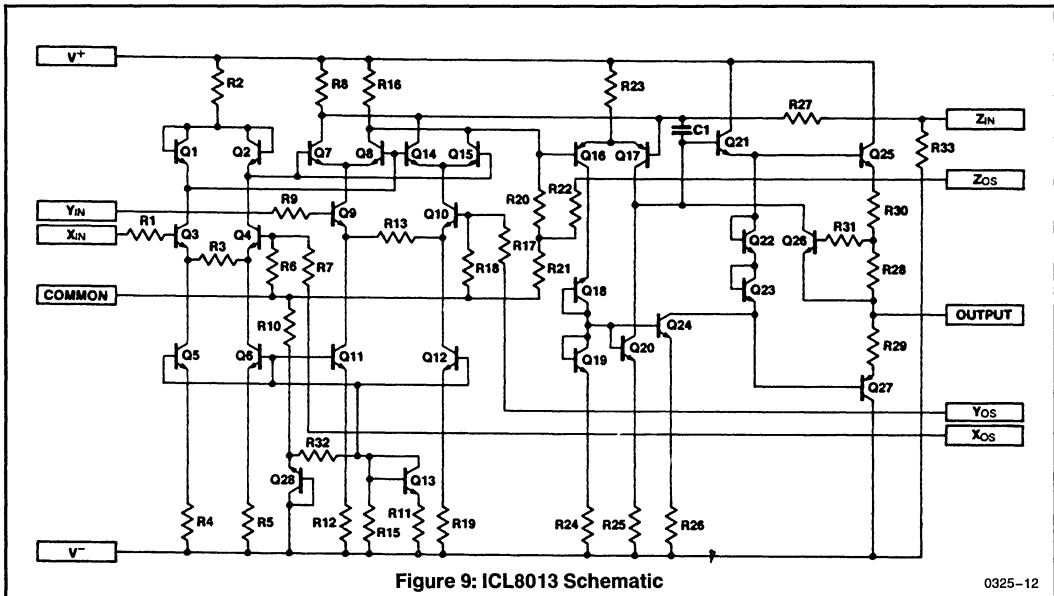


Figure 9: ICL8013 Schematic

0325-12

## MULTIPLICATION

In the standard multiplier connection, the Z terminal is connected to the op amp output. All of the modulator output current thus flows through the feedback resistor R27 and produces a proportional output voltage.

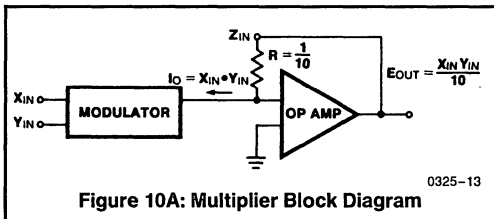


Figure 10A: Multiplier Block Diagram

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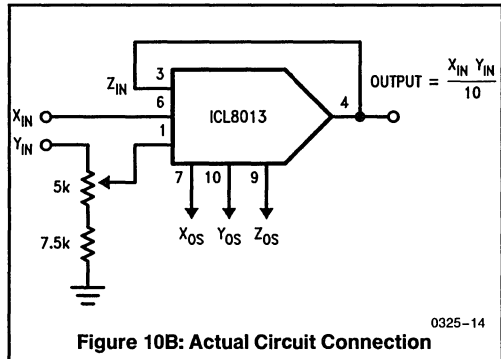


Figure 10B: Actual Circuit Connection

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## Multiplier Trimming Procedure

1. Set  $X_{IN} = Y_{IN} = 0V$  and adjust  $Z_{OS}$  for zero Output.
2. Apply a  $\pm 10V$  low frequency ( $\leq 100Hz$ ) sweep (sine or triangle) to  $Y_{IN}$  with  $X_{IN} = 0V$ , and adjust  $X_{OS}$  for minimum output.
3. Apply the sweep signal of Step 2 to  $X_{IN}$  with  $Y_{IN} = 0V$  and adjust  $Y_{OS}$  for minimum Output.
4. Readjust  $Z_{OS}$  as in Step 1, if necessary.
5. With  $X_{IN} = 10.0V$  DC and the sweep signal of Step 2 applied to  $Y_{IN}$ , adjust the Gain potentiometer for  $Output = Y_{IN}$ . This is easily accomplished with a differential scope plug-in (A + B) by inverting one signal and adjusting Gain control for  $(Output - Y_{IN}) = Zero$ .

## DIVISION

If the Z terminal is used as an input, and the output of the op-amp connected to the Y input, the device functions as a divider. Since the input to the op-amp is at virtual ground, and requires negligible bias current, the overall feedback forces the modulator output current to equal the current produced by Z.

$$\text{Therefore } I_O = X_{IN} \cdot Y_{IN} = \frac{Z_{IN}}{R} = 10Z_{IN}$$

$$\text{Since } Y_{IN} = E_{OUT}, E_{OUT} = \frac{10Z_{IN}}{X_{IN}}$$

Note that when connected as a divider, the X input must be a negative voltage to maintain overall negative feedback.

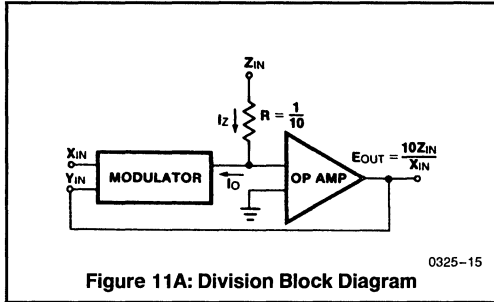


Figure 11A: Division Block Diagram

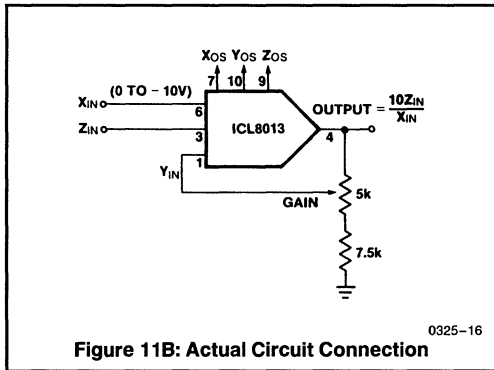


Figure 11B: Actual Circuit Connection

## Divider Trimming Procedure

1. Set trimming potentiometers at mid-scale by adjusting voltage on pins 7, 9 and 10 ( $X_{OS}$ ,  $Y_{OS}$ ,  $Z_{OS}$ ) for zero volts.
2. With  $Z_{IN}=0V$ , trim  $Z_{OS}$  to hold the Output constant, as  $X_{IN}$  is varied from  $-10V$  through  $-1V$ .
3. With  $Z_{IN}=0V$  and  $X_{IN}=-10.0V$  adjust  $Y_{OS}$  for zero Output voltage.
4. With  $Z_{IN}=X_{IN}$  (and/or  $Z_{IN}=-X_{IN}$ ) adjust  $X_{OS}$  for minimum worst-case variation of Output, as  $X_{IN}$  is varied from  $-10V$  to  $-1V$ .
5. Repeat Steps 2 and 3 if Step 4 required a large initial adjustment.
6. With  $Z_{IN}=X_{IN}$  (and/or  $Z_{IN}=-X_{IN}$ ) adjust the gain control until the output is the closest average around  $+10.0V$  ( $-10V$  for  $Z_{IN}=-X_{IN}$ ) as  $X_{IN}$  is varied from  $-10V$  to  $-3V$ .

## SQUARING

The squaring function is achieved by simply multiplying with the two inputs tied together. The squaring circuit may also be used as the basis for a frequency doubler since  $\cos^2\omega t = \frac{1}{2}(\cos 2\omega t + 1)$ .

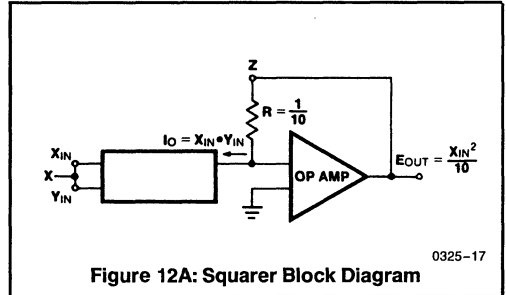


Figure 12A: Squarer Block Diagram

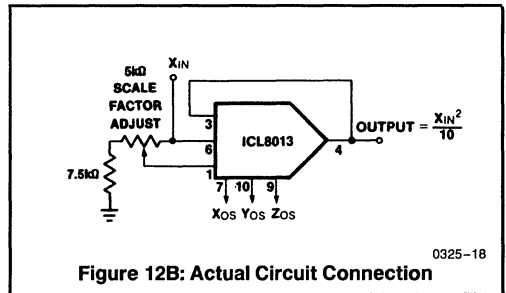


Figure 12B: Actual Circuit Connection

## SQUARE ROOT

Tying the X and Y inputs together and using overall feedback from the Op Amp results in the square root function. The output of the modulator is again forced to equal the current produced by the Z input.

$$I_O = X_{IN} \cdot Y_{IN} = (-E_{OUT})^2 = 10Z_{IN}$$

$$E_{OUT} = -\sqrt{10Z_{IN}}$$

The output is a negative voltage which maintains overall negative feedback. A diode in series with the Op Amp output prevents the latchup that would otherwise occur for negative input voltages.

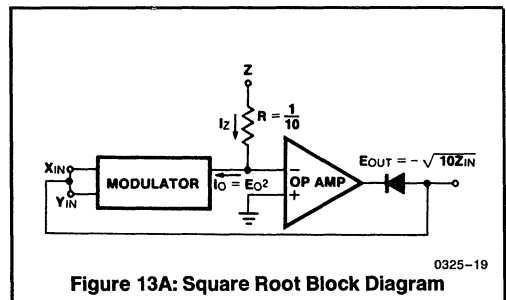


Figure 13A: Square Root Block Diagram

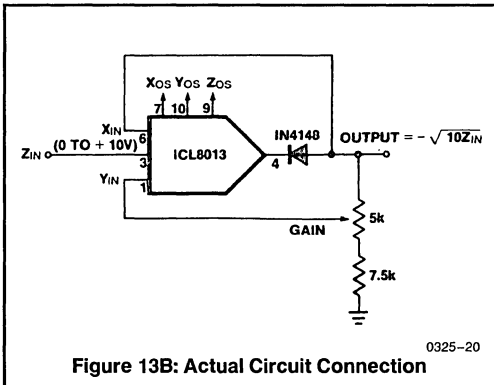


Figure 13B: Actual Circuit Connection

### Square Root Trimming Procedure

1. Connect the ICL8013 in the *Divider* configuration.
2. Adjust  $Z_{OS}$ ,  $Y_{OS}$ ,  $X_{OS}$ , and Gain using Steps 1 through 6 of *Divider Trimming Procedure*.
3. Convert to the *Square Root* configuration by connecting  $X_{IN}$  to the Output and inserting a diode between Pin 4 and the Output node.
4. With  $Z_{IN} = 0V$  adjust  $Z_{OS}$  for zero Output voltage.

### VARIABLE GAIN AMPLIFIER

Most applications for the ICL8013 are straight forward variations of the simple arithmetic functions described above. Although the circuit description frequently disguises the fact, it has already been shown that the frequency doubler is nothing more than a squaring circuit. Similarly the variable gain amplifier is nothing more than a multiplier, with the input signal applied at the X input and the control voltage applied at the Y input.

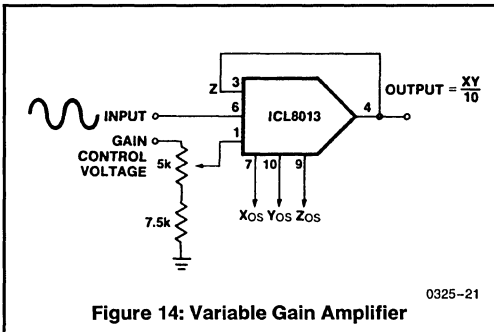


Figure 14: Variable Gain Amplifier

### TYPICAL APPLICATIONS

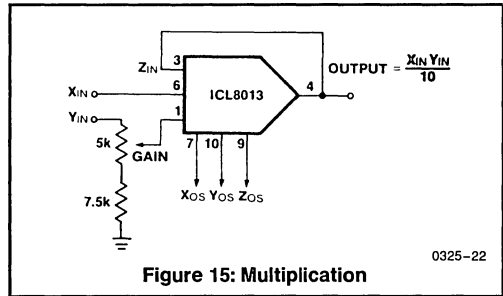


Figure 15: Multiplication

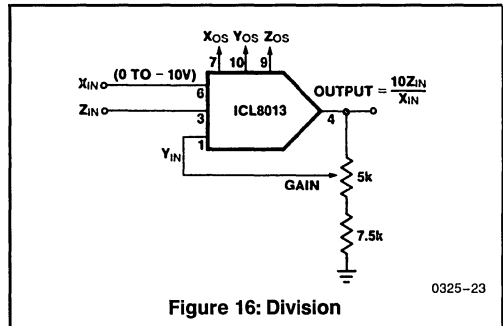


Figure 16: Division

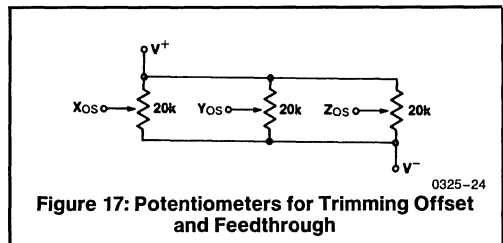


Figure 17: Potentiometers for Trimming Offset and Feedthrough

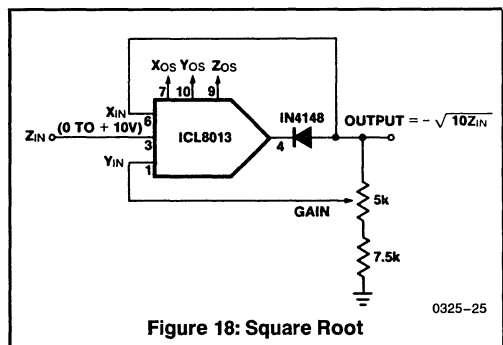
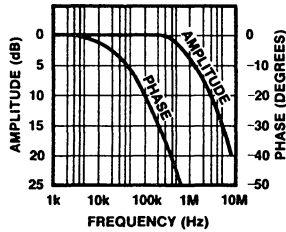


Figure 18: Square Root

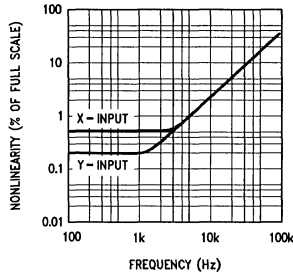
## TYPICAL PERFORMANCE CHARACTERISTICS

AMPLITUDE AND PHASE AS A FUNCTION OF FREQUENCY



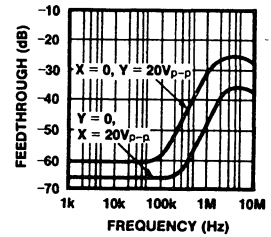
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NONLINEARITY AS A FUNCTION OF FREQUENCY



0325-27

FEEDTHROUGH AS A FUNCTION OF FREQUENCY



0325-28

## DEFINITION OF TERMS

**Multiplication/Division Error:** This is the basic accuracy specification. It includes terms due to linearity, gain, and offset errors, and is expressed as a percentage of the full scale output.

**Feedthrough:** With either input at zero, the output of an ideal multiplier should be zero regardless of the signal applied to the other input. The output seen in a non-ideal multiplier is known as the feedthrough.

**Nonlinearity:** The maximum deviation from the best straight line constructed through the output data, expressed as a percentage of full scale. One input is held constant and the other swept through its nominal range. The nonlinearity is the component of the total multiplication/division error which cannot be trimmed out.

# ICL8038

## Precision Waveform Generator/Voltage Controlled Oscillator

### GENERAL DESCRIPTION

The ICL8038 Waveform Generator is a monolithic integrated circuit capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency (or repetition rate) can be selected externally from .001Hz to more than 300kHz using either resistors or capacitors, and frequency modulation and sweeping can be accomplished with an external voltage. The ICL8038 is fabricated with advanced monolithic technology, using Schottky-barrier diodes and thin film resistors, and the output is stable over a wide range of temperature and supply variations. These devices may be interfaced with phase locked loop circuitry to reduce temperature drift to less than 250ppm/°C.

### FEATURES

- Low Frequency Drift With Temperature — 250ppm/°C
- Simultaneous Sine, Square, and Triangle Wave Outputs
- Low Distortion — 1% (Sine Wave Output)
- High Linearity — 0.1% (Triangle Wave Output)
- Wide Operating Frequency Range — 0.001Hz to 300kHz
- Variable Duty Cycle — 2% to 98%
- High Level Outputs — TTL to 28V
- Easy to Use — Just A Handful of External Components Required

### ORDERING INFORMATION

| Part Number  | Stability     | Temp. Range     | Package       |
|--------------|---------------|-----------------|---------------|
| ICL8038CCPD  | 250ppm/°C typ | 0°C to +70°C    | 14 pin DIP    |
| ICL8038CCJD  | 250ppm/°C typ | 0°C to +70°C    | 14 pin Cerdip |
| ICL8038BCJD  | 180ppm/°C typ | 0°C to +70°C    | 14 pin Cerdip |
| ICL8038ACJD  | 120ppm/°C typ | 0°C to +70°C    | 14 pin Cerdip |
| ICL8038BMJD* | 350ppm/°C max | -55°C to +125°C | 14 pin Cerdip |
| ICL8038AMJD* | 250ppm/°C max | -55°C to +125°C | 14 pin Cerdip |

\*Add /883B to part number if 883 processing is required.

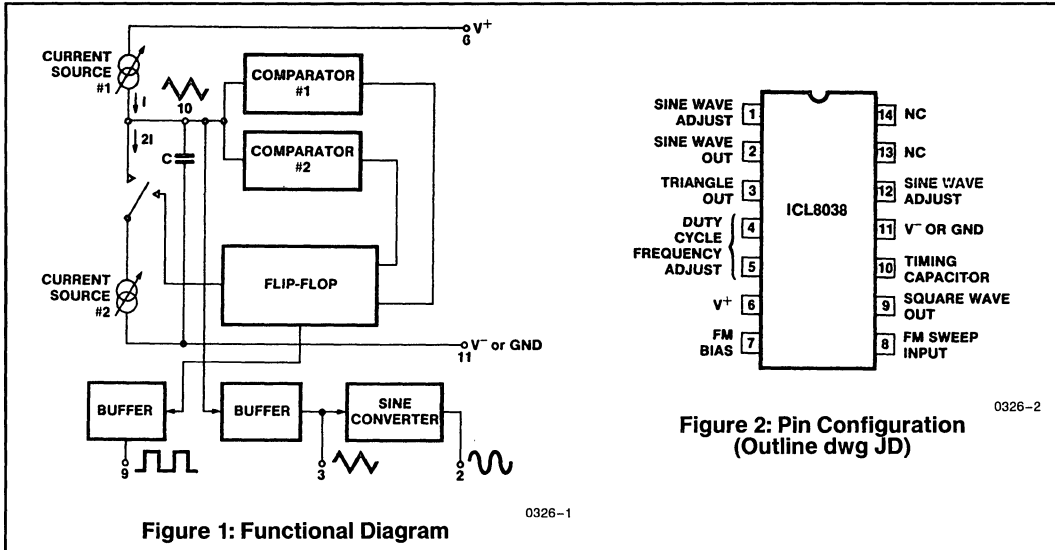


Figure 1: Functional Diagram

Figure 2: Pin Configuration (Outline dwg JD)

8  
SPECIAL  
ANALOG CIRCUITS

HARRIS SEMICONDUCTOR'S SOLE AND EXCLUSIVE WARRANTY OBLIGATION WITH RESPECT TO THIS PRODUCT SHALL BE THAT STATED IN THE WARRANTY ARTICLE OF THE CONDITION OF SALE. THE WARRANTY SHALL BE EXCLUSIVE AND SHALL BE IN LIEU OF ALL OTHER WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR USE.

NOTE: All typical values have been characterized but are not tested.

# ICL8038

## ABSOLUTE MAXIMUM RATINGS

|                                    |                |
|------------------------------------|----------------|
| Supply Voltage ( $V^-$ to $V^+$ )  | 36V            |
| Power Dissipation <sup>(1)</sup>   | 750mW          |
| Input Voltage (any pin)            | $V^-$ to $V^+$ |
| Input Current (Pins 4 and 5)       | 25mA           |
| Output Sink Current (Pins 3 and 9) | 25mA           |

|                                     |                 |
|-------------------------------------|-----------------|
| Storage Temperature Range           | -65°C to +150°C |
| Operating Temperature Range:        |                 |
| 8038AM, 8038BM                      | -55°C to +125°C |
| 8038AC, 8038BC, 8038CC              | 0°C to +70°C    |
| Lead Temperature (Soldering, 10sec) | 300°C           |

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**NOTE 1:** Derate ceramic package at 12.5mW/°C for ambient temperatures above 100°C.

## ELECTRICAL CHARACTERISTICS

( $V_{SUPPLY} = \pm 10V$  or  $+20V$ ,  $T_A = 25^\circ C$ ,  $R_L = 10k\Omega$ , Test Circuit Unless

Otherwise Specified)

| Symbol   | General Characteristics  | 8038CC  |      |          | 8038BC(BM) |      |          | 8038AC(AM) |      |          | Units               |
|--|--|---------|------|----------|------------|------|----------|------------|------|----------|---------------------|
|  |  | Min     | Typ  | Max      | Min        | Typ  | Max      | Min        | Typ  | Max      |                     |
| $V_{SUPPLY}$                                     | Supply Voltage Operating Range   |         |      |          |            |      |          |            |      |          |                     |
| $V^+$  | Single Supply  | +10     |      | +30      | +10        |      | 30       | +10        |      | 30       | V                   |
| $V^+$ , $V^-$                                    | Dual Supplies  | $\pm 5$ |      | $\pm 15$ | $\pm 5$    |      | $\pm 15$ | $\pm 5$    |      | $\pm 15$ | V                   |
| $I_{SUPPLY}$                                     | Supply Current ( $V_{SUPPLY} = \pm 10V$ ) <sup>(2)</sup>                       |         |      |          |            |      |          |            |      |          |                     |
|  | 8038AM, 8038BM   |         |      |          | 12         | 15   |          | 12         | 15   |          | mA                  |
|  | 8038AC, 8038BC, 8038CC   |         | 12   | 20       |            | 12   | 20       |            | 12   | 20       | mA                  |
| <b>Frequency Characteristics (all waveforms)</b> |  |         |      |          |            |      |          |            |      |          |                     |
| $f_{max}$  | Maximum Frequency of Oscillation   | 100     |      |          | 100        |      |          | 100        |      |          | kHz                 |
| $f_{sweep}$                                      | Sweep Frequency of FM Input  |         | 10   |          |            | 10   |          |            | 10   |          | kHz                 |
|  | Sweep FM Range <sup>(3)</sup>  |         | 35:1 |          |            | 35:1 |          |            | 35:1 |          |                     |
|  | FM Linearity 10:1 Ratio  |         | 0.5  |          |            | 0.2  |          |            | 0.2  |          | %                   |
| $\Delta f/\Delta T$                              | Frequency Drift With Temperature <sup>(5)</sup><br>8038 AC, BC, CC 0°C to 70°C |         | 250  |          |            | 180  |          |            | 120  |          | ppm/°C              |
|  | 8038 AM, BM, -55°C to 125°C  |         |      |          |            |      | 350      |            |      | 250      |                     |
| $\Delta f/\Delta V$                              | Frequency Drift With Supply Voltage<br>(Over Supply Voltage Range)             |         | 0.05 |          |            | 0.05 |          |            | 0.05 |          | %/V                 |
| <b>Output Characteristics</b>                    |  |         |      |          |            |      |          |            |      |          |                     |
| $I_{OLK}$  | <b>Square-Wave</b><br>Leakage Current ( $V_G = 30V$ )                          |         |      | 1        |            |      | 1        |            |      | 1        | $\mu A$             |
|  | <b>Saturation Voltage</b> ( $I_{SINK} = 2mA$ )                                 |         | 0.2  | 0.5      |            | 0.2  | 0.4      |            | 0.2  | 0.4      | V                   |
| $t_r$  | Rise Time ( $R_L = 4.7k\Omega$ )   |         | 180  |          |            | 180  |          |            | 180  |          | ns                  |
| $t_f$  | Fall Time ( $R_L = 4.7k\Omega$ )   |         | 40   |          |            | 40   |          |            | 40   |          | ns                  |
| $\Delta D$                                       | Typical Duty Cycle Adjust (Note 6)   | 2       |      | 98       | 2          |      | 98       | 2          |      | 98       | %                   |
| $V_{TRIANGLE}$                                   | <b>Triangle/Sawtooth/Ramp</b><br>Amplitude ( $R_{TRI} = 100k\Omega$ )          | 0.30    | 0.33 |          | 0.30       | 0.33 |          | 0.30       | 0.33 |          | $\times V_{SUPPLY}$ |
|  | Linearity  |         | 0.1  |          |            | 0.05 |          |            | 0.05 |          | %                   |
| $Z_{OUT}$  | Output Impedance ( $I_{OUT} = 5mA$ )   |         | 200  |          |            | 200  |          |            | 200  |          | $\Omega$            |
| $V_{SINE}$                                       | <b>Sine-Wave</b><br>Amplitude ( $R_{SINE} = 100k\Omega$ )                      | 0.2     | 0.22 |          | 0.2        | 0.22 |          | 0.2        | 0.22 |          | $\times V_{SUPPLY}$ |
| THD  | THD ( $R_S = 1M\Omega$ ) <sup>(4)</sup>  |         | 2.0  | 5        |            | 1.5  | 3        |            | 1.0  | 1.5      | %                   |
| THD  | THD Adjusted (Use Figure 6)  |         | 1.5  |          |            | 1.0  |          |            | 0.8  |          | %                   |

**NOTES:** 2.  $R_A$  and  $R_B$  currents not included.

3.  $V_{SUPPLY} = 20V$ ;  $R_A$  and  $R_B = 10k\Omega$ ,  $f \approx 10kHz$  nominal; can be extended 1000 to 1. See Figures 7a and 7b.

4. 82k $\Omega$  connected between pins 11 and 12, Triangle Duty Cycle set at 50%. (Use  $R_A$  and  $R_B$ .)

5. Figure 3, pins 7 and 8 connected,  $V_{SUPPLY} = \pm 10V$ . See Typical Curves for T.C. vs  $V_{SUPPLY}$ .

6. Not tested, typical value for design purposes only.

*NOTE: All typical values have been characterized but are not tested.*

## TEST CONDITIONS

| Parameter  |          | R <sub>A</sub> | R <sub>B</sub> | R <sub>L</sub> | C <sub>1</sub> | SW <sub>1</sub> | Measure               |
|--|----------|----------------|----------------|----------------|----------------|-----------------|-----------------------|
| Supply Current                                     |          | 10kΩ           | 10kΩ           | 10kΩ           | 3.3nF          | Closed          | Current into Pin 6    |
| Sweep FM Range <sup>(1)</sup>                      |          | 10kΩ           | 10kΩ           | 10kΩ           | 3.3nF          | Open            | Frequency at Pin 9    |
| Frequency Drift with Temperature                   |          | 10kΩ           | 10kΩ           | 10kΩ           | 3.3nF          | Closed          | Frequency at Pin 3    |
| Frequency Drift with Supply Voltage <sup>(2)</sup> |          | 10kΩ           | 10kΩ           | 10kΩ           | 3.3nF          | Closed          | Frequency at Pin 9    |
| Output Amplitude:<br>(Note 4)                      | Sine     | 10kΩ           | 10kΩ           | 10kΩ           | 3.3nF          | Closed          | Pk-Pk output at Pin 2 |
|  | Triangle | 10kΩ           | 10kΩ           | 10kΩ           | 3.3nF          | Closed          | Pk-Pk output at Pin 3 |
| Leakage Current (off) <sup>(3)</sup>               |          | 10kΩ           | 10kΩ           |                | 3.3nF          | Closed          | Current into Pin 9    |
| Saturation Voltage (on) <sup>(3)</sup>             |          | 10kΩ           | 10kΩ           |                | 3.3nF          | Closed          | Output (low) at Pin 9 |
| Rise and Fall Times (Note 5)                       |          | 10kΩ           | 10kΩ           | 4.7kΩ          | 3.3nF          | Closed          | Waveform at Pin 9     |
| Duty Cycle Adjust:<br>(Note 5)                     | MAX      | 50kΩ           | ~ 1.6kΩ        | 10kΩ           | 3.3nF          | Closed          | Waveform at Pin 9     |
|  | MIN      | ~ 25kΩ         | 50kΩ           | 10kΩ           | 3.3nF          | Closed          | Waveform at Pin 9     |
| Triangle Waveform Linearity                        |          | 10kΩ           | 10kΩ           | 10kΩ           | 3.3nF          | Closed          | Waveform at Pin 3     |
| Total Harmonic Distortion                          |          | 10kΩ           | 10kΩ           | 10kΩ           | 3.3nF          | Closed          | Waveform at Pin 2     |

**NOTES:** 1. The hi and lo frequencies can be obtained by connecting pin 8 to pin 7 (f<sub>hi</sub>) and then connecting pin 8 to pin 6 (f<sub>lo</sub>). Otherwise apply Sweep Voltage at pin 8 ( $\frac{2}{3} V_{SUPPLY} + 2V$ )  $\leq V_{SWEEP} \leq V_{SUPPLY}$  where  $V_{SUPPLY}$  is the total supply voltage. In Figure 7b, pin 8 should vary between 5.3V and 10V with respect to ground.

2.  $10V \leq V^+ \leq 30V$ , or  $\pm 5V \leq V_{SUPPLY} \leq \pm 15V$ .

3. Oscillation can be halted by forcing pin 10 to +5 volts or -5 volts.

4. Output Amplitude is tested under static conditions by forcing pin 10 to 5.0V then to -5.0V.

5. Not tested; for design purposes only.

## DEFINITION OF TERMS:

**Supply Voltage** ( $V_{SUPPLY}$ ). The total supply voltage from  $V^+$  to  $V^-$ .

**Supply Current.** The supply current required from the power supply to operate the device, excluding load currents and the currents through  $R_A$  and  $R_B$ .

**Frequency Range.** The frequency range at the square wave output through which circuit operation is guaranteed.

**Sweep FM Range.** The ratio of maximum frequency to minimum frequency which can be obtained by applying a sweep voltage to pin 8. For correct operation, the sweep voltage should be within the range

$$\left(\frac{2}{3} V_{SUPPLY} + 2V\right) < V_{SWEEP} < V_{SUPPLY}$$

**FM Linearity.** The percentage deviation from the best-fit straight line on the control voltage versus output frequency curve.

**Output Amplitude.** The peak-to-peak signal amplitude appearing at the outputs.

**Saturation Voltage.** The output voltage at the collector of Q<sub>23</sub> when this transistor is turned on. It is measured for a sink current of 2mA.

**Rise and Fall Times.** The time required for the square wave output to change from 10% to 90%, or 90% to 10%, of its final value.

**Triangle Waveform Linearity.** The percentage deviation from the best-fit straight line on the rising and falling triangle waveform.

**Total Harmonic Distortion.** The total harmonic distortion at the sine-wave output.

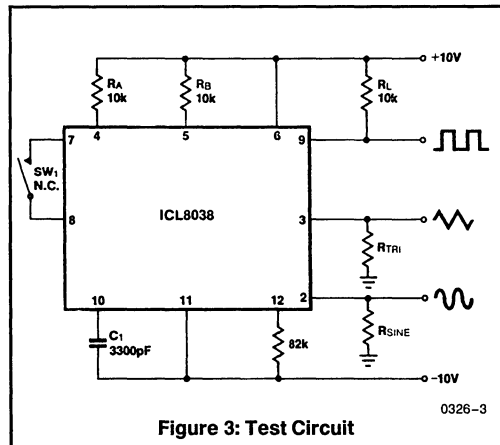
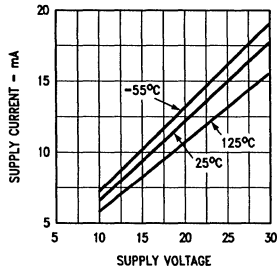


Figure 3: Test Circuit

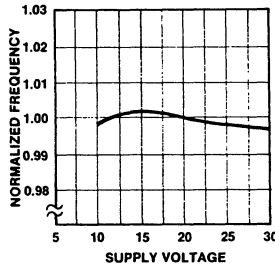
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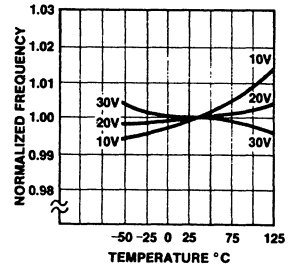
## TYPICAL PERFORMANCE CHARACTERISTICS



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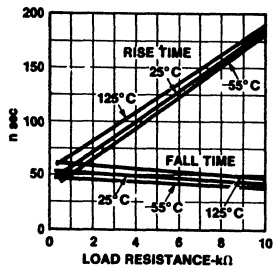


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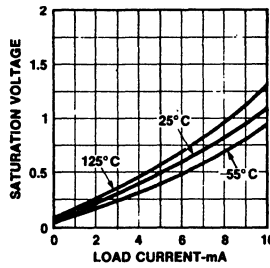


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### Performance of the Square-Wave Output

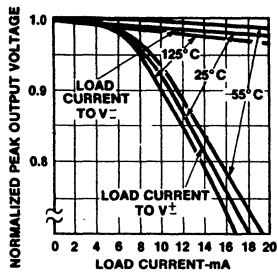


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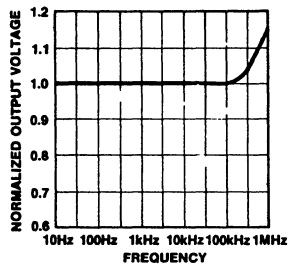


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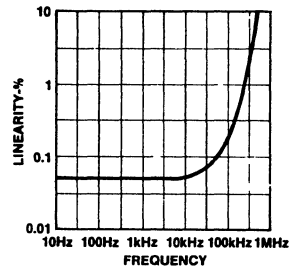
### Performance of Triangle-Wave Output



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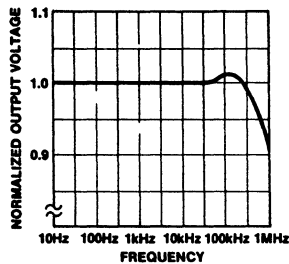


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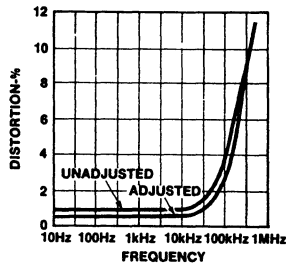


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### Performance of Sine-Wave Output



0326-12



0326-13

NOTE: All typical values have been characterized but are not tested.

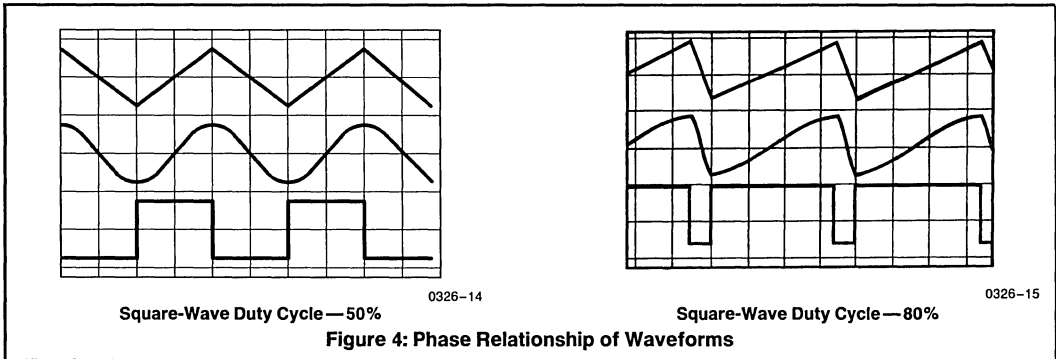


Figure 4: Phase Relationship of Waveforms

## DETAILED DESCRIPTION (See Figure 1)

An external capacitor C is charged and discharged by two current sources. Current source #2 is switched on and off by a flip-flop, while current source #1 is on continuously. Assuming that the flip-flop is in a state such that current source #2 is off, and the capacitor is charged with a current I, the voltage across the capacitor rises linearly with time. When this voltage reaches the level of comparator #1 (set at  $\frac{2}{3}$  of the supply voltage), the flip-flop is triggered, changes states, and releases current source #2. This current source normally carries a current 2I, thus the capacitor is discharged with a net-current I and the voltage across it drops linearly with time. When it has reached the level of comparator #2 (set at  $\frac{1}{3}$  of the supply voltage), the flip-flop is triggered into its original state and the cycle starts again.

Four waveforms are readily obtainable from this basic generator circuit. With the current sources set at I and 2I respectively, the charge and discharge times are equal. Thus a triangle waveform is created across the capacitor and the flip-flop produces a square-wave. Both waveforms are fed to buffer stages and are available at pins 3 and 9.

The levels of the current sources can, however, be selected over a wide range with two external resistors. Therefore, with the two currents set at values different from I and 2I, an asymmetrical sawtooth appears at terminal 3 and pulses with a duty cycle from less than 1% to greater than 99% are available at terminal 9.

The sine-wave is created by feeding the triangle-wave into a non-linear network (sine-converter). This network provides a decreasing shunt-impedance as the potential of the triangle moves toward the two extremes.

## WAVEFORM TIMING

The *symmetry* of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figure 5. Best results are obtained by keeping the timing resistors  $R_A$  and  $R_B$  separate (a).  $R_A$  controls the rising portion of the triangle and sine-wave and the 1 state of the square-wave.

The magnitude of the triangle-waveform is set at  $\frac{1}{3} V_{SUPPLY}$ ; therefore the rising portion of the triangle is,

$$t_1 = \frac{C \times V}{I} = \frac{C \times \frac{1}{3} \times V_{SUPPLY} \times R_A}{0.22 \times V_{SUPPLY}} = \frac{R_A \times C}{0.66}$$

The falling portion of the triangle and sine-wave and the 0 state of the square-wave is:

$$t_2 = \frac{C \times V}{I} = \frac{C \times \frac{1}{3} V_{SUPPLY}}{2(0.22) \frac{V_{SUPPLY}}{R_B} - 0.22 \frac{V_{SUPPLY}}{R_A}} = \frac{R_A R_B C}{0.66(2R_A - R_B)}$$

Thus a 50% duty cycle is achieved when  $R_A = R_B$ .

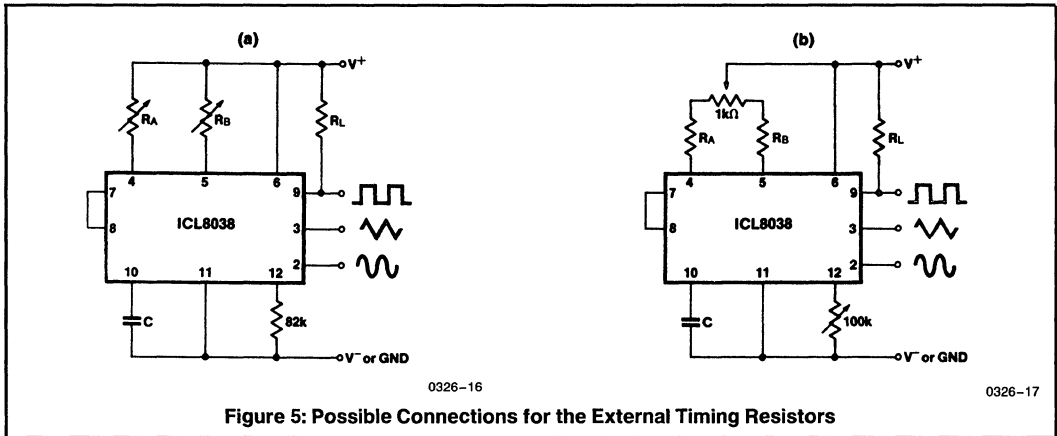
If the duty-cycle is to be varied over a small range about 50% only, the connection shown in Figure 5b is slightly more convenient.

With two separate timing resistors, the frequency is given by

$$f = \frac{1}{t_1 + t_2} = \frac{1}{\frac{R_A C}{0.66} \left( 1 + \frac{R_B}{2R_A - R_B} \right)}$$

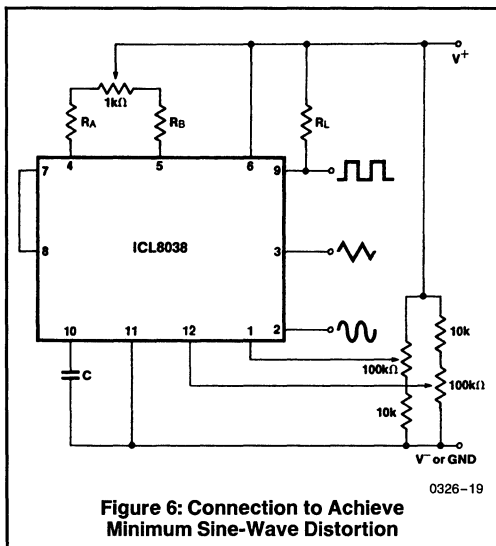
or, if  $R_A = R_B = R$

$$f = \frac{0.33}{RC} \text{ (for Figure 5a)}$$



Neither time nor frequency are dependent on supply voltage, even though none of the voltages are regulated inside the integrated circuit. This is due to the fact that both currents *and* thresholds are direct, linear functions of the supply voltage and thus their effects cancel.

To minimize *sine-wave* distortion the 82kΩ resistor between pins 11 and 12 is best made variable. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 6; this configuration allows a typical reduction of sine-wave distortion close to 0.5%.



## SELECTING $R_A$ , $R_B$ and $C$

For any given output frequency, there is a wide range of RC combinations that will work, however certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than 1μA are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents (>5mA), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will, therefore, be obtained with charging currents of 10μA to 1mA. If pins 7 and 8 are shorted together, the magnitude of the charging current due to  $R_A$  can be calculated from:

$$I = \frac{R_1 \times (V^+ - V^-)}{(R_1 + R_2)} \times \frac{1}{R_A} = \frac{0.22(V^+ - V^-)}{R_A}$$

$R_1$  and  $R_2$  are shown in Figure 13.

A similar calculation holds for  $R_B$ .

The capacitor value should be chosen at the upper end of its possible range.

## WAVEFORM OUT LEVEL CONTROL AND POWER SUPPLIES

The waveform generator can be operated either from a single power-supply (10 to 30 Volts) or a dual power-supply ( $\pm 5$  to  $\pm 15$  Volts). With a single power-supply the average levels of the triangle and sine-wave are at exactly one-half of the supply voltage, while the square-wave alternates between  $V^+$  and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The square-wave output is not committed. A load resistor can be connected to a different power-supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (30V). In this way, the square-wave output can be made TTL compatible (load resistor connected to +5 Volts) while the waveform generator itself is powered from a much higher voltage.

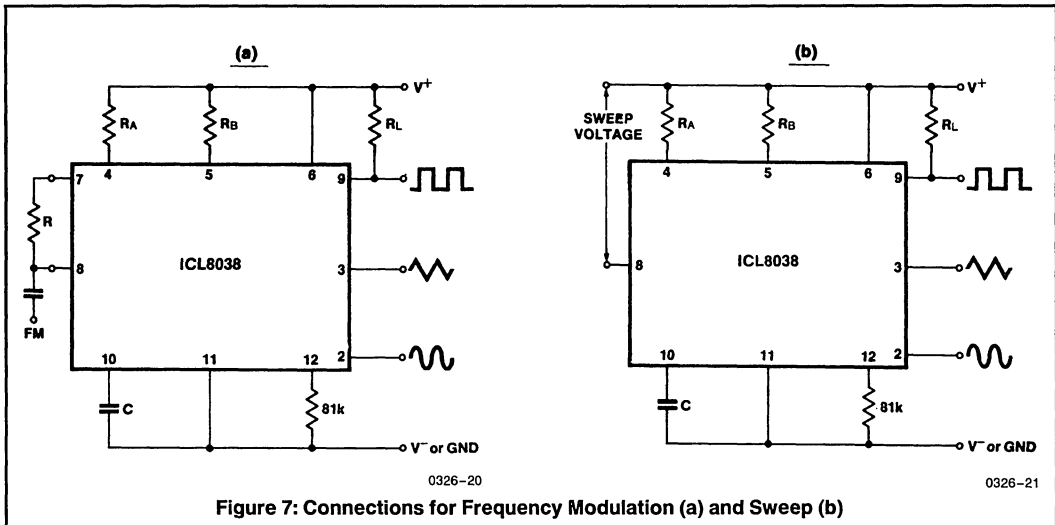


Figure 7: Connections for Frequency Modulation (a) and Sweep (b)

## FREQUENCY MODULATION AND SWEEPING

The frequency of the waveform generator is a direct function of the DC voltage at terminal 8 (measured from  $V^+$ ). By altering this voltage, frequency modulation is performed. For small deviations (e.g.  $\pm 10\%$ ) the modulating signal can be applied directly to pin 8, merely providing DC decoupling with a capacitor as shown in Figure 7a. An external resistor between pins 7 and 8 is not necessary, but it can be used to increase input impedance from about  $8k\Omega$  (pins 7 and 8 connected together), to about  $(R + 8k\Omega)$ .

For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8 (Figure 7b). In this way the entire bias for the current sources is created by the modulating signal, and a very large (e.g. 1000:1) sweep range is created ( $f=0$  at  $V_{sweep}=0$ ). Care must be taken, however, to regulate the supply voltage; in this configuration the charge current is no longer a function of the supply voltage (yet the trigger thresholds still are) and thus the frequency becomes dependent on the supply voltage. The potential on Pin 8 may be swept down from  $V^+$  by  $(\frac{1}{2} V_{SUPPLY} - 2V)$ .

## APPLICATIONS

The sine wave output has a relatively high output impedance ( $1k\Omega$  Typ). The circuit of Figure 8 provides buffering, gain and amplitude adjustment. A simple op amp follower could also be used.

With a dual supply voltage the external capacitor on Pin 10 can be shorted to ground to halt the ICL8038 oscillation. Figure 9 shows a FET switch, diode ANded with an input strobe signal to allow the output to always start on the same slope.

To obtain a 1000:1 Sweep Range on the ICL8038 the voltage across external resistors  $R_A$  and  $R_B$  must decrease to nearly zero. This requires that the highest voltage on con-

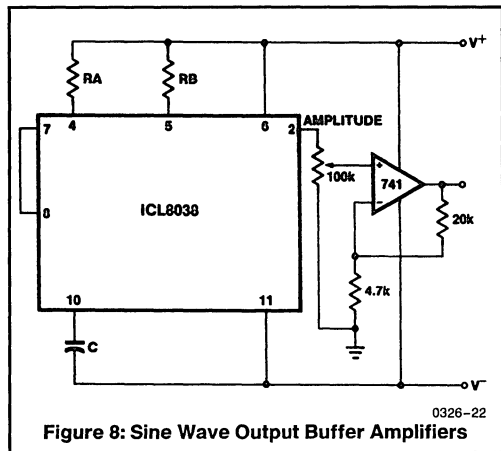


Figure 8: Sine Wave Output Buffer Amplifiers

trol Pin 8 exceed the voltage at the top of  $R_A$  and  $R_B$  by a few hundred millivolts. The Circuit of Figure 10 achieves this by using a diode to lower the effective supply voltage on the ICL8038. The large resistor on pin 5 helps reduce duty cycle variations with sweep.

The linearity of input sweep voltage versus output frequency can be significantly improved by using an op amp as shown in Figure 11.

## USE IN PHASE-LOCKED LOOPS

Its high frequency stability makes the ICL8038 an ideal building block for a phase-locked loop as shown in Figure 12. In this application the remaining functional blocks, the



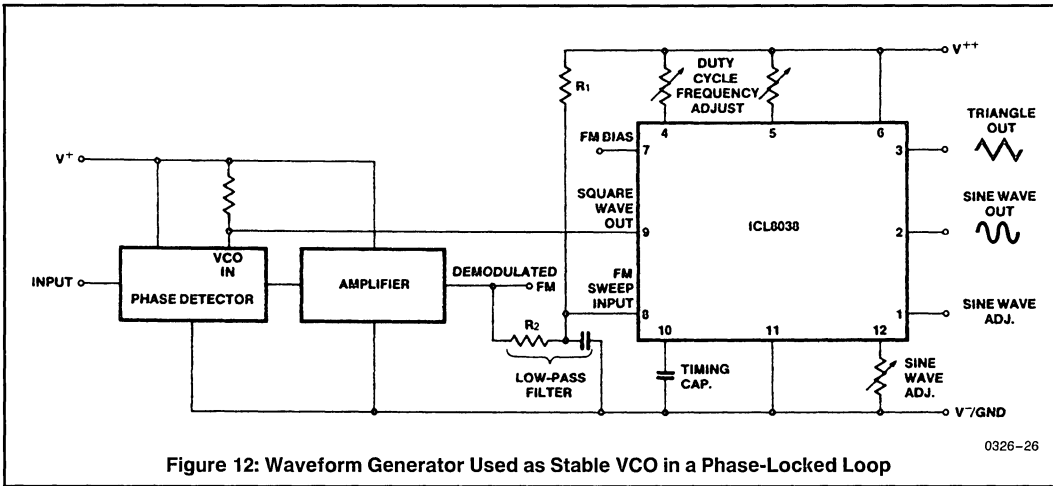


Figure 12: Waveform Generator Used as Stable VCO in a Phase-Locked Loop

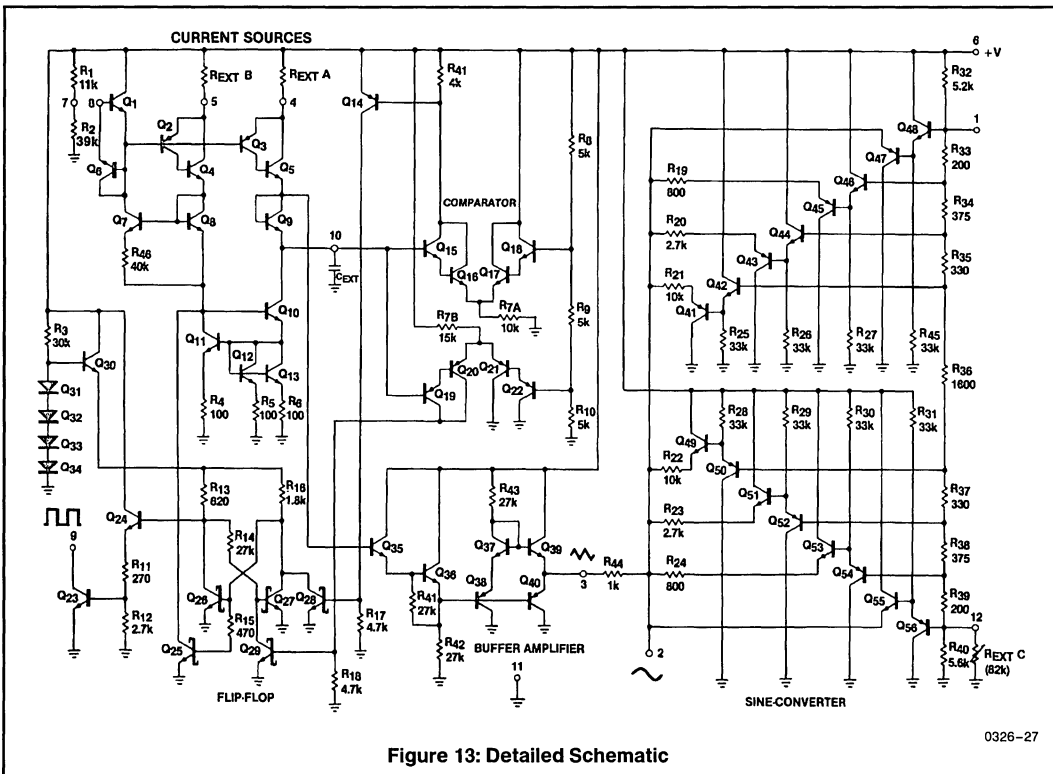


Figure 13: Detailed Schematic

NOTE: All typical values have been characterized but are not tested.

### GENERAL DESCRIPTION

The 8048 is a monolithic logarithmic amplifier capable of handling six decades of current input, or three decades of voltage input. It is fully temperature compensated and is nominally designed to provide 1 volt of output for each decade change of input. For increased flexibility, the scale factor, reference current and offset voltage are externally adjustable.

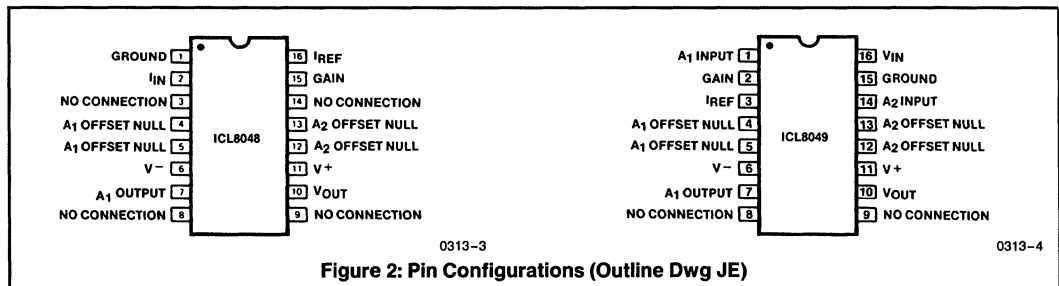
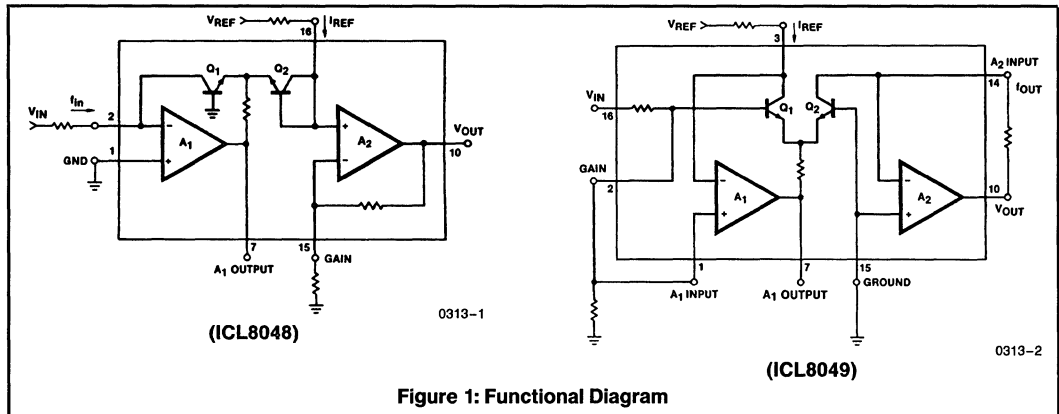
The 8049 is the antilogarithmic counterpart of the 8048; it nominally generates one decade of output voltage for each 1 volt change at the input.

### FEATURES

- ½% Full Scale Accuracy
- Temperature Compensated for 0°C to +70°C Operation
- Scale Factor 1V/Decade, Adjustable
- 120dB Dynamic Current Range (8048)
- 60dB Dynamic Voltage Range (8048 & 8049)
- Dual JFET-Input Op-Amps

### ORDERING INFORMATION

| Part Number | Error (25°C) | Temperature Range | Package       |
|-------------|--------------|-------------------|---------------|
| ICL8048BCJE | 30mV         | 0°C to +70°C      | 16 Pin CERDIP |
| ICL8048CCJE | 60mV         | 0°C to +70°C      | 16 Pin CERDIP |
| ICL8049BCJE | 10mV         | 0°C to +70°C      | 16 Pin CERDIP |
| ICL8049CCJE | 25mV         | 0°C to +70°C      | 16 Pin CERDIP |



# ICL8048/ICL8049

## ABSOLUTE MAXIMUM RATINGS (ICL8048)

|                                       |        |
|---------------------------------------|--------|
| Supply Voltage                        | ± 18V  |
| $I_{IN}$ (Input Current)              | 2mA    |
| $I_{REF}$ (Reference Current)         | 2mA    |
| Voltage between Offset Null and $V^+$ | ± 0.5V |
| Power Dissipation                     | 750mW  |

|                                     |                 |
|-------------------------------------|-----------------|
| Operating Temperature Range         | 0°C to +70°C    |
| Output Short Circuit Duration       | Indefinite      |
| Storage Temperature Range           | -65°C to +150°C |
| Lead Temperature (Soldering, 10sec) | 300°C           |

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS (ICL8048) $V_S = \pm 15V$ , $T_A = 25^\circ C$ , $I_{REF} = 1mA$ , scale factor adjusted for 1V/decade unless otherwise specified.

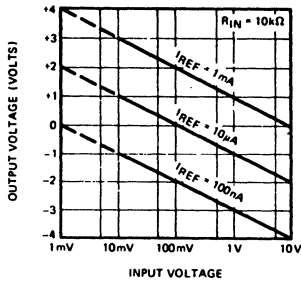
| Parameter  | Test Conditions                                      | 8048BC |      |      | 8048CC |      |     | Units         |
|--|--|--------|------|------|--------|------|-----|---------------|
|  |  | Min    | Typ  | Max  | Min    | Typ  | Max |               |
| Dynamic Range<br>$I_{IN}$ (1nA – 1mA)<br>$V_{IN}$ (10mV – 10V) | $R_{IN} = 10k\Omega$                                 | 120    |      |      | 120    |      |     | dB            |
|  |  | 60     |      |      | 60     |      |     | dB            |
| Error, % of Full Scale   | $T_A = 25^\circ C$ , $I_{IN} = 1nA$ to 1mA           |        | .20  | 0.5  |        | .25  | 1.0 | %             |
| Error, % of Full Scale   | $T_A = 0^\circ C$ to +70°C,<br>$I_{IN} = 1nA$ to 1mA |        | .60  | 1.25 |        | .80  | 2.5 | %             |
| Error, Absolute Value  | $T_A = 25^\circ C$ , $I_{IN} = 1nA$ to 1mA           |        | 12   | 30   |        | 14   | 60  | mV            |
| Error, Absolute Value  | $T_A = 0^\circ C$ to +70°C<br>$I_{IN} = 1nA$ to 1mA  |        | 36   | 75   |        | 50   | 150 | mV            |
| Temperature Coefficient of $V_{OUT}$                           | $I_{IN} = 1nA$ to 1mA                                |        | 0.8  |      |        | 0.8  |     | mV/°C         |
| Power Supply Rejection Ratio                                   | Referred to Output                                   |        | 2.5  |      |        | 2.5  |     | mV/V          |
| Offset Voltage ( $A_1$ & $A_2$ )                               | Before Nulling                                       |        | 15   | 25   |        | 15   | 50  | mV            |
| Wideband Noise   | At Output, for $I_{IN} = 100\mu A$                   |        | 250  |      |        | 250  |     | $\mu V$ (RMS) |
| Output Voltage Swing   | $R_L = 10k\Omega$                                    | ± 12   | ± 14 |      | ± 12   | ± 14 |     | V             |
|  | $R_L = 2k\Omega$                                     | ± 10   | ± 13 |      | ± 10   | ± 13 |     | V             |
| Power Consumption  |  |        | 150  | 200  |        | 150  | 200 | mW            |
| Supply Current   |  |        | 5    | 6.7  |        | 5    | 6.7 | mA            |

NOTE: All typical values have been characterized but are not tested.



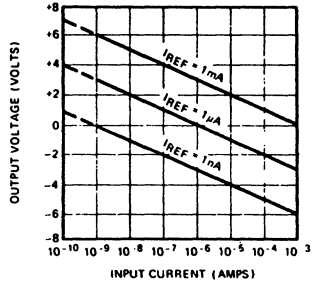
## TYPICAL PERFORMANCE CHARACTERISTICS

TRANSFER FUNCTION FOR VOLTAGE INPUTS



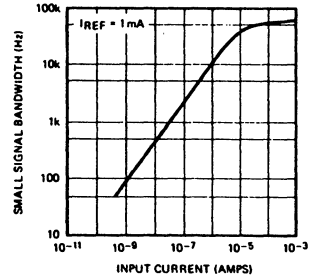
0313-5

TRANSFER FUNCTION FOR CURRENT INPUTS



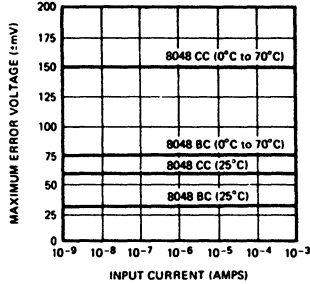
0313-6

SMALL SIGNAL BANDWIDTH AS A FUNCTION OF INPUT CURRENT



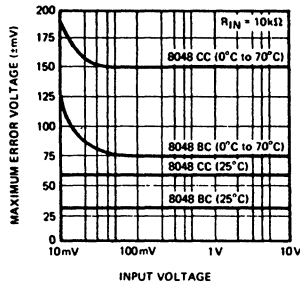
0313-7

MAXIMUM ERROR VOLTAGE AT THE OUTPUT AS A FUNCTION OF INPUT CURRENT



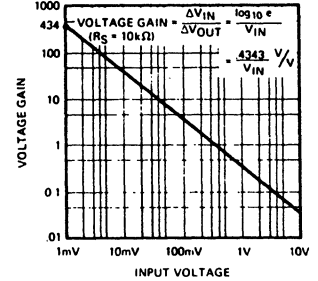
0313-8

MAXIMUM ERROR VOLTAGE AT THE OUTPUT AS A FUNCTION OF INPUT VOLTAGE



0313-9

SMALL SIGNAL VOLTAGE GAIN AS A FUNCTION OF INPUT VOLTAGE FOR  $R_S = 10\text{k}\Omega$



0313-10

NOTE: All typical values have been characterized but are not tested.

# ICL8048/ICL8049

## ABSOLUTE MAXIMUM RATINGS (ICL8049)

|                                       |       |
|---------------------------------------|-------|
| Supply Voltage                        | ±18V  |
| $V_{IN}$ (Input Voltage)              | ±15V  |
| $I_{REF}$ (Reference Current)         | 2mA   |
| Voltage between Offset Null and $V^+$ | ±0.5V |
| Power Dissipation                     | 750mW |

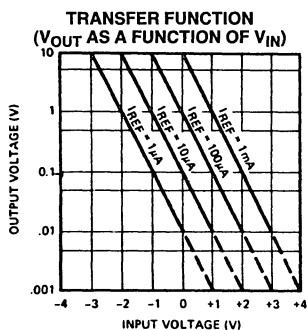
|                                     |                 |
|-------------------------------------|-----------------|
| Operating Temperature Range         | 0°C to +70°C    |
| Output Short Circuit Duration       | Indefinite      |
| Storage Temperature Range           | -65°C to +150°C |
| Lead Temperature (Soldering, 10sec) | 300°C           |

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS (ICL8049) $V_S = \pm 15V, T_A = 25^\circ C, I_{REF} = 1mA$ , scale factor adjusted for 1 decade (out) per volt (in), unless otherwise specified.

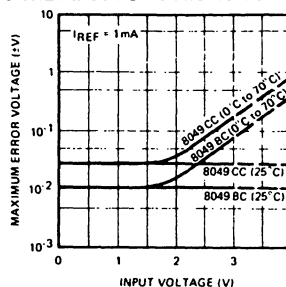
| Parameter                                     | Test Conditions  | 8049BC |      |     | 8049CC |      |     | Units        |
|---|--|--------|------|-----|--------|------|-----|--------------|
|   |  | Min    | Typ  | Max | Min    | Typ  | Max |              |
| Dynamic Range ( $V_{OUT}$ )                   | $V_{OUT} = 10mV$ to $10V$                                  | 60     |      |     | 60     |      |     | dB           |
| Error, Absolute Value                         | $T_A = 25^\circ C, 0V \leq V_{IN} \leq 2V$                 |        | 3    | 15  |        | 5    | 25  | mV           |
| Error, Absolute Value                         | $T_A = 0^\circ C$ to $+70^\circ C, 0V \leq V_{IN} \leq 3V$ |        | 20   | 75  |        | 30   | 150 | mV           |
| Temperature Coefficient, Referred to $V_{IN}$ | $V_{IN} = 3V$  |        | 0.38 |     |        | 0.55 |     | mV/°C        |
| Power Supply Rejection Ratio                  | Referred to Input, for $V_{IN} = 0V$                       |        | 2.0  |     |        | 2.0  |     | $\mu V/V$    |
| Offset Voltage ( $A_1$ & $A_2$ )              | Before Nulling   |        | 15   | 25  |        | 15   | 50  | mV           |
| Wideband Noise                                | Referred to Input, for $V_{IN} = 0V$                       |        | 26   |     |        | 26   |     | $\mu V(RMS)$ |
| Output Voltage Swing                          | $R_L = 10k\Omega$  | ±12    | ±14  |     | ±12    | ±14  |     | V            |
|   | $R_L = 2k\Omega$   | ±10    | ±13  |     | ±10    | ±13  |     | V            |
| Power Consumption                             |  |        | 150  | 200 |        | 150  | 200 | mW           |
| Supply Current                                |  |        | 5    | 6.7 |        | 5    | 6.7 | mA           |

## TYPICAL PERFORMANCE CHARACTERISTICS



0313-11

## MAXIMUM ERROR VOLTAGE REFERRED TO THE INPUT AS A FUNCTION OF $V_{IN}$



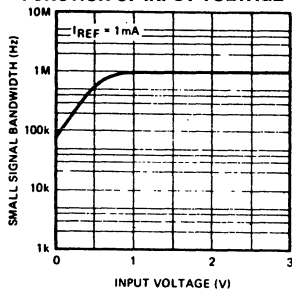
0313-12

NOTE: All typical values have been characterized but are not tested.

8  
SPECIAL  
ANALOG CIRCUITS

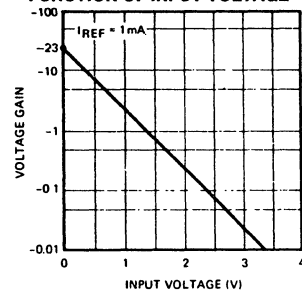
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

SMALL SIGNAL BANDWIDTH AS A FUNCTION OF INPUT VOLTAGE



0313-13

SMALL SIGNAL VOLTAGE GAIN AS A FUNCTION OF INPUT VOLTAGE



0313-14

### ICL8048 DETAILED DESCRIPTION

The ICL8048 relies for its operation on the well-known exponential relationship between the collector current and the base-emitter voltage of a transistor:

$$I_C = I_S [e^{qV_{BE}/kT} - 1] \quad (1)$$

For base-emitter voltages greater than 100mV, Eq. (1) becomes

$$I_C = I_S e^{qV_{BE}/kT} \quad (2)$$

From Eq. (2), it can be shown that for two identical transistors operating at different collector currents, the  $V_{BE}$  difference ( $\Delta V_{BE}$ ) is given by:

$$\Delta V_{BE} = -2.303 \times \frac{kT}{q} \log_{10} \left[ \frac{I_{C1}}{I_{C2}} \right] \quad (3)$$

Referring to Figure 3, it is clear that the potential at the collector of  $Q_2$  is equal to the  $\Delta V_{BE}$  between  $Q_1$  and  $Q_2$ . The output voltage is  $\Delta V_{BE}$  multiplied by the gain of  $A_2$ :

$$V_{OUT} = -2.303 \left( \frac{R_1 + R_2}{R_2} \right) \left( \frac{kT}{q} \right) \log_{10} \left[ \frac{I_{IN}}{I_{REF}} \right] \quad (4)$$

The expression  $2.303 \times \frac{kT}{q}$  has a numerical value of 59mV at 25°C; thus in order to generate 1 volt/decade at the output, the ratio  $(R_1 + R_2)/R_2$  is chosen to be 16.9. For this scale factor to hold constant as a function of temperature, the  $(R_1 + R_2)/R_2$  term must have a  $1/T$  characteristic to compensate for  $kT/q$ .

In the ICL8048 this is achieved by making  $R_1$  a thin film resistor, deposited on the monolithic chip. It has a nominal value of 15.9k $\Omega$  at 25°C, and its temperature coefficient is carefully designed to provide the necessary compensation.

Resistor  $R_2$  is external and should be a low T.C. type; it should have a nominal value of 1k $\Omega$  to provide 1 volt/decade, and must have an adjustment range of  $\pm 20\%$  to allow for production variations in the absolute value of  $R_1$ .

### ICL8048 OFFSET AND SCALE FACTOR ADJUSTMENT

A log amp, unlike an op-amp, cannot be offset adjusted by simply grounding the input. This is because the log of zero approaches minus infinity; reducing the input current to zero starves  $Q_1$  of collector current and opens the feedback loop around  $A_1$ . Instead, it is necessary to zero the offset voltage of  $A_1$  and  $A_2$  separately, and then to adjust the scale factor. Referring to Figure 3, this is done as follows:

- 1) Temporarily connect a 10k $\Omega$  resistor ( $R_0$ ) between pins 2 and 7. With no input voltage, adjust  $R_4$  until the output of  $A_1$  (pin 7) is zero. Remove  $R_0$ .  
Note that for a current input, this adjustment is not necessary since the offset voltage of  $A_1$  does not cause any error for current-source inputs.
- 2) Set  $I_{IN} = I_{REF} = 1\text{mA}$ . Adjust  $R_5$  such that the output of  $A_2$  (pin 10) is zero.
- 3) Set  $I_{IN} = 1\mu\text{A}$ ,  $I_{REF} = 1\text{mA}$ . Adjust  $R_2$  for  $V_{OUT} = 3$  volts (for a 1 volt/decade scale factor) or 6 volts (for a 2 volt/decade scale factor).

Step #3 determines the scale factor. Setting  $I_{IN} = 1\mu\text{A}$  optimizes the scale factor adjustment over a fairly wide dynamic range, from 1mA to 1nA. Clearly, if the 8048 is to be used for inputs which only span the range 100 $\mu\text{A}$  to 1mA, it would be better to set  $I_{IN} = 100\mu\text{A}$  in Step #3. Similarly, adjustment for other scale factors would require different  $I_{IN}$  and  $V_{OUT}$  values.

# ICL8048/ICL8049

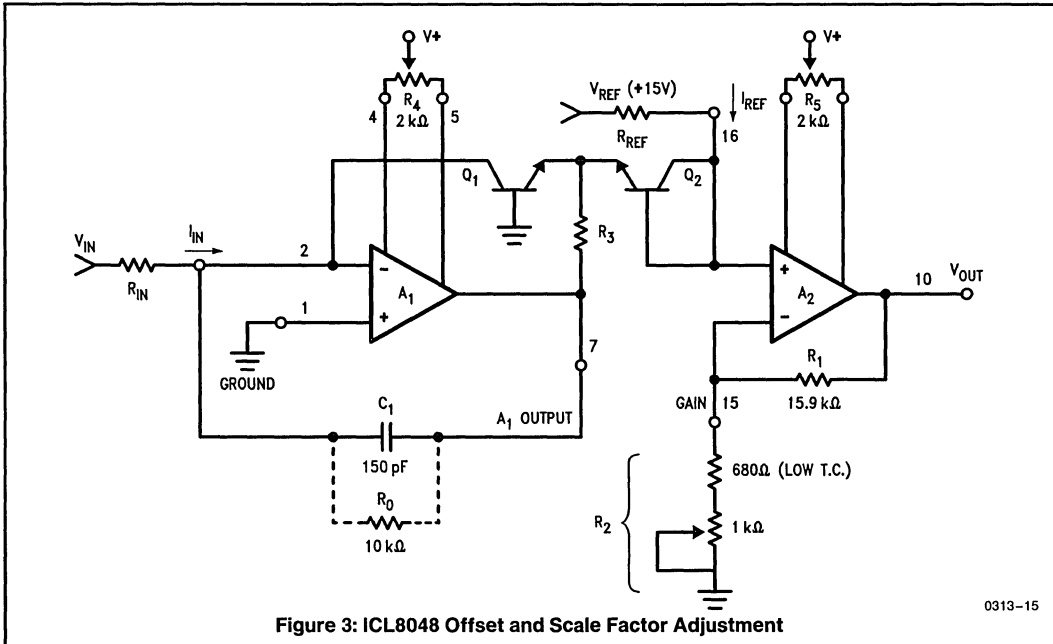


Figure 3: ICL8048 Offset and Scale Factor Adjustment

0313-15

## ICL8049 DETAILED DESCRIPTION

The ICL8049 relies on the same logarithmic properties of the transistor as the ICL8048. The input voltage forces a specific  $\Delta V_{BE}$  between  $Q_1$  and  $Q_2$  (Figure 4). This  $V_{BE}$  difference is converted into a difference of collector currents by the transistor pair. The equation governing the behavior of the transistor pair is derived from (2) on the previous page and is as follows:

$$\frac{I_{C1}}{I_{C2}} = \exp \left[ \frac{q \Delta V_{BE}}{kT} \right]$$

When numerical values for  $q/kT$  are put into this equation, it is found that a  $\Delta V_{BE}$  of 59mV (at 25°C) is required to change the collector current ratio by a factor of ten. But for ease of application, it is desirable that a 1 volt change at the input generate a tenfold change at the output. The required input attenuation is achieved by the network comprising  $R_1$  and  $R_2$ . In order that scale factors other than one decade per volt may be selected,  $R_2$  is external to the chip. It should have a value of 1kΩ, adjustable  $\pm 20\%$ , for one decade per volt.  $R_1$  is a thin film resistor deposited on the monolithic chip; its temperature characteristics are chosen to compensate the temperature dependence of equation 5, as explained on the previous page.

The overall transfer function is as follows:

$$\frac{I_{OUT}}{I_{REF}} = \exp \left[ \frac{-R_2}{(R_1 + R_2)} \times \frac{qV_{IN}}{kT} \right] \quad (6)$$

Substituting  $V_{OUT} = I_{OUT} \times R_{OUT}$  gives:

$$V_{OUT} = R_{OUT} I_{REF} \exp \left[ \frac{-R_2}{(R_1 + R_2)} \times \frac{qV_{IN}}{kT} \right] \quad (7)$$

For voltage references equation 7 becomes

$$V_{OUT} = V_{REF} \times \frac{R_{OUT}}{R_{REF}} \exp \left[ \frac{-R_2}{(R_1 + R_2)} \times \frac{qV_{IN}}{kT} \right] \quad (8)$$

## ICL8049 OFFSET AND SCALE FACTOR ADJUSTMENT

As with the log amplifier, the antilog amplifier requires three adjustments. The first step is to null out the offset voltage of  $A_2$ . This is accomplished by reverse biasing the base-emitter of  $Q_2$ .  $A_2$  then operates as a unity gain buffer with a grounded input. The second step forces  $V_{IN} = 0$ ; the output is adjusted for  $V_{OUT} = 10V$ . This step essentially "anchors" one point on the transfer function. The third step applies a specific input and adjusts the output to the correct voltage. This sets the scale factor. Referring to Figure 4, the exact procedure for 1 decade/volt is as follows:

- 1) Connect the input (pin #16) to +15V. This reverse biases the base-emitter of  $Q_2$ . Adjust  $R_7$  for  $V_{OUT} = 0V$ . Disconnect the input from +15V.
- 2) Connect the input to Ground. Adjust  $R_4$  for  $V_{OUT} = 10V$ . Disconnect the input from Ground.
- 3) Connect the input to a precise 2V supply and adjust  $R_2$  for  $V_{OUT} = 100mV$ .

The procedure outlined above optimizes the performance over a 3 decade range at the output (i.e.,  $V_{OUT}$  from 10mV to 10V). For a more limited range of output voltages, for example 1V to 10V, it would be better to use a precise 1 volt supply and adjust for  $V_{OUT} = 1V$ . For other scale factors and/or starting points, different values for  $R_2$  and  $R_{REF}$  will be needed, but the same basic procedure applies.

NOTE: All typical values have been characterized but are not tested.

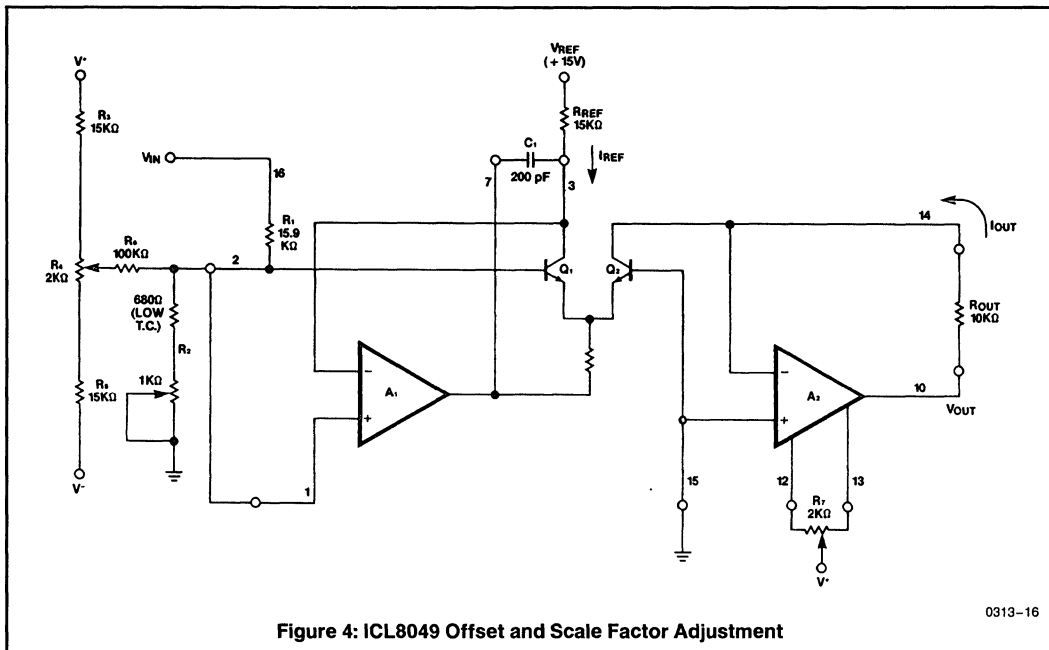


Figure 4: ICL8049 Offset and Scale Factor Adjustment

0313-16

## APPLICATIONS INFORMATION

### ICL8048 Scale Factor Adjustment

The scale factor adjustment procedures outlined previously for the ICL8048 and ICL8049, are primarily directed towards setting up 1 volt ( $\Delta V_{OUT}$ ) per decade ( $\Delta I_{IN}$  or  $\Delta V_{IN}$ ) for the log amp, or one decade ( $\Delta V_{OUT}$ ) per volt ( $\Delta V_{IN}$ ) for the antilog amp.

This corresponds to  $K=1$  in the respective transfer functions:

$$\text{Log Amp: } V_{OUT} = -K \log_{10} \left[ \frac{I_{IN}}{I_{REF}} \right] \quad (9)$$

$$\text{Antilog Amp: } V_{OUT} = R_{OUT} I_{REF} 10^{\frac{-V_{IN}}{K}} \quad (10)$$

By adjusting  $R_2$  (Figure 3 and Figure 4) the scale factor "K" in equation 9 and 10 can be varied. The effect of changing K is shown graphically in Figure 5 for the log amp, and Figure 6 for the antilog amp. The nominal value of  $R_2$  required to give a specific value of K can be determined from equation 11. It should be remembered that  $R_1$  has a  $\pm 20\%$  tolerance in absolute value, so that allowance shall be made for adjusting the nominal value of  $R_2$  by  $\pm 20\%$ .

$$R_2 = \frac{941}{(K - .059)} \Omega \quad (11)$$

### ICL8048 Automatic Offset Nulling Circuit

The ICL8048 is fundamentally a logarithmic current amplifier. It can be made to act as a voltage amplifier by placing a

resistor between the current input and the voltage source but, since  $I_{IN} = (V_{IN} - V_{OFFSET})/R_{IN}$ , this conversion is accurate only when  $V_{IN}$  is much greater than the offset voltage. A substantial reduction of  $V_{OFFSET}$  would allow voltage operation over a 120 dB range.

Figure 101 shows the ICL8048 in an automatic offset nulling configuration using the ICL7650S. The extremely low offset voltage of the ICL7650S forces its non-inverting input (and thus pin 2 of the ICL8048) to the same potential as its inverting input by nulling the first stage of the log amp. Since  $V_{OFFSET}$  is now within a few microvolts of ground potential,  $R_{IN}$  can perform its voltage to current conversion much more accurately, and without an offset trimmer pot. Step 1 of the offset and scale factor adjustment is eliminated, simplifying calibration.

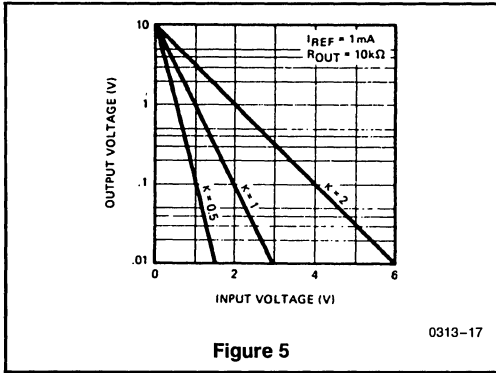
**NOTE:** The ICL7650S op amp has a maximum supply voltage of  $\pm 8$  volts. The ICL8048 will operate at this voltage, but  $I_{REF}$  must be limited to 200 microamps or less for proper calibration and operation. Best performance will be achieved when the ICL7650S has a  $\pm 3-8V$  supply and the ICL8048 is at its recommended  $\pm 15V$  supply. See A053 for a method of powering the ICL7650S from a  $\pm 15V$  source.

### Frequency Compensation

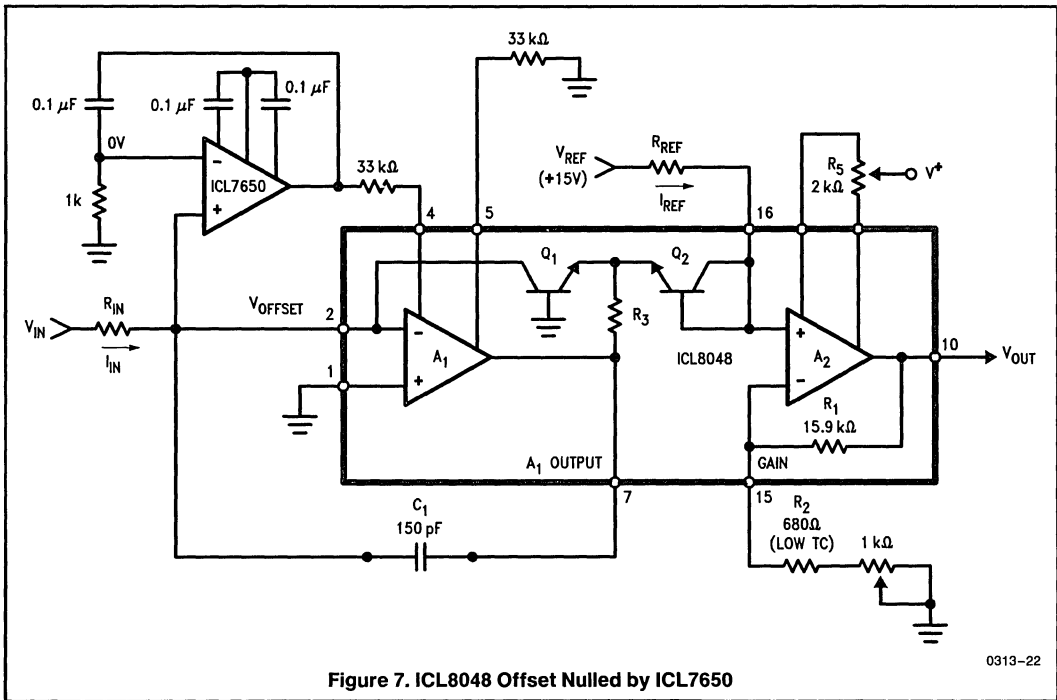
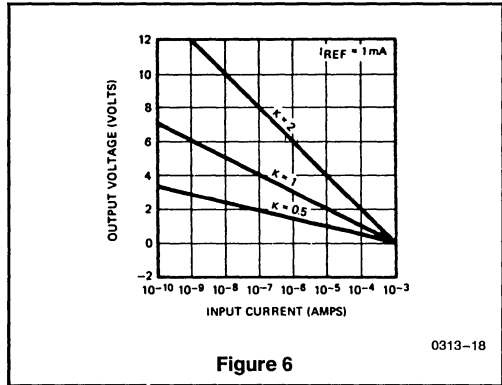
Although the op-amps in both the ICL8048 and the ICL8049 are compensated for unity gain, some additional frequency compensation is required. This is because the log transistors in the feedback loop add to the loop gain. In the 8048, 150pF should be connected between Pins 2 and 7 (Figure 3). In the 8049, 200pF between Pins 3 and 7 is recommended (Figure 4).

# ICL8048/ICL8049

EFFECT OF VARYING "K" ON THE ANTILOG AMPLIFIER



EFFECT OF VARYING "K" ON THE LOG AMPLIFIER



## Error Analysis

Performing a meaningful error analysis of a circuit containing log and antilog amplifiers is more complex than dealing with a similar circuit involving only op-amps. In this data sheet every effort has been made to simplify the analysis task, without in any way compromising the validity of the resultant numbers.

The key difference in making error calculations in log/antilog amps, compared with op-amps, is that the gain of the former is a function of the input signal level. Thus, it is nec-

essary, when referring errors from output to input, or vice versa, to check the input voltage level, then determine the gain of the circuit by referring to the graphs given in the Typical Performance Characteristics section.

The various error terms in the log amplifier, the ICL8048, are Referred To the Output (RTO) of the device. The error terms in the antilog amplifier, the ICL8049, are Referred To the Input (RTI) of the device. The errors are expressed in this way because in the majority of systems a number of log amps interface with an antilog amp, as shown in Figure 8.

NOTE: All typical values have been characterized but are not tested.

# ICL8048/ICL8049

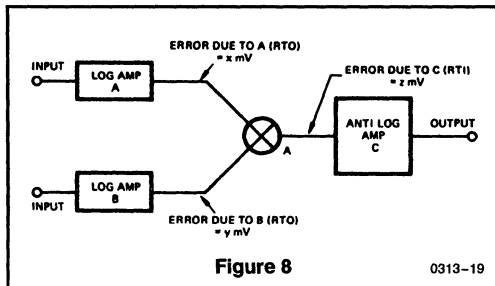


Figure 8

0313-19

It is very straightforward to estimate the system error at node (A) by taking the square root of the sum-of-the-squares of the errors of each contributing block.

$$\text{Total Error} = \sqrt{x^2 + y^2 + z^2} \text{ at (A)}$$

If required, this error can be referred to the system output through the voltage gain of the antilog circuit, using the voltage gain versus input voltage plot.

The numerical values of x, y, and z in the above equation are obtained from the maximum error voltage plots. For example, with the ICL8048BC, the maximum error at the output is 30mV at 25°C. This means that the measured output will be within 30mV of the theoretical transfer function, provided the unit has been adjusted per the procedures described previously. Figure 9 illustrates this point.

To determine the maximum error over the operating temperature range, the 0 to 70°C absolute error values given in the table of electrical characteristics should be used. For intermediate temperatures, assume a linear increase in the error between the 25°C value and the 70°C value.

For the antilog amplifier, the only difference is that the error refers to the input, i.e., the horizontal axis. It will be noticed that the maximum error voltage of the ICL8049, over the temperature range, is strongly dependent on the input voltage. This is because the output amplifier, A<sub>2</sub>, has an offset voltage drift which is directly transmitted to the output. When this error is referred to the input, it must be divided by the voltage gain, which is input voltage dependent. At V<sub>IN</sub> = 3V, for example, errors at the output are multiplied by 1/.023 (= 43.5) when referred to the input.

## TRANSFER FUNCTION FOR CURRENT INPUTS

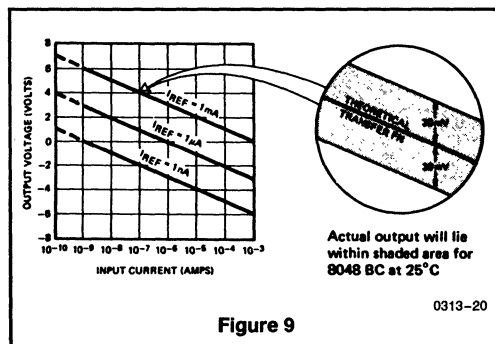


Figure 9

0313-20

It is important to note that both the ICL8048 and the ICL8049 require positive values of I<sub>REF</sub>, and the input (ICL8048) or output (ICL8049) currents (or voltages) respectively must also be positive. Application of negative I<sub>IN</sub> to the ICL8048 or negative I<sub>REF</sub> to either circuit will cause malfunction, and if maintained for long periods, would lead to device degradation. Some protection can be provided by placing a diode between pin 7 and ground.

## SETTING UP THE REFERENCE CURRENT

In both the ICL8048 and the ICL8049 the input current reference pin (I<sub>REF</sub>) is not a true virtual ground. For the ICL8048, a fraction of the output voltage is seen on Pin 16 (Figure 3). This does not constitute an appreciable error provided V<sub>REF</sub> is much greater than this voltage. A 10V or 15V reference satisfies this condition. For the ICL8049, a fraction of the input voltage appears on Pin 3 (Figure 4), placing a similar restraint on the value of V<sub>REF</sub>.

Alternatively, I<sub>REF</sub> can be provided from a true current source. One method of implementing such a current source is shown in Figure 10.

## LOG OF RATIO CIRCUIT, DIVISION

The 8048 may be used to generate the log of a ratio by modulating the I<sub>REF</sub> input. The transfer function remains the same, as defined by equation 9:

$$V_{OUT} = -K \log_{10} \left[ \frac{I_{IN}}{I_{REF}} \right] \quad (9)$$

Clearly it is possible to perform division using just one ICL8048, followed by an ICL8049. For multiplication, it is generally necessary to use two log amps, summing their outputs into an antilog amp.

To avoid the problems caused by the I<sub>REF</sub> input not being a true virtual ground (discussed in the previous section), the circuit of Figure 10 is again recommended if the I<sub>REF</sub> input is to be modulated.

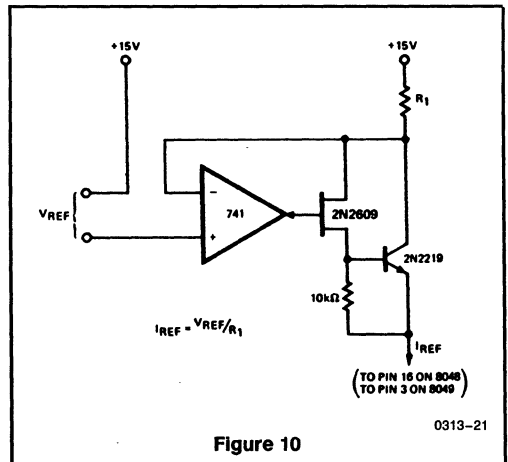


Figure 10

0313-21

# ICL8048/ICL8049

## DEFINITION OF TERMS

In the definitions which follow, it will be noted that the various error terms are referred to the output of the log amp, and to the input of the antilog amp. The reason for this is explained on the previous page.

**DYNAMIC RANGE** The dynamic range of the ICL8048 refers to the range of input voltages or currents over which the device is guaranteed to operate. For the ICL8049 the dynamic range refers to the range of output voltage over which the device is guaranteed to operate.

**ERROR, ABSOLUTE VALUE** The absolute error is a measure of the deviation from the theoretical transfer function, after performing the offset and scale factor adjustments as outlined, (ICL8048) or (ICL8049). It is expressed in mV and referred to the linear axis of the transfer function plot. Thus, in the case of the ICL8048, it is a measure of the deviation from the theoretical output voltage for a given input current or voltage. For the ICL8049 it is a measure of the deviation from the theoretical input voltage required to generate a specific output voltage.

The absolute error specification is guaranteed over the dynamic range.

**ERROR, % OF FULL SCALE** The error as a percentage of full scale can be obtained from the following relationship:

$$\text{Error, \% of Full Scale} = \frac{100 \times \text{Error, absolute value}}{\text{Full Scale Output Voltage}}$$

**TEMPERATURE COEFFICIENT OF  $V_{OUT}$  OR  $V_{IN}$**  For the ICL8048 the temperature coefficient refers to the drift with temperature of  $V_{OUT}$  for a constant input current.

For the ICL8049 it is the temperature drift of the input voltage required to hold a constant value of  $V_{OUT}$ .

**POWER SUPPLY REJECTION RATIO** The ratio of the voltage change in the linear axis of the transfer function ( $V_{OUT}$  for the ICL8048,  $V_{IN}$  for the ICL8049) to the change in the supply voltage, assuming that the log axis is held constant.

**WIDEBAND NOISE** For the ICL8048, this is the noise occurring at the output under the specified conditions. In the case of the ICL8049, the noise is referred to the input.

**SCALE FACTOR** For the log amp, the scale factor (K) is the voltage change at the output for a decade (i. e. 10:1) change at the input. For the antilog amp, the scale factor is the voltage change required at the input to cause a one decade change at the output. See equations 9 and 10.

## APPLICATION NOTES

For further applications assistance, see

**A007** "The ICL8048/8049 Monolithic Log-Antilog Amplifiers"



### GENERAL DESCRIPTION

The ICM7242 is a CMOS timer/counter circuit consisting of an RC oscillator followed by an 8-bit binary counter. It will replace the 2242 in most applications, with a significant reduction in the number of external components.

Three outputs are provided. They are the oscillator output, and buffered outputs from the first and eighth counters.

### ORDERING INFORMATION

| Part Number | Temperature Range | Package        |
|-------------|-------------------|----------------|
| ICM7242IPA  | -25°C to +85°C    | 8 pin MINI-DIP |
| ICM7242CBA  | 0°C to +70°C      | 8 pin S.O.I.C. |

### FEATURES

- Replaces The 2242 in Most Applications
- Timing From Microseconds to Days
- Cascadeable
- Monostable or Astable Operation
- Wide Supply Voltage Range: 2 - 16 volts
- Low Supply Current: 115 $\mu$ A @ 5 volts

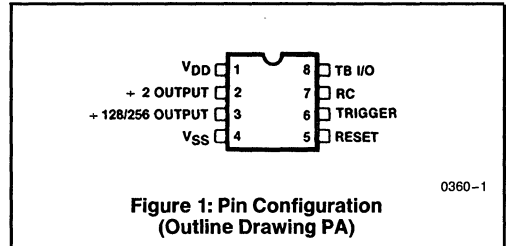
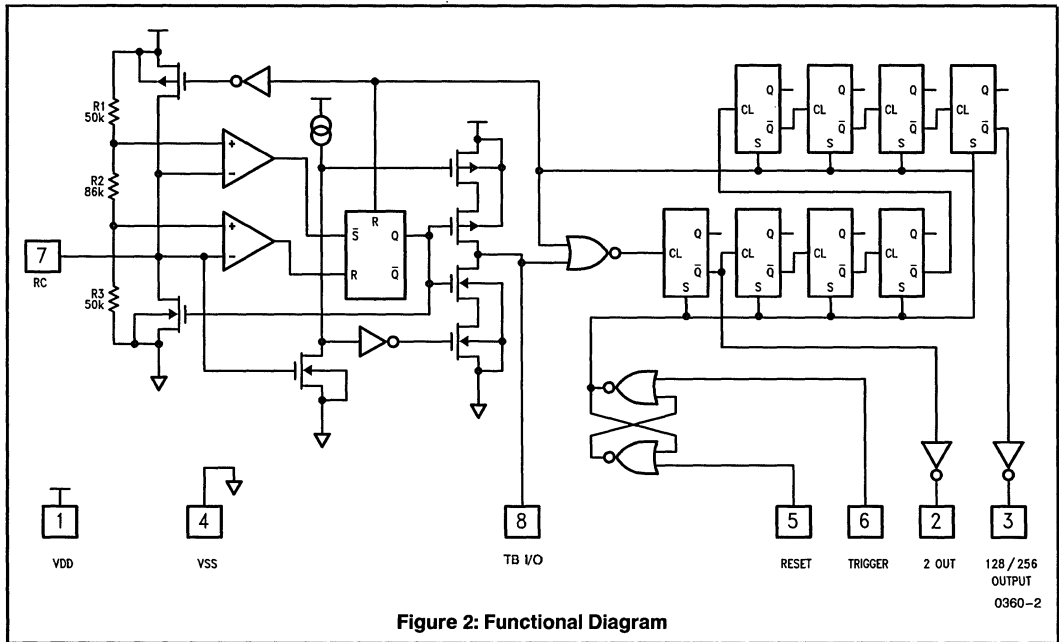


Figure 1: Pin Configuration (Outline Drawing PA)



# ICM7242

## ABSOLUTE MAXIMUM RATINGS

|  |                 |
|--|-----------------|
| Supply Voltage ( $V_{DD}$ to $V_{SS}$ )                                    | 18V             |
| Input Voltage <sup>[1]</sup>   |                 |
| Terminals (Pins 5, 6, 7, 8) ... ( $V_{SS} - 0.3V$ ) to ( $V_{DD} + 0.3V$ ) |                 |
| Maximum continuous output current (each output)                            | 50mA            |
| Power Dissipation <sup>[2]</sup>   | 200mW           |
| Operating Temperature Range  |                 |
| ICM7242I   | -25°C to +85°C  |
| ICM7242C   | 0°C to +70°C    |
| Storage Temperature Range  | -65°C to +150°C |
| Lead Temperature (Soldering, 10sec)  | 300°C           |

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**NOTES:** 1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than  $V_{DD}$  or less than  $V_{SS}$  may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same supply be applied to the device before its supply is established and, that in multiple supply systems, the supply to the ICM7242 be turned on first.  
2. Derate at -2mW/°C above 25°C.

## ELECTRICAL CHARACTERISTICS

( $V_{DD}=5V$ ,  $T_A = +25^\circ C$ ,  $R = 10k\Omega$ ,  $C = 0.1\mu F$ ,  $V_{SS} = 0V$  unless otherwise specified.)

| Symbol                    | Parameter                                 | Test Conditions  | Min | Typ                      | Max        | Units                                    |
|---------------------------|---|--|-----|--------------------------|------------|--|
| $V_{DD}$                  | Guaranteed Supply Voltage                 |  | 2   |                          | 16         | V  |
| $I_{DD}$                  | Supply Current                            | Reset<br>Operating, $R = 10k\Omega$ , $C = 0.1\mu F$<br>Operating, $R = 1M\Omega$ , $C = 0.1\mu F$<br>TB Inhibited, RC Connected to $V_{SS}$ |     | 125<br>340<br>220<br>225 | 800<br>600 | $\mu A$<br>$\mu A$<br>$\mu A$<br>$\mu A$ |
|                           | Timing Accuracy                           |  |     | 5                        |            | %  |
| $\Delta f/\Delta T$       | RC Oscillator Frequency Temperature Drift | Independent of RC Components   |     | 250                      |            | ppm/°C                                   |
| $V_{OTB}$                 | Time Base Output Voltage                  | $I_{SOURCE} = 100\mu A$<br>$I_{SINK} = 1.0mA$  |     | 3.5<br>0.40              |            | V<br>V                                   |
| $I_{TBLK}$                | Time Base Output Leakage Current          | RC = Ground  |     |                          | 25         | $\mu A$                                  |
| $V_{TRIG}$                | Trigger Input Voltage                     | $V_{DD} = 5V$<br>$V_{DD} = 15V$  |     | 1.6<br>3.5               | 2.0<br>4.5 | V<br>V                                   |
| $V_{RST}$                 | Reset Input Voltage                       | $V_{DD} = 5V$<br>$V_{DD} = 15V$  |     | 1.3<br>2.7               | 2.0<br>4.0 | V<br>V                                   |
| $I_{TRIG}$ ,<br>$I_{RST}$ | Trigger/Reset Input Current               |  |     | 10                       |            | $\mu A$                                  |
| $f_t$                     | Max Count Toggle Rate                     | $V_{DD} = 2V$<br>$V_{DD} = 5V$<br>$V_{DD} = 15V$<br>50% Duty Cycle Input with Peak to Peak Voltages Equal to $V_{DD}$ and $V_{SS}$           | 2   | 1<br>6<br>13             |            | MHz<br>MHz<br>MHz                        |
| $V_{SAT}$                 | Output Saturation Voltage                 | All Outputs except TB Output<br>$V_{DD} = 5V$ , $I_{OUT} = 3.2mA$  |     | 0.22                     | 0.4        | V  |
| $I_{SOURCE}$              | Output Sourcing Current 7242              | $V_{DD} = 5V$<br>Terminals 2 & 3, $V_{OUT} = 1V$   |     | 300                      |            | $\mu A$                                  |
| $C_t$                     | MIN Timing Capacitor (Note 1)             |  | 10  |                          |            | pF                                       |
| $R_t$                     | Timing Resistor Range (Note 1)            | $V_{DD} = 2-16V$   | 1K  |                          | 22M        | $\Omega$                                 |

**NOTE:** 1. For Design only, not tested.

*NOTE: All typical values have been characterized but are not tested.*

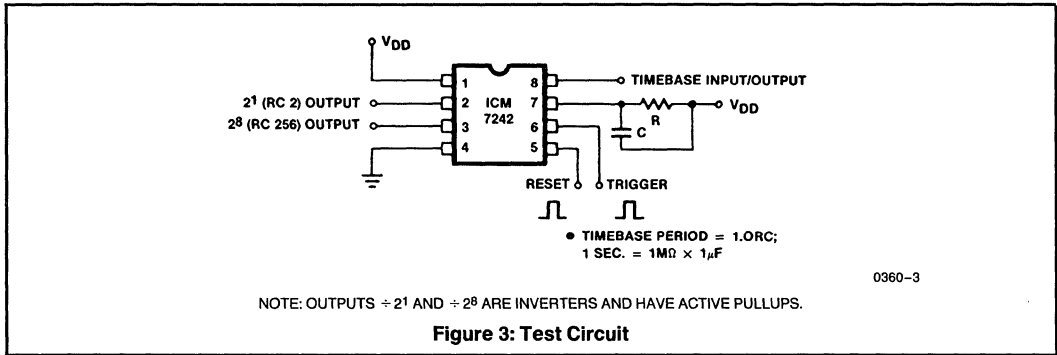
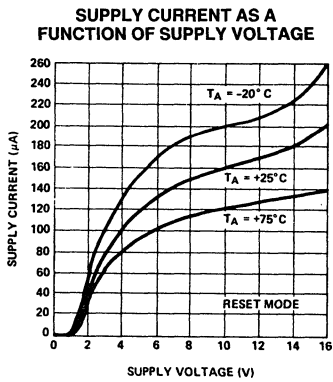


Figure 3: Test Circuit

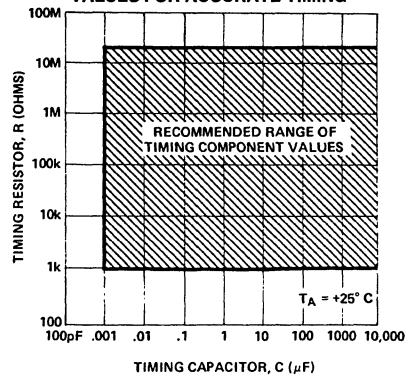
0360-3

## TYPICAL PERFORMANCE CHARACTERISTICS



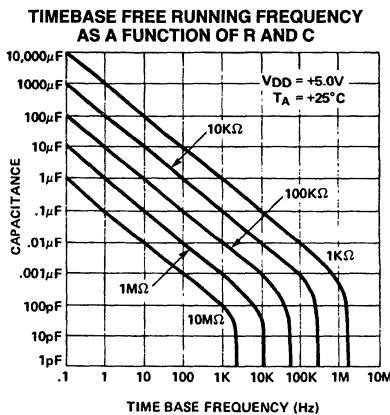
0360-4

### RECOMMENDED RANGE OF TIMING COMPONENT VALUES FOR ACCURATE TIMING



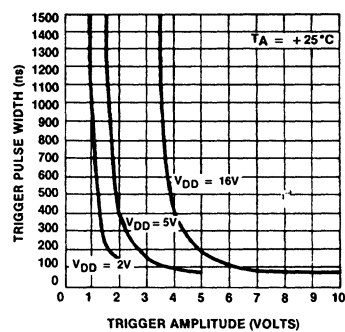
DIMENSIONS IN INCHES AND MILLIMETERS

0360-5



0360-6

### MINIMUM TRIGGER PULSE WIDTH AS A FUNCTION OF TRIGGER AMPLITUDE

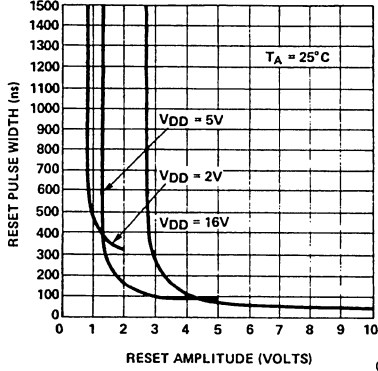


0360-7

NOTE: All typical values have been characterized but are not tested.

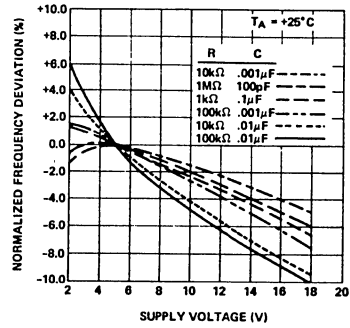
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

MINIMUM RESET PULSE WIDTH AS A FUNCTION OF RESET AMPLITUDE



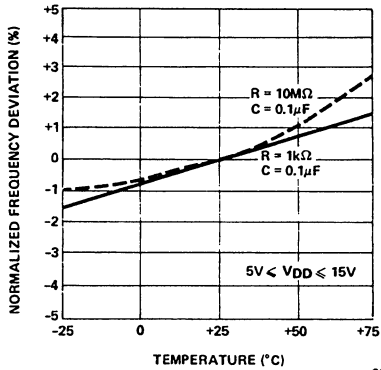
0360-8

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



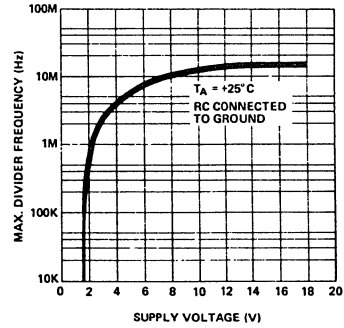
0360-9

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



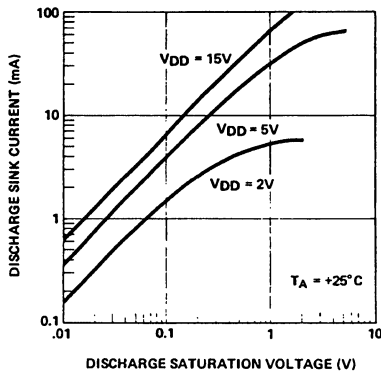
0360-10

MAXIMUM DIVIDER FREQUENCY vs. SUPPLY VOLTAGE



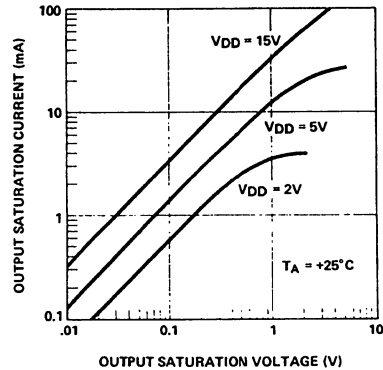
0360-11

DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



0360-12

OUTPUT SATURATION CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE



0360-13

NOTE: All typical values have been characterized but are not tested.

# ICM7242

## OPERATING CONSIDERATIONS

Shorting the RC terminal or output terminals to  $V_{DD}$  may exceed dissipation ratings and/or maximum DC current limits (especially at high supply voltages).

There is a limitation of 50pF maximum loading on the TB I/O terminal if the timebase is being used to drive the counter section. If higher value loading is used, the counter sections may miscount.

For greatest accuracy, use timing component values shown in the graph under typical performance characteristics. For highest frequency operation it will be desirable to use very low values for the capacitor; accuracy will decrease for oscillator frequencies in excess of 200KHz.

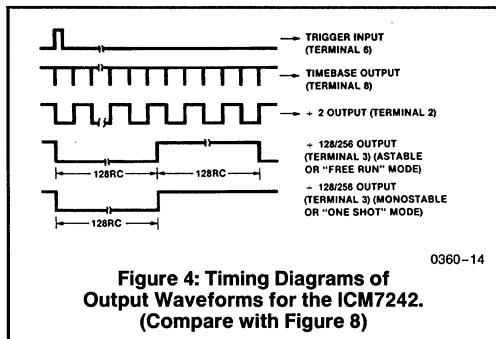
The timing capacitor should be connected between the RC pin and the positive supply rail,  $V_{DD}$ , as shown in Figure 3. When system power is turned off, any charge remaining on the capacitor will be discharged to ground through a large internal diode between the RC node and  $V_{SS}$ . Do NOT reference the timing capacitor to ground, since there is no high-current path in this direction to safely discharge the capacitor when power is turned off. The discharge current from such a configuration could potentially damage the device.

When driving the counter section from an external clock, the optimum drive waveform is a square wave with an amplitude equal to supply voltage. If the clock is a very slow ramp triangular, sine wave, etc., it will be necessary to "square up" the waveform; this can be done by using two CMOS inverters in series, operating from the same supply voltage as the ICM7242.

The ICM7242 is a non-programmable timer whose principal applications will be very low frequency oscillators and long range timers; it makes a much better low frequency oscillator/timer than a 555 or ICM7555, because of the on-chip 8-bit counter. Also, devices can be cascaded to produce extremely low frequency signals.

Because outputs will not be AND'd, output inverters are used instead of open drain N-channel transistors, and the external resistors used for the 2242 will not be required for the ICM7242. The ICM7242 will, however, plug into a socket for the 2242 having these resistors.

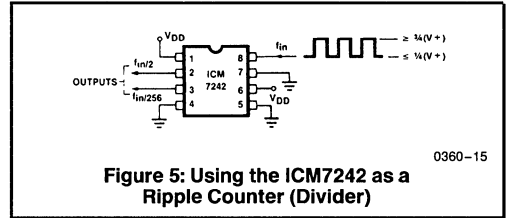
The timing diagram for the ICM7242 is shown in Figure 4. Assuming that the device is in the RESET mode, which occurs on powerup or after a positive signal on the RESET terminal (if TRIGGER is low), a positive edge on the trigger input signal will initiate normal operation. The discharge



**Figure 4: Timing Diagrams of Output Waveforms for the ICM7242. (Compare with Figure 8)**

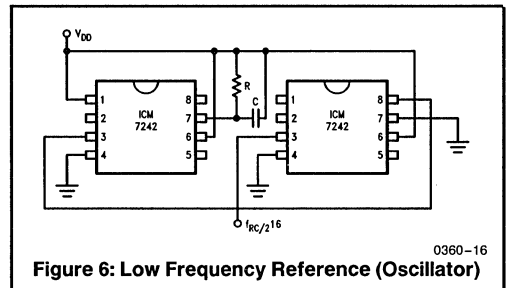
transistor turns on, discharging the timing capacitor C, and all the flip-flops in the counter chain change states. Thus, the outputs on terminals 2 and 3 change from high to low states. After 128 negative timebase edges, the  $\div 2^8$  output returns to the high state.

To use the 8-bit counter without the timebase, terminal 7 (RC) should be connected to ground and the outputs taken from terminals 2 and 3.



**Figure 5: Using the ICM7242 as a Ripple Counter (Divider)**

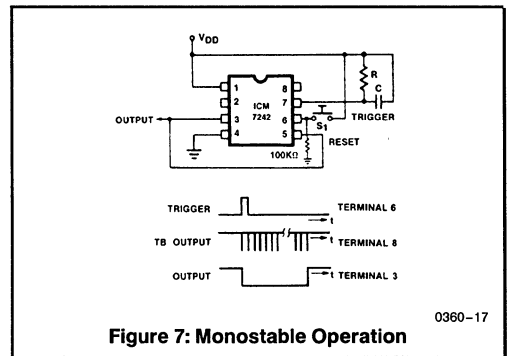
The ICM7242 may be used for a very low frequency square wave reference. For this application the timing components are more convenient than those that would be required by a 555 timer. For very low frequencies, devices may be cascaded (see Figure 6).



**Figure 6: Low Frequency Reference (Oscillator)**

For monostable operation the  $\div 2^8$  output is connected to the RESET terminal. A positive edge on TRIGGER initiates the cycle (NOTE: TRIGGER overrides RESET).

The ICM7242 is superior in all respects to the 2242 except for initial accuracy and oscillator stability. This is primarily due to the fact that high value p- resistors have been used on the ICM7242 to provide the comparator timing points.



**Figure 7: Monostable Operation**

NOTE: All typical values have been characterized but are not tested.

# ICM7242

## COMPARING THE ICM7242 WITH THE 2242

|   | ICM7242        | 2242         |
|---|----------------|--------------|
| a. Operating Voltage                                      | 2 – 16V        | 4 – 15V      |
| b. Operating Temp. Range                                  | –25°C to +85°C | 0°C to +70°C |
| c. Supply Current<br>V <sub>DD</sub> = 5V                 | 0.7mA Max.     | 7mA Max.     |
| d. Pullup Resistors                                       |                |              |
| TB Output   | No             | Yes          |
| ÷2 Output   | No             | Yes          |
| ÷256 Output   | No             | Yes          |
| e. Toggle Rate  | 3.0MHz         | 0.5MHz       |
| f. Resistor to Inhibit Oscillator                         | No             | Yes          |
| g. Resistor in Series with Reset for Monostable Operation | No             | Yes          |
| h. Capacitor TB Terminal for HF Operation                 | No             | Sometimes    |

By selection of R and C, a wide variety of sequence timing can be realized. A typical flow chart for a machine tool controller could be as follows:

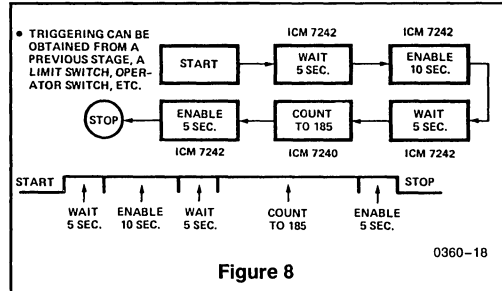


Figure 8

0360-18

By cascading devices, use of low cost CMOS AND/OR gates and appropriate RC delays between stages, numerous sequential control variations can be obtained. Typical applications include injection molding machine controllers, phonograph record production machines, automatic sequencers (no metal contacts or moving parts), milling machine controllers, process timers, automatic lubrication systems, etc.

## SEQUENCE TIMING

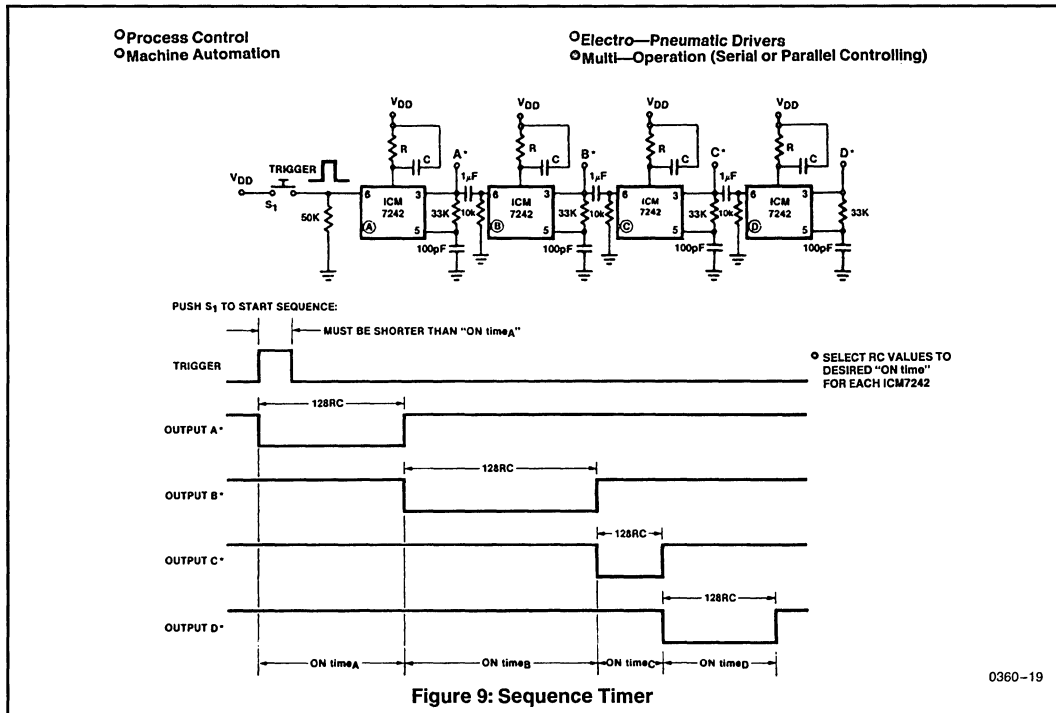


Figure 9: Sequence Timer

0360-19

NOTE: All typical values have been characterized but are not tested.

### GENERAL DESCRIPTION

The ICM7555/6 are CMOS RC timers providing significantly improved performance over the standard SE/NE555/6 and 355 timers, while at the same time being direct replacements for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, TRIGGER and RESET currents, no crowbaring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

Specifically, the ICM7555/6 are stable controllers capable of producing accurate time delays or frequencies. The ICM7556 is a dual ICM7555, with the two timers operating independently of each other, sharing only V<sup>+</sup> and GND. In the one shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the regular bipolar 555/6 devices, the CONTROL VOLTAGE terminal need not be decoupled with a capacitor. The circuits are triggered and reset on falling (negative) waveforms, and the output inverter can source or sink currents large enough to drive TTL loads, or provide minimal offsets to drive CMOS loads.

### ORDERING INFORMATION

| Part Number | Temperature Range | Package             |
|-------------|-------------------|---------------------|
| ICM7555CBA  | 0°C to +70°C      | 8 Lead SOIC         |
| ICM7555IPA  | -25°C to +85°C    | 8 Lead MiniDip      |
| ICM7555ITV  | -25°C to +85°C    | TO-99 Can           |
| ICM7555MTV* | -55°C to +125°C   | TO-99 Can           |
| ICM7556IPD  | -25°C to +85°C    | 14 Lead Plastic DIP |
| ICM7556MJD* | -55°C to +125°C   | 14 Lead CERDIP      |

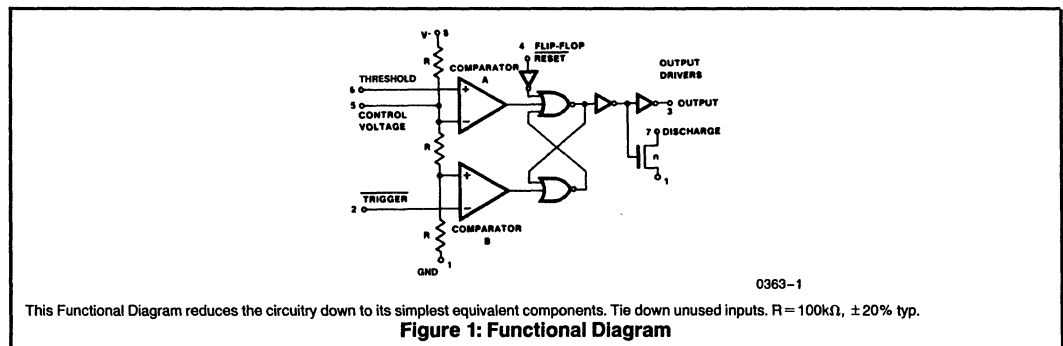
\*Add /883B to part number if 883B processing is desired.

### FEATURES

- Exact Equivalent in Most Cases for SE/NE555/556 or TLC555/556
- Low Supply Current — 60µA Typ. (ICM7555) 120µA Typ. (ICM7556)
- Extremely Low Trigger, Threshold and Reset Currents — 20pA Typical
- High Speed Operation — 1MHz Typical
- Wide Operation Supply Voltage Range Guaranteed 2 to 18 Volts
- Normal Reset Function — No Crowbaring of Supply During Output Transition
- Can Be Used With Higher Impedance Timing Elements Than Regular 555/6 for Longer RC Time Constants
- Timing From Microseconds Through Hours
- Operates in Both Astable and Monostable Modes
- Adjustable Duty Cycle
- High Output Source/Sink Driver Can Drive TTL/CMOS
- Typical Temperature Stability of 0.005% Per °C at 25°C
- Outputs Have Very Low Offsets, HI and LO

### APPLICATIONS

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Missing Pulse Detector

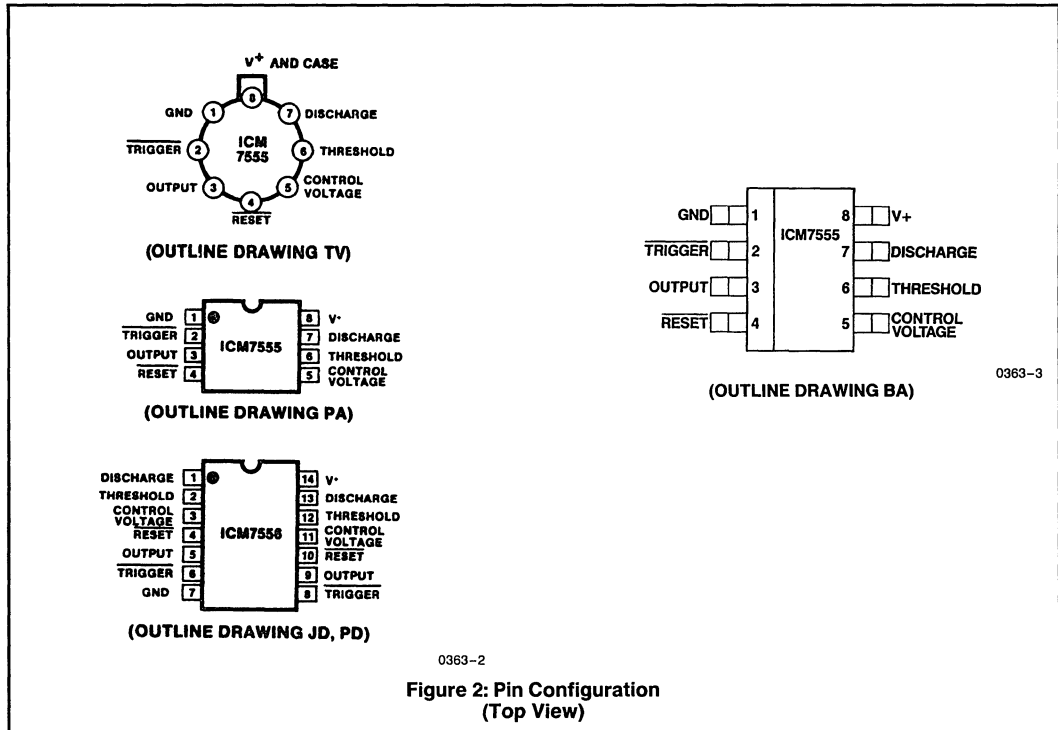


# ICM7555/ICM7556

## ABSOLUTE MAXIMUM RATINGS

|  |       |                              |
|--|-------|------------------------------|
| Supply Voltage                             | ..... | + 18 Volts                   |
| Input Voltage: Trigger,                    |       |                              |
| Control Voltage, Threshold,                | ....  | $V^+ + 0.3V$ to $GND - 0.3V$ |
| Reset <sup>[1]</sup>                       |       |                              |
| Output Current                             | ..... | 100mA                        |
| Power Dissipation <sup>[2]</sup> ICM7556   | ..... | 300mW                        |
| ICM7555                                    | ..... | 200mW                        |
| Storage Temperature                        | ..... | -65°C to +150°C              |
| Lead Temperature (Soldering, 10sec)        | ..... | +300°C                       |
| Operating Temperature Range <sup>[2]</sup> |       |                              |
| ICM7555/6 CX                               | ..... | 0°C to +70°C                 |
| ICM7555/6 IX                               | ..... | -25°C to +85°C               |
| ICM7555/6 MX                               | ..... | -55°C to +125°C              |

**NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



- NOTES 1:** Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than  $V^+ + 0.3V$  or less than  $V^- - 0.3V$  may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power-supply is established. In multiple systems, the supply of the ICM7555/6 must be turned on first.
- 2:** Junction temperatures should not exceed 135°C and the power dissipation must be limited to 20 mW at 125°C. Below 125°C power dissipation may be increased to 300 mW at 25°C. Derating factor is approximately 3 mW/°C (7556) or 2 mW/°C (7555).

NOTE: All typical values have been characterized but are not tested.



# ICM7555/ICM7556

## ICM7555 ELECTRICAL CHARACTERISTICS

| Symbol            | Parameter                     | Test Conditions   | ICM7555C,I,M          |      |      | ICM7555M                        |                   |      | Units                      |
|-------------------|-------------------------------|---|-----------------------|------|------|---------------------------------|-------------------|------|----------------------------|
|                   |                               |   | T <sub>A</sub> = 25°C |      |      | -55°C ≤ T <sub>A</sub> ≤ +125°C |                   |      |                            |
|                   |                               |   | Min                   | Typ  | Max  | Min                             | Typ               | Max  |                            |
| I <sup>+</sup>    | Static Supply Current         | V <sub>DD</sub> = 5V<br>V <sub>DD</sub> = 15V   |                       | 40   | 200  |                                 |                   | 300  | μA                         |
|                   |                               |   |                       | 60   | 300  |                                 |                   | 300  | μA                         |
|                   | Monostable Timing Accuracy    | RA = 10k, C = 0.1μF, V <sub>DD</sub> = 5V   |                       | 2    |      | 858                             |                   | 1161 | %<br>μs                    |
|                   | Drift with Temp*              | V <sub>DD</sub> = 5V<br>V <sub>DD</sub> = 10V<br>V <sub>DD</sub> = 15V                                  |                       |      |      |                                 | 150<br>200<br>250 |      | ppm/°C<br>ppm/°C<br>ppm/°C |
|                   | Drift with Supply*            | V <sub>DD</sub> = 5 to 15V  |                       | 0.5  |      |                                 | 0.5               |      | %/V                        |
|                   | Astable Timing Accuracy       | RA = RB = 10k, C = 0.1μF, V <sub>DD</sub> = 5V  |                       | 2    |      | 1717                            |                   | 2323 | %<br>μs                    |
|                   | Drift with Temp*              | V <sub>DD</sub> = 5V<br>V <sub>DD</sub> = 10V<br>V <sub>DD</sub> = 15V                                  |                       |      |      |                                 | 150<br>200<br>250 |      | ppm/°C<br>ppm/°C<br>ppm/°C |
|                   | Drift with Supply*            | V <sub>DD</sub> = 5V to 15V   |                       | 0.5  |      |                                 | 0.5               |      | %/V                        |
| V <sub>TH</sub>   | Threshold Voltage             | V <sub>DD</sub> = 15V   | 62                    | 67   | 71   | 61                              |                   | 72   | % V <sub>DD</sub>          |
| V <sub>TRIG</sub> | Trigger Voltage               | V <sub>DD</sub> = 15V   | 28                    | 32   | 36   | 27                              |                   | 37   | % V <sub>DD</sub>          |
| I <sub>TRIG</sub> | Trigger Current               | V <sub>DD</sub> = 15V   |                       |      | 10   |                                 |                   | 50   | nA                         |
| I <sub>TH</sub>   | Threshold Current             | V <sub>DD</sub> = 15V   |                       |      | 10   |                                 |                   | 50   | nA                         |
| V <sub>CV</sub>   | Control Voltage               | V <sub>DD</sub> = 15V   | 62                    | 67   | 71   | 61                              |                   | 72   | % V <sub>DD</sub>          |
| V <sub>RST</sub>  | Reset Voltage                 | V <sub>DD</sub> = 2 to 15V  | 0.4                   |      | 1.0  | 0.2                             |                   | 1.2  | V                          |
| I <sub>RST</sub>  | Reset Current                 | V <sub>DD</sub> = 15V   |                       |      | 10   |                                 |                   | 50   | nA                         |
| I <sub>DIS</sub>  | Discharge Leakage             | V <sub>DD</sub> = 15V   |                       |      | 10   |                                 |                   | 50   | nA                         |
| V <sub>OL</sub>   | Output Voltage Drop           | V <sub>DD</sub> = 15V, I <sub>sink</sub> = 20mA<br>V <sub>DD</sub> = 5V, I <sub>sink</sub> = 3.2mA      |                       | 0.4  | 1.0  |                                 |                   | 1.25 | V                          |
|                   |                               |   |                       | 0.2  | 0.4  |                                 |                   | 0.5  | V                          |
| V <sub>OH</sub>   | Output Voltage Drop           | V <sub>DD</sub> = 15V, I <sub>source</sub> = 0.8mA<br>V <sub>DD</sub> = 5V, I <sub>source</sub> = 0.8mA | 14.3                  | 14.6 |      | 14.2                            |                   |      | V                          |
|                   |                               |   | 4.0                   | 4.3  |      | 3.8                             |                   |      | V                          |
| V <sub>DIS</sub>  | Discharge Output Voltage Drop | V <sub>DD</sub> = 5V, I <sub>SINK</sub> = 15mA<br>V <sub>DD</sub> = 15V, I <sub>sink</sub> = 15mA       |                       | 0.2  | 0.4  |                                 |                   | 0.6  | V                          |
|                   |                               |   |                       |      |      |                                 |                   | 0.4  | V                          |
| V <sup>+</sup>    | Supply Voltage*               | Functional Oper.  | 2.0                   |      | 18.0 | 3.0                             |                   | 16.0 | V                          |
| t <sub>R</sub>    | Output Rise Time*             | RL = 10M, CL = 10pF, V <sub>DD</sub> = 5V   |                       | 75   |      |                                 |                   |      | ns                         |
| t <sub>F</sub>    | Output Fall Time*             | RL = 10M, CL = 10pF, V <sub>DD</sub> = 5V   |                       | 75   |      |                                 |                   |      | ns                         |
| f <sub>MAX</sub>  | Oscillator Frequency*         | V <sub>DD</sub> = 5V, RA = 470Ω,<br>RB = 270Ω C = 200pF   |                       | 1    |      |                                 |                   |      | MHz                        |

\*These parameters are based upon characterization data and are not tested.

NOTE: All typical values have been characterized but are not tested.

# ICM7555/ICM7556

## ICM7556

### ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ , unless otherwise specified.

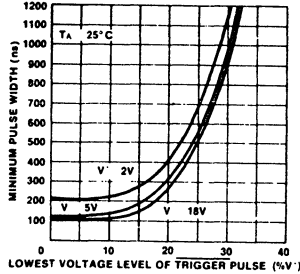
| Symbol            | Parameter                     | Test Conditions   | ICM7556I,M               |      |      | ICM7556M   |                   |      | Units   |
|-------------------|-------------------------------|---|--------------------------|------|------|--|-------------------|------|---|
|                   |                               |   | $T_A = 25^\circ\text{C}$ |      |      | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ |                   |      |   |
|                   |                               |   | Min                      | Typ  | Max  | Min  | Typ               | Max  |   |
| I <sup>+</sup>    | Static Supply Current         | $V_{DD} = 5\text{V}$<br>$V_{DD} = 15\text{V}$   |                          | 80   | 400  |  |                   | 600  | $\mu\text{A}$   |
|                   |                               |   |                          | 120  | 600  |  |                   | 600  | $\mu\text{A}$   |
|                   | Monostable Timing Accuracy    | $RA = 10\text{k}, C = 0.1\mu\text{F}, V_{DD} = 5\text{V}$   |                          | 2    |      | 858  |                   | 1161 | %<br>$\mu\text{s}$  |
|                   | Drift with Temp*              | $V_{DD} = 5\text{V}$<br>$V_{DD} = 10\text{V}$<br>$V_{DD} = 15\text{V}$  |                          |      |      |  | 150<br>200<br>250 |      | ppm/ $^\circ\text{C}$<br>ppm/ $^\circ\text{C}$<br>ppm/ $^\circ\text{C}$ |
|                   | Drift with Supply*            | $V_{DD} = 5\text{V to } 15\text{V}$   |                          | 0.5  |      |  | 0.5               |      | %/V   |
|                   | Astable Timing Accuracy       | $RA = RB = 10\text{k}, C = 0.1\mu\text{F}, V_{DD} = 5\text{V}$  |                          | 2    |      | 1717   |                   | 2323 | %<br>$\mu\text{s}$  |
|                   | Drift with Temp*              | $V_{DD} = 5\text{V}$<br>$V_{DD} = 10\text{V}$<br>$V_{DD} = 15\text{V}$  |                          |      |      |  | 150<br>200<br>250 |      | ppm/ $^\circ\text{C}$<br>ppm/ $^\circ\text{C}$<br>ppm/ $^\circ\text{C}$ |
|                   | Drift with Supply*            | $V_{DD} = 5\text{V to } 15\text{V}$   |                          | 0.5  |      |  | 0.5               |      | %/V   |
| V <sub>TH</sub>   | Threshold Voltage             | $V_{DD} = 15\text{V}$   | 62                       | 67   | 71   | 61   |                   | 72   | % $V_{DD}$  |
| V <sub>TRIG</sub> | Trigger Voltage               | $V_{DD} = 15\text{V}$   | 28                       | 32   | 36   | 27   |                   | 37   | % $V_{DD}$  |
| I <sub>TRIG</sub> | Trigger Current               | $V_{DD} = 15\text{V}$   |                          |      | 10   |  |                   | 50   | nA  |
| I <sub>TH</sub>   | Threshold Current             | $V_{DD} = 15\text{V}$   |                          |      | 10   |  |                   | 50   | nA  |
| V <sub>CV</sub>   | Control Voltage               | $V_{DD} = 15\text{V}$   | 62                       | 67   | 71   | 61   |                   | 72   | % $V_{DD}$  |
| V <sub>RST</sub>  | Reset Voltage                 | $V_{DD} = 2\text{V to } 15\text{V}$   | 0.4                      |      | 1.0  | 0.2  |                   | 1.2  | V   |
| I <sub>RST</sub>  | Reset Current                 | $V_{DD} = 15\text{V}$   |                          |      | 10   |  |                   | 50   | nA  |
| I <sub>DIS</sub>  | Discharge Leakage             | $V_{DD} = 15\text{V}$   |                          |      | 10   |  |                   | 50   | nA  |
| V <sub>OL</sub>   | Output Voltage Drop           | $V_{DD} = 15\text{V}, I_{\text{sink}} = 20\text{mA}$<br>$V_{DD} = 5\text{V}, I_{\text{sink}} = 3.2\text{mA}$      |                          | 0.4  | 1.0  |  |                   | 1.25 | V   |
|                   |                               |   |                          | 0.2  | 0.4  |  |                   | 0.5  | V   |
| V <sub>OH</sub>   | Output Voltage Drop           | $V_{DD} = 15\text{V}, I_{\text{source}} = 0.8\text{mA}$<br>$V_{DD} = 5\text{V}, I_{\text{source}} = 0.8\text{mA}$ | 14.3                     | 14.6 |      | 14.2   |                   |      | V   |
|                   |                               |   | 4.0                      | 4.3  |      | 3.8  |                   |      | V   |
| V <sub>DIS</sub>  | Discharge Output Voltage Drop | $V_{DD} = 5\text{V}, I_{\text{sink}} = 15\text{mA}$<br>$V_{DD} = 15\text{V}, I_{\text{sink}} = 15\text{mA}$       |                          | 0.2  | 0.4  |  |                   | 0.6  | V   |
|                   |                               |   |                          |      |      |  |                   | 0.4  | V   |
| V <sup>+</sup>    | Supply Voltage*               | Functional Oper.  | 2.0                      |      | 18.0 | 3.0  |                   | 16.0 | V   |
| t <sub>R</sub>    | Output Rise Time*             | $RL = 10\text{M}, CL = 10\text{pF}, V_{DD} = 5\text{V}$   |                          | 75   |      |  |                   |      | ns  |
| t <sub>F</sub>    | Output Fall Time*             | $RL = 10\text{M}, CL = 10\text{pF}, V_{DD} = 5\text{V}$   |                          | 75   |      |  |                   |      | ns  |
| f <sub>MAX</sub>  | Oscillator Frequency*         | $V_{DD} = 5\text{V}, RA = 470\Omega,$<br>$RB = 270\Omega, C = 200\text{pF}$                                       |                          | 1    |      |  |                   |      | MHz   |

\*These parameters are based upon characterization data and are not tested.

# ICM7555/ICM7556

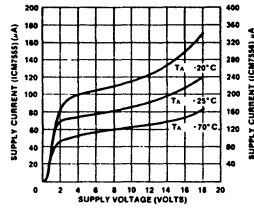
## TYPICAL PERFORMANCE CHARACTERISTICS

**MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING**



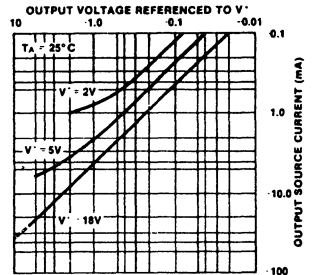
0363-4

**SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE**



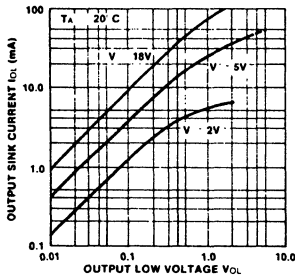
0363-5

**OUTPUT SOURCE CURRENT AS A FUNCTION OF OUTPUT VOLTAGE**



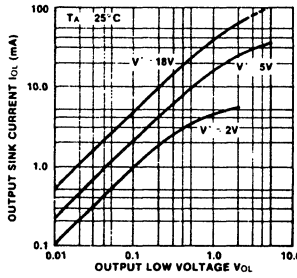
0363-6

**OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE**



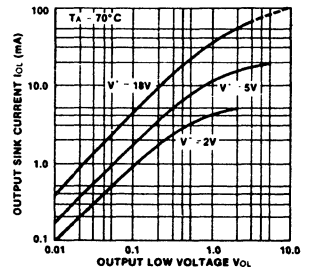
0363-7

**OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE**



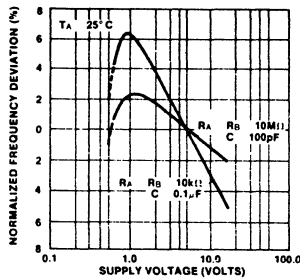
0363-8

**OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE**



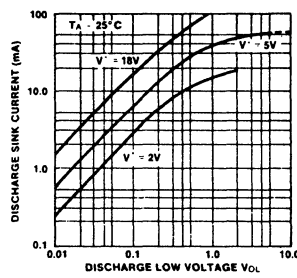
0363-9

**NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE**



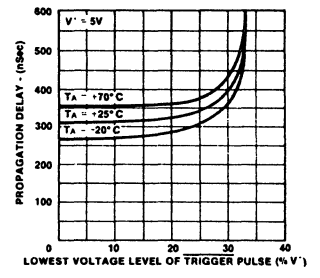
0363-10

**DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE**



0363-11

**PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE**



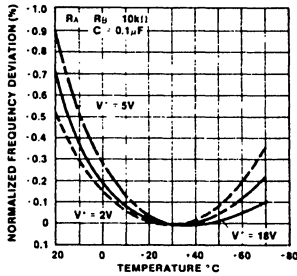
0363-12

NOTE: All typical values have been characterized but are not tested.

# ICM7555/ICM7556

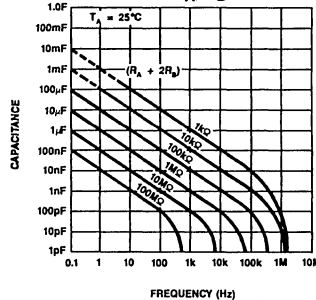
## TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

**NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE**



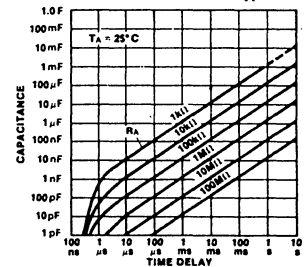
0363-13

**FREE RUNNING FREQUENCY AS A FUNCTION OF RA, RB AND C**



0363-14

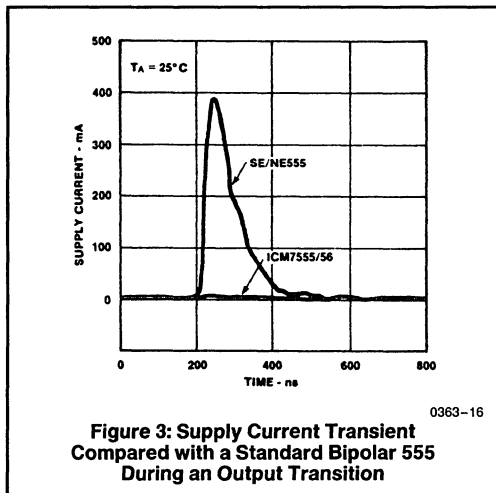
**TIME DELAY IN THE MONOSTABLE MODE AS A FUNCTION OF RA AND C**



0363-15

## APPLICATION NOTES GENERAL

The ICM7555/6 devices are, in most instances, direct replacements for the NE/SE 555/6 devices. However, it is possible to effect economies in the external component count using the ICM7555/6. Because the bipolar 555/6 devices produce large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The 7555/6 devices produce no such transients. See Figure 3.



**Figure 3: Supply Current Transient Compared with a Standard Bipolar 555 During an Output Transition**

0363-16

The ICM7555/6 produces supply current spikes of only 2-3mA instead of 300-400mA and supply decoupling is normally not necessary. Secondly, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications 2 capacitors can be saved using an ICM7555, and 3 capacitors with an ICM7556.

## POWER SUPPLY CONSIDERATIONS

Although the supply current consumed by the ICM7555/6 devices is very low, the total system supply can be high unless the timing components are high impedance. Therefore, use high values for R and low values for C in Figures 4 and 5.

## OUTPUT DRIVE CAPABILITY

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5 volts or more the ICM7555/6 will drive at least 2 standard TTL loads.

## ASTABLE OPERATION

The circuit can be connected to trigger itself and free run as a multivibrator, see Figure 4. The output swings from rail to rail, and is a true 50% duty cycle square wave. (Trip points and output swings are symmetrical). Less than a 1% frequency variation is observed, over a voltage range of +5 to +15V.

$$f = \frac{1.44}{RC}$$

The timer can also be connected as shown in Figure 4b. In this circuit, the frequency is:

$$f = 1.44/(R_A + 2R_B)C$$

The duty cycle is controlled by the values of  $R_A$  and  $R_B$ , by the equation:

$$D = R_B/(R_A + 2R_B)$$

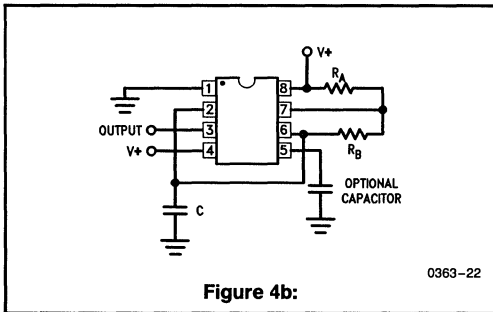
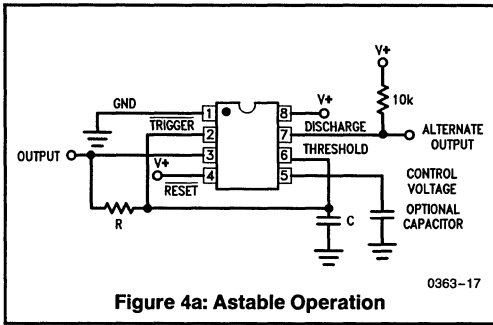
## MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot. Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative TRIGGER pulse to pin 2, the internal flip flop is set which releases the short circuit across the external capacitor and drives the OUTPUT high. The voltage across the capacitor now increases exponentially with a time constant  $t = R_A C$ . When the voltage across the capacitor equals  $\frac{2}{3} V^+$ , the comparator resets the flip flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. TRIGGER must return to a high state before the OUTPUT can return to a low state.

$$t_{\text{output}} = -\ln(\frac{1}{3}) R_A C = 1.1 R_A C$$

NOTE: All typical values have been characterized but are not tested.

# ICM7555/ICM7556

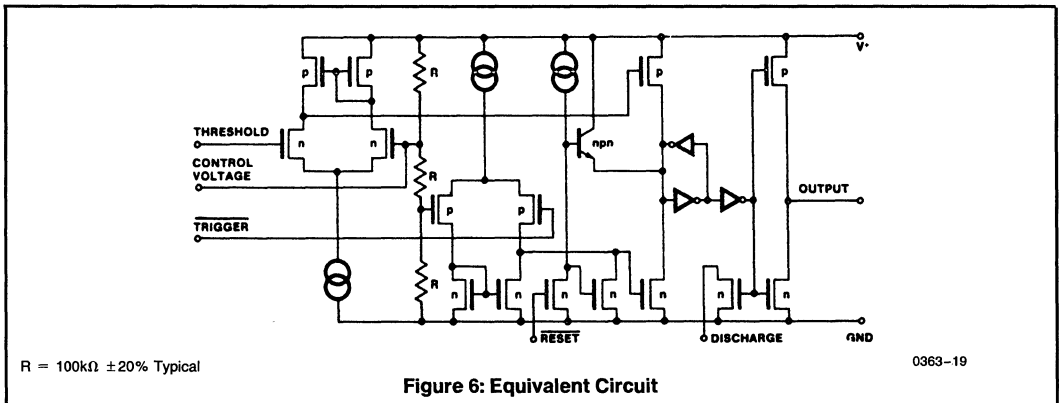
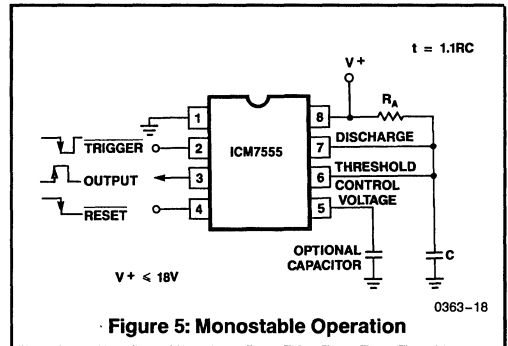


## CONTROL VOLTAGE

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and TRIGGER internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

## RESET

The RESET terminal is designed to have essentially the same trip voltage as the standard bipolar 555/6, i.e. 0.6 to 0.7 volts. At all supply voltages it represents an extremely high input impedance. The mode of operation of the RESET function is, however, much improved over the standard bipolar 555/6 in that it controls only the internal flip flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.



R = 100kΩ ±20% Typical

# ICM7555/ICM7556

## TRUTH TABLE

| Threshold Voltage    | $\overline{\text{Trigger}}$ Voltage | $\overline{\text{RESET}}$ | Output | Discharge Switch |
|----------------------|-------------------------------------|---------------------------|--------|------------------|
| DON'T CARE           | DON'T CARE                          | LOW                       | LOW    | ON               |
| $> \frac{2}{3}(V^+)$ | $> \frac{1}{3}(V^+)$                | HIGH                      | LOW    | ON               |
| $< \frac{2}{3}(V^+)$ | $> \frac{1}{3}(V^+)$                | HIGH                      | STABLE | STABLE           |
| DON'T CARE           | $< \frac{1}{3}(V^+)$                | HIGH                      | HIGH   | OFF              |

NOTE:  $\overline{\text{RESET}}$  will dominate all other inputs;  $\overline{\text{TRIGGER}}$  will dominate over THRESHOLD.



## TELECOMMUNICATIONS

|                                      | PAGE   |
|--------------------------------------|--|
| <b>TELECOMMUNICATION DATA SHEETS</b> |  |
| CD22100                              | CMOS 4 x 4 Crosspoint Switch with Control Memory . . . . . 9-3                   |
| CD22101                              | CMOS 4 x 4 x 2 Crosspoint Switches with Control Memory . . . . . 9-9             |
| CD22102                              | CMOS 4 x 4 x 2 Crosspoint Switches with Control Memory . . . . . 9-9             |
| CD22103A                             | CMOS HDB3 (High-Density Bipolar 3) Transcoder for 2.048/8.448 Mbs . . . . . 9-17 |
| CD22202E                             | 5V Low-Power DTMF Receiver . . . . . 9-24  |
| CD22203E                             | 5V Low-Power DTMF Receiver . . . . . 9-24  |
| CD22204                              | 5V Low-Power DTMF Receiver . . . . . 9-29  |
| CD22301                              | PCM Line Repeater . . . . . 9-34   |
| CD22354A                             | CMOS Single-Chip, Full-Feature PCM CODEC . . . . . 9-38                          |
| CD22357A                             | CMOS Single-Chip, Full-Feature PCM CODEC . . . . . 9-38                          |
| <b>CD22M3493</b>                     | <b>12 x 8 x 1 BiMOS-E Crosspoint Switch</b> . . . . . 9-46                       |
| <b>CD22M3494</b>                     | <b>16 x 6 x 1 BiMOS-E Crosspoint Switch</b> . . . . . 9-51                       |
| CD22859                              | COS/MOS Dual-Tone Multifrequency Tone Generator . . . . . 9-57                   |
| CD74HC22106                          | QMOS 8 x 8 x 1 Crosspoint Switch with Memory Control . . . . . 9-61              |
| CD74HCT22106                         | QMOS 8 x 8 x 1 Crosspoint Switch with Memory Control . . . . . 9-61              |
| HC 5502A                             | SLIC Subscriber Line Interface Circuit . . . . . 9-69                            |
| <b>HC 5502B</b>                      | <b>SLIC Subscriber Line Interface Circuit</b> . . . . . 9-75                     |
| HC 5504                              | SLIC Subscriber Line Interface Circuit . . . . . 9-82                            |
| <b>HC 5504B</b>                      | <b>SLIC Subscriber Line Interface Circuit</b> . . . . . 9-88                     |
| <b>HC 5504DLC</b>                    | <b>SLIC Subscriber Line Interface Circuit</b> . . . . . 9-95                     |
| <b>HC 5509B</b>                      | <b>SLIC Subscriber Line Interface Circuit</b> . . . . . 9-102                    |
| HC 5524                              | SLIC Subscriber Line Interface Circuit . . . . . 9-111                           |
| HC 5560                              | PCM Transcoder . . . . . 9-120   |
| HC 55536                             | Continuously Variable Slope Delta Demodulator (CVSD) . . . . . 9-129             |
| HC 55564                             | Continuously Variable Slope Delta-Modulator (CVSD) . . . . . 9-133               |

**NOTE:** Bold type designates a new product from Harris.





## CMOS 4 x 4 Crosspoint Switch with Control Memory High-Voltage Types (20V Rating)

August 1991

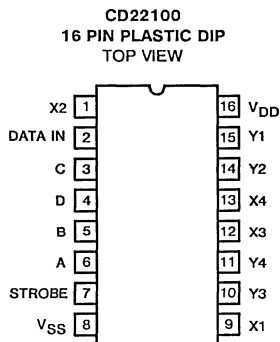
### Features

- Low ON Resistance ..... 75Ω Typ. at  $V_{DD} = 12V$
- "Built-In" Control Latches
- Large Analog Signal Capability .....  $\pm V_{DD}/2$
- 10MHz Switch Bandwidth
- Matched Switch Characteristics  $\Delta R_{ON} = 18\Omega$  Typ. at  $V_{DD} = 12V$
- High Linearity - 0.5% Distortion (Typ.) at  $f = 1kHz$ ,  $V_{IN} = 5Vp-p$ ,  $V_{DD} = 10V$ , and  $R_L = 1k\Omega$
- Standard CMOS Noise Immunity
- 100% Tested for Maximum Quiescent Current at 20V

### Description

CD22100 combines a 4 x 4 array of crosspoints (transmission gates) with a 4-line-to-16-line decoder and 16 latch circuits. Any one of the sixteen transmission gate (crosspoints) can be selected by applying the appropriate four line address. The selected transmission gate can be turned on or off by applying a logical one or zero, respectively, to the data input and strobing the strobe input to a logical one. Any number of the transmission gates can be ON simultaneously. When the required operating power is applied to the CD22100, the states of the 16 switches are indeterminate. Therefore, all switches must be turned off by putting the strobe high and data-in low, and then addressing all switches in succession.

### Pinout



### Functional Diagram

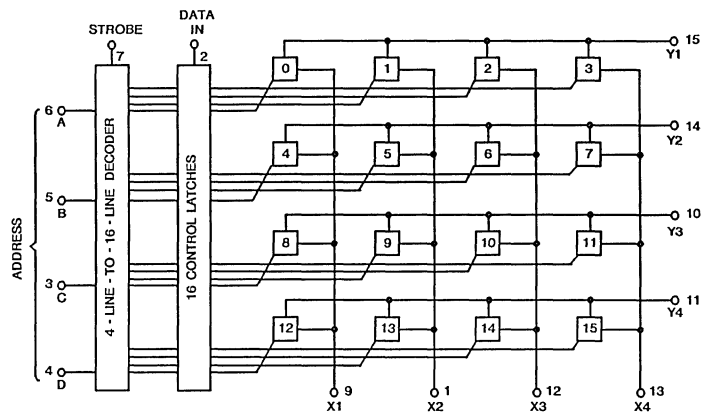


FIGURE 1.

# CD22100

## MAXIMUM RATINGS, Absolute-Maximum Values:

|  |   |
|--|---|
| DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )  | -0.5 to +20 V   |
| (Voltages referenced to $V_{SS}$ Terminal)                                     |   |
| INPUT VOLTAGE RANGE, ALL INPUTS  | -0.5 to $V_{DD} + 0.5$ V                                    |
| DC INPUT CURRENT, ANY ONE INPUT*   | $\pm 10$ mA   |
| POWER DISSIPATION PER PACKAGE ( $P_D$ ):                                       |   |
| For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)                        | 500 mW  |
| For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)                        | Derate Linearly at $12 \text{ mW}/^\circ\text{C}$ to 200 mW |
| For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPES D, F)                   | 500 mW  |
| For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPES D, F)                  | Derate Linearly at $12 \text{ mW}/^\circ\text{C}$ to 200 mW |
| DEVICE DISSIPATION PER TRANSMISSION GATE                                       |   |
| FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$          | 100 mW  |
| OPERATING-TEMPERATURE RANGE ( $T_A$ ):   |   |
| PACKAGE TYPES D, F   | $-55$ to $+125^\circ\text{C}$                               |
| PACKAGE TYPE E   | $-40$ to $+85^\circ\text{C}$                                |
| STORAGE TEMPERATURE RANGE ( $T_{stg}$ )  | $-65$ to $+150^\circ\text{C}$                               |
| LEAD TEMPERATURE (DURING SOLDERING):   |   |
| At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79$ mm) from case for 10 s max. | $+265^\circ\text{C}$  |

\* Maximum current through transmission gates (switches) = 25mA

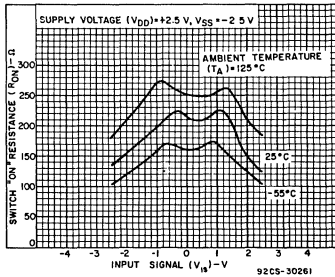


Fig. 2— Typical ON resistance as a function of input signal voltage at  $V_{DD} = -V_{SS} = 2.5$  V.

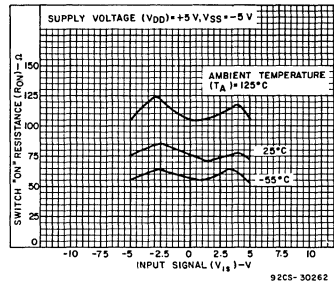


Fig. 3— Typical ON resistance as a function of input signal voltage at  $V_{DD} = -V_{SS} = 5$  V.

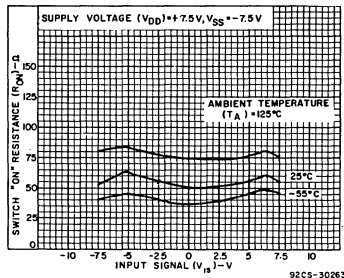


Fig. 4— Typical ON resistance as a function of input signal voltage at  $V_{DD} = -V_{SS} = 7.5$  V.

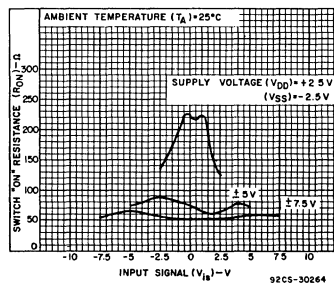


Fig. 5— Typical ON resistance as a function of input signal voltage at  $T_A = 25^\circ\text{C}$ .

# CD22100

## RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC  | LIMITS |      | UNITS |
|---|--------|------|-------|
|   | MIN.   | MAX. |       |
| Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range) | 3      | 18   | V     |

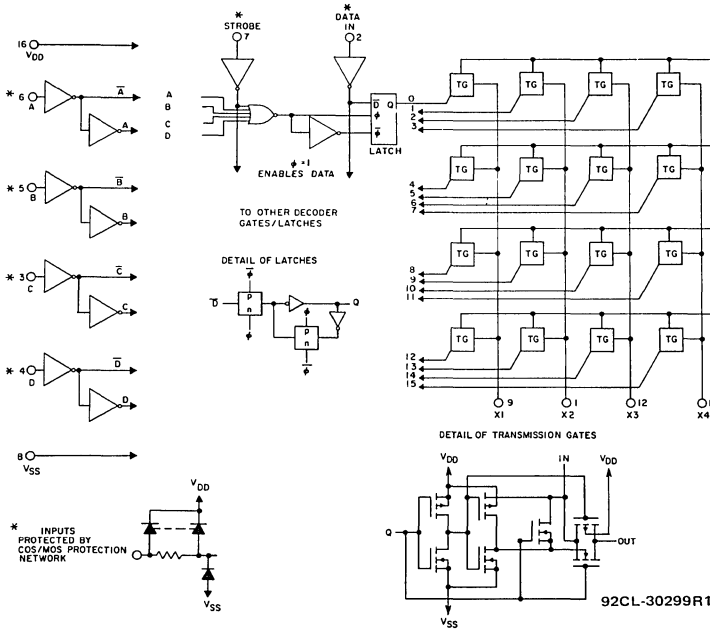


Fig. 6— Schematic diagram.

| TRUTH TABLE |   |   |   |        |         |   |   |   |        |
|-------------|---|---|---|--------|---------|---|---|---|--------|
| Address     |   |   |   | Select | Address |   |   |   | Select |
| A           | B | C | D |        | A       | B | C | D |        |
| 0           | 0 | 0 | 0 | X1Y1   | 0       | 0 | 0 | 1 | X1Y3   |
| 1           | 0 | 0 | 0 | X2Y1   | 1       | 0 | 0 | 1 | X2Y3   |
| 0           | 1 | 0 | 0 | X3Y1   | 0       | 1 | 0 | 1 | X3Y3   |
| 1           | 1 | 0 | 0 | X4Y1   | 1       | 1 | 0 | 1 | X4Y3   |
| 0           | 0 | 1 | 0 | X1Y2   | 0       | 0 | 1 | 1 | X1Y4   |
| 1           | 0 | 1 | 0 | X2Y2   | 1       | 0 | 1 | 1 | X2Y4   |
| 0           | 1 | 1 | 0 | X3Y2   | 0       | 1 | 1 | 1 | X3Y4   |
| 1           | 1 | 1 | 0 | X4Y2   | 1       | 1 | 1 | 1 | X4Y4   |

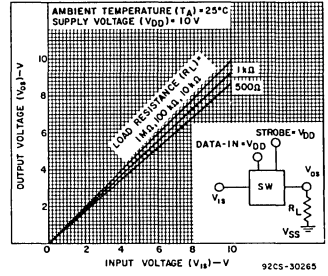


Fig. 7 — Typical switch ON transfer characteristics (1 of 16 switches).

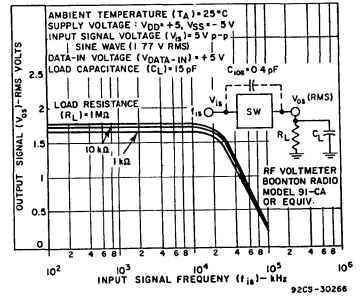


Fig. 8 — Typical switch ON frequency response characteristics.

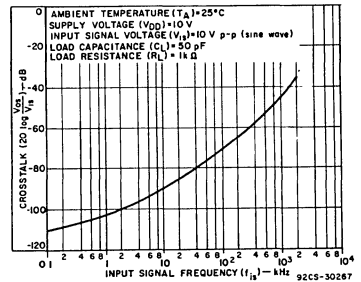


Fig. 9 — Typical crosstalk between switches as a function of signal frequency.

# CD22100

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC                                  | CONDITIONS   | LIMITS at Indicated Temperature (°C)       |                        |      |      |       |      |      |                   | Units |    |
|---|--|--|------------------------|------|------|-------|------|------|-------------------|-------|----|
|   |  | Values at -55,+25,+125, apply to D,F,H pkg |                        |      |      |       |      |      |                   |       |    |
|   |  | Values at -40,+25,+85, apply to E pkg      |                        |      |      |       |      |      |                   |       |    |
|   |  | V <sub>IN</sub><br>(V)                     | V <sub>DD</sub><br>(V) | -55  | -40  | +85   | +125 | +25  |                   |       |    |
|   |  |  |                        |      |      |       |      | Min. | Typ.              | Max.  |    |
| <b>CROSSPOINTS</b>                              |  |  |                        |      |      |       |      |      |                   |       |    |
| Quiescent Device Current, I <sub>DD</sub> Max.  | Any Switch   | -  | 5                      | 5    | 5    | 150   | 150  | -    | 0.04              | 5     | μA |
|   |  | -  | 10                     | 10   | 10   | 300   | 300  | -    | 0.04              | 10    |    |
|   |  | -  | 15                     | 20   | 20   | 600   | 600  | -    | 0.04              | 20    |    |
|   |  | -  | 20                     | 100  | 100  | 3000  | 3000 | -    | 0.08              | 100   |    |
| ON Resistance, R <sub>ON</sub> Max.             | Any Switch<br>V <sub>IS</sub> = 0 to V <sub>DD</sub> | -  | 5                      | 475  | 500  | 725   | 800  | -    | 225               | 600   | Ω  |
|   |  | -  | 10                     | 135  | 145  | 205   | 230  | -    | 85                | 180   |    |
|   |  | -  | 12                     | 100  | 110  | 155   | 175  | -    | 75                | 135   |    |
|   |  | -  | 15                     | 70   | 75   | 110   | 125  | -    | 65                | 95    |    |
| ΔON Resistance, ΔR <sub>ON</sub>                | Between any two switches                             | -  | 5                      | -    | -    | -     | -    | -    | 25                | -     | Ω  |
|   |  | -  | 10                     | -    | -    | -     | -    | -    | 10                | -     |    |
|   |  | -  | 12                     | -    | -    | -     | -    | -    | 8                 | -     |    |
|   |  | -  | 15                     | -    | -    | -     | -    | -    | 5                 | -     |    |
| OFF Switch Leakage Current, I <sub>L</sub> Max. | All switches OFF                                     | 0,18                                       | 18                     | ±100 |      | ±1000 |      | -    | ±1                | ±100* | nA |
| <b>CONTROLS</b>                                 |  |  |                        |      |      |       |      |      |                   |       |    |
| Input Low Voltage, V <sub>IL</sub> Max.         | OFF switch<br>I <sub>L</sub> < 0.2 μA                | -  | 5                      | 1.5  |      |       | -    | -    | 1.5               | V     |    |
|   |  | -  | 10                     | 3    |      |       | -    | -    | 3                 |       |    |
|   |  | -  | 15                     | 4    |      |       | -    | -    | 4                 |       |    |
| Input High Voltage, V <sub>IH</sub> Min.        | ON switch<br>see R <sub>ON</sub> characteristic      | -  | 5                      | 3.5  |      |       | 3.5  | -    | -                 | V     |    |
|   |  | -  | 10                     | 7    |      |       | 7    | -    | -                 |       |    |
|   |  | -  | 15                     | 11   |      |       | 11   | -    | -                 |       |    |
| Input Current, I <sub>IN</sub> Max.             | Any control  | 0,18                                       | 18                     | ±0.1 | ±0.1 | ±1    | ±1   | -    | ±10 <sup>-5</sup> | ±0.1  | μA |

\* Determined by minimum feasible leakage measurement for automatic testing.

## DYNAMIC ELECTRICAL CHARACTERISTICS at T<sub>A</sub> = 25°C

| CHARACTERISTIC   | CONDITIONS   |                      |                                     |                        | LIMITS |      |      | UNITS |
|--|--|----------------------|-------------------------------------|------------------------|--------|------|------|-------|
|  | f <sub>is</sub><br>kHz                                     | R <sub>L</sub><br>kΩ | V <sub>is</sub> <sup>o</sup><br>(V) | V <sub>DD</sub><br>(V) | Min.   | Typ. | Max. |       |
| <b>CROSSPOINTS</b>   |  |                      |                                     |                        |        |      |      |       |
| Propagation Delay Time, (Switch ON)<br>Signal Input to Output, t <sub>PHL</sub> , t <sub>PLH</sub> | -  | 10                   | 10                                  | 10                     | -      | 30   | 60   | ns    |
|  | -  | -                    | 15                                  | 15                     | -      | 15   | 20   |       |
| C <sub>L</sub> = 50 pF; t <sub>r</sub> , t <sub>f</sub> = 20 ns                                    |  |                      |                                     |                        |        |      |      |       |
| Frequency Response, (Any Switch ON)  | 1  | 1                    | 5                                   | 10                     | -      | 40   | -    | MHz   |
|  | Sine wave input,<br>20 log $\frac{V_{os}}{V_{is}} = -3$ dB |                      |                                     |                        |        |      |      |       |
| Sine Wave Response, (Distortion)   | 1  | 1                    | 5                                   | 10                     | -      | 0.5  | -    | %     |
| Feedthrough (All Switches OFF)   | 1.6  | 1                    | 5                                   | 10                     | -      | -80  | -    | dB    |
|  | Sine wave input  |                      |                                     |                        |        |      |      |       |

<sup>o</sup>Peak-to-peak voltage symmetrical about  $\frac{V_{DD}}{2}$ .

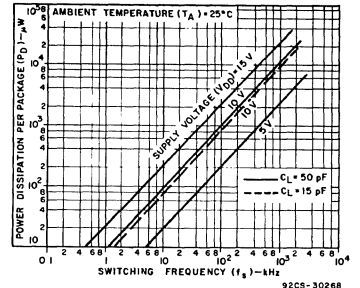


Fig. 10 - Typical dynamic power dissipation as a function of switching frequency.

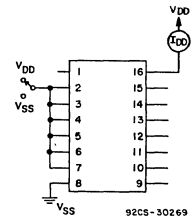


Fig. 11 - Quiescent current test circuit.

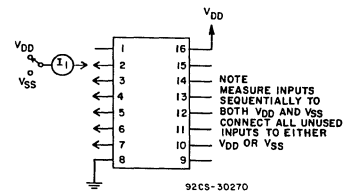


Fig. 12 - Input current test circuit.

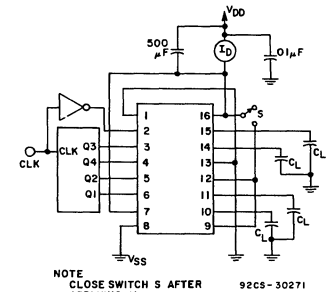


Fig. 13 - Dynamic power dissipation test circuit.

# CD22100

## DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$

| CHARACTERISTIC   | CONDITIONS  |                     |                 |                 | LIMITS |      |      | UNITS     |
|--|---|---------------------|-----------------|-----------------|--------|------|------|-----------|
|  | $f_{is}$<br>kHz   | $R_L$<br>k $\Omega$ | $V_{is}$<br>(V) | $V_{DD}$<br>(V) | Min.   | Typ. | Max. |           |
| <b>CROSSPOINTS (CONT'D)</b>  |   |                     |                 |                 |        |      |      |           |
| Frequency for Signal Crosstalk<br>Attenuation of 40 dB<br>Attenuation of 110 dB          | —   | 1                   | 10              | 10              | —      | 1.5  | —    | MHz       |
|  | Sine wave input   |                     |                 |                 | —      | 0.1  | —    | kHz       |
| Capacitance,<br>$X_n$ to Ground<br>$Y_n$ to Ground<br>Feedthrough                        |   | —                   | —               | 5-15            | —      | 18   | —    | pF        |
|  |   | —                   | —               | 5-15            | —      | 30   | —    |           |
|  |   | —                   | —               | —               | —      | 0.4  | —    |           |
| <b>CONTROLS</b>  |   |                     |                 |                 |        |      |      |           |
| Propagation Delay Time:<br>Strobe to Output, $t_{pZH}$<br>(Switch Turn-ON to High Level) | $R_L = 1\text{k}\Omega$ ,<br>$C_L = 50\text{pF}$ ,<br>$t_r, t_f = 20\text{ ns}$ | See Fig.            |                 | 5               | —      | 300  | 600  |           |
|  |   | 18                  | 10              | —               | 125    | 250  |      |           |
|  |   | 15                  | —               | —               | 80     | 160  |      |           |
| Data-In to Output, $t_{pZH}$<br>(Turn-On to High Level)                                  |   | 19                  | 5               | —               | 110    | 220  | ns   |           |
|  |   | 10                  | —               | —               | 40     | 80   |      |           |
|  |   | 15                  | —               | —               | 25     | 50   |      |           |
| Address to Output, $t_{pZH}$<br>(Turn-ON to High Level)                                  |   | 20                  | 5               | —               | 350    | 700  |      |           |
|  |   | 10                  | —               | —               | 135    | 270  |      |           |
|  |   | 15                  | —               | —               | 90     | 180  |      |           |
| Propagation Delay Time:<br>Strobe to Output, $t_{pHZ}$<br>(Switch Turn-OFF)              |   | 18                  | 5               | —               | 165    | 330  |      |           |
|  |   | 10                  | —               | —               | 85     | 170  |      |           |
|  |   | 15                  | —               | —               | 70     | 140  |      |           |
| Data-In to Output, $t_{pZL}$<br>(Turn-ON to Low Level)                                   |   | 19                  | 5               | —               | 210    | 420  | ns   |           |
|  |   | 10                  | —               | —               | 110    | 220  |      |           |
|  |   | 15                  | —               | —               | 100    | 200  |      |           |
| Address to Output, $t_{pHZ}$<br>(Turn-OFF)   | 20  | 5                   | —               | 435             | 870    |      |      |           |
|  | 10  | —                   | —               | 210             | 420    |      |      |           |
|  | 15  | —                   | —               | 160             | 320    |      |      |           |
| Minimum Setup Time,<br>Data-In to Strobe, Address, $t_{SU}$                              |   | 5                   | —               | 95              | 190    | ns   |      |           |
|  |   | 10                  | —               | 25              | 50     |      |      |           |
|  |   | 15                  | —               | 15              | 30     |      |      |           |
| Minimum Hold Time,<br>Data-In to Strobe, Address, $t_H$                                  |   | 5                   | —               | 180             | 360    | ns   |      |           |
|  |   | 10                  | —               | 110             | 220    |      |      |           |
|  |   | 15                  | —               | 35              | 70     |      |      |           |
| Maximum Switching Frequency, $f_\phi$  | $R_L = 1\text{k}\Omega$ , $C_L = 50\text{ pF}$<br>$t_r, t_f = 20\text{ ns}$     | 5                   | 0.6             | 1.2             | —      | MHz  |      |           |
|  |   | 10                  | 1.6             | 3.2             | —      |      |      |           |
|  |   | 15                  | 2.5             | 5               | —      |      |      |           |
| Minimum Strobe Pulse Width, $t_W$  |   | 5                   | —               | 300             | 600    | ns   |      |           |
|  |   | 10                  | —               | 120             | 240    |      |      |           |
|  |   | 15                  | —               | 90              | 180    |      |      |           |
| Control Crosstalk,<br>Data-In, Address, or Strobe to Output                              | —   | 10                  | 10              | 10              | —      | 75   | —    | mV (peak) |
|  | Square wave input<br>$t_r, t_f = 20\text{ ns}$                                  |                     |                 |                 |        |      |      |           |
| Input Capacitance, $C_{IN}$  | Any Control Input   |                     |                 | —               | —      | 5    | 7.5  | pF        |

• Peak-to-peak voltage symmetrical about  $\frac{V_{DD}}{2}$

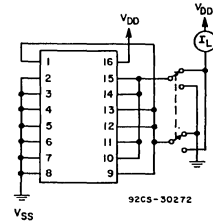
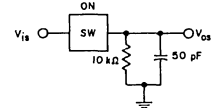


Fig. 14 - OFF switch input or output leakage current test circuit.



SW = ANY CROSSPOINT  
STROBE = DATA-IN + VDD

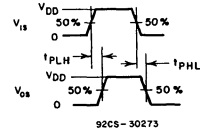


Fig. 15 - Propagation delay time test circuit and waveforms (signal input to signal output, switch ON).

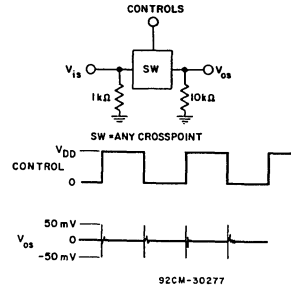


Fig. 16 - Test circuit and waveforms for crosstalk (control input to signal output).

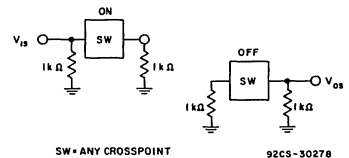


Fig. 17 - Test circuit for crosstalk between switch circuits in the same package.

# CD22100

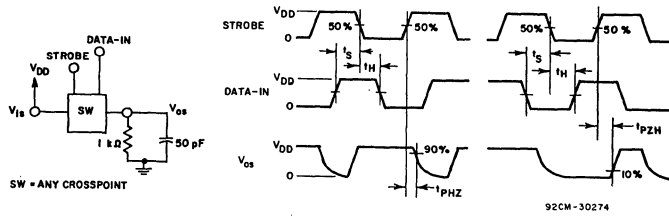


Fig. 18 — Propagation delay time test circuit and waveforms (strobe to signal output, switch Turn-ON or Turn-OFF).

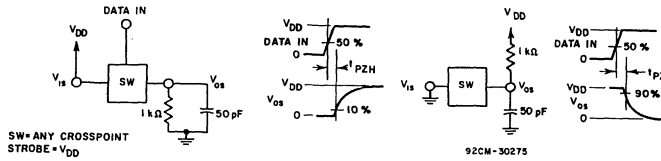


Fig. 19 — Propagation delay time test circuit and waveforms (data-in to signal output, switch Turn-ON to high or low level).

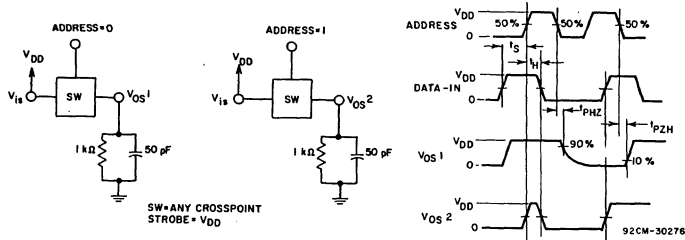
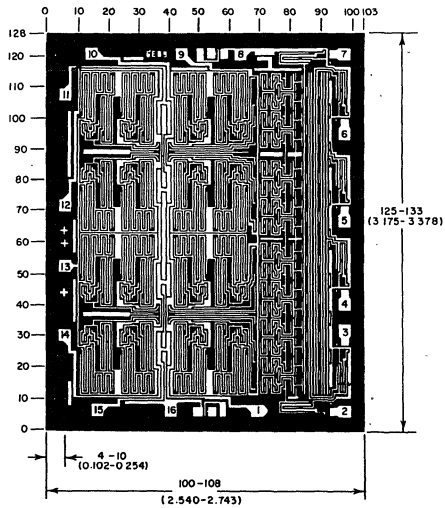


Fig. 20 — Propagation delay time test circuit and waveforms (address to signal output, switch Turn-On or Turn-Off).



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10<sup>-3</sup> inch).

# CD22101 CD22102

## CMOS 4 x 4 x 2 Crosspoint Switch With Control Memory

August 1991

### Features

- Low ON Resistance..... 75V Typ. at  $V_{DD} = 12V$
- "Built-In" Latched Inputs
- Large Analog Signal Capability .....  $\pm V_{DD}/2$
- Switch Bandwidth ..... 10MHz
- Matched Switch Characteristics  $\Delta R_{ON} = 8\Omega$  Typ. at  $V_{DD} = 12V$
- High Linearity - 0.25% Distortion (Typ.) at  $f = 1kHz$ ,  $V_{IN} = 5Vp-p$ ,  $V_{DD} - V_{SS} = 10V$ , and  $R_1 = 1k\Omega$
- Standard CMOS Noise Immunity

### Applications

- Telephone Systems
- PBX
- Studio Audio Switching
- Multisystem Bus Interconnect

### Description

CD22101 and CD22102 crosspoint switches consist of 4 x 4 x 2 arrays of crosspoint (transmission gates) 4-line to 16-line decoders and 16 latch circuits. Any one of the sixteen crosspoint pairs can be selected by applying the appropriate four-line address, and any number of crosspoints can be ON simultaneously. Corresponding crosspoints in each array are turned on and off simultaneously, also.

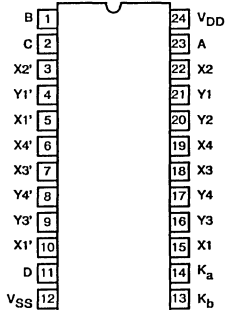
In the CD22101, the selected crosspoint pair can be turned on or off by applying a logical ONE or ZERO, respectively, to the data input, and applying a ONE to the strobe input. When the device is "powered up", the states of the 16 switches are indeterminate. Therefore, all switched must be turned off by putting the strobe high, data-in low, and then addressing all switches in succession.

The selected pair of crosspoints in the CD22102 is turned on by applying a logical ONE to the  $K_a$  (set) input while a logical ZERO is on the  $K_b$  input, and turned off by applying a logical ONE to the  $K_b$  (reset) input while a logical ZERO is on the  $K_a$  input. In this respect, the control latches of the CD22102 are similar to SET/RESET flip-flops. They differ, however, in that the simultaneous application of ONE's to the  $K_a$  and  $K_b$  inputs turns off (resets) all crosspoints. All crosspoints in both devices must be turned off as  $V_{DD}$  is applied.

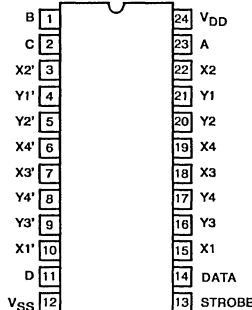
The CD22101 and CD22102 types are supplied in 24 lead Hermetic dual-in-line ceramic packages (D and F suffixes), 24 lead dual-in-line plastic packages (E suffix).

### Pinouts

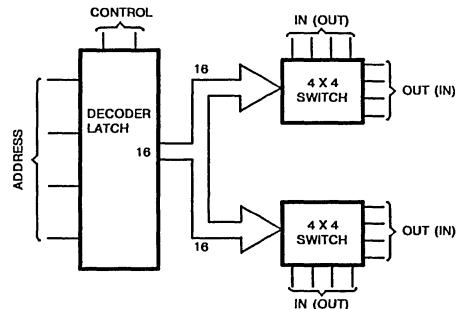
CD22101  
24 PIN CERAMIC/PLASTIC DIP  
TOP VIEW



CD22102  
24 PIN CERAMIC/PLASTIC DIP  
TOP VIEW



### Functional Diagram





# Specifications CD22101, CD22102

**MAXIMUM RATINGS, Absolute-Maximum Values:**

- DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ ) . . . . . -0.5 to +20 V  
(Voltages referenced to  $V_{SS}$  Terminal)
- INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to  $V_{DD} + 0.5$  V
- DC INPUT CURRENT, ANY ONE INPUT\* . . . . .  $\pm 10$  mA
- POWER DISSIPATION PER PACKAGE ( $P_D$ ):
  - For  $T_A = -40$  to  $+60^\circ\text{C}$  (PACKAGE TYPE E) . . . . . 500 mW
  - For  $T_A = +60$  to  $+85^\circ\text{C}$  (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/ $^\circ\text{C}$  to 200 mW
  - For  $T_A = -55$  to  $+100^\circ\text{C}$  (PACKAGE TYPES D, F) . . . . . 500 mW
  - For  $T_A = +100$  to  $+125^\circ\text{C}$  (PACKAGE TYPES D, F) . . . . . Derate Linearly at 12 mW/ $^\circ\text{C}$  to 200 mW
- DEVICE DISSIPATION PER OUTPUT TRANSISTOR  
FOR  $T_A =$  FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
- OPERATING-TEMPERATURE RANGE ( $T_A$ ):
  - PACKAGE TYPES D, F, H . . . . . -55 to  $+125^\circ\text{C}$
  - PACKAGE TYPE E . . . . . -40 to  $+85^\circ\text{C}$
- STORAGE TEMPERATURE RANGE ( $T_{stg}$ ) . . . . . -65 to  $+150^\circ\text{C}$
- LEAD TEMPERATURE (DURING SOLDERING):
  - At distance  $1/16 \pm 1/32$  inch ( $1.59 \pm 0.79$  mm) from case for 10 s max. . . . .  $+265^\circ\text{C}$

\* Maximum current through transmission gates (switches) = 25 mA.

**RECOMMENDED OPERATING CONDITIONS**

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC  | LIMITS |      | UNITS |
|---|--------|------|-------|
|   | Min.   | Max. |       |
| Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range) | 3      | 18   | V     |

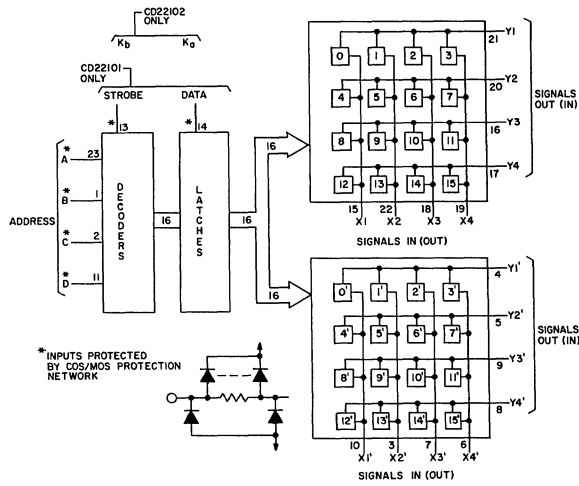


Fig. 1 - Functional block diagram.

# CD22101, CD22102

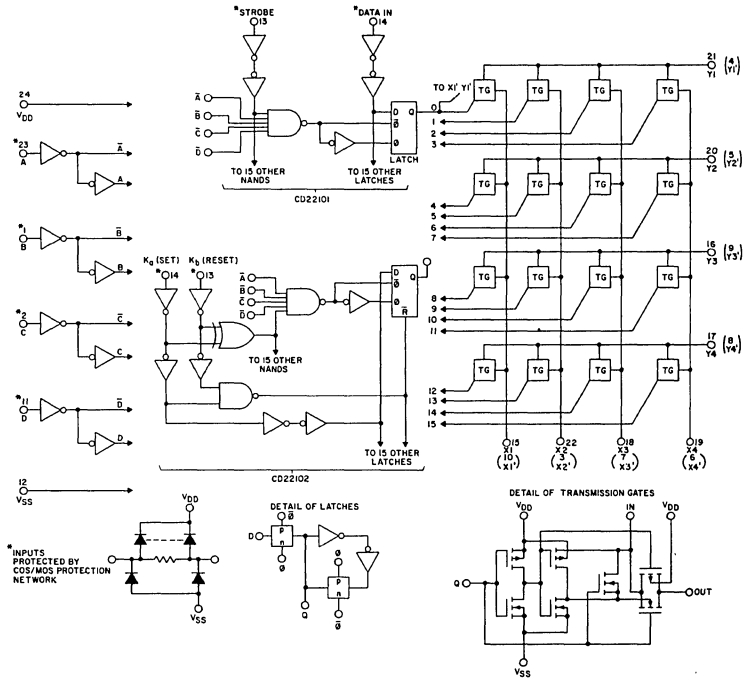


Fig. 2 - Logic diagram.

### DECODER TRUTH TABLE

| Address |   |   |   | Select          | Address |   |   |   | Select          |
|---------|---|---|---|-----------------|---------|---|---|---|-----------------|
| A       | B | C | D |                 | A       | B | C | D |                 |
| 0       | 0 | 0 | 0 | $X1Y1 & X1'Y1'$ | 0       | 0 | 0 | 1 | $X1Y3 & X1'Y3'$ |
| 1       | 0 | 0 | 0 | $X2Y1 & X2'Y1'$ | 1       | 0 | 0 | 1 | $X2Y3 & X2'Y3'$ |
| 0       | 1 | 0 | 0 | $X3Y1 & X3'Y1'$ | 0       | 1 | 0 | 1 | $X3Y3 & X3'Y3'$ |
| 1       | 1 | 0 | 0 | $X4Y1 & X4'Y1'$ | 1       | 1 | 0 | 1 | $X4Y3 & X4'Y3'$ |
| 0       | 0 | 1 | 0 | $X1Y2 & X1'Y2'$ | 0       | 0 | 1 | 1 | $X1Y4 & X1'Y4'$ |
| 1       | 0 | 1 | 0 | $X2Y2 & X2'Y2'$ | 1       | 0 | 1 | 1 | $X2Y4 & X2'Y4'$ |
| 0       | 1 | 1 | 0 | $X3Y2 & X3'Y2'$ | 0       | 1 | 1 | 1 | $X3Y4 & X3'Y4'$ |
| 1       | 1 | 1 | 0 | $X4Y2 & X4'Y2'$ | 1       | 1 | 1 | 1 | $X4Y4 & X4'Y4'$ |

### CONTROL TRUTH TABLE FOR CD22101

| Function   | Address |   |   |   | Strobe | Data | Select                   |
|------------|---------|---|---|---|--------|------|--------------------------|
|            | A       | B | C | D |        |      |                          |
| Switch On  | 1       | 1 | 1 | 1 | 1      | 1    | 15 (X4Y4) & 15' (X4'Y4') |
| Switch Off | 1       | 1 | 1 | 1 | 1      | 0    | 15 (X4Y4) & 15' (X4'Y4') |
| No Change  | X       | X | X | X | 0      | X    | X X X X                  |

1 = High Level; 0 = Low Level; X = Don't Care

### CONTROL TRUTH TABLE FOR CD22102

| Function                      | Address |   |   |   | $K_a$ | $K_b$ | Select                   |
|-------------------------------|---------|---|---|---|-------|-------|--------------------------|
|                               | A       | B | C | D |       |       |                          |
| Switch On                     | 1       | 1 | 1 | 1 | 1     | 0     | 15 (X4Y4) & 15' (X4'Y4') |
| Switch Off                    | 1       | 1 | 1 | 1 | 0     | 1     | 15 (X4Y4) & 15' (X4'Y4') |
| All Switches Off <sup>#</sup> | X       | X | X | X | 1     | 1     | All                      |
| No Change                     | X       | X | X | X | 0     | 0     | X X X X                  |

1 = High Level; 0 = Low Level; X = Don't Care

<sup>#</sup> In the event that  $K_a$  and  $K_b$  are changed from levels 1,1 to 0,0  $K_b$  should not be allowed to go to 0 before  $K_a$ , otherwise a switch which was off will inadvertently be turned on.

# CD22101, CD22102

## STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC                                 | CONDITIONS   | LIMITS at Indicated Temperature (°C)  |                        |       |      |      |      |      | Units             |      |    |
|--|--|---|------------------------|-------|------|------|------|------|-------------------|------|----|
|  |  | Values at -55,+25,+125,apply to D,F,H pkg<br>Values at -40,+25,+85,apply to E pkg |                        |       |      |      |      |      |                   |      |    |
|  |  | V <sub>IS</sub><br>(V)  | V <sub>DD</sub><br>(V) | -55   | -40  | +85  | +125 | +25  |                   |      |    |
| Min.   | Typ.   |   |                        |       |      |      |      | Max. |                   |      |    |
| <b>CROSSPOINTS</b>                             |  |   |                        |       |      |      |      |      |                   |      |    |
| Quiescent Device Current, I <sub>DD</sub> Max. |  | -   | 5                      | 5     | 5    | 150  | 150  | -    | 0.04              | 5    | μA |
|  |  | -   | 10                     | 10    | 10   | 300  | 300  | -    | 0.04              | 10   |    |
|  |  | -   | 15                     | 20    | 20   | 600  | 600  | -    | 0.04              | 20   |    |
|  |  | -   | 20                     | 100   | 100  | 3000 | 3000 | -    | 0.08              | 100  |    |
| ON Resistance, R <sub>ON</sub> Max.            | Any Switch<br>V <sub>IS</sub> = 0 to V <sub>DD</sub> | -   | 5                      | 475   | 500  | 725  | 800  | -    | 225               | 600  | Ω  |
|  |  | -   | 10                     | 135   | 145  | 205  | 230  | -    | 85                | 180  |    |
|  |  | -   | 12                     | 100   | 110  | 155  | 175  | -    | 75                | 135  |    |
|  |  | -   | 15                     | 70    | 75   | 110  | 125  | -    | 65                | 95   |    |
| ΔON Resistance, ΔR <sub>ON</sub>               | Between any two switches                             | -   | 5                      | -     | -    | -    | -    | -    | 25                | -    | Ω  |
|  |  | -   | 10                     | -     | -    | -    | -    | -    | 10                | -    |    |
|  |  | -   | 12                     | -     | -    | -    | -    | -    | 8                 | -    |    |
|  |  | -   | 15                     | -     | -    | -    | -    | -    | 5                 | -    |    |
| OFF Leakage Current, I <sub>L</sub> Max.       | All switches OFF                                     | 0,18  | 18                     | ±1000 |      |      | -    | ±1   | ±100*             | nA   |    |
| <b>CONTROLS</b>                                |  |   |                        |       |      |      |      |      |                   |      |    |
| Input Low Voltage, V <sub>IL</sub> Max.        | OFF switch<br>I <sub>L</sub> < 0.2 μA;               | -   | 5                      | 1.5   |      |      | -    | -    | 1.5               | V    |    |
|  |  | -   | 10                     | 3     |      |      | -    | -    | 3                 |      |    |
|  |  | -   | 15                     | 4     |      |      | -    | -    | 4                 |      |    |
| Input High Voltage, V <sub>IH</sub> Min.       | ON switch<br>see R <sub>ON</sub> characteristic      | -   | 5                      | 3.5   |      |      | 3.5  | -    | -                 | V    |    |
|  |  | -   | 10                     | 7     |      |      | 7    | -    | -                 |      |    |
|  |  | -   | 15                     | 11    |      |      | 11   | -    | -                 |      |    |
| Input Current, I <sub>IN</sub> Max.            | Any control  | 0,18  | 18                     | ±0.1  | ±0.1 | ±1   | ±1   | -    | ±10 <sup>-5</sup> | ±0.1 | μA |

\* Determined by minimum feasible leakage measurement for automatic testing.

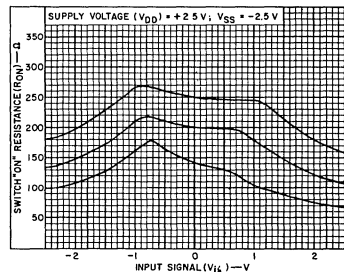


Fig. 3 - Typical ON resistance as a function of input signal voltage at V<sub>DD</sub> = -V<sub>SS</sub> = 2.5 V.

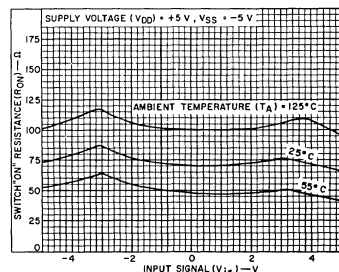


Fig. 4 - Typical ON resistance as a function of input signal voltage at V<sub>DD</sub> = -V<sub>SS</sub> = 5 V.

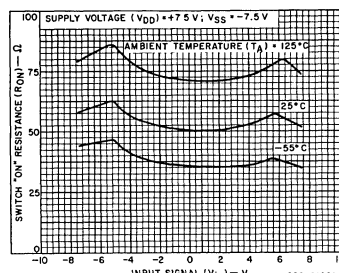


Fig. 5 - Typical ON resistance as a function of input signal voltage at V<sub>DD</sub> = -V<sub>SS</sub> = 7.5 V.

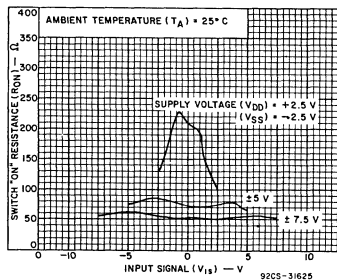


Fig. 6 - Typical ON resistance as a function of input signal voltage at T<sub>A</sub> = 25°C.

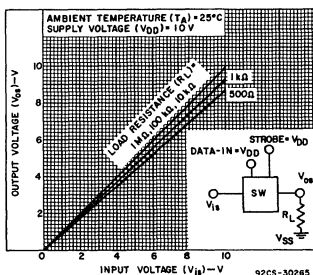


Fig. 7 - Typical switch ON transfer characteristics (1 of 16 switches).

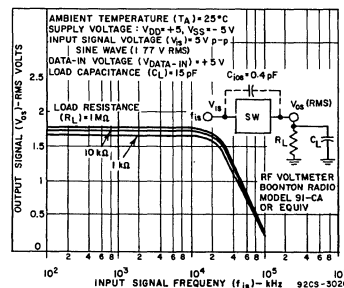


Fig. 8 - Typical ON frequency response characteristics.

# CD22101, CD22102

## DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$

| CHARACTERISTIC   | CONDITIONS  |                     |                              |                 | LIMITS      |                   |                    | UNITS |
|--|---|---------------------|------------------------------|-----------------|-------------|-------------------|--------------------|-------|
|  | $f_{is}$<br>kHz   | $R_L$<br>k $\Omega$ | $V_{is}$ <sup>●</sup><br>(V) | $V_{DD}$<br>(V) | Min.        | Typ.              | Max.               |       |
| <b>CROSSPOINTS</b>   |   |                     |                              |                 |             |                   |                    |       |
| Propagation Delay Time, (Switch ON)<br>Signal Input to Output, $t_{pHL}$ , $t_{pLH}$                                     | —   | 10                  | 5<br>10<br>15                | 5<br>10<br>15   | —<br>—<br>— | 30<br>15<br>10    | 60<br>30<br>20     | ns    |
| $C_L = 50\text{ pF}; t_r, t_f = 20\text{ ns}$  |   |                     |                              |                 |             |                   |                    |       |
| Frequency Response,<br>(Any Switch ON)   | 1   | 1                   | 5                            | 10              | —           | 40                | —                  | MHz   |
| Sine wave input,<br>$20 \log \frac{V_{os}}{V_{is}} = -3\text{ dB}$   |   |                     |                              |                 |             |                   |                    |       |
| Sine Wave Response, (Distortion)   | 1   | 1                   | 2.5                          | 5               | —           | 1                 | —                  | %     |
| 1 1 5 10 — 0.25 —  |   |                     |                              |                 |             |                   |                    |       |
| 1 1 7.5 15 — 0.15 —  |   |                     |                              |                 |             |                   |                    |       |
| Feedthrough<br>All Switches OFF (See Fig. 24)  | 1.6   | 0.6                 | 2 <sup>■</sup>               | 10              | —           | -96               | —                  | dB    |
| Sine wave input  |   |                     |                              |                 |             |                   |                    |       |
| Frequency for Signal Crosstalk<br>Attenuation of 40 dB   | —   | 0.6                 | 1 <sup>■</sup>               | 10              | —           | 2.5               | —                  | MHz   |
| Attenuation of 95 dB (See Fig. 23)   | Sine wave input   |                     |                              |                 | —           | 0.1               | —                  | kHz   |
| Capacitance,<br>$X_n$ to Ground<br>$Y_n$ to Ground<br>Feedthrough  | —   | —                   | —                            | —               | —           | 25                | —                  | pF    |
| — — — — — 60 —   |   |                     |                              |                 |             |                   |                    |       |
| <b>CONTROLS</b>  |   |                     |                              |                 |             |                   |                    |       |
| Propagation Delay Time, High Impedance<br>to High Level or Low Level, $t_{pZH}$ , $t_{pZL}$<br>Strobe to Output, CD22101 | $R_L = 1\text{ k}\Omega$ ,<br>$C_L = 50\text{ pF}$ ,<br>$t_r, t_f = 20\text{ ns}$ |                     | See<br>Fig.                  | 5<br>10<br>15   | —<br>—<br>— | 500<br>230<br>170 | 1000<br>460<br>340 | ns    |
| Data-In to Output, CD22101   |   |                     | 17                           | 5<br>10<br>15   | —<br>—<br>— | 515<br>220<br>170 | 1000<br>440<br>340 |       |
| $K_a$ to Output, CD22102   |   |                     |                              | 5<br>10<br>15   | —<br>—<br>— | 500<br>215<br>160 | 1000<br>430<br>320 |       |
| Address to Output,<br>CD22101, CD22102   |   |                     | 18                           | 5<br>10<br>15   | —<br>—<br>— | 480<br>225<br>155 | 960<br>450<br>300  |       |
| Propagation Delay Time, High Level or<br>Low Level to High Impedance, $t_{pHZ}$ , $t_{pLZ}$<br>Strobe to Output, CD22101 |   |                     |                              | 5<br>10<br>15   | —<br>—<br>— | 450<br>200<br>135 | 900<br>400<br>270  |       |
| $K_b$ to Output, CD22102   |   |                     |                              | 5<br>10<br>15   | —<br>—<br>— | 450<br>200<br>130 | 900<br>400<br>260  |       |
| Data-In to Output, CD22101   |   |                     |                              | 5<br>10<br>15   | —<br>—<br>— | 450<br>165<br>110 | 900<br>330<br>220  |       |
| $K_a \cdot K_b$ to Output, CD22102   |   |                     |                              | 5<br>10<br>15   | —<br>—<br>— | 280<br>130<br>90  | 560<br>260<br>180  |       |

● Peak-to-peak voltage symmetrical about  $V_{DD}$  unless otherwise specified.

■ RMS

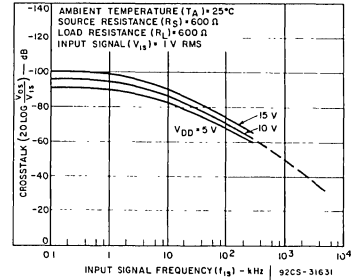


Fig. 9 — Typical crosstalk between switches as a function of signal frequency.

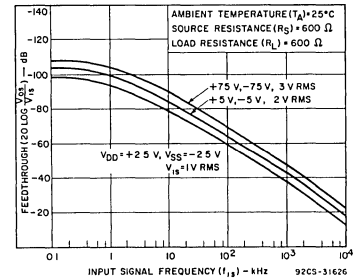


Fig. 10 — Typical feedthrough, any OFF switch as a function of frequency.

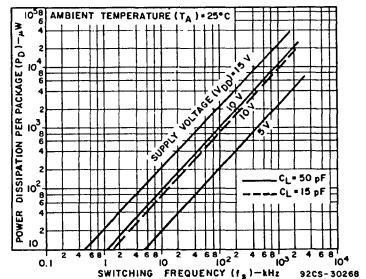
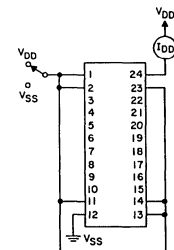


Fig. 11 — Typical dynamic power dissipation as a function of switching frequency for CD22101.



92CS-31627

Fig. 12 — Quiescent current test circuit.

# CD22101, CD22102

## DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$ (cont'd)

| CHARACTERISTIC   | CONDITIONS   |                     |                 | LIMITS          |      |      | UNITS |      |
|--|--|---------------------|-----------------|-----------------|------|------|-------|------|
|  | $f_{is}$<br>kHz  | $R_L$<br>k $\Omega$ | $V_{is}$<br>(V) | $V_{DD}$<br>(V) | Min. | Typ. |       | Max. |
| <b>CONTROLS (cont'd)</b>   |  |                     |                 |                 |      |      |       |      |
| Address to Output,<br>CD22101, CD22102                                     | $R_L = 1\text{ k}$ ,<br>$C_L = 50\text{ pF}$ ,<br>$t_r, t_f = 20\text{ ns}$            | See<br>Fig.         | 18              | 5               | —    | 425  | 850   | ns   |
|  |  |                     | 10              | 10              | —    | 190  | 380   |      |
|  |  |                     | 15              | 15              | —    | 130  | 260   |      |
| Minimum Strobe Pulse Width $t_{W}$<br>CD22101                              |  |                     | 5               | 5               | —    | 260  | 500   |      |
|  |  |                     | 10              | 10              | —    | 120  | 240   |      |
|  |  |                     | 15              | 15              | —    | 80   | 160   |      |
| Address to Strobe Setup or Hold Times,<br>$t_{SU}, t_H$ , CD22101          |  |                     | 19              | 5               | —    | -160 | 0     |      |
|  |  |                     | 10              | 10              | —    | -70  | 0     |      |
|  |  |                     | 15              | 15              | —    | -50  | 0     |      |
| Strobe to Data-In Hold Time,<br>Time, $t_{HHL}; t_{HLL}$ , CD22101         |  |                     | 20              | 5               | —    | 200  | 400   |      |
|  |  |                     | 10              | 10              | —    | 80   | 160   |      |
|  |  |                     | 15              | 15              | —    | 60   | 120   |      |
| Address to $K_a$ and $K_b$ Setup or Hold Times,<br>$t_{SU}, t_H$ , CD22102 |  |                     | 5               | 5               | —    | -160 | 0     |      |
|  |  |                     | 10              | 10              | —    | -70  | 0     |      |
|  |  |                     | 15              | 15              | —    | -50  | 0     |      |
| Minimum $K_a \cdot K_b$ Pulse Width, $t_{W}$<br>CD22102                    |  |                     | 5               | 5               | —    | 375  | 750   |      |
|  |  |                     | 10              | 10              | —    | 160  | 320   |      |
|  |  |                     | 15              | 15              | —    | 110  | 220   |      |
| Minimum $K_a$ Pulse Width, $t_{W}$<br>CD22102                              |  |                     | 5               | 5               | —    | 425  | 850   |      |
|  |  |                     | 10              | 10              | —    | 175  | 350   |      |
|  |  |                     | 15              | 15              | —    | 120  | 240   |      |
| Minimum $K_b$ Pulse Width, $t_{W}$<br>CD22102                              |  |                     | 5               | 5               | —    | 200  | 400   |      |
|  |  |                     | 10              | 10              | —    | 90   | 180   |      |
|  |  |                     | 15              | 15              | —    | 70   | 140   |      |
| Control Crosstalk,<br>Data-In, Address, or Strobe<br>to Output;            | 100  | 10                  | 21              | 5               | —    | 75   | —     |      |
|  | Square wave<br>input = 5 V,<br>$t_r, t_f = 20\text{ ns}$ ,<br>$R_s = 1\text{ k}\Omega$ |                     |                 |                 |      |      |       |      |
| Input Capacitance, $C_{IN}$  | Any Control<br>Input   |                     | —               | —               | 5    | 7.5  | pF    |      |

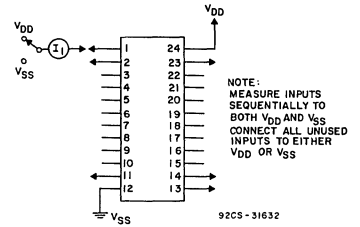


Fig. 13 - Input current test circuit.

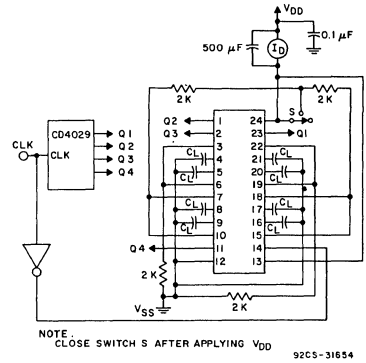


Fig. 14 - Dynamic power dissipation test circuit for CD22101.

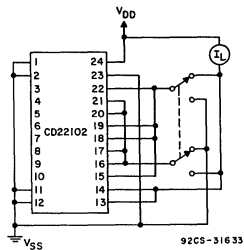


Fig. 15 - OFF switch input or output leakage current test circuit (16 of 32 switches).

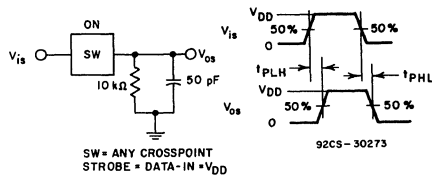


Fig. 16 - Propagation delay time test circuit and waveforms (signal input to signal output, switch ON).

# CD22101, CD22102

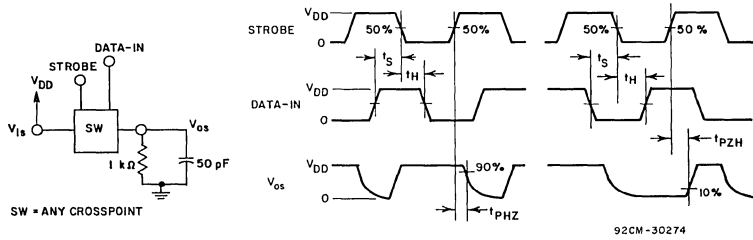


Fig. 17 — Propagation delay time test circuit and waveforms (strobe to signal output, switch Turn-ON or Turn-OFF).

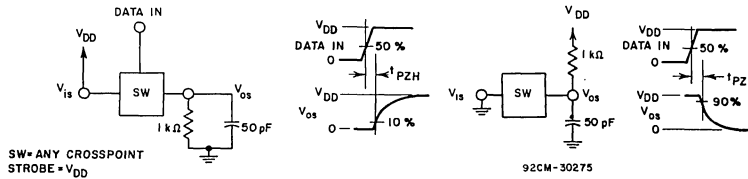


Fig. 18 — Propagation delay time test circuit and waveforms (data-in to signal output, switch Turn-ON to high or low level).

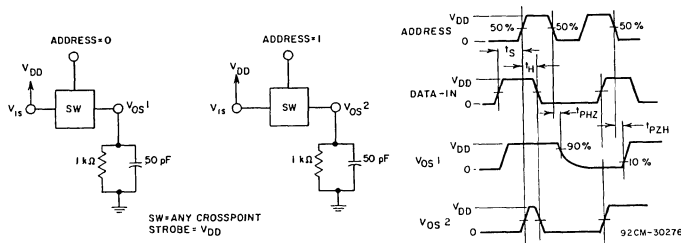
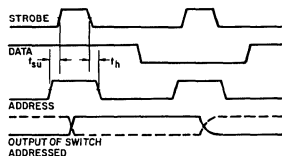


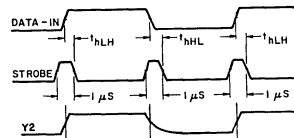
Fig. 19 — Propagation delay time test circuit and waveforms (address to signal output, switch turn-ON or Turn-OFF).



NOTE:  
IF SETUP AND HOLD TIMES PROVIDED ARE TOO SHORT AN UNADDRESSED SWITCH MAY BE TURNED ON OR OFF SIMULTANEOUSLY WITH THE ADDRESSED SWITCH.

92CS-31634

Fig. 20 — Address to strobe setup and hold times.



NOTE:  
SET ALL SWITCHES TO OFF INITIALLY. APPLY V<sub>DD</sub> TO ALL X INPUTS AND RETURN ALL Y OUTPUTS TO V<sub>SS</sub> THROUGH 1K. ADDRESS XIY<sub>2</sub> (A<sub>2</sub>B<sub>2</sub>C<sub>2</sub>) WITH t<sub>IN</sub>=10kHz

92CS-31635

Fig. 21 — Strobe to Data-In hold time t<sub>h</sub> for CD22101.

# CD22101, CD22102

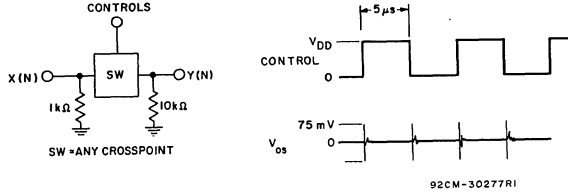


Fig. 22 - Test circuit and waveforms for crosstalk (control input to signal output).

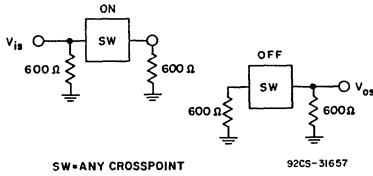


Fig. 23 - Test circuit for crosstalk between switch circuits in the same package.

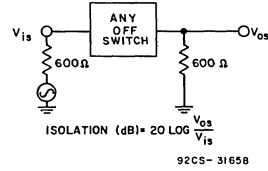
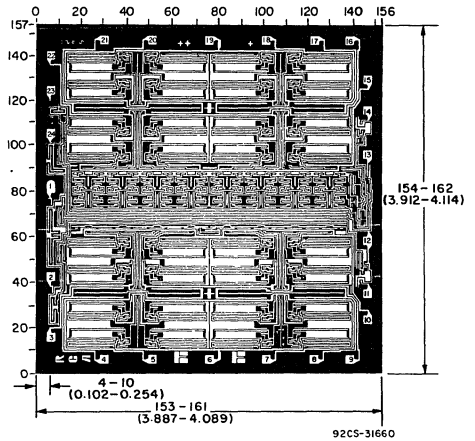
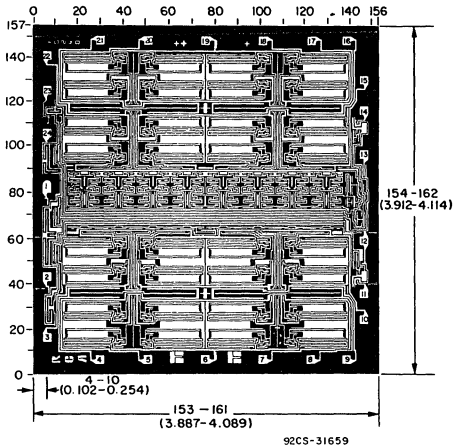


Fig. 24 - Test circuit for feedthrough (any OFF switch).



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

## CMOS HDB3 (High Density Bipolar 3) Transcoder for 2.048/8.448 Mb/s Transmission Applications

August 1991

### Features

- HDB3 Coding and Decoding for Data Rates from 50Kb/s to 10Mb/s in a Manner Consistent with CCITT G703 Recommendations
- HDB3/AMI Transmission Coding/Reception Decoding with Code Error Detection is Performed in Independent Coder and Decoder Sections
- All Transmitter and Receiver Inputs/Outputs are TTL Compatible
- Internal Loop Test Capability

### Description

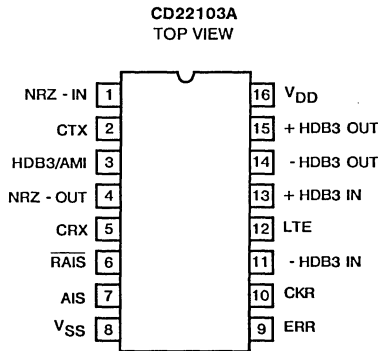
The CD22103A is an LSI SOS integrated circuit which performs the HDB3 transmission coding and reception decoding functions with error detection. It is used in 2.048Mb/s and 8.448Mb/s transmission applications. The CD22103A performs HDB3 coding and decoding for data rates from 50Kb/s to 10Mb/s in a manner consistent with CCITT G703 recommendations.

HDB3 transmission coding/reception decoding with code error detection is performed in independent coder and decoder sections. All transmitter and receiver inputs/outputs are TTL compatible.

The HDB3 transmitter coder codes an NRZ binary unipolar input signal (NRZ-IN) and a synchronous transmission clock (CTX) into two HDB3 binary unipolar RZ output signals (+HDB3 OUT, -HDB3 OUT). The TTL compatible output signals +HDB3 OUT, -HDB3 OUT are externally mixed to generate ternary bipolar HDB3 signals for driving transmission lines.

The receiver decoder converts binary unipolar inputs (+HDB3 IN, -HDB3 IN), which were externally split from ternary bipolar HDB3 signals, and a synchronous clock signal (CRX) into binary unipolar NRZ signals (NRZ-OUT).

### Pinout



### Block Diagram

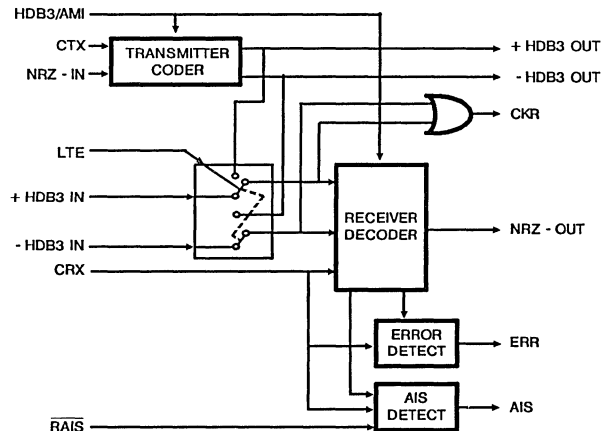


FIGURE 1.



## Specifications CD22103A

Received signals not consistent with HDB3 coding rules are detected as errors. The receiver error output (ERR) is active high during one CRX period of each bit of received data that is inconsistent with HDB3 coding rules.

An input string consisting of all ones (or marks) is detected and signaled by a high level at the Alarm Signal (AIS) output. The AIS output is set to a high level when less than three zeros are received during two consecutive periods of the Reset Alarm Inhibit Signal (RAIS). The AIS output is subsequently reset to a low level when three or more zeros are received during two periods of the reset signal (RAIS).

A diagnostic Loop-Test Mode may be entered by driving the Loop Test Enable Input (LTE) high. In this mode the HDB3 transmitter outputs (+HDB3 OUT, -HDB3 OUT) are internally connected to the HDB3 receiver inputs, and the external HDB3 receiver inputs (+HDB3 IN, -HDB3 IN) are disabled. The NRZ binary output signal (NRZ - OUT) corresponds to the NRZ binary input signal (NRZ - IN) delayed by approximately 8 clock periods.

The Clock Receiver Output (CKR) is the product of the two HDB3 input signals or-ed together. The CRX clock signal may be derived from the CKR signal with external clock extraction circuitry. In the Loop Test Mode (LTE = 1) CKR is the product of the +HDB3 OUT and -HDB3 OUT signals or-ed together.

The CD22103A may also be used to perform the AMI to NRZ coding/decoding function. To use the CD22103A in this mode, the HDB3/AMI control input is driven low.

The RCA-CD22103A operates with a 5 V  $\pm 10\%$  power supply voltage over the full military temperature range at data rates from 50 Kb/s up to 10 Mb/s.

The RCA-CD22103A is similar in function and pin configuration to type MJ1471.

The CD22103A types are supplied in 16-lead hermetic dual-in-line welded-seal ceramic packages (D suffix), 16-lead dual-in-line plastic packages (E suffix).

### MAXIMUM RATINGS, Absolute-Maximum Values:

|   |  |
|---|--|
| DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )   | -0.5 to + 8 V  |
| (Voltages referenced to $V_{SS}$ Terminal)                                    |  |
| INPUT VOLTAGE RANGE, ALL INPUTS   | -0.5 to $V_{DD}$ + 0.5 V                             |
| DC INPUT CURRENT, ANY ONE INPUT   | $\pm 10$ mA  |
| POWER DISSIPATION PER PACKAGE ( $P_D$ )                                       |  |
| For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)                       | 500 mW   |
| For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)                       | Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW |
| For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPE D)                      | 500 mW   |
| For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPE D)                     | Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR                                      |  |
| For $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$         | 100 mW   |
| OPERATING-TEMPERATURE RANGE ( $T_A$ )   |  |
| PACKAGE TYPES D   | -55 to $+125^\circ\text{C}$                          |
| PACKAGE TYPE E  | -40 to $+85^\circ\text{C}$                           |
| STORAGE TEMPERATURE RANGE ( $T_{stg}$ )                                       | -65 to $+150^\circ\text{C}$                          |
| LEAD TEMPERATURE (DURING SOLDERING):  |  |
| At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s max. | $+265^\circ\text{C}$                                 |

### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operating is always within the following ranges:

| CHARACTERISTIC   | LIMITS |      | UNITS |
|--|--------|------|-------|
|  | Min.   | Max. |       |
| DC Supply Voltage Range (For $T_A = \text{Full Package-Temperature Range}$ ) | 4.5    | 5.5  | V     |

## Specifications CD22103A

### STATIC ELECTRICAL CHARACTERISTICS, $V_{DD} = 5\text{ V} \pm 10\%$ ; $T_A = 25^\circ\text{C}$

| CHARACTERISTIC  | SYMBOL    | LIMITS |      |      | UNITS         |
|---|-----------|--------|------|------|---------------|
|   |           | Min.   | Typ. | Max. |               |
| Quiescent Device Current  | $I_{DD}$  | —      | —    | 100  | $\mu\text{A}$ |
| Operating Device Current ( $f_{CL} = 10\text{ MHz}$ )               |           | —      | —    | 8    | mA            |
| HDB3 Output Low (Sink) Current ( $V_{OL} = 0.5\text{ V}$ )          | $I_{OL1}$ | 1.6    | —    | —    |               |
| HDB3 Output High (Source) Current ( $V_{OH} = 2.8\text{ V}$ )       | $I_{OH1}$ | -10    | —    | —    |               |
| All Other Outputs Low (Sink) Current ( $V_{OL} = 0.5\text{ V}$ )    | $I_{OL2}$ | 1.6    | —    | —    |               |
| All Other Outputs High (Source) Current ( $V_{OH} = 2.8\text{ V}$ ) | $I_{OH2}$ | -1.6   | —    | —    |               |
| Input Low Current   | $I_{IL}$  | —      | —    | -1   | $\mu\text{A}$ |
| Input High Current  | $I_{IH}$  | —      | —    | 1    |               |
| Input Low Voltage (Max.)  | $V_{IL}$  | —      | —    | 0.8  | V             |
| Input High Voltage (Min.)   | $V_{IH}$  | 2      | —    | —    |               |
| Input Capacitance   | $C_{IN}$  | —      | —    | 5    | pF            |

### DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A$ range of $-40^\circ\text{C}$ to $+85^\circ\text{C}$ for plastic package; $-55^\circ\text{C}$ to $+125^\circ\text{C}$ for ceramic package; $V_{DD}$ range of 4.5 V to 5.5 V, $C_L = 15\text{ pF}$

| CHARACTERISTIC  | SYMBOL             | LIMITS |      |      | UNITS         |
|---|--------------------|--------|------|------|---------------|
|   |                    | Min.   | Typ. | Max. |               |
| INPUT   |                    |        |      |      |               |
| CTX, CRX Input Frequency                                | $f_{CTX}, f_{CRX}$ | 0.05   | —    | 10   | MHz           |
| CTX, CRX Input Rise Time *<br>Fall Time *               | $t_{rcl}$          | —      | —    | 1    | $\mu\text{s}$ |
|   | $t_{fcl}$          | —      | —    | 1    |               |
| NRZ-IN to CTX<br>Data Setup Time *<br>Data Hold Time *  | $t_s$              | 15     | —    | —    | ns            |
|   | $t_H$              | 15     | —    | —    |               |
| HDB3 IN to CRX<br>Data Setup Time §<br>Data Hold Time * | $t_s$              | 15     | —    | —    | ns            |
|   | $t_H$              | 0      | —    | —    |               |
| CRX to CKR<br>CRX = 8.448 MHz<br>Pretrigger •<br>Delay  | $t_p$              | —      | —    | 20   | ns            |
|   | $t_d$              | —      | —    | 20   |               |

\* See Fig. 4

§ See Fig. 5

• See Fig. 6

## Specifications CD22103A

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A$  range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  for plastic package;  
 $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  for ceramic package;  $V_{DD}$  range of 4.5 V to 5.5 V,  $C_L = 15\text{ pF}$

| CHARACTERISTIC  | SYMBOL               | LIMITS    |        |           | UNITS              |
|---|----------------------|-----------|--------|-----------|--------------------|
|   |                      | Min.      | Typ.   | Max.      |                    |
| <b>OUTPUT</b>   |                      |           |        |           |                    |
| Transmitter Coder<br>CTX to HDB3 OUT:<br>Data Propagation Delay Time *<br>Handling Delay Time                           | $t_{DD}$<br>$t_{HD}$ | —<br>—    | —<br>4 | 90<br>—   | ns<br>clock period |
| HDB3 OUT Output Pulse Width *<br>(Clock duty cycle = 50%)<br>$f_{CL} = 2.048\text{ MHz}$<br>$f_{CL} = 8.448\text{ MHz}$ | $t_w$<br>$t_w$       | 238<br>53 | —<br>— | 260<br>65 | ns                 |
| Receiver Decoder<br>CRX to NRZ OUT:<br>Data Propagation Delay Times §<br>Handling Delay Time #                          | $t_{DD}$<br>$t_{HD}$ | —<br>—    | —<br>4 | 90<br>—   | ns<br>clock period |
| HDB3 IN to CKR<br>HDB3 Propagation Delay Time §<br>LTE = 0<br>LTE = 1   | $t_{IN\ CKR}$        | —<br>—    | —<br>— | 65<br>30  | ns                 |

§ See Fig. 5

\* See Fig. 4

§ See Fig. 2

# See Fig. 3

### TRANSCODER OPERATION

#### Transmitter Coder (See Fig. 2)

The HDB3/AMI transmitter coder operates on 4-bit serial strings of NRZ binary data and a synchronous transmitter clock (CTX). NRZ binary data is serially clocked into the

transmitter on the negative transition of the (CTX) clock. HDB3/AMI coding is performed on the 4-bit string, and HDB3/AMI binary output data is clocked out to the (+HDB3 OUT, -HDB3 OUT) outputs on the positive transition of the transmitter clock (CTX) 4 clock pulses after the data appeared at the (NRZ-IN) input.

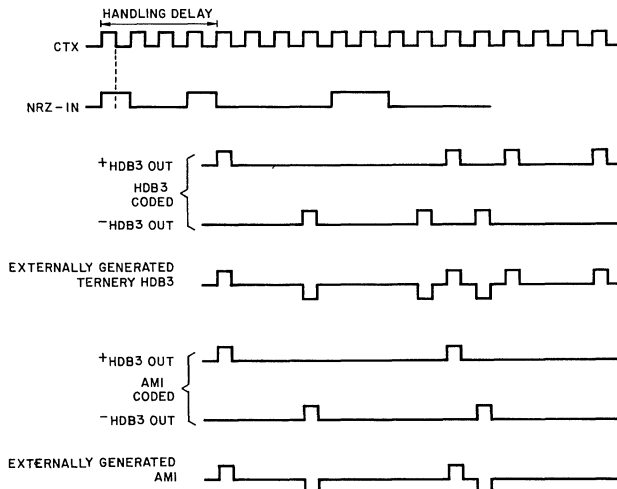


Fig. 2 - Transmitter coder operation timing waveforms - NRZ to HDB3/AMI coding.

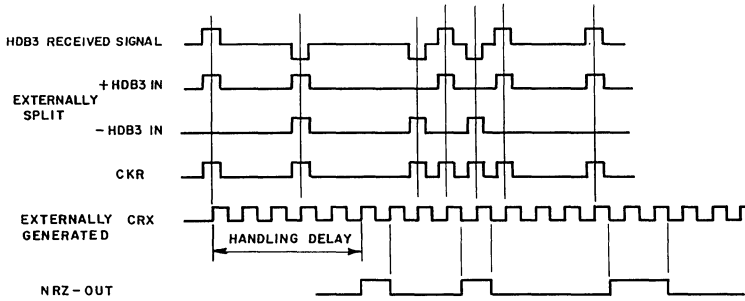
92CS-33992

# CD22103A

## Receiver Decoder (See Fig. 3)

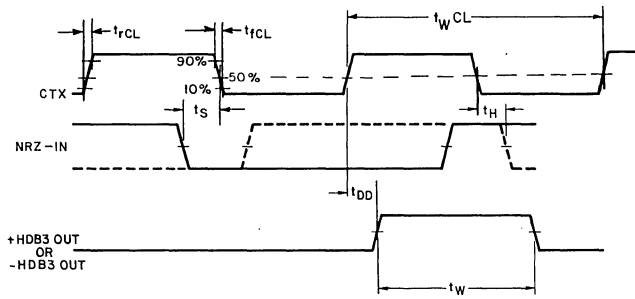
The HDB3/AMI receiver decoder operates on 4-bit serial strings of binary coded HDB3/AMI signals, and a synchronous receiver clock (CRX), HDB3/AMI binary data is serially clocked into the receiver on the positive transition

of the (CRX) clock. HDB3/AMI decoding is performed on the 4-bit string, and NRZ binary output data is clocked out to the (NRZ-OUT) output on the positive transition of the receiver clock (CRX) 4 clock pulses after the data appeared at the (+ HDB3 IN, -HDB3 IN) inputs.



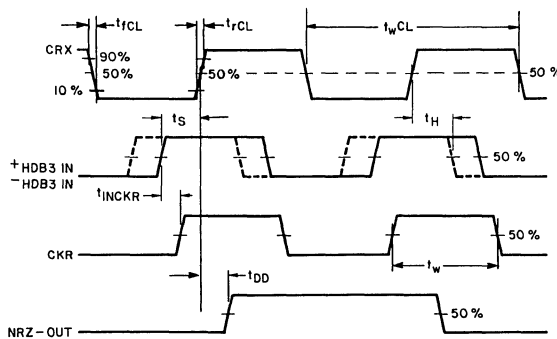
92CS-33989R1

Fig. 3 - Receiver decoder operation timing waveforms - HDB3 to NRZ decoding.



92CS-33993R2

Fig. 4 - Transmitter coder timing waveforms.



92CS-33994R2

Fig. 5 - Input requirements and output characteristics.

## CD22103A

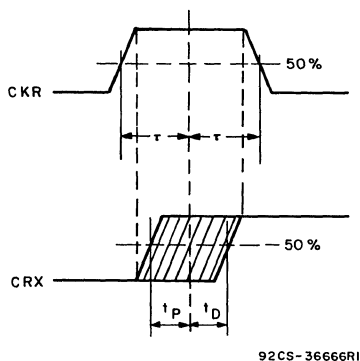


Fig. 6 - CRX reconstruction requirements.

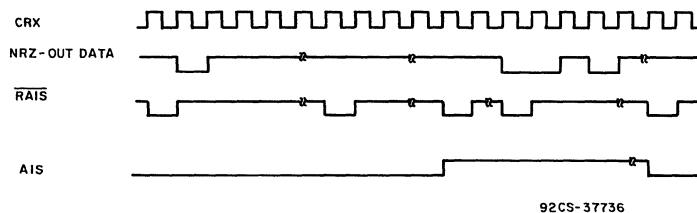


Fig. 7 - Receiver alarm-inhibit-signals timing waveforms.

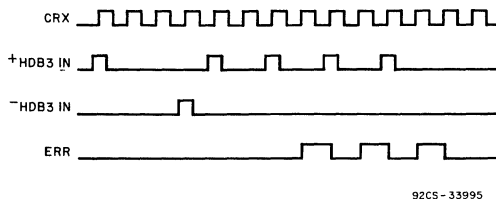


Fig. 8 - Receiver error-signals timing waveforms.

### Definition of HDB3 Code Used in CD22103A HDB3 Transcoder (As Per CCITT G703 Annex Recommendations) and Error Detection

Coding of a binary signal into an HDB3 signal is done according to the following rules:

1. HDB3 signal is pseudoternary; the three states are denoted B+, B-, and 0.
2. Spaces in the binary signal are coded as spaces in the HDB3 signal. For strings of four spaces, however, special rules apply (See Item 4 below).
3. Marks in the binary signal are coded alternately as B+ and B- in the HDB3 signal (alternate mark inversion). Violations of the rule of alternate mark inversion are introduced when coding strings of four spaces (See Item 4 below).
4. Strings of four spaces in the binary signal are coded according to the following rules:

- A) The first space of a string is coded as a space if the polarity of the preceding mark of the HDB3 signal has a polarity opposite to the preceding violation and is not a violation by itself; it is coded as a mark, i.e., not a violation (i.e., B+ or B-), if the preceding mark of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation.  
This rule ensures that successive violations are of alternate polarity so that no dc component is introduced.
- B) The second and third spaces of a string are always coded as spaces.
- C) The last space of a string of four is always coded as a mark, the polarity of which is such that it violates the rule of alternate mark inversion. Such violations are denoted V+ or V- according to their polarity.

## CD22103A

The CD22103A is designed to code and decode HDB3 signals which are coded as binary digital signals (NRZ-IN) and (+ HDB3 IN, -HDB3 IN), accompanied by sampling clocks (CTX) and (CRX). The two binary coded HDB3 outputs, (+ HDB3 OUT, -HDB3 OUT) may be externally mixed to create the ternary HDB3 signals (See Fig. 2).

The two binary HDB3 input signals have been split from the input ternary HDB3 in an external line receiver.

### Error Detection

Received HDB3/AMI binary input signals are checked for coding violations, and an error signal (ERR) is generated as described below.

### HDB3 Signals HDB3/AMI = High

The error signal (ERR) is flagged high for one CTX period if a violation pulse ( $\pm V$ ) is received of the same polarity as the last received violation pulse.

A violation pulse ( $\pm V$ ) is considered a reception error and does not cause replacement of the last string of 4 bits to zeros, if:

The received 4 data bits previous to reception of the violation pulse have not been the sequence BX00 (where X = don't care). The error signal (ERR) remains low.

### NOTES:

The data sequences B000V and BB00V are valid HDB3 codings of the NRZ binary sequence 10000.

The error signal (ERR) count, is the accurate number of all single bit errors.

### AMI Signals HDB3/AMI = Low

A coding error (ERR) is signaled when a violation pulse (+V) is received.

### In either the HDB3 or AMI mode:

When high levels appear simultaneously on both HDB3 inputs (+ HDB3 IN, -HDB3 IN) a logical one is assumed in the HDB3/AMI input stream and the error signal (ERR) goes high for the duration of the violation.

### Alarm Inhibit Signal

The alarm output (AIS) is set high if in two successive periods of the external Reset Alarm Signal, ( $\overline{\text{RAIS}}$ ), less than three zeros are received.

The alarm output (AIS) is reset low when three or more zeros are received during two reset alarm signal periods.

August 1991

## 5V Low-Power DTMF Receiver

### Features

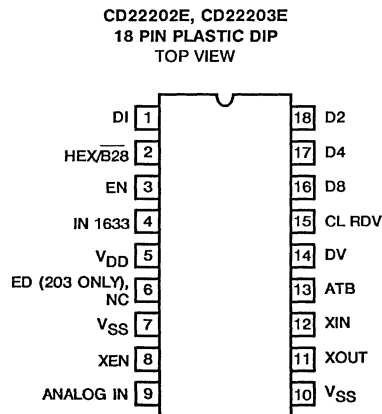
- Central-Office Quality
- No Front-End Band Splitting Filters Required
- Single, Low-Tolerance, 5V Supply
- Detects Either 12 or 16 Standard DTMF Digits
- Uses Inexpensive 3.579545MHz Crystal for Reference
- Excellent Speech Immunity
- Output in Either 4-Bit Hexadecimal Code or Binary Coded 2-of-8
- Synchronous or Handshake Interface
- Three-State Outputs
- Excellent Latch-Up Immunity

### Description

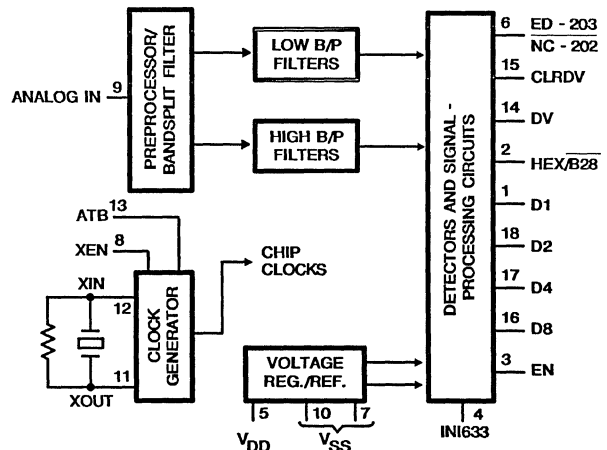
The CD22202E and CD22203E complete dual-tone multiple frequency (DTMF) receivers detect a selectable group of 12 or 16 standard digits. No front-end pre-filtering is needed. The only externally-required components are an inexpensive 3.579545MHz TV "colorburst" crystal (for frequency reference) and a bias resistor. Extremely high system density is possible through the use of the clock output of a crystal-connected CD22202E/CD22203E receiver to drive the time bases of additional receivers. This is a monolithic integrated circuit fabricated with low-power, complementary-symmetry CMOS processing. It only requires a single low-tolerance power supply and is packaged in a standard 18 pin dual-in-line plastic package (E suffix).

The CD22202E and CD22203E employ state-of-the-art circuit technology to combine the digital and analog functions on the same CMOS chip using a standard digital semiconductor process. The analog input is preprocessed by 60Hz reject and band-splitting filters and then hard-limited to provide AGC. Eight Bandpass filters detect the individual tones. The digital post-processor times the tone durations and provides the correctly coded digital outputs. Outputs interface directly to standard CMOS circuitry and are tri-state enabled to facilitate bus-oriented architectures.

### Pinout



### Functional Diagram



## Specifications CD22202E, CD22203E

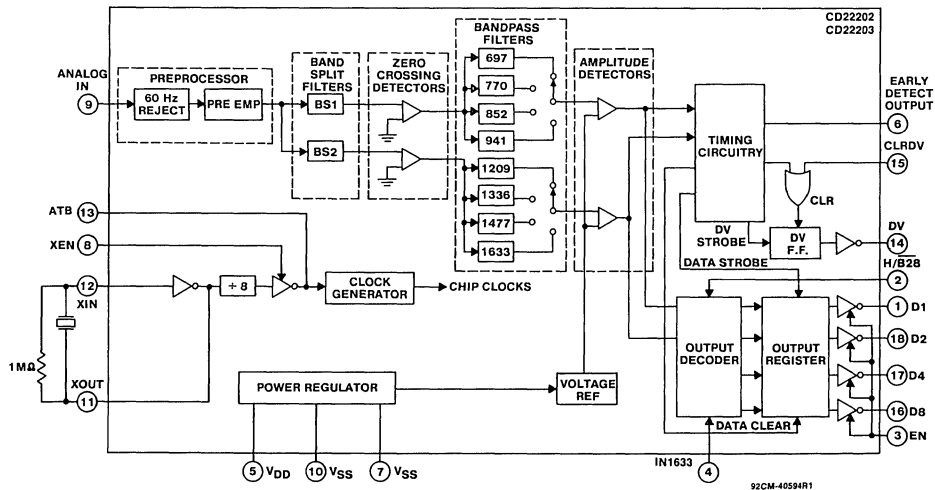
### MAXIMUM RATINGS, Absolute-Maximum Values:

|   |   |
|---|---|
| DC SUPPLY-VOLTAGE ( $V_{DD}$ ) (Referenced to $V_{SS}$ terminal)                                | +7 V                                      |
| OPERATING-TEMPERATURE RANGE ( $T_A$ )   | 0° C to 70° C                             |
| STORAGE-TEMPERATURE RANGE ( $T_{stg}$ )   | -65 to +150° C                            |
| POWER DISSIPATION ( $P_D$ ) @ $T_A = 25^\circ$ C (Derate above $T_A = 25^\circ$ C @ 6.25 mW/°C) | 65 mW                                     |
| INPUT VOLTAGE RANGE, ALL INPUTS EXCEPT ANALOG IN  | ( $V_{DD} + 0.5$ V) to -0.5 V             |
| ANALOG IN VOLTAGE RANGE   | ( $V_{DD} + 0.5$ V) to ( $V_{DD} - 10$ V) |
| DC CURRENT INTO ANY INPUT OR OUTPUT   | $\pm 20$ mA                               |
| LEAD TEMPERATURE (DURING SOLDERING):  |   |
| At distance $1/16 \pm 1/32$ in. ( $1.59 \pm 0.79$ mm) from case for 10 s max.                   | +265° C                                   |

Note: Unused inputs must be connected to  $V_{DD}$  or  $V_{SS}$  as appropriate.

### ELECTRICAL CHARACTERISTICS (0° C $\leq T_A \leq 70^\circ$ C, $V_{DD} = 5$ V $\pm 10\%$ )

| PARAMETER                        | CONDITIONS   | MIN.                      | TYP.           | MAX.                     | UNITS                                     |
|----------------------------------|--|---------------------------|----------------|--------------------------|---|
| Frequency Detect Bandwidth       |  | $\pm(1.5+2\text{Hz})$     | $\pm 2.3$      | $\pm 3.5$                | % of $f_t$                                |
| Amplitude for Detection          | each tone  | -32                       |                | -2                       | dBm<br>referenced to 600 $\Omega$         |
| Minimum Acceptable Twist         | twist = $\frac{\text{high tone}}{\text{low tone}}$         | -10                       |                | +10                      | dB  |
| 60-Hz Tolerance                  |  |                           |                | 0.8                      | V rms                                     |
| Dial Tone Tolerance              | "precise" dial tone  |                           |                | 0 dB                     | dB referenced to<br>lower amplitude tone  |
| Talk Off                         | MITEL tape #CM 7290  |                           | 2              |                          | hits                                      |
| Digital Outputs<br>(except XOUT) | "0" level, 400 $\mu$ A load<br>"1" level, 200 $\mu$ A load | 0<br>$V_{DD} - 0.5$       |                | 0.5<br>$V_{DD}$          | V   |
| Digital Inputs                   | "0" level<br>"1" level                                     | 0<br>0.7 $V_{DD}$         |                | 0.3 $V_{DD}$<br>$V_{DD}$ | V   |
| Power Supply Noise               | wide band  |                           |                | 10                       | mV p-p                                    |
| Supply Current                   | $T_A = 25^\circ$ C   |                           | 10             | 16                       | mA  |
| Noise Tolerance                  | MITEL tape<br>#CM 7290                                     |                           |                | -12                      | dB referenced to<br>lowest amplitude tone |
| Input Impedance                  | $V_{DD} \geq V_{IN} \geq (V_{DD} - 10)$                    | 100 k $\Omega$ //<br>15pF | 300 k $\Omega$ |                          |   |



NOTE: PIN 6: EARLY DETECT OUTPUT ON CD22203 ONLY.

Fig. 1 - Functional block diagram.



## CD22202E, CD22203E

### ANALOG IN

The Analog In pin accepts the analog input. It is internally biased so that the input signal may be either AC or DC coupled, as long as it does not exceed the positive supply voltage. Proper input coupling is illustrated below.

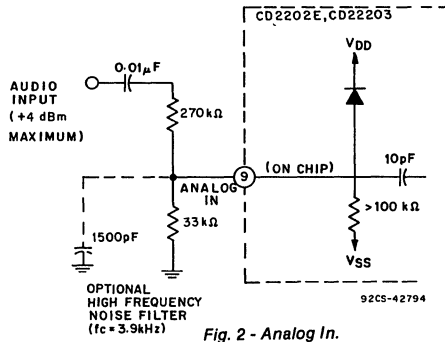


Fig. 2 - Analog In.

The CD22202E and CD22203E is designed to accept sinusoidal input waveforms, but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics that are at least 20 dB below the fundamental.

### CRYSTAL OSCILLATOR

The CD22202E and CD22203E contains an on-board inverter with sufficient gain to provide oscillation when connected to a low-cost television "color-burst" (3.579545-MHz) crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1-Megohm resistor is also connected between these pins in this mode. ATB is a clock-frequency output. Other CD22202E and CD22203E devices may use the same frequency reference by tying their ATB pins to the ATB output of a crystal-connected device. XIN and XEN of the auxiliary devices must then be tied high and low, respectively. Up to ten devices may be run from a single crystal-connected CD22202E and CD22203E as shown below.

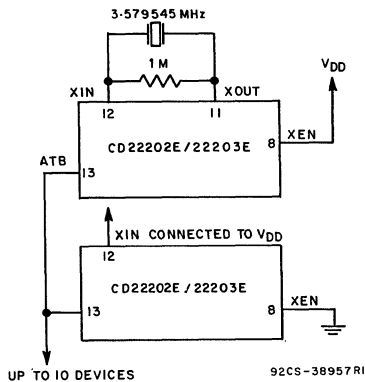


Fig. 3 - Crystal oscillator.

### HEX/B28

This pin selects the format of the digital output code. When HEX/B28 is tied high, the output is hexadecimal. When tied low, the output is binary coded 2-of-8. The following table describes the two output codes.

Table I - Output Codes

| Digit | Hexadecimal |    |    |    | Binary Coded 2-of-8 |    |    |    |
|-------|-------------|----|----|----|---------------------|----|----|----|
|       | D8          | D4 | D2 | D1 | D8                  | D4 | D2 | D1 |
| 1     | 0           | 0  | 0  | 1  | 0                   | 0  | 0  | 0  |
| 2     | 0           | 0  | 1  | 0  | 0                   | 0  | 0  | 1  |
| 3     | 0           | 0  | 1  | 1  | 0                   | 0  | 1  | 0  |
| 4     | 0           | 1  | 0  | 0  | 0                   | 1  | 0  | 0  |
| 5     | 0           | 1  | 0  | 1  | 0                   | 1  | 0  | 1  |
| 6     | 0           | 1  | 1  | 0  | 0                   | 1  | 1  | 0  |
| 7     | 0           | 1  | 1  | 1  | 1                   | 0  | 0  | 0  |
| 8     | 1           | 0  | 0  | 0  | 1                   | 0  | 0  | 1  |
| 9     | 1           | 0  | 0  | 1  | 1                   | 0  | 1  | 0  |
| *     | 1           | 0  | 1  | 1  | 1                   | 1  | 0  | 0  |
| #     | 1           | 1  | 0  | 0  | 1                   | 1  | 1  | 0  |
| A     | 1           | 1  | 0  | 1  | 0                   | 0  | 1  | 1  |
| B     | 1           | 1  | 1  | 0  | 0                   | 1  | 1  | 1  |
| C     | 1           | 1  | 1  | 1  | 1                   | 0  | 1  | 1  |
| D     | 0           | 0  | 0  | 0  | 1                   | 1  | 1  | 1  |

### ED

This pin, on the CD22203E only, indicates the presence of frequencies which are likely to be DTMF digits, but have not yet been verified by a DV signal. It is comparable to a "button-down" output, and it is useful as an EARLY DETECT signal to interrupt a microprocessor for digit storage and validation.

### DV and CLRDV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, and D8. DV remains high until a valid pause occurs or CLRDV is raised high, whichever is sooner. This handshake can save microprocessor time.

### OUTPUTS D1, D2, D4, D8 and EN

Outputs D1, D2, D4, D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedance) when disabled by pulling EN low. These digital outputs provide the code corresponding to the detected digit in the format programmed by the HEX/B28 pin. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed.

### DTMF DIALING MATRIX

|       | Col 0   | Col 1   | Col 2   | Col 3   |
|-------|---------|---------|---------|---------|
|       | 1209 Hz | 1336 Hz | 1477 Hz | 1633 Hz |
| Row 0 | 1       | 2       | 3       | A       |
| Row 1 | 4       | 5       | 6       | B       |
| Row 2 | 7       | 8       | 9       | C       |
| Row 3 | *       | 0       | #       | D       |

### Note:

Column 3 is for special applications and is not normally used in telephone dialing.

## CD22202E, CD22203E

### IN1633

When tied high, this pin inhibits detection of tone pairs containing the 1633-Hz component. For detection of all 16 standard digits, IN1633 must be tied low.

### N/C PIN

This pin has no internal connection and should be left floating.

### DIGITAL INPUTS AND OUTPUTS

All digital inputs and outputs of the DTMF receivers are represented by the schematic below. Only the "analog in" pin is different, and is described above. Care must be exercised not to exceed the voltage or current ratings on these pins as listed in the "maximum ratings" section.

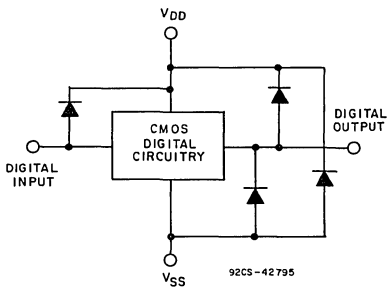


Fig. 4 - Digital inputs and outputs.

### INPUT FILTER

The CD22202E and CD22203E will tolerate total input noise of a maximum of 12 dB below the lowest-amplitude tone. For most telephone applications, the combination of the high-frequency attenuation of the telephone line and internal band-limiting make special circuitry at the input to these receivers unnecessary. However, noise near the 56 kHz internal sampling frequency will be aliased (folded back) into the audio spectrum, so if excessive noise is present above 28 kHz, the simple RC filter shown below may be used to band-limit the incoming signal. The cut-off frequency is 3.9 kHz.

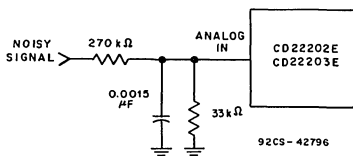


Fig. 5 - Filter for use in extreme high frequency input noise environment.

Noise will also be reduced by placing a grounded trace around XIN and XOUT pins on the circuit board layout when using a crystal. It is important to note that XOUT is not intended to drive an additional device. XIN may be driven externally; in this case, leave XOUT floating.

### TIMING WAVEFORMS

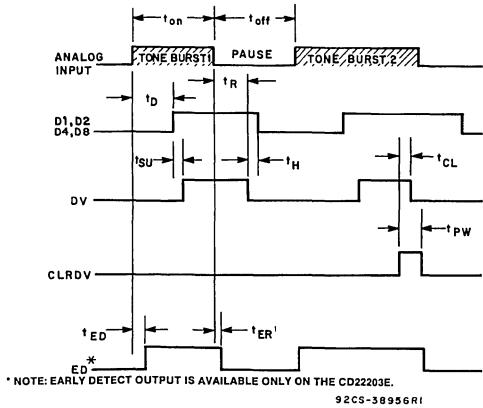


Fig. 6 - Timing waveforms.

| PARAMETER                   | SYMBOL    | MIN. | TYP. | MAX. | UNITS |
|-----------------------------|-----------|------|------|------|-------|
| <b>TONE TIME:</b>           |           |      |      |      |       |
| for detection               | $t_{ON}$  | 40   | —    | —    | ms    |
| for rejection               | $t_{ON}$  | —    | —    | 20   | ms    |
| <b>PAUSE TIME:</b>          |           |      |      |      |       |
| for detection               | $t_{OFF}$ | 40   | —    | —    | ms    |
| for rejection               | $t_{OFF}$ | —    | —    | 20   | ms    |
| DETECT TIME                 | $t_D$     | 25   | —    | 46   | ms    |
| RELEASE TIME                | $t_R$     | 35   | —    | 50   | ms    |
| DATA SETUP TIME             | $t_{SU}$  | 7    | —    | —    | μs    |
| DATA HOLD TIME              | $t_H$     | 4.2  | —    | 5    | ms    |
| DV CLEAR TIME               | $t_{CL}$  | —    | 160  | 250  | ns    |
| CLR DV pulse width          | $t_{PW}$  | 200  | —    | —    | ns    |
| ED Detect Time              | $t_{ED}$  | 7    | —    | 22   | ms    |
| ED Release Time             | $t_{ER}$  | 2    | —    | 18   | ms    |
| OUTPUT ENABLE TIME          | —         | —    | 200  | 300  | ns    |
| $C_L=50$ pF,<br>$R_L=1$ kΩ  | —         | —    | 150  | 200  | ns    |
| OUTPUT DIS-ABLE TIME        | —         | —    | 150  | 200  | ns    |
| $C_L=35$ pF,<br>$R_L=500$ Ω | —         | —    | 200  | 300  | ns    |
| OUTPUT RISE TIME            | —         | —    | 200  | 300  | ns    |
| $C_L=50$ pF                 | —         | —    | 160  | 250  | ns    |
| OUTPUT FALL TIME            | —         | —    | 160  | 250  | ns    |
| $C_L=50$ pF                 | —         | —    | 160  | 250  | ns    |

## CD22202E, CD22203E

### GUARD TIME

Whenever the DTMF receiver is continually monitoring a voice channel containing distorted or musical voices or tones, additional guard time may be added in order to prevent false decoding. This may be done in software by verifying that both ED and DV are present simultaneously for about 55 ms. An appropriate guard time should be

selected to balance the fastest expected dialing speed against the rejection of distorted or musical voices or tones (most autodialers operate in the 65 to 75 ms range although a few generate 50 ms tones). A hardware guard-time circuit is shown below. R3 and R4 should keep the voice amplitude as low as practical, while R2 and R5 adjust detection speed.

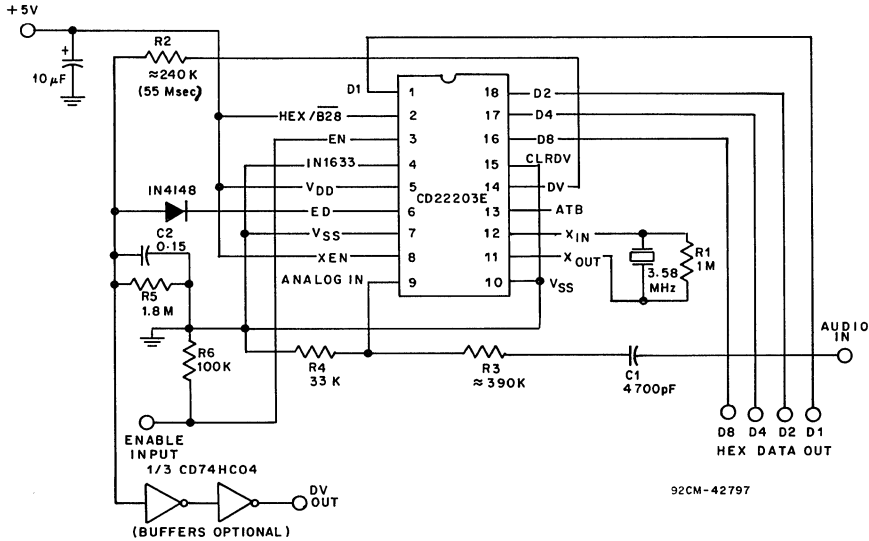


Fig. 7 - CD22203 DTMF receiver with guard time circuit to provide exceptional talk-off performance.

### OPERATING AND HANDLING CONSIDERATIONS

#### 1. Handling

All inputs and outputs of RCA CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."

#### 2. Operating

##### Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause  $V_{DD} - V_{SS}$  to exceed the absolute maximum rating.

##### Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than  $V_{DD}$  nor less than  $V_{SS}$ . Input currents must not exceed 20 mA even when the power supply is off.

##### Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either  $V_{DD}$  or  $V_{SS}$ , whichever is appropriate.

##### Output Short Circuits

Shorting of outputs to  $V_{DD}$  or  $V_{SS}$  may damage CMOS devices by exceeding the maximum device dissipation.

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### Features

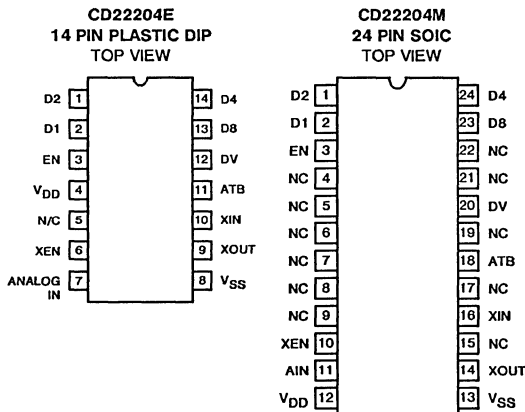
- No Front-End Band Splitting Filters Required
- Single Low-Tolerance 5V Supply
- Three-State Outputs for Microprocessor-Based Systems
- Detects all 16 Standard DTMF Digits
- Uses Inexpensive 3.579545MHz Crystal
- Excellent Speech Immunity
- Output in 4-Bit Hexadecimal Code
- Excellent Latch-Up Immunity

### Description

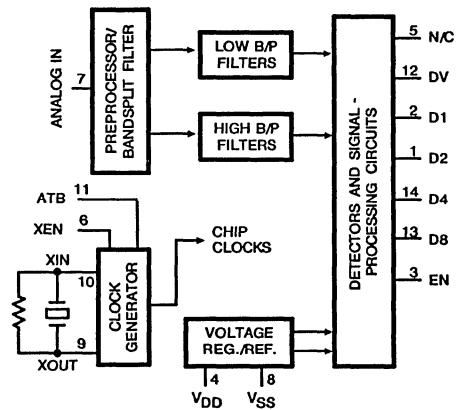
The CD22204 complete dual-tone multiple-frequency (DTMF) receiver detects a selectable group of 12 or 16 standard digits. No front-end pre-filtering is needed. The only externally-required components are an inexpensive 3.579545MHz TV "colorburst" crystal (for frequency reference) and a bias resistor. Extremely high system density is possible through the use of the Alternate Time Base (ATB) output of a crystal-connected CD22204 receiver to drive the time bases of up to 10 additional receivers. This is a monolithic integrated circuit fabricated with low-power, complementary-symmetry CMOS processing. It only requires a single power supply and is packaged in either a 14 pin dual-in-line plastic package (E suffix) or a 24 pin plastic SOIC (M suffix).

The CD22204 employs state-of-the-art "switched-capacitor" filter technology, resulting in approximately 40 poles of filtering and digital circuitry on the same CMOS chip. The analog input is preprocessed by 60Hz reject and band-splitting filters and then zero-cross detected to provide AGC. Eight bandpass filters detect the individual tones. Digital processing is used to measure the tone and pause durations and provides the correctly coded and timed digital outputs. The outputs interface directly to standard CMOS circuitry and are tri-state enabled to facilitate bus-oriented architectures.

### Pinouts



### Functional Diagram



# CD22204

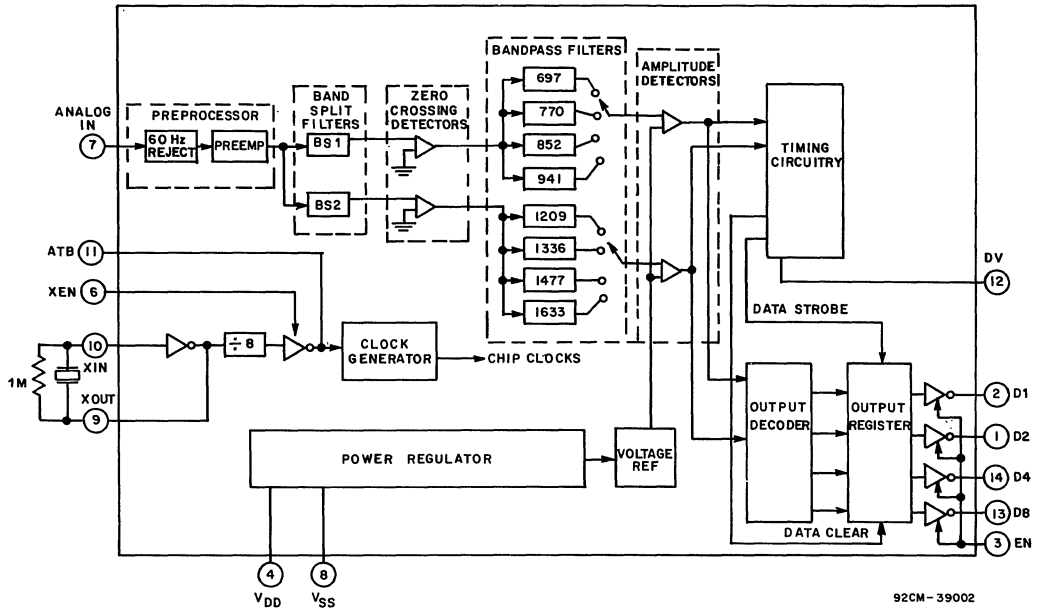


Fig. 1 - Functional Block Diagram

## Specifications CD22204

### MAXIMUM RATINGS, Absolute-Maximum Values:

|   |   |
|---|---|
| DC SUPPLY-VOLTAGE ( $V_{DD}$ ) (Referenced to $V_{SS}$ terminal) .....                      | +7 V                                    |
| OPERATING-TEMPERATURE RANGE ( $T_A$ ) .....   | 0° C to 70° C                           |
| STORAGE-TEMPERATURE RANGE ( $T_{stg}$ ) .....   | -65 to +150° C                          |
| POWER DISSIPATION ( $P_D$ ) @ $T_A = 25° C$ (Derate above $T_A = 25° C$ @ 6.25 mW/°C) ..... | 65 mW                                   |
| INPUT VOLTAGE RANGE, ALL INPUTS EXCEPT ANALOG IN .....                                      | ( $V_{DD} + 0.5 V$ ) to -0.5 V          |
| ANALOG IN VOLTAGE RANGE .....   | ( $V_{DD} + 0.5 V$ ) to $V_{DD} - 10 V$ |
| DC CURRENT INTO ANY INPUT OR OUTPUT .....   | ±20 mA                                  |
| LEAD TEMPERATURE (DURING SOLDERING):  |   |
| At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ....                   | +265° C                                 |

Note: Unused inputs must be connected to  $V_{DD}$  or  $V_{SS}$  as appropriate

### ELECTRICAL CHARACTERISTICS (0° C ≤ $T_A$ ≤ 70° C, $V_{DD} = 5 V \pm 10\%$ )

| PARAMETER                         | CONDITIONS                                      | MIN.                | TYP.   | MAX.                     | UNITS                                     |
|-----------------------------------|---|---------------------|--------|--------------------------|---|
| Frequency Detect Bandwidth        |   | ±(1.5 + 2 Hz)       | ±2.3   | ±3.5                     | % of $f_o$                                |
| Amplitude for Detection           | each tone                                       | -32                 |        | -2                       | dBm<br>referenced to 600 Ω                |
| Minimum Acceptable Twist          | high tone<br>twist = _____<br>low tone          | -8                  |        | +4                       | dB  |
| 60-Hz Tolerance                   |   |                     |        | 0.8                      | Vrms                                      |
| Dial Tone Tolerance               | "precise" dial tone                             |                     |        | 0dB                      | dB referenced to<br>lower amplitude tone  |
| Talk Off                          | MITEL tape<br>#CM 7290                          |                     | 2      |                          | hits                                      |
| Digital Outputs<br>(except XOOUT) | "0" level 400 μA load<br>"1" level, 200 μA load | 0<br>$V_{DD} - 0.5$ |        | 0.5<br>$V_{DD}$          | Volts<br>Volts                            |
| Digital Inputs                    | "0" level<br>"1" level                          | 0<br>0.7 $V_{DD}$   |        | 0.3 $V_{DD}$<br>$V_{DD}$ | Volts<br>Volts                            |
| Power Supply Noise                | wide band                                       |                     |        | 10                       | mV p-p                                    |
| Supply Current                    | $T_A = 25° C$                                   |                     | 10     | 20                       | mA  |
| Noise Tolerance                   | MITEL tape<br>#CM 7290                          |                     |        | -12                      | dB referenced to<br>lowest amplitude tone |
| Input Impedance                   | $V_{DD} \geq V_{IN} \geq V_{DD} - 10$           | 100 kΩ/15pF         | 300 kΩ |                          |   |

9

TELECOM

# CD22204

## ANALOG IN

The Analog In pin accepts the analog input. It is internally biased so that the input signal may be either AC or DC coupled, as long as it does not exceed the positive supply voltage. Proper input coupling is illustrated below.

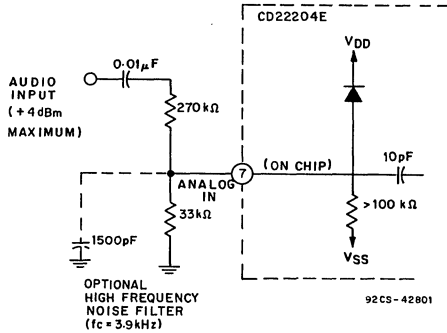


Fig. 2 - Analog In.

The CD22204E is designed to accept sinusoidal input waveforms, but will operate satisfactorily with any input that has the correct fundamental frequency with harmonics that are at least 20 dB below the fundamental.

## CRYSTAL OSCILLATOR

The CD22204 contains an on-board inverter with sufficient gain to provide oscillation when connected to a low-cost television "color-burst" (3.579545-MHz) crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1-Megohm resistor is also connected between these pins in this mode. ATB is a clock-frequency output. Other CD22204 devices may use the same frequency reference by tying their ATB pins to the ATB output of a crystal-connected device. XIN and XEN of the auxiliary devices must then be tied high and low, respectively. Up to ten devices may be run from a single crystal-connected CD22204 as shown below.

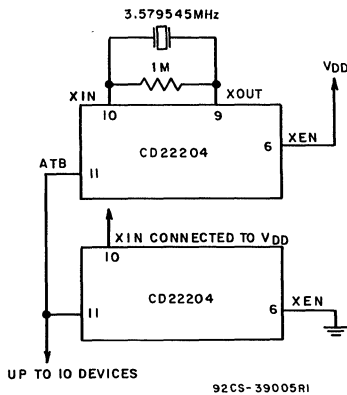


Fig. 3 - Crystal oscillator.

## OUTPUTS D1, D2, D4, D8 and EN

Outputs D1, D2, D4, D8 are CMOS push-pull when enabled (EN high) and open circuited (high impedance) when disabled by pulling EN low. These digital outputs provide the hexadecimal code corresponding to the detected digit. The digital outputs become valid after a tone pair has been detected and they are then cleared when a valid pause is timed. The table below describes the hexadecimal codes.

| OUTPUT CODE |    |    |    |    |
|-------------|----|----|----|----|
| Digit       | D8 | D4 | D2 | D1 |
| 1           | 0  | 0  | 0  | 1  |
| 2           | 0  | 0  | 1  | 0  |
| 3           | 0  | 0  | 1  | 1  |
| 4           | 0  | 1  | 0  | 0  |
| 5           | 0  | 1  | 0  | 1  |
| 6           | 0  | 1  | 1  | 0  |
| 7           | 0  | 1  | 1  | 1  |
| 8           | 1  | 0  | 0  | 0  |
| 9           | 1  | 0  | 0  | 1  |
| 0           | 1  | 0  | 1  | 0  |
| *           | 1  | 0  | 1  | 1  |
| #           | 1  | 1  | 0  | 0  |
| A           | 1  | 1  | 0  | 1  |
| B           | 1  | 1  | 1  | 0  |
| C           | 1  | 1  | 1  | 1  |
| D           | 0  | 0  | 0  | 0  |

## DV

DV signals a detection by going high after a valid tone pair is sensed and decoded at the output pins D1, D2, D4, D8. DV remains high until a valid pause occurs.

## N/C PIN

This pin has no internal connection and should be left floating.

## DTMF DIALING MATRIX

|                 | Col 0<br>1209 Hz | Col 1<br>1336 Hz | Col 2<br>1477 Hz | Col 3<br>1633 Hz |
|-----------------|------------------|------------------|------------------|------------------|
| Row 0<br>697 Hz | 1                | 2                | 3                | A                |
| Row 1<br>770 Hz | 4                | 5                | 6                | B                |
| Row 2<br>852 Hz | 7                | 8                | 9                | C                |
| Row 3<br>941 Hz | *                | 0                | #                | D                |

Note:  
Column 3 is for special applications and is not normally used in telephone dialing.

# CD22204

## DIGITAL INPUTS AND OUTPUTS

All digital inputs and outputs of the DTMF receiver are represented by the schematic below. Only the "analog in" pin is different, and is described above. Care must be exercised not to exceed the voltage or current ratings on these pins as listed in the "maximum ratings" section.

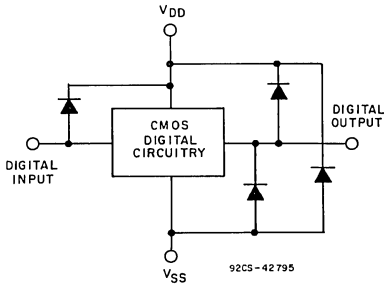


Fig. 4 - Digital inputs and outputs.

## TIMING WAVEFORMS

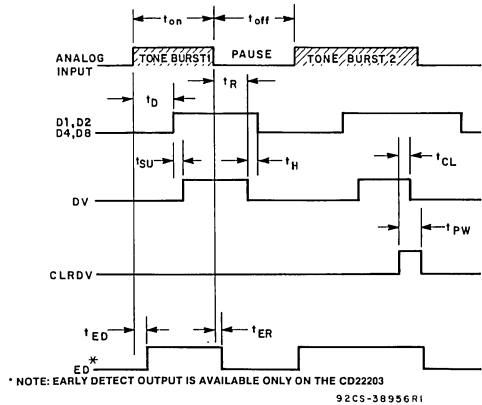


Fig. 6 - Timing waveforms.

## INPUT FILTER

The CD22204 will tolerate total input noise of a maximum of 12 dB below the lowest-amplitude tone. For most telephone applications, the combination of the high-frequency attenuation of the telephone line and internal band-limiting make special circuitry at the input to these receivers unnecessary. However, noise near the 56 kHz internal sampling frequency will be aliased (folded back) into the audio spectrum, so if excessive noise is present above 28 kHz, the simple RC filter shown below may be used to band-limit the incoming signal. The cut-off frequency is 3.9 kHz.

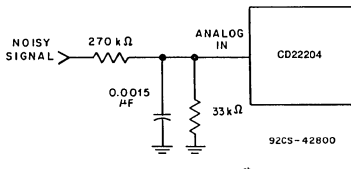


Fig. 5 - Filter for use in extreme high frequency input noise environment.

Noise will also be reduced by placing a grounded trace around XIN and XOUT pins on the circuit board layout when using a crystal. It is important to note that XOUT is not intended to drive an additional device. XIN may be driven externally; in this case, leave XOUT floating.

| PARAMETER          | SYMBOL    | MIN. | TYP. | MAX. | UNITS |
|--------------------|-----------|------|------|------|-------|
| Tone Time:         |           |      |      |      |       |
| for detection      | $t_{ON}$  | 40   | —    | —    | ms    |
| for rejection      | $t_{ON}$  | —    | —    | 20   | ms    |
| Pause Time:        |           |      |      |      |       |
| for detection      | $t_{OFF}$ | 40   | —    | —    | ms    |
| for rejection      | $t_{OFF}$ | —    | —    | 20   | ms    |
| Detect Time        | $t_D$     | 25   | —    | 46   | ms    |
| Release Time       | $t_R$     | 35   | —    | 50   | ms    |
| Data Setup Time    | $t_{SU}$  | 7    | —    | —    | μs    |
| Data Hold Time     | $t_H$     | 4.2  | —    | 5.0  | ms    |
| DV Clear Time      | $t_{CL}$  | —    | 160  | 250  | ns    |
| CLR DV pulse width | $t_{PW}$  | 200  | —    | —    | ns    |
| ED Detect Time     | $t_{ED}$  | 7    | —    | 22   | ms    |
| ED Release Time    | $t_{ER}$  | 2    | —    | 18   | ms    |
| Output Enable      |           |      |      |      |       |
| Time $C_L=50pF$    | —         | —    | 200  | 300  | ns    |
| $R_L=1K\Omega$     |           |      |      |      |       |
| Output Disable     |           |      |      |      |       |
| Time $C_L=35pF$    | —         | —    | 150  | 200  | ns    |
| $R_L=500\Omega$    |           |      |      |      |       |
| Output Rise        |           |      |      |      |       |
| Time $C_L=50pF$    | —         | —    | 200  | 300  | ns    |
| Output Fall Time   |           |      |      |      |       |
| $C_L=50pF$         | —         | —    | 160  | 250  | ns    |



August 1991

Telecommunications ICs

**Features**

- Automatic Line Buildout
- Supply Voltage ..... 5.1V
- Buffered Output

**Applications**

- Bipolar Carrier System ..... T1 1.544Mbits/s
- Ternary Carrier System ..... T148 2.37Mbits/s

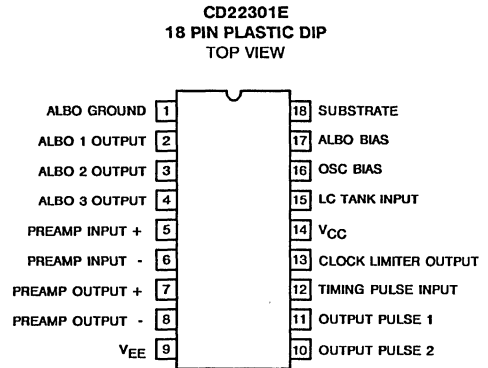
**Description**

The CD22301 monolithic PCM repeater circuit is designed for T1 carrier systems operating with a bipolar pulse train of 1.544Mbits/s. It can also be used in the T148 carrier system operating with a ternary pulse train of 2.37Mbits/s. The circuit operates from a 5.1V  $\pm 5\%$  externally regulated supply.

The CD22301 provides active circuitry to perform all functions of signal equalization and amplification, automatic line buildout (ALBO), threshold detection, clock extraction, pulse timing and buffered output formation.

The CD22301 is supplied in an 18 lead dual-in-line plastic package (E suffix).

**Pinout**



**Typical 1.544MHz T1 Repeater System**

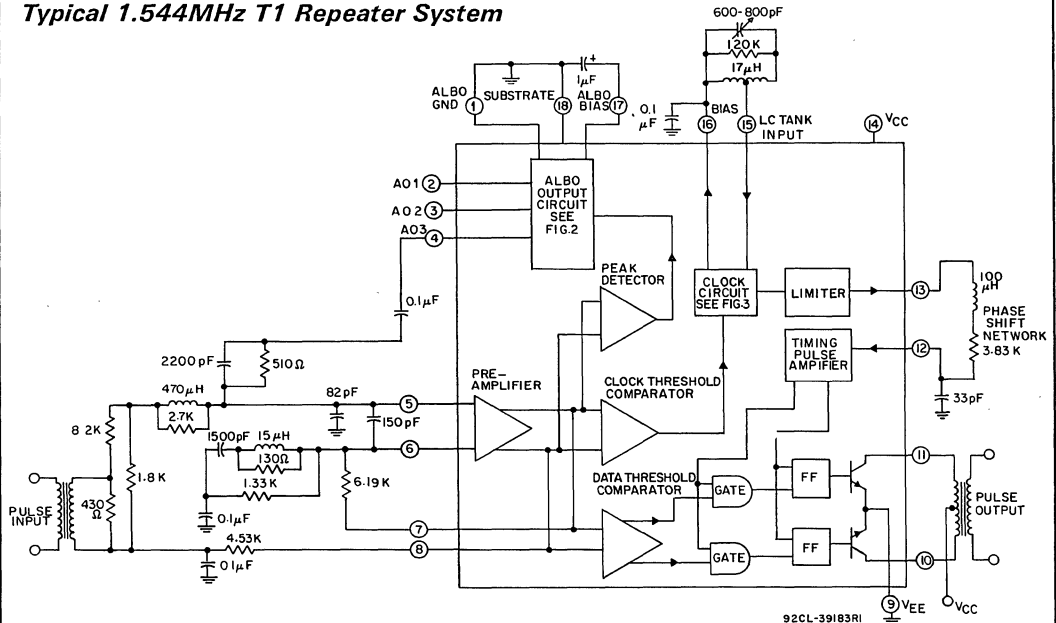


FIGURE 1.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.  
Copyright © Harris Corporation 1991

# CD22301

## MAXIMUM RATINGS, Absolute Maximum Values:

At ambient temperature ( $T_A$ ) = 25°C

|   |                                       |
|---|---------------------------------------|
| DC SUPPLY .....   | 10 V                                  |
| DC CURRENT (Into Pin 9 or 10) .....   | 25 mA                                 |
| PEAK CURRENT (Into Pin 9 or 10) .....   | 100 mA                                |
| INPUT SURGE VOLTAGE (Between Pins 5 and 6, $t = 10$ ms) .....                       | 50 V                                  |
| OUTPUT SURGE VOLTAGE (Between Pins 10 and 11, $t = 1$ ms) .....                     | 50 V                                  |
| POWER DISSIPATION PER PACKAGE ( $P_D$ )   |                                       |
| For $T_A = -40$ to $+60^\circ\text{C}$ .....  | 500 mW                                |
| For $T_A = +60^\circ\text{C}$ to $+85^\circ\text{C}$ .....                          | Derate linearly at 12 mW/°C to 200 mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR  |                                       |
| For $T_A = \text{Full Package-Temperature Range}$ .....                             | 100 mW                                |
| OPERATING TEMPERATURE RANGE ( $T_A$ ) .....   | -40 to $+85^\circ\text{C}$            |
| STORAGE TEMPERATURE ( $T_{stg}$ ) .....   | -65 to $+150^\circ\text{C}$           |
| LEAD TEMPERATURE (DURING SOLDERING)   |                                       |
| At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79$ mm) from case for 10 s max ..... | $+265^\circ\text{C}$                  |

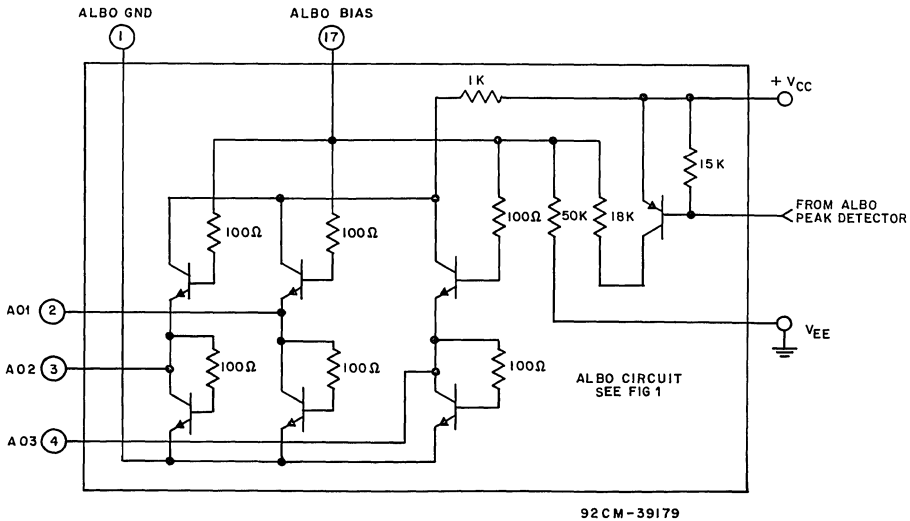


Fig. 2 - ALBO output circuit.

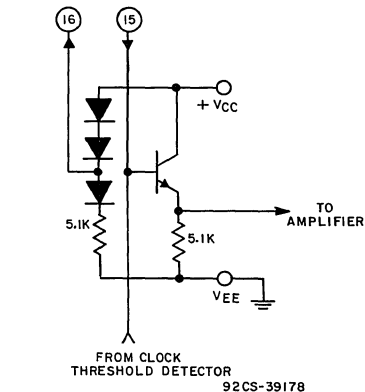


Fig. 3 - Clock interface circuit.

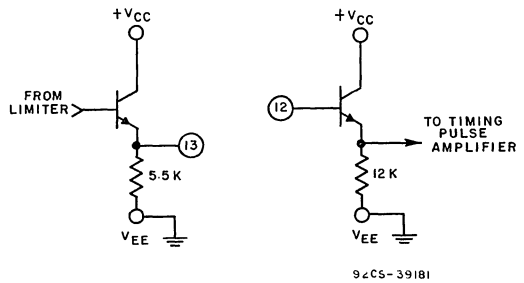


Fig. 4 - Phase-shift interface circuits.

## Specifications CD22301

### STATIC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5.1\text{ V} \pm 5\%$  (See Fig. 5)

| CHARACTERISTIC         | LIMITS |      |      | UNITS         |
|------------------------|--------|------|------|---------------|
|                        | Min.   | Typ. | Max. |               |
| <b>DC VOLTAGES</b>     |        |      |      |               |
| Pins 2, 3, 4 and 17    | —      | 0    | 0.1  | V             |
| Pins 5, 6, 7 and 8     | 2.4    | 2.9  | 3.4  | V             |
| Pins 10 and 11         | —      | 5.1  | —    | V             |
| Pins 12, 13, 15 and 16 | 3.1    | 3.6  | 4.1  | V             |
| <b>DC CURRENTS</b>     |        |      |      |               |
| Pin 14                 | —      | 22   | 30   | mA            |
| Pins 10 and 11         | —      | 0    | 100  | $\mu\text{A}$ |

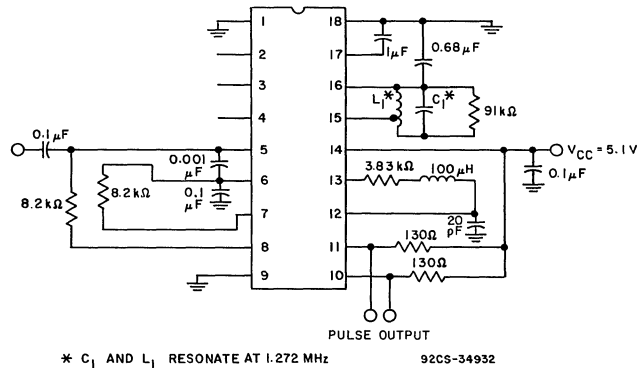


Fig. 5 - DC and output pulse test circuit.

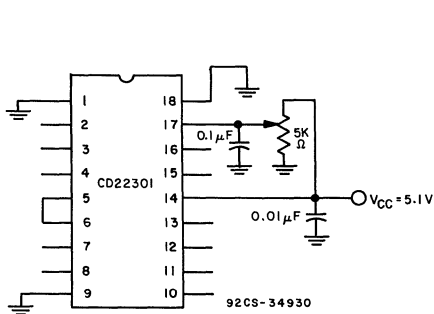


Fig. 6 - Test circuit for impedance measurement.

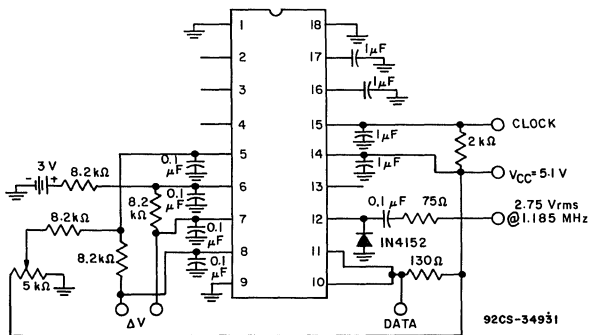


Fig. 7 - Test circuit for threshold voltage measurement.

## Specifications CD22301

### DYNAMIC ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5.1\text{ V} \pm 5\%$

| CHARACTERISTIC                     | FIG.             | NOTE | LIMITS |       |      | UNITS     |           |
|------------------------------------|------------------|------|--------|-------|------|-----------|-----------|
|                                    |                  |      | MIN.   | TYP.  | MAX. |           |           |
| Preamplifier Input Impedance       | $Z_{in}$         | 8    | 20     | —     | —    | $k\Omega$ |           |
| Preamplifier Output Impedance      | $Z_{out}$        | 8    | —      | —     | 2    | $k\Omega$ |           |
| Preamplifier Gain @ 2.37 MHz       | $A_o$            | 8    | 47     | 50    | —    | dB        |           |
| Preamplifier Output Offset Voltage | $\Delta V_{out}$ | 8    | 1      | -50   | 0    | 50        | mV        |
| Clock Limiter Input Impedance      | $Z_{in}(CL)$     | 6    | 2      | 10    | —    | —         | $k\Omega$ |
| ALBO Off Impedance                 | $Z_{ALBO(off)}$  | 6    | 3      | 20    | —    | —         | $k\Omega$ |
| ALBO On Impedance                  | $Z_{ALBO(on)}$   | 6    | 4      | —     | —    | 10        | $\Omega$  |
| DATA Threshold Voltage             | $V_{TH(D)}$      | 7    | 5, 8   | 0.62  | 0.7  | 0.78      | V         |
| CLOCK Threshold Voltage            | $V_{TH(CL)}$     | 7    | 6, 8   | 0.92  | 1.1  | 1.28      | V         |
| ALBO Threshold                     | $V_{TH(AL)}$     | 7    | 7, 8   | 1.4   | 1.5  | 1.6       | V         |
| $V_{TH(D)}$ as % of $V_{TH(AL)}$   |                  |      |        | 44    | 47   | 49        | %         |
| $V_{TH(CL)}$ as % of $V_{TH(AL)}$  |                  |      |        | 66    | 73   | 80        | %         |
| Buffer Gate Voltage (low)          | $V_{OL}$         | 5    | 9      | 0.65  | 0.8  | 0.95      | V         |
| Differential Buffer Gate Voltage   | $\Delta V_{OL}$  | 5    | 9      | -0.15 | 0    | 0.15      | V         |
| Output Pulse Rise Time             | $t_r$            | 5, 9 | 9, 10  | —     | —    | 40        | ns        |
| Output Pulse Fall Time             | $t_f$            | 5, 9 | 9, 10  | —     | —    | 40        | ns        |
| Output Pulse Width                 | $t_w$            | 5, 9 | 9, 10  | 290   | 324  | 340       | ns        |
| Pulse Width Differential           | $\Delta t_w$     | 5, 9 | 9, 10  | -10   | 0    | 10        | ns        |
| Clock Drive Current                | $I_{CL}$         |      |        | —     | 2    | —         | mA        |

#### Notes:

- No signal input. Measure voltage between pins 7 and 8.
- Measure clock limiter input impedance at pin 15.
- Adjust potentiometer for 0 volts. Measure ALBO off impedances from pins 2, 3 and 4 to pin 1.
- Increase potentiometer until voltage at pin 17 = 2 Vdc. Measure ALBO on impedances from pins 2, 3 and 4 to pin 1.
- Adjust potentiometer for  $\Delta V = 0$  volts. Then slowly increase  $\Delta V$  in the positive direction until pulses are observed at the DATA terminal.
- Continue increasing  $\Delta V$  until the DC level at the clock terminal drops to 4 volts.
- Continue increasing  $\Delta V$  until the ALBO terminal rises to 1 volt.
- Turn potentiometer in the opposite direction and measure negative threshold voltages by repeating tests outlined in notes 5, 6 and 7.
- Set  $e_{in} = 2.75$  mV(rms) at  $f \approx 1.185$  MHz. Adjust frequency until maximum amplitude is obtained at pin 15. Observe output pulses at pins 10 and 11.
- Adjust input signal amplitude until pulses just appear in outputs. Increase input amplitude by three dB.

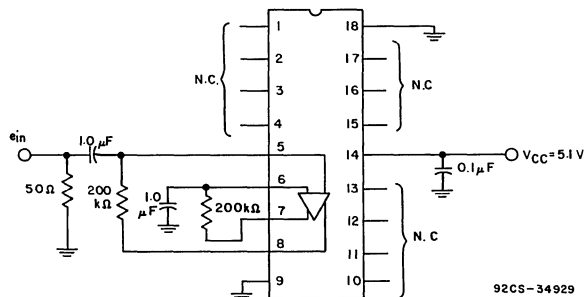


Fig. 8 - Preamplifier gain and impedance measurement circuit.

December 1990

### Features

- Meets or Exceeds All AT&T D3/D4 Specifications and CCITT Recommendations
- Complete CODEC and Filtering Systems: No External Components for Sample-and-Hold and Auto-Zero Functions. Receive Output Filter with SIN X/X Correction and Additional 8kHz Suppression
- Variable Data Clocks - From 64kHz ..... 2.1MHz
- Receiver Includes Power-Up Click Filter
- TTL or CMOS-Compatible Logic
- ESD Protection on All Inputs and Outputs

### Applications

- PABX
- Central Office Switching Systems
- Accurate A/D and D/A Conversions
- Digital Telephones
- Cellular Telephone Switching Systems
- Voice Scramblers - Descramblers
- T1 Conference Bridges
- Voice Storage and Retrieval Systems
- Sound Based Security Systems
- Computerized Voice Analysis
- Mobile Radio Telephone Systems
- Microwave Telephone Networks
- Fiber-Optic Telephone Networks

### Description

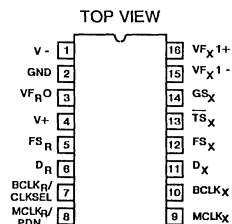
The CD22354A and CD22357A are monolithic silicongate, double-poly CMOS integrated circuits containing the band-limiting filters and the companding A/D and D/A conversion circuits that conform to the AT&T D3/D4 specifications and CCITT recommendations. The CD22354A provides the AT&T  $\mu$ -law and the CD22357A provides the CCITT A-law companding characteristic.

The primary applications for the CD22354A and CD22357A are in telephone systems. These circuits perform the analog and digital conversions between the subscriber loop and the PCM highway in a digital switching system. The functional block diagram is shown below.

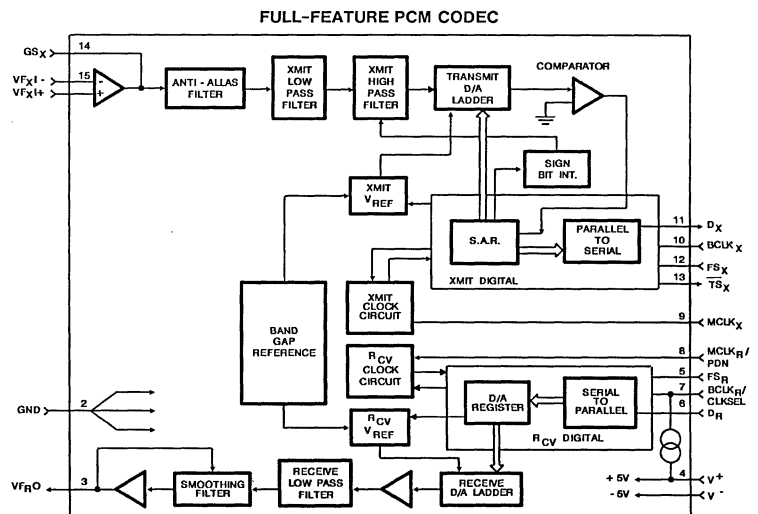
With the flexible features, including synchronous and asynchronous operations and variable data rates, the CD22354A and CD22357A are ideally suited for PABX, central office switching system, digital telephones as well as other applications that require accurate A/D and D/A conversions and minimal conversion time.

The CD22354A and CD22357A are supplied in 16-lead dual-in-line plastic packages (E suffix).

### Pinouts



### Functional Block Diagram



## Specifications CD22354A/CD22357A

### Absolute Maximum Ratings

|  |                          |  |                 |
|--|--------------------------|--|-----------------|
| DC Supply-Voltage, (V <sup>+</sup> )   | -0.5 to +7V              | Operating-Temperature Range (T <sub>A</sub> )                | -40°C to +80°C  |
| DC Supply-Voltage, (V <sup>-</sup> )   | +0.5 to -7V              | Storage Temperature (T <sub>STG</sub> )                      | -65°C to +150°C |
| DC Input Diode Current,  |                          | Lead Temperature (During Soldering):                         |                 |
| I <sub>IK</sub> (V <sub>I</sub> < V <sup>-</sup> -0.5V or V <sub>I</sub> > V <sup>+</sup> +0.5V) | ±20mA                    | At Distance 1/16± 1/32 in. (1.59 ± 0.79mm)                   |                 |
| DC Output Diode Current,   |                          | from Case for 10s Max.                                       | +265°C          |
| I <sub>OK</sub> (V <sub>I</sub> < V <sup>-</sup> -0.5V or V <sub>O</sub> > V <sup>+</sup> +0.5V) | ±20mA                    | Unit Insert into a PC Board (Min. Thickness 1/16 in. 1.59mm) |                 |
| DC Drain Current, Per Output   |                          | with Solder Contacting Lead Tips Only                        | +300°C          |
| I <sub>O</sub> (V <sup>-</sup> -0.5V < V <sub>O</sub> < V <sup>+</sup> +0.5V)                    | ±25mA                    |  |                 |
| DC Supply/Ground Current   | ±50mA                    |  |                 |
| Power Dissipation Per Package (P <sub>D</sub> ):   |                          |  |                 |
| For T <sub>A</sub> = -40°C to +60°C  | 500 mW                   |  |                 |
| For T <sub>A</sub> = +60°C to +85°C  | Derate Linearly @ 8mW/°C |  |                 |
|  | to 300mW                 |  |                 |

### Pin Function and Description

| PIN NO. | SYMBOL                    | DESCRIPTION   |
|---------|---------------------------|---|
| 1       | V-                        | Negative power supply, V <sup>-</sup> = -5V ± 5%  |
| 2       | GND                       | Analog and digital ground. All signals referenced to this pin.  |
| 3       | VF <sub>RO</sub>          | Analog output of RECEIVE FILTER   |
| 4       | V+                        | Positive power supply, V <sup>+</sup> = +5V ± 5%  |
| 5       | FS <sub>R</sub>           | Receive Frame Sync Pulse which enables BCLK <sub>R</sub> to shift PCM data into D <sub>R</sub> . FS <sub>R</sub> is an 8kHz PULSE TRAIN.  |
| 6       | D <sub>R</sub>            | Receive Data Input. PCM data is shifted into D <sub>R</sub> following the FS <sub>R</sub> leading edge.   |
| 7       | BCLK <sub>R</sub> /CLKSEL | The Bit Clock, which shifts data into D <sub>R</sub> after the Frame sync leading edge, may vary from 64kHz to 2.048MHz. Alternatively, the leading edge may be a logic input which selects either 1.536MHz or 1.544MHz or 2.048MHz for Master Clock in synchronous mode and BCLK <sub>X</sub> is used for both transmit and receive directions.              |
| 8       | MCLK <sub>R</sub> /PDN    | Receive Master Clock. Must be 1.536MHz or 1.544MHz or 2.048MHz. May be asynchronous with MCLK <sub>X</sub> but should be synchronous with MCLK <sub>X</sub> for best performance. When this pin is continuously connected low, MCLK <sub>X</sub> is selected for all internal timing. When this pin is continuously connected high, the device is power down. |
| 9       | MCLK <sub>X</sub>         | Transmit Master Clock. Must be 1.536MHz or 1.544MHz or 2.048MHz. May be asynchronous with MCLK <sub>R</sub> .   |
| 10      | BCLK <sub>X</sub>         | The Bit Clock which shifts out the PCM Data on D <sub>X</sub> . May vary from 64kHz to 2.048MHz but must be synchronous with MCLK <sub>X</sub> .  |
| 11      | D <sub>X</sub>            | The TRI-STATE PCM Data Output which is enabled by FS <sub>X</sub> .   |
| 12      | FS <sub>X</sub>           | Transmit Frame Sync Pulse input which enables BCLK <sub>X</sub> to shift out the data on D <sub>X</sub> . FS <sub>X</sub> is an 8kHz PULSE TRAIN.   |
| 13      | $\overline{TS}_X$         | Open drain output which pulses low during the encoder time slot.  |
| 14      | GS <sub>X</sub>           | Transmit gain adjust  |
| 15      | VF <sub>X</sub> I-        | Inverting input of the transmit input amplifier   |
| 16      | VF <sub>X</sub> I+        | Non-inverting input of the transmit input amplifier   |



TELECOM

**Functional Description**

**Power-Up**

When power is first applied, the Power-On reset circuitry initializes the CODEC and places it in a Power-Down mode. When the CODEC returns to an active state from the Power-Down mode, the receive output is muted briefly to minimize turn-on "click".

To power up the device, there are two modes available.

1. A logical zero at pin 8 will power up the device, provided FS<sub>X</sub> or FS<sub>R</sub> pulses are present.
2. Alternatively, a clock (MCLK<sub>R</sub>) must be applied to pin 8 and FS<sub>X</sub> or FS<sub>R</sub> pulses must be present.

**Power-Down**

Two power-down modes are available.

1. A logical 1 at pin 8, after approximately 0.5ms, will power down the device.
2. Alternatively, hold both FS<sub>X</sub> and FS<sub>R</sub> continuously low, the device will power down approximately 0.5ms after the last FS<sub>X</sub> or FS<sub>R</sub> pulse.

**Synchronous Operation**

The same master clock and bit-clock should be used for the receive and transmit sections. MCLK<sub>X</sub> (pin 9) is used to provide the master clock for the transmit section. The receive section will use the same master clock if the MCLK<sub>R</sub>/PDN (pin 8) is grounded (synchronous operation), or at V+ (power-down mode). Pin 8 may be clocked only if a clock is provided at Pin 7 as in asynchronous operation.

The BCLK<sub>X</sub> (pin 10) is used to provide the bit clock to the transmit section. In synchronous operation, this bit clock is used for the receive section if MCLK<sub>R</sub>/PDN (pin 8) is grounded. BCLK<sub>R</sub>/CLKSEL (pin 7) is then used to select the proper internal frequency division for 1.544MHz, 1.536MHz or 2.048MHz operation. See Table below for 1.544MHz operation. The device automatically compensates for the 193rd clock pulse each frame.

Each FS<sub>X</sub> pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D<sub>X</sub> output on the leading edge of the BCLK<sub>X</sub>. After 8 bit-clock periods, the tristate D<sub>X</sub> output is returned to a high impedance state. With a FS<sub>R</sub> pulse PCM data is latched via the D<sub>R</sub> input on the negative edge of the BCLK<sub>X</sub>.

FS<sub>X</sub> and FS<sub>R</sub> must be synchronous with MCLK<sub>X</sub>. For 1.544MHz operation, the device automatically compensates for 193rd clock pulse each frame.

**CLOCKING OPTIONS**

| BCLK <sub>R</sub> /CLKSEL | MASTER CLOCK FREQUENCY SELECTED |                      |
|---------------------------|---------------------------------|----------------------|
|                           | CD22354A                        | CD22357A             |
| Clocked                   | 1.536MHz or 1.544MHz            | 2.048MHz             |
| 0                         | 2.048MHz                        | 1.536MHz or 1.544MHz |
| 1(or open circuit)        | 1.536MHz or 1.544MHz            | 2.048MHz             |

**Asynchronous Operation**

For asynchronous operation separate transmit and receive clocks may be applied.

For CD22357A, the MCLK<sub>X</sub> and MCLK<sub>R</sub> must be 2.048MHz and for CD22354A must be 1.536MHz or 1.544MHz. These clocks may not be synchronous. However, for best transmission performance it is recommended that MCLK<sub>X</sub> and MCLK<sub>R</sub> should be synchronous.

For 1.544MHz operation the device automatically compensates for the 193rd clock pulse each frame. FS<sub>X</sub> must be synchronous with MCLK<sub>X</sub> and BCLK<sub>X</sub>. FS<sub>R</sub> must be synchronous with BCLK<sub>R</sub>. BCLK<sub>R</sub> must be clocked if MCLK<sub>R</sub> is to be clocked.

**Short-Frame Sync Mode**

When the power is first applied, the power initialization circuitry places the CODEC in a short-frame sync mode. In this mode both frame sync pulses must be 1 bit-clock period long, with timing relationship shown in Figure 1.

With FS<sub>X</sub> high during falling edge of the BCLK<sub>X</sub>, the next rising edge of BCLK<sub>X</sub> enables the D<sub>X</sub> tristate output buffer, which will output the sign bit. The following rising seven edges clock out the remaining seven bits, and the next falling edge disables the D<sub>X</sub> output.

With FS<sub>R</sub> high during the falling edge of the BCLK<sub>R</sub> (BCLK<sub>X</sub> in synchronous mode), the next falling edge latches in the sign bit. The following seven edges latch in the seven remaining bits.

**Long-Frame Sync Mode**

In this mode of operation, both the frame sync pulses must be three or more bit-clock periods long with timing relationship shown in Figure 2.

Based on the transmit frame sync FS<sub>X</sub>, the CODEC will sense whether short- or long-frame sync pulses are being used.

For 64kHz operation the frame sync pulse must be kept low for a minimum of 160ns.

The D<sub>X</sub> tristate output buffer is enabled with the rising edge of FS<sub>X</sub> or the rising edge of the BCLK<sub>X</sub>, whichever comes later and the first bit clocked out is the sign bit. The following seven rising edges of the BCLK<sub>X</sub> clock out the remaining seven bits. The D<sub>X</sub> output is disabled by the next falling edge of the BCLK<sub>X</sub> following the 8th rising edge or by FS<sub>R</sub> going low whichever comes later.

A rising edge on the receive frame sync, FS<sub>R</sub>, will cause the PCM data at D<sub>R</sub> to be latched in on the next falling edge of the BCLK<sub>R</sub>. The remaining seven bits are latched on the successive seven falling edges of the bit-clock (BCLK<sub>X</sub> in synchronous mode).

**Transmit Section**

The transmit section consists of a gain-adjustable input op-amp, an anti-aliasing filter, a low-pass filter, a high-pass filter and a compressing A/D converter. The input op-amp drives a RC active anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides 30-dB attenuation (minimum) at the sampling frequency. From this filter the signal enters a 5th order low-pass filter clocked at 128kHz, followed by a 3rd order high-pass filter clock at 32kHz. The output of the high-pass filter directly drives the encoder capacitor ladder at an 8kHz sampling rate. A precision voltage reference is trimmed in manufacturing to provide an input overload of nominally 2.5-V peak. Transmit frame sync pulse FS<sub>X</sub> controls the process. The 8-bit PCM data is clocked out at D<sub>X</sub> by the BCLK<sub>X</sub>.

BCLK<sub>X</sub> can be varied from 64kHz to 2.1MHz.

# CD22354A/CD22357A

## Receive Section

The receive section consists of an expanding D/A converter and a low-pass filter which fulfills both the AT&T D3/D4 specifications and CCITT recommendations. PCM data enters the receive section at  $D_R$  upon the occurrence of  $FS_R$ , Receive Frame sync pulse.  $BCLK_R$ , Receive Data Clock, which can range from 64kHz to 2.1MHz, clocks the 8-bit PCM data into the receive data register. A D/A conversion is performed on the 8-bit PCM data and the

corresponding analog signal is held on the D/A capacitor ladder. This signal is transferred to a switched capacitor low-pass filter clock at 128kHz to smooth the sample-and hold signal as well as to compensate for the SIN X/X distortion.

The filter is then followed by a second order Sallen and Key active filter capable of driving a 600- $\Omega$  load to a level 7.2 dBm.

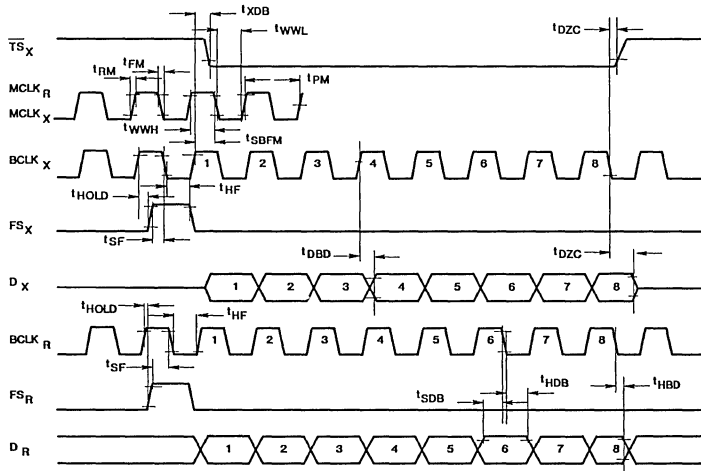


FIGURE 1. SHORT FRAME-SYNC TIMING

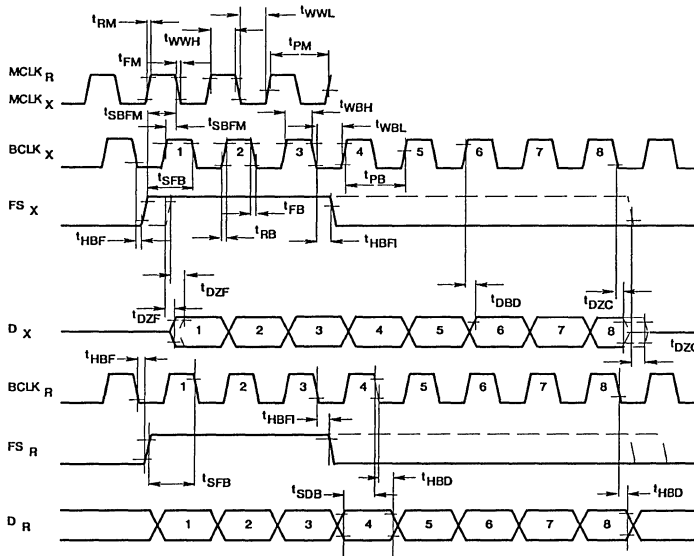


FIGURE 2. LONG FRAME-SYNC TIMING



## Specifications CD22354A/CD22357A

### Static Electrical Characteristics At $T_A = 25^\circ\text{C}$

| CHARACTERISTIC                | TEST CONDITIONS   | LIMITS   |      |       | UNITS |
|-------------------------------|-------------------|----------|------|-------|-------|
|                               |                   | MIN.     | TYP. | MAX.  |       |
| Positive Power Supply         | V+                | 4.75     | 5    | 5.25  | V     |
| Negative Power Supply         | V-                | -4.75    | -5   | -5.25 | V     |
| Power Dissipation (Operating) | P <sub>OPR</sub>  | V+ = 5V  |      | 90    | mW    |
| Power Dissipation (Standby)   | P <sub>STBY</sub> | V- = -5V |      | 15    | mW    |

### Static Electrical Characteristics At $T_A = 0^\circ\text{C}$ to $70^\circ\text{C}$ ; V+ = 5V, V- = -5V $\pm 5\%$

| CHARACTERISTIC                 | TEST CONDITIONS  | LIMITS                                     |      |      | UNITS         |
|--------------------------------|------------------|--|------|------|---------------|
|                                |                  | MIN.                                       | TYP. | MAX. |               |
| Analog Input Resistance        | R <sub>INA</sub> | 10   | -    | -    | M $\Omega$    |
| Input Capacitance              | C <sub>IN</sub>  | All Logic and Analog Inputs                |      | -    | pF            |
| Input Leakage Current, Digital | I <sub>I</sub>   | V <sub>I</sub> = 0V or V+                  |      | 10   | $\mu\text{A}$ |
| Low Level Input Voltage        | V <sub>IL</sub>  | I <sub>IL</sub> = $\pm 10\mu\text{A}$ max. |      | 0.8  | V             |
| High Level Input Voltage       | V <sub>IH</sub>  | I <sub>IH</sub> = $\pm 10\mu\text{A}$ max. |      | -    | V             |
| Low Level Output Voltage       | V <sub>OL</sub>  | I <sub>OL</sub> = 3.2mA                    |      | 0.4  | V             |
| High Level Output Voltage      | V <sub>OH</sub>  | I <sub>OH</sub> = 1.0mA                    |      | -    | V             |
| Open State Output Current      | I <sub>OZ</sub>  | GND < D <sub>X</sub> < V+                  |      | 10   | $\mu\text{A}$ |
| Input Leakage Current, Analog  | I <sub>I</sub>   | -2.5V $\leq$ V <sub>FX1</sub> $\leq$ 2.5V  |      | 200  | nA            |

### Transmit and Receive Filter Transfer Characteristics

V+ = 5V  $\pm 5\%$ , V- = -5V  $\pm 5\%$ , BCLK<sub>X</sub> = MCLK<sub>R</sub> = 1.544MHz, V<sub>IN</sub> = 0dBmO, T<sub>A</sub> = 0°C to 70°C

| CHARACTERISTIC  | TEST CONDITIONS                  | LIMITS |      |      | UNITS |
|---|----------------------------------|--------|------|------|-------|
|   |                                  | MIN.   | TYP. | MAX. |       |
| Transmit Gain<br>(Relative to Gain at 1020Hz)<br>Input Amplifier Set to Unit Gain | 16Hz                             | -      | -    | -40  | dB    |
|   | 50Hz                             | -      | -    | -30  | dB    |
|   | 60Hz                             | -      | -    | -26  | dB    |
|   | 200Hz                            | -1.8   | -    | -0.1 | dB    |
|   | 300 to 3000Hz                    | -0.15  | -    | 0.15 | dB    |
|   | 3300Hz                           | -0.35  | -    | 0.05 | dB    |
|   | 3400Hz                           | -0.7   | -    | 0    | dB    |
|   | 4000Hz                           | -      | -    | -14  | dB    |
| Receive Gain<br>(Relative to Gain at 1020Hz)<br>(Includes sin X/X Compensation)   | 4600Hz and up,<br>Measure 0-4kHz | -      | -    | -32  | dB    |
|   | 0Hz to 3000Hz                    | -0.15  | -    | 0.15 | dB    |
|   | 3300Hz                           | -0.35  | -    | 0.05 | dB    |
|   | 3400Hz                           | -0.7   | -    | 0    | dB    |
|   | 4000Hz                           | -      | -    | 14   | dB    |

## Specifications CD22354A/CD22357A

### A.C. Characteristics

Unless otherwise specified, the following conditions apply:

$$V^+ = 5V \text{ dc } \pm 5\%, V^- = -5V \text{ dc } \pm 5\%$$

$$GND_A, GND_D = 0V, F_{FX} = 1020\text{Hz at } 0\text{dBmO}$$

Transmit input amplifier operating in a unity gain configuration

Temperature ..... 0°C to 70°C

Receive output is measured single-ended. All output levels are SIN X/X corrected.

### Definition

#### AMPLITUDE RESPONSE

Absolute Levels Definition:

$$V_{REF} = -2.5V \text{ dc}$$

Nominal 0 dBmO level ..... 4dBm into 600Ω  
1.2276V (rms)

Maximum Overload Level:

Voltage reference ( $V_{REF}$ ) of -2.5V ..... 2.5V  $\mu$ -Law  
2.49V A-Law

### Encoding Format at D<sub>X</sub> Output

|  | CD22354A<br>$\mu$ -LAW |   |   |   |   |   |   |   | CD22357A<br>A-LAW<br>(INCLUDES EVEN BIT INVERSION) |   |   |   |   |   |   |   |
|--|------------------------|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|
|  | 1                      | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1  | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| $V_{IN}$ (at GS <sub>X</sub> ) = +Full-Scale | 1                      | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1  | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| $V_{IN}$ (at GS <sub>X</sub> ) = 0V          | 1                      | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1  | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
|  | 0                      | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0  | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| $V_{IN}$ (at GS <sub>X</sub> ) = -Full-Scale | 0                      | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

### Distortion Characteristics

| CHARACTERISTIC   | TEST CONDITIONS                     | LIMITS  |      |      | UNITS |         |
|--|-------------------------------------|---|------|------|-------|---------|
|  |                                     | MIN.  | TYP. | MAX. |       |         |
| Signal to Total Distortion<br>Xmit or R <sub>CV</sub>  | STD <sub>X</sub> , STD <sub>R</sub> | Level +3dBmO  | 33   | -    | -     | dBC     |
|  |                                     | 0 to -30dBmO  | 36   | -    | -     | dBC     |
|  |                                     | -40dBmO   | 30   | -    | -     | dBC     |
|  |                                     | -55dBmO, XMT  | 14   | -    | -     | dBC     |
|  |                                     | -55dBmO, R <sub>CV</sub>  | 15   | -    | -     | dBC     |
| Single Frequency Distortion<br>Xmit or R <sub>CV</sub> | SFD <sub>X</sub> , SFD <sub>R</sub> | -   | -    | -46  | dBC   |         |
| Intermodulation (End-to-End<br>Measurement) 2-Tone     | IMD                                 | $V_{FX} = -4\text{dBmO to } -21\text{dBmO}$<br>$f_1, f_2 \text{ from } 300 \text{ to } 3400\text{Hz}$ | -    | -    | -41   | dB      |
| Transmit Absolute Delay                                | $t_{DAX}$                           | $f = 1600\text{Hz}$   | -    | 280  | 315   | $\mu$ s |
| Transmit Envelope Delay<br>Relative to D <sub>AX</sub> | $t_{DEX}$                           | $f = 500\text{--}600\text{Hz}$  | -    | 170  | 220   | $\mu$ s |
|  |                                     | $f = 600\text{--}1000\text{Hz}$   | -    | 70   | 145   | $\mu$ s |
|  |                                     | $f = 1000\text{--}2600\text{Hz}$  | -    | 40   | 75    | $\mu$ s |
|  |                                     | $f = 2600\text{--}2800\text{Hz}$  | -    | 90   | 105   | $\mu$ s |
| Receive Absolute Delay                                 | $t_{DAR}$                           | $f = 1600\text{Hz}$   | -    | 180  | 200   | $\mu$ s |
| Receive Envelope Delay<br>Relative to D <sub>AR</sub>  | $t_{DER}$                           | $f = 500\text{--}600\text{Hz}$  | -40  | -25  | -     | $\mu$ s |
|  |                                     | $f = 600\text{--}1000\text{Hz}$   | -40  | -25  | -     | $\mu$ s |
|  |                                     | $f = 1000\text{--}2600\text{Hz}$  | -    | 60   | 90    | $\mu$ s |
|  |                                     | $f = 2600\text{--}2800\text{Hz}$  | -    | 110  | 125   | $\mu$ s |

## Specifications CD22354A/CD22357A

### Gain Tracking

| CHARACTERISTIC                           |     | TEST CONDITIONS   | LIMITS |      |      | UNITS |
|--|-----|---|--------|------|------|-------|
|  |     |   | MIN.   | TYP. | MAX. |       |
| Transmit Gain Tracking Error             | GTX | +3 to -40dBmO   | -      | -    | ±0.2 | dB    |
|  |     | -40 to -50dBmO  | -      | -    | ±0.4 | dB    |
|  |     | -50 to -55dBmO  | -      | -    | ±1.2 | dB    |
| Receive Gain Tracking Error              | GTR | +3 to -40dBmO   | -      | -    | ±0.2 | dB    |
|  |     | -40 to -50dBmO  | -      | -    | ±0.4 | dB    |
|  |     | -50 to -55dBmO  | -      | -    | ±1.2 | dB    |
| Transmit Input Amplifier Gain, Open Loop | AOL | $R_L \geq 1M\Omega$ at GSX  | 68     | -    | -    | dB    |
| Transmit Input Amplifier Gain, Unity     | ACL | Unity Gain Configuration<br>Inverting or Non-Inverting<br>$R_L \geq 10K, C_L \leq 50pF$ | -0.01  | -    | 0.01 | dB    |
| Transmit Gain, Absolute                  | GXA | $R_L \geq 10K, C_L \leq 50pF$   | -0.15  | -    | 0.15 | dB    |
| Receive Gain, Absolute                   | GRA | $R_L \geq 600\Omega, C_L \leq 500pF$  | -0.15  | -    | 0.15 | dB    |

### Noise Characteristics

| CHARACTERISTIC                     |                  | TEST CONDITIONS  | LIMITS |      |      | UNITS             |
|------------------------------------|------------------|--|--------|------|------|-------------------|
|                                    |                  |  | MIN.   | TYP. | MAX. |                   |
| Transmit Noise                     | N <sub>X</sub>   | $V_{FXI^-} = GND$  | -      | 12   | 15   | dBm <sub>cO</sub> |
|                                    |                  | $V_{FXI^+} = GND$  | -      | -74  | -67  | dBm <sub>Op</sub> |
| Receive Noise                      | N <sub>R</sub>   | PCM Code Equivalent<br>to Zero Volts   | -      | 7    | 11   | dBm <sub>cO</sub> |
|                                    |                  |  | -      | -83  | -79  | dBm <sub>Op</sub> |
| V+ Power Supply Rejection Transmit | PSRR             | $V_{FXI^+} = 0V$<br>$V^+ = 5V + (100mV RMS)$<br>$f = 0$ to 50kHz   | 40     | -    | -    | dBc               |
| V- Power Supply Rejection Transmit | PSRR             | $V_{FXI^-} = 0V$<br>$V^- = -5V + (100mV RMS)$<br>$f = 0$ to 50kHz  | 40     | -    | -    | dBc               |
| V+ Power Supply Rejection Receive  | PSRR             | PCM Code = All 1 Code<br>$V^+ = 5V + (100mV RMS)$<br>$f = 0$ to 4kHz<br><br>= 4 to 25kHz<br><br>= 25 to 50kHz  | 40     | -    | -    | dBc               |
|                                    |                  |  | 40     | -    | -    | dB                |
|                                    |                  |  | 36     | -    | -    | dB                |
| V- Power Supply Rejection Receive  | PSRR             | PCM Code = All 1 Code<br>$V^- = -5V + (100mV RMS)$<br>$f = 0$ to 4kHz<br><br>= 4 to 25kHz<br><br>= 25 to 50kHz | 40     | -    | -    | dBc               |
|                                    |                  |  | 40     | -    | -    | dB                |
|                                    |                  |  | 36     | -    | -    | dB                |
| Cross Talk Transmit to Receive     | CT <sub>XR</sub> | $V_{FXI^-} = 0dBmO @ 1020Hz$   | -      | -80  | -70  | dB                |
| Cross Talk Receive to Transmit     | CT <sub>RX</sub> | $D_R = 0dBmO @ 1020Hz,$<br>$V_{FXI^-} = 0V$  | -      | -76  | -70  | dB                |

## Specifications CD22354A/CD22357A

### Timing Specifications

| CHARACTERISTIC  | TEST CONDITIONS   | LIMITS      |                         |             | UNITS             |
|---|---|-------------|-------------------------|-------------|-------------------|
|   |   | MIN.        | TYP.                    | MAX.        |                   |
| Frequency of Master Clocks  | 1/TPM<br>Depends on the Device Used and the BCLK <sub>R</sub> /CLKSEL Pin MCLK <sub>X</sub> and MCLK <sub>R</sub> | -<br>-<br>- | 1.536<br>1.544<br>2.048 | -<br>-<br>- | MHz<br>MHz<br>MHz |
| Width of Master Clock High  | t <sub>WMH</sub><br>MCLK <sub>X</sub> and MCLK <sub>R</sub>   | 160         | -                       | -           | ns                |
| Width of Master Clock Low   | t <sub>WML</sub><br>MCLK <sub>X</sub> and MCLK <sub>R</sub>   | 160         | -                       | -           | ns                |
| Rise Time of Master Clock   | t <sub>RM</sub><br>MCLK <sub>X</sub> and MCLK <sub>R</sub>  | -           | -                       | 50          | ns                |
| Fall Time of Master Clock   | t <sub>FM</sub><br>MCLK <sub>X</sub> and MCLK <sub>R</sub>  | -           | -                       | 50          | ns                |
| Set-up Time from BCLK <sub>X</sub> High (and FS <sub>X</sub> in Long Frame Sync Mode) to MCLK <sub>X</sub> Falling Edge | t <sub>SBFM</sub><br>First Bit Clock after the Leading Edge of FS <sub>X</sub>                                    | 100         | -                       | -           | ns                |
| Period of Bit Clock   | t <sub>PB</sub>   | 485         | 488                     | 15,725      | ns                |
| Width of Bit Clock High   | t <sub>WBH</sub><br>V <sub>IH</sub> = 2.2V  | 160         | -                       | -           | ns                |
| Width of Bit Clock Low  | t <sub>WBL</sub><br>V <sub>IL</sub> = 0.6V  | 160         | -                       | -           | ns                |
| Rise Time of Bit Clock  | t <sub>RB</sub><br>t <sub>PB</sub> = 488ns  | -           | -                       | 50          | ns                |
| Fall Time of Bit Clock  | t <sub>FB</sub><br>t <sub>PB</sub> = 488ns  | -           | -                       | 50          | ns                |
| Holding Time from Bit Clock Low to Frame Sync   | t <sub>HBF</sub><br>Long Frame Only   | 0           | -                       | -           | ns                |
| Holding Time from Bit Clock High to Frame Sync  | t <sub>HOLD</sub><br>Short Frame Only   | 0           | -                       | -           | ns                |
| Set-up Time from Frame Sync to Bit Clock Low  | t <sub>SFB</sub><br>Long Frame Only   | 80          | -                       | -           | ns                |
| Delay Time from BCLK <sub>X</sub> High to Data Valid  | t <sub>DBD</sub><br>Load = 150pF plus 2 LSTTL Loads   | 0           | -                       | 180         | ns                |
| Delay Time to TS <sub>X</sub> Low   | t <sub>XD</sub><br>Load = 150pF plus 2 LSTTL Loads  | -           | -                       | 140         | ns                |
| Delay Time from BCLK <sub>X</sub> Low to Data Output Disabled   | t <sub>DZC</sub>  | 50          | -                       | 165         | ns                |
| Delay Time to Valid Data from FS <sub>X</sub> or BCLK <sub>X</sub> , Whichever Comes Later                              | t <sub>DZF</sub><br>C <sub>L</sub> = 0pF to 150pF   | 20          | -                       | 165         | ns                |
| Set-up Time from D <sub>R</sub> Valid to BCLK <sub>R/X</sub> Low  | t <sub>SDB</sub>  | 50          | -                       | -           | ns                |
| Hold Time from BCLK <sub>R/X</sub> Low to D <sub>R</sub> Invalid  | t <sub>HBD</sub>  | 50          | -                       | -           | ns                |
| Set-up Time from FS <sub>X/R</sub> to BCLK <sub>X/R</sub> Low   | t <sub>SF</sub><br>Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)                                | 50          | -                       | -           | ns                |
| Hold Time from BCLK <sub>X/R</sub> Low to FS <sub>X/R</sub> Low   | t <sub>HF</sub><br>Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)                                | 100         | -                       | -           | ns                |
| Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS <sub>X</sub> or FS <sub>R</sub> )                          | t <sub>HBF1</sub><br>Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)                                   | 100         | -                       | -           | ns                |
| Minimum Width of the Frame Sync Pulse (Low Level)   | t <sub>WFL</sub><br>64K Bits Operating Mode   | 160         | -                       | -           | ns                |

NOTE: 1. For short frame sync timing, FS<sub>X</sub> and FS<sub>R</sub> must go high while their respective bit clocks are high.

August 1991

### Features

- 96 Analog Switches
- Low  $R_{ON}$
- Guaranteed  $R_{ON}$  Matching
- Analog Signal Input Voltage Equal To The Supply Voltage
- Wide Operating Voltage: 4V To 16V
- Parallel Input Addressing
- High Latch Up Current: 50mA Minimum
- Very Low Crosstalk
- Pin And Functionally Compatible With The Following Types: SGS M3493, SGS M093, SSI 78A093A, and Mitel MT8812

### Applications

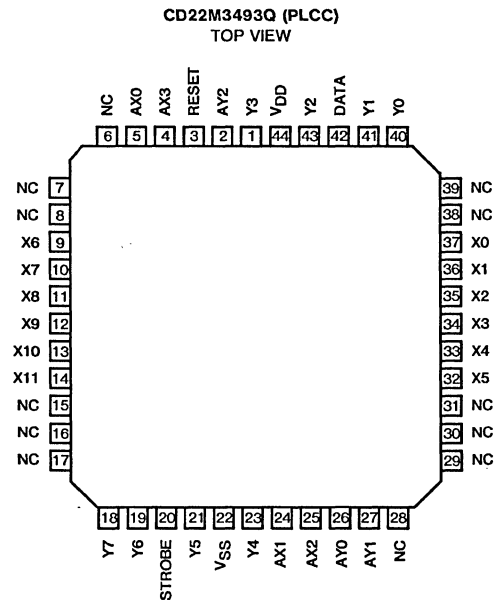
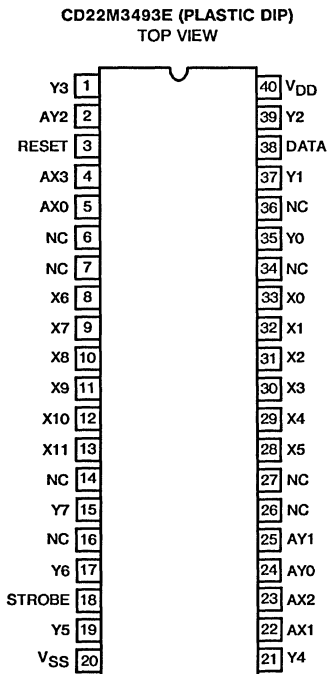
- PBX Systems
- Instrumentation
- Analog And Digital Multiplexers
- Video Switching Networks

### Description

The Harris CD22M3493 is an array of 96 analog switches capable of handling signals from DC to video. Because of the switch structure, input signals may swing through the total supply voltage range,  $V_{DD}$  to  $V_{SS}$ . Each of the 96 switches may be addressed via the ADDRESS input to the 7 to 96 line decoder. The state of the addressed switch is established by the signal to the DATA input. A low or zero input will open the switch, while a high logic level or a one will result in closure of the addressed switch when the STROBE input goes high from its normally low state. Any number or combination of connections may be active at one time. Each connection, however, must be made or broken individually in the manner previously described. All switches may be reset by taking the RESET input from a zero state to a one state and then returning it to its normal low state.

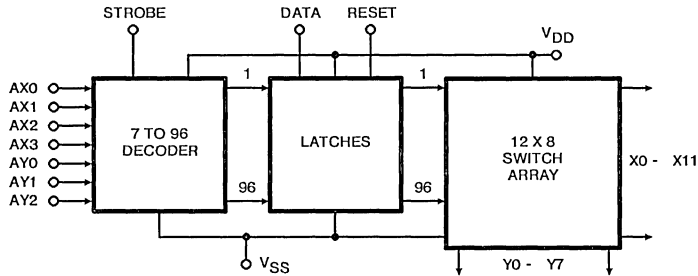
The CD22M3493 is offered both in Plastic DIP ('E' suffix) and in PLCC ('Q' suffix). The device is operational over the entire Industrial temperature range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ) in both packages.

### Pinouts



# CD22M3493

## Block Diagram



## Pin Descriptions

| SYMBOL                     | 40 PIN<br>PLASTIC DIP                | 44 PIN<br>PLCC                       | DESCRIPTION  |
|----------------------------|--------------------------------------|--------------------------------------|--|
| <b>POWER SUPPLIES</b>      |                                      |                                      |  |
| V <sub>DD</sub>            | 40                                   | 44                                   | Positive Supply  |
| V <sub>SS</sub>            | 20                                   | 22                                   | Negative Supply  |
| <b>ADDRESS</b>             |                                      |                                      |  |
| AX0 - AX3                  | 5, 22, 23,<br>& 4                    | 5, 24, 25,<br>& 4                    | X Address Lines. These pins select one of the 12 rows of switches. See the Truth Table for the valid addresses.  |
| AY0 - AY2                  | 24, 25,<br>& 2                       | 26, 27,<br>& 2                       | Y Address Lines. These pins select one of the 8 columns of switches. See the Truth Table for the valid addresses.  |
| <b>CONTROL</b>             |                                      |                                      |  |
| DATA                       | 38                                   | 42                                   | DATA Input determines the state of the addressed switch. A high or one will close the switch. A low or zero will open the switch.  |
| STROBE                     | 18                                   | 20                                   | STROBE Input enables the action defined by the DATA and ADDRESS Inputs. A low or zero results in no action. The ADDRESS Input must be stable before the STROBE Input goes to the active high level. The DATA Input must be stable on the falling edge of the STROBE. |
| RESET                      | 3                                    | 3                                    | MASTER RESET. A high or one on this line opens all switches.   |
| <b>INPUTS/OUTPUTS</b>      |                                      |                                      |  |
| X0 - X5<br>I/O<br>X6 - X11 | 33 - 28<br>8 - 13                    | 37 - 32<br>9 - 14                    | Analog or Digital Inputs/Outputs. These pins are the rows X0 - X11.  |
| Y0 - Y7<br>I/O             | 35, 37, 39,<br>1, 21, 19,<br>17 & 15 | 40, 41, 43,<br>1, 23, 21,<br>19 & 18 | Analog or Digital Inputs/Outputs. These pins are the columns Y0 - Y7.  |

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TELECOM

## Specifications CD22M3493

### Absolute Maximum Ratings

DC Supply Voltage ( $V_{DD}$ ):  
 (Voltages Referenced to  $V_{SS}$ ) ..... -0.5 to +17V  
 DC Input Diode Current,  $I_{IN}$  .....  $\pm 20$ mA  
 (For  $V_I < V_{SS} - 0.5$ V or  $V_I > V_{DD} + 0.5$ V)  
 DC Output Diode Current,  $I_{OK}$  .....  $\pm 20$ mA  
 (For  $V_O < V_{SS} - 0.5$ V or  $V_O > V_{DD} + 0.5$ V)  
 DC Transmission Gate Current .....  $\pm 25$ mA  
 Power Dissipation Per Package ( $P_o$ ):  
 For  $T_A = -40$  to  $+85^\circ\text{C}$  ..... 500mW  
 (Package Type E, 40 Pin Plastic DIP)  
 For  $T_A = -40$  to  $+85^\circ\text{C}$  ..... 600mW  
 (Package Type Q, 44 Pin PLCC)

Operating Temperature Range ( $T_A$ ):  
 Package Type E and Q .....  $-40$  to  $85^\circ\text{C}$   
 Storage Temperature Range ( $T_{STG}$ ) .....  $-65$  to  $150^\circ\text{C}$   
 Lead Temperature (During Soldering) For 10 sec max:  
 At a distance  $1/16 \pm 1/32$  in. ( $1.59 \pm 0.79$ mm) .....  $+265^\circ\text{C}$   
 From case for 10 sec max

\*Printed-circuit board mount 57mm x 57mm minimum area x 1.6mm thick GIO epoxy glass or equivalent.

### Recommended Operating Conditions

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC   | LIMITS               |                      | UNITS  |
|--|----------------------|----------------------|--------|
|  | MIN                  | MAX                  |        |
| Supply Voltage Range (For $T_A =$ Full Package Temperature Range) $V_{SS} = 0$ V<br>$V_{DD}$ | 4                    | 16                   | V      |
| DC Input or Output Voltage $V_I$ or $V_O$<br>Digital Input Voltage                           | $V_{SS}$<br>$V_{SS}$ | $V_{DD}$<br>$V_{DD}$ | V<br>V |

### Dynamic Electrical Characteristics ( $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ ) $V_{SS} = 0$ V, $V_{DD} = 14$ V, Unless Otherwise Specified

| CHARACTERISTIC                     | CONTROLS CONDITIONS                          | MIN | TYP | MAX        | UNITS         |
|------------------------------------|--|-----|-----|------------|---------------|
| Supply Current, $I_{DD}$           | $V_{DD} = 5$ V      Logic Inputs = $V_{DD}$  | -   | -   | 2          | mA            |
|                                    | $V_{DD} = 16$ V      Logic Inputs = $V_{DD}$ | -   | -   | 5          | mA            |
| High-Level Input Voltage, $V_{IH}$ |  | 2.4 | -   | -          | V             |
| Low-Level Input Voltage, $V_{IL}$  |  | -   | -   | 0.8        | V             |
| Input Leakage Current, $I_{IN}$    |  | -   | -   | $\pm 10^*$ | $\mu\text{A}$ |

| CHARACTERISTIC  | CROSSPOINTS CONDITIONS   | MIN | TYP | MAX        | UNITS         |
|---|--|-----|-----|------------|---------------|
| ON Resistance $R_{ON}$  | $T_A = 25^\circ\text{C}$ , $V_{DD} = 5$ V<br>$V_{IN} = V_{DD}/2$<br>$VX - VY = 0.25$ V                       | -   | 40  | 70         | $\Omega$      |
|   | $V_{DD} = 14$ V  | -   | 22  | 45         | $\Omega$      |
| ON Resistance $R_{ON}$  | $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ $V_{DD} = 5$ V<br>$V_{IN} = V_{DD}/2$<br>$VX - VY = 0.25$ V  | -   | -   | 80         | $\Omega$      |
|   | $V_{DD} = 14$ V  | -   | -   | 55         | $\Omega$      |
| Difference in ON Resistance between any two switches, $\Delta R_{ON}$ | $T_A = 25^\circ\text{C}$ ,<br>$V_{IN} = V_{DD}/2$<br>$VX - VY = 0.25$ V $V_{DD} = 14$ V                      | -   | 4   | 10         | $\Omega$      |
| Difference in ON Resistance between any two switches, $\Delta R_{ON}$ | $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$<br>$V_{IN} = V_{DD}/2$<br>$VX - VY = 0.25$ V $V_{DD} = 14$ V | -   | -   | 10         | $\Omega$      |
| OFF Leakage Current, $I_L$  | $ VX - VY  = 14$ V   | -   | -   | $\pm 10^*$ | $\mu\text{A}$ |

## CD22M3494

### Dynamic Electrical Characteristics (Continued)

( $T_A = +25^\circ\text{C}$ ),  $V_{SS} = 0\text{V}$ ,  $V_{EE} = 0\text{V}$ ,  $V_{DD} = 14\text{V}$ ,  $C_L = 50\text{pF}$ , Unless Otherwise Specified

| CHARACTERISTIC   | CROSSPOINTS CONDITIONS  | MIN | TYP  | MAX | UNITS |
|--|---|-----|------|-----|-------|
| Switch I/O Capacitance   | $V_{IN} = V_{DD}/2, f = 1\text{MHz}$  | -   | -    | 20  | pF    |
| Switch Feedthrough Capacitance   | $V_{IN} = V_{DD}/2, f = 1\text{MHz}$  | -   | 0.3  | -   | pF    |
| Propagation Delay Time (switch ON)<br>Signal Input to Output<br>$t_{PHL}$ or $t_{PLH}$ |   | -   | 30   | 100 | ns    |
| Frequency Response Channel ON<br>$f = 20\log(VX/VY) = -3\text{dB}$                     | $C_L = 3\text{pF}, R_L = 75\Omega, V_{IN} = 2VP-P$  | -   | 50   | -   | MHz   |
| Total Harmonic<br>THD  | $V_{IN} = 2VP-P, f = 1\text{kHz}$   | -   | 0.01 | -   | %     |
| Feedthrough Channel OFF<br>Feedthrough =<br>$20\log(VX/VY) = F_{DT}$                   | $V_{IN} = 2VP-P, f = 1\text{kHz}$   | -   | -95  | -   | dB    |
| Frequency for Signal Crosstalk, $f_{CT}$   | 40dB, $V_{IN} = 2VP-P, R_L = 75\Omega$  | -   | 10   | -   | MHz   |
| Attenuation of:  | 110dB, $V_{IN} = 2VP-P, R_L = 1k \parallel 10\text{pF}$   | -   | 5    | -   | kHz   |
| Control Crosstalk<br>DATA-Input, ADDRESS,<br>or STROBE to Output                       | Control Input = 3VP-P<br>Square Wave, $t_r = t_f = 10\text{ns}$<br>$R_{IN} = 1K, R_{OUT} = 10K \parallel 10\text{pF}$ | -   | 75   | -   | mVpk  |

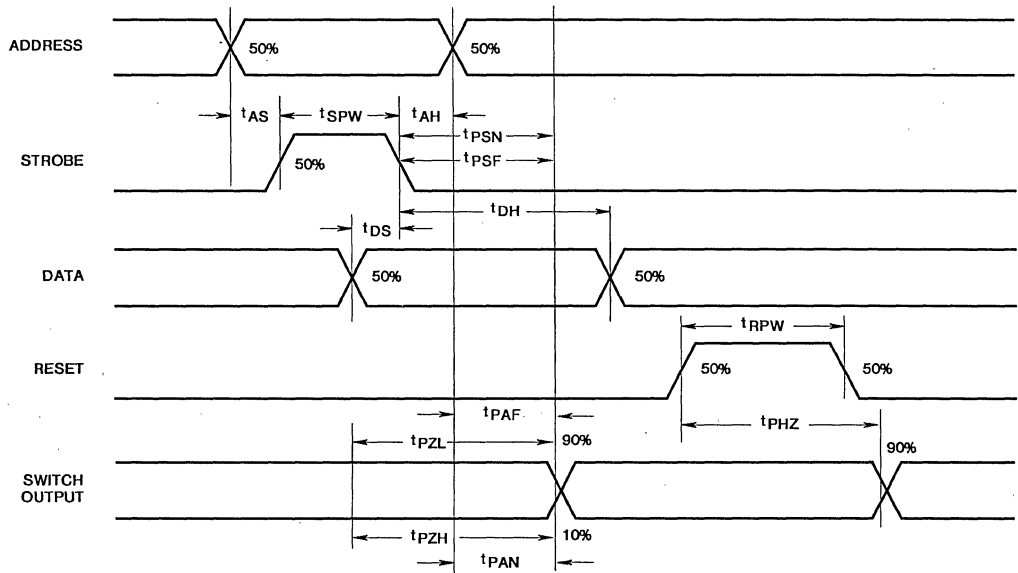
### Dynamic Electrical Characteristics

( $T_A = +25^\circ\text{C}$ ),  $V_{SS} = 0\text{V}$ ,  $V_{EE} = 0\text{V}$ ,  $V_{DD} = 14\text{V}$ ,  $R_L = 1K \parallel 50\text{pF}$ , Unless Otherwise Specified

| CHARACTERISTIC  | CONTROLS CONDITIONS                                | MIN                  | TYP               | MAX              | UNITS              |
|---|--|----------------------|-------------------|------------------|--------------------|
| Digital Input Capacitance   | $C_{IN} \quad V_{IN} = 5\text{V}, f = 1\text{MHz}$ | -                    | 5                 | -                | pF                 |
| Propagation Delay Time<br>STROBE to Output<br>(Switch turn-ON)<br>(Switch turn-OFF)                   | $t_{PSN}$<br>$t_{PSF}$                             | -<br>-               | 50<br>50          | 100<br>100       | ns<br>ns           |
| DATA-in to Output<br>(Turn-ON to high level)<br>(Turn-ON to low level)                                | $t_{PZH}$<br>$t_{PZL}$                             | -<br>-               | 60<br>70          | 100<br>100       | ns<br>ns           |
| ADDRESS to Output<br>(Turn-ON to high level)<br>(Turn-OFF to low level)                               | $t_{PAN}$<br>$t_{PAF}$                             | -<br>-               | 70<br>70          | -<br>-           | ns<br>ns           |
| Set-up Time<br>CS to STROBE<br>DATA-in to STROBE<br>ADDRESS to STROBE                                 | $t_{CS}$<br>$t_{DS}$<br>$t_{AS}$                   | 10<br>10<br>10       | -<br>-<br>-       | -<br>-<br>-      | ns<br>ns<br>ns     |
| Hold Time<br>STROBE to CS<br>ADDRESS to CS<br>STROBE to DATA-in<br>STROBE to ADDRESS<br>DATA-in to CS | $t_{CH}$<br>$t_{DH}$<br>$t_{AH}$                   | 10<br>10<br>20<br>10 | -<br>-<br>-<br>20 | -<br>-<br>-<br>- | -<br>ns<br>ns<br>- |
| Pulse Width<br>STROBE<br>RESET  | $t_{SPW}$<br>$t_{RPW}$                             | 20<br>20             | -<br>-            | -<br>-           | ns<br>ns           |
| RESET Turn OFF to<br>Output Delay   | $t_{PHZ}$  | -                    | 70                | 100              | ns                 |



**Timing Diagram**



**TRUTH TABLE X AXIS**

| X ADDRESS |     |     |     | SEE NOTE | X SWITCH   |
|-----------|-----|-----|-----|----------|------------|
| AX3       | AX2 | AX1 | AX0 |          |            |
| 0         | 0   | 0   | 0   |          | X0         |
| 0         | 0   | 0   | 1   |          | X1         |
| 0         | 0   | 1   | 0   |          | X2         |
| 0         | 0   | 1   | 1   |          | X3         |
| 0         | 1   | 0   | 0   |          | X4         |
| 0         | 1   | 0   | 1   |          | X5         |
| 0         | 1   | 1   | 0   | (1)      | No Connect |
| 0         | 1   | 1   | 1   | (1)      | No Connect |
| 1         | 0   | 0   | 0   |          | X6         |
| 1         | 0   | 0   | 1   |          | X7         |
| 1         | 0   | 1   | 0   |          | X8         |
| 1         | 0   | 1   | 1   |          | X9         |
| 1         | 1   | 0   | 0   |          | X10        |
| 1         | 1   | 0   | 1   |          | X11        |
| 1         | 1   | 1   | 0   | (1)      | No Connect |
| 1         | 1   | 1   | 1   | (1)      | No Connect |

**TRUTH TABLE Y AXIS**

| Y ADDRESS |     |     |  | SEE NOTE | Y SWITCH |
|-----------|-----|-----|--|----------|----------|
| AY2       | AY1 | AY0 |  |          |          |
| 0         | 0   | 0   |  |          | Y0       |
| 0         | 0   | 1   |  |          | Y1       |
| 0         | 1   | 0   |  |          | Y2       |
| 0         | 1   | 1   |  |          | Y3       |
| 1         | 0   | 0   |  |          | Y4       |
| 1         | 0   | 1   |  |          | Y5       |
| 1         | 1   | 0   |  |          | Y6       |
| 1         | 1   | 1   |  |          | Y7       |

NOTE: (1) When X switch addresses are in these states, no change in status will occur in switches between any X and Y points.

To make a connection (close switch) between any two points, specify an "X" address, a "Y" address, set "Data" high, and switch "Strobe" from low to high to break a connection, follow this same procedure with "Data" low.

Example:

- To connect switch X3 to switch Y4:
- To connect switch X6 to switch Y7:
- To break connection from X3 to Y4:

| DATA | X ADDRESS |     |     |     | Y ADDRESS |     |     |
|------|-----------|-----|-----|-----|-----------|-----|-----|
|      | AX3       | AX2 | AX1 | AX0 | AY2       | AY1 | AY0 |
| 1    | 0         | 0   | 1   | 1   | 1         | 0   | 0   |
| 1    | 1         | 0   | 0   | 0   | 1         | 1   | 1   |
| 0    | 0         | 0   | 1   | 1   | 1         | 0   | 0   |

August 1991

### Features

- 128 Analog Switches
- Low  $R_{ON}$
- Guaranteed  $R_{ON}$  Matching
- Analog Signal Input Voltage Equal to the Supply Voltage
- Wide Operating Voltage: 4V to 14V
- Parallel Input Addressing
- High Latch Up Current: 50mA Minimum
- Very Low Crosstalk
- Pin And Functionally Compatible with the Following Types: SGS M3494 and Mitel MT8816

### Applications

- PBX Systems
- Instrumentation
- Analog And Digital Multiplexers
- Video Switching Networks

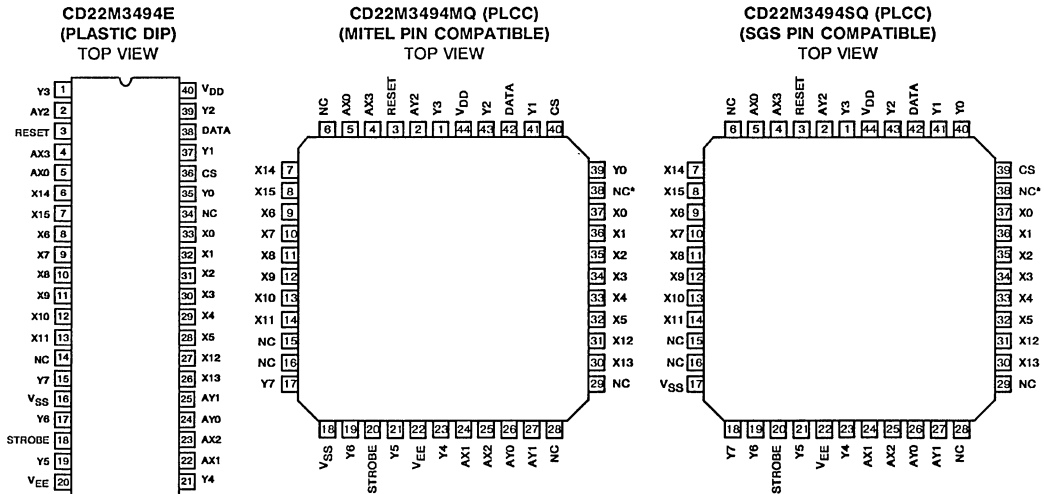
### Description

The Harris CD22M3494 is an array of 128 analog switches capable of handling signals from DC to video. Because of the switch structure, input signals may swing through the total supply voltage range,  $V_{DD}$  to  $V_{SS}$ . Each of the 128 switches may be addressed via the ADDRESS input to the 7 to 128 line decoder. The state of the addressed switch is established by the signal to the DATA input. A low or zero input will open the switch, while a high logic level or a one will result in closure of the addressed switch when the STROBE input goes high from its normally low state. Any number or combination of connections may be active at one time. Each connection, however, must be made or broken individually in the manner previously described. All switches may be reset by taking the RESET input from a zero state to a one state and then returning it to its normal low state.

CS allows crosspoint array to be cascaded for matrix expansion.

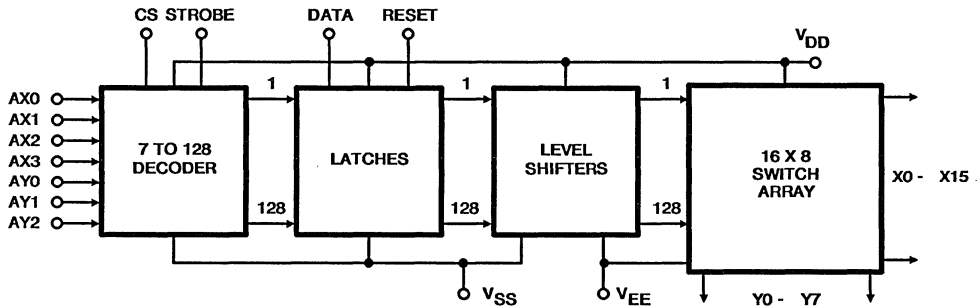
The CD22M3494 is offered both in Plastic DIP ('E' suffix) and in PLCC ('Q' suffix). The device is operational over the entire Industrial temperature range (-40°C to +85°C) in both packages.

### Pinouts



## CD22M3494

### Block Diagram



### Pin Descriptions

| SYMBOL                           | 40 PIN<br>PLASTIC DIP                | 44 PIN<br>PLCC                       |      | DESCRIPTION  |
|----------------------------------|--------------------------------------|--------------------------------------|------|--|
|                                  | (E)                                  | (MQ)                                 | (SQ) |  |
| <b>POWER SUPPLIES</b>            |                                      |                                      |      |  |
| V <sub>DD</sub>                  | 40                                   | 44                                   | 44   | Positive Supply  |
| V <sub>SS</sub>                  | 16                                   | 18                                   | 17   | Negative Supply (Digital)  |
| V <sub>EE</sub>                  | 20                                   | 22                                   | 22   | Negative Supply (Analog)   |
| <b>ADDRESS</b>                   |                                      |                                      |      |  |
| AX0 - AX3                        | 5, 22, 23,<br>& 4                    | 5, 24, 25,<br>& 4                    |      | X Address Lines. These pins select one of the 16 rows of switches. See the Truth Table for the valid addresses.  |
| AY0 - AY2                        | 24, 25,<br>& 2                       | 26, 27,<br>& 2                       |      | Y Address Lines. These pins select one of the 8 columns of switches. See the Truth Table for the valid addresses.  |
| <b>CONTROL</b>                   |                                      |                                      |      |  |
| DATA                             | 38                                   | 42                                   |      | DATA Input determines the state of the addressed switch. A high or one will close the switch. A low or zero will open the switch.  |
| STROBE                           | 18                                   | 20                                   |      | STROBE Input enables the action defined by the DATA and ADDRESS Inputs. A low or zero results in no action. The ADDRESS Input must be stable before the STROBE Input goes to the active high level. The DATA Input must be stable on the falling edge of the STROBE. |
| RESET                            | 3                                    | 3                                    |      | MASTER RESET. A high or one on this line opens all switches.   |
| CS                               | 36                                   | 40                                   | 39   | CHIP SELECT. Device is selected when CS is at a high level, allows the crosspoint array to be cascaded for matrix expansion.   |
| <b>INPUTS/OUTPUTS</b>            |                                      |                                      |      |  |
| X0 - X5<br>X6 - X11<br>X12 - X15 | 33 - 28<br>8 - 13<br>27, 26, 6, 7    | 37 - 32<br>9 - 14<br>31, 30, 7, 8    |      | Analog or Digital Inputs/Outputs. These pins are the rows X0 - X15.  |
| Y0 - Y7<br>I/O                   | 35, 37, 39,<br>1, 21, 19,<br>17 & 15 | 40, 41, 43,<br>1, 23, 21,<br>19 & 18 |      | Analog or Digital Inputs/Outputs. These pins are the columns Y0 - Y7.  |

## Specifications CD22M3494

### Absolute Maximum Ratings

DC Supply Voltage ( $V_{DD}$ ):

(Voltages Referenced to  $V_{SS}$ ) ..... -0.5 to +15V

DC Input Diode Current,  $I_{IN}$  .....  $\pm 20$ mA  
(For  $V_I < V_{SS} - 0.5V$  or  $V_I > V_{DD} + 0.5V$ )

DC Output Diode Current,  $I_{OK}$  .....  $\pm 20$ mA

(For  $V_O < V_{SS} - 0.5V$  or  $V_O > V_{DD} + 0.5V$ )

DC Transmission Gate Current .....  $\pm 25$ mA

Power Dissipation Per Package ( $P_o$ ):

For  $T_A = -40$  to  $+60^\circ\text{C}$  ..... 500mW

(Package Type E, 40 Pin Plastic DIP)

For  $T_A = +60^\circ\text{C}$  to  $+85^\circ\text{C}$  Derate Linearly .. 12mW/ $^\circ\text{C}$  to 200mW

For  $T_A = -40$  to  $+85^\circ\text{C}$  ..... 600mW

(Package Type Q, 44 Pin PLCC)

Operating Temperature Range ( $T_A$ ):

Package Type E and Q ..... -40 to  $85^\circ\text{C}$

Storage Temperature Range ( $T_{STG}$ ) ..... -65 to  $150^\circ\text{C}$

Lead Temperature (During Soldering) For 10 sec max:

At a distance 1/16  $\pm$  1/32 in. (1.59  $\pm$  0.79mm) .....  $+265^\circ\text{C}$

From case for 10 sec max

\*Printed-circuit board mount 57mm x 57mm minimum area x 1.6mm thick GIO epoxy glass or equivalent.

### Recommended Operating Conditions:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC   | LIMITS   |          | UNITS |
|--|----------|----------|-------|
|  | MIN      | MAX      |       |
| Supply Voltage Range (For $T_A =$ Full Package Temperature Range) $V_{SS} = 0V$ , $V_{EE} = 0V$ , $V_{DD}$ | 4        | 14       | V     |
| DC Input or Output Voltage $V_I$ or $V_O$  | $V_{EE}$ | $V_{DD}$ | V     |
| Digital Input Voltage  | $V_{SS}$ | $V_{DD}$ | V     |

### Dynamic Electrical Characteristics ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ ) $V_{SS} = V_{EE} = 0V$ , Unless Otherwise Specified

| CHARACTERISTIC <sup>925</sup>      | CONTROLS CONDITIONS                    | MIN | TYP | MAX        | UNITS         |
|------------------------------------|--|-----|-----|------------|---------------|
| Supply Current, $I_{DD}$           | $V_{DD} = 5V$ Logic Inputs = $V_{DD}$  | -   | -   | 2          | mA            |
|                                    | $V_{DD} = 16V$ Logic Inputs = $V_{DD}$ | -   | -   | 5          | mA            |
| High-Level Input Voltage, $V_{IH}$ |  | 2.4 | -   | -          | V             |
| Low-Level Input Voltage, $V_{IL}$  |  | -   | -   | 0.8        | V             |
| Input Leakage Current, $I_{IN}$    |  | -   | -   | $\pm 10^*$ | $\mu\text{A}$ |

| CHARACTERISTIC  | CROSSPOINTS CONDITIONS  | MIN | TYP | MAX       | UNITS    |
|---|---|-----|-----|-----------|----------|
| ON Resistance $R_{ON}$  | $V_{SS} = V_{EE} = 0V$<br>$T_A = +25^\circ\text{C}$ ,<br>$V_{IN} = V_{DD}/2$<br>$V_X - V_Y = 0.2V$ $V_{DD} = 10V$                         | -   | 40  | 75        | $\Omega$ |
|   | $V_{DD} = 12V$  | -   | 36  | 65        | $\Omega$ |
| ON Resistance $R_{ON}$  | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$<br>$V_{IN} = V_{DD}/2$<br>$V_X - V_Y = 0.2V$<br>$V_{SS} = V_{EE} = 0V$ $V_{DD} = 10V$    | -   | 50  | 90        | $\Omega$ |
|   | $V_{DD} = 12V$  | -   | 45  | 80        | $\Omega$ |
| Difference in ON Resistance between any two switches, $\Delta R_{ON}$ | $T_A = +25^\circ\text{C}$ ,<br>$V_{IN} = V_{DD}/2$<br>$V_X - V_Y = 0.2V$<br>$V_{SS} = V_{EE} = 0V$ $V_{DD} = 12V$                         | -   | 6   | 10        | $\Omega$ |
| Difference in ON Resistance between any two switches, $\Delta R_{ON}$ | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$<br>$V_{IN} = V_{DD}/2$<br>$V_X - V_Y = 0.2V$<br>$V_{SS}$ or $V_{DD} = 0V$ $V_{DD} = 12V$ | -   | -   | 10        | $\Omega$ |
| Input Leakage Current, $I_L$ (Digital Pins)                           | $V_{IN}$ (Digital) = $V_{SS}$ or $V_{DD}$ , $T_A = +25^\circ\text{C}$   | -   | -   | $\pm 100$ | nA       |
|   | $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$  | -   | -   | $\pm 3$   | nA       |

\*At  $+25^\circ\text{C}$  Limit is  $\pm 100$ nA

## Specifications CD22M3494

### Dynamic Electrical Characteristics (Continued)

(T<sub>A</sub> = +25°C), V<sub>SS</sub> = 0V, V<sub>EE</sub> = 0V, V<sub>DD</sub> = 14V, C<sub>L</sub> = 50pF, Unless Otherwise Specified

| CHARACTERISTIC  | CROSSPOINTS CONDITIONS   | MIN | TYP  | MAX | UNITS |
|---|--|-----|------|-----|-------|
| Switch I/O Capacitance  | V <sub>IN</sub> = V <sub>DD</sub> /2, f = 1MHz   | -   | -    | 20  | pF    |
| Switch Feedthrough Capacitance  | V <sub>IN</sub> = V <sub>DD</sub> /2, f = 1MHz   | -   | 0.3  | -   | pF    |
| Propagation Delay Time (switch ON)<br>Signal Input to Output<br>t <sub>PHL</sub> or t <sub>PLH</sub>  |  | -   | 30   | 100 | ns    |
| Frequency Response Channel ON<br>f = 20log (V <sub>X</sub> /V <sub>Y</sub> ) = -3dB                   | C <sub>L</sub> = 3pF, R <sub>L</sub> = 75Ω, V <sub>IN</sub> = 2VP-P  | -   | 50   | -   | MHz   |
| Total Harmonic<br>T <sub>HD</sub>   | V <sub>IN</sub> = 2VP-P, f = 1kHz  | -   | 0.01 | -   | %     |
| Feedthrough Channel OFF<br>Feedthrough =<br>20log (V <sub>X</sub> /V <sub>Y</sub> ) = F <sub>DT</sub> | V <sub>IN</sub> = 2VP-P, f = 1kHz  | -   | -95  | -   | dB    |
| Frequency for Signal Crosstalk, f <sub>CT</sub>   | 40dB, V <sub>IN</sub> = 2VP-P, R <sub>L</sub> = 75Ω  | -   | 10   | -   | MHz   |
| Attenuation of:   | 1.10dB, V <sub>IN</sub> = 2VP-P, R <sub>L</sub> = 1k    10pF   | -   | 5    | -   | kHz   |
| Control Crosstalk<br>DATA-Input, ADDRESS,<br>or STROBE to Output                                      | Control Input = 3VP-P<br>Square Wave, tr = tf = 10ns<br>R <sub>IN</sub> = 1K, R <sub>OUT</sub> = 10K    10pF | -   | 75   | -   | mVPK  |

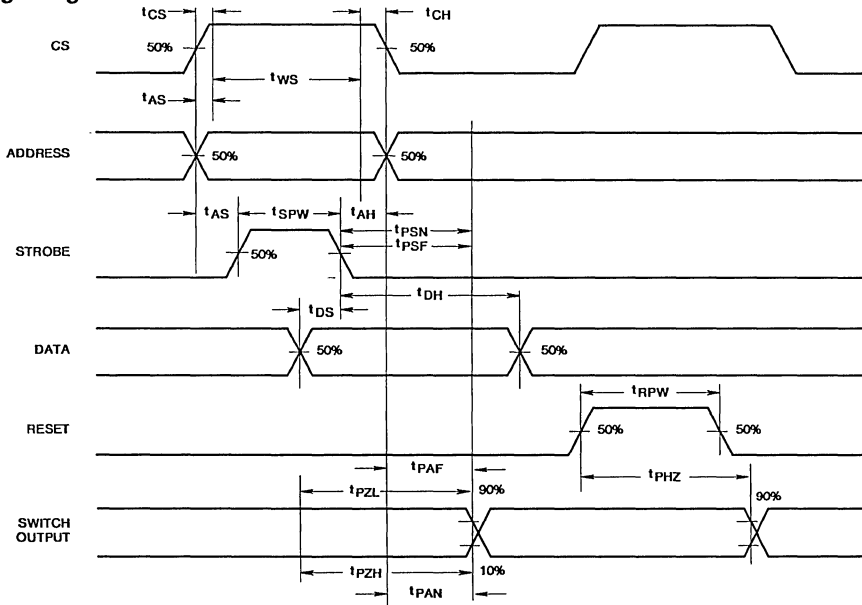
### Dynamic Electrical Characteristics

(T<sub>A</sub> = +25°C), V<sub>SS</sub> = 0V, V<sub>EE</sub> = 0V, V<sub>DD</sub> = 14V, R<sub>L</sub> = 1K || 50pF, Unless Otherwise Specified

| CHARACTERISTIC  | CONTROLS CONDITIONS                                       | MIN                  | TYP              | MAX              | UNITS                 |
|---|---|----------------------|------------------|------------------|-----------------------|
| Digital Input Capacitance   | C <sub>IN</sub> V <sub>IN</sub> = 5V, f = 1MHz            | -                    | 5                | -                | pF                    |
| Propagation Delay Time<br>STROBE to Output<br>(Switch turn-ON)<br>(Switch turn-OFF)                   | t <sub>PSN</sub><br>t <sub>PSF</sub>                      | -<br>-               | 50<br>50         | 100<br>100       | ns<br>ns              |
| DATA-in to Output<br>(Turn-ON to high level)<br>(Turn-ON to low level)                                | t <sub>PZH</sub><br>t <sub>PZL</sub>                      | -<br>-               | 60<br>70         | 100<br>100       | ns<br>ns              |
| ADDRESS to Output<br>(Turn-ON to high level)<br>(Turn-OFF to low level)                               | t <sub>PAN</sub><br>t <sub>PAF</sub>                      | -<br>-               | 70<br>70         | -<br>-           | ns<br>ns              |
| Set-up Time<br>CS to STROBE<br>DATA-in to STROBE<br>ADDRESS to STROBE                                 | t <sub>CS</sub><br>t <sub>DS</sub><br>t <sub>AS</sub>     | 10<br>10<br>10       | -<br>-<br>-      | -<br>-<br>-      | ns<br>ns<br>ns        |
| Hold Time<br>STROBE to CS<br>ADDRESS to CS<br>STROBE to DATA-in<br>STROBE to ADDRESS<br>DATA-in to CS | t <sub>CH</sub><br><br>t <sub>DH</sub><br>t <sub>AH</sub> | 10<br>10<br>20<br>10 | -<br>-<br>-<br>- | -<br>-<br>-<br>- | <br><br>ns<br>ns<br>- |
| Pulse Width<br>STROBE<br>RESET  | t <sub>SPW</sub><br>t <sub>RPW</sub>                      | 20<br>20             | -<br>-           | -<br>-           | ns<br>ns              |
| RESET Turn OFF to<br>Output Delay   | t <sub>PHZ</sub>  | -                    | 70               | 100              | ns                    |

## Specifications CD22M3494

### Timing Diagram



TRUTH TABLE X AXIS

| X ADDRESS |     |     |     |     | SEE NOTE | X SWITCH |
|-----------|-----|-----|-----|-----|----------|----------|
| AX3       | AX2 | AX1 | AX0 |     |          |          |
| 0         | 0   | 0   | 0   |     | X0       |          |
| 0         | 0   | 0   | 1   |     | X1       |          |
| 0         | 0   | 1   | 0   |     | X2       |          |
| 0         | 0   | 1   | 1   |     | X3       |          |
| 0         | 1   | 0   | 0   |     | X4       |          |
| 0         | 1   | 0   | 1   |     | X5       |          |
| 0         | 1   | 1   | 0   |     | X12      |          |
| 0         | 1   | 1   | 1   |     | X13      |          |
| 1         | 0   | 0   | 0   |     | X6       |          |
| 1         | 0   | 0   | 1   |     | X7       |          |
| 1         | 0   | 1   | 0   |     | X8       |          |
| 1         | 0   | 1   | 1   |     | X9       |          |
| 1         | 1   | 0   | 0   |     | X10      |          |
| 1         | 1   | 0   | 1   |     | X11      |          |
| 1         | 1   | 1   | 0   | (1) | X14      |          |
| 1         | 1   | 1   | 1   | (1) | X15      |          |

TRUTH TABLE Y AXIS

| Y ADDRESS |     |     |          |          |
|-----------|-----|-----|----------|----------|
| AY2       | AY1 | AY0 | SEE NOTE | Y SWITCH |
| 0         | 0   | 0   |          | Y0       |
| 0         | 0   | 1   |          | Y1       |
| 0         | 1   | 0   |          | Y2       |
| 0         | 1   | 1   |          | Y3       |
| 1         | 0   | 0   |          | Y4       |
| 1         | 0   | 1   |          | Y5       |
| 1         | 1   | 0   |          | Y6       |
| 1         | 1   | 1   |          | Y7       |

To make a connection (close switch) between any two points, specify an "X" address, a "Y" address, set "Data" high, and switch "Strobe" from low to high to break a connection, follow this same procedure with "Data" low.

Example:

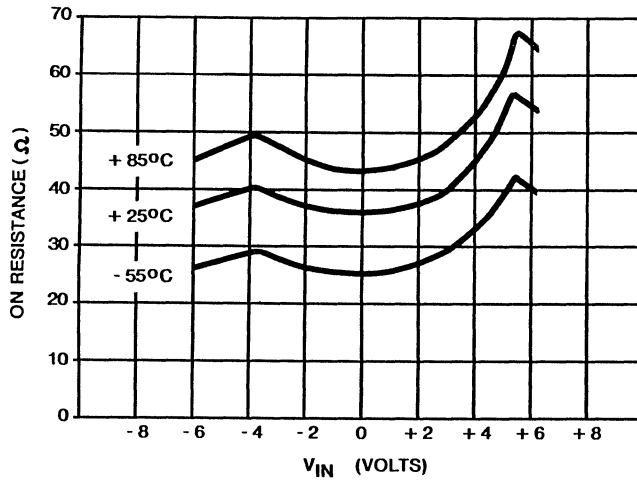
- To connect switch X3 to switch Y4:
- To connect switch X6 to switch Y7:
- To break connection from X3 to Y4:

| DATA | X ADDRESS |     |     |     | Y ADDRESS |     |     |
|------|-----------|-----|-----|-----|-----------|-----|-----|
|      | AX3       | AX2 | AX1 | AX0 | AY2       | AY1 | AY0 |
| 1    | 0         | 0   | 1   | 1   | 1         | 0   | 0   |
| 1    | 1         | 0   | 0   | 0   | 1         | 1   | 1   |
| 0    | 0         | 0   | 1   | 1   | 1         | 0   | 0   |

# CD22M3494

## Voltage and Resistance

RON vs. VIN  
@ -55°C, +25°C and +85°C  
VEE = -5V, VSS = 0V, VDD = 5V



**Features**

- Mute Drivers On-Chip
- Device Power can Either be Regulated DC or Telephone Loop Current
- Use of an Inexpensive 3.579545MHz TV Crystal Provides High Accuracy and Stability for all Frequencies

**Applications**

- For Use In Dual-tone Telephone Dialing Systems

**Description**

The CD22859 is a CMOS dual-tone multifrequency (DTMF) tone generator for use in dual-tone telephone dialing systems. The device can easily be interfaced to a standard pushbutton telephone keyboard, to provide enabling operation directly with the telephone lines.

The CD22859 generates standard DTMF sinusoidal dialing tones from an on-chip reference crystal oscillator. The reference oscillator uses an inexpensive 3.579545MHz color TV crystal to create highly stable and accurate tones. The sinusoidal tones are digitally synthesized by a stair-step approximation.

One of four low-frequency band row tones and one of four high-frequency band column tones are selected by driving one of the four row inputs and one of the four column inputs low. Simultaneous selection of more than one row input and/or more than one column input will inhibit tone generation, or generate a single-tone sinusoid. These operating modes are described in the functional truth table.

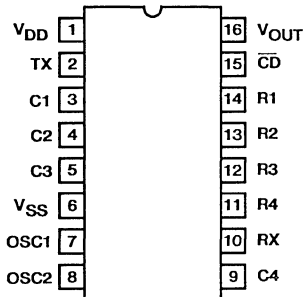
Control logic is included to allow easy interface to standard K500-types telephones. Two CMOS outputs Tx, Rx capable of driving external p-n-p receiver and transmitter muting transistors are provided. A low input to the CD pin, inhibits tone generation, turns off the reference oscillator and causes Tx and Rx outputs to logic '0'. During tone generation mode, CD = 1 and Tx, Rx = logic 1.

All row, column and CD inputs are provided with pull-up resistors to allow the use of SPST switch matrixes.

The CD22859 types are supplied in a 16 lead hermetic dual-in-line sidebraced ceramic package (D suffix) and a 16 lead dual-in-line plastic package (E suffix).

**Pinout**

CD22859 TYPES  
16 PIN CERAMIC SIDEBRAZED  
16 PIN PLASTIC DIP  
TOP VIEW





## Specifications CD22859

### Absolute Maximum Ratings

|   |   |   |   |
|---|---|---|---|
| DC Supply Voltage Range ( $V_{DD} - V_{SS}$ ) | ..... -0.5V to +12V                     | Power Dissipation Per Output                                    | ..... 100mW                             |
| Input Voltage Range                           | ..... -0.5V to $V_{DD} + 0.5V$          | Operating Temperature Range                                     | ..... -40°C to +85°C                    |
| Power Dissipation, $P_D$ :                    |   | Lead Temperature During Soldering: Distance 1/16 in. ± 1/32 in. | (1.59mm ± 0.79mm) from case for 10s max |
| $T_A = -40°C$ to $+60°C$                      | ..... 500mW                             |   | ..... +265°C                            |
| $T_A = +60°C$ to $+85°C$                      | .. Derate Linearly at 1.2mW/°C to 200mW |   |   |

### Dynamic Electrical Characteristics $T_A = -25°C$ to $+60°C$ All Voltages Referenced to $V_{SS} = 0V$

| CHARACTERISTICS                                | $V_{DD}$ | LIMITS |              | UNITS |
|--|----------|--------|--------------|-------|
|  |          | MIN    | MAX          |       |
| <b>DC SUPPLY VOLTAGE</b>                       |          |        |              |       |
| Tone Generation Mode with Valid Input (Note 1) |          | 2.5    | 10           | V     |
| Non-Tone Generation (Note 2)                   |          | 1.7    | 10           | V     |
| <b>OPERATING CURRENT</b>                       |          |        |              |       |
| Tone Generation Mode<br>Outputs Unloaded)      | 3.7V     | -      | 2.7          | mA    |
|  | 9.3V     | -      | 13           | mA    |
| No Keydown Mode                                | 3.7V     | -      | 100          | μA    |
|  | 9.3V     | -      | 200          | μA    |
| Input Pull-Up Current                          | 3V-10V   | -      | 400          | μA    |
| Input Low Voltage ( $V_{IL}$ ) Maximum         | 3V-10V   | -      | 0.2 $V_{DD}$ | V     |
| Input Low Voltage ( $V_{IH}$ ) Minimum         | 3V-10V   | -      | 0.8 $V_{DD}$ | V     |

### Static Electrical Characteristics $T_A = -25°C$ to $+60°C$

| CHARACTERISTICS                                      | $V_{DD}$ | $V_O$ | LIMITS    |           | UNITS |
|--|----------|-------|-----------|-----------|-------|
|  |          |       | MIN       | MAX       |       |
| <b>TONE OUTPUTS (<math>R_L = 82</math>)</b>          |          |       |           |           |       |
| $V_O$ ; Dual-Tone Output                             | 3.7-9.3  | -     | 350       | 700       | mVrms |
| $V_O$ ( $C_L$ ); Single-Tone Output, Column (Note 3) | 3.7-9.3  | -     | 300       | -         | mVrms |
| $V_O$ ( $R_L$ ); Single-Tone Output, Row (Note 4)    | 3.7-9.3  | -     | 260       | -         | mVrms |
| Distortion (Note 5)                                  | 3.9-9.3  | -     | -         | 10        | %     |
| Rise and Fall Time (Dual-Tone Out) (Note 6)          | 3.9-9.3  | -     | -         | 5         | ms    |
| Pre-Emphasis (Note 7)                                | 3.9-9.3  | -     | (Nom.-1%) | (Nom.+1%) | Hz    |
| <b>MUTE OUTPUT CURRENT</b>                           |          |       |           |           |       |
| Transmitter  | 1.7      | 1.2   | -0.5      | -         | mA    |
| $I_{OH}$ (Source)                                    | 10       | 9.5   | -3.4      | -         | mA    |
| $I_{OL}$ (Sink)                                      | 10       | 2.5   | -         | 10        | μA    |
| Receiver   | 1.7      | 1.2   | -0.5      | -         | mA    |
| $I_{OH}$ (Source)                                    | 10       | 9.5   | -3.4      | -         | mA    |
| $I_{OL}$ (Sink)                                      | 10       | 2.5   | -         | 10        | μA    |

#### NOTES:

- All logic and counters functional.
- Mute switches remain open.
- Two or more row inputs low, and one column input low.
- Two or more column inputs low, and one row input low.
- Distortion is defined as: The ratio of all extraneous frequency components generated in the voiceband 0.5kHz, to the power of the dual-tone signal, measure across  $R_L$ .
- Tone rise time is defined as the time for each of the 2 DTMF frequencies to attain 90% of full amplitude, measured from the time when a row and column signal are driven low.
- Pre-emphasis is the ratio of the high-group level to the low-group level.
- Refer to Figure 1. for standard DTMF frequencies.

$$= \frac{(V_1^2 + V_2^2 = \dots + V_n^2)}{V_L^2 + V_H^2}$$

where  $V_1, V_2, \dots, V_n$  are extraneous frequency components in the voiceband 0.5kHz to 3kHz,  $V_L$  is the low-band frequency tone, and  $V_H$  is the high-band frequency tone.

# CD22859

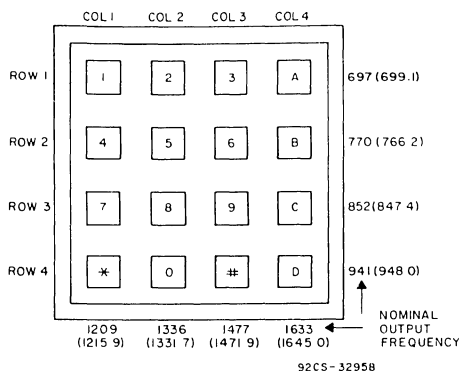


Fig. 1 - Bell and nominal output frequencies (in parenthesis) for 3.579545-MHz crystal.

### DTMF Generator Functional Truth Table

| Keyboard Mode                                    | Inputs                                  |                                    | $\overline{CD}$ | Tone   | Outputs     |     |     |
|--|---|------------------------------------|-----------------|--|-------------|-----|-----|
|  | Number of Column Inputs Activated "Low" | Number of Row Inputs Activated Low |                 |  | OSC Running | RX  | TX  |
| X<br>No key depressed                            | X                                       | X                                  | "0"             | None   | No          | "0" | "0" |
|  | 0                                       | 0                                  | "1"             | None   | No          | "0" | "0" |
|  | 0                                       | 1                                  | "1"             | Dual Tone<br>R <sub>a</sub> , C <sub>1</sub> | Yes         | "1" | "1" |
| Normal Dialing<br>One Key Depressed (See Note 1) | 1,2,3, or 4                             | 0                                  | "1"             | None   | No          | "0" | "0" |
|  | 1                                       | 1                                  | "1"             | Dual Tone<br>R <sub>a</sub> , C <sub>b</sub> | Yes         | "1" | "1" |
| Two or More Keys In Same Row (See Note 2)        | 2,3, or 4                               | 1                                  | "1"             | Single Row Tone<br>R <sub>a</sub>            | Yes         | "1" | "1" |
| Two or More Keys In Same Column                  | 1                                       | 2,3, or 4                          | "1"             | Single Column Tone<br>C <sub>b</sub>         | Yes         | "1" | "1" |
| Two or More Keys In Different Rows & Columns     | 2,3 or 4                                | 1                                  | "1"             | None   | Yes         | "1" | "1" |
|  | 1                                       |                                    | 1               | None   | Yes         | "1" | "1" |

Where:

X = Do Not Care

R<sub>a</sub>, C<sub>b</sub> refers to Tone Output frequencies corresponding to Row 1, Row 2, Row 3, Row 4, Column 1, Column 2, Column 3, Column 4

a = 1,2,3,4    b = 1,2,3,4    a = b, or a ≠ b

1. Corresponds to normal dual-tone operation.
2. Corresponds to single-tone generation mode.

CD22859

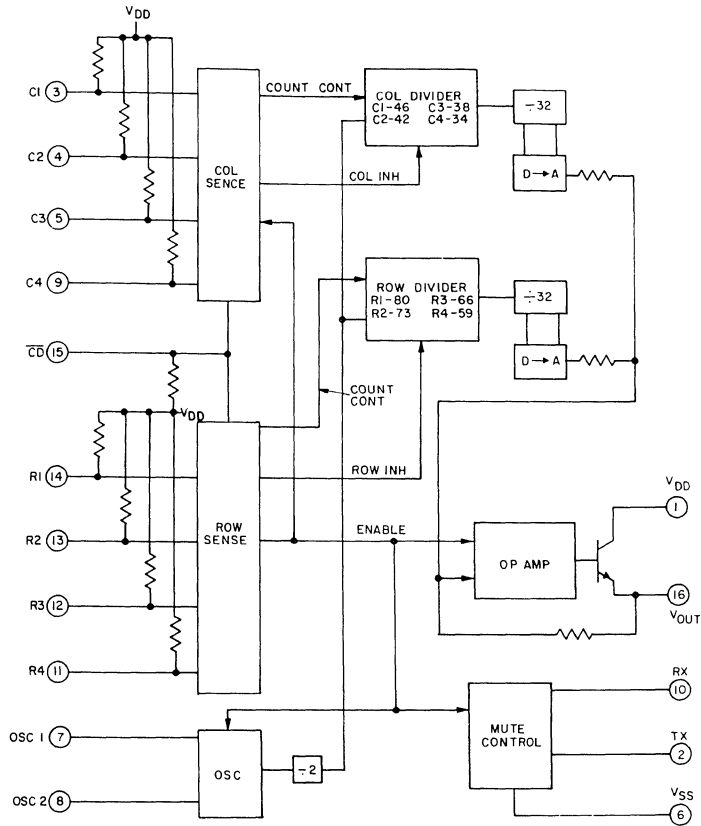


Fig. 2 - Touch-tone generator.

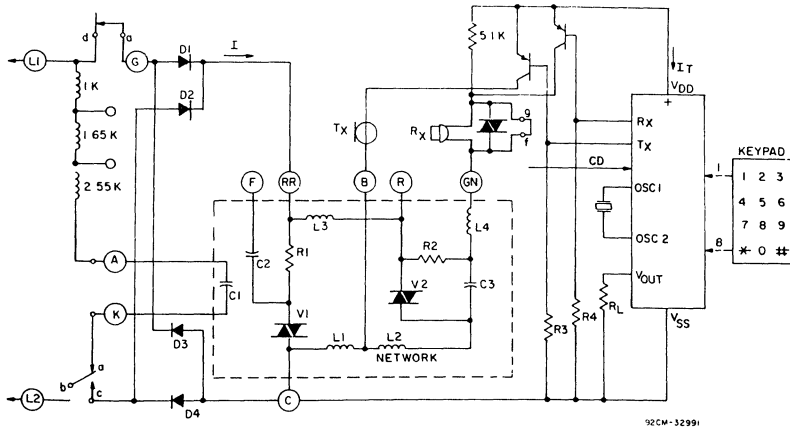


Fig. 3 - Interface with standard K500 telephone network.

# CD74HC22106 CD74HCT22106

CMOS 8 x 8 x 1 Crosspoint  
Switch with Memory Control

August 1991

### Type Features

- 64 Analog Switches in an 8 x 8 x 1 Array
- On-Chip Line Decoder and Control Latches
- Automatic Power-Up Reset by Using a 0.1 $\mu$ F Capacitor at the MR Pin
- RON Resisted 95 $\Omega$  @ VCC = 4.5V
- 2V to 10V Operation
- 4.5V to 5.5V Operation
- Analog Signal Capability: VCC2

### Family Features

- Wide Operating Temp. Range ..... -40 $^{\circ}$ C to +85 $^{\circ}$ C
- CD74HC Types:
  - ▶ 2V to 10V Operation
  - ▶ High Noise Immunity: N<sub>IL</sub> = 30%, N<sub>IH</sub> = 30% of VCC; @ VCC = 5V and 10V
- CD74HCT Types:
  - ▶ 4.5V to 5.5V Operation
  - ▶ Direct LSTTL Input Logic Compatibility: V<sub>IL</sub> = 0.8V Max, V<sub>IH</sub> = 2V Min
  - ▶ CMOS Input Compatibility: I<sub>I</sub> < 1 $\mu$ A @ V<sub>OL</sub>, V<sub>OH</sub>

### Description

The CD74HC22106 and CD74HCT22106 are digitally controlled analog switches which utilize silicon-gate CMOS technology. The CD74HC22106 types feature CMOS input-voltage-level compatibility and the CD74HCT22106 feature LSTTL input-voltage-level compatibility.

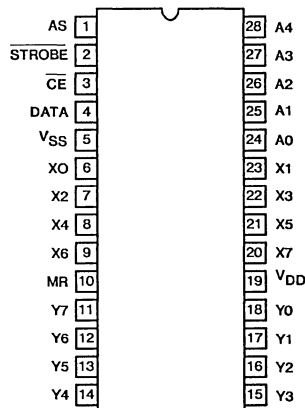
The Master Reset has an internal pull-up resistor and is normally used with a 0.1 $\mu$ F capacitor. During power-up all switches are automatically reset. The crosspoint switches will reset with MR = 0 even if CE is high. A 6-bit address through a 6-line-to-64-line decoder selects the transmission gate which can be turned on by applying a logical ONE to the DATA input and logical ZERO to the STROBE. Similarly, any transmission gate can be turned OFF by applying a logical ZERO to the DATA input while strobing the STROBE with a logical ZERO.

The CE pin allows the crosspoint array to be cascaded for matrix expansion in both the X and Y directions.

The CD74HC and CD74HCT devices are supplied in the 28 lead dual-in-line plastic packages (E suffix).

### Pinout

CD74HC22106, CD74HCT22106  
28 PIN PLASTIC DIP  
TOP VIEW



## Specifications CD74HC22106, CD74HCT22106

### Absolute Maximum Ratings

DC Supply-Voltage ( $V_{CC}$ ):  
 Voltage Reference to GND ..... -0.5V to +11V  
 DC Input Diode Current:  
 $I_{IK}$  (For  $V_I < -0.5$  or  $V_I > V_{CC} + 0.5V$ ) .....  $\pm 20mA$   
 DC Output Diode Current:  
 $I_{OK}$  (For  $V_O < -0.5$  or  $V_O > V_{CC} + 0.5V$ ) .....  $\pm 20mA$   
 DC Transmission Gate Current .....  $\pm 25mA$   
 Power Dissipation per Package ( $P_D$ ):  
 For  $T_A = -40^\circ C$  to  $+60^\circ C$  (Package Type E) ..... 500mW  
 For  $T_A = -60^\circ C$  to  $+85^\circ C$  (Package Type E) ... Derate Linearly at  
 12mW/ $^\circ C$  to 200mW

### Operating Temperature Range ( $T_A$ )

Package Type E .....  $-40^\circ C$  to  $+85^\circ C$   
 Storage Temperature (During Soldering) for 10s Max  
 At distance 1/16 in.  $\pm$  1/32 in. (1.59mm  $\pm$  0.79mm) for Case for  
 10s Max .....  $+265^\circ C$

**Recommended Operating Conditions:** For Maximum Reliability, Nominal Operating Conditions Should be Selected so that Operation is Always Within the Following Ranges:

| CHARACTERISTICS   | LIMITS |          | UNITS |
|---|--------|----------|-------|
|   | MIN    | MAX      |       |
| Supply Voltage Range (For $T_A =$ Full Package Temperature Range) $V_{CC}$ :<br>CD74HC22106 | 2      | 10       | V     |
| CD74HCT22106  | 4.5    | 5.5      | V     |
| DC Input of Output Voltage $V_I, V_O$   | 0      | $V_{CC}$ | V     |

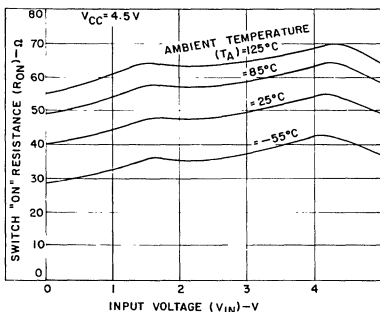


FIGURE 1. TYPICAL "ON" RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE

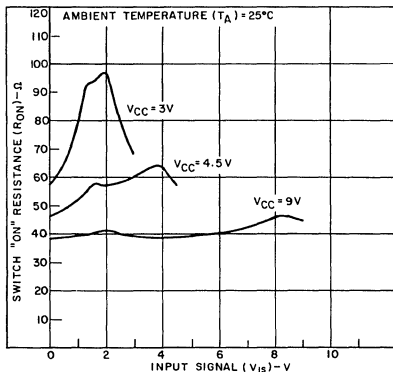


FIGURE 2. TYPICAL "ON" RESISTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE

## Specifications CD74HC22106, CD74HCT22106

### Static Electrical Characteristics

| CHARACTERISTICS   | CD74HC22106                  |                      |       |     |      |                | CDHCT22106 |   |                      |     |       |      | UNITS |                |     |   |  |
|---|------------------------------|----------------------|-------|-----|------|----------------|------------|---|----------------------|-----|-------|------|-------|----------------|-----|---|--|
|   | TEST CONDITIONS              |                      | +25°C |     |      | -40°C to +85°C |            |   | TEST CONDITIONS      |     | +25°C |      |       | -40°C to +85°C |     |   |  |
|   | V <sub>I</sub><br>V          | V <sub>CC</sub><br>V | MIN   | TYP | MAX  | MIN            | MAX        | V <sub>I</sub><br>V                                   | V <sub>CC</sub><br>V | MIN | TYP   | MAX  |       | MIN            | MAX |   |  |
| High-Level Input Voltage<br>V <sub>IH</sub>                     | -                            | 2                    | 1.5   | -   | -    | 1.5            | -          | -   | 4.5<br>to<br>5.5     | 2   | -     | -    | 2     | -              | V   |   |  |
|   | -                            | 4.5                  | 3.15  | -   | -    | 3.5            | -          | -   |                      |     |       |      |       |                |     |   |  |
|   | -                            | 9                    | 6.3   | -   | -    | 6.3            | -          | -   |                      |     |       |      |       |                |     |   |  |
| Low-Level Input Voltage<br>V <sub>IL</sub>                      | -                            | 2                    | -     | -   | 0.5  | -              | 0.5        | -   | 4.5<br>to<br>5.5     | -   | -     | 0.8  | -     | 0.8            | V   |   |  |
|   | -                            | 4.5                  | -     | -   | 1.35 | -              | 1.35       | -   |                      |     |       |      |       |                |     |   |  |
|   | -                            | 9                    | -     | -   | 2.7  | -              | 2.7        | -   |                      |     |       |      |       |                |     |   |  |
| Input Leakage Current<br>(Any Control)<br>I <sub>L</sub>        | V <sub>CC</sub><br>or<br>GND | 10                   | -     | -   | ±0.1 | -              | ±1         | Any<br>Voltage<br>Between<br>V <sub>CC</sub> &<br>GND | 5.5                  | -   | -     | ±0.1 | -     | ±1             | µA  |   |  |
| Quiescent Device<br>Current I <sub>CC</sub><br>(with MR = 1)    | V <sub>CC</sub><br>or<br>GND | 10                   | -     | -   | 5    | -              | 50         | V <sub>CC</sub><br>or<br>GND                          | 5.5                  | -   | -     | 2    | -     | 20             | µA  |   |  |
| Off Leakage Current<br>I <sub>L</sub><br>(with MR = 1)          | All<br>Switches<br>OFF       | 10                   | -     | -   | 0.1  | -              | 1          | -   | 5.5                  | -   | -     | 0.1  | -     | 1              | µA  |   |  |
| "On" Resistance<br>R <sub>ON</sub>                              | V <sub>CC</sub><br>to<br>GND | 2                    | -     | 470 | 700  | -              | 875        | -   | 4.5                  | -   | 64    | 95   | -     | 120            | Ω   |   |  |
|   |                              | 4.5                  | -     | 64  | 95   | -              | 120        |   |                      |     |       |      |       |                |     |   |  |
|   |                              | 9                    | -     | 45  | 70   | -              | 90         |   |                      |     |       |      |       |                |     |   |  |
|   | V <sub>CC</sub> /2           | -                    | -     | -   | -    | -              | -          | -   | -                    | 4.5 | -     | 58   | 85    | -              | 110 | Ω |  |
|   |                              | 4.5                  | -     | 58  | 85   | -              | 110        |   |                      |     |       |      |       |                |     |   |  |
|   |                              | 9                    | -     | 40  | 60   | -              | 80         |   |                      |     |       |      |       |                |     |   |  |
| "On" Resistance<br>Between Any Two<br>Channels ΔR <sub>ON</sub> | V <sub>CC</sub><br>to<br>GND | -                    | -     | -   | -    | -              | -          | V <sub>CC</sub><br>to<br>GND                          | 4.5                  | -   | 25    | -    | -     | -              | Ω   |   |  |
|   |                              | 4.5                  | -     | 25  | -    | -              | -          |   |                      |     |       |      |       |                |     |   |  |
|   |                              | 9                    | -     | 23  | -    | -              | -          |   |                      |     |       |      |       |                |     |   |  |

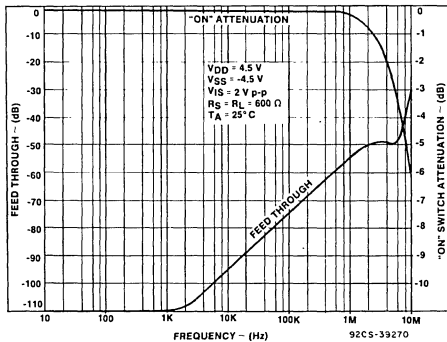


FIGURE 3. TYPICAL "ON" RESISTANCE AND CROSSTALK AS A FUNCTION OF FREQUENCY

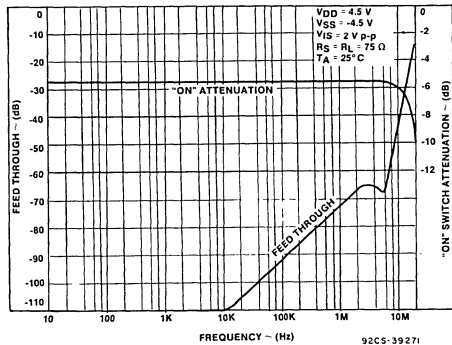


FIGURE 4. TYPICAL "ON" SWITCH ATTENUATION AND "OFF" SWITCH FEED THROUGH AS A FUNCTION OF FREQUENCY

**Specifications CD74HC22106, CD74HCT22106**

**Switching Characteristics**

| CHARACTERISTICS  | TEST CONDITIONS   | V <sub>SS</sub> | V <sub>CC</sub> | LIMITS |     |     |     |                |     |     |     | UNITS |
|--|---|-----------------|-----------------|--------|-----|-----|-----|----------------|-----|-----|-----|-------|
|  |   |                 |                 | +25°C  |     |     |     | -40°C to +85°C |     |     |     |       |
|  |   |                 |                 | HC     |     | HCT |     | HC             |     | HCT |     |       |
|  |   |                 |                 | MIN    | MAX | MIN | MAX | MIN            | MAX | MIN | MAX |       |
| <b>CONTROLS</b>  |   |                 |                 |        |     |     |     |                |     |     |     |       |
| Propagation Delay Time<br>Strobe to Output<br>(Switch Turn-On to<br>High Level) t <sub>PZH</sub> | R <sub>L</sub> = 10kΩ<br>C <sub>L</sub> = 50pF<br>t <sub>r</sub> , t <sub>f</sub> = 6ns | 0               | 2               | -      | 370 | -   | -   | -              | 385 | -   | -   | ns    |
|  |   | 0               | 4.5             | -      | 110 | -   | 120 | -              | 125 | -   | 135 | ns    |
|  |   | 0               | 9               | -      | 65  | -   | -   | -              | 70  | -   | -   | ns    |
| Data-In to Output<br>(Turn-On to High Level)<br>t <sub>PZH</sub>                                 |   | 0               | 2               | -      | 240 | -   | -   | -              | 255 | -   | -   | ns    |
|  |   | 0               | 4.5             | -      | 75  | -   | 85  | -              | 85  | -   | 95  | ns    |
|  |   | 0               | 9               | -      | 50  | -   | -   | -              | 55  | -   | -   | ns    |
| Address to Output<br>(Turn-On to High Level)<br>t <sub>PZH</sub>                                 |   | 0               | 2               | -      | 380 | -   | -   | -              | 400 | -   | -   | ns    |
|  |   | 0               | 4.5             | -      | 110 | -   | 120 | -              | 125 | -   | 135 | ns    |
|  |   | 0               | 9               | -      | 65  | -   | -   | -              | 75  | -   | -   | ns    |
| Propagation Delay Times<br>Strobe to Output)<br>t <sub>PHZ</sub>                                 |   | 0               | 2               | -      | 400 | -   | -   | -              | 420 | -   | -   | ns    |
|  |   | 0               | 4.5             | -      | 135 | -   | 150 | -              | 155 | -   | 170 | ns    |
|  |   | 0               | 9               | -      | 90  | -   | -   | -              | 100 | -   | -   | ns    |
| Data-In to Output<br>(Turn-On to Low Level)<br>t <sub>PZL</sub>                                  | 0   | 2               | -               | 240    | -   | -   | -   | 255            | -   | -   | ns  |       |
|  | 0   | 4.5             | -               | 75     | -   | 85  | -   | 85             | -   | 95  | ns  |       |
|  | 0   | 9               | -               | 50     | -   | -   | -   | 55             | -   | -   | ns  |       |
| Address to Output<br>(Turn-Off)<br>t <sub>PHZ</sub>  | 0   | 2               | -               | 420    | -   | -   | -   | 440            | -   | -   | ns  |       |
|  | 0   | 4.5             | -               | 140    | -   | 150 | -   | 155            | -   | 170 | ns  |       |
|  | 0   | 9               | -               | 95     | -   | -   | -   | 100            | -   | -   | ns  |       |
| Minimum Set-Up Time<br>(Data-In to Strobe<br>Address) t <sub>SU</sub>                            | 0   | 2               | 35              | -      | -   | -   | 40  | -              | -   | -   | ns  |       |
|  | 0   | 4.5             | 20              | -      | 20  | -   | 20  | -              | 20  | -   | ns  |       |
|  | 0   | 9               | 15              | -      | -   | -   | 15  | -              | -   | -   | ns  |       |
| Minimum Hold Time<br>(Data-In to Strobe<br>Address) t <sub>H</sub>                               | 0   | 2               | 85              | -      | -   | -   | 90  | -              | -   | -   | ns  |       |
|  | 0   | 4.5             | 25              | -      | 25  | -   | 25  | -              | 25  | -   | ns  |       |
|  | 0   | 9               | 20              | -      | -   | -   | 20  | -              | -   | -   | ns  |       |
| Minimum Strobe Pulse<br>Width<br>t <sub>W</sub>  | 0   | 2               | 200             | -      | -   | -   | 210 | -              | -   | -   | ns  |       |
|  | 0   | 4.5             | 45              | -      | 55  | -   | 55  | -              | 65  | -   | ns  |       |
|  | 0   | 9               | 25              | -      | -   | -   | 30  | -              | -   | -   | ns  |       |
| Maximum Switching<br>Frequency<br>F <sub>O</sub>   | 0   | 2               | 0.7             | -      | -   | -   | 0.6 | -              | -   | -   | MHz |       |
|  | 0   | 4.5             | 3.0             | -      | 2.8 | -   | 2.8 | -              | 2.6 | -   | MHz |       |
|  | 0   | 9               | 7               | -      | -   | -   | 6.5 | -              | -   | -   | MHz |       |
| Input (Control)<br>Capacitance C <sub>I</sub>  |   | -               | -               | -      | 10  | -   | 10  | -              | 10  | -   | pF  |       |

**Specifications CD74HC22106, CD74HCT22106**

**Analog Channel Characteristics**

| CHARACTERISTICS   | TEST CONDITIONS                                    | V <sub>IS</sub>                       | V <sub>SS</sub> | V <sub>CC</sub> | LIMITS          |                 |     |     |                |     |     |     | UNITS |
|---|--|---------------------------------------|-----------------|-----------------|-----------------|-----------------|-----|-----|----------------|-----|-----|-----|-------|
|   |  |                                       |                 |                 | +25°C           |                 |     |     | -40°C to +85°C |     |     |     |       |
|   |  |                                       |                 |                 | HC              |                 | HCT |     | HC             |     | HCT |     |       |
|   |  |                                       |                 |                 | MIN             | MAX             | MIN | MAX | MIN            | MAX | MIN | MAX |       |
| Propagation Delay Time, t <sub>PHL</sub>                        | R <sub>L</sub> = 10kΩ                              | -                                     | 0               | 2               | -               | 30              | -   | -   | -              | 33  | -   | -   | ns    |
| Signal Input to Output, t <sub>PLH</sub>                        | C <sub>L</sub> = 50pF                              | -                                     | 0               | 4.5             | -               | 20              | -   | 20  | -              | 22  | -   | 22  | ns    |
|   | t <sub>r</sub> , t <sub>f</sub> = 6ns              | -                                     | -               | 9               | -               | 15              | -   | -   | -              | 17  | -   | -   | ns    |
| Switch Frequency Response @ -3dB                                | R <sub>S</sub> = R <sub>L</sub> = 600Ω             | 2V <sub>p-p</sub>                     | -2.25           | 2.25            | Typical<br>5    | Typical<br>5    | -   | -   | -              | -   | -   | -   | MHz   |
|   |  | 2V <sub>p-p</sub>                     | -4.5            | 4.5             | 6               | 6               | -   | -   | -              | -   | -   | -   | MHz   |
| Crosstalk Between Any Two Channels                              | R <sub>S</sub> = R <sub>L</sub> = 600Ω<br>f = 1kHz | 2V <sub>p-p</sub>                     | -2.25           | 2.25            | Typical<br>-110 | Typical<br>-110 | -   | -   | -              | -   | -   | -   | dB    |
|   |  | 2V <sub>p-p</sub>                     | -2.25           | 2.25            | -53             | -53             | -   | -   | -              | -   | -   | -   | dB    |
|   |  | 2V <sub>p-p</sub>                     | -4.5            | 4.5             | -55             | -55             | -   | -   | -              | -   | -   | -   | dB    |
| Switch "OFF"<br>-40dB Feed Through Frequency                    | R <sub>S</sub> = R <sub>L</sub> = 600Ω             | 2V <sub>p-p</sub>                     | -2.25           | 2.25            | Typical<br>7    | Typical<br>7    | -   | -   | -              | -   | -   | -   | MHz   |
|   |  | 2V <sub>p-p</sub>                     | -4.5            | 4.45            | 8               | 8               | -   | -   | -              | -   | -   | -   | MHz   |
| Total Harmonic Distortion<br>t <sub>HD</sub>                    | R <sub>L</sub> = 10kΩ                              | 4V <sub>p-p</sub>                     | -2.25           | 2.25            | Typical<br>0.05 | Typical<br>0.05 | -   | -   | -              | -   | -   | -   | %     |
|   | f = 1kHz Sinewave                                  | 8V <sub>p-p</sub>                     | -4.5            | 4.5             | 0.05            | 0.05            | -   | -   | -              | -   | -   | -   | %     |
|   | R <sub>L</sub> = 600Ω                              | 4V <sub>p-p</sub>                     | -2.25           | 2.25            | 0.25            | 0.25            | -   | -   | -              | -   | -   | -   | %     |
|   | f = 1kHz Sinewave                                  | 7V <sub>p-p</sub>                     | -4.5            | 4.5             | 0.12            | 0.12            | -   | -   | -              | -   | -   | -   | %     |
| Control to Switch Feed-Thru Noise<br>(DATA IN, Strobe, Address) | R <sub>L</sub> = 10kΩ                              | 5                                     | 0               | 5               | Typical<br>35   | Typical<br>35   | -   | -   | -              | -   | -   | -   | mV    |
|   |  | t <sub>r</sub> , t <sub>f</sub> = 6ns | 10              | 0               | 20              | 65              | 65  | -   | -              | -   | -   | -   | mV    |
| Capacitance, C <sub>O</sub><br>X <sub>n</sub> to GND            | f = 1MHz   | -                                     | 0               | 10              | Typical<br>48   | Typical<br>48   | -   | -   | -              | -   | -   | -   | pF    |
| Y <sub>n</sub> to GND   | f = 1MHz   | -                                     | 0               | 10              | 44              | 44              | -   | -   | -              | -   | -   | -   | pF    |



CD74HC22106, CD74HCT22106

Truth Table

| A <sub>5</sub> | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> | SWITCH SELECT  |                | A <sub>5</sub> | A <sub>4</sub> | A <sub>3</sub> | A <sub>2</sub> | A <sub>1</sub> | A <sub>0</sub> | SWITCH SELECT  |                |
|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| 0              | 0              | 0              | 0              | 0              | 0              | X <sub>0</sub> | Y <sub>0</sub> | 1              | 0              | 0              | 0              | 0              | 0              | X <sub>0</sub> | Y <sub>4</sub> |
| 0              | 0              | 0              | 0              | 0              | 1              | X <sub>1</sub> | Y <sub>0</sub> | 1              | 0              | 0              | 0              | 0              | 1              | X <sub>1</sub> | Y <sub>4</sub> |
| 0              | 0              | 0              | 0              | 0              | 1              | X <sub>2</sub> | Y <sub>0</sub> | 1              | 0              | 0              | 0              | 0              | 1              | X <sub>2</sub> | Y <sub>4</sub> |
| 0              | 0              | 0              | 0              | 1              | 1              | X <sub>3</sub> | Y <sub>0</sub> | 1              | 0              | 0              | 0              | 1              | 0              | X <sub>3</sub> | Y <sub>4</sub> |
| 0              | 0              | 0              | 0              | 1              | 0              | X <sub>4</sub> | Y <sub>0</sub> | 1              | 0              | 0              | 1              | 0              | 0              | X <sub>4</sub> | Y <sub>4</sub> |
| 0              | 0              | 0              | 1              | 0              | 0              | X <sub>5</sub> | Y <sub>0</sub> | 1              | 0              | 0              | 0              | 1              | 0              | X <sub>5</sub> | Y <sub>4</sub> |
| 0              | 0              | 0              | 1              | 1              | 0              | X <sub>6</sub> | Y <sub>0</sub> | 1              | 0              | 0              | 1              | 1              | 0              | X <sub>6</sub> | Y <sub>4</sub> |
| 0              | 0              | 0              | 1              | 1              | 1              | X <sub>7</sub> | Y <sub>0</sub> | 1              | 0              | 0              | 1              | 1              | 1              | X <sub>7</sub> | Y <sub>4</sub> |
| 0              | 0              | 1              | 0              | 0              | 0              | X <sub>0</sub> | Y <sub>1</sub> | 1              | 0              | 1              | 0              | 0              | 0              | X <sub>0</sub> | Y <sub>5</sub> |
| 0              | 0              | 1              | 0              | 0              | 1              | X <sub>1</sub> | Y <sub>1</sub> | 1              | 0              | 1              | 0              | 0              | 1              | X <sub>1</sub> | Y <sub>5</sub> |
| 0              | 0              | 1              | 0              | 1              | 0              | X <sub>2</sub> | Y <sub>1</sub> | 1              | 0              | 1              | 0              | 0              | 1              | X <sub>2</sub> | Y <sub>5</sub> |
| 0              | 0              | 1              | 0              | 1              | 1              | X <sub>3</sub> | Y <sub>1</sub> | 1              | 0              | 1              | 0              | 1              | 0              | X <sub>3</sub> | Y <sub>5</sub> |
| 0              | 0              | 1              | 1              | 0              | 0              | X <sub>4</sub> | Y <sub>1</sub> | 1              | 0              | 1              | 1              | 0              | 0              | X <sub>4</sub> | Y <sub>5</sub> |
| 0              | 0              | 1              | 1              | 0              | 1              | X <sub>5</sub> | Y <sub>1</sub> | 1              | 0              | 1              | 1              | 0              | 1              | X <sub>5</sub> | Y <sub>5</sub> |
| 0              | 0              | 1              | 1              | 1              | 0              | X <sub>6</sub> | Y <sub>1</sub> | 1              | 0              | 1              | 1              | 1              | 0              | X <sub>6</sub> | Y <sub>5</sub> |
| 0              | 0              | 1              | 1              | 1              | 1              | X <sub>7</sub> | Y <sub>1</sub> | 1              | 0              | 1              | 1              | 1              | 1              | X <sub>7</sub> | Y <sub>5</sub> |
| 0              | 1              | 0              | 0              | 0              | 0              | X <sub>0</sub> | Y <sub>2</sub> | 1              | 1              | 0              | 0              | 0              | 0              | X <sub>0</sub> | Y <sub>6</sub> |
| 0              | 1              | 0              | 0              | 0              | 1              | X <sub>1</sub> | Y <sub>2</sub> | 1              | 1              | 0              | 0              | 0              | 1              | X <sub>1</sub> | Y <sub>6</sub> |
| 0              | 1              | 0              | 0              | 1              | 0              | X <sub>2</sub> | Y <sub>2</sub> | 1              | 1              | 0              | 0              | 1              | 0              | X <sub>2</sub> | Y <sub>6</sub> |
| 0              | 1              | 0              | 0              | 1              | 1              | X <sub>3</sub> | Y <sub>2</sub> | 1              | 1              | 0              | 0              | 1              | 1              | X <sub>3</sub> | Y <sub>6</sub> |
| 0              | 1              | 0              | 1              | 0              | 0              | X <sub>4</sub> | Y <sub>2</sub> | 1              | 1              | 0              | 1              | 0              | 0              | X <sub>4</sub> | Y <sub>6</sub> |
| 0              | 1              | 0              | 1              | 0              | 1              | X <sub>5</sub> | Y <sub>2</sub> | 1              | 1              | 0              | 1              | 0              | 1              | X <sub>5</sub> | Y <sub>6</sub> |
| 0              | 1              | 0              | 1              | 1              | 0              | X <sub>6</sub> | Y <sub>2</sub> | 1              | 1              | 0              | 1              | 1              | 0              | X <sub>6</sub> | Y <sub>6</sub> |
| 0              | 1              | 0              | 1              | 1              | 1              | X <sub>7</sub> | Y <sub>2</sub> | 1              | 1              | 0              | 1              | 1              | 1              | X <sub>7</sub> | Y <sub>6</sub> |
| 0              | 1              | 1              | 0              | 0              | 0              | X <sub>0</sub> | Y <sub>3</sub> | 1              | 1              | 1              | 0              | 0              | 0              | X <sub>0</sub> | Y <sub>7</sub> |
| 0              | 1              | 1              | 0              | 0              | 1              | X <sub>1</sub> | Y <sub>3</sub> | 1              | 1              | 1              | 0              | 0              | 1              | X <sub>1</sub> | Y <sub>7</sub> |
| 0              | 1              | 1              | 0              | 1              | 0              | X <sub>2</sub> | Y <sub>3</sub> | 1              | 1              | 1              | 0              | 0              | 1              | X <sub>2</sub> | Y <sub>7</sub> |
| 0              | 1              | 1              | 0              | 1              | 1              | X <sub>3</sub> | Y <sub>3</sub> | 1              | 1              | 1              | 0              | 1              | 0              | X <sub>3</sub> | Y <sub>7</sub> |
| 0              | 1              | 1              | 1              | 0              | 0              | X <sub>4</sub> | Y <sub>3</sub> | 1              | 1              | 1              | 1              | 0              | 0              | X <sub>4</sub> | Y <sub>7</sub> |
| 0              | 1              | 1              | 1              | 0              | 1              | X <sub>5</sub> | Y <sub>3</sub> | 1              | 1              | 1              | 1              | 0              | 1              | X <sub>5</sub> | Y <sub>7</sub> |
| 0              | 1              | 1              | 1              | 1              | 0              | X <sub>6</sub> | Y <sub>3</sub> | 1              | 1              | 1              | 1              | 1              | 0              | X <sub>6</sub> | Y <sub>7</sub> |
| 0              | 1              | 1              | 1              | 1              | 1              | X <sub>7</sub> | Y <sub>3</sub> | 1              | 1              | 1              | 1              | 1              | 1              | X <sub>7</sub> | Y <sub>7</sub> |

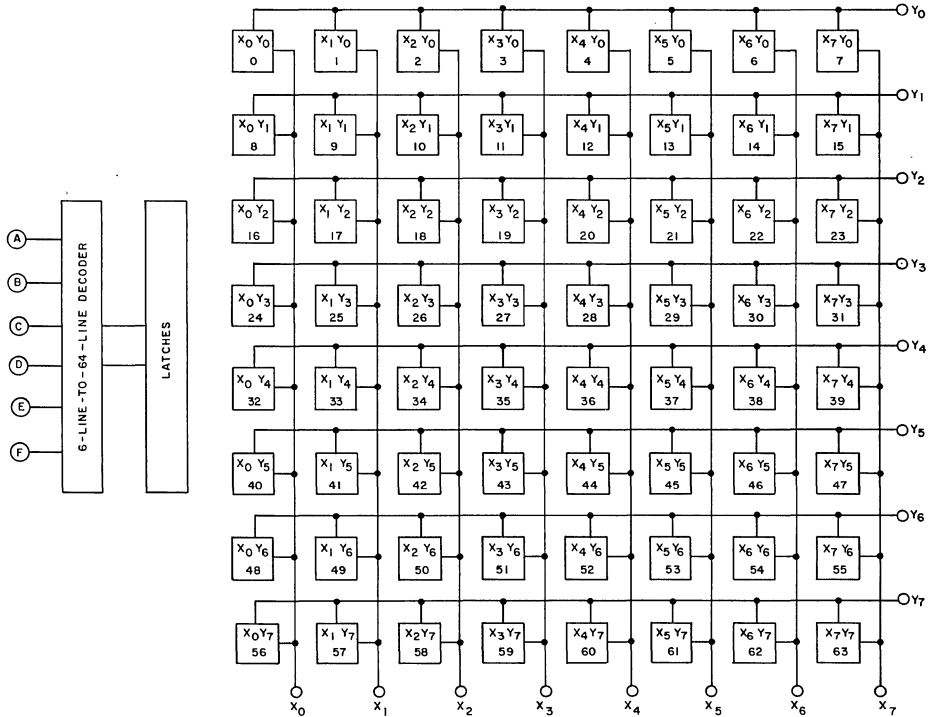


FIGURE 5. FUNCTIONAL DIAGRAM

Test Circuits and Waveforms

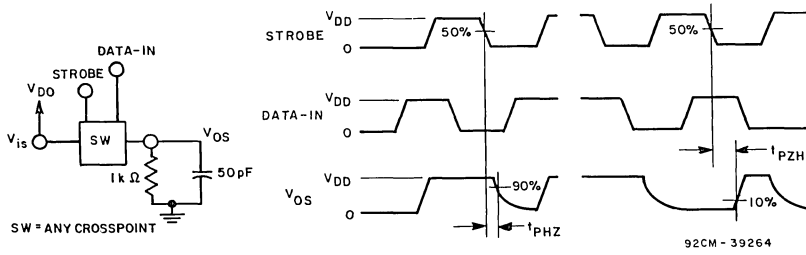


FIGURE 6. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (STROBE TO SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-OFF)

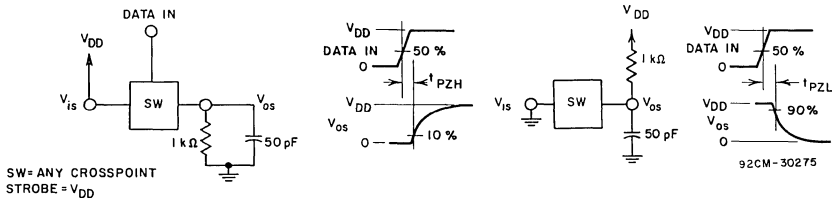


FIGURE 7. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (DATA-IN TO SIGNAL OUTPUT, SWITCH TURN-ON TO HIGH OR LOW LEVEL)

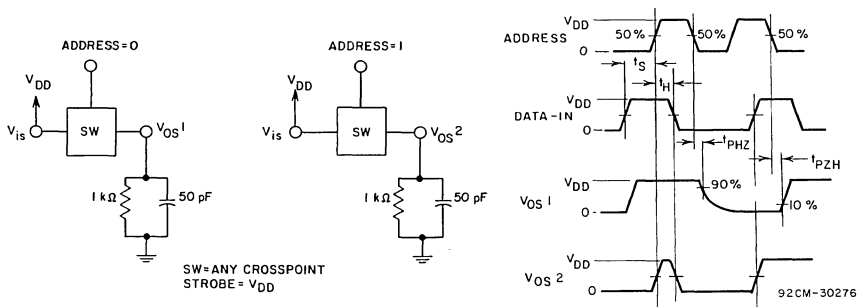


FIGURE 8. PROPAGATION DELAY TIME TEST CIRCUIT AND WAVEFORMS (ADDRESS SIGNAL OUTPUT, SWITCH TURN-ON OR TURN-OFF)

CD74HC22106, CD74HCT22106

Test Circuits and Waveforms (Continued)

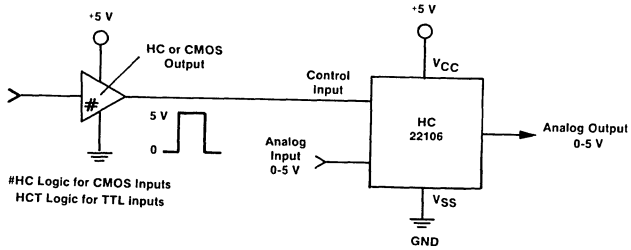


FIGURE 9. TYPICAL SINGLE-SUPPLY CONNECTION FOR HC22106

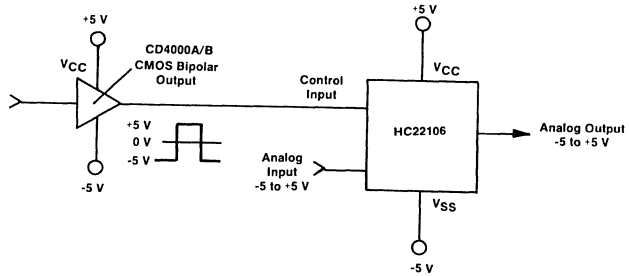


FIGURE 10. TYPICAL DUAL-SUPPLY CONNECTION FOR HC22106

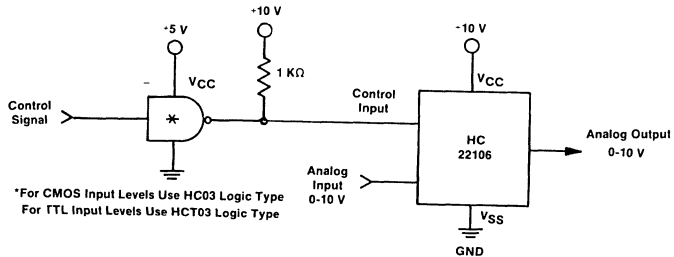


FIGURE 11. USE OF HC/HCT03 WHEN CONTROL SIGNAL IS 0V - 5V AND ANALOG SIGNAL IS 0V - 10V

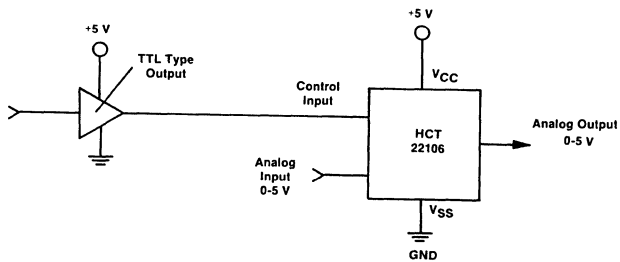


FIGURE 12. TYPICAL SINGLE-SUPPLY CONNECTION FOR HCT22106 WITH TTL INPUT

August 1991

### Features

- Monolithic Integrated Device
- DI High Voltage Process
- Compatible With Worldwide PBX Performance Requirements
- Controlled Supply of Battery Feed Current for Short Loops (30mA)
- Internal Ring Relay Driver
- Low Power Consumption During Standby
- Switch Hook, Ground Key and Ring Trip Detection Functions
- Selective Denial of Power to Subscriber Loops

### Applications

- Solid State Line Interface Circuit for Analog and Digital PBX Systems
- Direct Inward Dial (DID) Trunks
- Voice Messaging PBX's

### Description

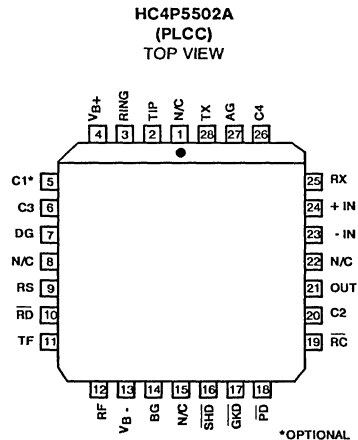
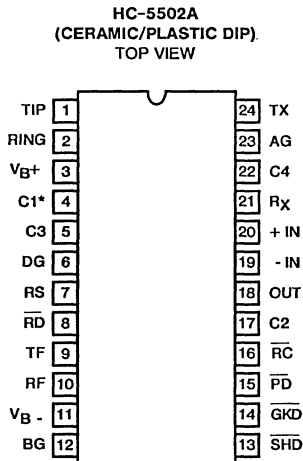
The Harris SLIC incorporates many of the BORSHT function on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents. Using the unique Harris dielectric isolation process, the SLIC can operate directly with a wide range of station battery voltages.

The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

The Harris SLIC is ideally suited for the design of new digital PBX systems, by eliminating bulky hybrid transformers.

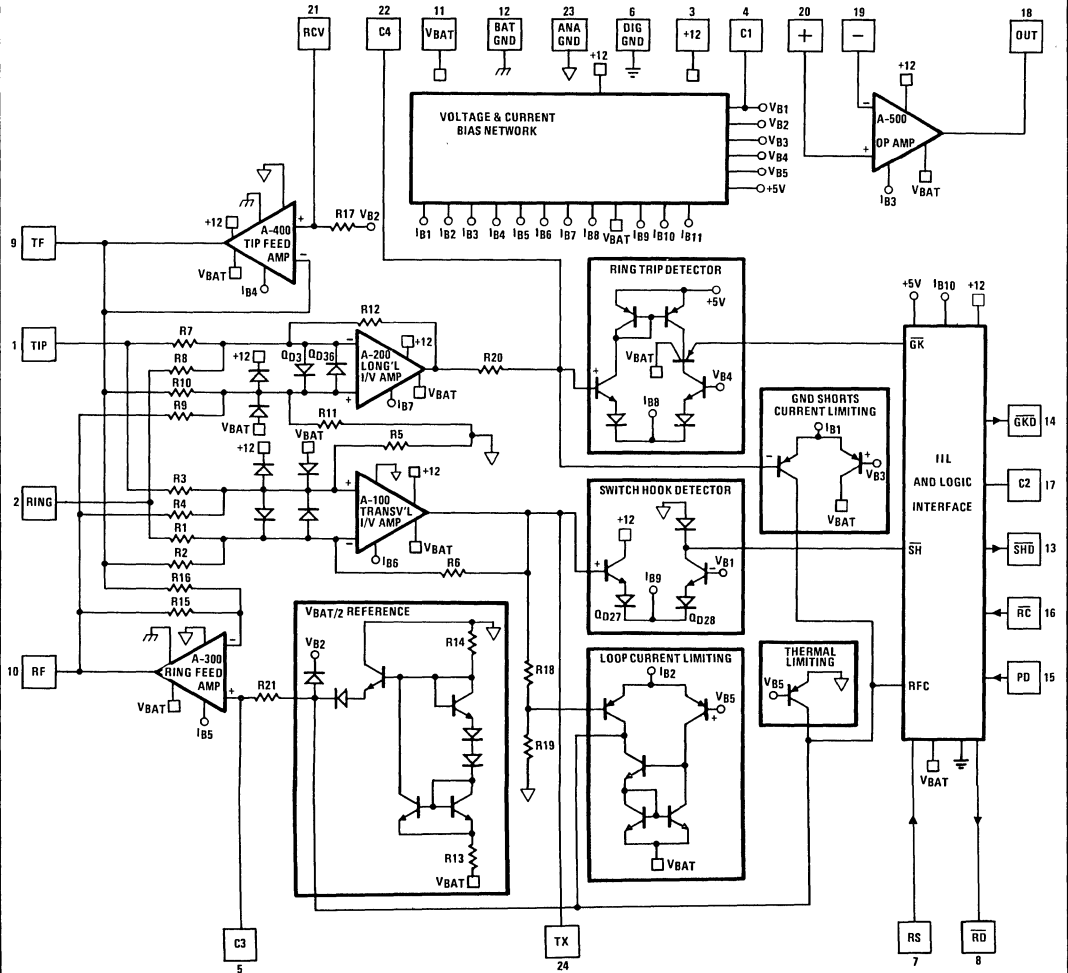
SLIC is available in either a 24 pin Dual-in-Line Plastic or Ceramic package, and a 28 pin PLCC package.

### Pinouts



# HC-5502A

## Schematic



HC-5502A SLIC FUNCTIONAL SCHEMATIC.

### Die Characteristics

|                           |               |               |
|---------------------------|---------------|---------------|
| Transistor Count .....    | 181           |               |
| Diode Count .....         | 27            |               |
| Die Dimensions .....      | 169 x 112     |               |
| Substrate Potential ..... | Unconnected   |               |
| Process .....             | Bipolar-DI    |               |
| Thermal Constants (°C/W)  | $\theta_{ja}$ | $\theta_{jc}$ |
| Ceramic DIP               | 51            | 16            |
| Plastic DIP               | 52            | 24            |

## Specifications HC-5502A

### Absolute Maximum Ratings (Note 1)

|  |  |
|--|--|
| Maximum Continuous Supply Voltages     | (V <sub>B-</sub> ) . . . . . -60 to +0.5 V         |
|  | (V <sub>B+</sub> ) . . . . . -0.5 to +15 V         |
|  | (V <sub>B+</sub> - V <sub>B-</sub> ) . . . . . 75V |
| Relay Drive Voltage (V <sub>RD</sub> ) | . . . . . -0.5 to +15V                             |
| Storage Temperature Range              | . . . . . -65°C to +150°C                          |
| Junction Temperature                   | . . . . . +175°C                                   |

### Recommended Operating Conditions

|  |                            |
|--|----------------------------|
| Relay Driver Voltage (V <sub>RD</sub> )    | . . . . . +5 to +12V       |
| Positive Supply Voltage (V <sub>B+</sub> ) | . . . . . 10.8 to 13.2V    |
| Negative Supply Voltage (V <sub>B-</sub> ) | . . . . . -42 to -58V      |
| Minimum High Level Logic Input Voltage     | . . . . . 2.4V             |
| Maximum Low Level Logic Input Voltage      | . . . . . 0.6V             |
| Loop Resistance (R <sub>L</sub> )          | . . . . . 200 to 1200 Ohms |
| Operating Temperature Range                |                            |
| HC-5502A-5,-7                              | . . . . . 0°C to +75°C     |
| HC-5502A-9                                 | . . . . . -40°C to +85°C   |

**Electrical Specifications** V<sub>B-</sub> = -48V, V<sub>B+</sub> = +12V, AG = BG = DG = 0V, Unless Otherwise Noted,  
 Typical Parameters +25°C. Min-Max Parameters are Over Operating Temperature Range.

| PARAMETER                          | CONDITIONS  | MIN  | TYP  | MAX  | UNITS       |
|------------------------------------|---|------|------|------|-------------|
| On Hook Power Dissipation          | I <sub>Long</sub> = 0   | -    | 135  | 174  | mW          |
| Off Hook Power Dissipation         | R <sub>LINE</sub> = 600 Ohms, I <sub>Long</sub> = 0   | -    | 450  | 580  | mW          |
| Off Hook IB+                       | R <sub>LINE</sub> = 600 Ohms, I <sub>Long</sub> = 0 @ -40°C   | -    | -    | 5.0  | mA          |
| Off Hook IB+                       | R <sub>LINE</sub> = 600 Ohms, I <sub>Long</sub> = 0 @ +25°C   | -    | -    | 4.3  | mA          |
| Off Hook IB-                       | R <sub>LINE</sub> = 600 Ohms, I <sub>Long</sub> = 0   | -    | -    | 38   | mA          |
| Off Hook Loop Current              | R <sub>LINE</sub> = 1200 Ohms, I <sub>Long</sub> = 0  | -    | 21   | -    | mA          |
| Off Hook Loop Current              | R <sub>LINE</sub> = 1200 Ohms, V <sub>B-</sub> = -42V, I <sub>Long</sub> = 0<br>T <sub>A</sub> = 25°C | 17.5 | -    | -    | mA          |
| Off Hook Loop Current              | R <sub>LINE</sub> = 200 Ohms, I <sub>Long</sub> = 0   | 25.5 | 30   | 34.5 | mA          |
| Fault Currents                     |   |      |      |      |             |
| TIP to Ground                      |   | -    | 14   | -    | mA          |
| RING to Ground                     |   | -    | 47   | -    | mA          |
| TIP to RING                        |   | -    | 30   | -    | mA          |
| TIP and RING to Ground             |   | -    | 47   | -    | mA          |
| Ring Relay Drive V <sub>OL</sub>   | I <sub>OL</sub> = 62mA  | -    | 0.2  | 0.5  | V           |
| Ring Relay Driver Off Leakage      | V <sub>RD</sub> = +12V, RC = 1 = HIGH, T <sub>A</sub> = 25°C  | -    | -    | 100  | μA          |
| Ring Rrip Detection Period         | R <sub>LINE</sub> = 600 Ohms, T <sub>A</sub> = +25°C  | -    | 2    | 3    | Ring Cycles |
| Switch Hook Detection Threshold    | SHD = V <sub>OL</sub>   | 10   | -    | -    | mA          |
|                                    | SHD = V <sub>OH</sub>   | -    | -    | 5    | mA          |
| Ground Key Detection Threshold     | GKD = V <sub>OL</sub>   | 20   | -    | -    | mA          |
|                                    | GKD = V <sub>OH</sub>   | -    | -    | 10   | -           |
| Loop Current During Power Denial   |   | -    | ±2   | -    | mA          |
| Dial Pulse Distortion              |   | 0    | -    | 5    | ms          |
| Receive Input Impedance            |   | -    | 90   | -    | kOhms       |
| Transmit Output Impedance          |   | -    | 5    | 20   | Ohms        |
| Two Wire Return Loss               | (Return Loss Referenced to 600Ω +2.16μF)  |      |      |      |             |
| SRL LO                             |   | -    | 15.5 | -    | dB          |
| ERL                                |   | -    | 24   | -    | dB          |
| SRL HI                             |   | -    | 31   | -    | dB          |
| Longitudinal Balance               | 1V Peak-Peak 200Hz - 3400Hz<br>0°C ≤ T <sub>A</sub> ≤ 75°C  |      |      |      |             |
| 2 Wire Off Hook                    |   | 58   | 65   | -    | dB          |
| 2Wire On Hook                      |   | 60   | 63   | -    | dB          |
| 4 Wire Off Hook                    |   | 50   | 58   | -    | dB          |
| Low Frequency Longitudinal Balance | R.E.A. Method, 0°C ≤ T <sub>A</sub> ≤ 75°C  | -    | -    | 23   | dBmC        |
|                                    |   | -    | -    | -67  | dBmOp       |

NOTES: 1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

## Specifications HC-5502A

### Electrical Specifications (Continued)

| PARAMETERS                       | CONDITIONS   | MIN  | TYP   | MAX   | UNITS |
|----------------------------------|--|------|-------|-------|-------|
| Insertion Loss                   | @1kHz, OdBm Input Level  | -    | ±0.05 | ±0.2  | dB    |
| 2 Wire - 4 Wire                  |  | -    | ±0.05 | ±0.2  | dB    |
| 4 Wire - 2 Wire                  |  | -    | ±0.05 | ±0.2  | dB    |
| Frequency Response               | 200 - 3400Hz Referenced to Absolute Loss at 1kHz and OdBm Signal Level | -    | ±0.02 | ±0.05 | dB    |
| Idle Channel Noise               | $0^{\circ}\text{C} \leq T_A \leq 75^{\circ}\text{C}$                   | -    | -     | -     | -     |
| 2 Wire - 4 Wire                  | $0^{\circ}\text{C} \leq T_A \leq 75^{\circ}\text{C}$                   | -    | 1     | 5     | dBmC  |
| 4 Wire - 2 Wire                  |  | -    | -89   | -85   | dBmOp |
| Absolute Delay                   | $0^{\circ}\text{C} \leq T_A \leq 75^{\circ}\text{C}$                   | -    | -     | -     | -     |
| 2 Wire - 4 Wire                  |  | -    | -     | 2     | µs    |
| 4 Wire - 2 Wire                  |  | -    | -     | 2     | µs    |
| Trans Hybrid Loss                | Balance Network Set Up for 600 Ohm Termination at 1kHz                 | 36   | 40    | -     | dB    |
| Overload Level                   | $0^{\circ}\text{C} \leq T_A \leq 75^{\circ}\text{C}$                   | -    | -     | -     | -     |
| 2 Wire - 4 Wire                  |  | 1.75 | -     | -     | Vpeak |
| 4 Wire - 2 Wire                  |  | 1.75 | -     | -     | Vpeak |
| Level Linearity                  | at 1kHz, $0^{\circ}\text{C} \leq T_A \leq 75^{\circ}\text{C}$          | -    | -     | -     | -     |
| 2 Wire - 4 Wire                  | +3 to -40dBm   | -    | -     | ±0.05 | dB    |
|                                  | -40 to -50dBm  | -    | -     | ±0.1  | dB    |
|                                  | -50 to -55dBm  | -    | -     | ±0.3  | dB    |
| 4 Wire - 2 Wire                  | +3 to -40dBm   | -    | -     | ±0.05 | dB    |
|                                  | -40 to -50dBm  | -    | -     | ±0.1  | dB    |
|                                  | -50 to -55dBm  | -    | -     | ±0.3  | dB    |
| Power Supply Rejection Ratio     | $0^{\circ}\text{C} \leq T_A \leq 75^{\circ}\text{C}$                   | -    | -     | -     | -     |
| V <sub>B+</sub> to 2 Wire        | 30 - 60Hz, R <sub>LINE</sub> = 600Ω                                    | 15   | -     | -     | dB    |
| V <sub>B+</sub> to Transmit      |  | 15   | -     | -     | dB    |
| V <sub>B-</sub> to 2 Wire        |  | 15   | -     | -     | dB    |
| V <sub>B-</sub> to Transmit      |  | 15   | -     | -     | dB    |
| V <sub>B+</sub> to 2 Wire        | 200 - 16kHz  | 30   | -     | -     | dB    |
| V <sub>B+</sub> to Transmit      | R <sub>LINE</sub> = 600Ω   | 30   | -     | -     | dB    |
| V <sub>B-</sub> to 2 Wire        |  | 30   | -     | -     | dB    |
| V <sub>B-</sub> to Transmit      |  | 30   | -     | -     | dB    |
| Logic Input Current (RS, RC, PD) | $0\text{V} \leq V_{IN} \leq 5\text{V}$                                 | -    | -     | ±100  | µA    |
| Logic Inputs                     |  | -    | -     | -     | -     |
| Logic '0' V <sub>I1</sub>        |  | -    | -     | 0.8   | Volts |
| Logic '1' V <sub>I1</sub>        |  | 2.0  | -     | 5.5   | Volts |
| Logic Outputs                    |  | -    | -     | -     | -     |
| Logic '0' V <sub>OL</sub>        | I <sub>LOAD</sub> 800µA  | -    | 0.1   | 0.5   | Volts |
| Logic '1' V <sub>OH</sub>        | I <sub>LOAD</sub> 80µA   | 2.7  | 5.0   | 5.5   | Volts |

### Uncommitted Op Amp Specifications

| PARAMETER                     | CONDITIONS           | MIN | TYP | MAX | UNITS |
|-------------------------------|----------------------|-----|-----|-----|-------|
| Input Offset Voltage          |                      | -   | ±5  | -   | mV    |
| Input Offset Current          |                      | -   | ±10 | -   | nA    |
| Input Bias Current            |                      | -   | 20  | -   | nA    |
| Differential Input Resistance |                      | -   | 1   | -   | MΩ    |
| Output Voltage Swing          | R <sub>L</sub> = 10K | -   | ±5  | -   | Vpeak |
| Output Resistance             | A <sub>VCL</sub> = 1 | -   | 10  | -   | Ω     |
| Small Signal GBW              |                      | -   | 1   | -   | MHz   |

## Pin Assignments HC-5502A

| 28 PIN PLCC | 24 PIN DIP | SYMBOL          | DESCRIPTION  |
|-------------|------------|-----------------|--|
| 2           | 1          | TIP             | An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω feed resistor and a ring relay. Functions with the Ring terminal to receive voice signals from the telephone and for Loop Monitoring Purposes.   |
| 3           | 2          | RING            | An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.  |
| 4           | 3          | V <sub>B+</sub> | Positive Voltage Source - Most positive supply. V <sub>B+</sub> is typically 12 volts with an operational range of 10.8 to 13.2 volts.   |
| 5           | 4          | C1              | Capacitor #1 - Optional Capacitor used to improve power supply rejection. This pin should be left open if unused.  |
| 6           | 5          | C3              | Capacitor #3 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering V <sub>B-</sub> supply. Typical value is 0.3μF, 30V.  |
| 7           | 6          | DG              | Digital Ground - To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC.   |
| 9           | 7          | RS              | Ring Synchronization Input - A TTL - compatible clock input. The clock is arranged such that a positive transition occurs on the negative going zero crossing of the ring voltage source, ensuring that the ring relay is activated and deactivated when the instantaneous ring voltage is near zero. If synchronization is not required, tie to +5V.  |
| 10          | 8          | RD              | Relay Driver - A low active open collector logic output. When enabled, the external ring relay is energized.   |
| 11          | 9          | TF              | Tip Feed - A low impedance analog output connected to the TIP terminal through a 150Ω feed resistor. Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.   |
| 12          | 10         | RF              | Ring Feed - A low impedance analog output connected to the RING terminal through a 150Ω feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal currents.  |
| 13          | 11         | V <sub>B-</sub> | Negative Voltage Source - Most negative supply. V <sub>B-</sub> is typically -48 volts with an operational range of -42 to -58 volts. Frequently referred to as "battery".   |
| 14          | 12         | BG              | Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.   |
| 16          | 13         | SHD             | Switch Hook Detection - A low active LS TTL - compatible logic output. This output is enabled for loop currents exceeding 10mA and disabled for loop currents less than 5mA.   |
| 17          | 14         | GKD             | Ground Key Detection - A low active LS TTL - compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 20mA, and disabled if this current difference is less than 10mA.   |
| 18          | 15         | PD              | Power Denial - A low active TTL - Compatible logic input. When enabled the switch hook detect (SHD) and ground key detect (GKD) are not necessarily valid, and the relay driver, (RD) output is disabled.  |
| 19          | 16         | RC              | Ring Command - A low active TTL - Compatible logic input. When enabled, the relay driver (RD) output goes low on the next rising edge of the ring sync (RS) input, as long as the SLIC is not in the power denial state (PD = 0) or the subscriber is not already off-hook (SHD = 0).  |
| 20          | 17         | C2              | Capacitor #2 - An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is 0.15μF, 10V. This capacitor is not used if ground key function is not required.   |
| 21          | 18         | OUT             | The analog output of the spare operational amplifier.  |
| 23          | 19         | -IN             | The inverting analog input of the spare operational amplifier.   |
| 24          | 20         | +IN             | The non-inverting analog input of the spare operational amplifier.   |
| 25          | 21         | RX              | Receive Input, Four Wire Side - A high impedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip feed and Ring feed amplifiers, which in turn drive tip and ring through 300 Ohms of feed resistance on each side of the line.   |
| 26          | 22         | C4              | Capacitor #4 - An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from near proximity power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5μF, to 1.0μF, 20V. This capacitor should be nonpolarized. |
| 27          | 23         | AG              | Analog Ground - To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.   |
| 28          | 24         | TX              | Transmit Output, Four Wire Side - A low impedance analog output which represents the differential voltage across Tip and Ring. Transhybrid balancing must be preformed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.                 |
| 1,8,15,22   |            | NC              | No Internal Connection.  |

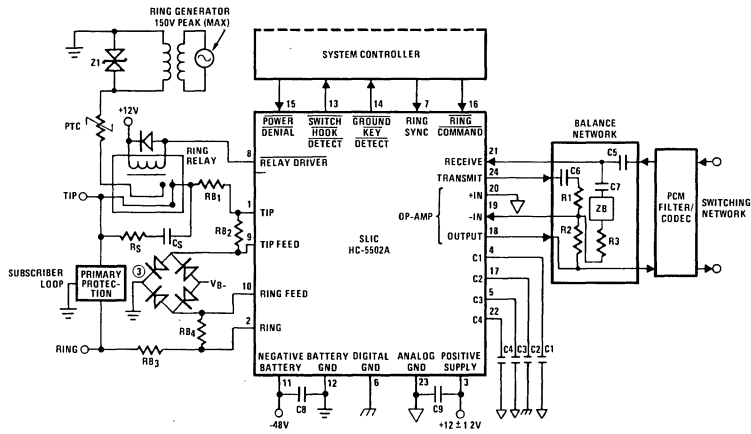
NOTE: All grounds (AG, BG, & DG) must be applied before VB+ or VB-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.



# HC-5502A

## Applications Diagram

### TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC



#### TYPICAL COMPONENT VALUES

- C1** = 0.5 $\mu$ F (Note 1) **C5** = 0.5 $\mu$ F, 20V  
**C2** = 0.15 $\mu$ F, 10V **C6** = **C7** = 0.5 $\mu$ F (10% Match Required) (Note 2), 20V  
**C3** = 0.3 $\mu$ F, 30V **C8** = 0.01 $\mu$ F, 100V  
**C4** = 0.5 $\mu$ V to 1.0 $\mu$ F,  $\pm$ 10%, 20V (Should be nonpolarized) **C9** = 0.01 $\mu$ F, 20V,  $\pm$ 20%

- R1**  $\rightarrow$  **R3** = 100k $\Omega$  (0.1% Match Required, 1% absolute value), **ZB** = 0 for 600 $\Omega$  Terminations (Note 2)  
**RB1** = **RB2** = **RB3** = **RB4** = 150 $\Omega$  (0.1% Match Required, 1% absolute value)  
**RS** = 1k $\Omega$ , **CS** = 0.1 $\mu$ F, 200V typically, depending on  $V_{Ring}$  and line length.  
**Z1** = 150V to 200V transient protector. PTC used as ring ballast.

**NOTE 1:** C1 is an optional capacitor used to improve +12V supply rejection. This pin must be left open if unused.

**NOTE 2:** To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C6-R1 and R2 and C7-ZB-R3, to match in impedance to within 0.3%. Thus, if C6 and C7 and 1 $\mu$ F each, a 20% match is adequate. It should be noted that the transmit output to C6 sees a -10.5 to -21 volt step when the loop is closed and that too large a value for C6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC.

A 0.5 $\mu$ F and 100k $\Omega$  gives a time constant of 50msec. The uncommitted op amp output is internally clamped to stay within  $\pm$ 5.5V and also has current limiting protection.

**NOTE 3:** Secondary protection diode bridge recommended is MDA 220 or equivalent.

ADDITIONAL INFORMATION IS CONTAINED IN APPLICATION NOTE 549, "THE HC-550X TELEPHONE SLICs"  
BY GEOFF PHILLIPS

## Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum of 30mA RMS, 15mA RMA per leg, without any performance degradation.

TABLE 1

| PARAMETER          | TEST CONDITION     | PERFORMANCE (MAX)    | UNITS  |
|--------------------|--------------------|----------------------|--------|
| Longitudinal Surge | 10 $\mu$ s Rise/   | $\pm$ 1000 (Plastic) | V Peak |
|                    | 1000 $\mu$ s/Fall  | $\pm$ 500 (Ceramic)  | V Peak |
| Metallic Surge     | 10 $\mu$ s Rise/   | $\pm$ 1000 (Plastic) | V Peak |
|                    | 1000 $\mu$ Fall    | $\pm$ 500 (Ceramic)  | V Peak |
| T/GND              | 10 $\mu$ s Rise/   | $\pm$ 1000 (Plastic) | V Peak |
| R/GND              | 1000 $\mu$ s Fall  | $\pm$ 500 (Ceramic)  | V Peak |
| 50/60Hz Current    |                    |                      |        |
| T/GND              | 700V rms           | 11                   | Cycles |
| R/GND              | Limited to 10A rms |                      |        |

August 1991

#### Features

- Pin For Pin Replacement For The HC-5502A
- Capable of +12V or +5V (VB+) Operation
- Monolithic Integrated Device
- DI High Voltage Process
- Compatible With Worldwide PBX Performance Requirements
- Controlled Supply of Battery Feed Current for Short Loops (30mA)
- Internal Ring Relay Driver
- Low Power Consumption During Standby
- Switch Hook, Ground Key and Ring Trip Detection Functions
- Selective Denial of Power to Subscriber Loops

#### Applications

- Solid State Line Interface Circuit for Analog and Digital PBX Systems
- Direct Inward Dial (DID) Trunks
- Voice Messaging PBX's

#### Description

The Harris SLIC incorporates many of the BORSHT function on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents. Using the unique Harris dielectric isolation process, the SLIC can operate directly with a wide range of station battery voltages.

The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

The Harris SLIC is ideally suited for the design of new digital PBX systems, by eliminating bulky hybrid transformers.

The SLIC is available in either a 24 pin Dual-in-Line Plastic or Ceramic package, a 28 pin PLCC package and a 24 pin SOIC package.

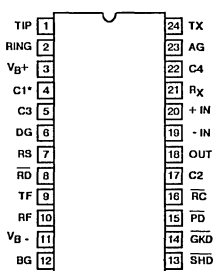
#### Pinouts

HC1-5502B (24 PIN CERAMIC DIP)

HC3-5502B (24 PIN PLASTIC DIP)

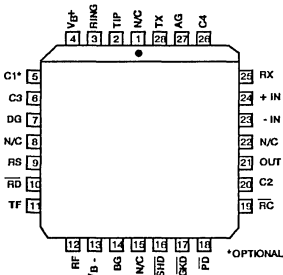
HC9P5502B (SOIC)

TOP VIEW

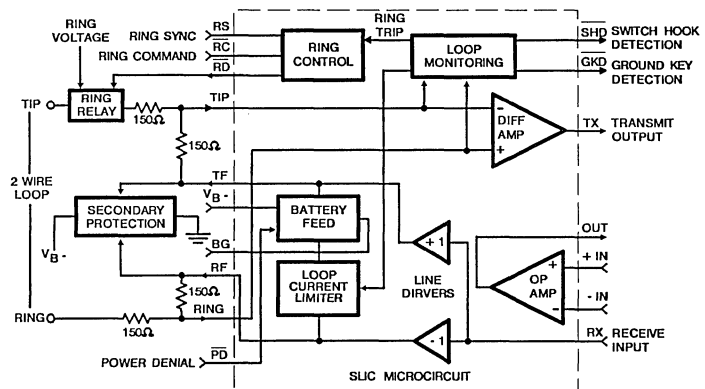


HC4P5502B (PLCC)

TOP VIEW

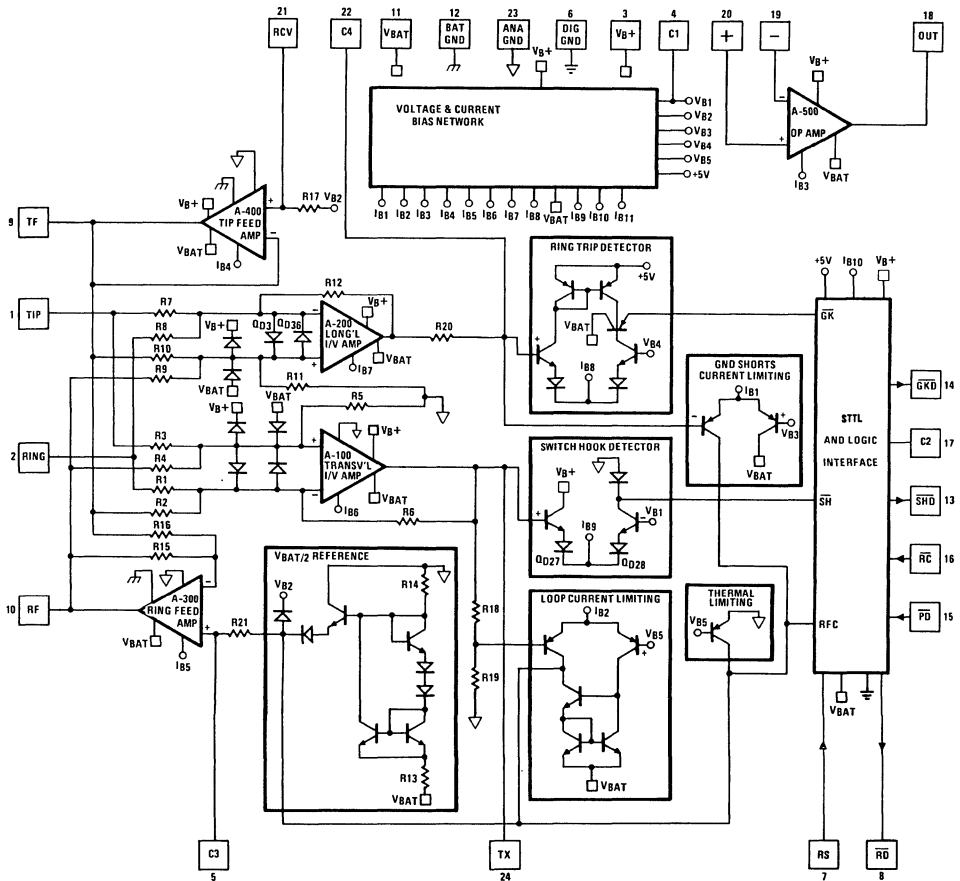


#### Functional Diagram



# HC-5502B

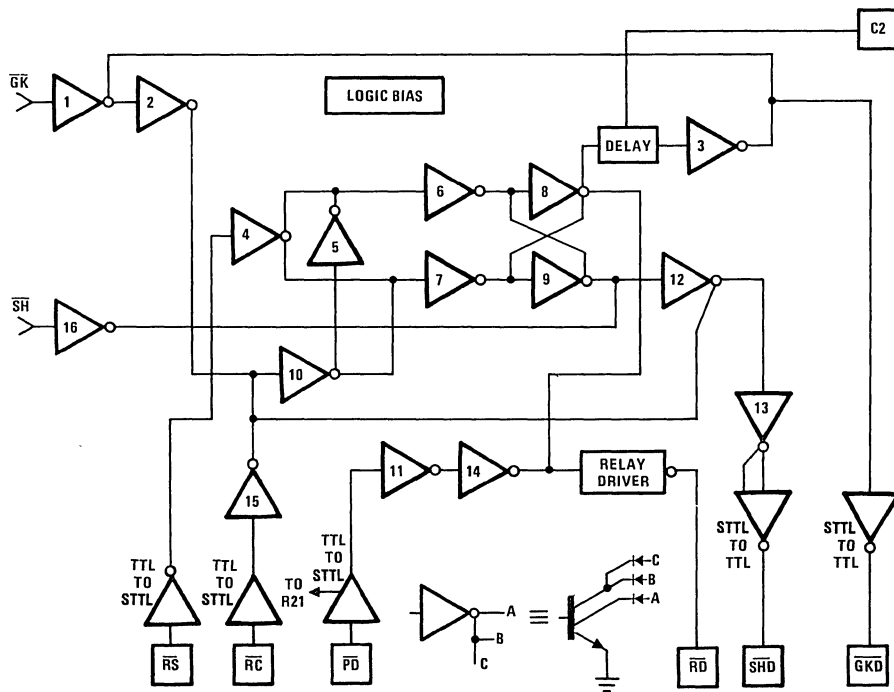
## Schematic



HC-5502B SLIC FUNCTIONAL SCHEMATIC.

# HC-5502B

## Schematic



HC-5502B LOGIC GATE SCHEMATIC

## Die Characteristics

|                           |                |               |
|---------------------------|----------------|---------------|
| Transistor Count .....    | 183            |               |
| Diode Count .....         | 33             |               |
| Die Dimensions .....      | 137 x 102 mils |               |
| Substrate Potential ..... | Connected      |               |
| Process .....             | Bipolar-DI     |               |
| Thermal Constants (°C/W)  | $\theta_{ja}$  | $\theta_{jc}$ |
| Ceramic DIP               | 52             | 15            |
| Plastic DIP               | 52             | 22            |
| PLCC                      | 67             | 29            |
| SOIC                      | 76             | 24            |

## Specifications HC-5502B

### Absolute Maximum Ratings (Note 1)

|  |   |
|--|---|
| Maximum Continuous Supply Voltages     | (V <sub>B-</sub> ) . . . . . -60 to +0.5 V          |
|  | (V <sub>B+</sub> ) . . . . . -0.5 to +15 V          |
|  | (V <sub>B+</sub> - V <sub>B-</sub> ) . . . . . +75V |
| Relay Drive Voltage (V <sub>RD</sub> ) | . . . . . -0.5 to +15V                              |
| Storage Temperature Range              | . . . . . -65°C to +150°C                           |
| Junction Temperature Ceramic           | . . . . . +175°C                                    |
| Junction Temperature Plastic           | . . . . . +150°C                                    |

### Recommended Operating Conditions

|  |  |
|--|--|
| Relay Driver Voltage (V <sub>RD</sub> )    | . . . . . +5 to +12V                     |
| Positive Supply Voltage (V <sub>B+</sub> ) | . . . . . 4.75 to 5.25V or 10.8 to 13.2V |
| Negative Supply Voltage (V <sub>B-</sub> ) | . . . . . -42 to -58V                    |
| High Level Logic Input Voltage             | . . . . . 2.4V                           |
| Low Level Logic Input Voltage              | . . . . . 0.6V                           |
| Loop Resistance (R <sub>L</sub> )          | . . . . . 200 to 1200 Ohms               |
| Operating Temperature Range                |  |
| HC-5502B-5                                 | . . . . . 0°C to +75°C                   |
| HC-5502B-9                                 | . . . . . -40°C to +85°C                 |

**Electrical Specifications** Unless Otherwise Specified, V<sub>B-</sub> = -48V, V<sub>B+</sub> = +12V and +5V, AG = BG = DG = 0V, Typical Parameters T<sub>A</sub> = +25°C. Min-Max Parameters are Over Operating Temperature Range.

| PARAMETER                          | CONDITIONS  | MIN  | TYP  | MAX  | UNITS       |
|------------------------------------|---|------|------|------|-------------|
| On Hook Power Dissipation          | I <sub>Long</sub> * = 0, V <sub>B+</sub> = +12V   | -    | 135  | 235  | mW          |
| Off Hook Power Dissipation         | R <sub>L</sub> = 600 Ohms, I <sub>Long</sub> * = 0, V <sub>B+</sub> = +12V                            | -    | 450  | 690  | mW          |
| Off Hook IB+                       | R <sub>L</sub> = 600 Ohms, I <sub>Long</sub> * = 0 T <sub>A</sub> = -40°C                             | -    | -    | 6.0  | mA          |
| Off Hook IB+                       | R <sub>L</sub> = 600 Ohms, I <sub>Long</sub> * = 0 T <sub>A</sub> = +25°C                             | -    | -    | 5.3  | mA          |
| Off Hook IB-                       | R <sub>L</sub> = 600 Ohms, I <sub>Long</sub> * = 0  | -    | -    | 39   | mA          |
| Off Hook Loop Current              | R <sub>L</sub> = 1200 Ohms, I <sub>Long</sub> * = 0   | -    | 21   | -    | mA          |
| Off Hook Loop Current              | R <sub>L</sub> = 1200 Ohms, V <sub>B-</sub> = -42V, I <sub>Long</sub> * = 0<br>T <sub>A</sub> = +25°C | 17.5 | -    | -    | mA          |
| Off Hook Loop Current              | R <sub>L</sub> = 200 Ohms, I <sub>Long</sub> * = 0  | 25.5 | 30   | 34.5 | mA          |
| Fault Currents                     |   |      |      |      |             |
| TIP to Ground                      |   | -    | 14   | -    | mA          |
| RING to Ground                     |   | -    | 47   | -    | mA          |
| TIP to RING                        |   | -    | 30   | -    | mA          |
| TIP and RING to Ground             |   | -    | 47   | -    | mA          |
| Ring Relay Drive V <sub>OL</sub>   | I <sub>OL</sub> = 62mA  | -    | 0.2  | 0.5  | V           |
| Ring Relay Driver Off Leakage      | V <sub>RD</sub> = +12V, R <sub>C</sub> = 1 = HIGH, T <sub>A</sub> = +25°C                             | -    | -    | 100  | µA          |
| Ring Trip Detection Period         | R <sub>L</sub> = 600 Ohms, T <sub>A</sub> = +25°C   | -    | 2    | 3    | Ring Cycles |
| Switch Hook Detection Threshold    | S <sub>HD</sub> = V <sub>OL</sub>   | 10   | -    | -    | mA          |
|                                    | S <sub>HD</sub> = V <sub>OH</sub>   | -    | -    | 5    | mA          |
| Ground Key Detection Threshold     | G <sub>KD</sub> = V <sub>OL</sub>   | 20   | -    | -    | mA          |
|                                    | G <sub>KD</sub> = V <sub>OH</sub>   | -    | -    | 10   | -           |
| Loop Current During Power Denial   | R <sub>L</sub> = 200 Ohms   | -    | ±2   | -    | mA          |
| Dial Pulse Distortion              |   | 0    | -    | 5    | ms          |
| Receive Input Impedance            | (Note 2)  | -    | 110  | -    | kOhms       |
| Transmit Output Impedance          | (Note 2)  | -    | 10   | 20   | Ohms        |
| Two Wire Return Loss               | (Referenced to 600Ω +2.16µF), (Note 2)  |      |      |      |             |
| SRL LO                             |   | -    | 15.5 | -    | dB          |
| ERL                                |   | -    | 24   | -    | dB          |
| SRL HI                             |   | -    | 31   | -    | dB          |
| Longitudinal Balance               | 1V <sub>RMS</sub> 200Hz - 3400Hz, (Note 2)  |      |      |      |             |
| 2 Wire Off Hook                    | IEEE Method   | 58   | 65   | -    | dB          |
| 2 Wire On Hook                     |   | 60   | 63   | -    | dB          |
| 4 Wire Off Hook                    | 0°C ≤ T <sub>A</sub> ≤ +75°C  | 50   | 58   | -    | dB          |
| Low Frequency Longitudinal Balance | R.E.A. Method, (Note 2), R <sub>L</sub> = 600,  | -    | -    | 23   | dBmC        |
|                                    | 0°C ≤ T <sub>A</sub> ≤ +75°C  | -    | -    | -67  | dBmOp       |

\* I<sub>Long</sub> = Longitudinal Current

NOTE: 1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

## Specifications HC-5502B

### Electrical Specifications (Continued)

| PARAMETERS   | CONDITIONS  | MIN                  | TYP              | MAX                   | UNITS                                  |
|--|---|----------------------|------------------|-----------------------|--|
| Insertion Loss<br>2 Wire - 4 Wire, 4 Wire - 2 Wire   | at 1kHz, 0dBm Input Level, Referenced 600Ω  | -                    | ±0.05            | ±0.2                  | dB                                     |
| Frequency Response   | 200 - 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level (Note 2)   | -                    | ±0.02            | ±0.05                 | dB                                     |
| Idle Channel Noise<br>2 Wire - 4 Wire, 4 Wire - 2 Wire   | (Note 2)  | -                    | 1                | 5                     | dBrnC                                  |
|  |   | -                    | -89              | -85                   | dBmOp                                  |
| Absolute Delay<br>2 Wire - 4 Wire, 4 Wire - 2 Wire   | (Note 2)  | -                    | -                | 2                     | μs                                     |
| Trans Hybrid Loss  | Balance Network Set Up for 600Ω Termination at 1kHz   | 36                   | 40               | -                     | dB                                     |
| Overload Level<br>2 Wire - 4 Wire, 4 Wire - 2 Wire   | V <sub>B+</sub> = +5V<br>V <sub>B+</sub> = +12V   | 1.5<br>1.75          | -                | -                     | V <sub>peak</sub><br>V <sub>peak</sub> |
| Level Linearity<br>2 Wire - 4 Wire, 4 Wire - 2 Wire  | at 1kHz, (Note 2)<br>+3 to -40dBm<br>-40 to -50dBm<br>-50 to -55dBm   | -                    | -                | ±0.05<br>±0.1<br>±0.3 | dB<br>dB<br>dB                         |
| Power Supply Rejection Ratio<br>V <sub>B+</sub> to 2 Wire<br>V <sub>B+</sub> to Transmit<br>V <sub>B-</sub> to 2 Wire<br>V <sub>B-</sub> to Transmit | (Note 2)<br>30 - 60Hz, R <sub>L</sub> = 600Ω  | 15<br>15<br>15<br>15 | -<br>-<br>-<br>- | -<br>-<br>-<br>-      | dB<br>dB<br>dB<br>dB                   |
| V <sub>B+</sub> to 2 Wire<br>V <sub>B+</sub> to Transmit<br>V <sub>B-</sub> to 2 Wire<br>V <sub>B-</sub> to Transmit                                 | 200 - 16kHz<br>R <sub>L</sub> = 600Ω  | 30<br>30<br>30<br>30 | -<br>-<br>-<br>- | -<br>-<br>-<br>-      | dB<br>dB<br>dB<br>dB                   |
| Logic Input Current (RS, RC, PD)   | 0V ≤ V <sub>IN</sub> ≤ +5V  | -                    | -                | ±100                  | μA                                     |
| Logic Inputs<br>Logic '0' V <sub>IL</sub><br>Logic '1' V <sub>IH</sub>   |   | -<br>2.0             | -<br>-           | 0.8<br>5.5            | Volts<br>Volts                         |
| Logic Outputs<br>Logic '0' V <sub>OL</sub><br>Logic '1' V <sub>OH</sub>  | I <sub>LOAD</sub> 800μA, V <sub>B+</sub> = +12V, +5V<br>I <sub>LOAD</sub> 80μA, V <sub>B+</sub> = +12V<br>I <sub>LOAD</sub> 40μA, V <sub>B+</sub> = +5V | -<br>2.7<br>2.7      | 0.1<br>5.0<br>-  | 0.5<br>5.5<br>5.0     | Volts<br>Volts<br>Volts                |

### Uncommitted Op Amp Specifications

| PARAMETER                     | CONDITIONS  | MIN | TYP      | MAX | UNITS                                  |
|-------------------------------|---|-----|----------|-----|--|
| Input Offset Voltage          |   | -   | ±5       | -   | mV                                     |
| Input Offset Current          |   | -   | ±10      | -   | nA                                     |
| Input Bias Current            |   | -   | 20       | -   | nA                                     |
| Differential Input Resistance | (Note 2)  | -   | 1        | -   | MΩ                                     |
| Output Voltage Swing          | R <sub>L</sub> = 10K, V <sub>B+</sub> = +12V<br>R <sub>L</sub> = 10K, V <sub>B+</sub> = +5V | -   | ±5<br>±3 | -   | V <sub>peak</sub><br>V <sub>peak</sub> |
| Output Resistance             | A <sub>VCL</sub> = 1 (Note 2)   | -   | 10       | -   | Ω                                      |
| Small Signal GBW              | (Note 2)  | -   | 1        | -   | MHz                                    |

NOTE: 2. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterised upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

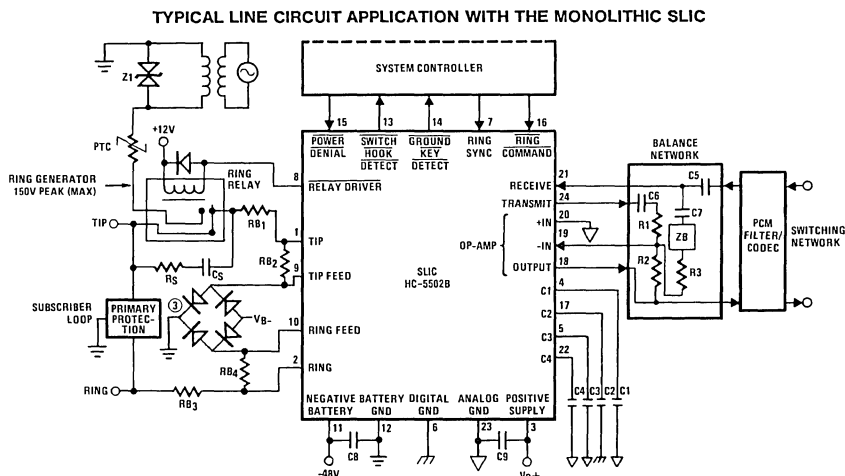
## Pin Assignments HC-5502B

| 28 PIN<br>PLCC | 24 PIN<br>DIP | SYMBOL                  | DESCRIPTION   |
|----------------|---------------|-------------------------|---|
| 2              | 1             | TIP                     | An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Ring terminal to receive voice signals from the telephone and for loop monitoring process.   |
| 3              | 2             | RING                    | An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.  |
| 4              | 3             | V <sub>B+</sub>         | Positive Voltage Source – Most positive supply. V <sub>B+</sub> is typically 12 volts or 5 volts.   |
| 5              | 4             | C1                      | Capacitor #1 – Optional Capacitor used to improve power supply rejection. This pin should be left open if unused.   |
| 6              | 5             | C3                      | Capacitor #3 – An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering V <sub>B-</sub> supply. Typical value is 0.3μF, 30V.   |
| 7              | 6             | DG                      | Digital Ground – To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC.  |
| 9              | 7             | RS                      | Ring Synchronization Input – A TTL – compatible clock input. The clock should be arranged such that a positive transition occurs on the negative going zero crossing of the ring voltage source, ensuring that the ring relay is activated and deactivated when the instantaneous ring voltage is near zero. If synchronization is not required, tie to +5V.  |
| 10             | 8             | $\overline{\text{RD}}$  | Relay Driver – A low active open collector logic output. When enabled, the external ring relay is energized.  |
| 11             | 9             | TF                      | Tip Feed – A low impedance analog output connected to the TIP terminal through a 150Ω feed resistor. Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.  |
| 12             | 10            | RF                      | Ring Feed – A low impedance analog output connected to the RING terminal through a 150Ω feed resistor. Functions with the TF terminal to provide loop current, feed voice signal to the telephone set, and sink longitudinal current.   |
| 13             | 11            | V <sub>B-</sub>         | Negative Voltage Source – Most negative supply. V <sub>B-</sub> is typically -48 volts with an operational range of -42 to -58 volts. Frequently referred to as "battery".  |
| 14             | 12            | BG                      | Battery Ground – To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.  |
| 16             | 13            | $\overline{\text{SHD}}$ | Switch Hook Detection – A low active LS TTL – compatible logic output. This output is enabled for loop currents exceeding 10mA and disabled for loop currents less than 5mA.  |
| 17             | 14            | $\overline{\text{GKD}}$ | Ground Key Detection – A low active LS TTL – compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 20mA, and disabled if this current difference is less than 10mA.  |
| 18             | 15            | $\overline{\text{PD}}$  | Power Denial – A low active TTL – Compatible logic input. When enabled the switch hook detect ( $\overline{\text{SHD}}$ ) and ground key detect ( $\overline{\text{GKD}}$ ) are not necessarily valid, and the relay driver ( $\overline{\text{RD}}$ ) output is disabled.  |
| 19             | 16            | $\overline{\text{RC}}$  | Ring Command – A low active TTL – Compatible logic input. When enabled, the relay driver ( $\overline{\text{RD}}$ ) output goes low on the next rising edge of the ring sync (RS) input, as long as the SLIC is not in the power denial state ( $\overline{\text{PD}} = 0$ ) or the subscriber is not already off-hook ( $\overline{\text{SHD}} = 0$ ).   |
| 20             | 17            | C2                      | Capacitor #2 – An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is 0.15μF, 10V. This capacitor is not used if ground key function is not required.  |
| 21             | 18            | OUT                     | The analog output of the spare operational amplifier.   |
| 23             | 19            | -IN                     | The inverting analog input of the spare operational amplifier.  |
| 24             | 20            | +IN                     | The non-inverting analog input of the spare operational amplifier.  |
| 25             | 21            | RX                      | Receive Input, Four Wire Side – A high impedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip feed and Ring feed amplifiers, which in turn drive tip and ring through 300 Ohms of feed resistance on each side of the line.  |
| 26             | 22            | C4                      | Capacitor #4 – An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from near by power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5μF, to 1.0μF, 20V. This capacitor should be nonpolarized. |
| 27             | 23            | AG                      | Analog Ground – To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.  |
| 28             | 24            | TX                      | Transmit Output, Four Wire Side – A low impedance analog output which represents the differential voltage across Tip and Ring. Transhybrid balancing must be performed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.          |
| 1,8,5,22       |               | NC                      | No Internal Connection.   |

NOTE: All grounds (AG, BG, & DG) must be applied before V<sub>B+</sub> or V<sub>B-</sub>. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

# HC-5502B

## Applications Diagram 1



### TYPICAL COMPONENT VALUES

- |  |  |
|--|--|
| C1 = 0.5 $\mu$ F (Note 1)  | C5 = 0.5 $\mu$ F, 20V                                    |
| C2 = 0.15 $\mu$ F, 10V   | C6 = C7 = 0.5 $\mu$ F (10% Match Required) (Note 2), 20V |
| C3 = 0.3 $\mu$ F, 30V  | C8 = 0.01 $\mu$ F, 100V                                  |
| C4 = 0.5 $\mu$ V to 1.0 $\mu$ F, $\pm$ 10%, 20V (Should be nonpolarized) | C9 = 0.01 $\mu$ F, 20V, $\pm$ 20%                        |

R1 = R2 = R3 = 100k $\Omega$  (0.1% Match Required, 1% absolute value), ZB = 0 for 600 $\Omega$  Terminations (Note 2)  
 RB1 = RB2 = RB3 = RB4 = 150 $\Omega$  (0.1% Match Required, 1% absolute value)  
 RS = 1k $\Omega$ , CS = 0.1 $\mu$ F, 200V typically, depending on V<sub>Ring</sub> and line length.  
 Z1 = 150V to 200V transient protector. PTC used as ring ballast.

NOTE 1: C1 is an optional capacitor used to improve V<sub>G+</sub> supply rejection. This pin must be left open if unused.

NOTE 2: To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C6-R1 and R2 and C7-ZB-R3, to match in impedance to within 0.3%. Thus, if C6 and C7 and 1 $\mu$ F each, a 20% match is adequate. It should be noted that the transmit output to C6 sees a -10.5 to -21 volt step when the loop is closed and that too large a value for C6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC.

A 0.5 $\mu$ F and 100k $\Omega$  gives a time constant of 50msec. The uncommitted op amp output is internally clamped to stay within  $\pm$ 5.5V and also has current limiting protection.

NOTE 3: Secondary protection diode bridge recommended is 2A, 200V type.

ADDITIONAL INFORMATION IS CONTAINED IN APPLICATION NOTE 549, "THE HC-550X TELEPHONE SLICs"  
 BY GEOFF PHILLIPS

## Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum of 30mA RMS, 15mA RMS per leg, without any performance degradation.

TABLE 1.

| PARAMETER          | TEST CONDITION     | PERFORMANCE (MAX)    | UNITS  |
|--------------------|--------------------|----------------------|--------|
| Longitudinal Surge | 10 $\mu$ s Rise/   | $\pm$ 1000 (Plastic) | V Peak |
|                    | 1000 $\mu$ s/Fall  | $\pm$ 500 (Ceramic)  | V Peak |
| Metallic Surge     | 10 $\mu$ s Rise/   | $\pm$ 1000 (Plastic) | V Peak |
|                    | 1000 $\mu$ Fall    | $\pm$ 500 (Ceramic)  | V Peak |
| T/GND              | 10 $\mu$ s Rise/   | $\pm$ 1000 (Plastic) | V Peak |
| R/GND              | 1000 $\mu$ s Fall  | $\pm$ 500 (Ceramic)  | V Peak |
| 50/60Hz Current    |                    |                      |        |
| T/GND              | 700V rms           | 11                   | Cycles |
| R/GND              | Limited to 10A rms | (Plastic)            |        |



August 1991

### Features

- Monolithic Integrated Device
- DI High Voltage Process
- Compatible With Worldwide PBX Performance Requirements
- Controlled Supply of Battery Feed Current for Short Loops (41mA)
- Internal Ring Relay Driver
- Allows Interfacing With Negative Superimposed Ringing Systems
- Low Power Consumption During Standby
- Switch Hook Ground Key and Ring Trip Detection Functions
- Selective Denial of Power to Subscriber Loops

### Applications

- Solid State Line Interface Circuit for Analog and Digital PBX Systems
- Direct Inward Dial (DID) Trunks
- Voice Messaging PBXs

### Description

The Harris SLIC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents.

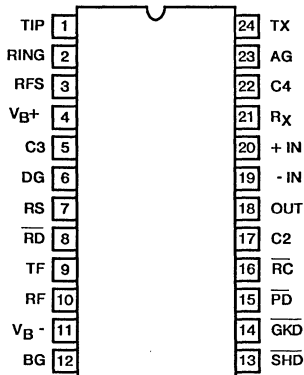
The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

The Harris SLIC is ideally suited for the design of new PBX systems, by eliminating bulky hybrid transformers.

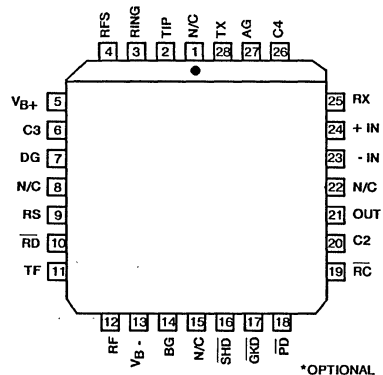
SLIC is available in either a 24 pin Dual-in-Line Plastic or Ceramic package and a 28 pin PLCC package.

### Pinouts

HC-5504  
(CERAMIC/PLASTIC DIP)  
TOP VIEW

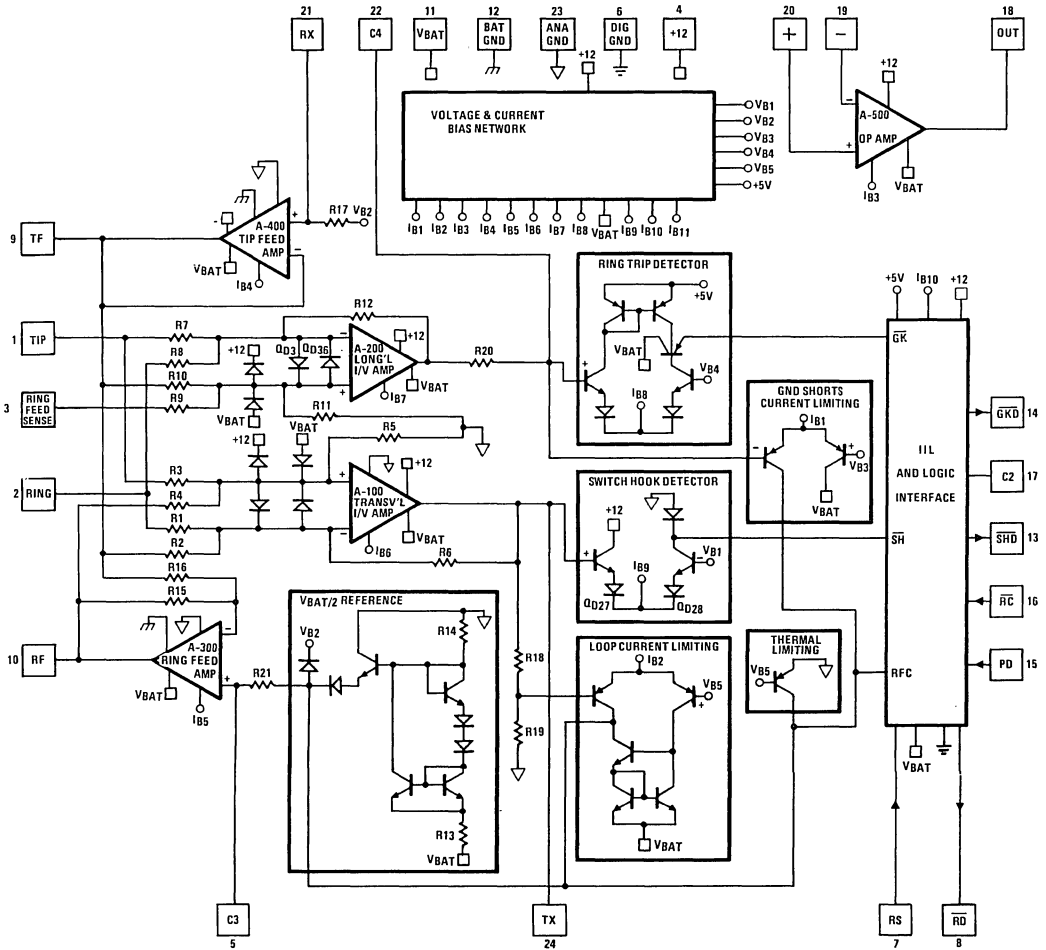


HC4P5504  
(PLCC)  
TOP VIEW



# HC-5504

## Schematic



HC-5504 SLIC FUNCTIONAL SCHEMATIC.

## Die Characteristics

|                           |               |               |
|---------------------------|---------------|---------------|
| Transistor Count .....    | 181           |               |
| Diode Count .....         | 27            |               |
| Die Dimensions .....      | 169 x 112     |               |
| Substrate Potential ..... | Unconnected   |               |
| Process .....             | Bipolar-DI    |               |
| Thermal Constants (°C/W)  | $\theta_{ja}$ | $\theta_{jc}$ |
| Ceramic DIP               | 51            | 16            |
| Plastic DIP               | 52            | 24            |
| PLCC                      | 68            | 25            |

## Specifications HC-5504

### Absolute Maximum Ratings (Note 1)

|                                    |                                      |       |                |
|------------------------------------|--------------------------------------|-------|----------------|
| Maximum Continuous Supply Voltages | (V <sub>B-</sub> )                   | ..... | -60 to +0.5 V  |
|                                    | (V <sub>B+</sub> )                   | ..... | -0.5 to +15 V  |
|                                    | (V <sub>B+</sub> - V <sub>B-</sub> ) | ..... | +75V           |
| Relay Drive Voltage (VRD)          | .....                                |       | -0.5 to +15V   |
| Storage Temperature Range          | .....                                |       | -65°C to 150°C |
| Junction Temperature               | .....                                |       | 175°C          |

### Recommended Operating Conditions

|  |       |                  |
|--|-------|------------------|
| Relay Driver Voltage (VRD)                 | ..... | +5 to +12V       |
| Positive Supply Voltage (V <sub>B+</sub> ) | ..... | 10.8 to 13.2V    |
| Negative Supply Voltage (V <sub>B-</sub> ) | ..... | -42 to -58V      |
| Minimum High Level Logic Input Voltage     | ..... | 2.4V             |
| Maximum Low Level Logic Input Voltage      | ..... | 0.6V             |
| Loop Resistance (R <sub>L</sub> )          | ..... | 200 to 1200 Ohms |
| Operating Temperature Range                |       |                  |
| HC-5504-5,-7                               | ..... | 0°C to +75°C     |
| HC-5504-9                                  | ..... | -40°C to +85°C   |

**Electrical Specifications** Unless Otherwise Specified, V<sub>B-</sub> = -48V, V<sub>B+</sub> = +12V, AG = BG = DG = 0V, Typical Parameters +25°C. Min-Max Parameters are Over Operating Temperature Range.

| PARAMETER                          | CONDITIONS   | MIN  | TYP  | MAX | UNITS       |
|------------------------------------|--|------|------|-----|-------------|
| On Hook Power Dissipation          | I <sub>Long</sub> = 0  | -    | 135  | 174 | mW          |
| Off Hook Power Dissipation         | R <sub>LINE</sub> = 600 Ohms, I <sub>Long</sub> = 0  | -    | 390  | 490 | mW          |
| Off Hook IB+                       | R <sub>LINE</sub> = 600 Ohms, I <sub>Long</sub> = 0 @ -40°C  | -    | -    | 5.0 | mA          |
| Off Hook IB+                       | R <sub>LINE</sub> = 600 Ohms, I <sub>Long</sub> = 0 @ +25°C  | -    | -    | 4.3 | mA          |
| Off Hook IB-                       | R <sub>LINE</sub> = 600 Ohms, I <sub>Long</sub> = 0  | -    | 35   | 40  | mA          |
| Off Hook Loop Current              | R <sub>LINE</sub> = 1200 Ohms, I <sub>Long</sub> = 0   | -    | 21   | -   | mA          |
| Off Hook Loop Current              | R <sub>LINE</sub> = 1200 Ohms, V <sub>B-</sub> = -42V, I <sub>Long</sub> = 0<br>T <sub>A</sub> = +25°C | 17.5 | -    | -   | mA          |
| Off Hook Loop Current              | R <sub>LINE</sub> = 200 Ohms, I <sub>Long</sub> = 0  | 36   | 41   | 48  | mA          |
| Fault Currents                     |  |      |      |     |             |
| TIP to Ground                      |  | -    | 14   | -   | mA          |
| RING to Ground                     |  | -    | 63   | -   | mA          |
| TIP to RING                        |  | -    | 41   | -   | mA          |
| TIP and RING to Ground             |  | -    | 63   | -   | mA          |
| Ring Relay Drive V <sub>OL</sub>   | I <sub>OL</sub> = 62mA   | -    | 0.2  | 0.5 | V           |
| Ring Relay Driver Off Leakage      | V <sub>RD</sub> = +12V, RC = 1 = HIGH, T <sub>A</sub> = 25°C   | -    | -    | 100 | µA          |
| Ring Rrip Detection Period         | R <sub>LINE</sub> = 600 Ohms   | -    | 2    | 3   | Ring Cycles |
| Switch Hook Detection Threshold    | $\overline{SHD} = V_{OL}$  | 10   | -    | -   | mA          |
|                                    | $\overline{SHD} = V_{OH}$  | -    | -    | 5   | mA          |
| Ground Key Detection Threshold     | $\overline{GKD} = V_{OL}$  | 20   | -    | -   | mA          |
|                                    | $\overline{GKD} = V_{OH}$  | -    | -    | 10  | -           |
| Loop Current During Power Denial   |  | -    | ±2   | -   | mA          |
| Dial Pulse Distortion              |  | 0    | -    | 5   | ms          |
| Receive Input Impedance            |  | -    | 90   | -   | kOhms       |
| Transmit Output Impedance          |  | -    | 5    | 20  | Ohms        |
| Two Wire Return Loss               | (Return Loss Referenced to 600Ω +2.16µF)   |      |      |     |             |
| SRL LO                             |  | -    | 15.5 | -   | dB          |
| ERL                                |  | -    | 24   | -   | dB          |
| SRL HI                             |  | -    | 31   | -   | dB          |
| Longitudinal Balance               | 1V Peak-Peak 200Hz - 3400Hz<br>0°C ≤ T <sub>A</sub> ≤ +75°C  |      |      |     |             |
| 2 Wire Off Hook                    |  | 58   | 65   | -   | dB          |
| 2Wire On Hook                      |  | 60   | 63   | -   | dB          |
| 4 Wire Off Hook                    |  | 50   | 58   | -   | dB          |
| Low Frequency Longitudinal Balance | R.E.A. Method, 0°C ≤ T <sub>A</sub> ≤ +75°C  | -    | -    | 23  | dBrnC       |
|                                    |  | -    | -    | -67 | dBmOp       |

NOTES: 1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

## Specifications HC-5504

### Electrical Specifications (Continued)

| PARAMETERS                       | CONDITIONS   | MIN  | TYP   | MAX   | UNITS |
|----------------------------------|--|------|-------|-------|-------|
| Insertion Loss                   | @ 1kHz, OdBm Input Level   | -    | ±0.05 | ±0.2  | dB    |
| 2 Wire - 4 Wire                  |  | -    | ±0.05 | ±0.2  | dB    |
| 4 Wire - 2 Wire                  |  | -    | ±0.02 | ±0.05 | dB    |
| Frequency Response               | 200 - 3400Hz Referenced to Absolute Loss at 1kHz and OdBm Signal Level | -    | -     | -     | dB    |
|                                  | $0^{\circ}\text{C} \leq T_A \leq 75^{\circ}\text{C}$                   |      |       |       |       |
|                                  | $0^{\circ}\text{C} \leq T_A \leq 75^{\circ}\text{C}$                   |      |       |       |       |
| Idle Channel Noise               |  | -    | -     | -     | dBmC  |
| 2 Wire - 4 Wire                  |  | -    | 1     | 5     | dBmC  |
|                                  |  | -    | -89   | -85   | dBm0p |
| 4 Wire - 2 Wire                  |  | -    | 1     | 5     | dBmC  |
|                                  |  | -    | -89   | -85   | dBm0p |
| Absolute Delay                   | $0^{\circ}\text{C} \leq T_A \leq 75^{\circ}\text{C}$                   | -    | -     | -     | µs    |
| 2 Wire - 4 Wire                  |  | -    | -     | 2     | µs    |
| 4 Wire - 2 Wire                  |  | -    | -     | 2     | µs    |
| Trans Hybrid Loss                | Balance Network Set Up for 600 Ohm Termination at 1kHz                 | 36   | 40    | -     | dB    |
| Overload Level                   | $0^{\circ}\text{C} \leq T_A \leq 75^{\circ}\text{C}$                   | -    | -     | -     | Vpeak |
| 2 Wire - 4 Wire                  |  | 1.75 | -     | -     | Vpeak |
| 4 Wire - 2 Wire                  |  | 1.75 | -     | -     | Vpeak |
| Level Linearity                  | at 1kHz, $0^{\circ}\text{C} \leq T_A \leq 75^{\circ}\text{C}$          | -    | -     | -     | dB    |
| 2 Wire - 4 Wire                  | +3 to -40dBm   | -    | -     | ±0.05 | dB    |
|                                  | -40 to -50dBm  | -    | -     | ±0.1  | dB    |
|                                  | -50 to -55dBm  | -    | -     | ±0.3  | dB    |
| 4 Wire - 2 Wire                  | +3 to -40dBm   | -    | -     | ±0.05 | dB    |
|                                  | -40 to -50dBm  | -    | -     | ±0.1  | dB    |
|                                  | -50 to -55dBm  | -    | -     | ±0.3  | dB    |
| Power Supply Rejection Ratio     | $0^{\circ}\text{C} \leq T_A \leq 75^{\circ}\text{C}$                   | -    | -     | -     | dB    |
| V <sub>B+</sub> to 2 Wire        | 30 - 60Hz, R <sub>LINE</sub> = 600Ω                                    | 15   | -     | -     | dB    |
| V <sub>B+</sub> to Transmit      |  | 15   | -     | -     | dB    |
| V <sub>B-</sub> to 2 Wire        |  | 15   | -     | -     | dB    |
| V <sub>B-</sub> to Transmit      |  | 15   | -     | -     | dB    |
| V <sub>B+</sub> to 2 Wire        | 200 - 16kHz  | 30   | -     | -     | dB    |
| V <sub>B+</sub> to Transmit      | R <sub>LINE</sub> = 600Ω   | 30   | -     | -     | dB    |
| V <sub>B-</sub> to 2 Wire        |  | 30   | -     | -     | dB    |
| V <sub>B-</sub> to Transmit      |  | 30   | -     | -     | dB    |
| Logic Input Current (RS, RC, PD) | $0\text{V} \leq V_{IN} \leq 5\text{V}$                                 | -    | -     | ±100  | µA    |
| Logic Inputs                     |  | -    | -     | -     | Volts |
| Logic '0' V <sub>I </sub>        |  | -    | -     | 0.8   | Volts |
| Logic '1' V <sub>I H</sub>       |  | 2.0  | -     | 5.5   | Volts |
| Logic Outputs                    |  | -    | -     | -     | Volts |
| Logic '0' V <sub>OL</sub>        | I <sub>LOAD</sub> 800µA  | -    | 0.1   | 0.5   | Volts |
| Logic '1' V <sub>OH</sub>        | I <sub>LOAD</sub> 80µA   | 2.7  | 5.0   | 5.5   | Volts |

### Uncommitted Op Amp Specifications

| PARAMETER                     | CONDITIONS           | MIN | TYP | MAX | UNITS |
|-------------------------------|----------------------|-----|-----|-----|-------|
| Input Offset Voltage          |                      | -   | ±5  | -   | mV    |
| Input Offset Current          |                      | -   | ±10 | -   | nA    |
| Input Bias Current            |                      | -   | 20  | -   | nA    |
| Differential Input Resistance |                      | -   | 1   | -   | MΩ    |
| Output Voltage Swing          | R <sub>L</sub> = 10K | -   | ±5  | -   | Vpeak |
| Output Resistance             | A <sub>VCL</sub> = 1 | -   | 10  | -   | Ω     |
| Small Signal GBW              |                      | -   | 1   | -   | MHz   |

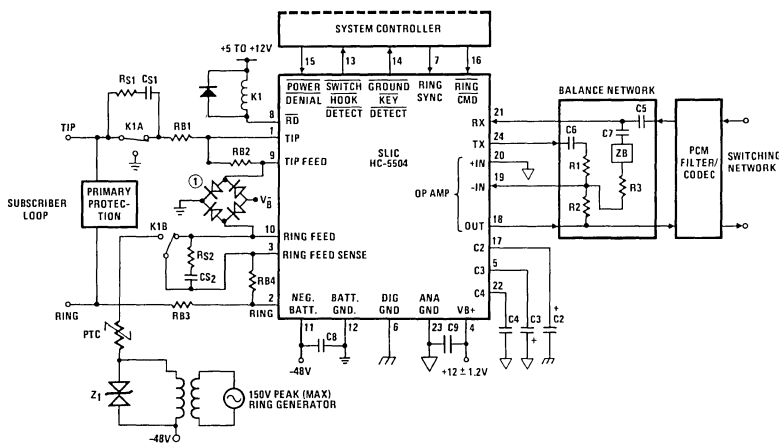
## Pin Assignments HC-5504

| 28 PIN PLCC | 24 PIN DIP | SYMBOL           | DESCRIPTION   |
|-------------|------------|------------------|---|
| 2           | 1          | TIP              | An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω feed resistor and a ring relay. Functions with the Ring terminal to receive voice signals from the telephone and for loop monitoring purposes.  |
| 3           | 2          | RING             | An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.   |
| 4           | 3          | RFS              | Senses ring side of loop for ground key and ring trip detection. During ringing, the ring signal is inserted into the line at this node and RF is isolated from RFS via a relay.  |
| 5           | 4          | V <sub>B+</sub>  | Positive Voltage Source - Most positive supply. V <sub>B+</sub> is typically 12 volts with an operational range of 10.8 to 13.2 volts.  |
| 6           | 5          | C3               | Capacitor #3 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering V <sub>B-</sub> . Typical value is 0.3μF, 30V.   |
| 7           | 6          | DG               | Digital Ground - To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC microcircuit.   |
| 9           | 7          | RS               | Ring Synchronization Input - A TTL - compatible clock input. The clock is arranged such that a positive pulse (50 -500μs) occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring relay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to +5V. |
| 10          | 8          | $\overline{RD}$  | Relay Driver - A low active open collector logic output. When enabled, the external ring relay is energized.  |
| 11          | 9          | TF               | Tip Feed - A low impedance analog output connected to the TIP terminal through a 150Ω feed resistor. Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.  |
| 12          | 10         | RF               | Ring Feed - A low impedance analog output connected to the RING terminal through a 150Ω feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal currents.   |
| 13          | 11         | V <sub>B-</sub>  | Negative Voltage Source - Most negative supply. V <sub>B-</sub> is typically -48 volts with an operational range of -42 to -58 volts. Frequently referred to as "battery".  |
| 14          | 12         | BG               | Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.  |
| 16          | 13         | $\overline{SHD}$ | Switch Hook Detection - A low active LS TTL - compatible logic output. This output is enabled for loop currents exceeding 10mA and disabled for loop currents less than 5mA.  |
| 17          | 14         | $\overline{GKD}$ | Ground Key Detection - A low active LS TTL - compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 20mA, and disabled if this current difference is less than 10mA.  |
| 18          | 15         | $\overline{PD}$  | Power Denial - A low active TTL - Compatible logic input. When enabled, the switch hook detect ( $\overline{SHD}$ ) and ground key detect ( $\overline{GKD}$ ) are not necessarily valid, and the relay driver ( $\overline{RD}$ ) output is disabled.  |
| 19          | 16         | $\overline{RC}$  | Ring Command - A low active TTL - Compatible logic input. When enabled, the relay driver ( $\overline{RD}$ ) output goes low on the next high level of the ring sync (RS) input, as long as the SLIC is not in the power denial state (PD = 0) or the subscriber is not already off-hook (SHD = 0).   |
| 20          | 17         | C2               | Capacitor #2 - An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is 0.15μF, 10V. This capacitor is not used if ground key function is not required and (Pin 17) may be left open or connected to digital ground.   |
| 21          | 18         | OUT              | The analog output of the spare operational amplifier. The output voltage swing is typically ±5V.  |
| 23          | 19         | -IN              | The inverting analog input of the spare operational amplifier.  |
| 24          | 20         | +IN              | The non-inverting analog input of the spare operational amplifier.  |
| 25          | 21         | RX               | Receive Input, Four Wire Side - A high impedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip feed and Ring feed terminals, which in turn drive tip and ring through 300 Ohms of feed resistance on each side of the line.   |
| 26          | 22         | C4               | Capacitor #4 - An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from near proximity power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5μF, to 1.0μF, 20V. This capacitor should be nonpolarized.  |
| 27          | 23         | AG               | Analog Ground - To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.  |
| 28          | 24         | TX               | Transmit Output, Four Wire Side - A low impedance analog output which represents the differential voltage across Tip and Ring. Transhybrid balancing must be preformed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.  |
| 1,8,15,22   |            | NC               | No Internal Connection.   |

NOTE: All grounds (AG, BG, & DG) must be applied before V<sub>B+</sub> or V<sub>B-</sub>. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

**Applications Diagram**

**TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC**



**TYPICAL COMPONENT VALUES**

- C2 = 0.15µF, 10V
- C3 = 0.3µF, 30V
- C4 = 0.5µF to 1.0µF, 10%, 20V (Should be nonpolarized)
- C5 = 0.5µF, 20V
- C6 = C7 = 0.5µF (10% Match Required) (Note 2)
- C8 = 0.01µF, 100V
- C9 = 0.01µF, 20V, ±20%

- R1 = R2 = R3 = 100k (0.1% Match Required, 1% absolute value) ZB = 0 for 600Ω Terminations (Note 2)
- RB1 = RB2 = RB3 = RB4 = 150Ω (0.1% Match Required, 1% absolute value)
- RS1 = RS2 = 1kΩ, typically.
- CS1 = CS2 = 0.1µF, 200V typically, depending on VRING and line length.
- Z1 = 150V to 200V transient protection.
- PTC used as ring generator ballast.

NOTE 1: Secondary protection diode bridge recommended is an MDA 220 or equivalent.

NOTE 2: To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C6-R1 and R2 and C7-ZB-R3, to match in impedance to within 0.3%. Thus, if C6 and C7 and 1µF each, a 20% match is adequate. It should be noted that the transmit output to C6 see's a -22V step when the loop is closed. Too large a value for C6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC.

A 0.5µF and 100kΩ gives a time constant of 50msec. The uncommitted op amp output is internally clamped to stay within ±5.5V and also has current limiting protection.

ADDITIONAL INFORMATION IS CONTAINED IN APPLICATION NOTE 549, "THE HC-550X TELEPHONE SLICs" BY GEOFF PHILLIPS

**Overvoltage Protection and Longitudinal Current Protection**

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum of 30mA RMS, 15mA RMA per leg, without any performance degradation.

**TABLE 1**

| PARAMETER          | TEST CONDITION     | PERFORMANCE (MAX) | UNITS  |
|--------------------|--------------------|-------------------|--------|
| Longitudinal Surge | 10µs Rise/         | ±1000 (Plastic)   | V Peak |
|                    | 1000µs/Fall        | ±500 (Ceramic)    | V Peak |
| Metallic Surge     | 10µs Rise/         | ±1000 (Plastic)   | V Peak |
|                    | 1000µ Fall         | ±500 (Ceramic)    | V Peak |
| T/GND              | 10µs Rise/         | ±1000 (Plastic)   | V Peak |
| R/GND              | 1000µs Fall        | ±500 (Ceramic)    | V Peak |
| 50/60Hz Current    |                    |                   |        |
| T/GND              | 700V rms           | 11                | Cycles |
| R/GND              | Limited to 10A rms |                   |        |

August 1991

### Features

- Pin for Pin Replacement for the HC-5504
- Capable of +5V or +12V (VB+) Operation
- Monolithic Integrated Device
- DI High Voltage Process
- Compatible With Worldwide PBX Performance Requirements
- Controlled Supply of Battery Feed Current for Short Loops (41mA)
- Internal Ring Relay Driver
- Allows Interfacing With Negative Superimposed Ringing Systems
- Low Power Consumption During Standby
- Switch Hook Ground Key and Ring Trip Detection Functions
- Selective Denial of Power to Subscriber Loops

### Applications

- Solid State Line Interface Circuit for Analog and Digital PBX Systems
- Direct Inward Dial (DID) Trunks
- Voice Messaging PBXs

### Description

The Harris SLIC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents. Using the unique Harris dielectric isolation process, the SLIC can operate directly with a wide range of station battery voltages.

The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

The Harris SLIC is ideally suited for the design of new digital PBX systems, by eliminating bulky hybrid transformers.

The SLIC is available in either a 24 pin Dual-in-Line Plastic or Ceramic package a 28 pin PLCC package, and a 24 pin SOIC package.

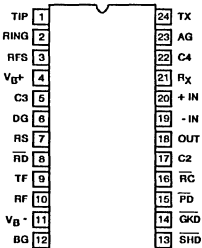
### Pinouts

HC1-5504B (24 PIN CERAMIC DIP)

HC3-5504B (24 PIN PLASTIC DIP)

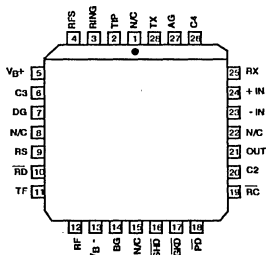
HC9P5504 (SOIC)

TOP VIEW

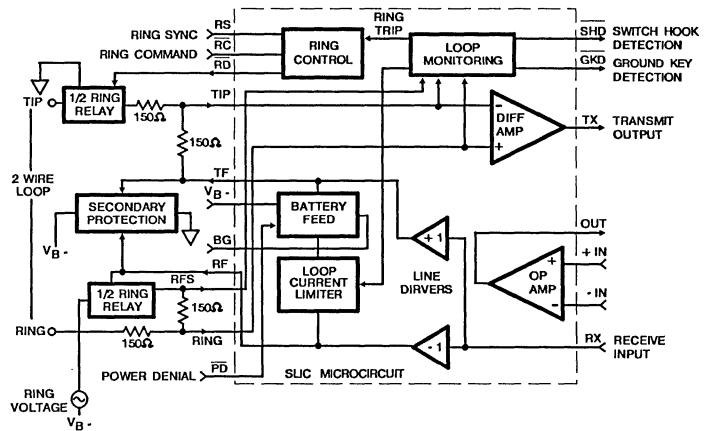


HC4P5504B (PLCC)

TOP VIEW

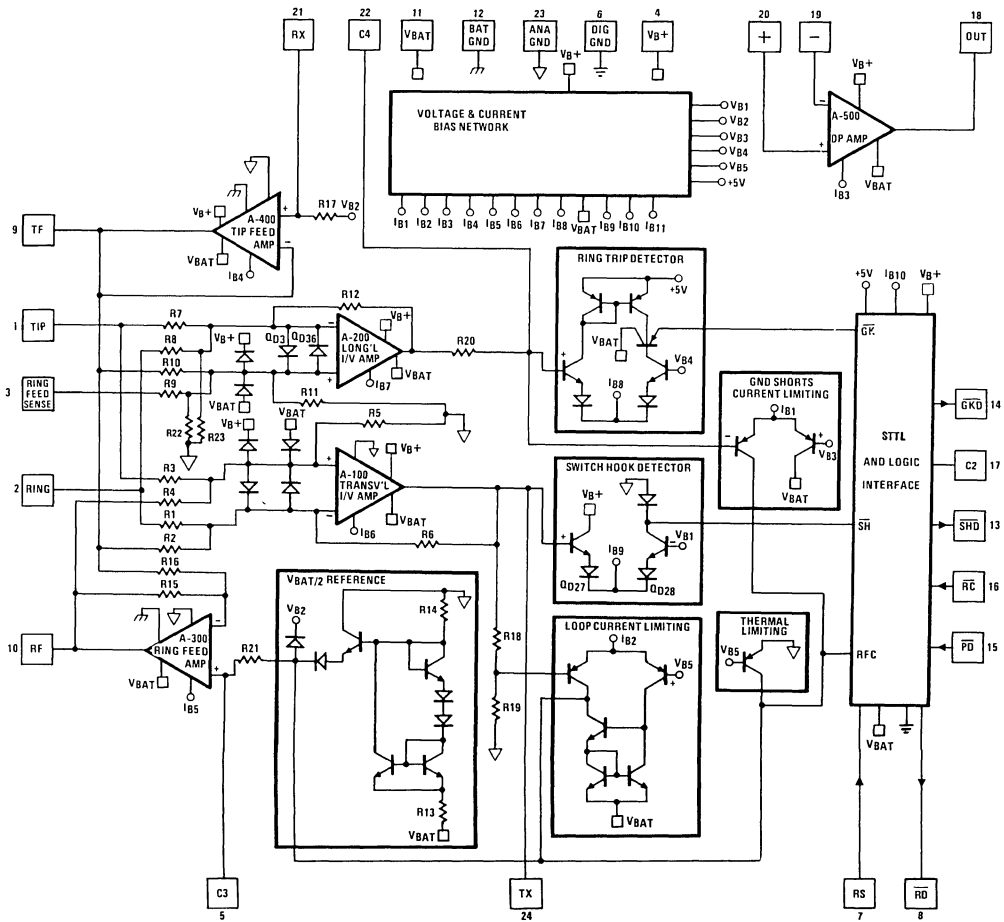


### Functional Diagram



# HC-5504B

## Schematic

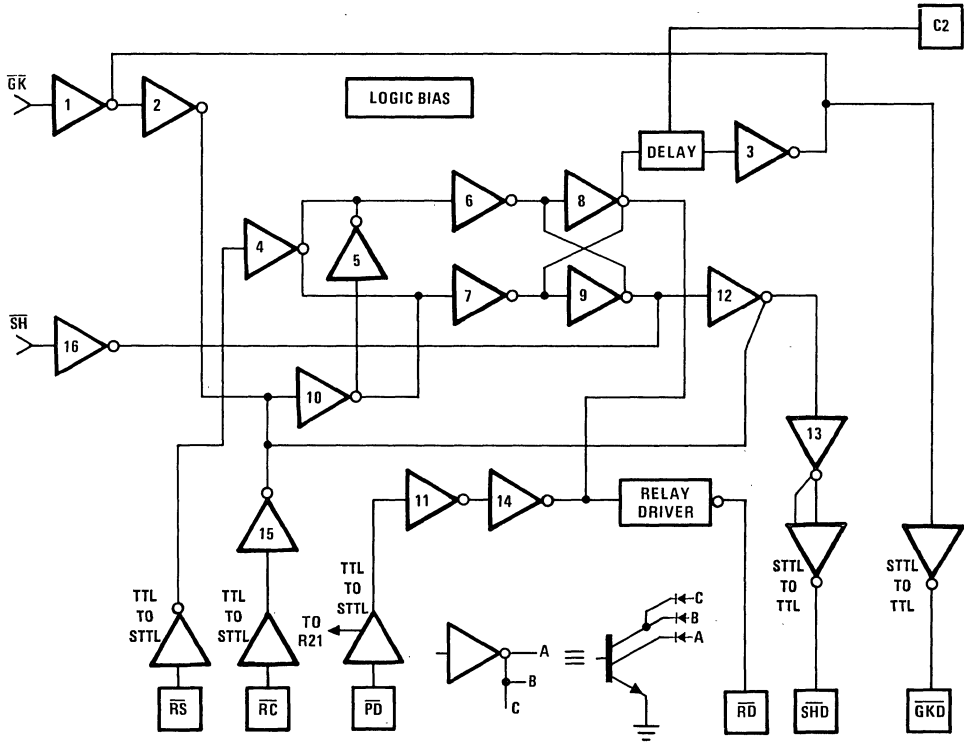


HC-5504B SLIC FUNCTIONAL SCHEMATIC



# HC-5504B

## Schematic (Continued)



HC-5504B LOGIC GATE SCHEMATIC

## Die Characteristics

|                           |               |               |
|---------------------------|---------------|---------------|
| Transistor Count .....    | 185           |               |
| Diode Count .....         | 36            |               |
| Die Dimensions .....      | 137 x 102     |               |
| Substrate Potential ..... | Connected     |               |
| Process .....             | Bipolar-DI    |               |
| Thermal Constants (OC/W)  | $\theta_{ja}$ | $\theta_{jc}$ |
| Ceramic DIP               | 52            | 15            |
| Plastic DIP               | 52            | 22            |
| PLCC                      | 67            | 29            |
| SOIC                      | 76            | 29            |

## Specifications HC-5504B

### Absolute Maximum Ratings (Note 1)

|  |   |
|--|---|
| Maximum Continuous Supply Voltages     | (V <sub>B-</sub> ) . . . . . -60 to +0.5 V          |
|  | (V <sub>B+</sub> ) . . . . . -0.5 to +15 V          |
|  | (V <sub>B+</sub> - V <sub>B-</sub> ) . . . . . +75V |
| Relay Drive Voltage (V <sub>RD</sub> ) | . . . . . -0.5 to +15V                              |
| Storage Temperature Range              | . . . . . -65°C to 150°C                            |
| Junction Temperature Ceramic           | . . . . . +175°C                                    |
| Junction Temperature Plastic           | . . . . . +150°C                                    |

### Recommended Operating Conditions

|  |   |
|--|---|
| Relay Driver Voltage (V <sub>RD</sub> )    | . . . . . +5 to +12V                    |
| Positive Supply Voltage (V <sub>B+</sub> ) | . . . . . 4.75 to 5.25 or 10.8 to 13.2V |
| Negative Supply Voltage (V <sub>B-</sub> ) | . . . . . -42 to -58V                   |
| High Level Logic Input Voltage             | . . . . . 2.4V                          |
| Low Level Logic Input Voltage              | . . . . . 0.6V                          |
| Loop Resistance (R <sub>L</sub> )          | . . . . . 200 to 1200 Ohms              |
| Operating Temperature Range                |   |
| HC-5504B-5                                 | . . . . . 0°C to +75°C                  |
| HC-5504B-9                                 | . . . . . -40°C to +85°C                |

**Electrical Specifications** Unless Otherwise Specified, V<sub>B-</sub> = -48V, V<sub>B+</sub> = +12V and +5V, AG = BG = DG = 0V, Typical Parameters T<sub>A</sub> = +25°C. Min-Max Parameters are Over Operating Temperature Range.

| PARAMETER                          | CONDITIONS  | MIN  | TYP  | MAX | UNITS       |
|------------------------------------|---|------|------|-----|-------------|
| On Hook Power Dissipation          | I <sub>Long</sub> * = 0, V <sub>B+</sub> = +12V   | -    | 170  | 235 | mW          |
| Off Hook Power Dissipation         | R <sub>L</sub> = 600 Ohms, I <sub>Long</sub> * = 0, V <sub>B+</sub> = +12V                            | -    | 425  | 550 | mW          |
| Off Hook IB+                       | R <sub>L</sub> = 600 Ohms, I <sub>Long</sub> * = 0, T <sub>A</sub> = -40°C                            | -    | -    | 6.0 | mA          |
| Off Hook IB+                       | R <sub>L</sub> = 600 Ohms, I <sub>Long</sub> * = 0, T <sub>A</sub> = +25°C                            | -    | -    | 5.3 | mA          |
| Off Hook IB-                       | R <sub>L</sub> = 600 Ohms, I <sub>Long</sub> * = 0  | -    | 35   | 41  | mA          |
| Off Hook Loop Current              | R <sub>L</sub> = 1200 Ohms, I <sub>Long</sub> * = 0   | -    | 21   | -   | mA          |
| Off Hook Loop Current              | R <sub>L</sub> = 1200 Ohms, V <sub>B-</sub> = -42V, I <sub>Long</sub> * = 0<br>T <sub>A</sub> = +25°C | 17.5 | -    | -   | mA          |
| Off Hook Loop Current              | R <sub>L</sub> = 200 Ohms, I <sub>Long</sub> * = 0  | 36   | 41   | 48  | mA          |
| Fault Currents                     |   |      |      |     |             |
| TIP to Ground                      |   | -    | 14   | -   | mA          |
| RING to Ground                     |   | -    | 55   | -   | mA          |
| TIP to RING                        |   | -    | 41   | -   | mA          |
| TIP and RING to Ground             |   | -    | 55   | -   | mA          |
| Ring Relay Drive V <sub>OL</sub>   | I <sub>OL</sub> = 62mA  | -    | 0.2  | 0.5 | V           |
| Ring Relay Driver Off Leakage      | V <sub>RD</sub> = +12V, R <sub>C</sub> = 1 = HIGH, T <sub>A</sub> = +25°C                             | -    | -    | 100 | μA          |
| Ring Trip Detection Period         | R <sub>L</sub> = 600 Ohms   | -    | 2    | 3   | Ring Cycles |
| Switch Hook Detection Threshold    | $\overline{SHD} = V_{OL}$   | 10   | -    | -   | mA          |
|                                    | $\overline{SHD} = V_{OH}$   | -    | -    | 5   | mA          |
| Ground Key Detection Threshold     | $\overline{GKD} = V_{OL}$   | 20   | -    | -   | mA          |
|                                    | $\overline{GKD} = V_{OH}$   | -    | -    | 10  | -           |
| Loop Current During Power Denial   | R <sub>L</sub> = 200 Ohms   | -    | ±2   | -   | mA          |
| Dial Pulse Distortion              |   | 0    | -    | 5   | ms          |
| Receive Input Impedance            | (Note 2)  | -    | 110  | -   | kOhms       |
| Transmit Output Impedance          | (Note 2)  | -    | 10   | 20  | Ohms        |
| Two Wire Return Loss               | (Referenced to 600Ω +2.16μF), (Note 2)  |      |      |     |             |
| SRL LO                             |   | -    | 15.5 | -   | dB          |
| ERL                                |   | -    | 24   | -   | dB          |
| SRL HI                             |   | -    | 31   | -   | dB          |
| Longitudinal Balance               | 1V <sub>RMS</sub> 200Hz - 3400Hz, (Note 2)  |      |      |     |             |
| 2 Wire Off Hook                    | IEEE Method   | 58   | 65   | -   | dB          |
| 2 Wire On Hook                     |   | 60   | 63   | -   | dB          |
| 4 Wire Off Hook                    | 0°C ≤ T <sub>A</sub> ≤ +75°C  | 50   | 58   | -   | dB          |
| Low Frequency Longitudinal Balance | R.E.A. Method, (Note 2), R <sub>L</sub> = 600   | -    | -    | 23  | dBmC        |
|                                    | 0°C ≤ T <sub>A</sub> ≤ +75°C  | -    | -    | -67 | dBm0p       |

\* I<sub>Long</sub> = Longitudinal Current

NOTE: 1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

## Specifications HC-5504B

### Electrical Specifications (Continued)

| PARAMETERS   | CONDITIONS  | MIN  | TYP   | MAX   | UNITS             |
|--|---|------|-------|-------|-------------------|
| Insertion Loss<br>2 Wire - 4 Wire, 4 Wire - 2 Wire   | at 1kHz, 0dBm Input Level, Referenced 600Ω  | -    | ±0.05 | ±0.2  | dB                |
| Frequency Response   | 200 - 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level (Note 2)   | -    | ±0.02 | ±0.05 | dB                |
| Idle Channel Noise<br>2 Wire - 4 Wire, 4 Wire - 2 Wire   | (Note 2)  | -    | 1     | 5     | dBmC              |
|  |   | -    | -89   | -85   | dBm0p             |
| Absolute Delay<br>2 Wire - 4 Wire, 4 Wire - 2 Wire   | (Note 2)  | -    | -     | 2     | μs                |
| Trans Hybrid Loss  | Balance Network Set Up for 600Ω Termination at 1kHz   | 36   | 40    | -     | dB                |
| Overload Level<br>2 Wire - 4 Wire, 4 Wire - 2 Wire   | V <sub>B+</sub> = +5V<br>V <sub>B+</sub> = +12V   | 1.5  | -     | -     | V <sub>peak</sub> |
|  |   | 1.75 | -     | -     | V <sub>peak</sub> |
| Level Linearity<br>2 Wire - 4 Wire, 4 Wire - 2 Wire  | at 1kHz, (Note 2)   |      |       |       |                   |
|  | +3 to -40dBm  | -    | -     | ±0.05 | dB                |
|  | -40 to -50dBm   | -    | -     | ±0.1  | dB                |
|  | -50 to -55dBm   | -    | -     | ±0.3  | dB                |
| Power Supply Rejection Ratio<br>V <sub>B+</sub> to 2 Wire<br>V <sub>B+</sub> to Transmit<br>V <sub>B-</sub> to 2 Wire<br>V <sub>B-</sub> to Transmit | (Note 2)<br>30 - 60Hz, R <sub>L</sub> = 600Ω  | 15   | -     | -     | dB                |
|  |   | 15   | -     | -     | dB                |
|  |   | 15   | -     | -     | dB                |
|  |   | 15   | -     | -     | dB                |
| V <sub>B+</sub> to 2 Wire<br>V <sub>B+</sub> to Transmit<br>V <sub>B-</sub> to 2 Wire<br>V <sub>B-</sub> to Transmit                                 | 200 - 16kHz<br>R <sub>L</sub> = 600Ω  | 30   | -     | -     | dB                |
|  |   | 30   | -     | -     | dB                |
|  |   | 30   | -     | -     | dB                |
|  |   | 30   | -     | -     | dB                |
| Logic Input Current (RS, RC, PD)   | 0V ≤ V <sub>IN</sub> ≤ +5V  | -    | -     | ±100  | μA                |
| Logic Inputs<br>Logic '0' V <sub>IL</sub><br>Logic '1' V <sub>IH</sub>   |   | -    | -     | 0.8   | Volts             |
|  |   | 2.0  | -     | 5.5   | Volts             |
| Logic Outputs<br>Logic '0' V <sub>OL</sub><br>Logic '1' V <sub>OH</sub>  | I <sub>LOAD</sub> 800μA, V <sub>B+</sub> = +12V, +5V<br>I <sub>LOAD</sub> 80μA, V <sub>B+</sub> = +12V<br>I <sub>LOAD</sub> 40μA, V <sub>B+</sub> = +5V | -    | 0.1   | 0.5   | Volts             |
|  |   | 2.7  | 5.0   | 5.5   | Volts             |
|  |   | 2.7  | -     | 5.0   | Volts             |

### Uncommitted Op Amp Specifications

| PARAMETER                     | CONDITIONS  | MIN | TYP | MAX | UNITS             |
|-------------------------------|---|-----|-----|-----|-------------------|
| Input Offset Voltage          |   | -   | ±5  | -   | mV                |
| Input Offset Current          |   | -   | ±10 | -   | nA                |
| Input Bias Current            |   | -   | 20  | -   | nA                |
| Differential Input Resistance | (Note 2)  | -   | 1   | -   | MΩ                |
| Output Voltage Swing          | R <sub>L</sub> = 10K, V <sub>B+</sub> = +12V<br>R <sub>L</sub> = 10K, V <sub>B+</sub> = +5V | -   | ±5  | -   | V <sub>peak</sub> |
|                               |   | -   | ±3  | -   | V <sub>peak</sub> |
| Output Resistance             | A <sub>VCL</sub> = 1 (Note 2)   | -   | 10  | -   | Ω                 |
| Small Signal GBW              | (Note 2)  | -   | 1   | -   | MHz               |

NOTE: 2. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterised upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

## Pin Assignments HC-5504B

| 28 PIN PLCC | 24 PIN DIP | SYMBOL           | DESCRIPTION   |
|-------------|------------|------------------|---|
| 2           | 1          | TIP              | An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Ring terminal to receive voice signals from the telephone and for loop monitoring purposes.  |
| 3           | 2          | RING             | An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.  |
| 4           | 3          | RFS              | Senses ring side of loop for ground key and ring trip detection. During ringing, the ring signal is inserted into the line at this node and RF is isolated from RFS via a relay.  |
| 5           | 4          | V <sub>B+</sub>  | Positive Voltage Source - Most positive supply. V <sub>B+</sub> is typically 12 volts or 5 volts.   |
| 6           | 5          | C3               | Capacitor #3 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering V <sub>B+</sub> . Typical value is 0.3μF, 30V.   |
| 7           | 6          | DG               | Digital Ground - To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC microcircuit.   |
| 9           | 7          | RS               | Ring Synchronization Input - A TTL - compatible clock input. The clock should be arranged such that a positive pulse transition occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring relay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to +5V. |
| 10          | 8          | $\overline{RD}$  | Relay Driver - A low active open collector logic output. When enabled, the external ring relay is energized.  |
| 11          | 9          | TF               | Tip Feed - A low impedance analog output connected to the TIP terminal through a 150Ω feed resistor. Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.  |
| 12          | 10         | RF               | Ring Feed - A low impedance analog output connected to the RING terminal through a 150Ω feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.  |
| 13          | 11         | V <sub>B-</sub>  | Negative Voltage Source - Most negative supply. V <sub>B-</sub> is typically -48 volts with an operational range of -42 to -58 volts. Frequently referred to as "battery".  |
| 14          | 12         | BG               | Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.  |
| 16          | 13         | $\overline{SHD}$ | Switch Hook Detection - A low active LS TTL - compatible logic output. This output is enabled for loop currents exceeding 10mA and disabled for loop currents less than 5mA.  |
| 17          | 14         | $\overline{GKD}$ | Ground Key Detection - A low active LS TTL - compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead by more than 20mA, and disabled if this current difference is less than 10mA.  |
| 18          | 15         | $\overline{PD}$  | Power Denial - A low active TTL - Compatible logic input. When enabled, the switch hook detect ( $\overline{SHD}$ ) and ground key detect ( $\overline{GKD}$ ) are not necessarily valid, and the relay driver ( $\overline{RD}$ ) output is disabled.  |
| 19          | 16         | $\overline{RC}$  | Ring Command - A low active TTL - Compatible logic input. When enabled, the relay driver ( $\overline{RD}$ ) output goes low on the next high level of the ring sync (RS) input, as long as the SLIC is not in the power denial state ( $\overline{PD} = 0$ ) or the subscriber is not already off-hook ( $\overline{SHD} = 0$ ).   |
| 20          | 17         | C2               | Capacitor #2 - An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is 0.15μF, 10V. This capacitor is not used if ground key function is not required and (Pin 17) may be left open or connected to digital ground.   |
| 21          | 18         | OUT              | The analog output of the spare operational amplifier. The output voltage swing is typically ±5V.  |
| 23          | 19         | -IN              | The inverting analog input of the spare operational amplifier.  |
| 24          | 20         | +IN              | The non-inverting analog input of the spare operational amplifier.  |
| 25          | 21         | RX               | Receive Input, Four Wire Side - A high impedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip feed and Ring feed terminals, which in turn drive tip and ring through 300 Ohms of feed resistance on each side of the line.   |
| 26          | 22         | C4               | Capacitor #4 - An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from near by power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5μF, to 1.0μF, 20V. This capacitor should be nonpolarized.   |
| 27          | 23         | AG               | Analog Ground - To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.  |
| 28          | 24         | TX               | Transmit Output, Four Wire Side - A low impedance analog output which represents the differential voltage across Tip and Ring. Transhybrid balancing must be performed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.  |
| 1,8,15,22   |            | NC               | No Internal Connection.   |

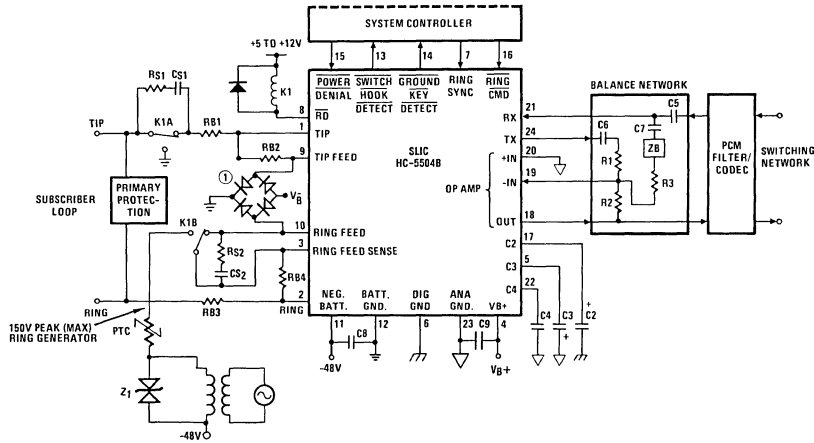
NOTE: All grounds (AG, BG, & DG) must be applied before V<sub>B+</sub> or V<sub>B-</sub>. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.



# HC-5504B

## Applications Diagram 1

### TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC



#### TYPICAL COMPONENT VALUES

C2 = 0.15 $\mu$ F, 10V

C3 = 0.3 $\mu$ F, 30V

C4 = 0.5 $\mu$ F to 1.0 $\mu$ F, 10%, 20V (Should be nonpolarized)

C5 = 0.5 $\mu$ F, 20V

C6 = C7 = 0.5 $\mu$ F (10% Match Required) (Note 2)

C8 = 0.01 $\mu$ F, 100V

C9 = 0.01 $\mu$ F, 20V,  $\pm$ 20%

R1 = R2 = R3 = 100k (0.1% Match Required, 1% absolute value) ZB = 0 for 600 $\Omega$  Terminations (Note 2)

RB1 = RB2 = RB3 = RB4 = 150 $\Omega$  (0.1% Match Required, 1% absolute value)

RS1 = RS2 = 1k $\Omega$ , typically.

CS1 = CS2 = 0.1 $\mu$ F, 200V typically, depending on V<sub>RING</sub> and line length.

Z1 = 150V to 200V transient protection.

PTC used as ring generator ballast.

NOTE 1: Secondary protection diode bridge recommended is a 2A, 200V type.

NOTE 2: To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C6-R1 and R2 and C7-ZB-R3, to match in impedance to within 0.3%. Thus, if C6 and C7 and 1 $\mu$ F each, a 20% match is adequate. It should be noted that the transmit output to C6 sees a -22V step when the loop is closed. Too large a value for C6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC.

A 0.5 $\mu$ F and 100k $\Omega$  gives a time constant of 50msec. The uncommitted op amp output is internally clamped to stay within  $\pm$ 5.5V and also has current limiting protection.

ADDITIONAL INFORMATION IS CONTAINED IN APPLICATION NOTE 549, "THE HC-550X TELEPHONE SLICs" BY GEOFF PHILLIPS

## Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum of 30mA RMS, 15mA RMS per leg, without any performance degradation.

TABLE 1

| PARAMETER          | TEST CONDITION    | PERFORMANCE (MAX)    | UNITS  |
|--------------------|-------------------|----------------------|--------|
| Longitudinal Surge | 10 $\mu$ s Rise/  | $\pm$ 1000 (Plastic) | V Peak |
|                    | 1000 $\mu$ s/Fall | $\pm$ 500 (Ceramic)  | V Peak |
| Metallic Surge     | 10 $\mu$ s Rise/  | $\pm$ 1000 (Plastic) | V Peak |
|                    | 1000 $\mu$ Fall   | $\pm$ 500 (Ceramic)  | V Peak |
| T/GND              | 10 $\mu$ s Rise/  | $\pm$ 1000 (Plastic) | V Peak |
| R/GND              | 1000 $\mu$ s Fall | $\pm$ 500 (Ceramic)  | V Peak |
| 50/60Hz Current    | T/GND             | 11                   | Cycles |
|                    | R/GND             | Limited to 10A RMS   |        |

August 1991

**Features**

- Pin for Pin Replacement for the HC-5504
- Capable of +5V or +12V (VB+) Operation
- Monolithic Integrated Device
- DI High Voltage Process
- Compatible With Worldwide PBX Performance Requirements
- Controlled Supply of Battery Feed Current for Short Loops (41mA)
- Internal Ring Relay Driver
- Allows Interfacing With Negative Superimposed Ringing Systems
- Low Power Consumption During Standby
- Switch Hook Ground Key and Ring Trip Detection Functions
- Selective Denial of Power to Subscriber Loops

**Applications**

- Solid State Line Interface Circuit for Analog and Digital PBX Systems
- Direct Inward Dial (DID) Trunks
- Voice Messaging PBXs
- Allows Multi-Phone Operation

**Description**

The Harris SLIC incorporates many of the BORSHT functions on a single IC chip. This includes DC battery feed, a ring relay driver, supervisory and hybrid functions. This device is designed to maintain transmission performance in the presence of externally induced longitudinal currents. Using the unique Harris dielectric isolation process, the SLIC can operate directly with a wide range of station battery voltages.

The SLIC also provides selective denial of power. If the PBX system becomes overloaded during an emergency, the SLIC will provide system protection by denying power to selected subscriber loops.

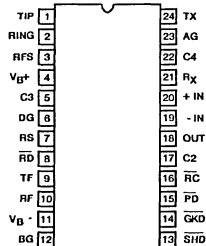
The Harris SLIC is ideally suited for the design of new digital PBX systems, by eliminating bulky hybrid transformers.

The SLIC is available in either a 24 pin Dual-in-Line Plastic or Ceramic package, a 28 pin PLCC package and a 24 pin SOIC package.

**Pinouts**

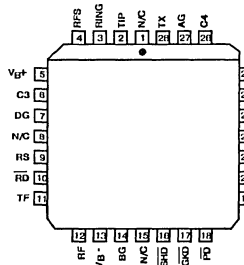
HC1-5504DLC (24 PIN CERAMIC DIP)  
 HC3-5504DLC (24 PIN PLASTIC DIP)  
 HC9P5504DLC (SOIC)

TOP VIEW

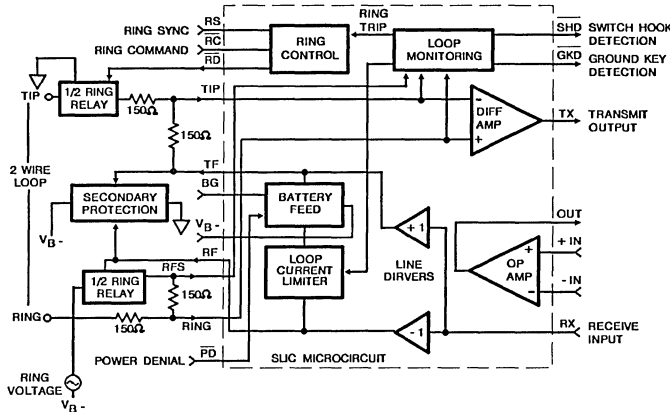


HC4P5504DLC (PLCC)

TOP VIEW



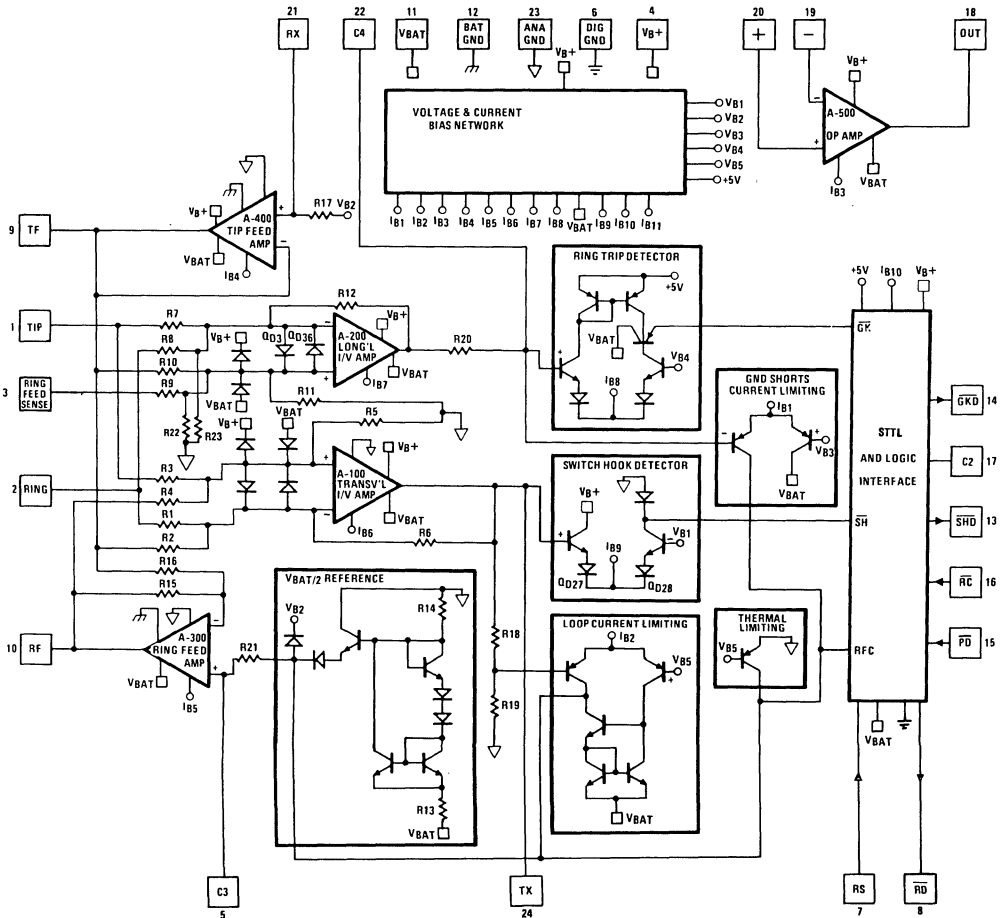
**Functional Diagram**



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.  
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# HC-5504DLC

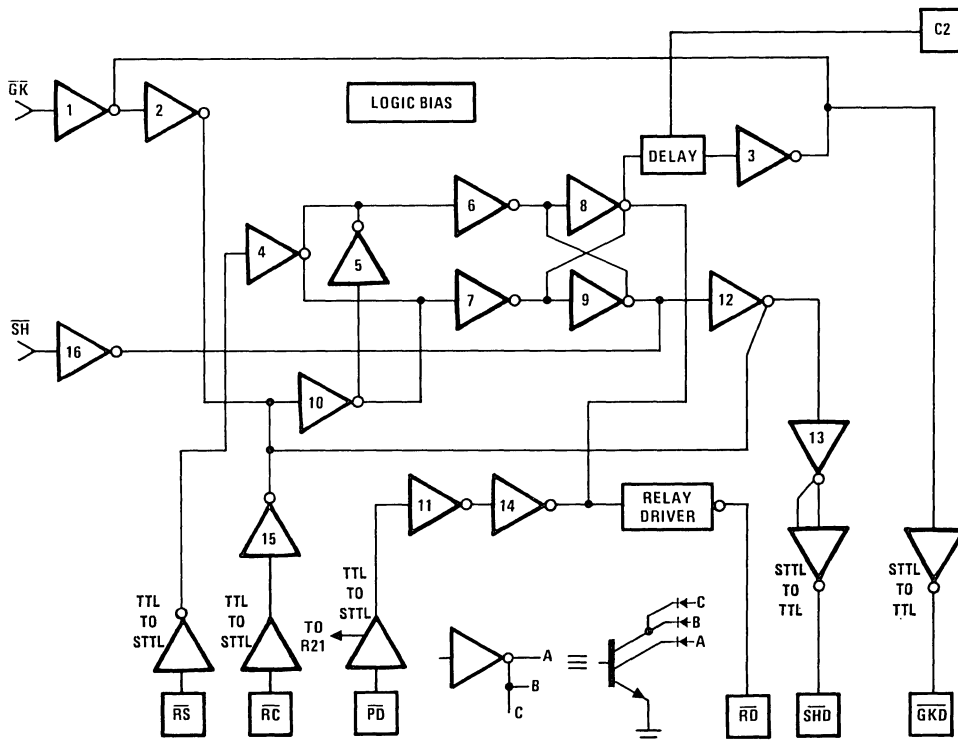
## Schematic



HC-5504DLC SLIC FUNCTIONAL SCHEMATIC

# HC-5504DLC

## Schematic (Continued)



HC-5504DLC LOGIC GATE SCHEMATIC

### Die Characteristics

|                           |                |               |
|---------------------------|----------------|---------------|
| Transistor Count .....    | 185            |               |
| Diode Count .....         | 36             |               |
| Die Dimensions .....      | 137 x 102 mils |               |
| Substrate Potential ..... | Connected      |               |
| Process .....             | Bipolar-DI     |               |
| Thermal Constants (°C/W)  | $\theta_{ja}$  | $\theta_{jc}$ |
| Ceramic DIP               | 52             | 15            |
| Plastic DIP               | 52             | 22            |
| PLCC                      | 67             | 29            |
| SOIC                      | 76             | 24            |



## Specifications HC-5504DLC

### Absolute Maximum Ratings (Note 1)

Maximum Continuous Supply Voltages (V<sub>B-</sub>) ..... -60 to +0.5 V  
 (V<sub>B+</sub>) ..... -0.5 to +15 V  
 (V<sub>B+</sub> - V<sub>B-</sub>) ..... +75 V  
 Relay Drive Voltage (V<sub>RD</sub>) ..... -0.5 to +15 V  
 Storage Temperature Range ..... -65°C to 150°C  
 Junction Temperature Ceramic ..... +175°C  
 Junction Temperature Plastic ..... +150°C

### Recommended Operating Conditions

Relay Driver Voltage (V<sub>RD</sub>) ..... +5 to +12V  
 Positive Supply Voltage (V<sub>B+</sub>) ..... 4.75 to 5.25 or 10.8 to 13.2V  
 Negative Supply Voltage (V<sub>B-</sub>) ..... -42 to -58V  
 High Level Logic Input Voltage ..... 2.4V  
 Low Level Logic Input Voltage ..... 0.6V  
 Loop Resistance (R<sub>L</sub>) ..... 200 to 1200 Ohms  
 Operating Temperature Range  
 HC-5504DLC-5 ..... 0°C to +75°C  
 HC-5504DLC-9 ..... -40°C to +85°C

### Electrical Specifications

Unless Otherwise Specified, V<sub>B-</sub> = -48V, V<sub>B+</sub> = +12V and +5V, AG = BG = DG = 0V,  
 Typical Parameters T<sub>A</sub> = +25°C. Min-Max Parameters are Over Operating Temperature Range.

| PARAMETER                          | CONDITIONS  | MIN  | TYP  | MAX | UNITS       |
|------------------------------------|---|------|------|-----|-------------|
| On Hook Power Dissipation          | I <sub>Long</sub> * = 0, V <sub>B+</sub> = +12V   | -    | 170  | 235 | mW          |
| Off Hook Power Dissipation         | R <sub>L</sub> = 600 Ohms, I <sub>Long</sub> * = 0, V <sub>B+</sub> = +12V                            | -    | 425  | 550 | mW          |
| Off Hook IB+                       | R <sub>L</sub> = 600 Ohms, I <sub>Long</sub> * = 0, T <sub>A</sub> = -40°C                            | -    | -    | 6.0 | mA          |
| Off Hook IB+                       | R <sub>L</sub> = 600 Ohms, I <sub>Long</sub> * = 0, T <sub>A</sub> = +25°C                            | -    | -    | 5.3 | mA          |
| Off Hook IB-                       | R <sub>L</sub> = 600 Ohms, I <sub>Long</sub> * = 0  | -    | 35   | 41  | mA          |
| Off Hook Loop Current              | R <sub>L</sub> = 1200 Ohms, I <sub>Long</sub> * = 0   | -    | 21   | -   | mA          |
| Off Hook Loop Current              | R <sub>L</sub> = 1200 Ohms, V <sub>B-</sub> = -42V, I <sub>Long</sub> * = 0<br>T <sub>A</sub> = +25°C | 17.5 | -    | -   | mA          |
| Off Hook Loop Current              | R <sub>L</sub> = 200 Ohms, I <sub>Long</sub> * = 0  | 36   | 41   | 48  | mA          |
| Fault Currents                     |   |      |      |     |             |
| TIP to Ground                      |   | -    | 14   | -   | mA          |
| RING to Ground                     |   | -    | 55   | -   | mA          |
| TIP to RING                        |   | -    | 41   | -   | mA          |
| TIP and RING to Ground             |   | -    | 55   | -   | mA          |
| Ring Relay Drive V <sub>OL</sub>   | I <sub>OL</sub> = 62mA  | -    | 0.2  | 0.5 | V           |
| Ring Relay Driver Off Leakage      | V <sub>RD</sub> = +12V, R <sub>C</sub> = 1 = HIGH, T <sub>A</sub> = +25°C                             | -    | -    | 100 | μA          |
| Ring Trip Detection Period         | R <sub>L</sub> = 600 Ohms   | -    | 2    | 3   | Ring Cycles |
| Switch Hook Detection Threshold    | $\overline{SHD} = V_{OL}$<br>$SHD = V_{OH}$   | 18   | -    | -   | mA          |
| Ground Key Detection Threshold     | $\overline{GKD} = V_{OL}$<br>$GKD = V_{OH}$   | 20   | -    | -   | mA          |
| Loop Current During Power Denial   | R <sub>L</sub> = 200 Ohms   | -    | ±2   | -   | mA          |
| Dial Pulse Distortion              |   | 0    | -    | 5   | ms          |
| Receive Input Impedance            | (Note 2)  | -    | 110  | -   | kOhms       |
| Transmit Output Impedance          | (Note 2)  | -    | 10   | 20  | Ohms        |
| Two Wire Return Loss               | (Referenced to 600Ω + 2.16μF), (Note 2)   |      |      |     |             |
| SRL LO                             |   | -    | 15.5 | -   | dB          |
| ERL                                |   | -    | 24   | -   | dB          |
| SRL HI                             |   | -    | 31   | -   | dB          |
| Longitudinal Balance               | 1V <sub>RMS</sub> 200Hz - 3400Hz, (Note 2)  |      |      |     |             |
| 2 Wire Off Hook                    | IEEE Method   | 58   | 65   | -   | dB          |
| 2 Wire On Hook                     |   | 60   | 63   | -   | dB          |
| 4 Wire Off Hook                    | 0°C ≤ T <sub>A</sub> ≤ +75°C  | 50   | 58   | -   | dB          |
| Low Frequency Longitudinal Balance | R.E.A. Method, (Note 2), R <sub>L</sub> = 600   | -    | -    | 23  | dBmC        |
|                                    | 0°C ≤ T <sub>A</sub> ≤ +75°C  | -    | -    | -67 | dBmOp       |

\* I<sub>Long</sub> = Longitudinal Current

NOTE: 1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

## Specifications HC-5504DLC

### Electrical Specifications (Continued)

| PARAMETERS   | CONDITIONS  | MIN                  | TYP              | MAX                   | UNITS                                  |
|--|---|----------------------|------------------|-----------------------|--|
| Insertion Loss<br>2 Wire - 4 Wire, 4 Wire - 2 Wire   | at 1kHz, 0dBm Input Level, Referenced 600Ω  | -                    | ±0.05            | ±0.2                  | dB                                     |
| Frequency Response   | 200 - 3400Hz Referenced to Absolute Loss at 1kHz and 0dBm Signal Level (Note 2)   | -                    | ±0.02            | ±0.05                 | dB                                     |
| Idle Channel Noise<br>2 Wire - 4 Wire, 4 Wire - 2 Wire   | (Note 2)  | -                    | 1                | 5                     | dBmC                                   |
|  |   | -                    | -89              | -85                   | dBmOp                                  |
| Absolute Delay<br>2 Wire - 4 Wire, 4 Wire - 2 Wire   | (Note 2)  | -                    | -                | 2                     | μs                                     |
| Trans Hybrid Loss  | Balance Network Set Up for 600Ω Termination at 1kHz   | 36                   | 40               | -                     | dB                                     |
| Overload Level<br>2 Wire - 4 Wire, 4 Wire - 2 Wire   | V <sub>B+</sub> = +5V<br>V <sub>B+</sub> = +12V   | 1.5<br>1.75          | -                | -                     | V <sub>peak</sub><br>V <sub>peak</sub> |
| Level Linearity<br>2 Wire - 4 Wire, 4 Wire - 2 Wire  | at 1kHz, (Note 2)<br>+3 to -40dBm<br>-40 to -50dBm<br>-50 to -55dBm   | -                    | -                | ±0.05<br>±0.1<br>±0.3 | dB<br>dB<br>dB                         |
| Power Supply Rejection Ratio<br>V <sub>B+</sub> to 2 Wire<br>V <sub>B+</sub> to Transmit<br>V <sub>B-</sub> to 2 Wire<br>V <sub>B-</sub> to Transmit | (Note 2)<br>30 - 60Hz, R <sub>L</sub> = 600Ω  | 15<br>15<br>15<br>15 | -<br>-<br>-<br>- | -<br>-<br>-<br>-      | dB<br>dB<br>dB<br>dB                   |
| V <sub>B+</sub> to 2 Wire<br>V <sub>B+</sub> to Transmit<br>V <sub>B-</sub> to 2 Wire<br>V <sub>B-</sub> to Transmit                                 | 200 - 16kHz<br>R <sub>L</sub> = 600Ω  | 30<br>30<br>30<br>30 | -<br>-<br>-<br>- | -<br>-<br>-<br>-      | dB<br>dB<br>dB<br>dB                   |
| Logic Input Current (RS, RC, PD)   | 0V ≤ V <sub>IN</sub> ≤ +5V  | -                    | -                | ±100                  | μA                                     |
| Logic Inputs<br>Logic '0' V <sub>IL</sub><br>Logic '1' V <sub>IH</sub>   |   | -<br>2.0             | -<br>-           | 0.8<br>5.5            | Volts<br>Volts                         |
| Logic Outputs<br>Logic '0' V <sub>OL</sub><br>Logic '1' V <sub>OH</sub>  | I <sub>LOAD</sub> 800μA, V <sub>B+</sub> = +12V, +5V<br>I <sub>LOAD</sub> 80μA, V <sub>B+</sub> = +12V<br>I <sub>LOAD</sub> 40μA, V <sub>B+</sub> = +5V | -<br>2.7<br>2.7      | 0.1<br>5.0<br>-  | 0.5<br>5.5<br>5.0     | Volts<br>Volts<br>Volts                |

### Uncommitted Op Amp Specifications

| PARAMETER                     | CONDITIONS  | MIN | TYP      | MAX | UNITS                                  |
|-------------------------------|---|-----|----------|-----|--|
| Input Offset Voltage          |   | -   | ±5       | -   | mV                                     |
| Input Offset Current          |   | -   | ±10      | -   | nA                                     |
| Input Bias Current            |   | -   | 20       | -   | nA                                     |
| Differential Input Resistance | (Note 2)  | -   | 1        | -   | MΩ                                     |
| Output Voltage Swing          | R <sub>L</sub> = 10K, V <sub>B+</sub> = +12V<br>R <sub>L</sub> = 10K, V <sub>B+</sub> = +5V | -   | ±5<br>±3 | -   | V <sub>peak</sub><br>V <sub>peak</sub> |
| Output Resistance             | A <sub>VCL</sub> = 1 (Note 2)   | -   | 10       | -   | Ω                                      |
| Small Signal GBW              | (Note 2)  | -   | 1        | -   | MHz                                    |

NOTE: 2. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterised upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

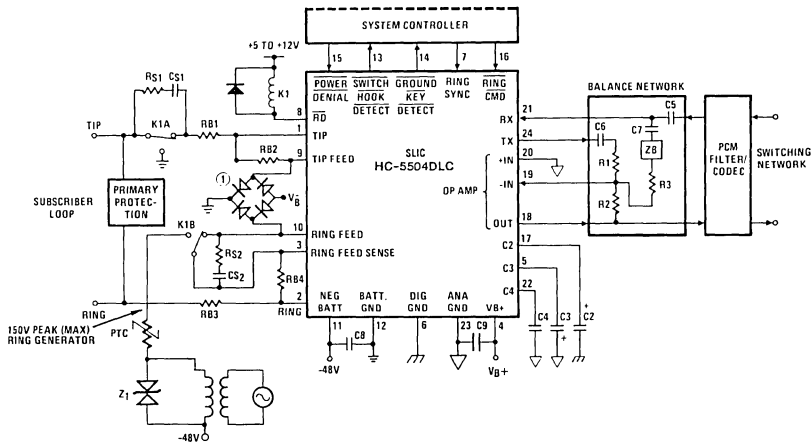
## Pin Assignments HC-5504DLC

| 28 PIN<br>PLCC | 24 PIN<br>DIP | SYMBOL                  | DESCRIPTION   |
|----------------|---------------|-------------------------|---|
| 2              | 1             | TIP                     | An analog input connected to the TIP (more positive) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Ring terminal to receive voice signals from the telephone and for loop monitoring purposes.  |
| 3              | 2             | RING                    | An analog input connected to the RING (more negative) side of the subscriber loop through a 150Ω feed resistor and a ring relay contact. Functions with the Tip terminal to receive voice signals from the telephone and for loop monitoring purposes.  |
| 4              | 3             | RFS                     | Senses ring side of loop for ground key and ring trip detection. During ringing, the ring signal is inserted into the line at this node and RF is isolated from RFS via a relay.  |
| 5              | 4             | V <sub>B+</sub>         | Positive Voltage Source – Most positive supply. V <sub>B+</sub> is typically 12 volts or 5 volts.   |
| 6              | 5             | C3                      | Capacitor #3 – An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function, and for filtering V <sub>B-</sub> . Typical value is 0.3μF, 30V.   |
| 7              | 6             | DG                      | Digital Ground – To be connected to zero potential and serves as a reference for all digital inputs and outputs on the SLIC microcircuit.   |
| 9              | 7             | RS                      | Ring Synchronization Input – A TTL – compatible clock input. The clock should be arranged such that a positive pulse transition occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring relay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to +5V. |
| 10             | 8             | $\overline{\text{RD}}$  | Relay Driver – A low active open collector logic output. When enabled, the external ring relay is energized.  |
| 11             | 9             | TF                      | Tip Feed – A low impedance analog output connected to the TIP terminal through a 150Ω feed resistor. Functions with the RF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.  |
| 12             | 10            | RF                      | Ring Feed – A low impedance analog output connected to the RING terminal through a 150Ω feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and sink longitudinal current.  |
| 13             | 11            | V <sub>B-</sub>         | Negative Voltage Source – Most negative supply. V <sub>B-</sub> is typically -48 volts with an operational range of -42 to -58 volts. Frequently referred to as "battery".  |
| 14             | 12            | BG                      | Battery Ground – To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.  |
| 16             | 13            | $\overline{\text{SHD}}$ | Switch Hook Detection – A low active LS TTL – compatible logic output.  |
| 17             | 14            | $\overline{\text{GKD}}$ | Ground Key Detection – A low active LS TTL – compatible logic output. This output is enabled if the DC current into the ring lead exceeds the DC current out of the tip lead and disabled if this current difference is below an internally set threshold.  |
| 18             | 15            | $\overline{\text{PD}}$  | Power Denial – A low active TTL – Compatible logic input. When enabled, the switch hook detect ( $\overline{\text{SHD}}$ ) and ground key detect ( $\overline{\text{GKD}}$ ) are not necessarily valid, and the relay driver ( $\overline{\text{RD}}$ ) output is disabled.   |
| 19             | 16            | $\overline{\text{RC}}$  | Ring Command – A low active TTL – Compatible logic input. When enabled, the relay driver ( $\overline{\text{RD}}$ ) output goes low on the next high level of the ring sync (RS) input, as long as the SLIC is not in the power denial state ( $\overline{\text{PD}} = 0$ ) or the subscriber is not already off-hook ( $\overline{\text{SHD}} = 0$ ).  |
| 20             | 17            | C2                      | Capacitor #2 – An external capacitor to be connected between this terminal and digital ground. Prevents false ground key indications from occurring during ring trip detection. Typical value is 0.15μF, 10V. This capacitor is not used if ground key function is not required and (Pin 17) may be left open or connected to digital ground.   |
| 21             | 18            | OUT                     | The analog output of the spare operational amplifier. The output voltage swing is typically ±5V.  |
| 23             | 19            | -IN                     | The inverting analog input of the spare operational amplifier.  |
| 24             | 20            | +IN                     | The non-inverting analog input of the spare operational amplifier.  |
| 25             | 21            | RX                      | Receive Input, Four Wire Side – A high impedance analog input which is internally biased. Capacitive coupling to this input is required. AC signals appearing at this input differentially drive the Tip feed and Ring feed terminals, which in turn drive tip and ring through 300 Ohms of feed resistance on each side of the line.   |
| 26             | 22            | C4                      | Capacitor #4 – An external capacitor to be connected between this terminal and analog ground. This capacitor prevents false ground key indication and false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from near by power lines and other noise sources. This capacitor is also required for the proper operation of ring trip detection. Typical value is 0.5μF, to 1.0μF, 20V. This capacitor should be nonpolarized.   |
| 27             | 23            | AG                      | Analog Ground – To be connected to zero potential and serves as a reference for the transmit output (TX) and receive input (RX) terminals.  |
| 28             | 24            | TX                      | Transmit Output, Four Wire Side – A low impedance analog output which represents the differential voltage across Tip and Ring. Transhybrid balancing must be performed (using the SLIC microcircuit's spare op amp) beyond this output to completely implement two to four wire conversion. This output is unbalanced and referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is essential.  |
| 1,8,15,22      |               | NC                      | No Internal Connection.   |

NOTE: All grounds (AG, BG, & DG) must be applied before V<sub>B+</sub> or V<sub>B-</sub>. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Applications Diagram 1

TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC



TYPICAL COMPONENT VALUES

- C2 = 0.15µF, 10V
- C3 = 0.3µF, 30V
- C4 = 0.5µF to 1.0µF, 10%, 20V (Should be nonpolarized)
- C5 = 0.5µF, 20V
- C6 = C7 = 0.5µF (10% Match Required) (Note 2)
- C8 = 0.01µF, 100V
- C9 = 0.01µF, 20V, ±20%

- R1 = R2 = R3 = 100k (0.1% Match Required, 1% absolute value) ZB = 0 for 600Ω Terminations (Note 2)
- RB1 = RB2 = RB3 = RB4 = 150Ω (0.1% Match Required, 1% absolute value)
- RS1 = RS2 = 1kΩ, typically.
- CS1 = CS2 = 0.1µF, 200V typically, depending on V<sub>RING</sub> and line length.
- Z1 = 150V to 200V transient protection.
- PTC used as ring generator ballast.

NOTE 1: Secondary protection diode bridge recommended is a 2A, 200V type.

NOTE 2: To obtain the specified transhybrid loss it is necessary for the three legs of the balance network, C6-R1 and R2 and C7-ZB-R3, to match in impedance to within 0.3%. Thus, if C6 and C7 and 1µF each, a 20% match is adequate. It should be noted that the transmit output to C6 sees a -22V step when the loop is closed. Too large a value for C6 may produce an excessively long transient at the op amp output to the PCM Filter/CODEC.

A 0.5µF and 100kΩ gives a time constant of 50msec. The uncommitted op amp output is internally clamped to stay within ±5.5V and also has current limiting protection.

ADDITIONAL INFORMATION IS CONTAINED IN APPLICATION NOTE 549, "THE HC-550X TELEPHONE SLICs" BY GEOFF PHILLIPS

**Overtoltage Protection and Longitudinal Current Protection**

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum of 30mA RMS, 15mA RMS per leg, without any performance degradation.

TABLE 1

| PARAMETER          | TEST CONDITION | PERFORMANCE (MAX)  | UNITS     |
|--------------------|----------------|--------------------|-----------|
| Longitudinal Surge | 10µs Rise/     | ±1000 (Plastic)    | V Peak    |
|                    | 1000µs/Fall    | ±500 (Ceramic)     | V Peak    |
| Metallic Surge     | 10µs Rise/     | ±1000 (Plastic)    | V Peak    |
|                    | 1000µ Fall     | ±500 (Ceramic)     | V Peak    |
| T/GND              | 10µs Rise/     | ±1000 (Plastic)    | V Peak    |
|                    | 1000µs Fall    | ±500 (Ceramic)     | V Peak    |
| 50/60Hz Current    | T/GND          | 700V RMS           | 11 Cycles |
|                    | R/GND          | Limited to 10A RMS | (Plastic) |

9 TELECOM

August 1991

## Subscriber Line Interface Circuit - SLIC

### Features

- DI Monolithic High Voltage Process
- Compatible with Worldwide PBX and CO Performance Requirements
- Controlled Supply of Battery Feed Current With Programmable Current Limit
- Operates with 5 Volt Positive Supply (VB+)
- Internal Ring Relay Driver and a Utility Relay Driver
- High Impedance Mode for Subscriber Loop
- High Temperature Alarm Output
- Low Power Consumption During Standby Functions
- Switch Hook, Ground Key, and Ring Trip Detection
- Selective Power Denial to Subscriber
- Voice Path Active During Power Denial
- On Chip Op-Amp for 2 Wire Impedance Matching

### Applications

- Solid State Line Interface Circuit for PBX or Central Office Systems, Digital Loop Carrier Systems
- Hotel/Motel Switching Systems
- Direct Inward Dialing (DID) Trunks
- Voice Messaging PBX's
- High Voltage 2W/4W, 4W/2W Hybrid

### Description

The HC-5509B telephone Subscriber Line Interface Circuit integrates most of the BORSCHT functions on a monolithic IC. The device is manufactured in a Dielectric Isolation (DI) process and is designed for use as a high voltage interface between the traditional telephone subscriber pair (Tip and Ring) and the low voltage filtering and coding/decoding functions of the line card. Together with a secondary protection diode bridge and "feed" resistors, the device will withstand 1000V lightning induced surges, in plastic packages. The SLIC also maintains specified transmission performance in the presence of externally induced longitudinal currents. The BORSCHT functions that the SLIC provides are:

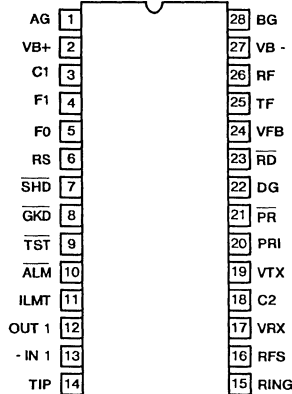
- Battery Feed with Subscriber Loop Current Limiting
- Overvoltage Protection
- Ring Relay Driver
- Supervisory Signaling Functions
- Hybrid Functions (with External Op-Amp)
- Test (or Battery Reversal) Relay Driver

In addition, the SLIC provides selective denial of power to subscriber loops, a programmable subscriber loop current limit from 20 to 60mA, a thermal shutdown with an alarm output and line fault protection. Switch hook detection, ring trip detection and ground key detection functions are also incorporated in the SLIC device.

The HC-5509B SLIC is available in a 28 pin Dual-in-Line Ceramic or Plastic package, a 44 pin Plastic Leaded Chip Carrier, or in a 28 Pin SOIC. It is ideally suited for line card designs in PBX and CO systems, replacing traditional transformer solutions.

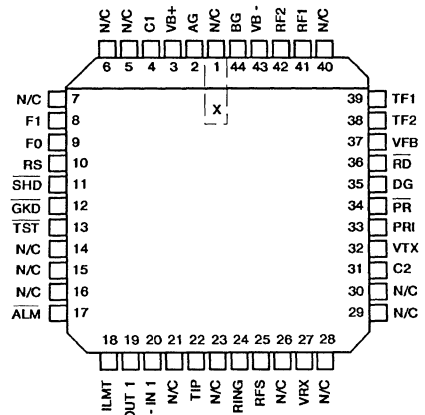
### Pinouts

HC1-5509B, HC3-5509B,  
& HC9P5509B  
TOP VIEW



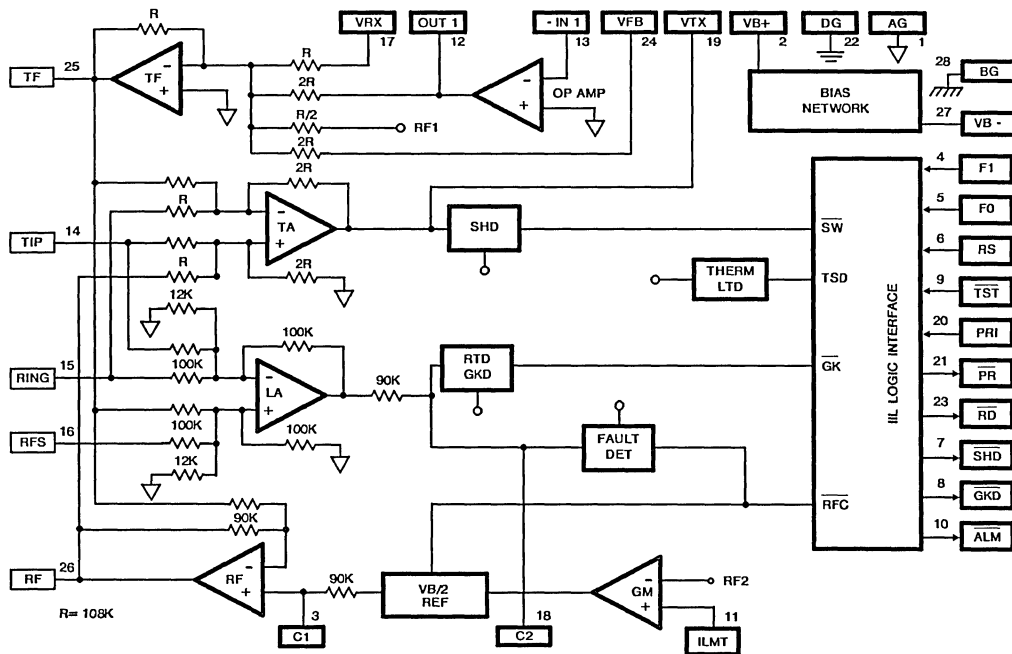
| TRUTH TABLE |    |                             |
|-------------|----|-----------------------------|
| F1          | F0 | Action                      |
| 0           | 0  | Normal Loop Feed            |
| 0           | 1  | RD Active                   |
| 1           | 0  | Power Down Latch<br>RESET   |
| 1           | 0  | Loop Power<br>on RESET      |
| 1           | 1  | Loop Power<br>Denial Active |

HC4P5509B  
TOP VIEW



HC-5509B

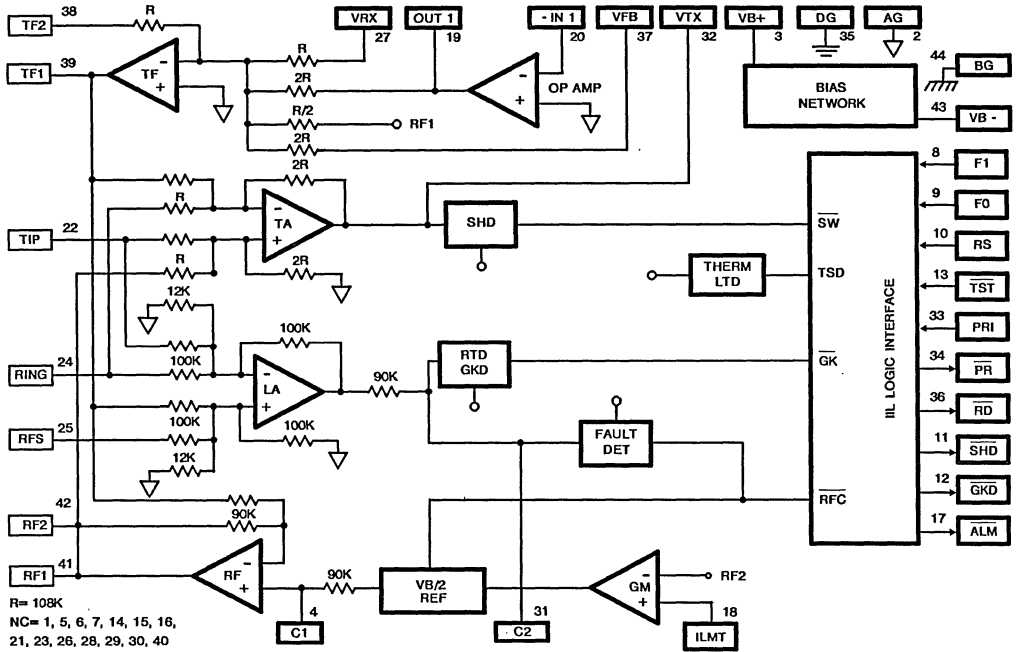
Functional Diagram



DIP OR SOIC

# HC-5509B

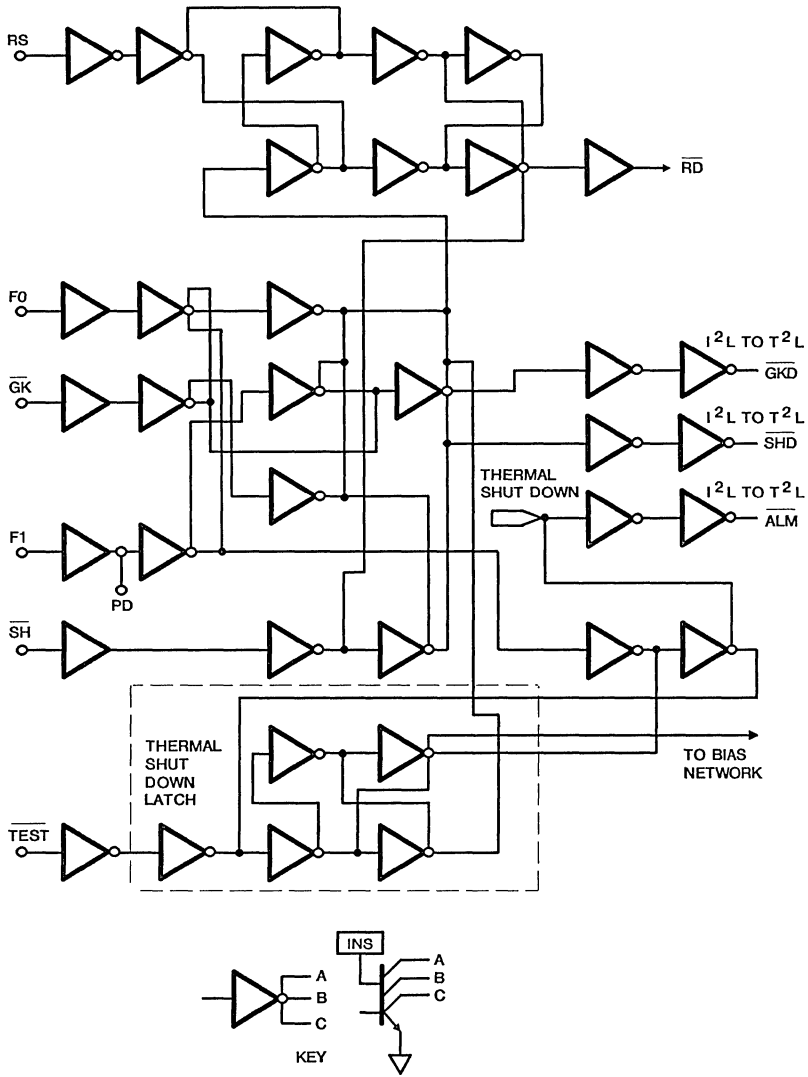
## Functional Diagram



PLCC

# HC-5509B

## Logic Diagram



## Die Characteristics

|                                     |                |               |
|-------------------------------------|----------------|---------------|
| Transistor Count .....              | 224            |               |
| Diode Count .....                   | 28             |               |
| Die Dimensions .....                | 174 x 120 mils |               |
| Substrate Potential .....           | Connected      |               |
| Process .....                       | Bipolar-DI     |               |
| Thermal Constants ( $^{\circ}C/W$ ) | $\theta_{ja}$  | $\theta_{jc}$ |
| Ceramic DIP                         | 48             | 12            |
| Plastic DIP                         | 51             | 21            |
| PLCC                                | 47             | 17            |
| SOIC                                | 72             | 22            |



## Specifications HC-5509B

### Absolute Maximum Ratings (Note 1)

|                                     |                 |
|-------------------------------------|-----------------|
| Relay Drivers .....                 | -0.5V to +15V   |
| Maximum Supply Voltages (VB+) ..... | -0.5V to +7V    |
| (VB+)-(VB-) .....                   | +75V            |
| Storage Temperature Range .....     | -65°C to +150°C |
| Junction Temperature Ceramic .....  | +175°C          |
| Junction Temperature Plastic .....  | +150°C          |

### Recommended Operating Conditions

|                                   |                |
|-----------------------------------|----------------|
| Relay Drivers .....               | +5V to +12V    |
| Positive Power Supply (VB+) ..... | +5V ±5%        |
| Negative Power Supply (VB-) ..... | -42V to -58V   |
| Loop Resistance (RL) .....        | 200Ω to 1750Ω* |
| Operating Temperature Range       |                |
| HC-5509B-5 .....                  | 0°C to +75°C   |
| HC-5509B-9 .....                  | -40°C to +85°C |

\*Note: May Be Extended to 1900Ω With Application Circuit.

### Electrical Specifications

Unless Otherwise Stated, Typical Parameters are at  $T_A = +25^\circ\text{C}$ , Min-Max Parameters are over Operating Temperature Range. VB- = -48V, VB+ = +5V, AG = DG = BG = 0V. All A.C. Parameters are specified at 600Ω 2 wire terminating impedance.

### A.C. Transmission Parameters

| PARAMETER                           | CONDITIONS   | MIN  | TYP   | MAX   | UNITS           |
|-------------------------------------|--|------|-------|-------|-----------------|
| RX Input Impedance                  | 300Hz to 3.4kHz (Note 2)   | -    | 100   | -     | K               |
| TX Output Impedance                 |  | -    | -     | 20    | Ω               |
| 4W Input Overload Level             | 300Hz to 3.4kHz<br>RL = 1200Ω, 600Ω Reference  | +1.5 | -     | -     | V <sub>Pk</sub> |
| 2W Return Loss                      | Matched for 600Ω (Note 2)  |      |       |       |                 |
| SRL LO                              |  | 26   | 35    | -     | dB              |
| ERL                                 |  | 30   | 40    | -     | dB              |
| SRL HI                              |  | 30   | 40    | -     | dB              |
| 2W Longitudinal to Metallic Balance | Per ANSI/IEEE STD 455-1976 (Note 2)  |      |       |       |                 |
| Off Hook                            | 300Hz to 3400Hz  | 58   | 63    | -     | dB              |
| 4W Longitudinal Balance             |  |      |       |       |                 |
| Off Hook                            | 300Hz to 3400Hz (Note 2)   | 50   | 55    | -     | dB              |
| Low Frequency Longitudinal Balance  | R.E.A. Test Circuit  | -    | -     | -67   | dBmp            |
|                                     | I <sub>LINE</sub> = .040A T <sub>A</sub> = +25°C (Note 2)                                | -    | -     | 23    | dBmnc           |
| Longitudinal Current Capability     | I <sub>LINE</sub> = .040A T <sub>A</sub> = +25°C (Note 2)                                | -    | -     | 30    | mArms           |
| Insertion Loss                      | 0dBm at 1kHz, Referenced 600Ω  |      |       |       |                 |
| 2W/4W                               |  | -    | ±0.05 | ±0.2  | dB              |
| 4W/2W                               |  | -    | ±0.05 | ±0.2  | dB              |
| 4W/4W                               |  | -    | -     | ±.12  | dB              |
| Frequency Response                  | 300Hz to 3400Hz (Note 2)<br>Referenced to Absolute<br>Level at 1kHz, 0dBm Referenced 600 | -    | ±0.02 | ±0.05 | dB              |
| Level Linearity                     | Referenced to -10dBm (Note 2)  |      |       |       |                 |
| 2W to 4W and 4W to 2W               | +3 to -40dBm   | -    | -     | ±0.05 | dB              |
|                                     | -40 to -50dBm  | -    | -     | ±0.1  | dB              |
|                                     | -50 to -55dBm  | -    | -     | ±0.3  | dB              |
| Absolute Delay                      | (Note 2)   |      |       |       |                 |
| 2W/4W                               | 300Hz to 3400Hz  | -    | -     | 1     | μs              |
| 4W/2W                               | 300Hz to 3400Hz  | -    | -     | 1     | μs              |
| 4W/4W                               | 300Hz to 3400Hz  | -    | -     | 1.5   | μs              |
| Transhybrid Loss, THL               | (Note 2) See Figure 1  | -    | 40    | -     | dB              |
| Total Harmonic Distortion           | Reference Level 0dBm at 600Ω   |      |       |       |                 |
| 2W/4W, 4W/2W, 4W/4W                 | 300Hz to 3400Hz (Note 2)   | -    | -     | -52   | dB              |
| Idle Channel Noise                  | (Note 2)   |      |       |       |                 |
| 2W and 4W                           | C-Message  | -    | -     | 5     | dBmnc           |
|                                     | Psophometric   | -    | -     | -85   | dBmp            |
|                                     | 3kHz Flat  | -    | -     | 15    | dBm             |

## Specifications HC-5509B

**Electrical Specifications** Unless Otherwise Stated, Typical Parameters are at  $T_A = +25^\circ\text{C}$ , Min-Max Parameters are over Operating Temperature Range.  $V_B^- = -48\text{V}$ ,  $V_B^+ = +5\text{V}$ ,  $AG = DG = BG = 0\text{V}$ . All A.C. Parameters are specified at  $600\Omega$  2 wire terminating impedance.

### A.C. Transmission Parameters (Continued)

| PARAMETERS                   | CONDITIONS                       | MIN | TYP | MAX | UNITS         |
|------------------------------|----------------------------------|-----|-----|-----|---------------|
| Power Supply Rejection Ratio | (Note 2)                         |     |     |     |               |
| VB+ to 2W                    | 30Hz to 200Hz, $R_L = 600\Omega$ | 20  | 29  | -   | dB            |
| VB+ to 4W                    |                                  | 20  | 29  | -   | dB            |
| VB- to 2W                    |                                  | 20  | 29  | -   | dB            |
| VB- to 4W                    |                                  | 20  | 29  | -   | dB            |
| VB+ to 2W                    | 200Hz to 16kHz                   | 30  | -   | -   | dB            |
| VB+ to 4W                    |                                  | 30  | -   | -   | dB            |
| VB- to 2W                    |                                  | 20  | 25  | -   | dB            |
| VB- to 4W                    |                                  | 20  | 25  | -   | dB            |
| Ring Sync Pulse Width        |                                  | 50  | -   | 500 | $\mu\text{s}$ |

### D.C. Parameters

| PARAMETERS                                       | CONDITIONS  | MIN | TYP      | MAX       | UNITS            |
|--|---|-----|----------|-----------|------------------|
| Loop Current Programming                         |   |     |          |           |                  |
| Limit Range                                      |   | 20  | 40       | 60        | mA               |
| Accuracy   |   | 10  | -        | -         | %                |
| Loop Current During Power Denial                 | $R_L = 200\Omega$   | -   | $\pm 3$  | $\pm 5$   | mA               |
| Fault Currents                                   |   |     |          |           |                  |
| TIP to Ground                                    |   | -   | 30       | -         | mA               |
| RING to Ground                                   |   | -   | 60       | -         | mA               |
| TIP and RING to Ground                           |   | -   | 90       | -         | mA               |
| Switch Hook Detection Threshold                  |   | -   | 12       | 15        | mA               |
| Ground Key Detection Threshold                   |   | -   | TBD      | -         | mA               |
| Thermal ALARM Output                             | Safe Operating Die Temperature Exceeded                               | 140 | -        | 160       | $^\circ\text{C}$ |
| Ring Trip Detection Threshold                    | $V_{RING} = 105V_{RMS}$ , $f_{RING} = 20\text{Hz}$                    | -   | TBD      | -         | mA               |
| Ring Trip Detection Period                       |   | -   | 100      | 150       | ms               |
| Dial Pulse Distortion                            |   | -   | 0.1      | 0.5       | ms               |
| Relay Driver Outputs                             | $I_{OL} (PR) = 60\text{mA}$ , $I_{OL} (RD) = 30\text{mA}$             |     |          |           |                  |
| On Voltage $V_{OL}$                              |   | -   | 0.2      | 0.5       | V                |
| Off Leakage Current                              | $V_{OH} = 13.2\text{V}$   | -   | $\pm 10$ | $\pm 100$ | $\mu\text{A}$    |
| TTL/CMOS Logic Inputs<br>(FO, F1, RS, TEST, PRI) |   |     |          |           |                  |
| Logic '0' $V_{IL}$                               |   | -   | -        | 0.8       | V                |
| Logic '1' $V_{IH}$                               |   | 2.0 | -        | 5.5       | V                |
| Input Current<br>(FO, F1, RS, TEST, PRI)         | $0\text{V} \leq V_{IN} \leq 5\text{V}$                                | -   | -        | $\pm 100$ | $\mu\text{A}$    |
| Logic Outputs                                    |   |     |          |           |                  |
| Logic '0' $V_{OL}$                               | $I_{LOAD} = 800\mu\text{A}$   | -   | 0.1      | 0.5       | V                |
| Logic '1' $V_{OH}$                               | $I_{LOAD} = 40\mu\text{A}$  | 2.7 | -        | -         | V                |
| Power Dissipation<br>On Hook                     | Relay Drivers Off   | -   | 200      | -         | mW               |
| $I_{B+}$   | $V_B^+ = +5.25\text{V}$ , $V_B^- = -58\text{V}$ , $R_{LOOP} = \infty$ | -   | -        | 6         | mA               |
| $I_{B-}$   | $V_B^+ = +5.25\text{V}$ , $V_B^- = -58\text{V}$ , $R_{LOOP} = \infty$ | -6  | -        | -         | mA               |

## Specifications HC-5509B

**Electrical Specifications** Unless Otherwise Stated, Typical Parameters are at  $T_A = +25^\circ\text{C}$ , Min-Max Parameters are over Operating Temperature Range.  $V_B = -48\text{V}$ ,  $V_B = +5\text{V}$ ,  $A_G = D_G = B_G = 0\text{V}$ . All A.C. Parameters are specified at  $600\Omega$  2 wire terminating impedance.

### Uncommitted Op Amp Parameters

| PARAMETER                     | CONDITIONS | MIN | TYP      | MAX | UNITS            |
|-------------------------------|------------|-----|----------|-----|------------------|
| Input Offset Voltage          |            | -   | $\pm 5$  | -   | mV               |
| Input Offset Current          |            | -   | $\pm 10$ | -   | nA               |
| Differential Input Resistance | (Note 2)   | -   | 1        | -   | $M\Omega$        |
| Output Voltage Swing          | RL = 10K   | -   | $\pm 3$  | -   | V <sub>p-p</sub> |
| Small Signal GBW              | (Note 2)   | -   | 1        | -   | MHz              |

#### NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterised upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

### Pin Descriptions

| DIP | PLCC | SYMBOL                  | DESCRIPTION  |
|-----|------|-------------------------|--|
| 1   | 2    | AG                      | Analog Ground - To be connected to zero potential. Serves as a reference for the transmit output and receive input terminals.  |
| 2   | 3    | VB+                     | Positive Voltage Source - Most Positive Supply.  |
| 3   | 4    | C1                      | Capacitor #C1 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function.  |
| 4   | 8    | F1                      | Function Address #1 - A TTL and CMOS compatible input used with F0 function address line to externally select logic functions. The three selectable functions are mutually exclusive. See Truth Table on page 1. F1 should be toggled high after power is applied.   |
| 5   | 9    | F0                      | Function Address #0 - A TTL and CMOS compatible input used with F1 function address line to externally select logic functions. The three selectable functions are mutually exclusive. See Truth Table on page 1.   |
| 6   | 10   | RS                      | Ring Synchronization Input - A TTL - compatible clock input. The clock is arranged such that a positive pulse (50 - 500 $\mu\text{s}$ ) occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring delay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to +5.   |
| 7   | 11   | $\overline{\text{SHD}}$ | Switch Hook Detection - An active low LS TTL compatible logic output. A line supervisory output.   |
| 8   | 12   | $\overline{\text{GKD}}$ | Ground Key Detection - An active low LS TTL compatible logic output. A line supervisory output.  |
| 9   | 13   | $\overline{\text{TST}}$ | A TTL logic input. A low on this pin will set a latch and keep the SLIC in a power down mode until the proper F1, F0 state is set and will keep $\overline{\text{ALM}}$ low. See Truth Table on page 1.  |
| 10  | 17   | $\overline{\text{ALM}}$ | A LS TTL compatible active low output which responds to the thermal detector circuit when a safe operating die temperature has been exceeded. When $\overline{\text{TST}}$ is forced low by an external control signal, $\overline{\text{ALM}}$ is latched low until the proper F1, F0 state and $\overline{\text{TST}}$ input is brought high. The $\overline{\text{ALM}}$ can be tied directly to the $\overline{\text{TST}}$ pin to power down the part when a thermal fault is detected and then reset with F0, F1. See Truth Table on page 1. It is possible to ignore transient thermal overload conditions in the SLIC by delaying the response to the $\overline{\text{TST}}$ pin from the $\overline{\text{ALM}}$ . Care must be exercised in attempting this as continued thermal overstress may reduced component life. |
| 11  | 18   | ILMT                    | Loop Current Limit - Voltage on this pin sets the short loop current limiting conditions using a resistive voltage divider.  |
| 12  | 19   | OUT1                    | The analog output of the spare operational amplifier.  |
| 13  | 20   | -IN1                    | The inverting analog input of the spare operational amplifier.   |
| 14  | 22   | TIP                     | An analog input connected to the TIP (more positive) side of the subscriber loop through a feed resistor and ring relay contact. Functions with the RING terminal to receive voice signals from the telephone and for loop monitoring purpose.   |

## HC-5509B

### Pin Descriptions (Continued)

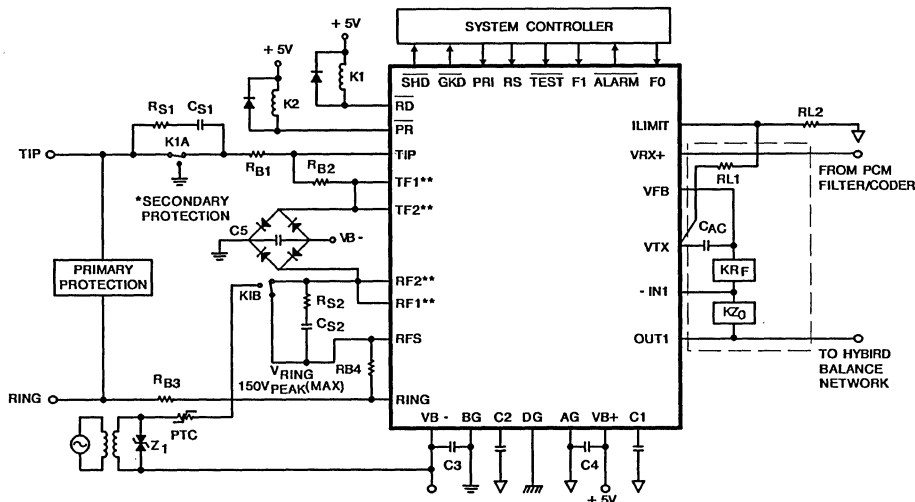
| DIP | PLCC   | SYMBOL          | DESCRIPTION  |
|-----|--|-----------------|--|
| 15  | 24   | RING            | An analog input connected to the RING (more negative) side of the subscriber loop through a feed resistor. Functions with the TIP terminal to receive voice signals from the telephone and for loop monitoring purposes.   |
| 16  | 25   | RFS             | Ring Feed Sense - Senses RING side of the loop for Ground Key Detection. During Ring injected ringing the ring signal at this node is isolated from RF via the ring relay. For Tip injected ringing, the RF and RFS pins must be shorted.  |
| 17  | 27   | VRX             | Receive Input, Four Wire Side - A high impedance analog input. A.C. signals appearing at this input drive the Tip Feed and Ring Feed amplifiers differentially.  |
| 18  | 31   | C2              | Capacitor #2 - An external capacitor to be connected between this terminal and ground. It prevents false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from power lines and other noise sources. This capacitor should be nonpolarized.   |
| 19  | 32   | VTX             | Transmit Output, Four Wire Side - A low impedance analog output which represents the differential voltage across TIP and RING. Transhybrid balancing must be performed beyond this output to completely implement two to four wire conversion. This output is referenced to analog ground. Since the D.C. level of this output varies with loop current, capacitive coupling to the next stage is necessary. |
| 20  | 33   | PRI             | A TTL compatible input used to control $\overline{PR}$ . PRI active High = $\overline{PR}$ active low.   |
| 21  | 34   | $\overline{PR}$ | An active low open collector output. Can be used to drive a Polarity Reversal Relay.   |
| 22  | 35   | DG              | Digital Ground - To be connected to zero potential. Serves as a reference for all digital inputs and outputs on the SLIC.  |
| 23  | 36   | $\overline{RD}$ | Ring Relay Driver - An active low open collector output. Used to drive a relay that switches ringing signals onto the 2 wire line.   |
| 24  | 37   | VFB             | Feedback signal from the tip feed amplifier. To be used in conjunction with transmit output signal and the spare op-amp to accommodate 2W line impedance matching.   |
| 25  | 38   | TF2             | Tip Feed - A low impedance analog output connected to the TIP terminal through a feed resistor. Functions with the RF terminal to provide loop current, and to feed voice signals to the telephone set and to sink longitudinal currents. Must be tied to TF1.   |
| NA  | 39   | TF1             | Tie directly to TF2 in the PLCC application.   |
| 26  | 41   | RF1             | Ring Feed - A low impedance analog output connected to the RING terminal through a feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and to sink longitudinal currents. Tie directly to RF2.   |
| NA  | 42   | RF2             | Tie directly to RF1 in the PLCC application.   |
| 27  | 43   | VB-             | The battery voltage source. The most negative supply.  |
| 28  | 44   | BG              | Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.   |
|     | 5, 6, 7,<br>1, 21,<br>26, 23,<br>30, 28,<br>29, 40,<br>14, 15,<br>16 | NC              | No internal connection.  |

NOTE: All grounds (AG, BG, DG) must be applied before VB+ or VB-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

# HC-5509B

## Applications Diagram 1

TYPICAL LINE CIRCUIT APPLICATION WITH THE HC-5509B



### TYPICAL COMPONENT VALUES

C1 = 0.5 $\mu$ F, 30V  
 C2 = 0.5 $\mu$ F-1.0 $\mu$ F  $\pm$ 10%, 20V (Should be nonpolarized)  
 C3 = 0.01 $\mu$ F, 100V  $\pm$ 20%  
 C4 = 0.01 $\mu$ F, 100V  $\pm$ 20%  
 C5 = 0.01 $\mu$ F, 100V  $\pm$ 20%

CAC = 0.5 $\mu$ F, 20V  
 KZ0 = 60K, (Z0 = 600 $\Omega$ , K = Scaling Factor = 100)

RL1, RL2; Current Limit Setting Resistors

RL1 + RL2 > 90k $\Omega$

ILIMIT = (0.6) (RL1 + RL2)/(200 x RL2), RL1 typically 100k $\Omega$

KRf = 20K, Rf = 2(RB2 + RB4), K = Scaling Factor = 100

RB1 = RB2 = RB3 = RB4 = 50 $\Omega$  (1% absolute, matching requirements covered in a Tech Brief)

RS1 = RS2 = 1k $\Omega$  typically

CS1 = CS2 = 0.1 $\mu$ F, 200V typically, depending on VRing and line length.

Z1 = 150V to 200V transient protector. PTC used as ring generator ballast.

\* Secondary protection diode bridge recommended is 3A, 200V type.

\*\* TF1, TF2 and RF1, RF2 are on PLCC only and should be connected together as shown.

NOTE: HC-5509B Applications Diagram shows Ring injected ringing configuration. A Balanced or Tip injected configuration may also be used.

## Overvoltage Protection Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 2.

The SLIC will withstand longitudinal currents up to a maximum of 30mArms, 15mArms per leg, without any performance degradation.

TABLE 2.

| PARAMETER                         | TEST CONDITION            | PERFORMANCE (MAX)    | UNITS  |
|-----------------------------------|---------------------------|----------------------|--------|
| Longitudinal Surge                | 10 $\mu$ s Rise/          | $\pm$ 1000 (Plastic) | Vp-p   |
|                                   | 1000 $\mu$ s/Fall         | $\pm$ 500 (Ceramic)  | Vp-p   |
| Metallic Surge                    | 10 $\mu$ s Rise/          | $\pm$ 1000 (Plastic) | Vp-p   |
|                                   | 1000 $\mu$ s Fall         | $\pm$ 500 (Ceramic)  | Vp-p   |
| T/GND<br>R/GND                    | 10 $\mu$ s Rise/          | $\pm$ 1000 (Plastic) | Vp-p   |
|                                   | 1000 $\mu$ s Fall         | $\pm$ 500 (Ceramic)  | Vp-p   |
| 50/60Hz Current<br>T/GND<br>R/GND | 700Vrms Limited to 10Arms | 11 (Plastic)         | Cycles |

August 1991

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- 2W/4W, 4W/2W Hybrid

### Description

The HC-5524 telephone Subscriber Line Interface Circuit integrates most of the BORSCHT functions on a monolithic IC. The device is manufactured in a Dielectric Isolation (DI) process and is designed for use as a 24V interface between the traditional telephone subscriber pair (Tip and Ring) and the low voltage filtering and coding/decoding functions of the line card. Together with a secondary protection diode bridge, the device will withstand 500V induced surges, in plastic packages. The SLIC also maintains specified transmission performance in the presence of externally induced longitudinal currents. The BORSCHT functions that the SLIC provides are:

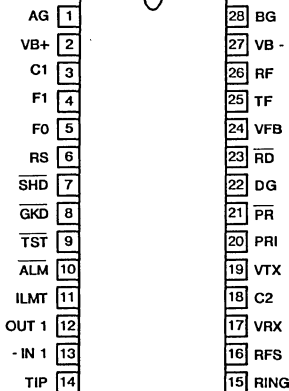
- Battery Feed with Subscriber Loop Current Limiting
- Overvoltage Protection
- Ring Relay Driver
- Supervisory Signaling Functions
- Hybrid Functions (with External Op-Amp)
- Test (or Battery Reversal) Relay Driver

In addition, the SLIC provides selective denial of power to subscriber loops, a programmable subscriber loop current limit from 20 to 60mA, a thermal shutdown with an alarm output and line fault protection. Switch hook detection, ring trip detection and ground key detection functions are also incorporated in the SLIC device.

The HC-5524 SLIC is available in a 28 pin Dual-in-Line Ceramic or Plastic package, a 44 pin Plastic Leaded Chip Carrier, or in a 28 Pin SOIC. It is ideally suited for line card designs in PBX and DLC systems, replacing traditional transformer solutions.

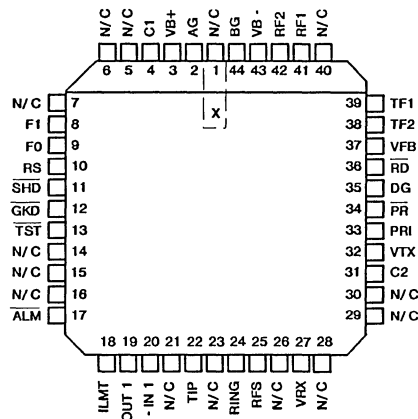
### Pinouts

HC1-5524, HC3-5524,  
& HC9P5524  
TOP VIEW



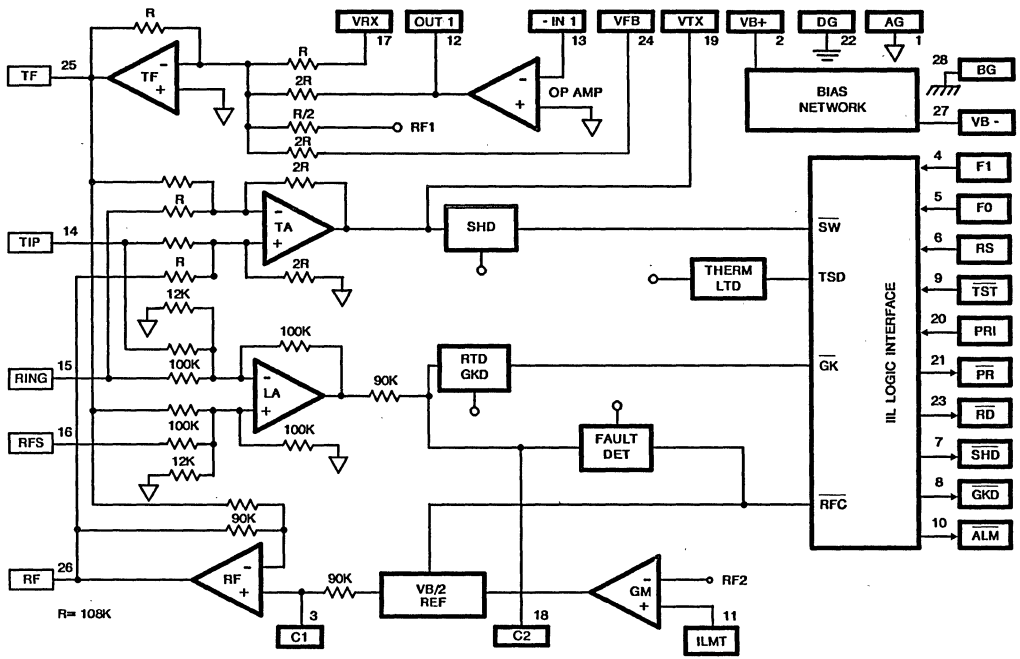
| TRUTH TABLE |    |                          |
|-------------|----|--------------------------|
| F1          | FO | Action                   |
| 0           | 0  | Normal Loop Feed         |
| 0           | 1  | RD Active                |
| 1           | 0  | Power Down Latch RESET   |
| 1           | 0  | Power on RESET           |
| 1           | 1  | Loop Power Denial Active |

HC4P5524  
TOP VIEW



# HC-5524

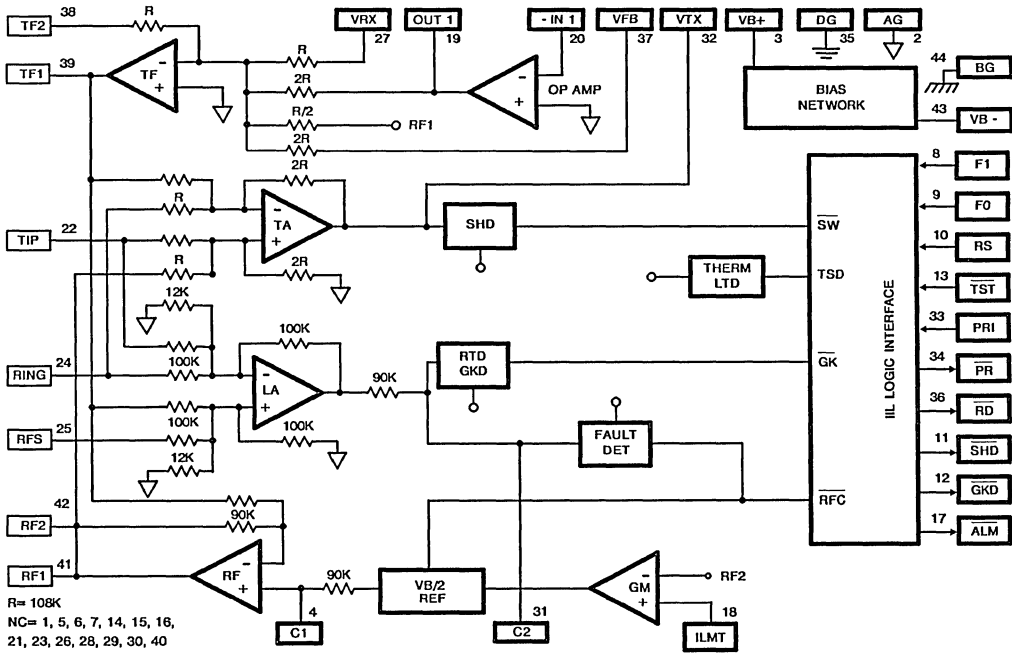
## Functional Diagram



DIP OR SOIC

# HC-5524

## Functional Diagram

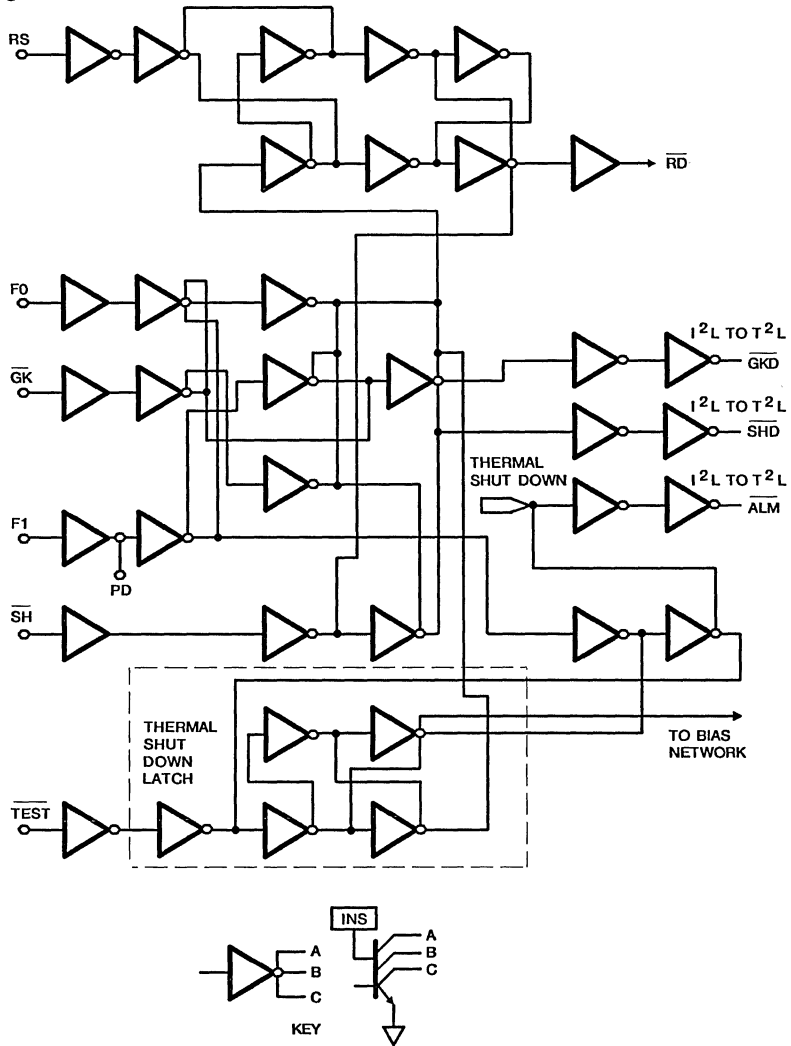


PLCC



# HC-5524

## Logic Diagram



## Die Characteristics

|                           |                             |
|---------------------------|-----------------------------|
| Transistor Count .....    | 224                         |
| Diode Count .....         | 28                          |
| Die Dimensions .....      | 174 x 120 mils              |
| Substrate Potential ..... | Connected                   |
| Process .....             | Bipolar-DI                  |
| Thermal Constants (°C/W)  | $\theta_{ja}$ $\theta_{jc}$ |
| Ceramic DIP               | 48      12                  |
| Plastic DIP               | 51      21                  |
| PLCC                      | 47      17                  |
| SOIC                      | 72      22                  |

## Specifications HC-5524

### Absolute Maximum Ratings (Note 1)

|                                     |                 |
|-------------------------------------|-----------------|
| Relay Drivers .....                 | -0.5V to +15V   |
| Maximum Supply Voltages (VB+) ..... | -0.5V to +7V    |
| (VB+)-(VB-) .....                   | +40V            |
| Storage Temperature Range .....     | -65°C to +150°C |
| Junction Temperature Ceramic .....  | +175°C          |
| Junction Temperature Plastic .....  | +150°C          |

### Recommended Operating Conditions

|                                   |                |
|-----------------------------------|----------------|
| Relay Drivers .....               | +5V to +12V    |
| Positive Power Supply (VB+) ..... | +5V ±5%        |
| Negative Power Supply (VB-) ..... | -20V to -28V   |
| Operating Temperature Range       |                |
| HC-5524-5 .....                   | 0°C to +75°C   |
| HC-5524-9 .....                   | -40°C to +85°C |

**Electrical Specifications** Unless Otherwise Stated, Typical Parameters are at  $T_A = +25^\circ\text{C}$ ,  $V_{B+} = +5\text{V}$ ,  $V_{B-} = -24\text{V}$ ,  $AG = DG = BG = 0\text{V}$ . Min-Max Parameters are Over Operating Positive and Negative Battery Voltages and Over the Industrial Temperature Range. All Parameters are Specified at 600Ω 2-Wire Terminating Impedance.

### A.C. Transmission Parameters

| PARAMETER   | CONDITIONS   | MIN  | TYP   | MAX   | UNITS           |
|---|--|------|-------|-------|-----------------|
| RX Input Impedance  | 300Hz to 3.4kHz (Note 2)   | -    | 100   | -     | K               |
| TX Output Impedance                                       |  | -    | -     | 20    | Ω               |
| 4W Input Overload Level                                   | 300Hz to 3.4kHz, 600Ω Reference  | +1.0 | -     | -     | V <sub>Pk</sub> |
| 2W Return Loss  | Matched for 600Ω (Note 2)  |      |       |       |                 |
| SRL LO  |  | 26   | 35    | -     | dB              |
| ERL   |  | 30   | 40    | -     | dB              |
| SRL HI  |  | 30   | 40    | -     | dB              |
| 2W Longitudinal to Metallic Balance                       | Per ANSI/IEEE STD 455-1976 (Note 2)  |      |       |       |                 |
| Off Hook  | 300Hz to 3400Hz  | 58   | 63    | -     | dB              |
| 4W Longitudinal Balance                                   |  |      |       |       |                 |
| Off Hook  | 300Hz to 3400Hz (Note 2)   | 50   | 55    | -     | dB              |
| Low Frequency Longitudinal Balance                        | R.E.A. Test Circuit  | -    | -80   | -67   | dBmp            |
|   | I <sub>LINE</sub> = 40mA T <sub>A</sub> = +25°C (Note 2)                                 | -    | 10    | 23    | dBrc            |
| Longitudinal Current Capability                           | I <sub>LINE</sub> = 40mA T <sub>A</sub> = +25°C (Note 2)                                 | -    | -     | 40    | mArms           |
| Insertion Loss  |  |      |       |       |                 |
| 2W/4W   | -1.58dBm @ 1kHz, Referenced 600Ω   | -    | ±0.05 | ±0.2  | dB              |
| 4W/2W   | 0dBm @ 1kHz, Referenced 600Ω   | -    | ±0.05 | ±0.2  | dB              |
| 4W/4W   | -1.58dBm @ 1kHz, Referenced 600Ω   | -    | -     | ±0.2  | dB              |
| Frequency Response  | 300Hz to 3400Hz (Note 2)<br>Referenced to Absolute<br>Level at 1kHz, 0dBm Referenced 600 | -    | ±0.02 | ±0.06 | dB              |
| Level Linearity   | Referenced to -10dBm (Note 2)  |      |       |       |                 |
| 2W to 4W and 4W to 2W                                     | +3 to -40dBm   | -    | -     | ±0.08 | dB              |
|   | -40 to -50dBm  | -    | -     | ±0.12 | dB              |
|   | -50 to -55dBm  | -    | -     | ±0.3  | dB              |
| Absolute Delay  | (Note 2)   |      |       |       |                 |
| 2W/4W   | 300Hz to 3400Hz  | -    | -     | 1     | μs              |
| 4W/2W   | 300Hz to 3400Hz  | -    | -     | 1     | μs              |
| 4W/4W   | 300Hz to 3400Hz  | -    | 0.95  | 1.5   | μs              |
| Total Harmonic Distortion                                 | Reference Level 0dBm at 600Ω   |      |       |       |                 |
| 2W/4W, 4W/2W, 4W/4W                                       | 300Hz to 3400Hz (Note 2)   | -    | -     | -50   | dB              |
| Idle Channel Noise  | (Note 2)   |      |       |       |                 |
| 2W and 4W   | C-Message  | -    | -     | 5     | dBrc            |
|   | Psophometric   | -    | -     | -85   | dBmp            |
|   | 3kHz Flat  | -    | -     | 16    | dBm             |
| Open Loop Voltage (V <sub>TIP</sub> - V <sub>RING</sub> ) | V <sub>B+</sub> = +5V, V <sub>B-</sub> = -24V  |      | 15.8  |       | V               |

## Specifications HC-5524

**Electrical Specifications** Unless Otherwise Stated, Typical Parameters are at  $T_A = +25^\circ\text{C}$ ,  $V_{B+} = +5\text{V}$ ,  $V_{B-} = -24\text{V}$ ,  $A_G = D_G = B_G = 0\text{V}$ . Min-Max Parameters are Over Operating Positive and Negative Battery Voltages and Over the Industrial Temperature Range. All Parameters are Specified at  $600\Omega$  2-Wire Terminating Impedance.

### A.C. Transmission Parameters (Continued)

| PARAMETERS                   | CONDITIONS                       | MIN | TYP | MAX | UNITS         |
|------------------------------|----------------------------------|-----|-----|-----|---------------|
| Power Supply Rejection Ratio | (Note 2)                         |     |     |     |               |
| $V_{B+}$ to 2W               | 30Hz to 200Hz, $R_L = 600\Omega$ | 20  | 40  | -   | dB            |
| $V_{B+}$ to 4W               |                                  | 20  | 40  | -   | dB            |
| $V_{B-}$ to 2W               |                                  | 20  | 40  | -   | dB            |
| $V_{B-}$ to 4W               |                                  | 20  | 50  | -   | dB            |
| $V_{B+}$ to 2W               | 200Hz to 16kHz                   | 30  | 40  | -   | dB            |
| $V_{B+}$ to 4W               |                                  | 20  | 28  | -   | dB            |
| $V_{B-}$ to 2W               |                                  | 20  | 50  | -   | dB            |
| $V_{B-}$ to 4W               |                                  | 20  | 50  | -   | dB            |
| Ring Sync Pulse Width        |                                  | 50  | -   | 500 | $\mu\text{s}$ |

### D.C. Parameters

| PARAMETERS  | CONDITIONS  | MIN | TYP      | MAX       | UNITS            |
|---|---|-----|----------|-----------|------------------|
| Loop Current Programming                                      |   |     |          |           |                  |
| Limit Range   |   | 20  | 40       | 60        | mA               |
| Accuracy  |   | 10  | -        | -         | %                |
| Loop Current During Power Denial                              | $R_L = 200\Omega$   |     | $\pm 4$  | $\pm 7$   | mA               |
| Fault Currents  |   |     |          |           |                  |
| TIP to Ground   |   | -   | 30       | -         | mA               |
| RING to Ground  |   | -   | 120      | -         | mA               |
| TIP and RING to Ground  |   | -   | 150      | -         | mA               |
| Switch Hook Detection Threshold                               |   | -   | 12       | 15        | mA               |
| Ground Key Detection Threshold                                |   | -   | TBD      | -         | mA               |
| Thermal ALM Output  | Safe Operating Die Temperature Exceeded                                       | 140 | -        | 160       | $^\circ\text{C}$ |
| Ring Trip Detection Threshold                                 | $V_{RING} = 105V_{RMS}$ , $f_{RING} = 20\text{Hz}$                            | -   | TBD      | -         | mA               |
| Ring Trip Detection Period                                    |   | -   | 100      | 150       | ms               |
| Dial Pulse Distortion   |   | -   | 0.1      | 0.5       | ms               |
| Relay Driver Outputs  | $I_{OL}(\overline{PR}) = 60\text{mA}$ , $I_{OL}(\overline{RD}) = 30\text{mA}$ |     |          |           |                  |
| On Voltage $V_{OL}$   |   | -   | 0.2      | 0.5       | V                |
| Off Leakage Current   | $V_{OH} = 13.2\text{V}$   | -   | $\pm 10$ | $\pm 100$ | $\mu\text{A}$    |
| TTL/CMOS Logic Inputs<br>(F0, F1, RS, $\overline{TST}$ , PRI) |   |     |          |           |                  |
| Logic '0' $V_{IL}$  |   | -   | -        | 0.8       | V                |
| Logic '1' $V_{IH}$  |   | 2.0 | -        | 5.5       | V                |
| Input Current<br>(F0, F1, RS, $\overline{TST}$ , PRI)         | $0\text{V} \leq V_{IN} \leq 5\text{V}$  | -   | -        | $\pm 100$ | $\mu\text{A}$    |
| Logic Outputs   |   |     |          |           |                  |
| Logic '0' $V_{OL}$  | $I_{LOAD} = 800\mu\text{A}$   | -   | 0.1      | 0.5       | V                |
| Logic '1' $V_{OH}$  | $I_{LOAD} = 40\mu\text{A}$  | 2.7 | -        | -         | V                |
| Power Dissipation<br>On Hook                                  | Relay Drivers Off   | -   | 60       | -         | mW               |
| $I_{B+}$  | $V_{B+} = +5.25\text{V}$ , $V_{B-} = -28\text{V}$ , $R_{LOOP} = \infty$       | -   | -        | 4         | mA               |
| $I_{B-}$  | $V_{B+} = +5.25\text{V}$ , $V_{B-} = -28\text{V}$ , $R_{LOOP} = \infty$       | -4  | -        | -         | mA               |
| $I_{B+}$  | $V_{B+} = +5\text{V}$ , $V_{B-} = -24\text{V}$ , $R_{LOOP} = 600\Omega$       | -   | 3        | 6         | mA               |
| $I_{B-}$  | $V_{B+} = +5\text{V}$ , $V_{B-} = -24\text{V}$ , $R_{LOOP} = 600\Omega$       | -28 | -24      | -         | mA               |

## Specifications HC-5524

**Electrical Specifications** Unless Otherwise Stated, Typical Parameters are at  $T_A = +25^{\circ}\text{C}$ ,  $V_{B+} = +5\text{V}$ ,  $V_{B-} = -24\text{V}$ ,  $AG = DG = BG = 0\text{V}$ . Min-Max Parameters are Over Operating Positive and Negative Battery Voltages and Over the Industrial Temperature Range. All Parameters are Specified at  $600\Omega$  2-Wire Terminating Impedance.

### Uncommitted Op Amp Parameters

| PARAMETER                     | CONDITIONS        | MIN | TYP      | MAX | UNITS     |
|-------------------------------|-------------------|-----|----------|-----|-----------|
| Input Offset Voltage          |                   | -   | $\pm 5$  | -   | mV        |
| Input Offset Current          |                   | -   | $\pm 10$ | -   | nA        |
| Differential Input Resistance | (Note 2)          | -   | 1        | -   | $M\Omega$ |
| Output Voltage Swing          | $RL = 10\text{K}$ | -   | $\pm 3$  | -   | $V_{p-p}$ |
| Small Signal GBW              | (Note 2)          | -   | 1        | -   | MHz       |

#### NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

### Pin Descriptions

| DIP | PLCC | SYMBOL                  | DESCRIPTION   |
|-----|------|-------------------------|---|
| 1   | 2    | AG                      | Analog Ground - To be connected to zero potential. Serves as a reference for the transmit output and receive input terminals.   |
| 2   | 3    | VB+                     | Positive Voltage Source - Most Positive Supply.   |
| 3   | 4    | C1                      | Capacitor #C1 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function.   |
| 4   | 8    | F1                      | Function Address #1 - A TTL and CMOS compatible input used with F0 function address line to externally select logic functions. The three selectable functions are mutually exclusive. See Truth Table on page 1. F1 should be toggled high after power is applied.  |
| 5   | 9    | F0                      | Function Address #0 - A TTL and CMOS compatible input used with F1 function address line to externally select logic functions. The three selectable functions are mutually exclusive. See Truth Table on page 1.  |
| 6   | 10   | RS                      | Ring Synchronization Input - A TTL - compatible clock input. The clock is arranged such that a positive pulse (50 - 500 $\mu\text{s}$ ) occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring delay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to +5.  |
| 7   | 11   | $\overline{\text{SHD}}$ | Switch Hook Detection - An active low LS TTL compatible logic output. A line supervisory output.  |
| 8   | 12   | $\overline{\text{GKD}}$ | Ground Key Detection - An active low LS TTL compatible logic output. A line supervisory output.   |
| 9   | 13   | $\overline{\text{TST}}$ | A TTL logic input. A low on this pin will set a latch and keep the SLIC in a power down mode until the proper F1, F0 state is set and will keep $\overline{\text{ALM}}$ low. See Truth Table on page 1.   |
| 10  | 17   | $\overline{\text{ALM}}$ | A LS TTL compatible active low output which responds to the thermal detector circuit when a safe operating die temperature has been exceeded. When $\overline{\text{TST}}$ is forced low by an external control signal, $\overline{\text{ALM}}$ is latched low until the proper F1, F0 state and $\overline{\text{TST}}$ input is brought high. The $\overline{\text{ALM}}$ can be tied directly to the $\overline{\text{TST}}$ pin to power down the part when a thermal fault is detected and then reset with F0, F1. See Truth Table on page 1. It is possible to ignore transient thermal overload conditions in the SLIC by delaying the response to the $\overline{\text{TST}}$ pin from the $\overline{\text{ALM}}$ . Care must be exercised in attempting this as continued thermal overstress may reduce component life. |
| 11  | 18   | ILMT                    | Loop Current Limit - Voltage on this pin sets the short loop current limiting conditions using a resistive voltage divider.   |
| 12  | 19   | OUT1                    | The analog output of the spare operational amplifier.   |
| 13  | 20   | -IN1                    | The inverting analog input of the spare operational amplifier.  |
| 14  | 22   | TIP                     | An analog input connected to the TIP (more positive) side of the subscriber loop through a feed resistor and ring relay contact. Functions with the RING terminal to receive voice signals from the telephone and for loop monitoring purposes.   |

**Pin Descriptions (Continued)**

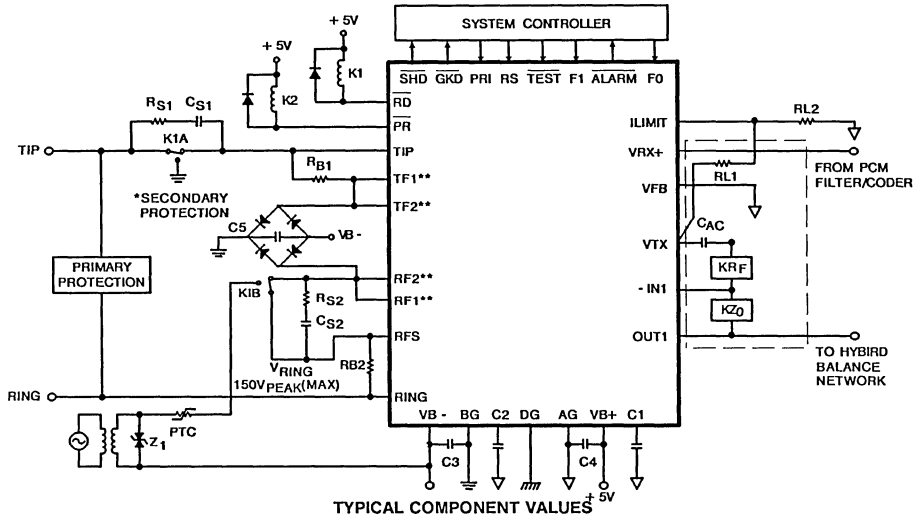
| DIP | PLCC   | SYMBOL          | DESCRIPTION   |
|-----|--|-----------------|---|
| 15  | 24   | RING            | An analog input connected to the RING (more negative) side of the subscriber loop through a feed resistor. Functions with the TIP terminal to receive voice signals from the telephone and for loop monitoring purposes.  |
| 16  | 25   | RFS             | Ring Feed Sense - Senses RING side of the loop for Ground Key Detection. During Ring injected ringing the ring signal at this node is isolated from RF via the ring relay. For Tip injected ringing, the RF and RFS pins must be shorted.   |
| 17  | 27   | VRX             | Receive Input, Four Wire Side - A high impedance analog input. A.C. signals appearing at this input drive the Tip Feed and Ring Feed amplifiers differentially.   |
| 18  | 31   | C2              | Capacitor #2 - An external capacitor to be connected between this terminal and ground. It prevents false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from power lines and other noise sources. This capacitor should be nonpolarized.  |
| 19  | 32   | VTX             | Transmit Output, Four Wire Side - A low impedance analog output which represents the differential voltage across TIP and RING Transhybrid balancing must be performed beyond this output to completely implement two to four wire conversion. This output is referenced to analog ground. Since the D.C. level of this output varies with loop current, capacitive coupling to the next stage is necessary. |
| 20  | 33   | PRI             | A TTL compatible input used to control $\overline{PR}$ . PRI active High = $\overline{PR}$ active low.  |
| 21  | 34   | $\overline{PR}$ | An active low open collector output. Can be used to drive a Polarity Reversal Relay.  |
| 22  | 35   | DG              | Digital Ground - To be connected to zero potential. Serves as a reference for all digital inputs and outputs on the SLIC.   |
| 23  | 36   | $\overline{RD}$ | Ring Relay Driver - An active low open collector output. Used to drive a relay that switches ringing signals onto the 2 wire line.  |
| 24  | 37   | VFB*            | Feedback input to the tip feed amplifier may be used in conjunction with transmit output signal and the spare op-amp to accommodate 2W line impedance matching. (This is not used in the typical applications circuit on page 8.)   |
| 25  | 38   | TF2             | Tip Feed - A low impedance analog output connected to the TIP terminal through a feed resistor. Functions with the RF terminal to provide loop current, and to feed voice signals to the telephone set and to sink longitudinal currents. Must be tied to TF1.  |
| NA  | 39   | TF1             | Tie directly to TF2 in the PLCC application.  |
| 26  | 41   | RF1             | Ring Feed - A low impedance analog output connected to the RING terminal through a feed resistor. Functions with the TF terminal to provide loop current, feed voice signals to the telephone set, and to sink longitudinal currents. Tie directly to RF2.  |
| NA  | 42   | RF2             | Tie directly to RF1 in the PLCC application.  |
| 27  | 43   | VB-             | The battery voltage source. The most negative supply.   |
| 28  | 44   | BG              | Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.  |
|     | 5, 6, 7,<br>1, 21,<br>26, 23,<br>30, 28,<br>29, 40,<br>14, 15,<br>16 | NC              | No internal connection.   |

NOTE: All grounds (AG, BG, DG) must be applied before VB+ or VB-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

\* Although not used in the typical applications circuit, VFB may be used in matching complex 2-wire impedances.

Applications Diagram 1

TYPICAL LINE CIRCUIT APPLICATION WITH THE HC-5524



TYPICAL COMPONENT VALUES

- C1 = 0.5µF, 20V
- C2 = 0.5µF-1.0µF ±10%, 50V (Should be nonpolarized)
- C3 = 0.01µF, 50V ±20%
- C4 = 0.01µF, 50V ±20%
- C5 = 0.01µF, 50V ±20%
- CAC = 0.5µF, 20V
- KZ0 = 50K, (Z0 = 600Ω, K = Scaling Factor = 100)
- RL1, RL2; Current Limit Setting Resistors
- RL1+RL2 > 90kΩ
- ILIMIT = (.6) (RL1+RL2)/(RL2X200), RL1 typically 100kΩ
- KRF = 20K, RF = 2(RB1+RB2), K = Scaling Factor = 100)

- RB1 = RB2 = 50Ω (1% absolute, matching requirements covered in a Tech Brief)
- RS1 = RS2 = 1kΩ typically
- CS1 = CS2 = 0.1µF, 200V typically, depending on VRING and line length.
- Z1 = 150V to 200V transient protector. PTC used as ring generator ballast.
- \* Secondary protection diode bridge recommended is 3A, 200V type.
- \*\* TF1, TF2 and RF1, RF2 are on PLCC only and should be connected together as shown.

NOTE: HC-5524 Applications Diagram shows Ring injected ringing configuration. A Balanced or Tip injected configuration may also be used.

**Overvoltage Protection  
Longitudinal Current Protection**

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

High voltage surge conditions are as specified in Table 2.

The SLIC will withstand longitudinal currents up to a maximum of 40mArms, 20mArms per leg, without any performance degradation.

NOTE: Overvoltage, Surge Condition Limits, listed in Table 2, may be increased with use of additional secondary protection to Tip & Ring.

TABLE 2.

| PARAMETER                         | TEST CONDITION            | PERFORMANCE (MAX) | UNITS  |
|-----------------------------------|---------------------------|-------------------|--------|
| Longitudinal Surge                | 10µs Rise/                | ±500 (Plastic)    | Vp-p   |
|                                   | 1000µs/Fall               | ±250 (Ceramic)    | Vp-p   |
| Metallic Surge                    | 10µs Rise/                | ±500 (Plastic)    | Vp-p   |
|                                   | 1000µs Fall               | ±250 (Ceramic)    | Vp-p   |
| T/GND<br>R/GND                    | 10µs Rise/                | ±500 (Plastic)    | Vp-p   |
|                                   | 1000µs Fall               | ±250 (Ceramic)    | Vp-p   |
| 50/60Hz Current<br>T/GND<br>R/GND | 350Vrms Limited to 10Arms | 11 (Plastic)      | Cycles |

August 1991

**PCM Transcoder**

### Features

- Single 5V Supply ..... 10mA Typ.
- Mode Selectable Coding Including:
  - ▶ AMI (T1, T1C)
  - ▶ B8ZS (T1)
  - ▶ HDB3 (PCM30)
- North American and European Compatibility
- Simultaneous Encoding and Decoding
- Asynchronous Operation
- Loop Back Control
- Transmission Error Detection
- Alarm Indication Signal
- Replaces MJ1440, MJ1471 and TCM2201 Transcoders

### Applications

- North American and European PCM Transmission Lines where Pseudo Ternary Line Code Substitution Schemes are Desired
- Any Equipment that Interfaces T1, T1C, T2 or PCM30 Lines Including Multiplexers, Channel Service Units, (CSUs) Echo Cancellers, Digital Cross-Connects (DSXs), T1 Compressors, etc.

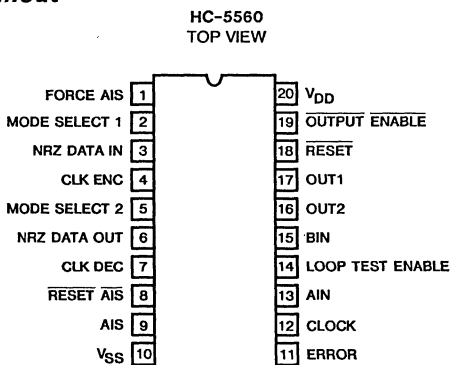
### Description

The HC-5560 digital line transcoder provides encoding and decoding of pseudo ternary line code substitution schemes. Unlike other industry standard transcoders, the HC-5560 provides four worldwide compatible mode selectable code substitution schemes, including HDB3 (High Density Bipolar 3), B6ZS, B8ZS (Bipolar with 6 or 8 Zero Substitution) and AMI (Alternate Mark Inversion).

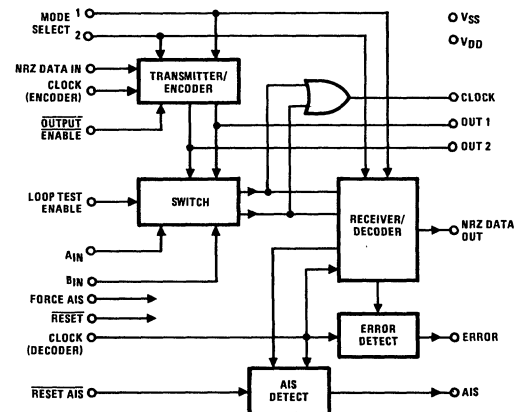
The HC-5560 is fabricated in CMOS and operates from a single 5V supply. All inputs and outputs are TTL compatible. The HC-5560 is available in 20 pin dual-in-line plastic packages over the commercial temperature range, 0°C to +70°C.

Application Note #573, "The HC-5560 Digital Line Transcoder," by D.J. Donovan is available.

### Pinout



### Functional Diagram



## Functional Description

The HC-5560 TRANSCODER can be divided into six sections: transmission (coding), reception (decoding), error detection, all ones detection, testing functions, and output controls.

The transmitter codes a non-return to zero (NRZ) binary unipolar input signal (NRZ Data In) into two binary unipolar return to zero (RZ) output signals (Out 1, Out 2). These output signals represent the NRZ data stream modified according to the selected encoding scheme (i.e., AMI, B8ZS, B6ZS, HDB3) and are externally mixed together (usually via a transistor or transformer network) to create a ternary bipolar signal for driving transmission lines.

The receiver accepts as its input the ternary data from the transmission line that has been externally split into two binary unipolar return to zero signals ( $A_{in}$  and  $B_{in}$ ). These signals are decoded, according to the rules of the selected line code into one binary unipolar NRZ output signal (NRZ Data Out).

The encoder and decoder sections of the chip perform independently (excluding loopback condition) and may operate simultaneously.

The Error output signal is active high for one cycle of CLK DEC upon the detection of any bipolar violation in the received  $A_{in}$  and  $B_{in}$  signals that is not part of the selected line coding scheme. The bipolar violation is not removed, however, and shows up as a pulse in the NRZ Data Out signal. In addition, the Error output signal monitors the received  $A_{in}$  and  $B_{in}$  signals for a string of zeros that violates the maximum consecutive zeros allowed for the selected line coding scheme

(i.e., 15 for AMI, 8 for B8ZS, 6 for B6ZS, and 4 for HDB3). In the event that an excessive amount of zeros is detected, the Error output signal will be active high for one cycle of CLK DEC during the zero that exceeds the maximum number. In the case that a high level should simultaneously appear on both received input signals  $A_{in}$  and  $B_{in}$  a logical one is assumed and appears on the NRZ Data Out stream with the Error output active.

An input signal received at inputs  $A_{in}$  and  $B_{in}$  that consists of all ones (or marks) is detected and signaled by a high level at the Alarm Indication Signal (AIS) output. This is also known as Blue Code. The AIS output is set to a high level when less than three zeros are received during one period of  $\overline{\text{Reset AIS}}$  immediately followed by another period of  $\overline{\text{Reset AIS}}$  containing less than three zeros. The AIS output is reset to a low level upon the first period of  $\overline{\text{Reset AIS}}$  containing 3 or more zeros.

A logic high level on LTE enables a loopback condition where Out 1 is internally connected to  $A_{in}$  and Out 2 is internally connected to  $B_{in}$  (this disables inputs  $A_{in}$  and  $B_{in}$  to external signals). In this condition, NRZ Data In appears at NRZ Data Out (delayed by the amount of clock cycles it takes to encode and decode the selected line code). A decode clock must be supplied for this operation.

The output controls are Output Enable and Force AIS. These pins allow normal operation, force Out 1 and Out 2 to zero, or force Out 1 and Out 2 to output all ones (AIS condition).



**Pin Assignments**

| PIN NO. | FUNCTION                          | DESCRIPTION  |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |
|---------|-----------------------------------|--|-----|-----|--------------|---|---|-----|---|---|------|---|---|------|---|---|------|
| 1       | Force AIS                         | Pin 19 must be at logic '0' to enable this pin. A logic '1' on this pin forces Out 1 and Out 2 to all ones. A logic '0' on this pin allows normal operation.   |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |
| 2,5     | Mode Select 1,<br>Mode Select 2   | <table border="1"> <thead> <tr> <th>MS1</th> <th>MS2</th> <th>functions as</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>AMI</td> </tr> <tr> <td>0</td> <td>1</td> <td>B8ZS</td> </tr> <tr> <td>1</td> <td>0</td> <td>B6ZS</td> </tr> <tr> <td>1</td> <td>1</td> <td>HDB3</td> </tr> </tbody> </table>  | MS1 | MS2 | functions as | 0 | 0 | AMI | 0 | 1 | B8ZS | 1 | 0 | B6ZS | 1 | 1 | HDB3 |
| MS1     | MS2                               | functions as   |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |
| 0       | 0                                 | AMI  |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |
| 0       | 1                                 | B8ZS   |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |
| 1       | 0                                 | B6ZS   |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |
| 1       | 1                                 | HDB3   |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |
| 3       | NRZ Data In                       | Input data to be encoded into ternary form. The data is clocked by the negative going edge of CLK ENC.   |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |
| 4       | CLK ENC                           | Clock encoder, clock for encoding data at NRZ Data In.   |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |
| 6       | NRZ Data Out                      | Decoded data from ternary inputs A <sub>IN</sub> and B <sub>IN</sub> .   |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |
| 7       | CLK DEC                           | Clock decoder, clock for decoding ternary data on inputs A <sub>IN</sub> and B <sub>IN</sub> .   |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |
| 8,9     | Reset AIS, AIS                    | Logic '0' on <u>Reset AIS</u> resets a decoded zero counter and either resets AIS output to zero provided 3 or more zeros have been decoded in the preceding Reset AIS period or sets AIS to '1' if less than 3 zeros have been decoded in the preceding two Reset AIS periods. A period of Reset AIS is defined from the bit following the bit during which Reset AIS makes a high to low transition to the bit during which Reset AIS makes the next high to low transition. |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |
| 10      | VSS                               | Ground reference.  |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |
| 11      | Error                             | A logic '1' indicates that a violation of the line coding scheme has been decoded.   |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |
| 12      | Clock                             | "OR" function of A <sub>IN</sub> and B <sub>IN</sub> for clock regeneration when pin 14 is at logic '0', "OR" function of Out 1 and Out 2 when pin 14 is at logic '1'.   |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |
| 13,15   | A <sub>IN</sub> , B <sub>IN</sub> | Inputs representing the received PCM signal. A <sub>IN</sub> = '1' represents a positive going '1' and B <sub>IN</sub> = '1' represents a negative going '1'. A <sub>IN</sub> and B <sub>IN</sub> are sampled by the positive going edge of CLK DEC. A <sub>IN</sub> and B <sub>IN</sub> may be interchanged.  |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |
| 14      | LTE                               | Loop Test Enable, this pin selects between normal and loop back operation. A logic '0' selects normal operation where encode and decode are independent and asynchronous. A logic '1' selects a loop back condition where Out 1 is internally connected to A <sub>IN</sub> and Out 2 is internally connected to B <sub>IN</sub> . A decode clock must be supplied.   |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |
| 16,17   | Out 1, Out 2                      | Outputs representing the ternary encoded NRZ Data In signal for line transmission. Out 1 and Out 2 are in return to zero form and are clocked out on the positive going edge of CLK ENC. The length of Out 1 and Out 2 is set by the length of the positive clock pulse.   |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |
| 18      | <u>Reset</u>                      | A logic '0' on this pin resets all internal registers to zero. A logic '1' allows normal operation of all internal registers.  |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |
| 19      | <u>Output Enable</u>              | A logic '1' on this pin forces outputs Out 1 and Out 2 to zero. A logic '0' allows normal operation.   |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |
| 20      | VDD                               | Power to chip.   |     |     |              |   |   |     |   |   |      |   |   |      |   |   |      |

## Specifications HC-5560

**Static Electrical Specifications** Unless Otherwise Specified. Typical parameters at +25°C.  
Min-Max parameters are over operating temperature range. V<sub>DD</sub> = +5V.

| SPECIFICATION  | SYMBOL           | MIN | TYP | MAX | UNITS |
|--|------------------|-----|-----|-----|-------|
| Quiescent Device Current   | I <sub>DD</sub>  |     |     | 100 | µA    |
| Operating Device Current   |                  |     | 10  |     | mA    |
| Out 1, Out 2 Low (Sink) Current<br>(V <sub>OL</sub> = 0.4V)      | I <sub>OL1</sub> | 3.2 |     |     | mA    |
| All Other Outputs Low (Sink) Current<br>(V <sub>OL</sub> = 0.8V) | I <sub>OL2</sub> | 2   |     |     | mA    |
| All outputs High (Source) Current<br>(V <sub>OH</sub> = 4.0V)    | I <sub>OH</sub>  | 2   |     |     | mA    |
| Input Low Current  | I <sub>IL</sub>  |     |     | 10  | µA    |
| Input High Current   | I <sub>IH</sub>  |     |     | 10  | µA    |
| Input Low Voltage  | V <sub>IL</sub>  |     |     | 0.8 | V     |
| Input High Voltage   | V <sub>IH</sub>  | 2.4 |     |     | V     |
| Input Capacitance  | C <sub>IN</sub>  |     |     | 8   | pF    |

**Dynamic Electrical Specifications** Unless otherwise Specified. Typical parameters at +25°C.  
Min-Max parameters are over operating temperature range. V<sub>DD</sub> = +5V.

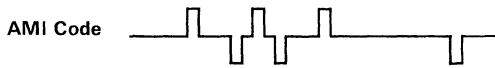
| SPECIFICATION  | SYMBOL            | MIN | TYP | MAX | UNITS | FIG. |
|--|-------------------|-----|-----|-----|-------|------|
| CLK ENC, CLK DEC Input Frequency                             | f <sub>cl</sub>   |     |     | 8.5 | MHz   |      |
| CLK ENC, CLK DEC Rise Time (1.544 MHz)                       | t <sub>rcl</sub>  |     | 10  | 60  | ns    | 1,2  |
| Fall Time  | t <sub>fccl</sub> |     | 10  | 60  | ns    | 1,2  |
| Rise Time (2.048 MHz)  | t <sub>rcl</sub>  |     | 10  | 40  | ns    | 1,2  |
| Fall Time  | t <sub>fccl</sub> |     | 10  | 40  | ns    | 1,2  |
| Rise Time (6.3212 MHz)                                       | t <sub>rcl</sub>  |     | 10  | 30  | ns    | 1,2  |
| Fall Time  | t <sub>fccl</sub> |     | 10  | 30  | ns    | 1,2  |
| Rise Time (8.448 MHz)  | t <sub>rcl</sub>  |     | 5   | 10  | ns    | 1,2  |
| Fall Time  | t <sub>fccl</sub> |     | 5   | 10  | ns    | 1,2  |
| NRZ-Data In to CLK ENC Data Setup Time                       | t <sub>s</sub>    | 20  |     |     | ns    | 1    |
| Data Hold Time   | t <sub>H</sub>    | 20  |     |     | ns    | 1    |
| A <sub>IN</sub> , B <sub>IN</sub> to CLK DEC Data Setup Time | t <sub>s</sub>    | 15  |     |     | ns    | 2    |
| Data Hold Time   | t <sub>H</sub>    | 5   |     |     | ns    | 2    |
| CLK ENC to Out 1, Out 2                                      | t <sub>DD</sub>   |     | 23  | 80  | ns    | 1    |
| Out 1, Out 2 Pulse Width (CLK ENC Duty Cycle = 50%)          |                   |     |     |     |       |      |
| f <sub>cl</sub> = 1.544 MHz                                  | t <sub>w</sub>    |     | 324 |     | ns    | 1    |
| f <sub>cl</sub> = 2.048 MHz                                  | t <sub>w</sub>    |     | 224 |     | ns    | 1    |
| f <sub>cl</sub> = 6.3212 MHz                                 | t <sub>w</sub>    |     | 79  |     | ns    | 1    |
| f <sub>cl</sub> = 8.448 MHz                                  | t <sub>w</sub>    |     | 58  |     | ns    | 1    |
| CLK DEC to NRZ-Data Out.                                     | t <sub>DD</sub>   |     | 25  | 54  | ns    | 2    |
| Setup Time CLK DEC to Reset AIS                              | t <sub>s2</sub>   | 35  |     |     | ns    | 3    |
| Hold Time of Reset AIS = '0'                                 | t <sub>H2</sub>   | 20  |     |     | ns    | 3    |
| Setup Time Reset AIS = '1' to CLK DEC                        | t <sub>s2</sub>   | 0   |     |     | ns    | 3    |
| Reset AIS to AIS output                                      | t <sub>pd5</sub>  |     |     | 42  | ns    | 3    |
| CLK DEC to Error output                                      | t <sub>pd4</sub>  |     |     | 62  | ns    | 3    |



**Line Code Descriptions**

AMI, Alternate Mark Inversion, is used primarily in North American T1 (1.544 MHz) and T1C (3.152 MHz) carriers. Zeros are coded as the absence of a pulse and one's are coded alternately as positive or negative pulses. This type of coding reduces the average voltage level to zero to eliminate DC spectral components, thereby eliminating DC wander. To simplify timing recovery, logic 1's are encoded with 50% duty cycle pulses.

e.g.  
PCM Code 0 0 0 1 0 1 1 1 0 1 0 0 0 0 0 1

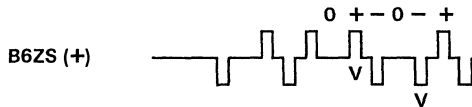
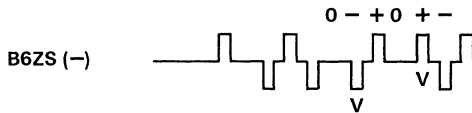


To facilitate timing maintenance at regenerative repeaters along a transmission path, a minimum pulse density of logic 1's is required. Using AMI, there is a possibility of long strings of zeros and the required density may not always exist, leading to timing jitter and therefore higher error rates.

A method for insuring minimum logic 1 density by substituting bipolar code in place of strings of 0's is called BNZS or Bipolar with N Zero Substitution. B6ZS is used commonly in North American T2 (6.3212MHz) carriers. For every string of 6 zeros, bipolar code is substituted according to the following rule;

If the immediate preceding pulse is of (-) polarity, then code each group of 6 zeros as 0 → 0+ → -, and if the immediate preceding pulse is of (+) polarity, code each group of 6 zeros as 0 → 0- → +. One can see the consecutive logic 1 pulses of the same polarity violate the AMI coding scheme.

e.g.  
PCM Code 0 0 0 1 0 1 1 1 0 0 0 0 0 0 0 1

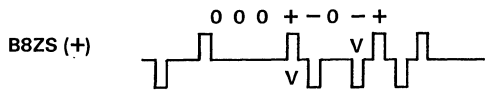
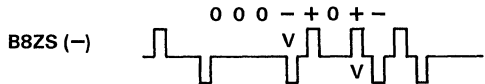


V = Violation

B8ZS is used commonly in North American T1 (1.544 MHz) and T1C (3.152 MHz) carriers. For every string of 8 zeros, bipolar code is substituted according to the following rules;

1. If the immediate preceding pulse is of (-) polarity, then code each group of 8 zeros as 000 → 0+ → -.
2. If the immediate preceding pulse is of (+) polarity then code each group of 8 zeros as 000 → 0- → +.

e.g.  
PCM Code 1 0 1 0 0 0 0 0 0 0 1 1 0



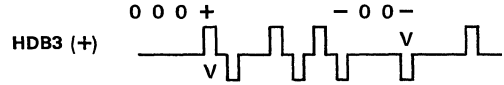
V = Violation

The BNZS coding schemes, in addition to eliminating DC wander, minimize timing jitter and allow a line error monitoring capability.

Another coding scheme is HDB3, high density bipolar 3 used primarily in Europe for 2.048 MHz and 8.448 MHz carriers. This code is similar to BNZS in that it substitutes bipolar code for 4 consecutive zeros according to the following rule;

1. If the polarity of the immediate preceding pulse is (-) and there have been an odd (even) number of logic 1 pulses since the last substitution, each group of 4 consecutive zeros is coded as 000 → (+00+).
2. If the polarity of the immediate preceding pulse is (+) then the substitution is 000 → (-00-) for odd (even) number of logic 1 pulses since the last substitution.

e.g.  
PCM Code 0 0 0 0 1 0 1 1 1 0 0 0 0 0 0 1

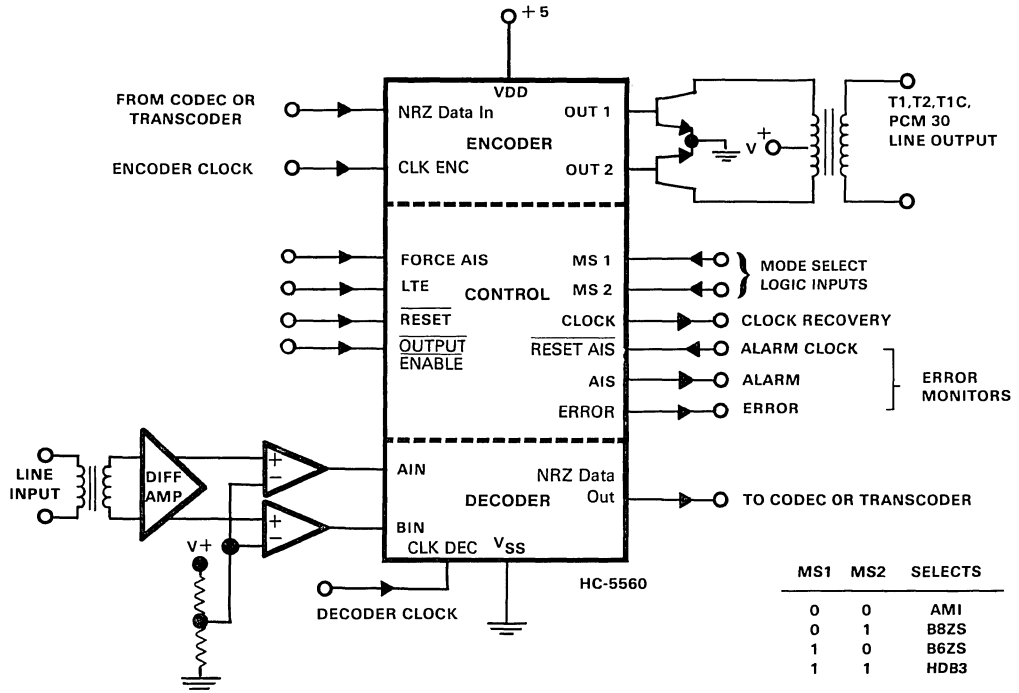


V = Violation

The 3 in HDB3 refers to the coding format that precludes strings of zeros greater than 3. Note that violations are produced only in the fourth bit location of the substitution code and that successive substitutions produce alternate polarity violations.

# HC-5560

## Application Diagram



## Die Characteristics

|                           |                             |
|---------------------------|-----------------------------|
| Transistor Count .....    | 4322                        |
| Die Dimensions .....      | 119 x 133                   |
| Substrate Potential ..... | +V                          |
| Process .....             | SAJI CMOS                   |
| Thermal Constants (°C/W)  | $\theta_{ja}$ $\theta_{jc}$ |
| Plastic DIP, HC-5560      | 67        25                |

Timing Waveforms

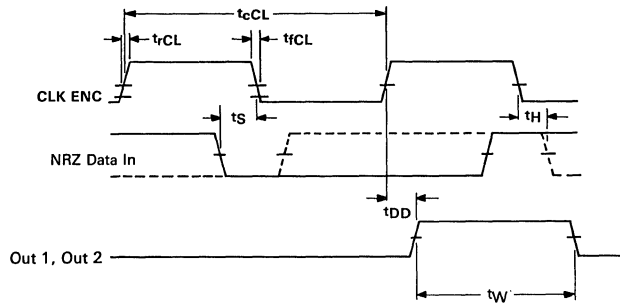


FIGURE 1. TRANSMITTER (CODER) TIMING WAVEFORMS

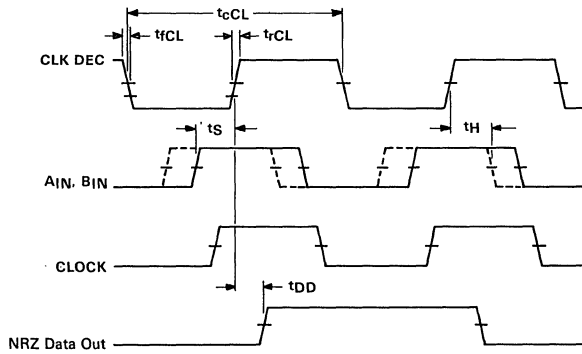


FIGURE 2. RECEIVER (DECODER) TIMING WAVEFORMS

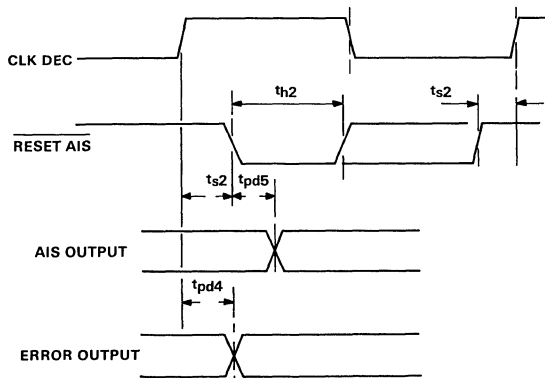


FIGURE 3. RESET AIS INPUT, AIS OUTPUT, ERROR OUTPUT

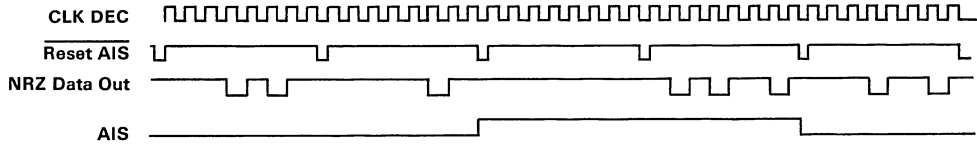


FIGURE 4.

Two consecutive periods of Reset AIS, each containing less than three zeros, sets AIS to a logic '1' and remains in a logic '1' state until a period of Reset AIS contains three or more zeros.

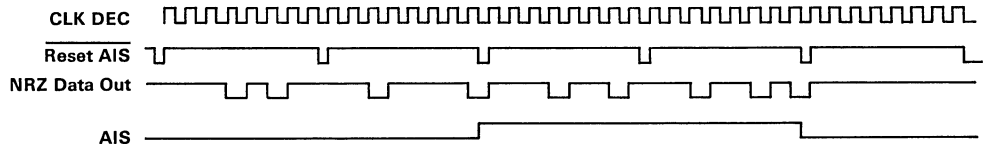


FIGURE 5.

Zeros which occur during a high to low transition of Reset AIS are counted with the zeros that occurred before the high to low transition.

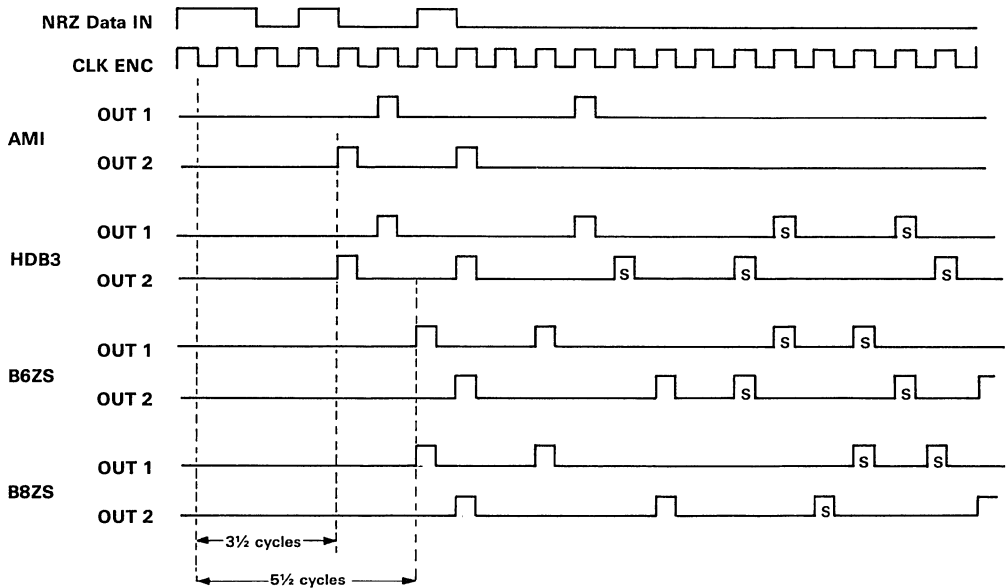


FIGURE 6. ENCODE TIMING AND DELAY

Data is clocked on the negative edge of CLK ENC and appears on Out 1, and Out 2. Out 1 and Out 2 are interchangeable. Bipolar violations and all other pulses inserted by the line coding scheme to encode strings of zeros are labeled with an "S".

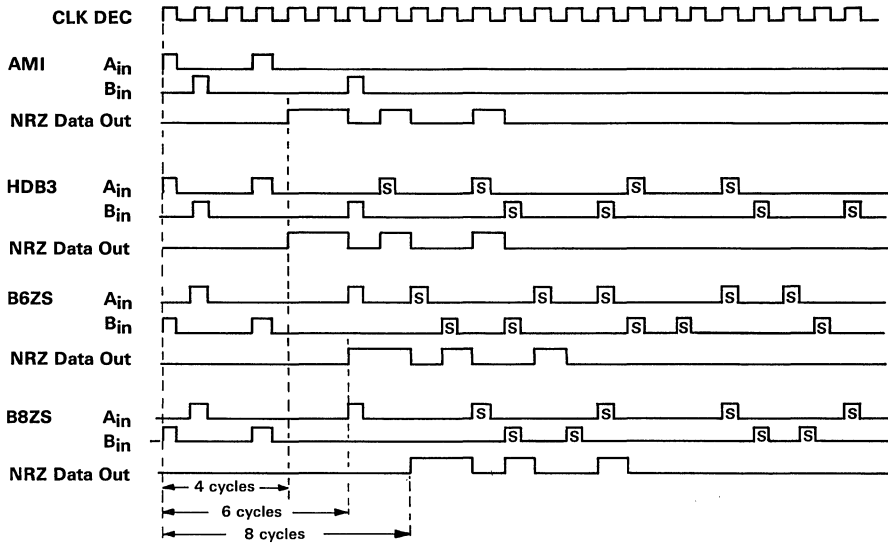


FIGURE 7. DECODE TIMING AND DELAY

Data that appears on A<sub>in</sub> and B<sub>in</sub> is clocked by the positive edge of CLK DEC, decoded and zeros are inserted for all valid line code substitutions. The data then appears in non-return to zero form at output NRZ Data Out. A<sub>in</sub> and B<sub>in</sub> are interchangeable.

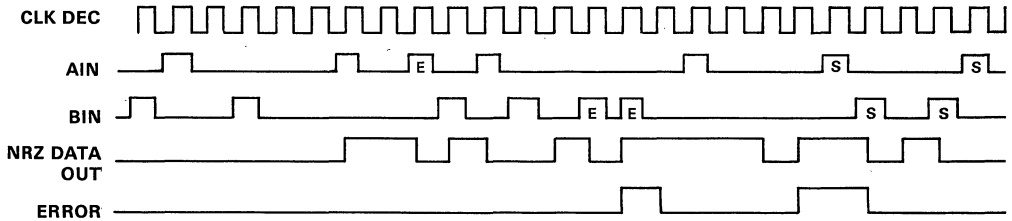


FIGURE 8.

The ERROR signal indicates bipolar violations that are not part of a valid substitution.

## Continuous Variable Slope Delta Demodulator (CVSD)

August 1991

### Features

- All Digital
- Requires Fewer External Parts
- Low Power Drain: 1.5mW from Single 3V-7V Supply
- Time Constants Determined by Clock Frequency; No Calibration or Drift Problems; Automatic Offset Adjustment
- Filter Reset by Digital Control
- Automatic Overload Recovery
- Automatic "Quiet" Pattern Generation

### Applications

- Voice Decoder for Digital Systems and Speech Syntheses
- Voice Main
- Audio Manipulations; Delay Lines, Echo Generation/Suppression, Special Effects, etc.
- Pager/Satellites

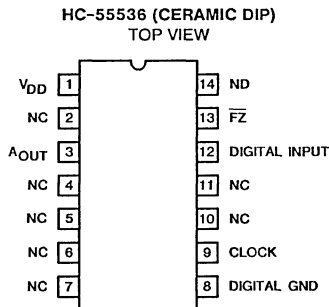
### Description

The HC-55536 is a CMOS integrated circuit used to convert serial NRZ digital data to an analog (voice) signal. Conversion is by delta demodulation, using the Continuously Variable Slope (CVSD) method of demodulation.

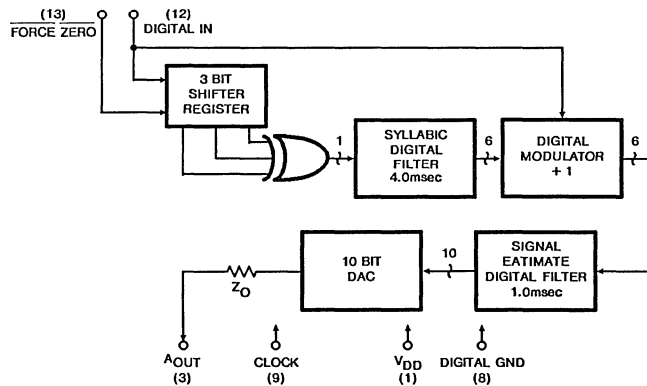
While signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by digital filters which use very low power and require no external timing components. This digital approach allows inclusion of many desirable features, which otherwise would be difficult to implement. The device is usable from 9Kbits/sec to above 64Kbits/sec, and may be easily configured with the HC-55536 CVSD for a complete transmit/receive voice channel.

The HC-55536 is available in a 14 pin Ceramic DIP package.

### Pinout



### Functional Diagram





## Specifications HC-55536

### Absolute Maximum Ratings

|                                |                              |
|--------------------------------|------------------------------|
| Voltage at Any Pin .....       | GND -0.3V to $V_{DD} + 0.3V$ |
| Maximum $V_{DD}$ Voltage ..... | +7.0V                        |
| Minimum $V_{DD}$ Voltage ..... | +3.0V                        |
| Operating $V_{DD}$ Range ..... | +3.0V to +7.0V               |
| Junction Temperature .....     | 175°C                        |

### Operating Temperature Ranges

|                                 |                 |
|---------------------------------|-----------------|
| HC-55536-5 .....                | 0°C to +75°C    |
| HC-55536-9 .....                | -40°C to +85°C  |
| Storage Temperature Range ..... | -65°C to +150°C |

**Electrical Specifications** Unless Otherwise Specified:  $V_{DD} = +5.0V$ ; Bit Range = 16K Bits/sec; typical parameters are at +25°C. Min-Max parameters are over operating temperature.

| PARAMETER                                 | MIN  | TYP  | MAX  | UNIT              | NOTE |
|---|------|------|------|-------------------|------|
| Clock Sampling Rate                       | 9    | 16   | 64   | Kbps              | (1)  |
| Clock Duty Cycle                          | 30   |      | 70   | %                 |      |
| Supply Voltage                            | +3.0 |      | +7.0 | V                 |      |
| Supply Current                            |      | 0.3  | 1.5  | mA                |      |
| Logic "1" Input, $V_{IH}$                 | 3.5  | 4.5  |      | V                 | (2)  |
| Logic "0" Input, $V_{IL}$                 |      |      | 1.5  | V                 | (2)  |
| Audio Output Voltage                      |      | 0.5  | 1.2  | $V_{rms}$         | (3)  |
| Audio Output Impedance                    |      | 150  |      | $k\Omega$         | (4)  |
| Syllabic Filter Time Constant             |      | 4.0  |      | ms                | (5)  |
| L.P. Signal estimate Filter Time Constant |      | 1.0  |      | ms                | (5)  |
| Step Size Ratio                           |      | 24   |      | dB                | (6)  |
| Resolution                                |      | 0.1  |      | %                 | (7)  |
| Minimum Step Size                         |      | 0.2  |      | %                 | (8)  |
| Signal/Noise Ratio                        | 25   |      |      | dB                |      |
| Quieting Pattern Amplitude                |      | 10   |      | mV <sub>p-p</sub> | (9)  |
| Clamping Threshold                        |      | 0.75 |      | F. S.             | (11) |

#### NOTES:

1. There is one NRZ data bit per clock period. Clock must be phased with digital data such that a positive clock transition occurs in the middle of each received data bit. Clock may be run at greater than 64Kbps or less than 9Kbps.
2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate and changes with negative clock transitions.
3. This output includes a DC bias of  $V_{DD}/2$ ; therefore, an AC coupling capacitor is required unless the output filter also includes this bias.
4. Presents approximately 150K $\Omega$  in series with recovered audio voltage. Zero-signal reference is  $V_{DD}/2$ .
5. Note that filter time constants are inversely proportional to clock rate. Both filters approximate single pole responses.
6. Step size compression ratio of the syllabic filter is defined as the ratio of the filter output, with an equal 1-0 bit density input to the filter, to its minimum output.
7. Minimum quantization voltage level expressed as a percentage of supply voltage.
8. The minimum step size between levels is twice the resolution.
9. The "quieting" pattern or idle-channel audio output steps at  $\frac{1}{2}$  the bit rate, changing state on negative clock transitions.
10. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).

# HC-55536

FIG. 1. Illustrates the frequency response of the HC-55536 for varying input levels. To prevent slope overload (slew rate limiting) do not exceed the 0dB boundary. The frequency response is directly proportional to the sampling rate. The output levels were measured after filtering.

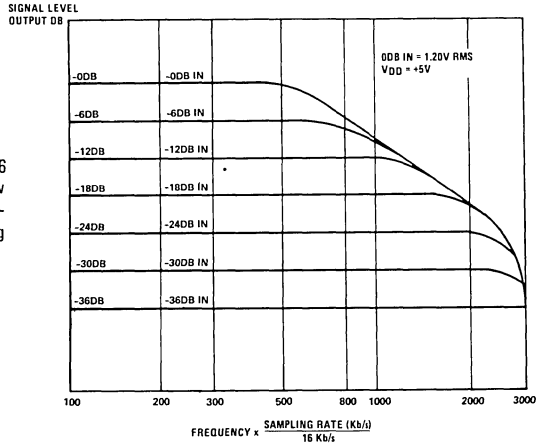


FIGURE 1 - TRANSFER FUNCTION FOR CVSD AT 16Kbps

## Die Characteristics

|                           |               |               |
|---------------------------|---------------|---------------|
| Transistor Count .....    | 1790          |               |
| Die Dimensions .....      | 154 x 93      |               |
| Substrate Potential ..... | +V            |               |
| Process .....             | SAJI CMOS     |               |
| Thermal Constants (°C/W)  | $\theta_{ja}$ | $\theta_{jc}$ |
| Ceramic DIP, HC-55536     | 75            | 15            |

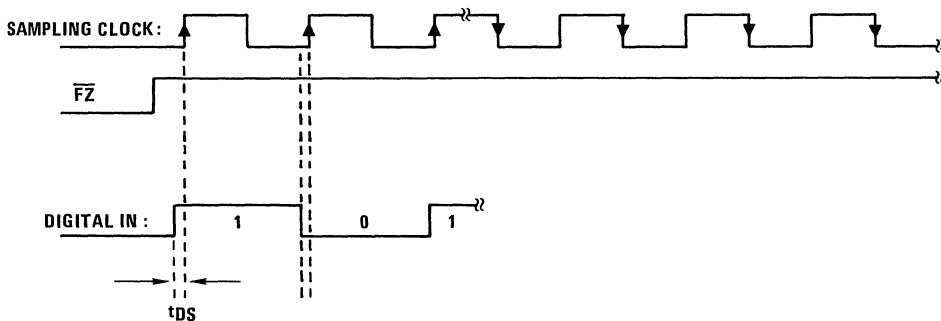
## HC-55536

### Pin Description

| PIN NO.<br>14-LEAD DIP | SYMBOL          | DESCRIPTION  |
|------------------------|-----------------|--|
| 1                      | V <sub>DD</sub> | Positive supply voltage.   |
| 2                      | N.C.            | No internal connection is made to this pin.  |
| 3                      | Audio Out       | Recovered audio out. Presents approximately 150K $\Omega$ source with DC offset of V <sub>DD</sub> /2 should be externally AC couples.       |
| 4                      | N.C.            | No internal connection is made to this pin.  |
| 5                      | N.C.            | No internal connection is made to this pin.  |
| 6,7                    | N.C.            | No internal connection is made to these pins.  |
| 8                      | Digital GND.    | Logic Ground.  |
| 9                      | Clock           | Sampling rate clock must be synchronized with the digital input data such that the data is valid at the positive clock transition.           |
| 10                     | N.C.            | No internal connection is made to this pin.  |
| 11                     | N.C.            | No internal connection is made to this pin.  |
| 12                     | Digital In      | Input for the received serial NRZ digital data.  |
| 13                     | $\overline{FZ}$ | Active low logic input. Activating this input resets the internal logic and forces the recovered audio output into the "quieting" condition. |
| 14                     | N.C.            | No internal connection is made to this pin.  |

NOTE: No active input should be left in a "floating condition".

### Timing Waveforms



$t_{DS}$  : DATA SET UP TIME 100ns TYPICAL

FIGURE 2 - CVSD TIMING DIAGRAM

## Continuously Variable Slope Delta-Modulator (CVSD)

August 1991

### Features

- All Digital
- Requires Few External Parts
- Low Power Drain: 1.5mW Typical From Single 3.0V-7V Supply
- Time Constants Determined by Clock Frequency; No Calibration or Drift Problems: Automatic Offset Adjustment
- Half Duplex Operation Under Digital Control
- Filter Reset Under Digital Control
- Automatic Overload Recovery
- Automatic "Quiet" Pattern Generation
- AGC Control Signal Available

### Applications

- Voice Transmission Over Data Channels (Modems)
- Voice/Data Multiplexing (Pair Gain)
- Voice Encryption/Scrambling
- Voicemail
- Audio Manipulations: Delay Lines, Time Compression, Echo Generation/Suppression, Special Effects, etc.
- Pagers/Satellites
- Data Acquisition Systems
- Voice I/O for Digital Systems and Speech Synthesis Requiring Small Size, Low Weight, and Ease of Reprogrammability

### Description

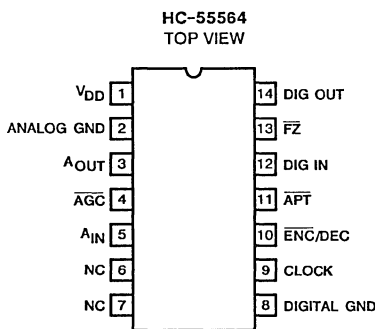
The HC-55564 is a half duplex modulator/demodulator CMOS integrated circuit used to convert voice signals into serial NRZ digital data and to reconver that data into voice. The conversion is by delta-modulation, using the Continuously Variable Slope (CVSD) method of modulation/de-modulation.

While the signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by very low power digital filters which require no external timing components. This approach allows inclusion of many desirable features which would be difficult to implement using other approaches.

The fundamental advantages of delta-modulation, along with its simplicity and serial data format, provide an efficient (low data rate/low memory requirements) method for voice digitization.

The HC-55564 is usable from 9K bits/sec to above 64Kbps. The unit is available in a 14 pin Ceramic DIP, in commercial 0°C to +75°C and industrial -40°C to +85°C, temperature ranges. See the Harris Military databook for a Mil-Std-883C compliant CVSD. Application Notes 607 and 576 are available.

### Pinout



### Functional Diagram

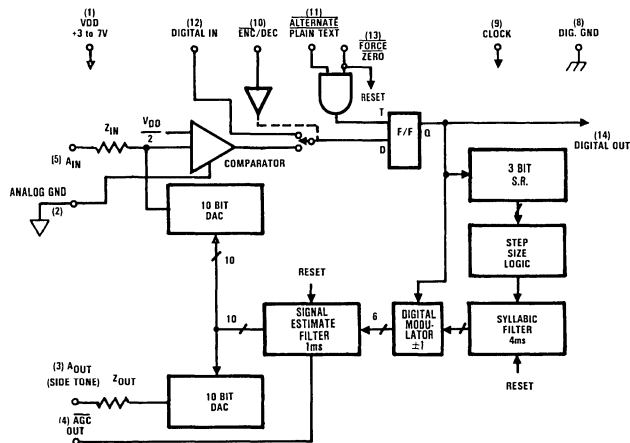


FIGURE 1.

## HC-55564

### Pin Description

| PIN #<br>14-PIN<br>DIP | SYMBOL                            | DESCRIPTION   |
|------------------------|-----------------------------------|---|
| 1                      | $V_{DD}$                          | Positive Supply Voltage. Voltage range is +3.0V to +7.0V.   |
| 2                      | Analog GND                        | Analog Ground connection to D/A ladders and comparator.   |
| 3                      | $A_{OUT}$                         | Audio Out recovered from 10 bit DAC. May be used as side tone at the transmitter. Presents approximately 150 kilohm source with D.C. offset of $V_{DD}/2$ . Within $\pm 2$ dB of Audio Input. Should be externally AC coupled.  |
| 4                      | $\overline{AGC}$                  | Automatic Gain Control output. A logic low level will appear at this output when the recovered signal excursion reaches one-half of full scale value. In each half cycle full scale is $V_{DD}/2$ . The mark-space ratio is proportional to the average signal level.   |
| 5                      | $A_{IN}$                          | Audio Input to comparator. Should be externally AC coupled. Presents approximately 280 kilohms in series with $V_{DD}/2$ .  |
| 6, 7                   | NC                                | No internal connection is made to these pins.   |
| 8                      | Digital GND                       | Logic ground. 0V reference for all logic inputs and outputs.  |
| 9                      | Clock                             | Sampling rate clock. In the decode mode, must be synchronized with the digital input data such that the data is valid at the positive clock transition. In the encode mode, the digital data is clocked out on the negative going clock transition. The clock rate equals the data rate.  |
| 10                     | $\overline{\text{Encode/}}Decode$ | A single CVSD can provide half-duplex operation. The encode or decode function is selected by the logic level applied to this input. A low level selects the encode mode, a high level the decode mode.   |
| 11                     | $\overline{APT}$                  | Alternate Plain Text input. Activating this input caused a digital quieting pattern to be transmitted, however; internally the CVSD is still functional and a signal is still available at the $A_{OUT}$ port. Active low.  |
| 12                     | Digital In                        | Input for the received digital NRZ data.  |
| 13                     | $\overline{FZ}$                   | Force Zero input. Activating this input resets the internal logic and forces the digital output and the recovered audio output into the "quieting" condition. An alternating 1-0 pattern appears at the digital output at $\frac{1}{2}$ the clock rate. When this is decoded by a receive CVSD, a 10mVp-p inaudible signal appears at audio output. Active low. |
| 14                     | Digital Out                       | Output for transmitted digital NRZ data.  |

NOTE: No active input should be left in a "floating condition."

## Specifications HC-55564

### Absolute Maximum Ratings

|                                       |                                    |                              |       |                 |
|---------------------------------------|------------------------------------|------------------------------|-------|-----------------|
| Voltage at Any Pin .....              | GND -0.3V to V <sub>DD</sub> +0.3V | Operating Temperature Ranges | ..... | 0°C to +75°C    |
| Maximum V <sub>DD</sub> Voltage ..... | +7.0V                              | HC-55564-5, -7 .....         |       | -40°C to +85°C  |
| Minimum V <sub>DD</sub> Voltage ..... | +3.0V                              | HC-55564-9 .....             |       | -55°C to +125°C |
| Operating V <sub>DD</sub> .....       | +3.0V to +7.0V                     | HC-55564-2 .....             |       | -65°C to +150°C |
| Junction Temperature .....            | +175°C                             | Storage Temperature .....    |       |                 |

**Electrical Specifications** Unless Otherwise Specified, typical parameters are at +25°C, min-max are over operating temperature ranges. V<sub>DD</sub> = +5.0V, Sampling Rate = 16Kbps, AG = DG = 0V, A<sub>IN</sub> = 1.2Vrms.

| SYMBOL           | PARAMETER                            | MIN  | TYP  | MAX  | UNITS | CONDITIONS  |
|------------------|--------------------------------------|------|------|------|-------|---|
| CLK              | Sampling Rate                        | 9    | 16   | 64   | Kbps  | Note 1  |
| I <sub>DD</sub>  | Supply Current                       | -    | 0.3  | 1.5  | mA    |   |
| V <sub>IH</sub>  | Logic '1' Input                      | 3.5  | -    | -    | V     | Note 2  |
| V <sub>IL</sub>  | Logic '0' Input                      | -    | -    | 1.5  | V     | Note 2  |
| V <sub>OH</sub>  | Logic '1' Output                     | 4.0  | -    | -    | V     | Note 3  |
| V <sub>OL</sub>  | Logic '0' Output                     | -    | -    | 0.4  | V     | Note 3  |
|                  | Clock Duty Cycle                     | 30   | -    | 70   | %     |   |
| A <sub>IN</sub>  | Audio Input Voltage                  | -    | 0.5  | 1.2  | Vrms  | AC Coupled. Note 4  |
| A <sub>OUT</sub> | Audio Output Voltage                 | -    | 0.5  | 1.2  | Vrms  | AC Coupled. Note 5  |
| Z <sub>IN</sub>  | Audio Input Impedance                | -    | 280  | -    | kΩ    | Note 6  |
| Z <sub>OUT</sub> | Audio Output Impedance               | -    | 150  | -    | kΩ    | Note 6  |
| A <sub>E-D</sub> | Transfer Gain                        | -2.0 | -    | +2.0 | dB    | No Load. Audio In to Audio Out.                                       |
| A <sub>E</sub>   | Encode Gain                          | -    | 0.34 | -    | dB    |   |
| A <sub>D</sub>   | Decode Gain                          | -    | 1.23 | -    | dB    |   |
| t <sub>SF</sub>  | Syllabic Filter Time Constant        | -    | 4.0  | -    | mS    | Note 7  |
| t <sub>SE</sub>  | Signal Estimate Filter Time Constant | 1.0  | -    | -    | mS    | Note 7  |
|                  | Resolution                           | -    | 0.1  | -    | %     | Note 8  |
|                  | Minimum Step Size                    | -    | 0.2  | -    | %     | Note 9  |
| V <sub>QP</sub>  | Quieting Pattern Amplitude           | -    | 10   | -    | mVp-p | F <sub>Z</sub> = 0V or APT = 0V, or A <sub>IN</sub> = 0V. Note 10, 13 |
| V <sub>ATH</sub> | AGC Threshold                        | -    | 0.5  | -    | F.S.  | Note 11   |
| V <sub>CTH</sub> | Clamping Threshold                   | -    | 0.75 | -    | F.S.  | Note 12   |

# HC-55564

**NOTES:**

1. There is one NRZ (Non-Return Zero) data bit clock period. Data is clocked out on the negative clock edge. Data is clocked into the CVSD on the positive going edge (see Figure 2). Clock may be run at less than 9Kbps and greater than 64Kbps.
2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate.
3. Logic outputs are CMOS compatible at supply voltage and will withstand short-circuits to  $V_{DD}$  or ground. Digital data output is NRZ and changes with negative clock transitions. Each output will drive one LS TTL load.
4. Recommended voice input range for best voice performance. Should be externally AC coupled.
5. May be used for side-tone in encode mode. Should be externally AC coupled. Varies with audio input level by  $\pm$ dB.
6. Presents series impedance with audio signal. Zero signal reference is approximately  $V_{DD}/2$ .
7. Note that filter time constants are inversely proportional to clock rate. Both filters approximate single pole responses.
8. Minimum quantization voltage level expressed as a percentage of supply voltage.
9. The minimum step size between levels is twice the resolution.
10. The "quieting" pattern or idle-channel audio output steps at one-half the bit rate, changing state on negative clock transitions.
11. A logic "0" will appear at the AGC output pin when the recovered signal reaches one-half of full-scale value (positive or negative), i.e. at  $V_{DD}/2 \pm 25\%$  of  $V_{DD}$ .
12. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches three-quarters of full-scale value, and will unclamp when it falls below this value (positive or negative).
13. Typical encoding threshold for quieting pattern generation is 6.5mVrms at 1kHz input signal, 16kHz clock. The threshold varies inversely with input frequency and proportionally with clock frequency.

## Timing Waveforms

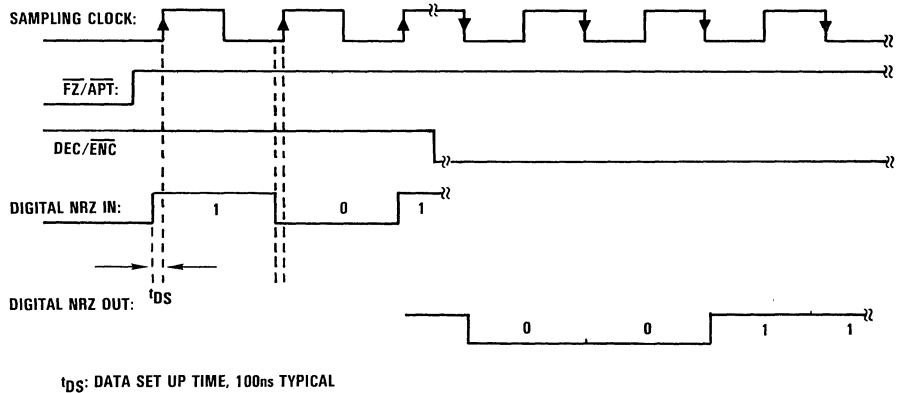
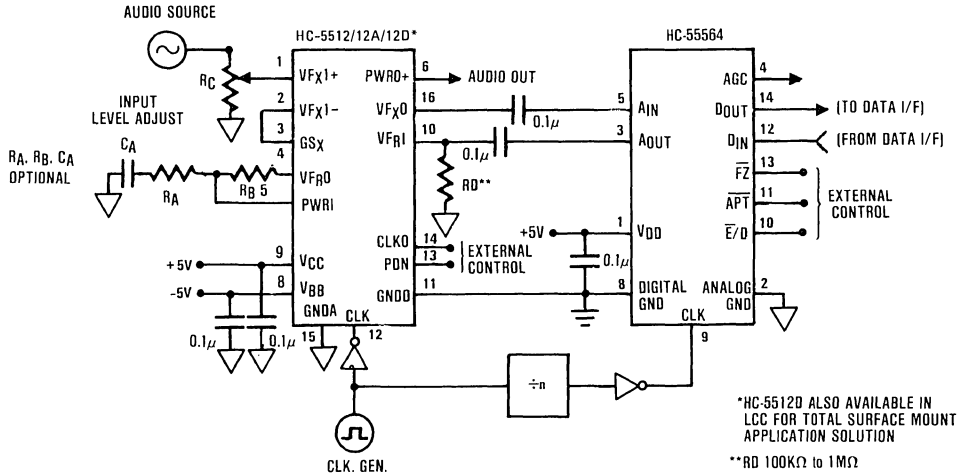


FIGURE 2. CVSD TIMING DIAGRAM

## Die Characteristics

|                           |                             |
|---------------------------|-----------------------------|
| Transistor Count .....    | 1896                        |
| Die Dimensions .....      | 154 x 93                    |
| Substrate Potential ..... | +V                          |
| Process .....             | SAJI CMOS                   |
| Thermal Constants (°C/W)  | $\theta_{ja}$ $\theta_{jc}$ |
| Ceramic DIP               | 75        15                |

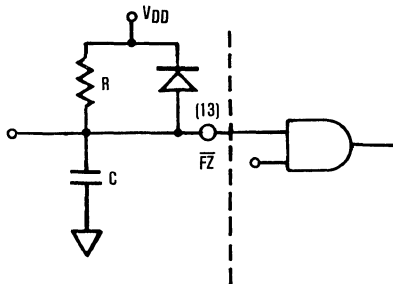
Interface Circuit for HC-55564 CVSD



CVSD Hookup for Evaluation

The circuit in Figure 3 is sufficient to evaluate the voice quality of the CVSD, since when encoding the feedback signal at the audio output pin is the reconstructed audio input signal. CVSD design considerations are as follows:

- 1) Care should be taken in layout to maintain isolation between analog and digital signal paths for proper noise consideration.
- 2) Power supply decoupling is necessary as close to the device as possible. A 0.1µF should be sufficient.
- 3) Ground, then power, must be present before any input signals are applied to the CVSD. Failure to observe this may cause a latchup condition which may be destructive. Latchup may be removed by cycling the power off/on. A power-up reset circuit may be used that strobes Force Zero (Pin 13) during power-up as follows:
- 4) Analog (signal) ground (Pin 2) should be externally tied to Pin 8 and power ground. It is recommended that the AIN and AOUT ground returns connect only to Pin 2.
- 5) Digital inputs and outputs are compatible with standard CMOS logic using the same supply voltage. All unused logic inputs must be tied to the appropriate logic level for desired operation. TTL outputs will require 1K Ohm pull-up resistors. Pins 4 and 14 will each drive CMOS logic or one low power TTL input.
- 6) Since the Audio Out pins are internally DC biased to VDD/2, AC coupling is required. In general, a value of 0.1µF is sufficient for AC coupling of the CVSD audio pins to a filter circuit.
- 7) The AGC output may be externally integrated to drive an AGC pre-amp, or it could drive an LED indicator through a buffer to indicate proper speaking volume.





# HC-55564

Figures 4, 5, and 6 illustrate the typical frequency response of the HC-55564 for varying input levels and for varying sampling rates. To prevent slope overload (slew limiting), the 0dB boundary should not be exceeded. The frequency response is directly proportional to the sampling clock rate.

The flat bandwidth at 0dB doubles for every 16kHz increase in sampling rate. The output levels were measured in the encode mode, without filtering, from  $A_{IN}$  to  $A_{OUT}$ , at  $V_{DD} = +5V$ . 0dB = 1.2Vrms.

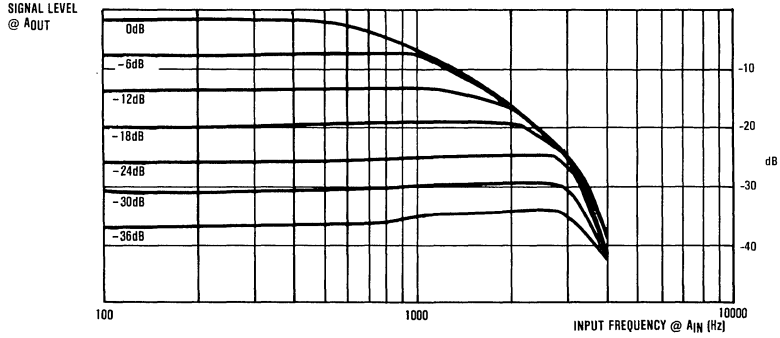


FIGURE 4. 16Kbps

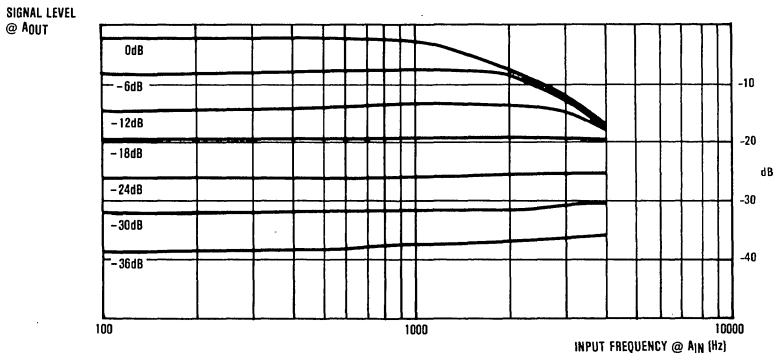


FIGURE 5. 32Kbps

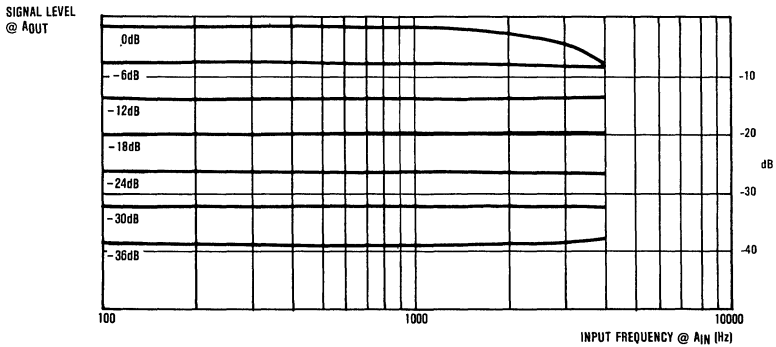


FIGURE 6. 64Kbps

# HC-55564

The following typical performance distortion graphs were realized with the test configuration of Figure 7. The measurement vehicle for Total Harmonic Distortion (THD) was an HP-339A distortion measurement set, and for 2nd and 3rd

harmonic distortion, an HP-3582A spectrum analyzer. All measurement conditions were at  $V_{DD} = +5V$ , and 2nd and 3rd harmonic distortion measurements were C-message filtered.  $0dB = 1.2V_{rms}$ .

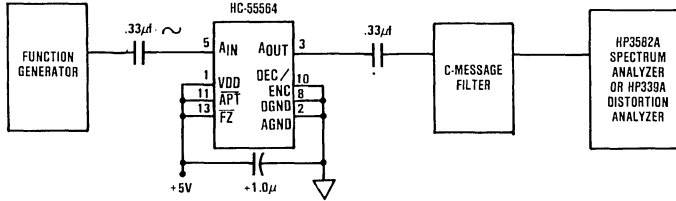


FIGURE 7. TEST AND MEASUREMENT CIRCUIT

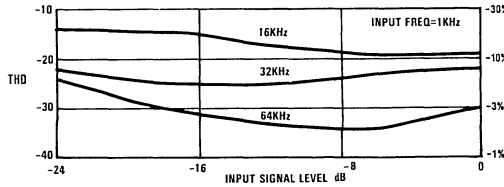


FIGURE 8. CVSD SIGNAL LEVEL vs. TOTAL HARMONIC DISTORTION

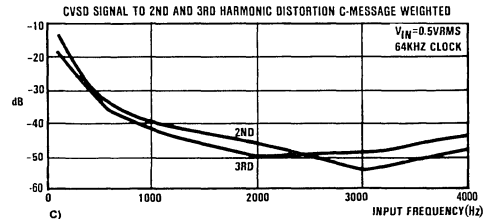
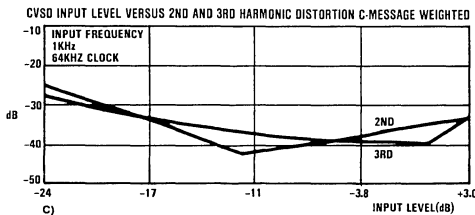
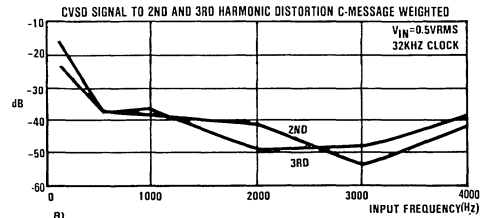
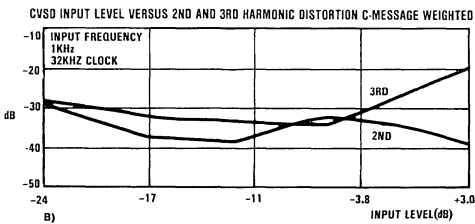
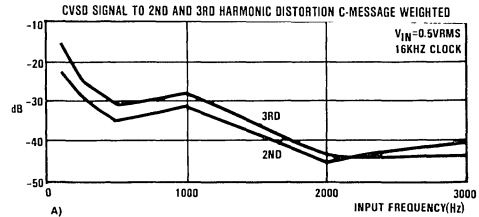
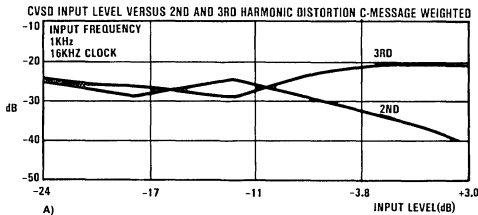


FIGURE 9A, B, C. CVSD INPUT LEVEL vs. 2ND AND 3RD HARMONIC DISTORTION

FIGURE 10A, B, C. CVSD INPUT FREQUENCY vs. 2ND AND 3RD HARMONIC DISTORTION



## HARRIS QUALITY AND RELIABILITY

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# Harris Quality & Reliability

## Introduction

Success in the integrated circuit industry means more than simply meeting or exceeding the demands of today's market. It also includes anticipating and accepting the challenges of the future. It results from a process of continuing improvement and evolution, with perfection as the constant goal.

Harris Semiconductor's commitment to supply only top value integrated circuits has made quality improvement a mandate for every person in our work force — from circuit designer to manufacturing operator, from hourly employee to corporate executive. Price is no longer the only determinant in marketplace competition. Quality, reliability, and performance enjoy significantly increased importance as measures of value in integrated circuits.

Quality in integrated circuits cannot be added on or considered after the fact. It begins with the development of capable process technology and product design. It continues in manufacturing, through effective controls at each process or step. It culminates in the delivery of products which meet or exceed the expectations of the customer.

## The Role of The Quality Organization

The emphasis on building quality into the design and manufacturing processes of a product has resulted in a significant refocus of the role of the Quality organization. In addition to facilitating the development of SPC and DOX programs and working with manufacturing to establish control charts, Quality professionals are involved in the measurement of equipment capability, standardization of inspection equipment and processes, procedures for chemical controls, analysis of inspection data and feedback to the manufacturing areas, coordination of efforts for process and product improvement, optimization of environmental or raw materials quality, and the development of quality improvement programs with vendors.

At critical manufacturing operations, process and product quality is analyzed through random statistical sampling and product monitors. The Quality organization's role is changing from policing quality to leadership and coordination of quality programs or

procedures through auditing, sampling, consulting, and managing Quality Improvement projects.

To support specific market requirements, or to ensure conformance to military or customer specifications, the Quality organization still performs many of the conventional quality functions (e.g., group testing for military products or wafer lot acceptance). But, true to the philosophy that quality is everyone's job, much of the traditional on-line measurement and control of quality characteristics is where it belongs — with the people who make the product. The Quality organization is there to provide leadership and assistance in the deployment of quality techniques, and to monitor progress.

## The Improvement Process

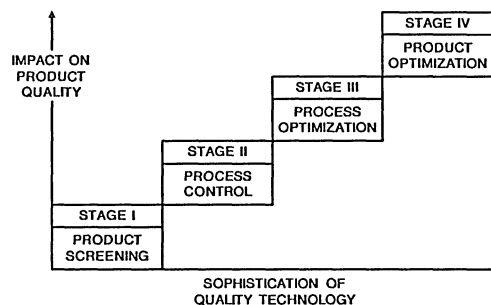


FIGURE 1. STAGES OF STATISTICAL QUALITY TECHNOLOGY

Harris Semiconductor's quality methodology is evolving through the stages shown in Figure 1. In 1981 we embarked on a program to move beyond Stage I, and we are currently in the transition from Stage II to Stage III, as more and more of our people become involved in quality activities. The traditional "quality" tasks of screening, inspection, and testing are being replaced by more effective and efficient methods, putting new tools into the hands of all employees. Table 1 illustrates how our quality systems are changing to meet today's needs.

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS

| AREA                     | FUNCTION                           | MANUFACTURING CONTROLS | QA/QC MONITOR AUDIT |
|--------------------------|------------------------------------|------------------------|---------------------|
| Wafer Fab                | • JAN Self-Audit                   |                        | X                   |
|                          | • Environmental                    |                        |                     |
|                          | - Room/Hood Particulates           | X                      | X                   |
|                          | - Temperature/Humidity             | X                      | X                   |
|                          | - Water Quality                    |                        | X                   |
|                          | • Product                          |                        |                     |
|                          | - Junction Depth                   | X                      |                     |
|                          | - Sheet Resistivities              | X                      |                     |
|                          | - Defect Density                   | X                      | X                   |
|                          | - Critical Dimensions              | X                      | X                   |
|                          | - Visual Inspection                | X                      | X                   |
|                          | - Lot Acceptance                   |                        | X                   |
|                          | • Process                          |                        |                     |
|                          | - Film Thickness                   | X                      | X                   |
|                          | - Implant Dosages                  | X                      |                     |
|                          | - Capacitance Voltage Changes      | X                      | X                   |
|                          | - Conformance to Specification     | X                      | X                   |
|                          | • Equipment                        |                        |                     |
| - Repeatability          | X                                  | X                      |                     |
| - Profiles               | X                                  | X                      |                     |
| - Calibration            |                                    | X                      |                     |
| - Preventive Maintenance | X                                  | X                      |                     |
| Assembly                 | • JAN Self-Audit                   |                        | X                   |
|                          | • Environmental                    |                        |                     |
|                          | - Room/Hood Particulates           | X                      | X                   |
|                          | - Temperature/Humidity             | X                      | X                   |
|                          | - Water Quality                    |                        | X                   |
|                          | • Product                          |                        |                     |
|                          | - Documentation Check              |                        | X                   |
|                          | - Dice Inspection                  | X                      | X                   |
|                          | - Wire Bond Pull Strength/Controls | X                      | X                   |
|                          | - Die Sear Controls                |                        | X                   |
|                          | - Pre-Seal Visual                  | X                      | X                   |
|                          | - Fine/Gross Leak                  | X                      | X                   |
|                          | - PIND Test                        | X                      |                     |
|                          | - Lead Finish Visuals, Thickness   | X                      | X                   |
|                          | - Die Shear                        |                        | X                   |
|                          | - Solderability                    |                        | X                   |
|                          | • Process                          |                        |                     |
|                          | - Operator Quality Performance     | X                      | X                   |
|                          | - Saw Controls                     | X                      |                     |
|                          | - Die Attach Temperatures          | X                      | X                   |
|                          | - Seal Parameters                  | X                      |                     |
|                          | - Seal Temperature Profile         | X                      | X                   |
|                          | - Sta-Bake Profile                 | X                      |                     |
|                          | - Temp Cycle Chamber Temperature   | X                      | X                   |
|                          | - ESD Protection                   | X                      | X                   |
|                          | - Plating Bath Controls            | X                      |                     |
|                          | - Mold Parameters                  | X                      | X                   |
| Test                     | • JAN Self-Audit                   |                        | X                   |
|                          | • Temperature/Humidity             | X                      | X                   |
|                          | • ESD Controls                     | X                      |                     |
|                          | • Temperature Test Calibration     | X                      |                     |
|                          | • Test System Calibration          | X                      |                     |
|                          | • Test Procedures                  |                        | X                   |
|                          | • Control Unit Compliance          | X                      |                     |
|                          | • Lot Acceptance Conformance       | X                      |                     |
|                          | • Group A Lot Acceptance           |                        | X                   |
| Probe                    | • JAN Self-Audit                   |                        | X                   |
|                          | • Wafer Repeat Correlation         | X                      |                     |
|                          | • Visual Requirements              | X                      | X                   |
|                          | • Documentation                    | X                      | X                   |
|                          | • Process Performance              | X                      | X                   |

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS (CONTINUED)

| AREA           | FUNCTION   | MANUFACTURING CONTROLS | QA/QC MONITOR AUDIT |
|----------------|--|------------------------|---------------------|
| Burn-In        | <ul style="list-style-type: none"> <li>• JAN Self-Audit</li> <li>• Functionality Board Check</li> <li>• Oven Temperature Controls</li> <li>• Procedural Conformance</li> </ul>           | X                      | X                   |
|                |  | X                      | X                   |
| Brand          | <ul style="list-style-type: none"> <li>• JAN Self-Audit</li> <li>• ESD Controls</li> <li>• Brand Permanency</li> <li>• Temperature/Humidity</li> <li>• Procedural Conformance</li> </ul> | X                      | X                   |
|                |  | X                      | X                   |
|                |  | X                      | X                   |
|                |  | X                      | X                   |
| QCI Inspection | <ul style="list-style-type: none"> <li>• JAN Self-Audit</li> <li>• Group B Conformance</li> <li>• Group C and D Conformance</li> </ul>   |                        | X                   |
|                |  |                        | X                   |
|                |  |                        | X                   |

**Designing For Manufacturability**

Assuring quality and reliability in integrated circuits begins with good product and process design. This has always been a strength in Harris Semiconductor's quality approach. We have a very long lineage of high reliability, high performance products that have resulted from our commitment to design excellence. All Harris products are designed to meet the stringent quality and reliability requirements of the most demanding end equipment applications, from military and space to industrial and telecommunications. The application of new tools and methods has allowed us to continuously upgrade the design process.

Each new design is evaluated throughout the development cycle to validate the capability of the new product to meet the end market performance, quality, and reliability objectives.

The validation process has four major components:

1. Design simulation/optimization
2. Layout verification
3. Product demonstration
4. Reliability assessment.

Harris designers have an extensive set of very powerful Computer-Aided Design (CAD) tools to create and optimize product designs (see Table 2).

TABLE 2. APPROACH AND IMPACT OF STATISTICAL QUALITY TECHNOLOGY

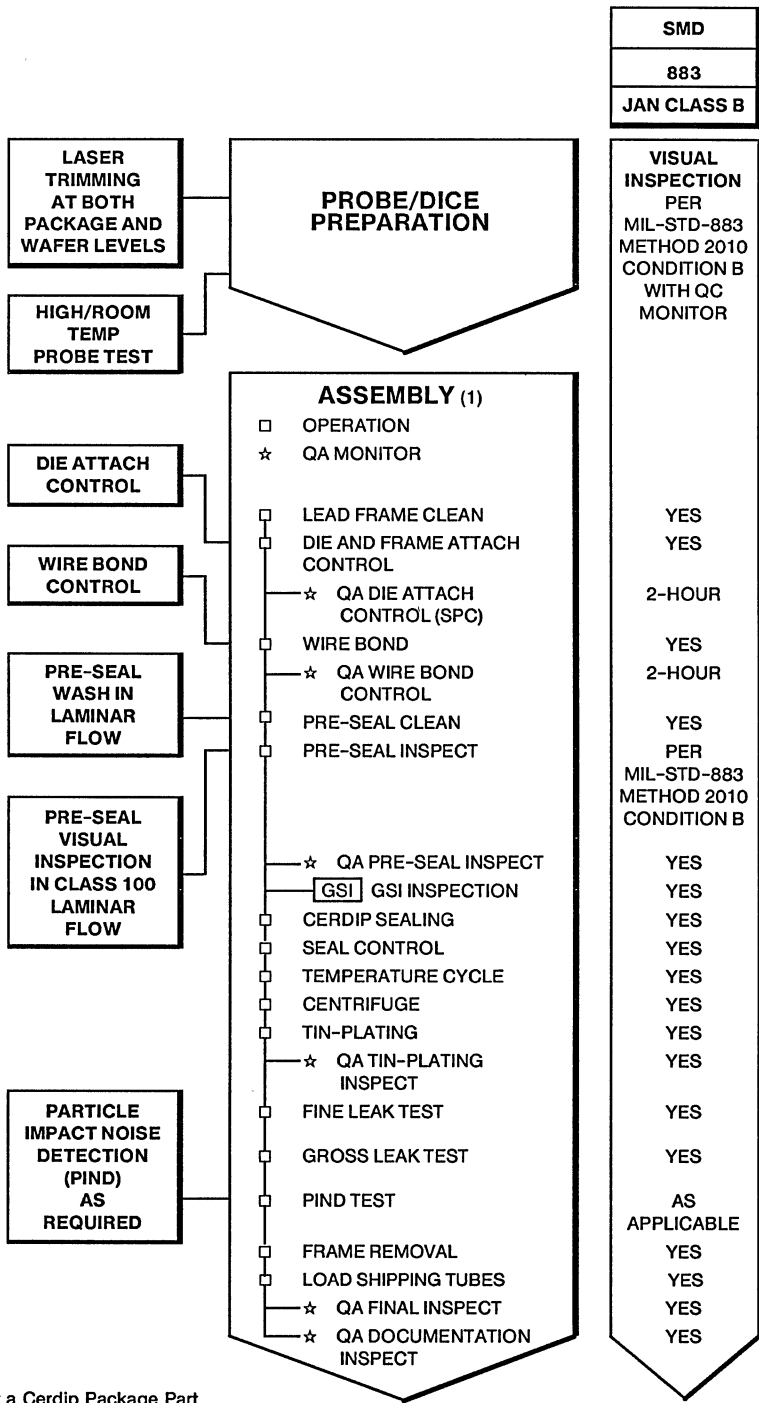
| STAGE                       | APPROACH  | IMPACT   |
|-----------------------------|---|--|
| I<br>Product Screening      | <ul style="list-style-type: none"> <li>• Stress and Test</li> <li>• Defective Prediction</li> </ul>                   | <ul style="list-style-type: none"> <li>• Limited Quality</li> <li>• Costly</li> <li>• After-The-Fact</li> </ul>                          |
| II<br>Process Control       | <ul style="list-style-type: none"> <li>• Statistical Process Control</li> <li>• Just-In-Time Manufacturing</li> </ul> | <ul style="list-style-type: none"> <li>• Identifies Variability</li> <li>• Reduces Costs</li> <li>• Real Time</li> </ul>                 |
| III<br>Process Optimization | <ul style="list-style-type: none"> <li>• Design of Experiments</li> <li>• Process Simulation</li> </ul>               | <ul style="list-style-type: none"> <li>• Minimizes Variability</li> <li>• Before-The-Fact</li> </ul>                                     |
| IV<br>Product Optimization  | <ul style="list-style-type: none"> <li>• Design for Producibility</li> <li>• Product Simulation</li> </ul>            | <ul style="list-style-type: none"> <li>• Insensitive to Variability</li> <li>• Designed-In Quality</li> <li>• Optimal Results</li> </ul> |

**Special Testing**

Harris Semiconductor offers several standard screen flows to support a customer's need for additional testing and reliability assurance. These flows include environmental stress testing, burn-in, and electrical testing at temperatures other than +25°C. The flows shown on pages 9-6 and 9-7 indicate the Harris standard screening processes. In addition, Harris can supply products tested to customer specifications both for electrical requirements and for non-standard environmental stress screening. Consult your field sales representative for details.



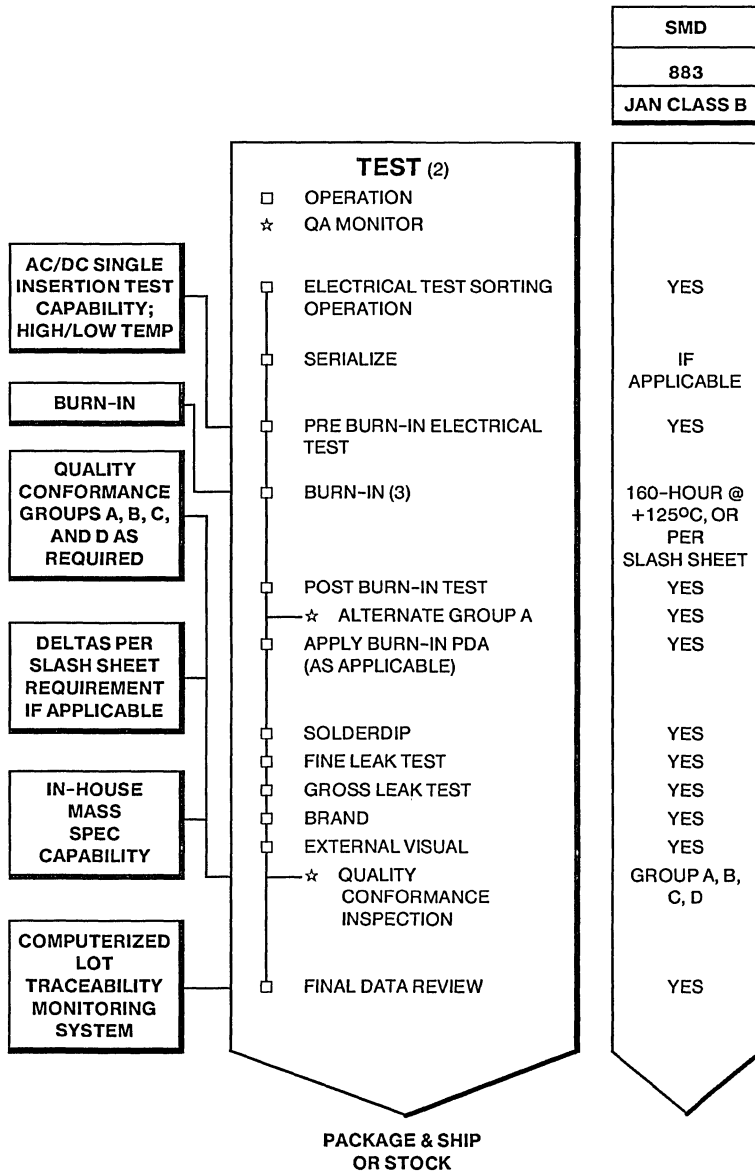
# Harris Semiconductor Standard Processing Flows



(1) Example for a Cerdip Package Part

# Harris Semiconductor Standard Processing Flows

(Continued)



**10**

QUALITY AND RELIABILITY

(2) -55°C TO +125°C

(3) Burn-in test temperatures can be increased and time reduced per regression tables in Mil-Std-883, Method 1015.

**TABLE 3. SUMMARIZING CONTROL APPLICATIONS**

| FAB  |   |  |  |
|--|---|--|--|
| <ul style="list-style-type: none"> <li>• Diffusion                             <ul style="list-style-type: none"> <li>- Junction Depth</li> <li>- Sheet Resistivities</li> <li>- Oxide Thickness</li> <li>- Implant Dose Calibration</li> <li>- Uniformity</li> </ul> </li> </ul>                                  | <ul style="list-style-type: none"> <li>• Thin Film                             <ul style="list-style-type: none"> <li>- Film Thickness</li> <li>- Uniformity</li> <li>- Refractive Index</li> <li>- Film Composition</li> </ul> </li> </ul>   | <ul style="list-style-type: none"> <li>• Photo Resist                             <ul style="list-style-type: none"> <li>- Critical Dimension</li> <li>- Resist Thickness</li> <li>- Etch Rates</li> </ul> </li> </ul>                           | <ul style="list-style-type: none"> <li>• Measurement Equipment                             <ul style="list-style-type: none"> <li>- Critical Dimension</li> <li>- Film Thickness</li> <li>- 4 Point Probe</li> <li>- Ellipsometer</li> </ul> </li> </ul> |
| ASSEMBLY   |   |  |  |
| <ul style="list-style-type: none"> <li>• Pre-Seal                             <ul style="list-style-type: none"> <li>- Die Prep Visuals</li> <li>- Yields</li> <li>- Die Attach Heater Block</li> <li>- Die Shear</li> <li>- Wire Pull</li> <li>- Saw Blade Wear</li> <li>- Pre-Cap Visuals</li> </ul> </li> </ul> | <ul style="list-style-type: none"> <li>• Post-Seal                             <ul style="list-style-type: none"> <li>- Internal Package Moisture</li> <li>- Tin Plate Thickness</li> <li>- PIND Defect Rate</li> <li>- Solder Thickness</li> <li>- Leak Tests</li> <li>- Module Rm. Solder Pot Temp.</li> <li>- Seal</li> <li>- Temperature Cycle</li> </ul> </li> </ul> | <ul style="list-style-type: none"> <li>• Measurement                             <ul style="list-style-type: none"> <li>- XRF</li> <li>- Radiation Counter</li> <li>- Thermocouples</li> <li>- GM-Force Measurement</li> </ul> </li> </ul>       |  |
| TEST   |   |  |  |
|  | <ul style="list-style-type: none"> <li>- Handlers/Test Systems</li> <li>- Defect Pareto Charts</li> <li>- Lot % Defective</li> <li>- ESD Failures per Month</li> </ul>  | <ul style="list-style-type: none"> <li>- Monitor Failures</li> <li>- Lead Strengthening Quality</li> <li>- After Burn-In PDA</li> </ul>  |  |
| OTHER  |   |  |  |
| <ul style="list-style-type: none"> <li>• IQC                             <ul style="list-style-type: none"> <li>- Vendor Performance</li> <li>- Material Criteria</li> <li>- Quality Levels</li> </ul> </li> </ul>   | <ul style="list-style-type: none"> <li>• Environment                             <ul style="list-style-type: none"> <li>- Water Quality</li> <li>- Clean Room Control</li> </ul> </li> </ul>  | <ul style="list-style-type: none"> <li>• IQC Measurement/Analysis                             <ul style="list-style-type: none"> <li>- XRF</li> <li>- ADE</li> <li>- 4 Point Probe</li> <li>- Chemical Analysis Equipment</li> </ul> </li> </ul> |  |

**Controlling and Improving the Manufacturing Process - SPC/DOX**

Statistical process control (SPC) is the basis for quality control and improvement at Harris Semiconductor. Harris manufacturing people use over 1,000 Shewhart control charts to determine the normal variabilities in processes, materials, and products. Critical process variables are measured and control limits are plotted on the control charts. Appropriate action is taken if the charts show that a variable is outside the process control limits or indicates a trend toward the limit. These same control charts are powerful tools for use in reducing variations in processing, materials, and products. Table 3 lists some typical manufacturing applications of control charts at Harris Semiconductor.

But SPC is only part of the solution. Processes which operate in statistical control are not always capable of meeting engineering requirements. The conventional way of dealing with this in the semiconductor industry has been to implement 100% screening or inspection steps to remove defects, but these techniques are insufficient to meet today's demands for the highest reliability and perfect quality performance.

Harris still uses screening and inspection to "grade" products and to satisfy specific customer requirements for burn-in, multiple temperature test insertions, environmental screening, and visual inspection as value-added testing options. However, inspection and screening are limited in their ability to reduce product

defects to the levels expected by today's buyers. In addition, screening and inspection have an associated expense, which raises product cost.

Harris engineers are, instead, using Design of Experiments (DOX), a scientifically disciplined mechanism for evaluating and implementing improvements in product processes, materials, equipment, and facilities. These improvements are aimed at reducing the number of defects by studying the key variables controlling the process, and optimizing the procedures or design to yield the best result. This approach is a more time-

**TABLE 4. HARRIS I.C. DESIGN TOOLS**

| DESIGN STEP           | PRODUCTS             |                               |
|-----------------------|----------------------|-------------------------------|
|                       | ANALOG               | DIGITAL                       |
| Functional Simulation | Slice                | Silos<br>Proteous<br>Socrates |
| Parametric Simulation | Slice<br>Monte Carlo | Slice                         |
| Schematic Capture     | Note 1               | Daisy<br>SDA-Mass Comp        |
| Functional Checking   | Note 1               | SDA-LVS                       |
| Rules Checking        | Calma-DRC            | Harris Dash                   |
| Parasitic Extraction  | Note 1               | SDA-LVS                       |

NOTE 1. Tools are in Development.

consuming method of achieving quality perfection, but a better product results from the efforts, and the basic causes of product nonconformance can be eliminated.

SPC, DOX, and design for manufacturability, coupled with our 100% test flows, combine in a product assurance program that delivers the quality and reliability performance demanded for today and for the future.

### Average Outgoing Quality (AOQ)

Average Outgoing Quality is a yardstick for our success in quality manufacturing. The average outgoing electrical defective is determined by randomly sampling units from each lot and is measured in parts per million (PPM). The current procedures and sampling plans outlined in MIL-STD-883 and MIL-M-38510 are used by our quality inspectors.

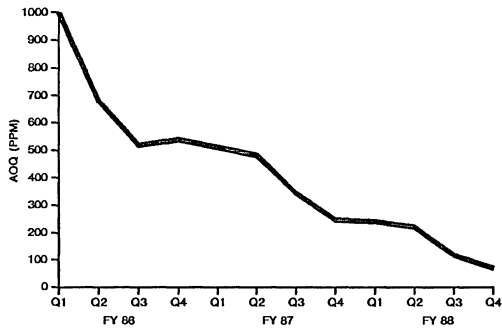


FIGURE 2. DEFECTIVE PARTS PER MILLION

The focus on this quality parameter has resulted in a continuous improvement over the past three years. AOQ has improved from 1,000 PPM to less than 100 PPM, and the goal for 1989 is to continue improvement toward a goal of 0 PPM.

### Training

The basis of a successful transition from conventional quality programs to more effective, total involvement is training. Extensive training of personnel involved in product manufacturing began in 1984 at Harris, with a comprehensive development program in statistical methods. Using the resources of the University of Tennessee, private consultants, and internally developed programs, training of over 2,000 engineers, supervisors, and operators/technicians has been completed.

Nearly 1,000 operators, 100 supervisors, and more than 800 engineers have been trained in SPC methods, providing them with tools to improve the overall level of uniformity of Harris products. Almost 300 engineers have received training in DOX methods: learning to evaluate changes in process operations, set up new processes, select or accept new equipment, evaluate materials, select vendors, compare two or more pieces of equipment, and compare two or more process techniques.

Over the past four years, Harris has also deployed a comprehensive training program for hourly operators and supervisors in job requirements and functional skills. All hourly manufacturing employees participate (see Table 5).

TABLE 5. SUMMARY OF TRAINING PROGRAMS

| COURSE                               | AUDIENCE                        | LENGTH   | TOPICS COVERED   |
|--------------------------------------|---------------------------------|----------|--|
| SPC                                  | Manufacturing Operators         | 8 Hours  | Basic Philosophy, Statistical Calculations<br>Graphing Techniques, Pareto Charts, Control Charts   |
| SPC                                  | Manufacturing Supervisors       | 21 Hours | Basic Philosophy, Statistical Calculations<br>Graphing Techniques, Pareto Charts, Control Charts,<br>Testing for Inspector Agreement, Cause & Effect Diagrams,<br>1 & 2 Sample Methods |
| SPC                                  | Engineers and Managers          | 48 Hours | Basic Philosophy, Graphical Methods, Control Charts,<br>Rational Subgrouping, Variance Components, 1 & 2<br>Sample Methods, Pareto Charts, Cause & Effect Diagrams                     |
| DOX<br>(Design of<br>Experiments)    | Engineers and Managers          | 88 Hours | Factorial Designs, Fractional Factorial Designs,<br>Blocking Designs, Variance Components,<br>Computer Usage, Normal Probability Plotting  |
| RSM<br>(Response Surface<br>Methods) | Engineers and Managers          | 40 Hours | Steepest Ascent, Central Composite Designs,<br>Box-Behnken Designs, Computer Usage,<br>Contour Plotting, Second Order Response Surfaces  |
| Continuous<br>Improvement<br>Methods | Manufacturing Supervisors       | 12 Hours | Basic Philosophy, Pareto Analysis, Imagineering,<br>Run Charts, Cause & Effect Diagrams, Histograms,<br>Ideas of Control Charts  |
| SPC-<br>The Essentials               | Department-Level<br>Work Groups | 20 Hours | Basic Philosophy, of Continuous Improvement, Imagineering<br>Pareto Charts, Cause & Effect Diagrams, Flow Charts,<br>Graphical Display, Control Charts, Ideas of Experiment            |

## Incoming Materials

With statistical procedures in place to improve quality in the manufacturing operation, the impact of silicon, chemicals, gases, and other materials used in processing the product has become more measurable. Quality and consistency are important; it is logical to feed the manufacturing line with materials manufactured by vendors using equivalent statistical controls.

In order to ensure optimum quality of materials purchased from vendors, Harris initiated and coordinated an aggressive program to link key suppliers to our manufacturing operations. This network is formed by certifying strategic vendors who meet the highest

quality standards while demonstrating a commitment to the use of statistical controls in their manufacturing operations.

SPC seminars, development of open working relationships, understanding of manufacturing needs and vendor capabilities, and continual improvement programs are all part of the certification process. Certified suppliers have passed stringent quality and SPC audits, while continuing to supply material with 100% conformance to Harris requirements.

In addition to the certification process, Harris has worked to promote improved quality in the performance of all our qualified vendors, who must meet rigorous incoming inspection criteria (see Table 6).

TABLE 6. INCOMING QUALITY CONTROL MATERIAL QUALITY CONFORMANCE

| MATERIAL                         | INCOMING INSPECTIONS  | VENDOR DATA REQUIREMENTS  |
|----------------------------------|---|---|
| Silicon                          | <ul style="list-style-type: none"> <li>• Resistivity</li> <li>• Crystal Orientation</li> <li>• Dimensions</li> <li>• Edge Conditions</li> <li>• Taper</li> <li>• Thickness</li> <li>• Total Thickness Variation</li> <li>• Backside Criteria</li> <li>• Oxygen</li> <li>• Carbon</li> </ul>   | <ul style="list-style-type: none"> <li>• Equipment Capability Control Charts               <ul style="list-style-type: none"> <li>- Oxygen</li> <li>- Resistivity</li> </ul> </li> <li>• Control Charts Related to               <ul style="list-style-type: none"> <li>- Enhanced Gettering</li> <li>- Total Thickness Variation</li> <li>- Total Indicated Reading</li> <li>- Particulates</li> </ul> </li> <li>• Certificate of Analysis for all Critical Parameters</li> </ul>  |
| Chemicals/Photoresists/<br>Gases | <ul style="list-style-type: none"> <li>• Chemicals               <ul style="list-style-type: none"> <li>- Assay</li> <li>- Major Contaminants</li> </ul> </li> <li>• Molding Compounds               <ul style="list-style-type: none"> <li>- Spiral Flow</li> <li>- Thermal Characteristics</li> </ul> </li> <li>• Gases               <ul style="list-style-type: none"> <li>- Impurities</li> </ul> </li> <li>• Photoresists               <ul style="list-style-type: none"> <li>- Viscosity</li> <li>- Film Thickness</li> <li>- Solids</li> <li>- Pinholes</li> </ul> </li> </ul> | <ul style="list-style-type: none"> <li>• Certificate of Analysis on all Critical Parameters</li> <li>• Control Charts               <ul style="list-style-type: none"> <li>- Assay</li> <li>- Contaminants</li> <li>- Water</li> <li>- Selected Parameters</li> </ul> </li> <li>• Control Charts               <ul style="list-style-type: none"> <li>- Assay</li> <li>- Contaminants</li> </ul> </li> <li>• Control Charts on               <ul style="list-style-type: none"> <li>- Photospeed</li> <li>- Thickness</li> <li>- UV Absorbance</li> <li>- Filterability</li> <li>- Water</li> <li>- Contaminants</li> </ul> </li> </ul> |
| Thin Film Materials              | <ul style="list-style-type: none"> <li>• Assay</li> <li>• Selected Contaminants</li> </ul>  | <ul style="list-style-type: none"> <li>• Control Charts               <ul style="list-style-type: none"> <li>- Assay</li> <li>- Contaminants</li> <li>- Dimensional Characteristics</li> </ul> </li> <li>• Certificate of Analysis for all Critical Parameters</li> </ul>   |
| Assembly Materials               | <ul style="list-style-type: none"> <li>• Visual Inspection</li> <li>• Physical Dimension Checks</li> <li>• Lead Integrity</li> <li>• Glass Composition</li> <li>• Bondability</li> <li>• Intermetallic Layer Adhesion</li> <li>• Ionic Contaminants</li> <li>• Thermal Characteristics</li> <li>• Lead Coplanarity</li> <li>• Plating Thickness</li> <li>• Hermeticity</li> </ul>   | <ul style="list-style-type: none"> <li>• Certificate of Analysis</li> <li>• Process Control Charts on Outgoing Product Checks and In-Line Process Controls</li> </ul>   |

## Manufacturing Science - CAM, JIT

In addition to SPC and DOX as key tools to control the product and processes, Harris is deploying other management mechanisms in the factory. On first examination, these tools appear to be directed more at schedules and capacity. However, they have a significant impact on quality results.

### Computer Aided Manufacturing (CAM)

CAM is a computer based inventory and productivity management tool which allows personnel to quickly identify production line problems and take corrective action. In addition, CAM improves scheduling and allows Harris to more quickly respond to changing customer requirements and aids in managing work in process (WIP) and inventories.

The use of CAM has resulted in significant improvements in many areas. Better wafer lot tracking has facilitated a number of process improvements by correlating yields to process variables. In several places CAM has greatly improved capacity utilization through better planning and scheduling. Queues have been reduced and cycle times have been shortened — in some cases by as much as a factor of 2.

The most dramatic benefit has been the reduction of WIP inventory levels, in one area by 500%. This results in fewer lots in the area and a resulting quality improvement. In wafer fab, defect rates are lower because wafers spend less time in production areas awaiting processing. Lower inventory also improves morale and brings a more orderly flow to the area. CAM facilitates all of these advantages.

### Just In Time (JIT)

A key adjunct to the CAM activity is Just In Time (JIT) material management. This is more than an inventory reduction technique: in many cases it involves reorganization of facilities and people. The essential concept is to form work units that are responsible for doing the whole job rather than bits of it. An employee has control over equipment, maintenance, cleanliness, scheduling, material, quality, and improvements.

In one Harris example, a photoresist flow consisting of several steps was previously organized in the classical departmentalized way. The inspection and etch areas were in different serial locations from the deposition and alignment areas. Work piled up at the slowest operation (inspection), and quality problems detected there were decoupled from the areas producing them by 20 to 30 feet and at least one day. Rework rates were very high; scrap was unacceptable.

When the area was reorganized into GT (group technology) cells (a basic concept of JIT), the inspection and alignment areas were physically coupled and people were organized into teams. The whole job (finished, defect-free wafers) was assigned to the GT cell (see Figure 3). Rework rates decreased 70%, scrap rates decreased 45%, and probe yields increased by 50%. This is only one of hundreds of examples of how JIT has improved our factory performance.

The JIT program/system works. This cultural change is vital and the benefits derived are impressive.

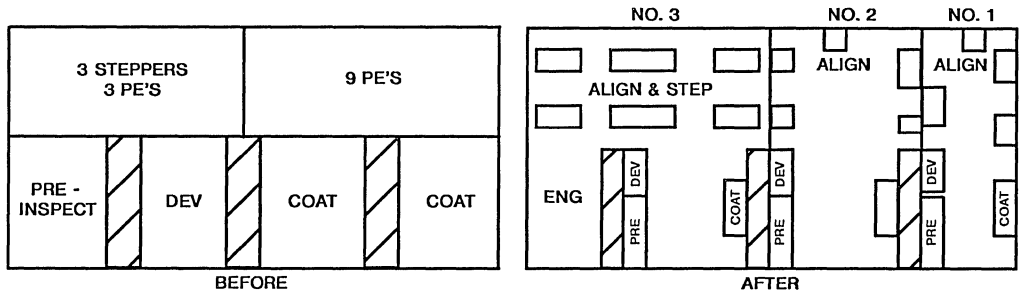


FIGURE 3. GROUP TECHNOLOGY CELL

10  
QUALITY AND  
RELIABILITY

## **Measurement**

### **Analytical Services Laboratory**

Harris facilities, engineering, manufacturing, and product assurance are supported by the Analytical Services Laboratory. Organized into chemical or microbeam analysis methodology, staff and instrumentation from both labs cooperate in fully integrated approaches necessary to complete analytical studies. The capabilities of each area are shown below.

**SPECTROSCOPIC METHODS:** Colorimetry, Optical Emission, Ultraviolet Visible, Fourier Transform-Infrared, Flame Atomic Absorption, Furnace Organic Carbon Analyzer, Mass Spectrometer.

**CHROMATOGRAPHIC METHODS:** Gas Chromatography, Ion Chromatography.

**THERMAL METHODS:** Differential Scanning Colorimetry, Thermogravimetric Analysis, Thermomechanical Analysis.

**PHYSICAL METHODS:** Profilometry, Microhardness, Rheometry.

**CHEMICAL METHODS:** Volumetric, Gravimetric, Specific Ion Electrodes.

**ELECTRON MICROSCOPE:** Transmission Electron Microscopy, Scanning Electron Microscope.

**X-RAY METHODS:** Energy Dispersive X-ray Analysis (SEM), Wavelength Dispersive X-ray Analysis (SEM), X-ray Fluorescence Spectrometry, X-ray Diffraction Spectrometry.

**SURFACE ANALYSIS METHODS:** Scanning Auger Microprobe, Electron Spectroscopy/Chemical Analysis, Secondary Ion Mass Spectrometry, Ion Scattering Spectrometry, Ion Microprobe.

The department also maintains ongoing working arrangements with commercial, university, and equipment manufacturers' technical service laboratories, and can obtain any materials analysis in cases where instrumental capabilities are not available in our own facility.

### **Calibration Laboratory**

Another important resource in the product assurance system is Harris Semiconductor's Calibration Lab. This area is responsible for calibrating the electronic, electrical, electro/mechanical, and optical equipment used in both the production and engineering areas. The accuracy of instruments used at Harris in calibration is traceable to the National Bureau of Standards. The lab maintains a system which conforms to the current revision of MIL-STD-45662, "Calibration System Requirements."

Each instrument requiring calibration is assigned a calibration interval based upon stability, purpose, and degree of use. The equipment is labeled with an identification tag on which is specified both the date of the last calibration and of the next required calibration. The Calibration Lab reports on a regular basis to each user

department. Equipment out of calibration is taken out of service until calibration is performed. The Quality organization performs periodic audits to assure proper control in the using areas. Statistical procedures are used where applicable in the calibration process.

### **Field Return Product Analysis System**

The purpose of this system is to enable Harris' Field Sales and Quality operations to properly route, track and respond to our customers' needs as they relate to product analysis.

The Product Failure Analysis Solution Team (PFAST) consists of the group of people who must act together to provide timely, accurate and meaningful results to customers on units returned for analysis. This team includes the salesman or applications engineer who gets the parts from the customer, the PFAST controller who coordinates the response, the Product or Test Engineering people who obtain characterization and/or test data, the analysts who failure analyze the units, and the people who provide the ultimate corrective action. It is the coordinated effort of this team, through the system described in this document that will drive the Customer responsiveness and continuous improvement that will keep Harris on the forefront of the semiconductor business.

The system and procedures define the processing of product being returned by the customer for analysis performed by Product Engineering, Reliability Failure Analysis and/or Quality Engineering. This system is designed for processing "sample" returns, not entire lot returns or lot replacements.

The philosophy is that each site analyzes its own product. This applies the local expertise to the solutions and helps toward the goal of quick turn time.

Goals: quick, accurate response, uniform deliverable (consistent quality) from each site, traceability.

The PFAST system is summarized in the following steps:

- 1) Customer calls the sales rep about the unit(s) to return.
- 2) Fill out PFAST Action Request - see the PFAST form in this section. This form is all that is required to process a Field Return of samples for failure analysis. This form contains essential information necessary to perform root cause analysis. (See copy of page 10-14).
- 3) The units must be packaged in a manner that prevents physical damage and prevents ESD. Send the units and PFAST form to the appropriate PFAST controller. This location can be determined at the field sales office or rep using "look-up" tables in the PFAST document.
- 4) The PFAST controller will log the units and route them to ATE testing for data log.
- 5) Test results will be reviewed and compared to customer complaint and a decision will be made to route the failure to the appropriate analytical group.

- 6) The customer will be contacted with the ATE test results and interim findings on the analysis. This may relieve a line down situation or provide a rapid disposition of material. The customer contact is valuable in analytical process to insure root cause is found.
- 7) A report will be written and sent directly to the customer with copies to sales, rep, responsible individuals with corrective actions and to the PFAST controller so that the records will capture the closure of the cycle.
- 8) Each report will contain a feedback form (stamped and preaddressed) so that the PFAST team can assess their performance based on the customers assessment of quality and cycle time.
- 9) The PFAST team objectives are to have a report in the customers hands in 28 days, or 14 days based on agreements. Interim results are given realtime.

#### Failure Analysis Laboratory

The Failure Analysis Laboratory's capabilities encompass the isolation and identification of all failure modes/failure mechanisms, preparing comprehensive technical reports, and assigning appropriate corrective actions. Research vital to understanding the basic physics of the failure is also undertaken.

Failure analysis is a method of enhancing product reliability and determining corrective action. It is the final and crucial step used to isolate potential reliability problems that may have occurred during reliability stressing. Accurate analysis results are imperative to assess effective corrective actions. To ensure the integrity of the analysis, correlation of the failure mechanism to the initial electrical failure is essential.

A general failure analysis procedure has been established in accordance with the current revision of MIL-STD-883, Section 5003. The analysis procedure was designed on the premise that each step should provide information on the failure without destroying information to be obtained from subsequent steps. The exact steps for an analysis are determined as the situation dictates. (See Figures 4 and 5). Records are maintained by laboratory personnel and contain data, the failure analyst's notes, and the formal Product Analysis Report.

### Reliability

#### Reliability Assessment and Enhancement

At Harris Semiconductor, reliability is built into every product by emphasizing quality throughout manufacturing. This starts by ensuring the excellence of the design, layout, and manufacturing process. The quality of the raw materials and workmanship is monitored using statistical process control (SPC) to preserve the reliability of the product. The primary and ultimate goal of these efforts is to provide full performance to the product specification throughout its useful life. Product reliability is maintained through the following sources: Qualifications, In-Line Reliability Monitors, Failure Analysis.

#### Qualifications

Qualifications at Harris de-emphasize the sole dependence on production product which is only available late in the development cycle. The focus is primarily on the use of test vehicles to establish design ground rules for the product and the process that will eliminate any wearout mechanisms during the useful life of the product. However, to comply with the military requirements concerning reliability, product qualifications are performed. (See Figure 6).

#### In-line Reliability Monitors

In-line reliability monitors provide immediate feedback to manufacturing regarding the quality of workmanship, quality of raw materials, and the ultimate reliability implications. The rudimentary implementation of this monitoring is the "First Line of Defense," which is a pass/fail acceptance procedure based on control charts and trend analysis. The second level of monitoring is referred to as the "Early Warning System" and incorporates wafer level reliability concepts for extensive diagnostic and characterization capabilities of various components that may impact the device reliability or stability. The quick feedback from these schemes allows more accurate correlation to process steps and corrective actions.

#### Product/Package Reliability Monitors

Reliability of finished product is monitored extensively under a program called Matrix I, II, III monitor. All major technologies are monitored.

**Matrix I** - Has a higher sampling size and rate per week and uses short duration test, usually less than 48 hours to assess day to day, week to week reliability. High volume types are prevalent in this data. Stresses - Operating Life, Static Life and HAST.  $T_A = +125^{\circ}\text{C}$  to  $+200^{\circ}\text{C}$

**Matrix II** - Longer duration test, much like requalification. The sample sizes are reduced in number and frequency, yet meet or exceed the JEDEC Standard 29. Stresses Operating Life, Storage, THB, Autoclave, Temp Cycle, and Thermal Shock.

**Matrix III** - Package specific test. Tests Solderability, Lead Fatigue, Physical Dimensions, Brand Adhesion, Flammability, Bond Pull, Constant Acceleration, and Hermeticity.

Data from these Monitor Stress Test provides the following information:

- Routine reliability monitoring of products by die technology and package styles.
- Data base for determining FIT Rates and Failures Mode trends used drive Continuous Improvement.
- Major source of reliability data for customers.
- Customers have used this data to qualify Harris products.





Request # \_\_\_\_\_  
 Customer Analysis # \_\_\_\_\_

## PFAST ACTION REQUEST

Date: \_\_\_\_\_

|  |   |
|--|---|
| ORIGINATOR _____<br>LOCATION/PHONE NO. _____<br>DEVICE TYPE/PART NO. _____<br>No. SAMPLES RETURNED _____ | CUSTOMER _____<br>LOCATION _____<br>PURCHASE ORDER NO. _____<br>QUANTITY RECEIVED _____ |
|--|---|

THE COMPLETENESS AND TIMELY RESPONSE OF THE EVALUATION IS DIRECTLY RELATED TO THE COMPLETENESS OF THE DATA PROVIDED. PLEASE PROVIDE ALL PERTINENT DATA. ATTACH ADDITIONAL SHEETS IF NECESSARY.

| TYPE OF PROBLEM  | DETAILS OF REJECT<br><small>(Where appropriate serialize units and specify for each)</small>   |
|--|--|
| <p>1. <input type="checkbox"/> INCOMING INSPECTION</p> <p style="margin-left: 20px;"><input type="checkbox"/> 100% SCREEN    <input type="checkbox"/> SAMPLE INSPECTION</p> <p style="margin-left: 20px;">No. TESTED _____ No. OF REJECTS _____</p> <p style="margin-left: 20px;">ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?</p> <p style="margin-left: 40px;"><input type="checkbox"/> YES            <input type="checkbox"/> NO</p> <p style="margin-left: 20px;"><input type="checkbox"/> BRIEF DESCRIPTION OF EVALUATION AND RESULTS ATTACHED</p> <p>2. <input type="checkbox"/> IN PROCESS/MANUFACTURING FAILURE</p> <p style="margin-left: 20px;"><input type="checkbox"/> BOARD CHECKOUT    <input type="checkbox"/> SYSTEM CHECKOUT</p> <p style="margin-left: 20px;"><input type="checkbox"/> FAILED ON TURN-ON</p> <p style="margin-left: 20px;"><input type="checkbox"/> FAILED AFTER _____ HOURS OPERATION</p> <p style="margin-left: 20px;">WAS UNIT RETESTED UNDER INCOMING INSPECTION CONDITIONS?    <input type="checkbox"/> YES    <input type="checkbox"/> NO</p> <p style="margin-left: 20px;"><input type="checkbox"/> BRIEF DESCRIPTION OF HOW FAILURE WAS ISOLATED TO COMPONENT ATTACHED</p> <p>3. <input type="checkbox"/> FIELD FAILURE</p> <p style="margin-left: 20px;">FAILED AFTER _____ HOURS OPERATION</p> <p style="margin-left: 20px;">ESTIMATED FAILURE RATE _____% PER 1000 HOURS</p> <p style="margin-left: 20px;">END USER _____ LOCATION _____</p> <p style="margin-left: 20px;">AMBIENT TEMPERATURE _____ C</p> <p style="margin-left: 20px;">MIN. _____ C            MAX. _____ C</p> <p style="margin-left: 20px;">REL. HUMIDITY _____%</p> <p style="margin-left: 20px;"><input type="checkbox"/> END USER FAILURE CORRESPONDENCE ATTACHED</p> | <p>TEST CONDITIONS RELATING TO FAILURE</p> <p style="margin-left: 20px;"><input type="checkbox"/> TESTER USED (MFR/MODEL) _____</p> <p style="margin-left: 20px;"><input type="checkbox"/> TEST TEMPERATURE _____</p> <p style="margin-left: 20px;"><input type="checkbox"/> TEST TIME:    <input type="checkbox"/> CONTINUOUS TEST</p> <p style="margin-left: 40px;">                                  <input type="checkbox"/> ONE SHOT (T = _____ SEC)</p> <p style="margin-left: 20px;"><input type="checkbox"/> DESCRIPTION OF ANY OBSERVED CONDITION TO WHICH FAILURE APPEARS SENSITIVE: _____</p> <hr/> <p>1. <input type="checkbox"/> DC FAILURES</p> <p style="margin-left: 20px;"><input type="checkbox"/> OPENS    <input type="checkbox"/> SHORTS    <input type="checkbox"/> LEAKAGE    <input type="checkbox"/> STRESS</p> <p style="margin-left: 20px;"><input type="checkbox"/> POWER DRAIN    <input type="checkbox"/> INPUT LEVEL    <input type="checkbox"/> OUTPUT LEVEL</p> <p style="margin-left: 20px;"><input type="checkbox"/> LIST OF FORCING CONDITIONS AND MEASURED RESULTS FOR EACH PIN IS ATTACHED</p> <p style="margin-left: 20px;"><input type="checkbox"/> POWER SUPPLY SEQUENCING ATTACHED</p> <p>2. <input type="checkbox"/> AC FAILURES</p> <p style="margin-left: 20px;">LIST FAILING CHARACTERISTICS _____</p> <hr/> <p style="margin-left: 20px;">ADDRESS OF FAILING LOCATION (IF APPLICABLE)</p> <hr/> <p>ATTACHED:</p> <p style="margin-left: 20px;"><input type="checkbox"/> LIST OF POWER SUPPLY AND DRIVER LEVELS (Include pictures of waveforms).</p> <p style="margin-left: 20px;"><input type="checkbox"/> LIST OF OUTPUT LEVELS AND LOADING CONDITIONS</p> <p style="margin-left: 20px;"><input type="checkbox"/> INPUT AND OUTPUT TIMING DIAGRAMS</p> <p style="margin-left: 20px;"><input type="checkbox"/> DESCRIPTION OF PATTERNS USED (If not standard patterns, give very complete description including address sequence).</p> <p>3. <input type="checkbox"/> PROM PROGRAMMING FAILURES</p> <p style="margin-left: 20px;">ADDRESS OF FAILURES _____</p> <p style="margin-left: 20px;">PROGRAMMER USED (MFG/MODEL/REV. No.) _____</p> <hr/> <p>4. <input type="checkbox"/> PHYSICAL/ASSEMBLY RELATED FAILURES</p> <p style="margin-left: 20px;"><input type="checkbox"/> SEE COMMENTS BELOW    <input type="checkbox"/> SEE ATTACHED</p> |
| <b>ACTION REQUESTED BY CUSTOMER</b>  |  |
| SPECIFIC ACTION REQUESTED _____<br>IMPACT OF FAILED UNITS ON CUSTOMER'S SITUATION: _____<br>_____<br>CUSTOMER CONTACTS WITH SPECIFIC KNOWLEDGE OF REJECTS<br>NAME _____<br>POSITION _____ PHONE _____  |  |

Additional Comments:

## Reliability Fundamentals

Reliability, by its nature, is a mixture of engineering and probability statistics. This combination has derived a vocabulary of terms essential for describing the reliability of a device or system. Since reliability involves a measurement of time, it is necessary to accelerate the failures which may occur. This, then, introduces terms like "activation

energy" and "acceleration factor," which are needed to relate results of stressing to normal operating conditions (see Table 7). Also, to assess product reliability requires failures. Therefore, only a statistical sample can be used to determine the model of the failure distribution for the entire population of product.

TABLE 7. FAILURE RATE PRIMER

### GLOSSARY OF TERMS

| TERMS/DEFINITION   | UNITS/DESCRIPTION  |
|--|--|
| <p><b>FAILURE RATE <math>\lambda</math></b></p> <p>For Semiconductors, usually expressed in FITs.</p> <p>Represents useful life failure rate (which implies a constant failure rate).</p> <p>FITs are not applicable for infant mortality or wearout failure rate expressions.</p> | <p><b>FIT - Failure In Time</b></p> <p>1 FIT - 1 failure in <math>10^9</math> device hours.<br/>Equivalent to 0.0001%/1000 hours</p> <p>FITs = <math display="block">\frac{\# \text{ Failures}}{\# \text{ Devices} \times \# \text{ hours stress} \times \text{AF}} \times 10^9 \times m</math></p> <p><math>m</math> - Factor to establish Confidence Interval<br/> <math>10^9</math> - Establishes in terms of FITs<br/>           AF - Acceleration Factor at temperature for a given failure mechanism</p> |
| <p><b>MTTF - Mean Time To Failure</b></p> <p>For semiconductors, MTTF is the average or mean life expectancy of a device.</p> <p>If an exponential distribution is assumed then the mean time to fail of the population will be when 63% of the parts have failed.</p>             | <p>Mean Time is measured usually in hours or years.</p> <p>1 Year = 8760 hours</p> <p>When working with a constant failure rate the MTTF can be calculated by taking the reciprocal of the failure rate.</p> <p><math>MTTF = 1/\lambda</math> (exponential model)</p> <p>Example: =10 FITs at +55°C</p> <p>The MTTF is: <math>MTTF = 1/\lambda = 0.1 \times 10^9</math> hours<br/>= 100M hours</p>   |
| <p><b>CONFIDENCE INTERVAL (C. I.)</b></p> <p>Establishes a Confidence Interval for failure rate predictions. Usually the upper limit is most significant in expressing failure rates.</p>  | <p>Example:</p> <p>"10 FITs @ a 95% C. I. @ 55°C" means <i>only</i> that you are 95% certain the the FITs &lt;10 at +55°C use conditions.</p>  |

### Failure Rate Calculations

Reliability data for products may be composed of several different failure mechanisms and requires careful combining of diverse failure rates into one comprehensive failure rate. Calculating the failure rate is further complicated because failure mechanisms are thermally accelerated at varying rates and thereby have differing accelerating factors. Additionally, this data is usually obtained a variety of life tests at unique stress temperatures. The equation below accounts for these considerations and then inserts a statistical factor to obtain the confidence interval for the failure rate.

$$FIT = \left( \frac{B}{\sum_{i=1}^B \frac{X_i}{K \sum_{j=1}^{TDH_j} AF_{ij}}} \right) \times 10^9 \times M$$

- B = # of distinct possible failure mechanisms
- K = # of life tests being combined
- X<sub>i</sub> = # of failures for a given failure mechanism i = 1, 2, . . . B
- TDG<sub>j</sub> = Total device hours of test time (unaccelerated) for Life Test<sub>j</sub>
- AF<sub>ij</sub> = Acceleration factor for appropriate failure mechanism i = 1, 2, . . . K
- M = Statistical factor for calculating the upper confidence limit (M is a function of the total number of failures and an estimate of the standard deviation of the failure rates)

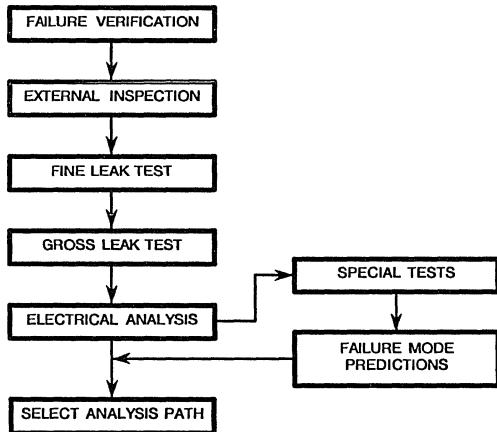


FIGURE 4. NON-DESTRUCTIVE

In the failure rate calculation, Acceleration Factors (AF<sub>ij</sub>) are used to derate the failure rate from thermally accelerated Life Test conditions to a failure rate indicative of use temperatures. Though no standards exist, a temperature of +55°C has been popular and allows some comparison of product failure rates. All Harris Semiconductor Reliability Reports will derate to +55°C at both the 60% and 95% confidence intervals.

### Acceleration Factors

The Acceleration Factors (AF) are determined from the Arrhenius Equation. This equation is used to describe physiochemical reaction rates and is an appropriate model for expressing the thermal acceleration of semiconductor failure mechanisms.

$$AF = \text{EXP} \left[ \frac{E_a}{K} \left( \frac{1}{T_{\text{use}}} - \frac{1}{T_{\text{stress}}} \right) \right]$$

- AF = Acceleration Factor
- E<sub>a</sub> = Thermal Activation Energy in eV from Table 8
- K = Boltzmann's Constant (8.62 x 10<sup>-5</sup> eV/°K)

Both T<sub>use</sub> and T<sub>stress</sub> (in degrees Kelvin) include the internal temperature rise of the device and therefore represent the junction temperature. With the use of the Arrhenius Equation, the thermal Activation Energy (E<sub>a</sub>) term is a major influence on the result. This term is usually empirically derived and can vary widely.

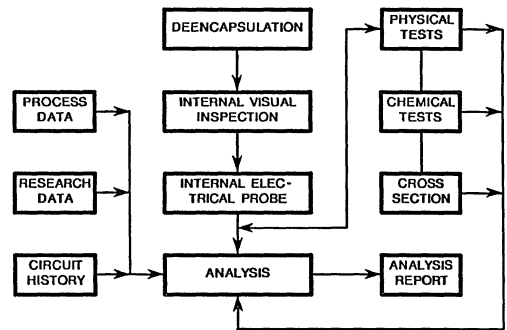


FIGURE 5. DESTRUCTIVE

## Activation Energy

To determine the Activation Energy ( $E_a$ ) of a mechanism (see Table 8) you must run at least two (preferably more) tests at different stresses (temperature and/or voltage). The stresses will provide the time to failure ( $T_f$ ) for the populations which will allow the simultaneous solution for the Activation Energy by putting the experimental results into the following equations.

$$\ln(t_{f1}) = C + \frac{E_a}{KT_1}$$

$$\ln(t_{f2}) = C + \frac{E_a}{KT_2}$$

Then, by subtracting the two equations, the Activation Energy becomes the only variable, as shown.

$$\ln(t_{f1}) - \ln(t_{f2}) = E_a/k(1/T_1 - 1/T_2)$$

$$E_a = K^* ((\ln(t_{f1}) - \ln(t_{f2})) / (1/T_1 - 1/T_2))$$

The Activation Energy may be estimated by graphical analysis plots. Plotting  $\ln$  time and  $\ln$  temperature then provides a convenient nomogram that solves (estimates) the Activation Energy.

Table 9 is a summary of military generic groups by process descriptions.

All Harris Reliability Reports from qualifications and Group C1 (all high temperature operating life tests) will provide the data on all factors necessary to calculate and verify the reported failure rate (in FITs) using the methods outlined in this primer.

TABLE 8. FAILURE MECHANISM

| FAILURE MECHANISM                          | ACTIVATION ENERGY | SCREENING AND TESTING METHODOLOGY   | CONTROL METHODOLOGY  |
|--|-------------------|---|--|
| Oxide Defects                              | 0.3 - 0.5eV       | High temperature operating life (HTOL) and voltage stress. Defect density test vehicles.        | Statistical Process Control of oxide parameters, defect density control, and voltage stress testing.                                 |
| Silicon Defects (Bulk)                     | 0.3 - 0.5eV       | HTOL & voltage stress screens.  | Vendor Statistical Quality Control programs, and Statistical Process Control on thermal processes.                                   |
| Corrosion                                  | 0.45eV            | Highly accelerated stress testing (HAST)  | Passivation dopant control, hermetic seal control, improved mold compounds, and product handling.                                    |
| Assembly Defects                           | 0.5 - 0.7eV       | Temperature cycling, temperature and mechanical shock, and environmental stressing.             | Vendor Statistical Quality Control programs, Statistical Process Control of assembly processes proper handling methods.              |
| Electromigration<br>- Al Line<br>- Contact | 0.6eV<br>0.9eV    | Test vehicle characterizations at highly elevated temperatures.                                 | Design ground rules, wafer process statistical process steps, photoresist, metals and passivation                                    |
| Mask Defects/<br>Photoresist<br>Defects    | 0.7eV             | Mask FAB comparator, print checks, defect density monitor in FAB, voltage stress test and HTOL. | Clean room control, clean mask, pellicles<br>Statistical Process Control or photoresist-<br>/etch processes.                         |
| Contamination                              | 1.0eV             | C-V stress at oxide/interconnect, wafer FAB device stress test (EWS) and HTOL.                  | Statistical Process Control of C-V data, oxide/<br>interconnect cleans, high integrity glassivation<br>and clean assembly processes. |
| Charge Injection                           | 1.3eV             | HTOL & oxide characterization.  | Design ground rules, wafer level Statistical<br>Process Control and critical dimensions for<br>oxides.                               |

## Qualification Procedures

New products are reliably introduced to market by the proper use of design techniques and strict adherence to process layout ground rules. Each design is reviewed from its conception through early production to ensure compliance to minimum failure rate standards. Ongoing monitoring of reliability performance is accomplished through compliance to 883C and standard Quality Conformance Inspection as defined in Method 5005.

New process/product qualifications have two major requirements imposed. First is a check to verify the proper use of process methodology, design tech-

niques, and layout ground rules. Second is a series of stress tests designed to accelerate failure mechanisms and demonstrate the reliability of integrated circuits.

From the earliest stages of a new product's life, the design phase, through layout, and in every step of the manufacturing process, reliability is an integral part of every Harris Semiconductor product. This kind of attention to detail "from the ground up" is the reason why our customers can expect the highest quality for any application.

TABLE 9. HIGH TEMPERATURE OPERATING LIFE TEST SUMMARY

### GROUP C

| GENERIC GROUP | GROUP NAME                     | PROCESS DESCRIPTION                     | QUANTITY | QUANTITY FAILURE | HOURS @ 125°C | FAILURE RATE FITs @ 55°C 60% CI |
|---------------|--------------------------------|---|----------|------------------|---------------|---------------------------------|
| D-49-3        | Op. Amplifiers                 | Std. Linear, DI w/NiCr resistors        | 3482     | 6                | 3,215,708     | 62                              |
| D-49-4        | Op. Amplifiers                 | Std. Linear, DI w/NiCr resistors        | 324      | 1                | 429,945       | 17                              |
| D-53          | High Voltage Op. Amplifiers    | High voltage DI                         | 315      | 0                | 284,943       | 20                              |
| D-56          | Data Acquisition               | High beta high frequency, DI, NiCr      | 1022     | 5                | 1,868,349     | 100                             |
| F-103         | Telecommunications             | SAJI IVA                                | 199      | 0                | 403,960       | 5                               |
| F-81-3        | A/D Converters                 | SAJI IVA                                | 201      | 0                | 183,222       | 10                              |
| F-81-4        | A/D Converters                 | SAJI IVA                                | 217      | 1                | 328,000       | 12                              |
| F-82          | Switches & Mux                 | DI AI Gate & Si Gate MOS                | 121      | 0                | 82,836        | 23                              |
| F-99-3        | Active Filters                 | SAJI IVA                                | 196      | 1                | 184,262       | 24                              |
| F-99-4        | Active Filters                 | SAJI IVA                                | 407      | 1                | 470,324       | 9                               |
| G-85          | Op. Amplifiers                 | Std. Linear, MOS, & High Frequency JFET | 532      | 1                | 535,728       | 11                              |
| G-86          | Comparators                    | Combination, Std. Linear & MOS          | 154      | 0                | 153,400       | 25                              |
| G-94-3        | Switches & Mux                 | DI AI & Si Gate Linear CMOS             | 4351     | 41               | 7,443,054     | 103                             |
| G-94-4        | Switches & Mux                 | DI AI & Si Gate Linear CMOS             | 906      | 0                | 889,816       | 20                              |
| C-41-4        | CMOS RAMs                      | SAJI CMOS                               | 2418     | 19               | 2,247,526     | 31                              |
| C-41-5        | CMOS RAMs                      | SAJI CMOS                               | 1104     | 10               | 1,105,094     | 53                              |
| C-42-4        | CMOS PROMs & HPALS             | SAJI CMOS                               | 2645     | 28               | 4,074,728     | 61                              |
| C-105-4       | Microprocessor and Peripherals | SAJI CMOS                               | 3638     | 12               | 4,099,002     | 17                              |

NOTE: All infant mortality failures (up to 168 hours or equivalent) have been removed from products sampled.

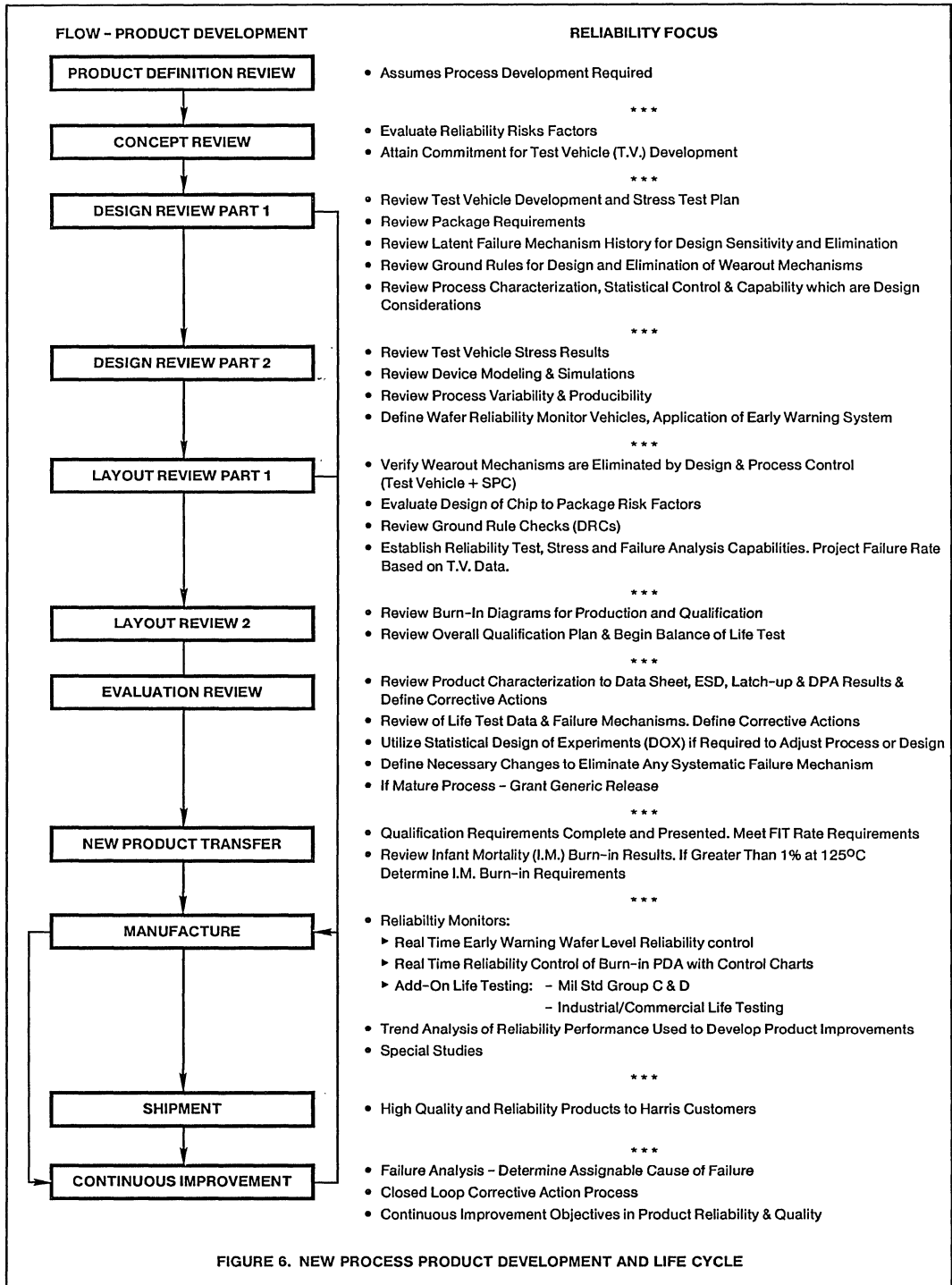


FIGURE 6. NEW PROCESS PRODUCT DEVELOPMENT AND LIFE CYCLE



## APPLICATION NOTE ABSTRACTS

| AN# | TITLE  | ABSTRACTS  |
|-----|--|--|
| 509 | A Simple Comparator Using The HA-2620                                  | Performance characteristics, application schematics, output parameter control methods.   |
| 514 | The HA-2400 PRAM Four Channel Operational Amplifier                    | HA-2400 PRogrammable Analog Microcircuit description, frequency compensation, applications (analog multiplexer, non-inverting programmable gain amplifier, inverting programmable gain amplifier, programmable attenuator, programmable adder-subtractor, phase selector, phase detector, synchronous rectifier, balanced modulator, integrator, ramp generator, track and hold, sample and hold, sine wave oscillator, multivibrator, active filter, programmable power supply, comparator, multiplying D/A converter). |
| 515 | Operational Amplifier Stability: Input Capacitance Considerations      | Input capacitance and stability, capacitive feedback compensation, guidelines for compensation requirements.   |
| 517 | Applications of a Monolithic Sample and Hold/ Gated Op Amp             | General Sample and Hold information and fourteen specific applications, including filtered Sample & Hold DAC de-glitcher, Integrate-Hold-Reset, gated op amp, etc.   |
| 519 | Operational Amplifiers Noise Prediction.                               | Noise model and equations, procedure for computing total output noise, example, broadband noise measurement, spot noise prediction techniques, typical spot noise curves, popcorn noise discussion.  |
| 525 | HA-5190/5195 Fast Settling Operational Amplifier                       | Internal schematic, prototyping considerations, frequency compensation, performance enhancement methods, applications.   |
| 526 | HA-5190/5195 Video Applications  | Video applications, video response tests, S/N ratio measurements, power supply requirements temperature considerations, design hints, prototyping tips, RF AGC amplifier, DC gain controlled video amplifier.  |
| 538 | Monolithic Sample/Hold Combines Speed and Precision                    | Description and electrical specifications for the HA-5320 Sample/Hold Amplifiers, explanation of errors sources, and HA-5320 applications.   |
| 540 | HA-5170 Precision Low Noise J-FET Input Operational Amplifier          | Internal design and technology, J-FET noise discussion, trimming of offset voltage, single op amp Instrumentation Amplifier, sine wave oscillator, high impedance transducer interface, current source/sink and current sense circuits.  |
| 541 | Using HA-2539/2540 Very High Slew-Rate Wideband Operational Amplifiers | Prototyping considerations, output short circuit protection, offset voltage adjustment, frequency compensation, composite amplifier scheme, DC error reduction, boosting output current, increasing output signal swing, cascade amplifier, video gain block, high frequency oscillator, wideband signal splitter.   |
| 544 | Micropower Op Amp Family, HA-514X,                                     | Operation, noise performance, applications (remote sensor loop transmitter, charge pool power supply, low power microphone preamplifier, AGC with squelch control, Wein bridge oscillator, bar code scanner, monostable multivibrator).  |



## Application Note Abstracts (Continued)

| AN# | TITLE  | ABSTRACTS  |
|-----|--|--|
| 546 | A Method of Calculating HA-2625 Gain Bandwidth Product vs. Temperature | A method of calculating Gain Bandwidth product performance versus temperature for the HA-2625 Op Amp.  |
| 548 | A Designer's Guide for the HA-5033 Video Buffer                        | Operation, video performance, video parameter specifications, Y parameters, applications (flash converter pre-driver, coaxial line driver, video gain block, high speed sample and hold, audio drivers, crystal oscillator).   |
| 549 | The HC-550X Telephone Subscriber Line Interface Circuit                | Complete description of device functionality and applications of SLIC.   |
| 550 | Using the HA-2541  | Prototyping guidelines, thermal considerations and heat sinking, performance enhancements, applications (Wein bridge oscillator, high power gain stage, video stage with clamp, multiplexer/demultiplexer, disk drive write amplifier, gain programmable amp, composite amp).  |
| 551 | Recommended Test Procedures for Operational Amplifiers                 | Operational amplifier test procedures for offset voltage, bias current, offset current, power supply rejection ratio, common mode rejection ratio, output voltage swing, output current, open loop gain, slew rate, full power bandwidth, transient response, settling time, GBP, phase margin, noise voltage and current, and channel separation. |
| 552 | Using the HA-2542  | Prototyping guidelines, thermal considerations and heat sinking, performance enhancements, applications (multi-channel security system, unbalanced coaxial driver, flash converter driver, programmable power supply, bridge load driver, high current stage, differential line driver, DC motor speed control).                                   |
| 553 | Using the HA-5147/5137/5127  | Construction and operation, low noise design applications (instrumentation amplifier bridge sensor, multiplexer, precision threshold detector, audio driver, NAB amplifier, multivibrator, programmable gain stage, log amp, professional mixer).  |
| 554 | Low Noise Family HA-5101/5102/5104/5112/5114                           | Low noise design, operation, applications (Electronic scales, programmable attenuator, Baxandall circuit, RIAA amplifier, NAB preamplifier, microphone amplifier, standard and simple biquads, professional mixer).  |
| 556 | Thermal Safe-Operating-Areas for High Current Op Amps                  | Thermal management equations and curves indicating areas of $V_{OUT}$ and $I_{OUT}$ safe operation. Also, the effects of packaging and heat sinking are examined.  |
| 558 | Using the HV1205 AC to DC Converter                                    | Explains the basic theory of operation of the HV-1205. Presents a discussion of external components required for operation, PC board layout recommendations and safety considerations  |
| 571 | Using Ring Sync with HC-5502A and HC5504 SLICs                         | Describes use of the SLICs Ring Synchronization pin and why you should use it.   |
| 573 | The HC-5560 Digital Line Transcoder                                    | Full functional and applications description of HC-5560 transcoder and line codes.   |
| 574 | Understanding PCM Coding   | The process of converting analog voice signals into Time Division Multiplexed (TDM) Pulse Code Modulated (PCM) format is described and illustrated.  |
| 607 | Delta Modulation for Voice Transmission                                | Introduction to delta modulation coding techniques, 4 general applications, including digital transmission encryption, voice scrambling and audio delay. Also CVSD evaluation guidelines.  |

## Application Note Abstracts (Continued)

| AN #     | TITLE  | ABSTRACTS   |
|----------|--|---|
| 9006     | HV-2405E Operation from Full Bridge                                  | A brief discussion of function of the source resistor ( $R_1$ ) and the benefits of using a bridge rectifier to reduce the power dissipation in $R_1$ . Presents several points to be kept in mind when implementing the full bridge (i.e. safety aspects, filtering of output so device will reset for the next cycle and circuit operation verification with test equipment). |
| 9101     | High Current Off Line Power Supply                                   | Explains the basic theory of operation of the HV-1205/2405E and show how to increase the maximum output current from 50mA to greater than 250mA. A detailed description of the circuit operation, to achieve the higher currents, is presented along with suggestions for external component selection.   |
| A007     | Using the 8048/8049 Monolithic Log-Anti-Log Amplifier                | Describes in detail the operation of the 8048 logarithmic amplifier, and its counterpart, the 8049 anti-log amp.  |
| A013     | Everything You Always Wanted to Know About the 8038                  | This note includes 17 of the most asked questions regarding the use of the 8038.  |
| A027     | Power Supply Design Using the ICL8211 and ICL8212                    | Explains the operation of the ICL8211/12 and describes various power supply configurations. Included are positive and negative voltage regulators, constant current source, programmable current source, current limiting, voltage crowbar, power supply window detector, etc.  |
| A040     | A Precision Four Quadrant Multiplier-The 8013                        | Describes, in detail, the operation of the 8013 analog multiplier. Included are multiplication, division, and square root applications.   |
| A051     | Principles and Applications of the ICL7660 CMOS Voltage Converter    | Describes internal operation of the ICL7660. Includes a wide range of possible applications.  |
| A053     | The ICL7650 - A New Era in Glitch-Free Chopper Stabilizer Amplifiers | A brief discussion of the internal operation of the ICL7650, followed by an extensive applications section including amplifiers, comparators, log-amps, pre-amps, etc.  |
| ICAN5290 | General Purpose Op Amps  | Discusses various uses of op amps   |
| ICAN5296 | CA3018   | Transistor Array  |
| ICAN5337 | CA3028   | RF amplifiers in the HF and VHF ranges.   |
| ICAN5380 | FM IF Amplifiers   | Discusses differential amplifier configurations.  |
| ICAN5766 | CA3020   | Multipurpose wideband power amplifiers  |
| ICAN6048 | CA3094   | Programmable power switch/amplifier.  |
| ICAN6077 | CA3094   | OTA with power capability.  |
| ICAN6157 | CA3085   | Monolithic voltage regulators.  |
| ICAN6182 | CA3059   | Zero-voltage switches.  |
| ICAN6247 | CA3126   | Chroma processing IC using sample and hold circuit techniques.  |

## Application Note Abstracts (Continued)

| AN #     | TITLE                    | ABSTRACTS   |
|----------|--------------------------|---|
| ICAN6257 | CA3089                   | FM IF Subsystem.  |
| ICAN6386 | CA3130                   | Understanding BiMOS op amps.  |
| ICAN6459 | CA3130                   | Why and how to use the BiMOS op amp.  |
| ICAN6472 | CA3126                   | A chrominance demodulator IC with dynamic flesh correction.                               |
| ICAN6525 | IC Handling              | Guide to IC handling.   |
| ICAN6668 | CA3080                   | High performance OTA.   |
| ICAN6669 | CA3240                   | BiMOS op amp mates directly to system sensors.  |
| ICAN6732 | Noise Measurement        | Measurement of burst noise and "popcorn" noise in ICs.                                    |
| ICAN6818 | CA3280                   | OTA simplifies complex analog designs.  |
| ICAN6915 | CA1524                   | Pulse-width modulators.   |
| ICAN6998 | Telecom                  | Telephony in Digital Evolution.   |
| ICAN7037 | Telecom                  | Logarithmic units of measure in telecommunications.                                       |
| ICAN7127 | CA3420                   | BiMOS amplifier circumvents low voltage limitations.                                      |
| ICAN7174 | CA1524                   | Pulse-width modulator in an electronic scale.   |
| ICAN7175 | CA3217                   | Integrated NTSC chrominance/luminance processor   |
| ICAN7304 | SCR Protection           | Discusses SCR Protection Circuits for ICs.  |
| ICAN8636 | Video Devices            | Discusses advanced video speed switches, multiplexers, crosspoints and buffer amplifiers. |
| ICAN8707 | CA3450                   | Single chip video line driver-high speed op amp.  |
| ICAN8742 | CD22402                  | Sync Generator  |
| ICAN8811 | CA5470                   | BiMOS-E process enhances quad op amp.   |
| ICE-402  | Operating Considerations | Discusses operating considerations for solid state devices.                               |

Harris Analog Spice Macro-Models available upon request.

## PACKAGING AND ORDERING INFORMATION

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# SOIC Packaging Information

## Commercial Signal Processing Linear Products Offered in SOIC

This table is provided as a guide for selecting devices which are available in Small Outline Packages. Enhanced electrical grades of these devices are available, or planned, as standard offerings. Devices in development at the time of printing

are included for future consideration, and are denoted by an \*\*. Please consult your nearest Harris Sales Office, Representative or Distributor for the most current information on packaging and availability.

### LINEAR SOIC PRODUCT OFFERINGS

| PRODUCT                              | DESCRIPTION                | LEAD COUNT | BODY WIDTH (MILS) | OPERATING TEMPERATURE (°C) |         |         |          |
|--------------------------------------|----------------------------|------------|-------------------|----------------------------|---------|---------|----------|
|                                      |                            |            |                   | 0/+70                      | -25/+85 | -40/+85 | -55/+125 |
| <b>SINGLE OPERATIONAL AMPLIFIERS</b> |                            |            |                   |                            |         |         |          |
| CA3078                               | Micropower Bipolar         | 8          | 150               | X                          | -       | -       | X        |
| CA3080                               | Transconductance Amplifier | 8          | 150               | X                          | -       | -       | X        |
| CA3100                               | Broadband BiMOS            | 8          | 150               | -                          | -       | X       | -        |
| CA3130                               | General Purpose BiMOS      | 8          | 150               | -                          | -       | X       | -        |
| CA3140                               | General Purpose BiMOS      | 8          | 150               | -                          | -       | -       | X        |
| CA3440 *                             | Nano Power BiMOS           | 8          | 150               | -                          | -       | -       | X        |
| CA5130                               | General Purpose +5V BiMOS  | 8          | 150               | -                          | X       | -       | X        |
| CA5130A *                            | General Purpose +5V BiMOS  | 8          | 150               | -                          | -       | -       | X        |
| CA5160 *                             | General Purpose +5V BiMOS  | 8          | 150               | -                          | -       | -       | X        |
| CA5420 *                             | Low Bias +5V BiMOS         | 8          | 150               | -                          | -       | -       | X        |
| HA-2525                              | High Slew Rate             | 8          | 150               | X                          | -       | X       | -        |
| HA-2529                              | High Slew Rate High Output | 8          | 150               | X                          | -       | X       | -        |
| HA-2539                              | Broadband High Slew Rate   | 14         | 150               | X                          | -       | X       | -        |
| HA-2540                              | Broadband Fast Settling    | 14         | 150               | X                          | -       | X       | -        |
| HA-2544                              | Video Unity Gain           | 8          | 150               | X                          | -       | X       | -        |
| HA-2548 *                            | Precision High Speed       | 8          | 150               | X                          | -       | -       | -        |
| HA-2605                              | General Purpose            | 8          | 150               | X                          | -       | X       | -        |
| HA-2625                              | Broadband                  | 8          | 150               | X                          | -       | X       | -        |
| HA-2839 *                            | High Slew Rate             | 8          | 150               | X                          | -       | X       | -        |
| HA-2840                              | High Slew Rate             | 8          | 150               | X                          | -       | X       | -        |
| HA-2841                              | Wideband Fast Settling     | 8          | 150               | X                          | -       | X       | -        |
| HA-2842                              | Wideband High Slew Rate    | 14         | 150               | X                          | -       | X       | -        |
| HA-5020                              | 100MHz Current Feedback    | 8          | 150               | X                          | -       | -       | -        |
| HA-5101                              | Low Noise Unity Gain       | 8          | 150               | X                          | -       | X       | -        |
| HA-5111                              | Low Noise Broadband        | 8          | 150               | X                          | -       | X       | -        |
| HA-5221 *                            | Broadband Precision        | 8          | 150               | X                          | -       | X       | -        |
| HA-5195                              | Fast Settling Wideband     | 14         | 150               | X                          | -       | X       | -        |
| HA-7712 *                            | Low Power Precision BiMOS  | 8          | 150               | X                          | -       | X       | -        |
| HA-7713 *                            | Low Power Precision BiMOS  | 8          | 150               | X                          | -       | X       | -        |
| HFA-0001 *                           | Ultra High Slew Rate       | 16         | 300               | X                          | -       | X       | -        |
| HFA-0002 *                           | Ultra Wideband Low Noise   | 8          | 150               | X                          | -       | X       | -        |
| HFA-0005 *                           | Ultra Wideband Unity Gain  | 8          | 150               | X                          | -       | X       | -        |
| ICL7611                              | Prog. Low Power CMOS       | 8          | 150               | X                          | -       | -       | -        |
| ICL7612                              | Prog. Low Power CMOS       | 8          | 150               | X                          | -       | -       | -        |
| <b>DUAL OPERATIONAL AMPLIFIERS</b>   |                            |            |                   |                            |         |         |          |
| CA158                                | General Purpose            | 8          | 150               | -                          | -       | -       | X        |
| CA2904                               | General Purpose            | 8          | 150               | -                          | -       | X       | -        |
| HA-5102                              | Low Noise Unity Gain       | 16         | 300               | X                          | -       | X       | -        |
| HA-5112                              | Low Noise Broadband        | 16         | 300               | X                          | -       | X       | -        |
| HA-5142                              | Low Power Bipolar          | 16         | 300               | X                          | -       | X       | -        |
| HA-5222 *                            | Broadband Precision        | 16         | 300               | X                          | -       | X       | -        |
| HA-5232 *                            | Low Cost Precision         | 16         | 300               | X                          | -       | -       | -        |
| ICL7621                              | Low Power CMOS             | 8          | 150               | X                          | -       | -       | -        |

\* Product in Development, Lead Count and Body Dimensions May Change.

**LINEAR SOIC PRODUCT OFFERINGS (Continued)**

| PRODUCT                                | DESCRIPTION                       | LEAD COUNT | BODY WIDTH (MILS) | OPERATING TEMPERATURE (°C) |         |         |          |
|--|-----------------------------------|------------|-------------------|----------------------------|---------|---------|----------|
|  |                                   |            |                   | 0/+70                      | -25/+85 | -40/+85 | -55/+125 |
| <b>QUAD OPERATIONAL AMPLIFIERS</b>     |                                   |            |                   |                            |         |         |          |
| CA124                                  | General Purpose                   | 14         | 150               | -                          | -       | -       | X        |
| CA5470                                 | Broadband +5V BiMOS               | 14         | 150               | -                          | -       | -       | X        |
| HA-4741                                | General Purpose                   | 16         | 300               | X                          | -       | X       | -        |
| HA-5104                                | Low Noise Unity Gain              | 16         | 300               | X                          | -       | X       | -        |
| HA-5114                                | Low Noise Broadband               | 16         | 300               | X                          | -       | X       | -        |
| HA-5144                                | Low Power Bipolar                 | 16         | 300               | X                          | -       | X       | -        |
| HA-5234*                               | Low Cost Precision                | 16         | 300               | X                          | -       | -       | -        |
| LM2902                                 | General Purpose                   | 14         | 150               | -                          | -       | X       | -        |
| <b>DIFFERENTIAL AMPLIFIERS</b>         |                                   |            |                   |                            |         |         |          |
| CA3028                                 | Differential/Cascode              | 8          | 150               | -                          | -       | -       | X        |
| CA3053                                 | Differential/Cascode              | 8          | 150               | -                          | -       | -       | X        |
| CA3054                                 | Transistor Array Dual Independent | 14         | 150               | -                          | -       | X       | -        |
| CA3102                                 | Dual High Frequency               | 14         | 150               | -                          | -       | -       | X        |
| <b>VIDEO BUFFER/CURRENT AMPLIFIERS</b> |                                   |            |                   |                            |         |         |          |
| HA-5002                                | High Slew Rate                    | 8          | 150               | X                          | -       | X       | -        |
| HA-5033                                | Broadband High Slew Rate          | 8          | 150               | X                          | -       | X       | -        |
| <b>COMPARATORS</b>                     |                                   |            |                   |                            |         |         |          |
| CA139                                  | General Purpose                   | 14         | 150               | -                          | -       | -       | X        |
| HA-4905 *                              | 130ns Bipolar Quad                | 16         | 300               | X                          | -       | -       | -        |
| HFA-0003*                              | Ultra-High Speed                  | 8          | 150               | X                          | -       | X       | -        |
| HFA-0003L*                             | Ultra-High Speed                  | 16         | 300               | X                          | -       | X       | -        |
| LM2901                                 | General Purpose                   | 14         | 150               | -                          | -       | X       | -        |
| LM3302                                 | General Purpose                   | 14         | 150               | -                          | -       | X       | -        |
| <b>TELECOM</b>                         |                                   |            |                   |                            |         |         |          |
| HC5509B                                | SLIC                              | 28         | -                 | X                          | -       | X       | -        |
| HC5502B*                               | SLIC                              | 24         | -                 | X                          | -       | X       | -        |
| HC5504B*                               | SLIC                              | 24         | -                 | X                          | -       | X       | -        |
| HC5504DLC*                             | SLIC                              | 24         | -                 | X                          | -       | X       | -        |
| HC5524*                                | SLIC                              | 28         | -                 | X                          | -       | X       | -        |

\* Product in development, lead count and body dimensions may change.

**LINEAR SOIC PRODUCT OFFERINGS (Continued)**

| PRODUCT                            | DESCRIPTION                      | LEAD COUNT | BODY WIDTH (MILS) | OPERATING TEMPERATURE (°C) |         |         |          |
|------------------------------------|----------------------------------|------------|-------------------|----------------------------|---------|---------|----------|
|                                    |                                  |            |                   | 0/+70                      | -25/+85 | -40/+85 | -55/+125 |
| <b>SAMPLE &amp; HOLDS</b>          |                                  |            |                   |                            |         |         |          |
| HA-2425 *                          | 3.2µs Monolithic S/H             | 14         | 150               | X                          | -       | -       | -        |
| HA-5340 *                          | 0.7µs Low Distortion Monolithic  | 14         | 150               | X                          | -       | X       | -        |
| <b>ARRAYS</b>                      |                                  |            |                   |                            |         |         |          |
| CA3039                             | General Purpose Diode            | 14         | 150               | -                          | -       | -       | X        |
| CA3046                             | General Purpose N-P-N Transistor | 14         | 150               | -                          | -       | -       | X        |
| CA3081                             | High Current N-P-N Transistor    | 16         | 300               | -                          | -       | -       | X        |
| CA3082                             | High Current N-P-N Transistor    | 16         | 300               | -                          | -       | -       | X        |
| CA3083                             | High Current N-P-N Transistor    | 16         | 150               | -                          | -       | -       | X        |
| CA3086                             | General Purpose N-P-N Transistor | 14         | 150               | -                          | -       | -       | X        |
| CA3096                             | N-P-N/P-N-P Transistor           | 16         | 300               | -                          | -       | -       | X        |
| CA3127                             | High Frequency N-P-N Transistor  | 16         | 300               | -                          | -       | -       | X        |
| CA3146                             | High Voltage N-P-N Transistor    | 14         | 150               | -                          | -       | X       | -        |
| CA3183                             | High Voltage N-P-N Transistor    | 16         | 300               | -                          | -       | X       | -        |
| CA3227                             | High Frequency N-P-N Transistor  | 16         | 300               | -                          | -       | -       | X        |
| CA3246                             | High Frequency N-P-N Transistor  | 14         | 150               | -                          | -       | X       | -        |
| <b>POWER MANAGEMENT ICs</b>        |                                  |            |                   |                            |         |         |          |
| CA3094                             | Prog. Power Switch/Amplifier     | 8          | 150               | -                          | -       | -       | X        |
| ICL7660                            | CMOS Voltage Converter           | 8          | 150               | X                          | -       | -       | -        |
| ICL7660S                           | CMOS Voltage Converter           | 8          | 150               | X                          | X       | -       | -        |
| ICL7662 *                          | CMOS High Voltage Converter      | 8          | 150               | X                          | -       | -       | -        |
| ICL7663S                           | CMOS Prog. Pos. Voltage Reg.     | 8          | 150               | X                          | X       | -       | -        |
| ICL7665S                           | CMOS Over/Under Voltage Det.     | 8          | 150               | X                          | X       | -       | -        |
| ICL7667                            | Dual Power MOS Driver            | 8          | 150               | X                          | -       | -       | -        |
| ICL7673                            | Battery Backup Switch            | 8          | 150               | X                          | -       | -       | -        |
| ICL8211                            | Programmable Voltage Detector    | 8          | 150               | X                          | -       | -       | -        |
| ICL8212                            | Programmable Voltage Detector    | 8          | 150               | X                          | -       | -       | -        |
| <b>SPECIAL ANALOG FUNCTION ICs</b> |                                  |            |                   |                            |         |         |          |
| CA555                              | 555 Timer                        | 8          | 150               | X                          | -       | -       | X        |
| HA-2406                            | 4 Channel Multiplexed Amplifier  | 16         | 300               | X                          | -       | X       | -        |
| HA-2546 *                          | Wideband Analog Multiplier       | 16         | 300               | X                          | -       | X       | -        |
| HA-2547 *                          | Wideband Two Quad                | 16         | 300               | X                          | -       | X       | -        |
| HA-2556 *                          | Wideband Four Quad               | 16         | 300               | X                          | -       | X       | -        |
| HA-2557 *                          | Wideband Four Quad               | 16         | 300               | X                          | -       | X       | -        |
| ICM7242                            | Log Antilog                      | 8          | 150               | X                          | -       | -       | -        |
| ICM7555                            | CMOS General Purpose Timer       | 8          | 150               | X                          | X       | -       | -        |

\* Product in Development, Lead Count and Body Dimensions May Change.

| FOR PRODUCTS WITH PREFIX OF: | THE SOIC PACKAGE CODE IS: | THE TAPE AND REEL CODE IS: |
|------------------------------|---------------------------|----------------------------|
| 'CA'                         | 'M' Suffix                | 'M96' Suffix               |
| 'HA', 'HC' or 'HFA'          | '9P' Prefix               | '-T' Suffix                |
| 'ICL' or 'ICM'               | 'B' Suffix                | '-T' Suffix                |

# CA/CD-Type Packaging & Ordering Information

## Linear (CA Series)/Telecom (CD Series)

Linear ICs and Telecom ICs are available in a wide variety of package designs. These packages are identified by suffix letters indicated in the chart below. When ordering Linear or Telecom devices, it is important that the appropriate suffix letter be affixed to the type number as indicated on the price schedule.

| PACKAGE                        | CA/CD SERIES |
|--------------------------------|--------------|
| Dual-In-Line Ceramic           | D            |
| Dual-In-Line Plastic           | E            |
| Frit-Seal Dual-In-Line Ceramic | F            |
| Quad-In-Line Plastic           | Q            |
| Plastic Lead Chip Carrier      | Q            |
| Dual-In-Line Formed Lead TO-5  | S            |
| TO-5 Style Package             | T            |
| Small Outline (SO) Plastic     | M            |

## Extra Value Screening

Linear product with extra value screening has an X added to the standard type number in the price list, and is also branded as such. A white dot will indicate location of Pin 1.

Example:

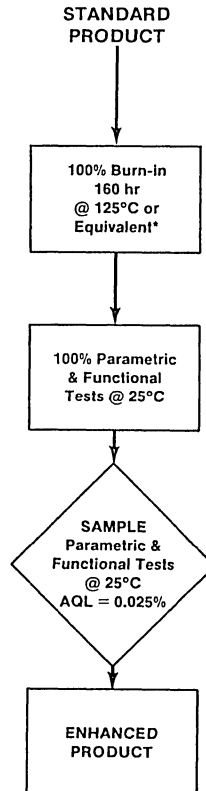
A CA3080E with Extra Value screening is designated CA3080EX in the price list. It is branded CA3080EX plus a white dot at pin number 1.

## Tape & Reel for Small-Outline Packages

With the introduction of small-outline packages, Harris now offers its customers the convenient tape and reel style packaging. Small-outline devices, which can be tape and reeled, are denoted with the suffix "M96" or "AM96" in the linear and high speed logic product lines. Devices must be ordered in multiples of quantities listed below. Any returns must be full and unopened reels.

| LEAD COUNT | TAPE WIDTH (mm) | REEL SIZE (INCHES) | DEVICES PER REEL |
|------------|-----------------|--------------------|------------------|
| 8          | 12              | 13                 | 2500             |
| 14         | 16              | 13                 | 2500             |
| 16         | 16              | 13                 | 2500             |
| 24         | 24              | 13                 | 1000             |

## Product Flow



- Production State or Process
- ◇ Quality Assurance Step

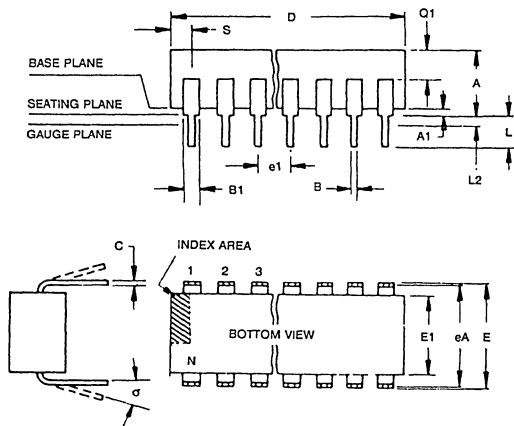


# Package Outlines

## Dual-In-Line Welded-Seal Ceramic Package

(D) SUFFIX

16-LEAD DUAL-IN-LINE WELDED-SEAL CERAMIC PACKAGE



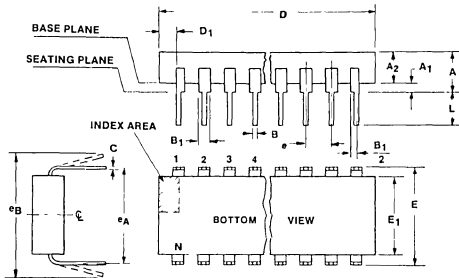
| SYMBOL   | INCHES   |       | MILLIMETERS |       | NOTES |
|----------|----------|-------|-------------|-------|-------|
|          | MIN.     | MAX.  | MIN.        | MAX.  |       |
| A        | 0.120    | 0.160 | 3.05        | 4.06  |       |
| A1       | 0.020    | 0.065 | 0.51        | 1.65  |       |
| B        | 0.014    | 0.020 | 0.356       | 0.508 |       |
| B1       | 0.050    | 0.065 | 1.27        | 1.65  |       |
| C        | 0.008    | 0.012 | 0.204       | 0.304 | 1     |
| D        | 0.745    | 0.840 | 18.93       | 21.33 |       |
| E        | 0.300    | 0.325 | 7.62        | 8.25  |       |
| E1       | 0.240    | 0.260 | 6.10        | 6.60  |       |
| e1       | 0.100 TP |       | 2.54 TP     |       | 2     |
| eA       | 0.300 TP |       | 7.62 TP     |       | 2, 3  |
| L        | 0.125    | 0.150 | 3.18        | 3.81  |       |
| L2       | 0.000    | 0.030 | 0.000       | 0.76  |       |
| $\alpha$ | 0°       | 15°   | 0°          | 15°   | 4     |
| N        | 16       |       | 16          |       | 5     |
| N1       | 0        |       | 0           |       | 6     |
| Q1       | 0.050    | 0.085 | 1.27        | 2.15  |       |
| S        | 0.065    | 0.090 | 1.66        | 2.28  |       |

**NOTES:**

Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013".
2. Leads within 0.005" (0.12mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. eA applies in zone L2 when unit installed.
4.  $\alpha$  applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N1 is the quantity of allowable missing leads.

## Dual-In-Line Plastic Packages



(E) SUFFIX (JEDEC MS-001-AB)  
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

| SYMBOL         | INCHES    |       | MILLIMETERS |       | NOTES |
|----------------|-----------|-------|-------------|-------|-------|
|                | MIN.      | MAX.  | MIN.        | MAX.  |       |
| A              | -         | 0.210 | -           | 5.33  | 9     |
| A1             | 0.015     | -     | 0.39        | -     | 9     |
| A2             | 0.115     | 0.195 | 2.93        | 4.95  |       |
| B              | 0.014     | 0.022 | 0.356       | 0.558 |       |
| B1             | 0.045     | 0.070 | 1.15        | 1.77  | 3     |
| C              | 0.008     | 0.015 | 0.204       | 0.381 |       |
| D              | 0.348     | 0.430 | 8.84        | 10.92 | 4     |
| D1             | 0.005     | -     | 0.13        | -     | 12    |
| E              | 0.300     | 0.325 | 7.62        | 8.25  | 5     |
| E1             | 0.240     | 0.280 | 6.10        | 7.11  | 6, 7  |
| e              | 0.100 BSC |       | 2.54 BSC    |       | 8     |
| e <sub>A</sub> | 0.300 BSC |       | 7.62 BSC    |       | 9     |
| e <sub>B</sub> | -         | 0.430 | -           | 10.92 | 10    |
| L              | 0.115     | 0.160 | 2.93        | 4.06  | 9     |
| N              | 8         |       | 8           |       | 11    |

(E) SUFFIX (JEDEC MS-001-AC)  
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

| SYMBOL         | INCHES    |       | MILLIMETERS |       | NOTES |
|----------------|-----------|-------|-------------|-------|-------|
|                | MIN.      | MAX.  | MIN.        | MAX.  |       |
| A              | -         | 0.210 | -           | 5.33  | 9     |
| A1             | 0.015     | -     | 0.39        | -     | 9     |
| A2             | 0.115     | 0.195 | 2.93        | 4.95  |       |
| B              | 0.014     | 0.022 | 0.356       | 0.558 |       |
| B1             | 0.045     | 0.070 | 1.15        | 1.77  | 3     |
| C              | 0.008     | 0.015 | 0.204       | 0.381 |       |
| D              | 0.725     | 0.795 | 18.42       | 20.19 | 4     |
| D1             | 0.005     | -     | 0.13        | -     | 12    |
| E              | 0.300     | 0.325 | 7.62        | 8.25  | 5     |
| E1             | 0.240     | 0.280 | 6.10        | 7.11  | 6, 7  |
| e              | 0.100 BSC |       | 2.54 BSC    |       | 8     |
| e <sub>A</sub> | 0.300 BSC |       | 7.62 BSC    |       | 9     |
| e <sub>B</sub> | -         | 0.430 | -           | 10.92 | 10    |
| L              | 0.115     | 0.160 | 2.93        | 4.06  | 9     |
| N              | 14        |       | 14          |       | 11    |

(E) SUFFIX (JEDEC MS-001-AA)  
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

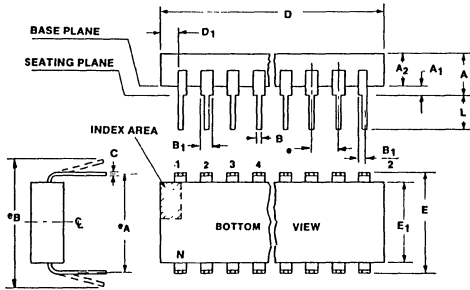
| SYMBOL         | INCHES    |       | MILLIMETERS |       | NOTES |
|----------------|-----------|-------|-------------|-------|-------|
|                | MIN.      | MAX.  | MIN.        | MAX.  |       |
| A              | -         | 0.210 | -           | 5.33  | 9     |
| A1             | 0.015     | -     | 0.39        | -     | 9     |
| A2             | 0.115     | 0.195 | 2.93        | 4.95  |       |
| B              | 0.014     | 0.022 | 0.356       | 0.558 |       |
| B1             | 0.045     | 0.070 | 1.15        | 1.77  | 3     |
| C              | 0.008     | 0.015 | 0.204       | 0.381 |       |
| D              | 0.745     | 0.840 | 18.93       | 21.33 | 4     |
| D1             | 0.005     | -     | 0.13        | -     | 12    |
| E              | 0.300     | 0.325 | 7.62        | 8.25  | 5     |
| E1             | 0.240     | 0.280 | 6.10        | 7.11  | 6, 7  |
| e              | 0.100 BSC |       | 2.54 BSC    |       | 8     |
| e <sub>A</sub> | 0.300 BSC |       | 7.62 BSC    |       | 9     |
| e <sub>B</sub> | -         | 0.430 | -           | 10.92 | 10    |
| L              | 0.115     | 0.160 | 2.93        | 4.06  | 9     |
| N              | 16        |       | 16          |       | 11    |

### NOTES:

- Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
- Protrusions (flash) on the base plane surface shall not exceed 0.010" (0.25mm).
- The dimension shown is for full leads. "Half" leads are optional at lead positions  $1, N, \frac{N}{2}, \frac{N}{2} + 1$ .
- Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.25mm).
- E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
- Dimension E1 does not include mold flash or protrusions.
- Package body and leads shall be symmetrical around center line shown in end view.

- Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
- This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010" (0.25mm) diameter for dimension e<sub>A</sub>.
- e<sub>B</sub> is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
- N is the maximum number of lead positions.
- Dimension D1 at the left end of the package must equal dimension D1 at the right end of the package within 0.030" (0.76mm).
- Pointed or rounded lead tips are preferred to ease insertion.
- For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

## Dual-In-Line Plastic Packages (Continued)



### (E) SUFFIX (JEDEC MS-001-AD) 18 LEAD DUAL-IN-LINE PLASTIC PACKAGE

| SYMBOL         | INCHES    |       | MILLIMETERS |       | NOTES |
|----------------|-----------|-------|-------------|-------|-------|
|                | MIN.      | MAX.  | MIN.        | MAX.  |       |
| A              | -         | 0.210 | -           | 5.33  | 9     |
| A1             | 0.015     | -     | 0.39        | -     | 9     |
| A2             | 0.115     | 0.195 | 2.93        | 4.95  |       |
| B              | 0.014     | 0.022 | 0.356       | 0.558 |       |
| B1             | 0.045     | 0.070 | 1.15        | 1.77  | 3     |
| C              | 0.008     | 0.015 | 0.204       | 0.381 |       |
| D              | 0.845     | 0.925 | 21.47       | 23.49 | 4     |
| D1             | 0.005     | -     | 0.13        | -     | 12    |
| E              | 0.300     | 0.325 | 7.62        | 8.25  | 5     |
| E1             | 0.240     | 0.280 | 6.10        | 7.11  | 6, 7  |
| e              | 0.100 BSC |       | 2.54 BSC    |       | 8     |
| e <sub>A</sub> | 0.300 BSC |       | 7.62 BSC    |       | 9     |
| e <sub>B</sub> | -         | 0.430 | -           | 10.92 | 10    |
| L              | 0.115     | 0.160 | 2.93        | 4.06  | 9     |
| N              | 18        |       | 18          |       | 11    |

### (E) SUFFIX (JEDEC MS-001-AF) 24 LEAD DUAL-IN-LINE PLASTIC PACKAGE

| SYMBOL         | INCHES    |       | MILLIMETERS |       | NOTES |
|----------------|-----------|-------|-------------|-------|-------|
|                | MIN.      | MAX.  | MIN.        | MAX.  |       |
| A              | -         | 0.210 | -           | 5.33  | 9     |
| A1             | 0.015     | -     | 0.39        | -     | 9     |
| A2             | 0.115     | 0.195 | 2.93        | 4.95  |       |
| B              | 0.014     | 0.022 | 0.356       | 0.558 |       |
| B1             | 0.045     | 0.070 | 1.15        | 1.77  | 3     |
| C              | 0.008     | 0.015 | 0.204       | 0.381 |       |
| D              | 1.125     | 1.275 | 28.6        | 32.3  | 4     |
| D1             | 0.005     | -     | 0.13        | -     | 12    |
| E              | 0.300     | 0.325 | 7.62        | 8.25  | 5     |
| E1             | 0.240     | 0.280 | 6.10        | 7.11  | 6, 7  |
| e              | 0.100 BSC |       | 2.54 BSC    |       | 8     |
| e <sub>A</sub> | 0.300 BSC |       | 7.62 BSC    |       | 9     |
| e <sub>B</sub> | -         | 0.430 | -           | 10.92 | 10    |
| L              | 0.115     | 0.160 | 2.93        | 4.06  | 9     |
| N              | 24        |       | 24          |       | 11    |

### (E) SUFFIX (JEDEC MS-011-AA) 24 LEAD DUAL-IN-LINE PLASTIC PACKAGE

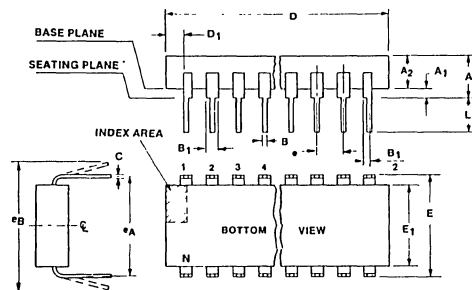
| SYMBOL         | INCHES    |       | MILLIMETERS |       | NOTES |
|----------------|-----------|-------|-------------|-------|-------|
|                | MIN.      | MAX.  | MIN.        | MAX.  |       |
| A              | -         | 0.250 | -           | 6.35  | 9     |
| A1             | 0.015     | -     | 0.39        | -     | 9     |
| A2             | 0.125     | 0.195 | 3.18        | 4.95  |       |
| B              | 0.014     | 0.022 | 0.356       | 0.558 |       |
| B1             | 0.030     | 0.070 | 0.77        | 1.77  | 3     |
| C              | 0.008     | 0.015 | 0.204       | 0.381 |       |
| D              | 1.150     | 1.290 | 29.3        | 32.7  | 4     |
| D1             | 0.005     | -     | 0.13        | -     | 12    |
| E              | 0.600     | 0.625 | 15.24       | 15.87 | 5     |
| E1             | 0.485     | 0.580 | 12.32       | 14.73 | 6, 7  |
| e              | 0.100 BSC |       | 2.54 BSC    |       | 8     |
| e <sub>A</sub> | 0.600 BSC |       | 15.24 BSC   |       | 9     |
| e <sub>B</sub> | -         | 0.700 | -           | 17.78 | 10    |
| L              | 0.115     | 0.200 | 2.93        | 5.08  | 9     |
| N              | 24        |       | 24          |       | 11    |

#### NOTES:

- Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
- Protrusions (flash) on the base plane surface shall not exceed 0.010" (0.25mm).
- The dimension shown is for full leads. "Half" leads are optional at lead positions  $1, N, \frac{N}{2}, \frac{N}{2} + 1$ .
- Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.25mm).
- E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
- Dimension E1 does not include mold flash or protrusions.
- Package body and leads shall be symmetrical around center line shown in end view.

- Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
- This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3), seating plane gauge). Leads shall be in true position within 0.010" (0.25mm) diameter for dimension e<sub>A</sub>.
- e<sub>B</sub> is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
- N is the maximum number of lead positions.
- Dimension D1 at the left end of the package must equal dimension D1 at the right end of the package within 0.030" (0.76mm).
- Pointed or rounded lead tips are preferred to ease insertion.
- For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

## Dual-In-Line Plastic Packages (Continued)



(E) SUFFIX (JEDEC MS-011-AB)  
28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

| SYMBOL         | INCHES    |       | MILLIMETERS |       | NOTES |
|----------------|-----------|-------|-------------|-------|-------|
|                | MIN.      | MAX.  | MIN.        | MAX.  |       |
| A              | -         | 0.250 | -           | 6.35  | 9     |
| A1             | 0.015     | -     | 0.39        | -     | 9     |
| A2             | 0.125     | 0.195 | 3.18        | 4.95  |       |
| B              | 0.014     | 0.022 | 0.356       | 0.558 |       |
| B1             | 0.030     | 0.070 | 0.77        | 1.77  | 3     |
| C              | 0.008     | 0.015 | 0.204       | 0.381 |       |
| D              | 1.380     | 1.565 | 35.1        | 39.7  | 4     |
| D1             | 0.005     | -     | 0.13        | -     | 12    |
| E              | 0.600     | 0.625 | 15.24       | 15.87 | 5     |
| E1             | 0.485     | 0.580 | 12.32       | 14.73 | 6, 7  |
| e              | 0.100 BSC |       | 2.54 BSC    |       | 8     |
| e <sub>A</sub> | 0.600 BSC |       | 15.24 BSC   |       | 9     |
| e <sub>B</sub> | -         | 0.700 | -           | 17.78 | 10    |
| L              | 0.115     | 0.200 | 2.93        | 5.08  | 9     |
| N              | 28        |       | 28          |       | 11    |

**NOTES:**

- Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
- Protrusions (flash) on the base plane surface shall not exceed 0.010" (0.25mm).
- The dimension shown is for full leads. "Half" leads are optional at lead positions  $1, N, \frac{N}{2}, \frac{N}{2} + 1$ .
- Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010" (0.25mm).
- E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
- Dimension E1 does not include mold flash or protrusions.
- Package body and leads shall be symmetrical around center line shown in end view.

(E) SUFFIX (JEDEC MS-011-AC)  
40 LEAD DUAL-IN-LINE PLASTIC PACKAGE

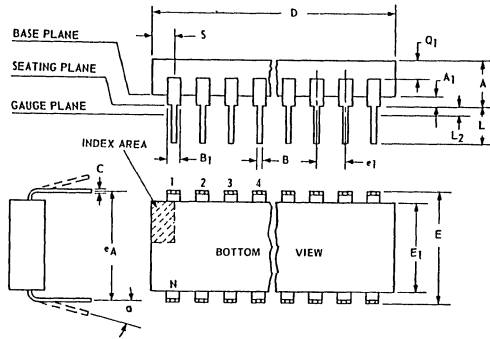
| SYMBOL         | INCHES    |       | MILLIMETERS |       | NOTES |
|----------------|-----------|-------|-------------|-------|-------|
|                | MIN.      | MAX.  | MIN.        | MAX.  |       |
| A              | -         | 0.250 | -           | 6.35  | 9     |
| A1             | 0.015     | -     | 0.39        | -     | 9     |
| A2             | 0.125     | 0.195 | 3.18        | 4.95  |       |
| B              | 0.014     | 0.022 | 0.356       | 0.558 |       |
| B1             | 0.030     | 0.070 | 0.77        | 1.77  | 3     |
| C              | 0.008     | 0.015 | 0.204       | 0.381 |       |
| D              | 1.980     | 2.095 | 50.3        | 53.2  | 4     |
| D1             | 0.005     | -     | 0.13        | -     | 12    |
| E              | 0.600     | 0.625 | 15.24       | 15.87 | 5     |
| E1             | 0.485     | 0.580 | 12.32       | 14.73 | 6, 7  |
| e              | 0.100 BSC |       | 2.54 BSC    |       | 8     |
| e <sub>A</sub> | 0.600 BSC |       | 15.24 BSC   |       | 9     |
| e <sub>B</sub> | -         | 0.700 | -           | 17.78 | 10    |
| L              | 0.115     | 0.200 | 2.93        | 5.08  | 9     |
| N              | 40        |       | 40          |       | 11    |

- Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
- This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3), seating plane gauge). Leads shall be in true position within 0.010" (0.25mm) diameter for dimension e<sub>A</sub>.
- e<sub>B</sub> is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
- N is the maximum number of lead positions.
- Dimension D1 at the left end of the package must equal dimension D1 at the right end of the package within 0.030" (0.76mm).
- Pointed or rounded lead tips are preferred to ease insertion.
- For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

12

PACKAGING AND  
ORDERING INFO.

## Dual-In-Line Frit-Seal Ceramic Packages



(F) SUFFIX (JEDEC MO-001-AB)  
14 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

| SYMBOL   | INCHES   |       | MILLIMETERS |       | NOTES |
|----------|----------|-------|-------------|-------|-------|
|          | MIN.     | MAX.  | MIN.        | MAX.  |       |
| A        | 0.155    | 0.200 | 3.94        | 5.08  |       |
| A1       | 0.020    | 0.050 | 0.508       | 1.27  |       |
| B        | 0.014    | 0.020 | 0.356       | 0.508 |       |
| B1       | 0.050    | 0.065 | 1.27        | 1.65  |       |
| C        | 0.008    | 0.012 | 0.204       | 0.304 | 1     |
| D        | 0.745    | 0.770 | 18.93       | 19.55 |       |
| E        | 0.300    | 0.325 | 7.62        | 8.25  |       |
| E1       | 0.265    | 0.285 | 6.73        | 7.24  |       |
| e1       | 0.100 TP |       | 2.54 TP     |       | 2     |
| eA       | 0.300 TP |       | 7.62 TP     |       | 2,3   |
| L        | 0.125    | 0.150 | 3.18        | 3.81  |       |
| L2       | 0.000    | 0.030 | 0.00        | 0.76  |       |
| $\alpha$ | 0°       | 15°   | 0°          | 15°   | 4     |
| N        | 14       |       | 14          |       | 5     |
| N1       | 0        |       | 0           |       | 6     |
| Q1       | 0.040    | 0.075 | 1.02        | 1.90  |       |
| S        | 0.065    | 0.090 | 1.66        | 2.28  |       |

(F) SUFFIX (JEDEC MO-001-AC)  
16 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

| SYMBOL | INCHES   |       | MILLIMETERS |       | NOTES |
|--------|----------|-------|-------------|-------|-------|
|        | MIN.     | MAX.  | MIN.        | MAX.  |       |
| A      | 0.155    | 0.200 | 3.94        | 5.08  |       |
| A1     | 0.020    | 0.050 | 0.051       | 1.27  |       |
| B      | 0.014    | 0.020 | 0.356       | 0.508 |       |
| B1     | 0.035    | 0.065 | 0.89        | 1.65  |       |
| C      | 0.008    | 0.012 | 0.204       | 0.304 | 1     |
| D      | 0.745    | 0.785 | 18.93       | 19.93 |       |
| E      | 0.300    | 0.325 | 7.62        | 8.25  |       |
| E1     | 0.265    | 0.285 | 6.73        | 7.24  |       |
| e1     | 0.100 TP |       | 2.54 TP     |       | 2     |
| eA     | 0.300 TP |       | 7.62 TP     |       | 2,3   |
| L      | 0.125    | 0.150 | 3.18        | 3.81  |       |
| L2     | 0.000    | 0.030 | 0.00        | 0.76  |       |
| a      | 0°       | 15°   | 0°          | 15°   | 4     |
| N      | 16       |       | 16          |       | 5     |
| N1     | 0        |       | 0           |       | 6     |
| Q1     | 0.040    | 0.075 | 1.02        | 1.90  |       |
| S      | 0.015    | 0.060 | 0.39        | 1.52  |       |

**NOTES:**

Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

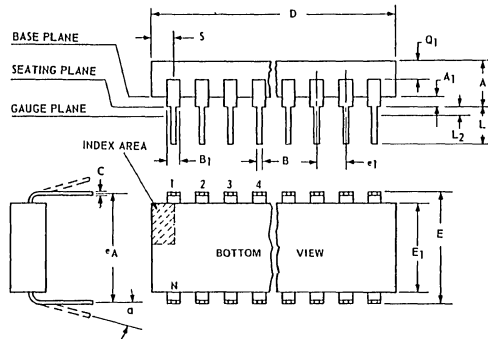
- When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33mm).
- Leads within 0.005" (0.12mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.

(F) SUFFIX  
18 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

| SYMBOL   | INCHES   |       | MILLIMETERS |       | NOTES |
|----------|----------|-------|-------------|-------|-------|
|          | MIN.     | MAX.  | MIN.        | MAX.  |       |
| A        | 0.155    | 0.200 | 3.94        | 5.08  |       |
| A1       | 0.020    | 0.050 | 0.508       | 1.27  |       |
| B        | 0.014    | 0.020 | 0.356       | 0.508 |       |
| B1       | 0.035    | 0.065 | 0.89        | 1.65  |       |
| C        | 0.008    | 0.012 | 0.204       | 0.304 | 1     |
| D        | 0.845    | 0.885 | 21.47       | 22.47 |       |
| E1       | 0.240    | 0.260 | 6.10        | 6.60  |       |
| e1       | 0.100 TP |       | 2.54 TYP    |       | 2     |
| eA       | 0.300 TP |       | 7.62 TYP    |       | 2,3   |
| L        | 0.125    | 0.150 | 3.18        | 3.81  |       |
| $\alpha$ | 0°       | 15°   | 0°          | 15°   | 4     |
| N        | 18       |       | 18          |       | 5     |
| N1       | 0        |       | 0           |       | 6     |
| S        | 0.015    | 0.060 | 0.39        | 1.52  |       |

- eA applies in zone L2 when unit installed.
- a applies to spread leads prior to installation.
- N is the maximum quantity of lead positions.
- N1 is the quantity of allowable missing leads.

## Dual-In-Line Frit-Seal Ceramic



### NOTES:

Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

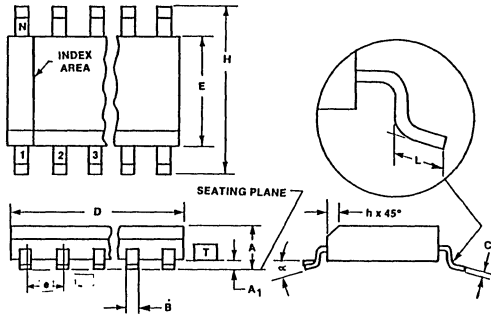
1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013" (0.33mm).
2. Leads within 0.005" (0.127mm) radius of True Position (TP) at gauge plane with maximum material condition.
3. eA applied in zone L2 when unit is installed.
4. Applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N1 is the quantity of allowable missing leads.

### (F) SUFFIX

#### 24 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC

| SYMBOL   | INCHES   |       | MILLIMETERS |       | NOTES |
|----------|----------|-------|-------------|-------|-------|
|          | MIN.     | MAX.  | MIN.        | MAX.  |       |
| A        | 0.120    | 0.250 | 3.10        | 6.30  |       |
| A1       | 0.020    | 0.070 | 0.51        | 1.77  |       |
| B        | 0.016    | 0.020 | 0.407       | 0.508 |       |
| B1       | 0.028    | 0.070 | 0.72        | 1.77  |       |
| C        | 0.008    | 0.012 | 0.204       | 0.304 | 1     |
| D        | 1.200    | 1.290 | 30.48       | 32.76 |       |
| E1       | 0.515    | 0.580 | 13.09       | 14.73 |       |
| e1       | 0.100 TP |       | 2.54 TP     |       | 2     |
| eA       | 0.600 TP |       | 15.24 TP    |       | 2, 3  |
| L        | 0.100    | 0.200 | 2.54        | 5.00  |       |
| L2       | 0.000    | 0.030 | 0.00        | 0.76  |       |
| $\alpha$ | 0°       | 15°   | 0°          | 15°   | 4     |
| N        | 24       |       | 24          |       | 5     |
| N1       | 0        |       | 0           |       | 6     |
| Q1       | 0.040    | 0.075 | 1.02        | 1.90  |       |
| S        | 0.040    | 0.100 | 1.02        | 2.54  |       |

## Small-Outline (SO) Packages



### NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.15mm (.006") per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed .25mm (0.010") per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimension: Millimeter.

### (M) SUFFIX (JEDEC MS-012AB) (Notes 1, 2, 3, 8, 9) 14 LEAD DUAL-IN-LINE SURFACE MOUNT PLASTIC PACKAGE

| SYMBOL | INCHES    |        | MILLIMETERS |      | NOTES |
|--------|-----------|--------|-------------|------|-------|
|        | MIN.      | MAX.   | MIN.        | MAX. |       |
| A      | 0.0532    | 0.0688 | 1.35        | 1.75 |       |
| A1     | 0.0040    | 0.0098 | 0.10        | 0.25 |       |
| B      | 0.0138    | 0.0192 | 0.35        | 0.49 |       |
| C      | 0.0075    | 0.0098 | 0.19        | 0.25 |       |
| D      | 0.3367    | 0.3444 | 8.55        | 8.75 | 4     |
| E      | 0.1497    | 0.1574 | 3.80        | 4.00 | 4     |
| e      | 0.050 BSC |        | 1.27 BSC    |      |       |
| H      | 0.2284    | 0.2440 | 5.80        | 6.20 |       |
| h      | 0.0099    | 0.0196 | 0.25        | 0.50 | 5     |
| L      | 0.016     | 0.050  | 0.40        | 1.27 | 6     |
| N      | 14        |        | 14          |      | 7     |
| α      | 0°        | 8°     | 0°          | 8°   |       |

### (M) SUFFIX (JEDEC MS-012AC) (Notes 1, 2, 3, 8, 9) 16 LEAD DUAL-IN-LINE SURFACE MOUNT PLASTIC PACKAGE

| SYMBOL | INCHES    |        | MILLIMETERS |       | NOTES |
|--------|-----------|--------|-------------|-------|-------|
|        | MIN.      | MAX.   | MIN.        | MAX.  |       |
| A      | 0.0532    | 0.0688 | 1.35        | 1.75  |       |
| A1     | 0.0040    | 0.0098 | 0.10        | 0.25  |       |
| B      | 0.0138    | 0.0192 | 0.35        | 0.49  |       |
| C      | 0.0075    | 0.0098 | 0.19        | 0.25  |       |
| D      | 0.3859    | 0.3937 | 9.80        | 10.00 | 4     |
| E      | 0.1497    | 0.1574 | 3.80        | 4.00  | 4     |
| e      | 0.050 BSC |        | 1.27 BSC    |       |       |
| H      | 0.2284    | 0.2440 | 5.80        | 6.20  |       |
| h      | 0.0099    | 0.0196 | 0.25        | 0.50  | 5     |
| L      | 0.016     | 0.050  | 0.40        | 1.27  | 6     |
| N      | 16        |        | 16          |       | 7     |
| α      | 0°        | 8°     | 0°          | 8°    |       |

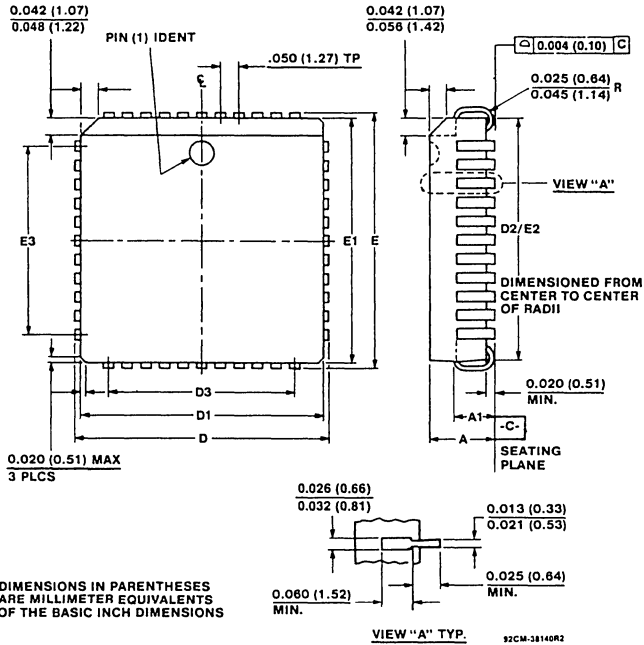
### (M) SUFFIX (JEDEC MS-012AA) (Notes 1, 2, 3, 8, 9) 8 LEAD DUAL-IN-LINE SURFACE-MOUNT PLASTIC PACKAGE

| SYMBOL | INCHES    |        | MILLIMETERS |      | NOTES |
|--------|-----------|--------|-------------|------|-------|
|        | MIN.      | MAX.   | MIN.        | MAX. |       |
| A      | 0.0532    | 0.0688 | 1.35        | 1.75 |       |
| A1     | 0.0040    | 0.0098 | 0.10        | 0.25 |       |
| B      | 0.0138    | 0.0192 | 0.35        | 0.49 |       |
| C      | 0.0075    | 0.0098 | 0.19        | 0.25 |       |
| D      | 0.1890    | 0.1968 | 4.80        | 5.00 | 4     |
| E      | 0.1497    | 0.1574 | 3.80        | 4.00 | 4     |
| e      | 0.050 BSC |        | 1.27 BSC    |      |       |
| H      | 0.2284    | 0.2440 | 5.80        | 6.20 |       |
| h      | 0.0099    | 0.0196 | 0.25        | 0.50 | 5     |
| L      | 0.016     | 0.050  | 0.40        | 1.27 | 6     |
| N      | 8         |        | 8           |      | 7     |
| α      | 0°        | 8°     | 0°          | 8°   |       |

### (M) SUFFIX (JEDEC MS-013AA) (Notes 1, 2, 3, 8, 9) 16 LEAD DUAL-IN-LINE SURFACE MOUNT PLASTIC PACKAGE

| SYMBOL | INCHES    |        | MILLIMETERS |       | NOTES |
|--------|-----------|--------|-------------|-------|-------|
|        | MIN.      | MAX.   | MIN.        | MAX.  |       |
| A      | 0.0926    | 0.1043 | 2.35        | 2.65  |       |
| A1     | 0.0040    | 0.0118 | 0.10        | 0.30  |       |
| B      | 0.0138    | 0.0192 | 0.35        | 0.49  |       |
| C      | 0.0091    | 0.0125 | 0.23        | 0.32  |       |
| D      | 0.3977    | 0.4133 | 10.10       | 10.50 | 4     |
| E      | 0.2914    | 0.2992 | 7.40        | 7.60  | 4     |
| e      | 0.050 BSC |        | 1.27 BSC    |       |       |
| H      | 0.394     | 0.419  | 10.00       | 10.65 |       |
| h      | 0.010     | 0.029  | 0.25        | 0.75  | 5     |
| L      | 0.016     | 0.050  | 0.40        | 1.27  | 6     |
| N      | 16        |        | 16          |       | 7     |
| α      | 0°        | 8°     | 0°          | 8°    |       |

# Plastic Chip Carrier



(Q) SUFFIX (JEDEC MO-047AC)  
44 LEAD SQUARE SURFACE-MOUNT PLASTIC PACKAGE

| SYMBOL | INCHES    |       | MILLIMETERS |        | NOTES |
|--------|-----------|-------|-------------|--------|-------|
|        | MIN.      | MAX.  | MIN.        | MAX.   |       |
| A      | 0.165     | 0.180 | 4.20        | 4.57   |       |
| A1     | 0.090     | 0.120 | 2.29        | 3.04   |       |
| D      | 0.685     | 0.695 | 17.40       | 17.65  |       |
| D1     | 0.650     | 0.656 | 16.510      | 16.662 | 2     |
| D2     | 0.590     | 0.630 | 14.99       | 16.00  | 1     |
| D3     | 0.500 REF |       | 12.70 BSC   |        |       |
| E      | 0.685     | 0.695 | 17.40       | 17.65  |       |
| E1     | 0.650     | 0.656 | 16.510      | 16.662 | 2     |
| E2     | 0.590     | 0.630 | 14.99       | 16.00  | 1     |
| E3     | 0.500 REF |       | 12.70 BSC   |        |       |
| N      | 44        |       | 44          |        | 3     |

**NOTES:**

- To be determined at seating plane.
- Dimensions D1 and E1 do not include mold protrusions.  
Allowable mold protrusion is 0.254mm/0.010 inch.
- "N" is the number of terminal positions.
- Controlling dimensions: Inch
- All leads at seating plane to be coplanar within 0.004 inch.

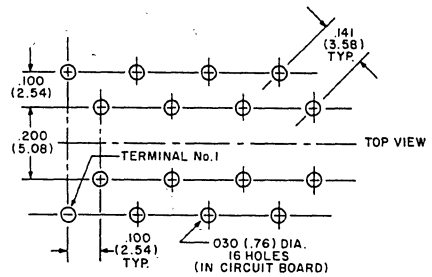
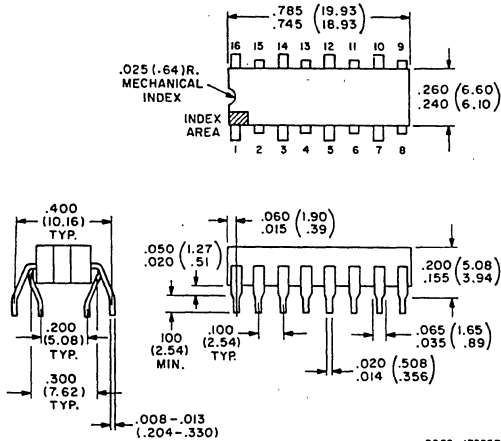
**12**  
PACKAGING AND ORDERING INFO.



# Quad-In-Line Plastic Packages

(Q) SUFFIX, 16 LEAD

## RECOMMENDED MOUNTING HOLE DIMENSIONS AND SPACING



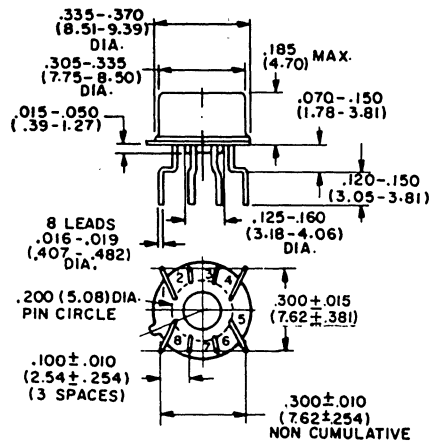
92CS-17533R2

**NOTES:**

1. Body width is measured 0.040" (1.02mm) from top surface.
2. Seating plane defined as the junction of the angle with the narrow portion of the lead.

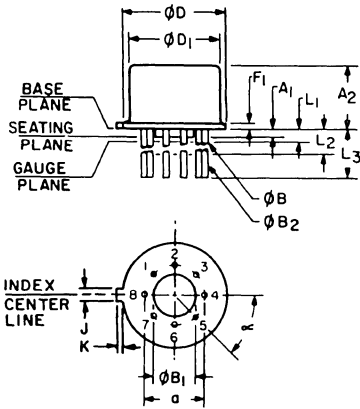
# TO-5 Style Package

(S) SUFFIX  
8 LEAD TO-5 STYLE WITH DUAL-IN-LINE FORMED LEADS (DILCAN)



All dimensions given in inches  
(millimeters)

## TO-5 Style Packages (Continued)



### (T) SUFFIX (JEDEC MO-002-AL) 8 LEAD TO-5 STYLE PACKAGE

| SYMBOL     | INCHES   |       | MILLIMETERS |       | NOTES |
|------------|----------|-------|-------------|-------|-------|
|            | MIN.     | MAX.  | MIN.        | MAX.  |       |
| a          | 0.200 TP |       | 5.88 TP     |       | 1     |
| A1         | 0.010    | 0.050 | 0.26        | 1.27  |       |
| A2         | 0.165    | 0.185 | 4.20        | 4.69  |       |
| $\phi B$   | 0.016    | 0.019 | 0.407       | 0.482 | 2     |
| $\phi B_1$ | 0.125    | 0.160 | 3.18        | 4.06  |       |
| $\phi B_2$ | 0.016    | 0.021 | 0.407       | 0.482 | 2     |
| $\phi D$   | 0.335    | 0.370 | 8.51        | 9.39  |       |
| $\phi D_1$ | 0.305    | 0.335 | 7.75        | 8.50  |       |
| F1         | 0.020    | 0.040 | 0.51        | 1.01  |       |
| j          | 0.028    | 0.034 | 0.712       | 0.863 |       |
| k          | 0.029    | 0.045 | 0.74        | 1.14  | 3     |
| L1         | 0.000    | 0.050 | 0.00        | 1.27  | 2     |
| L2         | 0.250    | 0.500 | 6.4         | 12.7  | 2     |
| L3         | 0.500    | 0.562 | 12.7        | 14.27 | 2     |
| $\alpha$   | 45° TP   |       | 45° TP      |       |       |
| N          | 8        |       | 8           |       | 5     |
| N1         | 3        |       | 3           |       | 4     |

### (T) SUFFIX (JEDEC MO-006-AF) 10 LEAD TO-5 STYLE PACKAGE

| SYMBOL     | INCHES   |       | MILLIMETERS |       | NOTES |
|------------|----------|-------|-------------|-------|-------|
|            | MIN.     | MAX.  | MIN.        | MAX.  |       |
| a          | 0.230 TP |       | 5.84 TP     |       | 1     |
| A1         | 0        | 0     | 0           | 0     |       |
| A2         | 0.165    | 0.185 | 4.19        | 4.70  |       |
| $\phi B$   | 0.016    | 0.019 | 0.407       | 0.482 | 2     |
| $\phi B_1$ | 0        | 0     | 0           | 0     |       |
| $\phi B_2$ | 0.016    | 0.021 | 0.407       | 0.533 | 2     |
| $\phi D$   | 0.335    | 0.370 | 8.51        | 9.39  |       |
| $\phi D_1$ | 0.305    | 0.335 | 7.75        | 8.50  |       |
| F1         | 0.020    | 0.040 | 0.51        | 1.01  |       |
| j          | 0.028    | 0.034 | 0.712       | 0.863 |       |
| k          | 0.029    | 0.045 | 0.74        | 1.14  | 3     |
| L1         | 0.000    | 0.050 | 0.00        | 1.27  | 2     |
| L2         | 0.250    | 0.500 | 6.4         | 12.7  | 2     |
| L3         | 0.500    | 0.562 | 12.7        | 14.27 | 2     |
| $\alpha$   | 36° TP   |       | 36° TP      |       |       |
| N          | 10       |       | 10          |       | 5     |
| N1         | 1        |       | 1           |       | 4     |

### (T) SUFFIX (JEDEC MO-006-AG) 12 LEAD TO-5 STYLE PACKAGE

| SYMBOL     | INCHES   |       | MILLIMETERS |       | NOTES |
|------------|----------|-------|-------------|-------|-------|
|            | MIN.     | MAX.  | MIN.        | MAX.  |       |
| a          | 0.230 TP |       | 5.84 TP     |       | 1     |
| A1         | 0        | 0     | 0           | 0     |       |
| A2         | 0.165    | 0.185 | 4.19        | 4.70  |       |
| $\phi B$   | 0.016    | 0.019 | 0.407       | 0.482 | 2     |
| $\phi B_1$ | 0        | 0     | 0           | 0     |       |
| $\phi B_2$ | 0.016    | 0.021 | 0.407       | 0.533 | 2     |
| $\phi D$   | 0.335    | 0.370 | 8.51        | 9.39  |       |
| $\phi D_1$ | 0.305    | 0.335 | 7.75        | 8.50  |       |
| F1         | 0.020    | 0.040 | 0.51        | 1.01  |       |
| j          | 0.028    | 0.034 | 0.712       | 0.863 |       |
| k          | 0.029    | 0.045 | 0.74        | 1.14  | 3     |
| L1         | 0.000    | 0.050 | 0.00        | 1.27  | 2     |
| L2         | 0.250    | 0.500 | 6.4         | 12.7  | 2     |
| L3         | 0.500    | 0.562 | 12.7        | 14.27 | 2     |
| $\alpha$   | 30° TP   |       | 30° TP      |       |       |
| N          | 12       |       | 12          |       | 5     |
| N1         | 1        |       | 1           |       | 4     |

#### NOTES:

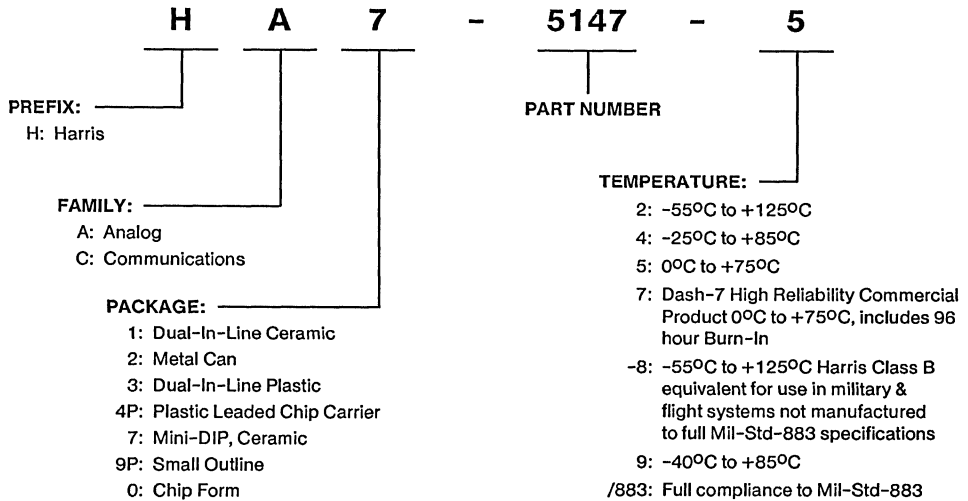
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

- Leads at gauge plane within 0.007" (0.178mm) radius of True Position (TP) at maximum material condition.
- $\phi B$  applies between L1 and L2.  $\phi B_2$  applies between L2 and 0.500" (12.70mm) from seating plane. Diameter is uncontrolled in L1 and beyond 0.500" (12.70mm).

- Measure from Max.  $\phi D$ .
- N1 is the quantity of allowable missing leads.
- N is the maximum quantity of lead positions.

# HA/HC/HFA/HV\*-Type Packaging & Ordering Information

## HARRIS PRODUCT CODE EXAMPLE

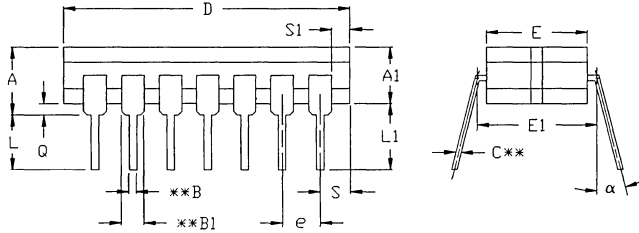


These products are available fully screened to Mil-Std-883C.  
Contact a Harris Sales Office for a copy of the /883 data sheet.

\*Ordering information for HV-1205 and HV-2405E only

# Package Outlines

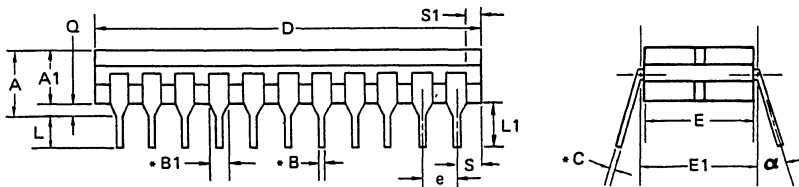
## 1- .300 CERAMIC DUAL-IN-LINE



| PKG CODE | LEAD COUNT | DIM A | DIM A1 | DIM B | DIM B1 | DIM C | DIM D | DIM E | DIM E1 | DIM e | DIM L | DIM L1 | DIM S | DIM S1 | DIM Q | DIM α |
|----------|------------|-------|--------|-------|--------|-------|-------|-------|--------|-------|-------|--------|-------|--------|-------|-------|
| 1-       | 8          | -     | .140   | .016  | .050   | .008  | .375  | .245  | .290   | .100  | .125  | .150   | -     | .005   | .015  | 0°    |
|          | SSI        | .200  | .160   | .023  | .065   | .015  | .395  | .265  | .310   | BSC   | .150  | -      | .055  | -      | .060  | 15°   |
| 1-       | 14         | -     | .140   | .016  | .050   | .008  | .753  | .265  | .290   | .100  | .125  | .150   | -     | .005   | .015  | 0°    |
|          | MSI        | .200  | .170   | .023  | .065   | .015  | .785  | .285  | .310   | BSC   | .180  | -      | .098  | -      | .060  | 15°   |
| 1-       | 14         | -     | .140   | .016  | .050   | .008  | .753  | .285  | .300   | .100  | .125  | .150   | -     | .005   | .015  | 0°    |
|          | LSI        | .200  | .170   | .023  | .065   | .015  | .785  | .305  | .320   | BSC   | .180  | -      | .098  | -      | .060  | 15°   |
| 1-       | 16*        | -     | .140   | .016  | .050*  | .008  | .753  | .265  | .290   | .100  | .125  | .150   | -     | .005   | .015  | 0°    |
|          | MSI        | .200  | .170   | .023  | .065*  | .015  | .785  | .285  | .310   | BSC   | .180  | -      | .080  | -      | .060  | 15°   |
| 1-       | 16*        | -     | .140   | .016  | .050*  | .008  | .753  | .285  | .300   | .100  | .125  | .150   | -     | .005   | .015  | 0°    |
|          | LSI        | .200  | .170   | .023  | .065   | .015  | .785  | .305  | .320   | BSC   | .180  | -      | .080  | -      | .060  | 15°   |
| 1-       | 18         | -     | .140   | .016  | .050*  | .008  | .882  | .285  | .300   | .100  | .125  | .150   | -     | .005   | .015  | 0°    |
|          | LSI        | .200  | .170   | .023  | .065*  | .015  | .915  | .305  | .320   | BSC   | .180  | -      | .098  | -      | .060  | 15°   |
| 1-       | 20         | -     | .140   | .016  | .050*  | .008  | .940  | .285  | .300   | .100  | .125  | .150   | -     | .005   | .015  | 0°    |
|          | LSI        | .200  | .170   | .023  | .065*  | .015  | .970  | .305  | .320   | BSC   | .180  | -      | .080  | -      | .060  | 15°   |

\*End leads are half leads where B remains the same and B1 is 0.035  
 \*\*Solder dip finish add +0.003 inches 0.045

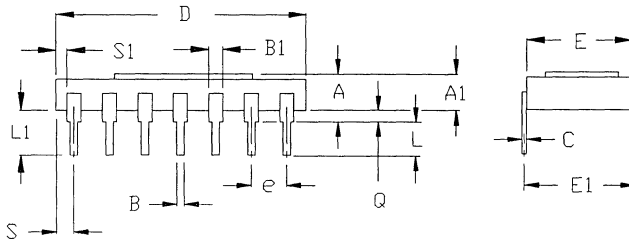
## 1- .600 CERAMIC DUAL-IN-LINE



| PKG CODE | LEAD COUNT | DIM A | DIM A1 | DIM B | DIM B1 | DIM C | DIM D | DIM E | DIM E1 | DIM e | DIM L | DIM L1 | DIM S | DIM S1 | DIM Q | DIM α |
|----------|------------|-------|--------|-------|--------|-------|-------|-------|--------|-------|-------|--------|-------|--------|-------|-------|
| 1-       | 24         | -     | .150   | .016  | .050   | .008  | 1.24  | .515  | .595   | .100  | .125  | .150   | -     | .005   | .015  | 0°    |
|          | LSI        | .225  | .180   | .023  | .065   | .015  | 1.27  | .535  | .615   | BSC   | .180  | -      | .098  | -      | .060  | 15°   |
| 1-       | 28         | -     | .160   | .016  | .050   | .008  | 1.44  | .515  | .595   | .100  | .125  | .150   | -     | .005   | .015  | 0°    |
|          | LSI        | .225  | .190   | .023  | .065   | .015  | 1.47  | .535  | .615   | BSC   | .180  | -      | .098  | -      | .060  | 15°   |

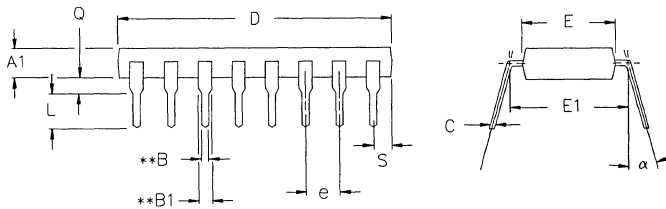
\*Solder dip finish add +0.003 inches

**1- .300 SIDEBRAZE DUAL-IN-LINE**



| PKG CODE | LEAD COUNT | DIM A | DIM A1 | DIM B | DIM B1 | DIM C | DIM D | DIM E | DIM E1 | DIM e | DIM L | DIM L1 | DIM S | DIM S1 | DIM Q |
|----------|------------|-------|--------|-------|--------|-------|-------|-------|--------|-------|-------|--------|-------|--------|-------|
| 1-       | 8          | .101  | -      | .016  | .040   | .008  | .380  | .280  | .290   | .100  | .125  | .150   | .015  | -      | .005  |
|          | LSI        | .150  | -      | .023  | .060   | .015  | .400  | .300  | .310   | BSC   | .180  | -      | .060  | .055   | -     |
| 1-       | 14         | .101  | -      | .016  | .040   | .008  | .738  | .280  | .290   | .100  | .125  | .150   | .015  | -      | .005  |
|          | LSI        | .150  | -      | .023  | .060   | .015  | .758  | .300  | .310   | BSC   | .180  | -      | .060  | .098   | -     |

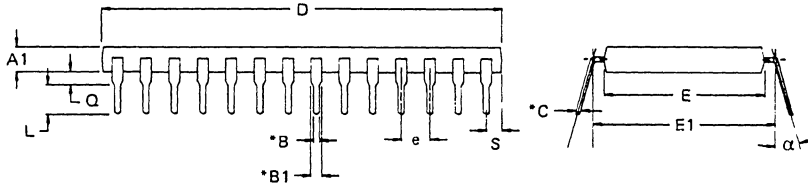
**3- .300 PLASTIC DUAL-IN-LINE**



| PKG CODE | LEAD COUNT | DIM A1 | DIM B | DIM B1 | DIM C | DIM D | DIM E | DIM E1 | DIM e | DIM L | DIM S | DIM Q | DIM alpha |
|----------|------------|--------|-------|--------|-------|-------|-------|--------|-------|-------|-------|-------|-----------|
| 3-       | 8          | .125   | .016  | .050   | .008  | .370  | .245  | .290   | .090  | .110  | .030  | .020  | 0°        |
|          |            | .140   | .023  | .070   | .015  | .390  | .265  | .310   | .110  | .150  | .050  | .040  | 15°       |
| 3-       | 14         | .125   | .016  | .050   | .008  | .750  | .245  | .290   | .090  | .110  | .030  | .020  | 0°        |
|          |            | .140   | .023  | .070   | .015  | .770  | .265  | .310   | .110  | .150  | .050  | .040  | 15°       |
| 3-       | 16*        | .125   | .016  | .050   | .008  | .750  | .245  | .290   | .090  | .110  | .025  | .020  | 0°        |
|          |            | .140   | .023  | .070   | .015  | .770  | .265  | .310   | .110  | .150  | .035  | .040  | 15°       |
| 3-       | 18         | .125   | .016  | .050   | .008  | .900  | .245  | .290   | .090  | .110  | .040  | .020  | 0°        |
|          |            | .140   | .023  | .070   | .015  | .920  | .265  | .310   | .110  | .150  | .060  | .040  | 15°       |
| 3-       | 20         | .130   | .016  | .050   | .008  | 1.030 | .250  | .290   | .090  | .110  | .060  | .020  | 0°        |
|          |            | .145   | .023  | .070   | .015  | 1.050 | .270  | .310   | .110  | .150  | .080  | .040  | 15°       |

\*End leads are half leads where B remains the same and B1 is 0.035  
 \*\*Solder dip finish add +0.003 inches 0.045

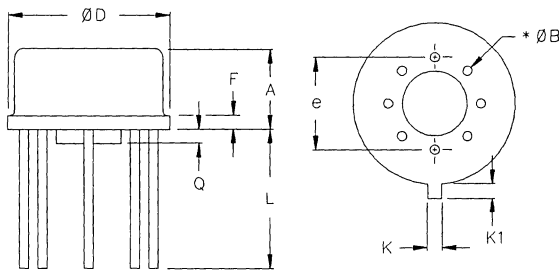
3- .600 PLASTIC DUAL-IN-LINE



| PKG CODE | LEAD COUNT | DIM A1 | DIM B | DIM B1 | DIM C | DIM D | DIM E | DIM E1 | DIM e | DIM L | DIM S | DIM Q | DIM alpha |
|----------|------------|--------|-------|--------|-------|-------|-------|--------|-------|-------|-------|-------|-----------|
| 3-       | 24         | .145   | .016  | .050   | .008  | 1.24  | .540  | .290   | .090  | .110  | .045  | .020  | 0°        |
|          |            | .155   | .023  | .070   | .015  | 1.26  | .560  | .610   | .110  | .150  | .095  | .040  | 15°       |
| 3-       | 28         | .145   | .016  | .050   | .008  | 1.54  | .540  | .590   | .090  | .110  | .110  | .020  | 0°        |
|          |            | .155   | .023  | .070   | .015  | 1.57  | .560  | .610   | .110  | .150  | .160  | .040  | 15°       |

\*Solder dip finish add +0.003 inches

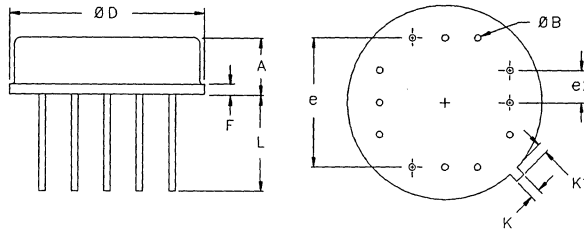
2- TO-99 METAL CAN



| PKG CODE | LEAD COUNT | DIM A | DIM phi B | DIM phi D | DIM e | DIM F | DIM K | DIM K1 | DIM L | DIM Q |
|----------|------------|-------|-----------|-----------|-------|-------|-------|--------|-------|-------|
| 2-       | 8<br>TO-99 | .165  | .016      | .345      | .190  | .020  | .028  | .028   | .505  | .015  |
|          |            | .185  | .018      | .365      | .210  | .040  | .034  | .040   | .550  | .040  |

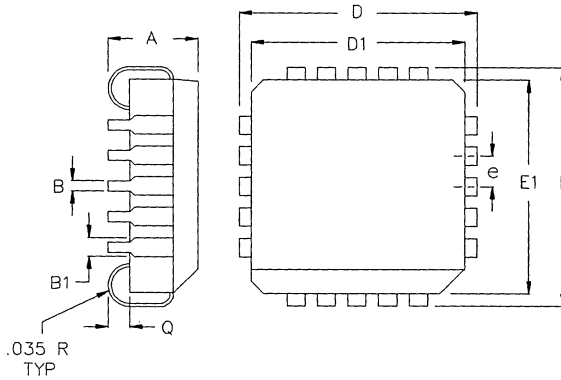
\*Solder dip finish add +0.003 inches

## 2- TO-8 METAL CAN



| PKG CODE | LEAD COUNT | DIM A | DIM $\phi$ B | DIM $\phi$ D | DIM e | DIM F | DIM K | DIM K1 | DIM L | DIM Q |
|----------|------------|-------|--------------|--------------|-------|-------|-------|--------|-------|-------|
| 2-       | 12         | .130  | .016         | .585         | .400  | .100  | .020  | .027   | .027  | .500  |
|          | TO-8       | .150  | .021         | .615         | BSC   | BSC   | .040  | .034   | .045  | .550  |

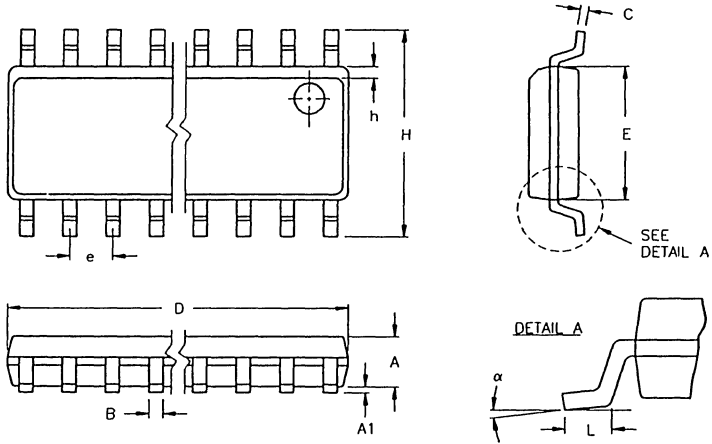
## 4P PLASTIC LEADED CHIP CARRIER



| PKG CODE | LEAD COUNT | DIM A | DIM B | DIM B1 | DIM D/E | DIM D1/E1 | DIM e | DIM Q |
|----------|------------|-------|-------|--------|---------|-----------|-------|-------|
| 4P       | 20         | .165  | .013  | .026   | .385    | .350      | .050  | .020  |
|          |            | .180  | .021  | .032   | .395    | .356      | BSC   | -     |
| 4P       | 28         | .165  | .013  | .026   | .485    | .450      | .050  | .020  |
|          |            | .180  | .021  | .032   | .495    | .456      | BSC   | -     |
| 4P       | 44         | .165  | .013  | .026   | .685    | .650      | .050  | .020  |
|          |            | .180  | .021  | .032   | .695    | .656      | BSC   | -     |

NOTE: Dimensions are  $\frac{\text{Min}}{\text{Max}}$ . Dimensions are in inches.

**9P SMALL OUTLINE PACKAGE (SOIC)**



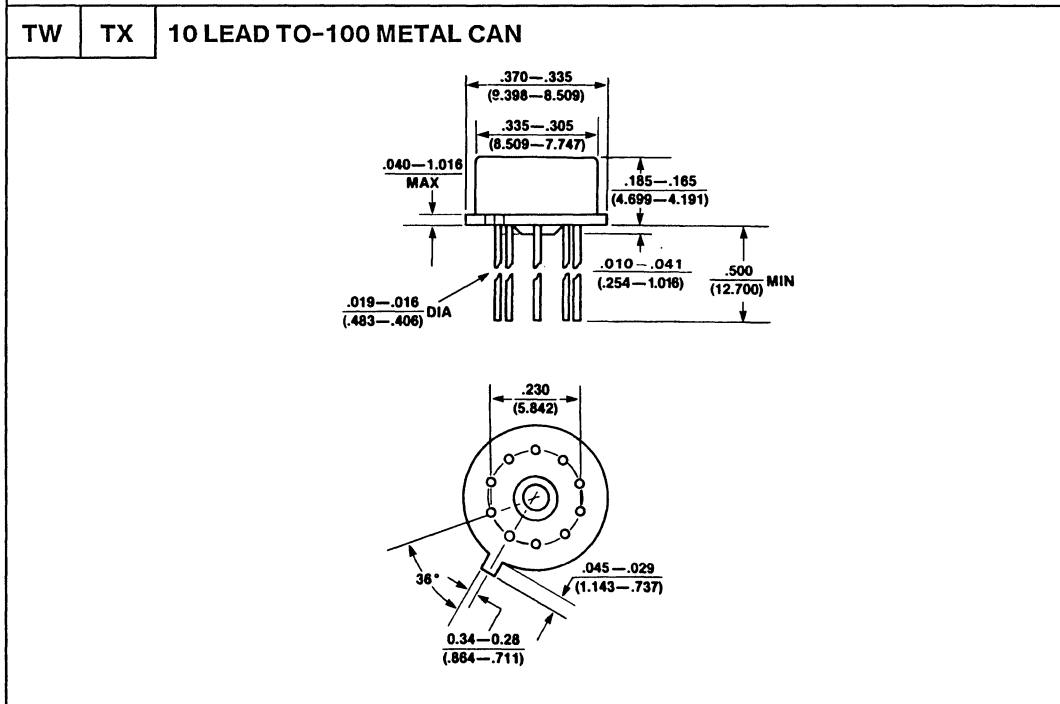
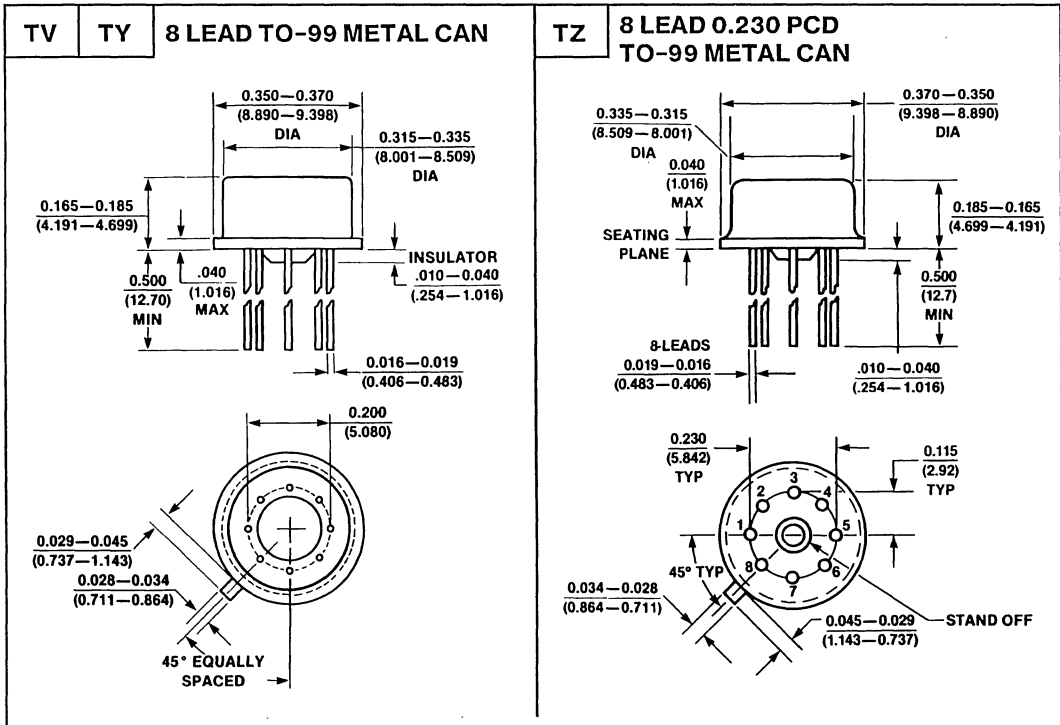
| PKG CODE | LEAD COUNT | DIM A        | DIM A1       | DIM B        | DIM C          | DIM D        | DIM E        | DIM e       | DIM H        | DIM h        | DIM L        | DIM α    |
|----------|------------|--------------|--------------|--------------|----------------|--------------|--------------|-------------|--------------|--------------|--------------|----------|
| 9P       | 8          | .054<br>.068 | .004<br>.009 | .014<br>.019 | .0075<br>.0098 | .189<br>.196 | .150<br>.157 | .050<br>BSC | .229<br>.244 | .010<br>.019 | .016<br>.050 | 0°<br>8° |
| 9P       | 14         | .054<br>.068 | .004<br>.009 | .014<br>.019 | .0075<br>.0098 | .337<br>.344 | .150<br>.157 | .050<br>BSC | .229<br>.244 | .010<br>.019 | .016<br>.050 | 0°<br>8° |
| 9P       | 16 (N)     | .054<br>.068 | .004<br>.009 | .014<br>.019 | .0075<br>.0098 | .386<br>.393 | .150<br>.157 | .050<br>BSC | .229<br>.244 | .010<br>.019 | .016<br>.050 | 0°<br>8° |
| 9P       | 16 (W)     | .093<br>.104 | .004<br>.011 | .014<br>.019 | .0091<br>.0125 | .398<br>.413 | .292<br>.299 | .050<br>BSC | .394<br>.419 | .010<br>.029 | .016<br>.050 | 0°<br>8° |
| 9P       | 24         | .093<br>.104 | .004<br>.011 | .014<br>.019 | .0091<br>.0125 | .599<br>.614 | .292<br>.299 | .050<br>BSC | .394<br>.419 | .010<br>.029 | .016<br>.050 | 0°<br>8° |
| 9P       | 28         | .093<br>.104 | .004<br>.011 | .014<br>.019 | .0091<br>.0125 | .697<br>.712 | .292<br>.299 | .050<br>BSC | .394<br>.419 | .010<br>.029 | .016<br>.050 | 0°<br>8° |

NOTE: Dimensions are  $\frac{\text{Min}}{\text{Max}}$ . Dimensions are in inches.



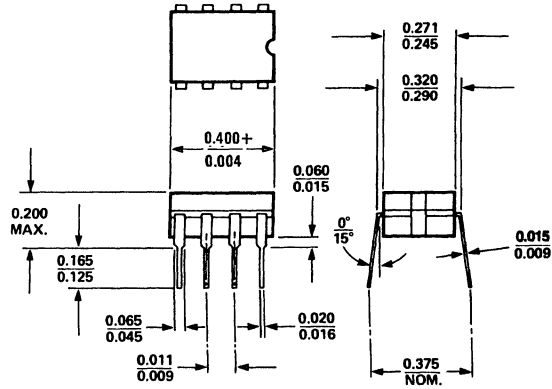


# Package Outlines

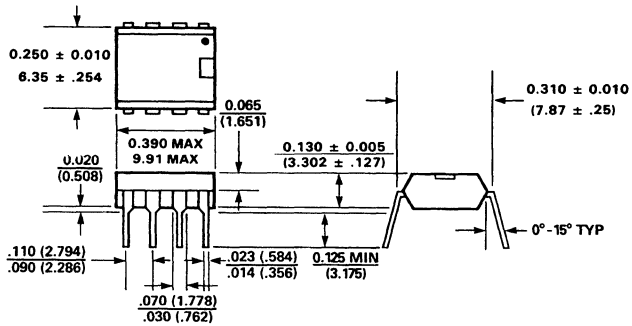


All dimensions given in  $\frac{\text{inches}}{\text{(millimeters)}}$

**JA 8 LEAD CERAMIC DUAL-IN-LINE**



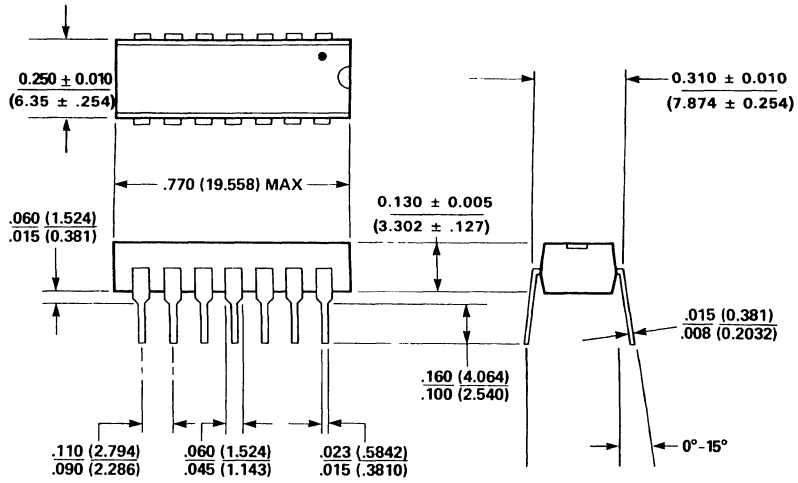
**PA 8 LEAD PLASTIC DUAL-IN-LINE**



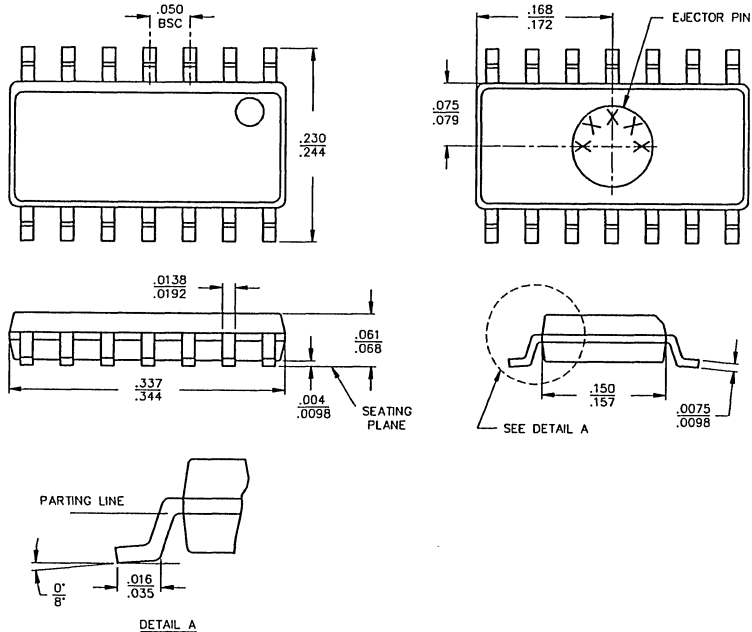
All dimensions given in  $\frac{\text{inches}}{\text{millimeters}}$



**PD 14 LEAD PLASTIC DUAL-IN-LINE**

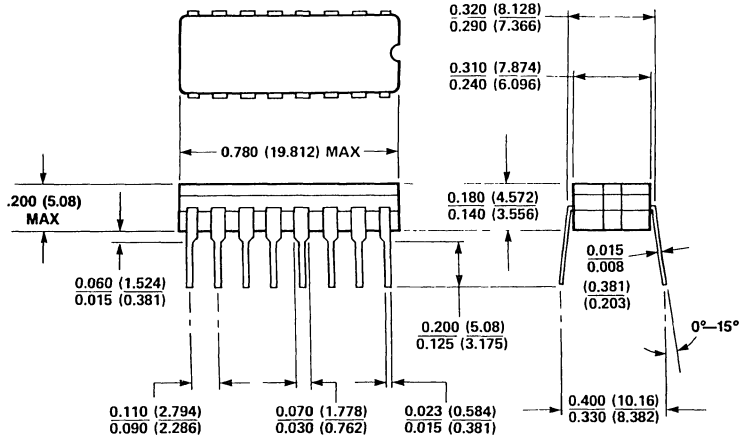


**BD 14 LEAD SOIC**

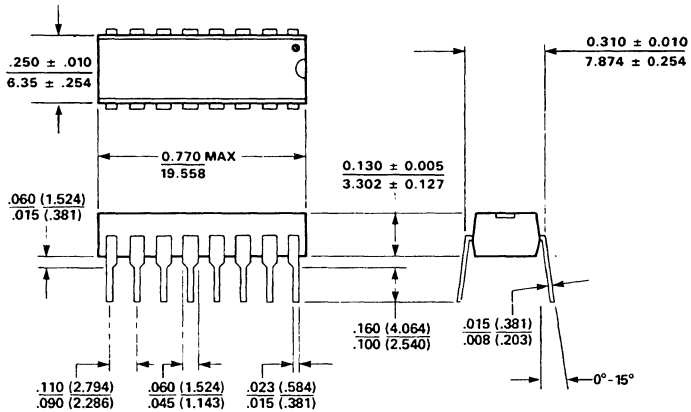


All dimensions given in  $\frac{\text{inches}}{\text{(millimeters)}}$

**JE 16 LEAD CERAMIC DUAL-IN-LINE**

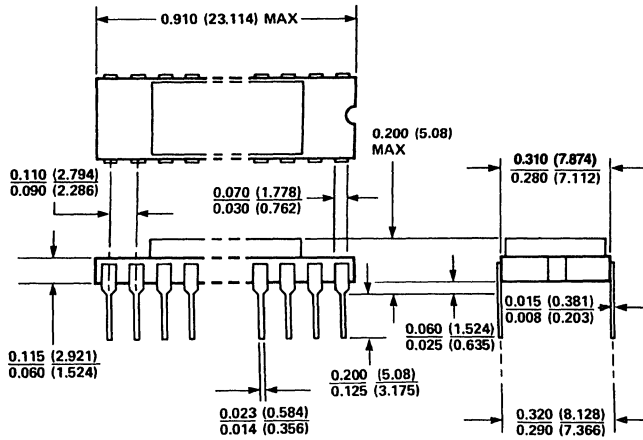


**PE 16 LEAD PLASTIC DUAL-IN-LINE**

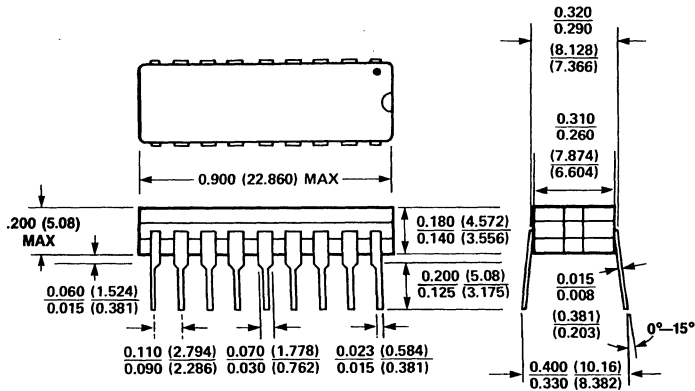


All dimensions given in  $\frac{\text{inches}}{\text{(millimeters)}}$

**DN 18 LEAD CERAMIC DUAL-IN-LINE**



**JN 18 LEAD CERAMIC DUAL-IN-LINE**



All dimensions given in  $\frac{\text{inches}}{\text{millimeters}}$

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