MB86292EB01

Orchid[MB86292] Evaluation System
Hardware Specifications
November 14th 2001 (Rev. 1.1)

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1 Overview

This board system is designed to mainly evaluate the functionally and performance of Fujitsu MB86292 ”Orchid” graphics display controller.

But this board could not evaluate “Super Impose Function” using “external sync”.

2 System Configuration

2.1 Board Configuration

Depending on a needs, this board can be used either by mounting on a PCI slot of ordinary Windows NT (or Windows 2000) PC or by combining with a specific CPU evaluation board (A stand alone configuration). The appliance CPU boards are SH-3 EVA BOD(CX06706C-9901, SH3 CPU evaluation board) or SH-4 EVA BOD(CX06710B-9901, SH4 CPU evaluation board) made by Computex, or KZ-V832-01(V832 evaluation board) made by Kyoto Micro Computers, Co. Ltd. When MB86292EB01 is used with this V832 board, the dedicated interface adapter board “MB86290EB02” is needed.

When MB86292 is mounted on a PCI slot, the PCI bus bridge device PCI9054(made by PLX) acts as a local bus master. When MB86292 is combined with a CPU board, the CPU itself mounted on that board takes this local bus master role.

***The video output of this board is only analog RGB(D-sub connector). Digital output using DFP connector does not work.**
***If you want to use to connect Local CPU board, you need other connection board.**

2.2 Component Outline

■ **Orchid**
MB86292 (Graphics Display Controller)

■ **PCI Bridge**
PCI9054 (made by PLX) and EEPROM [an equivalent 93CS56L]

■ **DFP(Digital Flat Panel) Transmitter SiI164** (made by Silicon Image)

■ **Video D/A Converter ADV7120** (made by Analog Devices)

■ **Digital Video Decoder SAA7113** (made by Philips)

■ **Analog Video Switch EL4331CS**(made by Elantec)

■ **RGB Video Amplifier LM1279AN** (made by National Semiconductor)

■ **8Bit DIP Switch**
Read only.

■ **8Bit LED**
Write only.

■ **LED**
Power on(Power on indicator)

■ **Local CPU Board Interface Connector**
2.54mm pitch 2x20pin x 3 pieces

■ **VGA Output Connector**
Dsub15pin female connector

■ **DFP Output Connector**
Base on MDR Half pitch 20pin female connector
*This connector does not work.

■ **Composite Video Connector**
Input Connector x 1

2.3 Power Supply

All the power source(5.0V, 2.5V, 3.3V) are supplied through connectors in either PCI bus mode or Local CPU board combination mode. But if you use Local CPU board combination mode and evaluate external video sync function using video switch , you have to supply 12V power.

Power connections on this board are as follows:

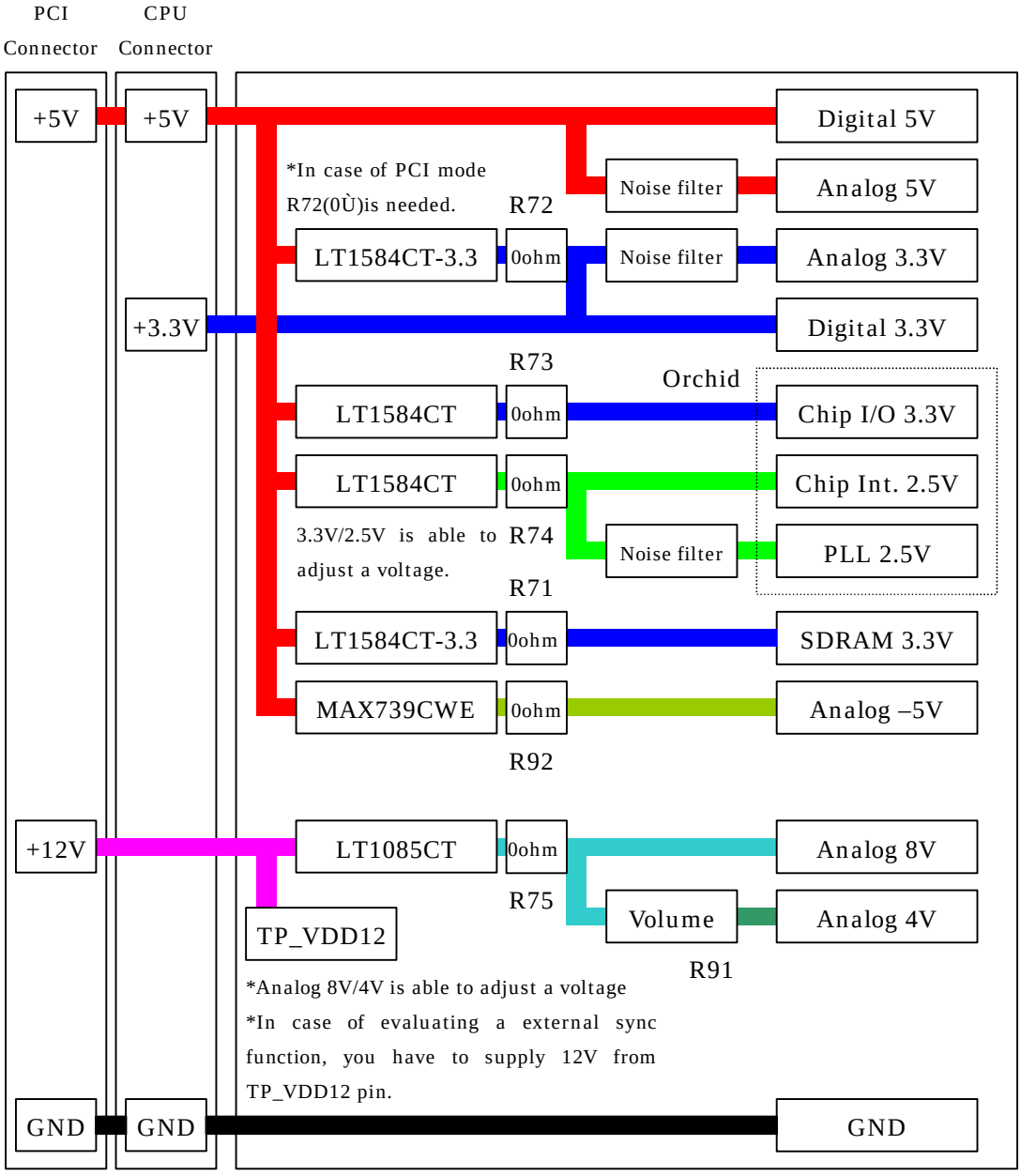

Fig2-1. MB86292EB01 Power Supply Lines

3 Hardware Block Diagram

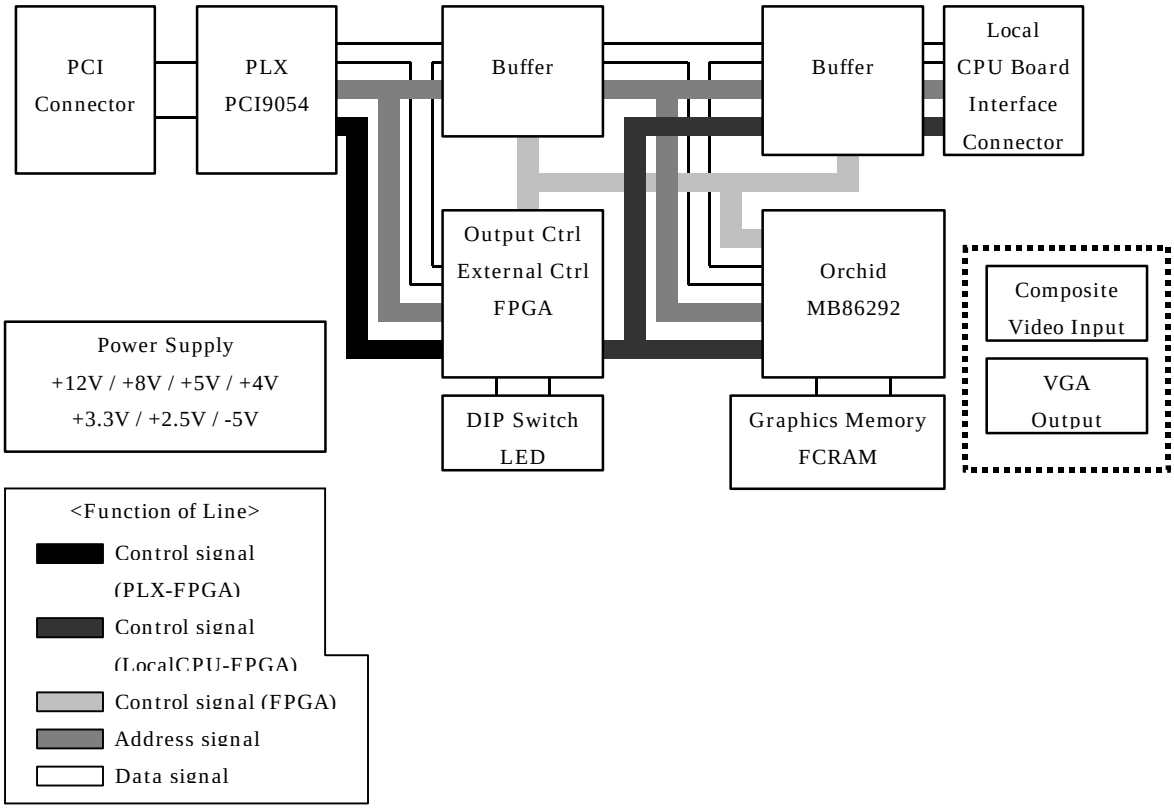

Fig3-1. MB86292EB01 Hardware Block Diagram

4 Memory Map

4.1 Memory Map in PCI bus access mode

1000 0000h 11FB FFFFh	Orchid Frame Memory Area	32bit	PCI Local Address Space 0
11FC 0000h 11FF FFFFh	Orchid Register Area	32bit	
1200 0000h 13FF FFFFh	Orchid Reserved Area	32bit	
1400 0000h 1400 0FFFh	PLX PCI9054 Internal Register Area	32bit	
1400 1000h 1400 1FFFh	FPGA Internal Register Area	32bit	

Table 4-1. MB86292EB01 Memory Map(PCI bus mode)

*4 piece of 16Mbyte x16 FCRAM is mounted on MB86292EB01.
Actual memory space is 8Mbyte.

4.2 Memory Map in Local CPU access mode

1000 0000h 11FB FFFFh	Orchid Frame Memory Area	32bit	SH_CS4
11FC 0000h 11FF FFFFh	Orchid Register Area	32bit	
1200 0000h 13FF FFFFh	Orchid Reserved Area	32bit	
1400 0000h 1400 0FFFh	PLX PCI9054 Internal Register Area	32bit	SH_CS5 &A12=0
1400 1000h 1400 1FFFh	FPGA Internal Register Area	32bit	SH_CS5 &A12=1

Table4-2. MB86292EB01 Memory Map (Local CPU mode)

*Actual memory space is 8Mbyte.

4.3 Register Map

Device	Register	Address	Access	Data Size	True State	R/W
LEDR	LED Register	0x1400 1000	32bit	7:0	1=Light	RW
CTLR	Control Register	0x1400 1004	32bit	7:0	1	RW
DIPSWR	DIP Switch Register	0x1400 1008	32bit	7:0	Off=1	RO
OPSWR	Option Switch Register	0x1400 100C	32bit	7:0	Off=1	RO

Table4-3. MB86292EB01 FPGA Register Map

4.4 Board Configuration Register

Name : CTLR
Address : 1400 1004H
Mode : Read / Write

Bit	Name	Function	0	1
D4	IMASK	Mask Interrupt (Only PCI bus access mode)	Disable Orchid Interrupt signal (Default)	Enable Orchid Interrupt signal

Table4-4. Board configuration register bit assignment

5 External Appearance

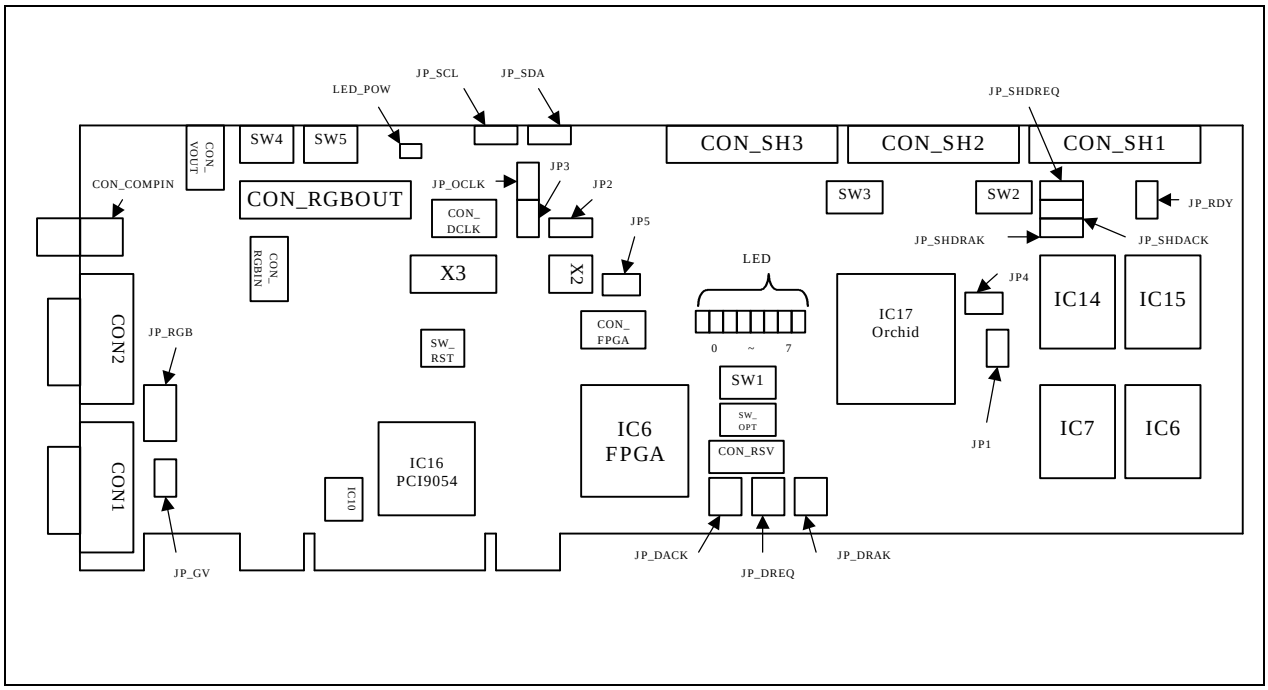

Fig5-1. MB86292EB01 External Appearance

5.1 Switch settings

Switch	Function	Set	Description
SW1-1 to 8	General purpose dip switch	ON=L OFF=H	Bit1=LSB Bit8=MSB (Default all off)
SW2-1 to 5	All Reserved for Orchid	OFF=H	Reserved (DefaultOFF)
SW2-6	Set Orchid clock mode (CKMpin)	ON	Select internal PLL output (Default)
		OFF	Select CPU bus clock(BCLKI pin)
SW2-7,8	Set Orchid CLKSEL pin input	Bit7,8	Note)1=OFF, 0=ON
		0,0	13.5MHz input
		0,1	14.32MHz input(Default)
		1,0	17.73MHz input
		1,1	Reserved
SW3-1	Set Orchid Ready signal mode (MODE2 pin)	ON	Set Normally Not Ready mode (Default)
		OFF	Set Normally Ready mode
SW3-2,3	Set Orchid Host CPU mode (MODE1,MODE0 pins)	Bit2,3	Note)1=OFF, 0=ON
		0,0	SH3 mode
		0,1	SH4 mode(Default)
		1,0	V832 mode
		1,1	SPARClite mode
SW3-4	Set Graphics memory width (Ctrl memory CS)	ON	64bit width (Default)
		OFF	32bit width
SW3-5	Set Orchid RGB output width (XRGBEN pin)	ON	RGB24bit =>Memory 32bit
		OFF	RGB15bit=>Memory 64bit (Default)
SW3-6	Reserved		
SW3-7	PCI9054 TEST pin input	ON	Normal mode(Default)
		OFF	PCI9054 Test mode
SW3-8	PCI9054 BIGEND# pin input	ON	Local Bus Big Endian
		OFF	Local Bus Little Endian(Default)

Table5-1. MB86292EB01 Switch settings(1)

Switch	Function	Set	Description
SW4-1to 4	Reserved	ALL OFF	
SW4-5	Reserved	ON	
SW4-6 to 8	Reserved		
SW5-1	Reserved	OFF	
SW5-2	Reserved	ON	
SW5-3	Set BLANK pin of ADV7120(Video DAC)	ON	Output Analog RGB Blank level (Ignore Digital RGB, REF_WHITE input)
		OFF	Output Analog RGB (Default)
SW5-4	Set REF_WHITE pin of ADV7120 (Video DAC)	ON	Output Analog RGB (Default)
		OFF	Output Analog RGB White level (Ignore Digital RGB input)
SW5-5 to 8	Reserved		
SW_OPT-1,3 to7	Reserved		
SW_OPT-2	Set access mode	ON	Local CPU bus mode
		OFF	PCI bus mode(Default)
SW_OPT-8	Set DOTCLK	ON	NTSC mode
		OFF	VGA mode(Default)
SW_RST	RESET switch		

Table5-2. MB86292EB01 Switch settings (2)

5.2 Jumper settings

Jumper	Function	Set	Description
JP_RGB	Select source RGB signal connecting to Dsub connector	1-2	Connect DAC output RGB signal to Dsub connector (Default)
		2-3	Connect EL4331CS(Video SW) output RGB signal to Dsub connector
JP_GV	Set Control signal of EL4331(Video SW)	1-2	Valid SW5-1 setting(Refer SW5-1)
		2-3	Valid Orchid output GV signal (Default)
JP_OCLK	Set Orchid input bus clock	1-2	Clock input normally(Default)
		2-3	Opposite clock input
JP_RDY	Set Pull-Up/Pull-Down for RDY signal	1-2	RDY signal Pull-Up
		2-3	RDY signal Pull-Down
		Open	Nothing Pull-Up/Pull-Down (Default)
JP_SCL	Set SCL signal for I2C I/F	1-2	Reserved (Default)
		2-3	Reserved
JP_SDA	Set SDA signal for I2C I/F	1-2	Reserved (Default)
		2-3	Reserved
JP_SHDACK	Set DACK signal of Local CPU bus mode	1-2	Select DACK0 signal
		2-3	Select DACK1 signal (Default)
JP_SHDRAK	Set DRAK signal of Local CPU bus mode	1-2	Select DRAK0 signal
		2-3	Select DRAK1 signal (Default)
JP_SHDREQ	Set DREQ signal of Local CPU bus mode	1-2	Select DREQ0 signal
		2-3	Select DREQ1 signal (Default)
JP_DACK	Set DTACK signal	2-4	Fixed (Default)
JP_DRAK	Set DRACK signal	2-4	Fixed (Default)
JP_DREQ	Set DREQ signal	2-4	Fixed (Default)
CON_DCLK	Set clock type for DCLKI pin of Orchid	1-2 Short	Select DOTCLK from PLL output(Default)
		3-4 Short	Select X3 clock (Not mounted)
		JP:Open, 2pin or 4pin: External clock input	Select external input clock

Table5-3. MB86292EB01 jumper settings(1)

Jumper	Function	Set	Description
JP1,JP4	Set CLK pin of Orchid	JP1:1-2,JP4:Open	Select X4(crystal oscillator) (Default)
		JP1:2-3,JP4:Short	Select X1(crystal oscillator)
		Others	Reserved
JP2,JP3	Select bus clock	JP2:1-2,JP3:2-3	PCI mode Select X2(crystal oscillator) (Default)
		JP2:2-3,JP3:2-3	PCI mode Select CCLK output
		JP2:Don't care, JP3:1-2	Local CPU mode
		Others	Reserved
JP5	Set X2(crystal oscillator) 1pin (For OE control device)	Short	1pin=VDD5(Default)
		Open	1pin=Open

Table5-4. MB86292EB01 Jumper Settings (2)

5.3 Switch and jumper settings for changing PCI mode or Local CPU mode

The switch and jumper settings for PCI bus mode or local CPU mode are follows:
Default is set to PCI mode.

Mode	SW_OPT-2	SW3-1 (Ready mode)	SW3-7	JP3
PCI bus mode	OFF	ON(NotReady mode)	ON	2-3
Local CPU mode	ON	OFF(Ready mode)	OFF	1-2

5.4 Local CPU interface connector pin assignment

This board has three special connectors to connect to local CPU connection board.
*****If you want to use to connect Local CPU board, **you need connection board that is same as "Scarlet interface board", called "Rose interface connection board".**

Note) The interrupt signal from Orchid is connected to **IRL2** and **IRL3** signal of local CPU connector through FPGA.

Status of Orchid Interrupt signal	Status of IRL[3:0] in local CPU connector
Interrupt (SH4 mode is Low)	0x3
No interrupt (SH4 mode is high)	0xf

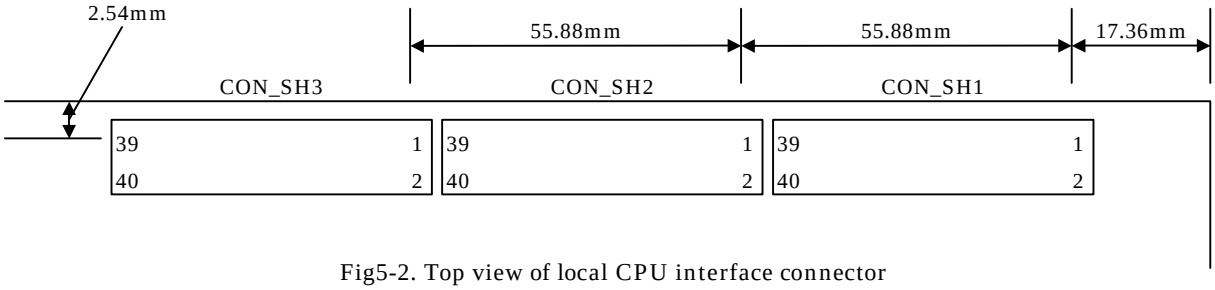

Fig5-2. Top view of local CPU interface connector

<Using connector (CON_SH1 ~ CON_SH3)>
Pin pitch 2.54mm, 2 rows x 20 pin header

<Parts number of "Rose I/F connector">
PS-40SD-D4TS1-1 (Made by JAE)

Local CPU interface connector pin assignment

CON_SH1				CON_SH2			
1	~CS0	2	~WE0	1	VDD5	2	VDD3
3	~CS1	4	~WE1	3	A2	4	A3
5	~CS2	6	~WE2	5	A4	6	A5
7	~CS3	8	~WE3	7	A6	8	A7
9	VDD5	10	VDD3	9	VDD5	10	VDD3
11	~CS4	12	RDWR	11	A8	12	A9
13	~CS5	14	~BS	13	A10	14	A11
15	~CS6	16	GND	15	A12	16	A13
17	~RD	18	CKIO	17	A14	18	A15
19	GND	20	GND	19	GND	20	GND
21	~IRL0	22	~IRL1	21	A16	22	A17
23	~IRL2	24	~IRL3	23	A18	24	A19
25	~RESETOUT	26	RDY	25	A20	26	A21
27	~BACK	28	~BREQ	27	A22	28	A23
29	VDD5	30	VDD3	29	VDD5	30	VDD3
31	DRAK1	32	DRAK0	31	A24	32	A25
33	~DREQ0	34	DACK0	33	VDD5	34	VDD3
35	~DREQ1	36	DACK1	35	GND	36	GND
37	GND	38	GND	37	GND	38	GND
39	GND	40	GND	39	GND	40	GND

CON_SH3			
1	D0	2	D1
3	D2	4	D3
5	D4	6	D5
7	D6	8	D7
9	VDD5	10	VDD3
11	D8	12	D9
13	D10	14	D11
15	D12	16	D13
17	D14	18	D15
19	GND	20	GND
21	D16	22	D17
23	D18	24	D19
25	D20	26	D21
27	D22	28	D23
29	VDD5	30	VDD3
31	D24	32	D25
33	D26	34	D27
35	D28	36	D29
37	D30	38	D31
39	GND	40	GND

Table5-5. Local CPU interface connector pin assignment

5.5 Digital RGB output connector pin assignment

CON_RGBOUT			
1	R0	2	R1
3	R2	4	R3
5	R4	6	R5
7	R6	8	R7
9	GND	10	GND
11	G0	12	G1
13	G2	14	G3
15	G4	16	G5
17	G6	18	G7
19	GND	20	GND
21	B0	22	B1
23	B2	24	B3
25	B4	26	B5
27	B6	28	B7
29	GND	30	GND
31	ORC_HSYNC	32	ORC_VSYNC
33	ORC_CSYNC	34	ORC_DE
35	DCLKO	36	N.C.
37	N.C.	38	N.C.
39	N.C.	40	GND

Table5-6. Digital RGB output connector pin assignment