Data Book

Linear Products

1990

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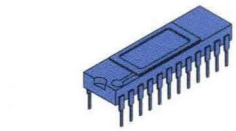

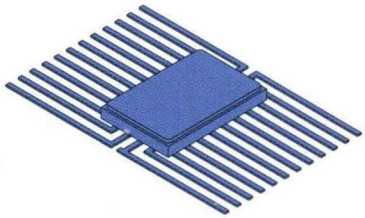

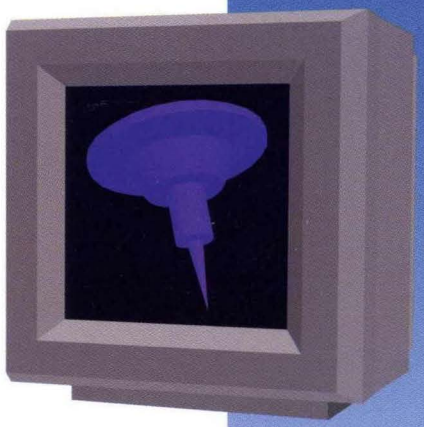

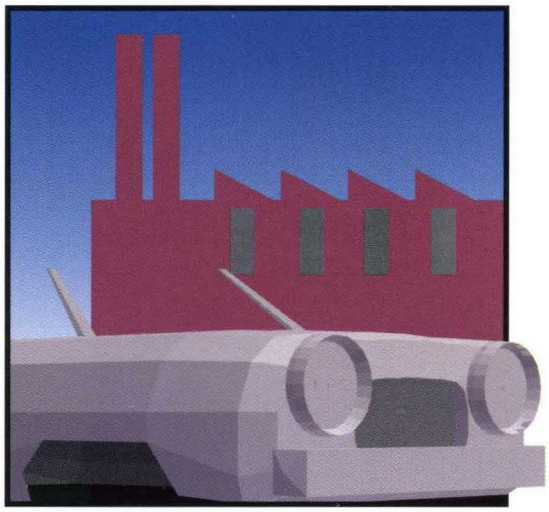

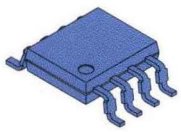

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Linear Products

1990
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Book

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Contents and Alphanumeric Product List

LINEAR PRODUCTS

Contents and Alphanumeric Product List (Continued)

LINEAR PRODUCTS

Contents and Alphanumeric Product List (Continued)

LINEAR PRODUCTS

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LINEAR PRODUCTS

Alphanumeric List of Fujitsu Part Numbers

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Linear PRODUCTS

Alphanumeric List of Fujitsu Part Numbers

Introduction

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Fujitsu's Linear Products

Fujitsu's Linear Products

Introduction

Fujitsu manufactures a wide range of integrated circuits that include: memories, microprocessors, telecommunication circuits, ASIC, high-speed ECL logic, power components (consisting of both discrete transistors and transistor arrays), and linear products.

The linear product line offers devices for use in a wide range of applications. These linear products are manufactured to meet the high standard of quality and reliability that is found in all Fujitsu products.

Operational Amplifiers

General purpose single, dual and quad configurations of industry standard op amps are available in standard DIP and surface mount (SOJ) flatpack packages. Designed for instrumentation and general purpose applications, these devices offer Fujitsu's superior performance, quality and reliability.

Comparators

Fujitsu's comparators include industry standard and proprietary functions and are available in both standard and surface mount packaging.

Automotive Audio

The audio products represent Fujitsu's considerable capability in automotive audio. The audio product line-up includes a comprehensive range of single-ended and balanced transformerless power amplifiers, associated pre-amplifiers, and control circuits.

Power Supply Controls

Fujitsu offers a complete line of Pulse Width Modulation (PWM) controllers for switching supplies, voltage detectors and series regulators. These power supply control devices are available in DIP, surface mount (flatpack) and, for some of the devices, a SIP package. A number of the devices have industry standard pinouts and all power control ICs provide superior performance, quality and reliability.

Fujitsu's Linear Products (Continued)

Motor Drivers

Motor drive products are useful for low power applications such as camera film transports, and door and access panel operation found in such products as VCRs and audio tape drives.

Disk Drivers

Disk drive products include a range of magnetic recording head amplifiers, head signal drivers, amplifiers, and variable frequency oscillators (VFOs).

Data Conversion

Video A/D and D/A converters, audio and general purpose D/A converters, multi-channel Data Acquisition systems and V/F converters are included in this section. Fujitsu offers the user superior performance and a wide array of packaging for video, graphic, multi-purpose instrumentation and process control applications.

Other Linear Products

Several Linear I.C.s, including an industry standard Video Amplifier, industry standard Quad Analog Switch, Lamp Open Detector and Timer, are included in this section.

Operational Amplifiers — *At a Glance*

Page	Device	Description	Features	Power Supply (V)	Package Options
1–3	MB3603	Single	Low Offset Wide Common Mode 1/P	+15 to –15	14-pin Plastic DIP 14-pin Ceramic DIP
1–11	MB3604	Single	GBW = 300MHz, with Buffer Tr (50 mA)	+12 to –6	16-pin Plastic DIP 16-pin Ceramic DIP
1–19	MB3607	Dual	On-chip Frequency Compensation	+15 to –15	8-pin Plastic DIP, FPT 8-pin Ceramic DIP
1–27	MB3614	Quad	Wide Common Mode 1/P	+3 to +30 ±1.5 to ±15	14-pin Plastic DIP, FPT 14-pin Ceramic DIP
1–33	MB3615	Quad	Low Crossover Distortion	+3 to +36 ±1.5 to ±18	14-pin Plastic DIP, FPT 8-pin Plastic FPT
1–39	MB47082	Dual	JFET Input Ii = 30 pA SR = 2 V/µS	±5 to ±15	8-pin Plastic DIP, FPT 9-pin Plastic SIP
1–47	MB47358	Dual	Low Crossover Distortion	+3 to +30 ±1.5 to ±15	8-pin Plastic DIP, FPT 9-pin Plastic SIP
1–55	MB47833	Dual	Low Noise Low Distortion	±1.5 to ±15	8-pin Plastic DIP, FPT 9-pin Plastic SIP

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FUJITSU

OPERATIONAL AMPLIFIER

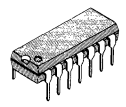
MB3603 MB3609

May 1988
Edition 1.0

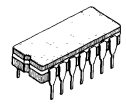
OPERATIONAL AMPLIFIER

The Fujitsu MB3603/3609 are high gain monolithic operational amplifiers. The MB3603/3609 are suitable for industrial measurement instrument or controller because of low offset voltage, high input impedance, wide common-mode input voltage range and wide output voltage range.

- Not required frequency compensation
- On-chip protection circuitry
- Adjustable offset voltage
- Wide common-mode input voltage range and wide output voltage range
- Low power dissipation
- No latch up
- Pin assignment: MB3609 same as μA741



PLASTIC PACKAGE
DIP-14P-M02



CERAMIC PACKAGE
DIP-14C-C01

MB3603

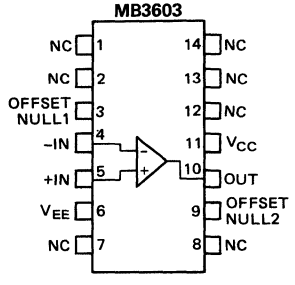
PLASTIC PACKAGE
DIP-08P-M01

CERAMIC PACKAGE
DIP-08C-C01

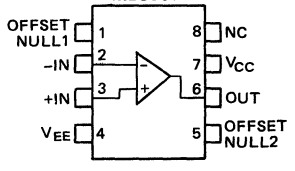
MB3609

PIN ASSIGNMENT

MB3603



MB3609



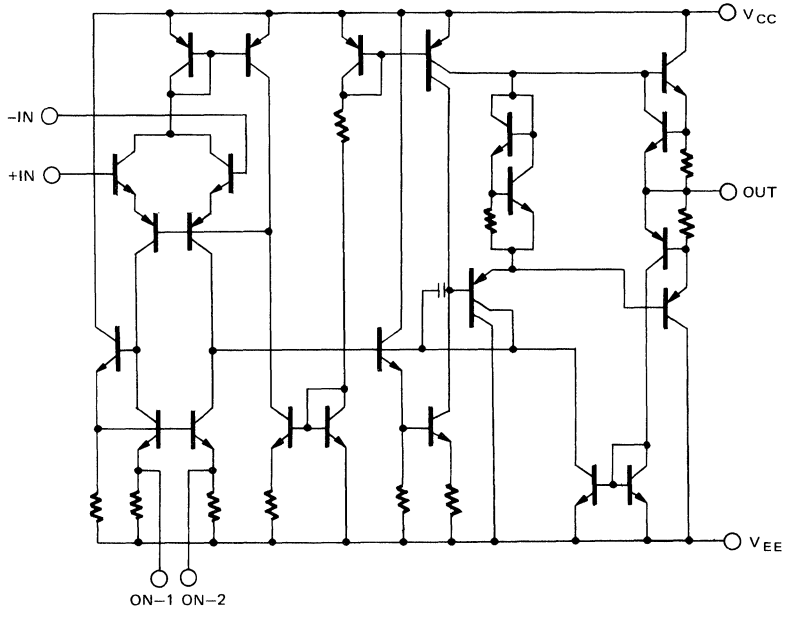
ABSOLUTE MAXIMUM RATINGS (See NOTE) (T_A = 25°C)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	+18	V
Power Supply Voltage		V_{EE}	-18	V
Differential Input Voltage		V_{ID}	±30	V
Common-mode Input Voltage		V_I	±15	V
Power Dissipation		P_D	500	mW
Storage Temperature	Plastic	T_{STG}	-55 to 125	°C
	Ceramic		-65 to 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB3603/3609 EQUIVALENT CIRCUITS



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	6 to 15	V
Power Supply Voltage	V_{EE}	−6 to −15	V
Operating Temperature	T_A	−20 to +75	°C

DC CHARACTERISTICS

(V_{CC} = +15V, V_{EE} = −15V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Input Offset Voltage	V_{IO}	R_S = 10kΩ, V_O = 0		10	mV
Input Offset Current	I_{IO}	V_O = 0		220	nA
Input Bias Current	I_I	V_O = 0		600	nA
Voltage Gain	A_V	R_L = 2kΩ, V_O = ±10V	15,000		
Common-mode Rejection Ratio	CMRR	V_I = ±7.5V	70		dB
Power Supply Rejection Ratio	SVRR	R_S = 10kΩ, ΔV_{CC} = 2.5V, ΔV_{EE} = 2.5V, V_O = 0		150	μV/V
Maximum Output Voltage	V_{OM}	R_L = 2kΩ	±10		V
Common-mode Input Voltage	V_{CM}		±12		V
Power Supply Current	I_{SUP}	V_O = 0		3.1	mA
Input Resistance	R_{IN}		300		kΩ

AC CHARACTERISTICS

(V_{CC} = +15V, V_{EE} = −15V, T_A = 25 ± 2°C)

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Frequency Bandwidth	BW	R_L = 2kΩ	100		kHz
Slew Rate	SR	R_L = 2kΩ, V_O = ±10V	0.1		V/μs

1

TYPICAL CHARACTERISTICS CURVES

Fig. 2 – OPEN LOOP VOLTAGE GAIN vs. POWER SUPPLY VOLTAGE

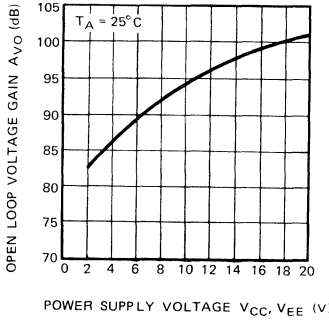


Fig. 3 – OUTPUT VOLTAGE vs. POWER SUPPLY VOLTAGE

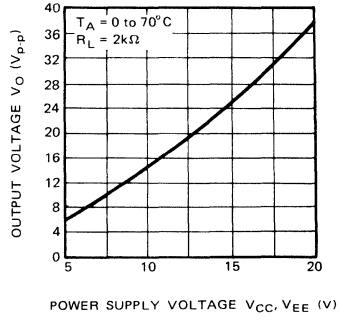


Fig. 4 – COMMON-MODE INPUT VOLTAGE vs. POWER SUPPLY VOLTAGE

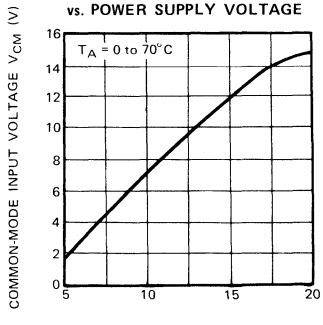


Fig. 5 – INPUT BIAS CURRENT vs. TEMPERATURE

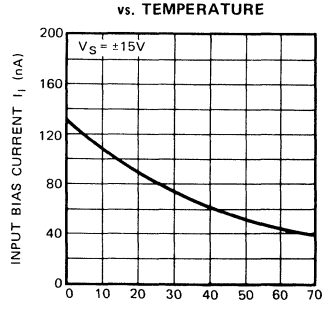


Fig. 6 – INPUT OFFSET CURRENT vs. TEMPERATURE

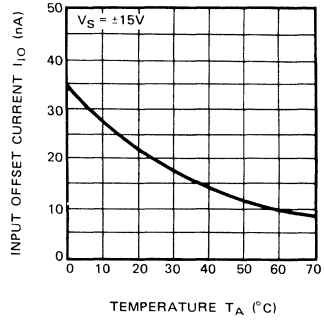


Fig. 7 – OUTPUT VOLTAGE vs. LOAD RESISTANCE

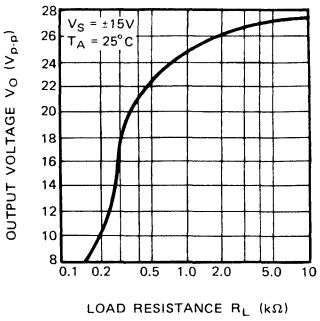


Fig. 8 – OPEN LOOP VOLTAGE GAIN vs. FREQUENCY

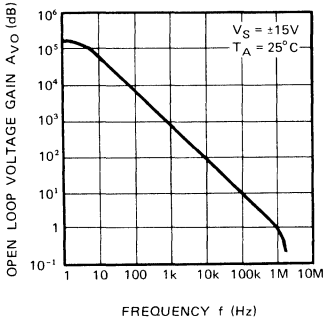


Fig. 9 – OUTPUT VOLTAGE vs. FREQUENCY

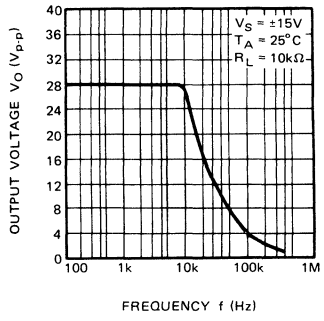
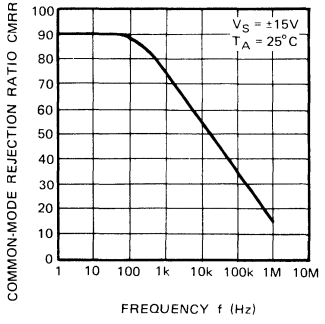


Fig. 10 – COMMON-MODE REJECTION RATIO vs. FREQUENCY



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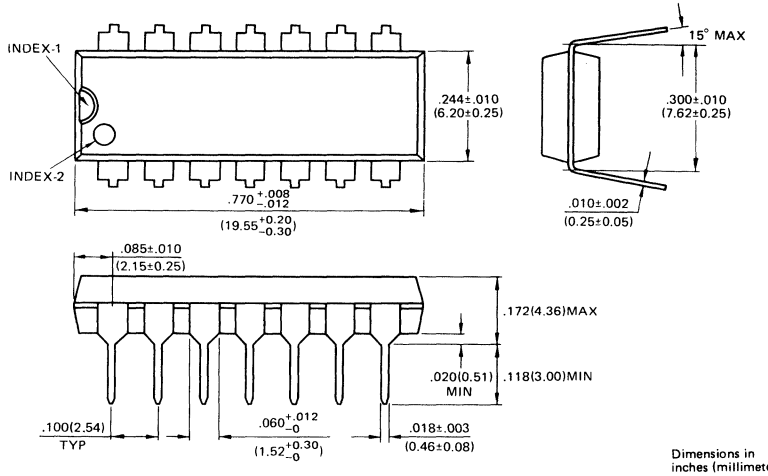
PACKAGE DIMENSIONS (MB3603)

14-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-14P-M02)



Dimensions in inches (millimeters)

14-LEAD CERAMIC CERDIP DUAL IN-LINE PACKAGE
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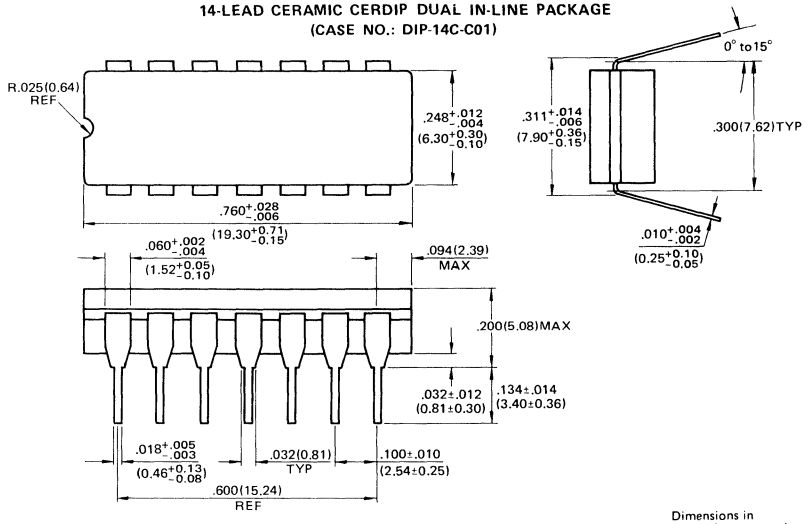

Dimensions in inches (millimeters)

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PACKAGE DIMENSIONS (MB3609)

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
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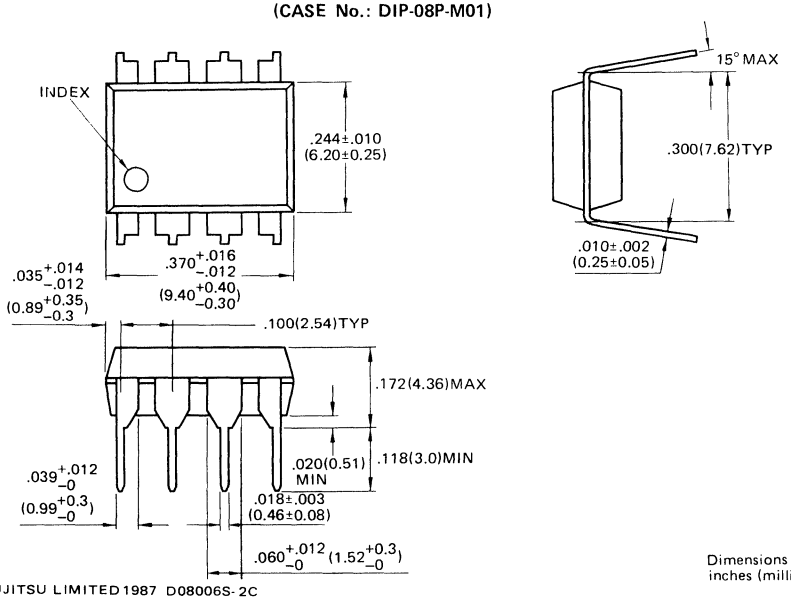

Dimensions in
inches (millimeters)

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PACKAGE DIMENSIONS (MB3609)

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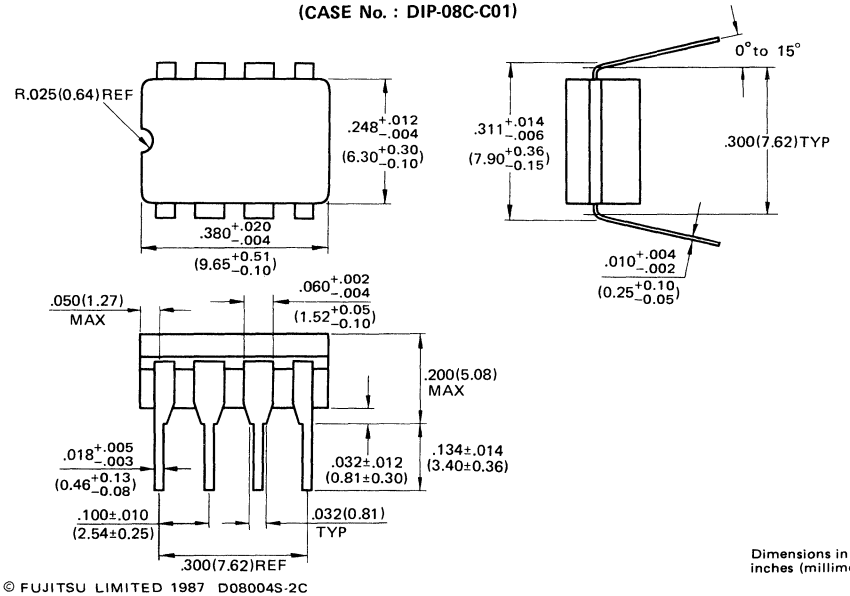
(CASE No. : DIP-08C-C01)



Dimensions in inches (millimeters)

FUJITSU

HIGH FREQUENCY OPERATIONAL AMPLIFIER

MB3604

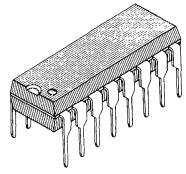
1

December 1987
Edition 1.0

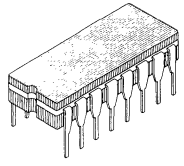
HIGH FREQUENCY OPERATIONAL AMPLIFIER

The Fujitsu MB3604 is a monolithic high frequency operational amplifier fabricated by Fujitsu Bipolar Technology.

The MB3604 has differential inputs, single-end output, and an on-chip buffer transistor for video band use.

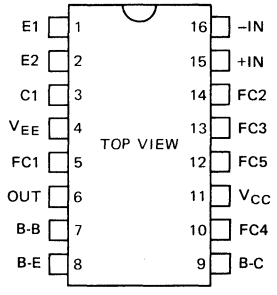


PLASTIC PACKAGE
DIP-16P-M04



CERAMIC PACKAGE
DIP-16C-C01

PIN ASSIGNMENT



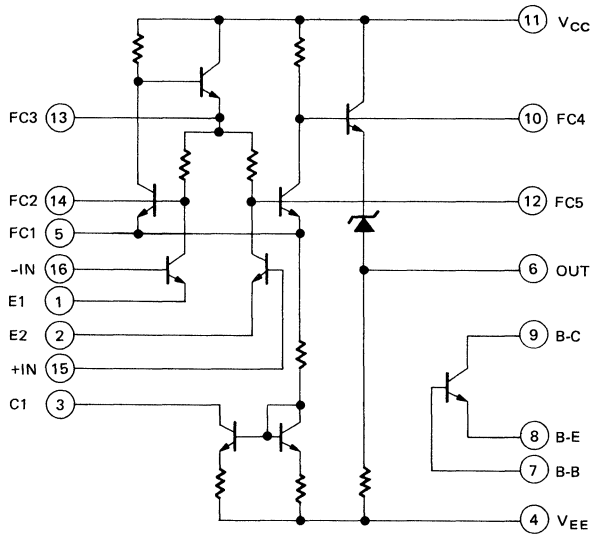
ABSOLUTE MAXIMUM RATINGS (See NOTE) (T_A = 25°C)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	+14	V
Power Supply Voltage		V_{EE}	−7	V
Differential Input Voltage		V_{ID}	±5	V
Common Mode Input Voltage		V_I	−7 to +1.4	V
Output Current		I_O	10	mA
Collector-Emitter Voltage for Buffer Transistor		V_{CEO}	21	V
Collector Current for Buffer Transistor		I_C	50	mA
Power Dissipation		P_D	500	mW
Storage Temperature	Ceramic	T_{STG}	−65 to +150	°C
	Plastic		−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB3604 EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+12±5%	V
Power Supply Voltage	V_{EE}	-6±5%	V
Operating Temperature	T_A	-20 to +75	°C

1

ELECTRICAL CHARACTERISTICS - I

(V_{CC} = +12V, V_{EE} = -6V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Input Offset Voltage	V_{IO}	R_S = 50Ω		6.0	mV
Input Offset Current	I_{IO}			5.0	μA
Input Bias Current	I_I			20	μA
Voltage Gain	A_V	$R_L \geq 5k\Omega$	60		dB
Common Mode Rejection Ratio	CMRR	R_S = 50Ω	70		dB
Maximum Positive Output Voltage	$V_{OM}(+)$	V_{IN} = 0.1V	4.0		V
Maximum Negative Output Voltage	$V_{OM}(-)$	V_{IN} = 0.1V	5.5		V
0dB Frequency	f_O	R_S = 50Ω, R_L = 50Ω	90		MHz
Input Resistance	R_{IN}	f = 1kHz	3.0		kΩ
Power Supply Current	$I_{SUP}(+)$			9.0	mA
Power Supply Current	$I_{SUP}(-)$			6.7	mA
Collector Cutoff Current for Buffer Transistor	I_{CBO}	V_{CB} = 18V, I_E = 0		2.0	μA
DC Current Gain for Buffer Transistcr	h_{FE}	V_{CB} = 6V, I_C = 20mA	40	200	

ELECTRICAL CHARACTERISTICS - II

(V_{CC} = +12V, V_{EE} = -6V, T_A = 25°C)

Parameter	Symbol	Condition	Value		Unit
			Min	Max	
Output Resistance	R_O	f = 1kHz		200	Ω
3dB Frequency	f_C	R_S = 50Ω, R_L = 50Ω	1		MHz
Slew Rate	SR	$A_V \doteq 1$, R_I = 50Ω	10		V/μs
Current Gain-Bandwidth Product for Buffer Transistor	f_T	V_{CE} = 6V, I_C = 20mA	300		MHz
Collector Capacitance for Buffer Transistor	C_{ob}	V_{CE} = 6V, I_E = 0A, f = 1MHz		5	pF

1

MEASUREMENT CIRCUT DIAGRAM

Fig. 2 – 0dB FEEDBACK AMPLIFIER

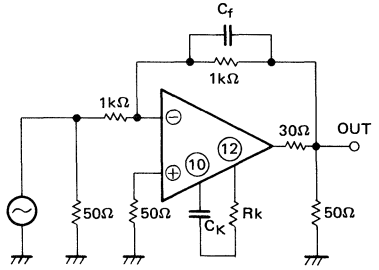


Fig. 3 – 20dB FEEDBACK AMPLIFIER

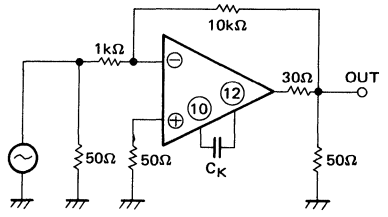
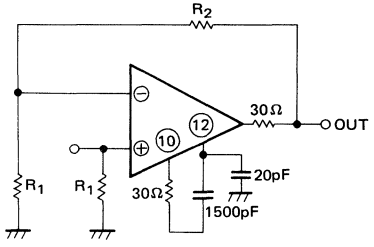


Fig. 4 – LOW FREQUENCY FEEDBACK AMPLIFIER



PIN CONNECTION FOR Fig. 2 to Fig. 5

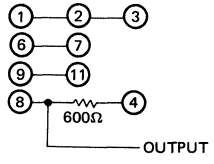


Fig. 5 – FREQUENCY CHARACTERISTICS MEASUREMENT CIRCUIT

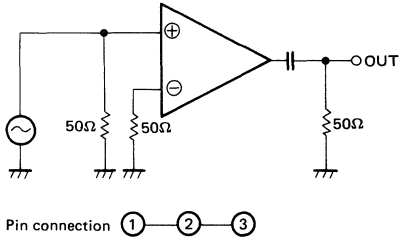
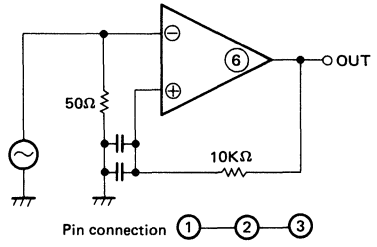


Fig. 6 – POWER SUPPLY VOLTAGE vs. VOLTAGE GAIN MEASUREMENT CIRCUIT



1

ELECTRICAL CHARACTERISTICS CURVES

Fig. 7 – 0dB FEEDBACK AMPLIFIER

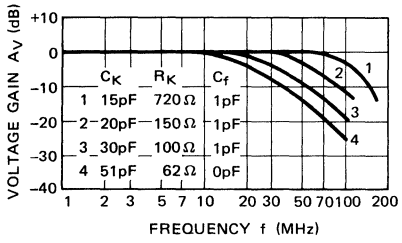


Fig. 8 – 20dB FEEDBACK AMPLIFIER

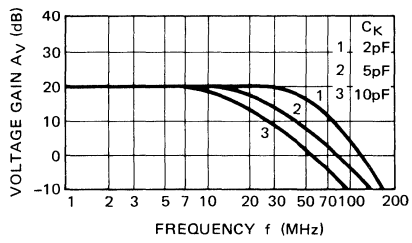


Fig. 9 – LOW FREQUENCY FEEDBACK AMPLIFIER

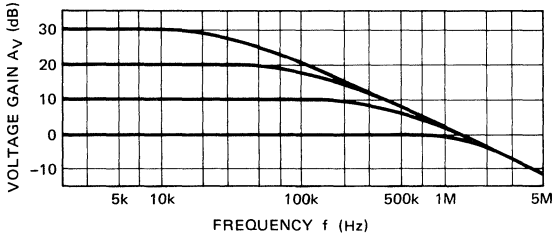


Fig. 10 – FREQUENCY CHARACTERISTICS

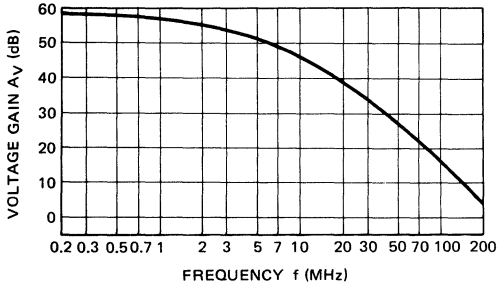
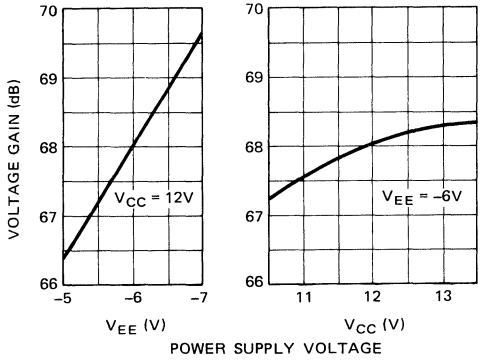


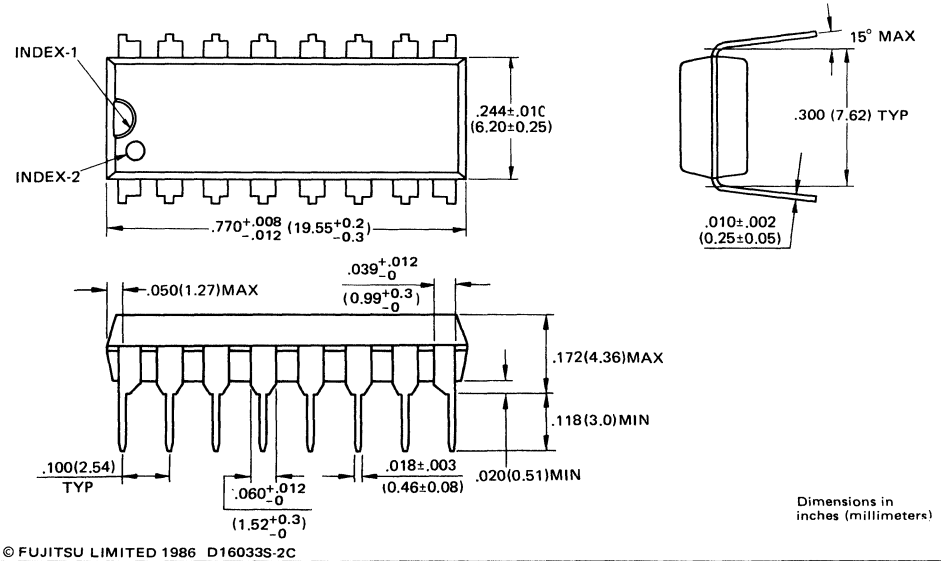
Fig. 11 – POWER SUPPLY VOLTAGE vs. VOLTAGE GAIN



1

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)



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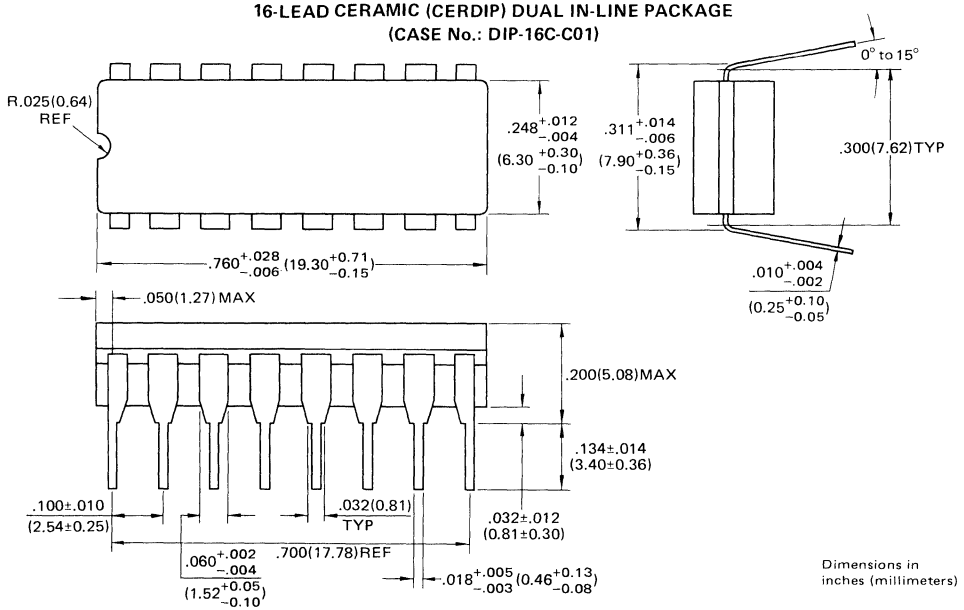
PACKAGE DIMENSIONS

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-C01)



FUJITSU

DUAL OPERATIONAL AMPLIFIER

MB3607

May 1988
Edition 1.0

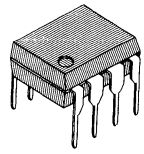
DUAL OPERATIONAL AMPLIFIER

The Fujitsu MB3607 is a dual silicon monolithic operational amplifier with on-chip internal frequency compensation circuitry, high input resistance and high gain.

It enables higher integration of function without increasing of mounting density because it integrates two circuitry on chip in one package.

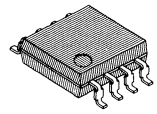
The MB3607 is compatible with MC1458.

- No frequency compensation required.
- On-chip over load protection circuitry.
- Not required external component for frequency compensation due to adoption of internal frequency compensation circuitry.
- High input resistance, large common-mode input voltage and large differential input voltage.
- High common-mode ripple rejection ratio.
- Owing to adoption of active load, low power consumption, high gain are achieved.
- No latch-up



PLASTIC PACKAGE
DIP-08P-M01

CERAMIC PACKAGE
DIP-08C-C01



PLASTIC PACKAGE
FPT-08P-M01

ABSOLUTE MAXIMUM RATINGS (See NOTE) (T_A = 25°C)

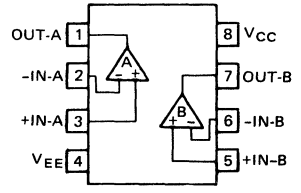
Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	+18	V
Power Supply Voltage		V_{EE}	-18	V
Differential Input Voltage		V_{ID}	±30*	V
Common-mode Input Voltage		V_I	±15*	V
Power Dissipation		P_D	500	mW
Storage Temperature	Plastic	T_{STG}	-55 to 125	°C
	Ceramic		-65 to 150	°C

* When power supply voltage V_{CC} is less than ±15V, $V_{ID} = \pm(V_{CC} + |V_{EE}|)$, V_I is equal to the V_{CC}.

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT

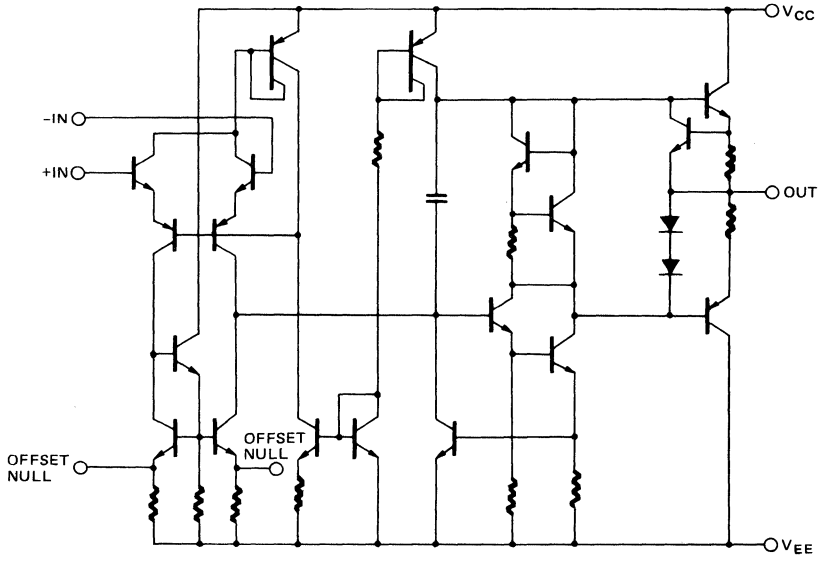
(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB3607 EQUIVALENT CIRCUIT



1

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	6 to 15	V
Power Supply Voltage	V_{EE}	−6 to −15	V
Operating Temperature	T_A	−20 to +75	°C

DC CHARACTERISTICS

(V_{CC} = +15V, V_{EE} = −15V, T_A = 25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Offset Voltage	V_{IO}	R_S = 10kΩ, V_O = 0V		1.0	6.0	mV
		R_S = 10kΩ, V_O = 0V, T_A = 0 to 70°C			7.5	
Input Offset Current	I_{IO}	V_O = 0V		20	200	nA
		V_O = 0V, T_A = 0 to 70°C			300	
Input Bias Current	I_I	V_O = 0V		80	500	nA
		V_O = 0V, T_A = 0 to 70°C			800	
Voltage Gain	A_V	R_L = 2kΩ, V_O = ±10V	15000			
Common-mode Rejection Ratio	CMRR	V_I = ±7.5V	70			dB
Power Supply Rejection Ratio	SVRR	R_S = 10kΩ			150	μV/V
Maximum Output Voltage	V_{OM}	R_L = 2kΩ	±10			V
Common-mode Input Voltage	V_{CM}		±12			V
Input Resistance	R_{IN}		300			kΩ
Power Supply Current	I_{SUP}	V_O = 0V		3.4	5.6	mA
		V_O = 0V, T_A = 0 to 70°C			6.2	

AC CHARACTERISTICS

(V_{CC} = +15V, V_{EE} = −15V, T_A = 25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Frequency Bandwidth	BW	R_L = 2kΩ, 0dB	0.1	1.0		MHz
Slew Rate	SR	R_L = 2kΩ, A_V = 1	0.25	0.6		V/μs
Channel Separation	CS	R_L = 2kΩ, f = 1kHz	55			dB

1

TYPICAL CHARACTERISTICS CURVES

Fig. 2 – OPEN LOOP VOLTAGE GAIN vs. POWER SUPPLY VOLTAGE

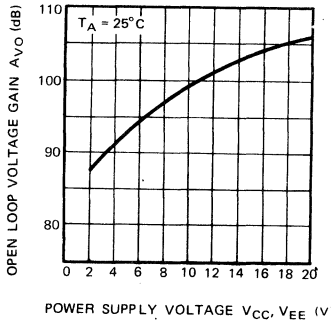


Fig. 3 – OUTPUT VOLTAGE vs. POWER SUPPLY VOLTAGE

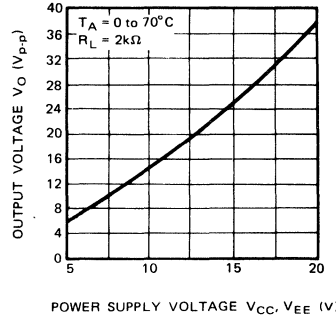


Fig. 4 – COMMON-MODE INPUT VOLTAGE vs. POWER SUPPLY VOLTAGE

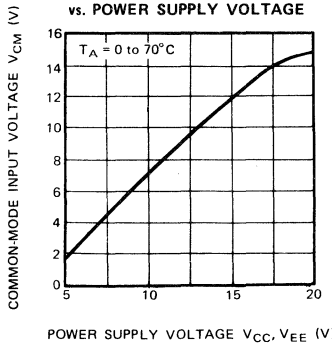


Fig. 5 – INPUT BIAS CURRENT vs. TEMPERATURE

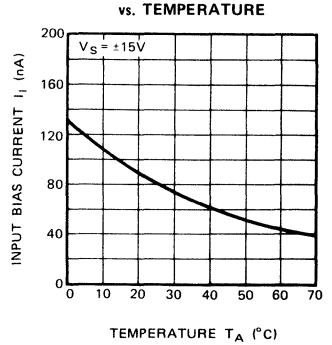


Fig. 6 – INPUT OFFSET CURRENT vs. TEMPERATURE

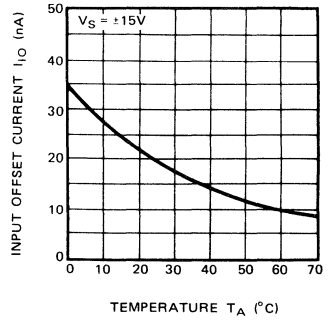


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Fig. 7 – OUTPUT VOLTAGE vs. LOAD RESISTANCE

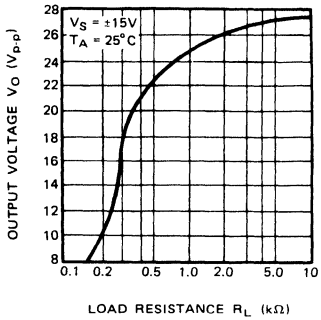


Fig. 8 – OPEN LOOP VOLTAGE GAIN vs. FREQUENCY

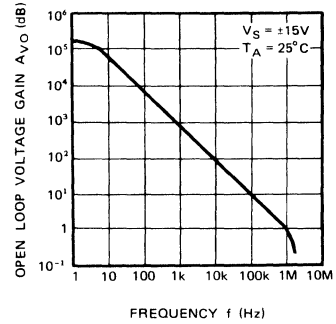


Fig. 9 – OUTPUT VOLTAGE vs. FREQUENCY

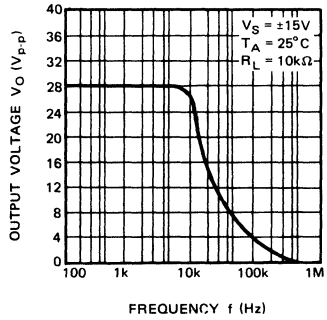
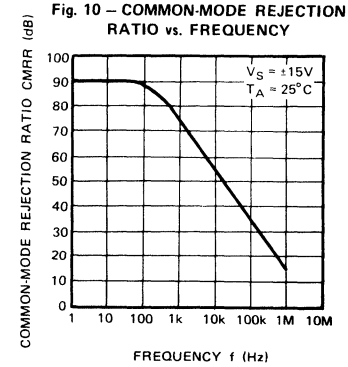


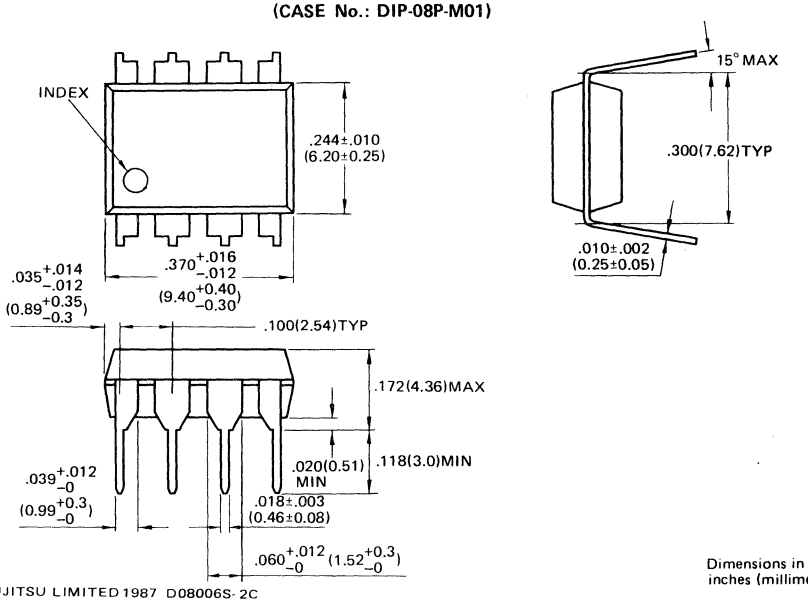
Fig. 10 – COMMON-MODE REJECTION RATIO vs. FREQUENCY



1

PACKAGE DIMENSIONS

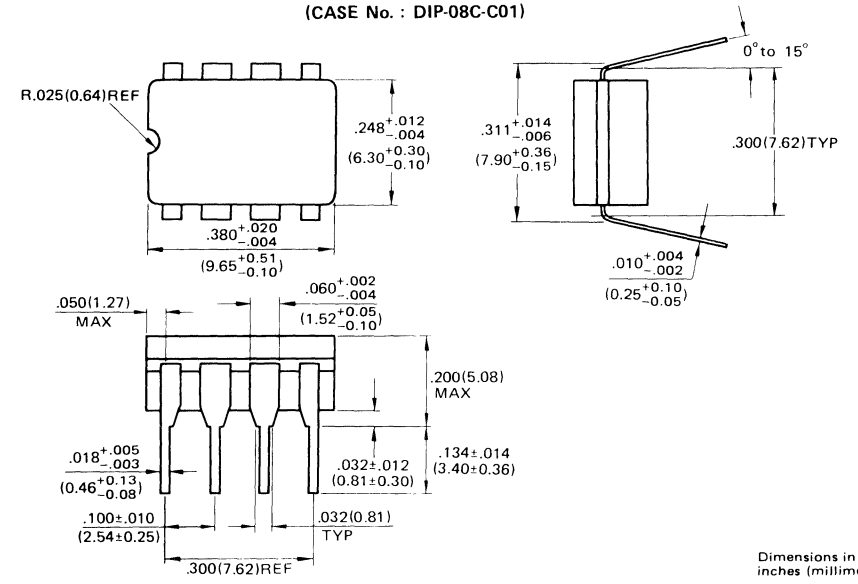
8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in
inches (millimeters)

1

8-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-08C-C01)

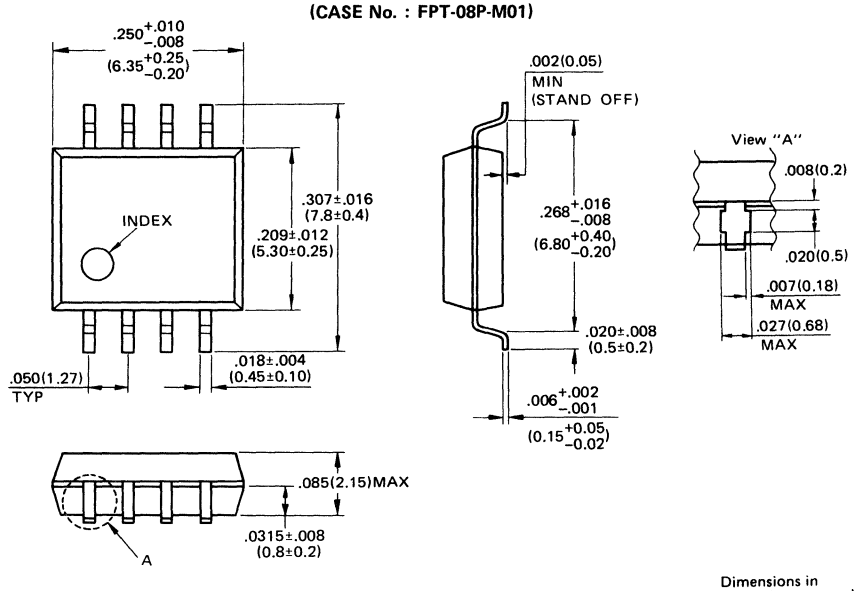


Dimensions in inches (millimeters)

1

PACKAGE DIMENSIONS (continued)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-08P-M01)



Dimensions in
inches (millimeters)

FUJITSU

QUAD OPERATIONAL AMPLIFIER

MB3614

September 1988
Edition 1.0

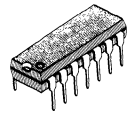
QUAD OPERATIONAL AMPLIFIER

The Fujitsu MB3614 is a Quad operational amplifier having a phase compensatory circuitry and operates from a single power supply or dual power supplies.

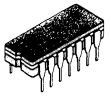
The device has equivalent electrical characteristics of current industrial standard operational amplifier and requires low power supply current.

MB3614 can be high density mounted because it integrates 4 circuits in DIP/FPT 14-pin package.

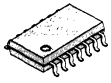
- No phase compensation required
- Wide power supply voltage
  - — Single power supply: +3 to +30 V
  - — Dual power supplies: ±1.5 to ±15 V
- Wide input common mode range: 0 to (Vcc -1.5) V
- Low power supply current: 0.8 mA typ.
- Low input offset voltage: 2 mV typ.
- Package
  - — 14-pin Plastic DIP package (Suffix: -P)
  - — 14-pin Ceramic DIP package (Suffix: -Z)
  - — 14-pin Plastic FPT package (Suffix: -PF)



PLASTIC PACKAGE
DIP-14P-M02



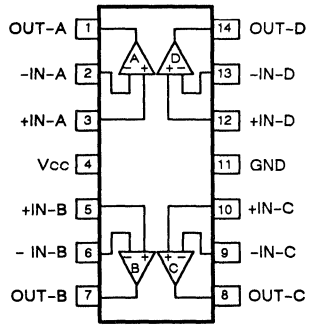
CERAMIC PACKAGE
DIP-14C-C04



PLASTIC PACKAGE
FPT-14P-M01

PIN ASSIGNMENT

(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS (see NOTE)

(TA=25°C)

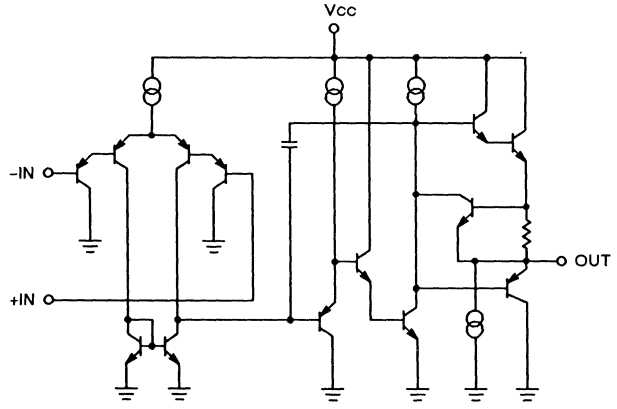
Rating		Symbol	Value	Unit
Power Supply Voltage		Vcc	36	V
Differential Input Voltage		VID	36	V
Input Common Mode Voltage		Vi	-0.3 to +36	V
Power Dissipation		PD	570	mW
Operating Temperature		TA	-20 to +75	°C
Storage Temperature	Plastic	TSTG	-55 to +125	°C
	Ceramic	TSTG	-65 to +150	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 — EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (Vcc = 5 V, TA = 25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Offset Voltage	V_{IO}			2	7	mV
Input Offset Current	I_{IO}			5	50	nA
Input Bias Current	I_I *			45	250	nA
Power Supply Current	I_{CC}	$R_L = \infty$		0.8	2.0	mA
Input Common Mode Voltage	V_{CM}		0		Vcc -1.5	V
Voltage Gain	A_V	$R_L \geq 2k\Omega$	25	100		V/mV
Output Voltage	V_{OH}	V_{CC} = 30V, R_L = 2kΩ	26	28		V
	V_{OL}	V_{CC} = 5V, $R_L \leq 10k\Omega$		5	20	mV
Output Current	I_{SOURCE}	V_{CC} = 15V, V_{IN} + = 1V	20	40		mA
	I_{SINK}	V_{CC} = 15V, V_{IN} − = 1V	10	20		mA
Common Mode Rejection Ratio	CMRR		65	85		dB
Power Supply Voltage Rejecton Ratio	SVRR		65	100		dB
Channel Separation	CS			120		dB

Note:

* A direction of the input bias current flows from IC because first input transistor consists of PNP.

TYPICAL CHARACTERISTICS CURVES

Fig. 2 - Power Supply Current vs. Power Supply Voltage

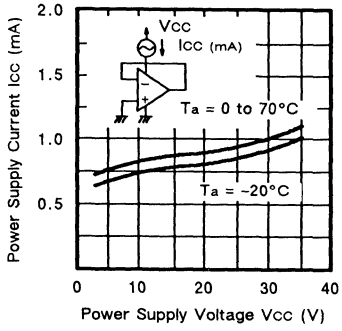


Fig. 3 - Input Bias Current vs. Temperature

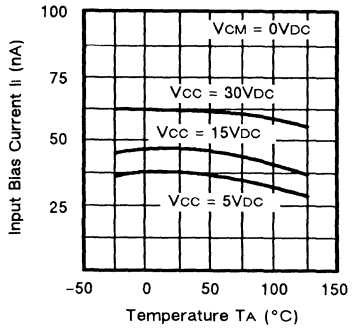


Fig. 4 - Voltage Gain vs. Power Supply Voltage

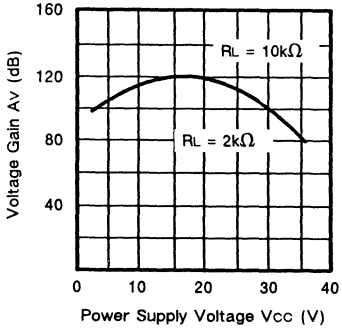


Fig. 5 - Voltage Gain vs. Frequency

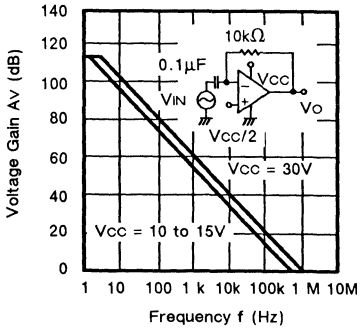


Fig. 6 - Output Voltage vs. Frequency

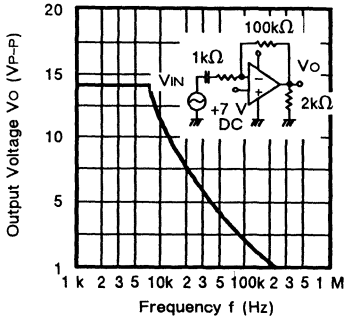
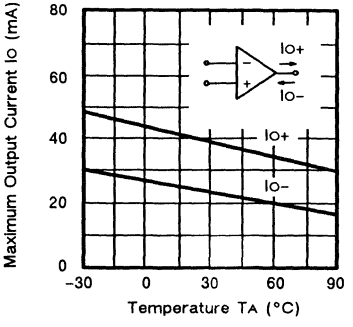


Fig. 7 - Maximum Output Voltage vs. Temperature



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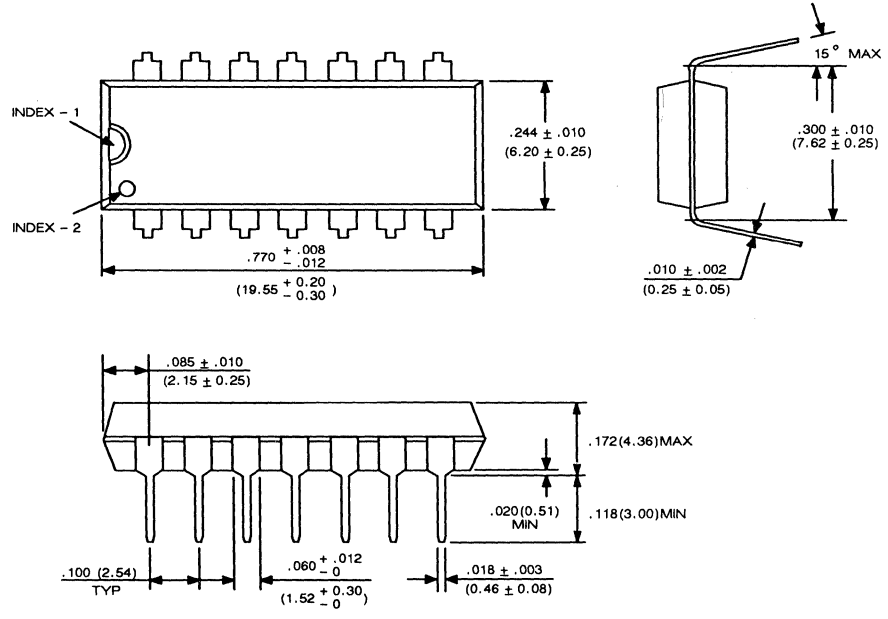
14-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-14P-M02)

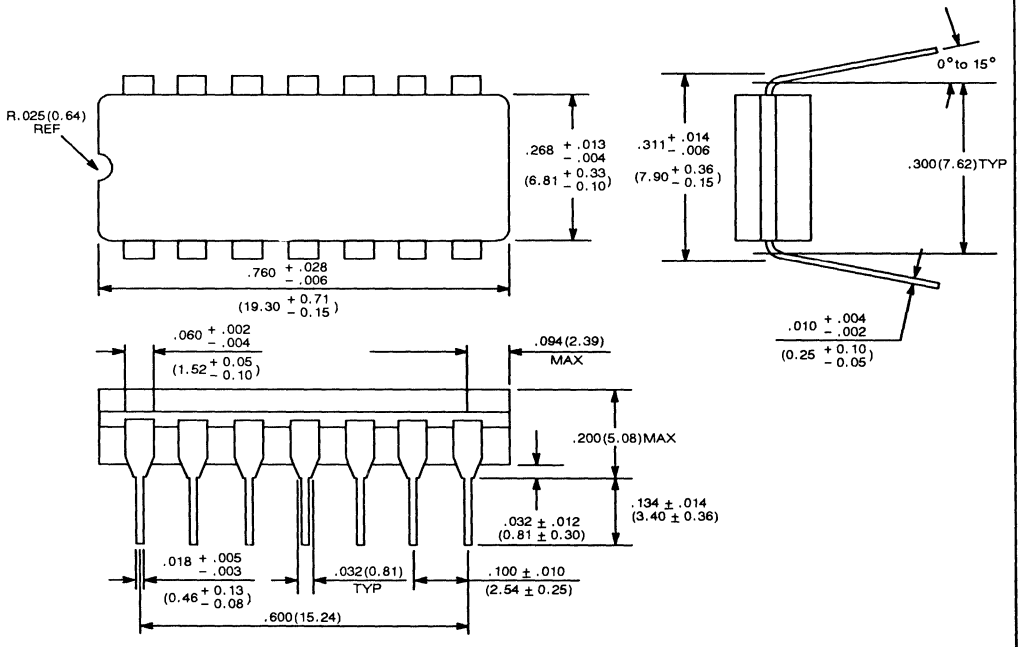


Dimensions in
inches (millimeters)

D14010S-3C

1

14-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(CASE NO.: DIP-14C-CO4)

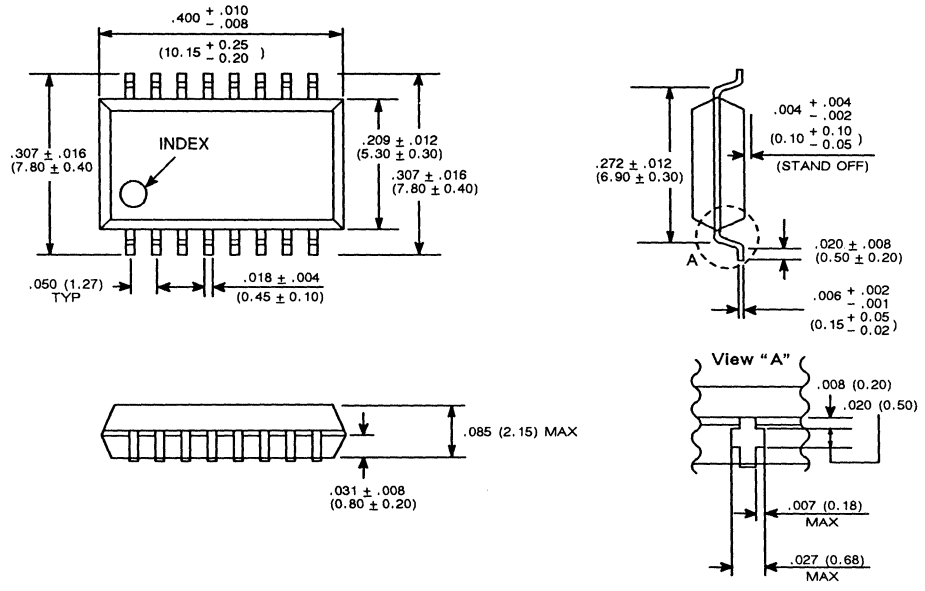


Dimensions in
inches (millimeters)

D14006S-2C

1

14-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-14P-M01)



Dimensions in
inches (millimeters)

F16005S-3C

QUAD OPERATIONAL AMPLIFIER

MB3615

November 1987
Edition 1.0

QUAD OPERATIONAL AMPLIFIER

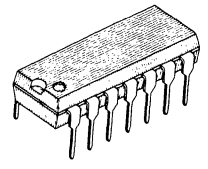
The Fujitsu MB3615 is a Quad operational amplifier having a phase compensatory circuit and operates from a single power supply or dual power supplies.

The device has equivalent electrical characteristics of current industrial standard operational amplifier and requires low power supply current.

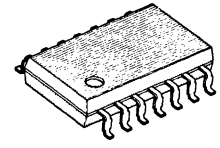
MB3615 can be mounted in high density because it integrates 4 circuits on a chip in 14-pin package. It is taking the countermeasure for cross-over distortion, so can be used for amplifying AC.

The MB3615 is pin compatible with Motorola MC3303.

- No phase compensation required
- Wide power supply voltage
  - — Single power supply: +3 to +36 V
  - — Dual power supplies: ±1.5 to ±18 V
- Wide input common mode range: V_{EE} to (V_{CC} −1.5) V
- Low power supply current: 2 mA typ.
- Low Cross-over distortion

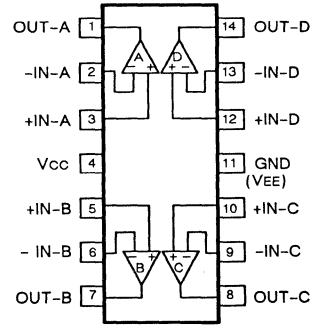


PLASTIC PACKAGE
DIP-14P-M02



PLASTIC PACKAGE
FPT-14P-M01

PIN ASSIGNMENT
(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

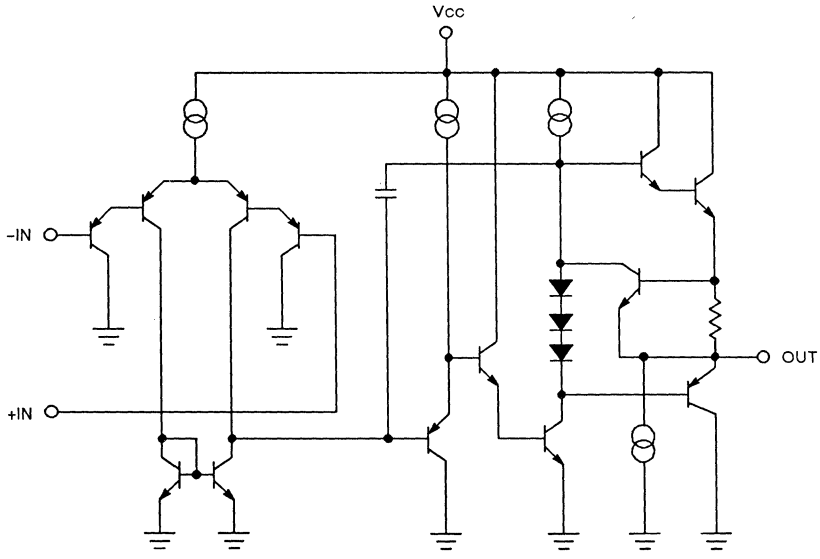
Rating	Symbol	Value	Unit
Power Supply Voltage *	V_{CC}	36	V
Differential Input Voltage *	V_{ID}	36	V
Input Common Mode Voltage *	V_I	−0.3 to +36	V
Power Dissipation	P_D	570	mW
Operating Temperature	T_A	−20 to +75	°C
Storage Temperature	T_{STG}	−55 to +125	°C

NOTE: * Single Power Supply.

Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1

Fig. 1 — MB3615 EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{CC} = +15V, V_{EE} = -15V, T_A = 25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Offset Voltage	V_{IO}			2	7	mV
Input Offset Current	I_{IO}			5	50	nA
Input Bias Current	I_I *			45	250	nA
Power Supply Current	I_{CC}	$R_L = \infty$		2.0	4.0	mA
Input Common Mode Voltage	V_{CM}		V_{EE}		V_{CC} -1.5	V
Voltage Gain	A_V	$R_L \geq 2k\Omega$	20	100		V/mV
Output Voltage	V_{OH}	$R_L = 2k\Omega$	± 10	12		V
	V_{OL}	$R_L = 10k\Omega$	± 12	13		V
Output Current	I_{SOURCE}		10	40		mA
	I_{SINK}		10	20		mA
Common Mode Rejection Ratio	CMRR		70	85		dB
Power Supply Voltage Rejection Ratio	SVRR		65	100		dB
Channel Separation	CS			120		dB

NOTE:

* A direction of the input bias current flows from IC because first input transistor consists of PNP.

1

TYPICAL CHARACTERISTICS CURVES

Fig. 2 - Power Supply Current vs. Power Supply Voltage

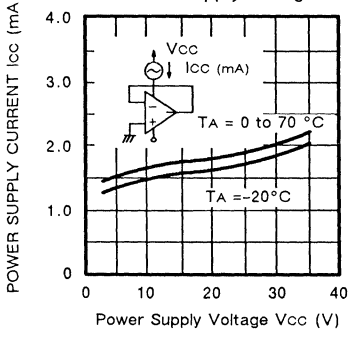


Fig. 3 - Input Bias Current vs. Temperature

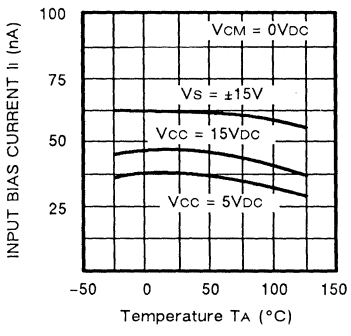


Fig. 4 - Voltage Gain vs. Power Supply Voltage

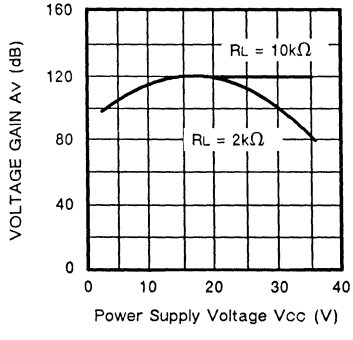


Fig. 5 - Voltage Gain vs. Frequency

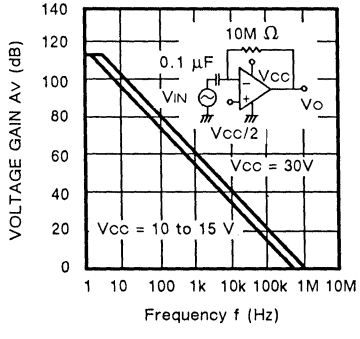


Fig. 6 - Output Voltage vs. Frequency

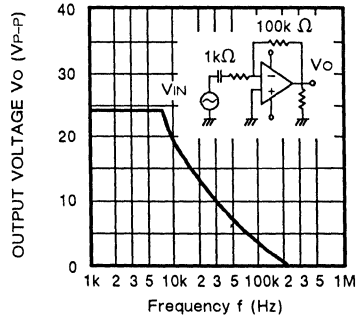
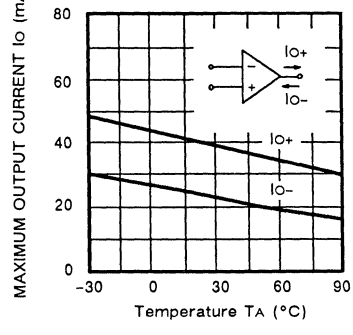


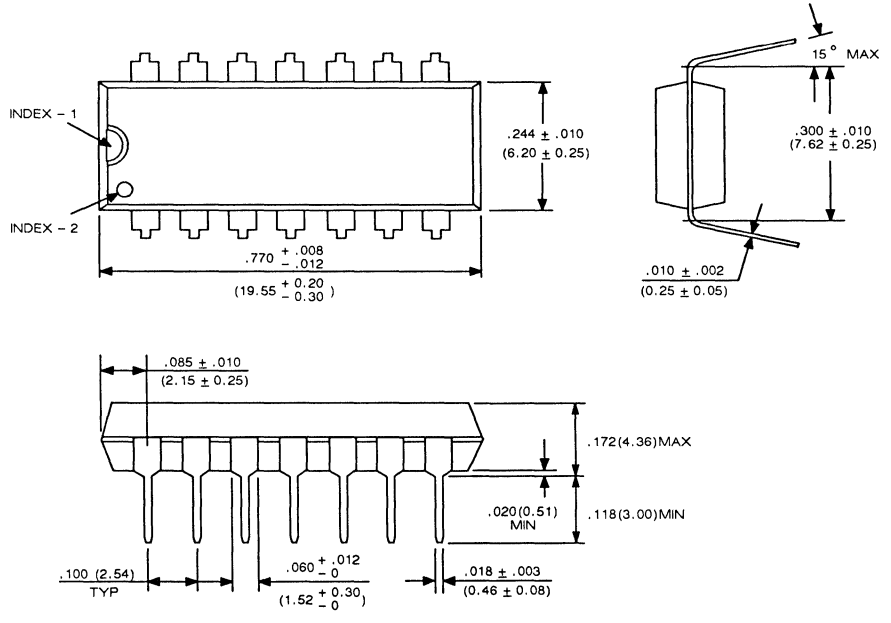
Fig. 7 - Maximum Output Current vs. Temperature



1

PACKAGE DIMENSIONS

14-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-14P-M02)



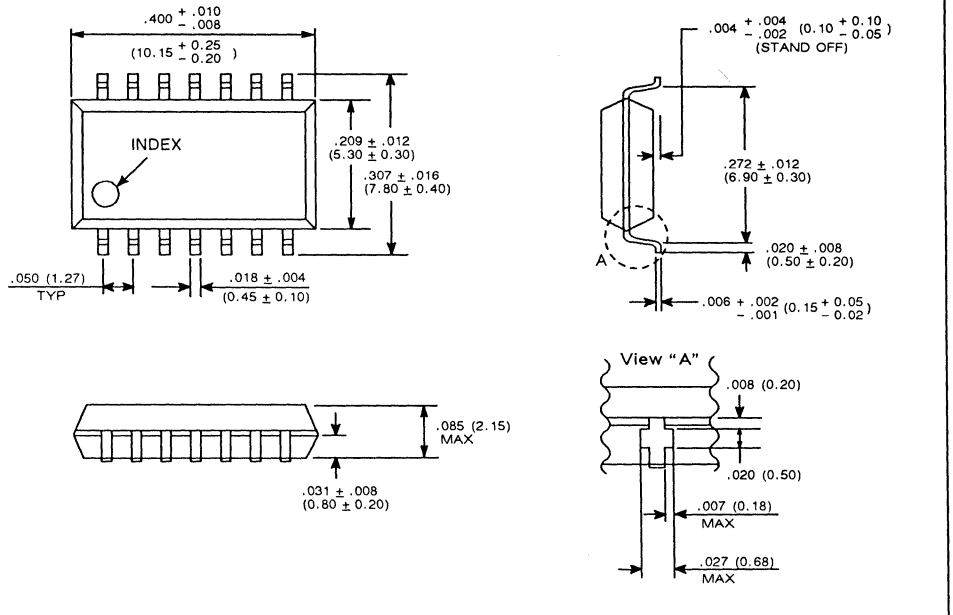
Dimensions in
inches (millimeters)

D14010S-3C

1

PACKAGE DIMENSIONS (Continued)

14-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-14P-M01)



Dimensions in
inches (millimeters)

F14003S-2C

FUJITSU

J-FET INPUT OPERATIONAL AMPLIFIER

MB47082

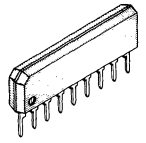
Apr. 1989
Edition 1.0

J-FET INPUT OPERATIONAL AMPLIFIER

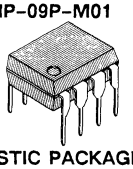
The Fujitsu MB47082 is designed for a dual operational amplifier with P channel-typed J-FET used at the input stage. Its slew rate is faster (more than one figure) comparing with the standard operational amplifier and also its band width is wide because of its high input impedance characteristics and well-built transmission conductance at the input stage comparing with the bipolar transistor.

The MB47082 is suitable for a D/A converter and a Sample & Hold circuit that need to cover from a small signal amplification to a fast and large signal change.

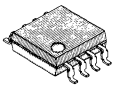
- Compatible with TL082
- Wide operating power supply voltage: ± 5V to ± 15V
- Fast slew rate : 13V/µs typ.
- Low input bias current : 30pA typ.
- Wide frequency bandwidth : 3MHz typ.
- On-chip internal frequency compensation
- Low noise



PLASTIC PACKAGE
SIP-09P-M01



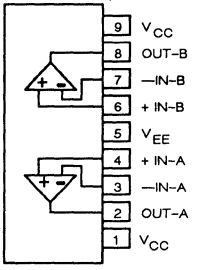
PLASTIC PACKAGE
DIP-08P-M01



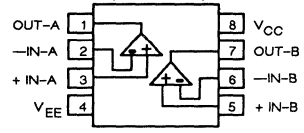
PLASTIC PACKAGE
FPT-08P-M01

PIN ASSIGNMENT

SIP: (FRONT VIEW)



DIP,FPT: (TOP VIEW)



ABSOLUTE MAXIMUM RATINGS (see NOTE)

(TA=25°C)

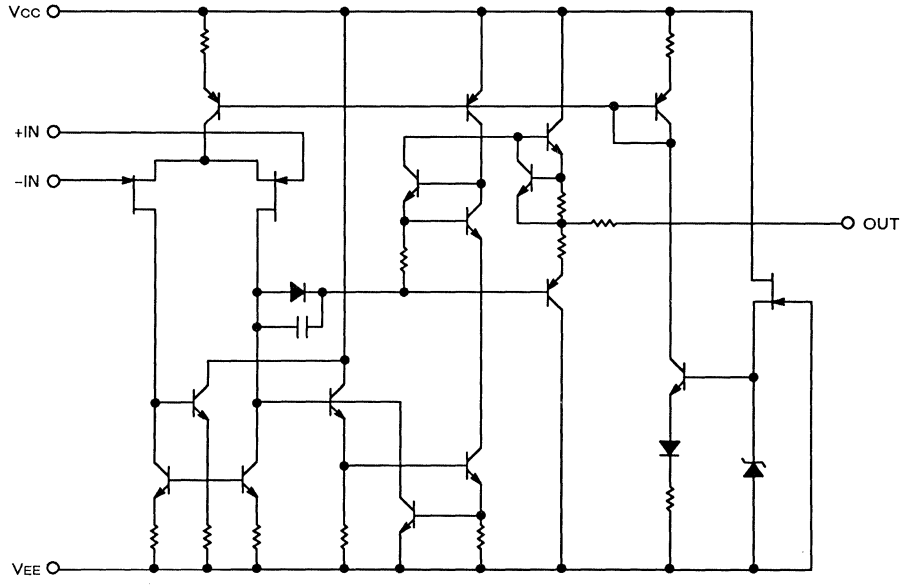
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	V
	V_{EE}	-18	V
Differential Input Voltage	V_{ID}	± 30	V
Common-mode Input Voltage	V_I	± 15	V
Power Dissipation	P_D	350 (TA ≤ 55°C)	mW
Operating Temperature	T_A	-20 to 75	°C
Storage Temperature	T_{STG}	-55 to 125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 — MB47082 EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}, V_{EE}	±5 to ±15	V
Operating Temperature	T_A	-20 to +75	°C

(T_A =25°C, V_{CC}=15V, V_{EE} =-15V)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Offset Voltage	V_{IO}	$R_S \leq 50\Omega$		5.0	15.0	mA
Input Offset Current	I_{IO}			5	200	pA
Input Bias Current	I_I			30	400	pA
Common-mode Input Voltage	V_{CM}		±10			V
Common-mode Rejection Ratio	CMRR	$R_S \leq 10k\Omega$	70	86		dB
Power Supply Voltage Rejection Ratio	SVRR	$R_S \leq 10k\Omega$	70	86		dB
Voltage Gain	A_V	R_L=2kΩ	25	200		V/mV
Power Supply Current	I_{CC}			3.5	5.6	mA
Maximum Output Voltage	V_{OM}	$R_L \geq 18k\Omega$	±12	±13.5		V
		$R_L \geq 2k\Omega$	±10	±12		V
Output Current	I_{SOURCE}	V_O=V_{EE}		-25	-10	mA
	I_{SINK}	V_O=V_{CC}	25	40		mA
Frequency Bandwidth	BW	R_L=2kΩ		3.0		MHz
Slew Rate	SR	R_L=2kΩ, C=100pF, AV=1		13		V/μs
Channel Separation	CS	f=1kHz		120		dB
Equivalent Input Noise Voltage	V_{NI}	f=1kHz, Rs=100Ω		25		$nV\sqrt{Hz}$

1

ELECTRICAL CHARACTERISTICS CURVES

Fig. 2 - Voltage Gain vs. Frequency

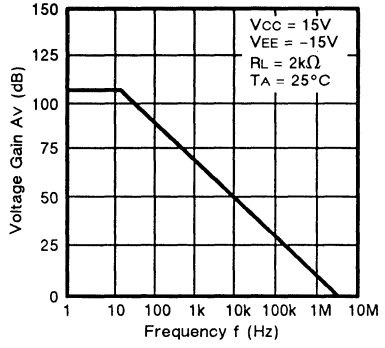


Fig. 3 - Output Voltage vs. Frequency

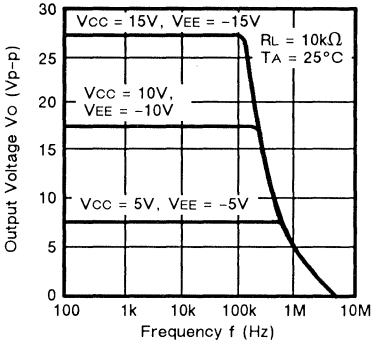


Fig. 4 - Input Bias Current vs. Common-Mode Input Voltage

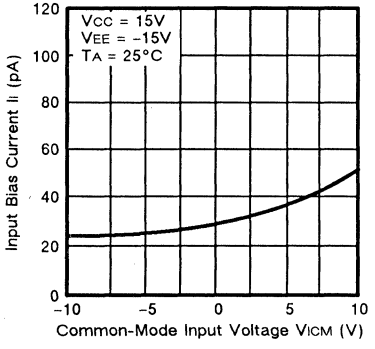


Fig. 5 - Input Bias Current vs. Temperature

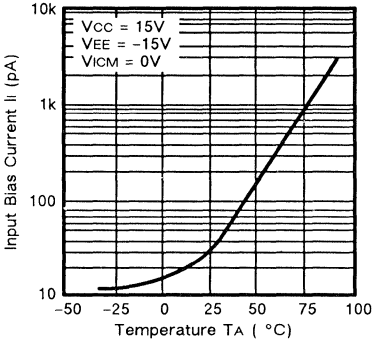


Fig. 6 - Output Voltage vs. Power Supply Voltage

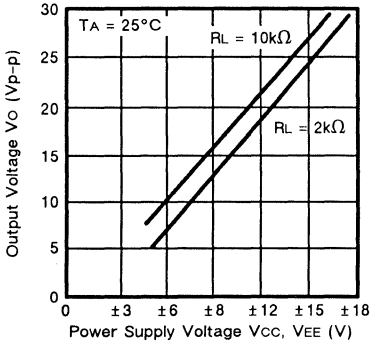
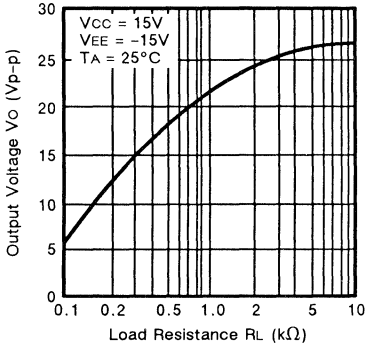


Fig. 7 - Output Voltage vs. Load Resistance



1

ELECTRICAL CHARACTERISTICS CURVES (Continued)

Fig. 8 - Input Noise Voltage vs. Frequency

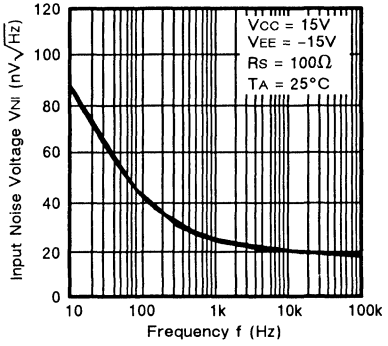


Fig. 9 - Pulse Response

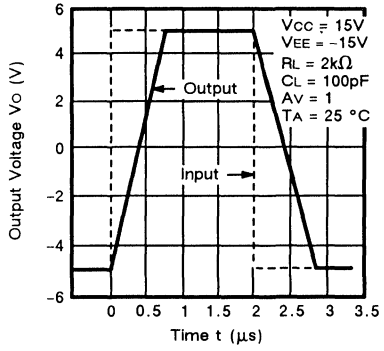


Fig. 10 - Power Supply Current vs. Power Supply Voltage

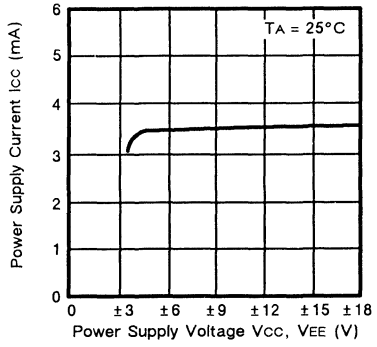
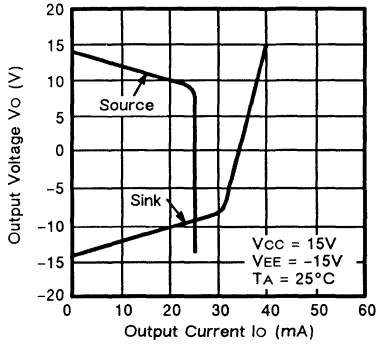


Fig. 11 - Output Voltage vs. Output Current



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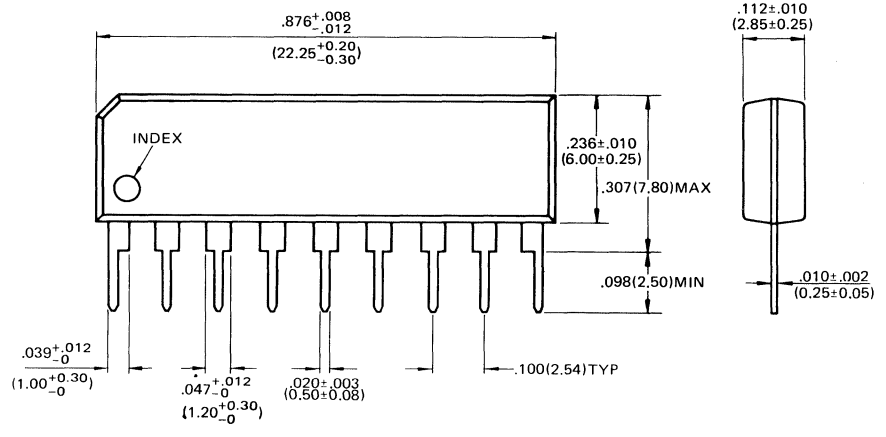
9-LEAD PLASTIC SINGLE-IN-LINE PACKAGE
(CASE No.: SIP-09P-M01)



Dimensions in
inches (millimeters)

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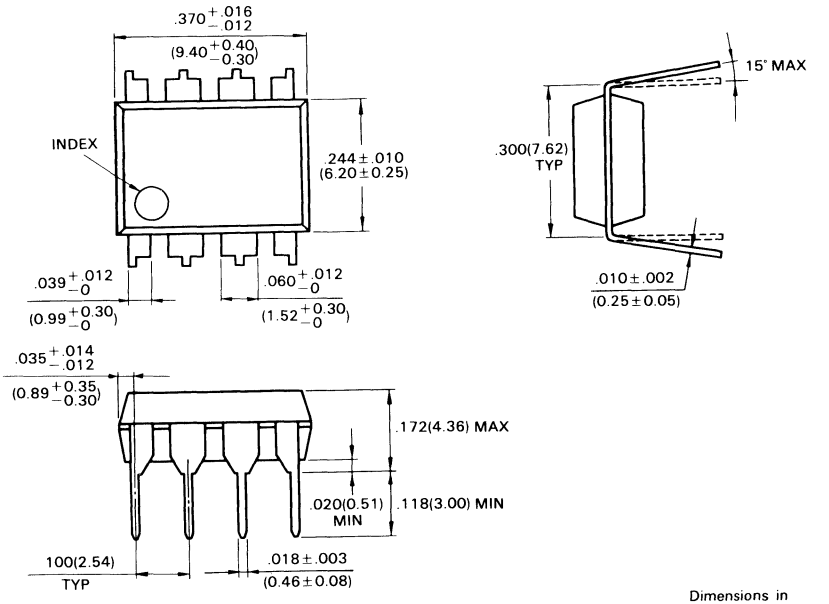
8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in inches (millimeters)

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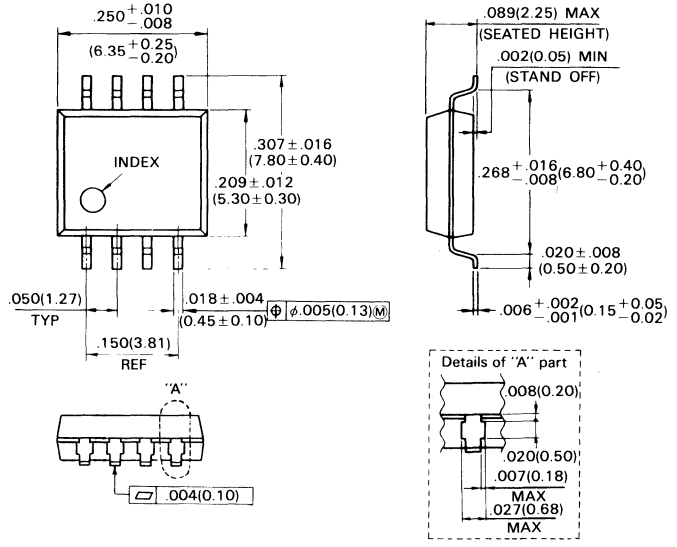
8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



Dimensions in
inches (millimeters)

FUJITSU

DUAL OPERATIONAL AMPLIFIER

MB47358

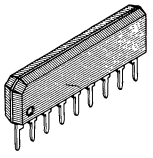
1

July 1988
Edition 2.0

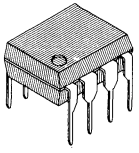
DUAL OPERATIONAL AMPLIFIER

The Fujitsu MB47358 is designed for a general purpose dual operational amplifier with internal frequency compensation and to operate from a single power supply or dual power supplies. The MB47358 is suitable for audio with the fast slew rate and with the reduction of cross-over distortion. The MB47358 fits an application of microcomputer because of its wide output voltage range. The MB47358 is compatible with LM358.

- Not required frequency compensation
- Wide power supply voltage range
  Single power supply: 3V to 30V
  Dual power supplies: ±1.5V to ±15V
- Wide output voltage range
- No cross-over distortion
- Fast slew rate – 2V/μs typ.



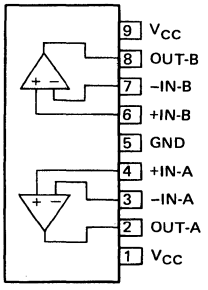
PLASTIC PACKAGE
SIP-09P-M01



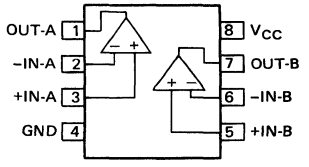
PLASTIC PACKAGE
DIP-08P-M01

FLAT PLASTIC PACKAGE See Page 7

PIN ASSIGNMENT
(FRONT VIEW: SIP)



(TOP VIEW: DIP, FPT)



ABSOLUTE MAXIMUM RATINGS (see NOTE) (T_A = 25°C)

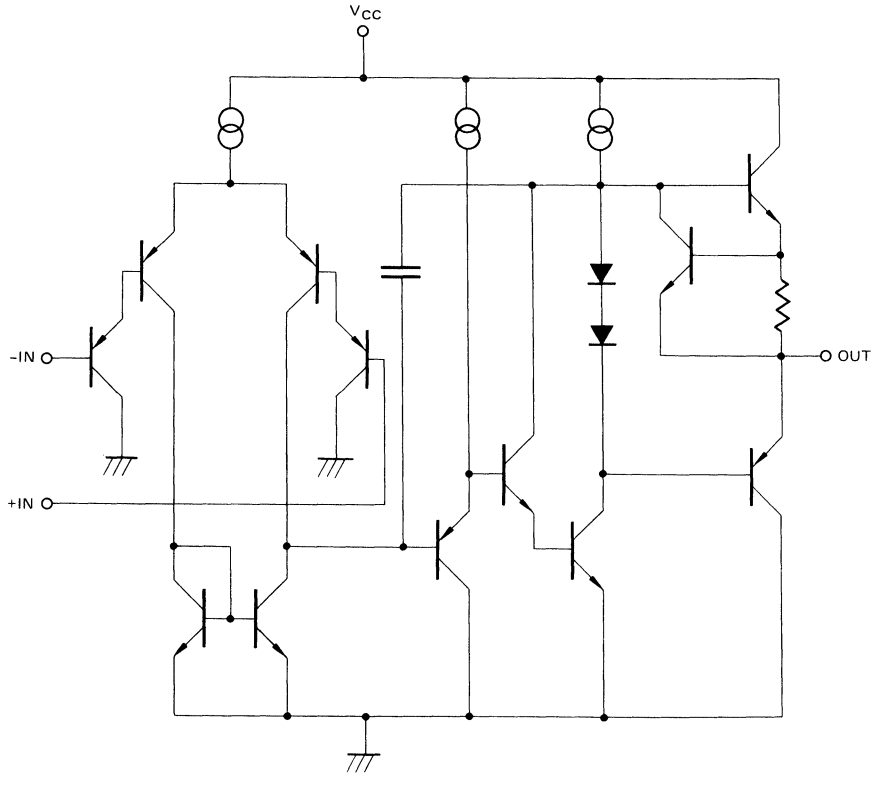
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	36	V
Differential Input Voltage	V_{ID}	36	V
Common-mode Input Voltage	V_{ICM}	-0.3 to +36	V
Power Dissipation	P_D	350 ($T_A \leq 55°C$)	mW
Operating Temperature	T_A	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

1

Fig. 1 – MB47358 EQUIVALENT CIRCUIT



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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	3 to 30	V
		±1.5 to ±15	
Operating Temperature	T_A	-20 to +75	°C

RECOMMENDED OPERATING CONDITIONS

(T_A = 25°C, V_{CC} = 5V)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Offset Voltage	V_{IO}		–	2	7	mV
Input Offset Current	I_{IO}		–	5	50	nA
Input Bias Current	I_I *		–	45	250	nA
Power Supply Current	I_{CC}	$R_L = \infty$, V_{CC} = 5V	–	2.0	3.0	mA
Common-mode Input Voltage	V_{ICM}		0	–	V_{CC}-1.5	V
Voltage Gain	A_V	$R_L \geq$ K 2kΩ	25	100	–	V/mV
Common-mode Rejection Ratio	CMRR		65	85	–	dB
Power Supply Voltage Rejection Ratio	SVRR		65	100	–	dB
Output Voltage	V_{OH}	R_L = 2kΩ	3.5	4.1	–	V
		R_L = 10kΩ	4.0	4.2	–	V
	V_{OL}	$I_{SINK} \leq$ 60μA	–	0.2	0.4	V
		$I_{SINK} \leq$ 2mA	–	0.8	1.5	V
Maximum Output Voltage	V_{OM}	$R_L \geq$ 10kΩ, V_{CC} = ±15V	±12	±14	–	V
		R_L = 2kΩ, V_{CC} = ±15V	±10	–	–	V
Output Current	I_{SOURCE}	V_{IN+} = 1V, V_{IN-} = 0V, V_{CC} = 15V	20	40	–	mA
	I_{SINK}	V_{IN+} = 0V, V_{IN-} = 1V, V_{CC} = 15V	10	20	–	mA
		V_{IN+} = 0V, V_{IN-} = 1V, V_O = 0.4V	60	150	–	μA
Channel Separation	CS	f = 1kHz	–	120	–	dB
Slew Rate	SR	R_L = 2kΩ	–	2	–	V/μs

NOTE: A direction of the input blas current flows from IC because first input transistor consists of PNP.

1

ELECTRICAL CHARACTERISTICS CURVES

Fig. 2 – POWER SUPPLY VOLTAGE vs. POWER SUPPLY CURRENT

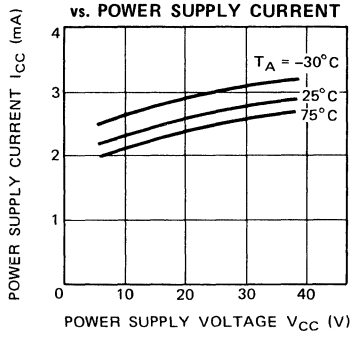


Fig. 3 – OUTPUT CURRENT vs. OUTPUT VOLTAGE

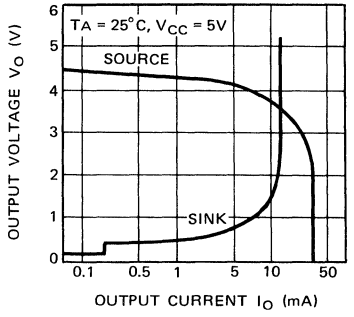


Fig. 4 – TEMPERATURE vs. INPUT BIAS CURRENT

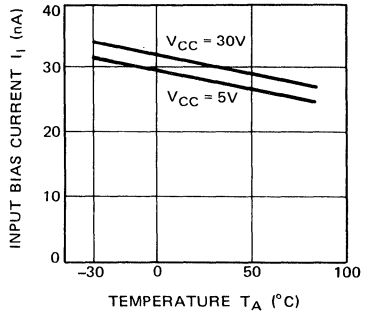


Fig. 5 – FREQUENCY vs. OUTPUT VOLTAGE

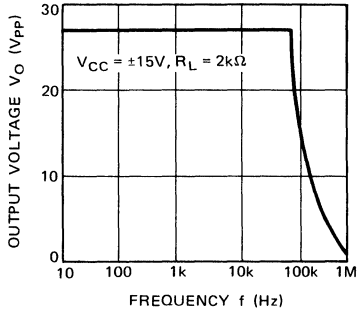
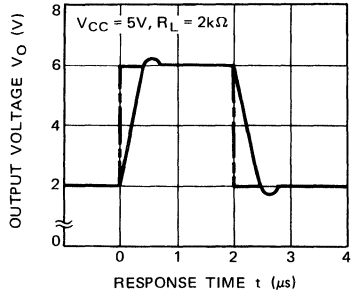


Fig. 6 – PULSE RESPONSE



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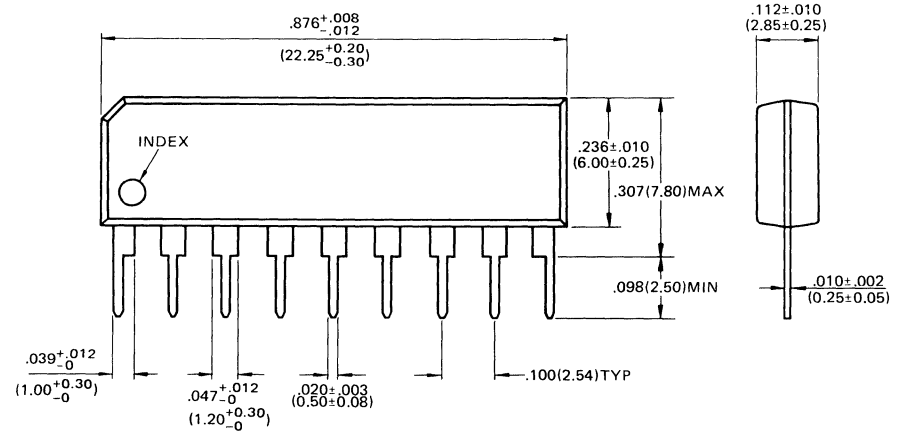
PACKAGE DIMENSIONS

9-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE No.: SIP-09P-M01)

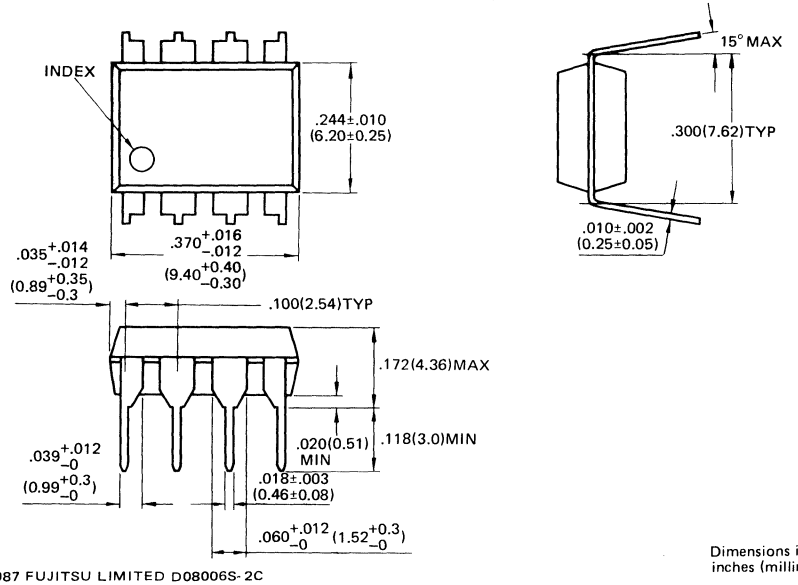


Dimensions in
inches (millimeters)

1

PACKAGE DIMENSIONS (continued)

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in
inches (millimeters)

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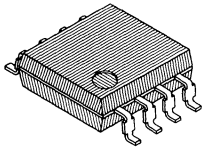
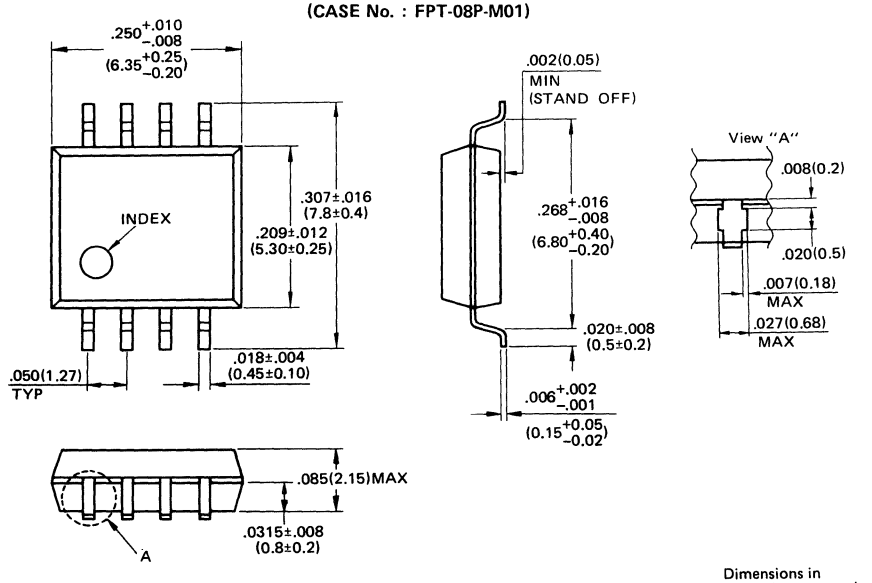


FPT-08P-M01

8-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-08P-M01)



Dimensions in
inches (millimeters)

FUJITSU

LOW NOISE DUAL OPERATIONAL AMPLIFIER

MB47833

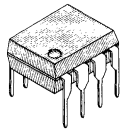
May 1988
Edition 1.0

LOW NOISE DUAL OPERATIONAL AMPLIFIER

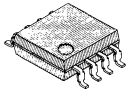
The Fujitsu MB47833 is a dual operational amplifier with a high slew rate, broad bandwidth and low noise characteristics.

The MB47833 is an excellent preamplifier for PCM and high-fidelity audio systems. The device is functionally compatible with the LM833.

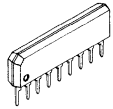
- Wide Power Supply Range: ±1.5V to ±15V
- High Slew Rate: 7 V/μs
- Low Input Noise Voltage: 4.5 nV/$\sqrt{Hz}$
- Wide Gain Bandwidth: 15 MHz
- Internal Phase Compensation



PLASTIC PACKAGE
DIP-08P-M01

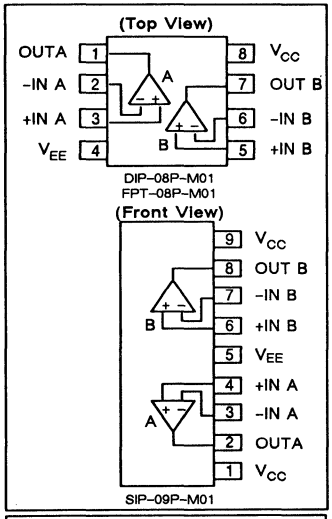


PLASTIC PACKAGE
FPT-08P-M01



PLASTIC PACKAGE
SIP-09P-M01

PIN ASSIGNMENTS



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

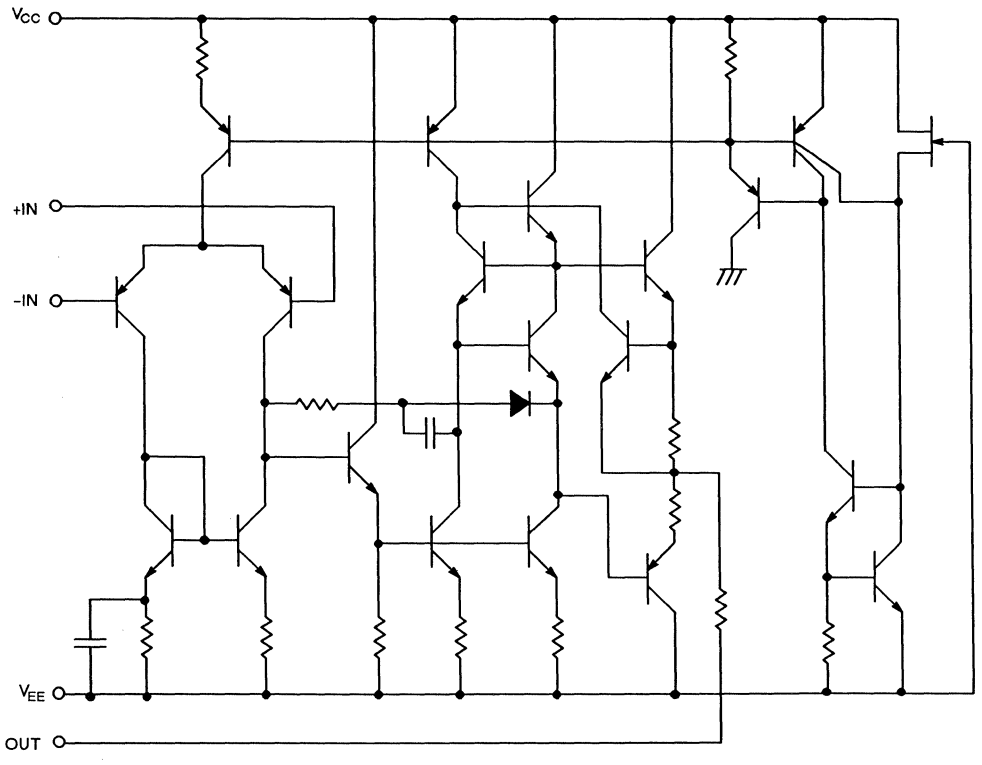
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+18	V
	V_{EE}	-18	V
Differential Input Voltage	V_{ID}	±30	V
Common Mode Input Voltage	V_I	±15	V
Power Dissipation	P_D	350 ($T_A \leq 55°C$)	mW
Operating Temperature	T_A	-30 to +85	°C
Storage Temperature	T_{STG}	-55 to +125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1

Fig. 1 — EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	±1.5 to ±15	V
	V_{EE}		
Ambient Operating Temperature	T_A	-30 to +85	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = +15V, V_{EE} = -15V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Value			Unit
			Minimum	Typical	Maximum	
Input Offset Voltage	V_{IO}			0.3	5.0	mV
Input Offset Current	I_{IO}			10	200	nA
Input Bias Current	I_{IN}			500	1000	nA
Common Mode Input Voltage	V_{CM}		±12	±14		V
Common Mode Rejection Ratio	CMR		80	100		dB
Supply Voltage Rejection Ratio	SVR		80	100		dB
Voltage Gain	A_V	R_L = 2kΩ	90	110		dB
Power Supply Current	I_{CC}			5.0	8.0	mA
Maximum Output Voltage	V_{OM}	$R_L \geq$ 10kΩ	±12	±13.5		V
		$R_L \geq$ 2kΩ	±10	±13.4		V
Gain Bandwidth Product	GBW	R_L = 2kΩ, f = 100kHz		15		MHz
Slew Rate	SR	R_L = 2kΩ, C = 100pF A_V = 1		7		V/μS
Channel Separation	CS	f = 1kHz		120		dB
Input Noise Voltage	V_{NI}	NAB, JISA RS = 600Ω, f = 1kHz		0.4		μV

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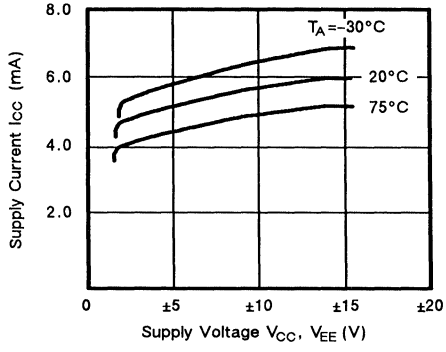
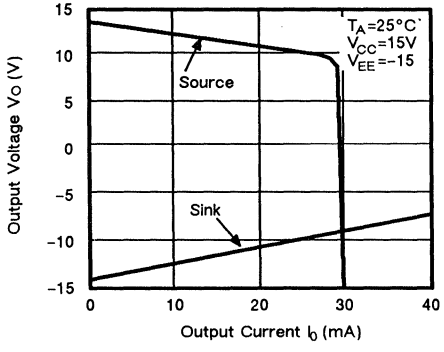
TYPICAL PERFORMANCE CHARACTERISTICS

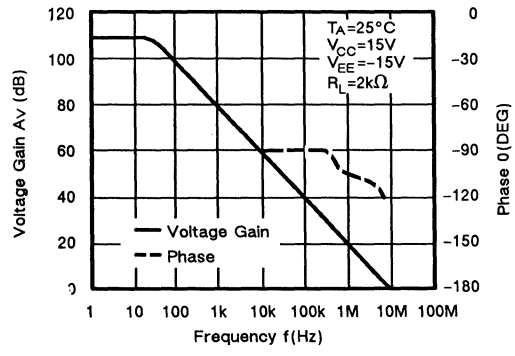
Supply Current vs Supply Voltage



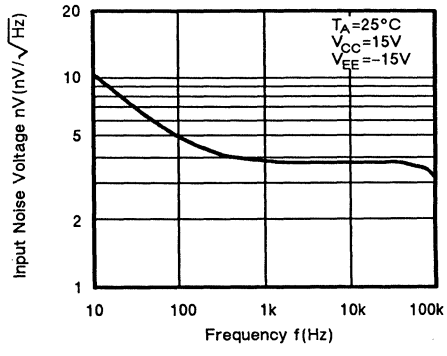
Output Voltage vs Output Current



Voltage Gain vs Frequency

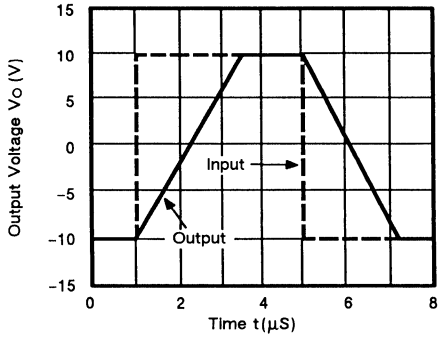


Input Noise Voltage vs Frequency

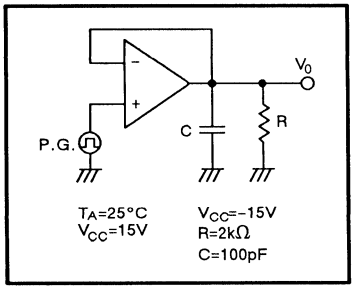


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Pulse Response Characteristics



Pulse Response vs Measurement Circuit



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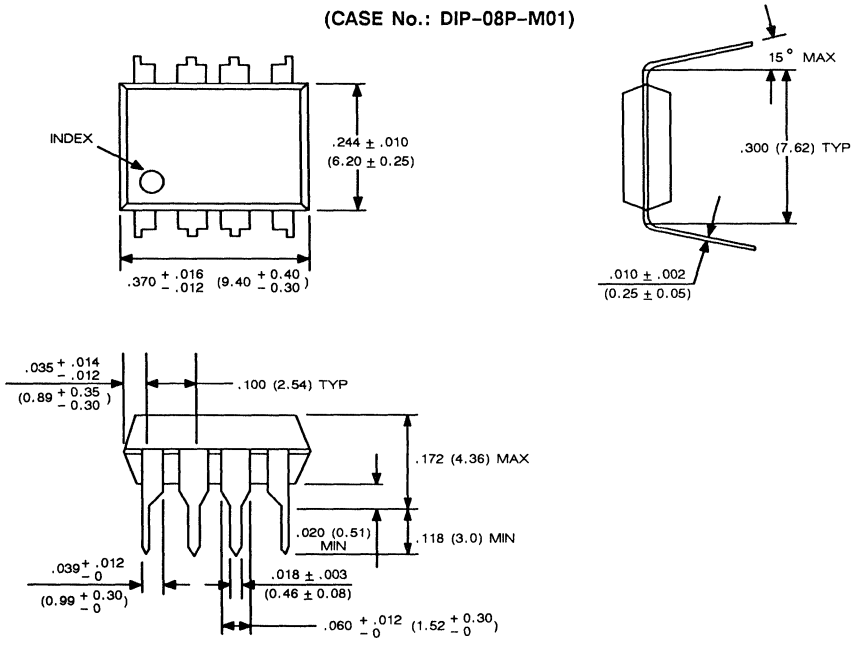
PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in
inches (millimeters)

D08006S-2C

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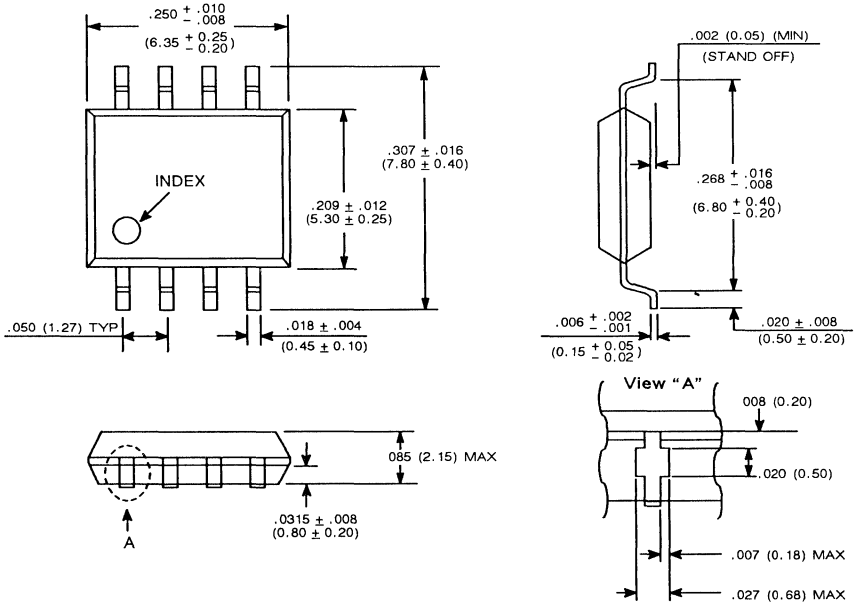
PACKAGE DIMENSIONS (continued)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



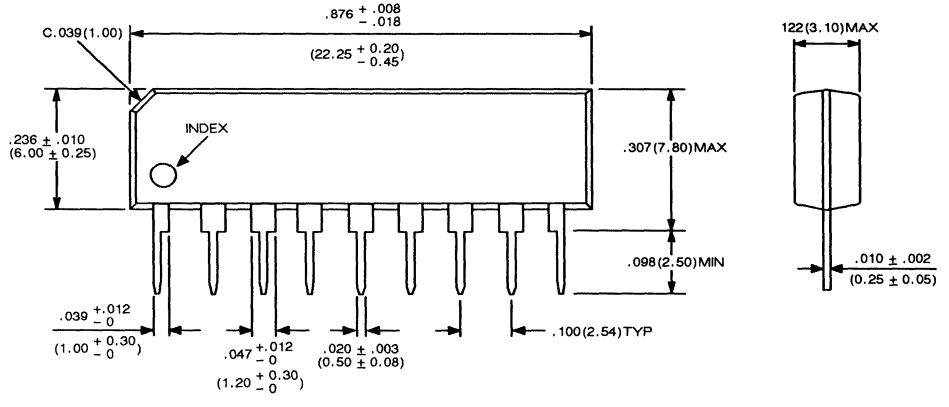
Dimensions in
inches (millimeters)

F08002S-2C

1

PACKAGE DIMENSIONS (continued)

9-LEAD PLASTIC SINGLE-IN-LINE PACKAGE
(CASE No.: SIP-09P-M01)



Dimensions in
inches (millimeters)

S09002S-2C

Section 2

2

Comparators — *At a Glance*

Page	Device	Description	Features	Power Supply (V)	Package Options
2–3	MB4001	Single	High Speed (t_{PD} = 50 ns) V_{RO} = 2 mV	+12 to –6	8-pin Plastic DIP, FPT
2–7	MB4002	Single	High Speed (t_{PD} = 25ns) V_{RO} = 1mV	+12 to –6	8-pin Plastic DIP, FPT
2–15	MB4204	Quad	Low Power (I_{CC} = 0.8mA)	+2 to +36	14-pin Plastic DIP, FPT
2–21	MB4205	Single	High Power I_{OL} = 0.5mA w/ Over Current Limit	+6.5 to +18	8-pin Plastic SIP
2–29	MB47393	Dual	Wide P/S Voltage Range	+2 to +36 ±1 to ±18	8-pin Plastic FPT 9-pin Plastic SIP

2

FUJITSU

HIGH SPEED COMPARATOR

MB4001

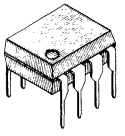
April 1989
Edition 1.0

2

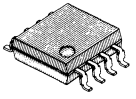
HIGH SPEED COMPARATOR

The Fujitsu MB4001 is a Monolithic High Speed Comparator. Its single-end output circuit is low impedance and input offset voltage is small, besides the device operation is stable against temperature variation. MB4001 is compatible with μA710.

- High Speed – 50 ns typ.
- Small Input offset voltage
- Low output impedance
- Package
  Plastic 8-pin Dual-In-Line (Suffix: -P)
  Plastic 8-pin FLAT Package (Suffix: -PF)



PLASTIC PACKAGE
DIP-08P-M01



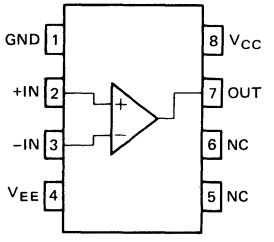
PLASTIC PACKAGE
FPT-08P-M01

ABSOLUTE MAXIMUM RATINGS (See NOTE) (T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+14	V
Power Supply Voltage	V_{EE}	−7	V
Input Voltage	V_I	±7	V
Storage Temperature	T_{STG}	−55 to +125	°C
Operating Temperature	T_A	−20 to +75	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

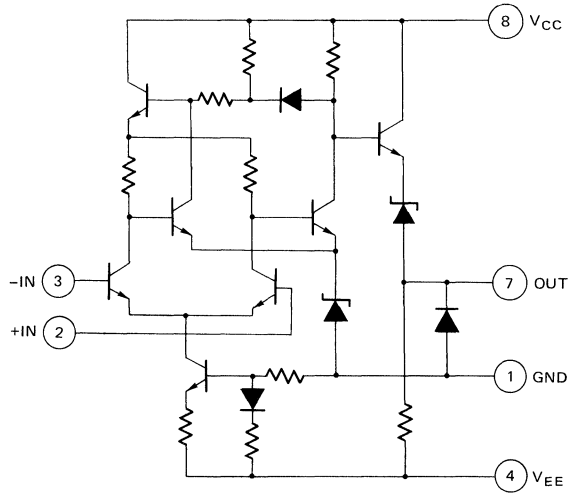
PIN ASSIGNMENT
(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 – MB4001 EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+12±5%	V
Power Supply Voltage	V_{EE}	-6±5%	V
Operating Temperature	T_A	-20 to +75	°C

ELECTRICAL CHARACTERISTICS

(T_A = 25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Offset Voltage	V_{IO}	$R_S \leq 200\Omega$, V_O = 1.4V		2	5	mV
Input Offset Current	I_{IO}	V_O = 1.4V		1		μA
Input Bias Current	I_I	V_O = 1.4V		10		μA
Voltage Gain	A_V	f = 1kHz, output pin is open	600	1500		
Propagation Delay Time	t_{pd}	V_I = 5mV, over drive		50		ns
High-level Output Voltage	V_{OH}	$\Delta V_I \geq$ 10mV, I_{IB} = 40μA	2.5	3.2		V
Low-level Output Voltage	V_{OL}	$\Delta V_I \geq$ 10mV, I_{OL} = 1.6μA		−0.5	0.37	V
Power Supply Current	I_{CC}	V_O = 1.4V		6		mA
Power Supply Current	I_{EE}	V_O = 1.4V		5		mA

TYPICAL CHARACTERISTICS CURVES

Fig. 2 – OUTPUT VOLTAGE vs. INPUT VOLTAGE

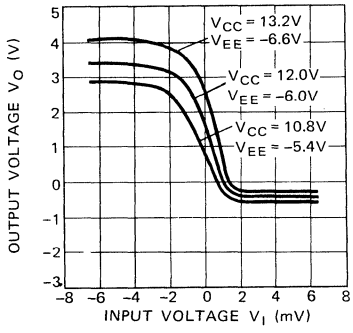


Fig. 3 – PULSE RESPONSE

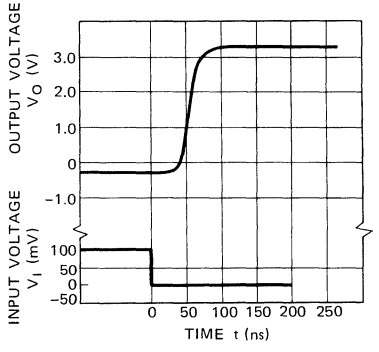
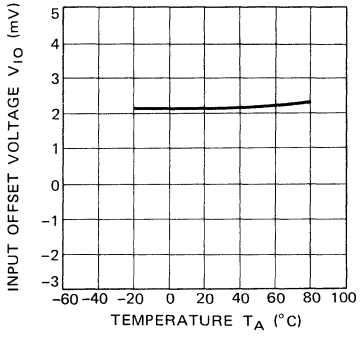


Fig. 4 – INPUT OFFSET VOLTAGE vs. TEMPERATURE

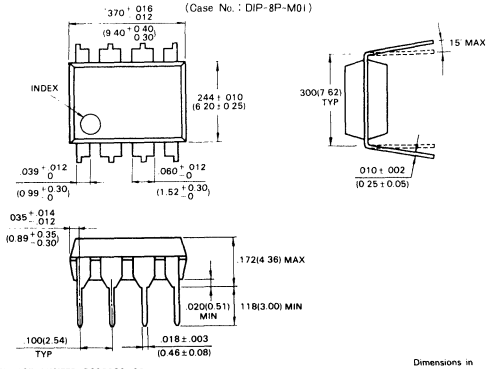


PACKAGE DIMENSIONS

2

8-LEAD PLASTIC DUAL IN-LINE PACKAGE

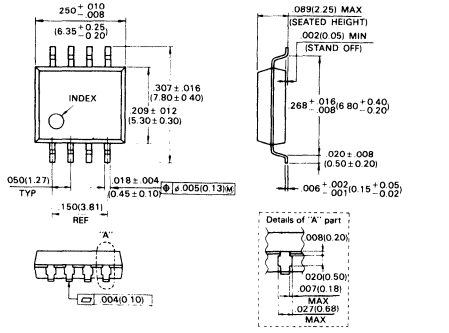
(Case No. : DIP-8P-M01)



Dimensions in inches (millimeters)

8-LEAD PLASTIC FLAT PACKAGE

(Case No. : FPT-8P-M01)



Dimensions in inches (millimeters)

FUJITSU

HIGH SPEED COMPARATOR

MB4002

April 1989
Edition 1.0

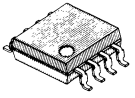
2

HIGH SPEED COMPARATOR

The Fujitsu MB4002 is a Unsaturated High Speed Comparator. Its output level is stable against power supply voltage and temperature variation.

- High Speed – 25 ns typ.
- Small Input Offset Voltage
- Package
  Plastic 8-pin DIP Package (Suffix: -P)
  Plastic 8-pin FLAT Package (Suffix: -PF)

PLASTIC PACKAGE
DIP-08P-M01



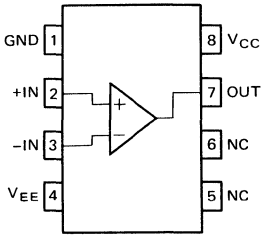
PLASTIC PACKAGE
FPT-08P-M01

ABSOLUTE MAXIMUM RATINGS (See NOTE) (T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+14	V
Power Supply Voltage	V_{EE}	-7	V
Input Voltage	V_I	±7	V
Storage Temperature	T_{STG}	-55 to +125	°C
Operating Temperature	T_A	-20 to +75	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

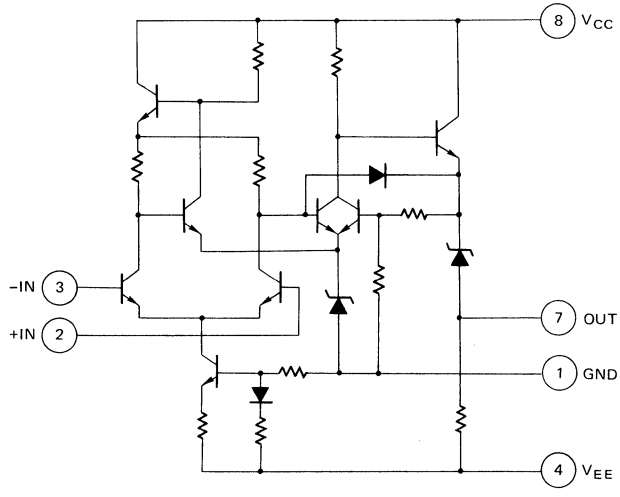
PIN ASSIGNMENT
(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 – MB4002 EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	+12±5%	V
Power Supply Voltage	V_{EE}	-6±5%	V
Operating Temperature	T_A	-20 to +75	°C

2

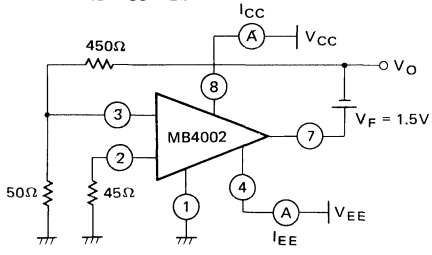
ELECTRICAL CHARACTERISTICS

(V_{CC} = 12V, V_{EE} = -6V, T_A = 25±2°C)

Parameter	Symbol	Condition	Test Circuit	Value			Unit
				Min	Typ	Max	
Input Offset Voltage	V_{IO}	$R_S \leq 200\Omega$, V_O = 1.5V	Fig. 2		1	5	mV
Input Offset Current	I_{IO}	V_O = 1.5V	Fig. 3		1	5	μA
Input Bias Current	I_I	V_O = 1.5V	Fig. 4		10	40	μA
Voltage Gain	A_V	f = 1kHz, output pin is open	Fig. 5	800	1500		
Propagation Delay Time	t_{pd}	V_I = 100mV, 5mV Over Drive	Fig. 7		25		ns
High-level Output Voltage	V_{OH}	$\Delta V_I \geq 10$mV, I_{OH} = 40μA	Fig. 6	2.8	3.2	3.6	V
Low-level Output Voltage	V_{OL}	$\Delta V_I \geq 10$mV, I_{OL} = 2.0mA	Fig. 6	-0.2	0	0.37	V
Power Supply Current	I_{CC}	V_O = 1.5V	Fig. 2		10.6	13.5	mA
Power Supply Current	I_{EE}	V_O = 1.5V	Fig. 2		6.8	8.5	mA

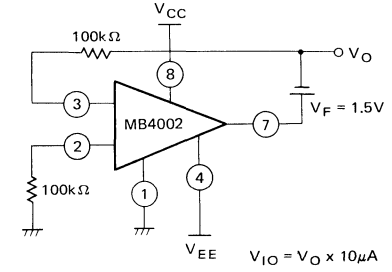
TEST CIRCUIT

Fig. 2 V_{IO}, I_{CC}, I_{EE}



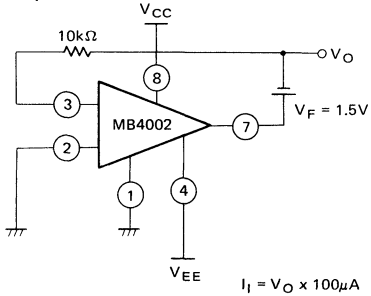
$V_{IO} = V_O \times 10^{-1}$mV

Fig. 3 I_{IO}



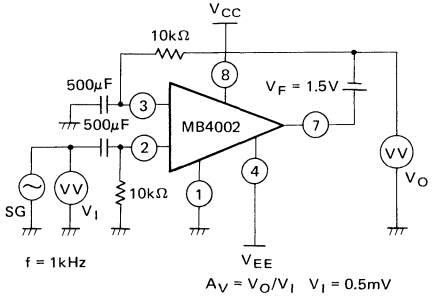
$V_{IO} = V_O \times 10\mu A$

Fig. 4 I_I



$I_I = V_O \times 100\mu A$

Fig. 5 A_V



$A_V = V_O/V_I$ V_I = 0.5mV

2

TEST CIRCUIT (continued)

Fig. 6 V_{OH}, V_{OL}

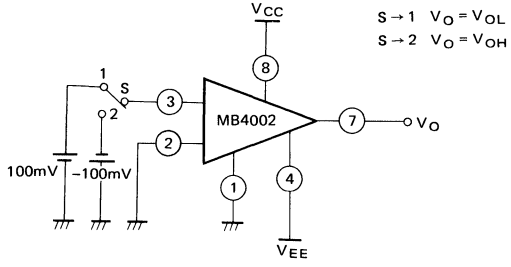
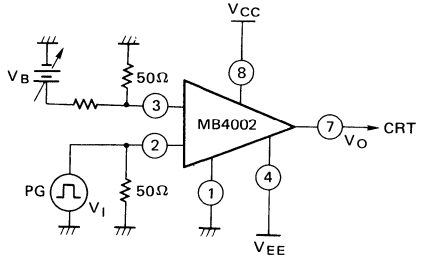
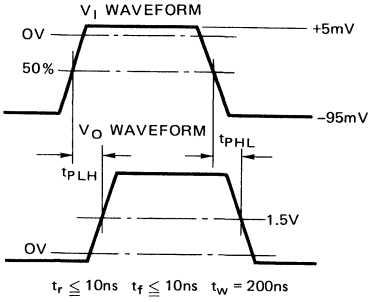


Fig. 7 t_{pd}





TYPICAL CHARACTERISTICS CURVES

Fig. 8 – INPUT PROPAGATION CHARACTERISTICS

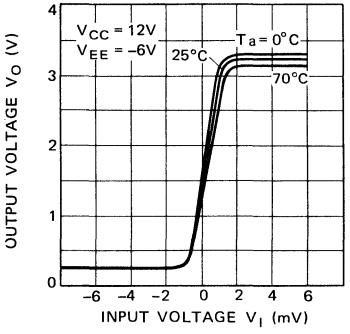
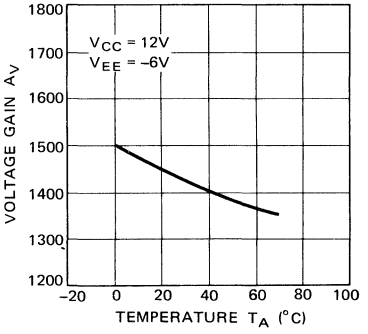


Fig. 9 – VOLTAGE GAIN vs. TEMPERATURE



TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 10 – INPUT BIAS CURRENT vs. TEMPERATURE

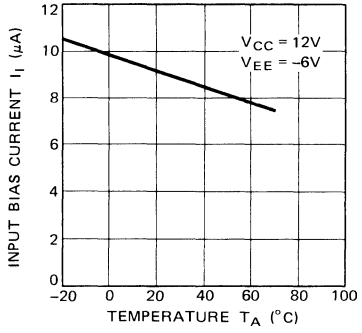


Fig. 11 – INPUT OFFSET CURRENT vs. TEMPERATURE

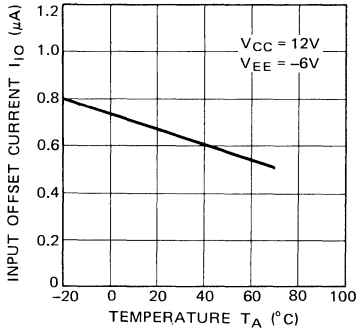


Fig. 12 – OUTPUT SINK CURRENT vs. TEMPERATURE

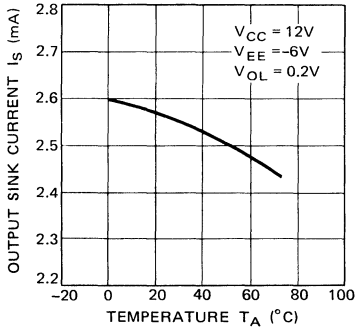
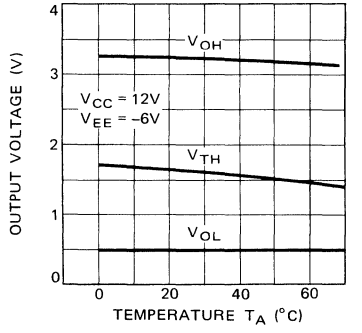


Fig. 13 – OUTPUT VOLTAGE vs. TEMPERATURE



TYPICAL CHARACTERISTICS CURVES (continued)

2

Fig. 14 – OUTPUT VOLTAGE vs. POWER SUPPLY VOLTAGE

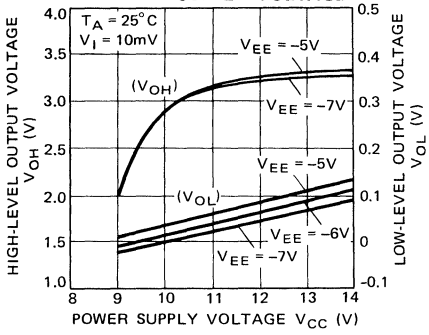


Fig. 15 – SWITCHING RESPONSE (1)

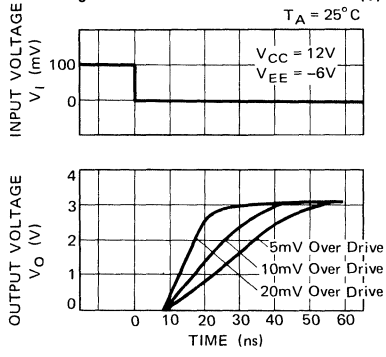


Fig. 16 – SWITCHING RESPONSE (2)

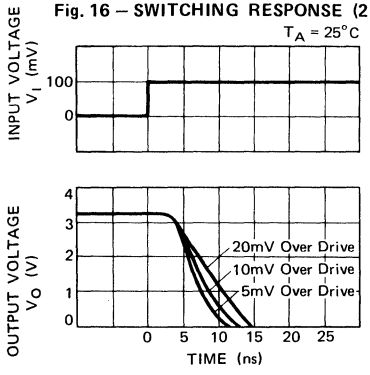
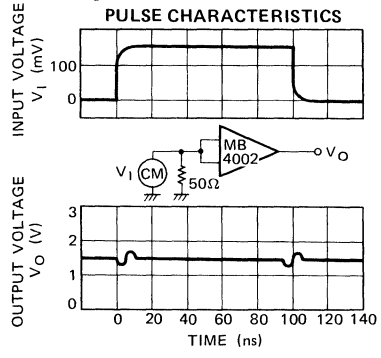


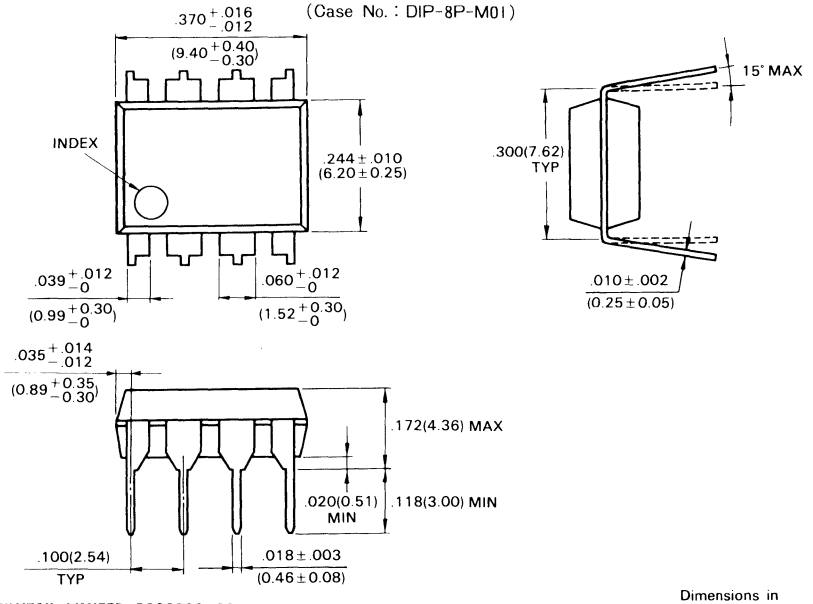
Fig. 17 – COMMON MODE INPUT PULSE CHARACTERISTICS



2

PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No. : DIP-8P-M01)



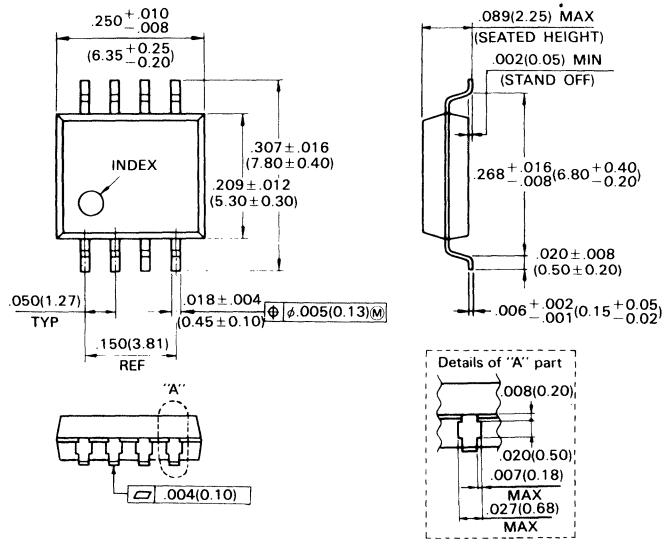
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (continued)

2

8-LEAD PLASTIC FLAT PACKAGE

(Case No. : FPT-8P-M01)



Dimensions in inches (millimeters)

May 1988
Edition 1.0

2

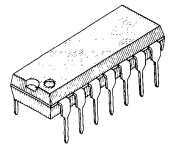
QUAD COMPARATOR

The Fujitsu MB4204 is a Quad Comparator which consists of four independent channels. The MB4204 is designed to operate form either a single power or dual power supplies over a wide range of voltages. The input characteristics is equivalent of current industry standard comparator. Even though operated from a single power supply, the MB4204 is suitably designed to compare multiple signals in parallel and to be operated with battery because its input common mode voltage range includes ground potential and it requires low power supply current.

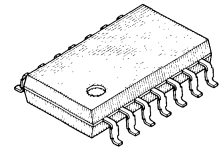
The MB4204 can be high density mounted because it integrates 4 circuits on a chip in DIP/FPT-14-pin package.

The MB4204 is pin compatible with National Semiconductor LM339.

- Wide power supply voltage range: +2 to +36V
- Wide input common mode range: 0 to (Vcc-1.5) V
- Low power supply current: 0.8 mA typ.
- Low input offset voltage: 2mV typ.
- Low input bias current: 25nA typ.
- Open Collectors Output allow to wired-OR Connection
- Package
  - — 14-pin Plastic DIP Package (Suffix: -P)
  - — 14-pin Plastic FPT Package (Suffix: -PF)

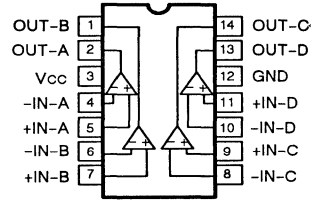


PLASTIC PACKAGE
DIP-14P-M02



PLASTIC PACKAGE
FPT-14P-M01

PIN ASSIGNMENT



(TOP VIEW)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

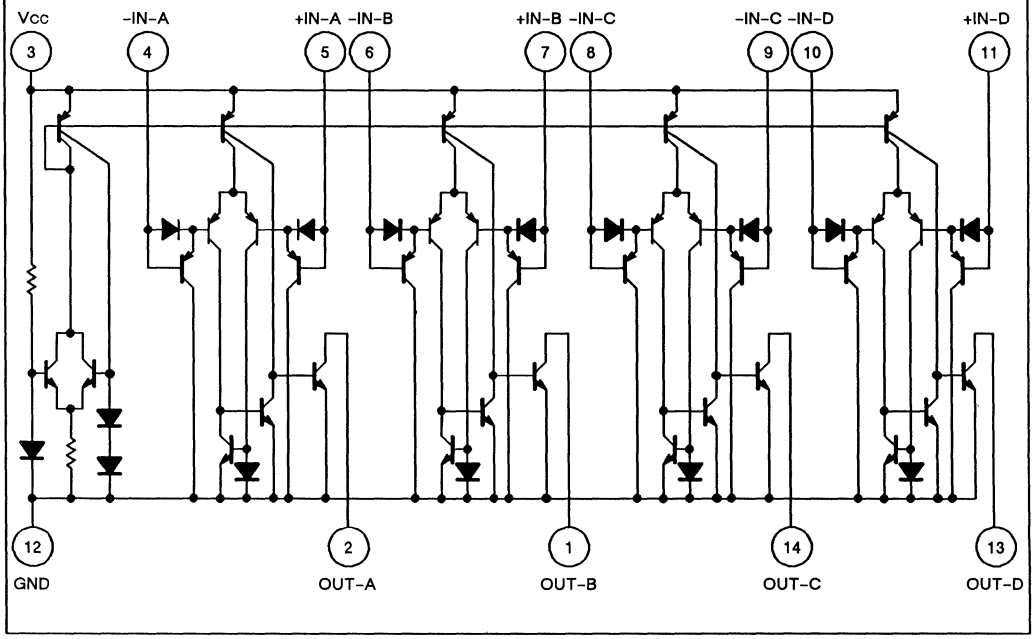
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	Vcc	36	V
Power Dissipation	PD	500	mW
Differential Input Voltage	VID	36	V
Common Mode Input Voltage	VI	-0.3 to +36	V
Output Short Circuit Duration		Infinite	
Operating Temperature	TA	-20 to +75	°C
Storage Temperature	TSTG	-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

Fig. 2 — EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (V_{CC}=+5V, T_A=25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_O = V_{REF} = 1.4V		2	5	mV
Input Offset Current	I_{IO}			5	50	nA
Input Bias Current	I_I *1			25	250	nA
Input Common Mode Voltage	V_{CM}		0		V_{CC} -1.5	V
Voltage Gain	A_V	R_L=15kΩ		200		V/mV
Transconductance				13		mhos
Large Signal Response Time	*2	R_L=5.1kΩ, V_{RL}=5V		300		ns
Response Time	*3	R_L=5.1kΩ, V_{RL}=5V		1.3		µs
Output Saturation Voltage	V_{OL}	V_{IN-}=1V, V_{IN+}= 0V, I_{SINK}=3 mA		250	400	mV
Output Sink Current	I_{SINK}	V_{IN-} =1V, V_{IN+}=0V, $V_O \leq 1.5V$	6	16		mA
Output Leakage Current	I_{LEAK}	V_{IN+}=1V, V_{IN-}=0V, V_O=5V		0.1		nA
Output Leakage Current	I_{LEAK}	V_{IN+}=1V, V_{IN-}=0V, V_O=30V			1	µA
Power Supply Current	I_{CC}	$R_L=\infty$		0.8	2	mA

Notes:

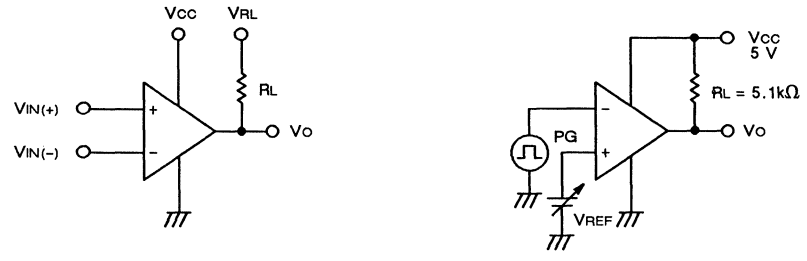
*1 The direction of the input bias current flows from IC.

*2 V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V

*3 V_{IN} = 100 mV, Overdrive = 5 mV

2

Fig. 3 — TEST CIRCUIT



TYPICAL CHARACTERISTICS CURVES

Fig. 4 - Power Supply Current vs. Power Supply Voltage

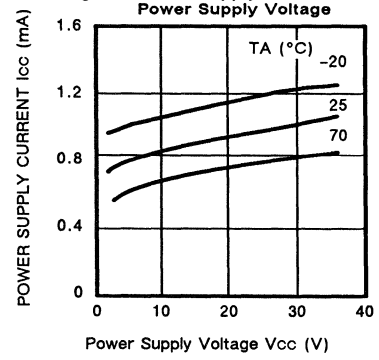


Fig. 5 - Output Saturation Voltage vs. Output Sink Current

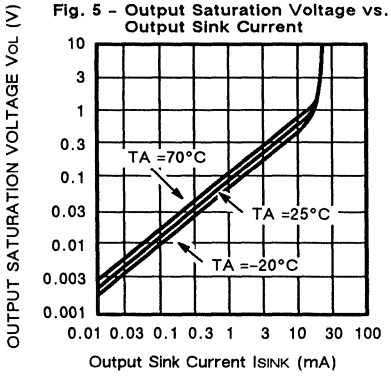


Fig. 6 - Input/Output Voltage vs. Time

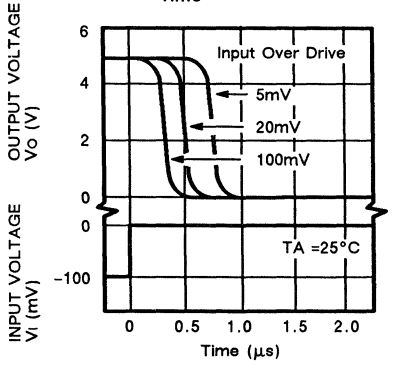
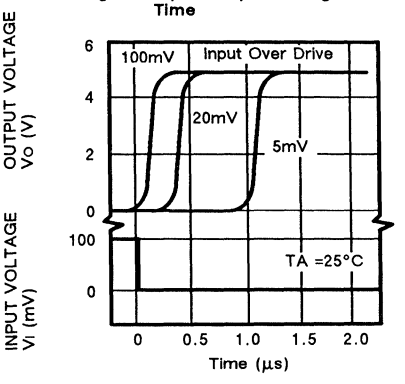


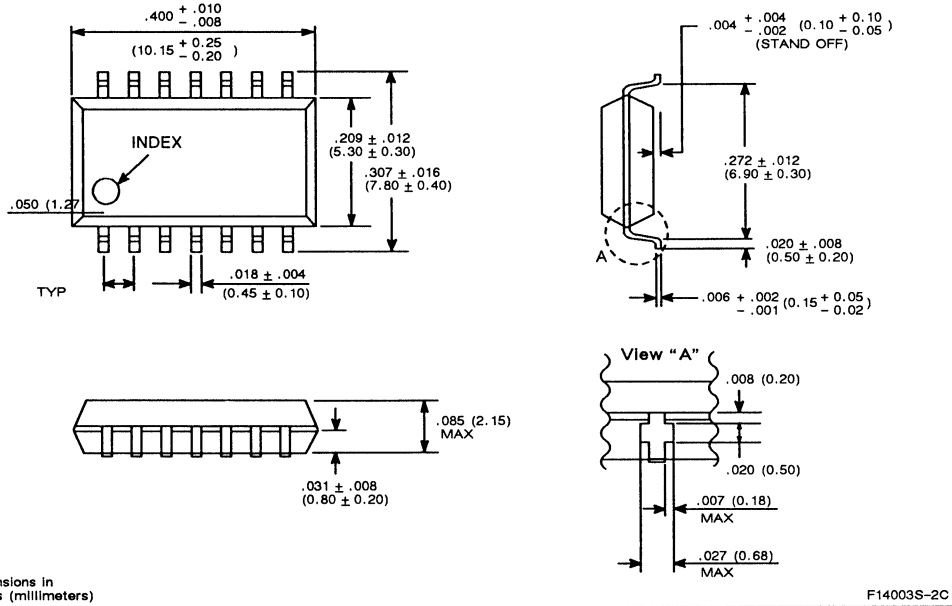
Fig. 7 - Input/Output Voltage vs. Time



2

PACKAGE DIMENSIONS

14-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-14P-M01)



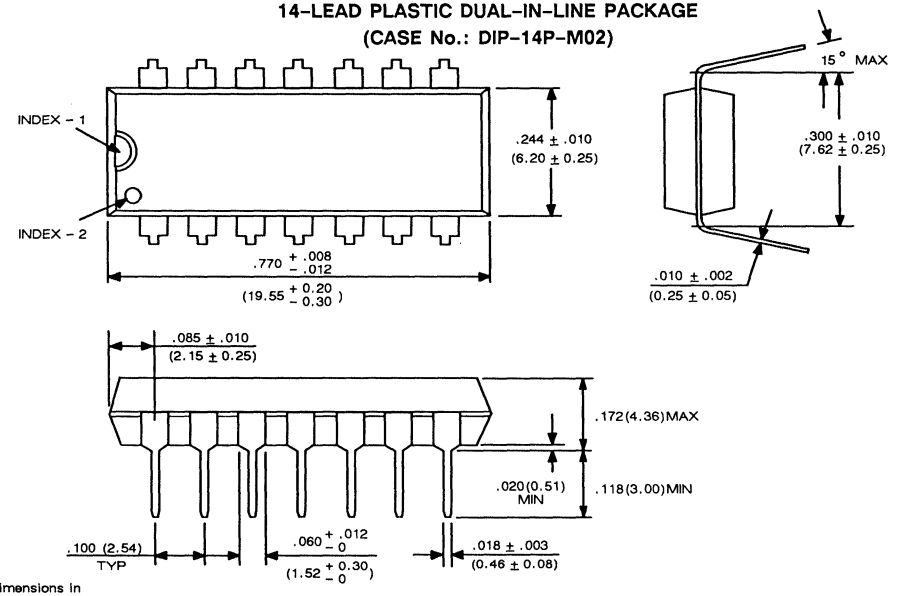
Dimensions in
inches (millimeters)

F14003S-2C

2

PACKAGE DIMENSIONS (Continued)

14-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-14P-M02)



Dimensions in
inches (millimeters)

D14010S-3C

HIGH POWER COMPARATOR

MB4205

March 1988
Edition 1.0

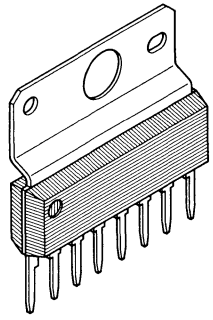
HIGH POWER COMPARATOR

The Fujitsu MB4205 is a comparator which is designed to operate from a single power supply voltage. It is capable of driving a load up to 0.5 A and have the current limiting circuitry, it enables a direct drive warning lamps.

As it is packaged in 8-pin plastic SIP package with heat sink, it enables easy mounting.

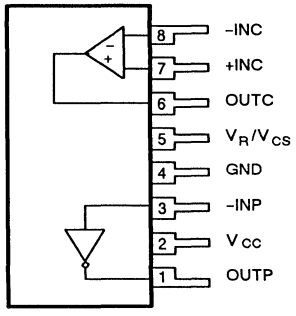
It is equipped with the function which turns the output "ON" by force, when the surge is inflicted in the application of automobile, and so on.

- PNP transistor input enables input control voltage from 0 V and a single power supply voltage operation
- High output drive capability : 0.5 A
- Resistance comparion is achieved due to on-chip switchable constant-current supply souce
  (Several hundred Ω to several kilo Ω)
- Hysteresis is set easily because V_{OH} level and V_R level is almost same
- On-chip current limiting circuitry
- Common pin for input control voltage pin V_{CS} and reference voltage output pin V_R



PLASTIC PACKAGE
SIP-08P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE) (T_A=25°C)

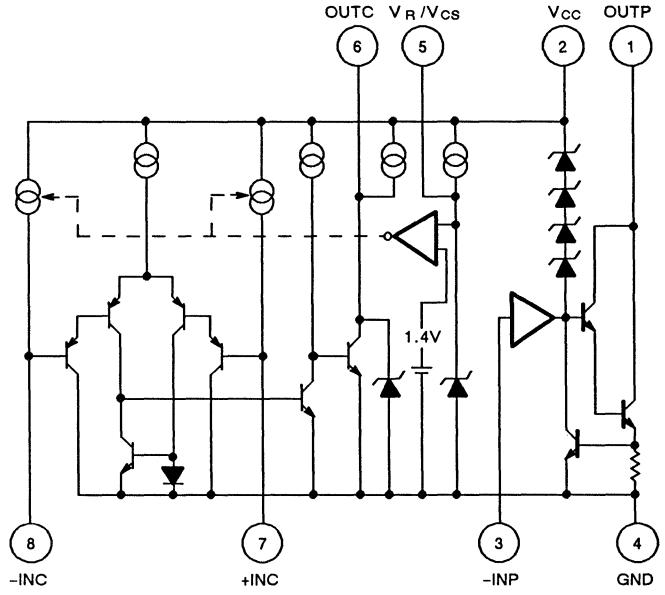
Rating	Symbol	Condition	Value	Unit
Power Supply Voltage	V_{CC}		18	V
Power Supply Current (Surge)	I_{CCS}	t≤50ms	100	mA
Load Current	I_{OL}		500	mA
Output Voltage	V_{OH}		40	V
Power Dissipation	P_D	T_A≤85°C	1	W
		T_C≤85°C	4	W
Operating Temperature	T_A		-30 to +85	°C
Storage Temperature	T_{STG}		-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

2

Fig. 1 — MB4205 EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (T_A=25°C, V_{CC}=13.2V, R_S=220Ω, R_L=54Ω)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power Supply Voltage	V_{CC}	R_S=0	6.5		18	V
Power Supply Current	I_{CC}	V_{CC}=10V, R_S=0		9	13	mA
Zener Voltage	V_{CCZ}	I_{CC}=50mA	26	30	36	V
Comparator section						
Input Offset Voltage	V_{IO}	V_{CS}=2.0V		2	10	mV
		V_{CS}=0.8V		5	20	mV
Input Bias Current *	I_I	V_{CS}=2.0V		0.5	3	μA
	I_{IB}	V_{CS}=0.8V	0.6	1.0	1.5	mA
Input Bias Current Ratio	I_{I+}/I_{I-}	V_{CS}=0.8V	0.95	1.0	1.05	
Common-mode Input Voltage Range	V_{CM}		0		V_{CC}-2	V
Output Voltage	V_{OL}	I_{SINK}=3mA		0.1	0.2	V
	V_{OH}	I_R=0.5mA	5.0	5.4	5.8	V
Sink Current	I_{SINK}	V_{OL}≤1V	8	20		mA
Output section						
Reference Voltage	V_R	R_L=100kΩ	5.0	5.4	5.8	V
Input Control Current	I_{CS}	V_{CS}=0.8V	0.5	1.0	1.8	mA
Input Bias Current	I_I	V_I=0		3	20	μA
		V_I=5.0V			1	μA
Output Voltage	V_{OL}	V_{IH}=2.0V, I_{OL}=0.2A		0.85	1.0	V
Output Current	I_{OH}	V_{IL}=0.8V, V_{IH}=40V		2	5	mA

Note: Input bias current flows from the IC.

2

ELECTRICAL CHARACTERISTICS CURVES

FIG. 2 — POWER SUPPLY CURRENT VS. POWER SUPPLY VOLTAGE

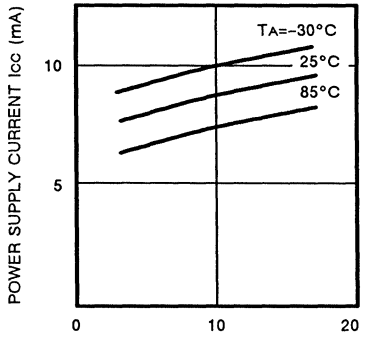


FIG. 3 — INPUT BIAS CURRENT VS. POWER SUPPLY VOLTAGE

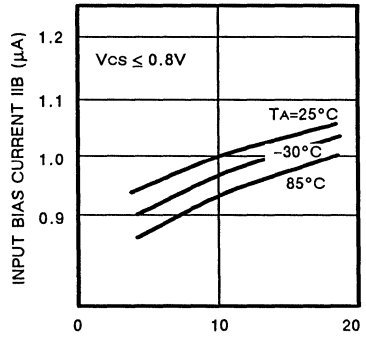


FIG. 4 — REFERENCE VOLTAGE/OUTPUT VOLTAGE VS.TEMPERATURE

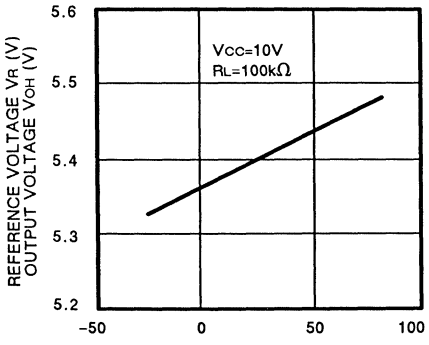
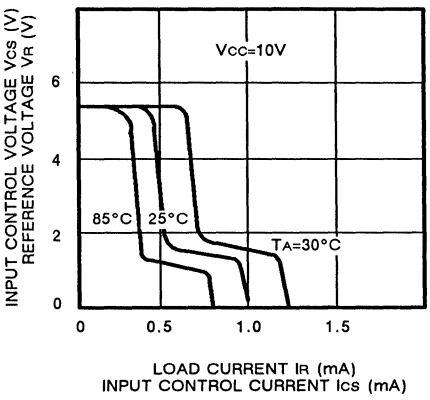


FIG. 5 — REFERENCE VOLTAGE VS. LOAD CURRENT INPUT CONTROL VOLTAGE VS. INPUT CONTROL CURRENT



ELECTRICAL CHARACTERISTICS CURVES (Continued)

FIG. 6 —OUTPUT VOLTAGE VS. INPUT VOLTAGE

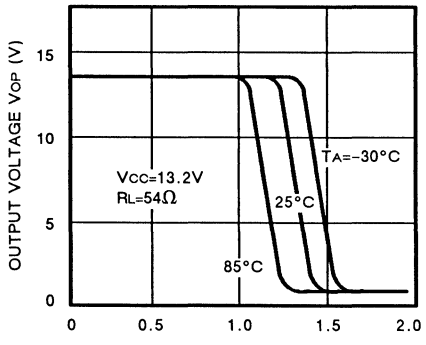
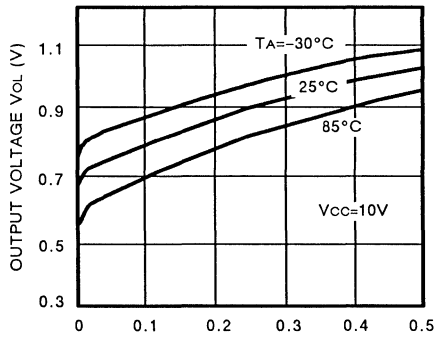
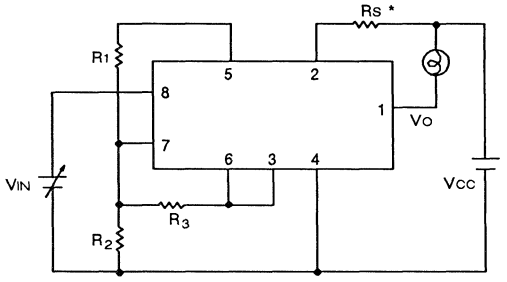


FIG. 7 —OUTPUT VOLTAGE VS. INPUT CURRENT

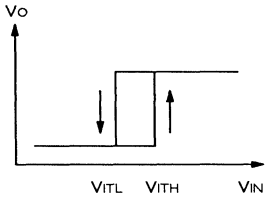


APPLICATION EXAMPLES

Fig. 8



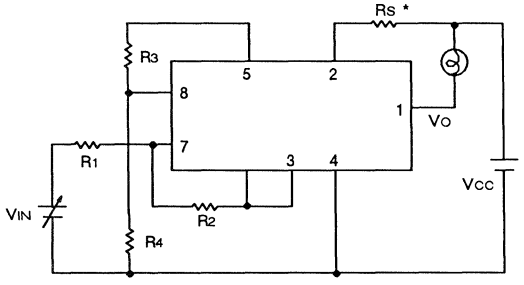
* Rs is not required if surge is not large.

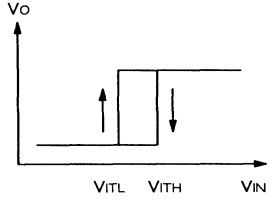


$$V_{ITH} \fallingdotseq \frac{R_2(R_1 + R_3)}{R_2(R_1 + R_3) + R_1R_3} V_R$$

$$V_{ITL} \fallingdotseq \frac{R_2R_3}{R_2(R_1 + R_3) + R_1R_3} V_R$$

Fig. 9

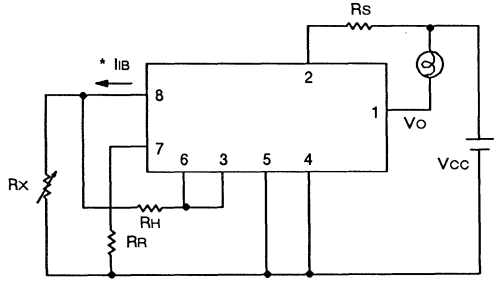




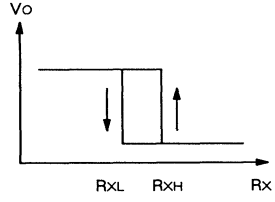
$$V_{ITH} = \left(1 + \frac{R_1}{R_2}\right)\left(\frac{R_4}{R_3 + R_4}\right)V_R$$

$$V_{ITL} = V_{ITH} - \frac{R_1}{R_2} V_R$$

Fig. 10



When 5 pin is connected to GND, constant current I_{IB} is generated internally.

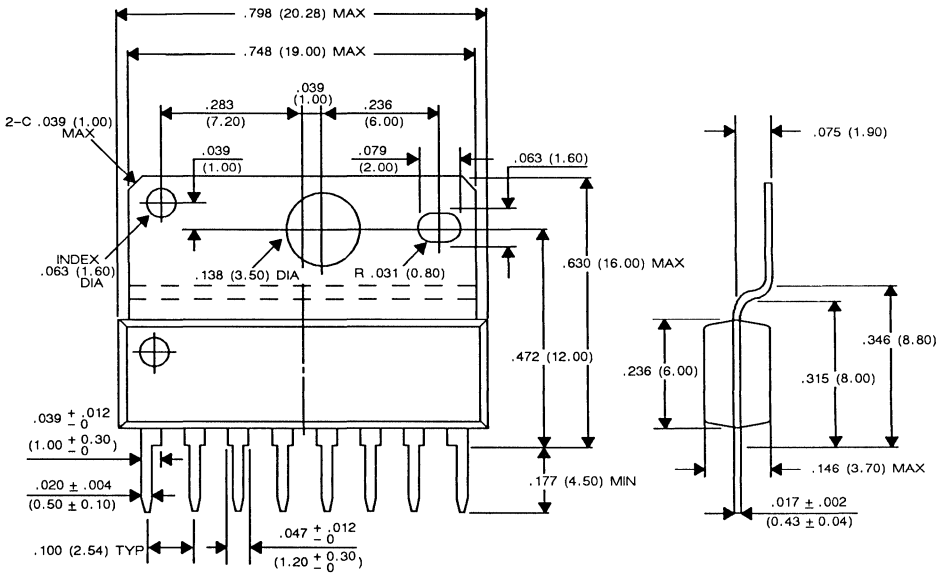


$$R_{XH} = \frac{R_R}{1 - \frac{R_R}{R_H}}$$

$$R_{XL} = \frac{R_R}{1 - \frac{R_R}{R_H} + \frac{V_R}{I_{IB}R_H}}$$

PACKAGE DIMENSIONS

8-LEAD PLASTIC SINGLE-IN-LINE PACKAGE
(CASE No.: SIP-08P-M01)



Dimensions in inches (millimeters)

S08004S-6C

DUAL COMPARATOR

MB47393

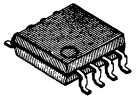
September 1988
Edition 1.0

DUAL COMPARATOR

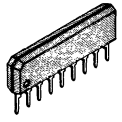
The Fujitsu MB47393 is a dual comparator which was designed to operate from a single power supply over a wide range of voltage. The input characteristics is equivalent of current industry standard comparator. Even though operated from a single power supply, the input common mode voltage range includes ground. Owing to adoption of clam-circuitry in input pins, mis-operation is prevented by negative input. The MB47393 is compatible with LM393.

- Wide power supply voltage range
  Single power supply ----- 2 V to 36 V
  Dual power supplies ----- ±1 V to ±18 V
- Wide input common-mode voltage range
  0 V to (Vcc - 1.5) V
- Low input bias current ----- 25 nA typ.
- High sink current capability because of open collector output
  40 mA min.
- Package
  Plastic 8 pin DIP package (Suffix: -P)
  Plastic 8 pin FPT package (Suffix: -PF)
  Plastic 9 pin SIP package (Suffix: -PS)

DIP-08P-M01



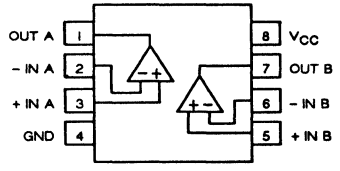
FPT-08P-M01



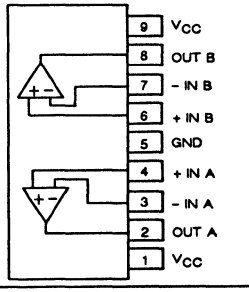
SIP-09P-M01

PIN ASSIGNMENT

(TOP VIEW)



(FRONT VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE) TA=25°C

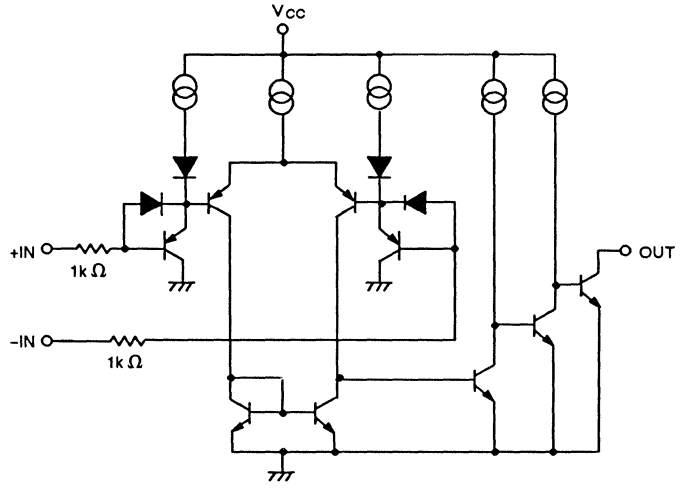
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	36	V
Differential Input Voltage	V_{ID}	36	V
Common-Mode Input Voltage	V_I	-5 to +36	V
Output Short Current to GND		Infinite *	
Power Dissipation	P_D	350 (TA≤55 °C)	mW
Operating Temperature	T_A	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +125	°C

* This value is specified with respect to the short circuit from output to GND. However, short circuit from the output to Vcc cause device destruction.

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

Fig. 1 — MB47393 EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	Vcc	2 to 30	V
		±1.0 to ±15	
Operating Temperature	TA	-20 to +75	°C
Output Sink Current	ISINK	≤ 40	mA

ELECTRICAL CHARACTERISTICS

(T_A=25°C, V_{CC}=5V)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Offset Voltage	V_{IO}	V_O=V_{REF}=1.4V		2	5	mV
Input Offset Current	I_{IO}			5	50	nA
Input Bias Current	I_I			25	250	nA
Common-Mode Input Voltage	V_{CM}		0		V_{CC}-1.5	V
Power Supply Current	I_{CC}	R_L=∞		2	3	mA
Voltage Gain	A_V	R_L=15kΩ, V_{CC}=15V		200		V/mV
Response Time		R_L=1kΩ		2		µs
Output Sink Current	I_{SINK}	V_{IN+}=0, V_{IN-}=1V, V_{OL}≤1.5V	40			mA
Output Saturation Voltage	V_{OL}	V_{IN+}=0, V_{IN-}=1V, I_{SINK}=30mA		0.2	0.4	V
Output Leakage Current	I_{LEAK}	V_{IN+}=1V, V_{IN-}=0V, V_O=30V			1	µA

Notes:

* I_I is measured when V_I≥0 and direction of the input current flows from IC. When negative voltage is applied to input pin, the pin is equivalently connected the GND through a 1kΩ of resistor.
When low voltage below than -5V is applied, please connect a resistor serially to input pin in order to prevent the high current flow.

* Positive input voltage may exceed the power supply voltage. As long as the other voltage remains in the common-mode input voltage range, the comparator will provide a proper output state.
When V_{CC}=5V, your are requested to use V_{IN} below 25 V.

TYPICAL CHARACTERISTIC CURVES

Fig. 2 — POWER SUPPLY CURRENT vs POWER SUPPLY VOLTAGE

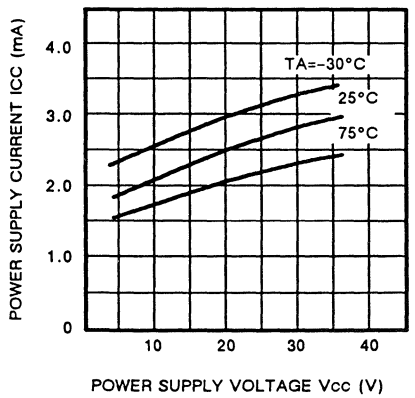
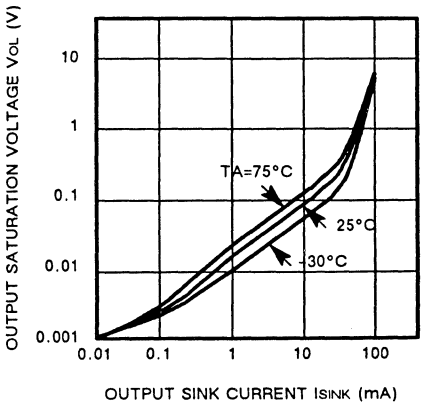


Fig. 3 — OUTPUT SATURATION VOLTAGE vs OUTPUT SINK CURRENT



TYPICAL CHARACTERISTIC CURVES (Continued)

2

Fig. 4 — INPUT CURRENT vs INPUT VOLTAGE

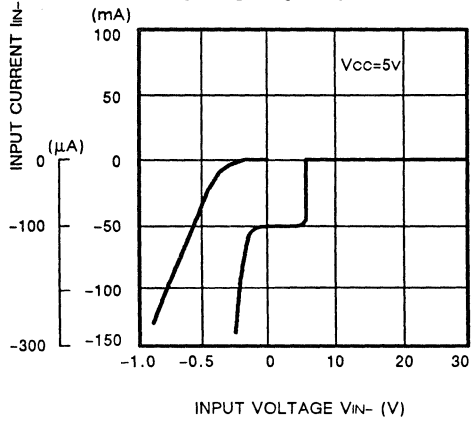


Fig. 5 — INPUT VOLTAGE/OUTPUT VOLTAGE vs RESPONSE TIME

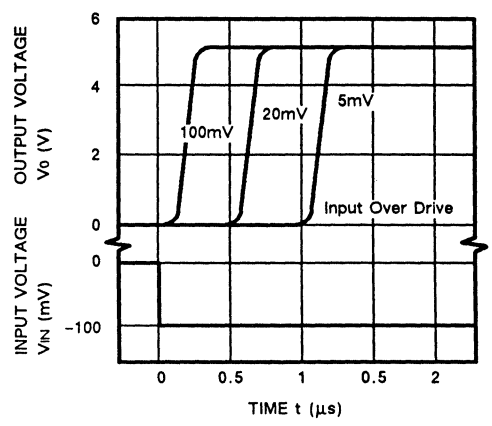


Fig. 6 — INPUT VOLTAGE/OUTPUT VOLTAGE vs RESPONSE TIME

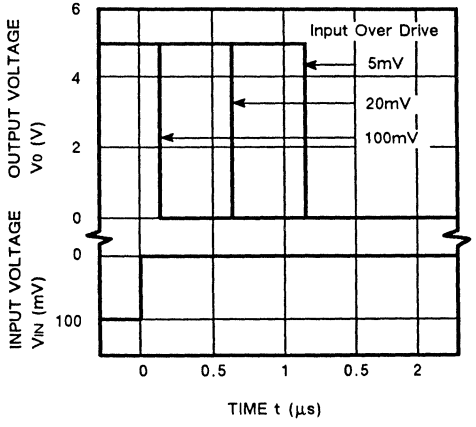
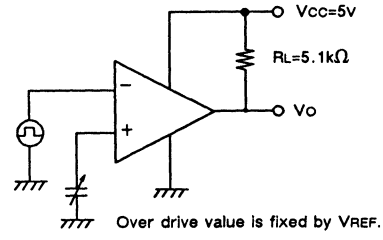


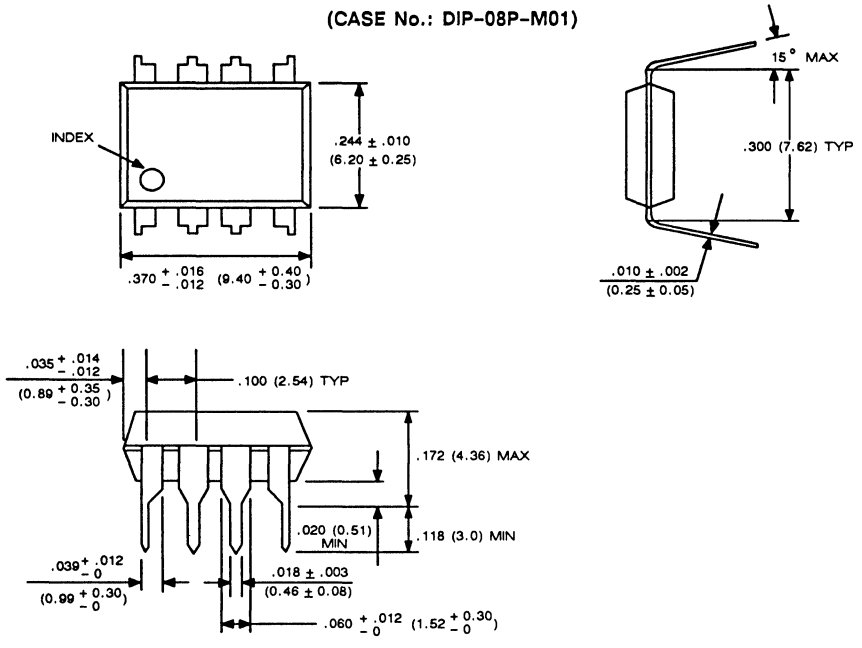
Fig. 7 — TEST CIRCUIT



2

PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



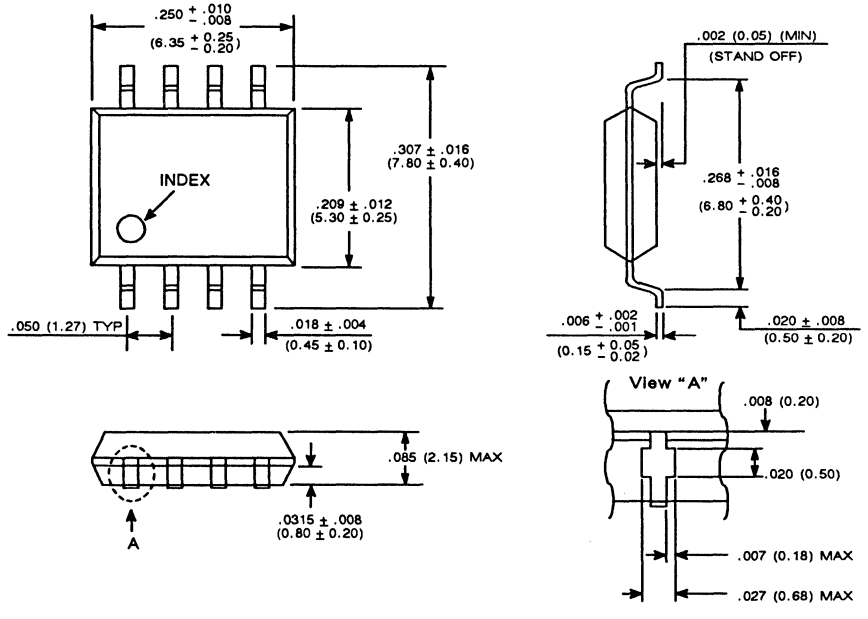
Dimensions in
inches (millimeters)

D08006S-2C

2

PACKAGE DIMENSIONS (Continued)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)

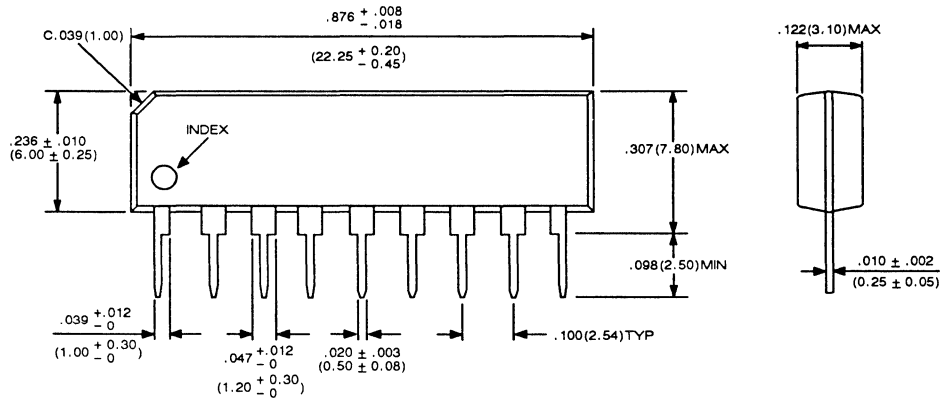


Dimensions in
inches (millimeters)

F08002S-2C

PACKAGE DIMENSIONS (Continued)

9-LEAD PLASTIC SINGLE-IN-LINE PACKAGE
(CASE No.: SIP-09P-M01)



Dimensions in
inches (millimeters)

S09002S-2C

2

Automotive Audio — *At a Glance*

Page	Device	Description	Features	Power Supply (V)	Package Options
3–3	MB3106	Dual Pre-amplifier	Low Distortion (0.05%). V_{ND} = 120 µV	+6 to +16	8-pin Plastic SIP
3–11	MB3110A	Dual Control Amplifier	Volume and Balance control, 20dB Voltage Gain	+6 to +16	8-pin Plastic SIP
3–17	MB3111	Distortion Limiting IC	.01% THD Low Noise 5 µV	+8 to +16	17-pin Plastic ZIP
3–25	MB3714A	6 W Power Amplifier	PO = 6 W/4Ω, 10 W/2Ω Audio Mute Full Protection Circuits	+8 to +16	8-pin Plastic SIP (with Heatsink)
3–31	MB3120	Compandor IC	Compression/ Expansion Mute, Low THD	+3.2 to +10	16-pin Plastic FPT 17-pin Plastic ZIP
3–43	MB3722	Dual Power Amplifier	Audio Mute Full Protection PO = 14 W/4Ω	+8 to +16	12-pin Plastic SIP (with Heatsink)
3–49	MB3730A	Balanced Transformerless (BTL) Amplifier	Audio Mute Full Protection PO = 18 W/4Ω	+8 to +16	7-pin Plastic SIP (with Heatsink)
3–55	MB3731	Balanced Transformerless (BTL) Amplifier	Audio Mute Full Protection PO = 14 W/4Ω	+8 to +16	12-pin Plastic SIP (with Heatsink)
3–61	MB3732/ MB3734	Balanced Transformerless (BTL) Amplifier	Audio Mute Full Protection PO = 20 W/4Ω	+8 to +16	7-pin Plastic SIP 9-pin Plastic SIP
3–69	MB3733	Balanced Transformerless (BTL) Amplifier	Audio Mute Full Protection	+8 to +16	12-pin Plastic SIP

Automotive Audio — *At a Glance (Continued)*

Page	Device	Description	Features	Power Supply (V)	Package Options
3–75	MB3735	Balanced Transformerless (BTL) Amplifier	DC Mute Full Protection PO = 15 W/4Ω	+8 to +16	9-pin Plastic SIP (with heatsink)
3–81	MB3736	Balanced Transformerless (BTL) Amplfier	DC Mute Full Protection PO = 15 W/4Ω	+8 to +16	9-pin Plastic SIP (with heatsink)
3–89	MB3737A	Balanced Transformerless (BTL) Amplifier with V_{CC} Standby	DC Mute Full Protection PO = 23 W/4Ω	+8 to +16	12-pin Plastic SIP, ZIP (with heatsink)
3–97	MB3742	Dual BTL Amplifier	Standby Mode Protection PO = 15 W x 2/Ω	+9 to +16	17-pin Plastic ZIP
3–105	MB3764	9-Level Detector and Driver for Level Meter	Internal Reference I_O = 20 mA maximum	+3.2 to +16	16-pin Plastic DIP
3–115	MB4104/ MB4105	FM Stereo Multiplex	Low Distortion .06% @ 300 mil	+8 to +16	16-pin Plastic DIP
3–125	MB87032	2-channel Elec. Volume Controller	For Stereo, TV, Video 1 dB Steps	+6 to +10	16-pin Plastic DIP

FUJITSU

DUAL LOW NOISE PRE-AMPLIFIER

MB3106

October 1987
Edition 1.0

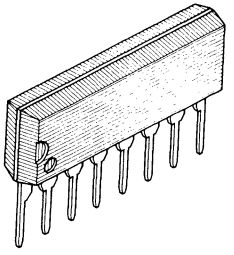
DUAL LOW NOISE PRE-AMPLIFIER

The Fujitsu MB3106 is a dual low noise pre-amplifier housed in a single in-line package for high density mounting on printed circuit boards for automotive audio stereo systems.

The MB3106 has a power supply stabilization circuit for low power supply voltage, and is designed to improve power efficiency at the output stage. Therefore, the MB3106 provides a wide output range, and can stably operate in a wide power supply voltage range and in a wide temperature range.

The MB3106 provides high gain in a low frequency range, because the feedback resistor operates in a wide tolerance condition.

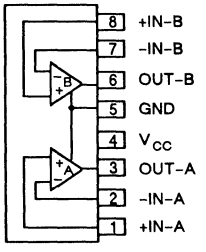
- High open loop gain : 90 dB typical
- Input noise voltage : 1 μV typical
- Protection circuit against over voltage at input stage
- On-chip power supply stabilizer
- Wide power supply range and high ripple rejection
- Package : 8-pin plastic SIP package
- Minimized number of external parts, due to on-chip bias circuit.



PLASTIC PACKAGE
SIP-08P-M03

PIN ASSIGNMENT

(Front View)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

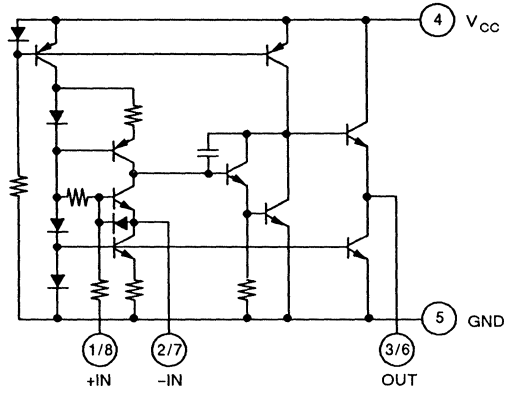
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	18	V
Power Dissipation	P_D	200 ($T_A \leq 75$ °C)	mW
Operating Temperature	T_A	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

Fig. 1 — EQUIVALENT CIRCUIT (ONE CHANNEL)



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	6 to 16	V
Temperature	T_A	-20 to +75	°C

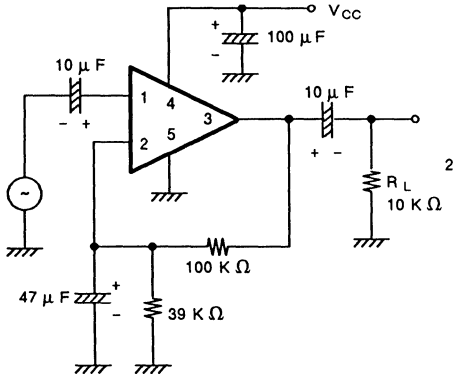
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 6V, f = 1kHz, R_L = 10kΩ)

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Power Supply Current	I_{CC}	—	—	3	4	mA
Open Loop Voltage Gain	A_{VO}	V_O = 0.8 V	75	90	—	dB
Closed Loop Voltage Gain	A_V	V_O = 0.8 V, NAB	—	42	—	dB
Maximum Output Voltage	V_{OM}	THD = 1%, NAB	1.0	1.6	—	V
Total Harmonic Distortion	THD	V_O = 0.8 V, NAB	—	0.05	0.3	%
Ouput Noise Voltage	V_{NO}	Rg = 2.2K Ω , NAB	—	120	200	μ V
Input Resistance	R_{IN}	NAB	50	150	—	kΩ
Channel Separation	—	V_O = 0.8 V, f = 10 KHz, NAB	—	65	—	dB
Ripple Rejection Ratio	—	f = 100 Hz, Rg = 2.2 KΩ, NAB	—	45	—	dB

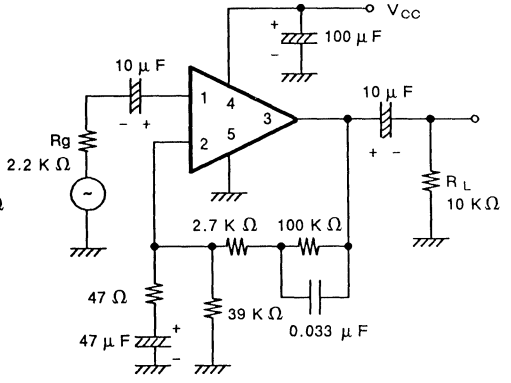
3

Fig. 2 — MEASUREMENT CIRCUITS
(Only one channel is illustrated)

1. I_{CC}, A_{VO}



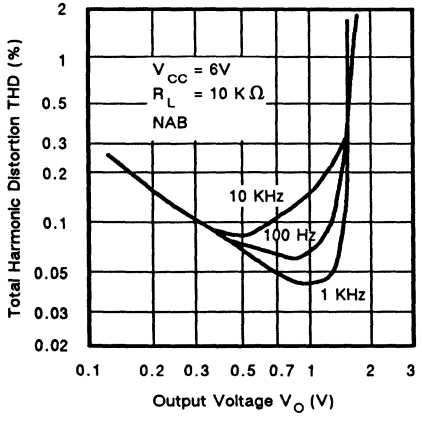
2. A_V, V_{OM}, THD, V_{NO}, R_{IN}



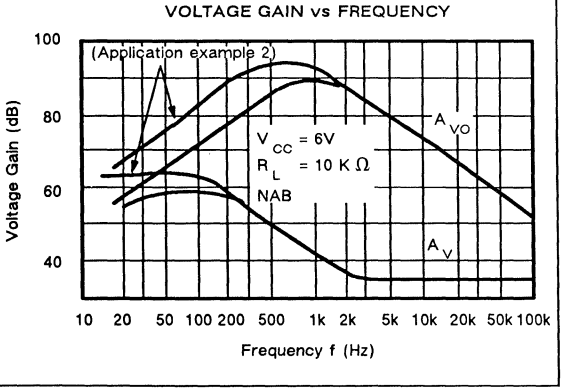
Note: V_{NO} is measured with the Bandpass filter of 30Hz to 30KHz.

TYPICAL PERFORMANCE CHARACTERISTICS

TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGE



VOLTAGE GAIN vs FREQUENCY



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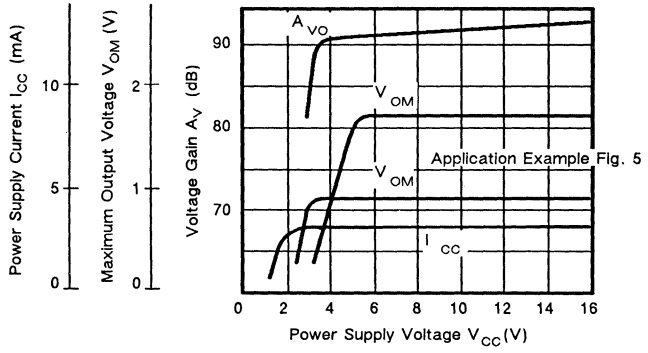
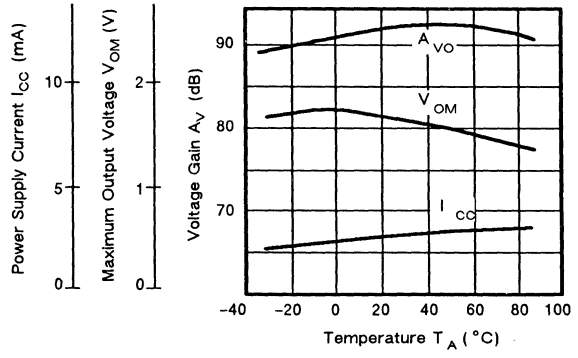
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

POWER SUPPLY CURRENT, MAXIMUM OUTPUT VOLTAGE, VOLTAGE GAIN vs POWER SUPPLY VOLTAGE

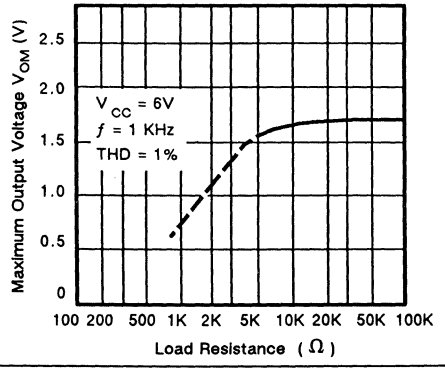


Application Example Fig. 5

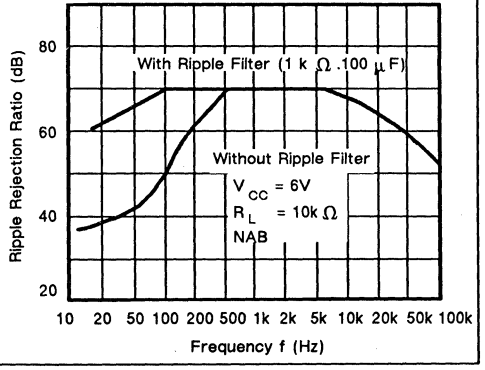
POWER SUPPLY CURRENT, MAXIMUM OUTPUT VOLTAGE, VOLTAGE GAIN vs TEMPERATURE



MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE

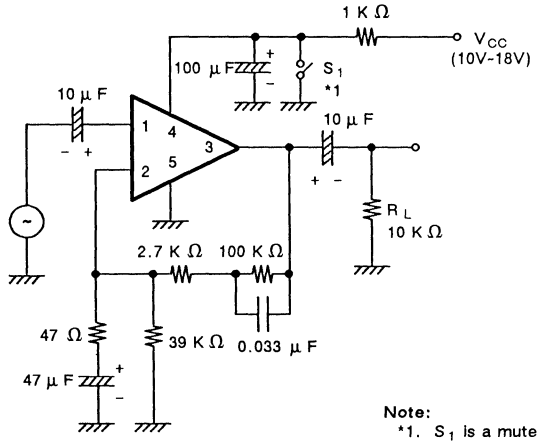


RIPPLE REJECTION RATIO vs FREQUENCY



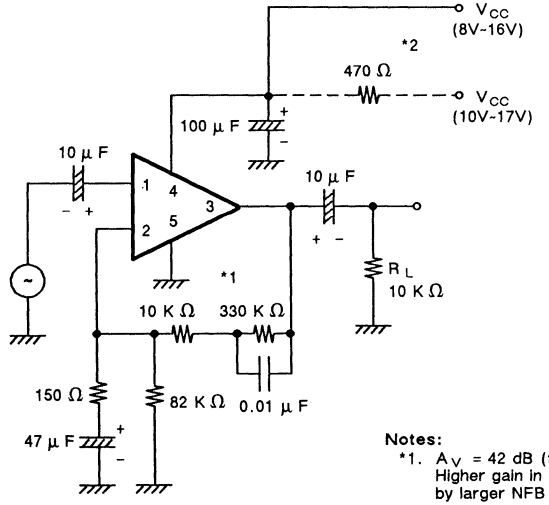
3

Fig. 3 — TYPICAL APPLICATION CIRCUIT
(Only one channel is illustrated)



Note:
*1. S_1 is a mute switch for the output.

Fig. 4 — HIGH GAIN CIRCUIT
(Only one channel is illustrated)



Notes:
*1. A_V = 42 dB (f = 1 KHz)
Higher gain in low band is obtained by larger NFB constant.

*2. To improve ripple rejection ratio.
(Improved as much as 20 dB at 100 Hz.

3

Fig. 5 — FOR LOW VOLTAGE POWER SUPPLY
(Only one channel is illustrated)

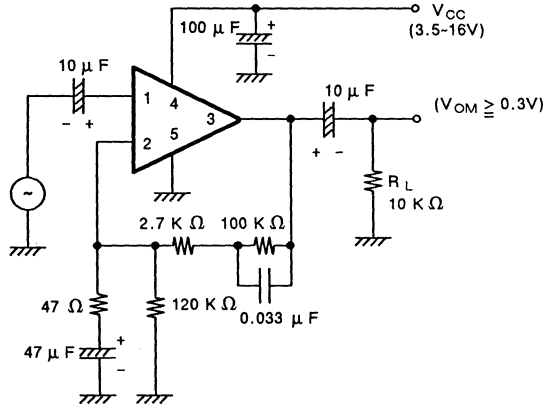
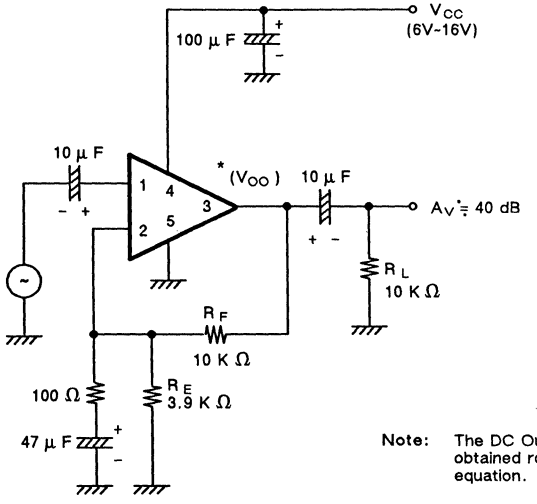


Fig. 6 — FLAT AMPLIFIER CIRCUIT
(Only one channel is illustrated)

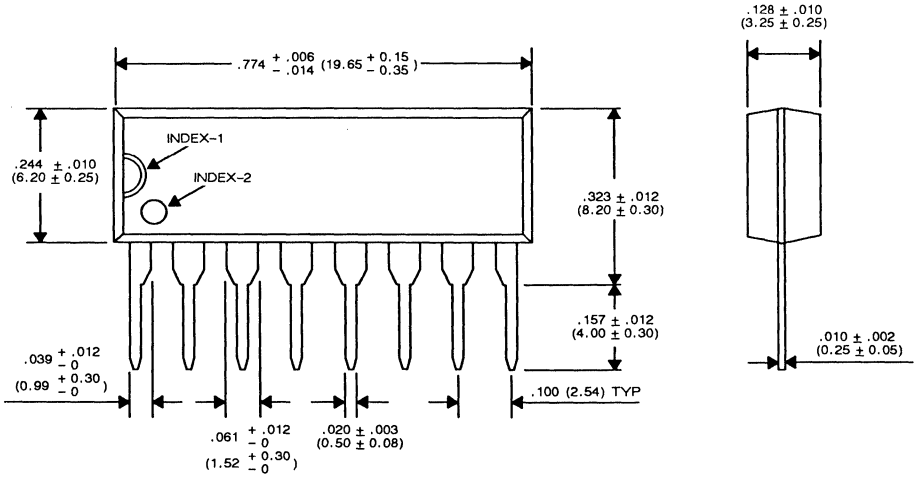


Note: The DC Output Voltage V_{OO} is obtained roughly from the following equation.

$$V_{OO} \simeq 0.75 \left(1 + \frac{R_F}{R_E}\right)$$

PACKAGE DIMENSIONS

8-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE No.: SIP-08P-M03)



Dimensions in inches (millimeters)

S08010S-2C

3

FUJITSU

DUAL CONTROL AMPLIFIER

MB3110A

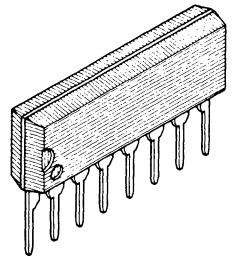
October 1987
Edition 1.0

DUAL CONTROL AMPLIFIER

The Fujitsu MB3110A is a dual-channel amplifier with separate volume-and-balance controls for both A-and-B channels. Each channel consists of a 20 dB amplifier with symmetrical balance attenuation over a wide range and low distortion of audio frequencies. Thus, the MB3110A is an excellent choice for general-purpose audio work and media reproduction that requires high-fidelity processing. The amplifier circuits are designed to provide optimum performance with a bare minimum of external parts.

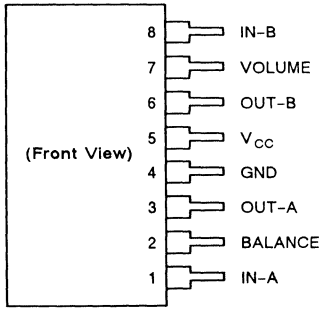
The MB3110A is housed in an 8-pin Single In-Line Package (SIP) that is especially useful where mounting space is limited or in applications where high-density populations are required.

- Voltage gain: 20 dB (typical)
- Input control voltage: OV to V_{CC}
- Maximum volume attenuation: 80 dB (typical)
- Maximum balance attenuation: 80 dB (typical)
- Low noise: 80 μV rms (typical)
- Maximum output voltage: 1.7V rms (typical)
- SIP package



PLASTIC PACKAGE
SIP-08P-M03

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS — T_A = 25 °C (see NOTE)

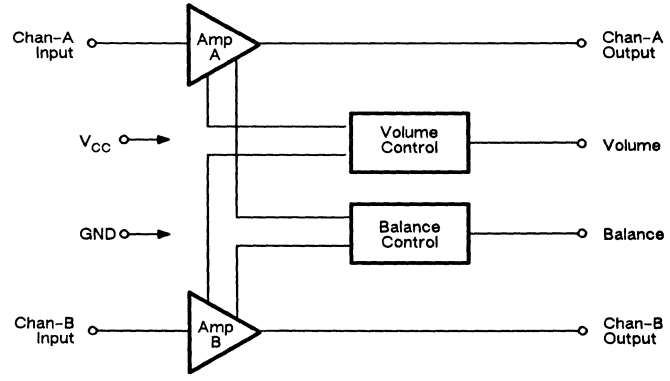
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	16	V
Input Control Voltage	V_C	0 to V_{CC}	V
Power Dissipation	P_D	530 ($T_A \leq 65$ °C)	mW
Operating Temperature	T_A	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

Fig. 1 — MB3110A BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	6 to 12	V
Load Resistance	R_L	≥ 32	Ω
Operating Temperature	T_A	-20 to +75	°C

ELECTRICAL CHARACTERISTICS

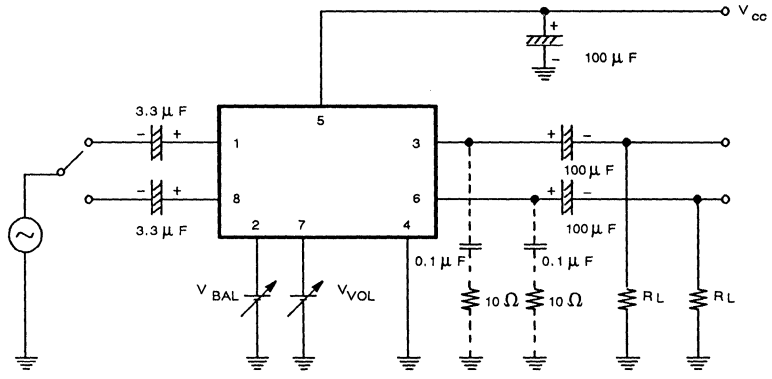
AC CHARACTERISTICS (V_{CC} = 9V, R_L = 100Ω, f = 1kHz, V_{IN} = 50 mV rms, and T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions (Note)	Values				Unit
			V_{VOL} (V)	Min	Typ	Max	
Power Supply Current	I_{CC}	V_{IN} = OV	9.0	—	8	14	mA
Voltage Gain	A_{VO}	—	9.0	18	20	22	dB
Volume Attenuation	A_{VMC}	—	4.0	8.5	10	11.5	dB
Maximum Volume Attenuation	A_{VMM}	—	0	70	80	—	dB
Balance Attenuation at Center Position	A_{BLC}	V_{BAL} = 4.5V	9.0	0.5	2.5	4.0	dB
Maximum Balance Attenuation	A_{BLM}	V_{BAL}= OV/9V	9.0	70	80	—	dB
Channel Balance	CB	—	9.0	-1	0	+1	dB
Channel Separation	CS	—	9.0	—	60	—	dB
Total Harmonic Distortion	THD	—	9.0	—	0.1	0.5	%
Maximum Output Voltage	V_{OM}	THD=1%	9.0	1.2	1.7	—	Vrms
Output Noise Voltage	V_{NO}	Rg = ∞, BW = 20 to 20kHz	0	—	80	200	μVrms
Input Resistance	R_{IN}	—	9.0	15	20	—	kΩ
Volume Control Input Current	I_{7H}	—	9.0	90	150	250	μA
High-level Balance Control Current	I_{2H}	V_{BAL} = 9.0V	9.0	36	60	100	μA
Low-level Balance Control Current	I_{2L}	V_{BAL} = OV	9.0	-100	-60	-36	μA

NOTE: Balance control pin is open unless otherwise specified.

3

Fig. 2 — TEST CIRCUIT

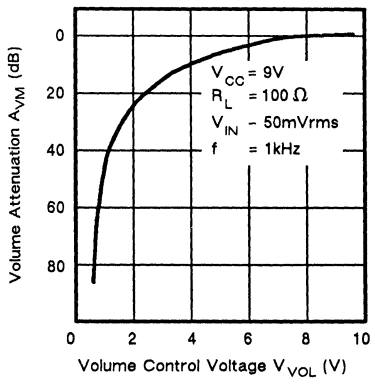


Notes:

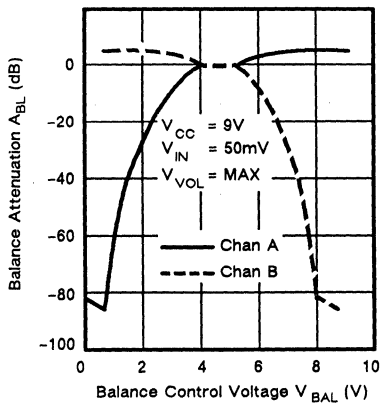
1. When measuring THD and V_{NO}, a bandpass filter with a bandwidth of 20Hz-to-20kHz is required; when measuring CS, a bandpass filter with a center frequency (fc) of 1 kHz is required.
2. Dotted-line components are used to inhibit parasitic oscillations.

TYPICAL PERFORMANCE CHARACTERISTICS

VOLUME RESPONSE

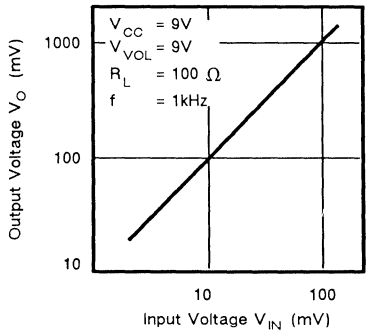


BALANCE RESPONSE

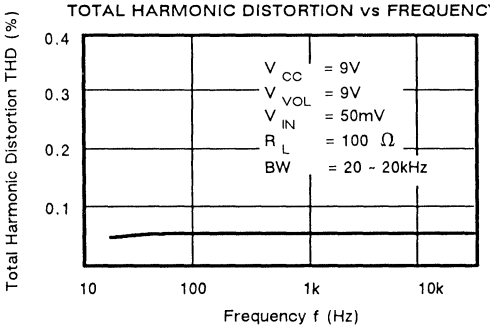


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

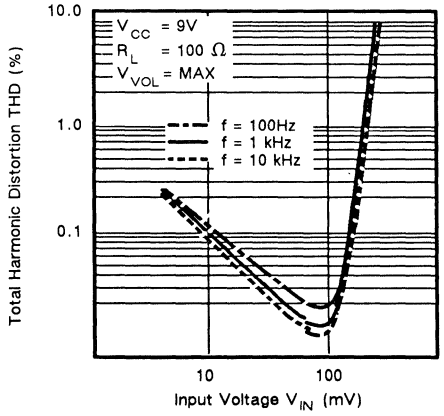
OUTPUT VOLTAGE vs INPUT VOLTAGE



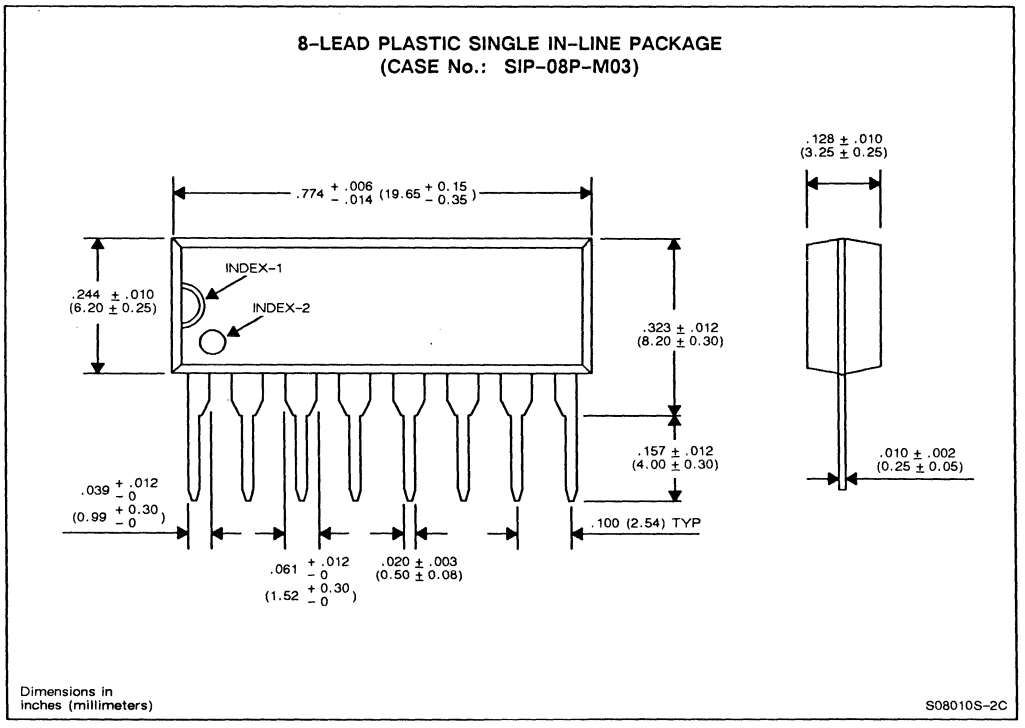
TOTAL HARMONIC DISTORTION vs FREQUENCY



TOTAL HARMONIC DISTORTION vs INPUT VOLTAGE



PACKAGE DIMENSIONS



FUJITSU

DISTORTION LIMITING IC FOR CAR AUDIO SYSTEMS

MB3111

April 1989
Edition 1.0

DISTORTION LIMITING IC

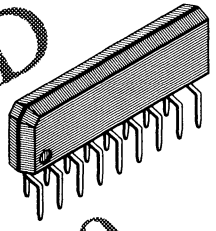
The Fujitsu MB3111 is a distortion limiting IC housed in a zig zag in-line package for high density mounting on print circuit boards for audio stereo systems.

The MB3111 is designed to avoid the clipping noise without poor dynamic response.

The MB3111 reads the output voltage of the power amplifier and automatically lowers the gain when the output voltage exceeds about 95% of the clipping level.

The MB3111 detects the possibility of wave clipping and controls the amplifier gain. The gain control works when large signal comes in and is determined by an external time constant.

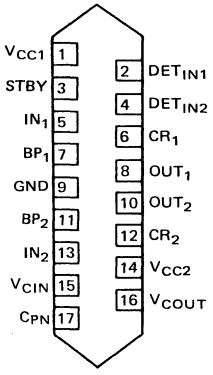
- Dual Distortion Limiting Circuits
- Keeping Dynamic Sound
- Low Output Noise Voltage
- Stand-by Mode
- Minimum External Circuit
- Small Package (ZIP-17-M01)



PLASTIC PACKAGE
ZIP-17P-M01

PIN ASSIGNMENT

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (See NOTE)

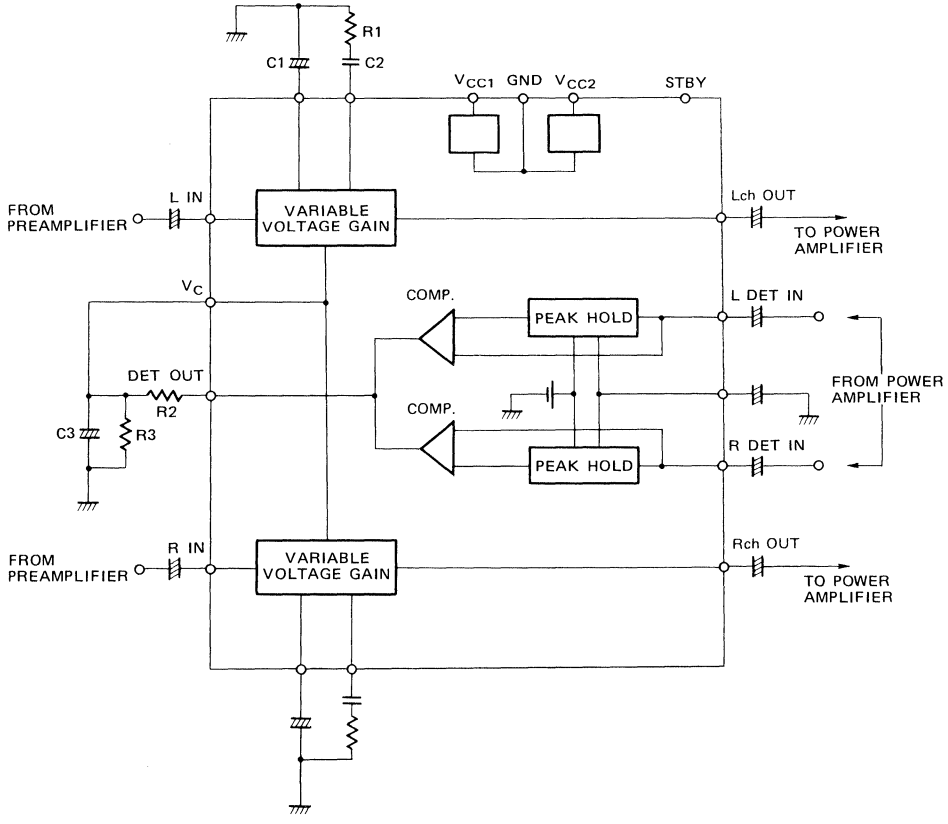
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC1}	−0.3 to 18	V
Power Dissipation	P_D	560	mW
Storage Temp.	T_{STG}	−55 to 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

Fig. 1 – BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Supply Voltage	V_{CC1}		8	13	16	V
	V_{CC2}		7	8	16	V
Input Voltage	V_I	Stand-by V_{IN}	0		16	V
			0			V
Output Load Resistance	R_{L1}	Out1, Out2		10		KΩ
	R_1	C_1 = 4700pF	0	40		KΩ
	R_2	V_{COUT}, C_3 = 4700pF	0	0.1		KΩ
	R_3		10	100		KΩ
Bypass Condenser	C	BP_1, BP_2		2.2		μF
Operating Ambient Temperature	T_a		-20		75	°C

ELECTRICAL CHARACTERISTICS

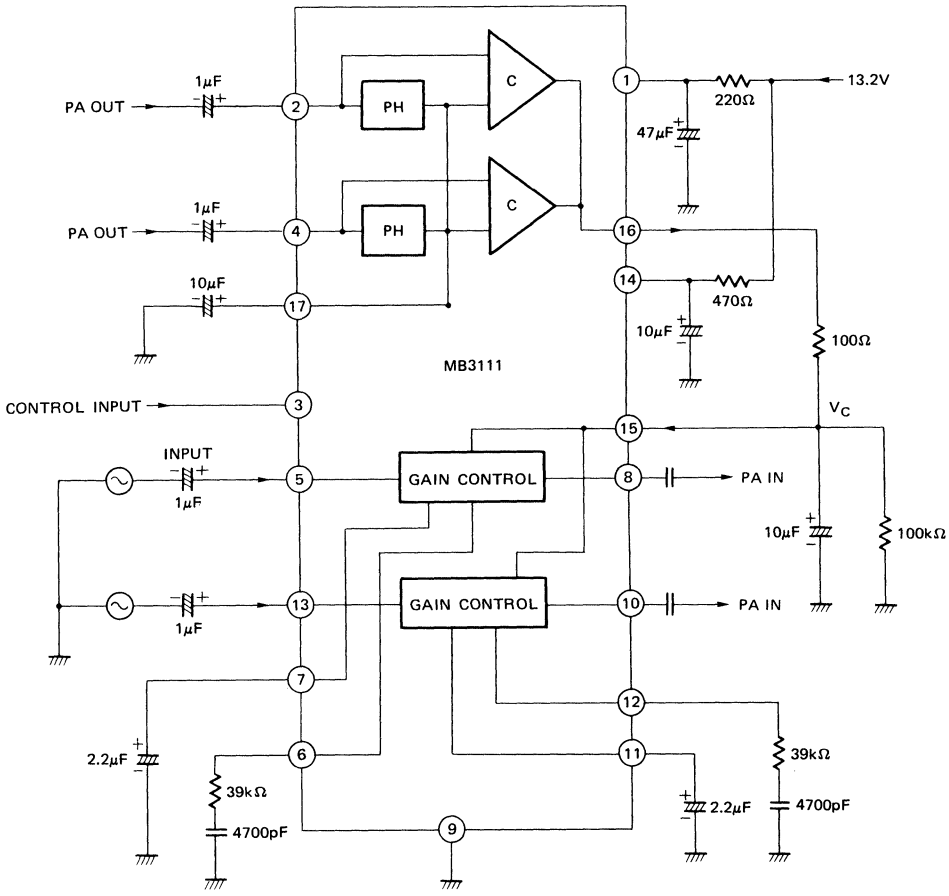
(T_a = 25°C, V_{CC1} = 13.2V, V_{CC2} = 8.5V, f = 1KHz, R_L = 10KΩ)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Supply Voltage	V_{CC1}		8	13	16	V
	V_{CC2}		7	8.5	16	V
Supply Current	I_{CC1}	DET_{IN} = 0V, V_{CC1}, V_{CC2} STBY = 0V		3.0	5.0	mA
	I_{CC2}			6.0	10.0	mA
	I_{CCO}				10	μA
Voltage Gain	A_V*	V = 0V	-1.0	0	1.0	dB
		V = 2.0V, f = 100Hz		-20	-15	dB
		V = 2.0V, f = 3kHz		-10		dB
Total Harmonic Distortion	THD	V_C = 0V, V_{IN} = 100mV		0.01		%
Maximum Input Voltage	V_{INMAX}	THD = 1%	1.0	1.5		V
Residual Noise Voltage	V_{no}	V_C = 0V, R_g = 0		5		μV
Stand-by Terminal Input Voltage	V_{IH}	Operating Stand-by	2.0		16	V
	V_{IL}		0		0.8	V
Detector Portion Input Resistance	$R_{IN(D)}$	Peak Hold Input		40		KΩ
Output Resistance	R_{OUT}	Internal Output Resistance		100		Ω
	I_{COUT}			100		μA
Control Portion Input Resistance	$R_{IN(C)}$	Gain Control Input		20		KΩ

*: R1 = 39KΩ, C2 = 4700pF

3

Fig. 2 – TYPICAL APPLICATION CIRCUIT



TYPICAL CHARACTERISTICS CURVES

Fig. 3 – GAIN vs. FREQUENCY

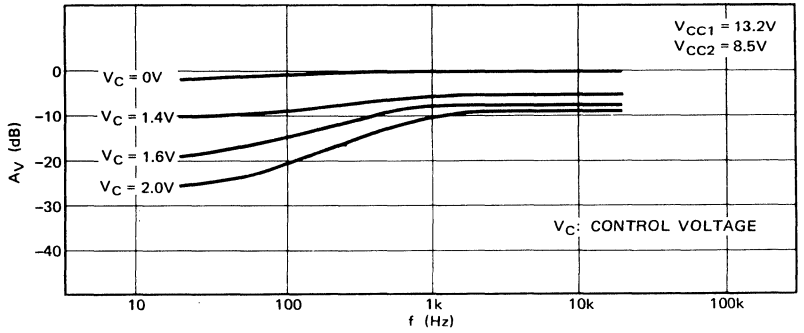


Fig. 4 – GAIN vs. CONTROL VOLTAGE

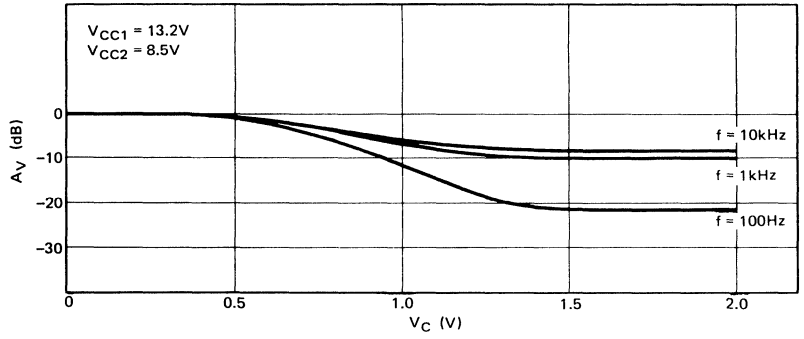
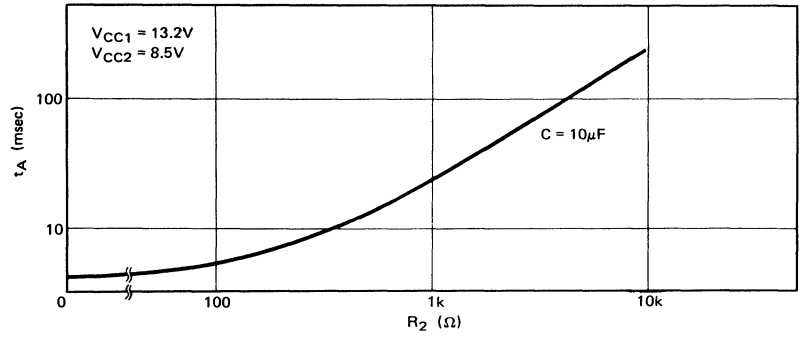


Fig. 5 – ATTACK TIME vs. EXTERNAL RESISTANCE (R2)



3

TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 6 – RELEASE TIME vs. EXTERNAL RESISTANCE (R3)

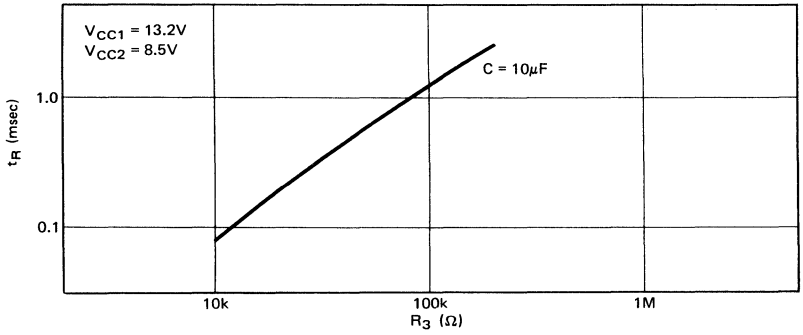
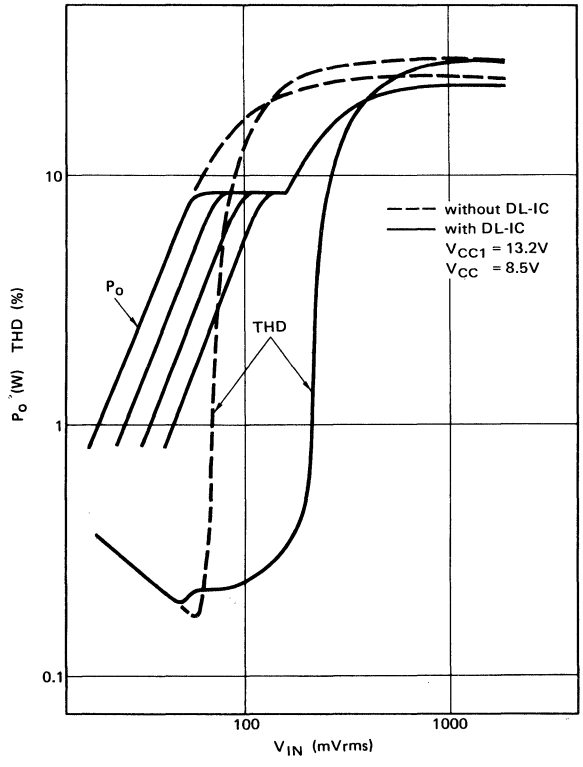


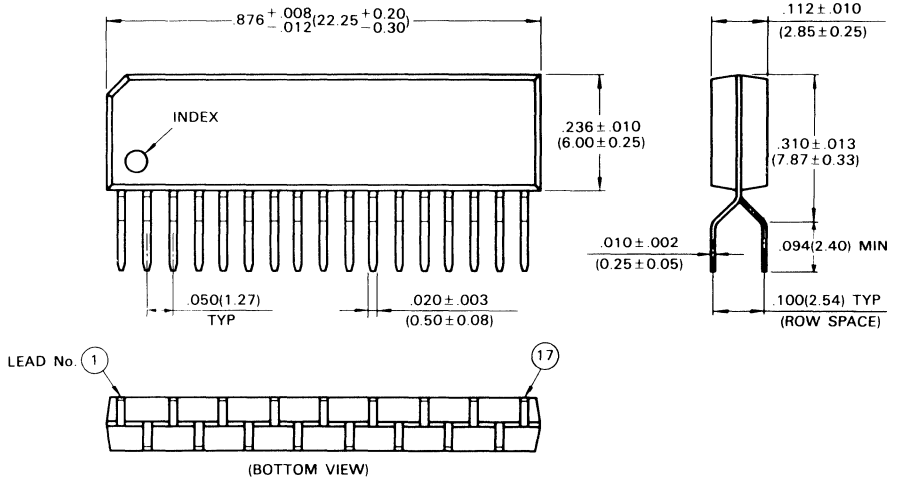
Fig. 7 – OUTPUT POWER/TOTAL HARMONIC DISTORTION vs. INPUT VOLTAGE



PACKAGE DIMENSIONS

17-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE

(Case No. : ZIP-17P-M01)



Dimensions in
inches (millimeters)

3

FUJITSU

6 WATT AUDIO AMPLIFIER

MB 3714A MB 3715A

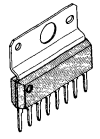
June 1986
Edition 1.0

MB 3714A/MB 3715A
6 Watt Audio Amplifier

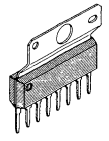
The Fujitsu MB 3714A and MB 3715A are monolithic integrated circuits of 6 Watt audio power amplifiers packaged in plastic single in-line package (SIP) with heat radiation fin.

The MB 3714A/MB 3715A are designed to reduce output distortion and power-on pop noise, working at high gain and high output power.

The MB 3714A and MB 3715A can drive even 2 ohm load and are designed against breakdown by load short and supply voltage surge. The packages are protected to mis-mounting with biased hole on the fin.



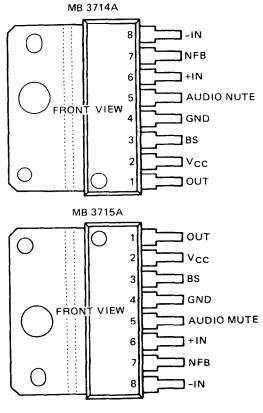
MB 3714A
PLASTIC PACKAGE
SIP-08P-M01



MB 3715A
PLASTIC PACKAGE
SIP-08P-M04

- High Power: 6.0 W typ/4Ω, 10.0 W typ/2Ω
- High Gain: 52.5 dB typ.
- Low Distortion
- Small Plastic 8-pin Single In-Line Package with Easily Heat Radiation and Mis-Mounting-Proof Form
- Minimum External Components
- Low Power-on Pop Noise
- Low Impedance Load: 2Ω Load
- Audio Mute Circuit
- Various Protection Circuits
- Power Supply Surge Protection
- Thermal Protection
- Load Short Protection

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Supply Voltage (Surge) ($t_s \leqq 0.2$ ms, $t_r \geqq 1$ ms)	V_{CCS}	40	V
Output Current (Peak)	I_{OP}	4.5	A
Power Dissipation ($T_C \leqq 75°C$)	P_D	7.5	W
Storage Temperature	T_{STG}	-55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

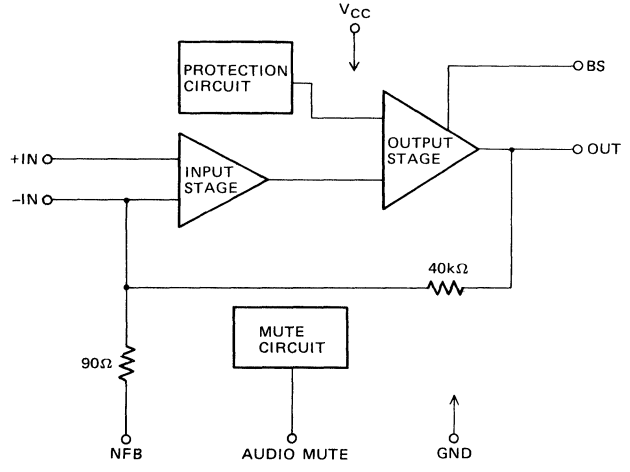
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	8.0		16.0	V
Operating Ambient Temperature	T_A	-20		+75	°C

BLOCK DIAGRAM

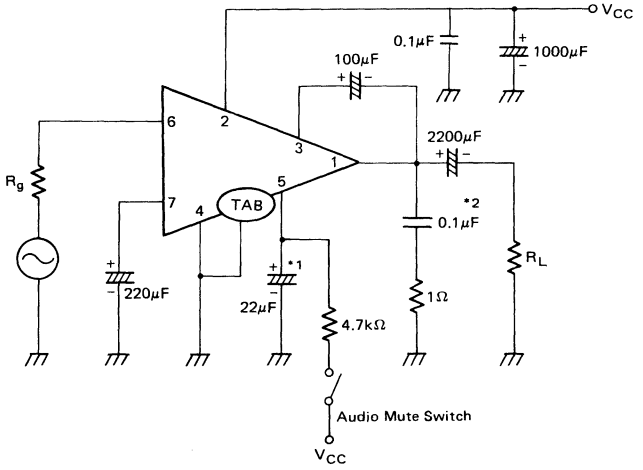


ELECTRICAL CHARACTERISTICS

(T_C = 25°C, V_{CC} = 13.2 V, R_L = 4 Ω and f = 1kHz, R_g = 600 Ω unless otherwise noted.)

Parameter	Condition	Symbol	Min	Typ	Max	Unit
Quiescent Power Supply Current	V_{IN} = 0	I_Q		30	60	mA
Voltage Gain	P_O = 1 W	A_V	50	52.5	55	dB
Output Power	THD = 10%	P_O	5.5	6.0		W
	THD = 10% R_L = 2 Ω		8.0	10.0		W
Output Noise Voltage	R_g = 10 kΩ BW = 20 to 20 kHz	V_{NO}		1.0	2.0	mV
Total Harmonic Distortion	P_O = 1 W	THD		0.2	1.0	%
	P_O = 1 W R_L = 2 Ω			0.3	1.0	%
Input Resistance		R_{IN}	20	30		kΩ
Attenuation Ratio at Audio Mute Mode		ATT		46		dB

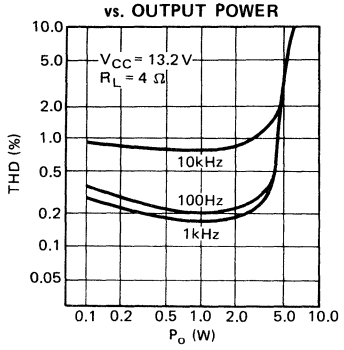
TYPICAL APPLICATION CIRCUIT



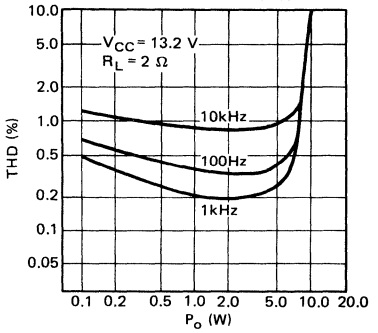
NOTE: *1: For improved ripple reduction, *2: Polyethlen Terephthalate Film Capacitor

3

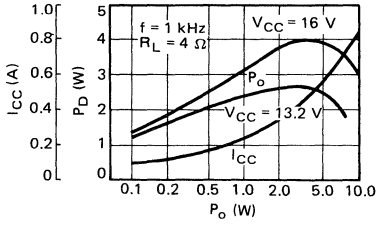
TOTAL HARMONIC DISTORTION
vs. OUTPUT POWER



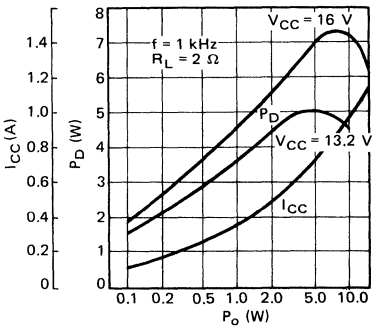
TOTAL HARMONIC DISTORTION
vs. OUTPUT POWER



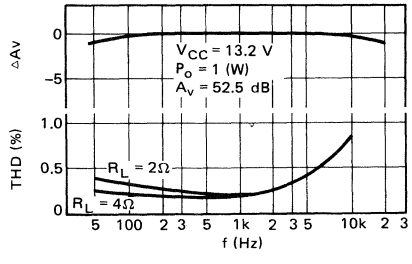
POWER DISSIPATION/SUPPLY
CURRENT vs. OUTPUT POWER



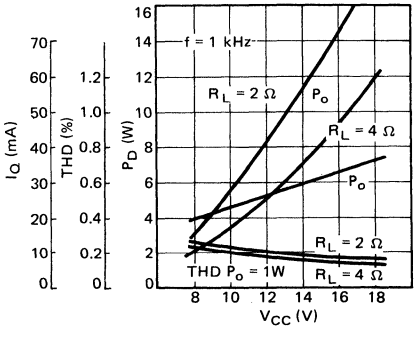
POWER DISSIPATION/SUPPLY
CURRENT vs. OUTPUT POWER



VOLTAGE GAIN/TOTAL HARMONIC
DISTORTION vs. FREQUENCY



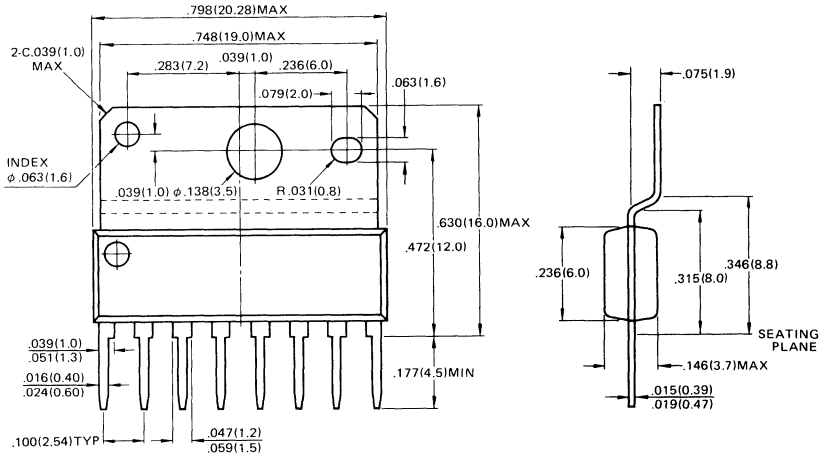
POWER DISSIPATION/THD/
SUPPLY CURRENT vs. V_{CC}



3

PACKAGE DIMENSIONS OF MB 3714A

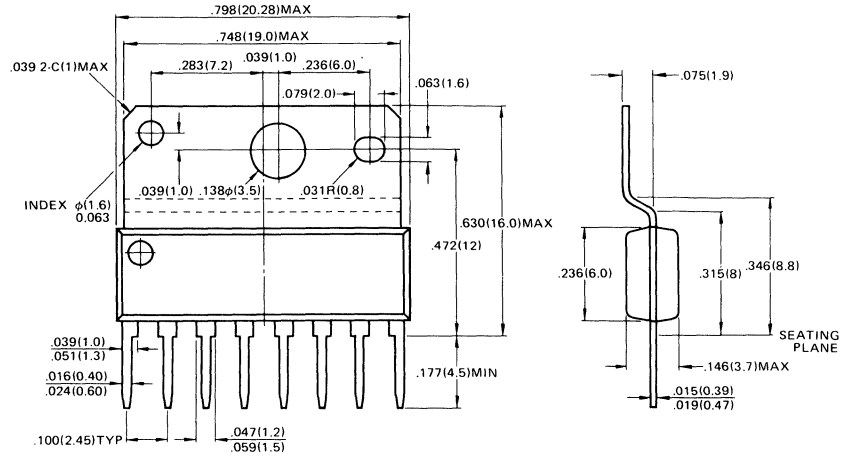
8-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE No.: SIP-08P-M01)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS OF MB 3715A

8-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE No.: SIP-08P-M04)



Dimensions in inches (millimeters)

December 1988
Edition 1.0

COMPANDOR IC

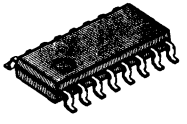
The Fujitsu MB3120 is a compandor IC to expand dynamic range at transmission/reception systems and to improve the tone quality by means of restricting noise.

Two function are loaded on one IC, the one is the compressor which has the 2/1 ratio of input/output ratio by logarithm, and the expandor which has the 1/2 ratio of input/output ratio by logarithm.

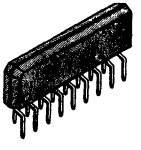
The MB3120 is encapsulated in a small package, this enables high density mounting.

The MB3120 is most suitable to a mobile radio system like as cellular radio, MCA and handy telephone set.

- Wide power supply voltage range (3.2V to 10.0V)
- Low power supply current
- ON-chip both compressor and expandor
- Wide dynamic range
- Less external elements
- Inhibit function with compression/expantion ratio of one
- Equipped with mute function which cut off the output signal
- 16-pin Flat Package
  17-pin Zig-zag In-line Package

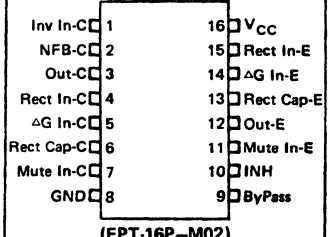


PLASTIC PACKAGE
FPT-16P-M04



PLASTIC PACKAGE
ZIP-17P-M01

PIN ASSIGNMENT
(TOP VIEW)



(FPT-16P–M02)

ZIP-17P-M01 Pin Assignment
Please See Page 12

ABSOLUTE MAXIMUM RATINGS (See NOTE)

(T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	12	V
Mute Control Voltage	V_{MUTE}	5*	V
Inhibit Control Voltage	V_{INH}	5*	V
Power Dissipation	P_D	560	mW
Operating Temperature	T_A	−20 to +75	°C
Storage Temperature	T_{STG}	−55 to +125	°C

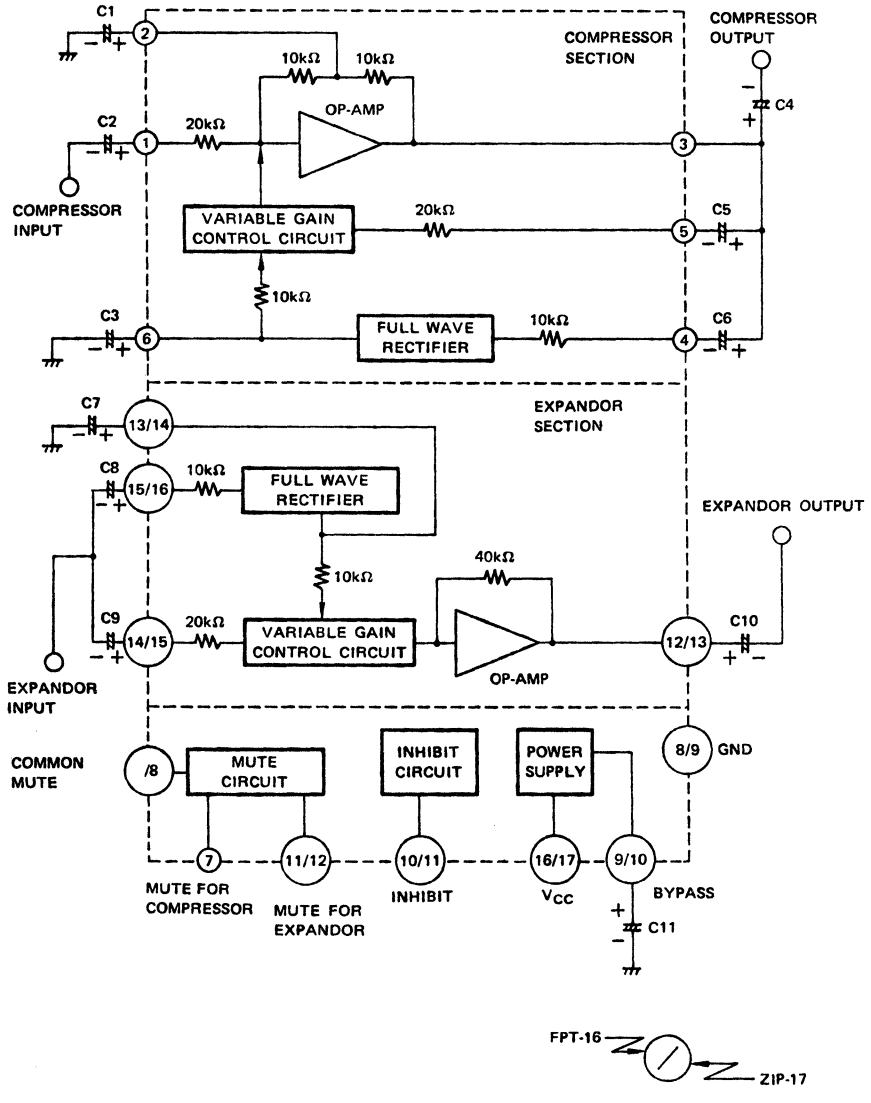
*: This value takes V_{CC} when V_{CC} is less than 5V.

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

MB3120 BLOCK DIAGRAM



BLOCK DESCRIPTIONS

C_1 : C_1 determines the low cut off frequency of compressor section.

$$fc = \frac{1}{2\pi R \cdot C_1}$$

R is on chip feed back resistor (10kΩ typ.)

C_2, C_8, C_9 : Input coupling condenser

C_3, C_7 : Smooth capacitor of full wave rectifier. Atack time and recovery time are determined by C_3 and C_7. Time constant T_C is specified as shown below.

T_C (ms) ≒ 10 x C_3 (μF)

C_4, C_{10} : Output coupling condenser

C_5, C_6 : Coupling condenser for internal feed back of compressor section.

C_{11} : Ripple filter condenser

3

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	3.2		10	V
Operating Temperature	T_A	-20		75	°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 8V, T_A = 25°C, f = 1kHz, R_L = 10kΩ)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power Supply Current	I_{CC}			3.0	4.5	mA

Compressor

Input Resistance	R_{INC}		14	20		kΩ
Input Reference Level	V_{OCO}	V_{IN} = -6dBm	-10.5	-9.0	-7.5	dBm
		V_{IN} = -6dBm, T_A = -20 to 75°C*2	-2.5	0	2.5	dB
Output Level*1	V_{OC1}	V_{IN} = -20dB	-10.5	-10.0	-9.5	dB
	V_{OC2}	V_{IN} = -40dB	-20.7	-20.0	-19.3	dB
	V_{OC3}	V_{IN} = -60dB	-31.5	-30.0	-29.0	dB
		V_{IN} = -60dB, T_A = -20 to 75°C*2	-4.0	0	3.0	dB
	V_{OC4}	V_{IN} = -80dB		-40.0		dB

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Expandor						
Input Resistance	R_{INE}		4.7	6.7		kΩ
Input Reference Level	V_{OE0}	V_{IN} = -9dBm	-1.5	0	1.5	dBm
		V_{IN} = -9dBm, T_A = -20 to 75°C*2	-2.5	0	2.5	dB
Output Level*1	V_{OE1}	V_{IN} = -10dB	-20.5	-20.0	-19.5	dB
	V_{OE2}	V_{IN} = -20dB	-40.7	-40.0	-39.3	dB
	V_{OE3}	V_{IN} = -30dB	-61.0	-60.0	-58.5	dB
		V_{IN} = -30dB, T_A = -20 to 75°C*2	-3.0	0	4.5	dB
	V_{OE4}	V_{IN} = -40dB		-80.0		dB
Compandor						
Total Harmonic Distortion	THD	V_O = 0dBm		0.5	2.0	%
Output Noise Voltage	V_{ON}	BW = 100Hz to 5kHz			-80.0	dBm
Voltage Gain	A_V	V_{IN} = -6dBm	4.5	6.0	7.5	dB
Gain Deviation 1	ΔA_{V1}	V_{IN} = -6dBm, T_A = -20 to 75°C*2	-3.0	0	3.0	dB
Gain Deviation 2	ΔA_{V2}	f = 200Hz to 5kHz, V_{OI} = 0dBm	-0.5	0	0.5	dB
Voltage Gain at Inhibit	A_{VINH}	V_{IN} = -6dBm, V_{ININH} = 0.4V	4.5	6.0	7.5	dB
Compressor Mute Attenuation	V_{OCMUTE}	V_{IN} = -6dBm, $V_{INCMUTE}$ = 2.7V		-50		dBm
Expandor Mute Attenuation*3	V_{OEMUTE}	V_{IN} = -9dBm, $V_{INEMUTE}$ = 2.7V		-70		dBm
High-level Control Voltage for Mute and Inhibit Pins*3	V_{IH}		2.7			V
Low-level Control Voltage for Mute and Inhibit Pins*3	V_{IL}				0.4	V

Notes:

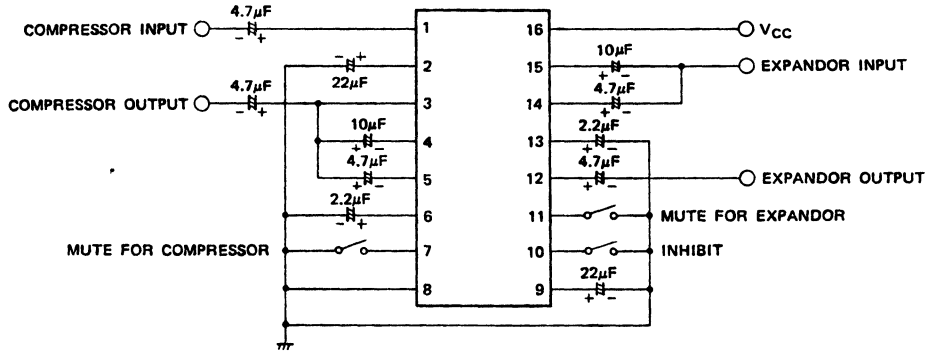
*1 Measured at input reference level of 0dB.

*2 Gain deviation with temperature when output level of 25°C is specified as 0dB.

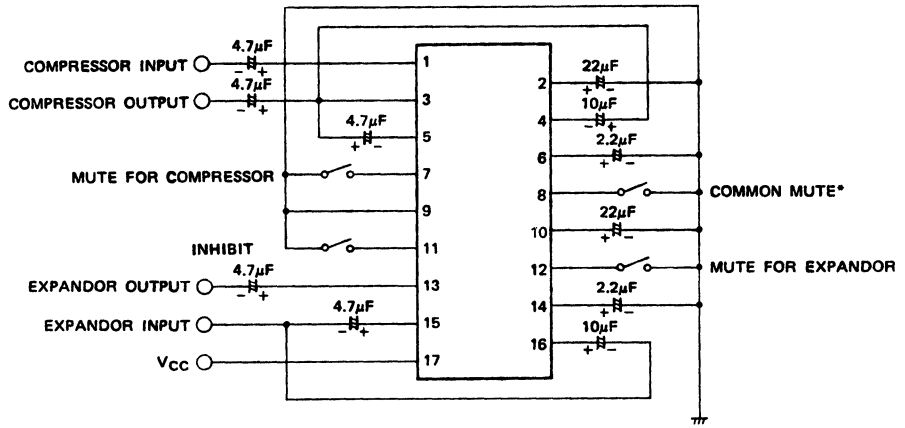
*3 As for Zip-17 pin, both compressor and expandor circuit enter mute function depending on 8 pin input.

TYPICAL CONNECTION EXAMPLE

FPT-16



ZIP-17



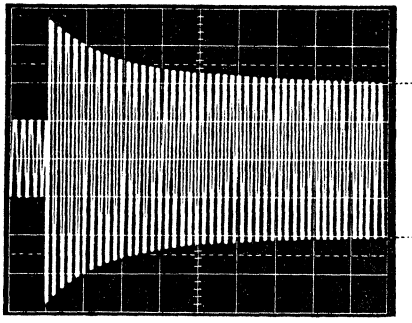
*: Both the mute of Compressor and Expandor can be controlled by this terminal.

OUTPUT TRANSITION RESPONSE CHARACTERISTICS

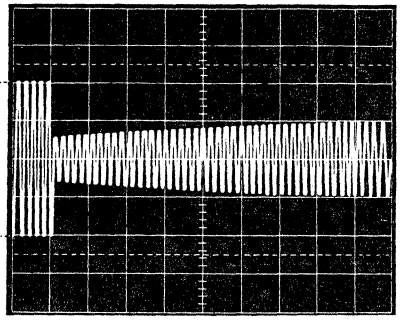
Condition: V_{CC} = 8V, f = 1kHz, R_L = 10kΩ, Mute OFF, INH OFF, Typ. connection

COMPRESSOR (Y: 0.2V/div, X: 5msec/div)

V_{IN} = −18dBm → −6dBm (V_O = −15dBm → −9dBm)

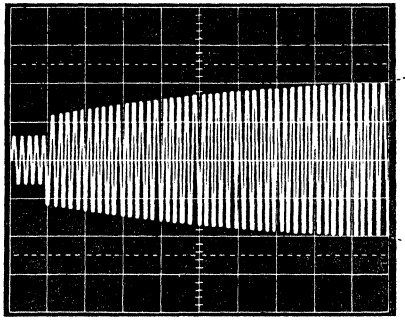


V_{IN} = −6dBm → −18dBm (V_O = −9dBm → −15dBm)

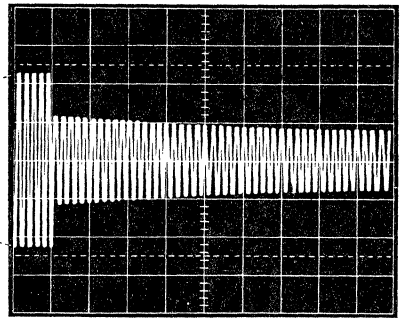


EXPANDOR (Y: 0.5V/div, X: 5msec/div)

V_{IN} = −15dBm → −9dBm (V_O = −12dBm → 0dBm)

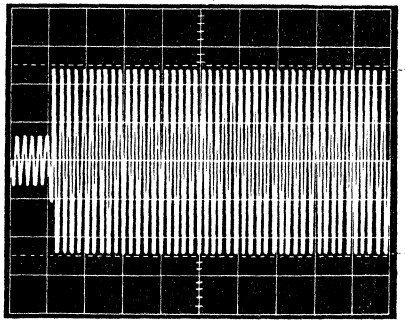


V_{IN} = −9dBm → −15dBm (V_O = 0dBm → −12dBm)

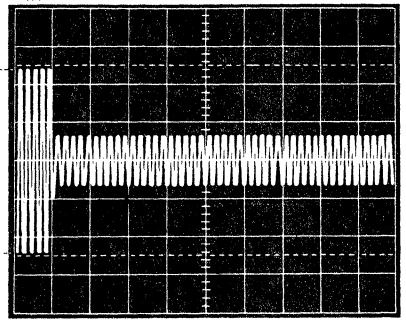


COMPANDOR (Y: 0.5V/div, X: 5msec/div)

V_{IN} = −18dBm → −6dBm (V_O = −12dBm → 0dBm)



V_{IN} = −6dBm → −18dBm (V_O = 0dBm → −12dBm)



TYPICAL CHARACTERISTICS CURVES

Fig. 1 – INPUT VOLTAGE vs. OUTPUT LEVEL

f = 1kHz
Mute OFF
INH OFF
Rg = 600Ω
R_L = 10kΩ
TYP. CONNECTION

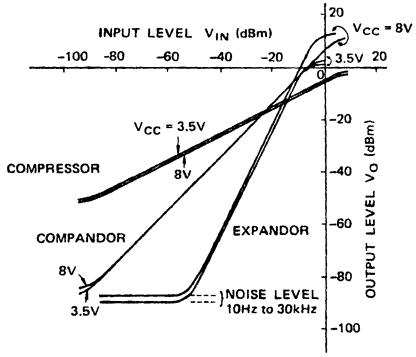


Fig. 2 – INPUT VOLTAGE vs. OUTPUT LEVEL (INHIBIT COND.)

f = 1kHz
Mute OFF
INH ON
Rg = 600Ω
R_L = 10kΩ
TYP. CONNECTION

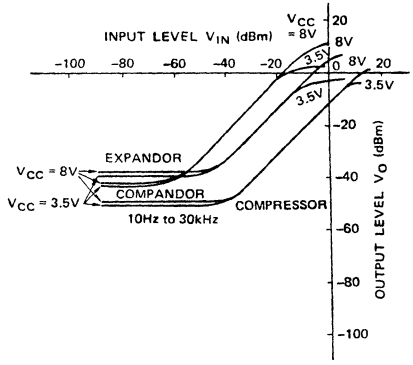


Fig. 3 – INPUT REFERENCE LEVEL vs. VOLTAGE SUPPLY

f = 1kHz
Mute OFF
INH OFF ------ R_L = 600Ω
Rg = 600Ω —— R_L = 10kΩ

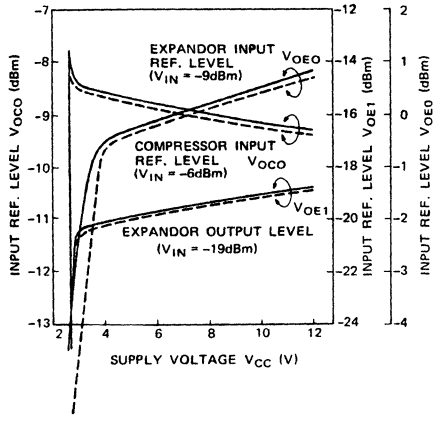
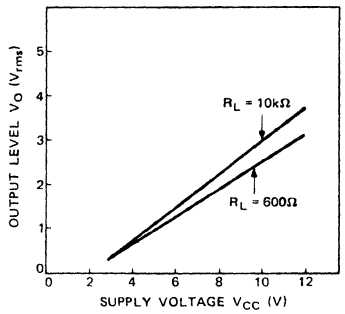


Fig. 4 – MAX. OUTPUT LEVEL vs. SUPPLY VOLTAGE (COMPANDOR)

LPF: 100kHz
THD = 1% INH OFF
Mute OFF Rg = 600Ω



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TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 5 – FREQUENCY vs. VOLTAGE GAIN (COMPANDOR)

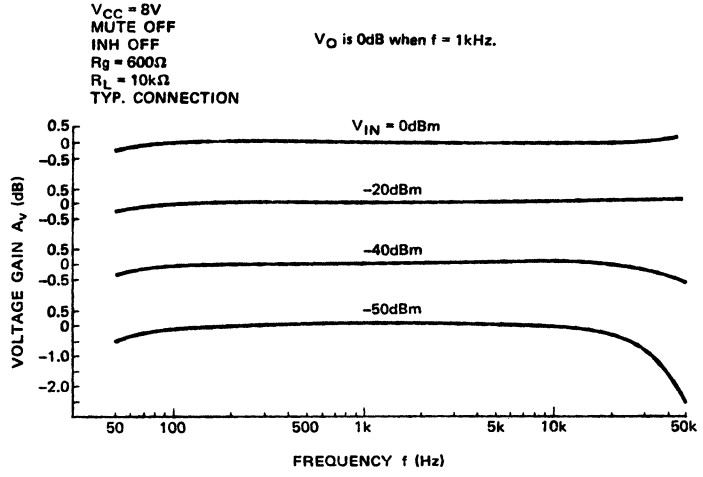


Fig. 6 – INPUT REFERENCE LEVEL vs. TEMPERATURE

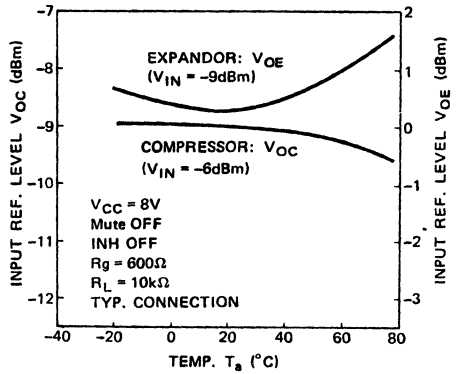
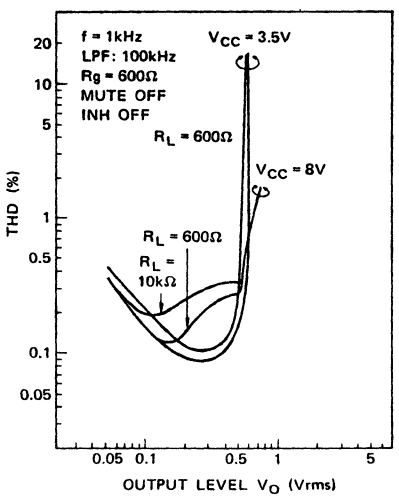


Fig. 7 – OUTPUT LEVEL vs. TOTAL HARMONIC DISTORTION (COMPRESSOR)



TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 8 – OUTPUT LEVEL vs. TOTAL HARMONIC DISTORTION (EXPANDOR)

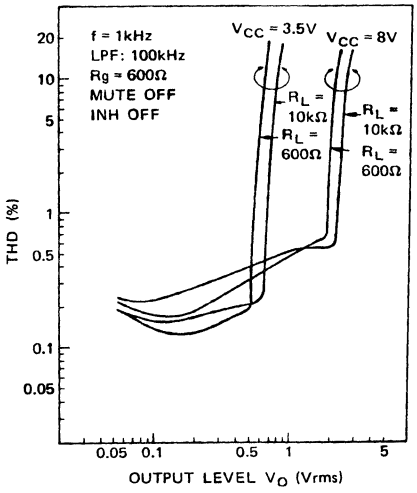


Fig. 9 – OUTPUT LEVEL vs. TOTAL HARMONIC DISTORTION (COMPANDOR)

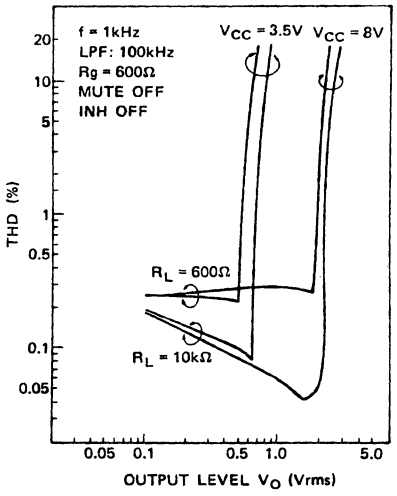


Fig. 10 – OUTPUT LEVEL vs. TOTAL HARMONIC DISTORTION (EXPANDOR INHIBIT COND.)

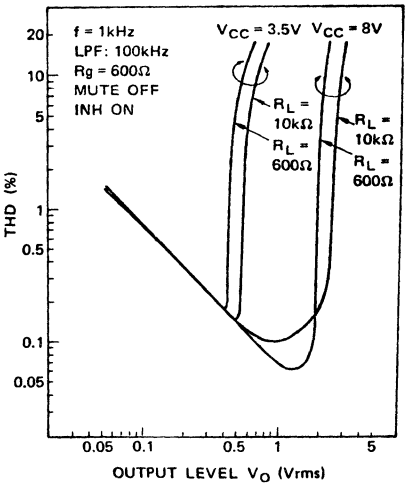
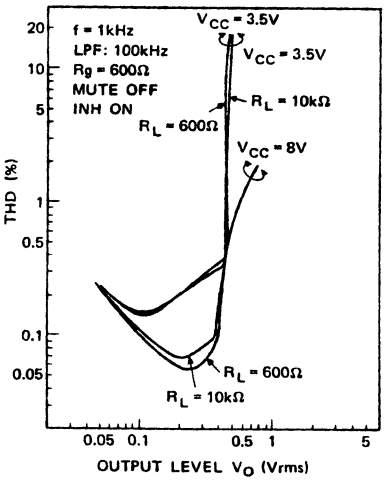


Fig. 11 – OUTPUT LEVEL vs. TOTAL HARMONIC DISTORTION (COMPRESSOR INHIBIT COND.)



TYPICAL CHARACTERISTICS CURVES (continued)

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Fig. 12 – FREQUENCY vs. TOTAL HARMONIC DISTORTION (COMPANDOR)

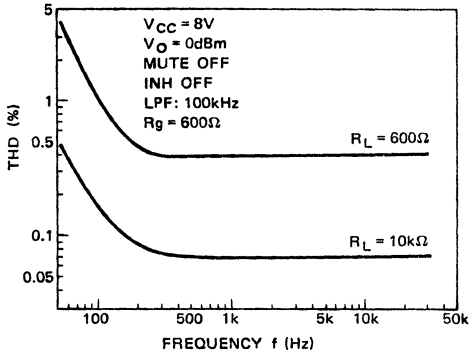


Fig. 13 – EXAPNDOR MUTE ATTENUATION

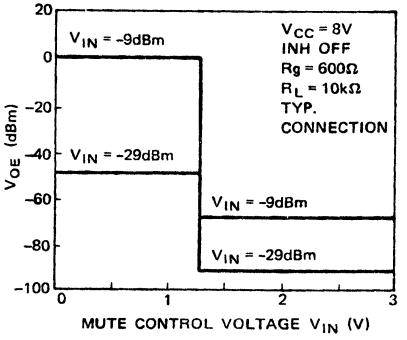
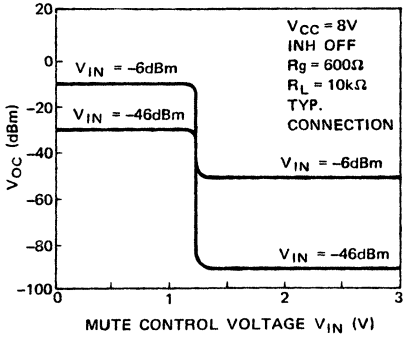
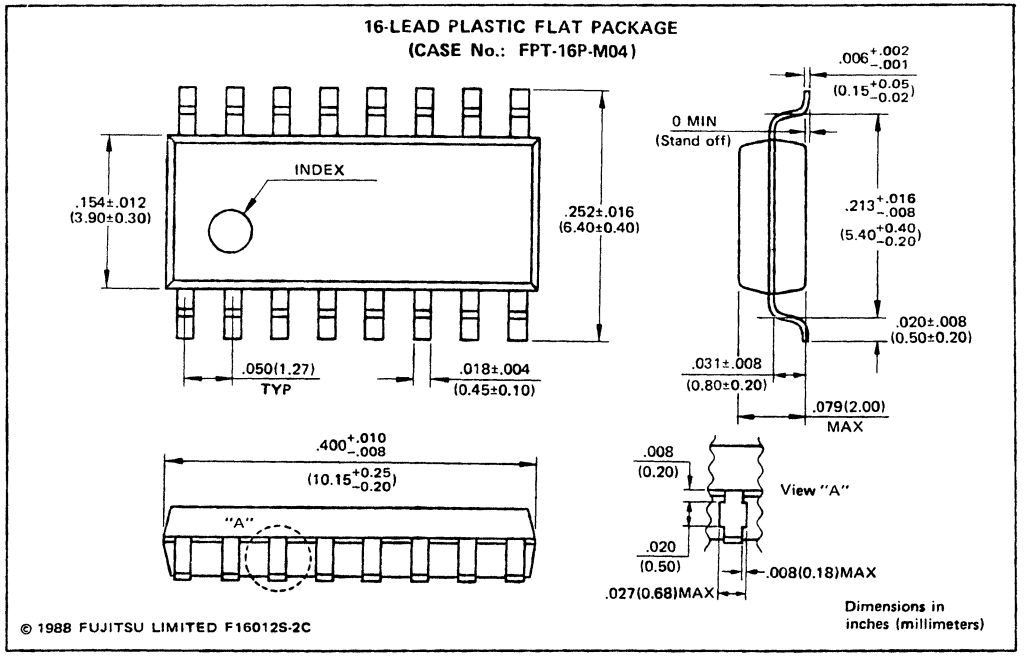


Fig. 14 – COMPRESSOR MUTE ATTENUATION



PACKAGE DIMENSIONS



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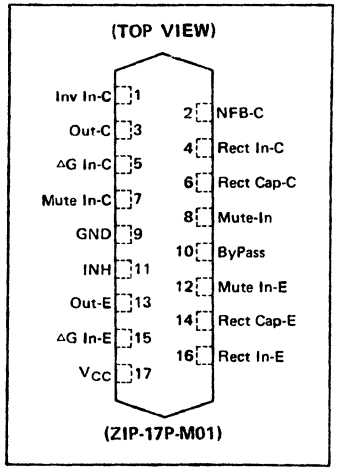
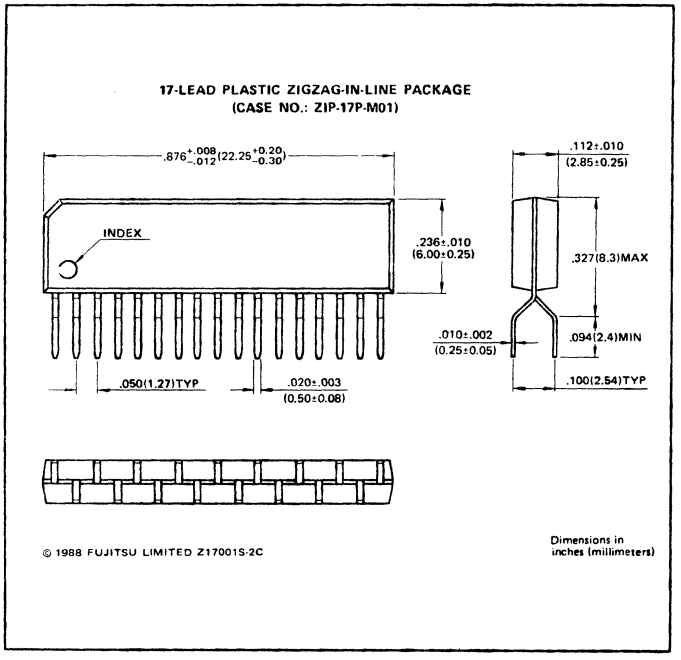
PACKAGE DIMENSIONS (continued)





FUJITSU

5.8 W DUAL AUDIO POWER AMPLIFIER

MB3722

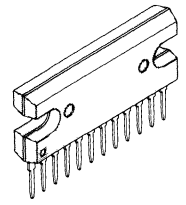
February 1989
Edition 1.0

5.8W DUAL AUDIO POWER AMPLIFIER

The Fujitsu MB3722 is designed for a dual low-frequency high-power amplifier which is packed in 12 pin single in line plastic package. The MB3722 requires a few external components, this enables high density mounting. Design for heat radiation is easy because thermal resistance is low.

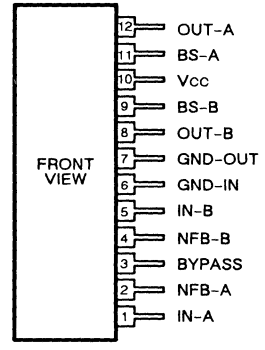
The MB3722 contains internal power-on pop noise protection circuitry and various protection circuitry. The device is suitable best for car-stereo.

- High power output: 5.8 W typ.
- Low Noise Output Voltage: 0.8 mV typ.
- Low Total Harmonic Distortion: 0.2 % typ.
- Minimum external components
- On chip power on pop noise protection circuit
- Audio mute function is provided
- Separated GND pins for Input/Output circuit
- Various protection circuits
  - — Over voltage protection
  - — Thermal protection
  - — Load short protection
  - — Output pin-to-DC short protection



PLASTIC PACKAGE
SIP-12P-M01

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

(Tc = 25°C)

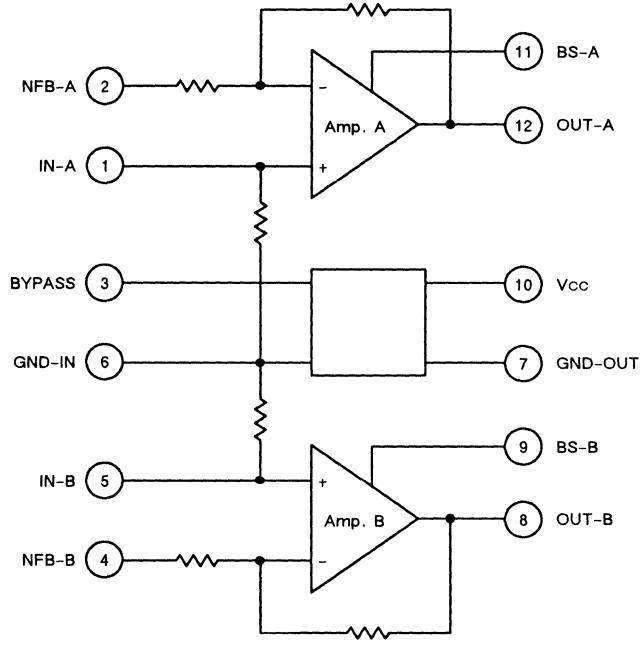
Rating	Symbol	Value	Unit
Power Supply Voltage (No signal)	V_{CCDC}	24	V
Power Supply Voltage (Operation)	V_{CC}	18	V
Power Supply Voltage (Surge)	V_{CCS}	40 *	V
Output Current (Peak)	I_{OPEAK}	4.5	A
Power Dissipation	P_D	18	W
Operating Temperature(Case)	T_c	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +150	°C

NOTE: * $t_s \leq 0.2$ sec, $t_r \geq 1$ msec

Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

Fig. 1 — MB3722 BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8 to 16	V
Operating Temperature	T_C	-20 to +75	°C
Output Load	R_L	2 to 8 *	Ω

Note:

* Dual operation.

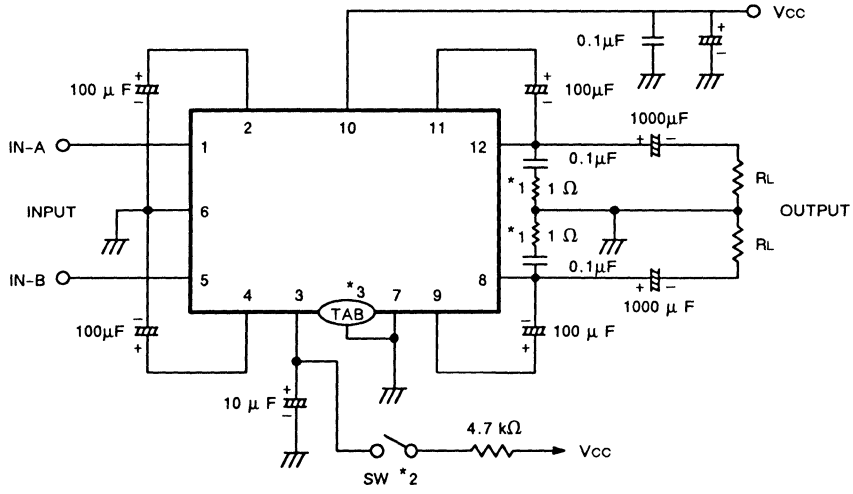
ELECTRICAL CHARACTERISTICS

(Vcc = 13.2 V, f = 1 kHz, RL = 4Ω, Tc = 25°C, One channel operation)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Quiescent Power Supply Current	IQ	VIN=0V		80	160	mA
Voltage Gain	AV	PO=1W	48.5	50.5	52.5	dB
Difference Voltage Gain	ΔAV	PO=1W		0	1.5	dB
Output Power	PO	THD=10%	5.0	5.8		W
Total Harmonic Distortion	THD	PO=1W		0.2	1.0	%
Output Noise Voltage	VNO	Rg=10kΩ, BW = 20 Hz to20 kHz		0.8	1.6	mV
Input Resistance	RIN		20	30		kΩ
Cross Talk		Rg=600Ω	40	50		dB
Audio Mute Attenuation		Rg=600Ω		40		dB

3

Fig. 2 — TYPICAL APPLICATION EXAMPLE



Notes:

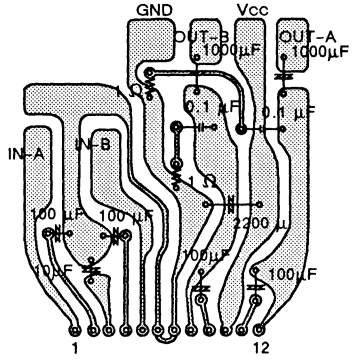
*1 Use Mylar condenser.

*2 When Vcc is apply to the pin 3, Audio mute (40dB) is available.

*3 The TAB should be connected with the GND.

3

Fig. 3 — TYPICAL APPLICATION CIRCUIT PATTERN (BOTTOM VIEW)



TYPICAL CHARACTERISTICS CURVES

Fig. 4 - TOTAL HARMONIC DISTORTION vs.OUTPUT POWER

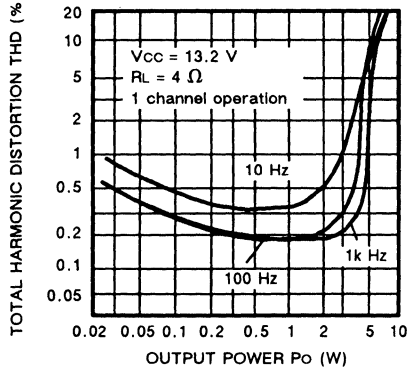


Fig. 5 - TOTAL HARMONIC DISTORTION vs.FREQUENCY

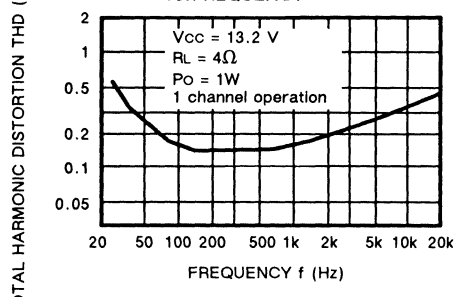
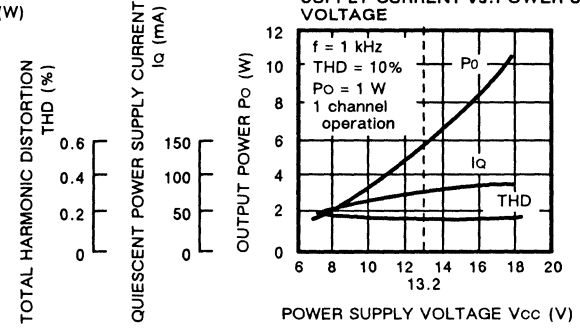


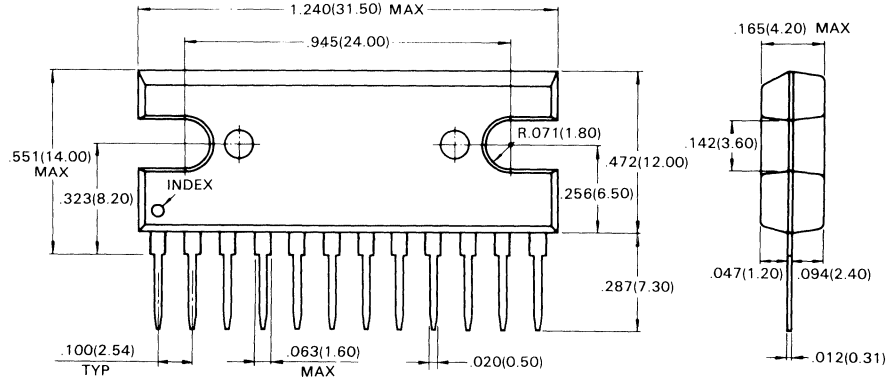
Fig. 6 - OUTPUT POWER/TOTAL HARMONIC DISTORTION/QUIESCENT POWER SUPPLY CURRENT vs.POWER SUPPLY VOLTAGE



3

12-LEAD PLASTIC SINGLE IN-LINE PACKAGE

(Case No. : SIP-12P-M01)



Dimensions in inches (millimeters)

3

FUJITSU

14 W BTL AUDIO POWER AMPLIFIER

MB3730A

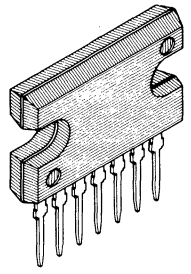
September 1988
Edition 1.0

14 W BTL AUDIO POWER AMPLIFIER

The Fujitsu MB3730A is designed for a low-frequency high-power amplifier with internal BTL (Balanced Transformer Less) circuitry. The MB3730A is packed in 7 pin single in line plastic package and requires a few external components, this enables high density mounting. Design for heat radiation is easy because thermal resistance is low 3°C/W.

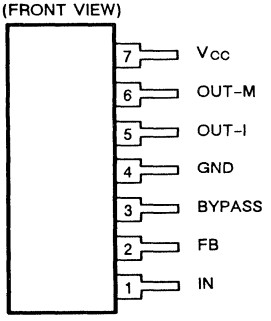
The MB3730A contains internal power-on pop noise protection circuit and various protection circuits. The device is suitable best for car-stereo.

- High power output : 14W typ.
- Minimum external components
- Various protection circuits
  - Over voltage protection
  - Load short protection
  - Thermal protection
  - Output pin-to-DC short protection
- No break-down: between pins is shorted or inverted insertion
- Low thermal resistance : 3°C/W
- On-chip power-on pop noise protection circuit
- 7-pin Plastic Single In Line package (Suffix: -PS)



PLASTIC PACKAGE
SIP-07P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE) (Tc=25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	18	V
Power Supply Voltage (Surge)	V_{CCS}	50 *	V
Output Current (Peak)	I_{OPEAK}	4.5	A
Power Dissipation	P_D	18	W
Operating Temperature (Case)	T_C	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +150	°C

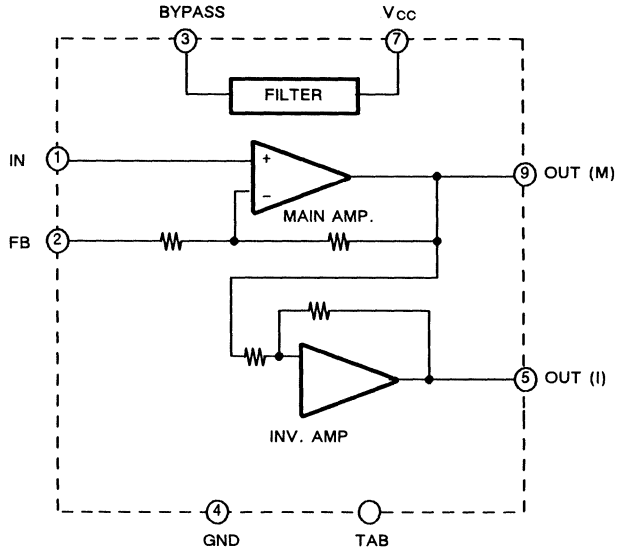
Note: * $ts \leq 0.2$ sec, $tr \geq 1$ msec

Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

Fig. 1 – MB3730A BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

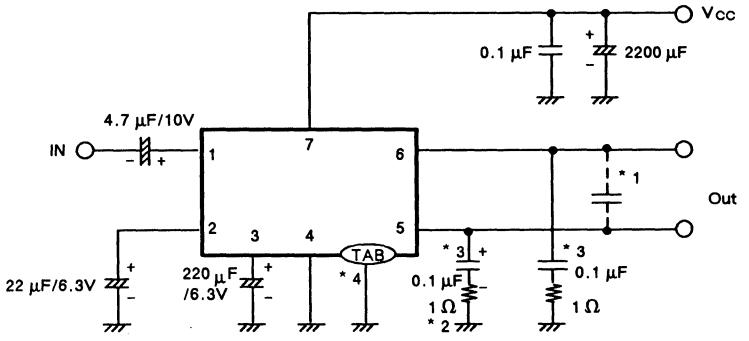
Parameter	Symbol	Value	Unit
Power Supply Voltage	Vcc	8 to 16	V
Operating Temperature(Case)	Tc	-20 to +75	°C

ELECTRICAL CHARACTERISTICS (Tc = 25°C, Vcc = 13.2V, RL = 4Ω, f = 1kHz))

Parameter	Symbol	Condition	Values			Unit
			Min	Typ	Max	
Quiescent Power Supply Current	I_Q	V_{IN}=OV, RL = ∞		80	200	mA
Voltage Gain	A_V	P_O = 1W	52.5	55	57.5	dB
Output Power	P_O	THD=10%	10	14		W
Total Harmonic Distortion	THD	P_O=1W		0.2	1.0	%
Output Noise Voltage	V_{NO}	Rg=10kΩ, BW=20 Hz to 20kHZ		1.0	2.0	mV
Input Resistance	R_{IN}		40	70		kΩ
Output Offset Voltage	V_{OO}	V_{IN} = OV		0.2	0.4	V

3

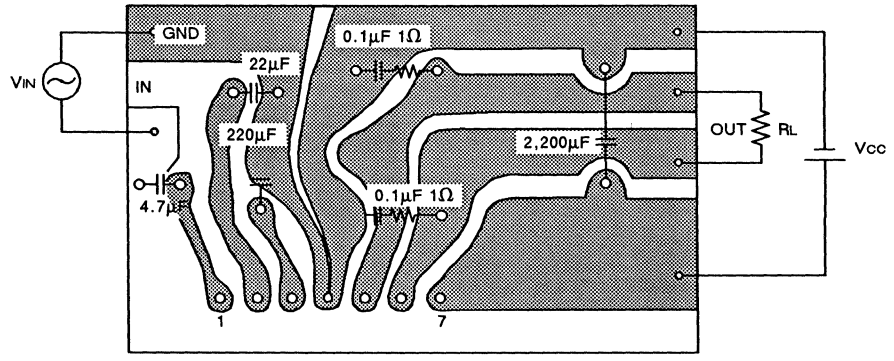
Fig. 2 – TYPICAL CONNECTION EXAMPLE



Notes:
*1 Effective to prevent from oscillation depending on printing pattern.
*2 When power supply line is stable, please connect with Vcc side, it restrains the oscillation.
*3 Use Mylar Capacitor.
*4 The TAB should be connected with GND.

3

Fig. 3 - RECOMMENDED CONNECTION PATTERN (BOTTOM VIEW)



TYPICAL CHARACTERISTICS CURVES

Fig. 4 - TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

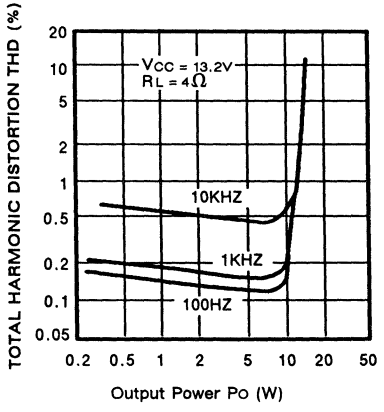
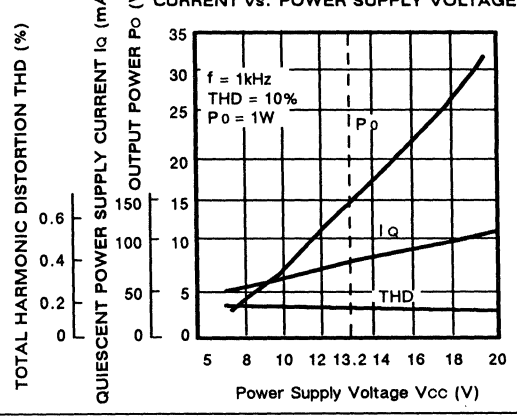


Fig. 5 - OUTPUT POWER/TOTAL HARMONIC DISTORTION/QUIESCENT POWER SUPPLY CURRENT vs. POWER SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS CURVES (Continued)

Fig. 6 - VOLTAGE GAIN vs. FREQUENCY

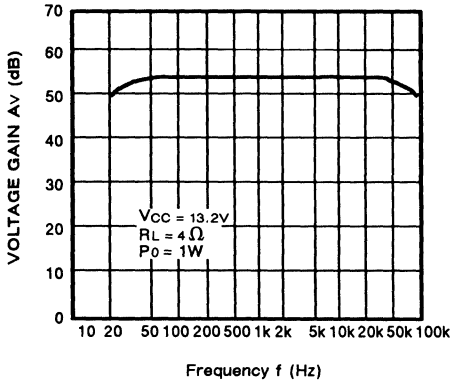


Fig. 7 - TOTAL HARMONIC DISTORTION vs. FREQUENCY

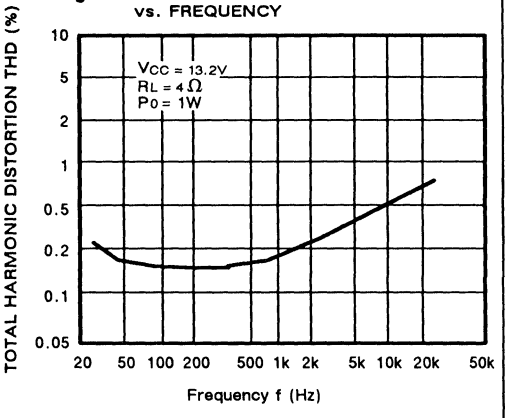
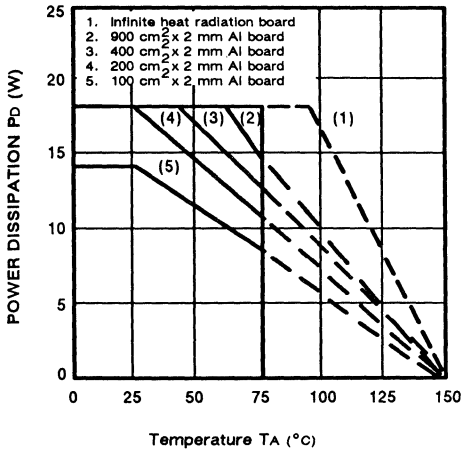


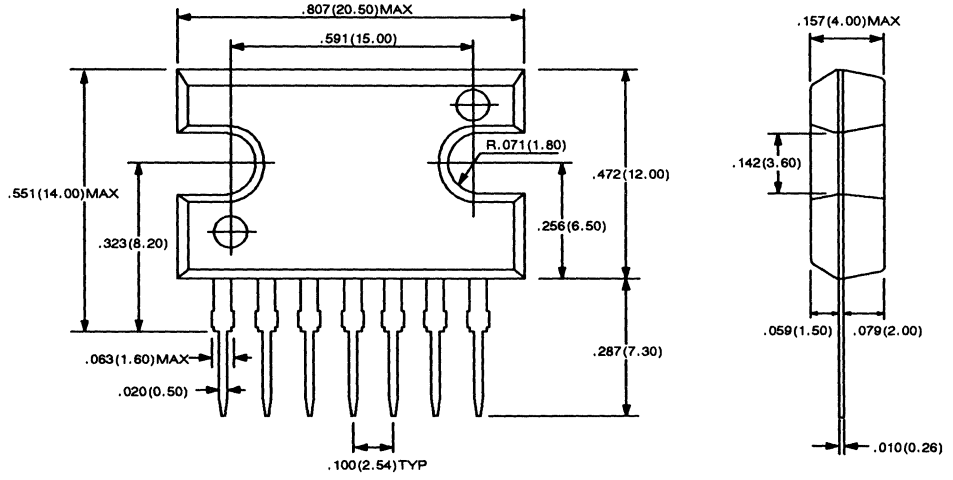
Fig. 8 - POWER DISSIPATION vs. TEMPERATURE



3

PACKAGE DIMENSION

7-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE No.: SIP-07P-M01)



Dimensions in
inches (millimeters)

S07002S-1C

FUJITSU

18 W BTL AUDIO POWER AMPLIFIER

MB3731

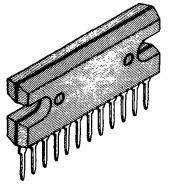
September 1988
Edition 1.0

18 W BTL AUDIO POWER AMPLIFIER

The Fujitsu MB3731 is designed for a low-frequency high-power amplifier with internal BTL (Balanced Transformer Less) circuitry. The MB3731 is packed in 12 pin Single in line plastic package and requires a few external components, this enables high density mounting. Design for heat radiation is easy because thermal resistance is low.

The MB3731 contains internal power-on pop noise protection circuit and various protection circuitry. The device is suitable best for car-stereo.

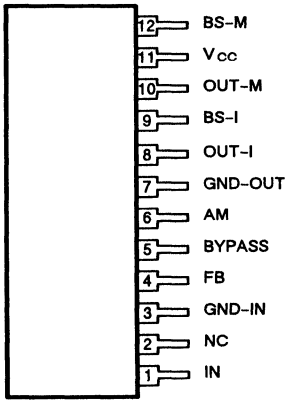
- High power output : 18W typ.
- Minimum external components
- On-chip power on pop noise protection circuit
- Audio mute function is provided
- Separated GND pins for Input/Output circuit
- Various protection circuits
  - Over voltage protection
  - Load short protection
  - Thermal protection
  - Output pin-to-DC short protection
- 12-lead Plastic single in-line Package (Suffix: -PS)



PLASTIC PACKAGE
SIP-12P-M01

PIN ASSIGNMENT

(FRONT VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE) (Tc=25°C)

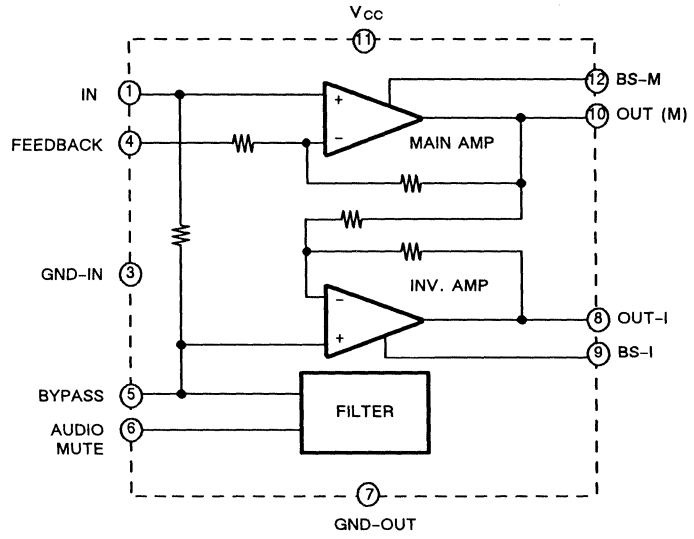
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	18	V
Power Supply Voltage (Surge)	V_{CCS}	40 *	V
Output Current (Peak)	I_{OPEAK}	4.5	A
Power Dissipation	P_D	18	W
Operating Temperature (Case)	T_C	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Note:

* $ts \leq 0.2$ sec, $tr \geq 1$ msec
Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

Fig. 1 – MB3731 BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

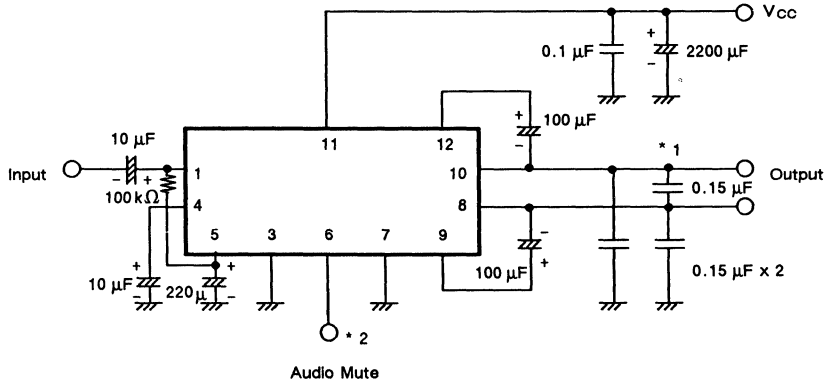
Parameter	Symbol	Value	Unit
Power Supply Voltage	Vcc	8 to 16	V
Operating Temperature (Case)	Tc	-20 to +75	°C

ELECTRICAL CHARACTERISTICS (T_A= 25°C, V_{CC}= 13.2V, RL=4Ω, f=1kHz)

Parameter	Symbol	Condition	Values			Unit
			Min	Typ	Max	
Quiescent Power Supply Current	I_Q	VIN=0V,RL= ∞		80	200	mA
Voltage Gain	A_V	PO=1W	44.5	47	49.5	dB
Output Power	P_O	THD=10%	15	18		W
Total Harmonic Distortion	THD	PO=1W		0.1	0.5	%
Output Noise Voltage	V_{NO}	RS=10kΩ,BW=20HZ to 20kHZ		0.5	1.0	mV
Input Resistance	R_{IN}		40	70		kΩ
Output Offset Voltage	V00	VIN=0V		0.2	0.4	V
Audio Mute Attenuation	—	PO=1W		43		dB

3

Fig. 2 – TYPICAL CONNECTION EXAMPLE

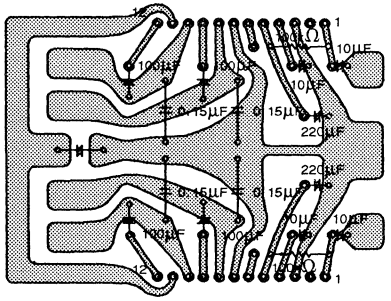


Notes: *1 Effective to prevent from the oscillation depending on printing pattern.
*2 The output can be cut off (Audio Mute) when pin 6 is connected with the GND.

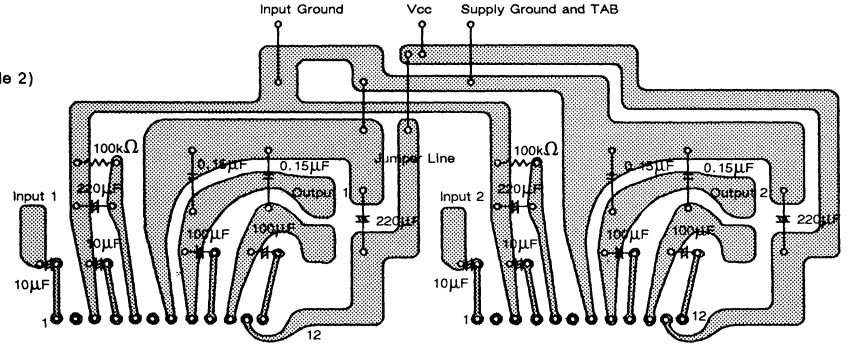
3

Fig. 3 – RECOMMENDED CONNECTION PATTERN (BOTTOM VIEW)

Example 1)



Example 2)



TYPICAL CHARACTERISTICS CURVES

Fig. 4 – TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

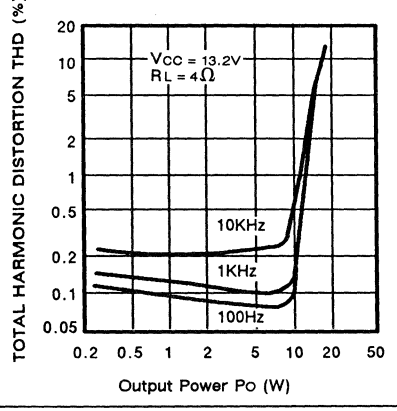
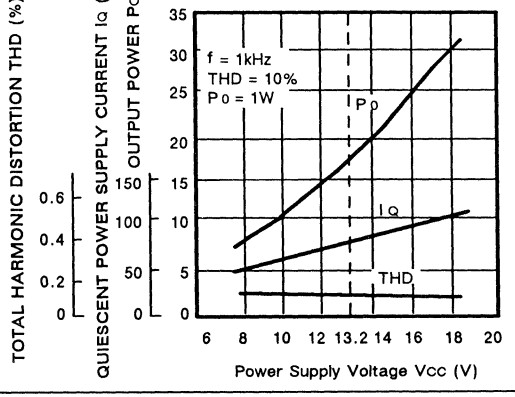


Fig. 5 – OUTPUT POWER/TOTAL HARMONIC DISTORTION/QUIESCENT POWER SUPPLY CURRENT vs. POWER SUPPLY VOLTAGE



TYPICAL CHARACTERISTICS CURVES (Continued)

Fig. 6 - VOLTAGE GAIN vs. FREQUENCY

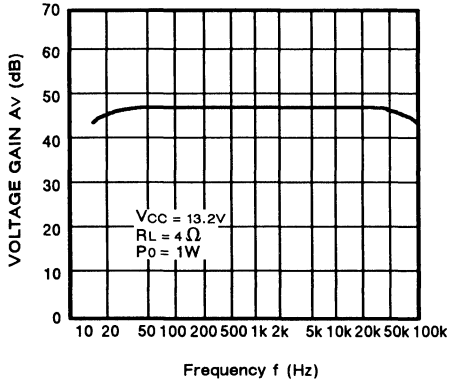


Fig. 7 - TOTAL HARMONIC DISTORTION vs. FREQUENCY

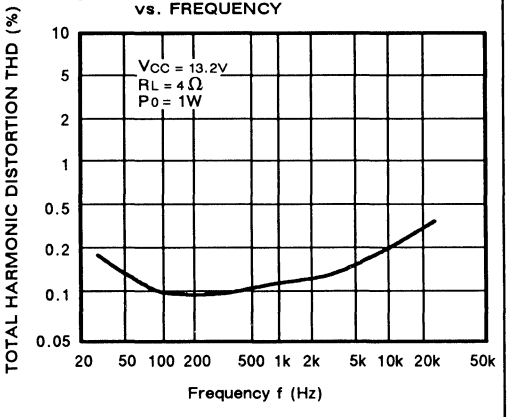


Fig. 8 - POWER DISSIPATION vs. TEMPERATURE

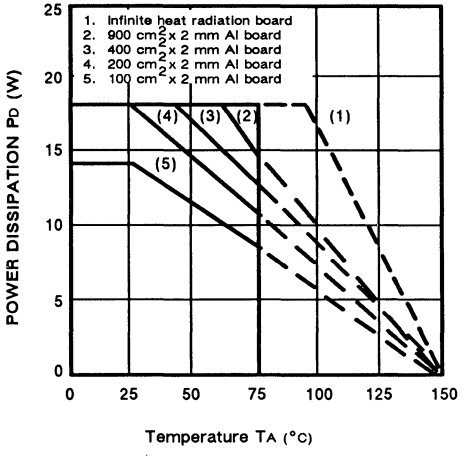
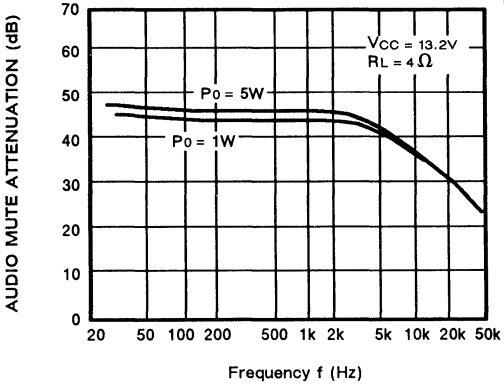
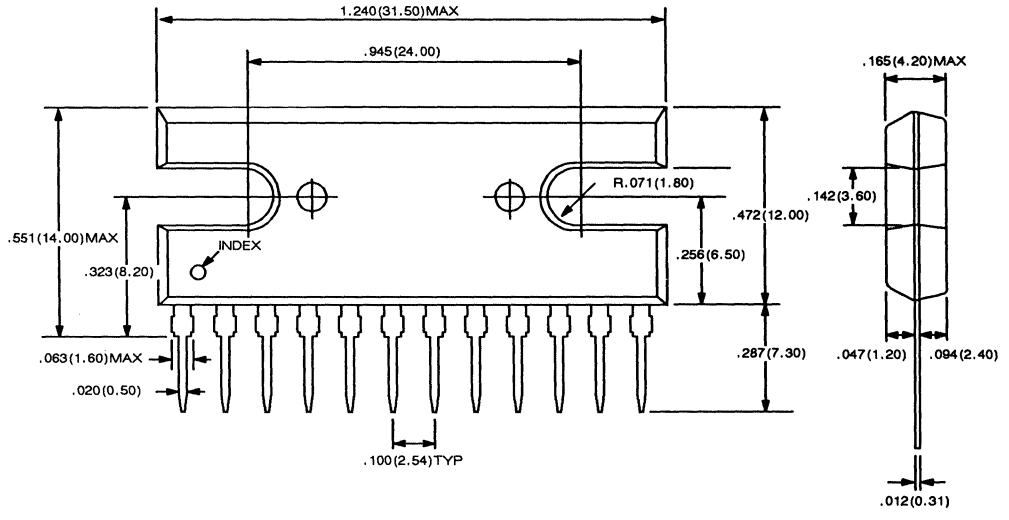


Fig. 9 - AUDIO METU ATTENUATION vs. FREQUENCY



PACKAGE DIMENSION

12-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE NO.: SIP-12P-M01)



Dimensions in
inches (millimeters)

S12001S-3C

FUJITSU

14W BTL AUDIO POWER AMPLIFIER

MB3732
MB3734

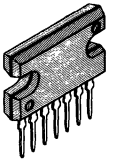
July 1988
Edition 2.0

14W BTL AUDIO POWER AMPLIFIER

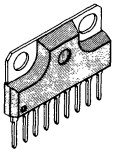
The Fujitsu MB3732 and MB3734 are low-frequency high-power amplifiers with internal BTL (Bridged Output Trans Former-less) circuitry. Suitable for car stereos, the MB3732 and the MB3734 are packed in small plastic packages which have low thermal resistance. Designing for heat radiation can be executed at a low cost. The devices require few external components, so high density mounting is optimized.

The MB3732 and MB3734 comprise various protection functions, including an internal power-on pop noise reduction circuit.

- High power output : 14W typical
- Small plastic package : 7-pin SIP for the MB3732
  9-pin SIP for the MB3734
- Minimum external components
- Low thermal resistance : 3°C/W in the MB3732
  4°C/W in the MB3734
- On-chip power-on pop noise reduction circuit
- No breakdown : between pins is shorted or insertion is inverted
- Low distortion : THD = 0.07% typical
- Various protection circuits:
  Power supply surge protection, Thermal protection
  Load short protection, Over voltage protection
  Output pin-to-DC short protection

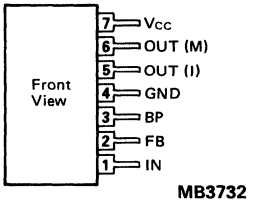


PLASTIC PACKAGE
SIP-07P-M01

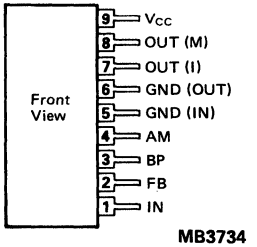


PLASTIC PACKAGE
SIP-09P-M02

PIN ASSIGNMENT



MB3732



MB3734

ABSOLUTE MAXIMUM RATINGS (see NOTE) (T_C = 25°C)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	18	V
Supply Voltage (Surge)	V_{CCS}	50*	V
Output Current (Peak)	I_{OPEAK}	4.5	A
Power Dissipation	P_D	18	W
Operating Temperature (Case)	T_C	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Note: $t_s \leq 0.2$ sec, $t_r \geq 1$ msec

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

Fig. 1 – MB3732 BLOCK DIAGRAM

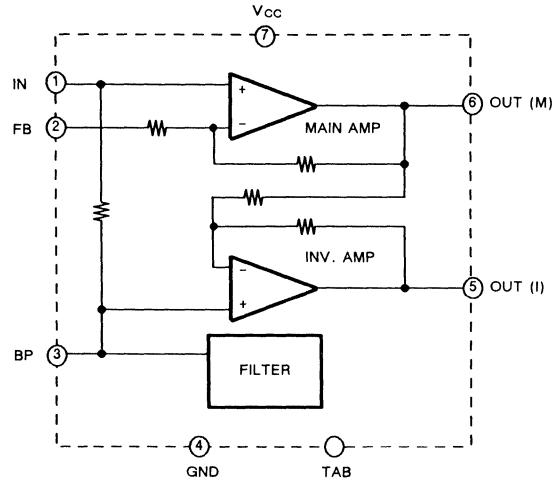
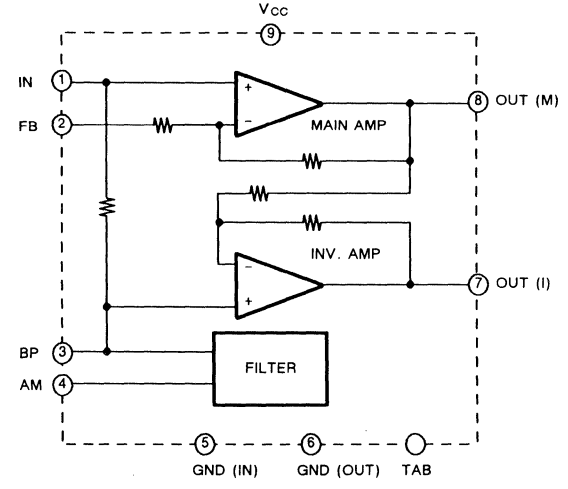


Fig. 2 – MB3734 BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Max	Unit
Power Supply Voltage	V_{CC}	8 to 16	V
Operating Temperature (Case)	T_C	−20 to +75	°C

3

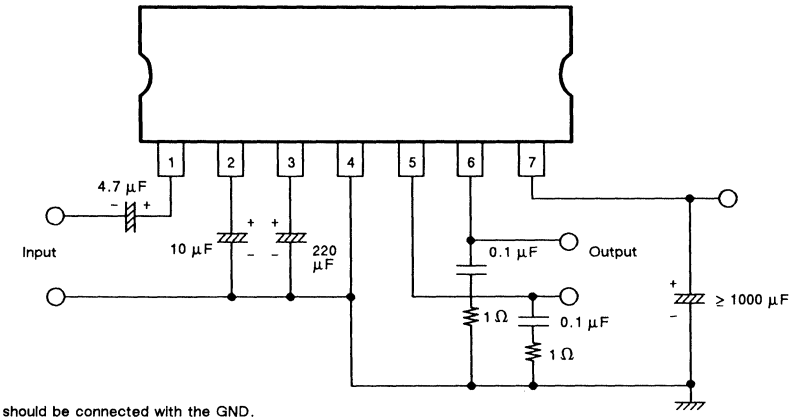
ELECTRICAL CHARACTERISTICS

(T_C = 25°C, V_{CC} = 13.2V, R_L = 4Ω, f = 1KHz)

Parameter	Symbol	Condition	Values			Unit
			Min	Typ	Max	
Quiescent Power Supply Current	I_Q	V_{IN} = 0V R_L = ∞	–	80	160	mA
Voltage Gain	A_V	–	45	47	49	dB
Output Power	P_O	THD = 10%	10	14	–	W
		THD = 1%	–	10	–	
Total Harmonic Distortion	THD	P_O = 1W	–	0.07	0.5	%
Output Noise Voltage	V_{NO}	R_g = 0Ω BW = 20Hz to 20KHz	–	0.3	–	mV
		R_g = 10KΩ BW = 20Hz to 20KHz	–	0.5	1.0	
Input Resistance	R_{IN}	–	20	30	–	kΩ
Output Offset Voltage	V_{OFF}	–	–	±0.1	±0.3	V
DC Mute Supply Current	I_{CCQ}	V_{3pin} = 0V	–	15	–	mA
Audio Mute Attenuation	–	MB3734 Only	–	60	–	dB

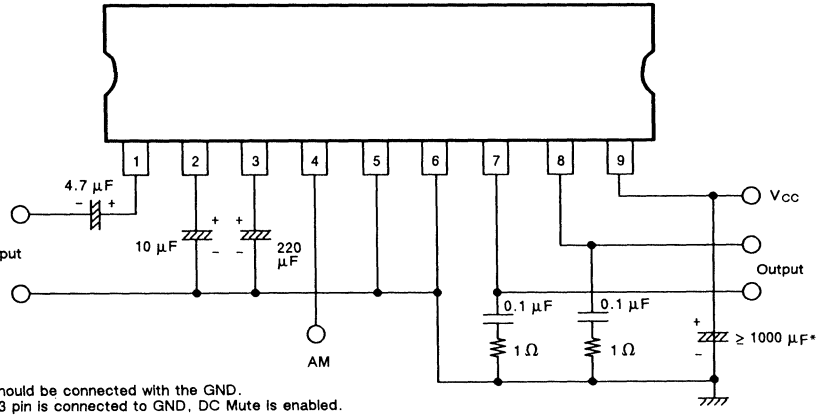
3

Fig. 3 – MB3732 TEST CIRCUIT



TAB should be connected with the GND.

Fig. 4 – MB3734 TEST CIRCUIT



TAB should be connected with the GND.
If the 3 pin is connected to GND, DC Mute is enabled.

NOTE: *When operation is unstable due to board design, insert 0.1 F condenser between V_{CC} and GND and between both outputs respectively, so that the unstable operation will be restrained.

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 5 – TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

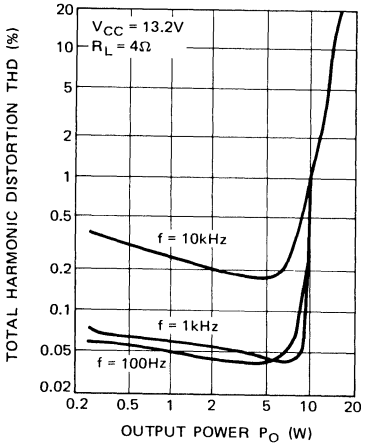


Fig. 6 – TOTAL HARMONIC DISTORTION vs. FREQUENCY

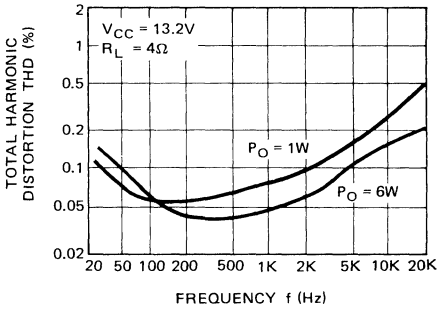


Fig. 7 – OUTPUT POWER vs. FREQUENCY

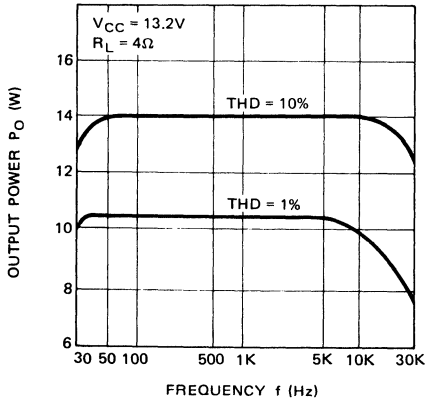
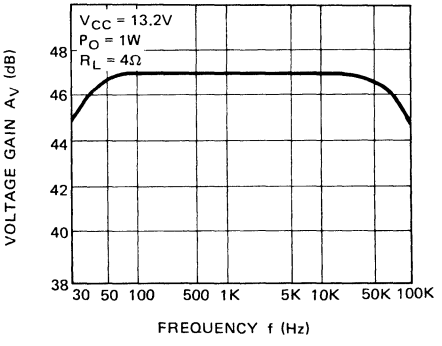


Fig. 8 – VOLTAGE GAIN vs. FREQUENCY



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

3

Fig. 9 – POWER DERATING CURVE
(MB3732)

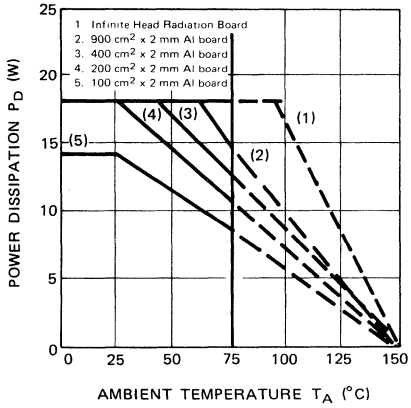
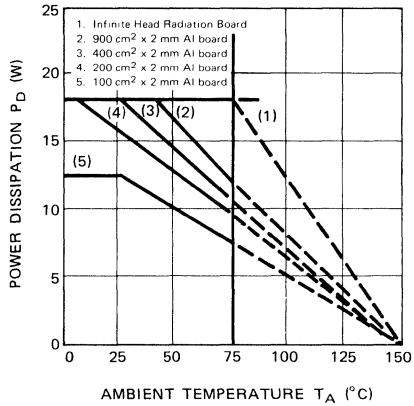


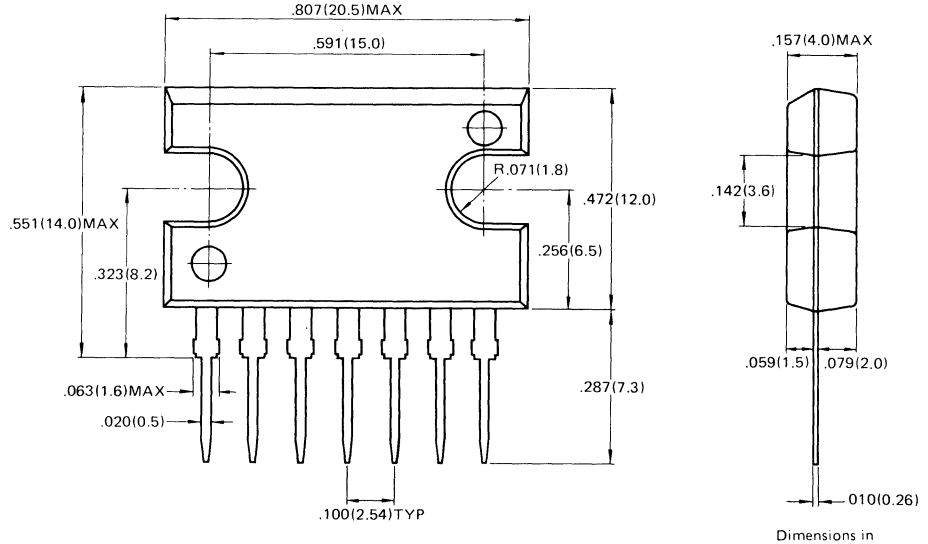
Fig. 10 – POWER DERATING CURVE
(MB3734)



3

PACKAGE DIMENSIONS

7-LEAD PLASTIC SINGLE-IN-LINE PACKAGE
(CASE No.: SIP-07P-M01)

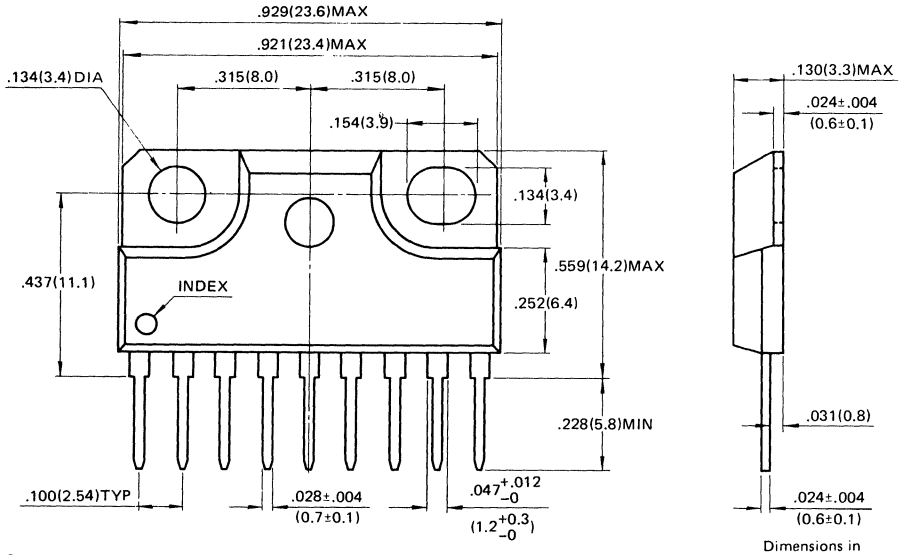


Dimensions in
inches (millimeters)

3

PACKAGE DIMENSIONS (continued)

9-LEAD PLASTIC SINGLE-IN-LINE PACKAGE
(CASE No.: SIP-09P-M02)



Dimensions in
inches (millimeters)

FUJITSU

20 WATT BTL AUDIO POWER AMPLIFIER

MB3733

April 1988
Edition 2.0

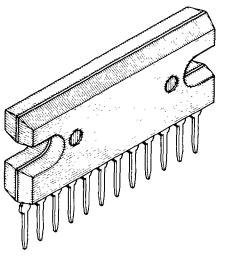
20 WATT BTL AUDIO POWER AMPLIFIER

The Fujitsu MB3733 is designed for a low-frequency high power amplifier with internal BTL (Balanced Transformer less) circuitry. Suitable for care stereos, the MB3733 is packed in a small plastic 12-pin Single In-Line Package (SIP) which has low thermal resistance. Designing for heat radiation can be executed easily.

The device requires few external components, so high density mounting is optimized.

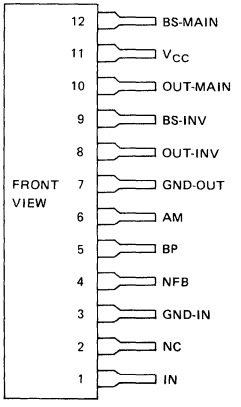
The MB3733 contains a filtering circuitry for power-on pop noise and various protection circuits.

- High Power Output: 20W with $R_L = 4\Omega$
- Minimum External Components
- Samll Plastic 12-pin Single In-Line Package
- Low Thermal Resistance
- Various Protection Circuitries:
  - Power Supply Surge Protection
  - Excess Voltage Protection
  - Load Short Protection
  - DC Short Protection for Outputs, Power Supply pin, and Ground pin
- Low Power-on Pop Noise
- Separated Ground pins for Input/Output
- Audio Mute Function
- Low Total Harmonic Distortion: 0.07% typ.



PLASTIC PACKAGE
SIP-12P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	18	V
Power Supply Voltage (Surge Voltage)	V_{CCS}	50*	V
Peak Output Current	I_O (Peak)	4.5	A
Power Dissipation	P_D	18	W
Operating Temperature (Case)	T_C	−20 to +75	°C
Storage Temperature	T_{STG}	−55 to +150	°C

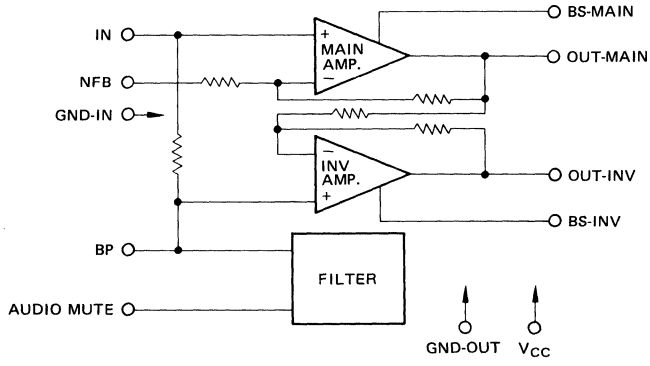
NOTE: * $t_s \leq 0.2$ (s), $t_r \geq 1$ (ms)

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

Fig. 1 – MB3733 BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8 to 16	V
Operating Temperature (Case)	T_C	-20 to +75	°C

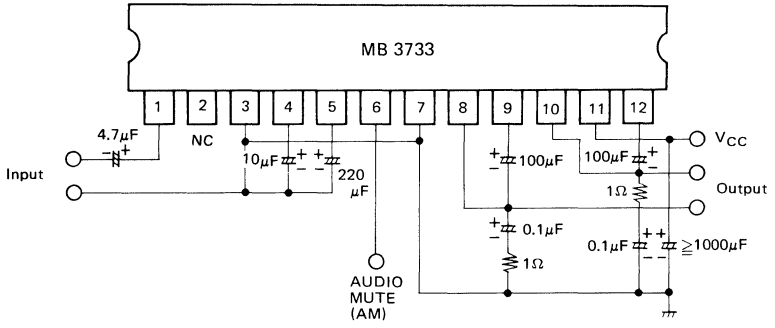
3

ELECTRICAL CHARACTERISTICS

(T_C = 25°C, V_{CC} = 13.2V, R_L = 4Ω, f = 1kHz)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
Quiescent Power Supply Current	V_{IN} = 0V, R_L = ∞	I_Q		80	160	mA
Voltage Gain		A_V	45	47	49	dB
Output Power	THD = 10%	P_{O1}	16	20		W
	THD = 1%	P_{O2}		14		W
Total Harmonic Distortion	P_O = 1W	THD		0.07	0.5	%
Output Noise Voltage	R_g = 0Ω, BW = 20 to 20kHz	V_{NO1}		0.3		mV
	R_g = 10kΩ, BW = 20 to 20kHz	V_{NO2}		0.5	1.0	mV
Input Resistance		R_{IN}	20	30		kΩ
Output Offset Voltage		V_{OFFSET}		±0.1	±0.3	V
Supply Current in DC MUTE mode	BP = 0V	I_{CCQ}		15		mA
AUDIO MUTE Attenuation	AM = 0V			50		dB

Fig. 2 – MEASUREMENT CIRCUIT



Note: When BP is grounded, DC Muting can be used. When AM is grounded, AUDIO Muting can be used.

3

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

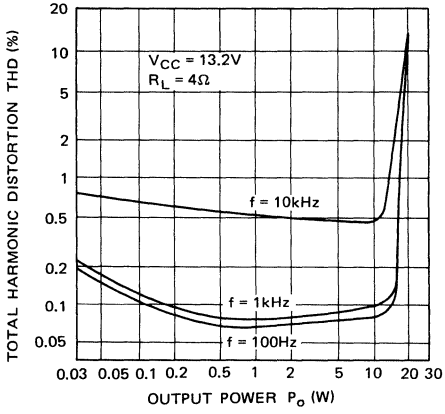


Fig. 4 – TOTAL HARMONIC DISTORTION vs. FREQUENCY

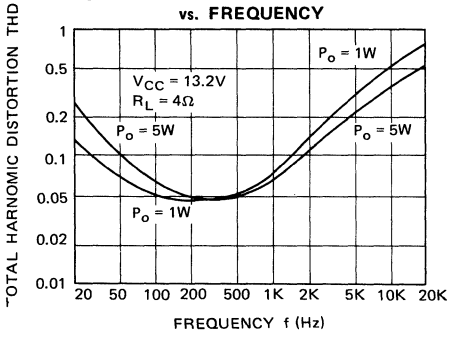


Fig. 5 – VOLTAGE GAIN vs. FREQUENCY

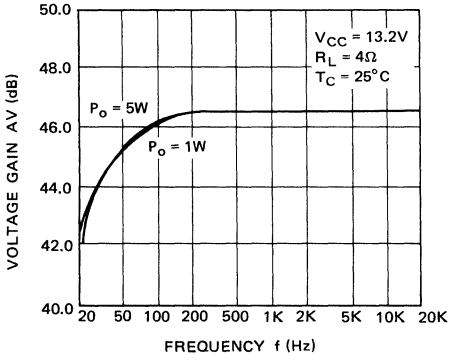


Fig. 6 – OUTPUT POWER vs. FREQUENCY

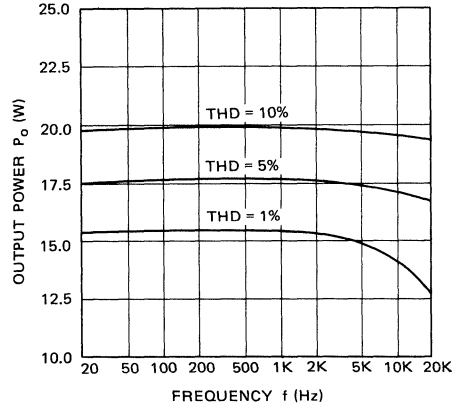


Fig. 7 – POWER DISSIPATION/POWER SUPPLY CURRENT vs. OUTPUT POWER

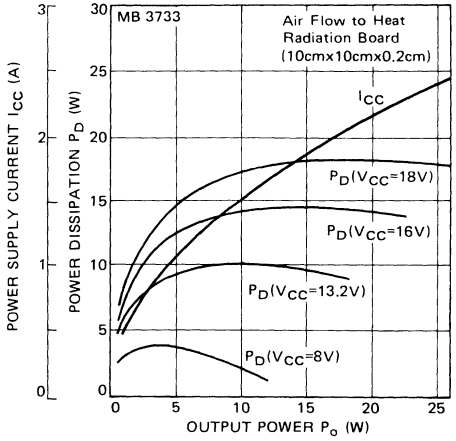
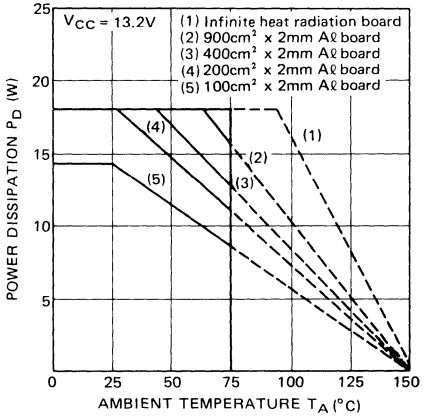


Fig. 8 – POWER DERATING CURVES



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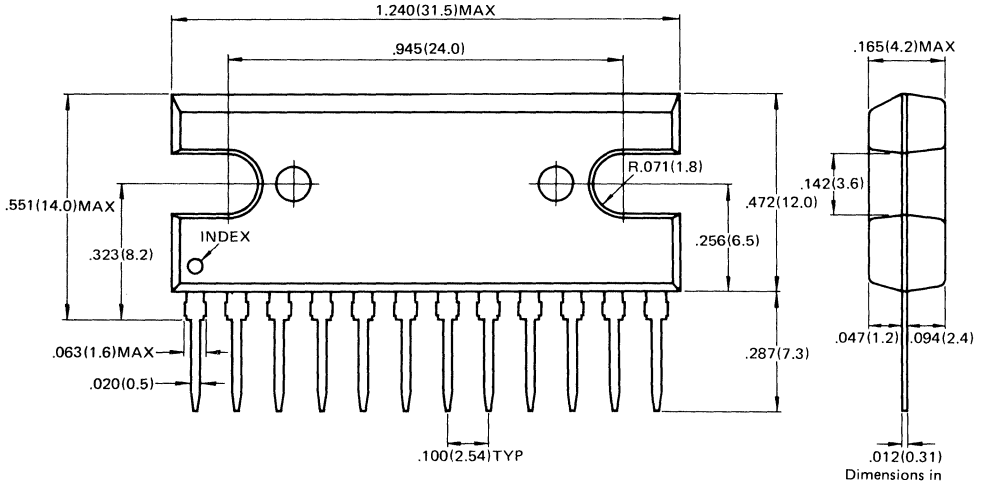
PACKAGE DIMENSIONS

12-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE NO.: SIP-12P-M01)



Dimensions in inches (millimeters)

FUJITSU

20 WATT BTL AUDIO POWER AMPLIFIER

MB 3735

April 1987
Edition 2.0

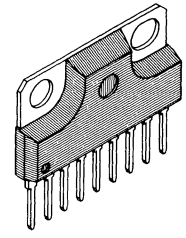
20 WATT BTL AUDIO POWER AMPLIFIER

The Fujitsu MB 3735 is designed for a low-frequency high-power amplifier with internal BTL (Balanced Transformer less) circuitry. The MB 3735 is packed in a small plastic 9-pin Single In-Line Package (SIP) which has low thermal resistance, so that a deseign for heat radiation can be performed with low cost.

Also, the MB 3735 requires such a few external components, so that it can be mounted on printed circuit board with high density.

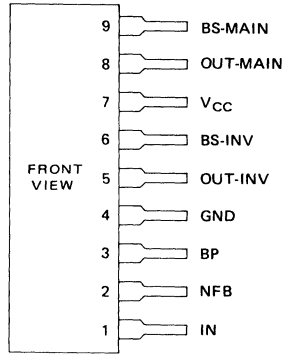
The MB 3735 contains a filtering circuitry for power-on pop noise and various protection circuits.

- High Power Output: 20W with $R_L = 4\Omega$
- Minimum External Components
- Small Plastic 9-pin Single In-Line Package
- Low Thermal Resistance
- Various Protection Circuitries:
  - Power Supply Surge Protection
  - Excess Voltage Protection
  - Load Short Protection
  - DC Short Protection for Outputs, Power Supply pin, and Ground pin
- Low Power-on Pop Noise



PLASTIC PACKAGE
SIP-09P-M02

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	18	V
Power Supply Voltage (Surge Voltage)	V_{CCS}	50*	V
Peak Output Current	$I_{O\,(Peak)}$	4.5	A
Power Dissipation	P_D	18	W
Operation Temperature	T_C	−20 to +75	°C
Storage Temperature	T_{STG}	−55 to +150	°C

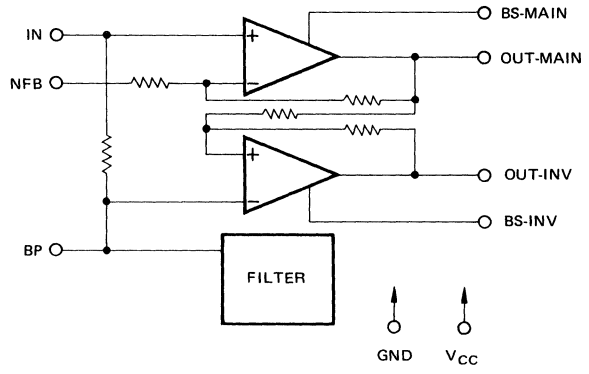
NOTE: * $t_s \leq 0.2$ (s), $t_r \geq 1$ (ms)

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

Fig. 1 – BLOCK DIAGRAM of MB 3735



RECOMMENDED OPERATING CONDITIONS

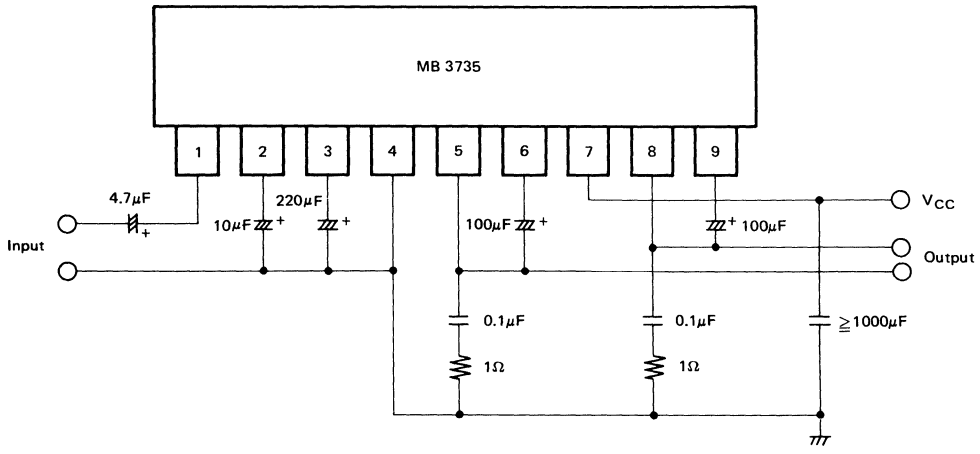
Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8 to 16	V
Case Temperature	T_C	–20 to +75	°C

ELECTRICAL CHARACTERISTICS

(T_C = 25°C, V_{CC} = 13.2V, R_L = 4Ω, f = 1kHz)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
Quescent Power Supply Current	V_{IN} = 0V, R_L = ∞	I_Q		80	160	mA
Voltage Gain		A_V	45	47	49	dB
Output Power	THD = 10%	P_{O1}	16	20		W
	THD = 1%	P_{O2}		14		W
Total Harmonic Distortion	P_O = 1W	THD		0.07	0.5	%
Output Noise Voltage	R_g = 0Ω, BW = 20 Hz to 20 kHz	V_{NO1}		0.3		mV
	R_g = 10kΩ BW = 20 Hz to 20 kHz	V_{NO2}		0.5	1.0	mV
Input Resistance		R_{IN}	20	30		kΩ
Output Offset Voltage		V_{OFFSET}		±0.1	±0.3	V
Supply Current in DC MUTE mode	BP = 0V	I_{CCO}		15		mA

Fig. 2 – MEASUREMENT CIRCUIT



Note: When BP is grounded, DC Muting can be used.

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

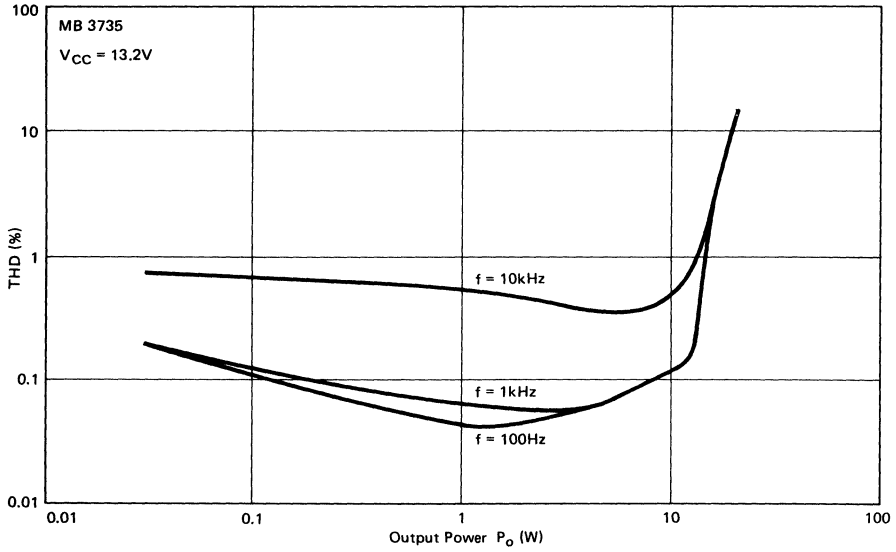


Fig. 4 – TOTAL HARMONIC DISTORTION vs. FREQUENCY

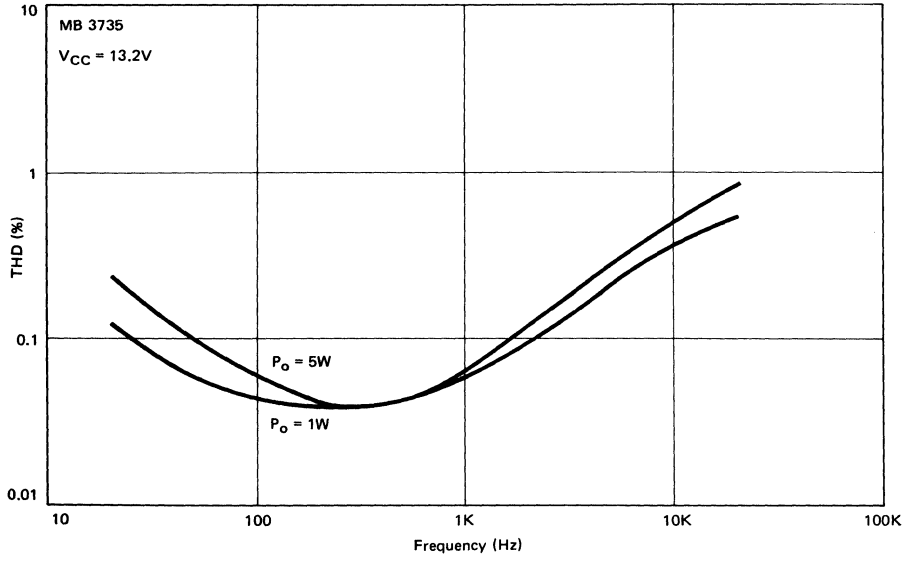


Fig. 5 – GAIN vs. FREQUENCY

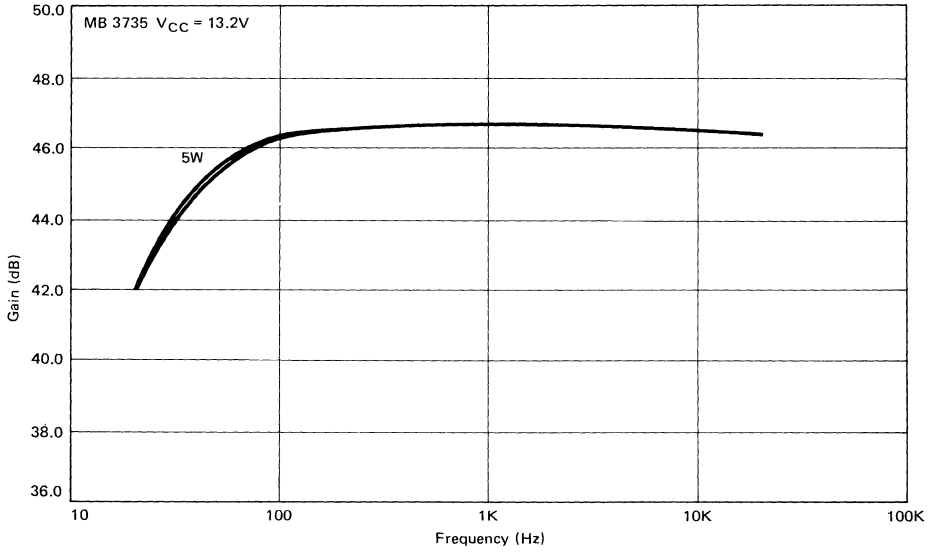
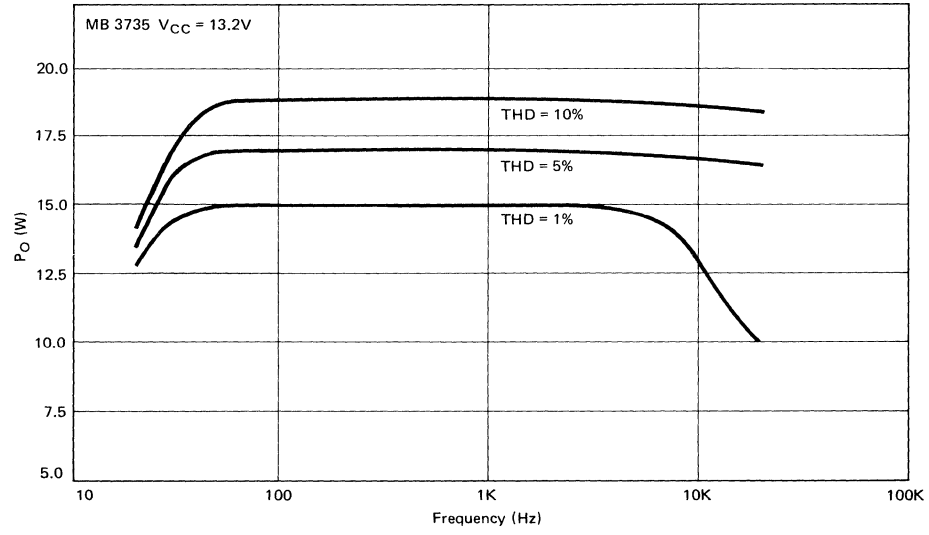


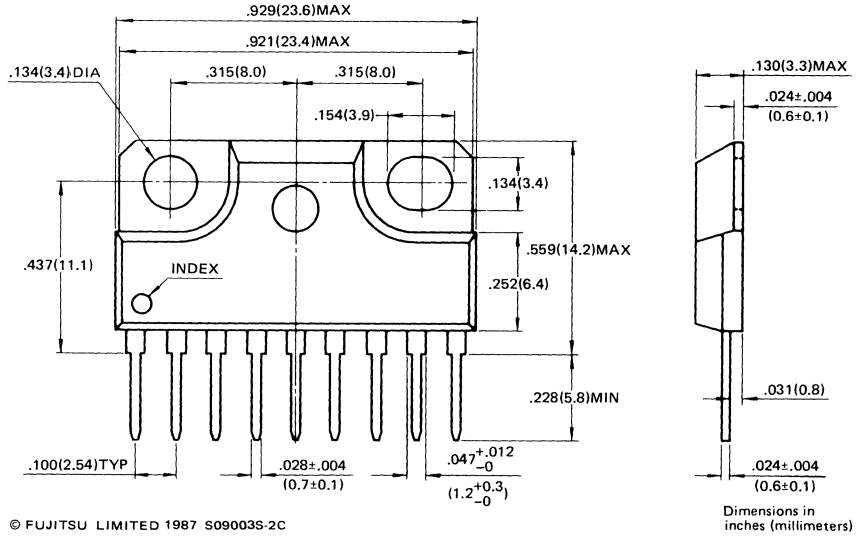
Fig. 6 – POWER BAND WIDTH



3

PACKAGE DIMENSIONS

9-LEAD PLASTIC SINGLE-IN-LINE PACKAGE
(CASE No.: SIP-09P-M02)



Dimensions in
inches (millimeters)

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MB3736
15W BTL AUDIO AMPLIFIER

15W BTL AUDIO AMPLIFIER WITH INTERNAL STAND BY FUNCTION

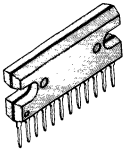
The Fujitsu MB3736 is designed for a low-frequency high-power amplifier with internal BTL (Balanced Transformer Less) circuitry.

Suitable for car stereos, the MB3736 is packed in 12 pin plastic Single in line small packaage or 12 pin plastic Zigzag in line small package which has low thermal resistance (SIP: 3°C/W, ZIP: 4°C/W). Design for heat radiation can be executed easily.

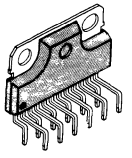
The MB3736 requires few external components, so high density mounting is optimized.

The MB3736 contains a power-on pop noise protection circuitry and various protection circuitry.

- High Output Power : 15W typ at 4Ω
- Minimum External Components (OCL, 5 capacitors, 2 resistors)
- Stand-by Function (TTL Drive)
- Various Protection Circuitry
  - Power Supply Surge Protection
  - Output pin-to DC Short Protection
  - Over Voltage Protection
  - Load Short Protection
  - Thermal Protection
- Low Power-on Pop Noise
- Package
  - 12 pin Plastic SIP package (Suffix: -PS)
  - 12 pin Plastic SIP package (Suffix: -PSZ)

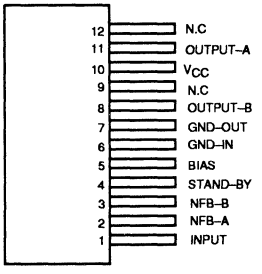


PLASTIC PACKAGE
SIP-12P-M01



PLASTIC PACKAGE
ZIP-12P-M01

PIN ASSIGNMENT
(Front View)



(SIP-12P-M01)
ZIP pin assignment:
Please see page 7

ABSOLUTE MAXIMUM RATINGS (see NOTE) (T_C = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	18	V
Power Supply Voltage (Surge)	V_{CCS}	50*	V
Output Current (Peak)	I_{OPEAK}	4.5	A
Power Dissipation	P_D	30	W
Operating Temperature (Case)	T_C	-20 to + 75	°C
Storage Temperature	T_{STG}	-55 to + 150	°C

*$T_S \leq$ 0.2 sec, $T_r \leq$ 1 msec

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

Fig. 1 — MB3736 BLOCK DIAGRAM

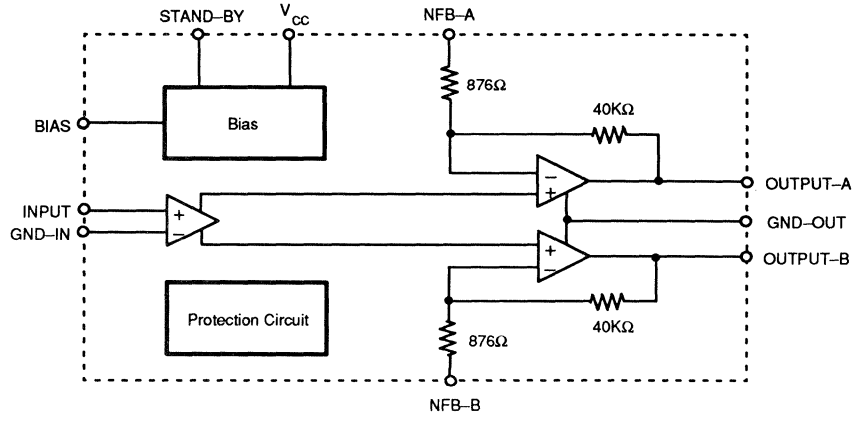
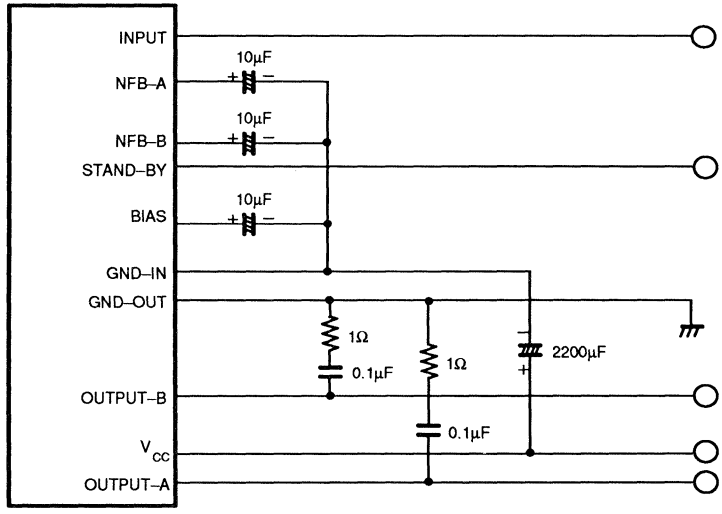


Fig. 2 – MB3736 CONNECTION EXAMPLE



RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	9 to 16	V
Operating Temperature (Case)	T_C	–20 to + 75	°C

ERECTRICAL CHARACTERISTICS

(T_C = 25°C, V_{CC} = 13.2V, f = 1 kHz, R_L = 4Ω)

Parameter	Symbol	Condition		Value			Unit
				Min	Typ	Max	
Quiescent Power Supply Current	I_{CCQ}	V_{IN} = 0V , R_L = ∞			100	200	mA
Voltage Gain	A_V			43	45	47	dB
Output Power	P_O	THD = 10%	R_L = 4Ω	12	15		W
			R_L = 2Ω	12	23		
Total Harmonic Distortion	THD	P_O = 5W			0.04	0.4	%
Output Noise Voltage	V_{NO}	R_g =10 kΩ, BW = 20Hz to 20kHz			0.4	1.0	m V
Input Resistance	R_{IN}			20	30		KΩ
Output Offset Voltage	V_{OFF}				± 0.1	± 0.3	V
Power Supply Current at Stand by mode	I_{CCS}				1	50	μA
Input Voltage, Stand–by Pin	V_{SBH}	Operating mode		2.4		V_{CC}	V
	V_{SBL}	Stand–by mode		0		0.4	V
Ripple Rejection Ratio	RR	Vrip = 1Vrms, f = 1kHz (1 μF is connected between V_{CC} and GND)		40	50		dB

3

TYPICAL CHARCTERISTICS CURVES

Fig. 3 – TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

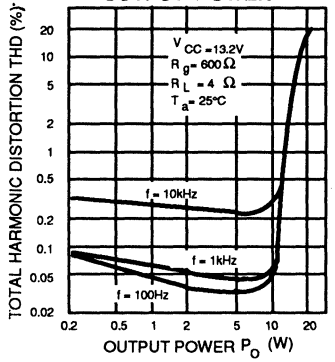


Fig. 4 – TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

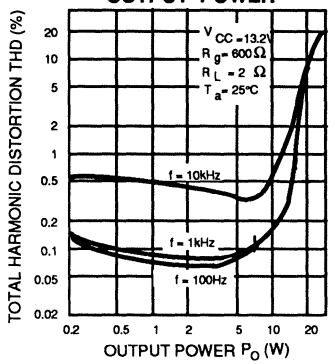


Fig. 5 – TOTAL HARMONIC DISTORTION vs. FREQUENCY

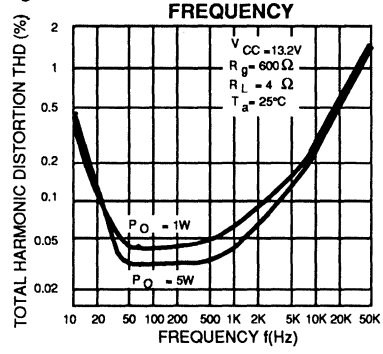


Fig. 6 – VOLTAGE GAIN vs. FREQUENCY

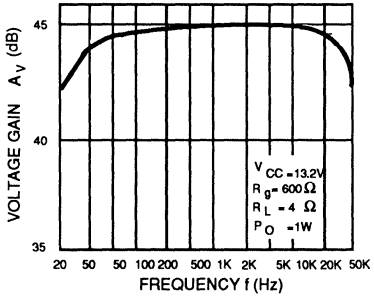


Fig. 7 – OUTPUT POWER vs. FREQUENCY

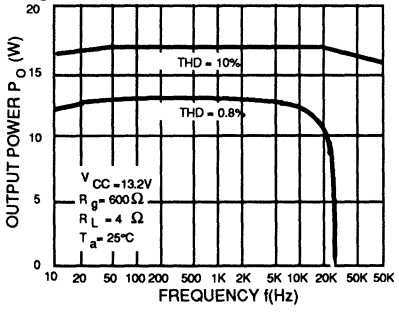


Fig. 8 – TOTAL HARMONIC DISTORTION vs. SIGNAL SOURCE IMPEDANCE

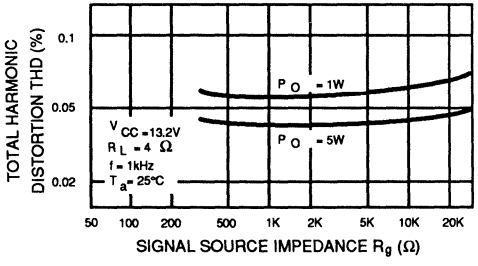


FIG.9 – OUTPUT NOISE VOLTAGE vs. SIGNAL SOURCE IMPEDANCE

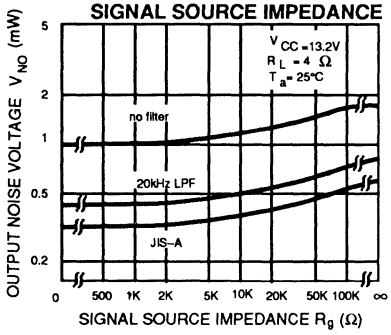


Fig. 10 – RIPPLE REJECTION vs. FREQUENCY

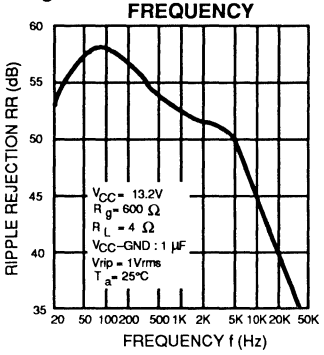


FIG.11 – POWER SUPPLY CURRENT/ POWER DISSIPATION vs. OUTPUT POWER

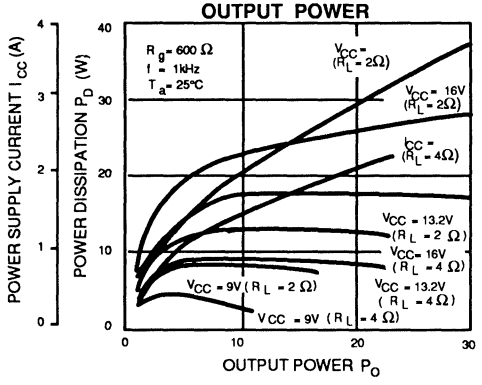


Fig. 12 – OUTPUT POWER vs. LOAD RESISTANCE

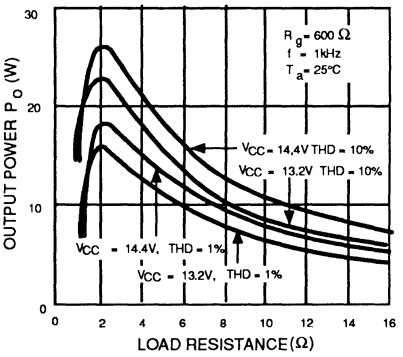


Fig. 13 – OUTPUT POWER vs. FREQUENCY

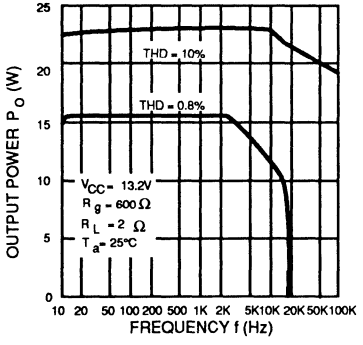
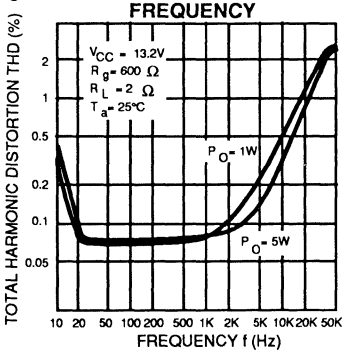
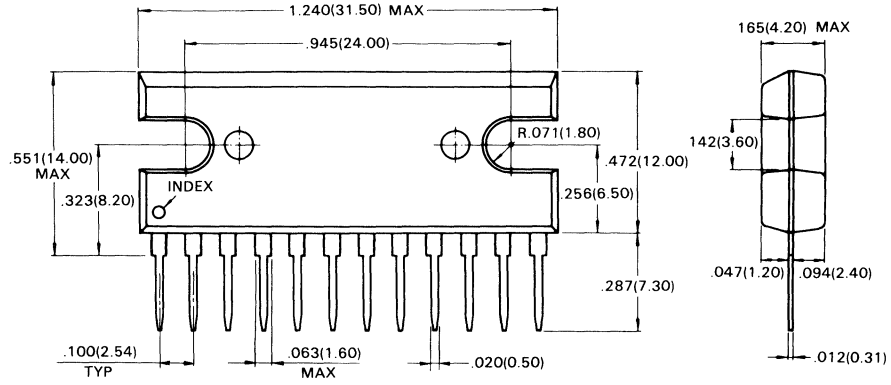


Fig. 14 – TOTAL HARMONIC DISTORTION FREQUENCY



PACKAGE DIMENSIONS

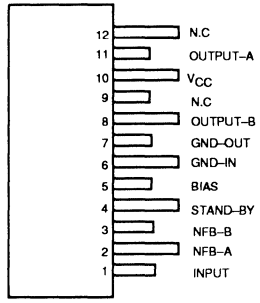
12-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(Case No.: SIP-12P-M01)



Dimensions in
inches (milimeters)

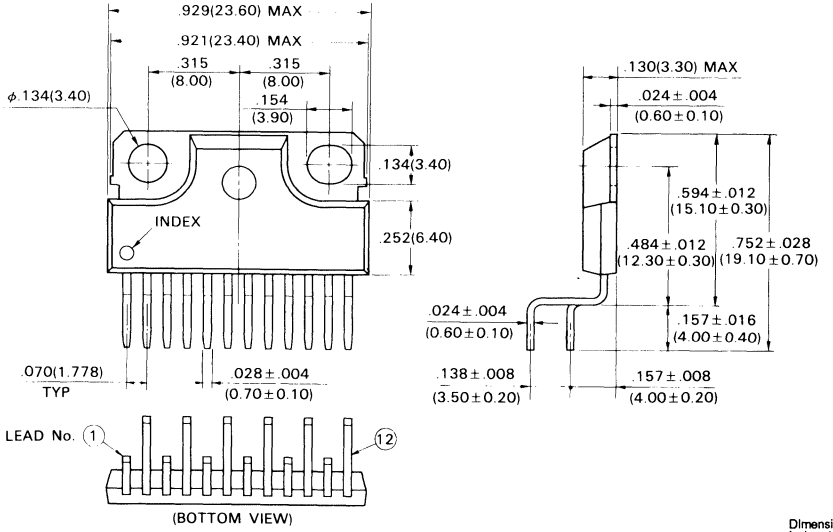
PACKAGE DIMENSIONS (Continued)

PIN ASSIGNMENT
(TOP VIEW)



(ZIP–12P–M01)

12–LEAD PLASTIC ZIG–ZAG IN–LINE PACKAGE
(Case No.: ZIP–12P–M01)



Dimensions in inches (milimeters)

3

October 1989
Edition 1.0

FUJITSU

DATA SHEET

MB3737A
23 W BTL AUDIO POWER AMPLIFIER

23 W BTL AUDIO POWER AMPLIFIER

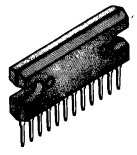
The Fujitsu MB3737A is designed for a low-frequency high-power amplifier with internal BTL (Bridged Output Transformer-less) circuitry.

Suitable for car stereos, the MB3737A is packed in 12 pin plastic Single in line package or 12 pin plastic Zigzag in line package which has low thermal resistance (SIP: 3°C/W, ZIP: 4°C/W). Design for heat radiation can be executed easily.

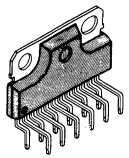
The MB3737A requires few external components, so high density mounting is optimized.

The MB3737A contains a power-on pop noise protection circuitry and various protection circuitry.

- High Output Power : 15W typ at 4Ω
- Minimum External Components
- Stand-by Function
- Various Protection Circuitry
  - Power Supply Surge Protection
  - Output pin-to DC Short Protection
  - Over Voltage Protection
  - Load Short Protection
  - Thermal Protection
- Low Power-on Pop Noise
- Package
  - 12 pin Plastic SIP package (Suffix: -PS)
  - 12 pin Plastic ZIP package (Suffix: -PSZ)

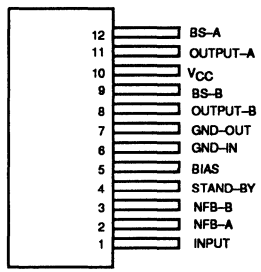


PLASTIC PACKAGE
SIP-12P-M01



PLASTIC PACKAGE
ZIP-12P-M01

PIN ASSIGNMENT
(Front View)



(SIP-12P-M01)

ZIP pin assignment:
Please see page 7

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE) (T_C = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	18	V
Power Supply Voltage (Surge)	V_{CCS}	50 *	V
Output Current (Peak)	I_{OPEAK}	4.5	A
Power Dissipation	P_D	30	W
Operating Temperature (Case)	T_C	-20 to + 75	°C
Storage Temperature	T_{STG}	-55 to + 150	°C

* $t_s \leq 0.2$ sec, $t_r \geq 1$ msec

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 — MB3737A BLOCK DIAGRAM

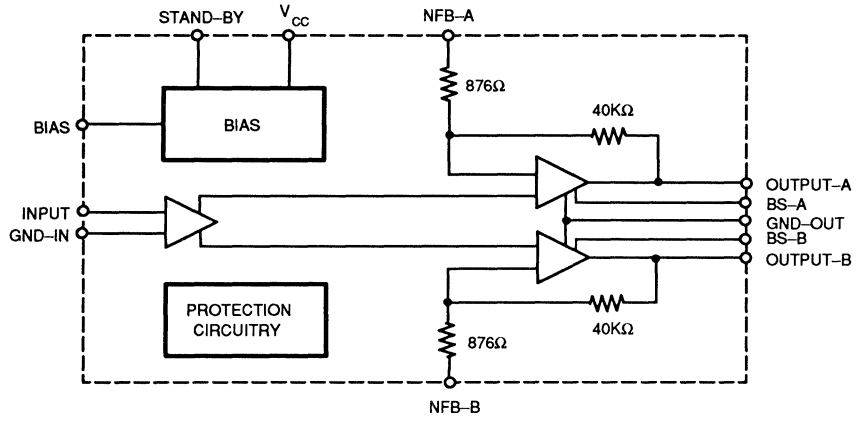
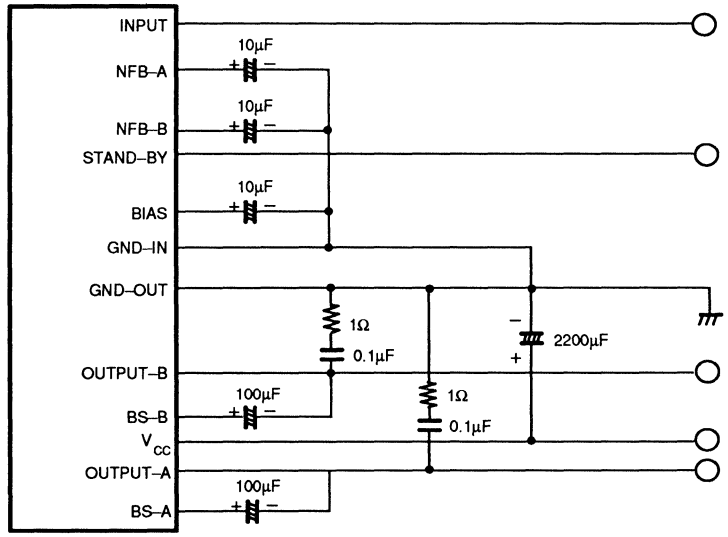


Fig. 2 – MB3737A TYPICAL CONNECTION EXAMPLE



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	9 to 16	V
Operating Temperature (Case)	T_C	–20 to + 75	°C

ERECTRICAL CHARACTERISTICS

(T_C = 25° C, V_{CC} = 13.2V, f = 1 kHz, R_L = 4Ω)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Quiescent Power Supply Current	I_{CCQ}	V_{IN} = 0V , R_L = ∞		100	200	mA
Voltage Gain	A_V		43	45	47	dB
Output Power	P_O	THD = 10%, R_L = 4Ω	18	23		W
		THD = 10%, R_L = 2Ω	18	26		W
Total Harmonic Distortion	THD	P_O = 5W		0.04	0.4	%
Output Noise Voltage	V_{NO}	R_g = 10 kΩ, BW = 20Hz to 20kHz		0.4	1.0	m V
Input Resistance	R_{IN}		20	30		KΩ
Output Offset Voltage	V_{OFF}			± 0.1	± 0.3	V
Power Supply Current at Stand–by mode	I_{CCS}			1	50	μA
Ripple Rejection Ratio	RR	Vrip = 1Vrms, f = 1kHz Capacitor 1μF is connected between V_{CC} and GND	40	50		dB
Input Voltage, Stand–by Pin	V_{SBH}	Operation mode	2.4		V_{CC}	V
	V_{SBL}	Stand–by mode	0		0.4	V

3

TYPICAL CHARACTERISTICS CURVES

Fig. 3 – TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

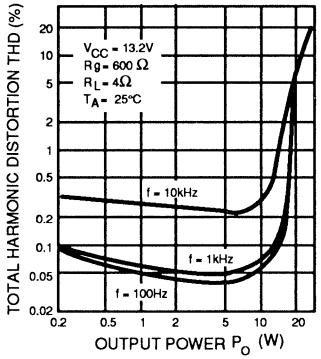


Fig. 4 – TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

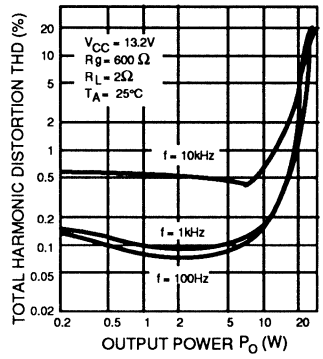


Fig. 5 – TOTAL HARMONIC DISTORTION vs. FREQUENCY

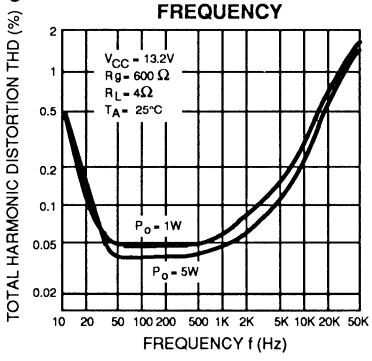


Fig. 6 – VOLTAGE GAIN vs. FREQUENCY

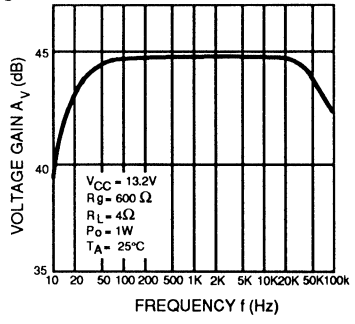


Fig. 7 – OUTPUT POWER vs. FREQUENCY

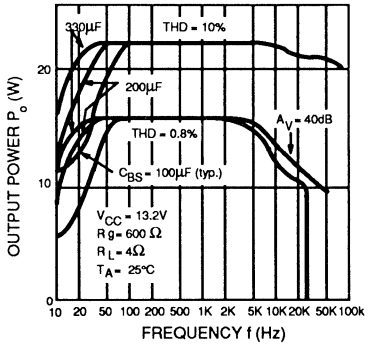
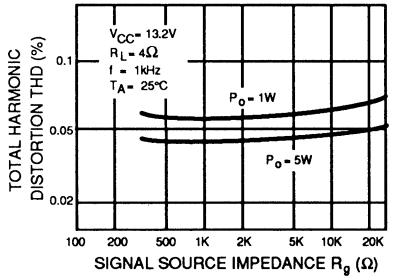


Fig. 8 – TOTAL HARMONIC DISTORTION vs. SIGNAL SOURCE IMPEDANCE



TYPICAL CHARACTERISTICS CURVES (Continued)

Fig. 9 – OUTPUT NOISE VOLTAGE SIGNAL SOURCE IMPEDANCE

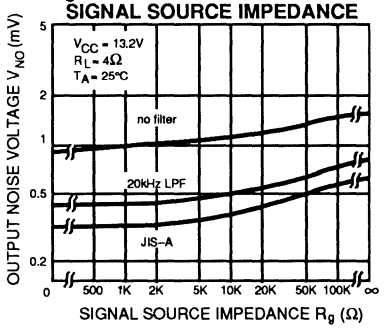


Fig. 10 – RIPPLE REJECTION vs. FREQUENCY

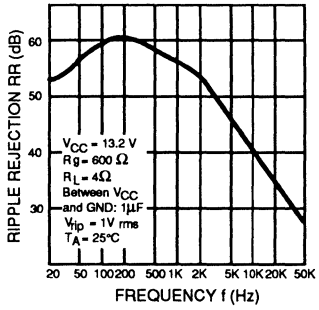


Fig. 11 – POWER SUPPLY CURRENT/POWER DISSIPATION vs. OUTPUT POWER

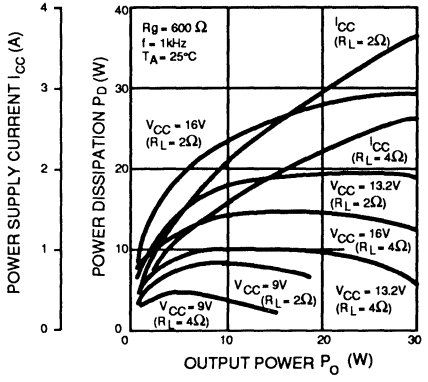


Fig. 12 – OUTPUT POWER vs. LOAD RESISTANCE

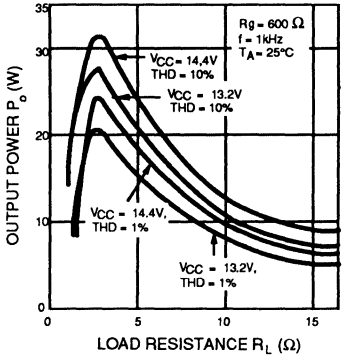


Fig. 13 – OUTPUT POWER vs. FREQUENCY

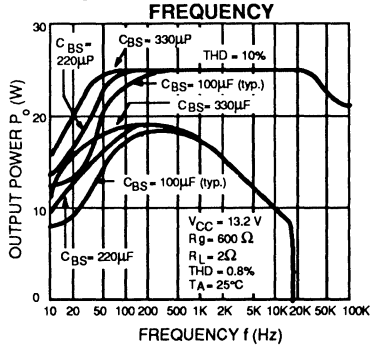
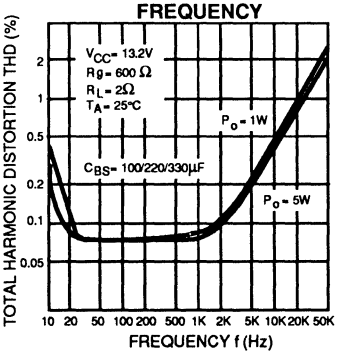
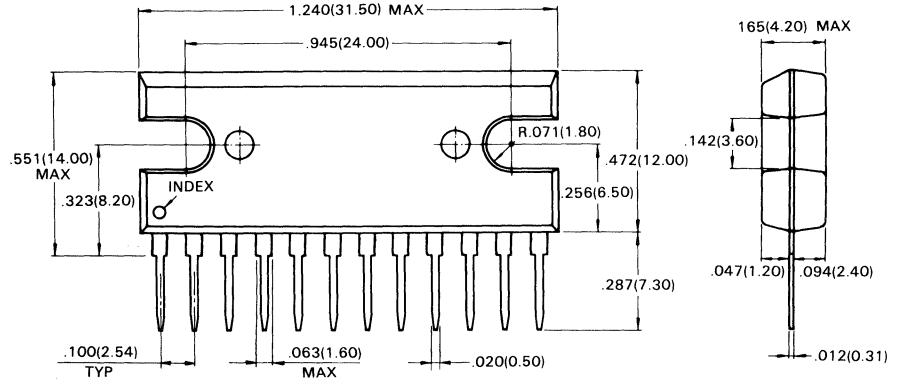


Fig. 14 – TOTAL HARMONIC DISTORTION FREQUENCY



PACKAGE DIMENSIONS

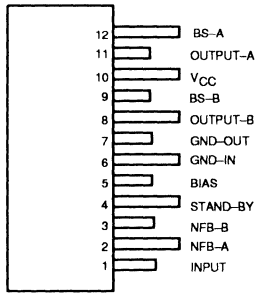
12–LEAD PLASTIC SINGLE IN–LINE PACKAGE
(Case No.: SIP–12P–M01)



Dimensions in
inches (millimeters)

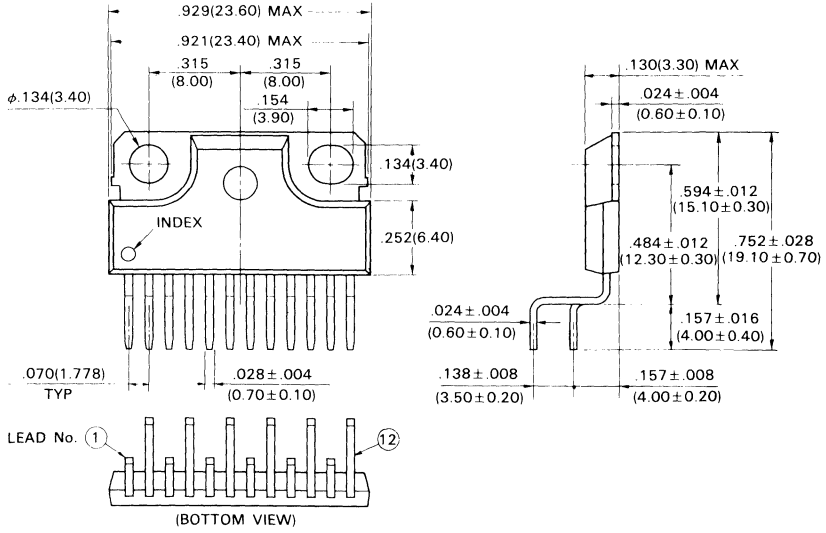
PACKAGE DIMENSIONS (Continued)

PIN ASSIGNMENT
(FRONT VIEW)



(ZIP–12P–M01)

12–LEAD PLASTIC ZIG–ZAG IN–LINE PACKAGE
(Case No.: ZIP–12P–M01)



Dimensions in inches (milimeters)

3

FUJITSU

15W DUAL BTL AUDIO POWER AMPLIFIER

MB3742

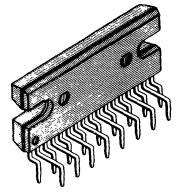
March 1989
Edition 1.0

15W DUAL BTL AUDIO POWER AMPLIFIER

The Fujitsu MB3742 is designed for a low-frequency high-power amplifier with internal BTL (Balanced Transformer Less) circuitry. The MB3742 is packed in 17 pin zig zag in line plastic package and requires a few external components, this enables high density mounting.

The MB3742 is internal power-on pop noise protection circuit and various protection circuits. The device is suitable best for car-stereo.

PRELIMINARY

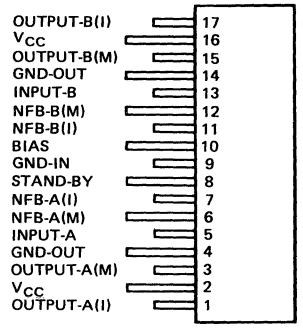


PLASTIC PACKAGE
ZIP-17P-M02

- High Output Power . . . 15W (typ.) x 2 (R_L = 4Ω)
- Small Plastic 17-pin ZIP Package
- Minimum External Components (OCL, C=9, R=4)
- Power Supply Stand-by Mode (1μA typ.)
- Various Protection Circuits
  - Power Supply Surge Voltage Protection
  - Excess Power Supply Voltage Protection
  - DC Short Protection Between Output Terminals
  - Short Protection Between Load And Power Supply/Ground
  - Thermal Shutdown
- Minimum Pop Noise from Power Supply Switching

PIN ASSIGNMENT

(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS (See Note) (T_A = 25°C)

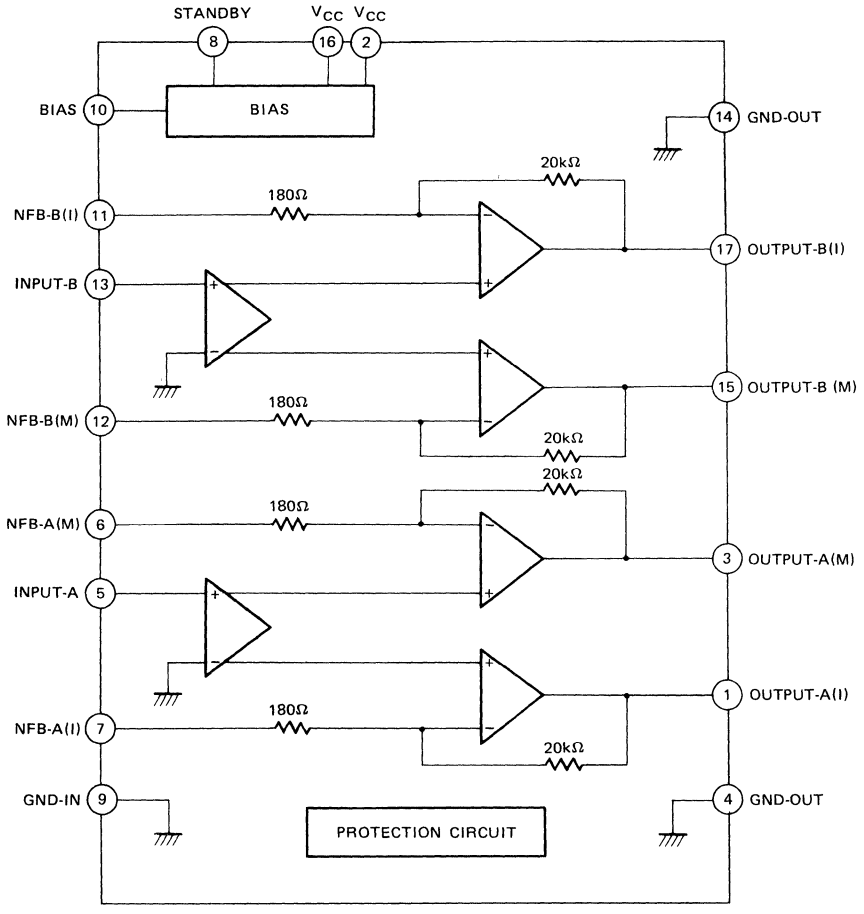
Item	Symbol	Typical Value	Unit
Power Supply Voltage	V_{CC}	18	V
Surge Voltage	$V_{CC(S)}$	50*	
Output Current	$I_{O(PEAK)}$	4.5	A
Power Dissipation	P_D	30	W
Operating Temperature	T_{OP}	−20 to +75	°C
Storage Temperature	T_{STG}	−55 to +150	

*: $t_s \leqq 0.2s$, $t_s \leqq 1ms$

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

CIRCUIT BLOCK



RECOMMENDED OPERATING CONDITIONS

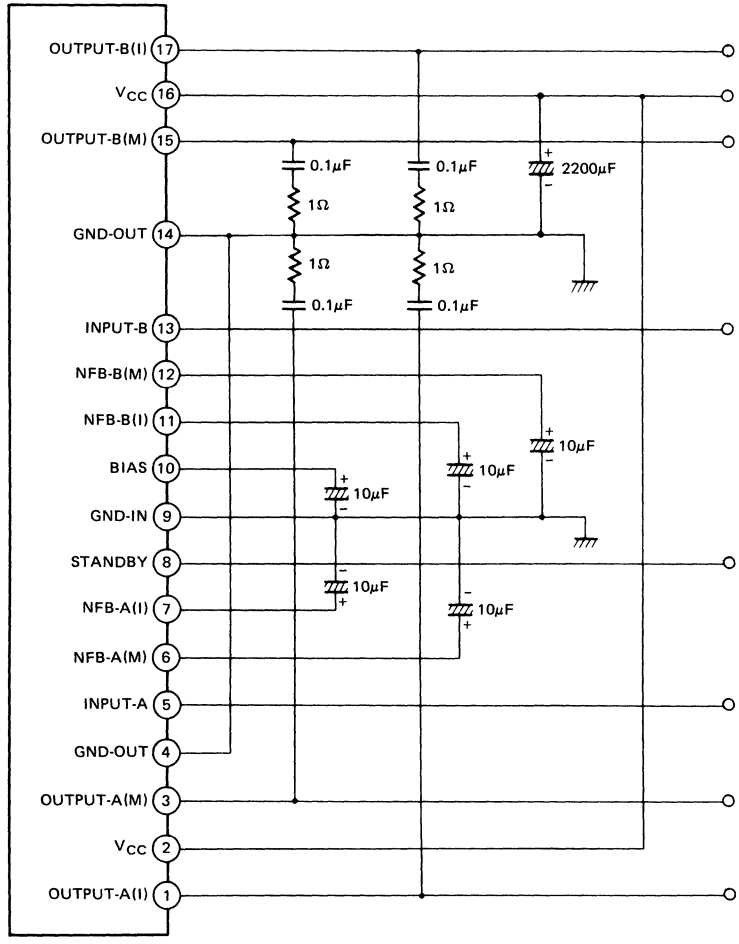
Item	Symbol	Typical Values	Unit
Power Supply Voltage	V_{CC}	9 to 16	V
Operating Temperature	T_{op}	−20 to +75	°C

ELECTRICAL CHARACTERISTICS

(T_C = 25°C, V_{CC} = 13.2V, f = 1kHz, R_L = 4Ω)

Item	Symbol	Conditions	Min	Typ	Max	Unit
Quiescent Power Supply Current	I_{CCQ}	V_{in} = 0V, R_L = ∞		180		mA
Voltage Gain	A_V		51	53	55	dB
Output Power	P_o	THD = 10%		15		W
Total Harmonic Distortion	THD	P_o = 5W		0.07		%
Output Noise Voltage	V_{NO}	R_g = 10kΩ, BW = 20Hz to 20kHz		1.0		mV
Input Resistance	R_{in}		20	30		kΩ
Output Offset Voltage	V_{OFF}			±0.1	±0.3	V
Power Supply Current at Stand-by Mode	Is	8-Pin Open		1		μA
Ripple Rejection Ratio	PSRR			50		dB
Input Voltage to Stand-by Terminal	V_{SBH}	at normal operation	2.4		V_{CC}	V
	V_{SBL}	at standby mode	0		0.4	
Channel Separation	CS	P_o ≒ 1W		60		dB

APPLICATION



TYPICAL CHARACTERISTICS CURVES

Fig. 1 – TOTAL HARMONIC DISTORTION vs. OUTPUT POWER

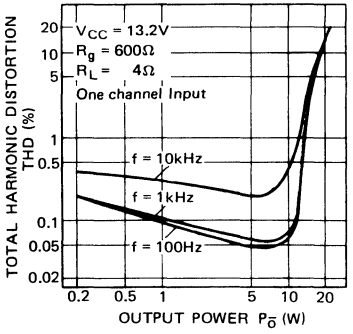


Fig. 2 – TOTAL HARMONIC DISTORTION vs. FREQUENCY

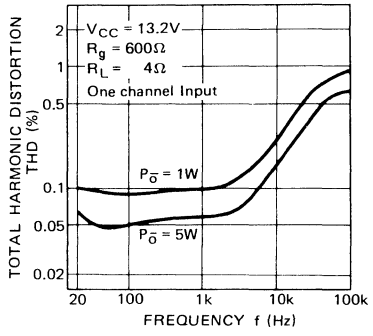


Fig. 3 – VOLTAGE GAIN vs. FREQUENCY

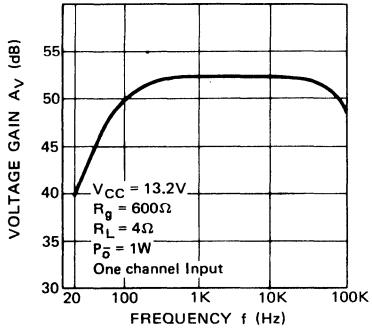


Fig. 4 – OUTPUT POWER vs. FREQUENCY

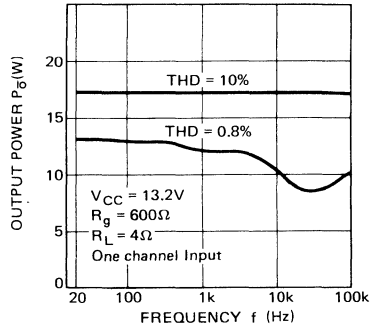
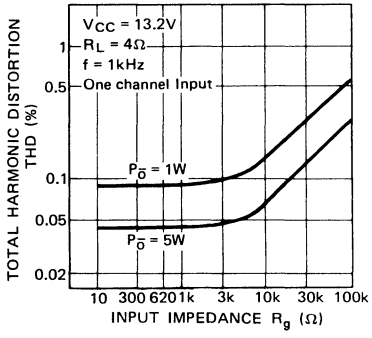


Fig. 5 – TOTAL HARMONIC DISTORTION vs. INPUT IMPEDANCE



3

TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 6 – OUTPUT NOISE VOLTAGE vs. INPUT IMPEDANCE

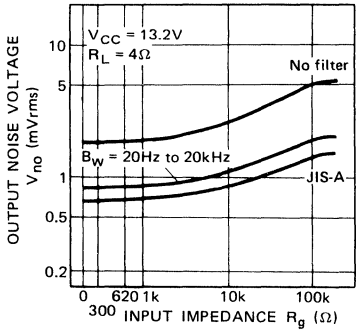


Fig. 7 – OUTPUT POWER vs. LOAD IMPEDANCE

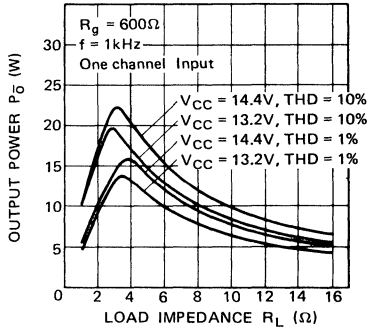


Fig. 8 – RIPPLE REJECTION vs. FREQUENCY

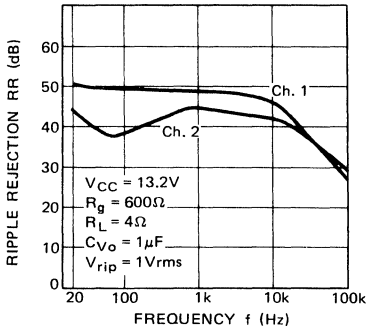


Fig. 9 – POWER DISSIPATION vs. OUTPUT POWER

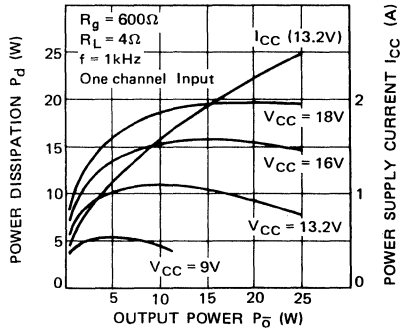
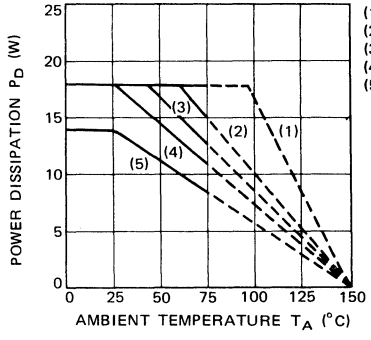


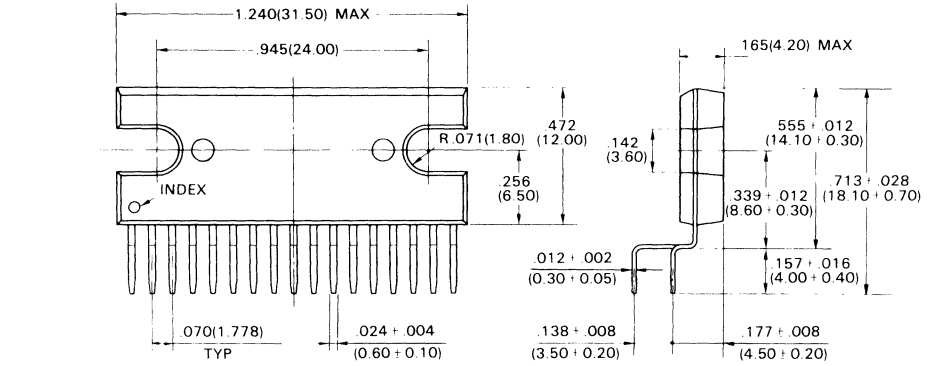
Fig. 10 – POWER DISSIPATION vs. AMBIENT TEMPERATURE

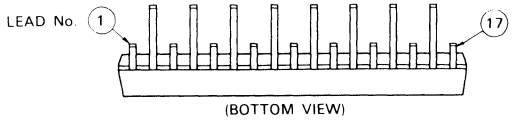


(1) Infinite Heat Sink
(2) 900cm² x 2mmAℓ
(3) 400cm² x 2mmAℓ
(4) 200cm² x 2mmAℓ
(5) 100cm² x 2mmAℓ

PACKAGE DIMENSIONS

17-LEAD PLASTIC ZIG-ZAG IN-LINE PACKAGE
(Case No. : ZIP-17P-M02)





Dimensions in inches
(millimeters)

3

FUJITSU

NINE-LEVEL DETECTOR AND DRIVER FOR LEVEL METER

MB3764

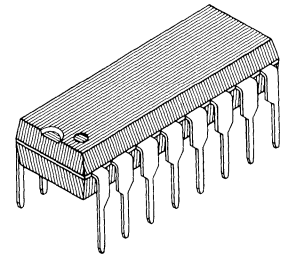
September 1987
Edition 1.0

3

NINE-LEVEL DETECTOR AND DRIVER FOR LEVEL METER

The Fujitsu MB3764 is a nine-level detector and driver for level meters. The MB3764 contains an internal reference voltage generator and an operational amplifier with offset, so it recognizes the extended analog voltage level range, including negative voltage.

- Nine output levels
- Wide range of preset reference voltages: 1.25 V to 13 V
- Reverse phase input operational amplifier with an offset of half a reference voltage.
- High output current: 20 mA max.
- Output enabling. (Output enable time T_{ON} = 120 ns max)



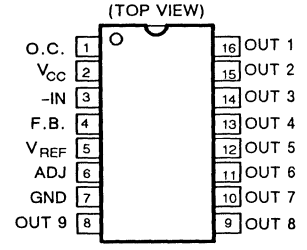
PLASTIC PACKAGE
DIP-16P-M04

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Condition	Value	Unit
Power Supply Voltage	V_{CC}	—	18	V
Output Voltage	V_{OH}	—	18	V
Amp Input Voltage	V_{IN}	—	-0.3 to V_{CC}	V
Control Input Voltage	V_{OC}	—	-0.3 to 7.0	V
Power Dissipation	P_D	$T_A \leq 75°C$	710	mW
Storage Temperature	T_{STG}	—	-55 to 125	°C

NOTE: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

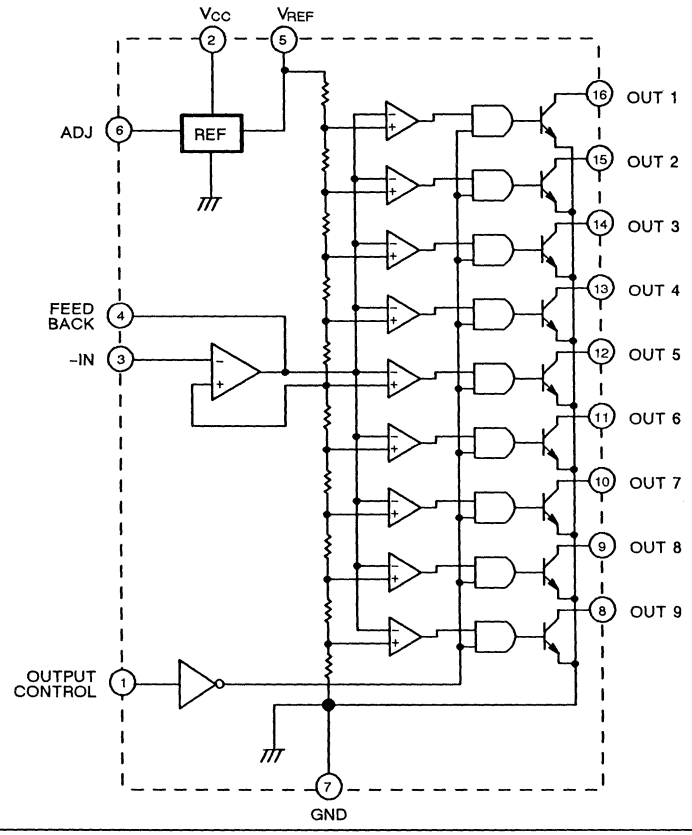
PIN ASSIGNMENT



Small geometry bipolar integrated circuits are occasionally susceptible to damage from static voltages or electric fields. It is therefore advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this device.

3

Figure 1. MB3764 Block Diagram



RECOMMENDED OPERATING CONDITIONS

Parameter	Designator	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	3.2	—	16	V
Output Current	I_{OUT}	—	10	20	mA
Feed Back Sink Current	I_{SINK}	—	—	0.5	mA
Feed Back Source Current	I_{SOURCE}	—	—	2	mA
Feed Back Voltage	V_{FB}	—	—	13	V
Reference Voltage Output Current	I_{REF}	0	—	5	mA
Reference Voltage	V_{REF}	1.2	—	13	V
Operating Ambient Temperature	T_A	-20	25	75	°C

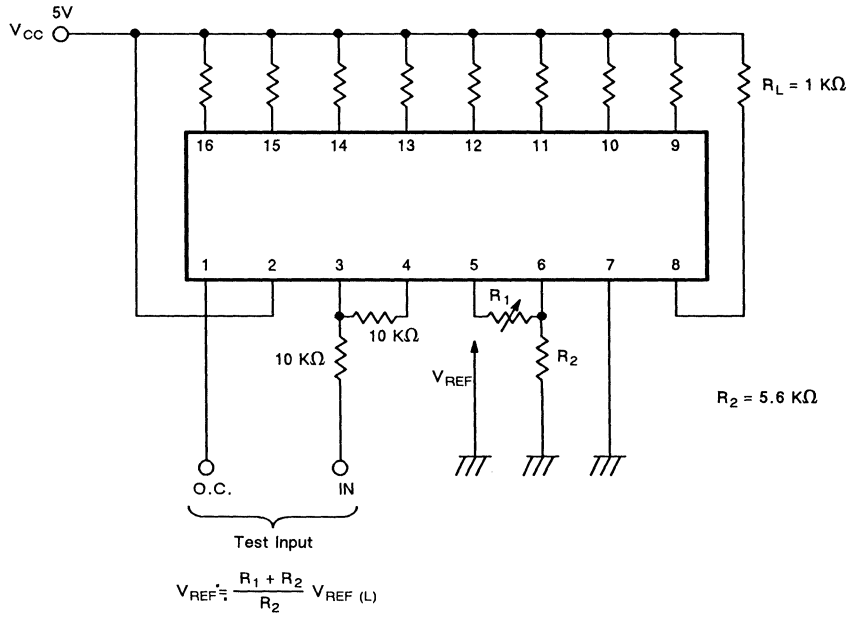
ELECTRICAL CHARACTERISTICS (V_{CC}= 5V, T_A = 25°C, V_{REF} = 2.5V)

Parameter		Designator	Conditions	Values			Unit
				Min	Typ	Max	
Power Supply Current		I_{CC}	R1=0, R2=∞	—	9	14	mA
Reference Voltage Generator Section	Output Voltage	V_{REFL}	R1=0	1.20	1.25	1.30	V
	Input Voltage Stability	ΔV_{RIN}	4.5 V ≤ V_{CC} ≤ 16 V	—	2	30	mV
	Load Voltage Stability	ΔV_{RLD}	0 ≤ I_{REF} ≤ 5 mA	—	2	30	mV
	Temperature Stability	ΔV_R	-20°C ≤ T_A ≤ 75°C	—	6	40	mV
	Short-circuit Current	I_{SC}	—	—	15	—	mA
Comparator Section	Quantumization Distortion	ϵ	—	—	±0.5	±2	%
	Center Voltage Deviation	V_M	3 and 4 Pins are connected.	1.20	1.25	1.30	V
Error Amplifier Section	Input Bias Current	I_{IB}	V3 = 0	-250	-30	—	nA
	Voltage Gain	A_V	0.5 V ≤ V_O ≤ 2.5 V	60	80	—	dB
	Band Width	BW		—	1	8	MHz
	Slew Rate	SR		—	0.5	—	V/µs
	High Level Output Voltage	V_{OH}	I_{SOURCE} = 2 mA	2.8	3.3	—	V
	Low Level Output Voltage	V_{OL}	I_{SINK} = 0.5 mA	—	0.1	0.3	V
Output Section	Output Saturation Voltage	V_{SAT1}	I_{OUT} = 10 mA	—	0.1	0.4	V
		V_{SAT2}	I_{OUT} = 20 mA	—	0.15	1.0	V
	Output Leakage Current	I_{OH}	V_O = 16V	—	—	10	µA
Control Section	High Level Input Current	I_{IH}	V_{OC} = 5V	—	50	300	µA
	Low Level Input Current	I_{IL}	V_{OC} = 0	-1.0	-0.6	—	mA
	High Level Input Voltage	V_{IH}	-20°C ≤ T_A ≤ 75°C	2.0	—	—	V
	Low Level Input Voltage	V_{IL}	-20°C ≤ T_A ≤ 75°C	—	—	0.8	V
	Delay Time	T_{ON}	R_L = 200Ω	—	40	120	ns
		T_{OFF}	R_L = 200Ω	—	60	—	ns

* $\epsilon = \frac{|\text{Each Threshold Error Voltage}| \text{ Max}}{|\text{Full Scale Voltage}|}$

3

Figure 2. Measurement Circuit



TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 3 – Power Supply Current vs Power Supply Voltage

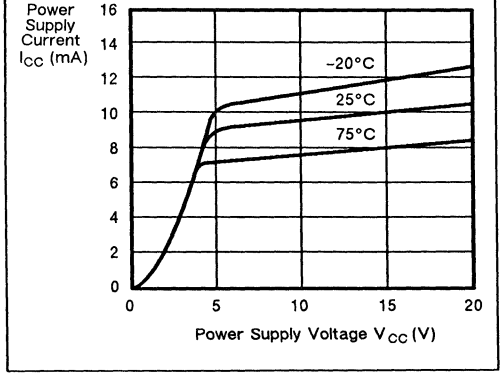
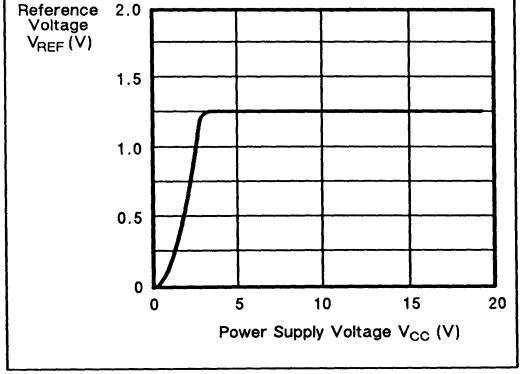


Fig. 4 – Reference Voltage vs Power Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 5 – Reference Voltage Stability vs Ambient Temperature

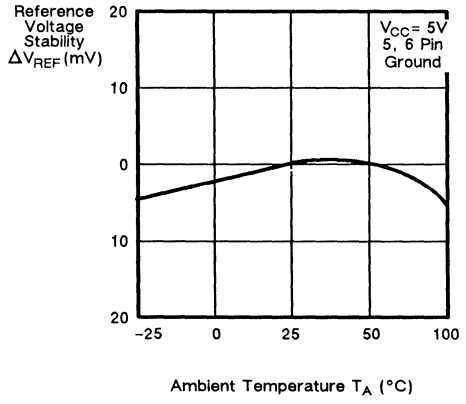


Fig. 6 – Output Voltage vs Op-Amp Output Current

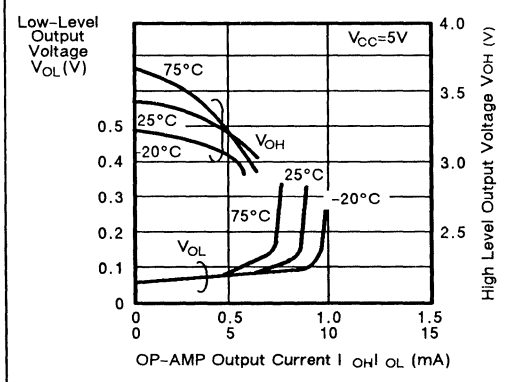


Fig. 7 – Output Saturation Voltage vs Output Current

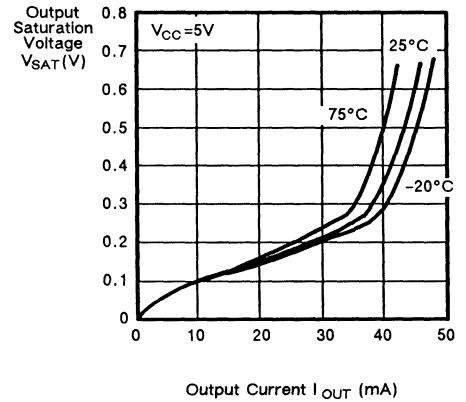
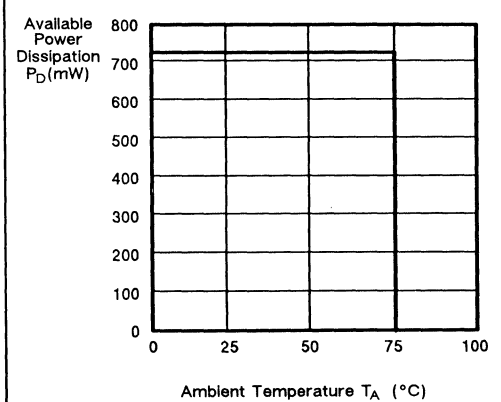
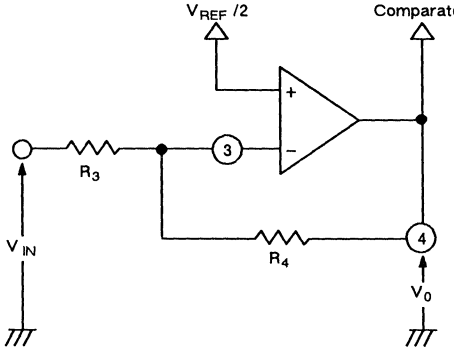


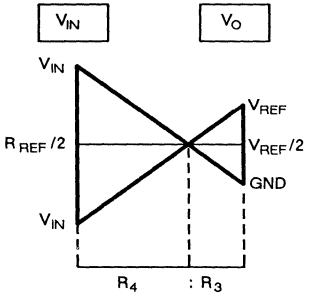
Fig. 8 – Available Power Dissipation vs Ambient Temperature



APPLICATION EXAMPLES

Figure 9. Voltage Recognition: V_{REF} /2





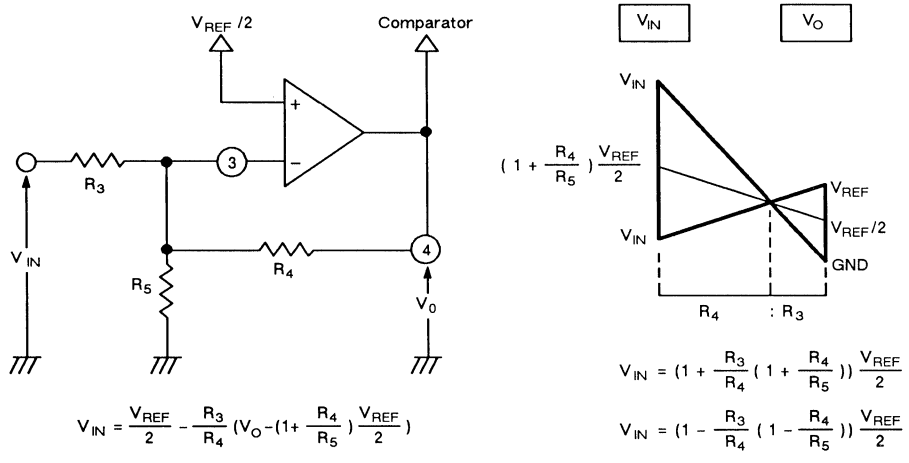
$$V_{IN} = \frac{V_{REF}}{2} - \frac{R_3}{R_4}\left(V_O - \frac{V_{REF}}{2}\right)$$

$$V_{IN} = \left(1 + \frac{R_3}{R_4}\right)\frac{V_{REF}}{2}$$

$$V_{IN} = \left(1 - \frac{R_3}{R_4}\right)\frac{V_{REF}}{2}$$

APPLICATION EXAMPLES (Continued)

Figure 10. Voltage Recognition: Above V_{REF} /2



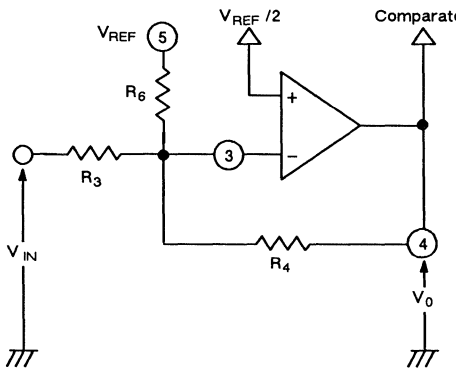
$$V_{IN} = \frac{V_{REF}}{2} - \frac{R_3}{R_4}\left(V_O - \left(1 + \frac{R_4}{R_5}\right)\frac{V_{REF}}{2}\right)$$

$$V_{IN} = \left(1 + \frac{R_3}{R_4}\left(1 + \frac{R_4}{R_5}\right)\right)\frac{V_{REF}}{2}$$

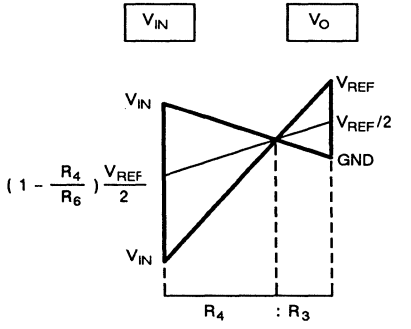
$$V_{IN} = \left(1 - \frac{R_3}{R_4}\left(1 - \frac{R_4}{R_5}\right)\right)\frac{V_{REF}}{2}$$

APPLICATION EXAMPLES (Continued)

Figure 11. Voltage Recognition: Below V_{REF} /2



$$V_{IN} = \frac{V_{REF}}{2} - \frac{R_3}{R_4}\left(V_O - \left(1 - \frac{R_4}{R_6}\right)\frac{V_{REF}}{2}\right)$$

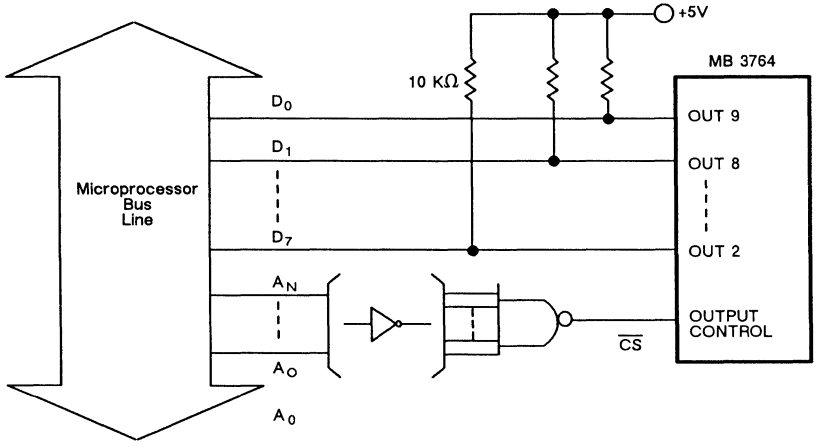


$$V_{IN} = \left(1 + \frac{R_3}{R_4}\left(1 - \frac{R_4}{R_6}\right)\right)\frac{V_{REF}}{2}$$

$$V_{IN} = \left(1 - \frac{R_3}{R_4}\left(1 + \frac{R_4}{R_6}\right)\right)\frac{V_{REF}}{2}$$

APPLICATION EXAMPLES (Continued)

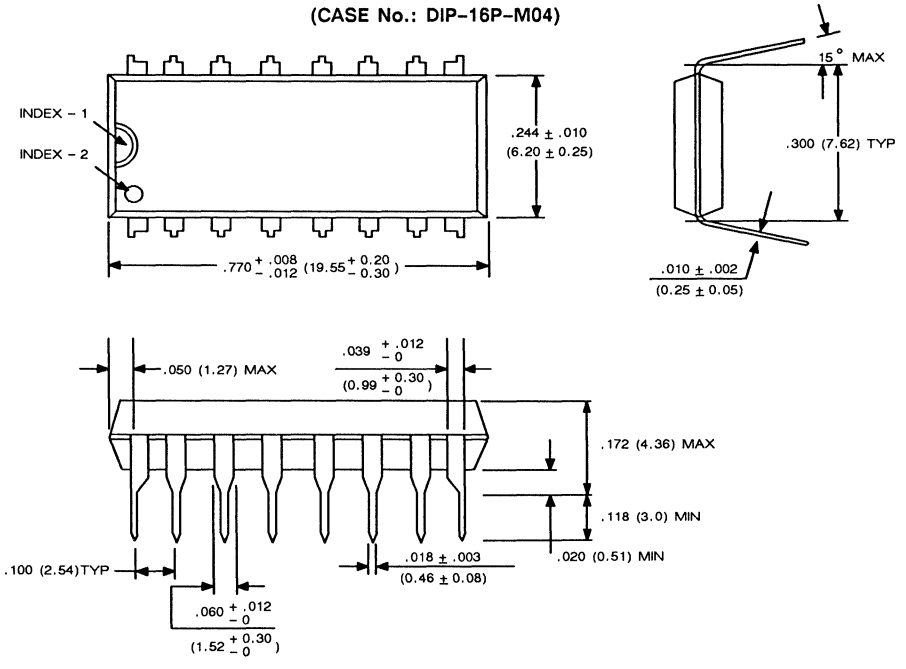
Figure 12. Connection with Microprocessor Bus



$\overline{CS}$: Chip Select (MB3764 Chip Select Pin, Selected at $\overline{CS}$ = 0)

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



Dimensions in
inches (millimeters)

D16033S-2C

FUJITSU

FM STEREO MULTIPLEX DEMODULATOR

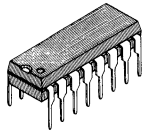
MB4104
MB4105

February 1989
Edition 2.0

FM STEREO MULTIPLEX DEMODULATOR

The Fujitsu MB4104/4105 is a monolithic FM stereo multiplex demodulator fabricated using Fujitsu's advanced bipolar technology. Using PLL circuitry, this device achieves stable performance against the variance condition of external elements.

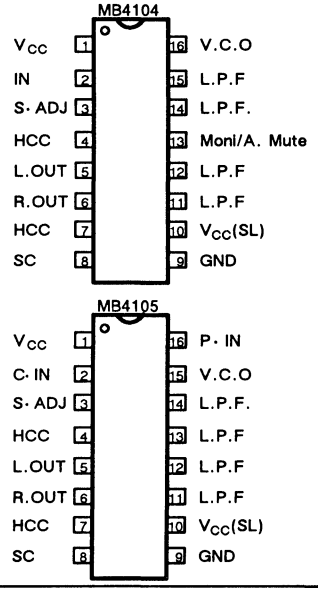
- Separation control circuit reduces noise, in a weak electrical field.
- PLL circuitry means less external elements.
- Reduced FM noise in weak electrical fields, with high cut control circuit.
- Low Distortion : 0.06% typical at 300 mV input.
- On-chip forced monaural, forced VCO stop, lamp driver, and audio muting circuits.
- Separate pilot signal and composite signal inputs MB 4105.
- 16-pin plastic DIP package (Suffix: -p)



PLASTIC PACKAGE
DIP-16P-M04

PIN ASSIGNMENT

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (see NOTE) (Tc = 25°C)

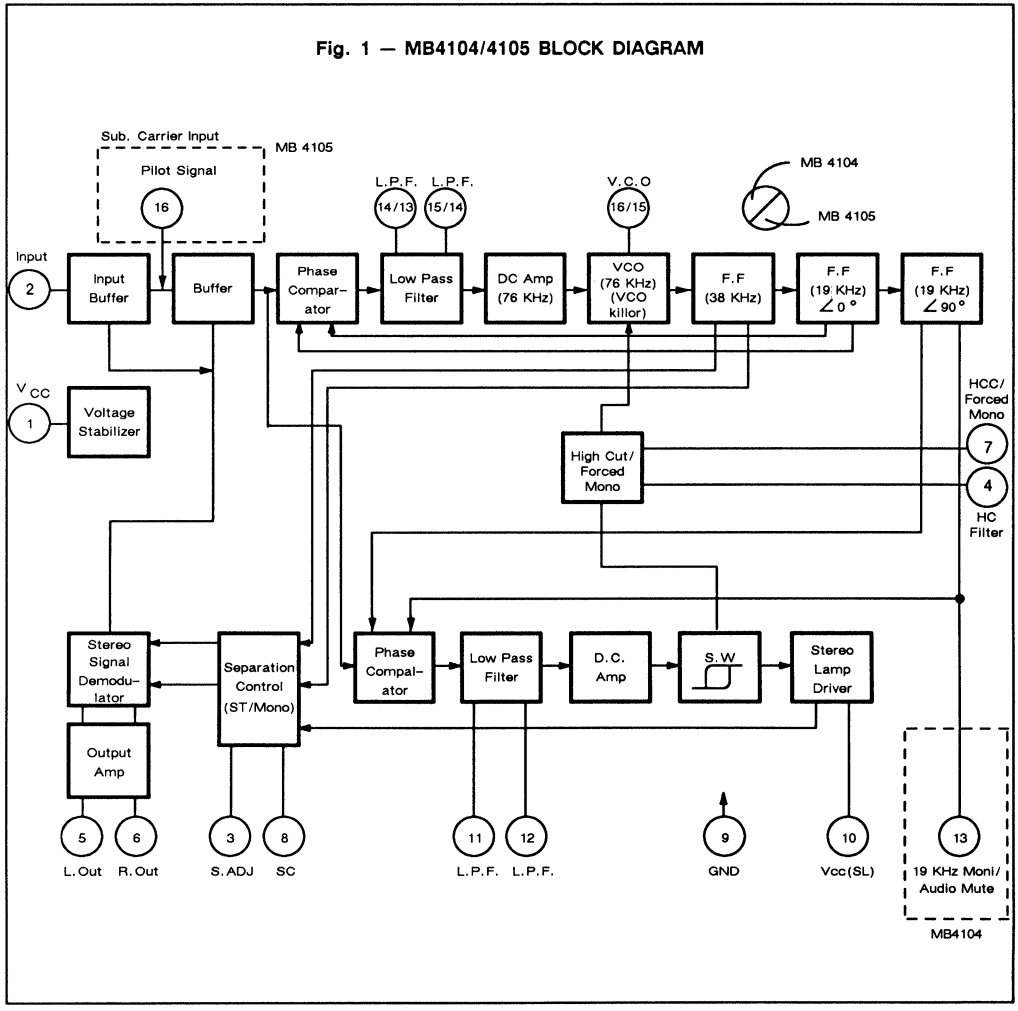
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	16	V
Lamp Drive Current	I_L	75	mA
Power Dissipation	P_D	520	mW
Operating Temperature	T_A	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

3

Fig. 1 — MB4104/4105 BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

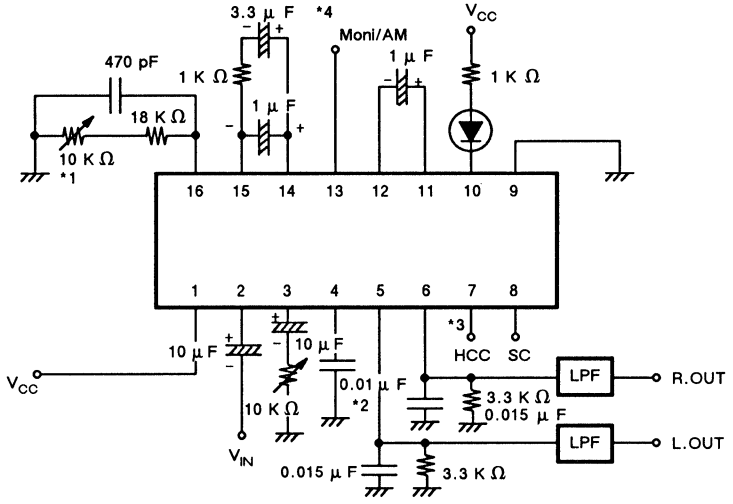
Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	8 to 14	V
Operating Temperature	T_A	-20 to +75	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 10 V, V_{IN} = 300 mVrms, f = 1 KHz, L + R = 90%, Pilot = 10%, T_A = 25°C)

Parameter	Symbol	Conditions	Values			Unit
			Min	Typ	Max	
Quiescent Power Supply Current	I_Q	V_{IN} = 0V		16	25	mA
Channel Separation	CS		40	55		dB
Total Harmonic Distortion	THD	Stereo		0.06	0.3	%
		Mono		0.06	0.3	%
Output Voltage	V_O		210	300	420	mVrms
Channel Balance	CB			0	1.5	dB
Lamp Level		Pilot Signal	5	8	12	mV
Lamp Hysteresis		Pilot Signal		4.5	7	dB
SCA Rejection Ratio				80		dB
S/N Ratio	S/N		70	78		dB
Input Impedance	R_{IN}		20	30		kΩ
Capture Range	CR	Pilot = 30 mV		±4		%
Maximum Input Voltage	$V_{IN(MAX)}$	THD ≦ %	600	1000		mVrms
SC Output Attenuation		V_8 = 0.6 V, Sub	-12	-6	-1	dB
SC Output Voltage		V_8 = 0.1 V, Sub			5	mV
HCC Output Attenuation 1		V_7 = 1.2 V	-3	-1	0	dB
HCC Output Attenuation 2		V_7 = 0.6 V	-18	-10	-2	dB
Power Supply Ripple Rejection Ration	R.R.			35		dB
Audio Mute Attenuation	—	V_{13} = 0.2 V		55		dB

3

Fig. 2 — MB4104 TEST CIRCUIT



Notes:

*1. VCO Free Running Frequency should be adjusted in order to output 19.000 KHz ±10 Hz, at pin 13.

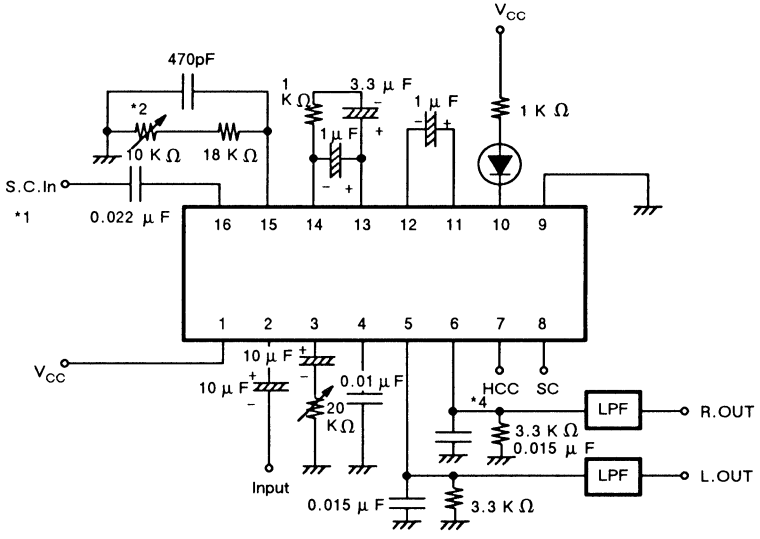
*2. The value is 100 μF when SC and HCC are measured.

*3. When over 7.0 V is applied to pin 7, the device is in forced monaural mode and VCO stops. If a voltage higher than V_{CC} is applied to pin 7, about 10 KΩ should be inserted.

*4. When pin 13 = GND, or is lower than 0.4 V, the device is in audio mute mode.

3

Fig. 3 — MB4105 TEST CIRCUIT



Notes:

*1. The pilot signal can be input to pin 16. Therefore input signal, without the pilot signal input to pin 2, makes the LPF design easier.

*2. VCO (76 KHz) signal should be adjusted.

*3. When over 7.0 V is applied to pin 7, the device is in forced monaural mode and VCO stops. If the voltage higher than V_{CC} is applied to pin 7, about 10 KΩ should be inserted.

3

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 4
TOTAL HARMONIC DISTORTION (MAIN, MONO), C.B vs INPUT VOLTAGE

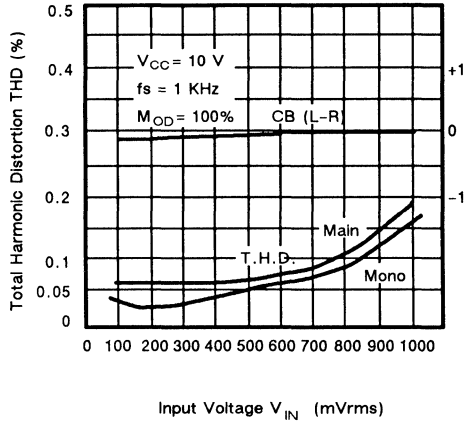


Fig. 5
TOTAL HARMONIC DISTORTION (MAIN, MONO), C.B vs POWER SUPPLY VOLTAGE

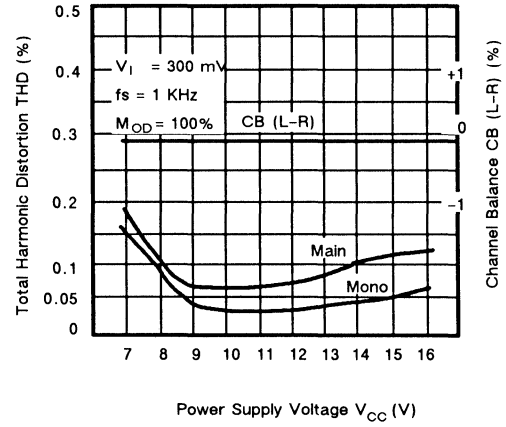


Fig. 6
CHANNEL SEPARATION vs INPUT VOLTAGE

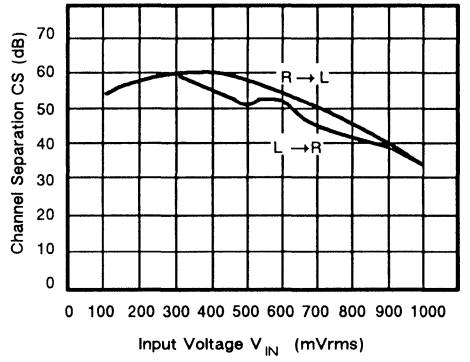
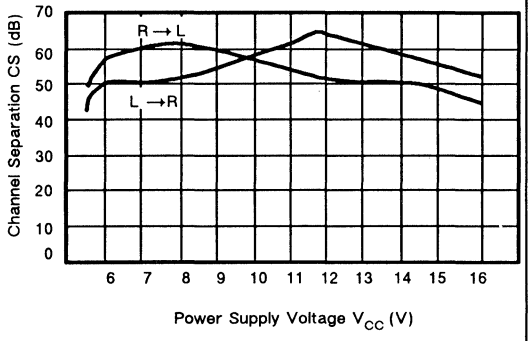


Fig. 7
CHANNEL SEPARATION vs POWER SUPPLY VOLTAGE



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 8
VOLTAGE GAIN, TOTAL HARMONIC DISTORTION vs FREQUENCY

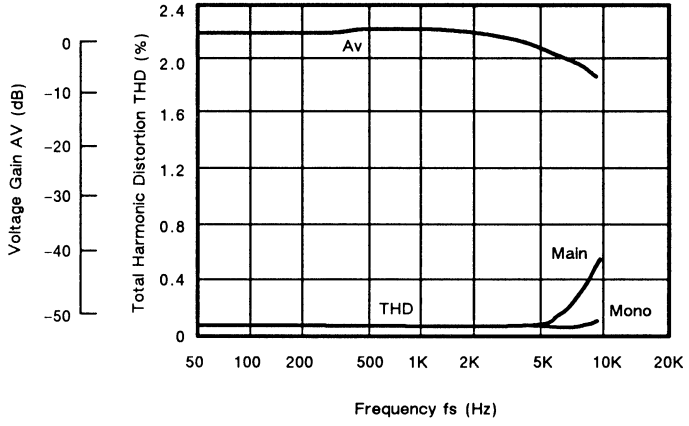


Fig. 9
CHANNEL SEPARATION vs FREQUENCY

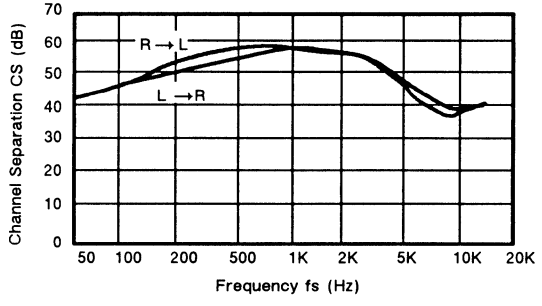
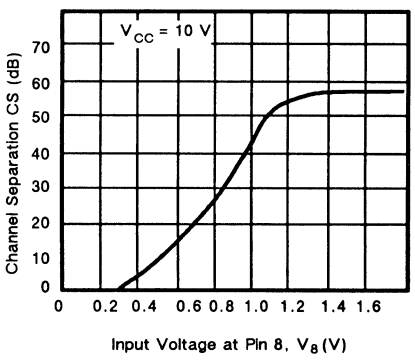


Fig. 10
CHANNEL SEPARATION vs INPUT VOLTAGE AT PIN 8



3

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 11
ATTENUATION vs INPUT VOLTAGE AT PIN 7

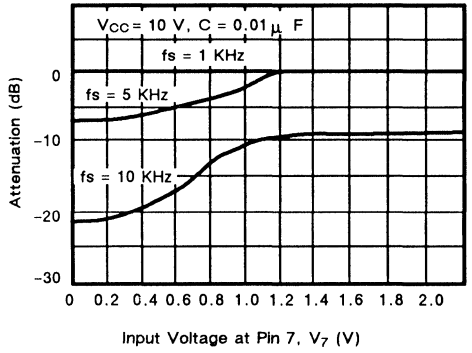


Fig. 12
INPUT VOLTAGE vs OSCILLATOR FREE RUNNING FREQUENCY

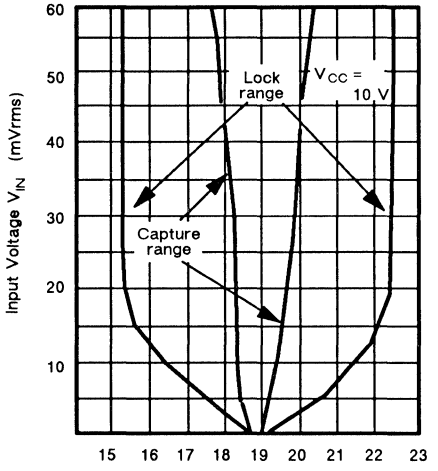


Fig. 13
PILOT SIGNAL VOLTAGE vs POWER SUPPLY VOLTAGE

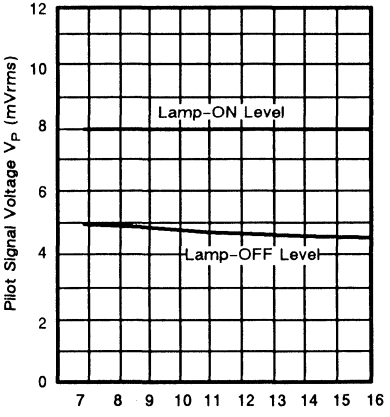
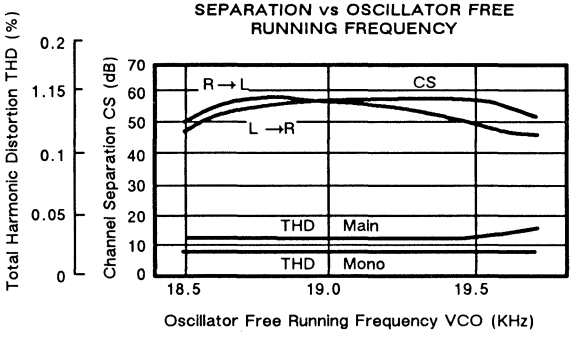


Fig. 14
TOTAL HARMONIC DISTORTION, CHANNEL SEPARATION vs OSCILLATOR FREE RUNNING FREQUENCY



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 15
PILOT SIGNAL VOLTAGE vs TEMPERATURE

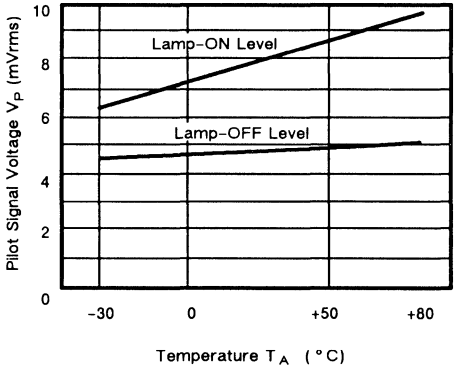


Fig. 16
OSCILLATOR FREE RUNNING FREQUENCY ERROR vs TEMPERATURE

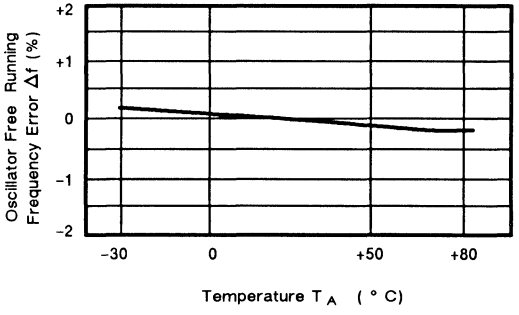


Fig. 17
OSCILLATOR FREE RUNNING FREQUENCY ERROR vs POWER SUPPLY VOLTAGE

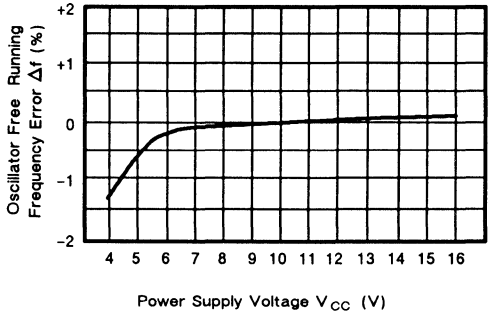
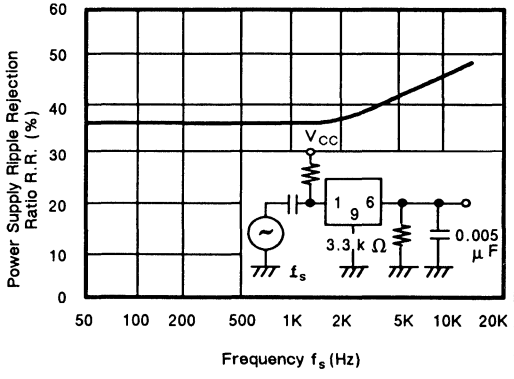
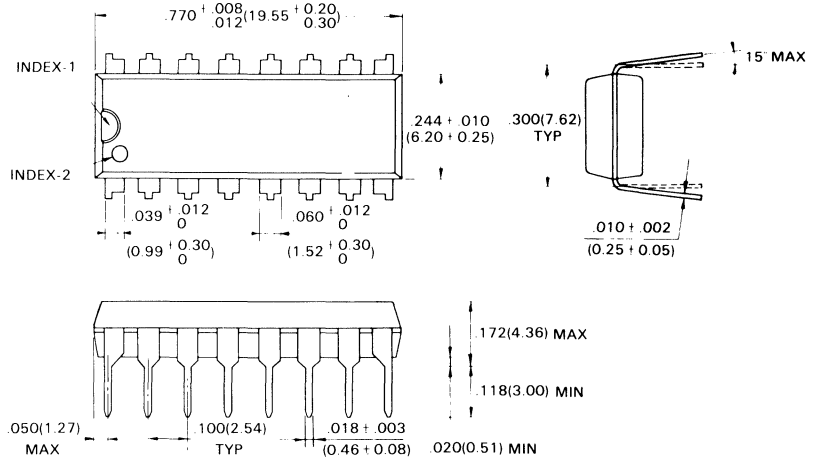


Fig. 18
POWER SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY



PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



Dimensions in inches (millimeters)

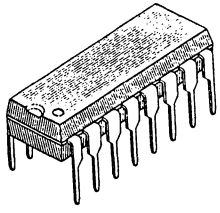
FUJITSU

MB87032

TS584-A87Z
December 1987

TWO-CHANNEL VOLUME CONTROLLER

PRELIMINARY

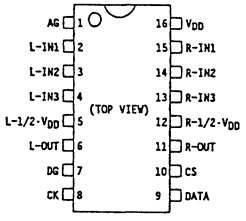


PLASTIC PACKAGE
DIP-16P-M03

The Fujitsu MB87032 is a high efficiency 2-channel electric volume fabricated using a CMOS silicon gate process.
The MB87032 has the selection of either volume, balance, loudness mode or volume, balance, tone control mode.
This device enables the feather touch control of TV, Video recoder and Car Stereo.

- TTL interface enables micro-computer control
- Volume gain control range
  0 dB to -78 dB every 1 dB step
  -80 dB (Mute mode)
- To control on-chip 2-channel volume (L-channel and R-channel), this enables balance control mode
- 13 kinds of tone control is selectable depending on exteranal condenser and resistor
- Loudness operation is possible from 0 dB
- Single supply voltage : +8 V
- 16-pin Dual-In-Line Package (Suffix: -P)

PIN ASSIGNMENT



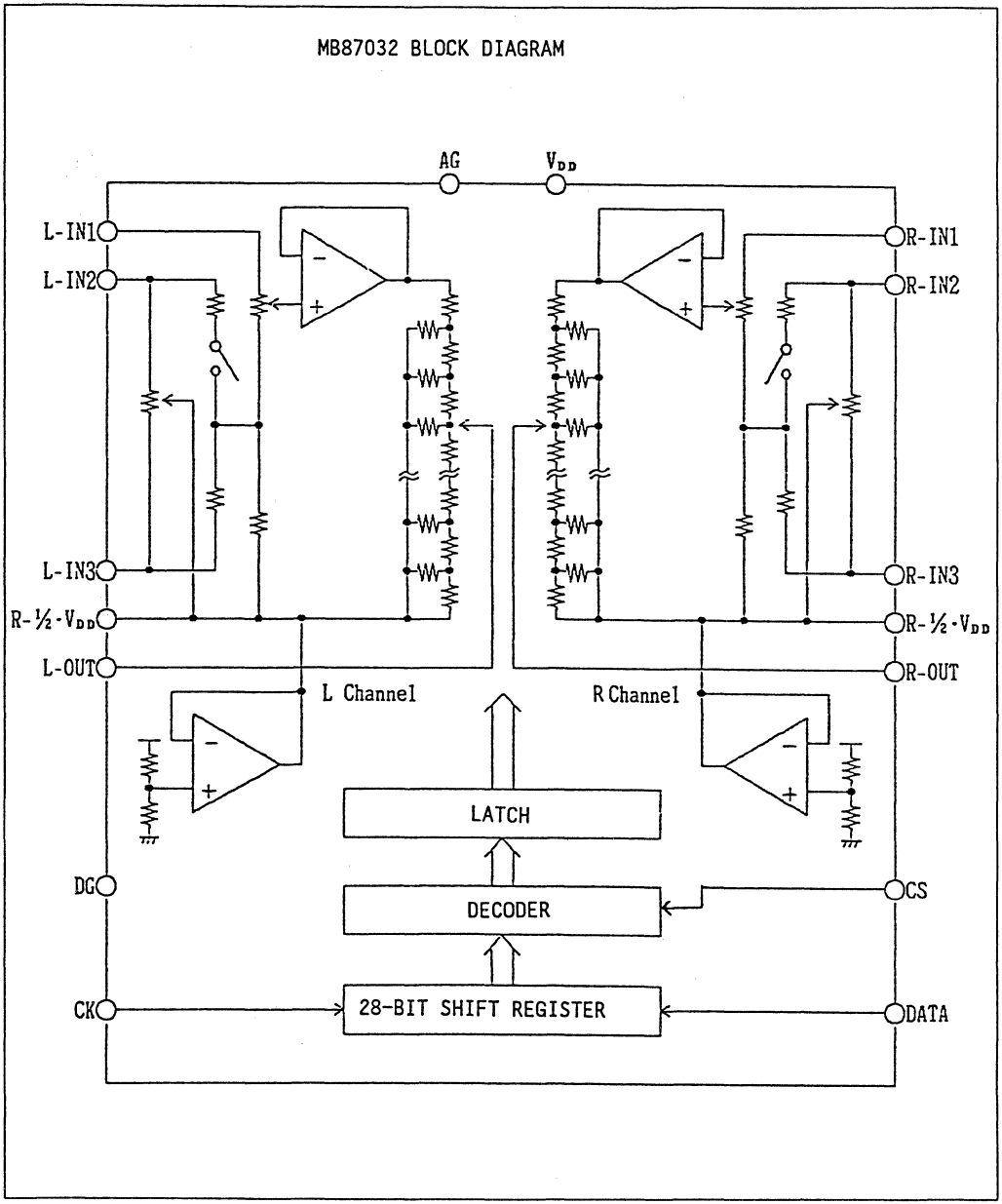
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Pin Name	Value			Unit
			Min	Typ	Max	
Supply Voltage	V_{DD}	V_{DD}			10	V
Input Voltage	V_I	All input pins	GND-0.3		V_{DD}+0.3	V
Output Voltage	V_O	All output pins	GND-0.3		V_{DD}+0.3	V
Storage Temperature	T_{STG}		-50		125	°C

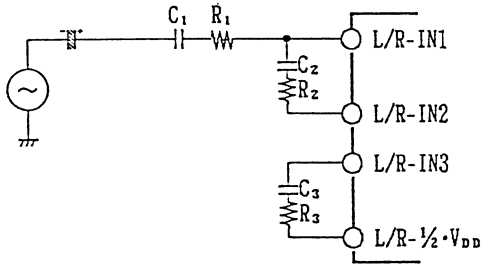
NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

MB87032 BLOCK DIAGRAM

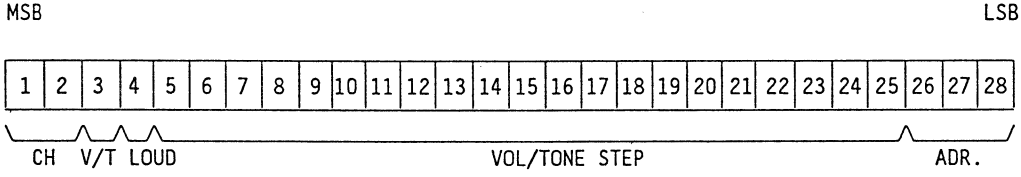


PIN DESCRIPTIONS

Pin No.	Pin Name	Descriptions
1	AG	Ground for analog circuit
2 15	L-IN1 R-IN1	Analog input pins These pins should be driven by a low impedance (100 Ω or less.)
3 14	L-IN2 R-IN2	
4 13	L-IN3 R-IN3	 Input pins connection example Volume, loudness, tone mode is selected depending on the value of R_1,R_2,R_3,C_1,C_2 and C_3. (including open and short) Please see the application example circuit.
5 12	L-1/2·V_{DD} R-1/2·V_{DD}	A half level of supply voltage is output.
6 11	L-OUT R-OUT	Electrical volume output pins If the following stage is low impedance, step error will occur because these output are high impedance. The following stage must be high impedance. (1 MΩ or greater.)
7	DG	Ground for digital circuit
8	CK	Clock signal input Data is input from DATA pin every falling edge of CK signal.
9	DATA	Data input Data consists of 28-bit data which is serially input every falling edge of CK signal.
10	CS	Strobe signal input Control data is latched every falling edge of CS signal. Unless strobe signal is input, control data keeps former condition. Please see the timing diagram.
16	V_{DD}	Supply voltage, +8 V

FUNCTIONAL DESCRIPTIONS

Input 28-bit data consists of channel selection data, volume/tone mode selection data, loudness mode selection data, volume step data or tone step data and address data. Input data format is shown below.



3

Parameter	Bit	Description
CH	1,2	Input data determines which channel is activated. 1st bit selects L-channel and 2nd bit selects R-channel. As the results, both channels operate separately. When this bit is high level, data is written. When this bit is low level, former data is latched. This data is used as right and left valance because R-channel and L-channel can operate respectively.
V/T	3	This data determines how 28-bit data is used, volume control data or tone control data. When this bit is high level, 28-bit data is used as volume control data. When this bit is low level, 28-bit data is used as tone control data.
LOUD	4	Loudness mode selection input When this bit is high level, loudness mode is selected. When this bit is low level, loudness mode is not selected.
VOL/TONE STEP	5 to 25	According to V/T bit, this data specify volume step data or tone step data. When volume mode, 5 to 20 bit data specify MAIN switch data, and 21 to 25 bit data specify FINE switch data. When tone mode, 5 to 17 bit specify tone step data. (18 to 25 bit is ignored, please set high or low.) Volume step is prepared by the combination of MAIN switch and FINE switch. Only one arbitrary bit of MAIN switch (5 to 20 bit) is allowed to set high level. Only one arbitrary bit of FINE switch (21 to 25 bit) is allowed to set high level. The others combination is not allowed. When tone mode, only one arbitrary bit of 13 bit (5 to 17 bit) is allowed to set high or all bit are set low level. The others combinatic is not allowed.

Parameter	Bit	Description

Serial data (5 to 25 bit)

VOL/TONE STEP — 5 to 25

5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
0	-5	-10	-15	-20	-25	-30	-35	-40	-45	-50	-55	-60	-65	-70	-75

Attenuation (dB)

MAIN SWITCH

21	22	23	24	25
0	-1	-2	-3	-4

Serial data (21 to 25 bit)

Attenuation (dB)

FINE SWITCH

5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	2	3	4	5	6	7	8	9	10	11	12	13	--	--	--

Tone step

21	22	23	24	25
--	--	--	--	--

ADR — 26 to 28

26 27 28
0 0 1

These data specify address bit. FJ specifies the address as MB87032 address. If the address is set as 0 0 1, 28-bit data are acceptable. If the others address is set, data is not acceptable.

The data format of volume mode is shown below.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
L	R	1	0	0	-5	-10	-15	-20	-25	-30	-35	-40	-45	-50	-55	-60	-65	-70	-75

CH — V/T (Fix) — LOUD — MAIN SECTION

21	22	23	24	25	26	27	28
0	-1	-2	-3	-4	0	0	1

FINE SECTION — ADR (Fix)

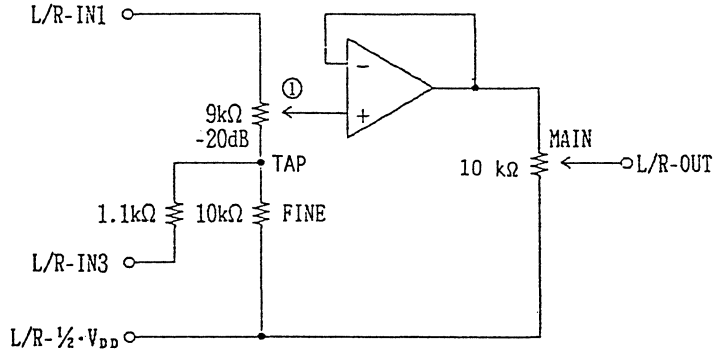
The data format of tone mode is shown below.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
L	R	0	0	11	12	13	14	15	16	17	18	19	20	21	22	23	--	--	--
CH		V/T	LOUD					TONE STEP											

21	22	23	24	25	26	27	28
---	--	--	--	--	0	0	1
					ADR (Fix)		

VOLUME SECTION SPECIFICATION

Parameter	Description
Step value	Attenuation range of 0 to -78 dB every -1 dB step is selected by the combination of MAIN section and FINE section. MAIN section variables every -5 dB steps and FINE section variables every -1 dB step.
-∞ (Mute)	When volume is set as -79 dB, -∞ (Mute) mode is selected.
Volume structure	

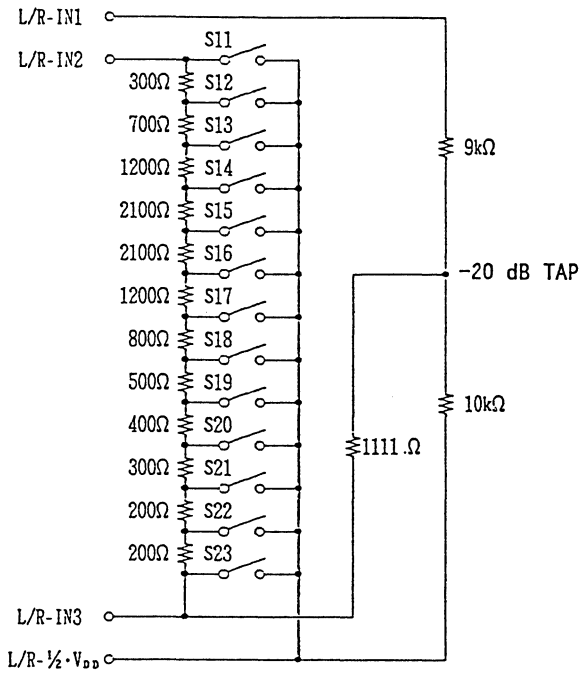


Attenuation range of 0 to -20 dB every -1 dB stpe is selected by (1)
Attenuation range of -20 to -78 dB every -1 dB step is selected by the the combination of MAIN and FINE.

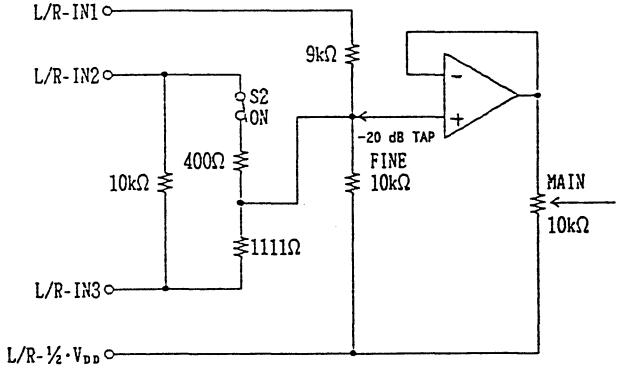
TONE SECTION / LOUDNESS SECTION SPECIFICATION

Parameter	Description
Step	13 steps
Volune tap	-20 dB

STEP structure



LOUDNESS structure



When S2 is on, loudness mode is selected. In this case, tap point is -20 dB.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Pin No.	Value			Unit
			Min	Typ	Max	
Supply Voltage	V_{DD}	16	6	8	10	V
Digital Input Voltage	V_{DI}	8,9,10	0		V_{DD}	V
Analog Input Voltage	V_{AI}	2,15		1	$\sqrt{2}$	Vrms
Operating Temperature	T_A		0		70	°C

DC CHARACTERISTICS

(V_{DD}=8V±10%, T_A=0 to 70°C unless otherwise noted.)

Parameter	Symbol	Pin No.	Value			Unit
			Min	Typ	Max	
Reference Voltage	V_{REF}	5,12	$1/2 \cdot V_{DD}$-10%	$1/2 \cdot V_{DD}$	$1/2 \cdot V_{DD}$+10%	V
Supply Current	I_{DD}	16			7	mA
Digital Input High Voltage	V_{IH}	8,9,10	2.4		V_{DD}	V
Digital Input Low Voltage	V_{IL}	8,9,10	0		0.4	V

AC CHARACTERISTICS

(V_{DD}=8V±10%, T_A=0 to 70°C unless otherwise noted.)

Parameter	Symbol	Pin No.	Condition	Value			Unit
				Min	Typ	Max	
Analog Input Voltage	V_{AI}	2,15			1		Vrms
Analog Input Frequency	A_f	2,15		40		20000	Hz
Attenuation		6,11	Referenced to $1/2 \cdot V_{DD}$ pin	0		-78	dB
Attenuation at Mute mode		6,11	0dBV=1Vrms			-80	dB
Attenuation Differential * Error	ΔLR	6,11	Referenced to $1/2 \cdot V_{DD}$ pin	-0.3		0.3	dB
L-R Attenuation Differential Error	ΔATT	6,11	Referenced to $1/2 \cdot V_{DD}$ pin	-0.5		0.5	dB
Total Harmonic Distortion	THD	6,11	Output=100mVrms Attenuation=0dB		0.01	0.05	%
Tone Total Resistance	R_{TONE}	3,14		6	10	14	kΩ
Volume Switch ON Resistance			T_A=25°C		300	500	Ω
Tone Switch ON Resistance			T_A=25°C		200	300	Ω

Note: Attenuation differential error between two steps at volume mode.

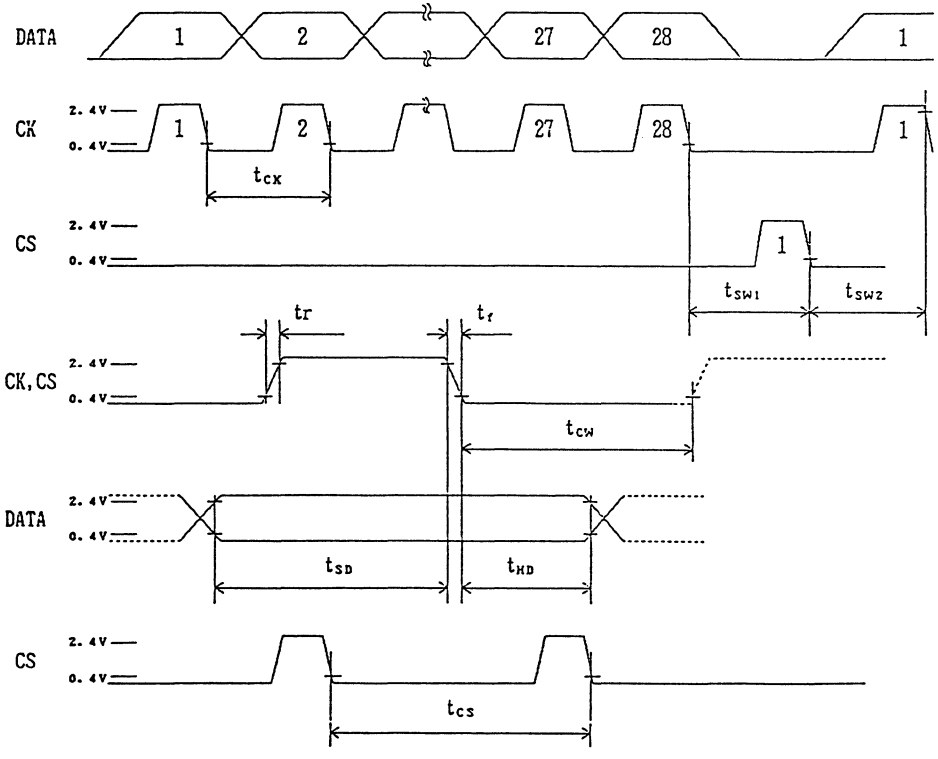
AC CHARACTERISTICS (Continued)

(V_{DD}=8V±10%, T_A=0 to 70°C unless otherwise noted.)

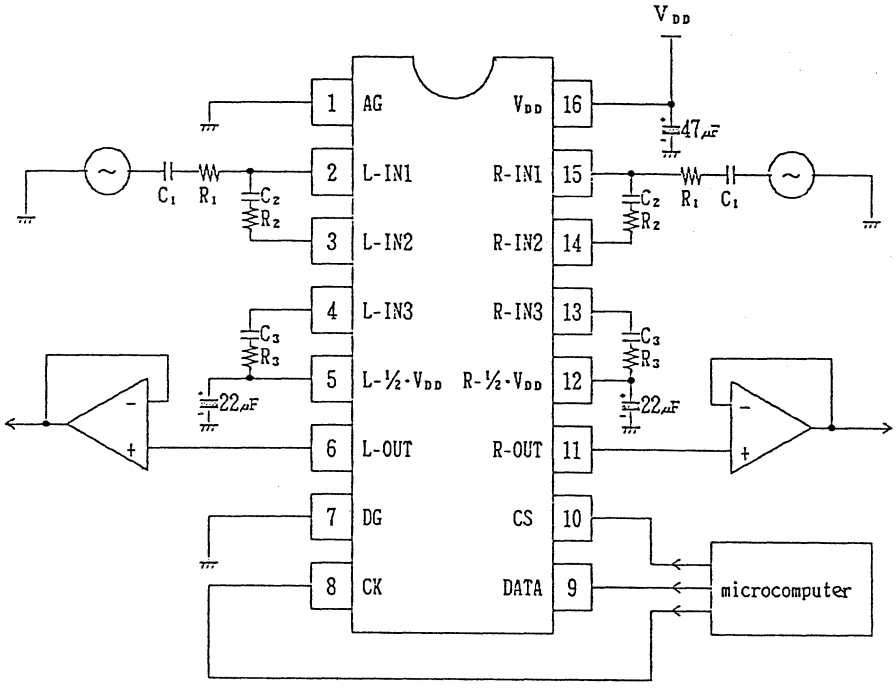
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Clock/Strobe Signal Pulse Width	t_{CW}	300			ns
Input Clock Signal Period	t_{CK}	500			ns
Input Strobe Signal Period	t_{CS}	14500			ns
Time Between CK(28) and CS	t_{SW1}	500			ns
Time Between CS and CK(1)	t_{SW2}	500			ns
Data Set-up Time	t_{SD}	150			ns
Data Hold Time	t_{HD}	200			ns
Rise Time	t_r			50	ns
Fall Time	t_f			50	ns

Notes:
Serial 28-bit data is input every falling edge of CK signal.
Serial 28-bit data is latched in internal latch every falling edge of CS signal.
It is prohibited to apply the clock and data while CS signal is rising.

TIMING DIAGRAM



APPLICATION EXAMPLE CIRCUIT



Mode	TONE S11 to S23	LOUD S2	R1	R2	R3	C1	C2	C3
Volume & Balance	OFF	OFF	Short	Open	Short	Short	Open	Short
Volume & Balance & Loundess	OFF	ON	Short	2.2 kΩ	0.22 kΩ	1μF	0.0047 μF	0.22 μF
Volume & Balance & Tone-1	One arbitrary bit is set high	OFF	4.7 kΩ	Short	Short	1μF	0.1 μF	1μF
Volume & Balance & Tone-2	One arbitrary bit is set high	OFF	4.7 kΩ	Short	Short	1μF	0.1 μF	Short

TYPICAL CHARACTERISTICS CURVES

FIG.3 - TONE VS. FREQUENCY EXAMPLE (Depend on application circuit)

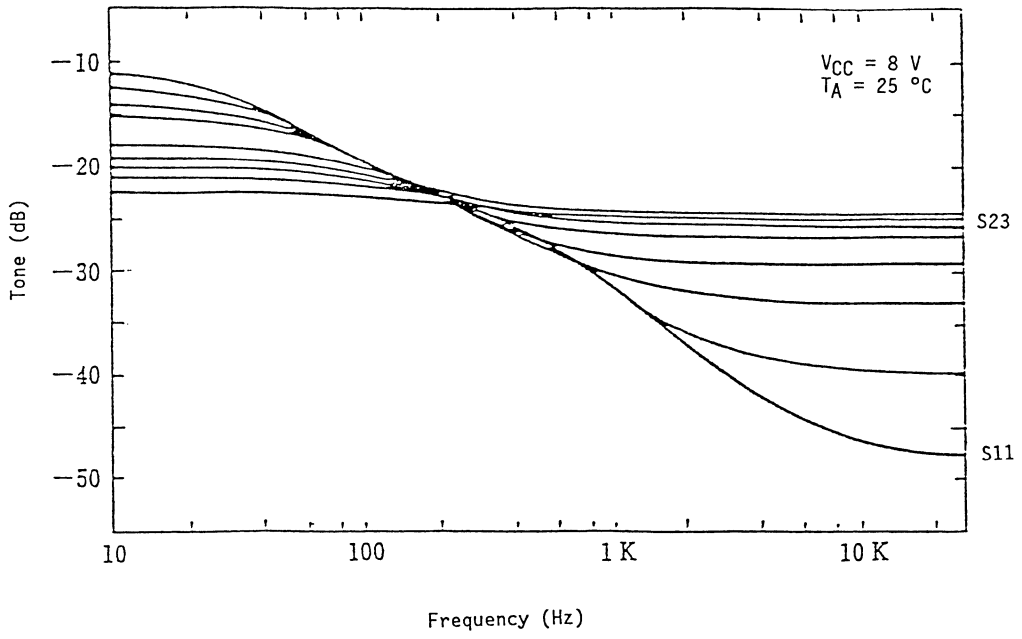
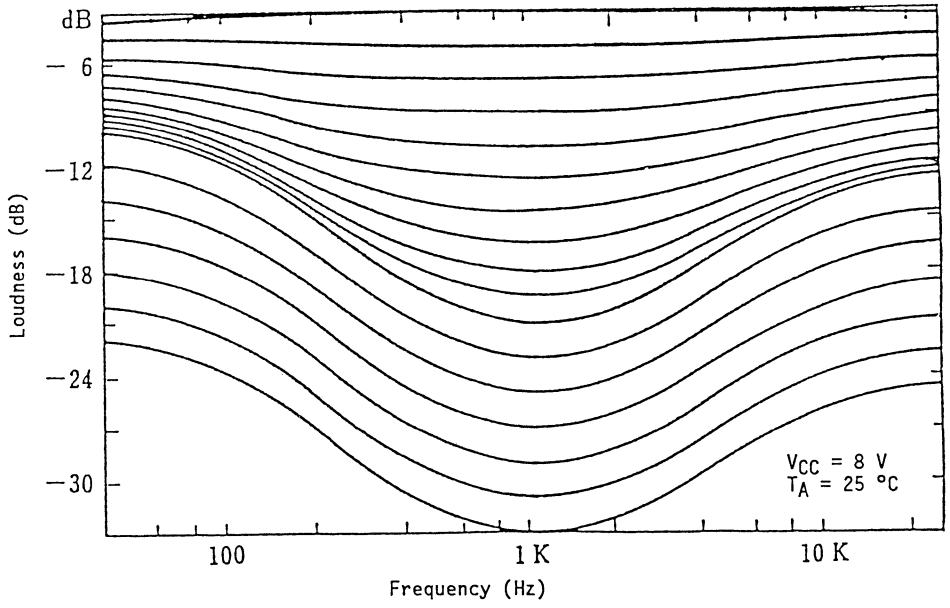
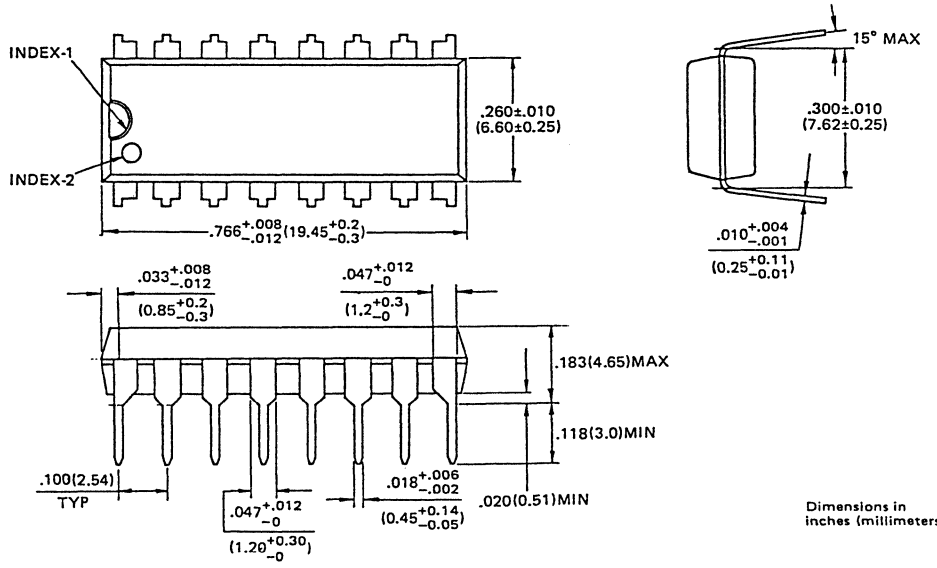


Fig.4 - LOUDNESS VS. FREQUENCY EXAMPLE (Depend on application circuit)



PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M03)



Section 4

Power Supply Controls — *At a Glance*

Page	Device	Description	Features	Power Supply (V)	Package Options
4–3	MB3752	Series Regulator	Load Regulation = 0.03%	+9.5 to +40	14-pin Plastic DIP, FPT 14-pin Ceramic DIP
4–17	MB3756	3-Out Series Voltage Regulator	Fixed (250 mA) Switchable (200/110 mA)	+11 to +16	8-pin Plastic SIP (with Heatsink)
4–25	MB3759	PWM Control Circuit Regulator (200 KHz)	Low Voltage Malfunction Protection 10 = 200 mA Steering Control	+7 to +32	16-pin Plastic DIP, FPT 16-pin Ceramic DIP
4–37	MB3761	Voltage Detector	Reference 1.2 V I_{CC} = 250 mA	+2.5 to +40	8-pin Plastic DIP, SIP, FPT
4–49	MB3769A	PWM Control Circuit Regulator	500 KHz Switching 10 = 600 mA Max.	+12 to +18	16-pin Plastic DIP, FPT
4–67	MB3771	Voltage Detector	V_{CC} On/Off Reset, V_{REF} = 1.24 ±1.5%	+3.5 to +18	8-pin Plastic DIP, SIP, FPT
4–87	MB3773	Voltage Detector	Watchdog timer for Over Protection	+3.5 to +18	8-pin Plastic DIP, SIP, FPT
4–99	MB3774	Car Audio System Power Supply IC	Power Distributor System: SV, 9.15 V, 8.4 V	+10 to +16	17-pin Plastic ZIP
4–111	MB3780A	Battery Backup IC	Dual Alarm, Hysteresis = 100 mV	–0.3 to +7	16-pin Plastic DIP, FPT 20-pin Plastic FPT

4

FUJITSU

VOLTAGE REGULATOR

MB3752

February 1988
Edition 1.0

VOLTAGE REGULATOR

The Fujitsu MB3752 is a monolithic voltage regulator IC. It contains a temperature compensated reference voltage circuit, a surge protected error amplifier and high current protected circuit.

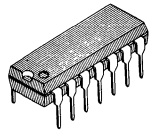
High current regulator, negative power supply regulator, floating regulator and switching regulator are made up by selection of external components.

Constant current limiting or foldback current limiting is selected by selection of external components.

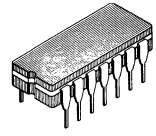
It is suitable both industrial and consumer voltage regulator system.

The high performance makes a lot of application and enables operation with various functions.

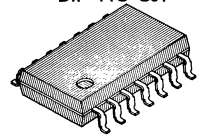
- High Load Regulation: 0.03 % (1 mA ≤ I_L ≤ 50 mA)
- Wide Input Voltage Range: 40 V max.
- Wide Output Voltage Range: 2 V to 37 V
- Compatible with Fairchild μA723
- Packages
  - — 14-pin plastic DIP package (Suffix: -P)
  - — 14-pin ceramic DIP package (Suffix: -Z)
  - — 14-pin plastic Flat package (Suffix: -PF)



PLASTIC PACKAGE
DIP-14P-M02

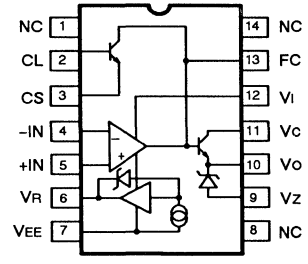


CERAMIC PACKAGE
DIP-14C-C01



PLASTIC PACKAGE
FPT-14P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE) (T_A = 25°C)

Rating	Symbol	Value			Unit
		Ceramic	Plastic	Flat	
Storage Temperature	T_{STG}	-65 ~ +150	-55 ~ +125	-55 ~ +125	°C
Operating Temperature	T_A	-55 ~ +125	-20 ~ +75	-20 ~ +75	°C
Power Dissipation	P_D	1000	800	620 *	mW
Output Current	I_L	150	150	150	mA
Zener Current	I_Z	25	25	25	mA
Current from V_{REF}	I_R	15	15	15	mA
Input Voltage	V_{IN}	40	40	40	V

NOTE: FLAT package is mounted on the epoxy board. (4cm x 4cm x 1.5mm)

Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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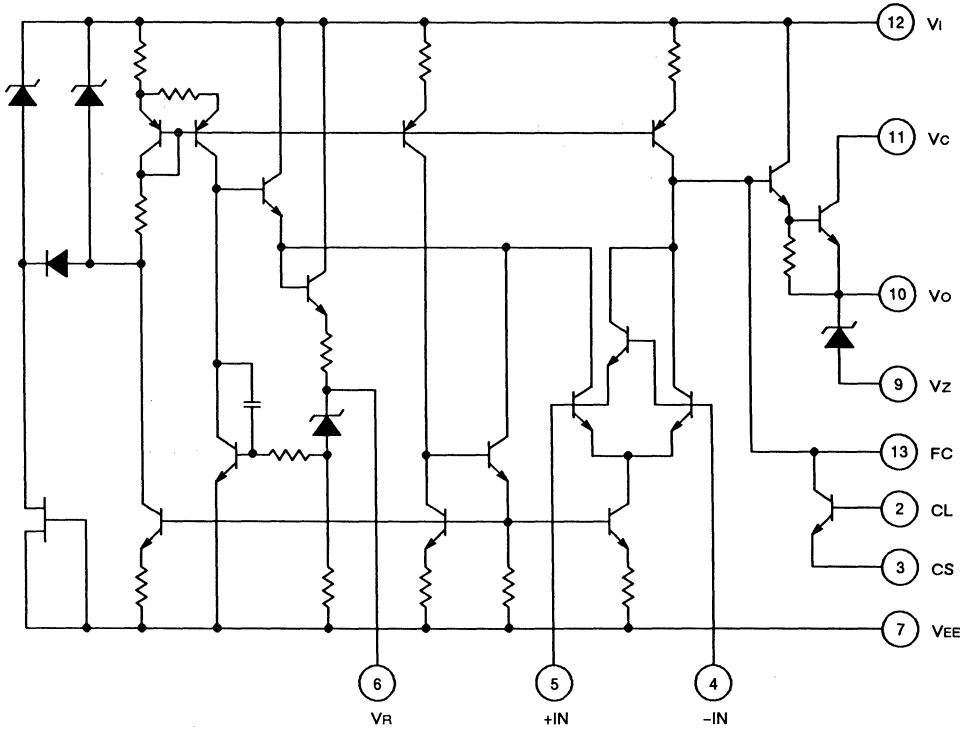
Fig. 1 — MB3752 EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

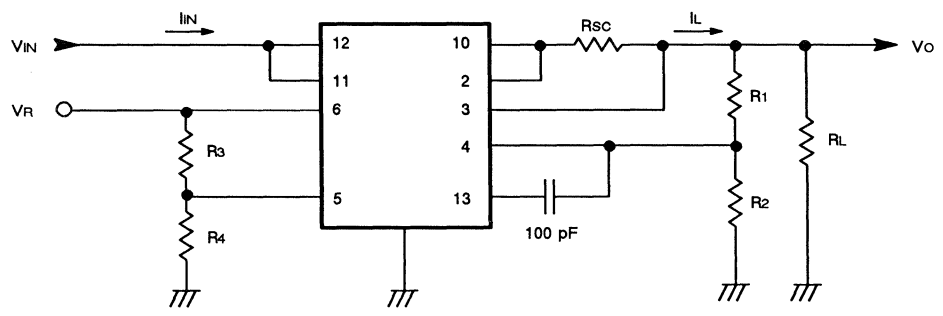
Parameter	Symbol	Value	Unit
Input Voltage	V_{IN}	9.5 to 40	V
Load Current	I_L	1 to 50	mA
Operating Temperature	T_A	-20 to 75	°C

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12 V, I_L = 1 mA, R_{SC} = 0, V_O = 5 V, T_A = 25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Voltage	V_{IN}		9.5		40	V
Output Voltage	V_O		2.0		37	V
Input-to-output Voltage Differential	V_{IN}–V_O		3.0		38	V
Bias Current	I_I	I_L = 0, V_{IN} = 30 V			4.0	mA
Reference Voltage	V_R		6.80	7.15	7.50	V
Input Regulation 1	R_{IN1}	12 V ≤ V_{IN} ≤ 15 V		0.01	0.1	%
Input Regulation 2	R_{IN2}	12 V ≤ V_{IN} ≤ 40 V		0.1	0.5	%
Input Regulation 3	R_{IN3}	12 V ≤ V_{IN} ≤ 15 V, 0°C ≤ T_A ≤ 70°C			0.3	%
Load Regulation 1	R_{LD1}	1 mA ≤ I_L ≤ 50 mA		0.03	0.2	%
Load Regulation 2	R_{LD2}	1 mA ≤ I_L ≤ 50 mA, 0°C ≤ T_A ≤ 70°C			0.6	%
Temperature Regulation	R_T	0°C ≤ T_A ≤ 70°C		0.2	1.0	%
Ripple Rejection Ratio	R.R.	f = 50 Hz to 10 kHz, C_R = 0		74		dB
		f = 50 Hz to 10 kHz, C_R = 5 µF		86		dB
Short Circuit Output Current	I_{SC}	V_O = 0, R_{SC} = 10 Ω	60	70	80	mA

Fig. 2 — MEASUREMENT CIRCUIT



i) $2\ V \leq V_O \leq V_R$ $\quad V_O = V_R \dfrac{R_4}{R_3 + R_4}$, $\quad R_1 = \dfrac{R_3 \cdot R_4}{R_3 + R_4}$, $\quad R_2 = \infty$, $R_3 + R_4 \fallingdotseq 7\ k\Omega$

ii) $V_R \leq V_O \leq 37\ V$ $\quad V_O = V_R \left(1 + \dfrac{R_1}{R_2}\right)$, $\quad R_3 = \dfrac{R_1 \cdot R_2}{R_1 + R_2}$, $\quad R_4 = \infty$, $R_2 \fallingdotseq 7\ k\Omega$

iii) Equations for measurement items

a) $I_B = I_{IN} \left(\begin{matrix} R_1 = 1.5\ k, R_3 = 0, I_L = 0, \\ R_2 = \infty, R_4 = \infty, R_L = \infty \end{matrix} \right)$

b) $R_{IN1} = \dfrac{V_O\ (15\ V) - V_O\ (12\ V)}{V_O\ (12\ V)} \times 100$

c) $R_{IN2} = \dfrac{V_O\ (40\ V) - V_O\ (12\ V)}{V_O\ (12\ V)} \times 100$

d) $R_{LD} = \dfrac{V_O\ (1\ mA) - V_O\ (50\ mA)}{V_O\ (1\ mA)} \times 100$

e) $I_{SC} = I_L \quad (R_L = 0)$

f) $R_T = \dfrac{V_O\ (MAX) - V_O\ (MIN)}{V_O\ (25\ °C)} \times 100$

Note: (b) to (f)
(V_O = 5 V setting, $R_1 = 1.5\ k\Omega$, $R_2 = \infty$, $R_3 = 2.15\ k\Omega$, $R_4 = 5\ k\Omega$, $R_L = 5\ k\Omega$)

TYPICAL CHARACTERISTICS CURVES

Fig. 3 - INPUT-TO-OUTPUT VOLTAGE DIFFERENTIAL vs. MAXIMUM LOAD CURRENT

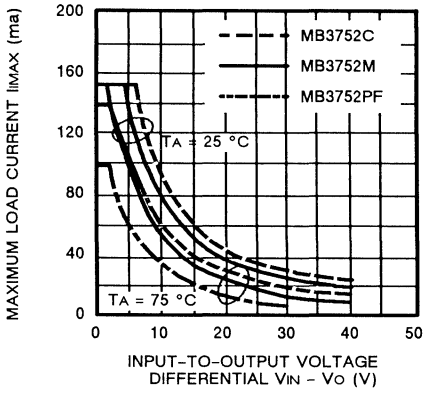


Fig. 4 - INPUT VOLTAGE vs. BIAS CURRENT

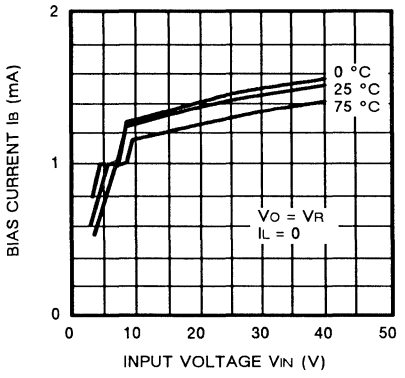


Fig. 5 - LOAD CURRENT vs. LOAD REGULATION

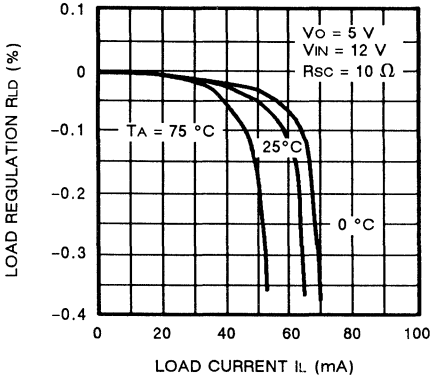
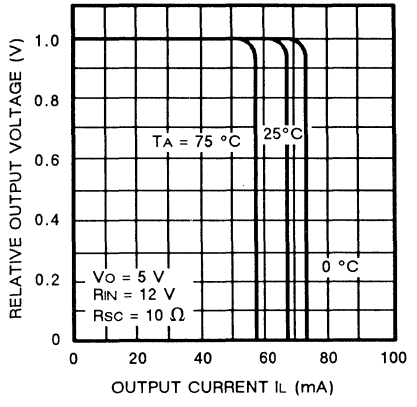


Fig. 6 - CURRENT LIMIT



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TYPICAL CHARACTERISTICS CURVES (Continued)

Fig. 7 - LOAD CURRENT vs. LOAD REGULATION

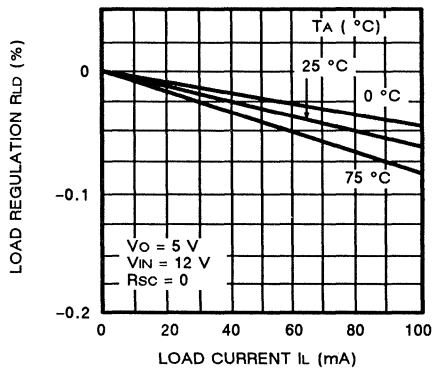


Fig. 8 - JUNCTION TEMPERATURE vs. CURRENT LIMIT SENSE VOLTAGE

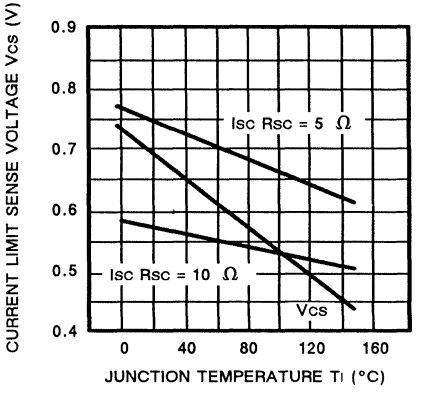


Fig. 9 - INPUT-TO-OUTPUT VOLTAGE DIFFERENTIAL vs. LINE REGULATION

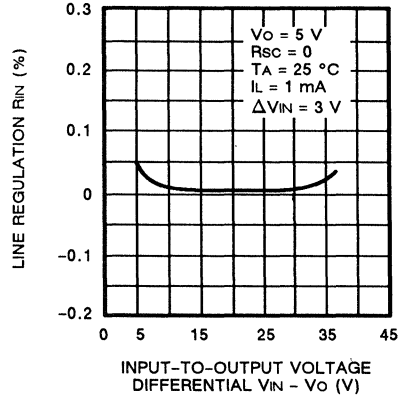
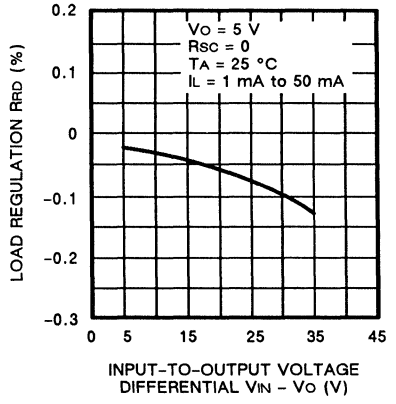


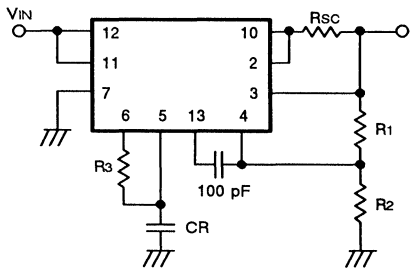
Fig. 10 - INPUT-TO-OUTPUT VOLTAGE DIFFERENTIALvs. LOAD REGULATION



APPLICATION EXAMPLES

Fig. 11 - BASIC HIGH VOLTAGE REGULATOR

$V_R \leq V_O \leq 37$ V

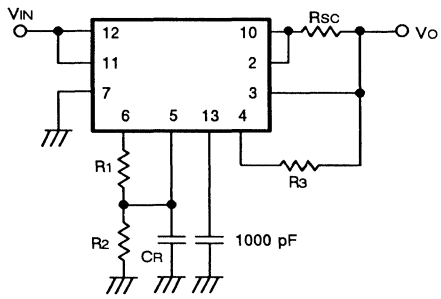


$$V_O = V_R \cdot \frac{R_1 + R_2}{R_2}$$

$$R_3 = \frac{R_1 \cdot R_2}{R_1 + R_2}$$ for minimum temperature drift

Fig. 12 - BASIC LOW VOLTAGE REGULATOR

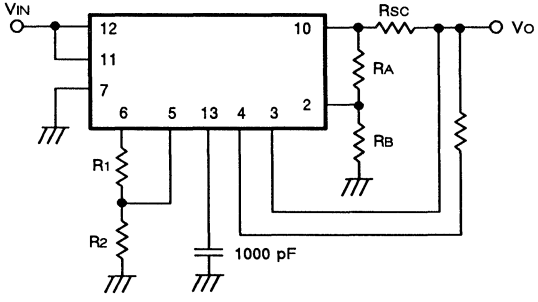
$2\ V \leq V_O \leq V_R$

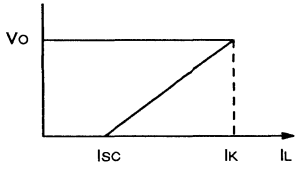


$$V_O = V_R \cdot \frac{R_2}{R_1 + R_2}$$

$$R_3 = \frac{R_1 \cdot R_2}{R_1 + R_2}$$ for minimum temperature drift

Fig. 13 - FOLDBACK CURRENT LIMITING REGULATOR





$I_L \leq I_K \quad V_O = V_R \cdot \frac{R_2}{R_1 + R_2}$

$$R_3 = \frac{R_1 \cdot R_2}{R_1 + R_2}$$ for minimum temperature drift

$$V_O = \frac{R_B \cdot R_{SC}}{R_A} \cdot I_L - V_{SC}\left(1 + \frac{R_B}{R_A}\right)$$

$$I_{SC} = \frac{V_{SC}}{R_{SC}} \cdot \left(1 + \frac{R_A}{R_B}\right), \quad V_{SC} \fallingdotseq 0.7\ V$$

$$I_K = I_{SC} + \frac{V_O}{R_{SC}} \cdot \frac{R_A}{R_B}$$

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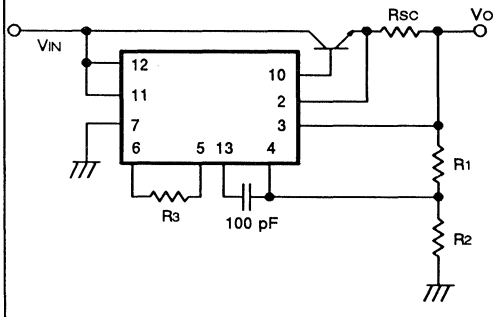
APPLICATION EXAMPLES (Continued)

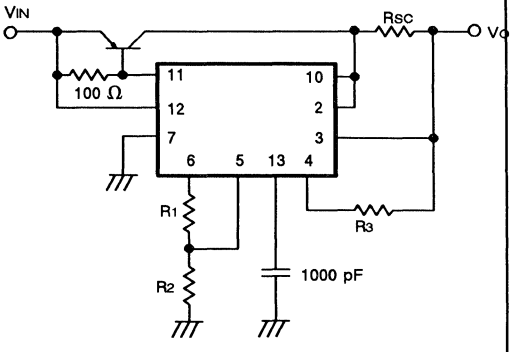
Fig. 14 - POSITIVE VOLTAGE REGULATOR NPN TRANSISTOR



$$V_O = V_R \cdot \frac{R_1 + R_2}{R_2}$$

$$R_3 = \frac{R_1 \cdot R_2}{R_1 + R_2}$$ for minimum temperature drift

Fig. 15 - POSITIVE VOLTAGE REGULATOR PNP TRANSISTOR

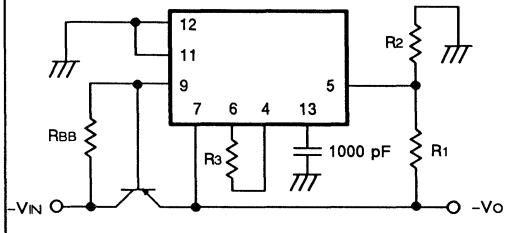


$$V_O = V_R \cdot \frac{R_2}{R_1 + R_2}$$

$$R_3 = \frac{R_1 \cdot R_2}{R_1 + R_2}$$ for minimum temperature drift

Fig. 16 - NEGATIVE VOLTAGE REGULATOR

$|V_O| \geq 9.5$ V

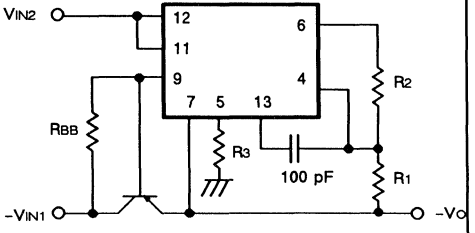


$$V_O = V_R \cdot \left(1 + \frac{R_2}{R_1}\right)$$

$$R_3 = \frac{R_1 \cdot R_2}{R_1 + R_2}$$ for minimum temperature drift

Fig. 17 - NEGATIVE VOLTAGE REGULATOR

$0 \leq |V_O| \leq V_R$



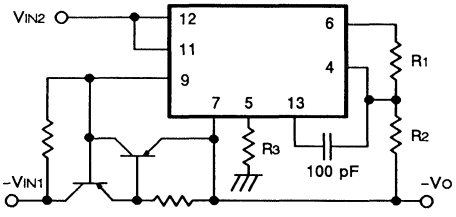
$$V_O = \frac{V_R}{(1 + R_2/R_1)}, \quad V_{IN2} + V_O \geq 9.5 \text{ V}$$

$$R_3 = \frac{R_1 \cdot R_2}{R_1 + R_2}$$ for minimum temperature drift

APPLICATION EXAMPLES (Continued)

Fig. 18 - NEGATIVE VOLTAGE REGULATOR (CURRENT LIMITING)

$0 \leq |V_O| \leq V_R$



$I_L = \frac{V_{CS}}{R_{SC}}$ ($V_{CS} \fallingdotseq 0.7$ V, $V_O = 0$)

$I_L = \frac{V_R}{(1 + R_2/R_1)}$, $V_{IN2} + V_O \geq 9.5$V

$R_3 = \frac{R_1 \cdot R_2}{R_1 + R_2}$ for minimum temperature drift

Fig. 19 - SWITCHING REGULATOR

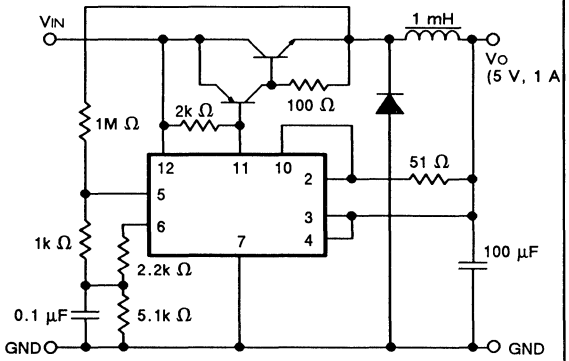


Fig. 20 DUAL TRACKING REGULATOR (CURRENT LIMITING)

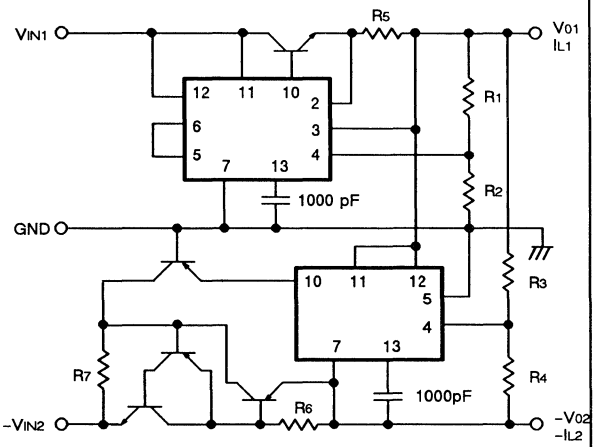
$V_{O1} = V_R \left(1 + \frac{R_1}{R_2}\right)$ $V_{O1} \geq V_R$

$V_{O2} = \frac{R_4}{R_3} V_{O1}$ $V_{O1} + V_{O2} \geq 40$ V

$I_{L1MAX} \fallingdotseq \frac{0.7}{R_5}$

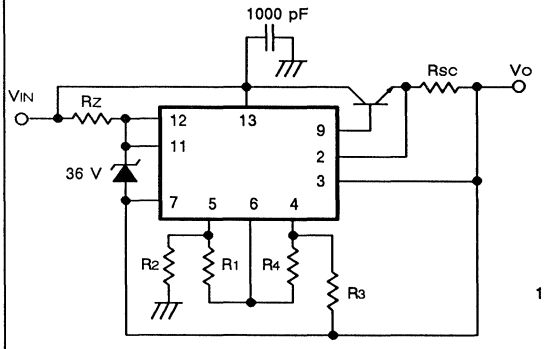
$I_{L2MAX} \fallingdotseq \frac{0.6}{R_5}$

Example for ±15V, ±1A
$R_1 = 8.2k\ \Omega$
$R_2 = 7.5k\ \Omega$
$R_3 = 15k\ \Omega$
$R_4 = 15k\ \Omega$
$R_5 = R_6 = 0.39\ \Omega$
$R_7 = 2k\ \Omega$



APPLICATION EXAMPLES (Continued)

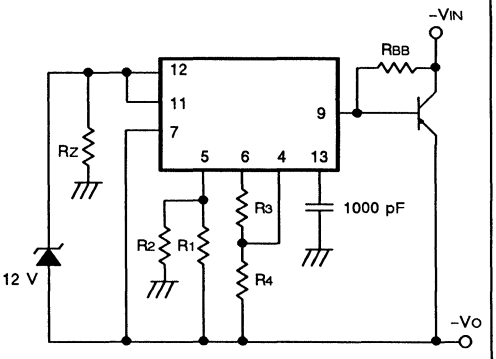
Fig. 21 - POSITIVE FLOATING VOLTAGE REGULATOR



$R_3 = R_4 = 3.3k\ \Omega$

$V_O = V_R \cdot \frac{R_2 - R_1}{2R_1}$

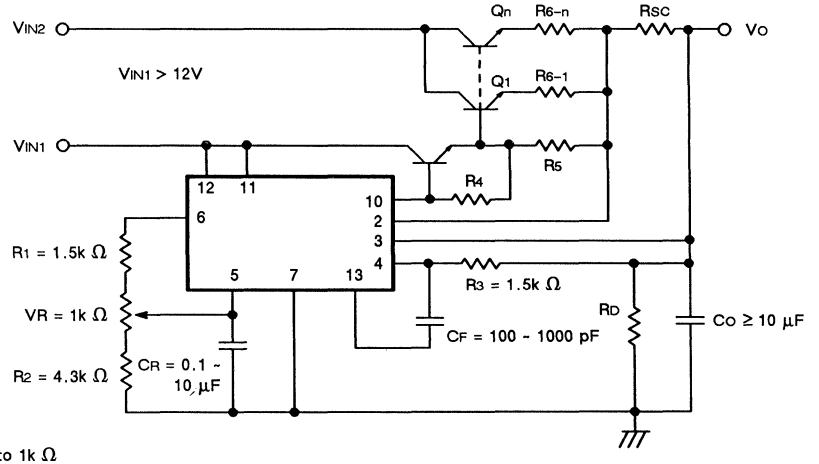
Fig. 22 - NEGATIVE FLOATING VOLTAGE REGULATOR



$R_3 = R_4 = 3.3k\ \Omega$

$V_O = V_R \cdot \frac{R_1 + R_2}{2R_1}$

Fig. 23 - 5 V HIGH CURRENT VOLTAGE REGULATOR



$R_4 = 100\ \Omega$ to $1k\ \Omega$

$R_5 = 10\ \Omega$ to $100\ \Omega$

$$I_{LMAX} = \frac{V_{CS}}{R_{SC}} \left(\begin{array}{c} V_{CS} \fallingdotseq 0.7\ V \text{ at } 25\ °C \\ \Delta V_{CS}/\Delta T_j = -2\ mV/\ °C \end{array} \right)$$

$$V_{IN2} > V_{OMAX} + V_{CESATOUT} + R_{SC} \cdot I_{LMAX} + \frac{1}{n} - R_6 \cdot I_{LMAX} + \frac{V_{IN2P}}{2}$$

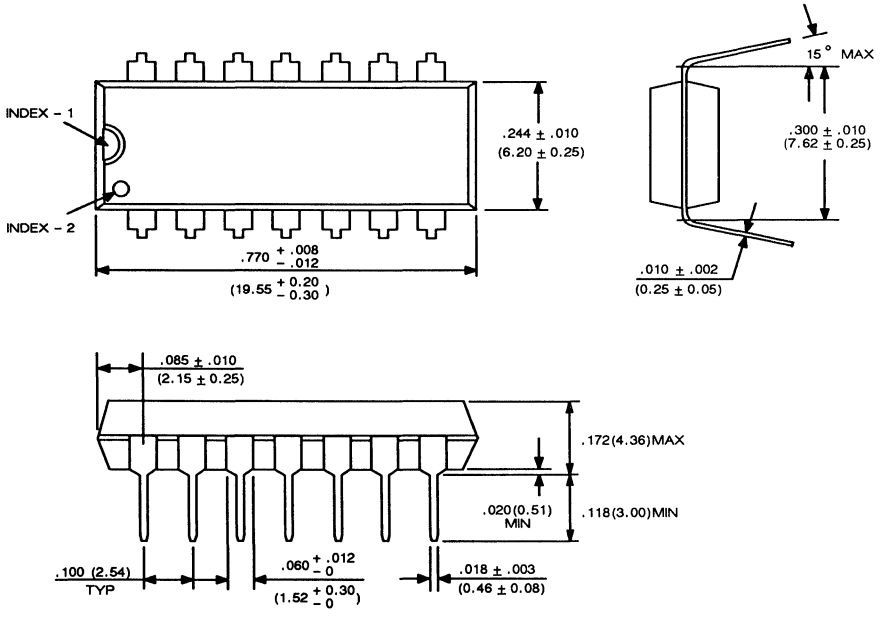
$V_{CESATOUT}$: Maximum value between Q_1 to Q_n

R_6 : $R_{6-1} = R_{6-2} \ldots\ldots = R_{6-n} = R_6$

V_{IN2P} : Maximum ripple amplitude of V_{IN2}

PACKAGE DIMENSIONS

14-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-14P-M02)



Dimensions in
inches (millimeters)

D14010S-3C

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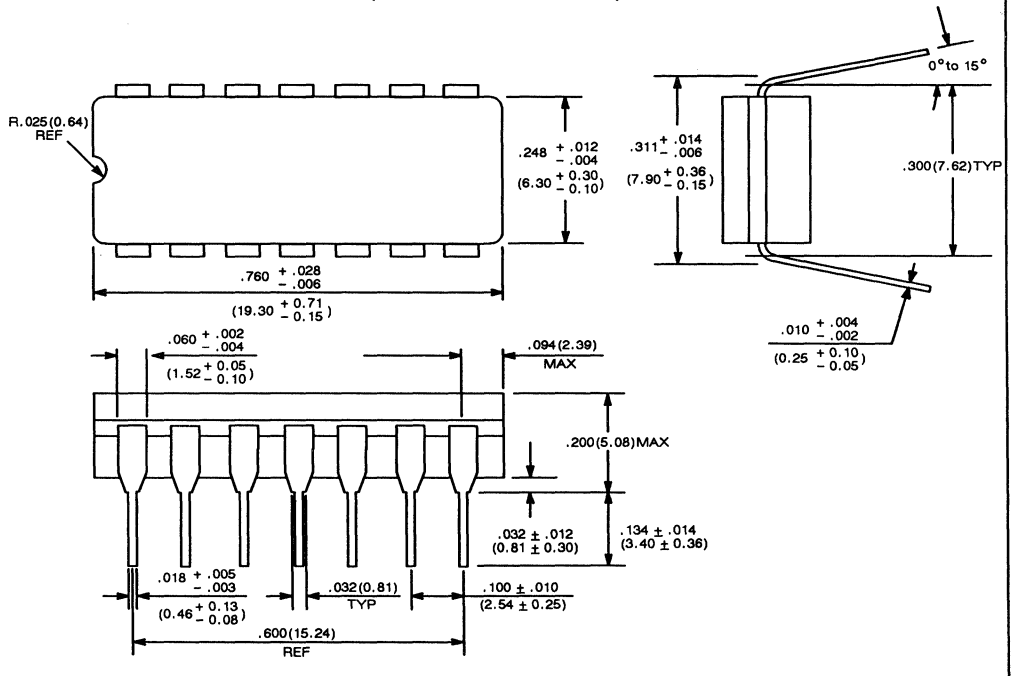
PACKAGE DIMENSIONS (Continued)

14-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(CASE NO.: DIP-14C-CO1)

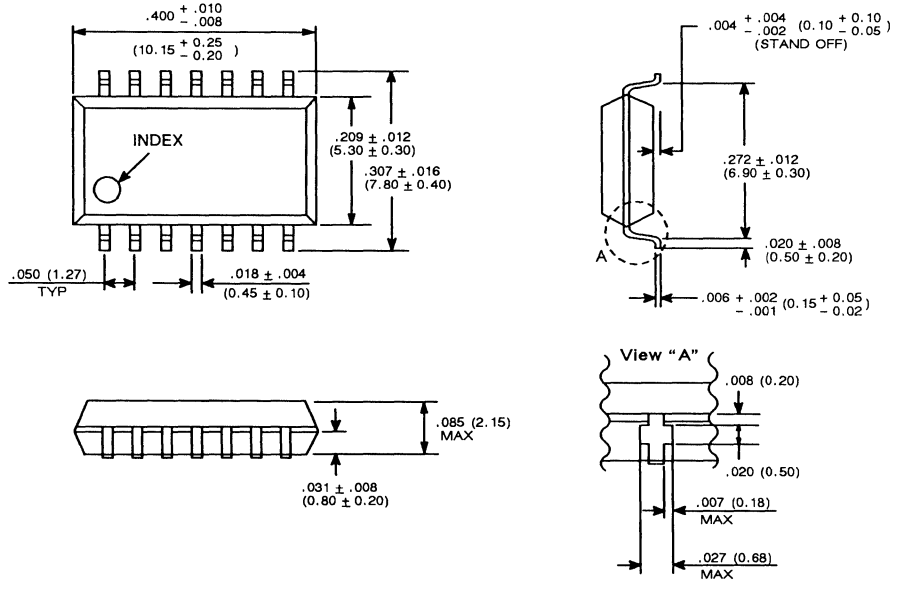


Dimensions in
inches (millimeters)

D14005S-2C

PACKAGE DIMENSIONS (Continued)

14-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-14P-M01)



Dimensions in
inches (millimeters)

F14003S-2C

4

FUJITSU

VOLTAGE REGULATOR

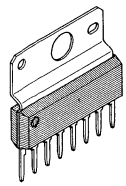
MB3756

May 1988
Edition 2.0

VOLTAGE REGULATOR

The Fujitsu MB3756 monolithic voltage regulator with three outputs is fabricated with a bipolar linear IC technology. Two alternately exchangeable outputs are provided for two stabilized output levels and controlled by an external control signal. Switching noise is prevented by internal circuitry that is suitable for switching between modes such as transmitting and receiving or AM and FM. The MB3756 is packaged in as 8-pin single-in-line package with a heat radiation fin to allow large power consumption.

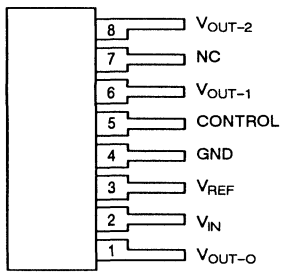
- No need for external components
- Good balance between three outputs
- On-chip noise protection circuitry
- On-chip overload current protection and thermal protection circuitry
- Good mountability
- High output current : 200 mA typical for V_{O2} output
  : 100 mA typical for V_{O0}, V_{O1} outputs



PLASTIC PACKAGE
SIP-08P-M01

PIN ASSIGNMENT

(FRONT VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

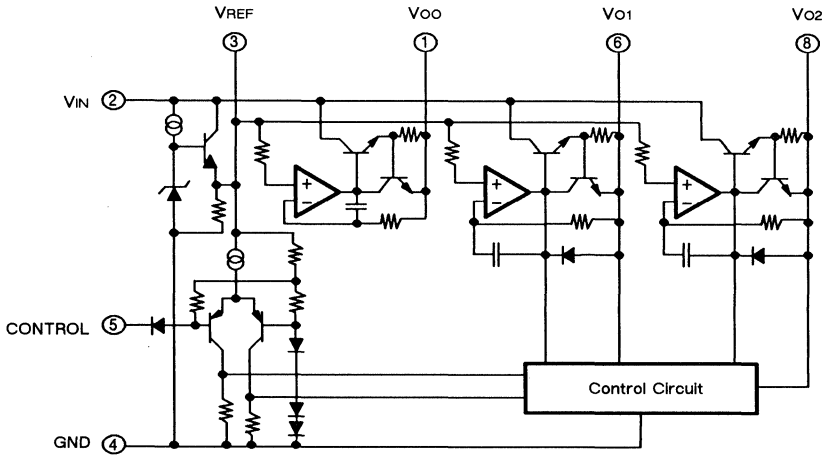
ABSOLUTE MAXIMUM RATINGS (see NOTE) TA = 25°C

Rating	Symbol	Value	Unit
Input Voltage	V_{IN}	18	V
Power Dissipation	P_D	1 *1	W
		4 *2	W
Operating Temperature	T_C	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +125	°C

Notes: *1 No Heat Sink (TA ≤ 70°C)
*2 Infinite Heat Sink (TA ≤ 70°C)
Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4

Fig. 1 — MB3756 EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Voltage	V_{IN}	11	–	16	V
Load Current	I_{L1} *1	0	–	100	mA
	I_{L2} *2	0	–	200	mA
Operating Temperature	T_C	-20	–	+75	°C

Note : *1 V00, V01
*2 V02

ELECTRICAL CHARACTERISTICS

(T_C = 25°C, V_{IN} = 14 V, R_{L0} = R_{L1} =200 Ω, R_{L2} = 100 Ω)

Parameter	Symbol	Condition	Values			Unit
			Min	Typ	Max	
Input Voltage	V_{IN}	—	10.6	—	18	V
Output Voltage	V_O	—	7.8	8.2	8.6	V
Input Regulation	—	11 V ≤ V_{IN} ≤ 18 V	—	20	100	mV
Load Regulation	—	(V_{00}, V_{01}) 1 mA ≤ I_L ≤ 100 mA	—	15	80	mV
	—	(V_{02}) 1 mA ≤ I_L ≤ 200 mA	—	20	100	mV
	—	(V_{00}, V_{01}) 1 mA ≤ I_L ≤ 100 mA VIN = 11.5 V	—	20	100	mV
	—	(V_{02}) 1 mA ≤ I_L ≤ 200 mA V_{IN} = 11.5 V	—	30	150	mV
Bias Current	I_B	V_{IN} = 18 V	—	6	10	mA
Ripple Rejection Ratio	—	f = 100 Hz	—	60	—	dB
Output Noise Voltage	—	10 Hz ≤ f ≤ 100kHz, C_R = 10 μF	—	40	—	μV
Input to Output Voltage Differential	V_{IN}-V_O	—	—	1.7	—	V
Temperature Coefficient of Output Voltage	TCV_O	—	—	-0.4	—	mV/C°
Output Voltage Deviation	ΔV_O	—	—	10	50	mV
Short Circuit Output Current	I_{SC}	(V_{00},V_{01})	—	200	—	mA
		(V_{02})	—	350	—	mA
Output Voltage	V_{01L}	V_{IC} = 0.8 V	0	—	0.2	V
	V_{02L}	V_{IC} = 0.8 V	7.8	8.2	8.6	V
	V_{01H}	V_{IC} = 2.0 V	7.8	8.2	8.6	V
	V_{02H}	V_{IC} = 2.0 V	0	—	0.2	V
Control Input Current	I_{IL}	V_{ICL} = 0 V	—	-0.2	-1.0	mA
	I_{IH}	V_{ICH} = 18V, V_{IN} = 18V	—	—	10	μA

4

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 2 — BIAS CURRENT vs INPUT VOLTAGE

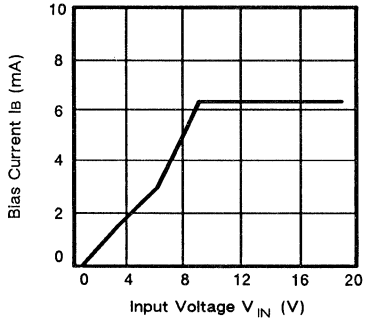


Fig.3 — INPUT TO OUTPUT VOLTAGE DIFFERENTIAL vs JUNCTION TEMPERATURE

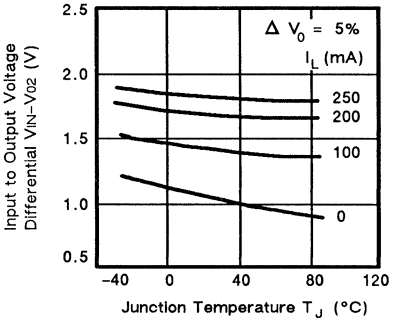


Fig. 4 — OUTPUT NOISE VOLTAGE vs EXTERNAL CAPACITANCE

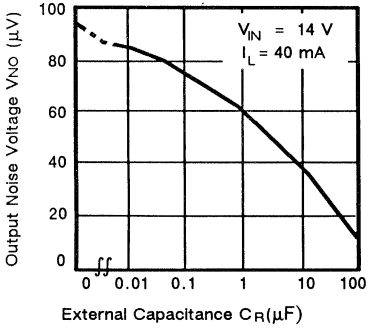
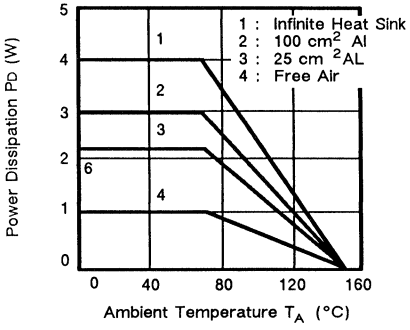


Fig. 5 — POWER DISSIPATION CURVES



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig.6 —OUTPUT VOLTAGE vs INPUT VOLTAGE

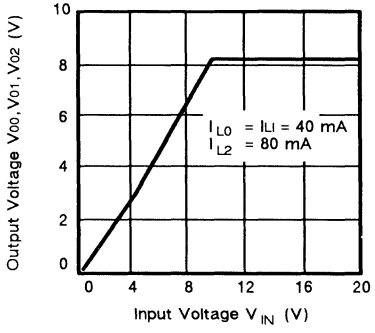


Fig.7 — OUTPUT VOLTAGE DEVIATION vs INPUT VOLTAGE

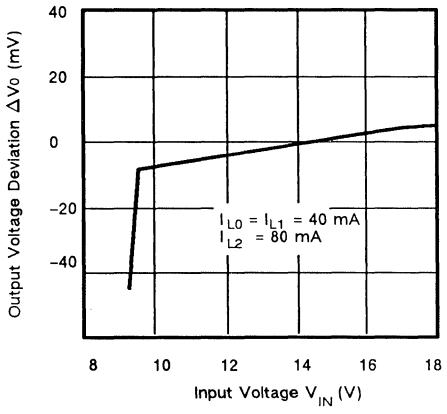


Fig.8 — OUTPUT VOLTAGE vs LOAD CURRENT

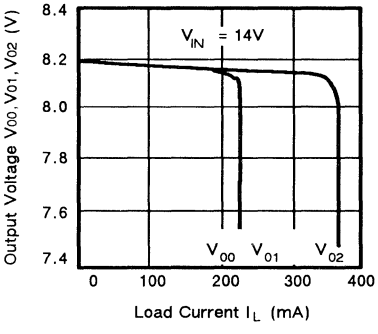
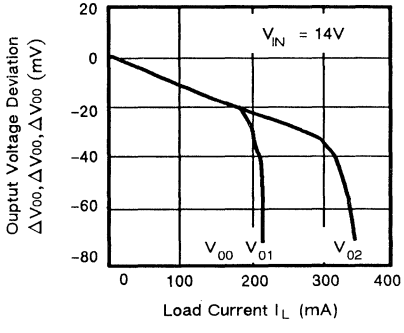


Fig. 9 — OUTPUT VOLTAGE DEVIATION vs LOAD CURRENT



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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig.10 — OUTPUT VOLTAGE vs CONTROL INPUT VOLTAGE

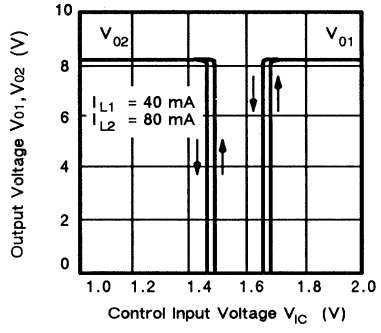


Fig. 11 — CONTROL INPUT CURRENT vs CONTROL INPUT VOLTAGE

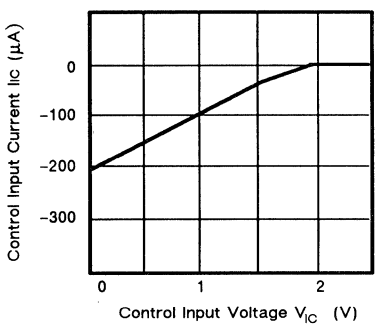
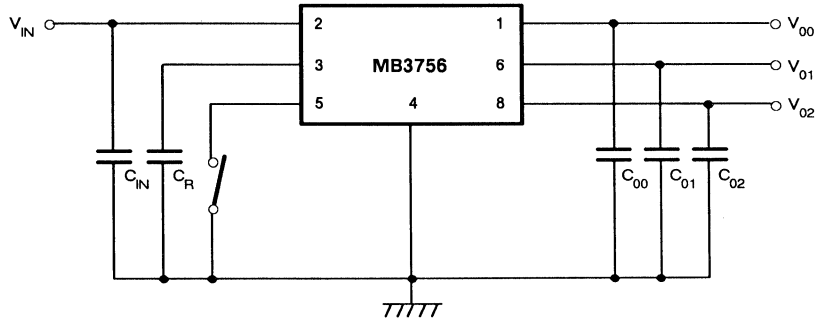


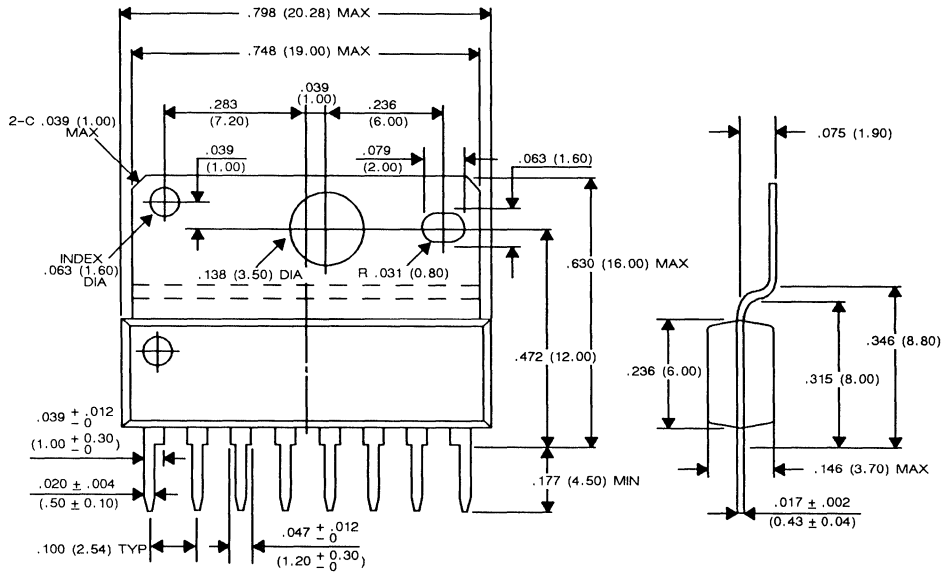
Fig. 12 — APPLICATION CIRCUIT



Note: C_{IN} is required if the regulator is located at a distance from the power supply filter.
C_L improves output noise and ripple rejection.
C_{00}, C_{01}, C_{02} improve transient response.

PACKAGE DIMENSIONS

8-LEAD PLASTIC SINGLE-IN-LINE PACKAGE
(CASE No.: SIP-08P-M01)



Dimensions in inches (millimeters)

S08004S-6C

FUJITSU

PULSE-WIDTH-MODULATION CONTROL CIRCUIT

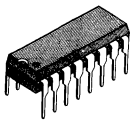
MB 3759

May 1987
Edition 1.0

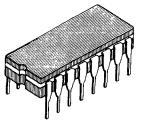
PULSE-WIDTH-MODULATION CONTROL CIRCUIT

The Fujitsu MB 3759 is complete pulse-width modulation control system on a single monolithic chip. The MB 3759 consists of an internal 5.00V reference, two or-connected amplifiers, externally timed (or synchronized) oscillator and control ramp generator. The MB 3759 provides for either push-pull or single-ended mode of operation with external control of dead-band.
The two NPN output transistors have uncommitted emitters and collectors that can be used to either sink or source up to 200 mA each.

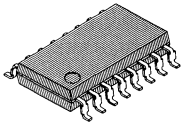
- Complete pulse-width-modulation system with power control circuit
- Either push-pull or single-ended mode of operation
- Internal circuitry prohibits double pulse at either output
- On-chip voltage reference
- Uncommitted output drivers
- Master or slave oscillator control
- Dual error amplifiers
- Under voltage lockout function
- Package: 16-pin Plastic DIP Package
  16-pin Ceramic DIP Package
  16-pin Plastic FPT Package



PLASTIC PACKAGE
DIP-16P-M04



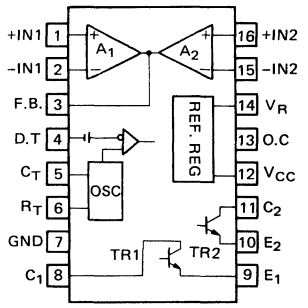
CERAMIC PACKAGE
DIP-16C-C01



PLASTIC PACKAGE
FPT-16P-M02

PIN ASSIGNMENT

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	41	V
Collector Output Voltage		V_{CE}	41	V
Collector Output Current		I_{CE}	250	mA
Amplifier Input Voltage		V_{IN}	V_{CC} + 0.3	V
Power Dissipation	Plastic DIP	P_D	1000 ($T_A \leq 25°C$)	mW
	Ceramic DIP		800 ($T_A \leq 60°C$)	
	Plastic FPT		620 ($T_A \leq 25°C$)*	
Operating Temperature	DIP	T_A	-20 to 85	°C
	FPT		-20 to 75	
Storage Temperature		T_{STG}	-55 to 125	°C

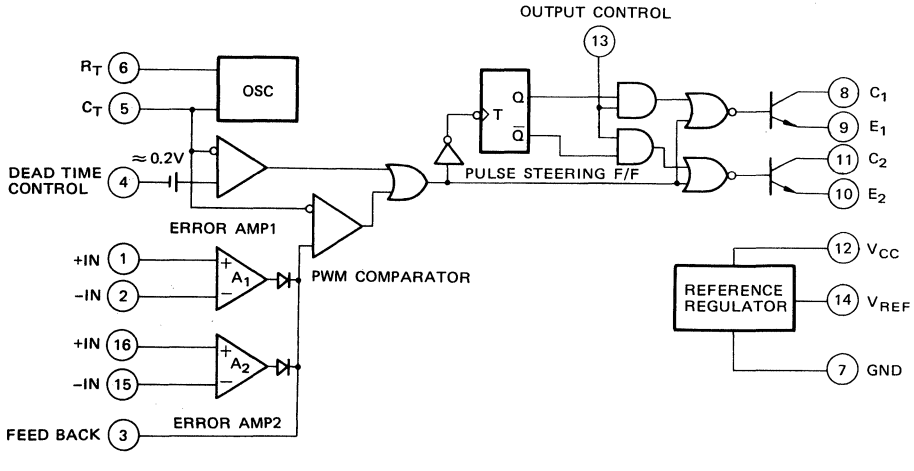
* PFT package is mounted on the epoxy board. (4 cm x 4 cm x 0.15 cm)

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

Fig. 1 – MB 3759 BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	DIP-package			FPT-package			Unit
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage	V_{CC}	7	15	32	7	15	24	V
Collector Output Voltage	V_{CE}			40			40	V
Collector Output Current	I_{CE}	5	100	200	5	50	100	mA
Amplifier Input Voltage	V_{IN}	-0.3	0 to V_{REF}	V_{CC}-2	-0.3	0 to V_{REF}	V_{CC}-2	V
FB Sink Current	I_{SINK}			0.3			0.3	mA
FB Source Current	I_{SOURCE}			2			2	mA
Reference Section Output Current	I_{REF}		5	10		3	10	mA
Timing Resistor	R_T	1.8	30	500	1.8	30	500	kΩ
Timing Capacitor	C_T	470	1000	10^6	470	1000	10^6	pF
Oscillator Frequency	f_{OSC}	1	40	300	1	40	300	kHz
Operating Temperature	T_A	-20	25	85	-20	25	75	°C

Note: These recommended operating conditions are based on the standard condition.
When used at higher supply voltage, careful consideration for the ambient temperature, power consumption and so on is necessary.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 15V)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Reference Section						
Output Voltage	V_{REF}	I_O = 1mA	4.75	5.0	5.25	V
Input Regulation	ΔV_{RIN}	7V ≤ V_{CC} ≤ 40V, T_A = 25°C		2	25	mV
Load Regulation	ΔV_{RLD}	1mA ≤ I_O ≤ 10mA, T_A = 25°C		-1	-15	mV
Temperature Stability	$\Delta V_R/\Delta T$	-20°C ≤ T_A ≤ 85°C		±200	±750	μV/°C
Short Circuit Output Current	I_{SC}		15	40		mA
Reference Lockout Voltage				4.3		V
Reference Hysteresis Voltage				0.3		V

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Oscillator Section						
Oscillator Frequency	f_{OSC}	R_T = 30kΩ, C_T = 1000pF	36	40	44	kHz
Standard Deviation of Frequency		R_T = 30kΩ, C_T = 1000pF		±3		%
Frequency Change with Voltage		7V ≤ V_{CC} ≤ 40V, T_A = 25°C		±0.1		%
Frequency Change with Temperature	$\Delta f_{osc}/\Delta T$	−20°C ≤ T_A ≤ 85°C		±0.01	±0.03	%/°C
Dead-Time Control Section						
Input Bias Current	I_D	0 ≤ V_I ≤ 5.25V		−2	−10	μA
Maximum Duty Cycle (Each Output)		V_I = 0	40	45		%
Input Threshold Voltage — 0% Duty Cycle	V_{DO}			3.0	3.3	V
Input Threshold Voltage — Max. Duty Cycle	V_{DM}		0			V
Effor Amplifier Section						
Input Offset Voltage	V_{IO}	$V_{O(pin3)}$ = 2.5V		±2	±10	mV
Input Offset Current	I_{IO}	$V_{O(pin3)}$ = 2.5V		±25	±250	nA
Input Bias Current	I_I	$V_{O(pin3)}$ = 2.5V		−0.2	−1.0	μA
Common-Mode Input Voltage	V_{CM}	7V ≤ V_{CC} ≤ 40V	−0.3		V_{CC}−2	V
Open-Loop Voltage Amplification	A_V	0.5 ≤ V_O ≤ 3.5V	70	95		dB
Unity-Gain Bandwidth	BW	A_V = 1		800		kHz
Common-Mode Rejection Ratio	CMR	V_{CC} = 40V	65	80		dB
Output Sink Current (3 pin)	I_{SINK}	−5V ≤ V_{ID} ≤ −15mV, V_O = 0.7V	0.3	0.7		mA
Output Source Current (3 pin)	I_{SOURCE}	15mV ≤ V_{ID} ≤ 5V, V_O = 3.5V	−2	−10		mA

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Output Section							
Collector Leakage Current		I_{CO}	V_{CE} = 40V, V_{CC} = 40V			100	μA
Emitter Leakage Current		I_{EO}	V_{CC} = V_C = 40V, V_E = 0V			−100	μA
Collector Emitter Saturation Voltage	Emitter Grounded	V_{SATC}	V_E = 0, I_C = 200mA		1.1	1.3	V
	Emitter Follower	V_{SATE}	V_C = 15V, I_E = −200mA		1.5	2.5	V
Output Control Input Current		I_{OPC}	V_I = V_{REF}		1.3	3.5	mA
PWM Comparator Section							
Input Threshold Voltage		V_{TH}	0% Duty		4	4.5	V
Input Sink Current (3 pin)		I_{SINK}	V_O (pin 3) = 0.7V	0.3	0.7		mA
Total Device							
Power Supply Current		I_{CC}	V4 = 2V, See Fig-2		8		mA
Stand-by Current		I_{CCQ}	$V_{(pin6)}$ = V_{REF}, I/O open		7	12	mA
Switching Characteristics							
Rise Time	Emitter Grounded	t_R	R_L = 68Ω		100	200	ns
Fall Time		t_F	R_L = 68Ω		25	100	ns
Rise Time	Emitter Follower	t_R	R_L = 68Ω		100	200	ns
Fall Time		t_F	R_L = 68Ω		40	100	ns

4

Fig. 2 – TEST CIRCUIT

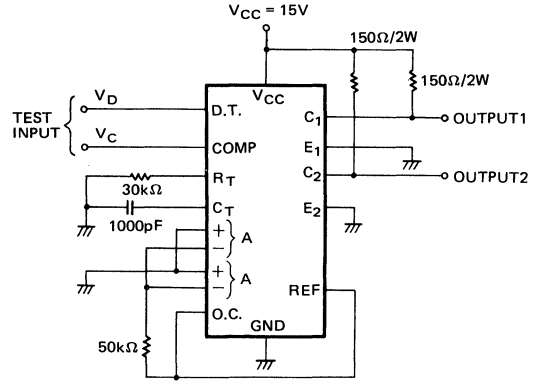
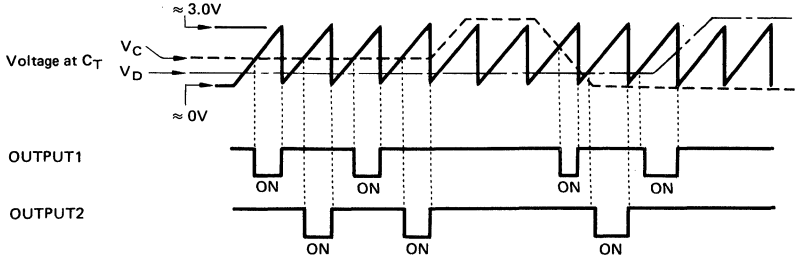


Fig. 3 – OPERATING TIMING



OSCILLATION FREQUENCY

$f_{OSC} \fallingdotseq 1.2/(R_T \cdot C_T)$

R_T : kΩ
C_T : μF
f_{OSC} : kHz

FUNCTION TABLE

Input (Output Control)	Output State
GND	Single-ended or parallel output
V_{REF}	Push-pull

TYPICAL ELECTRICAL CURVES

Fig. 4 – REFERENCE VOLTAGE vs. POWER SUPPLY VOLTAGE

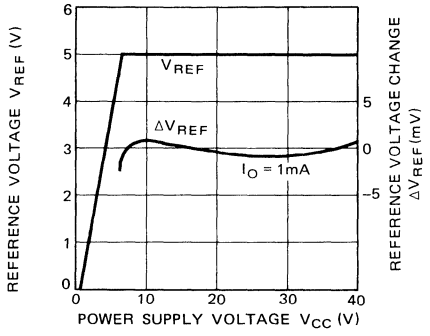


Fig. 5 – REFERENCE VOLTAGE vs. TEMPERATURE

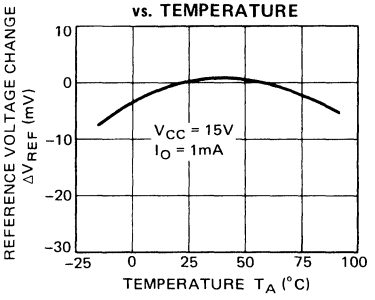


Fig. 6 – OSCILLATOR FREQUENCY vs. R_T, C_T

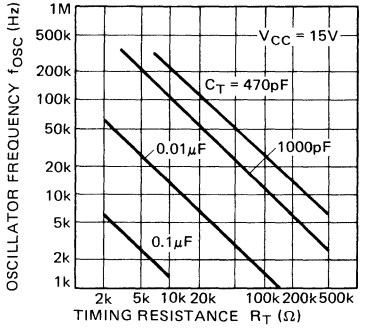


Fig. 7 – DUTY RATIO vs. DEAD TIME CONTROL VOLTAGE

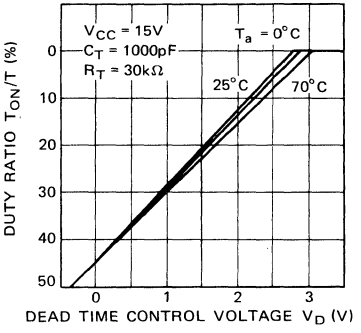


Fig. 8 – OPEN LOOP VOLTAGE AMPLIFICATION vs. FREQUENCY

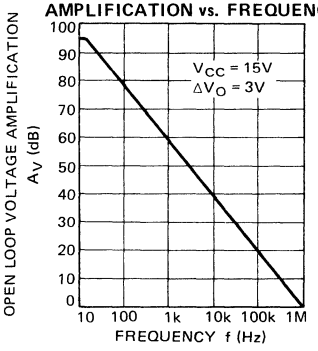
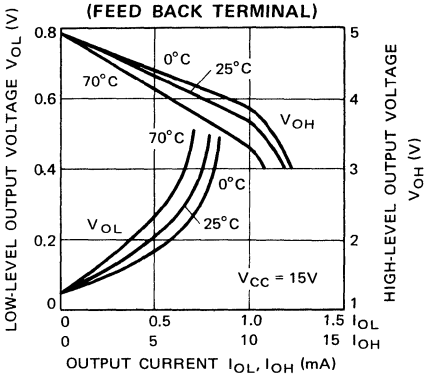


Fig. 9 – OUTPUT VOLTAGE vs. OUTPUT CURRENT (FEED BACK TERMINAL)



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TYPICAL ELECTRICAL CURVES (continued)

Fig. 10 – COLLECTOR SATURATION VOLTAGE vs. COLLECTOR OUTPUT CURRENT

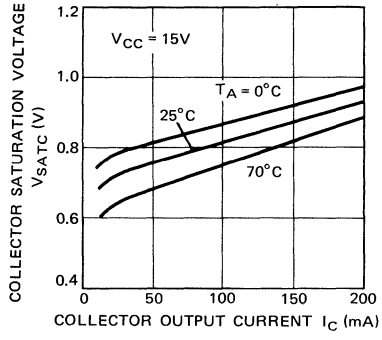


Fig. 11 – EMITTER SATURATION VOLTAGE vs. EMITTER OUTPUT CURRENT

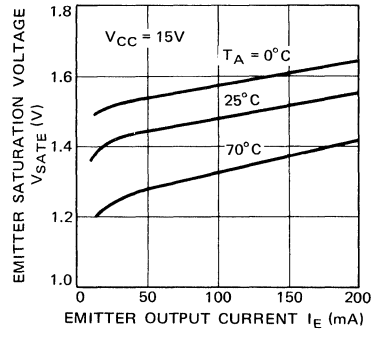


Fig. 12 – OUTPUT VOLTAGE vs. REFERENCE VOLTAGE

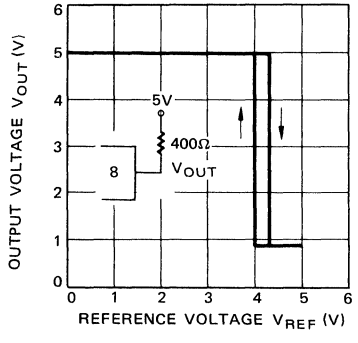


Fig. 13 – POWER SUPPLY CURRENT vs. POWER SUPPLY VOLTAGE

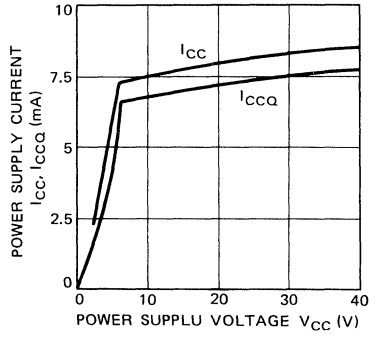


Fig. 14 – POWER DISSIPATION vs. POWER SUPPLY VOLTAGE

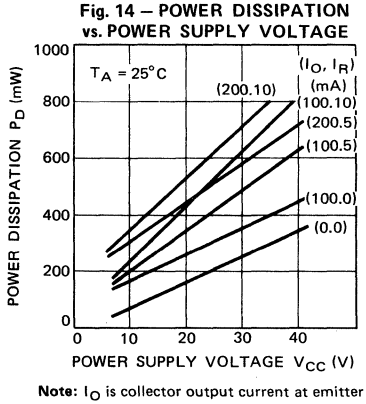
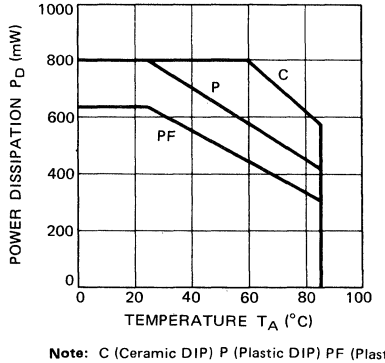


Fig. 15 – AVAILABLE POWER DISSIPATION vs. TEMPERATURE



Note: I_O is collector output current at emitter grounded mode.

Note: C (Ceramic DIP) P (Plastic DIP) PF (Plastic FPT)

TYPICAL APPLICATION

Fig. 16 — Chopper

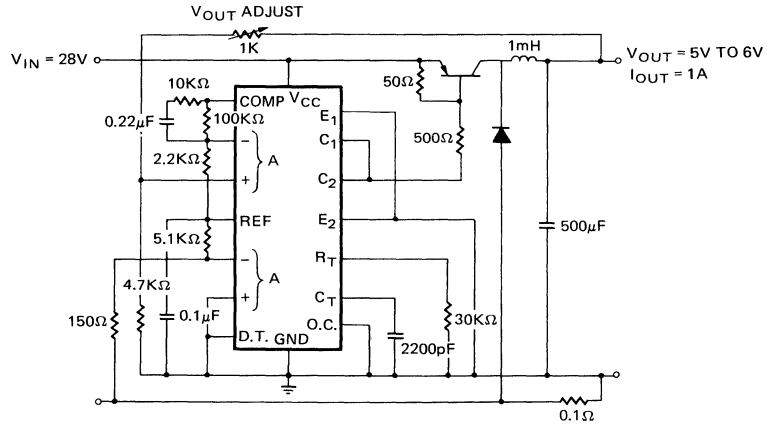
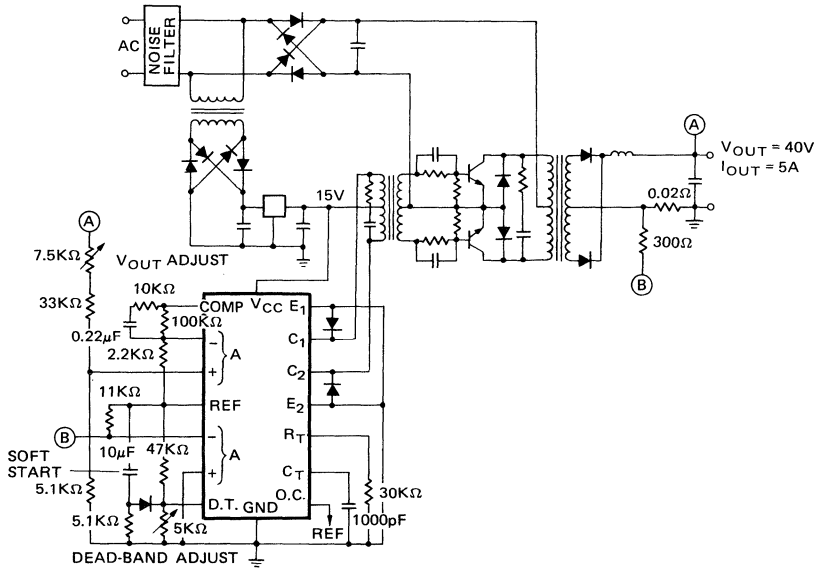
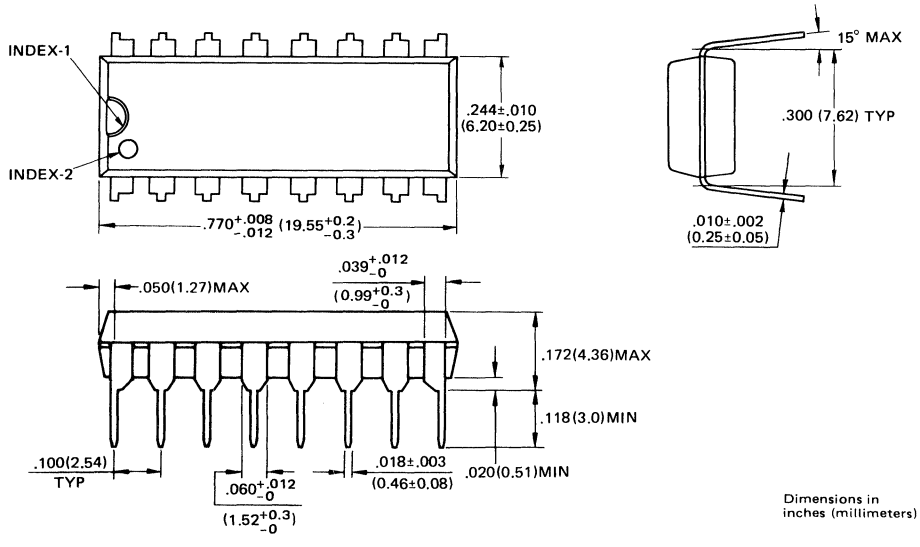


Fig. 17 — Operating from AC line



PACKAGE DIMENSIONS

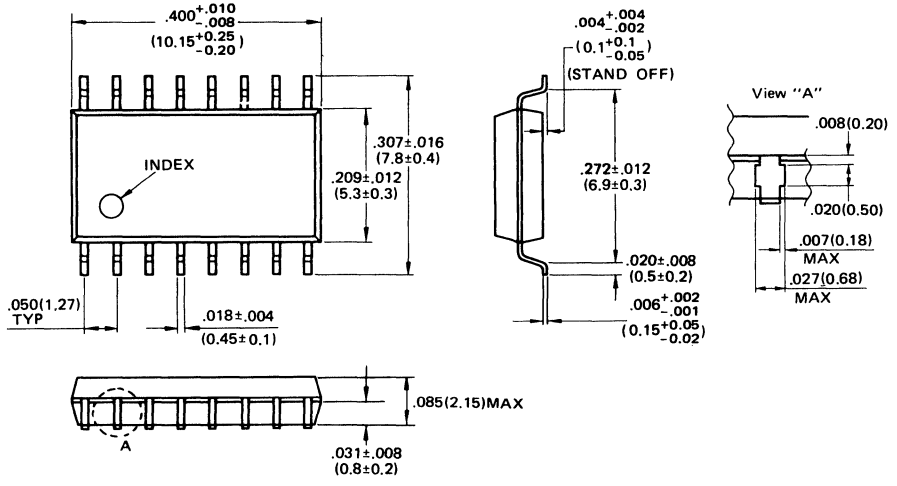
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



Dimensions in
inches (millimeters)

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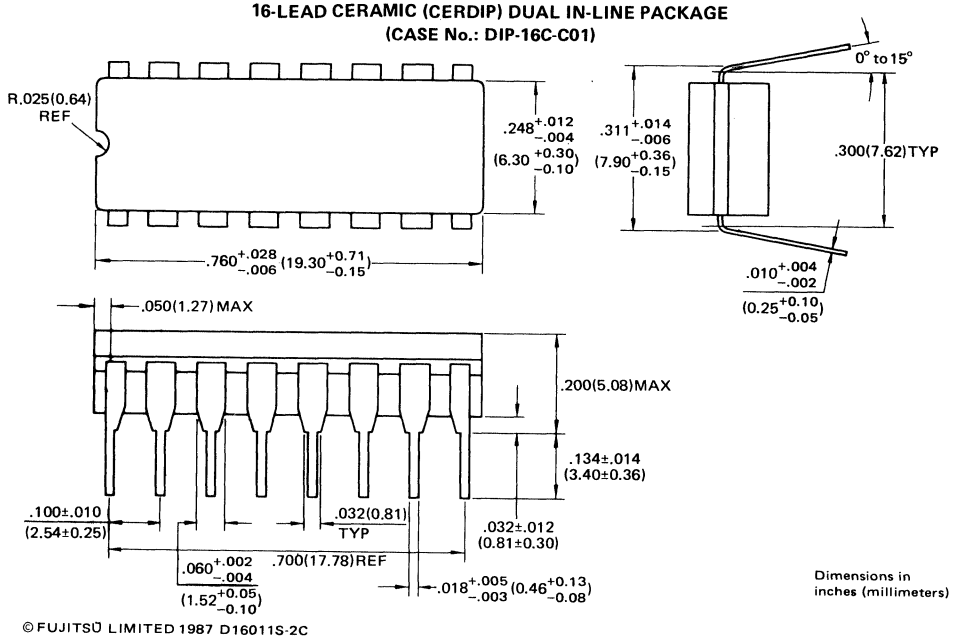
16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-16C-C01)



Dimensions in
inches (millimeters)

FUJITSU

VOLTAGE DETECTOR

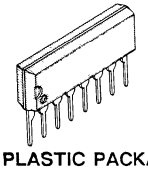
MB3761

October 1987
Edition 1.0

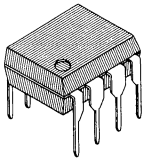
VOLTAGE DETECTOR

Designed for voltage detector applications, the Fujitsu MB3761 is a dual comparator with a built-in high precision reference voltage generator. Outputs are open-collector outputs and enable use of the OR-connection between both channels. Both channels have hysteresis control outputs. Because of a wide power supply voltage range and a low power supply current, the MB3761 is suitable for power supply monitors and battery backup systems.

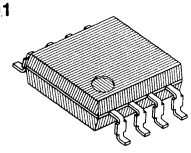
- Wide power supply voltage range: 2.5 V to 40 V
- Low power and small voltage dependency supply current: 250 µA typical.
- Built-in stable low voltage generator: 1.20 V typical.
- Easy-to-add hysteresis characteristics.
- Package: 8-pin Plastic SIP Package (Suffix: -PS)
  8-pin Plastic DIP Package (Suffix: -P)
  8-pin Plastic FPT Package (Suffix: -PF)



PLASTIC PACKAGE
SIP-08P-M03



PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

4

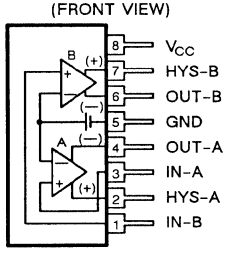
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	41	V
Output Voltage	V_O	41	V
Output Current	I_O	50	mA
Input Voltage	V_{IN}	-0.3 to +6.5	V
Power Dissipation	P_D	350 (TA ≤ 70°C)	mW
Storage Temperature	T_{STG}	-55 to 125	°C

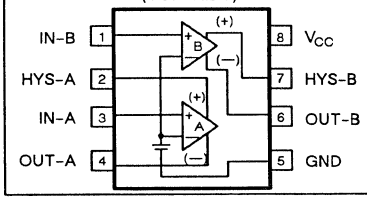
NOTE: Permanent device damage may occur if **ABSOLUTE MAXIMUM RATINGS** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT

(FRONT VIEW)

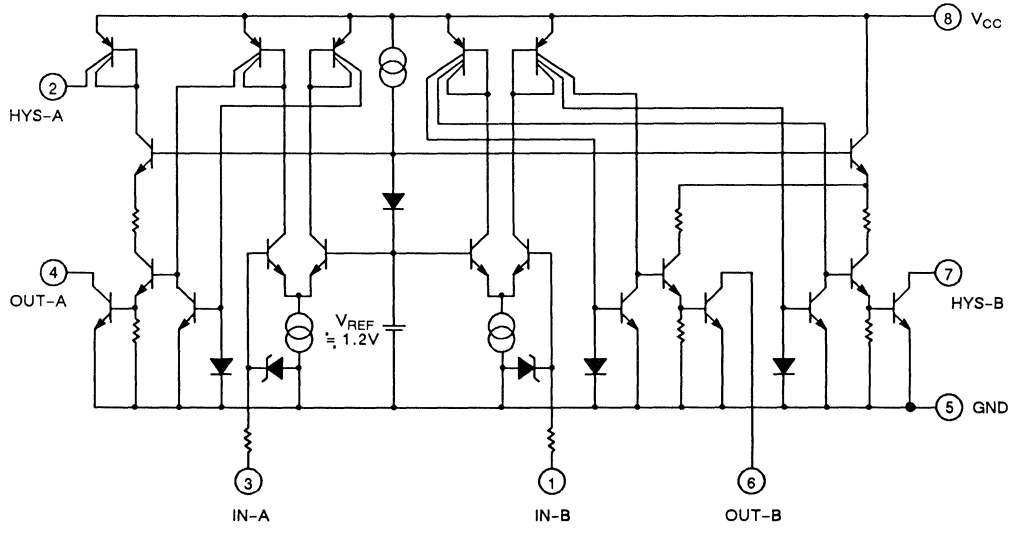


(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Figure 1. MB3761 Equivalent Circuit



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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	2.5 to 40	V
Operating Temperature	T_A	-20 to 75	°C
Output Current at pin 4	I_{O4}	4.5	mA
Output Current at pin 6	I_{O6}	3.0	mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 5V)

Parameter	Designator	Conditions	Values			Unit
			Min	Typ	Max	
Power Supply Voltage	I_{CCL}	V_{CC} = 40 V, V_{IL} = 1.0 V	—	250	400	μA
	I_{CCH}	V_{CC} = 40 V, V_{IH} = 1.5 V	—	400	600	μA
Threshold Voltage	V_{TH}	I_O = 2 mA, V_O = 1 V	1.15	1.20	1.25	V
Deviation of Threshold Voltage	ΔV_{TH1}	2.5 V ≤ V_{CC} ≤ 5.5 V	—	3	12	mV
	ΔV_{TH2}	4.5 V ≤ V_{CC} ≤ 40 V	—	10	40	mV
Offset Voltage between Outputs	V_{OOSA}	I_{OA} = 4.5 mA, V_{OA} = 2 V I_{HA} = 20 μA, V_{HA} = 3 V	—	2.0	—	mV
	V_{OSSB}	I_{OB} = 3 mA, V_{OB} = 2 V I_{HB} = 3 mA, V_{HB} = 2 V	—	2.0	—	mV
Temperature Coefficient of Threshold Voltage	α	-20°C ≤ T_A ≤ 70°C	—	±0.05	—	mV/°C
Difference Voltage on Threshold Voltage between Channel	ΔV_{THAB}		-10	—	10	mV
Input Current	I_{IL}	V_{IL} = 1.0 V	—	5	—	nA
	I_{IH}	V_{IH} = 1.5 V	—	100	500	nA
Output Leakage Current	I_{OH}	V_O = 40 V, V_{IL} = 1.0 V	—	—	1	μA
Hysteresis Output Leakage Current	I_{HLA}	V_{CC} = 40 V, V_{HA} = 0 V, V_{IL} = 1.0 V	—	—	0.1	μA
	I_{HHB}	V_{HB} = 40 V, V_{IH} = 1.5 V	—	—	1	μA
Output Sink Current	I_{OLA}	V_O = 1.0 V, V_{IH} = 1.5 V	6	12	—	mA
	I_{OLB}	V_O = 1.0 V, V_{IH} = 1.5 V	4	10	—	mA
Hysteresis Current	I_{HHA}	V_H = 0 V, V_{IH} = 1.5 V	40	80	—	μA
	I_{HLB}	V_H = 1.0 V, V_{IL} = 1.0 V	4	10	—	mA
Output Saturation Voltage	V_{OLA}	I_O = 4.5 mA, V_{IH} = 1.5 V	—	120	400	mV
	V_{OLB}	I_O = 3.0 mA, V_{IH} = 1.5 V	—	120	400	mV
Hysteresis Saturation Voltage	V_{HHA}	I_H = 20 μA, V_{IH} = 1.5 V	—	50	200	mV
	V_{HLB}	I_H = 3.0 mA, V_{IL} = 1.0 V	—	120	400	mV
Output Delay Time	t_{PHL}	R_L = 5 KΩ	—	2	—	μs
	t_{PLH}	R_L = 5 KΩ	—	3	—	μs

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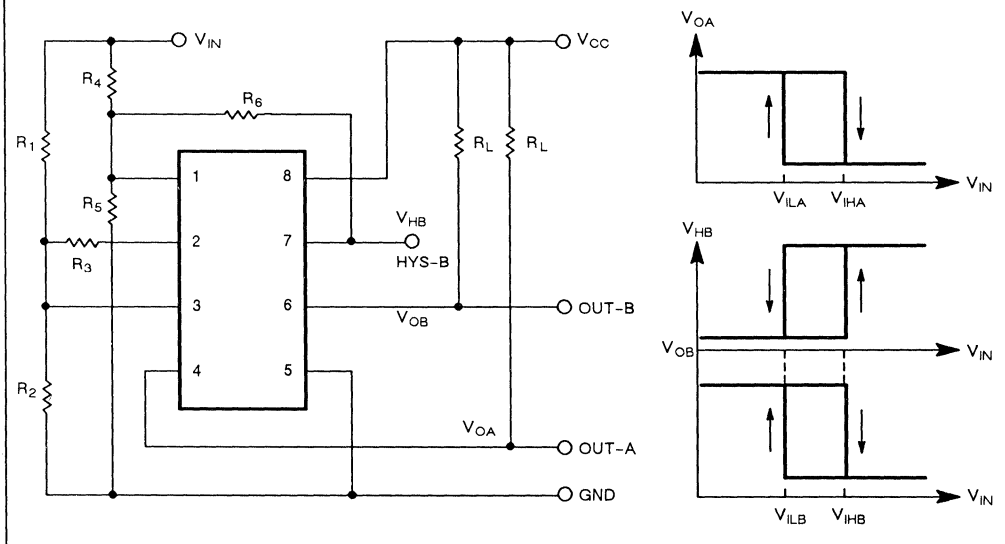
Figure 2. Operational Definitions



$V_{IHA} = (1 + \frac{R_1}{R_2}) V_R$

$V_{ILA} = (1 + \frac{R_1}{R_2 // R_3}) V_R - \frac{R_1}{R_3} V_{CC}$

$V_{IHB} = (1 + \frac{R_4}{R_5 // R_6}) V_R$

$V_{ILB} = (1 + \frac{R_4}{R_5}) V_R$

$V_R \fallingdotseq V_{TH} (\fallingdotseq 1.20V)$

$R_2 // R_3 = \frac{R_2 R_3}{R_2 + R_3}$

$R_5 // R_6 = \frac{R_5 R_6}{R_5 + R_6}$

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 3 – Power Supply Current vs Power Supply Voltage

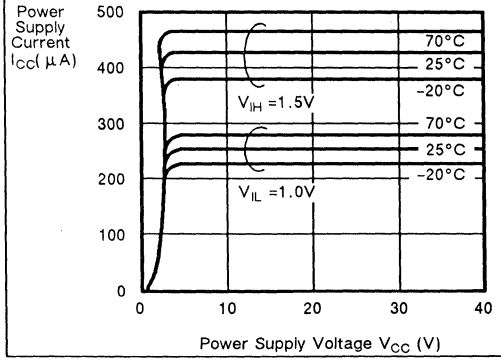
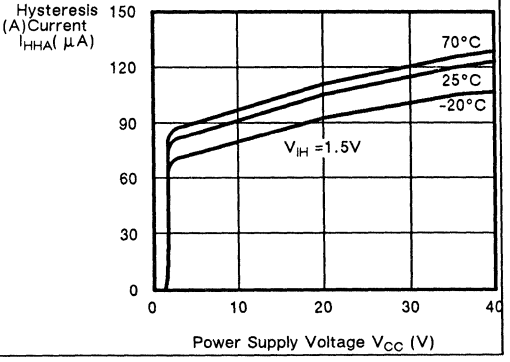


Fig. 4 – Hysteresis (A) Current vs Power Supply Voltage



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 5 – Output (A) Voltage vs. Output (A) Current

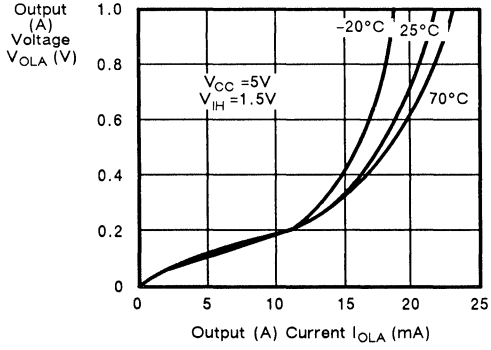


Fig. 6 – Output (B) Voltage vs. Output (B) Current

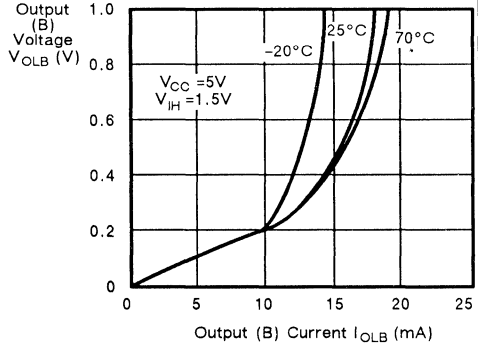


Fig. 7 – Threshold Voltage vs. Power Supply Voltage

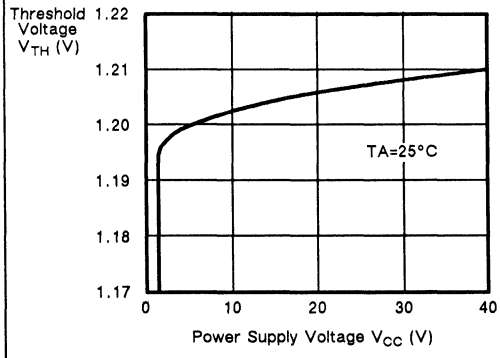
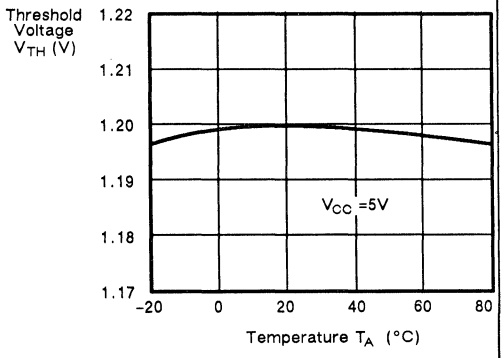


Fig. 8 – Threshold Voltage vs. Temperature



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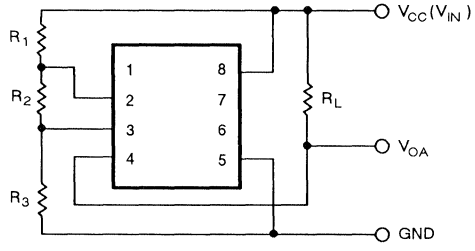
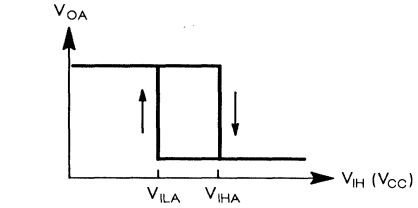
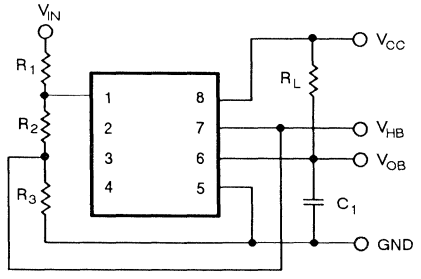
APPLICATION EXAMPLES

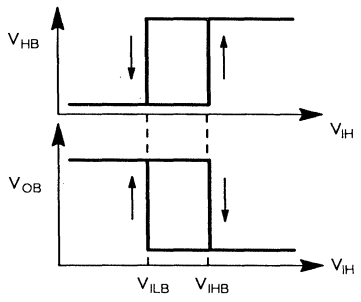
Figure 9. Addition of Hysteresis





$$V_{IHA} = (1 + \frac{R_1 + R_2}{R_3})V_R \qquad V_{ILA} = (1 + \frac{R_2}{R_3})V_R$$



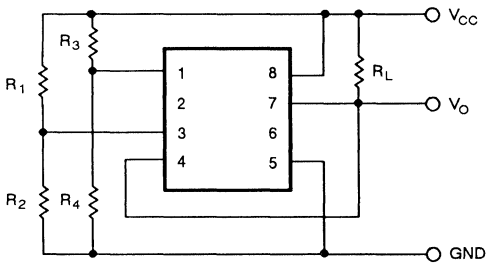


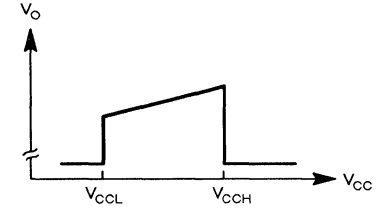
Note: All calculations occur with the output voltage at 0. The hysteresis values are adjusted for load condition and saturation voltage.

$$V_{IHB} = (1 + \frac{R_1}{R_2})V_R \qquad V_{ILB} = (1 + \frac{R_1}{R_2 + R_3})V_R$$

APPLICATION EXAMPLES (Continued)

Figure 10. Voltage Detection for Alarm



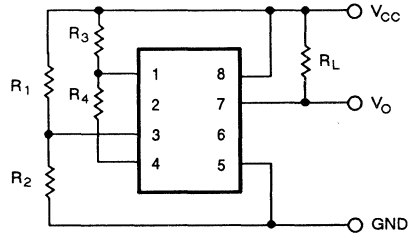


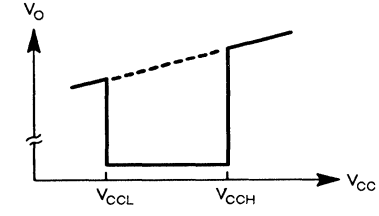
$$V_{CCH} = (1+\frac{R_1}{R_2})V_R \qquad V_{CCL} = (1+\frac{R_3}{R_4})V_R$$

$$V_{CCL} \geqq 2.5V$$

For hysteresis, a positive feedback from pin 2 or 7 is required.

Figure 11. Voltage Detection for Alarm



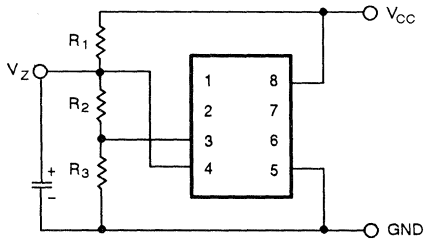


$$V_{CCH} = (1+\frac{R_3}{R_4})V_R \qquad V_{CCL} = (1+\frac{R_1}{R_2})V_R$$

$$V_{CCL} \geqq 2.5V$$

APPLICATION EXAMPLES (Continued)

Figure 12. Programmable Zener

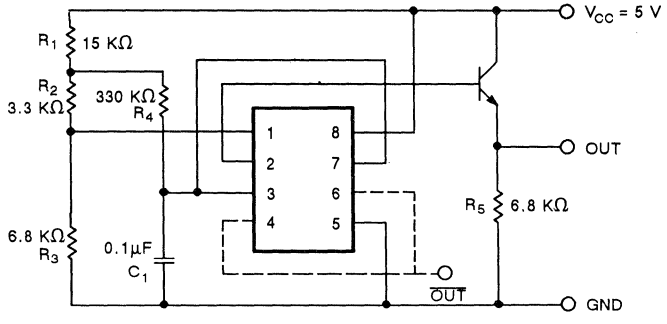


$$V_Z \fallingdotseq (1+\frac{R_2}{R_3})V_R$$

$$\frac{V_Z}{R_2+R_3} \leqq \frac{V_{CC}-V_Z}{R_1} \leqq 6mA$$

Channel B can be used independently.

Figure 13. Recovery Reset Circuit



APPLICATION EXAMPLES (Continued)

Figure 14. DC Characteristics

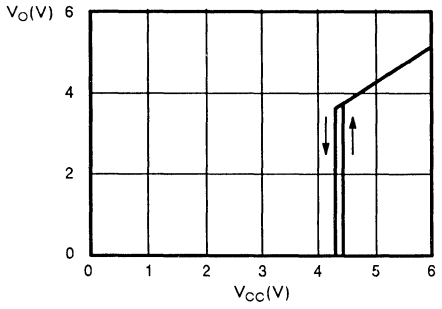
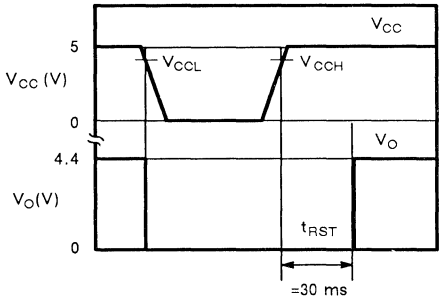


Figure 15. Response Characteristics



- Voltage Threshold Levels (V_{CCL} and V_{CCH}) and Hysteresis Width can be changed by the resistors (R_1 through R_4).

$$V_{CCL} = \frac{R_1 + R_2 + R_3}{R_3} V_{TH}$$

$$V_{CCH} = V_{CCL} + \frac{R_1 (R_2 + R_3)}{R_3 R_4} V_{TH}$$

- Power-On Reset Time is provided by the following approximate equation:

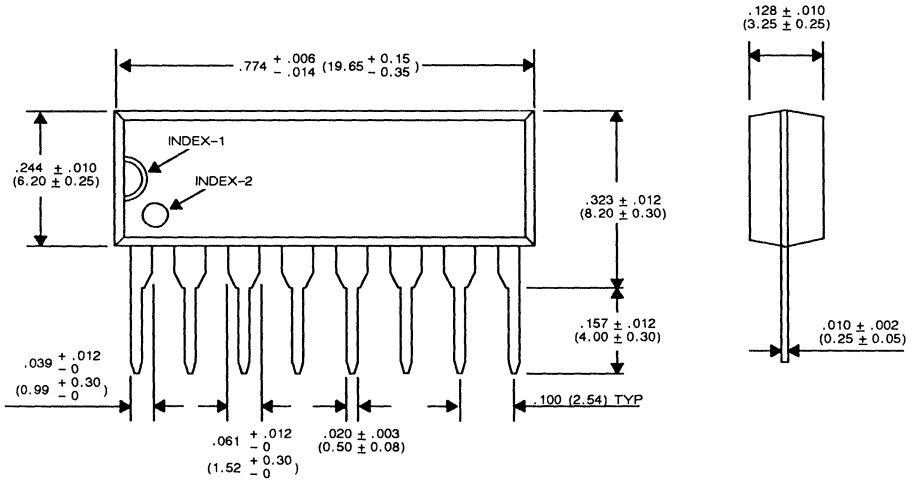
$$t_{RST} = -C_1 R_4 \cdot \ln \left\{ 1 - \frac{V_{TH}}{V_{CC}} \left(1 + \frac{R_1}{R_2 + R_3} \right) \right\}$$

- The recommended value of h_{FE} of the external transistor is from 50 to 200.
- In the case of an instant power fail, the remaining charge in C_1 effects t_{RST}.
- If necessary, the reversed output is provided on HYS terminal

4

PACKAGE DIMENSIONS

8-LEAD PLASTIC SINGLE-IN-LINE PACKAGE
(CASE No.: SIP-08P-M03)

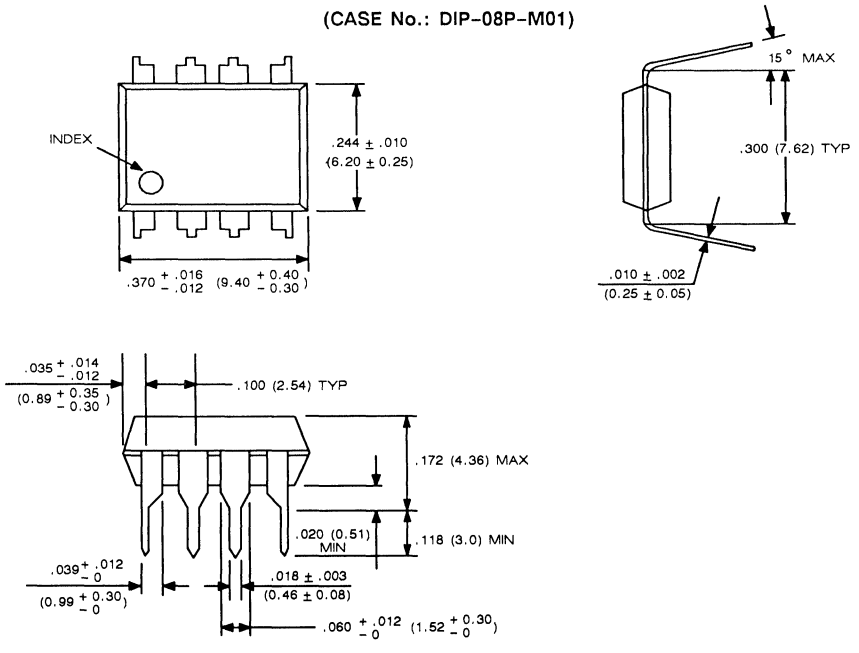


Dimensions in
inches (millimeters)

S08010S-2C

PACKAGE DIMENSIONS (Continued)

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)

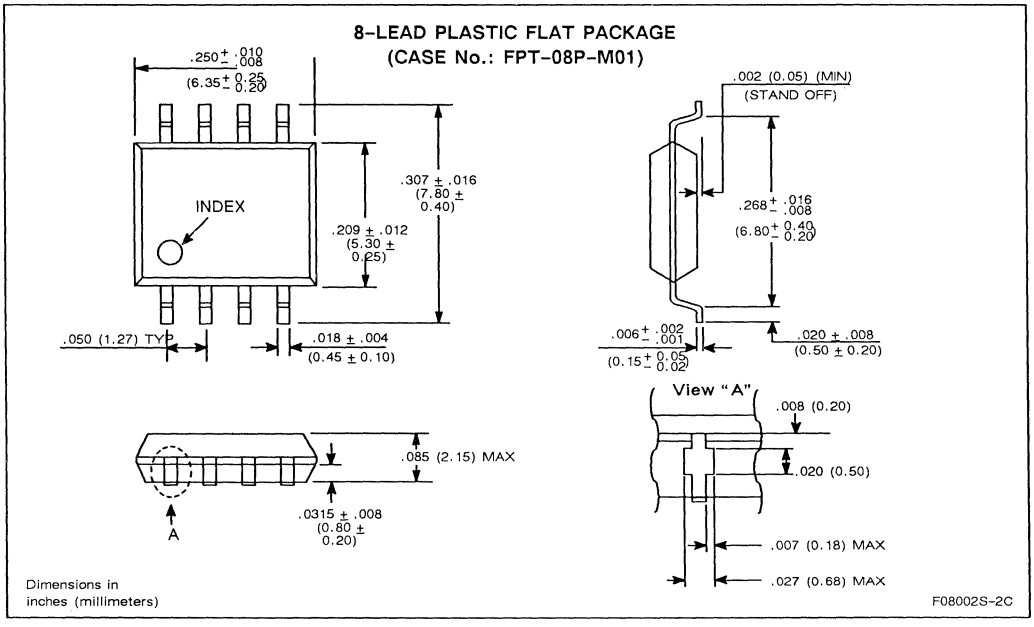


Dimensions in
inches (millimeters)

D08006S-2C

4

PACKAGE DIMENSIONS (Continued)



April 1990
Edition 1.0

FUJITSU

PRODUCT PROFILE

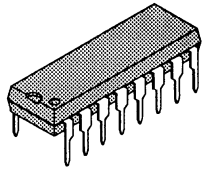
MB3769A

Regulating Pulse-Width-Modulation Control Circuit

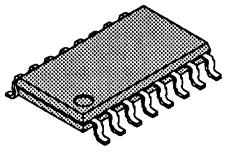
DESCRIPTION

The Fujitsu MB3769A is a pulse-width-modulation controller for fixed frequency pulse modulation application. The MB3769A contains a wide band width operational amplifier and a high speed comparator to construct a very high speed switching regulator system up to 700kHz. The output is suitable for a power MOS FET drive due to the adoption of a totem pole output.

The MB3769A provides a stand-by mode at low voltage power supply when it is used in a primary control system.

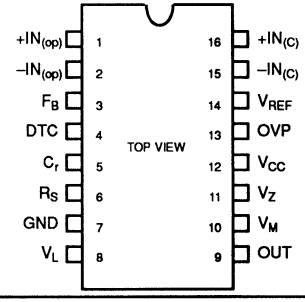


Plastic Package
DIP-16P-M04



Plastic Package
FPT-16P-M02

Pin Assignment



FEATURES

- High frequency oscillator (f = 1 to 700kHz)
- On-chip wide-band frequency operation amplifier (BW = 8MHz type)
- Internal reference voltage generator provides a stable reference supply (5 V ± 2 %)
- Low power dissipation (1.5 mA typ. at standby mode, 8 mA typ. at operating mode)
- Output current (± 600 mA at peak)
- High speed switching operation (tr = 60 ns, tf = 30 ns, C_L = 1000 pF typ.)
- Adjustable Dead-time
- On-chip soft start and quick shut down functions
- Internal circuitry prohibits double pulse at dynamic current limit operation
- Under-voltage lock-out function (OFF to ON: 10 V typ. ON to OFF: 8 V typ.)
- On-chip output shut-down circuit with latch function at over-voltage
- On-chip Zener diode (15 V)

ABSOLUTE MAXIMUM RATINGS

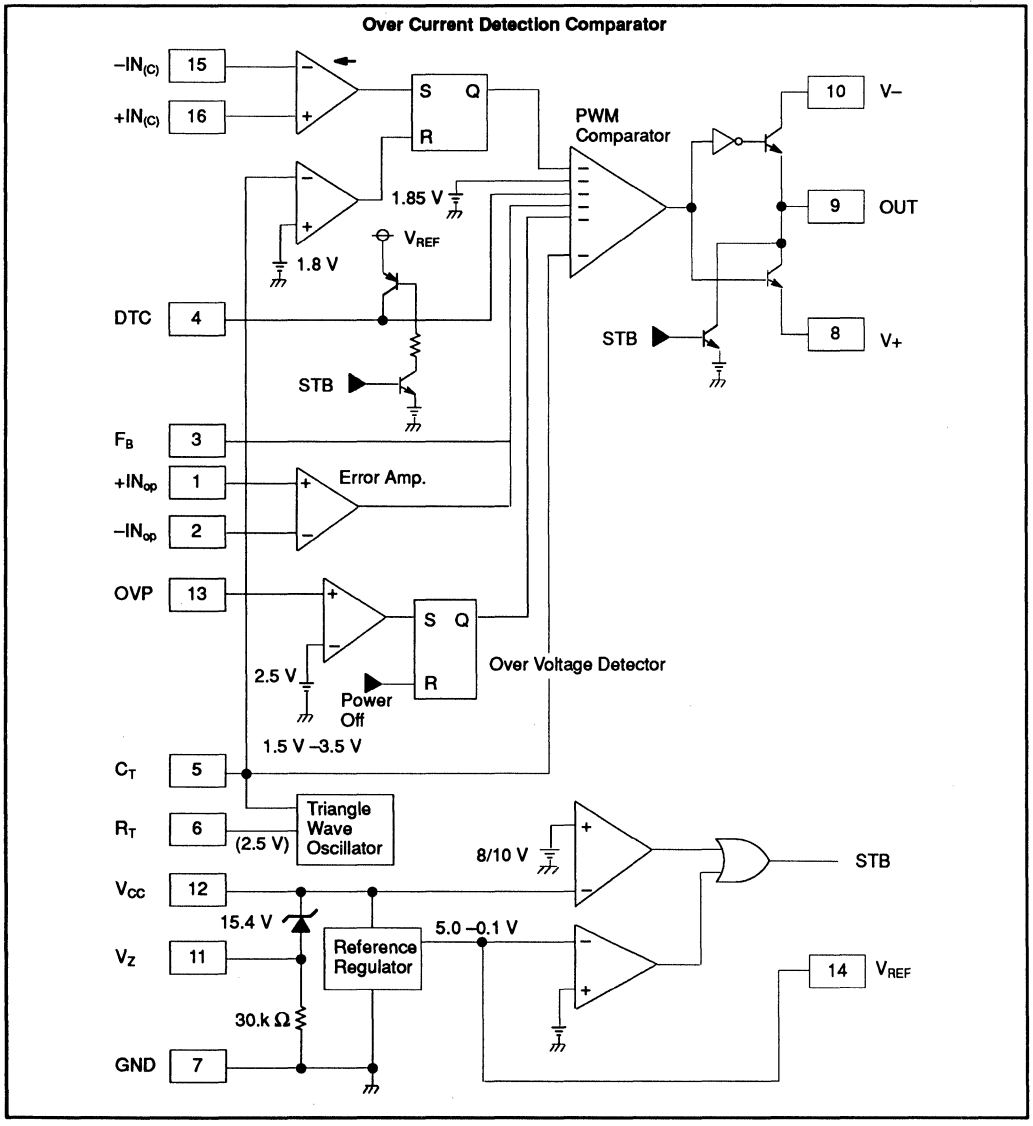
Parameter		Symbol	Ratings	Unit
Power Supply Voltage		V_{CC}	20	V
Output Current		I_{out}	120 (660[1])	mA
Operation Amp. Input Voltage		$V_{in\ (op)}$	V_{CC} +0.3 (S20)	V
Power Dissipation:	DIP	PD	1000[2]	mW
	FPT	PD	620[3]	mW
Operating Temperature:	DIP	T_{op}	−20 to +85	°C
	FPT	T_{op}	−20 to +75	°C
Storage Temperature		T_{stg}	−35 to +125	°C

Notes: [1]Duty ≤ 5%
[2]T_a = 25°C
[3]T_a = 25°C, FPT package is mounted on the epoxy board. (4_{cm} x 4_{cm} x 0.15_{cm})

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FIGURE 1. BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	DIP Package			FPT Package			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	12	15	18	12	15	18	V
Output Current (DC)	I_{OUT}	–100	—	100	–100	—	100	mA
Output Current (Peak)	$I_{OUTPEAK}$	600	—	600	–600	—	600	mA
Operation Amp. Input Voltage	V_{INOP}	–0.2	0 to V_{REF}	V_{CC} –3	–0.2	0 to V_{REF}	V_{CC} –3	V
FB Sink Current	I_{SINK}	—	—	0.3	—	—	0.3	mA
FB Source Current	I_{SOURCE}	—	—	2	—	—	2	mA
Comparator Input Voltage	V_{INC+}	–0.3	0 to 3	V_{CC}	–0.3	0 to 3	V_{CC}	V
	V_{INC-}	–0.3	0 to 2	2.5	–0.3	0 to 2	2.5	V
Reference Section Output Current	I_{REF}	—	5	10	—	2	10	mA
Timing Register	R_T	9	18	50	9	18	50	kΩ
Timing Capacitor	C_T	100	680	10^4	100	680	10^4	pF
Oscillator Frequency	F_{osc}	1	100	700	1	100	700	kHz
Zener Current	I_z	—	—	5	—	—	5	mA
Operating Temperature	T_{or}	–30	—	85	–30	—	75	°C

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ELECTRICAL CHARACTERISTICS

(V_{CC} = 15 V, T_a = 25°C)

Reference Section

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Output Voltage	V_{REF}	I_{REF} = 1 mA	4.9	5.0	5.1	V
Input Regulation	ΔV_{RIN}	12 V ≤ V_{CC} ≤ 18 V	—	2	15	mV
Load Regulation	ΔV_{RLD}	1 mA ≤ I_{REF} ≤ 10 mA	—	–1	–15	mV
Temperature Stability	ΔV_{RTEMP}	–20°C ≤ T_a ≤ +85°C	—	±200	±750	μV/°C
Short Circuit Output Current	I_{sc}	V_{REF} = 0 V	15	40	—	mA

ELECTRICAL CHARACTERISTICS (Continued)

Ocillator Section

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Oscillator Frequency	f_{osc}	R_f = 18k Ω, C_T = 680 pF	90	100	110	kHz
Voltage Stability	$\Delta f_{osc} / V$	12 V ≤ V_{CC} ≤ 18 V	—	±0.03	—	%
Temperature Stability	$\Delta f_{osc} / \Delta T$	−20°C ≤ T_a ≤ +85°C	—	±2	—	%

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Dead-Time Control Section

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Input Bias Current		I_D		—	2	10	μA
Maximum Duty Cycle		D_{max}	V_d = 1.5 V	75	80	75	%
Duty Cycle Set		D_{set}	V_d = 0.5 V_{REF}	45	50	55	%
Input Threshold Voltage	0% Duty Cycle	V_{DO}		—	3.5	3.8	V
	Maximum Duty Cycle	V_{DM}		1.55	1.85	—	V
Discharge Voltage		V_{DN}	V_{CC} = 7 V, I_{DTC} = −0.3 mA	4.5	—	—	V

Error Amplifier Section

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Input Offset Voltage	$V_{IO\ (OP)}$	V_3 = 2.5 V	—	±2	±10	mV
Input Offset Current	$I_{IO\ (OP)}$	V_3 = 2.5 V	—	±30	±300	nA
Input Bias Current	$I_{IB\ (OP)}$	V_3 = 2.5 V	−1	−0.3	—	μA
Common-mode Input Voltage	$V_{CW\ (OP)}$	12 V ≤ V_{CC} ≤ 18 V	−0.2	—	V_{CC} −3	V
Voltage Gain	$A_{V\ (OP)}$	0.5 V ≤ V_3 ≤ 4 V	70	90	—	dB
Band Width	BW	A_f = 0 dB	—	8	—	MHz
Slew Rate	SR	R_L = 10k Ω, A_v = 0 dB	—	6	—	V/μsec
Common-mode Rejection Rate	CMR	V_{IN} = 0 10 V	65	80	—	dB
High Level Output Voltage	V_{ON}	I_3 = −2 mA	4.0	4.6	—	V
Low Level Output Voltage	V_{OL}	I_3 = −3 mA	—	0.1	0.5	V

ELECTRICAL CHARACTERISTICS (Continued)

Current Comparator

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Input Offset Voltage	$V_{IO\,(C)}$	V_{IN} = 1 V	—	±5	±15	mV
Input Bias Voltage	$V_{IB\,(C)}$	V_{IN} = 1 V	–5	–1	—	µA
Common-mode Input Voltage	$V_{CM\,(C)}$		0	—	2.5	V
Voltage Gain	$A_{v\,(C)}$		—	200	—	V/V
Response Time	td	50 mV over drive	—	120	250	ns

PWM Comparator Section

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
0% Duty Cycle	$V_{or\,\Omega}$	R_t = 18k Ω, C_t = 680 pF	—	3.5	3.8	V
Maximum Duty Cycle	$V_{or\,\mu}$		1.55	1.85	—	V

Output Section

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
High Level Output Voltage	V_H	I_{OUT} = –100 mA	12.5	13.5	—	V
Low Level Output Voltage	V_L	I_{OUT} = –100 mA	—	1.1	1.3	V
Rise Time	t_r	C_L = 1000 pF, R_L = ∞	—	60	120	ns
Fall Time	t_f	C_L = 1000 pF, R_L = ∞	—	30	80	ns

Over Voltage Detector

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Threshold Voltage	V_{ovr}		2.4	2.5	2.6	V
Input Current	V_{invp}	V_{IN} = 0 V	–1.0	–0.2	—	µA
V_{CC} Reset	$V_{CC\,RST}$		2.0	3.0	4.5	V

4

ELECTRICAL CHARACTERISTICS (Continued)

Low Voltage Stop

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Off to No	V_{TNN}		9.2	10.0	10.8	V
On to Off	V_{TNL}		7.2	8.0	8.8	V

Total Device

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Standby (V_{CC} = 8 V)	I_{CCSTN}	R_t = 18k Ω 4-pin Open	—	1.5	2.0	mA
Operating	I_{CC}	R_t = 18k Ω	—	8.0	12.0	mA

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Zener Voltage	V_Z	I_Z = 1 mA	—	15.4	—	V
Zener Current	I_Z	V_{II-T} = 1 V	—	0.03	—	mA

FIGURES 2a and 2b. TEST CIRCUIT

Figure 2a

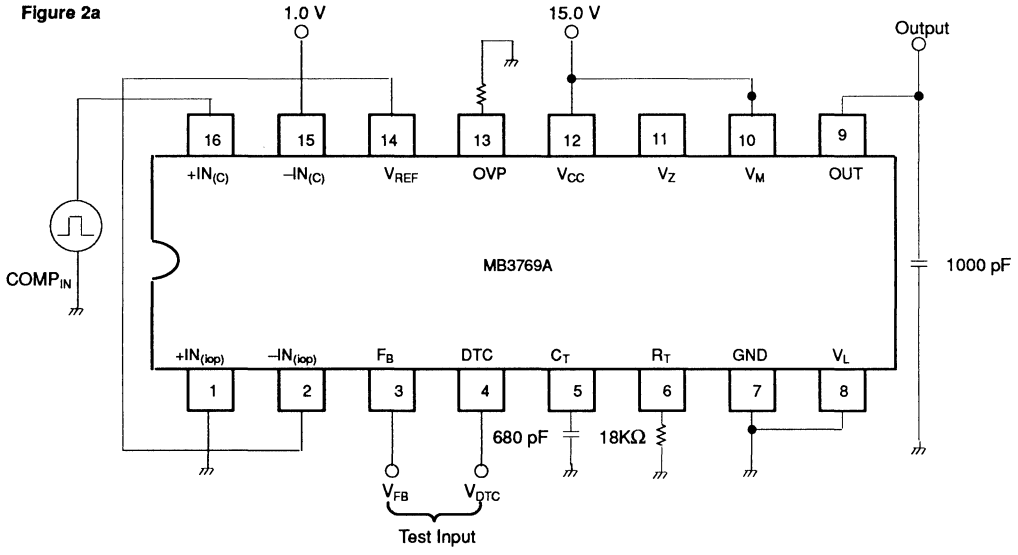


Figure 2b

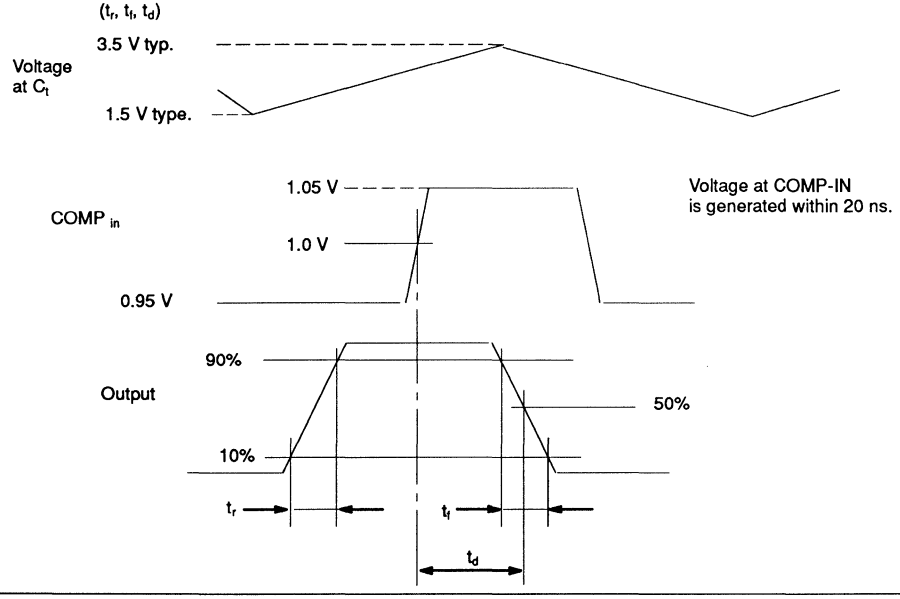
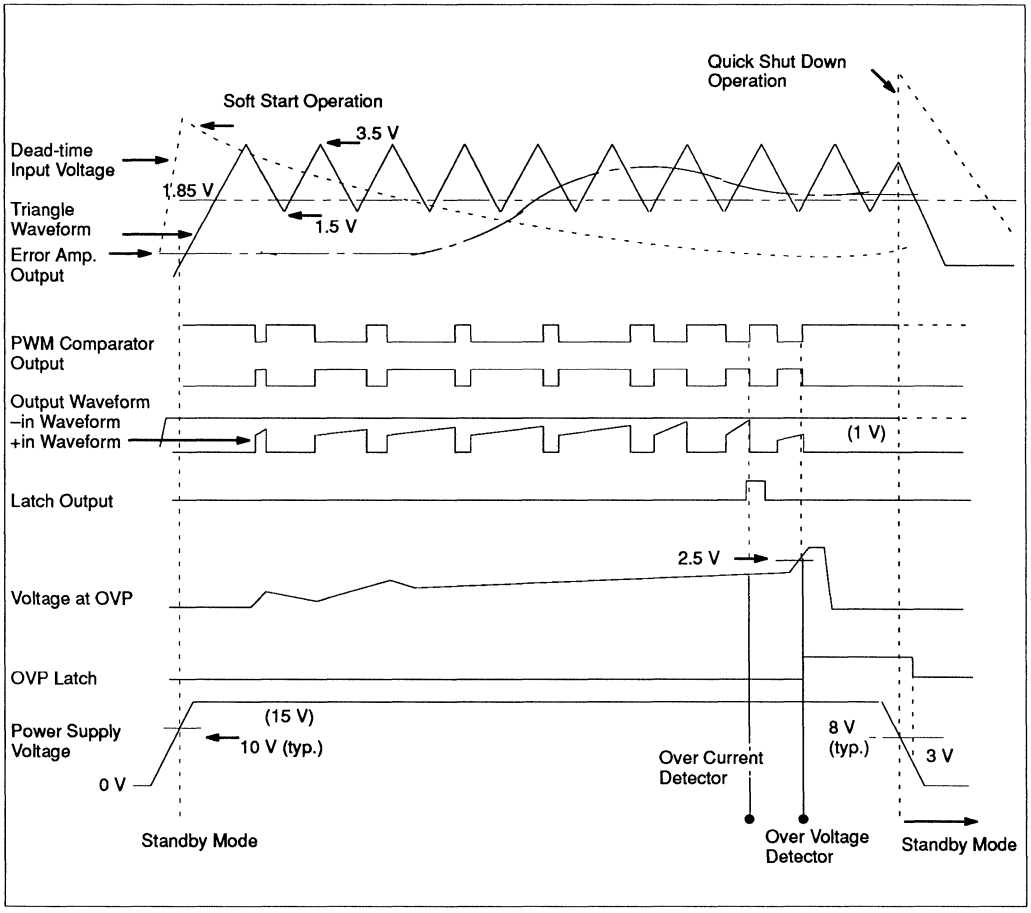


FIGURE 3. OPERATING TIMING



TYPICAL CHARACTERISTICS CURVES

Figure 4. Power Supply Current vs. Power Supply Voltage
(Low Voltage Stop of V_{CC})

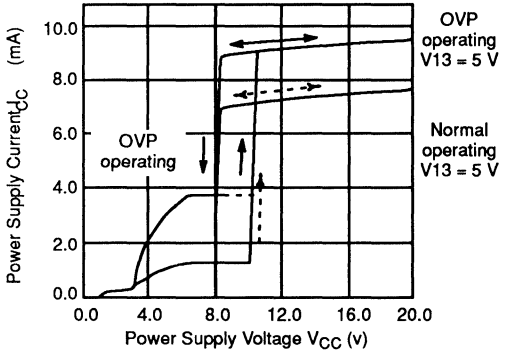


Figure 5. Standby Current vs. Temperature

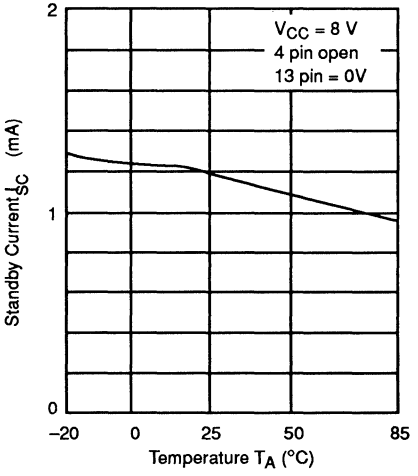


Figure 6. Reference Voltage vs. Temperature

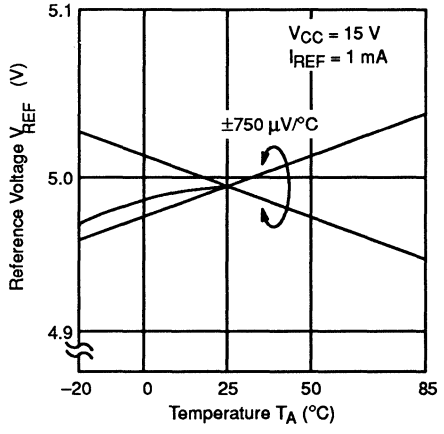
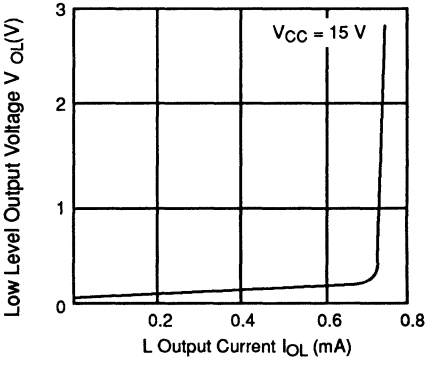


Figure 7. Low level Output Voltage vs. Low level Output Current



TYPICAL CHARACTERISTICS CURVES

Figure 8. High level Output Voltage vs. High level Output Current

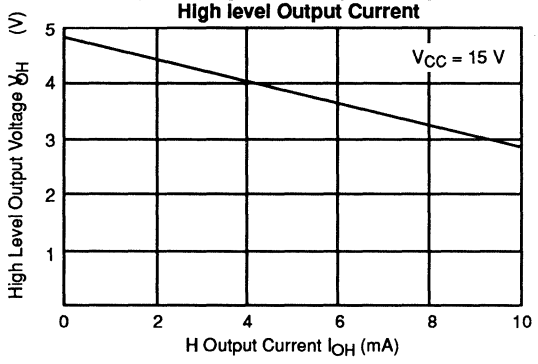


Figure 9. Oscillator Frequency vs. R_T

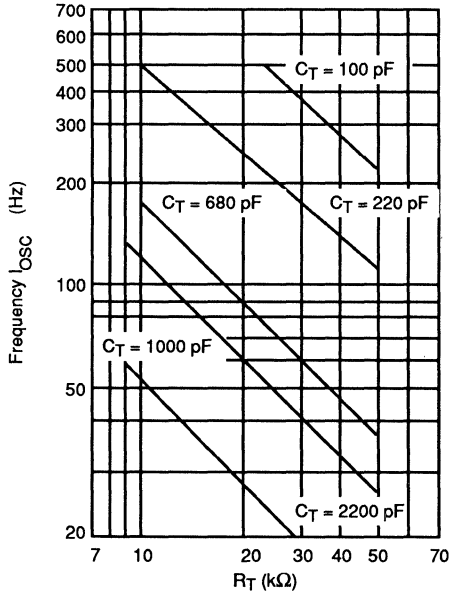
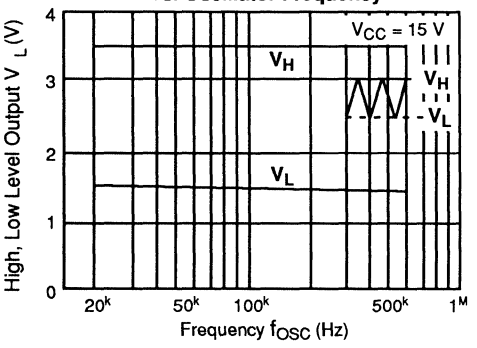


Figure 10. H, L level Output Voltage vs. Oscillator Frequency



TYPICAL CHARACTERISTICS CURVES

Figure 11. Duty Cycle vs. Dead Time Control Voltage

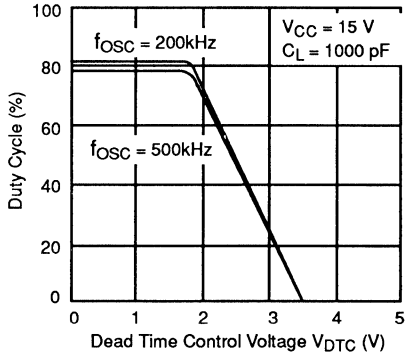


Figure 12. Oscillator Frequency vs. Temperature

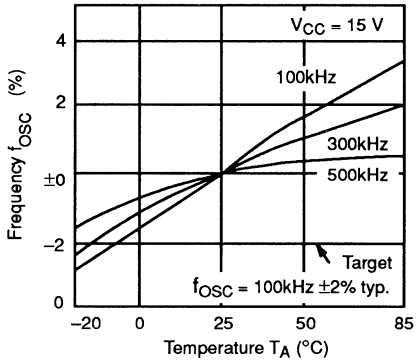


Figure 13. Dead Time Control Voltage vs. Current (Standby Mode)

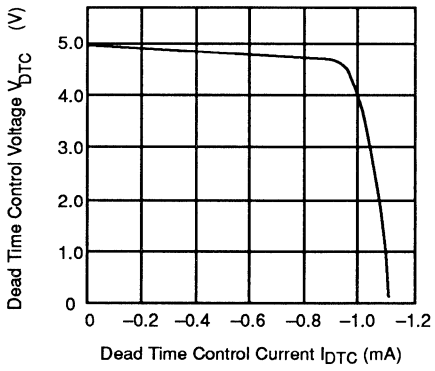
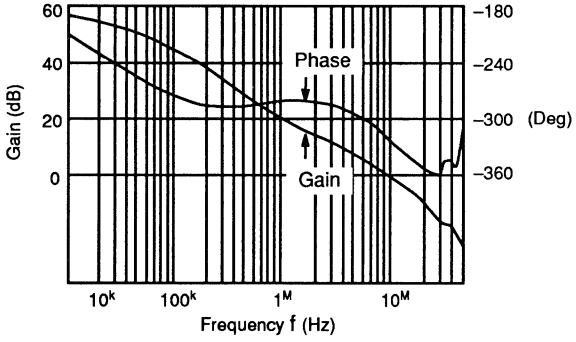


Figure 14. Gain/Phase vs. Frequency (Set G_V = 60 dB)



4

TYPICAL CHARACTERISTICS CURVES

Figure 15. Duty cycle vs. Temperature

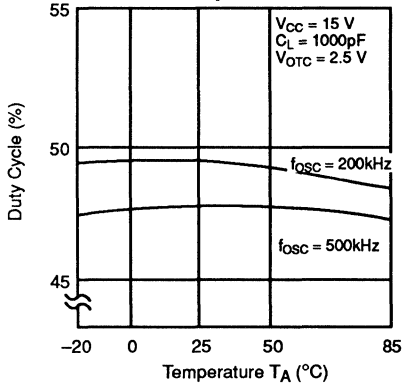


Figure 16. Low Level Output Voltage vs. Low level Output Current

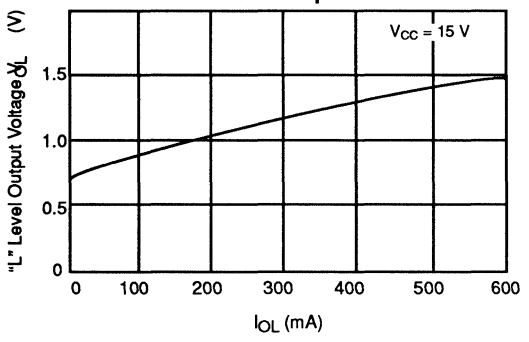


Figure 17. High Level Output Voltage vs. High level Output Current

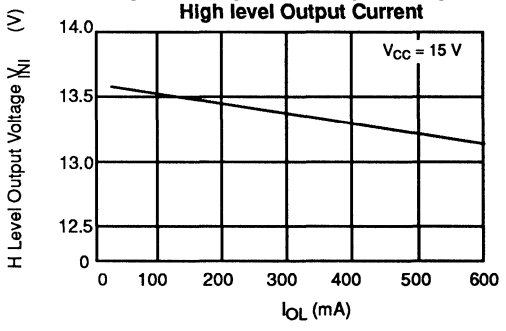
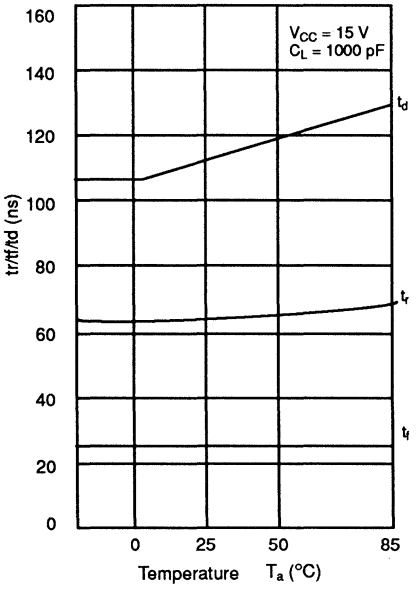


Figure 18. $t_R/t_f/t_d$ vs. Temperature



TYPICAL CHARACTERISTICS CURVES

Figure 19. Standby Power Supply Current vs. Temperature

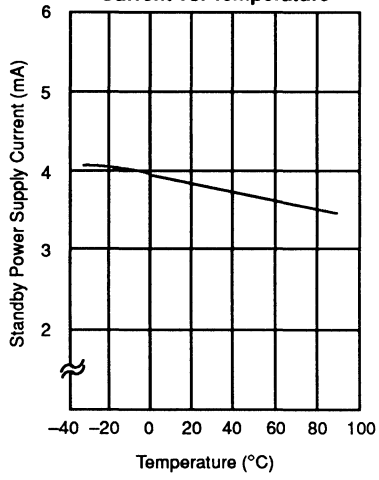


Figure 20. OVP Supply Voltage Reset vs. Temperature

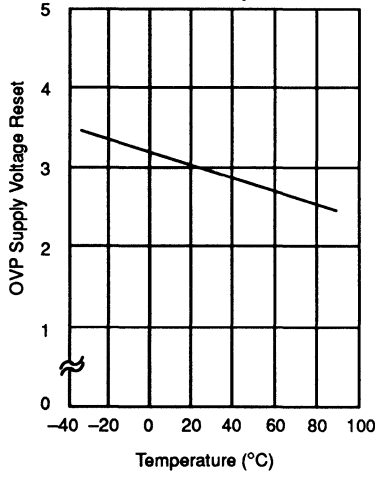


FIGURE 21. MB3769A TYPICAL APPLICATION
DC – DC Converter

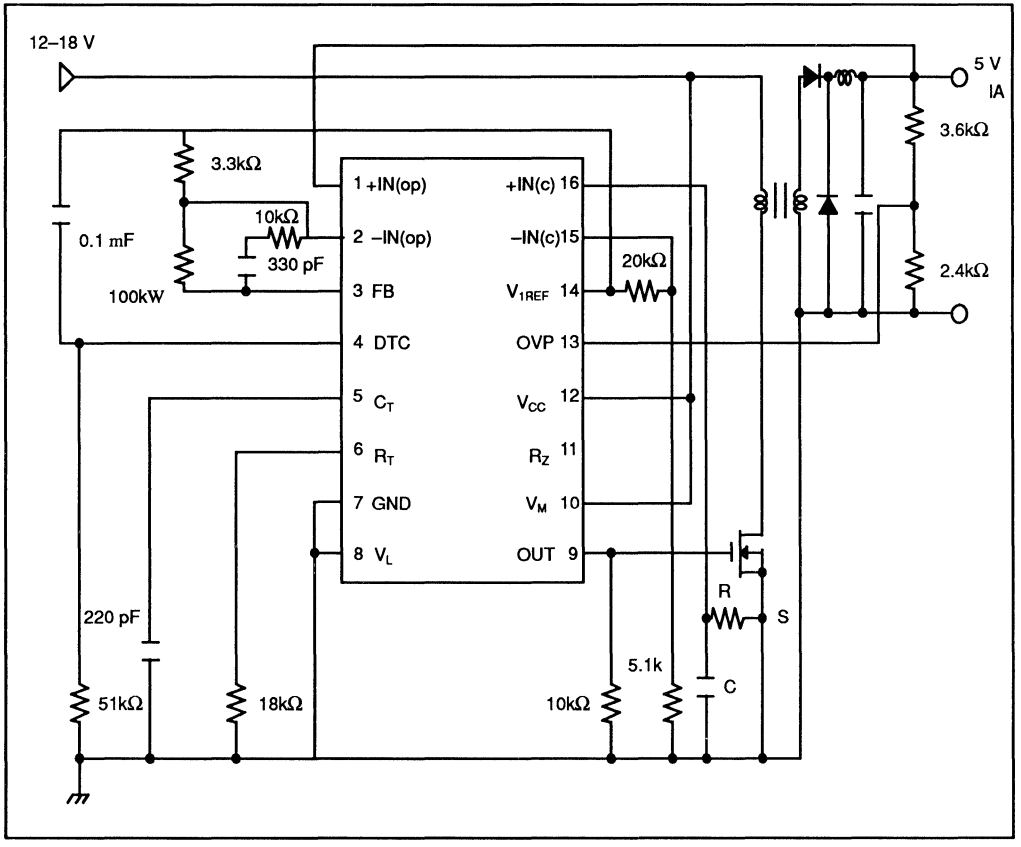


FIGURE 22. PRIMARY CONTROL

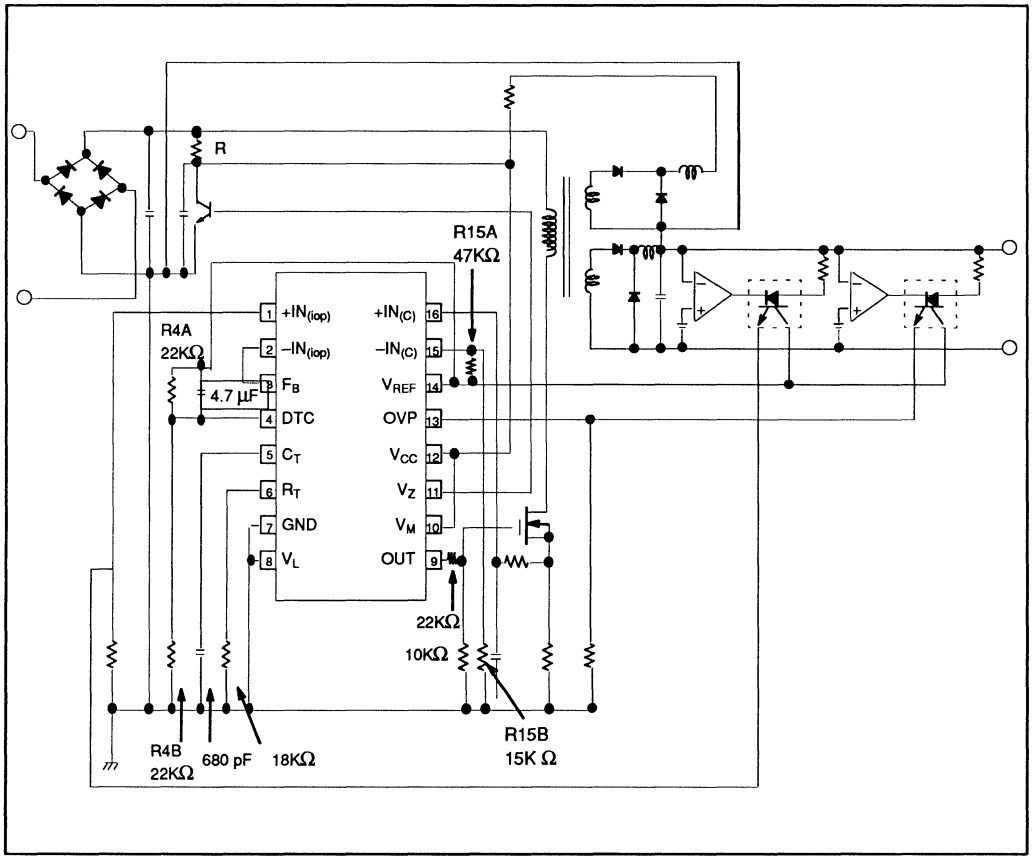
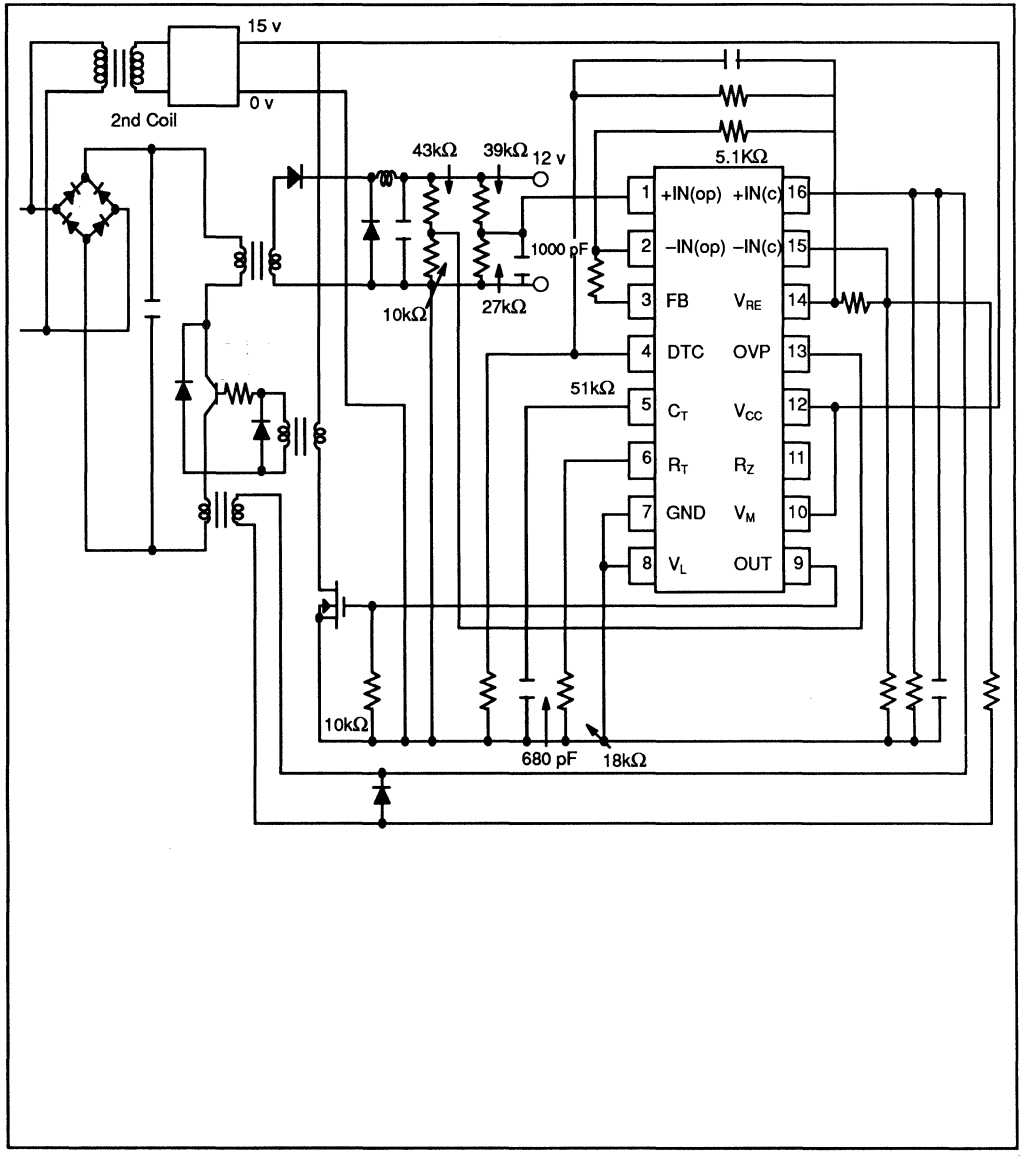
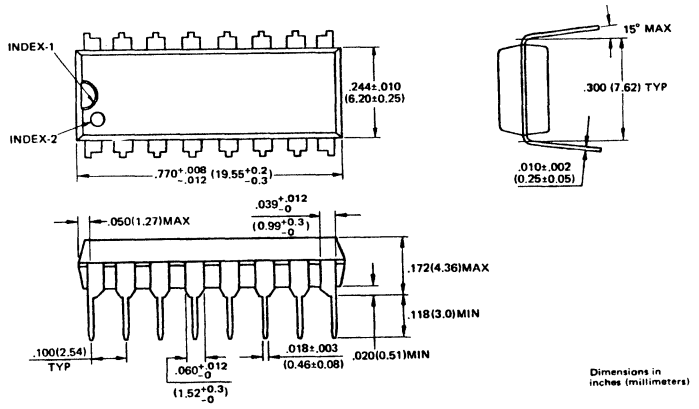


FIGURE 23. SECONDARY CONTROL

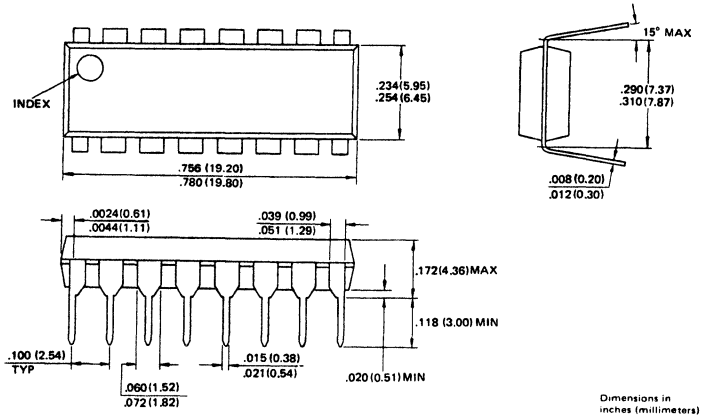


PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No. DIP-16P-M04)



16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No. FPT-16P-M02)



4

FUJITSU

POWER SUPPLY MONITOR

MB 3771

September 1986
Edition 1.0

POWER SUPPLY MONITOR

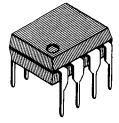
The Fujitsu MB 3771 is designed to monitor the voltage level of one or two power supplies (+5V and an arbitrary voltage) in a microprocessor circuit, memory board in large-size computer, for example.

If the circuit's power supply deviates more than a specified amount, then the MB 3771 generates a reset signal to the microprocessor. Thus, the computer data is protected from accidental erasure.

Using the MB 3771 requires few external components. To monitor only a +5V supply, the MB 3771 requires the connection of one external capacitor. The level of an arbitrary dectection voltage is determined by two external resistors.

The MB 3771 is available in an 8-pin Dual In-Line, Signal In-Line Package or space saving Flat Package.

- Precision voltage detection (V_{SA} = 4.1 to 4.3 V)
- User selectable threshold level with hysterisis ($V_{SB} \geqq 1.24$ V)
- Monitors the voltage of one or two power supplies (5 V and an arbitrary voltage, $\geqq 1.23$ V)
- Low voltage output for reset signal (V_{CC} = 0.8 V typ.)
- Minimal number of external components (one capacitor min.)
- Low power dissipation (I_{CC} = 0.35 mA typ., V_{CC} = 5 V)
- Available in a variety of packages
  - 8-pin Dual In-Line Package
  - 8-pin Single In-Line Package
  - 8-pin Flat Package

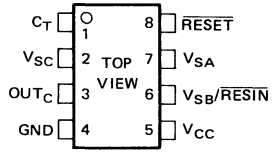


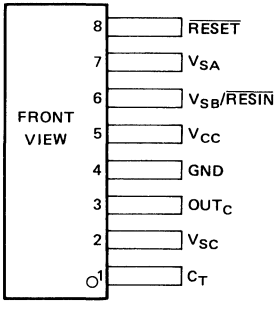
PLASTIC PACKAGE
DIP-08P-M01

PLASTIC PACKAGE
DIP-08P-M02

FPT-08P-M01: See page 20

PIN ASSIGNMENT





ABSOLUTE MAXIMUM RATINGS

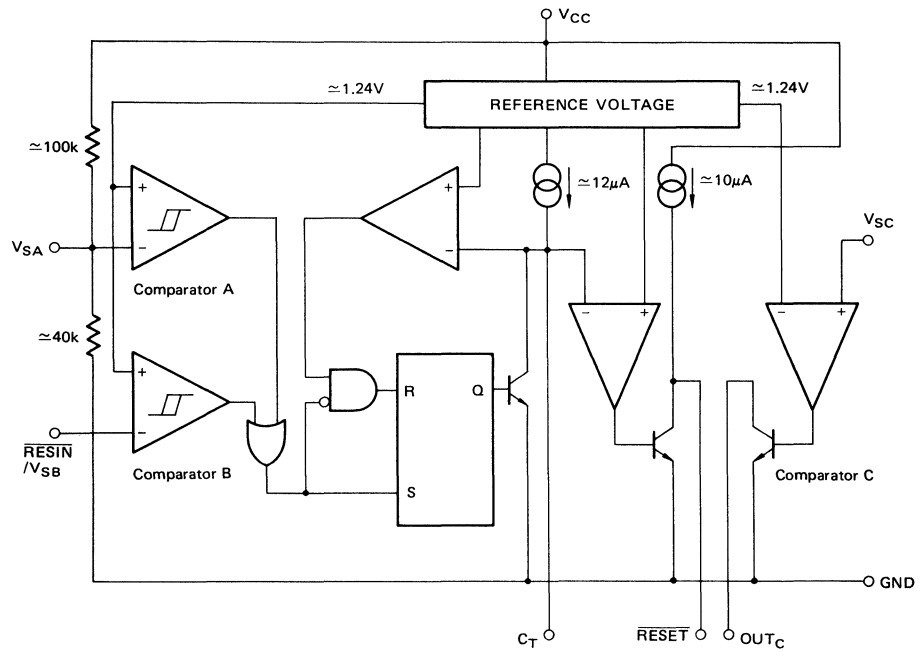
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +20	V
Input Voltage A	V_{SA}	-0.3 to V_{CC}+0.3 (<+20)	V
Input Voltage B	V_{SB}	-0.3 to +20	V
Input Voltage C	V_{SC}	-0.3 to +20	V
Power Dissipation	P_D	200 ($T_A \leqq 85°C$)	mW
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

BLOCK DIAGRAM OF MB 3771



FUNCTIONAL EXPLANATIONS

Detection voltage inputs A and B are connected to the inverting input of Comparators A and B respectively. Both comparators have built-in hysterisis. If either V_{SA} or V_{SB} drops lower than about 1.23V, then $\overline{RESET}$ goes low.

Comparator B is used for the arbitrary preset voltage detection (See Example 3), or as forced reset input for TTL logic level input. (See Example 6)

Comparator C is designed as an open-collector output with inverted polarity input/output characteristics. Comparator C has no hysteresis. It can be used for over-voltage detection (See Example 11), generation of $\overline{RESET}$ signal by positive logic (See Example 7), and generation of reference voltage (See Example 10).

Note that V_{SB} and V_{SC} should be connected with V_{CC} and GND respectively. (See Example 1.)

The MB 3771 can detect about 2μs voltage sag/surge of the power supply. The user can add delayed trigger capacity by connecting a capacitor between inputs V_{SA} and V_{SB}. (See Example 8)

Internal pull-up resistor on the $\overline{RESET}$ line provides for high impedance loading (i.e. CMOS logic).

RECOMMENDED OPERATING CONDITIONS

parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	+3.5 to +18	V
Output Current ($\overline{RESET}$)	I_{RESET}	0 to 20	mA
Output Current (OUT_C)	I_{OUTC}	0 to 6	mA
Operating Ambient Temperature	T_A	-40 to +85	°C

ELECTORICAL CHARACTERISTICS

DC Characteristics (V_{CC} = 5V, T_A = 25°C)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
Supply Current	V_{SB} = 5V, V_{SC} = 0V	I_{CC1}		350	500	μA
	V_{SB} = 0V, V_{SC} = 0V	I_{CC2}		400	600	μA
Sagging Detection Voltage Falling	V_{CC}	V_{SAL}	4.10	4.20	4.30	V
	V_{CC}, T_A = -40 to +85°C		4.05	4.20	4.35	V
Rising	V_{CC}	V_{SAH}	4.20	4.30	4.40	V
	V_{CC}, T_A = -40 to +85°C		4.15	4.30	4.45	V
Hysterisis Width		V_{HYSA}	50	100	150	mV
Sagging Detection Voltage	V_{SB}	V_{SB}	1.212	1.230	1.248	V
	V_{SB}, T_A = -40 to +85°C		1.200	1.230	1.260	V
Deviation of Detection Voltage	V_{CC} = 3.5 to 18V	$\triangle V_{SB}$		3	10	mV
Hysterisis Width		V_{HYSB}	14	28	42	mV
Input Current	V_{SB} = 5V	I_{IHB}		0	250	nA
	V_{SB} = 0V	I_{ILB}		20	250	nA
High-level Output Voltage	I_{RESET} = -5μA, V_{SB} = 5V	V_{OHR}	4.5	4.9		V
Output Saturation Voltage	I_{RESET} = 3mA, V_{SB} = 0V	V_{OLR}		0.28	0.4	V
	I_{RESET} = 10mA, V_{SB} = 0V			0.38	0.5	V
Output Sink Current	V_{OLR} = 1.0V, V_{SB} = 0V	I_{RESET}	20	40		mA
C_T Charge Current	V_{SB} = 5V, V_{CT} = 0.5V	I_{CT}	9	12	16	μA

ELECTORICAL CHARACTERISTICS (Cont'd)

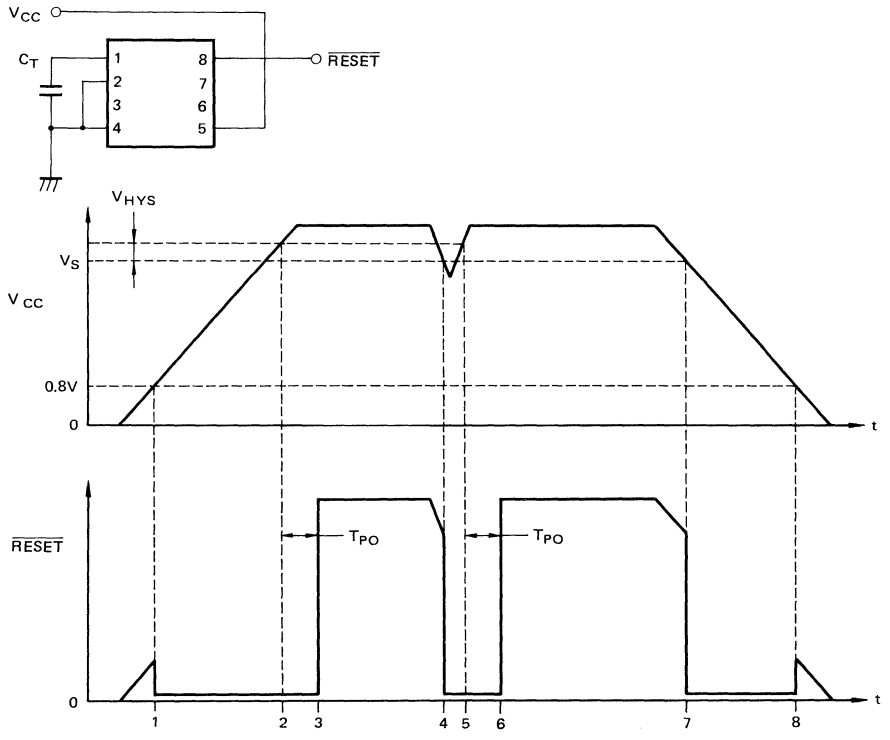
DC Characteristics (V_{CC} = 5V, T_A = 25°C)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
Input Current	V_{SC} = 5V	I_{IHC}		0	500	nA
	V_{SC} = 0V	I_{ILC}		50	500	nA
Detection Voltage	V_{SC}	V_{SC}	1.225	1.245	1.265	V
	V_{SC}, T_A = −40 to +85°C		1.205	1.245	1.285	V
Deviation of Detection Voltage	V_{CC} = 3.5 to 18V	ΔV_{SC}		3	10	mV
Output Leakage Current	V_{OHC} = 18V	I_{OHC}		0	1	μA
Output Saturation Voltage	I_{OUTC} = 4mA, V_{SC} = 5V	V_{OLC}		0.15	0.4	V
Output Sink Current	V_{OLC} = 1.0V, V_{SC} = 5V	I_{OUTC}	6	15		mA
Reset Operation Minimum Supply Voltage	V_{OLR}=0.4V, I_{RESET}=200μA	V_{CCL}		0.8	1.2	V

AC Characteristics (V_{CC} = 5V, T_A = 25°C, C_T = 0.01μF)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
Input Pulse Width	V_{SA}, V_{SB}	t_{PI}	5.0			μs
RESET Output Pulse Width		t_{PO}	0.5	1.0	1.5	ms
RESET Rising Time	R_L = 2.2kΩ, C_L = 100pF	t_R		1.0	1.5	μs
RESET Falling Time	R_L = 2.2kΩ, C_L = 100pF	t_F		0.1	0.5	μs
Propagation Delay Time	V_{SB}	t_{PD}		2	10	μs
	V_{SC}, R_L = 2.2kΩ, C_L = 100pF	t_{PHL}		0.5		μs
	V_{SC}, R_L = 2.2kΩ, C_L = 100pF	t_{PLH}		1.0		μs

FUNCTION EXPLANATION



Point 1: When V_{CC} rises to about 0.8V, $\overline{RESET}$ goes low.

Point 2: When V_{CC} reaches $V_S + V_{HYS}$, C_T then begins charging. $\overline{RESET}$ remains low during this time.

Point 3: $\overline{RESET}$ goes high when C_T begins charging.

$$T_{OP} \simeq C_T \times 10^5 \text{ [ms]}$$

Point 4: When V_{CC} level drops lower then V_S, then $\overline{RESET}$ goes low and C_T starts discharging.

Point 5: When V_{CC} level reaches $V_S + V_{HYS}$, then C_T starts charging.

In the case of voltage sagging, if the period from the time V_{CC} goes lower than or equal to V_S to the time V_{CC} reaches $V_S + V_{HYS}$ again, is longer than t_{P1}, (as speicified in the AC Characteristics), C_T is discharged and charged successively.

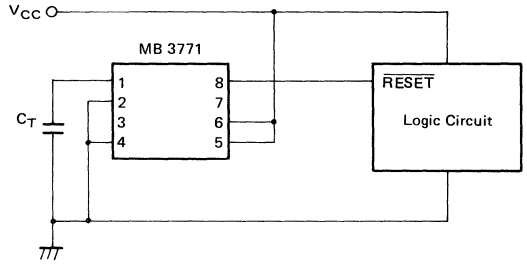
Point 6: After T_{PO} passes, and V_{CC} level exceeds $V_S + V_{HYS}$, then $\overline{RESET}$ goes high.

Point 7: Same as Point 4.

Point 8: $\overline{RESET}$ remains low until V_{CC} drops below 0.8V.

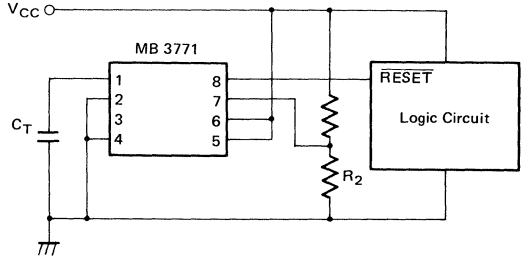
4

EXAMPLE 1: 5V Power Supply Monitor



NOTE: Monitored by V_{SA}. Detection Threshold Voltage is V_{SAL} and V_{SAH}.

EXAMPLE 2: 5V Power Supply Monitor with external adjust

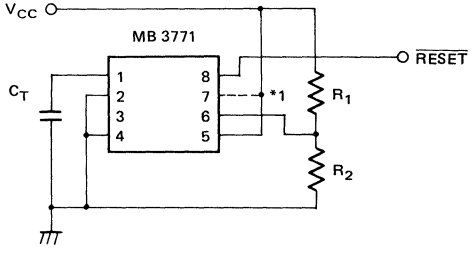


NOTE: Detection voltages can be adjusted as shown below.

R_1 [kΩ]	R_2 [kΩ]	Detection Voltage	
		V_{SAL} [V]	V_{SAH} [V]
10	3.9	4.4	4.5
9.1	3.9	4.1	4.2

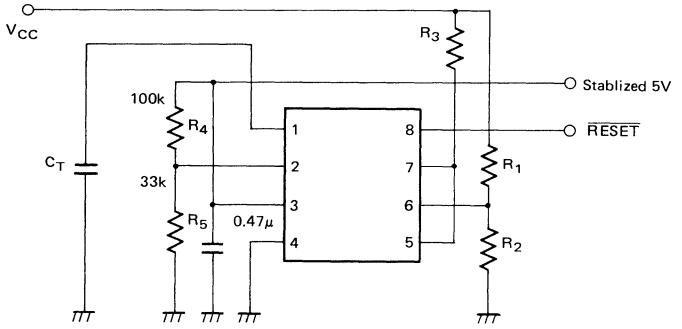
EXAMPLE 3: Arbitrary Voltage Supply Monitor

Example 3a: Case: $V_{CC} < 18V$



EXAMPLE 3: Arbitrary Voltage Supply Monitor

Example 3b: Case: $V_{CC} \geq 18V$

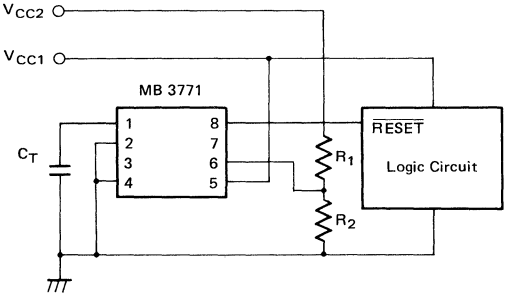


- $\overline{RESET}$ output levels range from 0V to 1V approximately. Device damage may occur if $\overline{RESET}$ exceeds its high level (1V).
- Output voltage and maximum $\overline{RESET}$ voltage levels are determined by resistor R_1 and R_2.
- In this case, the 5V stabilized output can be used to power TTL circuitry.
- Using the chart below, the value of R_3 can be determined with respect to the output current.

V_{CC} [V]	Detection Voltage [V]	Min. V_{CC}* for adequat RESET [V]	R_1 [MΩ]	R_2 [kΩ]	R_3 [kΩ]	Output Current [mA]
140	100	6.7	1.6	20	110	<0.2
100	81	3.8	1.3	20	56	<0.5
40	33	1.4	0.51	20	11	<1.6

NOTE: Resistor values are determined when $I_{OUTC} = 100\mu A$, $V_{OLC} = 0.4V$. All resistor are 1/4W.

EXAMPLE 4: 5V and 12V Power Supply Monitor ($V_{CC1} = 5V$, $V_{CC2} = 12V$)



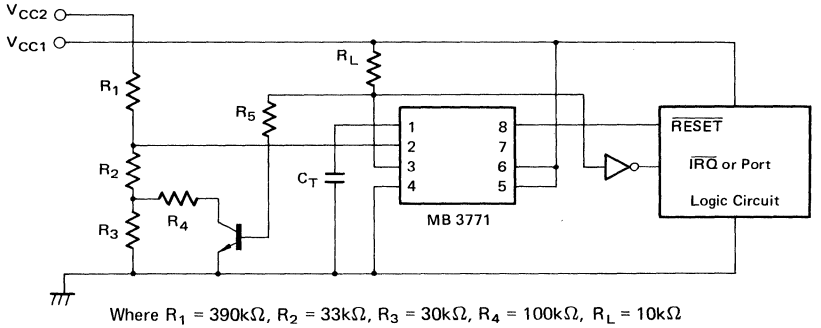
NOTE: 5V is monitored by V_{SA}. Detection voltage is about 4.2V.

12V is monitored by V_{SB}. When $R_1 = 390k\Omega$ and $R_2 = 62k\Omega$, Detection voltage is about 9.0V. Generally the detection voltage is determined by the following equation.

Detection Voltage = $(R_1 + R_2) \circ V_{SB}/R_2$

4

EXAMPLE 5: 5V and 12V Power Supply Monitor
($\overline{RESET}$ signal is generated by 5V, V_{CC1} = 5V, V_{CC2} = 12V)



Where R_1 = 390kΩ, R_2 = 33kΩ, R_3 = 30kΩ, R_4 = 100kΩ, R_L = 10kΩ

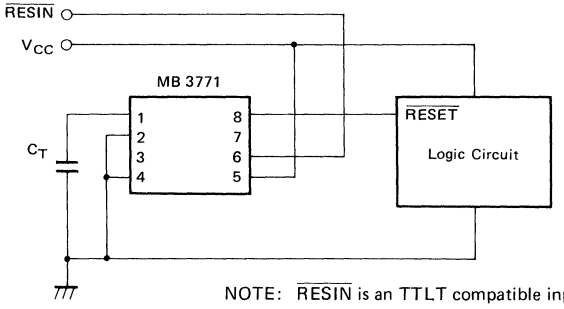
NOTE: 5V is monitored by V_{SA}, and generates $\overline{RESET}$ signal when V_{SA} detects voltage sagging. 12V is monitored by V_{SC}, and generates its detection signal at OUT_C.

The detection voltage of 12V monitoring and its hysterisis is determined by the following equations.

$$\text{Detection voltage} = \frac{R_1 + R_2 + R_3}{R_2 + R_3} V_{SC} \text{ (8.95 volts in the circuit above)}$$

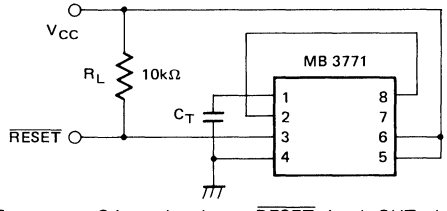
$$\text{Hysterisis width} = \frac{R_1 (R_3 - R_3 \| R_4)}{(R_2 + R_3)(R_2 + R_3 \| R_4)} V_{SC} \text{ (200mA in the circuit above)}$$

EXAMPLE 6: 5V Power Supply Monitor with forced $\overline{RESET}$ input



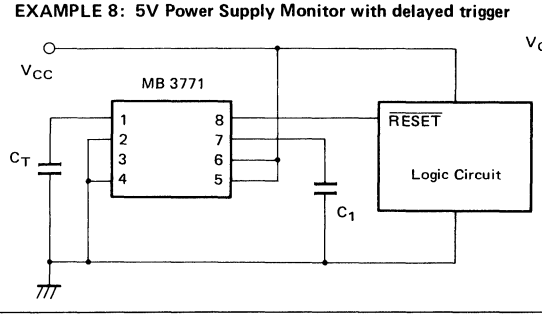
NOTE: $\overline{RESIN}$ is an TTLT compatible input.

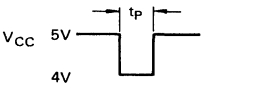
EXAMPLE 7: 5V Power Supply Monitor with Non-inverted RESET



NOTE: In this case, Comparator C is used to invert $\overline{RESET}$ signal. OUT_C is an open-collector output. R_L is used as a pull-up resistor.

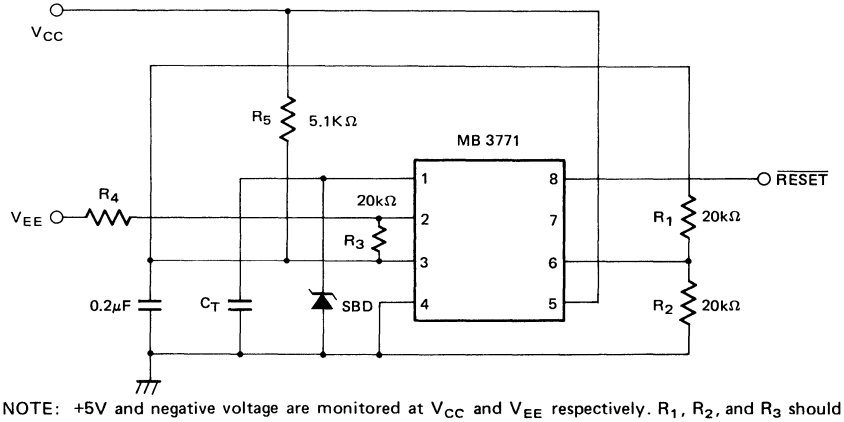
EXAMPLE 8: 5V Power Supply Monitor with delayed trigger





t_P min. = 40μs
when C_1 = 1000pF.

EXAMPLE 9: 5V and arbitrary negative voltage Monitor



NOTE: +5V and negative voltage are monitored at V_{CC} and V_{EE} respectively. R_1, R_2, and R_3 should be the same value. The negative detection voltage is determined by as the following equation.

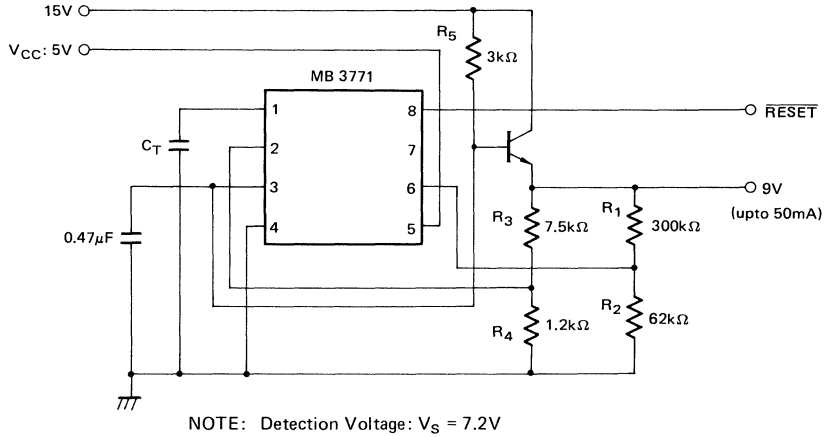
Detection voltage $V_S = V_{SB} - V_{SB} \cdot R_4/R_3$

Example: When V_{EE} = -5V and R_4 = 91kΩ, V_S = -4.37V.

4

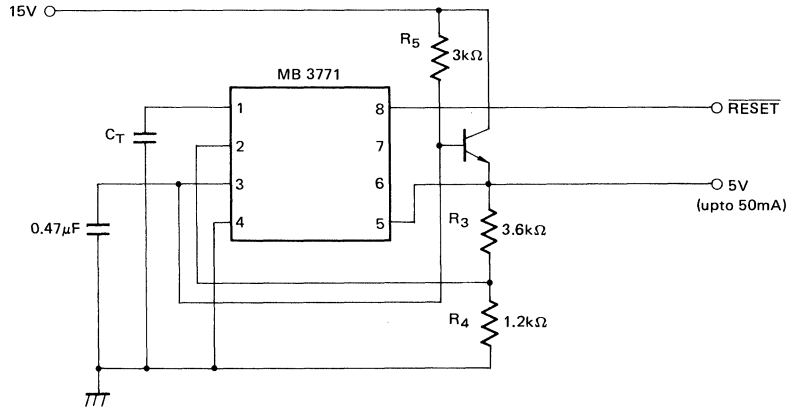
EXAMPLE 10: Reference Voltage Generation and Voltage Sagging Detection

Example 10a: 9V Reference Voltage Generation and 5V/9V Monitoring



NOTE: Detection Voltage: V_S = 7.2V

Example 10b: 5V Reference Voltage Generation and 5V Monitoring



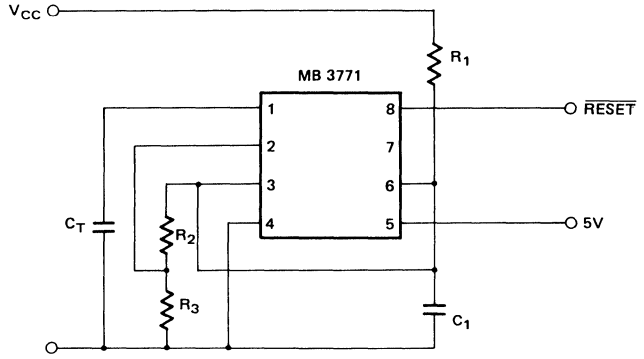
NOTE: Detection Voltage: V_S = 4.2V

NOTE: In the above examples, the output voltage and the detection voltage are determined by the following equations:

Output Voltage: $V_O = (R_3 + R_4) \cdot V_{SC}/R_4$

Detection Voltage: $V_S = (R_1 + R_2) \cdot V_{SB}/R_2$

Example 10c: 5V Reference Voltage Generation and 5V Monitoring

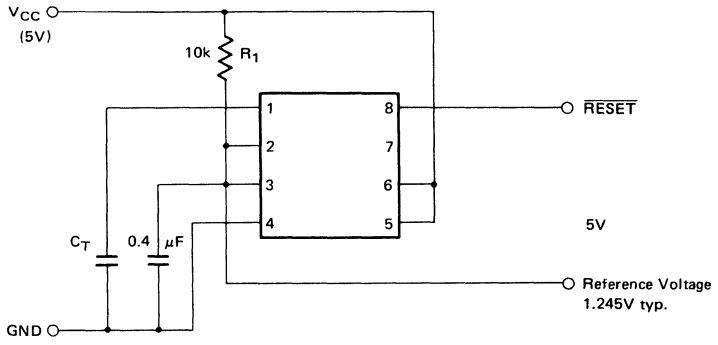


Using the reference table below, the value of R_1 can be determined. Where R_2 is 100kΩ, R_3 is 33kΩ, C_1 is 0.47μF.

Reference Table of R_1, V_{CC}, and the output current

V_{CC} [V]	R_1 [kΩ]	Output Current [mA]
40	11	<1.6
24	6.2	<1.4
15	4.7	<0.6

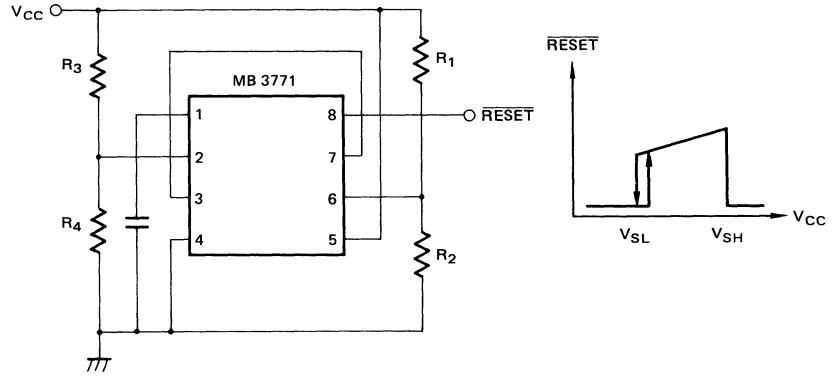
Example 10d: 1.245V Reference Voltage Generation and 5V Monitoring



NOTE: Resistor R_1 determines Reference current. Using 1.2kΩ as R_1, reference current is about 2mA.

4

EXAMPLE 11: Low Voltage and Over Voltage Detection



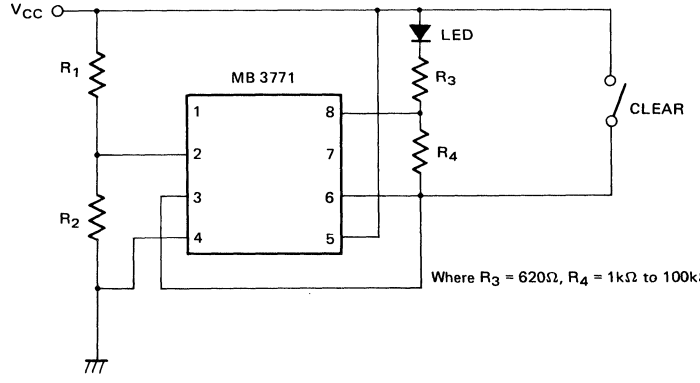
NOTE: V_{SH} has no hysteresis. When over voltage is detected, $\overline{RESET}$ is held in the constant time as well as when low voltage is detected.

$V_{SL} = (R_1 + R_2) \cdot V_{SB}/R_2$

$V_{SH} = (R_3 + R_4) \cdot V_{SC}/R_4$

EXAMPLE 12: Detection of Abnormal State of Power Supply System

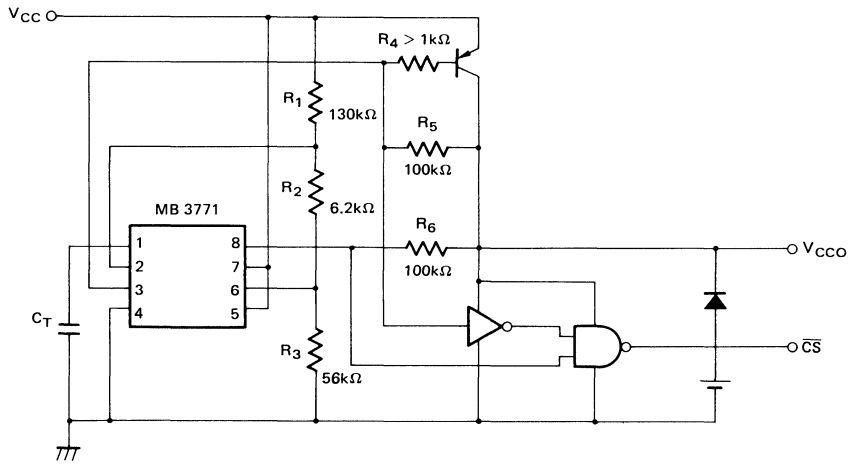
This example circuit detects abnormal low/over voltage of power supply voltage and is indicated by LED indicator. LED is reset by the CLEAR key.



NOTE: The detection levels of low/over voltages are determined by V_{SA}, and R_1 and R_2 respectively.

4

EXAMPLE 13: Back-up power supply system (V_{CC} = 5V)



NOTE: Use CMOS Logic and connect V_{DD} of CMOS logic with V_{CCO}.

The back-up battery works after $\overline{CS}$ goes high as $V_2 < V_1$.

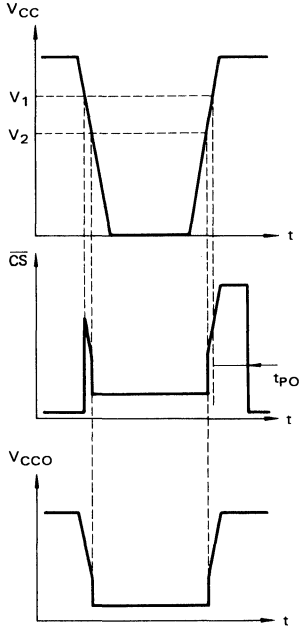
During t_{PO}, memory access is prohibited.

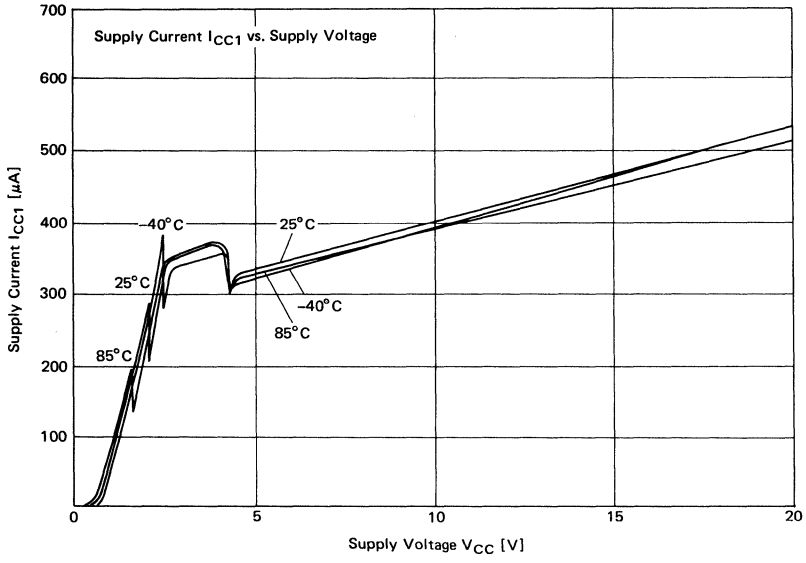
CS's threshold voltage V_1 is determined by the following equation:

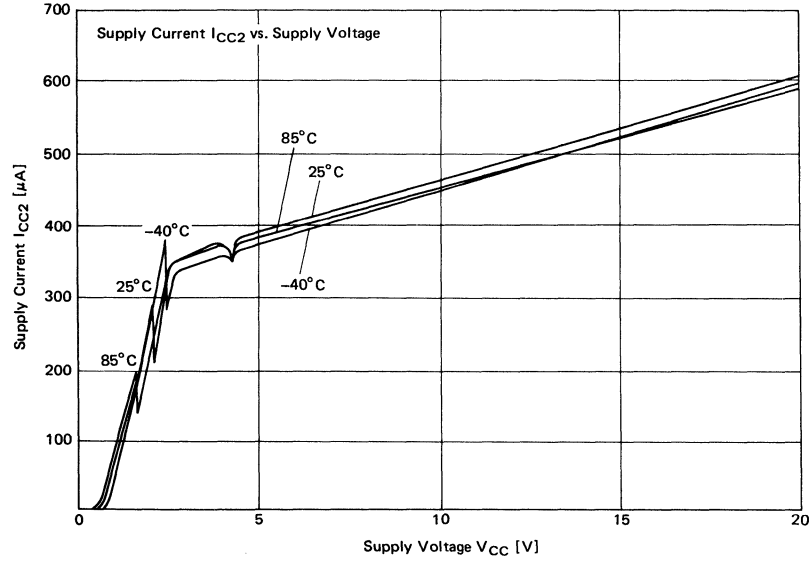
$$V_1 = (R_1 + R_2 + R_3)\ V_{SB}/R_3$$

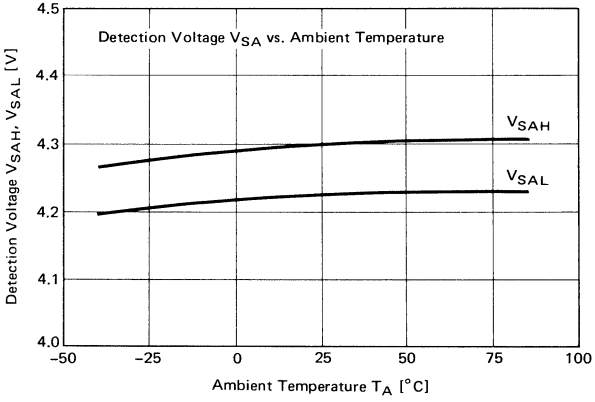
The voltage to change V_2 is provided as the following equation:

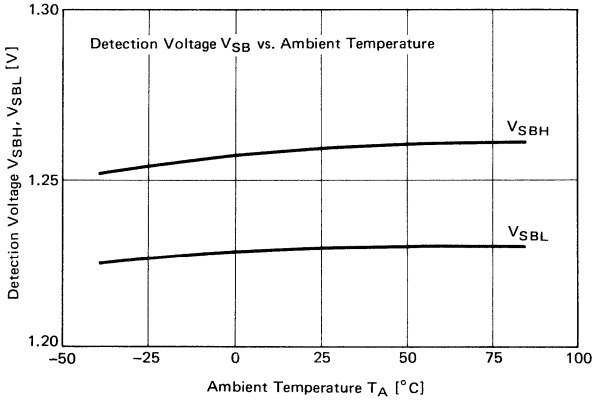
$$V_2 = (R_1 + R_2 + R_3) \cdot V_{SC}/(R_2 + R_3)$$

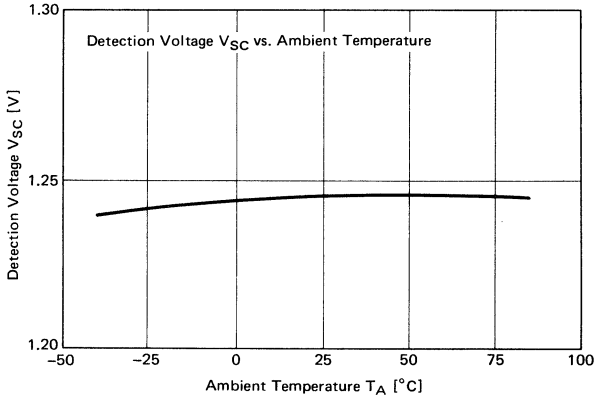



Supply Current I_{CC1} vs. Supply Voltage
Supply Current I_{CC1} [μA]
700
600
500
400
300
200
100
0
5
10
15
20
Supply Voltage V_{CC} [V]
-40°C
25°C
85°C
25°C
-40°C
85°C

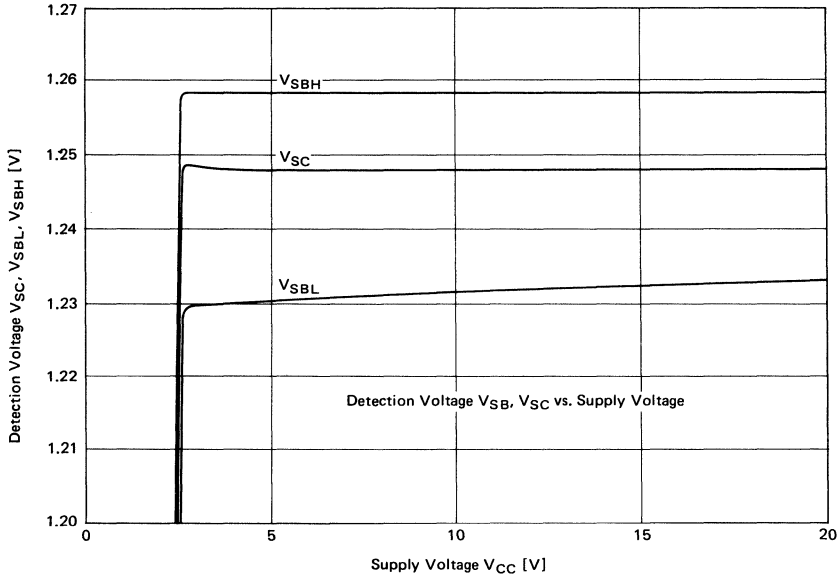

Supply Current I_{CC2} vs. Supply Voltage
Supply Current I_{CC2} [μA]
700
600
500
400
300
200
100
0
5
10
15
20
Supply Voltage V_{CC} [V]
85°C
25°C
-40°C
25°C
-40°C
85°C

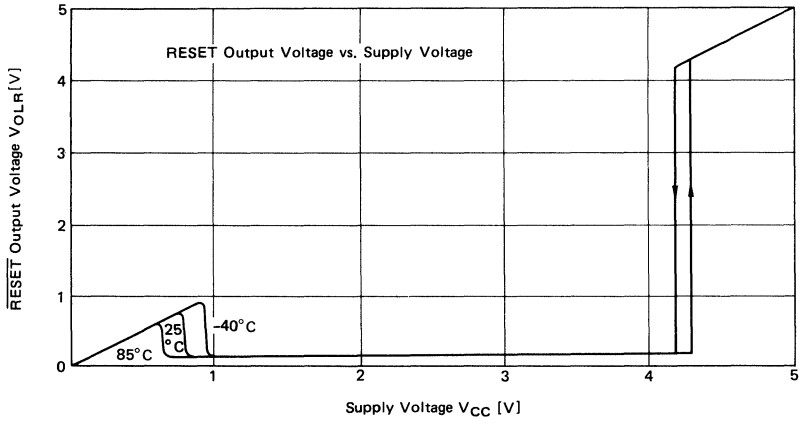

Detection Voltage V_{SA} vs. Ambient Temperature
Detection Voltage V_{SAH}, V_{SAL} [V]
4.5
4.4
4.3
4.2
4.1
4.0
V_{SAH}
V_{SAL}
–50
–25
0
25
50
75
100
Ambient Temperature T_A [°C]

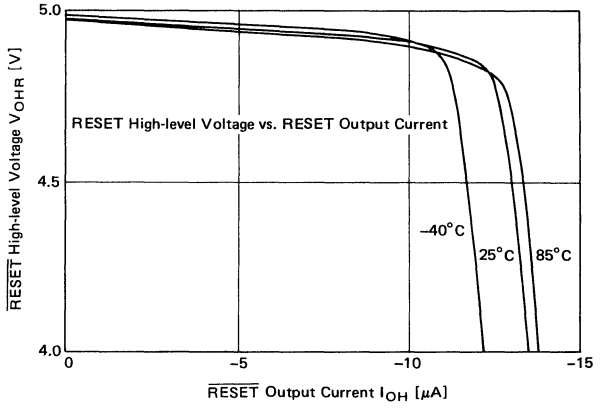

Detection Voltage V_{SB} vs. Ambient Temperature
Detection Voltage V_{SBH}, V_{SBL} [V]
1.30
1.25
1.20
V_{SBH}
V_{SBL}
–50
–25
0
25
50
75
100
Ambient Temperature T_A [°C]

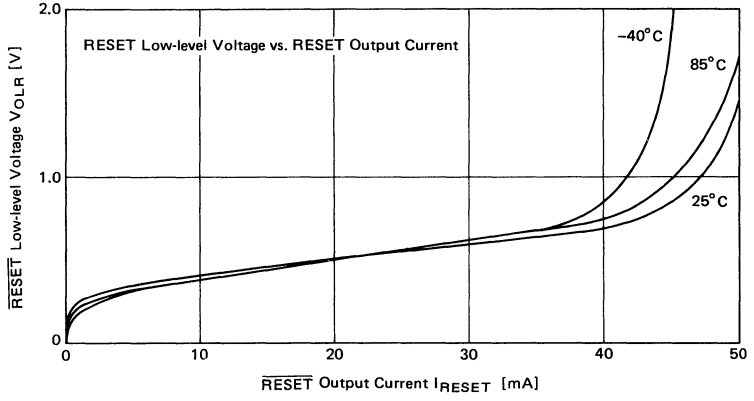

Detection Voltage V_{SC} vs. Ambient Temperature
Detection Voltage V_{SC} [V]
1.30
1.25
1.20
–50
–25
0
25
50
75
100
Ambient Temperature T_A [°C]

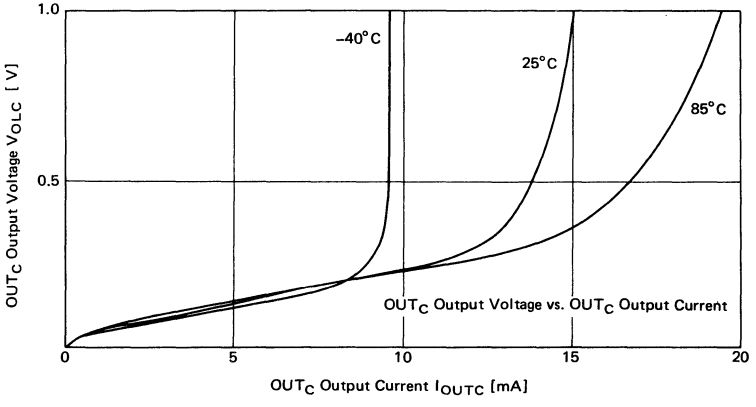
4


1.27
1.26
1.25
1.24
1.23
1.22
1.21
1.20
V_{SBH}
V_{SC}
V_{SBL}
Detection Voltage V_{SC}, V_{SBL}, V_{SBH} [V]
Detection Voltage V_{SB}, V_{SC} vs. Supply Voltage
0
5
10
15
20
Supply Voltage V_{CC} [V]


5
4
3
2
1
0
RESET Output Voltage vs. Supply Voltage
$\overline{RESET}$ Output Voltage V_{OLR} [V]
-40°C
25°C
85°C
1
2
3
4
5
Supply Voltage V_{CC} [V]

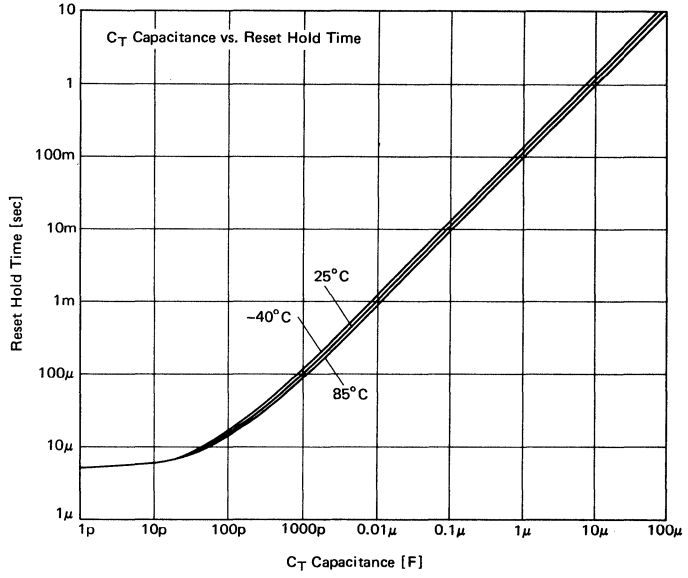

5.0
4.5
4.0
0
−5
−10
−15
RESET High-level Voltage vs. RESET Output Current
−40°C
25°C
85°C
RESET High-level Voltage V_{OHR} [V]
RESET Output Current I_{OH} [μA]

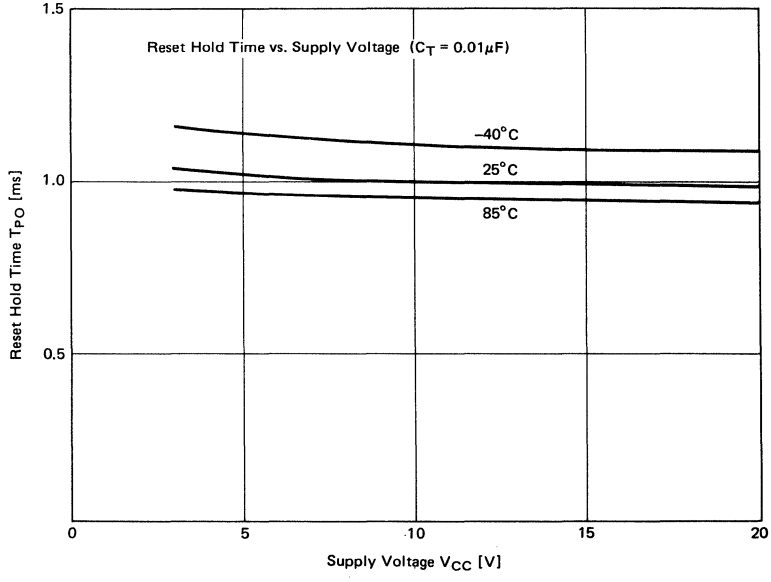

2.0
1.0
0
0
10
20
30
40
50
RESET Low-level Voltage vs. RESET Output Current
−40°C
85°C
25°C
RESET Low-level Voltage V_{OLR} [V]
RESET Output Current I_{RESET} [mA]


1.0
0.5
0
5
10
15
20
−40°C
25°C
85°C
OUT_C Output Voltage vs. OUT_C Output Current
OUT_C Output Voltage V_{OLC} [V]
OUT_C Output Current I_{OUTC} [mA]

4

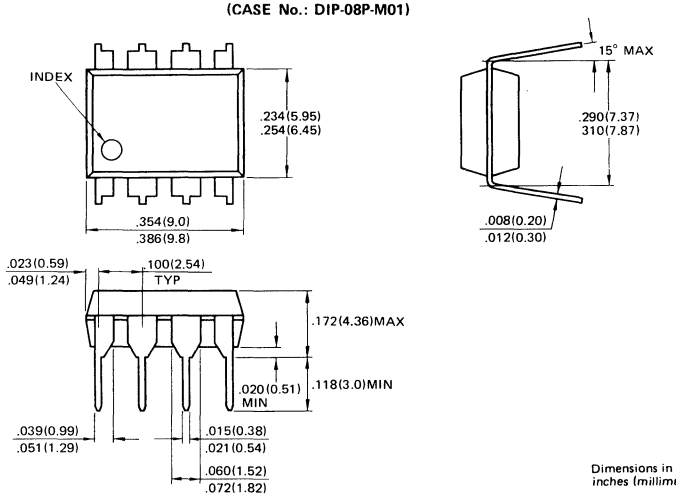
4


C_T Capacitance vs. Reset Hold Time
Reset Hold Time [sec]
10
1
100m
10m
1m
100μ
10μ
1μ
25°C
−40°C
85°C
1p
10p
100p
1000p
0.01μ
0.1μ
1μ
10μ
100μ
C_T Capacitance [F]


Reset Hold Time vs. Supply Voltage (C_T = 0.01μF)
Reset Hold Time T_{PO} [ms]
1.5
1.0
0.5
−40°C
25°C
85°C
0
5
10
15
20
Supply Voltage V_{CC} [V]

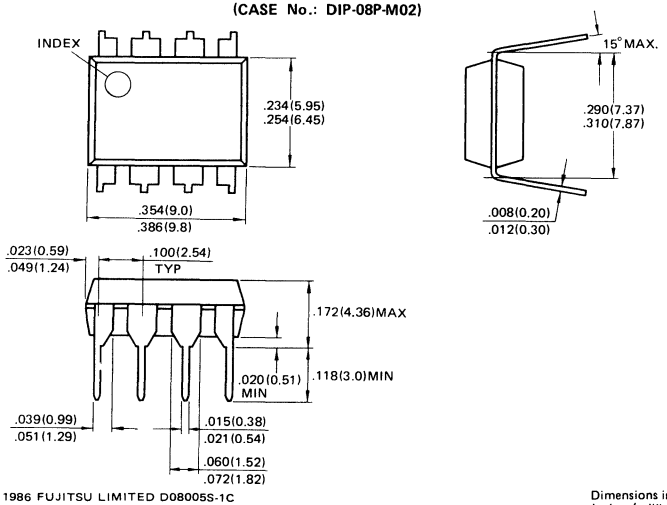
PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



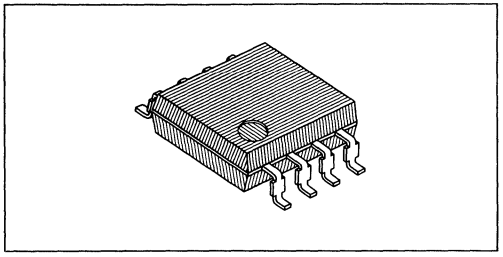
Dimensions in
inches (millimeters)

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M02)



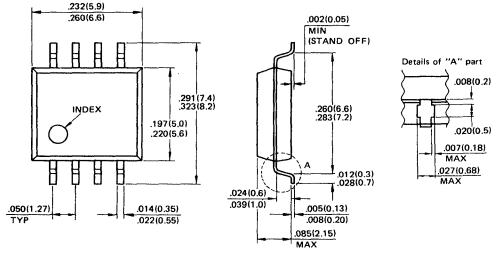
Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS



4

8-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-08P-M01)



Dimensions in inches
(millimeters)

September 1989
Edition 2.1

FUJITSU

DATA SHEET

MB3773

POWER SUPPLY MONITOR WITH WATCH–DOG TIMER

POWER SUPPLY MONITOR WITH WATCH-DOG TIMER

The Fujitsu MB3773 is designed to monitor the voltage level of a power supply (+5 V or an arbitrary voltage) in a microprocessor circuit, memory board in a large-size computer, for example. The MB3773 also contains a watch-dog timer function to detect uncontrol. Table status of processor and reset system/processor.

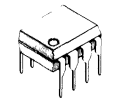
If the circuit's power supply deviates more than a specified amount, then the MB3773 generates a reset signal to the microprocessor. Thus, the computer data is protected from accidental erasure.

When the MB3773 does not receive the clock pulse from the processor in the specified period, the MB3773 generates a reset signal to the mciroprocessor.

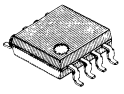
Using the MB3773 requires few external components. To monitor only a +5 volt supply, the MB3773 requires the connection of one external capacitor.

The MB3773 is available in an 8-pin Dual In-Line package space saving Flat Package, or a Single In-Line Package.

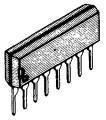
- Precision voltage detection (V_S = 4.2 V ±2.5%)
- Threshold level with hysterisis
- Low voltage output for reset signal (V_{CC} = 0.8 V typ.)
- Precision reference voltage output (V_{REF} = 1.245 V ±1.5%)
- External clock monitor and reset signal generator
- Negative-edge input watch-dog timer
- Minimal number of external components (one capacitor min.)
- Available in a variety of packages
  - 8-pin Dual In-Line Package
  - 8-pin Flat Package
  - 8-pin Single In-Line Package



PLASTIC PACKAGE
DIP-08P-M01

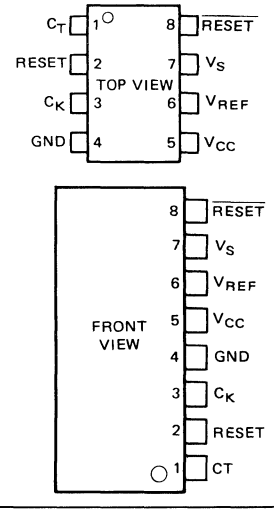


PLASTIC PACKAGE
FPT-08P-M01



PLASTIC PACKAGE
SIP-08P-M03

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

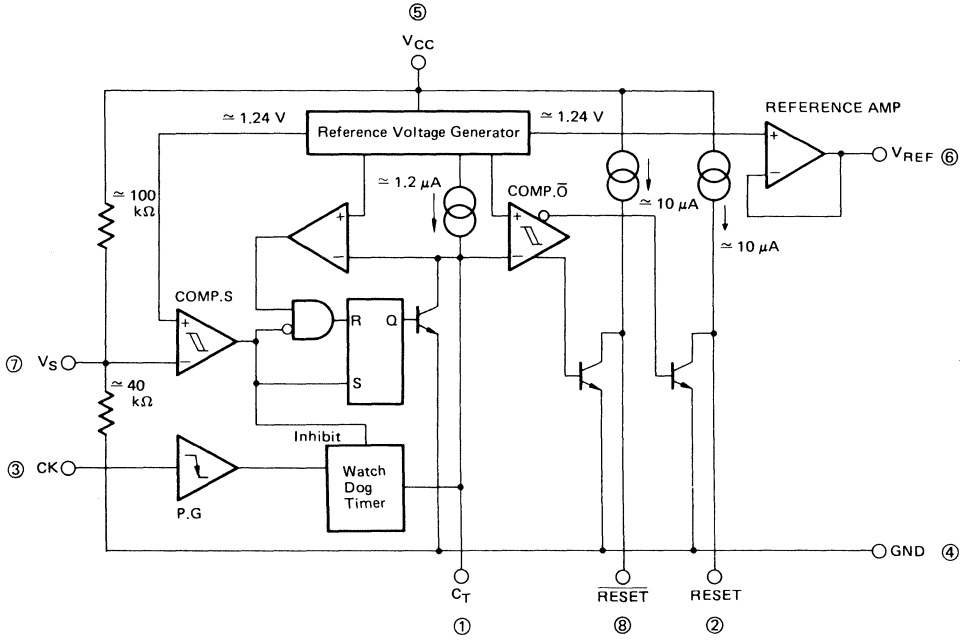
Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +18	V
Input Voltage	V_S	-0.3 to V_{CC} +0.3 (≦+18)	V
	V_{CK}	-0.3 to +18	V
$\overline{RESET}$, RESET Supply Voltage	V_{OH}	-0.3 to V_{CC} +0.3 (≦18)	V
Power Dissipation ($T_A \leqq 85°C$)	P_D	200	mW
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

Fig. 1 – MB3773 BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	+3.5 to +16	V
Reset, Reset Sink Current	I_{OL}	0 to 20	mA
V_{REF} Output Current	I_{OUT}	−200 to +5	mA
Watch Clock Setting Time	t_{WD}	0.1 to 1000	ms
Rising/Falling Time	t_{FC}, t_{RC}	<100	μs
Terminal Capacitance	C_T	0.001 to 10	μF
Operating Ambient Temperature	T_A	−40 to +85	°C

ELECTORICAL CHARACTERISTICS

(1) DC CHARACTERISTICS

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
Supply Current	Watch dog timer operating	I_{CC}		600	900	μA
Detection Voltage	V_{CC} ↘	V_{SL}	4.10	4.20	4.30	V
	T_A = −40°C to +85°C		4.05	4.20	4.35	
	V_{CC} ↗	V_{SH}	4.20	4.30	4.40	
	T_A = −40°C to +85°C		4.15	4.30	4.45	
Hysterisis Width	V_{CC} ↗↘	V_{HYS}	50	100	150	mV
Reference Voltage		V_{REF}	1.227	1.245	1.263	V
	T_A = −40°C to +85°C		1.215	1.245	1.275	
Reference Voltage Change Rate	V_{CC} = 3.5V to 16V	ΔV_{REF1}		3	10	mV
Reference Voltage Output Loading Change Rate	I_{OUT} = −200μA to +5μA	ΔV_{REF2}	−5		+5	mV
CK Threshold Voltage	T_A = −40°C to +85°C	V_{TH}	0.8	1.25	2.0	V
CK Input Current	V_{CK} = 5.0V	I_{IH}		0	1.0	μA
	V_{CK} = 0.0V	I_{IL}	−1.0	−0.1		
C_T Open Current	Watch Dog Timer Operating V_{CT} = 1.0V	I_{CTD}	7	10	14	μA
High Level Output Voltage	V_S open, I_{RESET} = −5μA	V_{OH1}	4.5	4.9		V
	V_S = 0V, I_{RESET} = −5μA	V_{OH2}	4.5	4.9		
Output Saturation Voltage	V_S = 0V, $I_{\overline{RESET}}$ = 3mA	V_{OL1}		0.2	0.4	V
	V_S = 0V, $I_{\overline{RESET}}$ = 10mA	V_{OL2}		0.3	0.5	
	V_S open, I_{RESET} = 3mA	V_{OL3}		0.2	0.4	
	V_S open, I_{RESET} = 10mA	V_{OL4}		0.3	0.5	
Output Sink Current	V_S = 0V, $V_{\overline{RESET}}$ = 1.0V	I_{OL1}	20	60		mA
	V_S open, V_{RESET} = 1.0V	I_{OL2}	20	60		

(1) DC CHARACTERISTICS (Continued)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
C_T Charge Current	Power on reset operating V_{CT} = 1.0V	I_{CTU}	0.5	1.2	2.5	μA
Min. Supply Voltage for $\overline{RESET}$	$V_{\overline{RESET}}$ = 0.4V $I_{\overline{RESET}}$ = 0.2mA	V_{CCL1}		0.8	1.2	V
Min. Supply Voltage for RESET	$V_{RESET} = V_{CC} - 0.1V$ R_L (2 pin – GND) = 1MΩ	V_{CCL2}		0.8	1.2	V

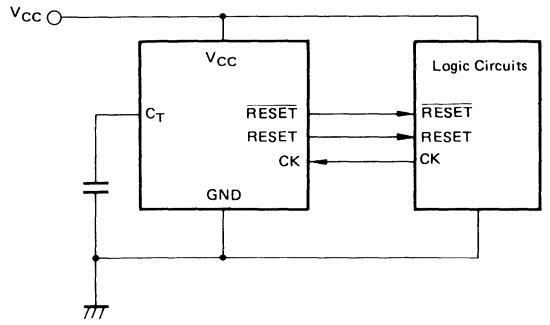
4

(2) AC CHARACTERISTICS

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
V_{CC} Input Pulse Width	V_{CC} 5V / 4V	T_{PI}	8.0			μs
CK Input Pulse Width	CK or	T_{CKW}	3.0			μs
CK Input Frequency		T_{CK}	20			μs
Watch Dog Timer Watching Time	C_T = 0.1μF	T_{WD}	5	10	15	ms
Watch Dog Timer Reset Time	C_T = 0.1μF	T_{WR}	1	2	3	ms
Rising Reset Hold Time	C_T = 0.1μF, V_{CC}	T_{PR}	50	100	150	ms
Output Propagation Delay Time from V_{CC}	$\overline{RESET}$, R_L = 2.2kΩ, C_L = 100pF	T_{PD1}		2	10	μs
	RESET, R_L = 2.2kΩ, C_L = 100pF	T_{PD2}		3	10	
Output Rising Time*	R_L = 2.2kΩ C_L = 100pF	t_R		1.0	1.5	μs
Output Falling Time*	R_L = 2.2kΩ C_L = 100pF	t_F		0.1	0.5	

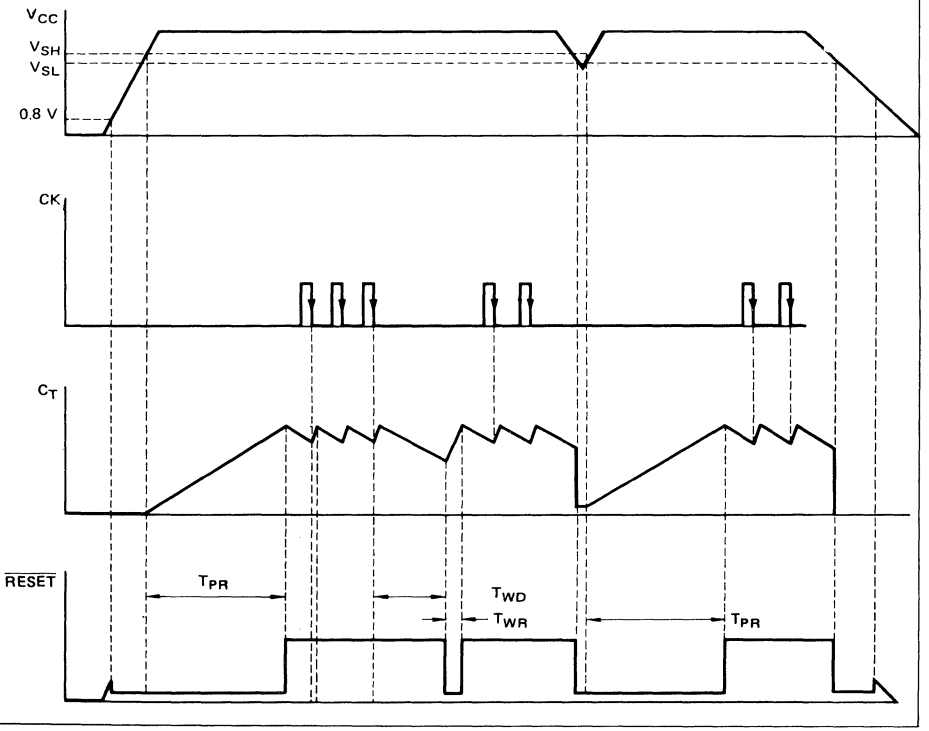
* Output Rising/Falling time are measured at 10% to 90% of Voltage.

Fig. 2 – MB 3773 BASIC OPERATION



C_T = 0.1 μF

$T_{PR} \fallingdotseq 1000 \cdot C_T$ (μF) (100 ms)
$T_{WD} \fallingdotseq 100 \cdot C_T$ (μF) (10 ms)
$T_{WR} \fallingdotseq 20 \cdot C_T$ (μF) (2 ms)



TYPICAL CHARACTERISTICS CURVES

Fig. 3 – SUPPLY CURRENT vs. SUPPLY VOLTAGE

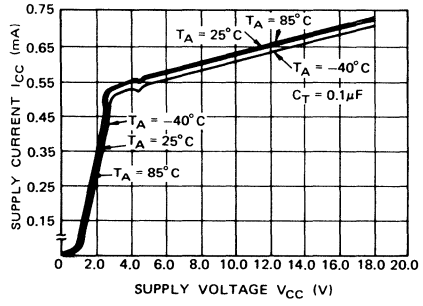


Fig. 4 – OUTPUT VOLTAG vs. SUPPLY VOLTAGE

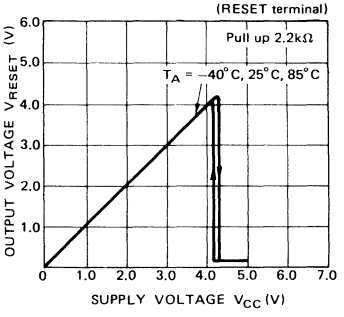


Fig. 5 – OUTPUT VOLTAGE vs. SUPPLY VOLTAGE

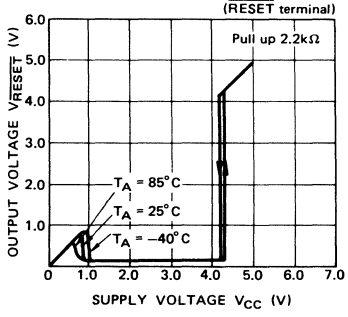


Fig. 6 – DETECTION VOLTAGE (V_{SH}, V_{SL}) vs. TEMPERATURE

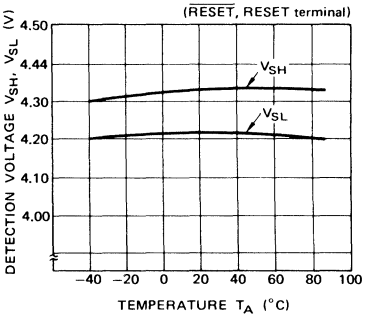


Fig. 7 – OUTPUT SATURATION VOLTAGE vs. OUTPUT SINK CURRENT

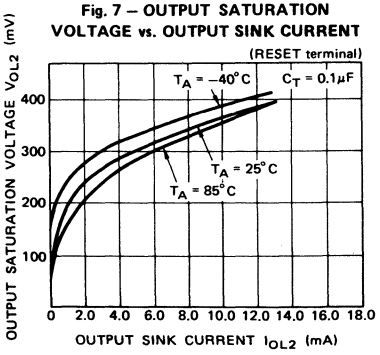
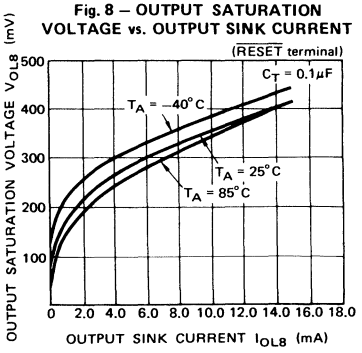


Fig. 8 – OUTPUT SATURATION VOLTAGE vs. OUTPUT SINK CURRENT



TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 9 – HIGH LEVEL OUTPUT VOLTAGE vs. HIGH LEVEL OUTPUT CURRENT

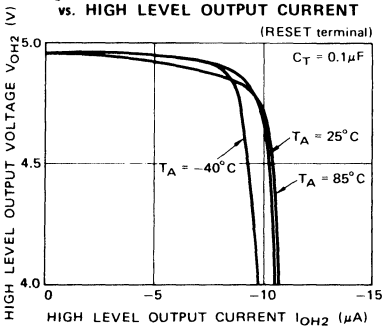


Fig. 10 – HIGH LEVEL OUTPUT VOLTAGE vs. HIGH LEVEL OUTPUT CURRENT

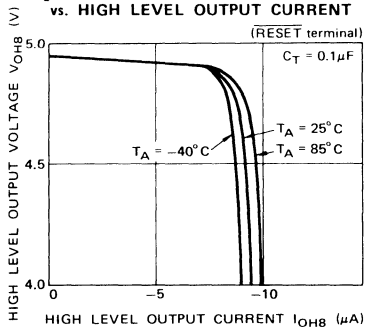


Fig. 11 – REFERENCE VOLTAGE vs. SUPPLY VOLTAGE

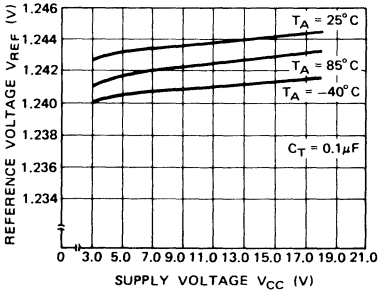


Fig. 12 – REFERENCE VOLTAGE vs. REFERENCE CURRENT

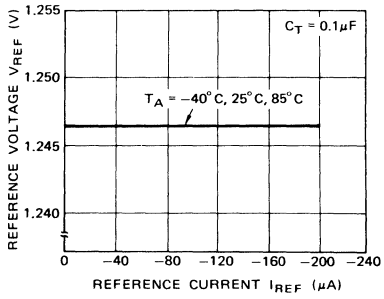


Fig. 13 – REFERENCE VOLTAGE vs. TEMPERATURE

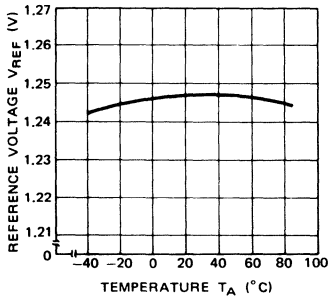
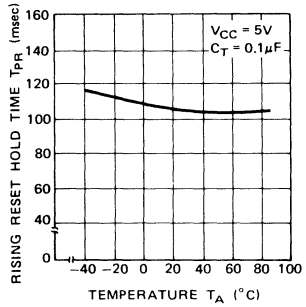


Fig. 14 – RISING RESET HOLD TIME vs. TEMPERATURE



4

TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 15 – RESET TIME vs. TEMPERATURE

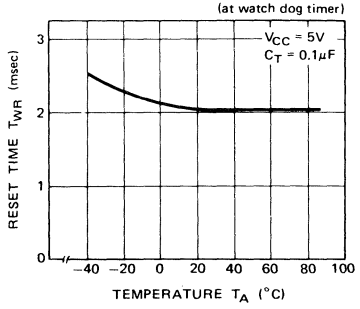


Fig. 16 – WATCH DOG TIMER WATCHING TIME vs. TEMPERATURE

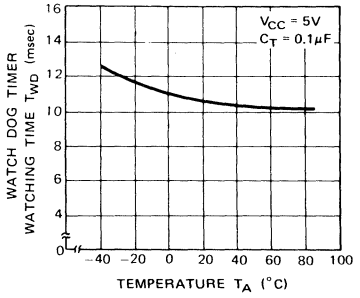


Fig. 17 – TERMINAL CPACITANCE vs. RISING RESET HOLD TIME

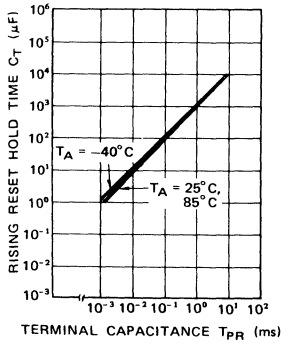


Fig. 18 – TERMINAL CAPACITANCE vs. RESET TIME

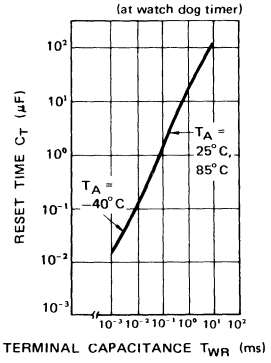


Fig. 19 – TERMINAL CAPACITANCE vs. WATCH DOG TIMER WATCHING TIME

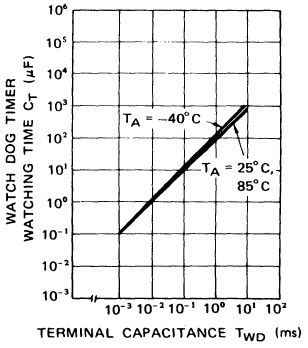
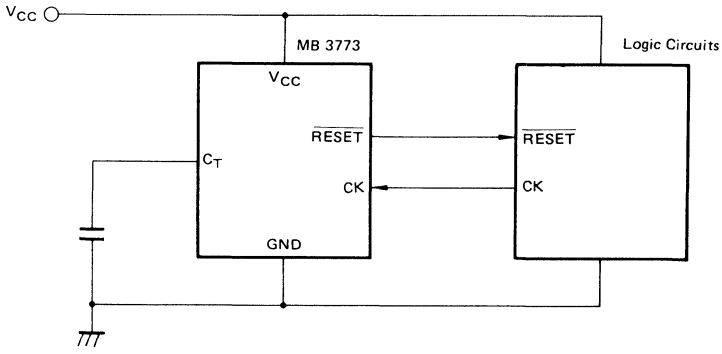
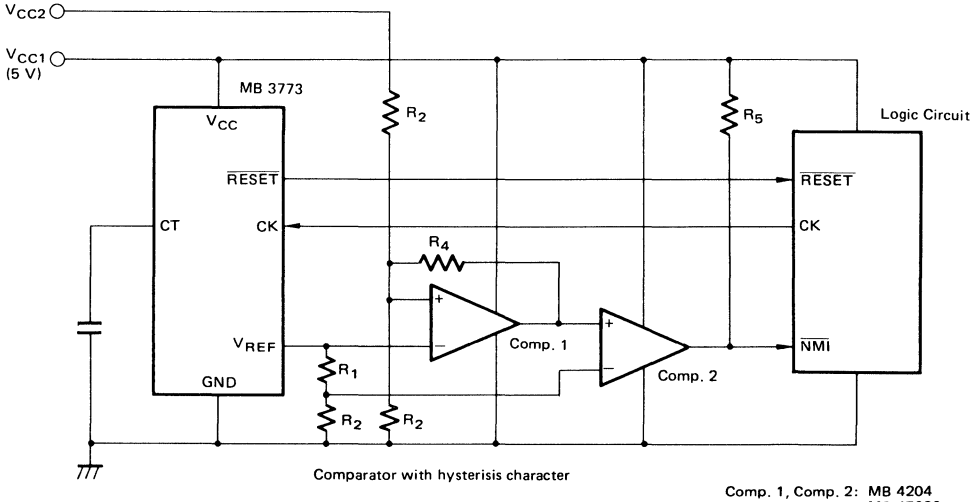


Fig. 20 – MB3773 APPLICATION EXAMPLE

- Sagging Monitor and Watch-Dog Timer



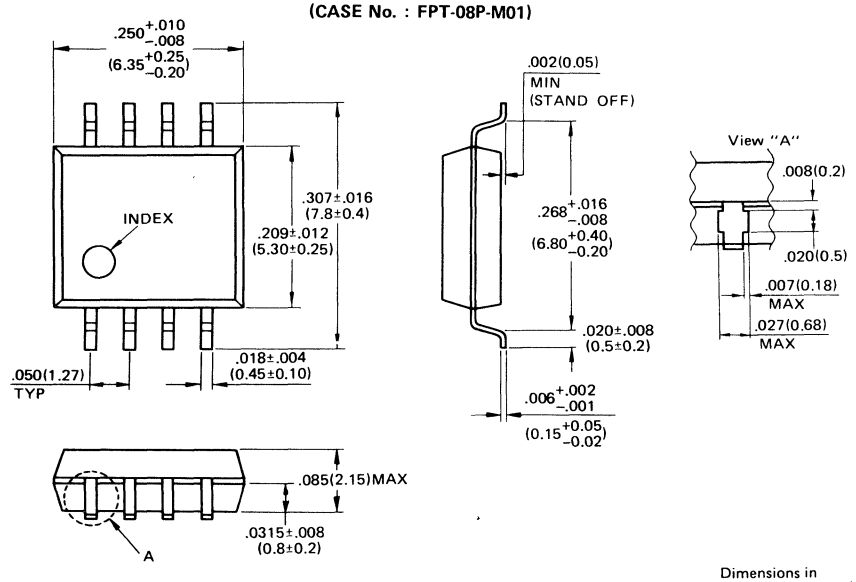
- Monitor for other power system



NOTE: When V_{CC2} in lower then the specified voltage, NMI low.
If over-voltage detection of V_{CC2}, Swap the inputs of comparator 2.

PACKAGE DIMENSIONS

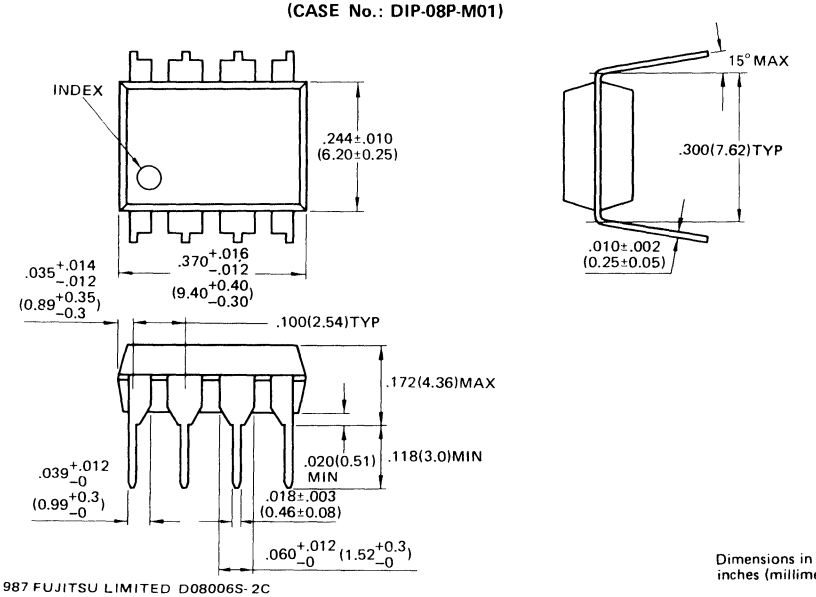
8-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-08P-M01)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (continued)

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)

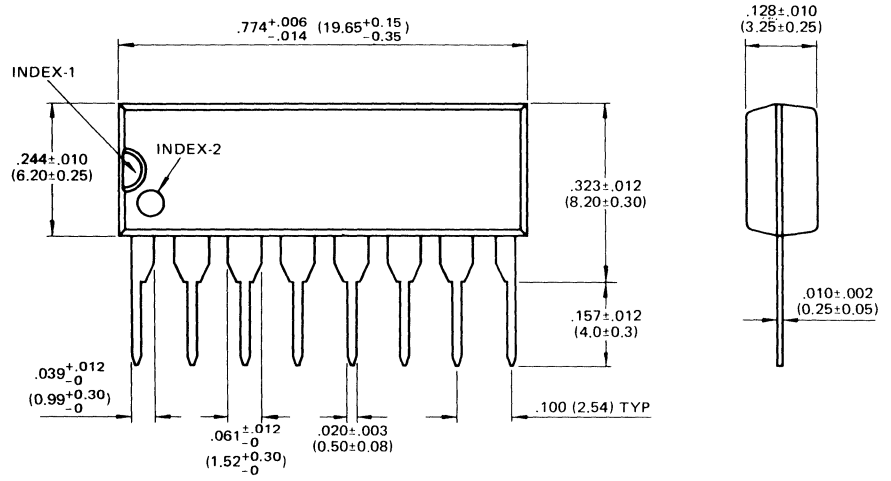


Dimensions in
inches (millimeters)

4

PACKAGE DIMENSIONS

8-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE No.: SIP-08P-M03)



Dimensions in
inches (millimeters)

FUJITSU

CAR AUDIO SYSTEM POWER SUPPLY IC

MB3774

November 1988
Edition 1.0

CAR AUDIO SYSTEM POWER SUPPLY IC

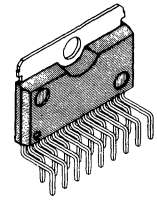
PRELIMINARY

The MB3774 is a multi-output, multi-function power supply IC, which was developed for car audio systems including digital tuning system.

The IC supplies 5 V to microcomputer, 9.15 V to RF stage for tuner and 8.4 V to an FM/AM receiver, a compact cassette tape deck and shared powers for them. It is easy to switch between power modes expect 5 V.

The multiplex drive method enables AM signals to be received even while the cassette tape deck is being used.

The MB3774 is a complete system power supply. The IC is mounted in a ZIP-17-pin small package to save space.

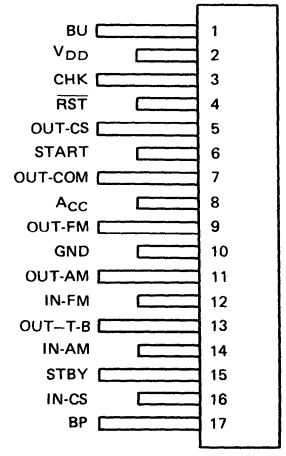


PLASTIC PACKAGE
ZIP-17P-M03

4

- Multiple output ports (5.0 V, 9.15 V. and four 8.4 V)
  Multiple function ports (4 control input ports and 3 control output ports)
- Suitable for car components for digital tuning system
  Control input for constant-voltage output on/off control (except 5V output)
- TTL and CMOS-compatible control input voltage
- Low saturation voltage (0.3 V typ.)
- Small backup current (350 μA typ.)
- Small package (ZIP-17 with radiation fin)
- Power supply surge voltage and overcurrent protection circuits

PIN ASSIGNMENT
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Input Voltage	V_{IN}	18	V
Input Surge Voltage	$V_{IN\ (S)}$	50 *	V
Power Dissipation	P_D	6.5 **	W
Storage Temperature	T_{STG}	-55 to +150	°C

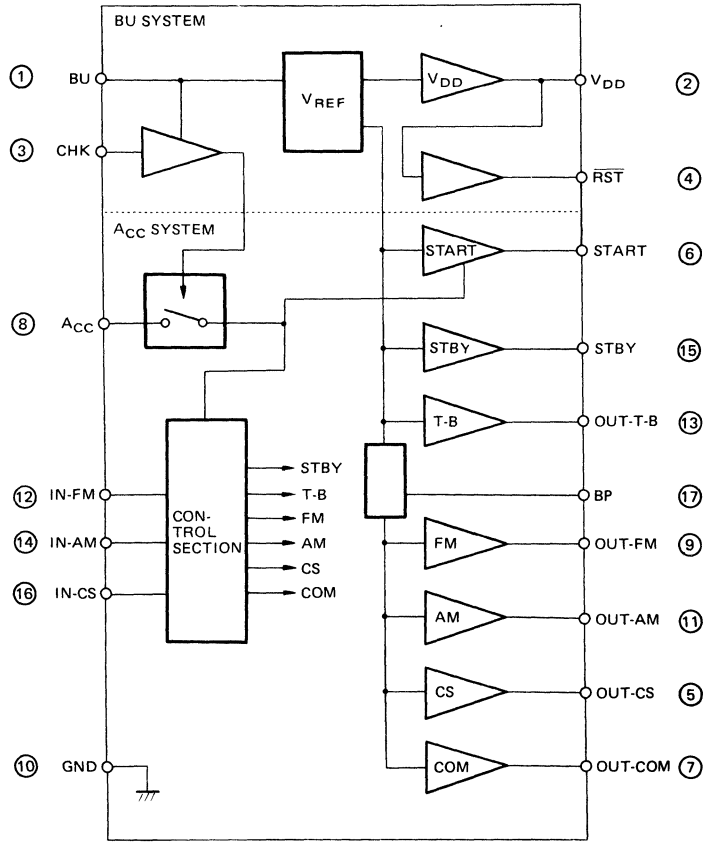
* ($t_r \geq 1$ms , $t_s \leq 0.2$sec)
** ($T_C \leq 85$ °C)

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

Fig. 1 – MB3774 BLOCK DIAGRAM



FUNCTIONAL EXPLANATIONS OF PINS

Terminal No.	Terminal name	Function
8	ACC	To be connected to the main battery.
1	BU	To be connected to the backup battery.
12	IN-FM	TTL or CMOS-level control can be supplied by output selection input with a microcomputer. (Function table and sequences 1 and 3)
14	IN-AM	
16	IN-CS	
3	CHK	ACC line connection check terminal. (Sequences 3 and 4) If the level is low, all outputs are turned off. The terminal uses hysteresis to compensate for AC line noise.
9	OUT-FM	Power supply for FM tuner such as FM IF and FM DEM.
11	OUT-AM	Power supply for AM tuner.
5	OUT-CS	Power supply for a cassette tape deck, such as equalizer and amplifier. Select IN-CS for this output.
7	OUT-COM	Power supply for common system functions such as tone control and volume/balance control. Select IN-FM, IN-AM, IN-CS for this output.
13	OUT-T-B	Power supply for the varicap for the first RF stage of tuner. Select IN-FM or IN-AM for this output.
15	STBY	Control output pin for a circuit that has a standby function, and that works on the same logic as OUT-COM.
6	START	Transmits system operation start information to the microprocessor according to the CHK voltage. (Sequence 4)
2	V_{DD}	Powers the microprocessor and is received power from the BU. The supply cannot be turned on or off by control input. (Sequence 2)
4	$\overline{RST}$	If V_{DD} goes down, this output terminal resets the microprocessor. (Sequence 5)
17	BP	Improves the ripple rejection ratio when the voltage is reduced. If no improvement,connect the terminal to ACC. For the usage, see the BP TERMINAL USAGE.
10	GND	Ground

4

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Voltage	$V_{IN(ACC)}$		10	13.2	16	V
Backup Input Voltage	$V_{IN(BU)}$		7.5	13.2	16	V
Output Current	I_O	T-B			10	mA
		OUT-FM			150	mA
		OUT-AM, OUT-CS			50	mA
		OUT-COM			100	mA
		START, STBY			5	mA
		V_{DD}			30	mA
Operating Temperature	T_{OP}		−40	25	85	°C

ELECTRICAL CHARACTERISTICS

Connect BP terminal to ACC terminal, $T_j = 25°C$

Parameter	Symbol	Condition			Standard			Unit
		I (mA)	V (V)		Min.	Typ.	Max.	
Output Voltage	V_{O1}	10	10	T-B	8.7	9.15	9.6	V
	V_{O2}	50	9.5	COM	8.0	8.4	8.8	V
		100	9.8		8.0	8.4	8.8	
	V_{O3}	100	9.5	FM	8.0	8.4	8.8	V
		150	9.8		8.0	8.4	8.8	
	V_{O4}	50	9.5	AM	8.0	8.4	8.8	V
	V_{O5}	50	9.5	CS	8.0	8.4	8.8	V
	V_{O6}	2	9.5	START	4.8	5.0	5.2	V
	V_{O7}	2	9.5	STBY	4.8	5.0	5.2	V
	V_{O8}	30	7.5	V_{DD}	4.8	5.0	5.2	V
Minimum I/O Voltage Difference	V_{DO1}	10		T-B		0.2	0.4	V
	V_{DO2}	50		COM		0.3	0.6	V
		100				0.6	0.9	
	V_{DO3}	100		FM		0.3	0.6	V
		150				0.6	0.9	
	V_{DO4}	50		AM		0.3	0.6	V
	V_{DO5}	50		CS		0.3	0.6	V
	V_{DO6}	2		START		1.5	2.1	V
	V_{DO7}	2		STBY		1.5	2.1	V
	V_{DO8}	30		V_{DD}		1.7	2.2	V
Output Offset Voltage	ΔV_O	50	10	$V_{O2} \sim V_{O5}$		60		mV
Input Stability	ΔV_{LINE}	10	10~16	V_{O1}		20		mV
		50	10~16	$V_{O2} \sim V_{O5}$		40		mV
		30	7.5~16	V_{O8}		25		mV

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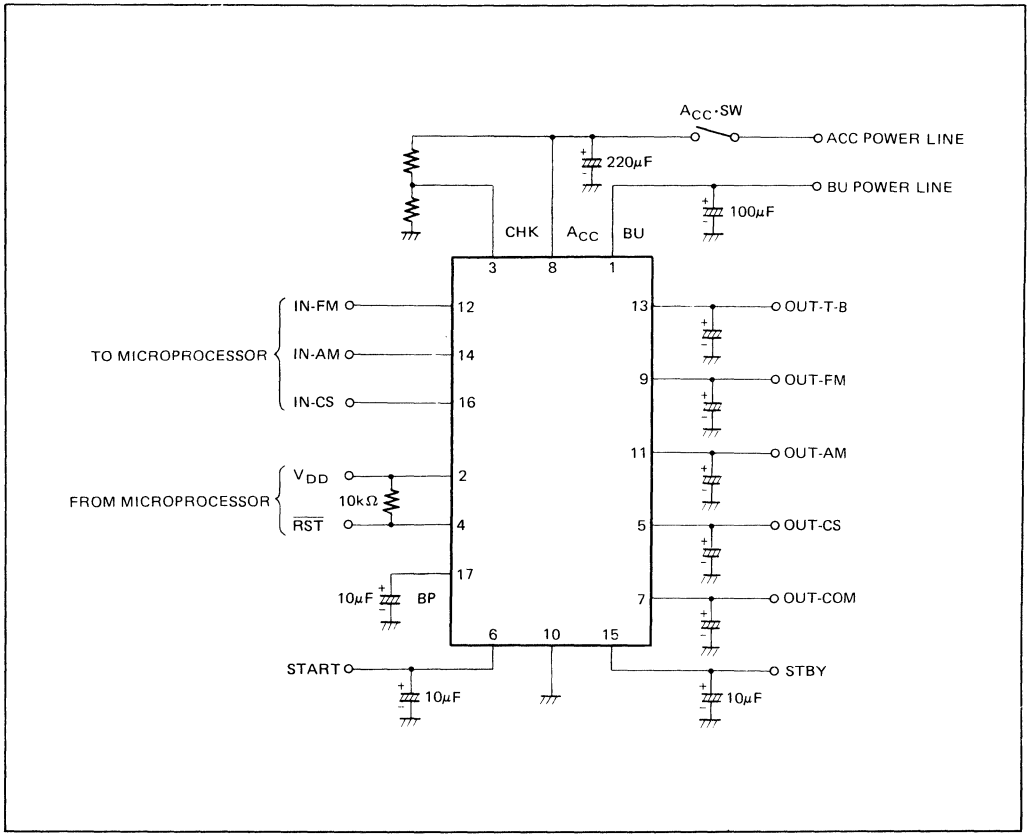
ELECTRICAL CHARACTERISTICS (continued)

Connect BP terminal to ACC terminal, $T_j = 25°C$

Parameter	Symbol	Condition			Standard			Unit
		I (mA)	V (V)		Min.	Typ.	Max.	
Load Stability	ΔV_{LOAD}	0~10	10	T-B		10		mV
		0~50	9.5	COM		30		mV
		0~100	9.8			60		mV
		0~100	9.5	FM		30		mV
		0~150	9.8			60		mV
		0~50	9.5	AM, CS		30		mV
		0~30	7.5	V_{DD}		10		mV
Control Terminal Input Voltage (FM, AM, CS)	V_{IH}		9.5		2.0		5.0	V
	V_{IL}		9.5		-0.3		0.8	
CHK Terminal Input Voltage	V_{IHC}		9.5		1.34		3.0	V
	V_{ILC}		9.5		-0.3		1.14	
Control Terminal Input Current (FM, AM, CS)	I_{IH}		9.5	$V_I = 5V$		50	70	μA
	I_{IL}		9.5	$V_I = 0V$	-32	-16		
CHK Terminal Input Current	I_{IHC}		9.5	$V_I = 1.34V$		1	10	μA
	I_{ILC}		9.5	$V_I = 0V$		0	5	
Hysteresis Width	V_{HYSC}			CHK		40		mV
	V_{HYSR}			$\overline{RST}$		160		
RST Terminal Output Voltage	V_{OHR}			$V_{DD} = 4.5V$	4.3			V
	V_{OHR}			$V_{DD} = 3.5V$			1.0	
ACC Terminal Input Current	I_{ACCO}			ACC = 10V $I_{DD} = 0mA$		2.5	4.0	mA
Backup Input Current	I_{BUO}			BU = 7.5V $I_{DD} = 0mA$		350	500	μA
Ripple Rejection Ratio	R.R.		13.2	$V_{IN} = 1V_{P-P}$		60		dB
Output Voltage Temperature Coefficient			10	V_{01}		0.045		%/°C
			9.5	V_{02}~V_{05}		0.041		
			7.5	V_{06}~V_{08}		0.025		

4

APPLICATION

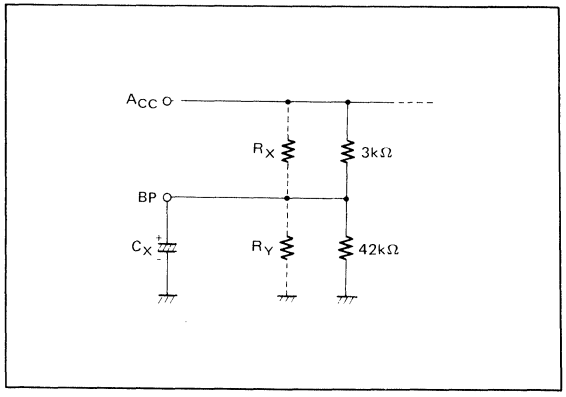


*Set the capacitance between the output and GND terminals from 10 μF to 470 μF, taking into account the operating conditions and the PC-board wiring pattern.
If the capacitance is too small, the load conditions and PC-board wiring may cause parasitic oscillation.

*Connecting a resistor between the BP and ACC terminals reduces the ripple rejection ratio. If a resistor is connected between the BP and GND terminals, the allowance increases.
The resistor must be at least 1 kΩ.

BP TERMINAL USAGE

The BP terminal is usually connected to the ACC terminal. However, if the resistor (R_x or R_y) shown in the figure below is added, the ripple rejection ratio of the 8.4V output system (V_{O2} to V_{O5}) can be improved when the voltage is low (non-stabilized ACC area).
The time constant (τ) is determined by C_x and the impedance (about 2.8kΩ if $R_x = \infty$. $R_y = \infty$) of the BP terminal ($\tau = C_x \times R$)



The output voltages when the R_x and R_y resistors are added can be calculated from the following expressions:

With R_x → $V_O = V_{IN\,(ACC)} \times 42\ k\Omega \div (3k\Omega \,//\, R_x + 42\ k\Omega)$

With R_y → $V_O = V_{IN\,(ACC)} \times 42\ k\Omega \,//\, R_y \div (42\ k\Omega \,//\, R_y + 3\ k\Omega)$

Note: The standard value of minimum I/O voltage is based on the conditions that $R_x = 0\Omega$ and $Ry = \infty$

The R_x value must be 20 kΩ or more because the output voltage is limited by the minimum I/O voltage difference.

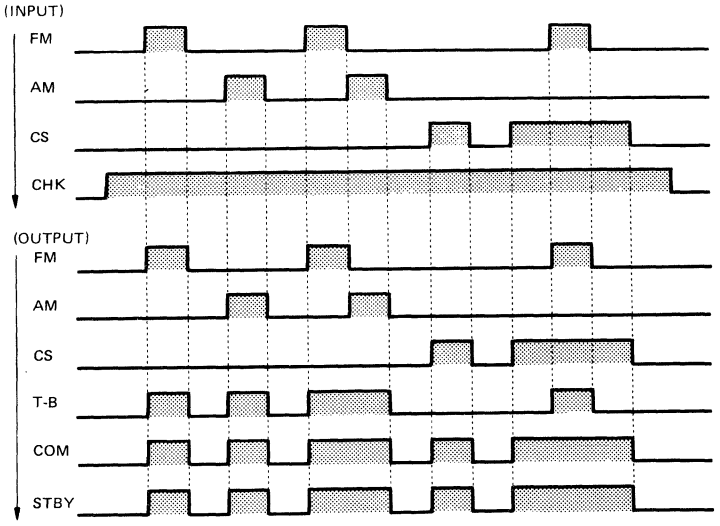
FUNCTION TABLE

ACC Detection	Input			Output						
CHK	FM	AM	CS	FM	AM	CS	T-B	COM	STBY	
L	X	X	X							All outputs off
H	L	L	L							All outputs off
H	H	L	L	A			A	A	A	FM selection
H	L	H	L		A		↓	↓	↓	AM selection
H	L	L	H			A	↓	↓	↓	CS selection
H	H	H	L	A	A		A	↓	↓	FM & AM selection
H	H	L	H	A		A	↓	↓	↓	FM & CS selection
H	L	H	H		A	A	↓	↓	↓	AM & CS selection
H	H	H	H	A	A	A	↓	↓	↓	All outputs on

A : Active status
X : Don't care
Note: Double selection increases heat dissipation. So the power consumption and layout must be designed carefully.

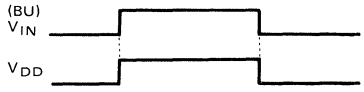
CONTROL SEQUENCE

(1) ACC system input



CONTROL SEQUENCE (continued)

(2) BU system I/O



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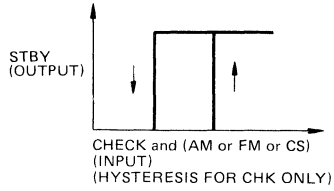
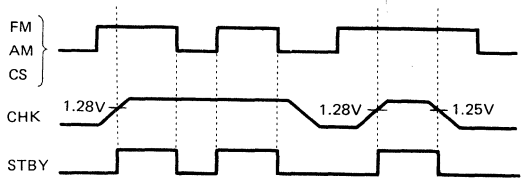
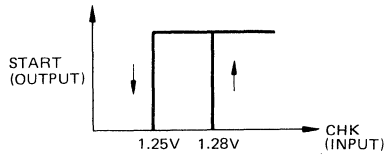
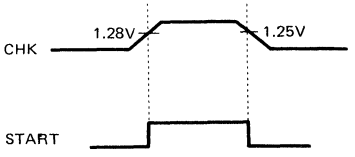
(3) Standby output (ACC system)



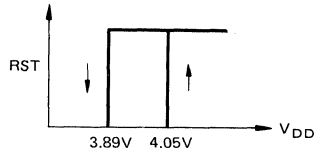


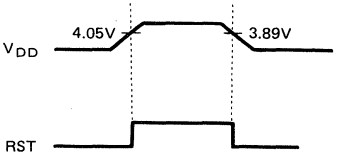
(4) Start output (ACC system)



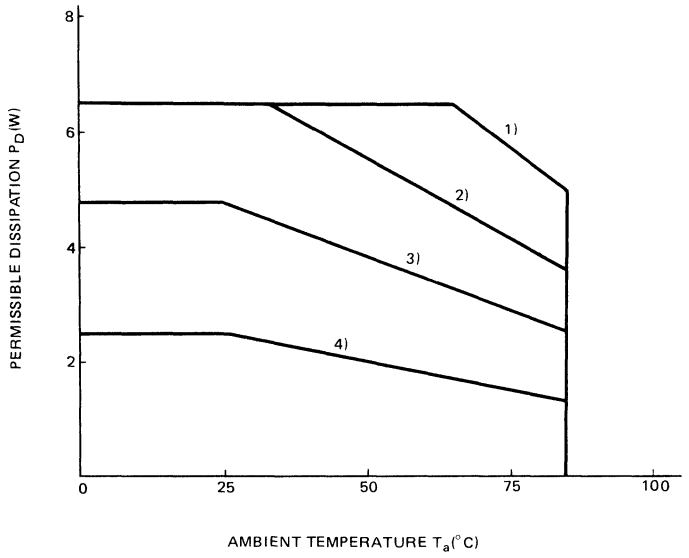


(5) Reset output (BU system)





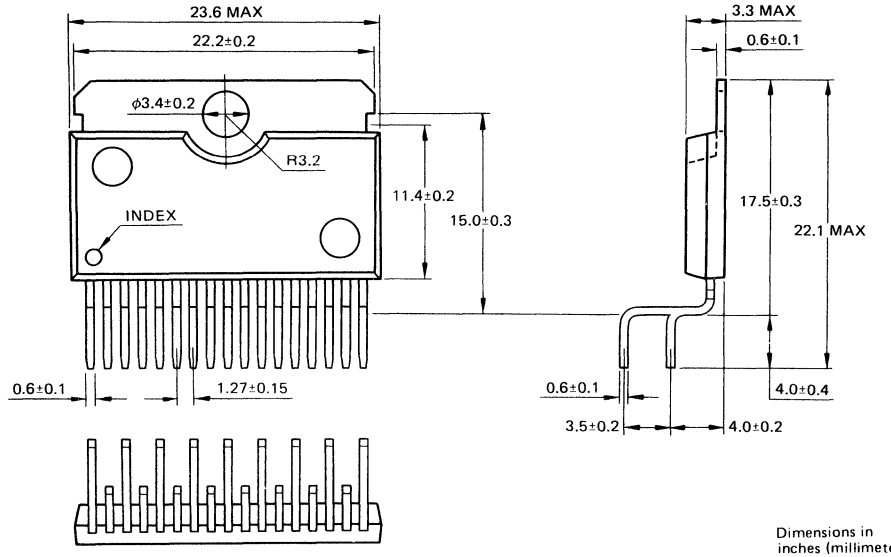
POWER DERATING CHARACTERISTICS



Conditions
1) 50 cm² x 2 mm-thick radiation board
2) 25 cm² x 2 mm-thick radiation board
3) 10 cm² x 2 mm-thick radiation board
4) No radiation board

PACKAGE DIMENSIONS

17-LEAD PLASTIC ZIGZAG-IN-LINE PACKAGE
(CASE No.: ZIP-17P-M03)



Dimensions in inches (millimeters)

FUJITSU

BATTERY BACKUP IC

MB3780A

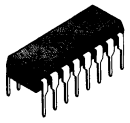
August 1989
Edition 1.0

BATTERY BACKUP IC

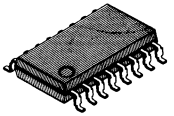
The Fujitsu MB3780A monolithic battery backup IC is fabricated with a bipolar linear IC technology, and is suitable for power supply of SRAM, ROM and Logic ICs.

The MB3780A generats a reset signal when power supply's ON/OFF or abnormal power supply. The MB3780A provides switching function for back up between modes such as primary bateery which is non-chargeable and secondary battery which is chargeable. All necessary functions for battery backup are available on a chip. The MB3780A is available in 16-pin Dual In-Line, space saving Flat package, or 20-pin shrink small outline which is suitable for memory card.

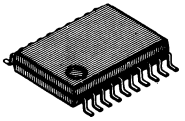
- Input circuit power consumption when unloaded: 1.0 mA typical
- Output drive current: 200 mA maximum (can be incleased with an external transistor)
- Input/output differential voltage: 230 mV typical
- Input loss voltage detection value: 4.2V ± 2.5%
- Onchip power-on reset circuit
- Low voltage detection value by primary battery: 2.65V, 2.37V
- Onchip secondary battery
- Output current at backup: 500 μA maximum
- Leak current at backup: 0.5 μA or less



PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M02



PLASTIC PACKAGE
FPT-20P-M04

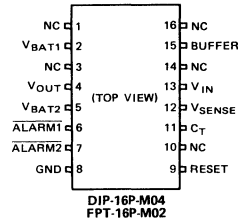
ABSOLUTE MAXIMUM RATINGS (See Note) (T_A = 25°C)

Ratings	Symbol	Value	Unit
Input Voltage	V_{IN}	−0.3 to 7	V
Battery Voltage	V_{BAT}	−0.3 to 7	V
Output Reset Voltage	V_{RESET}	7	V
Output Alarm Voltage	V_{ALARM}	7	V
Output Current	I_{OUT}	250	mA
Output Buffer Current	I_{BUF}	55	mA
Power Dissipation	P_D	*900	mW
		**540	mW
		***450	mW
Operating Temperature	T_{OP}	−30 to 85	°C
Storage Temperature	T_{STG}	−55 to 125	°C

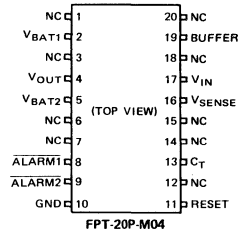
NOTE: * $T_A \leqq 25°C$ DIP-16P-M04
** $T_A \leqq 25°C$ FPT-16P-M02
*** $T_A \leqq 25°C$ FPT-20P-M04

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT



DIP-16P-M04
FPT-16P-M02



FPT-20P-M04

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

4

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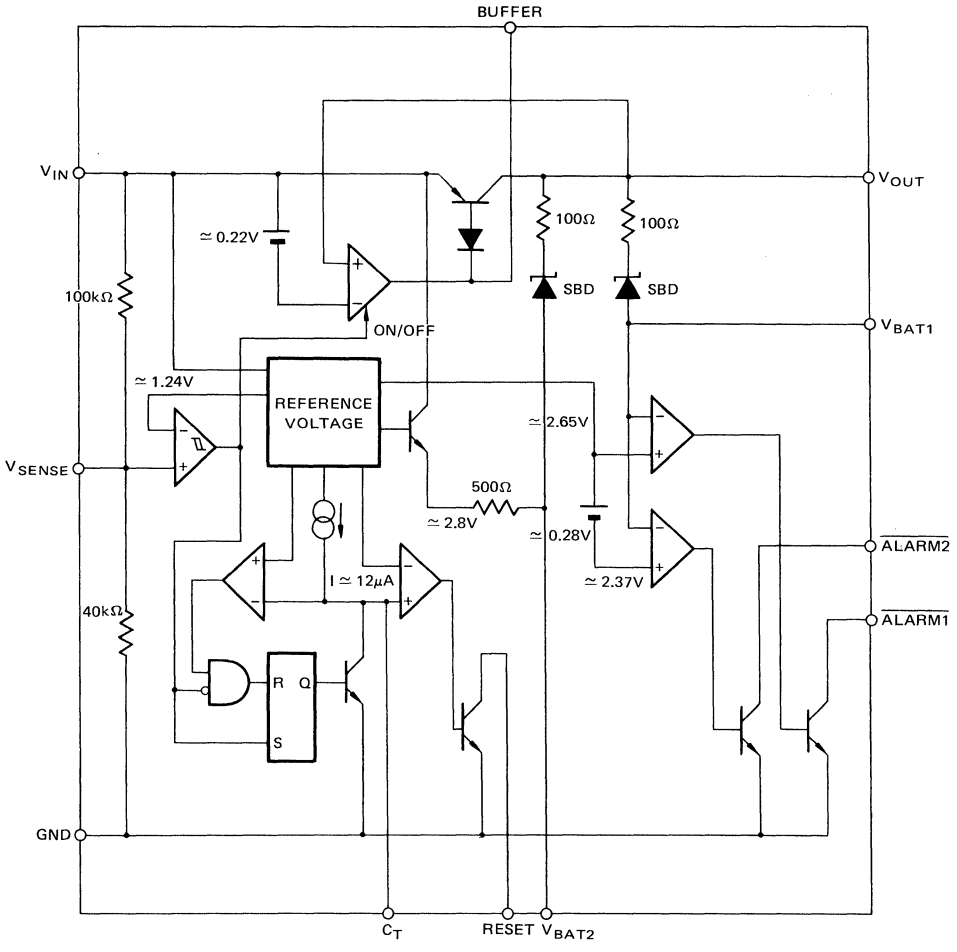
Fig. 1 – MB3780A EQUIVALENT CIRCUIT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Voltage	V_{IN}		5.0	6.0	V
Output Reset Current	I_{RESET}			3	mA
Output Alarm Current	I_{ALARM}			3	mA
Secondary Battery Charging Current	I_{CHARGE}	−3			mA
Output Current	I_{OUT}			200	mA
Output Buffer Current	I_{BUF}			50	mA
Backup Current	I_{BU}			500	μA
Operating Temperature	T_{op}	−30		85	* °C
		−30		70	** °C

NOTE: * DIP-16P-M04
** FPT-16P-M02, FPT-20P-M04

ELECTRICAL CHARACTERISTICS

(V_{IN} = 5V, T_A = 25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Whole Device						
Input Current	I_{IN1}	I_{OUT} = 0mA		1.0	1.5	mA
	I_{IN2}	I_{OUT} = 200mA		225	250	mA
	I_{IN3}	V_{IN} = 4.0V		1.0	1.5	mA
Backup System						
Input/Output Defferential Voltage	DV_1	I_{OUT} = 0mA	0.18	0.21	0.24	V
	DV_2	I_{OUT} = 200mA	0.19	0.22	0.25	V
Output Delay Time	tr_O	C_O = 0.01μF, C_T = 0		2.0	10	μs
Output Buffer Current	I_{BUF}	V_O = 4.7V, V_{BUF} = 4.0V	50			mA
Buffer Leak Current	I_{OHB}	V_{IN} = 0V, V_{BUF} = 4.5V			100	nA
Power Supply Monitoring System						
Input Loss Voltage	V_{INL}	V_{IN} 	4.10	4.20	4.30	V
	V_{INH}	V_{IN} 	4.20	4.30	4.40	V
Hysteresis Width of Input Loss Voltage	DV_{IN}	V_{INH}–V_{INL}	50	100	150	mV
Output Reset Voltage	V_{RESET}	I_{RESET} = 3mA		0.15	0.4	V
Output Reset Leak Current	I_{OHR}	V_{IN} = 4.0V, V_{RESET} = 6V		0	100	nA
Reset Pulse Width	t_{PO}	C_T = 0.01μF	0.5	1.0	1.5	ms
Input Pulse Width	t_{PI}	C_T = 0.01μF, V_{IN} 	5			μs
Reset Output Rising Time	tr_R	C_T = 0.01μF R_L = 5.1kΩ, C_L = 100pF		2.0	3.0	μs
Reset Output Falling Time	tf_R			0.1	0.5	μs
Reset Output Propagation Delay Time	tpd_R	C_T = 0.01μF		2.0	10	μs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 5V, T_A = 25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Primary Battery Monitoring System						
Low Voltage Detection (Primary)	V_{BATL1}	V_{BAT1} ↘	2.55	2.65	2.75	V
	V_{BATH1}	V_{BAT1} ↗	2.59	2.69	2.79	V
Hysteresis Width of Low Voltage Detection (Primary)	DV_{BAT1}	$V_{BATH1}-V_{BATL1}$	20	40	60	mV
Low Voltage Detection (Secondary)	V_{BATL2}	V_{BAT1} ↘	2.27	2.37	2.47	V
	V_{BATH2}	V_{BAT1} ↗	2.31	2.41	2.51	V
Hysteresis Width of Low Voltage Detection (Secondary)	DV_{VAT2}	$V_{BATH2}-V_{VATL2}$	20	40	60	mV
Differential Detected Low Voltage	DV_{BAT}	$V_{VATL1}-V_{BATL2}$	0.26	0.28	0.30	V
Input Current	I_{VATA}	V_{BAT} = 3V, V_{IN} = 5V	−100		500	nA
	I_{VATB}	V_{BAT} = 3V, V_{IN} = 0V	−100		500	nA
Output Differential Voltage	DV_{B1}	I_{BAT1} = 100μA		0.30	0.35	V
Alarm Output Voltage	V_{ALARM1}	I_{ALARM1} = 3mA		0.15	0.4	V
	V_{ALARM2}	I_{ALARM2} = 3mA		0.15	0.4	V
Alarm Output Leak Current	I_{OHA1}	V_{ALARM1} = 6V		0	100	nA
	I_{OHA2}	V_{ALARM2} = 6V		0	100	nA
Alarm Output Rising Time	tr_A	R_L = 5.1kΩ, C_L = 100pF		2.0	3.0	μs
Alarm Output Falling Time	tf_A			0.1	0.5	μs
Alarm Output Propagation Delay Time	tpd_A	50mV over drive		2.0	10	μs
Secondary Battery Monitoring System						
Output Voltage	V_{CHG}	I_{CHG} = −10μA	2.65	2.80	2.95	V
Charging Current	I_{CHGL}	V_{CHG} = 2.0V	0.6	1.6	3.0	mA
	I_{CHGH}	V_{CHG} = 3.3V	−1	0	1	μA
Defferential Output Voltage	DV_{B2}	I_{BAT2} = 100μA		0.30	0.35	V

NOTE: R_L and C_L are output logic of load resistance and capacitor.

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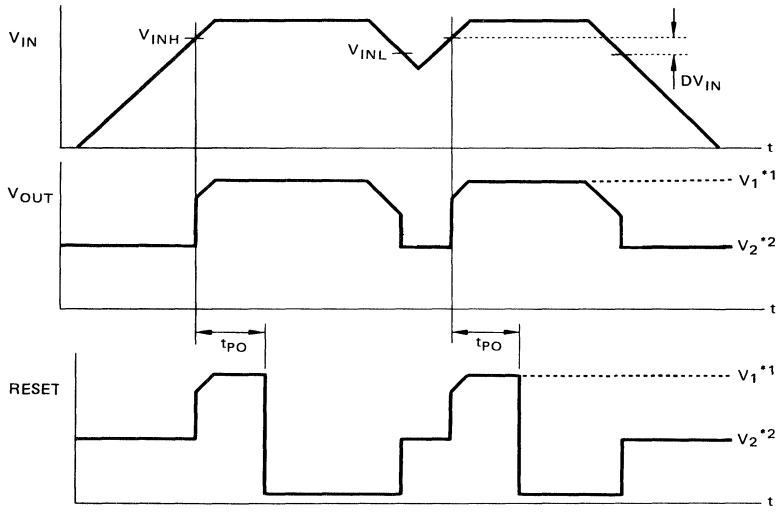
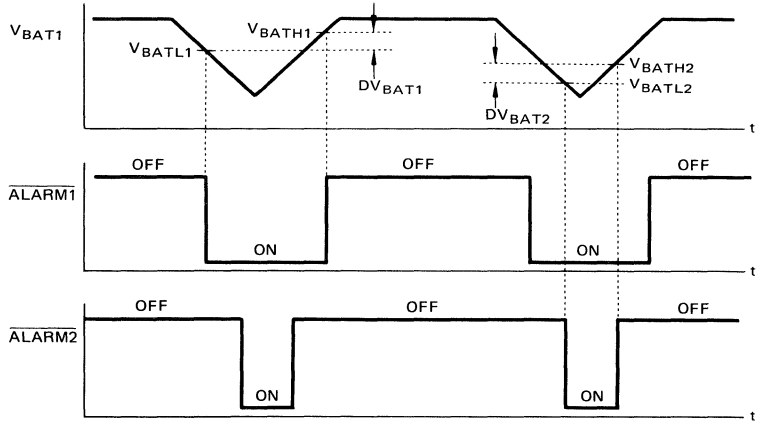
FUNCTION EXPLANATION

Fig. 2 – MB3780A INPUT ON/OFF OPERATION



*1) $V_1 = V_{IN} - DV_1$
*2) $V_2 = V_{BAT1} - DV_{B1}$

Fig. 3 – MB3780A ALARM OPERATION



Condition: $V_{IN} \geqq V_{INH}$

TIMMING DIAGRAM

Fig. 4 – MB3780A RISING/FALLING TIME OF RESET AND ALARM

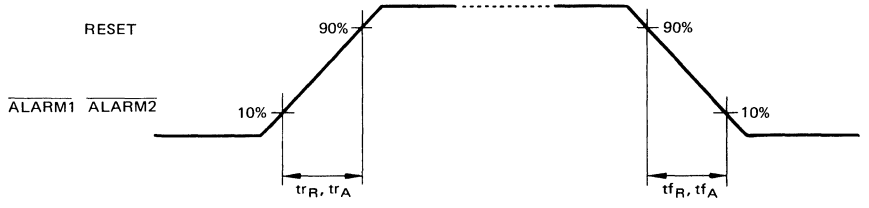
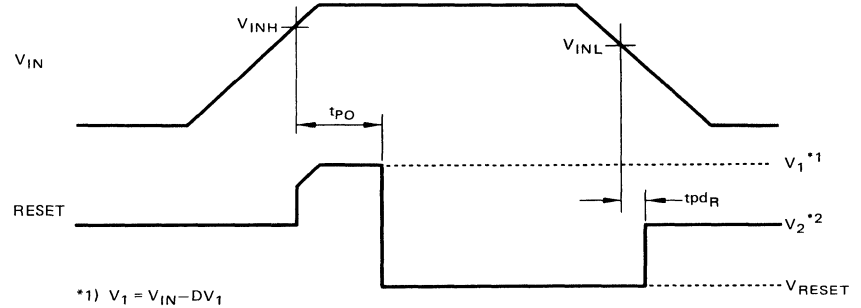
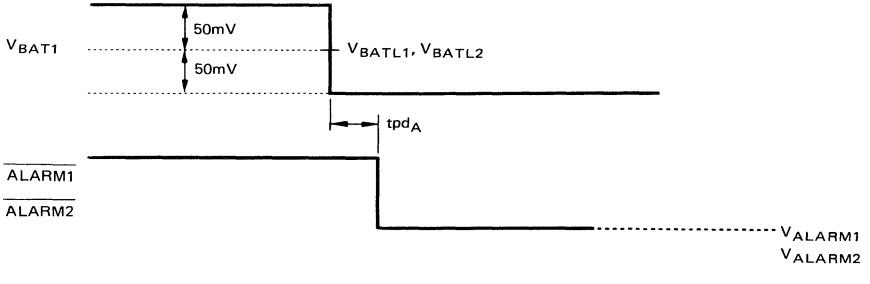


Fig. 5 – MB3780A RESET PULSE WIDTH, OUTPUT RESET PROPAGATION DELAY TIME



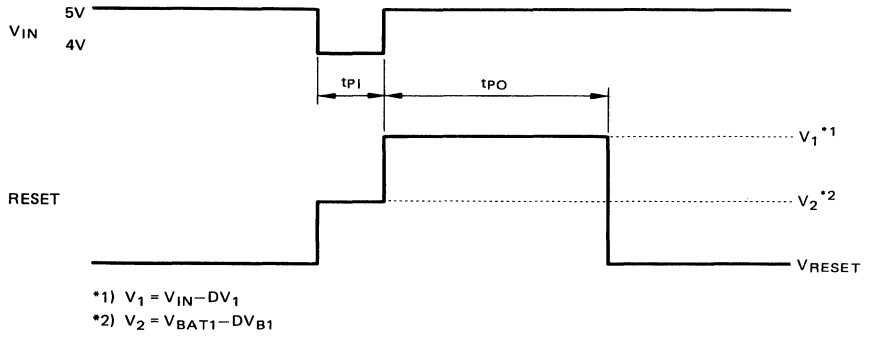
*1) $V_1 = V_{IN} - DV_1$
*2) $V_2 = V_{BAT1} - DV_{B1}$

Fig. 6 – MB3780A OUTPUT ALARM PROPAGATION DELAY TIME



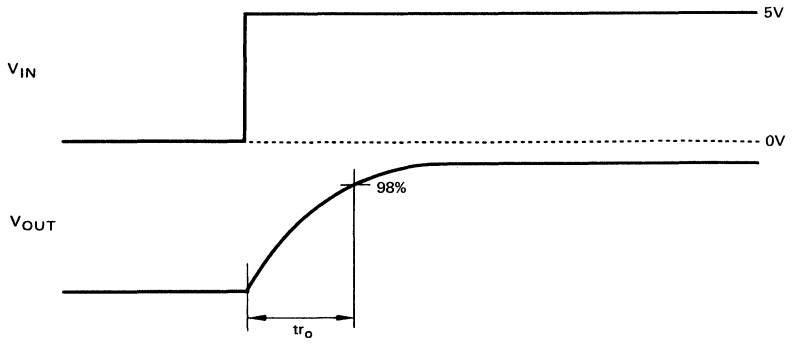
TIMING DIAGRAM (continued)

Fig. 7 – MB3780A INPUT PULSE WIDTH

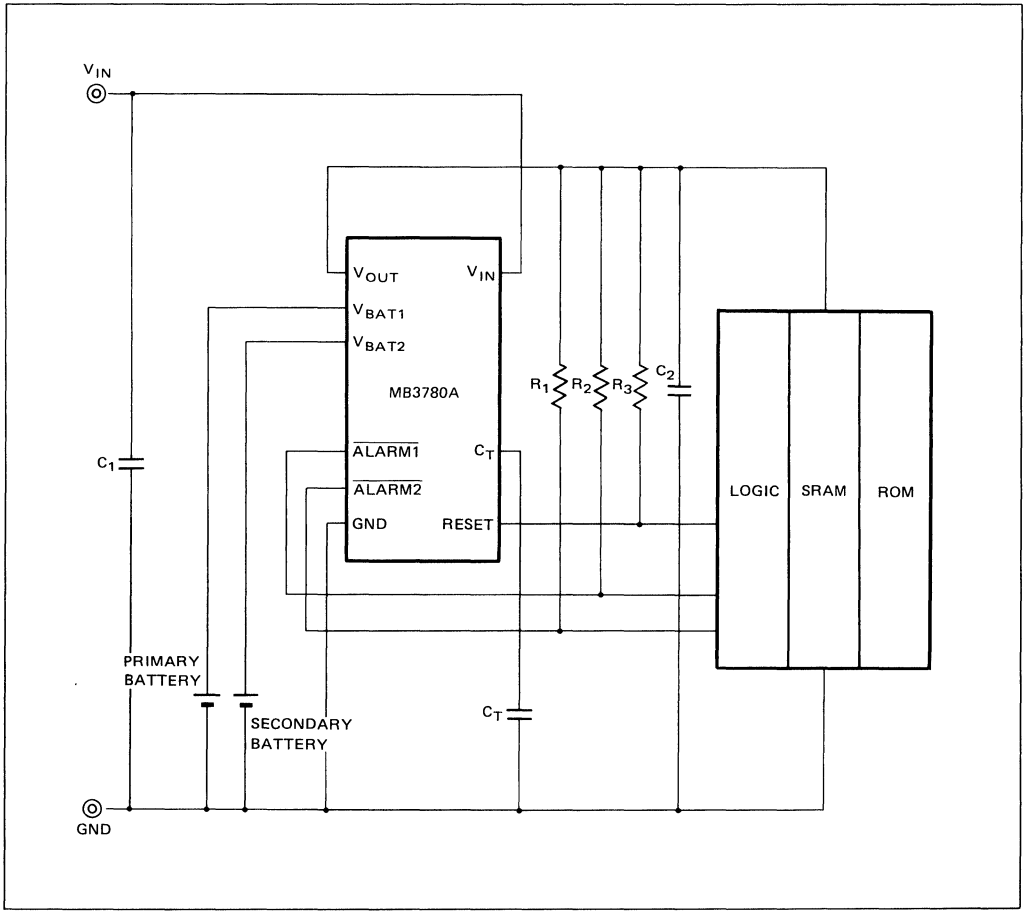


*1) $V_1 = V_{IN} - DV_1$
*2) $V_2 = V_{BAT1} - DV_{B1}$

Fig. 8 – MB3780A OUTPUT VOLTAGE PROPAGATION DELAY TIME



APPLICATION EXAMPLE



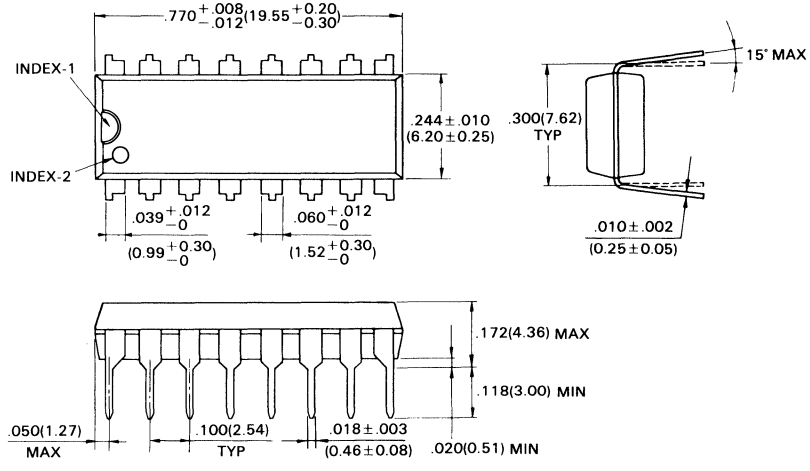
NOTE: The value of C_1 and C_2 should be more than 0.022μF.

4

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-16P-M04)

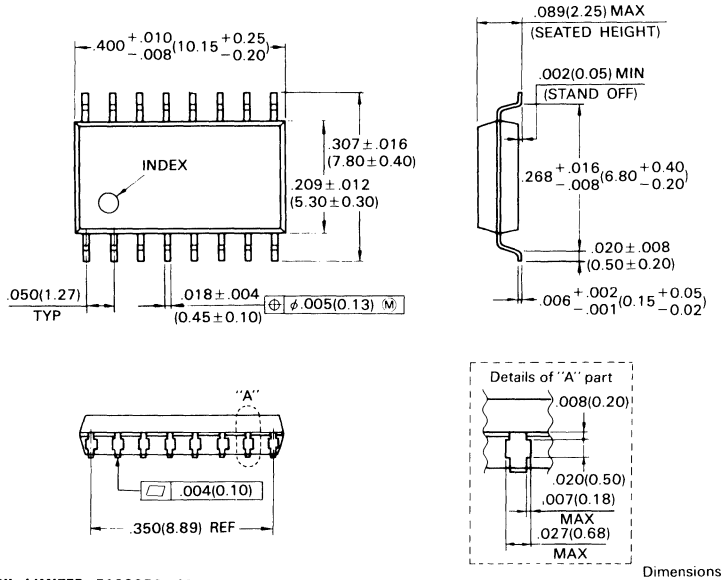


Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (continued)

16-LEAD PLASTIC FLAT PACKAGE

(Case No. : FPT-16P-M02)



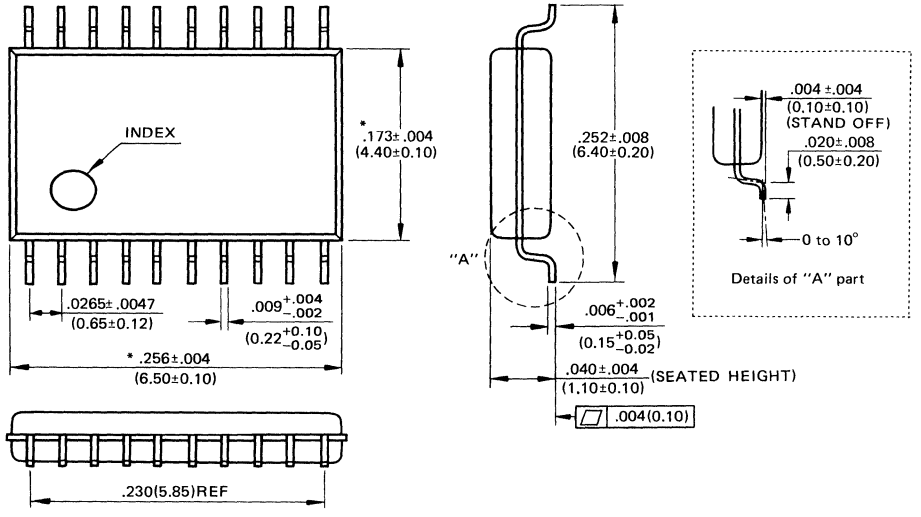
Dimensions in inches (millimeters)

4

4

PACKAGE DIMENSIONS (continued)

20 LEAD PLASTIC FLAT PACKAGE
(Case No.: FPT-20P-M04)



* This dimension does not include resin protrusion.

Dimensions in
inches (millimeters)

Section 5

Motor Drivers — *At a Glance*

Page	Device	Description	Features	Power Supply (V)	Package Options
5–3	MB3763	Motor Driver	IO = 180 mA and 330 mA	+4 to +18	8-pin Plastic DIP, SIP, FPT (with Heatsink)
5–13	MB3763H	Motor Driver	IO = 550 mA	+4 to +28	8-pin Plastic SIP (with Heatsink)
5–21	MB3854	Bidirectional Motor Driver	IO = 330 mA	+2.3 to +10	8-pin Plastic DIP, FPT

5

FUJITSU

BIDIRECTIONAL MOTOR DRIVER

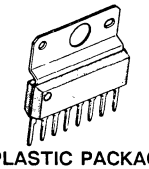
MB3763

October 1987
Edition 1.0

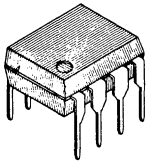
BIDIRECTIONAL MOTOR DRIVER

Fujitsu's MB3763 Motor Driver with forward/reverse control capability, is used in applications such as the front-loading mechanism in video tape, or the auto-reverse tape deck, driven by a TTL signal. The MB3763 has 300 mA drive units and braking capability with TTL control.

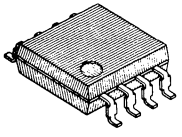
- Motor Drive Current : 300 mA maximum in a SIP Package
  : 150 mA maximum in a DIP/FPT Package
- Wide Power Supply Voltage Range : 4 V to 18 V
- TTL-control capability
- Standby capability when input is off.
- Brake capability at motor stop mode.
- Built-in diode for surge absorption
- Package : 8-pin plastic SIP package (Suffix: -PS)
  8-pin plastic DIP package (Suffix: -P)
  8-pin plastic FPT package (Suffix: -PF)



PLASTIC PACKAGE
SIP-08P-M01



PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

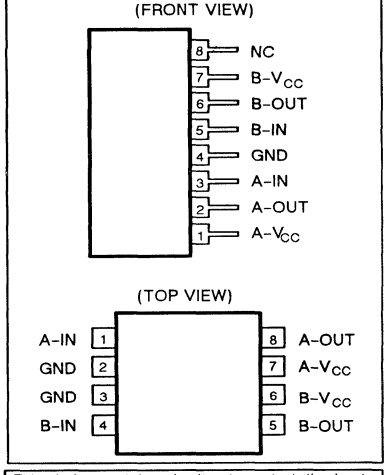
ABSOLUTE MAXIMUM RATINGS[1] (see NOTES)

Parameter	Symbol	Value		Unit
		DIP/FPT (Plastic)	SIP (Plastic)	
Power Supply Voltage	V_{CC}	20	20	V
Output Current	I_O	180 (330[2])	330	mA
Maximum Output Current	I_{OMAX} [4]	1.2	1.2	A
Power Dissipation	P_D	560[3]	1000	mW
Operating Temperature	T_C	-20 to +75	-20 to +75	°C
Storage Temperature	T_{STG}	-55 to +125	-55 to +125	°C

NOTES:

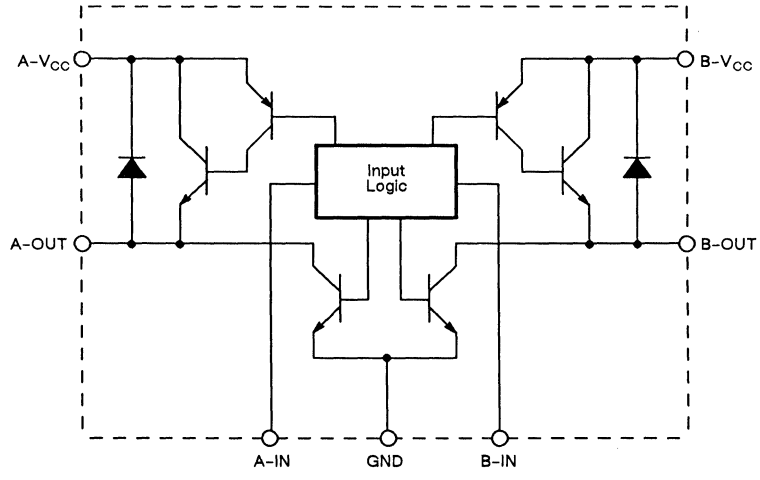
1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. $t_{ON} \leq 1$ sec, Duty = 50%
3. $T_A \leq 60°C$
4. $t \leq 5$ ms

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Figure 1. MB3763 Block Diagram



5

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		DIP/FPT (Plastic)	SIP (Plastic)	
Power Supply Voltage	V_{CC}	4 to 18	4 to 18	V
Output Current	I_O	0 to 150 (300 *1)	0 to 300	mA
Input High Voltage	V_{IH} *2	2.4 to V_{CC} + 0.3	2.4 to V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	0 to 0.4	0 to 0.4	V

NOTE: *1 $t_{ON} \leq 1$ sec, Duty = 50%

*2 When $V_{IH} \geq V_{CC}$, $I_{IH} \leq V_{CC} \times 0.2$ mA

ELECTRICAL CHARACTERISTICS FOR DIP AND FPT PACKAGE (PLASTIC) (V_{CC} = 12 V, I_O = 150 mA, T_A = 25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Standby Supply Current	I_{CC0}	V_{CC} = 18 V, V_{IA} = V_{IB} = 0 V	—	—	0.1	mA
Power Supply Current	I_{CC1}	I_O = 0 mA	—	10	20	mA
	I_{CC2}	I_O = 150 mA	—	10	—	mA
	I_{CC3}	I_O = 0 mA, V_{IA} = V_{IB} = 2.4 V	—	15	—	mA
Output High Voltage	V_{OH}	—	11.0	11.2	—	V
Output Low Voltage	V_{OL}	—	—	0.1	0.2	V
Output Saturation Voltage	V_{SAT}	—	—	0.9	1.2	V
Input Current	I_{IH}	V_{IN} = 2.4 V	—	250	400	μA
Input Switching Prohibition Time	T_{OFF}	—	10	—	—	μs

5

ELECTRICAL CHARACTERISTICS FOR SIP PACKAGE (PLASTIC) (V_{CC} = 12 V, I_O = 300 mA, T_A = 25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Standby Supply Current	I_{CC0}	V_{CC} = 18 V, V_{IA} = V_{IB} = 0 V	—	—	0.1	mA
Power Supply Current	I_{CC1}	I_O = 0 mA	—	10	20	mA
	I_{CC2}	I_O = 300 mA	—	15	—	mA
	I_{CC3}	I_O = 0 mA, V_{IA} = V_{IB} = 2.4 V	—	15	—	mA
Output High Voltage	V_{OH}	—	10.8	11.1	—	V
Output Low Voltage	V_{OL}	—	—	0.2	0.5	V
Output Saturation Voltage	V_{SAT}	—	—	1.1	1.7	V
Input Current	I_{IH}	V_{IN} = 2.4 V	—	250	400	μA
Input Switching Prohibition Time	T_{OFF}	—	10	—	—	μs

FUNCTIONAL DESCRIPTIONS

FORWARD/REVERSE MODE (MODE B & C)

In this mode, the transistor pairs Q2-Q3 and Q1-Q4 work alternatively, changing the output current direction.

When the mode B is selected, Q2 and Q3 are active and Q1 and Q4 are inactive. Therefore A-OUT is at low level and B-OUT is at high level, with the current flowing from B-OUT to A-OUT through the motor. On the other hand, when the mode C is selected, the current flows in the reverse direction.

BRAKE/STOP MODE (MODE A)

When the mode A is selected, Q1 and Q3 are inactive and Q2 and Q4 are active. A-OUT and B-OUT are stuck at low-level; terminals of motor are shorted and the motor is forced to stop.

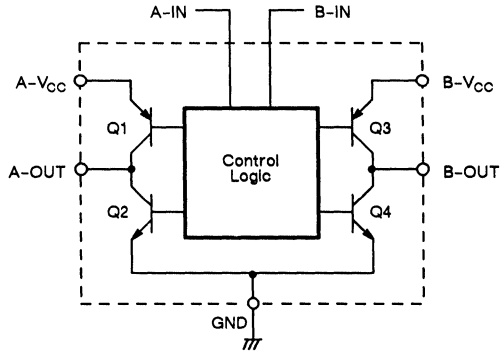
STANDBY MODE (MODE D)

In this mode, all transistors are inactive and the current through the motor does not flow. When the power supply voltage is applied to A-V_{CC} and B-V_{CC}, the supply current is still less than or equal to 0.1 mA.

5

CONTROL MODE

CONTROL BLOCK DIAGRAM

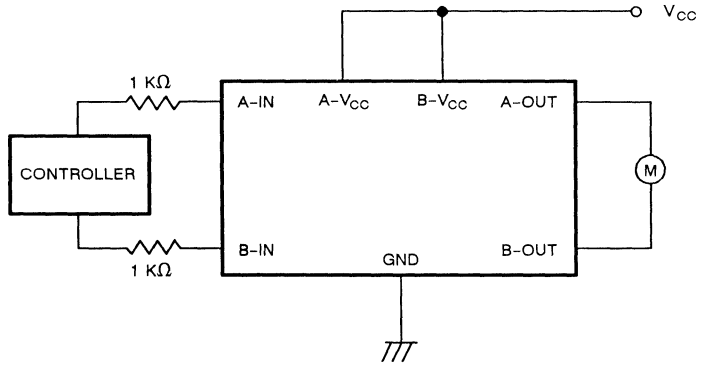


Mode	Input mode		Output mode		Operation
	A-IN	B-IN	A-OUT	B-OUT	
A	1	1	L	L	Short (Brake)
B	1	0	L	H	Forward
C	0	1	H	L	Reverse
D	0	0	-	-	Open (Standby)

NOTES: 1: ≥ 2.4 V
0: ≤ 0.4 V

TYPICAL APPLICATION

Figure 2. Typical Application Example



NOTE: In the case the control voltage is input when the power supply voltage is not applied because of the time lag between those two voltages, excess current flows into IC from the input terminals. In this case, please connect a resistor (≥ 1K Ω) serially to input pin in order to prevent excess current flow.

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 3 – Output Current vs Power Supply Current

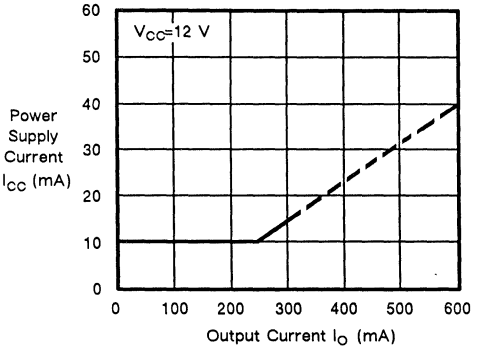
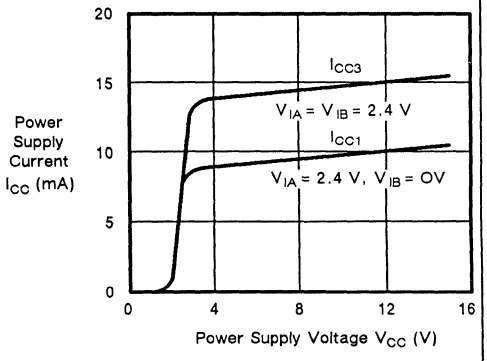


Fig. 4 – Power Supply Voltage vs Power Supply Current



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Fig. 5 – Output Current vs Output Voltage

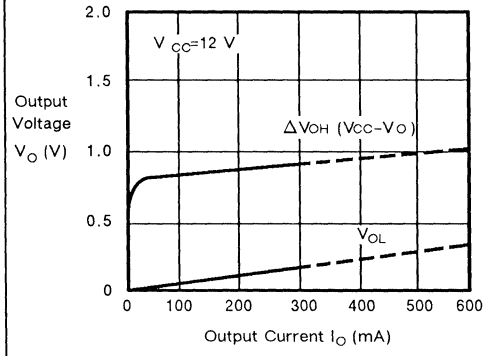


Fig. 6 – Input Voltage vs Input Current

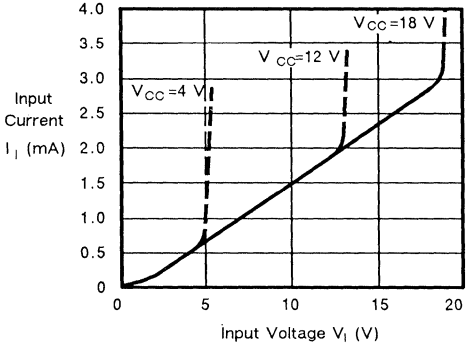
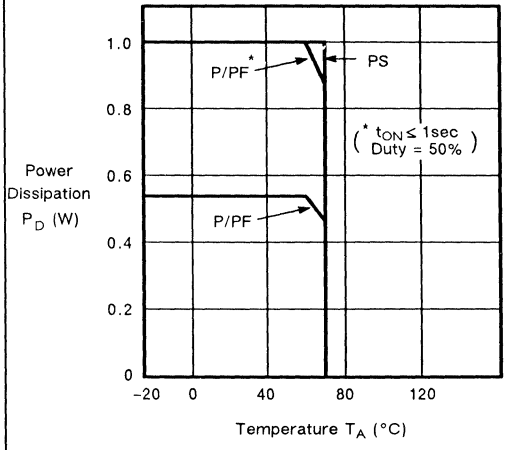


Fig. 7 – Temperature vs Power Dissipation



PF'S value is measured on the ceramic board (3.0 cm x 3.0 cm x 0.05 cm)

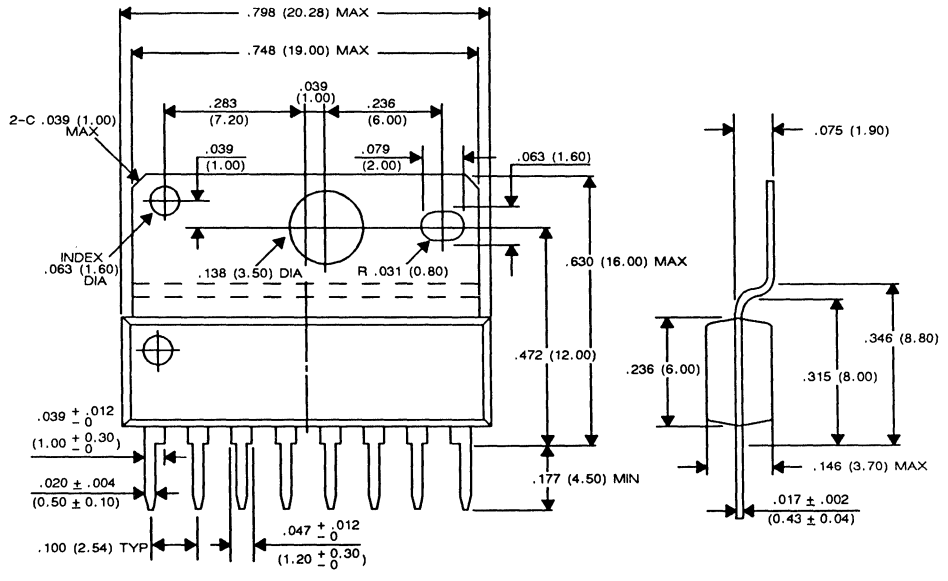
Notes P : Plastic DIP
PF : Plastic Flat Package
PS : Plastic SIP

Maximum power dissipation must be kept.

5

PACKAGE DIMENSIONS

8-LEAD PLASTIC SINGLE-IN-LINE PACKAGE
(CASE No.: SIP-08P-M01)



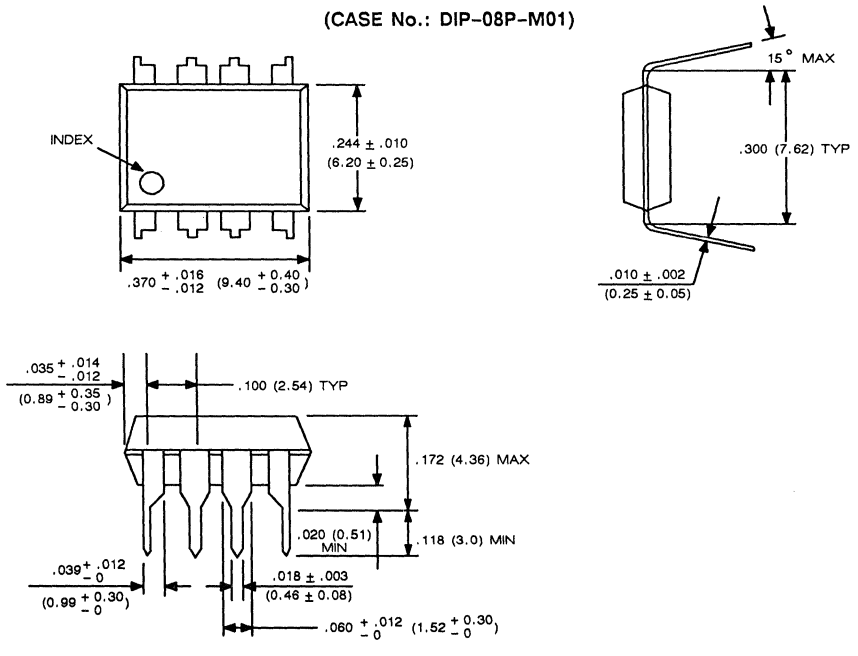
Dimensions in inches (millimeters)

S08004S-6C

5

PACKAGE DIMENSIONS (Continued)

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



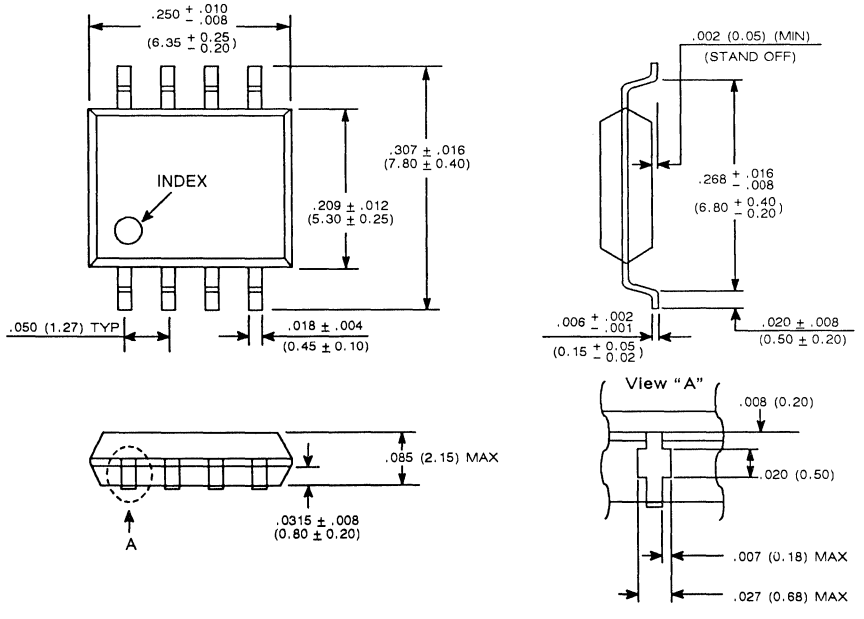
Dimensions in
inches (millimeters)

D08006S-2C

5

PACKAGE DIMENSIONS (Continued)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



Dimensions in
Inches (millimeters)

F08002S-2C

5

5

November 1989
Edition 1.0

FUJITSU

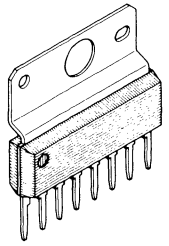
DATA SHEET

MB3763H
BIDIRECTIONAL MOTOR DRIVER

BIDIRECTIONAL MOTOR DRIVER

Fujitsu's MB3763H Motor Driver with forward/reverse control capability, is used in applications such as the front-loading mechanism in video cassette recorder or the auto-reverse tape deck, driven by a TTL signal. The MB3763H has 300mA drive units and braking capability with TTL control. The MB3736H has wider power supply voltage range comparison with MB3763 . Suitable for 24V monitors for office automation equipment

- Motor Drive Current: 300mA maximum
- Wide Power Supply Voltage Range: 4V to 28V
- TTL-control capability
- Standby capability when input is off.
- Brake capability at motor stop mode.
- Built–in diode for surge absorption.
- Package: 8-pin plastic SIP package (Suffix: -PS)

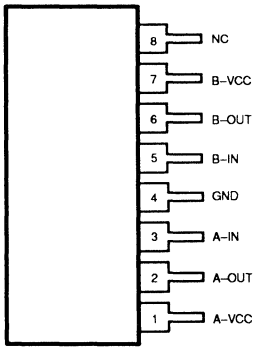


PLASTIC PACKAGE
SIP-08P-M01

5

PIN ASSIGNMENT

(FRONT VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

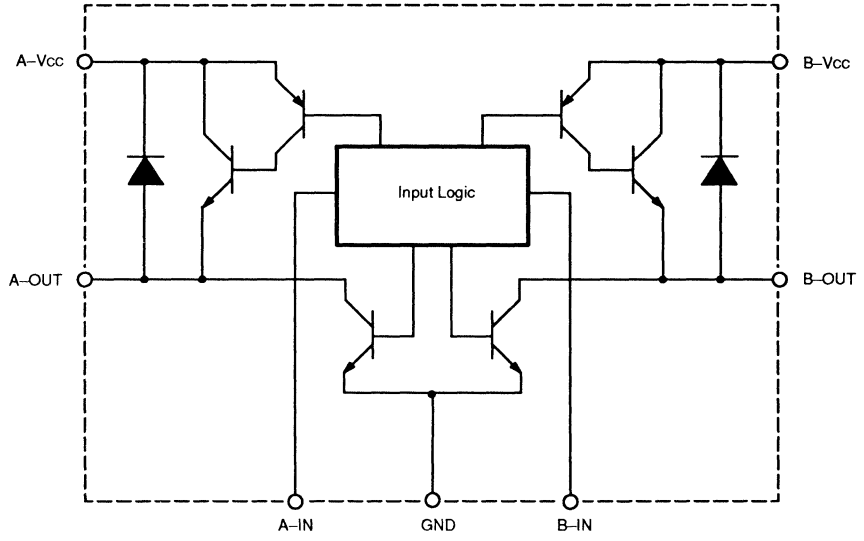
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	28	V
Output Current	I_O	550 *1	mA
Maximum Output Current	I_{OMAX} *3	1.2	A
Power Dissipation	P_D	2 *2	W
Operating Temperature	T_C	–20 to +75	°C
Strage Temperature	T_{STG}	–55 to +125	°C

Note: *1 $t_{ON} \leq 1$ sec, Duty = 50%
*2 $T_A \leq 30°C$
*3 $t \leq 5$ ms

Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 — MB3763H BLOCK DIAGRAM



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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	Vcc	4 to 28	V
Output Current	Io	0 to 300 (500 *1)	mA
Input High Voltage	VIH*2	2.4 to Vcc +0.3	V
Input Low Voltage	VIL	0 to 0.4	V

Note: *1 tON ≤ 1 sec, Duty = 50%
*2 When VIH ≥ Vcc, IIH ≤ Vcc x 0.2mA

ELECTRICAL CHARACTERISTICS

(Vcc = 24V, Io = 300mA, TA = 25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Standby Supply Current	I_{CC0}	V_{CC} = 24V, V_{IA} = V_{IB} = 0V	–	–	0.1	mA
Power Supply Current	I_{CC1}	Io = 0mA	–	12	27	mA
	I_{CC2}	Io = 300mA	–	15	–	mA
	I_{CC3}	Io = 0mA, V_{IA} = V_{IB} = 2.4V	–	18	–	mA
Output High Voltage	V_{OH}	–	22.8	23.1	–	V
Output Low Voltage	V_{OL}	–	–	0.2	0.5	V
Output Saturation Voltage	V_{SAT}	–	–	1.1	1.7	V
Input Current	I_{IH}	V_{IN} = 2.4V	–	250	400	µA
Input Switching Prohibition Time	T_{OFF}	–	10	–	–	µs

FUNCTIONAL DESCRIPTIONS

FORWARD/REVERSE MODE (MODE B & C)

In this mode, the transistor pairs Q2–Q3 and Q1–Q4 work alternatively, changing the output current direction.

When the mode B is selected, Q2 and Q3 are active and Q1 and Q4 are inactive. Therefore A–OUT is at low level and B–OUT is at high level, with the current flowing from B–OUT to A–OUT through the motor. On the other hand, when the mode C is selected, the current flows in the reverse direction.

BRAKE/STOP MODE (MODE A)

When the mode A is selected, Q1 and Q3 are inactive and Q2 and Q4 are active. A–OUT and B–OUT are stuck at low–level; terminal of motor are shorted and the motor is forced to stop.

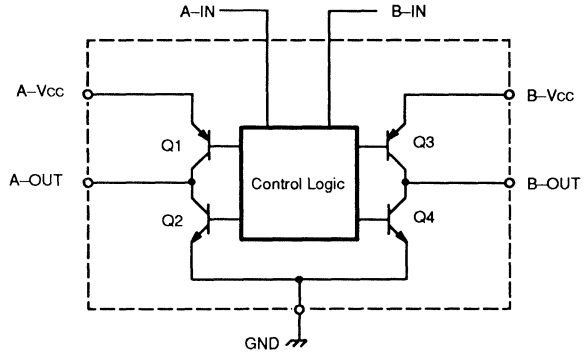
STANDBY MODE (MODE D)

In this mode, all transistors are inactive and the current through the motor does not flow. When the power supply voltage is applied to A–Vcc and B–Vcc, the supply current is still less than or equal to 0.1mA.

5

CONTROL MODE

CONTROL BLOCK DIAGRAM

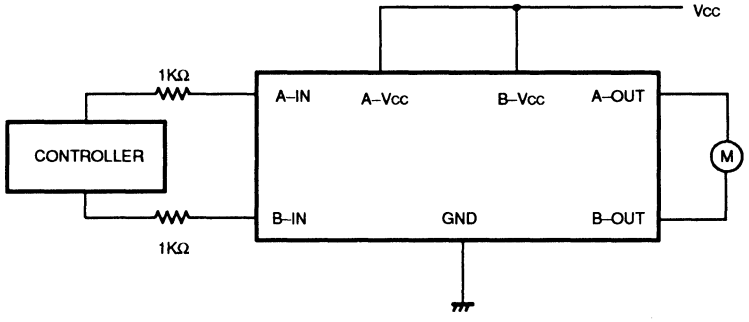


Mode	Input mode		Output mode		Operation
	A–IN	B–IN	A–OUT	B–OUT	
A	1	1	L	L	Short (Brake)
B	1	0	L	H	Forward
C	0	1	H	L	Reverse
D	0	0	–	–	Open (Standby)

Notes: 1: ≥ 2.4V
0: ≤ 0.4V

TYPICAL APPLICATION

Fig. 2 – TYPICAL APPLICATION EXAMPLE



Note: In the case the control voltage is inpupt when the power supply voltage is not applied because of the time lag between those two voltages, excess current flows into IC from the input terminals. In this case, please connect a resistor (≥ 1KΩ) serially to input pin in order to prevent excess current flow.

5

TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 3 – OUTPUT CURRENT vs. POWER SUPPLY CURRENT

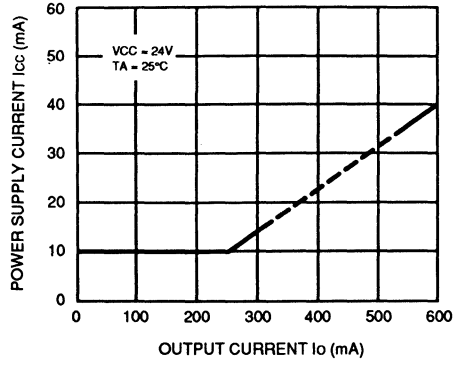
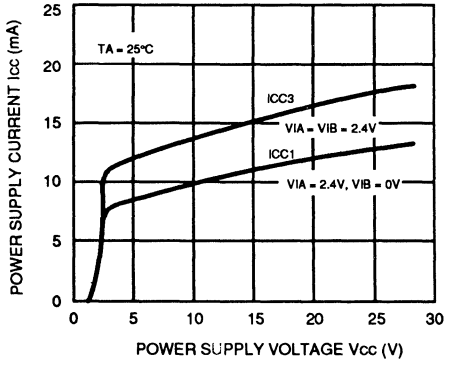


Fig. 4 – POWER SUPPLY VOLTAGE vs. POWER SUPPLY CURRENT



TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

5

Fig. 5 – OUTPUT CURRENT vs.OUTPUT VOLTAGE

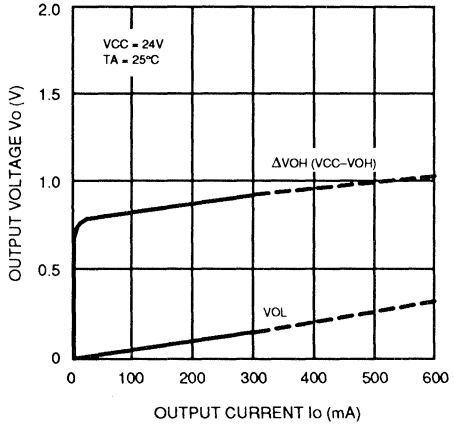


Fig. 6 – INPUT VOLTAGE vs.INPUT CURRENT

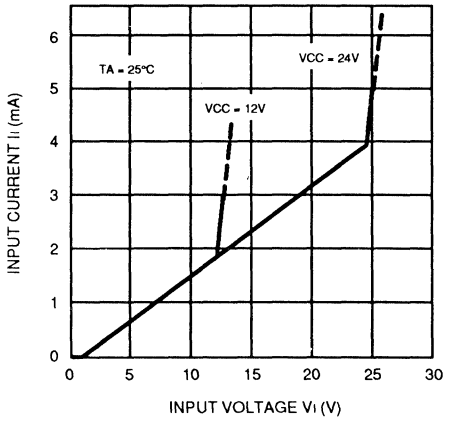
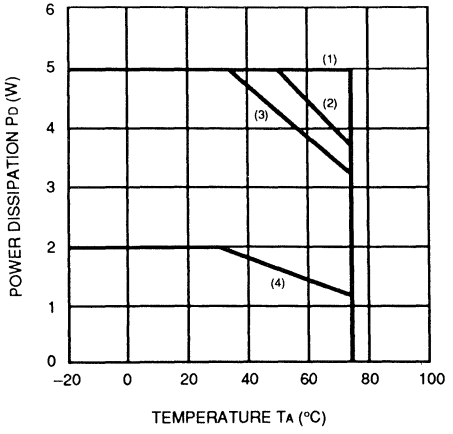


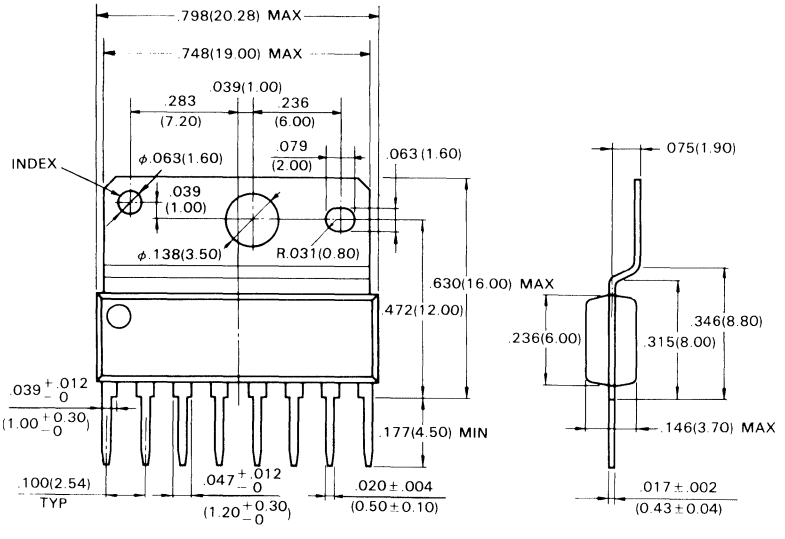
Fig. 7 – TEMPERATURE vs. POWER DISSIPATION



(1) Infinity Heat Board
(2) 100cm² x 2mm Al Board
(3) 50cm² x 2mm Al Board
(4) Free Air

PACKAGE DIMENSIONS

8-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(CASE No.: SIP-08P-M01)



Dimensions in
inches (millimeters)

5

FUJITSU

BI-DIRECTIONAL MOTOR DRIVER

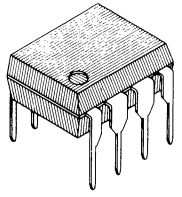
MB3854

April 1988
Edition 1.0

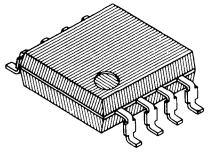
BI-DIRECTIONAL MOTOR DRIVER

The Fujitsu MB3854 is a low voltage motor driver with forward/reverse control capability for motor in auto focus, film advancing mechanism, in camera, in front loading mechanism in CD player, etc., which is driven by TTL-level signal.
The MB3854 has 300mA drive units and brake capability for stop with TTL control input.

- Motor drive current: 300mA max.
- Low power supply voltage operation: 2.3V to 10V
- TTL-control capability
- Standby capability when input is off
- Brake capability at motor stop mode
- Built-in diode for surge absorption
- Plastic 8-pin Dual-In-Line Package (Suffix: -P)
- Plastic 8-pin Flat Package (Suffix: -PF)

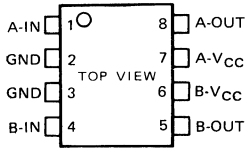


PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	12	V
Output Current	I_O	330 (550*1)	mA
Maximum Output Current	I_{OMAX} *2	0.8	A
Power Dissipation	P_D	560*3	mW
Operating Temperature	T_A	−20 to +75	°C
Storage Temperature	T_{STG}	−55 to +125	°C

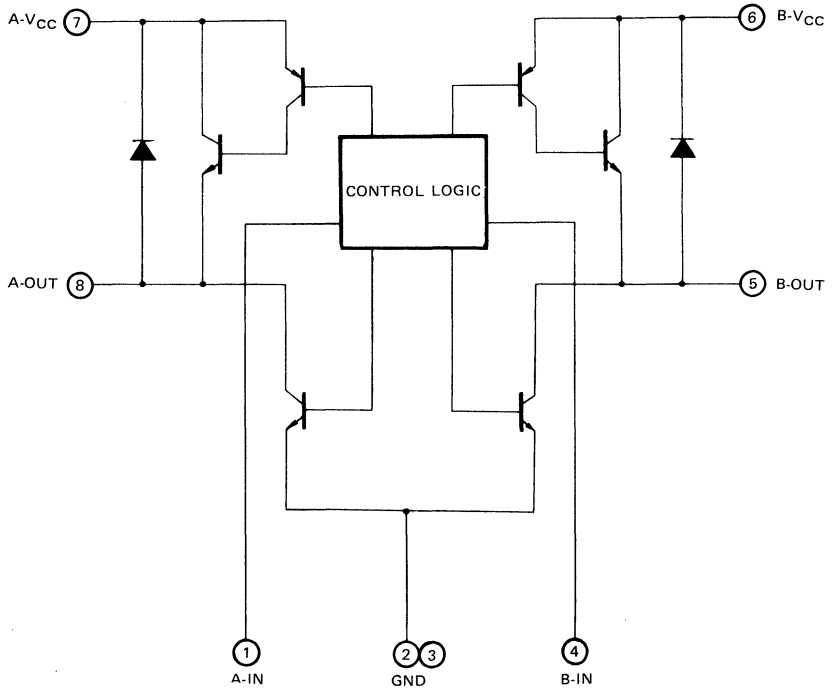
*1 $t_{ON} \leq 1$ sec, Duty = 50%
*2 $t \leq 5$ms
*3 $T_A \leq 60°C$

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

5

Fig. 1 – MB3854 BLOCK DIAGRAM



5

FUNCTIONAL DESCRIPTIONS

According to the control mode, output transistors in Fig. 2 work as follows.

FORWARD/REVERSE MODE

According to the control B/C mode, the transistor pairs Q2-Q3 and Q1-Q4 work alternatively and supply current to motor is changed.

When the mode B is selected, Q2 and Q3 are active. A-OUT is at low level and B-OUT is at high level, current flows from B-OUT to A-OUT through the motor.

On the other hand, when the mode C is selected, the current flows in reverse direction.

BRAKE MODE

When control mode A is selected, Q1 and Q3 are inactive, Q2 and Q4 are active. A-OUT and B-OUT are clamped at low level, terminals of the motor are shorted and the motor is forced to stop.

STAND-BY MODE

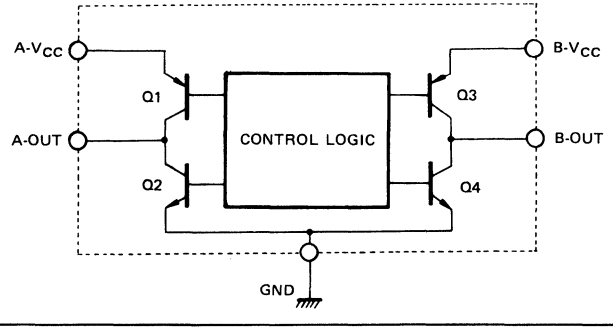
When stand-by mode is selected, all transistors are inactive and the current through motor does not flow. In this case, the supply current is less than 100μA.

Table 1 – CONTROL MODE TABLE

Mode	Input mode		Output level		Operation mode
	A-IN	B-IN	A-OUT	B-OUT	
A	1	1	L	L	Short (Brake)
B	1	0	L	H	Forward
C	0	1	H	L	Reverse
D	0	0	–	–	Open (Stand-by)

Note:
Input mode
1: $\geq$ 2.1V
2: $\leq$ 0.4V

Fig. 2



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	2.3 to 10	V
Output Current	I_O	0 to 300 (500*1)	mA
Input High Voltage	V_{IH}	2.1 to V_{CC}+0.3*2	V
Input Low Voltage	V_{IL}	0 to 0.4	V

Note: *1 $t_{ON} \leq 1$ sec, Duty = 50%
*2 When $V_{IH} \geq V_{CC}$, $I_{IH} \leq V_{CC} \times 0.2$mA

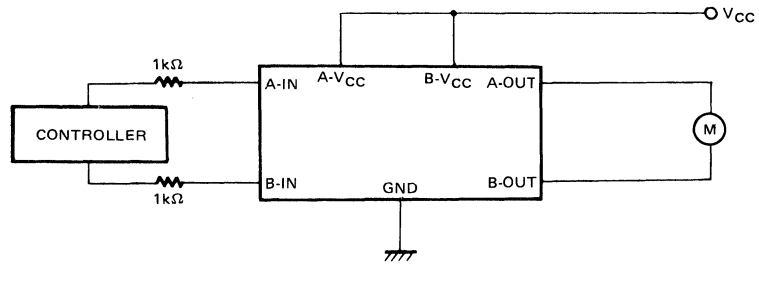
ELECTRICAL CHARACTERISTICS

(V_{CC} = 3V, V_{IH} = 2.4V, I_O = 300mA, T_A = 25°C)

5

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Stand-by Current	I_{CC0}	V_{CC} = 6V, V_{IA} = V_{IB} = 0V			100	μA
Power Supply Current	I_{CC1}	I_O = 0mA		4.5	8	mA
	I_{CC2}	I_O = 300mA		24		mA
	I_{CC3}	I_O = 0mA, V_{IA} = V_{IB} = 2.4V		7		mA
Output High Voltage	V_{OH}		1.85	2.1		V
Output Low Voltage	V_{OL}			0.25	0.35	V
Output Saturation Voltage	V_{SAT}			1.15	1.5	V
Input Current	I_{IH}	V_{IN} = 2.4V		250	400	μA

Fig. 3 – APPLICATION EXAMPLE



Note: In the case the control voltage is input when the power supply voltage is not applied because of the time lag between those two voltages, excess current flows into IC from the input terminals.
In this case, please connect a resistor (≥1kΩ) serially to input pin in order to prevent excess current flow.

TYPICAL CHARACTERISTICS CURVES (T_A = 25°C)

Fig. 4 – POWER SUPPLY VOLTAGE vs. POWER SUPPLY CURRENT

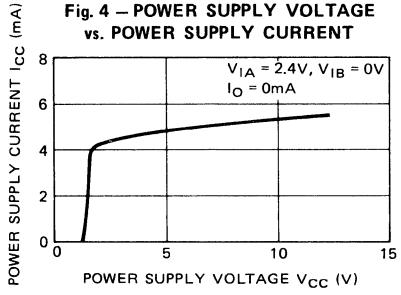


Fig. 5 – POWER SUPPLY VOLTAGE vs. POWER SUPPLY CURRENT (BRAKE MODE)

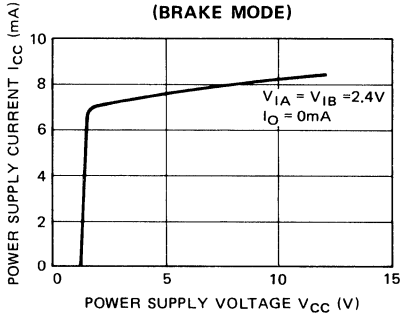


Fig. 6 – OUTPUT CURRENT vs. OUTPUT VOLTAGE

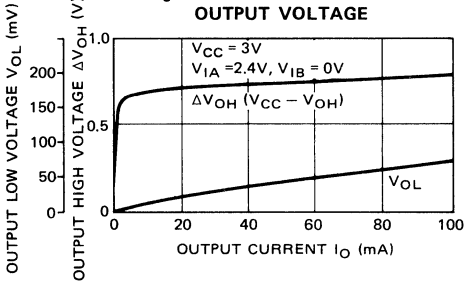
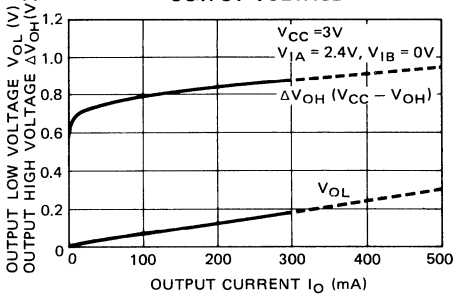


Fig. 7 – OUTPUT CURRENT vs. OUTPUT VOLTAGE



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TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 8 – OUTPUT CURRENT vs. POWER SUPPLY CURRENT

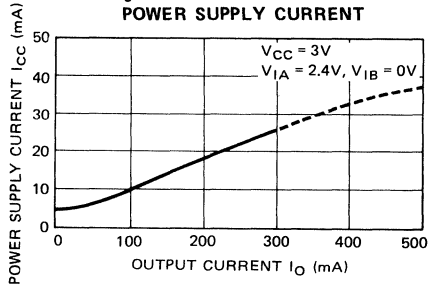


Fig. 9 – INPUT VOLTAGE vs. INPUT CURRENT

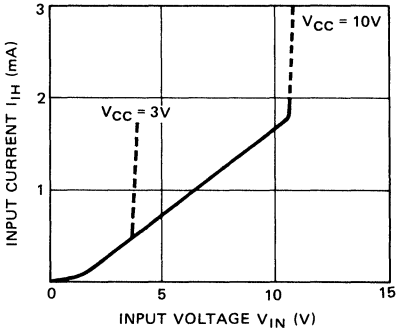
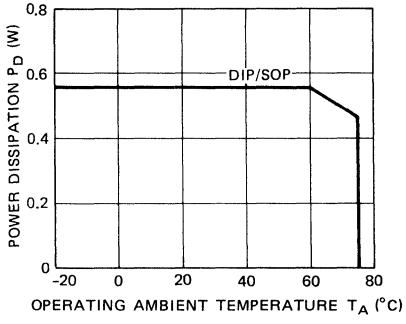


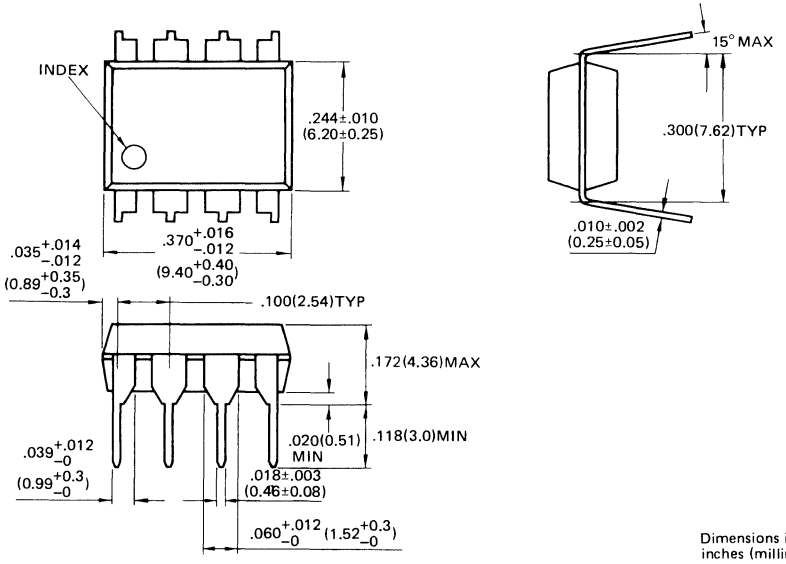
Fig. 10 – POWER DERATING CURVE



Notes: FPT package is mounted on the ceramic board (3.0cm x 3.0cm x 0.05cm).
Maximum power dissipation must be kept.

PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)

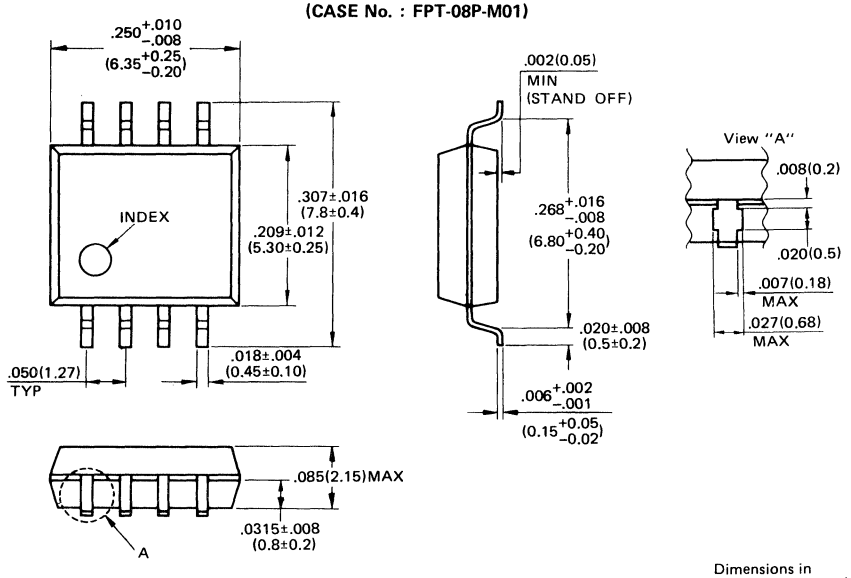


Dimensions in
inches (millimeters)

5

PACKAGE DIMENSIONS (continued)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-08P-M01)



Dimensions in
inches (millimeters)

5

Disk Drivers — *At a Glance*

Page	Device	Description	Features	Power Supply (V)	Package Options
6–3	MB4107A	Floppy Disk VFO Separator GAP and Mark Detector	VFO with PLL Data	+4.75 to +5.25	24-pin Plastic DIP, FPT
6–19	MB4108A	Floppy Disk VFO Separator GAP and Mark Detector	VFO with PLL Data	+4.75 to +5.25	24-pin Plastic DIP, FPT
6–31	MB4111 MB4113	Head 4-Ch R/W Amp Driver/Receiver	AV = 35 V/V Moving Head Read/Write	+5.7 to 6.3	24-pin Ceramic FPT
6–41	MB4114A	Head 4-Ch Amp for HDD	AV = 190 V/V	Dual: +5, +12	24-pin Ceramic FPT
6–57	MB4115 4116 4125 4126	Head 8-Ch Amp for HDD	AV = 120 V/V Damping Resistor	Dual: +5, +12	34-pin Plastic FPT
6–73	MB4117-4 4118-4	Head 4-Ch R/W Amp	AV = 110 V/V Damping Resistors	Dual +12, +5	22-pin Plastic DIP 24-pin Plastic FPT 24-pin Ceramic FPT
6–73	MB4117-6 4118-6	Head 6-Ch R/W Amp	AV = 110 V/V Damping Resistors	+12, +5	28-pin Plastic DIP 28-pin Ceramic FPT
6–85	MB4313	Driver/Receiver	Read/Write Interface	–5.2	16-pin Ceramic DIP
6–91	MB4316	Driver/Receiver for Disk Head Amp	With Write Current Source	–5.2 to –12	16-pin Ceramic DIP
6–99	MB4319	Head Positions Controller	Head Control	+15 to 15	16-pin Ceramic DIP

6

FUJITSU

FLOPPY DISK VFO

MB4107A

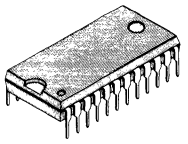
February 1989
Edition 2.0

FLOPPY DISK VFO

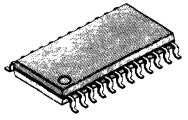
The Fujitsu MB4107A is a variable-frequency oscillator (VFO) IC for use in floppy-disk interfaces. It provides a complete data separation function, with a minimum of external parts and no adjustments, and can be used with a variety of disk controllers. It locks onto the read signal from the disk drive, which normally has jitter due to rotation speed variations and peak shifting, and produces a stable read signal for the controller. It also produces a window signal, which can be used to differentiate the clock and data pulses in the read signal.

The MB4107A includes functions for sync field detection, automatic loop filter gain switching, and address and index mark detection.

- The analog VFO (PLL) circuitry allows a wide read margin for the data separator.
- Can be connected to 8-inch ,5-inch and 3.5-inch floppy disk drives using the same external components.
- Handless both double-density (MFM) and single-density (FM) disks.
- Can be used with various floppy disk controllers such as the MB8876A, MB8877A, FD1791, and μPD 765.
- The discrimination function for gap and sync fields prevents incorrect locking on the gap field.
- The quick sync function (high gain) in the sync field is automatically switched to the stable tracking function (low gain).
- Because the sync pattern detector (data: 00_H, clock: FF_H) and the IBM format mark detector control PLL gain, the index, ID, and data fields can be locked onto without special control signals.
- A master clock is generated for the floppy disk controller, to prevent spikes when switching between each kind of floppy disks.
- External circuitry requires very few components, and no adjustments.
- Internal clock: 7 resistors, 5 capacitor, 1 crystal or ceramic resonator
  External clock: 5 resistors, 3 capacitors

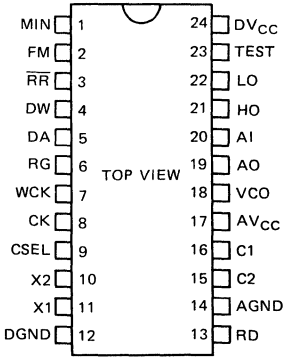


PLASTIC PACKAGE
DIP-24P-M02



PLASTIC PACKAGE
FPT-24P-M02

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Item	Symbol	Condition	Rating	Unit
Supply Voltage	V_{CC}		7	V
Logic Input Voltage	V_{IN}		7	V
Power Dissipation	P_D	$T \leqq 75°C$	550	mW
Storage Temperature	T_{STG}		-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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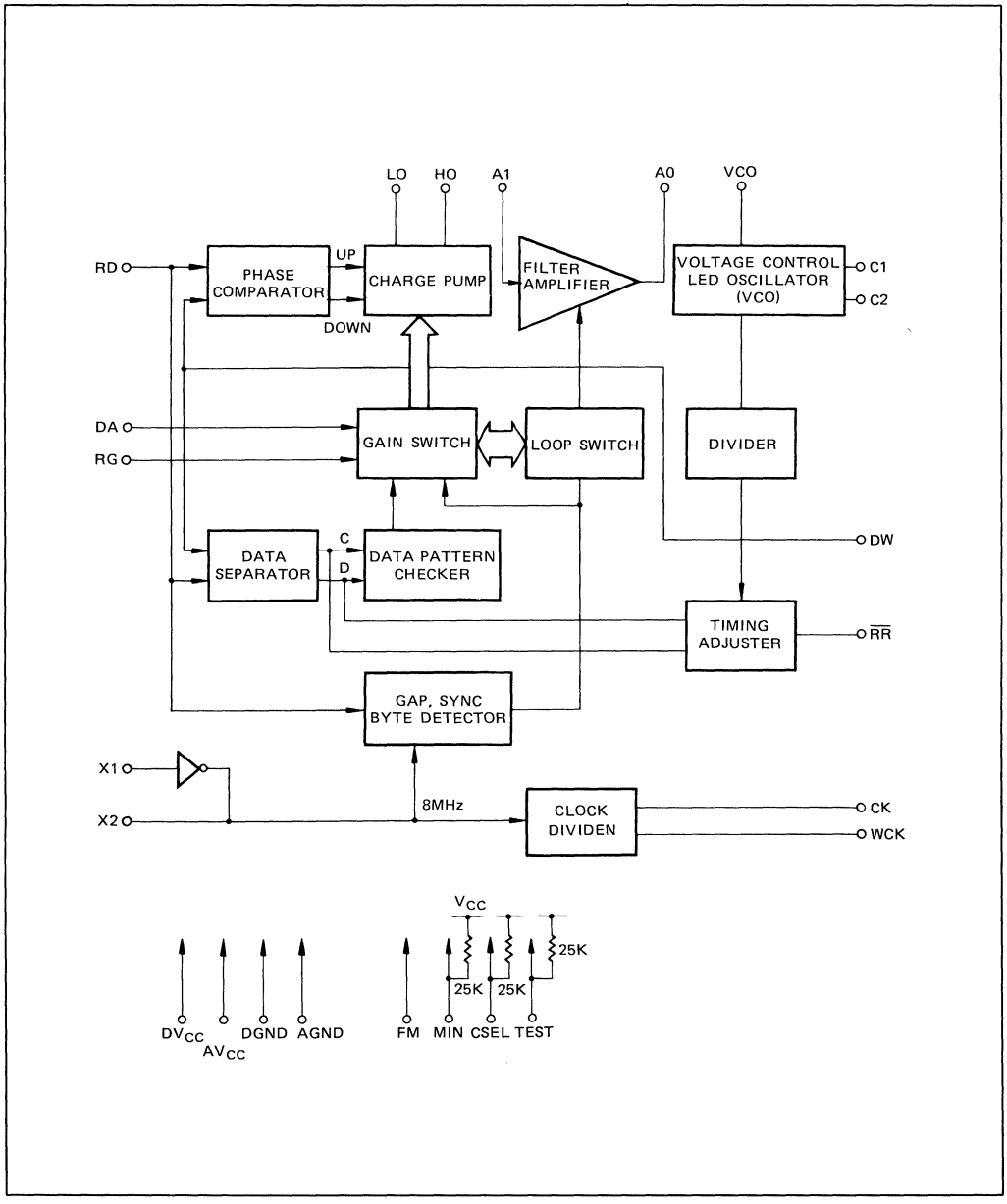

LO
HO
A1
A0
VCO
RD
PHASE COMPARATOR
UP
DOWN
CHARGE PUMP
FILTER AMPLIFIER
VOLTAGE CONTROL LED OSCILLATOR (VCO)
C1
C2
DA
RG
GAIN SWITCH
LOOP SWITCH
DIVIDER
DATA SEPARATOR
C
D
DATA PATTERN CHECKER
DW
TIMING ADJUSTER
RR
GAP, SYNC BYTE DETECTOR
X1
X2
8MHz
CLOCK DIVIDEN
CK
WCK
VCC
25K
25K
25K
DVCC
AVCC
DGND
AGND
FM
MIN
CSEL
TEST

PIN DESCRIPTION

Pin No.	Pin Name	Descriptions
1	MIN	Selects type of floppy disk as follows: – 8-inch floppy disk (STD) Low – 5-inch, 3.5-inch floppy disk 2D, 2DD (MIN) High 2HD, 2ED (3.5-inch 2MB) (STD) Low
2	FM	Selects the disk density as follows: – Single density (FM system) High – Double density (MFM system) Low
3	$\overline{RR}$	Read data signal for the FDC, including both clock and data pulses.
4	DW	Data window signal for separating the $\overline{RR}$ signal into data and clock pulses.
5	DA	Input for indicating a data field. When DA goes high, the PLL is kept as a low gain. Either RG or DA is used, but not both, and the unused pin is kept low.
6	RG	Read Gate (MB 8877A system) or VCO Sync (μPD765 system) input. When a high signal is applied to this pin, PLL is kept at a low gain.
7	WCK	The μPD 765 system FDC write clock pulse is output from this pin as follow: – STD 8-inch/MFM T = 1 μs – STD 8-inch/FM T = 2 μs – MIN 5-inch/MFM T = 2 μs – MIN 5-inch/FM T = 4 μs
8	CK	The FDC clock pulse is output from this pin as follows: – MB 8877A system/STD 8-inch 2 MHz – MB 8877A system/MIN 5-inch 1 MHz – μPD 765 system/STD 8-inch 8 MHz – μPD 765 system/MIN 5-inch 4 MHz
9	CSEL	Selects the FDC type shown below (an internal pull-up resistor is provided): – MB 8877A, FD 1791 system High – μPD 765 system Low
10	X2	(1) Inverter output for the quartz oscillator (2) This pin is open when a 8-MHz external clock is used.
11	X1	(1) Inverter input for the quartz oscillator (2) Input pin when an 8-MHz external clock is used.
12	DGND	Ground for digital circuits
13	RD	Input for the source read data from the FDD
14	AGND	Ground for analog circuits such as VCO and filter amplifier
15 16	C1 C2	An external capacitor for setting VCO oscillating frequency is connected to these pins.

PIN DESCRIPTION (continued)

Pin No.	Pin Name	Descriptions
17	AV_{CC}	Power supply for analog circuits such as the VCO and filter amplifier.
18	VCO	VCO control current input.
19	AO	Output pin for the low pass filter (LPF) amplifier in the VFO (PLL) circuit.
20	AI	Input pin for the LPF amplifier in the VFO (PLL) circuit
21	HO	Output pin to be externally connected to the LPF amplifier. This pin is selected at frequency lock after a sync field is detected. A high signal decreases the VCO frequency and a low signal increases it. (High gain)
22	LO	Output pin to be externally connected to the LPF amplifier. This pin is selected after frequency lock, for phase synchronization. A high signal delays the VCO phase, and a low signal advances it. (Low gain)
23	TEST	Used for the LSI function test. It is normally open or pulled up.
24	DV_{CC}	Power supply pin for digital circuits.

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Operating temperature range	T_{OP}	−20	25	75	°C

ELECTRICAL CHARACTERISTICS

1 — DC CHARACTERISTICS

Item	Symbol	Condition		Value Min	Value Typ	Value Max	Unit	Applicable pin	Note
Supply current	I_{CC}	V_{CC} = 5.25 V		–	70	100	mA	V_{CC}	*4
High level input voltage	V_{IH}	V_{CC} = 4.75 to 5.25V		2.0	–	–	V	MIN, FM DA, RG CS, X1 RD	*3
Low level input voltage	V_{IL}			–	–	0.8	V		*3
High level input current	I_{IH}	V_{CC} = 5.25 V, V_I = 2.7 V		–	–	20	μA	FM, DA RG, X1 RD	–
Current at maximum input voltage	I_I	V_{CC} = 5.25 V, V_I = 7.0 V		–	–	0.1	mA		–
Low level input current	I_{IL}	V_{CC} = 5.25 V, V_I = 0.4 V		-400	-20	–	μA		–
Open-circuit input voltage	V_{IP}			4.85	5.0	–	V	MIN, CS	–
Low level input current	I_{ILP}	V_I = 0 V		-1.1	-0.6	–	mA		–
High level output voltage 1	V_{OH1}	V_{CC} = 4.75 V, I_{OH} = -1.2 mA		2.7	3.3	–	V	$\overline{RR}$, DW	*1 *3
Low level output voltage 1	V_{OL1}	V_{CC} = 4.75 V	I_{OL} = 12 mA	–	0.28	0.4	V		*2 *3
			I_{OL} = 24 mA	–	0.35	0.5	V		
Short-circuit output current 1	I_{OS1}	V_{CC} = 5.25 V		-30	–	-160	mA		*1 *3
High level output voltage 2	V_{OH2}	V_{CC} = 4.75 V, I_{OH} = -0.4 mA		2.7	3.3	–	V	WCK, CK	*1 *3
Low level output voltage 2	V_{OL2}	V_{CC} = 4.75 V	I_{OL} = 4 mA	–	0.28	0.4	V		*2 *3
			I_{OL} = 8 mA	–	0.35	0.5	V		
Short-circuit output current 2	I_{OS2}	V_{CC} = 5.25 V		-20	–	-110	mA		*1 *3
High level output voltage 3	V_{OH3}	V_{CC} = 4.75 V, I_{OH} = -0.4 mA		2.7′	3.3	–	V	X2	*1 *3
Low level output voltage 3	V_{OL3}	V_{CC} = 4.75 V, I_{OL} = 1 mA		–	0.28	0.4	V		*2 *3
High output voltage	V_{HH}	I_{OH} = -1 mA		3.3	3.7	–	V	HO	*1
Low output voltage	V_{LH}	I_{OL} = 1 mA		–	2.0	2.4	V		*2
High output voltage	V_{HL}	I_{OH} = -0.2 mA		3.8	4.2	–	V	LO	*1
Low output voltage	V_{LL}	I_{OL} = 0.2 mA		–	1.5	1.9	V		*2
VCO free run frequency	f_{FR}			1.6	2.0	2.4	MHz		–

NOTE: *1 The output stage is set high. *2 The output stage is set low. *3 T_A = -20°C to 75°C

*4 V_{CC} is connected with A, V_{CC} & D, V_{CC}.

6

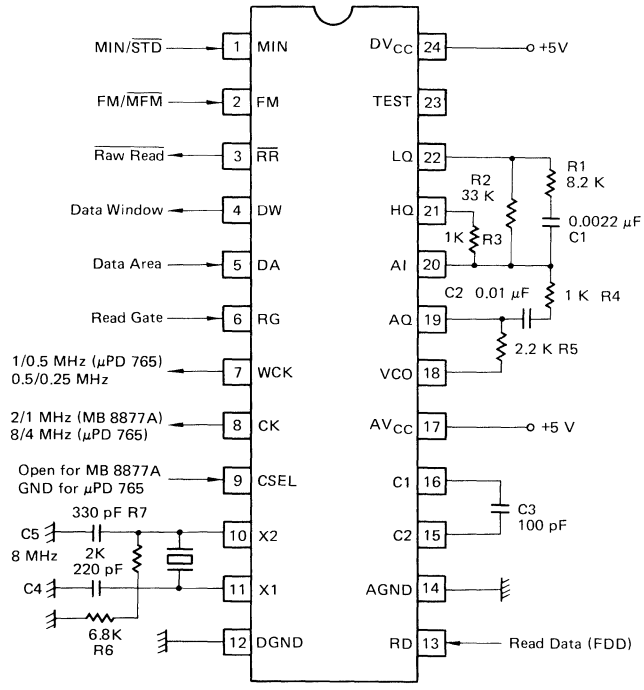
2 – AC CHARACTERISTICS

(V_{CC} = 5V, f_{X1} = 8MHz)

Item	Symbol	Condition		Value Min	Value Typ	Value Max	Unit	Applicable Pin
Rising Time	T_r	C_L = 25pF			3		ns	CK
Falling Time	T_f				2			
Frequency	f_{CK}	CSEL = "H" MB8876A	MIN = "L"		2		MHz	
			MIN = "H"		1			
		CSEL = "L" μPD765	MIN = "L"		8			
			MIN = "H"		4			
Duty Ratio	DR_{CK}	CSEL = "H"	C_L = 25pF		50		%	
		CSEL = "L"			50			
Rising Time	T_r	C_L = 25pF			3		ns	WCK
Falling Time	T_f				2			
Cycle Time	T_{CY}	MIN = "L"	MFM = "H"		1		μs	
			MFM = "L"		2			
		MIN = "H"	MFM = "H"		2			
			MFM = "L"		4			
"H" Level Width	T_{WH}	MIN = "L"	MFM = "H"		125		ns	
			MFM = "L"		125			
		MIN = "H"	MFM = "H"		250			
			MFM = "L"		250			
Rising Time	T_r	C_L = 25pF			3			DW
Falling Time	T_f				2			
Window Width ("H" Level Width)	T_W	MIN = "L"	MFM = "H"		1		μs	
			MFM = "L"		2			
		MIN = "H"	MFM = "H"		2			
			MFM = "L"		4			
Rising Time	T_r	C_L = 25pF			3		ns	$\overline{RR}$
Falling Time	T_f				2			
"L" Level Width	T_{WL}	MIN = "L"	MFM = "H"		0.25		μs	
			MFM = "L"		0.5			
		MIN = "H"	MFM = "H"		0.5			
			MFM = "L"		1			
Slip Off from DW Center	T_D				10		ns	
"H" Level Width	T_{WH}			50				RD
External Clock Duty Ratio	D_{EXT}	f_{X1} = 8MHz/9.6MHz		40	50	60	%	X1

6

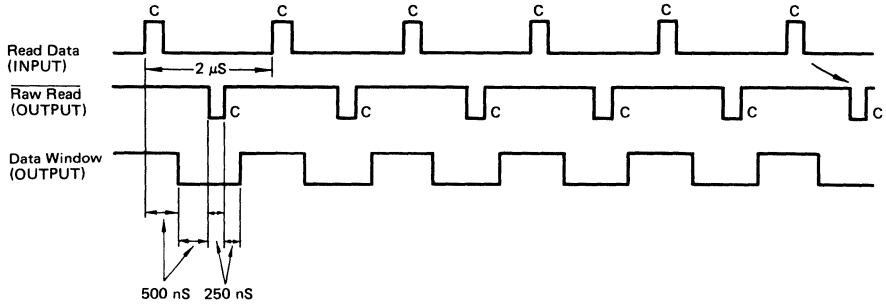
STANDARD EXTERNAL CIRCUITS (MB4107A)



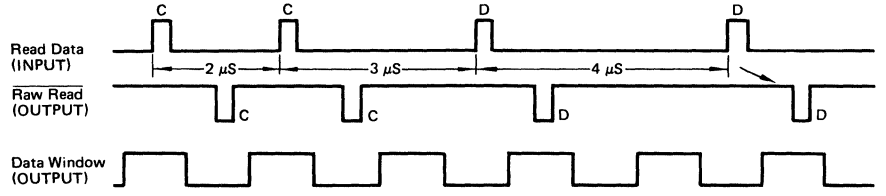
NOTE: 1. C_3 (±5%), R_5 (±1%), otherwise C (±10%), R (±5%)
2. Since the 8-MHz internal and 8-MHz external clocks require precision of ±1%, a ceramic resonator can be used when WCK and CK do not require a high precision.

TIMING CHARTS

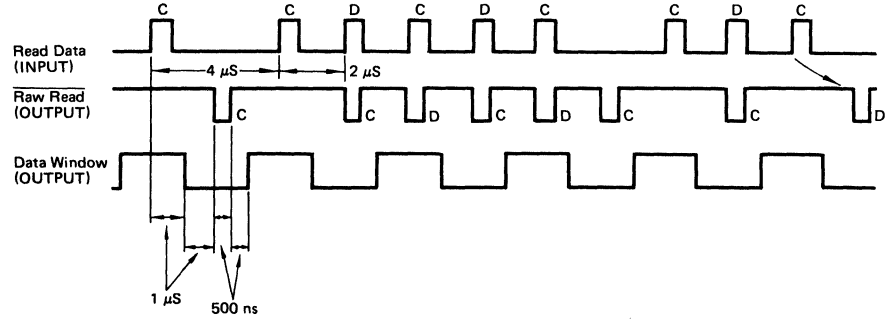
I 8 INCH, MFM, HIGH GAIN (SYNC FIELD)



II 8 INCH, MFM, LOW GAIN



III 8 INCH, FM, LOW GAIN.

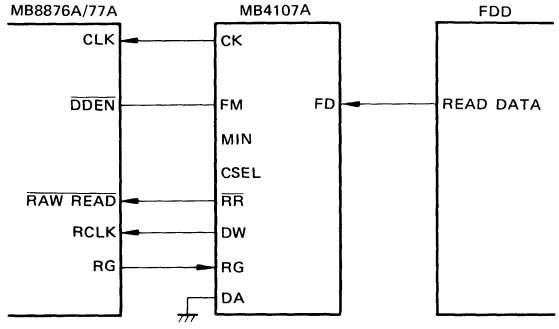


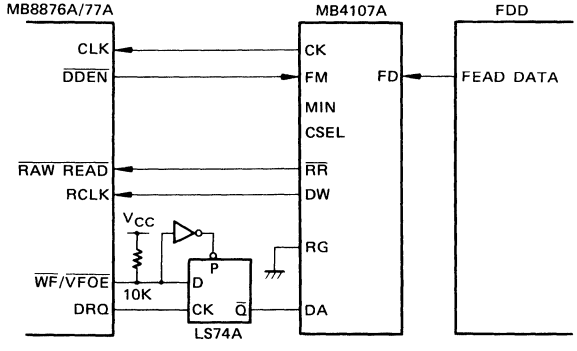
NOTES: 1. The above times are doubled for 5-inch floppy disks.
2. C = clock pulse, D = data pulse

STANDARD CONNECTION

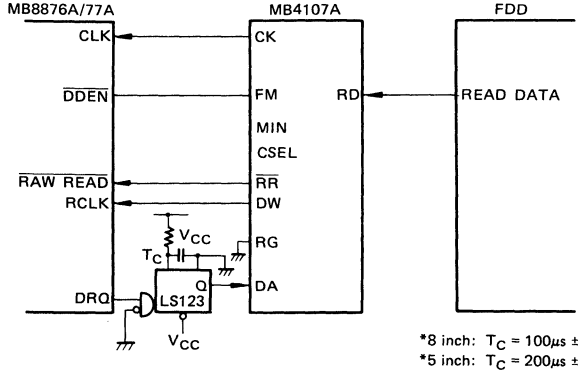
1. MB8876/77A

1-1) Read Gate





1-2) Data Request



*8 inch: $T_C = 100\mu s \pm 20\%$
*5 inch: $T_C = 200\mu s \pm 20\%$

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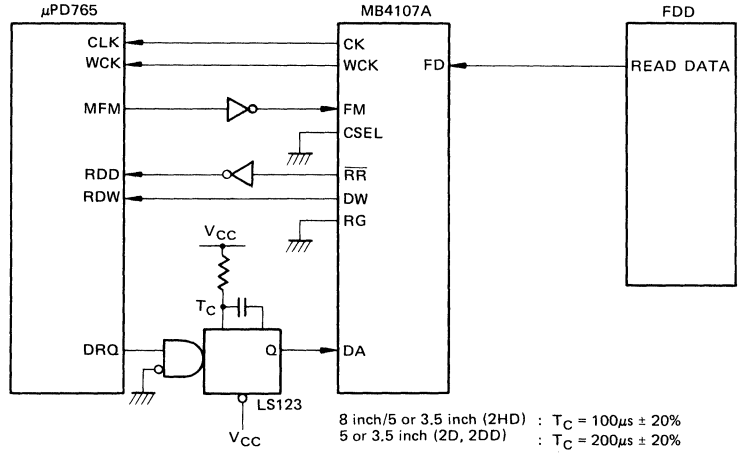
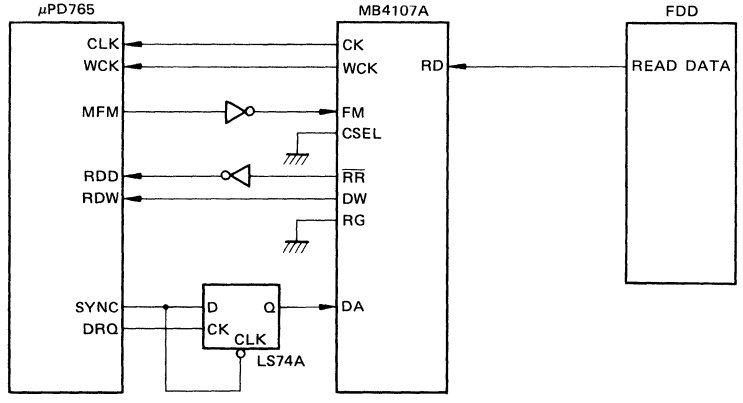
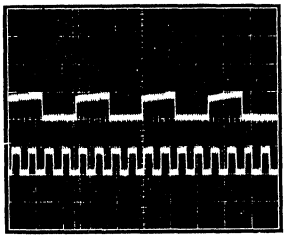
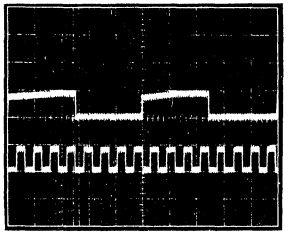
STANDARD CONNECTIONS (continued)

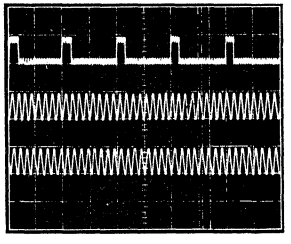
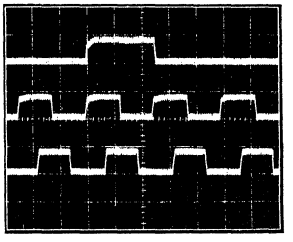
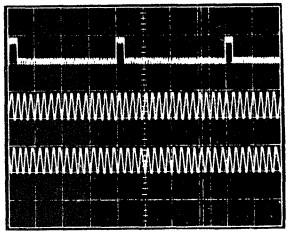
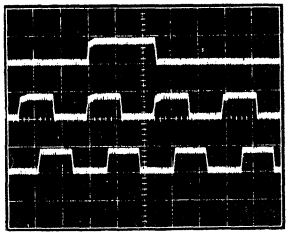
2. μPD765





CK, WCK TIMING (EXTERNAL CLOCK INPUT)

Mode	In/Output	Timing
CSEL = "H" MB8876A MB8877A STD MFM/FM	CK X1	
CSEL = "H" MB8876A MB8877A MIN MFM/FM	CK X1	

Mode	In/Output	Timing	Magnification
CSEL = "L" (μPD765) STD MFM	WCK CK X1		
CSEL = "L" (μPD765) STD FM	WCK CK X1		

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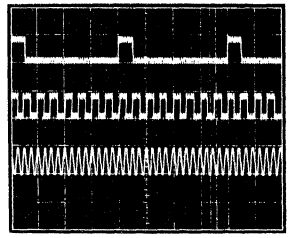
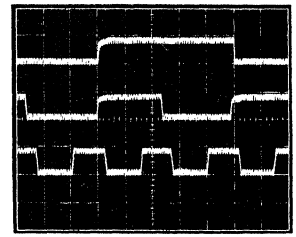
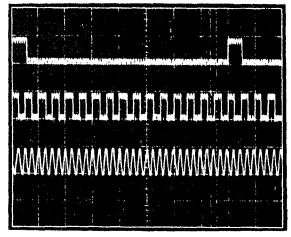
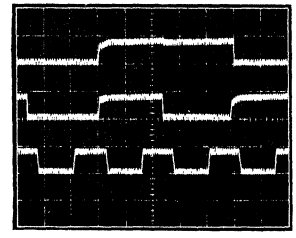
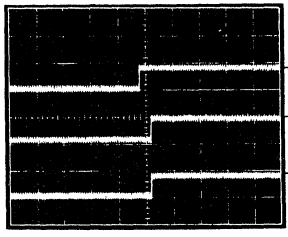
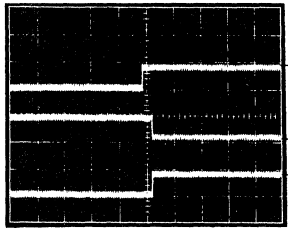
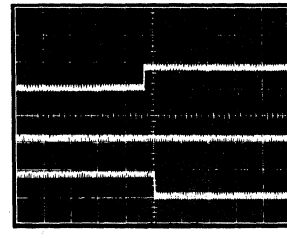
CK, WCK TIMING (EXTERNAL CLOCK INPUT) (continued)

Mode	In/Output	Timing	Magnification
CSEL = "L" (μPD765) MIN MFM	WCK CK X1		
CSEL = "L" (μPD765) MIN FM	WCK CK X1		

Delay of CW, WCK against input clock







TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1 – f_{V10} vs. VAD

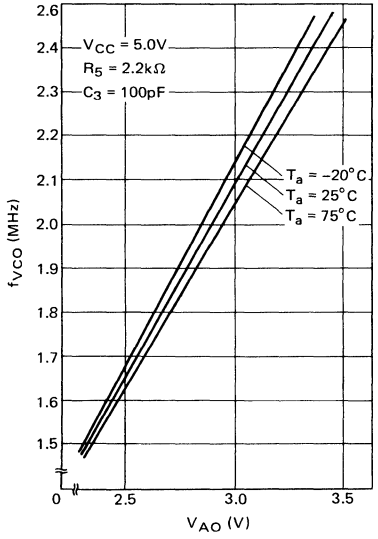


Fig. 2 – FREE RUN FREQUENCY vs. C_3

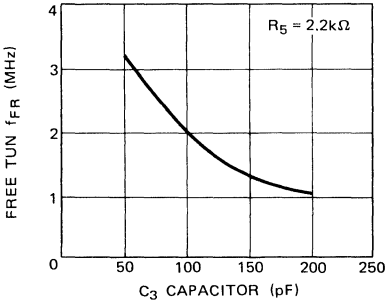


Fig. 3 – FREE RUN FREQUENCY vs. T_a

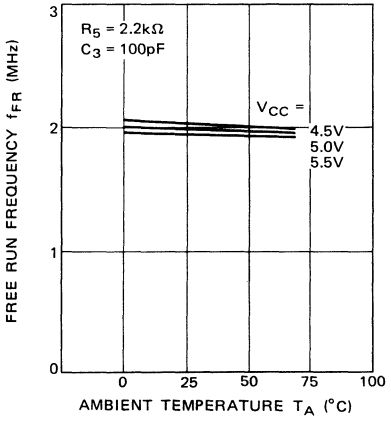
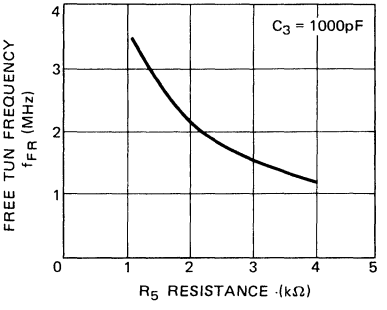


Fig. 4 – FREE RUN FREQUENCY vs. R_5



6

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Fig. 5 – TIME MARGIN vs. T_a

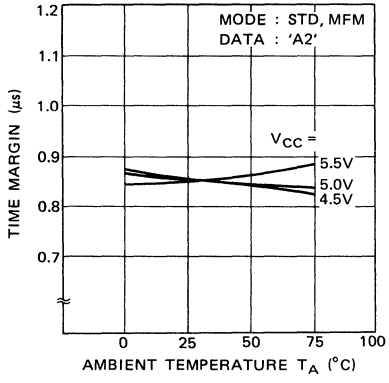


Fig. 6 – TIME MARGIN vs. FREE RUN FREQUENCY

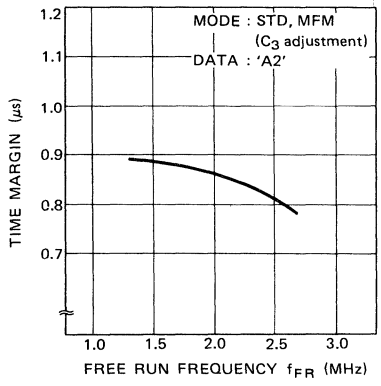
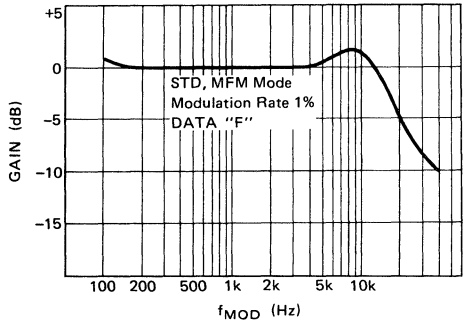
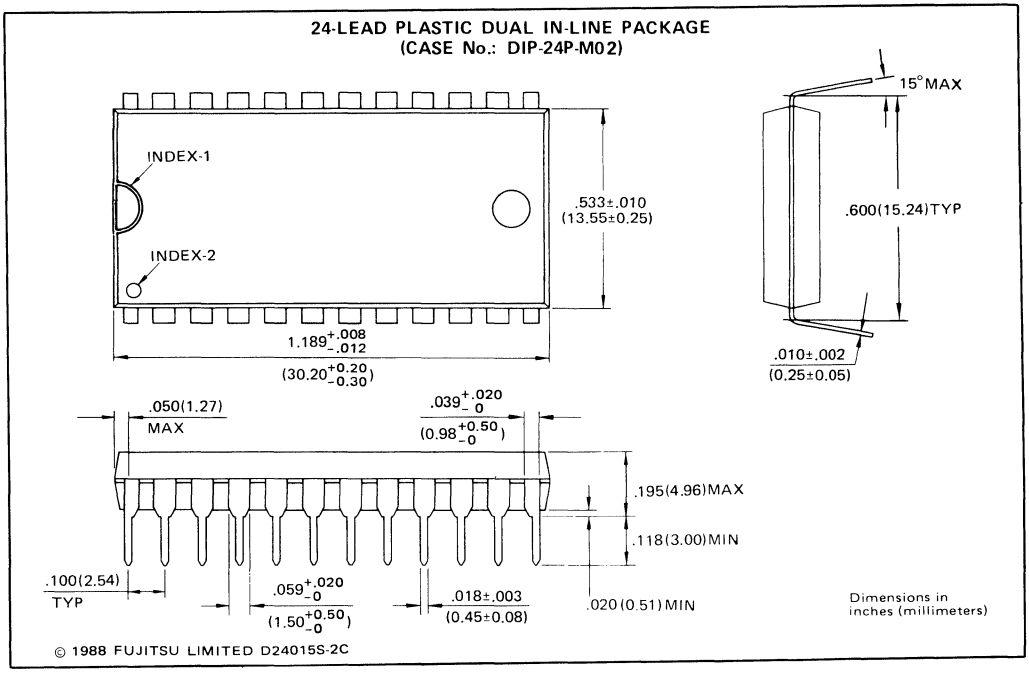


Fig. 7 – GAIN vs. f_{MOD}



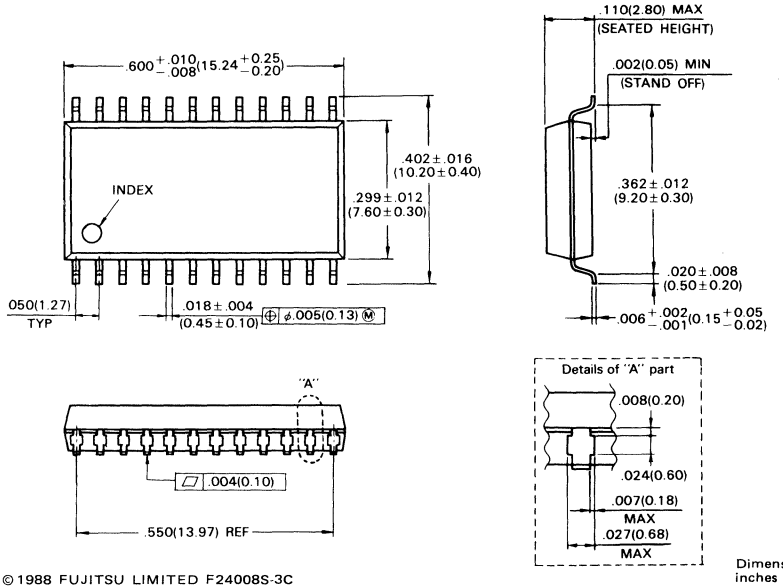
PACKAGE DIMENSIONS



6

PACKAGE DIMENSIONS (continued)

24-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-24P-M02)



Dimensions in inches (millimeters)

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FUJITSU

FLOPPY DISK VFO

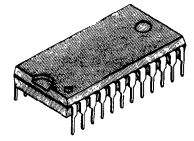
MB4108A

August 1988
Edition 1.0

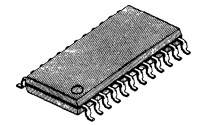
FLOPPY DISK VFO

PRELIMINARY

The Fujitsu MB4108A is variable frequency oscillator (VFO) IC for use in floppy-disk interfaces. It provides a complete data separation function, with a minimum of external parts and no adjustments, and can be used with a variety of disk controllers. It locks onto the read signal from the disk drive, which normally has jitter due to rotation speed variations and peak shifting and produces a stable read signal for the controller. It also produce a window signal which can be used to differentiate the clock and data pulse in the read signal. The MB4108A includes functions for sync field detection, automatic loop filter gain switching and address and index mark detection.



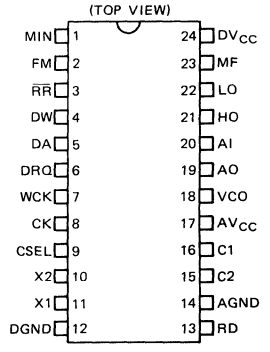
DIP-24P-M02



FPT-24P-M02

- The analog VFO (PLL) circuitry allows a wide read margin for the data separator.
- Can be connected to both 8-inch and 5-inch floppy disk drives using the same external components.
- Handles both double-density (MFM) and single-density (FM) disks.
- Can be used with various floppy disk controllers such as the MB8876A, MB8877A, FD1791 and μPD765.
- The discrimination function for gap and sync fields prevents incorrect locking on the gap field.
- The quick sync function (high gain) in the sync field is automatically switched to the stable tracking function (low gain)
- Because the sync pattern detector (data: 00H, clock: FFH) and the IBM format mark detector control PLL gain, the index, ID and data fields can be locked onto without special control signals.
- A master clock is generated for the floppy disk controller, to prevent spikes when switching between 8 and 5 inch floppy disks.
- External circuitry requires very few components and no adjustment.
  Internal clock: 7 resistors, 5 capacitors, 1 crystal or ceramic resonator
  External clock: 5 resistors, 3 capacitor

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Condition	Value	Unit
Power Supply Voltage	V_{CC}		7	V
Input Voltage	V_{IN}		7	V
Power Dissipation	P_D	$T_A \leq 75°C$	550	mW
Storage Temperature	T_{STG}		−55 to +125	°C
MF Input Voltage	V_{MF}		V_{CC}+0.3	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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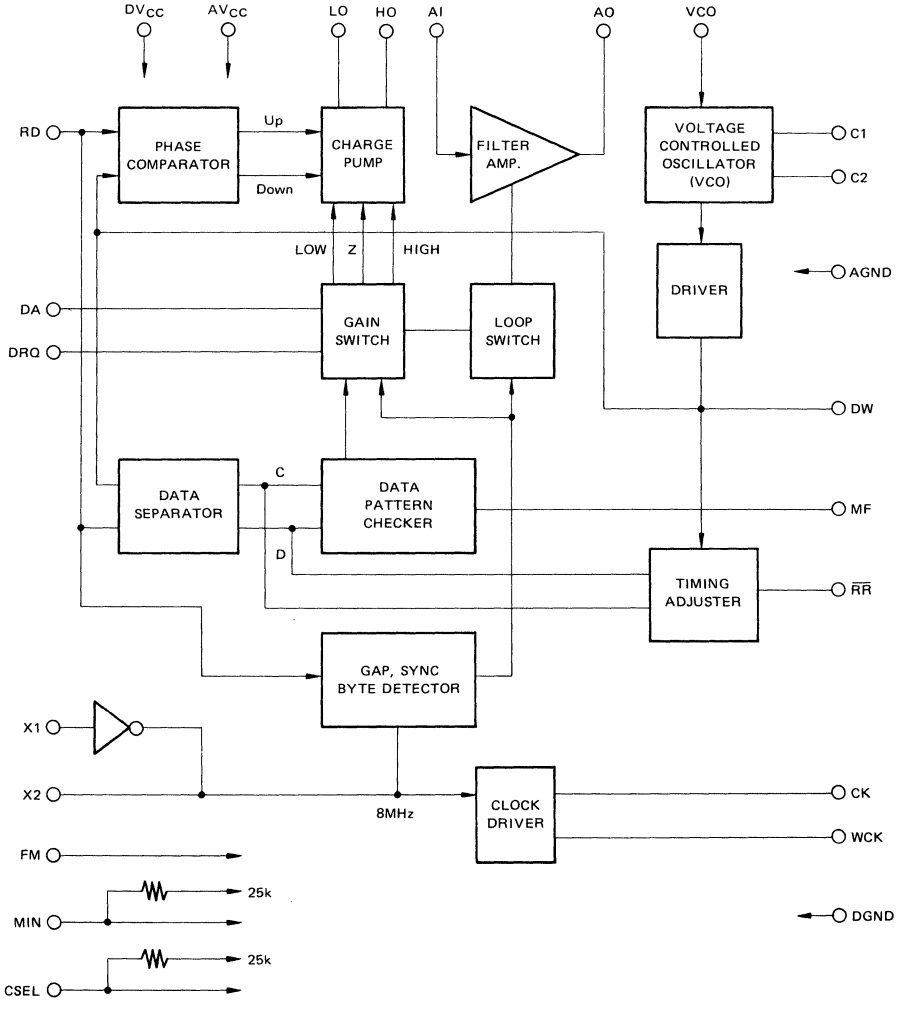
Fig. 1 – MB4108A BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Function
1	MIN	Selects type of floppy disk 5-inch floppy disk (MIN): High 8-inch floppy disk (STD): Low
2	FM	Selects the disk density Single density (FM system): High Double density (MFM system): Low
3	$\overline{RR}$	Read data signal for FDC includes clock and data pulse.
4	DW	Data window signal for separating the $\overline{RR}$ signal into data and clock pulses.
5	DA	Input for indicating a data field when there is no DRQ signal. When DRQ = H, the PLL keeps a low gain. Either RG or DA is used, but not both and the unused in is kept low.
6	DRQ	Input for Data Request. After mark is detected, PLL is kept as low gain when DRQ = H (positive edge trigger). 3 bytes data is input, PLL becomes high gain (Free run) when DRQ=L.
7	WCK	The μPD765 system FDC write clock pulse is output from this pin 8-inch/MFM : T = 1μs 8-inch/MF : T = 2μs 5-inch/MFM : T = 2μs 5-inch/MF : T = 4μs
8	CK	The FDC clock pulse is output from this pin MB8877A system/8-inch : 2MHz MB8877A system/5-inch : 1MHz μPD765 system/8-inch : 8MHz μPD765 system/5-inch : 4MHz
9	CSEL	Select the FDC type (On chip pull-up resistor) MB8877A, FD1791 system: High μPD765 system : Low
10	X2	Inverting output of the crystal oscillator The pin is open when 8MHz external clock is used.
11	X1	Inverting input of the crystal oscillator Input pin when 8MHz external clock is used.
12	DGND	Ground of digital circuit
13	RD	Source read data input from FDD
14	AGND	Ground for analog circuit such as VCO, filter amplifier
15 16	C1 C2	An external capacitor is connected to set VCO oscillation frequency
17	AV_{CC}	Power supply for analog circuit such as VCO and filter amplifier.
18	VCO	VCO control current input
19	AO	Low pass filter (LPF) output in the VFO circuit
20	AI	Low pass filter (LPF) input in the VFO circuit
21	HO	Output pin to be externally connected to the LPF amplifier. This pin is selected at frequency lock after a sync field is detected. High signal decreases VCO frequency and Low signal increase it (high gain).
22	LO	Output pin to be externally connected to the LPF amplifier. This pin is selected after frequency lock for phase synchronization. High signal delays the VCO phase and low signal advance it (low gain).
23	MF	When free run mode and high gain mode, MF becomes high. After mark is detected, it becomes low and keeps low level during low gain.
24	DV_{CC}	Power supply for digital circuit

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.75	5.00	5.25	V
Operating Temperature	T_A	−20	+25	+75	°C

DC CHARACTERISTICS

(V_{CC} = 5V, T_A = 25°C)

Parameter	Symbol	Condition	Value			Unit	Pin name	Note
			Min	Typ	Max			
Power Supply Current	I_{CC}	V_{CC} = 5.25V		70	100	mA	V_{CC}	*1
Input High Voltage	V_{IH}	V_{CC} = 4.75 to 5.25V, T_A = −20 to 75°C	2.0			V	MIN, FM, DA, DRQ, CX, X1, RD	
Input Low Voltage	V_{IL}				0.8	V		
Input High Current	I_{IH}	V_{CC} = 5.25V, V_I = 2.7V			20	μA	FM, DA, DRQ, X1, RD	
Input Current	I_I	V_{CC} = 5.25V, V_I = 7.0V			0.1	mA		
Input Low Current	I_{IL}	V_{CC} = 5.25V, V_I = 0.4V	−400	−20		μA		
Open-circuit Input Voltage	V_{IP}		4.85	5.0		V	MIN, CS	
Input Low Current	I_{ILP}	V_I = 0V	−1.1	−0.6		mA		
Output High Voltage*1	V_{OH1}	V_{CC} = 4.75V, I_{OH} = −1.2mA, T_A = −20 to 75°C	2.7	3.3		V	$\overline{RR}$, DW	*2
Output Low Voltage*1	V_{OL1}	V_{CC} = 4.75V, T_A = −20 to 70°C, I_{OL} = 12mA		0.28	0.4	V		*3
		V_{CC} = 4.75V, T_A = −20 to 70°C, I_{OL} = 24mA		0.35	0.5	V		
Short-Circuit Output Current*1	I_{OS1}	V_{CC} = 5.25V, T_A = −20 to 75°C	−30		−160	mA		*2

Note: *1 AV_{CC} and DV_{CC} are connected together.
*2 The output stage is set high.
*3 The output stage is set low.

DC CHARACTERISTICS

(V_{CC} = 5V, T_A = 25°C)

Parameter	Symbol	Condition	Value			Unit	Pin name	Note
			Min	Typ	Max			
Output High Voltage*2	V_{OH2}	V_{CC} = 4.75V, I_{OH} = −0.4mA, T_A = −20 to 75°C	2.7	3.3		V	WCK, CK	*2
Output Low Voltage*2	V_{OL2}	V_{CC} = 4.75V, T_A = −20 to 75°C, I_{OL} = 4mA		0.28	0.4	V	WCK, CK	*3
		V_{CC} = 4.75V, T_A = −20 to 75°C, I_{OL} = 8mA		0.35	0.5	V	WCK, CK	*3
Short-Circuit Output Current*2	I_{OS2}	V_{CC} = 5.25V, T_A = −20 to 75°C	−20		−110	mA	WCK, CK	*2
Output High Voltage*3	V_{OH3}	V_{CC} = 4.75V, I_{OH} = −0.4mA, T_A = −20 to 75°C	2.7	3.3		V	X2	*2
Output Low Voltage*3	V_{OL3}	V_{CC} = 4.75V, I_{OL} = 1mA, T_A = −20 to 75°C		0.28	0.4	V	X2	*3
Output Leakage Current	I_{OH4}	V_{CC} = 5.25V, V_O = 5.25V			20	μA	MF	*2
Output Low Voltage	V_{OL4}	V_{CC} = 5.25V, I_O = 1mA, T_A = −20 to 75°C		0.35	0.5	V	MF	*3
Output High Voltage	V_{HH}	I_{OH} = −1mA	3.3	3.7		V	HO	*2
Output Low Voltage	V_{LH}	I_{OL} = 1mA		2.0	2.4	V	HO	*3
Output High Voltage	V_{HL}	I_{OH} = −0.2mA	3.8	4.2		V	LO	*2
Output Low Voltage	V_{LL}	I_{OL} = 0.2mA		1.5	1.9	V	LO	*3
V_{CC} Free Running Frequency	f_{FR}		1.6	2.0	2.4	MHz		

Notes: *2 The output stage is set high.
*3 The output stage is set low.

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AC CHARACTERISTICS

(V_{CC} = 5V, f_{X1} = 8MHz)

Pin Name	Parameter	Symbol	Condition		Value			Unit
					Min	Typ	Max	
CK	Rising Time	t_r	C_L = 25pF			3		ns
	Falling Time	t_f				2		
	Frequency	f_{CK}	CSEL = H MB8876A	MIN = L		2		MHz
				MIN = H		1		
			CSEL = L μPD765	MIN = L		8		
				MIN = H		4		
	Duty Ratio	DR_{CK}	CSEL = H	C_L = 25pF		50		%
			CSEL = L			50		
WCK	Rising Time	t_r	C_L = 25pF			3		ns
	Falling Time	t_f				2		
	Cycle Time	T_{CY}	MIN = L	MFM = H		1		μs
				MFM = L		2		
			MIN = H	MFM = H		2		
				MFM = L		4		
	High level Width	T_{WH}	MIN = L	MFM = H		250		ns
				MFM = L		250		
			MIN = H	MFM = H		500		
				MFM = L		500		

6

(V_{CC} = 5V, f_{X1} = 8MHz)

Pin Name	Parameter	Symbol	Condition		Value Min	Value Typ	Value Max	Unit
DW	Rising Time	t_r	C_L = 25pF			3		ns
	Falling Time	t_f				2		
	Window Pulse Width (High level width)	T_W	MIN = L	MFM = H		1		μs
				MFM = L		2		
			MIN = H	MFM = H		2		
				MFM = L		4		
$\overline{RR}$	Rising Time	t_r	C_L = 25pF			3		ns
	Falling Time	t_f				2		
	Low-level Width	T_{WL}	MIN = L	MFM = H		0.25		μs
				MFM = L		0.5		
			MIN = H	MFM = H		0.5		
				MFM = L		1		
	Time Deviation from DW Center	T_D				10		ns
RD	High-level Width	T_{WH}			50			
DRQ	High-level Width	T_{WH}			50			
X1	External Clock Duty Ratio	DXET	f_{X1} = 8MHz/9.6MHz		45	50	55	%

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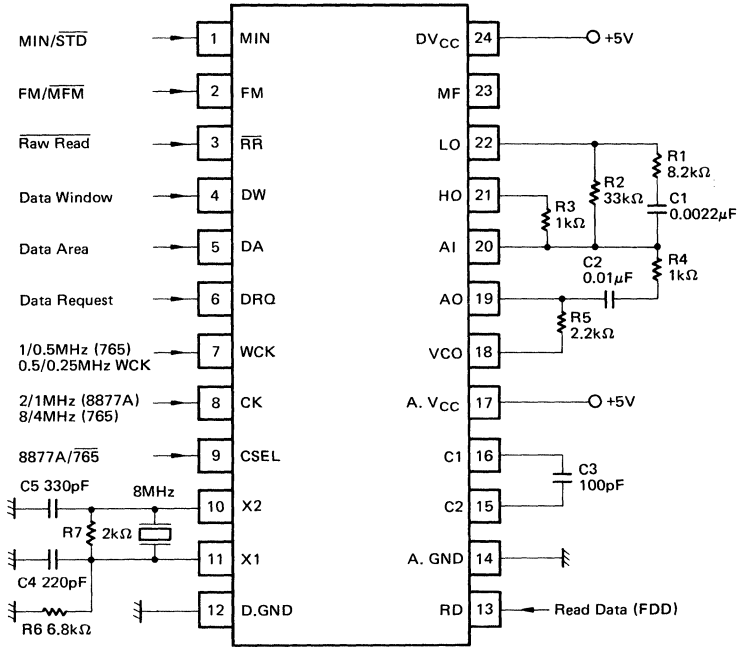
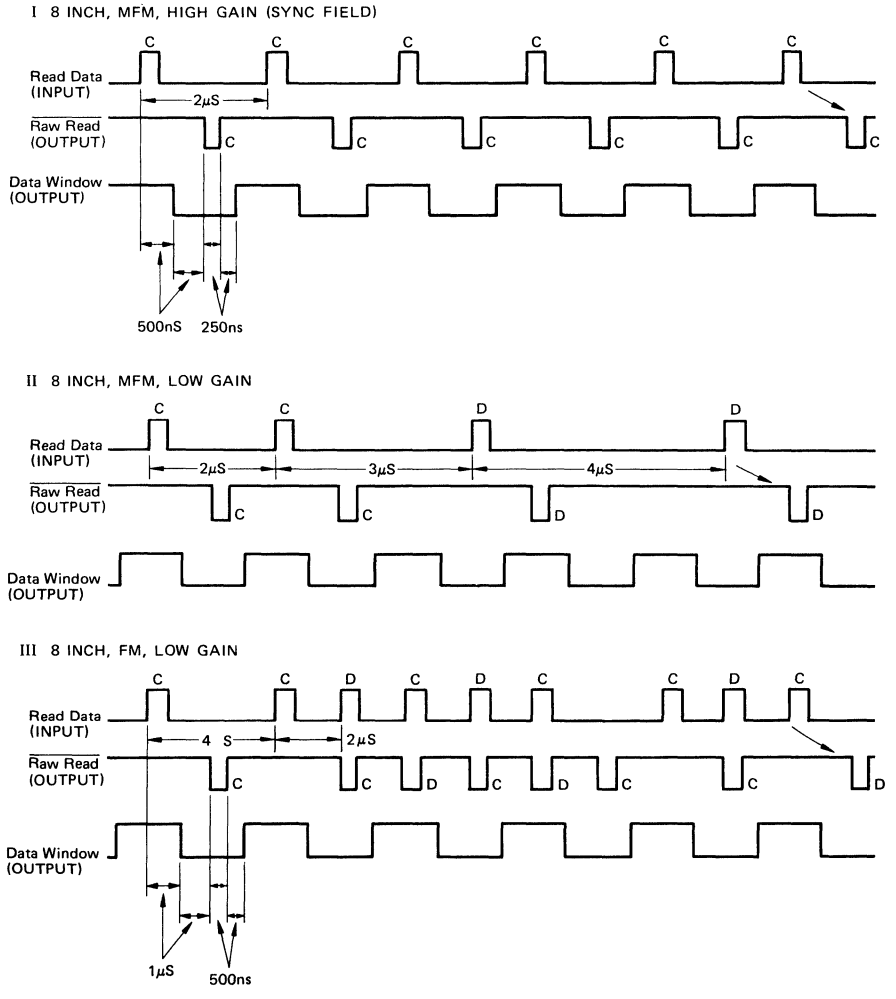
Fig. 2 – STANDARD EXTERNAL CIRCUITS



Notes: 1. C_3 (±5%), R_5 (±1%), otherwise C (±10%), R (±5%)
2. Since the 8MHz internal and 8MHz external clocks require precision of ±1%, a ceramic resonator can be used when WCK and CK do not required a high precision.

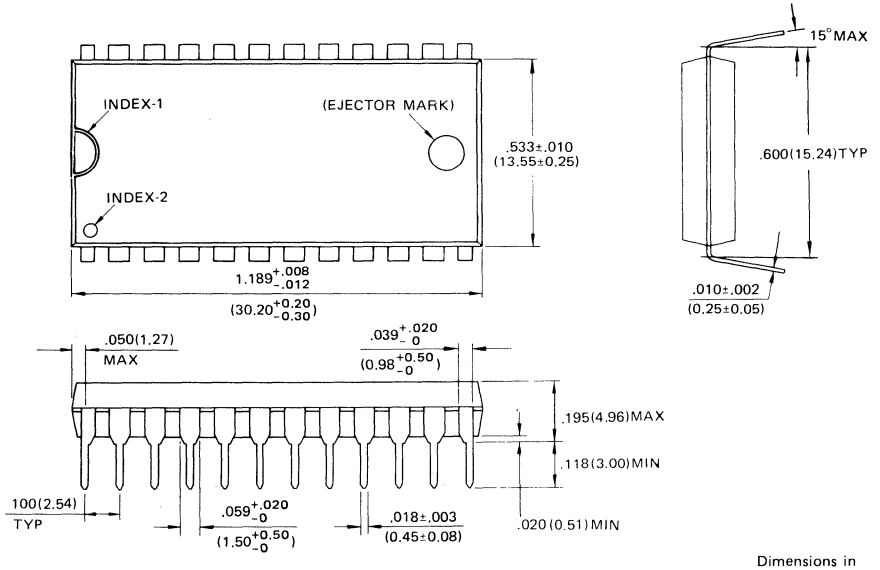
Fig. 3 – TIMING DIAGRAM



Notes: 1. The above times are doubled for 5-inch floppy disks.
2. C = clock pulse, D = data pulse.

PACKAGE DIMENSIONS

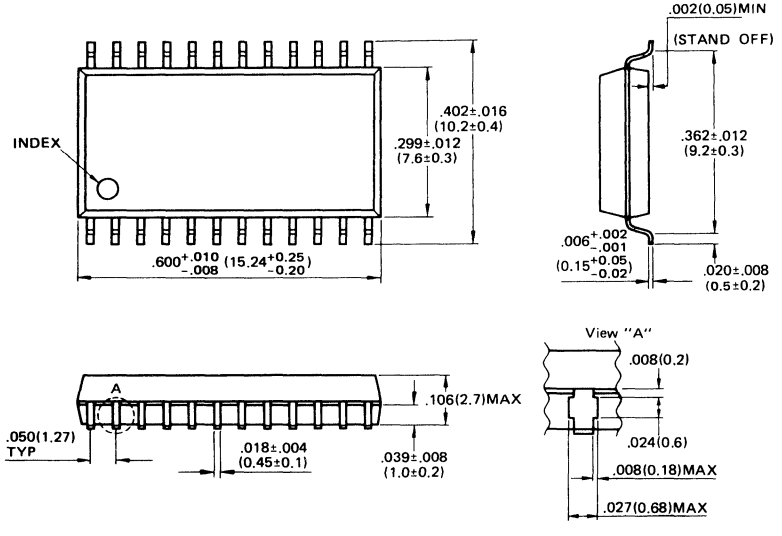
24-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-24P-M02)



Dimensions in
inches (milimeters)

6

24-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-24P-M02)



Dimensions in
inches (millimeters)

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FUJITSU

MAGNETIC DISK HEAD AMPLIFIER

MB4111 MB4113

December 1988
Edition 3.0

MAGNETIC DISK HEAD AMPLIFIER

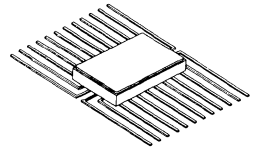
The Fujitsu MB4111/MB4113 is a monolithic bipolar integrated circuit optimized for high performance application to disk head systems.

The MB4111/MB4113 is featured with the following four major functions to interface with four magnetic heads.

- Write Amplifier Circuit
- Read Amplifier Circuit
- $\overline{RAS}$ (safety) Circuit
- Selection Decode Circuit

Also, the MB4111/MB4113 has three modes, Read, Write and Idle.

The MB4111/MB4113 is suitable for mounting directly on the arm of movable disk head.



CERAMIC PACKAGE
FPT-24C-F01

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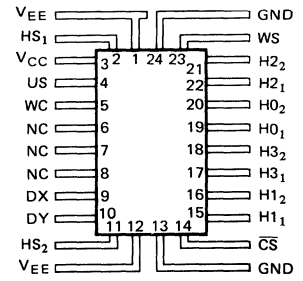
ABSOLUTE MAXIMUM RATINGS (*: Referenced to ground) (T_a = 25°C)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}*	7.0	V
Supply Voltage	V_{EE}*	-5.5	V
Operating Temperature	T_{OP}	0 to +70	°C
Storage Temperature	T_{STG}	-65 to +150	°C

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage (Read/Write/Idle)	V_{CC}	5.7		6.3	V
Supply Voltage (Read/Write/Idle)	V_{EE}	-4.2		-3.8	V

Ambient temperature: 0°C to +70°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

PIN NAMES

No.	Symbol	Name
1	V_{EE}	Supply Voltage
2	HS_1	Head Select 1
3	V_{CC}	Supply Voltage
4	US	Unsafe
5	WC	Write Current
6	NC	Non-connection*
7	NC	Non-connection*
8	NC	Non-connection*

No.	Symbol	Name
9	DX	Data X
10	DY	Data Y
11	HS_2	Head Select 2
12	V_{EE}	Supply Voltage
13	GND	Ground
14	WS	Write Select
15	H11	Head 1
16	H12	

No.	Symbol	Name
17	H31	Head 3
18	H32	
19	H01	Head 0
20	H02	
21	H21	Head 2
22	H22	
23	$\overline{CS}$	Chip Select
24	GND	Ground

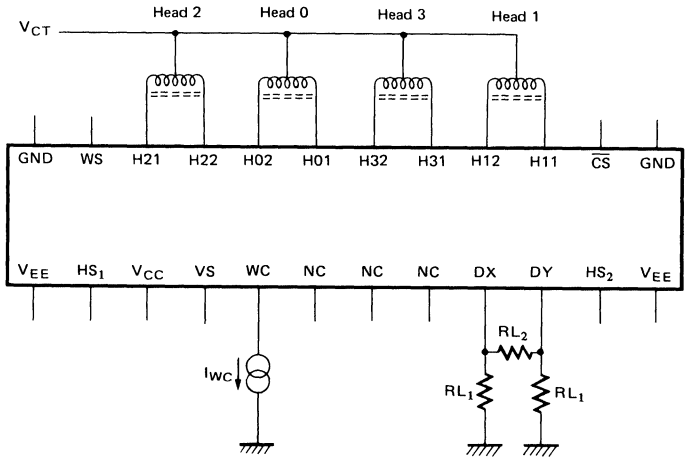
Note: NCs should be left open any time.

6

TEST CONDITIONS

Parameter	Symbol	Mode		Value	Unit
Supply Voltage	V_{CC}	Read/Write/Idle		6.0 ± 1.0%	V
	V_{EE}			-4.0 ± 1.0%	
Head Inductance	L_h	Read/Write	DC	0 (short)	μH
			AC	9.0	
Write Select Voltage	V_{WS}	Write		3.5 ± 1.0%	V
		Read		0.0 ± 0.01	
Chip Select Voltage	V_{CS}	Read/Write		0.0 ± 0.01	V
		Idle		6.0 ± 1.0%	
Unsafe Voltage	V_{US}	Read/Write/Idle		6.0 ± 1.0%	V
Termination Resistor	R_{L1}	Read/Write/Idle		200 ± 1.0%	Ω
	R_{L2}			100 ± 1.0%	
Write Current	I_{WC}	Write		40.0 ± 1.0%	mA
		Read		0.0 ± 0.2	
Ambient Temperature	T_A	Read/Write/Idle		25.0 ± 2.0	°C

Fig. 1 – TEST CIRCUIT



Note: NCs should be left open.

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ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Supply Current	I_{CC}	12	16	20	mA	Selected
				100	μA	Non Selected
	I_{EE}	-70			mA	Selected
		-45				Non Selected

MODE SELECT

Parameter	Sybmol	Mode	Value			Unit	Note
			Min	Typ	Max		
$\overline{CS}$ Input High Voltage	V_{IHC}	Idle	5.7	6.0	6.3	V	$-50\mu A < I_{CS} < 0\mu A$
$\overline{CS}$ Input Low Voltage	V_{ILC}	Read/Write	0.0	0.35	0.7	V	
$\overline{CS}$ Input High Current	I_{IHC}	Idle	-70			μA	
$\overline{CS}$ Input Low Current	I_{ILC}	Read/Write	-1.3	-1.0	-0.6	mA	V_{CS} = 0V
WS Input High Voltage	V_{IHW}	Write/Idle	3.2	3.5	3.8	V	
WS Input Low Voltage	V_{ILW}	Read/Idle	0	0.1	0.2	V	
WS Input High Current	I_{IHW1}	Write/Idle	0.7		2.8	mA	Transition Unsafe OFF
	I_{IHW2}	Write/Idle	0.7		3.5	mA	Transition Unsafe ON
WS Input Low Current	I_{ILW}	Read/Idle			0.1	mA	
Switching Delay	t_{SD}	All Modes			500	ns	

6

TOTAL HEAD INPUT CURRENT

Parameter	Symbol	Mode	Value			Unit	Note
			Min	Typ	Max		
Input Current	I_{I1}	Write			3.0	mA	V_{CT} = 3.5V
Input Current	I_{I2}	Read			0.16	mA	V_{CT} = 0V
Input Current	I_{I3}	Idle			0.5	mA	V_{CT} = 0, 3.5V

HEAD SELECT

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
HS Input High Voltage	V_{IHH}	T_A = 0°C to +70°C	-0.96		-0.81	V
HS Input Low Voltage	V_{ILH}	T_A = 0°C to +70°C	-1.85		-1.65	V
HS Input High Current	I_{IHH}				240	μA
HS Input Low Current	I_{ILH}				30	μA
Switching Delay	t_{SDH}				100	ns

HEAD SELECTION TABLE

Head No.	$\overline{CS}$	HS1	HS2
–	High	–	–
0	Low	High	High
1	Low	Low	High
2	Low	High	Low
3	Low	Low	Low

READ MODE

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Differential Gain		A_V	V_{IN} = 1mVp-p, 0V DC, f = 300KHz	22.0	35.0	46.0	V/V
Common Mode Rejection Ratio		CMRR	V_{IN} = 5mVp-p, 0V DC, f ≦ 5MHz	45			dB
Power Supply Rejection Ratio		SV_{RR}	V_{IN} = 0V, f ≦ 5MHz	45			dB
Band Width		BW	Z_{IN} = 0Ω (–3dB)	35			MHz
Channel Noise		V_n	V_{IN} = 0V, Z_{IN} = 0Ω, 10MHz Power Band Width			5.4	μV RMS
Input Current		I_{IN}	V_{IN} = 0V			40	μA
Input Capacitance		C_I				18.8	pF
Differential Input Resistance	MB4111	R_D		585	750	915	Ω
	MB4113			380	480	580	
Output Offset Voltage		V_{OFF}		–100		100	mV
Unsafe Current		I_U	V_{US} = 6.0V, I_{WC} = 45mA	40		45	mA
Dynamic Range		D		6			mVp-p
Channel Separation		S_I	See Note	40			dB
Common Mode Output Voltage		V_O		–0.75	–0.60	–0.45	V

Note: V_{IN} = 1mVp-p, f = 300KHz, 3 Channel driven.;

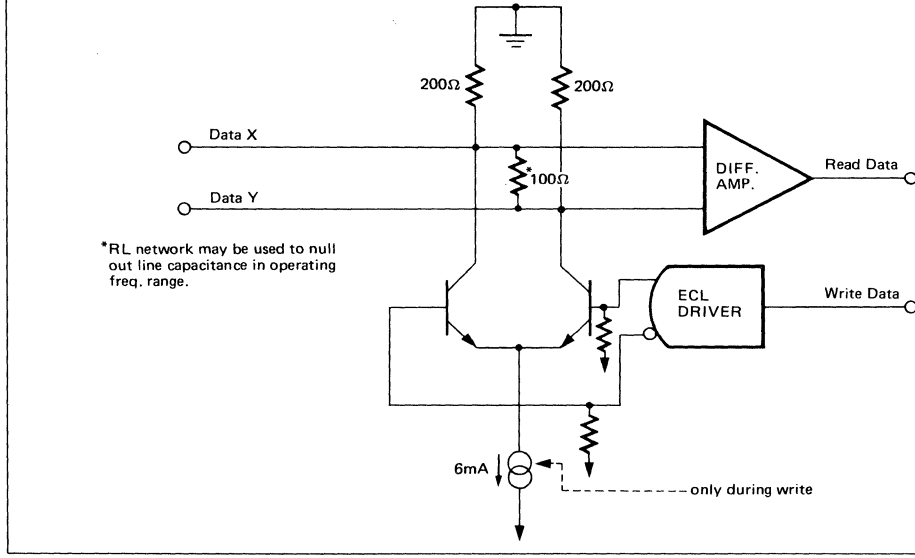
WRITE MODE

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Write Current		I_{WC}				50	mA
Current Gain		A_I	I_{WC} = 50mA	0.95			
Write Current Voltage		V_{WC}	I_{WC} = 50mA	V_{EE} +0.3		V_{EE} +1	V
Differential Input Voltage		V_{IN}		0.225			V
DX DY Input Current		I_{IN}		−2.0		2.0	mA
Unsafe Current		I_{US}	L = 7μH, f = 1.2MHz			0.1	mA
			L = 9μH, f = 0	20			
Head Current Transition Time		t_T	L = 0, f = 5MHz I_{WC} = 50mA		5	10	ns
Head Current Hysterisis		t_{HY}	L = 0, f = 5MHz I_{WC} ≧ 50mA			2.0	ns
Unselected Head Current		I_{OP}	L = 9μH, f = 2MHz, I_{WC} = 50mA			1.5	mA
Unsafe Switching Delay Time	MB4111	t_{USD}	L = 9μH, f = 6.0MHz to DC	0.5		4.0	μs
			L = 7μH, f = DC to 1.2MHz			1.0	
Differential Head Voltage		V_{DIF}	I_{WC} = 45mA L = 9μH	6.2		7.2	V

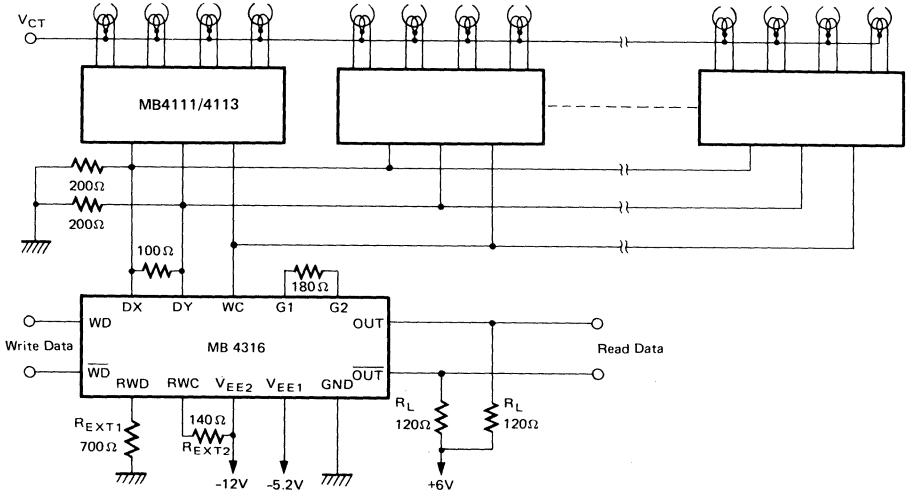
6

DISK HEAD APPLICATION NOTES

*BIDIRECTIONAL DATA BUS DRIVER

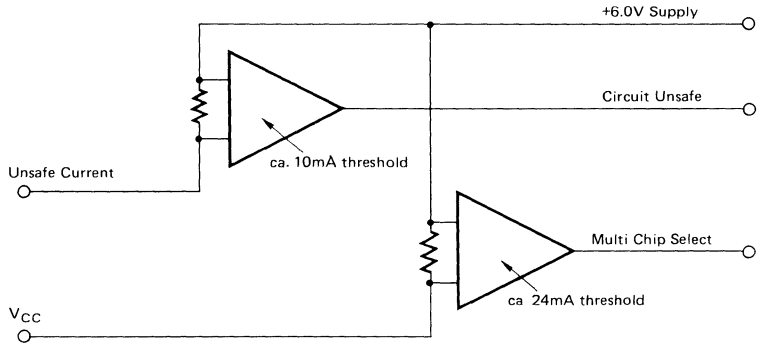


*USAGE IN COMBINATION WITH MB 4316 (BUS SWITCHING CIRCUIT)



Note: NCs should be left open.

*FAULT DETECTION CIRCUITRY



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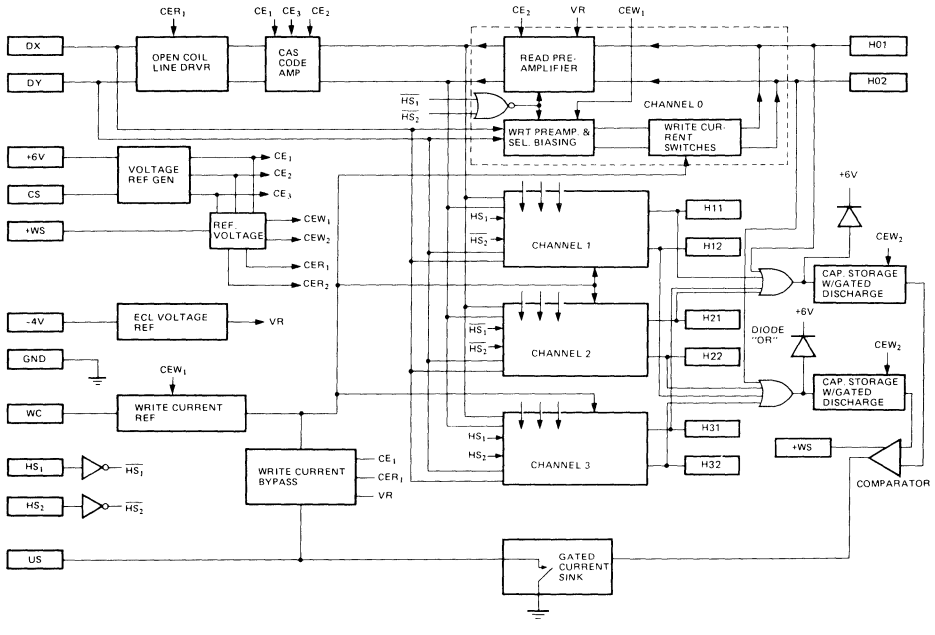
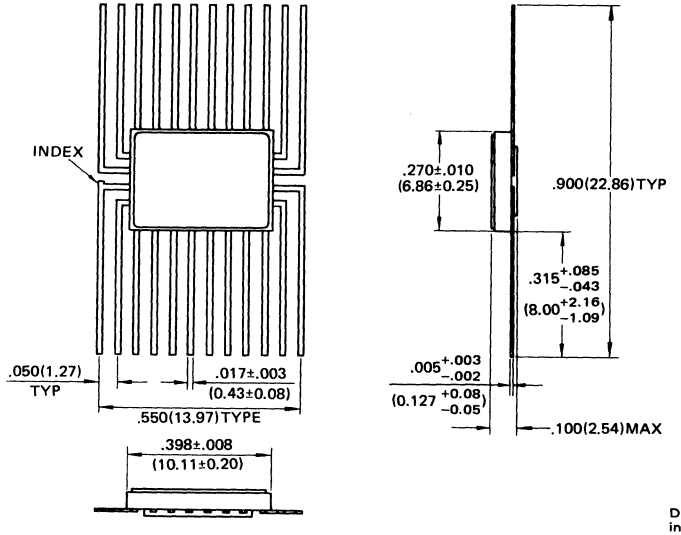
MB 4111/4113 BLOCK DIAGRAM



PACKAGE DIMENSIONS

24-PAD CERAMIC (FRIT SEAL) FLAT PACKAGE
(CASE No. : FPT-24C-F01)



Dimensions in
inches (millimeters)

6

January 1990
Edition 1.0

FUJITSU

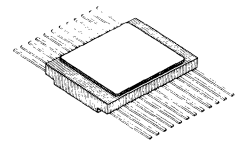
DATA SHEET

MB4114A
MAGNETIC DISK HEAD AMPLIFIER

4-ch MAGNETIC DISK THIN-FILM HEAD AMPLIFIER FOR HDD

The Fujitsu MB4114A is a monolithic bipolar integrated circuit optimized for high performance application to disk head system.
The MB4114A is 4-channel Read & Write Amplifier for thin film head of HDD.

- Power Supply Voltage: +5V and +12V
- Driving Four Thin-Film Disk Head
- Logic Interface: TTL Compatible
- On-chip write unsafe Detection circuitly
  Abnormal Detection on the Disk Head
- Low noise Read Amp.: 0.55nV/$\sqrt{Hz}$ typ.
- Low Input Capacitance: 27pF typ.



CERAMIC PACKAGE
FPT-24C-A01

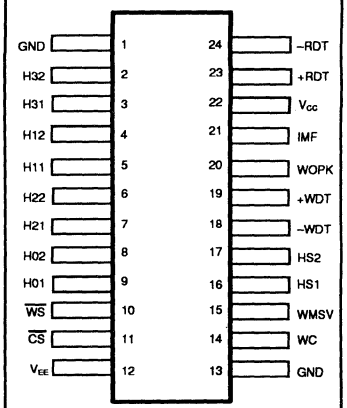
6

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Ratings	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.6 to +7.0	V
	V_{EE}	−10.0 to +0.6	V
Digital Input Voltage	V_{CS}, V_{WS} V_{HS1}, V_{HS2}	−0.4 to V_{CC} +0.3	V
	V_{+WDT}, V_{-WDT}	V_{EE} to +0.3	V
Head Input Voltage	V_{HEAD}	−0.6 to +0.4	V
Head Output Voltage	I_W	70	mA
Detection System Output Voltage	V_{WMSV}, V_{WOPK}, V_{IMF}	−0.4 to V_{CC} +0.3	V
Detection System Output Current	I_{SVL} I_{OPL}	20	mA
Write Current	I_{WC}	−70	mA
Read Output Voltage	V_{+RDT}, V_{-RDT}	−0.5 to V_{CC} +0.3	V
Storage Temperature	T_{stg}	−55 to 150	°C
Power Dissipation	P_D	1600($T_A \leq 25°C$)	mW

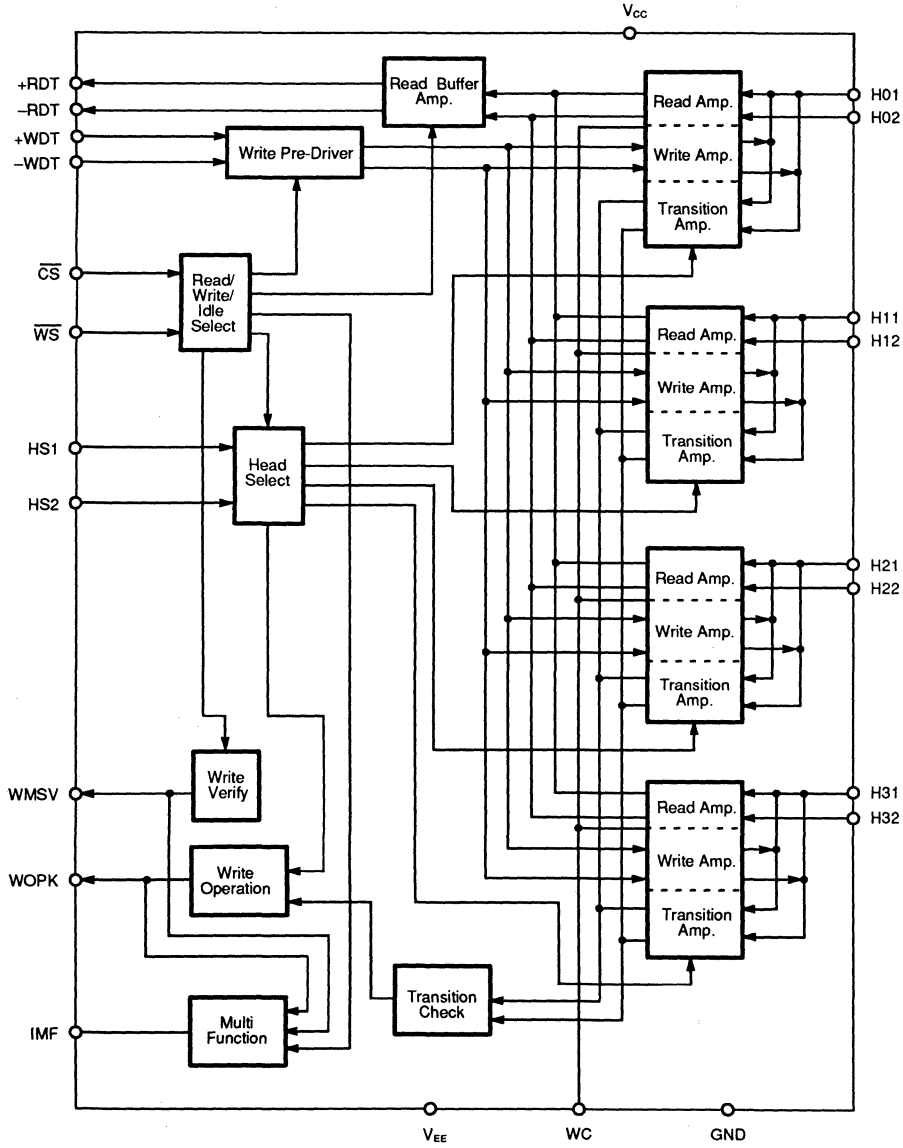
Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT
(TOP VIEW)



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Function
1	GND	Ground termination.
2 to 9	H01 to H31 H02 to H32	Disk Head connect termination. Channel 0 to 3.
10	$\overline{WS}$	Mode select termination (Read/Write) Refer to page 4.
11	$\overline{CS}$	Chip select termination. Control signal input termination which selects operating condition or Idle condition. Input logic interface is TTL compatible. Usage of plural MB4114A is possible.
12	V_{EE}	Power supply termination: –8V
13	GND	Ground termination. Should be connected with Pin No. 1.
14	WC	Write current termination. Should be connected with external power supply which is capable to drive "0 to 65mA".
15	WMSV	Monitor termination of write mode. When write mode is selected, this termination goes to low level. Open collector output.
16 17	HS1 HS2	Head select signal input termination. Let one of four channels to be operating mode. Input Logic interface is TTL compatible. Refer to page 4.
18 19	–WDT +WDT	Write Data differential input termination. Should be received differential signal input.
20	WOPK	Write mode abnormal detection output termination. Open collector output. To prevent mis-writing on the Disk, the output goes to high level when following conditions. • When input frequency of write data is "o". • When one of or both of head select termination is opened. • When head connect termination is opened. Refer to page 4.
21	IMF	Monitor termination of operating mode. The current flows from outside when Read or Write mode. Usage of plural MB4114A is possible. Refer to page 5.
22	V_{CC}	Power supply termination: +5V
23 24	+RDT –RDT	Output termination of Read Amp. circuit. Load Resistance (≥100Ω) should be connected between this termination and V_{CC}.

FUNCTION

1. MODE SELECTION TABLE

Mode	$\overline{CS}$ Termination Voltage	$\overline{WS}$ Termination Voltage
Idle (I)	H	–
Read (R)	L	H
Write (W)	L	L

Note) H: High Level L: Low Level

2. HEAD SELECTION TABLE

$\overline{CS}$ Termination Voltage	HS1 Termination Voltage	HS2 Termination Voltage	Head Selection
H	–	–	–
L	L	L	0
	H	L	1
	L	H	2
	H	H	3

Note) H: High Level L: Low Level

3. WMSV (WRITE MODE SELECT VERIFY) OUTPUT TRUTH TABLE

$\overline{CS}$ Termination Voltage	$\overline{WS}$ Termination Voltage	Mode	WMSV Termination Output Voltage
H	–	I	H
L	H	R	
	L	W	L

Note) H: High Level L: Low Level

4. WOPK (WRITE OPERATION OK) OUTPUT TRUTH TABLE

$\overline{CS}$ Termination Voltage	$\overline{WS}$ Termination Voltage	Mode	Condition	WOPK Termination Output Voltage
H	–	I	Idle Mode	H
L	H	R	Read Mode	
L	L	W	Write Mode	L
			Head Connect termination is opened. Head Select termination is opened. Input Frequency of write mode data is "0" Hz.	H

Note) H: High Level L: Low Level

FUNCTION (Continued)

5. IMF (MULTI FUNCTION CURRENT) OUTPUT TRUTH TABLE

$\overline{CS}$ Termination Voltage	$\overline{WS}$ Termination Voltage	Mode	Condition	IMF Output
H	–	I	Idle Mode	OFF
L	H	R	Read Mode	ON
L	L	W	Write Mode	
L	H	R	WMSV/WOPK terminations are opened or connected with GND.	OFF

Note) H: High Level L: Low Level

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	4.75 to 5.25	V
	V_{EE}	–8.40 to –7.60	V
Write Current	I_{WC}*	–5 to –65	mA
Operating temperature	Top	0 to 70	°C

Note) * Minus means current direction from IC to out side.

6

ELECTRICAL CHARACTERISTICS

1. DC CHARACTERISTICS

V_{CC} = 5V ± 5%, V_{EE} = –8V ± 5%, T_A = 25°C

Parameter		Symbol	Condition	Value				Unit
				Mode*	Min	Typ	Max	
Power Supply System	Power Supply Current (V_{CC})	I_{CCI}		I	–	6	12	mA
		I_{CCR}		R	–	30	67	
		I_{CCW}		W	–	24	50	
	Power Supply Current (V_{EE})	I_{EEI}		I	–10	–3	–	
		I_{EER}		R	–78	–50	–	
		I_{EEW}		W	–70	–46	–	
	Power Dissipation	Pd_I		I	–	60	180	mW
		Pd_R		R	–	650	1150	
		Pd_W	I_{WC} = –40mA	W	–	880	1320	
Digital System	High Level Input Voltage	V_{IH}	$\overline{CS}$, $\overline{WS}$, HS1, HS2		2.0	–	V_{CC} +0.3	V
	Low Level Input Voltage	V_{IL}	$\overline{CS}$, $\overline{WS}$, HS1, HS2		–0.3	–	0.8	
	+WDT,–WDT Input Voltage	V_{+WDT} V_{-WDT}			–1.87	–	0	
		ΔV_{IN}			0.25	0.9	–	
	$\overline{CS}$ Termination Input Current	I_{CSI}	$V_{CS} = V_{CC}$		–	–	0.1	mA
		I_{CSR}	V_{CS} = –0.3V, $V_{WS} = V_{IH}$		–1.6	–1.1	–	
		I_{CSW}	V_{CS} = –0.3V, $V_{WS} = V_{IL}$		–1.6	–1.1	–	
	$\overline{WS}$ Termination Input Current	I_{WSI}	$V_{WS} = V_{CC}$		–0.1	–	0.1	
		I_{WSR}	V_{WS} = 5.25V, $V_{CS} = V_{IL}$		–0.1	–	0.1	
		I_{WSW}	V_{WS} = –0.3V, $V_{CS} = V_{IL}$		–1.6	–1.1	–	
	HS Termination Input Current	I_{HSI}	V_{HS} = 5.25V, V_{CS} = 2V		–	–	0.1	
		I_{HSR}	V_{HS} = –0.3V, $V_{WS} = V_{IH}$		–	0.26	0.6	
		I_{HSW}	V_{HS} = –0.3V, $V_{WS} = V_{IH}$		–	0.26	0.6	
	+WDT,–WDT Termination Input Current	I_{WDI}	$V_{+WDT} = V_{-WDT}$ = –1.87V		–0.1	–	0.1	
		I_{WDW}	$V_{+WDT} = V_{-WDT}$ = –1.87V		–	9	50	µA

Note) * I: Idle, R: Read, W: Write

ELECTRICAL CHARACTERISTICS (Continued)

1. DC CHARACTERISTICS (Continued)

V_{CC} = 5V ± 5%, V_{EE} = –8V ± 5%, T_A = 25°C

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Read System	Head Input Bias Current	I_B	$V_{CS} = V_{IL}$, $V_{WS} = V_{IL}$	–	30	120	µA
	+RDT,–RDT Termination Output Current	I_{RDTI}	V_{CS} = 2.0V	–	–	0.1	mA
		I_{RDTR}	V_{CS} = 0.8V, V_{WS} = 2.0V	3	7	10	
	Output Offset Voltage	V_{OFF}	V_{WS} = 2.0V, Head termination short circuit	–	–	360	mV
	Input Resistance	R_I	Head terminal to GND	0.7	1.0	1.3	kΩ
Write System	Write Current Gain	Irat	V_{WS} = 0.8V, I_{WC} = –40mA Irat = I_W/I_{WC}	0.8	0.93	1.0	A/A
	WC Termination Voltage	V_{WC}	V_{WS} = 0.8V, I_{WC} = –30mA	V_{EE} –0.3	–8.0	–	V
	Non-Selected Head Current	I_{WOF}	V_{WS} = 0.8V, I_{WC} = –65mA	–	–	0.3	mA
Detection System	WOPK Output Voltage	V_{OPL}	V_{WS} = 2.0V, I_{WC} = –40mA	–	–	0.5	V
	WMSV Output Voltage	V_{SVL}	V_{CS} = 0.8V, V_{WS} = 0.8V	–	–	0.5	
	IMF Output Current (off)	I_{MFOF}		–	–	50	µA
	IMF Output Current (on)	I_{MFON}		2.4	3.0	3.6	mA

2. AC CHARACTERISTICS

V_{CC} = 5V ± 5%, V_{EE} = –8V ± 5%, T_A = 25°C

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Read System	Differential Volatge Gain	G_D	Vin = 1mV_{P-P}, fin = 1MHz R_L = 100Ω	100	145	190	V/V
	Band Width	B_W	Vin = 1mV_{P-P}, –3dB point, R_L = 100Ω	60	140	–	MHz
	Input Capacitance	C_I		–	27	–	pF
	Channel Noise	V_n	fin = 1 to 10MHz Head short	–	0.55	–	nV/√Hz
	Input Dynamic Range	D	fin = 10MHz, 3rd Harmonic wave	9	19	–	mA
	Common Mode Resistance Ratio	CMRR	Vin = 10mV_{P-P}, fin = 10MHz	40	60	–	dB
	Channel Separation	CSP	Vin = 1mV_{P-P}, fin = 1MHz	40	60	–	
	Power Supply Rejection Ratio	PSRR1	ΔV_{CC} = 0.1V_{P-P}, f = 10MHz	40	50	–	
		PSRR2	ΔV_{EE} = 0.1V_{P-P}, f = 10MHz	40	50	–	

6

ELECTRICAL CHARACTERISTICS (Continued)

3. SWITCHING CHARACTERISTICS

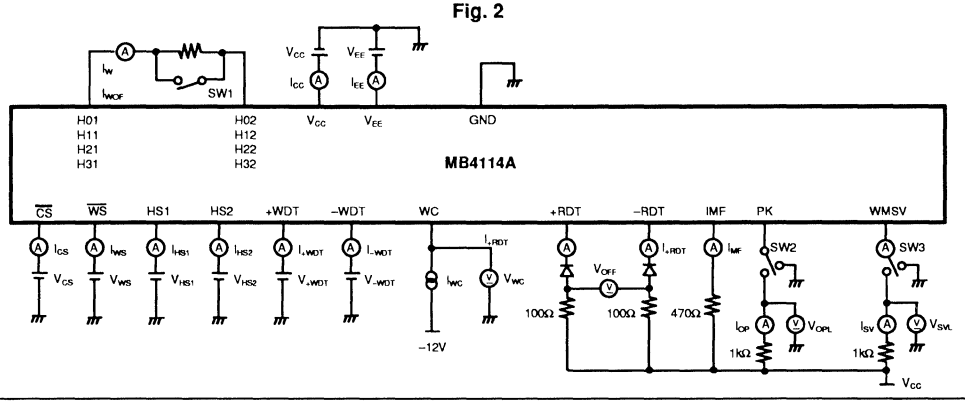
V_{CC} = 5V ± 5%, V_{EE} = −8V ± 5%, T_A = 25°C
L_H = 350nH, R_H = 20Ω, I_{WC} = −40mA

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Chip Select Transition Time	td_{LHW}, td_{HLR}	Idle → Write, Read	–	–	600	ns
	td_{HLW}, td_{LHR}	Write, Read → Idle	–	–	600	
Read/Write Transition Time	td_{LHW}	Read → Write	–	–	600	
	td_{LHR}	Read → Write	–	–	900	
Write/Read Transition Time	td_{HLW}	Write → Read	–	–	500	
	td_{HLR}	Write → Read	–	–	750	
Head Select Delay Time	td_{HLR}, td_{LHR}		–	–	500	
IMF Delay Time	td_{HL}		–	–	700	
	td_{LH}		–	–	500	
WMSV Delay Time	td_{HL}		–	–	650	
	td_{LH}		–	–	750	
WOPK Delay Time	$td_{\phi pL}$	fin = 0Hz → 2MHz, I_{WC} = −15mA	–	–	1000	
	$td_{\phi pH}$	fin = 18MHz → 0Hz	600	1600	3600	
Write Current Delay Time	tpd1		–	18	–	
	tpd2		–	18	–	
ΔWrite Current Delay Time	Δtpd		–	–	1	
Write Current Transition Time	tr		–	13	–	
	tf		–	13	–	

TEST CIRCUIT

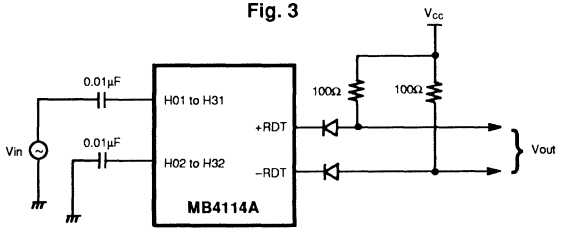
1. DC CHARACTERISTICS

Fig. 2



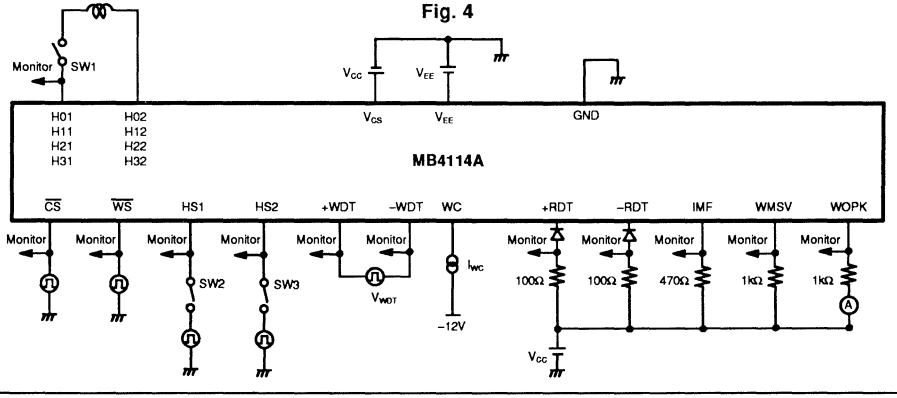
2. AC CHARACTERISTICS

Fig. 3



3. SWITCHING CHARACTERISTICS

Fig. 4



APPLICATION NOTES

Fig. 5

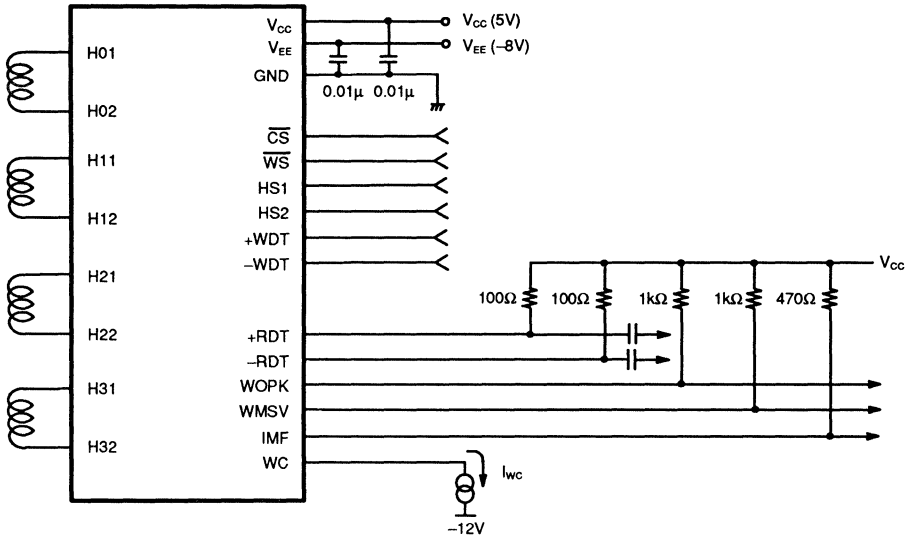
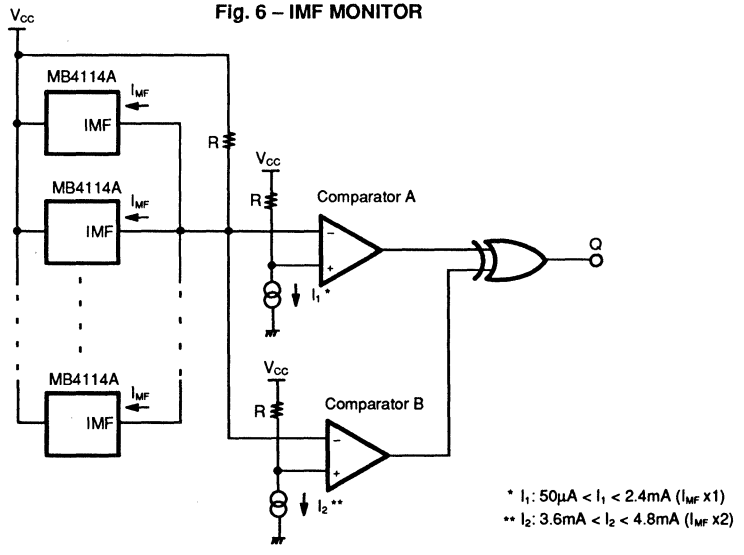


Fig. 6 – IMF MONITOR



6

TIMING CHART

Fig. 7 – CHIP SELECT TRANSITION TIME

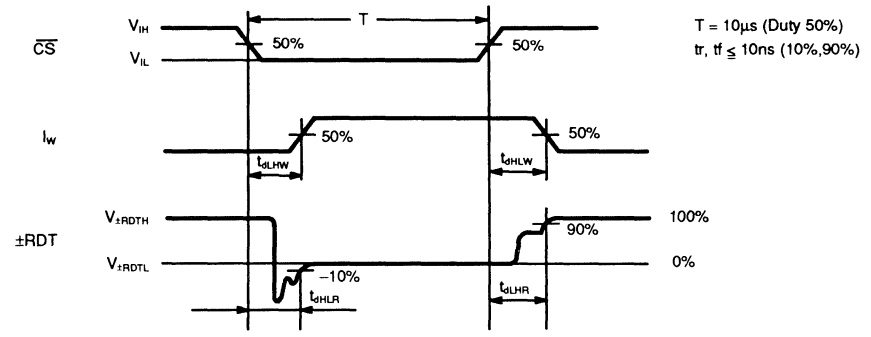


Fig. 8 – READ/WRITE, WRITE/READ TRANSITION TIME

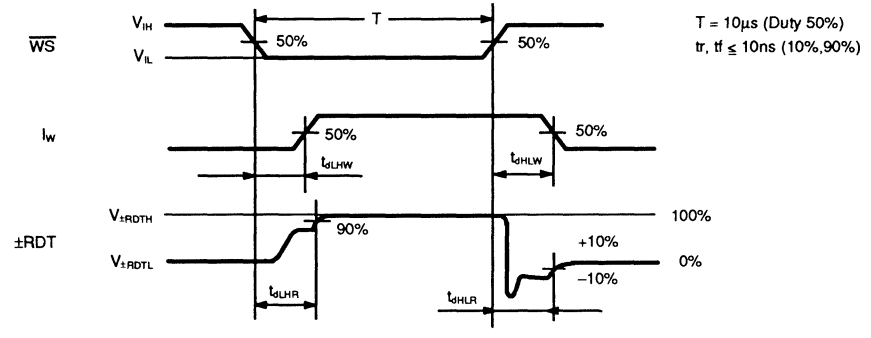
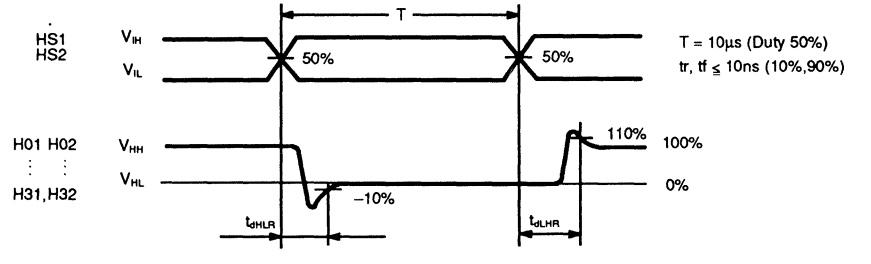


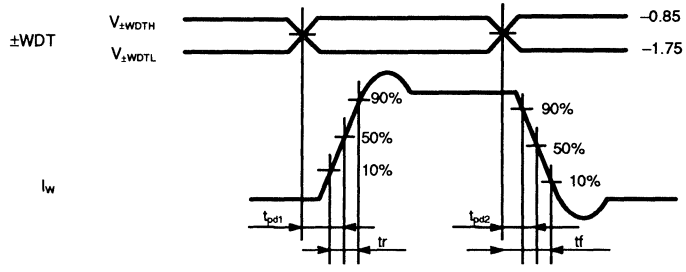
Fig. 9 – HEAD SELECT DELAY TIME



6

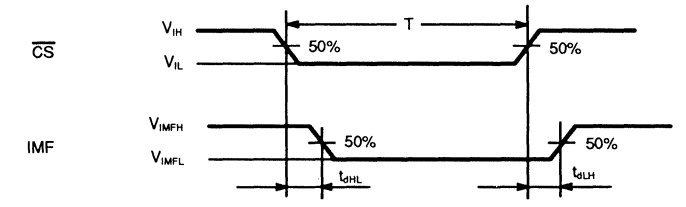
TIMING CHART (Continued)

Fig. 10 – WRITE CURRENT DELAY/TRANSITION TIME



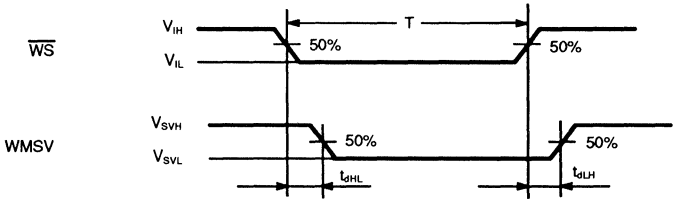
f_{WDT} = 5MHz
tr, tf ≦ 2ns (10%, 90%)

Fig. 11 – IMF DELAY TIME



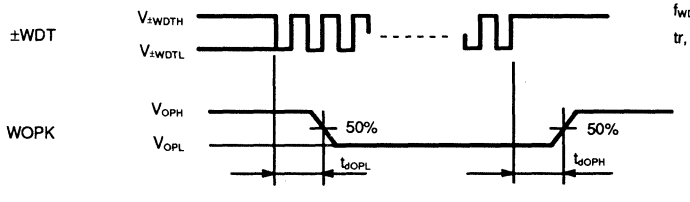
T = 10μs (Duty 50%)
tr, tf ≦ 10ns (10%,90%)

Fig. 12 – WMSU DELAY TIME



T = 10μs (Duty 50%)
tr, tf ≦ 10ns (10%,90%)

Fig. 13 – WOPK DELAY TIME



f_{WDT} = 2.0, 18MHz(Duty 50%)
tr, tf ≦ 2ns (10%,90%)

INPUT/OUTPUT EQUIVALENT CIRCUIT

Fig. 14 CS TERMINATION

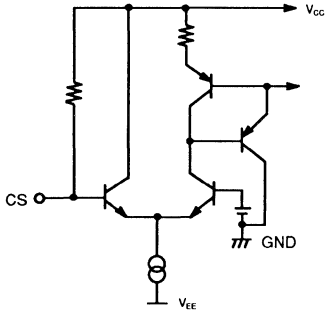


Fig.15 WS TERMINATION

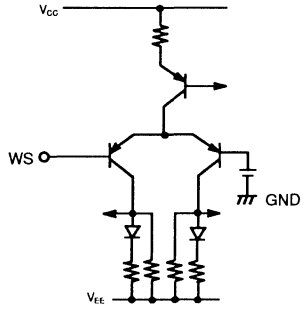


Fig. 16 HS1,HS2 TERMINATION

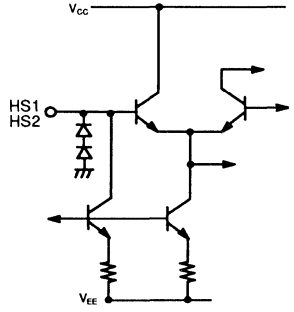


Fig. 17 –WDT, +WDT TERMINATION

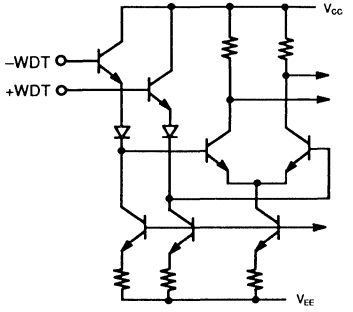


Fig. 18 IMF TERMINATION

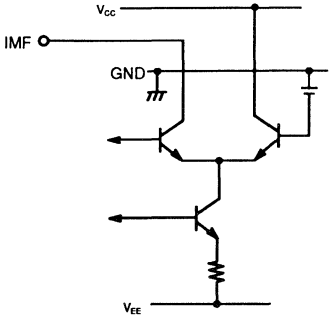
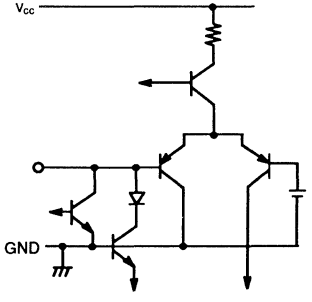


Fig. 19 WOPK, WMSV TERMINATION



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INPUT/OUTPUT EQUIVALENT CIRCUIT (Continued)

Fig. 20 HEAD SELECT TERMINATION

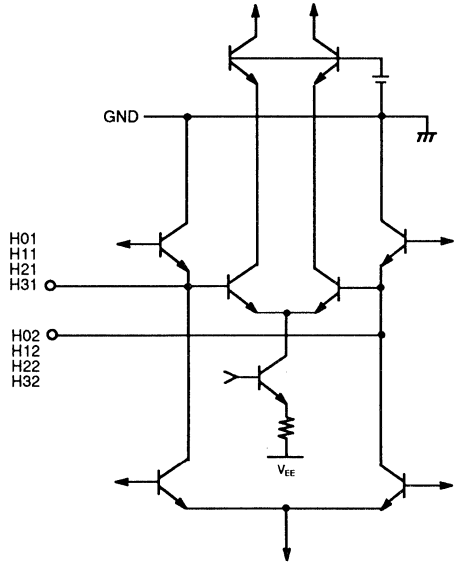


Fig. 21 –RDT, +RDT TERMINATION

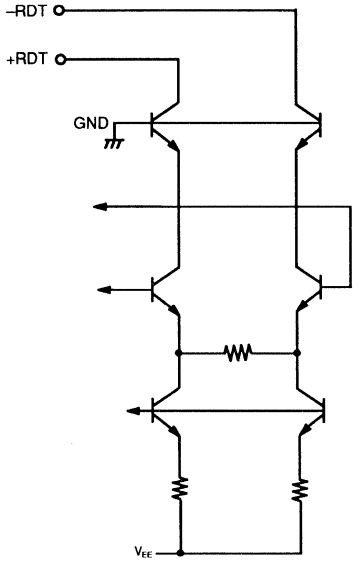
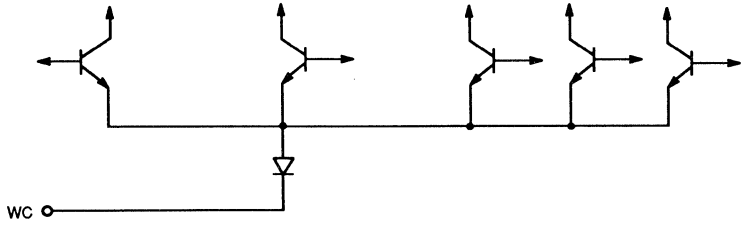


Fig. 22 WC TERMINATION



TYPICAL CHARACTERISTICS CURVES

Fig. 23 – WRITE CURRENT GAIN vs. WRITE CURRENT

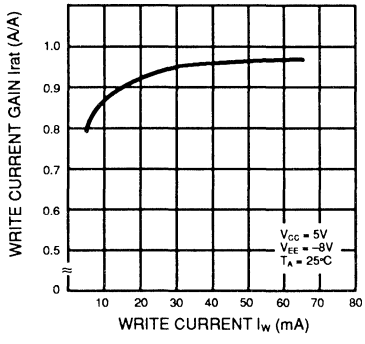


Fig. 24 – READ AMP. INPUT vs. OUTPUT VOLTAGE

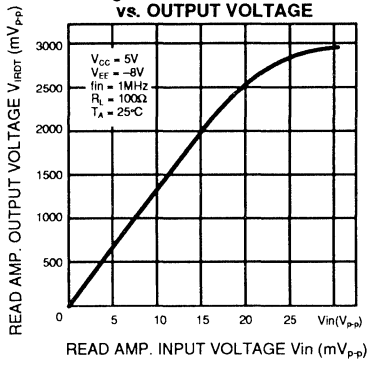


Fig. 25 – DIFFERENTIAL VOLTAGE GAIN vs. TEMPERATURE

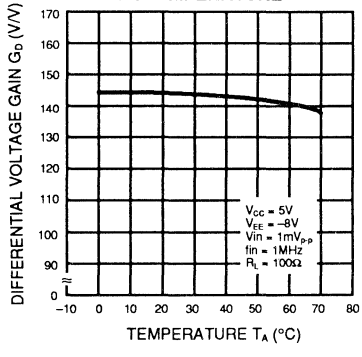


Fig. 26 – POWER DISSIPATION vs. TEMPERATURE

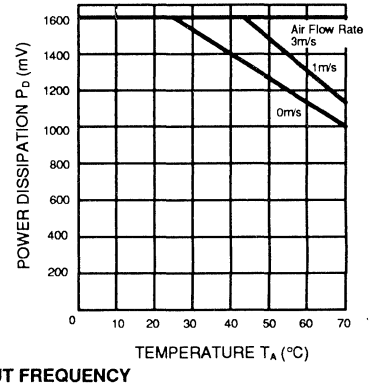
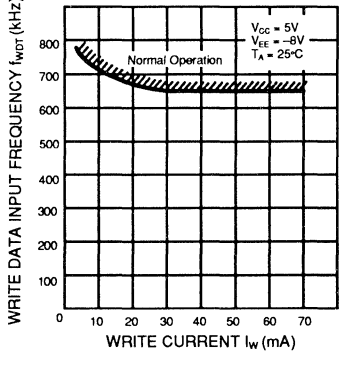
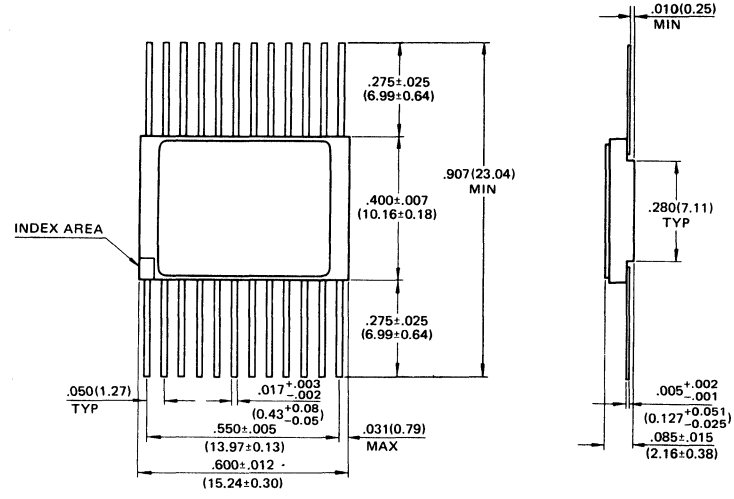


Fig. 27 –WRITE DATA INPUT FREQUENCY vs. WRITE CURRENT



PACKAGE DIMENSIONS

24-LEAD CERAMIC (METAL SEAL) FLAT PACKAGE
(Case No.: FPT-24C-A01)



Dimensions in
inches (millimeters)

6

October 1989
Edition 1.0

FUJITSU

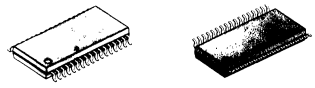
DATA SHEET

MB4115/4116/4125/4126
8–CH MAGNETIC DISC R/W AMP.FOR HDD

8–CHANNEL MAGNETIC DISK READ/WRITE AMPLIFIER FOR HDD

The Fujitsu MB4115/4116/4125/4126 are 8–channel magnetic disk read/write amplifier designed for hard disc drive equipments.

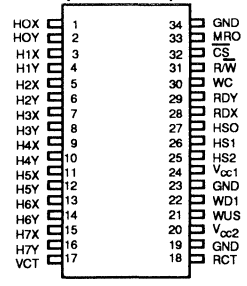
- Dual Power Supplies : +5V
  +12V
- Drive capability of 8 ferrite heads with centre tap
- Write data input, control input level : TTL level
- On–chip write current source
  Current value is controlled by an external resistor
- On–chip write unsafe detector in order to detect abnormal condition on head
- On–chip two systems of power supply monitors with hysteresis to prohibit mis–writing at abnormal voltage
- Read amplifier is low noise and differential voltage gain is 100
- On–chip head damping resistor 750Ω : MB4116, 4126
- A chip is mounted in a small 34–pin SOP package (lead pitch is 1.0mm)
- Pin assignment enables easy mounting
  MB4125, MB4126 pin assignment is reflected reversal image of MB4115, MB4116. This is suitable for mounting several devices on the PCB.
  Head pins are placed at the same side of centre tap voltage output pin (VCT pin)



PLASTIC PACKAGE
FPT–34P–M01 FPT–34P–M02

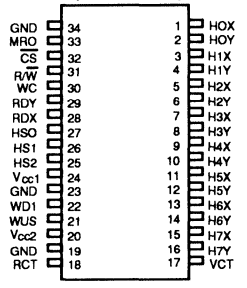
PIN ASSIGNMENT

(TOP VIEW)



MB4115,4116
FPT–34P–M01

(TOP VIEW)



MB4125,4126
FPT–34P–M02

ABSOLUTE MAXIMUM RATINGS (see NOTE) (T_A = 25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC1}	–0.3 to 7.0	V
	V_{CC2}	–0.3 to 15.0	V
	V_{RCT}	–0.3 to 15.0	V
Digital Input Voltage	V_{IN}	–0.3 to V_{CC1} + 0.3	V
Head Input/Output Voltage	V_{HEAD}	–0.3 to V_{CC2} + 0.3	V
WUS pin, Output Voltage	V_{WUS}	–0.3 to 15.0	V
Write Current	I_W	40	mA
Read Output Current	I_{RDO}	–10	mA
Centre Tap Output Current	I_{VCTO}	–40	mA
WUS pin, Output Current	I_{WUO}	+12	mA
Storage Temperature	T_{STG}	–55 to 125	°C
Power Dissipation	P_D	1100 ($T_A \leq 25°C$)	mW

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

6

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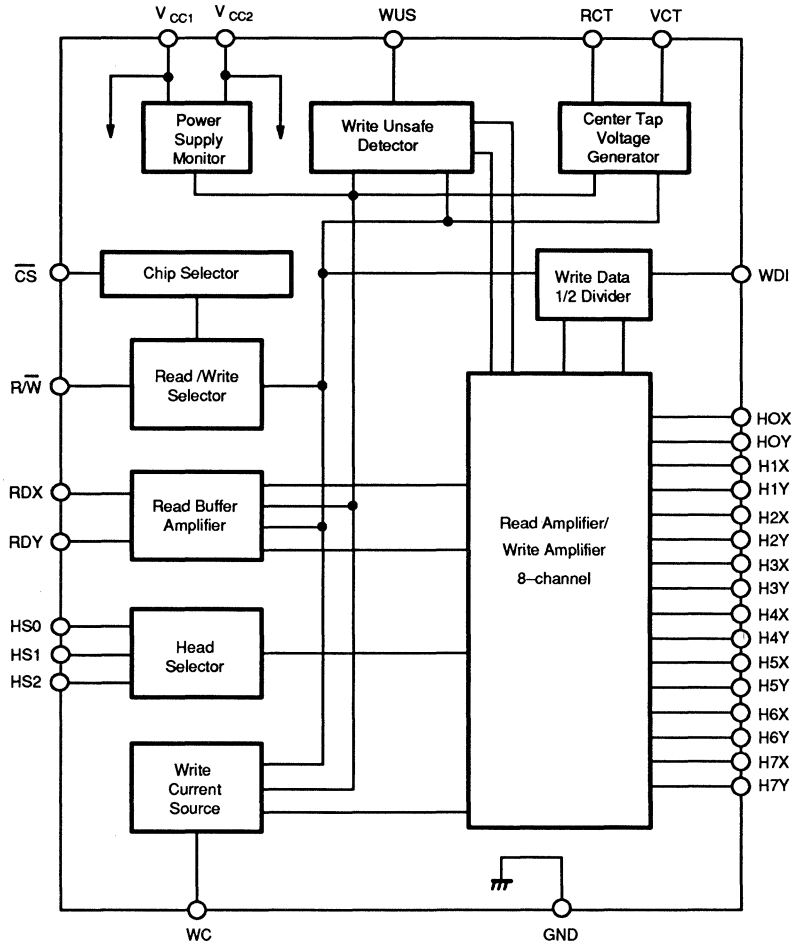
Fig. 1 — BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin Name	Descriptions
1 to 16	HOX to H7X HOY to H7Y	These pins are provided to connect the head from 0–channel to 7–channel
17	VCT	Output pin for head centre tap. Write current flows to head centre tap.
18	RCT	Power suppry pin for centre tap. VCT pin gets the current depending on write current. When this pin is connected with V_{CC2} pin through a resistor 120 Ω (1/2W), power dissipation will be reduced.
19	GND	Sub–ground pin Ground pin for analog circuitry which operats at 12V. This pin is connected with main–ground internally through a writing resistor about 1.5 Ω. The bypass condenser is easily connected between this pin and V_{CC2} pin (20 pin).
20	V_{CC2}	Power suppry voltage, 12V
21	WUS	Output pin for write abnormal detector This pin outputs high level to prevent a disc from mis–writing for each of the following conditions. • Input frequency of write data is zero or very low • VCT pin is open • WC pin is open • Head pins are open • Each head pin is shorted • Head pin and centre tap pin are shorted • Device is in read mode • Operation mode is not selected
22	WDI	Write data input pin Input data is divided by two which drives write circuirty.
23	GND	Sub–ground pin Ground pin for digital circuitry which operates at 5V. This pin is connected with main–ground internally through a writing resistor about 1.5 Ω. The bypass condenser is easily connected between this pin and V_{CC2} pin (24 pin).
24	V_{CC1}	Power supply voltage, 5V
25 26 27	HS2 HS1 HS0	Head selection signal input One of 8–channel becomes actrive condition by combination of these inputs.

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PIN DESCRIPTIONS (Continued)

Pin No.	Pin Name	Descriptions
28 29	RDX RDY	Differential output pin of read amplifier Emitter follower outpuit
30	WC	Write current settng input Write current is controlled by an external resistor R_{WC} connected between this pin and GND pin. Write current is formulated; I_W (A) = $K/R_{WC}(\Omega)$
31	R/$\overline{W}$	Read/Write mode select pin. When this pin is at high level, read mode is selected. When this pin is at low level, write mode is selected.
32	$\overline{CS}$	Chip select input Control signal input pin which selects operating mode or idle mode. When this pin is at high level, device enters idle mode When this pin is at low level, device enters operation mode The device can be applicable for usage with several IC's for this pin.
33	MRO	No connection This pin should be open.
34	GND	Main–ground This pin should be grounded as main–ground. Recommrnded to conect this pin with sub–ground.

6

FUNCTION

Table – 1. Mode selection

Mode	$\overline{CS}$ pin, Voltage	R/$\overline{W}$ pin, Voltage
Idle (I)	H	—
Read (R)	L	H
Write (W)	L	L

Table – 2. Head Selection

$\overline{CS}$ pin, Voltage	HSO pin, Voltage	HS1 pin, Voltage	HS2 pin, Voltage	Selected Head
H	—	—	—	—
L	L	L	L	0
	H	L	L	1
	L	H	L	2
	H	H	L	3
	L	L	H	4
	H	L	H	5
	L	H	H	6
	H	H	H	7

Table – 3. Output table of write abnormal detector

$\overline{CS}$ pin, Voltage	R/$\overline{W}$ pin, Voltage	Mode	Conditions	WUS pin, Output Voltage
H	—	I	Idle mode	H
L	H	R	Read mode	
L	L	W	Write mode	L
L	L	W	Output of the following conditions is occured • WDI pin, input frequency f_{WDI} = OMHz • VCT pin is open • WC pin is open • Head input pins are open • Both ends of head input pins are shorted • Head input pin and VCT pin are shorted	H

Note : H : High level
L : Low level

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC1}	4.5 to 5.5	V
	V_{CC2}	10.8 to 13.2	V
Write Current	I_W	8 to 30	mA
Operating Temperature	T_A	0 to 70	°C

ELECTRICAL CHARACTERISTICS

(V_{CC1} = 5V ±10%, V_{CC2} = 12V±10%, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Condition	Mode*	Value Min	Value Typ	Value Max	Unit
Power Section							
V_{CC1} Power Supply Current	I_{CC1I}	Symbol	I		16	24	mA
	I_{CC1R}		R		14	23	mA
	I_{CC1W}		W		20	30	mA
V_{CC2} Power Supply Current	I_{CC2I}		I		12	22	mA
	I_{CC2R}		R		28	38	mA
	I_{CC2W}		W		12+ I_W	12+ I_W	mA
Power Dissipation	P_{DI}		I		220	400	mW
	P_{DR}		R		410	600	mW
	P_{DWO}	I_W = 30mA	W		600	830	mW
	P_{DWI}	I_W = 30mA, Resistor 120Ω (1/2W) is placed between V_{CC2} pin and RCT pin	W		500	700	mW

***Note** I : Idle
R : Read
W : Write

ELECTRICAL CHARACTERISTICS (Continued)

(V_{CC1} = 5V ±10%, V_{CC2} = 12V±10%, T_A = 25 °C, unless otherwise noted.)

Parameter	Symbol	Condition	Value				Unit
			Mode	Min	Typ	Max	
Power Supply Monitor Section							
V_{CC1} Detection Voltage	V_{TH1}	When V_{CC1} is falling	R/W	3.45	3.90	4.30	V
		When V_{CC1} is rising	R/W	3.55	4.10	4.46	V
V_{CC1} Detection Voltage Hysteresis Width	ΔV_{TH1}		R/W		0.2		V
V_{CC2} Detection Voltage	V_{TH2}	When V_{CC2} is falling	R/W	7.50	8.80	10.10	V
		When V_{CC2} is rising	R/W	7.90	9.30	10.50	V
V_{CC2} Detection Voltage Hysteresis Width	ΔV_{TH2}		R/W		0.5		V
Head Input Current	I_{WOF1}	$0 < V_{CC1} \leq 5.5V$ $0 < V_{CC2} \leq 13.2V$	I/R	–100		100	µA
	I_{WOF2}	$0 < V_{CC1} < 3.45V$ $0 < V_{CC2} < 7.50V$	W	–100		100	µA
Digital Section							
High-level Input Voltage	V_{IH}	T_A = 0 to 70°C		2.0		V_{CC1} +0.3	V
High-level Input Current	I_{IH}	V_{IH} = 2.0V				100	µA
Low-level Input Voltage	V_{IH}	T_A = 0 to 70°C		–0.3		0.8	V
Low-level Input Current	I_{IL}	V_{IL} = 0.8V		–400			µA
Read/Write Transition Time	t_{RW}	Read to Write				600	ns
Write/Read Transition Time	t_{WR}	Write to Read				600	ns
Chip Selection Transition Time	t_{IR} t_{IW}	Idle to Read Idle to Write				1000	ns
Head Selection Delay Time	t_{dH}					1000	ns

Notes : I : Idle
R : Read
W : Write

6

ELECTRICAL CHARACTERISTICS (Continued)

(V_{CC1} = 5V ±10%, V_{CC2} = 12V±10%, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Read Section						
Differential Voltage Gain	G_D	V_{IN} = 1m V_{p-p} f_{IN} = 300kHz R_L = 1kΩ	80	100	120	V/V
Frequency Bandwidth	BW	–3dB V_{IN} = 1m V_{p-p} R_L = 1kΩ	30	50		MHz
Input Equivalent Noise	V_N	BW = 1MHz to 10MHz		1.4	2.0	nV $\sqrt{Hz}$
Input Capacitance	C_I	f_{IN} = 5MHz R_L = 1kΩ		16	23	pF
Dynamic Range	D	f_{IN} = 5MHz 3rd Harmonic wave : – 30dB	6			mV
Input Bias Current	I_{HR}			12	45	μA
Common mode Output Voltage	V_{RDX} V_{RDY}	Head input pins are shorted with VCT pin	5.0	6.0	7.0	V
Output Offset Voltage	V_{OFF}	Head input pins are shorted with VCT pin	–400		400	mV
Common mode Rejection Ratio	CMRR	f_{IN} = 5MHz V_{IN} = 100m V_{p-p}	50	65		dB
Power Supply Rejection Ratio	PSRR	f_{IN} = 5MHz V_{IN} = 100m V_{p-p}	45	70		dB
Channel Separation	CSP	f_{IN} = 5MHz V_{IN} = 100m V_{p-p}	45	55		dB
Differential Input Resistance	R_I	f_{IN} = 5MHz, MB4115	2			kΩ
		f_{IN} = 5MHz, MB4116	0.4			kΩ
Single-end Output Resistance	R_O	f_{IN} = 5MHz		18	50	Ω

6

ELECTRICAL CHARACTERISTICS (Continued)

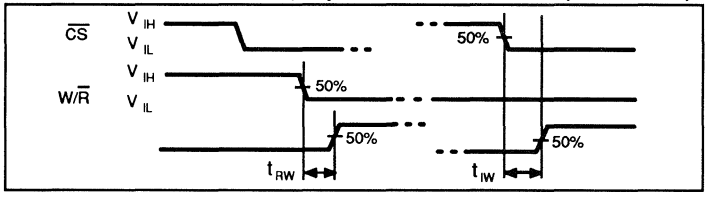
(V_{CC1} = 5V ±10%, V_{CC2} = 12V±10%, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Read Section						
Write Current Constant	K	I_W = 12mA	112	120	128	V
Write Current Transition Time	t_r t_f	L = 0μH I_W = 30mA			25	ns
Write Current Delay Time	tpd1 tpd2	L = 0μH I_W = 30mA			30	ns
Write Current Differential Delay Time	Δ tpd	L = 0μH I_W = 30mA Δtpd = | tpd1–tpd2 |			2	ns
Output Voltage Amplitude	ΔV_H		5.7			V
Damping Resistance	R_D	MB4125	525	750	975	Ω
		MB4126				
Write Abnormal Detector Section						
WUS pin, Output Voltage	V_{USL}	I_W = 10mA, R_D = 750Ω f_{WDI} = 2.5MHz, L = 10 μH		0.1	0.5	V
WUS pin, Output Voltage	I_{OH}	L = 10 μH, R_D = 750Ω I_W = 30mA, V_{OH} = 5.0V		0.1	100	μA
Write Unsafe Delay Time 1	t_{dSF}	Unsafe to Safe L = 10 μH I_W = 8mA, R_D = 750Ω F_{WDI} = 0 to 2.0MHz		0.06	1.00	μs
Write Unsafe Delay Time 2	t_{dUS}	Safe to Unsafe L = 10μH I_W = 30mA, R_D = 750Ω f_{WDI} = 5 to OMHz		5	8	μs

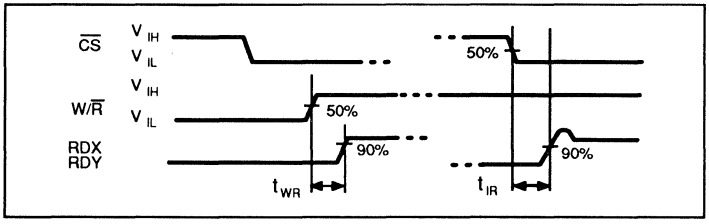
6

TIMING CHART

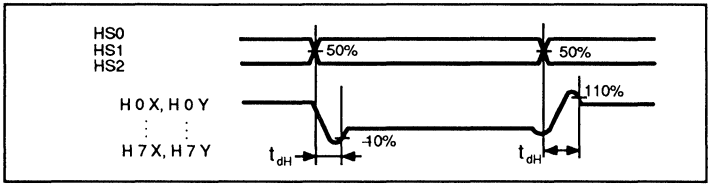
1. Read/Write Transition Time ,Chip Select Transition Time (Idle to Write)



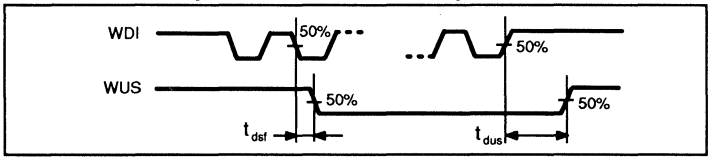
2. Write/Read transition Time, Chip Select Transition Time (Idle Write)



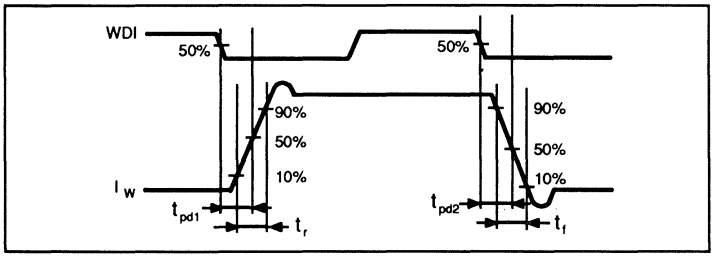
3. Head Select Transition Time



4. Wite Unsafe Delay Time 1, Write Unsafe Delay Time 2



5. Write Current Transition Time, Write Current Delay Time



6

APPLICATION

(1) Treatment of GND pin

It's recommended to ground three ground pins with common ground.If it is imposasible, please connect main–groundwith ground at least.

(2) Reduse power dissipation

When an external resistor 120 Ω (1/2W) is placed between RCT pin and V_{CC2} pin, power dissipation is reduced shown below.

Reduced power $P = I_W^2 \times 120$ (w)

(3) Setting write current

Write current I_W is set by an external resistor R_{WC}. Write current is formulated;

$I_W = K / R_{WC}$ (A) (Ajustable current range is 8 to 30mA)

External resistor shourld be located near IC.

(4) Damping resistor

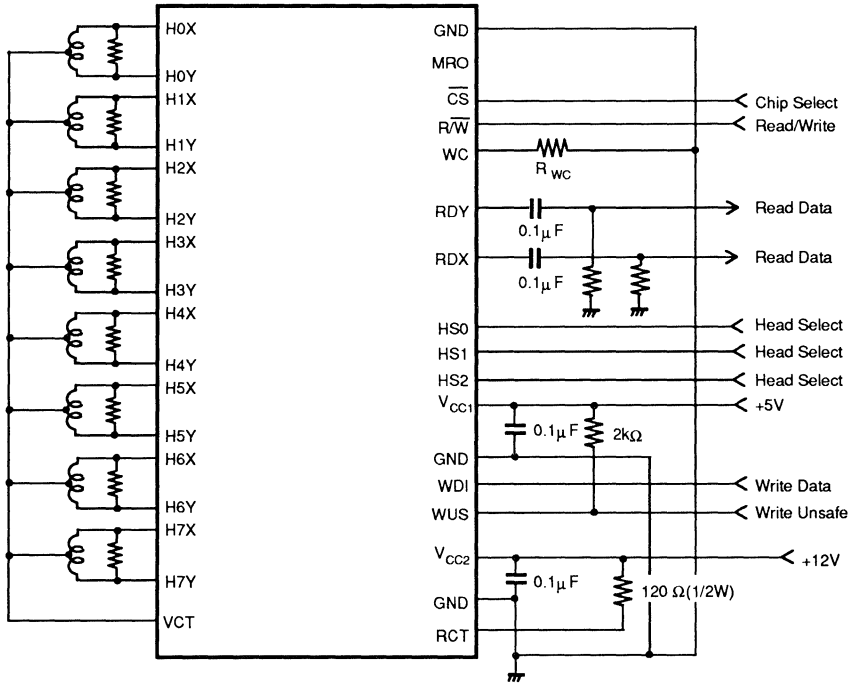
The device is intended to be used a head which has inductance of 5 to 15 μH.

Thus, please use the damping resistor between 500 to 2k Ω.

Also, write current and impedance should be meet the following formula.

I_W (mA) x L(μH) ≥ 200

Fig. 2 – APPLICATION EXAMPLE



6

INPUT/OUTPUT CIRCUIT CONFIGURATION

FIG.3 – $\overline{CS}$ pin , R/$\overline{W}$ pin , HSO to HS2 pins

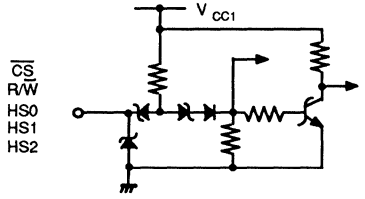


FIG. 4 – RCT pin , VCT pin

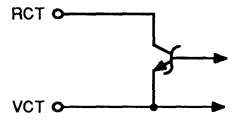


FIG. 5 – WC pin

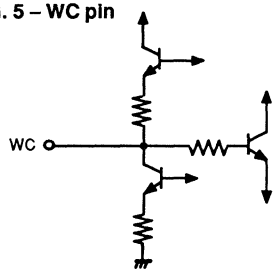


FIG. 6 – WUS pin

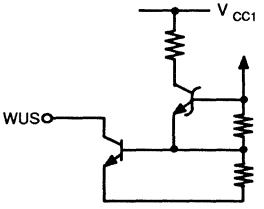


FIG. 7 – WDI pin

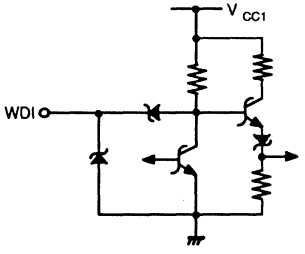


FIG. 8 – RDX pin , RDY pin

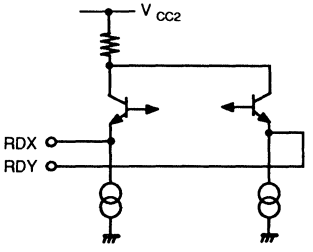
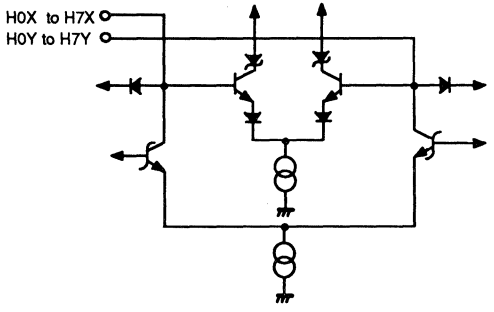


FIG. 9 – H0X to H7X pins, H0Y to H7Y pins



6

TYPICAL CHARACTERISTICS CURVES

Fig.10 – WRITE CURRENTE vs. POWER SUPPLR VOLTAGE

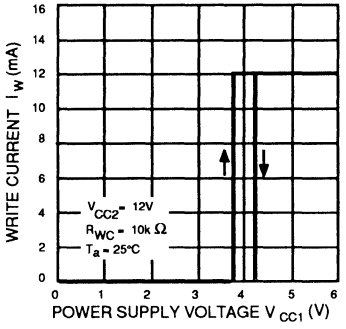


Fig.11 – WRITE CURRENTE vs. POWER SUPPLR VOLTAGE

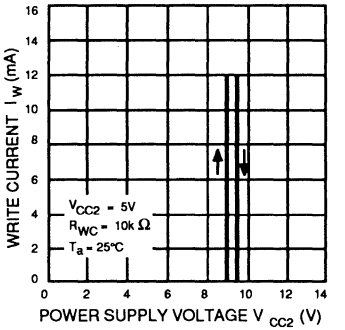


Fig.12 – WRITE CURRENTE CONSTANT vs. POWER SUPPLR VOLTAGE

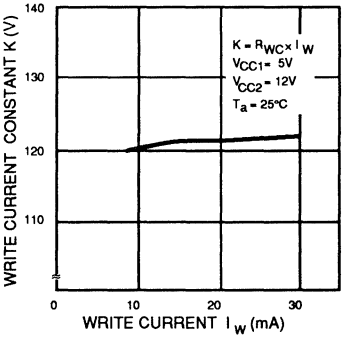


Fig.13 – WRITE CURRENTE vs. WRITE CURRENTE SETTING RESISOR

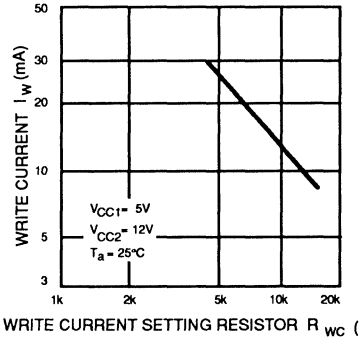


Fig.14 – WRITE CURRENTE CONSTANT vs. TEMPERATURE

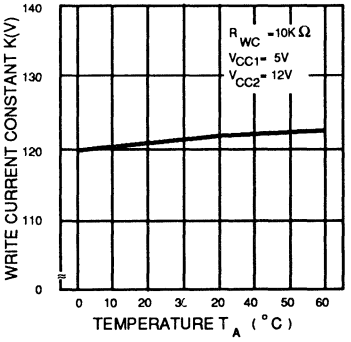
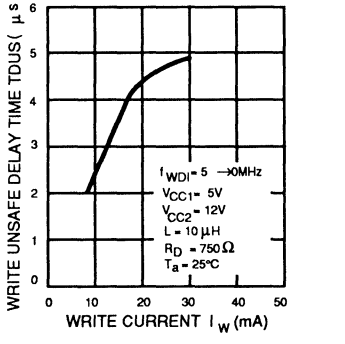


Fig.15 – WRITE UNSAFE DELAY TIME vs. WRITE CURRENTE



6

TYPICAL CHARACTERISTICS CURVES (Continued)

Fig.16 – READ OUTPUT VOLTAGE vs. READ INPUT VOLTAGE

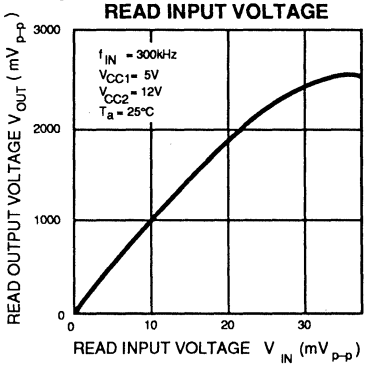


Fig.17 – DIFFERENTIAL VOLTAGE GAIN vs. TEMPERATURE

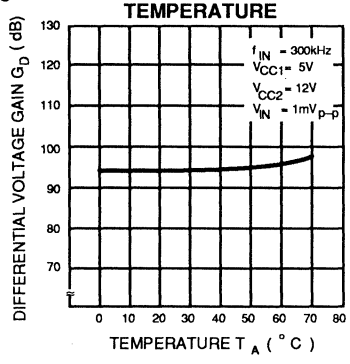


Fig.18 – DIFFERENTIAL VOLTAGE GAIN vs. FREQUENCY

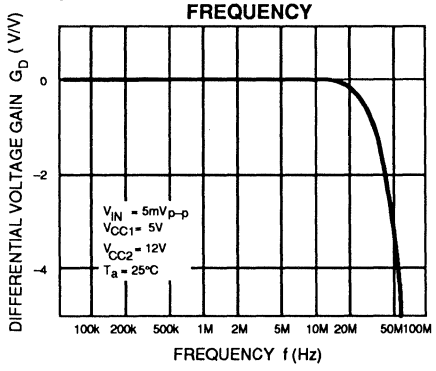
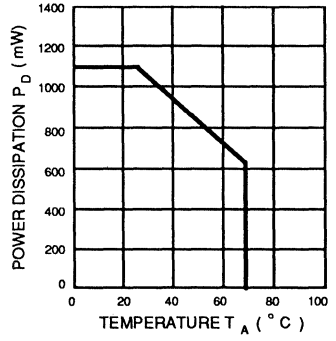
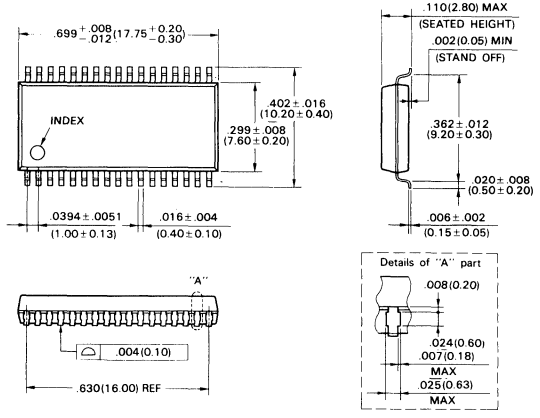


Fig.19 – POWER DERATING CURVE



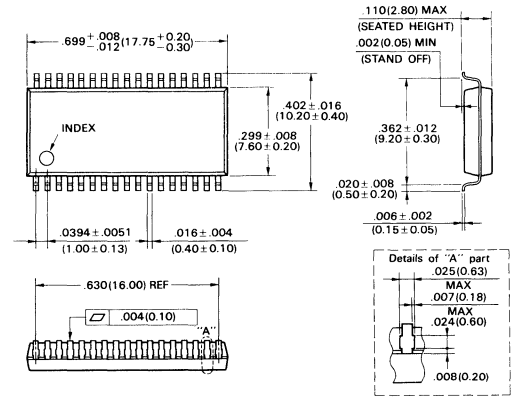
PACKAGE DIMENSIONS

34–LEAD PLASTIC FLAT PACKAGE
(Case No.: FPT–34P–M01)



Dimensions in inches (millimeters)

34–LEAD PLASTIC FLAT PACKAGE
(Case No.: FPT–34P–M02)



Dimensions in inches (millimeters)

FUJITSU

MAGNETIC DISK HEAD AMPLIFIER

MB 4117-4
MB 4117-6
MB 4118-4
MB 4118-6

March 1987
Edition 2.0

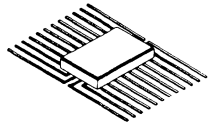
MAGNETIC DISK HEAD AMPLIFIER

The Fujitsu MB 4117-4 and MB 4118-4 are magnetic disk head amplifiers with Zener-zapped write current sourse for 4-channel head, MB 4117-6 and MB 4118-6 for 6-channel.

Their logic interface level is TTL level and their packages are suitable for mounting directly on the arm of movable disk head.

MB 4118 has on-chip dumping resistors for each channel.

- Four major functions to interface with magnetic heads: Write Amplifier/Read Amplifier/$\overline{RAS}$ (safety)/Selection Decode
- Three modes: Read/Write/Idel
- Power Supply Voltage: +5 V and +12 V
- Logic interface level: TTL compatible
- On-chip Zener-zapped write current source.
  Its current can be adjustable with external resistor.
- On-chip dumping resistors (MB 4118 only)



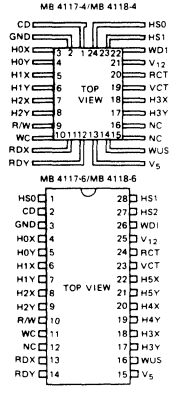
(MB 4117-4/MB 4118-4)
CERAMIC PACKAGE
FPT-24C-F01

DIP-22P-M03: See Page 8
FPT-24P-M02: See Page 9

(MB 4117-6/MB 4118-6)
PLASTIC PACKAGE
DIP-28P-M02

FPT-28C-A01: See Page 11

PIN ASSIGNMENT



DIP-22P-M03: See Page 8
FPT-24P-M02: See Page 9
FPT-28C-A01: See Page 11

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

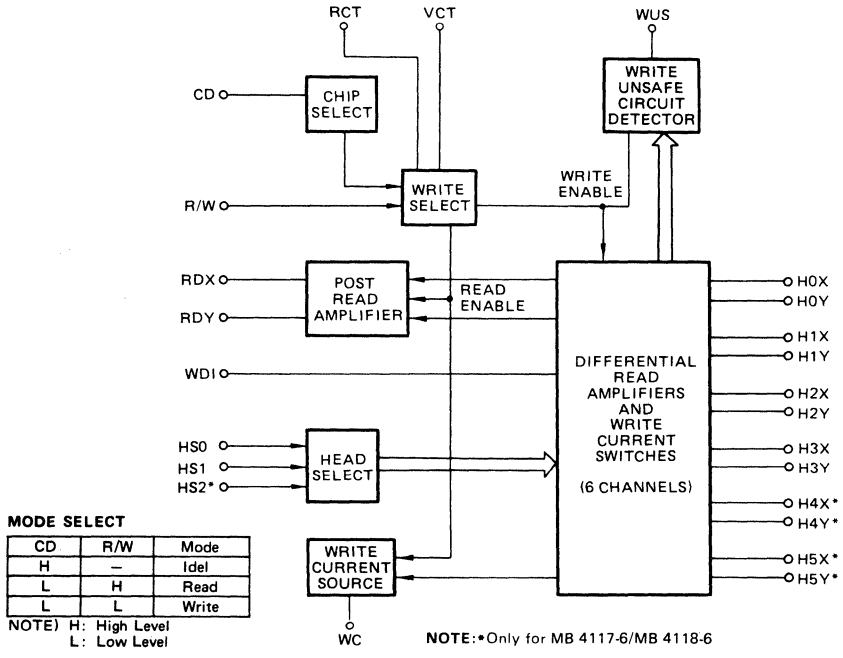
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{12}	14.0	V
Supply Voltage	V_5	6.0	V
Operating Ambient Temperature	T_A	0 to +70	°C
Storage Temperature	T_{STG}	−65 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6

Fig. 1 – BLOCK DIAGRAM OF MB 4117/MB 4118



MODE SELECT

CD	R/W	Mode
H	–	Idel
L	H	Read
L	L	Write

NOTE) H: High Level
L: Low Level

NOTE: *Only for MB 4117-6/MB 4118-6

HEAD SELECTION TABLE FOR MB 4117-4/MB 4118-4

Head No.	HS0	HS1
0	Low	Low
1	High	Low
2	Low	High
3	High	High

HEAD SELECTION TABLE FOR MB 4117-6/MB 4118-6

Head No.	HS0	HS1	HS2
0	Low	Low	Low
1	High	Low	Low
2	Low	High	Low
3	High	High	Low
4	Low	Low	High
5	High	Low	High

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage (Read/Write/Idel)	V_{12}	10.8	12.0	13.2	V
Supply Voltage (Read/Write/Idel)	V_5	4.75	5.0	5.25	V
High-level Input Voltage	V_{IH}	2.0		V_5+0.3	V
Low-level Input Voltage	V_{IL}	-0.3		0.8	V

DC CHARACTERISTICS

(Recommended operating condition unless otherwise noted.)

Parameter	Symbol	Condition	Value				Unit
			Mode*	Min	Typ	Max	
Power Supply Current	I_{5I}		I	–	17	28	mA
	I_{12I}		I	–	17	28	
	I_{5R}		R	–	14	25	
	I_{12R}		R	–	34	50	
	I_{5W}		W	–	20	30	
	I_{12W}		W	–	20+I_W	30+I_W	
CD Input Current	I_{CDH}	V_{CD} = 2.0 V	I	–	–	0.1	mA
	I_{CDL}	V_{CD} = 0.8 V	R/W	-0.4	-0.2	–	
R/W Input Current	$I_{R/WH}$	$V_{R/W}$ = 2.0 V	I/R	–	–	0.1	mA
	$I_{R/WL}$	$V_{R/W}$ = 0.8 V	I/W	-0.4	-0.2	–	
HS Input Current	I_{HSH}	$V_{HS0,HS0,(HS2)}$ = 2.0 V	I/R/W	–	–	0.1	mA
	I_{HSL}	$V_{HS0,HS1,(HS2)}$ = 0.8 V	I/R/W	-0.4	-0.2	–	
WDI Input Current	I_{WDIH}	V_{WDI} = 2.0 V	I/R/W	–	–	0.1	mA
	I_{WDIL}	V_{WDI} = 0.8 V	I/R/W	-0.4	-0.2	–	
HEAD Input Current	I_{HI}	V_{CD} = 2.0 V	I	–	–	0.1	mA
	I_{HR}	$V_{R/W}$ = 2.0 V	R	–	25	45	μA

NOTE: *I: Idle, R: Read, W: Write

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READ MODE

(Recommended operating condition unless otherwise noted.)

Parameter	Symbol	Condition		Value			Unit
				Min	Typ	Max	
Differential Voltage Gain	A_V	V_{IN} = 1 mV_{PP}, f = 300 kHz R_L = 1 kΩ		80	100	120	V/V
Band Width	B_W	V_{IN} = 1 mV_{PP}, R_L = 1 kΩ (–3 dB)		30	–	–	MHz
Input Noise Voltage	V_n	T_A = 25°C, B_W = 1 to 10 MHz		–	–	5.4	μV_{rms}
Input Capacitance	C_I	f = 5 MHz		–	–	23	pF
Differential Input Registance	R_D		MB 4117	2	–	–	kΩ
			MB 4118	525	750	975	Ω
Single-End Output Registance	R_O	f = 5 MHz		–	–	100	Ω
R_{DX}, R_{DY} Output Voltage	V_{RDX}			5.0	–	7.0	V
	V_{RDY}						
Output Offset Voltage	V_{OFF}			–480	–	+480	mV
Dynamic Range	D	f = 5 MHz		6	–	–	mV_{PP}
Common Mode Rejection Ratio	CMRR	f = 5 MHz, V_{IN} = 100 mV_{PP}		50	–	–	dB
Channel Separation	CSP	f = 300 kHz, V_{IN} = 1 mV_{PP}		45	–	–	dB
Power Supply Rejection Ratio	PSRR1	f = 5 MHz, V_5 = 100 mV_{PP}		45	–	–	dB
	PSRR2	f = 5 MHz, V_{12} = 100 mV_{PP}		45	–	–	dB

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WRITE MODE

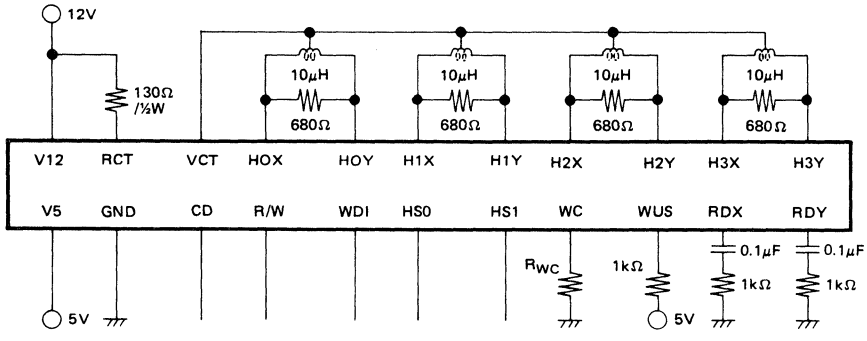
(Recommended operating condition unless otherwise noted.)

Parameter	Symbol	Condition		Value			Unit
				Min	Typ	Max	
Write Current	I_W		Plastic	8		30	mA
			Ceramic	8		50	
Write Current Constant	K*	I_W = 18 mA, K = $I_W \times R_{WC}$		128	140	152	V
Head Differential Voltage	V_{DIF}	L = 10 μH, I_W = 45 mA		6	8		V
Write Unsafe Switching Output Voltage	V_{USL}	L = 10 μH, I_W = 8 mA f_{WDI} = 2.5 MHz, I_{US} = 8 mA				0.5	V
Write Current Transition Time	t_r t_f	L = 0 μH, I_W = 45 mA				20	ns
Write Unsafe Switching Delay Time	t_{US}	L = 10 μH, I_W = 50 mA f_{WDI} = 5.0 MHz to 0 MHz		1.0		8.0	μs

NOTE: *K = $I_W \times R_{WC}$ (External resistor setting write current.)

6

Fig. 2 – MEASUREMENT CIRCUIT (MB 4117-4)



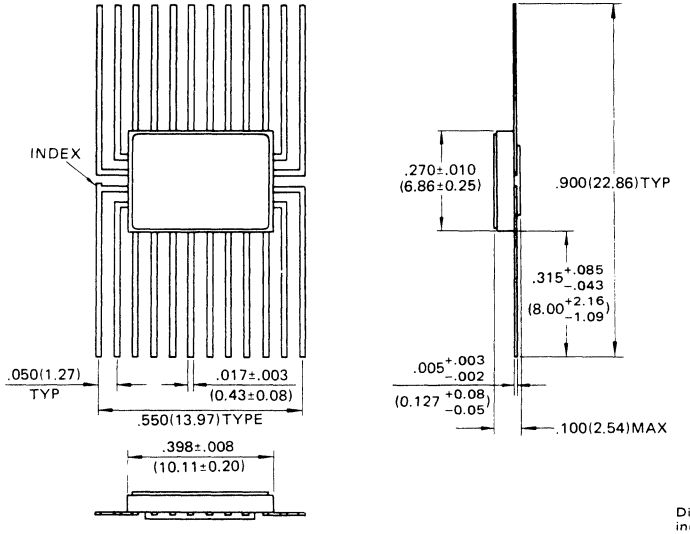
6

MEASUREMENT CONDITIONS

Parameter	Symbol	Condition		Value	Unit
Power Supply Voltage	V_{12}	Read/Write/Idle mode		12 ± 0.24	V
	V_5			5 ± 0.1	
Inductance of Magnetic Head	L_H	Read/Write mode	DC	0	μH
			AC	10	
CD Voltage	V_{CD}	Read/Write mode		0.2 ± 0.2	V
		Idle mode		3.3 to 5.0	
R/W Voltage	$V_{R/W}$	Write/Idle mode		0.2 ± 0.2	V
		Read/Idle mode		3.3 to 5.0	
HS Voltage	V_{HS0}	Read/Write/Idle mode		0.2 ± 0.2	V
	$V_{HS1/(HS2)}$			3.3 to 5.0	
WDI Voltage	V_{WDI}	Read/Write/Idle mode		0.2 ± 0.2	V
				3.3 to 5.0	
Ambient Temperature	T_A	Read/Write/Idle mode		25 ± 2.0	°C

PACKAGE DIMENSIONS (MB 4117-4/MB 4118-4)

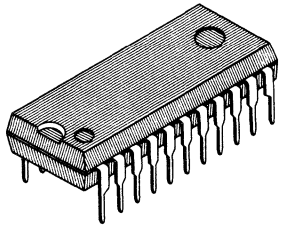
24-PAD CERAMIC (FRIT SEAL) FLAT PACKAGE
(CASE No. : FPT-24C-F01)



Dimensions in
inches (millimeters)

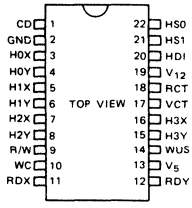
6

PACKAGE DIMENSIONS (MB 4117-4/MB 4118-4)

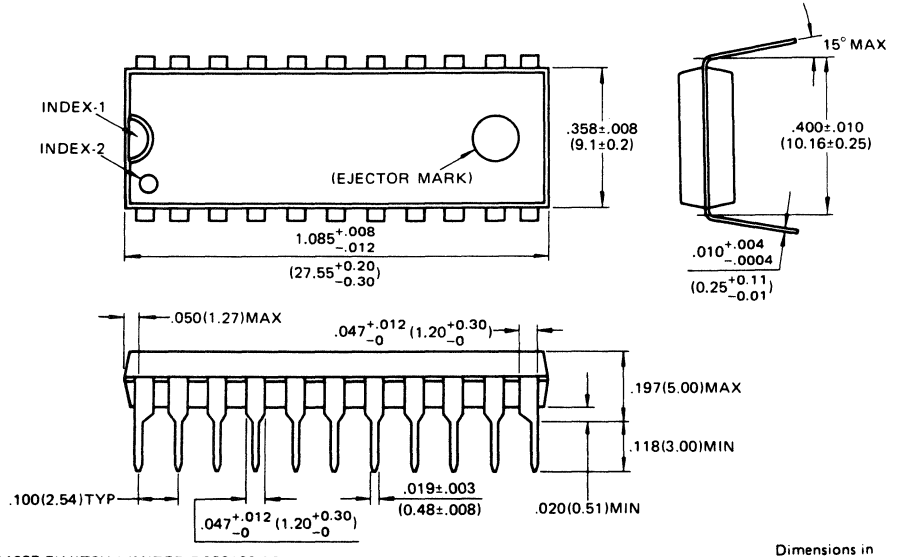


DIP-22P-M03

PIN ASSIGNMENT

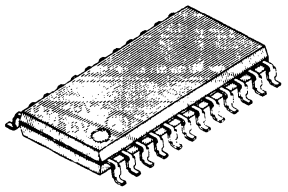


22-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-22P-M03)



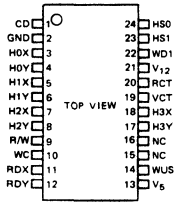
Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (MB 4117-4/MB 4118-4)

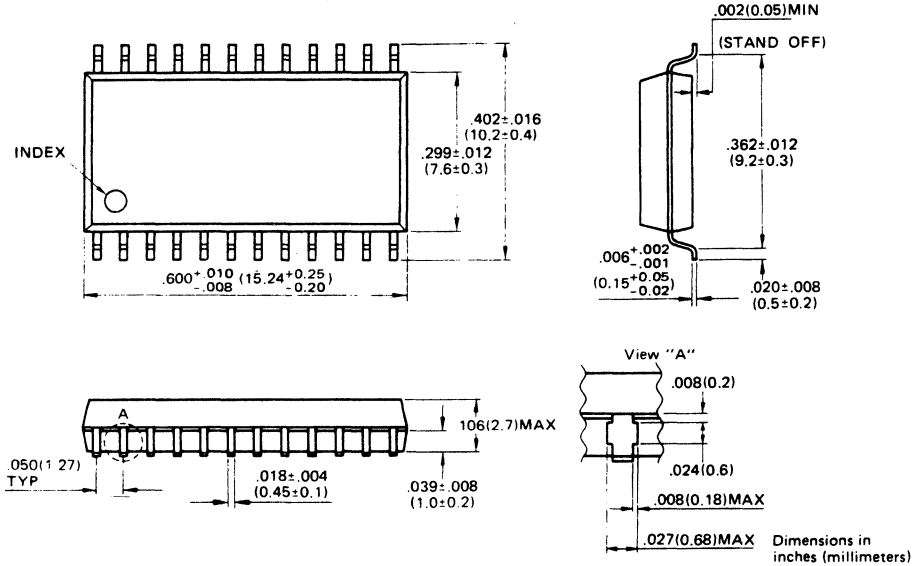


FPT-24P-M02

PIN ASSIGNMENT

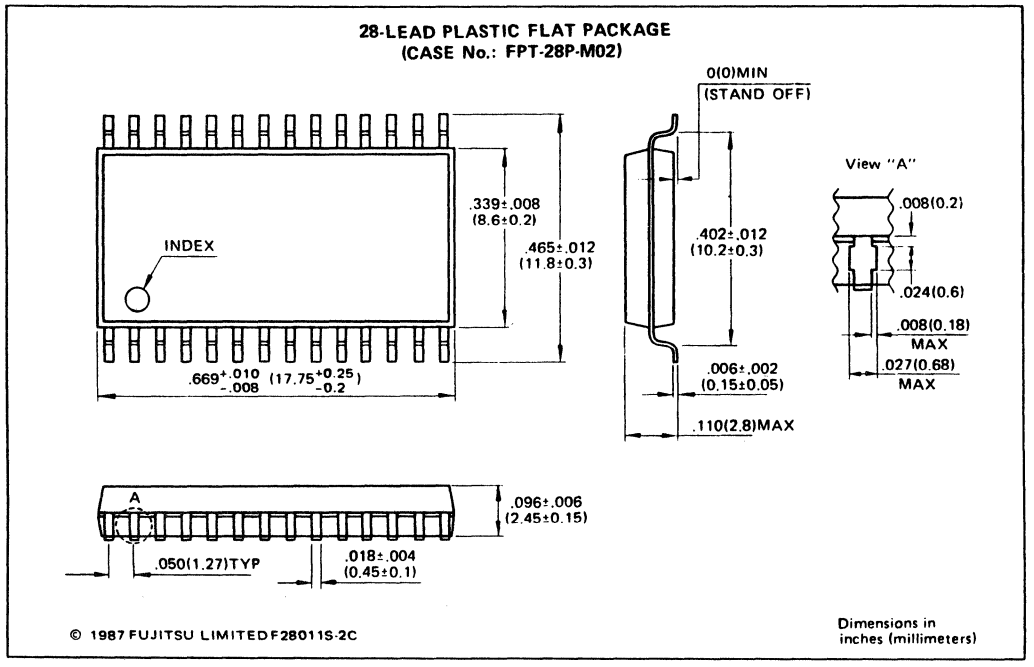


24-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-24P-M02)



6

PACKAGE DIMENSIONS (MB 4117-6/MB 4118-6)



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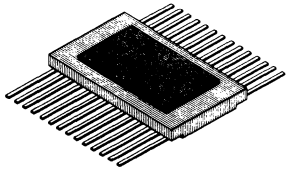
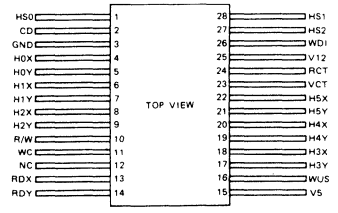
PACKAGE DIMENSIONS (MB 4117-6/MB 4118-6)

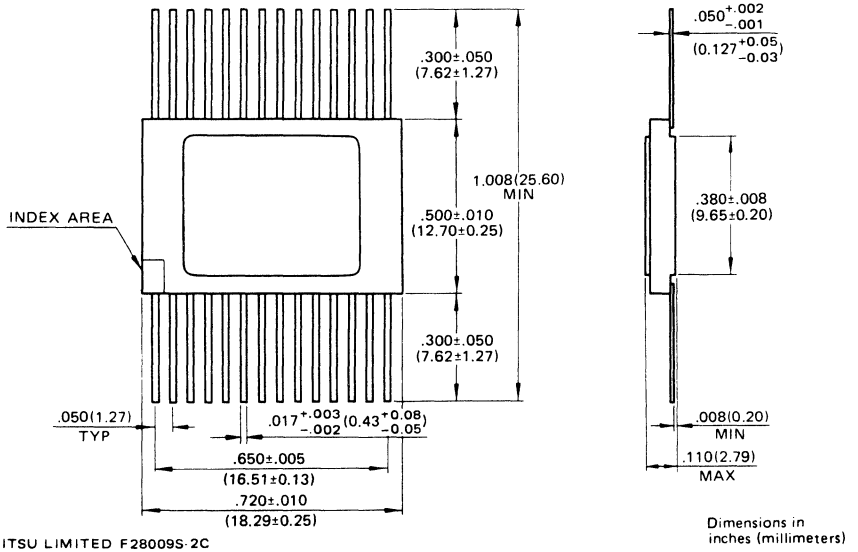


FPT-28C-A01

PIN ASSIGNMENT



28-LEAD CERAMIC (FRIT SEAL) FLAT PACKAGE
(CASE No.: FPT-28C-A01)



Dimensions in
inches (millimeters)

6

April 1990
Edition 1.0

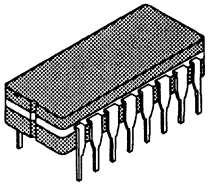
FUJITSU

PRODUCT PROFILE

MB4313
Read/Write Bus Driver/Receiver

DESCRIPTION

The Fujitsu MB4313 is designed as a driver/receiver to be used as an interface between a magnetic disk drive and a control unit. The MB4313 transfers the read-out signal from the disk head to the control unit, and the write signal from the control unit to the disk head.



DIP-16C-C02

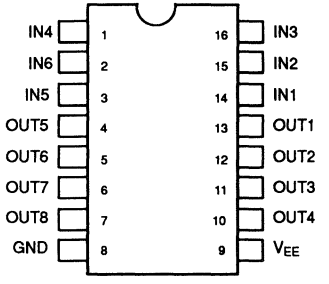
FEATURES

- ECL compatible input signals
- Propagation delay time 12 ns maximum
- Rise/Fall time 8 ns maximum
- Single –5.2 V supply

RECOMMENDED OPERATING CONDITIONS

Parameter	Conditions	Symbol	Value			Unit
			Min.	Typ.	Max.	
Input Voltage Pins 1,3,14,16	T_A=0°C	V_{IN}	–1.87		–0.86	V
	T_A=25°C		–0.85		–0.81	V
	T_A=70°C		–1.825		–0.7	V
Input Current Pins 2,15		I_{IN}			13	mA
Output Current Pins 4,5,12,13		I_{OUT}			5	mA
Supply Voltage		V_{EE}	–5.46	–5.2	–4.94	V
Operating Temperature		T_A	0		+70	°C

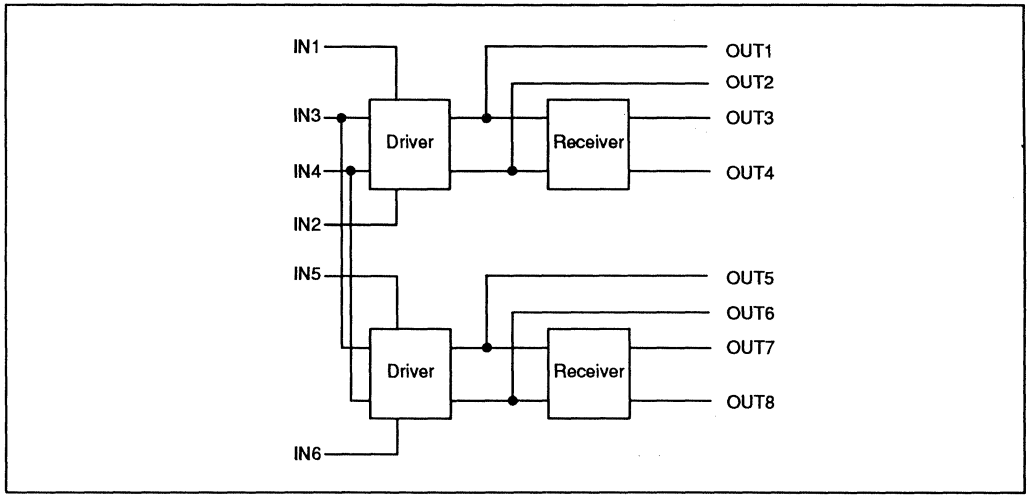
Pin Assignment
(Top View)



Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

(V_{EE} = −5.2V±5% at T_A = 0 to 70 °C, unless otherwise noted.)

DC CHARACTERISTICS

(Deviation : ± 2%)

Parameter	Conditions	Symbol	Value at T_A = 25±2°C			Value at T_A = 0 to 70°C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Voltage	$V_{IN1}=V_{IN5}=V_{Hmin}$, $V_{IN3}=V_{Hmax}$, $V_{in4}=V_{Hmin}$	V_{01H}				−10			mV
		V_{05H}				−10			mV
		V_{03H}		−0.8		−1.0		−0.6	V
		V_{07H}		−0.8		−1.0		−0.6	V
	$V_{IN1}=V_{IN5}=V_{Hmin}$, $V_{IN3}=V_{Lmin}$, $V_{in4}=V_{Hmax}$	V_{02H}				−10			mV
		V_{06H}				−10			mV
		V_{04H}		−0.8		−1.0		−0.6	V
		V_{08H}		−0.8		−1.0		−0.6	V
	$V_{IN1}=V_{IN4}=V_{Lmax}$, $V_{IN5}=V_{IN3}=V_{Hmin}$	V_{01L}		−0.51		−0.7		−0.4	V
		V_{03L}		−1.32		−1.6		−1.0	V
	$V_{IN1}=V_{IN3}=V_{Lmax}$, $V_{IN5}=V_{IN4}=V_{Hmin}$	V_{02L}		−0.51		−0.7		−0.4	V
		V_{04L}		−1.32		−1.6		−1.0	V
	$V_{IN1}=V_{IN3}=V_{Hmin}$, $V_{IN5}=V_{IN4}=V_{Lmax}$	V_{05L}		−0.51		−0.7		−0.4	V
		V_{07L}		−1.32		−1.6		−1.0	V
	$V_{IN1}=V_{IN4}=V_{Hmax}$, $V_{in5}=V_{IN3}=V_{Lmax}$	V_{06L}		−0.51		−0.7		−0.4	V
		V_{08L}		−1.32		−1.6		−1.0	V

DC CHARACTERISTICS (Continued)

Parameter	Conditions	Symbol	Value at T_A = 25±2°C			Value at T_A = 0 to 70°C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Current	$V_{IN1}=V_{Hmax}$	I_{IN1}		20				100	µA
Input Current	$V_{IN5}=V_{Hmax}$	I_{IN5}		20				100	µA
	$V_{IN3}=V_{Hmax}$, $V_{IN1}=V_{IN4}=V_{Lmin}$	I_{IN3}		20				400	µA
	$V_{IN4}=V_{Hmax}$ $V_{IN1}=V_{IN4}=V_{Lmin}$	I_{IN4}		20				400	µA
	R=430Ω±2%	I_{IN2}, I_{IN6}		10.1		8.5		12.1	mA
Supply Current	$V_{IN1}=V_{IN5}=V_{Hmax}$, $V_{IN3}=V_{Hmax}$, $V_{IN4}=V_{Lmax}$	I_{EE}		72				110	mA

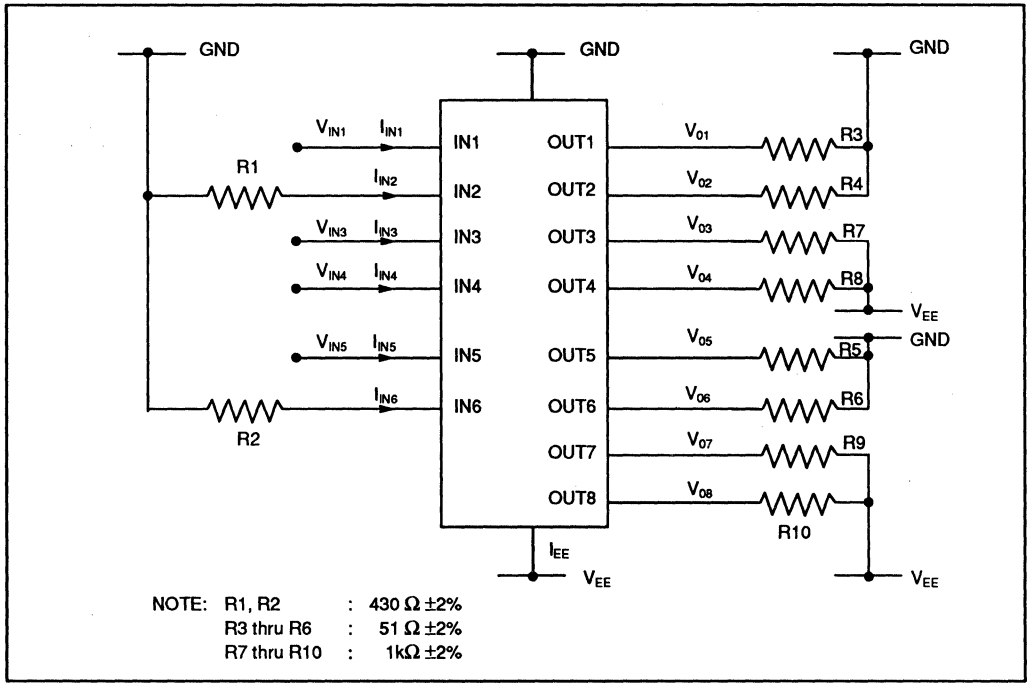
AC CHARACTERISTICS

(Deviation : ± 2%)

Parameter	Conditions	Symbol	Value at T_A = 25±2°C			Value at T_A = 0 to 70°C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time	$V_{IN1}=V_{IN5}=5_{Lmax}$, $V_{IN3}=-1.29V$, $V_{IN4}=V_{INA}$, Output Timing: $V_{02}, V_{04}, V_{06}, V_{08}$ as V_{OUTC}. $V_{01}, V_{03}, V_{05}, V_{07}$ as V_{OUTC}.	t_{d1}						12	ns
		t_{d2}						12	ns
		t_{d3}						12	ns
		t_{d4}						12	ns
Rise Time		t_{r1}						8	ns
		t_{r2}						8	ns
Fall Time		t_{f1}						8	ns
		t_{f2}						8	ns

6

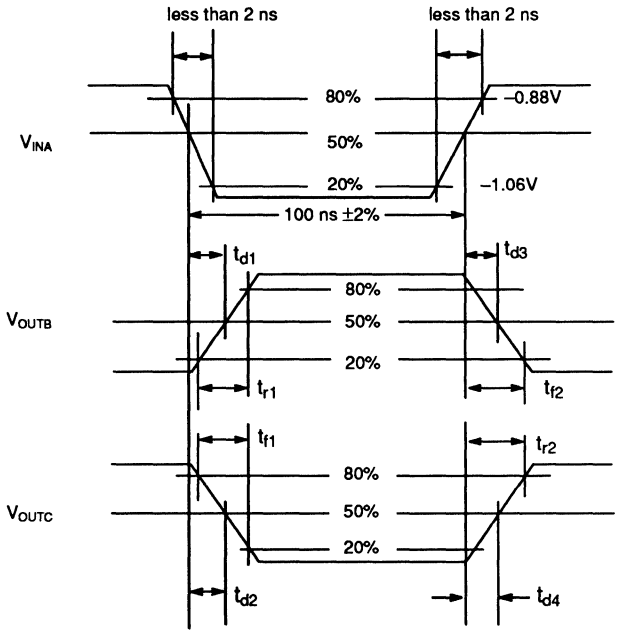
Test Circuit Example



NOTE: R1, R2 : 430 Ω ±2%
R3 thru R6 : 51 Ω ±2%
R7 thru R10 : 1kΩ ±2%

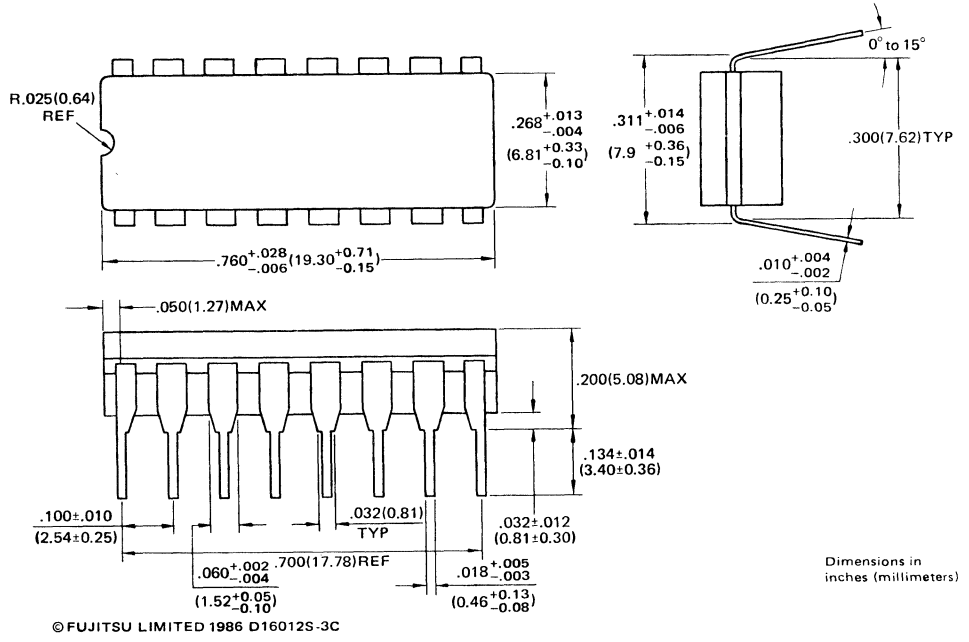
Test Temperature	Test Voltage				
T_A (°C)	V_{Hmax} (V)	V_{Hmin} (V)	V_{Lmax} (V)	V_{Lmin} (V)	V_{TH} (V)
0	–0.86	–1.155	–1.49	–1.87	–1.32
25	–0.81	–1.105	–1.475	–1.85	–1.29
70	–0.7	–1.035	–1.44	–1.825	–1.22

TIMING CHART



PACKAGE DIMENSIONS

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(DIP-16C-C02)



FUJITSU

DRIVER/RECEIVER FOR DISK HEAD AMPLIFIER

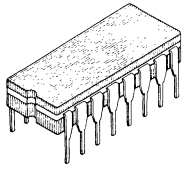
MB4316

December 1987
Edition 1.0

DRIVER/RECEIVER FOR DISK HEAD AMPLIFIER

The Fujitsu MB4316 is a driver/receiver designed for the MB4111/MB4112/MB4113 Disk Head Amplifier.

- Data inputs and Control inputs are CML level inputs.
- On-chip Write Current Source is adjustable by changing an external resistor.
- Bandwidth of Read Amplifier: 30 MHz min.
- 16-pin Ceramic DIP Package (Suffix: -Z)



CERAMIC PACKAGE
DIP-16C-C02

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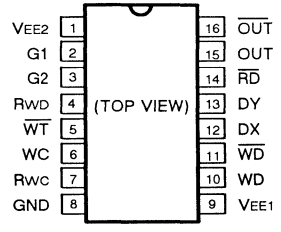
PIN ASSIGNMENT



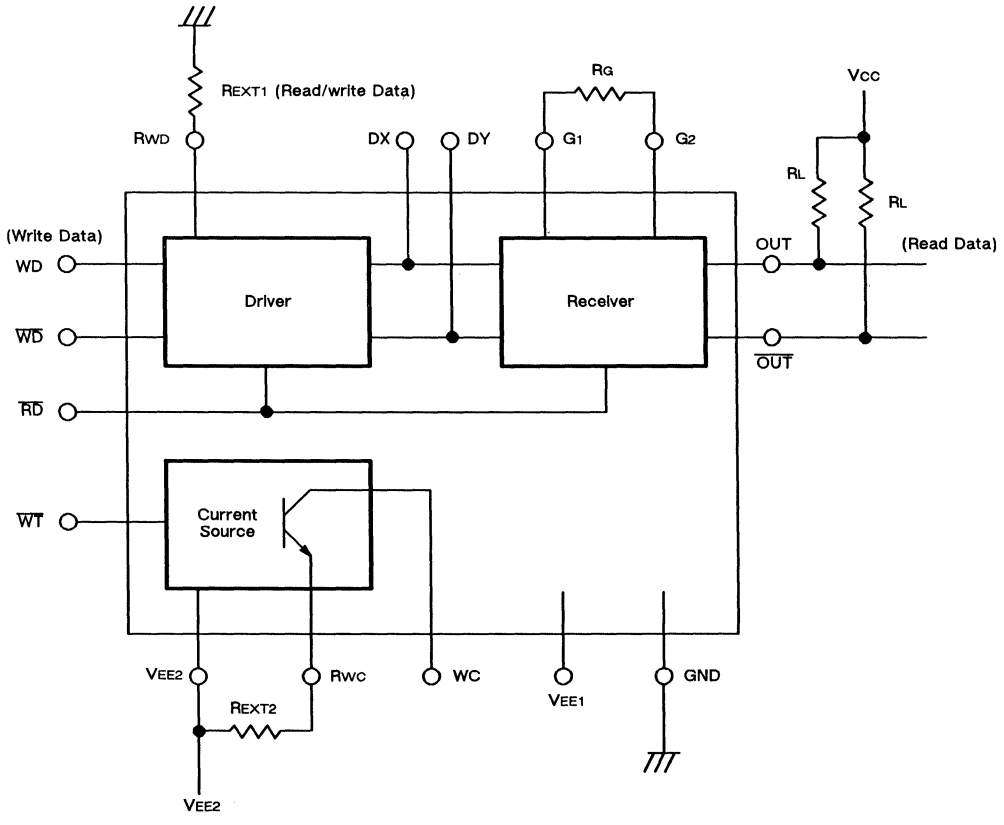
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{EE1}	-7.0 to 0	V
	V_{EE2}	-15.0 to 0	V
Output terminal voltage	V_{CC}	0 to 9.0	V
Input voltage	V_{IN}	-5.0 to 0	V
Write Current	I_{WC}	0 to 60	mA
Power Dissipation	P_D	580	mW
Operating Temperature	T_A	0 to 70	°C
Storage Temperature	T_{STG}	-55 to 150	°C

NOTE: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 — MB4316 BLOCK DIAGRAM



PIN DESCRIPTIONS

Table 1. Pin Functions

Pin Number	Symbol	Functions
1	V_{EE2}	Power Supply (-12 V)
2 3	G1 G2	Gain of output Amplifier (Receiver) is specified with an External resistor between G1 and G2.
4	RWD	This input specifies Data level in write mode.
5	$\overline{WT}$	WC switch. When it is at CML low level, WC is active.
6	WC	Write Current Source Output
7	RWC	Write Current is specified with resistor between RWC and V_{EE2} (See Block Diagram). ($I_{WC} \fallingdotseq 5.4$ V/R_{EXT2})
8	GND	Ground
9	V_{EE1}	Power Supply (-5.2 V)
10 11	WD $\overline{WD}$	Write Data, driven by complementary signal of CML level.
12 13	DX DY	Data Bus
14	$\overline{RD}$	Read/Write mode Switch. When it is at CML low level, read mode is selected, and at high level, write mode is selected.
15 16	OUT $\overline{OUT}$	Output for read data

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage	V_{EE1}	-5.2 ± 5%	V
	V_{EE2}	-12.0 ± 5%	V
Output Terminal Voltage	V_{CC}	6.0 ± 5%	V
External Resistance	R_{EXT1}	700 ± 2%	Ω

6

ELECTRICAL CHARACTERISTICS

(V_{EE1} = −5.2 V, V_{EE2} = −12.0 V, T_A = 25°C)

Parameter	Symbol	Conditions	Measurement Diagram	Min	Typ	Max	Unit
Supply Current	I_{EE1}	V_{EE1} = −5.46 V, V_{EE2} = −12.6 V	Fig. 2	—	—	65	mA
	I_{EE2R}		Fig. 2	—	—	15	mA
	I_{EE2W}		Fig. 2	—	—	10	mA
Input Current	$I_{I\overline{RD}}$	V_{EE1} = −5.46 V, V_{EE2} = −12.6 V; $V_{\overline{RD}}$ = −0.81 V, $V_{\overline{WT}}$ = −1.71 V	Fig. 2	—	—	0.2	mA
	I_{IWD}	V_{WD} = −0.81 V	Fig. 2	—	—	0.9	mA
	$I_{I\overline{WD}}$	$V_{\overline{WD}}$ = −0.81 V	Fig. 2	—	—	0.9	mA
	$I_{I\overline{WT}}$	$V_{\overline{RD}}$ = −1.71, $V_{\overline{WT}}$ = −0.81 V	Fig. 2	—	—	0.15	mA
Output Voltage	V_{WC}	$V_{\overline{RD}}$ = −0.89 V, $V_{\overline{WT}}$ = −1.75 V	Fig. 2	4.9	5.4	5.9	V
	V_{DXH}	$V_{\overline{RD}}$ = −0.96 V, $V_{\overline{WD}}$ = −0.96 V	Fig. 2	−0.59	—	−0.45	V
	V_{DXL}	$V_{\overline{WT}}$ = −1.65 V, V_{WD} = −0.96 V	Fig. 2	−0.75	—	−0.61	V
	V_{DYH}		Fig. 2	−0.59	—	−0.45	V
	V_{DYL}	$V_{\overline{WD}}$ = −0.96 V	Fig. 2	−0.75	—	−0.61	V
DX, DY Differential Output Voltage	$\lvert V_{XY} \rvert$	$\lvert V_{DX} - V_{DY} \rvert$	Fig. 2	160	—	—	mV
Voltage Gain	A_V	V_I = 100mV$_{PP}$, f = 5 MHz	Fig. 3	0.95	1.1	1.25	V/V
Band Width	BW		Fig. 3	30	—	—	MHz
Delay Time	t_{PLH1}	$\overline{WT} \rightarrow$ RWC	Fig. 4	—	—	350	ns
	t_{PHL1}		Fig. 4	—	—	100	ns
	t_{PLH2}	$\overline{RD} \rightarrow$ DX, DY	Fig. 5	—	—	200	ns
	t_{PHL2}		Fig. 5	—	—	100	ns

6

TEST CIRCUIT

Fig. 2

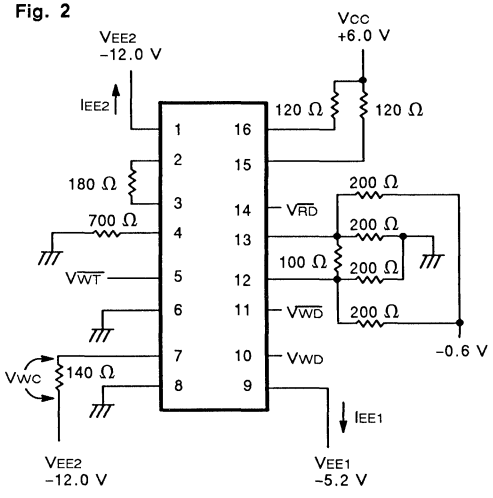
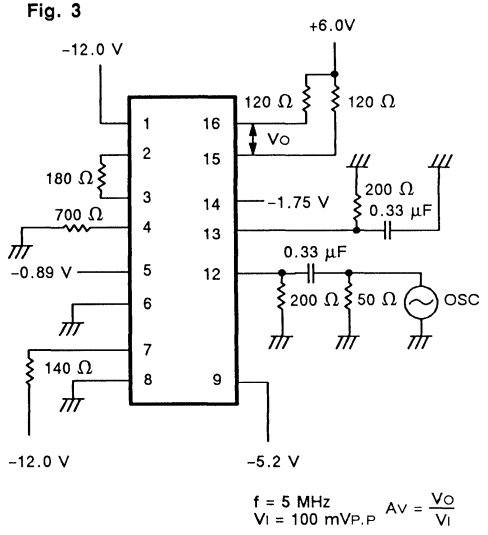
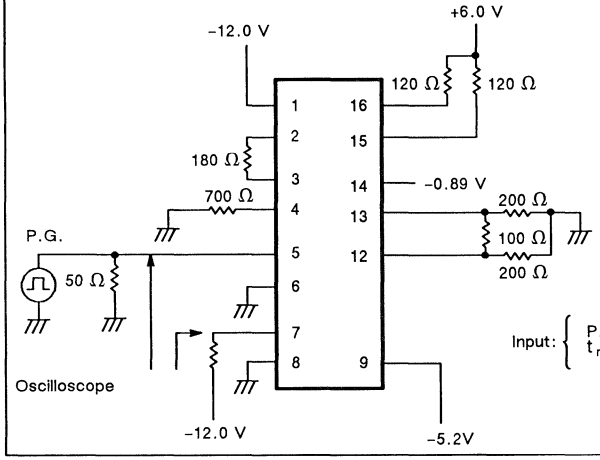


Fig. 3

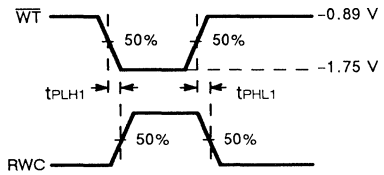


f = 5 MHz
V_I = 100 mV_{P-P}
$A_V = \frac{V_O}{V_I}$

Fig. 4



Input: { P.R.R.: 1.5 MHz
$t_r = t_f$ = 10 ns



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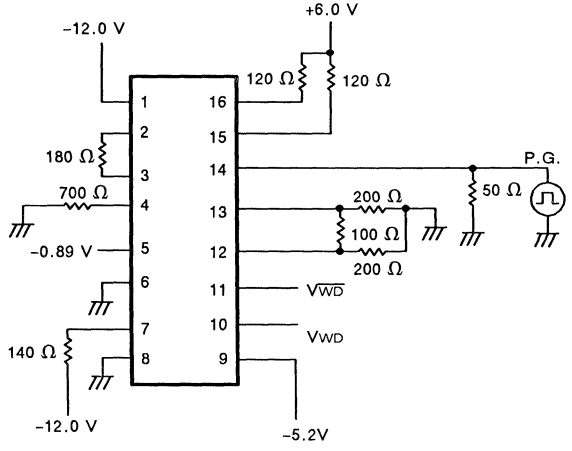
TEST CIRCUIT (Continued)

Fig. 5



OUTPUT	BIAS	
	V_{WD}	$V_{\overline{WD}}$
DX	-0.89 V	-1.75 V
DY	-1.75 V	-0.89 V

Input: { P.R.R.: 1.5 MHz
$t_r = t_f$ = 10 ns

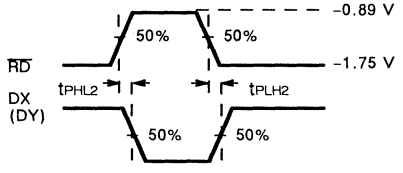


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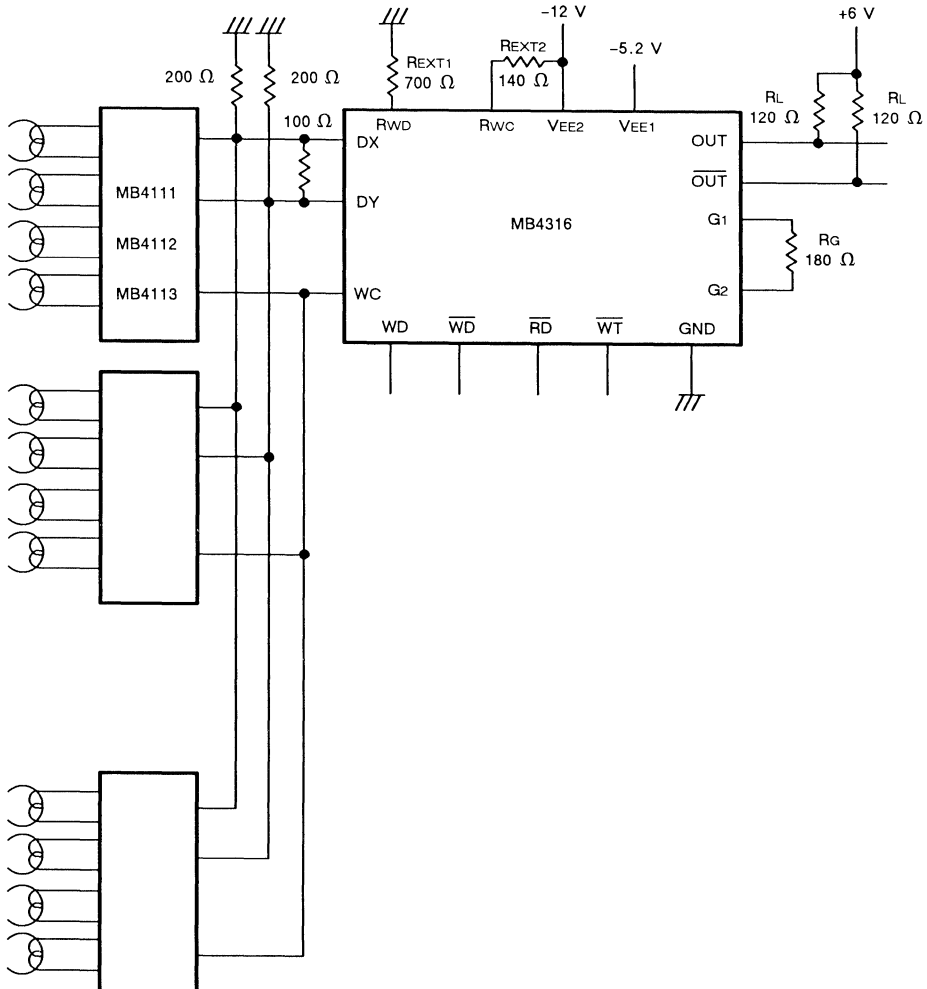
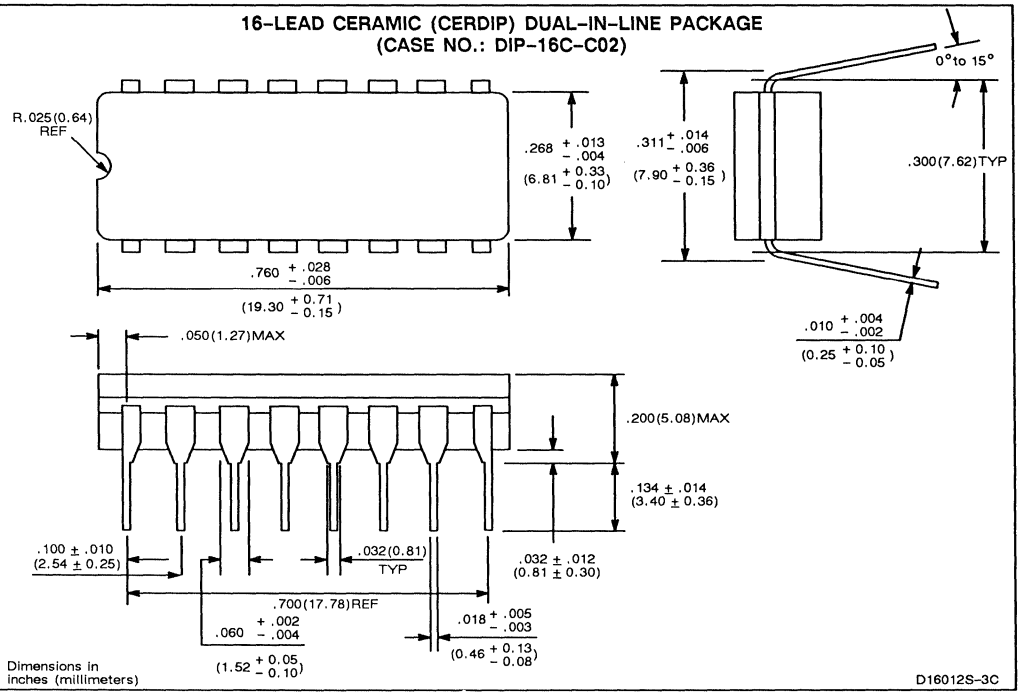
Fig. 6 — Application Circuit



PACKAGE DIMENSIONS

16-LEAD CERAMIC (CERDIP) DUAL-IN-LINE PACKAGE
(CASE NO.: DIP-16C-C02)



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March 1990
Edition 1.1

FUJITSU

PRODUCT PROFILE

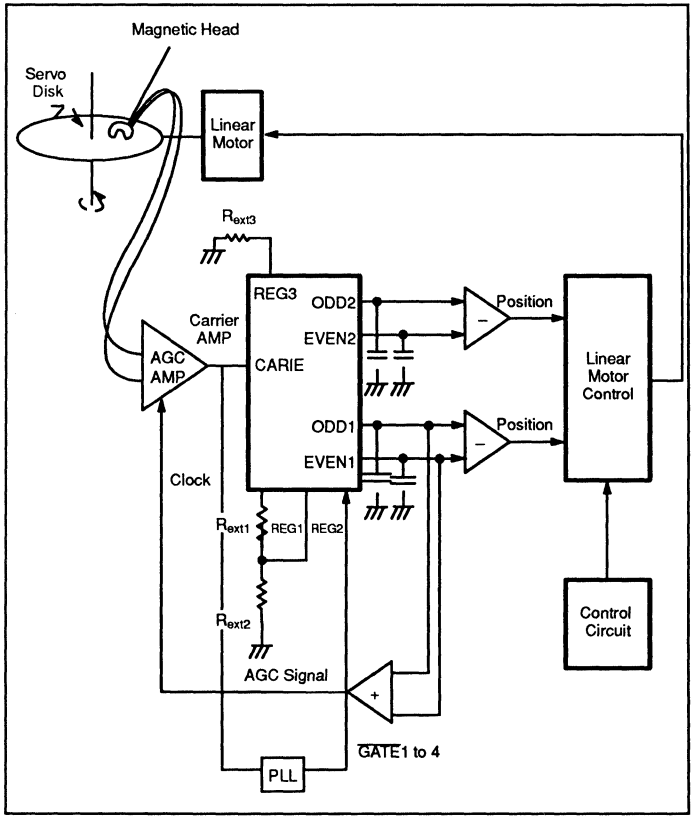
MB4319
Peakhold IC

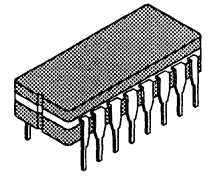
DESCRIPTION

The MB4319 is designed to generate the head position signal for head control in a magnetic disk unit similar to the one illustrated below. (See Figure 1.)

The MB4319 detects the peak of the servo signals that are read out from the servo disk via the carrier amplifier and makes the discharge continuously proportional to the head velocity. (See Figure 2.)

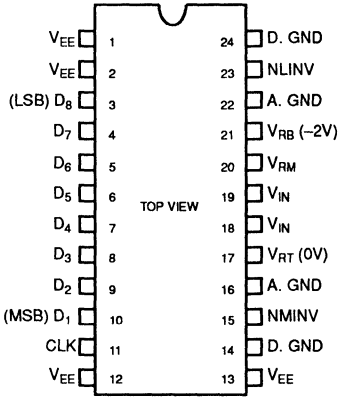
Figure 1. The MB4319 Disk Drive Application





Ceramic Package
DIP-16C-C05

Pin Assignment



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Figure 2. TIMING DIAGRAM

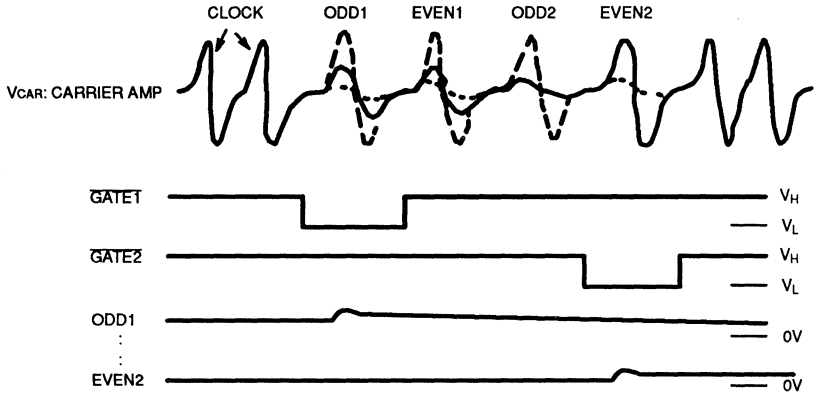
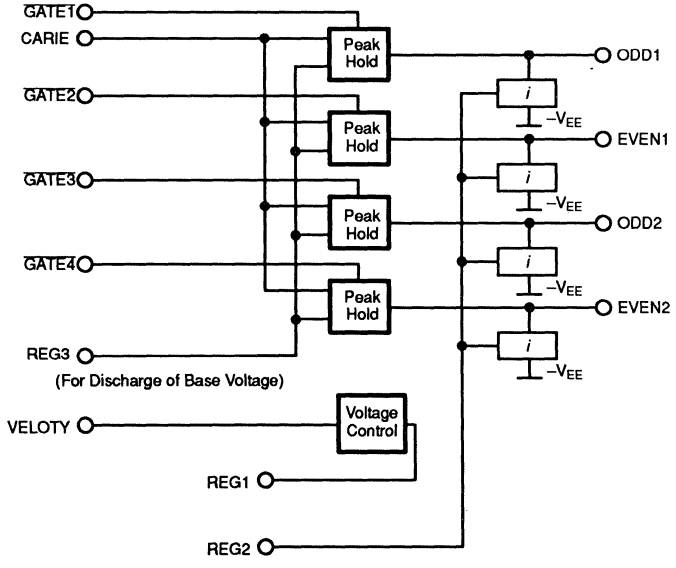


Figure 3. BLOCK DIAGRAM



Operation Details for the MB4319

The MB4319 detects each peak of the high frequency signal and selects the discharge constants externally. The MB4319 comprises four peak-hold circuits in order to control each discharge constant equally.

CARIE, the sampled signal illustrated in Figure 5, has a peak-to-peak value of 9 V Max. The gate signals are negative logic and have a 270 ns window for positive peak. When the gate is closed, the falling constant α is determined by the function of VELOTY, R R_{est1}. and R_{ext2}. VELOTY is negative voltage that is proportional to the velocity of the head. VELOTY has a range of 0 V through –6.0 V.

Example: Charge rising constant : 10 V/µs
Discharge falling constant : –0.13V/µs at Vv = 0 V
: –0.5V/µs at Vv = –5.5 V
Condition : C_{ext} = 680 pF

As shown in Figure 1, the ODD and EVEN outputs should be buffered from the following stages by high impedance input amplifiers.

Figure 4. EQUIVALENT CIRCUIT

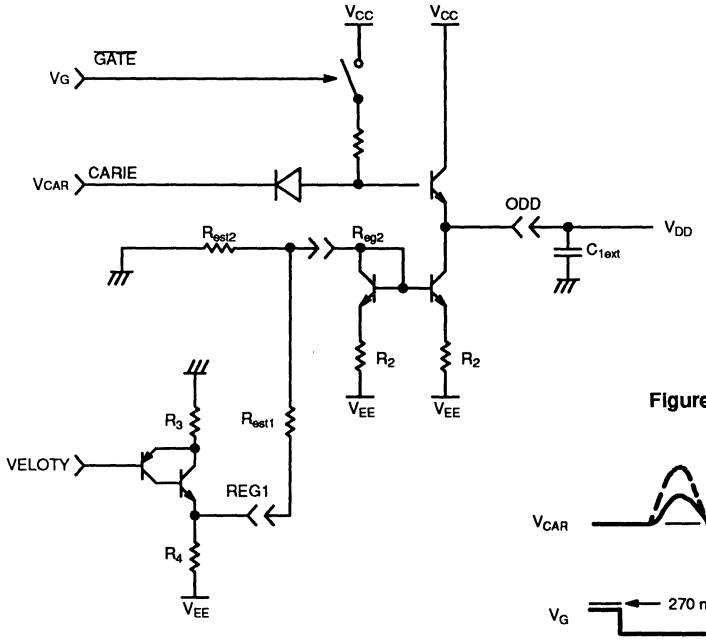
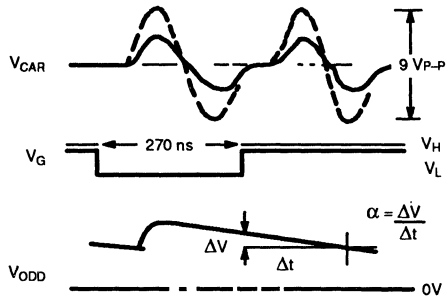
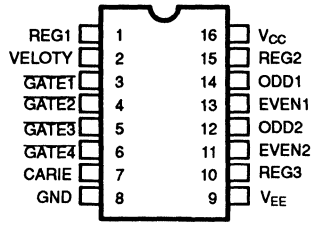


Figure 5. TIMING DIAGRAM



PIN ASSIGNMENT
(TOP VIEW)



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Absolute Maximum Ratings (TA = 25°C, unless otherwise noted.)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	+15	V
Supply Voltage	V_{EE}	–15	V
Power Dissipation	P_D	580	mW
Operating Temperature	T_{OP}	0 thru 70	°C
Storage Temperature	T_{STG}	–55 thru +150	°C
Input Voltage at CARIE	V_{CAR}	–5.5 thru +5.5	V
Input Voltage at $\overline{GATE_n}$	V_G	–0.5 thru +5.5	V
Input Voltage at VELOTY	V_V	V_{EE} thru +3.0	V
Input Current at REG2	I_{REG2}	1	mA
Input Current at REG3	I_{REG3}	5	mA
Output Load Current at ODD1/2 & EVEN1/2	I_{LOAD}	10	mA
Output Load Current at REG1	I_{REG1}	1	mA

Operating Conditions (TA = 0°C thru +70°C, unless otherwise noted.)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Supply Voltage	V_{CC}	11.4	12.0	12.6	V	
Supply Voltage	V_{EE}	–12.6	–12.0	–11.4	V	
Input Voltage at CARIE	V_{CAR}	–4.5	—	+4.5	V	
High-level Input Voltage at GATEn	V_{GH}	2.0	—	—	V	
Low-level Input Voltage at GATEn	V_{GL}	—	—	0.8	V	
Input Voltage at VELOTY	V_V	–5.5	—	+0.5	V	Rext1 = 22k Ω
Input Current at REG2	I_{REG2}	—	—	0.4	mA	
Input Current at REG3	I_{REG3}	—	—	2.5	mA	
Output Current at ODD1/2 & EVEN1/2	I_{LOAD}	—	—	1	mA	See Note
Output Current at REG1	I_{REG1}	—	—	0.3	mA	Vv = –5.5 V, Rext1 = 22k Ω

Note: I_{LOAD} is defined as illustrated below.

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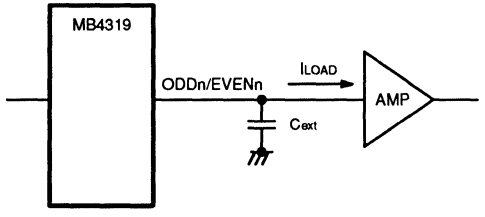
Figure 6. ILOAD



Electrical Characteristics

DC CHARACTERISTICS

(V_{CC} = +12 V, V_{EE} = −12 V, Tolerance: ±2%, unless otherwise noted.)

(V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5% when T_A = 0°C thru 70°C as a condition.)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Gate High Input Current	I_{G1H}, I_{G2H}, I_{G3H}, I_{G4H}	$V_{G1} = V_{G2} = V_{G3} = V_{G4}$ = 2.0V, T_A = 0°C thru 70°C, see Figure 1.	—	—	100	µA
Gate Low Input Current	I_{G1L}, I_{G2L}, I_{G3L}, I_{G4L}	$V_{G1} = V_{G2} = V_{G3} = V_{G4}$ = 0.8 V, T_A = 25 ±2°C, see Figure 1.	−1.8	−1.2	−0.6	mA
CARIE Input Current	I_{CAR}	$V_{G1} = V_{G2} = V_{G3} = V_{G4}$ = 2.0 V, T_A = 0°C thru 70°C, V_{CAR} = +4.0 V, see Figure 1.	—	—	100	mA
CARIE Input Current	I_{CAR}	$V_{G1} = V_{G2} = V_{G3} = V_{G4}$ = 2.0 V, T_A = 25 ±2°C, V_{CAR} = −0.4 V, see Figure 1.	−2.4	−1.5	−1.0	mA
CARIE Input Current	I_{CAR}	$V_{G1} = V_{G2} = V_{G3} = V_{G4}$ = 0.8 V, T_A = 25 ±2°C, V_{CAR} = +4.0 V, see Figure 1.	−2.9	−2.0	−1.4	mA
CARIE Input Current	I_{CAR}	$V_{G1} = V_{G2} = V_{G3} = V_{G4}$ = 0.8 V, T_A = 25 ±2°C, V_{CAR} = −4.0 V, see Figure 1.	−7.1	−5.1	−3.9	mA
REG2 Input Voltage	ΔV_{REG2}	I_{REG2} = 45 µA, see Figure 2.	0.72	0.86	1.0	V
REG3 Input Voltage	ΔV_{REG3}	I_{REG3} = 1.0 mA, see Figure 2.	1.0	1.5	2.1	V
VELOTY Input Current	I_{VEL}	V_{VEL} = −4.0 V, see Figure 1.	—	0.5	13	µA
REG1 Output Voltage	V_{REG1}	V_{VEL} = 0 V, see Figure 1.	—	—	−11.4	V
REG1 Output Voltage	V_{REG1}	V_{VEL} = −4.0 V, see Figure 1.	−8.0	−6.8	−5.5	V

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Electrical Characteristics (Continued)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
ODD1/2 EVEN1/2 Output Voltage	V_{ODD1} V_{ODD2} V_{EVEN1} V_{EVEN2}	$V_{G1} = V_{G2} = V_{G3} = V_{G4} = 2.0$ V, $T_A = 25 \pm 2°C$, see Figure 9. $V_{CAR} = +4.0$ V	–1.5	–1.2	–0.8	V
ODD1/2 EVEN1/2 Output Voltage	V_{ODD1} V_{ODD2} V_{EVEN1} V_{EVEN2}	$V_{G1} = V_{G2} = V_{G3} = V_{G4} = 2.0$ V, $T_A = 25 \pm 2°C$, see Figure 9. $V_{CAR} = +2.0$ V	–1.5	–1.2	–0.8	V
ODD1/2 EVEN1/2 Output Voltage	V_{ODD1} V_{ODD2} V_{EVEN1} V_{EVEN2}	$V_{G1} = V_{G2} = V_{G3} = V_{G4} = 2.0$ V, $T_A = 25 \pm 2°C$, see Figure 9. $V_{CAR} = 0$V	–1.5	–1.2	–0.8	V
ODD1/2 EVEN1/2 Output Voltage	V_{ODD1} V_{ODD2} V_{EVEN1} V_{EVEN2}	$V_{G1} = V_{G2} = V_{G3} = V_{G4} = 2.0$ V, $T_A = 25 \pm 2°C$, see Figure 9. $V_{CAR} = -4.0$ V	–1.5	–1.2	–0.8	V
ODD1/2 EVEN1/2 Output Voltage	V_{ODD1} V_{ODD2} V_{EVEN1} V_{EVEN2}	$V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.8$ V, $T_A = 25 \pm 2°C$, see Figure 9. $V_{CAR} = +4.0$ V	4.0	4.3	4.6	V
ODD1/2 EVEN1/2 Output Voltage	V_{ODD1} V_{ODD2} V_{EVEN1} V_{EVEN2}	$V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.8$ V, $T_A = 25 \pm 2°C$, see Figure 9. $V_{CAR} = +2.0$ V	2.0	2.3	2.6	V
ODD1/2 EVEN1/2 Output Voltage	V_{ODD1} V_{ODD2} V_{EVEN1} V_{EVEN2}	$V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.8$ V, $T_A = 25 \pm 2°C$, see Figure 9. $V_{CAR} = 0$V	0	0.3	0.6	V
ODD1/2 EVEN1/2 Output Voltage	V_{ODD1} V_{ODD2} V_{EVEN1} V_{EVEN2}	$V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.8$ V, $T_A = 25 \pm 2°C$, see Figure 9. $V_{CAR} = -4.0$ V	–1.5	–1.2	–0.8	V
ODD1/2 EVEN1/2 Output Difference Voltage	ΔV_{OUT}	$V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.8$ V, $V_{CAR} = 2.0$V, $T_A = 25 \pm 2°C$ The max difference voltage in the measurement of ODD1/2 & EVEN1/2 Output Voltage, see Figure 9.	—	—	0.1	V
ODD1/2 EVEN1/2	I_{OL1}	$V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.8$ V, $V_{ODD1} = V_{ODD2} = 2.0$ V, $V_{EVEN1} = V_{EVEN2} = 2.0$ V, $V_{CAR} = 0$V $R_{ext1} = R_{ext2}$: Open $T_A = 25 \pm 2°C$, see Figure 10.	–10	—	10	mA

Electrical Characteristics

AC CHARACTERISTICS

(V_{CC} = +12 V, V_{EE} = −12 V, Tolerance: ±2%, unless otherwise noted.)

(V_{CC} = +12 V ±5%, V_{EE} = −12 V ±5% when T_A = 0°C thru 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Rising Time of V_{ODDn}/ $EVEN_n$ when V_{Gn} is ON	t_{rO1}, t_{rO2}, t_{rE1}, t_{rE2}	V_{CAR} = 4 ±0.1 V, V_{VEL} = −4 ±0.1 V, T_A = 25 +2°C, see Figure 11.	—	350	500	ns
Rising Time of V_{ODDn}/ $EVEN_n$ when step input is input at V_{CAR}	t_{srO1}, t_{srO2}, t_{srE1}, t_{srE2}	V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.3V ±0.1 V, V_{VEL} = −4 ±0.1 V, T_A = 25 ±2°C see Figure 11.	—	190	300	ns
Falling Time of V_{ODDn}/ $EVEN_n$	t_{fO1}, t_{fO2}, t_{fE1}, t_{fE2}	V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.8 V, see Figure. 11, V_{VEL} = 0 V	50	90	180	µs
Falling Time of V_{ODDn}/ $EVEN_n$	t_{fO1}, t_{fO2}, t_{fE1}, t_{fE2}	V_{G1} = V_{G2} = V_{G3} = V_{G4} = 0.8 V, see Figure 11, V_{VEL} = −4 ±0.1 V	7	12.5	25	µs
Channel Separation	ΔV_{sp}	Change of VEVEN1 when V_{CAR} = +4.0 V, V_{G2} = 0.3 V, and V_{G1}, V_{G3}, and V_{G4} are changed from 2.0 V to 0.3 V at the same time. See Figure 11.	—	—	0.2	V

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Figure 7

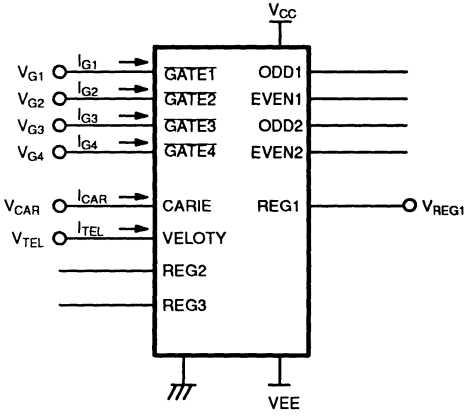

Figure 8

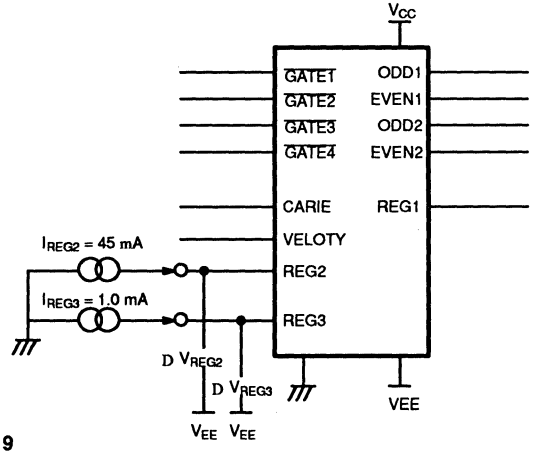

Figure 9

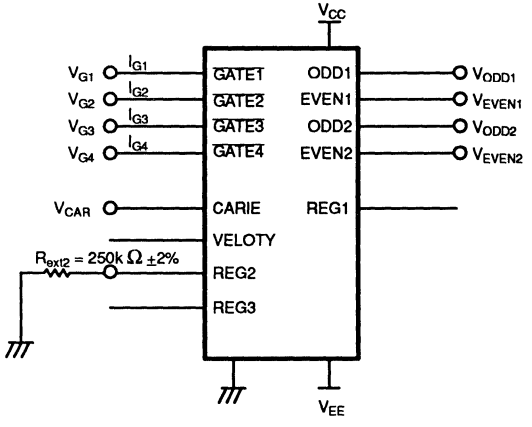

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Figure 10

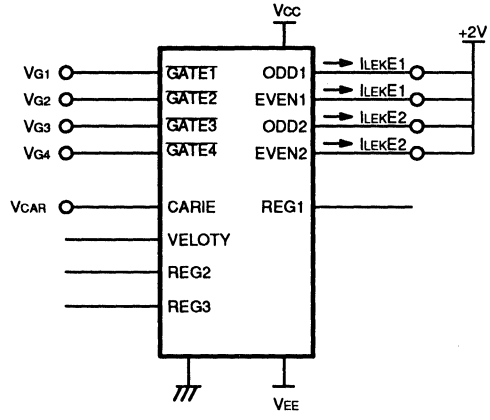
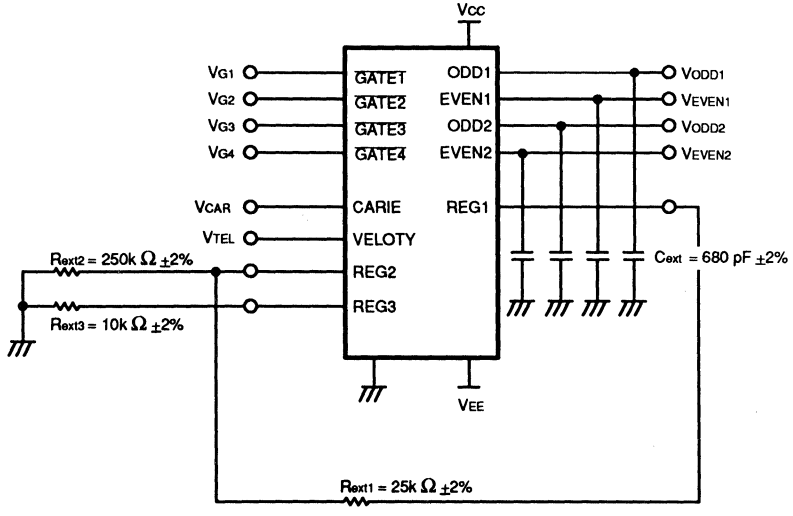
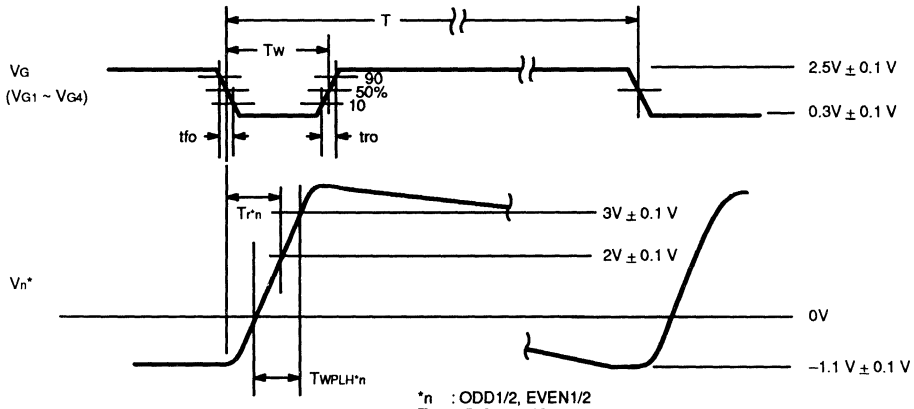


Figure 11

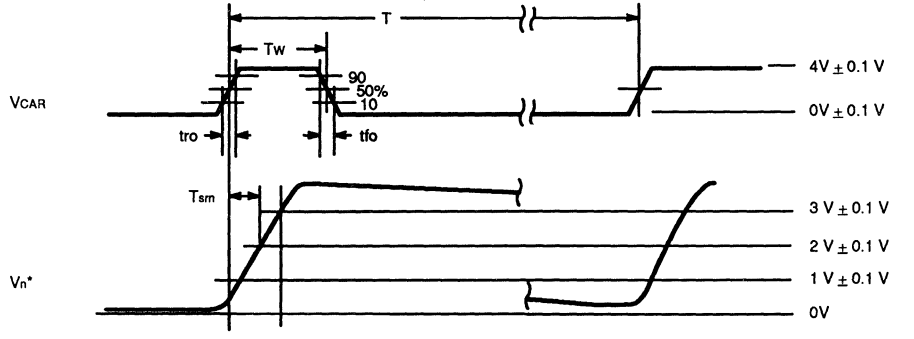


TIME CHART 1.



*n : ODD1/2, EVEN1/2
Tw = 500 ns ± 10 ns
tfo = tro ≤ 10 ns
T ≥ 220 µs

TIME CHART 2.



*n : ODD1/2, EVEN1/2
Tw = 500 ns ± 10 ns
tfo = tro ≤ 10 ns
T ≥ 220 µs

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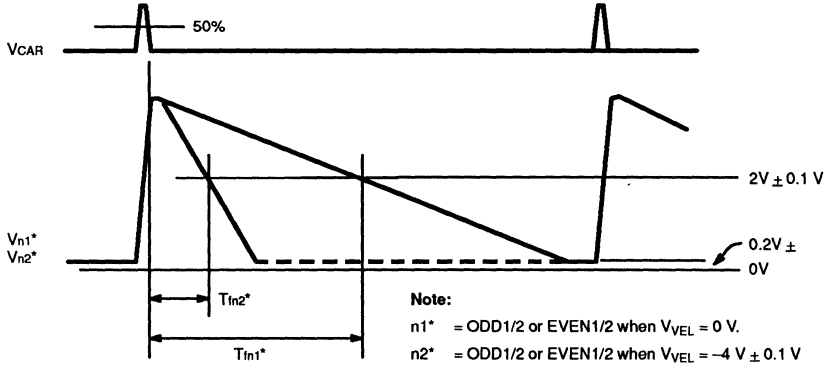
TIME CHART 3.



Note:

n1* = ODD1/2 or EVEN1/2 when V_{VEL} = 0 V.

n2* = ODD1/2 or EVEN1/2 when V_{VEL} = –4 V ± 0.1 V

V_{CAR} : As same as Time Chart 2.

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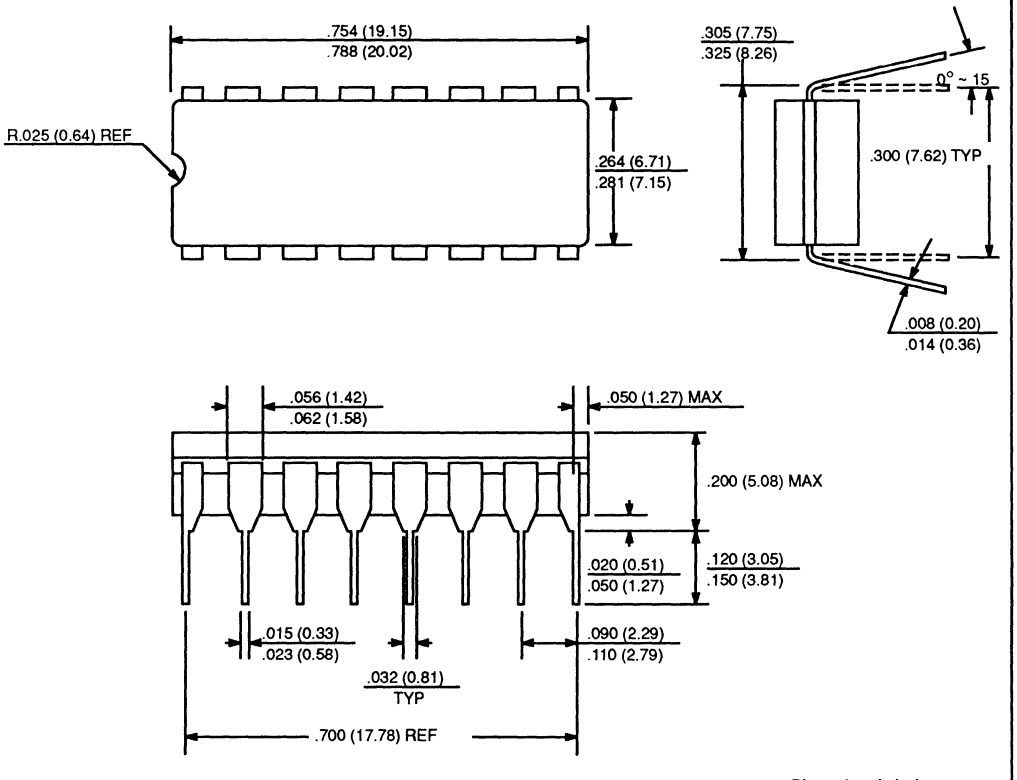
DIP–16C–C05



Dimensions in inches
and (millimeters)

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Section 7

Data Conversion — *At a Glance*

Page	Device	Description	Features	Power Supply (V)	Package Options
A/D Converters – Data Acquisition Systems					
7–3	MB4051	8-channel 1-bit	25 µs/Ch, SAR V_{IN} = 0 to +6.5 V	±5, ±8	42-pin Plastic DIP
7–27	MB4052	4-channel 8-bit	100 µs/Ch, SAR Three Analog Input Ranges	+5, +12	16-pin Plastic DIP, FPT 16-pin Ceramic DIP
7–39	MB4053 4063	6-channel 8-bit	300 µs/Ch, Slope Conversion On-Chip Reference	+5 to +15	16-pin Plastic DIP, FPT 16-pin Ceramic DIP
7–51	MB4056	8-channel 8-bit	100 µs/Ch, SAR, V_{IN} = 0 to 5 V or 0 to 1.25 V	+5 to +18	16-pin Plastic DIP 16-pin Ceramic DIP
7–61	MB4066	8-channel 8-bit	100µs/Ch, SAR	+7.6 to +18	16-pin Plastic DIP 16-pin Ceramic DIP
A/D Converters – Video					
7–69	MB40547-7 40547-8	1-channel 8-bit	30 MSPS (typ.) ECL	–5.2	24-pin Ceramic DIP
7–77	MB40576	1-channel 6-bit	30 MSPS (typ.) TTL	+5	16-pin Plastic DIP, FPT
7–89	MB40578 40578-7	1-channel 8-bit	30 MSPS (typ.) TTL	+5	22-pin Plastic DIP
D/A Converters – Multi-purpose					
7–97	MB4072	1-channel 8-bit	M – DAC, R/ZR	±4.5 to ±1.8	16-pin Plastic DIP, FPT 16-pin Ceramic DIP
7–105	MB88301A	1-channel 13-bit and 3-channel 6-bit	PWM, V_{OUT}	+5	16-pin Plastic DIP, FPT
7–117	MB88341 88342*	12- and 8-channels 8-bit	R/ZR, V_{OUT}	+5	20-pin Plastic DIP, FPT *16-pin Plastic DIP, FPT *20-pin Plastic FPT

Data Conversion — *At a Glance (Continued)*

Page	Device	Description	Features	Power Supply (V)	Package Options
D/A Converters – Video					
7–137	MB40748-8 40748-9 40748-10	1-channel 10-bit	30 MSPS, ECL	–5.46 to –4.94	24-pin Ceramic DIP
7–145	MB40776	1-channel 6-bit	30 MSPS, TTL	+4.75 to +5.25	16-pin Plastic DIP, FPT
7–157	MB40776H	1-channel 6-bit	60 MSPS, TTL	+4.75 to +5.25	16-pin Plastic DIP
7–167	MB40778	1-channel 8-bit	30 MSPS, TTL	+4.75 to +5.25	20-pin Plastic DIP, FPT
7–179	MB40788	1-channel 10-bit	125 MSPS, ECL	–5.46 to –4.94	24-pin Ceramic DIP
7–187	MB40874	1-channel 4-bit	4-bit LUT, TTL	+4.75 to +5.25	20-pin Plastic DIP 20-pin Ceramic DIP
7–199	MB40968 MB40968V	2-channel 8-bit	30 MSPS, TTL	+4.75 to +5.25	28-pin Plastic DIP, FPT
7–209	MB40978	3-channel 8-bit	60 MSPS, TTL	+4.75 to +5.25	42-pin Plastic DIP 44-pin Plastic DIP
A/D and D/A Converters					
7–219	MB40176	1-channel 6-bit	20 MSPS (min.) TTL	+4.75 to +5.25	16-pin Plastic DIP, FPT
7–229	MB87020	1-channel 16-bit	50KSPS, Audio	+4.75 to +5.25	40-pin Plastic DIP
V/F Converters					
7–261	MB4206	Frequency-to-Voltage	On-chip Comparator	+6.5 to +24	8-pin Plastic SIP
7–267	MB4207	Frequency-to-Voltage	Built-in Reference Voltage	+4.8 to +24	8-pin Plastic SIP

FUJITSU

8-CH 10-BIT A/D CONVERTER(ADC)

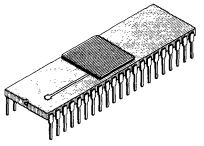
MB4051

July 1989
Edition 1.0

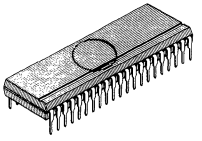
8-CHANNEL 10-BIT A/D CONVERTER

The Fujitsu MB4051 is a general purpose analog-to-digital converter (ADC) which features eight channels of analog inputs, 10-bit parallel data I/O port and programmable control register. Analog input signal on a selected input channel is converted to 10-bit digital data by the successive-approximation technique which provides high-speed conversion. The MB4051 is packaged in a standard 42-pin dual in-line packages.

- Multiplex 8-channel Analog Inputs
- Resolution: 10 bits
- Relative Accuracy: 8 bits Min.
- Linearity: ±1/2 LSB
- Successive-Approximation Technique: 50 μs/ch Max. at f_{CLK} = 250kHz
- Analog Input Voltage Range: 0V to 6.5V
- Analog Input Bias Current: 1μA Max.
- Input Impedance: over 500kΩ (for 6.5V Input)
- Built-in High Stabilized Reference Voltage Source
- Directly Connectable to DMA Controller as well as Microprocessor
- TTL Compatible Digital I/O Port
- Standard 42-pin DIP
- Power Supplies: +5V and ±8V
- Power Consumption: 400mW Typ.



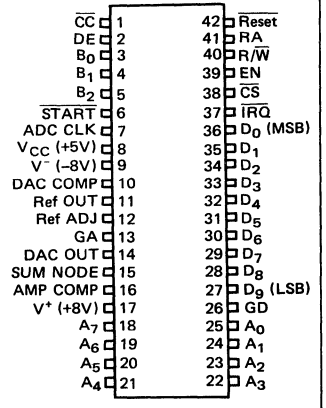
CERAMIC PACKAGE
DIP-42C-A01



PLASTIC PACKAGE
DIP-42P-M01

PIN ASSIGNMENT

(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS (All Voltage referenced to A.G/D.G)

Parameter		Symbol	Value	Unit
Supply Voltage 1		V_{CC}	+7	V
Supply Voltage 2		V^+	+10	V
Supply Voltage 3		V^-	-10	V
Digital Input Voltage		V_{ID}	-0.5 to +5.5	V
Analog Input Voltage		V_{IA}	-3.0 to V^+	V
Operating Temperature		T_A	-35 to +90	°C
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-40 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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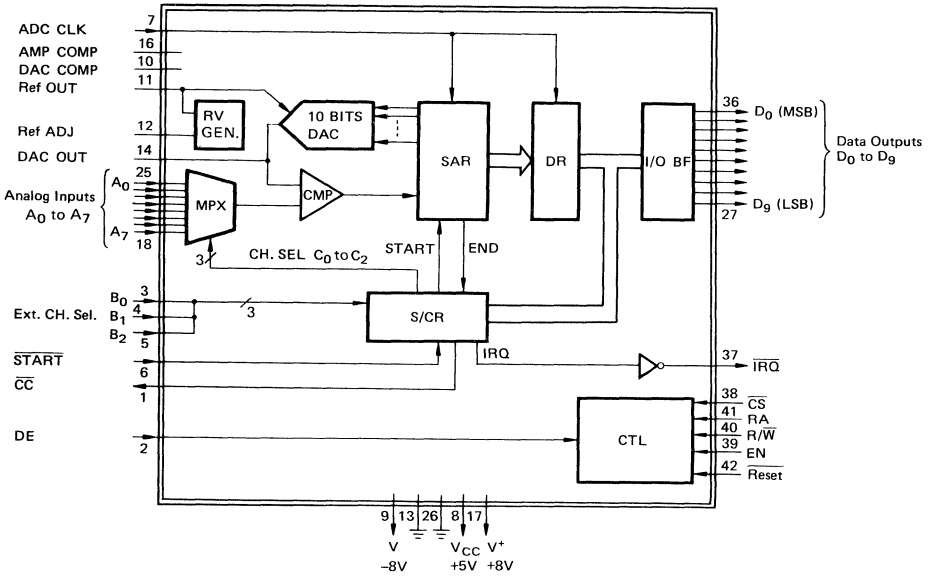
Fig. 1 – MB4051 BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage 1	V_{CC}	4.75	5.0	5.25	V
Supply Voltage 2	V^+	7.6	8.0	8.4	V
Supply Voltage 3	V^-	−8.4	−8.0	−7.6	V
Digital Output High Current	I_{OH}			−0.4	mA
Digital Output Low Current	I_{OL}			8	mA
Operating Temperature	T_{OP}	−30		+85	°C

NOTE: The negative value means "flow of current" from IC to out side of IC.

FUNCTIONAL BLOCK DESCRIPTIONS

Symbol	Name	Function
MPX	Multiplexer	Selects one channel from 8-channel analog input signals. Channel assignment is done by the 2nd thru 4th bits of control register which are programmed by the external channel select inputs B_0 thru B_2 or by a data from MPU.
CMP	Comparator	Compares an unknown analog input signal with an output signal of built-in DA converter. The result of comparison is transferred to the successive-approximation register (SAR).
DAC	DA Converter	10-bit digital-to-analog converter. Generates analog signal corresponding to digital signal specified by the SAR.
SAR	Successive-Approximation Register	According to the result from the comparator, generates the next step digital output to be transferred to the DAC and compared in the comparator. Composed of 10-bit register and control logic. After completion of data-conversion, acts as the data register (DR).
SR	Status Register	10-bit register which indicates the status of operations. Indicates the assigned channel by SR-2 to SR-4, status of the external control/MPU by SR-5, operation of AD conversion by SR-6 and completion of AD conversion by SR-7. (See Table 1, 2 of page 14)
CR	Control Register	10-bit register which controls the operation of ADC. Assigns a channel by CR-2 to CR-4, switches MPU/external control each other by CR-5, initiates AD conversion by CR-6. (See Table 1, 2 of page 14)
DR	Data Register	Stores a 10-bit data at the completion of AD conversion. Outputs the data at DE=1 during the external control mode (CR-5=5). If the DR is selected ($\overline{CS}$=0, RA=0, and R/$\overline{W}$=1) during the MPU control mode (CR-5=1), the contents can be read by MPU (EN=1).
I/O BF	Input/Output Buffer	Connected to the data-bus of MPU for sending or receiving the 10-bit data. The output is three-state TTL compatible.
CTL	Control Logic	Controls sending and receiving of data between blocks and used for initializing.
Ref	Reference Voltage Regulator	Specifies the maximum analog input signal level of ADC.

PIN DESCRIPTIONS

Symbol	Name	Function
A_0 to A_7	Analog Input	Analog input terminals of 8 channels, one of which is assigned by CR-2 to CR-4.
D_0 to D_9 D_0 ..... MSB D_9 ..... LSB	Data I/O Port	Connected to 10-bit parallel data-bus for transferring 10-bit data between internal registers and MPU.
$\overline{CS}$	Chip Select	Chip-select terminal of ADC which is selected at $\overline{CS}$=0.
RA	Register Address	Address input for the internal registers. Selects the data register (DR) at RA=0 and the control register (CR)/status register (SR) at RA=1.
R/$\overline{W}$	Read-Write Control	Input for the read-write signal from MPU (MPU read mode at R/$\overline{W}$=1).
EN	Enable Signal	Input for the enable signal of MPU system. EN is used as timing for data transfer between MPU and ADC.
$\overline{Reset}$	Reset	Initializes the ADC at $\overline{Reset}$=0.
B_0 to B_2	External Channel Select Input	When ADC is controlled external (CR-5=0), the inputs from B_0 to B_2 are set in CR-2 to CR-4 at the falling edge of $\overline{START}$. (See Table 3 of page 14)
$\overline{START}$	Start	AD conversion starts at the rising edge of $\overline{START}$ when the external control mode (CR-5=0).
$\overline{CC}$/$\overline{IRQ}$ (Open Collector)	Conversion Complete/ Interrupt Request	Indicates the completion of data conversion. After completion of data conversion, $\overline{CC}$ goes low at the external control mode (CR-5=0) or $\overline{IRQ}$ goes low at the MPU control mode (CR-5=1). In both cases, they go high after the content of the data register is read.
DE	Data Enable	During DE=1 at the external control mode, the data in a register assigned by RA are output on D_0 to D_9.
ADC CLK	AD Conversion Clock	Clock for AD conversion which is input to the SAR and determines the conversion speed of ADC. A data conversion is completed by 12 cycles of clock. Not required to synchronize with the EN (Enable) signal from MPU system. Minimum cycle time of this clock is 2μs.
Ref OUT/ Ref ADJ	Reference Output/ Reference Adjustment	Terminals for output of reference voltage which specifies the full-scale value of analog input signal and for its adjustment.
AMP COMP/ DAC COMP/ DAC OUT/ SUM NODE	Amplifier Compensation/ DAC Compensation/ DAC Output/ Sum Node	Terminals for frequency adjustment of the internal operational amplifier with connected capacitors having specified capacitances. SUM NODE is also used for offset adjustment.
$V^+/V_{CC}/V^-$	Terminals for Power Supply	To be supplied +8V, +5V and −8V, respectively. (Note 1)
GA/GD	Analog Ground/ Digital Ground	Terminals for ground.

NOTE 1: MB3758 DC-DC Converter is available, which generates +8V and −8V from signal +5V power supply.

ELECTRICAL CHARACTERISTICS

1. ANALOG CIRCUIT CHARACTERISTICS

(V_{CC} = +5V, V^+ = +8V, V^- = -8V, T_A = -30°C to +85°C)

Parameter		Value			Unit	Note
		Min	Typ	Max		
Resolution				10	bit	
Accuracy	Relative Accuracy	8			bit	
	Gain Error		±1		% of FSR	Adjustable
	Offset Error		±0.03		% of FSR	Adjustable
	Differential Linearity Error		±0.5		LSB	
Drift	Full Scale Voltage		40		ppm/°C	
	Offset Voltage		±0.5		ppm of FSR/°C	
Full Scale Power Supply Fluctuation Suppressing Ratio	Positive Power Supply		1.0		mV/V	8V±5%
	Negative Power Supply		-0.5		mV/V	-8V±5%
Analog Input	Input Current			1	μA	V_{IA} = 0 to 6.5V
	Full Scale Voltage			6.5	V	
Reference Voltage	Reference Voltage		5.0		V	
	Drift		30		ppm/°C	
Supply Current	Positive Power Supply		7	12	mA	
	Negative Power Supply		-10	-17	mA	
Conversion Cycle Time				50	μs/ch	f_{CLK} = 250Hz

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2. DIGITAL CIRCUIT DC CHARACTERISTICS

(V_{CC} = +5V ± 5%, V^+ = +8V, V^- = –8V, T_A = –30°C to +85°C)

Parameter	Symbol	Condition		Value			Unit
				Min	Typ	Max	
Input High Voltage	V_{IH}			2			V
Input Low Voltage	V_{IL}					0.8	V
Input Clamp Voltage	V_{IC}	V_{CC} = 4.75V, I_{IC} = –18mA				–1.5	V
Output High Voltage	V_{OH}	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = –2.6mA		2.4			V
Output Low Voltage	V_{OL}	V_{CC} = 4.75V, V_{IH} = 2V, V_{IL} = 0.8V,	I_{OL} = 4mA			0.4	V
			I_{OL} = 8mA			0.5	
Output Current (Off State)	I_{OZ}	V_{IH} = 2V, V_{CC} = 5.25V V_{IL} = 0.8V	V_O = 2.7V			20	μA
			V_O = 0.4V			–20	
Input High Current	I_{IH}	V_{IH} = 2.7V, V_{CC} = 5.25V				20	μA
		V_{IH} = 7V, V_{CC} = 5.25V				100	
Input Low Current	I_{IL}	V_{IL} = 0.4V, V_{CC} = 5.25V				–400	μA
Output Short Current	I_{OS}	V_O = 0V, V_{CC} = 5.25V		–15		–95	mA
Supply Current	I_{CC}	A_0 to A_7, $\overline{Reset}$ = GND, V_{CC} = 5.25V		30	55	92	mA

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3. DIGITAL CIRCUIT AC CHARACTERISTICS
(V_{CC} = +5V±5%, V^+ = +8V, V^- = –8V, T_A = –30°C to +85°C)

ADC CLK

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Cycle time	t_{CY}		4			μs
H Level Pulse Width	t_{WAC^+}		1			μs
L Level Pulse Width	t_{WAC^-}		1			μs

Read Mode

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
EN Pulse Width	P_{WEN}		270			ns
$\overline{CS}$, R/$\overline{W}$, RA Setup Time	t_{AS}		20			ns
$\overline{CS}$, R/$\overline{W}$, RA Hold Time	t_{AH}		10			ns
Enable Time from EN	t_{EEN}	Fig. 2*			160	ns
Access Time from RA	t_{ARA}	Fig. 2*			300	ns
Disable Time from EN	t_{DEN}	Fig. 2*	10		120	ns
$\overline{IRQ}$ Recovery Time from EN	t_{IR}	Fig. 3*			240	ns

* : See page 11

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Write Mode

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
EN Pulse Width	P_{WEN}		270			ns
$\overline{CS}$, R/$\overline{W}$, RA Setup Time	t_{AS}		20			ns
$\overline{CS}$, R/$\overline{W}$, RA Hold Time	t_{AH}		10			ns
Data Setup Time	t_{DS}		10			ns
Data Hold Time	t_{DH}		10			ns

External Control AD Conversion

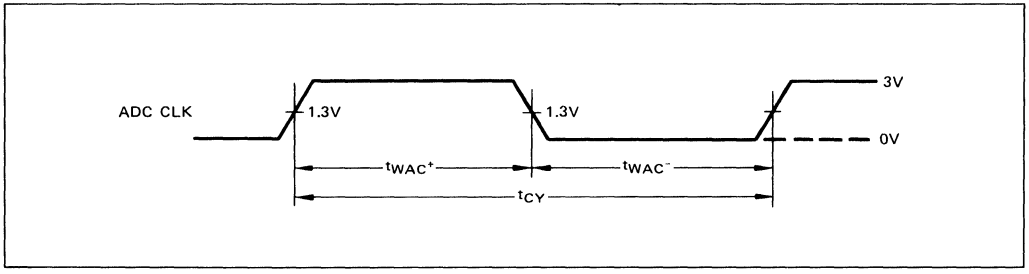
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
$\overline{START}$ Pulse Width	P_{WSL}		270			ns
Channel Setup Time	t_{BS}		20			ns
Channel Hold Time	t_{BH}		270			ns

External Control Read Mode

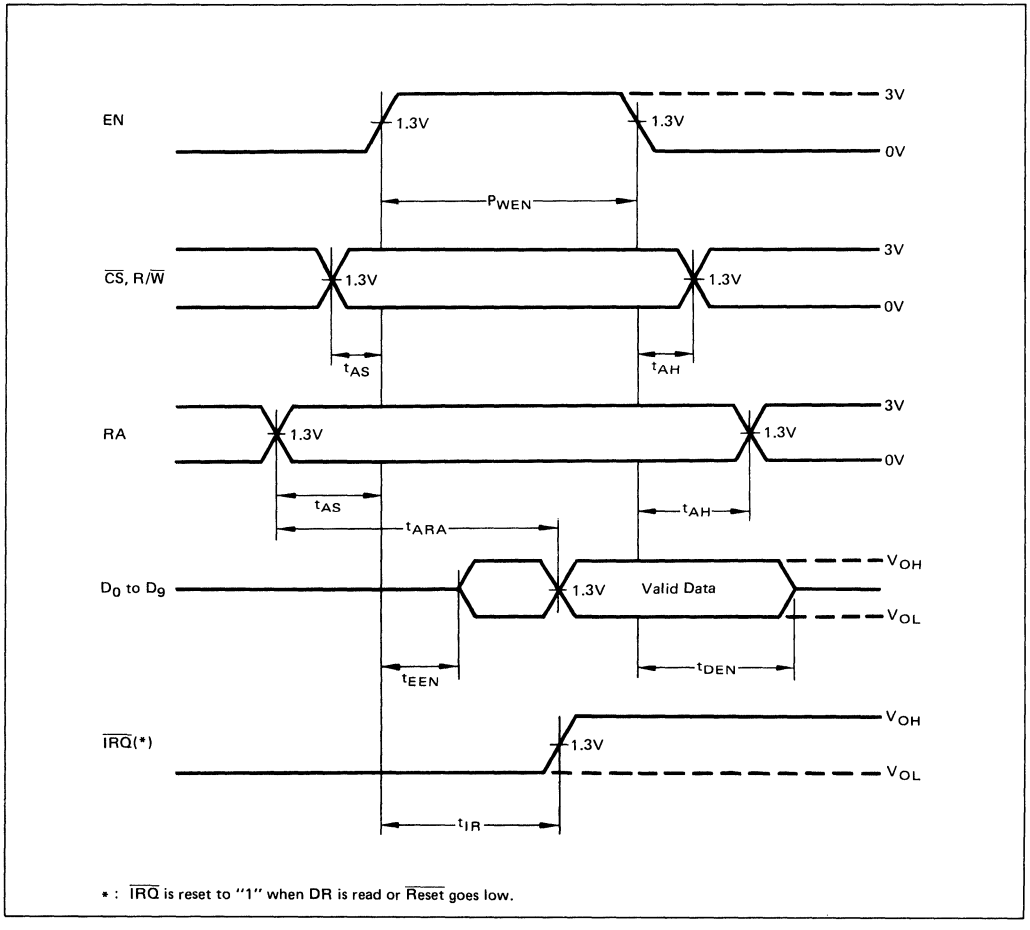
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
DE Pulse Width	P_{WDEH}		270			ns
Enable Time from DE	t_{EDE}	Fig. 2*			160	ns
Disable Time from DE	t_{DDE}	Fig. 2*	10		160	ns
$\overline{CC}$ Recovery Time from DE	t_{CCR}	Fig. 3*			280	ns

* : See page 11

ADC CLK



READ Timing Diagram



* : $\overline{IRQ}$ is reset to "1" when DR is read or $\overline{Reset}$ goes low.

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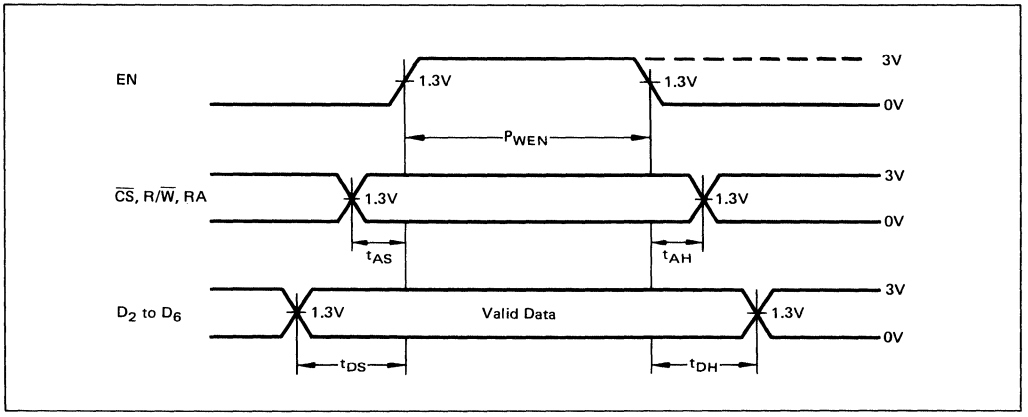
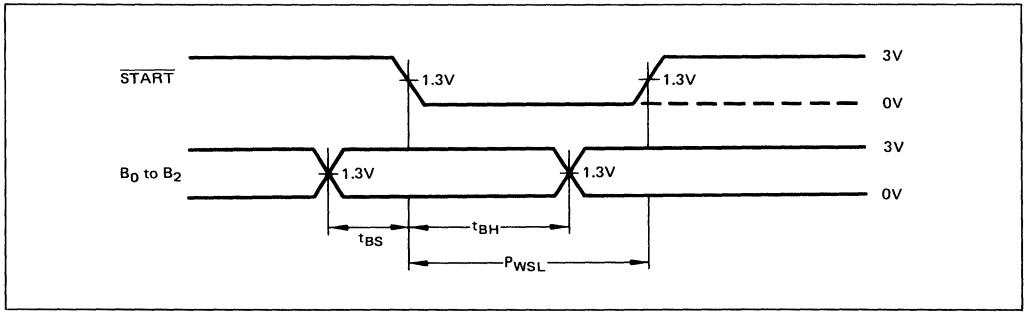
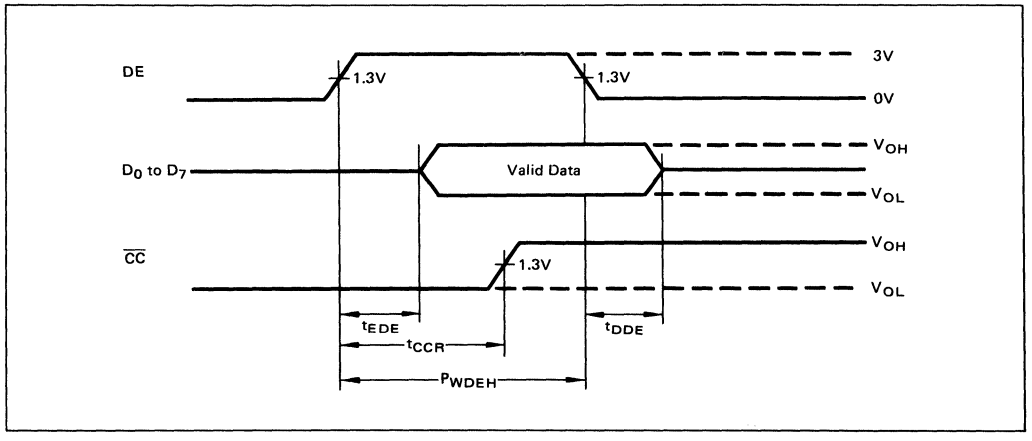
WRITE Timing Diagram



External Control AD Conversion Timing Diagram



External Control Read Timing Diagram



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4. SWITCHING CHARACTERISTICS TEST CONDITIONS

Fig. 2 – 3-STATE OUTPUT LOAD CONDITION

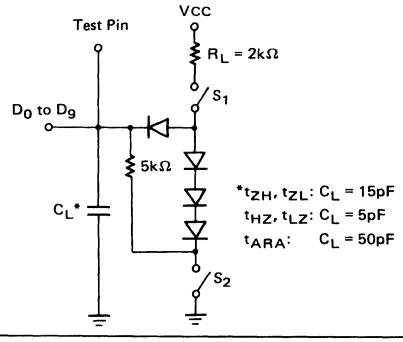
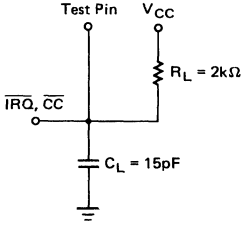
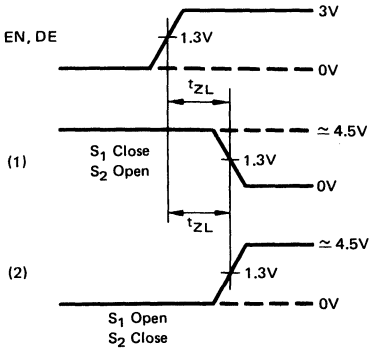


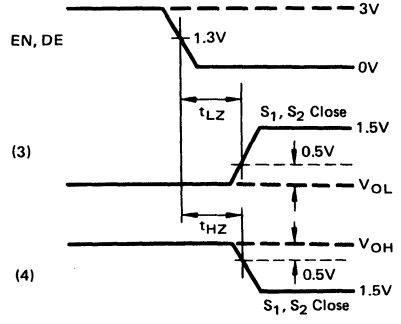
Fig. 3 – OPEN COLLECTOR OUTPUT LOAD CONDITION



5. SWITCHING WAVEFORM

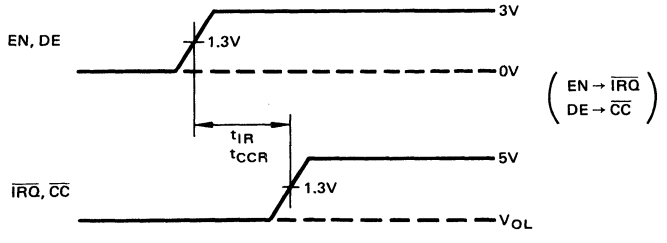
Enable, Disable Time (3-State Output)





Note S_1, S_2: See Fig. 2, above

$\overline{IRQ}$ or $\overline{CC}$ Recovery Time (Open Collector Output)



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TYPICAL CHARACTERISTICS CURVES

Fig. 4 – OUTPUT VOLTAGE vs. INPUT VOLTAGE

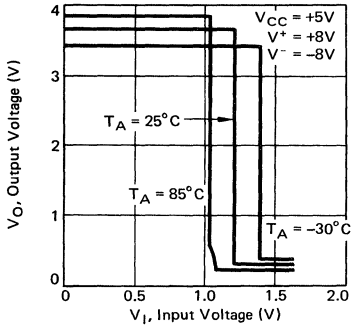


Fig. 5 – OUTPUT HIGH VOLTAGE vs. OUTPUT HIGH CURRENT

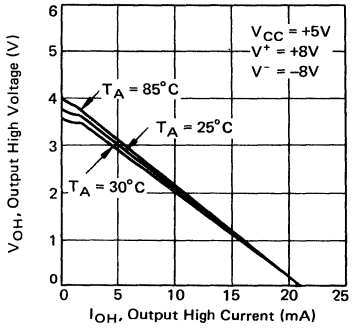


Fig. 6 – OUTPUT LOW VOLTAGE vs. OUTPUT LOW CURRENT

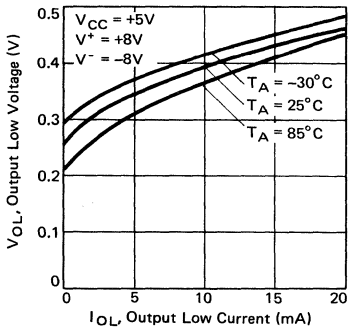


Fig. 7 – INPUT CURRENT vs. INPUT VOLTAGE (B_0 INPUT)

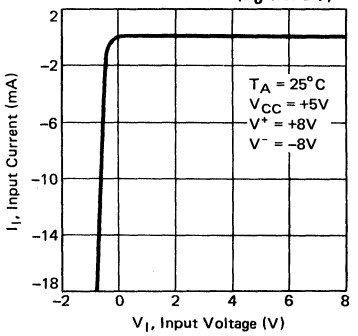
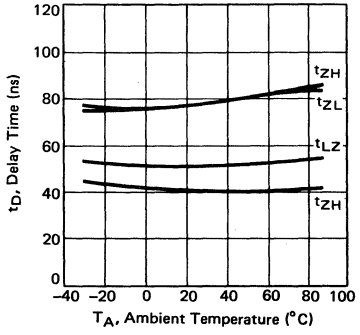


Fig. 8 – DELAY TIME vs. AMBIENT TEMPERATURE



TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 9 – SUPPLY CURRENT vs. SUPPLY VOLTAGE

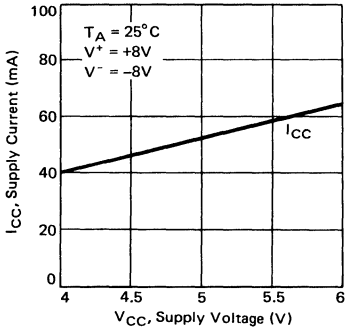


Fig. 10 – SUPPLY CURRENT vs. POSITIVE SUPPLY VOLTAGE

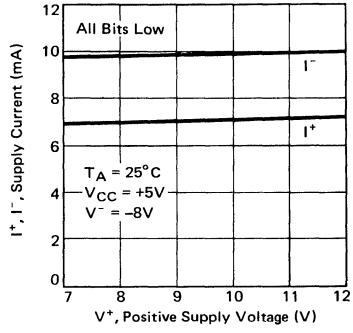


Fig. 11 – SUPPLY CURRENT vs. NEGATIVE SUPPLY VOLTAGE

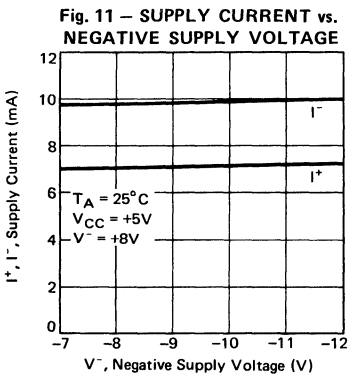


Fig. 12 – FULL SCALE VOLTAGE vs. REFERENCE VOLTAGE SUPPLY VOLTAGE (V^+, $|V^-|$)

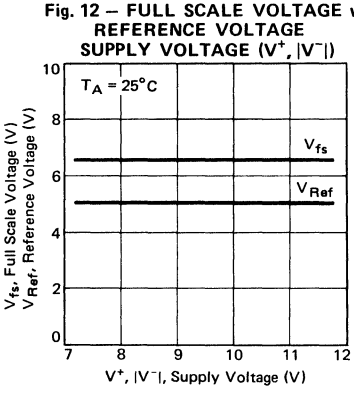
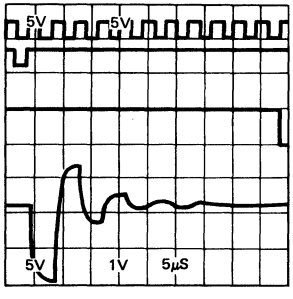


Fig. 13 – OPERATION WAVEFORM



f_{CLK} = 250kHz
Analog Input Voltage = 2.1646V
Output Coding = 0101010101

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Table 1. BIT CONSTRUCTION OF DR AND S/C R

	RA	R/$\overline{W}$	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9
DR	0	1 Read	Bit 0 (MSB)	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8	Bit 9 (LSB)
S/C R	1	1 Read	–	–	Input CH. Select			Mode Control	Busy	IRQ	–	–
		0 Write			C_0	C_1	C_2	INT/EXT	Start	–		

Table 2. CHANNEL SELECT FOR MPU CONTROL

C_2	C_1	C_0	Selected CH.
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

Table 3. CHANNEL SELECT FOR EXTERNAL CONTROL

B_2	B_1	B_0	Selected CH.
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

ADC OPERATION MODES

According to the status of 5th bit (CR-5) in the built-in control register, ADC has two operation modes: external control mode and MPU control mode.

Just after an initialization ($\overline{\text{Reset}}$ going from low to high), ADC is in the external control mode (designation of channel, start of data conversion and data output are controlled through the external control input terminals). This mode is useful for ADC applications only or for DMA operation independent of MPU.

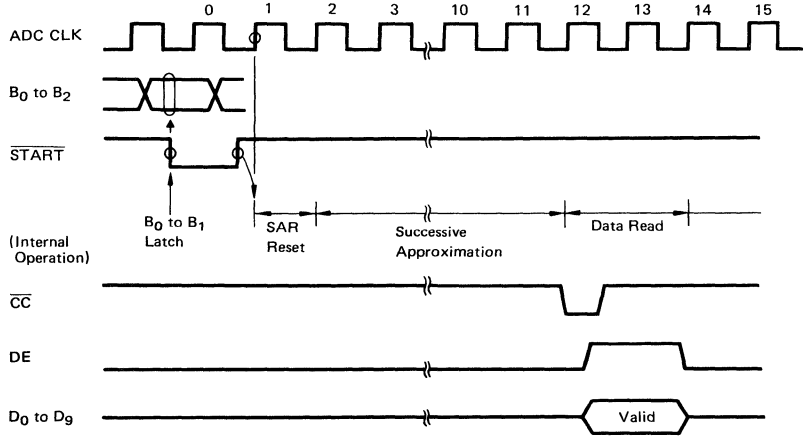
When the MPU control mode is required, set CR-5 of the control register high through MPU.

EXTERNAL CONTROL MODE (CR-5=0):

This mode is used when ADC is controlled by the external hardware. An analog input signal channel is designated by B_0 to B_2 and the AD conversion starts at the second rising edging of ADC clock after $\overline{\text{START}}$ goes low.

At the completion of 10-bit data conversion, $\overline{\text{CC}}$ (Convert Complete) goes low to notify it to external devices. The converted data is read after the low state of $\overline{\text{CC}}$ and DE goes high.

ADC TIMING FOR EXTERNAL CONTROL MODE



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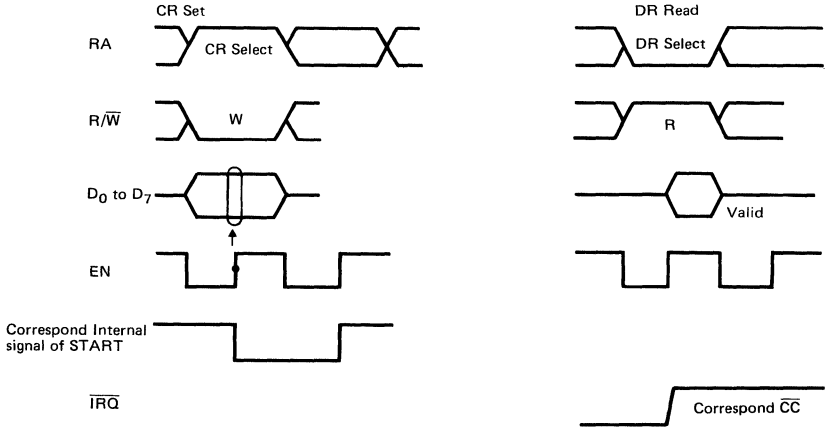
MPU CONTROL MODE (CR-5=1):

This mode is used when ADC is controlled by the MPU software. Because of CR-5=0 at initialization, CR-5 should be set high through MPU. After completion of the conversion, CR-7 (IRQ flag) is set high and $\overline{IRQ}$ output goes low to interrupt MPU operation.

After confirming $\overline{IRQ}$=0, MPU starts the interrupt routine to select the data register of ADC and reads it. After MPU reads the data register, $\overline{IRQ}$ is reset high. In this mode, all signals on $\overline{START}$ and B_0 to B_2 are ignored. When the ADC is required to return to the external control mode, CR-5 is set low through MPU or $\overline{RESET}$ is set low.

ADC TIMING FOR MPU CONTROL MODE



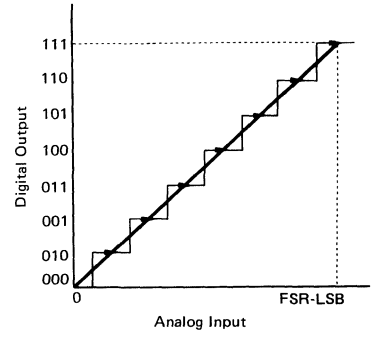
7

TECHNICAL INFORMATION

DEFINITION OF TERMS

Resolution:
The minimum distinguishable analog deviation in AD converter. Since MB4051 is 10-bit AD converter, it is possible to resolute an analog signal, from 0V to 6.5V (FSR), into 2^{10} = 1024 parts.

EXAMPLE OF RESOLUTION
(3-BIT RESOLUTION)

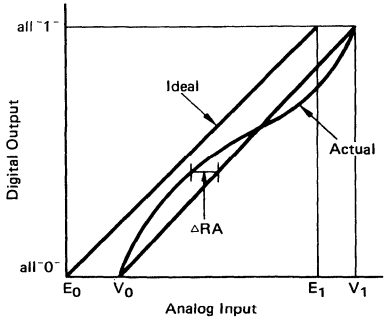


Relative Accuracy:
Deviation between a straight line from the zero point of the device (all "0") to the full-scale point (all 'L') and an actual conversion characteristic curve.

Gain Error:
Difference between an ideal input voltage span and an actual input voltage span. In the MB4051, according to the procedure described separately, it is possible to adjust the gain error to zero.

Offset Error:
Difference between an ideal cirtical input voltage which makes all output bits zero and an actual critical input voltage. In the MB4051, such offset error can be adjusted according to the procedure described separately.

RELATIVE ACCURACY/GAIN
ERROR/OFFSET ERROR



*: Relative Accuracy = ΔRA

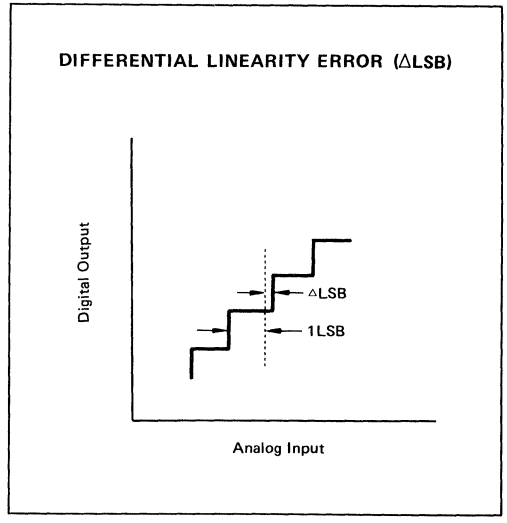
$$\text{Gain Error} = \frac{(V_1 - V_0) - (E_1 - E_0)}{\text{FSR}} \times 100 \text{ (\% of FSR)}$$

$$\text{Offset Error} = \frac{V_0 - E_0}{\text{FSR}} \times 100 \text{ (\% of FSR)}$$

7

DEFINITION OF TERMS (Continued)

Differential Linearity Error:
Input voltage deviation from an ideal input voltage which is necessary to change the output code as large as 1LSB. The differential linearity error of ±1/2LSB means that, when the input signal changes 1/2LSB to 3/2LSB, digital code varies 1LSB.



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Example of Output Coding

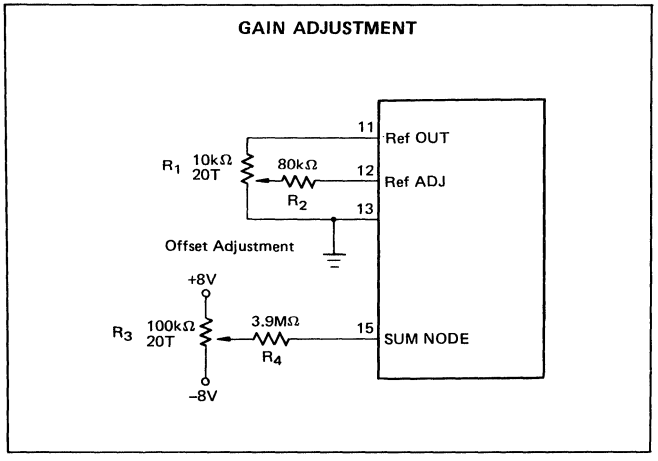
Scale	Input Voltage	MSB	D1	D2	D3	D4	D5	D6	D7	D8	LSB
FS-1LSB	6.4937	1	1	1	1	1	1	1	1	1	1
FS/2	3.2500	1	0	0	0	0	0	0	0	0	0
FS/4	1.6250	0	1	0	0	0	0	0	0	0	0
FS/8	0.8125	0	0	1	0	0	0	0	0	0	0
FS/16	0.4063	0	0	0	1	0	0	0	0	0	0
FS/32	0.2031	0	0	0	0	1	0	0	0	0	0
FS/64	0.1016	0	0	0	0	0	1	0	0	0	0
FS/128	0.0508	0	0	0	0	0	0	1	0	0	0
FS/256	0.0254	0	0	0	0	0	0	0	1	0	0
FS/512	0.0127	0	0	0	0	0	0	0	0	1	0
FS/1024 = 1LSB	0.0063	0	0	0	0	0	0	0	0	0	1
0	0.0000	0	0	0	0	0	0	0	0	0	0

APPLICATIONS INFORMATION

ADJUSTMENT OF OFFSET AND GAIN

In the MB4051, Both gain-error and offset-error can be adjusted to zero by trimmers connected as shown below. In this case, potentiometers and resistors for trimmers should have temperature characteristics below 100 ppm/°C to ensure long-term stability and less temperature drift.

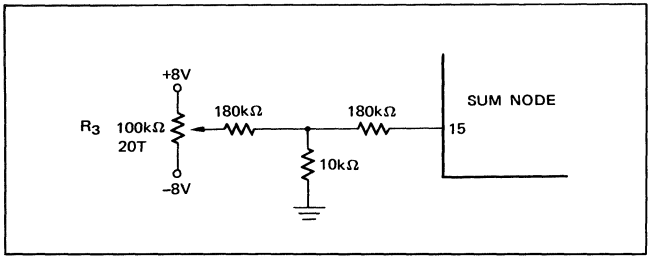
The following external adjustment circuits should be located as near as possible to the package.



Offset Adjustment

By applying the voltage of 1/2LSB, i.e., 3.2mV to an analog input channel, continuously execute AD conversion of the applied input voltage. Then, adjust potentiometer R_3 during the conversion so that the conversion results become "0000000000" and "0000000001", alternatively. The range of adjustment is about ±0.2% of FSR in the circuit shown below.

The R_4 resistor for offset adjustment can be replaced with smoller resistors as follows.



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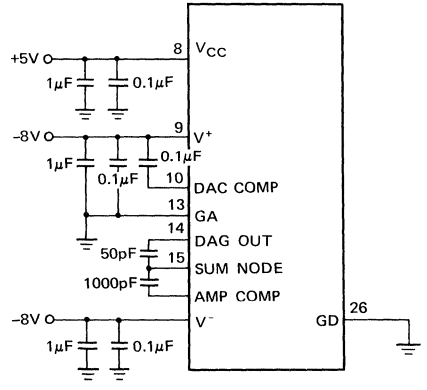
GAIN ADJUSTMENT

After offset adjustment, by applying FSR-3/2LSB (6.4905V) to an analog input, execute AD conversion of the applied input voltage. Then, adjust potentiometer R_1 during the conversion so that the conversion results become "1111111111" and "1111111110", alternatively. The range of adjustment is about −12% to +5% of FSR in the circuit shown.

PRECAUTIONS FOR CIRCUIT STABILIZATION

To stabilize the ADC operation and by-pass power supply line noise, connect the external capacitors as shown.

CAPACITORS FOR STABILIZATION AND POWER SUPPLY BYPASS

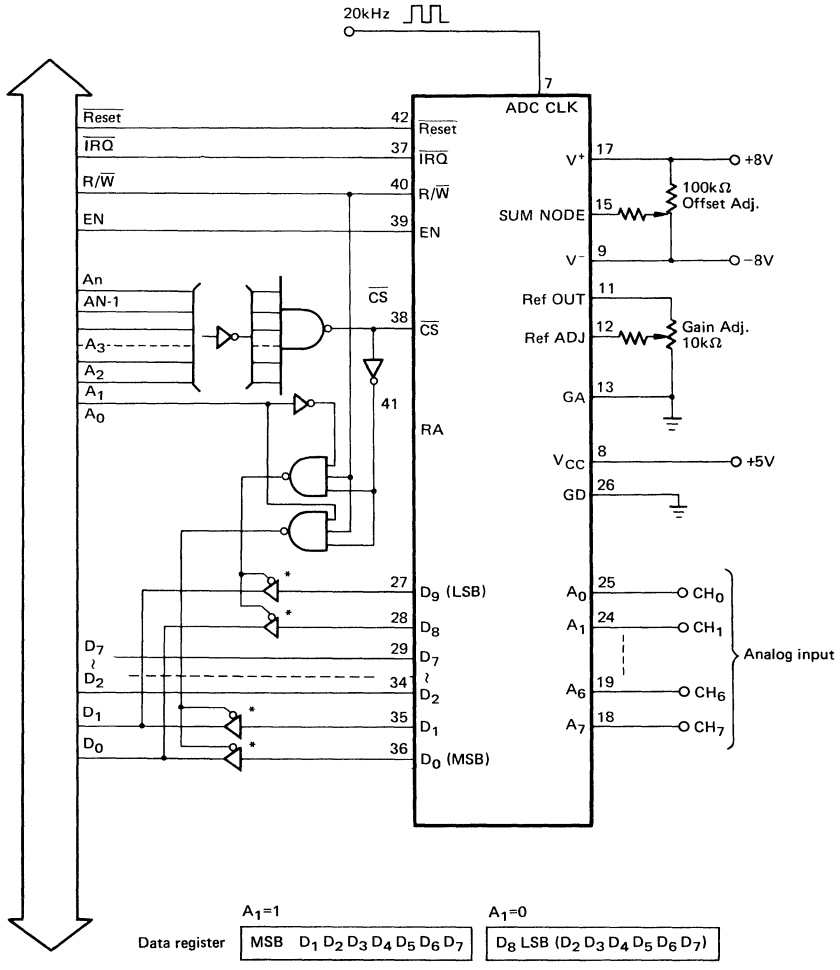


Bypass capacitor for filtering line-noise should have good high-frequency characteristics and should be connected as near as possible to the package.

If a printed circuit board is used, the ground-line should be made as wide as possible and the pattern should be made in such a manner that the analog input signal line does not pick up noise from the digital signal and so on. Unused digital input should be kept in an inactive state listed below and unused analog input should be connected to analog ground (GA).

Inactive State	Terminals
"L"	EN, RA, R/$\overline{W}$, DE, B_0 to B_2
"H"	$\overline{Reset}$, $\overline{CS}$, $\overline{START}$

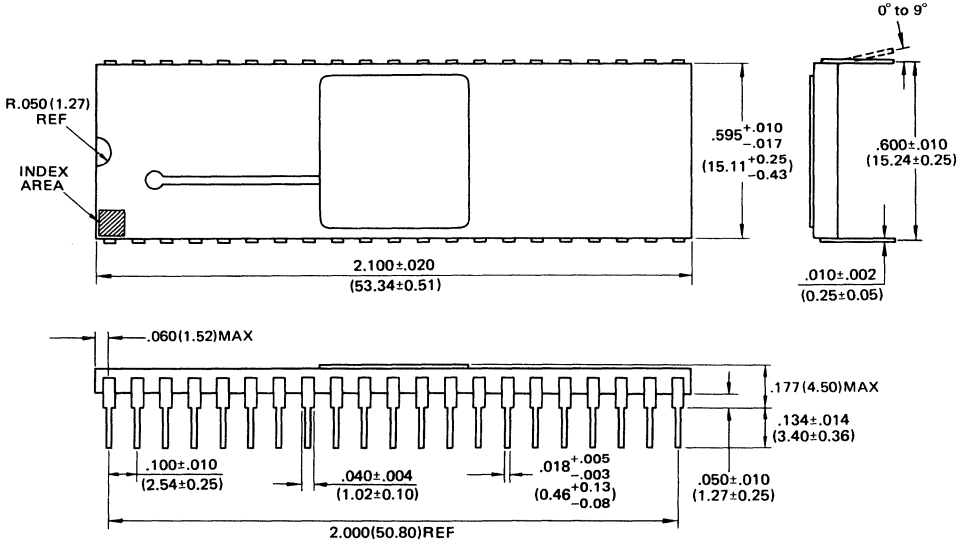
EXAMPLE OF INTERFACE TO 8-BIT MPU
(PROVIDE A CHANGE CIRCUIT FOR UPPER 2-BITS)



NOTE: * MB74LS367 or MB487x1

PACKAGE DIMENSIONS

42-LEAD CERAMIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-42C-A01)



Dimensions in inches (millimeters)

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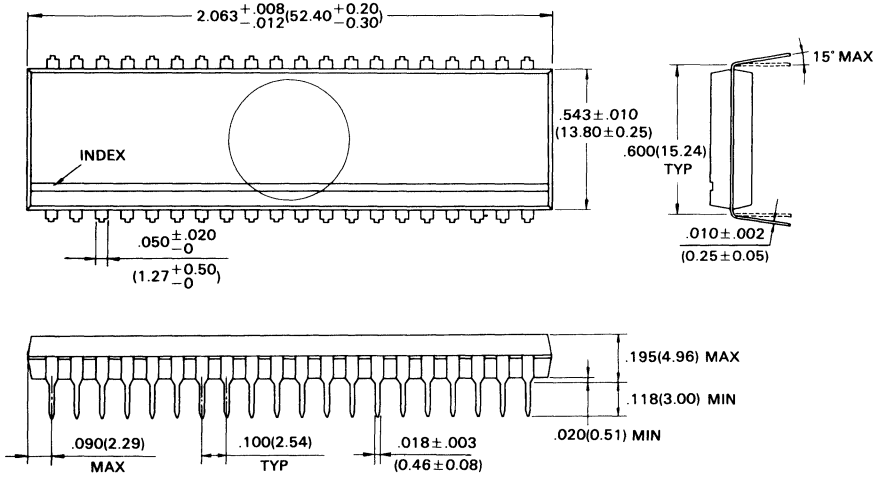
PACKAGE DIMENSIONS (continued)

40-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No.: DIP-40P-M01)



Dimensions in
inches (millimeters)

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7

FUJITSU

4-CHANNEL 8-BIT A/D CONVERTER

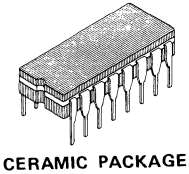
MB4052

July 1988
Edition 4.0

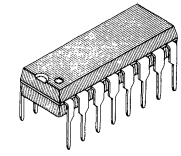
4-CHANNEL 8-BIT A/D CONVERTER SUBSYSTEM

The Fujitsu MB 4052 is an analog-to-digital converter (ADC) for general purpose which features four channels of analog inputs and 8-bit data length of digital output.
Analog input signal is converted to serial 8-bit digital data by the successive-approximation technique which provides high-speed conversion, i.e. many analog data can be converted within a short time.
All digital I/O signals including control inputs are TTL level compatible so as to provide wide application such as in microprocessor-controlled system and so on.

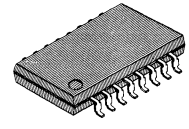
- Single Power Supply;
  DIP: +3.5V to +6.0V or +8.0V to +18V (with Internal Regulator)
  FPT: +3.5V to +6.0V or +8.0V to +13.2V (with Internal Regulator)
- Multiplex 4-Channel Analog Inputs
- Analog Input Voltage Ranges:
  0 to $1/2V_{CC1}$ (Standard mode: RS = 1)
  0 to $1/8V_{CC1}$ (Contracted mode: RS = 0)
  0 to $2V_{CC1}$ (Expanded mode: through built-in Divider)
- Analog Input Bias Current: 250nA Max.
- Resolution: 8 bits
- Linearity: 0.19% Max.
- Successive-Approximation Conversion: 100μs/ch Max. at f_{CLK} = 100 kHz
- Ratio-Metric Conversion by Reference Voltage V_{CC1}
- Serial Data Output (Open-Collector)
- TTL/CMOS Compatible Digital I/O
- Package: DIP-16C-C02
  DIP-16P-M04
  FPT-16P-M03



CERAMIC PACKAGE
DIP-16C-C02

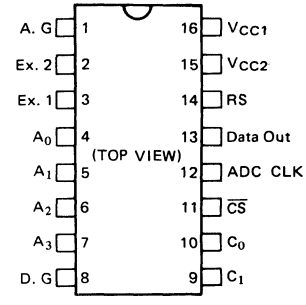


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M03

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (All Voltages referenced to A.G/D.G)

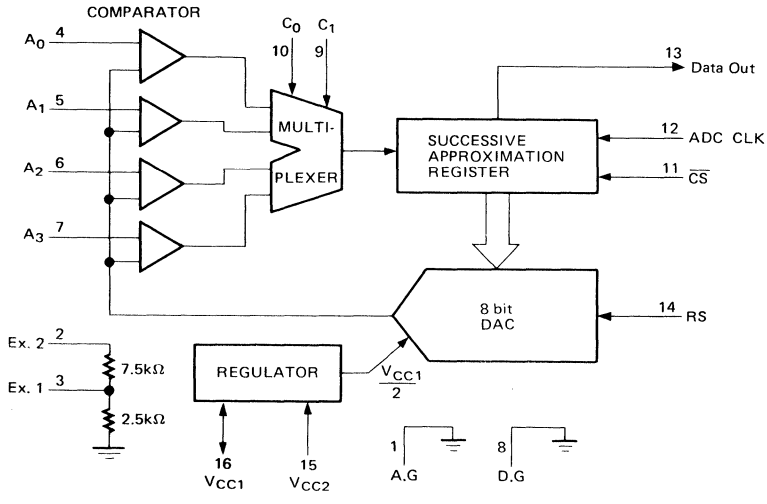
Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC1}	+7	V
		V_{CC2}	+20	V
Digital Input Voltage		V_{ID}	−0.5 to +20	V
Digital Output Voltage (Off-State)		V_{OH}	+20	V
Analog Input Voltage		V_{IA}	V_{CC1}+0.5	V
Storage Temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic		−40 to +125	

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

7

Fig. 1– MB 4052 BLOCK DIAGRAM



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RECOMMENDED OPERATING CONDITIONS

(T_A = –30°C to +85°C)

Parameter	Symbol		Value			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC1}		3.5	5.0	6.0	V
	V_{CC2}	DIP	8.0	12.0	18.0	V
		FPT	8.0	12.0	13.2	V
Digital Output Low Current	I_{OL}		–	–	8	mA
Operating Temperature	T_A		–30	–	+85	°C

PIN DESCRIPTIONS

INPUT FOR VOLTAGE RANGE EXPANSION (EX 2), PIN 2
This input pin is provided to expand the voltage range of analog input signal.
This input pin is connected to the internal one-to-four voltage divider which reduces an analog signal level to one fourth of input level.

OUTPUT FOR VOLTAGE RANGE EXPANSION (EX 1), PIN 3
This output pin is provided to expand the allowable analog input level in co-operation with the above EX 2 pin.
A reduced signal which is divided in the internal divider is output on this pin.
This output pin can be connected to any of standard analog inputs A_0, A_1, A_2 or A_3 so that the EX 2 pin can function as one of 4-channel inputs.

ANALOG INPUTS (A_0 TO A_3), PINS 4, 5, 6 AND 7
These input pins are provided to receive four channels of analog inputs.
One of these four channels is selected by a combination of C_0 and C_1 inputs.

CHANNEL SELECT (C_1 AND C_0), PINS 9 AND 10
These control inputs are used to designate one of four analog inputs as shown in Table 1.

Table 1 CHANNEL SELECTION

C_1	C_0	Channel
0	0	A_0
0	1	A_1
1	0	A_2
1	1	A_3

CHIP SELECT ($\overline{CS}$), PIN 11
This control input pin is used to start analog-to-digital conversion.
When $\overline{CS}$ goes low, the A/D conversion start and the DATA OUT output is enabled.
When an A/D conversion is completed or termination of conversion is required, $\overline{CS}$ is made high.

A/D CONVERSION CLOCK (ADC CLK), PIN 12
This clock signal is input to the internal successive approximation register and used as timing signal for A/D conversion.
The conversion speed of this device is determined by this clock rate.
Ten clock cycles are required for a complete 8-bit conversion.
A precise cycle time is not always required for this clock signal.

DATA OUTPUT (DATA OUT), PIN 13
This output pin is provided to output the A/D conversion results as digital signals.
The converted digital data are serially output in the order of start-bit, MSB (Most Significant Bit), 2SB (Second Significant Bit), . . . , 7SB, LSB (Least Significant Bit) and stop-bit in synchronization with the ADC CLK clock signal.

RANGE SELECT (RS), PIN 14
This control input is provided to select an analog input voltage range as shown in Table 2.
This input must not be changed during an A/D conversion.

Table 2 RANGE SELECTION

RS	Voltage Range
0	0 to 1/8 V_{CC1}
1	0 to 1/2 V_{CC1}

ANALOG GROUND (A.G) AND DIGITAL GROUND (D.G), PINS 1 AND 8
These are terminals for ground.
The analog circuitry and digital circuitry have seperate ground terminals, respectively.

POWER SUPPLIES (V_{CC2} AND V_{CC1}), PINS 15 AND 16
When the device operates within a voltage range of 3.5V to 6.0V, the power source is connected to V_{CC1} which is shorted to V_{CC2}.
When the device operates within a voltage range of 8V to 18V in case of DIP Packages and 8V to 13.2V in case of Flat Package, the power source is connected to V_{CC2}.
In this high voltage operation mode, the V_{CC1} pin is used as an output pin which supplies +5V stabilized voltage and 10mA load current and the supplied voltage is regurated in the internal voltage regurator.
V_{CC1} is used as the reference voltage of A/D conversion regardless any two types voltage.

7

ANALOG CIRCUIT CHARACTERISTICS FOR PLASTIC DIP PACKAGE

(V_{CC1} = 3.5V to 6.0V, T_A = -30°C to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Resolution			–	–	–	8	Bit
Linearity Error			V_{CC1} = 5V	–	–	±0.5	LSB
Differential Linearity Error				–	–	±0.9	LSB
Zero Transition Voltage	Contracted Range	V_{ZC}	V_{CC1} = 5V, T_A = 25°C	0	6	16	mV
	Standard Range	V_{ZS}		7	17	27	mV
	Expanded Range	V_{ZE}		22	62	102	mV
Full Scale Transition Voltage	Contracted range	V_{FC}		600	625	650	mV
	Standard Range	V_{FS}		2.475	2.500	2.525	V
	Expanded Range	V_{FE}		9.600	10.000	10.400	V
Comparator Input Current		I_{IC}	V_{CC1} = 5V	–	-100	-250	nA
Divider Input Resistance for Expanded Range		R_{INE}	–	5	10	15	kΩ
Regulator	Output Voltage	V_{OR}	8V ≤ V_{CC2} ≤ 18V	4.5	5.0	5.5	V
	Line Regulation			–	4.0	–	mV/V
	Load Regulation		V_{CC2} = 12V, 0mA ≤ I_{out} ≤ -10mA	–	0.5	–	mV/mA
	Output Voltage Temperature		V_{CC2} = 12V	–	50	–	ppm/°C
Conversion Cycle Time		t_{CYC}	f_{CLK} = 100kHz	–	–	100	μs/ch

A minus sign (–) prefixed to a current value indicates that the current flows from the IC to the external circuit.

ANALOG CIRCUIT CHARACTERISTICS FOR CERAMIC DIP PACKAGE

(V_{CC1} = 3.5V to 6.0V, T_A = −30°C to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Resolution			–	–	–	8	Bit
Linearity Error			V_{CC1} = 5V	–	–	±0.4	LSB
Differential Linearity Error				–	–	±0.8	LSB
Zero Transition Voltage	Contracted Range	V_{ZC}	V_{CC1} = 5V, T_A = 25°C	0	6	16	mV
	Standard Range	V_{ZS}		7	17	27	mV
	Expanded Range	V_{ZE}		22	62	102	mV
Full Scale Transition Voltage	Contracted range	V_{FC}		610	625	640	mV
	Standard Range	V_{FS}		2.480	2.500	2.520	V
	Expanded Range	V_{FE}		9.760	10.000	10.240	V
Comparator Input Current		I_{IC}	V_{CC1} = 5V	–	−100	−250	nA
Divider Input Resistance for Expanded Range		R_{INE}	–	5	10	15	kΩ
Regulator	Output Voltage	V_{OR}	8V ≤ V_{CC2} ≤ 18V	4.5	5.0	5.5	V
	Line Regulation			–	4.0	–	mV/V
	Load Regulation		V_{CC2} = 12V, 0mA ≤ I_{out} ≤ −10mA	–	0.5	–	mV/mA
	Output Voltage Temperature		V_{CC2} = 12V	–	50	–	ppm/°C
Conversion Cycle Time		t_{CYC}	f_{CLK} = 100kHz	–	–	100	μs/ch

A minus sign (−) prefixed to a current value indicates that the current flows from the IC to the external circuit.

7

ANALOG CIRCUIT CHARACTERISTICS FOR PLASTIC FLAT PACKAGE

(V_{CC1} = 3.5V to 6.0V, T_A = -30°C to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Resolution			–	–	–	8	Bit
Linearity Error			V_{CC1} = 5V	–	–	±0.5	LSB
Differential Linearity Error				–	–	±0.9	LSB
Zero Transition Voltage	Contracted Range	V_{ZC}	V_{CC1} = 5V, T_A = 25°C	0	6	16	mV
	Standard Range	V_{ZS}		7	17	27	mV
	Expanded Range	V_{ZE}		22	62	102	mV
Full Scale Transition Voltage	Contracted range	V_{FC}		600	625	650	mV
	Standard Range	V_{FS}		2.475	2.500	2.525	V
	Expanded Range	V_{FE}		9.600	10.000	10.400	V
Comparator Input Current		I_{IC}	V_{CC1} = 5V	–	-100	-250	nA
Divider Input Resistance for Expanded Range		R_{INE}	–	5	10	15	kΩ
Regulator	Output Voltage	V_{OR}	8V ≤ V_{CC2} ≤ 18V	4.5	5.0	5.5	V
	Line Regulation			–	4.0	–	mV/V
	Load Regulation		V_{CC2} = 12V, 0mA ≤ I_{out} ≤ -10mA	–	0.5	–	mV/mA
	Output Voltage Temperature		V_{CC2} = 12V	–	50	–	ppm/°C
Conversion Cycle Time		t_{CYC}	f_{CLK} = 100kHz	–	–	100	μs/ch

A minus sign (–) prefixed to a current value indicates that the current flows from the IC to the external circuit.

DIGITAL CIRCUIT DC CHARACTERISTICS

(V_{CC1} = 3.5V to 6.0V, T_A = -30°C to +85°C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Input Clamp Voltage	V_{IC}	V_{CC1} = 3.5V, I_{IL} = -18mA	–	–	-1.5	V
High Level Input Current	I_{OH}	V_{CC1} = 3.5V, V_{IH} = 2.0V, V_{IL} = 0.8V, V_{OH} = 20V	–	–	100	μA
Low Level Output Voltage	V_{OL1}	V_{CC1} = 3.5V, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OL} = 4mA	–	–	0.4	V
	V_{OL2}	V_{CC1} = 3.5V, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OL} = 8mA	–	–	0.5	V
High Level Input Current	I_{IH1}	V_{CC1} = 6.0V, V_{IH} = 2.7V	–	–	20	μA
	I_{IH2}	V_{CC1} = 6.0V, V_{IH} = 20V	–	–	100	μA
Low Level Input Current	I_{IL}	V_{CC1} = 6.0V, V_{IL} = 0.4V	–	-50	-150	μA
Power Supply Current for V_{CC1}	I_{CC1}	V_{CC1} = 6.0V	–	15*	30	mA
Power Supply Current for V_{CC2}	I_{CC2}	V_{CC1} = Open, V_{CC2} = 20V for DIP Package V_{CC2} = 13.2V for FLAT Package	–	15	25	mA

***Note:** This typical value is measured at V_{CC1} = 5.0V and T_A = 25°C.
A minus sign (–) prefixed to a current value indicates that the current flows from the IC to the external circuit.
The values are measured at V_{CC1} = V_{CC2} except the I_{CC2} parameter of .

DIGITAL CIRCUIT AC CHARACTERISTICS

(V_{CC1} = 3.5V to 6.0V, T_A = -30°C to +85°C)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
ADC CLK Cycle Time	t_{CY}	10	–	–	μs
ADC CLK H Level Pulse Width	t_{WAC+}	2.5	–	–	μs
ADC CLK L Level Pusle Width	t_{WAC-}	2.5	–	–	μs
$\overline{CS}$ H Level Pulse Width	t_{WCS+}	1.5	–	–	μs
$\overline{CS}$ Set-up Time	t_{SCS}	1	–	–	μs
$\overline{CS}$ Hold Tin.	t_{HCS}	1	–	–	μs
Channel Set-up Time	t_{SCH}	0	–	–	μs
Channel Hold Time	t_{HCH}	1	–	–	μs
Propagation Delay Time	t_{PLH} t_{PHL}	–	800	2,000	ns

7

Fig. 2 – AC CHARACTERISTICS WAVEFORM

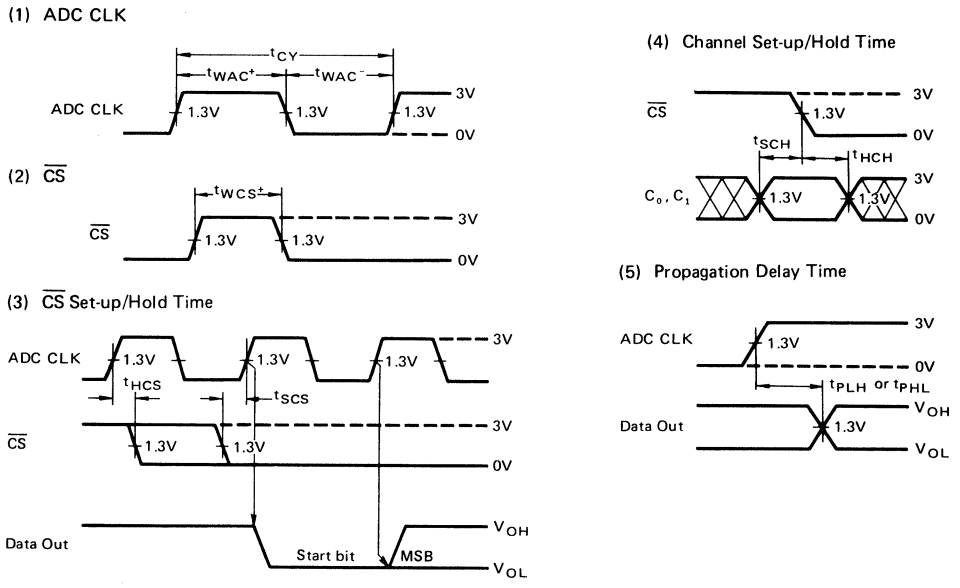
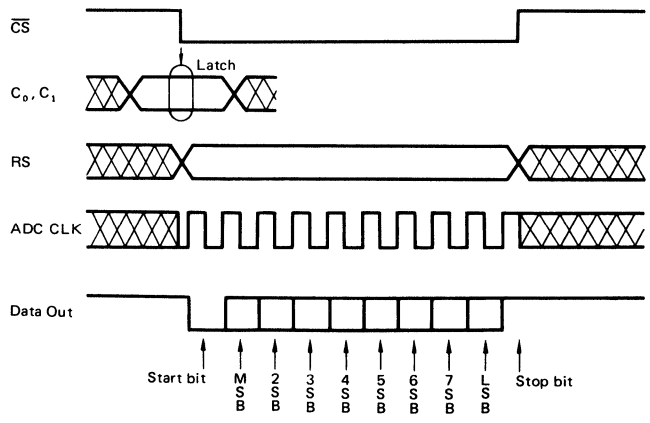
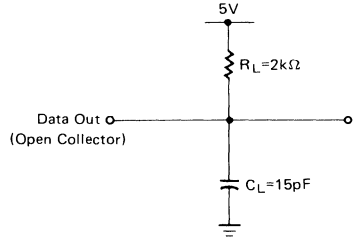


Fig. 3 – TIMING DIAGRAM



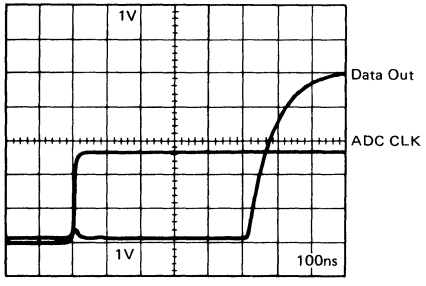
Note: RS should be held to one ranged "1" or "0" until data conversion is completed.

Fig. 4 – LOAD CONDITIONS

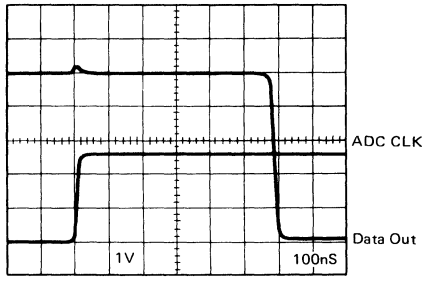


TYPICAL WAVEFORMS OF PROPAGATION DELAY

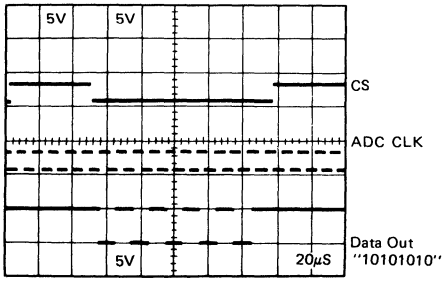
t_{PLH} (Data Out Transition from low-level to high-level)



t_{PHL} (Data Out Transition from high-level to low-level)



TYPICAL CONVERSION WAVEFORM



Condition
f_{CLK} = 100kHz
V_{CC1} = 5V
Standard Range
V_{IA} ≒ 1663 mV

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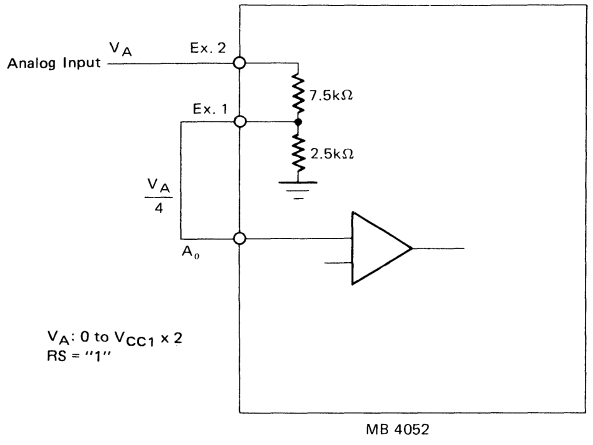
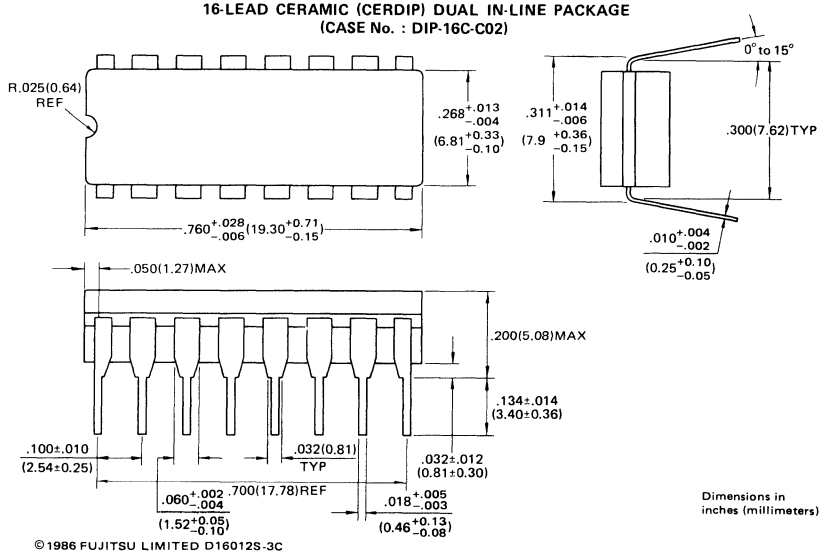
Fig. 5 – EXAMPLE OF EXPAND RANGE MODE CONNECTION



7

PACKAGE DIMENSIONS

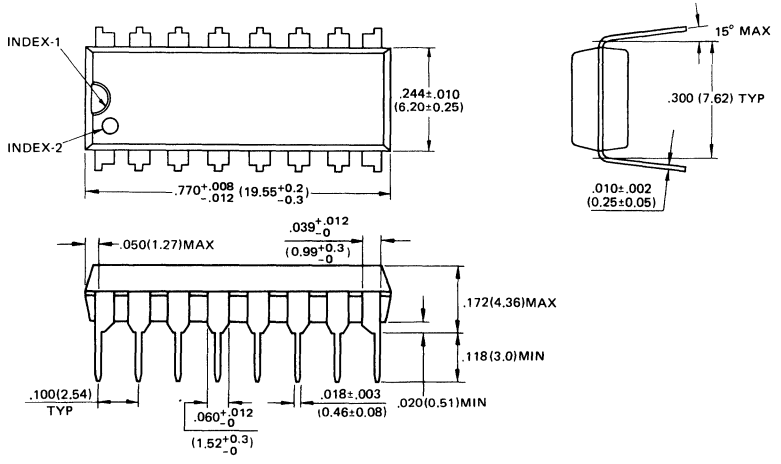
16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-16C-C02)



Dimensions in inches (millimeters)

7

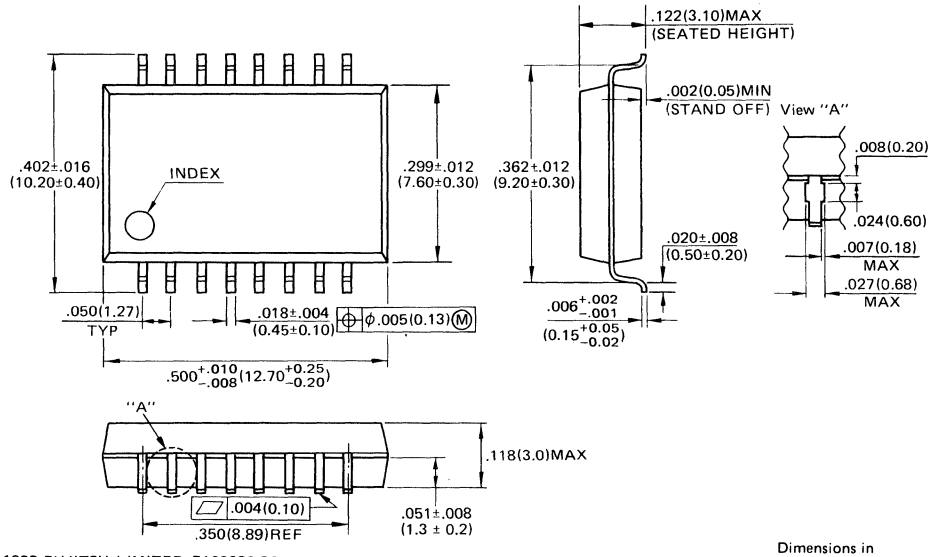
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)



Dimensions in inches (millimeters)

PACKAGE DIMENSIONS (continued)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M03)



Dimensions in
inches (millimeters)

7

FUJITSU

6-CHANNEL 8-BIT AID CONVERTER SUBSYSTEM

MB 4053
MB 4063

May 1986
Edition 3.0

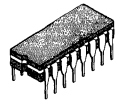
6-CHANNEL 8-BIT A/D CONVERTER SUBSYSTEM

The Fujitsu MB 4053 and MB 4063 are 6-channel, 8-bit, single-slope A/D converter subsystem designed to be used in a microprocessor based data control system. These devices provide the analog functions while the addressing, counting and timing functions are provided by a microprocessor such as the MB 8840/50, MBL 8048, MBL 8086, or MBL 8088.

The MB 4053 and MB 4063 are single monolithic bipolar IC providing a 1 of 8 address decoder, 8-channel analog multiplier, sample and hold, constant current generator, ramp integrator and comparator in a 16-pin package.

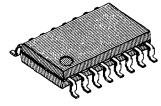
These A/D converter subsystems are suitable for a wide range of applications. The resolution required by an application can be obtained by arbitrarily selecting a suitable integration time. Also zero offset and full-scale error corrections can be made automatically (auto-zero and auto-calibration) to minimize conversion error.

- Microprocessor/TTL compatible
- Zero offset and full-scale error correction capability
- Ratiometric conversion capability
- Available in 16-pin DIP and Flat Pack
- Compatible with MC14443 and μA9708 (DIP package)
- Single power supply : +4.75 V to +15 V
- Excellent linearity : ±0.2% max. error
- Fast conversion time : 300 μs/ch typ.
- Analog input volgage : 0 V to V_{CC} − 2 V (5.25 V max.)
- Power Dissipation : 25 mW typ. at V_{CC} = 5 V
- Standard 16-pin DIP or flat package.



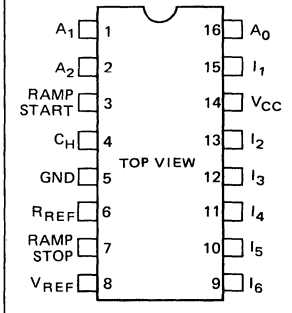
CERAMIC PACKAGE
DIP-16C-C02

CERAMIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Supply Voltage		V_{CC}	18	V
Digital Input Voltage		V_{ID}	-0.5 to +30	V
Digital Output Voltage when Off		V_{OH}	-0.5 to +18	V
Analog Input Voltage		V_{IA}	-0.5 to +30	V
Output Current		I_O	10	mA
Storage Temperature	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Fig. 1a – MB 4053 BLOCK DIAGRAM

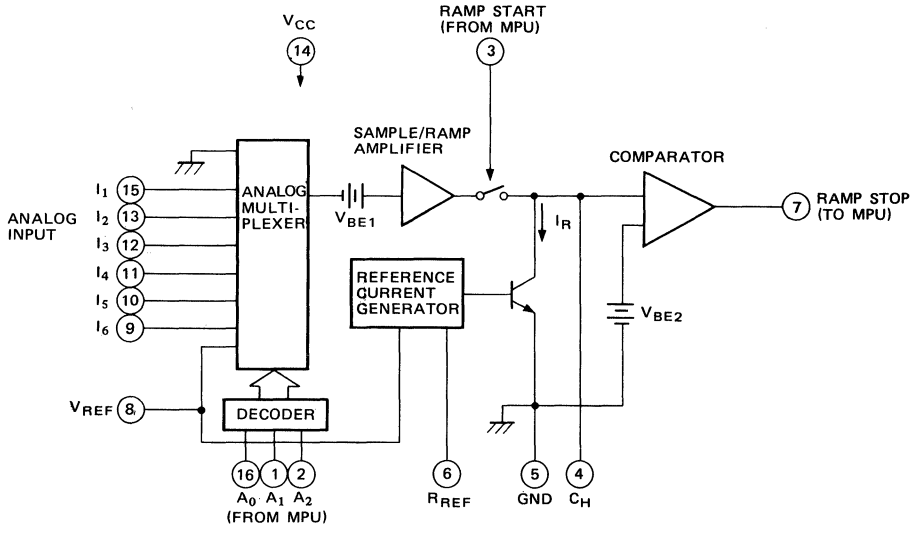
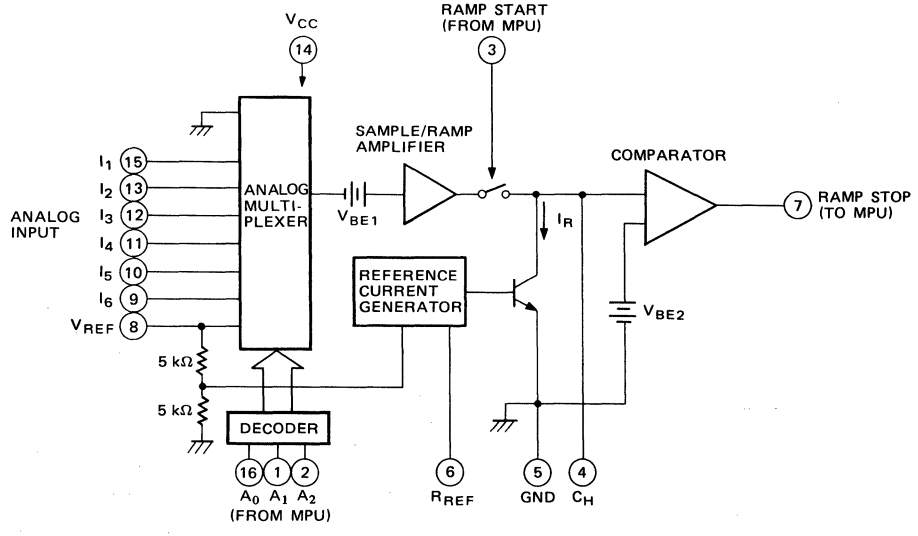


Fig. 1b – MB 4063 BLOCK DIAGRAM



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RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Condition			Unit
			Min.	Typ.	Max.	
Supply Voltage		V_{CC}	4.75	5.0	15	V
Reference Voltage*	MB 4053	V_{REF}	2.0		5.25	V
	MB 4063		2.8			
Ramp Capacity		C_H	300			pF
Reference Current		I_R	12		50	μA
Analog Input Voltage		V_{IA}	0		V_{REF}	V
Output Current		I_O			1.6	mA
Operating Temperature		T_A	-40		+85	°C

NOTE: *$2V \leqq V_{REF} \leqq V_{CC}-2V$ for MB 4053, $2.8V \leqq V_{REF} \leqq V_{CC}-2V$ for MB 4063

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75 V to 15 V, T_A = -40°C to 85°C)

Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Conversion Error	E_A		±0.2	±0.3	%	†1
Linearity Error	E_R		±0.08	±0.2	%	†2
Analog Input Current	I_B		-50	-250	nA	
Crosstalk Between Any Two Channels	V_{CR}	60			dB	†3
Multiplexer Input Offset Voltage	V_{OSM}		2.0	4.0	mV	
Conversion Time	t_C		296	350	μs/ch	See test circuit Analog input: 0 thru V_{REF} C_H = 3300 pF, I_R = 50 μA
Acquisition Time	t_A		20	40	μs	See test circuit C_H = 1000 pF †4
Acquisition Current	I_A	150			μA	
Ramp Start Delay Time	t_O		100		ns	
Multiplexer Address Time	t_M		1		μs	
Digital High Level Input Voltage	V_{IH}	2.0			V	
Digital Low Level Input Voltage	V_{IL}			0.8	V	
Digital Low Level Input Current	I_{IL}		-5	-15	μA	V_{IL} = 0.4 V
Digital High Level Input Current	I_{IH}			1	μA	V_{IH} = 5.5 V
High Level Output Current	I_{OH}			10	μA	V_{OH} = 15 V
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 1.6 mA
Supply Current	I_{CC}		5	10	mA	

A minus sign (–) prefixing a current value indicates that the current flows from the IC to the external circuit.

†1 Conversion error: For all channels, deviation from a straight line between two points obtained by channel addresses 000 (0 scale) and 111 (full scale).

†2 Linearity error: Deviation from a straight line between the 0 and full scale points for each channel.

†3 Crosstalk between channels: Voltage change V_{CH} of C_H terminal occurring when an input voltage of a channel is changed by $\triangle V_I$ while another channel is already charged (RAMP START = 0). This calculated by $20 \log \frac{\triangle V_{CH}}{\triangle V_I}$.

†4 Acquisition time: Sum of multiplexer delay time, RAMP START delay time, and time required to charge the selected input voltage to the ramp capacitor.

7

Fig. 2 – CONVERSION ERROR

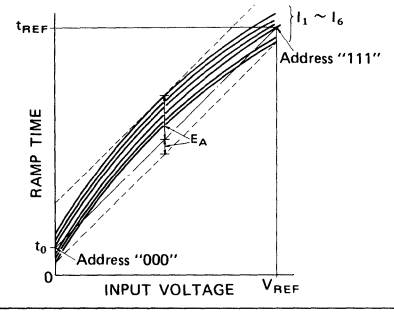


Fig. 3 – LINEARITY ERROR

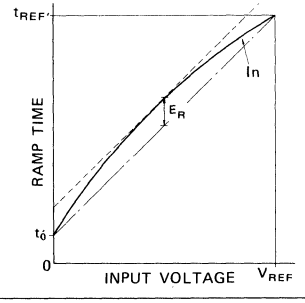
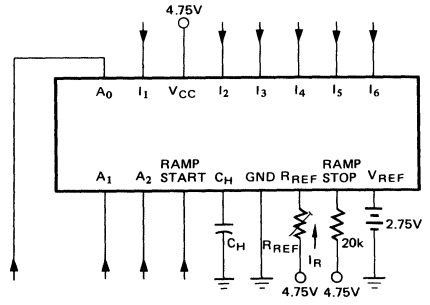


Fig. 4 – ACQUISITION/CONVERSION TIME TEST CIRCUIT

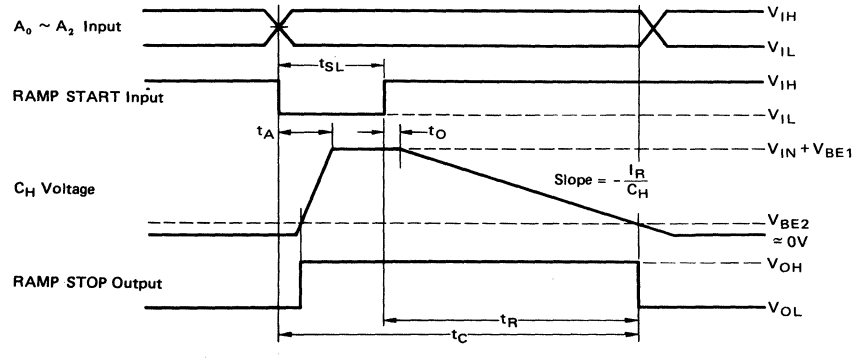


Adjust R_{REF} in the range 40 to 200 kΩ so that I_R is 12 to 50 μA.

CHANNEL SELECTION

Input address line			Selected analog input
A_2	A_1	A_0	
0	0	0	GND
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	V_{REF}

Fig. 5 – TIMING CHART



OPERATION DISCRIPTION

Refer to Fig. 1 MB 4053/MB 4063 BLOCK DIAGRAM, and Fig. 5 Timing Chart. Address inputs A_0 to A_2 are used to select the analog input to be converted, (one of the six analog inputs I_1 to I_6). The RAMP START input is switched from a logic 1 to a logic zero. This causes the external ramp capacitor C_H to charge at a fixed rate. (Note 1) until it reaches the sum of the selected analog input voltage and a constant offset voltage V_{BE1}. The RAMP STOP output (open-collector switches from a logic 0 to logic 1 when the voltage on C_H reaches the comparator reference voltage V_{BE2}. The RAMP START input is switched back to a logic 1 after C_H is completely charged. This disconnects the analog input from C_H and allows it to be gin discharging at a fixed rate (Note 2). When the voltage on C_H reaches the comparator reference voltage V_{BE2} the RAMP STOP output switches back to a logic 0. This completes a conversion cycle for 1 channel.

The time between the RAMP START input switching (0→1) and RAMP STOP output switching (1→0) is the RAMP TIME t_R. This would be directly proportional to the analog input voltage for the ideal situation where there was no comparator switching level error, leakage, switching delay times or effect of the impedance of the internal reference current source. t_R can be calculated for the ideal case as follows:

$$t_R = V_{IN} \times \frac{C_H}{I_R}$$

Where: V_{IN} = Analog input voltage to be measured
C_H = External ramp capacitor

$$I_R = \frac{V_{CC} - V_{REF}}{R_{REF}} \text{ for MB 4053}$$

$$I_R = \frac{V_{REF}}{2 - R_{REF}} \text{ for MB 4063}$$

This ramp time is converted to a digital representation by counting t_R with the microprocessor. If a small error can be tolerated, the A/D conversion software can be reduced and the conversion time minimized by omitting corrections.

NOTE:

*1 Charge slope $= \frac{I_A - I_R}{C_H} \geqq \frac{150\mu A - I_R}{C_H}$

Where: I_A is the acquisition current whose value is determined from the circuit constant in the IC.

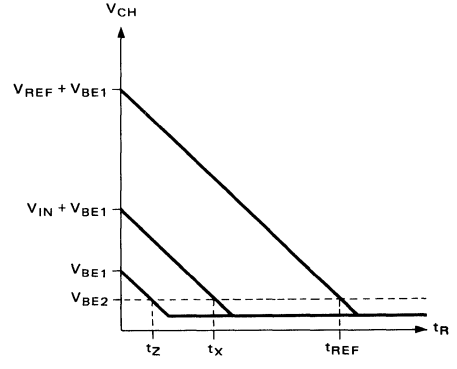
*2 Discharge slope $= -\frac{I_R}{C_H}$

ZERO OFFSET AND FULL-SCALE FACTOR CORRECTIONS

High precision conversions can be achieved by correcting for zero offset and full scale factor as follows:

The channel select address (A_0 to A_2) is set to 000. Ground (GND) is selected (internally) as the analog input and converted. This results in ramp time t_R. Next the address is set to 111. V_{REF} is selected (internally) and converted. This results in ramp time, t_{REF}. Finally the desired analog input (one of I_1 to I_6) is selected and converted. This results in ramp time t_X. This conversion sequence is arbitrary and the GND and V_{REF} conversions are not needed each time a channel is converted but only as required for calibration. The relationships between the inputs and ramp times are shown below.

$$(V_{BE1})_C = t_Z$$
$$(V_{REF} + V_{BE1})_C = t_{REF}$$
$$(V_{IN} + V_{BE1})_C = t_X$$
$$(V_{REF})_C = t_{REF} - t_Z$$
$$(V_{IN})_C = t_X - t_Z$$
$$\frac{(V_{IN})_C}{(V_{REF})_C} = \frac{t_X - t_Z}{t_{REF} - t_Z}$$



The conversion error can then be minimized by using the above results in the expression below to calculate the corrected analog input voltage.

$$(V_{IN})_C = (V_{REF})_C \times \frac{t_X - t_Z}{t_{REF} - t_Z}$$

Where: V_{IN} = Analog input voltage to be measured
V_{REF} = Reference voltage
V_{BE1} = Shift voltage in sample/ramp amplifier
V_{BE2} = Threshold voltage of comparator
V_{CH} = C_H voltage

The GND and V_{REF} conversion sequence is arbitrary, the GND and V_{REF} conversions not being needed each time a channel (I_1 to I_6) is converted.

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PIN DESCRIPTION

Pin number	Name	Symbol	Function
9 ~ 13 15	Analog input	I_1 thru I_6	Analog inputs for the six channels. One of the 6 is selected by a specific bit pattern on A_0 to A_2.
16 1 2	Channel selection input	A_0 A_1 A_2	Inputs for selecting an analog input channel. Either GND, one of channels I_1 to I_6 or V_{REF} is selected by a specific bit pattern on the 3 inputs.
3	RAMP START signal input	RAMP START	A/D conversion start signal input. RAMP START (1→0) Ramp time start signal input. RAMP START (0→1)
7	RAMP STOP signal output	RAMP STOP	Indicates that C_H is charged over comparator reference voltage V_{BE2}. RAMP STOP (0→1) A/D conversion end signal (C_H discharged to comparator reference voltage). RAMP STOP (0→1)
4	Ramp capacitor pin	C_H	Pin for externally connecting the ramp capacitor. The value of C_H in conjunction with V_{REF} and R_{REF} establishes the ramp time.
8	Reference voltage supply pin	V_{REF}	Reference voltage supply pin. This is the reference voltage source for determining the discharge current and the analog reference voltage for full-scale factor correction. When the channel selection input is set to 111, this pin is selected for channel conversion. The full-scale factor is corrected using the conversion results. The voltage at this pin must be set to (GND + 2 V) to (V_{CC} - 2 V) and 5.25 V or less.
6	Reference resistance pin	R_{REF}	Pin for external reference resistance for setting the discharge current.
			MB 4053: The external resistance is connected between the power source pin (V_{CC}) and the reference resistance pin (R_{REF}). The discharge current is, then, $I_R = (V_{CC} - V_{REF})/R_{REF}$.
			MB 4053: The external resistance is connected between the reference voltage supply pin (V_{REF}) and the reference resistance pin (R_{REF}). The discharge current is, then $I_R = V_{REF}/2R_{REF}$.
14	Power supply	V_{CC}	Power supply pin
5	Ground	GND	Ground pin This pin is grounded. When the channel selection input is set to 000, this terminal is selected for channel conversion. The zero offset is corrected using the conversion results.

NOTES ON USE

1. Since the impedance of th ramp capacitor pin is approximately 30 MΩ (high), a resistance must not be connected in paralleled with this input. A ramp capacitor with no leakage must be used.
2. At V_{IN} = 0 V, t_R has a finite value.
3. Since RAMP STOP is an open collector output, an external pull-up resistor is required. (For example, when a 20 KΩ external pull-up resistor is used.)
4. All digital inputs/output are TTL compatible.
5. The time from RAMP START input switching (0 → 1) to RAMP STOP output switching (1 → 0) is ramp time t_R.
6. $t_{SL} \geqq t_A\ (max) = \dfrac{C_H}{150\ \mu A - I_R} \times (V_{REF} + 0.7\ V)$
7. $t_R \fallingdotseq \dfrac{C_H}{I_R} \times V_{IN}$, $t_R\ (max) \fallingdotseq \dfrac{C_H}{I_R} \times V_{REF}$
8. $I_R = \dfrac{V_{CC} - V_{REF}}{R_{REF}}$ for MB 4053, $I_R = \dfrac{V_{REF}}{2 - R_{REF}}$ for MB 4063
9. $2\ V \leqq V_{REF} \leqq (V_{CC} - 2\ V)$ and $V_{REF} \leqq 5.25\ V$ for MB 4053
   $2.8V \leqq V_{REF} \leqq (V_{CC} - 2\ V)$ and $V_{REF} \leqq 5.25\ V$ for MB 4063
10. While and analog input voltage is being sampled, channel selection signals A_0, A_1, and A_2 must not be changed for (t_{SL}).

TYPICAL CHARACTERISTIC CURVES

7

Fig. 9 – LINEARITY ERROR vs INPUT VOLTAGE

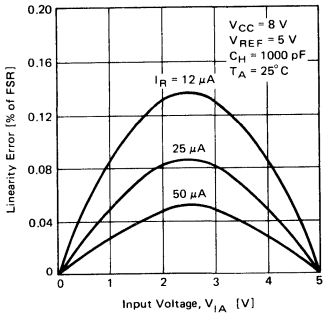


Fig. 10 – PEAK LINEARITY ERROR vs AMBIENT TEMPERATURE TA

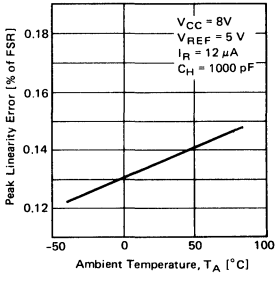
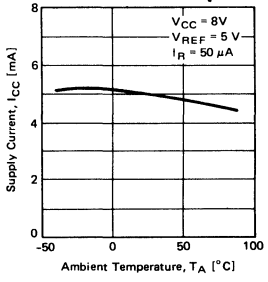


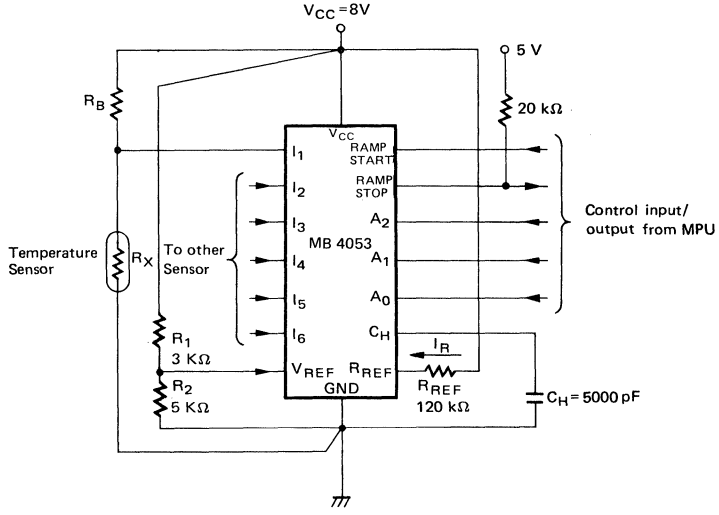
Fig. 11 – SUPPLY CURRENT vs AMBINENT TEMPERATURE



APPLICATION EXAMPLES

Examples of analog voltage (0 - 5V) A/D conversion with 10-bit resolution are shown in Fig.7 and Fig.8.

Fig. 7 — Application Example of MB 4053



Reference Voltage: $V_{REF} = \frac{R_2}{R_1 + R_2} V_{CC}$ 7-1

Ramp Current: $I_R = \frac{R_1}{R_1 + R_2} \cdot \frac{1}{R_{REF}} \cdot V_{CC}$ 7-2

Input Voltage: $V_{IN} = \frac{R_X}{R_X + R_B} \cdot V_{CC}$ 7-3

Ramp Time: $t_R \fallingdotseq V_{IN} \cdot \frac{C_H}{I_R}$

$= \frac{R_X}{R_X + R_B} \cdot (1 + \frac{R_2}{R_1}) \cdot C_H \cdot R_{REF}$ 7-4

$V_{REF} = \frac{5\ k\Omega}{3\ k\Omega + 5\ k\Omega} \times 8\ V = 5\ V$

$I_R = \frac{V_{CC} - V_{REF}}{R_{REF}} = \frac{8\ V - 5\ V}{120\ k\Omega} = 25\ \mu A$

$t_{SL} \geqq \frac{C_H \times V_{REF}}{I_{A(min)} - I_R} = \frac{5000\ pF \times (5\ V + 0.7\ V)}{150\ \mu A - 25\ \mu A} = 228\ \mu s$

$t_{R\,max} \fallingdotseq \frac{C_H \times V_{REF}}{I_R} = \frac{5000\ pF \times 5\ V}{25\ \mu A} = 1000\ \mu s$

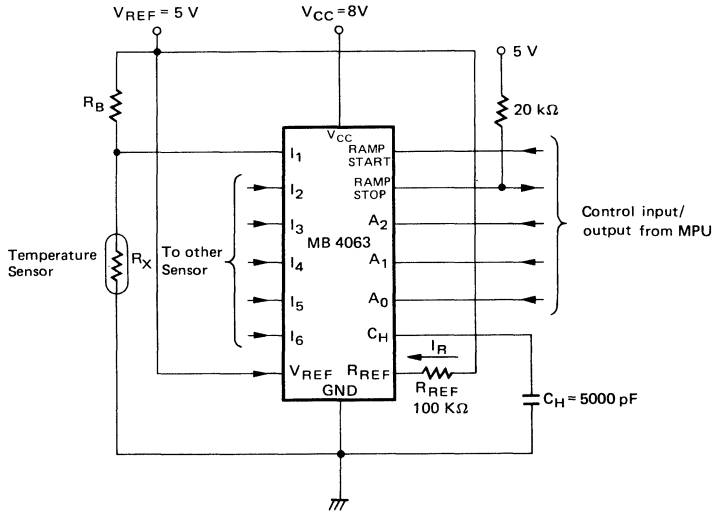
If the ramp time is counted with a 1 MHz clock, the following resolution is obtained.

$$\frac{1000\ \mu s}{1\ \mu s} = 1000 \fallingdotseq 2^{10}$$

As shown in this example, the voltage output of the sensor is proportional to V_{CC} (Eq. 7-3) and V_{REF} is also proportional to V_{CC} (Eq. 7-1), the sensor output conversion results (Eq. 7-4) are not influenced by power supply voltage fluctuation. Such a conversion is called ratio metric conversion and is effective for minimizing the effects of conversion error. Supply voltage fluctuations during discharge do result in error, however.

7

Fig. 8 – Application Example of MB 4063



Ramp Current: $I_R = \frac{V_{REF}}{2R_{REF}}$ 8-1

Input Voltage: $V_{IN} = \frac{R_X}{R_X + R_B} \cdot V_{REF}$ 8-2

Ramp Time: $t_R \fallingdotseq V_{IN} \cdot \frac{C_H}{I_R}$

$= \frac{R_X}{R_X + R_B} \cdot C_H \cdot 2R_{REF}$ 8-3

$I_R = \frac{V_{REF}}{2R_{REF}} = \frac{5V}{2 \times 100k\Omega} = 25\mu A$

$t_{SL} \geqq \frac{C_H \times V_{REF}}{I_A(min) - I_R} = \frac{5000pF \times (5V+0.7V)}{150\mu A - 25\mu A} = 228\mu s$

$t_{R\,max} \fallingdotseq \frac{C_H \times V_{REF}}{I_R} = \frac{5000pF \times 5V}{25\mu A} = 1000\mu s$

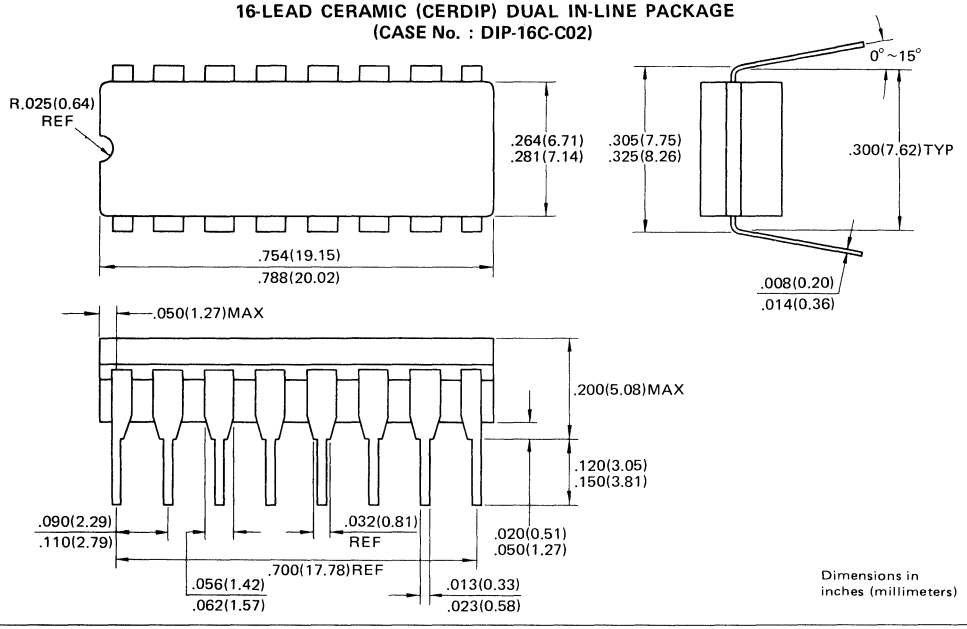
If the ramp time is counted with a 1 MHz clock, the following resolution is obtained.

$$\frac{1000\mu s}{1\mu s} = 1000 \fallingdotseq 2^{10}$$

7

PACKAGE DIMENSIONS

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-16C-C02)

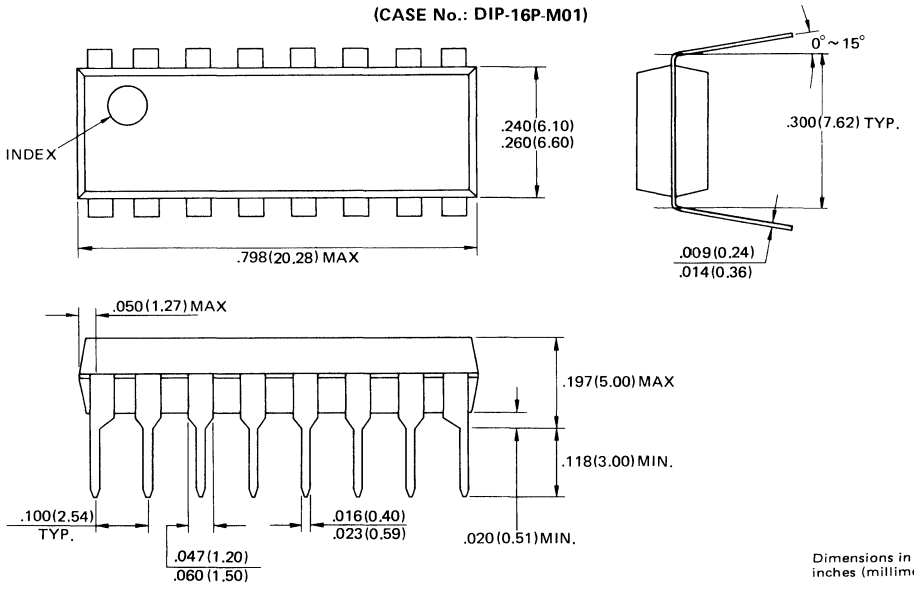


Dimensions in inches (millimeters)

7

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-16P-M01)

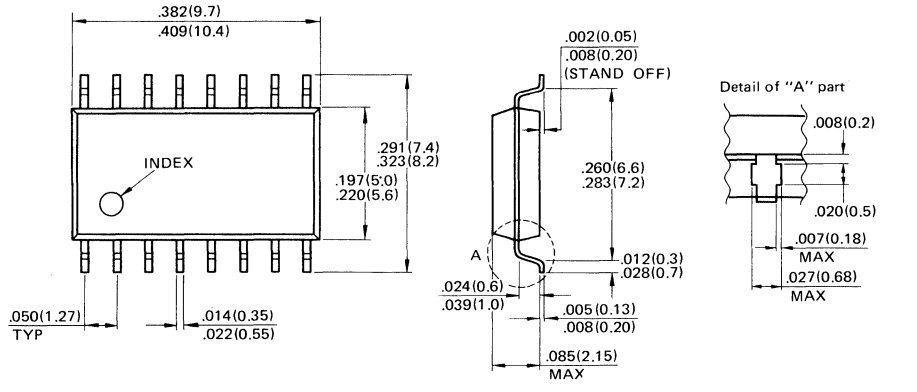


Dimensions in inches (millimeters)

7

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



Dimensions in
inches (millimeters)

7

FUJITSU

8-CHANNEL 8-BIT A/D CONVERTER

MB4056

April 1988
Edition 2.0

8-CHANNEL 8-BIT A/D CONVERTER

The Fujitsu MB4056 is an analog-to-digital converter (ADC) for general purpose which features eight channels of analog inputs and 8-bit data length of digital output.

Analog input signal is converted to serial 8-bit digital data by the successive-approximation technique which provides high-speed conversion, i.e. many analog data can be converted within a short time.

Additionally, the MB4056 has dual range conversion capability, which provides sequentially one data of both range, standard and contracted modes, to chose better data between them and to delete the range change time.

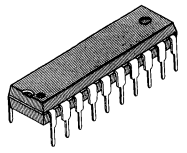
All digital I/O signals including control inputs are TTL level compatible so as to provide wide application such as in microprocessor-controlled system and so on.

- Single Power Supply: +4.75 V to +18 V
- Multiplex 8-Channel Analog Inputs:
- Resolution: 8 bits
- Linearity Error: ±0.19% Max.
- Analog Input Voltage Ranges:
  Automatic Range Change/Dual Range Conversion: 0 to 5 V Standard mode
  0 to 1.25 V Contracted mode
- Successive-Approximation Conversion: 100 μs/ch Max. at f_{CLK} = 100 kHz, S/D = 1
  200 μs/ch Max. at f_{CLK} = 100 kHz, S/D = 0
- Ratio-metric Conversion by Reference Voltage V_{REF}
- Analog Input Bias Current: 250 nA Max.
- TTL/CMOS Compatible Digital I/O
- Power Consumption: 160 mW Typ. at V_{CC} = 8V
- Standard 20-pin Plastic Package: Suffix: -P
  Standard 20-Pin Ceramic Package: Suffix: -Z

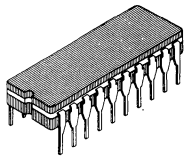
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	+20	V
Digital Input Voltage		V_{IH}	+20	V
Digital Output Voltage (Off-State)		V_{OH}	+20	V
Analog Input Voltage		V_{IA}	+20	V
Storage Temperature	Ceramic	T_{STG}	−55 to +150	°C
	Plastic	T_{STG}	−40 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

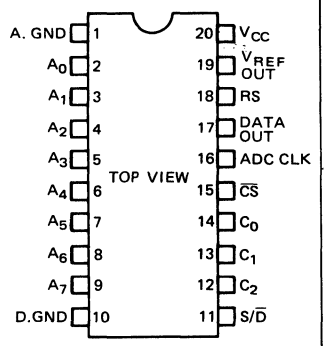


PLASTIC PACKAGE
DIP-20P-M01



PLASTIC PACKAGE
DIP-20C-C03

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

7

Fig. 1 – MB4056 BLOCK DIAGRAM

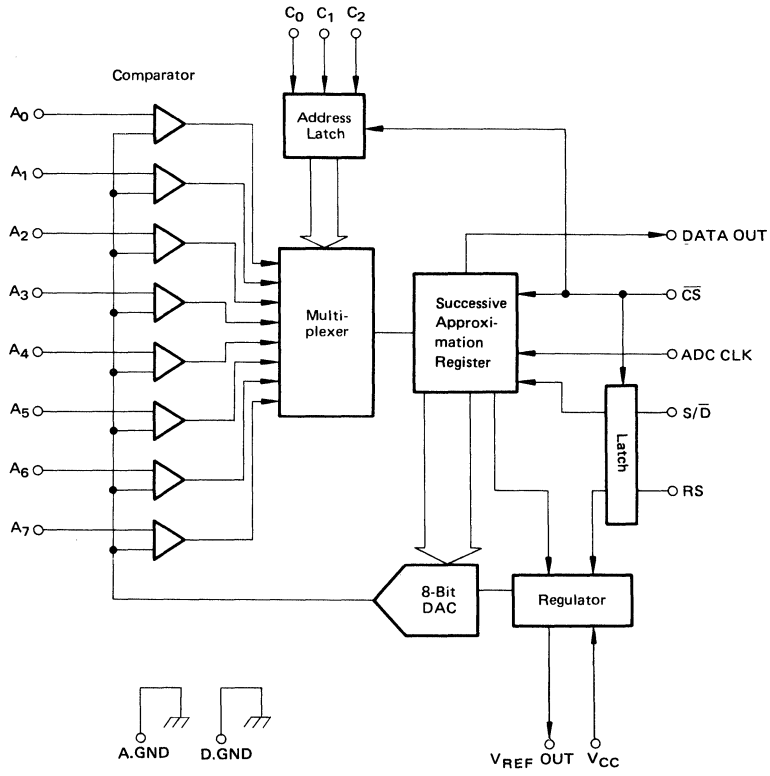


TABLE 1: CONVERSION MODES

S/D	RS	1st Conversion	2nd Conversion
L	L	Contracted Range	Standard Range
L	H	Standard Range	Contracted Range
H	L	Contracted Range	–
H	H	Standard Range	–

TABLE 2: CHANNEL SELECTIONS

C_2	C_1	C_0	Channel
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

PIN DESCRIPTIONS

Pin Name	Pin No.	Descriptions
A_0 to A_7	2 to 9	**Analog Inputs** These inputs are provided to receive eight channels of analog inputs. One of them is selected by a combination of C_0 to C_2.
S/$\overline{D}$	11	**Conversion Mode Select Input** This control input is provided to select a conversion sequence with RS input as shown in Table 1. When low, analog input voltage is converted in both ranges, and when high, in one range only. This input is latched at the falling edge of $\overline{CS}$.
C_2 to C_0	12 to 14	**Channel Select Inputs** These inputs are used to select one of eight analog input as shown in Table 2. This inputs are latched at the falling edge of $\overline{CS}$.
$\overline{CS}$	15	**Chip Select Input** This control input is used to start analog to digital conversion and to terminate it. When $\overline{CS}$ goes low, the A/D conversion starts and the DATA OUTPUT is enabled. When the A/D conversion is completed or termination of the conversion is required, $\overline{CS}$ is made high.
ADC CLK	16	**A/D Conversion Clock** This clock signal is used for A/D conversion. The conversion speed is determined by this clock rate. But precise stability of the clock rate is no required.
DATA OUT	17	**Data Outputs** This output is provided to output the A/D conversion results as digital signals. The converted digital data are serially output in the order of start-bit, MSB (Most Significant Bit), 2SB (Second Significant Bit), . . . , 7SB, LSB (Least Significant Bit) and stop-bit in synchronous with the ADC CLK.
RS	18	**Range Select Input** This control input is provided to select an analog input voltage as shown in Table 1. This input is latched at the falling edge of $\overline{CS}$.
V_{REF}	19	**Reference Voltage Output** This output provides the regulated 5V when V_{CC} is between 8V and 18V. About 10mA current of the output is supplyed externally.
A. GND D. GND	1 10	Analog Ground Digital Ground
V_{CC}	20	Power Supply Voltage, 4.75V to 18V.

7

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	4.75	12	18	V
Digital output Low Current	I_{OL}			8	mA
Ambient Operating Temperature	T_A	-40		+85	°C

ANALOG CIRCUIT CHARACTERISTICS

(V_{CC} = 4.75 to 18V, T_A = -40 to 85°C)

Parameter		Symbol	Condition	Value			Unit
				Max	Typ	Max	
Resolution						8	bit
Linearity Error						±0.5	LSB
Differential Linearity Error						±0.9	LSB
Zero Transition Voltage		V_{ZS}	Standard Conversion Mode $8V \leq V_{CC} \leq 18V$		20		mV
Full Scale Transition Voltage		V_{FS}			4980		mV
Zero Transition Voltage		V_{ZC}	Contracted Conversion Mode $4.75V \leq V_{CC} \leq 18V$		5		mV
Full Scale Transition Voltage		V_{FC}			1245		mV
Comparator Input Current		I_{COP}				-250	nA
Regulator	Output Voltage		$8V \leq V_{CC} \leq 18V$	4.5	5.0	5.5	V
	Line Regulation		$8V \leq V_{CC} \leq 18V$		4.0		mV/V
	Load Regulation		V_{CC} = 12V $-10mA \leq I_{OUT} \leq 0mA$		0.5		mV/mA
	Output Voltage Change with Temperature		V_{CC} = 12V		50		PPm/°C
Conversion Time		t_{CYC1}	f_{CLK} = 100kHz, S/D = "1"			100	μs/CH
		t_{CYC0}	f_{CLK} = 100kHz, S/D = "0"			200	μs/CH

DIGITAL CIRCUIT DC CHARACTERISTICS

(V_{CC} = 4.75 to 18V, T_A = −40 to 85°C)

Parameter	Symbol	Condition		Value			Unit
				Min	Typ	Max	
Input High Voltage	V_{IH}			2.0			V
Input Low Voltage	V_{IL}					0.8	V
Input Clamp Voltage	V_{IC}	I_{IL} = −18mA				−1.5	V
Output High Current	I_{OH}	V_{IH} = 2V, V_{IL} = 0.8V V_{OH} = 20V				100	μA
Output Low Voltage	V_{OL}	V_{IH} = 2V V_{IL} = 0.8V	I_{OL} = 4mA			0.4	V
			I_{OL} = 8mA			0.5	V
Input High Current	I_{IH}	V_{IH} = 2.7V				20	μA
		V_{IH} = 20V				100	μA
Input Low Current	I_{IL}	V_{IL} = 0.4V			−20	−100	μA
Power Supply Current	I_{CC}	V_{CC} = 20V			20	38	mA

DIGITAL CIRCUIT AC CHARACTERISTICS

(V_{CC} = 4.75 to 18V, T_A = −40 to 85°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
ADC CLK Cycle Time	t_{CY}	10			μs
ADC CLK H level Pulse Width	$t_{WAC}{}^{+}$	2.5			μs
ADC CLK L level Pulse Width	$t_{WAC}{}^{-}$	2.5			μs
$\overline{CS}$ H level Pulse Width	$t_{WCS}{}^{+}$	1.5			μs
$\overline{CS}$ Set-up Time	t_{SCS}	1			μs
$\overline{CS}$ Hold Time	t_{HCS}	1			μs
Channel Set-up Time	t_{SCH}	0			μs
Channel Hold Time	t_{HCH}	1.5			μs
Propagation Delay Time	t_{PLH}		0.8	2	μs
	t_{PHL}		0.8	2	μs

7

Fig. 2 – AC MEASUREMENT CIRCUIT

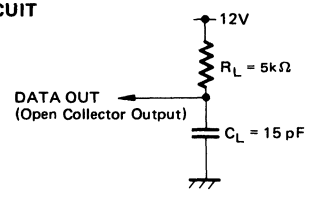


Fig. 3 – AC TIMING DIAGRAM

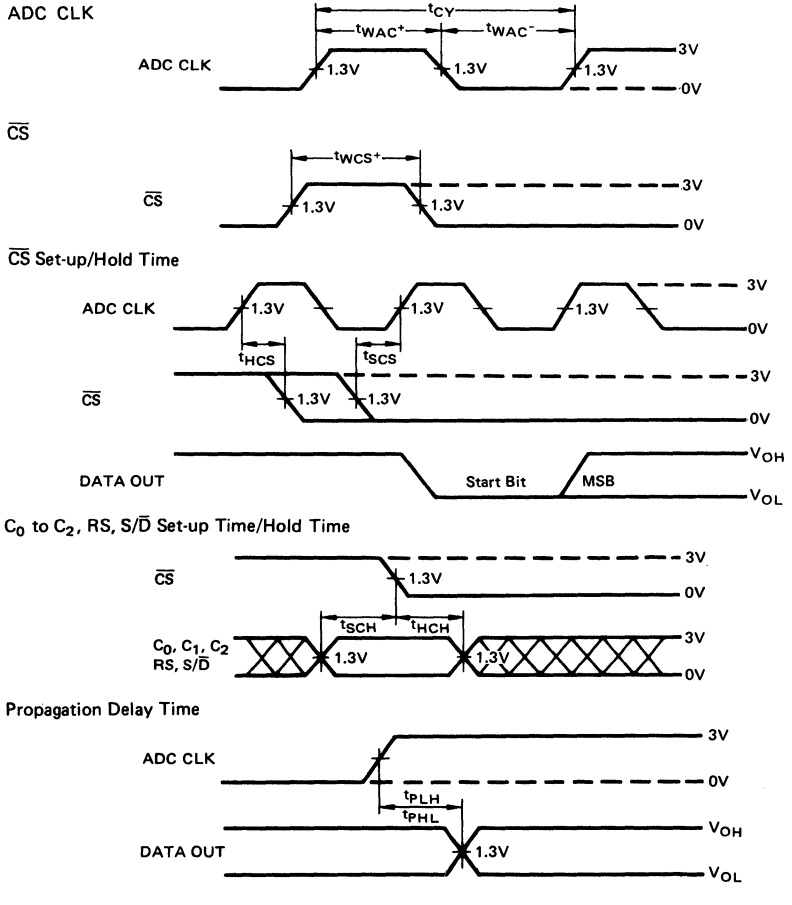


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Fig. 4 – TIMING DIAGRAM (S/$\overline{D}$ = "0")

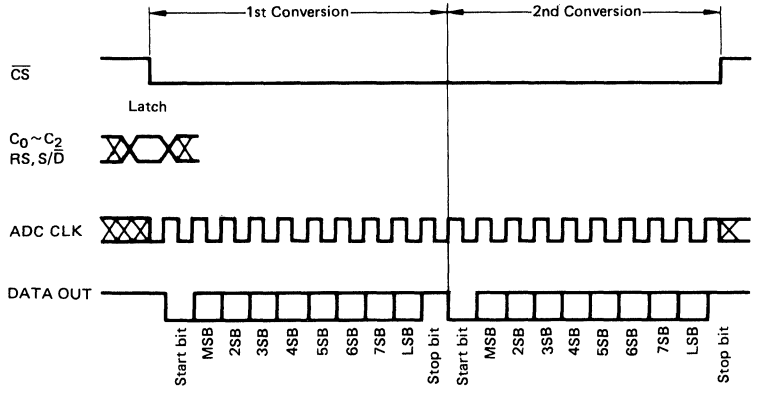
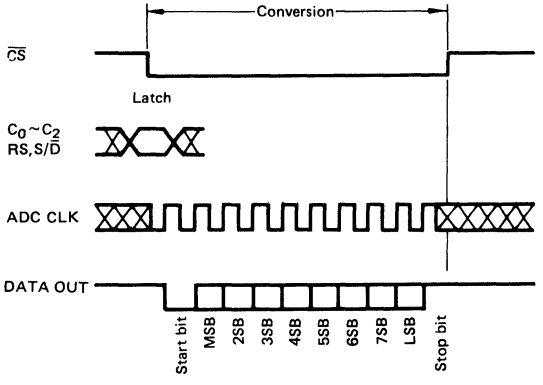


Fig. 5 – TIMING DIAGRAM (S/$\overline{D}$ = "1")



7

TYPICAL CHARACTERISTICS CURVES

Fig. 6 – ALLOWABLE V_{REF} OUT PIN OUTPUT CURRENT vs. POWER SUPPLY VOLTAGE

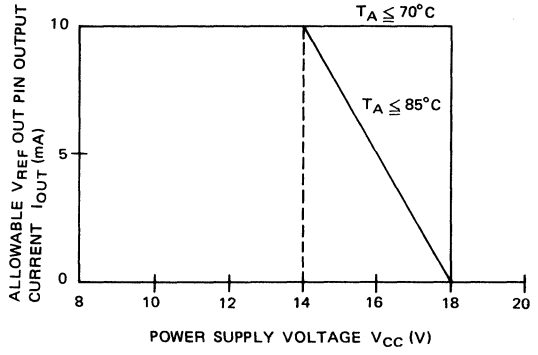
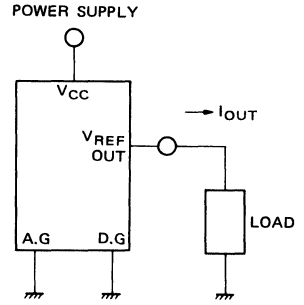


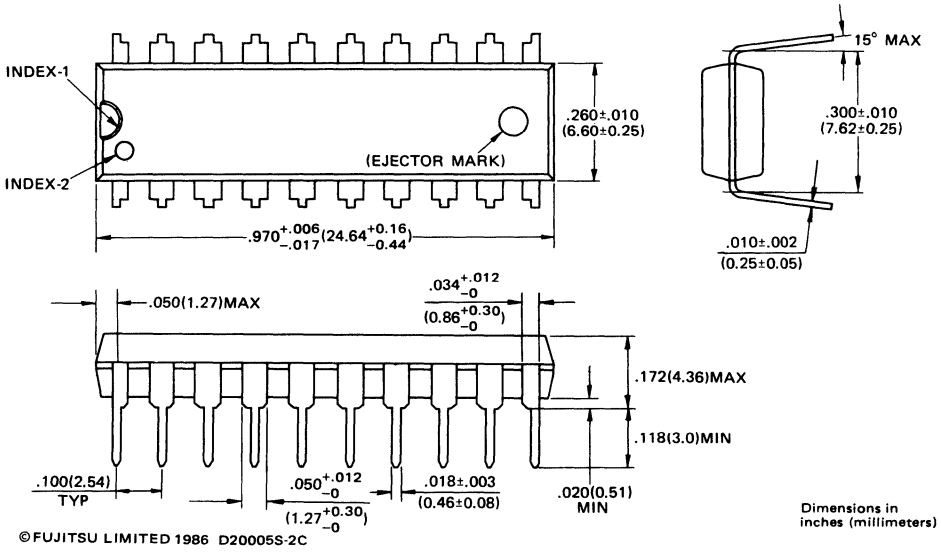
Fig. 7 – MEASUREMENT CIRCUIT



7

PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M01)



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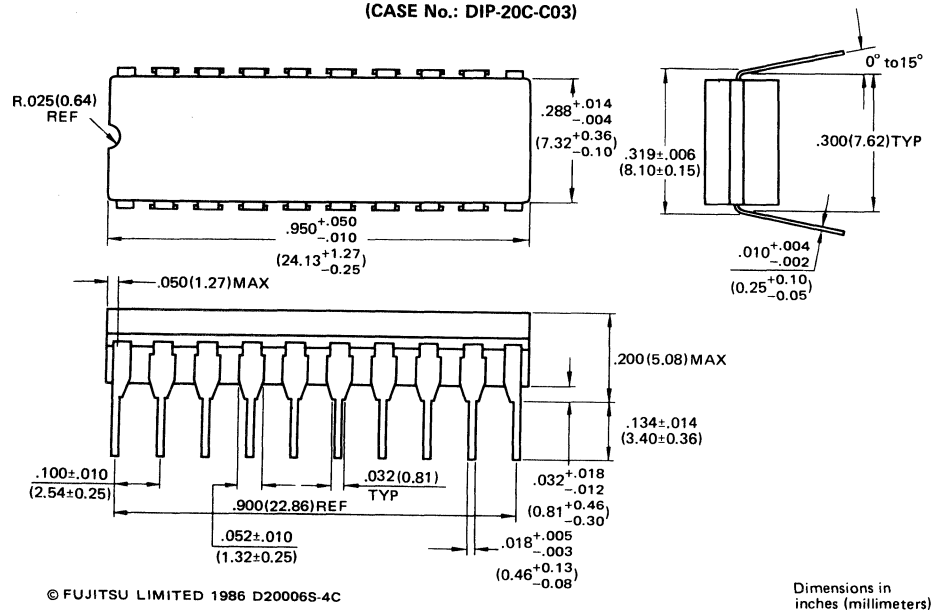
PACKAGE DIMENSIONS (continued)

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)



Dimensions in
inches (millimeters)

7

FUJITSU

8-CHANNEL 8-BIT A/D CONVERTER

MB 4066

June 1987
Edition 1.0

8-CHANNEL 8-BIT A/D CONVERTER

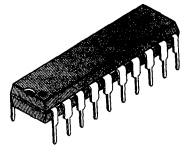
The Fujitsu MB 4066 is an analog-to-digital converter (ADC) for general purpose which features eight channels of analog inputs and 8-bit data length of digital output.

Analog input signal is converted to serial 8-bit digital data by the successive-approximation technique which provides high-speed conversion, i.e. many analog data can be converted within a short time.

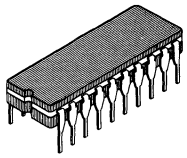
Additionally, the MB 4066 has dual range conversion capability, which provides sequentially one data of both range, standard and contracted modes, to chose better data between them and to delete the range change time.

All digital I/O signals including control inputs are TTL level compatible so as to provide wide application such as in microprocessor-controlled system and so on.

- Single Power Supply: +7.6 V to +18 V
- Multiplex 8-Channel Analog Inputs:
- Resolution: 8 bits
- Linearity: ±0.19% Max.
- Analog Input Voltage Ranges:
- Automatic Range Change/Dual Range Conversion: 0 to V_{REF} Standard mode, 0 to 1/4V_{REF} Contracted mode
- Successive-Approximation Conversion: 100 μs/ch Max. at f_{CLK} = 100 kHz
- Ratio-metric Conversion by Reference Voltage V_{REF}
- Serial Data Output (Open Collector)
- TTL/CMOS Compatible Digital I/O
- Power Consumption: 160 mW Typ. at V_{CC} = 8V
- Standard 20-pin Dual In-line Package

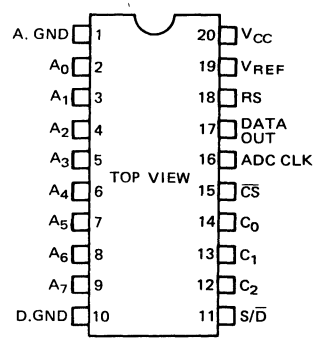


PLASTIC PACKAGE
DIP-20P-M01



CERAMIC PACKAGE
DIP-20C-C03

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC}	+20	V
Digital Input Voltage		V_{ID}	+20	V
Digital Output Voltage (Off-State)		V_{OH}	+20	V
Analog Input Voltage		V_{IA}	+20	V
Reference Voltage		V_{REF}	+5.5	V
Storage Temperature	Ceramic	T_{STG}	−55 to +150	V
	Plastic	T_{STG}	−40 to +125	V

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

7

Fig. 1 – MB 4066 BLOCK DIAGRAM

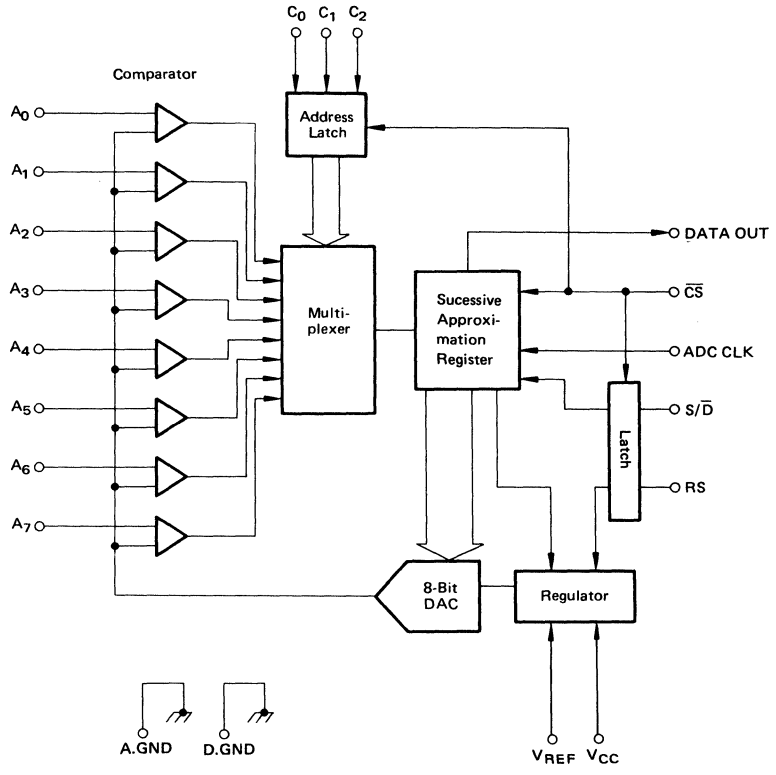


TABLE 1: CONVERSION MODES

S/D	RS	1st Conversion	2nd Conversion
L	L	Contracted Range	Standard Range
L	H	Standard Range	Contracted Range
H	L	Contracted Range	–
H	H	Standard Range	–

TABLE 2: CHANNEL SELECTIONS

C_2	C_1	C_0	Channel
0	0	0	A_0
0	0	1	A_1
0	1	0	A_2
0	1	1	A_3
1	0	0	A_4
1	0	1	A_5
1	1	0	A_6
1	1	1	A_7

PIN DESCRIPTIONS

Pin Name	Pin No.	Descriptions
A_0 to A_7	2 to 9	**Analog Inputs** These inputs are provided to receive eight channels of analog inputs. One of them is selected by a combination of C_0 to C_2.
S/$\overline{D}$	11	**Conversion Mode Select Input** This control input is provided to select a conversion sequence with RS input as shown in Table 1. When low, analog input voltage is converted in both ranges, and when high, in one range only. This input is latched at the falling edge of $\overline{CS}$.
C_2 to C_0	12 to 14	**Channel Select Inputs** These inputs are used to select one of eight analog input as shown in Table 2. This inputs are latched at the falling edge of $\overline{CS}$.
$\overline{CS}$	15	**Chip Select Input** This control input is used to start analog to digital conversion and to terminate it. When $\overline{CS}$ goes low, the A/D conversion starts and the DATA OUTPUT is enabled. When the A/D conversion is completed or termination of the conversion is required, $\overline{CS}$ is made high.
ADC CLK	16	**A/D Conversion Clock** This clock signal is used for A/D conversion. The conversion speed is determined by this clock rate. But precise stability of the clock rate is no required.
DATA OUT	17	This output is provided to output the A/D conversion results as digital signals. The converted digital data are serially output in the order of start-bit, MSB (Most Significant Bit), 2SB (Second Significant Bit), . . . , 7SB, LSB (Least Significant Bit) and stop-bit in synchronous with the ADC CLK.
RS	18	**Range Select Input** This control input is provided to select an analog input voltage as shown in Table 1. This input is latched at the falling edge of $\overline{CS}$.
V_{REF}	19	**Reference Voltage Input** This input provides the conversion reference for the analog to digital conversion circuit.
A. GND D. GND	1 10	Analog Ground Digital Ground
V_{CC}	20	Power Supply Voltage, 7.6 V to 18 V.

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CC}	7.6	12	18	V
Reference Voltage	V_{REF}	4.75	5.00	5.25	V
Digital Output Low Current	I_{OL}			8	mA
Ambient Operating Temperature	T_A	-40		+85	℃

ANALOG CIRCUIT CHARACTERISTICS

(Recommended Operating Condiions unless otherwise noted.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Resolution					8	bit
Linearity Error					±0.5	LSB
Differential Linearity Error					±0.9	LSB
Zero Transition Voltage	V_{ZS}	Standard Conversion Mode V_{REF} = 5.000V		20		mV
Full Scale Transistion Voltage	V_{FS}			4980		mV
Zero Transition Voltage	V_{ZC}	Contracted Conversion Mode V_{REF} = 5.000V		5		mV
Full Scale Transition Voltage	V_{FC}			1245		mV
V_{REF} Input Current	I_{REF}	V_{REF} = 5.000V	0.5	1.0	2.0	mA
Comparator Input Current	I_{COP}				-250	nA
Conversion Time	t_{CYC1}	f_{CLK} = 100kHz, S/D = "1"			100	μs/CH
	t_{CYC0}	f_{CLK} = 100kHz, S/D = "0"			200	μs/CH

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DIGITAL CIRCUIT DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter	Symbol	Condition		Value			Unit
				Min	Typ	Max	
Input High Voltage	V_{IH}			2.0			V
Input Low Voltage	V_{IL}					0.8	V
Input Clamp Voltage	V_{IC}	I_{IL} = −18mA				−1.5	V
Output High Current	I_{OH}	V_{IH} = 2V, V_{IL} = 0.8V V_{OH} = 20V				100	μA
Output Low Voltage	V_{OL}	V_{IH} = 2V V_{IL} = 0.8V	I_{OL} = 4mA			0.4	V
			I_{OL} = 8mA			0.5	V
Input High Current	I_{IH}	V_{IH} = 2.7V				20	μA
		V_{IH} = 20V				100	μA
Input Low Current	I_{IL}	V_{IL} = 0.4V			−20	−100	μA
Power Supply Current	I_{CC}	V_{CC} = 20V			20	38	mA

DIGITAL CIRCUIT AC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
ADC CLK Cycle Time	t_{CY}	10			μs
ADC CLK H level Pulse Width	$t_{WAC}{}^{+}$	2.5			μs
ADC CLK L level Pulse Width	$t_{WAC}{}^{-}$	2.5			μs
$\overline{CS}$ H level Pulse Width	$t_{WCS}{}^{+}$	1.5			μs
$\overline{CS}$ Set-up Time	t_{SCS}	1			μs
$\overline{CS}$ Hold Time	t_{HCS}	1			μs
Channel Set-up Time	t_{SCH}	0			μs
Channel Hold Time	t_{HCH}	1.5			μs
Propagation Delay Time	t_{PLH}		0.8	2	μs
	t_{PHL}				

7

Fig. 2 – AC MEASUREMENT CIRCUIT

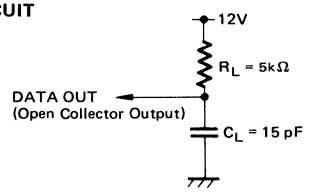

Fig. 3 – AC TIMING DIAGRAM

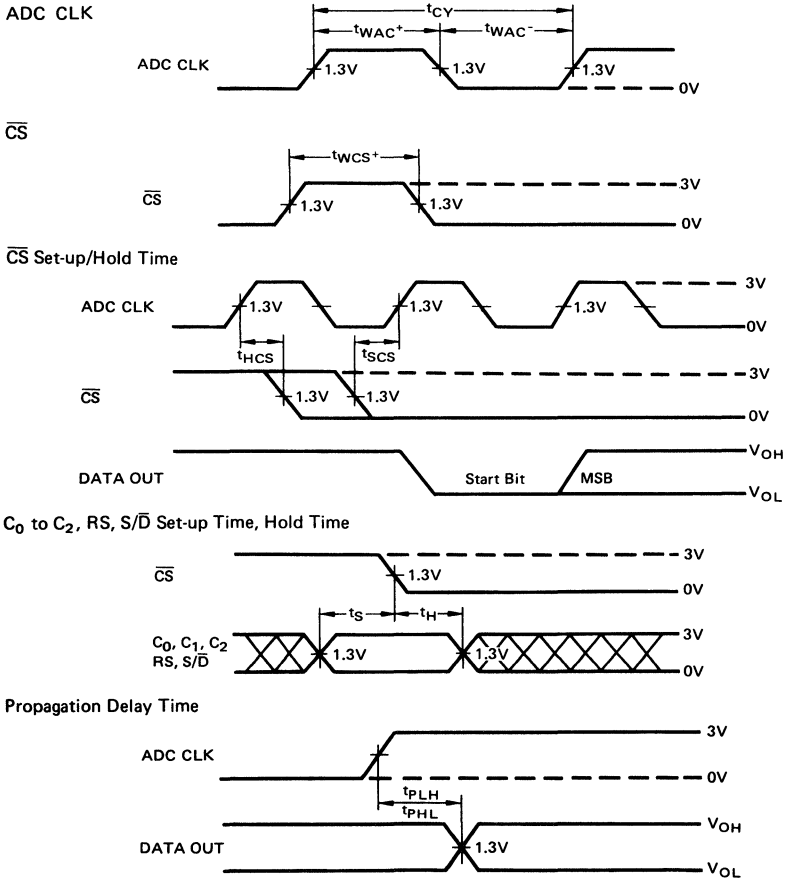

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Fig. 4 — TIMING DIAGRAM ($S/\overline{D}$ = "0")

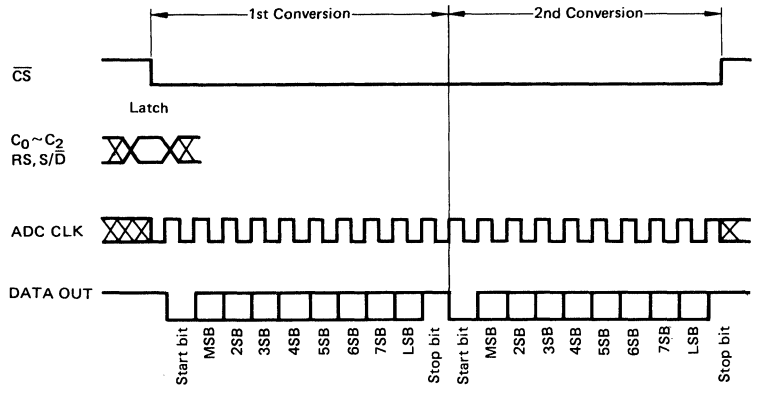
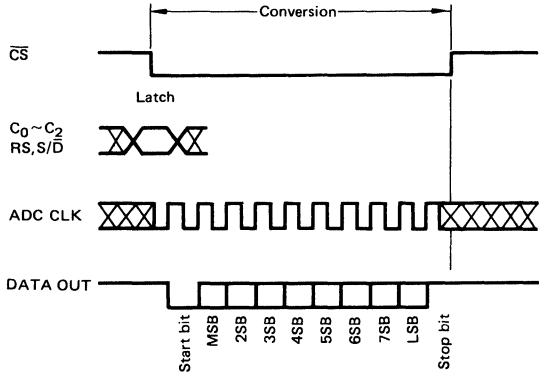


Fig. 5 — TIMING DIAGRAM ($S/\overline{D}$ = "1")



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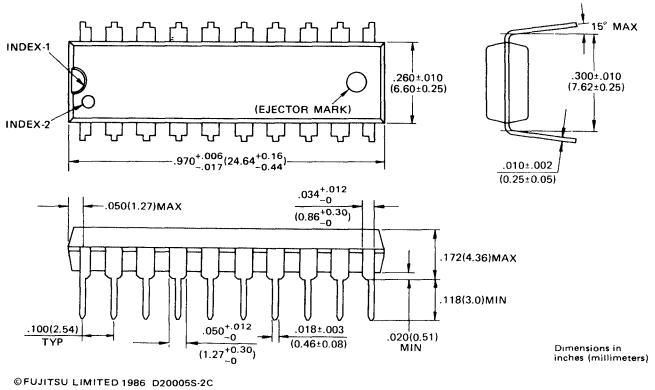
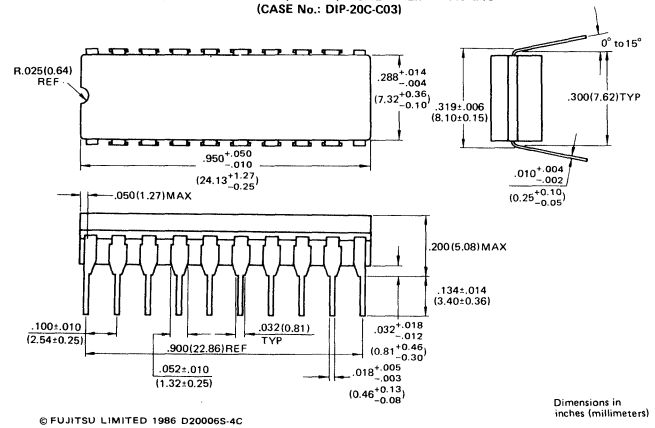
PACKAGE DIMENSIONS

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M01)



Dimensions in inches (millimeters)

20-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C03)



Dimensions in inches (millimeters)

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FUJITSU

8-BIT ULTRA-HIGH SPEED A/D CONVERTER

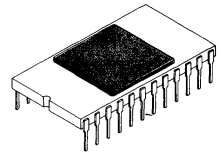
MB 40547-7
MB 40547-8

May 1984
Edition 2.0

8-BIT ULTRA HIGH SPEED A/D CONVERTER

The Fujitsu MB 40547 is an ultra-high A/D converter which is fabricated with Fujitsu Advanced Bipolar Technology. The MB 40547 uses the full-parallel comparision technique (flash method) for high speed conversion and can convert wide-band analog signals such as video to digital signals at a sampling rate from DC to 30 Megasamples/sec. without any sampling/holding circuit. Because of such high-speed operation, the MB 40547 is suitable for applications such as color-TV coding, video processing with computer, or radar signal processing.

- Resolution: 8 bits
- Linearity: MB 40547-7 : ±1 LSB
  MB 40547-8 : ±1/2 LSB
- Conversion Rate: 30 MSPS typ.
- Analog Input Voltage: 0 to -2 V
- No need for external sampling/holding circuit
- Digital I/O level: 10 K ECL level
- Output modes: Binary/2's Complement
- Single Power Supply: -5.2 V
- Power consumption: 900 mW typ.
- Package: Standard 24-pin DIP



CERAMIC PACKAGE
DIP-24C-A01

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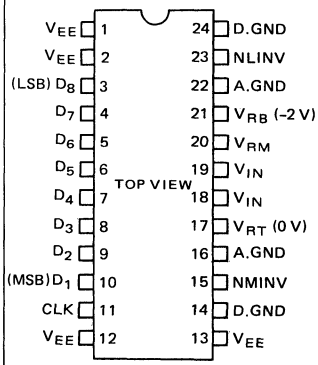
PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

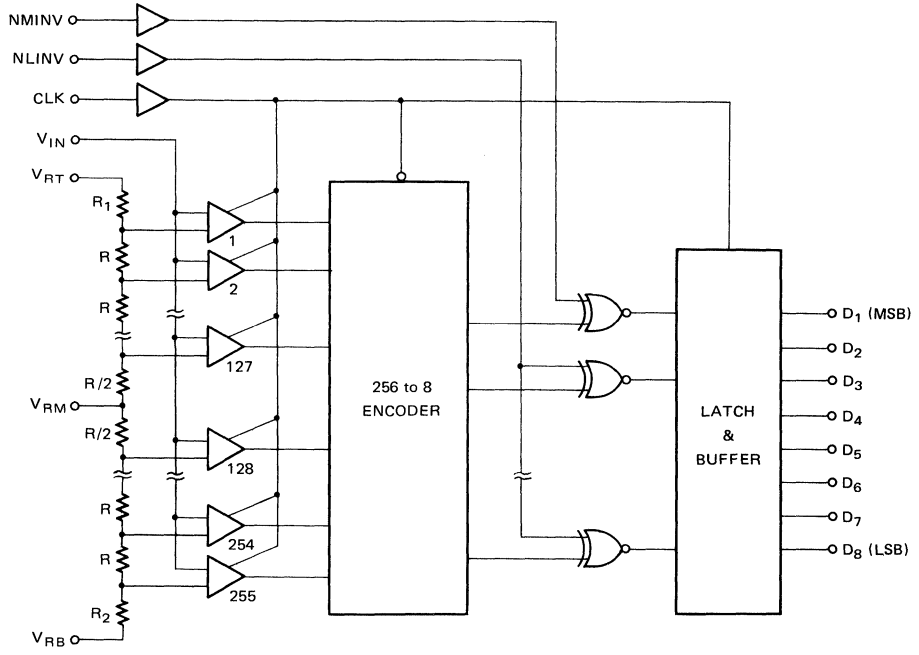
Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{EE}	+0.5 to -7.0	V
Digital Input Voltage	V_{IND}	+0.5 to V_{EE}	V
Analog Input Voltage	V_{INA}	+0.5 to V_{EE}	V
Analog Reference Voltage	V_R	+0.5 to V_{EE}	V
Output Current	I_O	-12*	mA
Storage Temperature	T_{STG}	-55 to +150	°C

* Negative value of current means that the current flows from the device.

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{EE}	-5.46	-5.20	-4.94	V
Analog Input Voltage	V_{INA}	-2.0		0	V
Analog Reference Voltage (Top Side)	V_{RT}		0	0.1	V
Analog Reference Voltage (Bottom Side)	V_{RB}	-2.1	-2.0		V
Clock Pulse Width at High level	t_w+	25			ns
Clock Pulse Width at Low level	t_w-	25			ns
Operating Temperature	T_A	0		70	°C

DC CHARACTERISTICS

(V_{EE} = -5.2 V, T_A = 0 to +70°C, Output Circuits: See TEST LOAD CIRCUIT)

Parameter		Symbol	Value			Unit
			Max	Typ	Max	
Resolution					8	bits
Linearity Error	MB 40547-7	E_R			±0.4	%
	MB 40547-8				±0.2	
Equivalent Input Resistance		R_{INA}	25			kΩ
Input Capacitance		C_{INA}		130	250	pF
High-level Input Current		I_{IHA}			300	μA
Low-level Input Current		I_{ILA}			290	μA
Reference Current		I_{RB}	-36	-20		mA

AC CHARACTERISTICS

(V_{EE} = -5.2 V, T_A = 0 to +70°C, Output Circuit: See TEST LOAD CIRCUIT)

Parameter	Symbol	T_A (°C)	Value			Unit
			Min	Typ	Max	
High-level Output Voltage	V_{OH}	0	-1.000		-0.840	V
		+25	-0.960		-0.810	
		+70	-0.900		-0.720	
Low-level Output Voltage	V_{OL}	0	-1.870		-1.665	V
		+25	-1.850		-1.650	
		+70	-1.830		-1.625	
High-level Input Voltage	V_{IHD}	0	-1.145			V
		+25	-1.105			
		+70	-1.045			
Low-level Input Voltage	V_{ILD}	0			-1.490	V
		+25			-1.475	
		+70			-1.450	
High-level Input Current	I_{IHD}				220	μA
Low-level Input Current	I_{ILD}				180	μA
Power Supply Current	I_{EE}		-280	-170		mA

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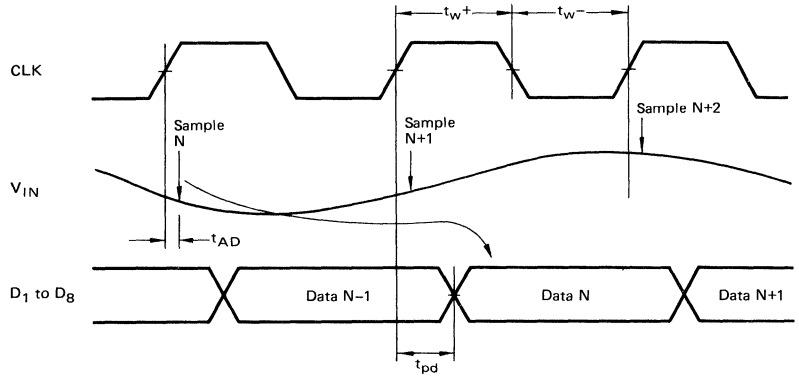
SWITCHING CHARACTERISTICS

(V_{EE} = -5.2 V, T_A = +25°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Maximum Conversion Rate	FS	20	30		MHz
Aperture Delay	t_{AD}				ns
Digital Output Delay	t_{pd}		15	25	ns

TIMING DIAGRAM



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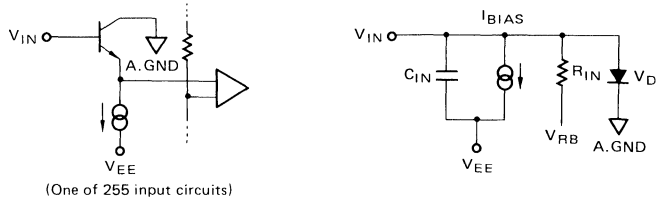
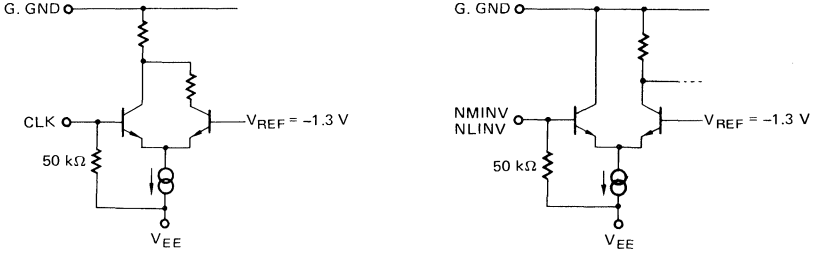
ANALOG INPUT EQUIVALENT CIRCUIT

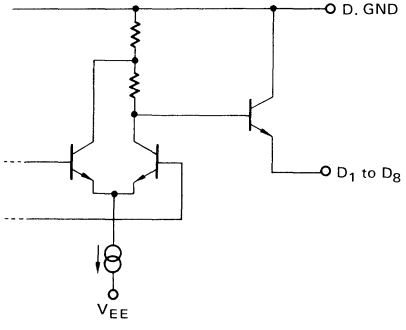


C_{IN}: Non-linear Emitter-follower Junction Capacitance
R_{IN}: Linear Resistance Model for Input Current Transition by Comparator Switching:
Infinite value for $V_{IN} < V_{RB}$ or when CLK = HIGH.
V_{RB}: Voltage at V_{RB} Terminal.
I_{BIAS}: Constant Input Bias Current
V_D: Diode consisting of the base-collector junction of emitter-follower transistor.

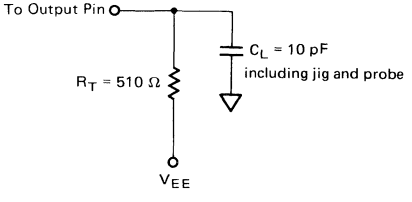
DIGITAL INPUT EQUIVALENT CIRCUIT



DIGITAL OUTPUT EQUIVALENT CIRCUIT



TEST LOAD CIRCUIT



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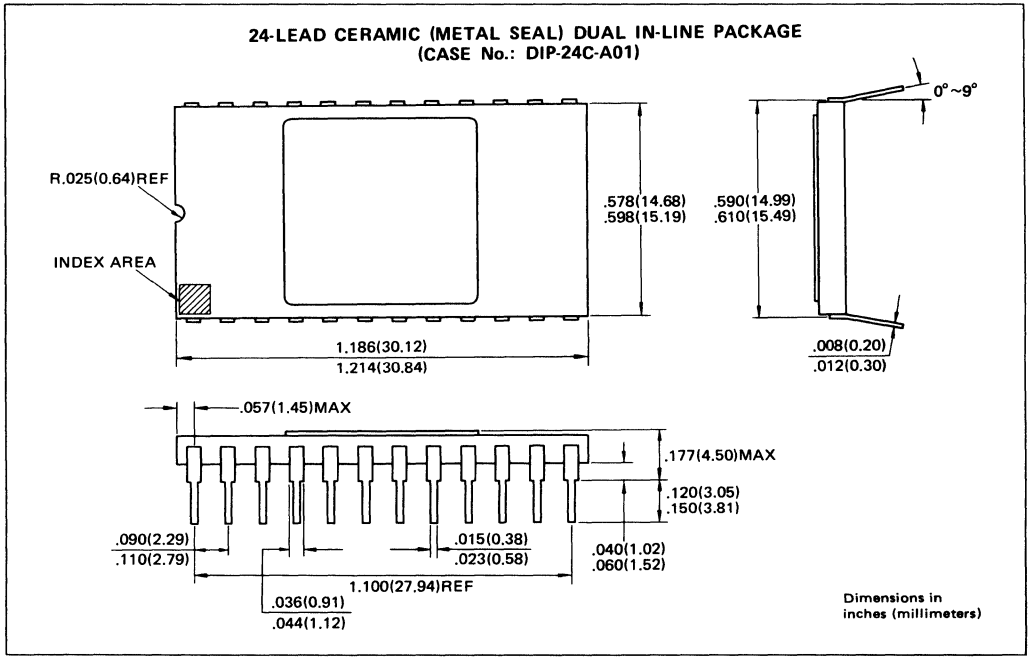
OUTPUT CODES

(Recommended Operating Conditions unless Otherwise noted, $V_{RT} \fallingdotseq 0V$, $V_{RD} = -1{,}000V$, Positive Logic)

STEP	RANGE		BINARY		OFFSET 2'S COMPLEMENT	
	-2.0000 V FS 7.8431 mV Step*1 (V)	-2.0000 V FS 8.000 mV Step*1 (V)	TRUE NMINV = 1 NLINV = 1	INVERTED NMINV = 0 NLINV = 1	TRUE NMINV = 0 NLINV = 0	INVERTED NMINV = 1 NLINV = 0
000	0.0000	0.0000	00000000	11111111	10000000	01111111
⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮
127	-0.9961	-1.0160	01111111	10000000	11111111	00000000
128	-1.0039	-1.0240	10000000	01111111	00000000	11111111
129	-1.0118	-1.0320	10000001	01111110	00000001	11111110
⋮	⋮	⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮	⋮	⋮
255	-2.0000	-2.0400	11111111	00000000	01111111	10000000

Note *1: Value of analog voltage is defined as value at the center of the step.

PACKAGE DIMENSIONS



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FUJITSU

6-BIT ULTRA-HIGH SPEED VIDEO A/D CONVERTER

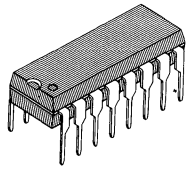
MB40576

April 1988
Edition 3.0

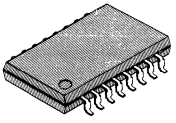
6-BIT ULTRA HIGH SPEED VIDEO A/D CONVERTER

The Fujitsu MB 40576 is a low power ultra-high speed video A/D converter fabricated with Fujitsu Advanced Bipolar Technology. The MB 40576 also adopts the fully-parallel comparison technique (flash method) for high speed convertion and can convert wide band analog signal such as video signal to digital signal at a sampling rate of DC through 20 Mega-samples/sec. Because of such high-speed operation, the MB 40576 is suitable for digital video applications such as the digital TV, video processing with computer, or radar signal processing.

- Resolution: 6 bits
- Linearity Error: ±0.8%
- Maximum Conversion Rate: 20 MSPS min.
- Analog Input Voltage: V_{CC} to V_{CC} −2V
- Analog Input Dynamic Range: 1 V
- Digital I/O level: TTL
- Single Power Supply: +5 V
- Power Dissipation: 270 mW typ.
- Package: Standard 16-pin DIP Package (Suffix: -P)
  Standard 16-pin FLAT Package (Suffix: -PF)

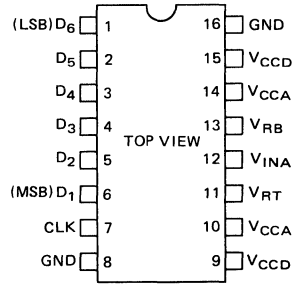


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M03

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CCA} V_{CCD}	-0.5 to +7.0	V
Digital Input Voltage	V_{IND}	-0.5 to +7.0	V
Analog Input Voltage	V_{INA}	-0.5 to V_{CC} +0.5	V
Analog Reference Voltage	V_{RT}, V_{RB}*	-0.5 to V_{CC} +0.5	V
Storage Temperature	T_{STG}	-55 to +125	°C

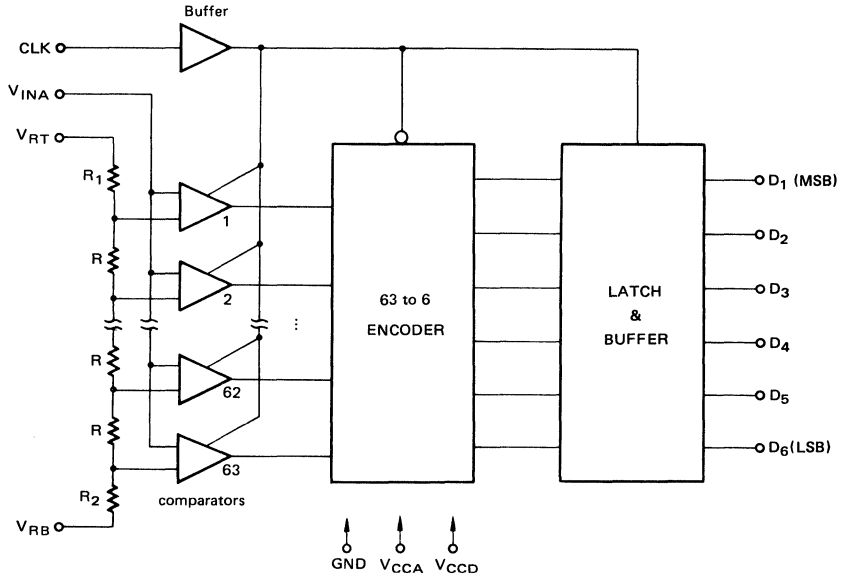
* $|V_{RT} - V_{RB}| < 2V$

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

7

Fig. 1 – MB40576 BLOCK DIAGRAM



7

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CCA} V_{CCD}	4.75	5.00	5.25	V
Analog Input Voltage*	V_{INA}	4		5	V
Analog Reference Voltage (Top side)*	V_{RT}	4	5	5.1	V
Analog Reference Voltage (Bottom side)*	V_{RB}	3	4	4.1	V
Digital High-level Output Current	I_{OHD}	-400			μA
Digital Low-level Output Current	I_{OLD}			4	mA
Clock Pulse Width at High level	t_{w+}	25			ns
Clock Pulse Width at Low level	t_{w-}	25			ns
Operating Temperature	T_A	0		70	°C

NOTE: * $V_{RB} < V_{INA} < V_{RT}$, $V_{RT} - V_{RB} = 1\ V \pm 0.1\ V$
Please keep V_{CCA} and V_{CCD} at the same potential.

7

ELECTRICAL CHARACTERISTICS

ANALOG DC CHARACTERISTICS

(V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Resolution	–				6	bits
Linearity Error	LE	DC			±0.8	%
Equivalent Analog Input Resistance	R_{INA}		100			KΩ
Input Capacitance	C_{INA}			35	65	pF
High-Level Input Current	I_{IHA}				75	μA
Low-Level Input Current	I_{ILA}				73	μA
Reference Current	I_{RB}	V_{RT} = 5 V V_{RB} = 4 V		4	7.2	mA

7

DIGITAL DC CHARACTERISTICS

(V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
High-level Output Voltage	V_{OHD}	I_{OHD} = –400 μA	2.7			V
Low-level Output Voltage	V_{OLD}	I_{OLD} = 1.6 mA			0.4	V
High-level Input Voltage	V_{IHD}		2			V
Low-level Input Voltage	V_{ILD}				0.8	V
Maximum Input Current	I_{ID}	V_{ID} = 7 V			100	μA
High-level Input Current	I_{IHD}	V_{IHD} = 2.7 V		0	20	μA
Low-level Input Current	I_{ILD}	V_{ILD} = 0.4 V	–400	–40		μA
Power Supply Current	I_{CC}			54	80	mA

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING CHARACTERISTICS

(V_{CC} = 5 V, T_A = 25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Maximum Conversion Rate	FS		20	30		MSPS
Digital Output Delay Time	t_{pd}		5	18	40	ns

TIMING DIAGRAM

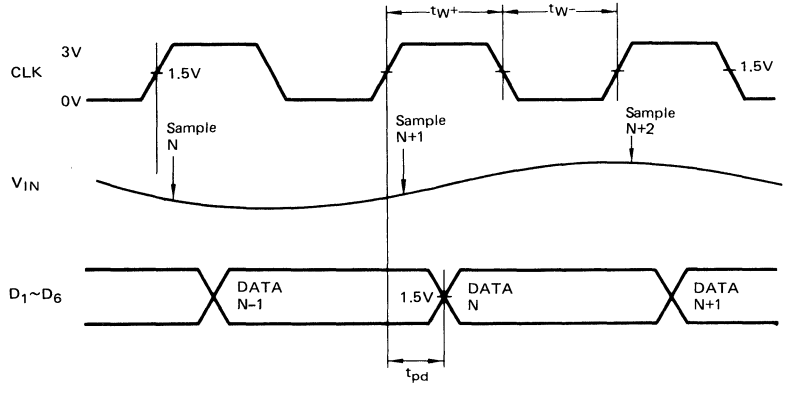


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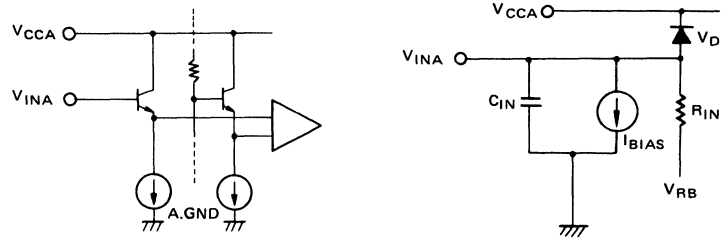
Fig. 2 – ANALOG INPUT EQUIVALENT CIRCUIT



C_{INA}: Non-linear Emitter-follower Junction Capacitance
R_{INA}: Linear Resistance Model for Input Current Transition by Comparator Switching:
Infinit value for $V_{INA} < V_{RB}$ or when CLK = High
V_{RB}: Voltage at V_{RB} terminal.
I_{BIAS}: Constant Input Bias Current
V_D: The base-collector junction diode of emitter-follower transistor.

7

Fig. 3– DIGITAL INPUT EQUIVALENT

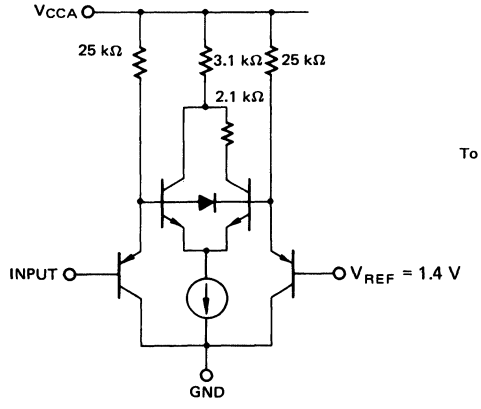
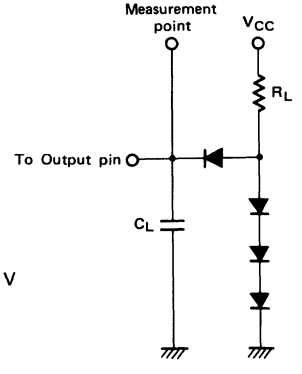


Fig. 4 – LOAD CIRCUIT FOR OUTPUT BUFFER



$R_L = 2k\Omega$
C_L = 15pF including scope and jig capacitance
Diodes : IN 3064 or equivalent.

OUTPUT CODE

(V_{CC} = 5 V, $V_{RT} \fallingdotseq V_{RB} \fallingdotseq$ 4 V)

Step	Analog Input Voltage	Digital Output Code
0	3.992 V	000000
1	4.008 V	000001
⋮	⋮	⋮
31	4.488 V	011111
32	4.504 V	100000
33	4.520 V	100001
⋮	⋮	⋮
62	4.984 V	111110
63	5.000 V	111111

NOTE: One step of output voltage (I_{LSB}) is 16 mV when V_{FT} is adjusted at 4.992V, and V_{ZT} at 4.000 V by V_{RT} and V_{RB}.
The Analog Input Voltage are the centre value of each step.

Fig. 5 – IDEAL CONVERSION CHARACTERRISTICS

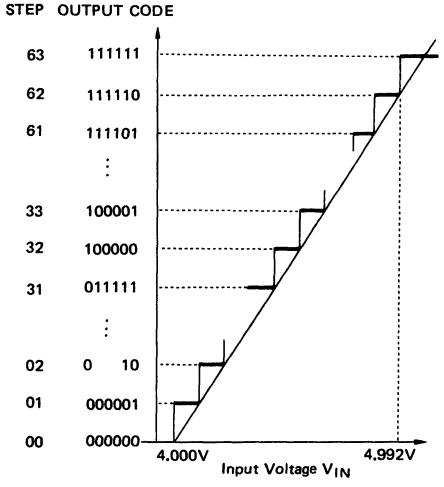
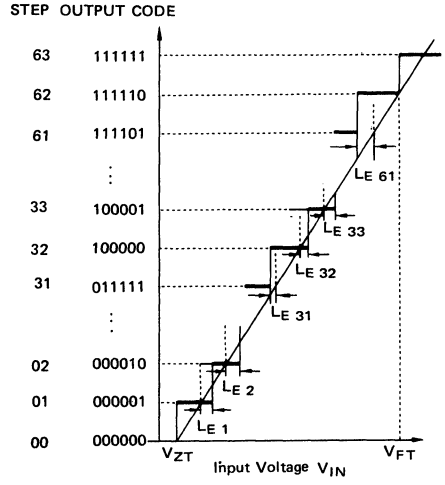


Fig. 6 – PRACTICAL CONVERSION CHARACTERISTICS



$$\text{Linearity Error} = \frac{|\,LEn\,|\ \text{max.}}{|\,FS\,|}$$

7

TYPICAL CHARACTERISTICS CURVES

Fig. 7 – POWER SUPPLY CURRENT vs. TEMPERATURE

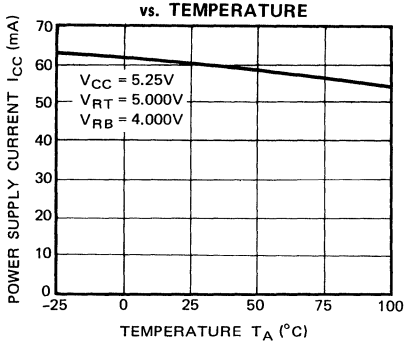


Fig. 8 – LINEARITY ERROR vs. TEMPERATURE

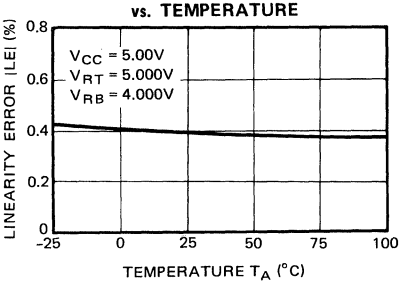


Fig. 9 – REFERENCE CURRENT vs. TEMPERATURE

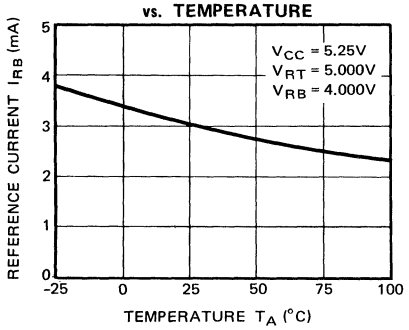


Fig. 10 – DIGITAL HIGH-LEVEL OUTPUT VOLTAGE vs. TEMPERATURE

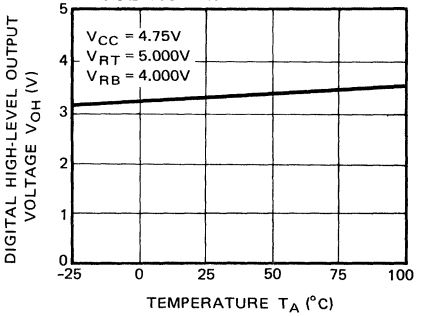


Fig. 11 – DIGITAL LOW-LEVEL OUTPUT VOLTAGE vs. TEMPERATURE

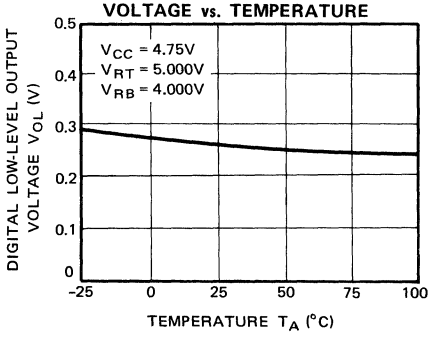


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Fig. 12 – DELAY TIME vs. TEMPERATURE

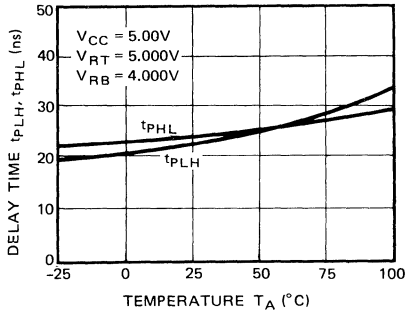


Fig. 13 – DELAY TIME vs. POWER SUPPLY VOLTAGE

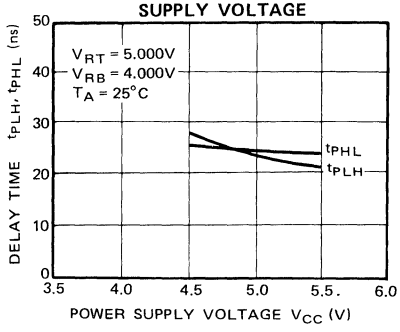


Fig. 14 – CLOCK PULSE WIDTH vs. TEMPERATURE

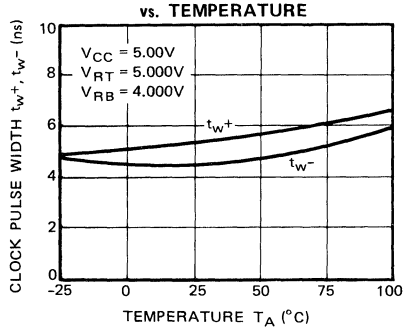


Fig. 15 – CLOCK PULSE WIDTH vs. POWER SUPPLY VOLTAGE

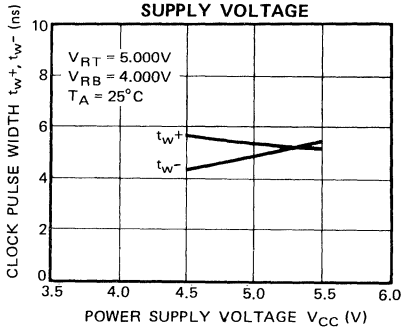
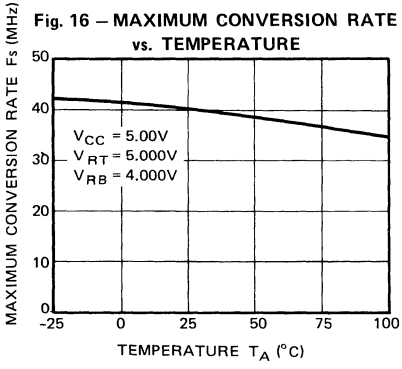


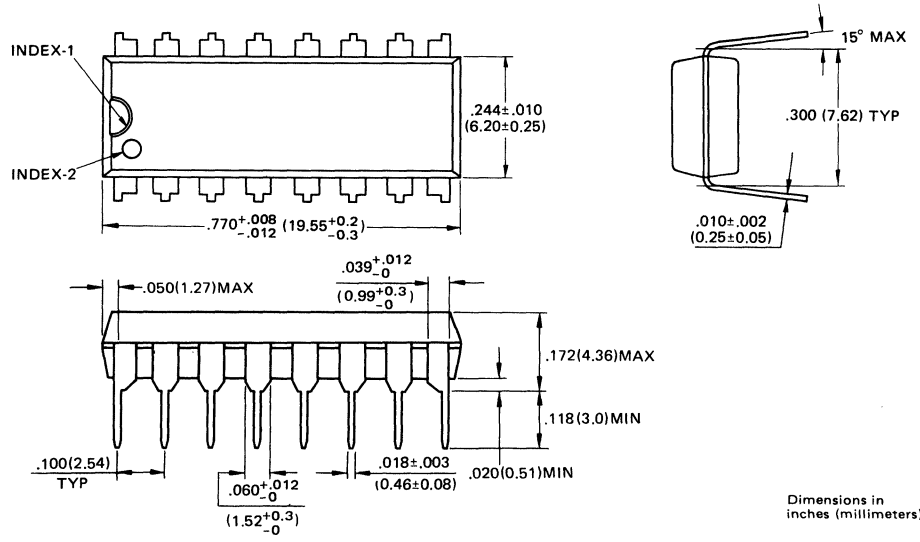
Fig. 16 – MAXIMUM CONVERSION RATE vs. TEMPERATURE



7

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)

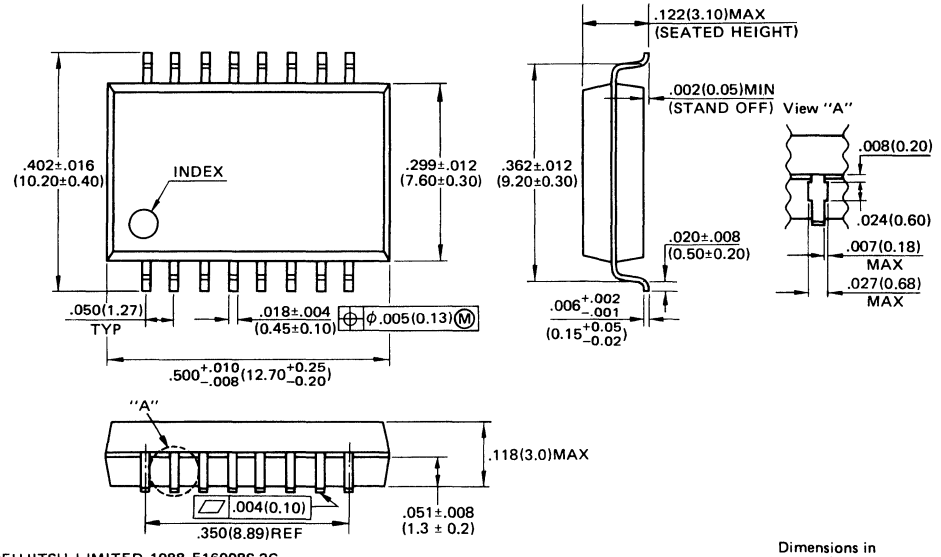


Dimensions in inches (millimeters)

7

PACKAGE DIMENSIONS (continued)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M03)



Dimensions in
inches (millimeters)

7

7

FUJITSU

8-BIT ULTRA-HIGH SPEED VIDEO A/D CONVERTER

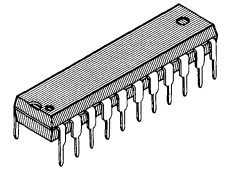
MB40578
MB40578-7

March 1988
Edition 2.0

8-BIT ULTRA HIGH SPEED VIDEO A/D CONVERTER

The Fujitsu MB 40578 is a low power ultra-high speed video A/D converter fabricated with Fujitsu Advanced Bipolar Technology. The MB 40578 also adopts the fully-parallel comparison technique (flash method) for high speed conversion and can convert wide band analog signal such as video signal to digital signal at a sampling rate of DC through 20 Mega-samples/sec. Because of such high-speed operation, the MB 40578 is suitable for digital video applications such as the digital TV, video processing with computer, or radar signal processing.

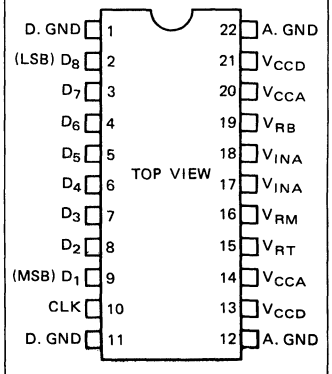
- Resolution: 8 bits
- Linearity Error: ±0.2% (MB40578)
  ±0.4% (MB40578-7)
- Maximum Conversion Rate: 20 MSPS min.
- Analog Input Voltage: 3.0V to 5.0V
- Digital I/O level: TTL
- Single Power Supply: +5V
- Power Dissipation: 480 mW typ.
- Package: Standard 22-pin DIP Package : Suffix : -P



PLASTIC PACKAGE
DIP-22P-M04

7

PIN ASSIGNMENT



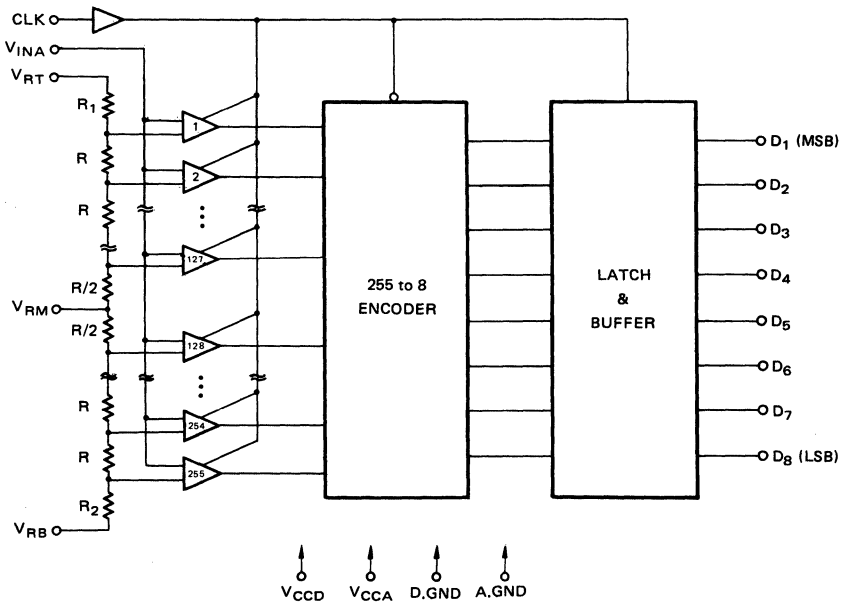
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CCA} V_{CCD}	−0.5 to +7.0	V
Digital Input Voltage	V_{IND}	−0.5 to +7.0	V
Analog Input Voltage	V_{INA}	−0.5 to V_{CC}+0.5	V
Analog Reference Voltage	V_{RT}, V_{RB}	−0.5 to V_{CC}+0.5	V
Storage Temperature	T_{STG}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB 40578 BLOCK DIAGRAM



7

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage *1	V_{CCA} V_{CCD}	4.75	5.00	5.25	V
Analog Input Voltage *2	V_{INA}	3		5	V
Analog Reference Voltage (Top side) *2	V_{RT}		5	5.1	V
Analog Reference Voltage (Bottom side) *2	V_{RB}	2.9	3		V
Digital High-level Output Current	I_{OHD}	-400			μA
Digital Low-level Output Current	I_{OLD}			4	mA
Clock Pulse Width at High Level	t_w^+	25			ns
Clock Pulse Width at Low Level	t_w^-	25			ns
Operating Temperature	T_A	0		70	°C

NOTE: *1 Please keep V_{CCA} and V_{CCD} at the same potential.
*2 $V_{RB} < V_{INA} < V_{RT}$, $V_{RT} - V_{RB} = 2V \pm 0.1V$.

7

ELECTRICAL CHARACTERISTICS

ANALOG DC CHARACTERISTICS

(V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Resolution		–				8	bits
Linearity Error	MB40578	LE	DC			±0.2	%
	MB40578-7					±0.4	
Equivalent Analog Input Resistance		R_{INA}		50			KΩ
Analog Input Capacitance		C_{INA}			120	230	pF
Analog High-Level Input Current		I_{IHA}				150	μA
Analog Low-Level Input Current		I_{ILA}				145	μA
Reference Current		I_{RB}	V_{RT} = 5 V V_{RB} = 3 V	–15	–9		mA

7

DIGITAL DC CHARACTERISTICS

(V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
High-Level Output Voltage	V_{OHD}	I_{OH} = –400 μA	2.7			V
Low-Level Output Voltage	V_{OLD}	I_{OL} = 1.6 mA			0.4	V
High-Level Input Voltage	V_{IHD}		2			V
Low-Level Input Voltage	V_{ILD}				0.8	V
Maximum Input Current	I_{ID}	V_{ID} = 7 V			100	μA
High-Level Input Current	I_{IHD}	V_{IHD} = 2.7 V		0	20	μA
Low-Level Input Current	I_{ILD}	V_{ILD} = 0.4 V	–400	–40		μA
Power Supply Current	I_{CC}			92	160	mA

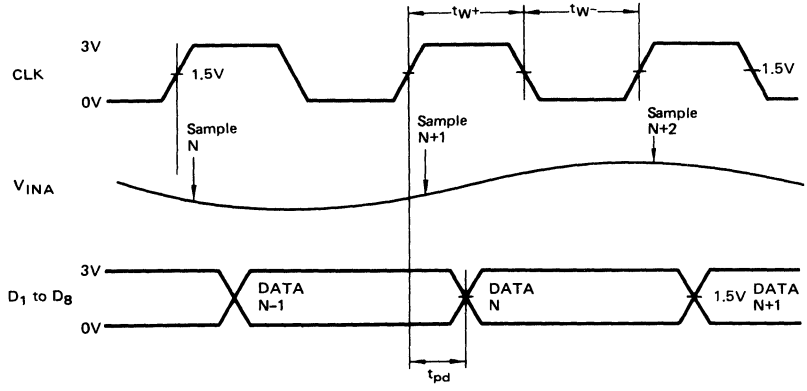
ELECTRICAL CHARACTERISTICS (continued)

SWITCHING CHARACTERISTICS

(V_{CC} = 5 V, T_A = 25°C)

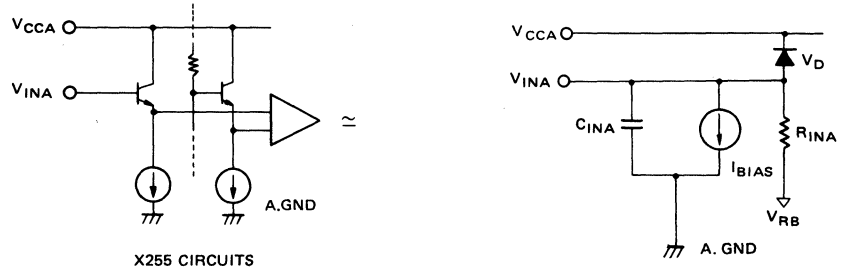
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Maximum Conversion Rate	FS		20	30		MSPS
Digital Output Delay Time	t_{pd}		5	15	40	ns

TIMING DIAGRAM



7

Fig. 2 – ANALOG INPUT EQUIVALENT CIRCUIT



C_{INA} : Non-linear Emitter-follower Junction Capacitance
R_{INA} : Linear Resistance Model for Input Current Transition by Comparator Switching:
Infinite value for $V_{IN} < V_{RB}$ or when CLK = High
V_{RB}: Voltage at V_{RB} terminal
I_{BIAS}: Constant Input Bias Current
V_D: The base-collector junction diode of emitter-follower transistor.

7

Fig. 3 – DIGITAL INPUT EQUIVALENT

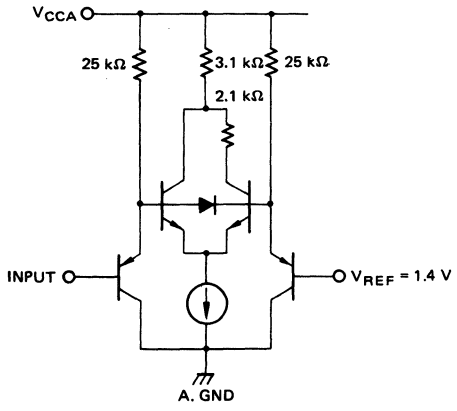
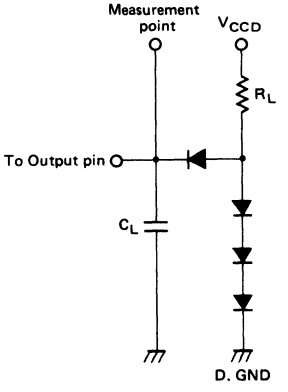


Fig. 4 – LOAD CIRCUIT FOR OUTPUT BUFFER



Note: $R_L = 2k\Omega$
C_L = 15pF including scope and jig capacitance
Diodes: IN3064 or equivalent

OUTPUT CODE

(V_{CC} = 5.0 V, $V_{RT} \fallingdotseq$ 5.0V, $V_{RB} \fallingdotseq$ 3.0V)

Step	Analog Input Voltage	Digital Output Code
0	2.960 V	00000000
1	2.968 V	00000001
⋮	⋮	⋮
127	3.976 V	01111111
128	3.984 V	10000000
129	3.992 V	10000001
⋮	⋮	⋮
254	4.992 V	11111110
255	5.000 V	11111111

Note: Ajust V_{ZT} = 2.964 V and V_{FT} = 4.996 V with V_{RT} and V_{RB}. The Analog Input Voltage are the center values of each step.

Fig. 5 — IDEAL CONVERSION CHARACTERISTICS

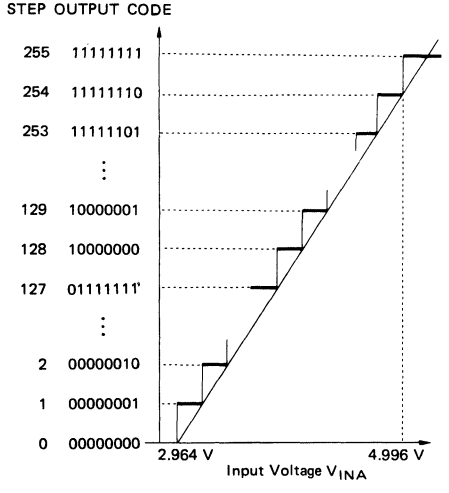
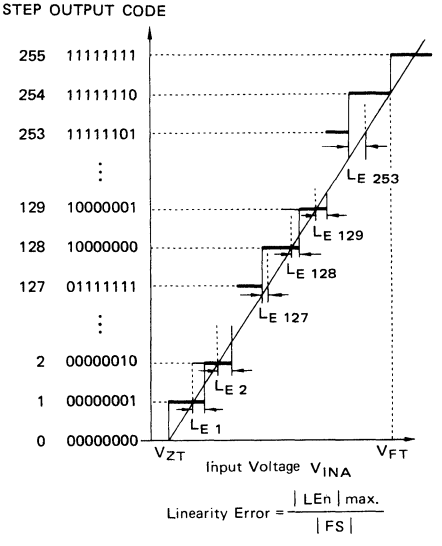


Fig. 6 — PRACTICAL CONVERSION CHARACTERISTICS

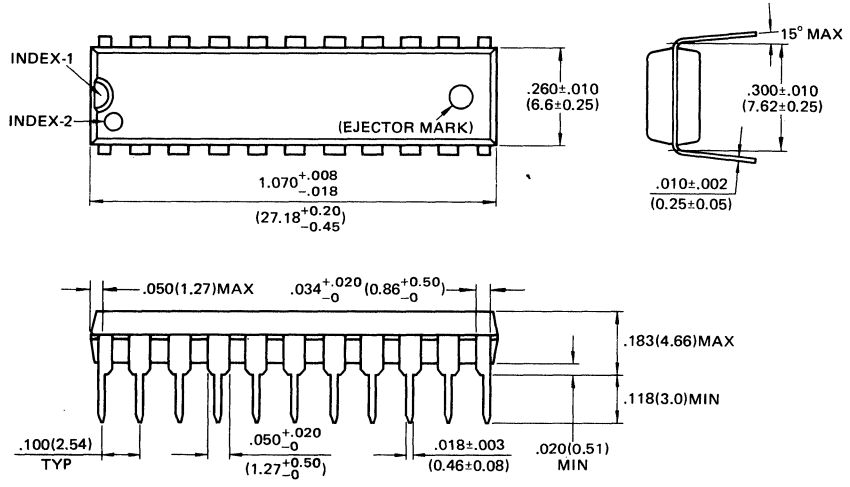


$$\text{Linearity Error} = \frac{|\,LEn\,|_{max.}}{|\,FS\,|}$$

7

PACKAGE DIMENSIONS

22-LEADS PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-22P-M04)



Dimensions in
inches (millimeters)

7

FUJITSU

8-BIT MULTIPLYING D/A CONVERTER

MB 4072

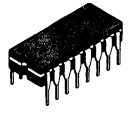
April 1984
Edition 1.0

HIGH-SPEED 8-BIT MULTIPLYING D/A CONVERTER

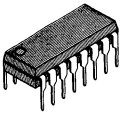
The Fujitsu MB 4072 is a High-Speed Digital to Analog Converter IC. The MB 4072's current outputs are high impedance open-collector, which provide voltage output with a load or current to voltage converter for various applications with operational amplifiers, microcomputers, etc.

Threshold level of digital inputs is variable with the level control input for various interface level.

- Settling Time : 85 ns
- Linearity Error : ±0.19% max.
- Full-scale Temperature coefficient : ±10 ppm/°C
- Output Voltage Compliance : -10 V to +18 V
- Multiplying Operation
- True/Complimentary Current Sink Output
- Adjustable Threshold Level of Digital Inputs: Interface directly with TTL, CMOS, ECL, etc.
- Wide Supply Voltage Range : ±4.5 V to ±18 V
- Low Power Consumption : 33 mW at ±5V
- Operation Temperature : -40°C to +85°C
- Package : Standard 16 pin DIP
- Compatible with DAC-08



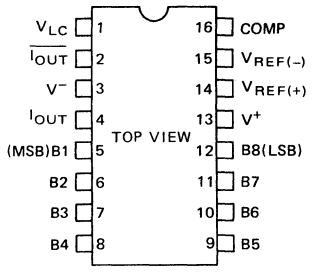
CERAMIC PACKAGE
DIP-16C-C02



PLASTIC PACKAGE
DIP-16P-M02

PLASTIC PACKAGE
FPT-16P-M02

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

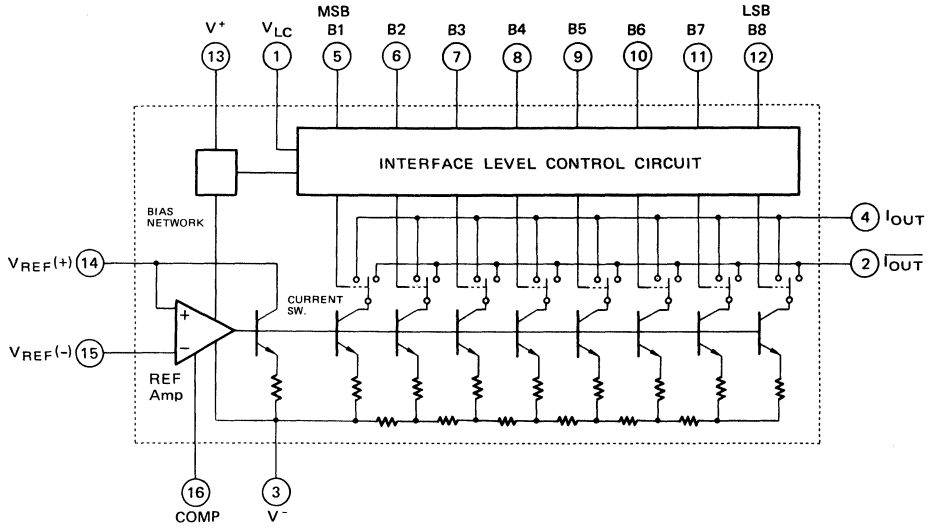
Parameter		Symbol	Ratings	Unit
Supply Voltage		V^+ to V^-	V^- to V^-+37	V
Digital Input Voltage		V_I	37	V
Threshold Control Voltage		V_{LC}	V^- to V^+	V
Reference Input Voltage		$V_{REF}(+)$	V^- to V^+	V
		$V_{REF}(-)$	V^- to V^+	V
Differential Reference Input Voltage		$V_{REF}(+)$ to $V_{REF}(-)$	±18.5	V
Reference Input Current		I_{REF}	5	mA
Power Consumption		P_D	500	mW
Storage Temp.	Ceramic	T_{STG}	-55 to +150	°C
	Plastic		-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

7

Fig. 1 – BLOCK DIAGRAM



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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V^+	+4.5		+18	V
	V^-	-4.5		-18	V
Operating Temperature	T_A	-40		+85	°C

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted. V^+ = +15 V, V^- = -15V, I_{REF} = 2.0 mA, T_A = -40°C to +85°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Resolution		8	8	8	bits
Monotonicity		8	8	8	bits
Linearity Error	LE			±0.19	%(FSR)
Settling Time (Final Value: ±1/2 LSB, T_A=25°C, On/Off Switching for Each bit/All bits)	t_s		85	150	ns
Propagation Delay Time (T_A=25°C, On/Off Switching for Each bit/All bits)	t_{PLH} t_{PHL}		35	60	ns
Temperature coefficient at full-scale	TC_{IFS}		±10	±50	ppm/°C
Output Voltage Range (ΔI_{FS} 1/2 LSB, R_{OUT} 20 MΩ typ.)	V_{OC}	-10		+18	V
Output Current at full-scale (V_{REF} = 10.000 V, R14 = 5.000 kΩ, R15 = 5.000 kΩ, T_A = 25°C)	I_{FS4}	1.94	1.99	2.04	mA
Symmetry at full-scale ($I_{FSS}=I_{FS4}-I_{FS2}$)	I_{FSS}		±1.0	±8.0	μA
Output Current at zero scale	I_{ZS}		0.2	2.0	μA
Output Current Range (R14 = 5.000 kΩ, R15 = 5.000 kΩ, V_{REF} = +15.0 V, V^- = -10 V)	I_{OR1}	2.1			mA
Output Current Range (R14 = 5.000 kΩ, R15 = 5.000 kΩ, V_{REF} = +25.0 V, V^- = -12 V)	I_{OR2}	4.2			mA
Low-level Input Voltage (V_{LC} = 0 V)	V_{IL}			0.8	V
High-level Input Voltage (V_{LC} = 0V)	V_{IH}	2.0			V
Low-level Input Current (V_{LC} = 0V, V_{IN} = -10 V to +0.8 V)	I_{IL}		-2.0	-10	μA
High-level Input Current (V_{LC} = 0 V, V_{IN} = 2.0 V to 18 V)	I_{IH}		0.002	10	μA

7

ELECTRICAL CHARACTERISTICS (Cont'd)

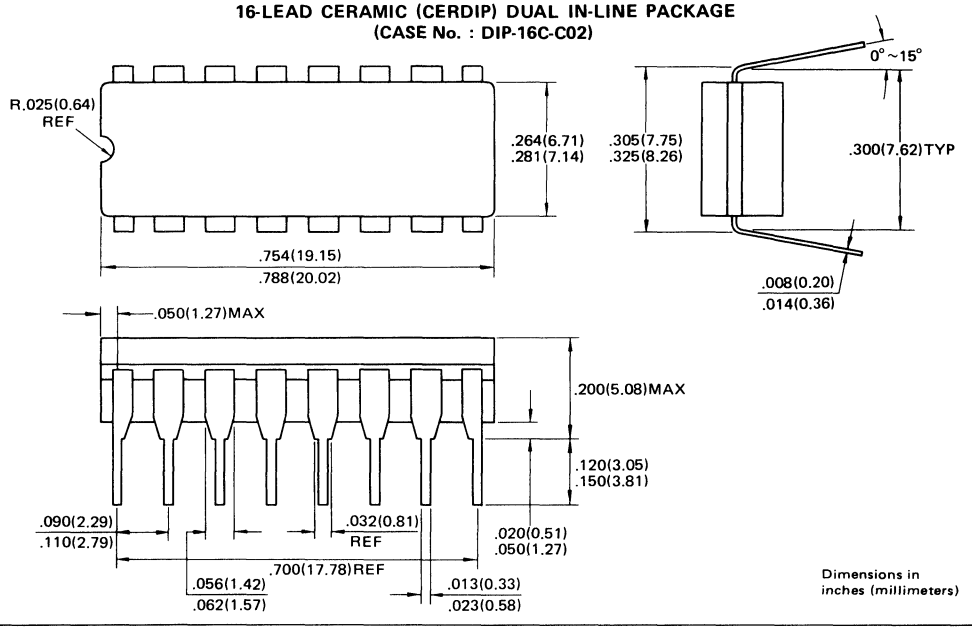
(Recommended Operating Conditions unless otherwise noted. $V^+ = +15$ V, $V^- = -15$ V, $I_{REF} = 2.0$ mA, $T_A = -40°C$ to $+85°C$)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Logic Input Voltage Range ($V^- = -15$ V)		V_{IS}	-10		+18	V
Logic Threshold Voltage Rnage ($V^+ = +15$ V, $V^- = -15$ V)		V_{THR}	-10		+13.5	V
Reference Bias Current		I_{15}		-1.0	-3.0	μA
Reference Input Through Rate ($R_{EQ} = 200\ \Omega$, $R_L = 100\ \Omega$, $C_L = 0$ pF)		$\frac{dI}{dt}$	4.0	8.0		mA/μs
Supply Voltage Sensitivity* ($V^+ = +4.5$ V to 18 V, $I_{REF} = 1$ mA)		$PSSI_{FS+}$		±0.0003	±0.01	%/%
Supply Voltage Sensitivity* ($V^- = -4.5$ V to -18 V, $I_{REF} = 1$ mA)		$PSSI_{FS-}$		±0.002	±0.01	%/%
Supply Current	($V^+ = +5$ V, $V^- = -5$ V, $I_{REF} = 1.0$ mA)	I^+		2.3	3.8	mA
		I^-		-4.3	-5.8	mA
	($V^+ = +5$ V, $V^- = -15$ V, $I_{REF} = 2.0$ mA)	I^+		2.4	3.8	mA
		I^-		-6.4	-7.8	mA
	($V^+ = +15$ V, $V^- = -15$ V, $I_{REF} = 2.0$mA)	I^+		2.5	3.8	mA
		I^-		-6.5	-7.8	mA
Power Dissipation	($V^+ = +5$ V, $V^- = -5$ V, $I_{REF} = 1.0$ mA)	P_D		33	48	mW
	($V^+ = 5$ V, $V^- = -15$ V, $I_{REF} = 2.0$ mA)	P_D		103	136	mW
	($V^+ = 15$ V, $V^- = -15$ V, $I_{REF} = 2.0$ mA)	P_D		135	174	mW

***Note:** $PSSI_{FS} = (\frac{\Delta I_{FS}}{I_{FS}} \times 100) / (\frac{18 - 4.5}{15} \times 100)$

PACKAGE DIMENSIONS

16-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No. : DIP-16C-C02)

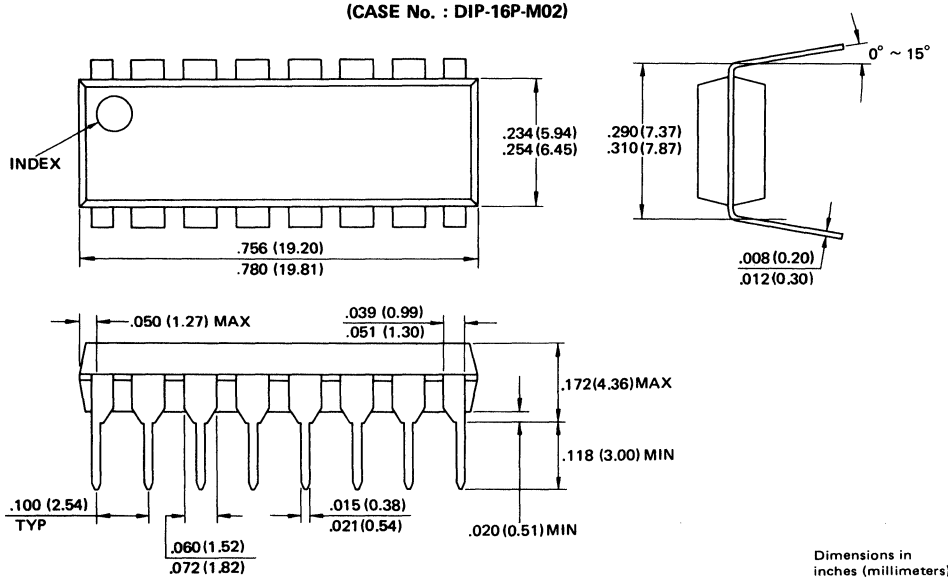


Dimensions in
inches (millimeters)

7

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M02)

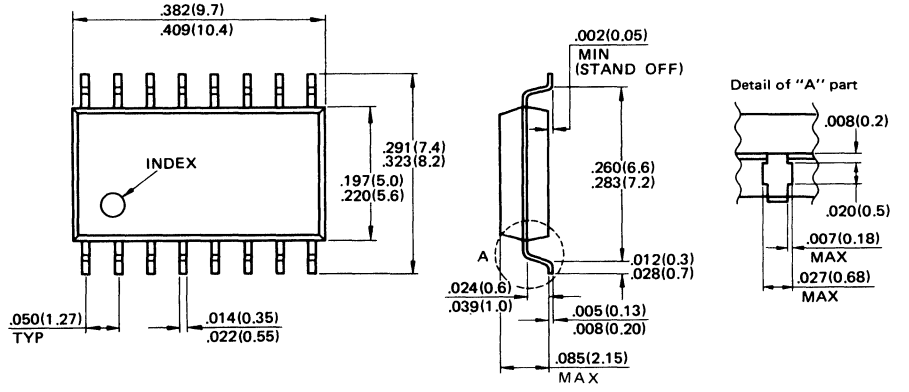


Dimensions in
inches (millimeters)

7

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



Dimensions in
inches (millimeters)

7

FUJITSU

NMOS 13-BIT × 1-CHANNEL, 6-BIT × 3-CHANNEL D/A CONVERTER

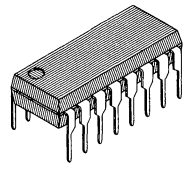
MB88301A

August 1987
Edition 3.2

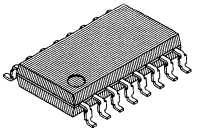
NMOS 13-BIT x 1-CHANNEL, 6-BIT x 3-CHANNEL D/A CONVERTER

The Fujitsu MB 88301A, a pulse width modulation (PWM) type digital-to-analog converter (DAC), is designed for interface with Fujitsu's MB 8840/8850 series and MB 88400/88500 series 4-bit single-ship microcomputers and also with a wide range of general 4-bit and 8-bit microprocessors.

The MB 88301A has four conversion outputs: one 13-bit resolution output and three 6-bit resolution outputs. All outputs generate positive pulse of varying pulse widths. The pulse widths vary in propotion to digital data programmed by the processor in the internal data register. With the connection of external filter circuits to the outputs, the MB 88301A provides an excellent, easy-to-configure DAC.



PLASTIC DIP
DIP-16P-M02

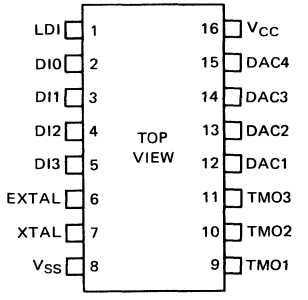


PLASTIC SOP
FPT-16P-M02

FEATURES

- Pulse width modulation D/A converter
- 4-bit parallel address/data loading
- Four on-chip pulse width modulators:
  - 13-bit resolution x 1 channel
  - 6-bit resolution x 3 channels
- On-chip 4 MHz clock generator with external crystal or ceramic resonator
- Clock cycle time / Clock frequency:
  - 0.25μs/4MHz for 13-bit resolution
  - 0.50μs/2MHz for 6-bit resolution
- Three synchronization clock outputs:
  - 2MHz clock output (4MHz divided by 2)
  - 15.625kHz clock output (4MHz divided by 2^8)
  - 488Hz clock output (4MHz divided by 2^{13})
- Single buffered conversion outputs.
- High-voltage open-drain conversion outputs
- Wide operating temperature range: -30°C to +70°C
- Single +5V power supply
- TTL compatible inputs/outputs
- N-channel silicon-gate E/D MOS process
- Two Package Options:
  - 16 pin plastic DIP (Suffix: -P)
  - 16 pin plastic SOP (Suffix: -PF)

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

7

Fig. 1 – LOGIC SYMBOL

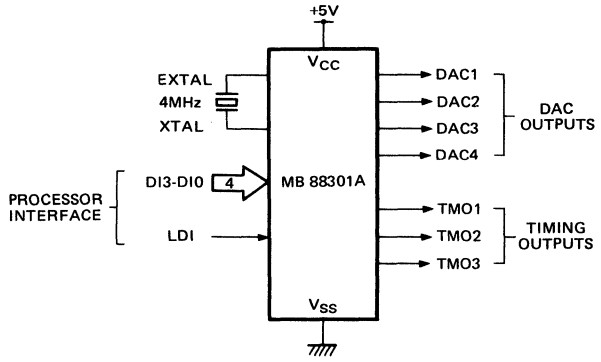
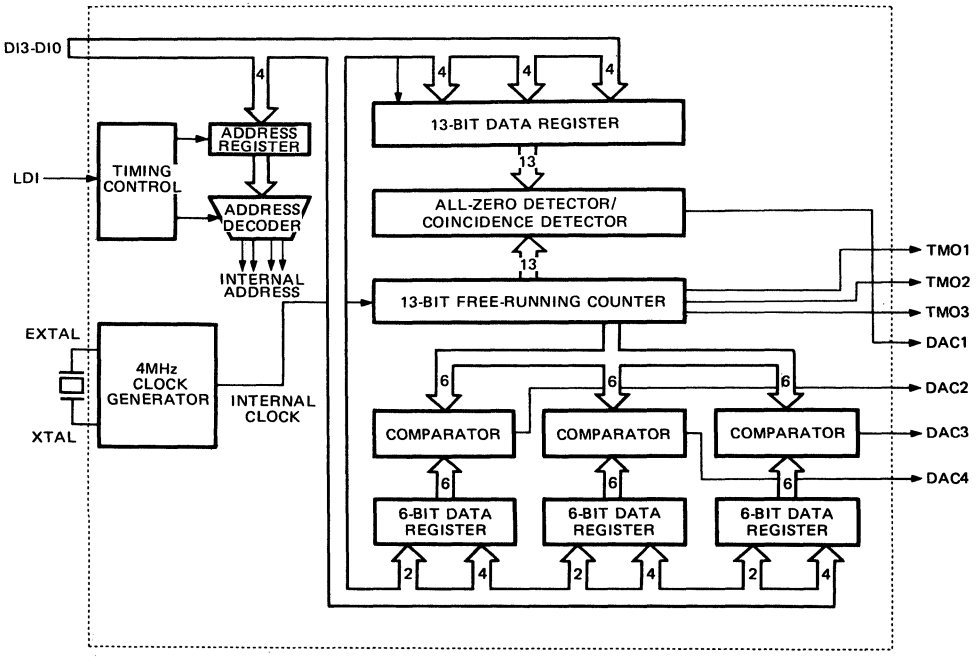


Fig. 2 – BLOCK DIAGRAM



7

PIN DESCRIPTION

The MB 88301A has two interfaces: One is the processor interface; D3-D0 and LDI, which are used for the processor to load the MB 88301A device with address and data. Another is the DAC/TIMING interface; DAC4-DAC1 and TM03-TM01, which are used for connection with user-designed external low-pass filter.

Table 1 – PIN DESCRIPTION

Symbol	Pin No.	Type	Function
V_{CC}	16	–	+5V power supply pin.
V_{SS}	8	–	Ground pin.
XTAL	7	–	External 4MHz crystal or ceramic resonator pins for the on-chip clock generator.
EXTAL	6	–	
DI3-DI0	5 to 2	I	4-bit parallel address/data input: The address/data format is that DI3 is the most significant bit (MSB) and that DI0 is the least significant bit (LSB). These inputs are TTL compatible. MSB LSB DI3 | DI2 | DI1 | DI0
LDI	1	I	Write strobe input for a 4-bit address/data: At the leading edge of LDI, a 4-bit address on the ID3 to ID0 inputs is latched into the internal address register. At the trailing edge of LDI, a 4-bit data on the DI3 to DI0 inputs are written into the internal data register designated by the address latched at the leading edge. This input is TTL compatible.
DAC1-DAC4	12 to 15	O	Pulse width modulator outputs (DAC outputs): DAC1: 13-bit resolution (one channel) DAC2-DAC4: 6-bit resolution (three channels) All four outputs are high-voltage open drain.
TMO1-TMO3	9 to 11	O	Synchronization clock outputs (Timing outputs): TMO1: 2MHz (4MHz divided by 2) TMO2: 15.625kHz (4MHz divided by 2^8) TMO3: 488Hz (4MHz divided by 2^{13}) All three clocks have a duty ratio of approximately 50%, and are TTL compatible.

7

FUNCTIONAL DESCRIPTION

GENERAL OPERATION

The MB 88301A is a pulse width modulation (PWM) type digital-to-analog converter (DAC). It converts digital data programmed by the processor in the internal data register (13-bit or 6-bit write-only register) into positive pulses. The width of these pulses is propotional to the value of the programmed data, and the cycle time of the pulses is defined by the resolution value (6 or 13 bits). The MB 88301A has four conversion outputs: channel 1 is a 13-bit resolution output DAC1, and channel 2 to 4 are 6-bit resolution outputs DAC2 to DAC4. The converted waveform appears at each DAC output. A user-designed external low-pass filter connected to the DAC output eliminates AC components from the output waveform and converts the waveform into a DC voltage propotional to the pulse width.

DIGITAL DATA INPUT

Fig. 3 shows the input timing of digital data to be converted: Digital data to define the width of the positive pulse is written into the 13-bit and 6-bit internal data registers through the DI3 to DI0 4-bit address/data inputs using the write strobe input LDI. At the leading edge of LDI, a 4-bit address on the DI3 to DI0 inputs is latched into the internal address register. At the trailing edge of LDI, a 4-bit data on the DI3 to DI0 inputs is loaded into the internal data register designated by the address register.

Fig. 4 shows the address/data format: DI3 is the most significant bit (MSB) and DI0 is the least significant bit (LSB).

Fig. 5 shows the internal data register address map: The whole space size is 10 words. Addresses #0 to #3, addresses #4 and #5, addresses #6 and #7, and addresses #8 and #9 are assigned to DAC1, DAC2, DAC3 and DAC4, respectively. Fig. 6 shows the internal data register format: To the DAC1 data register, three 4-bit and one 1-bit digital data must be written. To the DAC2 to DAC4 data registers, one 4-bit and one 2-bit digital data must be written.

Fig. 5 — INTERNAL DATA REGISTER ADDRESS MAP

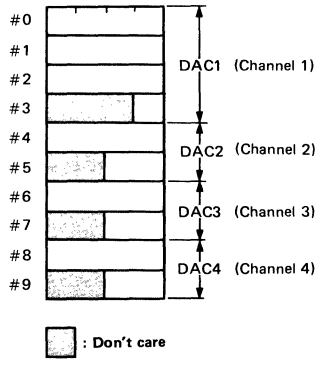


Fig. 3 — ADDRESS/DATA INPUT TIMING

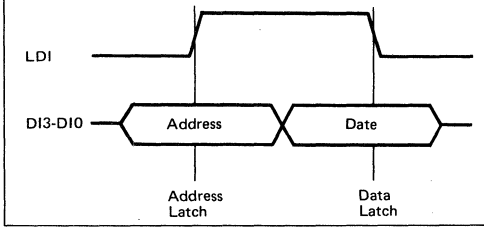


Fig. 4 — ADDRESS/DATA FORMAT

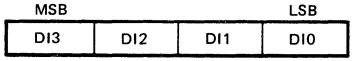
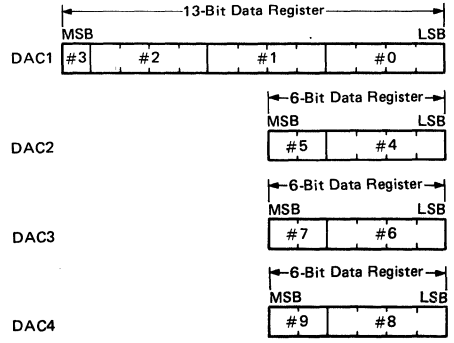


Fig. 6 — INTERNAL DATA REGISTER FORMAT



PULSE WIDTH MODULATION/DAC OUTPUT WAVEFORM Fig.

• 13-Bit Resolution D/A Converter: DAC1

Fig. 7 shows the configuration of the 13-bit resolution pulse width modulator: The on-chip clock generater provides 4MHz clock for the 13-bit free-running counter. When all bits of the counter is zero, the all-zero detector sets the output R-R-S flip-flop. The coincidence detector compares the counter with the data register. When they match, the coincidence detector resets the output flip-flop. The waveform appearing at the DAC1 output depends on the data register value, shown in Fig. 8.

Fig. 7 — 13-BIT PULSE WIDTH MODULATOR CONFIGURATION

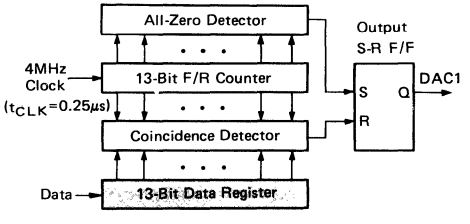
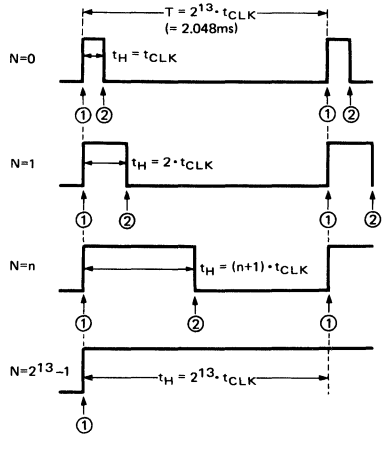


Fig. 8 — DAC1 OUTPUT WAVEFORM



NOTES: N : DATA REGISTER VALUE ($0 \leqq N \leqq 2^{13}-1$)
T : PULSE CYCLE TIME ($T = 2^{13} \cdot t_{CLK} = 2.048$ms)
t_H : PULSE WIDTH ($t_H = (N+1) \cdot t_{CLK}$)
t_{CLK} : COUNTER CLOCK CYCLE TIME ($t_{CLK} = 1/4$MHz $= 0.25\mu$s)
① : COUNTER IS ZERO.
② : COUNTER MATCHES DATA REGISTER.

• 6-Bit Resolution D/A Converters: DAC2 to DAC4

Fig. 9 shows the configulation of the 6-bit resolution pulse width modulator: The 2MHz clock that is the output of Bit 1 of the 13-bit free-running counter drives the 6-bit free-running counter. This 6-bit counter is also part of the 13-bit counter (Bits 2 to 7). The comparator compares the counter with the data register every cycle. When the counter value is equal to or less than the data register value, the comparator outputs a high level at the DAC output. When the counter value exceeds the date register value, the comparator outputs a low level at the DAC output. This produces the waveforms at the DAC2, DAC3, and DAC4 outputs, shown in Fig. 10.

Fig. 9 — 6-BIT PULSE WIDTH MODULATOR CONFIGURATION

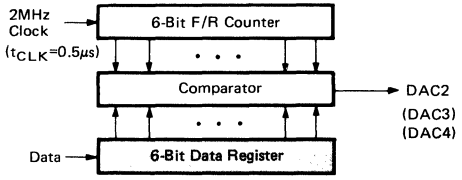
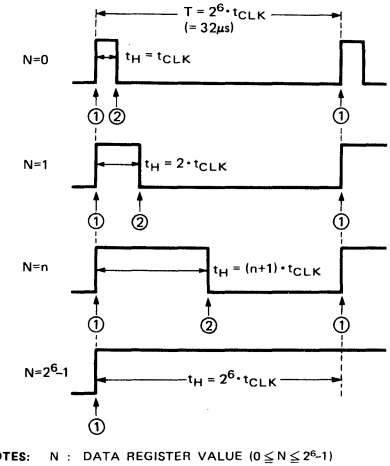


Fig. 10 — DAC2/DAC3/DAC4 OUTPUT WAVEFORM



NOTES: N : DATA REGISTER VALUE ($0 \leqq N \leqq 2^{6}-1$)
T : PULSE CYCLE TIME ($T = 2^{6} \cdot t_{CLK} = 32\mu$s)
t_H : PULSE WIDTH ($t_H = (N+1) \cdot t_{CLK}$)
t_{CLK} : COUNTER CLOCK CYCLE TIME ($t_{CLK} = 1/2$MHz $= 0.5\mu$s)
① : COUNTER IS ZERO. (OVERFLOW)
② : COUNTER EXCEEDS DATA REGISTER.

7

EXTERNAL FILTER CONFIGURATION

The on-chip pulse width modulator generates positive pulse waveforms similar to the one shown in Fig. 12 at the DAC outputs (DAC1 to DAC4). The pulse width (t_H) is proportional to the digital data programmed into the data register. The cycle time (T) is determined by the resolution value (6 or 13 bits).

User-designed low-pass filters are required at the DAC outputs to eliminate AC components from the output waveform and to convert the waveform to a DC voltage. Fig. 11 shows an example of a simple output configuration in which an RC integrator is used as the low-pass filter. With this circuit, the DAC waveform shown in Fig. 12 is converted to the V_{OUT} output waveform shown in Fig. 13 Ripple and response time (t_R) depend on the time constant of the RC filter. A longer time constant reduces ripple but increases response time. A time constant that best meets the tradeoff between desired accuracy and response time should be chosen. Also, since the DAC outputs are high-voltage open drain, they can externally be pulled up to a power supply higher than 5V. This prevents the output voltage from attenuating through the external low-pass filters.

Note:
The low-pass filter shown in Fig. 11 is just an example. In actual practice, depending on the user's system design, additional amplifiers, multi-stage filters, and other circuits will be needed for the external low-pass filter.

7

NOTICE

To change the DC output voltage of the external low-pass filter, the data register value must be updated to vary the positive pulse width (duty ratio) of the DAC output. However, all bits on the data register can not be changed at the same time. They are updated a nibble at a time by the 4-bit parallel data loading. In addition, the DAC output is single buffered. Because of this nibble-by-nibble update and single buffering, the data register value during update may become transient. During this pulse cycle, depending on the transient value, an undesirable duty ratio disturbance may occur at the DAC output, affecting the filter output. It is therefore necessary to design the output filter so that such disturbances in the DAC output waveform will not appear at the filter output. This notice applies to both the 13-bit and 6-bit resolution converters. With the 13-bit resolution converter, however, it is possible to avoid such disturbance by software. This is done by controlling the update timing of the data register value through monitoring of the DAC1 output and the TMO3 output waveforms.

Also, note the following thing when the DAC1 output is used: In the steady state where the DAC1 data register bits are all set (i.e., data is "1FFF") the DAC1 output remains high. But, when the data is updated, there is a possibility that the DAC1 output may become undefined during that output cycle time (less than one cycle time). To avoid this phenomenon, the following method is utilized:

1. Not use data of "1FFF", or
2. Change the DAC1 data register value (i.e., "1FFF") just before the counter become full (i.e., all bits are set). Since in this case an undesired pulse due to the data change may appear at the DAC1 output, the pulse must be eliminated with the external filter.

Fig. 11 – OUTPUT CIRCUIT CONFIGURATION (EXAMPLE)

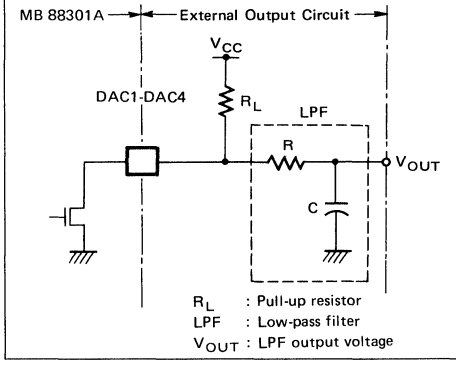


Fig. 12 – DAC OUTPUT WAVEFORM

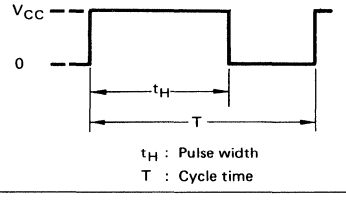
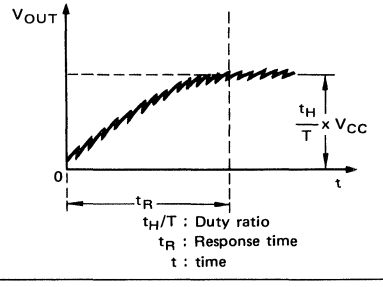


Fig. 13 – V_{OUT} OUTPUT WAVEFORM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Pins/Conditions	
Supply Voltage	V_{CC}	V_{SS} −0.3 to V_{SS} +8.0	V	V_{CC}	V_{SS} = 0 V
Input Voltage	V_{IN}	V_{SS} −0.3 to V_{SS} +8.0	V	DI0-DI3, LDI, EXTAL, XTAL	
Output Voltage	V_{OUT}	V_{SS} −0.3 to V_{SS} +15.0	V	DAC1-DAC4	
		V_{SS} −0.3 to V_{SS} +8.0		TMO1-TMO3	
Operating Temperature	T_A	−30 to +70	°C	Ambient temperature	
Storage Temperature	T_{stg}	−55 to +150	°C		

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}		0		
Input High Voltage	V_{IH}	2.0		V_{CC}	V
Input Low Voltage	V_{IL}	−0.3		0.8	V
Clock Frequency*	f_c	0.5		4.0	MHz
Operating Temperature	T_A	−30		70	°C

NOTE: * Crystal or ceramic resonator should be used. See Fig. 17.

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pins/Conditions	Value			Unit
			Min.	Typ.	Max.	
Output High Voltage	V_{OH}	TMO1-TMO3 I_{OH} = −200μA	2.4			V
		DAC1-DAC4	Open Drain			
Output Low Voltage	V_{OL}	TMO1-TMO3 I_{OL} = 1.8mA			0.4	V
		DAC1-DAC4 I_{OL} = 2.0mA, 5kΩ External Pull Up Resistor			0.8	V
Output Leakage Current	I_{LOH}	DAC1-DAC4 V_{OH} = 13.2V, OFF State			50	μA
Supply Current	I_{CC}	V_{CC} = 5.5V, All Outputs Open		15	25	mA

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AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Pins/Conditions	Min.		Max.	Unit
LDI Pulse Width	P_{WLDI}	LDI Fig. 14, Fig. 16	5			μs
LDI Rise/Fall times	t_{rLDI} t_{fLDI}	LDI Fig. 14, Fig. 16			1.5	μs
Address/Data Setup Time	t_S	DI3 - DI0 Fig. 14, Fig. 16	0.5			μs
Address/Data Hold Time	t_H	DI3 - DI0 Fig. 14, Fig. 16	2			μs
TMO Rise/Fall times	t_{rTMO} t_{fTMO}	TM01-TM03 Fig. 15, Fig. 16			0.2	μs

Fig. 14 – ADDRESS/DATA INPUT TIMING

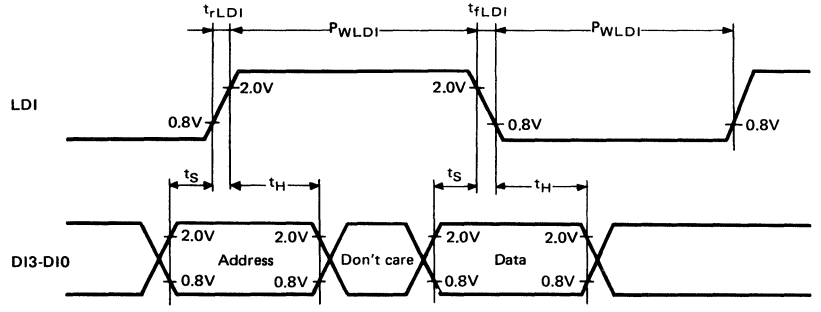


Fig. 15 – SYNCHRONIZATION CLOCK OUTPUT TIMING

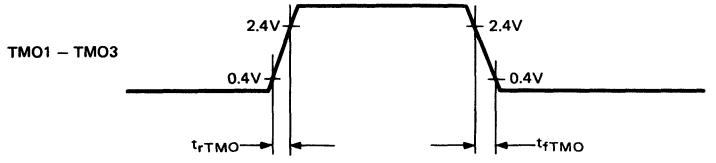
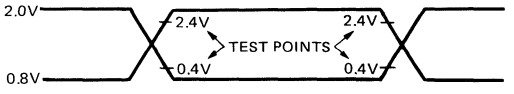


Fig. 16 – AC TEST CONDITIONS

INPUT CONDITIONS

- Input Levels:
  2.0V for a logic "1"
  0.8V for a logic "0"



OUTPUT CONDITIONS

- Timing Reference Levels:
  2.4V for a logic "1"
  0.4V for a logic "0"
- Output Load Circuit:
  C_L = 100pF (including scope and jig capacitances)
  R_L = 4kΩ

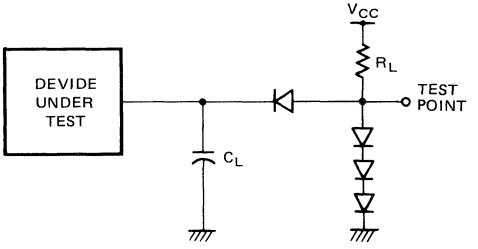
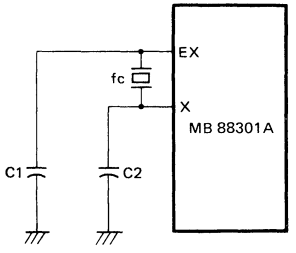


Fig. 17 – CRYSTAL/CERAMIC OSCILLATOR CIRCUIT



fc = 4MHz
C1 = C2 = 20pF – 60pF

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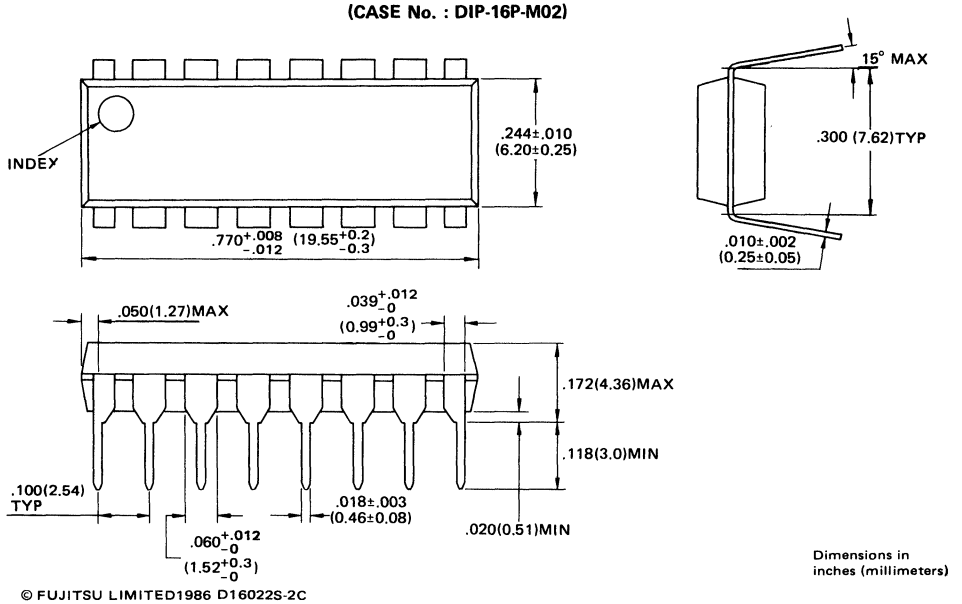
PACKAGE DIMENSIONS

PLASTIC DIP (Suffix: -P)

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M02)



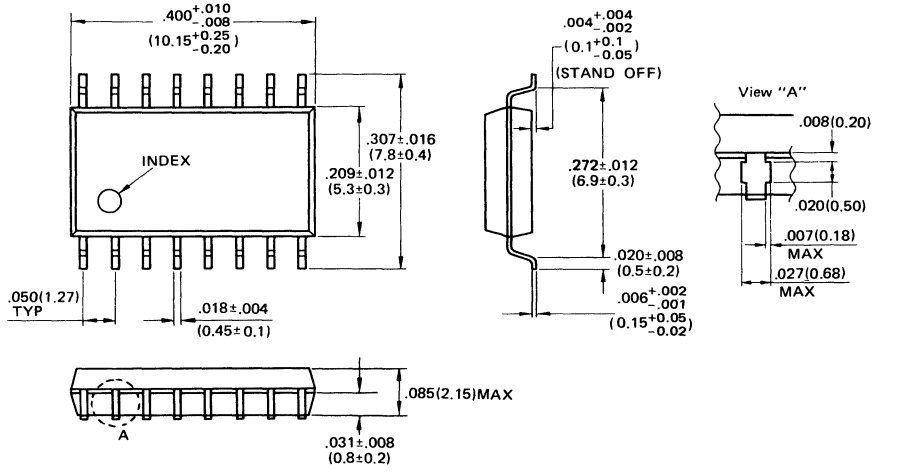
Dimensions in inches (millimeters)

7

PACKAGE DIMENSIONS

PLASTIC SOP(Suffix: -PF)

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



Dimensions in
inches (millimeters)

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October 1989
Edition 1.0

FUJITSU

DATA SHEET

MB88341/MB88342

R-2R TYPE 8-BIT D/A CONVERTER

DESCRIPTION

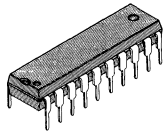
The Fujitsu MB88341 and MB88342 are R–2R type 8–bit resolution digital–to–analog converters (DAC), designed for interface with a wide range of general 4–bit and 8–bit microcomputers including Fujitsu's MB8840/50 series and MB88400/500 series 4–bit single–chip microcomputers.

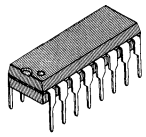
The MB88341 has an 8–bit x 12–channel D/A converter and the MB88342 has an 8–bit x 8–channel D/A converter. Digital data are input serially by individual channel units. The loaded digital data are convertered into analog DC voltages by the D/A converter in 60 µs settling time. The MB88341 and MB88342 are suitable for electronic volumes and replacement for potentiometers for adjustment, in addition to normal D/A converter applications.

FEATURES

- Conversion method : R–2R resistor ladder
- MB88341 : 8–bit x 12–channel D/A converter
- MB88342 : 8–bit x 8–channel D/A converter
- Serial data input
- Serial data output for cascade connection
- 60 µs DAC output settling time
- Two separate power supply/ground lines for digital and analog blocks.
- Single +5V power supply
- Wide operating temperature range: –20°C to +85°C
- Silicon–gate CMOS process
- Three package options :
  - –MB88341: 20–pin plastic DIP (Suffix : –P), 20–pin plastic SOP (Suffix : –PF), 20–pin plastic SSOP (Suffix : –PFV)
  - –MB88342: 16–pin plastic DIP (Suffix : –P), 16–pin plastic SOP (Suffix : –PF), 20–pin plastic SSOP (Suffix : –PFV)

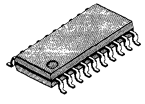
MB88341–P **MB88342–P**

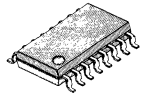




PLASTIC DIP (DIP–20P–M02) **PLASTIC DIP (DIP–16P–M04)**

MB88341–PF **MB88342–PF**





PLASTIC SOP (FPT–20P–M01) **PLASTIC SOP (FPT–16P–M02)**

MB88341–PFV/MB88342–PFV

PLASTIC SSOP (FPT–20P–M03)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Figure 1 Pin Assignment

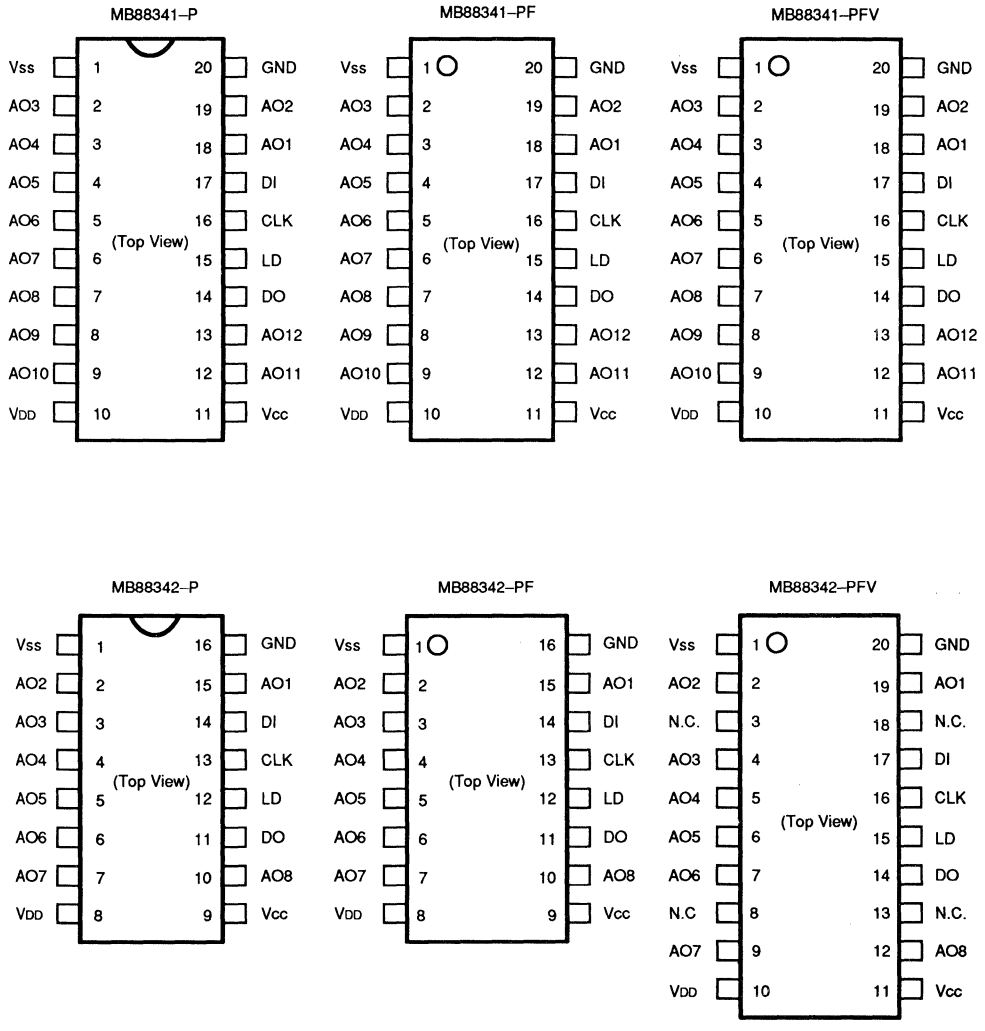


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Figure 2 Logic Symbol

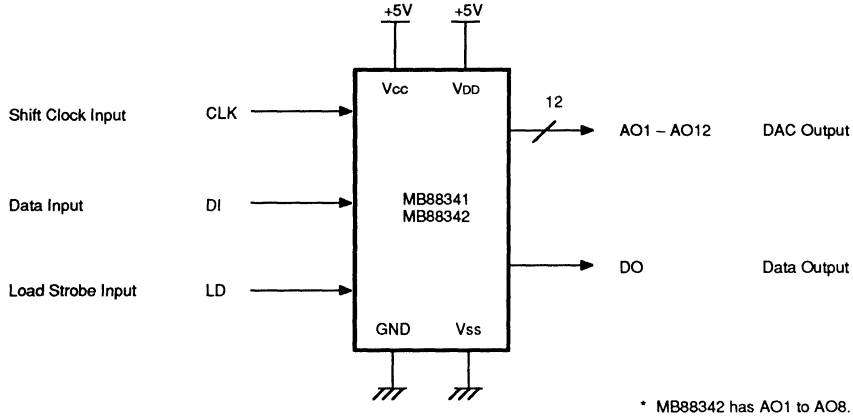
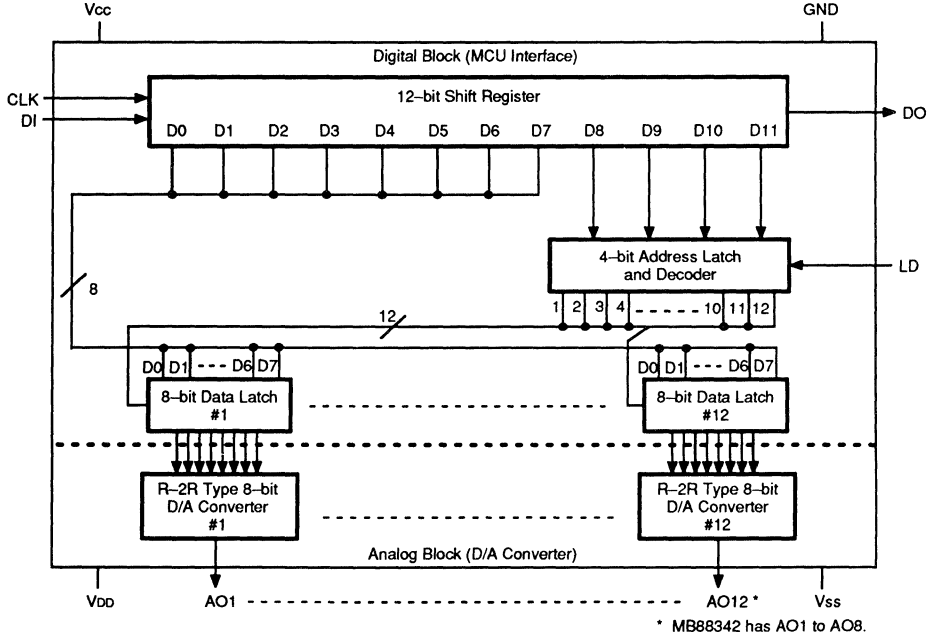


Figure 3 Block Diagram



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PIN DESCRIPTION

Figure 1 and Table 1 show the pin assignment and pin description of the MB88341 and MB88342.

Table 1 Pin Description

Symbol	Pin No. MB88341	Pin No. MB88342	Type	Name & Function
Power Supply				
Vcc	11	9 (11)	–	+5V DC power supply pin for the digital block (MCU interface).
GND	20	16 (20)	–	Ground pin for the digital block (MCU interface).
VDD	10	8 (10)	–	+5V DC power supply pin for the analog block (D/A converter).
Vss	1	1 (1)	–	Ground pin for the analog block (D/A converter).
Control Input				
CLK	16	13 (16)	I	Shift clock input to the internal 12–bit shift register: At the rising edge of CLK data on the DI pin is shifted into the LSB of the shift register and contents of the shift register are shifted right (to the MSB).
LD	15	12 (15)	I	Load strobe input for a 12–bit address/data : A high level on the LD pin latches a 4–bit address (upper 4 bits: D11 to D8) of the internal 12–bit shift register into the internal address latch/decoder, and writes 8–bit data (lower 8 bits: D7 to D0) of the shift register into an internal data latch selected by the latched address.
Data Input/Output				
DI	17	14 (17)	I	Serial address/data input to the internal 12–bit shift register: The address/data format is that upper 4 bits (D11 to D8) indicate an address and lower 8 bits (D7 to D0) indicate data. The D11 (MSB) is the first–in bit and D0 (LSB) is the last–in bit.
DO	14	11 (14)	O	Serial address/data output from the internal 12–bit shift register: This is an output pin of the MSB bit data of the 12–bit shift register. This pin allows a cascade connection of the device.
DAC Output				
AO1	18	15 (19)	O	8–bit resolution D/A converter outputs : MB88341: 12 channels (AO1 to AO12) MB88342: 8 channels (AO1 to AO8)
AO2	19	2 (2)		
AO3	2	3 (4)		
AO4	3	4 (5)		
AO5	4	5 (6)		
AO6	5	6 (7)		
AO7	6	7 (9)		
AO8	7	10 (12)		
AO9	8	– (–)		
AO10	9	– (–)		
AO11	12	– (–)		
AO12	13	– (–)		

Note : Pin numbers in parentheses are applied to MB88342–PFV.

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FUNCTIONAL DESCRIPTION

OVERVIEW

The MB88341 and MB88342 are R–2R resistor ladder type, 8–bit resolution digital–to–analog converter (DAC) devices. The MB88341 has 12 channels, and MB88342 has 8 channels of D/A converters. 8–bit digital data are loaded into internal data latches by individual DAC channel units. The loaded digital data are converted into analog DC voltages through the internal D/A converter in 60 µs settling time. For cascade connection, a serial data output is provided.

DEVICE CONFIGURATION

As illustrated in Figure 3 block diagram, the MB88341 (MB88342) device is composed by the digital block (MCU interface) and analog block (D/A converter). The digital block consists of a 12–bit shift register, a 4–bit address latch/decoder, and 12 (8) 8–bit data latches. The analog block includes 12 (8) 8–bit D/A converters connecting to the data latches. For electrically stable operation the power supply and ground lines are separate between the digital block (for MCU interface) and analog block (for D/A converter).

DEVICE OPERATION

Figure 4 shows the input/output timing. A 12–bit address/data is serially input into the shift register through the DI pin synchronously with the rising edge of CLK. The format of the shift register is shown in Figure 5. The lower 8 bits (D7 to D0) are data bits to be converted, and the upper 4 bits are address bits (D11 to D8) to select a data latch to be written. A high level on the LD pin loads the address latch/decoder with the 4–bit address to select a data latch, and writes the 8–bit data into a selected data latch. Figure 6 shows the data latch address map, and Table 2, address decoding. 8–bit data written into individual data latches are converted into analog DC voltages, dividing the supply voltage |V_{DD}–Vss| through R–2R resistor ladders of D/A converters. Figure 7 shows the R–2R resistor ladder D/A converter configuration, and Table 3 analog DC voltages corresponding to each digital data.

Figure 4 Input/Output Timing

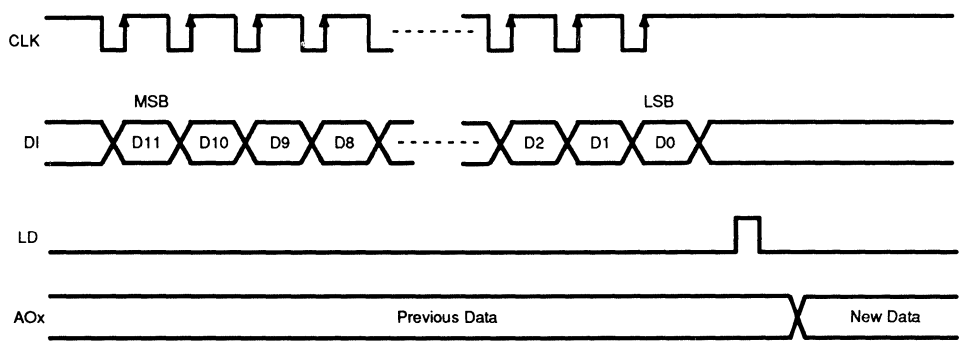

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Figure 5 Shift Register Format

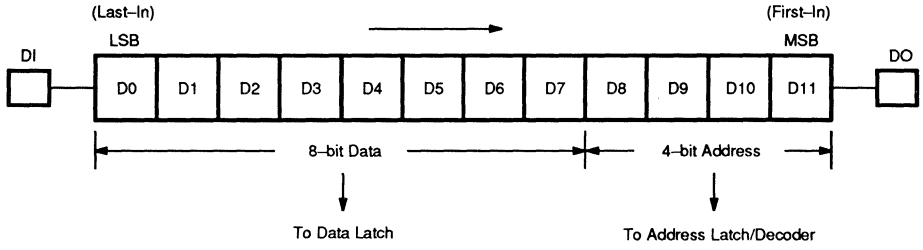

Figure 6 Data Latch Address Map

Address			
1H	Data Latch #1	D/A Converter #1	AO1
2H	Data Latch #2	D/A Converter #2	AO2
3H	Data Latch #3	D/A Converter #3	AO3
4H	Data Latch #4	D/A Converter #4	AO4
5H	Data Latch #5	D/A Converter #5	AO5
6H	Data Latch #6	D/A Converter #6	AO6
7H	Data Latch #7	D/A Converter #7	AO7
8H	Data Latch #8	D/A Converter #8	AO8
9H	Data Latch #9 *	D/A Converter #9 *	AO9 *
AH	Data Latch #10 *	D/A Converter #10 *	AO10 *
BH	Data Latch #11 *	D/A Converter #11 *	AO11 *
CH	Data Latch #12 *	D/A Converter #12 *	AO12 *

* : Available on MB88341 only

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Figure 7 R–2R Resistor Ladder D/A Converter Configuration

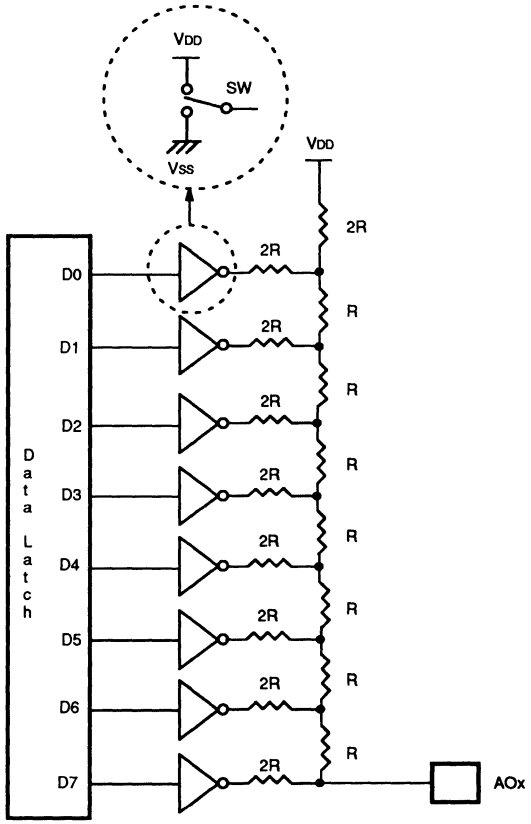


Table 2 Address Decoding

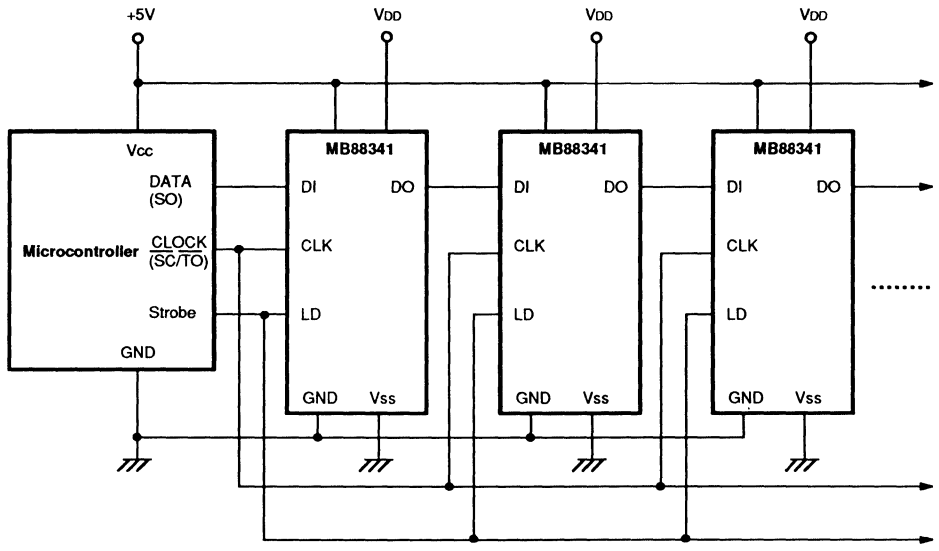
Address				Data Latch Selected	
D8	D9	D10	D11	MB88341	MB88342
0	0	0	0	Deselected	
0	0	0	1	Data Latch #1	
0	0	1	0	Data Latch #2	
0	0	1	1	Data Latch #3	
0	1	0	0	Data Latch #4	
0	1	0	1	Data Latch #5	
0	1	1	0	Data Latch #6	
0	1	1	1	Data Latch #7	
1	0	0	0	Data Latch #8	
1	0	0	1	Data Latch #9	Deselected
1	0	1	0	Data Latch #10	Deselected
1	0	1	1	Data Latch #11	Deselected
1	1	0	0	Data Latch #12	Deselected
1	1	0	1	Deselected	
1	1	1	0	Deselected	
1	1	1	1	Deselected	

7

Table 3 Data Conversion

Data								DAC Output Level
D7	D6	D5	D4	D3	D2	D1	D0	AOx
0	0	0	0	0	0	0	0	$\approx \lvert V_{DD} - V_{SS} \rvert \times 1/256$
0	0	0	0	0	0	0	1	$\approx \lvert V_{DD} - V_{SS} \rvert \times 2/256$
0	0	0	0	0	0	1	0	$\approx \lvert V_{DD} - V_{SS} \rvert \times 3/256$
0	0	0	0	0	0	1	1	$\approx \lvert V_{DD} - V_{SS} \rvert \times 4/256$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	1	1	0	$\approx \lvert V_{DD} - V_{SS} \rvert \times 255/256$
1	1	1	1	1	1	1	1	$\approx \lvert V_{DD} - V_{SS} \rvert$

Figure 8 Cascade Connection Example

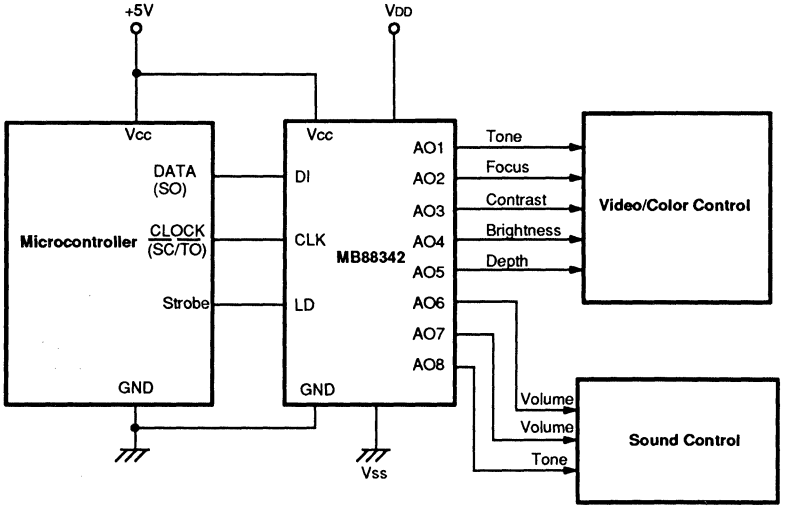


7

APPLICATION DESCRIPTION

The MB88341 and MB88342 are suitable for electronic volumes and replacement for adjustment potentiometers, in addition to normal D/A converter applications. Figure 8 illustrates an application example for TV set.

Figure 9 Application Example (for TV Set)



7

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS †

Parameter	Symbol	Rating			Unit	Condition
		Min	Typ	Max		
Supply Voltage	V_{CC}	−0.3		7.0	V	Ta = 25°C GND = 0 V
	V_{DD}	−0.3		7.0	V	
Input Voltage	V_{IN}	−0.3		7.0	V	Ta = 25°C GND = 0 V Should not exceed Vcc + 0.3V
Output Voltage	V_{OUT}	−0.3		7.0	V	
Power Dissipation	P_D			250	mW	
Operating Ambient Temperature	T_A	−20		+85	°C	
Storage Temperature	T_{STG}	−55		+150	°C	

† Permanent device damage may occur if the above ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Condition
		Min	Typ	Max		
Supply Voltage (for Digital Block)	Vcc	4.5	5.0	5.5	V	
	GND		0		V	
Supply Voltage (for Analog Block)	V_{DD}	3.0		Vcc	V	$V_{DD} \leq$ Vcc, Monotonicity, No load
	Vss	0		1.0	V	
Operating Ambient Temperature	T_A	−20		+85	°C	

7

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Digital Block (MCU Interface)

Parameter	Symbol	Value			Unit	Condition
		Min	Typ.	Max		
Active Supply Current	I_{CC}			1.0	mA	CLK = 1MHz
Standby Supply Current	I_{CCS}			10	µA	All inputs (including CLK) fixed at Vcc or GND. All outputs open.
Input Leakage Current	I_{ILK}	–10		10	µA	V_{IN} = 0 to Vcc
Input Low Voltage	V_{IL}			0.2•Vcc	V	
Input High Voltage	V_{IH}	0.8•Vcc			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 2.5 mA
Output High Voltage	V_{OH}	Vcc–0.4			V	I_{OH} = –400 µA

Analog Block (D/A Converter)

Parameter	Symbol	Value			Unit	Condition	
		Min	Typ	Max			
Supply Current	I_{DD}		1.5	3.0	mA	MB88341	No load
			1.2	2.5	mA	MB88342	
Resolution		8			bit	Monotonicity, I_{OUT} = –0.01 µA	
Variation of Linearity among Channels				±3	LSB	Monotonicity, No load	

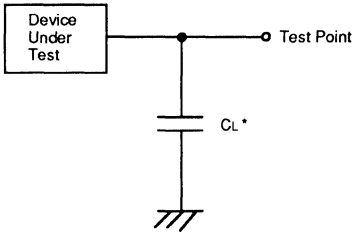
7

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

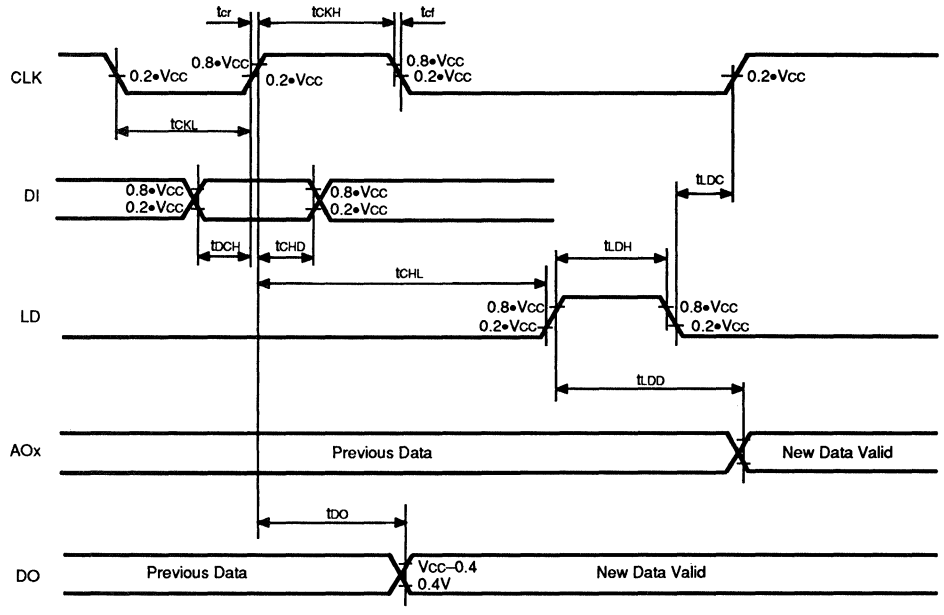
Parameter	Symbol	Value		Unit	Condition
		Min	Max		
Clock Low Time	t_{CKL}	200		ns	
Clock High Time	t_{CKH}	200		ns	
Clock Rise Time	t_{Cr}		200	ns	
Clock Fall Time	t_{Cf}		200	ns	
Data Setup Time	t_{DCH}	30		ns	
Data Hold Time	t_{CHD}	60		ns	
Load Strobe High Time	t_{LDH}	100		ns	
Load Strobe Setup Time	t_{CHL}	200		ns	
Load Strobe Hold Time	t_{LDC}	100		ns	
DAC Output Settling Time	t_{LDD}		60	µs	No load
Data Output Delay Time	t_{DO}	70	350	ns	*C_L = 20 pF (Min.), 100 pF (Max.)

Figure 10 AC Test Conditions



7

Figure 11 Input/Output Timing



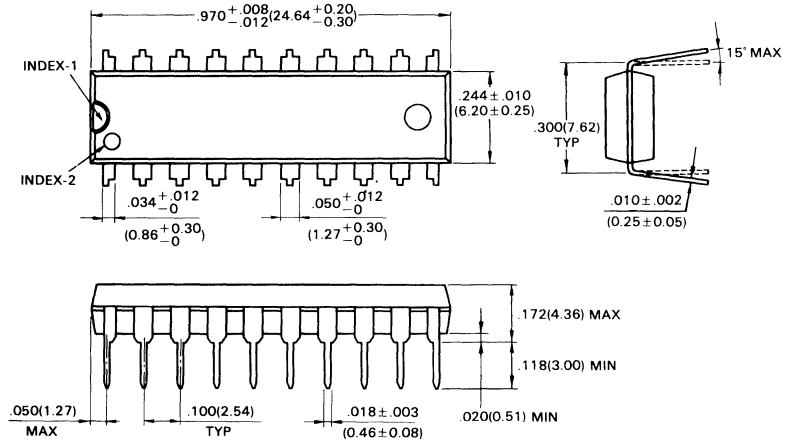
7

PACKAGE DIMENSIONS

MB88341–P

20-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-20P-M02)



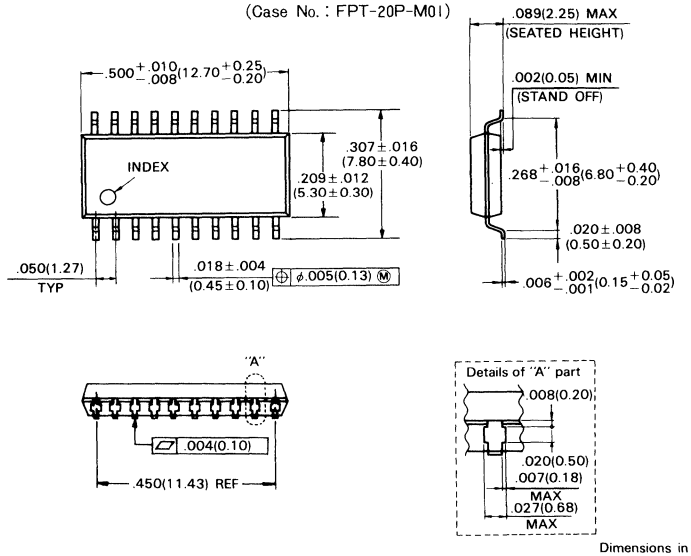
Dimensions in
inches (millimeters)

7

MB88341-PF

20-LEAD PLASTIC FLAT PACKAGE

(Case No. : FPT-20P-M01)

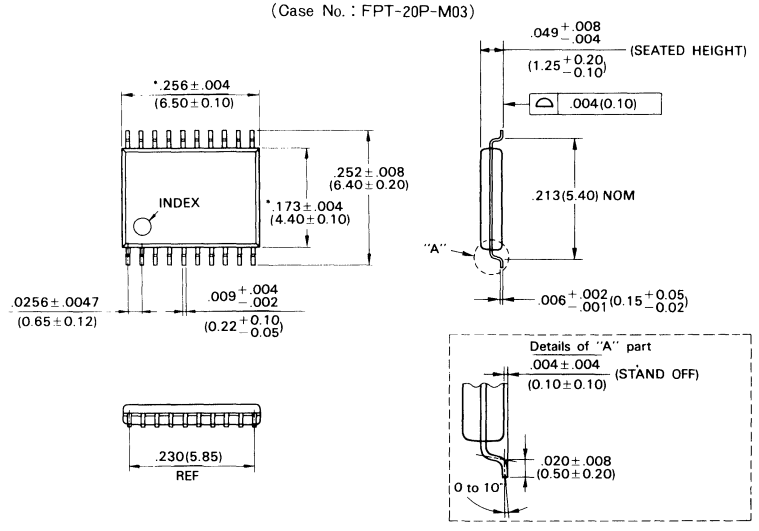


Dimensions in inches (millimeters)

7

MB88341–PFV

20-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-20P-M03)



* : This dimension does not include resin protrusion.

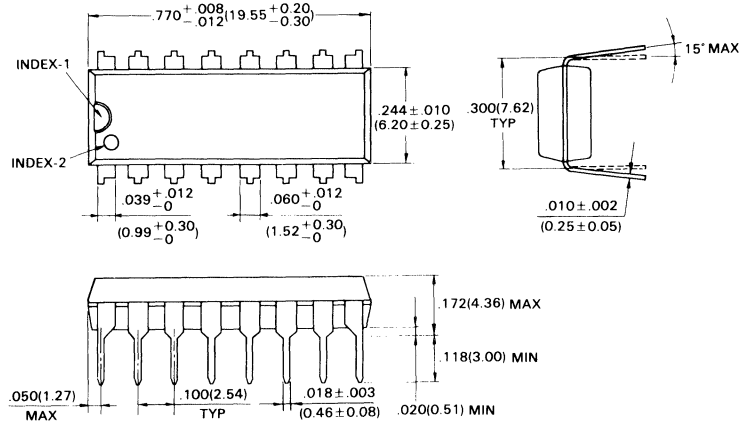
Dimensions in inches (millimeters)

7

MB88342-P

16-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-16P-M04)



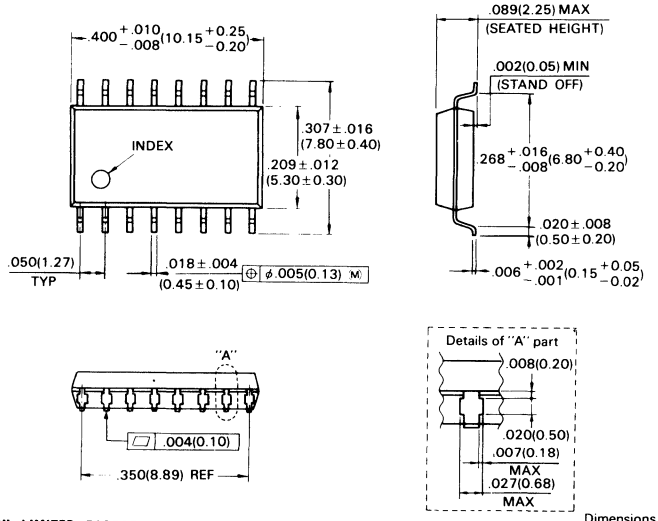
Dimensions in inches (millimeters)

7

MB88342–PF

16-LEAD PLASTIC FLAT PACKAGE

(Case No. : FPT-16P-M02)

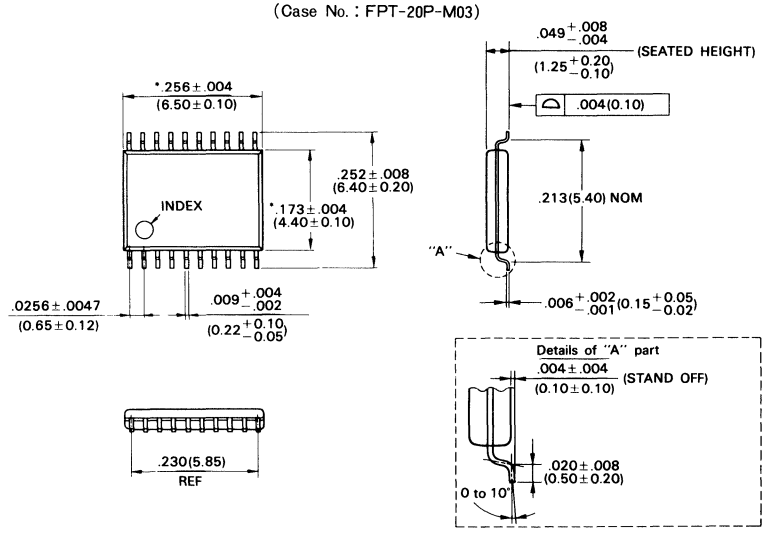


Dimensions in inches (millimeters)

7

MB88342-PFV

20-LEAD PLASTIC FLAT PACKAGE
(Case No. : FPT-20P-M03)



* : This dimension does not include resin protrusion.

Dimensions in inches (millimeters)

7

FUJITSU

10-BIT HIGH SPEED D/A CONVERTER

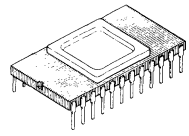
MB40748-8
MB40748-9
MB40748-10

August 1988
Edition 4.0

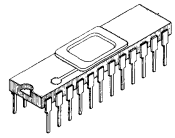
10-BIT HIGH SPEED D/A CONVERTER

The Fujitsu MB40748 is a 10 bit Ultra-high speed low-power Digital to Analog Converter which is fabricated with Fujitsu Advanced Bipolar Technology. The device can convert 10-bit digital signals into analog signals from DC to 20 Mega-samples/sec. (MSPS). Because of such high speed operation, the device is suitable for applications such as color television decoding, digital TV system and video processing with computer.

- Resolution : 10 bits
- Linearity MB40748-8 : ±0.2% max. (8 bit accuracy)
  MB40748-9 : ±0.1% max. (9 bit accuracy)
  MB40748-10 : ±0.05% max. (10 bit accuracy)
- Conversion Rate : 20 MSPS min.
- Analog Output Voltage : 0V to −1V
- Digital Input Voltage : 10k ECL level
- Input Code : Binary or 2's complement
- Single Power Supply : −5.2V
- Power Dissipation : 300mW typ.
- Package : DIP-24C-A06
  DIP-24C-A10

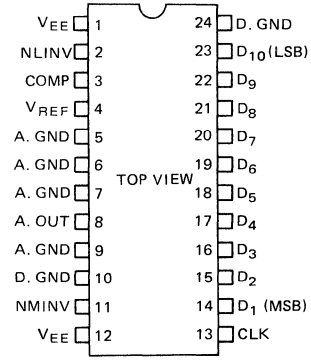


CERAMIC PACKAGE
DIP-24C-A06



CERAMIC PACKAGE
DIP-24C-A10

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS

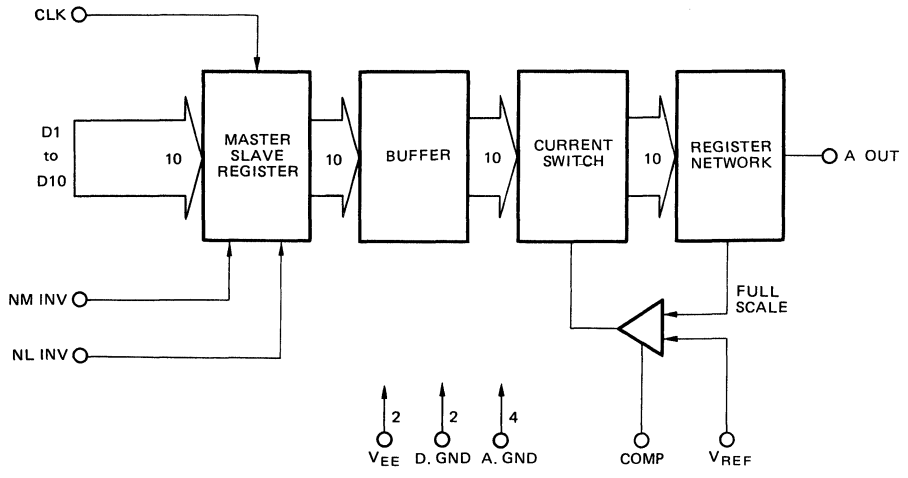
Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{EE}	+0.5 to −7.0	V
Digital Input Voltage	V_{IND}	+0.5 to V_{EE}	V
Analog Reference Voltage	V_{REF}	+0.5 to V_{EE}	V
Storage Temperature	T_{STG}	−55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

7

Fig. 1–MB40748 BLOCK DIAGRAM



7

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{EE}	-5.46	-5.20	-4.94	V
Analog Reference Voltage	V_{REF}	-1.2	-1.0	-0.8	V
Clock Pulse Width at High-level	$t_W{}^+$	15			ns
Clock Pulse Width at Low-level	$t_W{}^-$	15	—		ns
Data Setup Time	t_S	20			ns
Data Hold Time	t_H	0			ns
Operating Temperature	T_A	0		70	°C
Phase Compensation Capacitance*	C_{COMP}	1			μF

Note: The capacitor should be connected between COMP and V_{EE}

7

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.) (V_{EE} = -5.2 V, T_A = 0 V to +70 V °C)

ANALOG DC CHARACTERISTICS

Parameter	Condition & Note	Symbol	Value			Unit
			Min	Typ	Max	
Resolution					10	bits
Linearity Error	MB40748-8	LE			±0.2	%
	MB40748-9				±0.1	%
	MB40748-10				±0.05	%
Full-scale Analog Output Voltage	V_{REF} = -1.00V, A. OUT is open.	V_{OFS}	-1.06	-1.00	-0.94	V
Zero-scale Analog Output Voltage	V_{REF} = -1.00V, A. OUT is open.	V_{OZS}	-15	0	15	mV
Reference Input Current	V_{REF} = -1.00V	I_{REF}			10	μA
Output Impedance	T_A = 25°C	Z_{OUT}	70	80	90	Ω

ELECTRICAL CHARACTERISTICS (continued)

(Recommended Operating Conditions unless otherwise noted.) (V_{EE} = -5.2 V, T_A = 0 to +70°C)

DIGITAL DC CHARACTERISTICS

Parameter	Conditions	Symbol	Value			Unit
			Min	Typ	Max	
High-level Digital Input Voltage	T_A = 0°C	V_{IHD}	-1.145			V
	T_A = +25°C		-1.105			
	T_A = +70°C		-1.045			
Low-level Digital Input Voltage	T_A = 0°C	V_{ILD}			-1.490	V
	T_A = +25°C				-1.475	
	T_A = +70°C				-1.450	
High-level Digital Input Current		I_{IHD}			250	μA
Low-level Digital Input Current		I_{ILD}	0.5		200	μA
Supply Current	V_{REF} = -1.00 V	I_{EE}	-90	-56		mA

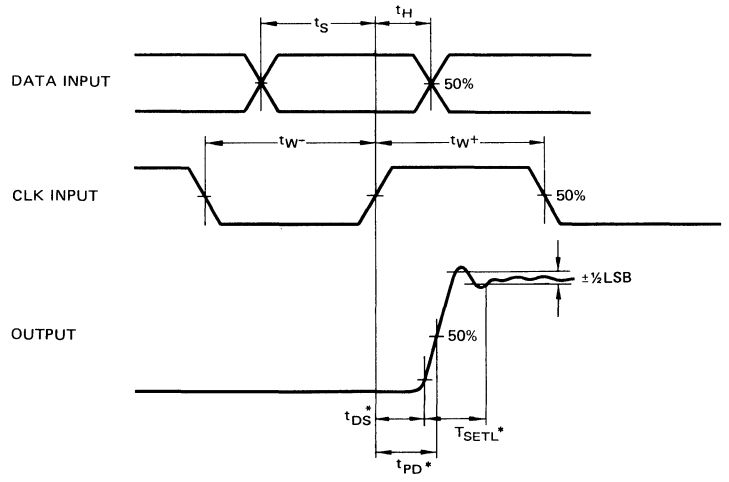
7

SWITCHING CHARACTERISTICS

(V_{EE} = -5.2 V, T_A = 0 to +70°C)

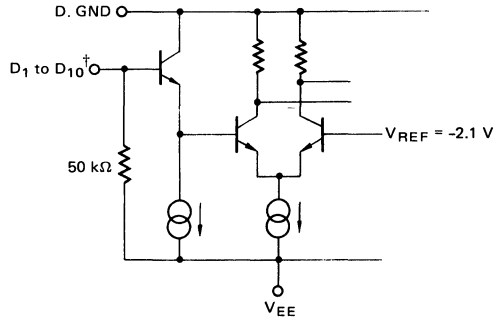
Parameter	Conditions	Symbol	Value			Unit
			Min	Typ	Max	
Maximum conversion Rate		FS	20	30		MSPS

TIMING DIAGRAM



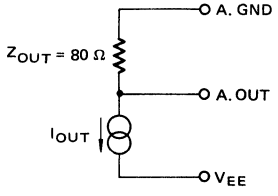
Note: *These values are not specified because they depend on application circuit.

EQUIVALENT DIGITAL INPUT CIRCUIT



Note: †V_{TH} = -1.3 V

EQUIVALENT OUTPUT CIRCUIT



7

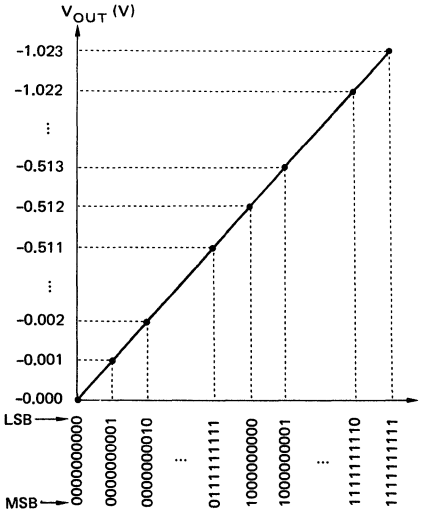
OUTPUT VOLTAGE

(Recommended Operating Conditions unless otherwise noted. V_{REF} = - 1.024 V, Positive Logic) (1 LSB = 1 mV)

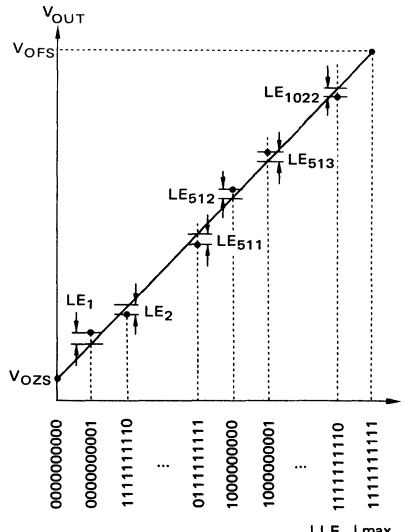
STEP	Digital Input	BINARY		OFFSET 2'S COMPLEMENT		Ideal Output Voltage (V)
		Non-inverting Input	Inverting Input	Non-inverting Input	Inverting Input	
	NMINV	1	0	0	1	
	MLINV	1	0	1	0	
0		0000000000	1111111111	1000000000	0111111111	-0.000
1		0000000001	1111111110	1000000001	0111111110	-0.001
⋮		⋮	⋮	⋮	⋮	⋮
511		0111111111	1000000000	1111111111	0000000000	-0.511
512		1000000000	0111111111	0000000000	1111111111	-0.512
513		1000000001	0111111110	0000000001	1111111110	-0.513
⋮		⋮	⋮	⋮	⋮	⋮
1022		1111111110	0000000001	0111111110	1000000001	-1.022
1023		1111111111	0000000000	0111111111	1000000000	-1.023

7

IDEAL OUTPUT OPERATION



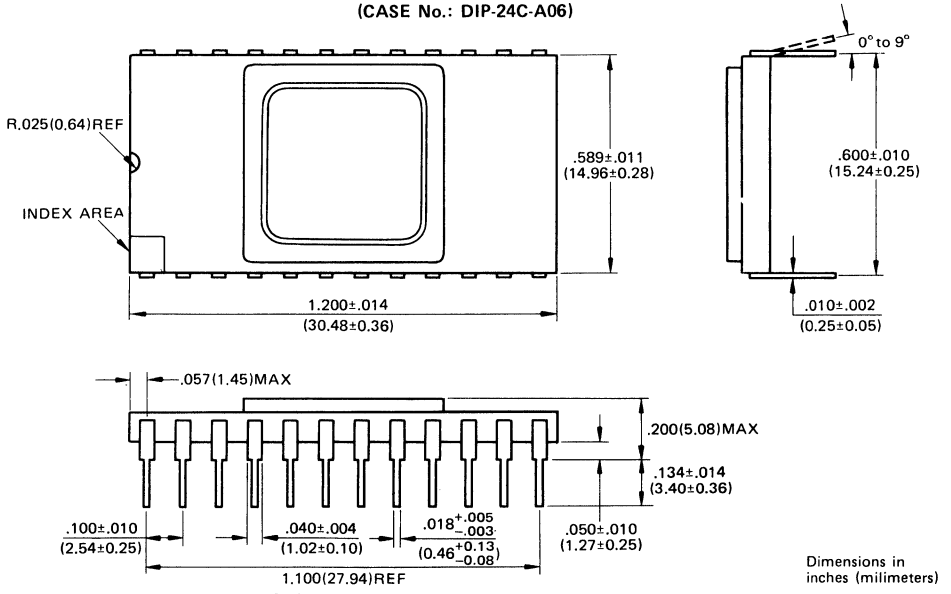
PRACTICAL OUTPUT OPERATION



$$\text{Linearity Error} = \frac{|LE_n|_{max}}{|FS|}$$

PACKAGE DIMENSIONS

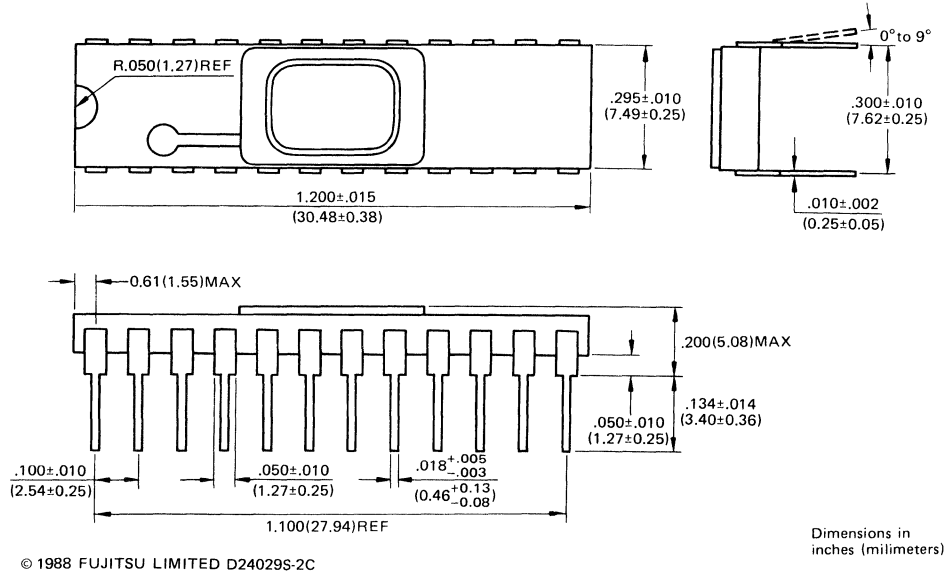
24-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-A06)



7

PACKAGE DIMENSIONS (continued)

24-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-A10)



Dimensions in
inches (milimeters)

7

FUJITSU

6-BIT HIGH SPEED D/A CONVERTER

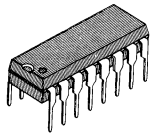
MB40776

December 1987
Edition 4.0

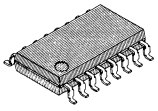
6-BIT HIGH SPEED D/A CONVERTER

The Fujitsu MB 40776 is a 6-bit low power ultra-high speed video D/A converter fabricated with Fujitsu Advanced Bipolar Technology. The MB 40776 can convert 6-bit digital signals into analog signals at a rate of DC to 20 mega-samples/sec (MSPS). Because of such high speed operation, the MB 40776 is suitable for applications such as digital color TV, video processing with computer, radar signal processing.

- Resolution : 6 bits
- Linearity : ±0.8%
- Maximum Conversion Rate : 20 MSPS min.
- Analog Output Voltage range : V_{CC} to V_{CC} -1 [V]
- Digital I/O level : TTL
- Single Power Supply : + 5 [V]
- Power Dissipation : 220 [mW] typ.
- Standard 16-pin DIP Package : (Suffix: -P)
  Standard 16-pin FPT Package : (Suffix: -PF)

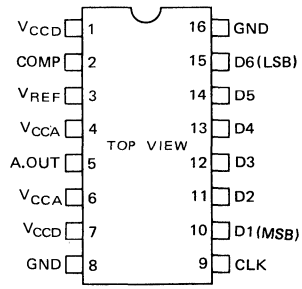


PLASTIC PACKAGE
DIP-16P-M04



PLASTIC PACKAGE
FPT-16P-M02

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

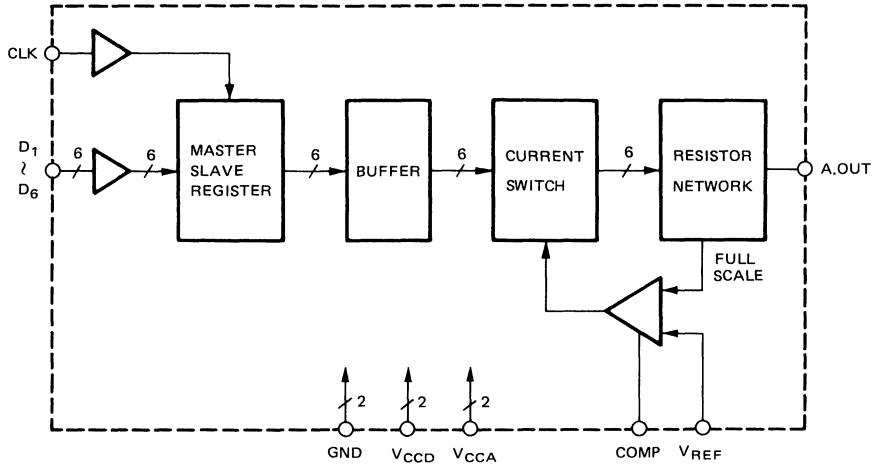
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CCA} V_{CCD}	-0.5 to +7.0	V
Digital Input Voltage	V_{IND}	-0.5 to +7.0	V
Analog Reference Voltage	V_{REF}	3.70 to V_{CC} + 0.5	V
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

7

Fig. 1– MB40776 BLOCK DIAGRAM



7

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CCA} V_{CCD}	4.75	5.00	5.25	V
Analog Reference Voltage *1	V_{REF}	3.70	4.00	4.30	V
Clock Pulse Width at High level	t_{w+}	25			ns
Clock Pulse Width at Low level	t_{w-}	25			ns
Data Setup Time	t_S	12.5			ns
Data Hold Time	t_H	12.5			ns
Operating Temperature	T_A	0		70	°C
Phase Compensation Capacitance*2	C_{COMP}	1			μF

NOTE: *1: $V_{CC} - V_{REF} \leqq 1.2$ V
*2: The capacitance should be connected between COMP and GND.

7

ELECTRICAL CHARACTERISTICS

ANALOG DC CHARACTERISTICS

(V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Resolution					6	bits
Linearity Error	LE	DC			±0.8	%
Full-Scale Analog Output Voltage	V_{OFS}	V_{CC} = 5.000 V V_{REF} = 3.976 V	V_{CCA} -0.015	V_{CCA}	V_{CCA} +0.015	V
Zero-Scale Analog Output Voltage	V_{OZS}	V_{CC} = 5.000 V V_{REF} = 3.976 V	3.932	3.992	4.052	V
Reference Input Current	I_{REF}	V_{REF} = 4.00 V			10	μA
Output Impedance	Z_{OUT}	T_A = 25°C	70	80	90	Ω

7

DIGITAL DC CHARACTERISTICS

(V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

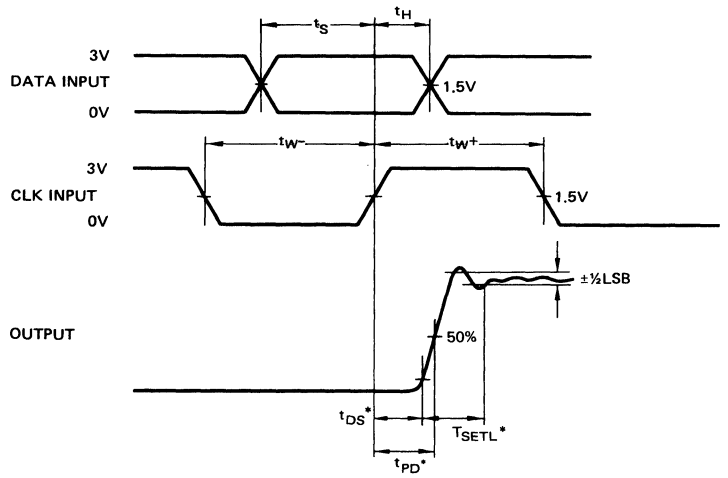
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
High-level Input Voltage	V_{IHD}		2.0			V
Low-level Input Voltage	V_{ILD}				0.8	V
Maximum Input Current	I_{ID}	V_{CC} = 5.25 V V_I = 7.00 V		0	100	μA
High-level Input Current	I_{IHD}	V_{CC} = 5.25 V V_{IHD} = 2.70 V		0	20	μA
Low-level Input Current	I_{ILD}	V_{CC} = 5.25 V V_{ILD} = 0.40 V	-400	-40		μA
Power Supply Current	I_{CC}	V_{REF} = 4.05 V		43*	65	mA

NOTE: * V_{CC} = 5.00 V, V_{REF} = 4.00 V

SWITCHING CHARACTERISTICS (V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Maximum Conversion Rate	FS		20	30	–	MSPS

TIMING DIAGRAM



Note: *These values are not specified because they depend on application circuit.

7

Fig. 2 – DIGITAL INPUT EQUIVALENT CIRCUIT

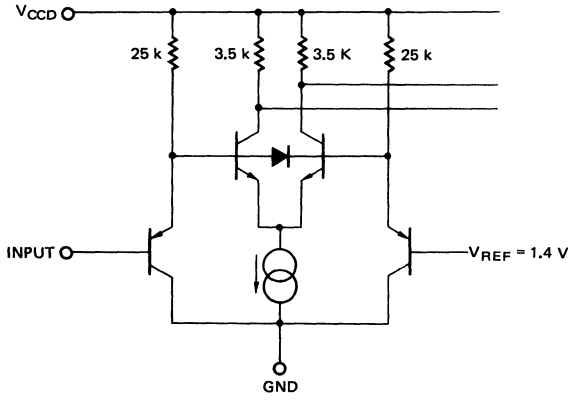
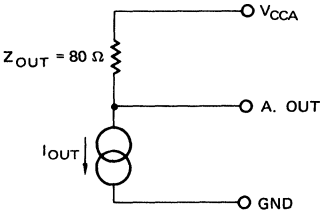


Fig. 3 – OUTPUT EQUIVALENT CIRCUIT



7

OUTPUT VOLTAGE

(V_{CCA} = 5.000 V, V_{REF} = 3.976 V)

Input Code	OUTPUT VOLTAGE (V)
000000	3.992
000001	4.008
.	.
.	.
.	.
011111	4.488
100000	4.504
100001	4.520
.	.
.	.
.	.
111110	4.984
111111	5.000

Note: 1LSB = 16 mV

Fig. 4 — IDEAL OUTPUT OPERATION

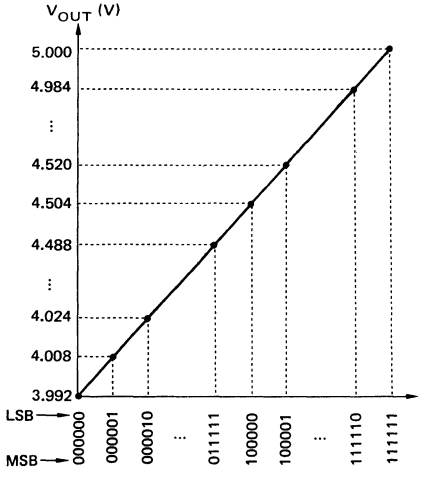
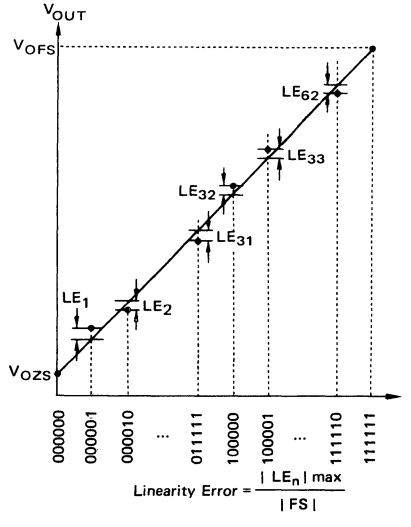


Fig. 5 — PLACTICAL OUTPUT OPERATION



7

TYPICAL CHARACTERISTICS CURVES

Fig. 6 – POWER SUPPLY CURRENT vs. TEMPERATURE

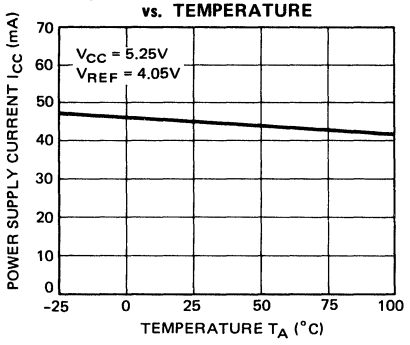


Fig. 7 – LINEARITY ERROR vs. TEMPERATURE

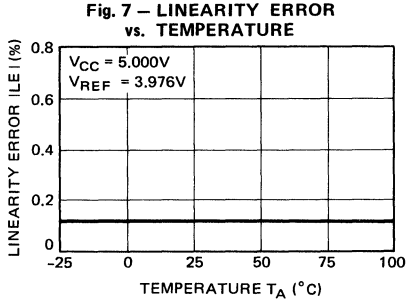


Fig. 8 – OUTPUT IMPEDANCE vs. TEMPERATURE

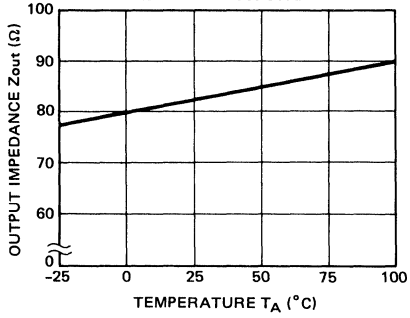


Fig. 9 – ZERO-SCALE ANALOG OUTPUT VOLTAGE vs. TEMPERATURE

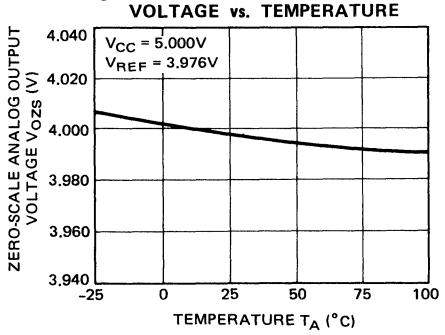


Fig. 10 – FULL-SCALE ANALOG OUTPUT VOLTAGE vs. TEMPERATURE

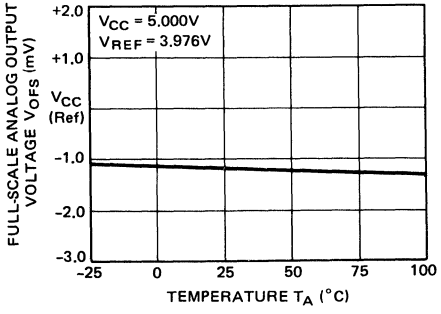


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Fig. 11 – DELAY TIME vs. TEMPERATURE

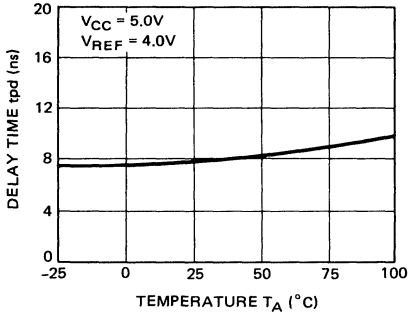


Fig. 12 – DELAY TIME vs. POWER SUPPLY VOLTAGE

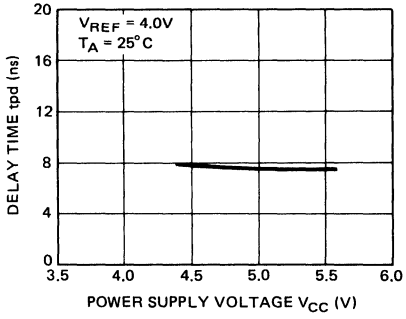


Fig. 13 – CLOCK PULSE WIDTH vs. TEMPERATURE

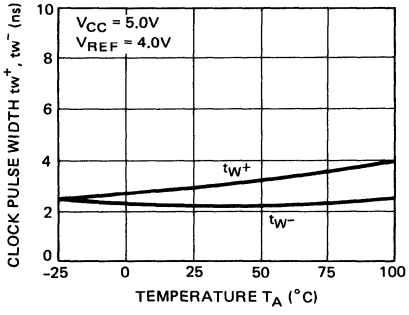


Fig. 14 – CLOCK PULSE WIDTH vs. POWER SUPPLY VOLTAGE

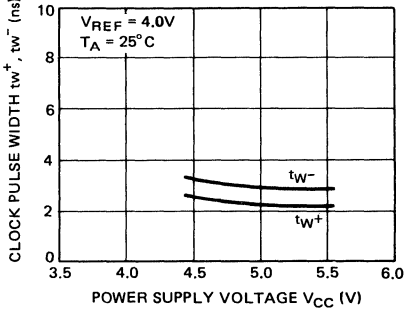
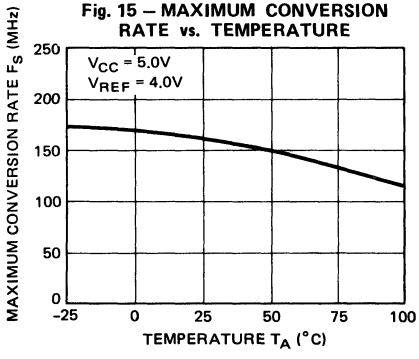


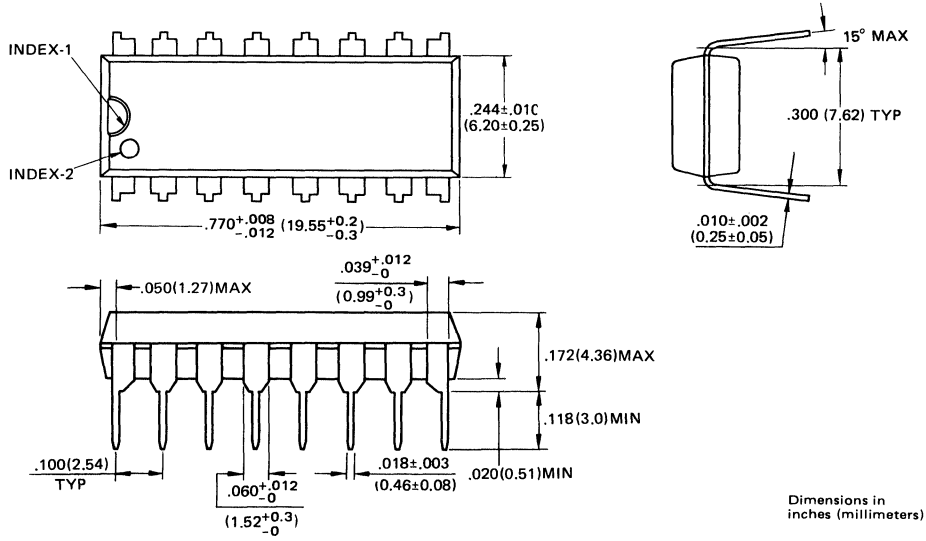
Fig. 15 – MAXIMUM CONVERSION RATE vs. TEMPERATURE



7

PACKAGE DIMENSIONS

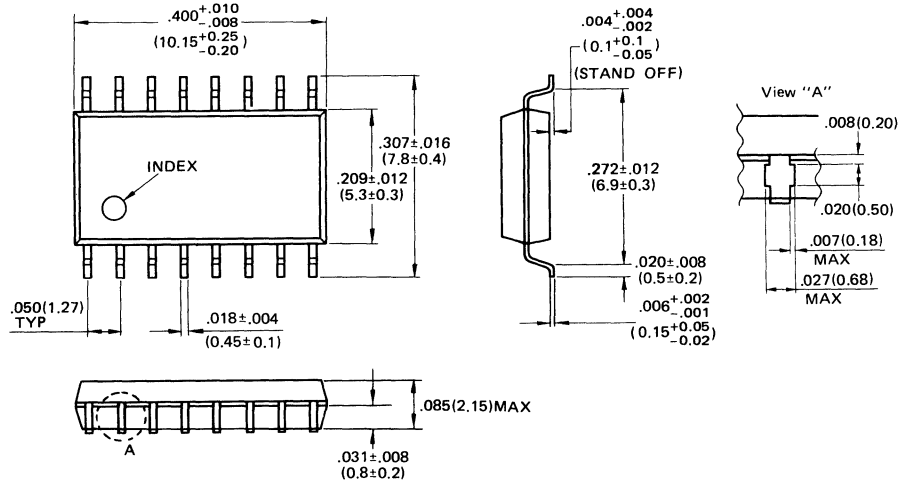
16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)



7

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M02)



Dimensions in
inches (millimeters)

7

7

FUJITSU

6-BIT HIGH SPEED D/A CONVERTER

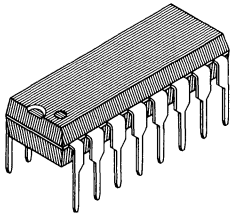
MB40776H

February 1988
Edition 1.0

6-BIT HIGH SPEED D/A CONVERTER

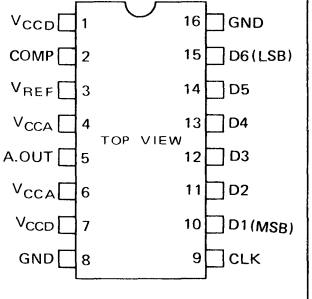
The Fujitsu MB40776H is a 6-bit low power ultra-high speed video D/A converter fabricated with Fujitsu Advanced Bipolar Technology. The MB40776H can convert 6-bit digital signals into analog signals at a rate of DC to 60 megasamples/sec (MSPS). Because of such high speed operation, the MB40776H is suitable for applications such as digital color TV, video processing with computer, radar signal processing.

- Resolution : 6 bits
- Linearity : ±0.8%
- Maximum Conversion Rate : 60 MSPS min.
- Analog Output Voltage range : V_{CC} to V_{CC} -1 [V]
- Digital I/O level : TTL
- Single Power Supply : + 5 [V]
- Power Dissipation : 220 [mW] typ.
- Standard 16-pin DIP Package : (Suffix: -P)



PLASTIC PACKAGE
DIP-16P-M04

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

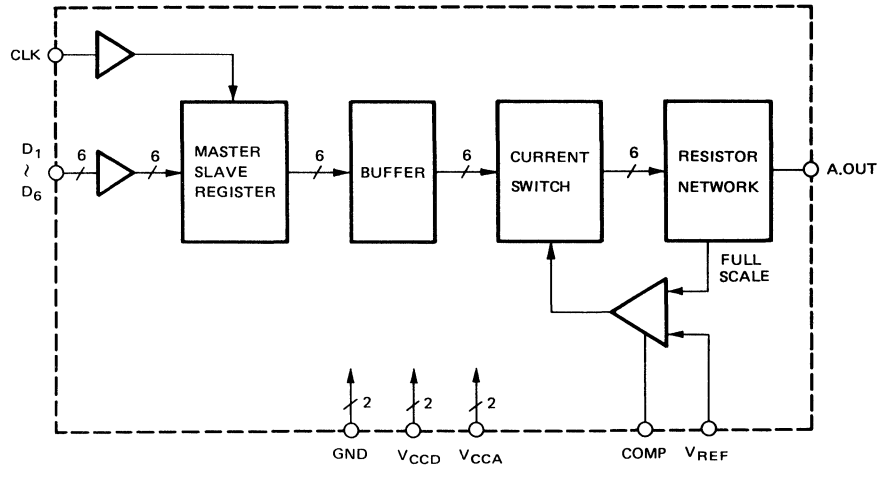
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CCA} V_{CCD}	-0.5 to +7.0	V
Digital Input Voltage	V_{IND}	-0.5 to +7.0	V
Analog Reference Voltage	V_{REF}	3.70 to V_{CC} + 0.5	V
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

7

Fig. 1 – MB40776H BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CCA} V_{CCD}	4.75	5.00	5.25	V
Analog Reference Voltage *1	V_{REF}	3.70	4.00	4.30	V
Clock Pulse Width at High level	t_{w+}	8.3			ns
Clock Pulse Width at Low level	t_{w-}	8.3			ns
Data Setup Time	t_S	10.0			ns
Data Hold Time	t_H	4.0			ns
Operating Temperature	T_A	0		70	°C
Phase Compensation Capacitance*2	C_{COMP}	1			μF

NOTE: *1: $V_{CC} - V_{REF} \leqq 1.2$ V
*2: The capacitance should be connected between COMP and GND.

7

ELECTRICAL CHARACTERISTICS

ANALOG DC CHARACTERISTICS

(V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Resolution					6	bits
Linearity Error	LE	DC			±0.8	%
Full-Scale Analog Output Voltage	V_{OFS}	V_{CC} = 5.000 V V_{REF} = 3.976 V	V_{CCA} -0.015	V_{CCA}	V_{CCA} +0.015	V
Zero-Scale Analog Output Voltage	V_{OZS}	V_{CC} = 5.000 V V_{REF} = 3.976 V	3.932	3.992	4.052	V
Reference Input Current	I_{REF}	V_{REF} = 4.00 V			10	μA
Output Impedance	Z_{OUT}	T_A = 25°C	70	80	90	Ω

7

DIGITAL DC CHARACTERISTICS

(V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

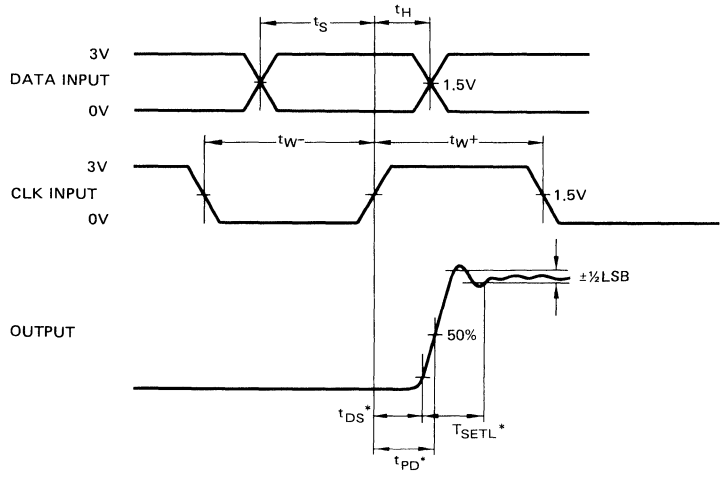
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
High-level Input Voltage	V_{IHD}		2.0			V
Low-level Input Voltage	V_{ILD}				0.8	V
Maximum Input Current	I_{ID}	V_{CC} = 5.25 V V_I = 7.00 V		0	100	μA
High-level Input Current	I_{IHD}	V_{CC} = 5.25 V V_{IHD} = 2.70 V		0	20	μA
Low-level Input Current	I_{ILD}	V_{CC} = 5.25 V V_{ILD} = 0.40 V	-400	-40		μA
Power Supply Current	I_{CC}	V_{REF} = 4.05 V		43*	65	mA

NOTE: * V_{CC} = 5.00 V, V_{REF} = 4.00 V

SWITCHING CHARACTERISTICS (V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Maximum Conversion Rate	FS		60	–	–	MSPS

TIMING DIAGRAM



Note: *These values are not specified because they depend on application circuit.

7

Fig. 2 – DIGITAL INPUT EQUIVALENT CIRCUIT

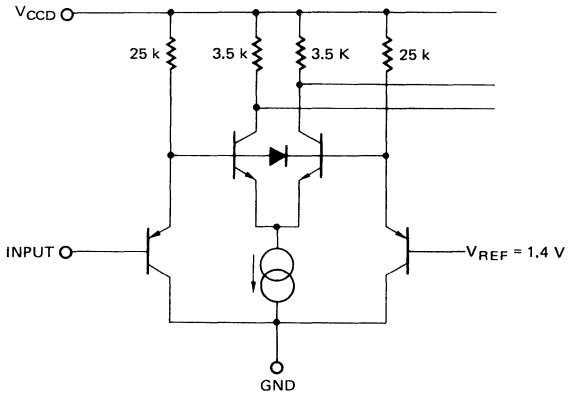
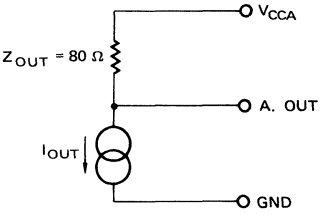


Fig. 3 – OUTPUT EQUIVALENT CIRCUIT



7

OUTPUT VOLTAGE

(V_{CCA} = 5.000 V, V_{REF} = 3.976 V)

Input Code	OUTPUT VOLTAGE (V)
000000	3.992
000001	4.008
.	.
.	.
.	.
011111	4.488
100000	4.504
100001	4.520
.	.
.	.
.	.
111110	4.984
111111	5.000

Note: 1LSB = 16 mV

Fig. 4 — IDEAL OUTPUT OPERATION

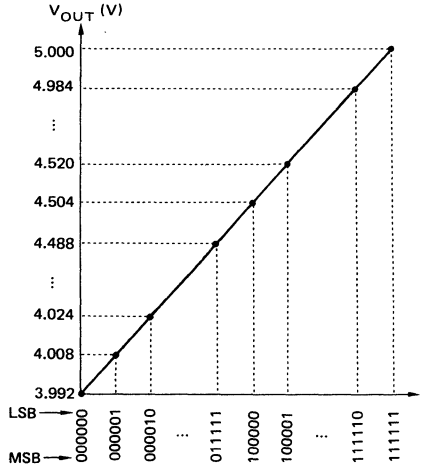
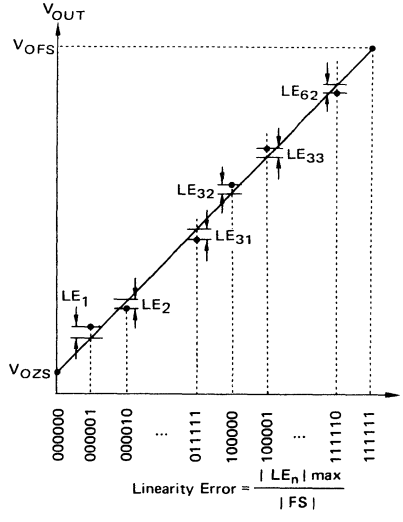


Fig. 5 — PLACTICAL OUTPUT OPERATION



7

TYPICAL CHARACTERISTICS CURVES

Fig. 6 – POWER SUPPLY CURRENT vs. TEMPERATURE

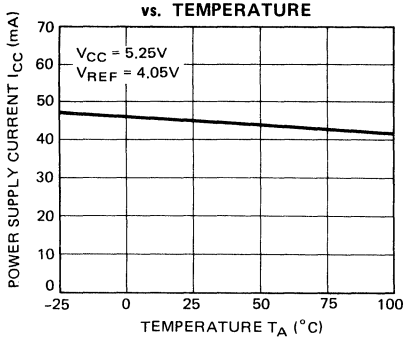


Fig. 7 – LINEARITY ERROR vs. TEMPERATURE

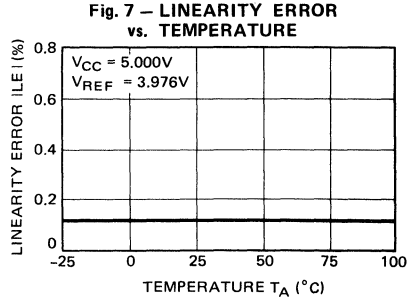


Fig. 8 – OUTPUT IMPEDANCE vs. TEMPERATURE

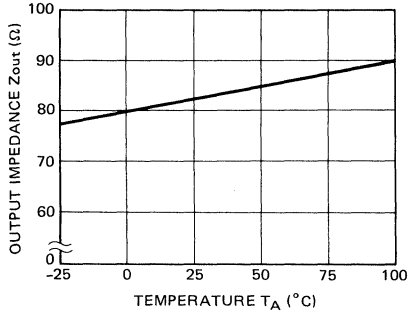


Fig. 9 – ZERO-SCALE ANALOG OUTPUT VOLTAGE vs. TEMPERATURE

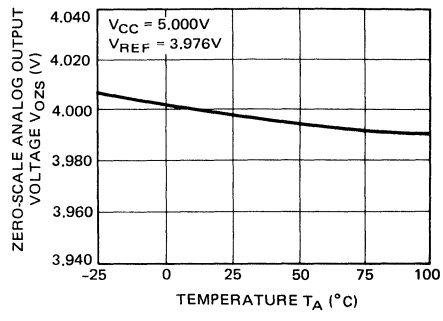
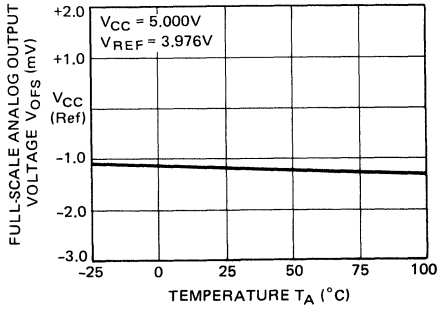


Fig. 10 – FULL-SCALE ANALOG OUTPUT VOLTAGE vs. TEMPERATURE



7

Fig. 11 – DELAY TIME vs. TEMPERATURE

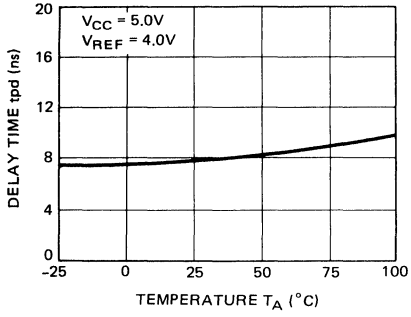


Fig. 12 – DELAY TIME vs. POWER SUPPLY VOLTAGE

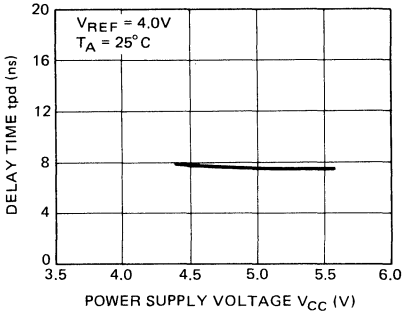


Fig. 13 – CLOCK PULSE WIDTH vs. TEMPERATURE

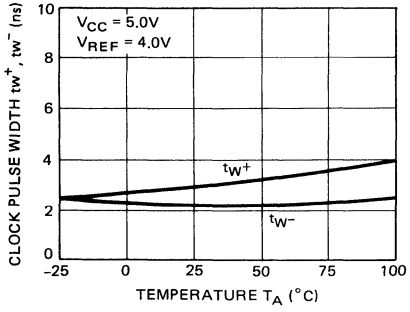


Fig. 14 – CLOCK PULSE WIDTH vs. POWER SUPPLY VOLTAGE

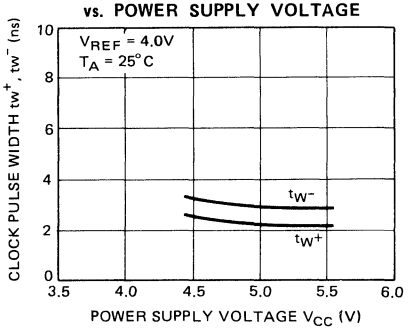
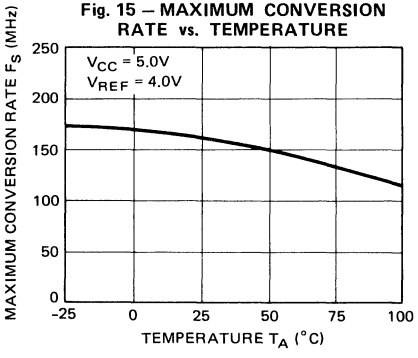


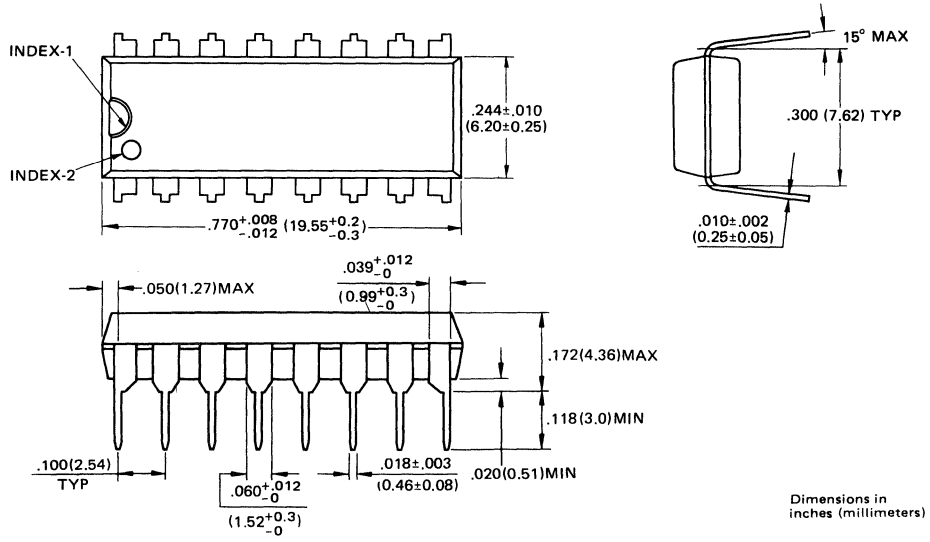
Fig. 15 – MAXIMUM CONVERSION RATE vs. TEMPERATURE



7

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-16P-M04)



7

FUJITSU

8-BIT HIGH SPEED D/A CONVERTER

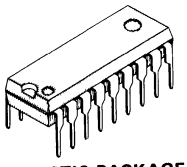
MB40778

October 1988
Edition 4.0

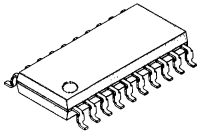
8-BIT HIGH SPEED D/A CONVERTER

The Fujitsu MB 40778 is a 8-bit low power ultra-high speed video D/A converter fabricated with Fujitsu Advanced Bipolar Technology. The MB 40778 can convert 8-bit digital signals into analog signals at a rate of DC to 20 megasamples/sec (MSPS). Because of such high speed operation, the MB 40778 is suitable for applications such as digital color TV, video processing with computer, radar signal processing.

- Resolution : 8 bits
- Linearity : ±0.2%
- Maximum Conversion Rate : 20 MSPS min.
- Analog Output Voltage range : V_{CC} to V_{CC} -1 [V]
- Digital I/O level : TTL
- Single Power Supply : +5 [V]
- Power Dissipation : 250 [mW] typ.
- Standard 18-pin DIP Package (Suffix: -P)



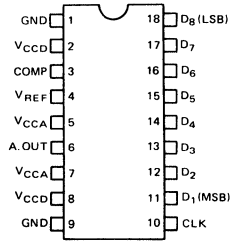
PLASTIC PACKAGE
DIP-18P-M02



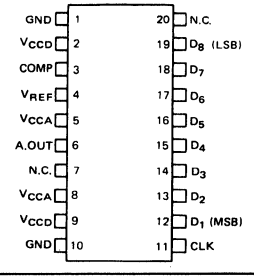
PLASTIC PACKAGE
FPT-20P-M01

PIN ASSIGNMENT

(TOP VIEW: DIP)



(TOP VIEW: FPT)



ABSOLUTE MAXIMUM RATINGS (See NOTE)

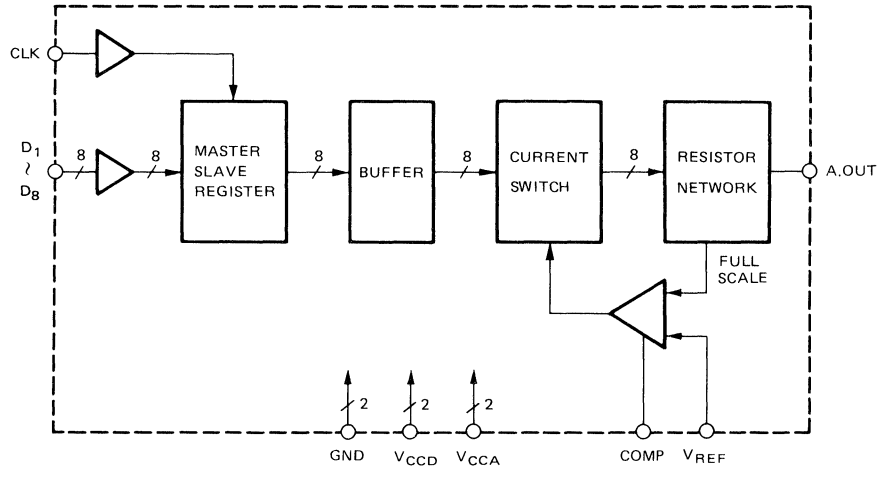
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CCA} V_{CCD}	-0.5 to +7.0	V
Digital Input Voltage	V_{IND}	-0.5 to +7.0	V
Analog Reference Voltage	V_{REF}	3.70 to V_{CC} + 0.5	V
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

7

Fig. 1– MB40778 BLOCK DIAGRAM



7

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CCA} V_{CCD}	4.75	5.00	5.25	V
Analog Reference Voltage *1	V_{REF}	3.70	4.00	4.30	V
Clock Pulse Width at High level	t_{w+}	25			ns
Clock Pulse Width at Low level	t_{w-}	25			ns
Data Setup Time	t_S	12.5			ns
Data Hold Time	t_H	12.5			ns
Operating Temperature	T_A	0		70	°C
Phase Compensation Capacitance*2	C_{COMP}	1			μF

Note: *1: $V_{CC} - V_{REF} \leqq 1.2$ V
*2: The capacitor should be connected between COMP and GND.

7

ELECTRICAL CHARACTERISTICS

ANALOG DC CHARACTERISTICS

(V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Resolution					8	bits
Linearity Error	LE	DC			±0.2	%
Full-Scale Analog Output Voltage	V_{OFS}	V_{CC} = 5.000 V V_{REF} = 3.976 V	V_{CCA} -0.015	V_{CCA}	V_{CCA} +0.015	V
Zero-Scale Analog Output Voltage	V_{OZS}	V_{CC} = 5.000 V V_{REF} = 3.976 V	3.919	3.980	4.042	V
Reference Current	I_{REF}	V_{REF} = 4.00 V			10	μA
Output Impedance	Z_{OUT}	T_A = 25°C	70	80	90	Ω

7

DIGITAL DC CHARACTERISTICS

(V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

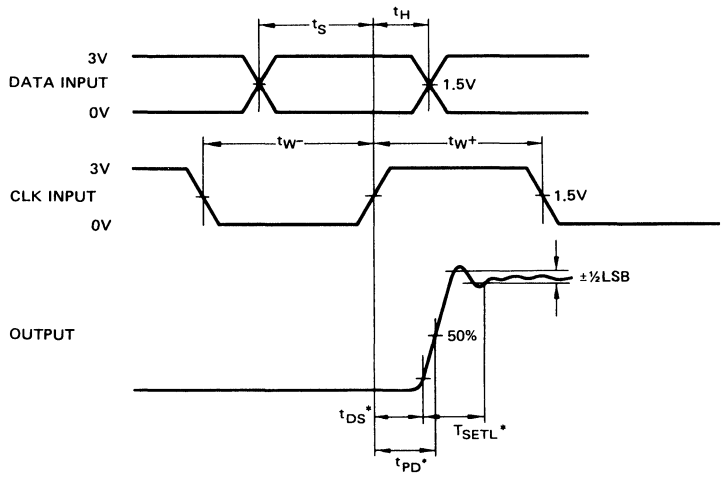
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
High-level Input Voltage	V_{IHD}		2.0			V
Low-level Input Voltage	V_{ILD}				0.8	V
Maximum Input Current	I_{ID}	V_{CC} = 5.25 V V_{ID} = 7.00 V		0	100	μA
High-level Input Current	I_{IHD}	V_{CC} = 5.25 V V_{IHD} = 2.70 V		0	20	μA
Low-level Input Current	I_{ILD}	V_{CC} = 5.25 V V_{ILD} = 0.40 V	-400	-40		μA
Power Supply Current	I_{CC}	V_{REF} = 4.05 V		50*	75	mA

Note: * V_{CC} = 5.00 V, V_{REF} = 4.00 V

SWITCHING CHARACTERISTICS (V_{CC} = 4.75 to 5.25 V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Maximum Conversion Rate	FS		20	30	–	MSPS

TIMING DIAGRAM



Note: *These values are not specified because they depend on application circuit.

7

Fig. 2 – DIGITAL INPUT EQUIVALENT CIRCUIT

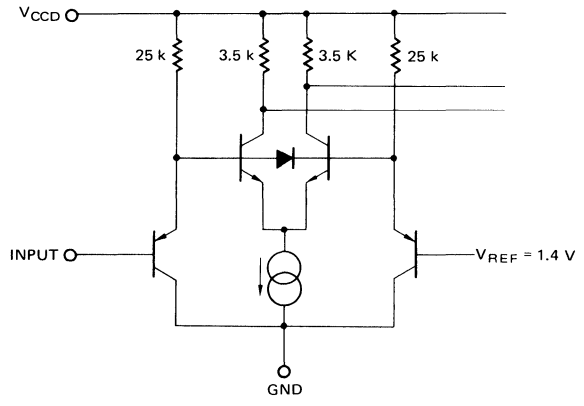
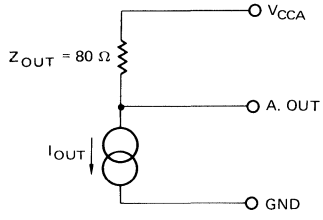


Fig. 3 – OUTPUT EQUIVALENT CIRCUIT



7

OUTPUT VOLTAGE

(V_{CCA} = 5.000 V, V_{REF} = 3.976 V)

Input Code	OUTPUT VOLTAGE (V)
00000000	3.980
00000001	3.984
.	.
.	.
.	.
01111111	4.488
10000000	4.492
10000001	4.496
.	.
.	.
.	.
11111110	4.996
11111111	5.000

Note: 1LSB = 4 mV

Fig. 4 – IDEAL OUTPUT OPERATION

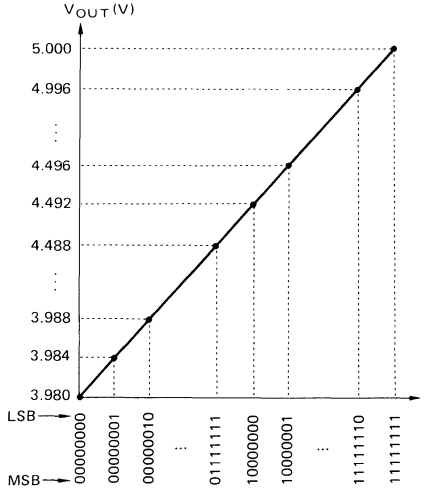
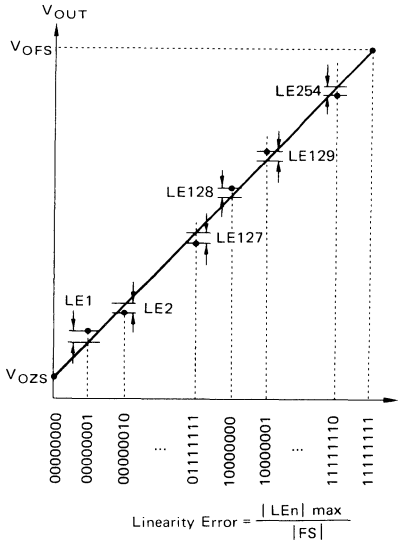


Fig. 5 – PRACTICAL OUTPUT OPERATION



7

TYPICAL CHARACTERISTICS CURVES

Fig. 6 – POWER SUPPLY CURRENT vs. TEMPERATURE

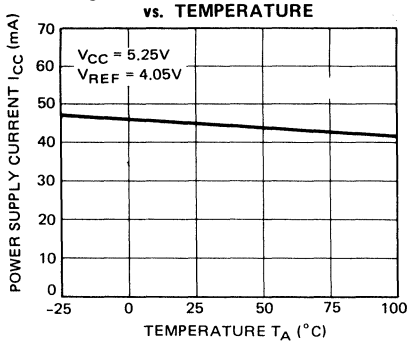


Fig. 7 – LINEARITY ERROR vs. TEMPERATURE

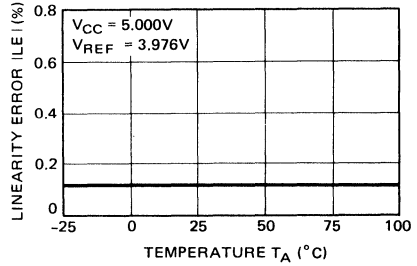


Fig. 8 – OUTPUT IMPEDANCE vs. TEMPERATURE

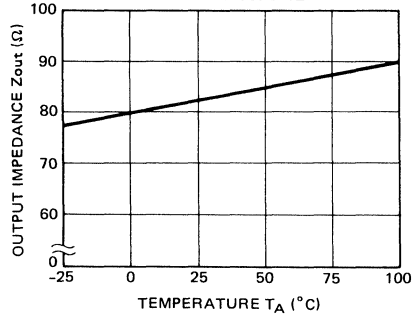


Fig. 9 – ZERO-SCALE ANALOG OUTPUT VOLTAGE vs. TEMPERATURE

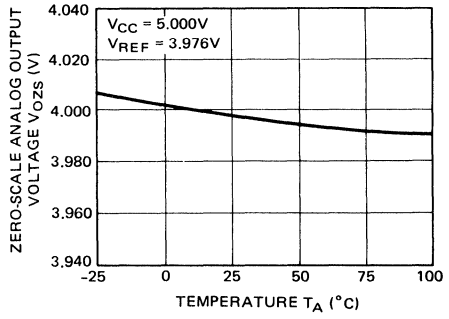
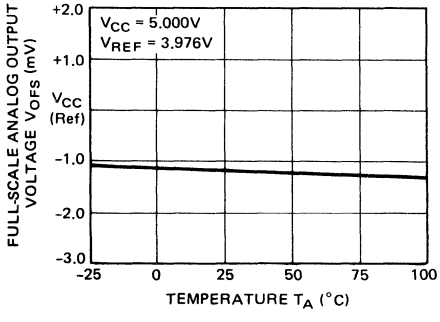


Fig. 10 – FULL-SCALE ANALOG OUTPUT VOLTAGE vs. TEMPERATURE



7

Fig. 11 – DELAY TIME vs. TEMPERATURE

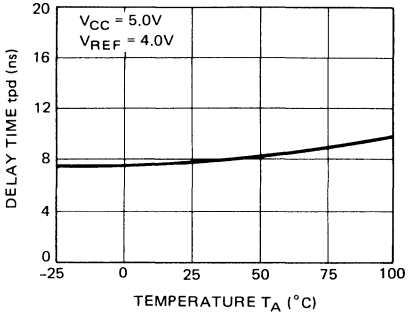


Fig. 12 – DELAY TIME vs. POWER SUPPLY VOLTAGE

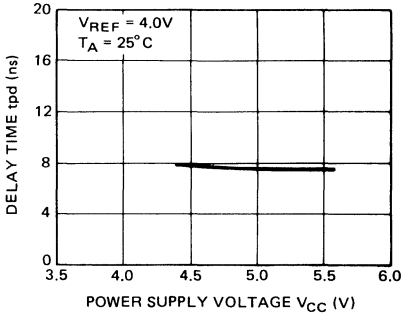


Fig. 13 – CLOCK PULSE WIDTH vs. TEMPERATURE

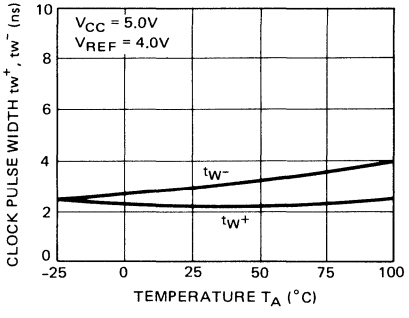


Fig. 14 – CLOCK PULSE WIDTH vs. POWER SUPPLY VOLTAGE

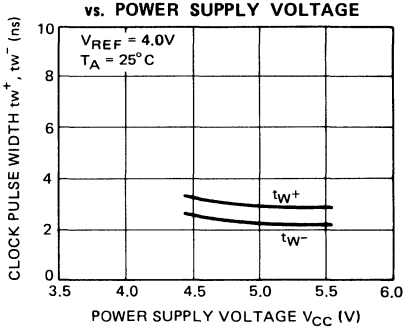
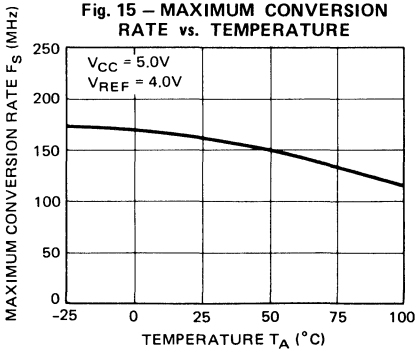


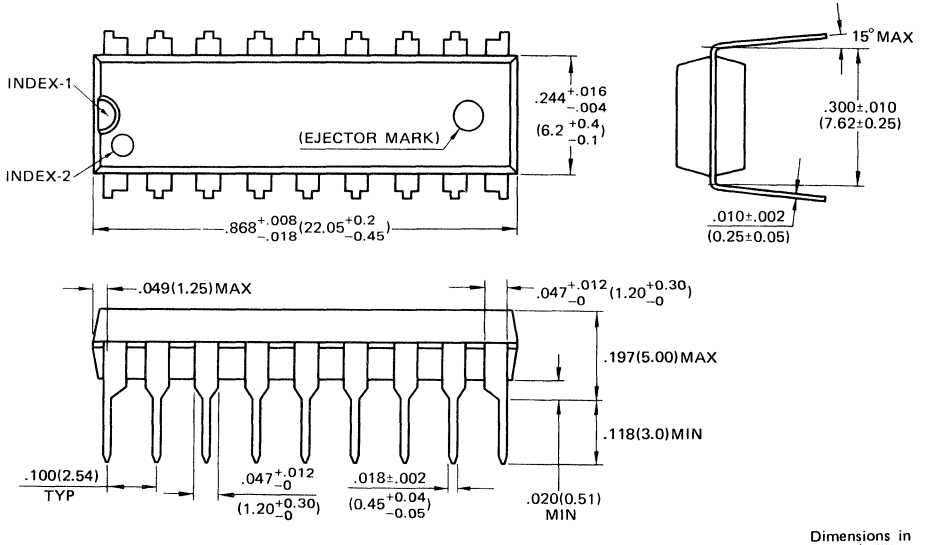
Fig. 15 – MAXIMUM CONVERSION RATE vs. TEMPERATURE



7

PACKAGE DIMENSIONS

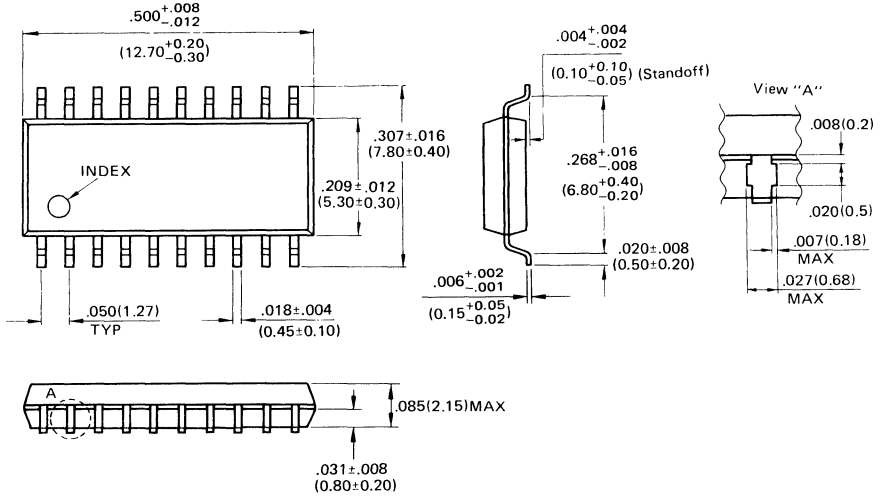
18-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-18P-M02)



Dimensions in inches (millimeters)

7

20-LEAD PLASTIC FLAT PACKAGE
(CASE No. : FPT-20P-M01)



Dimensions in inches
(millimeters)

7

7

FUJITSU

10-BIT ULTRA-HIGH SPEED D/A CONVERTER

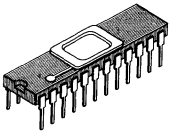
MB40788

August 1988
Edition 5.0

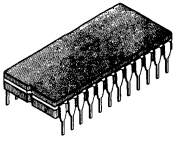
10-BIT ULTRA-HIGH SPEED D/A CONVERTER

The Fujitsu MB 40788 is 10 bit Ultra-high speed low-power Digital to Analog Converter which is fabricated with Fujitsu Advanced Bipolar Technology. The device can convert 10-bit digital signal into analog signal at a rate of DC to 125 Mega-samples/sec. (MSPS). Because of such high speed operation, the device is suitable for applications such as color television decoding system, video processing system with computer, and so on.

- Resolution : 10 bits
- Linearity : ±0.2% max.
- Conversion Rate : 125 MSPS min.
- Analog Output Voltage : 0 V to -1 V
- Digital Input Voltage : 10 k ECL level
- Input Code : Binary or 2's complement
- Single Power Supply (-5.2 V) : -5.2V
- Power Dissipation : 450mW typ.
- Standard 24-pin Dual-in-line Package



CERAMIC PACKAGE
DIP-24C-A10



CERAMIC PACKAGE
DIP-24C-C01

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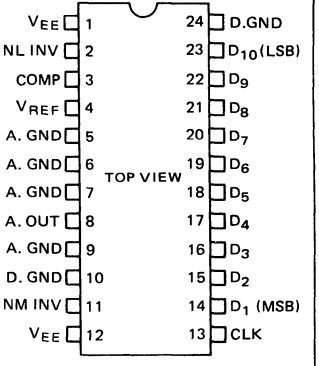
PIN ASSIGNMENT



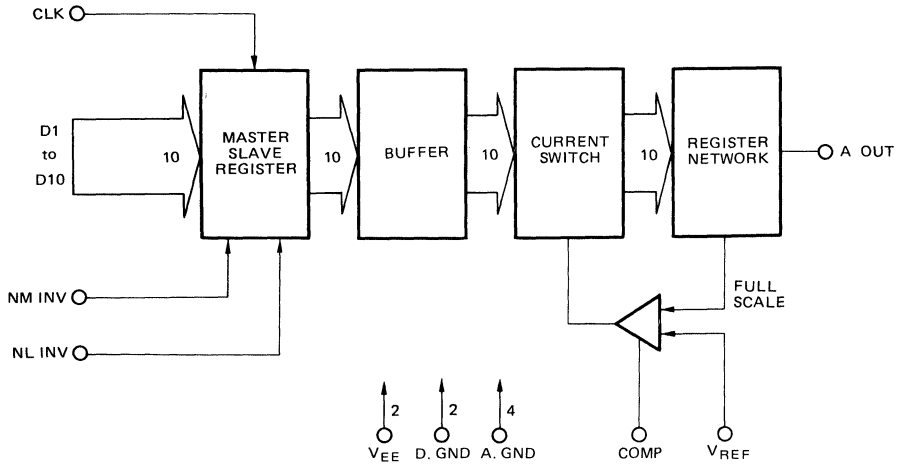
ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{EE}	+0.5 to -7.0	V
Digital Input Voltage	V_{IND}	+0.5 to V_{EE}	V
Analog Reference Voltage	V_{REF}	+0.5 to V_{EE}	V
Storage Temperature	T_{STG}	-55 to +150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB40788 BLOCK DIAGRAM



7

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{EE}	-5.46	-5.20	-4.94	V
Analog Reference Voltage	V_{REF}	-1.2	-1.0	-0.8	V
Clock Pulse Width (High-level)	$t_W{}^+$	3.0	–	–	ns
Clock Pulse Width (Low-level)	$t_W{}^-$	3.5	–	–	ns
Data Setup Time	t_S	3.0	–	–	ns
Data Hold Time	t_H	2.4	–	–	ns
Operating Temperature	t_A	0	–	70	°C
Phase Compensation Capacitance*1	C_{COMP}	1	–	–	μF

*1: The capacitor should be connected between COMP and V_{EE}

7

ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.) (V_{EE} = -5.2 V, T_A = 0 V to +70 V °C)

Parameter	Condition & Note	Symbol	Value			Unit
			Min.	Typ.	Max.	
Resolution		–	–	–	10	bits
Linearity Error	DC	L_E	–	–	±0.2	%
Full-scale Analog Output Voltage	V_{REF} = -1.00 V Output is open.	V_{OFS}	-1.06	-1.00	-0.94	V
Zero-scale Analog Output Voltage	V_{REF} = -1.00 V Output is open.	V_{OZS}	-15	0	15	mV
Reference Input Current	V_{REF} = -1.00 V	I_{REF}	–	–	20	μA
Output Impedance	T_A = 25°C	Z_{OUT}	70	80	90	Ω

ELECTRICAL CHARACTERISTICS (continued)

(Recommended Operating Conditions unless otherwise noted.) (V_{EE} = -5.2 V, T_A = 0 to +70°C)

Parameter	Conditions	Symbol	Value			Unit
			Min.	Typ.	Max.	
High-level Digital Input Voltage	T_A = 0°C T_A = +25°C T_A = +70°C	V_{IHD}	-1.145 -1.105 -1.045			V
Low-level Digital Input Voltage	T_A = 0°C T_A = +25°C T_A = +70°C	V_{ILD}			-1.490 -1.475 -1.450	V
High-level Digital Input Current		I_{IHD}		150	500	μA
Low-level Digital Input Current		I_{ILD}	0.5	115		μA
Supply Current	V_{REF} = -1.00 V	I_{EE}	-135	-84		mA

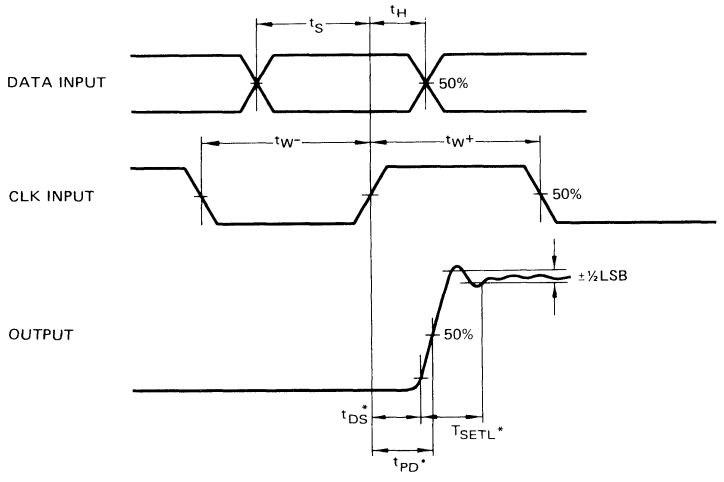
7

SWITCHING CHARACTERISTICS

(V_{EE} = -5.2 V, T_A = 0 to +70°C)

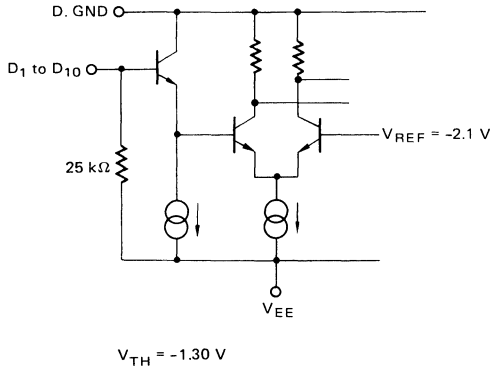
Parameter	Conditions	Symbol	Value			Unit
			Min.	Typ.	Max.	
Maximum Conversion Rate		FS	125			MSPS
Propagation delay time		t_{pd}	4.5	6.5	8.5	ns

TIMING CHART



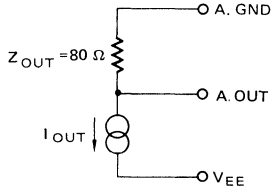
Note: *These values are not specified because they depend on application circuit.

EQUIVALENT DIGITAL INPUT CIRCUIT



V_{TH} = -1.30 V

EQUIVALENT OUTPUT CIRCUIT



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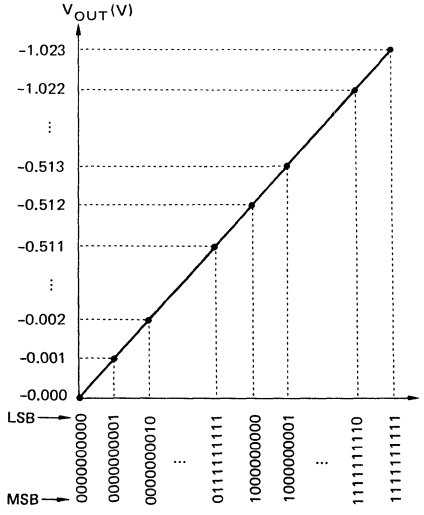
OUTPUT VOLTAGE

(Recommended Operating Conditions unless otherwise noted. V_{REF} = - 1.024 V) (1 LSB = 1 mV)

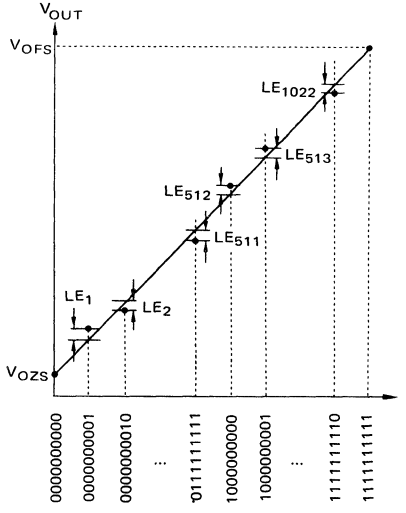
Step	Logic	Binary		Offset 2's complement		Output Voltage (V)
		Positive	Negative	Positive	Negative	
	NMINV	1	0	0	1	
	MLINV	1	0	1	0	
0		0000000000	1111111111	1000000000	0111111111	-0.000
1		0000000001	1111111110	1000000001	0111111110	-0.001
⋮		⋮	⋮	⋮	⋮	⋮
511		0111111111	1000000000	1111111111	0000000000	-0.511
512		1000000000	0111111111	0000000000	1111111111	-0.512
513		1000000001	0111111110	0000000001	1111111110	-0.513
⋮		⋮	⋮	⋮	⋮	⋮
1022		1111111110	0000000001	0111111110	1000000001	-1.022
1023		1111111111	0000000000	0111111111	1000000000	-1.023

7

IDEAL OUTPUT OPERATION



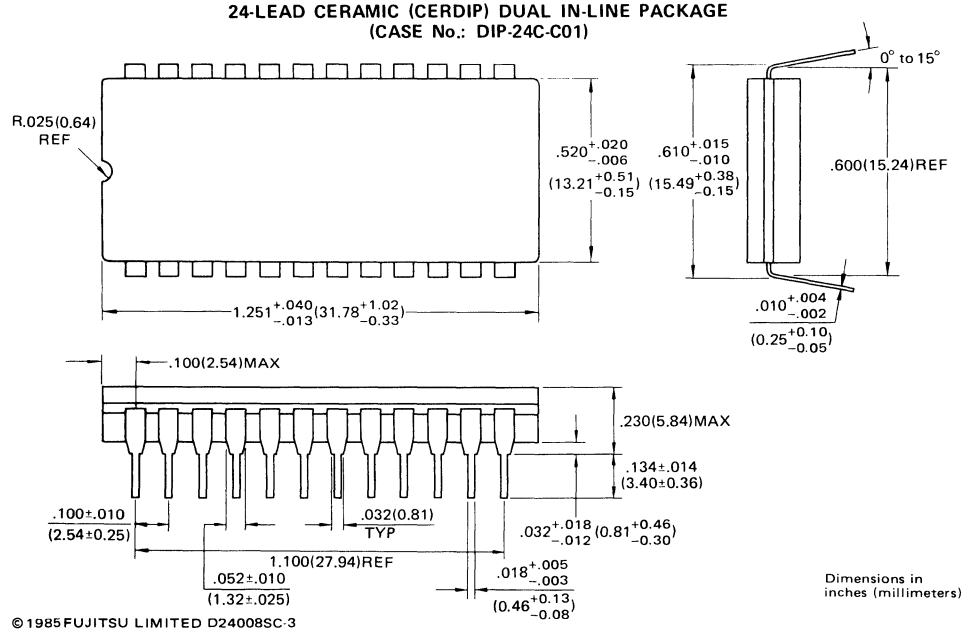
PRACTICAL OUTPUT OPERATION



$$\text{Linearity Error} = \frac{|LE_n|_{max}}{|FS|}$$

PACKAGE DIMENSIONS

24-LEAD CERAMIC (CERDIP) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-C01)



Dimensions in inches (millimeters)

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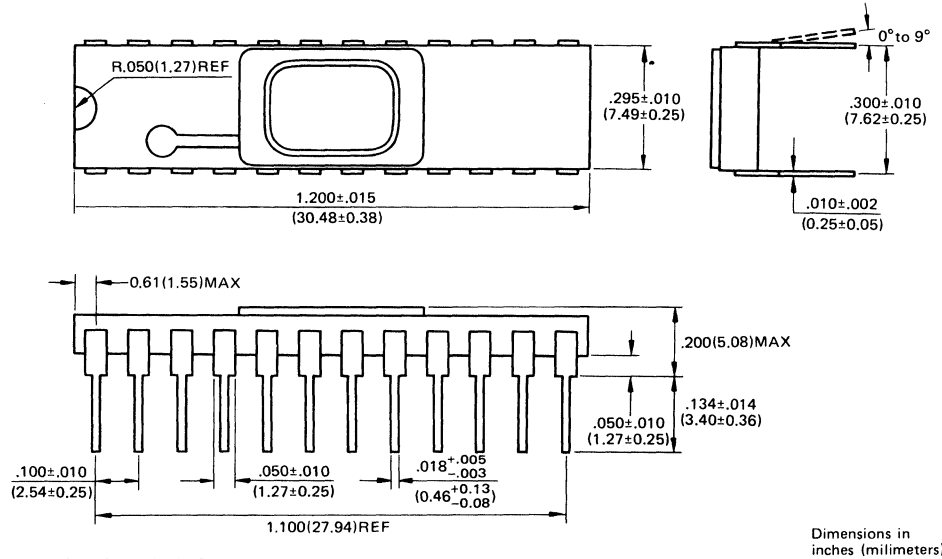
PACKAGE DIMENSIONS (continued)

24-LEAD CERAMIC (METAL SEAL) DUAL IN-LINE PACKAGE
(CASE No.: DIP-24C-A10)



Dimensions in
inches (milimeters)

7

FUJITSU

4-BIT DIGITAL-TO-ANALOG CONVERTER WITH LOOK-UP TABLE

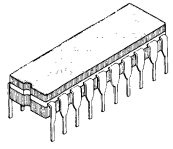
MB40874

Apr. 1989
Edition 1.0

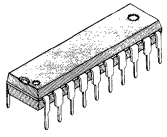
MB40874 4-BIT DIGITAL-TO-ANALOG CONVERTER WITH LOOK-UP TABLE

The Fujitsu MB40874 is 50 MSPS (Mega Sample Per Second) 4-bit Digital-to-Analog Converter with Look-up Table. The MB40874 is designed for high-speed video application with video RAM. Look-Up Table (LUT) is 16-word 4-bit memory to store luminance data. Instead of changing video RAM data, LUT data updating makes quick luminance change in monochrome video application, and quick color change in color video application.

- Resolution : 4 Bit
- Linearity : ±1/2LSB
- Operation Frequency : 50 MHz min.
- Analog Output Voltage : 4.0V to 5.0V
- Digital Input : TTL Compatible
- Power Supply Voltage: +5V
- Power Dissipation : 430mW typ.
- 20-pin Ceramic DIP (Suffix: -Z)
  20-pin Plastic DIP (Suffix: -P)

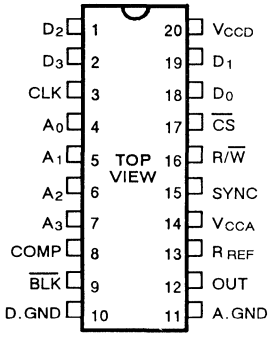


CERAMIC PACKAGE
DIP-20C-C01



PLASTIC PACKAGE
DIP-20P-M02

PIN ASSIGNMENT



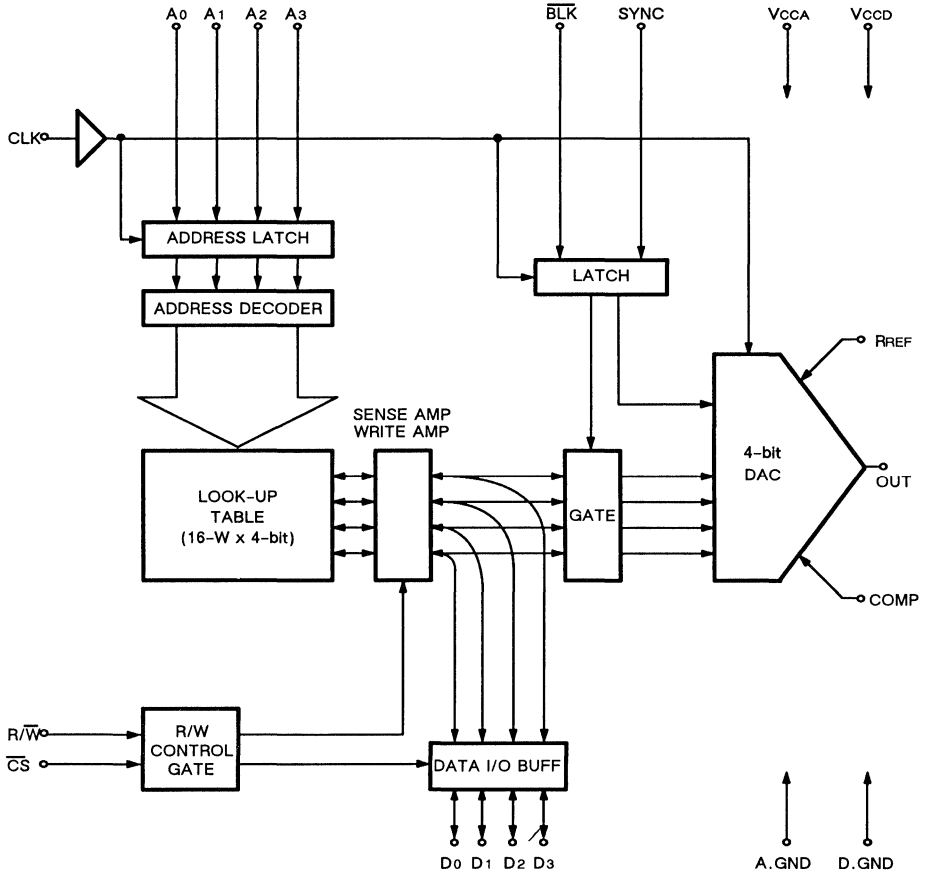
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating		Symbol	Value	Unit
Power supply voltage		V_{CCA}, V_{CCD}	-0.5 to +7.0	V
Digital input voltage		V_I	-0.5 to +7.0	V
Digital output voltage		V_{OZ}	+5.5	V
Storage Temperature	Plastic	T_{STG}	-55 to +125	°C
	Ceramic		-65 to +150	

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 - MB40874 BLOCK DIAGRAM



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PIN DESCRIPTION

Pin No.	Pin Name	Description
1,2,18,19	D0 to D3	Data Input/Output to read/write LUT data
3	CLK	Clock Input for Digital-to-Analog Operation; Operation Speed is dependent on this input. At the rising edge of this input, A0 to A3, $\overline{BLK}$, and SYNC are latched, and converted signal outputs at OUT.
4 to 7	A0 to A3	Address Input for LUT; During displaying time, dot data from VRAM is input. During display's flying line period, address is input in order to write or read the data of LUT.
8	COMP	Terminal for phase compensation capacitance; Capacitance of 1 μF or more should be inserted between COMP and A.GND.
9	$\overline{BLK}$	Input to make OUT at blank level; When $\overline{BLK}$ is at low level, OUT is at blank level. When $\overline{BLK}$ is at high level, content of LUT is converted and outputs at OUT.
10	A.GND	Ground for Analog circuit
11	D.GND	Ground for Digital circuit
12	OUT	Output of Digital-to-Analog converter; Load resistance should be inserted between OUT and V_{CCA}.
13	R_{REF}	Terminal for Reference Resistance; Reference resistor should be inserted between R_{REF} and V_{CCA}.
15	SYN	CInput for exclusive-ORed Vertical/Horizontal synchronous signal; This input is used to obtain composite output. SYNC input should be input while $\overline{BLK}$ is at low level.
16	R/$\overline{W}$	Mode Switch for Read/Write of LUT This input is effective when $\overline{CS}$ is at low level. When R/$\overline{W}$ is at high level, read mode is selected. R/$\overline{W}$ is at low level, write mode is selected.
17	$\overline{CS}$	Chip Select for LUT read/write mode
18	V_{CCA}	Power Supply pin for analog circuit
20	V_{CCD}	Power Supply pin for digital circuit

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage	V_{CCA}, V_{CCD}	4.75	5.00	5.25	V
Output high current	I_{OH}			-400	μA
Output low current	I_{OL}			8	mA
CLK frequency	f_{CLK}			50	MHZ
Phase compensation capacitance	C_{COMP}	1			μF
Operating temperature	T_A	0		70	°C

ELECTRICAL CHARACTERISTICS

ANALOG DC CHARACTERISTICS

(V_{CC} = +5.0V±5%, T_A = 0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Resolution					4	bits
Linear deviation	LE				±1/2	LSB
WHITE level output voltage	V_W		V_{CCA}-15	V_{CCA}	V_{CCA}+15	mV
BLACK level output voltage	V_B	V_{CCA}=5.000V		4.357		V
BLANK level output voltage	V_{BLANK}	R_{REF}=300Ω		4.286		V
SYNC level output voltage	V_{SYNC}	Output is		4.000		V
DAC output voltage	ΔV_{DAC}	pulled up	0.9	1.0	1.1	V
SYNC output voltage	ΔV_{SYNC}	to V_{CCA} at	236	286	336	mV
BLANK output voltage	ΔV_{BLANK}	37.5Ω	5	10(71mv)	15	IRE*
GRAY output voltage	ΔV_{GRAY}		85	90(643mV)	95	IRE*

Note: * IRE
The ratio of a reflection signal composition (V_{BLANK} to V_W) and a syncronous signal composition (V_{SYNC} to V_{BLANK}) is a 100:40 on EIA RS343A standard. 1/140 of the sum (Reflection signal composition and synchronous signal composition) is named 1IRE which is used as unit of a reflection signal.

ELECTRICAL CHARACTERISTICS (Continued)

DIGITAL DC CHARACTERISTICS

(V_{CC} = +5.0V±5%, T_A = 0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Condition		Value			Unit
				Min	Typ	Max	
Input high voltage	V_{IH}			2.0			V
Input low voltage	V_{IL}					0.8	V
Input cramp voltage	V_{IC}	V_{CC}=4.75V,	I_I=-18mA			-1.5	V
Input high current	I_{IH}	V_{CC}=5.25V	V_I=7V			100	µA
			V_I=2.7V			20	µA
Input low current	I_{IL}	V_{CC}=5.25V	V_I=0.4V			-0.4	mA
Output high voltage	V_{OH}	V_{CC}=4.75V,	I_{OH}=-400µA	2.7	3.4		V
Output low voltage	V_{OL}	V_{CC}=4.75V	I_{OL}=4mA		0.25	0.4	V
			I_{OL}=8mA		0.35	0.5	V
Output leakage current	I_{OS}	V_{CC}=5.25V		-20		-100	mA
Output current	I_{OZ}	V_{CC}=5.25V	V_O=2.4V			20	µA
Off condition (HI-Z)			V_O=0.4V			-20	µA
Power supply current	I_{CC}	V_{CC}=5.25V				120	mA

SWITCHING CHARACTERISTICS

Video Output

(V_{CC} = +5.0V±5%, T_A = 0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
CLK cycle time	t_{CLK}	20			ns
CLK high pulse width	t_{WCLK+}	7			ns
CLK low pulse width	t_{WCLK-}	7			ns
Address, $\overline{BLK}$, SYNC high pulse width	t_{WV+}	18			ns
Address, $\overline{BLK}$, SYNC low pulse width	t_{WV-}	18			ns
Address, $\overline{BLK}$, SYNC setup time	t_{SV}	6			ns
Address, $\overline{BLK}$, SYNC hold time	t_{HV}	3			ns
Propagation time	t_{PD}			25	ns

7

ELECTRICAL CHARACTERISTICS (Continued)

SWITCHING CHARACTERISTICS (Continued)

LUT Access (Read)

(V_{CC} = +5.0V±5%, T_A = 0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
$\overline{CS}$ pulse width low level time	t_{WCSR}	100			ns
R/$\overline{W}$ setup time	t_{SRWR}	10			ns
R/$\overline{W}$ hold time	t_{HRWR}	10			ns
$\overline{BLK}$ setup time	t_{SBR}	2xt_{CLK}+6			ns
$\overline{BLK}$ hold time	t_{HBR}	t_{CLK}+3			ns
Address setup time	t_{SAR}	2xt_{CLK}+6			ns
Address hold time	t_{HAR}	t_{CLK}+3			ns
Data setup time	t_{DEN}			50	ns
Data hold time	t_{DDIS}	15		50	ns

LUT Access (Write)

(V_{CC} = +5.0V±5%, T_A = 0°C to +70°C, unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
$\overline{CS}$ pulse width low level time	t_{WCSW}	100			ns
R/$\overline{W}$ setup time	t_{SRWW}	10			ns
R/$\overline{W}$ hold time	t_{HRWW}	10			ns
$\overline{BLK}$ setup time	t_{SBW}	2xt_{CLK}+6			ns
$\overline{BLK}$ hold time	t_{HBW}	t_{CLK}+3			ns
Address setup time	t_{SAW}	2xt_{CLK}+6			ns
Address hold time	t_{HAW}	t_{CLK}+3			ns
Data setup time	t_{SD}	10			ns
Data hold time	t_{HD}	10			ns

Fig. 2 — VIDEO OUTPUT TIMING DIAGRAM

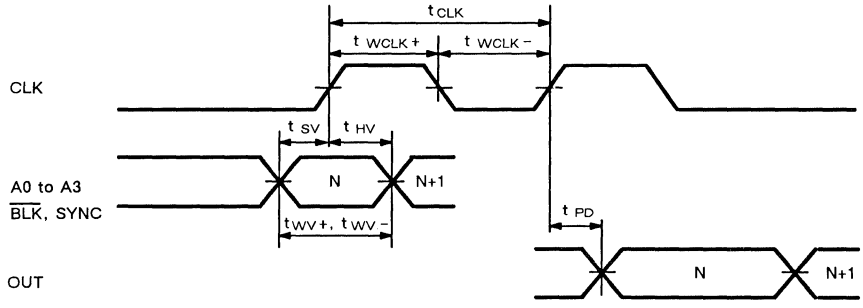

Fig. 3 — LUT ACCESS (READ) TIMING DIAGRAM

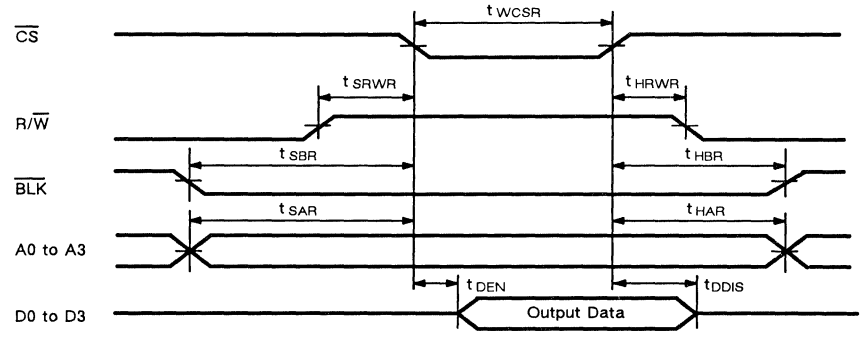

Fig. 4 — LUT ACCESS (WRITE) TIMING DIAGRAM

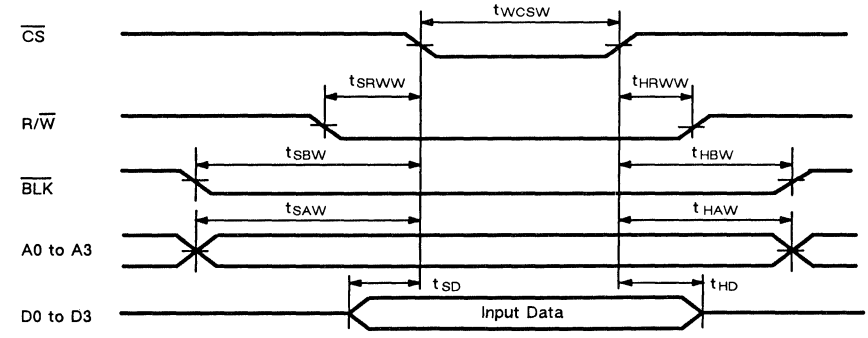

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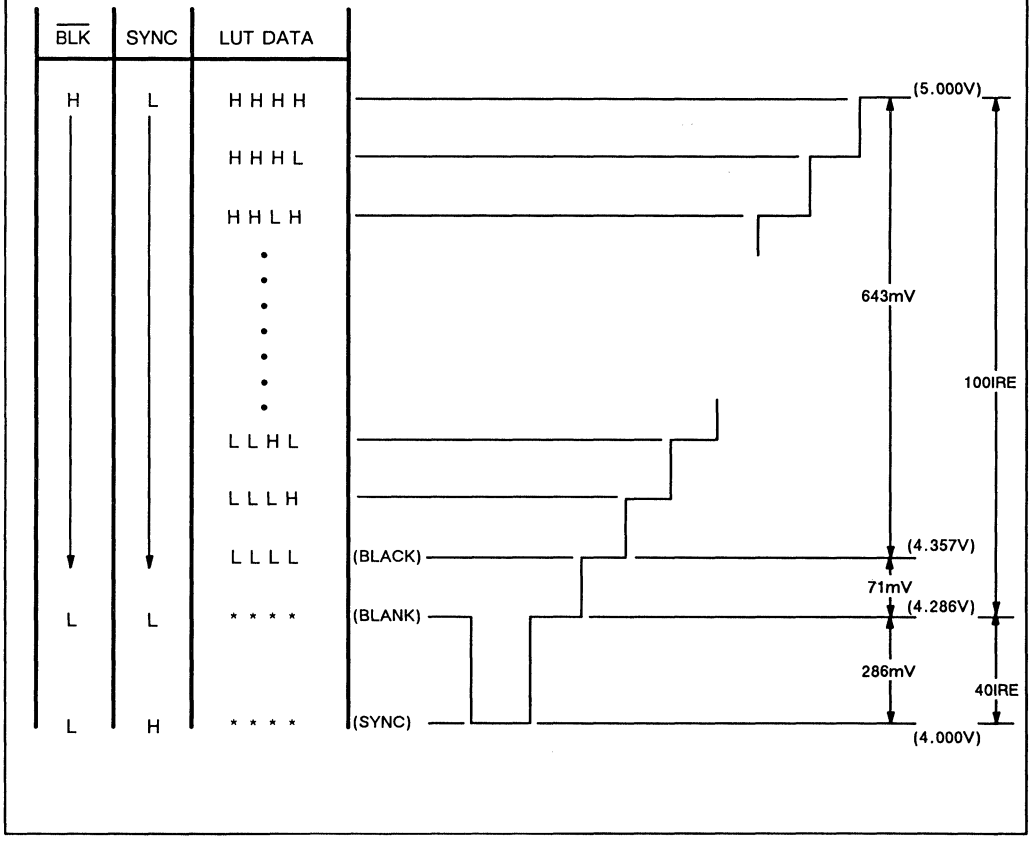
Fig. 5 — DAC OUTPUT VOLTAGE



Note: * Don't Care
Output is pulled up to V_{CCA} at 37.5Ω.

7

Fig. 6 — EXAMPLE OF MB40874 CONNECTION CIRCUIT

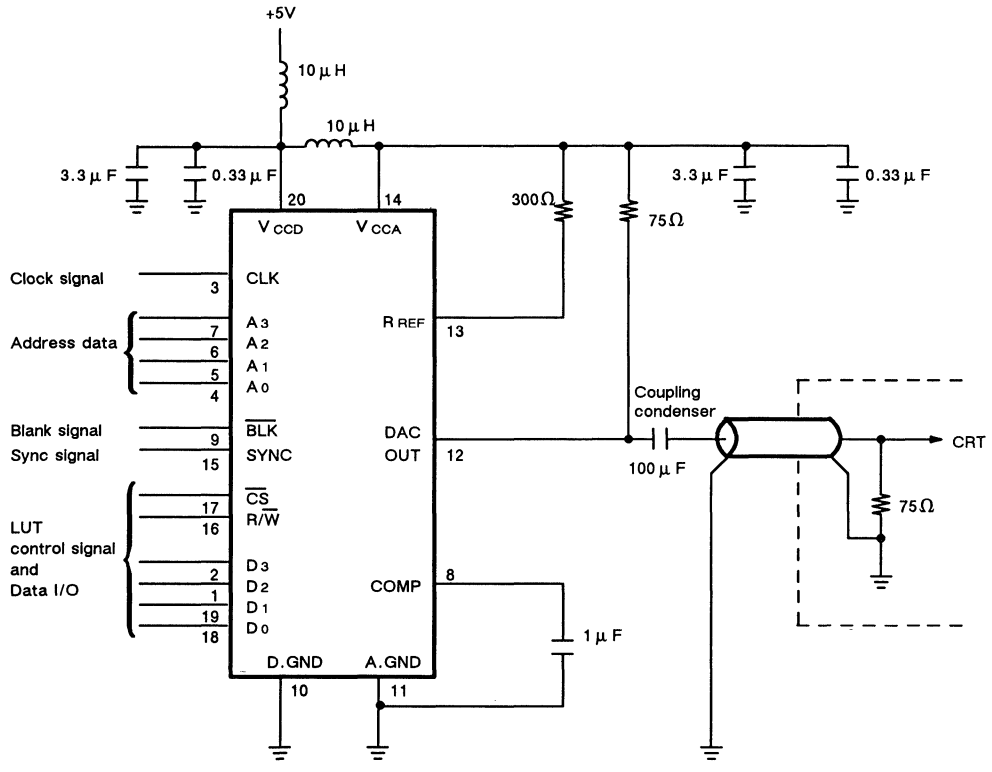
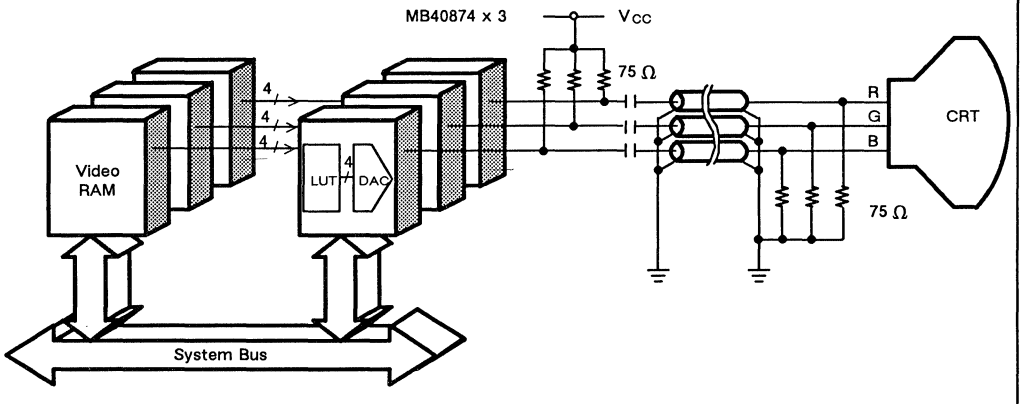


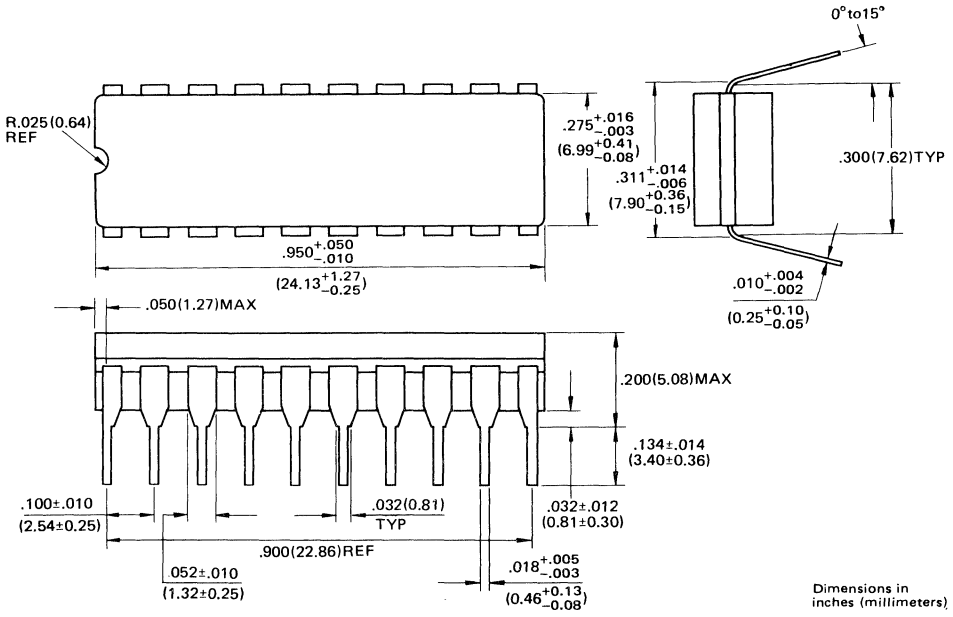
Fig. 7 — APPLICATION INFORMATION



The above application is an example of RGB system using 3 pcs of MB40874. The system allows user to simultaneously display whole 4096 kind of color defined by the number of bit of LUT and D/A converter and promptly change color tone.

PACKAGE DIMENSIONS

20-LEAD CERAMIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20C-C01)



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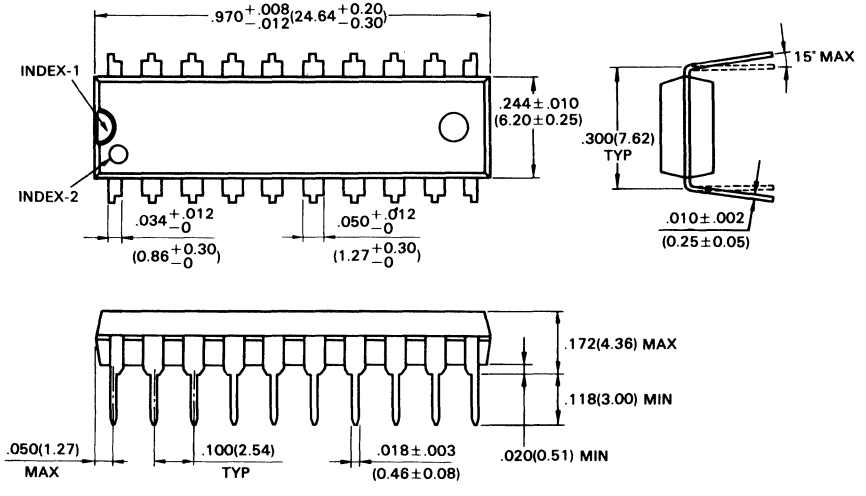
PACKAGE DIMENSIONS (Continued)

20-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-20P-M02)



Dimensions in
inches (millimeters)

7

November 1989
Edition 1.0

FUJITSU

DATA SHEET

MB40968/40968V
2-CHANNEL 8-BIT D/A CONVERTER

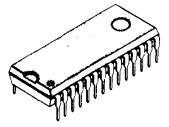
2-CHANNEL 8-BIT D/A CONVERTER

The Fujitsu MB40968/40968V is a 2-channel 8-bit high speed digital to analog converter for video frequency band fabricated by Fujitsu Advanced Bipolar Technology. This is suitable for YC signal processing of digital VCR.

- Resolution: 8-bits
- Linearity Error: ±0.2% (Max)
- Maximum Conversion Rate: 30MHz (Min)
- Analog Output Voltage Range: 3 to 5V
- Reference Voltage Output:

  MB40968: Resistance-type potential divider output (3/5 x V_{CCA})
  MB40968V: Band Gap Reference output (V_{CCA}–2 [V])

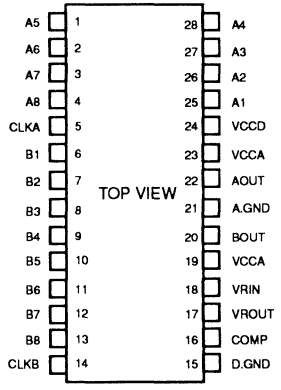
- Digital Input Voltage: TTL level
- Single Power Supply Voltage: +5.0 [V]
- Power Dissipation: 270 [mW] (Typ)



PLASTIC PACKAGE
DIP–28P–M03

PLASTIC PACKAGE
FPT–28P–M01

PIN ASSIGNMENT



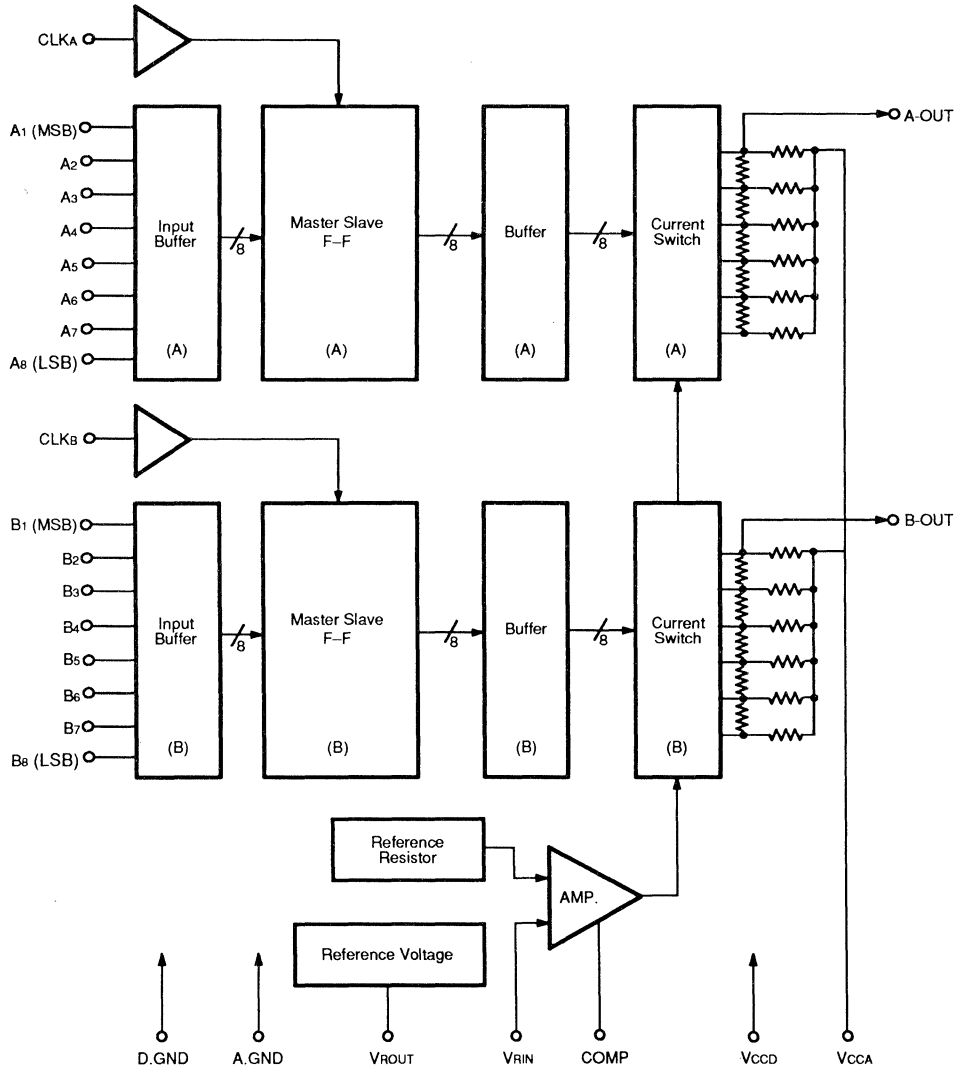
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE.)

Ratings	Symbol	Value	Unit
Power Supply Voltage	V_{CCA}, V_{CCD}	–0.5 to +7.0	V
Digital Input Voltage	V_{ID}	–0.5 to +7.0	V
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 — MB40968/40968V BLOCK DIAGRAM



PIN DESCRIPTION

Pin Number	Symbol	I/O	Descriptions
25 to 28 1 to 4	A_1 to A_8	I	A-channel Digital Signal Inputs: A_1 (MSB), A_8 (LSB)
6 to 13	B_1 to B_8	I	B-channel Digital Signal Inputs: B_1 (MSB), B_8 (LSB)
5	CLK_A	I	A-channel Clock Input
14	CLK_B	I	B-channel Clock Input
24	V_{CCD}	–	Power Supply for Digital Circuit
19, 23	V_{CCA}	–	Power Supply for Analog Circuit, two pins (19,23) should be used
5	D-GND	–	Ground for Digital Circuit
21	A-GND	–	Ground for Analog Circuit
18	V_{RIN}	I	Terminal for reference voltage input. Zero scale voltage of analog output is specified applying any voltage to this terminal. Input reference voltage should be 2.7 to 4.3V and, $V_{CCA} - V_{RIN} \leq 2.2V$.
17	MB40968 V_{ROUT}	O	Terminal for reference voltage output by resistance-type potential divider. Analog output of "V_{CCA} to 3/5 x V_{CCA}" is supplied connecting this terminal with V_{RIN} terminal.
	MB40968V V_{ROUT}	O	Terminal for reference voltage output consists of Band Gap reference. This terminal supplies the voltage of "V_{CCA} to V_{CCA} –2V". 2V output is maintained connecting this terminal with V_{RIN}, even if the power supply fluctuates frequently.
16	COMP	–	Terminal for phase compensation capacitance; Capacitance of 1μF or more should be inserted between COMP and A-GND.
22	A_{OUT}	O	A-channel Analog Signal Output
20	B_{OUT}	O	B-channel Analog Signal Output

7

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CCA}, V_{CCD} ($V_{CCA} - V_{CCD}$)	4.75 (–0.2)	5.00	5.25 (0.2)	V
Analog Reference Voltage	V_{RIN}	2.70	3.00	4.30	V
High Level Digital Input Voltage	V_{IHD}	2.0			V
Low Level Digital Input Voltage	V_{ILD}			0.8	V
Clock Frequency	f_{CLK}			30	MHz
Data Set Up Time	t_S	10.0			ns
Data Hold Time	t_h	4.0			ns
High Level Clock Pulse Width	t_{W+}	10.0			ns
Low Level Clock Pulse Width	t_{W-}	10.0			ns
Phase Compensation Capacitance	C_{COMP}	1.0			µF
Operating Temperature	T_A	0		70	°C

7

ELECTRICAL CHARACTERISTICS

[V_{CC} = 4.75 to 5.25 (V), T_A = 0 to 70°C]

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Resolution	–				8	Bit
Linearity Error	LE	DC			±0.2	%
Reference Input Current	I_{RIN}	V_{RIN}, V_{ROUT}			10	µA
High Level Digital Input Current	I_{IND}	V_{IND} = 2.7 (V)			20	µA
Low Level Digital Input Current	I_{ILD}	V_{ILD} = 0.4 (V)	–100			µA
2-channel's Output Voltage Ratio	FSR	V_{CC} = 5.00 (V) V_{RIN}, V_{ROUT}	0		4	%
Full-Scale Analog Output Voltage	V_{OFS}	V_{CC} = 5.00 (V) V_{RIN}, V_{ROUT}	V_{CCA}–15	V_{CCA}		mV
Zero-Scale Analog Output Voltage	V_{OZS}	V_{CC} = 5.00 (V) V_{RIN} = 3.000 (V)	2.938	3.008	3.078	V
Output Resistance	R_O	T_A = 25°C	192	240	288	Ω
Power Supply Current	I_{CC}	V_{CC} = 5.25 (V) V_{RIN}, V_{ROUT}		54*	80	mA

Note: *V_{CC} = 5.00 (V)

MB40968

Reference Output Voltage	V_{ROUT}	V_{CC} = 5.00 (V)	2.900	3.000	3.100	V

MB40968V

Reference Output Voltage	V_{ROUT}		V_{CCA} –1.800	V_{CCA} –2.000	V_{CCA} –2.200	V
Reference Output Voltage Temperature Constant				100		ppm/°C

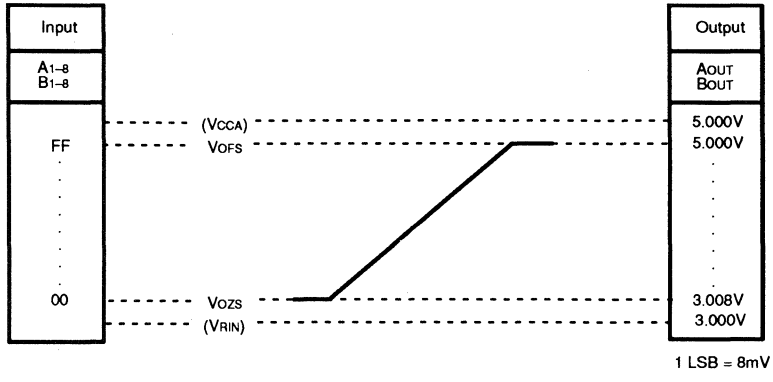
SWITCHING CHARACTERISTICS

[V_{CC} = 4.75 to 5.25 (V), T_A = 0 to 70°C]

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Minimum Conversion Rate	F_S		30			MSPS
Output Delay Time	t_{pd}	AOUT, BOUT 240Ω		10		ns
Output Rise Time	t_r	AOUT, BOUT 240Ω		5		ns
Output Fall Time	t_f	AOUT, BOUT 240Ω		5		ns
Reset Time	t_{set}	AOUT, BOUT 240Ω		15		ns

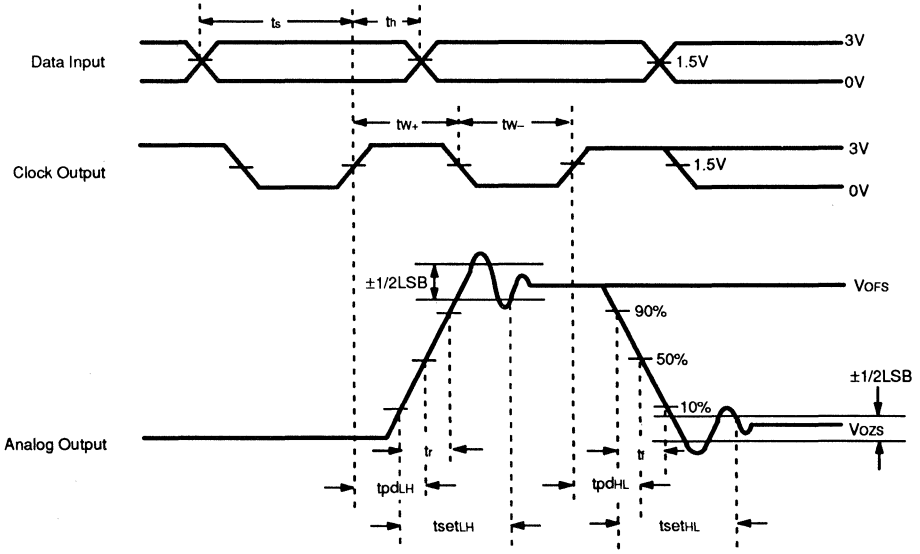
7

Fig. 2 – DAC OUTPUT VOLTAGE



SWITCHING CHARACTERISTICS (Continued)

Fig. 3 – TIMING DIAGRAM



7

Fig. 4 – DIGITAL INPUT EQUIVALENT CIRCUIT (A_1 to A_8, B_1 to B_8, CLK_A, CLK_B)

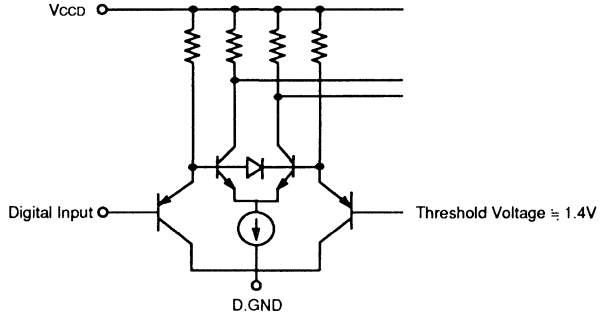


Fig. 5 – ANALOG OUTPUT EQUIVALENT CIRCUIT (A_{OUT}, B_{OUT})

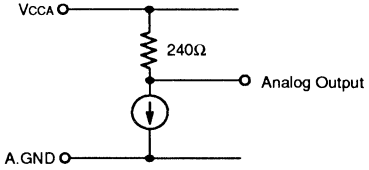


Fig. 6 – MB40968 REFERENCE OUTPUT VOLTAGE (V_{ROUT})

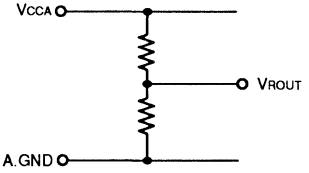
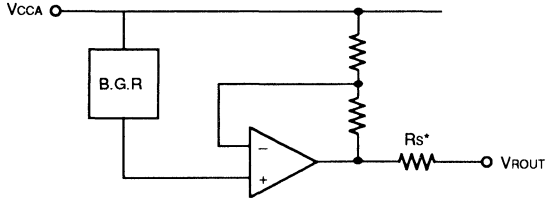


Fig. 7 – MB40968V REFERENCE OUTPUT VOLTAGE (V_{ROUT})



Note: *Reference for preventing over current when short circuit with GND.

7

The relations between Digital input code and Analog output voltage of MB40968/40968V are ideally indicated as follows.

$$V_{IN} = V_{CCA} - \frac{256 - N}{256} \cdot (V_{CCA} - V_{RIN}) \qquad N: 0 \text{ to } 255 \text{ Digital Input Code}$$

$$V_{OFS} = V_{CCA}$$

$$V_{OZS} = V_{CCA} - \frac{255}{256} \cdot (V_{CCA} - V_{RIN})$$

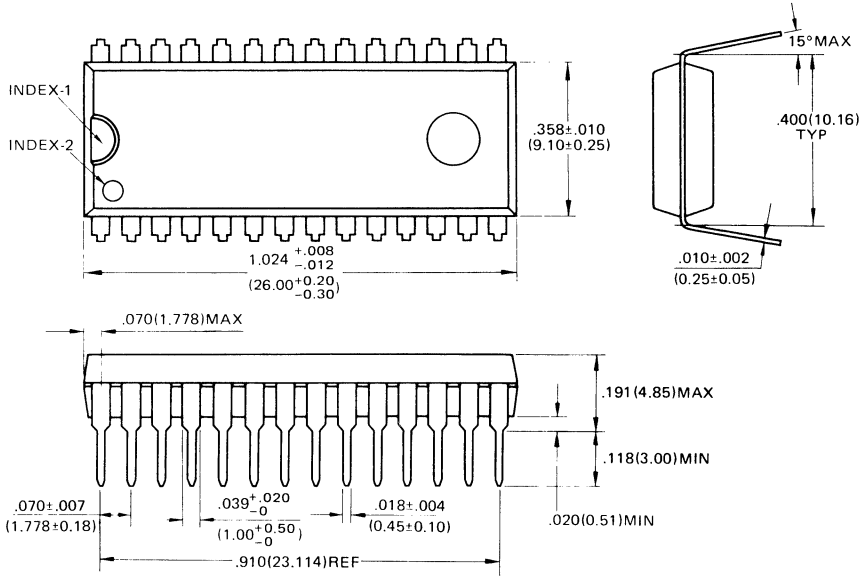
Output Voltage Ratio between 2 channels is calculated as follows.

$$FSR = \left[\frac{V_{OFS(A)} - V_{OZS(A)}}{V_{OFS(B)} - V_{OZS(B)}} - 1 \right] \times 100\%$$

7

PACKAGE DIMENSIONS

28–LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No.: DIP-28P-M03)

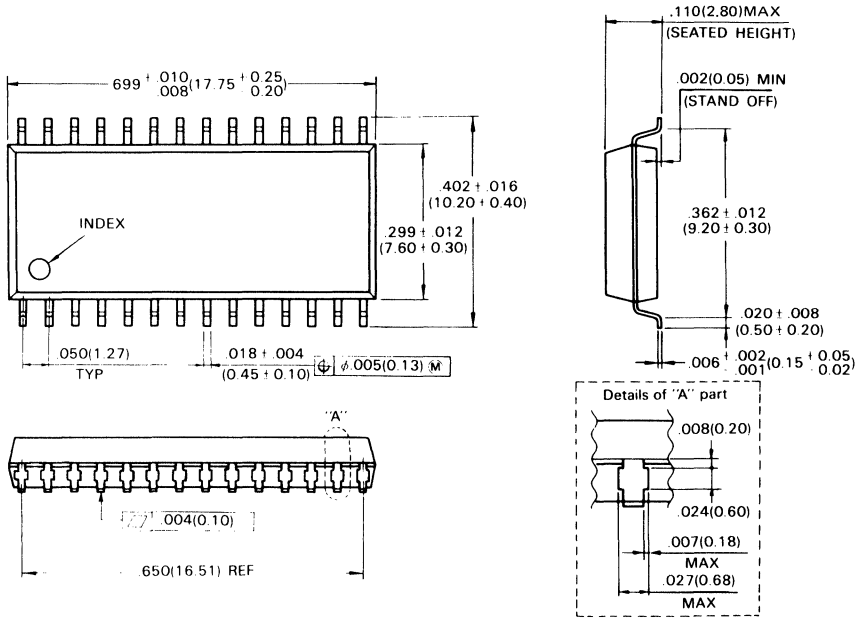


Dimensions in
inches (millimeters)

7

PACKAGE DIMENSIONS (Continued)

28–LEAD PLASTIC FLAT PACKAGE
(Case No.: FPT-28P-M01)



Dimensions in
inches (millimeters)

7

FUJITSU

8-BIT 60MSPS RGB 3-CHANNEL D/A CONVERTER

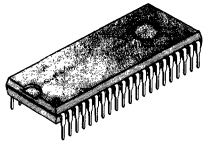
MB40978

July 1988
Edition 2.0

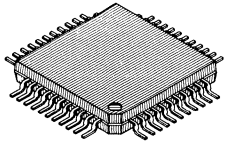
8-BIT 60MSPS RGB 3-CHANNEL D/A CONVERTER

The Fujitsu MB40978 is a 8-bit ultra high speed digital to analog converter for video frequency band fabricated by Fujitsu Advanced Bipolar Technology. Owing to adoption of RGB 3-channel input/output, it is suitable for digital TV, graphic display etc.

- Resolution : 8 bits
- Linearity : ±0.2% max.
- Maximum Conversion Rate : 60 MSPS min.
- Analog Output Voltage Range : V_{CC} to V_{CC}-1V
- Digital Input Voltage : TTL Level
- Single Power Supply Voltage : +5.0V
- Power Dissipation : 350mW typ.
- Package : Plastic DIP Package
  : Plastic Flat Package

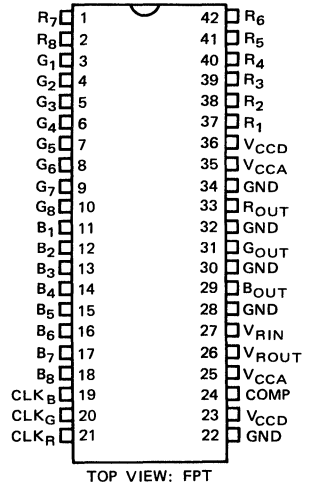


PLASTIC PACKAGE
DIP-42P-M02



PLASTIC PACKAGE
FPT-44P-M01

PIN ASSIGNMENT
TOP VIEW: DIP



TOP VIEW: FPT
See Page 10

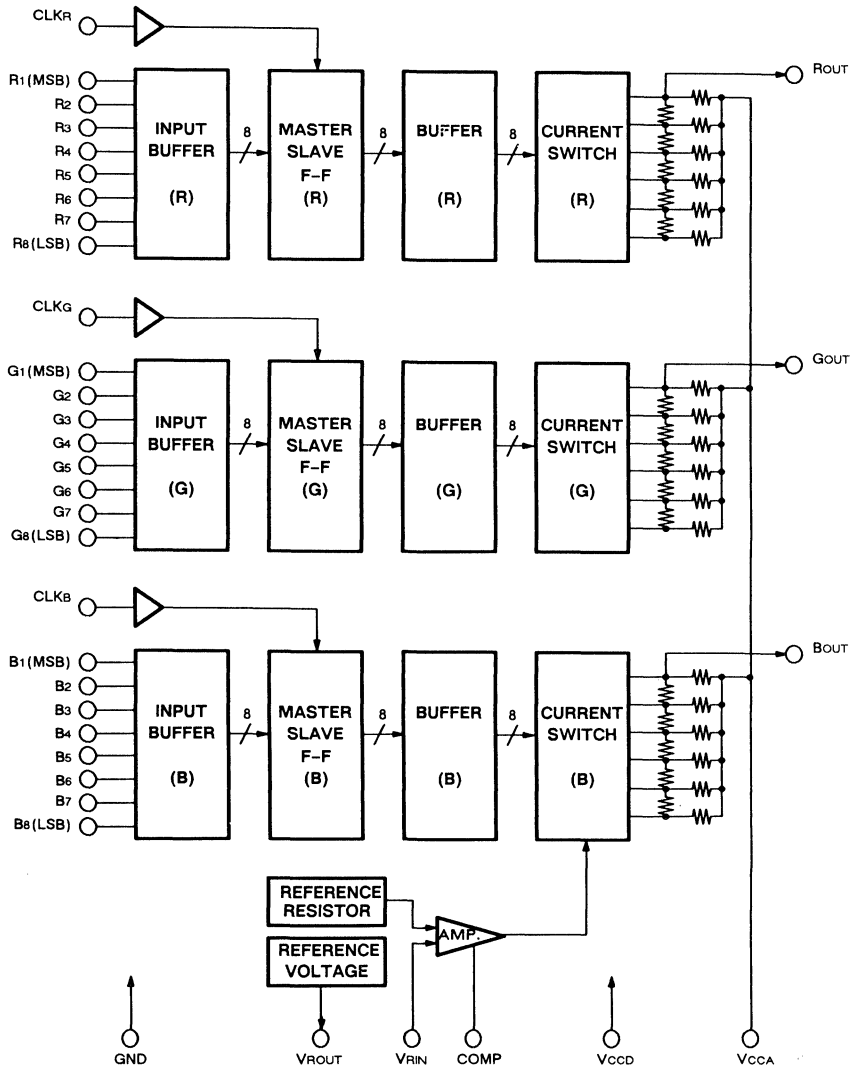
ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CCA}, V_{CCD}	−0.5 to +7.0	V
Digital Input Voltage	V_{ID}	−0.5 to +7.0	V
Storage Temperature	T_{STG}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB40978 BLOCK DIAGRAM



7

PIN DESCRIPTION

Pin Number	Symbol (DIP Pin Assignment)	Descriptions
R_1 to R_8	1, 2, 37 to 42	R-channel Digital Signal Inputs V_{IH} = 2.0V min. V_{IL} = 0.8V max.
G_1 to G_8	3 to 10	G-channel Digital Signal Inputs
B_1 to B_8	11 to 18	B-channel Digital Signal Inputs
R_{OUT}	33	R-channel Analog Signal Output
G_{OUT}	31	G-channel Analog Signal Output
B_{OUT}	29	B-channel Analog Signal Output
CLK_R	21	R-channel Clock Input V_{IH} = 2.0V min. V_{IL} = 0.8V max.
CLK_G	20	G-Channel Clock Input
CLK_B	19	B-channel Clock Input
V_{RIN}	27	Reference Voltage Input V_{CC} = −1.2V min.
V_{ROUT}	26	Reference Voltage Output
COMP	24	This pin is provided to connect a phase compensation capacitance. 1μF min capacitor is connected between GND.
V_{CCA}	25, 35	Power Supply for Analog Circuit 5V ± 5%
V_{CCD}	23, 36	Poer Supply for Digital Circuit 5V ± 5%
GND	22, 28, 30, 32, 34	Ground

7

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CCA}, V_{CCD} (V_{CCA}-V_{CCD})	4.75 (−0.2)	5.0	5.25 (0.2)	V
Analog Reference Voltage*	V_{RIN}	3.70	4.00	4.30	V
Digital High-level Input Voltage	V_{IHD}	2.0			V
Digital Low-level Input Voltage	V_{ILD}			0.8	V
Clock Frequency	f_{CLK}			60	MHz
Set-up Time	t_S	10			ns
Hold Time	t_H	4.0			ns
Minimum High Pulse Width	t_{W+}	7.5			ns
Minimum Low Pulse Width	t_{W-}	7.5			ns
Phase Compensation Capacitance	C_{COMP}	1.0			μF
Operating Temperature	T_A	0		70	°C

Note: *$V_{CCA} - V_{REF} \leq 1.2V$

7

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75 to 5.25V, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Resolution					8	Bits
Linearity Error	LE				±0.5	LSB
Reference Input Current	I_{RIN}	V_{RIN}, V_{ROUT} Short			10	μA
Reference Output Voltage	V_{ROUT}	V_{CC} = 5.00V	3.900	4.000	4.100	V
Digital High-level Input Current	I_{IHD}	V_{IHD} = 2.7V			20	μA
Digital Low-level Input Current	I_{ILD}	V_{ILD} = 0.4V	−100			μA
RGB Output Voltage Ratio	FSR		0	2	8	%
Full-Scale Output Voltage	V_{OFS}	V_{CC} = 5.00V V_{RIN}, V_{ROUT} Short	V_{CCA} −15	V_{CCA}		mV
Zero-Scale Output Voltage	V_{OZS}	V_{CC} = 5.00V V_{RIN} = 4.00V	3.944	4.004	4.064	V
		V_{CC} = 5.00V V_{RIN}, V_{ROUT} Short	3.884	4.004	4.124	V
Output Resistance	R_O			240		Ω
Power Supply Current	I_{CC}	V_{CC} = 5.25V V_{RIN}, V_{ROUT} Short		*70	102	mA

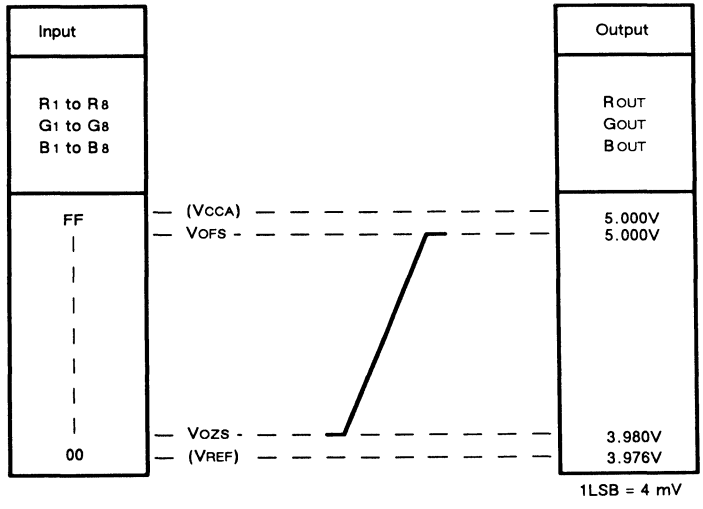
Note: *V_{CC} = 5.00V

SWITCHING CHARACTERISTICS

(V_{CC} = 4.75 to 5.25V, T_A = 0 to 70°C)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Maximum Conversion Rate	F_S	60			MSPS
Output Delay Time	t_{pd}		10		ns
Output Rise Time	t_r		5		ns
Output Fall Time	t_f		5		ns

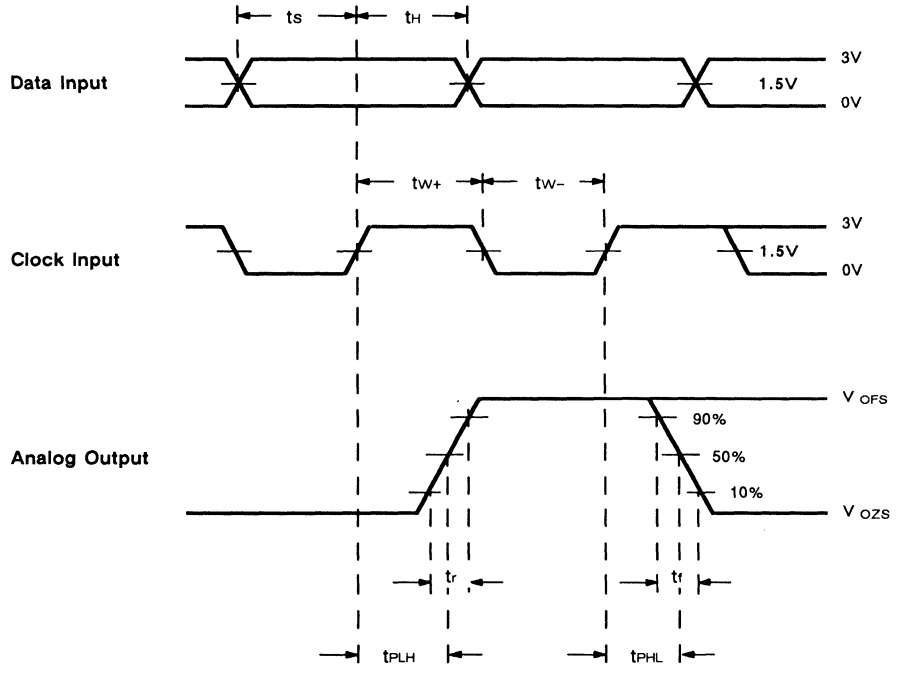
Fig. 2 – DAC OUTPUT VOLTAGE



7

SWITCHING CHARACTERISTICS (continued)

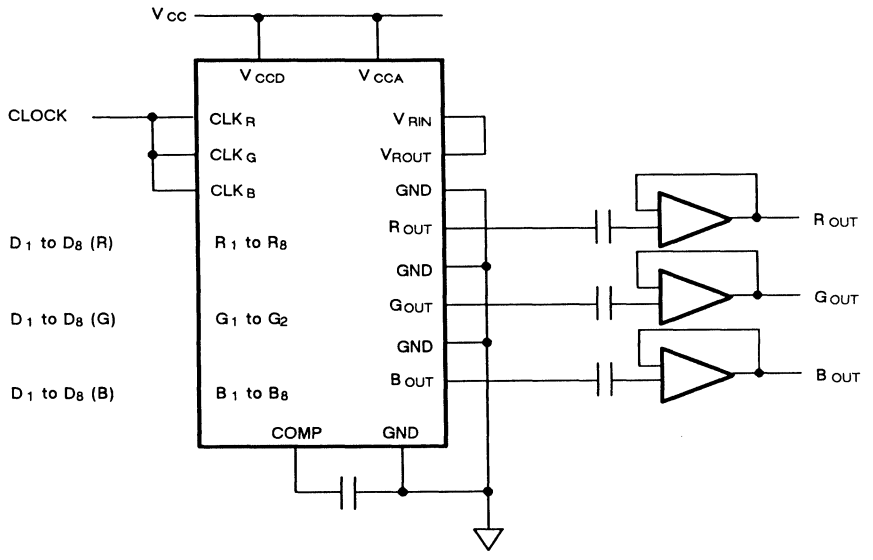
Fig. 3 – TIMING DIAGRAM



7

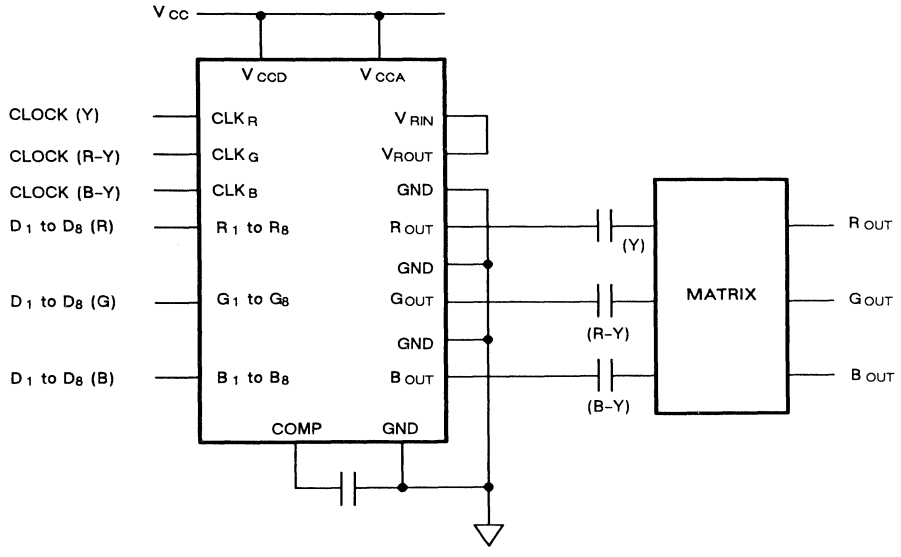
APPLICATION EXAMPLES

Fig. 4 – RGB SIGNAL PROCESS



APPLICATION EXAMPLES (continued)

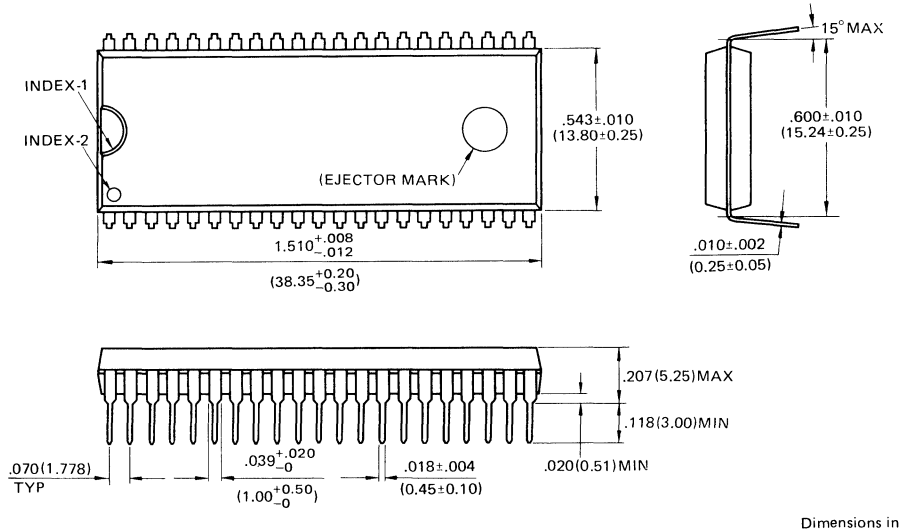
Fig. 5 – COMPONENT SIGNAL PROCESSING



7

PACKAGE DIMENSIONS

42-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-42P-M02)

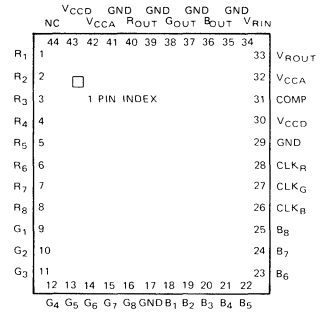


Dimensions in
inches (millimeters)

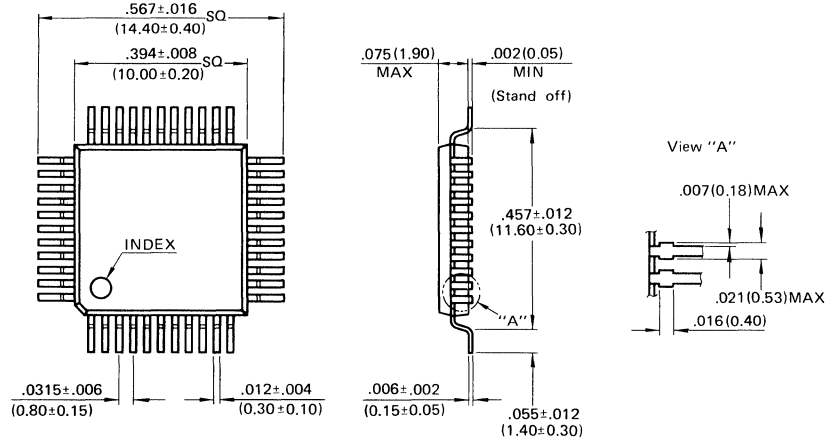
7

PACKAGE DIMENSIONS (continued)

PIN ASSIGNMENT



44-LEAD PLASTIC FLAT PACKAGE
(CASE NO.: FPT-44P-M01)



Dimensions in
inches (millimeters)

7

FUJITSU

6-BIT AD/DA CONVERTER WITH CLAMP CIRCUIT

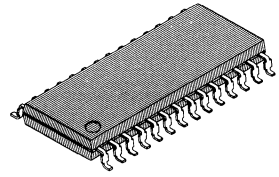
MB40176

September 1988
Edition 1.0

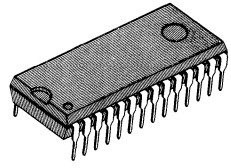
6-BIT AD/DA CONVERTER WITH CLAMP CIRCUIT

The Fujitsu MB40176 is a low power 6-bit AD/DA converter which is fabricated with Fujitsu Advanced Bipolar Technology. Owing to adoption of clamper and reference circuitry, it is suitable for video signal processing.

- Resolution : 6 bits
- Linearity Error : ±0.8% max.
- Maximum Conversion Rate : 20 MHz min.
- Analog Input Voltage Range : 0 to 1.0 V
- Analog Output Voltage Range : V_{CC} to V_{CC} - 1 V
- Digital I/O Level : TTL Level
- Power Supply Voltage : +5 V
- Power Dissipation : 300 mW typ.
- Package
  28 pin Plastic FLAT Package (Suffix: -PF)
  28 pin Plastic DIP Package (Suffix: -P)

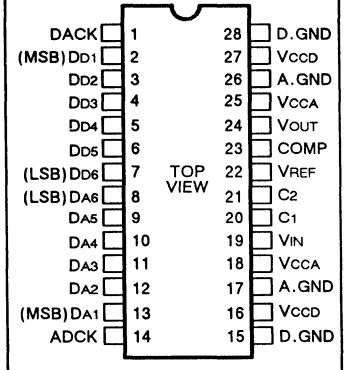


PLASTIC PACKAGE
FPT-28P-M01



PLASTIC PACKAGE
DIP-28P-M03

PIN ASSIGNMENT



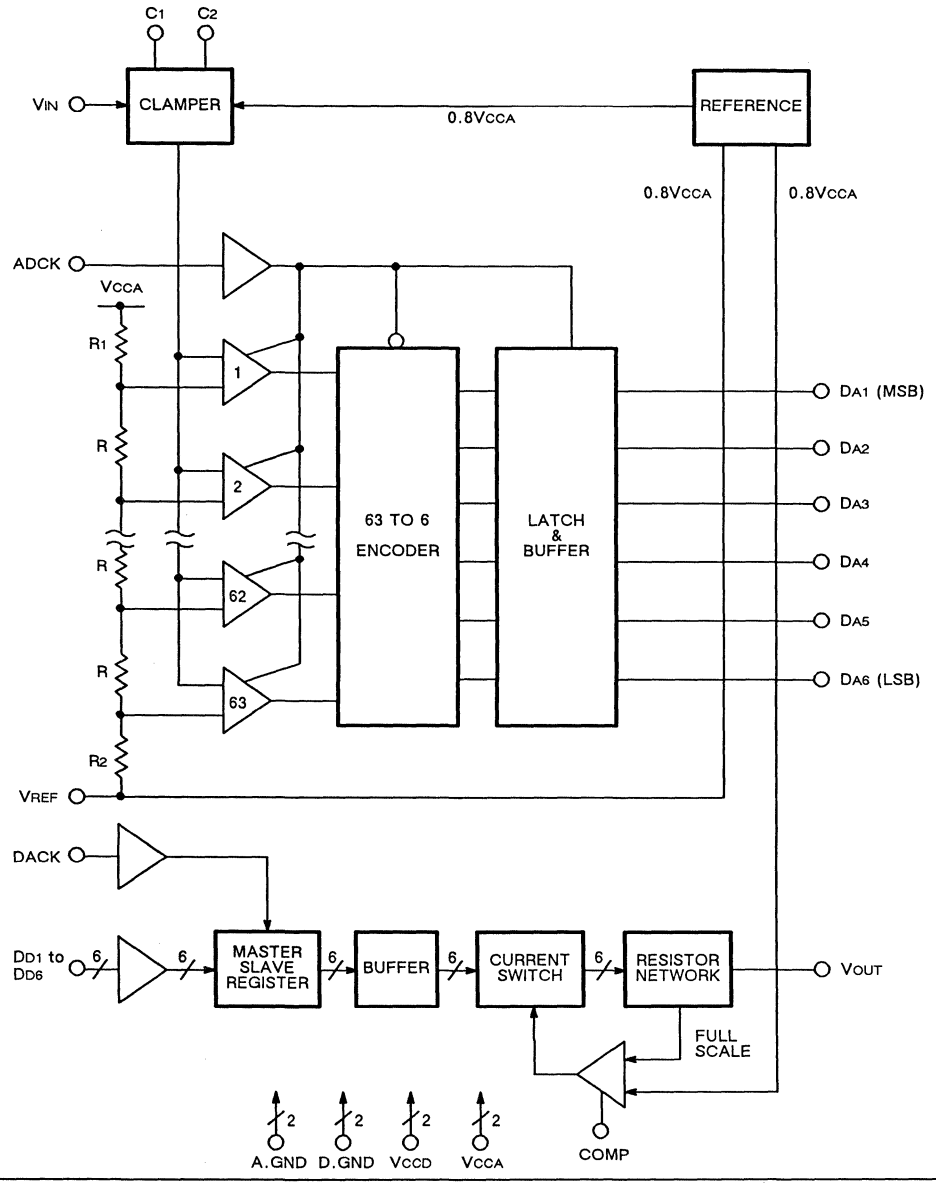
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CCA}, V_{CCD}	-0.5 to +7.0	V
Digital Input Voltage	V_{IND}	-0.5 to +7.0	V
Analog Input Voltage	V_{INA}	-0.5 to V_{CC} +0.5	V
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 — MB40176 BLOCK DIAGRAM



7

PIN DESCRIPTIONS

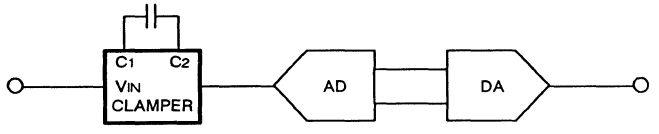
Section	Symbol	Pin No.	Type	Name & Function
A/D	V_{IN}	19	—	Analog signal input.
	V_{REF}	22	—	Reference voltage output.
	D_{A1} to D_{A6}	8 to 13	—	Digital signal outputs.
	C_1	20	—	Clamp capacitor is connected between these pins.
	C_2	21	—	
	ADCK	14	—	A/D conversion clock input.
D/A	V_{OUT}	24	—	Analog signal output.
	D_{D1} to D_{D6}	2 to 7	—	Digital signal inputs.
	COMP	23	—	Phase compensation capacitor is connected.
	DACK	1	—	D/A conversion clock input
Common	V_{CCA}	18, 25	—	Power supply for analog circuit.
	V_{CCD}	16, 27	—	Power supply for digital circuit.
	A.GND	17, 26	—	Ground for analog circuit.
	D.GND	15, 28	—	Ground for digital circuit.

7

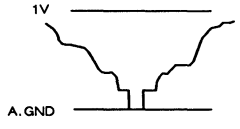
FUNCTIONAL DESCRIPTIONS

CLAMPER OPERATION

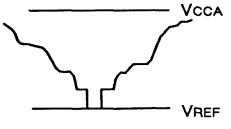
On-chip clamper is peak detection type which clamps the sink top of composite signal. Clamp voltage is common to the reference voltage (0.8 V_{CC}) of AD and DA circuits.



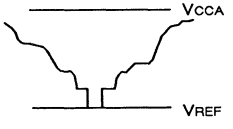
Input level of V_{IN}



Input level of AD circuit



Output level of DA circuit



RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage	V_{CCA}, V_{CCD}	4.75	5.0	5.25	V
Digital High-level Input Voltage	V_{IHD}	2.0			V
Digital Low-level Input Voltage	V_{ILD}			0.8	V
Clock Frequency	f_{CLK}			20	MHz
Clock Pulse Width at High Level	t_{W+}	20			ns
Clock Pulse Width at Low Level	t_{W-}	20			ns
Set-up Time	t_S	12.5			ns
Hold Time	t_H	7.5			ns
Phase Compensation Capacitance	C_{COMP}	1.0			µF
Clamp Capacitance	C_{CLAMP}	1.0			µF
Reference Voltage Capacitance	C_{VREF}	1.0			µF
Operating Temperature	T_A	0		70	°C

ELECTRICAL CHARACTERISTICS

ANALOG CIRCUIT DC CHARACTERISTICS (V_{CCA} = V_{CCD} = 5V±5%, T_A = 0 to 70°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Resolution					6	Bits
Linearity Error	LE	DC			±0.5	LSB
Analog Input Current	I_{IN}		-400			µA
Reference Voltage	V_{REF}*		3.9	4.0	4.1	V
Clamp Voltage	V_{CLP}			V_{REF}		V
Full-Scale Output Voltage	V_{OFS}			V_{CCA}		V
Zero-Scale Output Voltage	V_{OZ}			V_{REF}		V
Output Resistance	R_O			240		Ω
Power Supply Current	I_{CC}			60*	90	mA

Note: * V_{CCA} = V_{CCD} = 5.0V

DIGITAL CIRCUIT DC CHARACTERISTICS (V_{CCA} = V_{CCD} = 5V±5%, T_A = 25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Digital High-level Output Voltage	V_{OHD}		2.7			V
Digital Low-level Output Voltage	V_{OLD}	I_{OL} = 1.6mA			0.4	V
Digital High-level Input Voltage	V_{IHD}		2.0			V
Digital Low-level Input Voltage	V_{ILD}				0.8	V
Digital High-level Input Current	I_{IHD}				20	µA
Digital Low-level Input Current	I_{ILD}		-100			µA

SWITCHING CHARACTERISTICS

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Maximum Conversion Rate	Fs		20			MSPS
Digital Output Delay Time	t_{PDD}			15	30	ns
Analog Output Delay Time	t_{PDA}			13		ns
Analog Output Rise Time	t_r			15		ns
Analog Output Fall Time	t_f			15		ns

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Fig. 2 — APPLICATION CIRCUIT

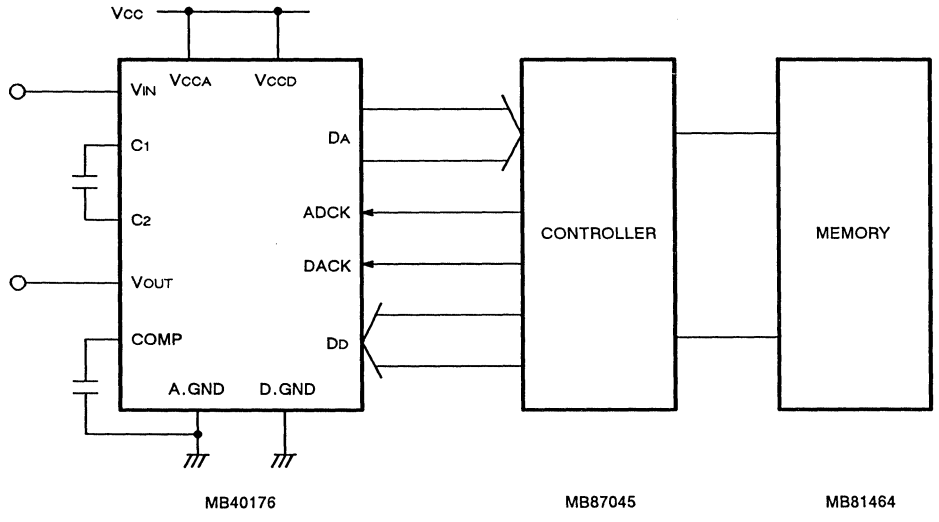

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Fig. 3 — TYPICAL CONNECTION EXAMPLE

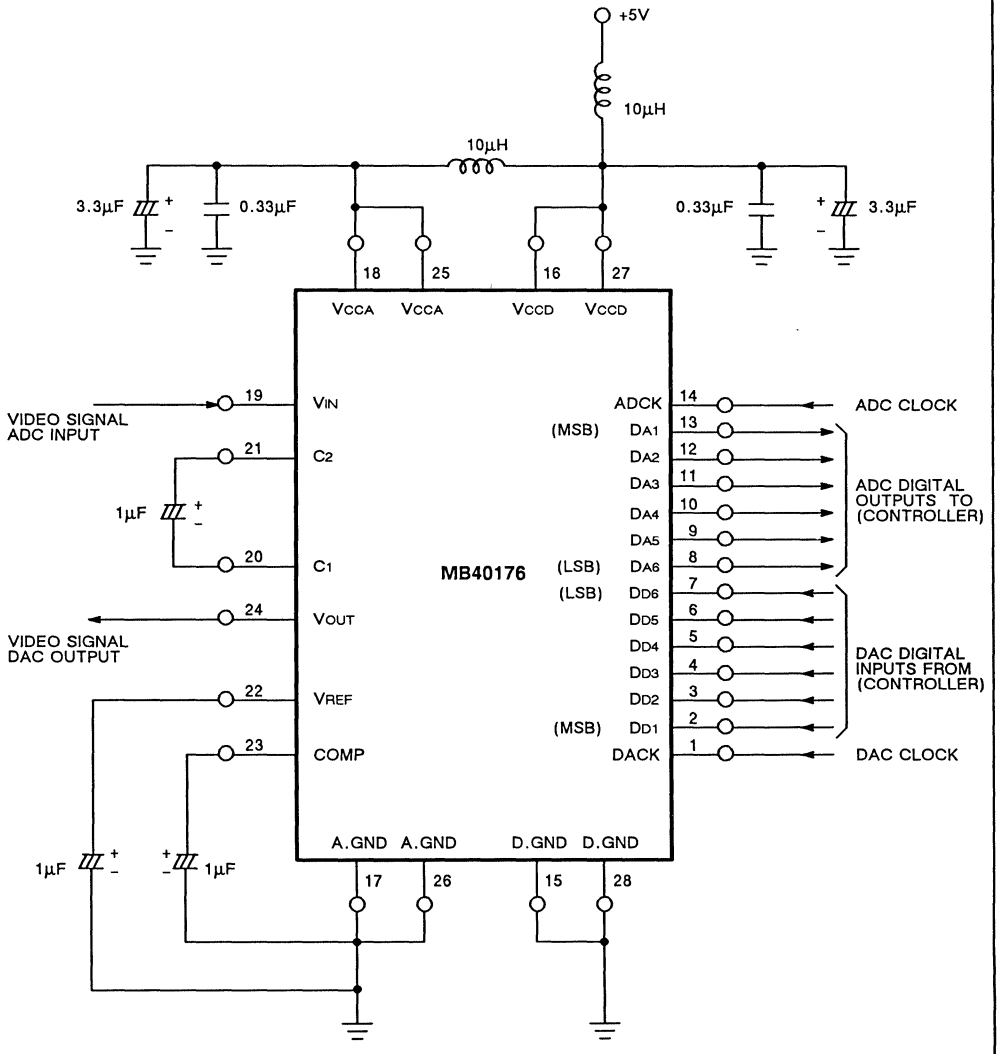

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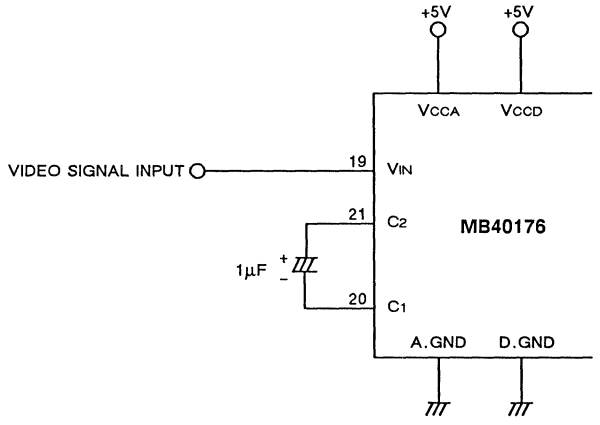
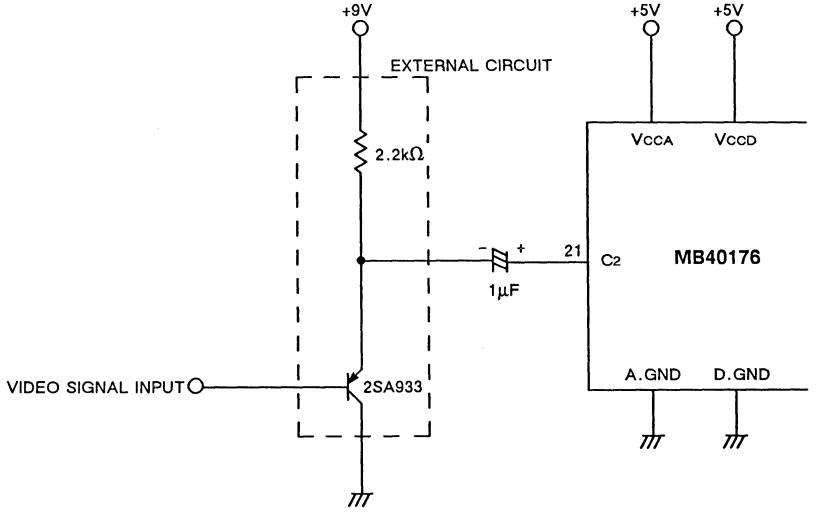
Fig. 4 — CONNECTION EXAMPLE ON-CHIP INPUT PNP TRANSISTOR IS UTILIZED



Note: Input impedance of V_{IN} input pin (19) is about 20 kΩ, please pay attention to output impedance of signal source.

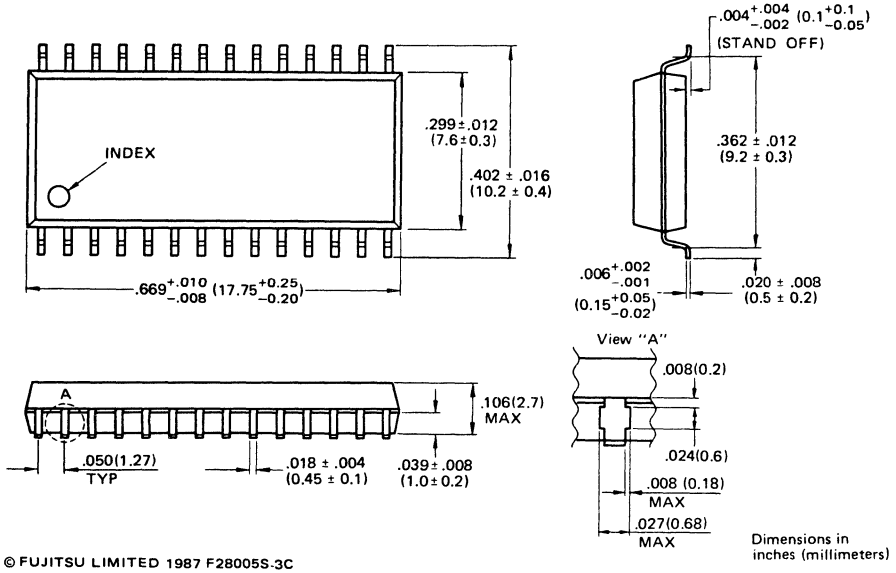
Fig. 5 — CONNECTION EXAMPLE INPUT PNP TRANSISTOR OF CLAMPER CIRCUIT IS PUT EXTERNALLY



Note: Both V_{IN} (19) and C_1 (20) are connected with V_{CCA}.

PACKAGE DIMENSIONS

28-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-28P-M01)



Dimensions in inches (millimeters)

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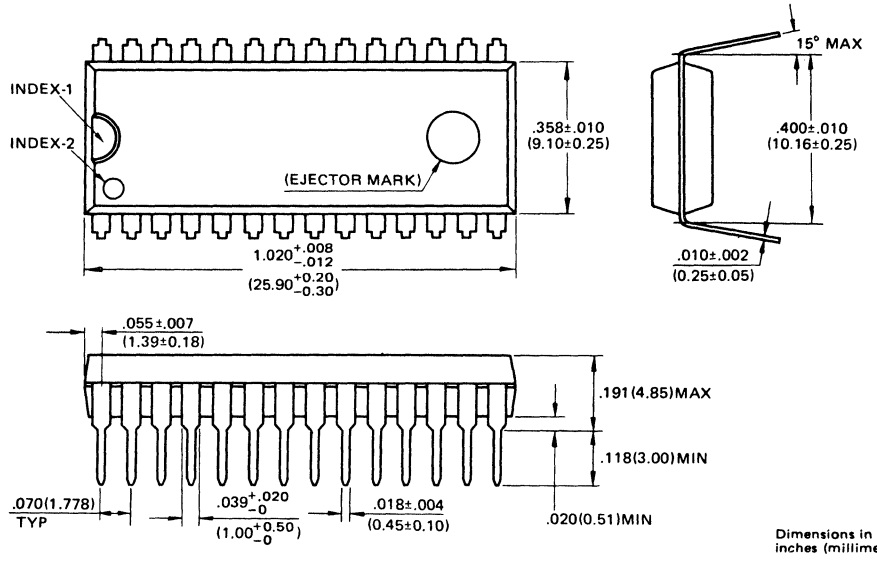
PACKAGE DIMENSIONS (Continued)

28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-28P-M03)



Dimensions in inches (millimeters)

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FUJITSU

16-BIT A/D AND D/A CONVERTER

MB87020

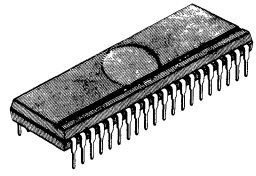
September 1988
Edition 1.0

16-BIT A/D AND D/A CONVERTER

The Fujitsu MB87020 is a 50kSPS (Kilo Sample Per Second) 16-bit Analog-to-Digital and Digital-to-Analog converter fabricated by Fujitsu Advanced CMOS technology. AD or DA function is selected by MODE input.

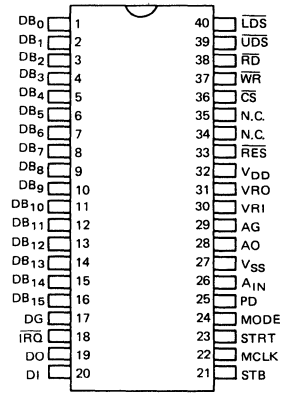
The MB87020 is synchronous/asynchronous 8/16-bit oriented data interface in order to transfer data between any processor directly and easily, and also serial data can be managed.

- Conversion Mode Selectable: A to D or D to A
- High Resolution: 16-bit
- High Conversion Speed: 50 kSPS max.
- High Linearity: 12-bit
- Low Power Dissipation and Stand by Mode Available
- Microprocessor oriented 8/16-bit bus compatibility including interrupt request as conversion completion
- Serial Data Port Available
- On-chip Sample and Hold circuit for Analog Input/Output
- On-chip Reference Voltage Generator: 2.5V typ.
- External Reference Voltage can be used.
- Power Supply Voltage: ±5V
- Packag: 40-pin Plastic Dual In-Line Package



PLASTIC PACKAGE
DIP-40P-M01

(TOP VIEW)



(DIP-40P-M01)

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	−0.3 to +7.0	V
	V_{SS}	−7.0 to +3.0	V
Analog Input/Output Voltage	V_{TA}	V_{SS}−0.3 to V_{DD} +0.3	V
Digital Input/Output Voltage	V_{TD}	−0.3 to V_{DD}+0.3	V
Input/Output Current	I_T	−10 to +10	mA
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	−40 to +125	°C
Ambient Operating Temperature	T_A	0 to +70	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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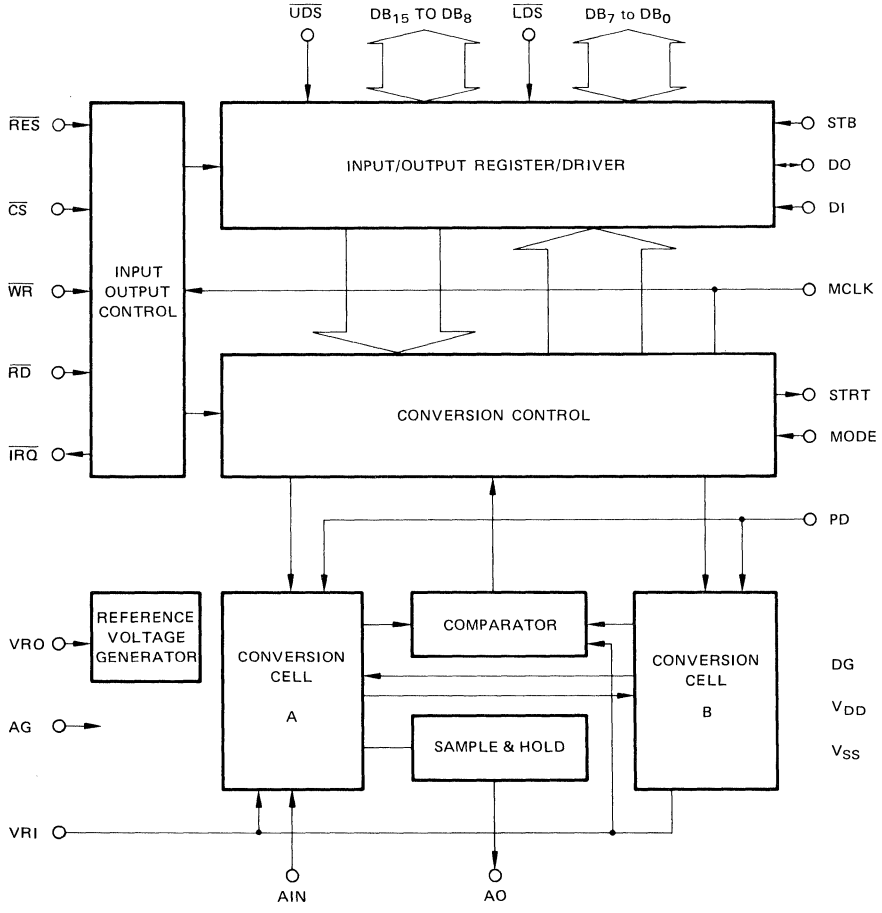
MB87020 BLOCK DIAGRAM



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PIN DESCRIPTION

Pin Name	Pin No.	Description
V_{DD}	32	+5V Power Supply Input for Digital/Analog Circuit
V_{SS}	27	–5V Power Supply Input for Digital/Analog Circuit
DG	17	Digital Ground
AG	29	Analog Ground
VRI	30	External Reference Voltage Input. +2.5V typ. When the internal reference voltage is used. VRI and VRO should be connected together.
VRO	31	Internal Reference Voltage Output. +2.5V typ.
MODE	24	Conversion Mode Select Input: When MODE is high, A/D mode is selected. When MODE is low, D/A mode is selected.
PD	25	Stand-by Mode Select Input for Analog Circuit: When PD is high, Stand-by mode is selected. When PD is low, the normal operation is selected.
$\overline{RES}$	33	Reset Input: When $\overline{RES}$ is low, all internal registers are reset and cleared. After power on, the reset operation is needed firstly.
MCLK	22	Conversion Clock Input: Conversion operation is synchronized with this clock.
A_{IN}	26	Analog Input for A/D Conversion: During STRT = H, this input data is sampled. During D/A conversion, this input pin is recommended to be tied with AG.
AO	28	Analog Output for D/A conversion: This output is updated after conversion, and keep the level until next completion of conversion.
DB_0 to DB_{15}	1 to 16	Parallel Data Input/Output: Can transmit A/D conversion data output or D/A conversion data input in 8- or 16-bit parallel. Due to three-state input, the pins are connected with microprocessor's bus directly. DB_{15} is MSB, DB_0 is LSB. When connected with 8-bit bus, DB_n and DB_{n+8} are connected together, where n = 0 to 7.
DI	20	Serial Data Input: At the rising edge of STB, the 1-bit data is transferred to the LSB of the input/output register. (See Serial Data Transfer.)
DO	19	Serial Data Output: The MSB of the input/output register is output. At the falling edge of STB, the output is changed. (See Serial Data Transfer.)
STB	21	Strobe Signal Input for Serial Data Transfer: Using $\overline{RD}$, $\overline{CS}$, $\overline{UDS}$ and $\overline{LDS}$, this input is internally gated. The rising edge of STB signal makes the output/input register shift by 1 bit. (See Serial Data Transfer.)
$\overline{CS}$	36	Chip Select Input: When $\overline{CS}$ is low, $\overline{RD}$ and $\overline{WR}$ signals are effective.
$\overline{WR}$	37	Data Write Input: When $\overline{WR}$ is low, stored data in DB_0 to DB_{15} are shifted into the input/output register, and the rising edge of the input makes the data latched and ready for AD or DA conversion operation. After $\overline{WR}$ goes high, conversion starts at the rising edge of MCLK, or at the completion of previous conversion.
$\overline{RD}$	38	Data Read Input: When $\overline{RD}$ is low, the stored data in output/input register are output at DB_0 to DB_{15}.
$\overline{UDS}$	39	High-order byte Select: When $\overline{UDS}$ is low, upper 8-bit data is transferred.
$\overline{LDS}$	40	Low-order byte Select: When $\overline{LDS}$ is low, the lower 8-bit data is transferred.
STRT	23	Conversion Start Output: This output indicates conversion start. During the first clock cycle of conversion, it becomes high. When it is high for AD conversion, A_{IN} input is sampled.
$\overline{IRQ}$	18	Interrupt Request Output as Conversion Completion: When conversion is completed, $\overline{IRQ}$ becomes low. When data transfer is instructed, ($\overline{RD}$ or $\overline{WR}$) and $\overline{CS}$, it becomes high. This output is an open-drain output.

Note: All digital input/output is TTL compatible.

OPERATIONAL DESCRIPTION

Input analog signal is converted to 16-bit digital signal or 16-bit digital signal is converted to analog signal. Either of function is selected by mode select pin. MB87020 can be used for either parallel I/O connection or serial I/O connection with microprocessor.

Parallel I/O: Connected with μP 80 series 8-bit, 68 series 8-bit, 8086 series 16-bit and 68000 series 16-bit.
Serial I/O: It needs a less signal lines compared with parallel I/O.

We are going to describe how to control MB87020 through these signal lines and receiving/delivering digital data.

1) MODE CONTROL

MB87020 has three operational modes, D/A conversion mode, A/D conversion mode and analog circuit stand-by mode. These mode is selected by MODE and PD pin as listed below.
When the mode change is indicated during converting, the actual change of operational mode is done after the completion of conversion.

Mode	PD	Function
L	L	D/A conversion mode
	H	Analog circuit stand-by mode
H	L	A/D conversion mode
	H	Analog circuit stand-by mode

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2) CONVERSION SEQUENCE

MB87020's conversion sequence comprises the following four process.

Conversion start request process — (Instruction to start conversion)
Conversion start process
Conversion process — Conversion process
Conversion completion process

The above process are synchronized with MCLK signal, but data management can be independent from MCLK signal. And during conversion, next conversion start request can be provided.

Conversion start request process

Conversion start request is generated by the write cycle ($\overline{CS}$=$\overline{WR}$=L). After write cycle is completed (Rising edge of $\overline{CS}$ or $\overline{WR}$), conversion start request is generated. During D/A mode, write is possible in using write cycle.
16-bit data is written from lower 8-bit then the upper 8-bit. After that conversion start request is generated.

$\overline{LDS}$ AND $\overline{UDS}$ IN WRITE CYCLE AND CONVERSION START REQUEST

Mode	$\overline{LDS}$	$\overline{UDS}$	Conversion Start Request	Data Xmit (Write)	Operation
D/A	L or ⊓⊔⊓	L or ⊓⊔⊓	Generated	DB_0 to DB_{15}	16-bit Parallel Write
	L or ⊓⊔⊓	H	Not Generated	DB_0 to DB_7	Low-order Byte Write
	H	L or ⊓⊔⊓	Generated	DB_0 to DB_{15}	High-order Byte Write
	H	H	Generated		Serial Data Conversion
A/D	Don't Care	Don't Care	Generated		A/D Conversion Start

⊓⊔⊓: Transmission of High to Low to High.

CONVERSION START PROCESS

When conversion is requested to start, operational conversion starts at the next rising edge of MCLK clock. When previous conversion is not completed, following conversion is postponed until previous conversion is completed.
At this moment, START becomes High level in one clock cycle in order to indicate conversion start. During this moment, it is prohibited that $\overline{WR}$ = $\overline{CS}$ = "L".
When A/D conversion, A_{IN} input is sampled at this moment.

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CONVERSION PROCESS

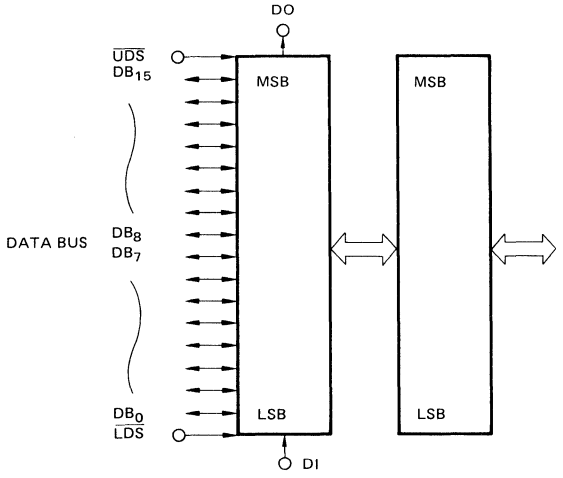
16th MCLK clock cycles are needed for one conversion process. From second MCLK clock cycle, Write Mode is available and Conversion Start Request can be generated for the following conversion.
Write Mode can be repeated in this period, but only the last Conversion Start Request and the last written data are effective.

CONVERSION COMPLETION PROCESS

Conversion Process is completed after 16th MCKL clock cycles are passed from conversion starts.
At the end of conversion, $\overline{IRQ}$ goes low to tell the completion of the conversion outside of the chip. This output is an open-drain output and connect to microprocessor and provides interrupt request signal to it.
When Write or Read Mode is excuted, $\overline{IRQ}$ goes high.
If Conversion Start Request is generated during conversion, the next conversion will start continuously after the current conversion is completed.
The result of D/A conversion is output at A_0 at this moment and output will remain at its last level.
More than 1 MCLK cycle passed after conversion is completed, the result of A/D conversion can be read out at DB_0 to DB_{15} when $\overline{RD}$ = $\overline{CS}$ = $\overline{UDS}$ = $\overline{LDS}$ = "L".

3) DATA TRANSMISSION

Data transmission between MB87020 and external is made through I/O register. I/O register does not control conversion directly, but they store A/D conversion results or D/A conversion data. Therefore, write/read are done freely except for the time of data transmission with register which directly control at the beginning and ending of conversion.
Using this function, 8-bit parallel transmission, 8-bit serial transmission and data exchange during conversion are possible.



PARALLEL TRANSMISSION

Data is transmitted through DB_0 to DB_{15} and controlled by $\overline{CS}$, $\overline{WR}$, $\overline{RD}$, $\overline{UDS}$ and $\overline{LDS}$. In the transmission mode, it requires $\overline{CS}$ = Low. And in the write mode to MB87020, it requires $\overline{WR}$ = L and read mode, $\overline{RD}$ = L.
Upper byte (DB_8 to DB_{15}) transmission mode, it requires $\overline{UDS}$ = L, lower byte (DB_7 to DB_0), $\overline{LDS}$ = L. All required conditions are satisfied, data is transmitted. If no, data transmission mode is stopped and data is latched for write mode.
During A/D mode, data is not written regardless $\overline{UDS}$ and $\overline{LDS}$.
I/O register stores latest A/D mode result or latest written data of D/A mode. During read cycle, it is possible to read out A/D conversion result and confirm D/A conversion result. Read/write of parallel data is controlled by control signal.

DATA CONTROL SIGNAL AND PARALLEL DATA TRANSMISSION

Mode	Reso-lution (Bit)	Read/ Write	Data control signal					Condition		Conversion Start request	$\overline{IRQ}$=L Clear	Operation	
			$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	$\overline{LDS}$	$\overline{UDS}$	DB_0 to DB_7	DB_8 to DB_{15}				
A/D			L	L	X	X	X	HZ	HZ	Generated	Clear	A/D conversion start request	
			L	X	L	H	H	HZ	HZ	Not generated	Clear	Serial output	
	8	Read mode		H		L	H	Output	HZ	Not generated	Clear	Read out conversion result	Lower byte
						H	L	HZ	Output	Not generated	Clear		Upper byte
	16					L	L	Output	Output	Not generated	Clear		All byte
D/A			L	L	X	H	H	HZ	HZ	Generated	Clear	Conversion start request of serial input data	
	8	Write mode				L	H	Input	HZ	Not generated	Clear	Read out conversion result	Lower byte
						H	L	HZ	Input	Generated	Clear		Upper byte
	16					L	L	Input	Input	Generated	Clear		All byte
			L	X	L	H	H	HZ	HZ	Not generated	Clear	Serial input	
	8	Read mode		H		L	H	Output	HZ	Not generated	Clear	Confirm conversion result	Lower byte
						H	L	HZ	Output	Not generated	Clear		Upper byte
	16					L	L	Output	Output	Not generated	Clear		All byte
X			L	H	H	X	X	HZ	HZ	Not generated	Not Clear		
			H	X	X	X	X	HZ	HZ	Not generated	Not Clear		

Note: X: Don't care

SERIAL TRANSMISION

DI, DO, STB, $\overline{RD}$ and $\overline{CS}$ are used for serial transmission. $\overline{UDS}$, $\overline{LDS}$ are settled as High, $\overline{RD}$, $\overline{CS}$ indicate transmission timing.

A/D MODE (DO OUTPUT)

After conversion is completed, MSB is output at the first falling edge of MCLK clock.
When STB = H and $\overline{CS}$ = $\overline{RD}$ = L, from 2nd rising edge of MCLK clock, A/D conversion result is output serially from upper side synchronized with falling edge of STB clock.
The output after 16-bit output is not related to any of converter result.
Serial transmission is stop when STB = L and $\overline{CS}$ or $\overline{RD}$ = H.

D/A MODE (DI INPUT)

After conversion is completed, when $\overline{CS}$ = $\overline{RD}$ = L at STB = H after one clock cycle, DI is sampled as MSB and after that DI is sampled from the MSB every rising edge of STB clock.
Transmission is completed when 16th DI is sampled as $\overline{CS}$ or $\overline{RD}$ = H at STB = L.

When 2 pcs of MB87020 are used A/D, D/A mode separately with connecting DO of A/D and DI of D/A, STB, $\overline{RD}$, $\overline{CS}$ direct transmission becomes possible.
If STB clock frequency is higher than MCLK clock, other signal or other conversion data can be transmitted by time sharing serially.
If no, STB requires H, DI requires H or L.

CONVERSION RANGE AND CODE

A/D MODE

Input Voltage	Output code (DB_{15} to DB_0)
$\geq +V_{REF}$	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
$+V_{REF} - 1LSB$	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
$+V_{REF}/2$	0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
-1LSB	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
$-V_{REF}/2$	1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0
$-V_{REF} + 1LSB$	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1
$\leq -V_{REF}$	1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1

Note: V_{REF} = VRI input voltage
1LSB = $V_{REF}/2^{15}$
Output code will not become 1000 0000 0000 0000 under $-V_{REF}$ input voltage.

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D/A MODE

Input code (DB_{15} to DB_0)	Output Voltage
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	$\geq +V_{REF} - 1LSB$
0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	$+V_{REF} - 1LSB$
0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	$+V_{REF}/2$
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	-1LSB
1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1	$-V_{REF} + 1LSB$
1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	$-V_{REF} + 1LSB$

Note: V_{REF} = VRI input voltage
1LSB = $V_{REF}/2^{15}$
Code input of 1000 0000 0000 0000 will not make the output of $-V_{REF}$.

RECOMMENDED OPERATING CONDITIONS

Parmeter	Symbol	Pin Name	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	V_{DD}	4.75	5.00	5.25	V
	V_{SS}	V_{SS}	-5.25	-5.00	-4.75	V
Reference Voltage	V_{RI}	V_{RI}		2.5		V
Load Impedance	R_L	AO	20			kΩ
	C_L				20	pF
Ambient Operating Temperature	T_A		0		70	°C

DC CHARACTERISTICS

($DG = AG = 0V$, $V_{DD} = 5V \pm 5\%$, $V_{SS} = -5V \pm 5\%$, $f_{MCLK} = 800$ kHz, $V_{RI} = 2.5V$, $T_A = 0$ to 70°C)

Parameter		Symbol	Pin Name	Condition	Min	Typ	Max	Unit
Power Supply Current		I_{DD}	V_{DD}				15	mA
		I_{SS}	V_{SS}		-15			mA
Power Supply Current at Power Down		I_{DDST}	V_{DD}				1	mA
		I_{SSST}	V_{SS}		-0.5			mA
Reference Voltage		V_{RO}	V_{RI}			2.5		V
Digital High-level Input Voltage		V_{IH}	*1		2		V_{DD}	V
Digital Low-level Input Voltage		V_{IL}			0		0.8	V
Digital High-level Output Voltage		V_{OH}	*2	$I_{OH} = 0.1$mA	4.0		V_{DD}	V
				$I_{OH} = 1$mA	2.4		V_{DD}	
Digital Low-level Output Voltage		V_{OL}	*3	$I_{OL} = 2.4$mA	0		0.4	V
Digital Input Leak Current	"L" Level	I_{IL}	*3		-10		10	μA
	"H" Level	I_{IH}			-10		10	μA
$\overline{IRQ}$ Leakage Current at OFF		I_{LIRQ}	$\overline{IRQ}$	$V_{OH} = V_{DD}$	-10		10	μA
DB High-level Leakage Current at OFF		I_{LDBH}	DB_0 to DB_{15}		-10		10	μA
DB Low-level Leakage Current at OFF		I_{LDBL}		$V_{OL} = 0V$	-10		10	μA
Off -set Voltage		V_{OFF}	AIN,AO		-50		+50	mV
Linearity Error		LE				±0.02		%FSR
Differential Linearity Error		DLE				±0.02		%FSR

Note: *1: DB_0 to DB_{15}, DI, STB, MCLK, $\overline{UDS}$, $\overline{LDS}$, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, PD, MODE, $\overline{RES}$
*2: DB_0 to DB_{15}, DO
*3; DB_0 to DB_{15}, DO, $\overline{IRQ}$

AC CHARACTERISTICS

($DG = AG = 0V$, $V_{DD} = 5V \pm 5\%$, $V_{SS} = -5V \pm 5\%$, $f_{MCLK} = 800$ kHz, $V_{RI} = 2.5V$, $T_A = 0$ to $70°C$)

Parameter	Symbol	Pin Name	Condition		Min	Typ	Max	Unit
Clock Frequency	f_{MCLK}	MCLK			10		800	kHz
	f_{STB}	STB					2.5	MHz
Clock Duty Ratio	D_{MCLK}	MCLK			45	50	55	%
Sampling Rate	f_{SAMPLE}						50	kSPS
Absolute Gain	G_A		1kHz, FS -20dB sine wave 50kSPS $T_a = 25°C$ BW = 20kHz	$V_{RI} = 2.5V$	-0.1	0	+0.1	dB
				Connect to V_{RI} and V_{RO}	-0.5	0	+0.5	
Total Harmonic Distortion	T.H.D.		1kHz, sine wave 50kSPS $T_a = 25°C$ PW=20kHz	FS -20dB			-60	dB
				FS		-76		
Input Impedance (R_I/C_I)	R_I	A_{IN}	A/D mode during STRT = H		100			kΩ
	C_I					50	100	pF

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SWITCHING CHARACTERISTICS

(DG = AG = 0V, V_{DD} = 5V, V_{SS} = -5V, f_{MCLK} = 720kHz, V_{RI} = 2.5V, T_A = 25°C)

Parameter	Fig.	Symbol	Min	Max	Unit
Data Write Pulse Width	1	t_{WT}	200		ns
Data Setup Time for Data Write	1	t_{SBW}	200		ns
Data Hold Time for Data Write	1	t_{HBW}	50		ns
Data Write Interval	1	t_{IW}	200		ns
Data Non-Write $\overline{LDS}/\overline{UDS}$ Setup Time	1	t_{SDW}	50		ns
Data Non-Write $\overline{LDS}/\overline{UDS}$ Hold Time	1	t_{HDW}	50		ns
Write Command Pulse Width	1	t_{WW}	200		ns
Write Command Hold Time for First Conversion Cycle	2	t_{HWN}	0		ns
Write Command Setup Time Preventing from Conversion Start	2	t_{SWI}	100		ns
Write Command Hold Time Not to Start Conversion	2	t_{HWP}	100		ns
Write Command Hold Time for Conversion Start	2	t_{SWP}	100		ns
$\overline{WR}$ Setup Time for Data Read (D/A mode only)	3	t_{SWC}	50		ns
$\overline{WR}$ Hold Time for Data Read (D/A mode only)	3	t_{HWC}	50		ns
Data Read Pulse Width	3	t_{WR}	200		ns
Delay Time to Valid Data Output	3	t_{EB}	0	200	ns
Disappearance Time for Valid Data	3	t_{DB}	0		ns
$\overline{RD}$ Hold Time for Last Conversion Cycle	4/5	t_{HRK}	0		ns
$\overline{RD}$ Setup Time for Last Conversion Cycle	4/5	t_{SRK}	0		ns
$\overline{LDS}/\overline{UDS}$ Setup Time for Serial Data Transfer Start	5	t_{SDR}	50		ns
$\overline{LDS}/\overline{UDS}$ Hold Time for Serial Data Transfer Completion	5	t_{HDR}	50		ns
STB Setup Time for Read Command	5	t_{STR}	100		ns
STB Hold Time for Read Command	5	t_{HTR}	100		ns
High-Level STB Pulse Width	5	t_{WSH}	200		ns
Low-Level STB Pulse Width	5	t_{WSL}	200		ns

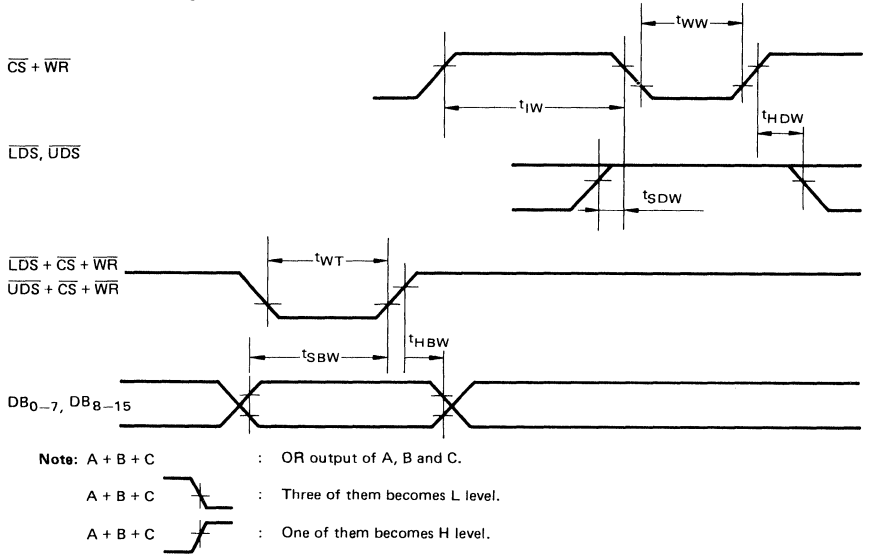
($DG = AG = 0V$, $V_{DD} = 5V$, $V_{SS} = -5V$, $f_{MCLK} = 720kHz$, $V_{RI} = 2.5V$, $T_A = 25°C$)

Parameter	Fig.	Symbol	Min	Max	Unit
MSB Output Delay Time	5	t_{DOK}	0	500	ns
Serial Output Delay Time	5	t_{DOT}	0	150	ns
MSB Input Setup Time	5	t_{SIR}	50		ns
MSB Input Hold Time	5	t_{HIR}	50		ns
Serial Input Setup Time	5	t_{SIT}	50		ns
Serial Input Hold Time	5	t_{HIT}	50		ns
STRT Output Delay Time	6	t_{DSK}	0	300	ns
Analog Input Setup Time	6	t_{SA}	1.2		μs
Analog Input Hold Time	6	t_{HA}	0		ns
Command Setup Time for $\overline{IRQ}$ = Low	6	t_{SCK}	200		ns
$\overline{IRQ}$ Falling Delay Time	6	t_{DIK}	0	200	ns
$\overline{IRQ}$ Rising Delay Time (Pull-up Resistance = 5kΩ, C_L = 10pF)	6	t_{DIC}	0	200	ns
Analog Output Settling Time	6	t_{DA}	0	8	μs
Valid Output Hold Time	6	t_{AE}		500	μs
$\overline{CS}$ Setup Time for Reset Completion	7	t_{SRES}	500		ns
$\overline{CS}$ Hold Time for Reset Completion	7	t_{HRES}	20		clock cycle
Reset Pulse Width	7	t_{WRES}	500		ns
PD Setup Time	8	t_{SPK}	100		ns
PD Hold Time	8	t_{HPK}	500		ns
MODE Setup Time	8	t_{SMK}	100		ns
MODE Hold Time	8	t_{HMK}	500		ns
Power Down Time from Conversion Completion	9	t_{PDK}		1	ms
Power Down Time from PD	9	t_{PDP}		1	ms
Power Up Time	9	t_{PUP}		10	ms

TIMMING DIAGRAM

PARALLE TRANSMISSION

Fig. 1 – WRITE CYCLE TIMING-1 (DATA TRANSMISSION)

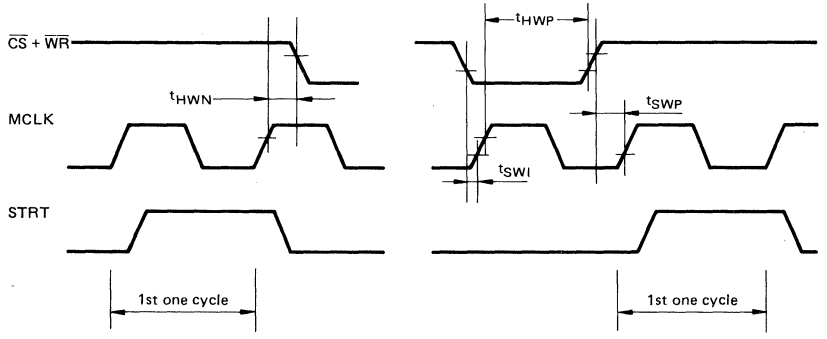


Note: A + B + C : OR output of A, B and C.

A + B + C : Three of them becomes L level.

A + B + C : One of them becomes H level.

Fig. 2 – WRITE CYCLE TIMING-2 (CONVERSION START)



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PARALLE TRANSMISSION

Fig. 3 – READ CYCLE TIMING-1 (DATA TRANSMISSION)

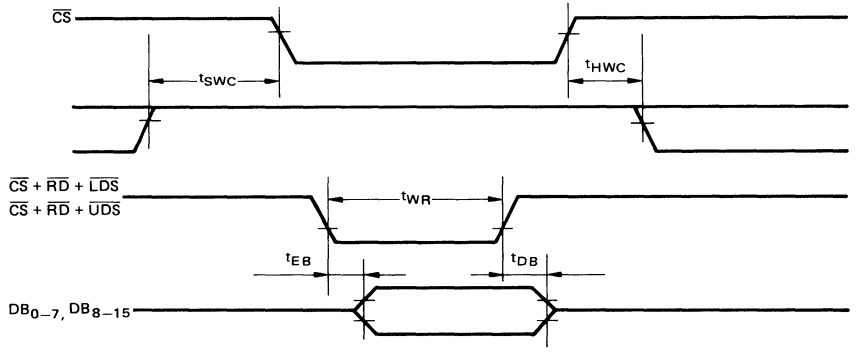
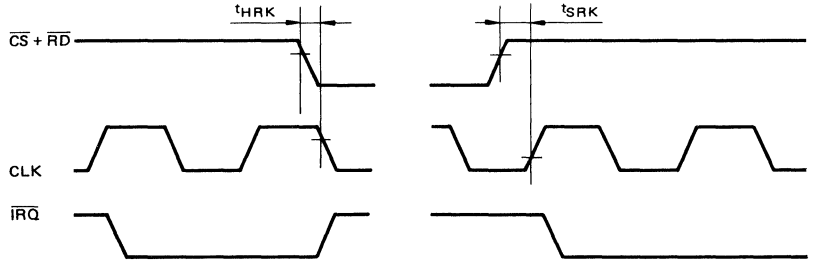


Fig. 4 – READ CYCLE TIMING-2 (CONVERSION START)

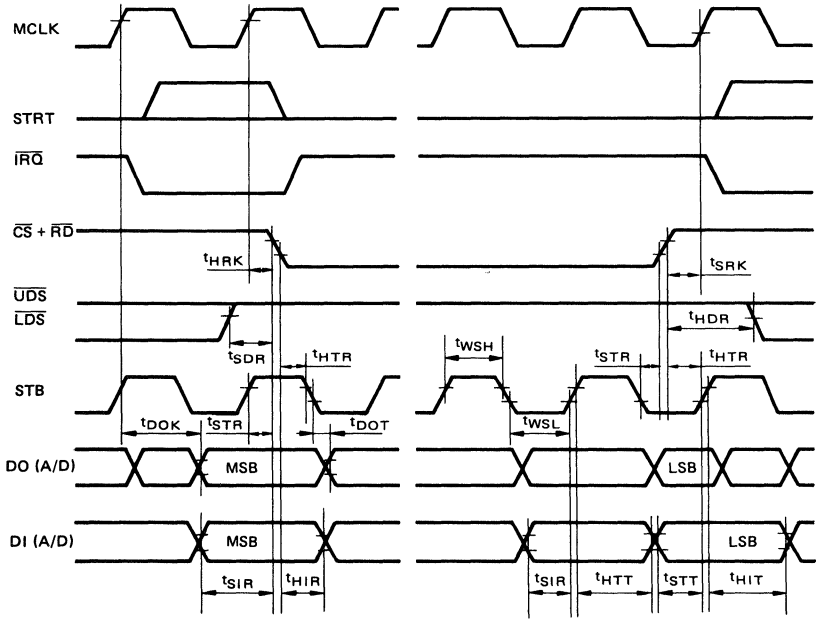


Note: Except for serial transmission mode, t_{HRK}, t_{SRK} specification is necessary to read out normally. Unless these spec are specified, the data will not destroy.

TIMMING DIAGRAM (continued)

SERIAL TRANSMISSION

Fig. 5 – SERIAL INPUT/OUTPUT



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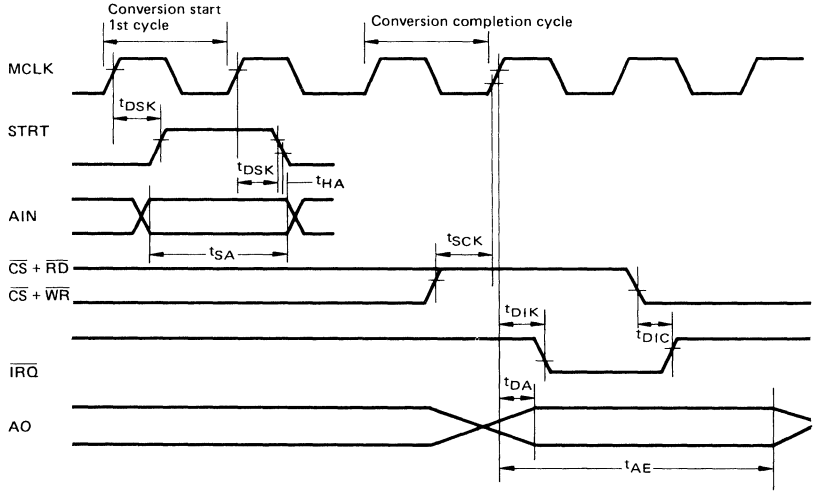
OTHER TIMING

Fig. 6 – STRT, IRQ, AIN, PO TIMING



Note: t_{SCX} is necessary condition that $\overline{IRQ}$ becomes L. However, if this condition is not satisfy, operation has no effect.

TIMMING DIAGRAM (continued)

Fig. 7 – POWER ON/REST TIMING

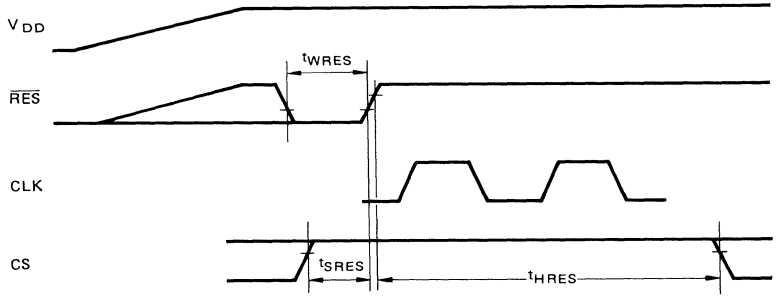


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Fig. 8 – MODE CHANGING TIMING

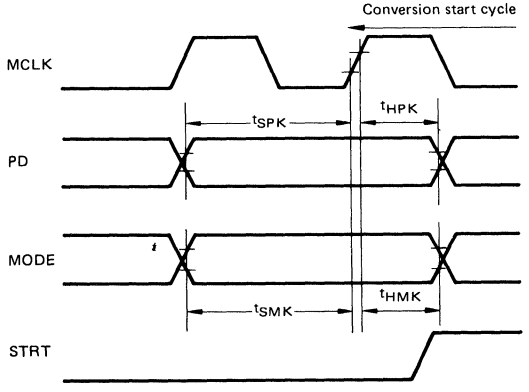
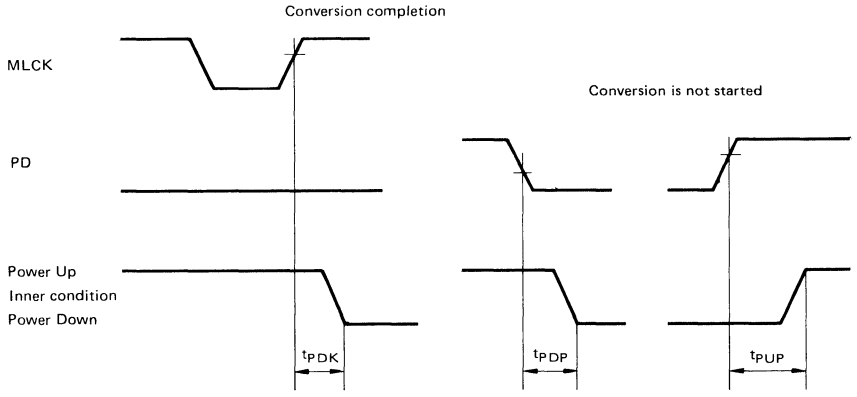


Fig. 9 – POWER DOWN TIMING



OPERATING TIMING

Fig. 10 – D/A, 8-BIT MICROPROCESSOR

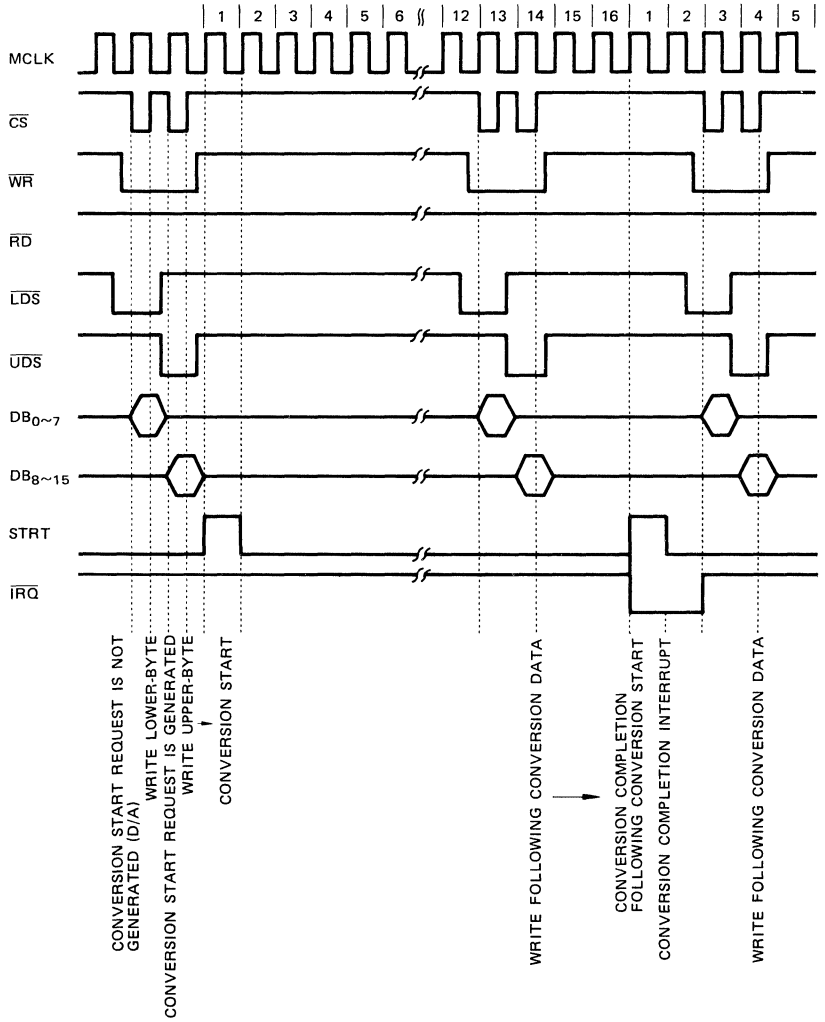


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Fig. 11 – A/D 16BIT MICRO PROSESSOR

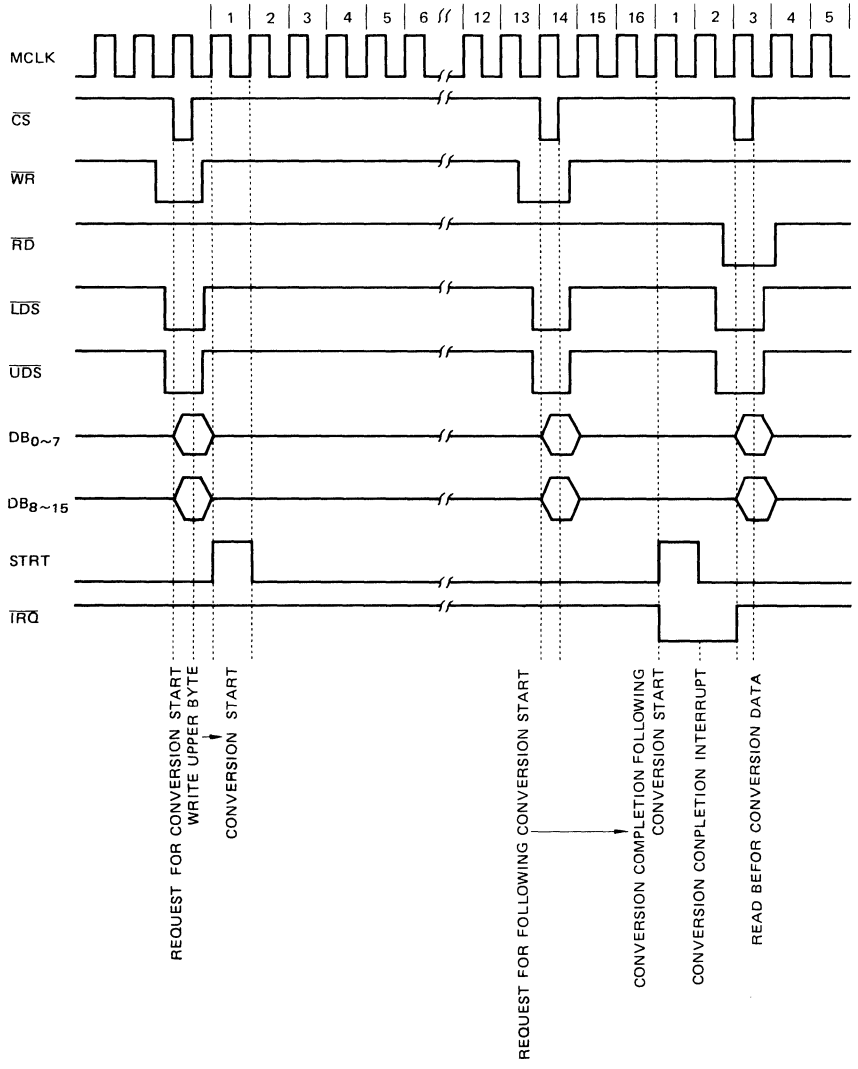

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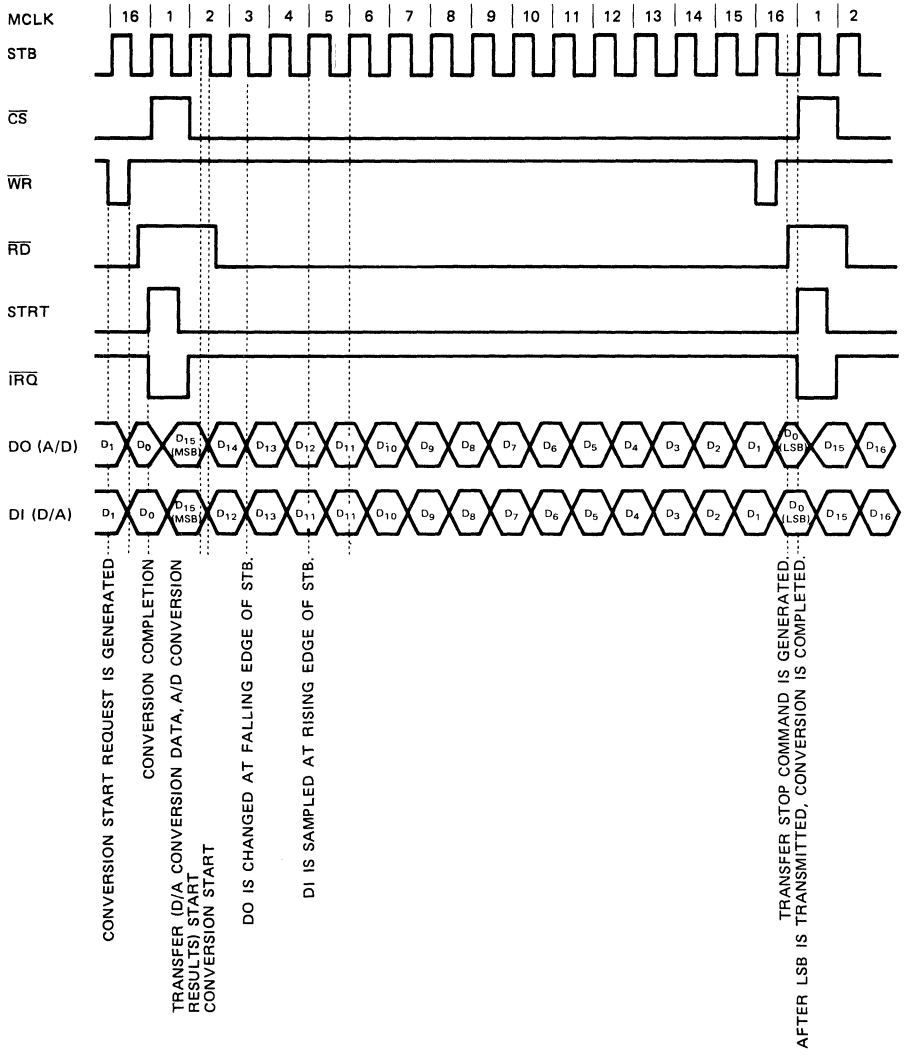
Fig. 12 – A/D, SERIAL OUTPUT OR D/A, SERIAL INPUT



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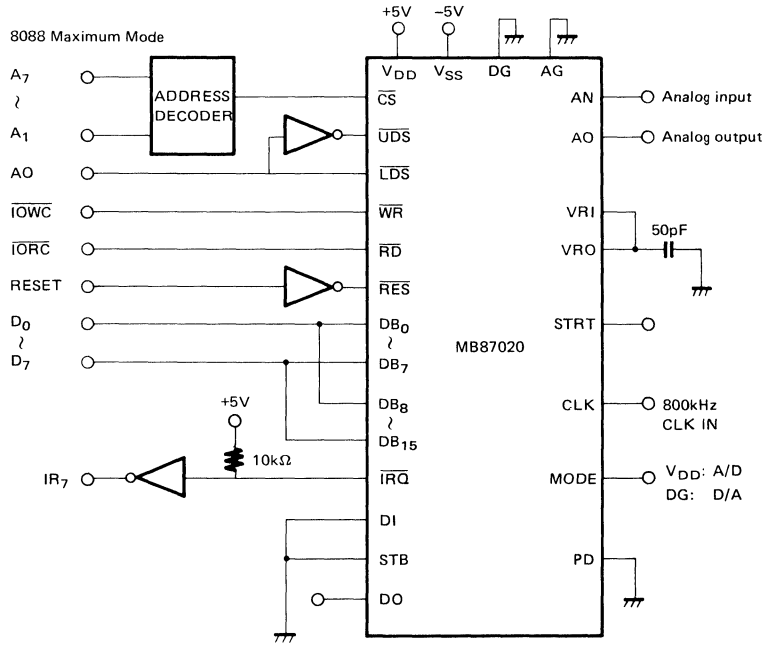
INTERFACE CIRCUIT EXAMPLE

Fig. 13 – INTERFACE WITH 8088 MAXIMUM MODE



Note: When $\overline{LDS}$ is low, even byte is stored in lower I/O register.
When $\overline{UDS}$ is low, odd byte is stored in high I/O register.
Interruption is used as the hight priority.
Conversion range is between –2.5V and +2.5V.
The data stored in AX register are D/A converted by OUT command.

7

INTERFACE EXAMPLE WITH VARIOUS INTERFACE

Object		Control Signal	Example of main input control pin of MB87020						
			DB_0 to DB_7	DB8 to DB_{15}	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	$\overline{UDS}$	$\overline{LDS}$
MP	Z80 (80 series 8-bit CPU)	$\overline{WR}$, $\overline{RD}$, D_0 to D_7, A_0 to A_{15}	D_0 to D_7	D_0 to D_7	Address decoder output	$\overline{WR}$	$\overline{RD}$	Inverted output of A	AO
	6800 (68 series 16-bit CPU)	R/$\overline{W}$, VMA, $\phi 2$, D_0 to D_7, A_0 to A_{15}	D_0 to D_7	D_0 to D_7	***	R/$\overline{W}$	Inverted output of R/$\overline{W}$	Inverted output of A	AO
	8086 (86 series 16-bit CPU)	$\overline{MWTC}$, $\overline{MRDC}$, D_0 to D_{15}, A_0 to A_{19}	D_0 to D_7	D_8 to D_{15}	Address decoder output	$\overline{MWTC}$	$\overline{MRDC}$	$\overline{BHE}$	AO
	68000 (68000 series 16-bit CPU)	R/$\overline{W}$, AS, $\overline{LDS}$, $\overline{UDS}$, A_0 to A_{23}	D_0 to D_7	D_8 to D_{15}	****	R/$\overline{W}$	Inverted output of R/$\overline{W}$	$\overline{UDS}$	$\overline{LDS}$
D/A conversion only, D_0 to D_{15} (Parallel data), Conversion start request signal ST (Low active)			D_0 to D_7	D_8 to D_{15}	L	$\overline{ST}$	H	L	L
A/D conversion only, Conversion start request signal ST (Low active) D_0 to D_{15} (Parallel data request)			D_0 to D_7	D_8 to D_{15}	L	$\overline{ST}$	L	L	L
A/D or D/A serial conversion transmission BUSY (Low active) Conversion start request signal ST (Low active)			L or H	L or H	L	$\overline{ST}$	$\overline{BUSY}$	H	H
MB87064 (Fujitsu 16-bit DSP)		$\overline{BCT}$, $\overline{ACT}$, D_0 to D_{15}	D_0 to D_7	D_8 to D_{15}	L	$\overline{BCT}$	$\overline{ACT}$	L	L

*** Address decoder output after VMA, ϕ_2 gate
**** Address decoder output after AS gate

7

TEST CIRCUIT

Fig. 14 – TEST CIRCUIT FOR DISTORTION RATIO (1)

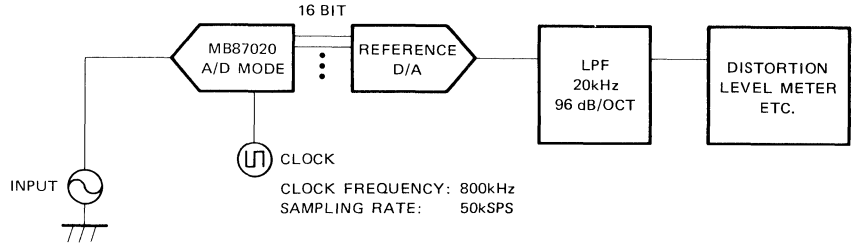


Fig. 15 – TEST CIRCUIT FOR DISTORTION RATIO (2)

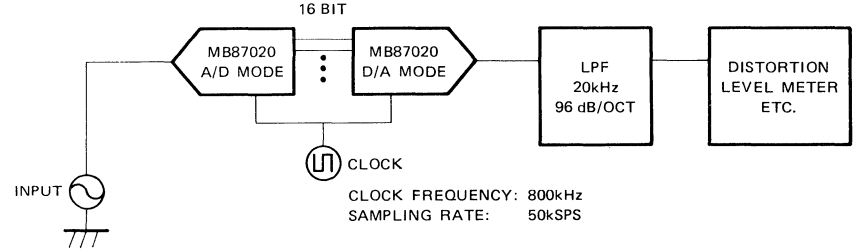
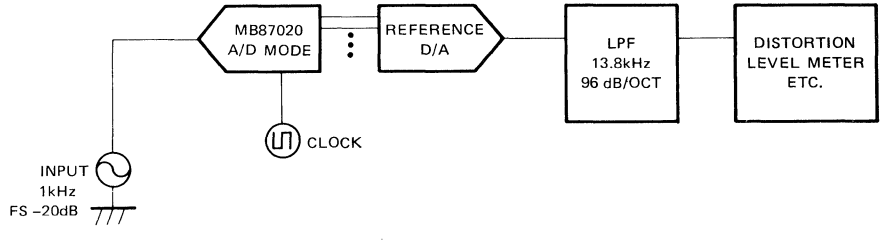


Fig. 16 – TEST CIRCUIT FOR DISTORTION RATIO (3)



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TEST CIRCUIT (continued)

Fig. 17 – TEST CIRCUIT FOR DISTORTION RATIO (4)

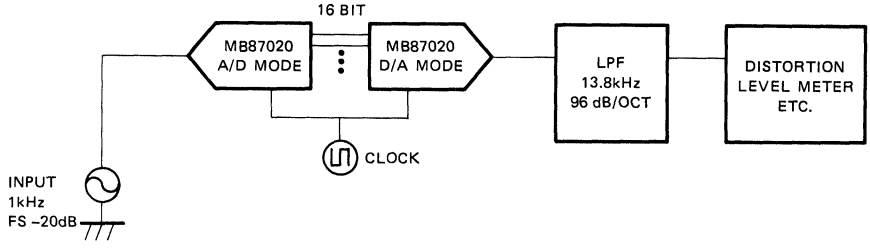

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Fig. 18 – TEST CIRCUIT FOR ABSOLUTE GAIN

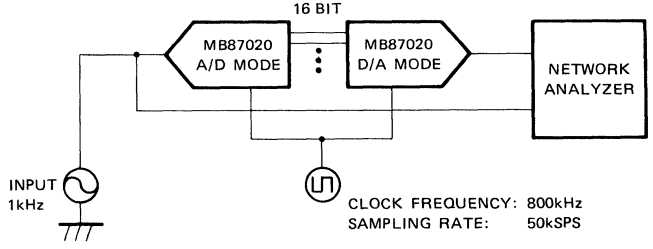

Fig. 19 – TEST CIRCUIT FOR FREQUENCY CHARACTERISTICS (1)

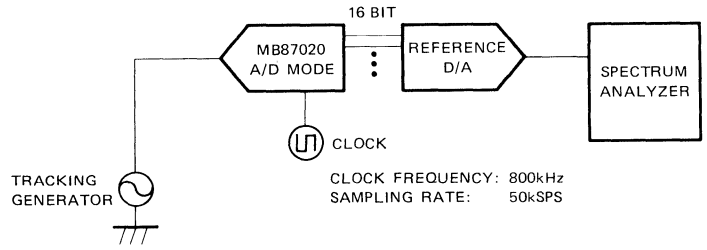

Fig. 20 – TEST CIRCUIT FOR FREQUENCY CHARACTERISTICS (2)

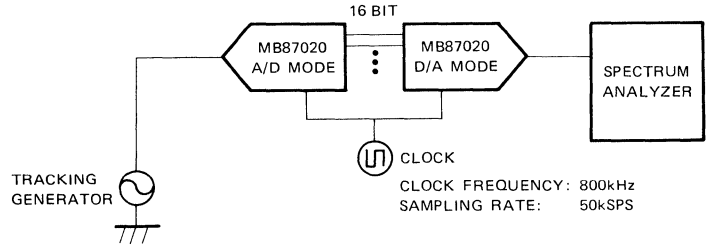

Fig. 21 – SIGNAL LEVEL OF ADC MODE vs. DISTORTION RATIO

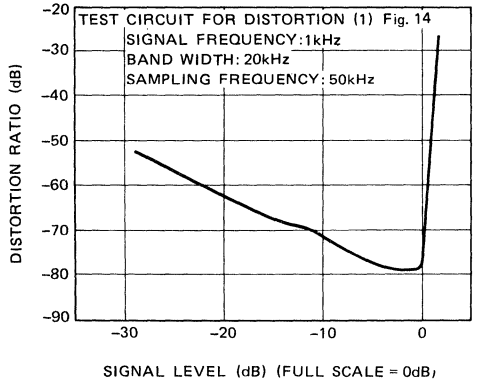

Fig. 22 – SIGNAL LEVEL OF DAC MODE vs. DISTORTION RATIO

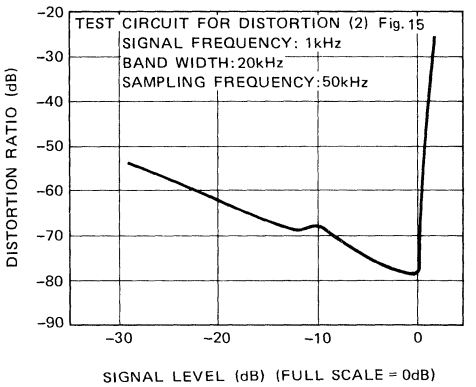

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Fig. 23 – SIGNAL FREQENCY vs. DISTORTION RATIO

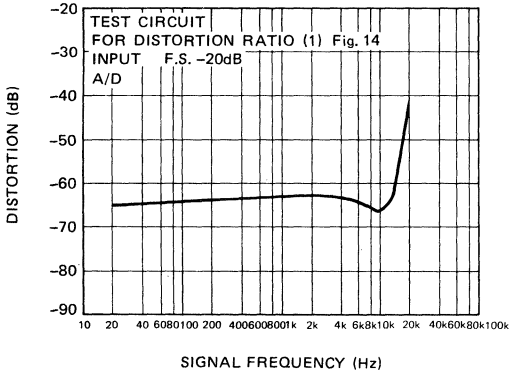

Fig. 24 – SIGNAL FREQUENCY vs. DISTORTION

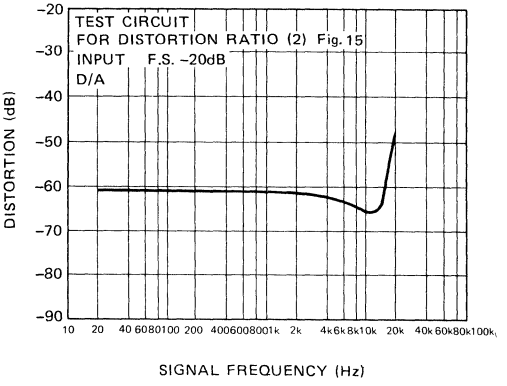

Fig. 25 – TEMPERATURE vs. DISTORTION RATIO (A/D MODE)

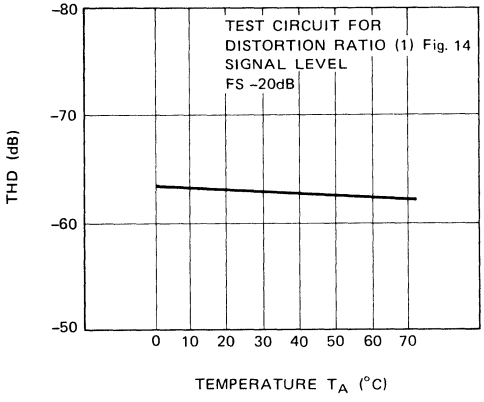

Fig.26 – TEMPERATURE vs. DISTORTION RATIO (D/A MODE)

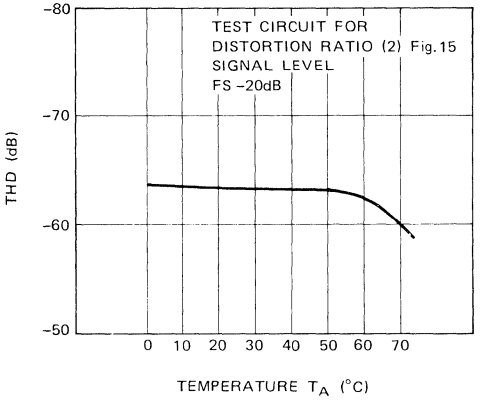

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Fig. 27 – SAMPLING FREQUENCY vs. DISTORTION RATIO

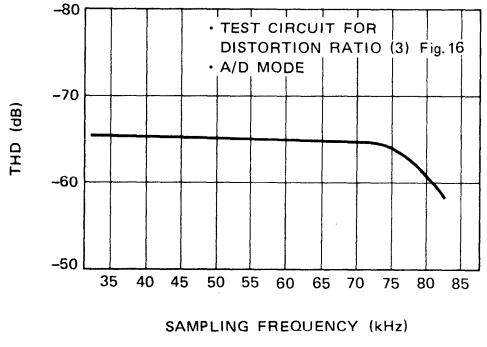


Fig. 28 – SAMPLING FREQUENCY vs. DISTORTION RATIO

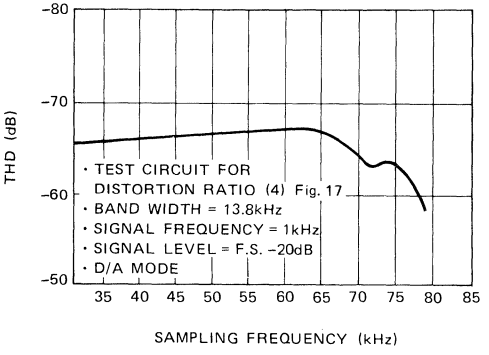
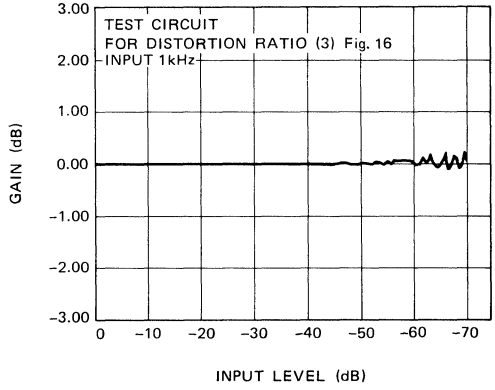


Fig. 29 – INPUT LEVEL vs. GAIN



7

Fig. 30 – SIGNAL FREQUENCY vs. GAIN

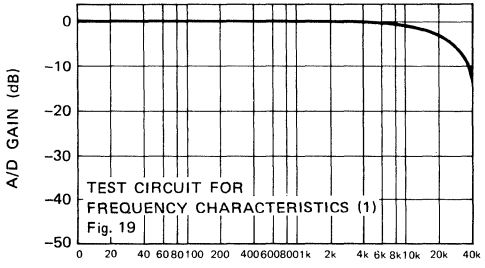
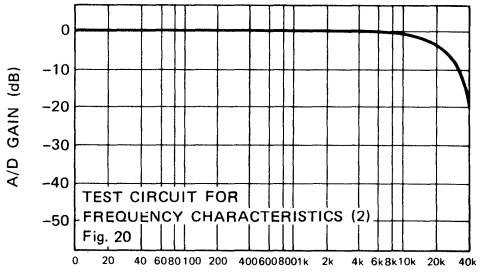
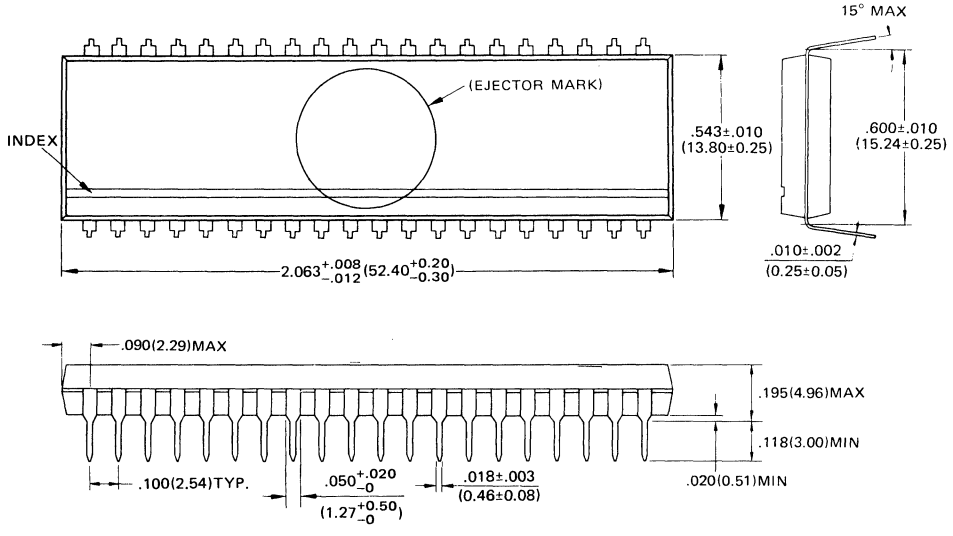


Fig.31 – SIGNAL FREQUENCY vs. GAIN



PACKAGE DIMENSIONS

40-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-40P-M01)



Dimensions in
inches (millimeters)

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FUJITSU

FREQUENCY-TO- VOLTAGE CONVERTER

MB4206

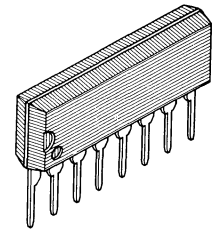
September 1987
Edition 1.0

FREQUENCY-TO-VOLTAGE CONVERTER

The Fujitsu MB4206 is a frequency-to-voltage converter with an on-chip comparator. The MB4206 uses a charge pump driven by a positive-edge Schmitt trigger/flip-flop input so stable operation is achieved against noise signal input. The output of the comparator is zener-clamped to a reference voltage; thus, a precise hysteresis output is obtained. The overall design makes the circuit fairly tolerant of imperfections in the input waveform.

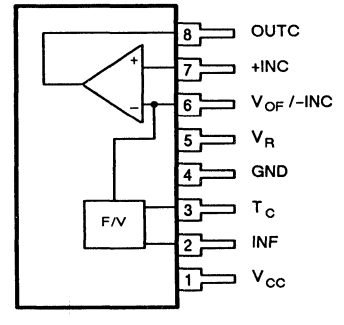
The MB4206 is housed in an 8-pin single inline package (SIP).

- Conversion coefficient determined by RC pair:
  $V_{OF} = F_{IN} \cdot R_T \cdot C_T \cdot V_R$
- Positive edge-triggered frequency input
- Equal internal reference generator high-level ouput and comparator high level output



PLASTIC PACKAGE
(SIP-08P-M03)

PIN ASSIGNMENTS



(Front View)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS (see NOTE)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	24	V
Surge Voltage at VCC	V_{CCS}	40 ($t \leq 50$ ms)	V
Zener Current	I_Z	20	mA
Power Dissipation	P_D	300 ($T_A \leq 85$ °C)	mW
Operating Temperature	T_A	-30 to +85	°C
Storage Temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Fig. 1 — MB4206 BLOCK DIAGRAM

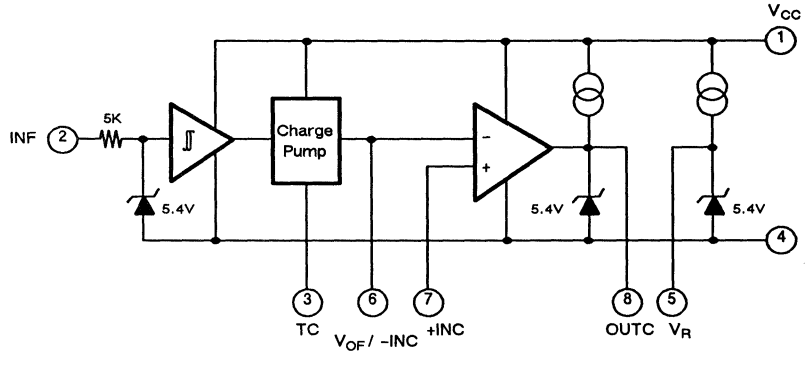
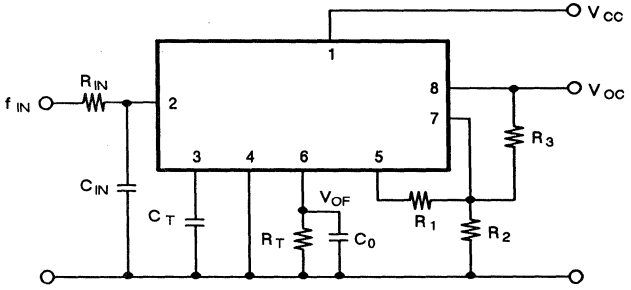
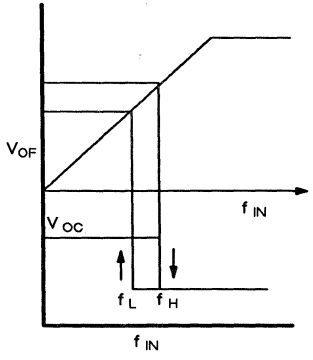


FIG. 2 — TYPICAL HOOKUP AND OPERATING PARAMETERS





The following equations define the operating frequency of the comparator.

$$f_H \cong \frac{1}{C_T R_T} \cdot \frac{R_2}{R_2 + \frac{R_1 R_3}{R_1 + R_3}}$$

$$f_L \cong \frac{1}{C_T R_T} \cdot \frac{R_2 R_3}{R_1 R_2 + R_1 R_3 + R_2 R_3}$$

R_{IN} and C_{IN} are needed when input noise is excessive.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 12V)

Parameter	Symbol	Condition	Values			Unit
			Min	Typ	Max	
Power Supplies						
Power Supply Current	I_{CC}	—	—	7.0	10.0	mA
Power Supply Voltage	V_{CC}	—	6.5	—	24	V
Reference Voltage	V_R	I_{LR} = 1mA	5.0	5.4	5.8	V
Reference Voltage Temperature Coefficient	—	I_{LR} = 1mA	—	+1.4	—	mV/°C
F/V Converter						
Input High Voltage	V_{IH}	—	2.4	—	24	V
Input Low Voltage	V_{IL}	—	0	—	1.2	V
Positive-edge	—	—	1	—	—	V/ms
Negative-edge	—	—	0.1	—	—	V/ms
Input Current	I_I	V_{IHF} = 24V	—	4	8	mA
		V_{ILF} = 1.2V	—	—	0.1	mA
Output Current	I_O	V_{TC} = 2.5V	0.26	0.4	0.58	mA
F/V Coefficient [1]	K	C_T = 0.1 μF, R_T= 47kΩ, f = 100Hz	0.9	1.0	1.1	—
Linearity [2]	—	C_T = 0.1 μF, R_T= 47kΩ	—	±0.3	—	%
Comparator						
Input Offset Voltage [3]	V_{IO}	—	—	2.0	10	mV
Input Bias Current [4]	I_I	—	—	0.5	3	μA
Common Mode Input Voltage	V_{ICM}	—	0	—	V_R	V
Voltage Gain	A_V	R_L =10kΩ	—	100	—	dB
Output Voltage	V_{OL}	I_{SINK} = 3mA	—	0.1	0.2	V
	V_{OH}	I_L = 0.5mA	5.0	5.4	5.8	V
Sink Current	I_{SINK}	V_{OL} ≥1V	8	22	—	mA

NOTES 1. $V_{OF} = K \cdot V_R \cdot C_T \cdot R_T \cdot f$

2. With f_{IN}= 100Hz as a reference, linearity is defined as the straight-line deviation over an input frequency range of 50 - to - 150 Hz — see TYPICAL PERFORMANCE CHARACTERISTICS.

3. The current flows from IC.

4. If V_{CC} is lower than V_R, use (V_{CC}-2).

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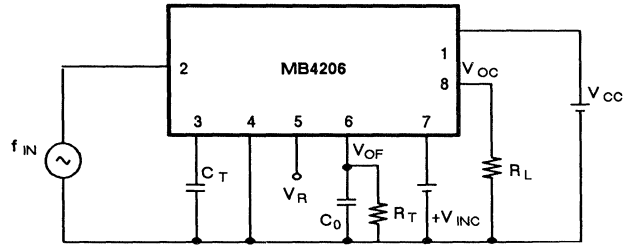
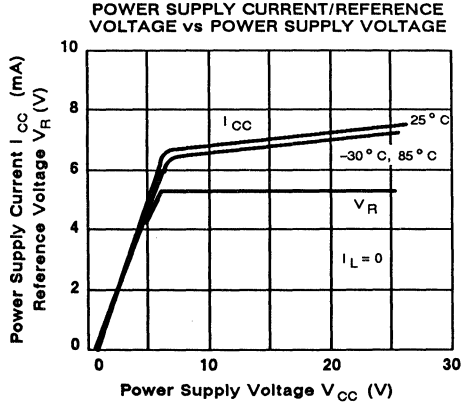
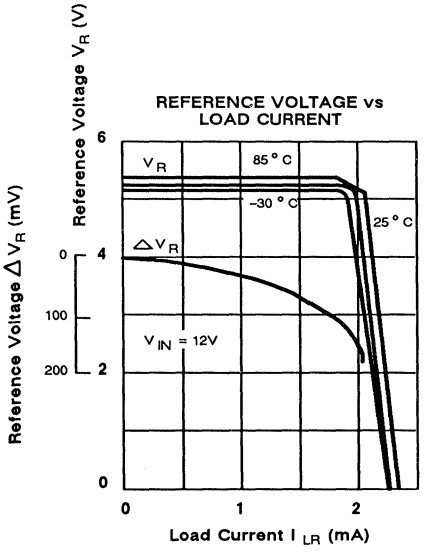
Fig. 3 — TEST CIRCUIT



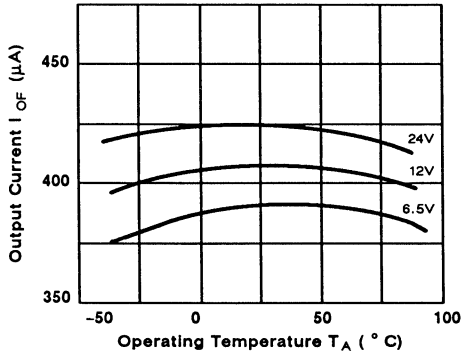
TYPICAL PERFORMANCE CHARACTERISTICS



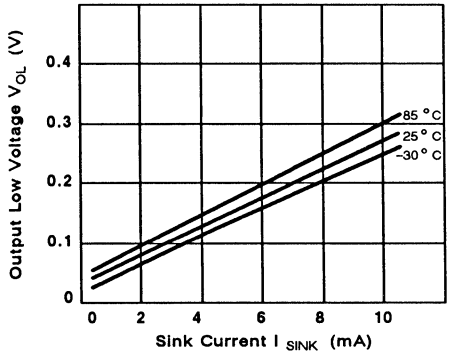


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

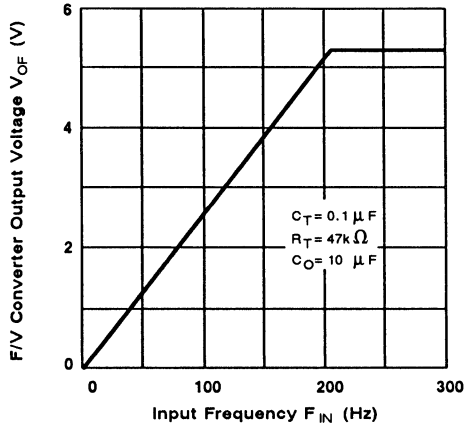
OUTPUT CURRENT vs OPERATING TEMPERATURE



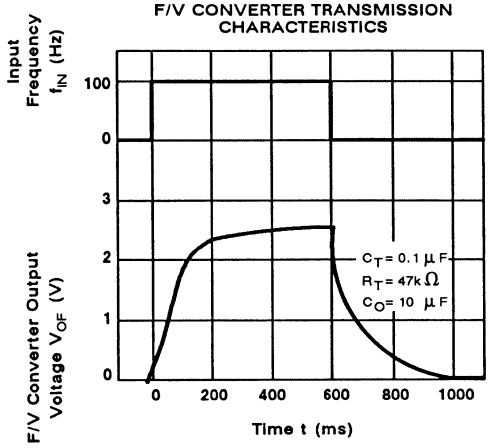
OUTPUT LOW VOLTAGE vs SINK CURRENT



F/V CONVERTER OUTPUT VOLTAGE vs INPUT FREQUENCY



F/V CONVERTER TRANSMISSION CHARACTERISTICS



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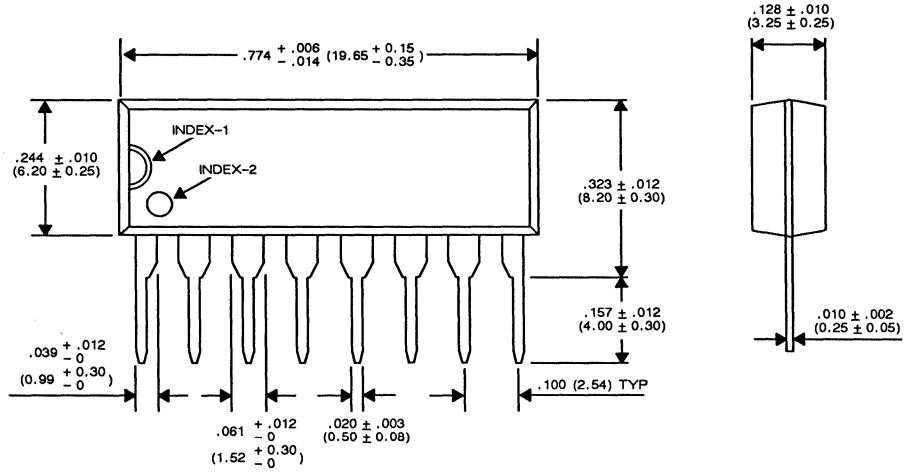
PACKAGE DIMENSIONS

8-LEAD PLASTIC SINGLE-IN-LINE PACKAGE
(CASE No.: SIP-08P-M03)



Dimensions in
inches (millimeters)

S08010S-2C

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April 1990
Edition 1.0

FUJITSU

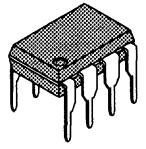
PRODUCT PROFILE

MB4207
Frequency-to-Voltage Converter

DESCRIPTION

The Fujitsu MB4207 is a single power supply frequency-to-voltage converter with a comparator. The MB4207 can stabilize a noisy signal using the charge pump driven by a Schmitt trigger and flip-flop circuit.

The comparator provides precise hysteresis output due to clamping at the reference voltage with Zener diode.



DIP-8P-M01

FEATURES

- An RC pair provides the coefficient of conversion:

$$V_O = \frac{2}{3} \cdot V_Z \cdot C_T \cdot R_T \cdot f_{IN}$$

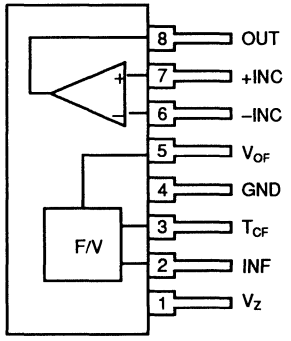
- Output is clamped at the built-in reference voltage (High-level).
- Positive-edge trigger frequency input.

ABSOLUTE MAXIMUM RATING (T_A = 25°C)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	24[1]	V
Surge Voltage at V_{CC}	V_{CCS}	100[2]	V
Zener Current	I_Z	30	mA
Power Dissipation	P_D	300[3]	mW
Operating Temperature	T_{OP}	−30 to +85	°C
Storage Temperature	T_{STG}	−55 to +125	°C

Notes: [1] R_s = 680 Ω
[2] t < 50 msec, R_s = 680 Ω
[3] T_A<85°C

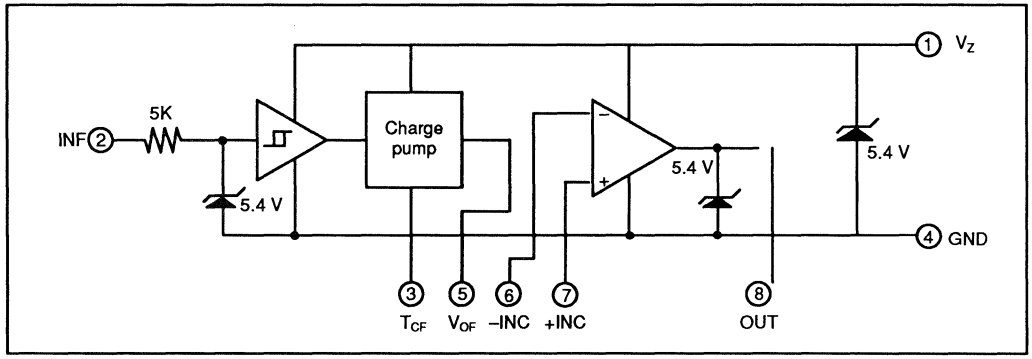
Pin Assignment (Front View)



Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

BLOCK DIAGRAM



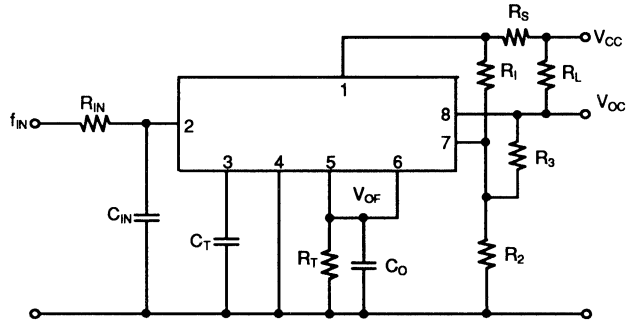
ELECTRICAL CHARACTERISTICS

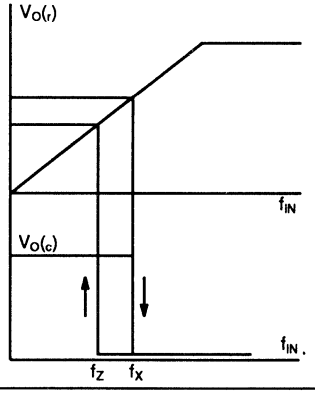
(T_A = 25 °C, V_{CC} = 12V, R_S = 680Ω)

	Parameter	Conditions	Symbol	Value Min.	Value Typ.	Value Max.	Unit
	Supply Current	R_S=0Ω, V_{CC}=4.8V	I_{CC}	–	3.0	5.0	mA
	Reference Voltage	See Figure 1	V_Z	5.0	5.4	5.8	V
		V_{CC} = 10 to 16 V	ΔV_Z	—	0.05	0.1	V
V/F CONVERTER	Input High Level		V_{IH}	2.4	–	24	V
	Input Low Level		V_{IL}	0	–	1.2	V
	Positive-edge			1	–	–	V/ms
	Negative-edge			0.1	–	–	V/ms
	Input Current	V_{IHF} = 24 V V_{ILF} = 1.2 V	I_{INF}	— —	4 —	8 0.1	mA mA
	Output Current	V_{TCF} = 2.5 V	I_{OF}	0.26	0.4	0.58	mA
	F/V Coefficient	C_T = 0.1 µF, R_T = 47k Ω f = 100 Hz	K[1]	0.9	1.0	1.1	
	Linearity Error	V_T = 0.1 µF, R_T = 47k Ω[2]		–	±0.3	–	%
COMPARATOR	Input Offset Voltage		V_{IOC}	–	2	10	mA
	Input Bias Current	(See Note[3])	I_{IBC}	–	0.5	3	µA
	Common Mode Input Voltage		V_{CM}	0	–	3	V
	Voltage Gain	R_L = 10k Ω	A_V	–	100	–	dB
	Output Voltage	I_{SINK} = 3 mA	V_{OLC}	–	0.1	0.2	V
		I_L = 0.5 mA	V_{OLC}	5.0	5.4	5.8	V
	Sink Current	V_{OLC}<1 V	I_{SINK}	8	20	–	mA

Notes: [1]$V_O = (2/3) \cdot K \cdot V_Z \cdot C_T \cdot R_T \cdot f_{IN}$
[2]At 50/100 Hz on the basis at 100 Hz.
[3]The current flows outward from the IC.

APPLICATION EXAMPLE





Operating frequency of the comparator is provided by the following equations.

$$f_X \approx \frac{3}{2C_TR_T} \cdot \frac{R_Z}{R_2 + R_I /\!/ R_3}$$

$$f_Z \approx \frac{3}{2C_TR_T} \cdot \frac{R_2 /\!/ R_3}{R_I + R_2 /\!/ R_3}$$

R_{IN} and C_{IN} are needed when the input has chattering noise.

7

TYPICAL CHARACTERISTIC CURVES

Figure 1. Supply Current/Reference Voltage vs. Supply Voltage

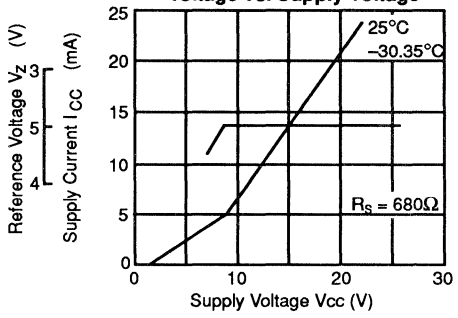


Figure 2. Output Current vs. Ambient Temperature

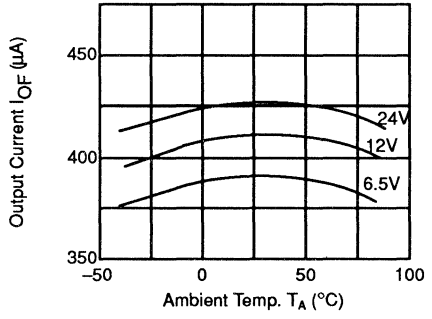
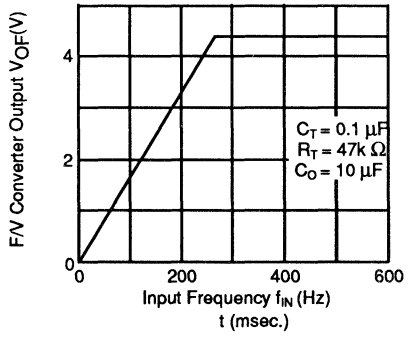


Figure 3. F/V Converter Output Voltage vs. Input Frequency



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TYPICAL CHARACTERISTIC CURVES (Continued)

Figure 4. Zener Current vs. Reference Voltage

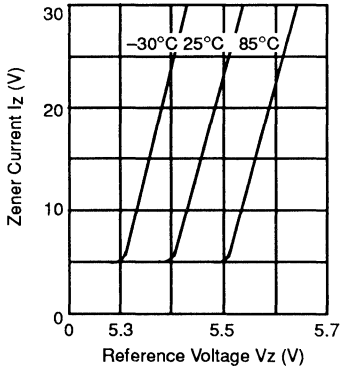


Figure 5. Low-Level Output Voltage vs. Sink Current

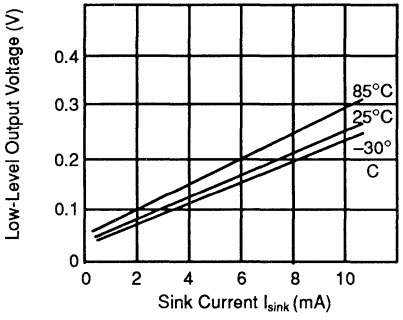
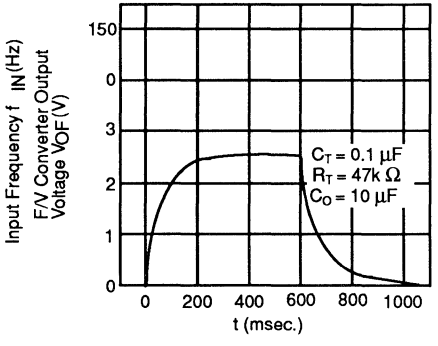


Figure 6. F/V Converter Transition Characteristics



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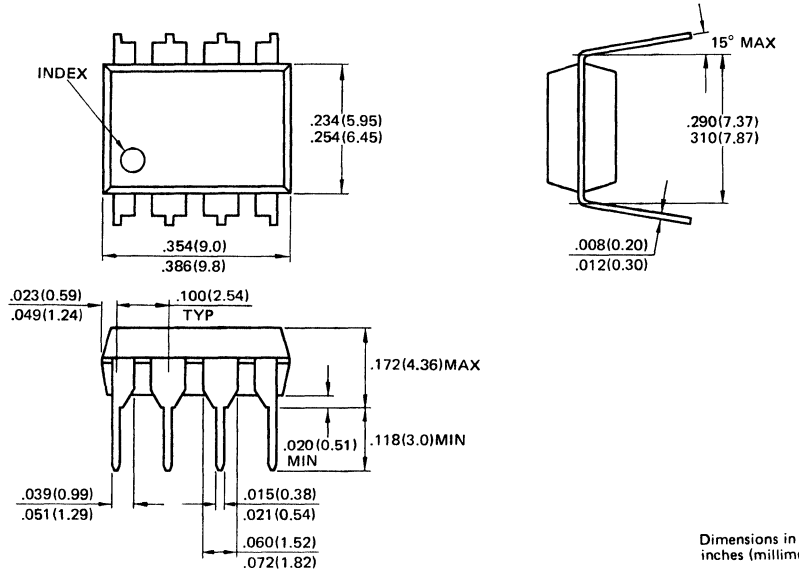
PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL IN-LINE PACKAGE
(Case No.: DIP-08-M01)



Dimensions in inches (millimeters)

7

Section 8

Other Linear Products — *At a Glance*

Page	Device	Description	Features	Power Supply (V)	Package Options
8–3	MB3501	Wide Band Video Amplifier	Adjustable gain from 10 to 400	±6 V	14-pin Plastic DIP, FPT
8–11	MB4210	Lamp Detector for Automobiles	Precise Comparator and Voltage Reference Units	+1.6 to +4.5	8-pin Plastic SIP
8–15	MB4214	Timer	Two pair of Comparators On-chip	+4.5 to +16	17-pin Plastic ZIP
8–27	MB47201	Quad SPST Analog Switch	Bipolar Technology CMOS and TTL Compatible		16-pin Plastic DIP, FPT

FUJITSU

WIDE BAND VIDEO AMPLIFIER

MB3501

July 1988
Edition 2.0

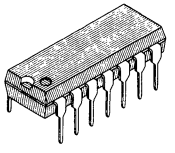
WIDE BAND VIDEO AMPLIFIER

The MB3501 is a monolithic differential input, differential output, wideband video amplifier. Owing to adoption of feedback circuitry, wide bandwidth and gain stability are achieved. Adjustable gain from 10 to 400 are obtained by external resistor without external frequency compensation.

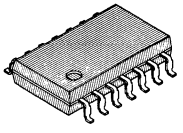
The MB3501 is most suitable for sense-amplifier of magnetic memory equipment, video amplifier and pulse amplifier.

The MB3501 is compatible with μA733.

- Supply Voltage: ±6V
- Wide Bandwidth: 150MHz
- Selectable Gain: 10 to 400
- Frequency Compensation is not required.
- 14-pin DIP Package (Suffix: -P)
  14-pin Flat Package (Suffix: -PF)

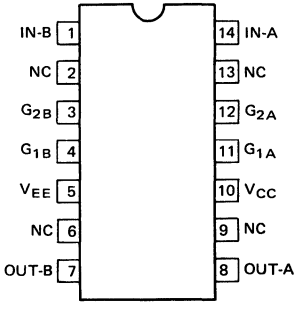


PLASTIC PACKAGE
DIP-14P-M02



PLASTIC PACKAGE
FPT-14P-M01

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (see NOTE)

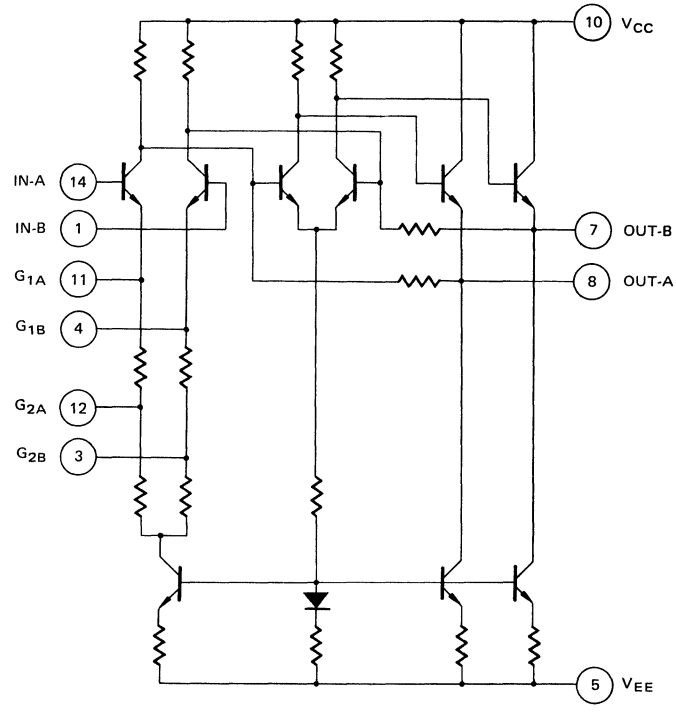
Rating	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	+8	V
Negative Supply Voltage	V_{EE}	−8	V
Input Voltage	V_{IN}	+1.5 to −5	V
Output Current	I_O	10	mA
Power Dissipation	P_D	500	mW
Storage Temperature	T_{STG}	−55 to +125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

8

Fig. 1 – MB3501 EQUIVALENT CIRCUIT



8

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Positive Supply Voltage	V_{CC}	+6±5%	V
Negative Supply Voltage	V_{EE}	−6±5%	V
Operating Temperature	T_A	−20 to +75	°C

DC CHARACTERISTICS

(V_{CC} = 6V, V_{EE} = –6V, T_A = 25°C)

Parameter	Symbol	Condition	Test Circuit	Value			Unit
				Min	Typ	Max	
Output Low Voltage	V_{OL}	ΔV_I = 200mV	Figs 2, 3		0.4	1.0	V
Output High Voltage	V_{OH}	ΔV_I = 200mV	Figs 2, 3	4.8	5.2		V
Output Voltage	V_O	*1	Fig. 4	1.6	2.7	3.9	V
Output Offset Voltage	V_{OFF}	*1	Fig. 4		0.35	1.4	V
Input Offset Current	I_{IO}		Fig. 4		0.4		μA
Input Bias Current	I_I		Fig. 4		9	30	μA
Output Sink Current	I_{SINK}	ΔV_I = 200mV			3.6		mA
Supply Current	I_{CC}	*1	Fig. 4		17	27	mA

AC CHARACTERISTICS

(V_{CC} = 6V, V_{EE} = –6V, T_A = 25°C)

Parameter	Symbol	Condition	Test Circuit	Value			Unit
				Min	Typ	Max	
Voltage Gain	AV_1	f = 1kHz, R_L = 1kΩ*2	Fig. 5	250	400	600	
	AV_2	f = 1kHz, R_L = 1kΩ*3	Fig. 5	80	100	120	
	AV_3	f = 1kHz, R_L = 1kΩ*4	Fig. 5	9	11	14	
Frequency Bandwidth	BW_1	R_S = 50Ω, R_L = 1kΩ*2	Fig. 6		50		MHz
	BW_2	R_S = 50Ω, R_L = 1kΩ*3	Fig. 6	80	110		MHz
	BW_3	R_S = 50Ω, R_L = 1kΩ*4	Fig. 6		150		MHz
Recovery Time	t_{REC}	R_S = 50Ω, R_L = 1kΩ, ΔV_I = 100mV			20		ns
Common Mode Gain	CMG	f ≤ 100kHz*3			-60		dB

Notes: *1 Inputs pins ground.
*2 Pins 4 and 11 connected together.
*3 Pins 3 and 12 connected together.
*4 Gain select pins open.

8

TEST CIRCUIT

Fig. 2 – V_{OL}, V_{OH}

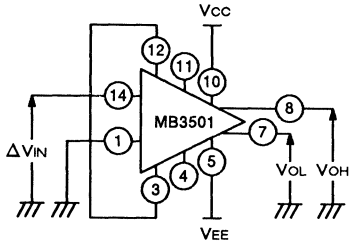


Fig. 3 – V_{OL}, V_{OH}

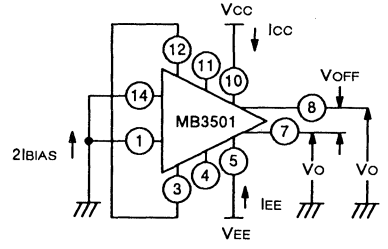


Fig. 4 – V_O, V_{OFF}, I_I

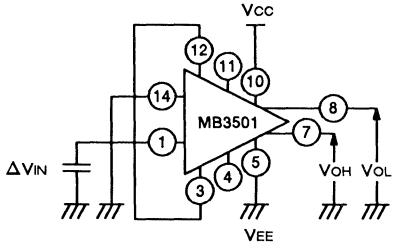


Fig. 5 – AV

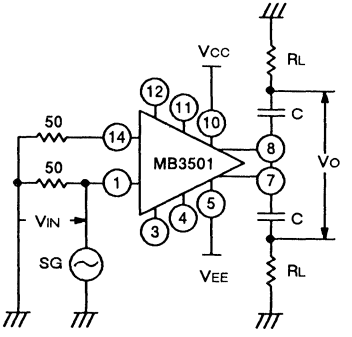
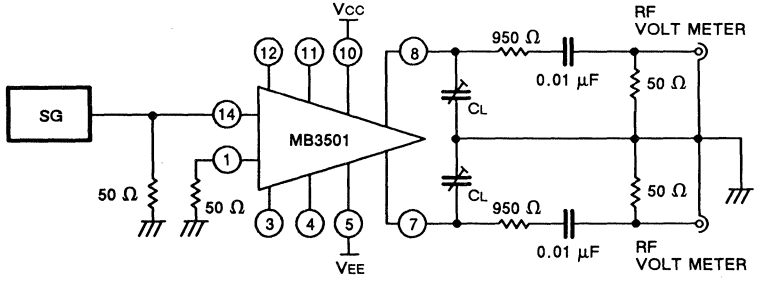


Fig. 6 – BW



8

TYPICAL CHARACTERISTICS CURVES

Fig. 7 – SINGLE VOLTAGE GAIN vs. FREQUENCY

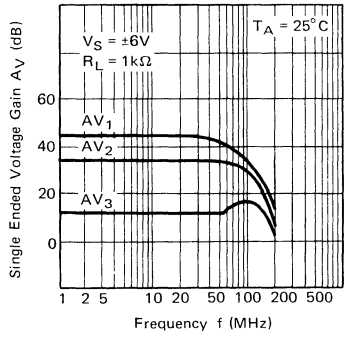


Fig. 8 – SINGLE ENDED VOLTAGE GAIN vs. FREQUENCY

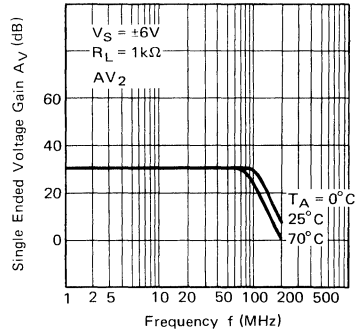


Fig. 9 – SINGLE ENDED VOLTAGE GAIN vs. FREQUENCY

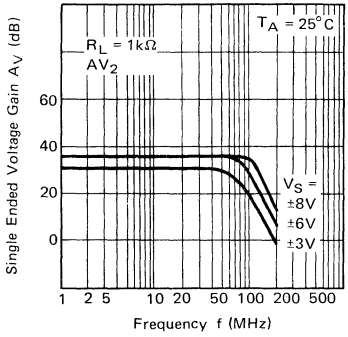


Fig. 10 – PHASE SHIFT vs. FREQUENCY

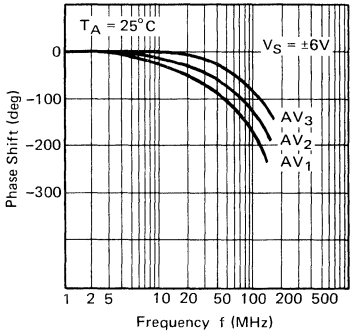


Fig. 11 – RECOVERY TIME vs. DIFFERENTIAL INPUT VOLTAGE

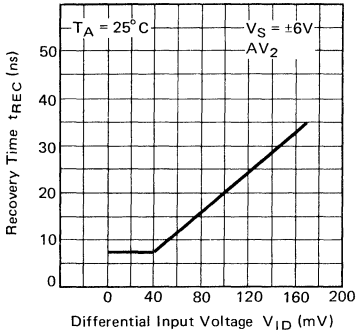
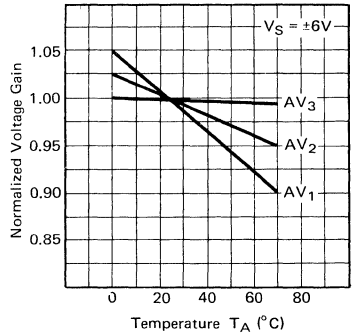


Fig. 12 – NORMALIZED VOLTAGE GAIN vs. TEMPERATURE



8

TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 13 – NORMALIZED VOLTAGE GAIN vs. SUPPLY VOLTAGE

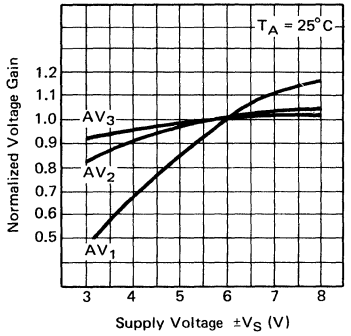


Fig. 14 – COMMON MODE GAIN vs. FREQUENCY

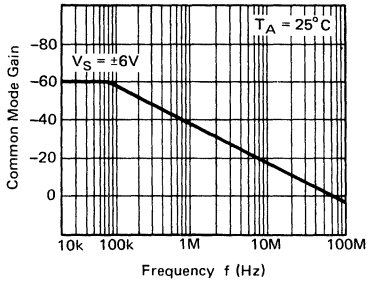
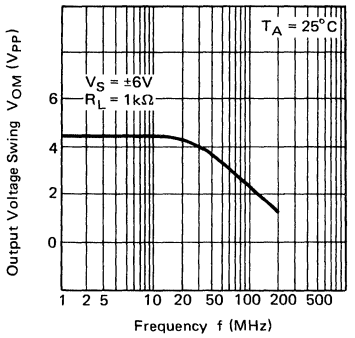


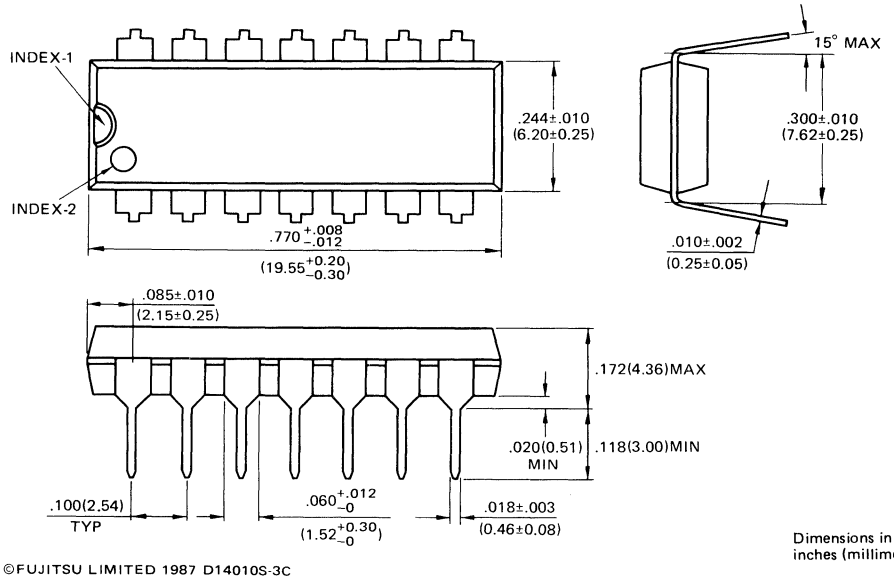
Fig. 15 – OUTPUT VOLTAGE SWING vs. FREQUENCY



8

PACKAGE DIMENSIONS

14-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-14P-M02)

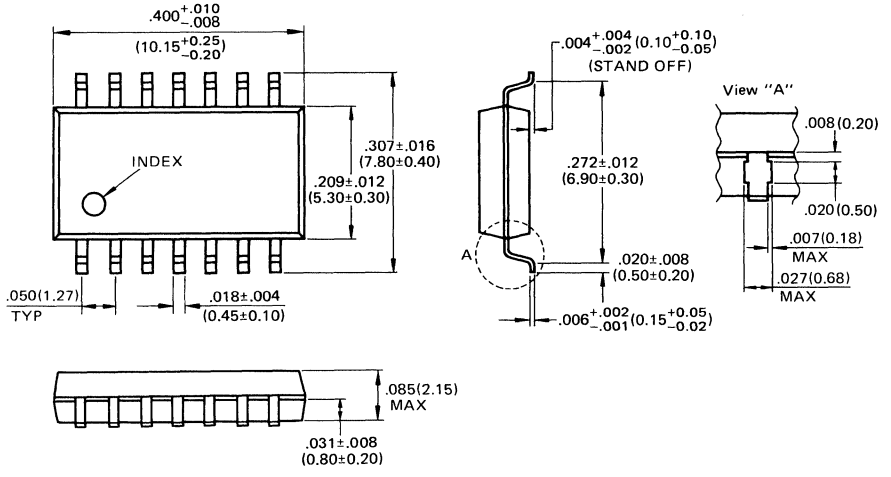


Dimensions in
inches (millimeters)

8

PACKAGE DIMENSIONS (continued)

14-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-14P-M01)



Dimensions in
inches (millimeters)

8

April 1990
Edition 1.0

FUJITSU

PRODUCT PROFILE

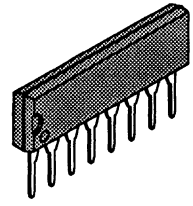
MB4210
Lamp Failure Detector for Automobiles

DESCRIPTION

The Fujitsu MB4210 is a bipolar integrated circuit designed for lamp failure systems in automobiles. Single lamp failure of two to four lamps can be detected because the MB4210 has a precise comparator and voltage reference circuits. The voltage reference has voltage characteristics similar to those of automobile lamps.

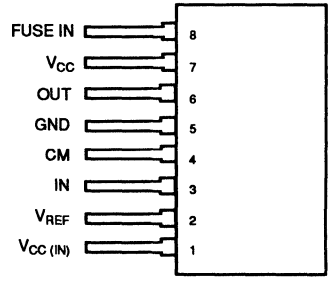
FEATURES

- Single lamp failure detection among 2 to 4 lamps
- Delay and memory by external condenser
- Fuse open detection
- High drive current for warning display
- Reference output
- Minimum Popcorn Noise



SIP-08-M03

Pin Assignment
(Front View)



ABSOLUTE MAXIMUM RATINGS

(T_a = 25°C)

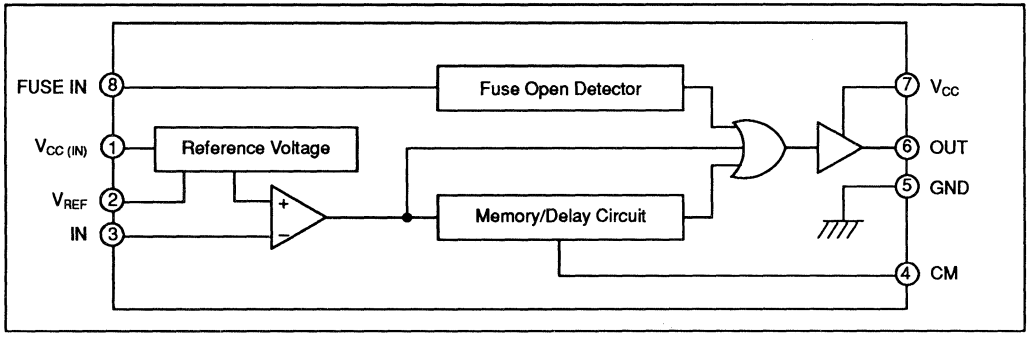
Item	Symbol	Typical Value	Unit
Operating Power Supply Voltage	$V_{CC\ (OP)}$	18	V
DC Power Supply Voltage	$V_{CC\ (DC)}$	24	
Power Supply Surge Current	$I_{CC\ (S)}$	200	mA
Input Surge Voltage	$V_{IN\ (S)}$	55	V
Output Current	I_{OL}	300	mA
Power Dissipation	P_D	420	mW
Operating Temperature	T_{OP}	−30 ~ +85	°C
Storage Temperature	T_{stg}	−55 ~ +150	

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

8

CIRCUIT BLOCK DIAGRAM



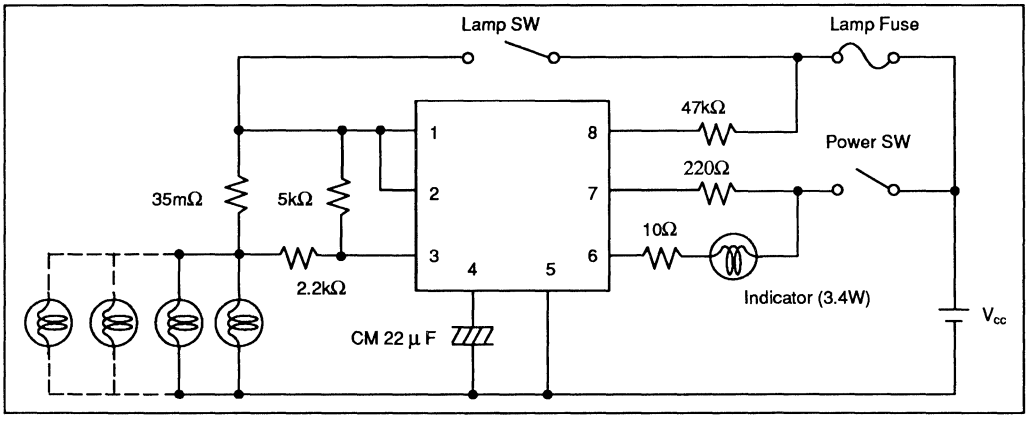
ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 13.2 V, R_L = 50 Ω, R_S = 220 Ω)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Power Supply Current	I_{CCO} I_{CCH}	V_{IF} = 0 V V_{CC} = 24 V, V_{IF} = 24 V		1.6 2.0	2.6 3.0	4.5 5.0	mA
Input Supply Current	$I_{CC(H)}$	V_{CC} = 24 V		1.6	2.4	4.0	
Input Bias Current	I_I	V_{IN} = $V_{CC(IN)}$ = 13.2 V		—	400	1000	nA
Input Offset Voltage	V_{IO}			—	2	4	mV
Voltage Reference	$V_{R(12)}$	$V_{CC(IN)}$ = 12 V		110	115	120	
	V_{RS}/V_{R12}	$V_{CC(IN)}$ = 8 V		0.775	0.815	0.855	
	V_{R16}/V_{R12}	$V_{CC(IN)}$ = 16 V		1.120	1.175	1.230	
Reference Resistance	R_R	I_R = 1 mA		250	400	550	Ω
Memory Start Time	T_{MS}	C_M = 1 µF		27	54	100	mS
Memory Hold Time	T_{MH}	V_{CC} = 7.8 V		4.6	5.0	5.4	V
Open Detection Voltage	$V_{TH(F)}$	R_F = 47K Ω		2.6	3.8	5.0	
Low Level Clamp Voltage	$V_{IL(F)}$	V_{CC} = 0 V	$V_{IN(F)}$ = 18 V	—	1.0	1.8	
High Level Clamp Voltage	$V_{IH(F)}$	V_{CC} = 18 V	R = 47kΩ	5.0	5.4	5.8	
Output Saturation Voltage	V_{OL}	I_{OL} = 240 mA		—	0.9	1.2	
Output Current (High-level)	I_{OH}	V_{CC} = 24 V		—	—	1.0	mA
Over Voltage Protection	V_{CCZ}	I_{CC} = 200 mA, τ = 100 mA		35	40	45	V

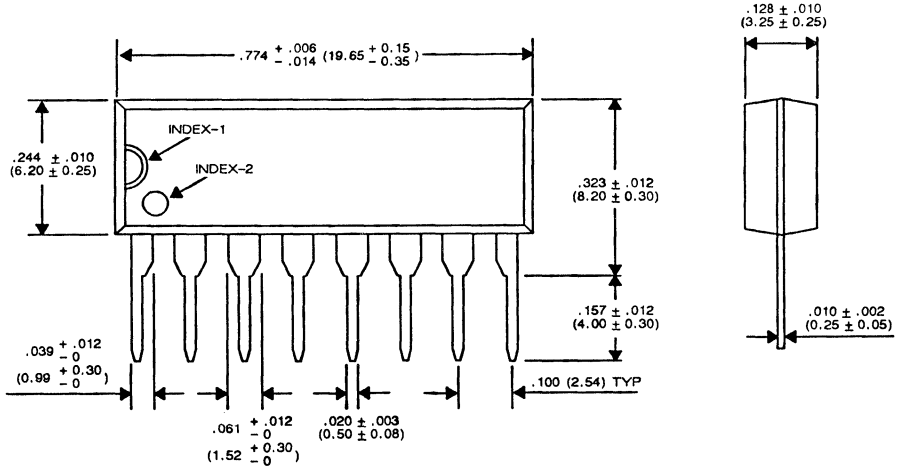
8

APPLICATION



PACKAGE DIMENSIONS

8-LEAD PLASTIC SINGLE IN-LINE PACKAGE
(Case No. SIP-08-M03)



Dimensions in inches (millimeters)

S08010S-2C

8

April 1990
Edition 1.0

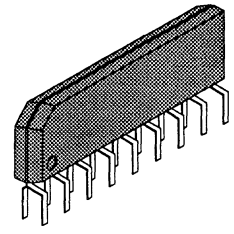
FUJITSU

PRODUCT PROFILE

MB4214
Long Period Timer

DESCRIPTION

The Fujitsu MB4214 is designed to be a long period timer. It contains an oscillator, divider (13-state flip-flop), output circuit, power supply circuit, and two-channel comparator. Arbitrary period is set by an external resistor (RT), capacitor (C_T), and input voltage (V_S).



Plastic Package
ZIP-17P-M01

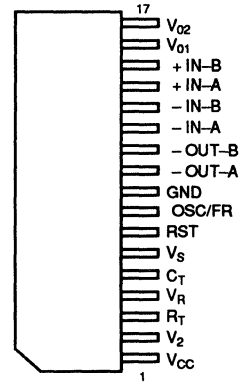
FEATURES

- Time adjustable: 500 ms to 100 hours
- Oscillator period is controlled by V_S input voltage
- Free running oscillation is achieved
- On-chip low power IIL (Integrated Injection Logic) divider
- On-chip Zener diode to maintain stability
- On-chip two-channel comparator
- Timer output level: TTL (open collector)
- Plastic 17-pin ZIP Package

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Power Supply Voltage	V_{CC}	18	V
Zener Current	I_Z	20	mA
Input Voltage	V_{IN}	−0.3 to 18 ($V_{IN} \leq V_{CC}$)	V
Output Voltage	V_O	18	V
Power Dissipation	P_D	360 ($T_A \leq 85°C$)	mW
Operating Temperature	T_A	−30 to +85	°C
Storage Temperature	T_{STG}	−55 to +125	°C

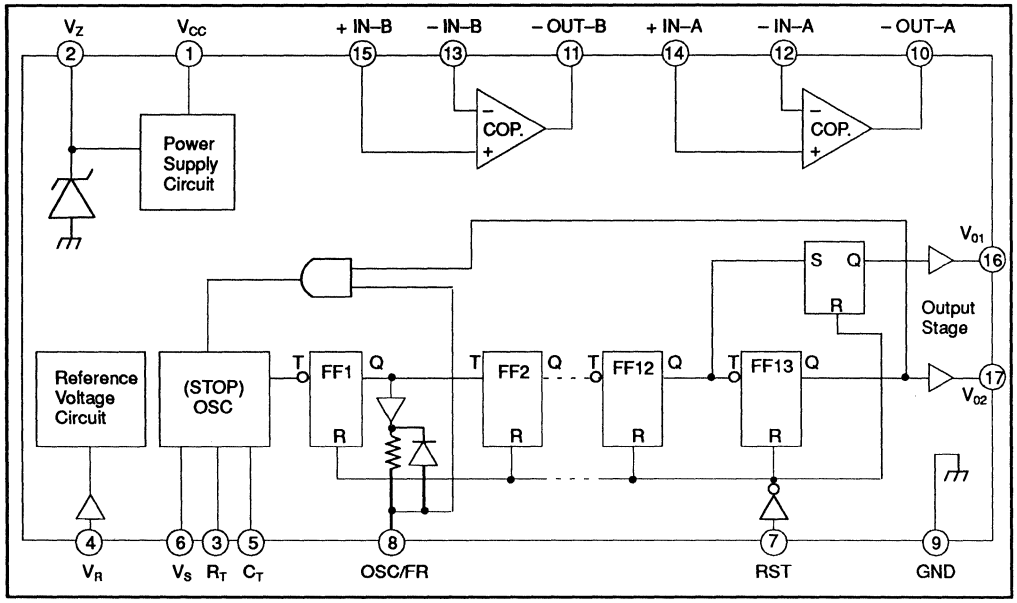
Pin Assignment
(Front View)



Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

FIGURE 1. MB4214 BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin No.	Pin Name	Description
1	V_{CC}	Power Supply Voltage, 4.5 to 16 V
2	V_Z	Zener Pin V_Z pin outputs Zener current 20 mA max. Unless it is used as stability power supply source, it should be connected to the VCC pin through a resistor about 100 kΩ.
3	R_T	R_T Input Pin This pin is provided to connect the time constant of a resistor which controls the oscillator period.
4	V_R	Reference Voltage Output Reference voltage of 3.5 V is output. This pin can supply the current up to 3 mA.
5	C_T	C_T Input Pin This pin is provided to connect a capacitor which controls the oscillator period.
6	V_S	V_S Input Voltage Input Voltage to this pin controls the oscillator period.
7	RST	Reset Pin Counter operation is interruped by the instruction of RST pininput level. The counter is cleared when this pin is connected to GND. Power on reset is achieved by connecting an external capacitor.

Continued on next page

PIN DESCRIPTIONS

Pin No.	Pin Name	Description
8	OSC/FR	Free Running Oscillator Output When this pin is connected to GND, the output is 4096 times longer than the normal oscillator frequency.
9	GND	Ground
10	OUT–A	Open Collector Outputs
11	OUT–B	
12	–IN–A	
13	–IN–B	Comparator Inputs
14	+IN–A	
15	+IN–B	
16	V_{01}	Timer Output Pin No. 1 expands the oscillator period 2048 times the fundamental oscillator period.
17	V_{02}	Time Output Pin No. 2 The 4096 times as long as fundamental oscillator period is kept. Owing to free running oscillation, the 4096 times as long as oscillator frequency is output.

FUNCTIONAL DESCRIPTION

The MB4214 contains a reference voltage circuit, oscillator, divider and comparator. Oscillator frequency is arbitrarily controlled by external resistor R_T, capacitor C_T, and input voltage V_S.

The divider consists of a 13-stage divider circuit which is constructed with the IIL (Integrated Injection Logic) technique. It expands the oscillator period up to 4096 times the fundamental period. This expanded period allows the capacitor to achieve a period of approximately 100 hours.

A free running oscillation (long period, low frequency) is achieved when the OSC/FR pins connected to GND.

8

START RESISTORS R_S

R_S is a start resistor which controls the Zener diode current. The Zener current is 20 mA max and generates a stable Zener voltage of 6.2 V.

RESET FUNCTION

Counter operation is interruped by means of the reset pin (pin 7). All counters are cleared when this pin is connected to GND.

Power on reset is availble by connecting an external capacitor (C_{RS}). Power on reset time (t_{POR}) is calculated by the following fomula:

$$t_{POR} = 3.5 \frac{C_{RS}}{I_{RS}} \ (s)$$

OSCILLATOR PERIOD

Two ways of selecting the oscillator period are provided.

(1) Divide the internal reference voltage by external resistance, to change the V_S voltage. The R_T pin voltage and reference voltage have a 2:3.5 ratio. The oscillator period is calculated using the following formula:

$$t_{OSC} = \frac{3.5}{2} R_T C_T \frac{R_2}{R_1 + R_2} \ (s)$$

(2) Provide VS voltage to the other power supply source.

$$t_{OSC} = K \frac{R_T\ C_T}{2} V_S\ (s)$$

Note: Conversion value K ≈ 1

FREE RUNNING OSCILLATION

Free running oscillation is achieved when the OSC/FR pin is conected to GND. The V02 pin outputs 4096 times the fundamental oscillator frequency. After the voltage is applied or reset is released, V02 maintains a frequency 2048 times longer than the fundamental period. When the OSC/FR pin is left open, the first divider data is output.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	4.5 to 16	V
Timing Resistance	R_T	10 to 220	kΩ
Timing Capacitance	C_T	0.001 to 100	μF
Operating Temperature	T_A	–30 to +85	°C

ELECTRICAL CHARACTERISTICS

Comparator Section (T_A = 25°C, V_{CC} = 12 V, R_S = 100 kΩ)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Offset Voltage	V_{IO}			2.0	5.0	mV
Input Offset Current	I_{IO}			5	50	nA
Input Bias Current	I_I		–250	–25		nA
Common-Mode Input Voltage	V_{CM}		0		V_{CC}–1.5	V
Voltage Gain	A_V	RL = 15 kΩ	25	200		V/mV
Output Saturation Voltage	V_{OL}	IOL = 10 mA		0.2	0.4	V
Output Sink Current	I_{SINK}	VOL = 1.5 V	20			mA
Output Leakage Current	I_{OH}	VOH = 18 V			1.0	μA
Response Time	t_R	RL = 5.1 kΩ, VRL = 5 V		1.3		μs
Large Signal Response Time	t_{RL}	RL = 5.1 kΩ, VRL = 5 V		300		ns

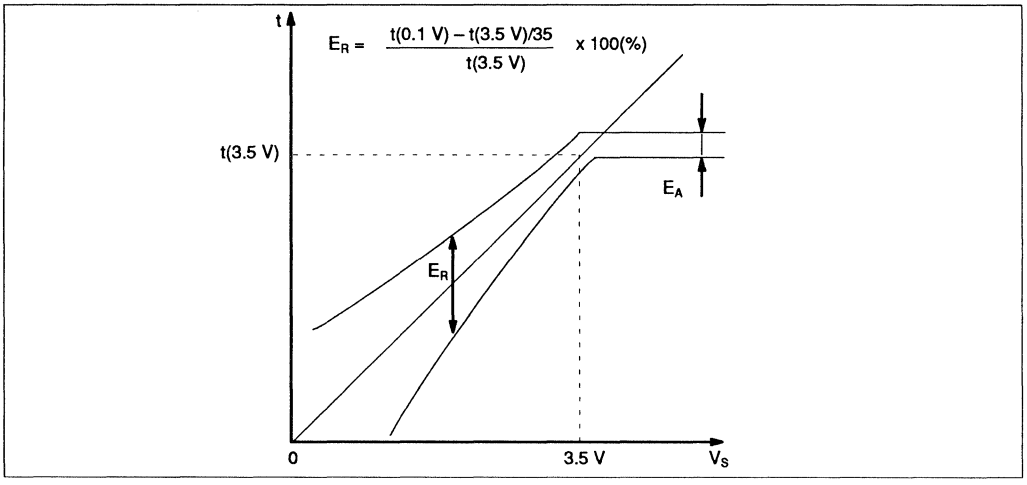
8

ELECTRICAL CHARACTERISTICS (Continued)

Timer Section (T_A = 25°C, V_{CC} = 12 V, R_S = 100 kΩ)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power Supply Curent	I_{CC}	V_{CC} = 12 V	5.0	8.0	12	mA
Zener Voltage	V_Z	I_Z = 0.3 ~ 5 mA	5.7	6.2	6.7	V
Reference Voltage	V_R	V_{CC} = 4.5 ~ 16 V, I_R = 0~ –3 mA	3.3	3.5	3.7	V
	V_{RT}	I_{RT} = –200 µA	1.88	2.0	2.12	V
Charge Current	I_{CT1}	I_{RT} = 10 µA	–11	–10	–9	µA
	I_{CT2}	I_{RT} = –200 µA	–220	–200	–180	µA
Maximum Oscillation Frequency	f_{MAX}		10	100		kHz
Reset Input Threshold Frequency	V_{IL}		1.1	1.4	1.7	V
	V_{IH}		3.2	3.5	3.8	V
Reset Charge Current	I_{RS}	V_{RS} = 0 V	–160	–100	–60	µA
OSC/FR Output Voltage	V_{OL}		1.1	1.4	1.7	V
	V_{OH}		3.7	4.2	4.7	V
Stop Input Current	I_{IST}	V_{ST} = 0.4 V	–20	–100		µA
Output Saturation Voltage	V_{OL}	I_{OL} = 10 mA		0.2	0.4	V
Output Sink Current	I_{SINK}	V_{OL} = 1.5 V	20			mA
Output Leakage Current	I_{OH}	V_{OH} = 18 V			1.0	µA
VS Input Curent	I_{IS}	V_S = 0.4 V	–5	–1		µA
VS Input Voltage	V_{INS}		0.1		VCC–2	V
VT Setting Error	E_A	C_T = 0.01µF, R_T = 100 kΩ, V_S = V_R	–10		10	%
Linearity Error	E_R	C_T = 0.01µF, R_T = 100 kΩ	–2.5		2.5	%

FIGURE 2. LINEARITY ERROR



OSCILLATOR PERIOD

$$1.\ t_{OSC} \approx K \bullet \frac{R_T\ C_T}{2} \bullet V_S\ (s)$$

$$2.\ t_{OSC} \approx \frac{3.5}{2}\ R_T\ C_T\ \frac{R_2}{R_1 + R_2}\ (s)$$

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Note: Divide the internal reference voltage (V_R) by external resistance to obtain the V_S Voltage.

Figure 3. Power Supply Current vs. Power Supply Voltage

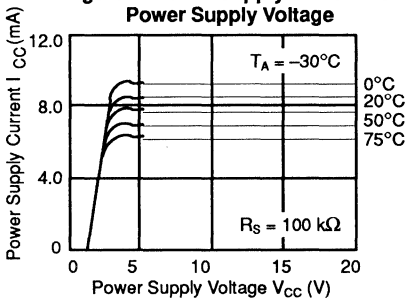


Figure 4. Zener Current vs. Zener Voltage

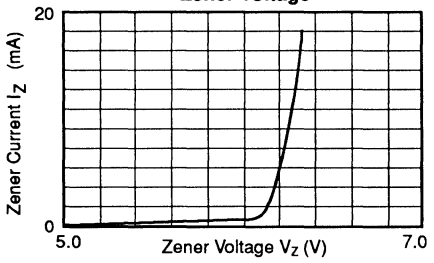


Figure 5. Reference Voltage vs. Ambient Temperature

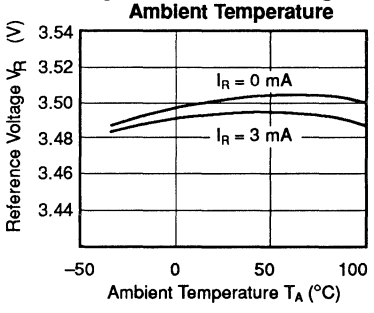
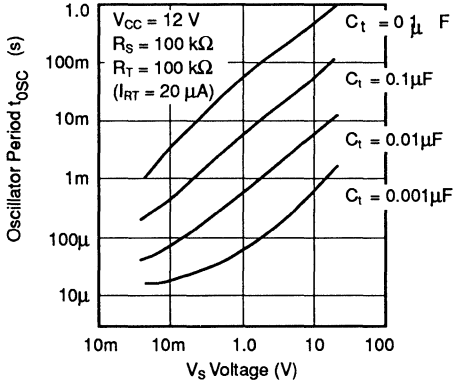


Figure 6. Oscillator Period vs. Voltage



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TYPICAL CHARACTERISTICS CURVES (Continued)

Timer Section (Continued)

Figure 7. Oscillator Period vs. R_T Resistor

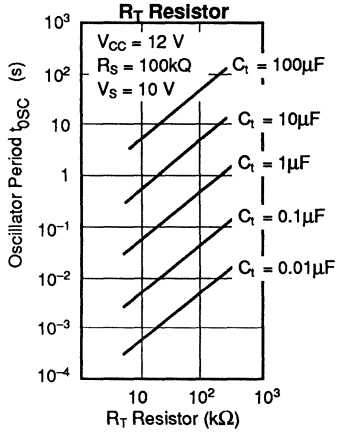

Figure 8. Delay Time vs. R_T Resistor

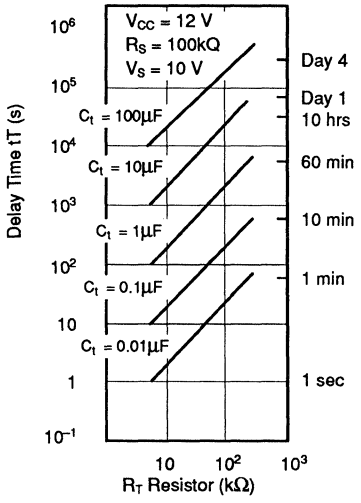

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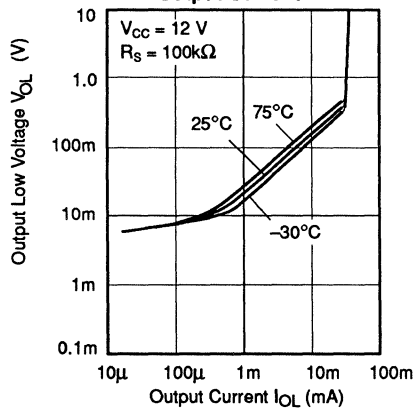
Figure 9. Output Low Voltage vs. Output Current



TYPICAL CHARACTERISTICS CURVES (Continued)

Comparator Section

Figure 10. Input Voltage/Output Voltage vs. Time

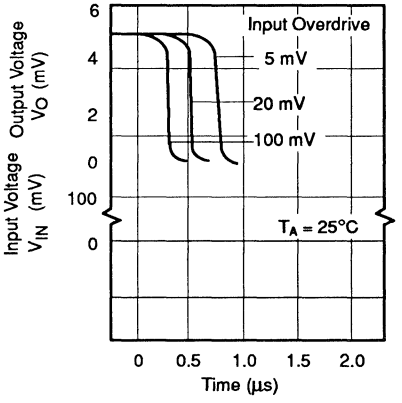


Figure 11. Output Low Voltage vs.Output Current

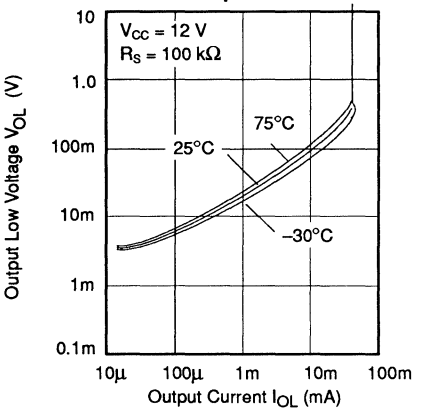
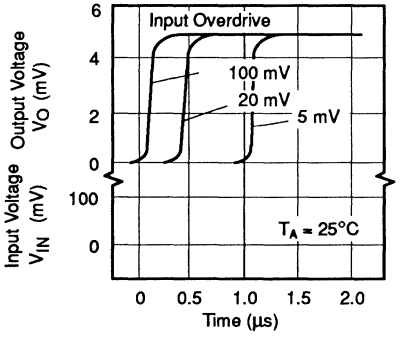


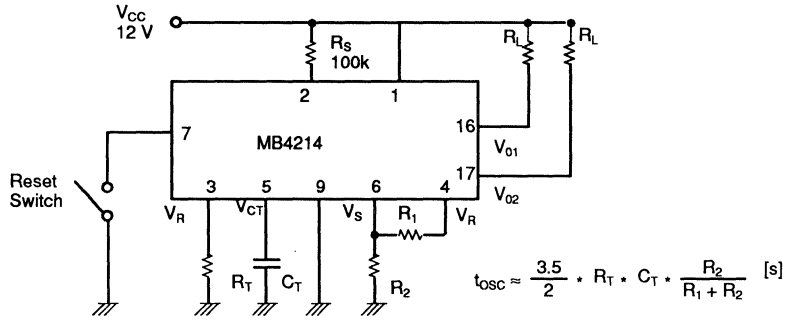
Figure 12. Input Voltage/Output Voltage vs. Time

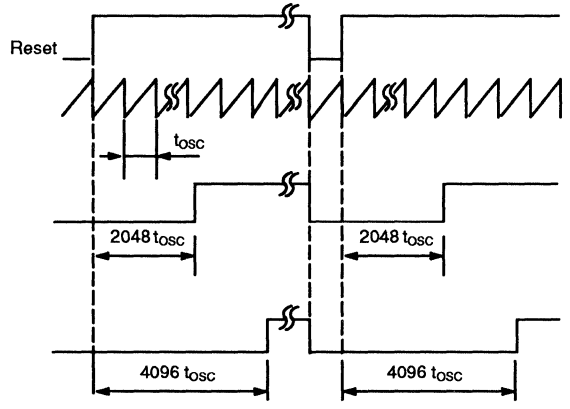


8

APPLICATION EXAMPLES

FIGURE 13. TIMING





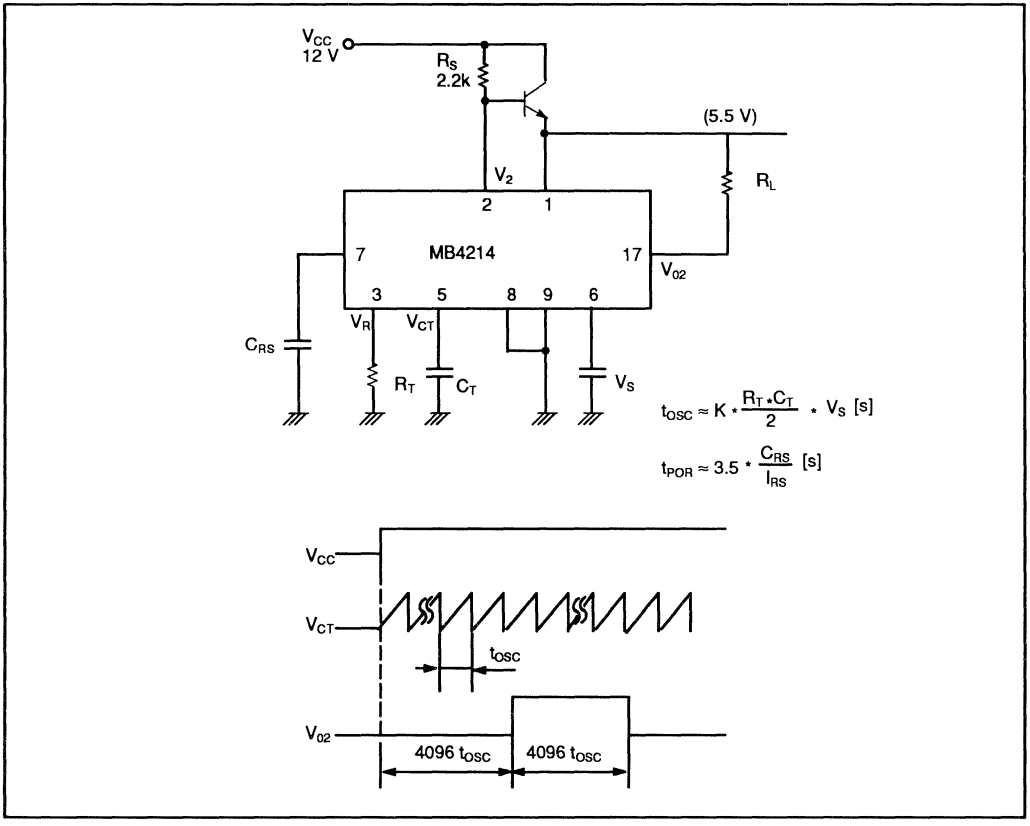
Start Timing: Rising edge of reset signal
Stop Timing: Rising edge of V_{01} output

100 mV

8

APPLICATION EXAMPLES (Continued)

FIGURE 14. SUPER LOW FREQUENCY OSCILLATOR



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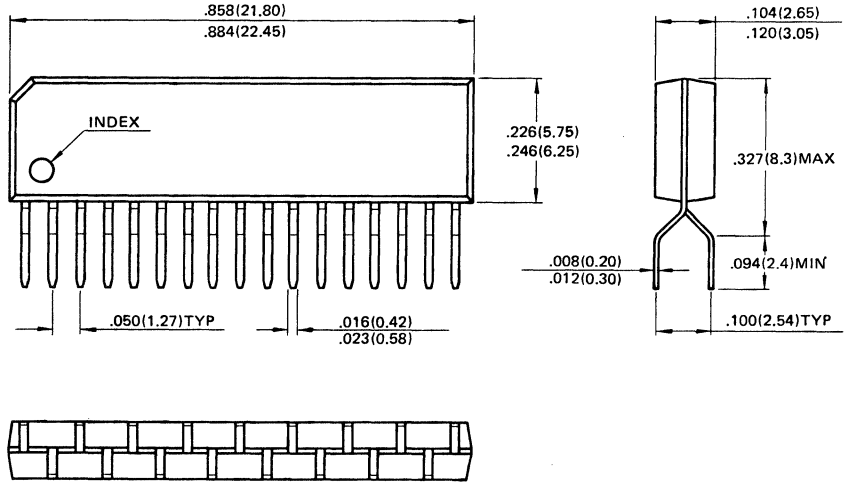
PACKAGE DIMENSIONS

7-LEAD PLASTIC ZIGZAG IN-LINE PACKAGE
(Case No. ZIP-17P-M01)



Dimensions in
inches (millimeters)

8

FUJITSU

QUAD SPST BI-FET ANALOG SWITCH

MB47201

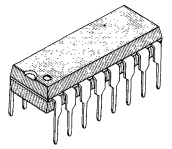
May 1988
Edition 1.0

QUAD SPST BI-FET ANALOG SWITCH

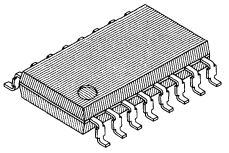
The Fujitsu MB47201 is a quad SPST (Single-pole Signal-Throw) BI-FET analog switch manufactured using Fujitsu Advanced Bipolar Technology. The MB47201 has four independent one-input one-output bi-directional analog switch which provides a constant resistance over the wide temperature and input voltage ranges.

The logic level of its input is CMOS and TTL compatible and break-before-make switching action can be surely operated.

- Low ON resistance : 110 Ω typ.
- Small temperature coefficient of ON resistance : 0.1%/°C
- Small supply voltage coefficient of ON resistance : 0.4%/V
- High speed switching
- Break-before-make action : $t_{ON} > t_{OFF}$
- Low Leakage current : 0.1 nA
- Logic input level : CMOS/TTL
- Compatible with DG201, LF11201, SW-01
- Package 16-pin Plastic DIP Package (Suffix: -P)
  16-pin Plastic FPT package (Suffix: -PF)



PLASTIC PACKAGE
DIP-16P-M04



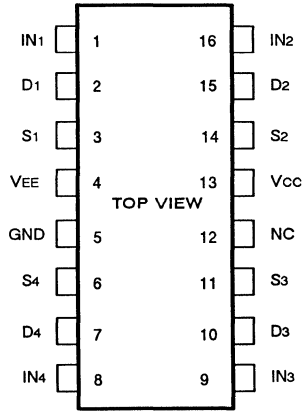
PLASTIC PACKAGE
FPT-16P-M02

ABSOLUTE MAXIMUM RATINGS (TA=25°C)

Rating	Symbol	Value	Unit
Power Supply Voltage (Between VCC and VEE)		36	V
Positive supply voltage (Between VCC and GND)		36	V
Analog Input Voltage	V_{INA}	VEE-10 to VCC+1	V
Logic Input Voltage	V_{IND}	-4 to VCC, ≧VEE	V
Analog Input Current	I_{INA}	± 30	mA
Power Dissipation	P_D	800	mW
Operating Temperature	T_A	-30 to +85	°C
Storage Temperature	TSTG	-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT



This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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Fig. 1 – MB47201 BLOCK DIAGRAM

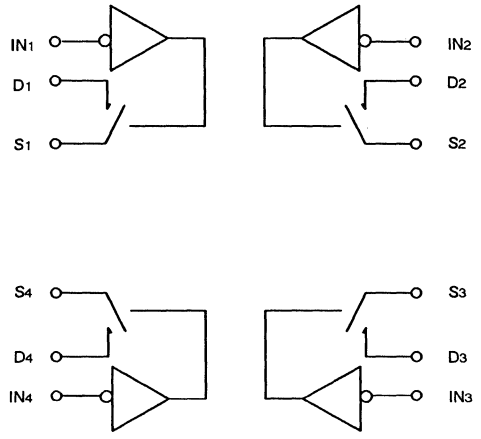
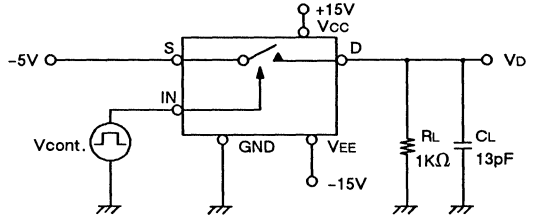
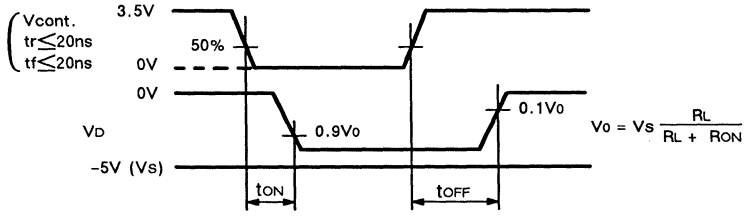


Fig. 2 – tON, tOFF MEASUREMENT CIRCUIT



Switch is ON when IN is at low level.



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ELECTRICAL CHARACTERISTICS (VCC=15V, VEE=-15V, TA=25°C)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
ON Resistance	R_{ON}	V_{INA}=0V, I_D=1mA		110	150	Ω
ON Resistance Matching		V_A=0, I_D=100μA		4	10	%
Analog Input Voltage	V_{INA}	I_D=1mA	10	11		V
		$\lvert\Delta R_{ON}/R(V_A=0)\rvert$<10%		-13	- 10	
ON Resistance deviation		$\lvert V_A\rvert \leq$10V, $I_D \leq$ 1mA $\lvert\Delta R_{ON}/R(V_A=0)\rvert$		4	10	%
ON Resistance Coefficient with Temperature		V_A=0, I_D=100μA		0.1		%/°C
Analog Input Current	I_{NA}	$\lvert V_A\rvert \leq$10V	5	10		mA
Source Current (OFF)	I_{SOFF}	V_S=10V, V_D=-10V		0.1	10	nA
Drain Current (OFF)	I_{DOFF}	V_S=10V, V_D=- 10V		0.1	10	nA
OFF Isolation	I_{SOOFF}	f=500kHz, $R_{L=680}$Ω		58		dB
Crosstalk Attenuation	X_{CH}	f=500KHz, R_L=680Ω		70		dB
Turn ON Time	t_{ON}	V_S=-5V, R_L=1kΩ		300		ns
Turn OFF Time	t_{OFF}	V_S=- 5V, R_L=1kΩ		200		ns
Break-before-make (t_{ON} to t_{OFF})	t_{BBM}			100		ns
Source Input Capacitance	C_{SOFF}	V_A=0		7		pF
Drain Input Capacitance	C_{DOFF}	V_A=0		7		pF
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input High Current	I_{IH}				1	μA
Input Low Current	I_{IL}		-10	-1		μA
Positive Supply Current	I_{CC}			6.8	9.5	mA
Negative Supply Current	I_{EE}		-6.0	- 3.3		mA
Ground Current	I_{GND}		-5.0	-3.5		mA

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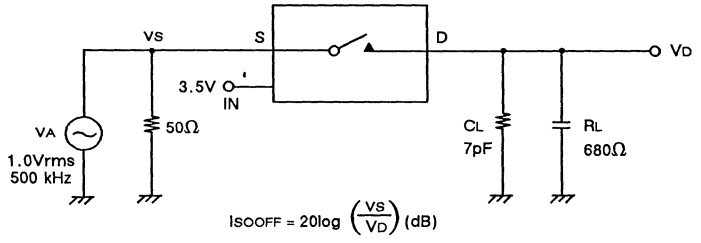
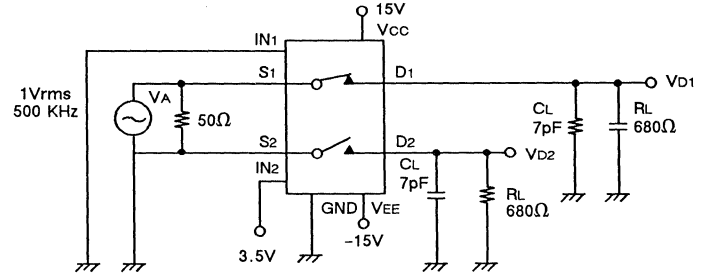
Fig. 3 – ISOOFF MEASUREMENT CIRCUIT



$$ISOOFF = 20\log\left(\frac{VS}{VD}\right)(dB)$$

Fig. 4 – XCH MEASUREMENT CIRCUIT



Crosstalk attenuation $XCH = 20\log\left(\frac{VD2}{VD1}\right)dB$

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TYPICAL CHARACTERISTICS CURVES

Fig. 5 – TURN ON/OFF TIME vs. ANALOG INPUT VOLTAGE

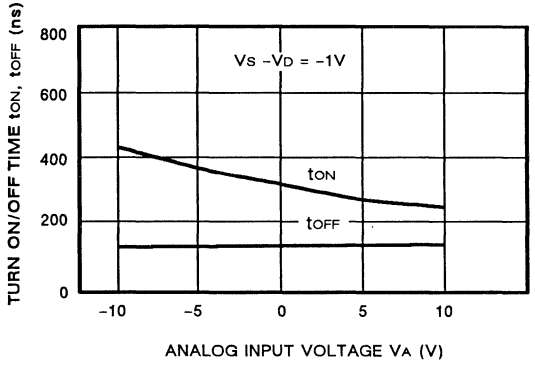


Fig. 6 – TURN ON/OFF TIME vs. TEMPERATURE

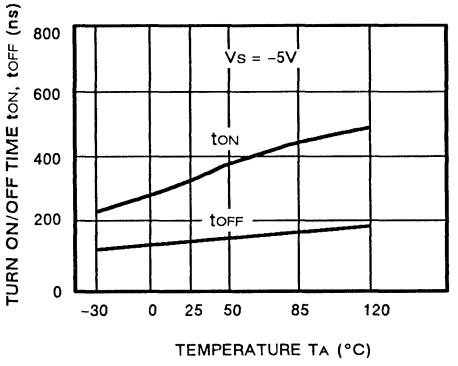


Fig. 7 – ON RESISTANCE vs. ANALOG INPUT CURRENT

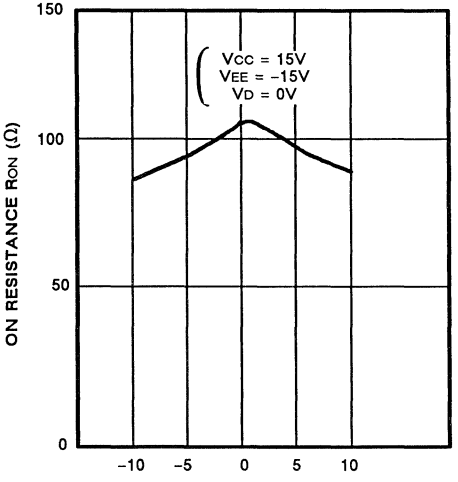
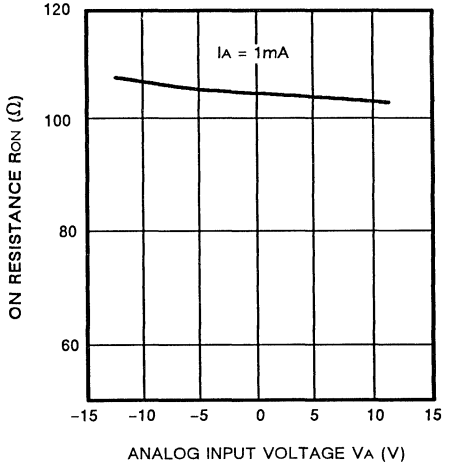


Fig. 8 – ON RESISTANCE vs. ANALOG INPUT VOLTAGE



8

TYPICAL CHARACTERISTICS CURVES (Continued)

Fig. 9 - ON RESISTANCE vs. TEMPERATURE

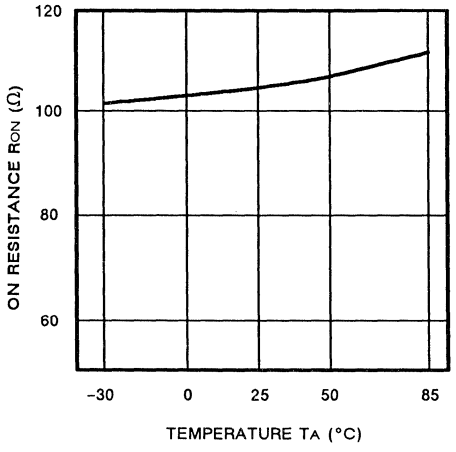


Fig. 10 - ON RESISTANCE vs. POWER SUPPLY VOLTAGE

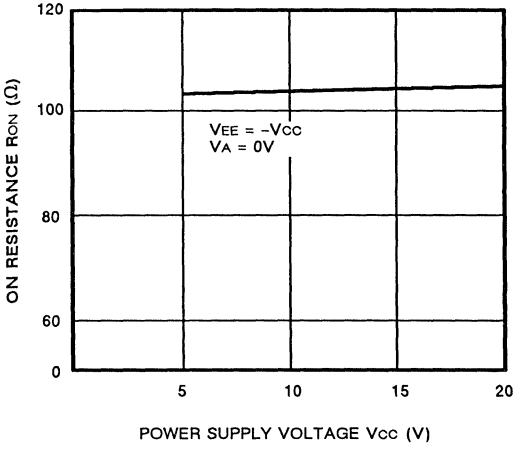


Fig. 11 - OFF ISOLATION/CROSSTALK ATTENUATION vs.FREQUENCY

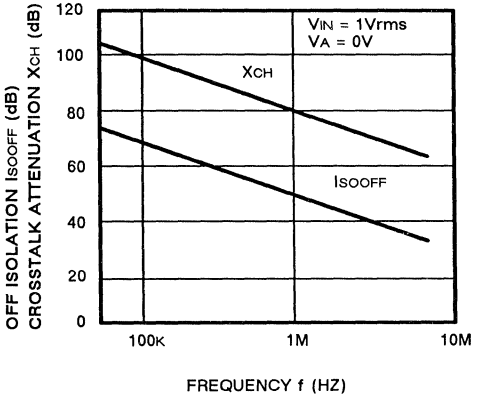
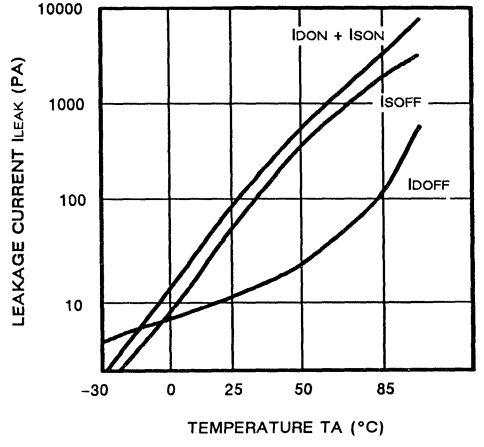


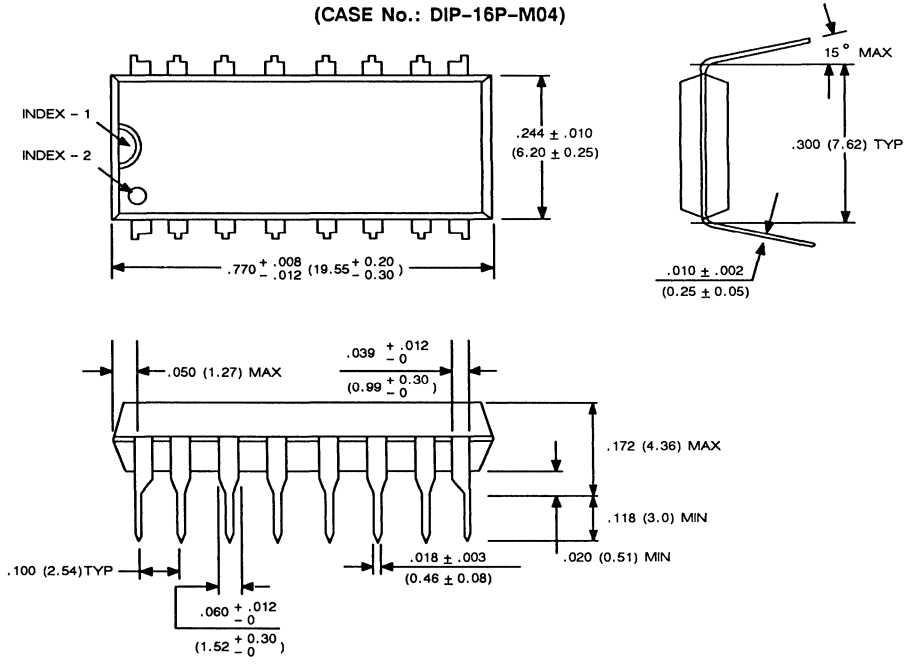
Fig. 12 - LEAKAGE CURRENT vs. TEMPERATURE



8

PACKAGE DIMENSIONS

16-LEAD PLASTIC DUAL-IN-LINE PACKAGE
(CASE No.: DIP-16P-M04)



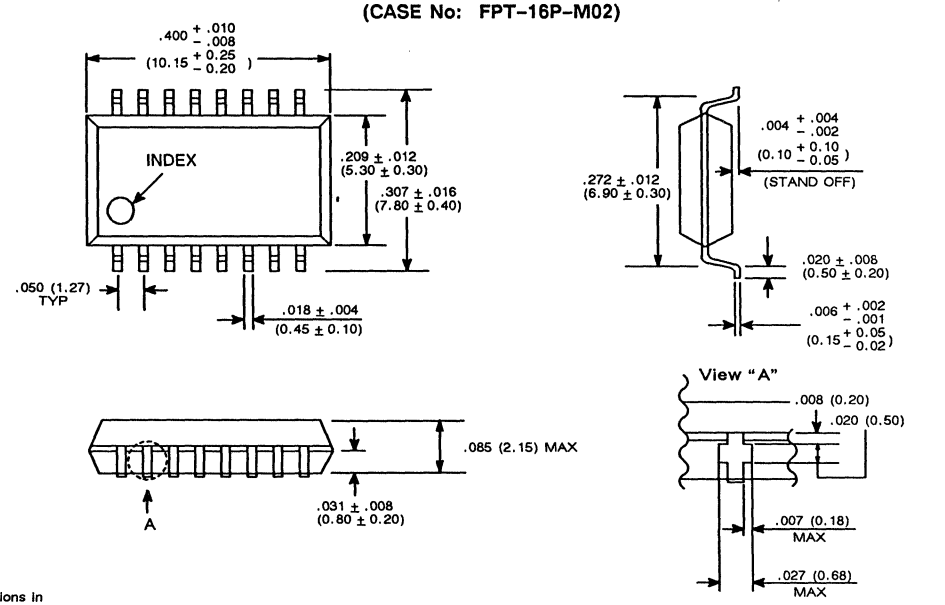
Dimensions in
inches (millimeters)

D16033S-2C

8

PACKAGE DIMENSIONS

16-LEAD PLASTIC FLAT PACKAGE
(CASE No: FPT-16P-M02)



Dimensions in
inches (millimeters)

F16005S-3C

8

Section 9

Quality and Reliability — *At a Glance*

9

9

Quality Control at Fujitsu

Built-in Quality and Reliability

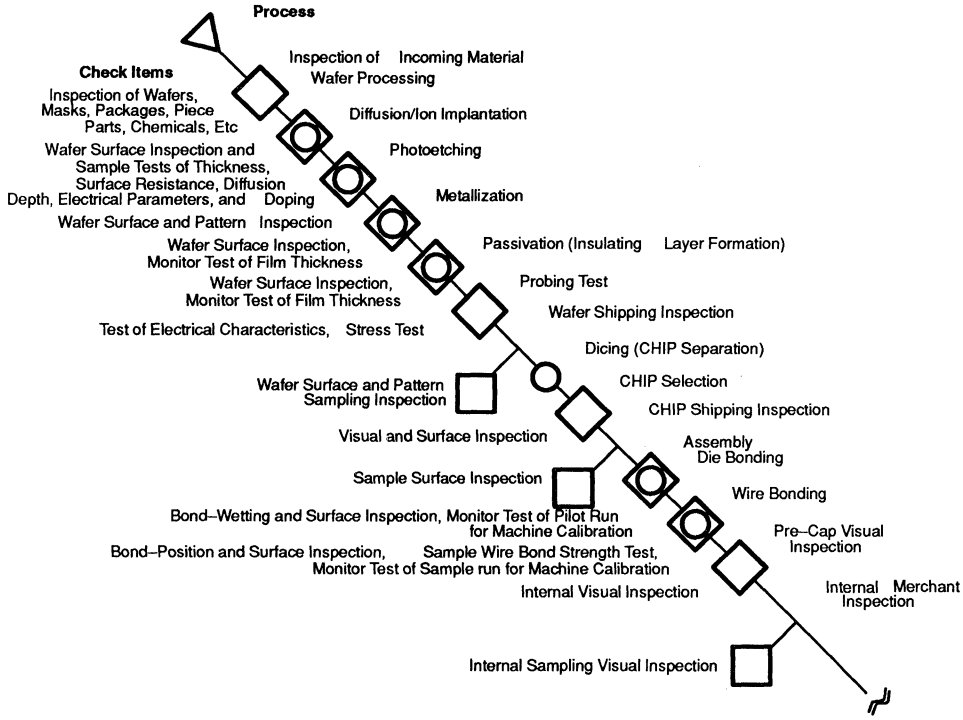
Fujitsu's integrated circuits work. The reason they work is Fujitsu's single-minded approach to built-in quality and reliability, and its dedication to providing components and systems that meet exacting requirements allowing no room for failure.

Fujitsu's philosophy is to build quality and reliability into every step of the manufacturing process. Each design and process is scrutinized by individuals and teams of professionals dedicated to perfection.

The quest for perfection does not end when the product leaves the Fujitsu factory. It extends to the customer's factory as well, where integrated circuits are subsystems of the customer's final product. Fujitsu emphasizes meticulous interaction between the individuals who design, manufacture, evaluate, sell, and use its products.

Quality control for all Fujitsu products is an integrated process that crosses all lines of the manufacturing cycle. The quality control process begins with inspection of all incoming raw materials and ends with shipping and reliability tests following final test of the finished product. Prior to warehousing, Fujitsu products have been subjected to the scrutiny of man, machine, and technology, and are ready to serve the customer in the designated application.

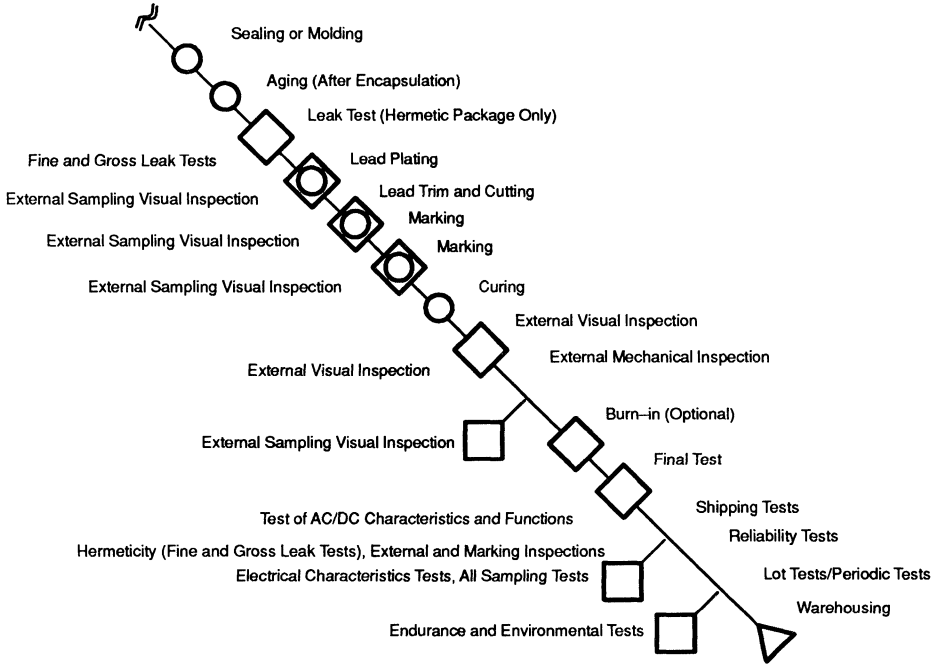
Quality Control Processes at Fujitsu



Continued on next page

9

Quality Control Processes at Fujitsu (Continued)



Legend:

- Production Process
- Test/Inspection
- Production Process and Test/Inspection
- QC Gate (Sampling)

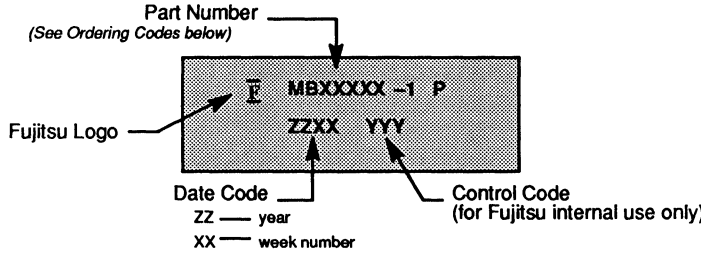
Note:
The flow sequence may vary slightly with individual product type.

9

Section 10

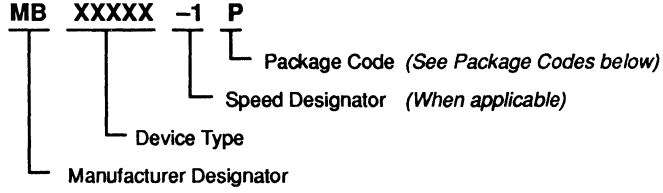
Ordering Information — *At a Glance*

IC Product Marking



Note: Marking formats may vary, depending on the product. The country of origin appears on all finished parts.

IC Ordering Code (Part Number)



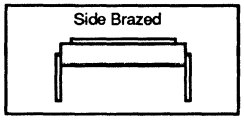
MB Identifies an IC designed and manufactured by Fujitsu that uses a Fujitsu-designated device number.
MBM Identifies an IC designed and manufactured by Fujitsu that uses a device number designated by the industry to be the industry standard number.
Note: Please contact your nearest Fujitsu sales office, representative, or distributor for exact part number/order information.

IC Package Codes

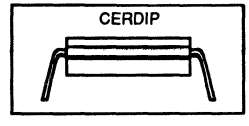
Ceramic	
Package Type	*Package Code*
LCC (Leadless Chip Carrier)	TV,CV
PGA (Pin Grid Array)	CR
DIP (Side Brazed)[1]	C
DIP (CERDIP)[2]	Z
Shrink DIP	CSH
Flatpack, Metal Seal	CF
Flatpack, Glass Seal	ZF
SOJ (Small Outline J-lead)	CJ

Plastic	
Package Type	*Package Code*
LCC (Leadless Chip Carrier)	PV
PLCC (Leaded Chip Carrier)	PD
PGA (Pin Grid Array)	PR
DIP (Dual In-line Package)	P,M
Shrink DIP	PSH
Flatpack	PF
Single In-line, straight leads	PS
Single in-line, zig-zag leads	PSZ,PZ
SOJ (Small Outline J-lead)	PJ

1 Side Brazed



2 CERDIP



Section 11

Sales Information — *At a Glance*

11

Introduction to Fujitsu

Fujitsu Limited

Fujitsu Limited, headquartered near Tokyo, Japan, is the largest supplier of computers in Japan and is among the top ten companies operating in Japan. Fujitsu is also one of the world's largest suppliers of telecommunications equipment and semiconductor devices.

Established in 1935 as the Communications Division spinoff of Fuji Electric Company Limited, Fujitsu Limited, in 1985, celebrated 50 years of service to the world through the development and manufacture of state-of-the-art products in data processing, telecommunications and semiconductors.

Fujitsu has five plants in key industrial regions in Japan covering all steps of semiconductor production. Five wholly-owned Japanese subsidiaries provide additional capacity for production of advanced semiconductor devices. Two additional facilities operate in the U.S. and one in Europe to help meet the growing worldwide demand for Fujitsu semiconductor products.

Introduction to Fujitsu (Continued)

Fujitsu Microelectronics, Inc.

Fujitsu Microelectronics, Inc. (FMI), with headquarters in San Jose, California, was established in 1979 as a wholly-owned Fujitsu Limited subsidiary for the marketing, sales, and distribution of Fujitsu integrated circuit and component products. Since 1979, FMI has grown to three marketing divisions, two manufacturing divisions and a subsidiary. FMI offers a complete array of semiconductor products for its customers.

The Advanced Products Division (APD) is responsible for the complete product development cycle, from design through operations support and worldwide marketing and sales. Products are the result of both internal development and external relationships, such as joint development agreements, technology licenses, and joint ventures. The SPARC™ RISC processor was developed by both APD and Sun Microsystems, Inc.

In addition to designing and selling a full line of SPARC processors and peripheral chips, APD also designed and is selling the EtherStar™ LAN controller — the first VLSI device to integrate both StarLAN™ and Ethernet® protocols into one device. The core of APD's EtherStar chip was the result of APD's cooperative venture with Ungermann-Bass.

The Microwave and Optoelectronics Division (MOD) markets GaAs, FETs, and FET power amplifiers, lightwave and microwave devices, optical devices, emitters, and SI transistors.

The largest FMI marketing division is the Integrated Circuits Division (ICD).

Memory and programmable devices marketed by ICD include the following:

DRAMs and DRAM Modules
EPROMs
EEPROMs
NOVRAMs
CMOS masked ROMs
CMOS SRAMs and CMOS SRAM Modules
BiCMOS SRAMs
Bipolar PROMs
ECL RAMs
STRAMs (self-timed RAM)
Hi-Rel PROMs and SRAMs
Ultra High-speed ECL/ECL—TTL Translator Circuits
Linear ICs and Transistors

Introduction to Fujitsu (Continued)

ASIC products offered by ICD include the following:

CMOS, ECL, and BiCMOS gate arrays
CMOS standard cells
Design Software Support

Customer support and customer training for ASIC products are available through the following FMI design centers:

San Jose	Gresham
Dallas	Chicago
Atlanta	Boston

Microcomputer and communications products offered by ICD include the following:

4-bit MCUs
8- and 16-bit MPUs
SCSI and controllers
DSPs
Prescalers
PLLs
Memory Cards

FMI's manufacturing divisions are in San Diego, California and Gresham, Oregon. The San Diego Manufacturing Division assembles and tests memory devices. In 1988, the Gresham Manufacturing Division began manufacturing ASIC products and DRAM memories. This facility, when completed, will have one million square feet of manufacturing—the largest Fujitsu manufacturing plant outside Japan.

FMI's subsidiary, **Fujitsu Components of America**, markets connectors, keyboards, plasma displays, relays, and hybrid ICs.

Fujitsu Mikroelektronik GmbH (European Sales Operation)

Fujitsu Mikroelektronik GmbH (FMG) was established in June, 1980, in Frankfurt, West Germany, and is a wholly-owned subsidiary of Fujitsu Limited, Tokyo. FMG is the sole representative of the Fujitsu Electronic Device Group in Europe. The wide range of ICs, LSI memories, microprocessors, and ASIC products are noted throughout Europe for design excellence and unmatched reliability. Branch offices are located in Munich, London, Paris, Stockholm, and Milan.

Introduction to Fujitsu (Continued)

Fujitsu Microelectronics Ireland, Ltd. (European Production Operation)

Fujitsu Microelectronics Ireland, Ltd. (FME) was established in 1980, in the suburbs of Dublin, as Fujitsu's European Production Center for integrated circuits. FME assembles DRAMs, EPROMs, and other LSI memory products.

Fujitsu Microelectronics, Ltd. (European ASIC Design Operation)

Fujitsu Microelectronics, Ltd., Fujitsu's European VLSI Design Center, opened in October of 1983 in Manchester, England. The Design Center is equipped with highly sophisticated CAD systems to ensure fast and reliable processing of input data. An experienced staff of engineers is available to assist in all phases of the design process.

Fujitsu Microelectronics Asia PTE Ltd. (Asian/Oceanian Sales Operation)

Fujitsu Microelectronics Asia PTE Ltd. (FMA) opened in August 1986 in Hong Kong as a wholly-owned Fujitsu subsidiary for sales of electronic devices to Asian and Southwest Pacific markets.

11

SPARC™ is a trademark of Sun Microsystems, Inc.
Ethernet® is a registered trademark of Xerox Corporation.
EtherStar™ is a trademark of Fujitsu Microelectronics, Inc.
StarLAN™ is a trademark of AT&T.

Integrated Circuits Corporate Headquarters — Worldwide

International Corporate Headquarters

FUJITSU LIMITED
Marunouchi Headquarters
6–1, Marunouchi 1–chome
Chiyoda–ku, Tokyo 100
Japan
Tel: (03) 216-3211
Telex: 781–22833
FAX: (03) 213-7174

For integrated circuits marketing information please contact the following:

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FUJITSU LIMITED
Integrated Circuits and Semiconductor Marketing
Furukawa Sogo Bldg.
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Chiyoda–ku, Tokyo 100
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Tel: (03) 216-3211
Telex: 781–2224361
FAX: (03) 211-3987

Headquarters for North and South America

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Integrated Circuits Division
3545 North First Street
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Tel: (408) 922–9000
Telex: 910–338–0190
FAX: (408) 432–9044

Headquarters for Europe

FUJITSU MIKROELEKTRONIK GmbH
Lyoner Strasse 44–48
Arabella Centre 9. OG
D–6000 Frankfurt 71
Federal Republic of Germany
Tel: (069) 66320
Telex: 441963
FAX: (069) 6632122

Headquarters for Asia and Australia

FUJITSU MICROELECTRONICS ASIA PTE LIMITED
06-04/06-07 Plaza by the Park
No. 52 Bras Basah Road
Singapore 0718
Tel: (65) 336–1600
Telex: 55573
FAX: (65) 336–1609

Fujitsu Microelectronics, Inc. (FMI) Sales Offices for *North and South America*

NORTHERN CALIFORNIA

Fujitsu Microelectronics, Inc.
10600 N. De Anza Blvd.
Suite 225
Cupertino, CA 95014
Tel: (408) 996–1600
FAX: (408) 725–8746

SOUTHERN CALIFORNIA

Fujitsu Microelectronics, Inc.
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Suite 510
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FAX: (714) 724–8778

COLORADO (Denver)

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Englewood, CO 80111
Tel: (303) 740–8880
FAX: (303) 740–8988

GEORGIA (Atlanta)

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Tel: (404) 449–8539
FAX: (404) 441–2016

ILLINOIS (Chicago)

Fujitsu Microelectronics, Inc.
One Pierce Place
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FAX: (708) 250–8591

MASSACHUSETTS (Boston)

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FAX: (617) 964–3301

MINNESOTA (Minneapolis)

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Eagan, MN 55122–1303
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FAX: (612) 454–0601

NEW JERSEY (Mt. Laurel)

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3000 Atrium Way
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FAX: (609) 727–9797

NEW YORK (Hauppauge)

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601 Veterans Memorial Highway
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Hauppauge, NY 11788–1054
Tel: (516) 361–6565
FAX: (516) 361–6480

OREGON (Portland)

Fujitsu Microelectronics, Inc.
5285 SW Meadows Road
Suite 222
Lake Oswego, OR 97035–9998
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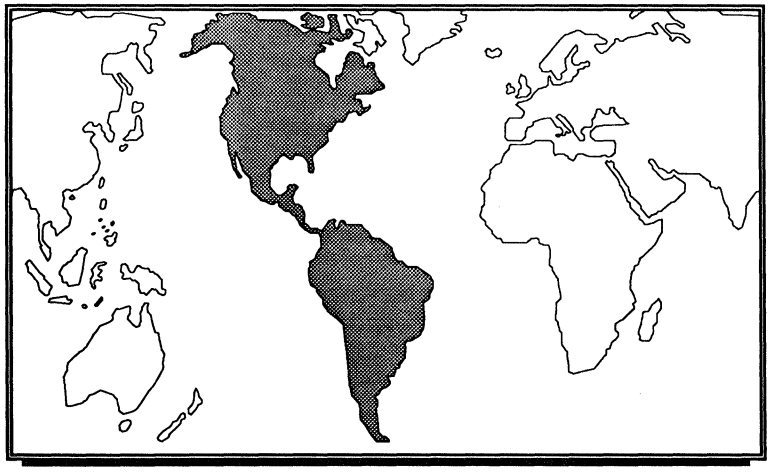
FAX: (503) 684–4547

TEXAS (Dallas)

Fujitsu Microelectronics, Inc.
14785 Preston Road
Suite 670
Dallas, TX 75240
Tel: (214) 233–9394
FAX: (214) 386–7917



FMI Representatives — USA

For product information, contact your nearest Representative.

Alabama

The Novus Group, Inc.
2905 Westcorp Blvd.
Suite 120
Huntsville, AL 35805
Tel: (205) 534–0044
FAX: (205) 534–0186

Arizona

Aztech Component Sales Inc.
15230 N 75th Street
Suite 1031
Scottsdale, AZ 85260
Tel: (602) 991–6300
FAX: (602) 991–0563

California

Harvey King, Inc.
6393 Nancy Ridge Drive
San Diego, CA 92121
Tel: (619) 587–9300
FAX: (619) 587–0507

Infinity Sales, Inc.
4500 Campus Drive
Suite 300
Newport Beach, CA 92660
Tel: (714) 833–0300
FAX: (714) 833–0303

Norcomp
3350 Scott Blvd.,
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Tel: (408) 727–7707
FAX: (408) 986–1947

Norcomp
2140 Professional Drive
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Roseville, CA 95661
Tel: (916) 782–8070
FAX: (916) 782–8073

Sonika Electronica of America
925 Hale Place
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Tel: (619) 482–8700
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Colorado

Front Range Marketing
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Suite 404
Boulder, CO 80303
Tel: (303) 443–4780
FAX: (303) 447–0371

Connecticut

Conntech Sales, Inc.
182 Grand Street
Suite 318
Waterbury, CT 06702
Tel: (203) 754–2823
FAX: (203) 573–0538

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657 Maitland Avenue
Altamonte Springs, FL 32701
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Semtronic Associates, Inc.
1467 S. Missouri Avenue
Clearwater, FL 33516
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FAX: (813) 442–2234

Semtronic Associates, Inc.
3471 NW 55th Street
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FAX: (305) 731–1019

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Norcross, GA 30093
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FAX: (708) 256–9592

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Fred Dorsey & Associates
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Carmel, IN 46032
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FAX: (317) 844–4843

Iowa

Electromec Sales
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Tel: (319) 362–6413
FAX: (319) 362–6535

Kansas

Rothkopf & Associates, Inc.
1948 E. Santa Fe
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Arbotek Associates
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FAX: (301) 337–2781

Massachusetts

Mill–Bern Associates
2 Mack Road
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Tel: (617) 932–3311
FAX: (617) 932–0511

Michigan

Greiner Associates, Inc.
15324 E. Jefferson Avenue
Suite 12
Grosse Point Park, MI 48230
Tel: (313) 499–0188
FAX: (313) 499–0665

FMI Representatives — USA (Continued)

Minnesota

Electromec Sales
1601 E Highway 13
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Burnsville, MN 55337
Tel: (612) 894–8200
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Rothkopf & Associates, Inc.
8721 Manchester Road
St. Louis, MO 63144
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FAX: (314) 961–4736

New Jersey

BGR Associates
Evesham Commons
525 Route 73
Suite 100
Marlton, NJ 08053
Tel: (609) 983–1020
FAX: (609) 983–1879

Technical Applications & Marketing
91 Clinton Road
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Fairfield, NJ 07006
Tel: (201) 575–4130
FAX: (201) 575–4563

New York

Quality Components
3343 Harlem Road
Buffalo, NY 14225
Tel: (716) 837–5430
FAX: (716) 837–0662

Quality Components
116 Fayette Street
Manlius, NY 13104
Tel: (315) 682–8885
FAX: (315) 682–2277

Quality Components
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FAX: (716) 342–7227

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FAX: (513) 899–3260

Spectrum ESD
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FAX: (503) 645–6196

Texas

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3320 Wiley Post Road
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FAX: (214) 387–3605

Technical Marketing, Inc.
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FAX: (713) 783–5307

Technical Marketing, Inc.
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FAX: (512) 338–1596

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FAX: (206) 828–6102

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Beta Technology
9401 W Beloit Street
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Mexico

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FAX: (36) 473433

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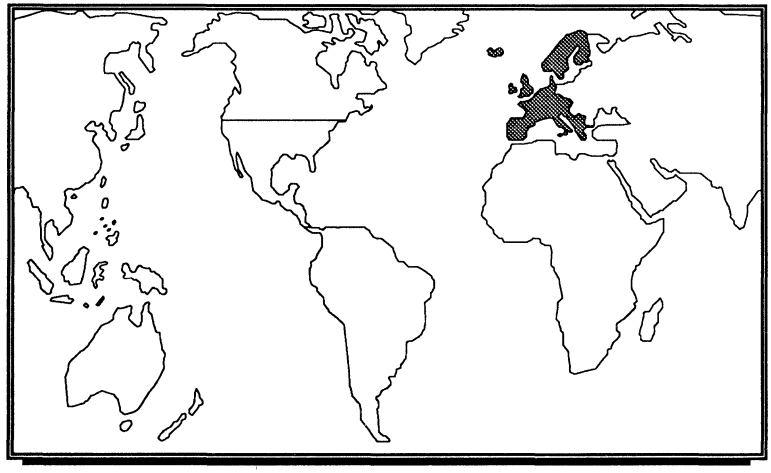

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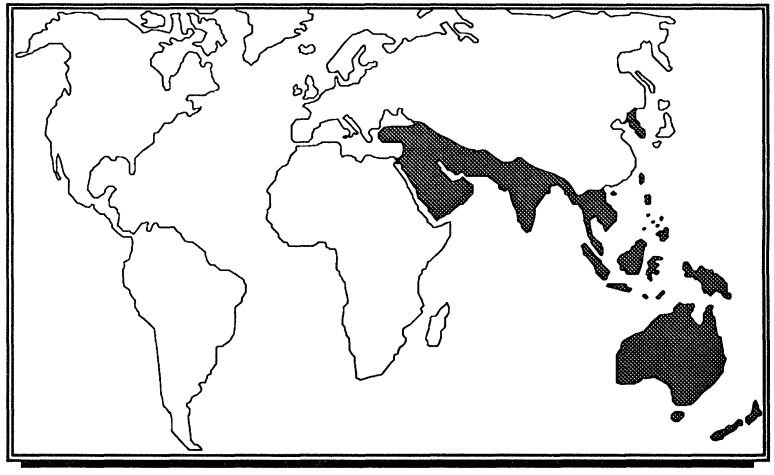

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Section 12

Design Information — *At a Glance*

12

Appendix 1

Cross Reference Guide

Linear Products Cross Reference Guide

Part Number	Package	Pins	Description	Alterrnate Source Part Number	Manufacturer
MB3106	Plastic SIP	8	Dual Low Noise Pre-Amplifier		
MB3110A	Plastic SIP	8	Dual Control Amplifier		
MB3111	Plastic ZIP	17	Distortion Limiting IC		
MB3120	Plastic FPT ZIP	16 17	Compandor IC		
MB3501	Plastic DIP FPT	14 14	Wide Bank Video Amplifier		
MB3603	Plastic DIP Ceramic DIP	14 14	High Gain Operational Amplifier	µA741	National
MB3604	Plastic DIP Ceramic DIP	16 16	High Frequency Operational Amplifier		
MB3607	Plastic DIP FPT Ceramic DIP	8 8 8	Dual Operational Amplifier	MC1458 CA1458 HA21458 HA5102 MPOP14 µA1458HC LF412 µPC1458 µPC251 OP14 OP215 OP270 RC2041 NE5512 LF412 TA75458	Motorola, Samsung GE/RCA Harris Harris Micro Power National National NEC NEC PMI PMI PMI Raytheon Signetics TI Toshiba
MB3609			High Gain Operational Amplifier	LM741	National
MB3614	Plastic DIP FPT Ceramic DIP	14 14 14	Quad Operational Amplifier	LM324	National
MB3615	Plastic DIP FPT FPT	14 14 8	Quad Operational Amplifier	MC3303 µA303 OP421	Mot., Signetics, TI National PMI
MB3714A		8	6 W Audio Power Amplifier		
MB3715A		8	6 W Audio Power Amplifier		
MB3722	Plastic SIP	12	5.8 W Dual Audio Power Amplifier		

Continued on next page

Linear Products Cross Reference Guide

Part Number	Package	Pins	Description	Alterrnate Source Part Number	Manufacturer
MB3730A	Plastic SIP	7	14 W BTL Audio Power Amplifier		
MB3731	Plastic SIP	12	18 W BTL Audio Power Amplifier		
MB3732	Plastic SIP	7	14 W BTL Audio Power Amplifier		
MB3733	Plastic SIP	12	20 W BTL Audio Power Amplifier		
MB3734	Plastic SIP	9	14 W BTL Audio Power Amplifier		
MB3735	Plastic SIP	9	20 W BTL Audio Power Amplifier		
MB3736	Plastic SIP	9	15 W BTL Audio Power Amplifier		
MB3737A	Plastic SIP ZIP	12 12	23 W BTL Audio Power Amplifier		
MB3742	Plastic ZIP	17	15 W BTL Audio Power Amplifier		
MB3752	Plastic DIP FPT Ceramic DIP	14 14 14	Series Voltage Regulator	µA723 CA723 LM723 HA17723 RC723 RM723 SG723	Nat'l, Signetics, TI GE/RCA GE/Intersil, National Hitachi Raytheon Raytheon Silicon General
MB3756	Plastic SIP	8	Series Voltage Regulator, 3 Outputs		
MB3759	Plastic DIP FPT Ceramic DIP	16 16 16	High Speed PWM Control Circuit	TL494 µC494A	TI Unitrode
MB3761	Plastic DIP SIP FPT	8 8 8	Voltage Detector		
MB3763	Plastic DIP SIP FPT	8 8 8	Bidirectional Motor Driver		
MB3763H	Plastic SIP	8	Bidirectional Motor Driver		
MB3764		16	9-Level Detector and Driver for Level Meter		
MB3769A	Plastic DIP FPT	16 16	High Speed PWM Control Circuit	µC384	Unitrode

Continued on next page

Linear Products Cross Reference Guide

Part Number	Package	Pins	Description	Alternate Source Part Number	Manufacturer
MB3771	Plastic DIP SIP FPT	8 8 8	Power Supply Monitor		
MB3773	Plastic DIP SIP FPT	8 8 8	Power Supply Monitor with Timer		
MB3774	Plastic ZIP	17	Car Audio System Power Supply		
MB3780A	Plastic DIP FPT FPT	16 16 20	Battery Backup IC		
MB3854	Plastic DIP FPT	8 8	Bidirectional Motor Driver		
MB4001	Plastic DIP FPT	8 8	High Speed Comparator	µA710	National
MB4002	Plastic DIP FPT	8 8	High Speed Comparator	µA710 (Impr)	National
MB4051	Plastic DIP	42	8-Channel 10-Bit A/D Converter		
MB4053	Plastic DIP FPT Ceramic DIP	16 16 16	6-Channel 10-Bit A/D Converter	MC14443 µA9708	Motorola National
MB4056	Plastic DIP Ceramic DIP	16 16	8-Channel 8–Bit A/D Converter		
MB4063	Plastic DIP FPT Ceramic DIP	16 16 16	6-Channel 8-Bit A/D Converter	MC14443 µA9708	Motorola National
MB4066	Plastic DIP Ceramic DIP	16 16	6-Bit A/D and D/A with Clamp Circuit Converter		
MB40176	Plastic DIP FPT	16 16	6-Bit A/D and D/A with Clamp Circuit Converter		
MB40547-7	Ceramic DIP	24	8-Bit Ultra High-speed Video A/D Converter ± 1 LSB		
MB40547-8	Ceramic DIP	24	8-Bit Ultra High-speed Video A/D Converter ± 1/2 LSB		
MB40576	Plastic DIP FPT	16 16	6-Bit Ultra High-speed Video A/D Converter	TL5501 TD6712* CXD1172P	TI Toshiba Sony
MB40578	Plastic DIP	22	8-Bit Ultra High-speed Video A/D Converter ± 0.2% LE	TL5502	TI
MB40578-7	Plastic DIP	22	8-Bit Ultra High-speed Video A/D Converter ± 0.4% LE		

*Toshiba part is pin-compatible with Fujitsu's, except for pins 14 and 15.

Continued on next page

Linear Products Cross Reference Guide

Part Number	Package	Pins	Description	Alterrnate Source Part Number	Manufacturer
MB4072	Plastic DIP FPT Ceramic DIP	16 16 16	8-Bit Multiplying D/A Converter		
MB40748-8	Ceramic DIP	24	10-Bit High-speed D/A Converter	DAC08	PMI
MB40748-9	Ceramic DIP	24	10-Bit High-speed D/A Converter		
MB40748-10	Ceramic DIP	24	10-Bit High-speed D/A Converter		
MB40776	Plastic DIP FPT Ceramic DIP	16 16 24	6-Bit Multiplying D/A Converter	TL5601	TI
MB40776H	Plastic DIP	16	6-Bit Multiplying D/A Converter		
MB40778	Plastic DIP FPT	20 20	8-Bit High-speed D/A Converter	TL5602	TI
MB40788	Ceramic DIP	24	10-Bit Ultra High-speed D/A Converter		
MB40874	Plastic DIP Ceramic DIP	20 20	4-Bit D/A Converter with Lookup Table 4-Bit D/A with RAM		
MB40968	Plastic DIP FPT	28 28	2-channel 8-Bit D/A Converter		
MB40968/V	Plastic DIP FPT	28 28	2-channel 8-Bit D/A Converter		
MB40978		42 44	3-channel 8-Bit, 60 MSPS D/A Converter, RGB	TL5632	TI
MB4104	Plastic DIP	16	FM Sterro Multiplex Demodulator		
MB4105	Plastic DIP	16	FM Sterro Multiplex Demodulator		
MB4107A	Plastic DIP FPT	24 24	Floppy Disk VFO		
MB4108A	Plastic DIP FPT	24 24	Floppy Disk VFO		
MB4111	Ceramic FPT	24	Magnetic Disk Head Amplifier 4-Channel	SSI104	Silicon Systems
MB4114A	Ceramic FPT	24	Magnetic Disk Head Amplifier 4-Channel		
MB4113	Ceramic FPT	24	Magnetic Disk Head Amplifier 4-Channel		
MB4115	Plastic FPT	34	Magnetic Disk Head R/W Amplifier, 8-Channel for HDD		
MB4116	Plastic FPT	24	Magnetic Disk Head R/W Amplifier, 8-Channel for HDD		
MB4117-4	Plastic DIP FPT Ceramic FPT	22 24 24	Magnetic Disk Head Amplifier 4-Channel	SSI117	Silicon Systems
MB4117-6	Plastic DIP Ceramic FPT	28 28	Magnetic Disk Head Amplifier 6-Channel	SSI117	Silicon Systems

Continued on next page

Linear Products Cross Reference Guide

Part Number	Package	Pins	Description	Alterrnate Source Part Number	Manufacturer
MB4118-4	Plastic DIP FPT Ceramic FPT	22 24 24	Magnetic Disk Head Amplifier 4-Channel	SSI118	Silicon Systems
MB4118-6	Plastic DIP Ceramic FPT	28 28	Magnetic Disk Head Amplifier 6-Channel	SSI118	Silicon Systems
MB4125	Plastic FPT	34	Magnetic Disk Head R/W Amplifier 8-Channel for HDD		
MB4126	Plastic FPT	34	Magnetic Disk Head R/W Amplifier 8-Channel for HDD		
MB4204	Plastic DIP FPT	14 14	Quad Comparator	CA339 GL339 LM339 µPC137/177/339 CMP04 PMI139/339	GE/RCA/Harris Goldstar Mot., Nat'l., TI, Ray. NEC PMI PMI
MB4205	Plastic SIP	8	High Power Comparator		
MB4206	Plastic SIP	8	Frequency-to-Voltage V/F Converter		
MB4207	Plastic SIP	8	Single Power Supply Frequency-to-Voltage V/F Converter with Comparator		
MB4210	Plastic SIP	8	Lamp Open Detector for Automobiles		
MB4214	Plastic ZIP	17	Timer		
MB4313	Ceramic DIP	16	Read/Write Bus Driver/Receiver		
MB4316	Ceramic DIP	16	Driver/Receiver Disk Head Amplifier		
MB4319	Ceramic DIP	16	Peak Detector for Head Position Control		
MB4547-7	Ceramic DIP	24	8-Bit Ultra High-speed A/D Converter 8-Bit Ultra High-speed A/D Converter	TL082	Ti
MB4547-8	Ceramic DIP	24	8-Bit Ultra High-speed A/D Converter		
MB47082	Plastic DIP FPT SIP	8 8 9	J-FET Input Operational Amplifier	XRO82 TL082 CA082	Exar TI GE/RCA
MB47201	Plastic DIP FPT	16 16	Quad SPST BiFET Analog Switch	ADG201 DG201 HI201 MAX331 MP201 LF11201 LF13201 SW201 TSC4201/4202	Analog Devices GE/Intersil Harris Maxim Micro Power National National PMI Teledyne

Continued on next page

Linear Products Cross Reference Guide

Part Number	Package		Pins	Description	Alterrnate Source Part Number	Manufacturer
MB47358	Plastic	DIP	8	Dual Operational Amplifier	LM358	Nat'l., Mot., Sig.
		FPT	8		CA358A	GE/RCA
		SIP	9		GL358	Goldstar
					HA17358	Hitachi
					OP221	PMI
					NE532	Signetics
					LM348	TI
					TA75358	Toshiba
MB47393	Plastic	FPT	8	Dual Comparator	LM393	National
		SIP	9		HAI7393	Hitachi
					µPC277	NEC
					TA75393	Toshiba
MB47833	Plastic	DIP	8	Low Noise Dual Operation Amplifier	LM833	National
		FPT	8			
		SIP	9			
MB87020	Plastic	DIP	40	16-bit A/D, D/A Converter		
MB87032	Plastic	DIP		2-channel Electric Volume Controller		
MB88301A	Plastic	DIP	16	1-Channel x 13-Bit x 3-Channel, 6-Bit D/A Converter		
		FPT	16			
MB88341	Plastic	DIP	20	12-Channel 8-Bit R-2R D/A Converter		
		FPT	20			
MB88342	Plastic	DIP	16	8-Channel 8-Bit R-2R D/A Converter		
		FPT	16			
		FPT	20			

Appendix 2

D/A Converters

November 1989
Edition 1.1

APPLICATION NOTE

FUJITSU

Video Timing Calculations for Fujitsu's MB40978 D/A Converter

by Roy Richards
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ABSTRACT

This application note gives the design engineer information about the timing requirements of a typical modern digital video system that uses digital-to-analog (D/A) and analog-to-digital (A/D) converters. Examples of the calculations made to establish the sample rate and pixel clock frequency requirements of the system are included.

Modern video display systems use high-speed A/D and D/A video converters to provide a large selection of colors and picture elements. Often repeated digital recordings and playback signals also use high-speed video converters.

The Fujitsu MB40978, an 8-bit ultra high-speed D/A converter, is designed for red-green-blue (RGB) applications in digital television and computer graphics display systems. It is capable of conversion rates of 60 MSPS and clock frequencies of 60 MHz.

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Introduction

The first step in designing a video system is to determine the screen format. The display resolution for a home television screen in the United States is 525 lines of interlaced vertical scan lines and screen resolutions for a personal computer's CRT are 1024 horizontal pixels x 768 vertical interlaced scan lines. Computer-aided-design/Computer-aided-manufacturing (CAD/CAM) monitors have even higher pixel densities and use non-interlaced formats for shorter screen rewrite times. On a monitor where text is used in a 7 x 9 pixel font, a definition of at least 720 pixels per line is required (seven horizontal pixels for the character +2, minimum for the space between characters = 9. 0 x 80 characters = 720 pixels per line).

Each horizontal line sweeps the electron beam in the CRT simultaneously from the left to the right for all three guns and returns or "flies back" at an accelerated rate. The portion of the horizontal scan that includes the pixel information is called the *raster line* and the remaining horizontal scan, including the fly back or retrace time and the black spaces at the edge of the screen that are blanked, is called the *blanking region*. The horizontal scan rate is calculated by inverting the sum of the raster time (active region) plus the blanked time.

The horizontal scan rate for U.S. television is 15,750 KHz (found by multiplying the 30 Hz vertical scan rate and the 525 line definition). Commercial U.S. television sets (standardized by NTSC*) have screens that are 60 Hz line-synchronized and use an interlaced format that results in a 30 Hz vertical scan rate. European television (standardized by PAL**) has a format that is synchronized at 50 Hz and 625 lines and that results in a 15,625 KHz scan rate.

Interlacing

Interlacing is a technique used to eliminate screen flicker. In an interlaced display format the first scan begins on the second line and continues scanning every other line to the end of the display. When the first scan is completed, the beam returns to scan the first line and all remaining lines to complete the design. To the human eye, the interlaced lines appear to merge and the scan rate appears doubled. One scan of interlaced pixel data is called a *field* and two scans are called a *frame*. Interlacing cuts the bandwidth needed to write a frame by a factor of 2.

*National Television System committee
**Phase alteration line, the West German television system

DOT Clock Rate

The DOT clock rate, or the clock frequency, is the rate that data is applied to the three RGB data-to-analog converters which, in turn, apply analog voltages, one pixel at a time, to the CRT. See Figure 1. DOT clock rates depend upon the monitor screen resolution and may exceed 50 MHz in many high resolution graphics systems.

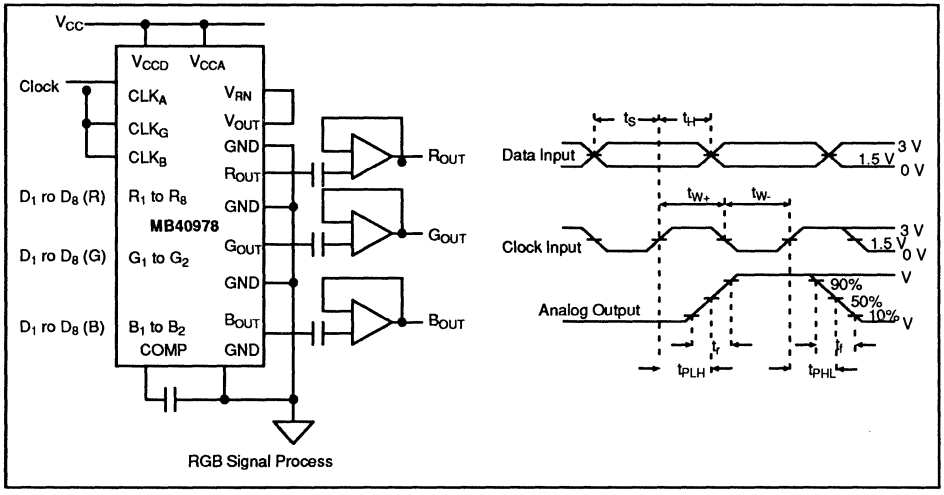

Figure 1. The Fujitsu MB40978 Triple 8-Bit D/A Converter

Each digital-to-analog converter of Fujitsu's MB40978 has an 8-bit resolution which means each color gun can have 256 intensity levels. With this configuration, the color palette can have 16,777,216 colors. Typically some of the bits would be used in a common pattern that allows all three guns to control intensity and results in a reduction of the possible number of colors for the color palette.

Example of Video Timing Calculations for an Interlaced Monitor

To calculate the total horizontal raster time for a 1024 x 768 interlaced 60 Hz monitor, use the parameters in the following chart.

Table 1.

Monitor Specifications 1024H x 768 V Interlaced at 60 Hz sync	Vertical	Horizontal
Blanking time before syncronization (front porch) t_{fp}	2 horizontal lines about 70 µs	2 µs
Synchronization pulse width t_s	200 µs	2.5 µs
Blanking time before raster line (back porch) t_{bp}	NA	3.5 µs
Raster time t_r	NA	To be calculated

To find the pixel or DOT clock rate, divide the raster time by the number or horizontal pixels. To find the pixel time, invert t_p as shown in the following sample calculation.

The total horizontal time t_h is	$t_h = t_{hfp} + t_{hs} + t_{hbp} + t_{hr} = 2 + 2.5 + 3.5 + t_{hr}$
and the horizontal raster time t_{hr} is	$t_{hr} = t_h - 8\ \mu s$
The total vertical time t_v is	$t_v = t_h\ 768 + t_{vfp} + t_{vs} + t_{vbp}$
for 60 Hz interlaced frames	$t_v = 1/30\ Hz = 33\ \mu s$
which allows a total horizontal time t_h of	$t_h = (t_v - t_{vfp} - t_{vs} - t_{vp})/768\ lines$ $= (33{,}000 - 70 - 200 - 0)/768\ lines$ $= 41.66\ \mu s$
The horizontal raster time left is t_{hr}	$t_{hr} = 41.66 - 8 = 33.66\ \mu s$
and the resulting time for each pixel is t_p	$t_p = 33.66/1024 = 32.87\ ns$
This corresponds to a D/A conversion rate	
and minimum clock frequency of	$30.5\ MSPS$

Example of Timing Calculation for a Non-Interlaced Monitor

If the monitor is non-interlaced, with an improved video response to reduce the front porch, sync and back porch times, the writing speed can be improved to a higher sample rate. The following chart gives the parameters for a non-interlaced monitor.

Table 2.

Monitor specifications 1024Hx768V Non-Interlaced at 60 Hz sync	Vertical	Horizontal
Blanking time before sync. (front porch) t_{fp}	2 horizontal lines about 35 us	1.0 µs
Synchronization pulse width ts	200 us	1.5 µs
Blanking time before raster line (back porch) t_{bp}	NA	2.0 µs
Raster time t_r	NA	To be calculated

With these parameters use the following calculations.

$$t_v = 1/60\ Hz = 16{,}700\ \mu s$$

$$t_h = (16{,}700 - 35 - 200)/768 = 21.44\ \mu s$$

$$t_{hr} = 21.44 - 1.0 - 1.5 - 2.0 = 16.94\ \mu s$$

The resulting sample rate must be 59 MSPS and the pixel clock must run at 60 MHz.

The Fujitsu MB40978 is ideally suited to use for either of these video monitors. Fujitsu also has video D/A and A/D converters which can be used in a wide variation of video and high performance audio display and recording functions.

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