

# MB85501-010/-012/-015

## CMOS 8M x 36 Synchronous DRAM Module

### CMOS 8M x 36 Bit Synchronous DRAM Module

The Fujitsu MB85501 is a fully decoded, CMOS Synchronous Dynamic Random Access Memory (SDRAM) module consisting of eighteen MB81116421 devices which organized as CMOS two banks of 2,097,152-word x 4-bit. The MB85501 organized as 8,388,608 x 36-bit is optimized for those applications requiring high speed, high performance, large memory shortage, and high density memory organizations. This module is ideally suited for supercomputers, workstations, laser printers, high resolution graphic adapters, accelerators and other applications where a simple interface is needed.

The all inputs/outputs are LVTTTL compatible, and supply voltage tolerance is  $\pm 9\%$ .

### PRODUCT LINE & FEATURES

Parameters	MB85501-010	MB85501-012	MB85501-015
Clock Frequency	100 MHz max	83 MHz max	66 MHz max
Burst Mode Cycle Time	10 ns min	12 ns min	15 ns min
$\overline{\text{RAS}}$ Access Time	57 ns max	66 ns max	74 ns max
$\overline{\text{CAS}}$ Access Time	27 ns max	31 ns max	34 ns max
Output Valid From Clock(CL=3)	7 ns max	8 ns max	9 ns max
Operating Current (Burst Mode)	6404mW max	5904mW max	5407mW max
Power Down Mode Current	78.5mW max (ADD=L)		

- 8M words x 36 bits (MB81116421 x 18)
- 72 pin socket type (pin pitch 1.27mm)
- 100MHz (Max.) data transfer
- +3.3V $\pm$ 0.3V supply voltage
- 4096 refresh cycles every 65.6 ms
- Dual bank operation
- LVTTTL compatible I/O
- Programmable burst type
- Programmable burst length
- Auto and Self-refresh
- CKE power down mode
- Output Enable and Input Data Mask

### ABSOLUTE MAXIMUM RATINGS (See NOTE.)

Parameter	Symbol	Value	Unit
Supply Voltage	VCC	-0.5 to +4.6	V *1
Input Voltage	VIN	-0.5 to +4.6	V *1
Output Voltage	VOUT	-0.5 to +4.6	V *1
Short Circuit Output Current	IOUT	$\pm 50$	mA
Power Dissipation	PD	24	W
Storage Temperature	TSTG	-55 to +125	°C

\*1 VSS=0V

**NOTE:** Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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DQ0	2	1	VSS
DQ2	4	3	DQ1
DQ4	6	5	DQ3
DQ6	8	7	DQ5
VCC	10	9	DQ7
DQ9	12	11	DQ8
DQ11	14	13	DQ10
DQ13	16	15	DQ12
DQ14	18	17	VSS
NC	20	19	DQ15
$\overline{\text{CS}}$ 1	22	21	CS0
A2	24	23	A3
VCC	26	25	A1
A10	28	27	A0
NC	30	29	A11
$\overline{\text{RAS}}$	32	31	VSS
$\overline{\text{WE}}$	34	33	$\overline{\text{CAS}}$
A5	36	35	A4
A7	38	37	A6
A9	40	39	A8
VSS	42	41	NC
CKE1	44	43	CKE0
CLK	46	45	NC
DQM0	48	47	VCC
DQ16	50	49	DQM1
DQ18	52	51	DQ17
DQ20	54	53	DQ19
VSS	56	55	DQ21
DQ23	58	57	DQ22
DQ25	60	59	DQ24
DQ26	62	61	VCC
DQ28	64	63	DQ27
DQ30	66	65	DQ29
DQ32	68	67	DQ31
DQ34	70	69	DQ33
VSS	72	71	DQ35

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.