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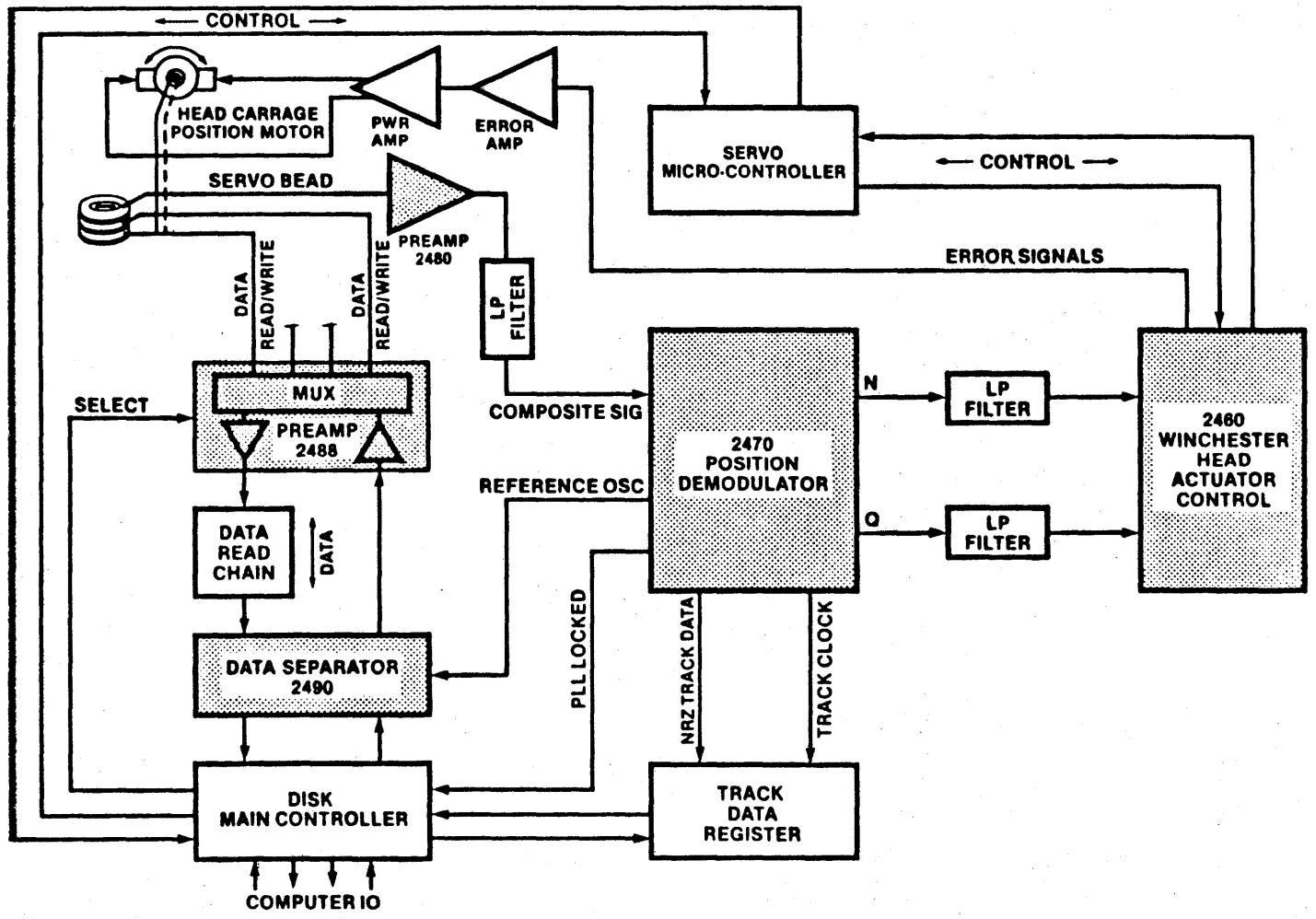
Simplified Disk System Block Diagram



LINEAR

FAIRCHILD
A Schlumberger Company

μA2460 • μA2461
Servo Control Chips

April 1986

Linear Division Computer Peripherals

Description

The μA2460 and μA2461 provide the analog signal processing required between a drive resident microprocessor and the servo power amplifier for Winchester disk closed loop head positioning. The μA2460 and μA2461 receive quadrature position signals from the servo channel, and from them, derives actual head seek velocity as well as position-mode off-track error. In the seek mode, the DAC is used to command velocity, while actual velocity is obtained by differentiating the quadrature position signals provided at V1 for external processing. The velocity signal (V2) obtained by integrating the motor current is also available for extra damping, if desired. Further, the DAC may be used for detenting the head off-track for any pupose such as thermal compensation or soft-error retrys.

- **Microprocessor Compatible Interface**
- **Quadrature Di-Bit Compatible**
- **On Board DAC**
- **Velocity V1 Derived from Position Signal**
- **Velocity V2 Derived from Motor Current**
- **Quarter-Track-Crossing Signal Outputs**
- **Minimal External Components**
- **Compatible with μA2470 Demodulator**

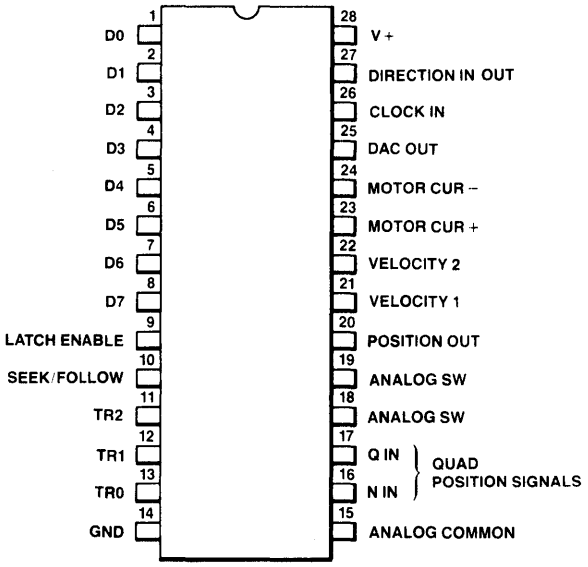
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Plastic LCC	−65°C to +150°C
Operating Temperature Range	
Commercial	0°C to 70°C
Lead Temperature	
Ceramic DIP (soldering, 60s)	300°C
Plastic LCC (soldering, 10s)	265°C
Internal Power Dissipation[1, 2]	
28L-Ceramic DIP	2.50 W
28L-Plastic LCC	1.39 W
Supply Voltage	15 V Max
Analog Common Voltage	8.0 V Max
All inputs	V supply Max

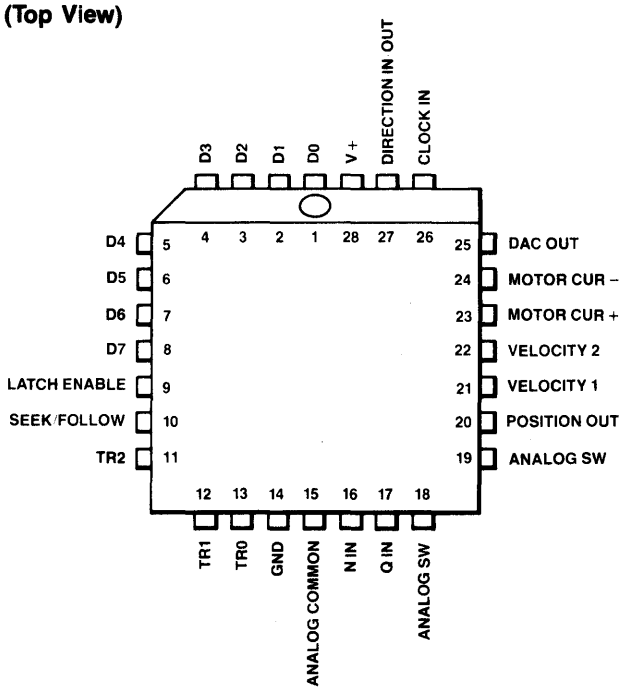
Notes:

1. $T_{J\ Max}$ = 150°C for the Plastic LCC, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 28L-Ceramic DIP at 16.7 mW/°C, and the 28L-Plastic LCC at 11.2 mW/°C.

Connection Diagram
28-Lead DIP
(Top View)



Connection Diagram
28-Lead PLCC
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2460DC	FM	Ceramic DIP
μA2461DC	FM	Ceramic DIP
μA2460QC	KH	Plastic LCC
μA2461QC	KH	Plastic LCC

Fairchild Semiconductor Corporation, Linear Division
313 Fairchild Drive, Mountain View, California 94042
(415) 962-4011 TWX MVLD

Description of Lead Functions

Lead	Name	Description of Function
Inputs		
1–8	DAC Input Word (D0–D7)	Programs DAC output. oooooooo=Analog Command Lead 1 = LSB Lead 8 = MSB
9	Latch Enable	Allows present DAC input word to be latched
10	Seek/Follow Mode	Configures the feedback loop for either seeking or track-following. (High = Seek, Low = Follow)
14	Ground	
15	Analog Common	Analog signal reference level (5.0 V)
16	N	Normal position input signal.
17	Q	Quadrature position input signal.
23	Motor Current +	Motor current sense input to motor current integrator.
24	Motor Current –	
26	Clock	4.0 MHz (maximum) input square wave.
27	Direction In/Out	Changes the polarity of DAC output from positive to negative consistent with the desired direction of head motion.
28	V_{CC}	12 V supply
Outputs		
11	Track 2^2 (T_2)	TTL signal indicating N, Q (for μA2460) TTL signal whose frequency is 2 times N (or Q) (for μA2461).
12	Track 2^1 (T_1)	TTL signal indicating N*, Q (for μA2460) TTL signal whose frequency is 4 times N (or Q) (for μA2461).
13	Track 2^0 (T_0)	TTL signal whose frequency is 8 times N (or Q).
18	Analog Switch	Analog switch to be used externally for changing from seek to follow.
19	Analog Switch	
Inputs		
20	Position Output	Analog signal representing sensed off track amplitude
21	Velocity 1	Analog output representing velocity processed from position signals N and Q.
22	Velocity 2	Analog output representing the integral of motor current.
25	DAC Output	Used to command velocity and position.

Functional Description

Figure 2 shows a block diagram of the μA2460/μA2461 Servo Controller.

Power Supply and Reference requirements

The μA2460/μA2461 is designed to operate from a single supply of 10 V to 12 V. Also required is a reference voltage of 5.0 V called Analog Common which serves two functions; all analog signals will be referenced to this voltage and in addition the internal DAC will use it to set full scale.

A clock signal must be provided as a reference for the internal switched capacitor position differentiator and motor current integrator. The clock signal should be a sine or square wave between Analog Common and ground at a maximum frequency of 4.0 MHz.

All digital inputs and outputs are TTL compatible levels referenced to ground.

Input signals and Track crossing outputs

The input format selected for position feedback is consistent with a large class of sensors that generate two cyclical output signals displaced in space phase by 90 degrees (so called quadrature signal pairs). These sensors include resolvers, inducto-syns, optical encoders, and most importantly, servo demodulators designed for rigid disk head position sensing.

The input signals N and Q are quadrature quasi triangular waveforms with amplitudes of ±2.5 V nominal referenced to Analog Common. The periods of the input signals are subdivided by internal comparators and logic and sent to the Track Crossing outputs T_0, T_1, and T_2. The relationship of these outputs to the inputs N and Q is shown in *Figure 3* (for μA2460) and *Figure 3A* (for μA2461).

Note that different servo patterns may yield different numbers of track centerlines for each period of the quadrature signal pair. The relationship of T_0, T_1, and T_2 to N and Q is independent of track centerlines, leaving the correct interpretations to the microcontroller.

DAC

The DAC is an 8-bit, buffered input, voltage output digital to analog converter. The output voltage with an input code of all zeros is equal to Analog Common. Full scale is equal to Analog Common ±2.35 V. The polarity depends on the Direction In Signal; Direction In High will result in a positive DAC output.

The DAC enable line when high will cause the DAC's input buffer to become transparent, i.e. input data will affect the the output voltage immediately. When DAC enable is brought low the data present on the input lines will be latched and any further changes to the input data will not change the output voltage. The DAC functions in both Seek and Follow Mode. During Seek Mode the DAC output is used as a velocity reference. In Follow Mode the DAC output can be summed into the position reference signal to offset the heads from track center.

Analog Switch

An uncommitted single pole single throw analog switch with an ON resistance of approximately 300 Ω is provided. This switch is ON during Follow Mode.

Mode Select

The two major intended operating modes for the μA2460 are controlled by the microcontroller via the SEEK/FOLLOW input. Mode Select input high enables Seek Mode, low enables Track Follow Mode.

SEEK, when asserted by the microcontroller along with DIRECTION and a non-zero VELOCITY value as inputs, causes the actuator system to accelerate in the requested direction. During the ensuing motion, the acuator system will come under velocity feedback control. The velocity feedback signal is created by differentiation of the quadrature position signals and, additionally, by integration of motor current.

FOLLOW, the negation of SEEK, changes the feedback loop to a track-following or position mode. Position servos are typically second order systems and without loop compensation are potentially unstable. External components are used, along with the μA2460, to achieve stable track following performance. Velocity information V1 is made available as an output in this mode as an aid in stabilizing certain loops. If non-zero data is supplied to the velocity latches in this mode, it will result in a track offset in the direction indicated by DIRECTION IN/OUT. *Figure 4* shows typical seek operation.

Position Output

When the μA2460/μA2461 is set to Seek Mode the signal from Position Output lead is shown in *Figure 5*. This signal is made by switching the position inputs, (N and Q) through an inverter if required, (N* and Q*) to the output using the track crossing signals. It can be used, if deired, to interpolate between DAC steps by attenuating it and summing it with the DAC output.

Track Follow Mode is entered when the heads are near the end of a seek, usually within one half to one track away from the target track centerline. The final setting to the track center is done by the position loop.

When the device is switched to Follow Mode, the position input signal (N, N*, Q or Q*) that is currently selected to the output is latched and the Position Out signal follows the

Figure 1 Head Actuator Control System

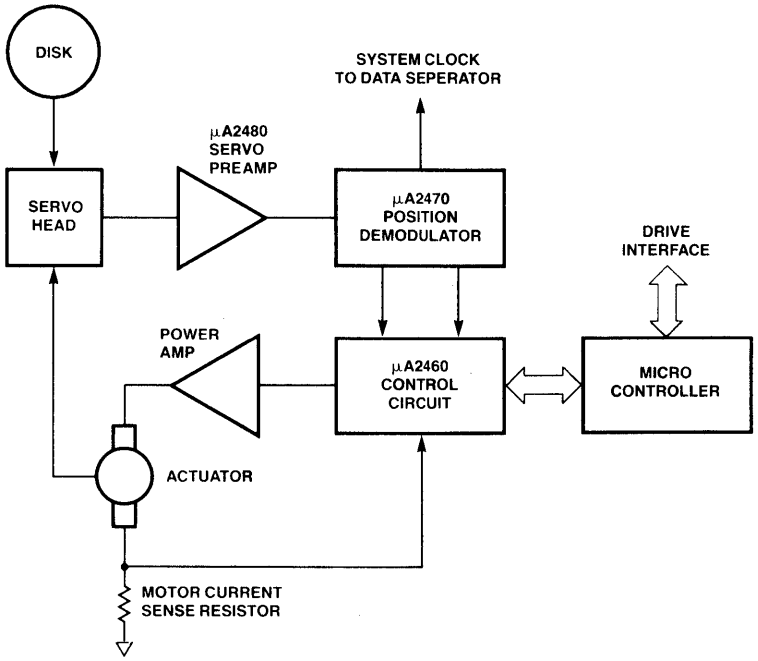
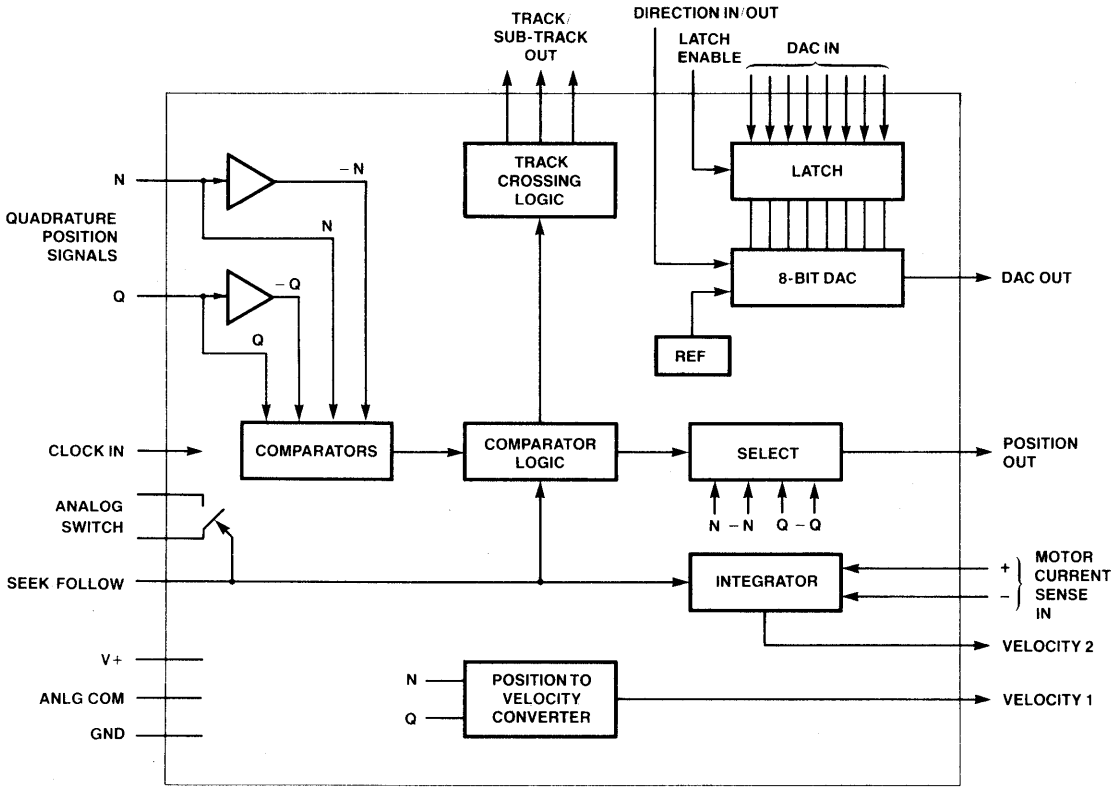


Figure 2 Block Diagram



Functional Description (Cont.)

selected position input signal until the device is switched back to Seek Mode. This implies that the switch to Follow Mode must not be made until the signal that will be the correct Position error signal for the target track is present at the output. If track centers are defined as the zero crossings of both N and Q this means that the switch to Follow Mode must be made less than one-half track away from the target track. (This is with respect to a convention of 4 track per encoder cycle, so switching must be done within 90° of the period of N or Q).

Velocity Outputs

There are two analog signal outputs representing velocity. The first, V1, is derived by differentiating the position input siganls. The entire differentiator is on chip, using switched capacitor techniques and requires no external components.

The transfer function of the differentiator is:

$$V_O = dv/dt\ (input) \times 14.3 / f\ (clock)\ Hz$$

As an example; a 10 kHz triangular signal pair into N and Q of 6.0 V peak-to-peak amplitude (dv/dt = 120kv/sec) would result in a velocity voltage output of 1.716 volts referenced to Analog Common with a clock of 1.0 MHz. The polarity will be positive if N is leading Q by 90 degrees and negative if Q is leading N. This block functions during both Seek and Follow modes.

The second velocity output is obtained by integrating a voltage proportional to the current in the motor using the following function:

$$dv/dt\ (out) = V\ (+I_{in} - -I_{in}) \times 2\times10^{-4}\ f\ (clock)\ Hz.$$

The motor current integrator output is clamped to Analog Common during Follow Mode and is released at the initiation of a seek.

Figure 6 shows a typical application set up for the Servo Control chip.

Figure 3a Track Crossing Outputs (for μA2460)

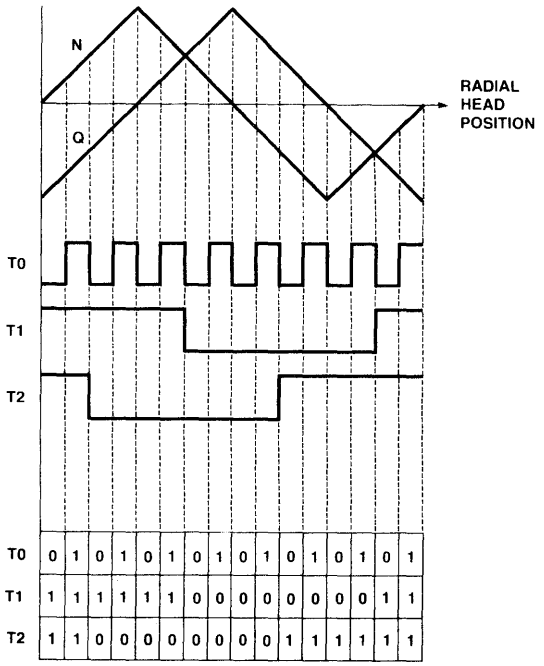


Figure 3b Track Crossing Outputs (for μA2461)

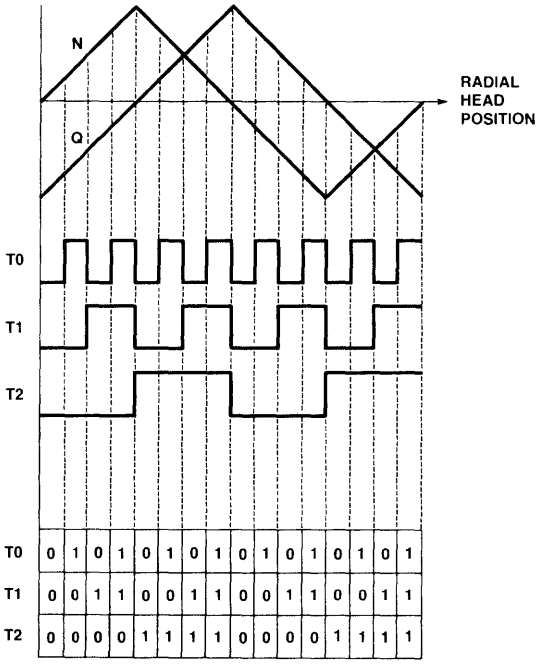


Figure 4 Typical Seek

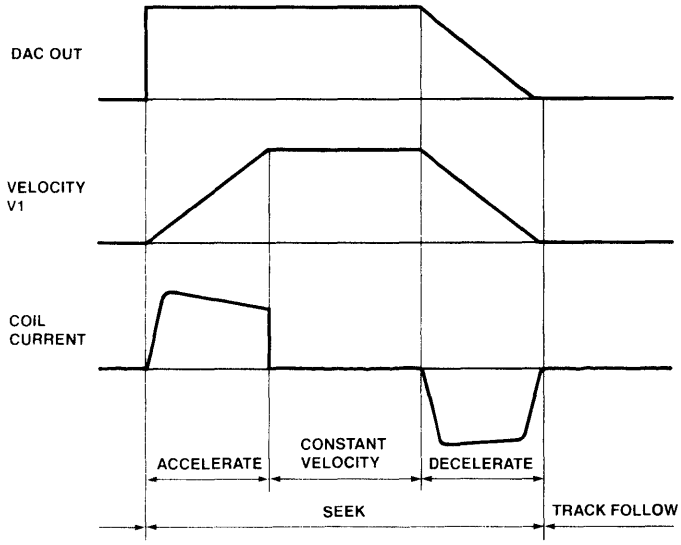


Figure 5 Position Output During Seek Mode

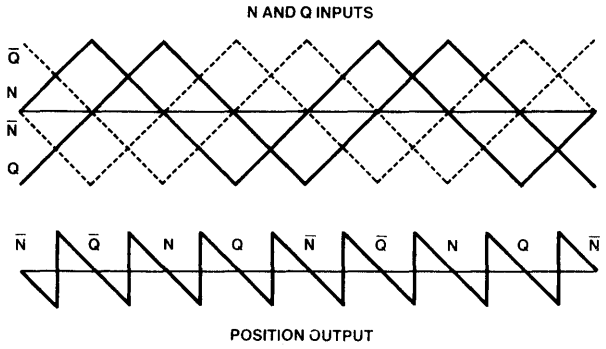
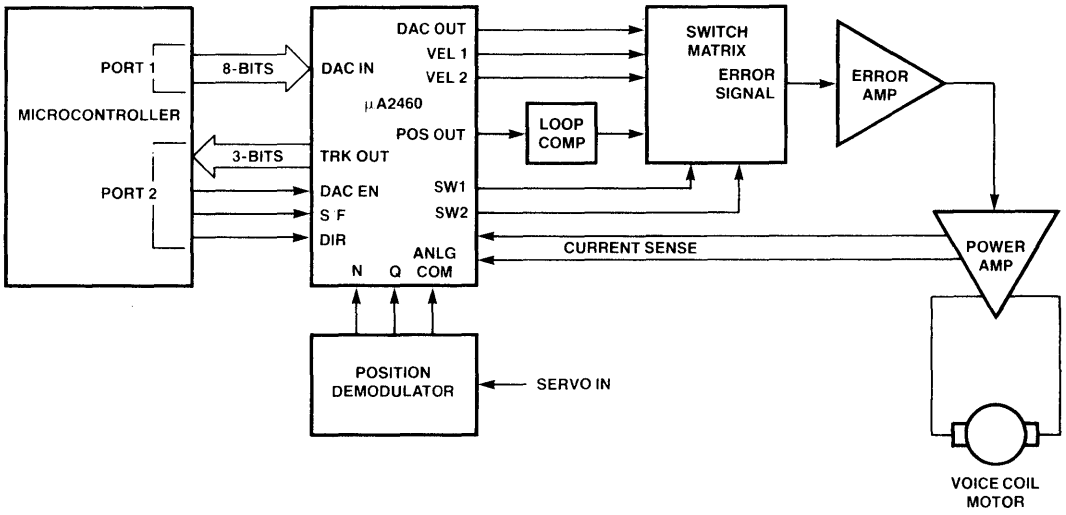


Figure 6 Typical Application Setup



μA2460, μA2461
Electrical Characteristics TA=0°C to 70°C, V_{CC}=12 V, f_{clk}=2.0 MHz, Analog Common=5.0 V unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
Digital I/O	Input Voltage LOW				0.8	V
	Input Voltage HIGH		2.0			V
	Output Voltage LOW	I_{OL} = 2.5 mA			0.45	V
	Output Voltage HIGH	I_{OH} = 40 μA	2.4			V
	Input Load Current	V_I = 0 to V_{CC}			0.2	mA
Clock Input	Input Comparator		2.0	2.5	3.0	V
	Reference Level Input Impedance		15	20		kΩ
DAC	Linearity[1]		−1		+1	LSB
	Resolution			8.0		bits
	Differential Nonlinearity		Monotonicity Guaranteed			
	Full Scale Output Voltage	Direction In High	7.25	7.35	7.45	V
		Direction In Low	2.55	2.65	2.75	V
	Zero Scale Voltage	To ½ LSB All bits ON or OFF		5.0		V
	Output Offset Voltage				±10	mV
	Settling Time[2, 4]					μs
Position Inputs	Input Voltage Range		1.0		9.0	V
	Input Impedance		15	20		kΩ
Analog Switch	On Resistance	V_{CM} = 0 to 12 V		100	200	Ω
	Off Leakage[3]			2.0	100	nA
Position Output	Output Voltage Swing	R_L = 15K Follow Mode	1.0		9.0	V
	Voltage Gain		0.9		1.1	—
	Output Offset Voltage				±20	mV
Velocity Outputs	Output Voltage Swing	R_L = 15K	1.0		9.0	V
	Output Offset Voltage V2				±20	mV
	Output Offset Voltage V1				+15	mV
I_{CC}	Positive supply	V_{CC} = 13.2 V		10	15	mA
I_{SS}	Negative supply	V_{CC} = 13.2 V	−15	−10		mA
I_{AC}	Analog Common I		−2.0	0	+2.0	mA

μA2460, μA2461
Electrical Characteristics (Cont.)

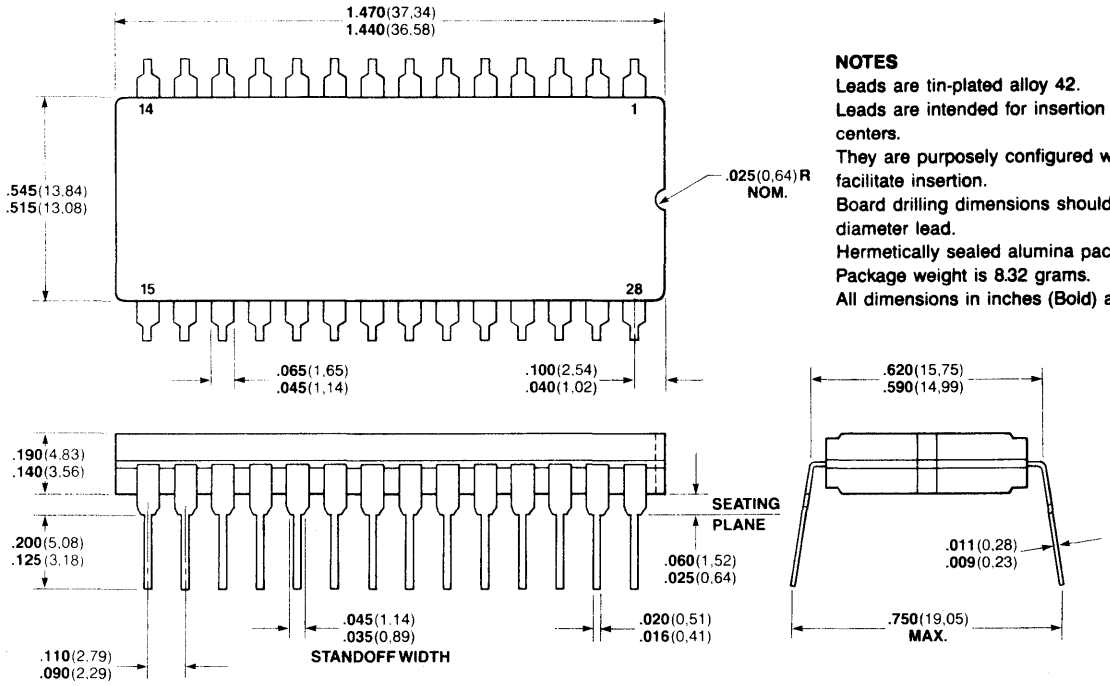
Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V1—Differentiator	Linearity	f_{clk} = 1.0 MHz to 4 MHz; $f_{N/Q} \leq$ 10 kHz		0.25		%
V2—Integrator	Linearity	f_{clk} = 1.0 MHz to 4 MHz		1.0		%

Note

1. DAC Linearity is a function of the Clock frequency; Linearity at 1.0 MHz is typically ±½ LSB.
2. DAC Settling Time is approx 5 μs, plus a delay of maximum 32 × Clock period i.e., 5 + 32 μs at Clock = 1.0 MHz Minimum could be 5μs.
3. Equivalent to 50 MΩ.
4. Guaranteed, but not tested in production.

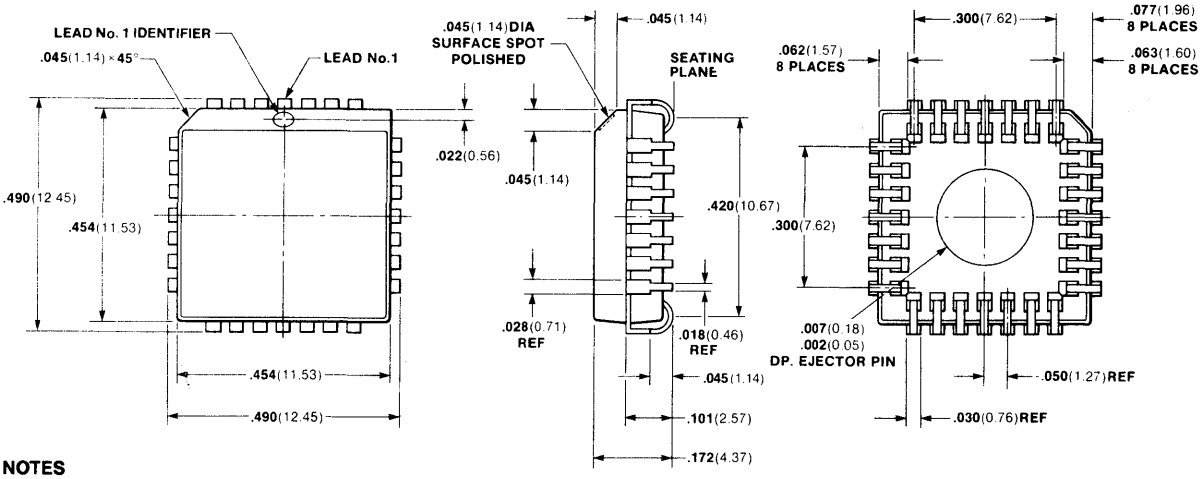
Package Outlines

28-Lead MSI Cerdip



NOTES
Leads are tin-plated alloy 42.
Leads are intended for insertion in hole rows on **.600** (15.24) centers.
They are purposely configured with "positive" misalignment to facilitate insertion.
Board drilling dimensions should equal your practice for **.020** (0.51) diameter lead.
Hermetically sealed alumina package.
Package weight is 8.32 grams.
All dimensions in inches (Bold) and millimeters (Parentheses)

28-Lead PLCC



NOTES
All tolerances are ±.003 unless otherwise noted.
The leads are solder dipped or solder plated copper alloy.
Package material is plastic.
All dimensions in inches (Bold) and millimeters (Parentheses)

Preliminary Data - March 1986

UA2470

WINCHESTER DISK POSITION DEMODULATOR

LINEAR DIVISION COMPUTER PERIPHERALS

DESCRIPTION

The UA2470 is a monolithic analog/digital integrated circuit which decodes a quadrature di-bit pattern from the dedicated servo surface of a disk file into head position, track data, and timing components. The UA2470 accepts the servo signal after amplification by a preamp such as the UA2480 and processes the various components for input to a UA2460 type servo controller. These three circuits and their external components form a disk control system for closed loop positioning applications.

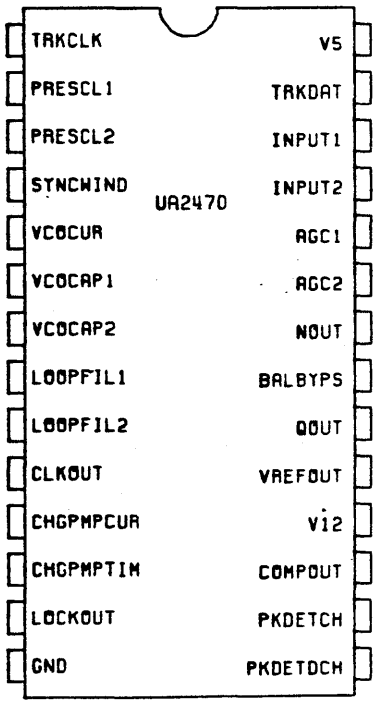
- o Quadrature Position Signals
- o Programmable Charge and Discharge in Peak Detectors
- o Sync Lock by PLL with Lock Detection Output
- o NRZ Track Data and Clock Output
- o AGC amplifier with 36Db Range
- o Servo Frame Rates to 400Khz
- o 5.0V Band Gap Reference
- o Standard 5.0V and 12.0V Power Supplies
- o Compatible with UA2480 Servo Preamp and UA2460 Servo Controller

ABSOLUTE MAXIMUM RATINGS

Vcc	6.0 Volts
V12	15.0 Volts
Operating Temperature Range	0 to 70 Deg C.
Storage Temperature Range	-65 to 150 Deg C.
Pin Temperature(Soldering, 10 Sec.)	260 Deg C.

ORDER INFORMATION

Type	Package	Code	Part No.
UA2470	Ceramic Dip	FM	UA2470DC



DESCRIPTION OF PIN FUNCTIONS

INPUT SIGNALS

PIN	NAME	FUNCTION
2 3	Prescaler LSB Prescaler MSB	Programs the Prescaler for VCO frequency relative to the frame rate. Divide ratios of 32, 64, 96, and 128 are available. Inputs are TTL Levels.
5	VCO Current	Voltage Input Sets the VCO Current.
11	Charge Pump Current	Voltage Input Sets the Current Level into the Loop Filter.
14	Ground	
18	V12	12 Volt Supply Input.
25 26	Inverting In Noninverting In	Composite Signal Inputs.
28	VCC	5 Volt Supply Input.

OUTPUTS

1	Track Clock Out	Clock Output Derived from the Sync Signal. Used as Reference for Track Data. TTL.
10	Clock Out	VCO Output. TTL.
13	Lock Out	Logic High when PLL is Locked. TTL.
17	Composite Out	AGC Amplifier Output.
19	Reference Out	5.0 Volt Reference Output. Used as reference for N and Q Outputs.
20	Q Out	Quadrature Position Output.
21	N Out	Normal Position Output.
27	Track Data	NRZ Data from Missing Sync Pulses. TTL.

EXTERNAL COMPONENTS

4	Sync Window	Oneshot Timing RC Network. Sets Length of Window used in Sync Separator.
6-7	VCO Capacitor	VCO Timing Capacitor. Sets VCO Center Frequency.
8-9	Loop Filter	PLL Loop Filter.
12	Charge Pump Time	Oneshot Timing RC Network. Sets Length of Current Pulse Out of the Phase detector.
15	Peak Detector Discharge Current	Resistor to Ground. Sets the Internal Peak Detector Discharge Current.
16	Peak Detector Charge Current	Resistor to Ground. Sets the Internal Peak Detector Charge Current.
21	Balance Bypass	Bypass Capacitor for the offset canceling circuit in the AGC Amplifier. Sets the Low Frequency Rolloff of the Amplifier.
23	AGC1	Loop Filter Capacitor for AGC Amplifier.
24	AGC2	Bypass Capacitor for AGC Amplifier.

THEORY OF OPERATION

The purpose of the UA2470 is to demodulate both analog and digital information from the composite servo signal as shown in figure 1. This signal contains the the digital signals DATA and SYNC and the analog quadrature di-bit signals N, N*, Q, and Q*.

DATA: The track data is presented as NRZ with a companion clock signal for latch control. The track data is decoded from the first pulse in each servo cell. This data permits identification of index position, guardband etc. The codes and schemes are entirely at the user's option as no decoding is done on chip.

SYNC: The sync pulse is the one pulse in the frame which is always present in every frame on every track. This pulse is used to synchronize the PLL and makes decoding the rest of the information in the frame possible.

QUADRATURE POSITION SIGNALS: The four position pulses are analog signals whose amplitude encodes the position of the disk file heads with respect to the data track centers. N and Q are in a quadrature relationship, i.e. when N and N* are equal in magnitude the difference between Q and Q* is at maximum and vice versa. Equal magnitudes of N and N* represent odd tracks and Q and Q* the even tracks.

AGC AMPLIFIER: The UA2470 AGC amplifier is a fully differential design with a typical bandwidth of 20Mhz and active offset cancelling. The composite signal input level must be between 30 and 300 millivolts to be within the amplifiers active AGC range. The offset cancelling circuit requires an external filter capacitor which incidentally provides control of the low frequency response. An external capacitor is used to control the AGC bandwidth. The AGC amplifier output amplitude is typically 3.5 volts peak to peak and is available at an output pin on the device for monitoring.

SYNC SEPARATOR: The sync separator shown in figure 2 operates on the composite signal as it appears at the output of the AGC amplifier. The hysteresis comparator has thresholds of +0.7 and 0 volts and produces pulses whose trailing edges are at the zero crossings of the composite signal. The trailing edges of these pulses trigger the oneshot. The output of the oneshot is anded with the pulse stream from the hysteresis comparator to produce the sync pulse. The pulse length from the oneshot should be long enough to enclose the next pulse in the stream only if it is the sync bit. Sync separator timing is shown in figure 3.

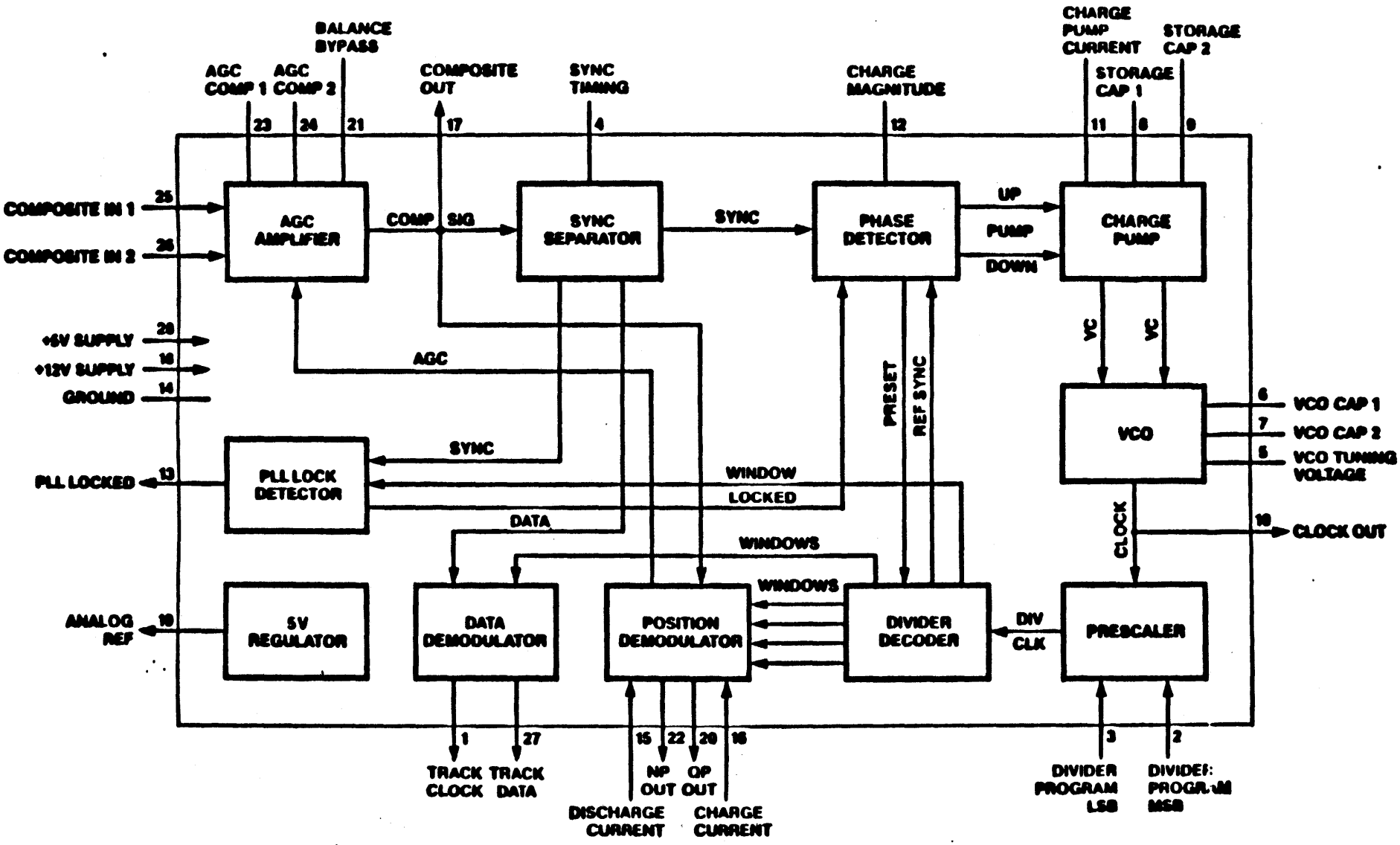
TRACK DATA DEMODULATOR: The track data encoding flip-flop changes state whenever there is a data pulse present producing NRZ data for the user.

PHASE LOCK LOOP: When a disk sync pulse is sensed by the sync separator, the PLL compares the phase of disk sync with the phase of a reference sync pulse generated by the window decoder. Refer to figure 4 and 5. Every other sync pulse from the sync separator causes the window decoder counter to preset. This This forces the decoder into phase alignment with the disk sync. Starting from a known condition allows a phase comparison to be made on the next frame by comparing the trailing edges of the reference sync with the disk sync pulses and outputing a correction signal to the charge pump to increase or decrease the VCO frequency to correct the phase error. On the next frame the cycle is repeated.

LOCK DETECTOR: When the frequency and phase of the VCO are correct, the trailing edge of the sync pulse will coincide with the trailing edge of count 4 from the counter/decoder. The decoder generates a window from the end of count 3 to the end of count 5, so that the sync edge will ideally fall in the middle. Whenever the sync falls inside the window four consecutive times, lock is detected and the Lock signal goes true. In order for the Lock signal to be reset the sync pulse must be outside the window for four consecutive frames.

POSITION DEMODULATOR: Figure 6 shows the position signals as a function of servo head position. The position demodulator consists of four digitally enabled peak detectors, two summing amplifiers and a precision band gap reference. Each of the four peak detectors is enabled by the window decoder during one of the position pulses as shown in figure 7. The N position output is derived by taking the difference between the first two peak detector outputs. The Q output is similarly obtained from the second pair. The outputs are referenced to the 5 volt reference which is available as an output to be used as an analog baseline. The charging and discharging slew rates in the peak detectors are programmable by external resistors. The charging slew rate is associated with acquisition of the peak and the discharge slew rate controls the droop rate between peaks.

Block Diagram



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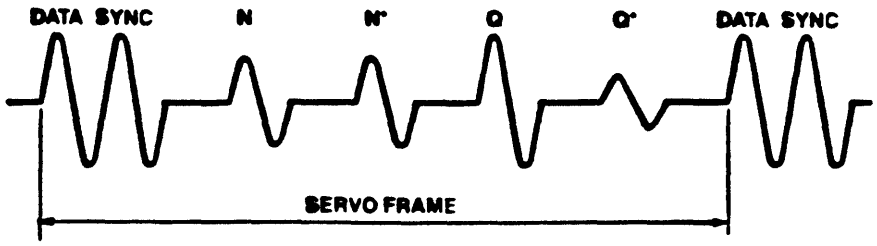


Figure 1.

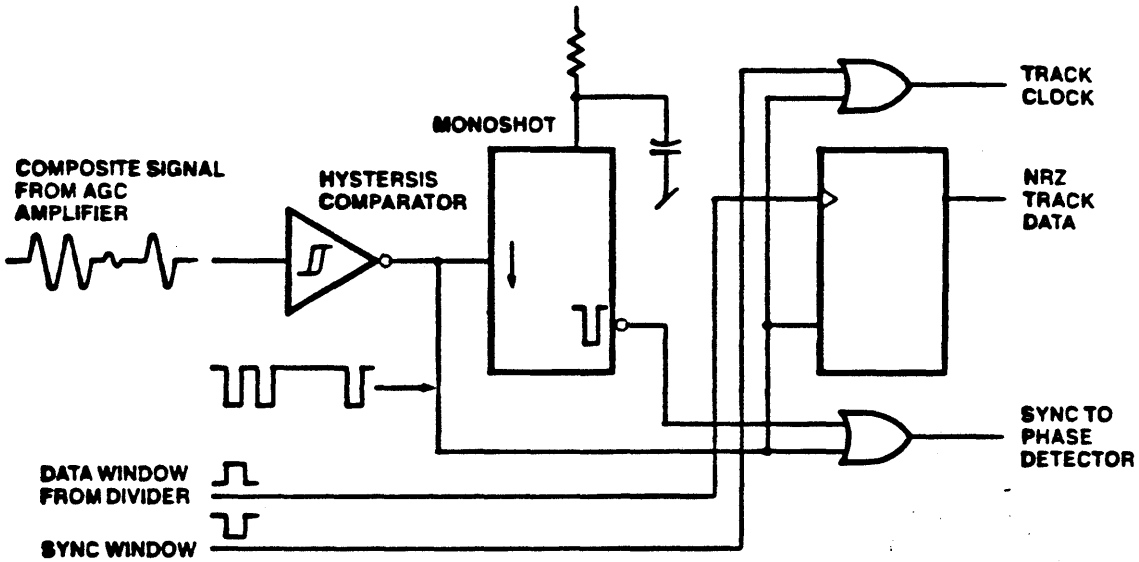


Figure 2.

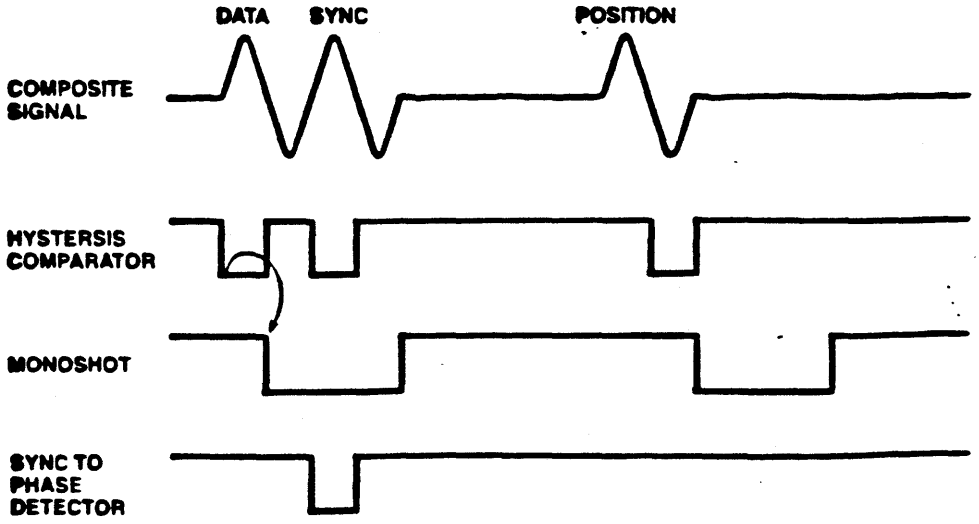


Figure 3. Sync Separator Timing

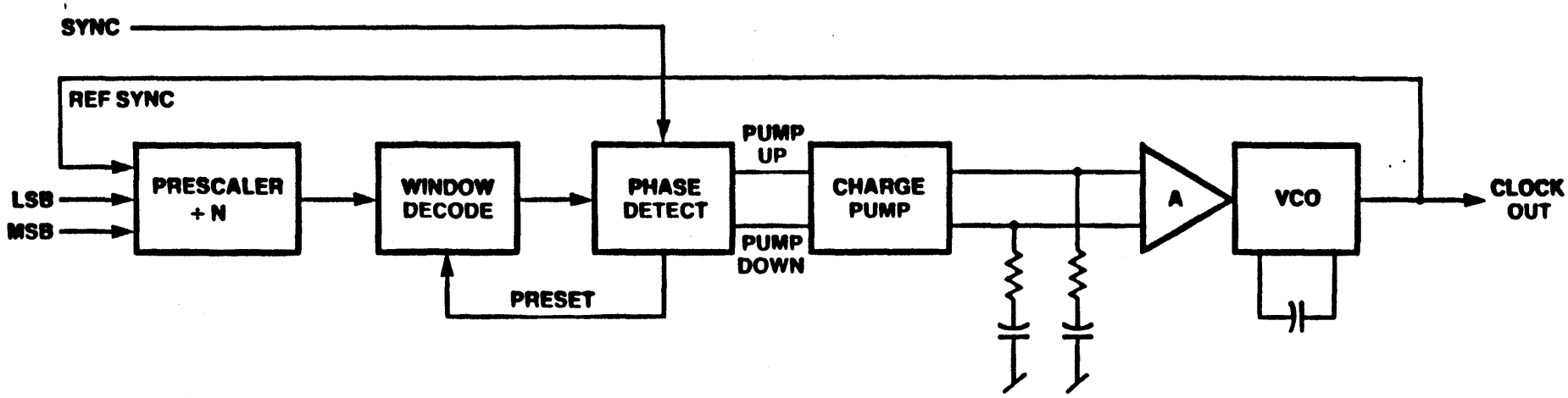


Figure 4. Phase Lock Loop Block Diagram

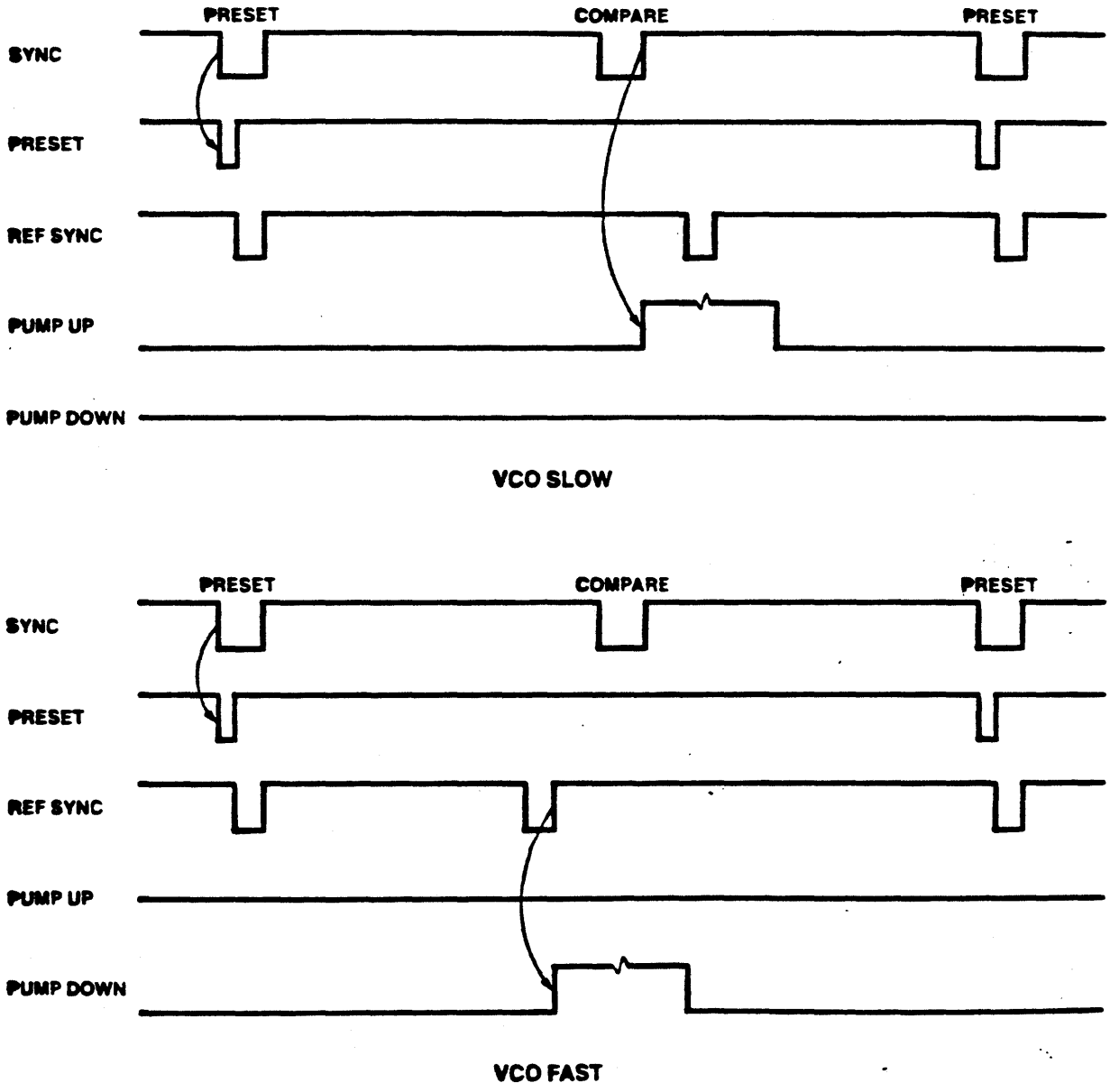


Figure 5. VCO Fast/Slow Timing Diagram

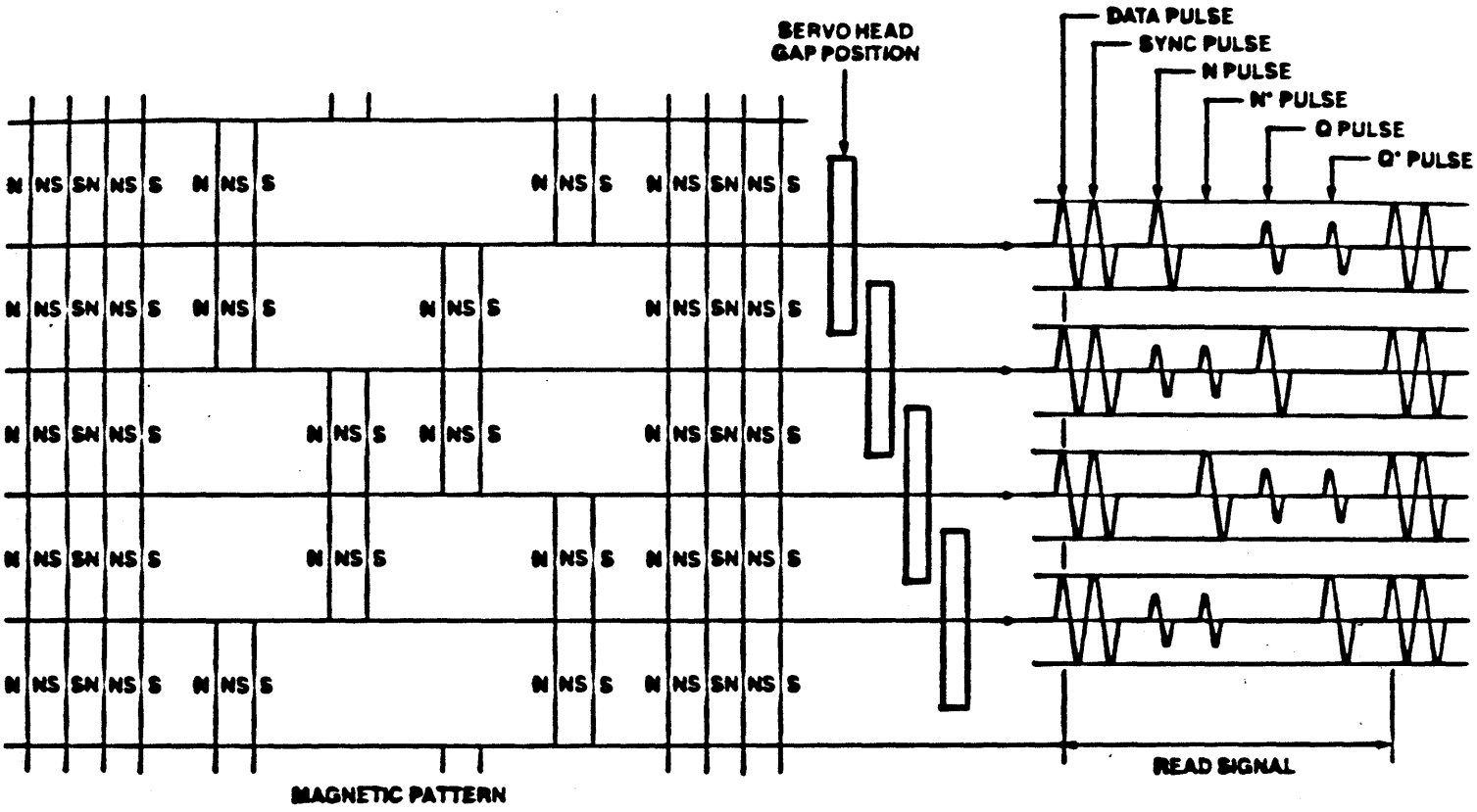


Figure 6. Magnetized Pattern of Quadrature Di-Bit Servo Signal and Read Signal

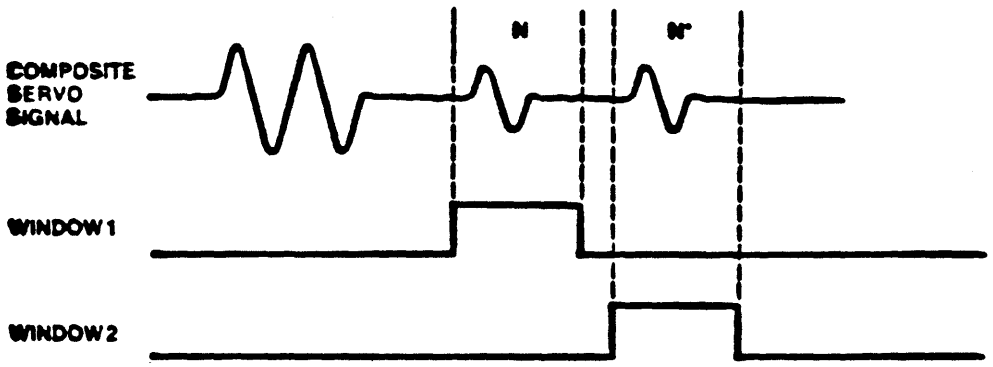


Figure 7.

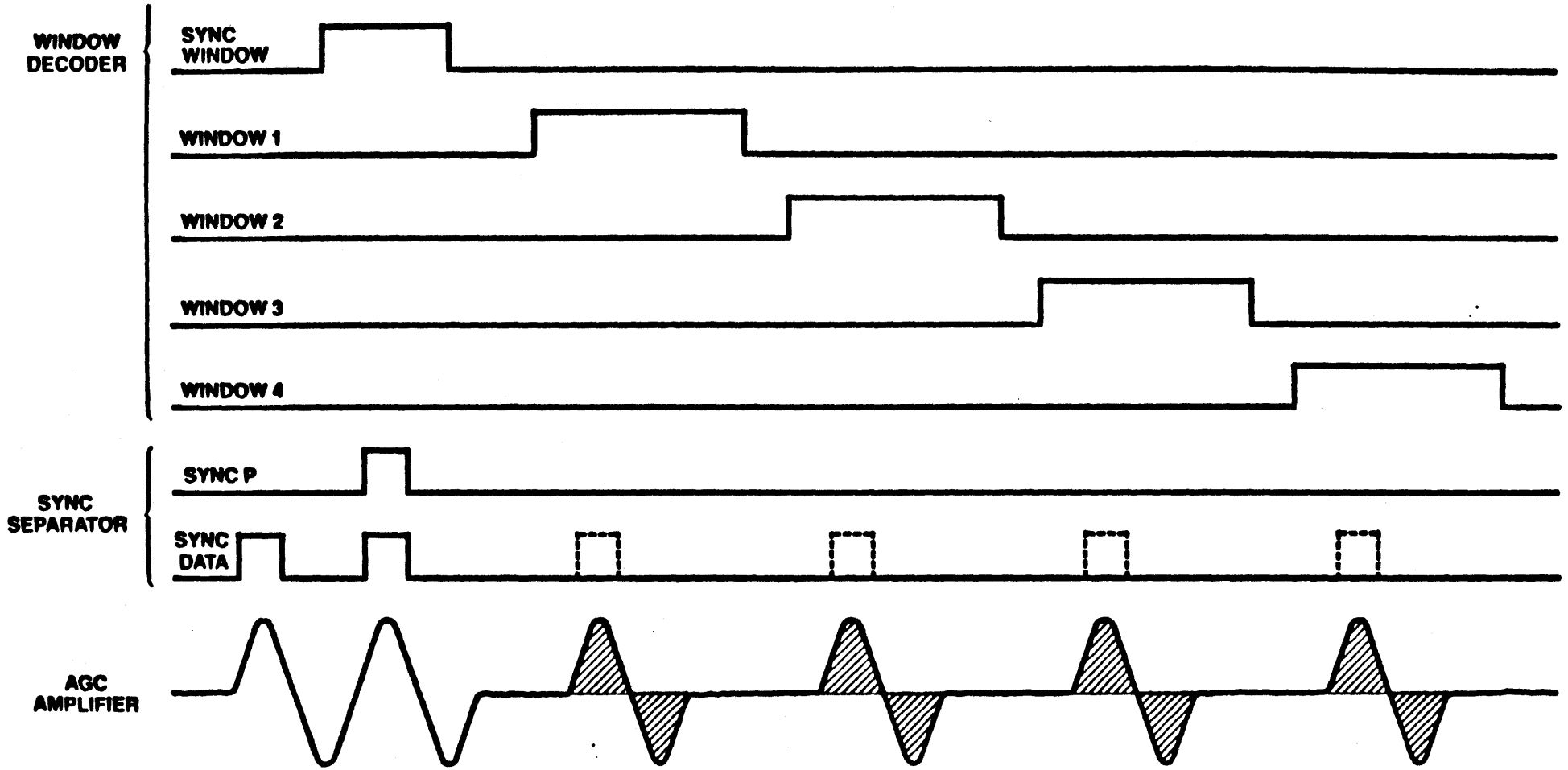
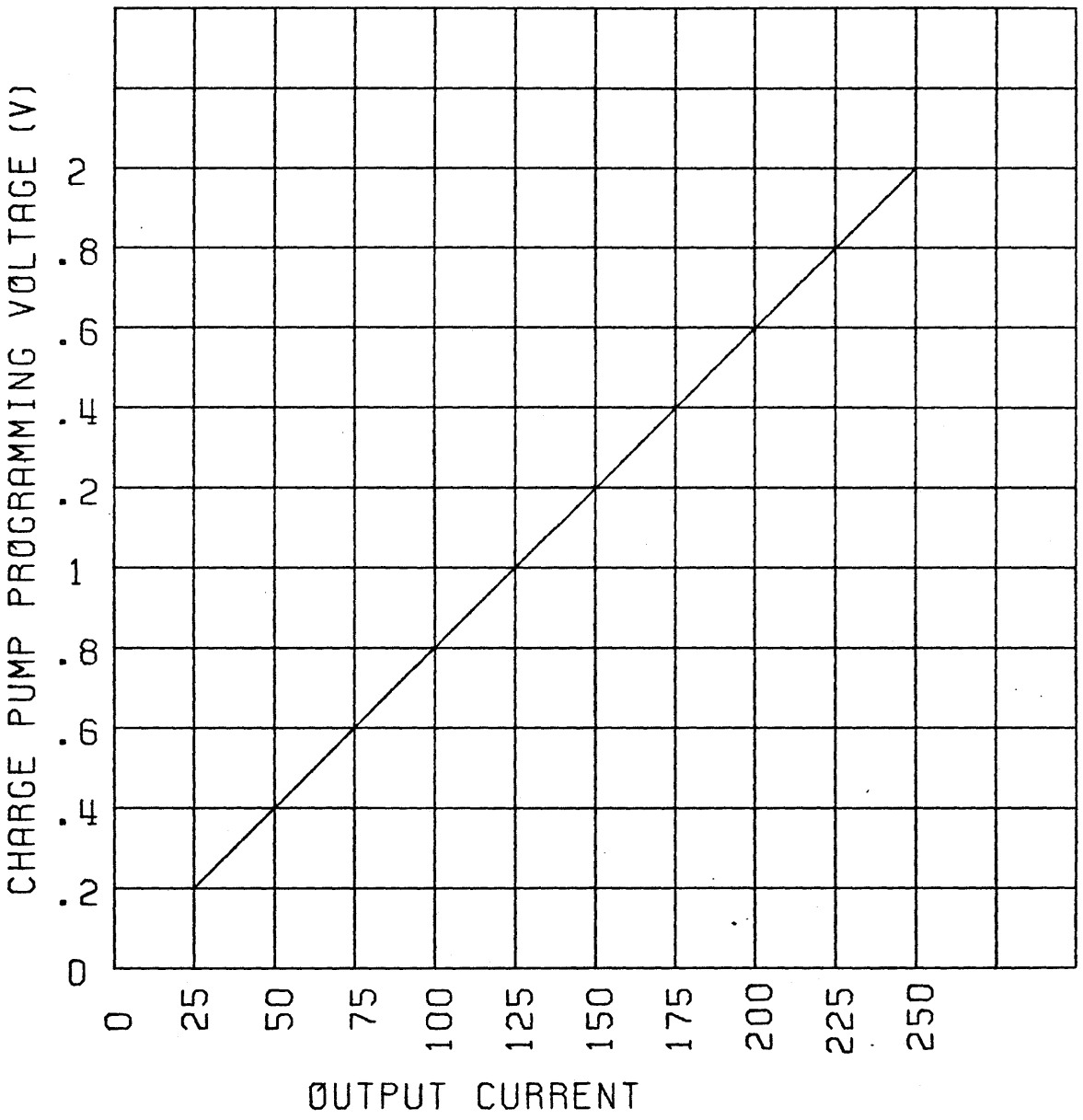

WINDOW DECODER
SYNC WINDOW
WINDOW 1
WINDOW 2
WINDOW 3
WINDOW 4
SYNC SEPARATOR
SYNC P
SYNC DATA
AGC AMPLIFIER
PLL SYNCHRONIZING EVENT
May or may not be present. Width varies.
May be present at any amplitude (from zero to sync pulse amplitude)
µA2470 TIMING DIAGRAM when Loop is locked.

Figure 8.

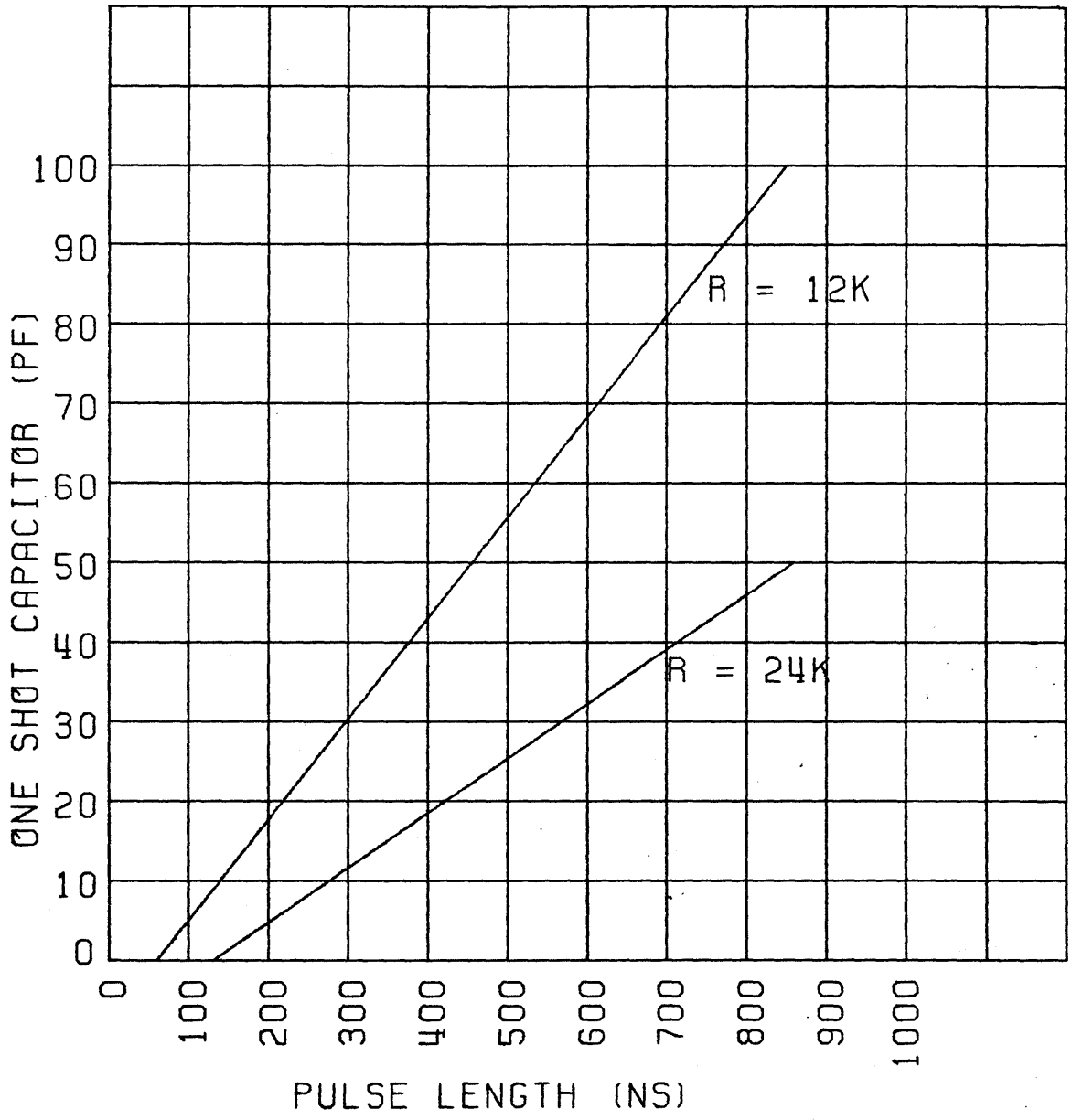
UA2470



CHARGE PUMP CURRENT VS PROGRAMMING VOLTAGE

JF 3/14/86

UA2470

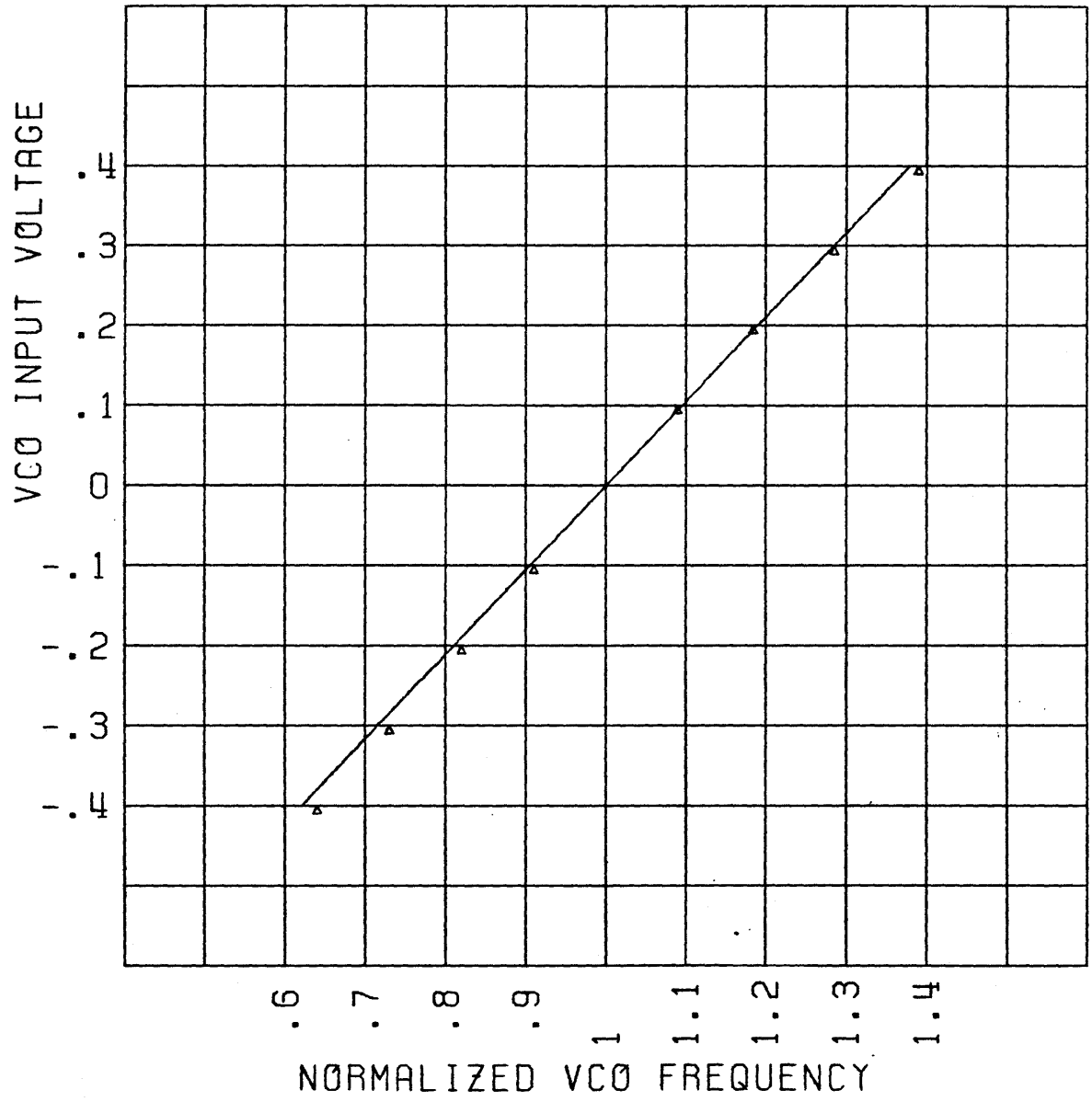


SYNC PULSE DEMODULATOR AND CHARGE PUMP

ONE-SHOT PULSE LENGTH VS. CAPICATOR VALUE

JF 3/14/86

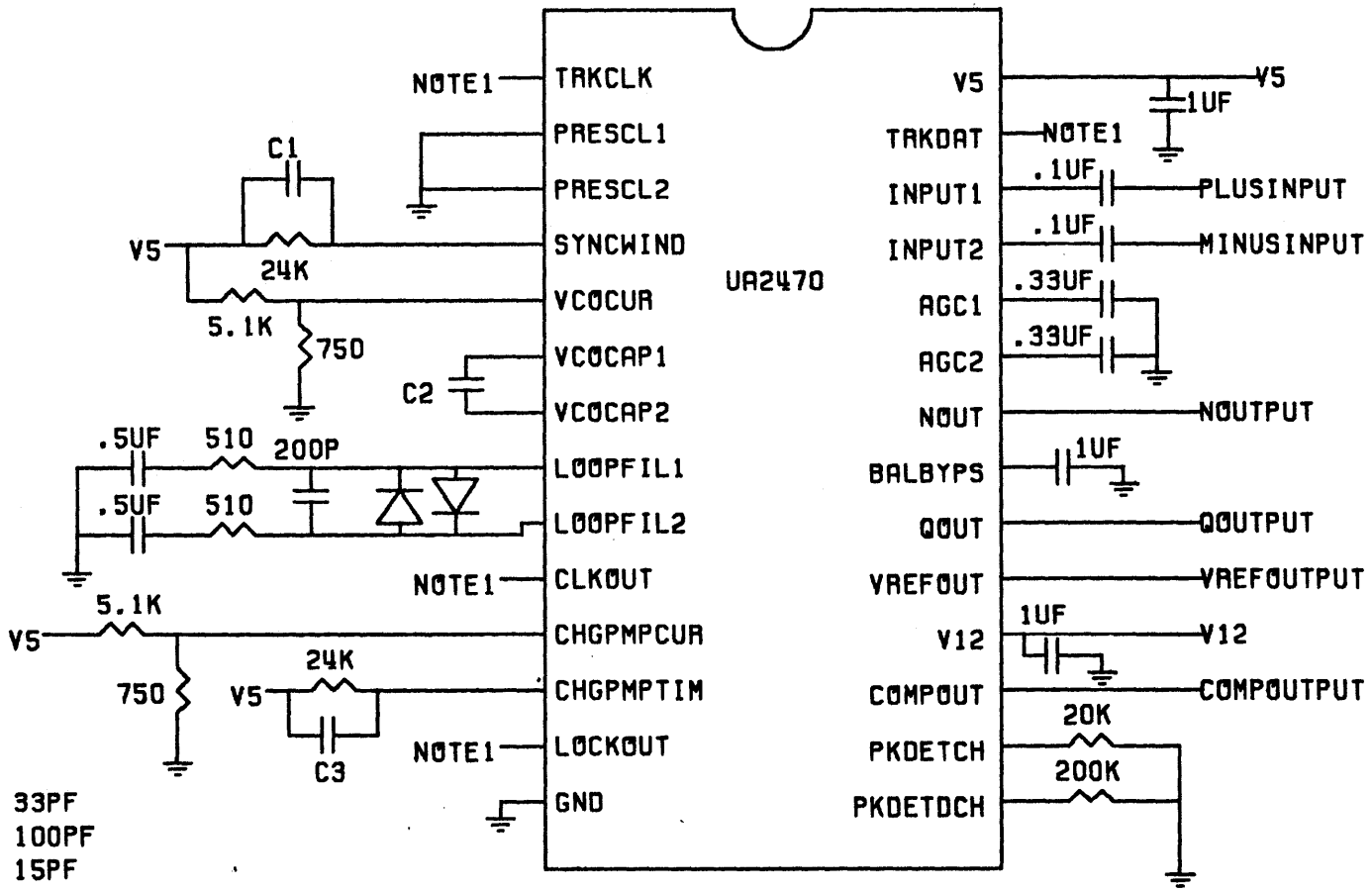
UA2470



VCO FREQUENCY VS CONTROL VOLTAGE

JF 3/14/86

TEST CIRCUIT FOR UA2470



C1 - 33PF
C2 - 100PF
C3 - 15PF
VALUES ARE FOR A FRAME FREQUENCY OF 150KHZ
SCALE LINEARLY FOR OTHER FRAME RATES

NOTE1: OPEN COLLECTOR DIGITAL OUTPUTS

FAIRCHILD
A Schlumberger Company

μA248X • μA248XR Series Winchester Disk Read/Write Preamplifiers

April 1986

Linear Division Disk Drives

Description

The μA248X/μA248XR Series High Performance Read/Write Preamplifiers are intended for use in Winchester disk drives which employ center tapped ferrite or manganese-zinc read/write heads. The circuit can interface with up to eight Read/Write heads which makes it ideal for multi-platter disk drive designs. Designed to reside in the Head/Disk Assembly (HDA) of Winchester disk drives, the Read/Write preamplifiers provide termination, gain, and output buffering for the disk heads as well as switched write current. Certain write fault conditions are detected and reported to protect recording integrity. The parts are available with internal damping resistor (μA248XR) and without internal damping resistor. (μA248X)

- **Wide Bandwidth, High Gain, Low Noise**
- **Up To Eight Read/Write Channels**
- **Internal Write Fault Condition Detection**
- **5 V & 12 V Power Supply Voltages**
- **Independent Read & Write Data Lines**
- **TTL Control And Data Logic Levels**
- **Externally Programmable Write Current**
- **Available With Internal Damping Resistor**
- **Compatible With SSI 117 Family**

Absolute Maximum Ratings

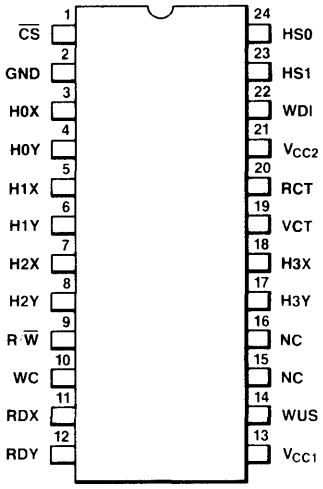
Storage Temperature Range	
Ceramic	−65°C to +175°C
Plastic	−65°C to +150°C
Operating Junction Temperature Range	25°C to 135°C
Lead Temperature	
Ceramic (soldering, 60s)	300°C
Plastic (soldering, 10s)	265°C
Internal Power Dissipation,[1,2]	
28L-Ceramic DIP	2.50 W
24L-Ceramic DIP	1.95 W
18L-Ceramic DIP	1.88 W
32L-Brazed Flatpak	1.50 W
24L-Brazed Flatpak	0.88 W
24L-Ceramic Flatpak	0.79 W
44L-Plastic LCC	1.92 W
28L-Plastic LCC	1.39 W
Supply Voltage, V_{CC1}	6.0 V
Supply Voltage, V_{CC2}	15 V
Write Current (IWC)	70 mA

Notes

1. $T_{J\ Max}$ = 150°C for the Plastic, and 175°C for the Ceramic.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 28L. Ceramic DIP at 16.7 mW/°C, the 24L-Ceramic DIP at 13.0 mW/°C, the 18L-Ceramic DIP at 12.5 m/W/°C, the 32L-Brazed Flatpak at 10.0 mW/°C, the 24L-Brazed Flatpack at 5.9 mW/°C, the 24L Ceramic Flatpak at 5.3 mW/°C, the 44L-Plastic LCC at 15.3 mW/°C, and the 28L-Plastic LCC at 11.2 mW/°C.

Connection Diagram

24-Lead DIP
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2484DC	7L	Ceramic DIP
μA2484RDC	7L	Ceramic DIP

Input Voltages

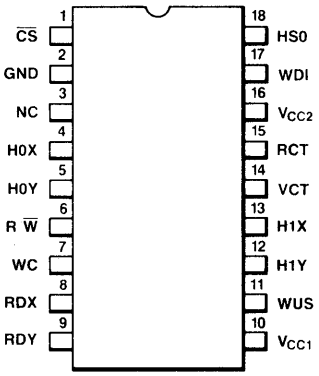
Head Select (HS0, HS1, HS2)	−0.4 V to V_{CC1} +0.3 V
Write Current (WC) Voltage in read and idle modes. (Write mode must be current limited to −70 mA)	−0.3 V to V_{CC1} +0.3 V
Chip Select (CS)	−0.4 V to V_{CC1} +0.3 V
Read/Write (R/W)	−0.4 V to V_{CC1} +0.3 V

Recommended Operating Conditions

V_{CC1}	5.0 V
V_{CC2}	12 V

Fairchild Semiconductor Corporation, Linear Division
313 Fairchild Drive, Mountain View, California 94042
(415) 962-4011 TWX MVLD

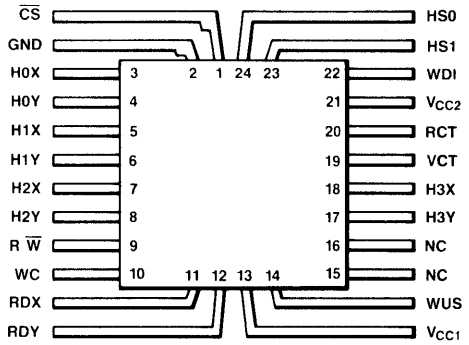
Connection Diagram
18-Lead DIP
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2482DC	FU	Ceramic DIP
μA2482RDC	FU	Ceramic DIP

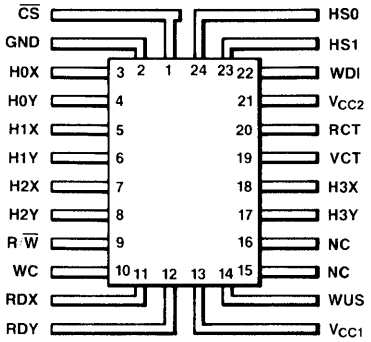
Connection Diagram
24-Lead Cerpak
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2484FC	FN	Ceramic Flatpak
μA2484RFC	FN	Ceramic Flatpak

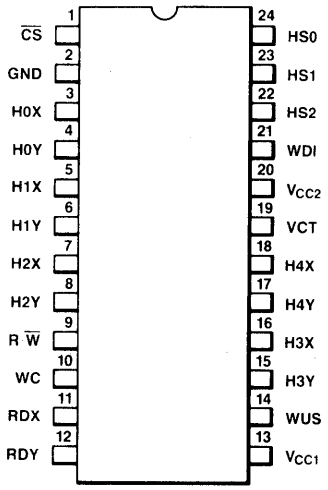
Connection Diagram
24-Lead Flatpak
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2484GC	FR	Brazed Flatpak
μA2484RGC	FR	Brazed Flatpak

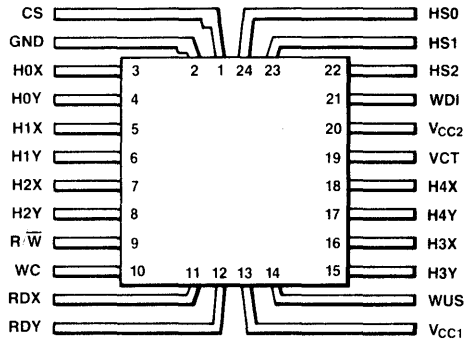
Connection Diagram
24-Lead DIP
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2485DC	7L	Ceramic DIP
μA2485RDC	7L	Ceramic DIP

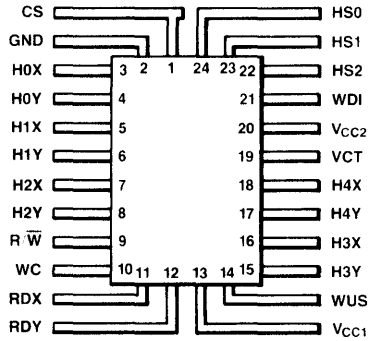
Connection Diagram
24-Lead Cerpak
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2485FC	FN	Ceramic Flatpak
μA2485RFC	FN	Ceramic Flatpak

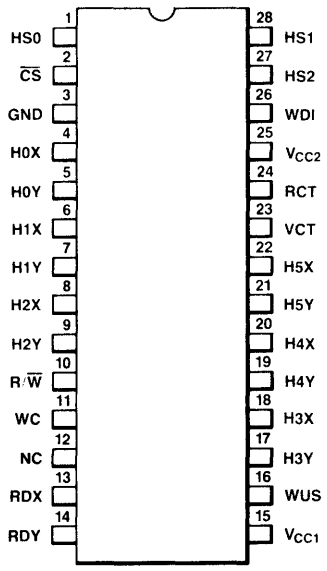
Connection Diagram
24-Lead Flatpak
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2485GC	FR	Brazed Flatpak
μA2485RGC	FR	Brazed Flatpak

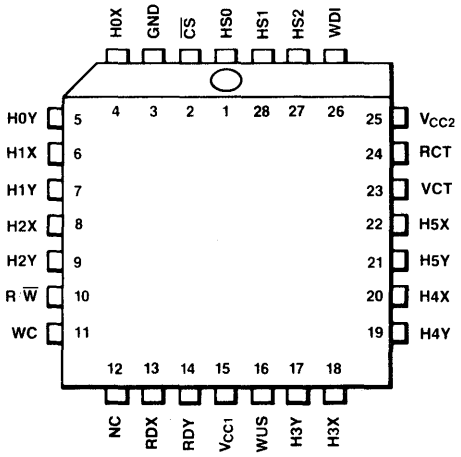
Connection Diagram
28-Lead DIP
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2486DC	FM	Ceramic DIP
μA2486RDC	FM	Ceramic DIP

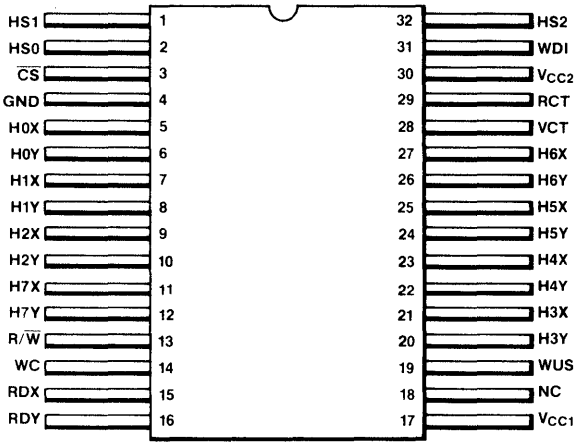
Connection Diagram
28-Lead PLCC
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2486QC	KH	Plastic LCC
μA2486RQC	KH	Plastic LCC

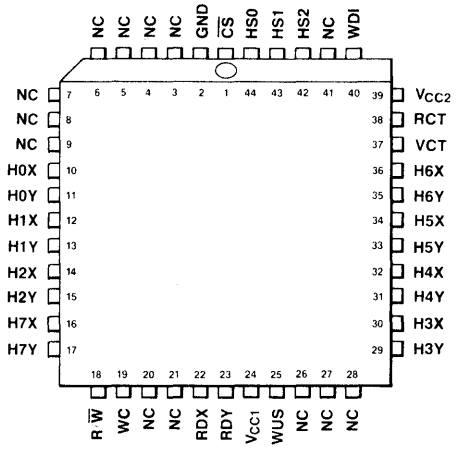
Connection Diagram
32-Lead Flatpak
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2488GC	FS	Brazed Flatpak
μA2488RGC	FS	Brazed Flatpak

Connection Diagram
44-Lead PLCC
(Top View)



Order Information

Device Code	Package Code	Package Description
μA2488QC	KI	Plastic LCC
μA2488RQC	KI	Plastic LCC

Functional Description

In the Write mode, the μA248X/μA248XR Series accepts TTL compatible write data pulses on the WDI lead. On the falling edge of each write data pulse, a current transition is made in the selected head. Head selection is accomplished via TTL input signals: HS0, HS1, HS2 (*see Table B*). Internal circuitry senses the following conditions:

1. Absense of data transitions.
2. Open circuit head connection.
3. Absence of write current.
4. Short circuit head connection.
5. Idle or read mode.

Any or all of the above conditions would result in a high level on the write unsafe (WUS) output signal.

During read operations, the μA284X amplifies the differential voltages appearing across the selected R/W head lead and applies the amplified signal differentially to data lines RDX and RDY.

Description of Lead Functions

Lead	Name	Description of Functions
$\overline{CS}$	Chip Select	Chip Select High disables the read/write function of the device and forces idle mode. (TTL)
R/$\overline{W}$	Read/Write Select	A Logic high places the devices in read mode and a Logic low forces write mode. *Refer to Table A.* (TTL)
HOX, Y Through H7X, Y	Read Write Head Connections	The μA2488 has eight pairs of read/write connections. The X and Y phases are made consistent with the read output, RDX and RDY, phases. (Differential)
RDX, Y	Read Data Outputs	The chip has one pair of read data outputs which is multiplexed to the appropriate head connections. (Differential)
HS0 through HS2	Head Select Inputs	The eight read/write heads are addressed with the head select inputs. *Refer to Table B.* (TTL)
WC	Write Current Input	This lead sets the current level for the write mode. An external resistor is connected from this lead to ground, and write current is determined by the value of this resistor divided into the write current constant, K which is typically 140 V.
WDI	Write Data Input	The write data input toggles the write current between the X and Y selected head connections. Write current is switched on the negative edge of WDI. The initial direction for write current is the X side of the switch and is set upon entering read or idle mode. (TTL)
RCT	Resistor Center Tap	In some versions (determined by lead availability) of the μA248X series, a resistor may be connected between RCT and V_{CC2} to reduce internal power dissipation. If this resistor is not used, RCT must be connected externally to V_{CC2}.
VCT	Center Tap Voltage	The center tap output provides bias voltage for the head inputs in read and write mode. It should be connected to the center tap of the read/write heads.
WUS	Write Unsafe	A high logic level at the write unsafe output indicates a fault condition during write. Write unsafe will also be high during read and idle mode. (Open collector)

Operating Modes

Chip Select $\overline{CS}$	Read/Write R/$\overline{W}$	Mode
1	X	Idle
0	1	Read
0	0	Write

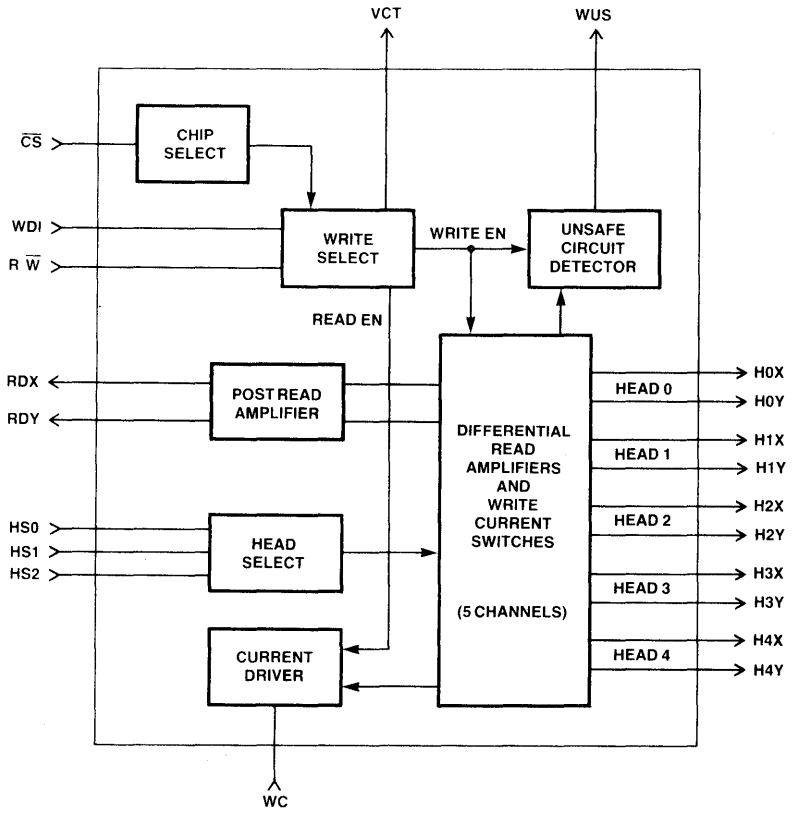
Head Selection

HS0	HS1	HS2	Head Selected[1]
0	0	0	0
1	0	0	1
0	1	0	2
1	1	0	3
0	0	1	4
1	0	1	5
0	1	1	6
1	1	1	7

Note:

1. If selected head is beyond the capacity of the μA248X model, the open input condition on the selected input will be reported as an unsafe level at the WUS output.

Block Diagram (Typical, μA248X)



Absolute Maximum Ratings All voltages referenced to GND

Symbol	Characteristic		Value	Unit
V_{DD1}	DC Supply Voltage		−0.3 to +14	V
V_{DD2}			−0.3 to +14	V
V_{CC}			−0.3 to +6.0	V
V_{in}	Digital Input Voltage Range		−0.3 to V_{CC} +0.3	V
V_H	Head Port Voltage Range		−0.3 to V_{DD} +0.3	V
V_{wus}	WUS Port Voltage Range		−0.3 to +14	V
I_W	Write Current		60	mA
I_O	Output Current	RDX, RDY	−10	mA
		VCT	−60	
		WUS	+12	

Recommended Operating Conditions

Symbol	Characteristic	Value	Unit
V_{DD1}	DC Supply Voltage	12 ± 10%	V
V_{DD2}		6.5 to V_{DD1}	V
V_{CC}		5.0 ± 10%	V
Lh	Head Inductance	5.0 to 15	μH
RD	Damping Resistor (External)	500 to 2000	Ω
RCT	RCT Resistor	90 ± 5.0% (½ watt)	Ω
IW	Write Current	25 to 50	mA
I_O	RDX, RDY Output Current	0 to 100	μA

DC Characteristics 25°C ≤ T_J ≤ 125°C V_{DD1} = 12 V, V_{CC} = 5.0 V, Unless otherwise specified

Symbol	Characteristic		Condition		Min	Max	Unit
V_{CC}	Supply Current		Read/Idle Mode			25	mA
			Write Mode			30	
V_{DD}	Supply Current		Idle Mode			25	mA
			Read Mode			50	
			Write Mode			30 + IW	
P_C	Power Consumption		T_J = 125°C	Idle Mode		400	mW
				Read Mode		600	
				Write Mode, IW = 50 mA, RCT = 90Ω		850	
				Write Mode, IW = 50 mA, RCT = 0 Ω		1050	
V_{IL}	Digital Inputs:	Input Voltage LOW			−0.3	0.8	V
V_{IH}		Input Voltage HIGH			2.0	V_{CC} + 0.3	V
I_{IL}		Input Current LOW	V_{IL} = 0.8 V		−0.4		mA
I_{IH}		Input Current HIGH	V_{IH} = 2.0 V			100	µA
V_{OL}	WUS Output		I_{OL} = 8.0 mA			0.5	V
I_{OH}			V_{OH} = 5.0 V			100	µA
V_{CT}	Center Tap Voltage		Read Mode		4.0 (typ)		V
			Write Mode		6.0 (typ)		V

Write Characteristics V_{DD1} = 12 V, V_{CC} = 5.0, IW = 45 mA, Lh = 10 µH, f(Data) = 5.0 MHz, CL (RDX, RDY) ≤ 20 pF, $R_{D\ EXT}$ = 750 Ω, or $R_{D\ INT}$. Unless otherwise specified.

Characteristic	Condition	Min	Max	Unit
Write Current Range		10	50	mA
Write Current Constant "K"		133	147	V
Differential Head Voltage Swing		5.7		V (pk)
Unselected Diff. Head Current			2.0	mA (pk)
Differential Output Capacitance			15	pF
Differential Output Resistance	Without Internal Resistors	10K		Ω
	With Internal Resistors	538	1.0K	
WDI Transition Frequency	WUS = I_{OW}			kHz
I_{wc} to Head Current Gain		18 (typ)		mA/mA

Read Characteristics V_{DD1} = 12 V, V_{CC} = 5.0 V, Lh = 10 μH, f (Data) = 5.0 MHz, CL (RDX, RDY) ≤ 20 pF, (V_{in} is referenced to V_{CT}), $R_{D\ EXT}$ = 750 Ω, or $R_{D\ INT}$. Unless otherwise specified.

Characteristic	Condition		Min	Max	Unit
Differential Voltage Gain	V_{in} = 1.0 mVp−p at 300 kHz RL (RDX), RL (RDY) = 1.0 kΩ		80	120	V/V
Dynamic Range	Input Voltage, V_I, Where Gain Falls by 10%. V_{in} V_I + 0.5 m V_{p-p} at 300 kHz		−2.0	+2.0	mV
Bandwidth (−3db)	I Zs I < 5.0 Ω, V_{in} = 1.0 mV_{p-p}		30		MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0			2.1	nV/√Hz
Differential Input Capacitance	f = 5.0 MHz			23	pF
Differential Input Resistance	f = 5.0 MHz	Without Internal Resistors	2K		Ω
		With Internal Resistors	440	850	
Input Bias Current				45	μA
Common Mode Rejection Ratio	V_{CM} = V_{CT} + 100 mV_{p-p} at 5.0 MHz		50		db
Power Supply Rejection Ratio	100 m V_{p-p} at 5.0 MHz on V_{DD1}, V_{DD2}, or V_{CC}		45		db
Channel Separation	Unselected Channels: V_{in} = 100 mV_{p-p} at 5.0 MHz and Selected Channel: V_{in} = 0 mV_{p-p}		45		db
Output Offset Voltage			−480	+480	mV
Common Mode Output Voltage			5.0	7.0	V
Single Ended Output Resistance	f = 5.0 MHz			35	Ω
Internal Damping Resistor			560	1070	Ω

Switching Characteristics V_{DD1} = 12 V, V_{CC} = 5.0 V, T_J = 25°C, I_W = 45 mA, Lh = 10 μH, f (Data) = 5.0 MHz, $R_{D\ EXT}$ = 750 Ω, or $R_{D\ INT}$. Unless otherwise specified.

Symbol	Characteristic	Condition	Min	Max	Unit
R/$\overline{W}$	R/$\overline{W}$ to Write	Delay to 90% of Write Current		1.0	μs
	R/$\overline{W}$ to Read	Delay to 90% of 100 mV 10 MHz Read Signal Envelope or to 90% Decay of Write Current		1.0	μs
$\overline{CS}$	$\overline{CS}$ to Select	Delay to 90% of Write Current or to 90% of 100 mV 10 MHz Read Signal Envelope		1.0	μs
	$\overline{CS}$ to Unselect	Delay to 90% Decay of Write Current		1.0	
HS0 HS1 HS2	to any Head	Delay to 90% of 100 mV 10 MHz Read Signal Envelope		1.0	μs
WUS	Safe to Unsafe — TD1	I_w = 50 mA	1.6	8.0	μs
	Unsafe to Safe — TD2	I_w = 20 mA		1.0	

Figure 1 Head Current Timing

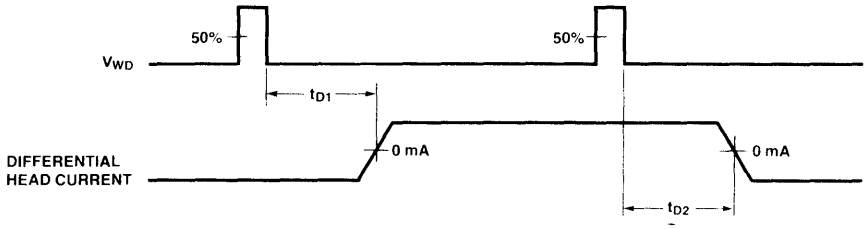


Figure 2a Unsafe to Safe Timing

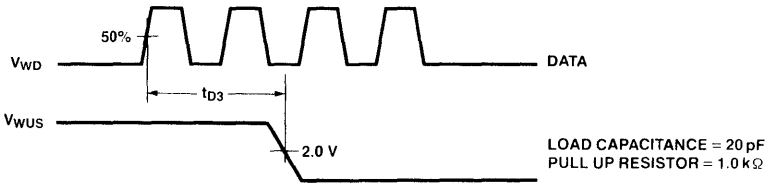
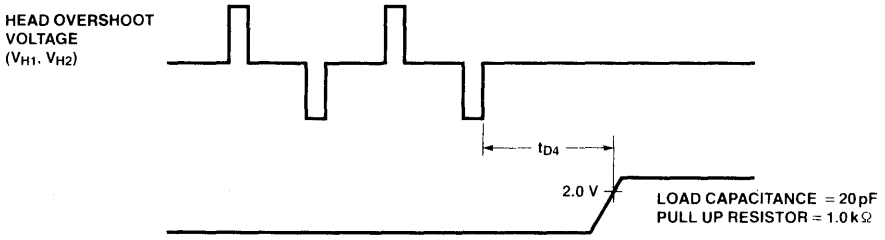
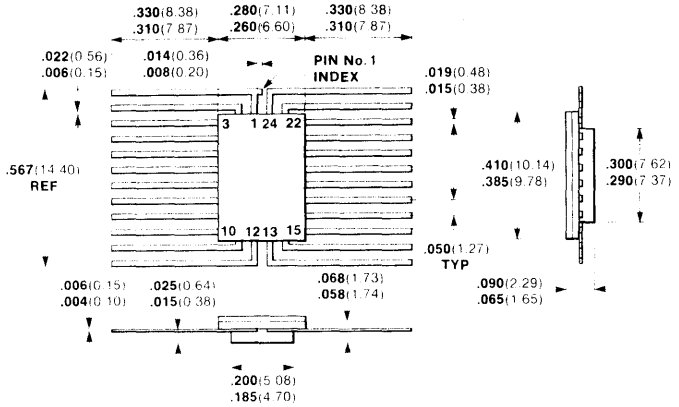


Figure 2b Safe to Unsafe Timing



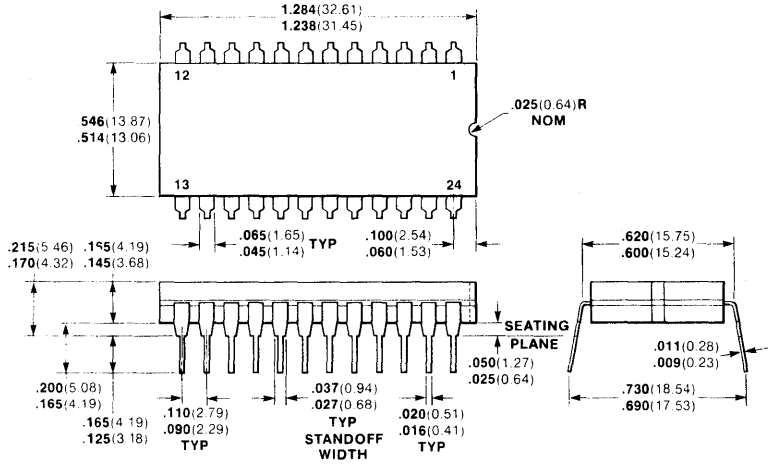
Package Outlines

24-Lead Flatpak



NOTES
Leads are gold plated alloy 42.
If solder-dipped leads are used, the maximum limits for these dimensions may be increased by **.003** (0.08).
Package weight is 0.53 grams.
Dimensions are in inches (Bold) and millimeters (Parentheses)

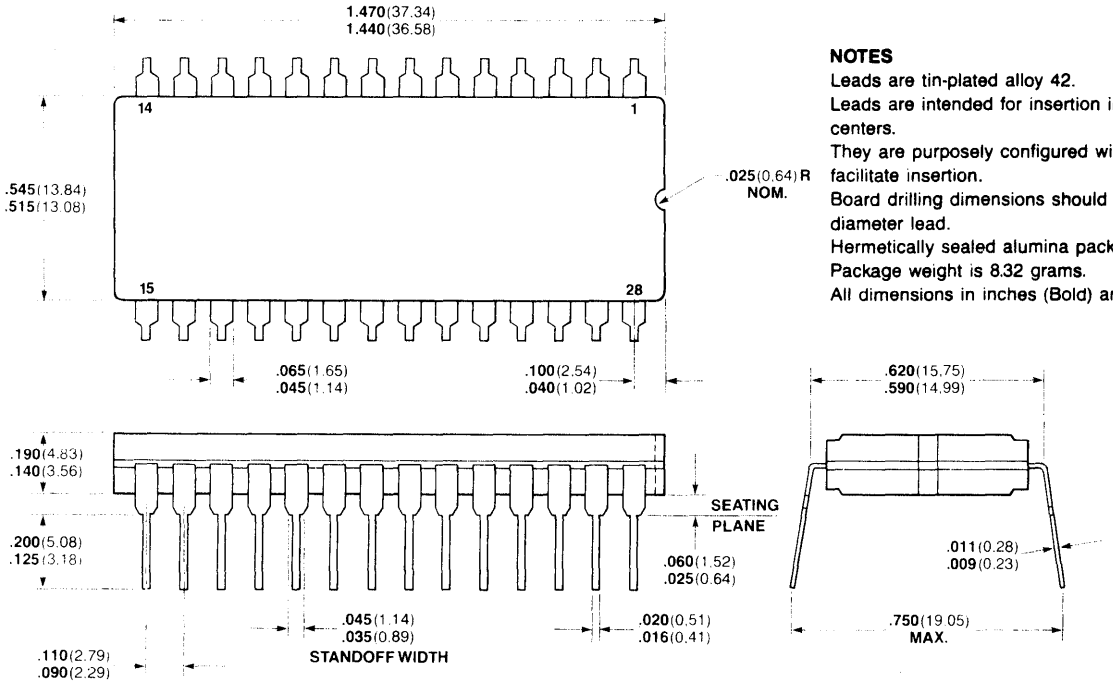
24-Lead DIP



NOTES
Leads are tin-plated alloy 42.
Leads are intended for insertion in hole rows on **.600** (15.24) centers.
They are purposely configured with "positive" misalignment to facilitate insertion.
Board drilling dimensions should equal your practice for **.020** (0.51) diameter lead.
Hermetically sealed alunina package.
Base cavity metallization is gold.
Package weight is 7.1 grams.
All dimensions are inches (Bold) and millimeters (Parentheses)

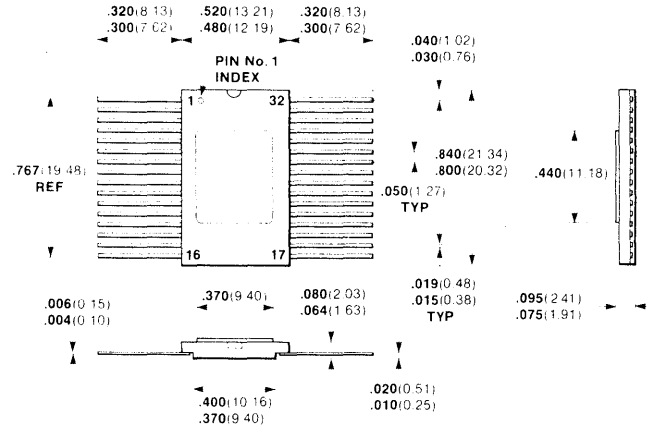
Package Outlines (Cont.)

28-Lead DIP



NOTES
Leads are tin-plated alloy 42.
Leads are intended for insertion in hole rows on **.600** (15.24) centers.
They are purposely configured with "positive" misalignment to facilitate insertion.
Board drilling dimensions should equal your practice for **.020** (0.51) diameter lead.
Hermetically sealed alumina package.
Package weight is 8.32 grams.
All dimensions in inches (Bold) and millimeters (Parentheses)

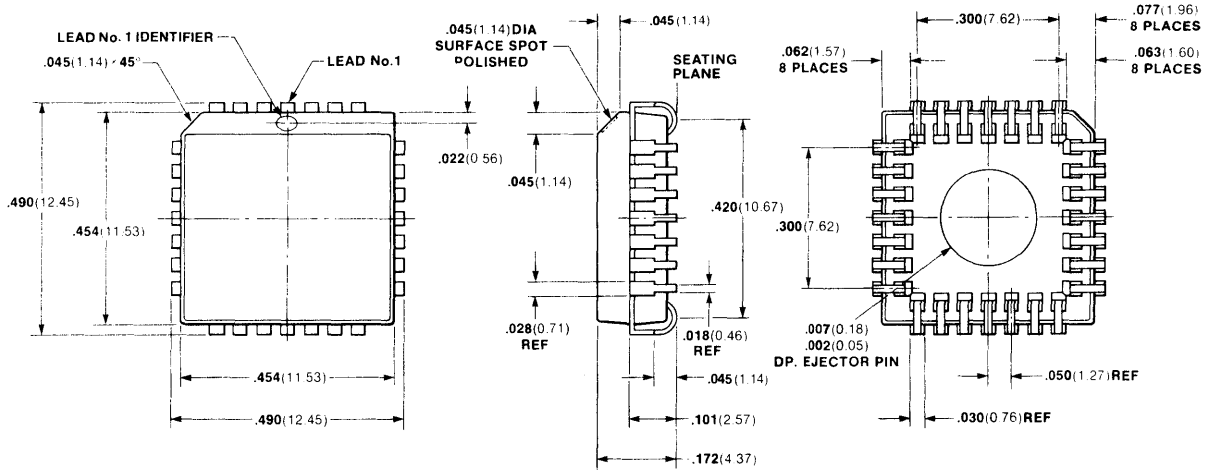
32-Lead Flatpak



NOTES
Leads are gold plated alloy 42.
If solder-dipped leads are used, the maximum limits for these dimensions may be increased by **.003** (0.08).
Package weight is 1.97 grams.
All dimensions are in inches (Bold) and millimeters (Parentheses)

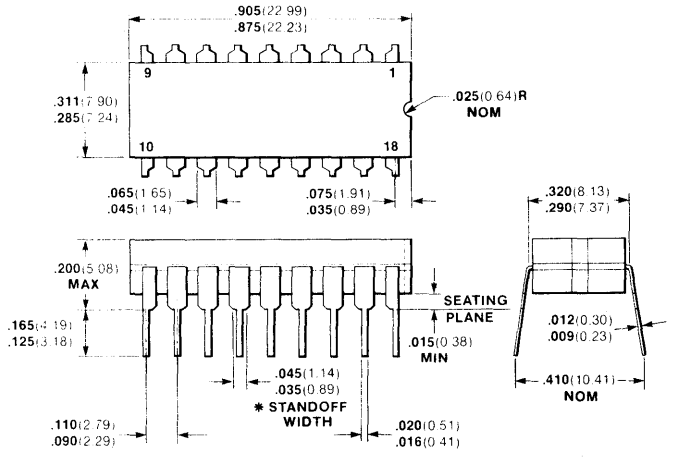
Package Outlines (Cont.)

28-Lead PLCC



NOTES
All tolerances are ±.003 unless otherwise noted.
The leads are solder dipped or solder plated copper alloy.
Package material is plastic.
All dimensions in inches (Bold) and millimeters (Parentheses)

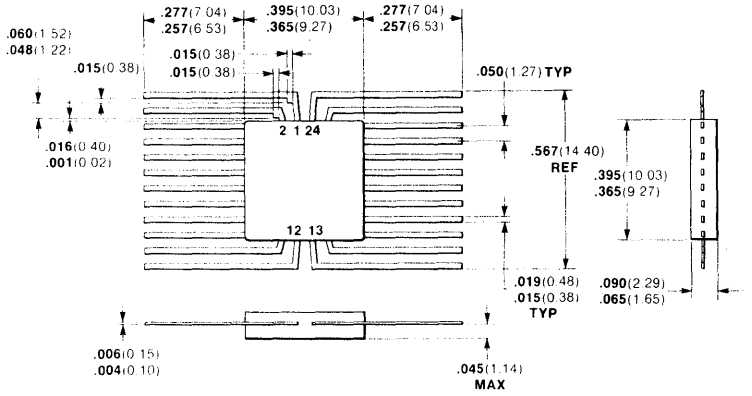
18-Lead DIP



NOTES
Leads are tin-plated alloy 42.
Leads are intended for insertion in hole rows on **.300** (7.62) centers.
They are purposely configured with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 (0.51) diameter lead.
Hermetically sealed alumina package.
*The **.035–.045** (0.89–1.14) dimension does not apply to the corner leads.
Package weight is 2.6 grams.
All dimensions are in inches (Bold) and millimeters (Parentheses)

Package Outlines (Cont.)

24-Lead Flatpak



NOTES
Leads are tin-plated alloy 42.
Increase maximum limits by **.003** (0.08) if leads are solder dipped.
Package weight is 0.68 grams.
All dimensions in inches (Bold) and millimeters (Parentheses)

FAIRCHILD

A Schlumberger Company

μA2480 Winchester Disk Servo Preamplifier

Linear Products

Description

The μA2480 provides termination, gain, and impedance buffering for the servo read head in Winchester disk drives. It is a differential input, differential output design with fixed gain of approximately 100. The bandwidth is guaranteed greater than 10 mHz.

The internal design of the μA2480 is optimized for low input noise voltage to allow its use in low input signal level applications. It is offered in 8-pin mini dip (plastic) or 10-lead flatpack suitable for surface mounting.

Features

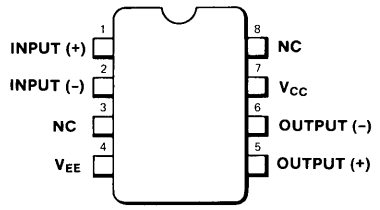
- **LOW INPUT NOISE VOLTAGE.**
- **WIDE POWER SUPPLY RANGE (8 TO 13V).**
- **INTERNAL DAMPING RESISTORS (1kohm).**
- **PDIP OR CERPAK (FLATPACK).**

Order Information

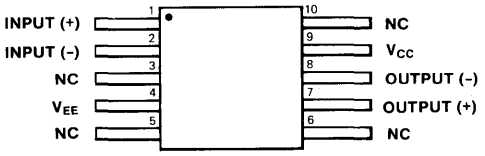
Type	Package	Code	Part No.
μA2480	Molded	9T	μA2480TC
μA2480	Flatpack	3F	μA2480FC

Connection Diagrams

8-LEAD MINIDIP (TOP VIEW)



10-LEAD FLATPAK (TOP VIEW)



Linear

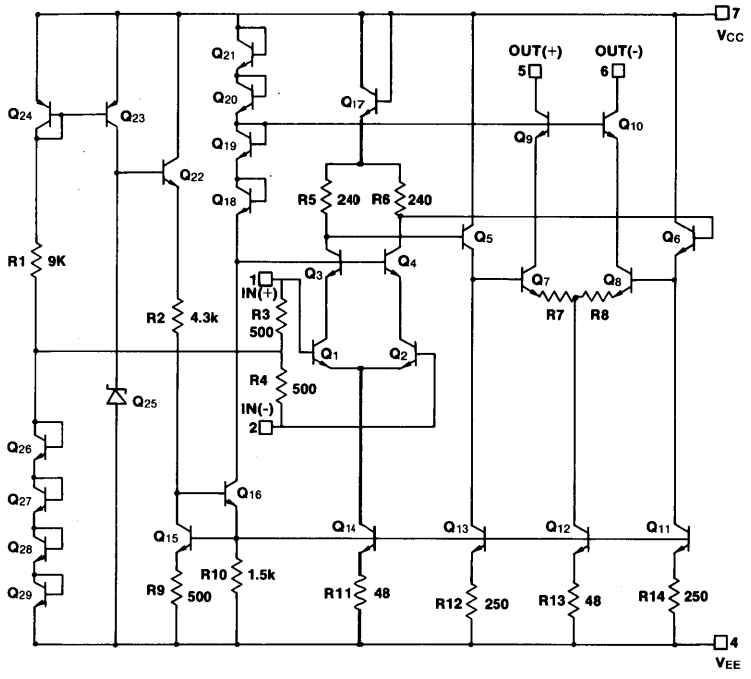
Absolute Maximum Ratings

Power Supply Voltage	15V
Output Voltage	15V
Differential Input Voltage	±1V
Storage Temperature Range	-65° C to 150° C
Operating Temperature Range	0° C to 70° C

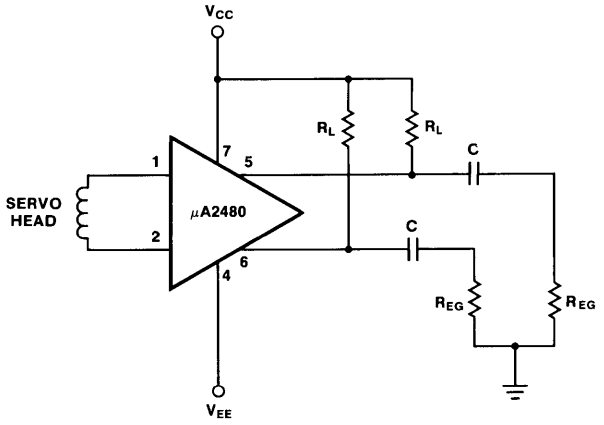
ELECTRICAL CHARACTERISTICS: T_A = 25° C, (Vcc-Vee) = 8 to 13.2V, unless otherwise noted

SYM	Parameter	Conditions	Min	Typ	Max	Units
G	Gain (differential)	Rp=130 ohm, (Vcc-Vee)=12V	92	115	138	
G	Gain (differential)	Rp = 130 Ohm, (Vcc-Vee) = 12V T_A = 0° C to 70° C	80		150	
BW	Bandwidth (3 dB)	Vi = 2mV (pp)	10	30		MHz
Rin	Input Resistance		800	1000	1200	Ohms
Cin	Input Capacitance			3		pF
Vin	Input Dynamic Range (Differential)	Rp=130 ohm (Vcc-Vee)=12V	3			mV(p-p)
Is	Power Supply Current	(Vcc-Vee) = 12V		30	40	mA
ΔVo	Output Offset (Differential)	Rs = 0, Rp = 130 ohm,			600	mV
Vn	Equivalent Input Noise	BW = 4 MHz		1.5	10	μV
PSRR	Power Supply Rejection Ratio	Rs = 0, f < 5 MHz	50	65		dB
ΔG/ΔV	Gain Sensitivity (Supply)	Δ (Vcc-Vee) = ±10%, Rp = 130 ohm		±1.3		%/V
ΔG/ΔT	Gain Sensitivity (Temp.)	Ta = 25° C to 70° C, Rp = 130 ohm		-0.2		%/° C
CMRR	Common Mode Rejection Ratio (Input)	f < 5 MHz	55	70		dB

Schematic Diagram

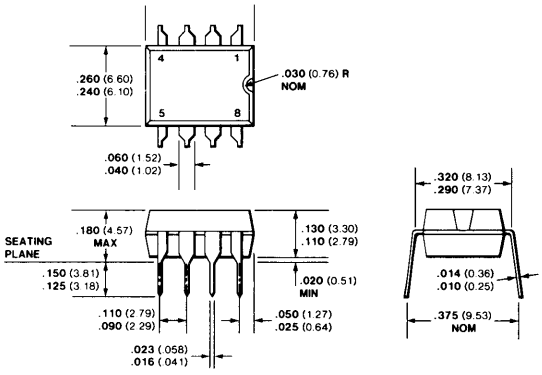


Typical Applications



1. Pins shown for 8-lead minidip.
2. Req is equivalent load resistance.
3. $Rp = \frac{R_L \cdot Req}{R_L + Req}$
4. G = .88 Rp
   Where Rp = value from 3 (above) in ohms

8-Pin Molded Dual In-Line Package Outline



9T

Notes

Pins are solder dipped copper alloy

Pins are intended for insertion in hole rows on .300 (7.62) centers

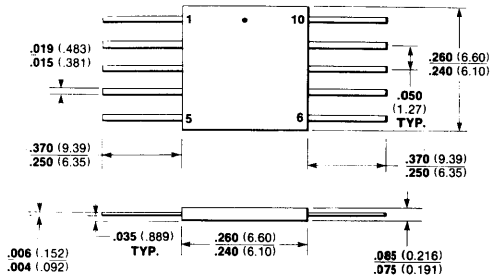
Units are purposely shipped with "positive" misalignment to facilitate insertion

Board drilling dimensions should equal your practice for .020 (0.51) diameter pin

Package material is plastic

Package weight is 0.6 gram

In Accordance with JEDEC (TO-91) OUTLINE 10-PIN CERPAK



3F

Notes

Pins are tin-plated alloy 42

Hermetically sealed alumina package

Package weight is 0.25 grams

Linear

Fairchild Linear Products
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313 Fairchild Drive
Mt. View, CA 94039-7282