FAIRCHILD SEMICONDUCTOR

MADE IN FAIRCHILD

THE LINEAR INTEGRATED CIRCUITS DATA CATALOG

LINEAR

LINEAR

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LINEAR

NOVEMBER 1971

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Introduction

This data catalog contains complete information on Fairchild's entire line of quality linear integrated circuits . . . the most comprehensive line in the industry. Some idea of just how comprehenisve our product line is can be gained quickly by referring to the chart below, which summarizes by market and by major end-equipments within each market, the types of Fairchild devices that serve their needs. There are currently 84 device types in production.

You'll find that the catalog is organized to permit quick, convenient reference to such information as specification data, connection diagrams, block diagrams and ordering information.

Also included are the following special sections devoted to:

- Selection guides to consumer products, interface elements, operational amplifiers and voltage comparators.
- A comprehensive industry-wide cross reference listing direct replacement and equivalent Fairchild products.
- Fairchild's UNIQUE 38510 high reliability program, showing process summary product screening levels and device types currently available.
- A statement on dice, summarizing electrical performance specifications, visual inspection criteria and availability.
- A planned new products listing, illustrating Fairchild's continued technological advancement in proprietary and second source devices.

PRODUCT/MARKET RELATIONSHIP

Product Classifications	COMPUTER		CONSUMER				MILITARY		INDUSTRIAL						
	Mainframe	Peripheral	Transportation	Home Entertainment	Musical Instruments	Appliance	Vehicles/Ordnance	Communications Equipment	Office Machines	Control & Processing	Test & Measuring	Communications	Medical & Scientific		
General Purpose Op Amps		▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲		
Precision Op Amps							▲		▲	▲	▲	▲	▲		
Multiple Op Amps		▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲		
Comparators			▲		▲			▲		▲	▲	▲	▲		
Drivers/Receivers	▲	▲					▲	▲		▲	▲	▲	▲		
TV Circuits				▲	▲			▲		▲			▲		
Voltage Regulators	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲	▲		
Sense Amps	▲	▲					▲	▲	▲	▲					
Low Level Amps								▲				▲			
RF/IF Amps				▲				▲				▲			
AC Power Control				▲		▲			▲	▲					
Ordnance							▲								

Product Index

Selection Guides

Consumer Products
Line Drivers/Receivers
Operational Amplifiers
Voltage Comparators

SELECTION GUIDE FOR CONSUMER TV CIRCUITS

CHROMA PROCESSING AND DEMODULATION

PARAMETER	μA780/781/746	μA3066/3067	μA782
ACC Figure of Merit	ΔV_{out} = −3 dB for ΔV_{in} = −20 dB	ΔV_{out} = 3 dB for ΔV_{in} = −20 dB	ΔV_{out} = 3 dB for ΔV_{in} = −20 dB
Chroma Input Resistance	2.4 kΩ	50 kΩ	1.8 kΩ
Demodulator Output Resistance	300 Ω	5 Ω	50 Ω
Max B-Y Output	10 volts	3.6 volts	7 volts
Chroma Input for Max Demodulator Output	200 mV	200 mV	20 mV
Number of External Components	77	62	42
Number of Alignment Adjustments	4	7	5

SOUND IF AND DETECTOR*

PARAMETER	μA754	TAA640**	CA3065**
Sensitivity (μV)	70	100	200
AMR (dB) at 30% AM	50	44	50
Audio Output (Volts) RMS	3.0	1.6	2.5
IF Voltage Gain (dB)	72	76	68
Detector—Recovered Audio Voltage at Detector Out (mV)	450	—	750

*Typical measurements made at 4.5 MHz for the μA754/CA3065 and 5.5 MHz for the TAA640 (formerly μA784)
**Includes DC Volume Control

SELECTION GUIDE FOR LINE DRIVERS/INTERFACE DRIVERS

Key Features		μA9614	μA9616 (1)	μA9621	μA9624 (2)	μA9644 (3, 4)	75450 (3,5)
Supply Voltages		+5.0	+12 −12	+5.0 +12	+5.0 0 to −30	+5.0	+5.0
V_{IH} (V)	51	1.7		2.0	1.9	2.1	
	59	1.8	2.0	2.0	1.9	2.1	
V_{IL} (V)	51	0.9		1.0	1.1	1.0	
	59	0.85	0.8	1.0	1.1	0.85	
V_{OH} (V)		+3.2	+6.0	+4.3	−0.5	30 Max	30 Max
V_{OL} (V)		+0.2	−6.0	+0.2	+0.2	0.8 1.25	0.4
I_O (on) (mA)						500	250
I_O (off) (μA)						100	100
I_{SC} (mA)		−90	+15 −15	300	−20		
P_D (mW)		175	250	120	40	120	30
t_{pd} (ns)		16	300	10	120	50	

NOTES FOR LINE DRIVERS/INTERFACE DRIVERS

1. The μA9616 is a triple EIA line driver. Each driver incorporates an internal response control circuit. The slew rate is a maximum of 30 V/μs and a minimum of 4 V/μs (3% of unit interval at 20 k band). The two values for I_{SC} are the typical V_{OH} and V_{OL} short circuit currents. The t_{pd} is measured from 1.5 V on the input to the output passing through the 0 V point. The delay is caused by the internally controlled slew rate of the output. The μA9616 meets the electrical interface requirements of EIA-RS-232-C and the CCITT recommendation V.24. By using an external capacitor from the output to ground for wave shaping, the μA9616 will also meet the low level digital interface for MIL STD 188C.
2. The μA9624 is designed to operate with a V_{DD} from 0 to −30 V.
3. The V_{OH} value is a maximum stand off voltage on the collector of the output device. I_O (on) is the maximum steady state current sinking capability of the output device. I_O (off) is the maximum leakage current into the output with the output device off.
4. V_{OL} is the typical V_{CE} (sat) of the output device at collector currents of 100 mA (V_{OL} = 0.8 V) and 500 mA (V_{OL} = 1.25 V).
5. V_{OL} is a typical V_{CE} (sat) of the output transistor at collector currents of 100 mA (V_{OL} = 0.25 V) and 300 mA (V_{OL} = 0.5 V).

SELECTION GUIDE FOR LINE RECEIVERS/INTERFACE RECEIVERS

Key Features		μA9615 (1)	μA9617 (1, 2)	μA9620 (1, 3)	μA9622 (1)	μA9625 (1, 4)
Supply Voltages		+5.0	+5.0	+5.0 +12	+5.0 −10	+5.0 −11 to −30
V_{OL} (V)	51	0.40		0.40	0.40	0.40
	59	0.45	0.40	0.45	0.45	0.50
V_{OH} (V)	51	2.4		3.0	3.0	2.6
	59	2.4	2.4	3.0	3.0	2.6
V_{TH} (V)		±0.5	+1.5	±0.5	±2.0	−3.0 −9.0
VCM (V)		±15	±25	±15	±10	
R_{IN} (kΩ)		7	4	2.4	5	22
P_{DISS} (mW)		175	100	110	140	60
t_{pd} (ns)		28	50	30	35	70
Diff. Inputs		X		X	X	
Output Enable		X			X	
Response Control		X	X	X		
Line Terminator		X	X		X	
Wired–OR Output		X	X	X	X	
Failsafe Control			X		X	

NOTES FOR LINE RECEIVERS/INTERFACE RECEIVERS

1. V_{OL} is the worst-case, guaranteed maximum output low voltage at 25°C. V_{OH} is the worst-case, guaranteed minimum output high voltage at 25°C. Upper listed voltages are for 51 grade (temperature range −55°C to +125°C) devices, while lower voltages are for 59 grade (0°C to 70°C) devices.

2. The μA9617 receiver has a V_{TH} of 1.0 when the hysteresis pin is left open. If the response control pin is shorted to the hysteresis pin, the μA9617 receiver will operate with a typical 1.3 volts of hysteresis (i.e. V_{IH} = 20 V, V_{IL} = 0.7 V). With or without hysteresis, the receiver in the μA9617 operates in a failsafe mode as described in section 2.5 of EIA RS-232-C. The inputs are protected to ±25 volts (reference to ground). The μA9617 also meets the CCITT recommendation V.24.

3. The μA9620 provides two sets of differential inputs to each receiver: a 5 to 1 attenuated input (normally used) and a direct input. The V_{TH} and V_{CM} shown refer to the attenuated inputs. Divide the values by a factor of five to find values for the direct inputs. The response control on the μA9620 may be achieved by using two capacitors for each receiver; one from each direct input to ground. The attenuator inputs are connected to the line.

4. The μA9625 is not a line receiver; it is a dual MOS to TTL logic level converter. The negative 3.0 V V_{TH} is the guaranteed worst case V_{IH} necessary to produce a V_{OH}. The supply voltage range of −11 to −30 V is the min and max V_{DD} voltages allowable.

SELECTION GUIDE FOR COMMERCIAL GRADE OPERATIONAL AMPLIFIERS*

Key Features	μA702[x] Wide Band General Purpose	μA709 General Purpose	μA715 High Slew Rate Wide Band	μA725 High Accuracy Low Drift Excellent Stability	μA739 Low Noise Dual	μA740 High Z_{in} $10^{12}\Omega$ High Slew Rate	μA741 Internally Compensated General Purpose	μA747 Dual
Input Offset Voltage Max. (mV)	5.0	7.5	7.5	2.5	6.0	100	6.0	6.0
Input Offset Current Max. (nA)	2000	500	250	35	1000		200	200
Input Bias Current Max. (nA)	7500	1500	1500	125	2000	2.0	500	500
Minimum Voltage Gain (V/mV)	3.4	15	10	250	6.5	25	20	20
Operating Supply Voltage Range Min. (V)	+6, −3	±9.0	±6.0	±3.0	±4.0	±5.0	±5.0	±5.0
Max. (V)	+14,−7	±18	±18	±22	±18	±22	±18	±18
Unity Gain Bandwidth (MHz)	30	5.0	65	2.0	10	3.0	1.0	1.0
Slew Rate A_{CL} = 1 (V/μs)	3.5	0.3	18		1.0	6.0	0.5	0.5
A_{CL} = −1 (V/μs)	3.5	0.3	100		2.5	6.0	0.5	0.5
A_{CL} = 10 (V/μs)	5.0	3.0	38		8.0	6.0	0.5	0.5
Input Voltage Range (V)	+1.5, −6.0	±10	±15	±22	±15	±15	±15	±15
Differential Input Voltage (V)	±5.0	±5.0	±15	±22	±5.0	±30	±30	±30
Temp. Coefficient of Input Offset Voltage† (μV/°C)	10	10	6.0	0.5	4.0	20	7.0	7.0
Internal Compensation						x	x	x
Offset Adjust		x	x	x	x	x	x	x
Input Protection			x	x	x	x	x	x
Output Protection				x	x	x	x	x

SELECTION GUIDE FOR COMMERCIAL GRADE OPERATIONAL AMPLIFIERS*(Continued)

Key Features	μA748 Extended Bandwidth General Purpose	μA749 Dual Low Cost	μA776 Programmable		μA777 Precision	LM201 Extended Bandwidth General Purpose	LM301A Precision
			I_{SET} = 1.5 μA	I_{SET} = 15 μA			
Input Offset Voltage Max. (mV)	6.0	6.0	6.0	6.0	7.5	7.5	7.5
Input Offset Current Max. (nA)	200	500	6.0	25	50	200	50
Input Bias Current Max. (nA)	500	1000	10	50	250	500	250
Minimum Voltage Gain (V/mV)	20	15	50	50	25	20	25
Operating Supply Voltage Range Min. (V)	±5.0	±4.0	±1.2	±1.2	±5.0	±5.0	±5.0
Max. (V)	±18	±18	±18	±18	±20	±20	±20
Unity Gain Bandwidth (MHz)	1.0	10	0.2	1.0	1.0	1.0	1.0
Slew Rate A_{CL} = 1 (V/μs)	0.5	1.5	0.1	0.7	0.5	0.5	0.5
A_{CL} = −1 (V/μs)	6.0	2.5	0.1	0.7	6.0	6.0	6.0
A_{CL} = 10 (V/μs)	2.0	8.0	0.1	0.7	2.0	2.0	2.0
Input Voltage Range (V)	±15	±15	±15	±15	±15	±15	±15
Differential Input Voltage (V)	±30	±5.0	±30	±30	±30	±30	±30
Temp. Coefficient of Input Offset Voltage† (μV/°C)	7.0	3.0	3.0	3.0	3.0	7.0	6.0
Internal Compensation			x	x			
Offset Adjust	x	x	x	x	x	x	x
Input Protection	x	x	x	x	x	x	x
Output Protection	x	x	x	x	x	x	x

*V_S = ±15 V, T_A = 25°C unless otherwise specified † Typical value, 0°C ≤ T_A ≤ 70°C x V_S = +12, −6 V

SELECTION GUIDE FOR MILITARY GRADE OPERATIONAL AMPLIFIERS*

Key Features	μA702× Wide Band General Purpose	μA709 (312) General Purpose	μA709A (311) General Purpose	μA715 High Slew Rate Wide Band	μA725 High Accuracy Low Drift Excellent Stability	μA740 High Z_{in} $10^{12}\ \Omega$ High Slew Rate	μA741 Internally Compensated General Purpose	μA747 Dual
Input Offset Voltage Max. (mV)	2.0	5.0	2.0	5.0	1.0	20	5.0	5.0
Input Offset Current Max. (nA)	500	200	50	250	20		200	200
Input Bias Current Max. (nA)	5000	500	200	750	100	0.2	500	500
Minimum Voltage Gain (V/mV)	3.6	25	25	15	1000	50	50	50
Operating Supply Voltage Range Min. (V)	+6, −3	±9.0	±9.0	±6.0	±3.0	±5.0	±5.0	±5.0
Max. (V)	+14, −7	±18	±18	±18	±22	±22	±22	±22
Unity Gain Bandwidth (MHz)	30	5.0	5.0	65	2.0	3.0	1.0	1.0
Slew Rate A_{CL} = 1 (V/μs)	3.5	0.3	0.3	18		6.0	0.5	0.5
A_{CL} = −1 (V/μs)	3.5	0.3	0.3	100		6.0	0.5	0.5
A_{CL} = 10 (V/μs)	5.0	3.0	3.0	38		6.0	0.5	0.5
Input Voltage Range (V)	+1.5, −6.0	±10	±10	±15	±22	±15	±15	±15
Differential Input Voltage (V)	±5.0	±5.0	±5.0	±15	±22	±30	±30	±30
Temp. Coefficient of Input Offset Voltage† (μV/°C)	10	10	1.8	6.0	0.5	20	7.0	7.0
Internal Compensation						x	x	x
Offset Adjust		x	x	x	x	x	x	x
Input Protection				x	x	x	x	x
Output Protection					x	x	x	x

SELECTION GUIDE FOR MILITARY GRADE OPERATIONAL AMPLIFIERS*(Continued)

Key Features	μA748 Extended Bandwidth General Purpose	μA749 Dual Low Cost	μA776 Programmable I_{SET} = 1.5 μA	μA776 Programmable I_{SET} = 15 μA	μA777 Precision	LM101 Extended Bandwidth General Purpose	LM101A Precision
Input Offset Voltage Max. (mV)	5.0	3.0	5.0	5.0	2.0	5.0	2.0
Input Offset Current Max. (nA)	200	400	3.0	15	10	200	10
Input Bias Current Max. (nA)	500	750	7.5	50	75	500	75
Minimum Voltage Gain (V/mV)	50	25	50	50	50	50	50
Operating Supply Voltage Range Min. (V)	±5.0	±4.0	±1.2	±1.2	±5.0	±5.0	±5.0
Max. (V)	±22	±18	±18	±18	±20	±20	±20
Unity Gain Bandwidth (MHz)	1.0	10	0.2	1.0	1.0	1.0	1.0
Slew Rate A_{CL} = 1 (V/μs)	0.5	1.5	0.1	0.7	0.5	0.5	0.5
A_{CL} = −1 (V/μs)	6.0	2.5	0.1	0.7	6.0	6.0	6.0
A_{CL} = 10 (V/μs)	2.0	8.0	0.1	0.7	2.0	2.0	2.0
Input Voltage Range (V)	±15	±15	±15	±15	±15	±15	±15
Differential Input Voltage (V)	±30	±5.0	±30	±30	±30	±30	±30
Temp. Coefficient of Input Offset Voltage† (μV/°C)	7.0	3.0	3.0	3.0	3.0	3.0	3.0
Internal Compensation			x	x			
Offset Adjust	x	x	x	x	x	x	x
Input Protection	x	x	x	x	x	x	x
Output Protection	x	x	x	x	x	x	x

*V_S = ±15 V, T_A = 25°C unless otherwise specified
† Typical value, −55°C ≤ T_A ≤ 125°C
× V_S = +12, −6 V

SELECTION GUIDE FOR COMMERCIAL GRADE VOLTAGE COMPARATORS (1)

PARAMETER	μA710	μA711	μA734	μA760
Input Offset Voltage, Max. (mV) (2)	5.0	5.0	7.5	6.0
Temperature Coefficient of Input Offset Voltage (μV/°C)	5.0	5.0	3.5	3.0
Input Bias Current, Max. (μA)	40	150	0.15	60
Input Offset Current, Max. (μA)	7.5	25	0.045	7.5
Supply Voltage (V)	+12, −6.0	+12, −6.0	±5.0 to ±15	±4.5 to ±6.5
Response Time (ns)	40	40	200	16
Input Voltage Range (V)	±5.0 (3)	±5.0 (3)	±5.0	±4.0
Output Voltage Swing (V)	−0.5 to −3.2	−0.5 to +3.2	0 to +8.0	0 to ±3.0
Voltage Gain, Min. (V/mV)	0.8	0.5	25	5.0 (4)
Power Consumption, Max. (mW)	150	230 (5)	145	325
TTL Fanout	1	1	2	2
Diff. Input Voltage Range (V)	±5.0	±5.0	±10	±5.0

(1) Typical values at 25°C unless otherwise specified.
(2) Minimum and maximum values are for $0°C \leq T_A \leq 70°C$.
(3) $V^- = -7.0$ V.
(4) Typical.
(5) $T_A = +25°C$.

SELECTION GUIDE FOR MILITARY GRADE VOLTAGE COMPARATORS (1)

PARAMETER	μA710	μA711	μA734	μA760
Input Offset Voltage, Max. (mV) (2)	3.0	4.5	4.0	6.0
Temperature Coefficient of Input Offset Voltage (μV/°C)	3.5	5.0	2.5	3.0
Input Bias Current, Max, (μA)	45	150	0.15	60
Input Offset Current, Max. (μA)	7.0	20	0.02	7.5
Supply Voltage (V)	+12, −6.0	+12, −6.0	±5.0 to ±15	±4.5 to ±6.5
Response Time (ns)	40	40	200	16
Input Voltage Range (V)	±5.0 (3)	±5.0 (3)	±10	±4.0
Output Voltage Swing (V)	−0.5 to +3.2	−0.5 to +3.2	0 to +8.0	0 to +3.0
Voltage Gain, Min. (V/mV)	1.0	0.5	25	5.0 (4)
Power Consumption, Max (mW)	150	200 (5)	145	312
TTL Fanout	1	1	2	2
Diff. Input Voltage Range (V)	±5.0	±5.0	±10	±5.0

(1) Typical values at 20°C unless otherwise specified.
(2) Maximum and minimum values are for $-55°C \leq T_A \leq +125°C$.
(3) $V^- = -7.0$ V.
(4) Typical.
(5) $T_A = +25°C$.

Competitive Cross-Reference

MOTOROLA	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
MC1303L		U6A7739393
MC1304P	U6A7732394	
MC1304PQ	U7F7732394	
MC1305P	U6A7729394	
MC1305PQ	U7F7729394	
MC1307P	U6A7767394	
MC1307PQ	U7F7767394	
MC1326PQ		U7F7746394
MC1326P		U6A7746394
MC1328G	U5E7746394	
MC1328P	U6A7746394	
MC1328PQ	U7F7746394	
MC1345P		TBA550
MC1350P		U6A7757394
MC1351P		U6A7754394
MC1352P		U6A7757394
MC1353P		U6A7757394
MC1353PQ		U7F7757394
MC1355P		U6A7754394
MC1355PQ		U7F7754394
MC1357P		U6A7754394
MC1357PQ		U7F7754394
MC1414L		U6A7711393
MC1414P		U6A7711393
MC1429G		U5B7730393
MC1430F		U3F7702312
MC1430G		U5B7702393
MC1430L		U6A7702393
MC1430P		U6A7702393
MC1431F		U3F7702312
MC1431G		U5B7702393
MC1431L		U6A7702393
MC1431P		U6A7702393
MC1433F		U3F7101311
MC1433G		U5B7101392
MC1433L		U6A7101392
MC1436G		U5B7101392
MC1437L		U6A7749393
MC1437P		U6A7749393
MC1438P		U6A7749393
MC1439G		U5B7101392
MC1439L		U6A7101392
MC1440F		SN7525
MC1440G		SN7525
MC1440L		SN7525
MC1440P		SN7525
MC1441F		SN7524
MC1441L		SN7524
MC1441P		SN7524

MOTOROLA	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
MC1445F		U3F7733312
MC1445G		U5F7733393
MC1445L		U6A7733393
MC1446L		U6A7733393
MC1456G		U5T7725393
MC1458G		U5F7747393
MC1458P		U6A7747393
MC1460G		U5R7723393
MC1460R		U5R7723312
MC1461G		U5R7723393
MC1461R		U5R7723393
MC1463R		U5R7723393
MC1466L		U6A7723393
MC1469R		U5R7723393
MC1488L		U6A9616393
MC1489L		U6A9617393
MC1489AL		U6A9617393
MC1495L	U6A7795393	
MC1496G	U5E7796393	
MC1510F		U3F7733312
MC1510G		U5F7733312
MC1514L		U6A7711312
MC1519G		U5F7733312
MC1520F		U3F7101311
MC1520G		U5B7101311
MC1525G		U5B7730312
MC1526G		U5B7730312
MC1529G		U5B7730312
MC1530F		U3F7702312
MC1530G		U5B7702312
MC1531F		U3F7702312
MC1531G		U5B7702312
MC1533F		U3F7101311
MC1533G		U5B7101311
MC1533L		U6A7101311
MC1535F		U6A7749312
MC1535G		U6A7749312
MC1536G		U5B7741312
MC1537L		U6A7749312
MC1539G		U5B7101311
MC1539L		U6A7101311
MC1540F		SN7525
MC1540G		SN7525
MC1540L		SN7525
MC1541F		SN7524
MC1541L		SN7524
MC1543L		SN7524
MC1545F		U3F7733312
MC1545G		U5F7733312

MOTOROLA	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
MC1545L		U6A7733312
MC1546L		U6A7733312
MC1550F		U6A7757312
MC1550G		U6A7757312
MC1552G		U5F7715312
MC1553G		U5F7715312
MC1556G		U5T7725312
MC1558G		U5F7747312
MC1558P		U6A7747312
MC1560G		U5R7723312
MC1560R		U5R7723312
MC1561G		U5R7723312
MC1561R		U5R7723312
MC1563R		U5R7723312
MC1566L		U6A7723312
MC1569R		U5R7723312
MC1580L		U6B961551X
MC1582L		U6B961451X
MC1583L		U6B961551X
MC1584L		U6B961551X
MC1590G		U6A7757394
MC1595L	U6A7795393	
MC1596G	U6A7796312	
MC1709CF	U3F7709312	
MC1709CG	U5B7709393	
MC1709CL	U6A7709393	
MC1709F	U3F7709312	
MC1709G	U5B7709312	
MC1709L	U6A7709312	
MC1710CF	U3F7710312	
MC1710CG	U5B7710393	
MC1710CL	U6A7710393	
MC1710F	U3F7710312	
MC1710G	U5B7710312	
MC1710L	U6A7710312	
MC1711CF	U3F7711312	
MC1711CG	U5F7711393	
MC1711CL	U6A7711393	
MC1711F	U3F7711312	
MC1711G	U5F7711312	
MC1711L	U6A7711312	
MC1712CF	U3F7702312	
MC1712CG	U5B7702393	
MC1712CL	U6A7702393	
MC1712F	U3F7702312	
MC1712L	U6A7702312	
MC1723CG	U5R7723393	
MC1723G	U5R7723312	
MC1723CL	U6A7723393	
MC1723L	U6A7723312	
MC1741CF	U3F7741312	
MC1741CG	U5B7741393	
MC1741CL	U6A7741393	
MC1741CP	U9T7741393	
MC1741F	U3F7741312	
MC1741G	U5B7741312	
MC1741G	U5B7702312	
MC1741L	U6A7741312	
MFC4060		U5R7723393
MFC6010		U5Z7703394
MFC8000		U6A7739393
MFC8001		U6A7739393
MFC8002		U6A7739393
MFC8040		UGH7791393

NATIONAL	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
LH101		U5B7741312
LH101D		U6A7741312
LH101F		U3F7741312
LH201		U5B7741393
LH740A		U5B7740312
LH740AC		U5B7740393
LM100		U5R7723312
LM101	LM101	
LM101A	LM101A	
LM101AD	LM101AD	
LM101D	LM101D	
LM101F	LM101F	
LM104		U5R7723312
LM105		U5R7723312
LM106		U5B7710312
LM106F		U3F7710312
LM107		U5B7741312
LM107D		U6A7741312
LM107F		U3F7741312
LM109K	LM109K	
LM110		U5B7741312
LM111		U5B7734312
LM112		U5B7776312
LM201	LM201	
LM201A	LM201A	
LM201AF	LM201AF	
LM201AD	LM201AD	
LM207		U5B7741312
LM207D		U6A7741312
LM207F		U3F7741312
LM209K	LM209K	
LM210		U5B7741312
LM211		U5B7734312
LM212		U5B7776312
LM300		U5R7723393
LM301A	LM301A	
LM301AD	LM301AD	
LM301AF	LM301AF	
LM304		U5R7723393
LM305		U5R7723393
LM306		U5B7710393
LM307		U5B7741393
LM307D		U6A7741393

NATIONAL	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
LM307F		U3F7741393
LM309K	LM309K	
LM310		U5B7741393
LM311		U5B7734393
LM312		U5B7776393
LM376		U6A7723393
LM701C	U5B7710393	
LM703L	U5B7703393	
LM709	U5B7709312	
LM709A	U5B7709311	
LM709C	U5B7709393	
LM709CN	U6A7709393	
LM710	U5B7710312	
LM710A	U5B7710312	
LM710CN	U6A7710393	
LM711	U5F7711312	

NATIONAL	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
LM711C	U5F7711393	
LM711CN	U6A7711393	
LM723	U6R7723312	
LM723C	U5R7723393	
LM741	U5B7741312	
LM741C	U5B7741393	
LM748	U5B7748312	
LM748C	U5B7748393	
LM1303	U6A7739393	
LM1304	U6A7732394	
LM1305	U6A7732394	
LM1458		U5F7747312
LM1558		U5F7747393
LM3065	CA3065	
LM7524	SN7524	
LM7525	SN7525	

RCA	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
CA3000		U5B7702312
CA3001		U5F7733312
CA3002		U5Z7703394
CA3004		U5Z7703394
CA3005		U5Z7703394
CA3006		U5Z7703394
CA3007		U5B7716393
CA3008		U3F7702312
CA3010		U5B7702312
CA3011		U5E7754394
CA3012		U5E7754394
CA3013		U5E7754394
CA3014		U5Z7754394
CA3015		U5B7702312
CA3016		U3F7702312
CA3018	CA3018	
CA3019	CA3019	
CA3021		U6A7757394
CA3022		U6A7757394
CA3023		U6A7757394
CA3026	CA3026	
CA3028		U5Z7703394
CA3028A		U5Z7703394
CA3029		U6A7702393
CA3030		U6A7702393
CA3031	U5B7702312	
CA3032	U5B7702393	
CA3033		U6A7709312

RCA	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
CA3035		U6A7739393
CA3036	CA3036	
CA3037		U6A7709312
CA3038		U6A7709312
CA3039	CA3039	
CA3040		U5F7733312
CA3041		CA3065
CA3042		CA3065
CA3043		CA3065
CA3044		
CA3045	CA3045	
CA3046	CA3046	
CA3047		U6A7709393
CA3048		U6A7749393
CA3052		U6A7739393
CA3053		U5Z7703394
CA3054	CA3054	
CA3055		U5R7723312
CA3056A		U5B7702312
CA3059		U6A7742393
CA3060		U6A7739393
CA3064	CA3064	
CA3065	CA3065	
CA3066	CA3066	
CA3067	CA3067	
CA3068	CA3068	
CA3075	CA3075	
CA3076	CA3076	

SIGNETICS	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
SE501K		U5B7733312
NE501K		U5B7733393
NE501A		U6A7733393
NE510A		U6A7754394
NE511A		CA3045
SE515K		U5B7730312
NE515K		U5B7730393
SE518K		U5F7711312
NE518K		U5F7711393
NE518A		U6A7711393
SE526K		U5B7710312
NE526K		U5B7710393
NE526A		U6A7710393
NE528B		U7B7525393
SE528E		U7B7525312
SE528R		U7B7525312
SE531T		U5F7715312
NE531T		U5F7715393
SE533T		U5B7776312
NE533T		U5B7776393
SE536T	U5B7740312	
NE536T	U5B7740393	
SE550L		U5R7723312
NE550L		U5R7723393
NE550A		U6A7723393
S5101T	U5B7101312	
S51A1T		U5B7101312
S51A8T		U5B7108312
N5201T	U5B7101333	
N5201A		U6A7101333
N53A1T		U5B7101392
N53A1V		U9T7101393
N53A8T		U5B7108392
N5595A		U6A7795393
S5595F	U6A7796393	
S5596K	U5E7796312	
N5596K	U5E7796393	
N5596A		U6A7796393
S5709T	U5B7709312	
N5709T	U5B7709393	
N5709A		U6A7709393
S5710T	U5B7710312	
N5710T	U5B7710393	
N5710A		U6A7710393
S5711K	U5F7711312	
S5711T		U5F7711312
N5711K	U5E7711393	
N5711A		U6A7711393
S5723L	U5R7723312	
N5723L	U5R7723393	
N5723A		U6A7723393
S5733K	U5F7733312	
N5733K	U5F7733393	
N5733A		U6A7733393
S5733F	U6A7733312	
S5740T	U5B7740312	
N5740T	U5B7740393	
S5741T	U5B7741312	
N5741T	U5B7741393	
N5741A		U6A7741393
N5741V	U9T7741393	
S5748T	U5B7748312	
N5748T	U5B7748393	
N5748A		U6A7748393
N5748V	U9T7748393	
N7524B	SN7524	
N7525B	SN7525	

SPRAGUE	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
ULN2111A		U6A7754394
ULN2111N		U7F7754394
ULN2113A		U6A7754394
ULN2113N		U7F7754394
ULN2114A	U6A7746394	
ULN2114K	U5E7746394	
ULN2114N	U7F7746394	
ULN2114W	U5E7746394	
ULN2120A	U6A7732394	
ULN2120N	U7F7732394	
ULN2121A		U6A7767394
ULN2121N		U7F7767394
ULN2122A	U6A7729394	
ULN2122N	U7F7729394	
ULN2124A	U6B7780394	
ULN2124N	U7F7780394	
ULN2126A		U6A7739393
ULN2126N		U7F7739393
ULN2127A	U6A7781394	
ULN2127N	U7F7781394	
ULN2128A	U6A7767394	
ULN2128N	U7F7767394	
ULN2129A	CA3075	
ULN2129N	CA3075	
ULN2131A		U6A7754394
ULN2131N		U7F7754394
ULN2165A	CA3065	
ULN2165N	CA3065	

TI	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
SN5512L		U5F7733312
SN7512L		U5F7733393
SN5514L		U5F7733312
SN7514L		U5F7733393
SN55107AJ	SN55107J	
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SN75107AN	SN75107N	
SN55108AJ	SN55108J	
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SN75150J		U6A9616393
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SN75100L		U7B961559X
SN75154J		U6A9617393
SN75154N		U6A9617393
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SN52702AS		U3F7702312
SN52702L		U5B7702312
SN52702S		U3F7702312
SN72702N		U6A7702393
SN52702N		U6A7702312
SN72702L		U5B7702312
SN72702S		U3F7702312
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SN52101AL	LM101AH	
SN52101AZ	LM101AF	
SN72301AJ	LM301AD	
SN72301AN	LM301AD	
SN72301AL	LM301AH	
SN72301AZ	LM301AF	
SN52107J		U6A7777312
SN52107L		U5B7777312
SN52107S		U3F7777312
SN72107J		U6A7777393
SN72307N		U6A7777393
SN72307P		U9T7777393
SN72307L		U5B7777393
SN72307Z		U3F7777312
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SN72810Z		U3F7710312
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SN72510Z		U3F7710312
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SN52711L	U5F7711312	
SN52711S	U3F7711312	
SN72711J	U6A7711393	
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SN52811L		U5F7711312
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SN72811L		U5F7711393
SN2720N		U6A7711393
SN52820J		U6A7734312
SN52820N		U6A7734312
SN72820J		U6A7734393
SN52733N	U6A7733312	
SN52733L	U5F7733393	
SN72733N	U6A7733393	
SN72733L	U5F7733393	
SN5510L		U5F7733312
SN5510F		U3F7733312
SN52741J	U6A7741312	
SN52741N	U6A7741312	
SN52741L	U5B7741312	
SN52741Z	U3F7741312	
SN72741N	U6A7741393	
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SN72741P	U9T7741393	
SN72741L	U5B7741393	
SN72741Z	U3F7741312	
SN52558L		U5F7747312
SN72558P		U7A7747393
SN72558L		U5F7747312
SN52747J	U7A7747312	
SN52747N	U7A7747314	
SN52747L	U5F7747312	
SN72747J	U7A7747393	
SN72747N	U7A7747393	

TI	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
SN72747L	U5F7747393	
SN52748J	U6A7748312	
SN52748N	U6A7748312	
SN52748L	U5B7748312	
SN52748Z	U3F7748312	
SN72748J	U6A7748393	
SN72748N	U6A7748393	
SN72748P	U9T7748393	
SN72748L	U5B7748393	
SN72748Z	U3F7748312	
SN52770L		U5B7740312
SN72770L		U5B7740393
SN52771L		U5B7740312
SN72771L		U5B7740393
SN7524J	SN7524J	
SN7524N	SN7524N	
SN7525J	SN7525J	
SN7525N	SN7525N	
SN75235J	SN75235J	
SN75235N	SN75235N	
SN75450AN	SN75450AN	

TI	FAIRCHILD DIRECT REPLACEMENT	FAIRCHILD FUNCTIONAL EQUIVALENT
SN75451AP	SN75451P	
SN72400N		U6A7723393
SN72400L		U5R7723393
SN56514J		U6A7796393
SN56514N		U6A7706393
SN56514L		U5F7796393
SN76110N	U6A7767394	
SN76104	U6A7732394	
SN76105	U6A7729394	
SN76131	U6A7739393	
SN76242	U6B7780394	
SN76243	U6A7781394	
SN76246	U6A7746394	
SN76630	U6B7786364	
SN76533	U6B7785394	
SN76564	CA3064	
SN76619		U5Z7703394
SN76640		U6A7754394
SN76660		CA3065
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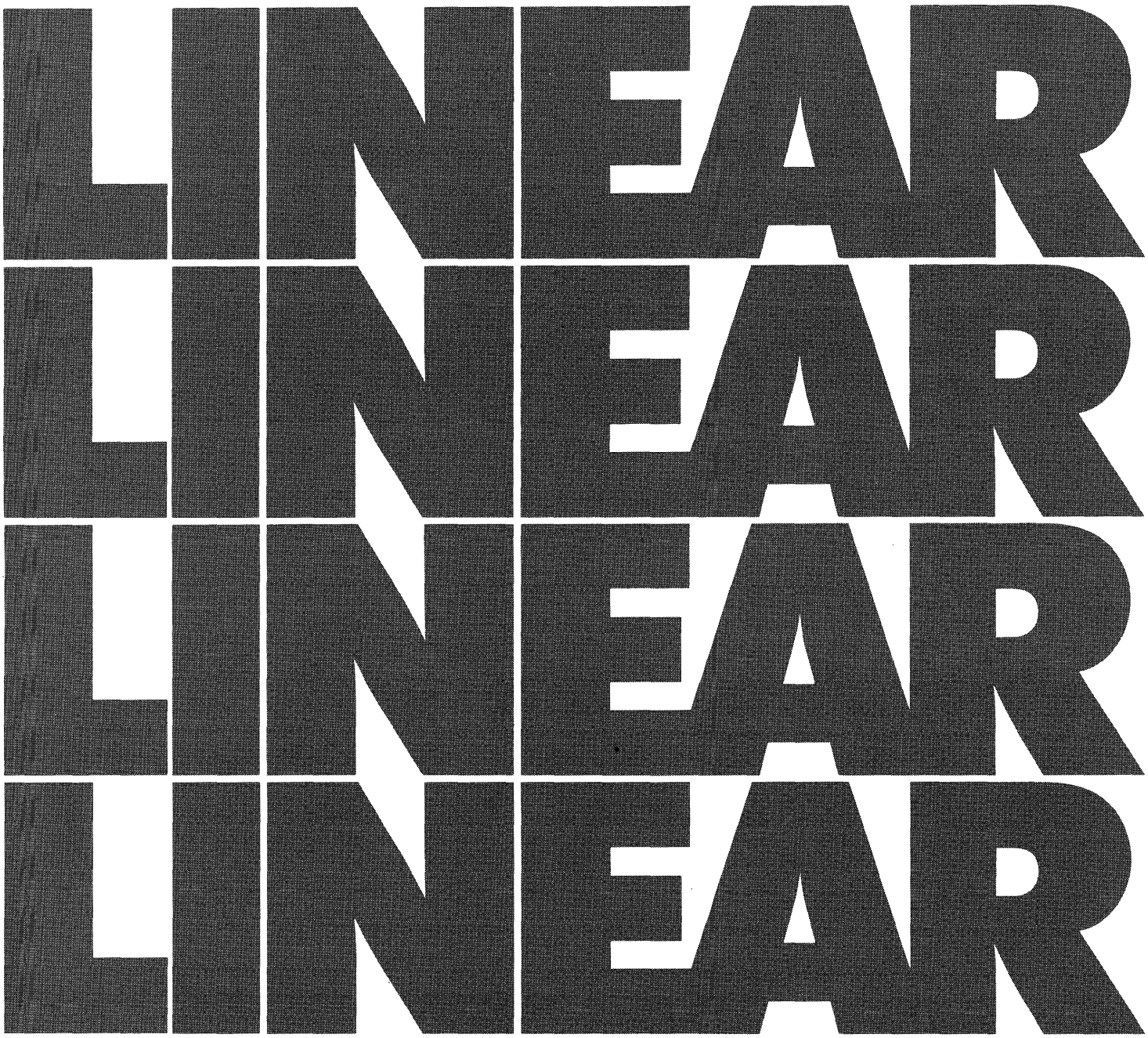
SN76110	U6A7767394	

For Complete Ordering Information See Page 304

Data Sheets



μA702

WIDEBAND DC AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA702 is a complete DC amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for use as an operational amplifier in miniaturized analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from DC to 30 MHz.

- **LOW OFFSET VOLTAGE**
- **LOW OFFSET VOLTAGE DRIFT**
- **WIDE BANDWIDTH – 20 MHz TYP.**
- **HIGH SLEW RATE – 5 V/μs TYP.**

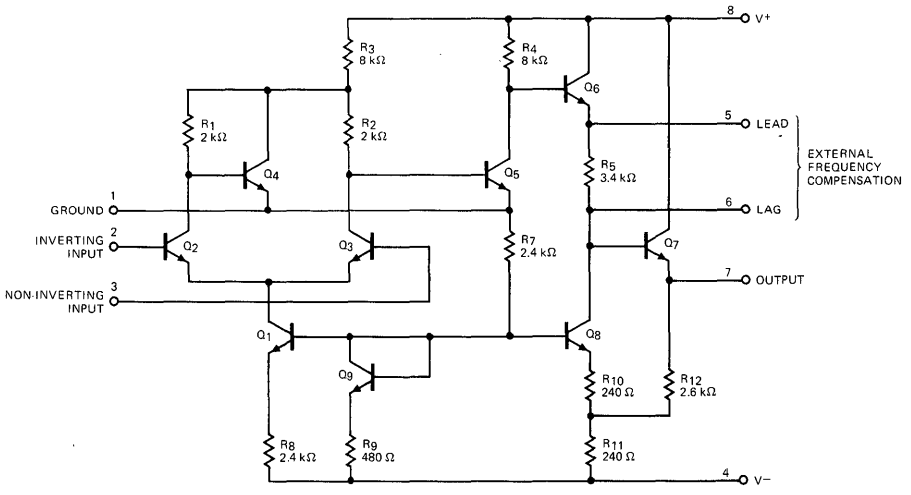
ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	21 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	+1.5 V to –6.0 V
Internal Power Dissipation (Note)	
Metal Can	500 mW
Ceramic DIP	670 mW
Flatpak	570 mW
Operating Temperature Range	
Military (312 Grade)	–55°C to +125°C
Commercial (393 Grade)	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

NOTE

Rating applies to ambient temperature up to 70° C. Above 70° C ambient derate linearly at 6.3 mW/°C for Metal Can, 8.3 mW/°C for Ceramic DIP and 7.1 mW/°C for the Flatpak package.

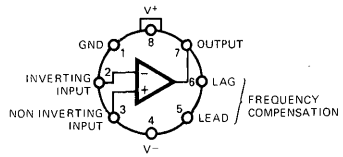
EQUIVALENT CIRCUIT



Pin numbers are shown for Metal Can only.

CONNECTION DIAGRAMS

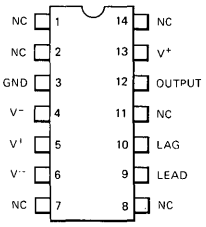
8 LEAD METAL CAN
(TOP VIEW)



NOTE: Pin 4 connected to case.

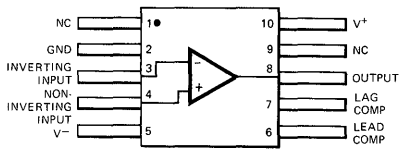
ORDER PART NOS:
U5B7702312
U5B7702393

14 LEAD DIP
(TOP VIEW)



ORDER PART NOS.
U6A7702312
U6A7702393

FLATPAK
(TOP VIEW)



ORDER PART NOS:
U3F7702312

*Planar is a patented Fairchild process.

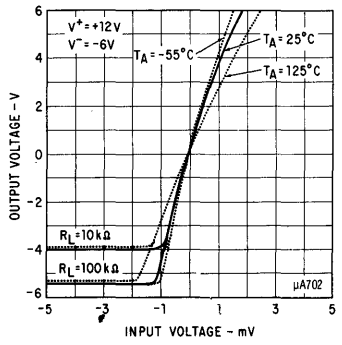
312 GRADE

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

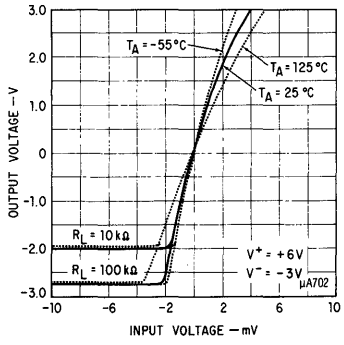
PARAMETER	CONDITIONS	V+ = 12.0 V, V− = −6.0 V MIN.	TYP.	MAX.	V+ = 6.0V, V− = −3.0 V MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 2\text{k}\Omega$		0.5	2.0		0.7	3.0	mV
Input Offset Current			180	500		120	500	nA
Input Bias Current			2.0	5.0		1.2	3.5	μA
Input Resistance		16	40		22	67		kΩ
Input Voltage Range		−4.0		+0.5	−1.5		+0.5	V
Common Mode Rejection Ratio	$R_S \leq 2\text{ k}\Omega$, f ≤ 1 kHz	80	100		80	100		dB
Large-Signal Voltage Gain	$R_L \geq 100\text{ k}\Omega$, $V_{OUT} = \pm 5.0$ V	2500	3600	6000				
	$R_L \geq 100\text{ k}\Omega$, $V_{OUT} = \pm 2.5$ V				600	900	1500	
Output Resistance			200	500		300	700	Ω
Supply Current	$V_{OUT} = 0$		5.0	6.7		2.1	3.3	mA
Power Consumption	$V_{OUT} = 0$		90	120		19	30	mW
Transient Response (unity-gain)	$C_I = 0.01\ \mu\text{F}$, $R_I = 20\ \Omega$, $R_L \geq 100\text{ k}\Omega$, $V_{IN} = 10$ mV							
Risetime			25	120				ns
Overshoot	$C_L \leq 100$ pF		10	50				%
Transient Response (x100 gain)	$C_3 = 50$ pF, $R_L \geq 100\text{ k}\Omega$, $V_{IN} = 1$ mV							
Risetime			10	30				ns
Overshoot			20	40				%
The following specifications apply for $-55°\text{C} \leq T_A \leq +125°\text{C}$:								
Input Offset Voltage	$R_S \leq 2\text{ k}\Omega$			3.0			4.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 25°\text{C}$ to $T_A = +125°\text{C}$		2.5	10		3.5	15	μV/°C
	$R_S = 50\ \Omega$, $T_A = 25°\text{C}$ to $T_A = -55°\text{C}$		2.0	10		3.0	15	μV/°C
Input Offset Current	$T_A = +125°\text{C}$		80	500		50	500	nA
	$T_A = -55°\text{C}$		400	1500		280	1500	nA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°\text{C}$ to $T_A = +125°\text{C}$		1.0	5.0		0.7	4.0	nA/°C
	$T_A = 25°\text{C}$ to $T_A = -55°\text{C}$		3.0	16		2.0	13	nA/°C
Input Bias Current	$T_A = -55°\text{C}$		4.3	10		2.6	7.5	μA
Input Resistance		6.0			8.0			kΩ
Common Mode Rejection Ratio	$R_S \leq 2\text{ k}\Omega$, f ≤ 1 kHz	70	95		70	95		dB
Supply Voltage Rejection Ratio	V+ = 12 V, V− = −6 V to V+ = 6 V, V− = −3 V, $R_S \leq 2\text{ k}\Omega$		75	200		75	200	μV/V
Large-Signal Voltage Gain	$R_L \geq 100\text{ k}\Omega$, $V_{OUT} = \pm 5.0$ V	2000		7000				
	$R_L \geq 100\text{ k}\Omega$, $V_{OUT} = \pm 2.5$ V				500		1750	
Output Voltage Swing	$R_L \geq 100\text{ k}\Omega$	±5.0	±5.3		±2.5	±2.7		V
	$R_L \geq 10\text{ k}\Omega$	±3.5	±4.0		±1.5	±2.0		V
Supply Current	$T_A = +125°\text{C}$, $V_{OUT} = 0$		4.4	6.7		1.7	3.3	mA
	$T_A = -55°\text{C}$, $V_{OUT} = 0$		5.0	7.5		2.1	3.9	mA
Power Consumption	$T_A = +125°\text{C}$, $V_{OUT} = 0$		80	120		15	30	mW
	$T_A = -55°\text{C}$, $V_{OUT} = 0$		90	135		19	35	mW

TYPICAL PERFORMANCE CURVES (312 GRADE)

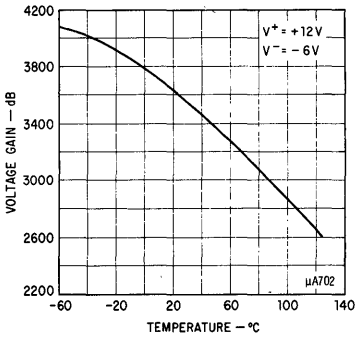
VOLTAGE TRANSFER CHARACTERISTIC



VOLTAGE TRANSFER CHARACTERISTIC



VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



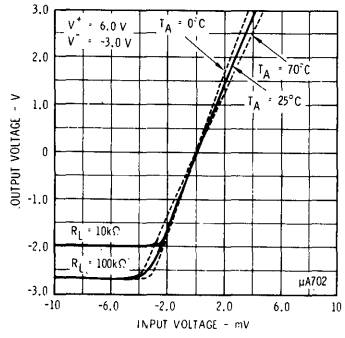
393 GRADE

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

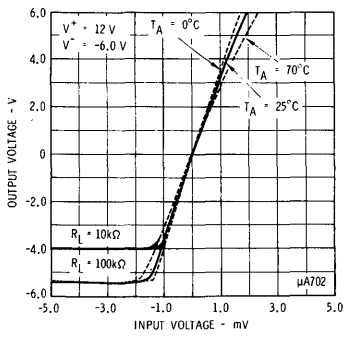
PARAMETER	CONDITIONS	V+ = 12.0 V, V− = −6.0 V MIN.	TYP.	MAX,	V+ = 6.0 V, V− = −3.0 V MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 2\ k\Omega$		1.5	5.0		1.7	6.0	mV
Input Offset Current			0.5	2.0		0.3	2.0	μA
Input Bias Current			2.5	7.5		1.5	5.0	μA
Input Resistance		10	32		16	55		kΩ
Input Voltage Range		−4.0		+0.5	−1.5		+0.5	V
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, f ≤ 1 kHz	70	92		70	92		dB
Large-Signal Voltage Gain	$R_L \geq 100\ k\Omega$, V_{OUT} = ±5.0 V	2000	3400	6000				
	$R_L \geq 100\ k\Omega$, V_{OUT} = ±2.5 V				500	800	1500	
Output Resistance			200	600		300	800	Ω
Supply Current	V_{OUT} = 0		5.0	6.7		2.1	3.3	mA
Power Consumption	V_{OUT} = 0		90	120		19	30	mW
Transient Response (unity gain)	C_I = 0.01 μF, R_I = 20 Ω, $R_L \leq 100\ k\Omega$, V_{IN} = 10 mV							
Risetime			25	120				ns
Overshoot	$C_L \leq 100$ pF		10	50				%
Transient Response (x100 gain)	C_3 = 50 pF, $R_L \geq 100\ k\Omega$, V_{IN} = 1 mV							
Risetime			10	30				ns
Overshoot			20	40				%
The following specifications apply for 0°C ≤ T_A ≤ +70°C:								
Input Offset Voltage	$R_S \leq 2\ k\Omega$			6.5			7.5	mV
Average Temperature Coefficient of Input Offset Voltage	R_S = 50 Ω, T_A = +70°C to T_A = 0°C		5.0	20		7.5	25	μV/°C
Input Offset Current				2.5			2.5	μA
Average Temperature Coefficient of Input Offset Current	T_A = 25°C to T_A = +70°C		4.0	10		3.0	8.0	nA/°C
	T_A = 25°C to T_A = 0°C		6.0	20		5.5	18	nA/°C
Input Bias Current	T_A = 0°C		4.0	12		2.7	8	μA
Input Resistance		6.0	18		9.0	27		kΩ
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, f ≤ 1 kHz	65	86		65	86		dB
Supply Voltage Rejection Ratio	V+ = 12 V, V− = 6 V to V+ = 6 V, V− = 3 V, $R_S \leq 2\ k\Omega$		90	300		90	300	μV/V
Large-Signal Voltage Gain	$R_L \geq 100\ k\Omega$, V_{OUT} = ±5.0 V	1500		7000				
	$R_L \geq 100\ k\Omega$, V_{OUT} = ±2.5 V				400		1750	
Output Voltage Swing	$R_L \geq 100\ k\Omega$	±5.0	±5.3		±2.5	±2.7		V
	$R_L \geq 10\ k\Omega$	±3.5	±4.0		±1.5	±2.0		V
Supply Current	V_{OUT} = 0		5.0	7.0		2.1	3.9	mA
Power Consumption	V_{OUT} = 0		90	125		19	35	mW

TYPICAL PERFORMANCE CURVES (393 GRADE)

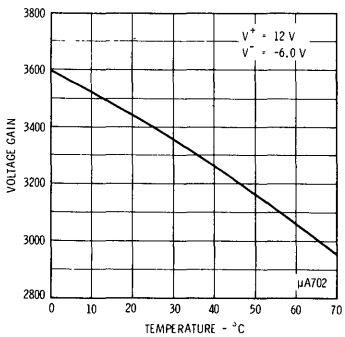
VOLTAGE TRANSFER CHARACTERISTIC



VOLTAGE TRANSFER CHARACTERISTIC

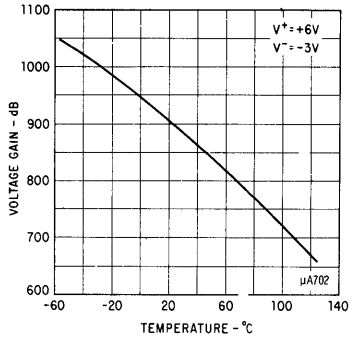


VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

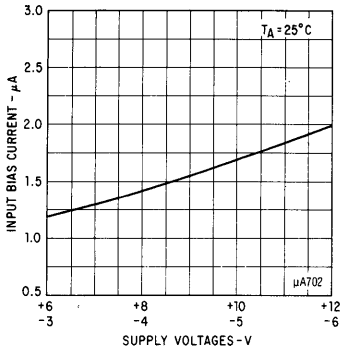


TYPICAL PERFORMANCE CURVES (312 GRADE)

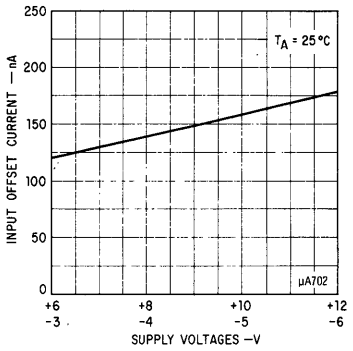
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



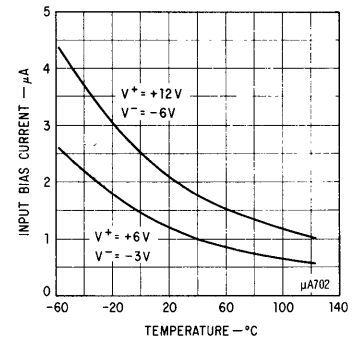
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



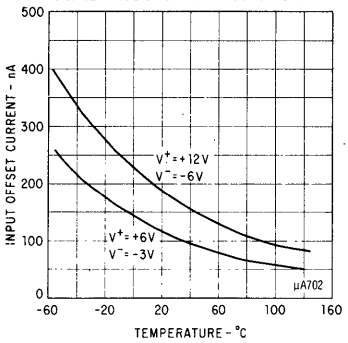
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



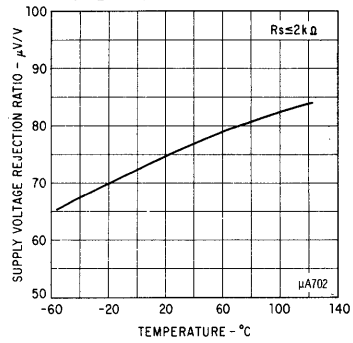
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



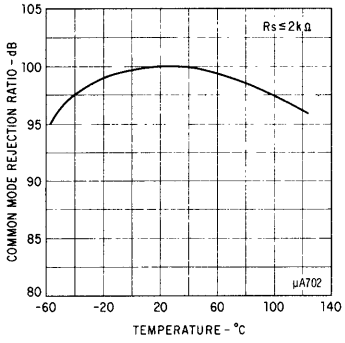
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



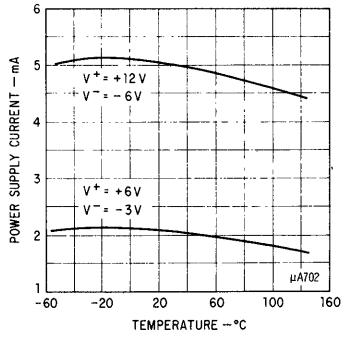
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



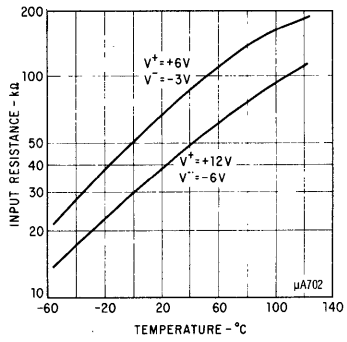
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



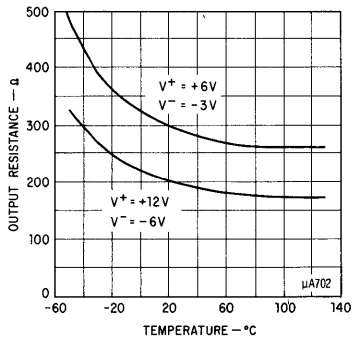
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

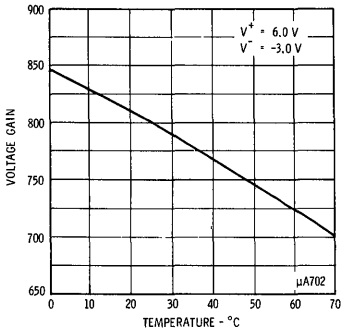


OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

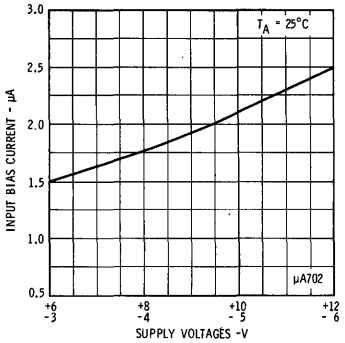


TYPICAL PERFORMANCE CURVES (393 GRADE)

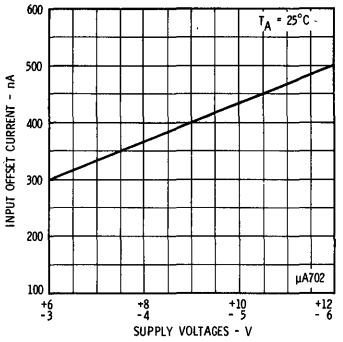
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



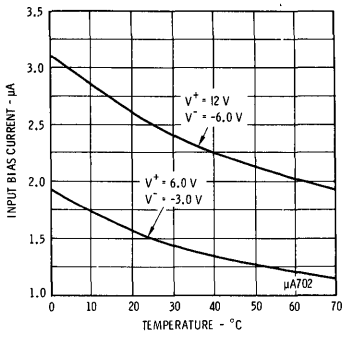
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



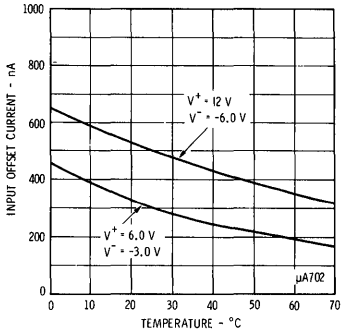
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



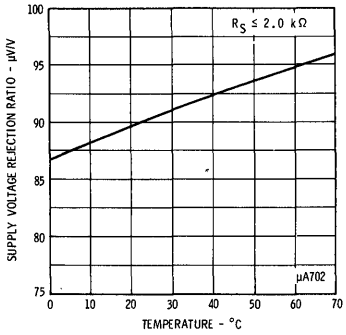
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



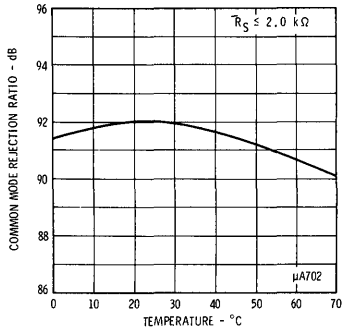
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



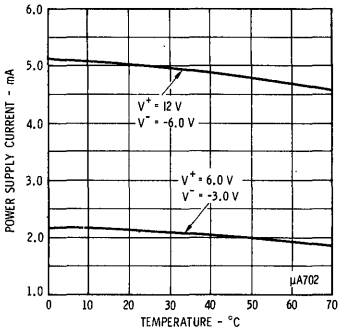
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



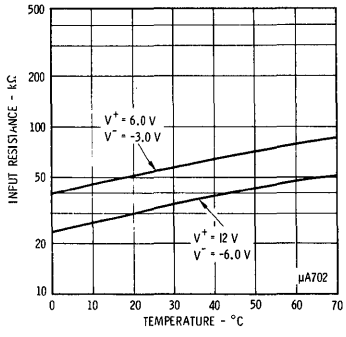
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



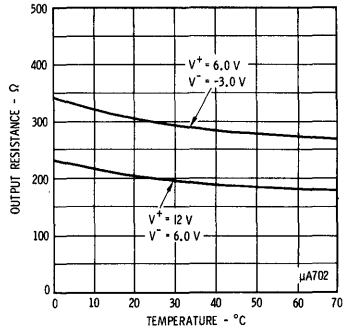
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

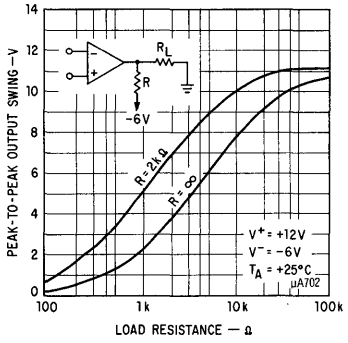


OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

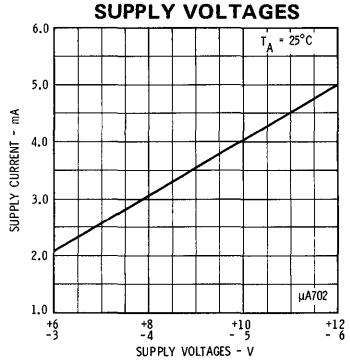


TYPICAL PERFORMANCE CURVES (312 AND 393 GRADES)

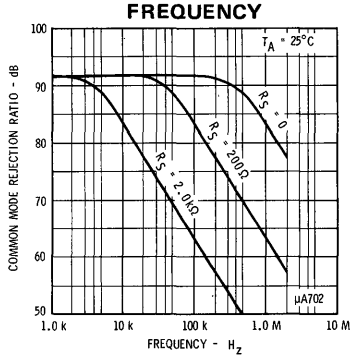
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



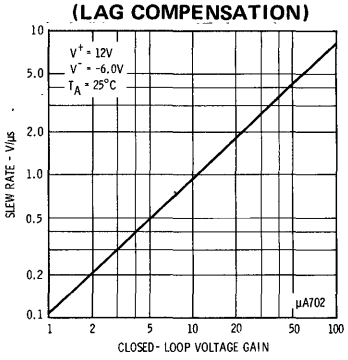
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



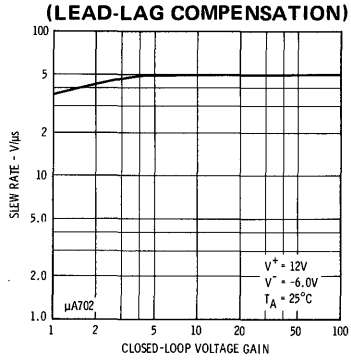
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



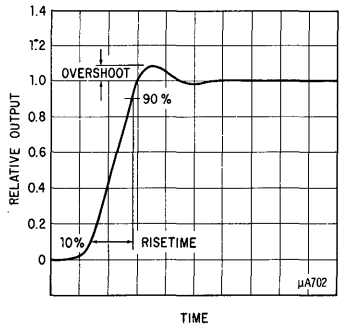
SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)



SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)

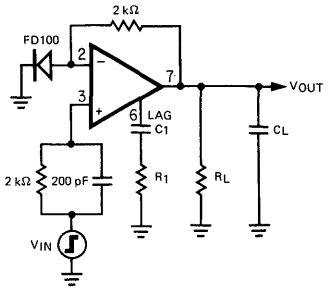


TRANSIENT RESPONSE

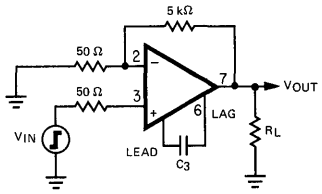


TRANSIENT RESPONSE TEST CIRCUITS

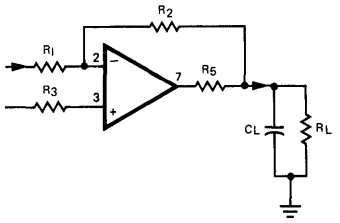
UNITY-GAIN AMPLIFIER (LAG COMPENSATION)



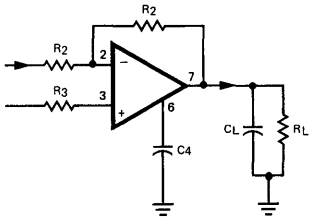
X100 AMPLIFIER (LEAD COMPENSATION)



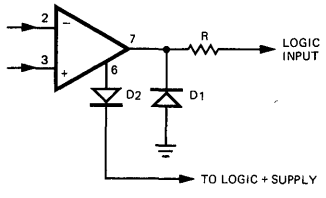
SERIES RESISTANCE LIMITING*



OUTPUT RISE-TIME LIMITING*



LOGIC COMPATIBILITY

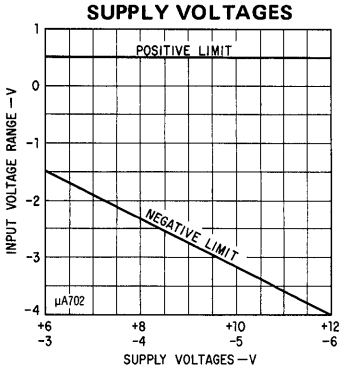


*Peak Current Limiting with Capacitive Loads.

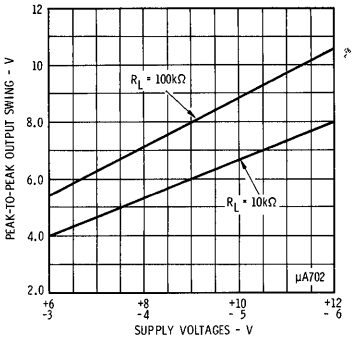
Pin numbers are shown for Metal Can only.

TYPICAL PERFORMANCE CURVES (312 AND 393 GRADES)

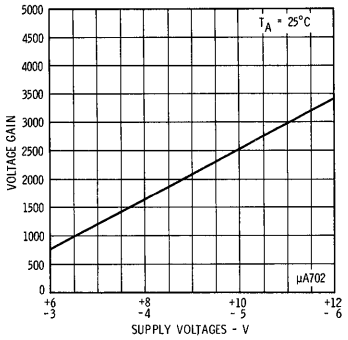
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES



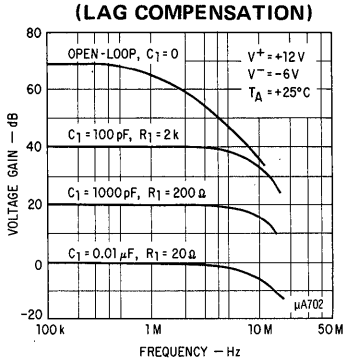
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES



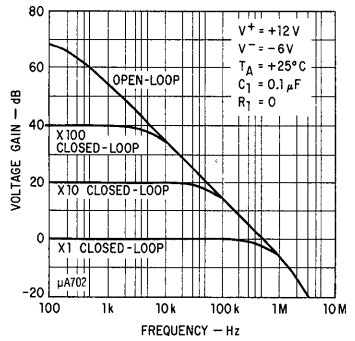
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



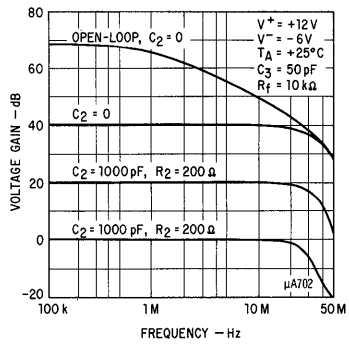
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



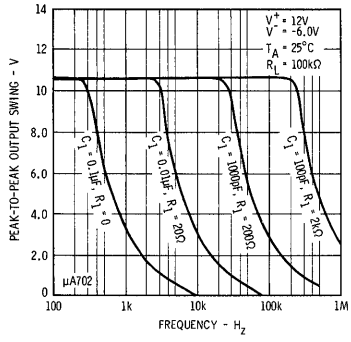
FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK



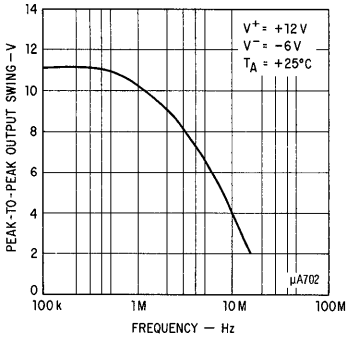
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS

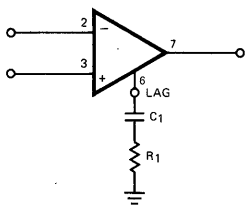


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY WITH LEAD-LAG COMPENSATION

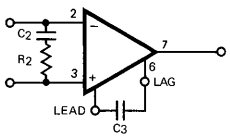


FREQUENCY COMPENSATION CIRCUITS

LAG COMPENSATION



LEAD-LAG COMPENSATION



Pin numbers are shown for Metal Can only.

μA703
RF-IF AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

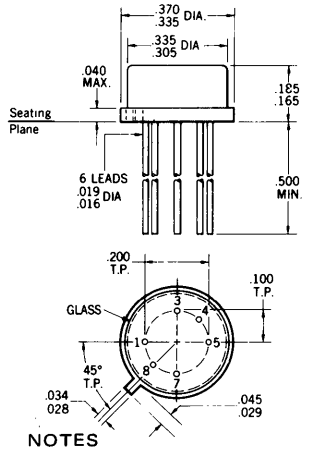
GENERAL DESCRIPTION — The μA703 is an RF-IF amplifier constructed on a single silicon chip and is intended for use as a limiting or non-limiting amplifier, harmonic mixer, or oscillator to 150 MHz. The low internal feedback of the device insures a higher stability-limited gain than that available from conventional circuitry. Including the biasing network in the same package reduces the number of external components required, thereby increasing the reliability and versatility of the device.

- **29 mmho MINIMUM FORWARD TRANSADMITTANCE**
- **1.0 mmho/0.05 mmho MAXIMUM INPUT/OUTPUT CONDUCTANCE**
- **12.5 pF/4.0 pF MAXIMUM INPUT/OUTPUT CAPACITANCE**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	20 V
Output Collector Voltage	24 V
Voltage Between Input Terminals	±5.0 V
Internal Power Dissipation	500 mW
Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

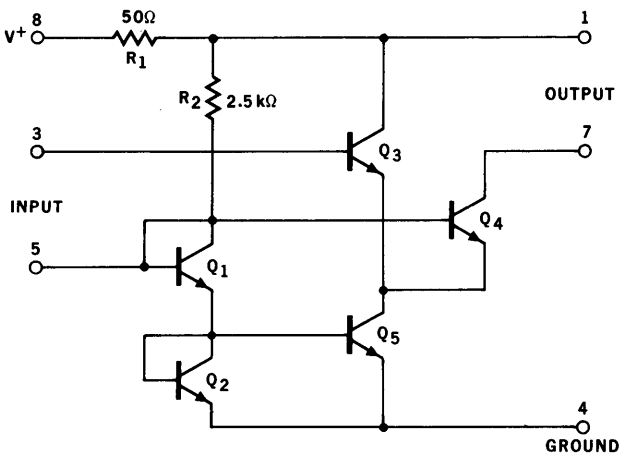
PHYSICAL DIMENSIONS
in accordance with JEDEC (TO-78) outline



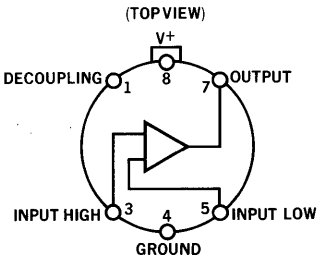
NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.95 gram

ORDER PART NO. U5Z7703394

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



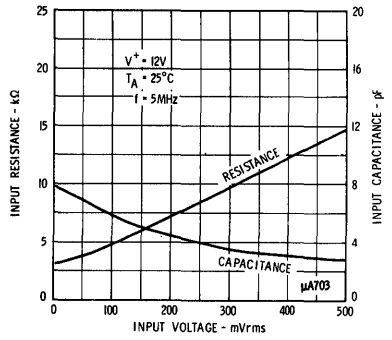
NOTE: Pin 4 connected to case.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12 V unless otherwise specified)

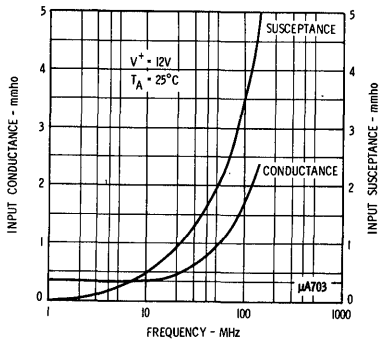
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Power Consumption	e_{in} = 0		110	170	mW
Quiescent Output Current	e_{in} = 0	1.5	2.5	3.3	mA
Peak-to-Peak Output Current	e_{in} = 400 mV_{rms}, f = 1 kHz	3.0			mA
Output Saturation Voltage				1.7	V
Forward Transadmittance	e_{in} = 10 mV_{rms}, f = 1 kHz	29	33		mmho
Input Conductance	e_{in} < 10 mV_{rms}, f = 10.7 MHz		0.35	1.0	mmho
Input Capacitance	e_{in} <10 mV_{rms}, f = 10.7 MHz		9.0	12.5	pF
Output Capacitance	e_o = 100 mV_{rms}, f = 10.7 MHz		2.0	4.0	pF
Output Conductance	e_o = 100 mV_{rms}, f = 10.7 MHz			0.05	mmho
Noise Figure	f = 30 MHz, R_S = 500 Ω		6.5		dB
	f = 100 MHz, R_S = 500 Ω		8.0		dB
The following specifications apply for 0°C ≤ T_A ≤ 70°C:					
Quiescent Output Current	e_{in} = 0	1.7		3.5	mA
Peak-to-Peak Output Current	e_{in} = 400 mV_{rms}, f = 1 kHz	3.2			mA
Output Saturation Voltage				1.8	V
Forward Transadmittance	e_{in} = 10 mV_{rms}, f = 1 kHz	22			mmho
Input Conductance	e_{in} <10 mV_{rms}, f = 1 kHz			0.71	mmho
Output Conductance	e_o = 100 mV_{rms}, f ≤5 MHz			0.06	mmho

TYPICAL PERFORMANCE CURVES

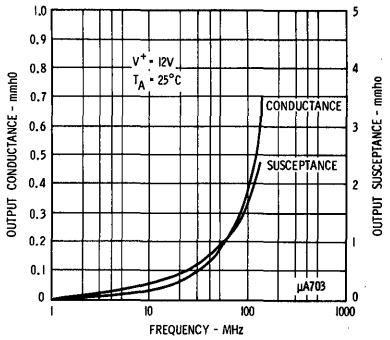
INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE



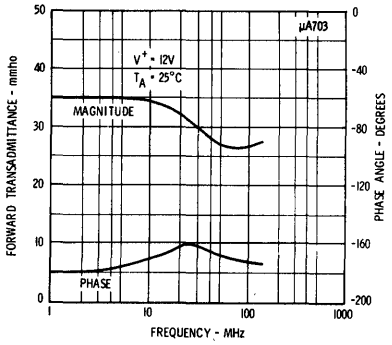
INPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



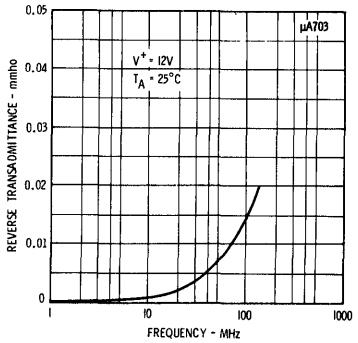
OUTPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



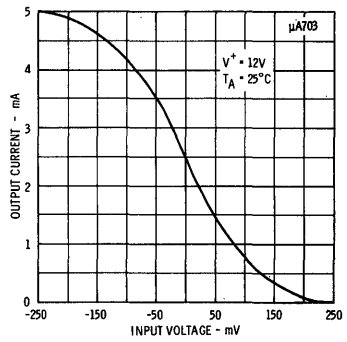
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



MAXIMUM REVERSE TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



μA709

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA709 is a high gain operational amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions.

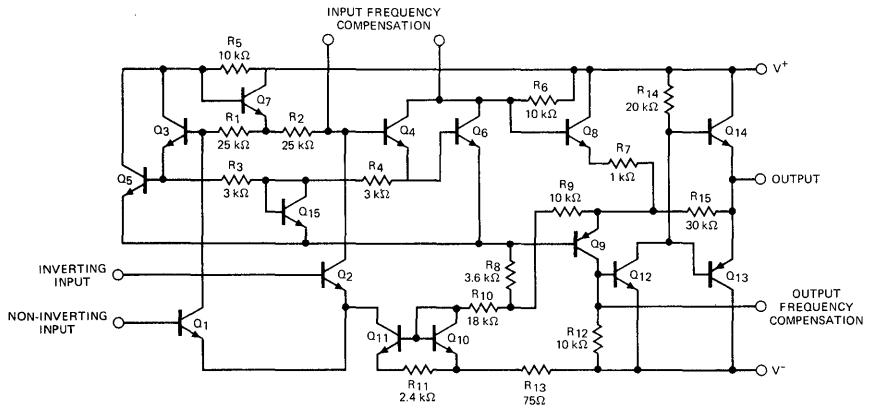
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note)	
Metal Can	500 mW
Ceramic DIP	670 mW
Flatpak	570 mW
Differential Input Voltage	±5.0 V
Input Voltage	±10 V
Storage Temperature Range	
Metal Can, Ceramic DIP, and Flatpak	−65°C to +150°C
Operating Temperature Range	
Military (311 and 312 Grades)	−55°C to +125°C
Commerical (393 Grade)	0°C to +70°C
Lead Temperature	
Metal Can, Ceramic DIP and Flatpak (Soldering 60 seconds)	300°C
Output Short Circuit Duration	5 seconds

NOTE

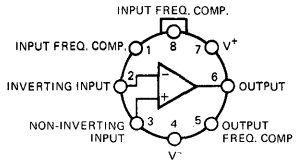
Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for Metal Can, 6.3 mW/°C for Silicone DIP, 8.3 mW/°C for Ceramic DIP and 7.1 mW/°C for the Flatpak package.

EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS
(TOP VIEWS)

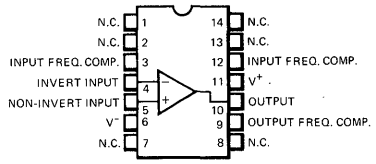
8 LEAD METAL CAN



NOTE: Pin 4 connected to case

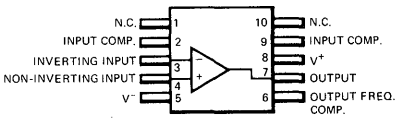
ORDER PART NOS.:
U5B7709311
U5B7709312
U5B7709393

14 LEAD DIP



ORDER PART NOS.:
U6A7709311
U6A7709312
U6A7709393

FLATPAK



ORDER PART NOS.:
U3F7709311
U3F7709312

*Planar is a patented Fairchild process.

(311 GRADE)

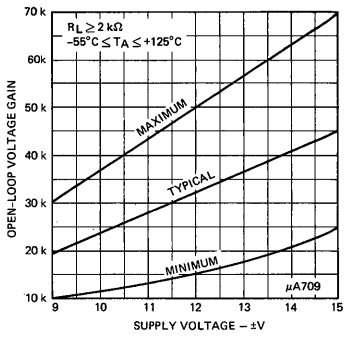
ELECTRICAL CHARACTERISTICS (T_A = +25°C, ±9 V ≤ V_S ≤ ±15 V unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		0.6	2.0	mV
Input Offset Current			10	50	nA
Input Bias Current			100	200	nA
Input Resistance		350	700		kΩ
Output Resistance			150		Ω
Supply Current	V_S = ±15 V		2.5	3.6	mA
Power Consumption	V_S = ±15 V		75	108	mW
Transient Response	V_S = ±15 V, V_{IN} = 20 mV, R_L = 2 kΩ, C_1 = 5 nF, R_1 = 1.5 kΩ, C_2 = 200 pF, R_2 = 50Ω				
Risetime				1.5	μs
Overshoot	$C_L \leq 100$ pF			30	%
The following specifications apply for –55°C ≤ T_A ≤ +125°C:					
Input Offset Voltage	$R_S \leq 10$ kΩ			3.0	mV
Average Temperature Coefficient of Input Offset Voltage	R_S = 50Ω, T_A = +25°C to +125°C		1.8	10	μV/°C
	R_S = 50Ω, T_A = +25°C to –55°C		1.8	10	μV/°C
	R_S = 10 kΩ, T_A = +25°C to +125°C		2.0	15	μV/°C
	R_S = 10 kΩ, T_A = +25°C to –55°C		4.8	25	μV/°C
Input Offset Current	T_A = +125°C		3.5	50	nA
	T_A = –55°C		40	250	nA
Average Temperature Coefficient of Input Offset Current	T_A = +25°C to T_A = +125°C		0.08	0.5	nA/°C
	T_A = +25°C to T_A = –55°C		0.45	2.8	nA/°C
Input Bias Current	T_A = –55°C		300	600	nA
Input Resistance	T_A = –55°C	85	170		kΩ
Input Voltage Range	V_S = ±15 V	±8.0			V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	80	110		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		40	100	μV/V
Large-Signal Voltage Gain	V_S = ±15 V, $R_L \geq 2$ kΩ, V_{OUT} = ±15 V	25,000		70,000	
Output Voltage Swing	V_S = ±15 V, $R_L \geq 10$ kΩ	±12	±14		V
	V_S = ±15 V, $R_L \geq 2$ kΩ	±10	±13		V
Supply Current	T_A = +125°C, V_S = ±15 V		2.1	3.0	mA
	T_A = –55°C, V_S = ±15 V		2.7	4.5	mA
Power Consumption	T_A = +125°C, V_S = ±15 V		63	90	mW
	T_A = –55°C, V_S = ±15 V		81	135	mW

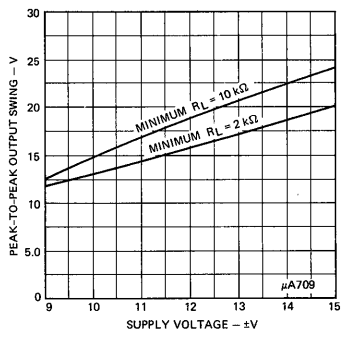
GUARANTEED ELECTRICAL CHARACTERISTICS

(311 GRADE)

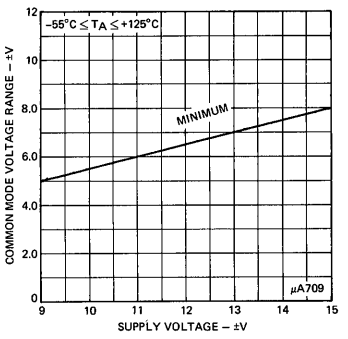
VOLTAGE GAIN



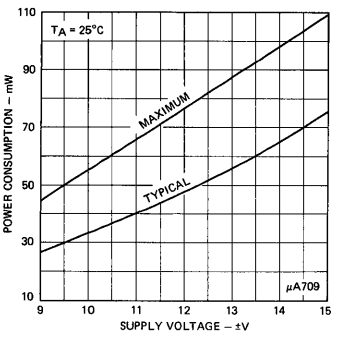
OUTPUT VOLTAGE SWING



INPUT COMMON MODE VOLTAGE RANGE



POWER CONSUMPTION



(312 GRADE)

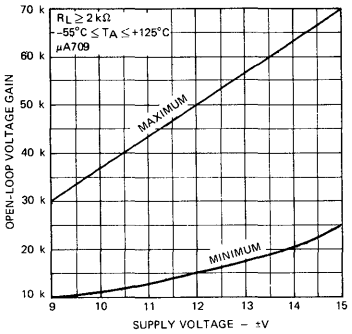
ELECTRICAL CHARACTERISTICS (T_A = +25°C, ±9 V ≤ V_S ≤ ±15 V unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current			50	200	nA
Input Bias Current			200	500	nA
Input Resistance		150	400		kΩ
Output Resistance			150		Ω
Power Consumption	V_S = ±15 V		80	165	mW
Transient Response	V_{IN} = 20 mV, R_L = 2 kΩ,				
Risetime	C_1 = 5000 pF, R_1 = 1.5 kΩ, C_2 = 200 pF, R_2 = 50Ω		0.3	1.0	μs
Overshoot	$C_L \leq 100$ pF		10	30	%
The following specifications apply for −55°C ≤ T_A ≤ +125°C:					
Input Offset Voltage	$R_S \leq 10$ kΩ			6.0	mV
Average Temperature Coefficient of Input Offset Voltage	R_S = 50Ω		3.0		μV/°C
	$R_S \leq 10$ kΩ		6.0		μV/°C
Large-Signal Voltage Gain	V_S = ±15 V, $R_L \geq 2$ kΩ, V_{OUT} = ±10 V	25,000	45,000	70,000	
Output Voltage Swing	V_S = ±15 V, $R_L \geq 10$ kΩ	±12	±14		V
	V_S = ±15 V, $R_L \geq 2$ kΩ	±10	±13		V
Input Voltage Range	V_S = ±15 V	±8.0	±10		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		25	150	μV/V
Input Offset Current	T_A = +125°C		20	200	nA
	T_A = −55°C		100	500	nA
Input Bias Current	T_A = −55°C		0.5	1.5	μA
Input Resistance		40	100		kΩ

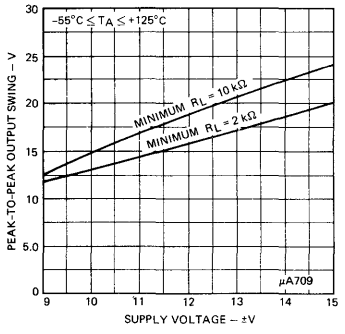
GUARANTEED ELECTRICAL CHARACTERISTCS

(312 GRADE)

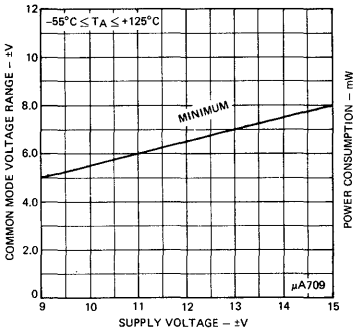
VOLTAGE GAIN



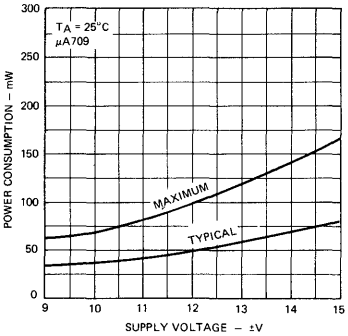
OUTPUT VOLTAGE SWING



INPUT COMMON MODE VOLTAGE RANGE



POWER CONSUMPTION



(393 GRADE)

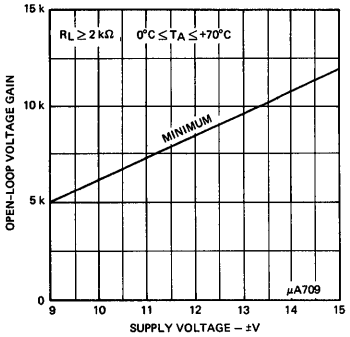
ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ, ±9 V ≤ V_S ≤ ±15 V		2.0	7.5	mV
Input Offset Current			100	500	nA
Input Bias Current			0.3	1.5	μA
Input Resistance		50	250		kΩ
Output Resistance			150		Ω
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	15,000	45,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Input Voltage Range		±8.0	±10		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	65	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		25	200	μV/V
Power Consumption			80	200	mW
Transient Response	V_{IN} = 20 mV, R_L = 2 kΩ,				
Risetime	C_1 = 5000 pF, R_1 = 1.5 kΩ, C_2 = 200 pF, R_2 = 50Ω		0.3		μs
Overshoot	$C_L \leq 100$ pF		10		%
The following specifications apply for 0°C ≤ T_A ≤ +70°C:					
Input Offset Voltage	$R_S \leq 10$ kΩ, ±9 V ≤ V_S ≤ ±15 V			10	mV
Input Offset Current				750	nA
Input Bias Current				2.0	μA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	12,000			
Input Resistance		35			kΩ

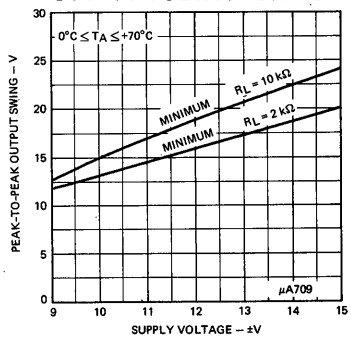
GUARANTEED ELECTRICAL CHARACTERISTICS

(393 GRADE)

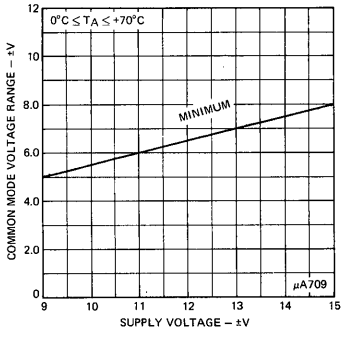
VOLTAGE GAIN



OUTPUT VOLTAGE SWING

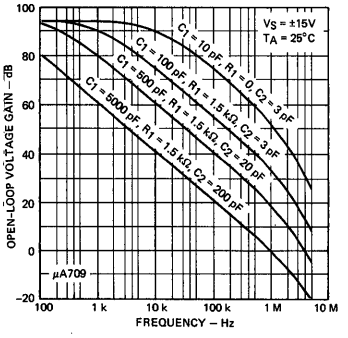


INPUT COMMON MODE VOLTAGE RANGE

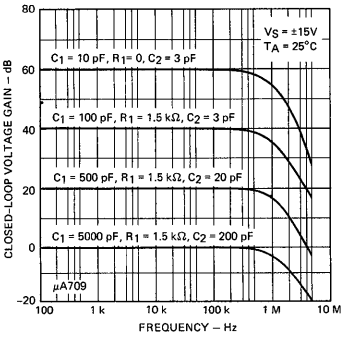


FREQUENCY COMPENSATION CURVES(FOR ALL GRADES)

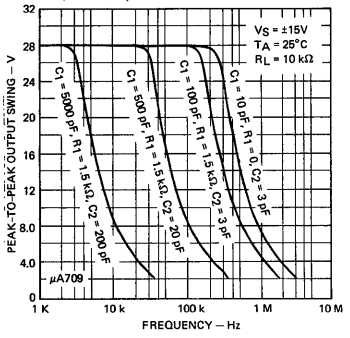
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS

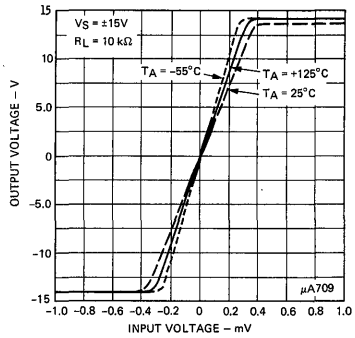


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS

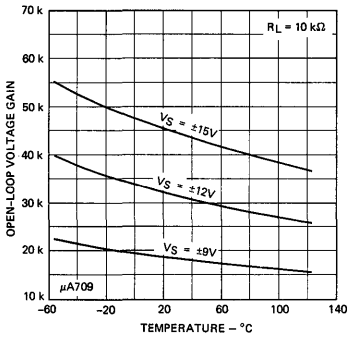


TYPICAL PERFORMANCE CURVES (FOR 311 GRADE)

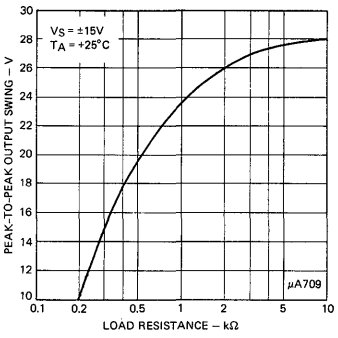
VOLTAGE TRANSFER CHARACTERISTIC



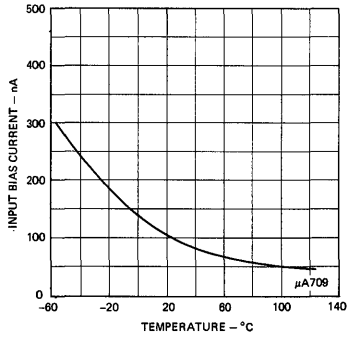
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



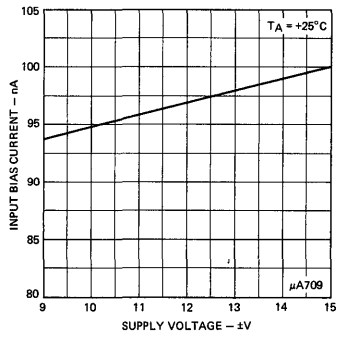
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



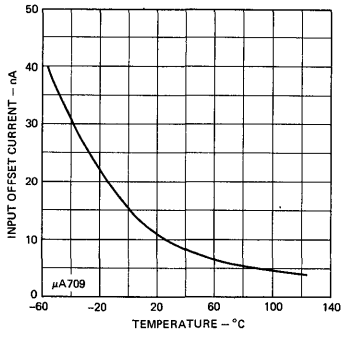
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



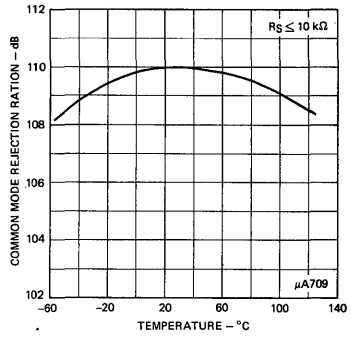
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



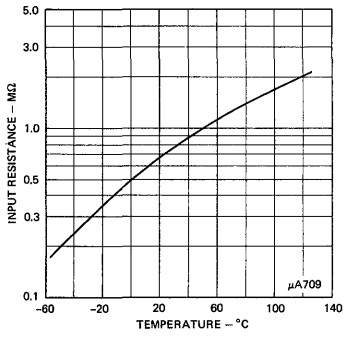
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



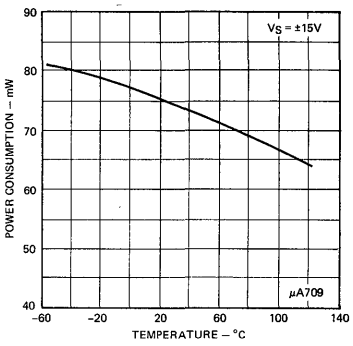
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



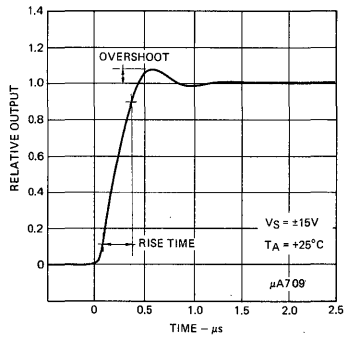
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



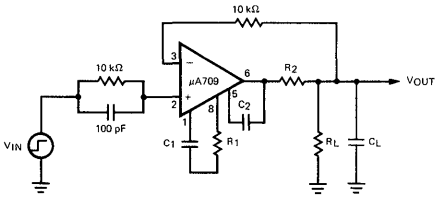
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



TRANSIENT RESPONSE

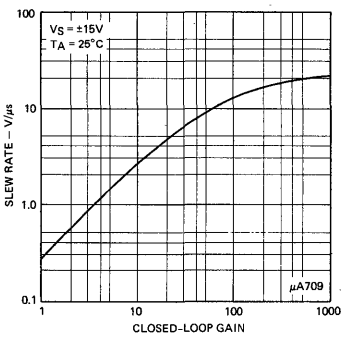


TRANSIENT RESPONSE TEST CIRCUIT



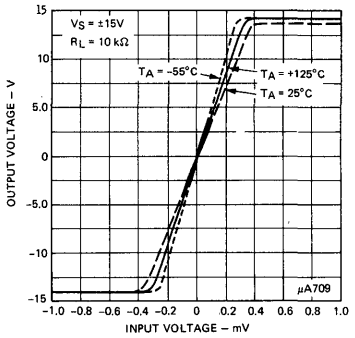
Pin numbers only apply to metal can package.

SLEW RATE AS A FUNCTION OF CLOSED-LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS

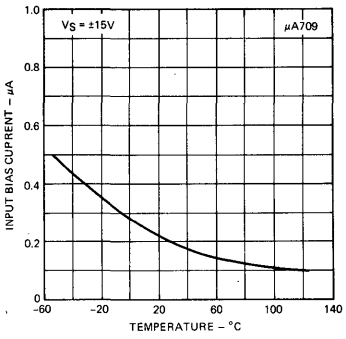


TYPICAL PERFORMANCE CURVES
(FOR 312 AND 393 GRADES)

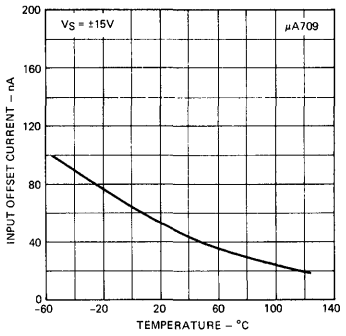
VOLTAGE TRANSFER CHARACTERISTIC



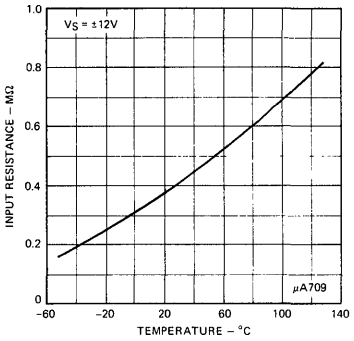
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



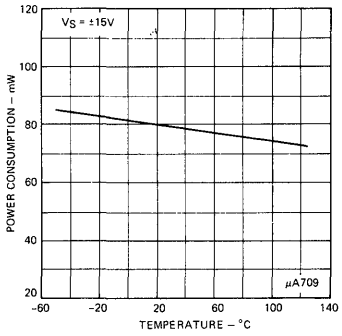
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



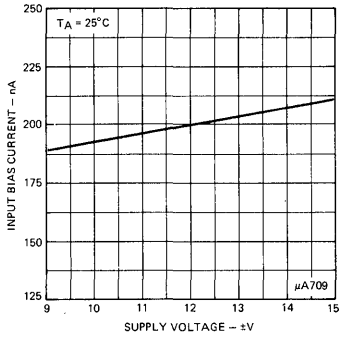
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



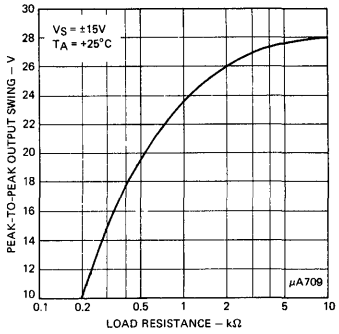
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



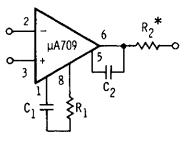
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

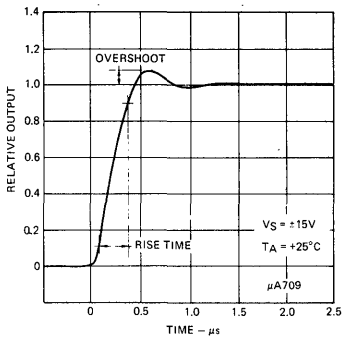


FREQUENCY COMPENSATION CIRCUIT



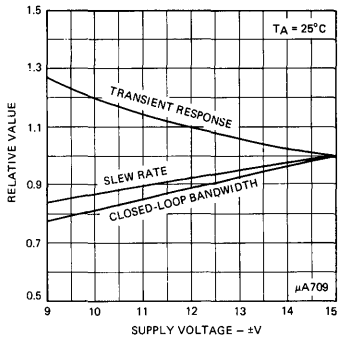
* Use R_2 = 50 Ω when the amplifier is operated with capacitive loading.

TRANSIENT RESPONSE

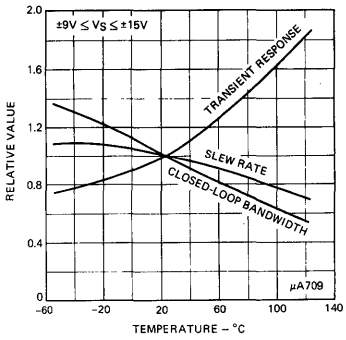


TYPICAL PERFORMANCE CURVES
(FOR 312 AND 393 GRADES)

FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



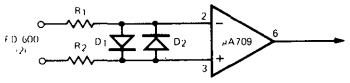
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



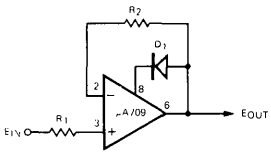
PROTECTION CIRCUITS

OUTPUT SHORT-CIRCUIT PROTECTION

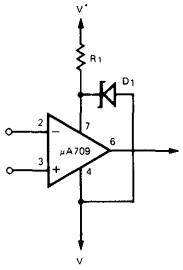
INPUT BREAKDOWN PROTECTION



LATCH-UP PROTECTION



SUPPLY OVERVOLTAGE PROTECTION



Pin numbers only apply to metal can package.

μA710
HIGH-SPEED DIFFERENTIAL COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

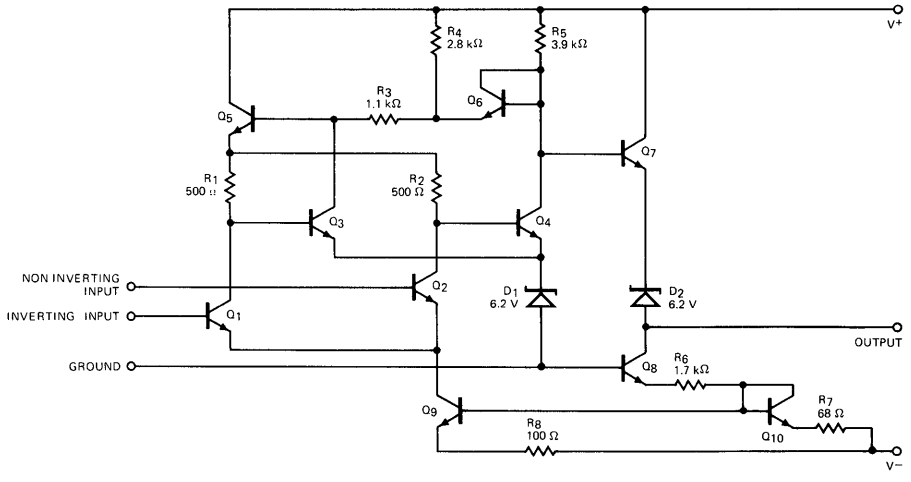
GENERAL DESCRIPTION – The μA710 is a differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A/D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

- **5 mV MAXIMUM OFFSET VOLTAGE**
- **5 μA MAXIMUM OFFSET CURRENT**
- **1000 MINIMUM VOLTAGE GAIN**
- **20 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+14.0 V
Negative Supply Voltage	−7.0 V
Peak Output Current	10 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Ceramic DIP	670 mW
Flatpak	570 mW
Storage Temperature Range	
Metal Can, Ceramic DIP, and Flatpak	−65°C to +150°C
Operating Temperature Range	
Military (312 Grade)	−55°C to +125°C
Commercial (393 Grade)	0°C to + 70°C
Lead Temperature	
Metal Can, Ceramic DIP and Flatpak (Soldering, 60 seconds)	300°C

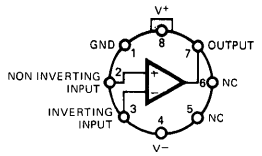
EQUIVALENT CIRCUIT



Notes on following pages.

CONNECTION DIAGRAMS

8 LEAD METAL CAN
(TOP VIEW)

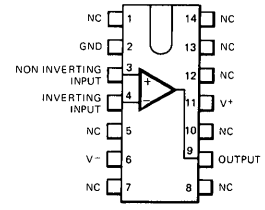


NOTE: Pin 4 connected to case.

ORDER PART NOS:

U5B7710312
U5B7710393

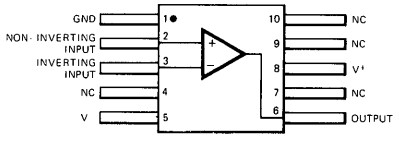
14 LEAD DIP
(TOP VIEW)



ORDER PART NOS:
FOR CERAMIC DIP

U6A7710312
U6A7710393

FLATPAK
(TOP VIEW)



ORDER PART NO: U3F7710312

*Planar is a patented Fairchild process.

312 GRADE

ELECTRICAL CHARACTERISTICS (T_A = +25°C, V+ = 12.0 V, V− = −6.0 V unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS (Note 3)	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		0.6	2.0	mV
Input Offset Current			0.75	3.0	μA
Input Bias Current			13	20	μA
Voltage Gain		1250	1700		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	2.0	2.5		mA
Response Time (Note 3)			40		ns
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 200\ \Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 25°C$ to $T_A = +125°C$		3.5	10	μV/°C
	$R_S = 50\ \Omega$, $T_A = 25°C$ to $T_A = -55°C$		2.7	10	μV/°C
Input Offset Current	$T_A = +125°C$		0.25	3.0	μA
	$T_A = -55°C$		1.8	7.0	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +125°C$		5.0	25	nA/°C
	$T_A = 25°C$ to $T_A = -55°C$		15	75	nA/°C
Input Bias Current	$T_A = -55°C$		27	45	μA
Input Voltage Range	V− = −7.0 V	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\ \Omega$	80	100		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		1000			
Positive Output Level	$\Delta V_{IN} \geq 5$ mV, $0 \leq I_{OUT} \leq 5.0$ mA	2.5	3.2	4.0	V
Negative Output Level	$\Delta V_{IN} \geq 5$ mV	−1.0	−0.5	0	V
Output Sink Current	$T_A = +125°C$, $\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	0.5	1.7		mA
	$T_A = -55°C$, $\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	1.0	2.3		mA
Positive Supply Current	$V_{OUT} \leq 0$		5.2	9.0	mA
Negative Supply Current			4.6	7.0	mA
Power Consumption			90	150	mW

393 GRADE

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V+ = 12.0 V, V− = −6.0 V unless otherwise specified)

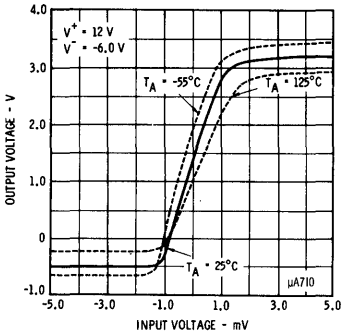
PARAMETERS (see definitions)	CONDITIONS (Note 3)	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.6	5.0	mV
Input Offset Current			1.8	5.0	μA
Input Bias Current			16	25	μA
Voltage Gain		1000	1500		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	1.6	2.5		mA
Response Time (Note 2)			40		ns
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 200\ \Omega$			6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 0°C$ to $T_A = +70°C$		5.0	20	μV/°C
Input Offset Current				7.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +70°C$		15	50	nA/°C
	$T_A = 25°C$ to $T_A = 0°C$		24	100	nA/°C
Input Bias Current	$T_A = 0°C$		25	40	μA
Input Voltage Range	V− = −7.0 V	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\ \Omega$	70	98		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		800			
Positive Output Level	$\Delta V_{IN} \geq 5$ mV, $0 \leq I_{OUT} \leq 5.0$ mA	2.5	3.2	4.0	V
Negative Output Level	$\Delta V_{IN} \geq 5$ mV	−1.0	−0.5	0	V
Output Sink Current	$\Delta V_{IN} \geq 5$ mV, $V_{OUT} = 0$	0.5			mA
Positive Supply Current	$V_{OUT} \leq 0$		5.2	9.0	mA
Negative Supply Current			4.6	7.0	mA
Power Consumption			90	150	mW

NOTES

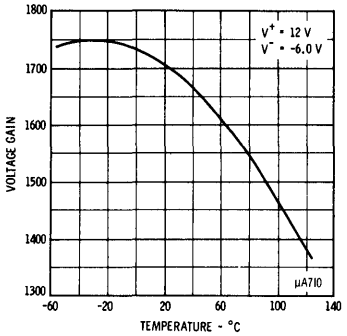
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for Metal Can, 8.3 mW/°C for Ceramic DIP, 6.3 mW/°C for Silicone DIP and 7.1 mW/°C for the Flatpak package.
2. Derate linearly at 4.4 mW/°C for case temperatures above +115°C; Derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.
3. The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.
4. The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage as follows: For 312 grade, 1.8 V at −55°C, 1.4 V at +25°C and 1.0 V at +125°C. For 393 grade, 1.5 V at +25°C and 1.2 V at +70°C.

312 GRADE
TYPICAL PERFORMANCE CURVES

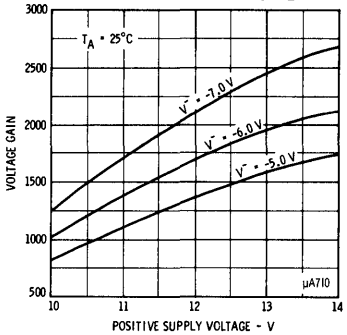
VOLTAGE TRANSFER CHARACTERISTIC



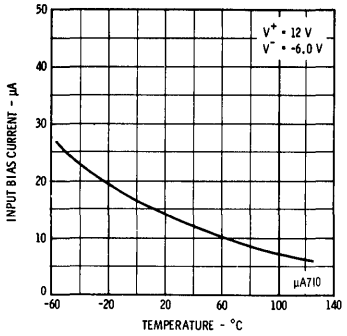
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



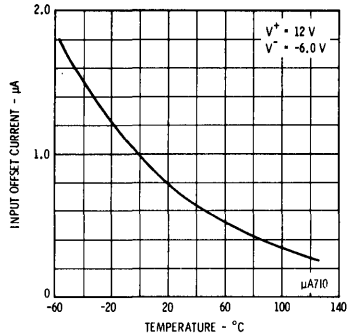
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



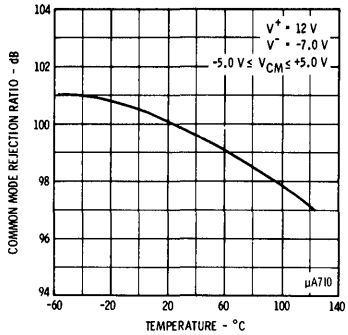
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



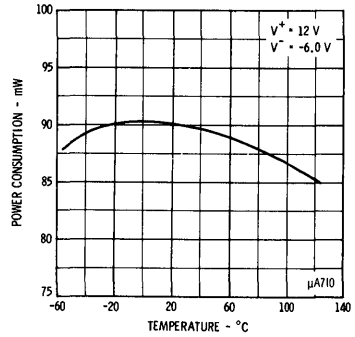
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



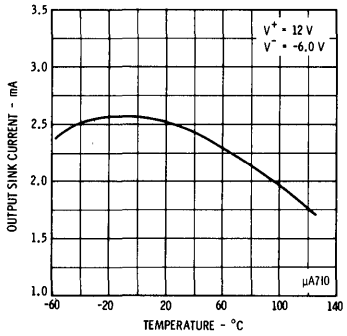
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



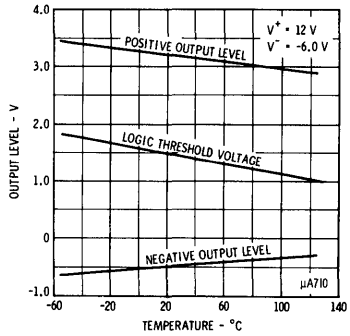
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



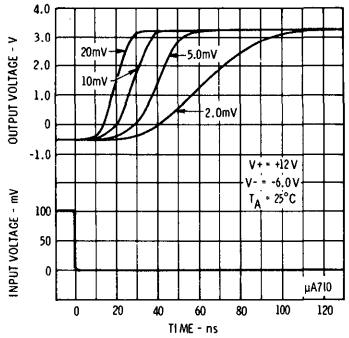
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



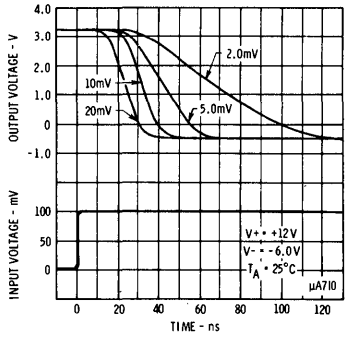
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



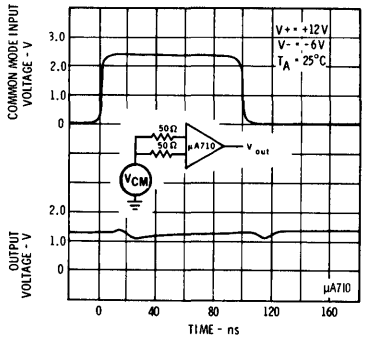
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

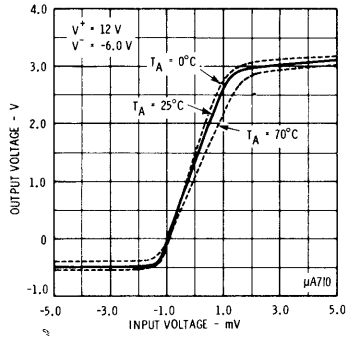


COMMON MODE PULSE RESPONSE

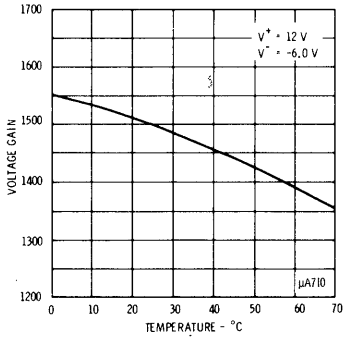


393 GRADE
TYPICAL PERFORMANCE CURVES

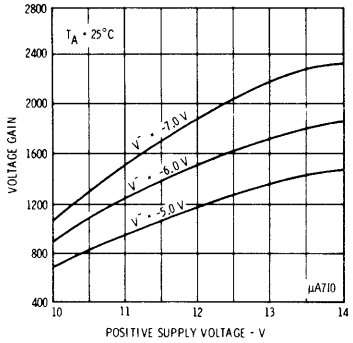
VOLTAGE TRANSFER CHARACTERISTIC



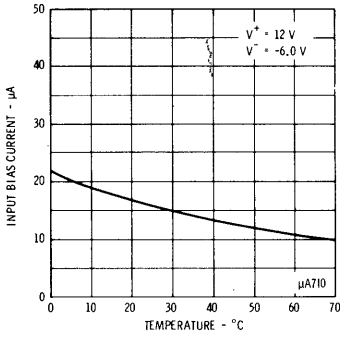
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



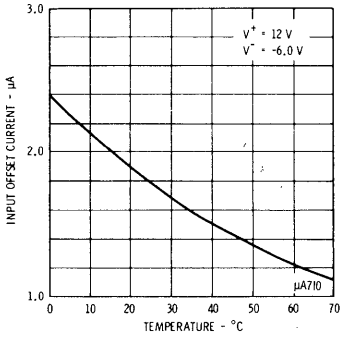
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



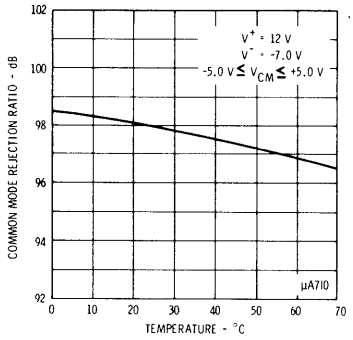
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



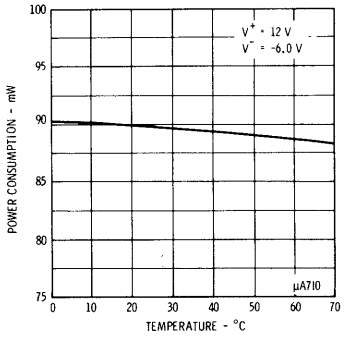
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



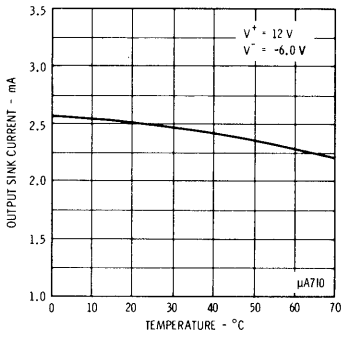
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



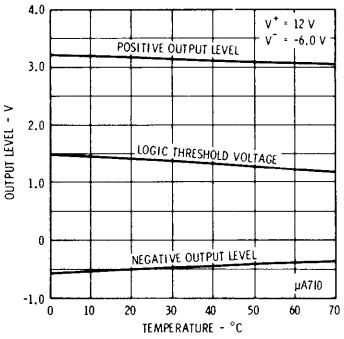
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



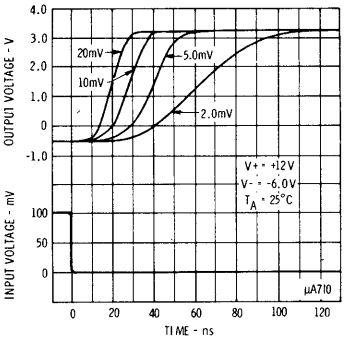
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



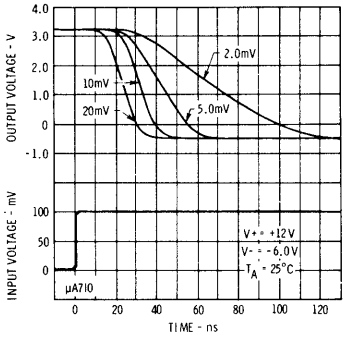
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



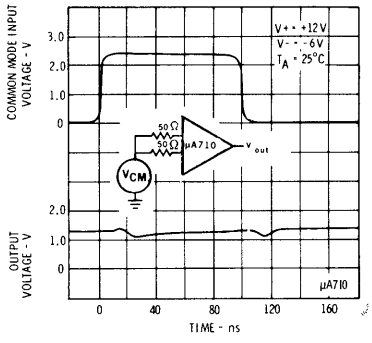
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



COMMON MODE PULSE RESPONSE



μA711
DUAL COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

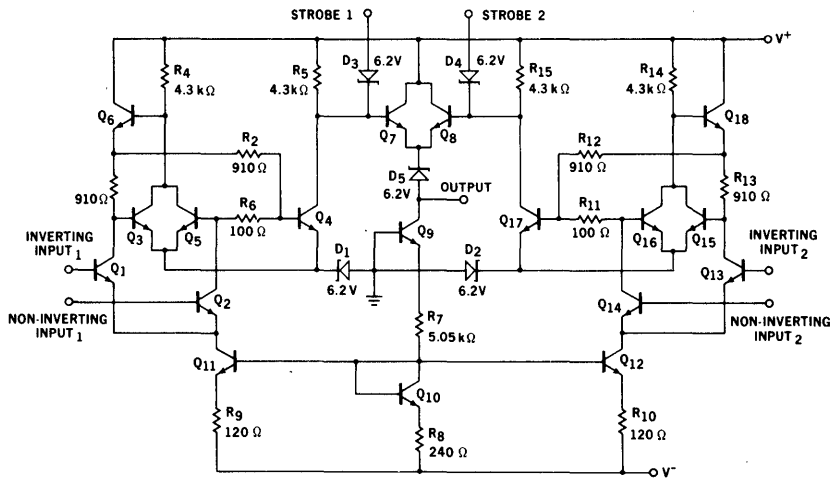
GENERAL DESCRIPTION — The μA711 is a dual, differential voltage comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double-ended limit detector for automatic Go/No-go test equipment. The μA711, which is similar to the μA710 differential comparator, is constructed using the Fairchild Planar* epitaxial process.

- **FAST RESPONSE TIME - 40 ns TYPICAL**
- **5 mV MAXIMUM OFFSET VOLTAGE**
- **10 μA MAXIMUM OFFSET CURRENT**
- **INDEPENDENT STROBING OF EACH COMPARATOR**

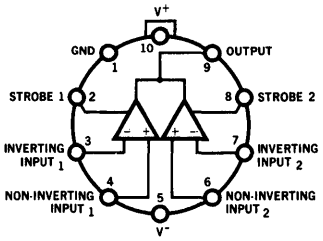
ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+14 V
Negative Supply Voltage	−7.0 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Strobe Voltage	0 to +6.0 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Ceramic DIP	670 mW
Flatpak	570 mW
Operating Temperature Range	
Military (312 Grade)	−55°C to +125°C
Commercial (393 Grade)	0°C to + 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	
Metal Can, Ceramic DIP and Flatpak (Soldering, 60 seconds)	300°C

EQUIVALENT CIRCUIT



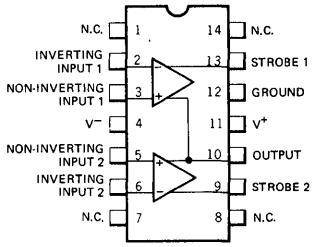
CONNECTION DIAGRAMS
(TOP VIEWS)
10 LEAD METAL CAN



Note: Pin 5 connected to case.

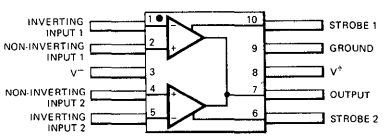
ORDER PART NOS. **U5F7711312**
U5F7711393

14 LEAD DIP



ORDER PART NOS.
FOR CERAMIC DIP: **U6A7711312**
U6A7711393

10 LEAD FLATPAK



ORDER PART NOS. **U3F7711312**

Notes on following page.

*Planar is a patented Fairchild process.

312 GRADE

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12 V, V^- = −6.0 V unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	V_{out} = +1.4 V, $R_S \leq 200\ \Omega$, V_{CM} = 0		1.0	3.5	mV
	V_{out} = +1.4 V, $R_S \leq 200\ \Omega$		1.0	5.0	mV
Input Offset Current	V_{out} = +1.4 V		0.5	10.0	μA
Input Bias Current			25	75	μA
Voltage Gain		750	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	V^- = −7.0 V	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Positive Output Level	$V_{in} \geq 10$ mV		4.5	5.0	V
Loaded Positive Output Level	$V_{in} \geq 10$ mV, I_O = 5 mA	2.5	3.5		V
Negative Output Level	$V_{in} \geq 10$ mV	−1.0	−0.5	0	V
Strobed Output Level	$V_{strobe} \leq 0.3$ V	−1.0		0	V
Output Sink Current	$V_{in} \geq 10$ mV, $V_{out} \geq 0$	0.5	0.8		mA
Strobe Current	V_{strobe} = 100 mV		1.2	2.5	mA
Positive Supply Current	$V_{out} \leq 0$		8.6		mA
Negative Supply Current			3.9		mA
Power Consumption			130	200	mW
The following specifications apply for −55°C ≤ T_A ≤ +125°C:					
Input Offset Voltage (Note 3)	$R_S \leq 200\ \Omega$, V_{CM} = 0			4.5	mV
	$R_S \leq 200\ \Omega$			6.0	mV
Input Offset Current (Note 3)				20	μA
Input Bias Current				150	μA
Temperature Coefficient of					
Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

NOTES

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can, 8.3 mW/°C for the Ceramic DIP, and 7.1 mW/°C for the Flatpak package.
2. The response time specified (see definitions) is for a 100 mV step input with 5 mV overdrive.
3. The input offset voltage is specified for a logic threshold as follows:
   312 Grade: 1.8 V at −55°C, 1.4 V at +25°C, 1.0 V at +125°C
   393 Grade: 1.5 V at 0°C, 1.4 V at +25°C, 1.2 V at +70°C

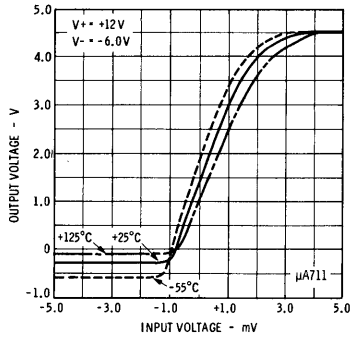
393 GRADE

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12 V, V^- = −6.0 V unless otherwise specified)

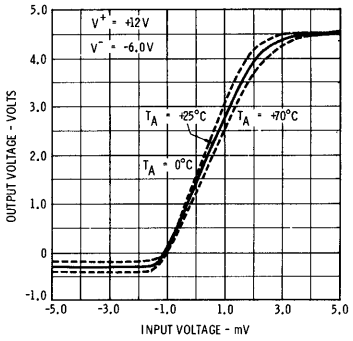
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	V_{out} = +1.4 V, $R_S \leq 200\ \Omega$, V_{CM} = 0		1.0	5.0	mV
	V_{out} = +1.4 V, $R_S \leq 200\ \Omega$		1.0	7.5	mV
Input Offset Current	V_{out} = +1.4 V		0.5	15	μA
Input Bias Current			25	100	μA
Voltage Gain		700	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	V^- = −7.0 V	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Positive Output Level	$V_{in} \geq 10$ mV		4.5	5.0	V
Loaded Positive Output Level	$V_{in} \geq 10$ mV, I_O = 5 mA	2.5	3.5		V
Negative Output Level	$V_{in} \geq 10$ mV	−1.0	−0.5	0	V
Strobed Output Level	$V_{strobe} \leq 0.3$ V	−1.0		0	V
Output Sink Current	$V_{in} \geq 10$ mV, $V_{out} \geq 0$	0.5	0.8		mA
Strobe Current	V_{strobe} = 100 mV		1.2	2.5	mA
Positive Supply Current	$V_{out} \leq 0$		8.6		mA
Negative Supply Current			3.9		mA
Power Consumption			130	230	mW
The following specifications apply for 0°C ≤ T_A ≤ +70°C:					
Input Offset Voltage (Note 3)	$R_S \leq 200\ \Omega$, V_{CM} = 0			6.0	mV
	$R_S \leq 200\ \Omega$			10	mV
Input Offset Current (Note 3)				25	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

TYPICAL PERFORMANCE CURVES

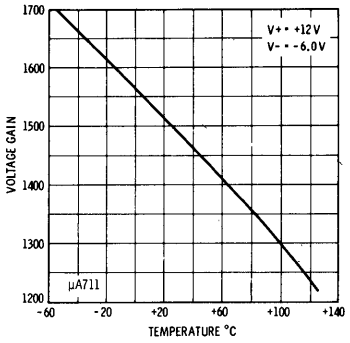
VOLTAGE TRANSFER CHARACTERISTIC 312 GRADE



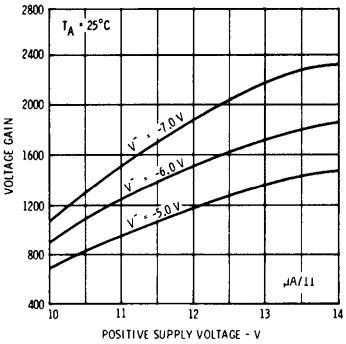
VOLTAGE TRANSFER CHARACTERISTIC 393 GRADE



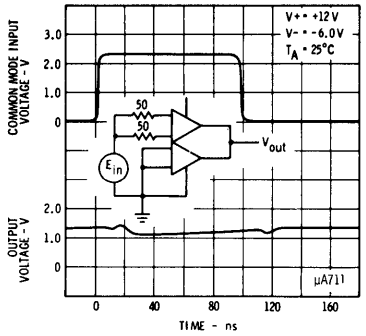
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



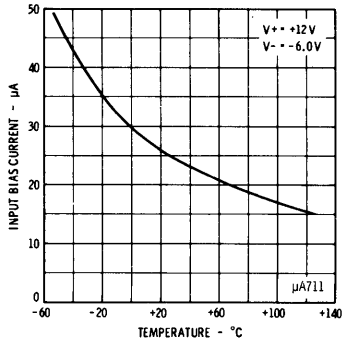
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



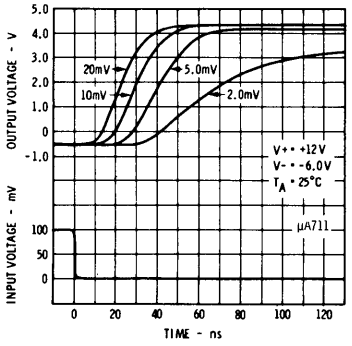
COMMON MODE PULSE RESPONSE



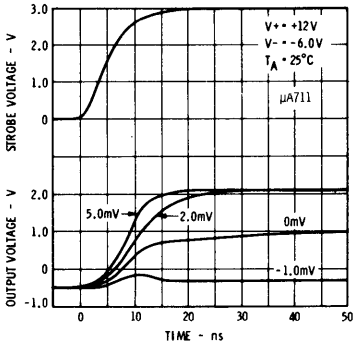
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



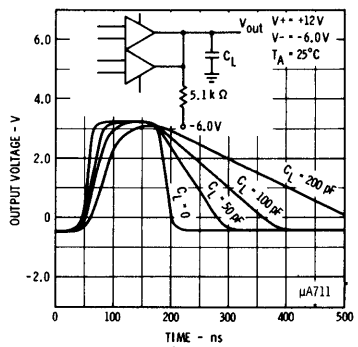
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



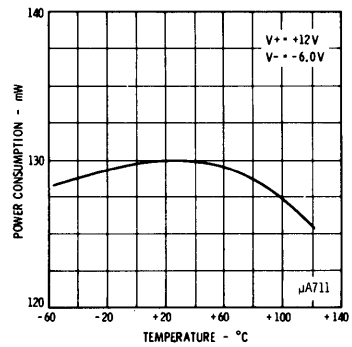
STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES



OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



μA715
HIGH SPEED OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

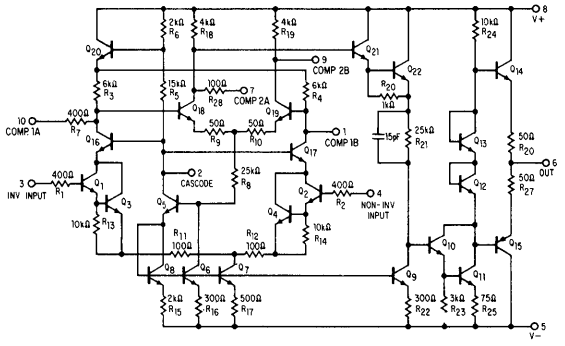
GENERAL DESCRIPTION – The μA715 is a high speed, high gain, monolithic operational amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It is intended for use in a wide range of applications where fast signal acquisition or wide bandwidth is required. The μA715 features fast settling time, high slew rate, low offsets, and high output swing for large signal applications. In addition, the device displays excellent temperature stability and will operate over a wide range of supply voltages. The μA715 is ideally suited for use in A to D and D to A converters, active filters, deflection amplifiers, video amplifiers, phase locked loops, multiplexed analog gates, precision comparators, sample and holds, and general feedback applications requiring DC wide bandwidth operation.

- **HIGH SLEW RATE . . . . . 100 V/μs**
- **FAST SETTLING TIME . . . . . 300 ns**
- **WIDE BANDWIDTH . . . . . 65 MHz**
- **WIDE OPERATING SUPPLY RANGE**
- **WIDE INPUT VOLTAGE RANGES**

ABSOLUTE MAXIMUM RATINGS

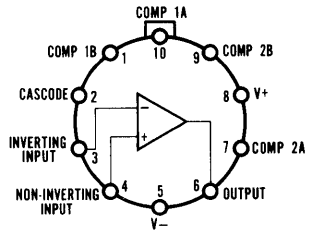
Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Ceramic DIP	670 mW
Differential Input Voltage	±15 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, Ceramic DIP	−65°C to +150°C
Operating Temperature Range	
Military (312 grade)	−55°C to +125°C
Commercial (393 grade)	0°C to +70°C
Lead Temperature (Soldering, 60 Seconds)	
Metal Can, Ceramic DIP	300°C

EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS

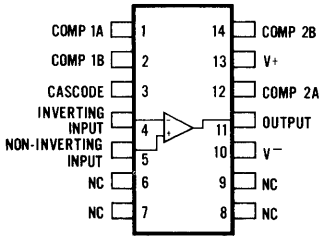
10 LEAD METAL CAN
(TOP VIEW)



ORDER PART NOS:

U5F7715312
U5F7715393

14 LEAD DIP
(TOP VIEW)



ORDER PART NOS:

For Ceramic DIP
U6A7715312
U6A7715393

Notes on following pages.

*Planar is a patented Fairchild process.

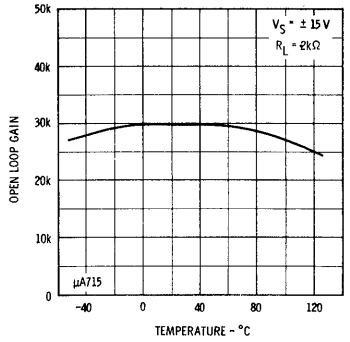
312 Grade

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise specified)

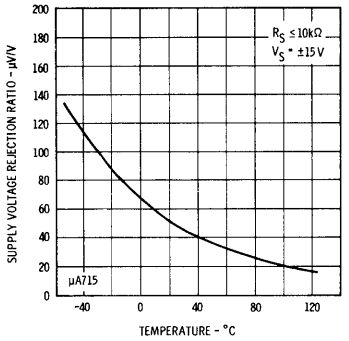
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10\ k\Omega$		2.0	5.0	mV
Input Offset Current			70	250	nA
Input Bias Current			400	750	nA
Input Resistance			1.0		MΩ
Input Voltage Range		±10	±12		Volts
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	15,000	30,000		
Output Resistance			75		Ω
Supply Current			5.5	7.0	mA
Power Consumption			165	210	mW
Acquisition Time (Unity Gain)	V_{OUT} = +5 V		800		ns
Settling Time (Unity Gain)			300		ns
Transient Response (Unity Gain)	V_{IN} = 400 mV				
Risetime			30	60	ns
Overshoot			25	40	%
Slew Rate	Av = 100		70		V/μs
	Av = 10		38		V/μs
	Av = 1 (non-inverting)	15	18		V/μs
	Av = 1 (inverting)		100		V/μs
The following apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10\ k\Omega$			7.5	mV
Input Offset Current	T_A = +125°C			250	nA
	T_A = −55°C			800	nA
Input Bias Current	T_A = +125°C			750	nA
	T_A = −55°C			4.0	μA
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	74	92		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		45	300	μV/V
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	10,000			
Output Voltage Swing	$R_L \geq 2\ k\Omega$	±10	±13		V

TYPICAL PERFORMANCE CURVES

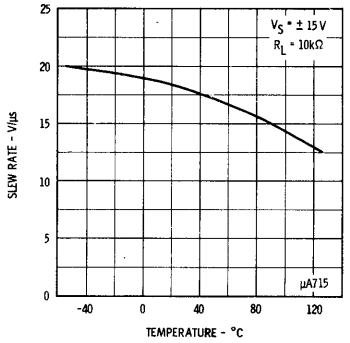
OPEN LOOP GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



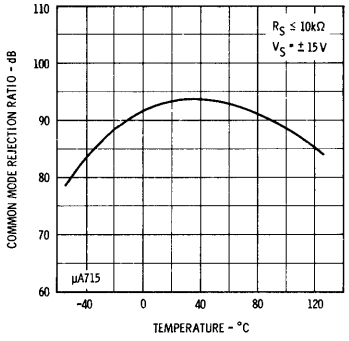
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



SLEW RATE AS A FUNCTION OF TEMPERATURE



COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



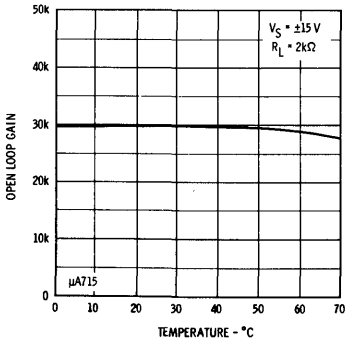
393 Grade

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25° C unless otherwise specified)

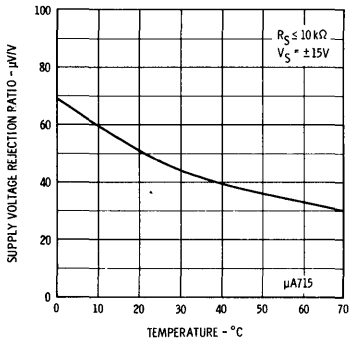
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	7.5	mV
Input Offset Current			70	250	nA
Input Bias Current			0.4	1.5	nA
Input Resistance			1.0		MΩ
Input Voltage Range		±10	±12		Volts
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	74	92		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		45	400	μV/V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	10,000	30,000		
Output Resistance			75		Ω
Supply Current			5.5	10	mA
Power Consumption			165	300	mW
Acquisition Time (Unity Gain)	V_{OUT} = +5 V		800		ns
Settling Time (Unity Gain			300		ns
Transient Response (Unity Gain)	V_{IN} = 400 mV				
Risetime			30	75	ns
Overshoot			25	50	%
Slew Rate	Av = 100		70		V/μs
	Av = 10		38		V/μs
	Av = 1 (non-inverting)	10	18		V/μs
	Av = 1 (inverting)		100		V/μs
The following apply for 0° C ≤ T_A ≤ +70° C:					
Input Offset Voltage	$R_S \leq 10$ kΩ			10	mV
Input Offset Current	T_A = +70° C			250	nA
	T_A = 0° C			750	nA
Input Bias Current	T_A = +70° C			1.5	μA
	T_A = 0° C			7.5	μA
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	8,000			
Output Voltage Swing	$R_L \geq 2$ kΩ	±10	±13		Volts

TYPICAL PERFORMANCE CURVES

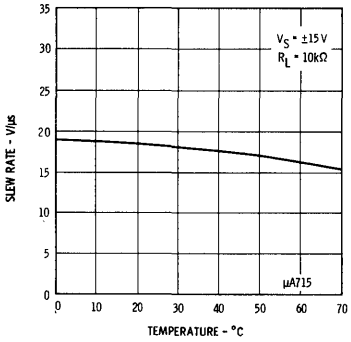
OPEN LOOP GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



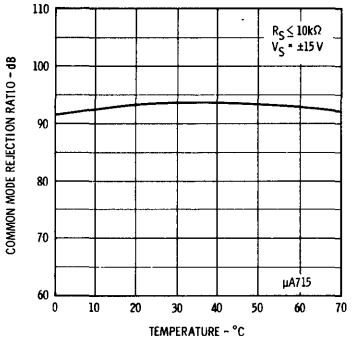
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



SLEW RATE AS A FUNCTION OF TEMPERATURE

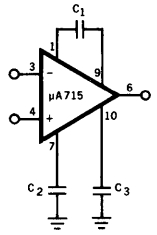


COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL PERFORMANCE CURVES FOR 312 AND 393 GRADES
(unless otherwise specified)

FREQUENCY COMPENSATION CIRCUIT

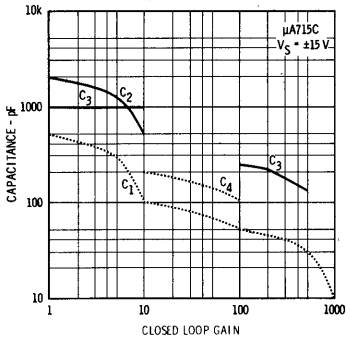


NON-INVERTING COMPENSATION COMPONENTS VALUES

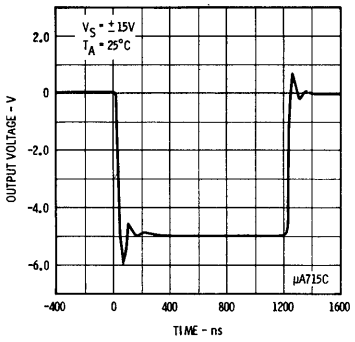
CLOSED LOOP GAIN	C_1	C_2	C_3
1000	10 pF	—	—
100	50 pF	—	250 pF
10	100 pF	500 pF	1000 pF
1	500 pF	2000 pF	1000 pF

*For Gain 10, compensation may be simplified by removing C_2, C_3 and adding a 200 pF capacitor (C_4) between Pin 7 and 10.

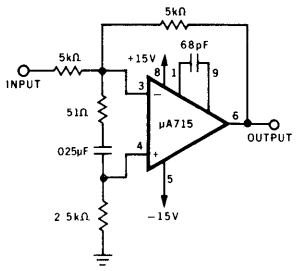
SUGGESTED VALUES OF COMPENSATION CAPACITORS AS A FUNCTION OF THE CLOSED LOOP GAIN



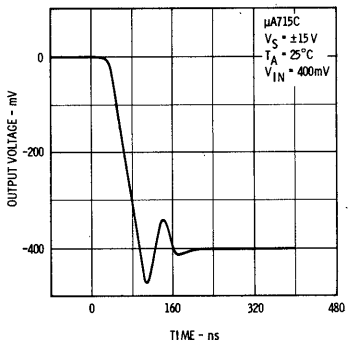
LARGE SIGNAL PULSE RESPONSE UNITY GAIN



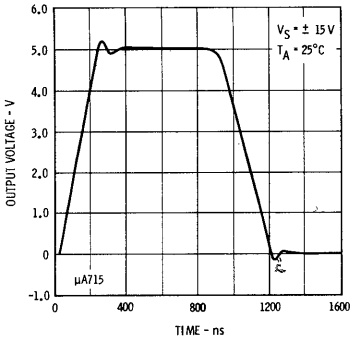
INVERTING UNITY GAIN HIGH SLEW RATE CIRCUIT



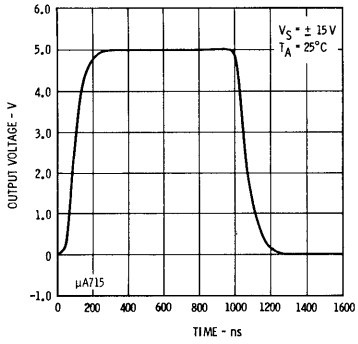
SMALL SIGNAL PULSE RESPONSE INVERTING UNITY GAIN



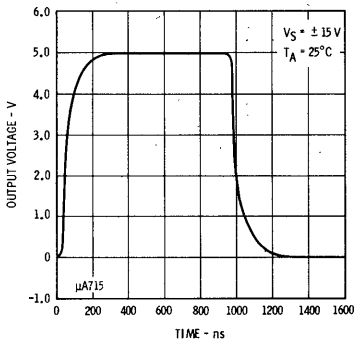
UNITY GAIN LARGE SIGNAL PULSE RESPONSE



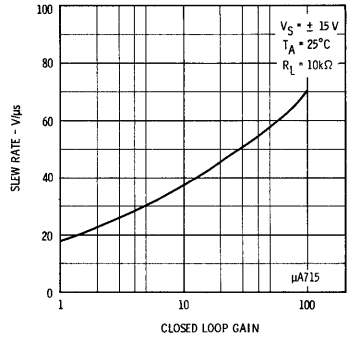
LARGE SIGNAL PULSE RESPONSE FOR GAIN 10



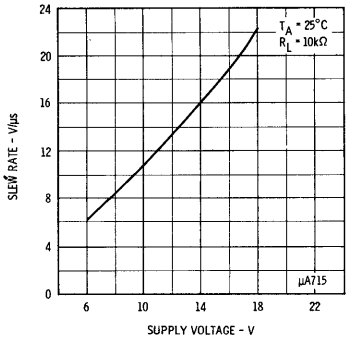
LARGE SIGNAL PULSE RESPONSE FOR GAIN 100



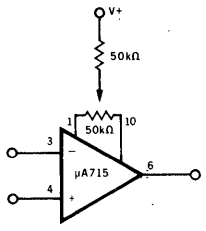
SLEW RATE AS A FUNCTION OF THE CLOSED LOOP GAIN



SLEW RATE AS A FUNCTION OF SUPPLY VOLTAGE



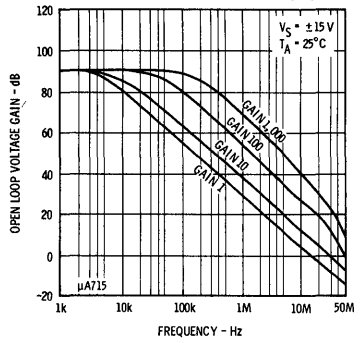
VOLTAGE OFFSET NULL CIRCUIT



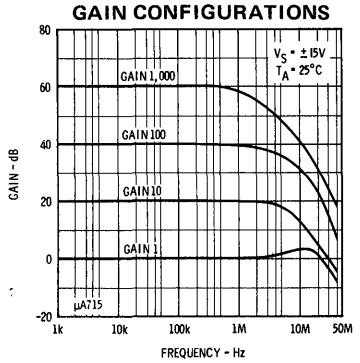
TYPICAL PERFORMANCE CURVES FOR 312 AND 393 GRADES

(unless otherwise specified)

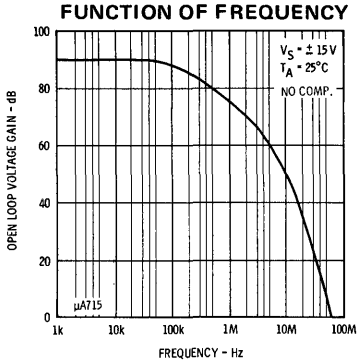
OPEN LOOP RESPONSE WITH COMPENSATION NECESSARY FOR VARIOUS CLOSED LOOP GAIN CONFIGURATIONS



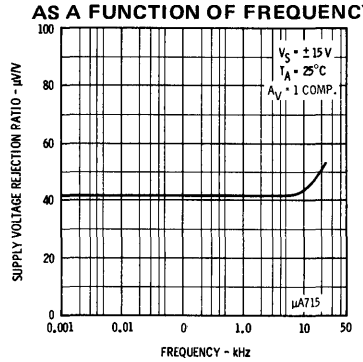
CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS GAIN CONFIGURATIONS



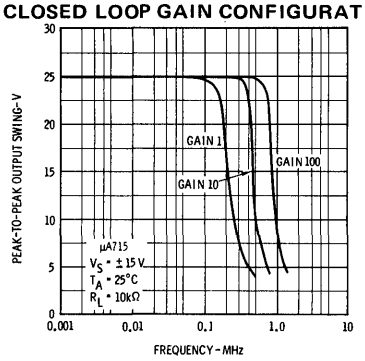
OPEN LOOP GAIN AS A FUNCTION OF FREQUENCY



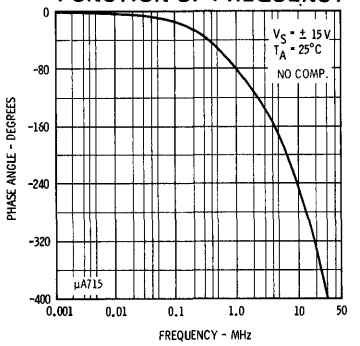
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF FREQUENCY



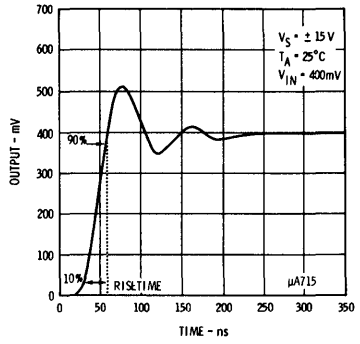
OUTPUT SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS CLOSED LOOP GAIN CONFIGURATIONS



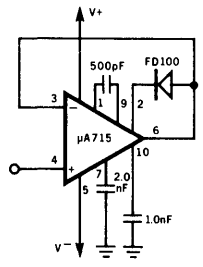
OPEN LOOP PHASE AS A FUNCTION OF FREQUENCY



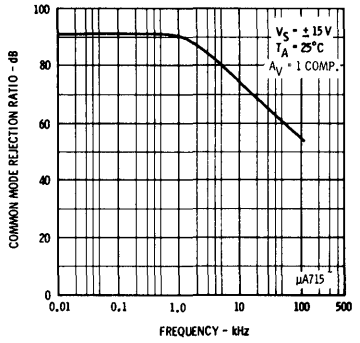
VOLTAGE FOLLOWER TRANSIENT RESPONSE



VOLTAGE FOLLOWER



COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY

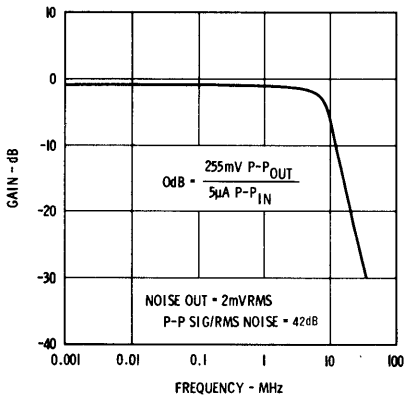


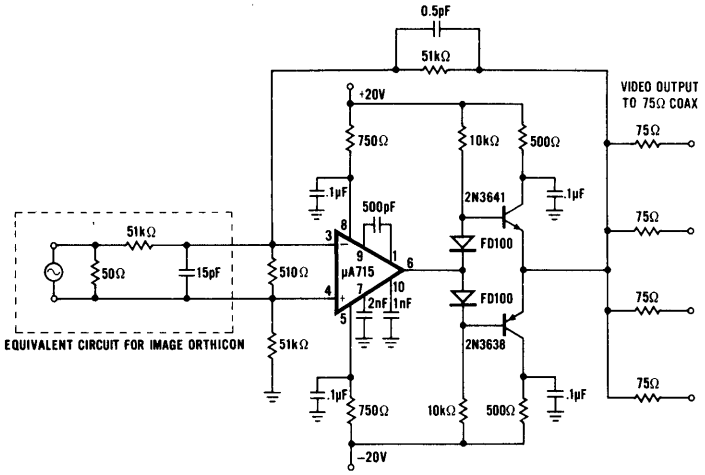
NOTES

1. Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for Metal Can and 8.3 mW/°C for the Ceramic DIP package.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

TYPICAL APPLICATIONS

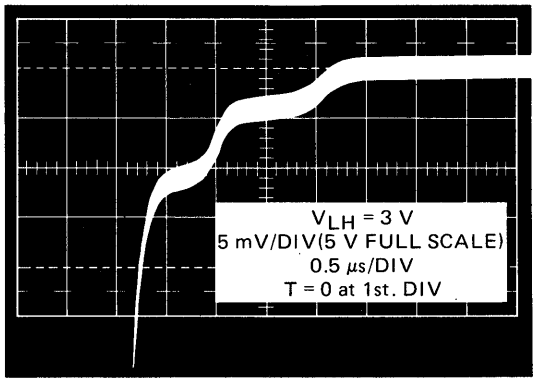
WIDE BAND VIDEO AMPLIFIER WITH 75 Ω COAX CABLE DRIVE CAPABILITY



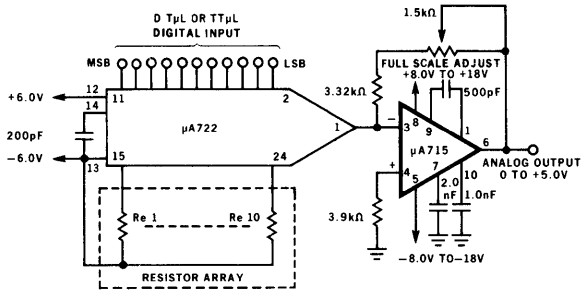


HIGH SPEED 10 BIT DIGITAL TO ANALOG CONVERTER

ANALOG OUTPUT 0 TO +5.0 V



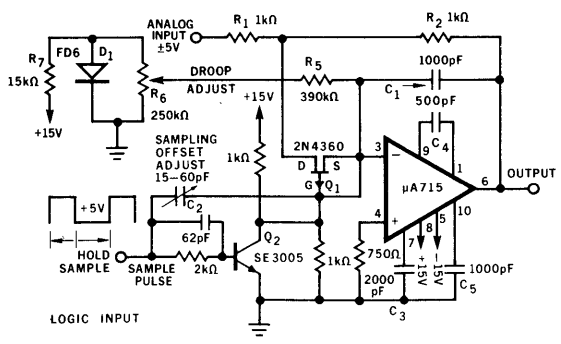
μA722/μA715 op amp switching ON, as it should with typical logic voltage on least significant bits. Note complete absence of ringing.



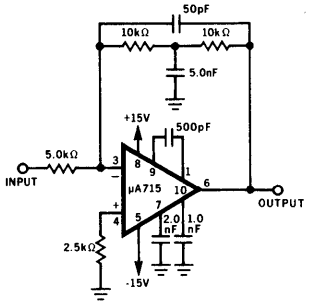
Conversion Rate
6 bits - 300 ns
8 bits - 600 ns
10 bits - 1000 ns

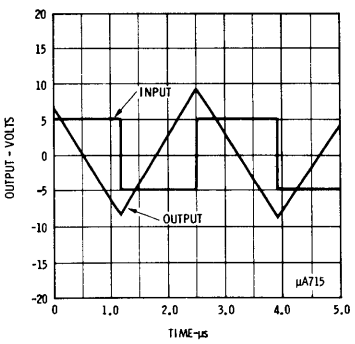
NOTE:
Contact Fairchild for additional information including how to increase conversion speed by clamping LSB's and how to obtain bipolar outputs.

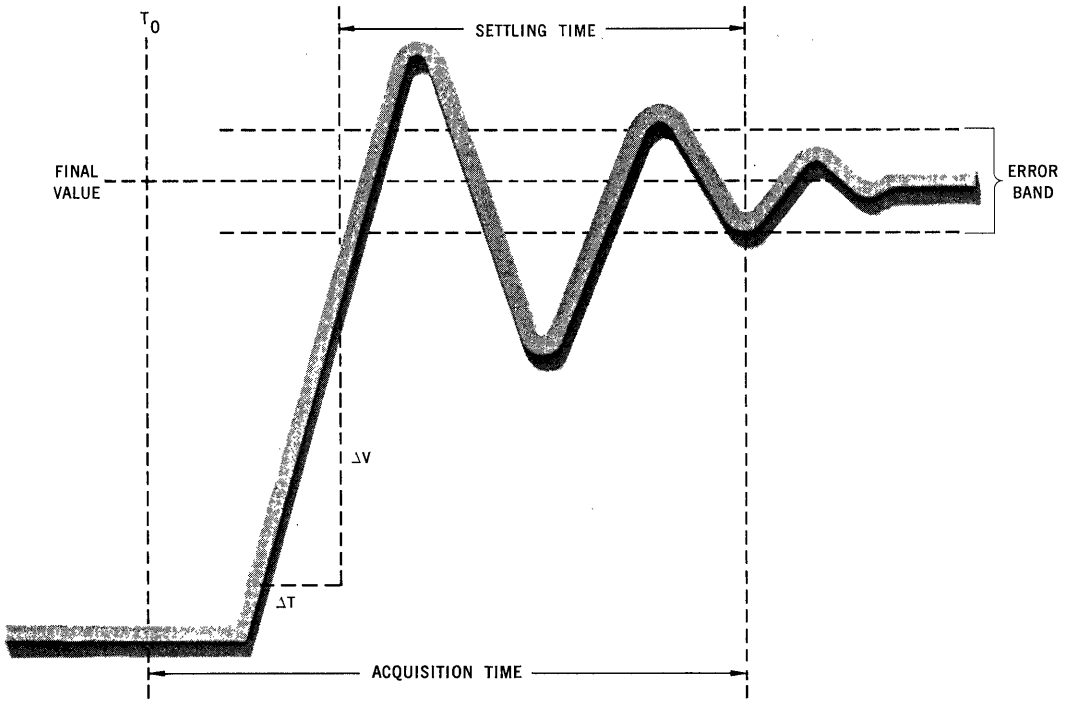
HIGH SPEED SAMPLE AND HOLD



HIGH SPEED INTEGRATOR







HELPFUL HINTS

LAYOUT – The layout should be such that stray capacitance is minimal.

SUPPLIES – The supplies should be adequately bypassed. Use of 0.1 μF high quality ceramic capacitors is recommended.

RINGING – Excessive ringing (long acquisition time) may occur with large capacitive loads. This may be reduced by isolating the capacitive load with a resistance of 100 Ω. Large source resistances may also give rise to the same problem and this may be decreased by the addition of a capacitance across the feedback resistance. A value of around 50 pF for unity gain configuration and around 3.0 pF for gain 10 should be adequate.

LATCH UP – This may occur when the amplifier is used as a voltage follower. The inclusion of a diode between pins 6 and 2 with the cathode towards pin 2 is the recommended preventive.

μA716
FIXED-GAIN, LOW DISTORTION AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

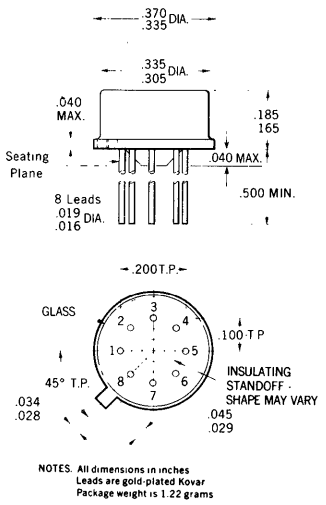
GENERAL DESCRIPTION — The μA716 is a fixed-gain, medium power amplifier intended for use as a telephone system channel amplifier, headset amplifier or general purpose audio amplifier. It provides medium output current capability, low distortion, excellent gain stability, and wide bandwidth. Fixed voltage gains of 10, 20, 100 and 200 are available by selecting external taps.

ABSOLUTE MAXIMUM RATINGS:

Supply Voltage	27 V
Internal Power Dissipation	500 mW
Input Voltage	±5 V
Peak Output Current ($T_A = 25°C$)	100 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C

PHYSICAL DIMENSIONS

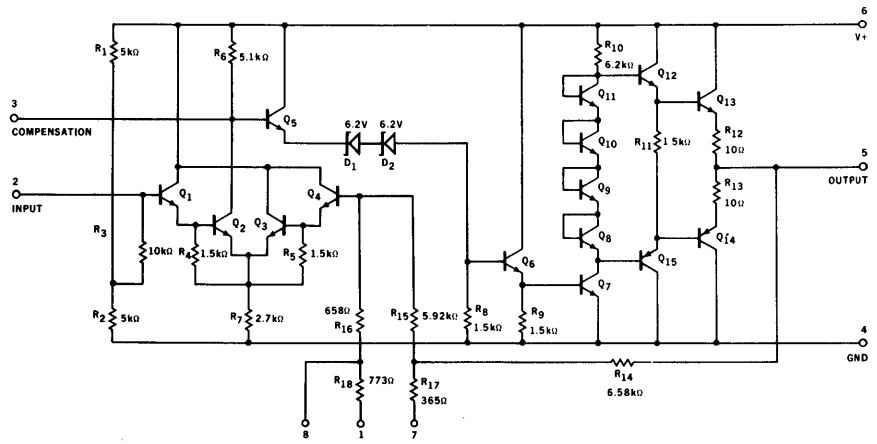
in accordance with JEDEC(TO-99) outline



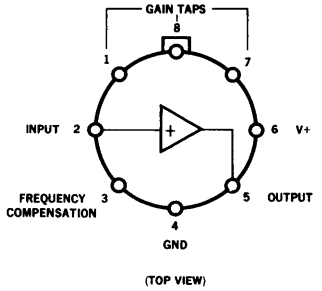
NOTES. All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO.U5B7716393

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



(TOP VIEW)

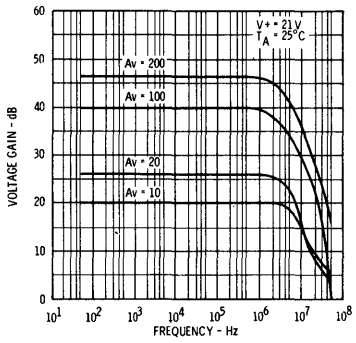
NOTE: Pin 4 internally connected to case.

ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V^+ = 21V$ unless otherwise specified)

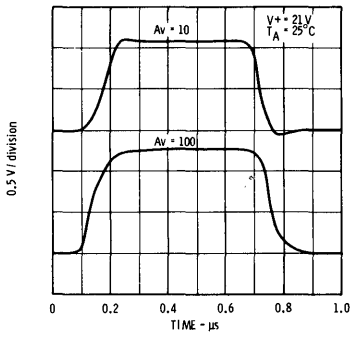
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Quiescent Power Consumption	$T_A = 25°C$		280	350	mW
Total Harmonic Distortion	$A_V = 10$, $f = 1$ kHz, $P_O = 50$ mW, $R_L = 150\ \Omega$		0.01	0.05	%
	$A_V = 100$, $f = 1$ kHz, $P_O = 50$ mW, $R_L = 150\ \Omega$		0.10	0.50	%
Input Noise Voltage	$R_S = 600\ \Omega$, $T_A = 25°C$, $B_n = 16$ Hz to 150 kHz		8.0		μV_{rms}
Output Voltage Swing	$R_L = 150\ \Omega$	10	14		V_{p-p}
	$R_L \geq 5k\ \Omega$	15	17		V_{p-p}
Input Resistance		9.0	11		kΩ
Output Resistance			1.0		Ω
Voltage Gain	See Table I				
10x		9.0	10	11	
20x		18	20	22	
100x		95	105	115	
200x		185	205	225	
Bandwidth	$T_A = 25°C$		2.0		MHz
Temperature Stability of Voltage Gain	$T_{ref} = 25°C$				
10x			±0.02	±0.25	dB
20x			±0.02	±0.25	dB
100x			±0.02	±0.25	dB
200x			±0.05	±0.50	dB

TYPICAL PERFORMANCE CURVES

VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

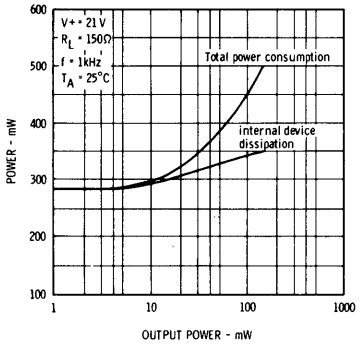


TRANSIENT RESPONSE

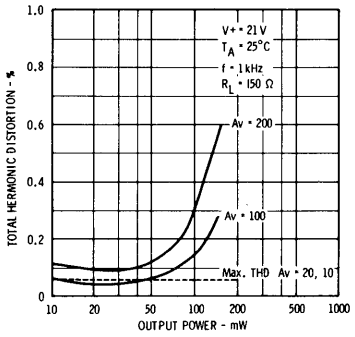


TYPICAL PERFORMANCE CURVES

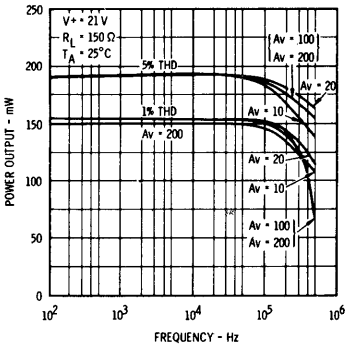
TOTAL POWER CONSUMPTION AND INTERNAL DEVICE DISSIPATION AS A FUNCTION OF OUTPUT POWER



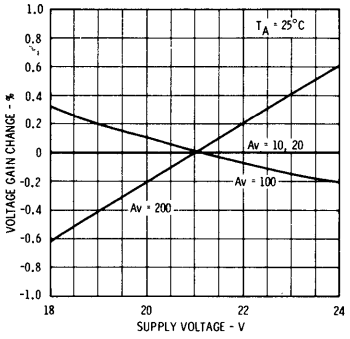
TOTAL HARMONIC DISTORTION AS A FUNCTION OF OUTPUT POWER



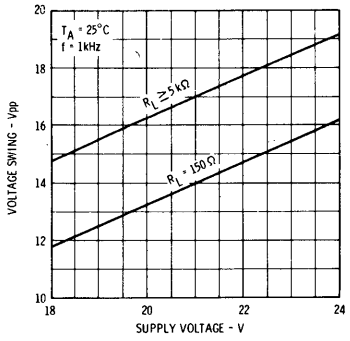
POWER OUTPUT AS A FUNCTION OF FREQUENCY 5% AND 1% THD



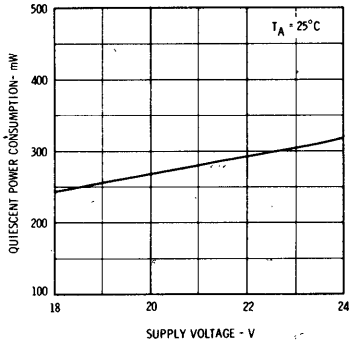
RELATIVE VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



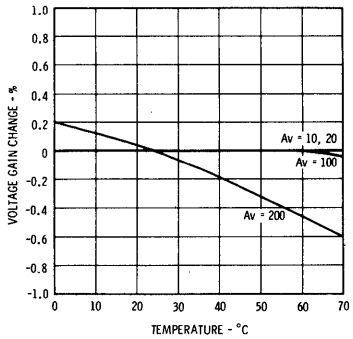
VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



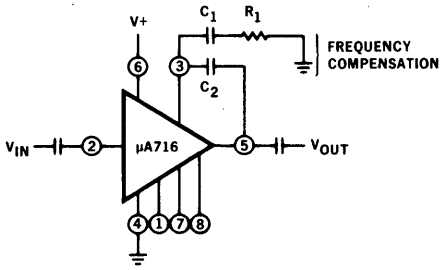
QUIESCENT POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



RELATIVE VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



CONNECTION DIAGRAM AND COMPONENT TABLE FOR AVAILABLE GAIN OPTIONS



Voltage Gain	C_1	C_2	R_1	Decouple Pins:
10	68 pF	39 pF	75 Ω	1
20	50 pF	27 pF	75 Ω	8
100	None	3 pF	None	1, 7
200	None	3 pF	None	7, 8

TABLE I

μA722
10-BIT CURRENT SOURCE
FAIRCHILD LINEAR INTEGRATED CIRCUITS

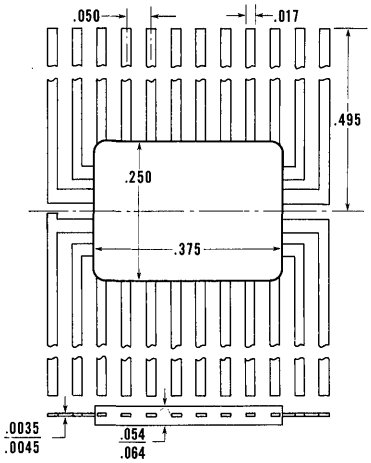
GENERAL DESCRIPTION — The μA722 is a high-speed, 10-bit precision current source intended for use in current-summing digital-to-analog converters or as the feedback element in successive approximation analog-to-digital converters. It is constructed on a single silicon chip, using the Fairchild Planar* epitaxial process, and consists of a reference supply, 10 current sources connected to a single output summing line, and associated logic switches. The full-scale current and coding format are set by an external resistor array, which may be preselected and fixed for general usage or trimmed for greater accuracy. The μA722 is compatible with the Fairchild families of linear and digital circuits.

- **8 ± ½ BIT ACCURACY FROM 0°C TO +55°C**
- **7±½ BIT ACCURACY FROM −20°C TO +85°C**
- **600 ns SWITCHING SPEED**
- **INTERNAL PRECISION REFERENCE**
- **TTL COMPATIBLE**

ABSOLUTE MAXIMUM RATINGS

Voltage from V^+ to V^-	−0.5 V to +18 V
Voltage from Output to V^+	−12 V to +6 V
Voltage from Output to V^-	0 V to +12 V
Voltage from Logic Inputs to Output	−9 V to +7 V
Voltage from Logic Inputs to V^+	−18 V to 0 V
Voltage from Logic Inputs to V^-	0 V to +12 V
Internal Power Dissipation (Note 1)	450 mW
Operating Temperature Range	−20°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

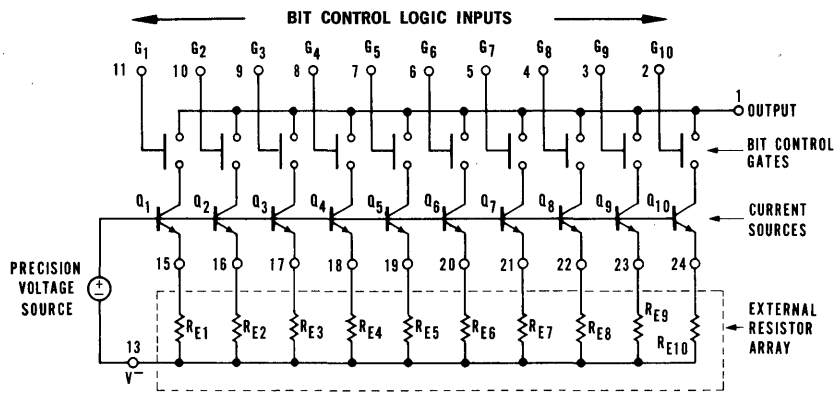
PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)



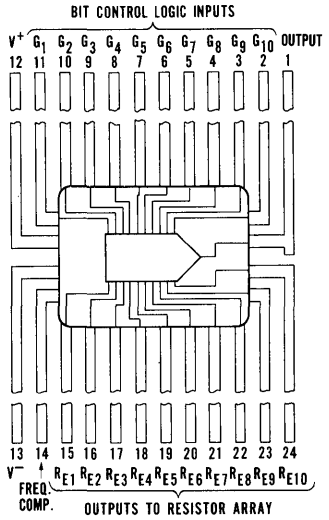
ORDER PART NOS.:

U3M7722333
U3M7722334

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



NOTE: PIN 13 INTERNALLY CONNECTED TO CASE.

Notes on following pages.

*Planar is a patented Fairchild process.

(333 GRADE)

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS (Note 2)	MIN.	TYP.	MAX.	UNITS
Resolution				10	Bits
Absolute Error	$T_A = 25°C$		±.07	±.20	%
	$0°C \leq T_A \leq +55°C$		±.10	±.20	%
	$-20°C \leq T_A \leq +85°C$		±.13	±.39	%
Output Current					
Full-Scale	Logic Inputs = 0.4 V	2160	2560	3000	μA
Zero-Scale	Logic Inputs = 2.5 V		±.002	±.25	μA
Power Supply Rejection	$\Delta V^+ = \Delta V^- = \pm 5\%$		±.06	±0.1	%/%
Output Resistance		0.2	1.2		MΩ
Switching Speed			600		ns
Logic Input High Voltage		2.1	2.5		V
Logic Input Low Voltage			0.4	0.7	V
Power Consumption			165	250	mW

(334 GRADE)

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS (Note 2)	MIN.	TYP.	MAX.	UNITS
Resolution				10	Bits
Absolute Error	$T_A = 25°C$		±.08	±.39	%
	$0°C \leq T_A \leq +55°C$		±.17	±.39	%
	$-20°C \leq T_A \leq +85°C$		±.22	±.78	%
Output Current					
Full-Scale	Logic Inputs = 0.4 V	2160	2560	3000	μA
Zero-Scale	Logic Inputs = 2.5 V		±.002	±.25	μA
Power Supply Rejection	$\Delta V^+ = \Delta V^- = \pm 5\%$		±.06	±0.1	%/%
Output Resistance		0.2	1.2		MΩ
Switching Speed			600		ns
Logic Input High Voltage		2.1	2.5		V
Logic Input Low Voltage			0.4	0.7	V
Power Consumption			165	250	mW

NOTES:

(1) Rating applies for ambient temperatures to +85°C.

(2) Unless otherwise specified, $T_A = 25°C$, $V^+ = 6.00$ V ± .01 V, $V^- = -6.00$ V ± .01 V, $V_{out} = 0$ V, $C_I = 200$ pF, and external resistor array as per Table 1.

(3) In Table 1, the maximum absolute value tolerance for $R_{E1} = \pm 10\%$.

TYPICAL FULL-SCALE OUTPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

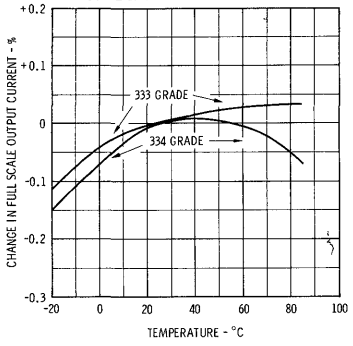
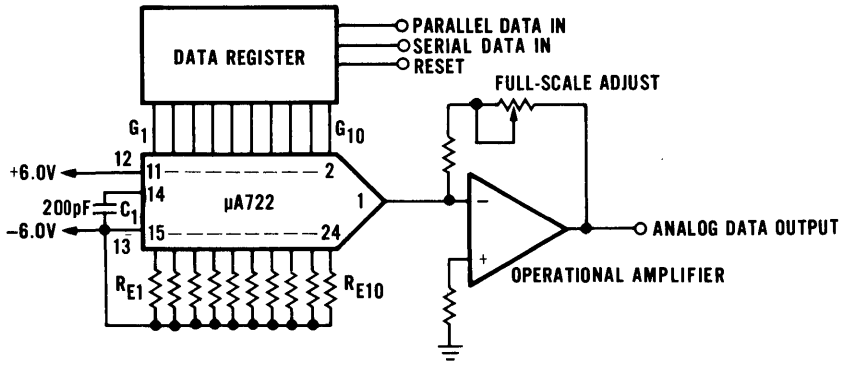


TABLE 1

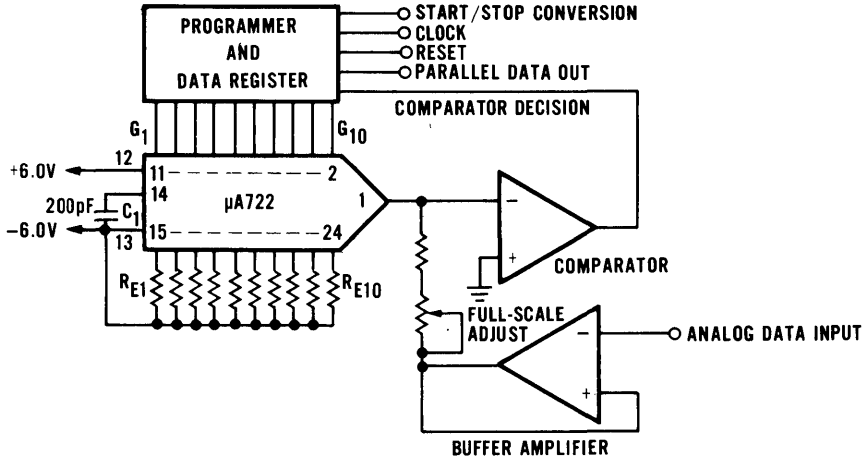
BINARY CODE RESISTOR ARRAY FOR 8 ± ½ BIT ACCURACY

			333 GRADE		334 GRADE	
Resistor Number (R_{EJ})	Nominal Value (kΩ)	Nominal Ratio (R_{EJ}/R_{E1})	Max. Ratio Tolerance ($T_A = 25°C$) (%)	Max. Ratio Temp. Coeff. (ppm/°C)	Max. Ratio Tolerance ($T_A = 25°C$) (%)	Max. Ratio Temp. Coeff. (ppm/°C)
R_{E1}	2.547	1.000	Note 3	±5	Note 3	±20
R_{E2}	5.094	2.000	±0.02	±5	±0.10	±20
R_{E3}	10.245	4.022	±0.05	±10	±0.20	±50
R_{E4}	20.60	8.088	±0.10	±20	±0.20	±50
R_{E5}	41.43	16.265	±0.20	±20	±0.50	±100
R_{E6}	81.93	32.17	±0.20	±50	±0.50	±100
R_{E7}	163.4	64.16	±0.50	±100	±1.0	±500
R_{E8}	325.7	127.9	±1.0	±200	±1.0	±500
R_{E9}	644.9	253.2	±2.0	±500	±5.0	±1000
R_{E10}	1275	500.8	±2.0	±500	±5.0	±1000

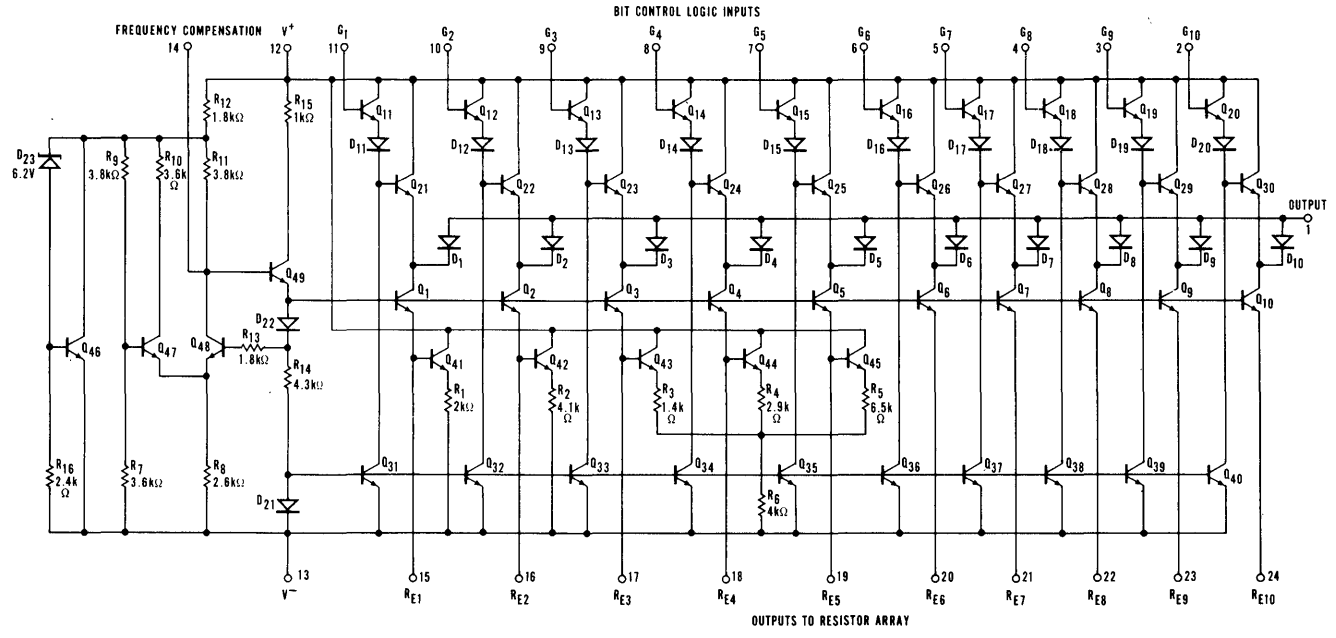
TYPICAL DIGITAL-TO-ANALOG CONVERTER



TYPICAL ANALOG-TO-DIGITAL CONVERTER



SCHEMATIC DIAGRAM



μA723
PRECISION VOLTAGE REGULATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

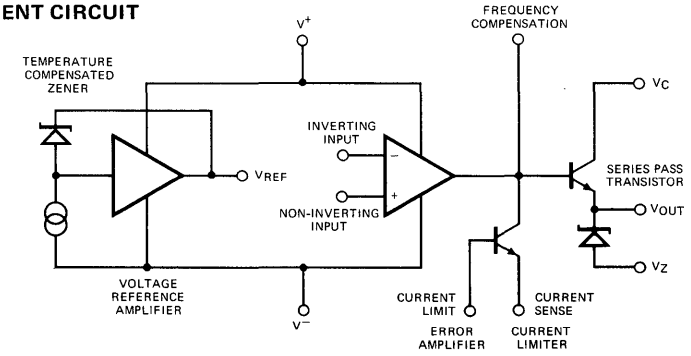
GENERAL DESCRIPTION – The μA723 is a monolithic voltage regulator constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The μA723 is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems and other power supplies for digital and linear circuits.

- **POSITIVE OR NEGATIVE SUPPLY OPERATION**
- **SERIES, SHUNT, SWITCHING OR FLOATING OPERATION**
- **.01% LINE AND LOAD REGULATION**
- **OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37 VOLTS**
- **OUTPUT CURRENT TO 150 mA WITHOUT EXTERNAL PASS TRANSISTOR**

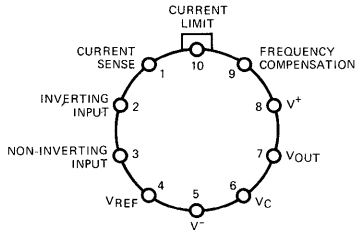
ABSOLUTE MAXIMUM RATINGS

Pulse Voltage from V^+ to V^-, (50 ms) (312 Grade)	50 V
Continuous Voltage from V^+ to V^-	40 V
Input-Output Voltage Differential	40 V
Differential Input Voltage	±5 V
Voltage Between Non-Inverting Input and V^-	+8 V
Current from V_Z	25 mA
Current from V_{REF}	15 mA
Internal Power Dissipation (Note 1)	
Metal Can	800 mW
Ceramic DIP	1000 mW
Silicone DIP	620 mW
Storage Temperature Range	
Metal Can, Ceramic DIP	−65°C to +150°C
Silicone DIP	−55°C to +125°C
Operating Temperature Range	
Military (312 Grade)	−55°C to +125°C
Commercial (393 Grade)	0°C to + 70°C
Lead Temperature	
Metal Can, Ceramic DIP (Soldering, 60 seconds)	300°C
Silicone DIP (Soldering, 10 seconds)	260°C

EQUIVALENT CIRCUIT



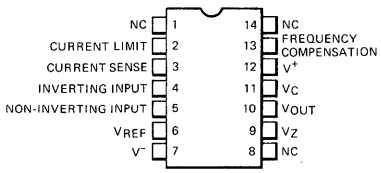
CONNECTION DIAGRAMS
(TOP VIEW)
10 LEAD METAL CAN



Note: Pin 5 connected to case.

ORDER PART NOS: U5R7723312
U5R7723393

14 LEAD DIP
(TOP VIEW)



FOR CERAMIC DIP
ORDER PART NOS.: U6A7723312
U6A7723393

FOR SILICONE DIP
ORDER PART NO.: U9A772393

Notes on following pages.

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (Note 2) (312 GRADE)

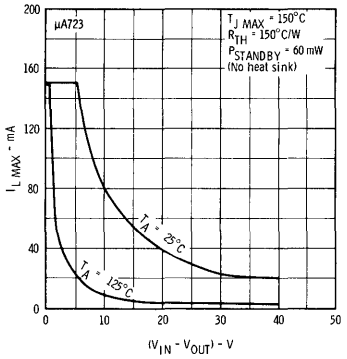
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Line Regulation	$V_{IN} = 12$ V to $V_{IN} = 15$ V		.01	0.1	% V_{OUT}
	$V_{IN} = 12$ V to $V_{IN} = 40$ V		.02	0.2	% V_{OUT}
	$-55°C \leq T_A \leq +125°C$, $V_{IN} = 12$ V to $V_{IN} = 15$ V			0.3	% V_{OUT}
Load Regulation	$I_L = 1$ mA to $I_L = 50$ mA		.03	0.15	% V_{OUT}
	$-55°C \leq T_A \leq +125°C$, $I_L = 1$ mA to $I_L = 50$ mA			0.6	% V_{OUT}
Ripple Rejection	f = 50 Hz to 10 kHz, $C_{REF} = 0$		74		dB
	f = 50 Hz to 10 kHz, $C_{REF} = 5$ μF		86		dB
Average Temperature Coefficient of Output Voltage	$-55°C \leq T_A \leq +125°C$		.002	.015	%/°C
Short Circuit Current Limit	$R_{SC} = 10\ \Omega$, $V_{OUT} = 0$		65		mA
Reference Voltage		6.95	7.15	7.35	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, $C_{REF} = 0$		20		μV_{rms}
	BW = 100 Hz to 10 kHz, $C_{REF} = 5$ μF		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	$I_L = 0$, $V_{IN} = 30$ V		2.3	3.5	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input-Output Voltage Differential		3.0		38	V

ELECTRICAL CHARACTERISTICS (Note 2) (393 GRADE)

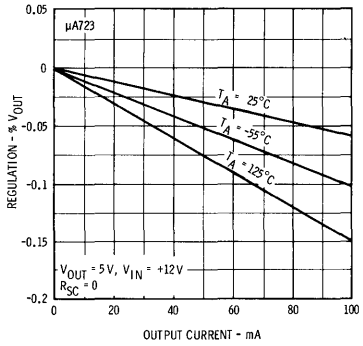
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Line Regulation	$V_{IN} = 12$ V to $V_{IN} = 15$ V		.01	0.1	% V_{OUT}
	$V_{IN} = 12$ V to $V_{IN} = 40$ V		0.1	0.5	% V_{OUT}
	$0°C \leq T_A \leq 70°C$, $V_{IN} = 12$ V to $V_{IN} = 15$ V			0.3	% V_{OUT}
Load Regulation	$I_L = 1$ mA to $I_L = 50$ mA		.03	0.2	% V_{OUT}
	$0°C \leq T_A \leq 70°C$, $I_L = 1$ mA to $I_L = 50$ mA			0.6	% V_{OUT}
Ripple Rejection	f = 50 Hz to 10 kHz, $C_{REF} = 0$		74		dB
	f = 50 Hz to 10 kHz, $C_{REF} = 5$ μF		86		dB
Average Temperature Coefficient of Output Voltage	$0°C \leq T_A \leq 70°C$		.003	.015	%/°C
Short Circuit Current Limit	$R_{SC} = 10\ \Omega$, $V_{OUT} = 0$		65		mA
Reference Voltage		6.80	7.15	7.50	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, $C_{REF} = 0$		20		μV_{rms}
	BW = 100 Hz to 10 kHz, $C_{REF} = 5$ μF		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	$I_L = 0$, $V_{IN} = 30$ V		2.3	4.0	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input-Output Voltage Differential		3.0		38	V

TYPICAL PERFORMANCE CURVES (312 GRADE)

MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



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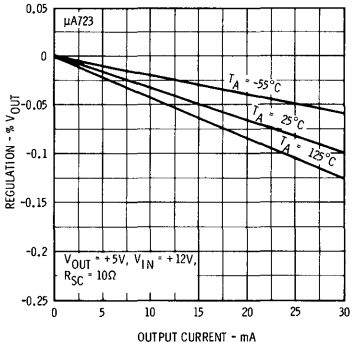
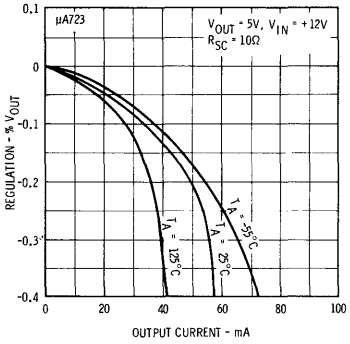
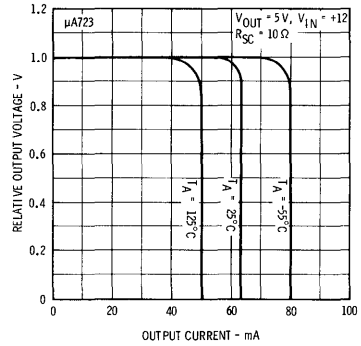


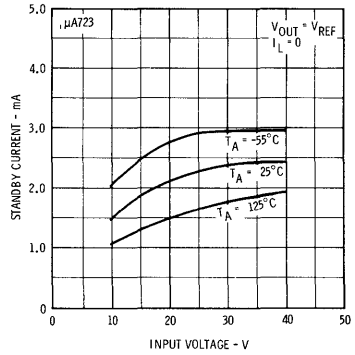
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



CURRENT LIMITING CHARACTERISTICS

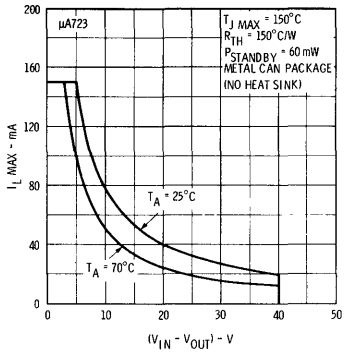


STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

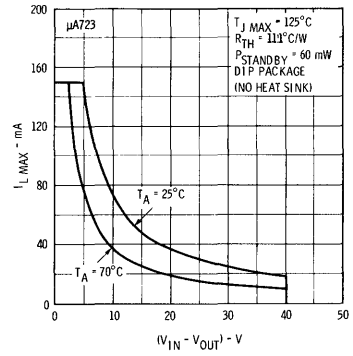


TYPICAL PERFORMANCE CURVES (393 GRADE)

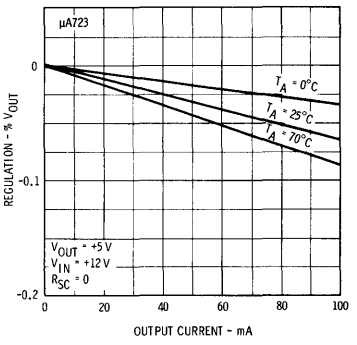
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



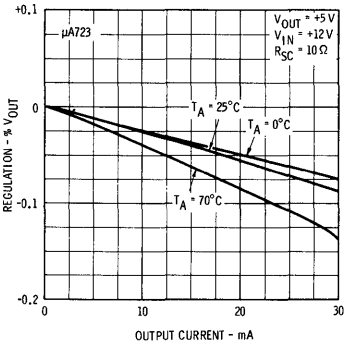
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



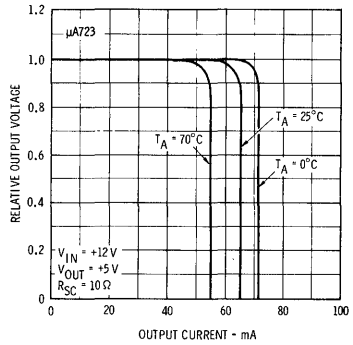
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



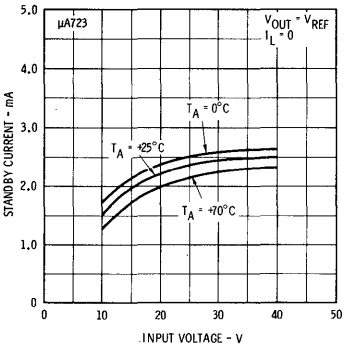
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



CURRENT LIMITING CHARACTERISTICS

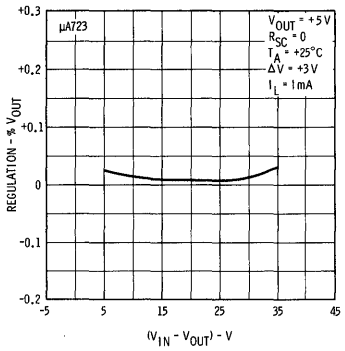


STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE

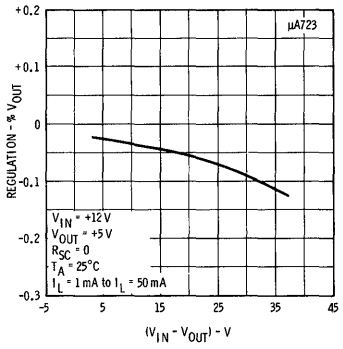


TYPICAL PERFORMANCE CURVES (FOR 312 AND 393 GRADES)

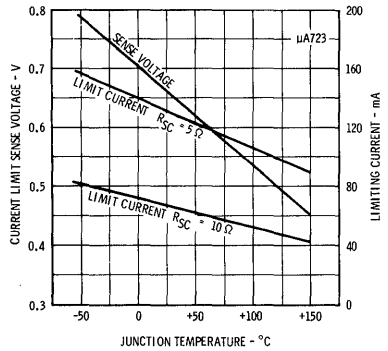
LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



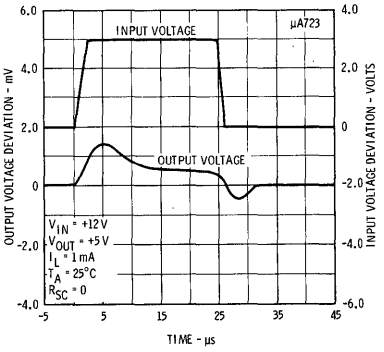
LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



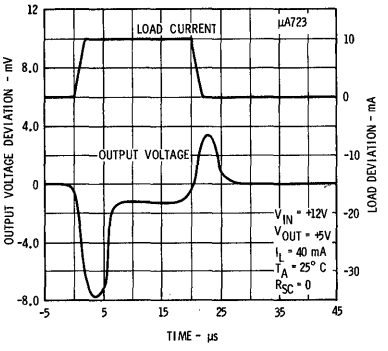
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



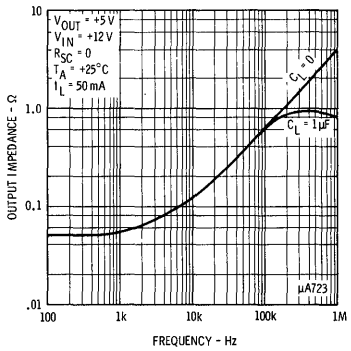
LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



NOTES

1. Rating applies to ambient temperatures up to 25°C. Above 25°C ambient derate linearly at 6.3 mW/°C for the Metal Can, 8.3 mW/°C for the Ceramic DIP and 6.3 mW/°C for the Silicone DIP.
2. Unless otherwise specified, T_A = 25°C, V_{IN} = V^+ = V_C = 12 V, V^- = 0, V_{OUT} = 5 V, I_L = 1 mA, R_{SC} = 0, C_1 = 100 pF, C_{REF} = 0 and divider impedance as seen by error amplifier ≤ 10 kΩ connected as shown in Fig. 1. Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.
3. L_1 is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009" air gap.
4. Figures in parentheses may be used if R_1/R_2 divider is placed on opposite side of error amp.
5. Replace R_1/R_2 in figures with divider shown in figure 13.
6. V^+ must be connected to a +3 V or greater supply.
7. For metal can applications where V_Z is required, an external 6.2 volt zener diode should be connected in series with V_{OUT}.

TABLE I
RESISTOR VALUES (kΩ) FOR STANDARD OUTPUT VOLTAGES

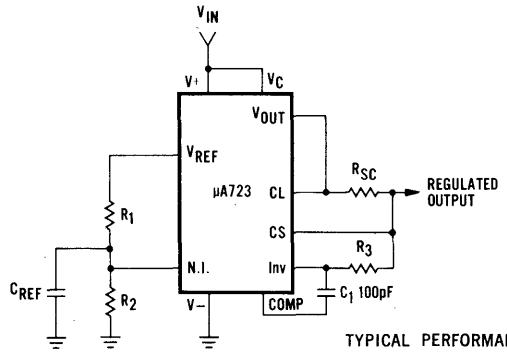
POSITIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (Note 5)			NEGATIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		5% OUTPUT ADJUSTABLE ±10%		
	(Note 4)	R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	.75	0.5	2.2	−6 (note 6)	3, (10)	3.57	2.43	1.2	0.5	.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 12, 9)	1.87	7.15	.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

TABLE II
FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts [Figures 1, 5, 6, 9, 12, (4)] $V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$	Outputs from +4 to +250 volts [Figure 7] $V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_2 - R_1}{R_1}]$; $R_3 = R_4$	Current Limiting $I_{LIMIT} = \frac{V_{SENSE}}{R_{sc}}$
Outputs from +7 to +37 volts [Figures 2, 4, (5, 6, 9, 12)] $V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$	Outputs from −6 to −250 volts [Figures 3, 8, 10] $V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}]$; $R_3 = R_4$	Foldback Current Limiting $I_{KNEE} = [\frac{V_{OUT} R_3}{R_{sc} R_4} + \frac{V_{SENSE}(R_3 + R_4)}{R_{sc} R_4}]$ $I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}]$

Figure 1

BASIC LOW VOLTAGE REGULATOR
(V_{out} = 2 to 7 Volts)



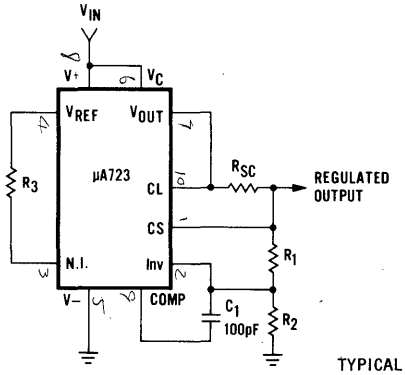
TYPICAL PERFORMANCE

Regulated Output Voltage	5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Note: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.

Figure 2

BASIC HIGH VOLTAGE REGULATOR
(V_{out} = 7 to 37 Volts)

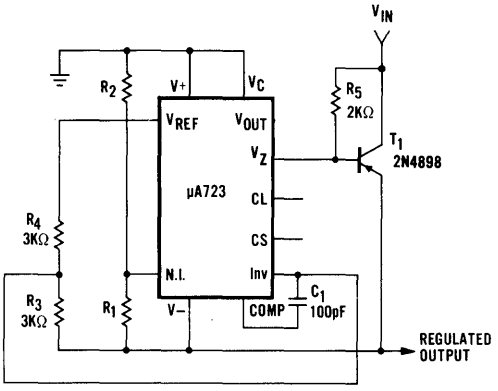


TYPICAL PERFORMANCE

Regulated Output Voltage	15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5 mV
Load Regulation (ΔI_L=50 mA)	4.5 mV

Note: $R_3 = \frac{R_1 R_2}{R_1 + R_2}$ for minimum temperature drift.
R_3 may be eliminated for minimum component count.

Figure 3
NEGATIVE VOLTAGE REGULATOR

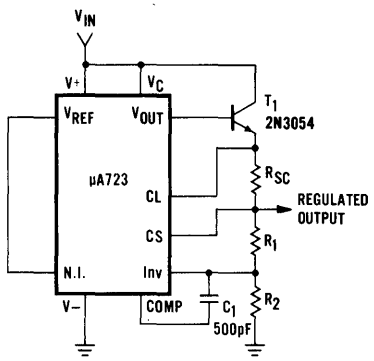


TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1 mV
Load Regulation ($\Delta I_L = 100$ mA)	2 mV

Note 7

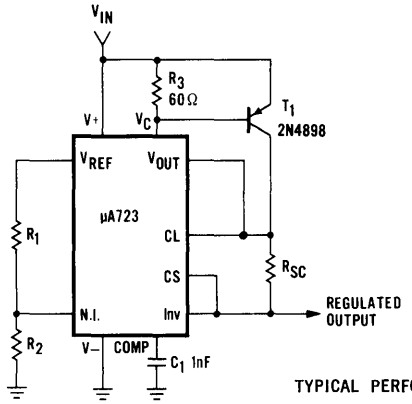
Figure 4
POSITIVE VOLTAGE REGULATOR (External NPN Pass Transistor)



TYPICAL PERFORMANCE

Regulated Output Voltage	+15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1.5 mV
Load Regulation ($\Delta I_L = 1$ A)	15 mV

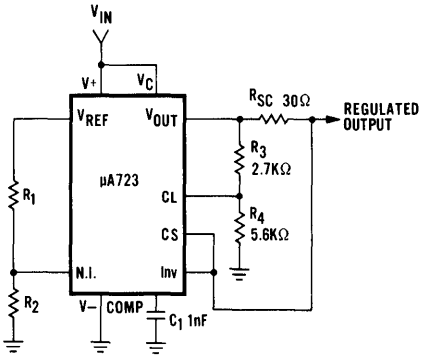
Figure 5
POSITIVE VOLTAGE REGULATOR (External PNP Pass Transistor)



TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 1$ A)	5 mV

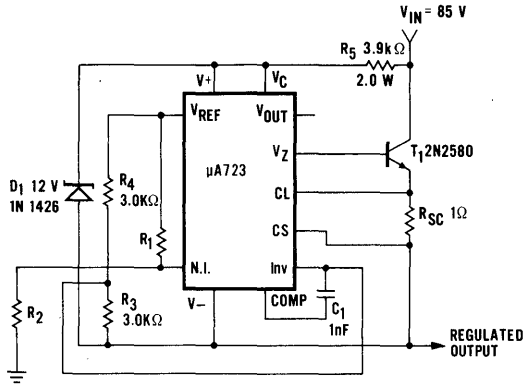
Figure 6
FOLDBACK CURRENT LIMITING



TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 10$ mA)	1 mV
Short Circuit Current	20 mA

Figure 7
POSITIVE FLOATING REGULATOR

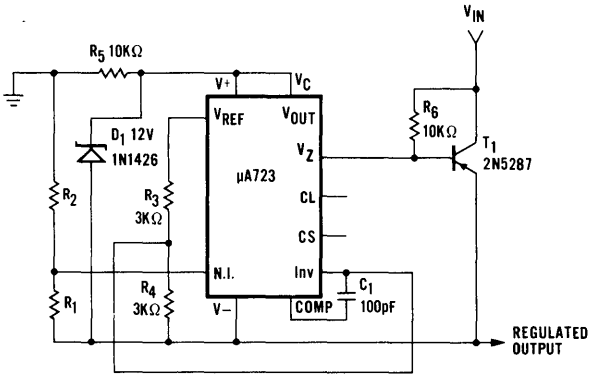


TYPICAL PERFORMANCE

Regulated Output Voltage	+50 V
Line Regulation ($\Delta V_{IN} = 20$ V)	15 mV
Load Regulation ($\Delta I_L = 50$ mA)	20 mV

Note 7

Figure 8
NEGATIVE FLOATING REGULATOR

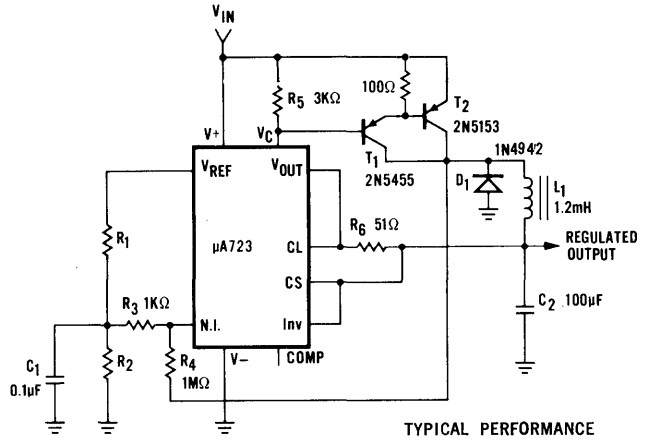


TYPICAL PERFORMANCE

Regulated Output Voltage	−100 V
Line Regulation ($\Delta V_{IN} = 20$ V)	30 mV
Load Regulation (ΔI_L=100 mA)	20 mV

Note 7

Figure 9
POSITIVE SWITCHING REGULATOR

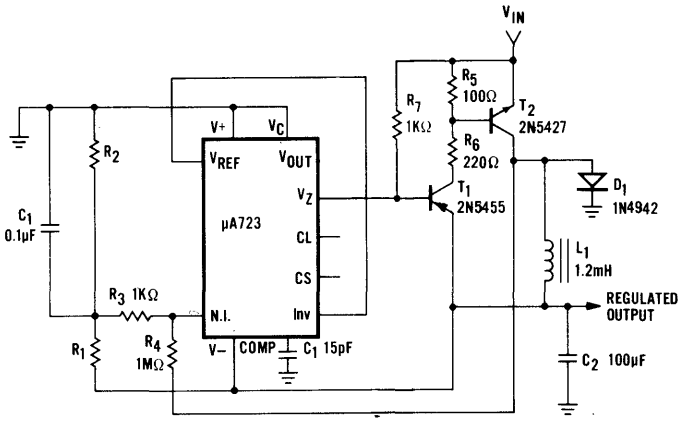


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 30$ V)	10 mV
Load Regulation ($\Delta I_L = 2$ A)	80 mV

Note 3

Figure 10
NEGATIVE SWITCHING REGULATOR

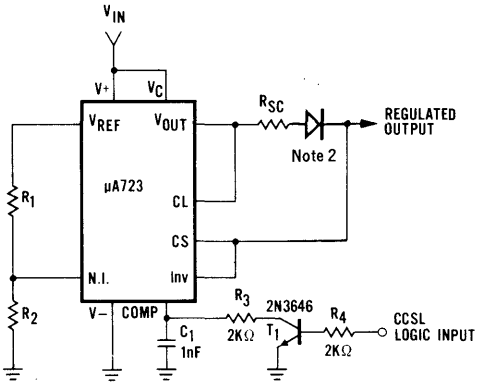


TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 20$ V)	8 mV
Load Regulation ($\Delta I_L = 2$ A)	6 mV

Notes 3, 7

Figure 11
REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING



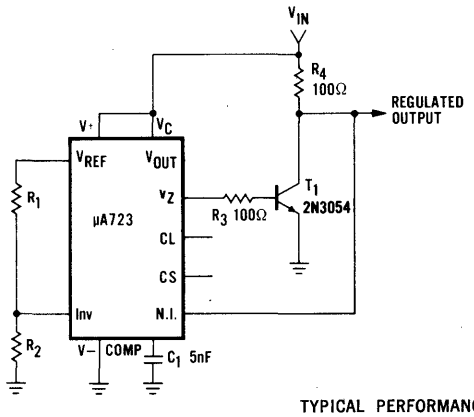
Note 1: Current limit transistor may be used for shutdown if current limiting is not required.

2: Add if Vout > 10 V

TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Figure 12
SHUNT REGULATOR

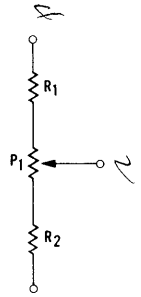


TYPICAL PERFORMANCE

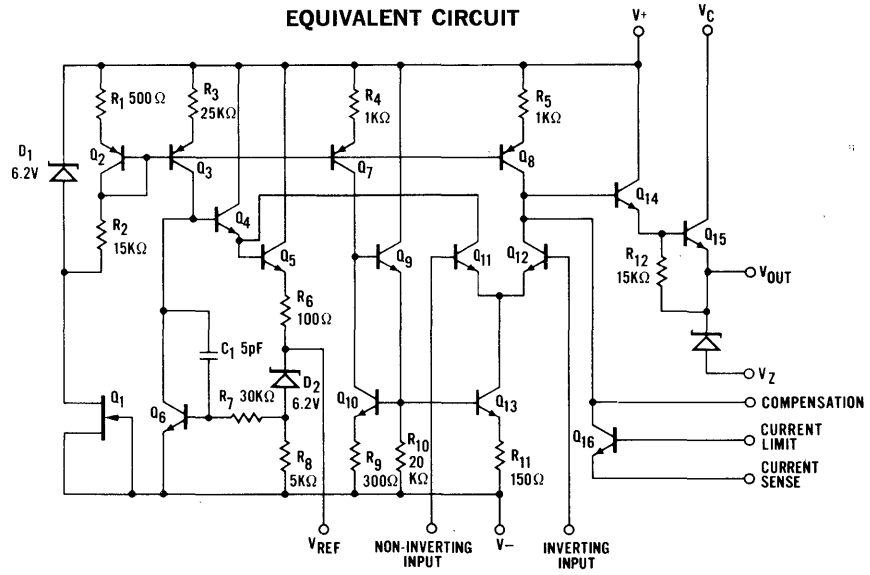
Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 10$ V)	0.5 mV
Load Regulation (ΔI_L=100 mA)	1.5 mV

Note 7

Figure 13
OUTPUT VOLTAGE ADJUST



EQUIVALENT CIRCUIT



μA725

INSTRUMENTATION OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

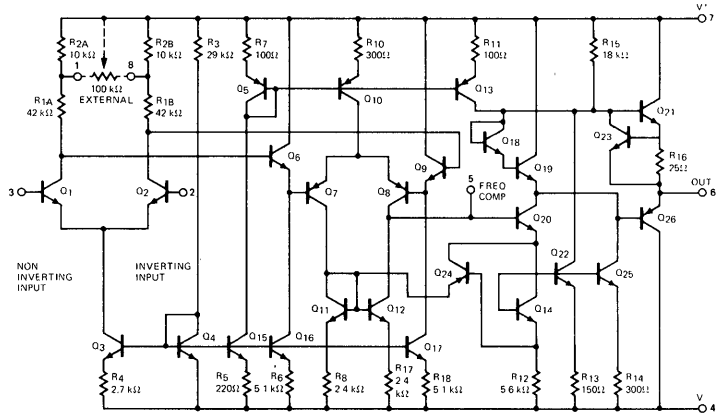
GENERAL DESCRIPTION — The μA725 is an instrumentation operational amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It is intended for precise, low level signal amplification applications where low noise, low drift and accurate closed loop gain are required. The offset null capability, low power consumption, very high voltage gain as well as wide power supply voltage range provide superior performance for a wide range of instrumentation applications. The μA725 is pin compatible with the popular μA741 operational amplifier.

- **LOW INPUT NOISE CURRENT . . . . . 0.15 pA $\sqrt{Hz}$**
- **HIGH OPEN LOOP GAIN 3,000,000**
- **LOW INPUT OFFSET CURRENT . . . . . 2 nA**
- **LOW INPUT VOLTAGE DRIFT . . . . . 0.6 μV/°C**
- **HIGH COMMON MODE REJECTION . . . 120 dB**
- **HIGH INPUT VOLTAGE RANGE . . . . . ±14 V**
- **WIDE POWER SUPPLY RANGE . . . . . ±3 V TO ±22 V**
- **OFFSET NULL CAPABILITY**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Ceramic DIP	670 mW
Differential Input Voltage (Note 2)	±22 V
Input Voltage (Note 3)	±22 V
Voltage Between Offset Null and V^+	±0.5 V
Storage Temperature Range	
Metal Can, Ceramic DIP	−65°C to +150°C
Operating Temperature Range	
Military (312 grade)	−55°C to +125°C
Instrument (333 grade)	−20°C to +85°C
Commercial (393 grade)	0°C to +70°C
Lead Temperature	
Metal Can, Ceramic DIP (Soldering, 60 Seconds)	300°C

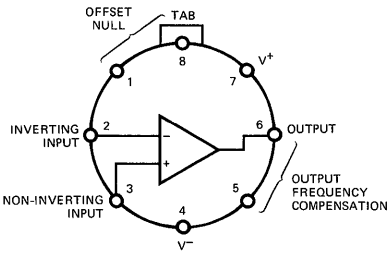
EQUIVALENT CIRCUIT



Pin numbers are shown for Metal Can only.

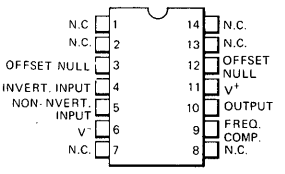
CONNECTION DIAGRAM

8 LEAD METAL CAN
(TOP VIEW)



ORDER PART NOS.:
U5T7725312
U5T7725333
U5T7725393

14 LEAD DIP
(TOP VIEW)



FOR CERAMIC DIP
ORDER PART NOS.:
U6A7725312
U6A7725333
U6A7725393

Notes on following pages.

*Planar is a patented Fairchild process.

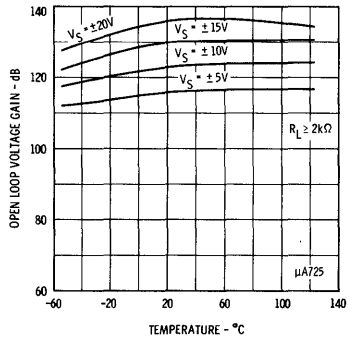
312 GRADE

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise specified)

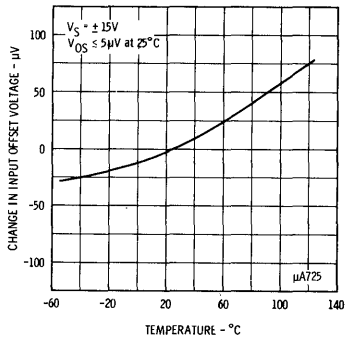
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage (Without external trim)	$R_S \leq 10\ k\Omega$		0.5	1.0	mV
Input Offset Current			2.0	20	nA
Input Bias Current			42	100	nA
Input Noise Voltage	f_o = 10 Hz		15		nV/$\sqrt{Hz}$
	f_o = 100 Hz		9.0		nV/$\sqrt{Hz}$
	f_o = 1 kHz		8.0		nV/$\sqrt{Hz}$
Input Noise Current	f_o = 10 Hz		1.0		pA/$\sqrt{Hz}$
	f_o = 100 Hz		0.3		pA/$\sqrt{Hz}$
	f_o = 1 kHz		0.15		pA/$\sqrt{Hz}$
Input Resistance			1.5		MΩ
Input Voltage Range		±13.5	±14		V
Large Signal Voltage Gain	$R_L \geq$ 2 kΩ V_o = ±10 V	1,000,000	3,000,000		V/V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	110	120		dB
Power Supply Rejection Ratio	$R_S \leq 10\ k\Omega$		2.0	10	μV/V
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±13.5		V
	$R_L \geq$ 2 kΩ	±10	±13.5		V
Output Resistance			150		Ω
Power Consumption			80	105	mW
The following specifications apply for $-55°C \leq T_A \leq +125°C$ unless otherwise specified:					
Input Offset Voltage (Without external trim)	$R_S \leq 10\ k\Omega$			1.5	mV
Average Input Offset Voltage Drift (Without external trim)	R_S = 50Ω		2.0	5.0	μV/°C
Average Input Offset Voltage Drift (With external trim)	R_S = 50Ω		0.6		μV/°C
Input Offset Current	T_A = +125°C		1.2	20	nA
	T_A = −55°C		7.5	40	nA
Average Input Offset Current Drift			35	150	pA/°C
Input Bias Current	T_A = +125°C		20	100	nA
	T_A = −55°C		80	200	nA
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, T_A = +125°C	1,000,000			V/V
	$R_L \geq 2\ k\Omega$, T_A = −55°C	250,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	100			dB
	$R_S \leq 10\ k\Omega$			20	μV/V
	$R_L \geq$ 2 kΩ	±10			V

TYPICAL PERFORMANCE CURVES
312 GRADE

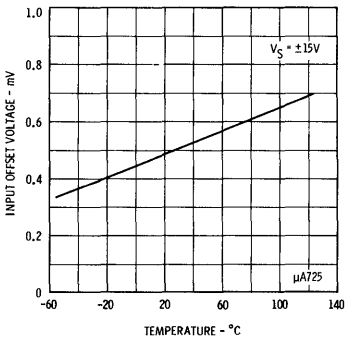
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE FOR VARIOUS SUPPLY VOLTAGES



NULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



UNNULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



333 GRADE

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise specified)

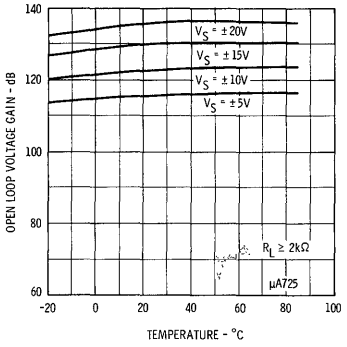
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ		0.5	1.5	mV
Input Offset Current			2.0	20	nA
Input Bias Current			50	100	nA
Input Noise Voltage	f_o = 10 Hz		15		nV/$\sqrt{Hz}$
	f_o = 100 Hz		12		nV/$\sqrt{Hz}$
	f_o = 1 kHz		8.0		nV/$\sqrt{Hz}$
Input Noise Current	f_o = 10 Hz		1.0		pA/$\sqrt{Hz}$
	f_o = 100 Hz		0.8		pA/$\sqrt{Hz}$
	f_o = 1 kHz		0.6		pA/$\sqrt{Hz}$
Input Resistance			1.5		MΩ
Input Voltage Range		±13.5	±14		V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	500,000	3,000,000		V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	100	120		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		2.0	10	μV/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±13.5		V
	$R_L \geq 2$ kΩ	±10	±13.5		V
Output Resistance			150		Ω
Power Consumption			80	120	mW
The following specifications apply for −20°C ≤ T_A ≤ +85°C unless otherwise specified:					
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ			2.5	mV
Average Input Offset Voltage Drift (Without external trim)	R_S = 50Ω		2.0	10	μV/°C
Average Input Offset Voltage Drift (With external trim)	R_S = 50Ω		0.6		μV/°C
Input Offset Current	T_A = +85°C		2.0	20	nA
	T_A = −20°C		5.0	40	nA
Average Input Offset Current Drift				300	pA/°C
Input Bias Current	T_A = +85°C			100	nA
	T_A = −20°C			200	nA
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, T_A = +85°C	500,000			V/V
	$R_L \geq 2$ kΩ, T_A = −20°C	250,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	100			dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ			20	μV/V
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V

NOTES

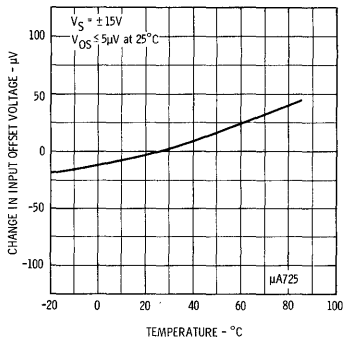
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for Metal Can and 8.3 mW/°C for Ceramic DIP package.
2. Rating applies for 5 ms pulses with 10% duty cycle, derate to ±5 V for continuous operation.
3. For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.

TYPICAL PERFORMANCE CURVES
333 GRADE

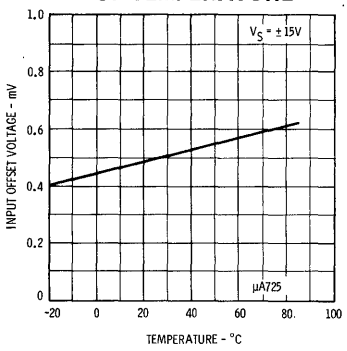
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE FOR VARIOUS SUPPLY VOLTAGES



NULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



UNNULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE



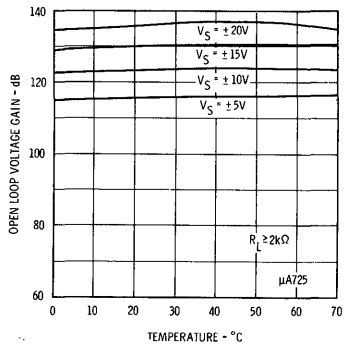
393 GRADE

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise specified)

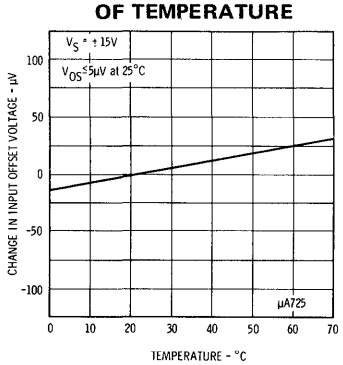
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ		0.5	2.5	mV
Input Offset Current			2.0	35	nA
Input Bias Current			42	125	nA
Input Noise Voltage	f_o = 10 Hz		15		nV/$\sqrt{Hz}$
	f_o = 100 Hz		9.0		nV/$\sqrt{Hz}$
	f_o = 1 kHz		8.0		nV/$\sqrt{Hz}$
Input Noise Current	f_o = 10 Hz		1.0		pA/$\sqrt{Hz}$
	f_o = 100 Hz		0.3		pA/$\sqrt{Hz}$
	f_o = 1 kHz		0.15		pA/$\sqrt{Hz}$
Input Resistance			1.5		MΩ
Input Voltage Range		±13.5	±14		V
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	250,000	3,000,000		V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	94	120		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		2.0	35	μV/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±13.5		V
	$R_L \geq 2$ kΩ	±10	±13.5		V
Output Resistance			150		Ω
Power Consumption			80	150	mW
The following specifications apply for 0°C ≤ T_A ≤ +70°C unless otherwise specified:					
Input Offset Voltage (Without external trim)	$R_S \leq 10$ kΩ			3.5	mV
Average Input Offset Voltage Drift (Without external trim)	R_S = 50Ω		2.0		μV/°C
Average Input Offset Voltage Drift (With external trim)	R_S = 50Ω		0.6		μV/°C
Input Offset Current	T_A = +70°C		1.2	35	nA
	T_A = 0°C		4.0	50	nA
Average Input Offset Current Drift			10		pA/°C
Input Bias Current	T_A = +70°C			125	nA
	T_A = 0°C			250	nA
Large Signal Voltage	$R_L \geq 2$ kΩ, T_A = +70°	125,000			V/V
	$R_L \geq 2$ kΩ, T_A = 0°C	125,000			V/V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ		115		dB
Power Supply Rejection Ratio	$R_S \leq 10$ kΩ		20		μV/V
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V

TYPICAL PERFORMANCE CURVES 393 GRADE

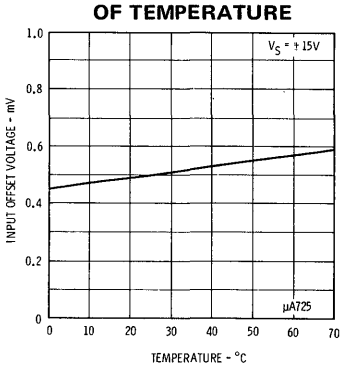
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE FOR VARIOUS SUPPLY VOLTAGES



NULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE

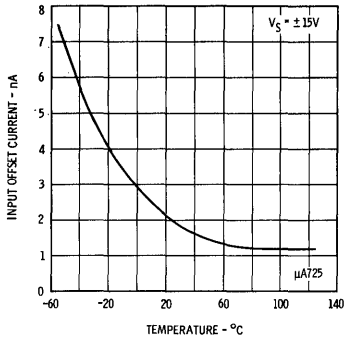


UNNULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF TEMPERATURE

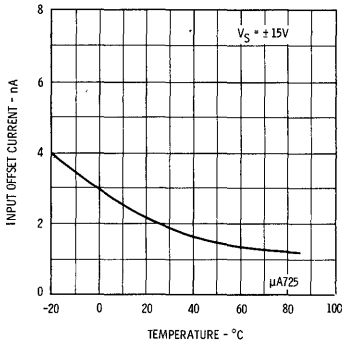


TYPICAL PERFORMANCE CURVES FOR ALL GRADES (Unless Otherwise Specified)

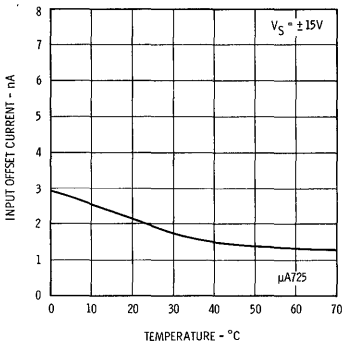
INPUT OFFSET CURRENT AS A FUNCTION OF TEMPERATURE 312 GRADE



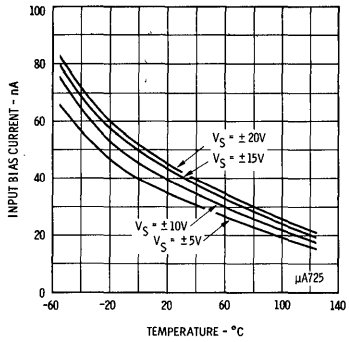
INPUT OFFSET CURRENT AS A FUNCTION OF TEMPERATURE 333 GRADE



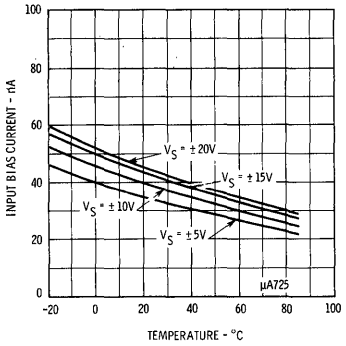
INPUT OFFSET CURRENT AS A FUNCTION OF TEMPERATURE 393 GRADE



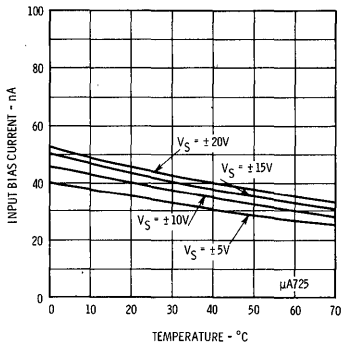
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE 312 GRADE



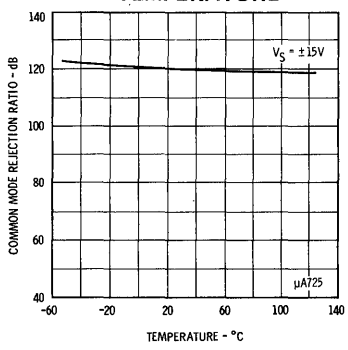
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE 333 GRADE



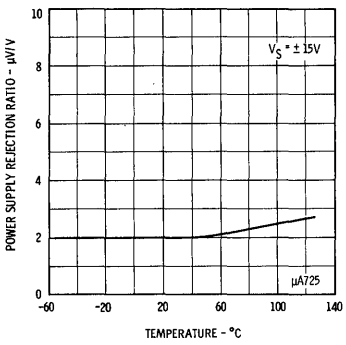
INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE 393 GRADE



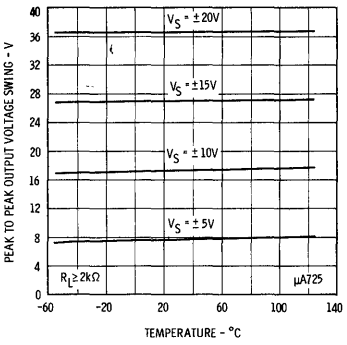
COMMON MODE REJECTION RATIO AS A FUNCTION OF TEMPERATURE



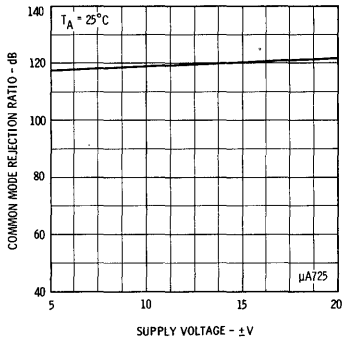
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF TEMPERATURE



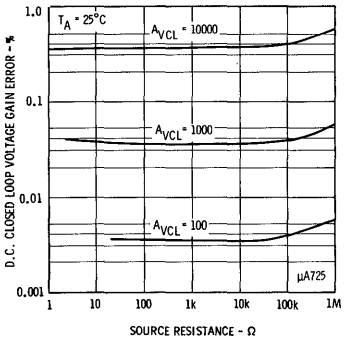
OUTPUT VOLTAGE SWING AS A FUNCTION OF TEMPERATURE



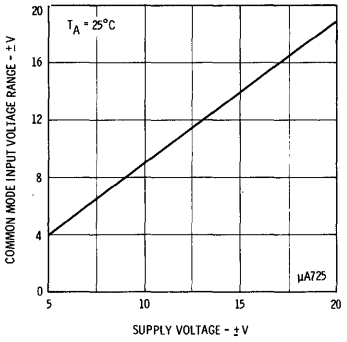
COMMON MODE REJECTION RATIO AS A FUNCTION OF SUPPLY VOLTAGE



D.C. CLOSED LOOP VOLTAGE GAIN ERROR AS A FUNCTION OF SOURCE RESISTANCE

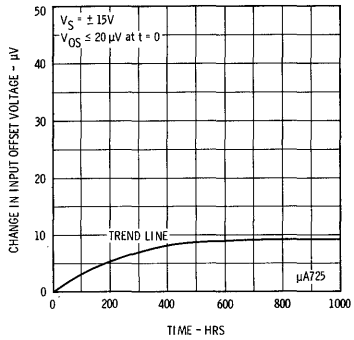


COMMON MODE INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

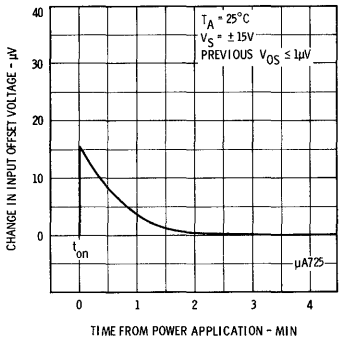


TYPICAL PERFORMANCE CURVES FOR ALL GRADES (Unless Otherwise Specified)

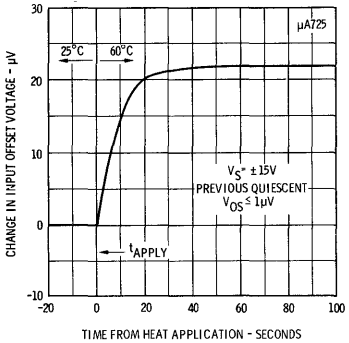
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



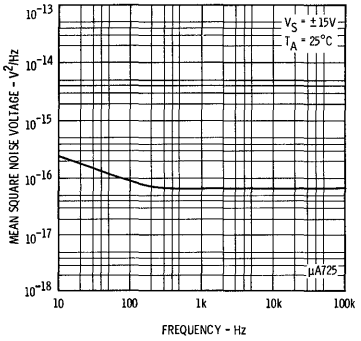
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



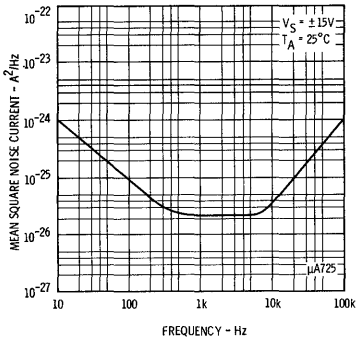
CHANGE IN INPUT OFFSET VOLTAGE DUE TO THERMAL SHOCK AS A FUNCTION OF TIME



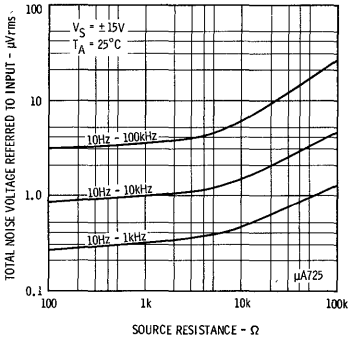
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



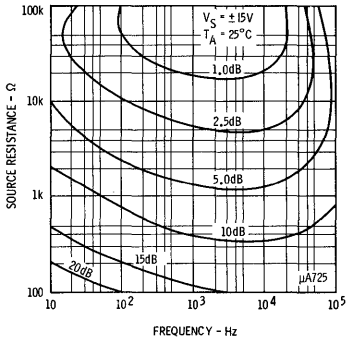
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



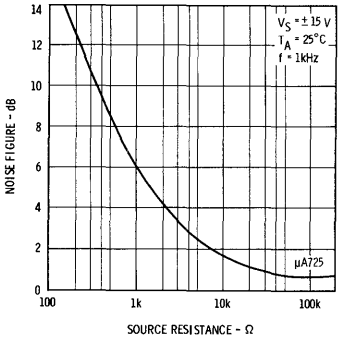
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



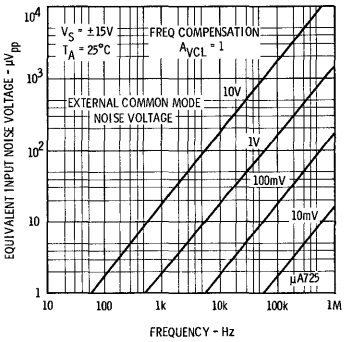
NARROW BAND SPOT NOISE FIGURE CONTOURS



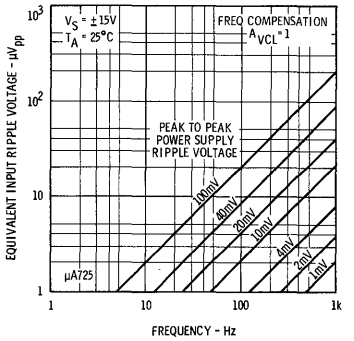
NOISE FIGURE AS A FUNCTION OF SOURCE RESISTANCE



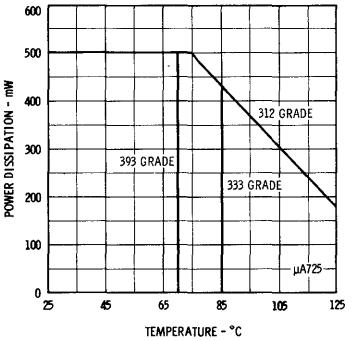
EQUIVALENT INPUT NOISE VOLTAGE DUE TO EXTERNAL COMMON MODE NOISE AS A FUNCTION OF FREQUENCY



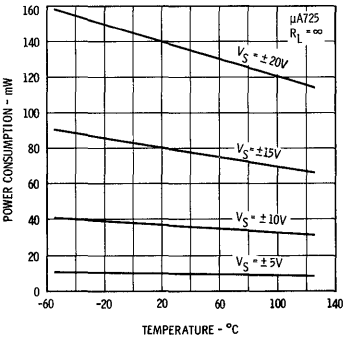
EQUIVALENT INPUT RIPPLE VOLTAGE DUE TO POWER SUPPLY RIPPLE AS A FUNCTION OF FREQUENCY



ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

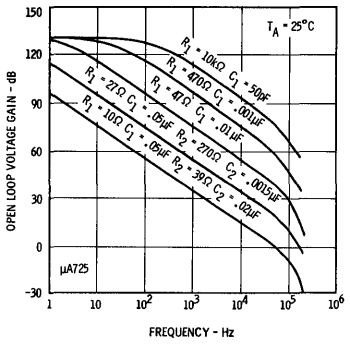


POWER CONSUMPTION AS A FUNCTION OF TEMPERATURE

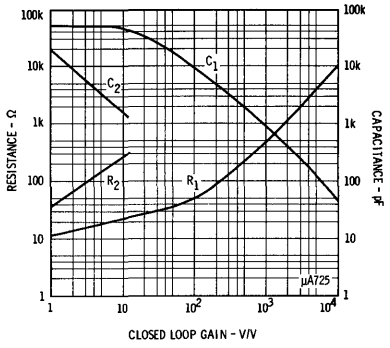


TYPICAL PERFORMANCE CURVES FOR ALL GRADES

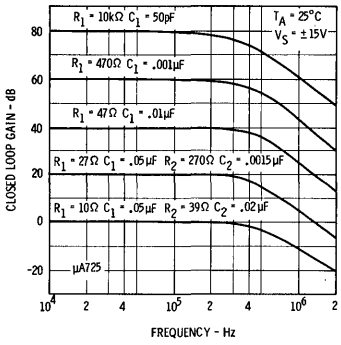
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY USING RECOMMENDED COMPENSATION NETWORKS



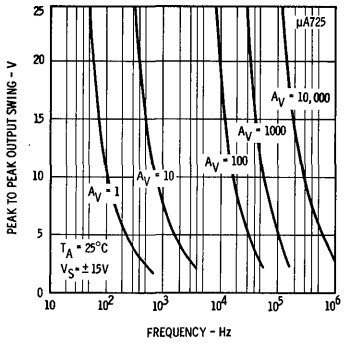
VALUES FOR SUGGESTED COMPENSATION NETWORKS FOR VARIOUS CLOSED LOOP VOLTAGE GAINS



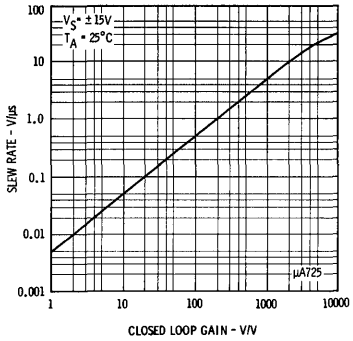
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS USING RECOMMENDED COMPENSATION NETWORKS



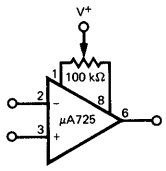
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR RECOMMENDED COMPENSATION NETWORKS



SLEW RATE AS A FUNCTION OF CLOSED-LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS



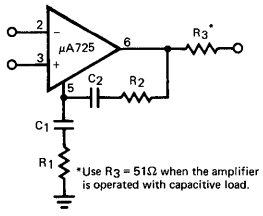
VOLTAGE OFFSET NULL CIRCUIT



COMPENSATION COMPONENT VALUES

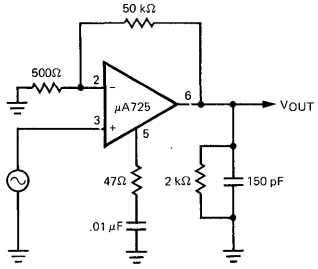
A_{VCL}	R_1 (Ω)	C_1 (μF)	R_2 (Ω)	C_2 (μF)
10,000	10 k	50 pF	—	—
1,000	470	.001	—	—
100	47	.01	—	—
10	27	.05	270	.0015
1	10	.05	39	.02

FREQUENCY COMPENSATION CIRCUIT



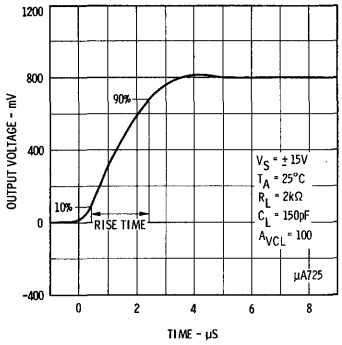
*Use R_3 = 51Ω when the amplifier is operated with capacitive load.

TRANSIENT RESPONSE TEST CIRCUIT



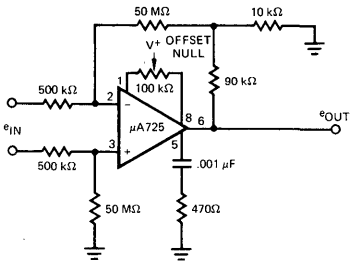
Pin numbers are shown for Metal Can only.

TRANSIENT RESPONSE



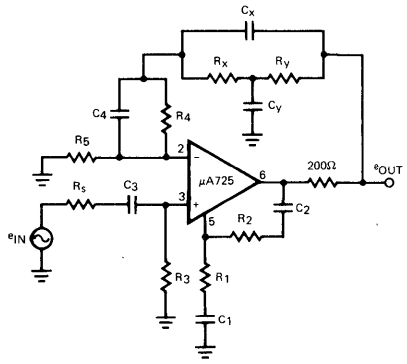
TYPICAL APPLICATIONS

PRECISION AMPLIFIER – A_{VCL} = 1000

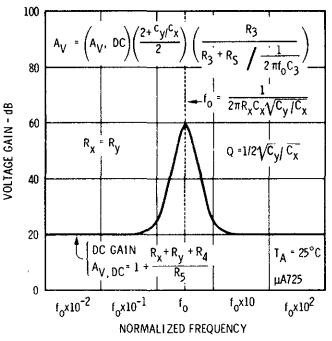


CHARACTERISTICS:
- A_{VCL} = 1000 = 60 dB
- DC Gain Error = 0.05%
- Bandwidth = 1 kHz for –0.05% error
- Diff. Input Res. = 1 MΩ
- Typical amplifying capability
  e_{IN} = 10 μV on V_{CMI} = 1.0 V
- Caution: Minimize Stray Capacitance

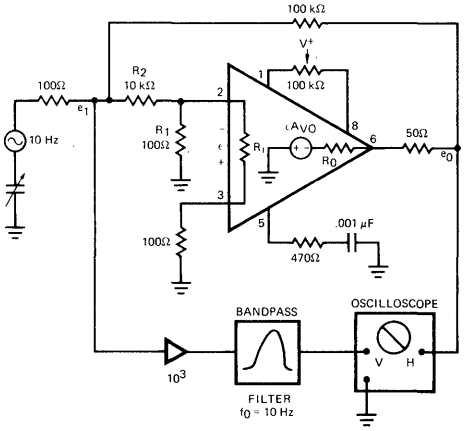
ACTIVE FILTER – BANDPASS WITH 60 dB GAIN



ACTIVE FILTER FREQUENCY RESPONSE

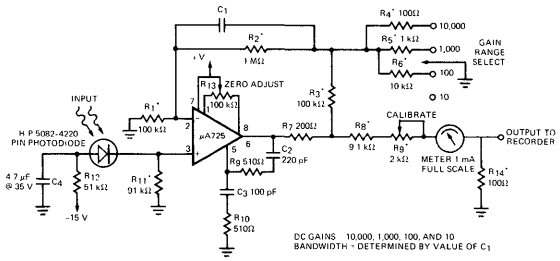


OPEN LOOP VOLTAGE GAIN TEST CIRCUIT



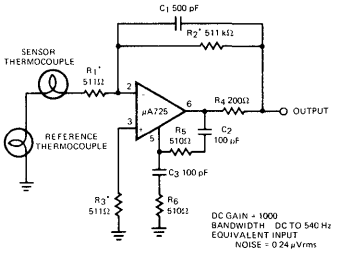
$$A_{VO} \simeq \frac{e_0}{e_1}\left(\frac{R_2 R_i + R_1 R_i + R_1 R_2}{R_1 R_i}\right) = \frac{e_0}{e_1}\ 101$$

PIN PHOTODIODE AMPLIFIER



NOTE: * Indicates ±1% Metal film resistors recommended for temperature stability.

THERMOCOUPLE AMPLIFIER



NOTE: * Indicates ±1% metal film resistors recommended for temperature stability.

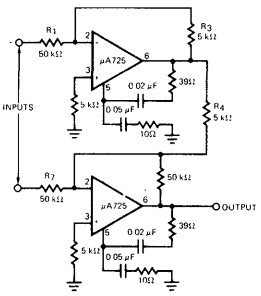
±100 V COMMON MODE RANGE INSTRUMENTATION AMPLIFIER

$$\frac{R_1}{R_7} = \frac{R_3}{R_4} \text{ for best CMRR}$$

$R_3 = R_4$

$R_1 = R_6 = 10R_3$

$$\text{Gain} = \frac{R_7}{R_6}$$



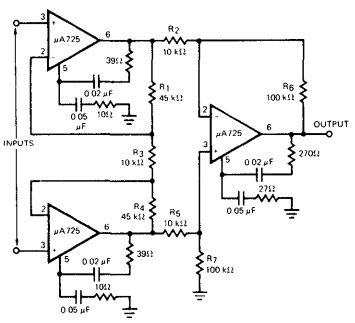
INSTRUMENTATION AMPLIFIER WITH HIGH COMMON MODE REJECTION

$$\frac{R_2}{R_5} = \frac{R_6}{R_7} \text{ for best CMR}$$

$R_1 = R_4$

$R_2 = R_5$

$$\text{Gain} = \frac{R_6}{R_2}\left(1 + \frac{2R_1}{R_3}\right)$$



μA726

TEMPERATURE-CONTROLLED DIFFERENTIAL PAIR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA726 is a monolithic transistor pair in high thermal-resistance package, held at a constant temperature by active temperature regulator circuitry. The transistor pair displays the excellent matching, close thermal coupling, and fast thermal response inherent in monolithic construction. The high gain and low standby dissipation of the regulator circuit permits tight temperature control over a wide range of ambient temperatures. It is intended for use as an input stage in very-low-drift DC amplifiers, replacing complex chopper-stabilized amplifiers; it is also useful as the nonlinear element in logarithmic amplifiers and multipliers where the highly predictable exponential relation between emitter-base voltage and collector current is employed. The device is constructed on a single silicon chip using the Fairchild Planar* process.

ABSOLUTE MAXIMUM RATINGS

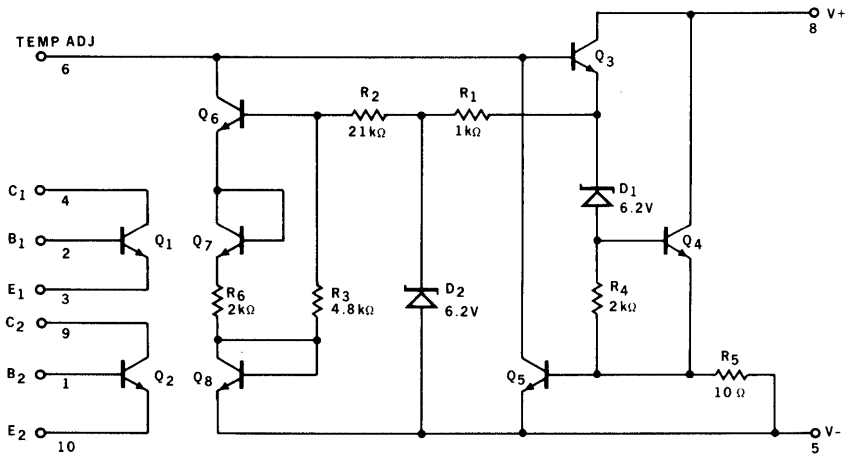
Operating Temperature Range	
Military (312 Grade)	−55° C to +125° C
Commercial (323 Grade)	0° C to +85° C
Storage Temperature Range	−65° C to +150° C
Lead Temperature (Soldering, 60 seconds)	300° C
Supply Voltage	±18 V
Internal Power Dissipation	500 mW

MAXIMUM RATINGS FOR EACH TRANSISTOR

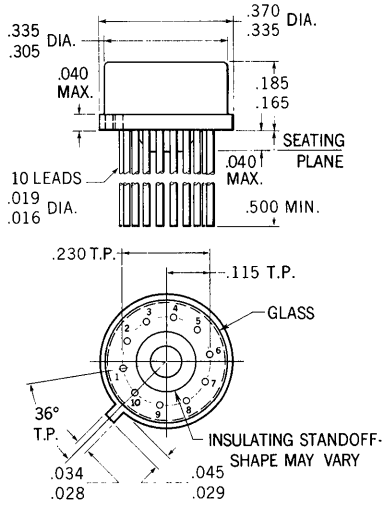
Maximum collector-to-substrate voltage	40 V
BV_{CBO}	40 V
LV_{CEO} (Note 1)	30 V
BV_{EBO}	5 V
Collector Current	5 mA

Note 1: Measured at 1 mA collector current.

SCHEMATIC DIAGRAM



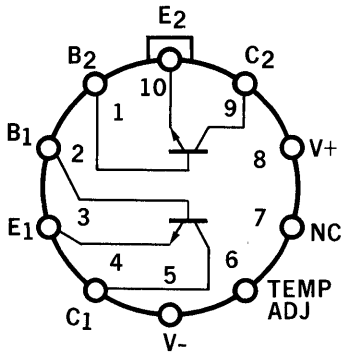
PHYSICAL DIMENSIONS



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams

ORDER PART NOS. U5U7726312
U5U7726323

CONNECTION DIAGRAM
(TOP VIEW)



*Planar is a patented Fairchild process

312 GRADE

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq +125°C$, $V_S = \pm 15$ V, $R_{adj} = 62$ kΩ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	10 μA ≤ I_C ≤ 100 μA V_{CE} = 5 V, R_S ≤ 50Ω		1.0	2.5	mV
Input Offset Current	I_C = 10 μA, V_{CE} = 5 V		10	50	nA
Input Offset Current	I_C = 100 μA, V_{CE} = 5 V		50	200	nA
Average Input Bias Current	I_C = 10 μA, V_{CE} = 5 V		50	150	nA
Average Input Bias Current	I_C = 100 μA, V_{CE} = 5 V		250	500	nA
Offset Voltage Change	I_C = 10 μA, 5 V ≤ V_{CE} ≤ 25 V, R_S ≤ 100 kΩ		0.3	6.0	mV
Offset Voltage Change	I_C = 100 μA, 5 V ≤ V_{CE} ≤ 25 V, R_S ≤ 10 kΩ		0.3	6.0	mV
Input Offset Voltage Drift	10 μA ≤ I_C ≤ 100 μA, V_{CE} = 5 V, R_S ≤ 50Ω, +25°C ≤ T_A ≤ +125°C		0.2	1.0	μV/°C
Input Offset Voltage Drift	10μA ≤ I_C ≤ 100 μA, V_{CE} = 5 V, R_S ≤ 50Ω, −55°C ≤ T_A ≤ +25°C		0.2	1.0	μV/°C
Input Offset Current Drift	I_C = 10 μA, V_{CE} = 5 V		10		pA/°C
Input Offset Current Drift	I_C = 100 μA, V_{CE} = 5 V		30		pA/°C
Supply Voltage Rejection Ratio	10μA ≤ I_C ≤100 μA, R_S ≤ 50Ω,		25		μV/V
Low-Frequency Noise	I_C = 10 μA, V_{CE} = 5 V, R_S ≤ 50Ω BW = .001 Hz to 0.1 Hz		4.0		μV pp
Broadband Noise	I_C = 10 μA, V_{CE} = 5 V, R_S ≤ 50Ω BW = 0.1 Hz to 10 kHz		10		μV pp
Long-term Drift	10 μA ≤ I_C ≤ 100 μA, V_{CE} = 5 V, R_S ≤ 50Ω, T_A=25°C		5.0		μV/week
High Frequency Current Gain	f = 20 MHz, I_C = 100 μA, V_{CE} = 5 V	1.5	3.5		
Output Capacitance	I_E = 0, V_{CB} = 5 V		1.0		pF
Emitter Transition Capacitance	I_E = 100 μA		1.0		pF
Collector Saturation Voltage	I_B = 100 μA, I_C = 1 mA		0.5	1.0	V

323 GRADE

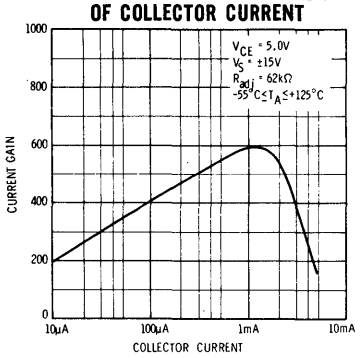
ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +85°C$, $V_S = \pm 15$V, $R_{adj} = 75$ kΩ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	10 μA ≤ I_C ≤ 100 μA V_{CE} = 5V, R_S ≤ 50Ω		1.0	3.0	mV
Input Offset Current	I_C = 10 μA, V_{CE} = 5V		10	100	nA
Input Offset Current	I_C = 100 μA, V_{CE} = 5V		50	400	nA
Average Input Bias Current	I_C = 10 μA, V_{CE} = 5V		50	300	nA
Average Input Bias Current	I_C = 100 μA, V_{CE} = 5V		250	1000	nA
Offset Voltage Change	I_C = 10 μA, 5V ≤ V_{CE} ≤ 25V, R_S ≤ 100 kΩ		0.3	6.0	mV
Offset Voltage Change	I_C = 100 μA, 5V ≤ V_{CE} ≤ 25V, R_S ≤ 10 kΩ		0.3	6.0	mV
Input Offset Voltage Drift	I_C = 100 μA, V_{CE} = 5V, R_S ≤ 50Ω		0.2	2.0	μV/°C
Input Offset Current Drift	I_C = 10 μA, V_{CE} = 5V		10		pA/°C
Input Offset Current Drift	I_C = 100 μA, V_{CE} = 5V		30		pA/°C
Supply Voltage Rejection Ratio	I_C = 100 μA, R_S = 50Ω		25		μV/V
Low-Frequency Noise	I_C = 10 μA, V_{CE} = 5V, R_S ≤ 50Ω, BW = 0.001 Hz to 0.1 Hz		4.0		μV pp
Broadband Noise	I_C = 10 μA, V_{CE} = 5V, R_S ≤ 50Ω, BW = 0.1 Hz to 10 kHz		10		μV pp
Long-Term Drift	I_C = 100 μA, V_{CE} = 5V, R_S ≤ 50Ω, T_A = 25°C		5.0		μV/week
High-Frequency Current Gain	f = 20 MHz, I_C = 100 μA, V_{CE} = 5V	1.5	3.5		
Output Capacitance	I_E = 0, V_{CB} = 5V		1.0		pF
Emitter Transition Capacitance	I_E = 100 μA		1.0		pF
Collector Saturation Voltage	I_B = 100 μA, I_C = 1 mA		0.5	1.0	V

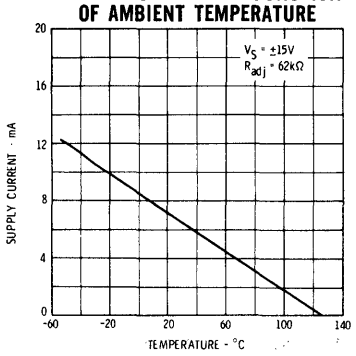
TYPICAL PERFORMANCE CURVES

312 GRADE

CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT

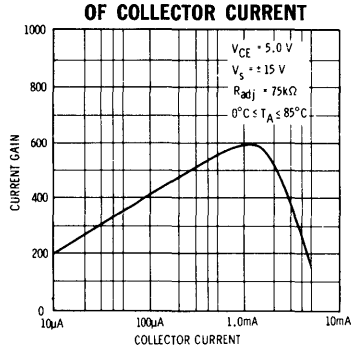


SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

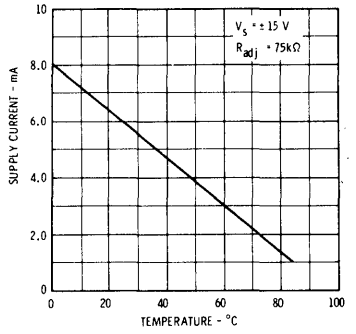


323 GRADE

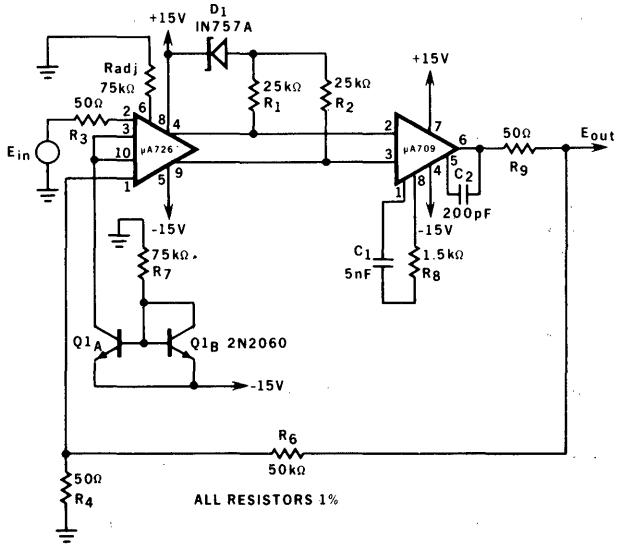
CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL X1000 CIRCUIT



μA727

PREAMPLIFIER TEMPERATURE-CONTROLLED DIFFERENTIAL

FAIRCHILD LINEAR INTEGRATED CIRCUITS

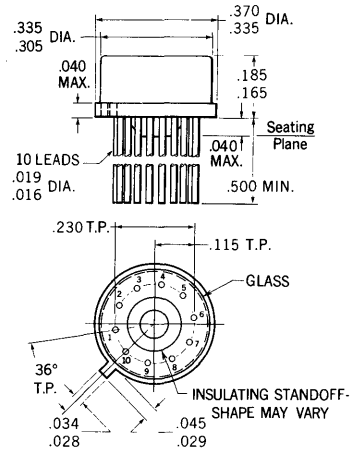
GENERAL DESCRIPTION — The μA727 is a monolithic, fixed gain, differential-input differential-output amplifier, constructed with the Fairchild Planar* epitaxial process, mounted in a high thermal-resistance package, and held at constant temperature by active regulator circuitry. The high gain and low standby dissipation of the regulator circuit give tight temperature control over a wide ambient temperature range. The device is intended for use as a self-contained input stage in very low-drift DC amplifiers, replacing complex chopper-stabilized amplifiers in such applications as thermo-couple bridges, strain gage transducers, and A to D converters.

- **VERY LOW OFFSET DRIFTS**
- **HIGH INPUT IMPEDANCE**
- **WIDE COMMON MODE RANGE**

ABSOLUTE MAXIMUM RATINGS

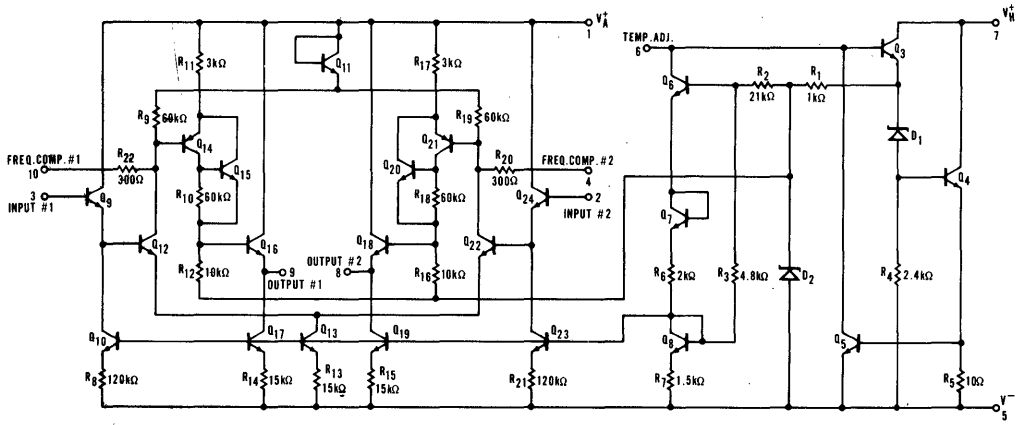
Operating Temperature Range	
Military (312 Grade)	−55°C to +125°C
Commercial (333 Grade)	−20°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 second time limit)	300°C
Internal Power Dissipation	500 mW
Supply Voltage (Amplifier and Heater)	±18 V
Differential Input Voltage	±10 V
Common Mode Input Voltage	±15 V

PHYSICAL DIMENSIONS
(In accordance with JEDEC TO-100)

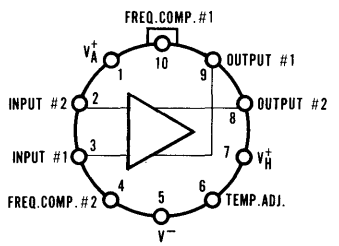


NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams

ORDER PART NOS. U5U7727312
U5U7727333



CONNECTION DIAGRAM
(Top View)



312 GRADE

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq +125°C$, $V_H^+ = V_A^+ = +15\ V$, $V^- = -15\ V$, $R_{ADJ} = 330\ k\Omega$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\ \Omega$		2.0	10	mV
Input Offset Current			2.5	15	nA
Input Bias Current			12	40	nA
Input Offset Voltage Drift	$R_S \leq 50\ \Omega$, $+25°C \leq T_A \leq +125°C$		0.6	1.5	μV/°C
	$R_S \leq 50\ \Omega$, $-55°C \leq T_A \leq +25°C$		0.6	1.5	μV/°C
Input Offset Current Drift	$+25°C \leq T_A \leq +125°C$		2.0		pA/°C
	$-55°C \leq T_A \leq +25°C$		2.0		pA/°C
Input Bias Current Drift	$-55°C \leq T_A \leq +125°C$		15		pA/°C
Differential Input Resistance			300		MΩ
Common Mode Input Resistance			1000		MΩ
Input Voltage Range		±12	±13		V
Supply Voltage Rejection Ratio	$R_S \leq 100\ k\Omega$		80		μV/V
Common Mode Rejection Ratio	$R_S \leq 100\ k\Omega$	80	100		dB
Output Resistance			1.0	4.0	kΩ
Output Common Mode Voltage		−6.0	−5.0	−4.0	V
Differential Output Voltage Swing		±5.0	±7.0	±10	V
Output Sink Current		10	30	80	μA
Differential Load Rejection			5.0	10	μV/μA
Differential Voltage Gain		60	100	250	
Low Frequency Noise	BW = 10 Hz to 500 Hz, $R_S \leq 50\ \Omega$		3.0		μVrms
Long Term Drift	$R_S \leq 50\ \Omega$		5.0		μV/week
Amplifier Supply Current	$T_A = +25°C$		1.0	2.0	mA
Heater Supply Current	$T_A = +25°C$		10	15	mA

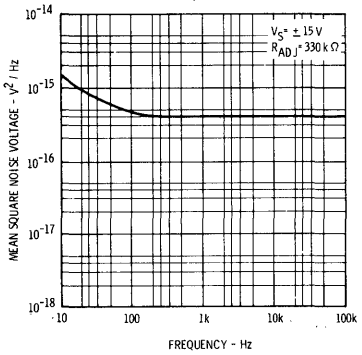
333 GRADE

ELECTRICAL CHARACTERISTICS ($-20°C \leq T_A \leq +85°C$, $V_H^+ = V_A^+ = +15\ V$, $V^- = -15\ V$, $R_{ADJ} = 1M\Omega$, unless otherwise specified)

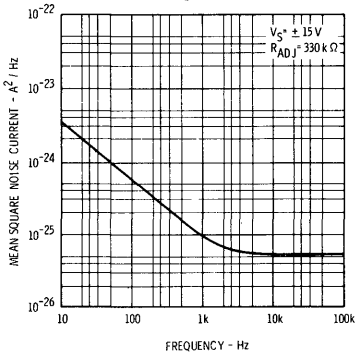
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\ \Omega$		2.0	10	mV
Input Offset Current			2.5	25	nA
Input Bias Current			12	75	nA
Input Offset Voltage Drift	$R_S \leq 50\ \Omega$		0.6	3.0	μV/°C
Input Offset Current Drift			2.0		pA/°C
Input Bias Current Drift			15		pA/°C
Differential Input Resistance			300		MΩ
Common Mode Input Resistance			1000		MΩ
Input Voltage Range		±12	±13		V
Supply Voltage Rejection Ratio	$R_S \leq 100\ k\Omega$		80		μV/V
Common Mode Rejection Ratio	$R_S \leq 100\ k\Omega$	70	100		dB
Output Resistance			1.0	4.0	kΩ
Output Common Mode Voltage		−7.0	−5.0	−4.0	V
Differential Output Voltage Swing		±3.0	±7.0	±10	V
Output Sink Current		10	30	80	μA
Differential Load Rejection			5.0	15	μV/μA
Differential Voltage Gain		50	100	250	
Low Frequency Noise	BW = 10 Hz to 500 Hz, $R_S \leq 50\ \Omega$		3.0		μV_{rms}
Long Term Drift	$R_S \leq 50\ \Omega$		5.0		μV/week
Amplifier Supply Current	$T_A = +25°C$		1.0	2.0	mA
Heater Supply Current	$T_A = +25°C$		10	15	mA

TYPICAL PERFORMANCE CURVES

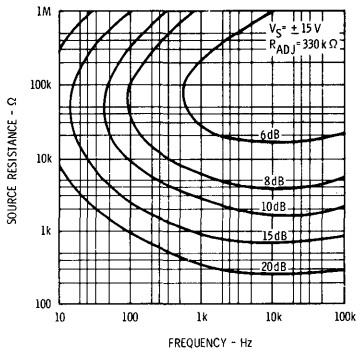
NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



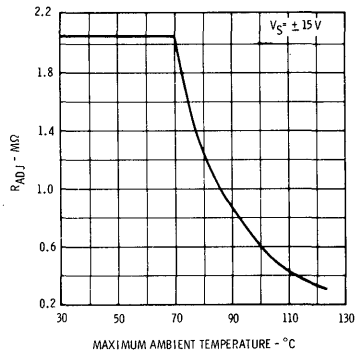
NOISE CURRENT AS A FUNCTION OF FREQUENCY



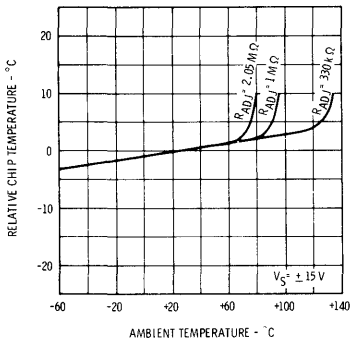
SPOT NOISE FIGURE CONTOURS



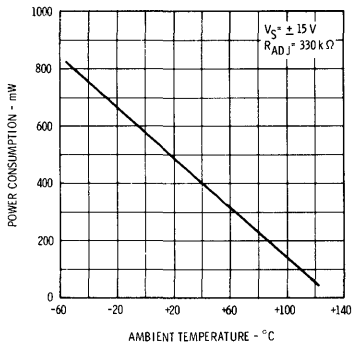
RECOMMENDED R_{ADJ} AS A FUNCTION OF MAXIMUM AMBIENT TEMPERATURE



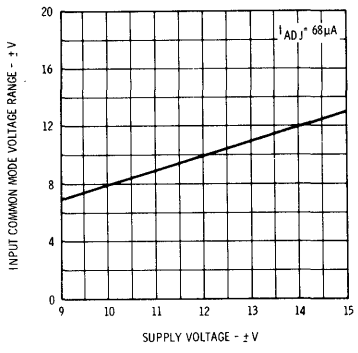
RELATIVE CHIP TEMPERATURE AS A FUNCTION OF AMBIENT TEMPERATURE



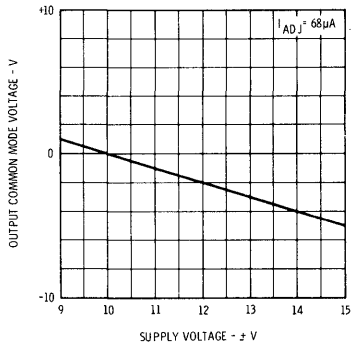
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



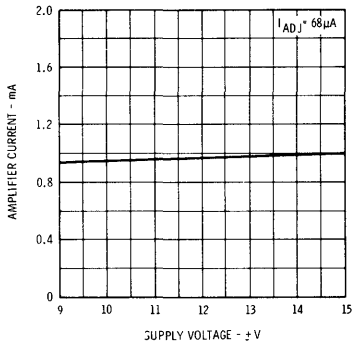
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



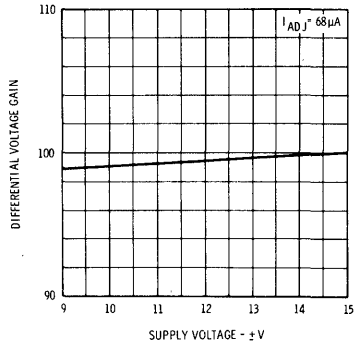
OUTPUT COMMON MODE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



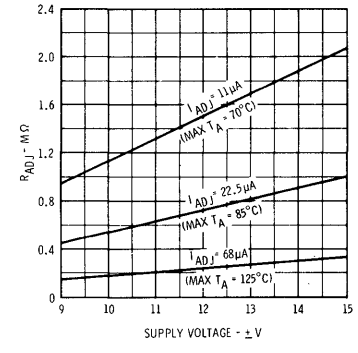
AMPLIFIER CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



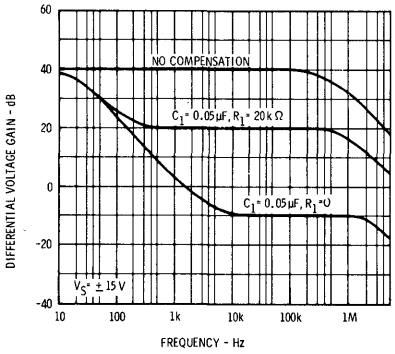
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



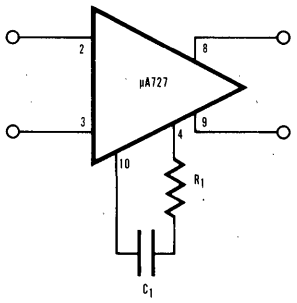
REQUIRED R_{ADJ} FOR CONSTANT I_{ADJ} AS A FUNCTION OF SUPPLY VOLTAGE



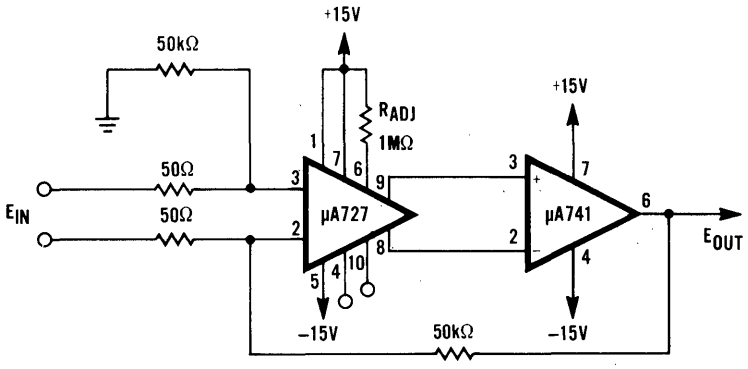
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



FREQUENCY COMPENSATION CIRCUIT



TYPICAL X1000 CIRCUIT



μA729
FM STEREO MULTIPLEX DECODER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

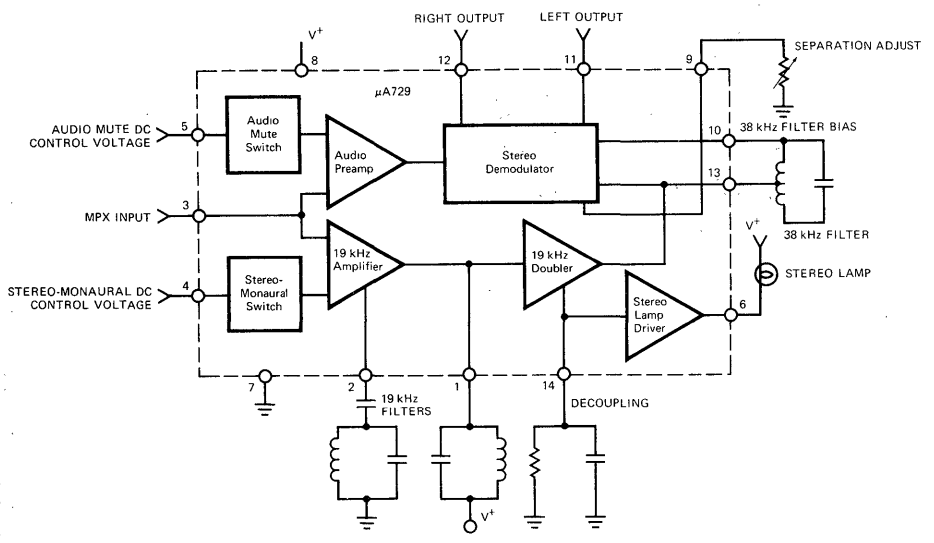
GENERAL DESCRIPTION — The μA729 is a monolithic FM Stereo Multiplex Decoder System constructed on a single silicon chip using the Fairchild Planar* Epitaxial Process. This integrated circuit accomplishes the demodulation of a Stereo Multiplex Signal into the Right and Left audio channels while inherently suppressing SCA frequency components. Internal provision is made for interstation audio muting, stereo/mono mode switching and driving an external stereo mode indicator lamp. The excellent performance, wide supply range and low external parts requirement makes the μA729 suitable for all line-operated and automotive FM Stereo Multiplex applications. For Stereo Decoding with internal separation adjustment, see the μA732 Data Sheet. For stereo decoding without automatic muting and stereo switching, see the μA767 Data Sheet. See Note 1.

- **55 dB CHANNEL SEPARATION, EXTERNALLY ADJUSTABLE**
- **55 dB STORECAST REJECTION WITHOUT SCA FILTERS**
- **HIGH-CURRENT STEREO INDICATOR LAMP DRIVER**
- **OPERATION WITH 8 V TO 14 V SUPPLIES**
- **INTERNAL STEREO SWITCHING AND AUDIO MUTING FUNCTIONS**

ABSOLUTE MAXIMUM RATINGS

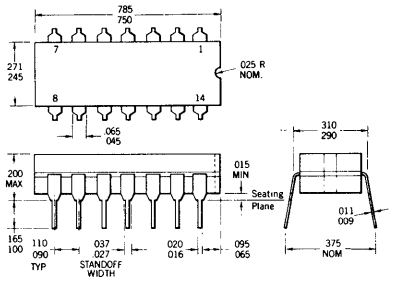
Supply Voltage (Note 2)	+15 V
Voltage at Stereo Lamp Driver Terminal	+22 V
Current into Stereo Lamp Driver Terminal (Note 3)	100 mA
Internal Power Dissipation	670 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 Sec.)	+260°C

BLOCK DIAGRAM



PHYSICAL DIMENSIONS
CERAMIC DIP

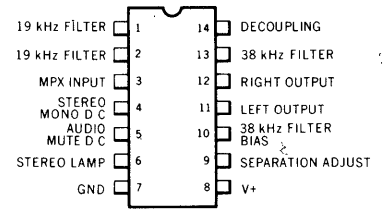
In accordance with
JEDEC (TO-116) outline



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

ORDER PART NO. U6A7729394

CONNECTION DIAGRAM
(TOP VIEW)



Notes on following page.

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = +12$ V, 200 mV RMS Standard Stereo Multiplex signal applied to Input, unless otherwise specified (Note 4). Refer to Test Circuit of Figure 1.)

PARAMETER	MIN.	TYP.	MAX.	UNITS
Supply Current		10	18	mA
Input Resistance	12	20		kΩ
Stereo Separation (Adjusted)				
f = 100 Hz		45		dB
f = 1 kHz	30	55		dB
f = 10 kHz	20	50		dB
Channel Balance (Monaural Input)		0.2		dB
Total Harmonic Distortion		0.5	1.0	%
Voltage Gain		1.0		V/V
67 kHz Storecast Rejection (Note 5)		55		dB
19 kHz Pilot Level Required at Input for:				
Stereo Indicator Lamp on		12	22	mV RMS
Stereo Indicator Lamp off	4.0	8.0		mV RMS
DC Voltage Required at Pin 4 for Stereo-Monaural Switching				
Stereo on	1.0	1.25	1.5	V DC
Stereo off	0.6	0.85	1.0	V DC
DC Voltage Required at Pin 5 for Audio Mute Switching				
Audio on	1.0	1.20	1.5	V DC
Audio off	0.6	0.85	1.0	V DC
Mute Attenuation of Audio	45	55		dB
High Frequency Audio Components in Left and Right Outputs (dB below 1 kHz output)				
19 kHz		30		dB
38 kHz		25		dB

NOTES:

(1) The μA729 is a plug-in replacement for the MC1305. For μA729 applications information, and other Fairchild Communications Integrated circuits see listing on last page.

(2) Power supply transients up to 22V are permissible for periods of 15 seconds. However, extended operation at voltages greater than 15V should be avoided as the maximum allowable internal power dissipation for this device may be exceeded.

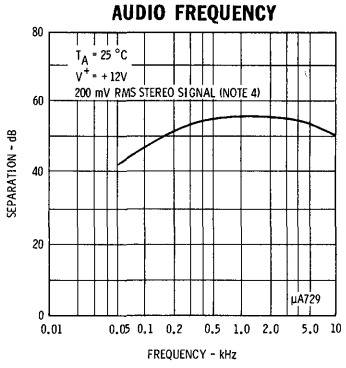
(3) Rating applies to steady state current. Maximum permissible surge current during turn-on of the Stereo Indicator Lamp is 500 mA.

(4) "Standard Stereo Multiplex Signal" here refers to a 200mV RMS (0.56V p-p) composite stereo signal including 10% pilot with L = 1 and R = 1 as described in the FCC Rules on FM Broadcasting.

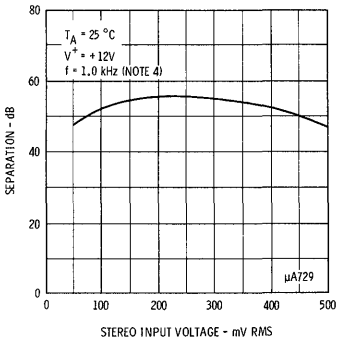
(5) Measured with a stereo composite signal consisting of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on FM Broadcasting.

TYPICAL PERFORMANCE CURVES

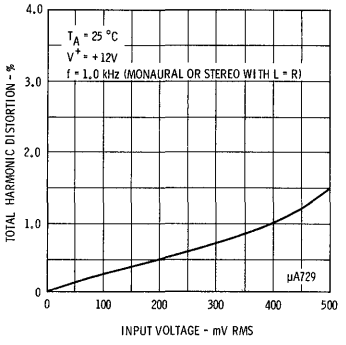
SEPARATION VERSUS AUDIO FREQUENCY



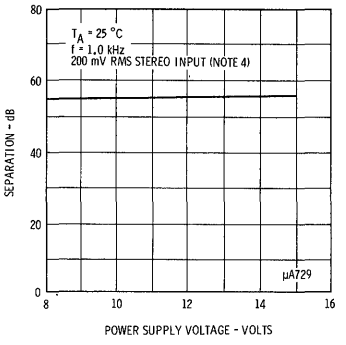
1 kHz SEPARATION VERSUS COMPOSITE INPUT VOLTAGE



1 kHz DISTORTION VERSUS INPUT VOLTAGE



1 kHz SEPARATION VERSUS POWER SUPPLY VOLTAGE



μA729 FM STEREO MULTIPLEX DECODER TEST CIRCUIT AND TYPICAL APPLICATION

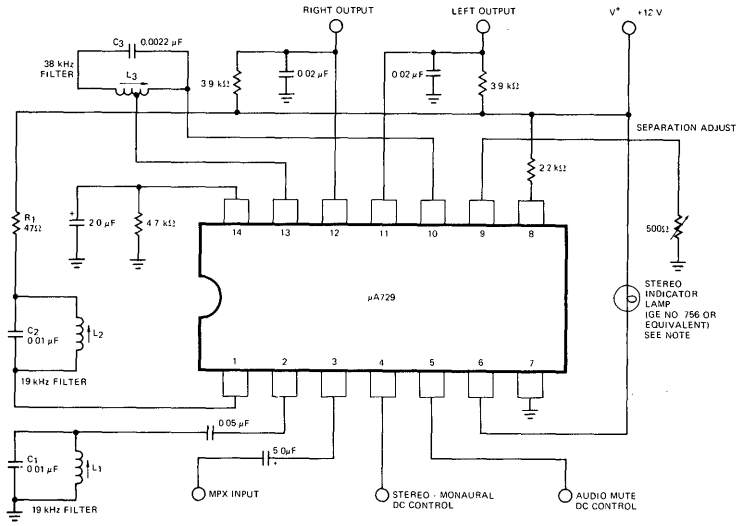
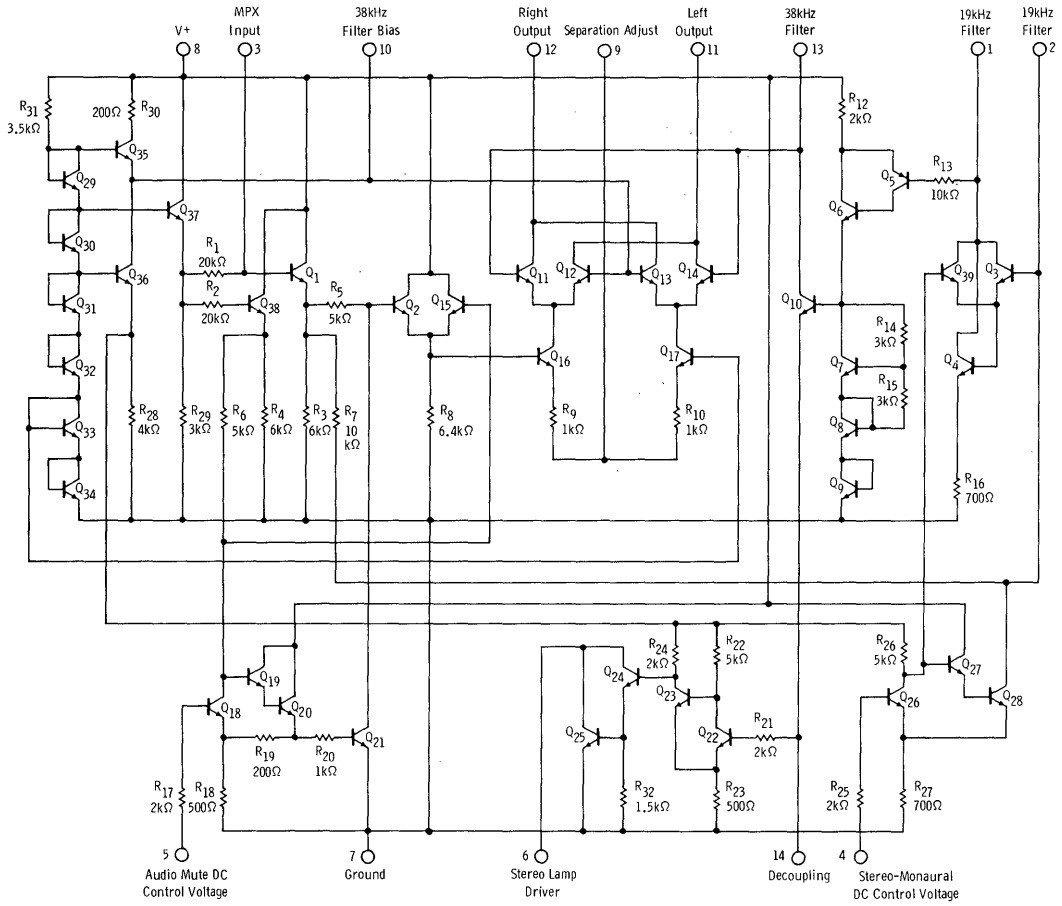


Fig. 1

NOTES:
(1) Capacitors C_1, C_2 and C_3 should be polystyrene or mylar.
(2) Coils L_1 and L_2 are 7.0 mH nominal with $Q_{ul} = 60$ (Miller #1361 or equivalent).
(3) Coil L_3 is 8.0 mH nominal with $Q_{ul} = 80$, tapped at 10:1 turns ratio. (Miller #1362 or equivalent).
(4) Resistor R_1 can be increased (or decreased) in value to increase (or decrease) the 19kHz sensitivity.

μA729 FM STEREO MULTIPLEX DECODER EQUIVALENT CIRCUIT



μA730
DIFFERENTIAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA730 is a differential amplifier constructed on a single silicon-chip using the Fairchild Planar* epitaxial process. This device has a wide range of applications since it has both a differential input and output; any combination of single-ended or differential configurations can be employed at its input and output. The emitter follower output stage gives this device a low output impedance making it useful as a preamplifier.

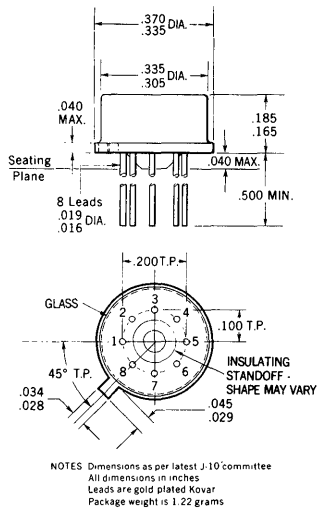
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	15 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	2.5 to 5.5 V
Internal Power Dissipation (Note 1)	500 mW
Operating Temperature Range	
Military (312 Grade)	−55°C to +125°C
Commercial (393 Grade)	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

NOTES:
(1) Rating applies for ambient temperature to +70°C; derate linearly at 6.3 mW/°C for ambient temperatures above +70°C.

PHYSICAL DIMENSIONS

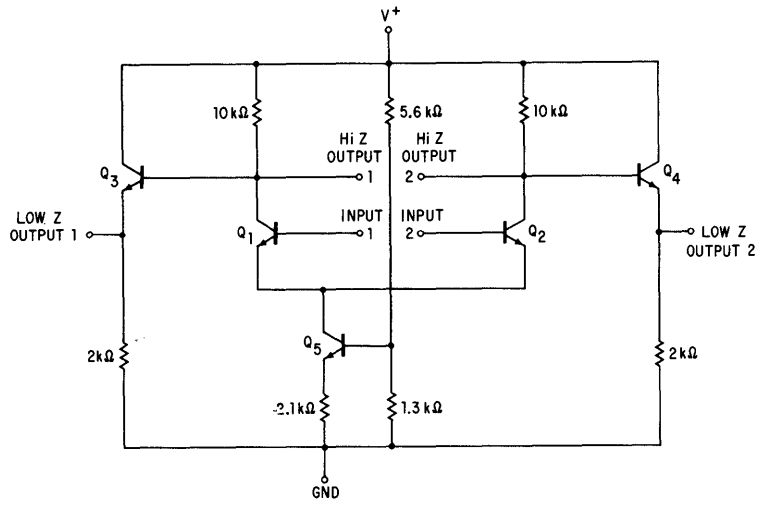
in accordance with JEDEC(TO-99) outline



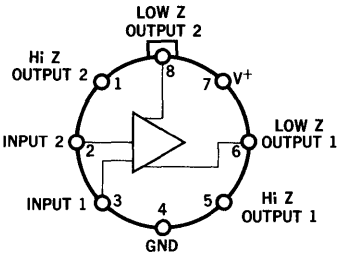
NOTES Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold plated Kovar
Package weight is 1.22 grams

ORDER PART NOS. U5B7730312
U5B7730393

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top View)



Note: Pin 4 connected to case

*Planar is a patented Fairchild process.

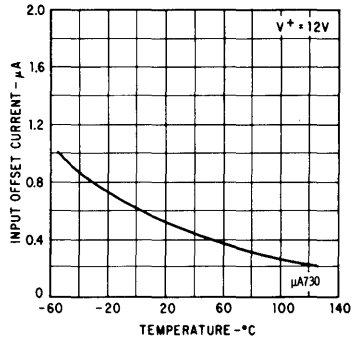
312 GRADE

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V+ = 12.0$ V, and $V_{CM} = 3.5$ V unless otherwise specified)

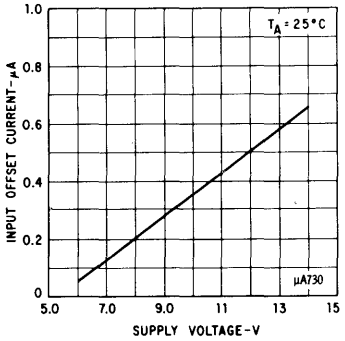
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		1.0	2.5	mV
Input Offset Current			0.5	1.5	μA
Input Bias Current			3.5	7.5	μA
Input Resistance		5.0	20		kΩ
Differential Voltage Gain	$R_L \geq 100$ kΩ	100	145	160	
Differential Distortion	$R_L \geq 100$ kΩ		80	300	mVpp
Bandwidth		1.0	1.5		MHz
Single-Ended Output Resistance			70	500	Ω
Output Voltage Swing	$R_L \geq 100$ kΩ	5.0	8.0		Vpp
Supply Current	$R_L \geq 100$ kΩ		9.5	13	mA
Power Consumption	$R_L \geq 100$ kΩ		114	156	mW
The following specifications apply for $-55°C \leq T_A \leq 125°C$:					
Input Offset Voltage	$R_S \leq 50\Omega$			3.5	mV
Input Offset Current	$T_A = +125°C$		0.2	1.5	μA
	$T_A = -55°C$		1.0	3.0	μA
Input Bias Current	$T_A = -55°C$		6.5	15	μA
Input Resistance		0.9			kΩ
Input Voltage Range		3.5		5.2	V
Common Mode Rejection Ratio	$R_S \leq 50\Omega$, $f \leq 1.0$ kHz, $+3.5\text{ V} \leq V_{CM} \leq +5.2\text{ V}$	70	85		dB
Differential Voltage Gain	$R_L \geq 100$ kΩ	90		175	
Common Mode Output Voltage		5.5	7.0	7.75	V
Output Resistance				600	Ω
Output Voltage Swing		4.5	6.8		Vpp
Supply Current	$T_A = -55°C$		10	15	mA
	$T_A = 125°C$		8.0	11	mA
Power Consumption	$T_A = -55°C$		120	180	mW
	$T_A = 125°C$		96	121	mW

TYPICAL PERFORMANCE CURVES

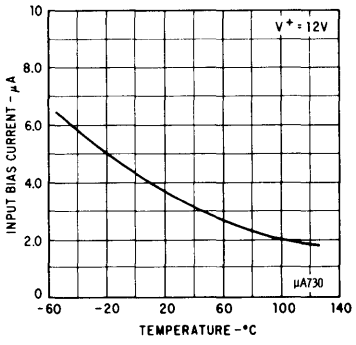
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



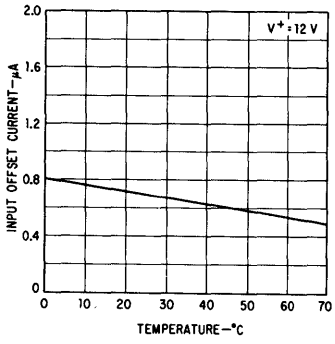
393 GRADE

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V+ = 12.0$ V, and $V_{CM} = 3.5$ V unless otherwise specified)

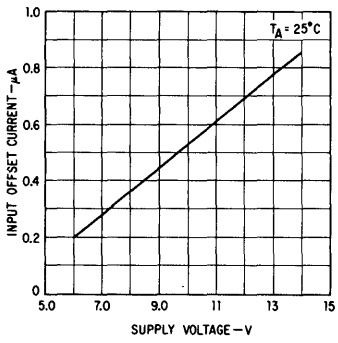
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		2.0	5.0	mV
Input Offset Current			0.7	3.0	μA
Input Bias Current			4.5	16.0	μA
Input Resistance		2.5	15		kΩ
Differential Voltage Gain	$R_L \geq 100$ kΩ	100	135	160	
Differential Distortion	$R_L \geq 100$ kΩ		85	300	mVpp
Bandwidth		1.0	1.5		MHz
Single-Ended Output Resistance			70	500	Ω
Output Voltage Swing	$R_L \geq 100$ kΩ	5.0	8.0		Vpp
Supply Current	$R_L \geq 100$ kΩ		9.5	13	mA
Power Consumption	$R_L \geq 100$ kΩ		114	156	mW
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage	$R_S \leq 50\Omega$			7.5	mV
Input Offset Current	$T_A = +70°C$		0.5	3.0	μA
	$T_A = 0°C$		0.8	5.0	μA
Input Bias Current	$T_A = 0°C$		5.0	20	μA
Input Resistance		1.8			kΩ
Input Voltage Range		+3.5		+5.2	
Common Mode Rejection Ratio	$R_S \leq 50\Omega$, $f \leq 1.0$ kHz, $+3.5\text{ V} \leq V_{CM} \leq +5.2\text{ V}$	60	80		dB
Differential Voltage Gain	$R_L \geq 100$ kΩ	80		190	
Common Mode Output Voltage		5.0	7.0	8.0	V
Output Resistance				600	Ω
Output Voltage Swing		4.5	7.5		Vpp
Supply Current	$T_A = 0°C$		10	15	mA
	$T_A = +70°C$		8.8	13	mA
Power Consumption	$T_A = 0°C$		120	180	mW
	$T_A = +70°C$		106	156	mW

TYPICAL PERFORMANCE CURVES

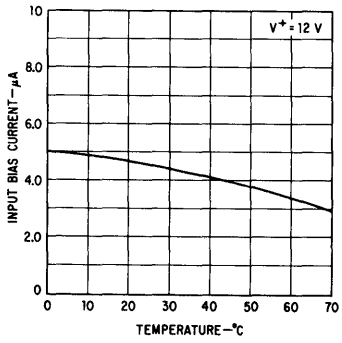
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

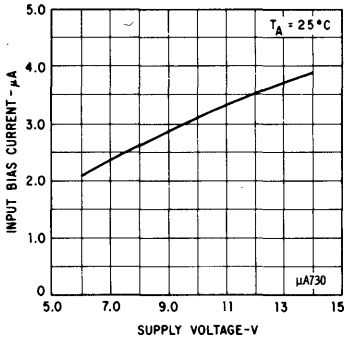


INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

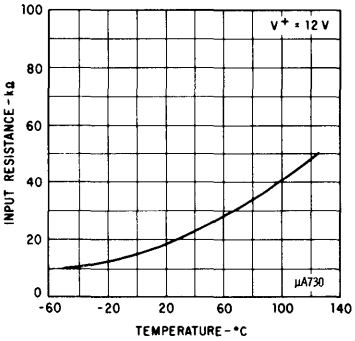


TYPICAL PERFORMANCE CURVES
(FOR 312 GRADE)

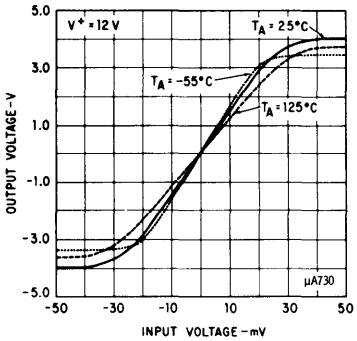
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



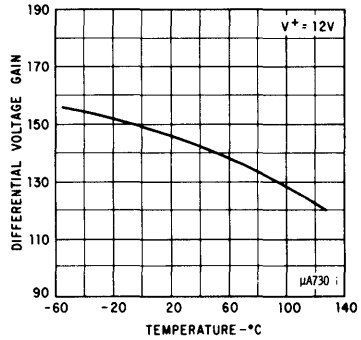
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



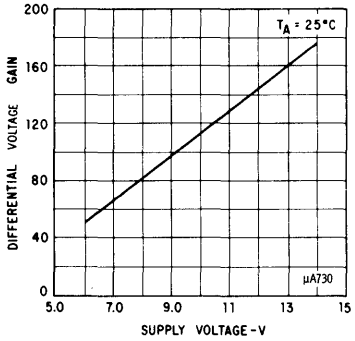
VOLTAGE TRANSFER CHARACTERISTICS



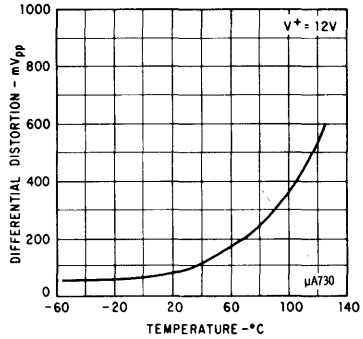
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



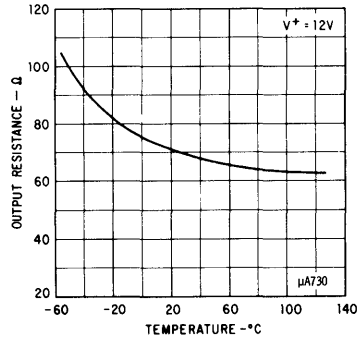
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



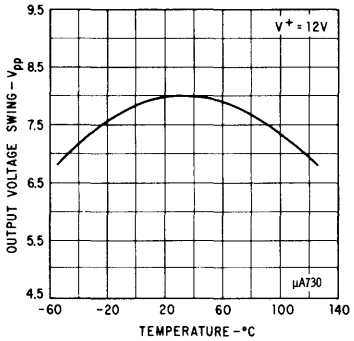
DIFFERENTIAL DISTORTION AS A FUNCTION OF AMBIENT TEMPERATURE



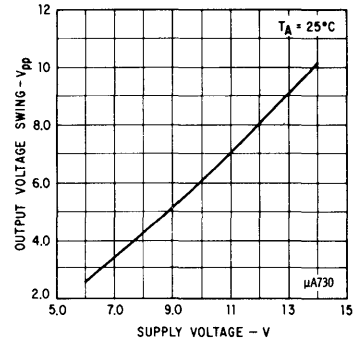
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



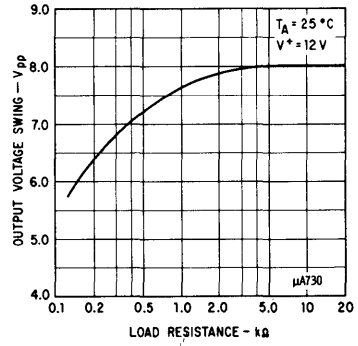
OUTPUT VOLTAGE SWING AS A FUNCTION OF AMBIENT TEMPERATURE



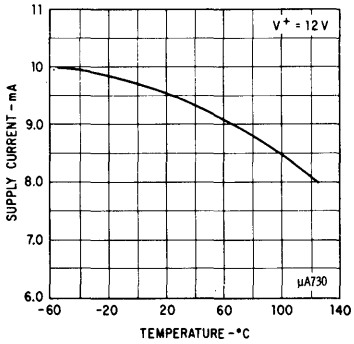
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



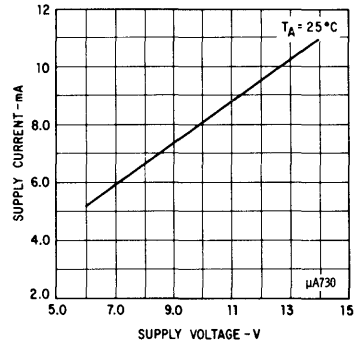
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

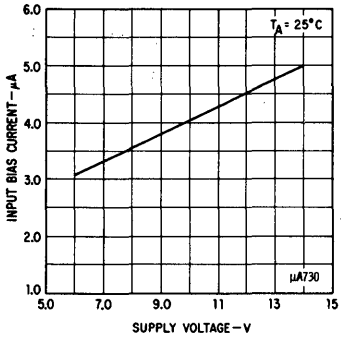


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

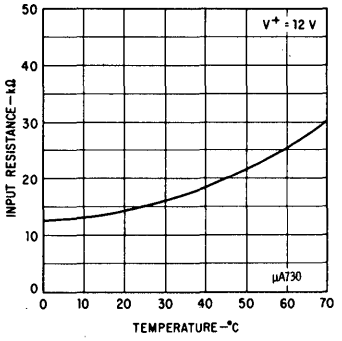


TYPICAL PERFORMANCE CURVES
(FOR 393 GRADE)

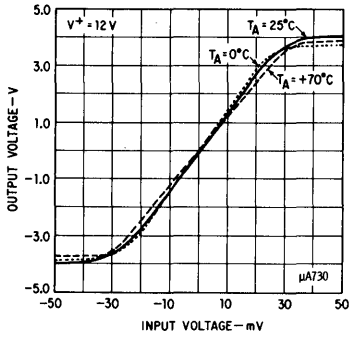
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



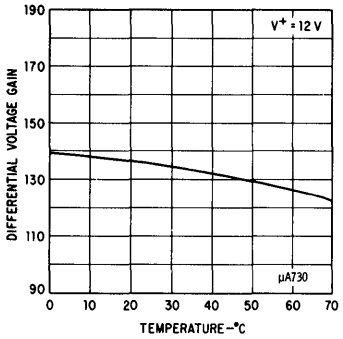
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



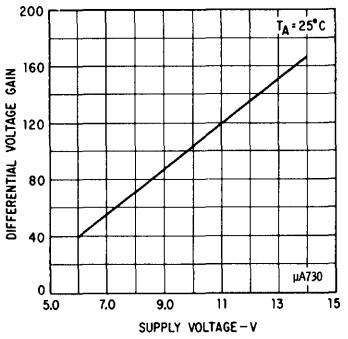
VOLTAGE TRANSFER CHARACTERISTICS



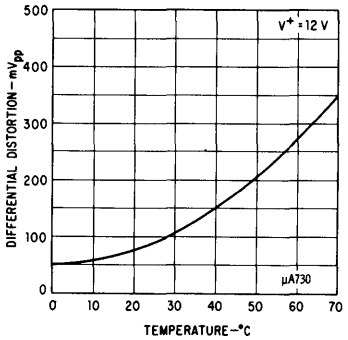
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



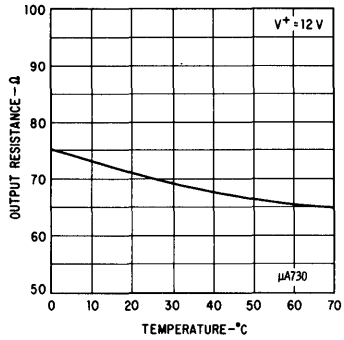
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



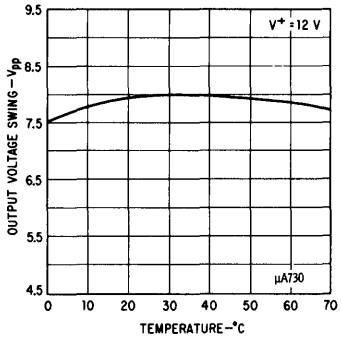
DIFFERENTIAL DISTORTION AS A FUNCTION OF AMBIENT TEMPERATURE



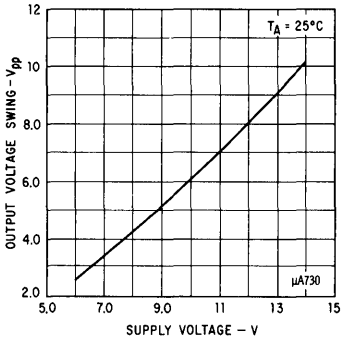
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



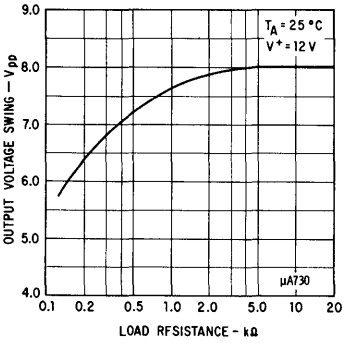
OUTPUT VOLTAGE SWING AS A FUNCTION OF AMBIENT TEMPERATURE



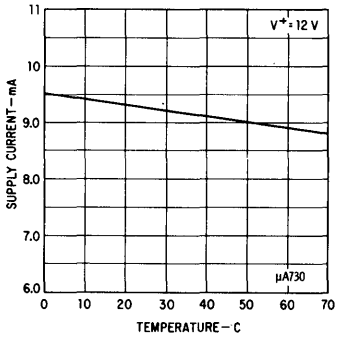
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



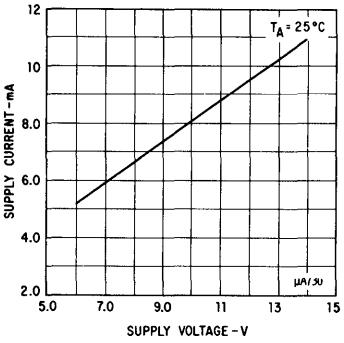
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

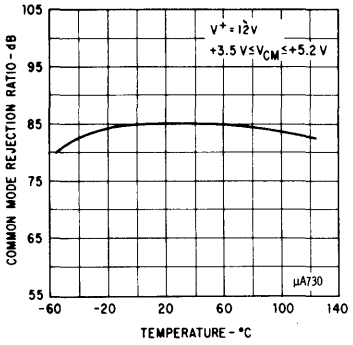


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

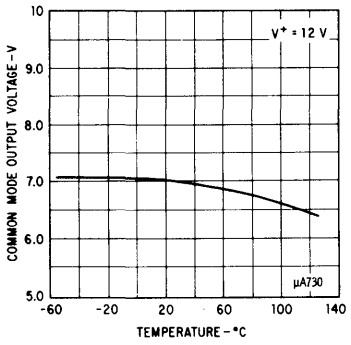


TYPICAL PERFORMANCE CURVES

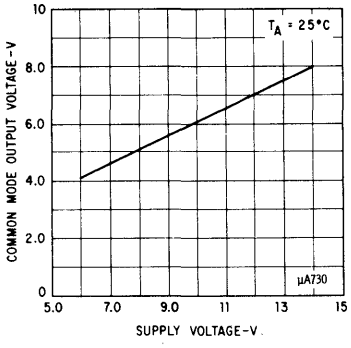
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



μA732
FM STEREO MULTIPLEX DECODER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

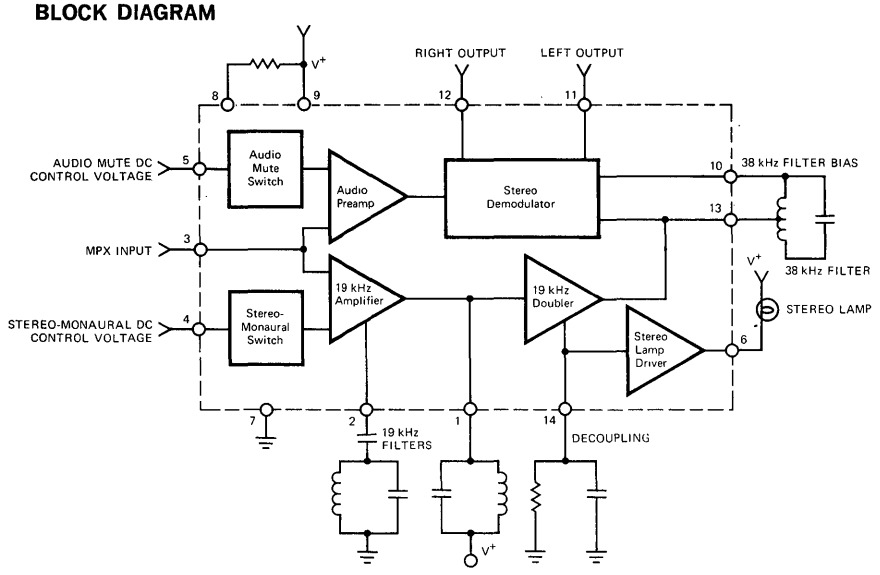
GENERAL DESCRIPTION — The μA732 is a monolithic FM Stereo Multiplex Decoder System constructed on a single silicon chip using the Fairchild Planar* Epitaxial Process. This integrated circuit accomplishes the demodulation of a Stereo Multiplex Signal into the Right and Left audio channels while inherently suppressing SCA frequency components. Internal provision is made for interstation audio muting, stereo/mono mode switching and driving an external stereo mode indicator lamp. The excellent performance, wide supply range and low external parts requirement makes the μA732 suitable for all line-operated and automotive FM Stereo Multiplex applications. For Stereo Decoding with external separation adjustment, see the μA729 Data Sheet. See Note 1.

- **45 dB CHANNEL SEPARATION**
- **55 dB STORECAST REJECTION WITHOUT SCA FILTERS**
- **HIGH-CURRENT STEREO INDICATOR LAMP DRIVER**
- **OPERATION WITH 8 V TO 14 V SUPPLIES**
- **INTERNAL STEREO SWITCHING AND AUDIO MUTING FUNCTIONS**

ABSOLUTE MAXIMUM RATINGS

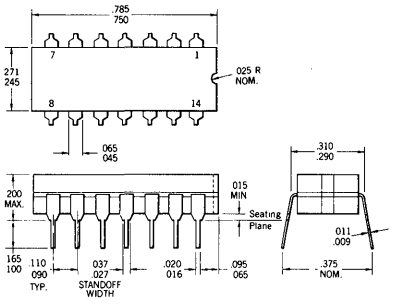
Supply Voltage (Note 2)	+15 V
Voltage at Stereo Lamp Driver Terminal	+22 V
Current into Stereo Lamp Driver Terminal (Note 3)	100 mA
Internal Power Dissipation	670 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 Sec.)	+260°C

BLOCK DIAGRAM



PHYSICAL DIMENSIONS
CERAMIC DIP

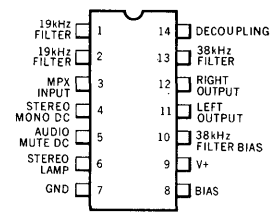
In accordance with
JEDEC (TO-116) outline



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

ORDER PART NO. U6A7732394

CONNECTION DIAGRAM
(TOP VIEW)



Notes on following page.

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = +12$ V, 200 mV RMS Standard Stereo Multiplex signal applied to Input, unless otherwise specified (Note 4). Refer to Test Circuit of Figure 1.)

PARAMETER	MIN.	TYP.	MAX.	UNITS
Supply Current		11	18	mA
Input Resistance	12	20		kΩ
Stereo Separation				
f = 100 Hz		40		dB
f = 1 kHz	30	45		dB
f = 10 kHz	20	40		dB
Channel Balance (Monaural Input)		0.2		dB
Total Harmonic Distortion		0.5	1.0	%
Voltage Gain		1.0		V/V
67 kHz Storecast Rejection (Note 5)		55		dB
19 kHz Pilot Level Required at Input for:				
Stereo Indicator Lamp on		12	22	mV RMS
Stereo Indicator Lamp off	4.0	8.0		mV RMS
DC Voltage Required at Pin 4 for Stereo-Monaural Switching				
Stereo on	1.0	1.25	1.5	V DC
Stereo off	0.6	0.85	1.0	V DC
DC Voltage Required at Pin 5 for Audio Mute Switching				
Audio on	1.0	1.20	1.5	V DC
Audio off	0.6	0.85	1.0	V DC
Mute Attenuation of Audio	45	55		dB
High Frequency Audio Components in Left and Right Outputs (dB below 1 kHz output)				
19 kHz		30		dB
38 kHz		25		dB

NOTES:

(1) The μA732 is a plug-in replacement for the MC1304.

(2) Power supply transients up to 22V are permissible for periods of 15 seconds. However, extended operation at voltages greater than 15V should be avoided as the maximum allowable internal power dissipation for this device may be exceeded.

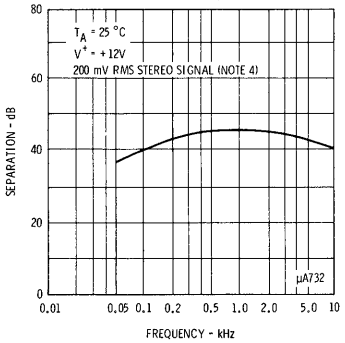
(3) Rating applies to steady state current. Maximum permissible surge current during turn-on of the Stereo Indicator Lamp is 500 mA.

(4) "Standard Stereo Multiplex Signal" here refers to a 200mV RMS (0.56V p-p) composite stereo signal including 10% pilot with L = 1 and R = 1 as described in the FCC Rules on FM Broadcasting.

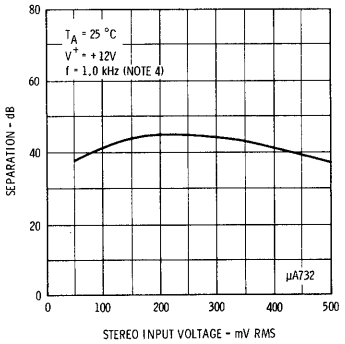
(5) Measured with a stereo composite signal consisting of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on FM Broadcasting.

TYPICAL PERFORMANCE CURVES

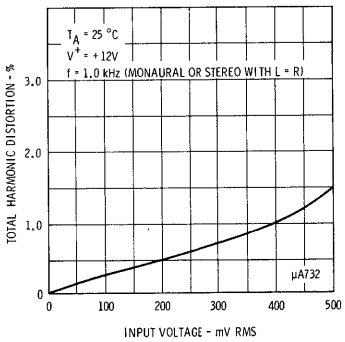
SEPARATION VERSUS AUDIO FREQUENCY



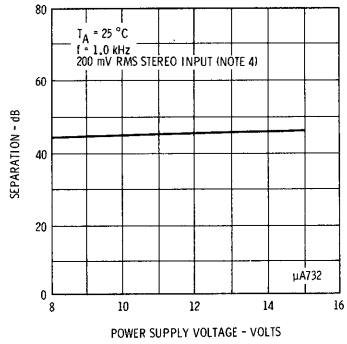
1 kHz SEPARATION VERSUS COMPOSITE INPUT VOLTAGE



1 kHz DISTORTION VERSUS INPUT VOLTAGE



1 kHz SEPARATION VERSUS POWER SUPPLY VOLTAGE



μA732 FM STEREO MULTIPLEX DECODER TEST CIRCUIT AND TYPICAL APPLICATION

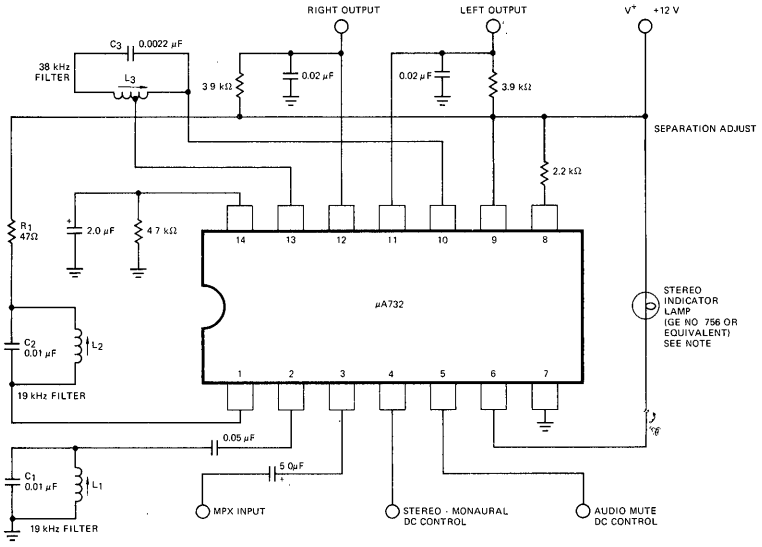
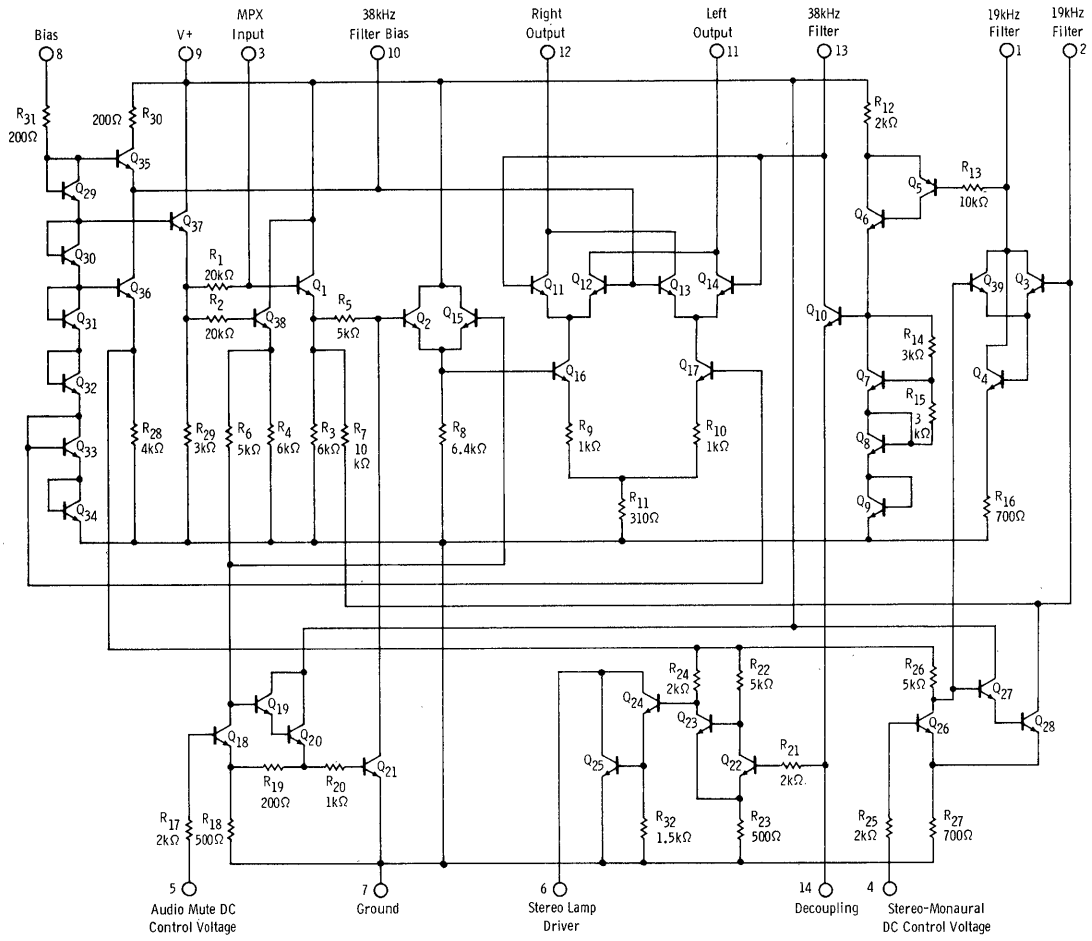


Fig. 1

NOTES:

(1) Capacitors C_1, C_2 and C_3 should be polystyrene or mylar.
(2) Coils L_1 and L_2 are 7.0 mH nominal with $Q_{u1} = 60$ (Miller #1361 or equivalent).
(3) Coil L_3 is 8.0mH nominal with $Q_{u1} = 80$, tapped at 10:1 turns ratio. (Miller #1362 or equivalent).
(4) Resistor R_1 can be increased (or decreased) in value to increase (or decrease) the 19kHz sensitivity.

μA732 FM STEREO MULTIPLEX DECODER EQUIVALENT CIRCUIT



μA733

DIFFERENTIAL VIDEO AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA733 is a monolithic two-stage differential input, differential output video amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. Internal series-shunt feedback is used to obtain wide bandwidth, low phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. It offers fixed gains of 10, 100, or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding and in high-speed thin film or plated wire memories. Other applications include general-purpose video and pulse amplifiers where wide bandwidth, low phase shift, and excellent gain stability are required.

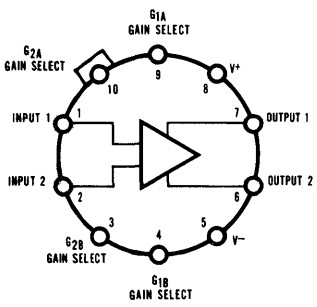
- **120 MHz BANDWIDTH**
- **250 kΩ INPUT RESISTANCE**
- **SELECTABLE GAINS OF 10, 100, AND 400**
- **NO FREQUENCY COMPENSATION REQUIRED**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±8 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	±6 V
Output Current	10 mA
Internal Power Dissipation (Note 1)	
Flatpak	570 mW
Metal Can	500 mW
Ceramic DIP	670 mW
Operating Temperature Range	−55° C to +125° C
Storage Temperature Range	−65° C to +150° C
Lead Temperature (Soldering, 60 second time limit)	300° C

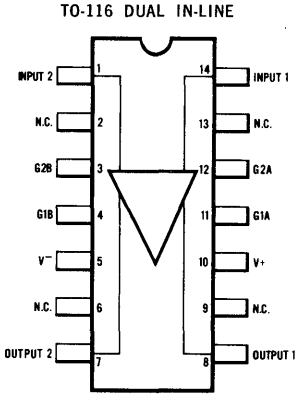
CONNECTION DIAGRAM (Top Views)

TO-100 METAL CAN

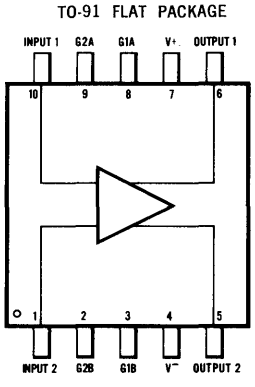


Note: Pin 5 connected to case.

TO-116 DUAL IN-LINE



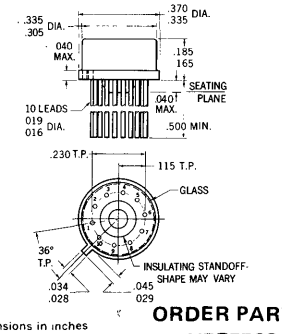
TO-91 FLAT PACKAGE



PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-100) outline

METAL CAN

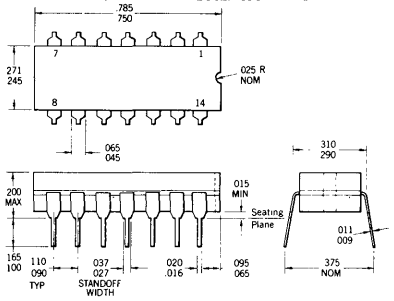


NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams
Lead 5 is connected to case

ORDER PART NO.
U5F773312
U5F773393

In accordance with JEDEC (TO-116) outline

14 LEAD DUAL IN-LINE

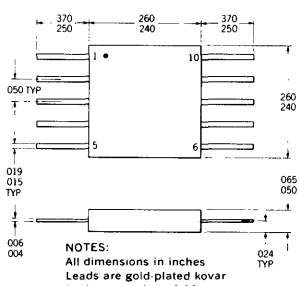


NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams

ORDER PART NO. U6A7733312
U6A7733393

In accordance with JEDEC (TO-91) outline

10 LEAD CERPAK



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.26 gram

ORDER PART NO. U3F7733312

Notes on following pages.

*Planar is a patented Fairchild process.

312 GRADE

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_S = \pm 6.0$ V unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain					
Gain 1 (Note 2)		300	400	500	
Gain 2 (Note 3)		90	100	110	
Gain 3 (Note 4)		9.0	10	11	
Bandwidth	$R_S = 50\ \Omega$				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	$R_S = 50\ \Omega$, $V_{out} = 1$ Vpp				
Gain 1			10.5		ns
Gain 2			4.5	10	ns
Gain 3			2.5		ns
Propagation Delay	$R_S = 50\ \Omega$, $V_{out} = 1$ Vpp				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		kΩ
Gain 2		20	30		kΩ
Gain 3			250		kΩ
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	3.0	μA
Input Bias Current			9.0	20	μA
Input Noise Voltage	$R_S = 50\ \Omega$, BW = 1 kHz to 10 MHz		12		μVrms
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	$V_{cm} = \pm 1$ V, f ≤ 100 kHz	60	86		dB
Gain 2	$V_{cm} = \pm 1$ V, f = 5 MHz		60		dB
Supply Voltage Rejection Ratio					
Gain 2	$\Delta V_S = \pm 0.5$ V	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.0	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		Vpp
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA
The following specifications apply for $-55°C \leq T_A \leq +125°C$					
Differential Voltage Gain					
Gain 1 (Note 2)		200		600	
Gain 2 (Note 3)		80		120	
Gain 3 (Note 4)		8.0		12	
Input Resistance—Gain 2		8.0			kΩ
Input Offset Current				5.0	μA
Input Bias Current				40	μA
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio		50			dB
Supply Voltage Rejection Ratio		50			dB
Output Offset Voltage—Gain 1				1.5	V
Output Offset Voltage—Gain 2 & 3				1.2	V
Output Swing		2.5			Vpp
Output Sink Current		2.2			mA
Positive Supply Current				27	mA

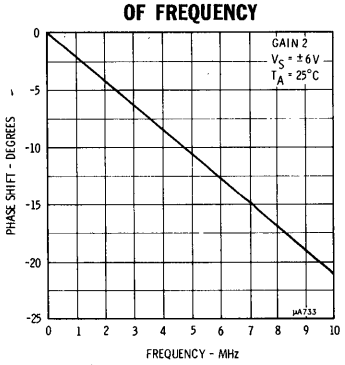
393 GRADE

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V_S = \pm 6.0$ V unless otherwise specified)

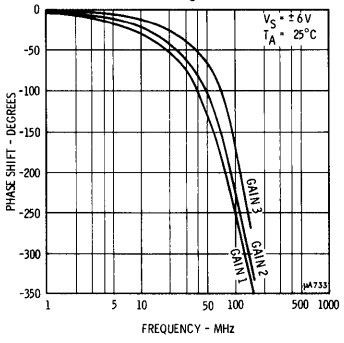
PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain					
Gain 1 (Note 2)		250	400	600	
Gain 2 (Note 3)		80	100	120	
Gain 3 (Note 4)		8.0	10	12	
Bandwidth	$R_S = 50\ \Omega$				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	$R_S = 50\ \Omega$, $V_{out} =$ 1 Vpp				
Gain 1			10.5		ns
Gain 2			4.5	12	ns
Gain 3			2.5		ns
Propagation Delay	$R_S = 50\ \Omega$, $V_{out} =$ 1 Vpp				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		kΩ
Gain 2		10	30		kΩ
Gain 3			250		kΩ
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	5.0	μA
Input Bias Current			9.0	30	μA
Input Noise Voltage	$R_S = 50\ \Omega$, BW = 1 kHz to 10 MHz		12		μVrms
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	$V_{cm} = \pm 1$ V, f ≤ 100 kHz	60	86		dB
Gain 2	$V_{cm} = \pm 1$ V, f = 5 MHz		60		dB
Supply Voltage Rejection Ratio					
Gain 2	$\Delta V_S = \pm 0.5$ V	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.5	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		Vpp
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Differential Voltage Gain					
Gain 1 (Note 2)		250		600	
Gain 2 (Note 3)		80		120	
Gain 3 (Note 4)		8.0		12	
Input Resistance—Gain 2		8.0			kΩ
Input Offset Current				6.0	μA
Input Bias Current				40	μA
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	$V_{cm} = \pm 1$ V, f ≤ 100 kHz	50			dB
Supply Voltage Rejection Ratio					
Gain 2	$\Delta V_S = \pm 0.5$ V	50			dB
Output Offset Voltage (All Gain)				1.5	V
Output Voltage Swing		2.8			Vpp
Output Sink Current		2.5			mA
Power Supply Current				27	mA

TYPICAL PERFORMANCE CURVES

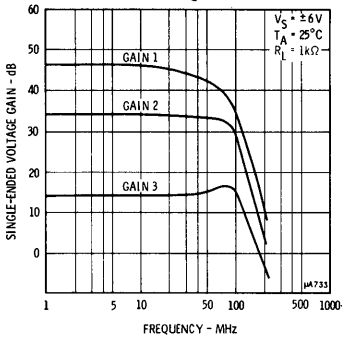
PHASE SHIFT AS A FUNCTION OF FREQUENCY



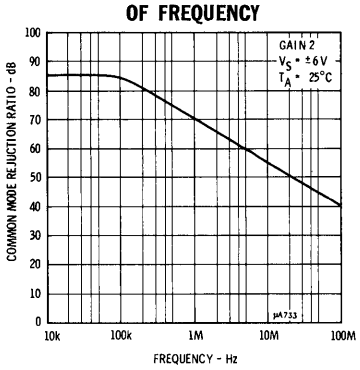
PHASE SHIFT AS A FUNCTION OF FREQUENCY



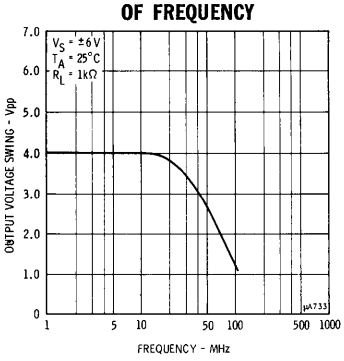
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



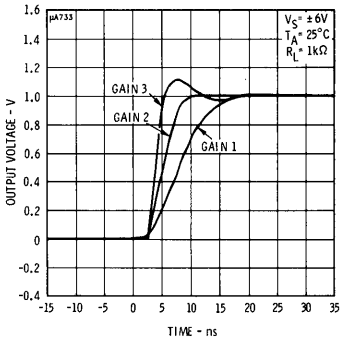
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



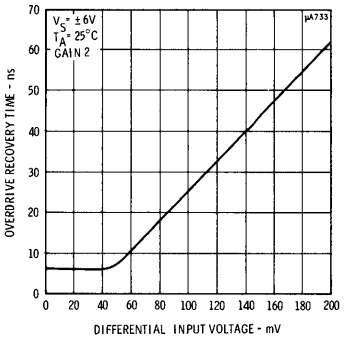
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



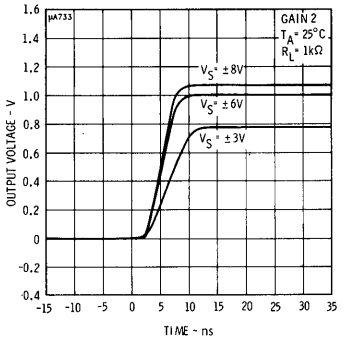
PULSE RESPONSE



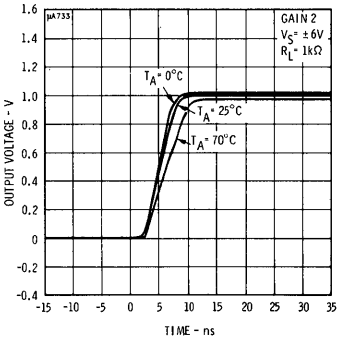
DIFFERENTIAL OVERDRIVE RECOVERY TIME



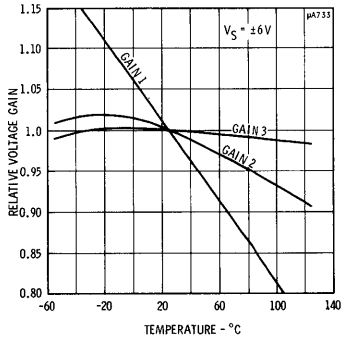
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



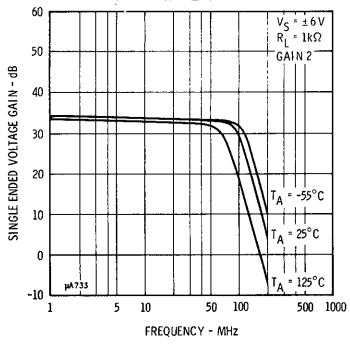
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



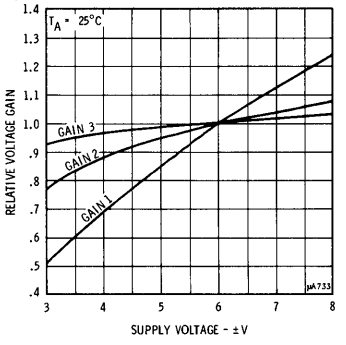
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



GAIN VERSUS FREQUENCY AS A FUNCTION OF TEMPERATURE

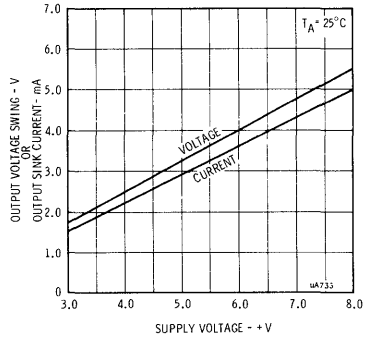


VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

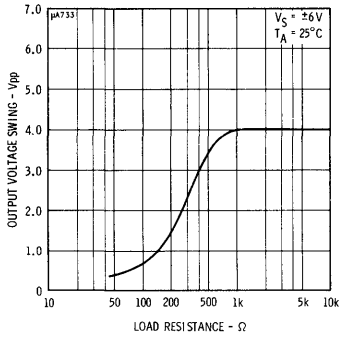


TYPICAL PERFORMANCE CURVES

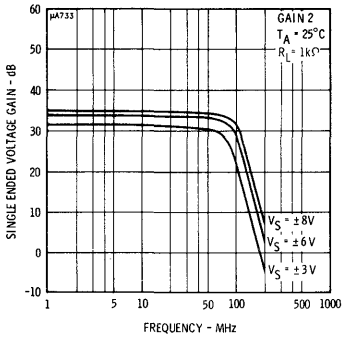
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



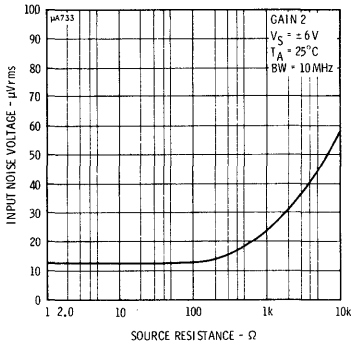
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



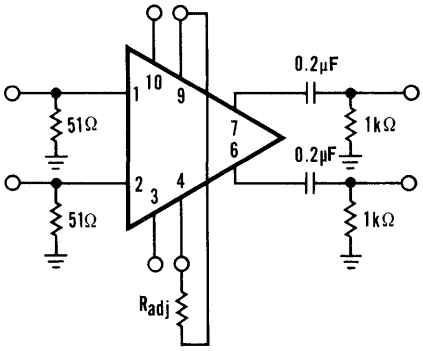
GAIN VERSUS FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



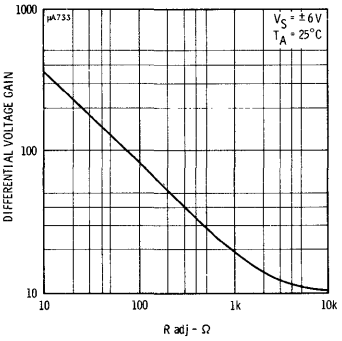
INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE



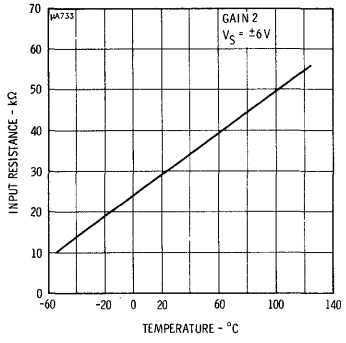
VOLTAGE GAIN ADJUST CIRCUIT



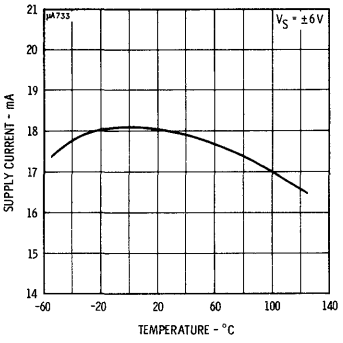
VOLTAGE GAIN AS A FUNCTION OF R_{ADJ}



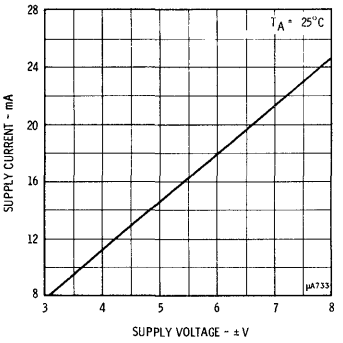
INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

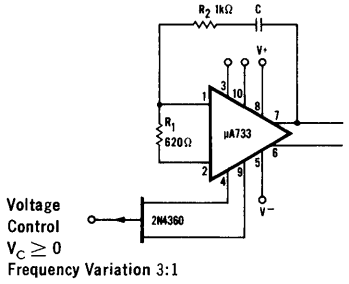


NOTES

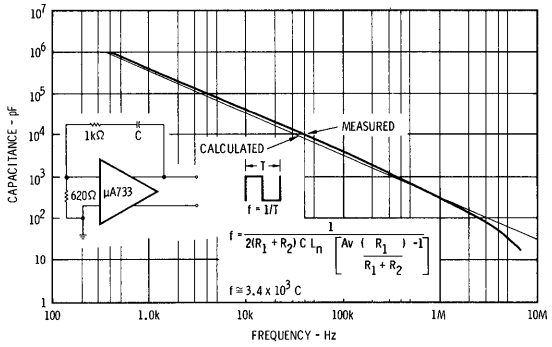
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can, 8.3 mW/°C for the Ceramic DIP and 7.1 mW/°C for the Flatpak package.
2. Gain Select pins G_{1A} and G_{1B} connected together.
3. Gain Select pins G_{2A} and G_{2B} connected together.
4. All Gain Select pins open.

TYPICAL APPLICATIONS

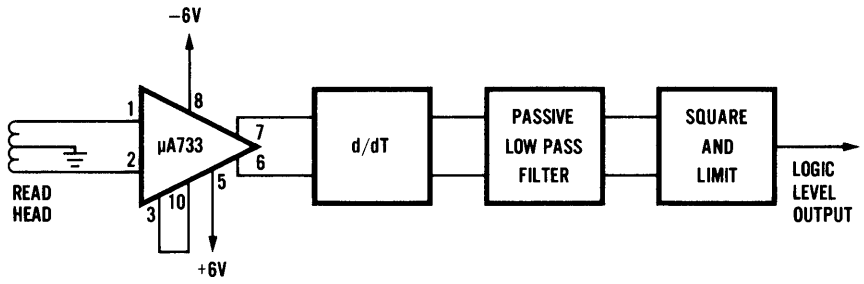
VOLTAGE CONTROLLED OSCILLATOR



OSCILLATOR FREQUENCY FOR VARIOUS CAPACITOR VALUES

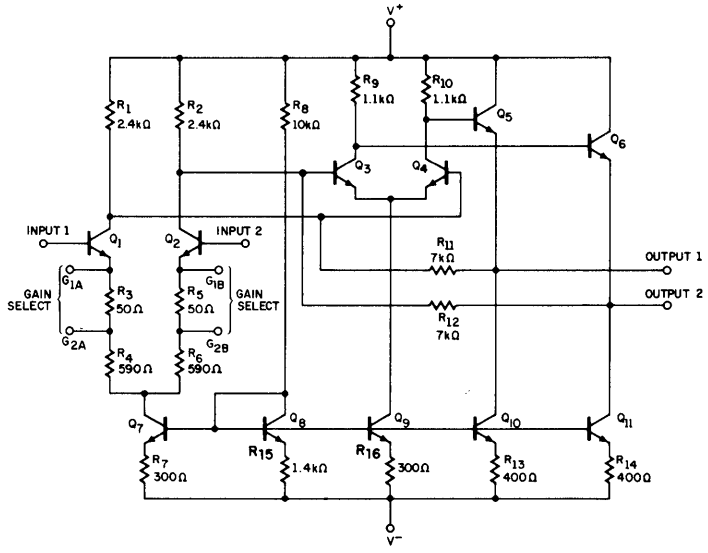


PHASE ENCODING PLAYBACK SYSTEM



Phase Linearity:	±2° from 2 to 5 MHz
Input Resistance:	25 kΩ
Input Capacity:	2 pF
Fixed Gain:	100

EQUIVALENT CIRCUIT



μA734

PRECISION VOLTAGE COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

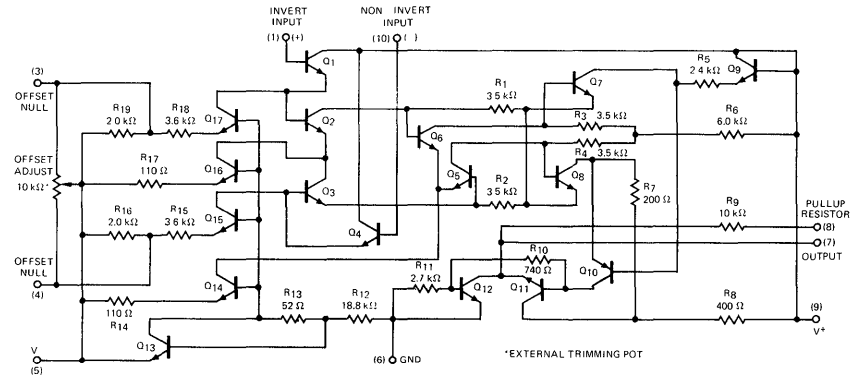
GENERAL DESCRIPTION — The μA734 is a precision voltage comparator constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It is specifically designed for high accuracy level sensing and measuring applications. The μA734 is extremely useful for analog-to-digital converters with twelve bit accuracies and one mega-bit conversion rates. Maximum resolution is obtained by high gain, low input offset current, and low input offset voltage. Its superior temperature stability can be improved by offset nulling which further reduces offset voltage drift. Balanced or unbalanced supply operation and standard TTL logic compatibility enhance the μA734's versatility.

- **CONSTANT INPUT IMPEDANCE OVER DIFFERENTIAL INPUT RANGE**
- **HIGH INPUT IMPEDANCE**
- **LOW DRIFT**
- **HIGH GAIN**
- **BALANCED OFFSET NULL CAPABILITY**
- **WIDE SUPPLY VOLTAGE RANGE**
- **TTL COMPATIBLE**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Peak Output Current	10 mA
Differential Input Voltage	±10 V
Input Voltage Range	$\pm V_S$ −2.0 V
Voltage Between Offset Null and V⁻	±0.5 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Ceramic DIP	670 mW
Silicone DIP	340 mW
Mini DIP	310 mW
Operating Temperature Range	
Military (312 Grade)	−55°C to +125°C
Commercial (393 Grade)	0°C to + 70°C
Storage Temperature Range	
Metal Can, Ceramic DIP	−65°C to +150°C
Silicone DIP and Mini DIP	−55°C to +125°C
Lead Temperature	
Metal Can, Ceramic DIP (Soldering, 60 Seconds Max.)	300°C
Silicone DIP and Mini DIP (Soldering, 10 Seconds Max.)	260°C

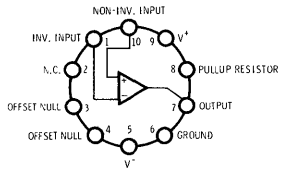
EQUIVALENT CIRCUIT



Notes on following pages.

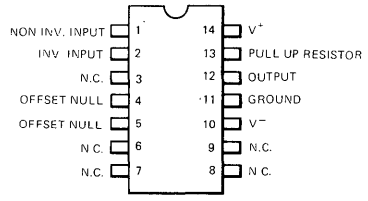
CONNECTION DIAGRAMS

10 LEAD METAL CAN
(TOP VIEW)



ORDER PART NOS: U5F7734312
U5F7734393

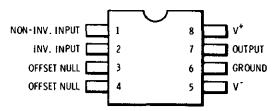
14 LEAD DIP
(TOP VIEW)



FOR CERAMIC DIP
ORDER PART NOS: U6A7734312
U6A7734393

FOR SILICONE DIP
ORDER PART NO: U9A7734393

MINI DIP
(TOP VIEW)



ORDER PART NO: U9T7734393

*Planar is a patented Fairchild process.

±15 VOLT OPERATION FOR 312 GRADE

ELECTRICAL CHARACTERISTICS [T_A = 25°C, Pin 8 (Note 2) tied to +15 V, unless otherwise specified]

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\ k\Omega$		0.9	3.0	mV
Input Offset Current			1.5	10	nA
Input Bias Current			28	50	nA
Input Resistance		20	60		MΩ
Input Capacitance			3.0		pF
Offset Voltage Adjustment Range			8.5		mV
Large Signal Voltage Gains	R_L = 1.5 kΩ to +5.0V	35k	70k		V/V
Positive Supply Current – Output Low			4.0	5.0	mA
Negative Supply Current – Output Low			1.5	2.0	mA
Power Consumption – Output Low			82	105	mW
Transient Response	R_L = 1.5 kΩ to +5.0V 5mV overdrive, 100mV pulse		0.2		μs
The following specifications apply for -55°C ≤ T_A ≤ +125°C					
Input Offset Voltage	$R_S \leq 50\ k\Omega$		1.1	4.0	mV
Input Offset Current			3.0	20	nA
Average Input Offset Voltage Drift	$R_S \leq 50\ k\Omega$				
Without External Trim			2.5	15	μV/°C
Average Input Offset Current Drift					
	+25°C to +125°C		0.01	0.1	nA/°C
	+25°C to -55°C		0.05	0.4	nA/°C
Input Bias Current				150	nA
Large Signal Voltage Gain	R_L = 1.5 kΩ to +5.0V	25k			V/V
Input Common Mode Voltage Range		±10			V
Differential Input Voltage Range		±10			V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	70	100		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$		5.0	100	μV/V
(V_S = ±5V to ±18V)					
Positive Output Voltage Level	I_O = .080 mA	7.0			V
	I_O = .080 mA, V_8 = +5V	2.4		5.0	V
Negative Output Voltage Level	I_{SINK} = 3.2 mA			0.4	V
Positive Supply Current – Output Low				7.0	mA
Negative Supply Current – Output Low				2.5	mA
Power Dissipation – Output Low				145	mW

±15 VOLT OPERATION FOR 393 GRADE

ELECTRICAL CHARACTERISTICS [T_A = 25°C, Pin 8 (Note 2) tied to +15 V, unless otherwise specified]

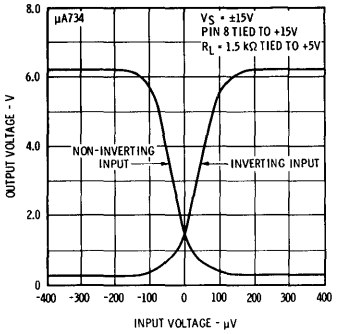
PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\ k\Omega$		1.1	5.0	mV
Input Offset Current			3.5	25	nA
Input Bias Current			30	100	nA
Input Resistance		7.0	55		MΩ
Input Capacitance			3.0		pF
Offset Voltage Adjustment Range			8.5		mV
Large Signal Voltage Gains	R_L = 1.5 kΩ to +5.0V	35k	60k		V/V
Positive Supply Current – Output Low			4.0	5.0	mA
Negative Supply Current – Output Low			1.5	2.0	mA
Power Consumption – Output Low			82	105	mW
Transient Response	R_L = 1.5 kΩ to +5.0V 5 mV overdrive, 100 mV Pulse		0.2		μs
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage	$R_S \leq 50\ k\Omega$		1.2	7.5	mV
Input Offset Current			4.0	45	nA
Average Input Offset Voltage Drift	$R_S \leq 50\Omega$				
Without External Trim			3.5	20	μV/°C
Average Input Offset Current Drift					
	+25°C to +70°C		0.02	0.3	nA/°C
	+25°C to 0°C		0.05	0.75	nA/°C
Input Bias Current				150	nA
Large Signal Voltage Gain	R_L = 1.5 kΩ to +5.0V	25k			V/V
Input Common Mode Voltage Range		±10			V
Differential Input Voltage Range		±10			V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	70	100		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$		6.0	100	μV/V
(V_S = ±15V to ±18V)					
Positive Output Voltage Level	I_O = .080 mA	7.0			V
	I_O = .080 mA, V_8 = +5V	2.4		5.0	V
Negative Output Voltage Level	I_{SINK} = 3.2 mA			0.4	V
Positive Supply Current – Output Low				7.0	mA
Negative Supply Current – Output Low				2.5	mA
Power Dissipation – Output Low				145	mW

NOTES

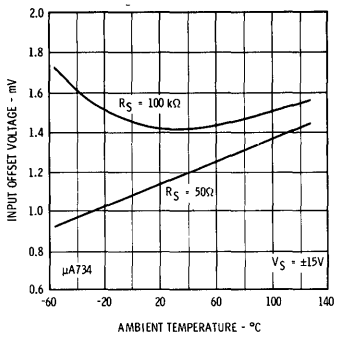
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for Metal Can, 8.3 mW/°C for Ceramic DIP, 6.3 mW/°C for Silicone DIP and 5.6 mW/°C for the Mini DIP package.
2. Pin numbers refer to metal can package.

TYPICAL PERFORMANCE CURVES (Note 2)

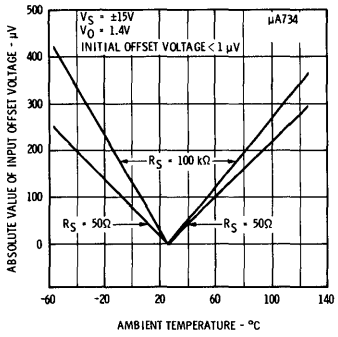
TRANSFER CHARACTERISTICS



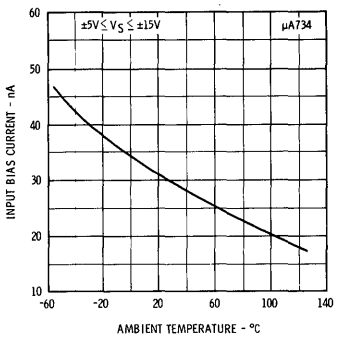
UN-NULLED INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



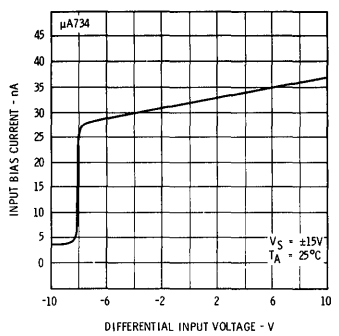
INPUT OFFSET VOLTAGE CHANGE AS A FUNCTION OF AMBIENT TEMPERATURE - NULLED TO ZERO AT 25°C



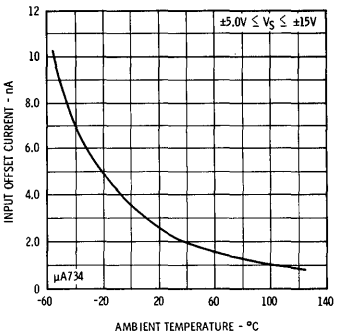
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



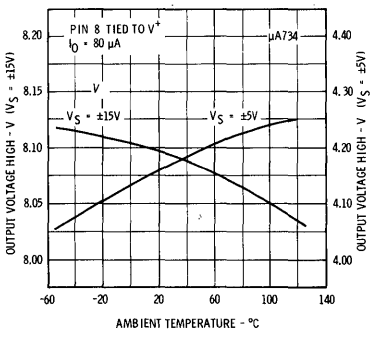
INPUT BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



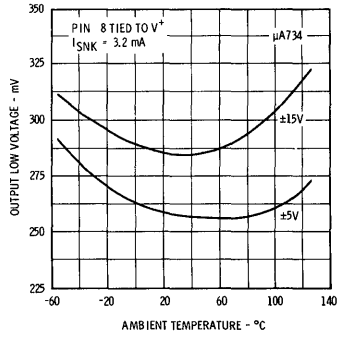
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



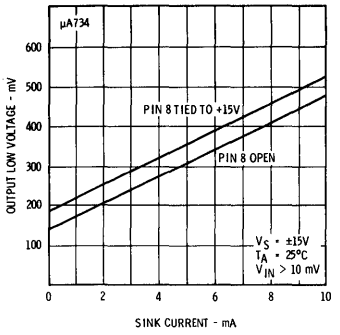
OUTPUT HIGH VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE AND AMBIENT TEMPERATURE



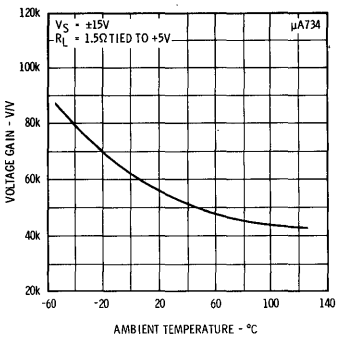
OUTPUT LOW VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE AND AMBIENT TEMPERATURE



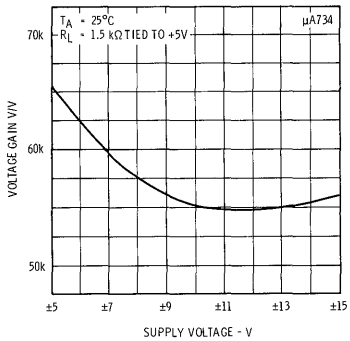
OUTPUT VOLTAGE LOW VS SINK CURRENT



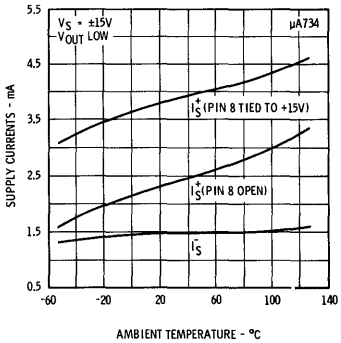
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

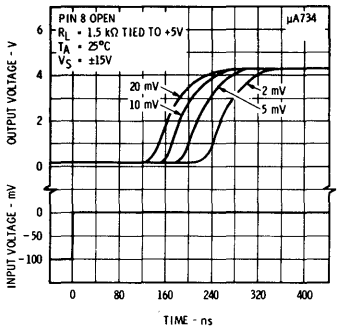


POSITIVE AND NEGATIVE SUPPLY CURRENTS AS A FUNCTION OF AMBIENT TEMPERATURE

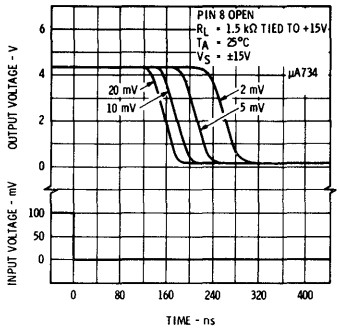


TYPICAL PERFORMANCE CURVES

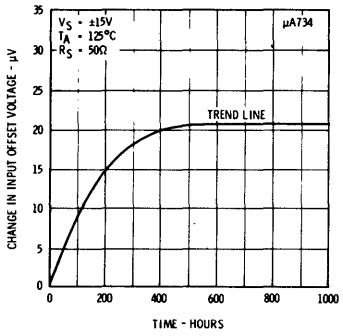
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



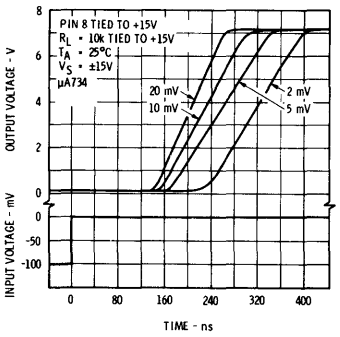
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



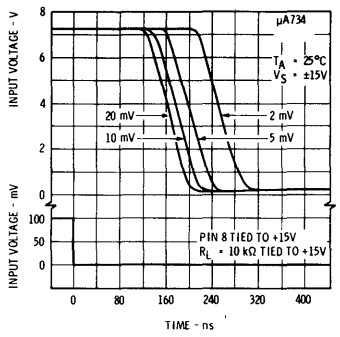
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



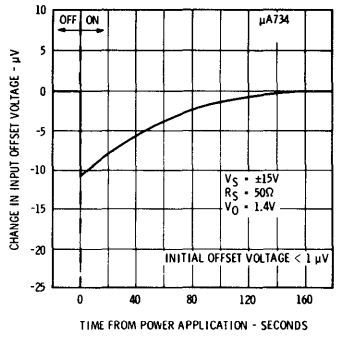
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



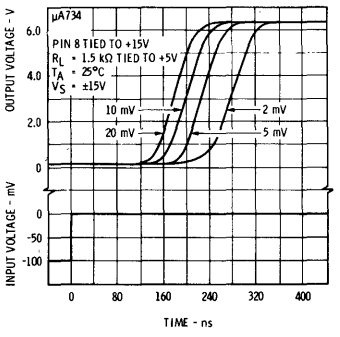
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



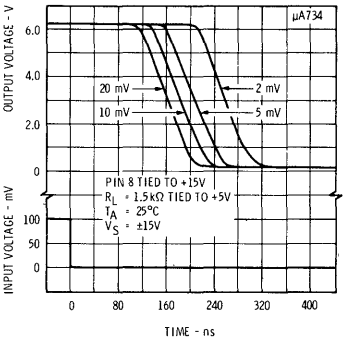
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



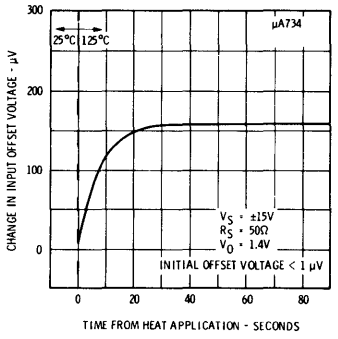
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



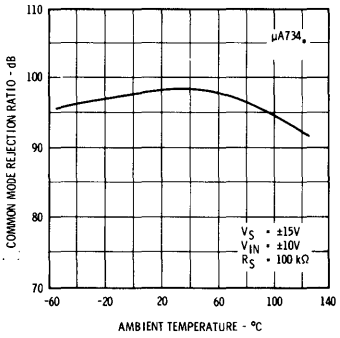
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



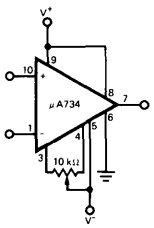
THERMAL RESPONSE OF INPUT OFFSET VOLTAGE TO STEP CHANGE OF CASE TEMPERATURE



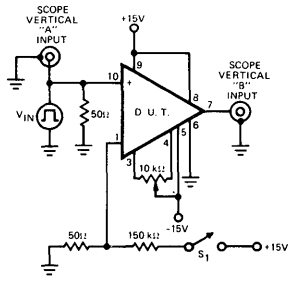
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



OFFSET NULL CIRCUIT TO-100 PIN NUMBERS



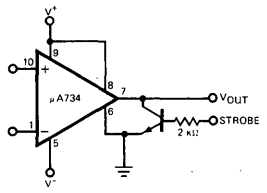
A. C. TEST CIRCUIT



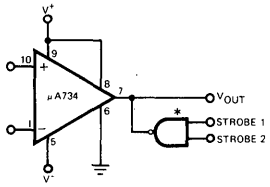
V_{IN} = -100 mV, 100 kHz

TYPICAL APPLICATIONS (Note 2)

STROBE CIRCUITRY

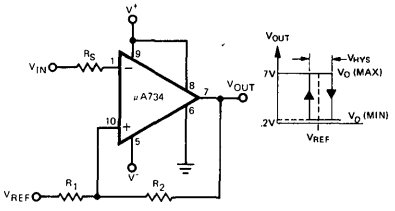


ALTERNATE STROBE CIRCUITRY



* 1/2 9944

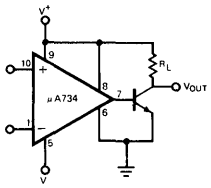
LEVEL DETECTOR WITH HYSTERESIS



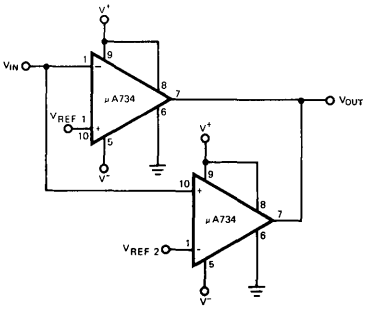
$$R_S = \frac{R_1 R_2}{R_1 + R_2} \quad \text{FOR MINIMUM OFFSET}$$

$$V_{HYS} = \frac{R_1 [V_{O\,MAX} - V_{O\,MIN}]}{R_1 + R_2}$$

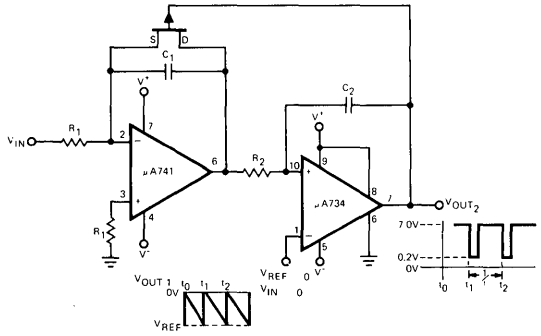
HIGH POWER OUTPUT CIRCUITS



PRECISION DUAL LIMIT GO-NO GO TESTER

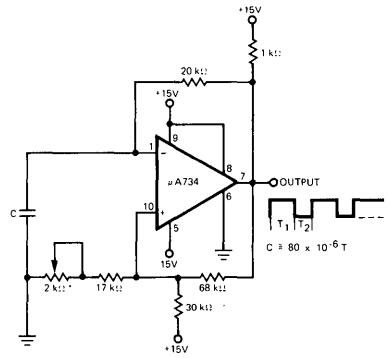


VOLTAGE CONTROLLED OSCILLATOR



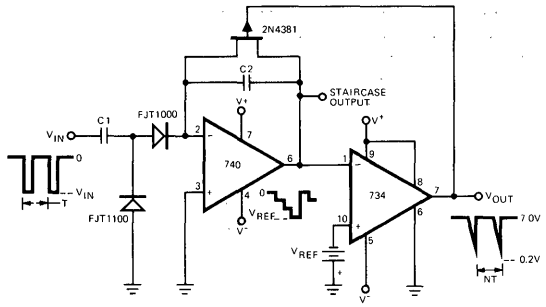
$$f = \frac{V_{IN}}{|V_{REF}| R_1 C_1} \qquad R_2 C_2 > \frac{|V_{REF}| C_1}{I_{DSS}}$$

FREE RUNNING OSCILLATOR



* Adjusts $\frac{T_1}{T_2}$

FREQUENCY DIVIDER & STAIRCASE GENERATOR

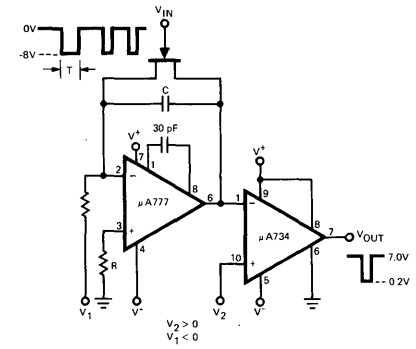


$$|V_{REF}| = 2V_D + N\left[3.5T + 2V_D - \frac{C_1 V_{IN}}{C_2}\right]$$

T In Seconds

V_D for FJT 1000 ≈ 0.31V

PULSE WIDTH DISCRIMINATOR

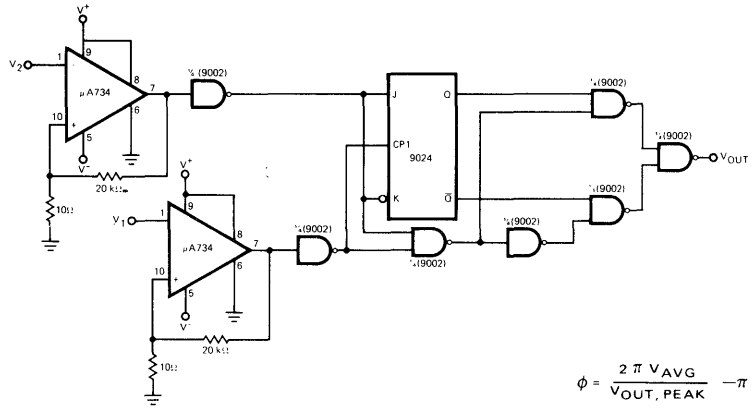


V_{OUT} Pulse Appears

Whenever $T > \frac{R C V_2}{|V_1|}$

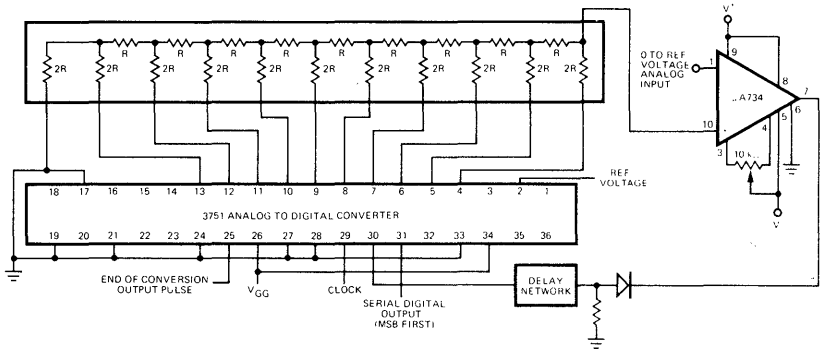
TYPICAL APPLICATIONS (Note 2)

PHASE METER



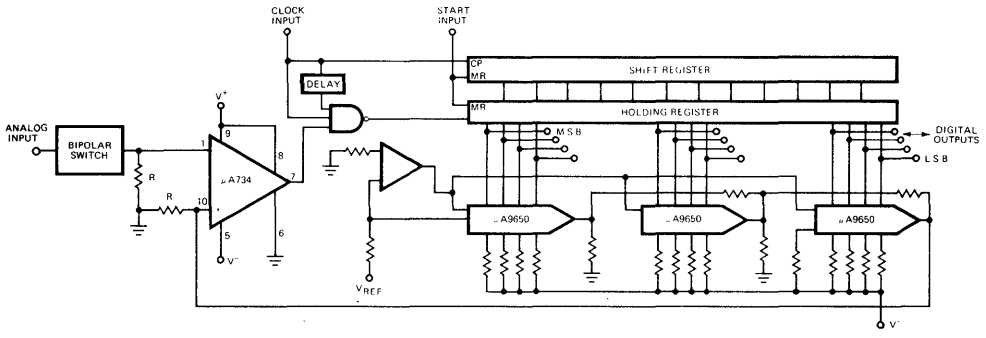
$$\phi = \frac{2\pi V_{AVG}}{V_{OUT,PEAK}} - \pi$$

12 BIT A/D CONVERTER



NO. OF BITS	R VALUE
8	12.5kΩ
9	25kΩ
10	50kΩ
12	200kΩ

12 BIT A/D CONVERTER



μA739

DUAL LOW-NOISE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA739 consists of two identical operational amplifiers constructed on a single silicon chip using the Fairchild Planar* epitaxial process. These low-noise, high-gain amplifiers exhibit extremely stable operating characteristics over a wide range of supply voltage and temperatures. The device is intended for a variety of applications requiring two high performance operational amplifiers.

- **SINGLE OR DUAL SUPPLY OPERATION**
- **LOW NOISE FIGURE, 2.0 dB**
- **HIGH GAIN, 20,000 V/V**
- **LARGE COMMON MODE RANGE, ±11 V**
- **EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE**
- **NO LATCH-UP**
- **OUTPUT SHORT CIRCUIT PROTECTED**

TYPICAL APPLICATIONS

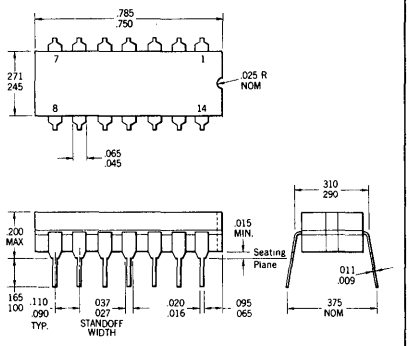
- **DUAL OPERATIONAL AMPLIFIER**
- **PHONO AND TAPE STEREO PREAMPLIFIER**
- **TV REMOTE CONTROL RECEIVER**
- **DUAL COMPARATOR**
- **SENSE AMPLIFIER**
- **OSCILLATOR**
- **ACTIVE FILTER**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	670 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	−55°C to +125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	260°C
Output Short-Circuit Duration, $T_A = 25°C$ (Note 3)	30 seconds

PHYSICAL DIMENSIONS

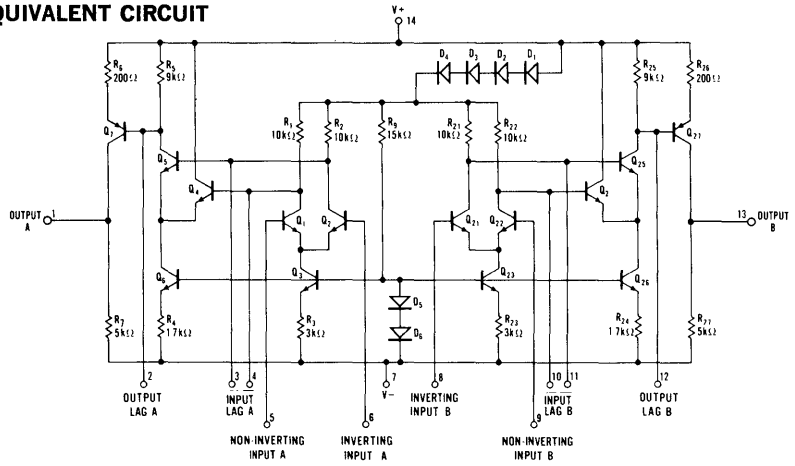
In accordance with JEDEC (TO-116) outline
14 Lead Dual In-Line



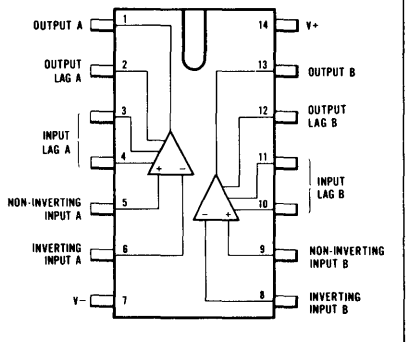
NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead.
Leads are gold-plated kovar
Package weight is 0.9 gram

ORDER PART NO. U6A7739393

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



Notes on following page.

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $R_L = 50$ kΩ to Pin 7, $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.0	6.0	mV
Input Offset Current			50	1000	nA
Input Bias Current			300	2000	nA
Input Resistance		37	150		kΩ
Large-Signal Voltage Gain	$V_{OUT} = \pm 5.0$ V	6500	20,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Output Resistance	f = 1.0 kHz		5.0		kΩ
Input Voltage Range		±10	±11		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		50		μV/V
Power Consumption	$V_{OUT} = 0$		270	420	mW
Supply Current	$V_{OUT} = 0$		9.0	14	mA
Broadband Noise Figure	$R_S = 5.0$kΩ, BW = 10 Hz to 10 kHz		2.0		dB
Turn On Delay (See Figure 1)	Open Loop, $V_{IN} = \pm 20$ mV		0.2		μs
Turn Off Delay (See Figure 1)	Open Loop, $V_{IN} = \pm 20$ mV		0.3		μs
Slew Rate (unity gain) (See Figure 2)	$C_1 = 0.1\ \mu$F, $R_1 = 4.7\ \Omega$		1.0		V/μs
Channel Separation (See Figure 3)	$R_S \leq 10$ kΩ, f = 10 kHz		140		dB
The following specifications apply for $V_S = \pm 4.0$ V, $T_A = 25°C$					
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.0	6.0	mV
Input Offset Current			50	1000	nA
Input Bias Current			300		nA
Supply Current	$V_{OUT} = 0$		2.5		mA
Power Consumption	$V_{OUT} = 0$		20		mW
Large-Signal Voltage Gain	$V_{OUT} = \pm 1.0$ V	2500	15,000		V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V

NOTES:
(1) Rating applies at ambient temperature below 70°C.
(2) For supply voltages less than ± 15 V, the absolute maximum input voltage is equal to the supply voltage.
(3) Short circuit may be to ground or either supply.

PULSE RESPONSE WAVEFORMS

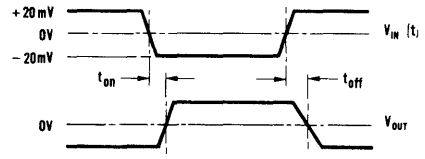


Figure 1

FREQUENCY RESPONSE TEST CIRCUIT

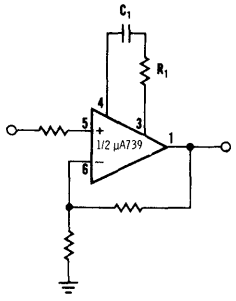


Figure 2

CHANNEL SEPARATION TEST CIRCUIT

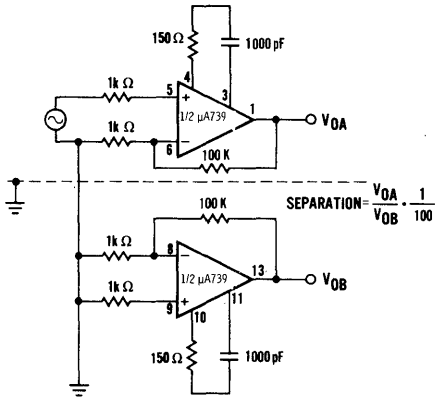
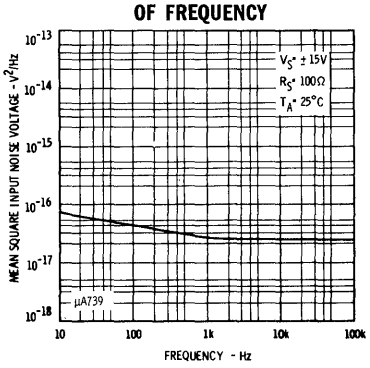


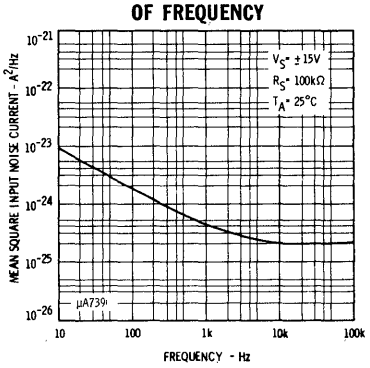
Figure 3

TYPICAL PERFORMANCE CURVES

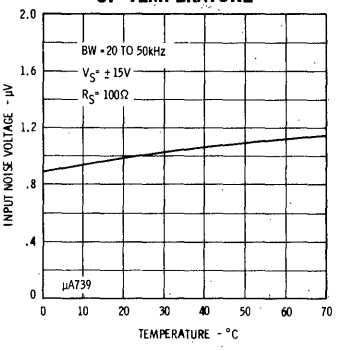
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



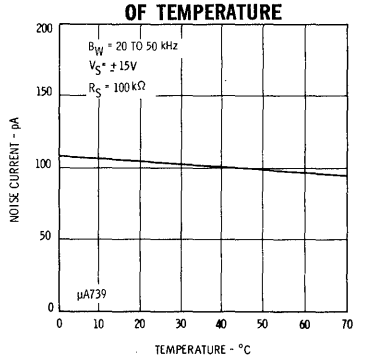
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



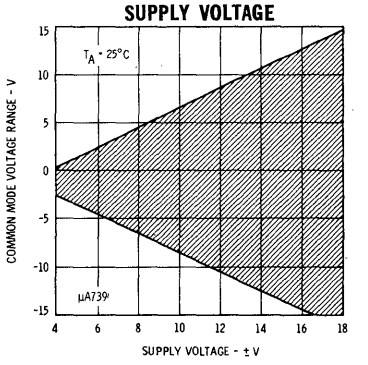
WIDE BAND INPUT NOISE VOLTAGE AS A FUNCTION OF TEMPERATURE



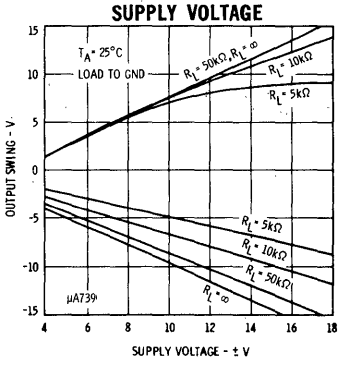
WIDE BAND INPUT NOISE CURRENT AS A FUNCTION OF TEMPERATURE



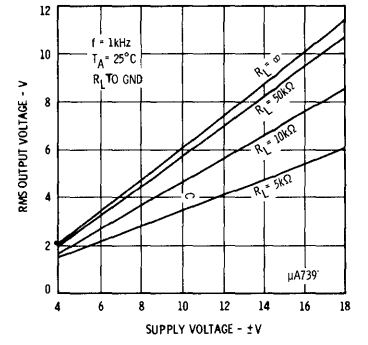
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



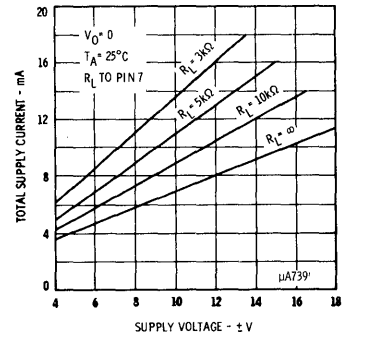
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



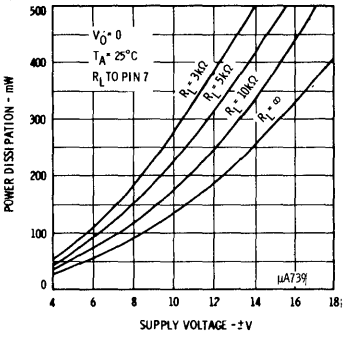
OUTPUT CAPABILITY AS A FUNCTION OF SUPPLY VOLTAGE



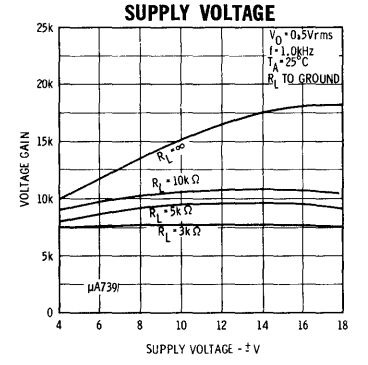
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



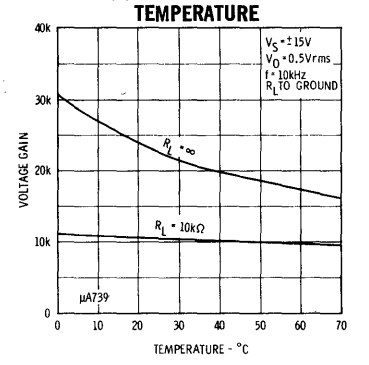
TOTAL POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE AND LOAD



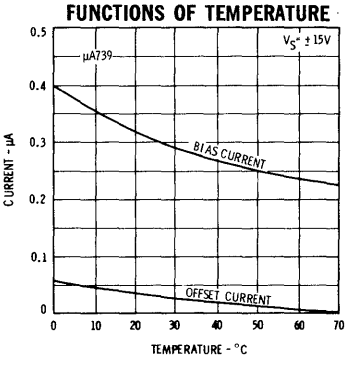
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE

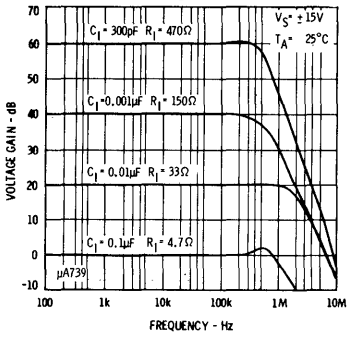


INPUT OFFSET CURRENT AND BIAS CURRENT AS FUNCTIONS OF TEMPERATURE

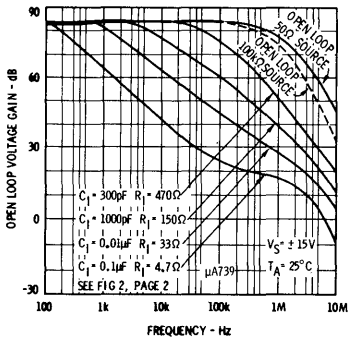


TYPICAL PERFORMANCE CURVES

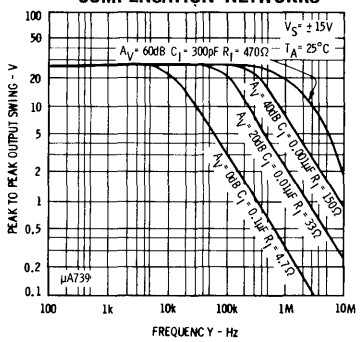
CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY



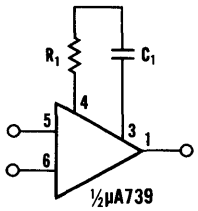
OPEN LOOP FREQUENCY RESPONSE USING RECOMMENDED COMPENSATION NETWORKS



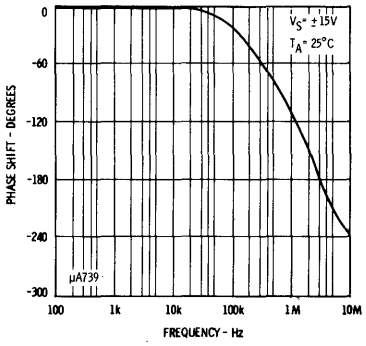
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



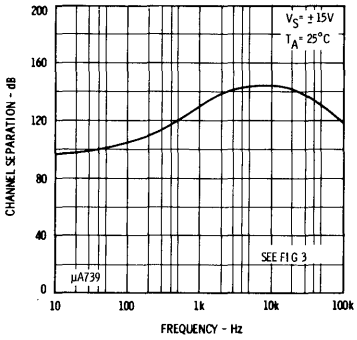
FREQUENCY COMPENSATION NETWORK



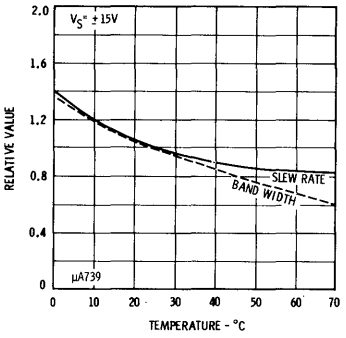
OPEN LOOP PHASE SHIFT WITHOUT COMPENSATION



CHANNEL SEPARATION AS A FUNCTION OF FREQUENCY

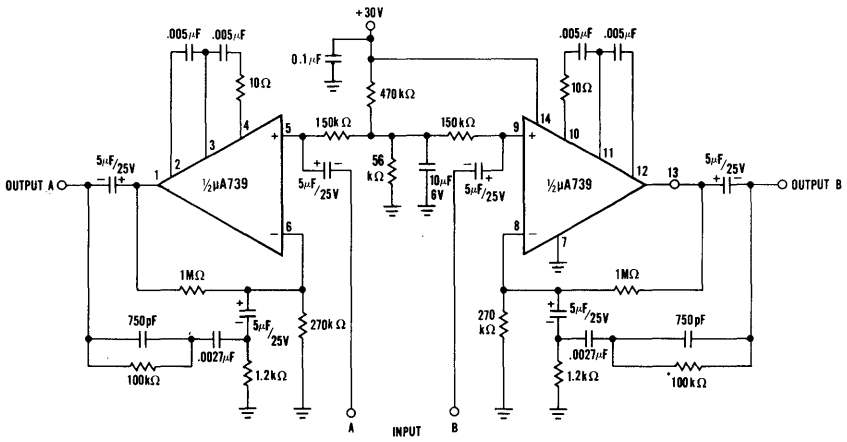


CHANGE OF A.C. CHARACTERISTICS WITH TEMPERATURE



TYPICAL APPLICATION

STEREO PHONO PREAMPLIFIER—RIAA EQUALIZED



TYPICAL PERFORMANCE

Gain 40 dB at 1 kHz, RIAA equalized
Input overload point, 80 mV rms
Noise level, 2μV referred to input
Signal to noise ratio, 74 dB below 10 mV
Channel separation @ 1 kHz, 80 dB

μA740

FET INPUT OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

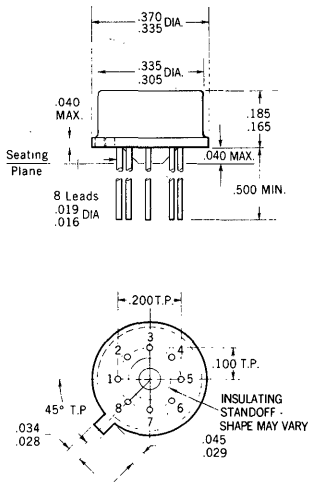
GENERAL DESCRIPTION — The μA740 is a high performance FET input operational amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications where very high input impedance is required and features very low input offset current and very low input bias current. High slew rate, high common mode voltage range and absence of "latch up" make the μA740 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in active filters, integrators, summing amplifiers, sample and holds, transducer amplifiers, and other general feedback applications. The μA740 is short circuit protected and has the same pin configuration as the popular μA741 operational amplifier. No external components for frequency compensation are required as the internal 6 dB/octave roll-off insures stability in closed loop applications.

- **HIGH INPUT IMPEDANCE . . . 1,000,000 MΩ**
- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **NO LATCH UP**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage between Offset Null and V+	±0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (312 Grade)	−55°C to +125°C
Commercial (393 Grade)	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

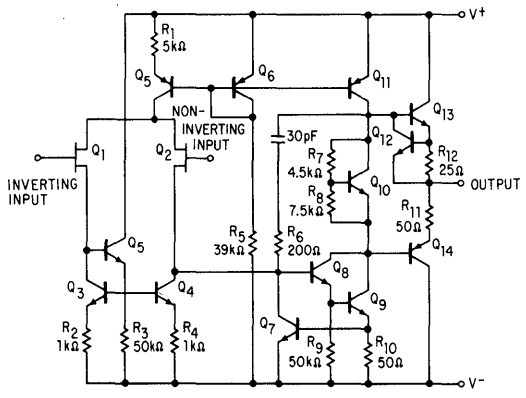
PHYSICAL DIMENSIONS
in accordance with JEDEC (TO-99) outline



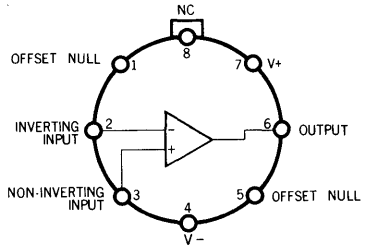
NOTES:
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NOS. U5B7740312
U5B7740393

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



NOTE: PIN 4 CONNECTED TO CASE

Notes on following pages.

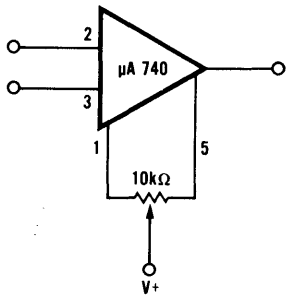
*Planar is a patented Fairchild process.

312 GRADE

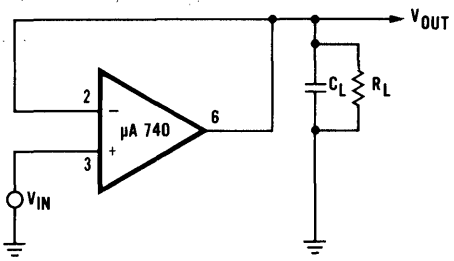
ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_C = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 100$ kΩ		10	20	mV
Input Offset Current			40		pA
Input Current (either input)			100	200	pA
Input Resistance			1,000,000		MΩ
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	50,000	1,000,000		
Output Resistance			75		Ω
Output Short-Circuit Current			20		mA
Common Mode Rejection Ratio		64	80		dB
Supply Voltage Rejection Ratio			70	300	μV/V
Supply Current			4.2	5.2	mA
Power Consumption			126	156	mW
Slew Rate			6.0		V/μs
Unity Gain Bandwidth			3.0		MHz
Transient Response (Unity Gain)	$C_L \leq 100$ pF, $R_L = 2$ kΩ, $V_{in} = 100$ mV				
Risetime			110		ns
Overshoot			10	20	%
The following specifications apply for $T_C = -55°C$ to $+85°C$:					
Input Voltage Range		±10		±12	V
Large Signal Voltage Gain		25,000			
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Input Offset Voltage	$R_S \leq 100$ kΩ		15	30	mV
Input Offset Current	$T_A = -55°C$		185		pA
	$T_A = +85°C$		30		pA
Input Current (either input)	$T_A = -55°C$			200	pA
	$T_A = +85°C$		2.5	4.0	nA

VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



393 GRADE

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_C = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 100$ kΩ		30		mV
Input Offset Current			60		pA
Input Current (either input)			0.1	2.0	nA
Input Resistance			1,000,000		MΩ
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V		1,000,000		
Output Resistance			75		Ω
Output Short-Circuit Current			20		mA
Supply Current			4.2	8.0	mA
Power Consumption			126	240	mW
Slew Rate			6.0		V/μs
Unity Gain Bandwidth			1.0		MHz
Transient Response (Unity Gain)	$C_L \leq 100$ pF, $R_L = 2$ kΩ, $V_{in} = 100$ mV				
Risetime			300		ns
Overshoot			10		%
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Voltage Range			±12		V
Common Mode Rejection Ratio			80		dB
Supply Voltage Rejection Ratio			70		μV/V
Large Signal Voltage Gain			500,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Input Offset Voltage			30		mV
Input Offset Current			60		pA
Input Current (either input)			1.1	10	nA

NOTES:
(1) Rating applies for ambient temperature to +70°C; derate linearly at 6.3 mW/°C for ambient temperatures above +70°C.
(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
(3) Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

μA741

FREQUENCY-COMPENSATED OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

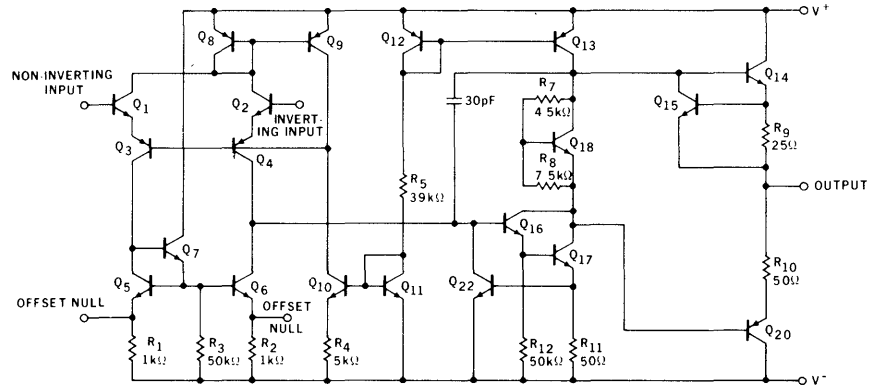
GENERAL DESCRIPTION — The μA741 is a high performance monolithic operational amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the μA741 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications.

- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

ABSOLUTE MAXIMUM RATINGS

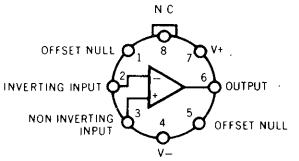
Supply Voltage	
Military (312 Grade)	±22 V
Commercial (393 Grade)	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Ceramic DIP	670 mW
Silicone DIP	340 mW
Mini DIP	310 mW
Flatpak	570 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, Ceramic DIP, and Flatpak	−65°C to +150°C
Mini DIP and Silicon DIP	−55°C to +125°C
Operating Temperature Range	
Military (312 Grade)	−55°C to +125°C
Commercial (393 Grade)	0°C to + 70°C
Lead Temperature (Soldering)	
Metal Can, Ceramic DIP and Flatpak (60 seconds)	300°C
Mini DIP and Silicone DIP (10 seconds)	260°C
Output Short Circuit Duration (Note 3)	Indefinite

EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS
(TOP VIEW)

8 LEAD METAL CAN

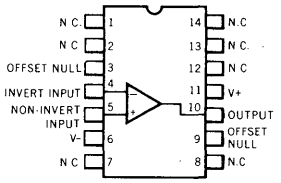


NOTE PIN 4 CONNECTED TO CASE

ORDER PART NOS.

U5B7741312
U5B7741393

14 LEAD DIP



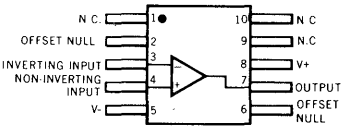
FOR CERAMIC DIP ORDER PART NOS.

U6A7741312
U6A7741393

FOR SILICONE DIP ORDER PART NO. :

U9A7741393

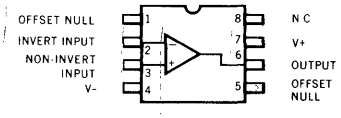
FLATPACK



ORDER PART NO.

U3F7741312

MINIDIP



ORDER PART NO.

U9T7741393

Notes on following pages.

*Planar is a patented Fairchild process.

312 GRADE

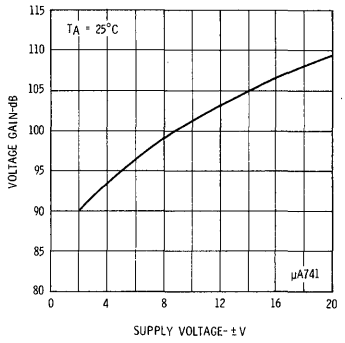
ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			1.4		pF
Offset Voltage Adjustment Range			±15		mV
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	50,000	200,000		
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.7	2.8	mA
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate	$R_L \geq 2$ kΩ		0.5		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current	$T_A = +125°C$		7.0	200	nA
	$T_A = -55°C$		85	500	nA
Input Bias Current	$T_A = +125°C$		0.03	0.5	μA
	$T_A = -55°C$		0.3	1.5	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	25,000			
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Supply Current	$T_A = +125°C$		1.5	2.5	mA
	$T_A = -55°C$		2.0	3.3	mA
Power Consumption	$T_A = +125°C$		45	75	mW
	$T_A = -55°C$		60	100	mW

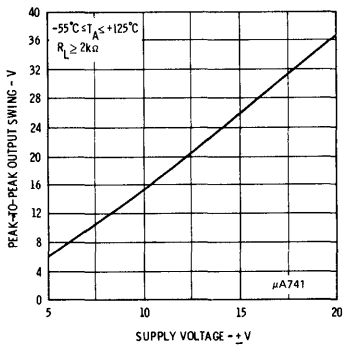
TYPICAL PERFORMANCE CURVES

312 GRADE

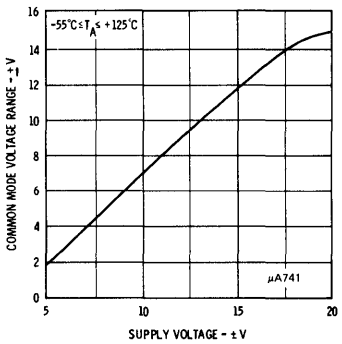
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



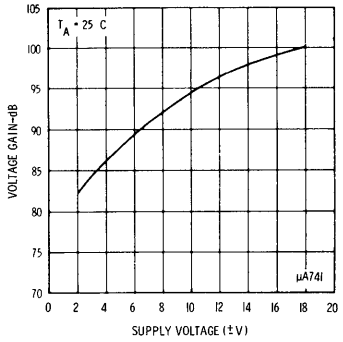
393 GRADE

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

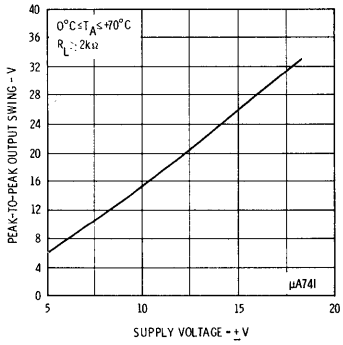
PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			1.4		pF
Offset Voltage Adjustment Range			±15		mV
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	20,000	200,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.7	2.8	mA
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate	$R_L \geq 2$ kΩ		0.5		V/μs
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage				7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	15,000			
Output Voltage Swing	$R_L \geq 2$ kΩ	±10	±13		V

TYPICAL PERFORMANCE CURVES
393 GRADE

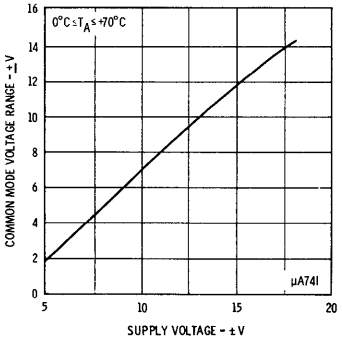
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

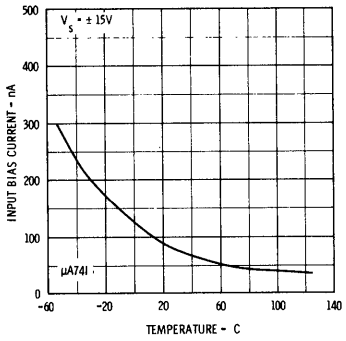


NOTES

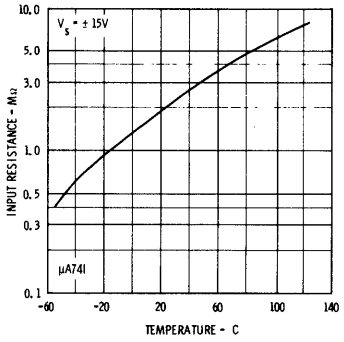
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can, 8.3 mW/°C for the Ceramic DIP, 6.3 mW/°C for the Silicone DIP, 5.6 mW/°C for the Mini DIP and 7.1 mW/°C for the Flatpak.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or 75°C ambient temperature.

TYPICAL PERFORMANCE CURVES (312 GRADE)

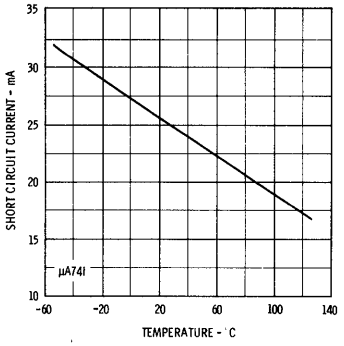
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



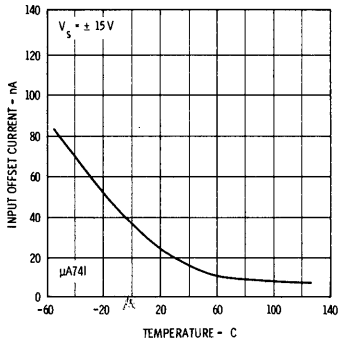
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



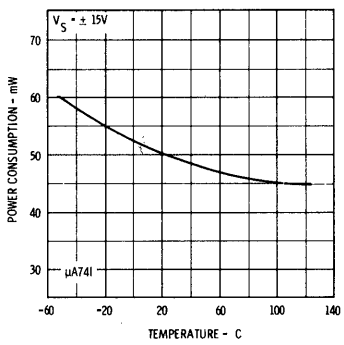
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



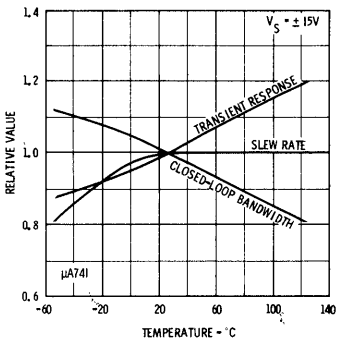
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

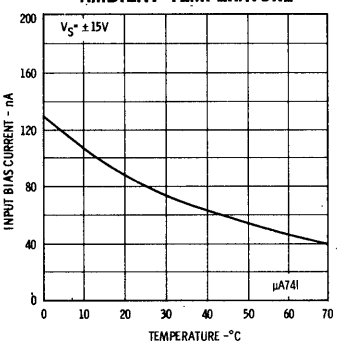


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

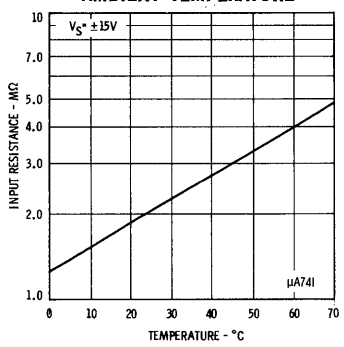


(393 GRADE)

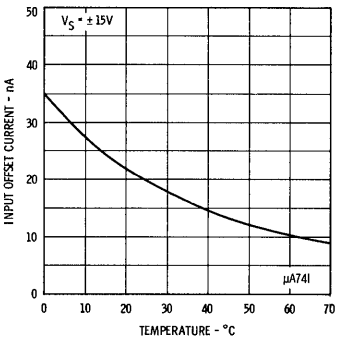
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



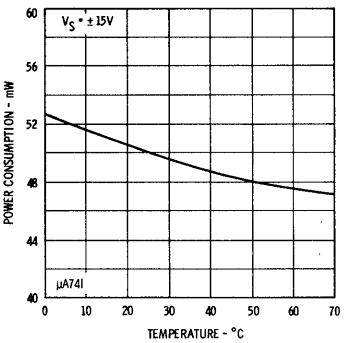
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



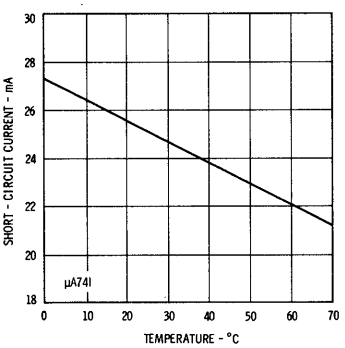
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



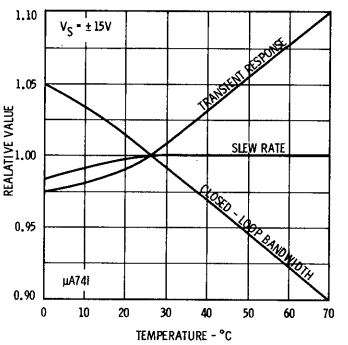
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

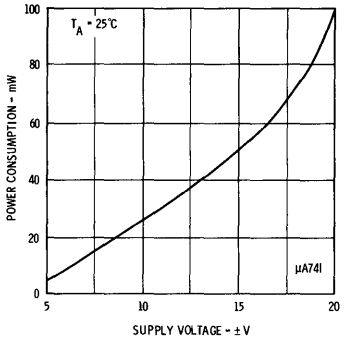


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

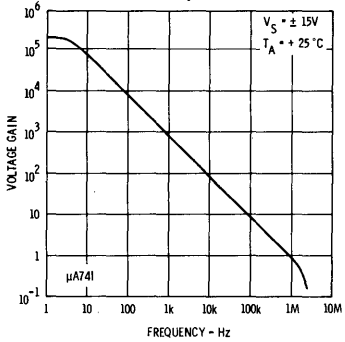


TYPICAL PERFORMANCE CURVES (312 AND 393 GRADES)

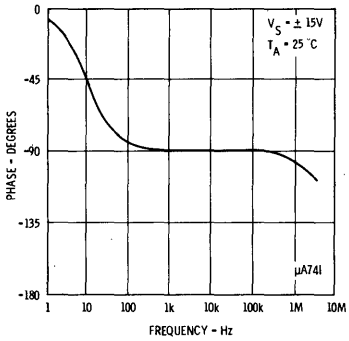
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



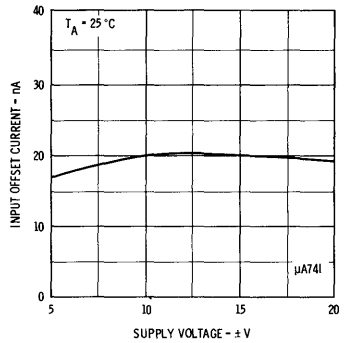
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



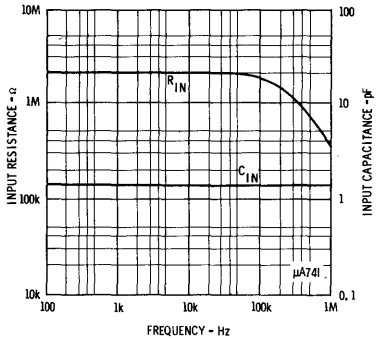
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



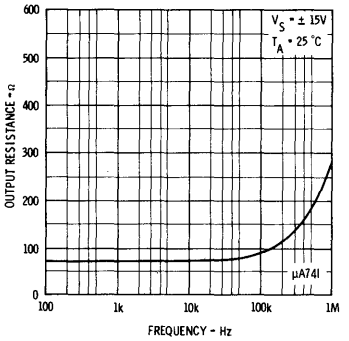
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



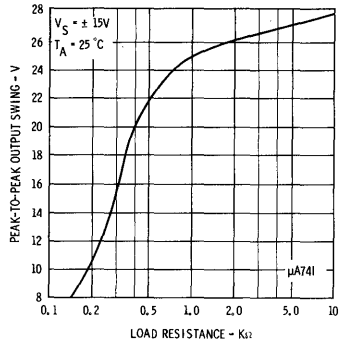
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



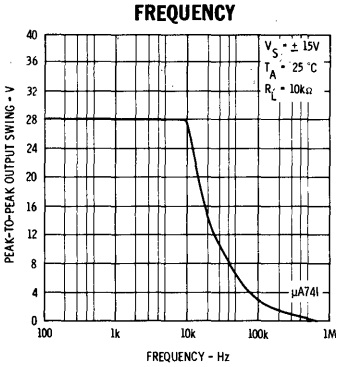
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



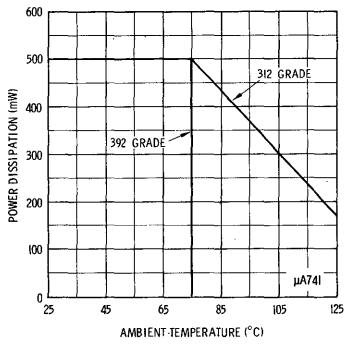
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



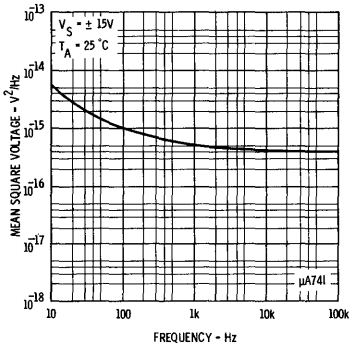
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



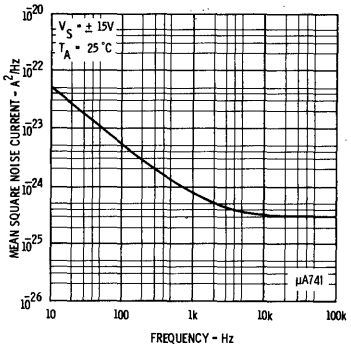
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



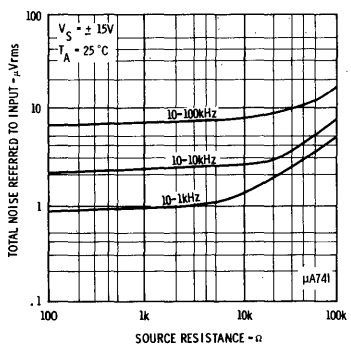
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



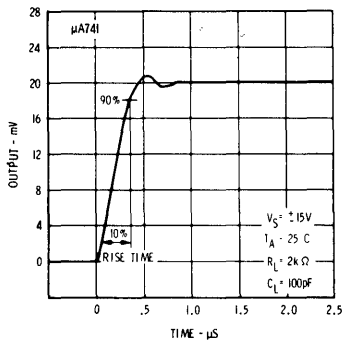
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



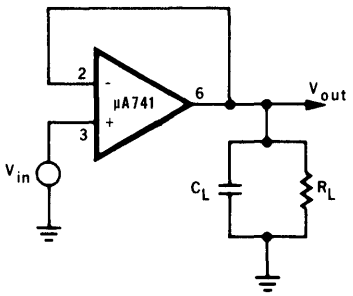
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



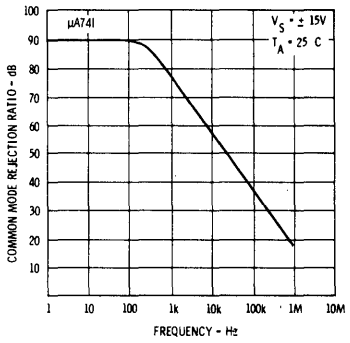
TRANSIENT RESPONSE



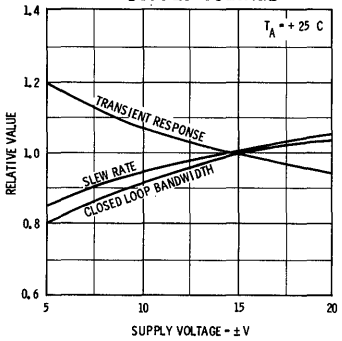
TRANSIENT RESPONSE TEST CIRCUIT



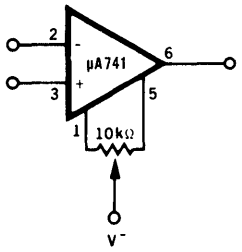
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



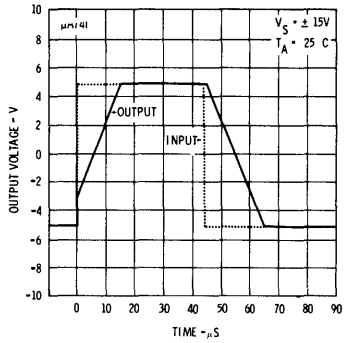
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE OFFSET NULL CIRCUIT

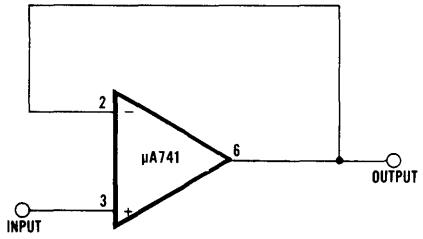


VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



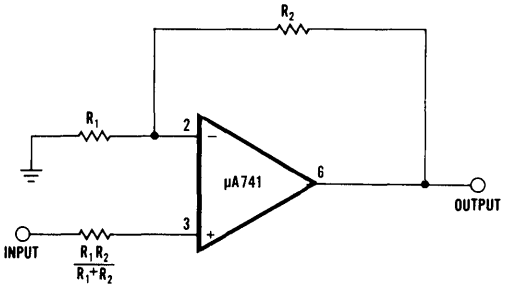
TYPICAL APPLICATIONS

UNITY-GAIN VOLTAGE FOLLOWER



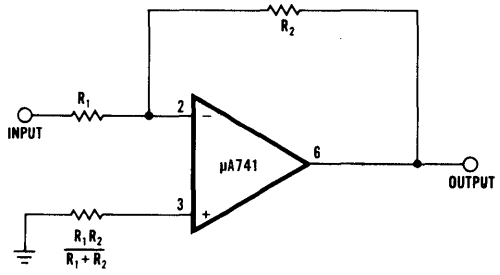
R_{IN} = 400 MΩ
C_{IN} = 1 pF
R_{out} << 1 Ω
B.W. = 1 MHz

NON-INVERTING AMPLIFIER



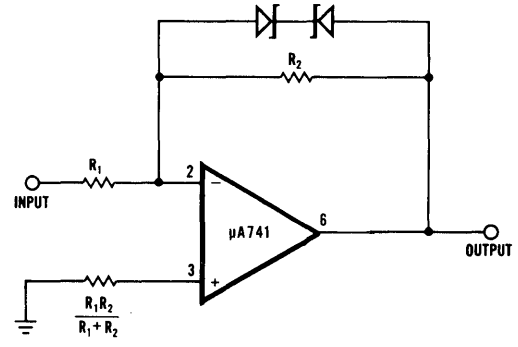
GAIN	R_1	R_2	B.W.	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

INVERTING AMPLIFIER



GAIN	R_1	R_2	B.W.	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

CLIPPING AMPLIFIER

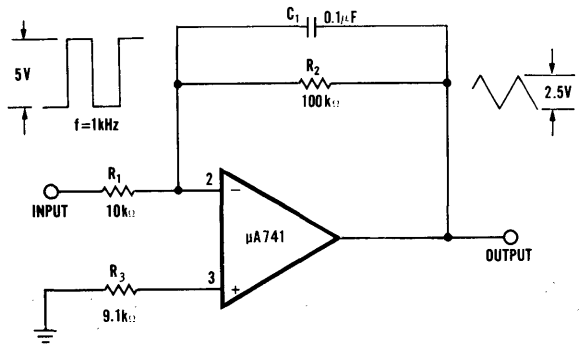


$$\frac{E_{out}}{E_{IN}} = \frac{R_2}{R_1} \text{ if } |E_{out}| \leq V_Z + 0.7\ V$$

where V_Z = Zener breakdown voltage

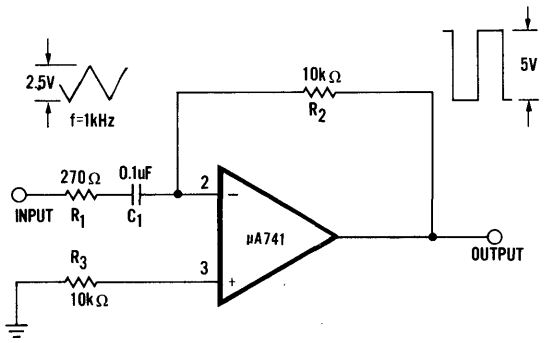
TYPICAL APPLICATIONS

SIMPLE INTEGRATOR



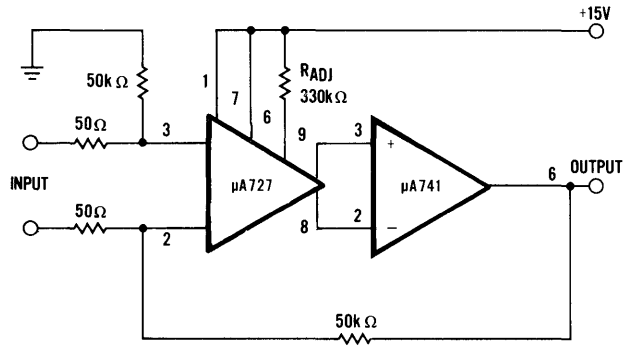
$$E_{out} = -\frac{1}{R_1C_1}\int E_{IN}dt$$

SIMPLE DIFFERENTIATOR



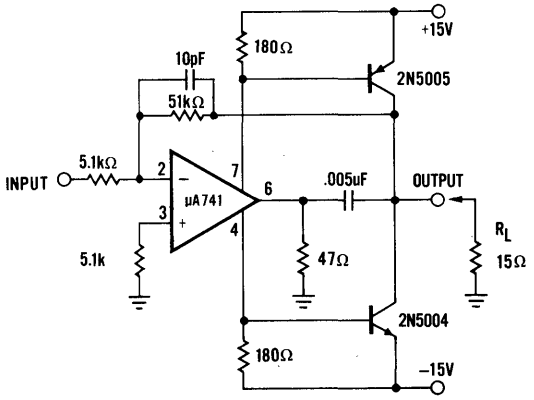
$$E_{out} = -R_2C_1\frac{dE_{IN}}{dt}$$

LOW DRIFT LOW NOISE AMPLIFIER

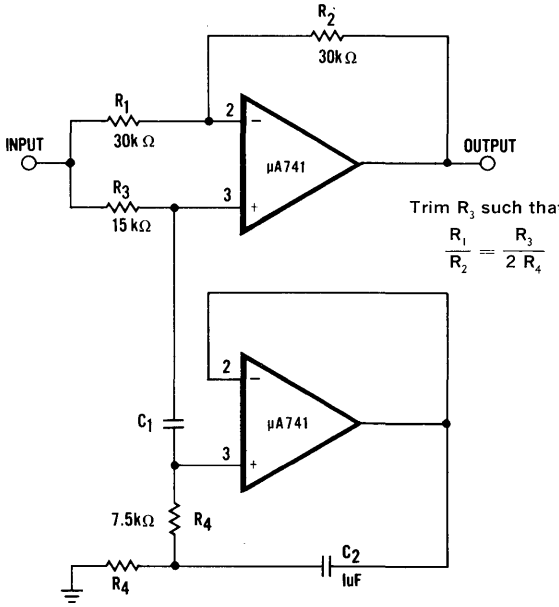


Voltage Gain = 10^3
Input Offset Voltage Drift = 0.6 μV/°C
Input Offset Current Drift = 2.0 pA/°C

HIGH SLEW RATE POWER AMPLIFIER



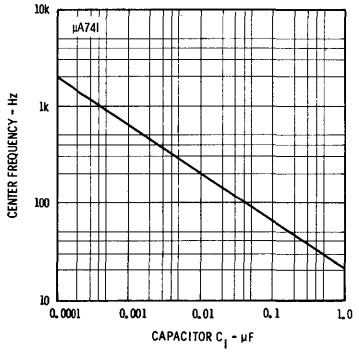
NOTCH FILTER USING THE μA741 AS A GYRATOR



Trim R_3 such that

$$\frac{R_1}{R_2} = \frac{R_3}{2\,R_4}$$

NOTCH FREQUENCY AS A FUNCTION OF C_1



μA742

ZERO CROSSING AC TRIGGER-TRIGAC

FAIRCHILD LINEAR INTEGRATED CIRCUITS

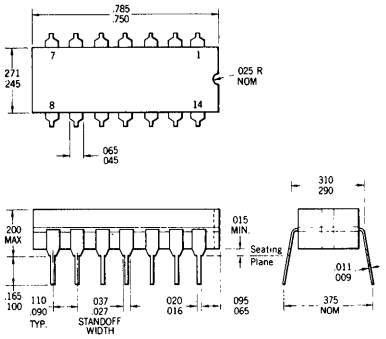
GENERAL DESCRIPTION — The μA742 is a Zero Crossing AC Trigger - TRIGAC which is constructed on a single chip utilizing the Fairchild Planar* Epitaxial Process. It is intended for use in AC power control circuits for operation directly off the AC line or with a separate AC or DC power supply. The TRIGAC functions as a threshold detector and a driver for triacs and SCR's; as a threshold detector, it senses level changes at the inputs and as a driver it supplies high energy pulses for thyristor triggering. The trigger pulses occur at the zero crossing of the load current and therefore minimize RFI generation for either resistive or inductive loads.

- **DESIGNED FOR APPLICATIONS IN 60 Hz AND 400 Hz AC POWER CONTROL SYSTEMS HAVING RESISTIVE OR INDUCTIVE LOADS**
- **OPERATES DIRECTLY FROM AN AC LINE OR FROM A DC SUPPLY**
- **INPUT COMPATIBLE WITH A WIDE RANGE OF SENSOR IMPEDANCES**
- **BRIDGE SENSING WITH ADJUSTABLE HYSTERESIS SET POINTS**
- **PROVISIONS FOR TIME PROPORTIONING OPERATION**
- **PROVIDES ZERO CROSSING THYRISTOR TRIGGERING FOR MINIMUM RFI**
- **EVEN NUMBER OF CONSECUTIVE HALF-CYCLE TRIGGERING FOR TRIACS AND INVERSE PARALLEL SCR's IN MOST APPLICATIONS**

ABSOLUTE MAXIMUM RATINGS

Peak Current into Supply Terminal (AC Operation)	±30 mA
Continuous Current into Supply Terminal (DC Operation)	20 mA
RMS Current into Sync Input Terminal	15 mA
Current into Switch Terminal	10 mA
Power Dissipation	670 mW
Voltage at (+) or (−) Input Terminal	(Note 1)
Differential Voltage between (+) and (−) Input Terminals	±7 V
Current into Clamp Terminal (Clamp ON)	20 mA
Voltage at Clamp Terminal (Clamp OFF)	20 V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 second time limit)	260°C
Trigger Output Short-Circuit Duration (Note 2)	Continuous

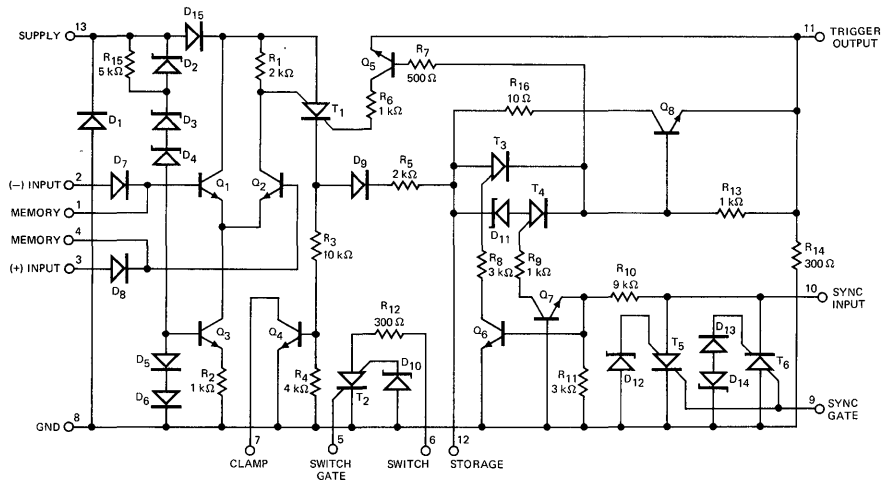
PHYSICAL DIMENSIONS
(Typical Dual In-Line Package)



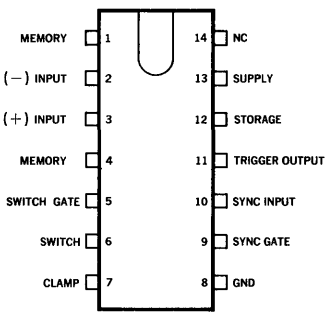
NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin plated kovar
Package weight is 2.0 grams

ORDER PART NO. U6A7742393

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



Notes on following page.

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, Voltage Range at the (+) and (−) Input Terminals: 0.15 to 0.75•(V_{Supply}); $V_{(+)Input} - V_{(-)Input} \geq 100$ mV, Test Circuit 1, unless otherwise specified.

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Peak Supply Voltage	S_1 in DC position		20		Volts
	S_1 in AC position, positive half cycles of AC line		20		Volts
	S_1 in AC position, negative half cycle of AC line		−0.7		Volts
Peak Trigger Output Pulse	S_1 in AC position, beginning of positive half cycles		0.9		Amp
	S_1 in AC or DC position, beginning of negative half cycles		1.3		Amp
	S_1 in DC position beginning of positive half cycles		2.2		Amp
Bias Current at (+) and (−) Input Terminals			10		μA
ON Voltage at Clamp Terminal	$I_C = 1$ mA		0.1		Volts
ON Voltage at Switch Terminal	$I_F = 5$ mA		1.0		Volts
ON Voltage at Sync Input Terminal	$I_F = 10$ mA		1.0		Volts
Switching Voltage at Sync Input Terminal			6.0		Volts
Switching Voltage at Switch Terminal			7.0		Volts
Holding Current at Switch Terminal			25		μA
Sync Input Threshold Current for Trigger Output	Beginning of positive half cycles		0.3		mA
	Beginning of negative half cycles		−0.7		mA
Sync Input Threshold Voltage for Trigger Output	Beginning of positive half cycles		2.0		Volts
	Beginning of negative half cycles		−0.7		Volts

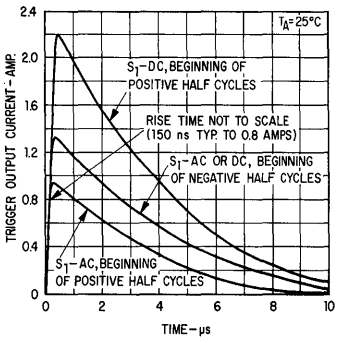
DEFINITIONS

VOLTAGE RANGE: The range of voltage on the (+) or (−) input terminals, which, if exceeded, could cause the TRIGAC to cease functioning.
BIAS CURRENT: The average of the two currents into the (+) and (−) input terminals.

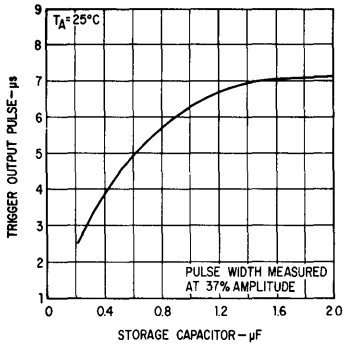
NOTES:
(1) The maximum voltage should not exceed the instantaneous supply voltage of the μA742.
(2) Rating applies for an external storage capacitor having a value of not more than 2μF.

TYPICAL ELECTRICAL CHARACTERISTICS
(TEST CIRCUIT 1 UNLESS OTHERWISE SPECIFIED)

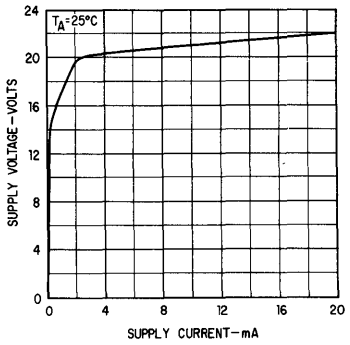
TRIGGER OUTPUT PULSE WAVE FORMS



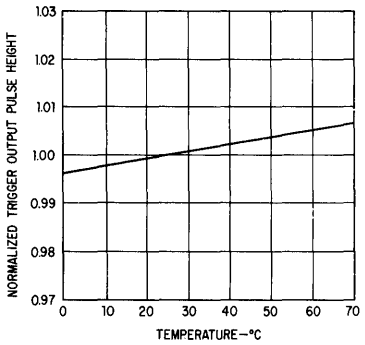
TRIGGER OUTPUT PULSE WIDTH VERSUS STORAGE CAPACITOR



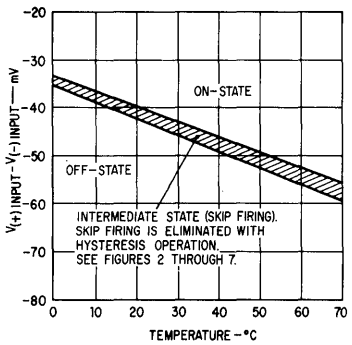
SUPPLY VOLTAGE VERSUS SUPPLY CURRENT



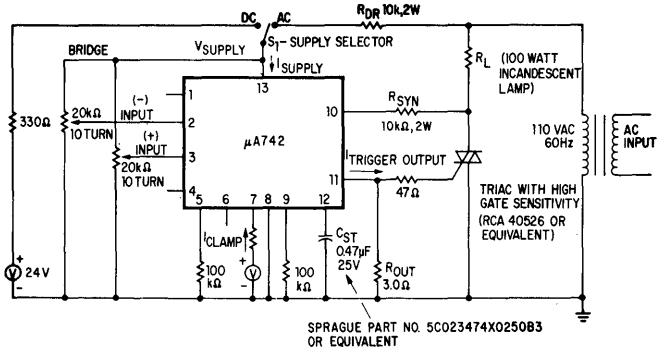
NORMALIZED TRIGGER OUTPUT PULSE HEIGHT VERSUS TEMPERATURE



OPERATING STATE AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE AND TEMPERATURE



μA742 TEST CIRCUIT 1



TYPICAL APPLICATIONS

FIG. 1 — ZERO CROSSING CONTROL CIRCUIT WITHOUT HYSTERESIS

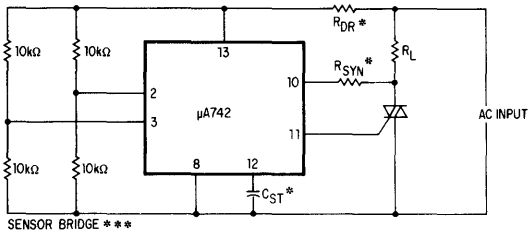


FIG. 2 — ZERO CROSSING CIRCUIT WITH DC SUPPLY

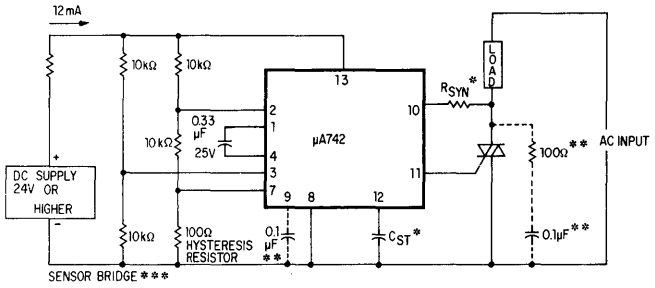


FIG. 3 — ZERO CROSSING CIRCUIT

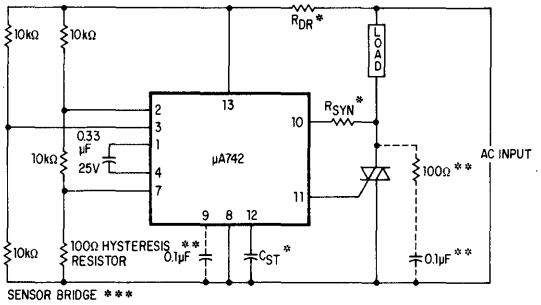


FIG. 4 — SCR FIRING — HALF WAVE

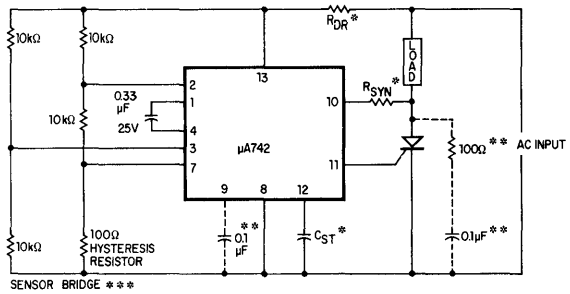


FIG. 5 — INVERSE PARALLEL SCR PAIR FIRING WITH A PULSE TRANSFORMER

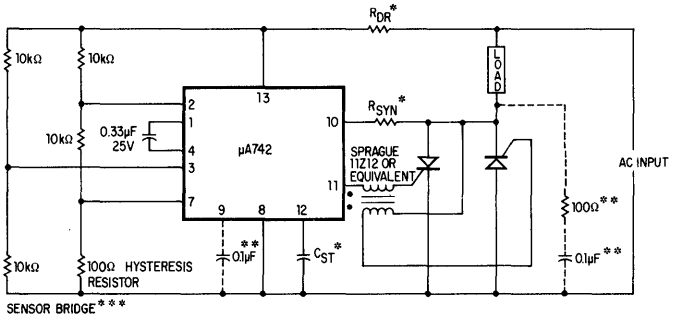


FIG. 6 — INVERSE PARALLEL SCR PAIR FIRING WITH A THIRD SCR

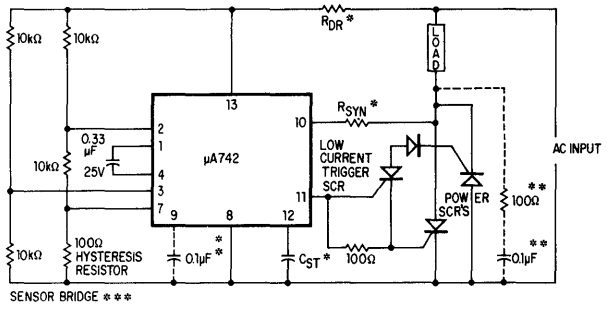
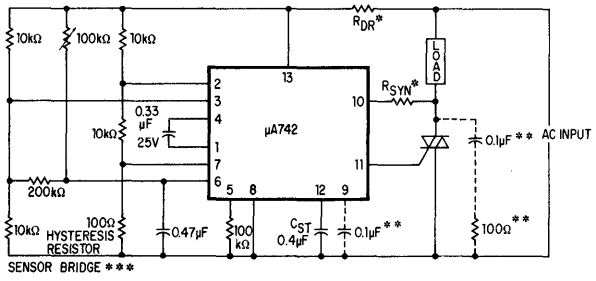


FIG. 7 — ZERO CROSSING WITH PROPORTIONAL CONTROL



*Recommended Values

AC Supply Voltage 60 Hz Volts - RMS	R_{DR}	R_{SYN}	C_{ST}
24	1.0 kΩ	2.2 kΩ	0.47 μF/25 V
110	10 kΩ	10 kΩ	0.47 μF/25 V
220	22 kΩ	22 kΩ	0.47 μF/25 V

FOR SUPPLY VOLTAGE FREQUENCY OF 400 Hz REDUCE C_{ST} TO .047 μF/25 V

**Necessary with inductive loads.

***The sensor resistance will determine the values of the bridge resistors. For the values of R_{DR} shown, the total current into the bridge should not exceed 5 mA at 20 V.

μA746

COLOR TV CHROMA DEMODULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

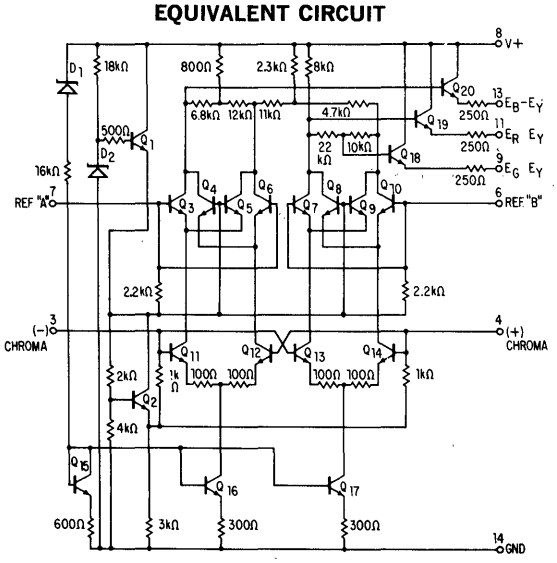
GENERAL DESCRIPTION — The μA746 is a color TV chroma demodulator constructed on a single silicon chip using the Fairchild Planar* epitaxial process. This device demodulates the chroma subcarrier information contained in a color television video signal and provides color-difference signals at the outputs. The low voltage drift of the D.C. output insures excellent performance in direct-coupled chrominance output circuitry.

- **LOW OUTPUT VOLTAGE DRIFT WITH TEMPERATURE**
- **DOUBLY BALANCED DEMODULATION**
- **INTERNAL COLOR-DIFFERENCE MATRIX FOR NTSC COLOR TV**
- **10 VOLT PEAK-TO-PEAK E_B - E_Y OUTPUT**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+28 V
Minimum Load Resistance	3 kΩ
Peak-to-Peak Reference Input Voltage	5.0 V
Peak-to-Peak Chroma Input Voltage	5.0 V
Internal Power Dissipation	
Metal Can	500 mW
Ceramic DIP	670 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	
(5E and 6A Packages)	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	
(5E and 6A Packages)	+300°C

EQUIVALENT CIRCUIT

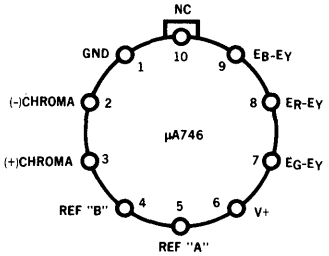


Pin numbers shown for Dual In-Line Package.

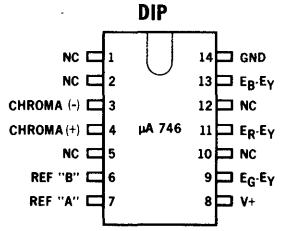
CONNECTION DIAGRAMS

(TOP VIEWS)

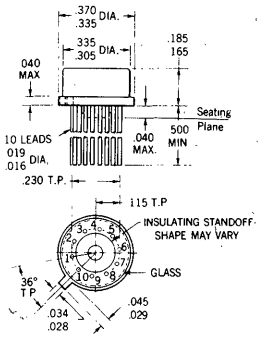
METAL CAN



DIP



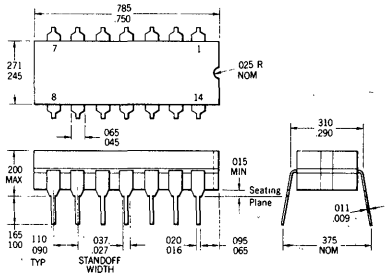
PHYSICAL DIMENSIONS



NOTES:

All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams

ORDER PART NO. U5E7746394



ORDER PART NO. U6A7746394

NOTES:

All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Package weight is 2.0 grams.

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 24$ V, Test Circuit 1 unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$e_C = 0$, $R_L = 1$ MΩ	5.5	9.0	12.5	mA
	$e_C = 0$, $R_L = 1$ MΩ, $T_A = 70°C$		9.0	13.0	mA
	$e_C = 0$	16.5	22	25.5	mA
	$e_C = 0$, $T_A = 70°C$		22		mA
Internal Power Dissipation	$e_C = 0$		340	430	mW
	$e_C = 0$, $T_A = 70°C$		340	445	mW
DC Voltage at any Output Terminal	$e_C = 0$	13.2	14.5	15.8	Volts
	$e_C = 0$, $T_A = 70°C$	13.0	14.5	16.0	Volts
Temperature Coefficient of DC Voltage at any Output Terminal	$e_C = 0$	−5.0	−0.3	+5.0	mV/°C
Absolute Value of DC Difference Voltage between any Two Outputs	$e_C = 0$		0.15	0.6	Volts
DC Voltage at either Reference Terminal	$e_A = e_B = e_C = 0$		5.8		Volts
DC Voltage at either Chroma Terminal	$e_C = 0$		3.2		Volts
Reference Input Resistance	$e_C = 0$		1.7		kΩ
Reference Input Capacitance	$e_C = 0$		6.0		pF
Chroma Input Resistance			0.8		kΩ
Chroma Input Capacitance			5.0		pF
Peak-to-Peak Chroma Input Voltage	$E_B - E_Y = 5$ Vp-p		0.4	0.7	Volts
Peak-to-Peak $E_R - E_Y$ Output Voltage	$E_B - E_Y = 5$ Vp-p	3.5	3.8	4.2	Volts
Peak-to-Peak $E_G - E_Y$ Output Voltage	$E_B - E_Y = 5$ Vp-p	0.75	1.0	1.25	Volts
Maximum Peak-to-Peak $E_B - E_Y$ Output Voltage	$e_C = 1.5$ Vp-p	8.0	10		Volts
$E_B - E_Y$ Demodulation Angle	$E_B - E_Y = 5$ Vp-p		3		Degrees
$E_R - E_Y$ Demodulation Angle	$E_B - E_Y = 5$ Vp-p		109		Degrees
$E_G - E_Y$ Demodulation Angle	$E_B - E_Y = 5$ Vp-p		259		Degrees
$E_R - E_Y$ Demodulation Angle relative to $E_B - E_Y$ Demodulation Angle	$E_B - E_Y = 5$ Vp-p	101	106	111	Degrees
$E_B - E_Y$ Demodulation Angle relative to $E_G - E_Y$ Demodulation Angle	$E_B - E_Y = 5$ Vp-p	96	104	112	Degrees
Highest Peak-to-Peak Demodulator AC Unbalance Voltage at any Output Terminal	$e_C = 0$		0.3	0.8	Volts

DEFINITIONS

Color-Difference Demodulation Angle — A color-difference demodulation angle is defined as the instantaneous phase of the (+) Chroma input signal which produces the most positive voltage at the respective color-difference output with the phase of Reference "A" taken at 3 degrees and the phase of Reference "B" taken at 106 degrees.

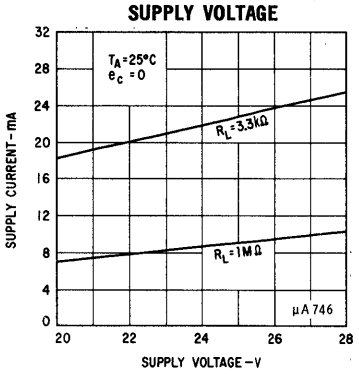
(+) Chroma Input — A composite chroma signal containing the burst at a phase of 180 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (+) Chroma input.

(—) Chroma Input — A composite chroma signal containing the burst at a phase of 0 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (—) Chroma input.

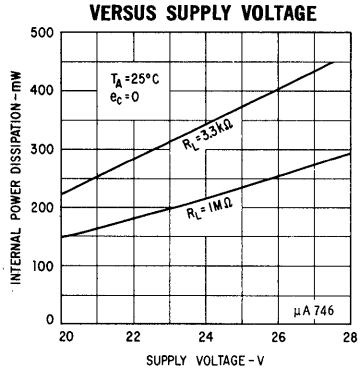
TYPICAL ELECTRICAL CHARACTERISTICS

(TEST CIRCUIT 1 UNLESS OTHERWISE SPECIFIED)

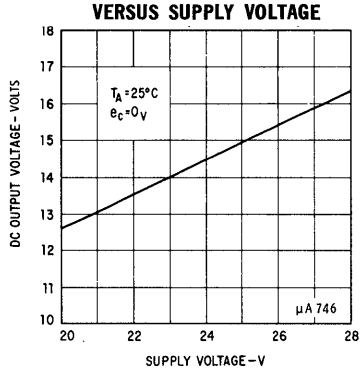
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



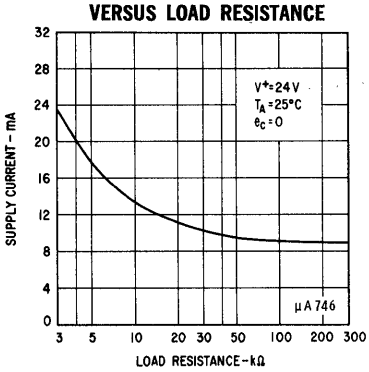
INTERNAL POWER DISSIPATION VERSUS SUPPLY VOLTAGE



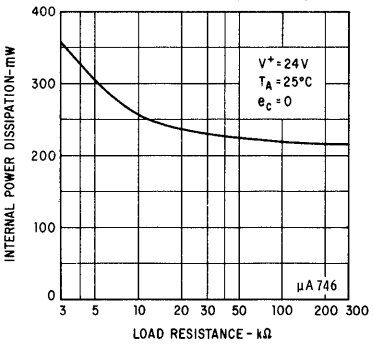
DC VOLTAGE AT ANY OUTPUT VERSUS SUPPLY VOLTAGE



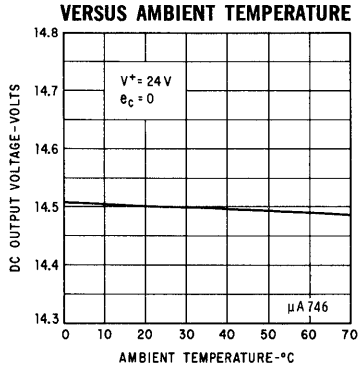
SUPPLY CURRENT VERSUS LOAD RESISTANCE



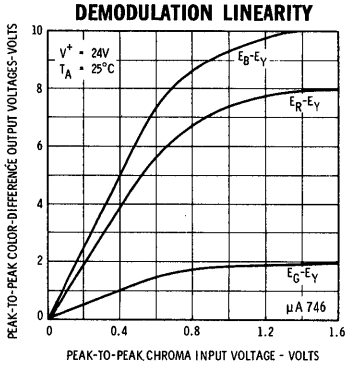
INTERNAL POWER DISSIPATION VERSUS LOAD RESISTANCE



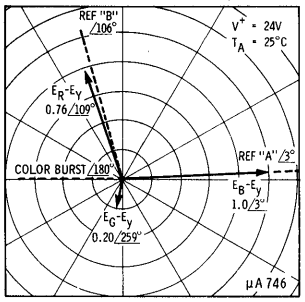
DC VOLTAGE AT ANY OUTPUT VERSUS AMBIENT TEMPERATURE



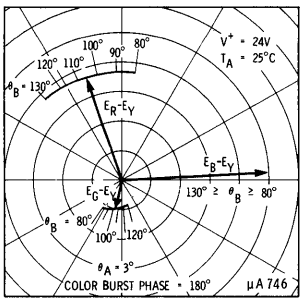
DEMODULATION LINEARITY



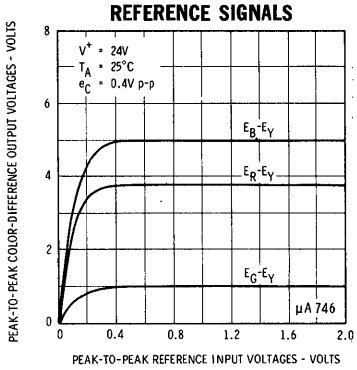
DEMODULATION ANGLES AND RELATIVE GAINS



DEMODULATION SENSITIVITY TO RELATIVE PHASING OF REFERENCE SIGNALS



DEMODULATION SENSITIVITY TO AMPLITUDE OF REFERENCE SIGNALS

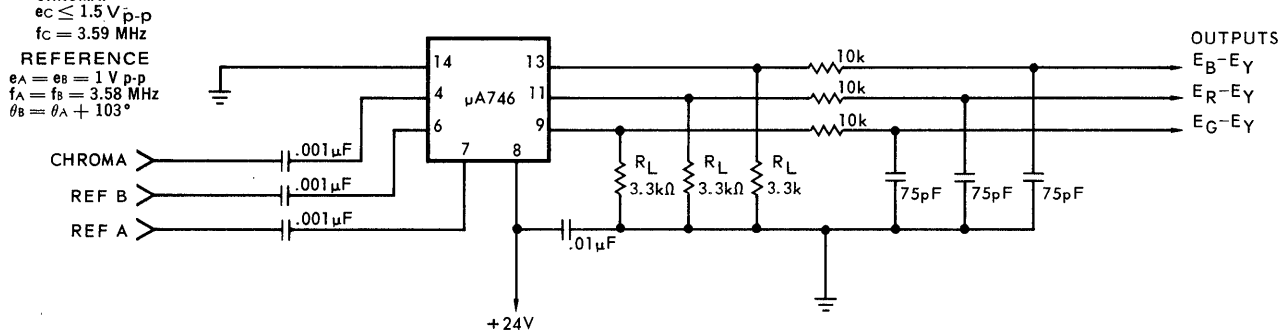


INPUTS

CHROMA:
$e_C \leq 1.5\ V_{p\text{-}p}$
$f_C = 3.59$ MHz

REFERENCE
$e_A = e_B = 1$ V p-p
$f_A = f_B = 3.58$ MHz
$\theta_B = \theta_A + 103°$

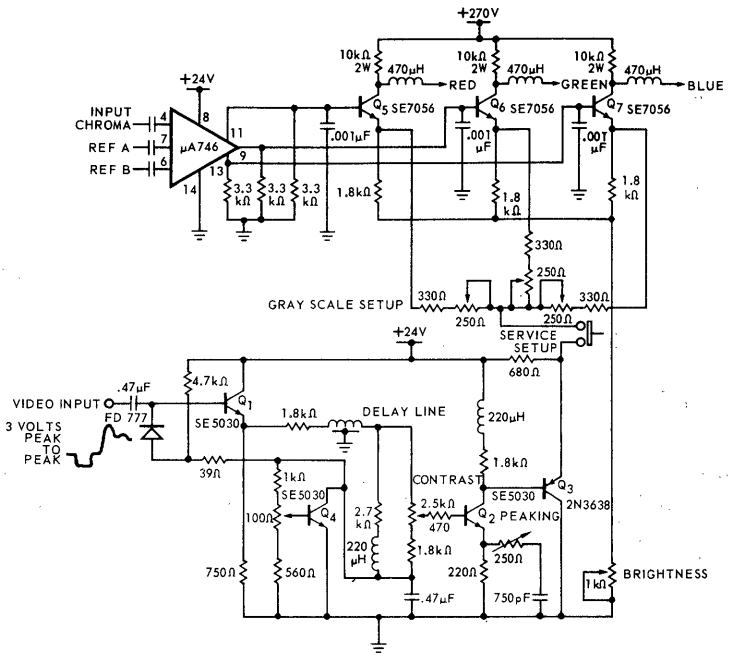
TEST CIRCUIT 1



Pin numbers shown for Dual In-Line Package.

TYPICAL APPLICATION

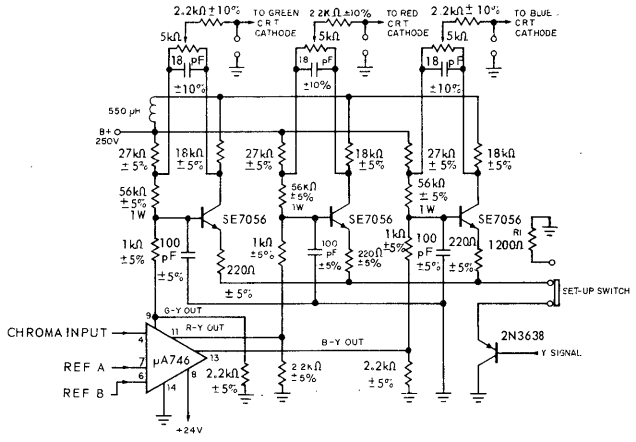
COMPLETE R-G-B VIDEO OUTPUT STAGE



PIN NUMBER SHOWN FOR DUAL IN-LINE PACKAGE

Fully D.C. coupled circuit exhibits negligible drift with temperature, eliminates interaction between contrast and brightness controls, and minimizes gray-scale set-up time. For further applications information, see Application Brief 104.

COMPLETE R-G-B VIDEO OUTPUT STAGE



Pin numbers shown for Dual In-Line Package.

From:

"A Semiconductor Video Output Amplifier for a Red Blue Green Large Screen Color Television Receiver", by D. Poppy. IEEE Transactions on Broadcast and Television Receivers, BTR-15, #2, pp. 167-70, July 1969.

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μA747

DUAL FREQUENCY COMPENSATED OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

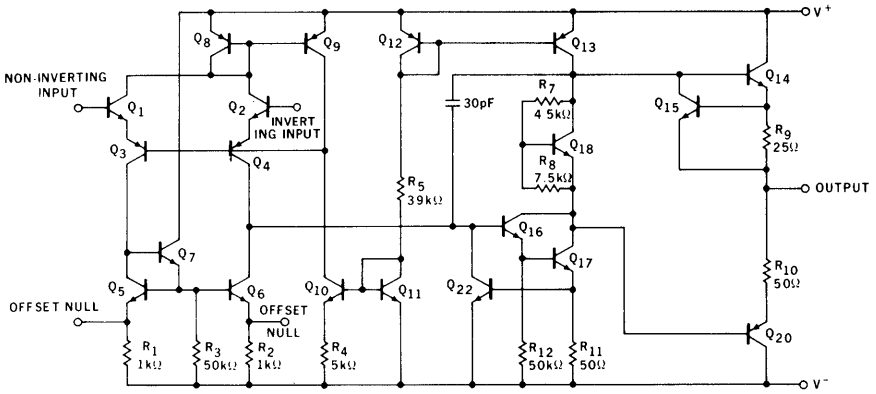
GENERAL DESCRIPTION – The μA747 is a pair of high performance monolithic operational amplifiers constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of "latch-up" make the μA747 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The μA747 is short-circuit protected and requires no external components for frequency compensation. The internal 6 dB/octave roll-off insures stability in closed loop applications. For single amplifier performance, see μA741 data sheet.

- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

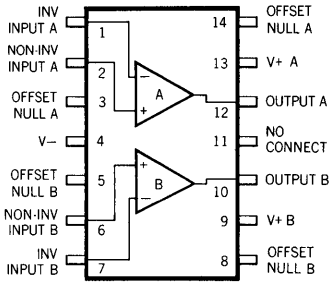
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
Military (312 Grade)	±22 V
Commercial (393 Grade)	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Ceramic DIP	670 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage between Offset Null and V−	±0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 seconds)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

EQUIVALENT CIRCUIT (Each Side)

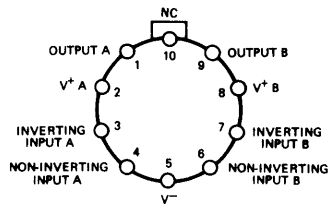


CONNECTION DIAGRAMS
(TOP VIEWS)
14 LEAD DIP



ORDER PART NOS.
U7A7747312
U7A7747393

10 LEAD METAL CAN



ORDER PART NOS.
U5F7747312
U5F7747393

Notes on following pages.

*Planar is a patented Fairchild process.

312 GRADE

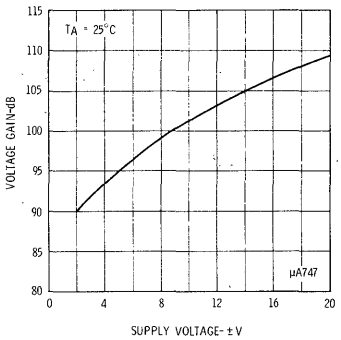
ELECTRICAL CHARACTERISTICS — Each Amplifier ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			1.4		pF
Offset Voltage Adjustment Range			±15		mV
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	50,000	200,000		
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.7	2.8	mA
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate	$R_L \geq 2$ kΩ		0.5		V/μs
Channel Separation			120		dB
The following specifications apply for $-55°C \leq T_A \leq +125°C$.					
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current	$T_A = +125°C$		7.0	200	nA
	$T_A = -55°C$		85	500	nA
Input Bias Current	$T_A = +125°C$		0.03	0.5	μA
	$T_A = -55°C$		0.3	1.5	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	25,000			
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Supply Current	$T_A = +125°C$		1.5	2.5	mA
	$T_A = -55°C$		2.0	3.3	mA
Power Consumption	$T_A = +125°C$		45	75	mW
	$T_A = -55°C$		60	100	mW

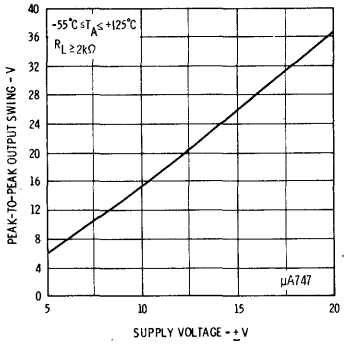
TYPICAL PERFORMANCE CURVES (Each Amplifier)

TYPICAL PERFORMANCE CURVES

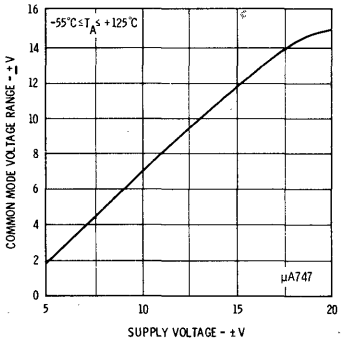
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



393 GRADE

ELECTRICAL CHARACTERISTICS — Each Amplifier ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

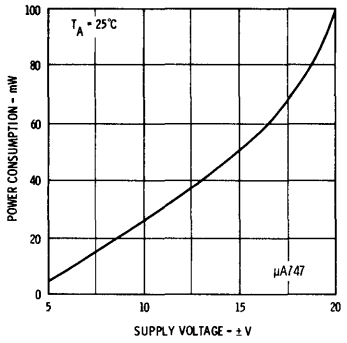
PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			1.4		pF
Offset Voltage Adjustment Range			±15		mV
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	25,000	200,000		
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.7	2.8	mA
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate	$R_L \geq 2$ kΩ		0.5		V/μs
Channel Separation			120		dB
The following specifications apply for $0°C \leq T_A \leq +70°C$.					
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	7.5	mV
Input Offset Current			7.0	300	nA
Input Bias Current			0.03	0.8	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	15,000			
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Supply Current			2.0	3.3	mA
Power Consumption			60	100	mW

NOTES

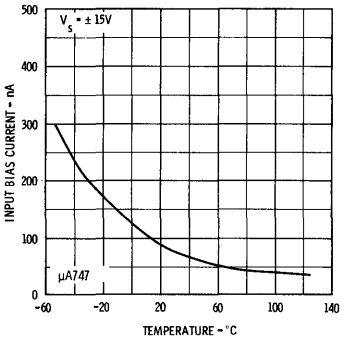
1. Rating applies to ambient temperatures up to 70° C. Above 70° C ambient derate linearly at 6.3 mW/°C for the Metal Can and 8.3 mW/°C for the Ceramic DIP package.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Military rating applies to +125° C case temperature or +60° C ambient temperature for each side.

TYPICAL PERFORMANCE CURVES (Each Amplifier)

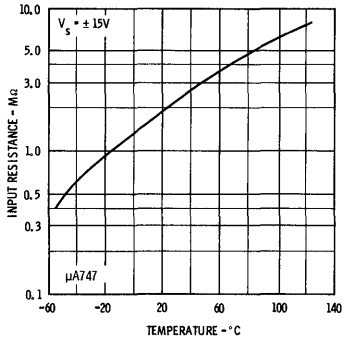
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



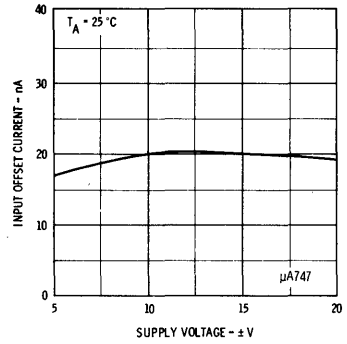
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



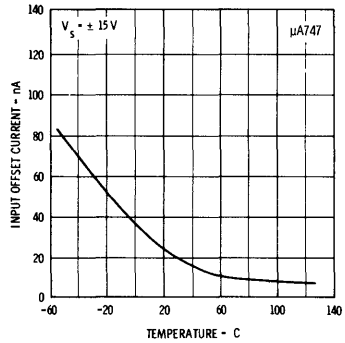
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



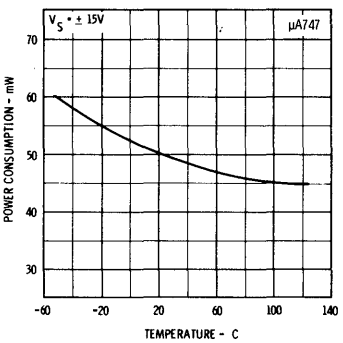
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



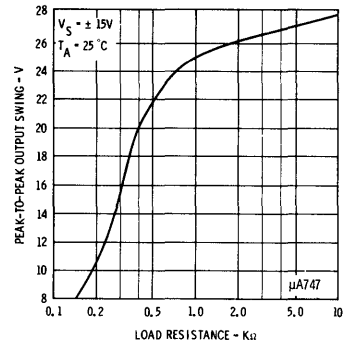
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



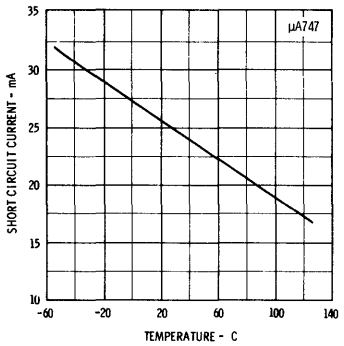
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



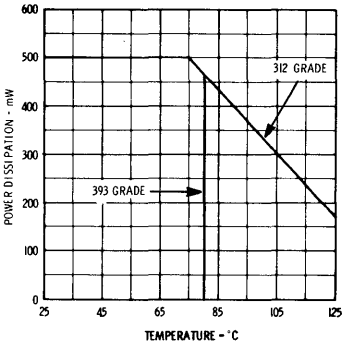
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



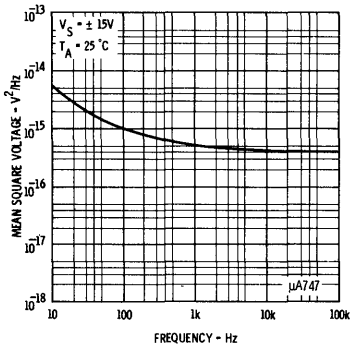
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



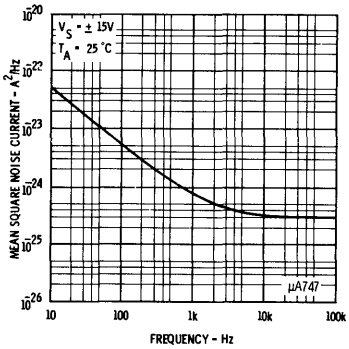
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



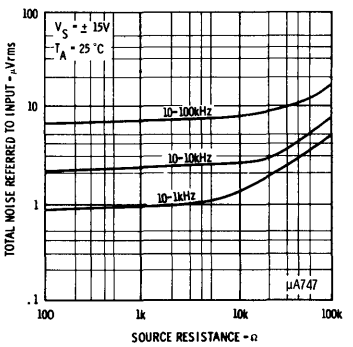
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

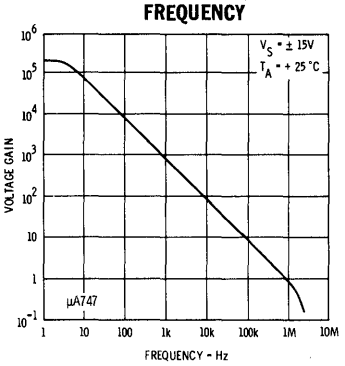


BROADBAND NOISE FOR VARIOUS BANDWIDTHS

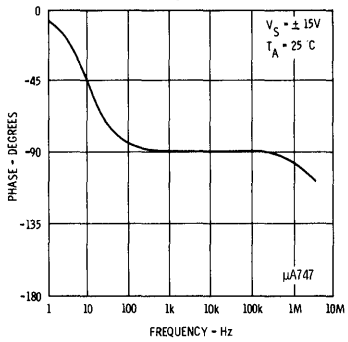


TYPICAL PERFORMANCE CURVES (Each Amplifier)

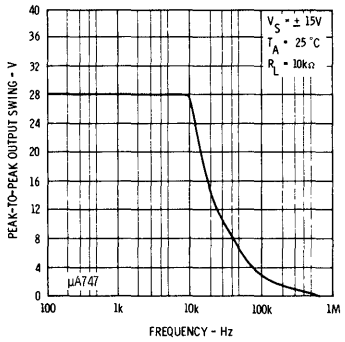
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



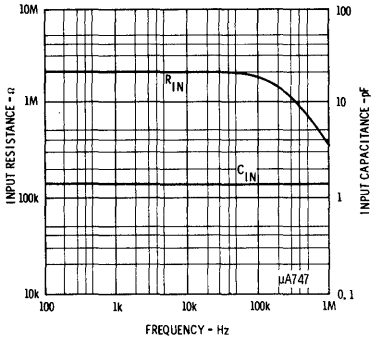
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



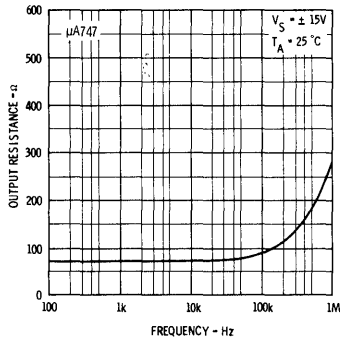
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



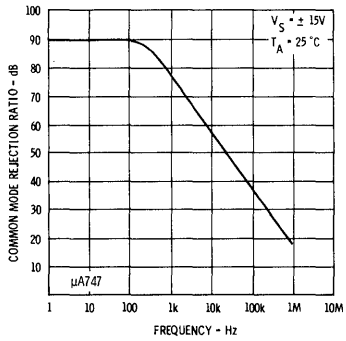
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



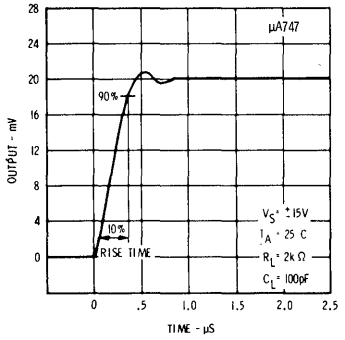
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



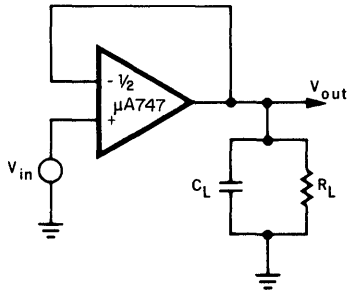
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



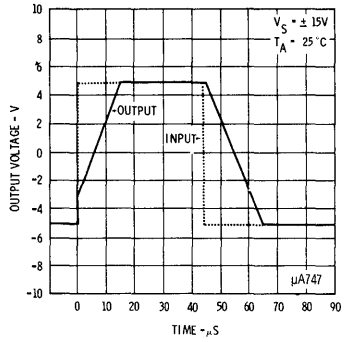
TRANSIENT RESPONSE



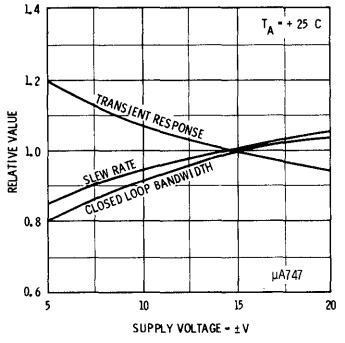
TRANSIENT RESPONSE TEST CIRCUIT



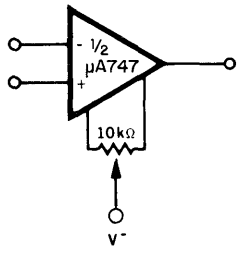
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



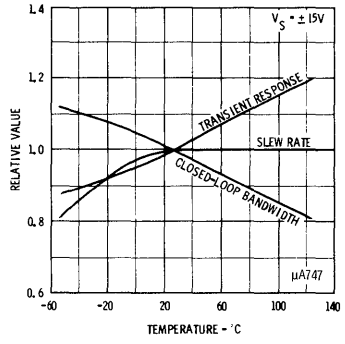
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE OFFSET NULL CIRCUIT

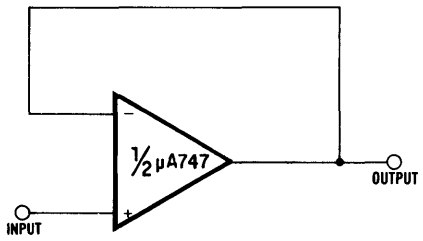


FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



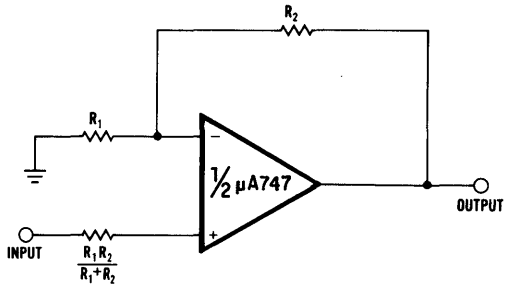
TYPICAL APPLICATIONS

UNITY-GAIN VOLTAGE FOLLOWER



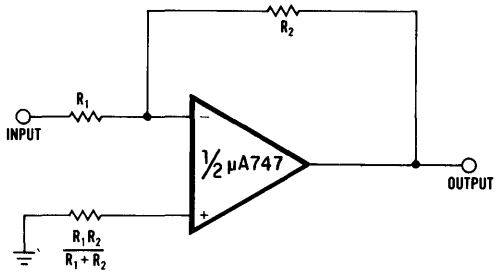
$R_{IN} = 400\ M\Omega$
$C_{IN} = 1\ pF$
$R_{out} << 1\ \Omega$
B.W. = 1 MHz

NON-INVERTING AMPLIFIER



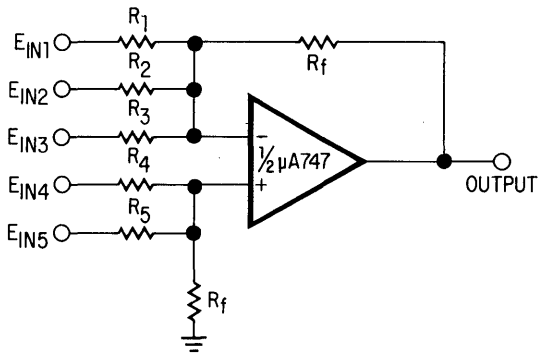
GAIN	R_1	R_2	B.W.	R_{IN}
10	1 kΩ	9 kΩ	100 kHz	400 MΩ
100	100 Ω	9.9 kΩ	10 kHz	280 MΩ
1000	100 Ω	99.9 kΩ	1 kHz	80 MΩ

INVERTING AMPLIFIER



GAIN	R_1	R_2	B.W.	R_{IN}
1	10 kΩ	10 kΩ	1 MHz	10 kΩ
10	1 kΩ	10 kΩ	100 kHz	1 kΩ
100	1 kΩ	100 kΩ	10 kHz	1 kΩ
1000	100 Ω	100 kΩ	1 kHz	100 Ω

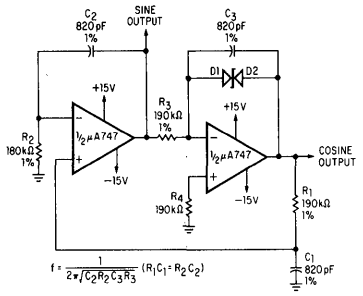
WEIGHTED AVERAGING AMPLIFIER



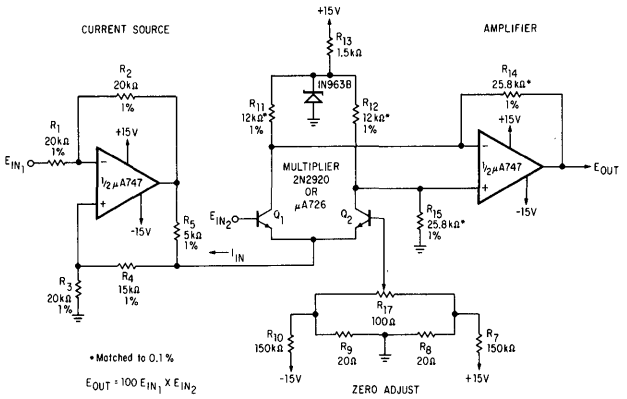
$$-E_{out} = E_{IN1}\left(\frac{R_f}{R_1}\right) + E_{IN2}\left(\frac{R_f}{R_2}\right) + E_{IN3}\left(\frac{R_f}{R_3}\right) - E_{IN4}\left(\frac{R_f}{R_4}\right) - E_{IN5}\left(\frac{R_f}{R_5}\right)$$

TYPICAL APPLICATIONS

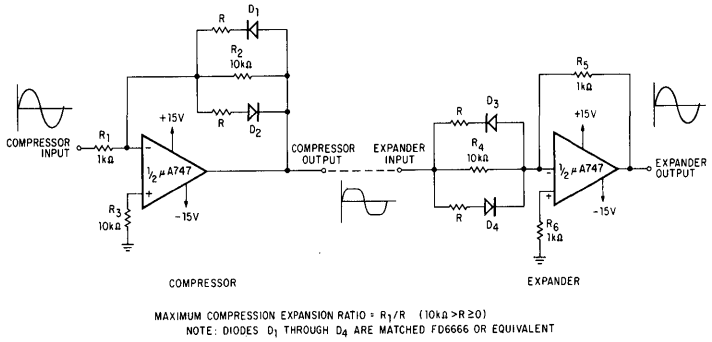
QUADRATURE OSCILLATOR



ANALOG MULTIPLIER

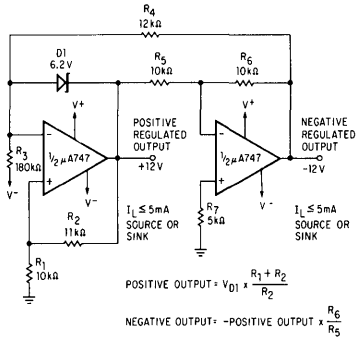


COMPRESSOR/EXPANDER AMPLIFIERS



MAXIMUM COMPRESSION EXPANSION RATIO = R_1/R $(10k\Omega > R \geq 0)$
NOTE: DIODES D_1 THROUGH D_4 ARE MATCHED FD6666 OR EQUIVALENT

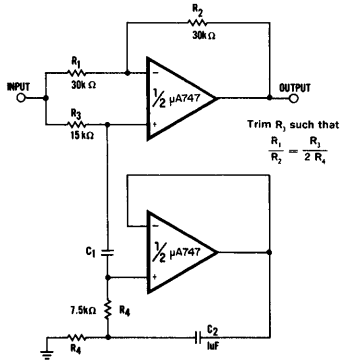
TRACKING POSITIVE AND NEGATIVE VOLTAGE REFERENCES



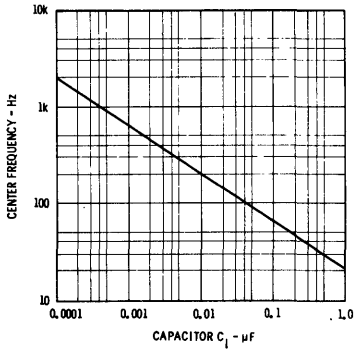
POSITIVE OUTPUT = $V_{D1} \times \frac{R_1 + R_2}{R_2}$

NEGATIVE OUTPUT = -POSITIVE OUTPUT $\times \frac{R_6}{R_5}$

NOTCH FILTER USING THE μA747 AS A GYRATOR



NOTCH FREQUENCY AS A FUNCTION OF C_1



μA748

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

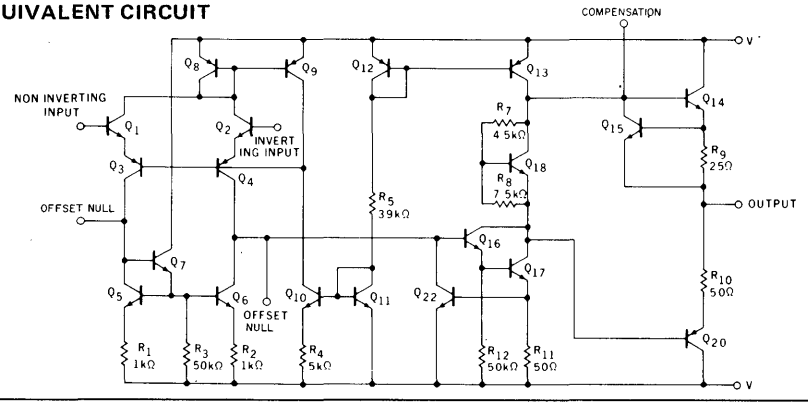
GENERAL DESCRIPTION – The μA748 is a high performance monolithic operational amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications where tailoring of frequency characteristics is desirable. High common mode voltage range and absence of "latch-up" make the μA748 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The μA748 is short-circuit protected and has the same pin configuration as the popular μA741 operational amplifier. Unity gain frequency compensation is achieved by means of a single 30 pF capacitor.

- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

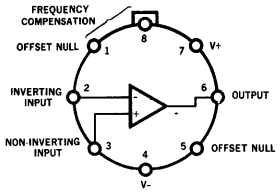
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Ceramic Dip	670 mW
Mini DIP	310 mW
Flatpak	570 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, Ceramic DIP, and Flatpak	−65°C to +150°C
Mini DIP	−55°C to +125°C
Operating Temperature Range	
Military (312 grade)	−55°C to +125°C
Commercial (393 grade)	0°C to +70°C
Lead Temperature (Soldering, 60 Seconds)	
Metal Can, Ceramic DIP and Flatpak	300°C
Mini DIP and Silicone DIP	260°C
Output Short Circuit Duration (Note 3)	Indefinite

EQUIVALENT CIRCUIT



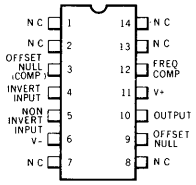
8 LEAD METAL CAN
(TOP VIEW)



NOTE: Pin 4 connected to case

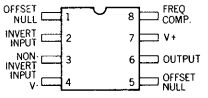
ORDER PART NOS: U5B7748312
U5B7748393

14 LEAD DIP
(TOP VIEW)



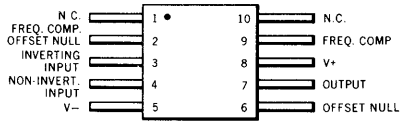
ORDER PART NOS: U6A7748312
U6A7748393

MINI DIP
(TOP VIEW)



ORDER PART NO: U9T7748393

10 LEAD FLATPAK‡
(TOP VIEW)



‡Available on special request

ORDER PART NO: U3F7748312

Notes on following pages.

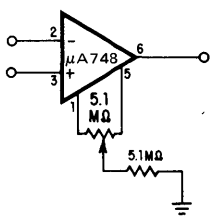
*Planar is a patented Fairchild process.

312 GRADE

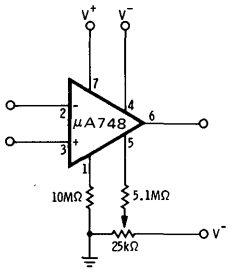
ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C, C_C = 30 pF unless otherwise specified)

PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			2.0		pF
Offset Voltage Adjustment Range			±15		mV
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	50,000	150,000		V/V
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.9	2.8	mA
Power Consumption			60	85	mW
Transient Response (Voltage Follower, Gain of 1)	V_{IN} = 20 mV, C_C = 30 pF, R_L = 2 kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)	$R_L \geq 2$ kΩ		0.5		V/μs
Transient Response (Voltage Follower, Gain of 10)	V_{IN} = 20 mV, C_C = 3.5 pF, R_L = 2 kΩ, $C_L \leq 100$ pF				
Risetime			0.2		μs
Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)	$R_L \geq 2$ kΩ, C_C = 3.5 pF		5.5		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current	T_A = +125°C		10	200	nA
	T_A = −55°C		50	500	nA
Input Bias Current	T_A = +125°C		0.03	0.5	μA
	T_A = −55°C		0.3	1.5	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	25,000			V/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Supply Current	T_A = +125°C		1.5	2.5	mA
	T_A = −55°C		2.0	3.3	mA
Power Consumption	T_A = +125°C		45	75	mW
	T_A = −55°C		60	100	mW

VOLTAGE OFFSET NULL CIRCUIT



SUGGESTED



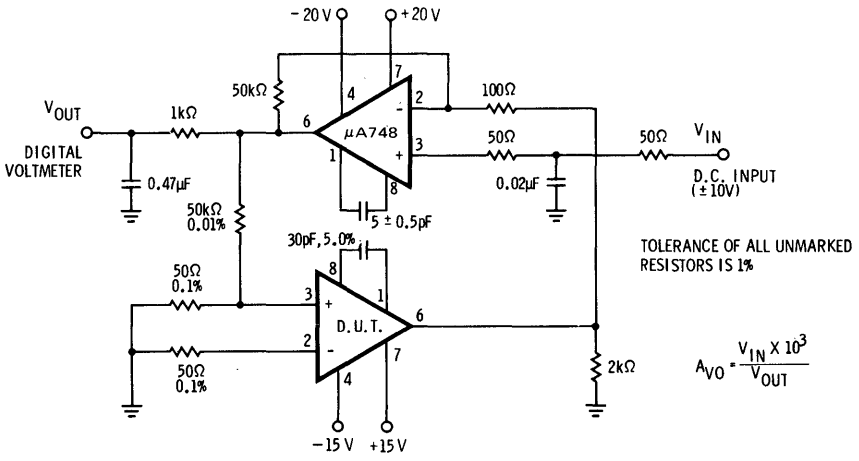
ALTERNATE

393 GRADE

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C, C_C = 30 pF unless otherwise specified)

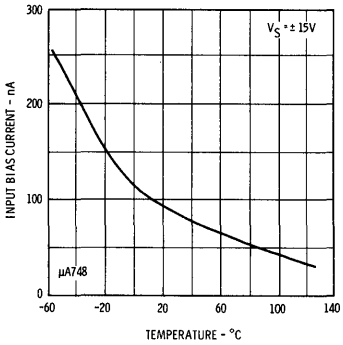
PARAMETERS (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0	mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			2.0		pF
Offset Voltage Adjustment Range			±15		mV
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	20,000	150,000		V/V
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.9	2.8	mA
Power Consumption			60	85	mW
Transient Response (Voltage Follower, Gain of 1)	V_{IN} = 20 mV, C_C = 30 pF, R_L = 2 kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)	$R_L \geq 2$ kΩ		0.5		V/μs
Transient Response (Voltage Follower, Gain of 10)	V_{IN} = 20 mV, C_C = 3.5 pF, R_L = 2 kΩ, $C_L \leq 100$ pF				
Risetime			0.2		μs
Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)	$R_L \geq 2$ kΩ		5.5		V/μs
The following specifications apply for 0°C ≤ T_A ≤ +70°C:					
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, V_{OUT} = ±10 V	15,000			V/V
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Power Consumption			60	100	mW

GAIN TEST CIRCUIT

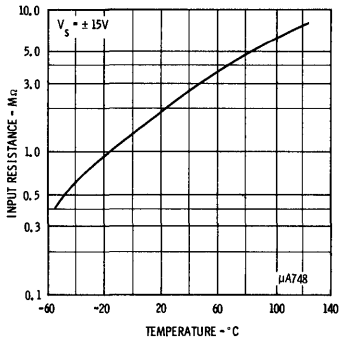


TYPICAL PERFORMANCE CURVES (FOR 312 GRADE)

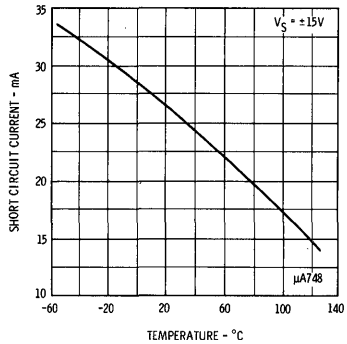
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



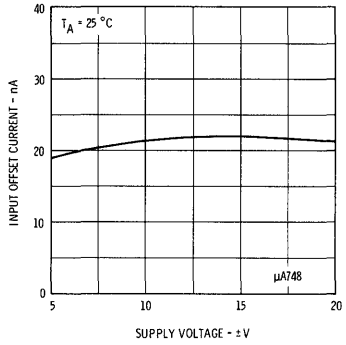
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



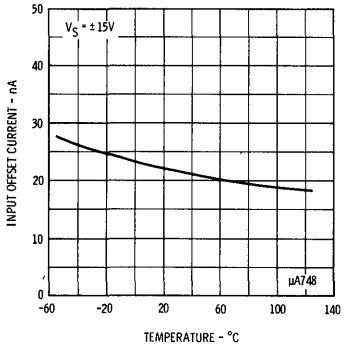
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



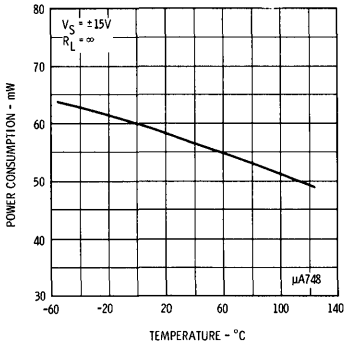
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

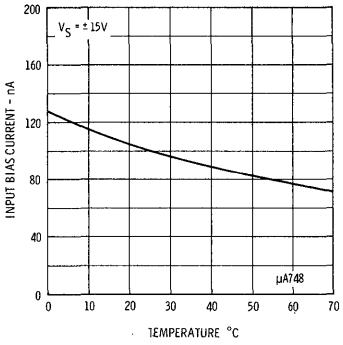


POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

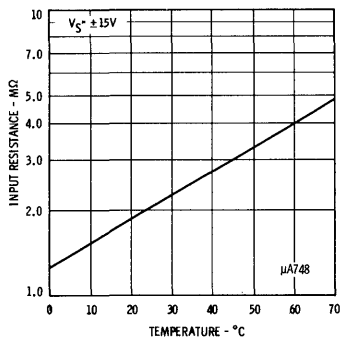


TYPICAL PERFORMANCE CURVES (FOR 393 GRADE)

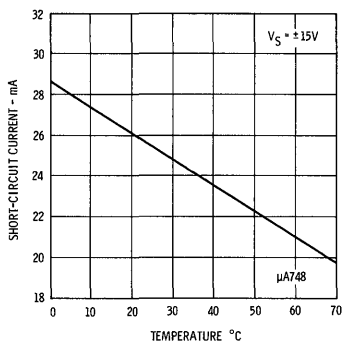
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



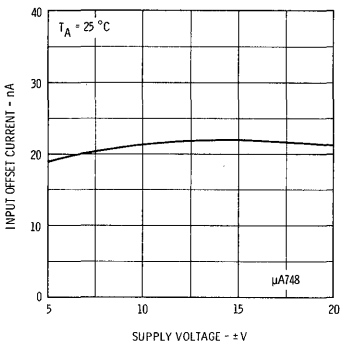
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



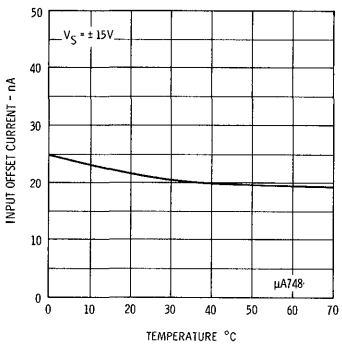
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



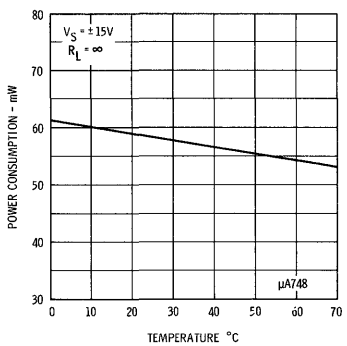
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



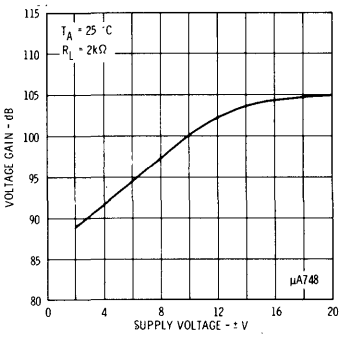
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



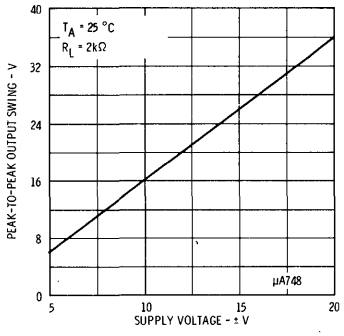
TYPICAL PERFORMANCE CURVES (FOR 312 AND 393 GRADES)

(unless otherwise specified)

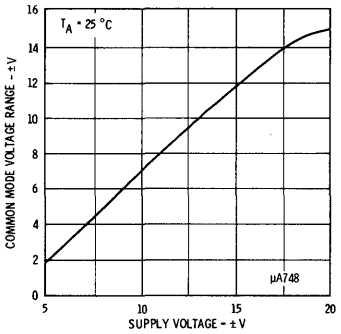
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



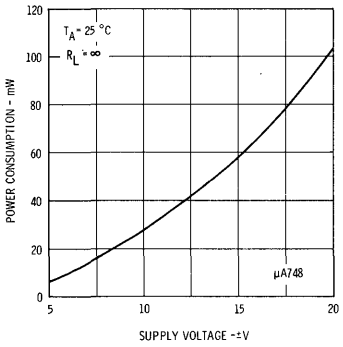
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



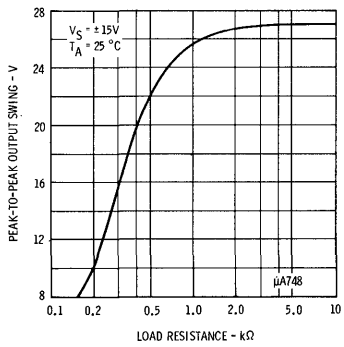
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



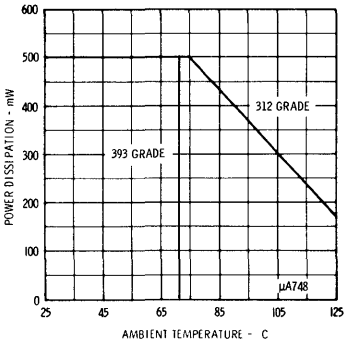
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



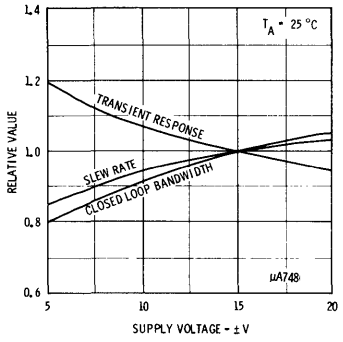
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



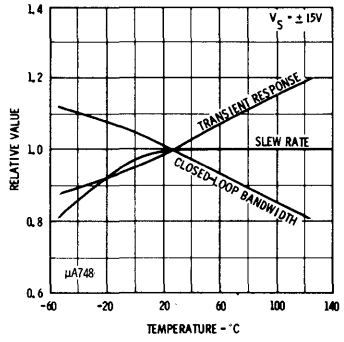
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



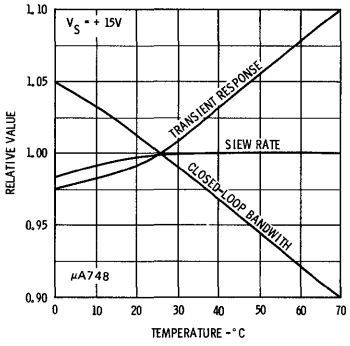
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



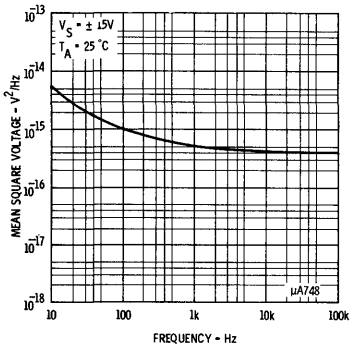
312 GRADE FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



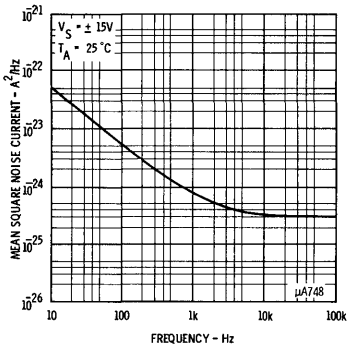
393 GRADE FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



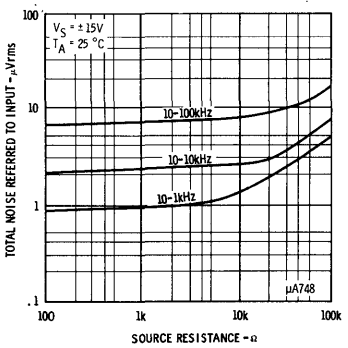
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

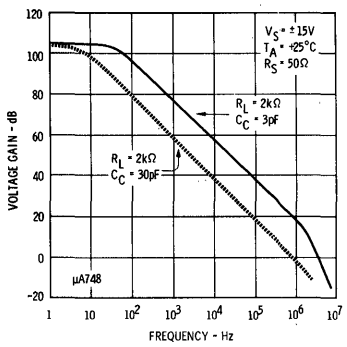


BROADBAND NOISE FOR VARIOUS BANDWIDTHS

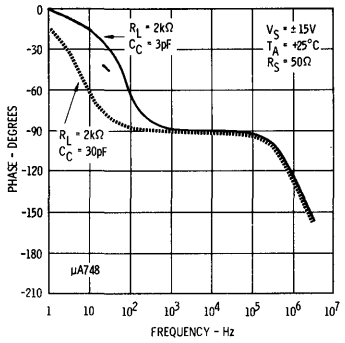


TYPICAL PERFORMANCE CURVES (FOR 312 AND 393 GRADES)

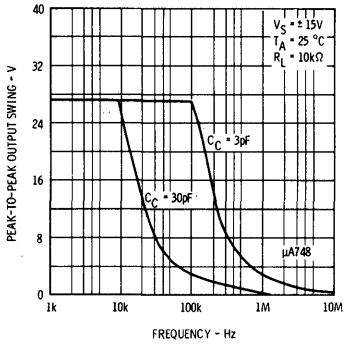
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



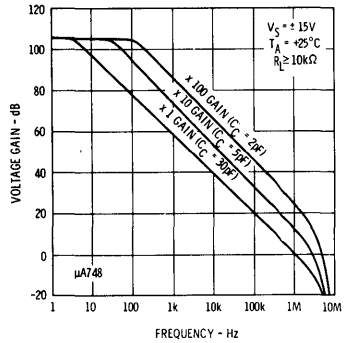
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



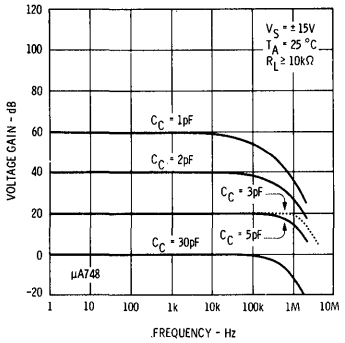
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



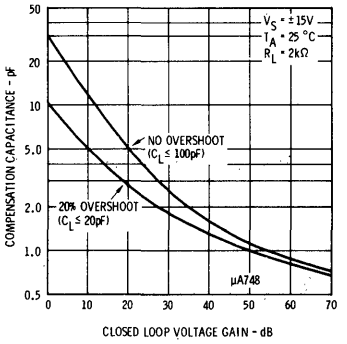
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY FOR VARIOUS GAIN/COMPENSATION OPTIONS



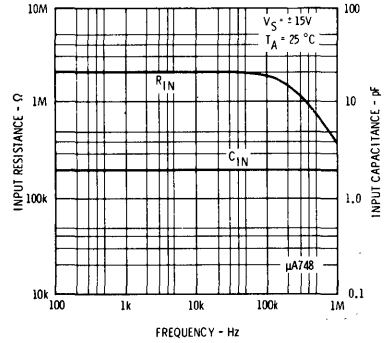
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



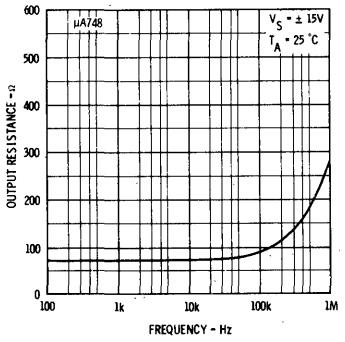
COMPENSATION CAPACITANCE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN



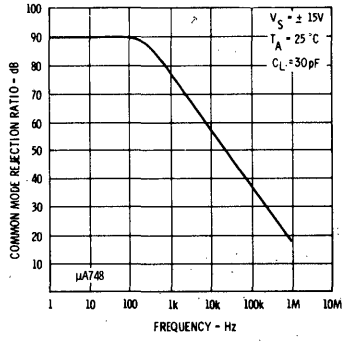
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



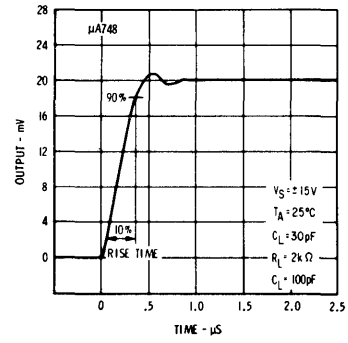
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



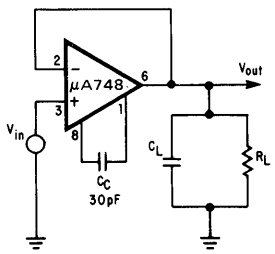
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



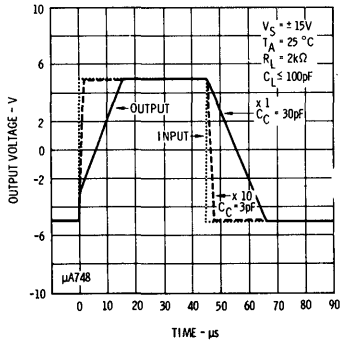
VOLTAGE FOLLOWER TRANSIENT RESPONSE (GAIN OF 1)



TRANSIENT RESPONSE TEST CIRCUIT

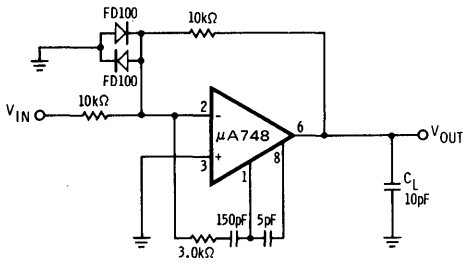


VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE

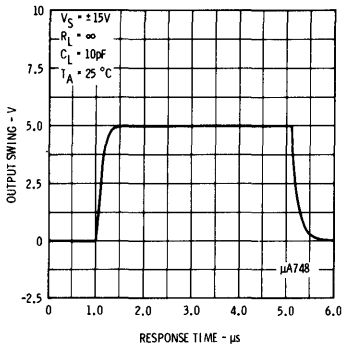


TYPICAL PERFORMANCE CURVES (FOR 312 AND 393 GRADES)

FEED-FORWARD COMPENSATION

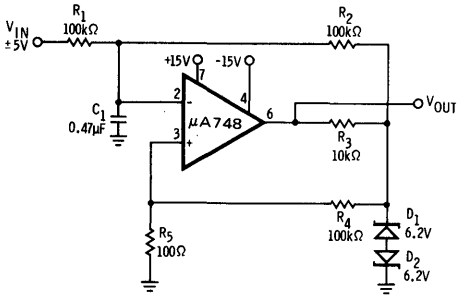


LARGE SIGNAL FEED–FORWARD TRANSIENT RESPONSE

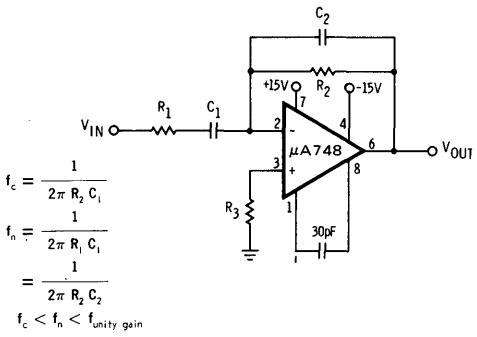


TYPICAL APPLICATIONS

PULSE WIDTH MODULATOR



PRACTICAL DIFFERENTIATOR



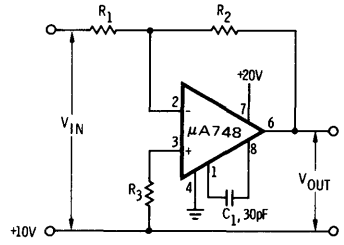
$$f_c = \frac{1}{2\pi R_2 C_1}$$

$$f_n = \frac{1}{2\pi R_1 C_1}$$

$$= \frac{1}{2\pi R_2 C_2}$$

$$f_c < f_n < f_{unity\ gain}$$

CIRCUIT FOR OPERATING THE μA748 WITHOUT A NEGATIVE SUPPLY



NOTES

1. Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can, 8.3 mW/°C for the Ceramic DIP, 5.6 mW/°C for the Mini DIP and 7.1 mW/°C for the Flatpak package.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C case temperature or +75°C ambient temperature.

μA749

DUAL OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

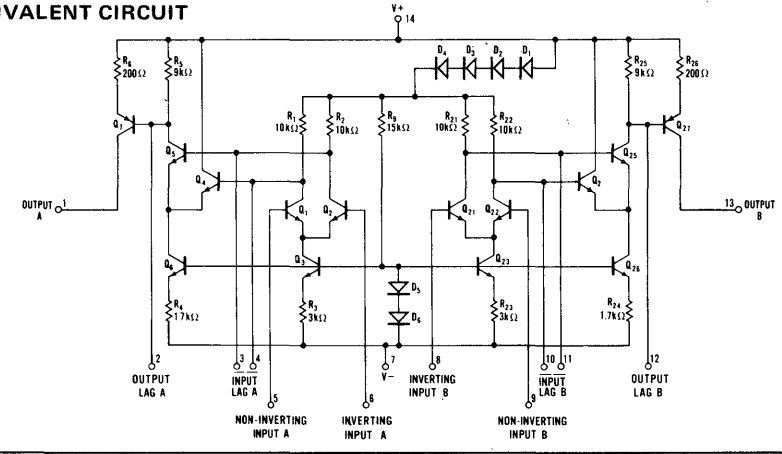
GENERAL DESCRIPTION – The μA749 consists of two identical high gain operational amplifiers constructed on a single silicon chip using the Fairchild Planar* epitaxial process. These three-stage amplifiers use class A PNP transistor output stages with uncommitted collectors. This enables a variety of loads to be employed for general purpose applications from DC to 10 MHz where two high performance operational amplifiers are required. In addition, the outputs may be 'OR'ed for use as a dual comparator or they may function as diodes in low threshold rectifying circuits such as absolute value amplifiers, peak detectors, etc.

- **SINGLE OR DUAL SUPPLY OPERATION**
- **LOW POWER CONSUMPTION**
- **HIGH GAIN, 25,000 V/V**
- **LARGE COMMON MODE RANGE, +11 V, −13 V**
- **EXCELLENT GAIN STABILITY VS. SUPPLY VOLTAGE**
- **NO LATCH-UP**
- **OUTPUT SHORT CIRCUIT PROTECTED**

ABSOLUTE MAXIMUM RATINGS

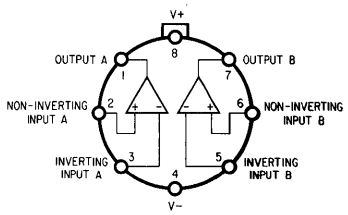
Supply Voltage	
(312 and 393 Grades)	±18 V
(393 Grade)	±12 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Ceramic DIP	650 mW
Differential Input Voltage	±5 V
Input Voltage (Note 2)	
(312 and 393 Grades)	±15 V
(393 Grade)	±12 V
Storage Temperature Range	−65° C to +150° C
Operating Temperature Range	
(312 Grade)	−55° C to +125° C
(393 and 394 Grades)	0° C to +70° C
Lead Temperature (Soldering, 60 seconds)	300° C
Output Short-Circuit Duration, T_A = 25° C (Note 3)	30 seconds

EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS
(TOP VIEWS)

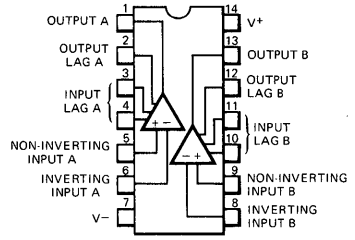
8 LEAD METAL CAN



Note: Pin 4 connected to case

ORDER PART NO. U5B7749394

14 LEAD DIP



ORDER PART NOS:
U6A7749312
U6A7749393

Notes on following pages.

*Planar is a patented Fairchild process.

312 GRADE

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, R_L = 5 kΩ to Pin 7, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	R_S = 200 Ω		1.0	3.0	mV
Input Offset Current			50	400	nA
Input Bias Current			0.30	0.75	μA
Input Resistance		100	150		kΩ
Large-Signal Voltage Gain	V_{OUT} = ±10 V	20,000	50,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Output Resistance	f = 1.0 kHz		5.0		kΩ
Common Mode Rejection Ratio	R_S = 200 Ω, V_{IN} = +11.5 V to −13.5 V	70	90		dB
Positive Supply Voltage Rejection Ratio	R_S = 200 Ω		50	200	μV/V
Negative Supply Voltage Rejection Ratio	R_S = 200 Ω		50	200	μV/V
Input Voltage Range		−13		+11	V
Internal Power Dissipation	V_{OUT} = 0		180	220	mW
Supply Current	V_{OUT} = 0		9.0	10.4	mA
Broadband Noise Figure	R_S = 10 kΩ BW = 10 Hz to 10 kHz		2.5		dB
Turn On Delay (See Fig. 3)	Open Loop, V_{IN} = ±20 mV		0.2		μs
Turn Off Delay (See Fig. 3)	Open Loop, V_{IN} = ±20 mV		0.3		μs
Slew Rate (unity gain) (See Figure 2)	C_1 = .02 μF, R_1 = 33 Ω, C_2 = 10 pF		2.0		V/μs
Channel Separation (See Fig. 4)	R_S = 1 kΩ, f = 10 kHz		140		dB
The following specifications apply for V_S = ±4.0 V, R_L = 10 kΩ to Pin 7 T_A = 25°C :					
Input Offset Voltage	R_S = 200 Ω		1.0	3.0	mV
Input Offset Current			50	300	nA
Input Bias Current			0.15	0.75	μA
Supply Current	V_{OUT} = 0		2.5	4.8	mA
Internal Power Dissipation	V_{OUT} = 0		20	36	mW
Large-Signal Voltage Gain	V_{OUT} = ± 2.0 V	20,000	60,000		V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V
The following specifications apply for −55°C ≤ T_A ≤ +125°C: V_S = ±15 V, R_L = 5 kΩ to Pin 7:					
Large Signal Voltage Gain	V_{OUT} = ±10 V, T_A = +125°C	6,500	20,000		V/V
	V_{OUT} = ±10 V, T_A = −55°C	20,000	30,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Input Offset Voltage	R_S = 200 Ω		1.0	6.0	mV
Input Offset Current	T_A = +125°C		0.05	1.0	μA
	T_A = −55°C		0.05	1.5	μA
Input Bias Current	T_A = +125°C		0.15	0.75	μA
	T_A = −55°C		0.3	3.0	μA
Input Offset Voltage Drift	R_S = 200 Ω, +25°C ≤ T_A ≤ +125°C		3.0		μV/°C
	R_S = 200 Ω, −55°C ≤ T_A ≤ +25°C		3.0		μV/°C
Input Offset Current Drift	+25°C ≤ T_A ≤ +125°C		0.5		nA/°C
	−55°C ≤ T_A ≤ +25°C		2.0		nA/°C
Input Bias Current Drift	−55°C ≤ T_A ≤ +125°C		5.0		nA/°C
Supply Current	V_{OUT} = 0, T_A = +125°C			9.7	mA
	V_{OUT} = 0, T_A = −55°C			13	mA
Internal Power Dissipation	V_{OUT} = 0, T_A = +125°C			200	mW
	V_{OUT} = 0, T_A = −55°C			300	mW
The following specifications apply for −55°C ≤ T_A ≤ +125°C: V_S = ±4 V, R_L = 10 kΩ to Pin 7:					
Input Offset Voltage	R_S = 200 Ω		1.5	6.0	mV
Input Offset Current			50	750	nA
Large-Signal Voltage Gain	V_{OUT} = ±2.0 V, T_A = +125°C	5,000			V/V
	V_{OUT} = ±2.0 V, T_A = −55°C	20,000			V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V

NOTES

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 8.3 mW/°C for the Ceramic DIP package.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply.

393 GRADE

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, R_L = 5 kΩ to Pin 7, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	R_S = 200 Ω		1.0	6.0	mV
Input Offset Current			50	750	nA
Input Bias Current			0.30	1.5	μA
Input Resistance		50	150		kΩ
Large-Signal Voltage Gain	V_{OUT} = ±10 V	15,000	50,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Output Resistance	f = 1.0 kHz		5.0		kΩ
Common Mode Rejection Ratio	R_S = 200 Ω, V_{IN} = +11.5 V to −13.5 V	70	90		dB
Positive Supply Voltage Rejection Ratio	R_S = 200 Ω		50	350	μV/V
Negative Supply Voltage Rejection Ratio	R_S = 200 Ω		50	200	μV/V
Input Voltage Range		−13		+11	V
Internal Power Dissipation	V_{OUT} = 0		180	330	mW
Supply Current	V_{OUT} = 0		9.0	14	mA
Broadband Noise Figure	R_S = 10 kΩ, BW = 10 Hz to 10 kHz		2.5		dB
Turn On Delay (See Fig. 3)	Open Loop, V_{IN} = ±20 mV		0.2		μs
Turn Off Delay (See Fig. 3)	Open Loop, V_{IN} = ±20 mV		0.3		μs
Slew Rate (unity gain) (See Figure 2)	C_1 = .02 μF, R_1 = 33 Ω, C_2 = 10 pF		2.0		V/μs
Channel Separation (See Fig. 4)	R_S = 1 kΩ, f = 10 kHz		140		dB
The following specifications apply for V_S = ±4.0 V, R_L = 10 kΩ to Pin 7, T_A = 25°C:					
Input Offset Voltage	R_S = 200 Ω		1.0	6.0	mV
Input Offset Current			50	600	nA
Input Bias Current			0.3	1.5	μA
Supply Current	V_{OUT} = 0		2.5		mA
Internal Power Dissipation	V_{OUT} = 0		20		mW
Large-Signal Voltage Gain	V_{OUT} = ± 2.0 V	15,000	60,000		V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V
The following specifications apply for 0°C ≤ T_A ≤ +70°C: V_S = ±15 V, R_L = 5 kΩ to Pin 7:					
Large Signal Voltage Gain	V_{OUT} = ±10 V, T_A = +70°C	8,000	40,000		V/V
	V_{OUT} = ±10 V, T_A = 0°C	15,000	50,000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		−14	−15		V
Input Offset Voltage	R_S = 200 Ω		1.0	9.0	mV
Input Offset Current			0.05	1.5	μA
Input Bias Current			0.3	3.0	μA
Input Offset Voltage Drift	R_S = 200 Ω, +25°C ≤ T_A ≤ +70°C		3.0		μV/°C
	R_S = 200 Ω, 0°C ≤ T_A ≤ +25°C		3.0		μV/°C
Input Offset Current Drift	+25°C ≤ T_A ≤ +70°C		0.5		nA/°C
	0°C ≤ T_A ≤ +25°C		2.0		nA/°C
Input Bias Current Drift	0°C ≤ T_A ≤ +70°C		4.0		nA/°C
The following specifications apply for 0°C ≤ T_A ≤ +70°C: V_S = ±4 V, R_L = 10 kΩ to Pin 7:					
Input Offset Voltage	R_S = 200 Ω		1.5	9.0	mV
Input Offset Current			0.05	1.0	μA
Large-Signal Voltage Gain	V_{OUT} = ±2.0 V, T_A = 70°C	8,000			V/V
Large-Signal Voltage Gain	V_{OUT} = ±2.0 V, T_A = 0°C	15,000			V/V
Positive Output Voltage Swing		+2.5	+2.8		V
Negative Output Voltage Swing		−3.6	−4.0		V

394 GRADE

ELECTRICAL CHARACTERISTICS ($V_S = \pm 6$ V, $R_L = 10$ kΩ to Pin 4. $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\ \Omega$		1.0	10	mV
Input Offset Current			50	600	nA
Input Bias Current			300	1500	nA
Input Resistance		50	150		kΩ
Large-Signal Voltage Gain	$V_{OUT} = \pm 4.0$ V	10,000	20,000		V/V
Positive Output Voltage Swing		+4.5	+5		Volts
Negative Output Voltage Swing		−5.5	−6		Volts
Output Resistance	f = 1.0 kHz		10		kΩ
Input Voltage Range		−4		+2.5	Volts
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		50	100	μV/V
Power Consumption (including load)	$V_{OUT} = 0$	24	36	54	mW
Supply Current (including load)	$V_{OUT} = 0$	2.0	3.0	4.5	mA
Turn On Delay (See Figure 1)	Open Loop, $V_{IN} = \pm 20$ mV, $R_L = 5$ kΩ		0.2		μs
Turn Off Delay (See Figure 1)	Open Loop, $V_{IN} = \pm 20$ mV, $R_L = 5$ kΩ		0.3		μs
Channel Separation (See Figure 3)	$R_S \leq 10$ kΩ, f = 10 kHz		140		dB

OFFSET NULL NETWORK

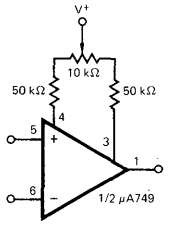


Fig. 1

FREQUENCY RESPONSE TEST CIRCUIT

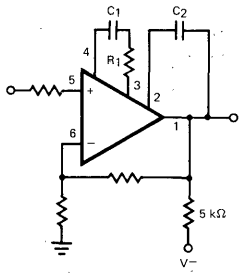


Fig. 2

CHANNEL SEPARATION TEST CIRCUIT

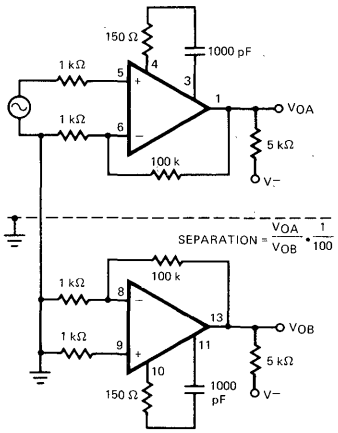


Fig. 4

PULSE RESPONSE WAVEFORMS

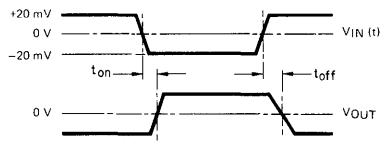
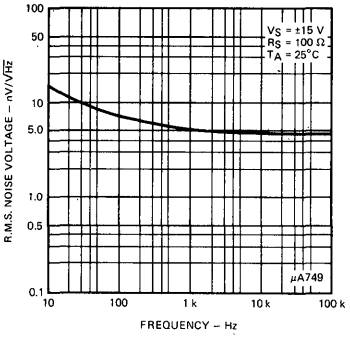


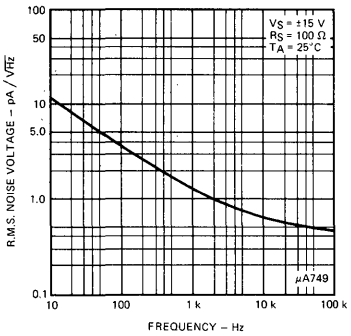
Fig. 3

TYPICAL PERFORMANCE CURVES

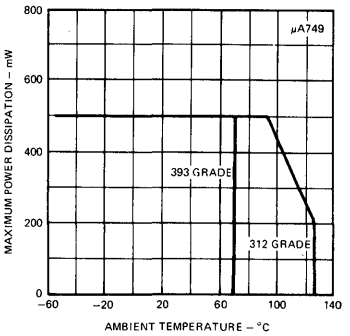
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



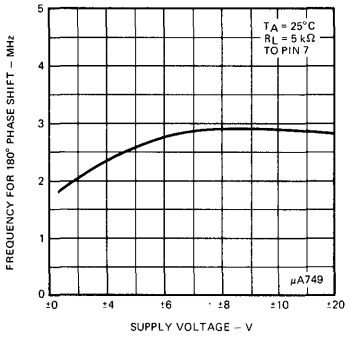
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



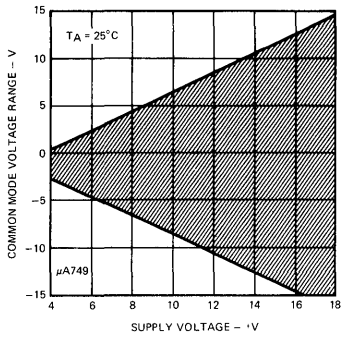
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF TEMPERATURE



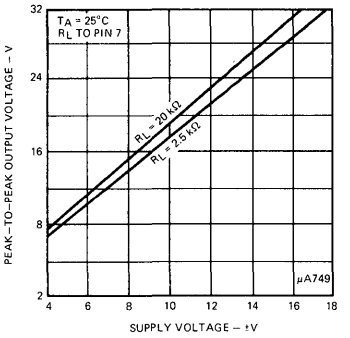
OPEN LOOP 180° PHASE SHIFT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



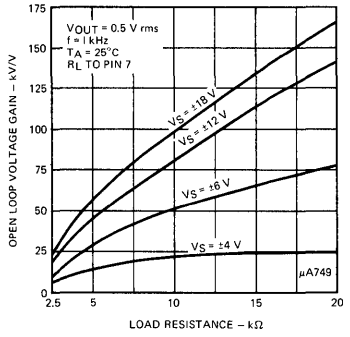
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



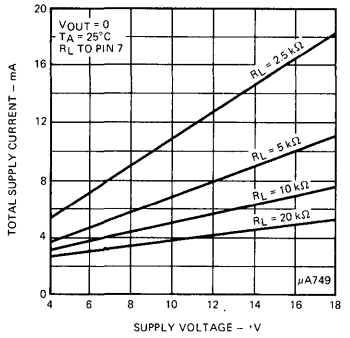
TYPICAL OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



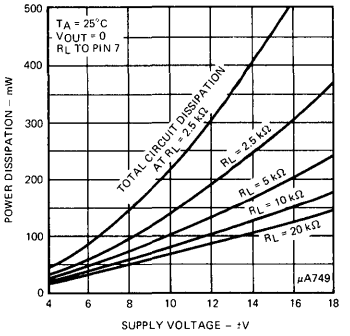
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF LOAD RESISTANCE



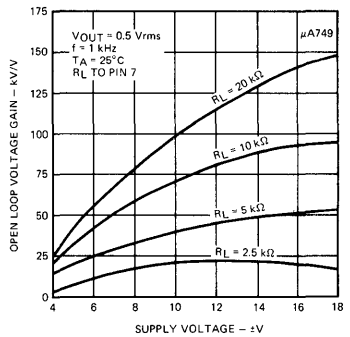
TOTAL SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



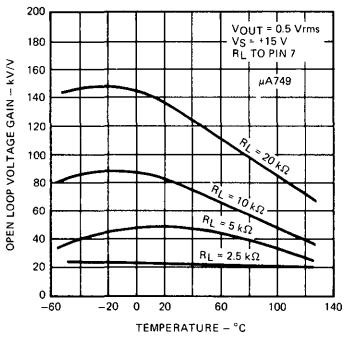
TOTAL POWER DISSIPATION AS A FUNCTION OF SUPPLY VOLTAGE AND LOAD



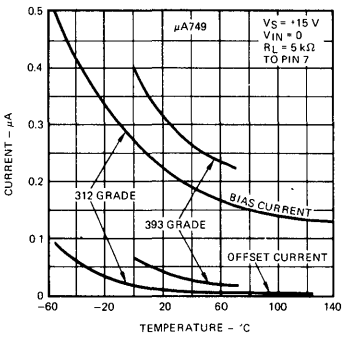
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OPEN LOOP GAIN AS A FUNCTION OF TEMPERATURE

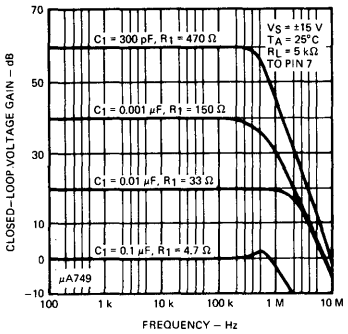


INPUT OFFSET CURRENT AND BIAS CURRENT AS FUNCTIONS OF TEMPERATURE

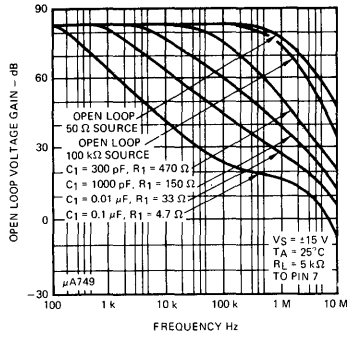


TYPICAL PERFORMANCE CURVES

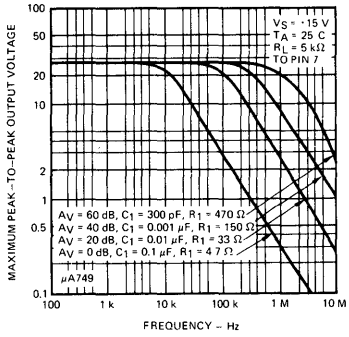
CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY



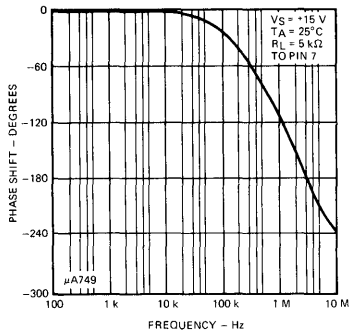
OPEN LOOP FREQUENCY RESPONSE USING RECOMMENDED COMPENSATION NETWORKS



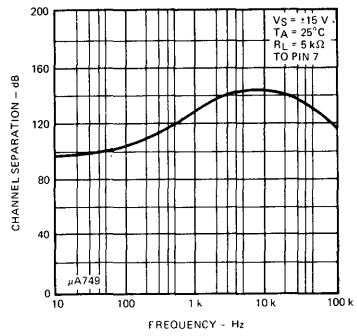
OUTPUT CAPABILITY AS A FUNCTION OF FREQUENCY AND COMPENSATION



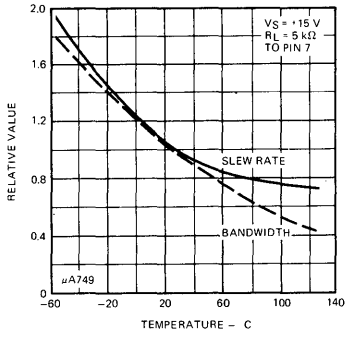
OPEN LOOP PHASE SHIFT WITHOUT COMPENSATION



CHANNEL SEPARATION AS A FUNCTION OF FREQUENCY

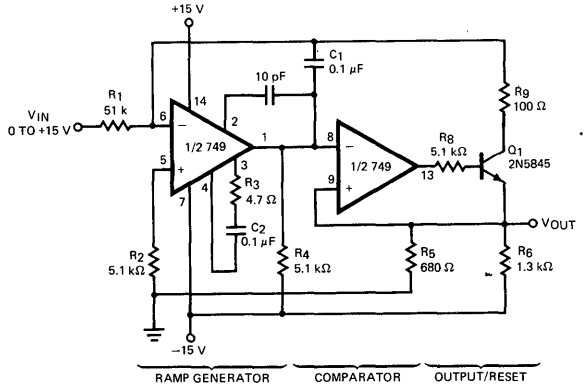


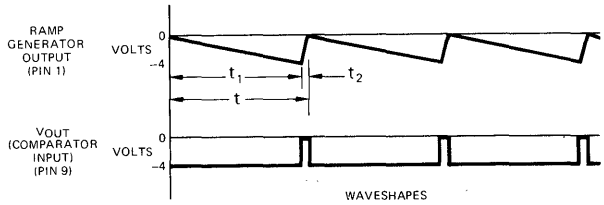
CHANGE OF A.C. CHARACTERISTICS WITH TEMPERATURE



APPLICATION

VOLTAGE TO FREQUENCY CONVERTER





$$t = t_1 + t_2 = 4\,\frac{R_1\,C_1}{V_{IN}} + \frac{4\,R^*\,C_1}{15}$$

$R^* = R$ pin 1 + R_9 + R_{CE} Q_1 + R_6 output stage.

μA754

TV/FM SOUND SYSTEM

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA754 monolithic TV/FM Sound System consists of a four-stage limiting IF amplifier, doubly-balanced Quadrature FM Detector and a high output audio driver stage constructed on a single silicon chip using the Fairchild Planar* Epitaxial Process. Excellent sensitivity, high AM rejection and an internally regulated power supply coupled with low external component requirement make the μA754 suitable for a wide variety of applications including TV sound channels, line operated and automobile FM radios and mobile communications equipment. Other applications include analog multipliers, phase-locked loops, and synchronous detectors.

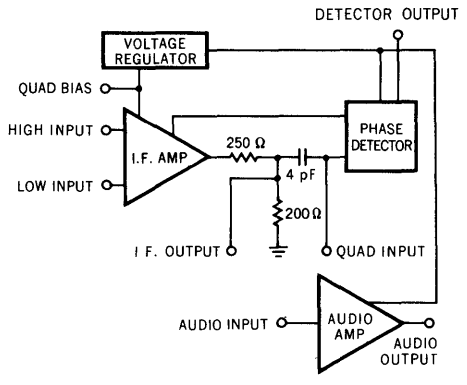
- **70 μV SENSITIVITY**
- **50 dB AM REJECTION**
- **INTERNALLY REGULATED SUPPLY**
- **SINGLE COIL QUADRATURE DETECTOR**
- **3 VRMS AUDIO OUTPUT**
- **LOW EXTERNAL COMPONENT COUNT**

ABSOLUTE MAXIMUM RATINGS

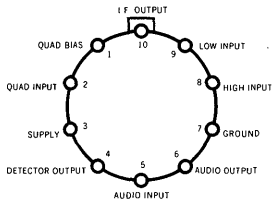
Voltage at any terminal must not exceed V_{SUPPLY}

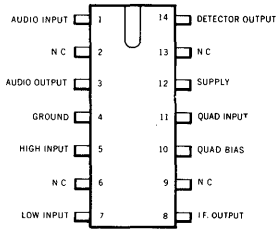
Supply Current	40 mA
Input Voltage (Note 1)	±5 Volts
Internal Power Dissipation (Note 2)	
Metal Can	500 mW
Ceramic DIP	670 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	
TO-100 and Ceramic DIP	−65°C to +150°C
Lead Temperature	
TO-100 and Ceramic DIP (Soldering, 60 seconds)	+300°C
Audio Output Short Circuit Duration	60 Seconds

BLOCK DIAGRAM

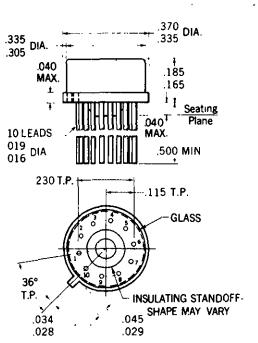


CONNECTION DIAGRAMS
(TOP VIEW)





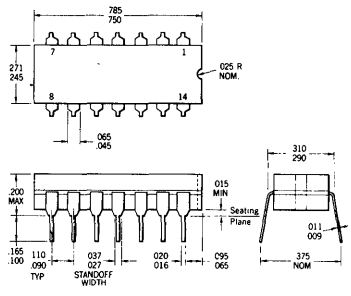
PHYSICAL DIMENSIONS
In accordance with JEDEC (TO-100) Outline



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams

ORDER PART NO. U5E7754394

14 LEAD CERAMIC DIP



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

ORDER PART NO. U6A7754394

Notes on following page.

*Planar is a patented Fairchild process.

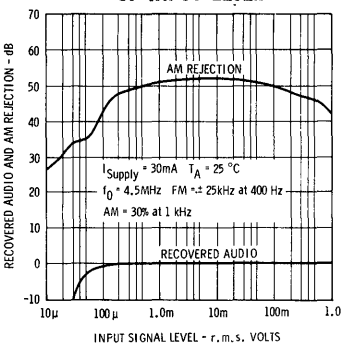
ELECTRICAL CHARACTERISTICS (T_A = 25°C, I^+ = 35 mA, unless otherwise specified)

PARAMETERS	CONDITIONS	TEST CIRCUIT	MIN.	TYP.	MAX.	UNITS
Static Characteristics						
Voltage at SUPPLY terminal		1	11.8	13	13.5	Volts
Supply Current	V_{supply} = 9.0 V	1	11.8	23	28	mA
Voltage at LOW INPUT terminal		1	1.2	1.4	1.8	Volts
Voltage at QUAD BIAS terminal		1	2.5	2.8	3.5	Volts
Voltage at I.F. OUTPUT terminal		1		0.7		Volts
Voltage at AUDIO INPUT terminal		1	1.2	1.5	1.7	Volts
Voltage at AUDIO OUTPUT terminal		1	4.8	5.7	7.5	Volts
Internal Power Dissipation		1	400	450	480	mW
Voltage at DETECTOR OUTPUT terminal		1	5.8	8.0	9.5	Volts
Short-circuit Current at AUDIO OUTPUT terminal		1		35	45	mA
Dynamic Characteristics of IF Amplifier & Detector at 4.5 MHz (FM = ±25 kHz at 400 Hz, V_{in} = 10 mV)						
Input Voltage for −3 dB Limiting		2		70	200	μV
IF Amplifier Voltage Gain		2	65	72		dB
A.M. Rejection	**AM** = 30% at 1 kHz	2	40	50		dB
Recovered Audio Voltage at Detector Output		2	250	450		mV
Total Harmonic Distortion		2		1.0	2.0	%
Detector Output Resistance				8.0		kΩ
Quad. Input Resistance				90		kΩ
Quad. Input Capacitance				7.0		pF
IF Amplifier Input Resistance				10		kΩ
IF Amplifier Input Capacitance				4.0		pF
IF Output Voltage		2	0.4	0.6		V_{p-p}
IF Output Resistance				125		Ω
IF Output Capacitance				7.0		pF
Dynamic Characteristics of IF Amplifier & Detector at 10.7 MHz (FM = ±75 kHz at 400 Hz, V_{in} = 10 mV)						
Input Voltage for −3 dB Limiting		2		200	300	μV
IF Amplifier Voltage Gain		2	55	62		dB
A.M. Rejection	**AM** = 30% at 1 kHz	2	35	45		dB
Recovered Audio Voltage at Detector Output		2	200	300		mV
Total Harmonic Distortion		2		0.5	2.0	%
Detector Output Resistance				8.0		kΩ
Quad. Input Resistance				100		kΩ
Quad. Input Capacitance				7.0		pF
IF Amplifier Input Resistance				10		kΩ
IF Amplifier Input Capacitance				4.0		pF
IF Output Voltage		2	0.4	0.6		V_{p-p}
IF Output Resistance				150		Ω
IF Output Capacitance				7.0		pF
Dynamic Characteristics of Audio Section (f = 1 kHz, R_S = 50 Ω)						
Open Loop Voltage Gain		3	12.5	16		V/V
Input Resistance			0.1	1.0		kΩ
Output Resistance				30		Ω
Maximum Output Voltage	**THD** = 5%, R_L = 2.4 kΩ	3	2.5	3.0		Vrms
Total Harmonic Distortion	V_{out} = 2 Vrms, R_L = 2.4 kΩ	3		0.8	3.0	%

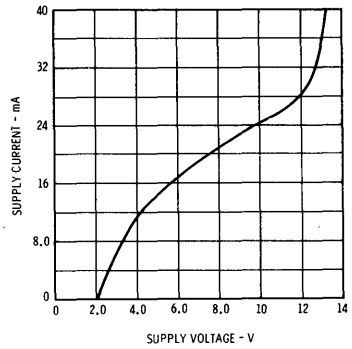
NOTES
1. Voltage applied from High Input to Low Input.
2. Rating applies to ambient temperatures up to 70° C.

TYPICAL PERFORMANCE CURVES

RECOVERED AUDIO AND AM REJECTION AS A FUNCTION OF INPUT LEVEL

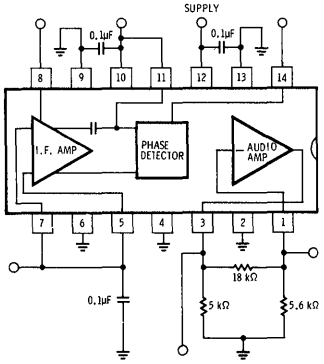


SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

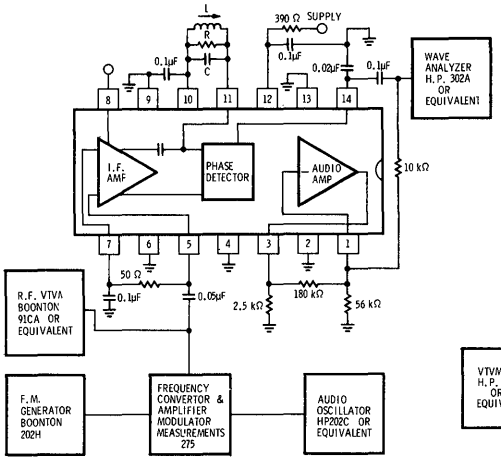


TEST CIRCUITS

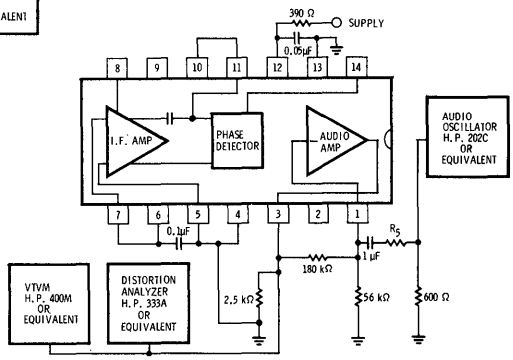
TEST CIRCUIT 1 STATIC CHARACTERISTICS



TEST CIRCUIT 2 DYNAMIC CHARACTERISTICS OF IF AMPLIFIER & QUADRATURE DETECTOR

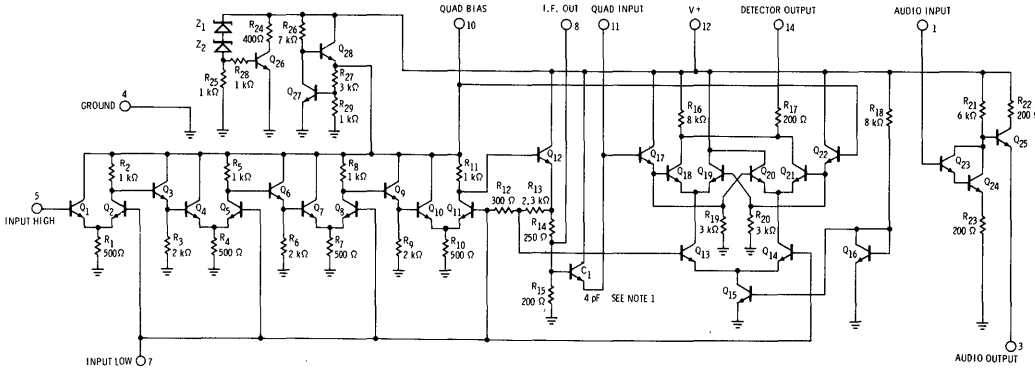


TEST CIRCUIT 3 AUDIO AMPLIFIER DYNAMIC CHARACTERISTICS



NOTE: For values of Quadrature Components — see Table 1 below

EQUIVALENT CIRCUIT



NOTES:

(1) C_l is a reverse-biased E-B Junction Capacitor.

(2) Pin numbers shown for Dual In-Line Package.

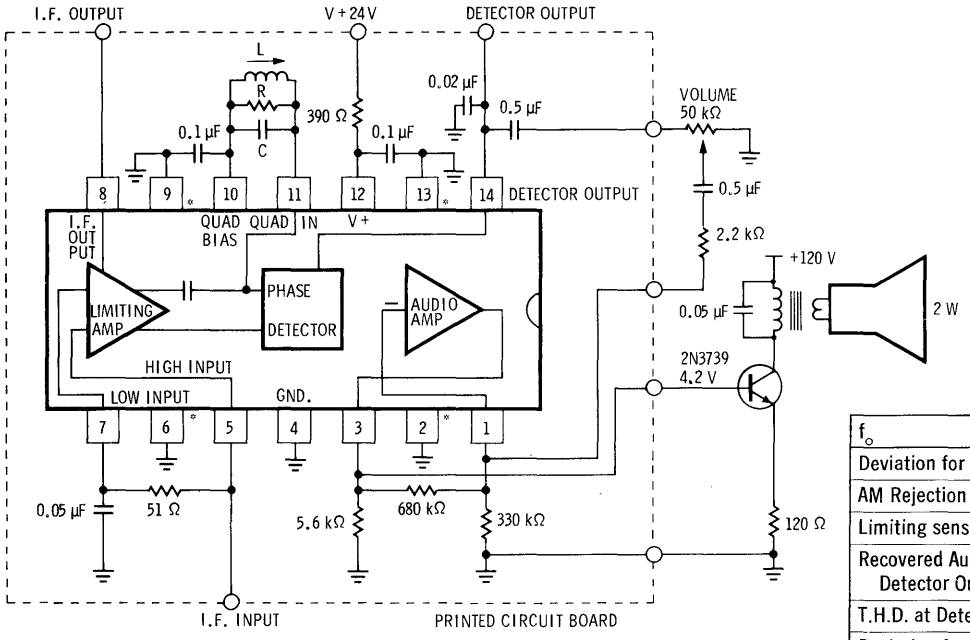
TABLE 1 VALUE OF QUADRATURE COMPONENTS

TABLE I

f_o	4.5 MHz	10.7 MHz
FM	± 25 kHz	75 kHz
L	10.4 μH	3.1 μH
C	120 pF	68 pF
Q_u	40	40
Q_L	30	15
Separation	300 kHz	1.1 MHz

TYPICAL APPLICATION

I.F. AMPLIFIER-DETECTOR 2W CLASS A OUTPUT STAGE



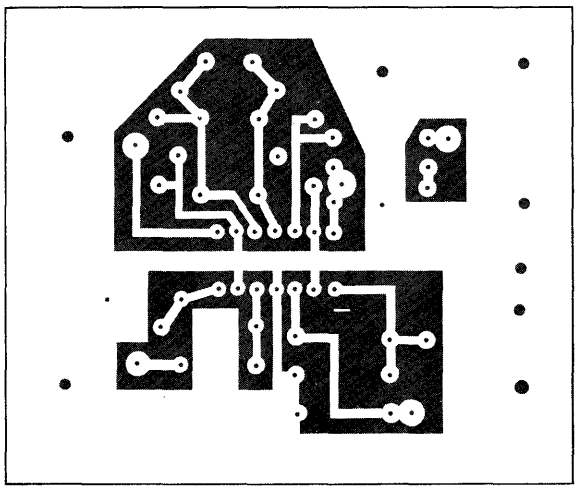
f_o	4.5	10.7	MHz
L	10.4	3.1	μH
C	120	68	pF
R	20 k	3.3 k	Ω

TYPICAL PERFORMANCE OF 2W CIRCUIT

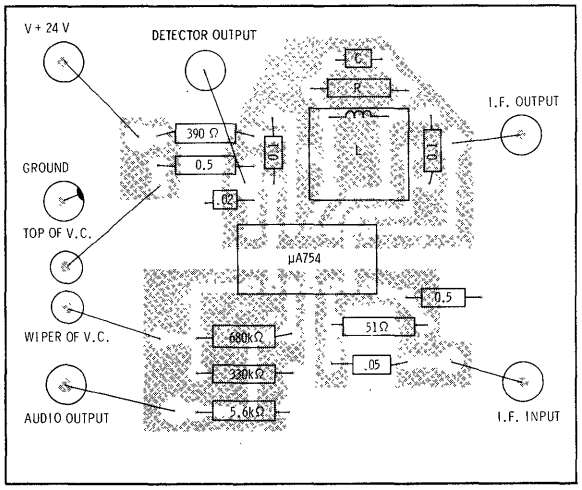
f_o	4.5 MHz	10.7 MHz
Deviation for 100% FM	±25 kHz	±75 kHz
AM Rejection at 1 mV	45 dB	35 dB
Limiting sensitivity	80 μV	150 μV
Recovered Audio at Detector Output	380 mV	160 mV
T.H.D. at Detector Output	1.0%	0.5%
Deviation for 2W output	±15 kHz	—

NOTES:
(1) Circuitry on printed circuit board shown inside dotted lines.
✲(2) Unused pins should be grounded for shielding.

SUGGESTED CIRCUIT LAYOUT



COPPER SIDE



COMPONENT SIDE

μA757

GAIN CONTROLLED IF AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

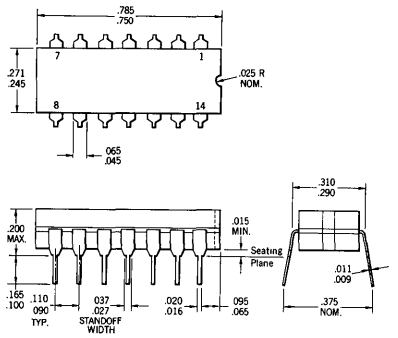
GENERAL DESCRIPTION — The μA757 is a high performance, gain-controlled IF amplifier constructed on a silicon chip using the Fairchild Planar* epitaxial process. The amplifier contains two sections which may be operated independently, or in cascade, from audio frequencies to 25 MHz. The μA757 is intended primarily as a gain-controlled, intermediate-frequency amplifier in AM and FM communications receivers. It also has excellent performance when operated in FM receivers as a limiting-amplifier.

- **70 dB GAIN AT 10.7 MHz**
- **70 dB AGC RANGE AT 10.7 MHz**
- **300 mV SIGNAL HANDLING CAPABILITY AT INPUT**
- **CONSTANT INPUT AND OUTPUT IMPEDANCE WITH AGC**
- **STABLE GAIN WITH SUPPLY VOLTAGE AND TEMPERATURE AT ALL LEVELS OF GAIN REDUCTION.**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+15 V
Voltage at any Output Terminal	+24 V
Voltage at either AGC Terminal (Note 1)	±12 V
Differential Voltage at either Input (Pins 1 and 14, Pins 2 and 10)	±5 V
Internal Power Dissipation (Note 2)	670 mW
Storage Temperature Range	
Ceramic DIP	−65°C to +150°C
Operating Temperature Range	
Military (312 grade)	−55°C to +125°C
Commercial (393 grade)	0°C to +70°C
Lead Temperature	
Ceramic DIP (Soldering 60 seconds)	300°C

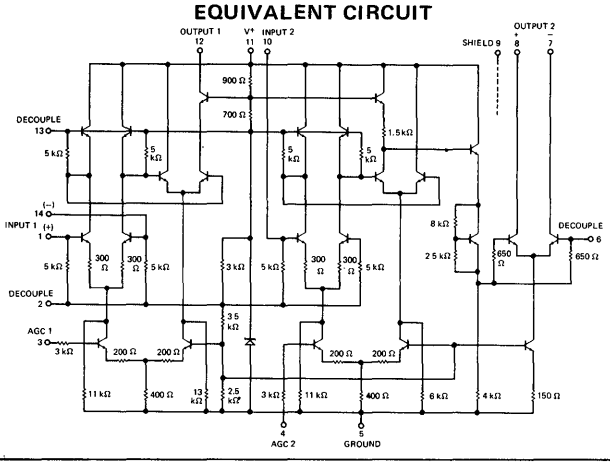
PHYSICAL DIMENSIONS
in accordance with JEDEC (TO-116) outline



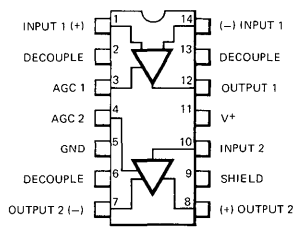
NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

ORDER PART NOS: U6A7757312
U6A7757393

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



Notes on following pages.

*Planar is a patented Fairchild process.

T_A = +25°C, 312 GRADE

ELECTRICAL CHARACTERISTICS (V^+ = +12 V, unless otherwise specified)

PARAMETERS	CONDITIONS	TEST CIRCUIT	MIN.	TYP.	MAX.	UNITS
Supply Current	$V_{AGC\ 1,2}$ = +0.8 V	1		13	17	mA
	$V_{AGC\ 1,2}$ = +3.0 V			17	20	mA
Internal Power Dissipation	$V_{AGC\ 1,2}$ = +0.8 V	1		170	210	mW
	$V_{AGC\ 1,2}$ = +3.0 V			200	240	mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2}$ = +0.8 V, f = 500 kHz	2	65	74		dB
	$V_{AGC\ 1,2}$ = +0.8 V, f = 10.7 MHz	2	60	70		dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2}$ = +1.7 V, f = 500 kHz	2	20	39	46	dB
	$V_{AGC\ 1,2}$ = +1.7 V, f = 10.7 MHz	2		37		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2}$ = +3.0 V, f = 500 kHz	2		2.0	10	dB
	$V_{AGC\ 1,2}$ = +3.0 V, f = 10.7 MHz	2		1.0	8	dB
Current into either AGC Terminal	$V_{AGC\ 1,2}$ = +3.0 V	1		15	50	μA
Gain Reduction Sensitivity	$V_{AGC\ 1,2}$ = +1.7 V, f = 500 kHz	2		50		dB/V
Input Voltage for −3 dB Limiting at Output	$V_{AGC\ 1,2}$ = +0.8 V, f = 500 kHz	2		0.5		mV
Intermodulation Products	Two-tone signal f_1 = 500 kHz, e_1 = 100 mV f_2 = 510 kHz, e_2 = 100 mV I_{OUT} = 1 mA p-p	2		−50		dB
SECTION 1						
Input Resistance at either Input Terminal	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz		3.0	5.0		kΩ
	$V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			4.5		kΩ
Input Capacitance at either Input Terminal	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz			2.5		pF
	$V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			2.2		pF
Output Resistance	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz			100		kΩ
	$V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			100		kΩ
Output Capacitance	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz			2.6		pF
	$V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			2.2		pF
Forward Transadmittance	$V_{AGC\ 1}$ = +0.8 V, f = 500 kHz			14		mmho
	$V_{AGC\ 1}$ = +0.8 V, f = 10.7 MHz			13		mmho
Peak-to-Peak Output Current	$V_{AGC\ 1}$ = +3.0 V, f = 500 kHz Output in full limiting		0.25	0.4		mA
Output Saturation Voltage	I_{OUT} = 0.1 mA, $V_{AGC\ 1}$ = +3.0 V			8.0	9.0	Volts
Noise Figure	R_S = 1.0 kΩ, f = 10.7 MHz			8.0		dB
Noise Figure	R_S = 1.0 kΩ, f = 500 kHz			8.0		dB
Interfering Signal Voltage at Input for 1.0% Cross Modulation	Carrier signal, f_c = 500 kHz Interfering signal, f_i = 510 kHz I_{OUT} = 0.5 mA p-p, $V_{AGC\ 1}$ = +0.8 V			15		mV
SECTION 2						
Input Resistance	$V_{AGC\ 2}$ = +0.8 V, f = 10.7 MHz		3.0	5.0		kΩ
	$V_{AGC\ 2}$ = +3.0 V, f = 10.7 MHz			4.5		kΩ
Input Capacitance	$V_{AGC\ 2}$ = +0.8 V, f = 10.7 MHz			2.5		pF
	$V_{AGC\ 2}$ = +3.0 V, f = 10.7 MHz			2.2		pF
Output Resistance at either Output Terminal	$V_{AGC\ 2}$ = +0.8 V, f = 10.7 MHz			26		kΩ
	$V_{AGC\ 2}$ = +3.0 V, f = 10.7 MHz			20		kΩ
Output Capacitance at either Output Terminal	$V_{AGC\ 2}$ = +0.8 V, f = 10.7 MHz			2.2		pF
	$V_{AGC\ 2}$ = +3.0 V, f = 10.7 MHz			2.5		pF
Forward Transadmittance	$V_{AGC\ 2}$ = +0.8 V, f = 500 kHz			440		mmho
	$V_{AGC\ 2}$ = +0.8 V, f = 10.7 MHz			280		mmho
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2}$ = +3.0 V		1.7	2.4	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2}$ = +3.0 V, f = 500 kHz Output in full limiting		3.8	4.8	7.0	mA
Output Saturation Voltage at either Output Terminal	I_{OUT} = 1.0 mA, $V_{AGC\ 2}$ = +3.0 V			5.0	6.0	Volts
Power Supply Sensitivity	V_S = 12 V to 15 V					
	0 dB Gain Reduction			0.5		dB/V
	30 dB Gain Reduction			0.8		dB/V
	60 dB Gain Reduction			1.0		dB/V

$T_A = +125°C$, 312 GRADE

ELECTRICAL CHARACTERISTICS ($V^+ = +12$ V, unless otherwise specified)

PARAMETERS	CONDITIONS	TEST CIRCUIT	MIN.	TYP.	MAX.	UNITS
Supply Current	$V_{AGC\ 1,2} = +0.8$ V	1		14	17	mA
	$V_{AGC\ 1,2} = +3.0$ V			17	20	mA
Internal Power Dissipation	$V_{AGC\ 1,2} = +0.8$ V	1		170	210	mW
	$V_{AGC\ 1,2} = +3.0$ V			200	240	mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2} = +0.8$ V, f = 500 kHz	2	55	71		dB
	$V_{AGC\ 1,2} = +0.8$ V, f = 10.7 MHz	2		62		dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2} = +1.7$ V, f = 500 kHz	2		35		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2} = +3.0$ V, f = 500 kHz	2		2.0	15	dB
	$V_{AGC\ 1,2} = +3.0$ V, f = 10.7 MHz	2		−1.0		dB
Current into either AGC Terminal	$V_{AGC\ 1,2} = +3.0$ V	1		15	50	μA
SECTION 1						
Peak-to-Peak Output Current	$V_{AGC\ 1} = +3.0$ V, f = 500 kHz Output in full limiting		0.2	0.4		mA
Output Saturation Voltage	$I_{OUT} = 0.1$ mA, $V_{AGC\ 1} = +3.0$ V			8.0	9.4	Volts
SECTION 2						
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V		1.7	2.8	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V, f = 500 kHz Output in full limiting		3.8	5.6	7.0	mA
Output Saturation Voltage at either Output Terminal	$I_{OUT} = 1.0$ mA, $V_{AGC\ 2} = +3.0$ V			6.0	7.0	Volts

$T_A = -55°C$, 312 GRADE

ELECTRICAL CHARACTERISTICS ($V^+ = +12$ V, unless otherwise specified)

PARAMETERS	CONDITIONS	TEST CIRCUIT	MIN.	TYP.	MAX.	UNITS
Supply Current	$V_{AGC\ 1,2} = +0.8$ V	1		10	17	mA
	$V_{AGC\ 1,2} = +3.0$ V			14	20	mA
Internal Power Dissipation	$V_{AGC\ 1,2} = +0.8$ V	1		120	210	mW
	$V_{AGC\ 1,2} = +3.0$ V			170	240	mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2} = +0.8$ V, f = 500 kHz	2	55	68		dB
	$V_{AGC\ 1,2} = +0.8$ V, f = 10.7 MHz	2		64		dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2} = +1.7$ V, f = 500 kHz	2		28		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2} = +3.0$ V, f = 500 kHz	2		2.0	15	dB
	$V_{AGC\ 1,2} = +3.0$ V, f = 10.7 MHz	2		−3.0		dB
Current into either AGC Terminal	$V_{AGC\ 1,2} = +3.0$ V	1		30	70	μA
SECTION 1						
Peak-to-Peak Output Current	$V_{AGC\ 1} = +3.0$ V, f = 500 kHz Output in full limiting		0.2	0.4		mA
Output Saturation Voltage	$I_{OUT} = 0.1$ mA, $V_{AGC\ 1} = +3.0$ V			8.0	9.0	Volts
SECTION 2						
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V		1.0	1.7	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2} = +3.0$ V, f = 500 kHz Output in full limiting		2.3	3.4	7.0	mA
Output Saturation Voltage at either Output Terminal	$I_{OUT} = 1.0$ mA, $V_{AGC\ 2} = +3.0$ V			4.0	6.0	Volts

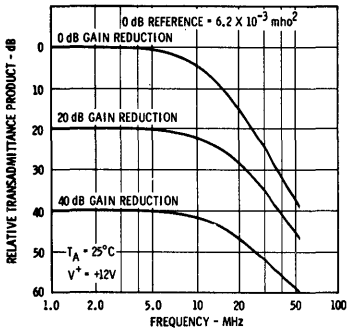
393 GRADE

ELECTRICAL CHARACTERISTICS (V^+ = +12 V, T_A = +25°C, unless otherwise specified)

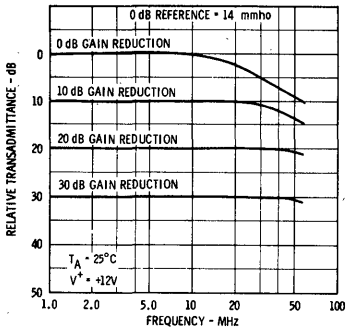
PARAMETERS	CONDITIONS	TEST CIRCUIT	MIN.	TYP.	MAX.	UNITS
Supply Current	$V_{AGC\ 1,2}$ = +1.0 V	1		14	17	mA
	$V_{AGC\ 1,2}$ = +3.0 V			18	22	mA
Internal Power Dissipation	$V_{AGC\ 1,2}$ = +1.0 V	1		170	210	mW
	$V_{AGC\ 1,2}$ = +3.0 V			220	270	mW
Voltage Gain at no Gain Reduction	$V_{AGC\ 1,2}$ = +1.0 V, f = 500 kHz	2	65	74		dB
	$V_{AGC\ 1,2}$ = +1.0 V, f = 10.7 MHz	2	60	70		dB
Voltage Gain at Partial Gain Reduction	$V_{AGC\ 1,2}$ = +1.7 V, f = 500 kHz	2	20	39	46	dB
	$V_{AGC\ 1,2}$ = +1.7 V, f = 10.7 MHz	2		37		dB
Voltage Gain at Full Gain Reduction	$V_{AGC\ 1,2}$ = +3.0 V, f = 500 kHz	2		2.0	10	dB
	$V_{AGC\ 1,2}$ = +3.0 V, f = 10.7 MHz	2		1.0	8	dB
Current into either AGC Terminal	$V_{AGC\ 1,2}$ = +3.0 V	1		15	50	μA
Gain Reduction Sensitivity	$V_{AGC\ 1,2}$ = +1.7 V, f = 500 kHz	2		50		dB/V
Input Voltage for −3 dB Limiting at Output	$V_{AGC\ 1,2}$ = +1.0 V, f = 500 kHz	2		0.5		mV
Intermodulation Products	Two-tone signal	2		−50		dB
	f_1 = 500 kHz, e_1 = 100 mV					
	f_2 = 510 kHz, e_2 = 100 mV					
	I_{OUT} = 1 mA p-p					
SECTION 1						
Input Resistance at either Input Terminal	$V_{AGC\ 1}$ = +1.0 V, f = 10.7 MHz		3.0	5.0		kΩ
	$V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			4.5		kΩ
Input Capacitance at either Input Terminal	$V_{AGC\ 1}$ = +1.0 V, f = 10.7 MHz			2.5		pF
	$V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			2.2		pF
Output Resistance	$V_{AGC\ 1}$ = +1.0 V, f = 10.7 MHz			100		kΩ
	$V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			100		kΩ
Output Capacitance	$V_{AGC\ 1}$ = +1.0 V, f = 10.7 MHz			2.6		pF
	$V_{AGC\ 1}$ = +3.0 V, f = 10.7 MHz			2.2		pF
Forward Transadmittance	$V_{AGC\ 1}$ = +1.0 V, f = 500 kHz			14		mmho
	$V_{AGC\ 1}$ = +1.0 V, f = 10.7 MHz			13		mmho
Peak-to-Peak Output Current	$V_{AGC\ 1}$ = +3.0 V, f = 500 kHz		.25	0.4		mA
	Output in full limiting					
Output Saturation Voltage	I_{OUT} = 0.1 mA, $V_{AGC\ 1}$ = +3.0 V			8.0	9.0	Volts
Noise Figure	R_S = 1.0 kΩ, f = 10.7 MHz			8.0		dB
Noise Figure	R_S = 1.0 kΩ, f = 500 kHz			8.0		dB
Interfering Signal Voltage at Input	Carrier signal, f_c = 500 kHz			15		mV
for 1.0% Cross Modulation	Interfering signal, f_i = 510 kHz					
	I_{OUT} = 0.5 mA p-p, $V_{AGC\ 1}$ = +1.0 V					
SECTION 2						
Input Resistance	$V_{AGC\ 2}$ = +1.0 V, f = 10.7 MHz		3.0	5.0		kΩ
	$V_{AGC\ 2}$ = +3.0 V, f = 10.7 MHz			4.5		kΩ
Input Capacitance	$V_{AGC\ 2}$ = +1.0 V, f = 10.7 MHz			2.5		pF
	$V_{AGC\ 2}$ = +3.0 V, f = 10.7 MHz			2.2		pF
Output Resistance at either Output Terminal	$V_{AGC\ 2}$ = +1.0 V, f = 10.7 MHz			26		kΩ
	$V_{AGC\ 2}$ = +3.0 V, f = 10.7 MHz			20		kΩ
Output Capacitance at either Output Terminal	$V_{AGC\ 2}$ = +1.0 V, f = 10.7 MHz			2.2		pF
	$V_{AGC\ 2}$ = +3.0 V, f = 10.7 MHz			2.5		pF
Forward Transadmittance	$V_{AGC\ 2}$ = +1.0 V, f = 500 kHz			440		mmho
	$V_{AGC\ 2}$ = +1.0 V, f = 10.7 MHz			280		mmho
Quiescent Output Current at either Output Terminal	$V_{AGC\ 2}$ = +3.0 V		1.7	2.4	3.5	mA
Peak-to-Peak Current at either Output Terminal	$V_{AGC\ 2}$ = +3.0 V, f = 500 kHz		3.8	4.8	7.0	mA
	Output in full limiting					
Output Saturation Voltage at either Output Terminal	I_{OUT} = 1.0 mA, $V_{AGC\ 2}$ = +3.0 V			5.0	6.0	Volts
Power Supply Sensitivity	V_S = 12 V to 15 V					
	0 dB Gain Reduction			0.5		dB/V
	30 dB Gain Reduction			0.8		dB/V
	60 dB Gain Reduction			1.0		dB/V

TYPICAL PERFORMANCE CURVES

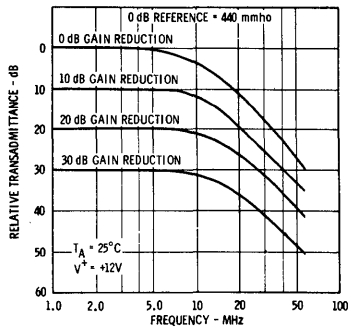
PRODUCT OF SECTIONS 1 AND 2 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



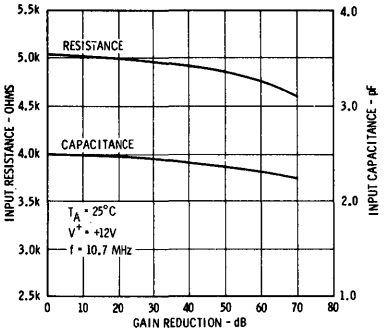
SECTION 1 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



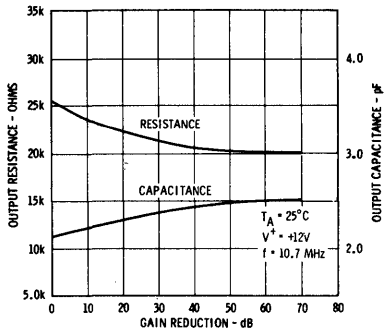
SECTION 2 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



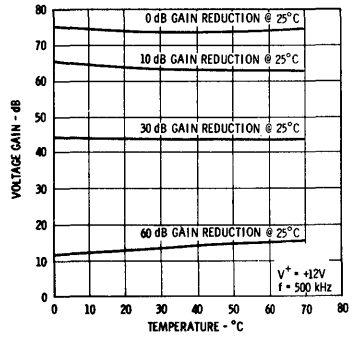
SECTION 1 AND 2 INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF GAIN REDUCTION



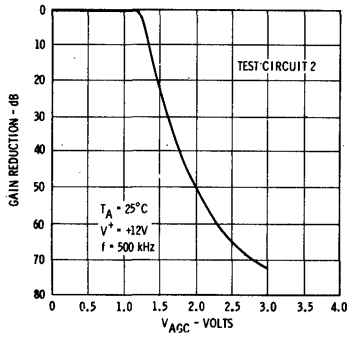
SECTION 2 OUTPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF GAIN REDUCTION



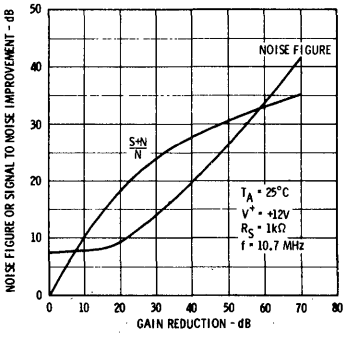
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



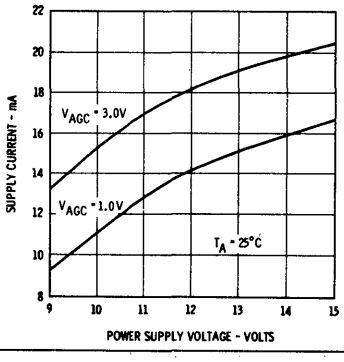
GAIN REDUCTION AS A FUNCTION OF GAIN CONTROL VOLTAGE



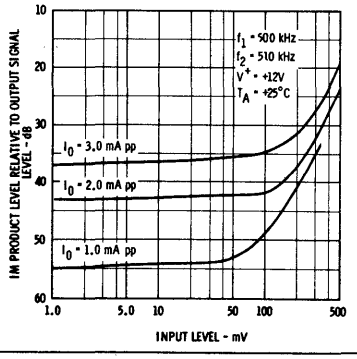
SIGNAL TO NOISE RATIO IMPROVEMENT AND NOISE FIGURE AS A FUNCTION OF GAIN REDUCTION



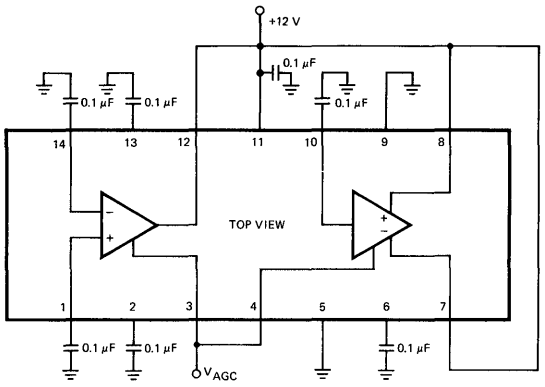
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



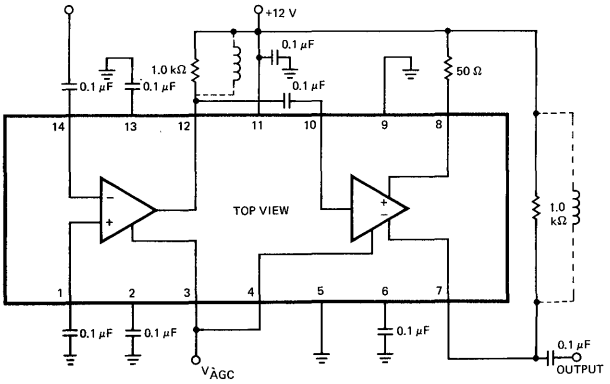
TWO TONE IM DISTORTION PRODUCTS AS A FUNCTION OF INPUT SIGNAL LEVEL



TEST CIRCUIT 1



TEST CIRCUIT 2



NOTE
For 10.7 MHz measurements, interstage capacitance and Section 2 output capacitance are tuned out.
Pin 9 should be connected to GND

NOTES
1. For supply voltages less than +12 V, the absolute maximum voltage at either AGC terminal is equal to the supply voltage.
2. Rating applies to ambient temperatures up to 70° C. Above 70° C ambient derate linearly at 8.3 mW/° C.

μA760

HIGH SPEED DIFFERENTIAL COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

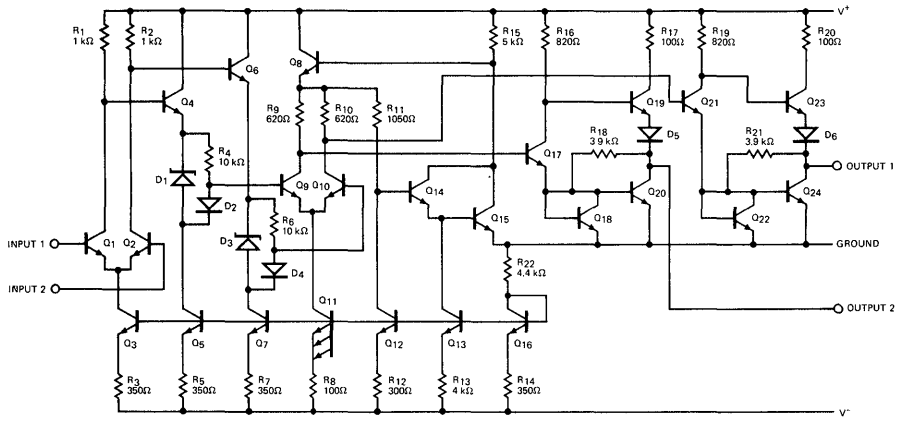
GENERAL DESCRIPTION – The μA760 is a differential voltage comparator offering considerable speed improvement over the μA710 family and operation from symmetric supplies of from ±4.5 volts to ±6.5 volts. Complementary outputs are TTL compatible with a minimum sink capability of two gate loads.

- **GUARANTEED HIGH SPEED**
- **GUARANTEED DELAY MATCHING ON BOTH OUTPUTS**
- **COMPLEMENTARY TTL COMPATIBLE OUTPUTS**
- **HIGH SENSITIVITY**
- **USES STANDARD SUPPLY VOLTAGES**

ABSOLUTE MAXIMUM RATINGS

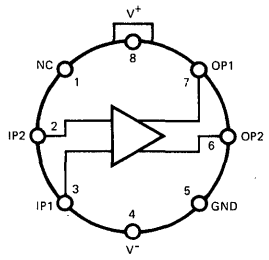
Positive Supply Voltage		+8 V
Negative Supply Voltage		-8 V
Peak Output Current		10 mA
Differential Input Voltage		±5 V
Input Voltage		$\pm V_S$
Internal Power Dissipation (Note 1)	Metal Can	500 mW
	Ceramic DIP	670 mW
	Mini DIP	310 mW
Operating Temperature Range		
Military (312 Grade)		-55°C to 125°C
Commercial (393 Grade)		0°C to 70°C
Storage Temperature Range		
Metal Can and DIP		-65°C to 150°C
Mini DIP		-55°C to 125°C

EQUIVALENT CIRCUIT



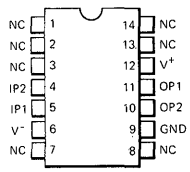
CONNECTION DIAGRAM

8 LEAD METAL CAN
(TOP VIEW)



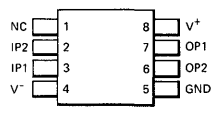
ORDER PART NOS.: PRODUCT CODE
U5B7760312
U5B7760393

14 LEAD DIP
(TOP VIEW)



ORDER PART NOS.: PRODUCT CODE
U6A7760312
U6A7760393

MINI DIP
(TOP VIEW)



ORDER PART NO.: PRODUCT CODE
U9T7760393

Notes on following pages.

312 GRADE

ELECTRICAL CHARACTERISTICS (V_S = ±4.5V to ±6.5V, T_A = −55°C to +125°C, T_A = 25°C for typical figures unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
Input Offset Current			0.5	7.5	μA
Input Bias Current			8.0	60	μA
Output Resistance	$V_{OUT} = V_{OH}$		100		Ω
Response Time	Note 2, T_A = 25°C		18	30	ns
	Note 3, T_A = 25°C			25	ns
	Note 4		16		ns
Response Time Difference between outputs					
$t_{pd+1} - t_{pd-2}$	Note 2, T_A = 25°C			5.0	ns
$t_{pd+2} - t_{pd-1}$	Note 2, T_A = 25°C			5.0	ns
$t_{pd+1} - t_{pd+2}$	Note 2, T_A = 25°C			7.5	ns
$t_{pd-1} - t_{pd-2}$	Note 2, T_A = 25°C			7.5	ns
Input Resistance	f = 1 MHz		12		kΩ
Input Capacitance	f = 1 MHz		8.0		pF
Average Temperature Coefficient of Input Offset Voltage	R_S = 50Ω, T_A = −55°C to T_A = +125°C		3.0		μV/°C
Average Temperature Coefficient of Input Offset Current	T_A = 25°C to T_A = +125°C		2.0		nA/°C
	T_A = 25°C to T_A = −55°C		7.0		nA/°C
Input Voltage Range	V_S = ±6.5V	±4.0	±4.5		V
Differential Input Voltage Range			±5.0		V
Positive Output Level	$0 \leq I_{OUT} \leq 5.0$ mA				
	V_S = ±5.0V	2.4	3.2		V
	I_{OUT} = 80 μA, V_S = ±4.5V	2.4	3.0		V
Negative Output Level	I_{SINK} = 3.2 mA		0.25	0.4	V
Positive Supply Current	V_S = ±6.5V		18	32	mA
Negative Supply Current	V_S = ±6.5V		9.0	16	mA

393 GRADE

ELECTRICAL CHARACTERISTICS (V_S = ±4.5V to ±6.5V, T_A = 0°C to +70°C, T_A = 25°C for typical figures unless otherwise specified.)

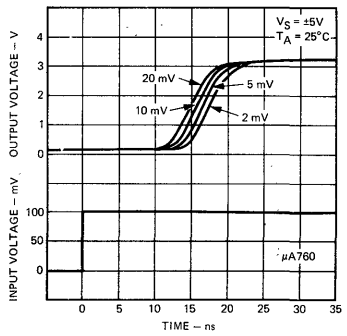
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		1.0	6.0	mV
Input Offset Current			0.5	7.5	μA
Input Bias Current			8.0	60	μA
Output Resistance	$V_{OUT} = V_{OH}$		100		Ω
Response Time	Note 2, T_A = 25°C		18	30	ns
	Note 3, T_A = 25°C			25	ns
	Note 4		16		ns
Response Time Difference between outputs					
$t_{pd+1} - t_{pd-2}$	Note 2, T_A = 25°C			5.0	ns
$t_{pd+2} - t_{pd-1}$	Note 2, T_A = 25°C			5.0	ns
$t_{pd+1} - t_{pd+2}$	Note 2, T_A = 25°C			10	ns
$t_{pd-1} - t_{pd-2}$	Note 2, T_A = 25°C			10	ns
Input Resistance	f = 1 MHz		12		kΩ
Input Capacitance	f = 1 MHz		8.0		pF
Average Temperature Coefficient of Input Offset Voltage	R_S = 50Ω, T_A = 0°C to T_A = +70°C		3.0		μV/°C
Average Temperature Coefficient of Input Offset Current	T_A = 25°C to T_A = +70°C		5.0		nA/°C
	T_A = 25°C to T_A = 0°C		10		nA/°C
Input Voltage Range	V_S = ±6.5V	±4.0	±4.5		V
Differential Input Voltage Range			±5.0		V
Positive Output Level	$0 \leq I_{OUT} \leq 5.0$ mA				
	V_S = ±5.0V	2.4	3.2		V
	I_{OUT} = 80 μA, V_S = ±4.5V	2.5	3.0		V
Negative Output Level	I_{SINK} = 3.2 mA		0.25	0.4	V
Positive Supply Current	V_S = ±6.5V		18	34	mA
Negative Supply Current	V_S = ±6.5V		9.0	16	mA

NOTES

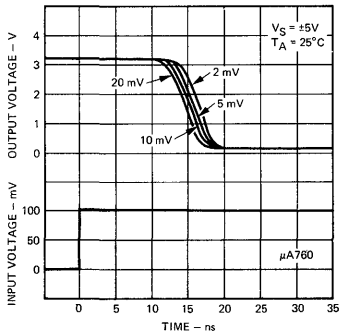
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for Metal Can and 8.3 mW/°C for the Ceramic DIP.
2. Response time measured from the 50% point of a 30 mVp-p 10 MHz sinusoidal input to the 50% point of the output.
3. Response time measured from the 50% point of a 2 Vp-p 10 MHz sinusoidal input to the 50% point of the output.
4. Response time measured from the start of a 100 mV input step with 5 mV overdrive to the time when the output crosses the logic threshold.

TYPICAL PERFORMANCE CURVES

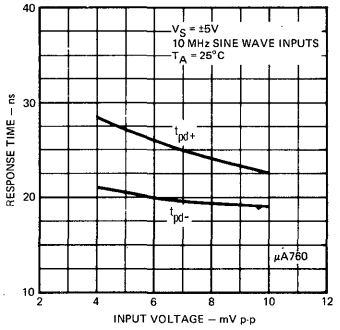
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



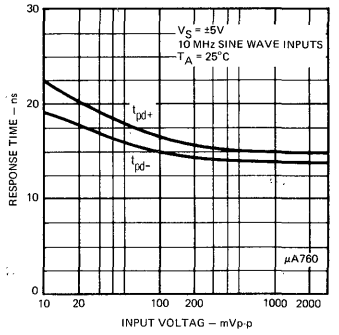
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



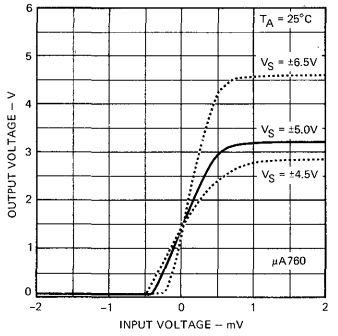
RESPONSE TIME AS A FUNCTION OF INPUT VOLTAGE



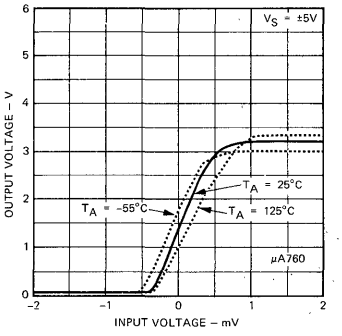
RESPONSE TIME AS A FUNCTION OF INPUT VOLTAGE



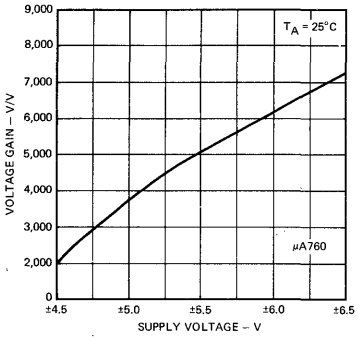
VOLTAGE TRANSFER CHARACTERISTIC



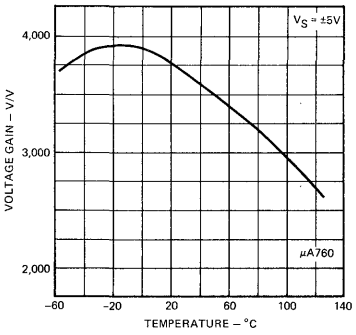
VOLTAGE TRANSFER CHARACTERISTIC



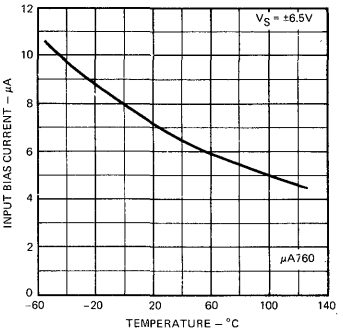
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



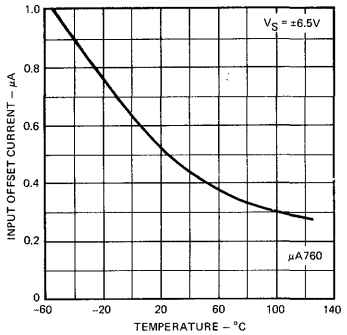
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



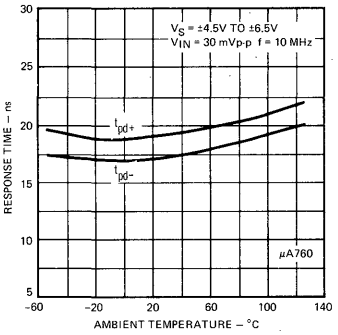
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



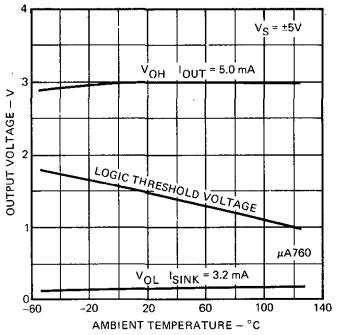
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



RESPONSE TIME AS A FUNCTION OF AMBIENT TEMPERATURE

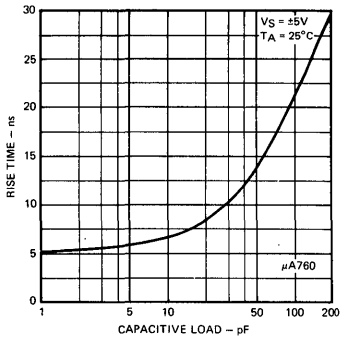


OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE

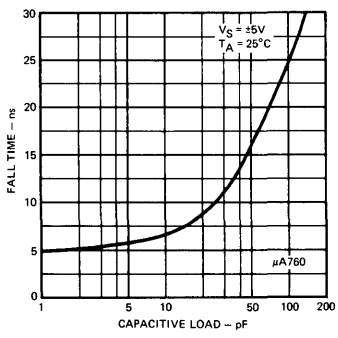


TYPICAL PERFORMANCE CURVES (Cont.)

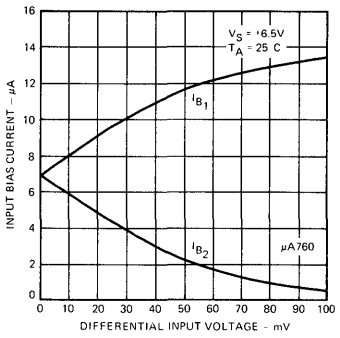
RISE TIME AS A FUNCTION OF CAPACITIVE LOAD



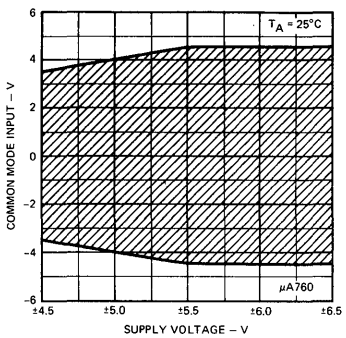
FALL TIME AS A FUNCTION OF CAPACITIVE LOAD



INPUT BIAS CURRENT AS A FUNCTION OF DIFFERENTIAL INPUT VOLTAGE



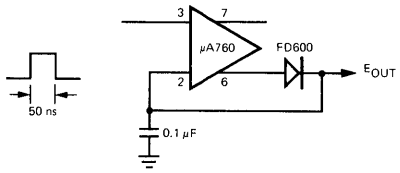
COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



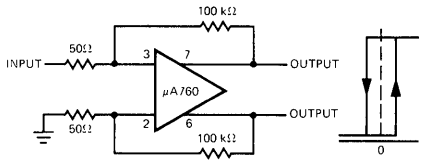
APPLICATIONS

Pin numbers shown are only for Metal Can and Mini-DIP.

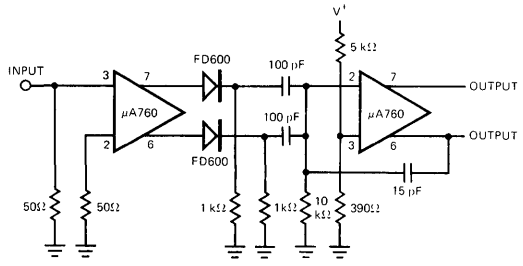
FAST POSITIVE PEAK DETECTOR



LEVEL DETECTOR WITH HYSTERESIS

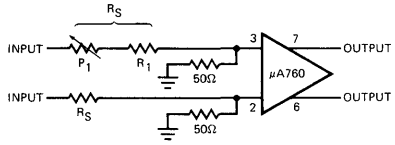


ZERO CROSSING DETECTOR



Total delay = 30 ns
Input frequency = 300 Hz to 3 MHz
Minimum input voltage = 20 mVp-p

LINE RECEIVER WITH HIGH COMMON MODE RANGE



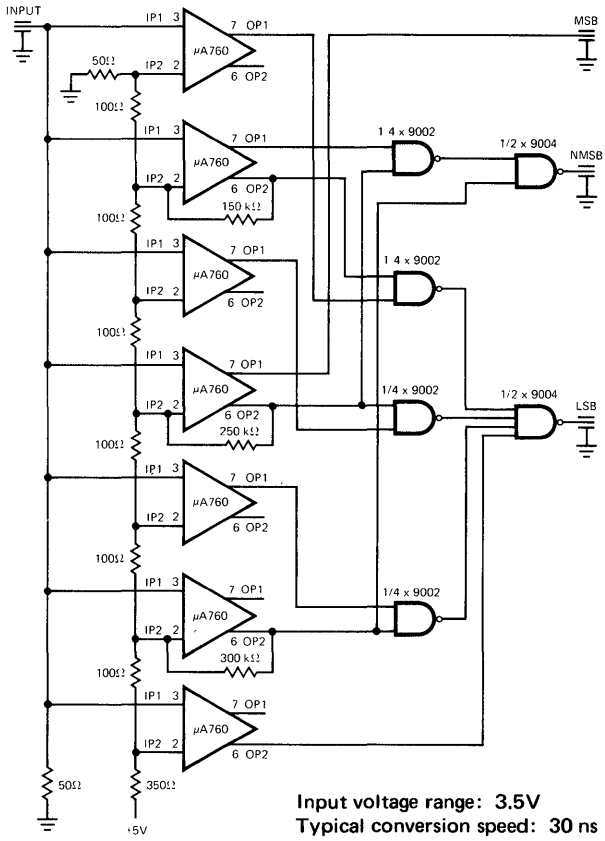
Common mode range = $\pm 4 \times \frac{R_S}{50}$ V

Differential Input sensitivity = $5 \times \frac{R_S}{50}$ mV

P_1 must be adjusted for optimum common mode rejection.

For R_S = 200Ω
Common mode range = ±16V
Sensitivity = 20 mV

HIGH SPEED 3-BIT A/D CONVERTER



Input voltage range: 3.5V
Typical conversion speed: 30 ns

μA767
FM STEREO MULTIPLEX DECODER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

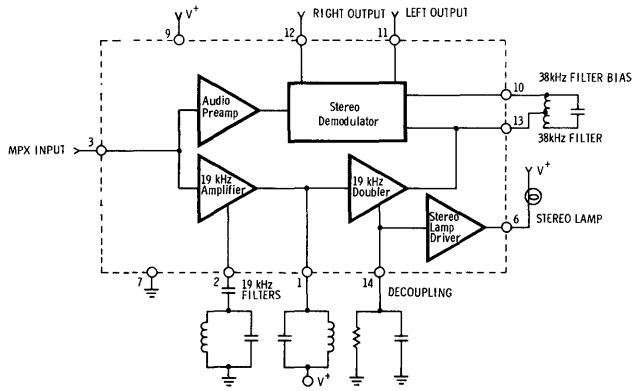
GENERAL DESCRIPTION—The μA767 is a monolithic FM Stereo Multiplex Decoder System constructed on a single silicon chip using the Fairchild Planar* Epitaxial Process. This integrated circuit accomplishes the demodulation of a Stereo Multiplex Signal into the Right and Left audio channels while inherently suppressing SCA frequency components. Internal provision is made for driving an external stereo mode indicator lamp. The excellent performance, wide supply range and low external parts requirement makes the μA767 suitable for all line-operated and automotive FM Stereo Multiplex applications. For Stereo Decoding including interstation audio muting and stereo/mode switching, see the μA729 and μA732 data sheets. See Note 1.

- **45 dB CHANNEL SEPARATION**
- **55 dB STORECAST REJECTION WITHOUT SCA FILTERS**
- **HIGH-CURRENT STEREO INDICATOR LAMP DRIVER**
- **OPERATION WITH 8 V TO 14 V SUPPLIES**

ABSOLUTE MAXIMUM RATINGS

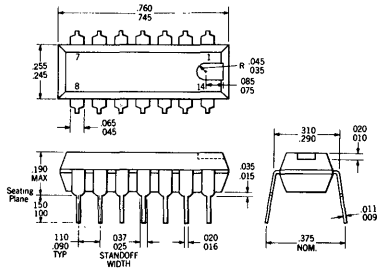
Supply Voltage (Note 2)		+15 V
Voltage at Stereo Lamp Driver Terminal		+22 V
Current into Stereo Lamp Driver Terminal (Note 3)		100 mA
Internal Power Dissipation		
Ceramic DIP		670 mW
Silicone DIP		340 mW
Operating Temperature Range		0°C to + 70°C
Storage Temperature Range	9A Package	-55°C to + 125°C
	6A Package	-65°C to + 150°C
Lead Temperature (Soldering, 10 seconds)	9A Package	+ 260°C
(Soldering, 60 seconds)	6A Package	+ 300°C

BLOCK DIAGRAM



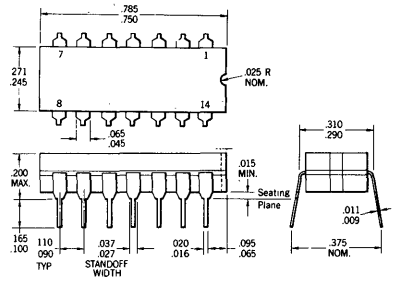
PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-116) outline
14 LEAD SILICONE DUAL IN-LINE



ORDER PART NO. U9A7767394

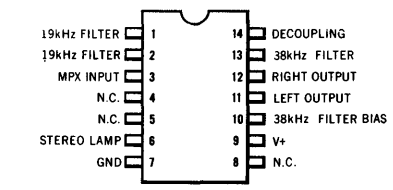
In accordance with JEDEC (TO-116) outline
14 LEAD CERAMIC DUAL IN-LINE



ORDER PART NO. U6A7767394

NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 0.9 gram for 9A
2.0 gram for 6A package

CONNECTION DIAGRAM
(TOP VIEW)



Notes on following page.

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = + 12 V, 200 mV RMS Standard Stereo Multiplex signal applied to Input, unless otherwise specified (Note 4). Refer to Test Circuit of Figure 1.)

PARAMETER	MIN.	TYP.	MAX.	UNITS
Supply Current		12	18	mA
Input Resistance	12	20		kΩ
Stereo Separation				
f = 100 Hz		40		dB
f = 1 kHz	30	45		dB
f = 10 kHz	20	40		dB
Channel Balance (Monaural Input)		0.2		dB
Total Harmonic Distortion		0.5	1.0	%
Voltage Gain		1.0		V/V
67 kHz Storecast Rejection (Note 5)		55		dB
19 kHz Pilot Level Required at Input for:				
Stereo Indicator Lamp on		12	22	mV RMS
Stereo Indicator Lamp off	4.0	8.0		mV RMS
High Frequency Audio Components in Left and Right Outputs (dB below 1 kHz output)				
19 kHz		30		dB
38 kHz		25		dB

NOTES:

(1) The μA767 is a plug-in replacement for the MC1307.

(2) Power supply transients up to 22V are permissible for periods of 15 seconds. However, extended operation at voltages greater than 15V should be avoided as the maximum allowable internal power dissipation for this device may be exceeded.

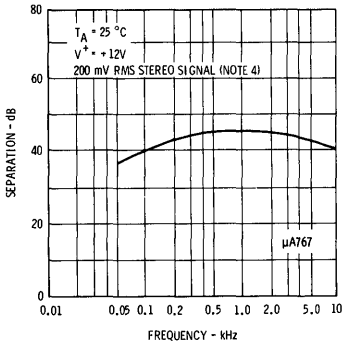
(3) Rating applies to steady state current. Maximum permissible surge current during turn-on of the Stereo Indicator Lamp is 500 mA.

(4) "Standard Stereo Multiplex Signal" here refers to a 200mV RMS (0.56V p-p) composite stereo signal including 10% pilot with L=1 and R = 1 as described in the FCC Rules on FM Broadcasting.

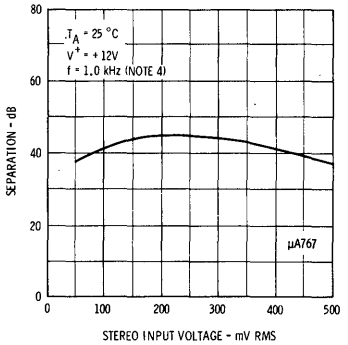
(5) Measured with a stereo composite signal consisting of 80% stereo, 10% pilot and 10% SCA as defined in the FCC Rules on FM Broadcasting.

TYPICAL PERFORMANCE CURVES

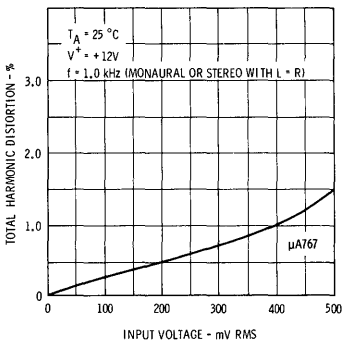
SEPARATION VERSUS AUDIO FREQUENCY



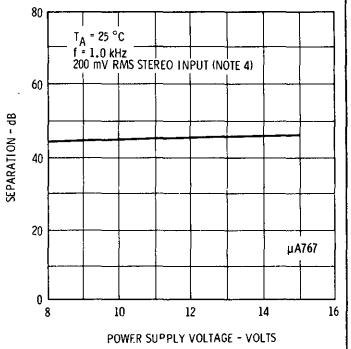
1 kHz SEPARATION VERSUS COMPOSITE INPUT VOLTAGE



1 kHz DISTORTION VERSUS INPUT VOLTAGE



1 kHz SEPARATION VERSUS POWER SUPPLY VOLTAGE



μA767 FM STEREO MULTIPLEX DECODER TEST CIRCUIT AND TYPICAL APPLICATION

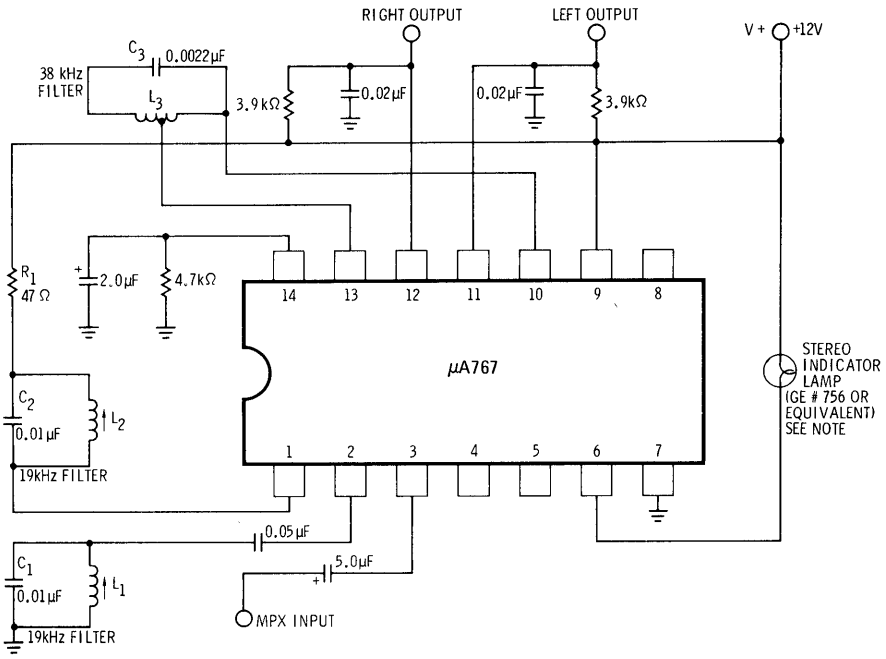
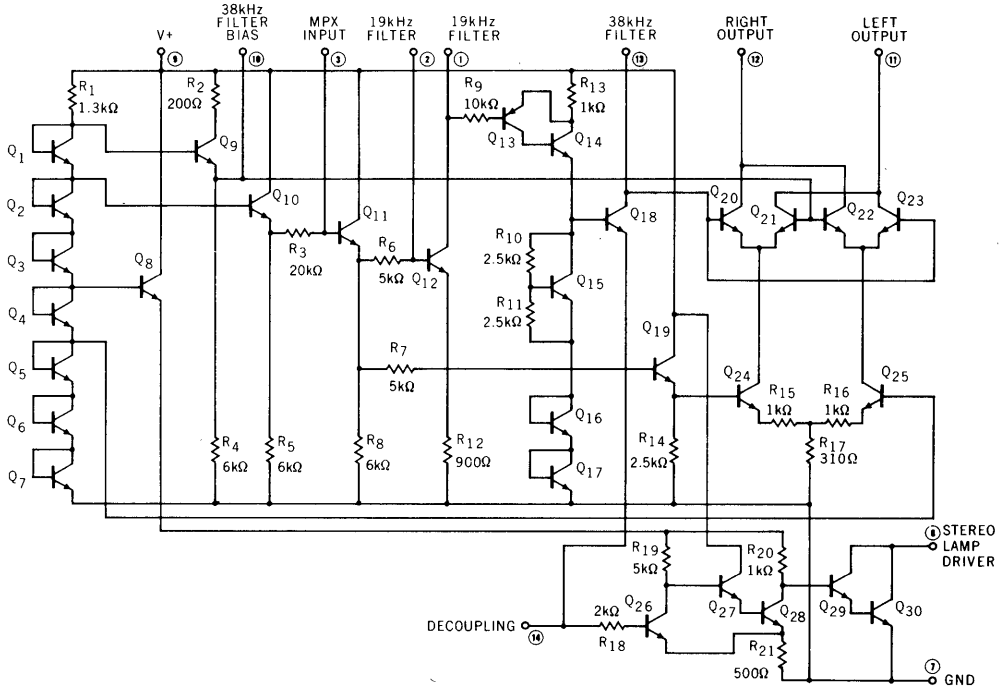


Fig. 1

NOTES:
(1) Capacitors C_1, C_2, and C_3 should be polystyrene or mylar.
(2) Coils L_1 and L_2 are 7.0 mH nominal with Q_{UL} = 60 (Miller #1361 or equivalent).
(3) Coil L_3 is 8.0 mH nominal with Q_{UL} = 80, tapped at 10:1 turns ratio. (Miller #1362 or equivalent).
(4) Resistor R_1 can be increased (or decreased) in value to increase (or decrease) the 19kHz sensitivity.

μA767 FM STEREO MULTIPLEX DECODER EQUIVALENT CIRCUIT



μA776

MULTI-PURPOSE PROGRAMMABLE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

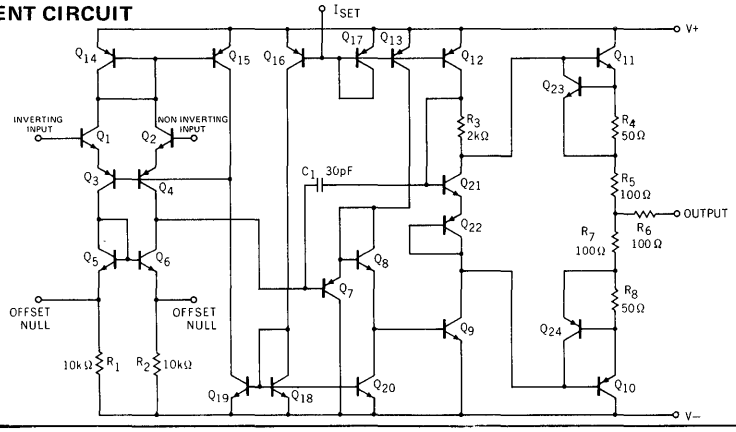
DESCRIPTION – The μA776 Programmable Operational Amplifier is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. High input impedance, low supply currents, and low input noise over a wide range of operating supply voltages coupled with programmable electrical characteristics result in an extremely versatile amplifier for use in high accuracy, low power consumption analog applications. Input voltage and current noise, power consumption, and input current can be optimized by a single resistor or current source that sets the chip quiescent current for nano-watt power consumption or for characteristics similar to the μA741. Internal frequency compensation, absence of latch up high slew rate and short circuit current protection assure ease of use in long time integrators, active filters, and sample and hold circuits.

- **MICROPOWER CONSUMPTION**
- **±1.2V to ±18V OPERATION**
- **NO FREQUENCY COMPENSATION REQUIRED**
- **LOW INPUT BIAS CURRENTS**
- **WIDE PROGRAMMING RANGE**
- **HIGH SLEW RATE**
- **LOW NOISE**
- **SHORT CIRCUIT PROTECTION**
- **OFFSET NULL CAPABILITY**
- **NO LATCH UP**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Ceramic DIP	670 mW
Silicone DIP	340 mW
Mini DIP	310 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage Between Offset Null and V–	±0.5 V
I_{SET} (Maximum Current at I_{SET})	200 μA
V_{SET} (Maximum Voltage to Ground at I_{SET})	$(V^+ - 1.0\ V) \leqslant V_{SET} \leqslant V^+$
Storage Temperature Range	
Metal Can, Ceramic DIP	–65°C to +150°C
Mini DIP and Silicone DIP	–55°C to +125°C
Operating Temperature Range	
Military (312 Grade)	–55°C to +125°C
Commercial (393 Grade)	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	
Metal Can, Ceramic DIP	300°C
Mini DIP and Silicone DIP	260°C
Output Short-Circuit Duration (Note 3)	Indefinite

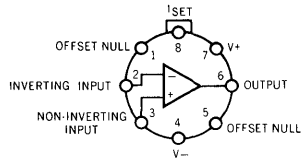
EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS

8 LEAD METAL CAN

(TOP VIEW)

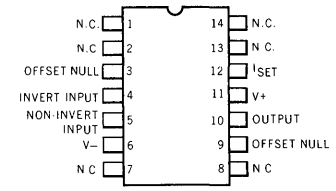


PRODUCT CODE

ORDER PART NOS: **U5B7776312**
U5B7776393

14 LEAD DIP

(TOP VIEW)

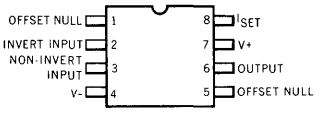


ORDER PART NOS:
FOR CERAMIC DIP : PRODUCT CODE
U6A7776312
U6A7776393

FOR SILICONE DIP : PRODUCT CODE
U9A7776393

MINI DIP

(TOP VIEW)



PRODUCT CODE:

ORDER PART NO.: **U9T7776393**

Notes on following page.

*Planar is a patented Fairchild process.

±3 VOLT OPERATION FOR 312 GRADE

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Unless Otherwise Specified)

		I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	5.0		2.0	5.0	mV
Input Offset Current			0.7	3.0		2.0	15	nA
Input Bias Current			2.0	7.5		15	50	nA
Input Resistance			50			5.0		MΩ
Input Capacitance			2.0			2.0		pF
Offset Voltage Adjustment Range			9.0			18		mV
Large Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT}=±1V	50k	200k					V/V
	$R_L \geq 5k\Omega$, V_{OUT}=±1V				50k	200k		V/V
Output Resistance			5k			1k		Ω
Output Short-Circuit Current			2.0			5.0		mA
Supply Current			13	20		100	130	μA
Power Consumption			78	120		600	720	μW
Transient Response (unity gain)	V_{IN} = 20mV, $R_L \geq 5k\Omega$, C_L=100pF							
Risetime			3.0			0.6		μs
Overshoot			0			5		%
Slew Rate	$R_L \geq 5k\Omega$		0.03			0.35		V/μs
The following specifications apply for $-55°C \leq T_A \leq 125°C$								
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			6.0	mV
Input Offset Current	T_A = +125°C			5.0			15	nA
	T_A = −55°C			10			40	nA
Input Bias Current	T_A = +125°C			7.5			50	nA
	T_A = −55°C			20			120	nA
Input Voltage Range		±1.0			±1.0			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	86		70	86		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		25	150		25	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT}=±1V	25k						V/V
	$R_L \geq 5k\Omega$, V_{OUT}=±1V				25k			V/V
Output Voltage Swing	$R_L \geq 75k\Omega$	±2.0	±2.4					V
	$R_L \geq 5k\Omega$				±1.9	±2.1		V
Supply Current				25			135	μA
Power Consumption				150			750	μW

NOTES

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for Metal Can, 8.3 mW/°C for the Ceramic DIP, 6.3 mW/°C for the Silicone DIP and 5.6 mW/°C for the Mini DIP package.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature for $I_{SET} \leq 30\ \mu A$.

±15 VOLT OPERATION FOR 312 GRADE

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Unless Otherwise Specified)

		I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	5.0		2.0	5.0	mV
Input Offset Current	$R_S \leq 10k\Omega$		0.7	3.0		2.0	15	nA
Input Bias Current			2.0	7.5		15	50	nA
Input Resistance			50			5.0		MΩ
Input Capacitance			2.0			2.0		pF
Offset Voltage Adjustment Range			9.0			18		mV
Large-Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT} = ±10V	200k	400k					V/V
	$R_L \geq 5k\Omega$, V_{OUT} = ±10V				100k	400k		V/V
Output Resistance			5.0k			1.0k		Ω
Output Short-Circuit Current			2.0			10		mA
Supply Current			20	25		125	150	μA
Power Consumption				0.75			4.5	mW
Transient Response (unity gain)	V_{IN}=20mV, $R_L \geq 5k\Omega$, $C_L \leq 100pF$							
Risetime			1.6			0.35		μs
Overshoot			0			10		%
Slew Rate	$R_L \geq 5k\Omega$		0.1			0.8		V/μs
Output Voltage Swing	$R_L \geq 75k\Omega$	±12	±14					V
	$R_L \geq 5k\Omega$				±10	±13		V
The following specifications apply	$-55°C \leq T_A \leq +125°C$							
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			6.0	mV
Input Offset Current	T_A = +125°C			5.0			15	nA
	T_A = −55°C			10			40	nA
Input Bias Current	T_A = +125°C			7.5			50	nA
	T_A = −55°C			20			120	nA
Input Voltage Range		±10			±10			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		25	150		25	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT}=±10V	100k			75k			V/V
Output Voltage Swing	$R_L \geq 75k\Omega$	±10			±10			V
Supply Current				30			170	μA
Power Consumption				0.9			5.1	mW

±3 VOLT OPERATION FOR 393 GRADE

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Unless Otherwise Specified)

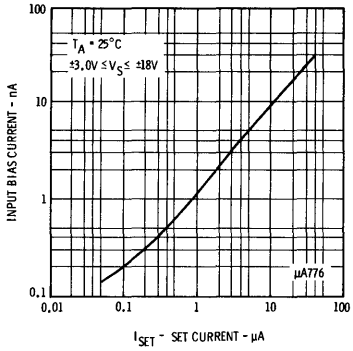
		I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	6.0		2.0	6.0	mV
Input Offset Current			0.7	6.0		2.0	25	nA
Input Bias Current			2.0	10		15	50	nA
Input Resistance			50			5.0		MΩ
Input Capacitance			2.0			2.0		pF
Offset Voltage Adjustment Range			9.0			18		mV
Large-Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT}=±1V	25k	200k					V/V
	$R_L \geq 5k\Omega$, V_{OUT}=±1V				25 k	200k		V/V
Output Resistance			5.0			1.0		kΩ
Output Short-Circuit Current			2.0			5.0		mA
Supply Current			13	20		100	130	μA
Power Consumption			78	120		600	720	μW
Transient Response (unity gain)	V_{IN} = 20mV, $R_L \geq 5k\Omega$, C_L = 100pF							
Risetime			3.0			0.6		μs
Overshoot			0			5		%
Slew Rate	$R_L \geq 5k\Omega$		0.03			0.35		V/μs
The following specifications apply for $0°C \leq T_A \leq +70°C$								
Input Offset Voltage	$R_S \leq 10k\Omega$			7.5			7.5	mV
Input Offset Current	T_A = +70°C			6.0			25	nA
	T_A = 0°C			10			40	nA
Input Bias Current	T_A = +70°C			10			50	nA
	T_A = 0°C			20			100	nA
Input Voltage Range		±1.0			±1.0			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	86		70	86		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		25	200		25	200	μV/V
Large-Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT}=±1V	25k						V/V
	$R_L \geq 5k\Omega$, V_{OUT}=±1V				25k			V/V
Output Voltage Swing	$R_L \geq 75k\Omega$	±2.0	±2.4					V
	$R_L \geq 5k\Omega$				±2.0	±2.1		V
Supply Current				25			135	μA
Power Consumption				150			750	μW

±15 VOLT OPERATION FOR 393 GRADE

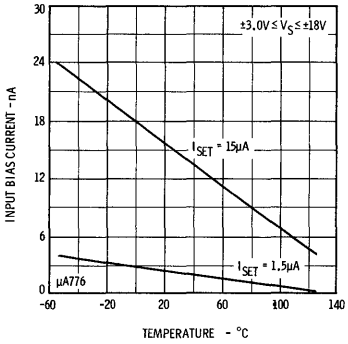
ELECTRICAL CHARACTERISTICS (T_A = 25°C, Unless Otherwise Specified)

		I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	6.0		2.0	6.0	mV
Input Offset Current			0.7	6.0		2.0	25	nA
Input Bias Current			2.0	10		15	50	nA
Input Resistance			50			5.0		MΩ
Input Capacitance			2.0			2.0		pF
Offset Voltage Adjustment Range			9.0			18		mV
Large-Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT}=±10V	50k	400k					V/V
	$R_L \geq 5k\Omega$, V_{OUT}=±10V				50k	400k		V/V
Output Resistance			5.0			1.0		kΩ
Output Short-Circuit Current			2.0			10		mA
Supply Current			20	30		125	160	μA
Power Consumption				0.9			4.8	mW
Transient Response (unity gain)	V_{IN} = 20mV, $R_L \geq 5k\Omega$, $C_L \leq 100pF$							
Risetime			1.6			0.35		μs
Overshoot			0			10		%
Slew Rate	$R_L \geq 5k\Omega$		0.1			0.8		V/μs
Output Voltage Swing	$R_L \geq 75k\Omega$	±12	±14					V
	$R_L \geq 5k\Omega$				±10	±13		V
The following specifications apply to $0°C \leq T_A \leq +70°C$								
Input Offset Voltage	$R_S \leq 10k\Omega$			7.5			7.5	mV
Input Offset Current	T_A = +70°C			6.0			25	nA
	T_A = 0°C			10			40	nA
Input Bias Current	T_A = +70°C			10			50	nA
	T_A = 0°C			20			100	nA
Input Voltage Range		±10			±10			V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		25	200		25	200	μV/V
Large-Signal Voltage Gain	$R_L \geq 75k\Omega$, V_{OUT}=±10V	50k			50k			V/V
Output Voltage Swing	$R_L \geq 75k\Omega$	±10			±10			V
Supply Current				35			170	μA
Power Consumption				1.05			5.10	mW

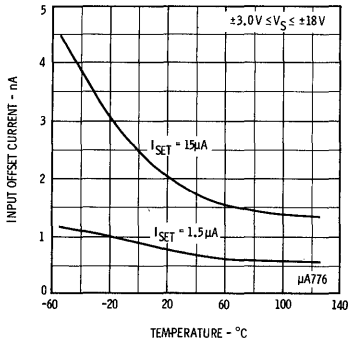
INPUT BIAS CURRENT AS A FUNCTION OF SET CURRENT



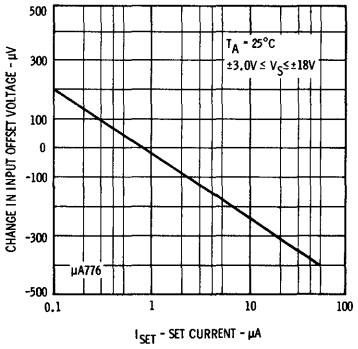
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



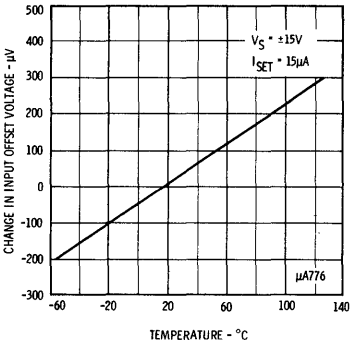
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



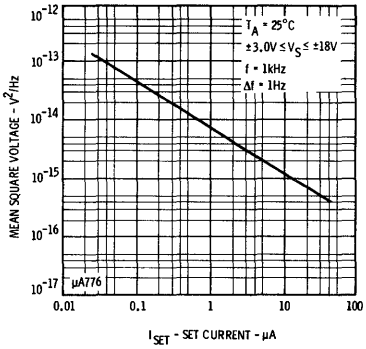
CHANGE IN INPUT OFFSET VOLTAGE AS A FUNCTION OF SET CURRENT



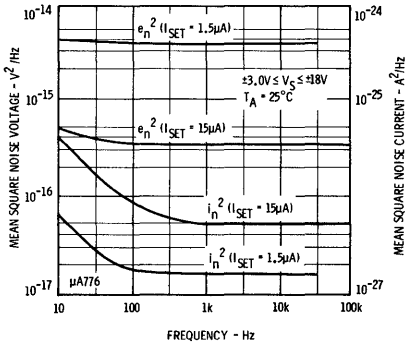
CHANGE IN INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE (UNNULLED)



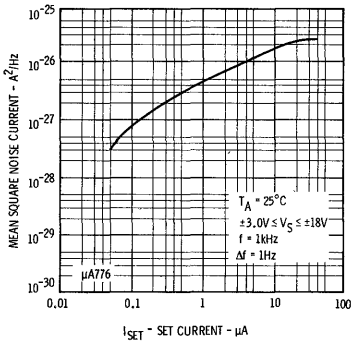
INPUT NOISE VOLTAGE AS A FUNCTION OF SET CURRENT



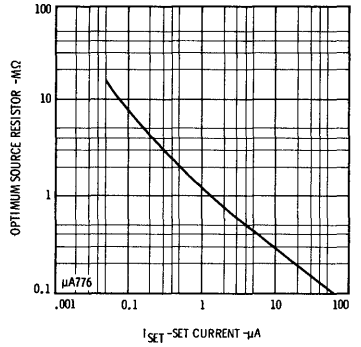
INPUT NOISE VOLTAGE AND CURRENT AS A FUNCTION OF FREQUENCY



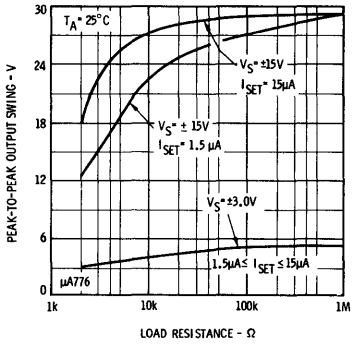
INPUT NOISE CURRENT AS A FUNCTION OF SET CURRENT



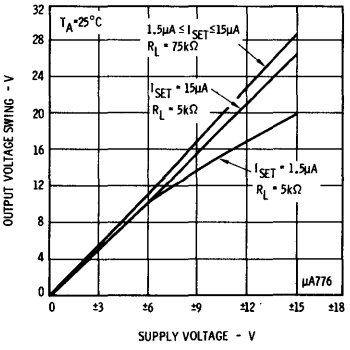
OPTIMUM SOURCE RESISTOR FOR MINIMUM NOISE AS A FUNCTION OF SET CURRENT



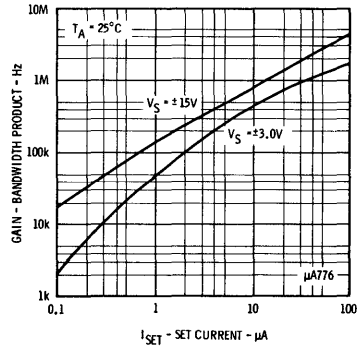
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



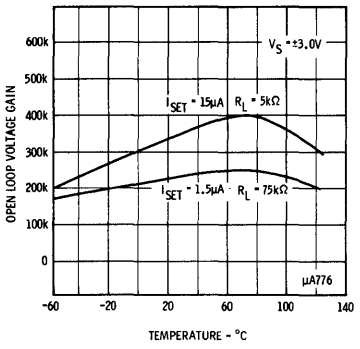
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



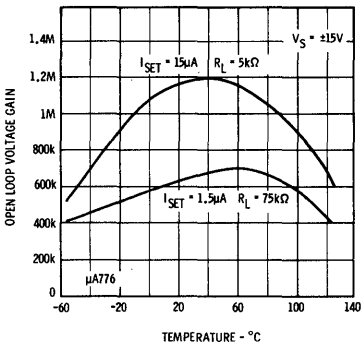
GAIN-BANDWIDTH PRODUCT AS A FUNCTION OF SET CURRENT



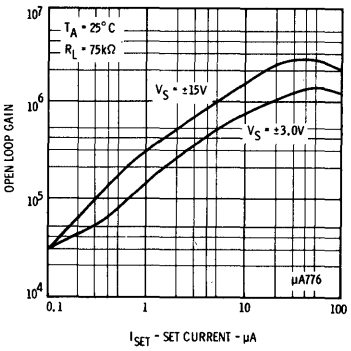
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



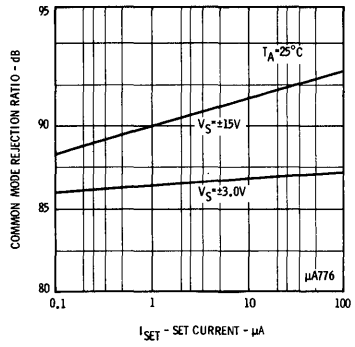
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



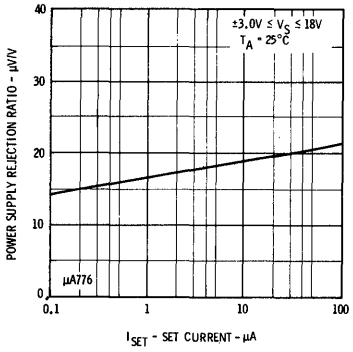
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SET CURRENT



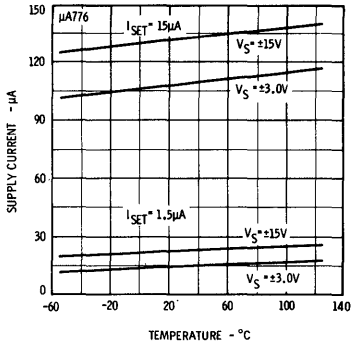
COMMON MODE REJECTION RATIO AS A FUNCTION OF SET CURRENT



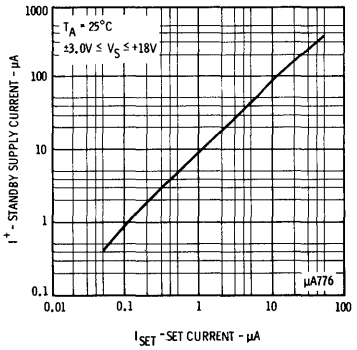
POWER SUPPLY REJECTION RATIO AS A FUNCTION OF SET CURRENT



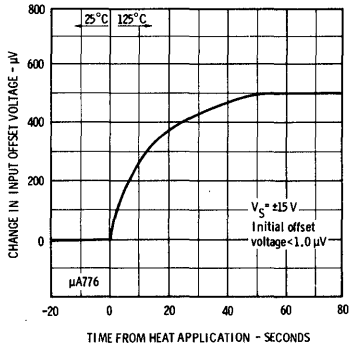
SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



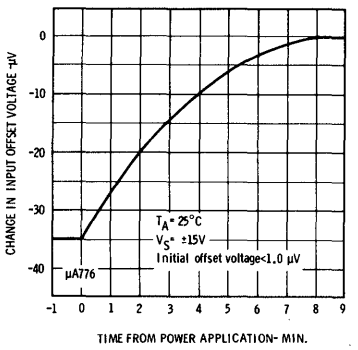
STANDBY SUPPLY CURRENT AS A FUNCTION OF SET CURRENT



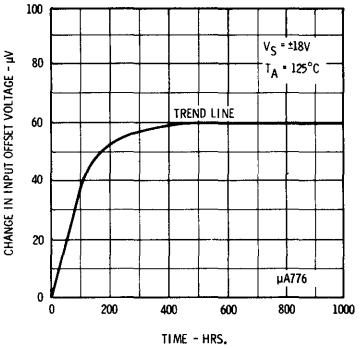
THERMAL RESPONSE OF INPUT OFFSET VOLTAGE TO STEP CHANGE OF CASE TEMPERATURE



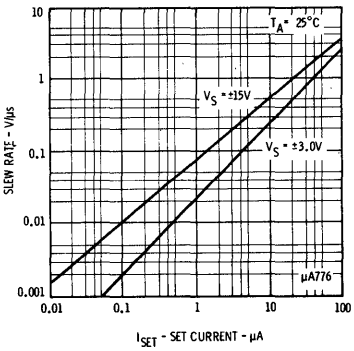
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER ON



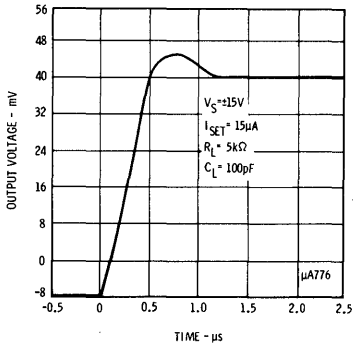
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



SLEW RATE AS A FUNCTION OF SET CURRENT

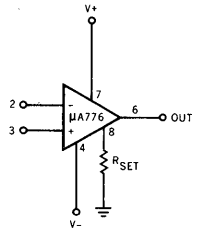


VOLTAGE FOLLOWER TRANSIENT RESPONSE (UNITY GAIN)



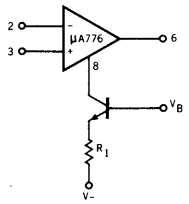
BIASING CIRCUITS

RESISTOR BIASING

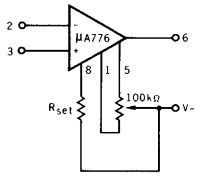


R_{SET} CONNECTED TO GROUND

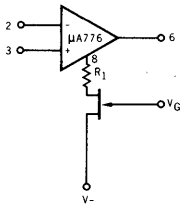
TRANSISTOR CURRENT SOURCE BIASING



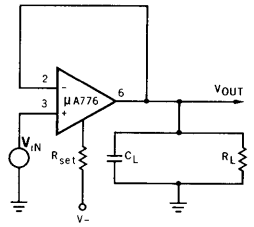
VOLTAGE OFFSET NULL CIRCUIT

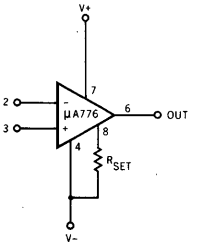


FET CURRENT SOURCE BIASING



TRANSIENT RESPONSE TEST CIRCUIT

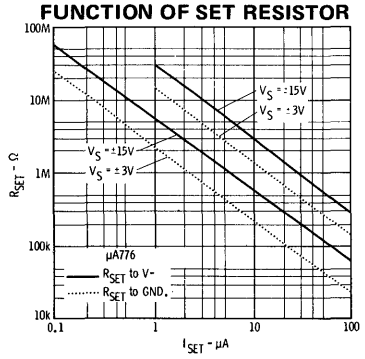




R_{SET} CONNECTED TO V^-*

*Recommended for supply voltages less than ±6V.

SET CURRENT AS A FUNCTION OF SET RESISTOR



QUIESCENT CURRENT SETTING RESISTOR (I_{SET} TO V^-)

V_S	I_{SET}	
	1.5μA	15μA
±1.5 V	1.7MΩ	170kΩ
±3.0 V	3.6MΩ	360kΩ
±6.0 V	7.5MΩ	750kΩ
±15 V	20MΩ	2.0MΩ

Note: The μA776 may be operated with R_{set} connected to ground or V^-.

I_{SET} EQUATIONS:

$$I_{SET} = \frac{V^+ - 0.7 - V^-}{R_{SET}}$$

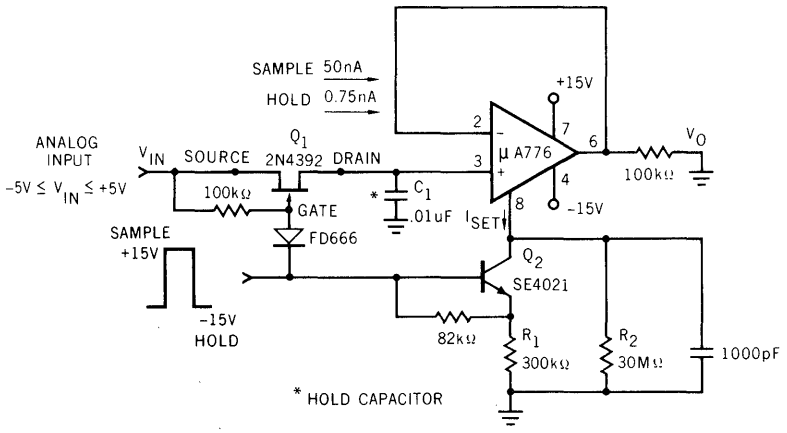
where R_{SET} is connected to V^-

$$I_{SET} = \frac{V^+ - 0.7}{R_{SET}}$$

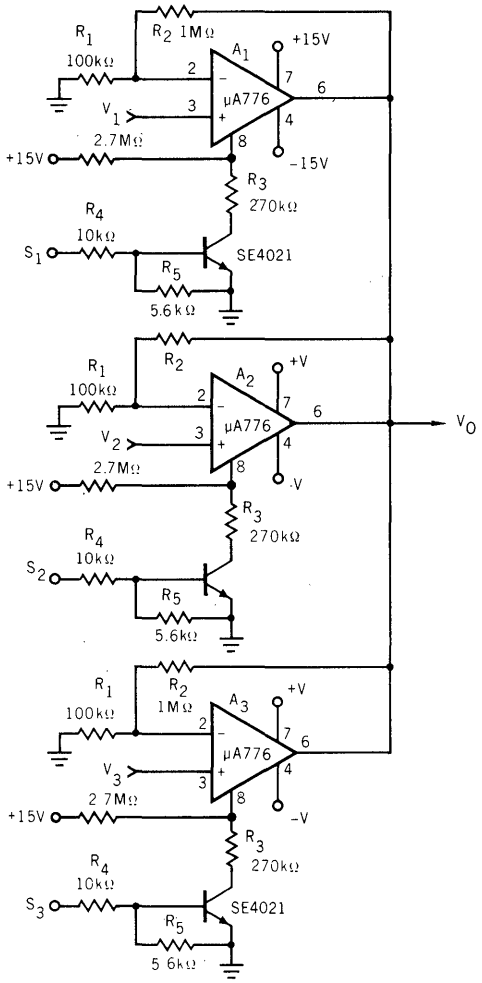
where R_{SET} is connected to ground.

TYPICAL APPLICATIONS

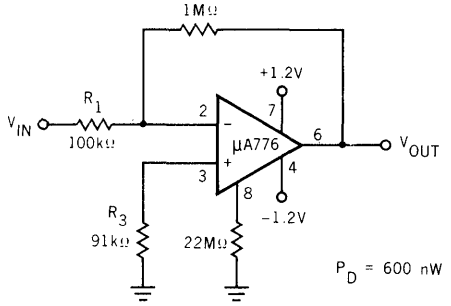
HIGH ACCURACY SAMPLE AND HOLD



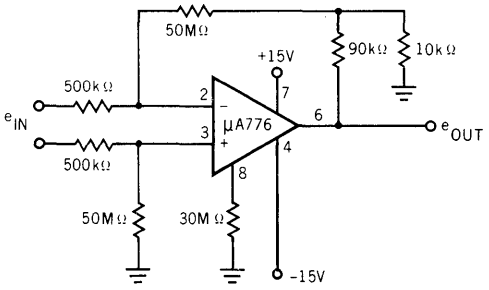
MULTIPLEXING AND SIGNAL CONDITIONING WITHOUT FET'S



NANO-WATT AMPLIFIER



HIGH INPUT IMPEDANCE AMPLIFIER



μA777
PRECISION OPERATIONAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

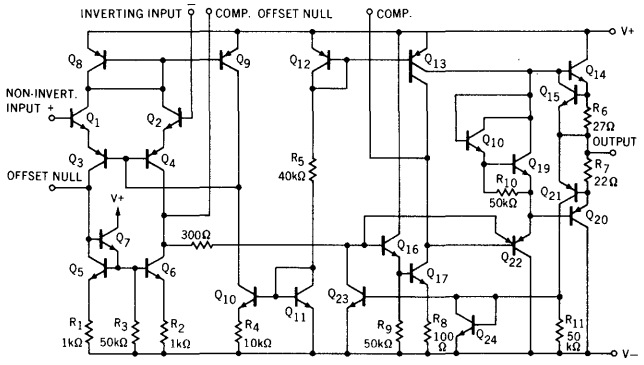
GENERAL DESCRIPTION — The μA777 is a precision operational amplifier constructed on a single silicon chip, using a low noise Fairchild Planar* epitaxial process. It is an excellent choice when performance versus cost trade-offs are possible between super beta or FET input operational amplifiers and low cost general purpose operational amplifiers. Low offset and bias currents improve system accuracy when used in applications such as long term integrators, sample and hold circuits and high source impedance summing amplifiers. Even though the input bias current is extremely low, the μA777 maintains full ± 30 V differential voltage range. The internal construction utilizes isothermal layout and special electrical design to maintain system performance despite variations in temperature or output load. High common mode input voltage range, latch-up protection, short circuit protection and simple frequency compensation make the device versatile and essentially foolproof.

- **LOW OFFSET VOLTAGE AND OFFSET CURRENT**
- **LOW OFFSET VOLTAGE AND CURRENT DRIFT**
- **LOW INPUT BIAS CURRENT**
- **LOW INPUT NOISE VOLTAGE**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**

ABSOLUTE MAXIMUM RATINGS

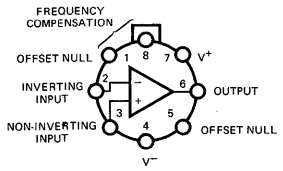
Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Ceramic DIP	670 mW
Silicone DIP	340 mW
Mini DIP	310 mW
Flatpak	570 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, Ceramic DIP, and Flatpak	−65°C to +150°C
Mini DIP and Silicone DIP	−55°C to +125°C
Operating Temperature Range	
Military (312 Grade)	−55°C to +125°C
Commercial (393 Grade)	0°C to 70°C
Lead Temperature (Soldering, 60 Seconds)	
Metal Can, Ceramic DIP and Flatpak	300°C
Mini DIP and Silicone DIP	260°C
Output Short Circuit Duration (Note 3)	Indefinite

EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS

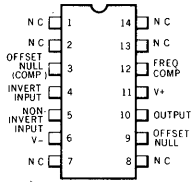
8 LEAD METAL CAN
(TOP VIEW)



NOTE: Pin 4 connected to case

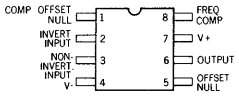
ORDER PART NOS: U5B7777312
U5B7777393

14 LEAD DIP
(TOP VIEW)



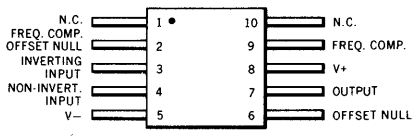
ORDER PART NOS: U6A7777312
U6A7777393
U9A7777393

MINI DIP
(TOP VIEW)



ORDER PART NO: U9T7777393

10 LEAD FLAT PACK ‡
(TOP VIEW)



‡Available on special request

ORDER PART NO: U3F7777312

Notes on following pages.

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS FOR μA777 (312 GRADE) ($V_S = \pm 15$ V, $T_A = 25°C$, $C_C = 30$ pF unless otherwise specified)

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50$ kΩ		.5	2.0	mV
Input Offset Current			.25	3.0	nA
Input Bias Current			8.0	25	nA
Input Resistance		2.0	10.0		MΩ
Input Capacitance			3.0		pF
Offset Voltage Adjustment Range			±25		mV
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$V	50,000	250,000		
Output Resistance			100		Ω
Output Short-Circuit Current			±25		mA
Supply Current			1.9	2.8	mA
Power Consumption			60	85	mW
Transient Response	$V_{IN} = 20$ mV, $C_C = 30$ pF,				
(Voltage Follower, Gain of 1)	$R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			.3		μs
Overshoot			5.0		%
Slew Rate	$R_L \geq 2$kΩ		.5		V/μs
(Voltage Follower, Gain of 1)					
Transient Response	$V_{IN} = 20$ mV, $C_C = 3.5$ pF,				
(Voltage Follower, Gain of 10)	$R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			.2		μs
Overshoot			5.0		%
Slew Rate	$R_L \geq 2$ kΩ, $C_C = 3.5$ pF		5.5		V/μs
(Voltage Follower, Gain of 10)					
The following specifications apply for	$-55°C \leq T_A \leq +125°C$:				
Input Offset Voltage	$R_S \leq 50$ kΩ		0.5	3.0	mV
Average Input Offset Voltage Drift	$R_S \leq 50$ kΩ		2.5	15	μV/°C
Input Offset Current				10	nA
Average Input Offset Current Drift	$25°C \leq T_A \leq 125°C$		2.5	30	pA/°C
	$-55°C \leq T_A \leq 25°C$		6.5	150	pA/°C
Input Bias Current				75	nA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 50$ kΩ	80	95		dB
Supply Voltage Rejection Ratio	$R_S \leq 50$ kΩ		13	100	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	25,000			
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Supply Current	$T_A = +125°C$		1.5	2.5	mA
	$T_A = -55°C$		2.0	3.3	mA
Power Consumption	$T_A = +125°C$		40	75	mW
	$T_A = -55°C$		60	100	mW

ELECTRICAL CHARACTERISTICS FOR μA777 (393 GRADE) ($V_S = \pm 15$ V, $T_A = 25°C$, $C_C = 30$ pF unless otherwise specified)

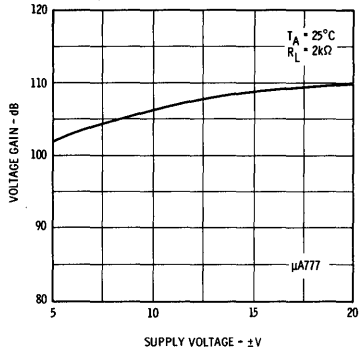
PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50$ kΩ		0.7	5.0	mV
Input Offset Current			0.7	20.0	nA
Input Bias Current			25	100	nA
Input Resistance		1.0	2.0		MΩ
Input Capacitance			3.0		pF
Offset Voltage Adjustment Range			±25		mV
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$V	25,000	250,000		
Output Resistance			100		Ω
Output Short-Circuit Current			±25		mA
Supply Current			1.9	2.8	mA
Power Consumption			60	85	mW
Transient Response	$V_{IN} = 20$ mV, $C_C = 30$ pF,				
(Voltage Follower, Gain of 1)	$R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			.3		μs
Overshoot			5.0		%
Slew Rate	$R_L \geq 2$ kΩ		.5		V/μ
(Voltage Follower, Gain of 1)					
Transient Response	$V_{IN} = 20$ mV, $C_C = 3.5$ pF,				
(Voltage Follower, Gain of 10)	$R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			.2		μs
Overshoot			5.0		%
Slew Rate	$R_L \geq 2$ kΩ		5.5		V/μs
(Voltage Follower, Gain of 10)					
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage	$R_S \leq 50$ kΩ		0.8	5.0	mV
Average Input Offset Voltage Drift	$R_S \leq 50$ kΩ		4	30	μV/°C
Input Offset Current				40	nA
Average Input Offset Current Drift	$25°C \leq T_A \leq 70°C$		.01	0.3	nA/°C
	$0°C \leq T_A \leq 25°C$		.02	0.6	nA/°C
Input Bias Current				200	nA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 50$ kΩ	70	95		dB
Supply Voltage Rejection Ratio	$R_S \leq 50$ kΩ		15	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	15,000			
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Power Consumption			60	100	mW

NOTES

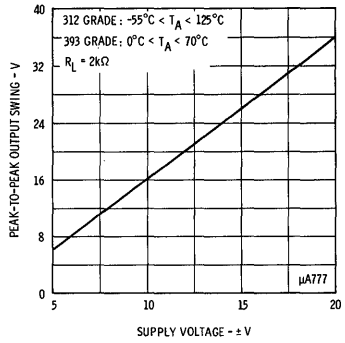
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for Metal Can, 8.3 mW/°C for the Ceramic DIP, 6.3 mW/°C for Silicone DIP, 5.6 mW/°C for the Mini DIP and 7.1 mW/°C for the Flatpak package.
2. For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

TYPICAL PERFORMANCE CURVES

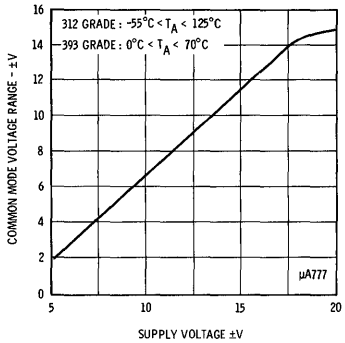
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



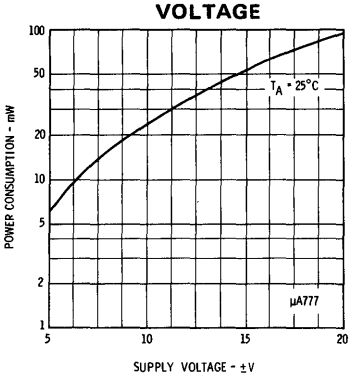
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



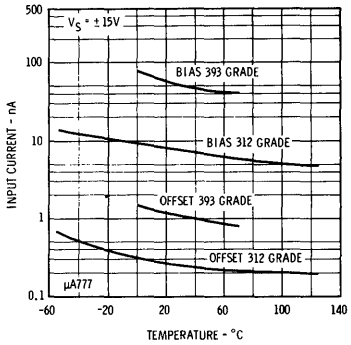
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



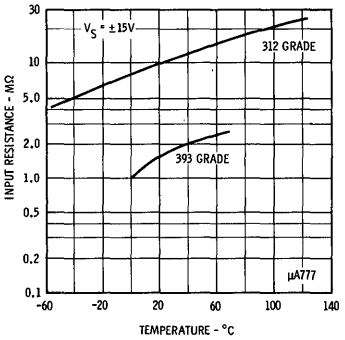
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



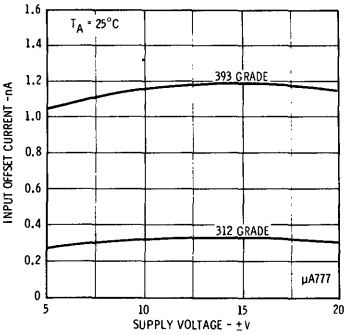
INPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



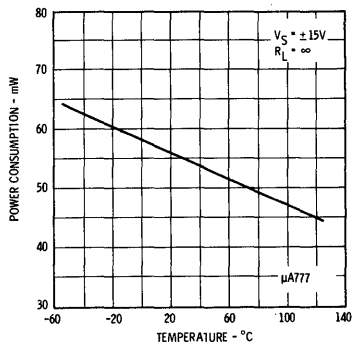
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



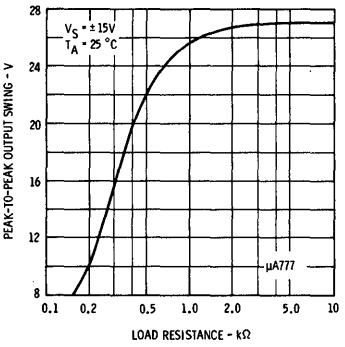
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



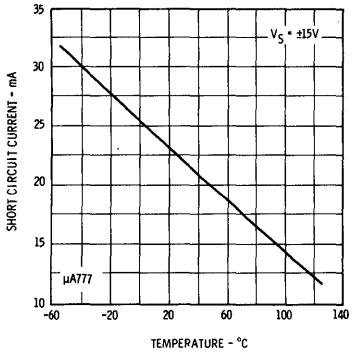
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



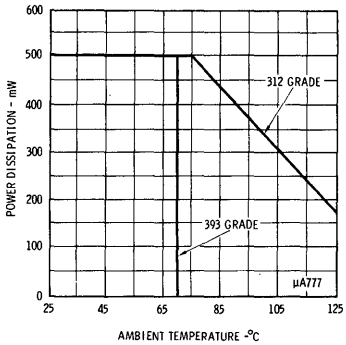
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



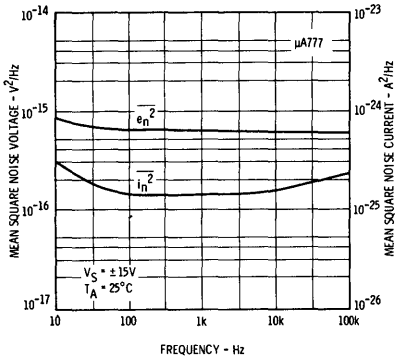
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE

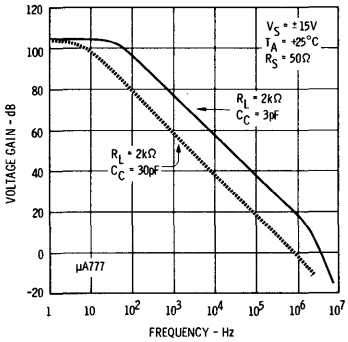


INPUT NOISE VOLTAGE AND CURRENT AS A FUNCTION OF FREQUENCY

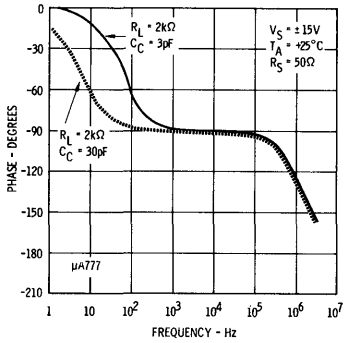


TYPICAL PERFORMANCE CURVES

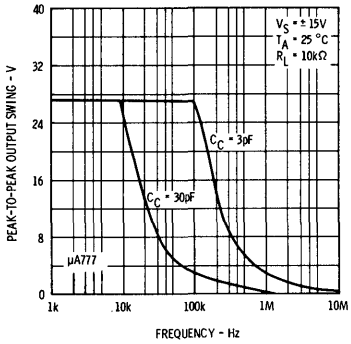
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



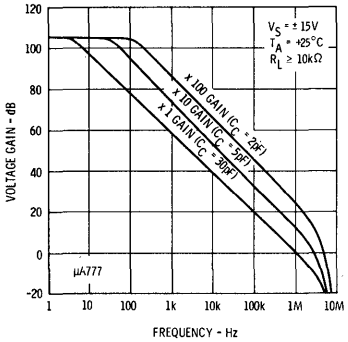
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



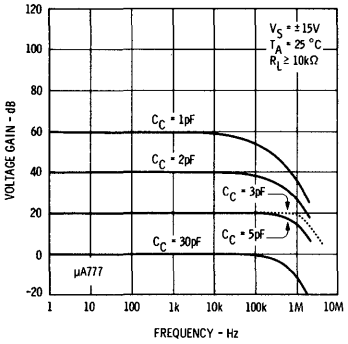
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



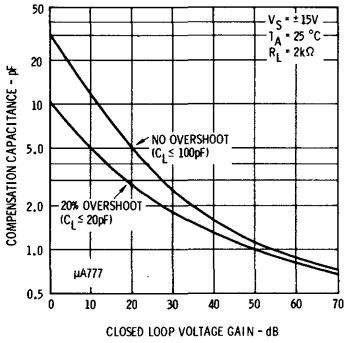
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY FOR VARIOUS GAIN/COMPENSATION OPTIONS



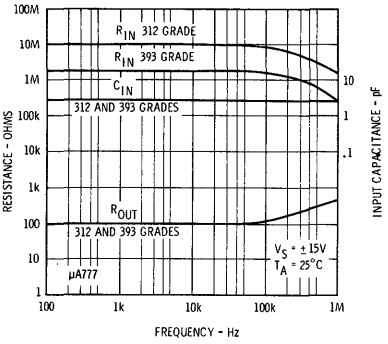
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



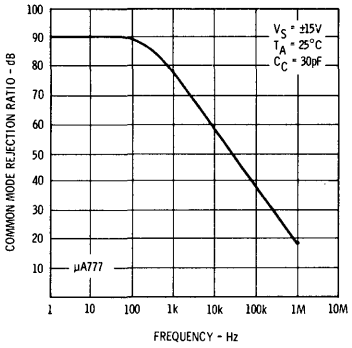
COMPENSATION CAPACITANCE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN



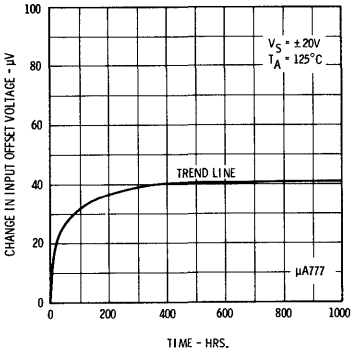
INPUT RESISTANCE, OUTPUT RESISTANCE, AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



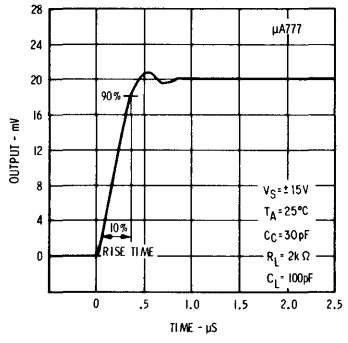
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



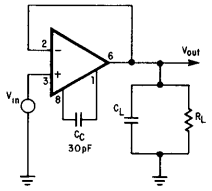
INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME



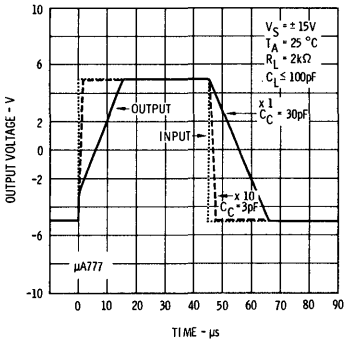
VOLTAGE FOLLOWER TRANSIENT RESPONSE (GAIN OF 1)



TRANSIENT RESPONSE TEST CIRCUIT

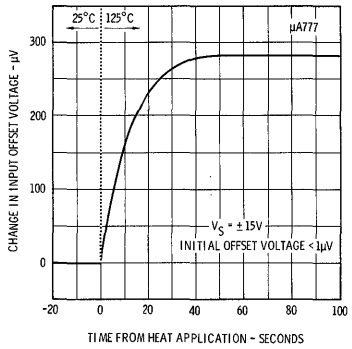


VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE

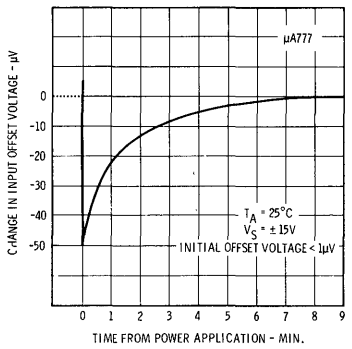


TYPICAL PERFORMANCE CURVES

THERMAL RESPONSE OF INPUT OFFSET VOLTAGE TO STEP CHANGE OF CASE TEMPERATURE

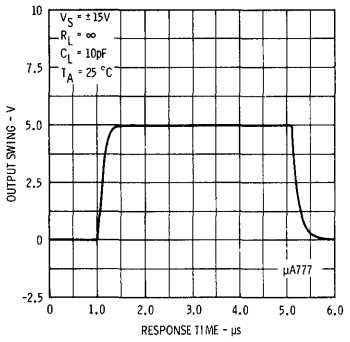


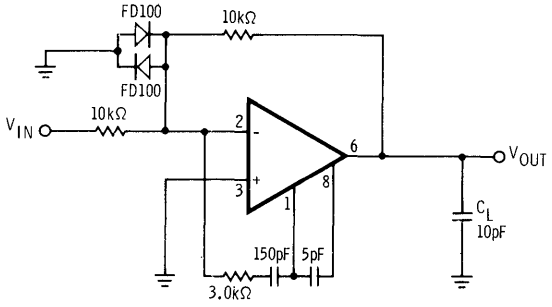
STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON



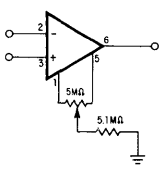
FEED-FORWARD COMPENSATION

LARGE SIGNAL FEEDFORWARD TRANSIENT RESPONSE

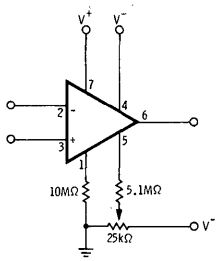




VOLTAGE OFFSET NULL CIRCUIT

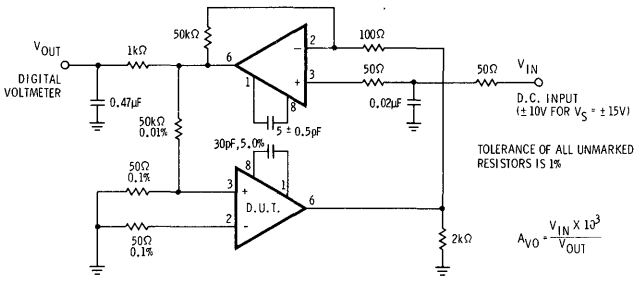


SUGGESTED



ALTERNATE

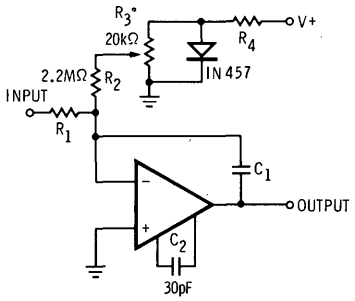
GAIN TEST CIRCUIT



ALTERNATE

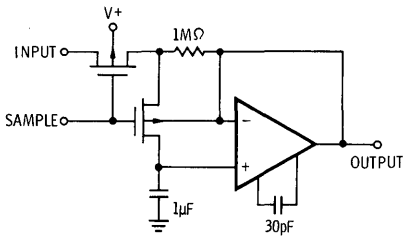
TYPICAL APPLICATIONS

BIAS COMPENSATED LONG TIME INTEGRATOR

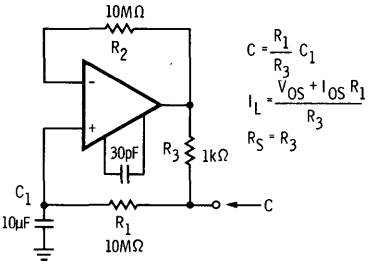


*Adjust R_3 for minimum integrator drift

SAMPLE AND HOLD



CAPACITANCE MULTIPLIER

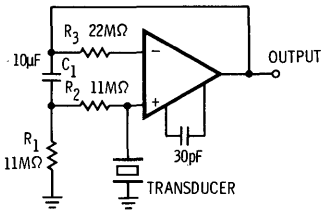


$$C = \frac{R_1}{R_3} C_1$$

$$I_L = \frac{V_{OS} + I_{OS} R_1}{R_3}$$

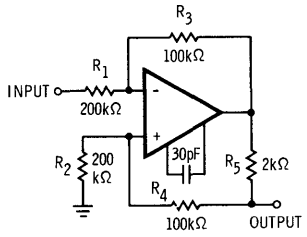
$$R_S = R_3$$

AMPLIFIER FOR CAPACITANCE TRANSDUCERS



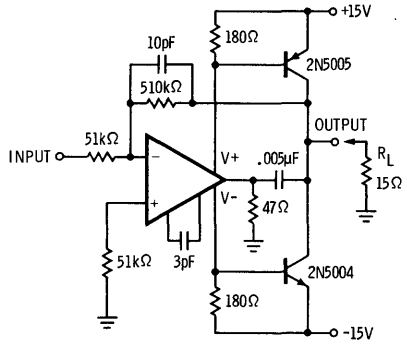
Low Frequency Cutoff $R_1 \times C_1$

BILATERAL CURRENT SOURCE

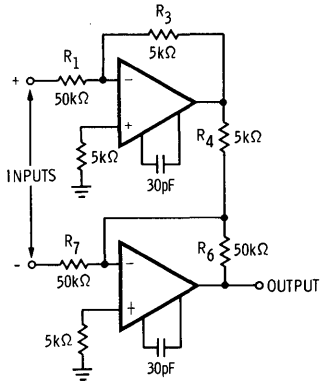


$$I_{OUT} = \frac{R_3 V_{IN}}{R_1 R_5} \; ; \; R_1 = R_2; R_3 = R_4 + R_5$$

HIGH SLEW RATE POWER AMPLIFIER



± 100 V COMMON MODE RANGE INSTRUMENTATION AMPLIFIER



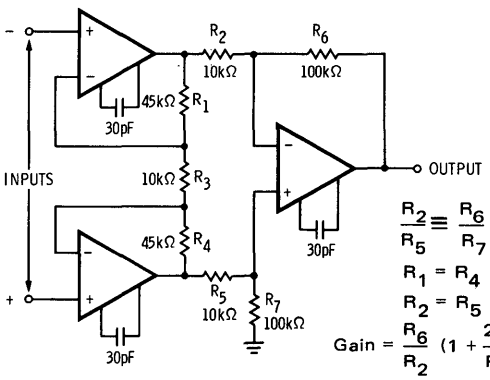
$\frac{R_1}{R_7} \equiv \frac{R_3}{R_4}$ for best CMRR

$R_3 = R_4$

$R_1 = R_6 = 10R_3$

$\text{Gain} = \frac{R_7}{R_6}$

INSTRUMENTATION AMPLIFIER WITH HIGH COMMON MODE REJECTION



$\frac{R_2}{R_5} \equiv \frac{R_6}{R_7}$ for best CMRR

$R_1 = R_4$

$R_2 = R_5$

$\text{Gain} = \frac{R_6}{R_2}\left(1 + \frac{2R_1}{R_3}\right)$

μA780
PHASE LOCKED LOOP
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA780 is a Phase Locked Loop designed for use as a Color TV Subcarrier Regenerator and is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. This integrated circuit, which uses an Automatic Phase Control (APC) loop, accepts the composite NTSC color video signal, extracts the color subcarrier reference and generates a CW signal suitable for use as a chroma demodulation reference. Other features include control of the CW phase (tint) by a DC voltage, blanking of the CW output during burst time and synchronous generation of an Automatic Color Control (ACC) voltage.

The μA780 in combination with the μA781 Chroma IF Amplifier and the μA746 Chroma Demodulator form a complete low cost, high quality chroma processing system for color TV receivers.

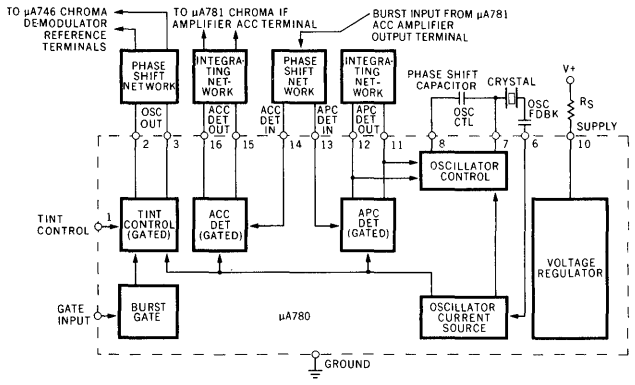
The μA780 is also useful as a communications phase locked loop system to select, amplify and demodulate AM, FM, FSK and SSB signals.

- **COMPLETE COLOR TV SUBCARRIER REGENERATOR**
- **AUTOMATIC PHASE CONTROL LOOP**
- **DC TINT CONTROL**
- **SYNCHRONOUS ACC/KILLER DETECTOR**
- **COLOR BURST GATING AND BLANKING**
- **INTERNALLY REGULATED SUPPLY**

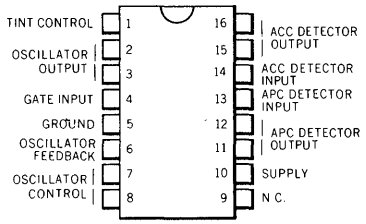
ABSOLUTE MAXIMUM RATINGS

Supply Current	40 mA
Current into Gate Input Terminal	5 mA
Peak-to-Peak Voltage at either APC or ACC Detector Input Terminals	5 V
Internal Power Dissipation Ceramic DIP	730 mW
Storage Temperature Range Ceramic DIP	−65° C to +150° C
Operating Temperature Range	0° C to + 70° C
Lead Temperature Ceramic DIP (Soldering, 60 seconds)	300° C

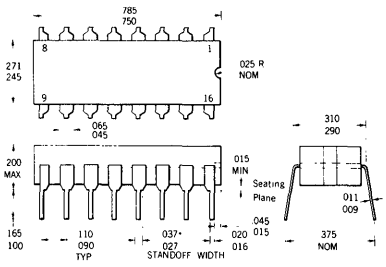
BLOCK DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



PHYSICAL DIMENSIONS
6B–PACKAGE CERAMIC DIP



ORDER PART NO. U6B7780394

NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

*Planar is a patented Fairchild process.

STATIC ELECTRICAL CHARACTERISTICS (T_A = 25°C, Gate "ON," Test Circuit 1 unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current			26		mA
Voltage at Supply Terminal		11.3	12.0	12.6	V
Supply Regulation	V^+ = 21 V to V^+ = 27 V		40		mV
Total Current into Oscillator Output Terminals	Gate "OFF," 50 k Ω resistor connected between Pin 10 and Pin 6, Pin 2 shorted to Pin 3	4.2	5.8	7.6	mA
Current into either APC Detector Output Terminal	12 k Ω resistor connected between Pin 6 and Ground		12	40	μA
Offset Voltage between ACC Detector Output Terminals (V_{15} -V_{16})	50 k Ω resistor connected between Pin 10 and Pin 6	-330	-70	+300	mV
Offset Voltage between APC Detector Output Terminals (V_{11} -V_{12})	50 k Ω resistor connected between Pin 10 and Pin 6	-315	-50	+315	mV
Offset Voltage between Oscillator Control Terminals (V_7 -V_8)	12 k Ω resistor connected between Pin 6 and Ground, V_{11} = V_{12} = 9.5 V	-330	-20	+330	mV
Offset Voltage between Oscillator Output Terminals (V_2 -V_3)	Gate "OFF"	-200	+300	+800	mV
Voltage at Oscillator Feedback Terminal			2.8		V
Voltage at ACC Detector Input Terminal		6.0	6.5	7.0	V
Voltage at APC Detector Input Terminal		6.0	6.5	7.0	V
Voltage at Tint Control Terminal			200	300	mV
Voltage at Tint Control Terminal	Gate "OFF"	7.3	7.6	8.2	V
Internal Power Dissipation			310	400	mV

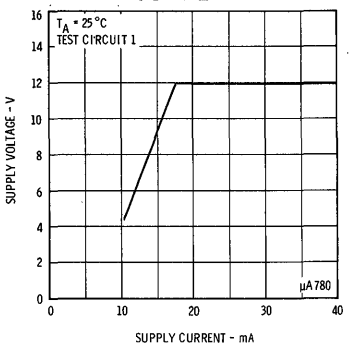
DYNAMIC ELECTRICAL CHARACTERISTICS (T_A = 25°C, peak-to-peak burst level at APC Detector Input Terminal = 200 mV. Standard NTSC Signal, f_o=3.579545 MHz, Test Circuit 2 unless otherwise specified.)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Oscillator Pull-in Range	$f_{\text{free run}} > f_o$		+510		Hz
	$f_{\text{free run}} < f_o$		-750		Hz
Oscillator Static Phase Error	$f_{\text{free run}} = f_o$ + 120 Hz		+2.2		Degree
	$f_{\text{free run}} = f_o$ - 120 Hz		-2.2		Degree
Oscillator Control Sensitivity			12		Hz/mV
Input Resistance at Oscillator Feedback Terminal			2.2		k Ω
Input Capacitance at Oscillator Feedback Terminal			4.5		pF
Peak-to-Peak Current at Oscillator Output Terminal (Pin 3)	Tint Control Wiper at Ground		6.8		mA
ACC Detector Input Resistance			2.2		k Ω
ACC Detector Input Capacitance			4.5		pF
ACC Detector Sensitivity	100 mV p-p burst level at ACC Detector Input Terminal, Oscillator Locked		+2.2		mV DC/mV p-p
APC Detector Input Resistance			2.2		k Ω
APC Detector Input Capacitance			4.5		pF
APC Detector Sensitivity			5		mV/Degree

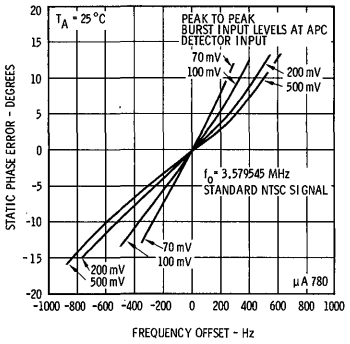
TYPICAL PERFORMANCE CURVES

(Test Circuit 2 unless otherwise specified)

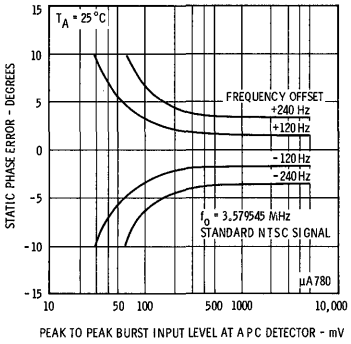
SUPPLY VOLTAGE AS A FUNCTION OF SUPPLY CURRENT



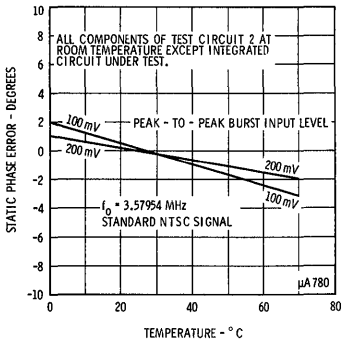
STATIC PHASE ERROR AS A FUNCTION OF FREQUENCY OFFSET



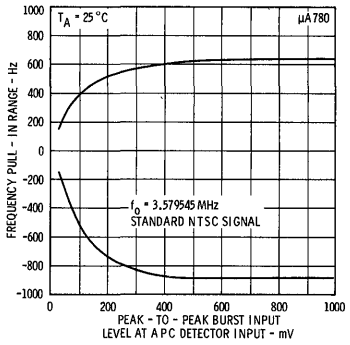
STATIC PHASE ERROR AS A FUNCTION OF BURST INPUT LEVEL



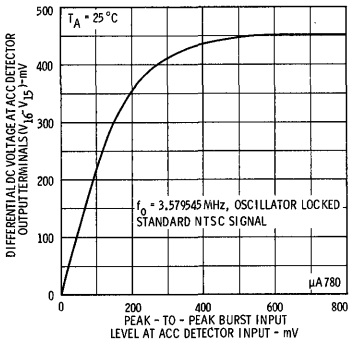
STATIC PHASE ERROR AS A FUNCTION OF TEMPERATURE



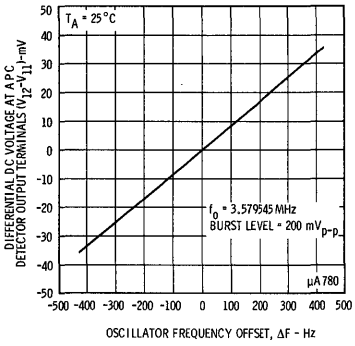
FREQUENCY PULL-IN RANGE AS A FUNCTION OF BURST INPUT LEVEL



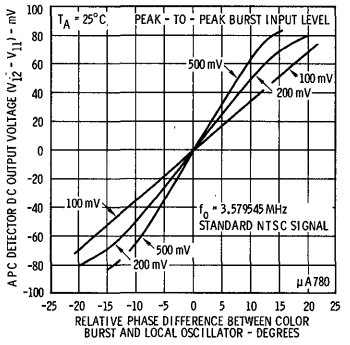
DIFFERENTIAL DC VOLTAGE AT ACC DETECTOR OUTPUT AS A FUNCTION OF BURST INPUT LEVEL



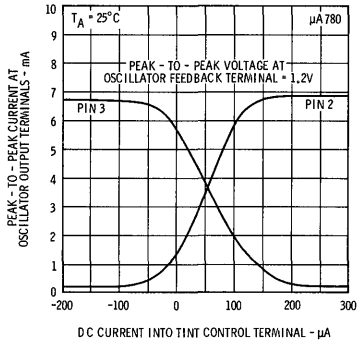
DIFFERENTIAL DC VOLTAGE AT APC DETECTOR OUTPUT TERMINALS AS A FUNCTION OF OSCILLATOR FREQUENCY OFFSET



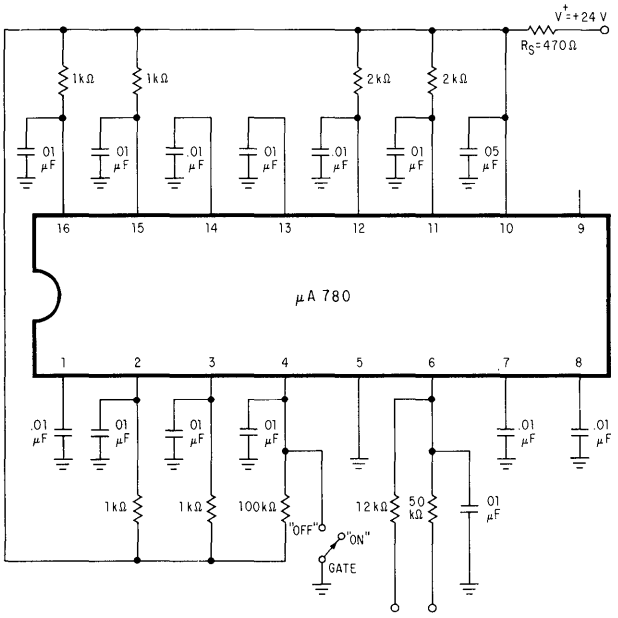
APC DETECTOR OUTPUT AS A FUNCTION OF RELATIVE PHASE DIFFERENCE



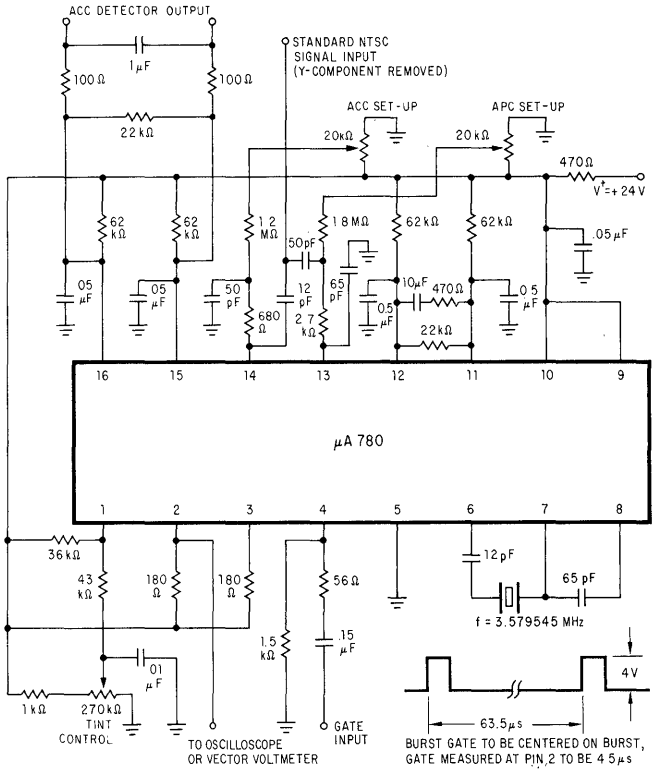
OSCILLATOR OUTPUT AS A FUNCTION OF TINT CONTROL CURRENT



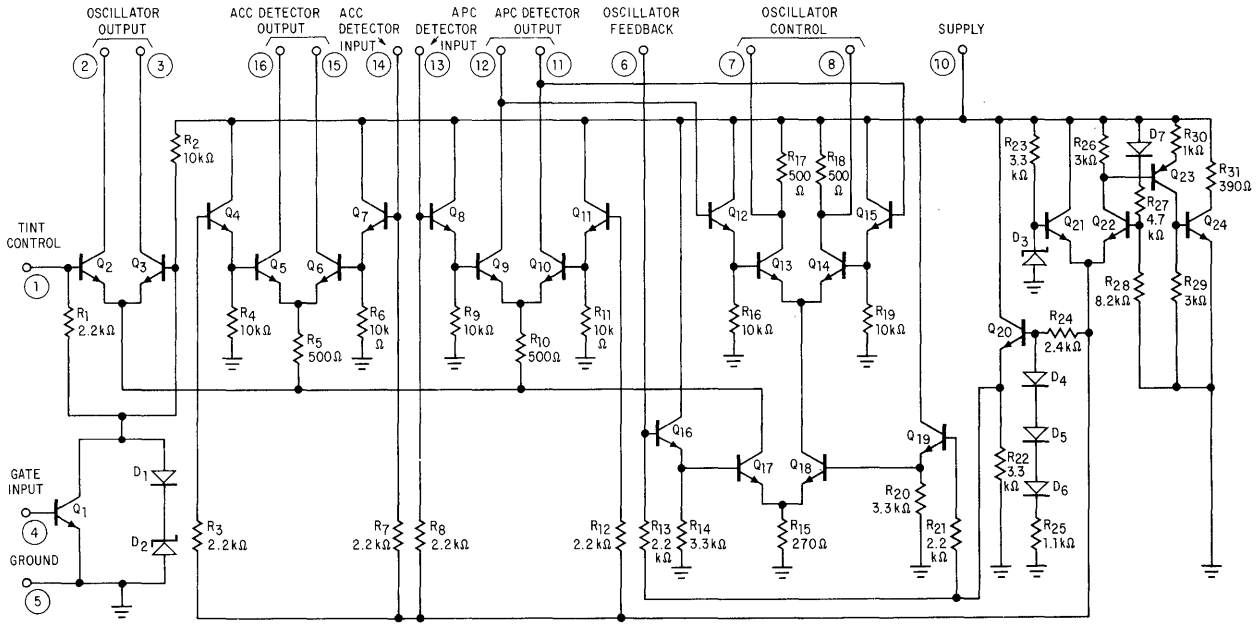
TEST CIRCUIT 1



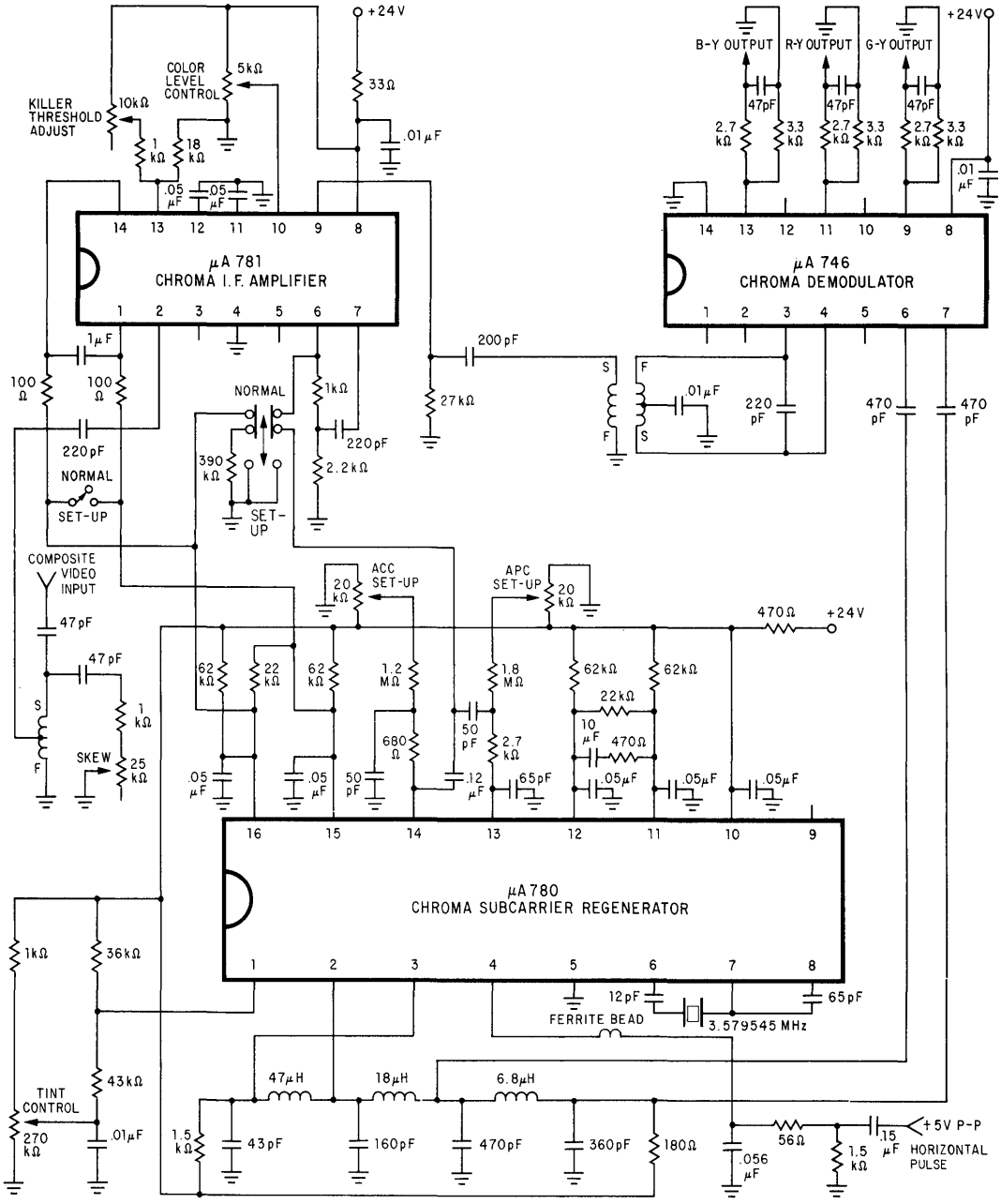
TEST CIRCUIT 2



EQUIVALENT CIRCUIT

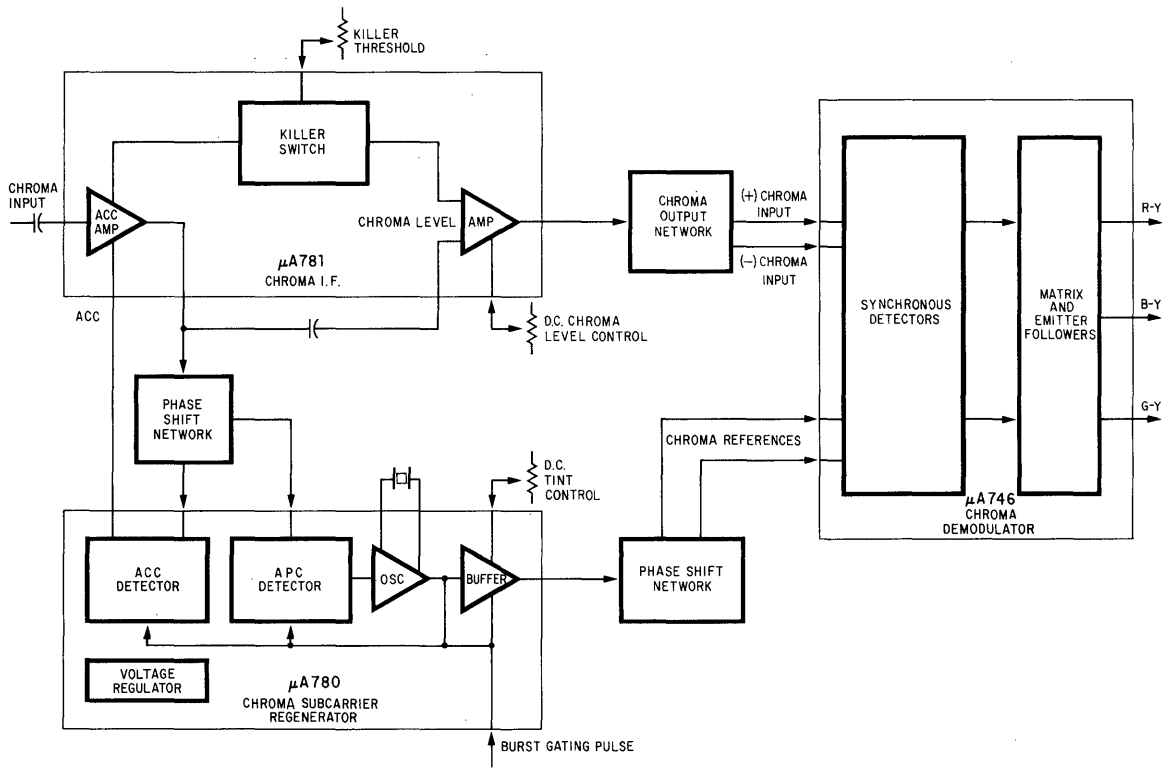


INTEGRATED CIRCUIT COLOR TV CHROMA PROCESSING SYSTEM (COMPLETE SCHEMATIC)



INTEGRATED CIRCUIT COLOR TV CHROMA PROCESSING SYSTEM

(BLOCK DIAGRAM)



μA781
GAIN CONTROLLED IF AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA781 is a dual gain controlled IF amplifier designed for use as a Color TV Chroma IF Amplifier and constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The first section is a gain controlled chroma signal amplifier whose output is used to drive a subcarrier regenerator circuit. The gain of the second section is controlled by means of an external DC voltage to set chroma level. In addition, the second stage may be gated off to provide "color killing" action in the absence of a color signal with the trip point of the gate adjusted externally.

The μA781 in combination with the μA780 Phase Locked Loop Subcarrier Regenerator and the μA746 Chroma Demodulator forms a complete low cost, high quality chroma processing system for color TV receivers.

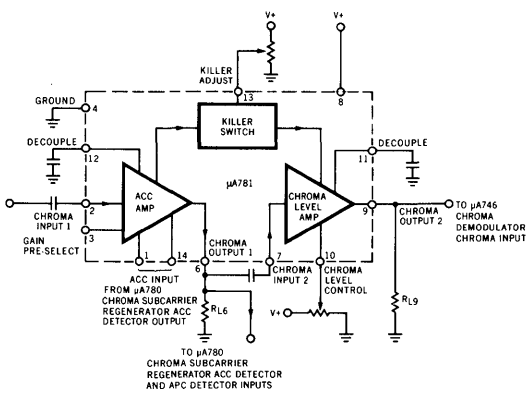
The μA781 is also useful as a gain-controlled, intermediate-frequency amplifier in AM and FM communication circuits.

- **COMPLETE COLOR TV CHROMA IF AMP**
- **10 MHz BANDWIDTH**
- **AUTOMATIC COLOR CONTROL (ACC) AMPLIFIER**
- **DC CHROMA LEVEL CONTROL**
- **ADJUSTABLE COLOR KILLER**
- **OUTPUT SHORT CIRCUIT PROTECTION**

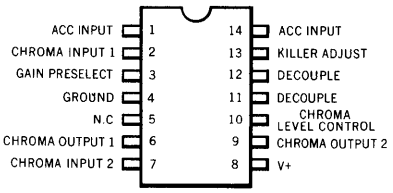
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	30 V
Internal Power Dissipation	
Ceramic DIP	670 mW
Storage Temperature Range	
Ceramic DIP	−65°C to +150°C
Operating Temperature Range	0°C to + 70°C
Lead Temperature	
Ceramic DIP (Soldering, 60 seconds)	300°C
Output Short Circuit Duration	30 seconds

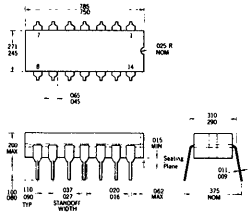
BLOCK DIAGRAM



CONNECTION DIAGRAM



PHYSICAL DIMENSIONS
6A PACKAGE - CERAMIC DIP



ORDER PART NO. U6A7781394

NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar

Package weight is 2.0 grams

*Planar is a patented Fairchild process.

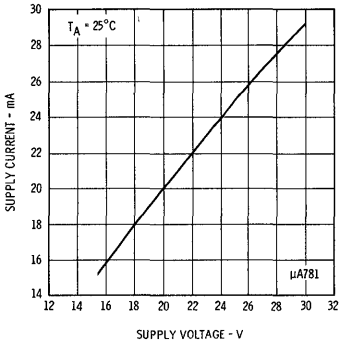
ELECTRICAL CHARACTERISTICS (NOTE 1)

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
Supply Current	$R_{L6} = R_{L9} = 1\ M\Omega$	8	13	18	mA
Supply Current		17	24	31	mA
Internal Power Dissipation			400	550	mW
Short Circuit Load Current, Chroma Output 1	$R_{L6} = 0\ \Omega$	20	42		mA
Short Circuit Load Current, Chroma Output 2	$R_{L9} = 0\ \Omega$	20	36		mA
DC Voltage at Chroma Output 1 Terminal		15.5	17.5	20.0	V
DC Voltage at Chroma Output 2 Terminal		17.5	18.0	18.5	V
Gain, ACC Amplifier Stage		14	17	19	dB
Gain Reduction ACC Amplifier Stage	$V_{ACC} = V_1 - V_{14} = 0$ mV to $V_1 - V_{14} = -75$ mV	12	14	16	dB
Maximum Gain, Chroma Level Amplifier Stage		12	15.8	17	dB
DC Voltage at Chroma Level Control Terminal for 90% Maximum Output Level, Chroma Level Amplifier Stage	Chroma Level Control set for 90% Maximum Output	2.3	3.5	4.8	V
DC Voltage at Chroma Level Control Terminal for 10% Maximum Output Level, Chroma Level Amplifier Stage	Chroma Level Control Wiper set for 10% of Maximum Output	17	19.5	21.7	V
Killer "ON" Threshold			16.6	17.0	V
Killer "OFF" Threshold		16.0	16.3		V
DC Voltage at Decouple Terminal, Pin 11		15	15.5	16	V
DC Voltage at Decouple Terminal, Pin 12		14.5	15.3	16	V
DC Voltage at Gain Preselect Terminal		0.7	1.0	1.2	V
DC Voltage at Chroma Input 1 Terminal			1.7		V
DC Voltage at Chroma Input 2 Terminal			1.4		V
Gain Change with V^+, Chroma Level Amplifier Stage	$V^+ = 24$ V to $V^+ = 21$ V	-1.9	-0.4	1.6	dB
	$V^+ = 24$ V to $V^+ = 27$ V	-1.9	0.8	1.6	dB
	Adjust Input Level at Chroma Input 2 for Output Level = 1.0 V RMS at Maximum Gain. Set Chroma Level Control Wiper for Output Level = 100 mV RMS				
Gain Change with Temperature, Chroma Level Amplifier Stage	$T_A = 25°C$ to $T_A = 70°C$ Adjust Input Level at Chroma Input 2 for Output Level = 1.0 V RMS at Maximum Gain. Set Chroma Level Control Wiper for Output Level = 100 mV RMS		0.7		dB
Chroma Input 1 Resistance			2.4		k Ω
Chroma Input 1 Capacitance			6.2		pF
Chroma Input 2 Resistance			2.4		k Ω
Chroma Input 2 Capacitance			4.2		pF

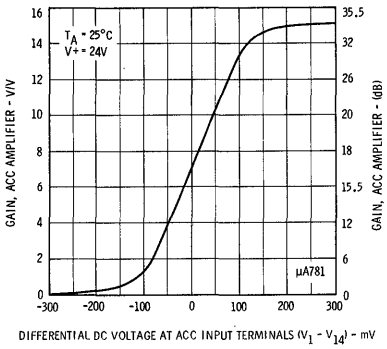
NOTE (1)

$T_A = 25°C$, $V^+ = 24$ V, $R_{L6} = 3.3$ k Ω, $R_{L9} = 2.7$ k Ω, Chroma Level Control Wiper at Ground, Voltage at ACC Input Terminals = 10 V, zero Differential Voltage between ACC Input Terminals, f = 3.58 MHz, Peak-to-peak Input at Chroma Input 1 = 200 mV, Peak-to-peak Input at Chroma Input 2 = 400 mV, unless otherwise specified. Refer to Test Circuit 1.

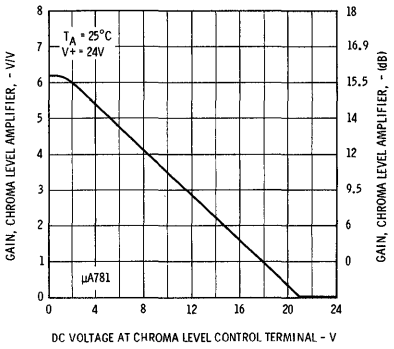
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



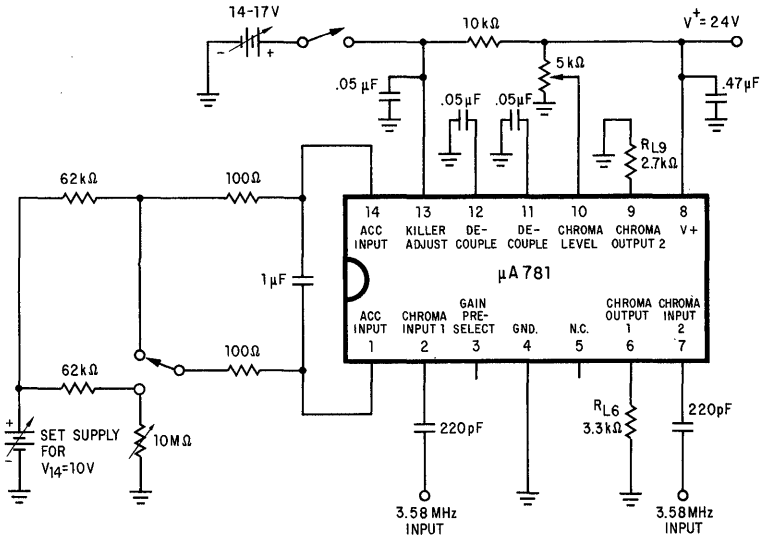
ACC AMPLIFIER GAIN AS A FUNCTION OF DIFFERENTIAL DC VOLTAGE AT ACC INPUT TERMINALS



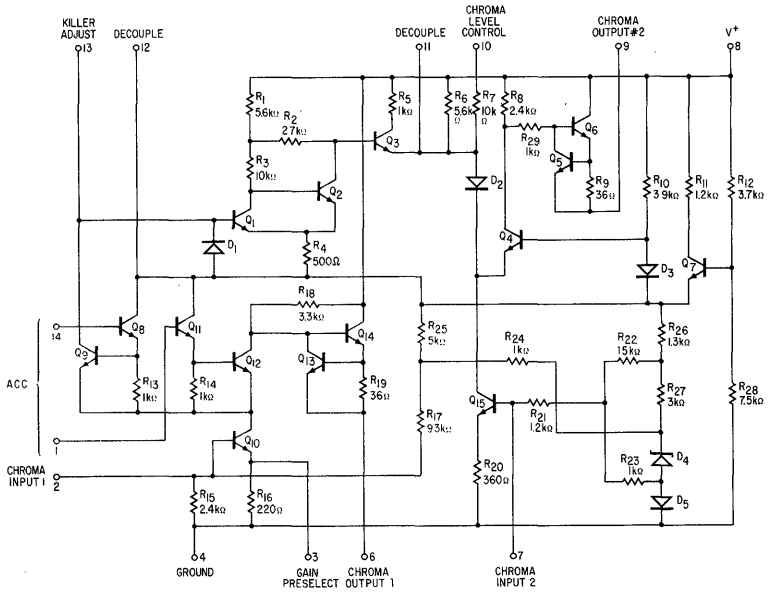
CHROMA LEVEL AMPLIFIER GAIN AS A FUNCTION OF DC VOLTAGE AT CHROMA LEVEL CONTROL TERMINAL



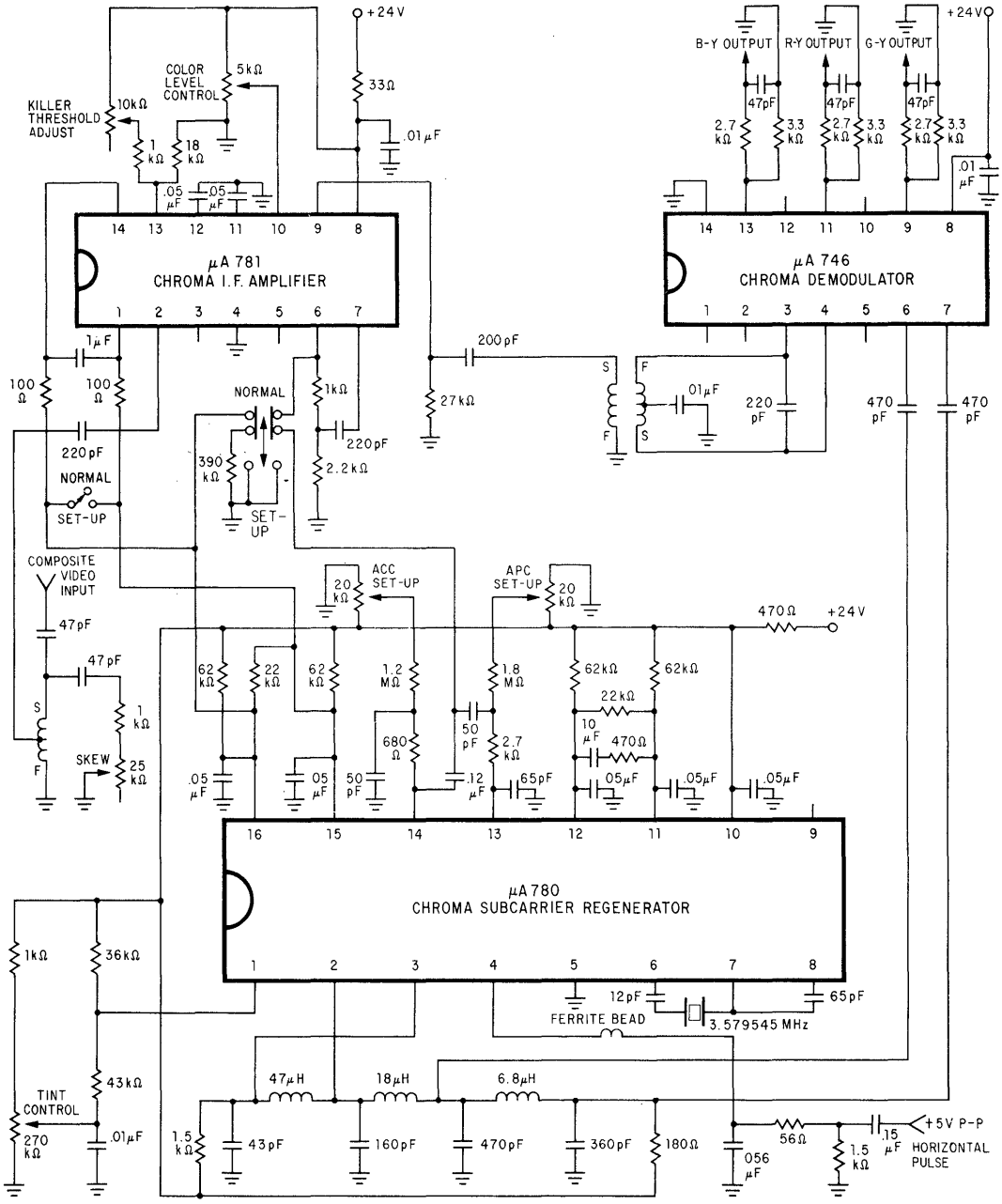
TEST CIRCUIT



EQUIVALENT CIRCUIT

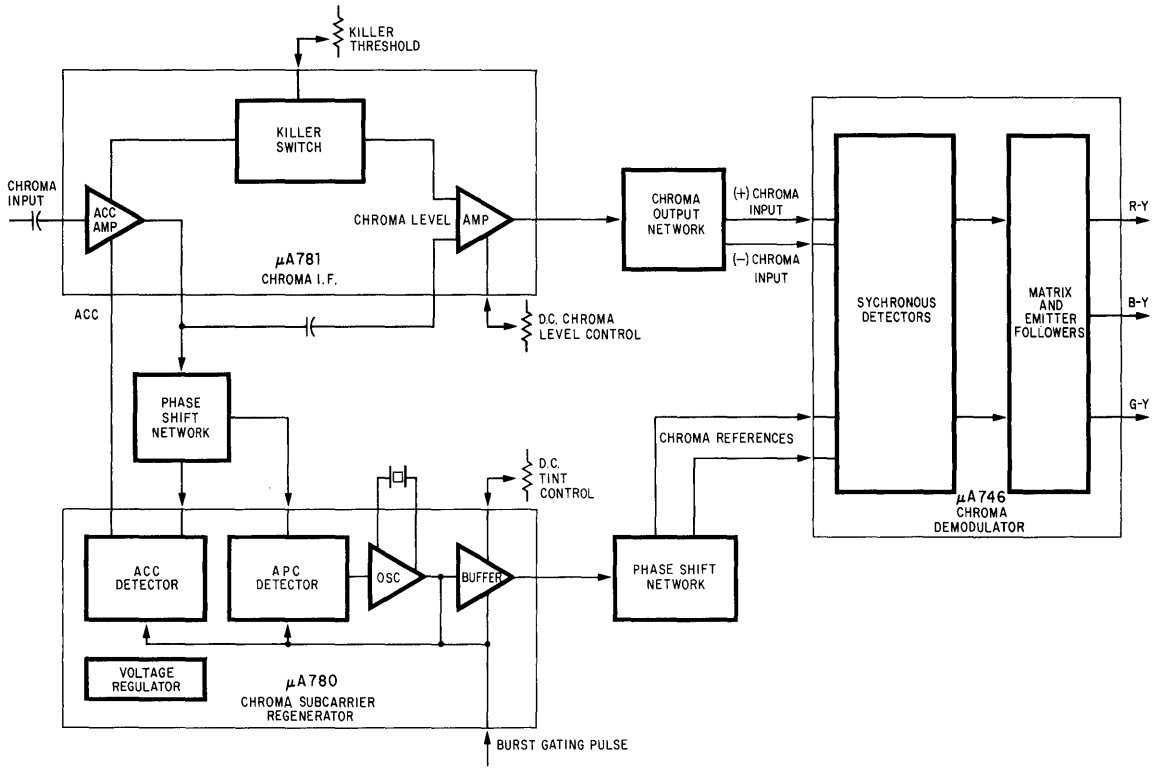


INTEGRATED CIRCUIT COLOR TV CHROMA PROCESSING SYSTEM



INTEGRATED CIRCUIT COLOR TV CHROMA PROCESSING SYSTEM

(BLOCK DIAGRAM)



μA795

FOUR QUADRANT MULTIPLIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

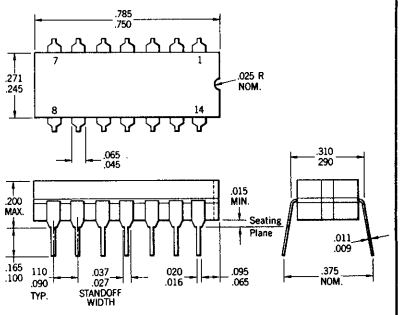
GENERAL DESCRIPTION — The μA795 is a four Quadrant Analog Multiplier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The μA795 provides excellent linearity and operates over a wide supply range and input voltage range. The differential output current is the product of two input analog voltages multiplied by a pre-determined scale factor. The μA795 is ideally suited for applications as a multiplier, squarer, divider, phase detector, frequency doubler or balanced modulator.

- **EXCELLENT LINEARITY**
- **HIGH INPUT VOLTAGE RANGE**
- **WIDE SUPPLY VOLTAGE OPERATION**
- **WIDE BANDWIDTH**
- **EXCELLENT PHASE MATCHING**
- **ADJUSTABLE GAIN FACTOR**
- **EXCELLENT TEMPERATURE STABILITY**

ABSOLUTE MAXIMUM RATINGS

Applied Voltage (Note 1)	30 V
Differential Input Signal	$V_9 - V_{12} = \pm(6 + I_{13} R_x)$
	$V_4 - V_8 = \pm(6 + I_3 R_y)$
Maximum Bias Current	10 mA
Power Dissipation (Note 2)	670 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (soldering, 60 seconds)	300°C

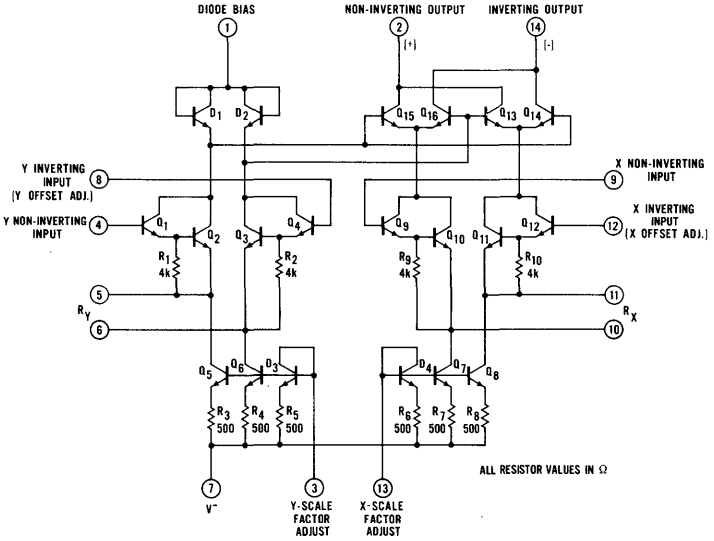
PHYSICAL DIMENSIONS
In accordance with JEDEC (TO-116) outline



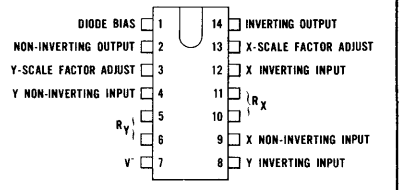
NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

ORDER PART NO. U6A7795393

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM



Notes on following page.

*Planar is a patented Fairchild process.

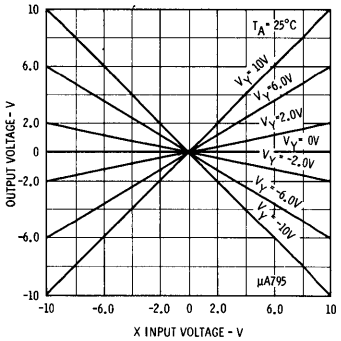
ELECTRICAL CHARACTERISTICS (Note 3; $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Linearity Error in % Of Full Scale	$-10 < V_X < +10$	$V_Y = +10\,V$		1.0	2.0	%
	$-10 < V_X < +10$	$V_Y = -10\,V$		2.0		%
	$-10 < V_Y < +10$	$V_X = +10\,V$		2.0	4.0	%
	$-10 < V_Y < +10$	$V_X = -10\,V$		2.0	4.0	%
Squaring Mode Error				0.75		%
Scale Factor Adjustable $K = \frac{2\,R_L}{I_3\,R_X\,R_Y}$				0.1		—
Input Resistance	f = 20 Hz			20		MΩ
Differential Output Resistance	f = 20 Hz			300		kΩ
Input Bias Current				2.0	12	μA
Input Offset Current				0.4	2.0	μA
Frequency Response	−3 dB Bandwidth			3.0		MHz
	3° Relative Phase Shift			750		kHz
	1% Absolute Error Due to Input-Output Phase Shift			30		kHz
Input Voltage Range			±10.5	±12		V
Common Mode Gain			−40	−50		dB
Output Common Mode Voltage				21		V
Differential Output Voltage Swing				±14		V
Positive Supply Voltage Rejection Ratio				5.0		mV/V
Negative Supply Voltage Rejection Ratio				10		mV/V
Negative Supply Current				6.0	7.0	mA
Power Consumption				135	170	mW
The following specifications apply for $0°C \le T_A \le +70°C$:						
Linearity Error in % Of Full Scale	$-10 < V_X < +10$	$V_Y = +10\,V$		1.5		%
	$-10 < V_X < +10$	$V_Y = -10\,V$		3.0		%
	$-10 < V_Y < +10$	$V_X = +10\,V$		3.0		%
	$-10 < V_Y < +10$	$V_X = -10\,V$		3.0		%
Squaring Mode Error				1.0		%
Average Temperature Coefficient Of Input Offset Current				2.0		nA/°C

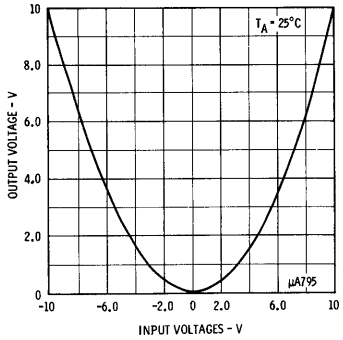
NOTES:
(1) Voltage applied between pins 2-1, 14-1, 1-9, 1-12, 1-4, 1-8, 12-7, 9-7, 8-7, 4-7.
(2) Applies for ambient temperature to 70°C.
(3) Connected as shown in Figure 1, set up 1, with resistor values as shown.

TYPICAL ELECTRICAL CHARACTERISTICS

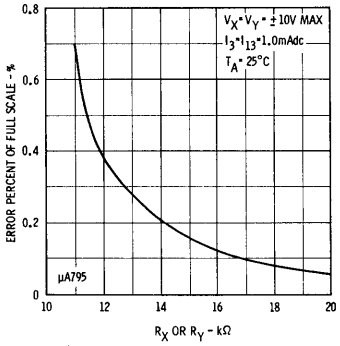
FOUR-QUADRANT MULTIPLIER TRANSFER CHARACTERISTIC



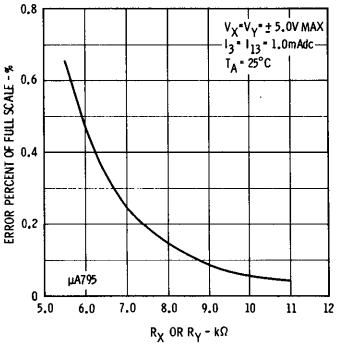
SQUARING MODE TRANSFER CHARACTERISTIC



ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER CHARACTERISTICS

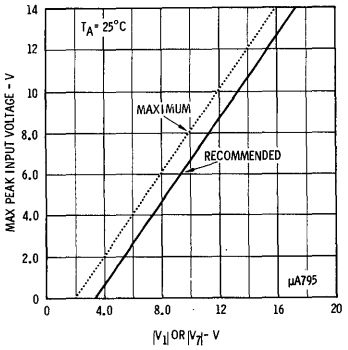


ERROR CONTRIBUTED BY INPUT DIFFERENTIAL AMPLIFIER CHARACTERISTICS

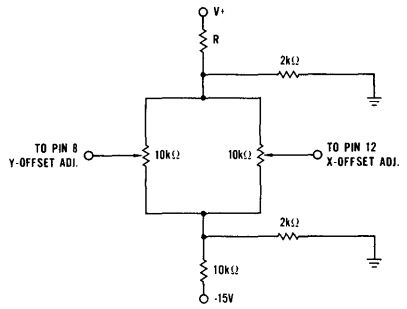


TYPICAL ELECTRICAL CHARACTERISTICS

MAXIMUM ALLOWABLE INPUT VOLTAGE VERSUS OUTPUT VOLTAGE (PIN 1 OR PIN 7)



OFFSET ADJUSTMENT

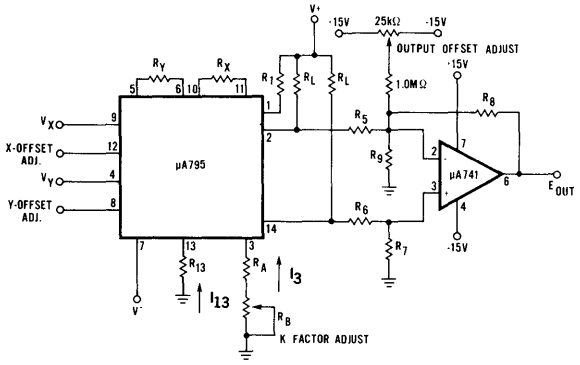


for $V^+ = 15$ V, $R = 10$ kΩ
$V^+ = 32$ V, $R = 22$ kΩ

For best output accuracy, use above network; see RECOMMENDED ZERO ADJUST AND SCALE SETTING PROCEDURE on back page.

TYPICAL APPLICATIONS

MULTIPLY WITH OP-AMP LEVEL SHIFT



SET UP	RESISTOR*	R_1	R_5	R_6	R_7	R_8	R_9	R_{13}	R_A	R_B	R_L	R_X	R_Y
	TOLERANCE	5%	1%	1%	1%	1%	1%	1%	5%	20%	0.5%	5%	5%
1	$V^+ = +32$ V, $V^- = -15$ V -10 V $\leq V_X \leq +10$ V -10 V $\leq V_Y \leq +10$ V	9.1	121	100	11	121	15	13.7	12	5.0	11	15	15
2	$V^+ = +15$ V, $V^- = -15$ V -5 V $\leq V_X \leq +5$ V -5 V $\leq V_Y \leq +5$ V	3.0	300	100	100	300	∞	13.7	12	5.0	3.4	8.2	8.2
3	$V^+ = +15$ V, $V^- = -15$ V -10 V $\leq V_X \leq +10$ V -10 V $\leq V_Y \leq +10$ V	1.2	121	100	11	910	13.7	13.7	12	5.0	1.5	15	15

*All resistors are k ohms

Figure 1

TYPICAL APPLICATIONS

DIVIDE AND SQUARE ROOT

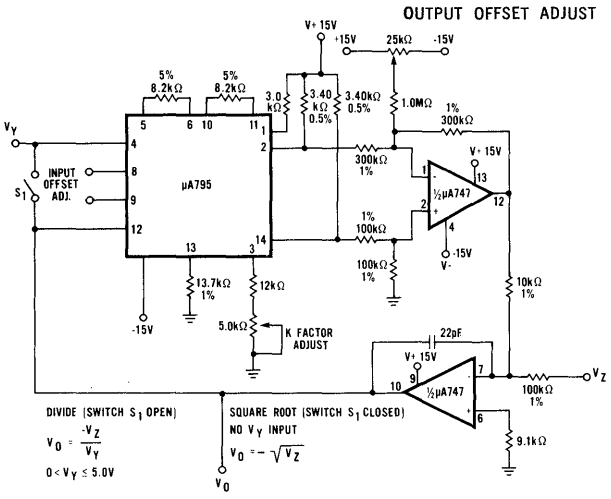


Figure 2

FREQUENCY DOUBLER

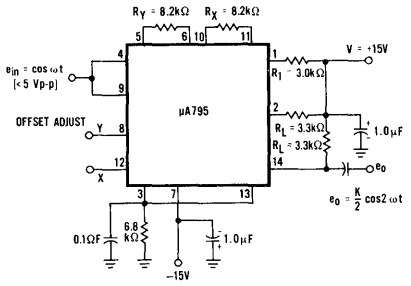


Figure 3

RECOMMENDED ZERO ADJUST AND SCALE SETTING PROCEDURE

With $V_X = V_Y = 0$ volts adjust the output offset adjustment until the output of the external amplifier reads zero volts. Set $V_X = 5.000$ volts, $V_Y = 0.000$ volt and adjust the Y-input offset control until the output amplifier reads zero volts. Repeat this procedure for $V_X = 0.000$ volt, $V_Y = 5.000$ volts and adjust the X-input offset control until the output amplifier reads zero volts. This procedure should be repeated until complete null is achieved.

Next, set $V_X = V_Y = 5.000$ volts and adjust the K factor potentiometer until the output reads the desired output.

$V_{out} = 2.500V = K V_X V_Y$ for a K factor of .100.

When a high degree of accuracy is unnecessary for small output signals, the above procedure may be simplified by eliminating the output offset adjustment.

SUGGESTIONS AND GENERAL PRECAUTIONS

The high frequency performance of the μA795 is primarily determined by two conditions. One, by the load resistors and the associated stray output capacitance of the multiplier and two, the operational amplifier used at the output. For maximum frequency of operation, low value load resistors and a μA715 wideband high slew rate operational amplifier should be used.

Phase shift at higher frequencies due to load resistors and output stray capacitances and relative phase shift between X and Y channels should be considered for maximum accuracy. As an example if the input to output phase shift is only 0.6°, the output product of two sine waves will exhibit a vector error of 1%. A 3° relative phase shift between the input signals will result in a vector error of 5%.

The normal circuit precautions should be taken to avoid parasitic oscillation. Leads should be as short as possible and the power supplies should be decoupled with a 0.1 μF high frequency capacitor. An RC parasitic suppression network of 510 Ω in series with a 10 pF from each input to ground can be used to reduce the Q_2 of a source-tuned circuit, which may cause the oscillation. As an alternate solution, a 510Ω resistor network can be placed in series with each input of the μA795.

μA796

DOUBLE-BALANCED MODULATOR/DEMODULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

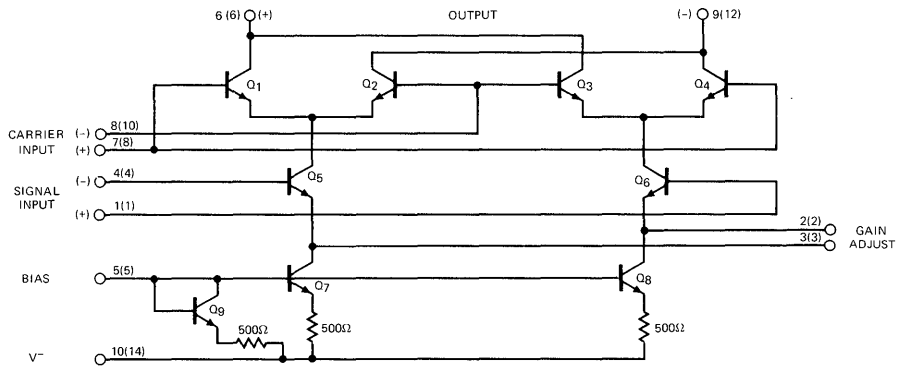
GENERAL DESCRIPTION – The μA796 is a monolithic Double-Balanced Modulator/Demodulator constructed on a single silicon chip using the Fairchild Planar* epitaxial process. This circuit produces an output voltage which is the product of an input voltage (signal) and a switching function (carrier). Communications applications include modulation and demodulation of AM, SSB, DSB, FSK, FM and phase encoded signals. Signal conditioning techniques possible include frequency doubling and halving, linear mixing and chopping, with additional uses as phase detectors in phase locked loops and as differentiators in NRZ and phase encoded digital tape and disk memories.

- **EXCELLENT CARRIER SUPPRESSION**
- **LOW OFFSETS AND DRIFT**
- **FULLY BALANCED INPUTS AND OUTPUT**
- **USEFUL TO 100 MHz**
- **WIDE RANGE OF APPLICATION**

ABSOLUTE MAXIMUM RATINGS

Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Ceramic DIP	670 mW
Applied Voltage (Note 2)	30 V
Differential Input Signal ($V_7 - V_8$)	±5.0 V
Differential Input Signal ($V_4 - V_1$)	$\pm(5 + I_5R_e)$ V
Input Signal ($V_2 - V_1$, $V_3 - V_4$)	5.0 V
Bias Current (I_5)	12 mA
Storage Temperature Range	
Metal Can, Ceramic DIP	−65°C to +150°C
Operating Temperature Range	
Military (312 Grade)	−55°C to +125°C
Commerical (393 Grade)	0°C to +70°C
Lead Temperature	
Metal Can, Ceramic DIP (Soldering, 60 seconds)	300°C

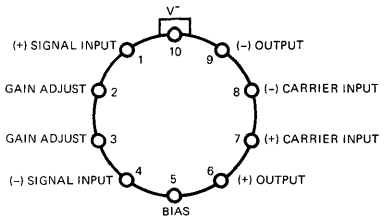
EQUIVALENT CIRCUIT



Pin numbers, see Note 3.

CONNECTION DIAGRAMS

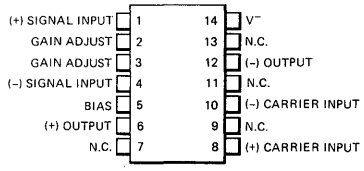
10 LEAD METAL CAN
(TOP VIEW)



Pin 10 electrically connected to case through substrate.

ORDER PART NOS: U5E7796312
U5E7796393

14 LEAD DIP
(TOP VIEW)



ORDER PART NOS:
For Ceramic DIP
U6A7796312
U6A7796393

Notes on following page.

*Planar is a patented Fairchild process.

312 GRADE

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Figure 1 unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Carrier Feedthrough	V_C = 60 mV (rms) sine wave f_C = 1.0 kHz, offset adjusted		40		μV (rms)
	V_C = 60 mV (rms) sine wave f_C = 10 MHz, offset adjusted		140		μV (rms)
	V_C = 300 mV_{pp} square wave f_C = 1.0 kHz, offset adjusted		0.04	0.2	mV (rms)
	V_C = 300 mV_{pp} square wave f_C = 1.0 kHz, offset not adjusted		20	100	mV (rms)
Carrier Suppression	f_S = 10 kHz, 300 mV (rms) f_C = 500 kHz, 60 mV (rms) sine wave offset adjusted	50	65		dB
	f_S = 10 kHz, 300 mV (rms) f_C = 10 MHz, 60 mV (rms) sine wave offset adjusted		50		dB
Transadmittance Bandwdith	R_L = 50Ω Carrier Input Port, V_C = 60 mV (rms) sine wave f_S = 1.0 kHz, 300 mV (rms) sine wave		300		MHz
	Signal Input Port, V_S = 300 mV (rms) sine wave $V_7 - V_8$ = 0.5 V dc		80		MHz
Voltage Gain, Signal Channel	V_S = 100 mV (rms), f = 1.0 kHz $V_7 - V_8$ = 0.5 V dc	2.5	3.5		V/V
Input Resistance, Signal Port	f = 5.0 MHz $V_7 - V_8$ = 0.5 V dc		200		kΩ
Input Capacitance, Signal Port	f = 5.0 MHz $V_7 - V_8$ = 0.5 V dc		2.0		pF
Single Ended Output Resistance	f = 10 MHz		40		kΩ
Single Ended Output Capacitance	f = 10 MHz		5.0		pF
Input Bias Current	$(I_1 + I_4)/2$		12	25	μA
Input Bias Current	$(I_7 + I_8)/2$		12	25	μA
Input Offset Current	$(I_1 - I_4)$		0.7	5.0	μA
Input Offset Current	$(I_7 - I_8)$		0.7	5.0	μA
Average Temperature Coefficient of Input Offset Current	(−55°C < T_A < +125°C)		2.0		nA/°C
Output Offset Current	$(I_6 - I_9)$		14	50	μA
Average Temperature Coefficient of Output Offset Current	(−55°C < T_A < +125°C)		90		nA/°C
Signal Port Common Mode Input Voltage Range	f_S = 1.0 kHz		5.0		V_{p-p}
Signal Port Common Mode Rejection Ratio	$V_7 - V_8$ = 0.5 V dc		−85		dB
Common Mode Quiescent Output Voltage			8.0		Vdc
Differential Output Swing Capability			8.0		V_{p-p}
Positive Supply Current	$(I_6 + I_9)$		2.0	3.0	mA
Negative Supply Current	(I_{10})		3.0	4.0	mA
Power Dissipation			33		mW

NOTES

1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for Metal Can and 8.3 mW/°C for the Ceramic DIP package.
2. Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.
3. Pin numbers are for TO-100 package in all specification tables. Parenthesis in Equivalent Circuit denotes DIP package.

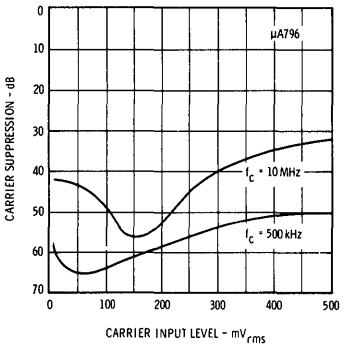
393 GRADE

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Figure 1 unless otherwise specified)

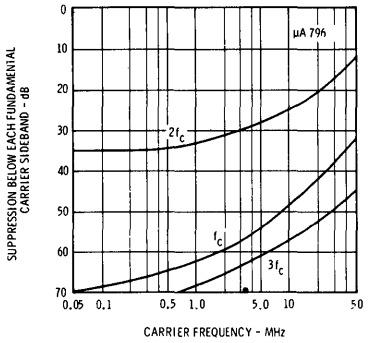
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Carrier Feedthrough	V_C = 60 mV (rms) sine wave f_C = 1.0 kHz, offset adjusted		40		μV (rms)
	V_C = 60 mV (rms) sine wave f_C = 10 MHz, offset adjusted		140		μV (rms)
	V_C = 300 mV_{pp} square wave f_C = 1.0 kHz, offset adjusted		0.04	0.2	mV (rms)
	V_C = 300 mV_{pp} square wave f_C = 1.0 kHz, offset not adjusted		20	150	mV (rms)
Carrier Suppression	f_S = 10 kHz, 300 mV (rms) f_C = 500 kHz, 60 mV (rms) sine wave offset adjusted	50	65		dB
	f_S = 10 kHz, 300 mV (rms) f_C = 10 MHz, 60 mV (rms) sine wave offset adjusted		50		dB
Transadmittance Bandwidth	R_L = 50Ω Carrier Input Port, V_C = 60 mV (rms) sine wave f_S = 1.0 kHz, 300 mV (rms) sine wave		300		MHz
	Signal Input Port, V_S = 300 mV (rms) sine wave $V_7 - V_8$ = 0.5 V dc		80		MHz
Voltage Gain, Signal Channel	V_S = 100 mV (rms), f = 1.0 kHz $V_7 - V_8$ = 0.5 V dc	2.5	3.5		V/V
Input Resistance, Signal Port	f = 5.0 MHz $V_7 - V_8$ = 0.5 V dc		200		kΩ
Input Capacitance, Signal Port	f = 5.0 MHz $V_7 - V_8$ = 0.5 V dc		2.0		pF
Single Ended Output Resistance	f = 10 MHz		40		kΩ
Single Ended Output Capacitance	f = 10 MHz		5.0		pF
Input Bias Current	$(I_1 + I_4)/2$		12	30	μA
Input Bias Current	$(I_7 + I_8)/2$		12	30	μA
Input Offset Current	$(I_1 - I_4)$		0.7	5.0	μA
Input Offset Current	$(I_7 - I_8)$		0.7	5.0	μA
Average Temperature Coefficient of Input Offset Current	$0°C \leq T_A \leq +70°C$		2.0		nA/°C
Output Offset Current	$(I_6 - I_9)$		14	60	μA
Average Temperature Coefficient of Output Offset Current	$0°C < T_A < +70°C$		90		nA/°C
Signal Port Common Mode Input Voltage Range	f_S = 1.0 kHz		5.0		V_{p-p}
Signal Port Common Mode Rejection Ratio	$V_7 - V_8$ = 0.5 V dc		–85		dB
Common Mode Quiescent Output Voltage			8.0		Vdc
Differential Output Swing Capability			8.0		V_{p-p}
Positive Supply Current	$(I_6 + I_9)$		2.0	3.0	mA
Negative Supply Current	(I_{10})		3.0	4.0	mA
Power Dissipation			33		mW

TYPICAL PERFORMANCE CURVES

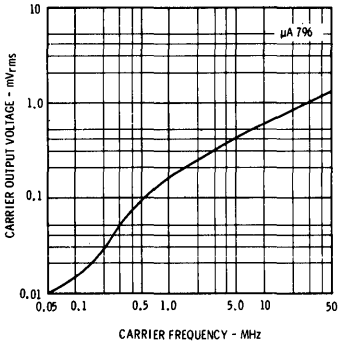
CARRIER SUPPRESSION VERSUS CARRIER INPUT LEVEL



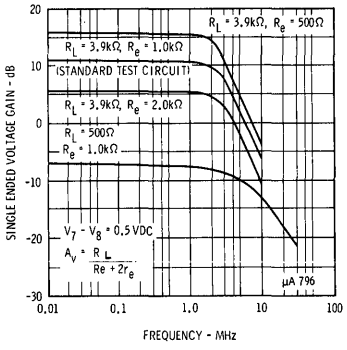
CARRIER SUPPRESSION VERSUS FREQUENCY



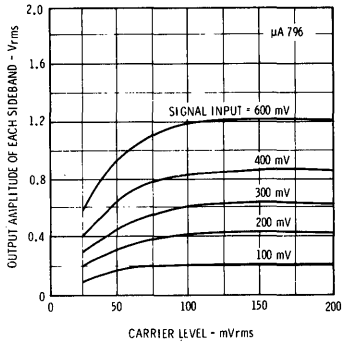
CARRIER FEEDTHROUGH VERSUS FREQUENCY



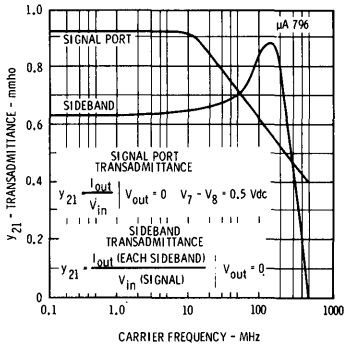
SIGNAL-PORT FREQUENCY RESPONSE



SIDEBAND OUTPUT VERSUS CARRIER LEVELS

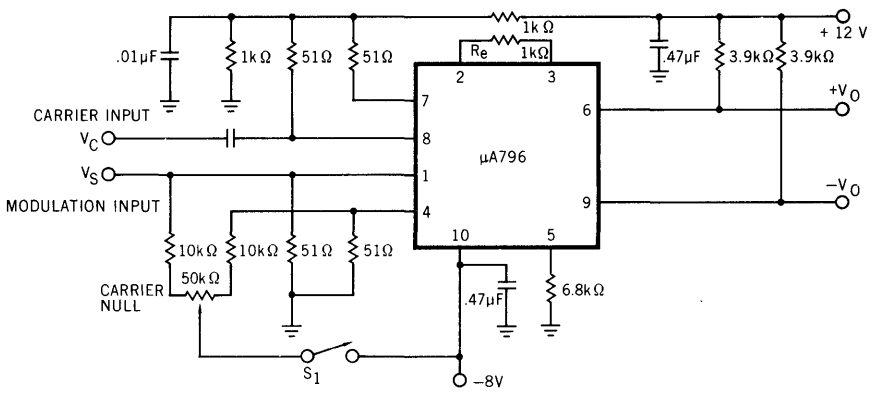


SIDEBAND AND SIGNAL PORT TRANSADMITTANCES VERSUS FREQUENCY



TYPICAL APPLICATIONS

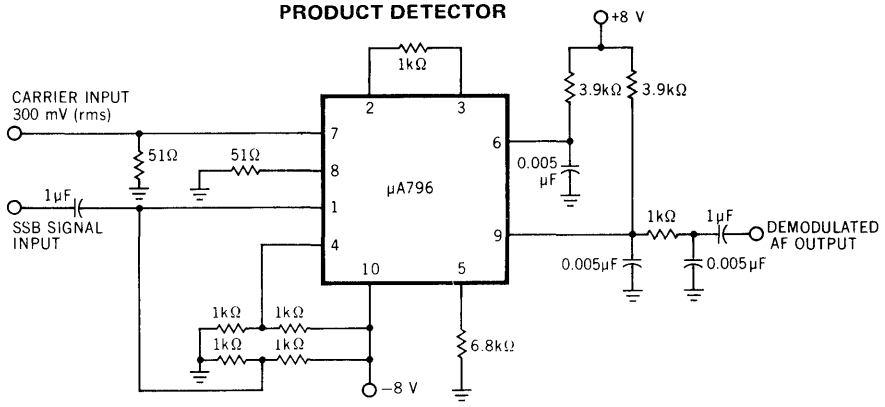
TYPICAL MODULATOR CIRCUIT



Note: S_1 is closed for "adjusted" measurements.

Fig. 1

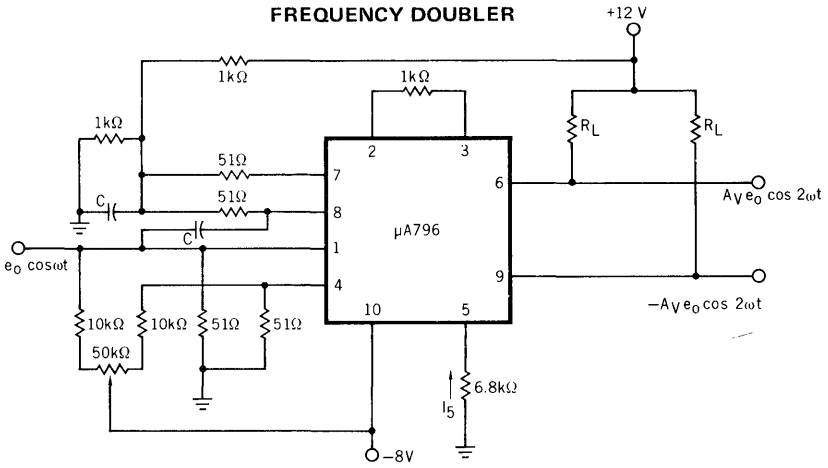
PRODUCT DETECTOR



This figure shows the μA796 used as a single sideband (SSB) suppressed carrier demodulator (product detector). The carrier signal is applied to the carrier input port with sufficient amplitude for switching operation. A carrier input level of 300 mV(rms) is optimum. The composite SSB signal is applied to the signal input port with an amplitude of 5.0 to 500 mV(rms). All output signal components except the desired demodulated audio are filtered out, so that an offset adjustment is not required. This circuit may also be used as an AM detector by applying composite and carrier signals in the same manner as described for product detector operation.

Fig. 2

FREQUENCY DOUBLER



The frequency doubler circuit shown will double low-level signals with low distortion. The value of C should be chosen for low reactance at the operating frequency.

Signal level at the carrier input must be less than 25 mV peak to maintain operation in the linear region of the switching differential amplifier. Levels to 50 mV peak may be used with some distortion of the output waveform. If a larger input signal is available a resistive divider may be used at the carrier input, with full signal applied to the signal input.

Fig. 3

μA7800 SERIES

THREE - TERMINAL POSITIVE VOLTAGE REGULATORS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

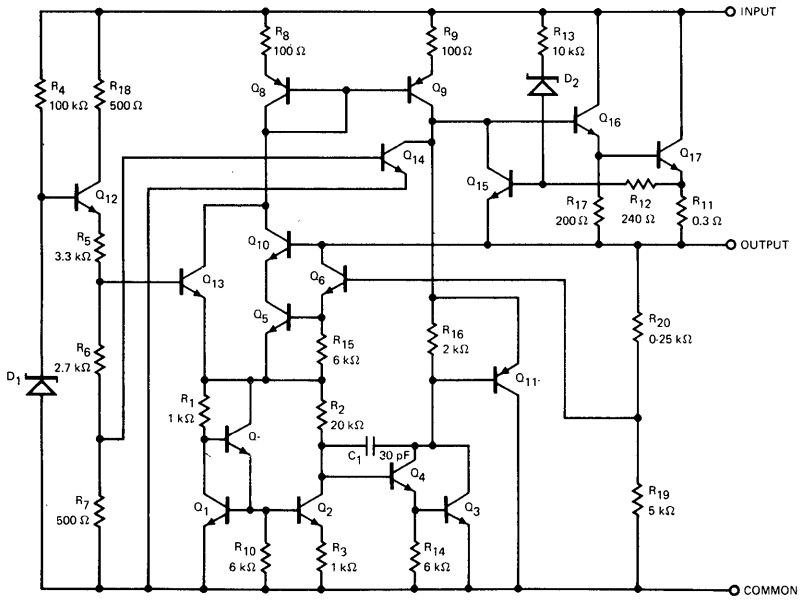
GENERAL DESCRIPTION — The μA7800 series of Three-Terminal Positive Voltage Regulators are constructed using the Fairchild Planar* epitaxial process. These regulators employ internal current limiting, thermal shutdown and safe-area compensation making them essentially blow-out proof. If adequate heat sinking is provided, they can deliver over 1A output current. They are intended as fixed-voltage regulators in a wide range of applications including local, on-card regulation for elimination of noise and distribution problems associated with single point regulation. In addition to use as fixed voltage regulators, these devices can be used with external components to obtain adjustable output voltages and currents and as the power pass element in precision regulators.

- **OUTPUT CURRENT IN EXCESS OF 1 AMP**
- **NO EXTERNAL COMPONENTS**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL SHORT CIRCUIT CURRENT LIMITING**
- **OUTPUT TRANSISTOR SAFE-AREA COMPENSATION**
- **AVAILABLE IN THE PLASTIC TO-220 AND THE METAL TO-3 PACKAGE**

ABSOLUTE MAXIMUM RATINGS

Input Voltage (5 V through 18 V)	35 V
(24 V)	40 V
Internal Power Dissipation (Note 1)	Internally Limited
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	0°C to +125°C
Lead Temperature (Soldering, 60 second time limit) TO-3 Package	300°C
(Soldering, 10 second time limit) TO-220 Package	230°C

EQUIVALENT CIRCUIT

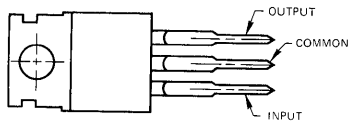


Note on following page.

VOLTAGE RANGE

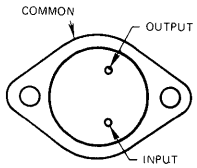
μA7805	5 V
μA7806	6 V
μA7808	8 V
μA7812	12 V
μA7815	15 V
μA7818	18 V
μA7824	24 V

CONNECTION DIAGRAMS
TO-220 PLASTIC POWER PACKAGE
(TOP VIEW)



ORDER PART NOS: UGH7805393
UGH7806393
UGH7808393
UGH7812393
UGH7815393
UGH7818393
UGH7824393

TO-3 PACKAGE
(TOP VIEW)



ORDER PART NOS: UGJ7805393
UGJ7806393
UGJ7808393
UGJ7812393
UGJ7815393
UGJ7818393
UGJ7824393

*Planar is a patented Fairchild process.

μA7805

ELECTRICAL CHARACTERISTICS (V_{IN} = 10 V, I_{OUT} = 500 mA, 0°C < T_J < 125°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C	4.8	5.0	5.2	V
Line Regulation	T_J = 25°C, I_{OUT} = 100 mA				
	7 V ≤ V_{IN} ≤ 25 V		7.0	50	mV
	8 V ≤ V_{IN} ≤ 12 V		2.0	25	mV
	T_J = 25°C, I_{OUT} = 500 mA				
	7 V ≤ V_{IN} ≤ 25 V		35	100	mV
	8 V ≤ V_{IN} ≤ 12 V		8.0	50	mV
Load Regulation	T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 1.5 A		11	100	mV
	250 mA ≤ I_{OUT} ≤ 750 mA		4.0	50	mV
Output Voltage	7 V ≤ V_{IN} ≤ 20 V, 5 mA ≤ I_{OUT} ≤ 1.0 A p ≤ 15 W	4.75		5.25	V
Quiescent Current	T_J = 25°C		4.3	8.0	mA
Quiescent Current Change	7 V ≤ V_{IN} ≤ 25 V			1.3	mA
	5 mA ≤ I_{OUT} ≤ 1.5 A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		40		μV
Long Term Stability				20	mV
Ripple Rejection	I_{OUT} = 20 mA, f = 120 Hz		70		dB
Dropout Voltage	I_{OUT} = 1A, T_J = 25°C		2.0		V
Output Resistance			30		mΩ
Short Circuit Current Limit	T_J = 25°C		750		mA
Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0°C ≤ T_A ≤ 125°C		−1.3		mV/°C

μA7806

ELECTRICAL CHARACTERISTICS (V_{IN} = 11 V, I_{OUT} = 500 mA, 0°C < T_J < 125°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C	5.75	6.0	6.25	V
Line Regulation	T_J = 25°C, I_{OUT} = 100 mA				
	8 V ≤ V_{IN} ≤ 25 V		9.0	60	mV
	9 V ≤ V_{IN} ≤ 13 V		3.0	30	mV
	T_J = 25°C, I_{OUT} = 500 mA				
	8 V ≤ V_{IN} ≤ 25 V		43	120	mV
	9 V ≤ V_{IN} ≤ 13 V		10	60	mV
Load Regulation	T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 1.5 A		13	120	mV
	250 mA ≤ I_{OUT} ≤ 750 mA		5.0	60	mV
Output Voltage	8 V ≤ V_{IN} ≤ 21 V, 5 mA ≤ I_{OUT} ≤ 1.0 A p ≤ 15 W	5.7		6.3	V
Quiescent Current	T_J = 25°C		4.3	8.0	mA
Quiescent Current Change	8 V ≤ V_{IN} ≤ 25 V			1.3	mA
	5 mA ≤ I_{OUT} ≤ 1.5 A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		45		μV
Long Term Stability				24	mV
Ripple Rejection	I_{OUT} = 20 mA, f = 120 Hz		65		dB
Dropout Voltage	I_{OUT} = 1 A, T_J = 25°C		2.0		V
Output Resistance	I_{OUT} = 500 mA		35		mΩ
Short Circuit Current Limit	T_J = 25°C		550		mA
Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0°C ≤ T_A ≤ 125°C		−1.0		mV/°C

NOTE 1. Thermal resistance without a heat sink for junction to case temperature is 4.0°C/W for TO-3 package, 2.0°C/W for TO-220 package; ambient to case temperature is 35°C/W for TO-3 package and 50°C/W for TO-220 package.

μA7808

ELECTRICAL CHARACTERISTICS (V_{IN} = 14 V, I_{OUT} = 500 mA, 0°C < T_J < 125°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C	7.7	8.0	8.3	V
Line Regulation	T_J = 25°C, I_{OUT} = 100 mA				
	10.5 V ≤ V_{IN} ≤ 25 V		12	80	mV
	11 V ≤ V_{IN} ≤ 17 V		5.0	40	mV
	T_J = 25°C, I_{OUT} = 500 mA				
	10.5 V ≤ V_{IN} ≤ 25 V		50	160	mV
	11 V ≤ V_{IN} ≤ 17 V		22	80	mV
Load Regulation	T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 1.5 A		26	160	mV
	250 mA ≤ I_{OUT} ≤ 750 mA		9.0	80	mV
Output Voltage	10.5 V ≤V_{IN}≤ 23 V, 5 mA ≤I_{OUT} ≤ 1.0 A, p ≤ 15 W	7.6		8.4	V
Quiescent Current	T_J = 25°C		4.3	8.0	mA
Quiescent Current Change	10.5 V ≤ V_{IN} ≤ 25 V			1.0	mA
	5 mA ≤ I_{OUT} ≤ 1.5 A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		52		μV
Long Term Stability				32	mV
Ripple Rejection	I_{OUT} = 20 mA, f = 120 Hz		62		dB
Dropout Voltage	I_{OUT} = 1 A, T_J = 25°C		2.0		V
Output Resistance	I_{OUT} = 500 mA		40		mΩ
Short Circuit Current Limit	T_J = 25°C		450		mA
Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0°C ≤ T_A ≤ 125°C		−1.0		mV/°C

μA7812

ELECTRICAL CHARACTERISTICS (V_{IN} = 19 V, I_{OUT} = 500 mA, 0°C < T_J < 125°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C	11.5	12.0	12.5	V
Line Regulation	T_J = 25°C, I_{OUT} = 100 mA				
	14.5 V ≤ V_{IN} ≤ 30 V		13	120	mV
	16 V ≤ V_{IN} ≤ 22 V		6.0	60	mV
	T_J = 25°C, I_{OUT} = 500 mA				
	14.5 V ≤ V_{IN} ≤ 30 V		55	240	mV
	16 V ≤ V_{IN} ≤ 22 V		24	120	mV
Load Regulation	T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 1.5 A		46	240	mV
	250 mA ≤ I_{OUT} ≤ 750 mA		17	120	mV
Output Voltage	14.5 V ≤ V_{IN} ≤ 27 V, 5 mA ≤ I_{OUT} ≤ 1.0 A, p ≤ 15 W			12.6	V
Quiescent Current	T_J = 25°C		4.4	8.0	mA
Quiescent Current Change	14.5 V ≤ V_{IN} ≤ 30 V			1.0	mA
	5 mA ≤ I_{OUT} ≤ 1.5 A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		75		μV
Long Term Stability				48	mV
Ripple Rejection	I_{OUT} = 20 mA, f = 120 Hz		61		dB
Dropout Voltage	I_{OUT} = 1 A, T_J = 25°C		2.0		V
Output Resistance	I_{OUT} = 500 mA		75		mΩ
Short Circuit Current Limit	T_J = 25°C		350		mA
Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0°C ≤ T_A ≤ 125°C		−2.0		mV/°C

μA7815

ELECTRICAL CHARACTERISTICS (V_{IN} = 23 V, I_{OUT} = 500 mA, 0°C < T_J < 125°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C	14.4	15.0	15.6	V
Line Regulation	T_J = 25°C, I_{OUT} = 100 mA				
	17.5 V ≤ V_{IN} ≤ 30 V		14	150	mV
	20 V ≤ V_{IN} ≤ 26 V		6.0	75	mV
	T_J = 25°C, I_{OUT} = 500 mA				
	17.5 V ≤ V_{IN} ≤ 30 V		57	300	mV
	20 V ≤ V_{IN} ≤ 26 V		27	150	mV
Load Regulation	T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 1.5 A		68	300	mV
	250 mA ≤ I_{OUT} ≤ 750 mA		25	150	mV
Output Voltage	17.5 V ≤ V_{IN} ≤ 30 V, 5 mA ≤ I_{OUT} ≤ 1.0 A, p ≤ 15 W	14.25		15.75	V
Quiescent Current	T_J = 25°C		4.4	8.0	mA
Quiescent Current Change	17.5 V ≤ V_{IN} ≤ 30 V			1.0	mA
	5 mA ≤ I_{OUT} ≤ 1.5 A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		90		μV
Long Term Stability				60	mV
Ripple Rejection	I_{OUT} = 20 mA, f = 120 Hz		60		dB
Dropout Voltage	I_{OUT} = 1 A, T_J = 25°C		2.0		V
Output Resistance	I_{OUT} = 500 mA		95		mΩ
Short Circuit Current Limit	T_J = 25°C		230		mA
Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0°C ≤ T_A ≤ 125°C		−2.0		mV/°C

μA7818

ELECTRICAL CHARACTERISTICS (V_{IN} = 27 V, I_{OUT} = 500 mA, 0°C < T_J < 125°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C	17.3	18.0	18.7	V
Line Regulation	T_J = 25°C, I_{OUT} = 100 mA				
	21 V ≤ V_{IN} ≤ 33 V		25	180	mV
	24 V ≤ V_{IN} ≤ 30 V		10	90	mV
	T_J = 25°C, I_{OUT} = 500 mA				
	21 V ≤ V_{IN} ≤ 33 V		90	360	mV
	24 V ≤ V_{IN} ≤ 30 V		50	180	mV
Load Regulation	T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 1.0 A		110	360	mV
	250 mA ≤ I_{OUT} ≤ 750 mA		55	180	mV
Output Voltage	21 V ≤ V_{IN} ≤ 33 V, 5 mA ≤ I_{OUT} ≤ 1.0 A p ≤ 15 W	17.1		18.9	V
Quiescent Current	T_J = 25°C		4.5	8.0	mA
Quiescent Current Change	21 V ≤ V_{IN} ≤ 33 V			1.0	mA
	5 mA ≤ I_{OUT} ≤ 1.0 A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		110		μV
Long Term Stability				72	mV
Ripple Rejection	I_{OUT} = 20 mA, f = 120 Hz		59		dB
Dropout Voltage	I_{OUT} = 1 A, T_J = 25°C		2.0		V
Output Resistance	I_{OUT} = 500 mA		110		mΩ
Short Circuit Current Limit	T_J = 25°C		200		mA
Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0°C ≤ T_A ≤ 125°C		−1.0		mV/°C

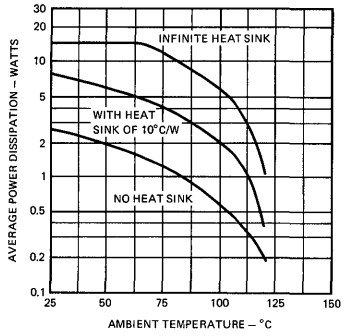
μA7824

ELECTRICAL CHARACTERISTICS (V_{IN} = 33 V, I_{OUT} = 500 mA, 0°C < T_J < 125°C, unless otherwise specified)

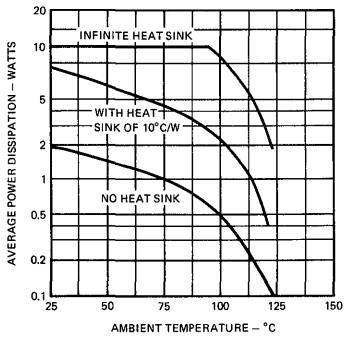
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	T_J = 25°C	23.0	24.0	35.0	V
Line Regulation	T_J = 25°C, I_{OUT} = 100 mA				
	27 V ≤ V_{IN} ≤ 38 V		31	240	mV
	30 V ≤ V_{IN} ≤ 36 V		14	120	mV
	T_J = 25°C, I_{OUT} = 500 mA				
	27 V ≤ V_{IN} ≤ 38 V		118	480	mV
	30 V ≤ V_{IN} ≤ 36 V		70	240	mV
Load Regulation	T_J = 25°C, 5 mA ≤ I_{OUT} ≤ 1.0 A		150	480	mV
	250 mA ≤ I_{OUT} ≤ 750 mA		85	240	mV
Output Voltage	27 V ≤ V_{IN} ≤ 38 V, 5 mA ≤ I_{OUT} ≤ 1.0 A	22.8		25.2	V
	p ≤ 15 W				
Quiescent Current	T_J = 25°C		4.6	8.0	mA
Quiescent Current Change	27 V ≤ V_{IN} ≤ 38 V			1.0	mA
	5 mA ≤ I_{OUT} ≤ 1.0 A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ f ≤ 100 kHz		170		μV
Long Term Stability				96	mV
Ripple Rejection	I_{OUT} =20 mA, f = 120 Hz		56		dB
Dropout Voltage	I_{OUT} = 1 A, T_J = 25°C		2.0		V
Output Resistance	I_{OUT} = 500 mA		150		mΩ
Short Circuit Current Limit	T_J = 25°C		150		mA
Average Temperature Coefficient of Output Voltage	I_{OUT} = 5 mA, 0°C ≤ T_A ≤ 125°C		−1.0		mV/°C

TYPICAL PERFORMANCE CURVES

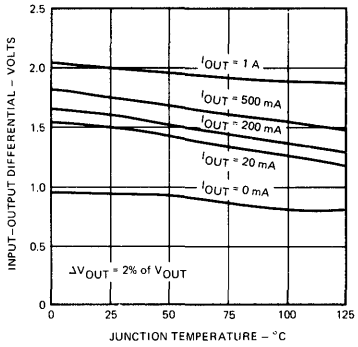
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-3 PACKAGE)



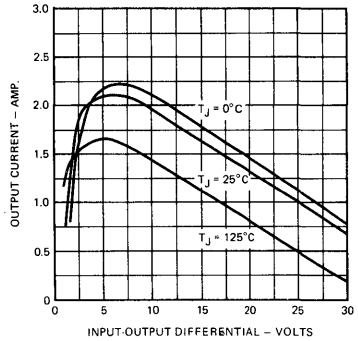
MAXIMUM AVERAGE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE (TO-220 PACKAGE)



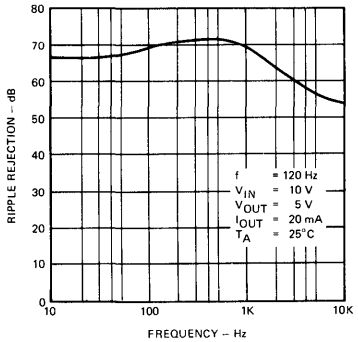
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



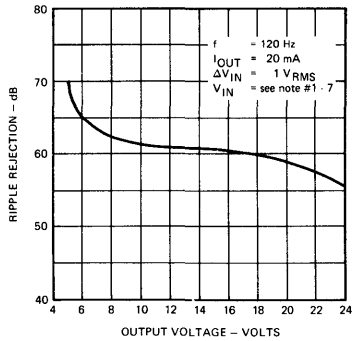
PEAK OUTPUT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE



RIPPLE REJECTION AS A FUNCTION OF FREQUENCY

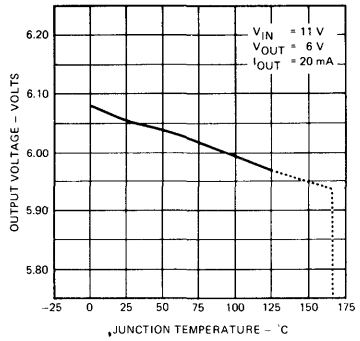


RIPPLE REJECTION AS A FUNCTION OF OUTPUT VOLTAGES

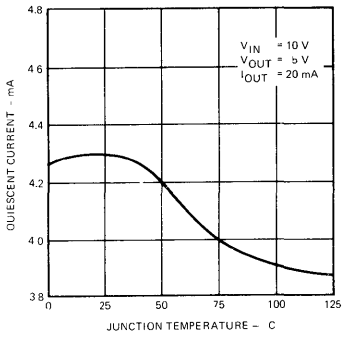


TYPICAL PERFORMANCE CURVES (cont'd)

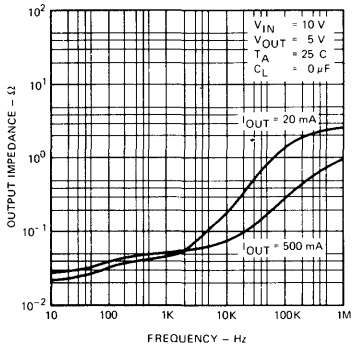
OUTPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



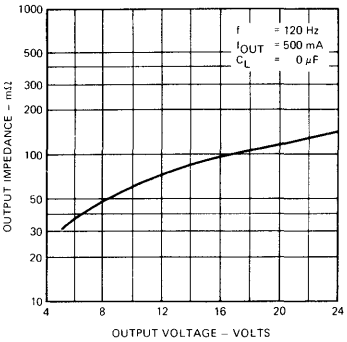
QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



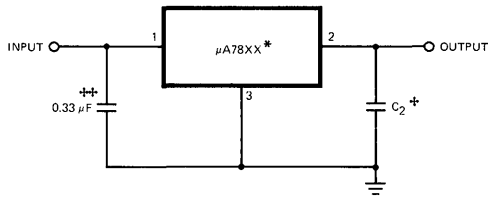
OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



OUTPUT IMPEDANCE AS A FUNCTION OF OUTPUT VOLTAGE

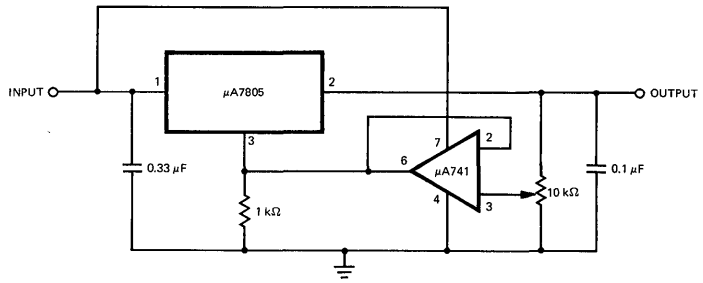


APPLICATIONS



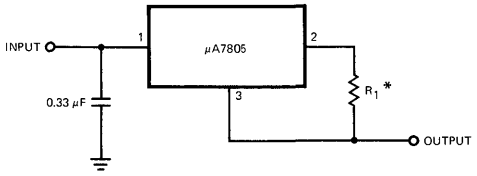
NOTES:
*To specify an output voltage, substitute voltage value for "XX".
+Although no output capacitor is needed for stability, it does improve transient response.
++ Required if regulator is located an appreciable distance from power supply filter.

FIXED OUTPUT REGULATOR



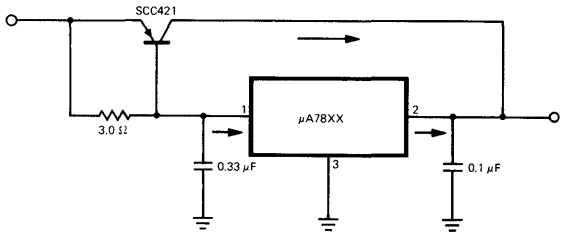
V_{OUT}, 7 V to 20 V
$V_{IN} - V_{OUT} \geq 2$ V

ADJUSTABLE OUTPUT REGULATOR – HIGH LINE REGULATION



*R_1 determines output current.

CURRENT REGULATOR



HIGH CURRENT VOLTAGE REGULATOR

μA9614
DUAL DIFFERENTIAL LINE DRIVER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA9614 is a TTL compatible Dual Differential Line Driver. It is designed to drive transmission lines either differentially or single-ended, back-matched or terminated. The outputs are similar to TTL, with the active pull-up and the pull-down split and brought out to adjacent pins. This allows multiplex operation (Wired-OR) at the driving site in either the single-ended mode via the uncommitted collector, or in the differential mode by use of the active pull-ups on one side and the uncommitted collectors on the other (See Fig. 5). The active pull-up is short circuit protected and offers a low output impedance to allow back-matching. The two pairs of outputs are complementary providing "NAND" and "AND" functions of the inputs, adding greater flexibility. The input and output levels are TTL compatible with clamp diodes provided at both, input and output, to handle line transients.

- **SINGLE 5 VOLT SUPPLY**
- **TTL COMPATIBLE INPUTS**
- **OUTPUT SHORT CIRCUIT PROTECTION**
- **INPUT CLAMP DIODES**
- **OUTPUT CLAMP DIODES FOR TERMINATION OF LINE TRANSIENTS**
- **COMPLIMENTARY OUTPUTS FOR 'NAND', 'AND' OPERATION**
- **UNCOMMITTED COLLECTOR OUTPUTS FOR WIRED-OR APPLICATION**
- **MILITARY TEMPERATURE RANGE**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

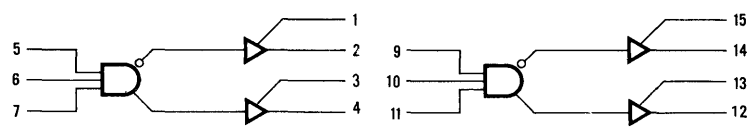
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.7 V to +7.0 V
Input Voltage	−0.5 V to +5.5 V
Voltage Supplied to Outputs (Open Collector)	−0.5 V to +12 V
Lead Temperature (Soldering, 60 seconds)	300°C
Internal Power Dissipation (Note 1)	
Ceramic DIP	730 mW
Flatpak	570 mW

NOTE

1. Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3 mW/°C for the Ceramic DIP and 7.1 mW/°C for the Flatpak Package.

ORDER INFORMATION – Specify U7B9614XXX for 16-pin Dual In-Line Package or U4L9614XXX for the 16-pin Flatpak where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

LOGIC DIAGRAM



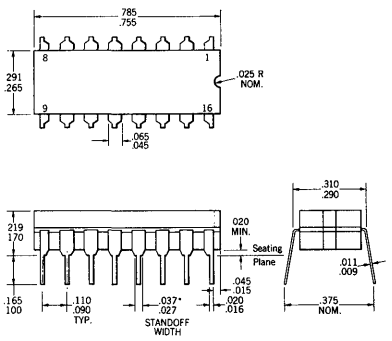
V_{CC} = Pin 16

Gnd = Pin 8

Fig. 3

PHYSICAL DIMENSIONS

16 Lead Dual In-Line

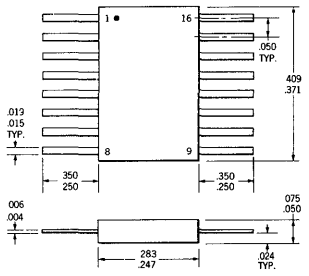


NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter Lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*The $\frac{.037}{.027}$ dimension does not apply to the corner leads

Fig. 1

FLAT PACKAGE

16 Lead BeO Cerpak



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

Fig. 2

ELECTRICAL CHARACTERISTICS
MILITARY TEMPERATURE RANGE (−55°C to +125°C, V_{CC} = 5.0 V ±10%) (U7B/4L961451X)

SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS & COMMENTS	
		−55°C		+25°C			+125°C				
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OL}	Output Low Voltage		400		200	400		400	mV	I_{OL} = 40 mA	V_{CC} = 4.5 V
V_{OH}	Output High Voltage	2.4		2.4	3.2		2.4		V	I_{OH} = −10 mA	V_{CC} = 4.5 V
I_{SC}	Output "Short Circuit" Current			−40	−90	−120			mA	V_{OUT} = 0.0 V	V_{CC} = 5.5 V
I_{CEX}	Output Leakage Current				10	100		200	μA	V_{CEX} = 12.0 V	V_{CC} = 5.5 V
I_F	Input Forward Current		−1.60		−1.10	−1.60		−1.60	mA	V_F = 0.4 V	V_{CC} = 5.5 V
I_R	Input Reverse Current				35	60		100	μA	V_R = 4.5 V	V_{CC} = 5.5 V
V_{IL}	Guaranteed Input Low Voltage		0.8		1.3	0.9		0.8	V	V_{CC} = 5.5 V	
V_{IH}	Guaranteed Input High Voltage	2.0		1.7	1.5		1.4		V	V_{CC} = 4.5 V	
V_{OLC}	Clamped Output Low Voltage				−0.8	−1.5			V	I_{OLC} = −40 mA	V_{CC} = 5.5 V
I_{CC}	Supply Current				34	48.7			mA	Inputs = 0 V	V_{CC} = 5.5 V
I_{max}	Supply Current				46	65.7			mA	Inputs = 0 V	V_{MAX} = 7.0 V
t_{PLH}	Turn-Off Time				14	20			ns	C_L = 30 pF	V_{CC} = 5.0 V
t_{PHL}	Turn-On Time				18	20			ns	See Fig. 4	V_M = 1.5 V
V_{IC}	Input Clamp Voltage				−1.0	−1.5			V	V_{CC} = 4.5 V	I_{IC} = −12 mA

ELECTRICAL CHARACTERISTICS
INDUSTRIAL TEMPERATURE RANGE (0°C to +75°C, V_{CC} = 5.0 V ±5%) (U7B/4L961459X)

SYMBOL	CHARACTERISTIC	LIMITS							UNITS	CONDITIONS & COMMENTS	
		0°C		+25°C			+75°C				
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OL}	Output Low Voltage		450		200	450		450	mV	I_{OL} = 40 mA	V_{CC} = 4.75 V
V_{OH}	Output High Voltage	2.4		2.4	3.2		2.4		V	I_{OH} = −10 mA	V_{CC} = 4.75 V
I_{SC}	Output "Short Circuit" Current			−40	−90	−120			mA	V_{OUT} = 0.0 V	V_{CC} = 5.25 V
I_{CEX}	Output Leakage Current				10	100		200	μA	V_{CEX} = 5.25 V	V_{CC} = 5.25 V
I_F	Input Forward Current		−1.60		−1.10	−1.60		−1.60	mA	V_F = 0.45 V	V_{CC} = 5.25 V
I_R	Input Reverse Current				35	60		100	μA	V_R = 4.5 V	V_{CC} = 5.25 V
V_{IL}	Guaranteed Input Low Voltage		0.85		1.3	0.85		0.85	V	V_{CC} = 5.25 V	
V_{IH}	Guaranteed Input High Voltage	1.9		1.8	1.5		1.6		V	V_{CC} = 4.75 V	
V_{OLC}	Clamped Output Low Voltage				−0.8	−1.5			V	I_{OLC} = −40 mA	V_{CC} = 5.25 V
I_{CC}	Supply Current				33	48.7			mA	Inputs = 0 V	V_{CC} = 5.25 V
I_{max}	Supply Current				46	70			mA	Inputs = 0 V	V_{MAX} = 7.0 V
t_{PLH}	Turn-Off Time				14	30			ns	C_L = 30 pF	V_{CC} = 5.0 V
t_{PHL}	Turn-On Time				18	30			ns	See Fig. 4	V_M = 1.5 V
V_{IC}	Input Clamp Voltage				−1.0	−1.5			V	V_{CC} = 4.75 V	I_{IC} = −12 mA

SWITCHING CIRCUIT AND WAVEFORMS

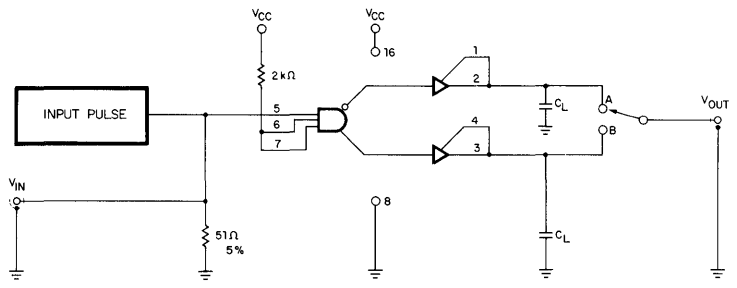
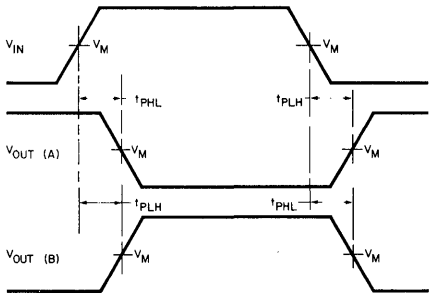


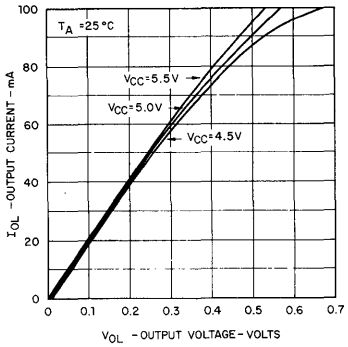
Fig. 4



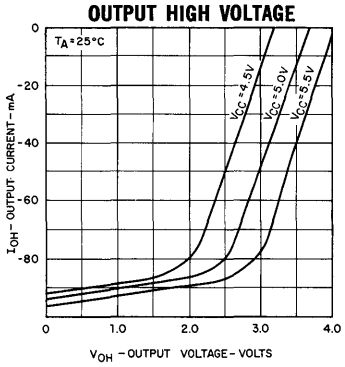
INPUT PULSE
Frequency = 500 kHz
Amplitude = 3.0 ±0.1 V
Pulse Width = 110 ±10 ns
$t_r = t_f \leq 5.0$ ns

TYPICAL ELECTRICAL CHARACTERISTICS

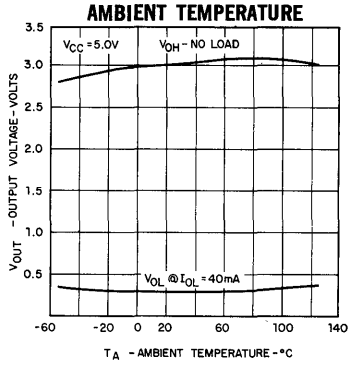
OUTPUT LOW CURRENT VERSUS OUTPUT LOW VOLTAGE



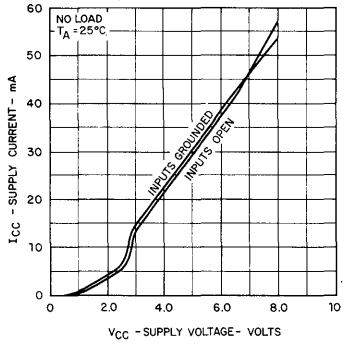
OUTPUT HIGH CURRENT VERSUS OUTPUT HIGH VOLTAGE



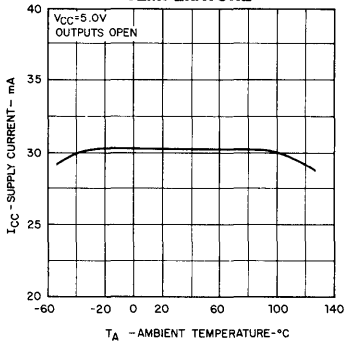
LOGIC LEVELS VERSUS AMBIENT TEMPERATURE



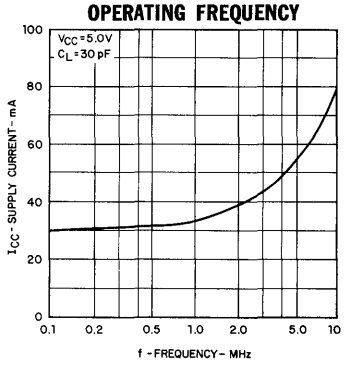
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



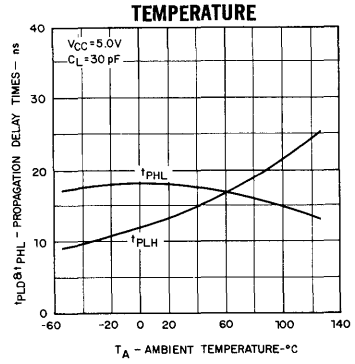
SUPPLY CURRENT VERSUS TEMPERATURE



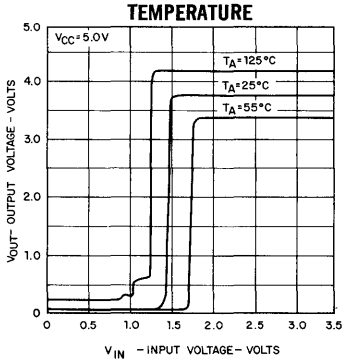
SUPPLY CURRENT VERSUS OPERATING FREQUENCY



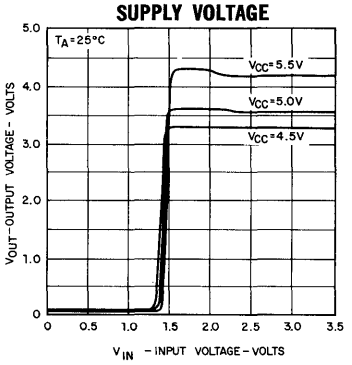
PROPAGATION DELAY TIME VERSUS TEMPERATURE



TRANSFER CHARACTERISTICS VERSUS TEMPERATURE

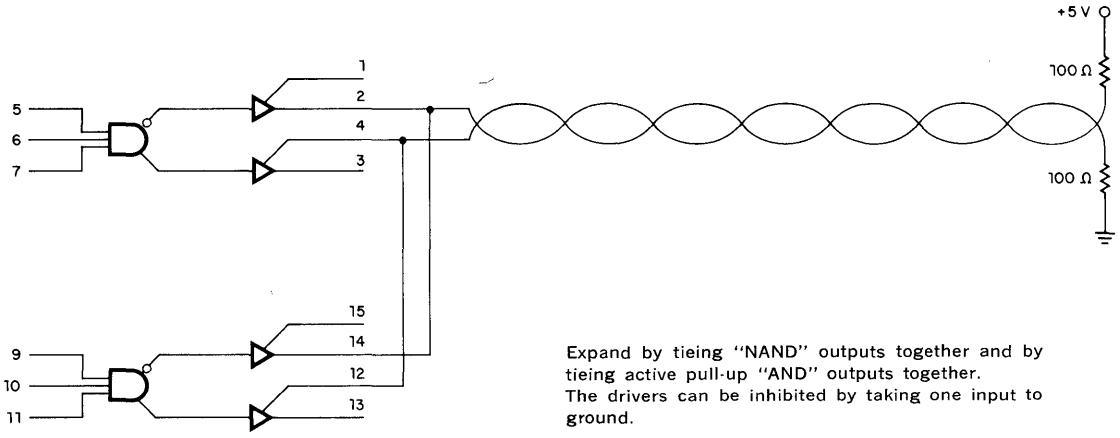


TRANSFER CHARACTERISTICS VERSUS SUPPLY VOLTAGE



APPLICATIONS

DIFFERENTIAL MODE EXPANSION



Expand by tieing "NAND" outputs together and by tieing active pull-up "AND" outputs together. The drivers can be inhibited by taking one input to ground.

Fig. 5

TYPICAL REFLECTION DIAGRAM

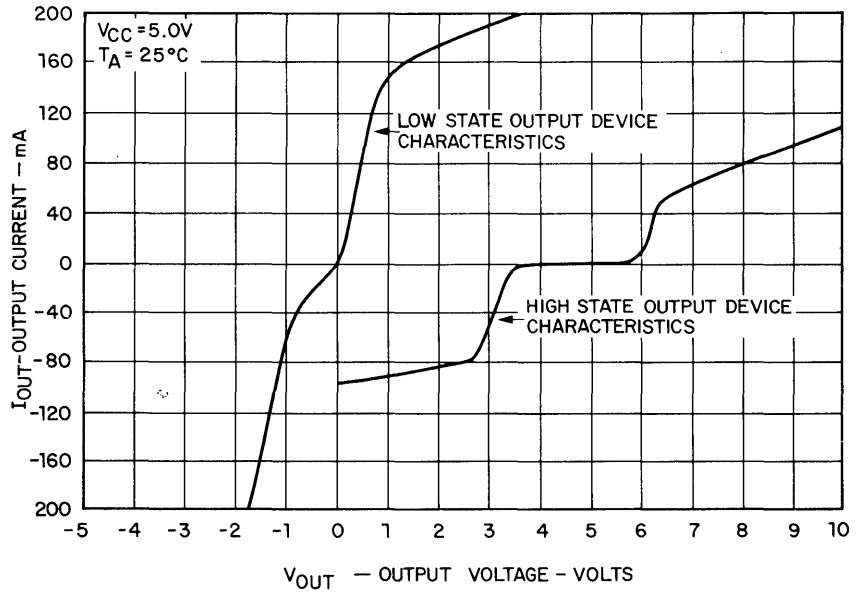


Fig. 6

μA9615
DUAL DIFFERENTIAL LINE RECEIVER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The μA9615 is a dual differential line receiver designed to receive differential digital data from transmission lines and operate over the military and industrial temperature ranges using a single 5 volt supply. It can receive ±500 mV of differential data in the presence of high level (±15 V) common mode voltages and deliver undisturbed TTL logic to the output.

The response time can be controlled by use of an external capacitor. A strobe is provided along with a 130 Ω terminating resistor (at the inputs). The output has an uncommitted collector with an active pull-up available on an adjacent pin.

- **TTL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE VOLTAGE RANGE**
- **CHOICE OF AN UNCOMMITTED COLLECTOR OR ACTIVE PULL-UP**
- **STROBE**
- **FULL MILITARY TEMPERATURE RANGE**
- **SINGLE 5 VOLT SUPPLY VOLTAGES**
- **FREQUENCY RESPONSE CONTROL**
- **130 Ω TERMINATING RESISTOR**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC1} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage Referred to Ground (Attenuator Inputs)	±20 V
Voltage Applied to Outputs for High Output State without Active Pull-up	−0.5 V to +13.2 V
Voltage Applied to Strobe	−0.5 V to +5.5 V
Lead Temperature (Soldering, 60 seconds)	300°C
Internal Power Dissipation (Note 1)	
Ceramic DIP	730 mW
Flatpak	570 mW

NOTE

1. Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3 mW/°C for the Ceramic DIP and 7.1 mW/°C for the Flatpak Package.

ORDER INFORMATION — Specify U7B9615XXX for 16-pin Dual In-Line Package or U4L9615XXX for 16-pin Flatpak where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

LOGIC DIAGRAM

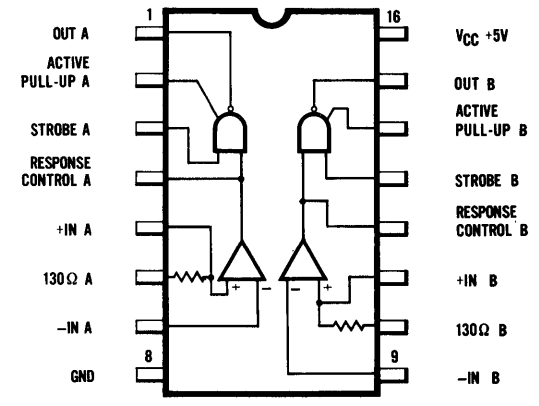
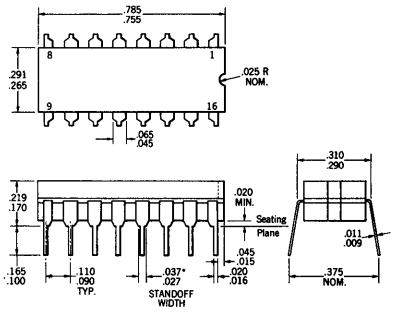


Fig. 3

PHYSICAL DIMENSION

16 Lead Dual In-Line

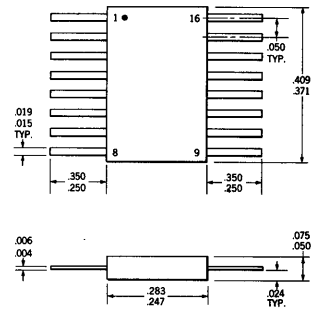


NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Hermetically sealed alumina ceramic package
Leads are tin-plated kovar
Package weight is 2.2 grams
*The .027/.037 dimension does not apply to the corner leads

Fig. 1

FLATPAK

16 Lead BeO Cerpak



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

Fig. 2

ELECTRICAL CHARACTERISTICS (Temperature Range −55°C to +125°C, V_{CC} = 5.0 V ±10%) (Part No. U7B/4L961551X)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OL}	Output Low Voltage		0.40		0.18	0.40		0.40	Volts	V_{CC} = 4.5 V, V_{OUT} = ** I_{OL} = 15.0 mA, *V_{DIFF} = 0.5 V
V_{OH}	Output High Voltage	2.2		2.4	3.2		2.4		Volts	V_{CC} = 4.5 V, V_{OUT} = ** I_{OH} = −5.0 mA, *V_{DIFF} = −0.5 V
I_{CEX}	Output Leakage Current					100		200	μA	V_{CEX} = 12 V, *V_{DIFF} = V_{CC} = 4.5 V
I_{SC}	Output Shorted Current			−15	−39	−80			mA	V_{CC} = 5.5 V, **V_{SC} = 0 V, *V_{DIFF} = −0.5 V
I_{IN}	Input Current		−0.9		−0.49	−0.7		−0.7	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V Other Input = 5.5 V
$I_{IN(ST)}$	Strobe Input Current				−1.15	−2.4			mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V *V_{DIFF} = 0.5 V
$I_{IN(R-C)}$	Response Control Input Current			−1.2	−3.4				mA	V_{CC} = 5.5 V, *V_{DIFF} = 0.5 V
V_{CM}	Common Mode Voltage	−15	+15	−15	±17.5	+15	−15	+15	Volts	V_{CC} = 5.0 V, *V_{DIFF} = 2.0 V
$I_{R(ST)}$	Strobe Input Leakage Current					2.0		5.0	μA	V_{CC} = 4.5 V, *V_{DIFF} = −0.5 V V_R = 4.5 V
R_{IN}	Input Resistor			77	130	167			ohms	V_{CC} = 5.0 V, $V_{IN(R)}$ = 1.0 V, +Input = Gnd.
V_{TH}	Differential Input Threshold Voltage		500		80	500		500	mV	V_{CC} = 5.0 V ±10%
I_{CC}	Power Supply Current				28.7	50			mA	V_{CC} = 5.5 V, −Inputs = 0 V, +Inputs = 0.5 V
t_{pd+}	Turn-off Time				30	50			ns	R_L = 3.9 kΩ, V_{CC} = 5.0 V, C_L = 30 pF, Fig. 4
t_{pd-}	Turn-on Time				30	50			ns	R_L = 390 Ω, V_{CC} = 5.0 V, C_L = 30 pF, Fig. 4

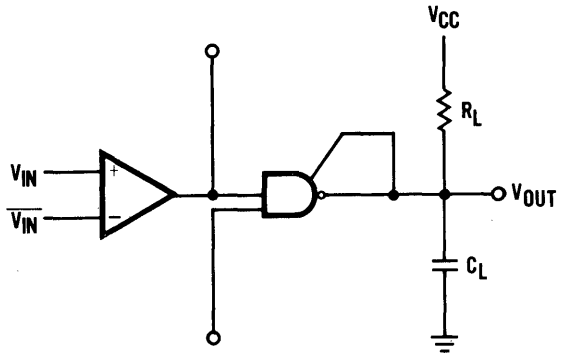
*V_{DIFF} is a differential input voltage referred from "+IN A" to "−IN A" and from "+IN B" to "−IN B".
**Connect Output "A" to Active Pull-up "A" and Output "B" to Active Pull-up "B".

ELECTRICAL CHARACTERISTICS (Temperature Range 0°C to +75°C, V_{CC} = 5.0 V ±5%) (Part No. U7B/4L961559X)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.45	Volts	V_{CC} = 4.75 V, V_{OUT} = ** I_{OL} = 15.0 mA, *V_{DIFF} = 0.5 V
V_{OH}	Output High Voltage	2.4		2.4	3.3		2.4		Volts	V_{CC} = 4.75 V, V_{OUT} = ** I_{OH} = −5.0 mA, *V_{DIFF} = −0.5 V
I_{CEX}	Output Leakage Current					100		200	μA	V_{CEX} = 5.25 V, *V_{DIFF} = V_{CC} = 4.75 V
I_{SC}	Output Shorted Current			−14		−100			mA	V_{CC} = 5.25 V, **V_{SC} = 0 V, *V_{DIFF} = −0.5 V
I_{IN}	Input Current		−0.9		−0.49	−0.7		−0.7	mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V Other Input = 5.25 V
$I_{IN(ST)}$	Strobe Input Current				−1.15	−2.4			mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V *V_{DIFF} = 0.5 V
$I_{IN(R-C)}$	Response Control Input Current			−1.2	−3.4				mA	V_{CC} = 5.25 V, *V_{DIFF} = 0.5 V
V_{CM}	Common Mode Voltage	−15	+15	−15	±17.5	+15	−15	+15	Volts	V_{CC} = 5.0 V, *V_{DIFF} = 2.0 V
$I_{R(ST)}$	Strobe Input Leakage Current					5.0		10	μA	V_{CC} = 4.75 V, *V_{DIFF} = −0.5 V V_R = 4.5 V
R_{IN}	Input Resistor			74	130	179			ohms	V_{CC} = 5.0 V, $V_{IN(R)}$ = 1.0 V, +Input = Gnd.
V_{TH}	Differential Input Threshold Voltage		500		80	500		500	mV	V_{CC} = 5.0 V ±5%
I_{CC}	Power Supply Current				28.7	50			mA	V_{CC} = 5.25 V, +Inputs = 0.5 V, −Inputs = 0 V
t_{pd+}	Turn-off Time				30	75			ns	R_L = 3.9 kΩ, V_{CC} = 5.0 V, C_L = 30 pF, Fig. 4
t_{pd-}	Turn-on Time				30	75			ns	R_L = 390 Ω, V_{CC} = 5.0 V, C_L = 30 pF, Fig. 4

*V_{DIFF} is a differential input voltage referred from "+IN A" to "−IN A" and from "+IN B" to "−IN B".
**Connect Output "A" to Active Pull-up "A" and Output "B" to Active Pull-up "B".

SWITCHING TIME TEST CIRCUIT



WAVEFORMS

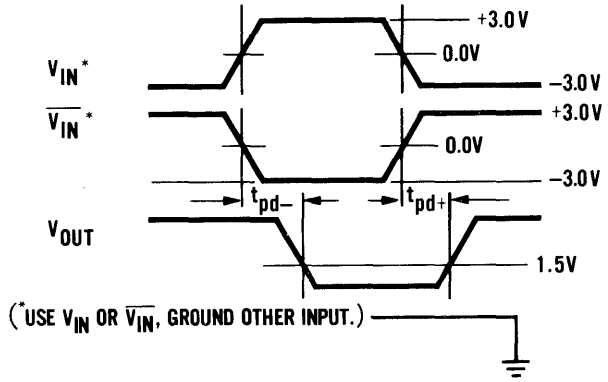
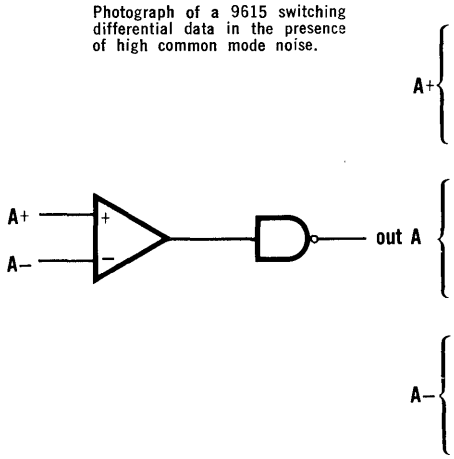
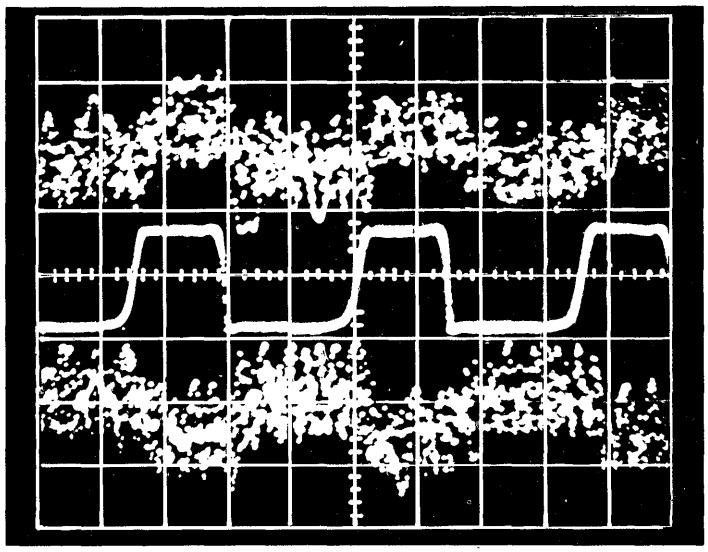


Fig. 4

Photograph of a 9615 switching differential data in the presence of high common mode noise.





VERTICAL=2.0V/DIV. HORIZONTAL=50ns/DIV.

Fig. 5

STANDARD USAGE

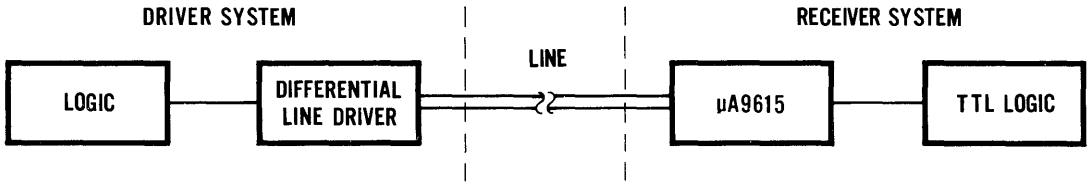
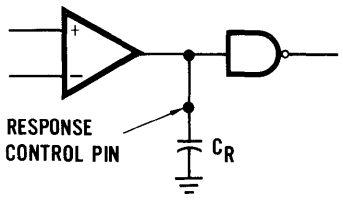


Fig. 6

FREQUENCY RESPONSE CONTROL



FREQUENCY RESPONSE VERSUS CAPACITANCE

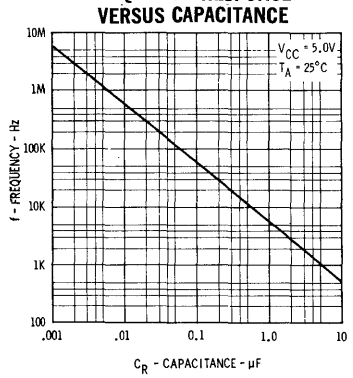
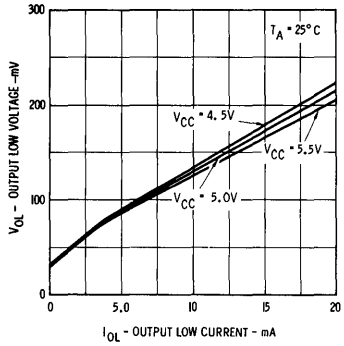


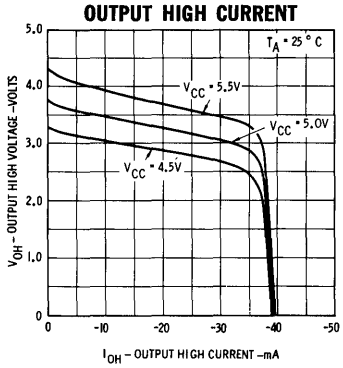
Fig. 7

TYPICAL ELECTRICAL CHARACTERISTICS

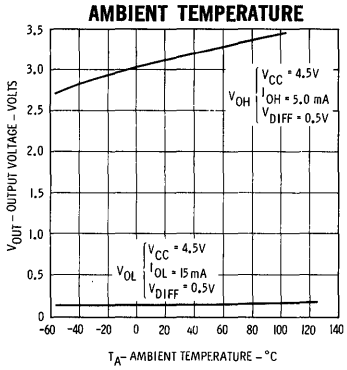
OUTPUT LOW VOLTAGE VERSUS OUTPUT LOW CURRENT



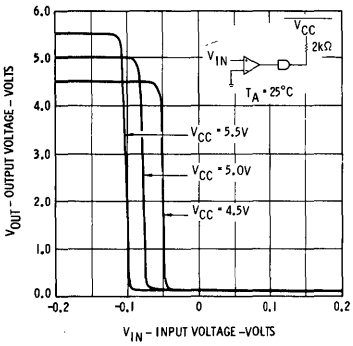
OUTPUT HIGH VOLTAGE VERSUS OUTPUT HIGH CURRENT



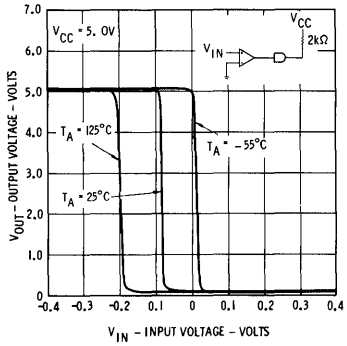
OUTPUT VOLTAGE VERSUS AMBIENT TEMPERATURE



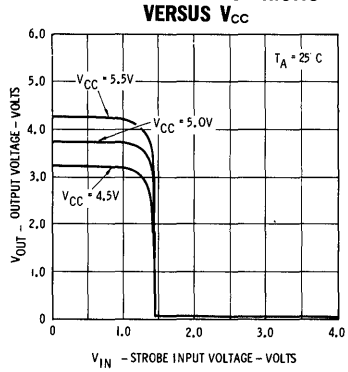
INPUT-OUTPUT TRANSFER CHARACTERISTIC VERSUS V_{CC}



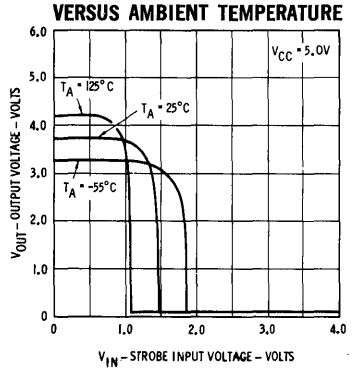
INPUT-OUTPUT TRANSFER CHARACTERISTIC VERSUS TEMPERATURE



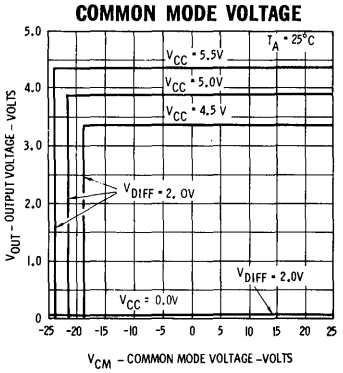
STROBE INPUT-OUTPUT TRANSFER CHARACTERISTIC VERSUS V_{CC}



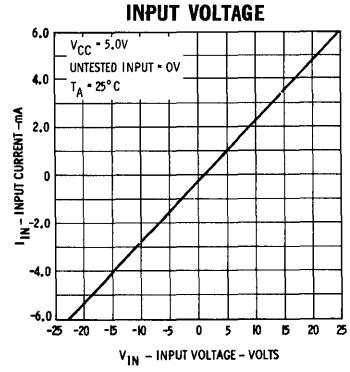
STROBE INPUT-OUTPUT TRANSFER CHARACTERISTIC VERSUS AMBIENT TEMPERATURE



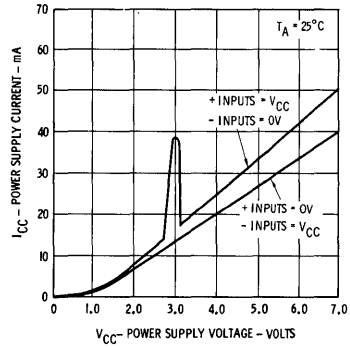
OUTPUT VOLTAGE VERSUS COMMON MODE VOLTAGE



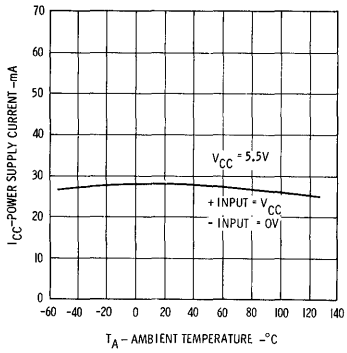
INPUT CURRENT VERSUS INPUT VOLTAGE



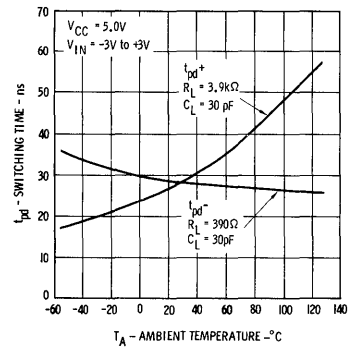
POWER SUPPLY CURRENT VERSUS POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE



SWITCHING TIME VERSUS AMBIENT TEMPERATURE



μA9620

DUAL DIFFERENTIAL LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The μA9620 is a dual differential line receiver designed to receive differential digital data from transmission lines and operate over the military and industrial temperature ranges. It can receive ±500 mV of differential data in the presence of high level (±15 V) common mode voltages and deliver undisturbed TTL logic to the output. In addition to line reception the μA9620 can perform many functions, a few of which are presented in the applications section. It can interface with nearly all input logic levels including CML, CTL, HLLDTL, RTL and TTL. HLLDTL logic can be provided by tieing the output to V_{CC2} (+12 V) through a resistor. The outputs can also be wire OR'ed. The μA9620 offers the advantages of logic compatible voltages (+5 V, +12 V), TTL output characteristics, and a flexible input array with a high common mode range. The direct inputs are provided in addition to the attenuated inputs (normally used) to allow the input attenuation and response time to be changed by use of external components.

- **TTL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE VOLTAGE RANGE**
- **WIRED-OR CAPABILITY**
- **DIRECT INPUTS (A_D, B_D)**
- **FULL MILITARY TEMPERATURE RANGE**
- **LOGIC COMPATIBLE SUPPLY VOLTAGES**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

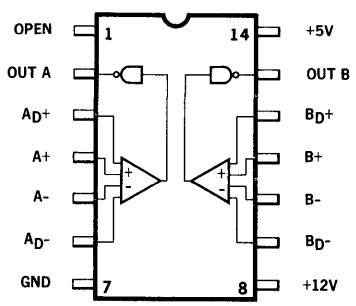
Storage Temperature	−65° C to +150° C
Temperature (Ambient) Under Bias	−55° C to +125° C
V_{CC1} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage Referred to Ground (Attenuator Inputs)	±20 V
Voltage Applied to Outputs for High Output State	−0.5 V to +13.2 V
V_{CC2} Pin Potential to Ground Pin	V_{CC1} to +15 V
Lead Temperature (Soldering, 60 seconds)	300° C
Internal Power Dissipation (Note 1)	
Ceramic DIP	670 mW
Flatpak	570 mW

NOTE

1. Rating applies to ambient temperatures up to 70° C. Above 70° C derate linearly at 8.3 mW/° C for the Ceramic DIP and 7.1 mW/° C for the Flatpak Package.

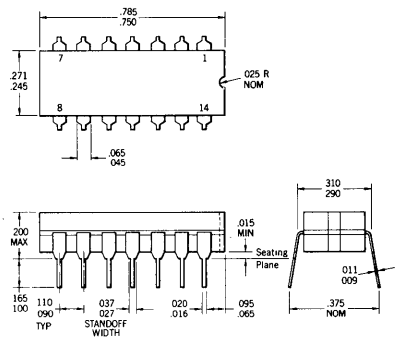
ORDER INFORMATION — Specify U6A9620XXX for 14-pin Dual In-Line Package or U3I9620XXX for 14-pin Flatpak where XXX is 51X for the −55° C to +125° C temperature range, or 59X for the 0° C to +75° C temperature range.

LOGIC DIAGRAM



PHYSICAL DIMENSIONS

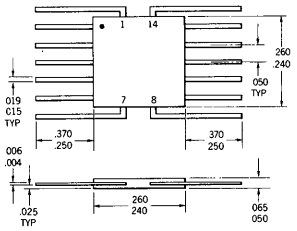
in accordance with JEDEC (TO-116) outline
14 Lead Dual-In-line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion.
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

FLAT PACKAGE

14 Lead BeO Cerpak



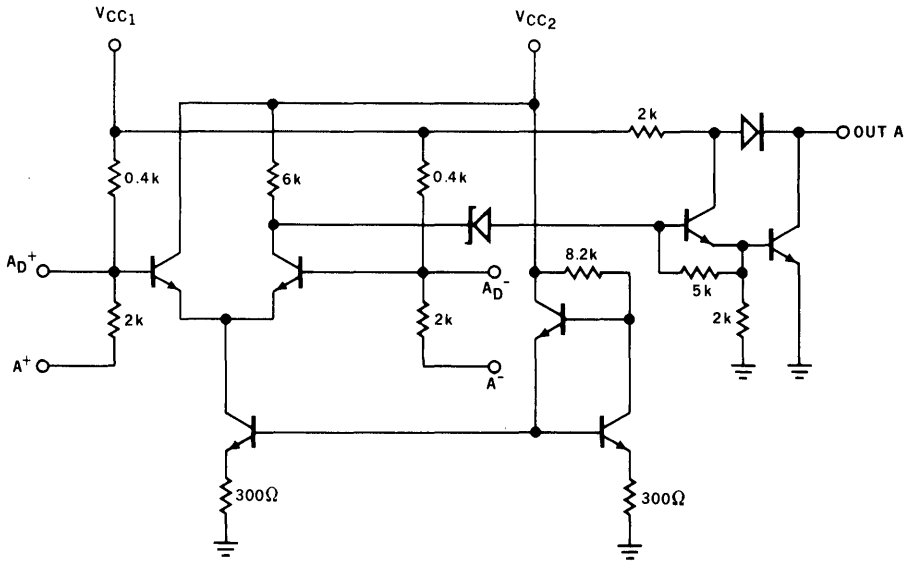
NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.26 gram

ELECTRICAL CHARACTERISTICS (Temperature Range −55° C to +125° C, V_{CC1} = 5.0 V ±10%, V_{CC2} = 12.0 V ±10%)

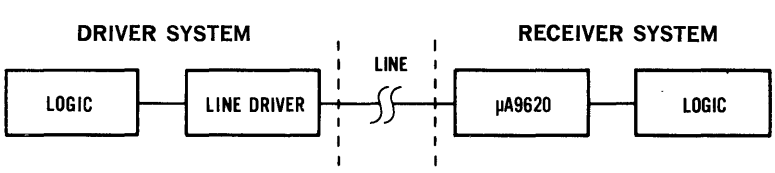
SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OL}	Output Low Voltage		0.40		0.21	0.40		0.45	Volts	V_{CC1} = 4.5 V I_{OL} = 15.0 mA	V_{CC2} = 10.8 V *V_{DIFF} = 0.5 V
V_{OH}	Output High Voltage	2.8		3.0	3.7		2.9		Volts	V_{CC1} = 4.5 V I_{OH} = −0.2 mA	V_{CC2} = 10.8 V *V_{DIFF} = −0.5 V
I_{CEX}	Output Leakage Current		50			100		200	μA	V_{CEX} = 13.2 V	
I_{SC}	Output Shorted Current			−1.4	−2.15	−3.1			mA	V_{CC1} = 5.0 V	V_{CC2} = 12.0 V
I_F	Input Forward Current		−3.1		−2.1	−3.0		−3.0	mA	V_{CC1} = 5.0 V	V_{CC2} = 12.0 V V_{Input} = 0 V+
†V_{TH}	Differential Input Threshold Voltage		500		120	500		500	mV	V_{CC1} = 5.0 V	V_{CC2} = 12.0 V
†V_{CM}	Common Mode Voltage	−15	15	−15	±17.5	15	−15	15	Volts	V_{CC1} = 5.0 V *V_{DIFF} = 2.0 V	V_{CC2} = 12.0 V
I_{VCC1}	5 V Supply Current		13		8.2	13		13	mA	V_{CC1} = 5.5 V V_{CC2} = 13.2 V	+Input = 5.5 V −Input = 0 V
I_{VCC2}	12 V Supply Current		8.0		5.6	8.0		8.0	mA	V_{CC1} = 5.5 V V_{CC2} = 13.2 V	+Input = 5.5 V −Input = 0 V
t_{pd+}	Turn-off Time				35	50			ns	R_L = 3.9 kΩ	C_L = 30 pF
t_{pd-}	Turn-on Time				20	50			ns	R_L = 390 Ω	C_L = 30 pF

†All input voltages are referred to the attenuated inputs (A^+, A^-, B^+, B^-)
*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.

Fig. 1 — SCHEMATIC DIAGRAM



STANDARD USAGE

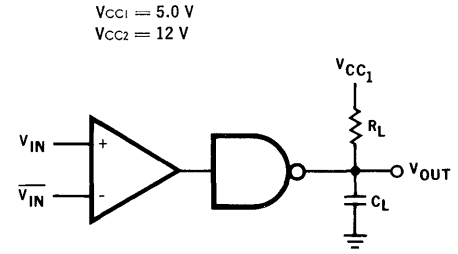


ELECTRICAL CHARACTERISTICS (Temperature Range 0°C to +75°C, V_{CC1} = 5.0 V ±5%, V_{CC2} = 12.0 V ±5%)

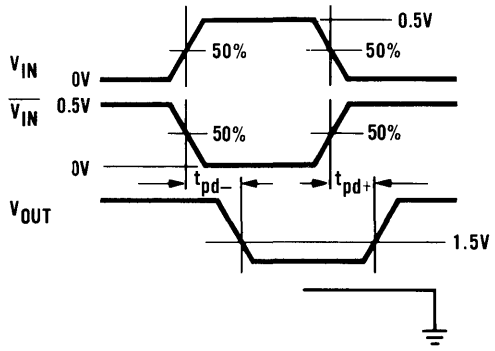
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.50	Volts	V_{CC1} = 4.75 V I_{OL} = 15.0 mA	V_{CC2} = 11.4 V *V_{DIFF} = 0.5 V
V_{OH}	Output High Voltage	2.8		3.0	3.3		2.9		Volts	V_{CC1} = 4.75 V I_{OH} = −0.2 mA	V_{CC2} = 12.6 V *V_{DIFF} = −0.5 V
I_{CEX}	Output Leakage Current		50			100		200	μA	V_{CEX} = 5.25 V	
I_{SC}	Output Shorted Current			−1.4	−2.15	−3.1			mA	V_{CC1} = 5.0 V	V_{CC2} = 12.0 V
I_F	Input Forward Current		−3.1		−2.1	−3.0		−3.0	mA	V_{CC1} = 5.0 V	V_{CC2} = 12.0 V V_{Input} = 0 V +
†V_{TH}	Differential Input Threshold Voltage		500		120	500		500	mV	V_{CC1} = 4.75 V	V_{CC2} = 12.6 V
†V_{CM}	Common Mode Voltage	−12	12	−12	±17.5	12	−12	12	Volts	V_{CC1} = 5.0 V *V_{DIFF} = 2.0 V	V_{CC2} = 12.0 V
I_{VCC1}	5 V Supply Current		13.5		8.2	13.5		13.5	mA	V_{CC1} = 5.25 V V_{CC2} = 12.6 V	+Input = 5.25 V −Input = 0 V
I_{VCC2}	12 V Supply Current		8.5		5.6	8.5		8.5	mA	V_{CC1} = 5.25 V V_{CC2} = 12.6 V	+Input = 5.25 V −Input = 0 V
t_{pd+}	Turn-off Time				35	75			ns	R_L = 3.9 kΩ	C_L = 30 pF
t_{pd-}	Turn-on Time				20	75			ns	R_L = 390 Ω	C_L = 30 pF

†All input voltages are referred to the attenuated inputs (A^+, A^-, B^+, B^-)
*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.

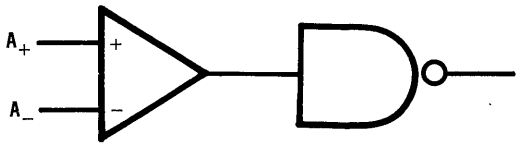
Fig. 2 — SWITCHING TIME TEST CIRCUIT

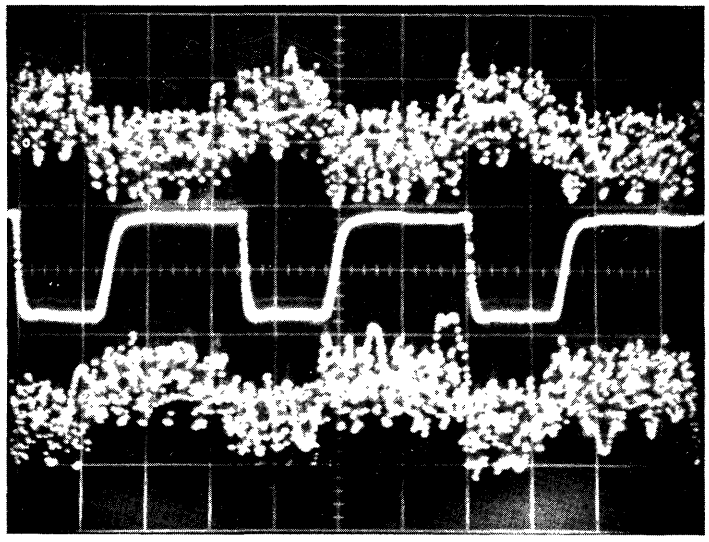


WAVEFORMS



Photograph of a 9620 switching differential data in the presence of high common mode noise.

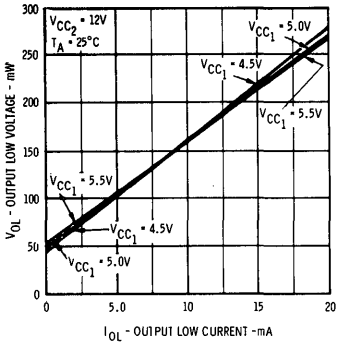




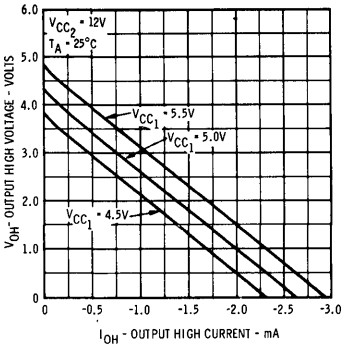
VERT = 2.0 V/div. HORIZ = 50 ns/div.

TYPICAL ELECTRICAL CHARACTERISTICS

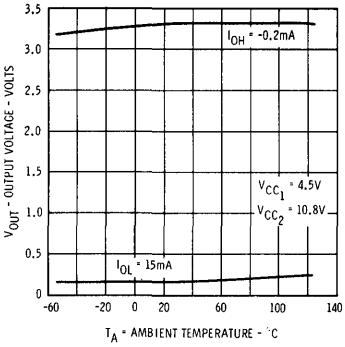
TYPICAL OUTPUT LOW VOLTAGE VERSUS OUTPUT LOW CURRENT



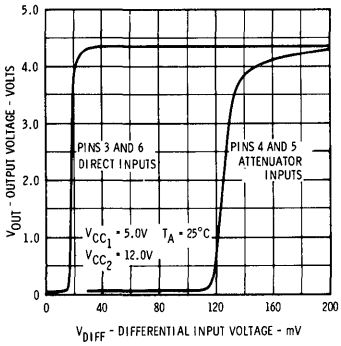
TYPICAL OUTPUT HIGH VOLTAGE VERSUS OUTPUT HIGH CURRENT



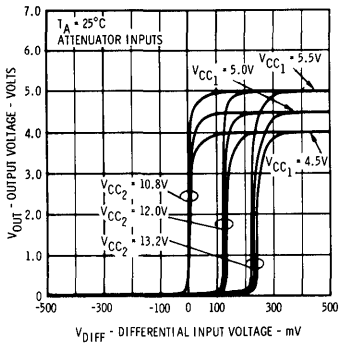
LOGIC LEVELS VERSUS AMBIENT TEMPERATURE



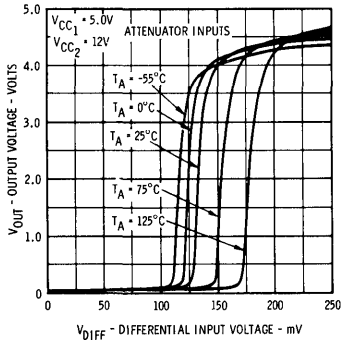
TYPICAL V_{out} VERSUS V_{DIFF} TRANSFER CHARACTERISTIC



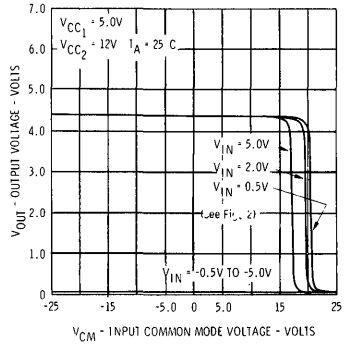
TYPICAL V_{out} VERSUS V_{DIFF} TRANSFER CHARACTERISTIC



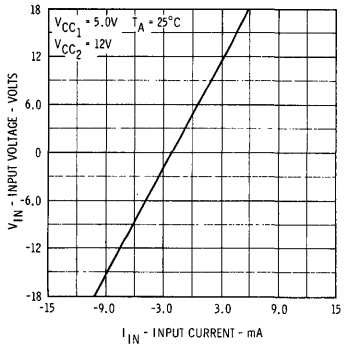
TYPICAL V_{out} VERSUS V_{DIFF} TRANSFER CHARACTERISTIC



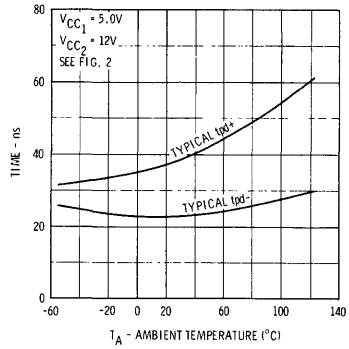
TYPICAL V_{out} VERSUS V_{CM} CHARACTERISTICS



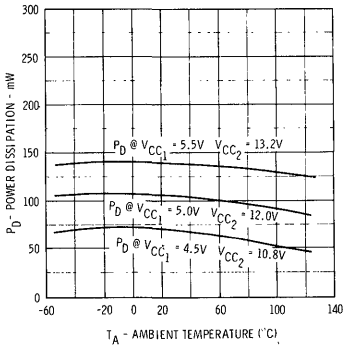
INPUT VOLTAGE VERSUS INPUT CURRENT



SWITCHING TIME VERSUS AMBIENT TEMPERATURE

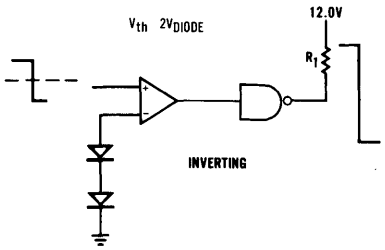


POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



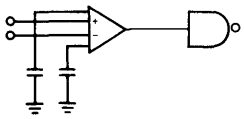
APPLICATIONS

DIGITAL COMPARATOR WITH DIODE REFERENCE AND HIGH LEVEL LOGIC OUT

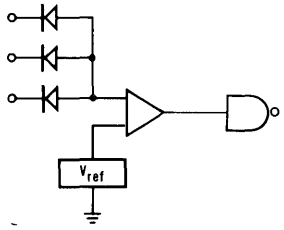


$R_1 \geq 750\ \Omega$

DIGITAL DIFFERENTIAL LINE RECEIVER WITH INPUTS ROLLED OFF

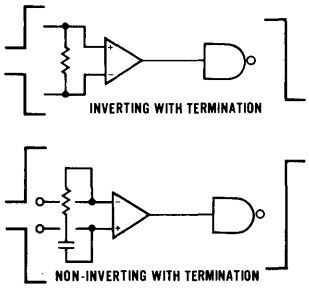


EXPANDED INTERFACE

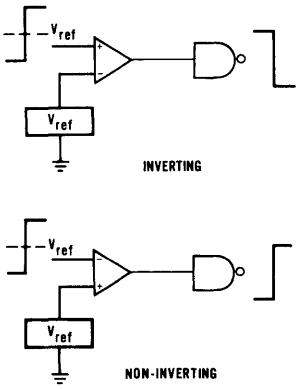


V_{ref} = Resistor, Diodes, or Supply

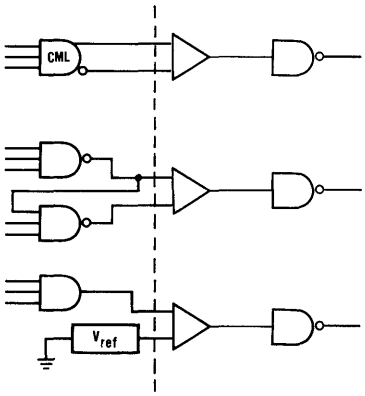
DIGITAL DIFFERENTIAL AMPLIFIER (Line Receiver)



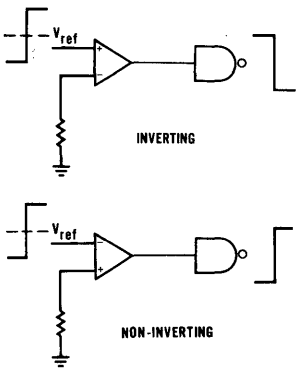
DIGITAL COMPARATOR



INTERFACING METHODS

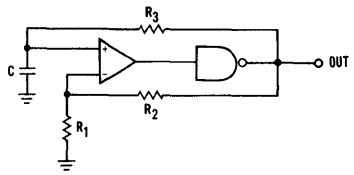


DIGITAL COMPARATOR WITH RESISTIVE DIVIDER AS REFERENCE



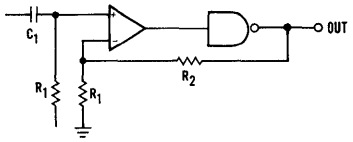
APPLICATIONS

MULTIVIBRATOR



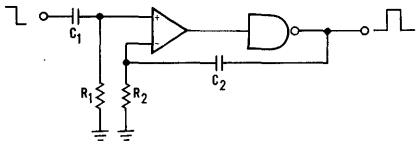
TYPICALLY
$R_1 = 1.6\ k\Omega$, $R_2 = 2.7\ k\Omega$, $T = 1.3\ R_3C$

A.C. COUPLED DIGITAL AMPLIFIER WITH HYSTERESIS



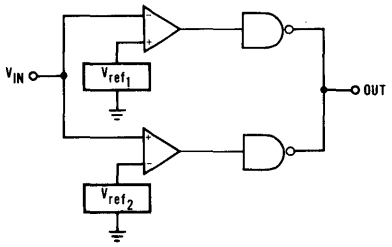
TYPICALLY
$R_1 = 1.6\ k\Omega$, $R_2 = 2.7\ k\Omega$

MONOSTABLE MULTIVIBRATOR NEGATIVE EDGE TRIGGERING



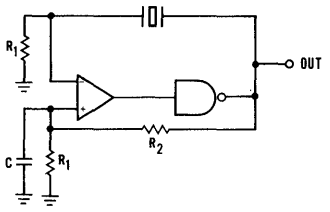
TYPICALLY
$C_1 = 0.1\ \mu F$, $R_1 = 1.2\ k\Omega$, $R_2 = 1.0\ k\Omega$
Pulse Width = 50 ns + $3.15 \times 10^3\ C_2$

DOUBLE-ENDED COMPARATOR



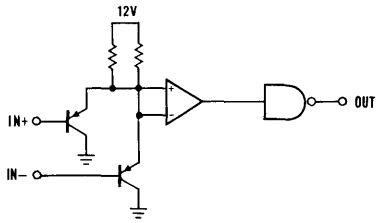
$V_{OH} = V_{Ref1} < V_{IN} < V_{Ref2}$

CRYSTAL CONTROLLED MULTIVIBRATOR



TYPICALLY
$R_1 = 1.6\ k\Omega$, $R_2 = 2.7\ k\Omega$, $C = \frac{R_2}{1000}$

HIGH INPUT IMPEDANCE LINE RECEIVER (Positive Signals Only)



μA9621

DUAL-LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA9621 was designed to drive transmission lines in either a differential or a single-ended mode. Output clamp diodes and back-matching resistors for 130 Ω twisted pair are provided. The output has the capability of driving high capacitance loads. It can typically switch >200 mA during transients.

- **TTL COMPATIBILITY**
- **TRANSMISSION LINE BACK-MATCHING**
- **OUTPUT CLAMP DIODES**
- **HIGH CAPACITANCE DRIVE**
- **HIGH OUTPUT VOLTAGE**
- **MILITARY TEMPERATURE RANGE**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

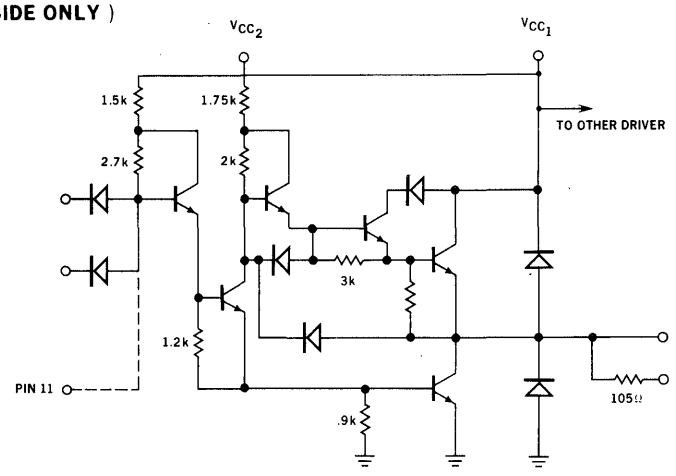
Storage Temperature	−65° C to +150° C
Temperature (Ambient) Under Bias	−55° C to +125° C
V_{CC1} Pin Potential to Ground Pin	+3.8 V to +8 V
Input Voltage	−0.5 V to +15 V
Voltage Applied to Outputs	−2 V to +V_{CC1} +1 V
V_{CC2} Pin Potential to Ground Pin	V_{CC1} to +15 V
Lead Temperature (Soldering, 60 seconds)	300° C
Internal Power Dissipation (Note)	
Ceramic DIP	670 mW
Flatpak	570 mW

NOTE

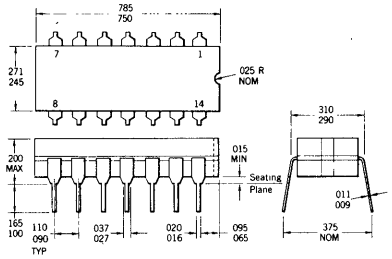
Rating applies to ambient temperatures up to 70° C. Above 70° C derate linearly at 8.3 mW/° C for the Ceramic DIP and 7.1 mW/° C for the Flatpak Package.

ORDER INFORMATION – Specify U6A9621XXX for 14-pin Dual In-Line Package or U3I9621XXX for 14-pin Flatpak where XXX is 51X for the −55° C to +125° C temperature range, or 59X for the 0° C to +75° C temperature range.

SCHEMATIC DIAGRAM
(ONE SIDE ONLY)

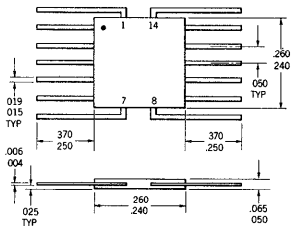


PHYSICAL DIMENSIONS
Similar* to JEDEC (TO-116) outline
14 Lead Dual-In-Line



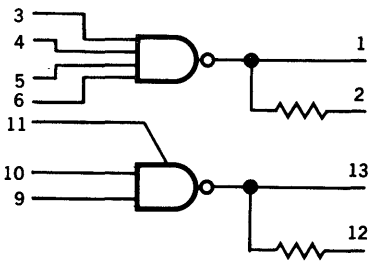
NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

FLAT PACKAGE
16 Lead BeO Cerpak



NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.26 gram

LOGIC DIAGRAM



V_{CC_1} = 14, V_{CC_2} = 8, GND = 7

ELECTRICAL CHARACTERISTICS
MILITARY TEMPERATURE RANGE −55°C to +125°C (UXX962151X)

SYMBOL	NOTES	CHARACTERISTICS	LIMITS							UNITS	CONDITIONS & COMMENTS	
			−55°C		+25°C			+125°C				
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OL}		Output Low Voltage		350		200	350		400	mV	I_{OL} = 20 mA	V_{CC1} = 4.5 V V_{CC2} = 10.8 V
V_{OH}		Output High Voltage	4.0		4.0	4.3		4.0		V	I_{OH} = −20 mA	V_{CC1} = 4.5 V V_{CC2} = 10.8 V
I_{SC}	1	Output "Short Circuit" Current			−180	−420				mA	V_{OUT} = 0 V	V_{CC1} = 4.5 V V_{CC2} = 10.8 V
I_{OL}	1	Output Low Current			150	200				mA	V_{OUT} = 5.0 V	V_{CC1} = 4.5 V V_{CC2} = 10.8 V
I_F		Input Forward Current		−1.8		−1.15	−1.8		−1.8	mA	V_F = 0 V	V_{CC1} = 5.5 V V_{CC2} = 13.2 V
I_R		Input Reverse Current		2.0		<1.0	2.0		5.0	μA	V_R = 5.5 V	V_{CC1} = 5.5 V V_{CC2} = 13.2 V
V_{OLR}	2	Resistive Output Low Voltage				380	500			V	I_{OL} = 2.8 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OHR}	2	Resistive Output High Voltage			4.0	4.2				V	I_{OH} = −2.3 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OLC}	3	Clamped Output Low Voltage				−1.0	−2.0			V	I_{OL} = −20 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OHC}	3	Clamped Output High Voltage				6.0	7.0			V	I_{OH} = 20 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
I_{CC1}		+5 V Supply Current		7.0		4.7	7.0		7.3	mA	Inputs Open	V_{CC1} = 5.5 V V_{CC2} = 13.2 V
I_{CC2}		+12 V Supply Current		9.8		6.5	9.8		9.8	mA		
t_{pd+}	4	Turn-Off Time				30	150			ns	C_L = 5000 pF	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
t_{pd-}	4	Turn-On Time				80	150			ns		
t_{pd+}		Turn-Off Time				13	25			ns	C_L = 30 pF	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
t_{pd-}		Turn-On Time				9	25			ns		
V_{IL}		Input Low Voltage		1.3		1.5	1.0		0.7	V	V_{CC1} = 5.5 V V_{CC2} = 10.8 V	
V_{IH}		Input High Voltage	2.2		2.0	1.7		1.8		V	V_{CC1} = 4.5 V V_{CC2} = 13.2 V	

NOTES:
(1) Pulse tests to insure transient current handling (test time = 3 seconds maximum — one side only).
(2) Test output resistance including 105Ω output resistor.
(3) Tests output clamp diodes.
(4) With both sides loaded at T_A = +125°C, maximum frequency = 500 kHz for Dual In-Line package (θ_{JA} = 95°C/W) or 300 kHz for Ceramic Flat Pak (θ_{JA} = 165°C/W).

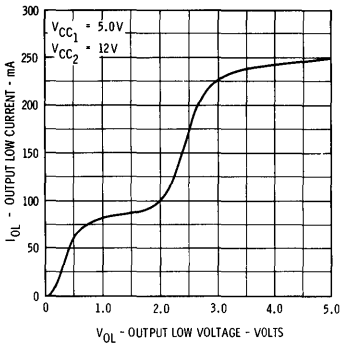
ELECTRICAL CHARACTERISTICS
INDUSTRIAL TEMPERATURE RANGE 0°C to +75°C (UXX962159X)

SYMBOL	NOTES	CHARACTERISTICS	LIMITS							UNITS	CONDITIONS & COMMENTS	
			0°C		+25°C			+75°C				
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OL}		Output Low Voltage		400		200	400		450	mV	I_{OL} = 20 mA	V_{CC1} = 4.75 V V_{CC2} = 11.4 V
V_{OH}		Output High Voltage	4.2		4.2	4.4		4.2		V	I_{OH} = −20 mA	V_{CC1} = 4.75 V V_{CC2} = 11.4 V
I_{SC}	1	Output "Short Circuit" Current			−100	−420				mA	V_{OUT} = 0 V	V_{CC1} = 4.75 V V_{CC2} = 11.4 V
I_{OL}	1	Output Low Current			75	200				mA	V_{OUT} = 5.0 V	V_{CC1} = 4.75 V V_{CC2} = 11.4 V
I_F		Input Forward Current		1.8		1.15	1.8		1.8	mA	V_F = 0 V	V_{CC1} = 5.25 V V_{CC2} = 12.6 V
I_R		Input Reverse Current		5.0		<1.0	5.0		10.0	μA	V_R = 5.5 V	V_{CC1} = 5.25 V V_{CC2} = 12.6 V
V_{OLR}	2	Resistive Output Low Voltage				380	500			V	I_{OL} = 2.8 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OHR}	2	Resistive Output High Voltage			4.0	4.2				V	I_{OH} = −2.3 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OLC}	3	Clamped Output Low Voltage				−1.0	−2.0			V	I_{OL} = −20 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OHC}	3	Clamped Output High Voltage				6.0	7.0			V	I_{OH} = 20 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
I_{CC1}		+5 V Supply Current		7.0		4.7	7.0		7.3	mA	Inputs Open	V_{CC1} = 5.25 V V_{CC2} = 12.6 V
I_{CC2}		+12 V Supply Current		9.8		6.5	9.8		9.8	mA		
t_{pd+}	4	Turn-Off Time				30	200			ns	C_L = 5000 pF	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
t_{pd-}	4	Turn-On Time				80	200			ns		
t_{pd+}		Turn-Off Time				13	40			ns	C_L = 30 pF	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
t_{pd-}		Turn-On Time				9	40			ns		
V_{IL}		Input Low Voltage		1.3		1.5	1.0		0.7	V	V_{CC1} = 5.25 V V_{CC2} = 12.6 V	
V_{IH}		Input High Voltage	2.2		2.0	1.7		1.8		V	V_{CC1} = 4.75 V V_{CC2} = 11.4 V	

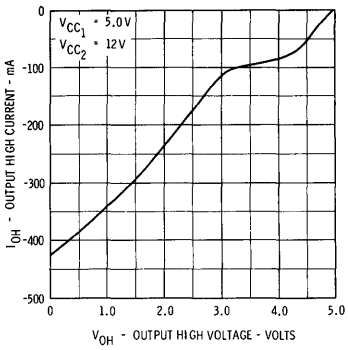
NOTES:
(1) Pulse tests to insure transient current handling (test time = 3 seconds maximum — one side only).
(2) Test output resistance including 105Ω output resistor.
(3) Tests output clamp diodes.
(4) Maximum frequency = 500 kHz with both sides loaded at T_A = +75°C for both Dual In-Line package and Ceramic Flat Pak.

TYPICAL ELECTRICAL CHARACTERISTICS

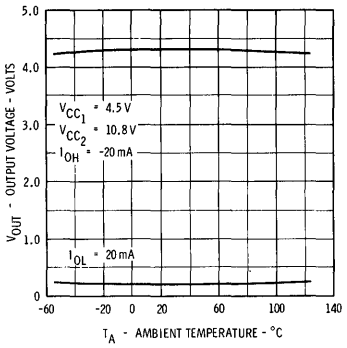
OUTPUT LOW CURRENT VERSUS OUTPUT LOW VOLTAGE



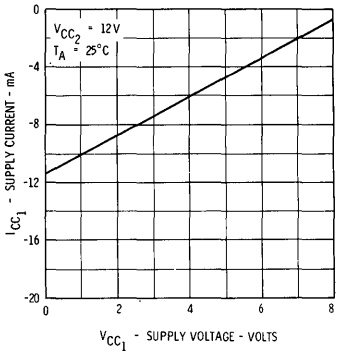
OUTPUT HIGH CURRENT VERSUS OUTPUT HIGH VOLTAGE



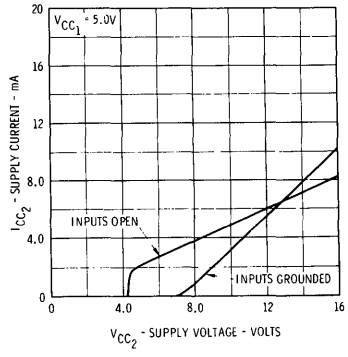
LOGIC LEVELS VERSUS AMBIENT TEMPERATURE



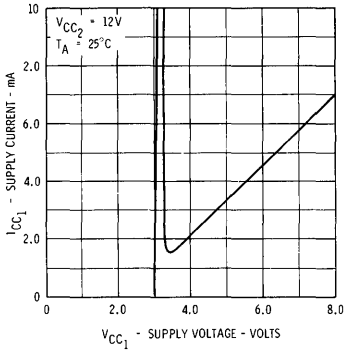
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE INPUTS GROUNDED



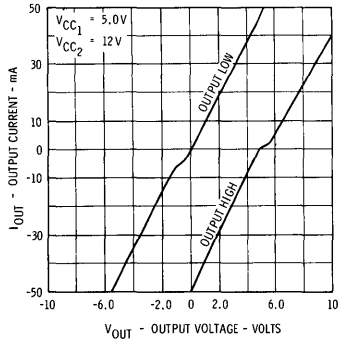
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE INPUTS OPEN



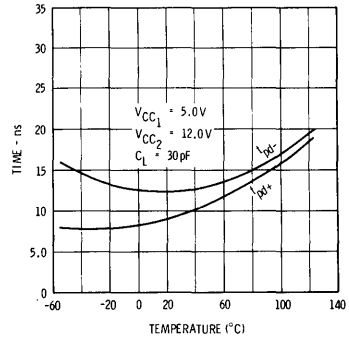
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



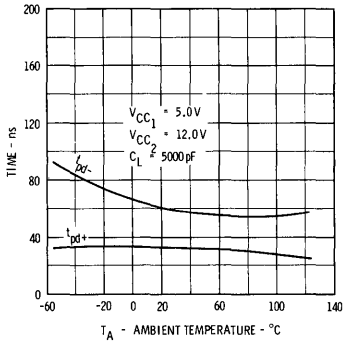
TYPICAL OUTPUT IMPEDANCE WITH BACK MATCHING RESISTORS



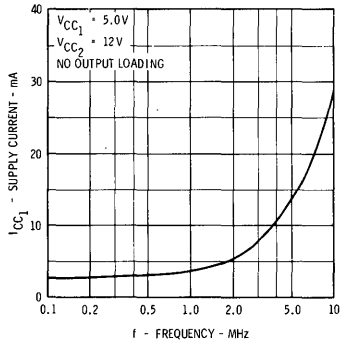
SWITCHING TIME VERSUS TEMPERATURE



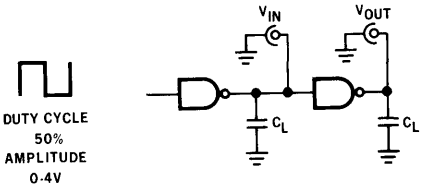
SWITCHING TIME VERSUS TEMPERATURE



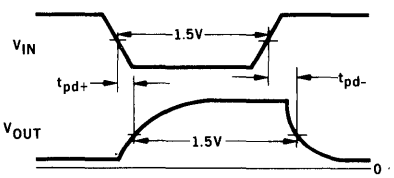
SUPPLY CURRENT VERSUS FREQUENCY



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



DESCRIPTION OF REFLECTION DIAGRAM USAGE

The reflections on any line may be found by using the following procedure:

1. Draw the driver output characteristics for both the "high state" and the "low state" on an I - V graph in the same manner as the reflection diagram.
2. Draw the receiver input characteristic on the same graph. The two points of intersection of the receiver and driver characteristics are the two DC operating points.
3. Choose to analyze either the reflections for the output going low or high. In the example chosen the negative transition is analyzed.
4. Draw a line with a slope equal to the impedance of the line to be used, ($Z_0 = 100\Omega$ in the example), from the "high state" operating point (labeled A on our graph) to the "low state" output device characteristic (B_1). B_1 equals the conditions at the driver output immediately after turn-on.
5. Reverse the slope of Z_0 and sketch it from B_1 to the receiver input characteristic (C_1). C_1 equals the conditions at the receiver when the wavefront B_1 first reaches it.
6. By continuing this procedure of reversing the slope of Z_0 at each node all the reflections (B_1, C_1, B_2, C_2, B_3, C_3 - - - B_N, C_N), where B_X is the voltage at the driver and C_X is the voltage at the receiver, can be found.

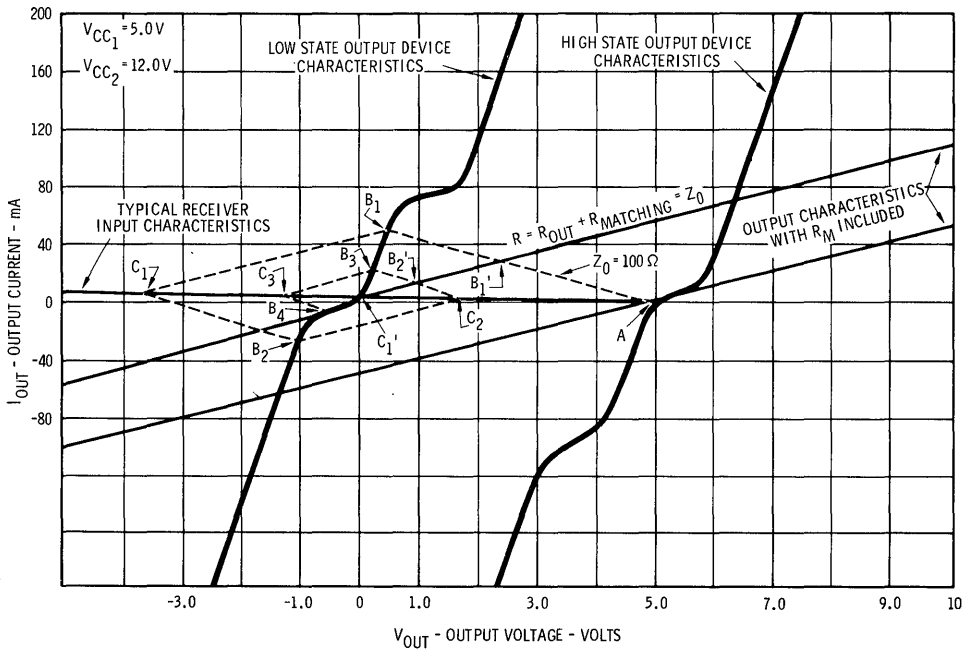
The same procedure is used to check the reflections when switching the output high.

BACK-MATCHING, also referred to as reverse termination, offers several advantages to the user. It reduces the system power by not requiring the high current for resistive termination and it reduces the DC line losses because IR drops in the line become minimum.
To back-match any line (output switching low):

1. Measure the output resistance, R_{out}, from the "low state" operating point to B_1.
2. Subtract R_{out} from Z. ($R_{out} + R_M = Z_0$). This value R_M, is the required back-matching resistance.
3. Place R_M in series with the output of driver.
4. The reflections that occur on the line with R_M inserted can be treated in the same manner as the general case. The results are B_1' and C_1' and the receiver will not see any reflections.

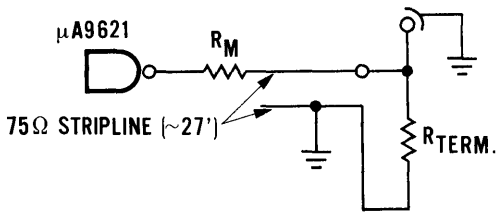
When switching the line differentially $R_M + R_{out} = Z_0/_2$. The matched output characteristics of the 9621 make it possible to back-match effectively and require analysis of switching only one state.

TYPICAL REFLECTION DIAGRAM*



* GRAPHICAL ANALYSIS
First Presented by John B. James of I.C.T. (Eng.) LTD.

REFLECTION TEST CIRCUIT

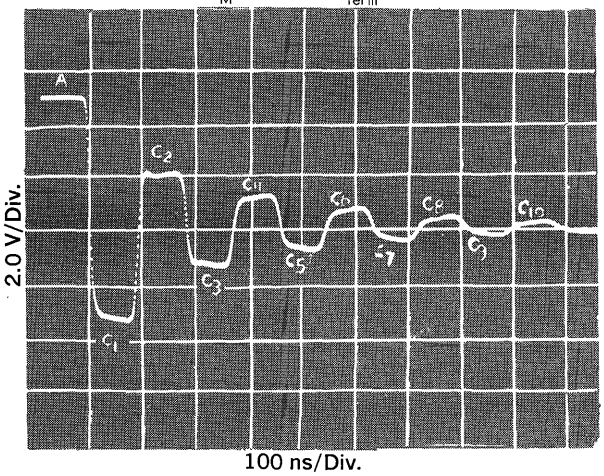


The reflections are two delay's of the line wide. R_{term} is the total impedance seen at the receiving end.

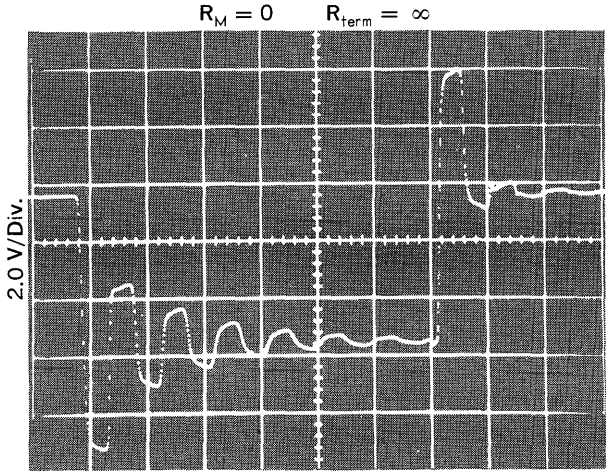
BACK MATCHING TABLE

Z_O	R_M when used single ended	R_M when used differentially
50 Ω	32 Ω	16 Ω
75 Ω	62 Ω	30 Ω
92 Ω	82 Ω	41 Ω
100 Ω	90 Ω	45 Ω
130 Ω	120 Ω	60 Ω
300 Ω	290 Ω	145 Ω
600 Ω	590 Ω	295 Ω

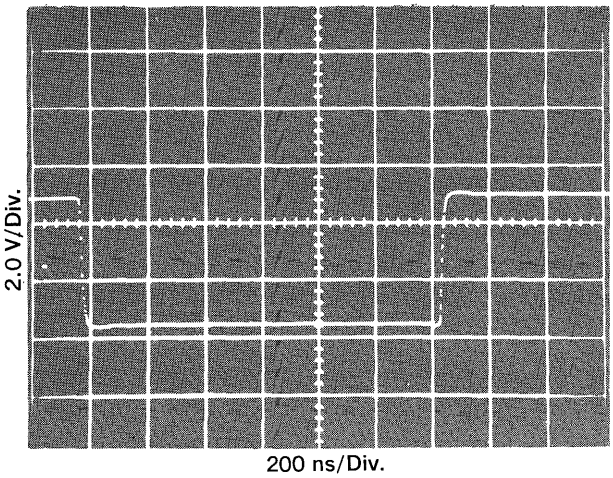
$R_M = 0$ $R_{term} = \infty$



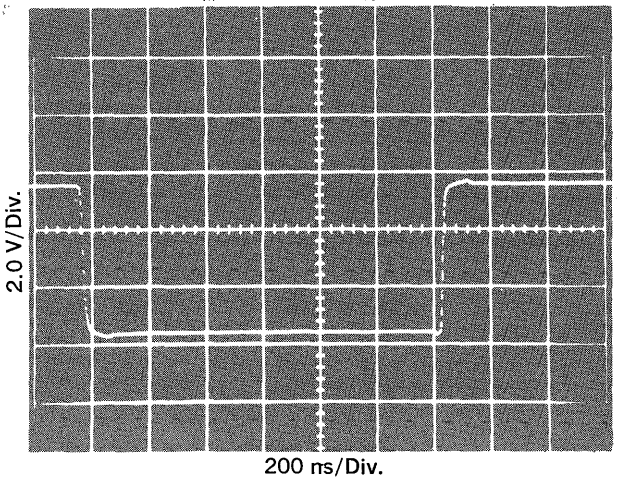
$R_M = 0$ $R_{term} = \infty$



$R_M = 0$ $R_{term} = 75\Omega$



$R_M = 62\ \Omega$ $R_{term} = \infty$



μA9622
DUAL LINE RECEIVER
FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA9622 is a dual line receiver designed to discriminate a worst case logic swing of 2 volts from a ±10 volt common mode noise signal or ground shift. A 1.5 volt threshold is built into the differential amplifier to offer a TTL compatible threshold voltage and maximum noise immunity. The offset is obtained by use of current sources and matched resistors and varies only ±5% (75 mV) over the military and industrial temperature ranges.

The μA9622 allows the choice of output states with the inputs open without affecting circuit performance by use of S3. A 130 Ω terminating resistor is provided at the input of each line receiver. An enable is also provided for each line receiver. The output is TTL compatible. The output high level can be increased to +12 V by tieing it to a positive supply through a resistor. The outputs can be wire-OR'ed.

- **TTL COMPATIBLE THRESHOLD VOLTAGE**
- **INPUT TERMINATING RESISTORS**
- **CHOICE OF OUTPUT STATE WITH INPUTS OPEN**
- **TTL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE**
- **WIRE-OR CAPABILITY**
- **ENABLE INPUTS**
- **FULL MILITARY TEMPERATURE RANGE**
- **LOGIC COMPATIBLE SUPPLY VOLTAGES**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

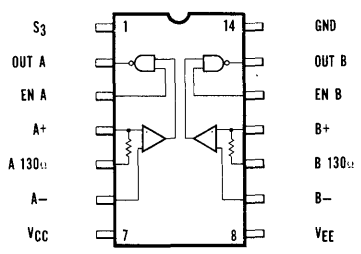
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Internal Power Dissipation (Note 1)	
Ceramic DIP	670 mW
Flatpak	570 mW
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Input Voltage	±15 V
Voltage Applied to Outputs for High Output State	−0.5 V to +13.2 V
V_{EE} Pin Potential to Ground Pin	−0.5 V to −12 V
Enable Pin Potential to Ground Pin	−0.5 V to +15 V
Lead Temperature (Soldering, 60 seconds)	300°C

NOTE

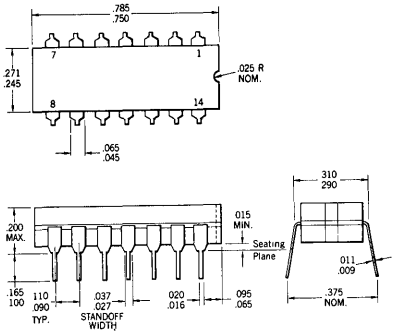
1. Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3 mW/°C for the Ceramic DIP and 7.1 mW/°C for the Flatpak Package.

ORDER INFORMATION – Specify U6A9622XXX for 14-pin Dual In-Line Package, U3I9622XXX for 14-pin Flatpak where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

LOGIC DIAGRAM

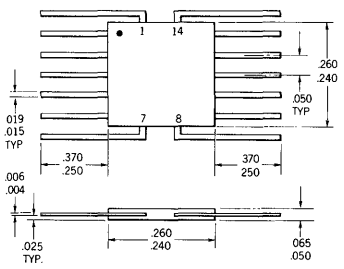


TYPICAL DUAL IN-LINE PACKAGE
In Accordance With
JEDEC (TO-116) Outline



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.
Leads are tin-plated kovar
Package weight is 2.0 grams

FLAT PACKAGE
TOP VIEW



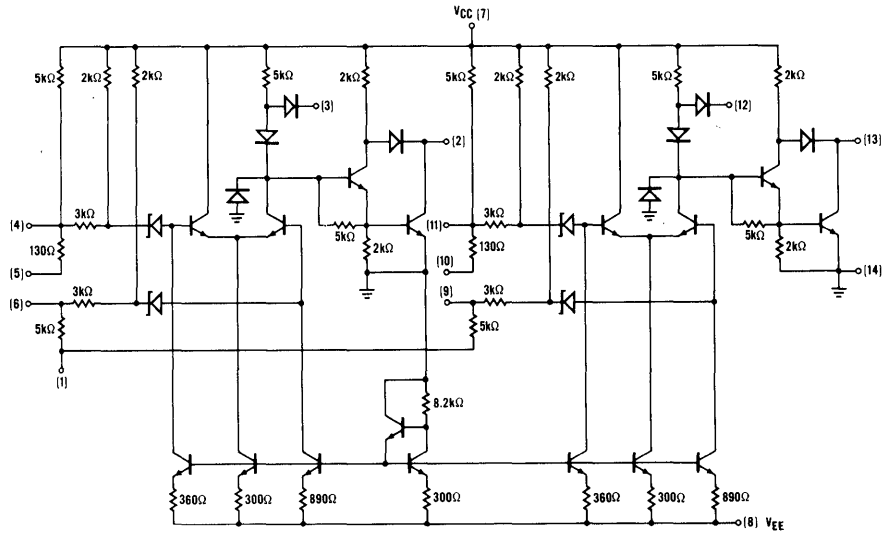
NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.26 gram

ELECTRICAL CHARACTERISTICS (Temperature Range −55°C to +125°C, V_{CC} = 5.0 V ± 10%)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OL}	Output Low Voltage		0.40		0.17	0.40		0.40	V	V_{CC} = 4.5 V, V_{EE} = −11 V, *V_{DIFF} = 2.0 V, I_{OL} = 12.4 mA
V_{OH}	Output High Voltage	2.8		3.0	3.3		2.9		V	V_{CC} = 4.5 V, V_{EE} = −9.0 V, *V_{DIFF} = 1.0 V, I_{OH} = −0.2 mA
I_{CEX}	Output Leakage Current		50			100		200	μA	V_{CC} = 4.5 V, V_{EE} = −11 V, *V_{DIFF} = 1.0 V, V_{CEX} = 12 V
I_{SC}	Output Shorted Current	−1.3	−3.1	−1.4	−2.15	−3.1	−1.3	−3.1	mA	V_{CC} = 5.0 V, V_{EE} = −10 V, *V_{DIFF} = 1.0 V, V_{SC} = 0 V
$I_{R(ENABLE)}$	Enable Input Leakage Current					2.0		5.0	μA	V_{CC} = 4.5 V, V_{EE} = −11 V, S_3 = 4.5 V, V_R = 4.0 V
$I_{F(ENABLE)}$	Enable Input Forward Current		−1.5		−0.96	−1.5		−1.5	mA	V_{CC} = 5.5 V, V_{EE} = −9.0 V, S_3 = 0 V, V_F = 0 V
$I_{F(+Input)}$	+ Input Forward Current		−2.3		−1.67	−2.1		−2.0	mA	V_{CC} = 5.0 V, V_{EE} = −10 V, − Input = Gnd, V_F = 0 V
$I_{F(-Input)}$	− Input Forward Current		−2.6		−1.87	−2.4		−2.3	mA	V_{CC}, S_3 = 5.0 V, V_{EE} = −10 V, + Input = Gnd, V_F = 0 V
$V_{IL(ENABLE)}$	Input Low Voltage		1.3		1.4	1.0		0.7	V	V_{CC} = 5.0 V ±10%, V_{EE} = −10 V ±10%
V_{th}	Differential Input Threshold Voltage	1.0	2.0	1.0	1.5	2.0	1.0	2.0	V	V_{CC} = 5.0 V ±10%, V_{EE} = −10 V ±10%
V_{CM}	Common Mode Voltage			−10	±12	+10			V	V_{CC} = 5.0 V, V_{EE} = −10 V, *V_{DIFF} = 1.0 V or 2.0 V
$R_{130\Omega}$	Terminating Resistance			100	130	175			Ω	
I_{CC}	5 V Supply Current				13.7	22.9			mA	V_{CC} = 5.5 V, V_{EE} = −11 V, S_3, + Inputs = 5.5 V, − Inputs = 0 V
I_{EE}	−10 V Supply Current				−6.5	−11.1			mA	V_{CC} = 5.5 V, V_{EE} = −11 V, S_3, + Inputs = 5.5 V, − Inputs = 0 V
t_{pd+}	Turn-off Time				38	50			ns	V_{CC} = 5.0 V, V_{EE} = −10 V, V_{IN} 0→3 V, R_L = 3.9 kΩ, C_L = 30 pF
t_{pd-}	Turn-on Time				35	50			ns	V_{CC} = 5.0 V, V_{EE} = −10 V, V_{IN} 0→3.0 V, R_L = 0.39 kΩ, C_L = 30 pF

*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.

SCHEMATIC DIAGRAM

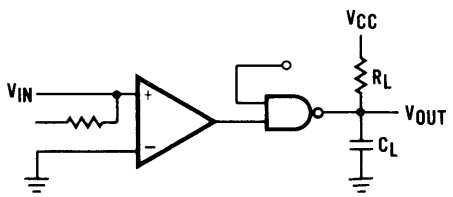


ELECTRICAL CHARACTERISTICS (Temperature Range 0°C to +75°C, V_{CC} = 5.0 V ± 5%)

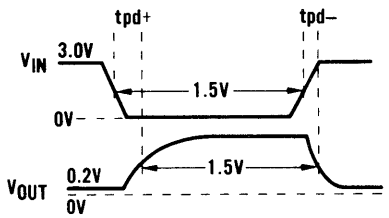
SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OL}	Output Low Voltage		0.45		0.17	0.45		0.45	V	V_{CC} = 4.75 V *V_{DIFF} = 2.0 V	V_{EE} = −10.5 V I_{OL} = 14.1 mA
V_{OH}	Output High Voltage	2.9		3.0	3.3		2.9		V	V_{CC} = 4.75 V *V_{DIFF} = 1.0 V	V_{EE} = −9.5 V I_{OH} = −0.2 mA
I_{CEX}	Output Leakage Current		80			100		200	μA	V_{CC} = 4.75 V *V_{DIFF} = 1.0 V	V_{EE} = −10.5 V V_{CEX} = 5.25 V
I_{SC}	Output Shorted Current	−1.3	−3.1	−1.4	−2.15	−3.2	−1.3	−3.1	mA	V_{CC} = 5.0 V *V_{DIFF} = 1.0 V	V_{EE} = −10 V V_{SC} = 0 V
$I_{R(ENABLE)}$	Enable Input Leakage Current					5		10	μA	V_{CC} = 4.75 V S_3 = 4.75 V	V_{EE} = −10.5 V V_R = 4.0 V
$I_{F(ENABLE)}$	Enable Input Forward Current		−1.5		−.96	−1.5		−1.5	mA	V_{CC} = 5.25 V S_3 = 0 V	V_{EE} = −9.5 V V_F = 0 V
$I_{F(+Input)}$	+ Input Forward Current		−2.6		−1.67	−2.4		−2.3	mA	V_{CC} = 5.0 V − Input = Gnd	V_{EE} = −10 V V_F = 0 V
$I_{F(-Input)}$	− Input Forward Current		−2.9		−1.87	−2.7		−2.6	mA	V_{CC}, S_3 = 5.0 V + Input = Gnd	V_{EE} = −10 V V_F = 0 V
$V_{IL(ENABLE)}$	Input Low Voltage		1.2		1.4	1.0		0.85	V	V_{CC} = 5.0 V ±5% V_{EE} = −10 V ±5%	
V_{th}	Differential Input Threshold Voltage	1.0	2.0	1.0	1.5	2.0	1.0	2.0	V	V_{CC} = 5.0 V ±5% V_{EE} = −10 V ±5%	
V_{CM}	Common Mode Voltage			−7.5	±12	+7.5			V	V_{CC} = 5.0 V *V_{DIFF} = 1.0 V or 2.0 V	V_{EE} = −10 V
$R_{I30}\Omega$	Terminating Resistance			91	130	185			Ω		
I_{CC}	5 V Supply Current				13.7	22.9			mA	V_{CC} = 5.25 V S_3, +Inputs = 5.25 V, −Inputs = 0 V	V_{EE} = −10.5 V
I_{EE}	−10 V Supply Current				−6.5	−11.1			mA	V_{CC} = 5.25 V S_3, +Inputs = 5.25 V, −Inputs = 0 V	V_{EE} = −10.5 V
t_{pd+}	Turn-off Time				38	100			ns	V_{CC} = 5.0 V V_{IN} 0→3.0 V, R_L = 3.9 kΩ, C_L = 30 pF	V_{EE} = −10 V
t_{pd-}	Turn-on Time				35	100			ns	V_{CC} = 5.0 V V_{IN} 0→3.0 V, R_L = 0.39 kΩ, C_L = 30 pF	V_{EE} = −10 V

*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.

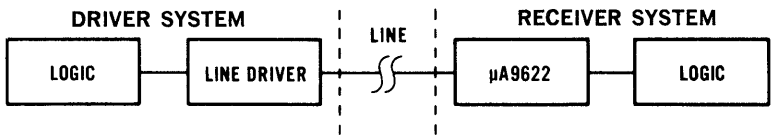
SWITCHING TIME TEST CIRCUIT



WAVEFORMS

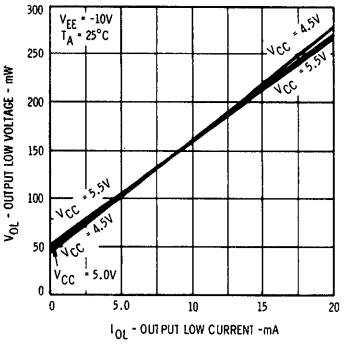


STANDARD USAGE

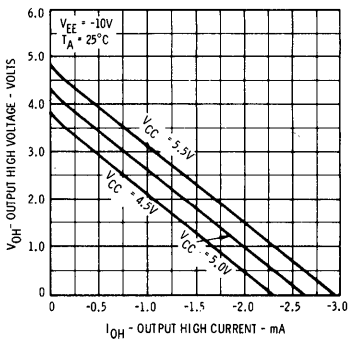


TYPICAL ELECTRICAL CHARACTERISTICS

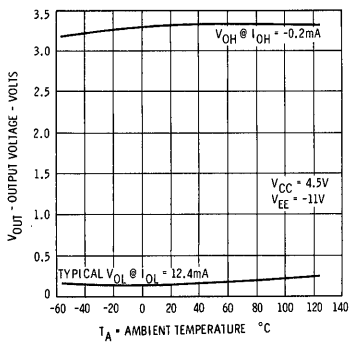
OUTPUT LOW VOLTAGE VERSUS OUTPUT LOW CURRENT



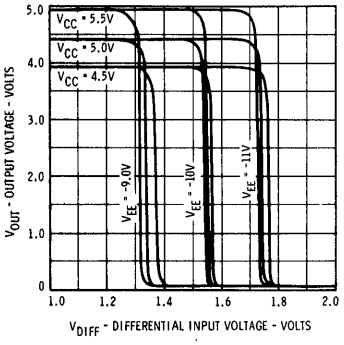
OUTPUT HIGH VOLTAGE VERSUS OUTPUT HIGH CURRENT



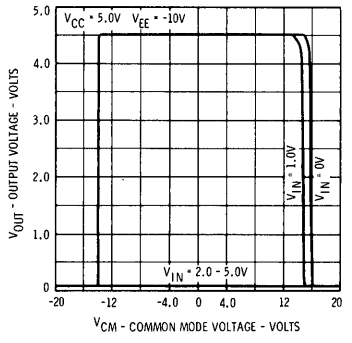
LOGIC LEVELS VERSUS AMBIENT TEMPERATURE



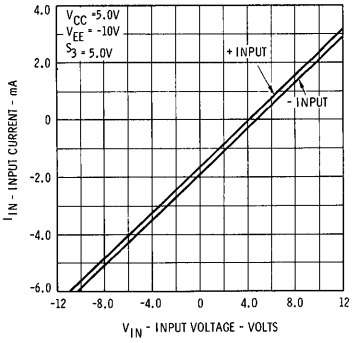
V_{out} - V_{DIFF} TRANSFER CHARACTERISTICS



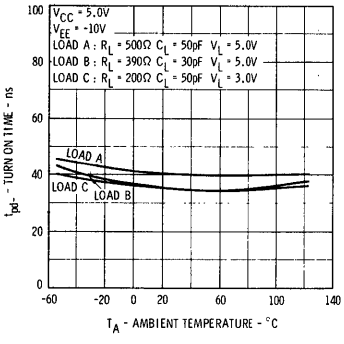
OUTPUT VOLTAGE VERSUS COMMON MODE VOLTAGE



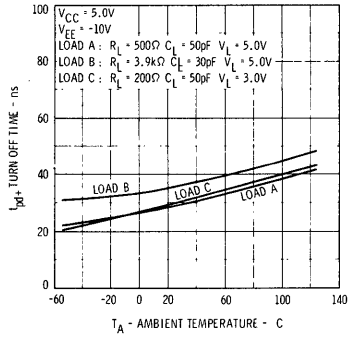
INPUT CURRENT VERSUS INPUT VOLTAGE



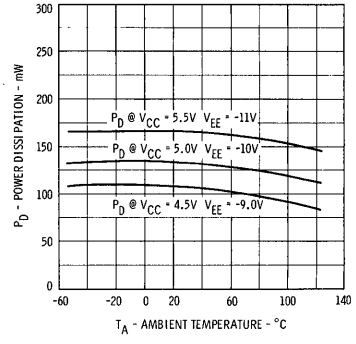
TURN ON TIME VERSUS AMBIENT TEMPERATURE



TURN OFF TIME VERSUS AMBIENT TEMPERATURE



POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



μA9624 • μA9625

DUAL TTL, MOS INTERFACE ELEMENTS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA9624 is a dual two-input TTL compatible interface gate specifically designed to drive MOS. The output swing is adjustable and will allow it to be used as a data driver, clock driver or discrete MOS driver. It has an active output for driving medium capacitive loads.

The μA9625 is a dual MOS to TTL level converter. It is designed to convert standard negatige MOS logic levels to TTL levels. The μA9625 features a high input impedance which allows preservation of the driving MOS logic level.

Both the μA9624 and μA9625 are available in the 14-pin Ceramic Dual In-Line Package and the 1/4 x 1/4 Flatpak.

NOTE: The TTL and MOS devices manufactured by Fairchild Semiconductor are considered as positive TRUE logic (the more positive voltage level is assigned the binary state of "1" or TRUE). Following MIL-STD-806B logic symbol specifications, the μA9624 is represented as a NAND gate and the μA9625 as a non-inverting buffer. This convention (of assuming MOS as a positive TRUE logic) has not been uniformly accepted by the industry; therefore, it is necessary to note that with negative TRUE MOS logic (the more negative voltage level is assigned the binary state "1" or TRUE), the μA9624 acts as an AND gate and the μA9625 as an inverter.

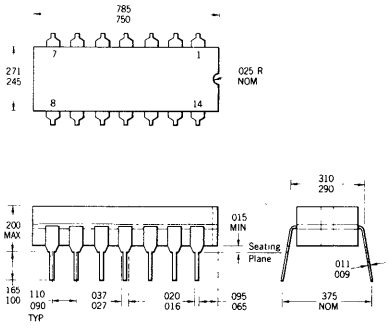
- **TTL COMPATIBLE INPUTS/OUTPUT**
- **MOS COMPATIBLE OUTPUT/INPUTS**
- **LOW POWER**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65° C to +150° C
Temperature (Ambient) Under Bias	−55° C to +125° C
V_{CC} Pin Potential to Ground Pin	V_{DD} to +10 V
Voltage Applied to Outputs for High Output State (μA9624)	V_{DD} to +V_{CC} value
Voltage Applied to Outputs for High Output State (μA9625)	−0.5 V to V_{CC} value
Input Voltage (D.C.) (μA9624)	−0.5 V to +5.5 V
Input Voltage (D.C.) (μA9625)	V_{CC} to V_{DD}
V_{DD} Pin Potential to Ground Pin	−30 V to +0.5 V
V_{DD} Pin Potential to Tap Pin (μA9624)	−30 V to +0.5 V
V_{TAP}	V_{CC} +0.5 V
Internal Power Dissipation (Note 3)	
Ceramic DIP	670 mW
Flatpak	570 mW
Lead Temperature (Soldering, 60 seconds)	300° C

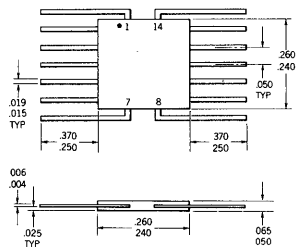
ORDER INFORMATION – Specify U6A9624XXX and U6A9625XXX for 14-pin TO-116 Dual In-Line Package or U3I9624XXX and U3I9625XXX for 14-pin Flatpak where XXX is 51X for the −55° C to +125° C temperature range, or 59X for the 0° C to +75° C temperature range.

TYPICAL DUAL IN-LINE PACKAGE
In Accordance With
JEDEC (TO-116) Outline



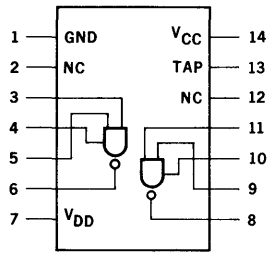
NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

FLATPAK
in accordance with JEDEC (TO-86) outline
14 Lead CERPAK

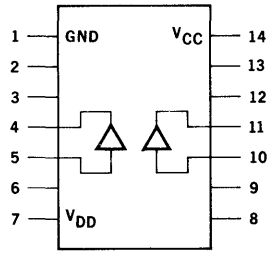


NOTES:
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.26 gram

μA9624



μA9625



Notes on following page.

TABLE I —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS
		−55°C		+25°C			+125°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.		
V_{OH1}	Output High Voltage	−1.0		−1.0	−0.5		−1.0	Volts	$V_{CC} = 4.5\ V$, $V_{DD} = -28\ V$, $V_{TAP} = 0\ V$ $I_{OH} = -10\ \mu A$
V_{OH2}	Output High Voltage	+3.5		+3.5	+4.0		+3.5		$V_{CC} = 5.5\ V$, $V_{DD} = -20\ V$, $V_{TAP} = 5.5\ V$ Inputs at threshold voltages (V_{IL}) $I_{OH} = -10\ \mu A$
V_{OL}	Output Low Voltage			See Note 1				Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 10\ mA$, $V_{DD} = -15$ to $-28\ V$ @ V_{IH}, $0 \le V_{TAP} \le V_{CC}$ (Note 2)
V_{IH}	Input High Voltage	2.1		1.9			1.7	Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1	0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.40			−1.25	−1.13	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$ $V_{DD} = -11$ to $-28\ V$
I_R	Input Leakage Current		2.0			2.0	5.0	μA	$V_{CC} = 5.5\ V$, $V_R = 4.0\ V$ $V_{DD} = -11$ to $-28\ V$
I_{CEX}	Output Leakage Current					50		μA	$V_{CC} = 5.5\ V$, $V_{TAP} = 0\ V$ $V_{DD} = -28\ V$, $V_{OUT} = 0\ V$
I_{SC}	Output Short Circuit Current	−12	−31	−14		−32	−11 −28	mA	$V_{CC} = 4.5\ V$, $V_{TAP} = 0\ V$, $V_{IN} = 0\ V$ $V_{DD} = -11\ V$, $V_{OUT} = -11\ V$
I_{VCC}	V_{CC} Supply Current					6.1		mA	$V_{CC} = 5.5V$, $V_{DD} = -15\ V$, $V_{TAP} = 0\ V$ Inputs Open
I_{MAX}	Max. Current					10		mA	$V_{CC} = 10\ V$, $V_{DD} = -30\ V$, Inputs Open $V_{TAP} = 0\ V$
t_{pd+}	Switching Speed				190	250		ns	$V_{CC} = 5.0\ V$, See Figure 2
t_{pd-}	Switching Speed				50	100		ns	$V_{DD} = -13\ V$, $V_{TAP} = 0\ V$

NOTES

1. Max = V_{DD} +1.0 V over Temperature Range. Typ = V_{DD} +0.2 V over Temperature Range.
2. At no time shall the voltage from V_{DD} to V_{TAP} exceed 30 volts. See Absolute Maximum Ratings on Page 1.
3. Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3 mW/°C for the Ceramic DIP and 7.1 mW/°C for the Flatpak package.

μA9624 SCHEMATIC DIAGRAM

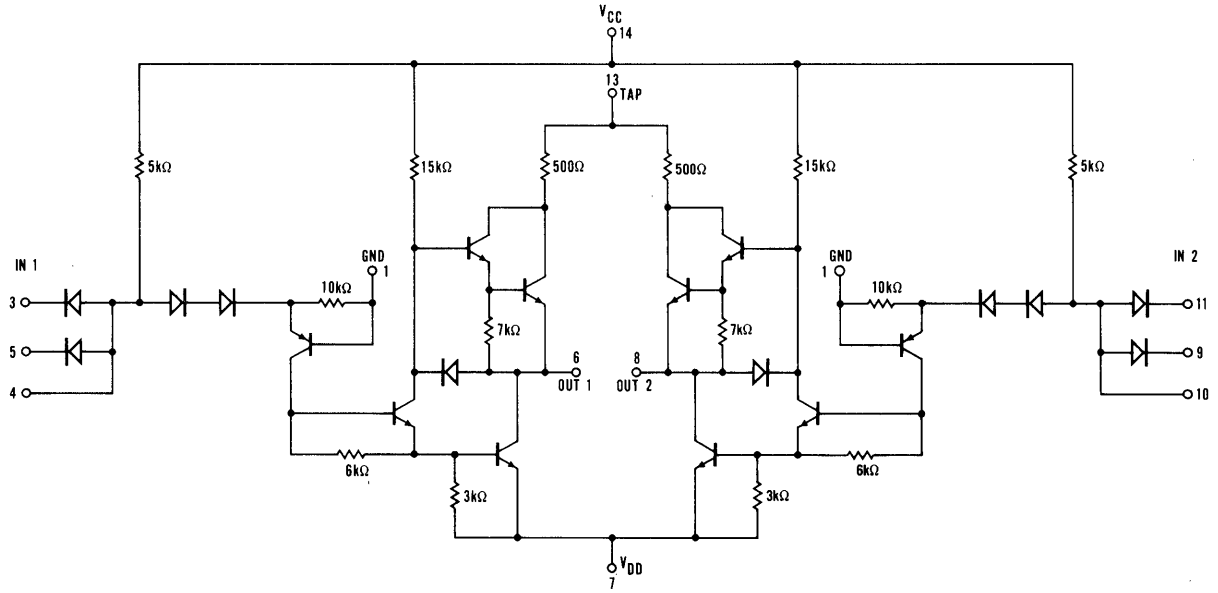


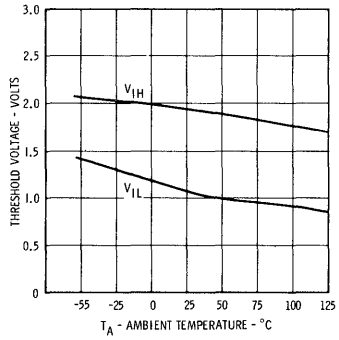
Fig. 1

TABLE II —
ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%)

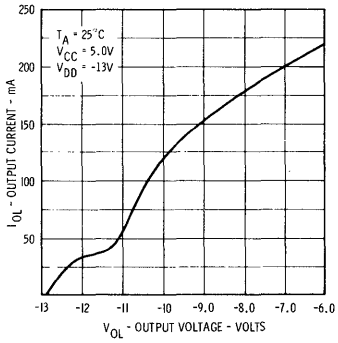
SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS
V_{OH1}	Output High Voltage	−1.0		−1.0	−0.5		−1.0		Volts	V_{CC} = 4.75 V, V_{DD} = −28 V, V_{TAP} = 0 V I_{OH} = −10 μA
V_{OH2}	Output High Voltage	+3.25		+3.25	+3.75		+3.25		Volts	V_{CC} = 5.25 V, V_{DD} = −20 V, V_{TAP} = 5.25 V I_{OH} = −10 μA Inputs at threshold voltages (V_{IL} or V_{IH})
V_{OL}	Output Low Voltage				See Note 1				Volts	V_{CC} = 4.5 V, I_{OL} = 10 mA, V_{DD} = −11 to −28 V @ 0 ≤ V_{TAP} ≤ V_{CC} (Note 2)
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.32			−1.25		−1.20	mA	V_{CC} = 5.25 V, V_F = 0.45 V
I_R	Input Leakage Current		5.0			5.0		10	μA	V_{CC} = 5.25 V, V_R = 4.5 V
I_{CEX}	Output Leakage Current					100			μA	V_{CC} = 5.25 V, V_{TAP} = 0 V V_{DD} = −28 V, V_{OUT} = 0 V
I_{SC}	Output Short Circuit Current	−12	−31	−14		−32	−12	−31	mA	V_{CC} = 4.75 V, V_{TAP} = 0 V, V_{IN} = 0 V V_{DD} = −11 V, V_{OUT} = −11 V
I_{VCC}	V_{CC} Supply Current					6.1			mA	V_{CC} = 5.25 V, V_{DD} = −15 V, V_{TAP} = 0 V Input Open
I_{MAX}	Max. Current					10			mA	V_{CC} = 10 V, V_{DD} = −30 V, V_{TAP} = 0 V Input Open
t_{pd+}	Switching Speed				190	250			ns	V_{CC} = 5.0 V, See Figure 2
t_{pd-}	Switching Speed				50	100			ns	V_{DD} = −13 V, V_{TAP} = 0 V

TYPICAL ELECTRICAL CHARACTERISTICS • μA9624

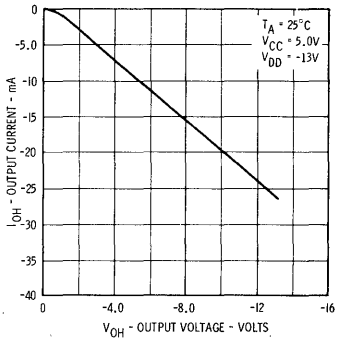
THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



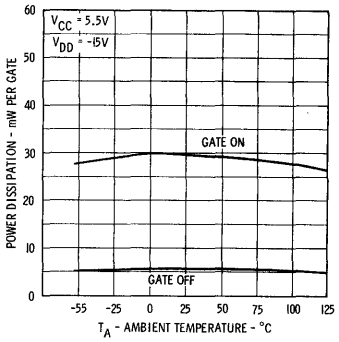
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)



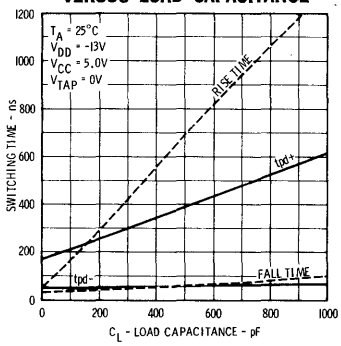
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (HIGH STATE)



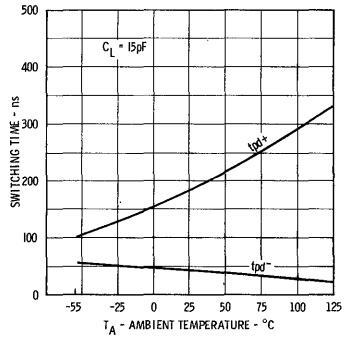
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



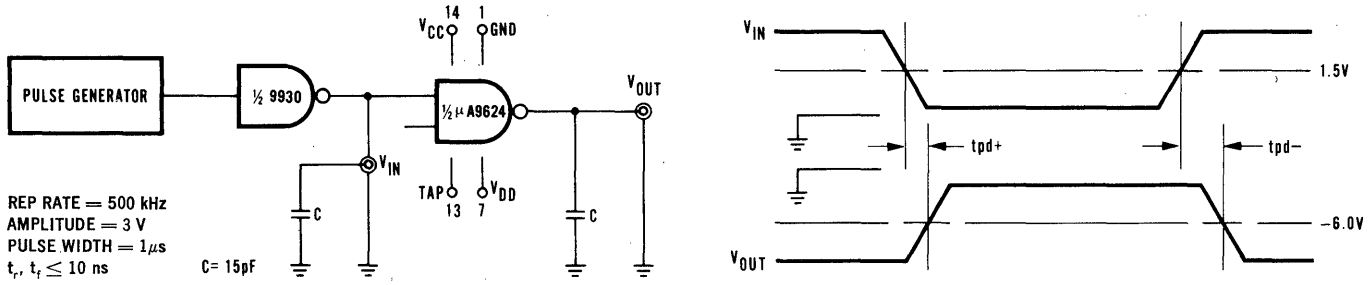
SWITCHING TIME VERSUS LOAD CAPACITANCE



SWITCHING TIME VERSUS AMBIENT TEMPERATURE



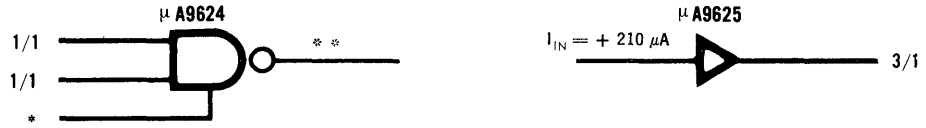
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
μA9624



TESTS	CONDITIONS			
	T_A (°C)	V_{CC} (Volts)	V_{DD} (Volts)	Tap Voltage
t_{pd+}, t_{pd-}	25	5.0	−13	0

Fig. 2

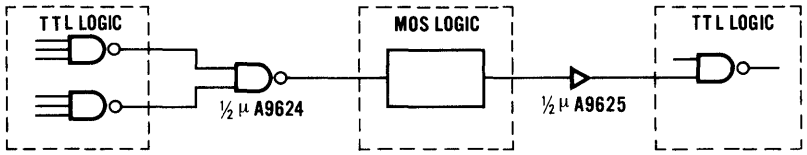
LOADING RULES:



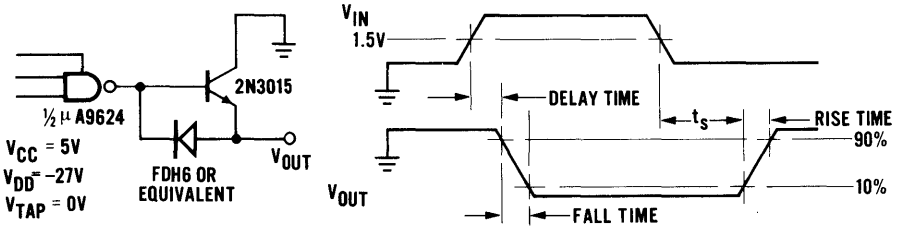
*The extender pin allows the number of inputs to be extended by adding diodes or the DTμL 933 extender.

**Fan out into MOS is limited only by MOS leakage currents.

APPLICATION:



CLOCK DRIVING (using a high capacitance drive scheme)



TYPICAL SWITCHING TIMES VERSUS LOAD CAPACITANCE

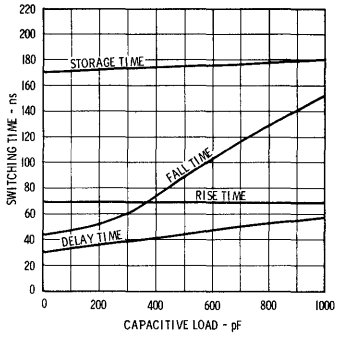


TABLE III —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS
		−55°C		+25°C			+125°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.		
V_{OH}	Output High Voltage	2.5		2.6			2.5	Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -60\ \mu A$ $V_{DD} = -11\ V$ Inputs at threshold voltages (V_{IH})
V_{OL}	Output Low Voltage		0.5			0.5	0.5	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 1.5\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 1.2\ mA$ $V_{DD} = -11\ V$ Inputs at threshold voltages (V_{IL})
V_{IH}	Input High Voltage	−3.0				−3.0	−3.0	Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage	−9.0		−9.0			−9.0	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		210			210	210	μA	$V_{CC} = 5.0\ V$, $V_F = -3.0\ V$, $V_{DD} = -13\ V$
I_{CEX}	Output Leakage Current					50		μA	$V_{CC} = V_{CEX} = 4.5\ V$, $V_{DD} = -13\ V$
I_{VCCL}	Supply Current					4.8		mA	$V_{CC} = 5.5\ V$, $V_{DD} = -15\ V$, $V_{IN} = -10\ V$
I_{VCCH}	Supply Current					2.1			$V_{CC} = 5.5\ V$, $V_{DD} = -15\ V$, $V_{IN} = 0\ V$
I_{VDD}	V_{DD} Supply Current					−9.0		mA	$V_{CC} = 5.5\ V$, $V_{DD} = -15\ V$ Input open or gnd
I_{MAX}	Max. V_{DD} Supply Current					−25		mA	$V_{CC} = 8.0\ V$, $V_{DD} = -20\ V$, $V_{IN} = 0\ V$
t_{pd+}	Switching Speed				55	100		ns	$V_{CC} = 5.0\ V$, $V_{DD} = -13\ V$
t_{pd-}	Switching Speed				90	150		ns	See Figure 4

μA9625 SCHEMATIC DIAGRAM

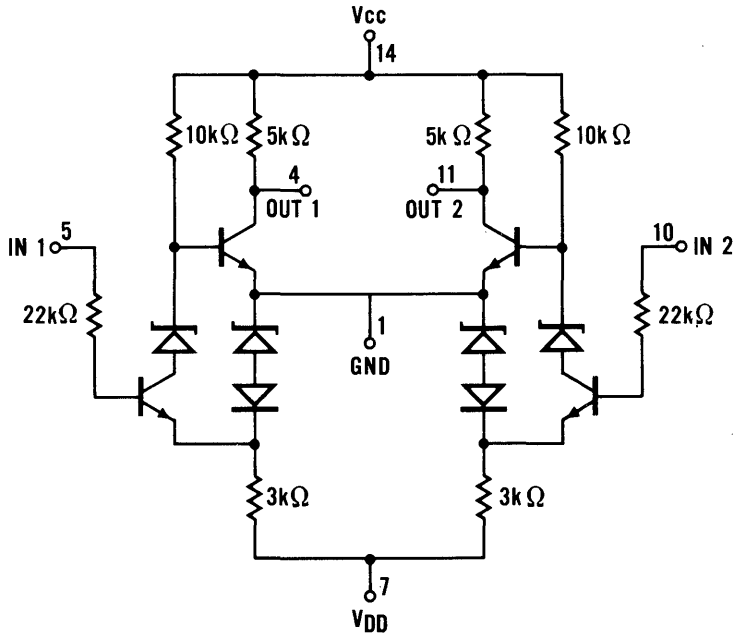


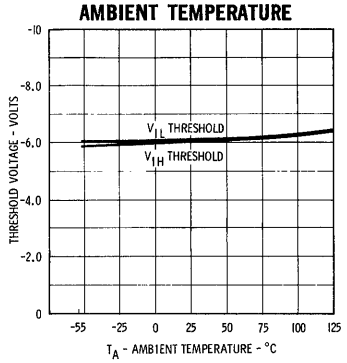
Fig. 3

TABLE IV —
ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%)

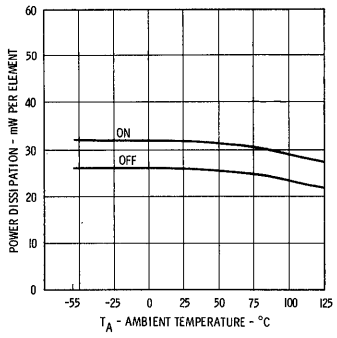
SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	MAX.	+25°C MIN.	TYP.	MAX.	+75°C MIN.	MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.5		2.6			2.5		Volts	V_{CC} = 4.75 V, I_{OH} = −60 μA V_{DD} = −11 V Inputs at threshold voltages (V_{IH})
V_{OL}	Output Low Voltage		0.5			0.5		0.5	Volts	V_{CC} = 5.25 V, I_{OL} = 1.52 mA V_{CC} = 4.75 V, I_{OL} = 1.33 mA Inputs at threshold voltages (V_{IL})
V_{IH}	Input High Voltage	−3.0				−3.0		−3.0	Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage	−9.0		−9.0			−9.0		Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		210			210		210	μA	V_{CC} = 5.0 V, V_F = −3.0 V, V_{DD} = −13 V
I_{CEX}	Output Leakage Current					100			μA	V_{CC} = V_{CEX} = 4.75 V, V_{DD} = −13 V
I_{VCCL}	Supply Current					4.8			mA	V_{CC} = 5.25 V, V_{DD} = −15 V, V_{IN} = −10 V
I_{VCCH}	Supply Current					2.1			mA	V_{CC} = 5.25 V, V_{DD} = −15 V, V_{IN} = 0 V
I_{VDD}	V_{DD} Supply Current					−9.0			mA	V_{CC} = 5.5 V, V_{DD} = −15 V Input open or gnd
I_{MAX}	Max. V_{DD} Supply Current					−25			mA	V_{CC} = 8.0 V, V_{DD} = −20 V, V_{IN} = 0 V
t_{pd+}	Switching Speed				55	100			ns	V_{CC} = 5.0 V, V_{DD} = −13 V See Figure 4
t_{pd-}	Switching Speed				90	150			ns	

TYPICAL ELECTRICAL CHARACTERISTICS • μA9625

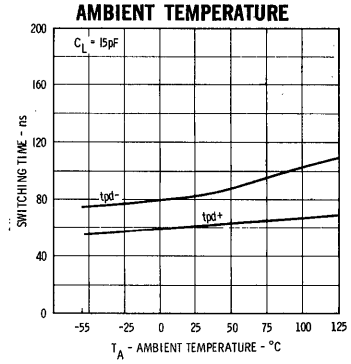
THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



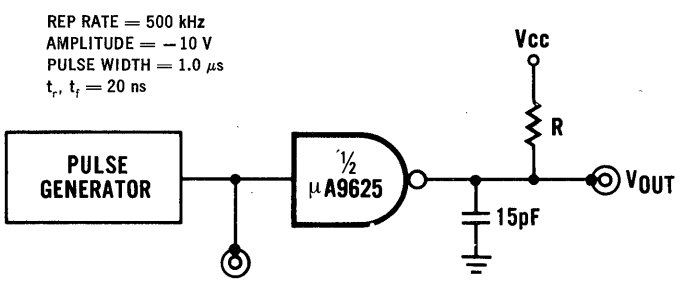
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

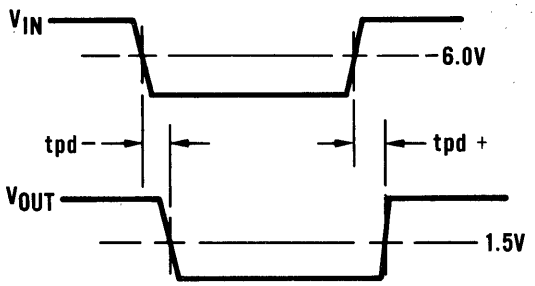


SWITCHING TIME VERSUS AMBIENT TEMPERATURE



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





TESTS	CONDITIONS T_A (°C)	V_{CC} (Volts)	V_{DD} (Volts)	R (kΩ)
t_{pd+}, t_{pd-}	25	5.0	−13	3.75

Fig. 4

μA9644

DUAL HIGH-VOLTAGE, HIGH CURRENT DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA9644 is a Dual 4-Input NAND Gate whose output can sink 500 mA in the low state, and maintain 30 volts in the high state. The outputs are uncommitted collectors in a Darlington configuration which have typical saturation voltages of 0.8 volts at low currents and 1.2 volts at 500 mA. The inputs are TTL Compatible and feature input clamp diodes. The input fan-in requirement is typically 1/2 a normal DTL Unit Load. An input strobe common to both gates is provided, and an expander input node on each gate is available for input diode expansion. Separate ground pins are provided for each gate to minimize ground pin offset voltages at high current levels.

- **500 mA CURRENT SINKING CAPABILITY**
- **OUTPUT VOLTAGES UP TO 30 VOLTS**
- **LOW AVERAGE POWER, TYPICALLY 30 mW PER GATE**
- **HIGH SPEED, TYPICALLY 50 ns DELAY TIMES**
- **TTL COMPATIBLE INPUTS**
- **INPUT CLAMP DIODES**
- **LOW FAN-IN LOADING REQUIREMENTS**
- **COMMON STROBE INPUT**
- **EXPANDER NODE FOR INPUT DIODE EXPANSION**

ABSOLUTE MAXIMUM RATING

Storage Temperature		−65° C to +175° C
Temperature (Ambient) Under Bias		−55° C to +125° C
V_{CC} Pin Potential to Ground Pin		−0.5 V to +8.0 V
Input Voltages (D.C.)		−0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	See Safe Area	−0.5 V to +30 V
Output Current (D.C.) (Output Low)		640 mA
Internal Power Dissipation (Note)		730 mW
Lead Temperature (Soldering, 60 seconds)		300° C

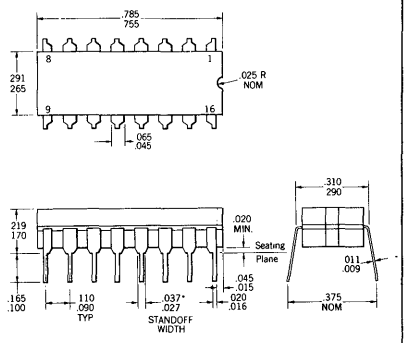
NOTE

Rating applies to ambient temperatures up to 70° C. Above 70° C derate linearly at 8.3 mW/° C for the Ceramic DIP

ORDER INFORMATION – Specify U7B9644XXX for 16-pin Dual In-Line Package where XXX is 51X for the −55° C to +125° C temperature range, or 59X for the 0° C to +75° C temperature range.

PHYSICAL DIMENSIONS

16 Lead MSI Dual In-Line



NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead
Leads are tin plated kovar
Package weight is 2.2 grams
*The $\frac{.037}{.027}$ dimension does not apply to the corner leads

Fig. 2

LOGIC DIAGRAM

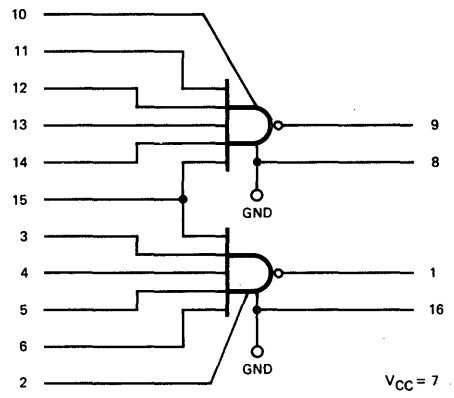


Fig. 1

CONNECTION DIAGRAM

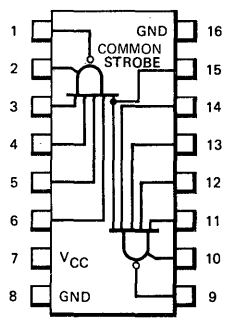


Fig. 3

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

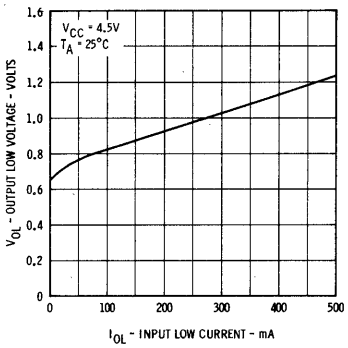
SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS
V_{OL}	Output Low Voltage		1.7		1.25	1.5		1.5	Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 500\ mA$, Inputs = V_{IH}
					0.8	1.0			Volts	$V_{CC} = 5.0\ V$, $I_{OL} = 100\ mA$, Inputs = V_{IH}
I_{CEX}	Output Leakage Current				<1.0	200		500	μA	$V_{CC} = 5.5\ V$, $V_{CEX} = 30\ V$, $V_{IN} = V_{IL}$
I_R	Input Reverse Current				<1.0	2.0		5.0	μA	$V_{CC} = 5.5\ V$, $V_{IN} = 4.5\ V$, Other Inputs = Gnd
I_F	Input Forward Current		−0.75		−0.18	−0.75		−0.75	mA	$V_{CC} = 5.5\ V$, $V_{IN} = 0.4\ V$
I_{RS}	Strobe Reverse Current				<1.0	4.0		10	μA	$V_{CC} = 5.5\ V$, $V_{IN} = 4.5\ V$, Other Inputs = Gnd
I_{FS}	Strobe Forward Current		−1.5		−0.36	−1.5		−1.5	mA	$V_{CC} = 5.5\ V$, $V_{IN} = 0.4\ V$
I_{FX}	Expander Node Forward Current				−2.68	−3.9			mA	$V_{CC} = 5.5\ V$, $V_{IN} = 0.4\ V$
I_{CC}	V_{CC} Current (Gate On)				20.4	30			mA	$V_{CC} = 5.5\ V$, Inputs = Open
I_{MAX}	Max. V_{CC} Rating				7.0	12			mA	$V_{CC} = 8.0\ V$, Inputs = Gnd
V_{F3}	Input Clamp Diode Voltage				−0.8	−1.5			Volts	$V_{CC} = 4.5\ V$, $I_{IN} = -10\ mA$, Other Inputs = Open
V_{IL}	Input Low Voltage		1.3		1.1	1.0		0.7	Volts	Guaranteed Input Low Threshold
V_{IH}	Input High Voltage	2.3		2.1	1.7		1.9		Volts	Guaranteed Input High Threshold
t_{pd+}	Propagation Delay				50	100			ns	$V_{CC} = 5.0\ V$, $C_L = 40\ pF$,
t_{pd-}	Propagation Delay				50	100			ns	$R_L = 75\ \Omega$ to $+30\ V$ (See Fig. 3)

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0 \pm 5\%$)

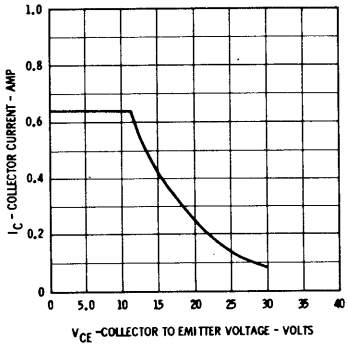
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OL}	Output Low Voltage		1.6		1.25	1.5		1.5	Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 500\ mA$, Inputs = V_{IH}
					0.8	1.0			Volts	$V_{CC} = 5.0\ V$, $I_{OL} = 100\ mA$, Inputs = V_{IH}
I_{CEX}	Output Leakage Current				<1.0	250		500	μA	$V_{CC} = 5.25\ V$, $V_{CEX} = 30\ V$, $V_{IN} = V_{IL}$
I_R	Input Reverse Current				<1.0	5.0		10	μA	$V_{CC} = 5.25\ V$, $V_{IN} = 4.5\ V$, Other Inputs = Gnd
I_F	Input Forward Current		−0.75		−0.18	−0.75		−0.75	mA	$V_{CC} = 5.25\ V$, $V_{IN} = 0.45\ V$
I_{RS}	Strobe Reverse Current				<1.0	10		20	μA	$V_{CC} = 5.25\ V$, $V_{IN} = 4.5\ V$, Other Inputs = Gnd
I_{FS}	Strobe Forward Current		−1.5		−0.36	−1.5		−1.5	mA	$V_{CC} = 5.25\ V$, $V_{IN} = 0.45\ V$
I_{FX}	Expander Node Forward Current				−2.68	−3.9			mA	$V_{CC} = 5.25\ V$, $V_{IN} = 0.45\ V$
I_{CC}	V_{CC} Current (Gate On)				20.4	30			mA	$V_{CC} = 5.25\ V$, Inputs = Open
I_{MAX}	Max. V_{CC} Rating				7.0	12.8			mA	$V_{CC} = 8.0\ V$, Inputs = Gnd
V_{F3}	Input Clamp Diode Voltage				−0.8	−1.5			Volts	$V_{CC} = 4.75\ V$, $I_{IN} = -10\ mA$, Other Inputs = Open
V_{IL}	Input Low Voltage		0.85		1.1	0.85		0.75	Volts	Guaranteed Input Low Threshold
V_{IH}	Input High Voltage	2.2		2.1	1.7		2.1		Volts	Guaranteed Input High Threshold
t_{pd+}	Propagation Delay				50	200			ns	$V_{CC} = 5.0\ V$, $C_L = 40\ pF$,
t_{pd-}	Propagation Delay				50	200			ns	$R_L = 75\ \Omega$ to $+30\ V$ (See Fig. 3)

TYPICAL ELECTRICAL CHARACTERISTICS

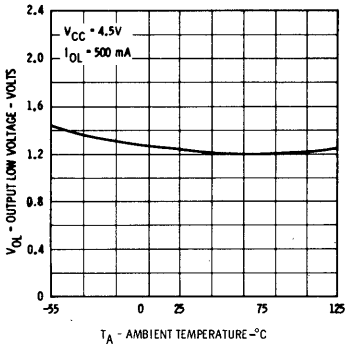
OUTPUT LOW VOLTAGE VERSUS INPUT LOW CURRENT



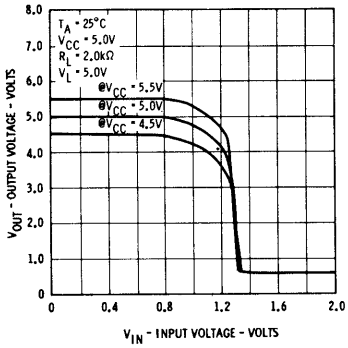
SAFE AREA CURVE



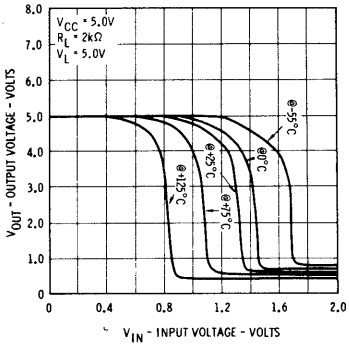
OUTPUT LOW VOLTAGE VERSUS AMBIENT TEMPERATURE



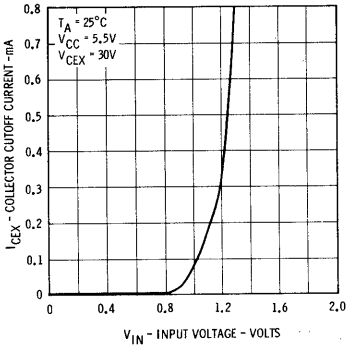
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE AND SUPPLY VOLTAGE



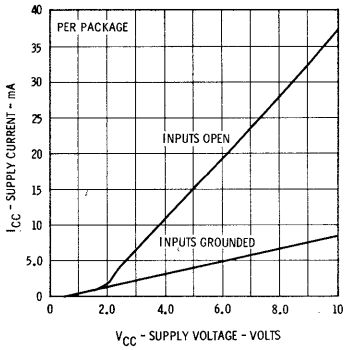
OUTPUT VOLTAGE VERSUS INPUT VOLTAGE AND TEMPERATURE



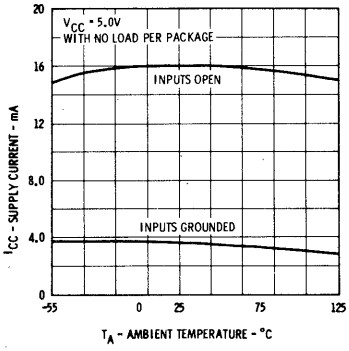
COLLECTOR CUTOFF CURRENT VERSUS INPUT VOLTAGE



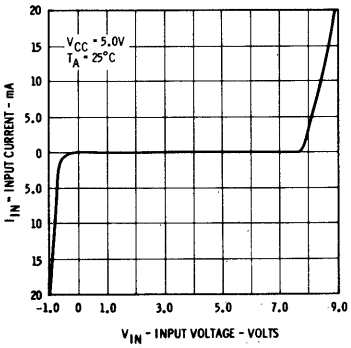
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



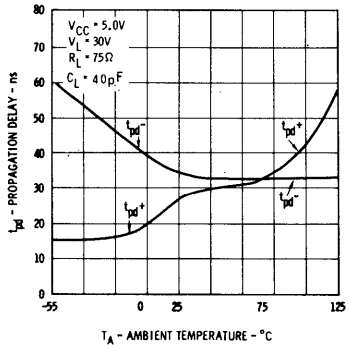
SUPPLY CURRENT VERSUS AMBIENT TEMPERATURE



INPUT CURRENT VERSUS INPUT VOLTAGE



PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE



CURRENT SINKING DERATING CURVE

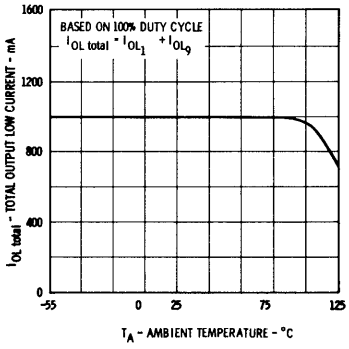
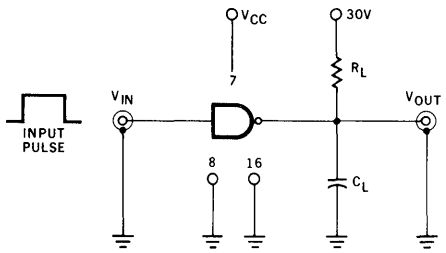
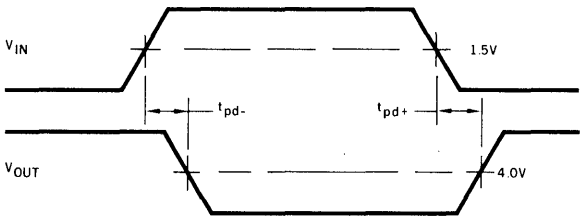


Fig. 3 — SWITCHING CIRCUIT AND WAVEFORMS

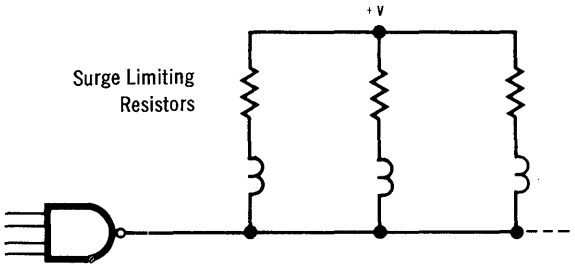




Input Requirements:
Frequency ≃ 100 kHz
Amplitude 3 ±0.1 V
Pulse Width ≃ 500 ns
Rise Time ≦ 10 ns
Fall Time ≦ 10 ns

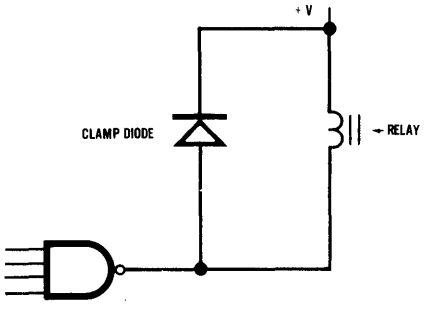
$R_L = 75\ \Omega$
$C_L = 40$ pF

APPLICATIONS



$I_{OL} \leq 500\ mA = N \bullet I_{Bulb} + N \bullet I_{Surge}$

MULTIPLE LAMP DRIVING



+V	$R_{COIL\ (min)}$	I_{max}
28 V	280 Ω	100 mA
24 V	160 Ω	150 mA
18 V	57 Ω	300 mA
15 V	35 Ω	400 mA
12 V	22 Ω	500 mA
6 V	10 Ω	500 mA
5 V	8 Ω	500 mA

The clamp diode must be capable of keeping the μA9644 within its SAFE AREA. The clamp diode must handle all the coil current.

RELAY DRIVING

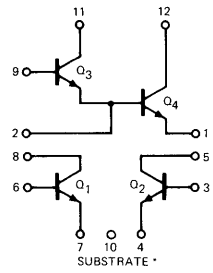
CA3018·CA3018A·CA3019·CA3026·CA3036
CA3039·CA3045·CA3046·CA3054·CA3086

TRANSISTOR AND DIODE ARRAYS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

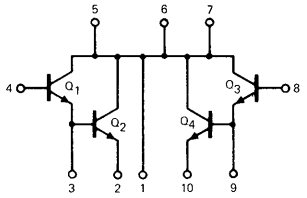
GENERAL DESCRIPTION – Fairchild transistor and diode arrays consist of general purpose integrated circuit devices constructed on a single substrate, using the Fairchild Planar* epitaxial process. These arrays are arranged to offer maximum flexibility in circuit design for applications from D.C. to 120 MHz. Excellent transistor and diode matching and temperature tracking allow circuit techniques unavailable when using discrete devices. Multiple devices in one package permit a greater packing density and cost savings than with individual packaged transistors.

- **PRECISION MONOLITHIC MATCHING**
- **DESIGN FLEXIBILITY**
- **CUSTOM APPLICATIONS**

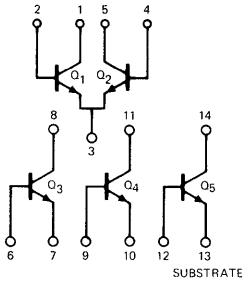


ORDER PART NO.
CA3018/CA3018A
PACKAGE: 5G

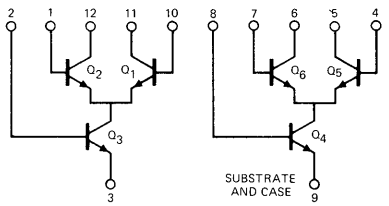
CASE



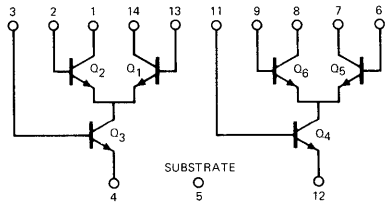
ORDER PART NO.
CA3036
PACKAGE: 5E



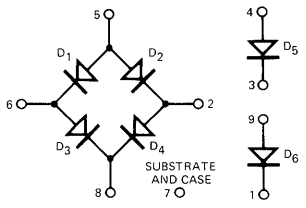
ORDER PART NOS.
CA3045/3046/3086
PACKAGE: 6A



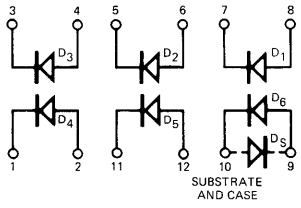
ORDER PART NO.
CA3026
PACKAGE: 5G



ORDER PART NO.
CA3054
PACKAGE: 6A



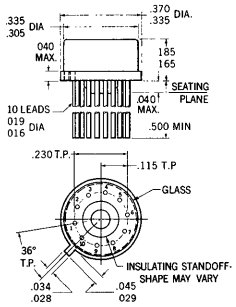
ORDER PART NO.
CA3019
PACKAGE: 5E



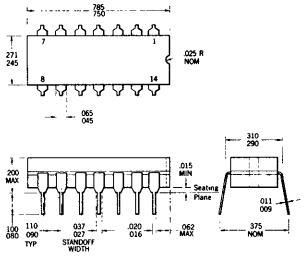
ORDER PART NO.
CA3039
PACKAGE: 5G

PHYSICAL DIMENSIONS

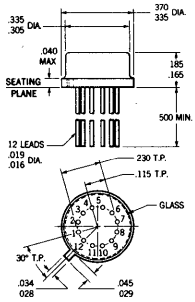
PACKAGE 5E



PACKAGE 6A



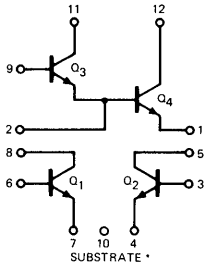
PACKAGE 5G



*Planar is a patented Fairchild process.

- **MATCHED MONOLITHIC GENERAL PURPOSE TRANSISTORS**
- **h_{FE} MATCHED ±10%**
- **V_{BE} MATCHED ±2 mV CA3018A (±5 mV CA3018)**
- **OPERATION FROM DC TO 120 MHz**
- **WIDE OPERATING CURRENT RANGE**
- **CA3018A PERFORMANCE CHARACTERISTICS CONTROLLED FROM 10 μA TO 10 mA**
- **LOW NOISE FIGURE – 3.2 dB TYPICAL AT 1 kHz**
- **FULL MILITARY TEMPERATURE RANGE CAPABILITY (–55 TO +125°C)**

EQUIVALENT CIRCUIT



APPLICATIONS

- General Use in Signal Processing Systems in DC Through VHF Range
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers

ABSOLUTE MAXIMUM RATINGS

	CA3018	CA3018A
Power Dissipation (Note 1)		
Any One Transistor	300 mW	300 mW
Total Package	450 mW	450 mW
Temperature Range		
Operating Temperature	–55°C to +125°C	–55°C to +125°C
Storage Temperature	–65°C to +200°C	–65°C to +200°C
The following ratings apply for each transistor in the device:		
Collector-to-Emitter Voltage, V_{CEO}	15 V	15 V
Collector-to-Base Voltage, V_{CBO}	20 V	30 V
Collector-to-Substrate Voltage, V_{CIO} (Note 2)	20 V	40 V
Emitter-to-Base Voltage, V_{EBO}	5 V	5 V
Collector Current, I_C	50 mA	50 mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	MIN.	TYP.	MAX	UNITS
				CA3018			CA3018A		
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0		0.002	100		0.002	40	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0		See Curve	5		See Curve	0.5	μA
Collector-Cutoff Current Darlington Pair	I_{CEOD}	V_{CE} = 10 V, I_B = 0						5	μA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	24		15	24		V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	20	60		30	60		V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5	7		5	7		V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	20	60		40	60		V
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B = 1 mA, I_C = 10 mA		0.23			0.23	0.5	V
Static Forward Current Transfer Ratio	h_{FE}	V_{CE} = 3 V, I_C = 10 mA		100		50	100		
		V_{CE} = 3 V, I_C = 1 mA	30	100		60	100		
		V_{CE} = 3 V, I_C = 10 μA		54		30	54		
Magnitude of Static-Beta Ratio (Isolated Transistors Q_1 and Q_2)		V_{CE} = 3 V, I_{C1} = I_{C2} = 1 mA	0.9	0.97		0.9	0.97		
Static Forward Current Transfer Ratio Darlington Pair (Q_3 & Q_4)	h_{FED}	V_{CE} = 3 V, I_C = 1 mA	1500	5400		2000	5400		
		V_{CE} = 3 V, I_C = 100 μA				1000	2800		
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_E = 1 mA		0.715		0.600	0.715	0.800	V
		V_{CE} = 3 V, I_E = 10 mA		0.800			0.800	0.900	
Input Offset Voltage	$\lvert V_{BE_1} \rvert$ / $\lvert V_{BE_2} \rvert$	V_{CE} = 3 V, I_E = 1 mA		0.48	5		0.48	2	mV
Temperature Coefficient: Base-to-Emitter Voltage Q_1, Q_2	$\frac{\lvert \Delta V_{BE} \rvert}{\Delta T}$	V_{CE} = 3 V, I_E = 1 mA		–1.9			–1.9		mV/°C
Base (Q_3)-to-Emitter (Q_4) Voltage-Darlington Pair	V_{BED} ($V_{9\text{-}1}$)	V_{CE} = 3 V, I_E = 10 mA		1.46			1.46	1.60	V
		V_{CE} = 3 V, I_E = 1 mA		1.32		1.10	1.32	1.50	
Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair-Q_3,Q_4	$\frac{\lvert \Delta V_{BED} \rvert}{\Delta T}$	V_{CE} = 3 V, I_E = 1 mA		4.4			4.4		mV/°C
Temperature Coefficient of Input-Offset Voltage	$\frac{\lvert V_{BE_1} - V_{BE_2} \rvert}{\Delta T}$	V_{CC} = +6 V, V_{EE} = –6 V,		10			10		μV/°C

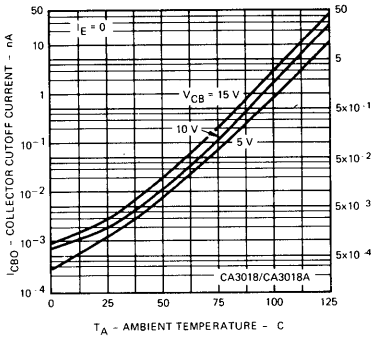
NOTES
1. Derate at 5 mW/°C for T_A > 85°C.
2. Substrate must be connected to the most negative voltage to maintain normal operation.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

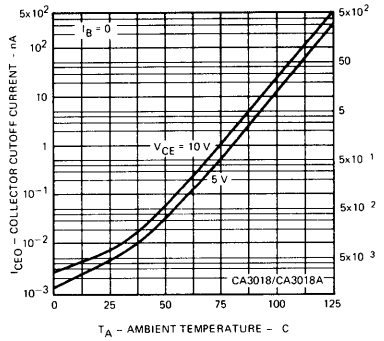
PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS
Low Frequency Noise Figure	NF	f = 1 kHz, V_{CE} = 3 V, I_C = 100 μA Source resistance = 1 kΩ		3.25		dB
Low-Frequency, Small-Signal Equivalent Circuit Characteristics:						
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA		110		
Short-Circuit Input Impedance	h_{ie}			3.5		k Ω
Open-Circuit Output Impedance	h_{oe}			15.6		μmho
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}			1.8×10^{-4}		
Admittance Characteristics:						
Forward Transfer Admittance	Y_{fe}	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA		31–j 1.5		mmho
Input Admittance	Y_{ie}			0.3+j 0.04		mmho
Output Admittance	Y_{oe}			0.001+j 0.03		mmho
Reverse Transfer Admittance	Y_{re}			See Curve		mmho
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 3 mA	300	500		MHz
Emitter-to-Base Capacitance	C_{eb}	V_{EB} = 3 V, I_E = 0		0.6		pF
Collector-to-Base Capacitance	C_{CI}	V_{CB} = 3 V, I_C = 0		0.58		pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CI} = 3 V, I_C = 0		2.8		pF

TYPICAL PERFORMANCE CURVES

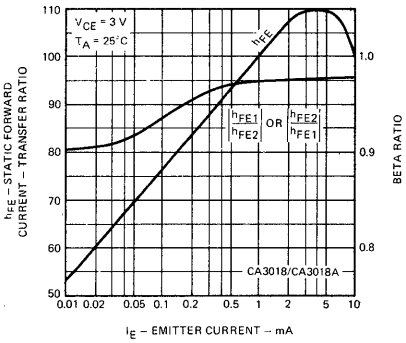
COLLECTOR-TO-BASE CUTOFF CURRENT VERSUS AMBIENT TEMPERATURE FOR EACH TRANSISTOR



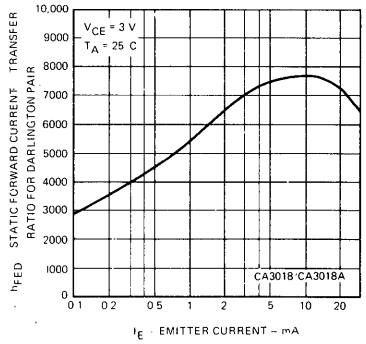
COLLECTOR-TO-EMITTER CUTOFF CURRENT VERSUS AMBIENT TEMPERATURE FOR EACH TRANSISTOR



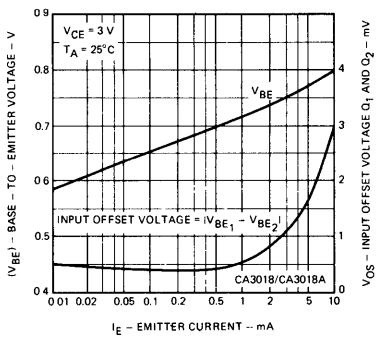
STATIC FORWARD CURRENT-TRANSFER AND BETA RATIO FOR TRANSISTORS Q_1, Q_2 VERSUS EMITTER CURRENT



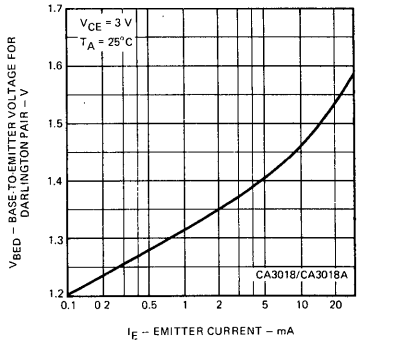
STATIC FORWARD CURRENT-TRANSFER RATIO FOR DARLINGTON CONNECTED TRANSISTORS Q_3, Q_4 VERSUS EMITTER CURRENT



STATIC BASE-TO-EMITTER VOLTAGE AND INPUT OFFSET VOLTAGE FOR Q_1, Q_2 VERSUS EMITTER CURRENT

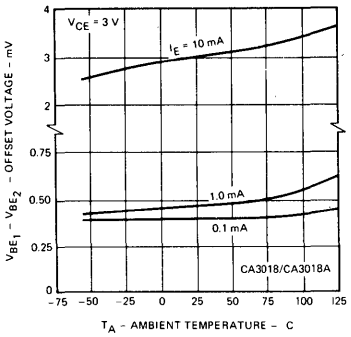


STATIC INPUT VOLTAGE FOR DARLINGTON PAIR Q_3, Q_4 VERSUS EMITTER CURRENT

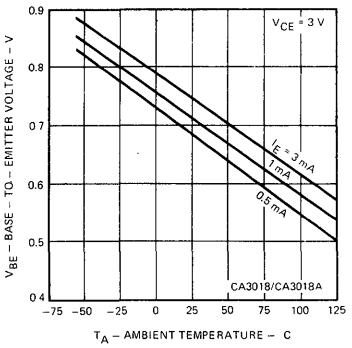


TYPICAL PERFORMANCE CURVES

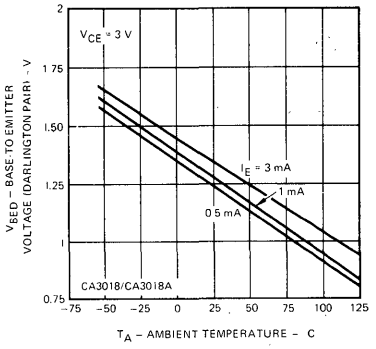
OFFSET VOLTAGE CHARACTERISTIC VERSUS AMBIENT TEMPERATURE



BASE-TO-EMITTER VOLTAGE CHARACTERISTIC FOR EACH TRANSISTOR VERSUS AMBIENT TEMPERATURE

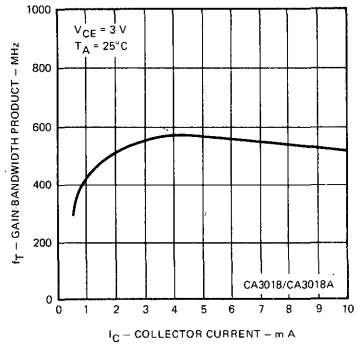


STATIC INPUT VOLTAGE FOR DARLINGTON PAIR (Q_3, Q_4) VERSUS AMBIENT TEMPERATURE

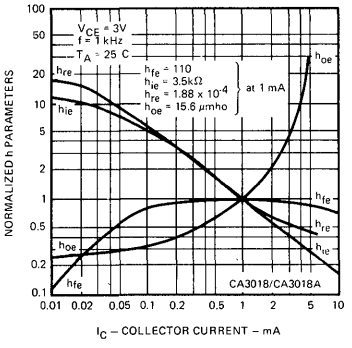


TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

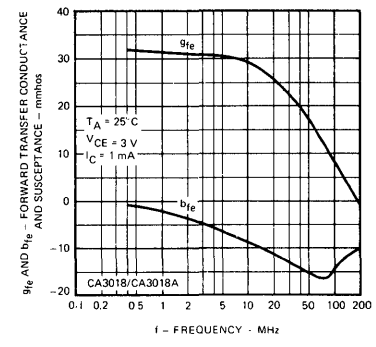
GAIN-BANDWIDTH PRODUCT (f_T) VERSUS COLLECTOR CURRENT



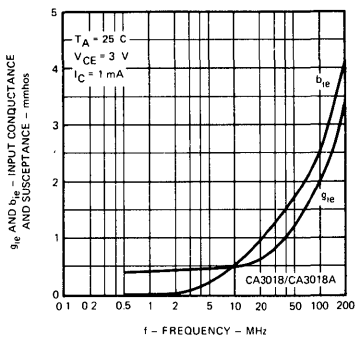
NORMALIZED h PARAMETERS VERSUS COLLECTOR CURRENT



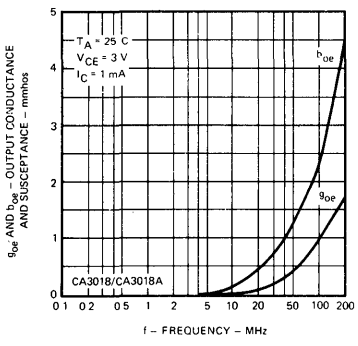
FORWARD TRANSFER ADMITTANCE (Y_{fe}) VERSUS FREQUENCY



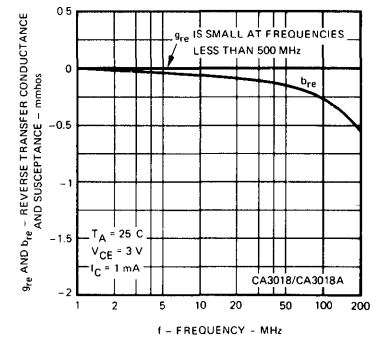
INPUT ADMITTANCE (Y_{ie}) VERSUS FREQUENCY



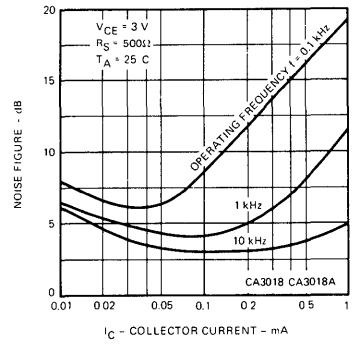
OUTPUT ADMITTANCE (Y_{oe}) VERSUS FREQUENCY



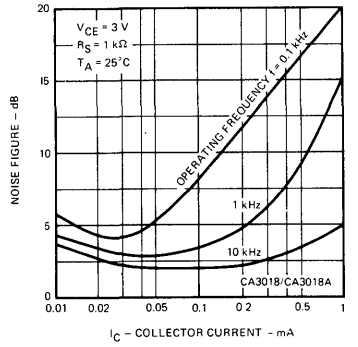
REVERSE TRANSFER ADMITTANCE (Y_{re}) VERSUS FREQUENCY



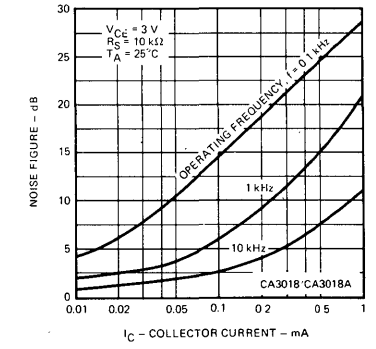
NOISE FIGURE VERSUS COLLECTOR CURRENT, R_S = 500 Ω



NOISE FIGURE VERSUS COLLECTOR CURRENT, R_S = 1 kΩ

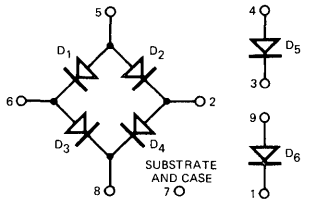


NOISE FIGURE VERSUS COLLECTOR CURRENT, R_S = 10 kΩ



- **EXCELLENT DIODE MATCHING – 1 mV TYP.**
- **LOW REVERSE LEAKAGE CURRENT – 5 mA TYP.**

EQUIVALENT CIRCUIT



APPLICATIONS

- Modulator
- Mixer
- Balanced Modulator
- Analog Switch
- Diode Gate for Chopper-Modulator Applications

ABSOLUTE MAXIMUM RATINGS

Power Dissipation	
For each Diode	20 mW
Total For Device	120 mW
Temperature Range	
Storage Temperature	−65°C to +200°C
Operating Temperature	−55°C to +125°C
Voltage (Note 1)	18 V

ELECTRICAL CHARACTERISTICS (For each diode, $T_A = 25°C$ unless otherwise specified)

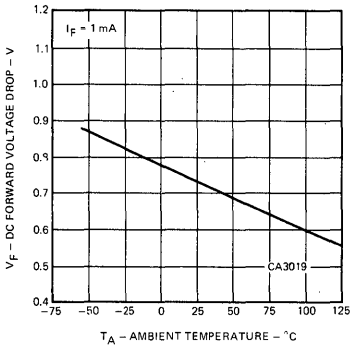
PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS
DC Forward Voltage Drop	V_F	DC Forward Current, I_F = 1 mA		0.73	0.78	V
DC Reverse Breakdown Voltage	$V_{(BR)R}$	DC Reverse Current, $I_R = -10\,\mu A$	4.0	6.0		V
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	DC Reverse Current, $I_R = -10\,\mu A$	25	80		V
DC Reverse (Leakage) Current	I_R	DC Reverse Voltage, $V_R = -4$ V		0.0055	10	μA
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	DC Reverse Voltage, $V_R = -4$ V		0.010	10	μA
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\lvert V_{F_1} - V_{F_2} \rvert$	DC Forward Current, I_F = 1 mA		1.0	5.0	mV
Single Diode Capacitance	C_D	Frequency, f = 1 MHz DC Reverse Voltage, $V_R = -2$ V		1.8		pF
Diode Quad-to-Substrate Capacitance	C_{DQ-1}	Frequency, f = 1 MHz DC Reverse Voltage, V_R between Pins 2,5,6, or 8 of Diode Quad and Pin 7 (Substrate) = −2 V				
		Pin 2 or 6 to Pin 7		4.4		pF
		Pin 5 or 8 to Pin 7		2.7		pF
Series Gate Switching Pedestal Voltage	V_S			10		mV

NOTE

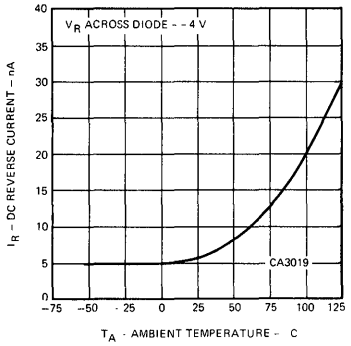
1. Substrate (Pin 7) must be connected to the most negative potential.

TYPICAL PERFORMANCE CURVES

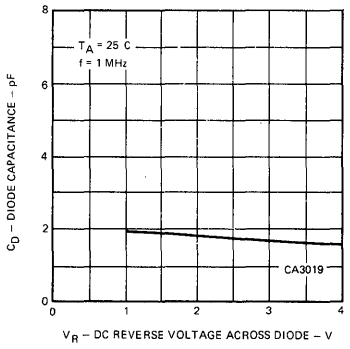
DC FORWARD VOLTAGE DROP (EACH DIODE) VERSUS TEMPERATURE



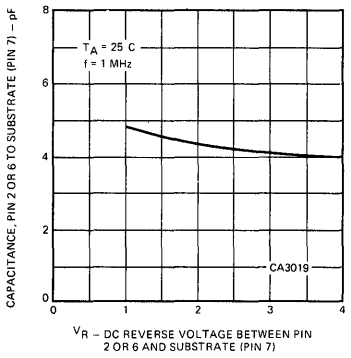
REVERSE (LEAKAGE) CURRENT (EACH DIODE) VERSUS TEMPERATURE



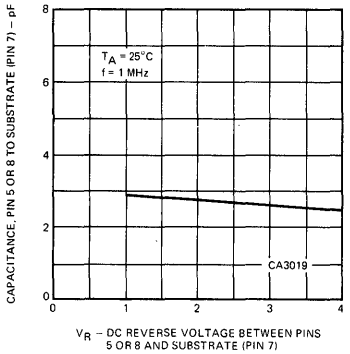
DIODE CAPACITANCE (EACH DIODE) VERSUS REVERSE VOLTAGE



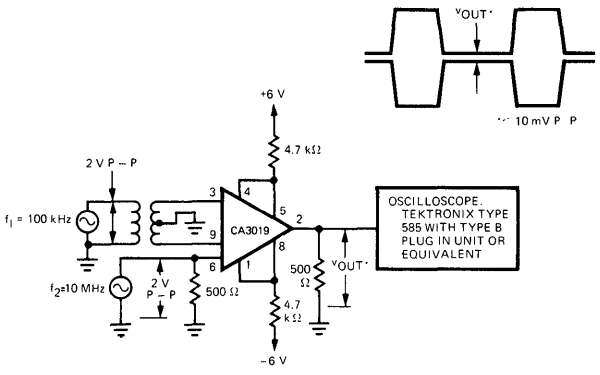
DIODE QUAD-TO-SUBSTRATE CAPACITANCE VERSUS REVERSE VOLTAGE



DIODE QUAD-TO-SUBSTRATE CAPACITANCE VERSUS REVERSE VOLTAGE

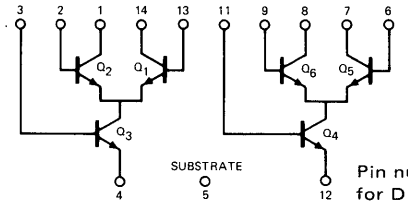


SERIES GATE SWITCHING TEST SETUP



- **LOW INPUT OFFSET VOLTAGE – ±5 mV**
- **WIDEBAND OPERATION**
- **INDEPENDENTLY ACCESSIBLE INPUTS AND OUTPUTS**
- **TWO MATCHED DIFFERENTIAL AMPLIFIERS**

EQUIVALENT CIRCUIT



Pin numbers shown for DIP only.

APPLICATIONS

- Dual Sense Amplifiers
- Dual Schmitt Triggers
- Multifunction Combinations – RF/Mixer/Oscillator; Converter/IF
- IF Amplifiers (Differential and/or Cascode)
- Product Detectors
- Doubly Balanced Modulators and Demodulators
- Balanced Quadrature Detectors
- Cascade Limiters
- Synchronous Detectors
- Pairs of Balanced Mixers
- Synthexizer Mixers
- Balanced (Push-Pull) Cascode Amplifiers

ABSOLUTE MAXIMUM RATINGS (For Each Transistor)

	CA3026	CA3054
Power Dissipation (Note 1)		
Any One Transistor	300 mW	300 mW
Total Package	600 mW	750 mW
Temperature Range		
Operating Temperature	−55°C to +125°C	0°C to +85°C
Storage Temperature	−65°C to +200°C	−25°C to +85°C
The following ratings apply for each transistor in the device		
Collector-to-Emitter Voltage, V_{CEO}		15 V
Collector-to-Base Voltage, V_{CBO}		20 V
Collector-to-Substrate Voltage, V_{CIO} (Note 2)		20 V
Emitter-to-Base Voltage, V_{EBO}		5 V
Collector Current, I_C		50 mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) CA3026 and CA3054

PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS
For Each Differential Amplifier						
Input Offset Voltage	V_{IO}			0.45	5	mV
Input Offset Current	I_{IO}	V_{CB} = 3 V		0.3	2	μA
Input Bias Current	I_I			10	24	μA
Quiescent Operating Current Ratio	$\frac{I_{C(Q_1)}}{I_{C(Q_2)}}$ or $\frac{I_{C(Q_5)}}{I_{C(Q_6)}}$	$I_{E(Q_3)} = I_{E(Q_4)}$ = 2 mA		0.98 to 1.02		
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\Delta\lvert V_{IO}\rvert}{\Delta T}$			1.1		μV/°C
For Each Transistor						
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CB} = 3 V, I_C = 50 μA		0.630	0.700	V
		1 mA		0.715	0.800	
		3 mA		0.750	0.850	
		10 mA		0.800	0.900	
Temperature Coefficient of Base to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CB} = 3 V, I_C = 1 mA		−1.9		mV/°C
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0		0.002	100	nA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	24		V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	20	60		V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	20	60		V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5	7		V

NOTES

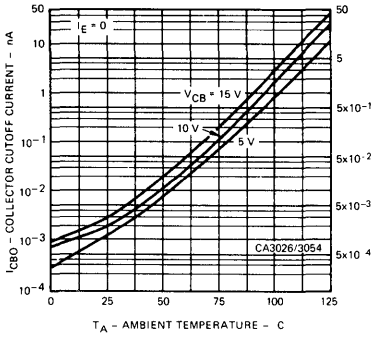
1. For $T_A > 55°C$; CA3026 derates at 5 mW/°C and CA3054 at 6.67 mW/°C
2. The collector of each transistor of the CA3026 and CA3054 is isolated from the substrate by an integral diode. Substrate must be connected to the most negative voltage to maintain normal operation.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) CA3026 and CA3054 (Continued)

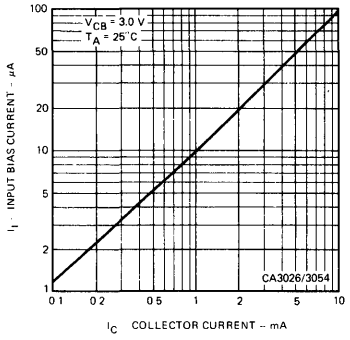
PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS
Common-Mode Rejection Ratio for Each Amplifier	CMR	V_{CC} = 12 V		100		dB
AGC Range, One Stage	AGC	V_{EE} = −6 V		75		dB
Voltage Gain, Single Stage Double-Ended Output	A	V_X = −3.3 V		32		dB
AGC Range, Two Stage	AGC	f = 1 kHz		105		dB
Voltage Gain, Two Stage Double-Ended Output	A			60		dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: (for Single Transistor)						
Forward Current-Transfer Ratio	h_{fe}			110		
Short-Circuit Input Impedance	h_{ie}	f = 1 kHz, V_{CE} = 3 V,		3.5		kΩ
Open-Circuit Output Impedance	h_{oe}	I_C = 1 mA		15.6		μmho
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}			1.8×10^{-4}		
1/f Noise Figure (for Single Transistor)	NF	f = 1 kHz, V_{CE} = 3 V		3.25		dB
Gain-Bandwidth Product (for Single Transistor)	f_T	V_{CE} = 3 V, I_C = 3 mA		550		MHz
Admittance Characteristics; Differential Circuit Configuration: (for Each Amplifier)						
Forward Transfer Admittance	y_{21}	V_{CB} = 3 V		−20+j 0		mmho
Input Admittance	y_{11}	Each Collector		0.22+j 0.1		mmho
Output Admittance	y_{22}	$I_C \approx$ 1.25 mA		0.01+j 0		mmho
Reverse Transfer Admittance	y_{12}	f = 1 MHz		−0.003+j 0		mmho
Admittance Characteristics; Cascode Circuit Configuration: (for Each Amplifier)						
Forward Transfer Admittance	y_{21}	V_{CB} = 3 V		68-j 0		mmho
Input Admittance	y_{11}	Total Stage		0.55+j 0		mmho
Output Admittance	y_{22}	$I_C \approx$ 2.5 mA		0+j 0.02		mmho
Reverse Transfer Admittance	y_{12}	f = 1 MHz		0.004-j 0.005		μmho
Noise Figure	NF	f = 100 MHz		8		dB

TYPICAL PERFORMANCE CURVES

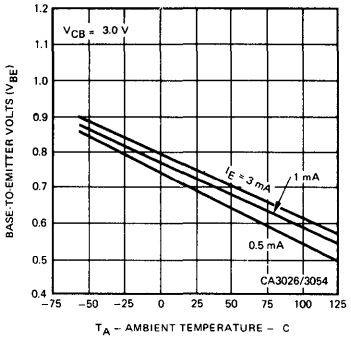
COLLECTOR-TO-BASE CUTOFF CURRENT VERSUS AMBIENT TEMPERATURE FOR EACH TRANSISTOR



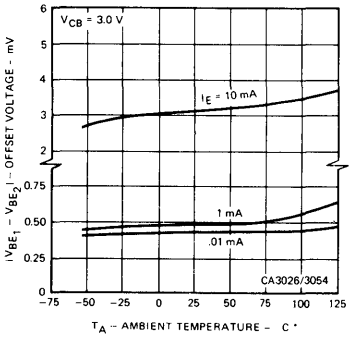
INPUT BIAS CURRENT CHARACTERISTIC VERSUS COLLECTOR CURRENT FOR EACH TRANSISTOR



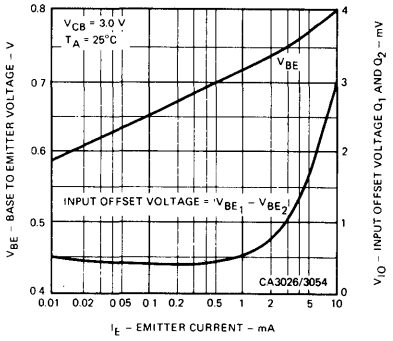
BASE-TO-EMITTER VOLTAGE CHARACTERISTIC FOR EACH TRANSISTOR VERSUS AMBIENT TEMPERATURE



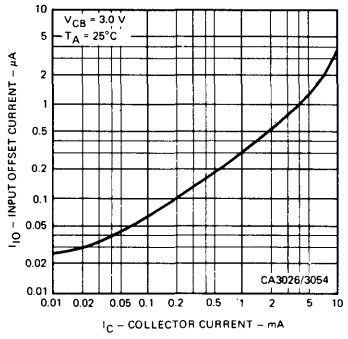
OFFSET VOLTAGE CHARACTERISTIC VERSUS AMBIENT TEMPERATURE FOR DIFFERENTIAL PAIRS



STATIC BASE-TO-EMITTER VOLTAGE CHARACTERISTIC AND INPUT OFFSET VOLTAGE FOR DIFFERENTIAL PAIRS VS EMITTER CURRENT

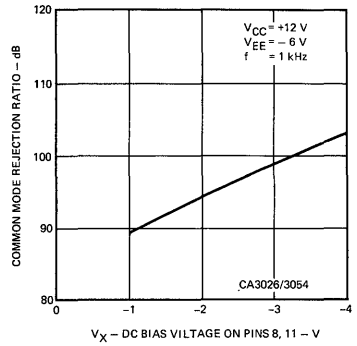


INPUT OFFSET CURRENT FOR MATCHED DIFFERENTIAL PAIRS VERSUS COLLECTOR CURRENT

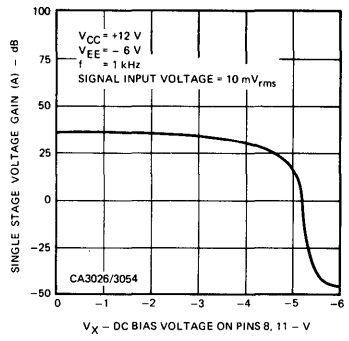


TYPICAL PERFORMANCE CURVES

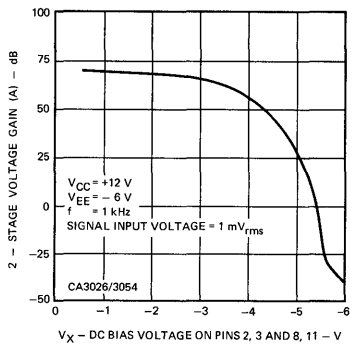
COMMON MODE REJECTION RATIO

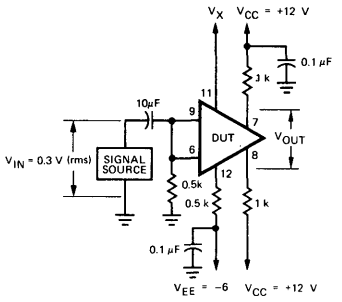


SINGLE STAGE VOLTAGE GAIN

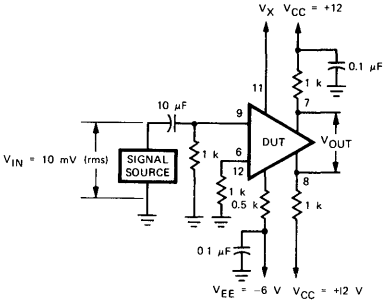


TWO-STAGE VOLTAGE GAIN

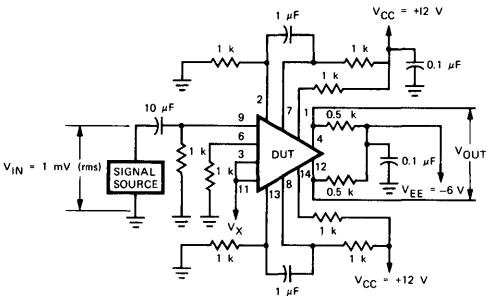




Test setup



Test setup

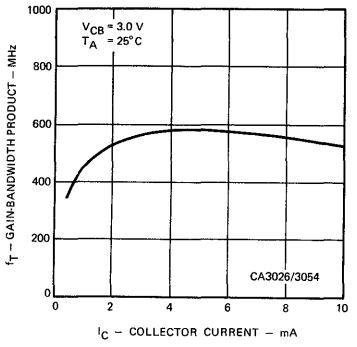


Test setup

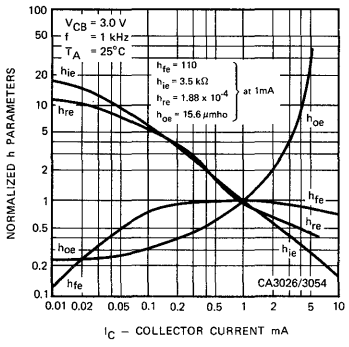
Pin numbers are shown for CA3054 (DIP) only.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

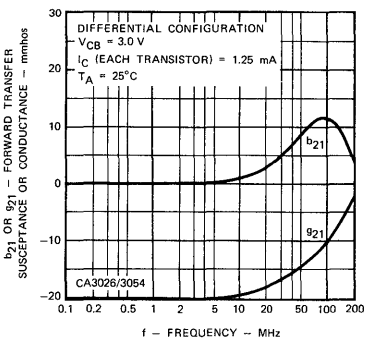
GAIN BANDWIDTH PRODUCT (f_T) VERSUS COLLECTOR CURRENT



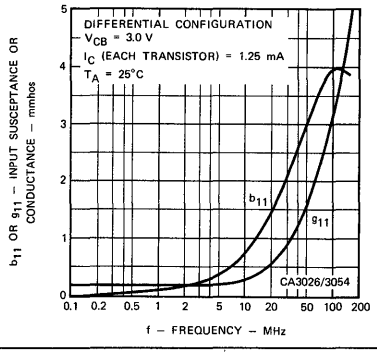
NORMALIZED h PARAMETER VERSUS COLLECTOR CURRENT FOR EACH TRANSISTOR



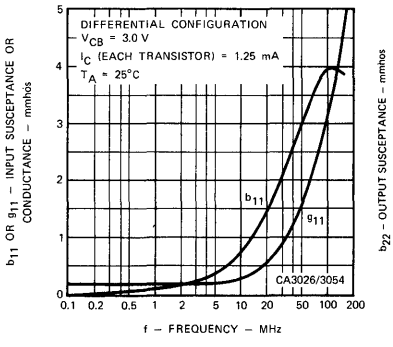
FORWARD TRANSFER ADMITTANCE (Y_{21}) VERSUS FREQUENCY



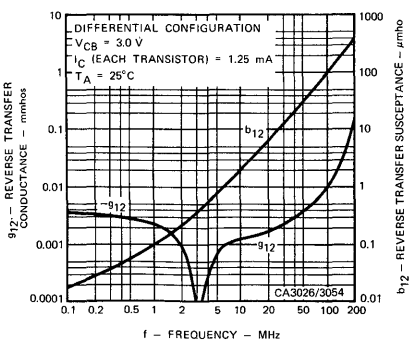
INPUT ADMITTANCE (Y_{11}) VERSUS FREQUENCY



OUTPUT ADMITTANCE (Y_{22}) VERSUS FREQUENCY

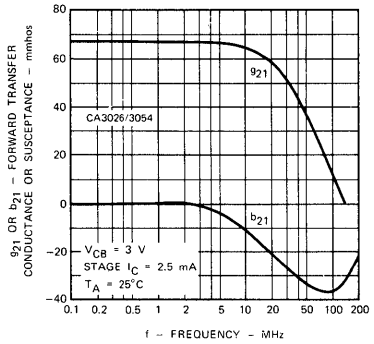


REVERSE TRANSFER ADMITTANCE (Y_{12}) VERSUS FREQUENCY

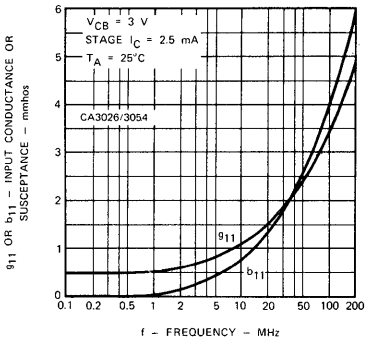


TYPICAL DYNAMIC CHARACTERISTICS FOR EACH CASCODE AMPLIFIER

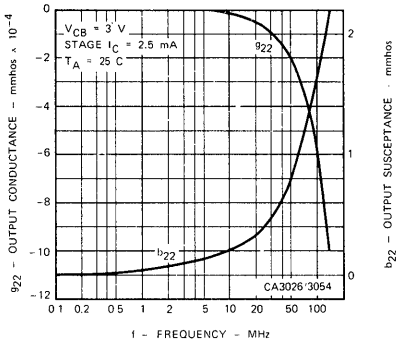
FORWARD TRANSFER ADMITTANCE (Y_{21}) VERSUS FREQUENCY



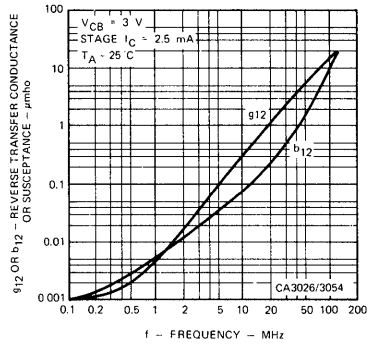
INPUT ADMITTANCE (Y_{11}) VERSUS FREQUENCY



OUTPUT ADMITTANCE (Y_{22}) VERSUS FREQUENCY



REVERSE TRANSFER ADMITTANCE (Y_{12}) VERSUS FREQUENCY



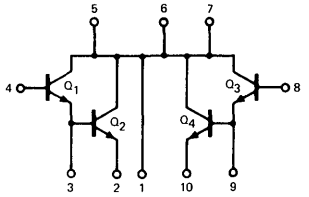
- **MATCHED TRANSISTOR PERFORMANCE**
- **LOW NOISE PERFORMANCE**
- **200 MHz GAIN BANDWIDTH PRODUCT**

APPLICATIONS

- Stereo Phonograph Preamplifiers
- Low-level Stereo and Single Channel Amplifier Stages
- Low-noise, Emitter-follower Differential Amplifiers
- Operational Amplifier Drivers

EQUIVALENT CIRCUIT

CASE



ABSOLUTE MAXIMUM RATINGS (For Each Transistor)

Power Dissipation	
Any One Transistor	300 mW
Total For Array	300 mW
Temperature Range	
Operating Temperature	−55°C to +125°C
Storage Temperature	−65°C to +200°C
The following ratings apply for each transistor in the array	
Collector-to-Emitter Voltage, V_{CEO}	15 V
Collector-to-Base Voltage, V_{CBO}	30 V
Emitter-to-Base Voltage, V_{EBO}	5 V
Collector Current, I_C	50 mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

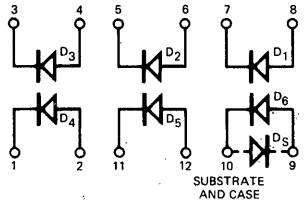
PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS
For Each Transistor (Q_1, Q_2, Q_3, Q_4)						
Collector-Cutoff Current	I_{CBO}	V_{CB} = 5 V, I_E = 0			0.5	μA
Collector-Cutoff Current	I_{CEO}	V_{CE} = 15 V, I_B = 0			5.0	μA
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	20		V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	30	44		V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5.0	6.0		V
For Either Input Transistor (Q_1 or Q_3)						
Static Forward Current-Transfer Ratio	h_{FE}	I_{C1} or I_{C3} = 1 mA	30	82		
For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)						
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO(D)}$	I_{E2} or I_{E4} = 10 μA	10	12.6		V
Static Forward Current-Transfer Ratio	$h_{FE(D)}$	$I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 1 mA	1000	4540		
For Each Input Transistor (Q_1 or Q_3)						
Short-Circuit Forward Current-Transfer Ratio	h_{fe}			82		
Short-Circuit Input Impedance	h_{ie}	f = 1 kHz		2.6		kΩ
Open-Circuit Output Admittance	h_{oe}	I_{C1} or I_{C3} = 1 mA		7.0		μmho
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}			9.8×10^{-5}		
For Either Darlington Pair (Q_1, Q_2 or Q_3, Q_4)						
Short-Circuit Forward Current-Transfer Ratio	$h_{fe(D)}$	f = 1 kHz		1300		
Short-Circuit Input Impedance	$h_{ie(D)}$	$I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 1 mA		82		kΩ
Open-Circuit Output Admittance	$h_{oe(D)}$			108		μmho
Open-Circuit Reverse Voltage-Transfer Ratio	$h_{re(D)}$			2.7×10^{-3}		
Noise Voltage	E_N	f = 100 Hz		0.2	3.0	$\frac{\mu V\ (rms)}{\sqrt{f(Hz)}}$
		f = 1 kHz		0.05	0.3	
		f = 10 kHz		0.012	0.1	
For Either Input Transistor (Q_1 or Q_3)						
Forward Transfer Admittance	y_{fe}			0.68 + j 7.9		mmho
Input Admittance (Output Short-Circuited)	y_{ie}	f = 50 MHz		4.4 + j 5.95		mmho
Output Admittance (Input Short-Circuited)	y_{oe}	I_{C1} or I_{C3} = 2 mA		1.94 + j 2.64		mmho
Reverse Transfer Admittance (Input Short-Circuited)	y_{re}			Negligible		mmho
For Either Darlington Pair (Q_1, Q_2, or Q_3, Q_4)						
Input Admittance (Output Short-Circuited)	$y_{ie(D)}$	f = 50 MHz		1.71 + j 2.8		mmho
Output Admittance (Input Short-Circuited)	$y_{oe(D)}$	$I_{C1} + I_{C2}$ or $I_{C3} + I_{C4}$ = 2 mA		3.96 + j 2.6		mmho
Gain-Bandwidth Product	$f_T(D)$		150	200		MHz

- **EXCELLENT DIODE MATCHING – 1 mV TYP.**
- **REVERSE RECOVERY TIME – 1 ns TYP.**
- **LOW DIODE CAPACITANCE – 0.65 pF @ V_R = –2 V**

APPLICATIONS

- Balanced Modulators or Demodulators
- Ring Modulators
- High Speed Diode Gates
- Analog Switches

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Power Dissipation (See note)	
Any One Diode Unit	100 mW
Total for Device	600 mW
Temperature Range	
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +200°C
Voltages and Currents	
Peak Inverse Voltage, PIV for: D_1 - D_5	5 V
D_6	0.5 V
Peak Diode-to-Substrate Voltage, V_{DI} for D_1 - D_5 (term. 1,4,5,8 or 12 to term. 10)	+20, - 1 V
DC Forward Current, I_F	25 mA
Peak Recurrent Forward Current, I_f	100 mA
Peak Forward Surge Current, I_f (surge)	100 mA

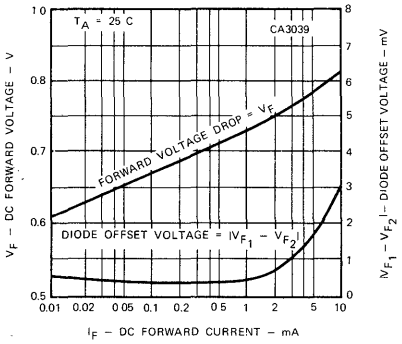
ELECTRICAL CHARACTERISTICS (For each diode unit, T_A = 25°C unless otherwise specified)

PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS
DC Forward Voltage Drop	V_F	I_F = 50 μA		0.65	0.69	V
		1 mA		0.73	0.78	V
		3 mA		0.76	0.80	V
		10 mA		0.81	0.90	V
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = –10 μA	5.0	7.0		V
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	I_R = –10 μA	20			V
DC Reverse (Leakage) Current	I_R	V_R = –4 V		0.016	100	nA
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	V_R = –10 V		0.022	100	nA
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\lvert V_{F_1} - V_{F_2} \rvert$	I_F = 1 mA		0.5	5.0	mV
Temperature Coefficient of $\lvert V_{F_1} - V_{F_2} \rvert$	$\frac{\Delta \lvert V_{F_1} - V_{F_2} \rvert}{\Delta T}$	I_F = 1 mA		1.0		μV/°C
Temperature Coefficient of Forward Drop	$\frac{\Delta V_F}{\Delta T}$	I_F = 1 mA		–1.9		mV/°C
DC Forward Voltage Drop for Anode-to-Substrate Diode (D_S)	V_F	I_F = 1 mA		0.65		V
Reverse Recovery Time	t_{rr}	I_F = 10 mA, I_R = 10 mA		1.0		ns
Diode Resistnace	R_D	f = 1 kHz, I_F = 1 mA	25	30	45	Ω
Diode Capacitance	C_D	V_R = –2 V, I_F = 0		0.65		pF
Diode-to-Substrate Capacitance	C_{DI}	V_{DI} = +4 V, I_F = 0		3.2		pF

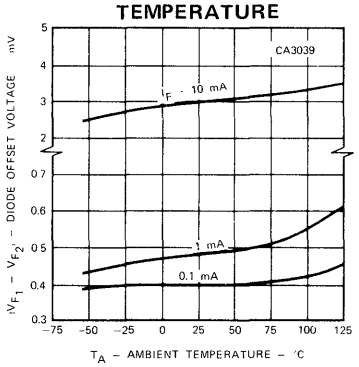
NOTE: Derate at 5.7 mW/°C for $T_A > 55°C$.

TYPICAL PERFORMANCE CURVES

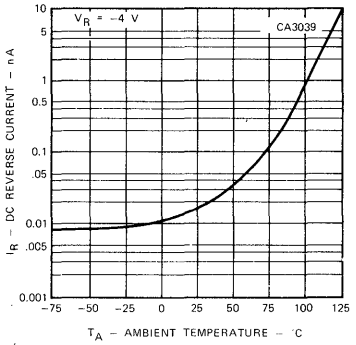
DC FORWARD VOLTAGE DROP (ANY DIODE) AND DIODE OFFSET VOLTAGE VERSUS DC FORWARD CURRENT



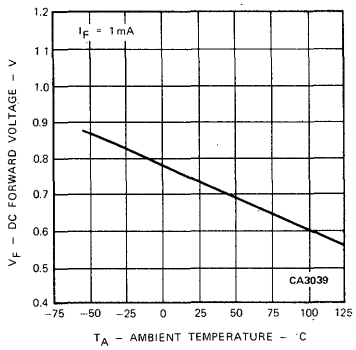
DIODE OFFSET VOLTAGE (ANY DIODE) VERSUS TEMPERATURE



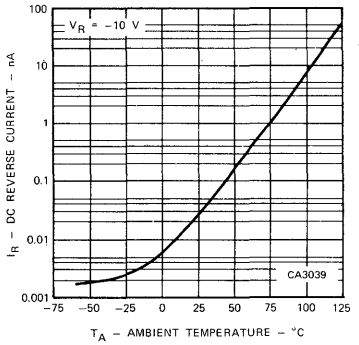
DC REVERSE (LEAKAGE) CURRENT (DIODES 1, 2, 3, 4, 5) VERSUS TEMPERATURE



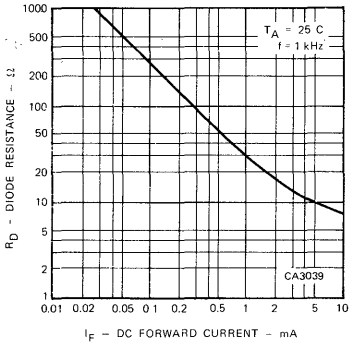
DC FORWARD VOLTAGE DROP (ANY DIODE) VERSUS TEMPERATURE



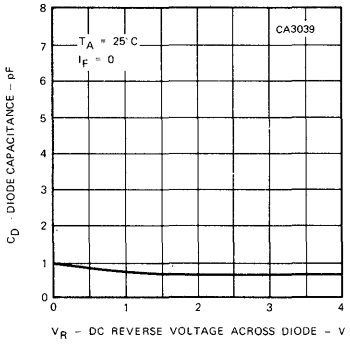
DC REVERSE (LEAKAGE) CURRENT BETWEEN DIODES (1, 2, 3, 4, 5) AND SUBSTRATE VERSUS TEMPERATURE



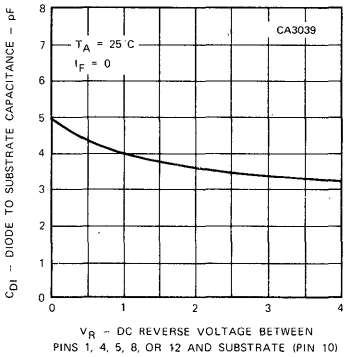
DIODE RESISTANCE (ANY DIODE) VERSUS DC FORWARD CURRENT



DIODE CAPACITANCE (DIODES 1, 2, 3, 4, 5) VERSUS REVERSE VOLTAGE



DIODE-TO-SUBSTRATE CAPACITANCE VERSUS REVERSE VOLTAGE

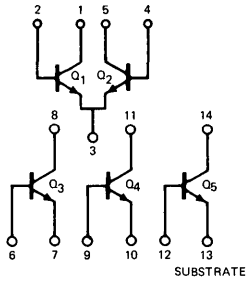


- **LOW INPUT OFFSET VOLTAGE**
- **WIDEBAND OPERATION**
- **LOW NOISE**

APPLICATIONS

- General Use in all Types of Signal Processing Systems Operating Anywhere in the Frequency Range From DC to VHF
- Custom Designed Differential Amplifiers
- Temperature Compensated Amplifiers

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (For Each Transistor)

	CA3045		CA3046/3086	
Power Dissipation (Note 1)	**Each Transistor**	**Total Package**	**Each Transistor**	**Total Package**
At T_A = 25°C	300 mW	750 mW	300 mW	750 mW
At T_A = 25°C to 55°C			300 mW	750 mW
At T_A = 25°C to 75°C	300 mW	750 mW		
Voltages and Currents				
Collector-to-Emitter Voltage, V_{CEO}	15 V		15 V	
Collector-to-Base Voltage, V_{CBO}	20 V		20 V	
Collector-to-Substrate Voltage, V_{CIO} (Note 2)	20 V		20 V	
Emitter-to-Base Voltage, V_{EBO}	5 V		5 V	
Collector Current, I_C	50 mA		50 mA	
Temperature Range				
Operating Temperature	−55°C to +125°C		(CA3046) 0°C to +85°C (CA3086) −40°C to +85°C	
Storage Temperature	−65°C to +200°C		−55°C to +125°C	

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

PARAMETER		CONDITIONS	CA3045, CA3046			CA3086			UNITS
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	20	60		20	60		V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	24		15	24		V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	20	60		20	60		V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5.0	7.0		5.0	7.0		V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0		0.002	40		0.002	100	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0		See curve	0.5		See curve	5.0	μA
Static Forward Current-Transfer Ratio (Static Beta)	h_{FE}	V_{CE} = 3 V, I_C = 10 mA		100			100		
		V_{CE} = 3 V, I_C = 1 mA	40	100		40	100		
		V_{CE} = 3 V, I_C = 10 μA		54			54		
Input Offset Current for Matched Pair Q_1 and Q_2 $\lvert I_{IO_1} - I_{IO_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA		0.3	2.0				μA
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_E = 1 mA		0.715			0.715		V
		V_{CE} = 3 V, I_E = 10 mA		0.800			0.800		
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE_1} - V_{BE_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA		0.45	5.0				mV
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE_3} - V_{BE_4} \rvert$, $\lvert V_{BE_4} - V_{BE_5} \rvert$, $\lvert V_{BE_5} - V_{BE_3} \rvert$		V_{CE} = 3 V, I_C = 1 mA		0.45	5.0				mV
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA		−1.9			−1.9		mV/°C
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_B = 1 mA, I_C = 10 mA		0.23			0.23		V
Temperature Coefficient of Input-Offset Voltage	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA		1.1					μV/°C

NOTES

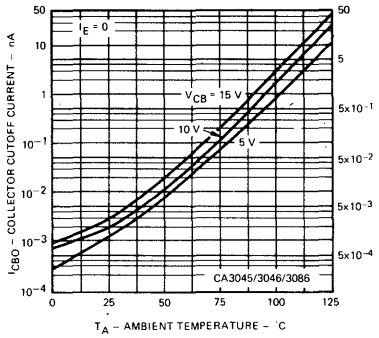
1. CA3046 and CA3086 derate at 6.67 mW/°C for $T_A > 55°C$, CA3045 at 8 mW/°C for $T_A > 75°C$.
2. Substrate (Pin 10) must be connected to the most negative voltage to maintain normal operation.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Continued)

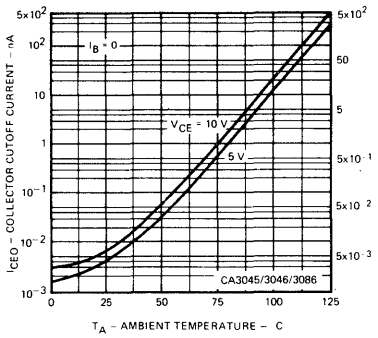
PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS
Low-Frequency Noise Figure	NF	f = 1 kHz, V_{CE} = 3 V, I_C = 100 μA, R_S = 1 kΩ		3.25		dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:						
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA		110 (CA3045, CA3046)		
Forward Current-Transfer Ratio	h_{fe}			110 (CA3086)		
Short-Circuit Input Impedance	h_{ie}			3.5		kΩ
Open-Circuit Output Impedance	h_{oe}			15.6		μmho
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}			1.8×10^{-4}		
Admittance Characteristics:						
Forward Transfer Admittance	Y_{fe}	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA		31 - j 1.5		
Input Admittance	Y_{ie}			0.3+j 0.04		
Output Admittance	Y_{oe}			0.001+j 0.03		
Reverse Transfer Admittance	Y_{re}			See curve		
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 3 mA	300	550		
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3V, I_E = 0		0.6		pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0		0.58		pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0		2.8		pF

TYPICAL PERFORMANCE CURVES

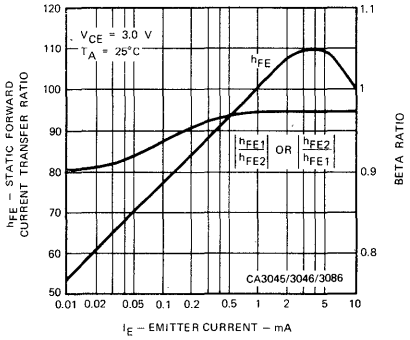
COLLECTOR-TO-BASE CUTOFF CURRENT VERSUS AMBIENT TEMPERATURE FOR EACH TRANSISTOR



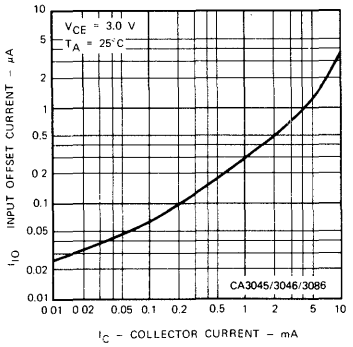
COLLECTOR-TO-EMITTER CUTOFF CURRENT VERSUS AMBIENT TEMPERATURE FOR EACH TRANSISTOR



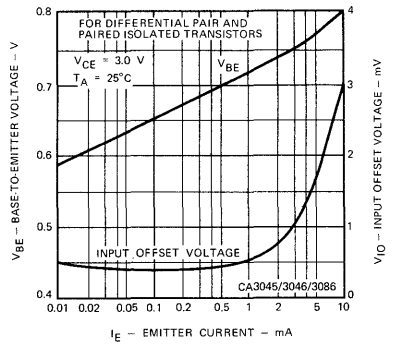
STATIC FORWARD CURRENT-TRANSFER AND BETA RATIO FOR TRANSISTORS Q_1, Q_2 VERSUS EMITTER CURRENT



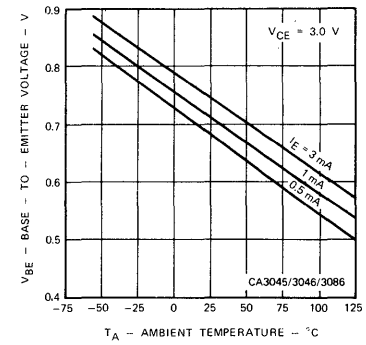
INPUT OFFSET CURRENT FOR MATCHED TRANSISTOR PAIR Q_1, Q_2 VERSUS COLLECTOR CURRENT



STATIC BASE-TO-EMITTER VOLTAGE AND INPUT OFFSET VOLTAGE VERSUS EMITTER CURRENT

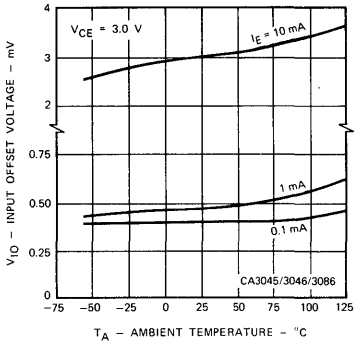


BASE-TO-EMITTER VOLTAGE CHARACTERISTIC VERSUS AMBIENT TEMPERATURE FOR EACH TRANSISTOR

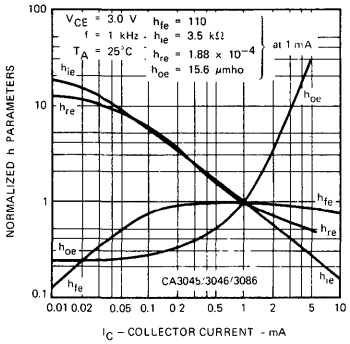


TYPICAL PERFORMANCE CURVES

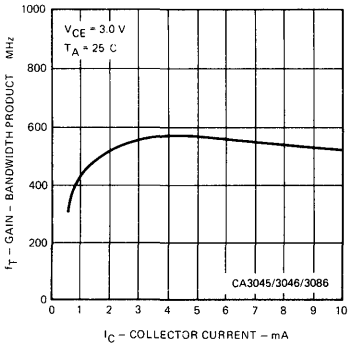
INPUT OFFSET VOLTAGE FOR DIFFERENTIAL PAIR AND PAIRED ISOLATED TRANSISTORS VERSUS AMBIENT TEMPERATURE



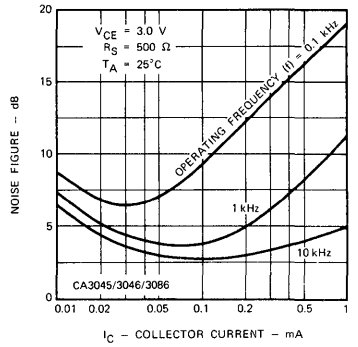
NORMALIZED h PARAMETERS VERSUS COLLECTOR CURRENT



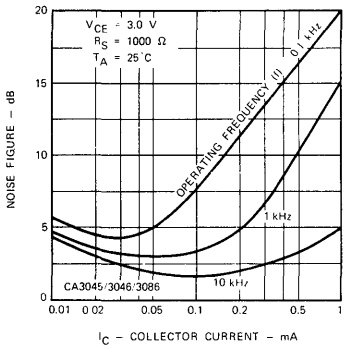
GAIN-BANDWIDTH PRODUCT VERSUS COLLECTOR CURRENT



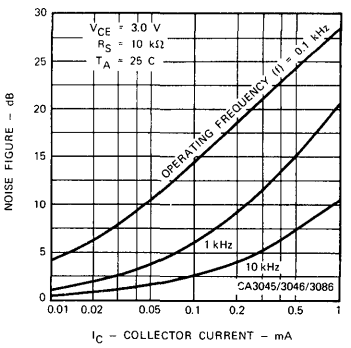
NOISE FIGURE VERSUS COLLECTOR CURRENT



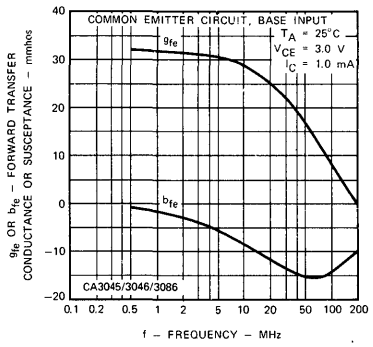
NOISE FIGURE VERSUS COLLECTOR CURRENT



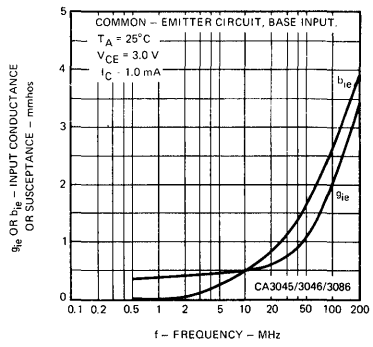
NOISE FIGURE VERSUS COLLECTOR CURRENT



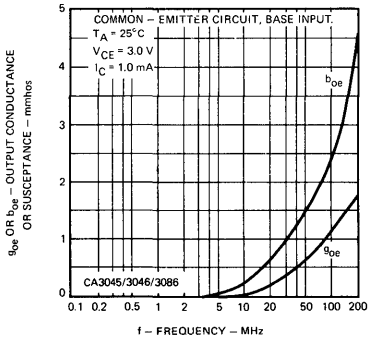
FORWARD TRANSFER ADMITTANCE VERSUS FREQUENCY



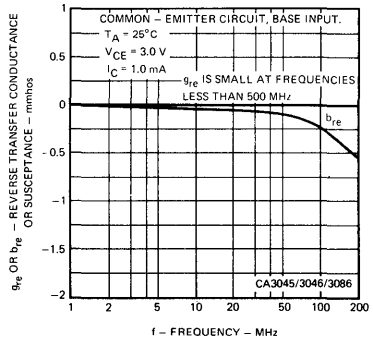
INPUT ADMITTANCE VERSUS FREQUENCY



OUTPUT ADMITTANCE VERSUS FREQUENCY



REVERSE TRANSFER ADMITTANCE VERSUS FREQUENCY



CA3064

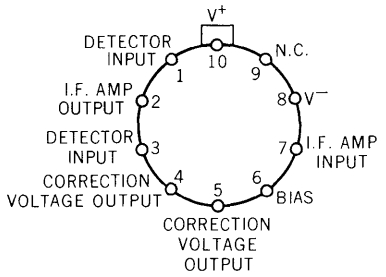
TV AUTOMATIC FINE-TUNING CIRCUIT

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The CA3064 is a TV automatic fine-tuning linear integrated circuit constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The CA3064 combines all of the automatic fine-tuning circuitry, except transformers, in one integrated circuit. Systems with low level I.F. amplifiers can now achieve tuning accuracies of ±25 kHz due to the CA3064's high sensitivity. Internal voltage regulation improves overall performance and reduces system cost.

- **HIGH SENSITIVITY**
- **25 kHz MAX. FREQUENCY DEVIATION**
- **INTERNAL VOLTAGE REGULATOR**
- **INTERNAL AGC**

CONNECTION DIAGRAM
(TOP VIEW)



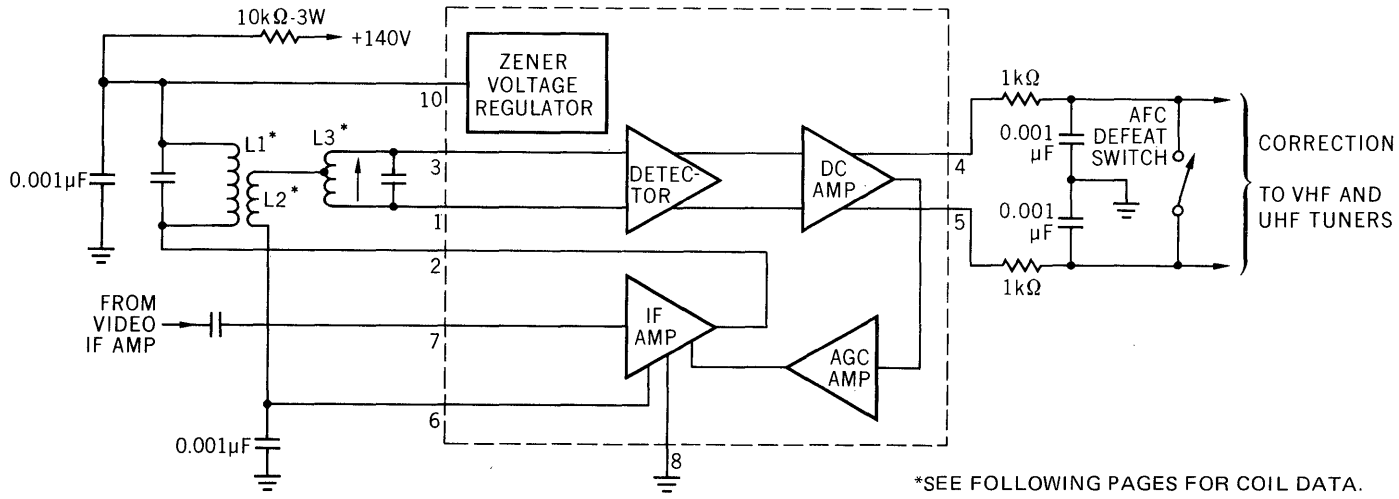
ORDER PART NO: CA3064

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage	Note 2
Internal Power Dissipation (Note 3)	700 mW
Detector Differential Voltage (V_{1-3})	± 10 V
Detector Input Voltage Range (V_1, V_3)	+ 5 V, -6 V
I.F. Amp Output (V_2)	+ 20 V, 0 V
Bias Voltage (V_6)	+ 2 V, 0 V
Storage Temperature Range	-65°C to + 150°C
Operating Temperature range	-40°C to + 85°C
Lead Temperature (soldering, 60 seconds)	300°C

NOTES:
(1) All voltages referenced to V^- except as noted.
(2) V^+ terminal may be connected to any positive voltage source through a suitable dropping resistor, provided the dissipation rating is not exceeded.
(3) Derate linearly at 5.6 mW/°C for ambient temperatures above + 25°C.

BLOCK DIAGRAM



*SEE FOLLOWING PAGES FOR COIL DATA.

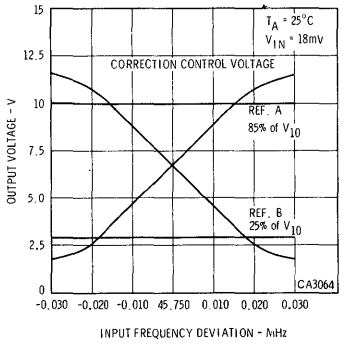
*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (V_{CC} = + 30 V, R_S = 1.5 kΩ, T_A = 25°C unless otherwise specified)

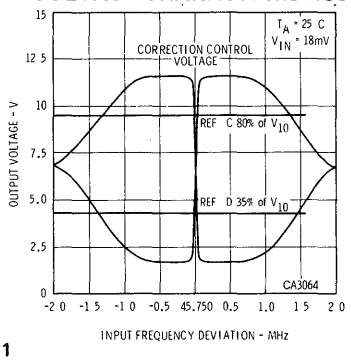
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Power Consumption	T_A = + 25°C	130	140	150	mW
	T_A = -25°C		135	150	mW
	T_A = + 85°C		145	150	mW
Supply Current – I^+	V^+ = + 10.5 V	4.0	6.5	9.5	mA
Regulated Supply Voltage – V^+		10.9	11.8	12.8	V
Quiescent Operating Current – I_2		1.0	2.0	4.0	mA
Quiescent Operating Voltages – V_4, V_5		5.0	6.9	8.0	V
Output Offset Voltage – (V_4 –V_5)		–1.0	0	1.0	V
Input Admittance – Y_{11}	f = 45.75 MHz		0.41 + j 1.0		mmho
Reverse Transfer Admittance – Y_{12}	f = 45.75 MHz		0 + j 3.4		μmho
Forward Transfer Admittance – Y_{21}	f = 45.75 MHz		24.5 -j 29		mmho
Output Admittance – Y_{22}	f = 45.75 MHz		0.04 + j 0.9		mmho
Correction Control Voltage – V_4 (Test Circuit 1)	V_{IN} = 18 mV RMS				
	f_o = 45.750 MHz				
	Δf as listed (MHz)				
	-0.030	85			% V^+
	+ 0.030			25	% V^+
	-0.900	80			% V^+
	+ 0.900			35	% V^+
	-1.500			80	% V^+
	+ 1.500	35			% V^+
Correction Control Voltage – V_5 (Test Circuit 1)	V_{IN} = 18 mV RMS				
	f_o = 45.750 MHz				
	Δf as listed (MHz)				
	-0.030			25	% V^+
	+ 0.030	85			% V^+
	-0.900			35	% V^+
	+ 0.900	80			% V^+
	-1.500	35			% V^+
	+ 1.500			80	% V^+

TYPICAL PERFORMANCE CURVES

NARROW-BAND DYNAMIC CONTROL VOLTAGE CHARACTERISTICS

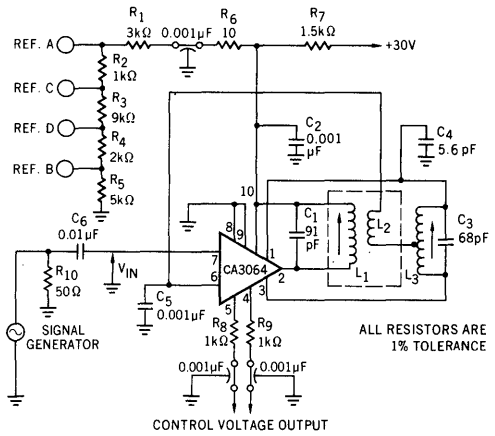


WIDE-BAND DYNAMIC CONTROL VOLTAGE CHARACTERISTICS



SEE TEST CIRCUIT 1

TEST CIRCUIT 1
CORRECTION VOLTAGES



NOTE: Parts placement is cricital. Use P.C. board layout on last page for best results.

L_1 is aligned for symmetrical bandwidth on either side of 45.750 MHz.

L_2 tertiary winding wound on L_1 coil form

L_3 is aligned for zero differential output between terminals 4 and 5 at f_o = 45.750 MHz

REFERENCE VOLTAGE PERCENTAGES

Ref. A	85% of V_{10}
Ref. B	25% of V_{10}
Ref. C	80% of V_{10}
Ref. D	35% of V_{10}

COIL DATA FOR DISCRIMINATOR WINDINGS

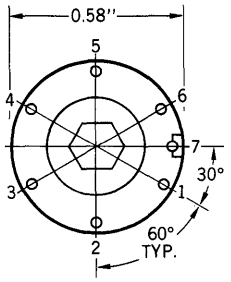
L_1 – Discriminator Primary: 3 1/6 turns; #20 Enamel-covered wire–close-wound, at bottom of coil form. Inductance of L_1 = 0.165 μH; Q_o = 120 at f_o = 45.75 MHz.
Start winding at Terminal #6; finish at Terminal #1. See Notes below.

L_2 – Tertiary Windings: 2 1/6 turns; #20 Enamel-covered wire–close wound over bottom end of L_1. Start winding at Terminal #3; finish at Terminal #4. See Notes below.

L_3 – Discriminator Secondary: 3 1/2 turns; center-tapped, space wound at bottom of coil form. Inductance of L_3 = 0.180 μH; Q_o = 150 at f_o =45.75 MHz.
Start winding at Terminal #2; finish at Terminal #5, connect center tap to Terminal #7. See Notes below.

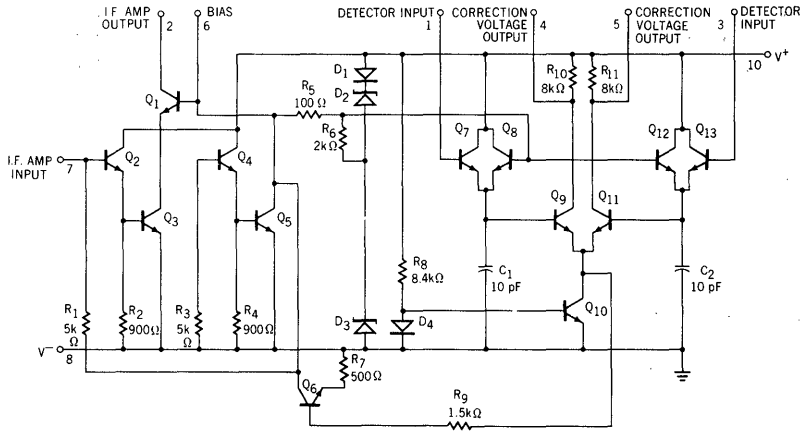
Notes:
1. Coil Forms; Cylindrical; 0.30" Dia. max.
2. Tuning Core: 0.250" Dia. x 0.37" Length.
   : Material: Carbinal J or equivalent.
3. Coil Form Base: See drawing below.
4. End of coil nearest terminal board to be designated the winding start end.

COIL FORM BASE TERMINAL DIAGRAM



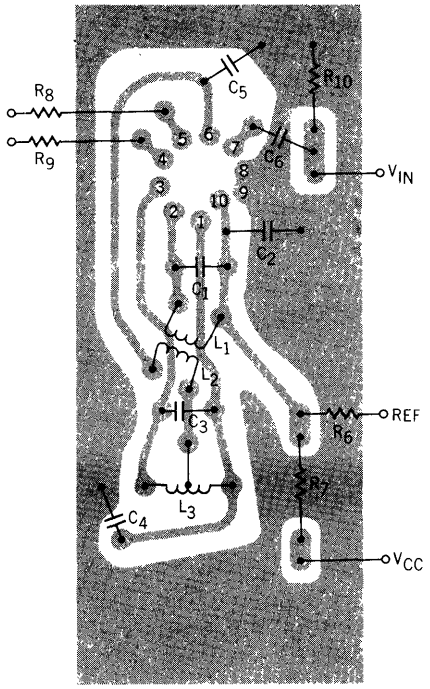
Coil	RCA Distributor Part No.
(L_1, L_2)	122 213
L_3	122 203

CA3064 EQUIVALENT CIRCUIT



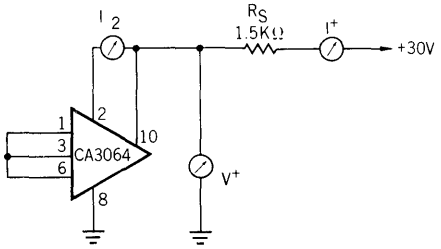
PRINTED CIRCUIT BOARD FOR CORRECTION VOLTAGE TEST CIRCUIT

Full Size Bottom View



TEST CIRCUIT 2

Regulated Voltage, Total Supply Current and Quiescent Current at Terminal 2



CA3065

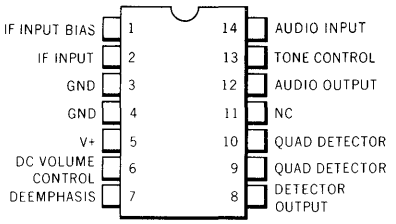
TV/FM SOUND SYSTEM

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The CA3065 Monolithic TV/FM Sound System consists of a Multistage Limiting IF Amplifier, DC Gain (Volume) control, FM Detector, and an Audio Driver constructed on a single silicon chip using the Fairchild planar* epitaxial process. Excellent sensitivity, high AM rejection and an internally regulated power supply coupled with low external component requirement makes the CA3065 suitable for a wide variety of applications including TV Sound Channels, Line Operated and Automobile FM Radios and Mobile Communications Equipment.

- **DC VOLUME CONTROL ELIMINATES NEED FOR SHIELDED CABLES**
- **EXCELLENT AM REJECTION -50dB TYPICAL AT 4.5 MHz**
- **DIFFERENTIAL PEAK DETECTOR REQUIRES ONLY ONE SINGLE-TUNED COIL**
- **INTERNAL ZENER DIODE REGULATED SUPPLY**
- **LOW HARMONIC DISTORTION**

CONNECTION DIAGRAM
(TOP VIEW)



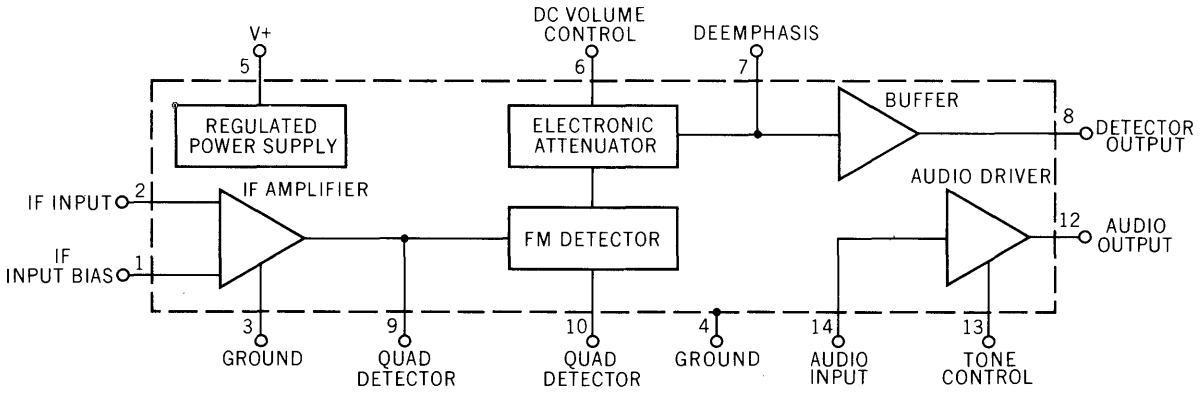
ORDER PART NO: CA3065

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	Note 1
Internal Power Dissipation (Note 2)	670 mW
Power Supply Current	50 mA
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to + 150° C
Lead Temperature Range (Soldering, 60 seconds)	300°C

NOTES
1. V^+ terminal may be connected to any positive voltage through a suitable dropping resistor, provided the dissipation rating is not exceeded.
2. Rating applies to ambient temperature up to 70° C. Above 70° C ambient derate linearly 8.3 mW/° C for the Ceramic DIP.

BLOCK DIAGRAM



*Planar is a patented Fairchild process

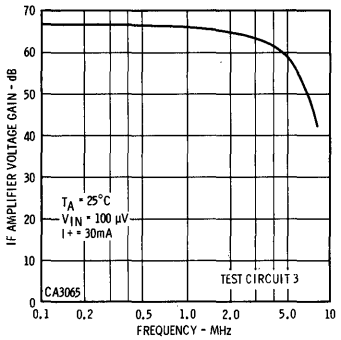
ELECTRICAL CHARACTERISTICS (T_A = 25°C, I^+ = 30 mA unless otherwise specified)

PARAMETER	CONDITIONS	TEST CIRCUIT	MIN	TYP	MAX	UNITS
STATIC CHARACTERISTICS						
Zener Regulating Voltage (V_5)			10.3	11.2	12.2	Volts
Supply Current (I_5)	V_{Supply} = 9.0V		10	16	24	mA
Internal Power Dissipation	I^+ = 33mA		343	370	400	mW
Voltage at IF Input Bias (V_1)				2.0		Volts
Voltage at DC Volume Control (V_6)				4.8		Volts
Voltage at De Emphasis (V_7)				6.1		Volts
Voltage at Quad Detector (V_9)				3.7		Volts
Voltage at Audio Output (V_{12})			4.0	5.1	5.8	Volts
DYNAMIC CHARACTERISTICS						
IF AMPLIFIER	(f_o = 4.5 MHz, FM±25KHz at 400 Hz, V_{IN} = 100μV)	1				
Input Limiting Voltage at -3dB point				200	400	μV
AM Rejection	AM = 30% at 4.5 MHz	1	40	50		dB
IF Transconductance	f = 4.5 MHz					
Magnitude				500		mmho
Phase Angle				46		degrees
Feedback Capacitance	f = 1.0 MHz, Pin 2 to Pin 9			<0.02		pF
Input Impedance Components	f = 4.5 MHz, Pin 1 to Pin 2					
Parallel Input Resistance				17		kΩ
Parallel Input Capacitance				4.0		pF
Output Impedance Components	f = 4.5 MHz, Pin 9 to Ground					
Parallel Output Resistance				3.25		kΩ
Parallel Output Capacitance				75		pF
DETECTOR	(f_o = 4.5 MHz, FM= ±25kHz at 400 Hz, V_{IN} = 100 mV)					
Recovered AF Voltage		1	0.5	0.75		Vrms
Total Harmonic Distortion		1		0.9	2.0	%
Output Resistance						
De emphasis Output				7.5		kΩ
Detector Output				300		Ω
ATTENUATOR						
Max. Attenuation	$R_x = \infty$	1	60	80		dB
Max. Play-through Voltage*	$R_x = \infty$	1		0.075	1.0	mV
AUDIO AMPLIFIER						
Voltage Gain	V_1 = 0.1 Vrms, f = 400 Hz	2	17.5	20		dB
Total Harmonic Distortion	V_0 = 2 Vrms, f = 400 Hz	2		1.5		%
Undistorted Output Voltage	THD = 5%, f = 400 Hz	2	2.0	2.5		Vrms
Input Resistance	f = 400 Hz			70		kΩ
Output Resistance	f = 400 Hz			270		Ω

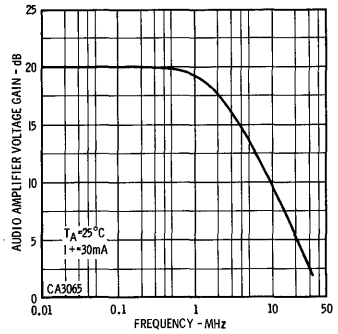
*Play-through voltage is the unwanted signal, measured at the detector output, when the volume control is set for minimum output.

TYPICAL PERFORMANCE CURVES

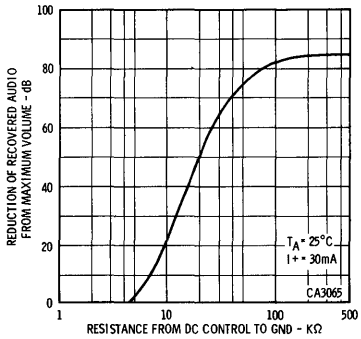
FREQUENCY RESPONSE OF IF AMPLIFIER SECTION



FREQUENCY RESPONSE OF AUDIO AMPLIFIER SECTION



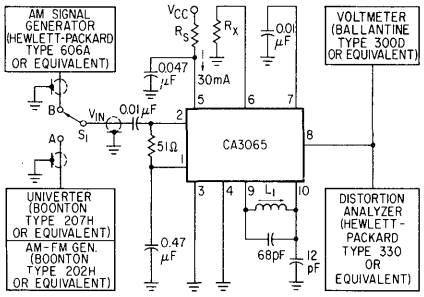
AUDIO GAIN REDUCTION VERSUS DC VOLUME CONTROL RESISTANCE



TEST CIRCUITS

TEST CIRCUIT 1

INPUT LIMITING VOLTAGE, AM REJECTION, RECOVERED AUDIO, TOTAL HARMONIC DISTORTION, MAXIMUM ATTENUATION, MAXIMUM "PLAY-THROUGH" TEST CIRCUIT.



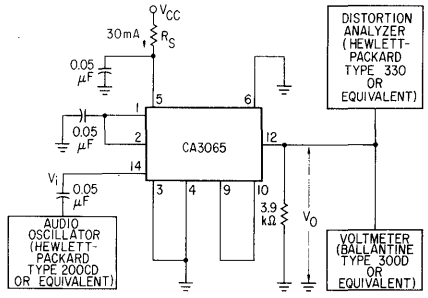
PINS 11, 12, 13, 14 NO CONNECTION

*L_1 = 16μH NOMINAL

$Q_{(UNLOADED)}$ = 50

TEST CIRCUIT 2

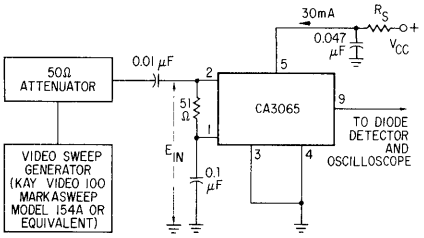
AUDIO VOLTAGE GAIN (UNDISTORTED OUTPUT)



PINS 7, 8, 11, 13 NO CONNECTION

TEST CIRCUIT 3

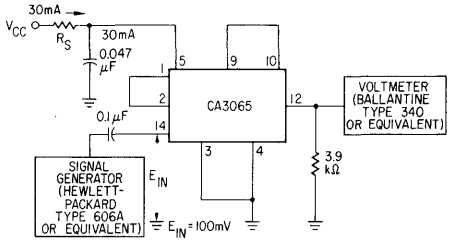
IF AMPLIFIER SECTION



E_{IN} = 100μVrms

TEST CIRCUIT 4

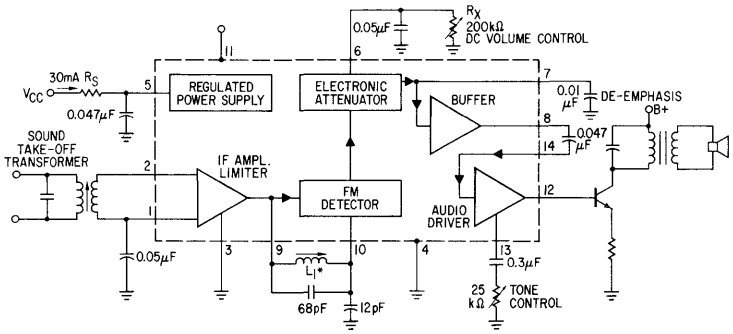
AUDIO AMPLIFIER SECTION



E_{IN} = 100 mV

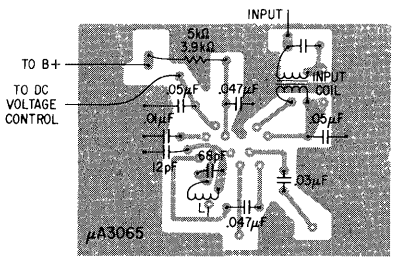
TYPICAL APPLICATION

TV SOUND SYSTEM



*L_1 = 16μH NOMINAL , $Q_{(UNLOADED)}$ = 50

SUGGESTED CIRCUIT LAYOUT COMPONENT SIDE



LM101A • LM201A • LM301A

GENERAL PURPOSE OPERATIONAL AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

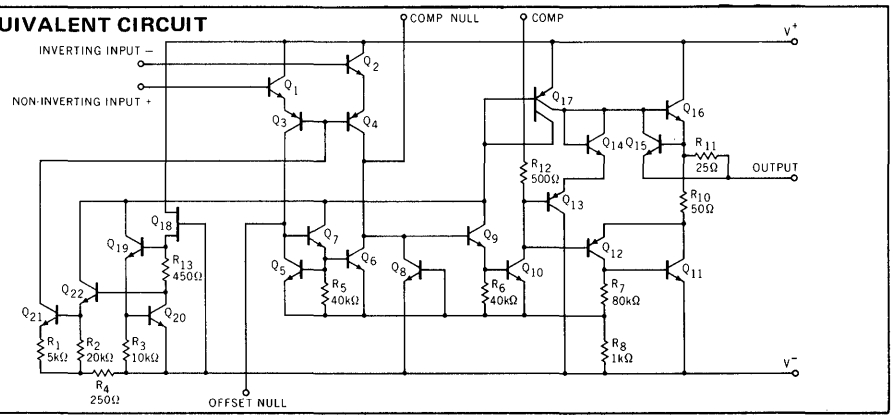
GENERAL DESCRIPTION — The LM101A, LM201A and LM301A are general purpose monolithic operational amplifiers constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. These integrated circuits are intended for applications requiring low input offset voltage or low input offset current. The accuracy of long interval integrators, timers and sample and hold circuits is improved due to the low drift and low bias currents of the LM101A, LM201A, or LM301A. Frequency response may be matched to the individual circuit need with one external capacitor. The absence of "Latch-Up" coupled with internal short circuit protection make the LM101A, LM201A and LM301A virtually foolproof. The LM101A, LM201A and LM301A are pin compatible with the popular μA709, μA741, μA748 and μA777.

- **LOW OFFSET CURRENT AND VOLTAGE**
- **LOW OFFSET CURRENT DRIFT**
- **LOW BIAS CURRENT**
- **SHORT CIRCUIT PROTECTED**
- **LOW POWER CONSUMPTION**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
Military and Instrument (LM101A and LM201A)	±22 V
Commercial (LM301A)	±18 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
Ceramic DIP	670 mW
Silicone DIP	340 mW
Flatpak	570 mW
Mini DIP	310 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, Ceramic DIP, and Flatpak	-65°C to + 150°C
Mini DIP and Silicon DIP	-55°C to + 125°C
Operating Temperature Range	
Military (LM101A)	-55°C to + 125°C
Instrument (LM201A)	−25°C to + 85°C
Commercial (LM301A)	0°C to + 70°C
Lead Temperature (Soldering)	
Metal Can, Ceramic DIP and Flatpak (60 seconds)	300°C
Mini DIP and Silicone DIP (10 seconds)	260°C
Output Short Circuit Duration (Note 3)	Indefinite

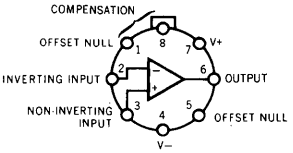
EQUIVALENT CIRCUIT



Notes on following pages.

CONNECTION DIAGRAMS
(TOP VIEW)

8 LEAD METAL CAN

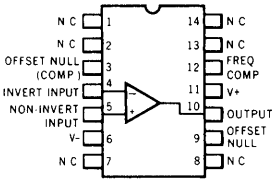


NOTE: PIN 4 CONNECTED TO CASE.

ORDER PART NOS.

LM101AH
LM201AH
LM301AH

14 LEAD DIP



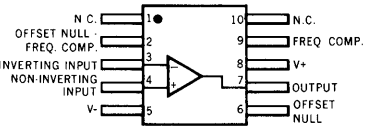
FOR CERAMIC DIP ORDER PART NOS.

LM101AD
LM201AD
LM301AD

FOR SILICONE DIP ORDER PART NO.

LM301AP

FLATPACK

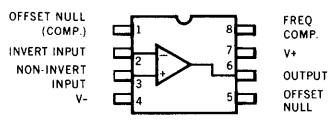


ORDER PART NOS.

LM101AF*
LM201AF*

*Available on special request

MINIDIP



ORDER PART NO.

LM301AN

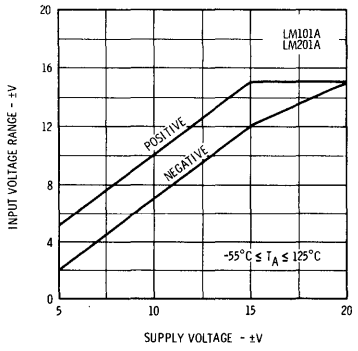
*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS FOR LM101A and LM201A ($\pm 5.0V \leqslant V_s \leqslant \pm 20V$, $T_A = 25°C$, $C_1 = 30$ pF unless otherwise specified)

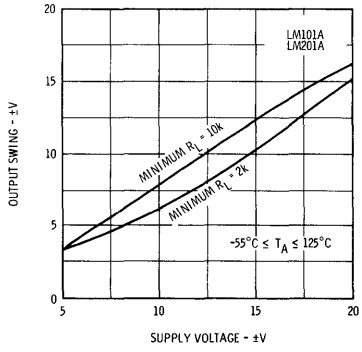
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_s \leqslant 50\ k\Omega$		0.7	2.0	mV
Input Offset Current			1.5	10	nA
Input Bias Current			30	75	nA
Input Resistance		1.5	4.0		M Ω
Supply Current	$V_s = \pm 20V$		1.8	3.0	mA
Large Signal Voltage Gain	$V_s = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geqslant 2\ k\Omega$	50	160		V/mV
The following specifications apply for $-55°C \leqslant T_A \leqslant +125°C$: (Note 4)					
Input Offset Voltage	$R_s \leqslant 50\ k\Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15	μV/°C
Input Offset Current				20	nA
Average Temperature Coefficient of Input Offset Current	$+25°C \leqslant T_A \leqslant +125°C$ $-55°C \leqslant T_A \leqslant +25°C$		0.01 0.02	0.1 0.2	nA/°C nA/°C
Input Bias Current				100	nA
Supply Current	$T_A = +125°C$, $V_s = \pm 20V$		1.2	2.5	mA
Large Signal Voltage Gain	$V_s = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geqslant 2\ k\Omega$	25			V/mV
Output Voltage Swing	$V_s = \pm 15V$, $R_L = 10\ k\Omega$ $R_L = 2\ k\Omega$	±12 ±10	±14 ±13		V V
Input Voltage Range	$V_s = \pm 20V$	±15			V
Common Mode Rejection Ratio	$R_s \leqslant 50\ k\Omega$	80	96		dB
Supply Voltage Rejection Ratio	$R_s \leqslant 50\ k\Omega$	80	96		dB

GUARANTEED PERFORMANCE CURVES (LM101A AND LM201A)

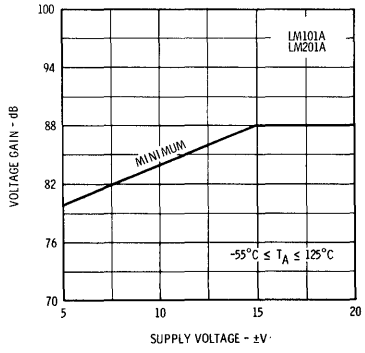
INPUT VOLTAGE RANGE VS. SUPPLY



OUTPUT SWING VS. SUPPLY



VOLTAGE GAIN VS. SUPPLY



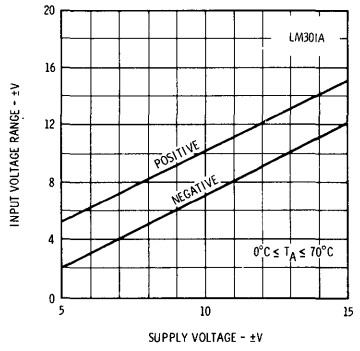
ELECTRICAL CHARACTERISTICS FOR LM301A ($\pm 5.0\,V \leq V_S \leq \pm 15V$, $T_A = 25°C$, $C_1 = 30\,pF$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 50\,k\Omega$		2.0	7.5	mV
Input Offset Current			3	50	nA
Input Bias Current			70	250	nA
Input Resistance		0.5	2		MΩ
Supply Current	$V_S = \pm 15V$		1.8	3.0	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2\,k\Omega$	25	160		V/mV
The following specifications apply for $0°C \leq T_A \leq 70°C$:					
Input Offset Voltage	$R_S \leq 50\,k\Omega$			10	mV
Average Temperature Coefficient of Input Offset Voltage			6.0	30	μV/°C
Input Offset Current				70	nA
Average Temperature Coefficient of Input	$25°C \leq T_A \leq 70°C$		0.01	0.3	nA/°C
	$0°C \leq T_A \leq 25°C$		0.02	0.6	nA/°C
Input Bias Current				300	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2\,k\Omega$	15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\,k\Omega$	±12	±14		V
	$R_L = 2\,k\Omega$	±10	±13		V
Input Voltage Range	$V_S = \pm 15V$	±12			V
Common Mode Rejection Ratio	$R_S \leq 50\,k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\,k\Omega$	70	96		dB

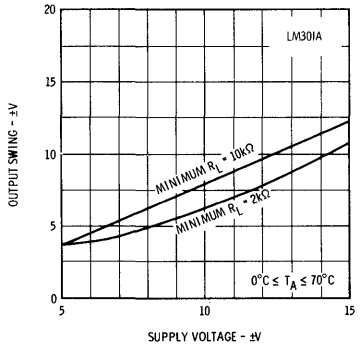
NOTES:
(1) Rating applies to ambient temperature up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for the Metal Can, 8.3 mW/°C for the Ceramic DIP, 6.3 mW/°C for the Silicone DIP, 5.6 mW/°C for the Mini DIP and 7.1 mW/°C for the Flatpak.
(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
(3) Short circuit may be to ground or either supply. LM101A and LM201A ratings apply to +125°C case temperature or +75°C ambient temperature. LM301A ratings apply for case temperatures to 70°C.
(4) All LM201A specifications apply for $-25°C \leq T_A \leq +85°C$ unless otherwise specified.

GUARANTEED PERFORMANCE CURVES (LM301A)

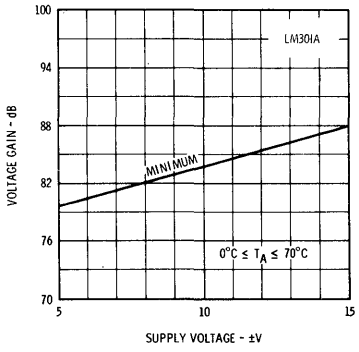
INPUT VOLTAGE RANGE VS. SUPPLY



OUTPUT SWING VS. SUPPLY

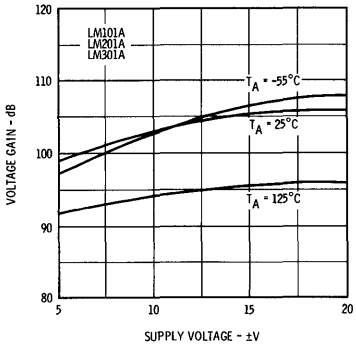


VOLTAGE GAIN VS. SUPPLY

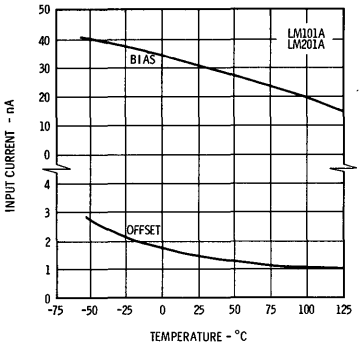


TYPICAL PERFORMANCE CURVES

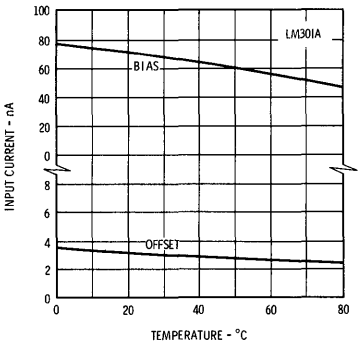
VOLTAGE GAIN



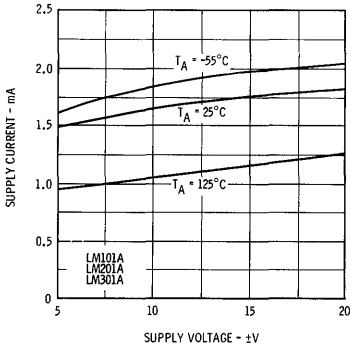
INPUT CURRENT (LM101A AND LM201A)



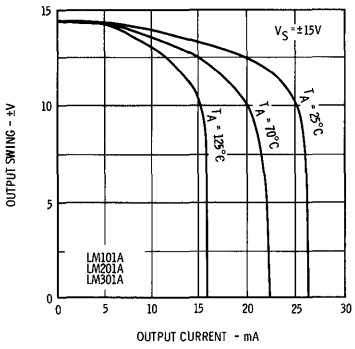
INPUT CURRENT (LM301A)



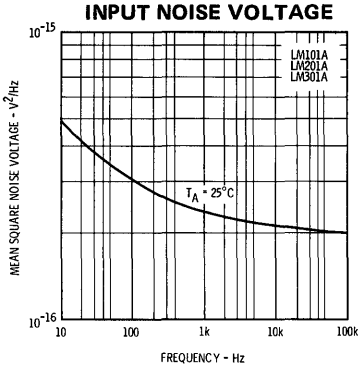
SUPPLY CURRENT



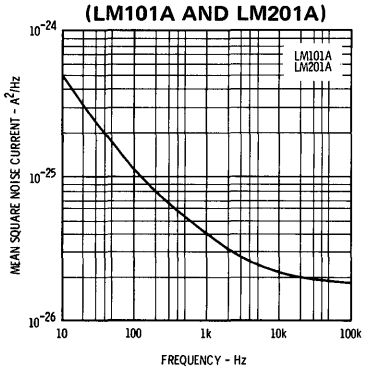
CURRENT LIMITING



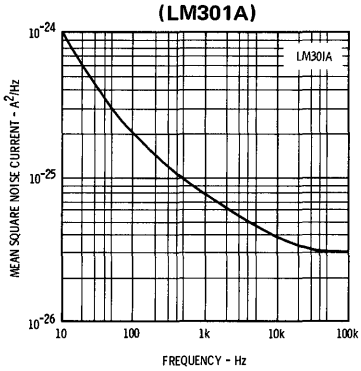
INPUT NOISE VOLTAGE



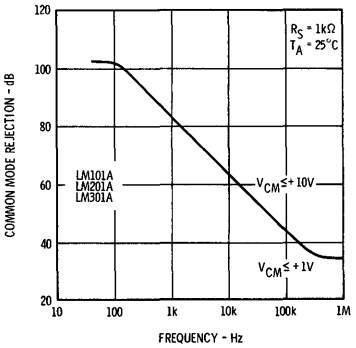
INPUT NOISE CURRENT (LM101A AND LM201A)



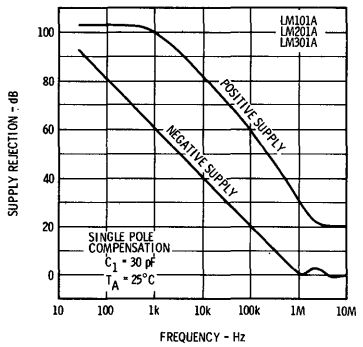
INPUT NOISE CURRENT (LM301A)



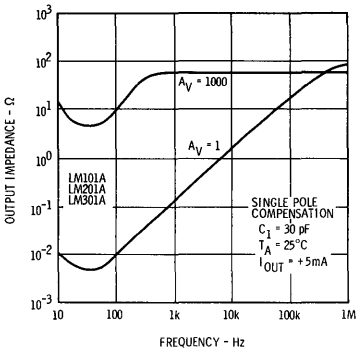
COMMON MODE REJECTION



POWER SUPPLY REJECTION

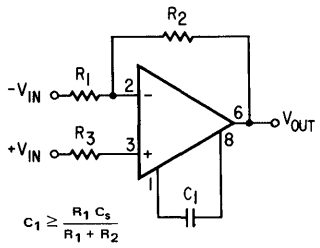


CLOSED LOOP OUTPUT IMPEDANCE

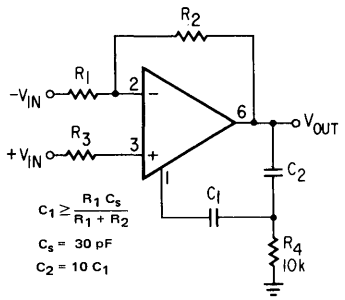


COMPENSATION CIRCUITS

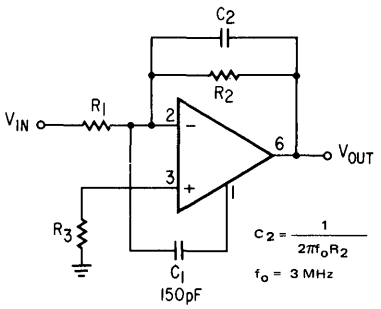
SINGLE POLE COMPENSATION



TWO POLE COMPENSATION

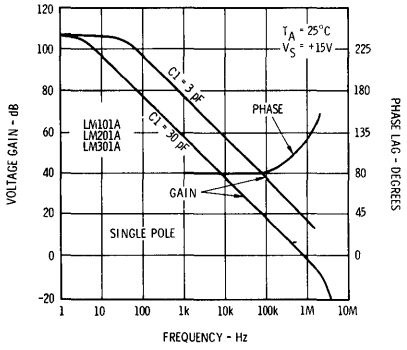


FEEDFORWARD COMPENSATION

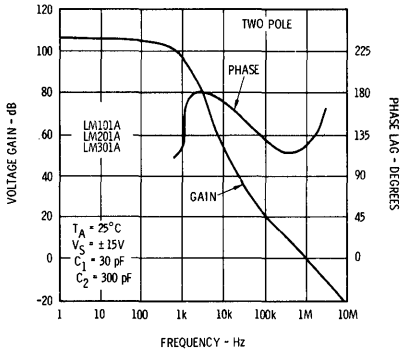


TYPICAL PERFORMANCE CURVES

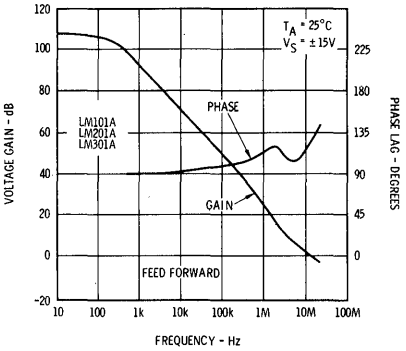
OPEN LOOP FREQUENCY RESPONSE



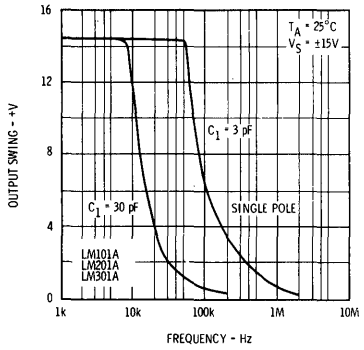
OPEN LOOP FREQUENCY RESPONSE



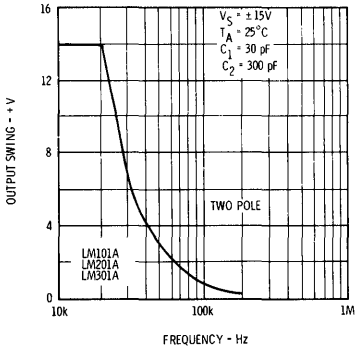
OPEN LOOP FREQUENCY RESPONSE



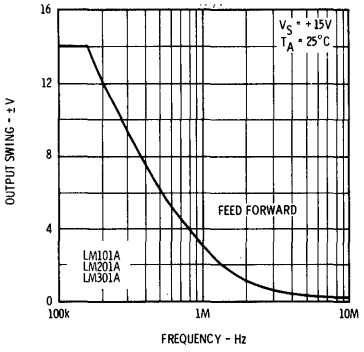
LARGE SIGNAL FREQUENCY RESPONSE



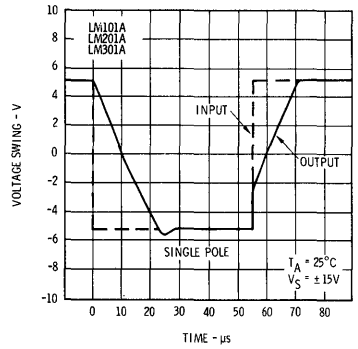
LARGE SIGNAL FREQUENCY RESPONSE



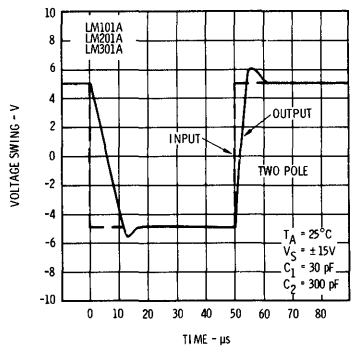
LARGE SIGNAL FREQUENCY RESPONSE



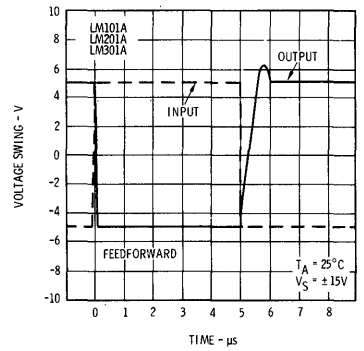
VOLTAGE FOLLOWER PULSE RESPONSE



VOLTAGE FOLLOWER PULSE RESPONSE



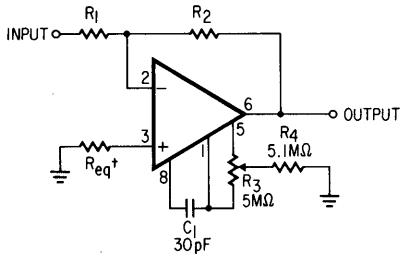
INVERTER PULSE RESPONSE



TYPICAL APPLICATIONS

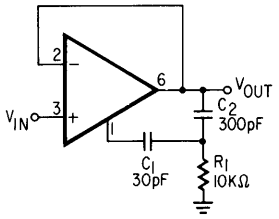
(All pin numbers shown refer to 8 pin TO-5 package)

INVERTING AMPLIFIER –WITH BALANCING CIRCUIT



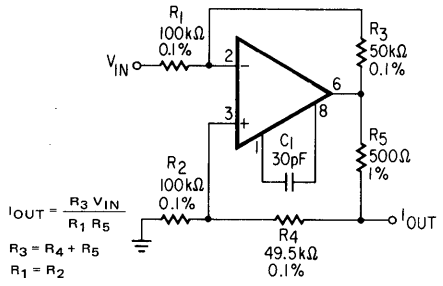
† May be zero or equal to parallel combination of R1 and R2 for minimum offset.

FAST VOLTAGE FOLLOWER



Power Bandwidth: 15 kHz
Slew Rate: 1V/μs

BILATERAL CURRENT SOURCE

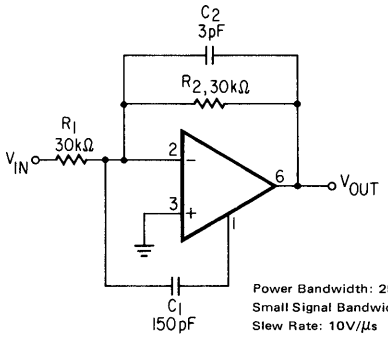


$I_{OUT} = \frac{R_3 V_{IN}}{R_1 R_5}$

$R_3 = R_4 + R_5$

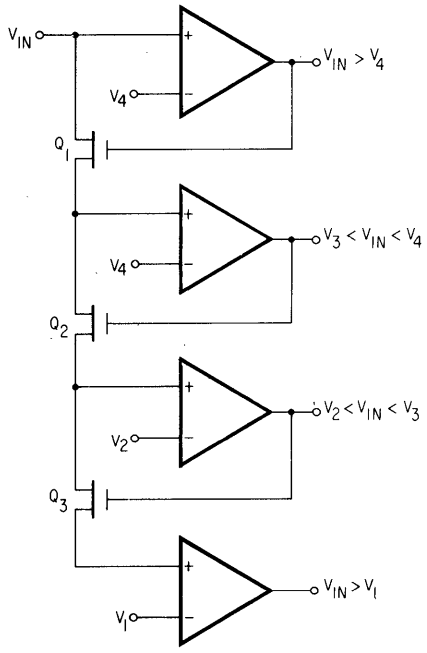
$R_1 = R_2$

FAST SUMMING AMPLIFIER

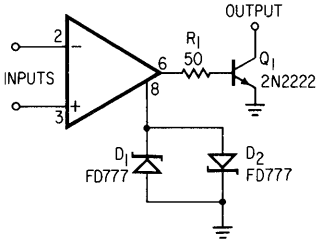


Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10V/μs

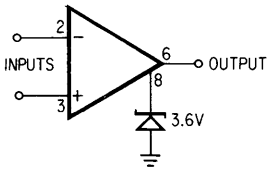
MULTIPLE APERTURE WINDOW DISCRIMINATOR



VOLTAGE COMPARATOR FOR DRIVING RTL LOGIC OR HIGH CURRENT DRIVER



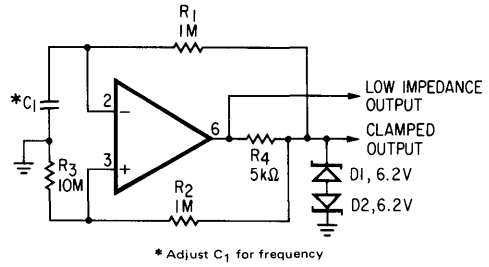
VOLTAGE COMPARATOR FOR DRIVING DTL OR TTL INTEGRATED CIRCUITS



TYPICAL APPLICATIONS (CON'D)

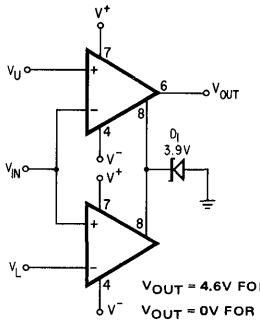
(All pin numbers shown refer to 8 pin TO-5 package)

LOW FREQUENCY SQUARE WAVE GENERATOR



* Adjust C_1 for frequency

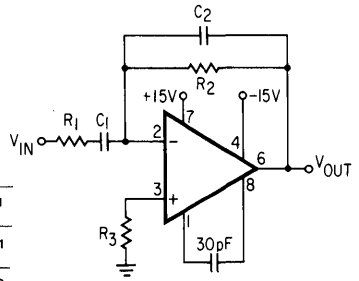
DOUBLE ENDED LIMIT DETECTOR



V_{OUT} = 4.6V FOR $V_L \leq V_{IN} \leq V_U$

V_{OUT} = 0V FOR $V_{IN} < V_L$ OR $V_{IN} < V_U$

PRACTICAL DIFFERENTIATOR

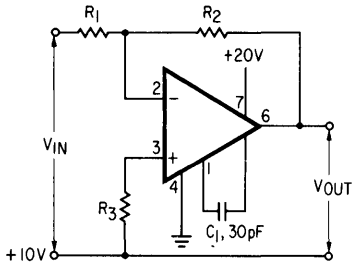


$$f_c = \frac{1}{2\pi R_2 C_1}$$

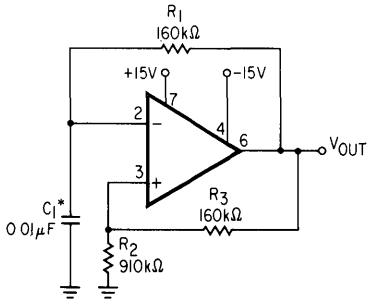
$$f_h = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_2 C_2}$$

$f_c < f_h < f_{unity\ gain}$

CIRCUIT FOR OPERATING WITHOUT A NEGATIVE SUPPLY

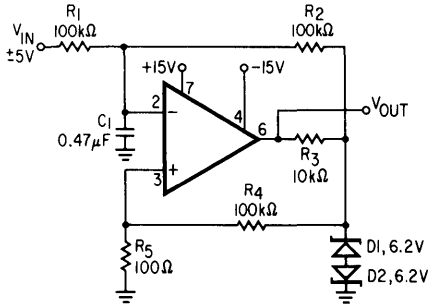


FREE-RUNNING MULTIVIBRATOR

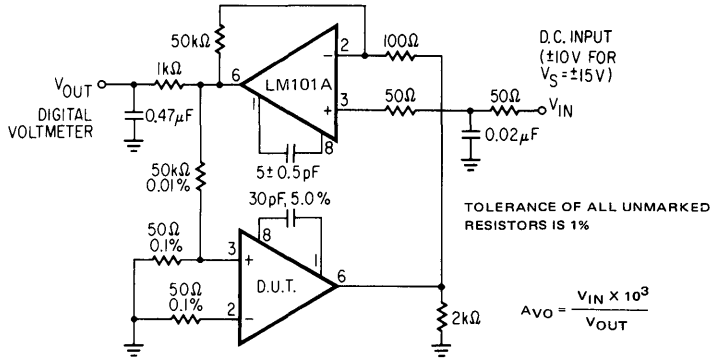


*Chosen for oscillation at 100 Hz

PULSE WIDTH MODULATOR



GAIN TEST CIRCUIT



TOLERANCE OF ALL UNMARKED RESISTORS IS 1%

$$A_{VO} = \frac{V_{IN} \times 10^3}{V_{OUT}}$$

LM109•LM209•LM309

5 VOLT REGULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The LM109, LM209 and LM309 are complete 5 volt regulators constructed on a single silicon chip using the Fairchild Planar* epitaxial process. These regulators employ internal current limiting, thermal shutdown and safe-area compensation making them essentially blow-out proof. They are intended for use as local regulators, eliminating noise and distribution problems associated with single point regulation. If adequate heat sinking is provided, they can provide over 1 A. The LM109, LM209 and LM309 are intended primarily for use with TTL and DTL logic and are completely specified under worst case conditions to match the power supply requirements of these logic families. In addition to use as a fixed 5 volt regulator, these devices can be used with external components to obtain adjustable output voltages and currents and as the power pass element in precision regulators.

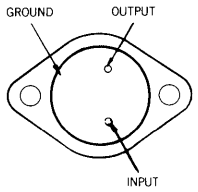
- **OUTPUT CURRENT IN EXCESS OF 1 AMP**
- **SPECIFIED TO MATCH WORST CASE TTL AND DTL REQUIREMENTS**
- **NO EXTERNAL COMPONENTS**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **OUTPUT TRANSISTOR SAFE-AREA COMPENSATION**

ABSOLUTE MAXIMUM RATINGS

Input Voltage	35 V
Internal Power Dissipation	Internally Limited
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	
LM109	−55°C to +150°C
LM209	−25°C to +150°C
LM309	0°C to +125°C
Lead Temperature (Soldering, 60 second time limit)	300°C

CONNECTION DIAGRAM

TO-3 PACKAGE
(TOP VIEW)

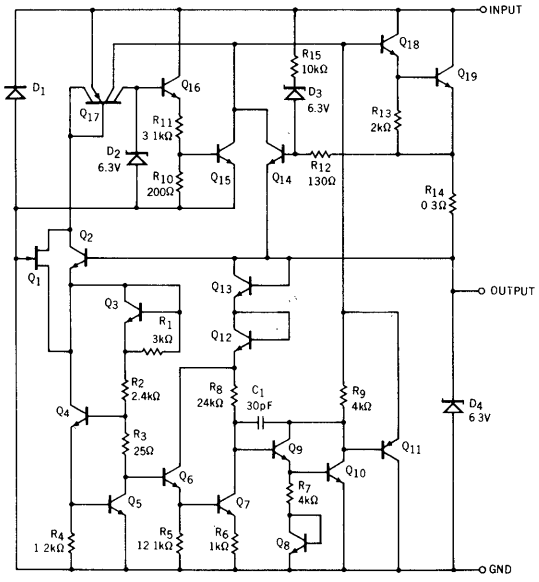


Case is connected to ground.

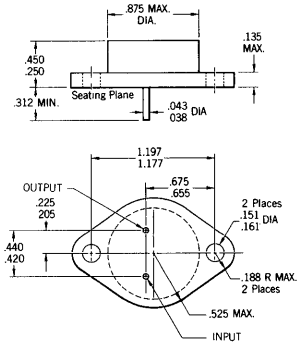
ORDER PART NO:

LM109K
LM209K
LM309K

EQUIVALENT CIRCUIT



PHYSCIAL DIMENSIONS
TO-3 PACKAGE



NOTES
All dimensions in inches
Leads 1 and 2 electrically isolated from case
Case is third electrical connection
Leads are gold-plated copper cored kovar
Package weight is 7.4 grams.

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS FOR LM109 AND LM209 (Note 1)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_j = 25°C$	4.7	5.05	5.3	V
Line Regulation	$T_j = 25°C$				
	$7\ V \leqslant V_{IN} \leqslant 25\ V$		4.0	50	mV
Load Regulation	$T_j = 25°C$				
	$5\ mA \leqslant I_{OUT} \leqslant 1.5\ A$		50	100	mV
Output Voltage	$7\ V \leqslant V_{IN} \leqslant 25\ V$				
	$5\ mA \leqslant I_{OUT} \leqslant I_{MAX}$				
	$P \leqslant P_{MAX}$	4.6		5.4	V
Quiescent Current	$7\ V \leqslant V_{IN} \leqslant 25\ V$		5.2	10	mA
Quiescent Current Change	$7\ V \leqslant V_{IN} \leqslant 25\ V$			0.5	mA
	$5\ mA \leqslant I_{OUT} \leqslant I_{MAX}$			0.8	mA
Output Noise Voltage	$T_A = 25°C$				
	$10\ Hz \leqslant f \leqslant 100\ kHz$		40		μV
Long Term Stability				10	mV
Thermal Resistance					
Junction to Case (Note 2)			3.0		°C/W

ELECTRICAL CHARACTERISTICS FOR LM309 (Note 3)

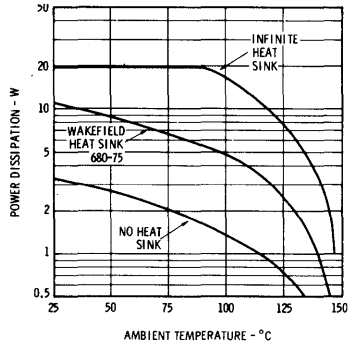
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Voltage	$T_j = 25°C$	4.8	5.05	5.2	V
Line Regulation	$T_j = 25°C$				
	$7\ V \leqslant V_{IN} \leqslant 25\ V$		4.0	50	mV
Load Regulation	$T_j = 25°C$				
	$5\ mA \leqslant I_{OUT} \leqslant 1.5\ A$		50	100	mV
Output Voltage	$7\ V \leqslant V_{IN} \leqslant 25\ V$				
	$5\ mA \leqslant I_{OUT} \leqslant I_{MAX}$	4.75		5.25	V
	$P \leqslant P_{MAX}$				
Quiescent Current	$7\ V \leqslant V_{IN} \leqslant 25\ V$		5.2	10	mA
Quiescent Current Change	$7\ V \leqslant V_{IN} \leqslant 25\ V$			0.5	mA
	$5\ mA \leqslant I_{OUT} \leqslant I_{MAX}$			0.8	mA
Output Noise Voltage	$T_A = 25°C$				
	$10\ Hz \leqslant f \leqslant 100\ kHz$		40		μV
Long Term Stability				20	mV
Thermal Resistance					
Junction to Case (Note 2)			3.0		°C/W

NOTES

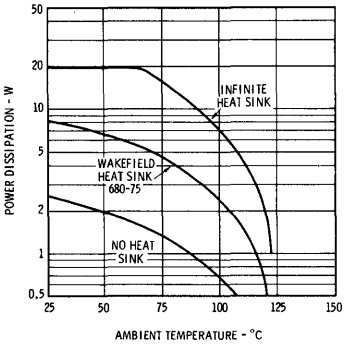
1. Unless otherwise specified, these specifications apply for $-55°C \leqslant T_j \leqslant 150°C$ ($-25°C \leqslant T_j \leqslant 150°C$ for the LM209), $V_{IN} = 10\ V$ and $I_{OUT} = 0.5\ A$.
2. Without a heat sink, the thermal resistance is about 150°C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the sink.
3. Unless otherwise specified, these specifications apply for $0°C \leqslant T_j \leqslant 125°C$, $V_{IN} = 10\ V$ and $I_{OUT} = 0.5\ A$. $I_{MAX} = 1.0\ A$ and $P_{MAX} = 20\ W$.

TYPICAL PERFORMANCE CURVES
(For all grades unless otherwise specified)

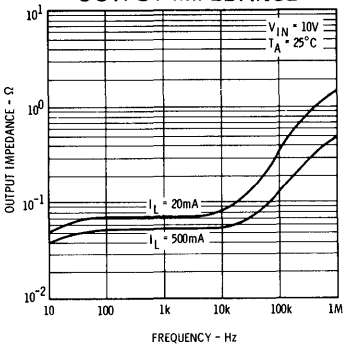
TO–3 MAXIMUM AVERAGE POWER DISSIPATION (LM109 and LM209)



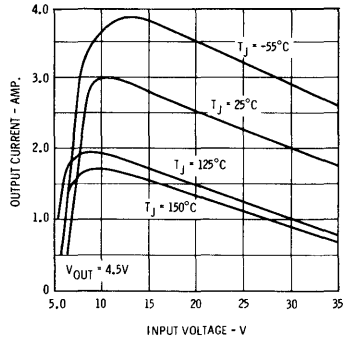
TO–3 MAXIMUM AVERAGE POWER DISSIPATION (LM309)



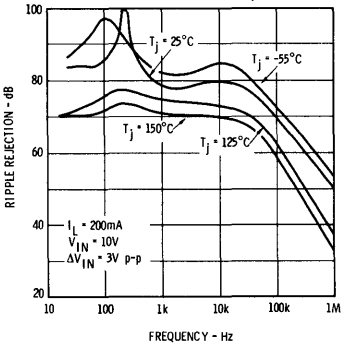
OUTPUT IMPEDANCE



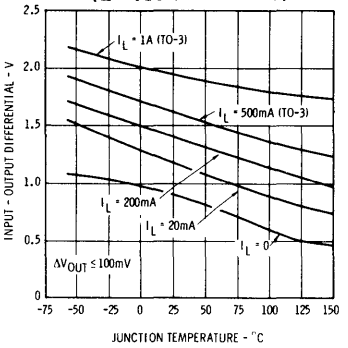
TO–3 PEAK OUTPUT CURRENT



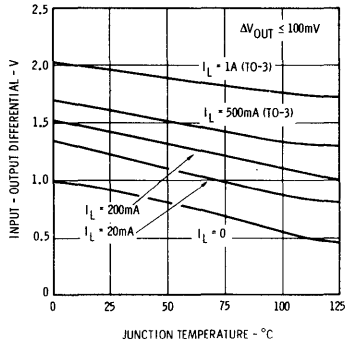
RIPPLE REJECTION



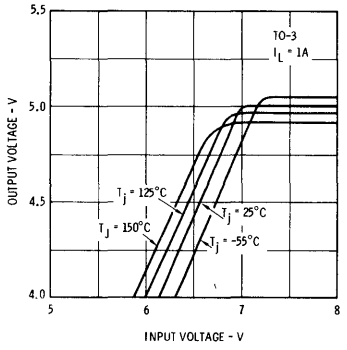
DROPOUT VOLTAGE (LM109 and LM209)



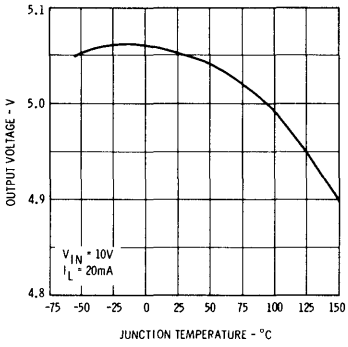
DROPOUT VOLTAGE (LM309)



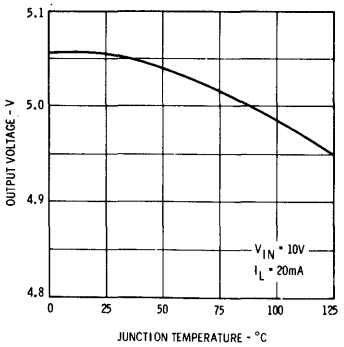
DROPOUT CHARACTERISTIC



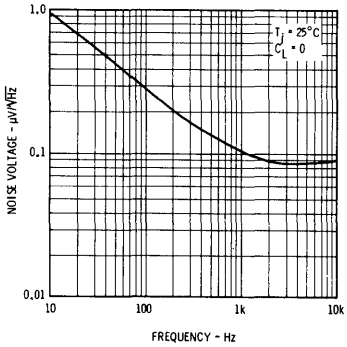
OUTPUT VOLTAGE (LM109 and LM209)



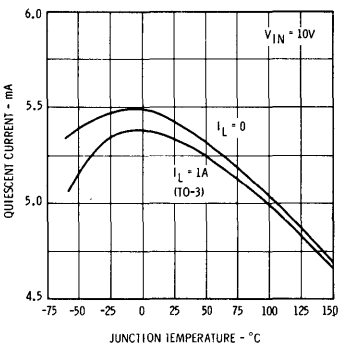
OUTPUT VOLTAGE (LM309)



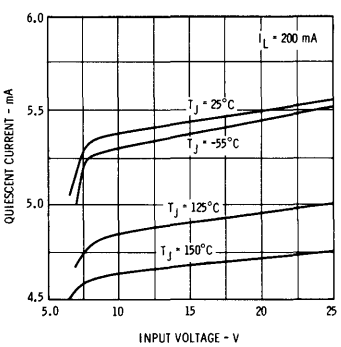
OUTPUT NOISE VOLTAGE



QUIESCENT CURRENT

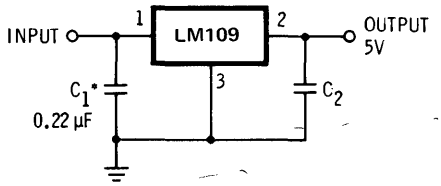


QUIESCENT CURRENT



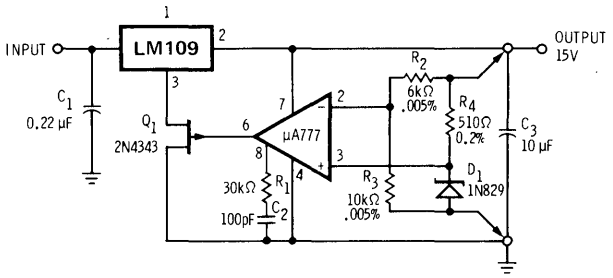
APPLICATIONS

FIXED 5 V REGULATOR



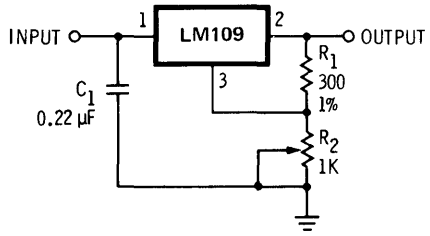
NOTES:
* Required if regulator is located an appreciable distance from power supply filter.
† Although no output capacitor is needed for stability, it does improve transient response.

PRECISION VOLTAGE REGULATOR

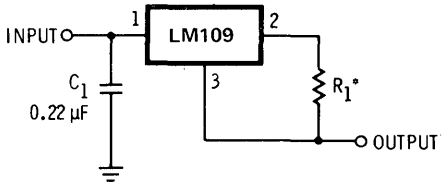


NOTES:
* Regulation better than 0.01% load, line and temperature, can be obtained.
† Determines zener current. May be adjusted to minimize thermal drift.
‡ Solid tantalum.

ADJUSTABLE OUTPUT REGULATOR



CURRENT REGULATOR



NOTES:
* Determines output current.

SN7524 • SN7525

TWO CHANNEL CORE MEMORY SENSE AMPLIFIERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The SN7524 and SN7525 are two channel core memory sense amplifiers constructed on a silicon chip using the patented Fairchild Planar* epitaxial process. They can be used for small (1K to 8K words) memories as well as larger memory systems. The devices are suitable for small core sizes facilitating very fast memory cycle times. The SN7524 and SN7525 feature tight threshold accuracy, fast response time, and independent strobe selection. Unit to unit variations are minimized so that individual adjustments of the threshold and strobe timing are not necessary.

All logic inputs and outputs are fully TTL compatible. The SN7524 and SN7525 can be combined with the Fairchild MSI Quad Latch 9314 to provide complete memory data register capability.

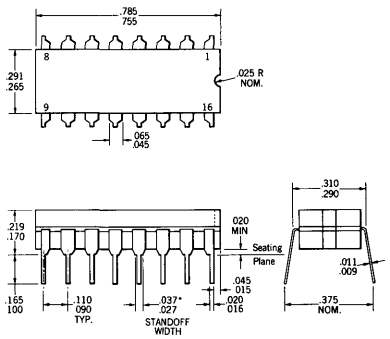
- **±2 mV THRESHOLD VARIATION**
- **25 ns PROPAGATION DELAY**
- **DUAL INDEPENDENT STROBES**
- **TTL COMPATIBLE**

ABSOLUTE MAXIMUM RATINGS

Differential Input Voltage	±5.0 V
Supply Voltage	±7.0 V
Logic Input Voltage	+5.5 V
Power Dissipation	730 mW
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Lead Temperature (Soldering 60 seconds)	+300°C
Signal Input	±3.0 V
Reference Input	±3.0 V

PHYSICAL DIMENSIONS

16 Lead Ceramic Dual In-Line

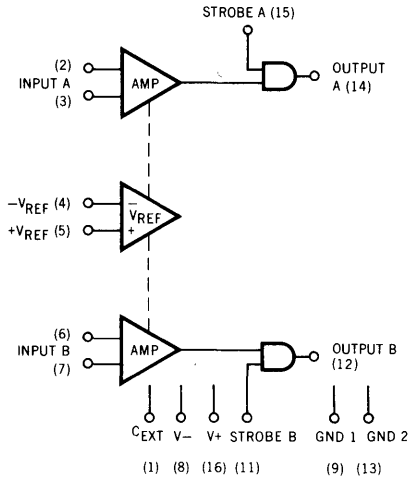


NOTES:
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020" diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
The .037/.027 dimension does not apply to the corner leads

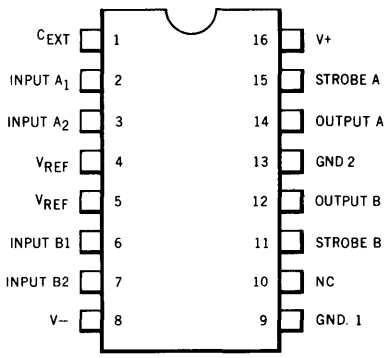
ORDER PART NOS.

SN7524J
SN7525J

BLOCK DIAGRAM



CONNECTION DIAGRAM



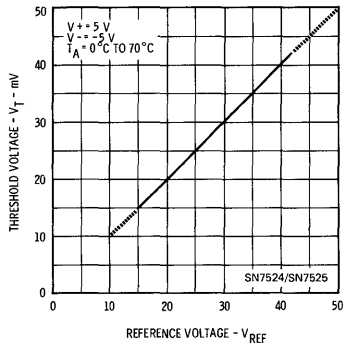
*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (V^+ = 5.0 V, V^- = −5.0 V, 0°C to +70°C either Amplifier unless otherwise specified)

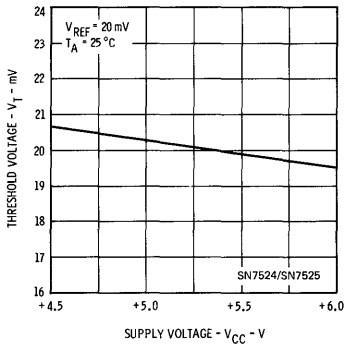
PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
SN7524					
Differential Input Threshold Voltage	V_{ref} = 15 mV	11		19	mV
	V_{ref} = 40 mV	36		44	mV
SN7525					
Differential Input Threshold Voltage	V_{ref} = 15 mV	8.0		22	mV
	V_{ref} = 40 mV	33		47	mV
The following specifications apply to either the SN7524 or the SN7525:					
Threshold Voltage Range					
Minimum			10		mV
Maximum			50		nV
Threshold Uncertainty			±2.0		mV
Differential Input Bias Current	V_{IND} = 0 mV		15	75	μA
Differential Input Offset Current	V_{IND} = 0 mV		1.0		μA
Differential Input Impedance	f = 1.0 kHz		2.5		kΩ
Positive Supply Current	T_A = 25°C, V^+ = 5.25 V, V^- = −5.25 V		25	40	mA
Negative Supply Current	T_A = 25°C, V^+ = 5.25 V, V^- = −5.25 V		10	20	mA
Output Short Circuit Current	V^+ = 5.25 V, V^- = −5.25 V	2.1		3.5	mA
LOGIC INPUT/OUTPUT CONDITIONS (See Fig. 2)					
Output Voltage Logical "1"	1 Load = 400 μA $V_{IN(1)}$ Strobe = 2.0 V $V_{IN(0)}$ Strobe = 0.8 V V^+ = 4.75 V, V^- = −4.75 V	2.4	3.9		V
Output Voltage Logical "0"	I Sink = 16 mA $V_{IN(0)}$ Strobe = 0.8 V V^+ = 4.75 V, V^- = −4.75 V		0.25	0.4	V
Logical "1" Input (Strobe Inputs)	$V_{IN(0)}$ Strobe = 0.8 V V^+ = 4.75 V, V^- = −4.75 V	2.0			V
Logical "0" Input (Strobe Inputs)	$V_{IN(1)}$ Strobe = 2.0 V V^+ = 4.75 V, V^- = −4.75 V			0.8	V
Logical "0" Input Current (Strobe Inputs)	$V_{IN(0)}$ Strobe = 0.4 V V^+ = 5.25 V, V^- = −5.25 V		−1.0	−1.6	mA
Logical "1" Input Current (Strobe Inputs)	$V_{IN(1)}$ Strobe = 2.4 V V^+ = 5.25 V, V^- = −5.25 V			40	μA
Logical "1" Input Current (Strobe Inputs)	$V_{IN(1)}$ Strobe = V^+ V^+ = 5.25 V, V^- = −5.25 V			1.0	mA
A.C. CHARACTERISTICS	T_A = 25°C				
Common Mode Input Firing Voltage	$t_r = t_f \leq 15$ ns t_p = 50 ns		±3.0		V
Differential Input Overload Recovery Time	V_{IN} + 2.0 V, $t_r = t_f$ = 20 ns		20		ns
Common Mode Input Overload Recovery Time	$V_{IN\ CM}$ = ±2.0 V, $t_r = t_f$ = 20 ns		20		ns
Input to Output Delay (See Figure 1)	t_{pd} (1) D		25	40	ns
	t_{pd} (0) D		35		ns
Strobe to Output Delay (See Figure 1)	t_{pd} (1) Strobe		15	30	ns
	t_{pd} (0) Strobe		25		ns

TYPICAL PERFORMANCE CURVES

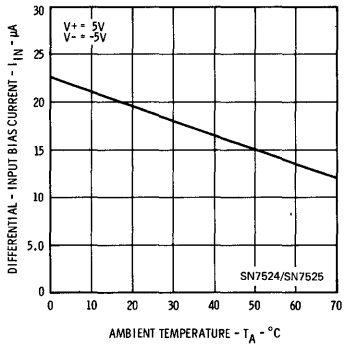
THRESHOLD VOLTAGE VERSUS REFERENCE VOLTAGE



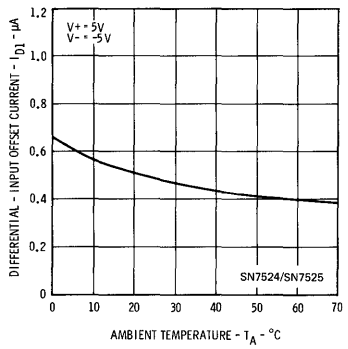
THRESHOLD VOLTAGE VERSUS SUPPLY VOLTAGE



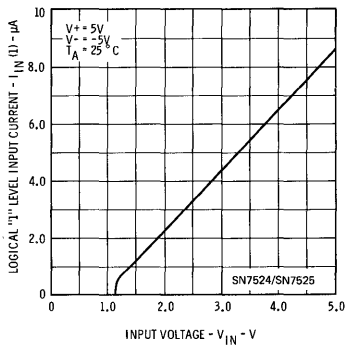
DIFFERENTIAL-INPUT BIAS CURRENT VERSUS AMBIENT TEMPERATURE



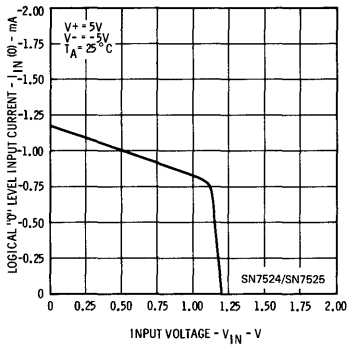
DIFFERENTIAL-INPUT OFFSET CURRENT VERSUS AMBIENT TEMPERATURE



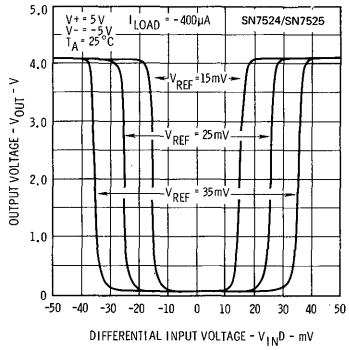
LOGICAL "1" LEVEL INPUT CURRENT VERSUS INPUT VOLTAGE



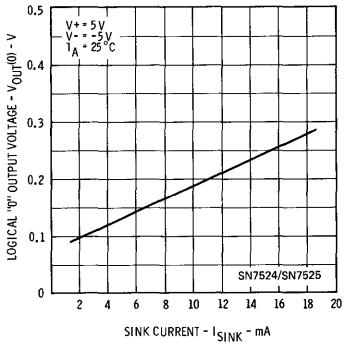
LOGICAL "0" LEVEL INPUT CURRENT VERSUS INPUT VOLTAGE



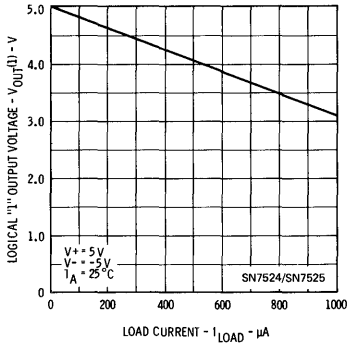
OUTPUT VOLTAGE VERSUS DIFFERENTIAL INPUT VOLTAGE



LOGICAL "0" OUTPUT VOLTAGE VERSUS SINK CURRENT



LOGICAL "1" OUTPUT VOLTAGE VERSUS LOAD CURRENT



COMMON-MODE FIRING VOLTAGE VERSUS AMBIENT TEMPERATURE

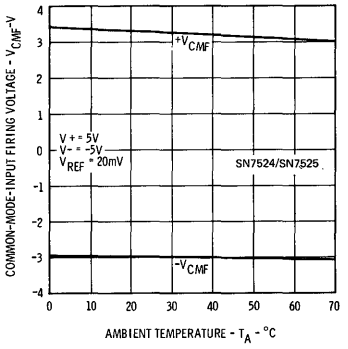
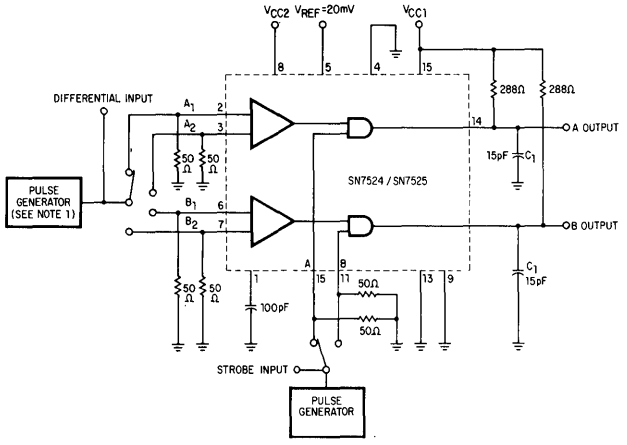
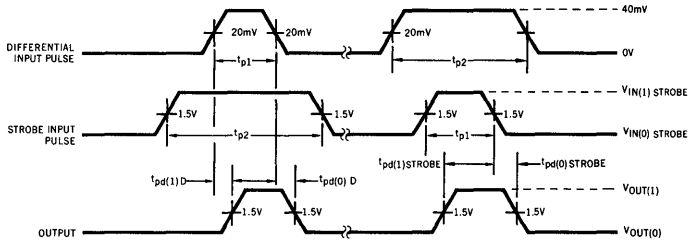


FIG. 1 PROPAGATION DELAY

TEST CIRCUITS



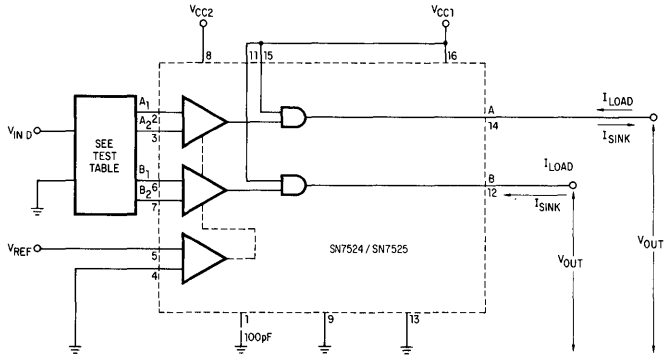
VOLTAGE WAVEFORMS



NOTES:

1. Pulse generators have the following characteristics: Z_{OUT} = 50 Ω, $t_r = t_f$ = 15 (±5) ns, t_{p1} = 100 ns, t_{p2} = 300 ns, PRR = 1 MHz.
2. Strobe input pulse is applied to Strobe A when inputs A_1 - A_2 are being tested and to Strobe B when inputs B_1 - B_2 are being tested.
3. C_1 includes probe and jig capacitance.

FIG. 2 DC TEST



TEST TABLE

TYPE	INPUTS	V_{ref}	V_{inD}	OUTPUT		
				V_{out}	I_{sink}	I_{load}
SN7524	A_1 - A_2 or B_1 - B_2	15 mV	< 11 mV	⩽ 0.4 V	16 mA	–
	A_1 - A_2 or B_1 - B_2	15 mV	> 19 mV	⩾ 2.4 V	–	–400 μA
	A_1 - A_2 or B_1 - B_2	40 mV	< 36 mV	⩽ 0.4 V	16 mA	–
	A_1 - A_2 or B_1 - B_2	40 mV	> 44 mV	⩾ 2.4 V	–	–400 μA
SN7525	A_1 - A_2 or B_1 - B_2	15 mV	< 8 mV	⩽ 0.4 V	16 mA	–
	A_1 - A_2 or B_1 - B_2	15 mV	> 22 mV	⩾ 2.4 V	–	–400 μA
	A_1 - A_2 or B_1 - B_2	40 mV	< 33 mV	⩽ 0.4 V	16 mA	–
	A_1 - A_2 or B_1 - B_2	40 mV	> 47 mV	⩾ 2.4 V	–	–400 μA

SN75450

DUAL PERIPHERAL DRIVER

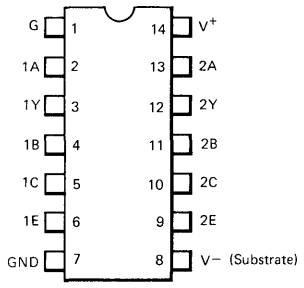
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The SN75450 is a versatile general purpose dual interface driver circuit that employs TTL or DTL logic. The SN75450 features two standard series 74 TTL gates and two uncommitted, high current, high voltage transistors offering the system designer the flexibility to tailor the circuit to his application. The SN75450 is useful in high speed logic buffers, power drivers, lamp drivers, relay drivers, line drivers, MOS drivers, clock drivers and memory drivers.

- **HIGH SPEED**
- **300 mA CURRENT CAPABILITY**
- **HIGH VOLTAGE CAPABILITY**
- **UNCOMMITTED OUTPUT DEVICES**
- **TTL OR DTL INPUT COMPATIBILITY**

CONNECTION DIAGRAMS
(TOP VIEW)

14 LEAD DIP

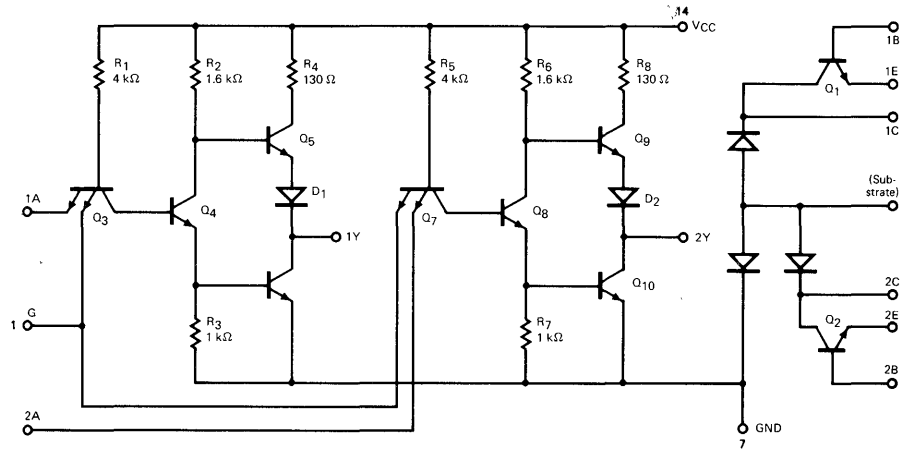


ORDER PART NO.
SN75450J

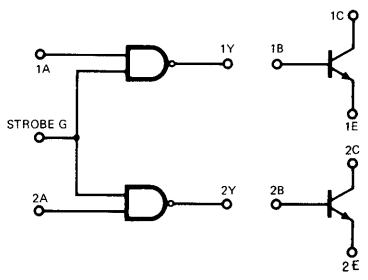
ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)	+7 V
Internal Power Dissipation (Note 2)	800 mW
Input Voltage (Note 3)	5.5 V
V_{CC} to Substrate or Collector to Substrate Voltage	35 V
Collector to Base Voltage	35 V
Emitter To Base Voltage	5 V
Collector to Base Voltage (Note 4)	30 V
Continuous Collector Current	300 mA
Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 60 seconds)	300°C

EQUIVALENT CIRCUIT



BLOCK DIAGRAM



Notes on following page.

ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $T_A = 25°C$ for typical values, unless otherwise specified.) (Note 5)

PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
TTL Gate					
Input HIGH Voltage	$V^+ = 4.75$ V	2.0			V
Input LOW Voltage	$V^+ = 4.75$ V			0.8	V
Output HIGH Voltage	$V^+ = 4.75$ V, $V_{IN} = 0.8$ V, $I_{OUT} = -400\ \mu A$	2.4	3.3		V
Output LOW Voltage	$V^+ = 4.75$ V, $V_{IN} = 2$ V, $I_{SINK} = 16$ mA		0.22	0.40	V
Low Level Input Current	$V^+ = 5.25$ V, $V_{IN} = 0.4$ V				
Input A				−1.6	mA
Input B				−3.2	mA
High Level Input Current					
Input A	$V^+ = 5.25$ V, $V_{IN} = 2.4$ V			40	μA
Input B				80	μA
Input A	$V^+ = 5.25$ V, $V_{IN} = 5.5$ V			1.0	mA
Input B				2.0	mA
Short Circuit Output Current (Note 7)	$V^+ = 5.25$ V	−18		−55	mA
Output LOW Supply Current	$V^+ = 5$ V, All Inputs HIGH		6.0	11	mA
Output HIGH Supply Current	$V^+ = 5$ V, All Inputs LOW		2.0	4.0	mA
Output Transistor					
Collector to Base Breakdown Voltage	$I_C = 100\ \mu A$, $I_E = 0$	35	48		V
Emitter to Base Breakdown Voltage	$I_E = 100\ \mu A$, $I_C = 0$	5.0	6.0		V
Collector to Emitter Breakdown Voltage	$I_C = 100\ \mu A$, $R_{BE} = 500\ \Omega$	30			V
*Collector Substrate Breakdown Voltage	$I_{CS} = 100\ \mu A$	35	50		V
Static Forward Current Transfer Ratio	$V_{CE} = 2$ V, $I_C = 100$ mA, $T_A = 25°C$	25			
(Note 6)	$V_{CE} = 2$ V, $I_C = 300$ mA, $T_A = 25°C$	30			
	$V_{CE} = 2$ V, $I_C = 100$ mA, $T_A = 0°C$	20			
	$V_{CE} = 2$ V, $I_C = 300$ mA, $T_A = 0°C$	25			
Saturated Base to Emitter Forward Voltage	$I_C = 100$ mA, $I_B = 10$ mA		0.85	1.00	V
(Note 6)	$I_C = 300$ mA, $I_B = 30$ mA		1.05	1.2	V
Collector to Emitter Saturated Voltage	$I_C = 100$ mA, $I_B = 10$ mA		0.25	0.40	V
(Note 6)	$I_C = 300$ mA, $I_B = 30$ mA		0.50	0.70	V

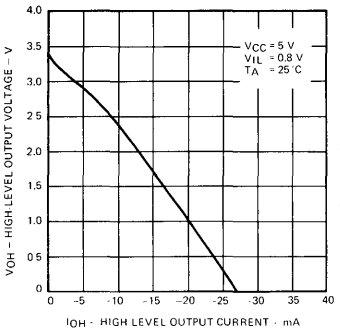
AC CHARACTERISTICS – $V^+ = +5$ V, $T_A = 25°C$, $C_L = 15$ pF, $R_L = 400\ \Omega$

TTL Gate					
Turn Off Delay Input to Output, t_{PLH}	Figure 1		12	22	ns
Turn On Delay Input to Output, t_{PHL}			8.0	15	ns
Output Transistor	$I_C = 200$ mA, $I_B{}^+ = 20$ mA, $I_B{}^- = 40$ mA				
Delay Time, t_d			8.0	15	ns
Rise Time, t_r	Figure 2		12	20	ns
Storage Time, t_s			7.0	15	ns
Fall Time, t_f			6.0	15	ns
Combined Gate and Transistor	$I_C = 200$ mA, $I_B = I_{OS}$, $C_L = 15$ pF				
Turn Off Delay Time, t_{PLH}			17		ns
Turn On Delay Time, t_{PHL}	Figure 3		16		ns
Turn Off Transistion Time, t_{TLH}			7.0		ns
Turn On Transistion Time, t_{THL}			9.0		ns

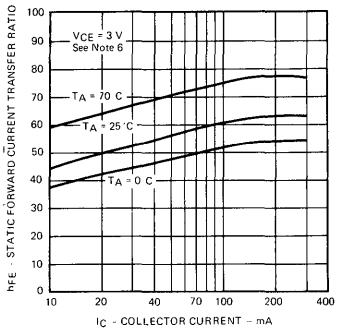
NOTES:
1. All voltage values are with respect to device ground terminal.
2. Rating applies for ambient temperatures to 70°C.
3. Input voltage should be zero or positive with respect to device ground terminal.
4. Applies for $R_{BE} < 500\ \Omega$
5. The substrate pin must always be tied to the most negative voltage for proper operation.
6. These parameters must be measured using pulse techniques. $t_w = 300\ \mu s$, duty cycle = 2%.
7. Not more than one output should be shorted at a time.

TYPICAL CHARACTERISTICS

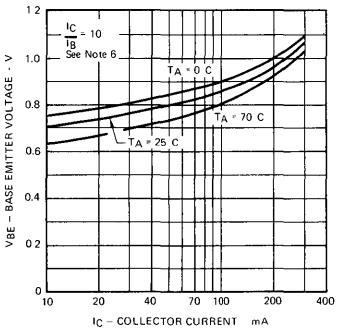
TTL GATE HIGH-LEVEL OUTPUT VOLTAGE VERSUS HIGH-LEVEL OUTPUT CURRENT



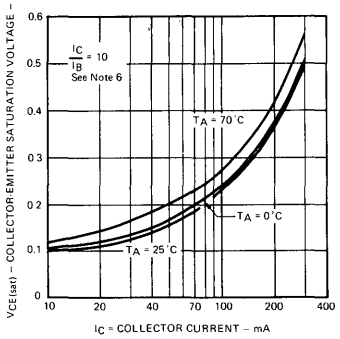
TRANSISTOR STATIC FORWARD CURRENT TRANSFER RATIO VERSUS COLLECTOR CURRENT



TRANSISTOR BASE TO EMITTER VOLTAGE VERSUS COLLECTOR CURRENT

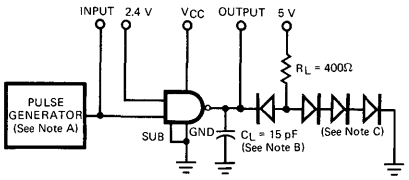


TRANSISTOR COLLECTOR TO EMITTER SATURATION VOLTAGE VERSUS COLLECTOR CURRENT

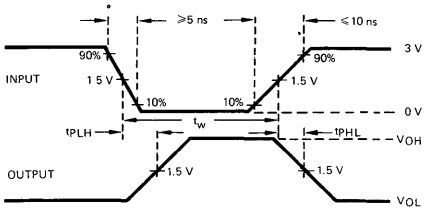


SWITCHING CHARACTERISTICS

PROPAGATION DELAY TIMES, EACH GATE



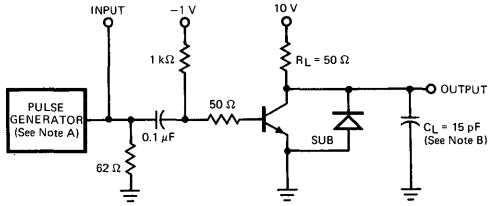
TEST CIRCUIT



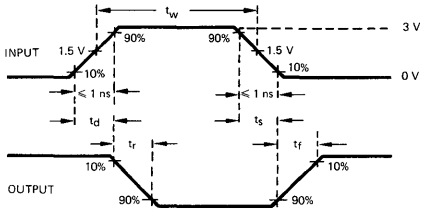
VOLTAGE WAVEFORMS

NOTES:
A. The pulse generator has the following characteristics: t_w = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L include probe and jig capacitance.
C. All diodes are 1N3064.

SWITCHING TIMES, EACH TRANSISTOR



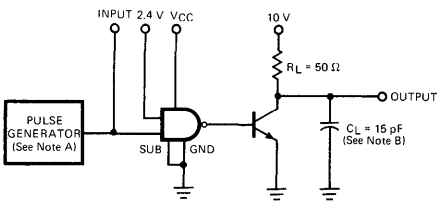
TEST CIRCUIT



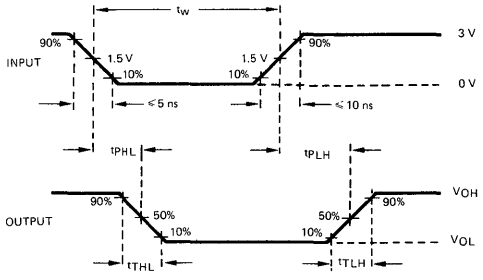
VOLTAGE WAVEFORMS

NOTES:
A. The pulse generator has the following characteristics: t_w = 0.3 μs, duty cycle ≤ 1%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

SWITCHING TIMES, GATE AND TRANSISTOR



TEST CIRCUIT

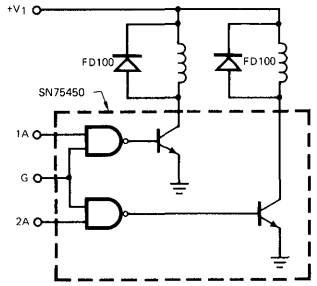


VOLTAGE WAVEFORMS

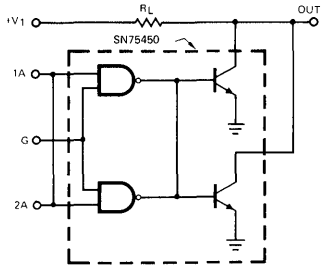
NOTES:
A. The pulse generator has the following characteristics: t_w = 0.5 μs, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

TYPICAL APPLICATIONS

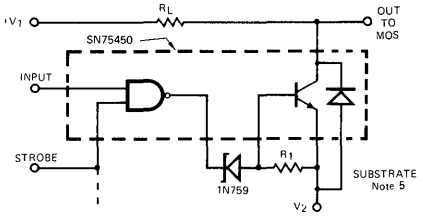
DUAL RELAY DRIVER



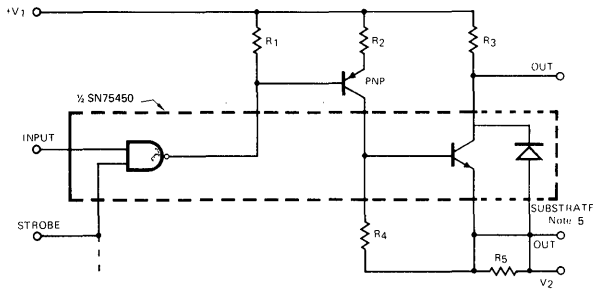
300 mA SINK DRIVER



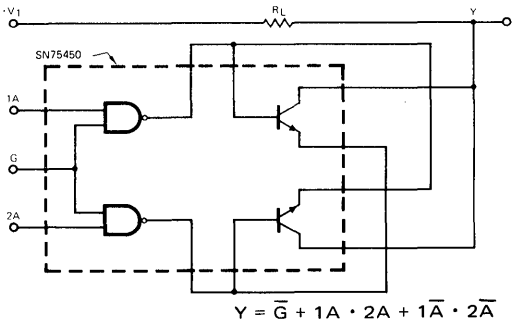
MOS DRIVER



FLOATING SWITCH

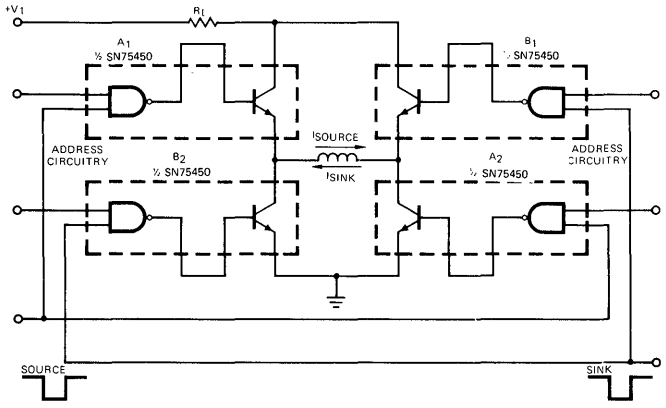


GATED COMPARATOR

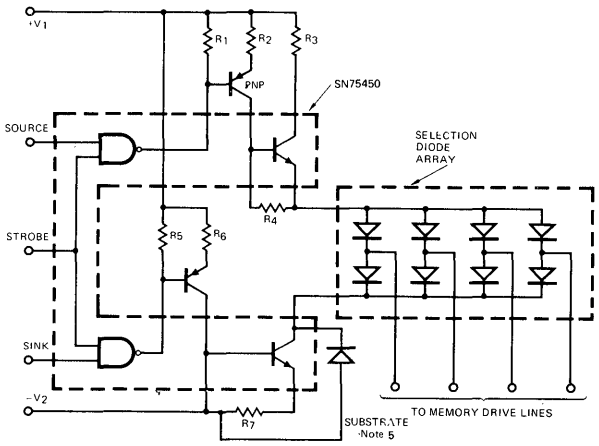


$$Y = \overline{G} + 1A \cdot 2A + 1\overline{A} \cdot 2\overline{A}$$

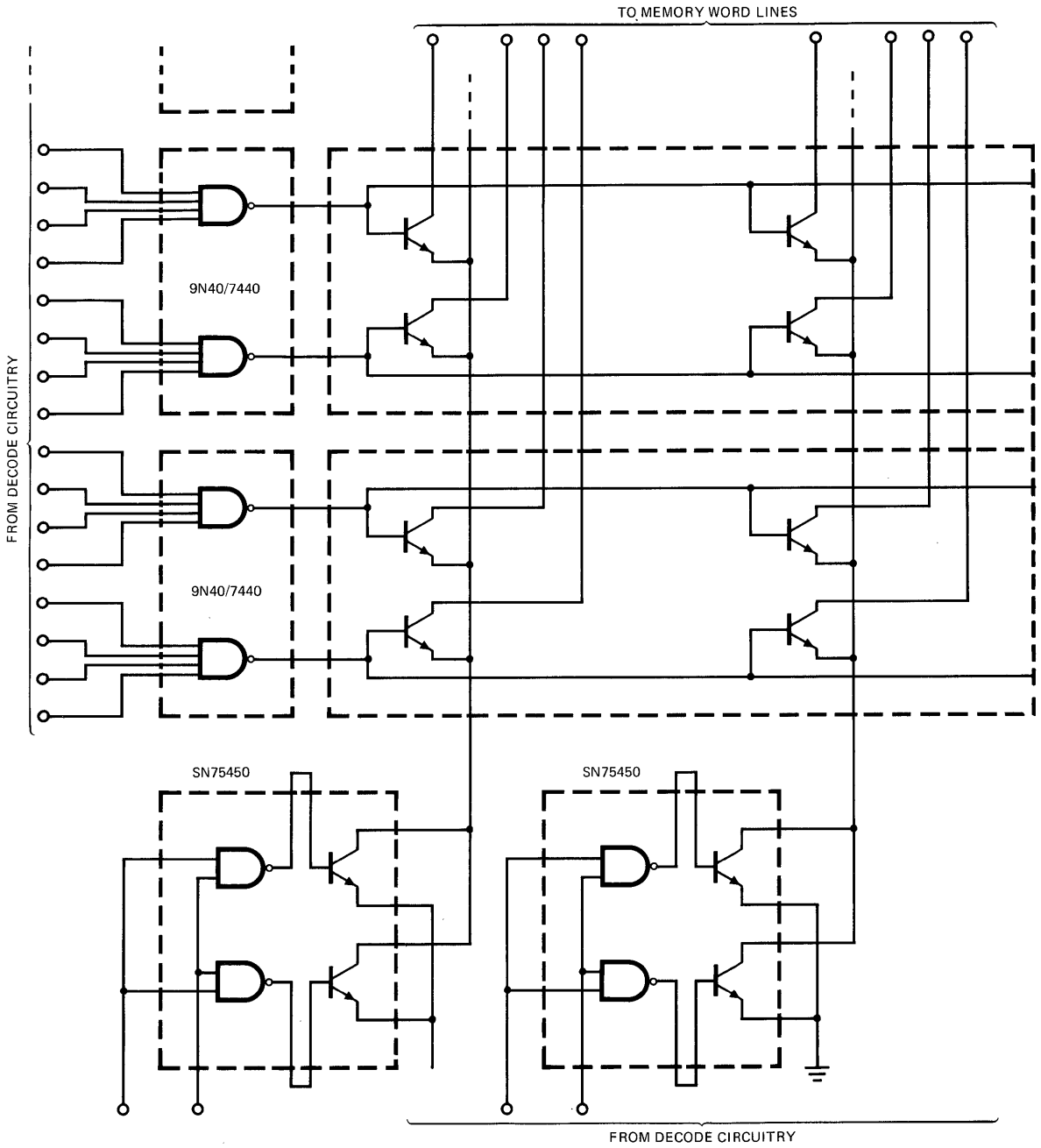
FILM MEMORY DIGIT DRIVER



CORE MEMORY DRIVER



APPLICATIONS (cont'd)



WORD LINE MEMORY DRIVER USING SN75450

SN75450 CIRCUIT APPLICATIONS

- Dual Lamp Driver
- Dual Relay Driver
- Gated Comparator
- Floating Switch
- Dual MOS-to-TTL Driver
- Dual TTL-to-MOS Driver
- 500 mA Sink Driver
- Dual Linear Amplifier
- Dual Photo Switch (TTL Compatible Output)
- NAND Gate Schmitt (Timed Relay or Lamp Control)
- High Input Impedance Low Speed Schmitt with TTL Output
- Dual High-Speed Gate
- Square Wave Generator
- SCR Gate Driver
- Super TTL Gate with 250 mA Sinking Ability
- Dual-Channel Single-Ended Line Driver
- Memory System Current Sink
- Memory System Current Source
- Film Memory Digit Driver
- Core Memory Driver
- Phase Detector
- DC to AC Converter
- Dwell Meter Driver
- Tachometer
- MOS Memory Write Driver

TAA630 †

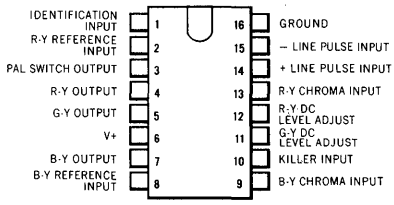
PAL TV CHROMA DEMODULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The TAA630 is a synchronous demodulator for direct drive of color video output stages constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It is designed for use in color television receivers operating on the Phase Alternate Line (PAL) system. The circuit consists of two synchronous demodulators, a decoding matrix, a PAL switch with internal multivibrator, and a color killer switch.

- **DOUBLE-BALANCED SYNCHRONOUS DEMODULATOR**
- **INTERNAL DECODING MATRIX**
- **EMITTER FOLLOWER OUTPUTS**
- **INTERNAL PAL SWITCH**
- **INTERNAL COLOR KILLER**
- **PROVISION FOR OUTPUT DC LEVEL MATCHING**

CONNECTION DIAGRAM
(TOP VIEW)



ORDERING INFORMATION

Ceramic Dual In-Line	**TAA630/6B**
Ceramic Quad In-Line	**TAA630/7H****

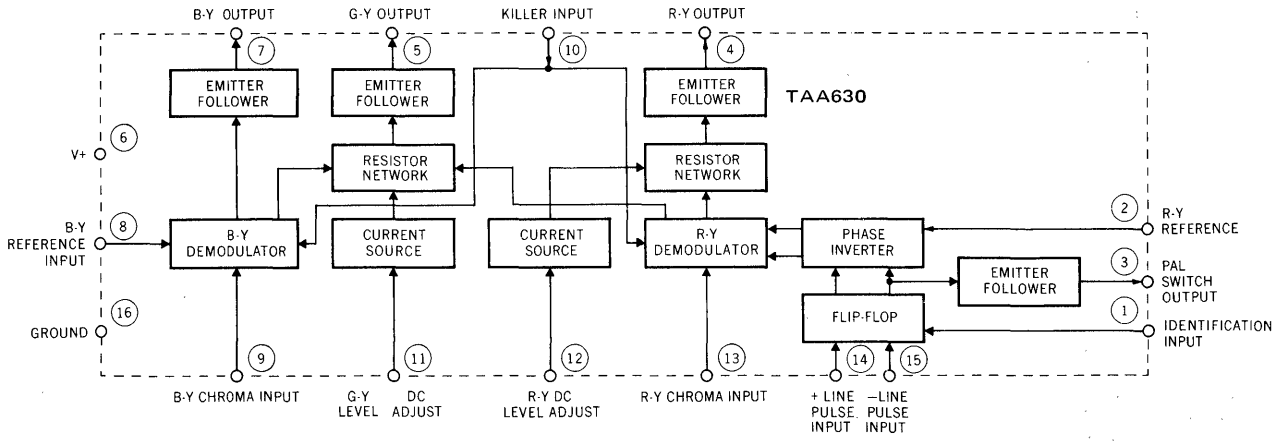
**Available from factory on special request.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)	13.2 V
Internal Power Dissipation (Note 2)	730 mW
Color Difference Output Currents	5 mA
Operating Temperature Range	−40° C to +85° C
Storage Temperature Range	−65° C to +150° C
Lead Temperature (Soldering, 60 seconds)	300° C

† Formerly referred to as the μA786

BLOCK DIAGRAM



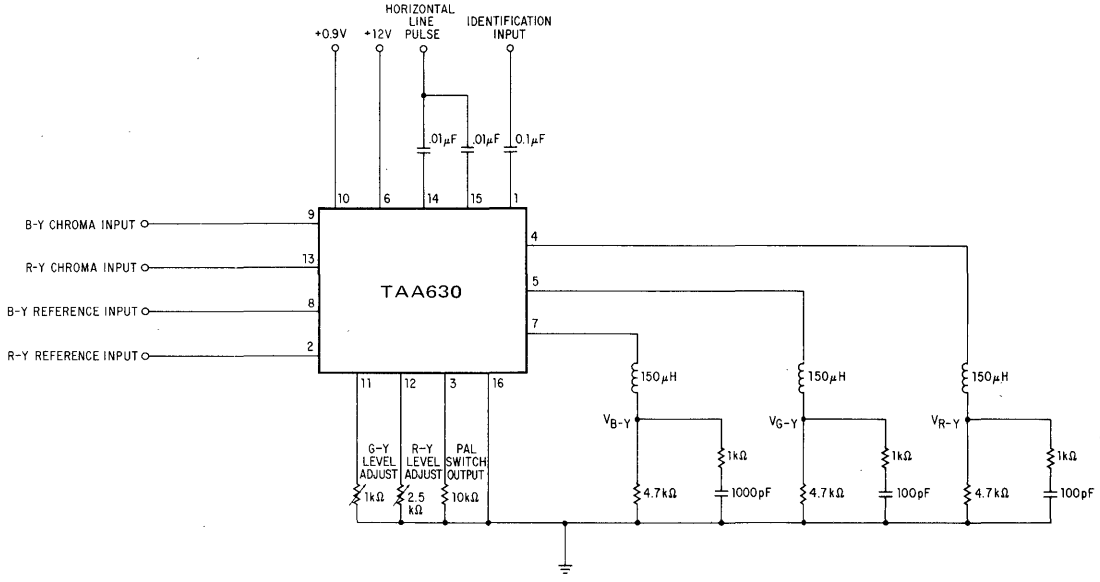
Notes on following page.

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V+ = 12V, Test Circuit 1, unless otherwise specified. See Note 3)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (I_6)			33	40	mA
DC Voltage at B-Y Output	(NOTE 4)	6.8	7.4	7.8	V
Output Resistance at Color Difference Terminals (R_4, R_5, R_7)				100	Ω
Color Difference Gain					
R-Y Channel			7.0		V/V
B-Y Channel			12.5		V/V
G-Y Channel			(NOTE 5)		
Maximum Color Difference Output Voltage	(NOTE 6)				
R-Y Output (V_4)			3.2		Vp-p
B-Y Output (V_7)			4.0		Vp-p
G-Y Output (V_5)			1.8		Vp-p
Input Resistance of Chroma Inputs (R_9, R_{13})			1000		Ω
Input Capacitance of Chroma Inputs (C_9, C_{13})			10		pF
DC Voltage at Chroma Inputs (V_9, V_{13})			3.2		V
Input Resistance of Reference Input (R_2, R_8)			900		Ω
DC Voltage at Reference Inputs (V_2, V_8)			2.2		V
Color Killer Voltage Threshold (V_{10})					
Color "ON"				0.9	V
Color "OFF"		0.3			V
Peak-To-Peak PAL Switch Output Voltage (V_3)		2.0	3.0		Vp-p

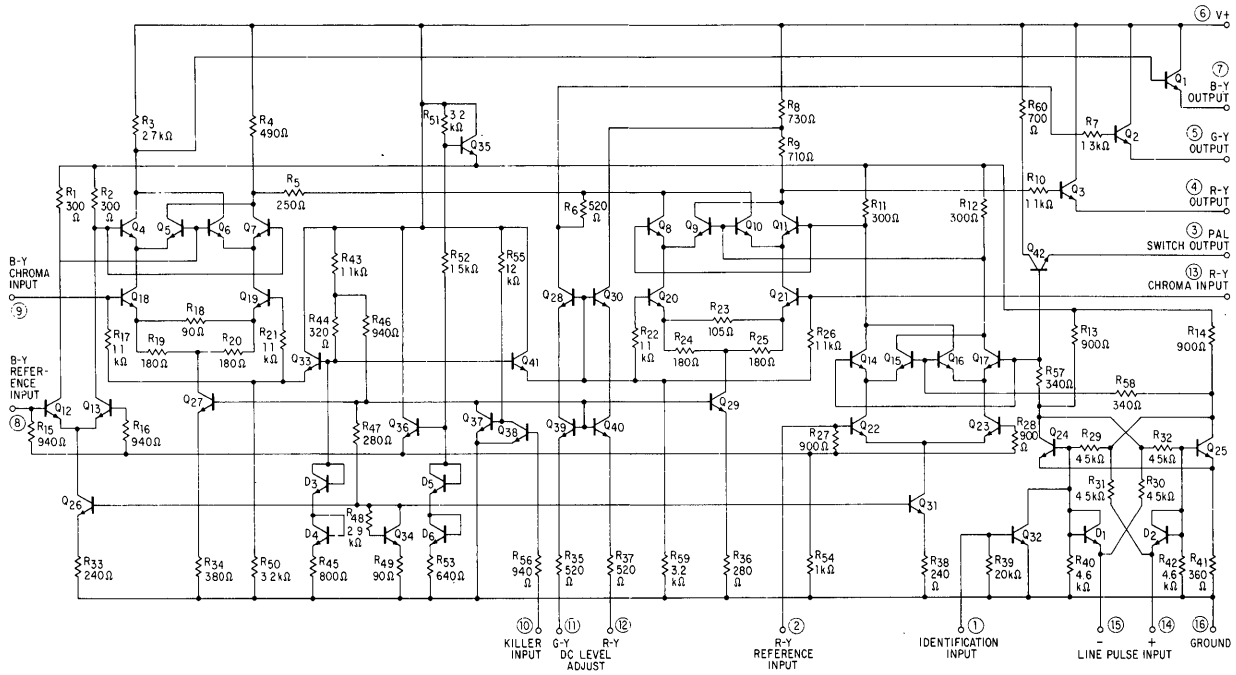
TEST CIRCUIT 1



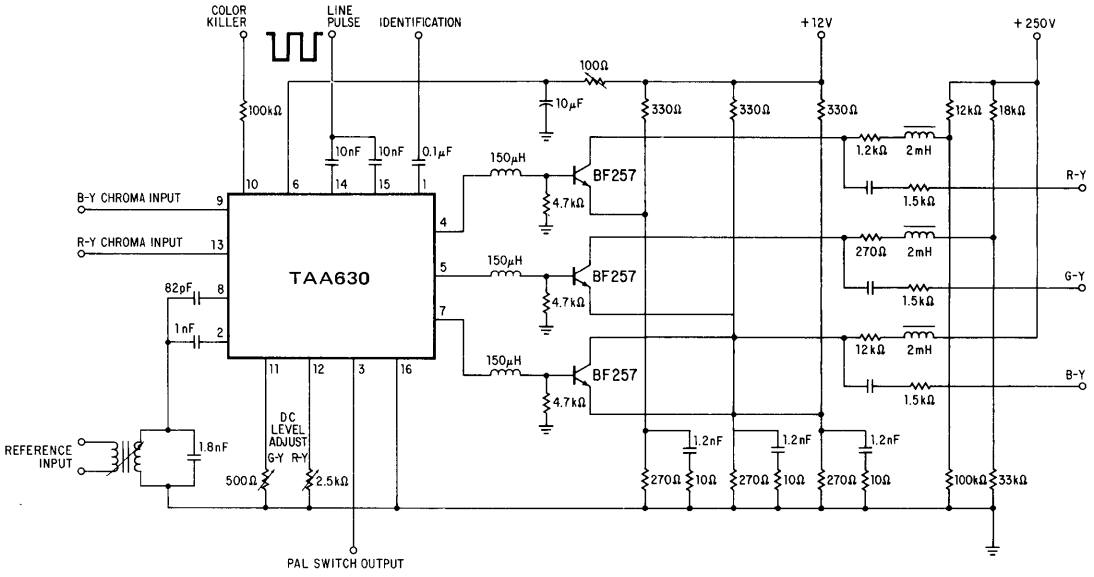
NOTES

1. 16 volts is permissible during warmup.
2. Rating applies for ambient temperatures to 70°C. Derate linearly at 9.1 mW/°C above 70°C.
3. Killer Voltage, V_{10} = 0.9 V; Reference Voltages V_2 and V_8 = 1 Vp-p @ 4.4 MHz, V_2 leads by 90°; Line Input Pulses, V_{14} and V_{15} = −2.5 V peak; Chroma Input voltages V_9 and V_{13} = 50 mVp-p; Identification Input Voltage, V_1 = 4 Vp-p.
4. DC Output Levels at R-Y and G-Y outputs are adjustable to B-Y level with a variable voltage ($V \leq 1.2$ V) or with variable resistors connected between pins 11 and 12 to ground. See typical application.
5. G-Y Output is typically equal to 0.51 (R-Y) −0.19)B-Y).
6. Gain Linearity is greater than 0.7.

EQUIVALENT CIRCUIT



TYPICAL APPLICATION – PAL COLOR TV SYSTEM



TAA640†

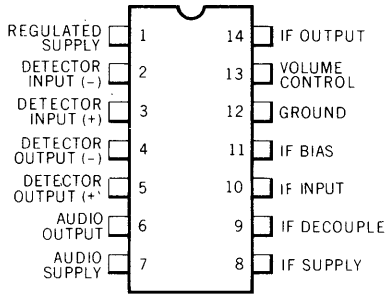
TV/FM SOUND SYSTEM

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The TAA640 is a monolithic TV/FM sound system constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device consists of a four stage limiting IF amplifier, modified FM slope detector, and an audio preamplifier. The circuit incorporates a dc volume control and may be remotely controlled over a 60 dB range. Excellent sensitivity, high AM rejection, an internally regulated power supply, coupled with low external component count, make the TAA640 an ideal choice for TV sound channels and line operated or automobile FM radios.

- **100 μV SENSITIVITY**
- **44 dB AM REJECTION**
- **DC VOLUME CONTROL**
- **INTERNALLY REGULATED SUPPLY**
- **SINGLE COIL SLOPE DETECTOR**
- **LOW EXTERNAL COMPONENT COUNT**

CONNECTION DIAGRAM
(TOP VIEW)



ORDERING INFORMATION

Ceramic Dual In-Line	**TAA640/6A**
Ceramic Quad In-Line	**TAA640/7F****

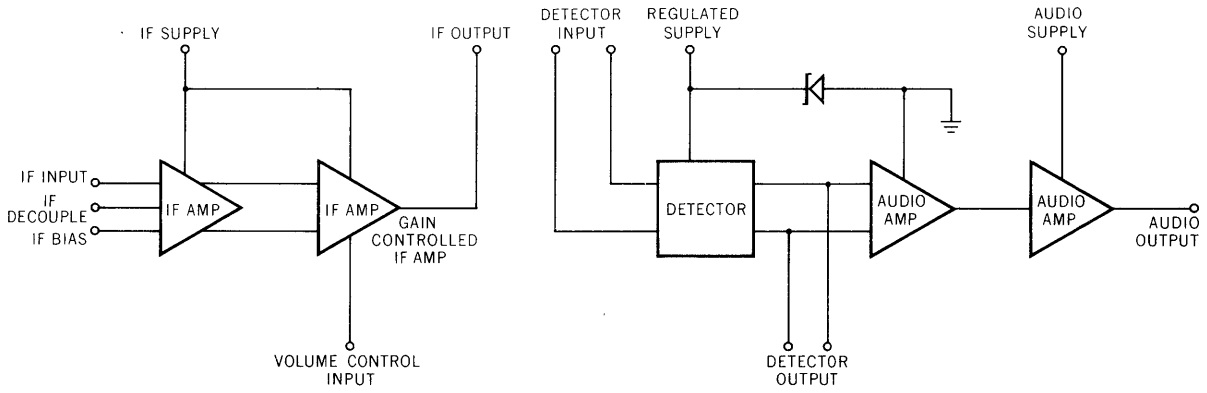
**Available from factory on special request.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages (Note 1) V_7	32 V
V_8	9 V
Supply Currents (Note 1) $I_1+I_7+I_8$	40 mA
I_1	28 mA
Internal Power Dissipation (Note 2)	
Ceramic DIP	670 mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

† Formerly referred to as μA784

BLOCK DIAGRAM



Notes on following page.

*Planar is a patented Fairchild process.

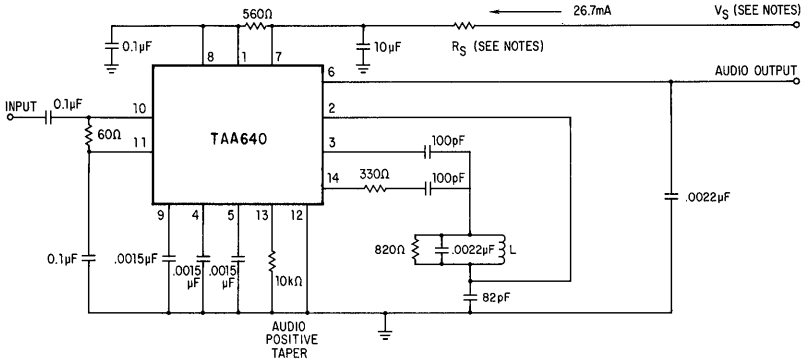
ELECTRICAL CHARACTERISTICS $T_A = 25^\circ C$. See note 3.

Parameter	Condition	MIN	TYP	MAX	UNITS
Zener Voltage, V_1			7.4	8.5	V
Voltage at Pin 7			22		V
Current at Pin 7			0.7		mA
IF Input Voltage for 3 dB Limiting			100		μV
IF Amplifier Voltage Gain		70	76		dB
IF Output Voltage			1.7		V_{p-p}
AM Rejection	30% AM		44		dB
Audio Output Voltage	$\Delta f = \pm 50$ kHz		1.6		V_{rms}
Total Distortion	$\Delta f = \pm 15$ kHz		1.6		%
	$\Delta f = \pm 50$ kHz			5.0	%
Remote Volume Control Range		60			dB

NOTES
1. Rating permissible during warmup.
2. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 8.3 mW/°C for the Ceramic DIP package.
3. Test Circuit 1 applicable. Adjust $I_1 + I_7 + I_8$ to equal = 26.7 mA. IF input = 5.5 MHz; modulation = ±15 kHz unless otherwise specified.

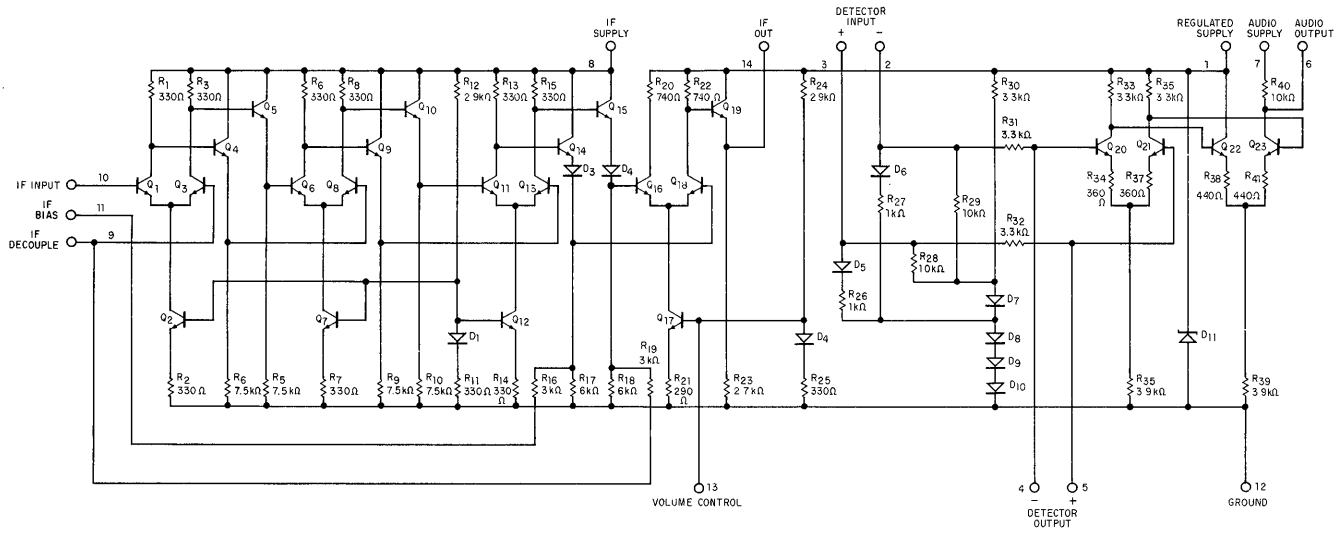
TEST CIRCUIT AND TYPICAL APPLICATION

TV SOUND SYSTEM



Notes:
1. Adjust V_S and R_S so that $I_S = 26.7$ mA.
2. Detector coil for 5.5 MHz operation: 6.5 turns 0.5 mm wire; Coil Former: Ferroxcube AP 3016/02 less frame; Can: AP 3015/02; Core: 3122 104 93040.

EQUIVALENT CIRCUIT



TBA550 †

TV SIGNAL PROCESSING CIRCUIT

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The TBA550 is a TV signal Processing Circuit constructed on a single silicon chip using the Fairchild Planar* Epitaxial process. This device serves as a central processing and distribution circuit for the video, AGC, noise, and synchronization signals for both monochrome and color TV systems including receivers, monitors and cameras. Other applications are in raster-scan alpha-numeric displays, video tape recorders and studio and broadcast equipment.

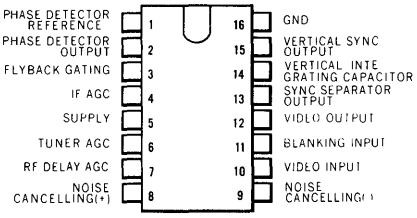
- **VIDEO PREAMPLIFIER WITH EMITTER FOLLOWER OUTPUT**
- **GATED AGC DETECTOR SUPPLYING CONTROL VOLTAGES FOR VIDEO I.F. AGC AND TUNER DELAYED AGC**
- **AUTOMATIC FREQUENCY CONTROL VOLTAGE FOR HORIZONTAL OSCILLATOR**
- **VERTICAL SYNC PULSE SEPARATOR**
- **VIDEO BLANKING FACILITY**
- **NOISE CANCELLATION IN AGC AND SYNC CIRCUITS**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)		16 V
Power Dissipation (Note 2)		730 mW
Operating Temperature Range		−25°C to +125°C
Storage Temperature Range	Ceramic DIP	−65°C to +150°C
Lead Temperature (Soldering)	Ceramic DIP, 60 Seconds	300°C

CONNECTION DIAGRAM

(TOP VIEW)



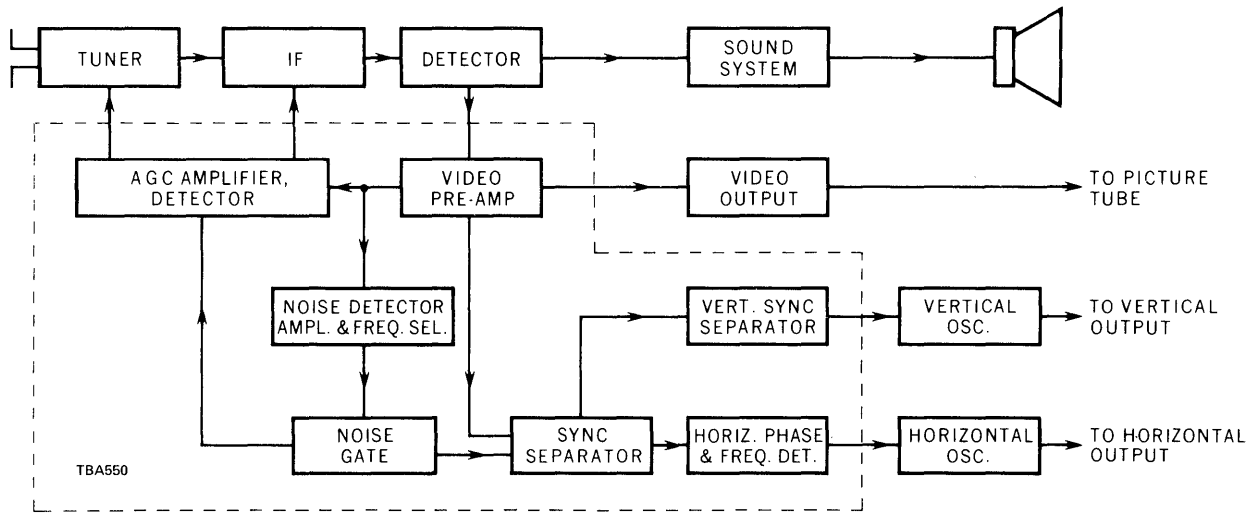
ORDERING INFORMATION

Ceramic Dual-in-line	**TBA550/6B**
Ceramic Quad-in-line	**TBA550/7H***

*Available on special request.

†Formerly referred to as μA785/TAA700

BLOCK DIAGRAM



Notes on following page.

*Planar is a patented Fairchild process.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = + 12 V, Test Circuit 1, unless otherwise specified)

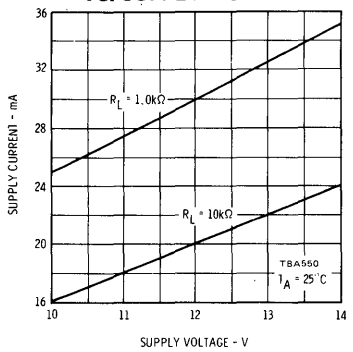
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current, I_5	$R_L = \infty$, $V_{10} = 0$		19	25	mA
	R_L = 1 kΩ, $V_{10} = 0$		30		mA
VIDEO PREAMPLIFIER					
Voltage Gain			3.0		V/V
Input Resistance, R_{10}			2.7		kΩ
Input Capacitance, C_{10}				1.0	pF
Bandwidth	-3dB	5.0	14		MHz
Black Level at Video Output	$V_{10} = 2V_{P-P}$, Direct Coupled		5.0		V
Video DC Output Voltage, V_{12}	$V_{10} = 0$	8.5	9.8	10.6	V
Tracking of Video Output Voltage with Supply Variation, $\frac{\Delta V_{12}}{\Delta V_5}$	$V_{10} = 0$		0.7		V/V
Peak Video Output Current	(Note 3)		14		mA
Required Video Blanking Input Voltage Pulse, V_{11}	(Note 4)	1.0			V
Required Video Blanking Input Current Pulse, I_{11}	(Note 4)	1.0			mA
Required Flyback Gating Voltage Pulse, V_3	(Note 4)	1.0			V
Required Flyback Gating Current Pulse, I_3	(Note 4)	1.0			mA
AGC CIRCUIT					
Control Voltage at IF AGC Terminal, V_4	V_{10} = 0V		0		V
	V_{10} = - 2.5 V_{DC}		8.0		V
Control Voltage at Tuner AGC Terminal, V_6	V_{10} = 0V		0		V
	V_{10} = - 2.5V_{DC}		7.0		V
SYNCHRONIZATION CIRCUIT					
AFC Operating Reference Voltage, V_2	$V_1 = 3V_{DC}$, $V_2 = 7\ V_{P-P}$, (Note 5)		7.0		V_{DC}
Vertical Sync Pulse Output, V_{15}		10	11.5		V_{P-P}
Vertical Sync Output Resistance			2.0		kΩ
Slicing Level (Percentage Below Top of Sync Pulse)	(Note 6)		30		%
NOISE GATE					
Amplitude of Noise Pulses Above Sync Tips to Activate Noise Gate	(Note 7)		0.9		V
Minimum Frequency of Noise Pulses to Activate Noise Gate	(Note 7)		3.5		MH_z
Video Input Level to reduce V_8 to 10 V			3.3		V_{PEAK}

NOTES

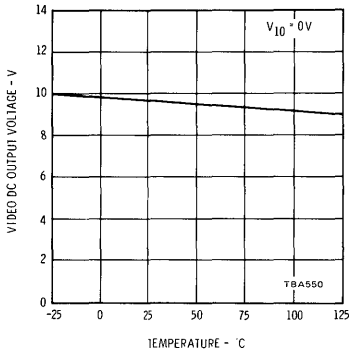
1. Rating permissible during warm-up; however, continuous maximum supply voltage is 14 volts.
2. Derate linearly at 9.1 mW/°C for ambient temperatures above 70°C.
3. Operation with R_L less than 430 Ω is not recommended.
4. The TBA550 may be operated ungated if pin 3 is connected to the positive supply line via a resistor of a suitable value (e.g. 10 kΩ). However, the following precaution should be taken: The decoupling capacitors at the i.f. and tuner control points must be larger to prevent ripple voltages due to the vertical sync pulses. As a consequence the AGC will not follow fast input signal fluctuations (airplane flutter). Since the horizontal phase detector is designed to be gated, ungated operation will result in the phase detector not operating as a frequency detector when the horizontal oscillator is out of sync. This considerably decreases the pull-in range.
5. These values apply for an oscillator-reactance stage having a control sensitivity of 400 Hz/V. This yields a hold-in range of about ±1000 Hz. If the phase detector is gated a pull-in range of about ±700 Hz is obtained without affecting the noise immunity.
6. The slicing level is independent of the video input level.
7. The noise detector of the TBA550 is frequency and amplitude selective, i.e., frequencies and noise levels above the values given will turn off the sync and AGC detectors.

TYPICAL PERFORMANCE CURVES
(TEST CIRCUIT 1 UNLESS OTHERWISE SPECIFIED)

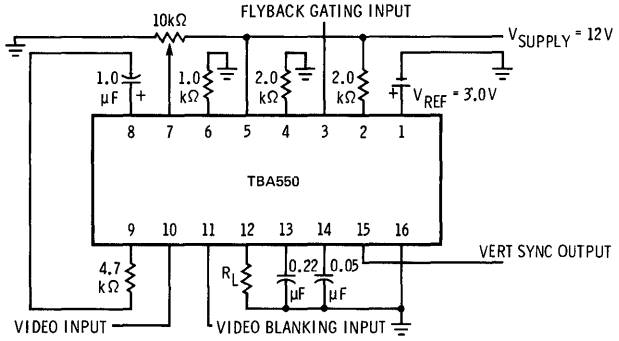
SUPPLY CURRENT VS. SUPPLY VOLTAGE



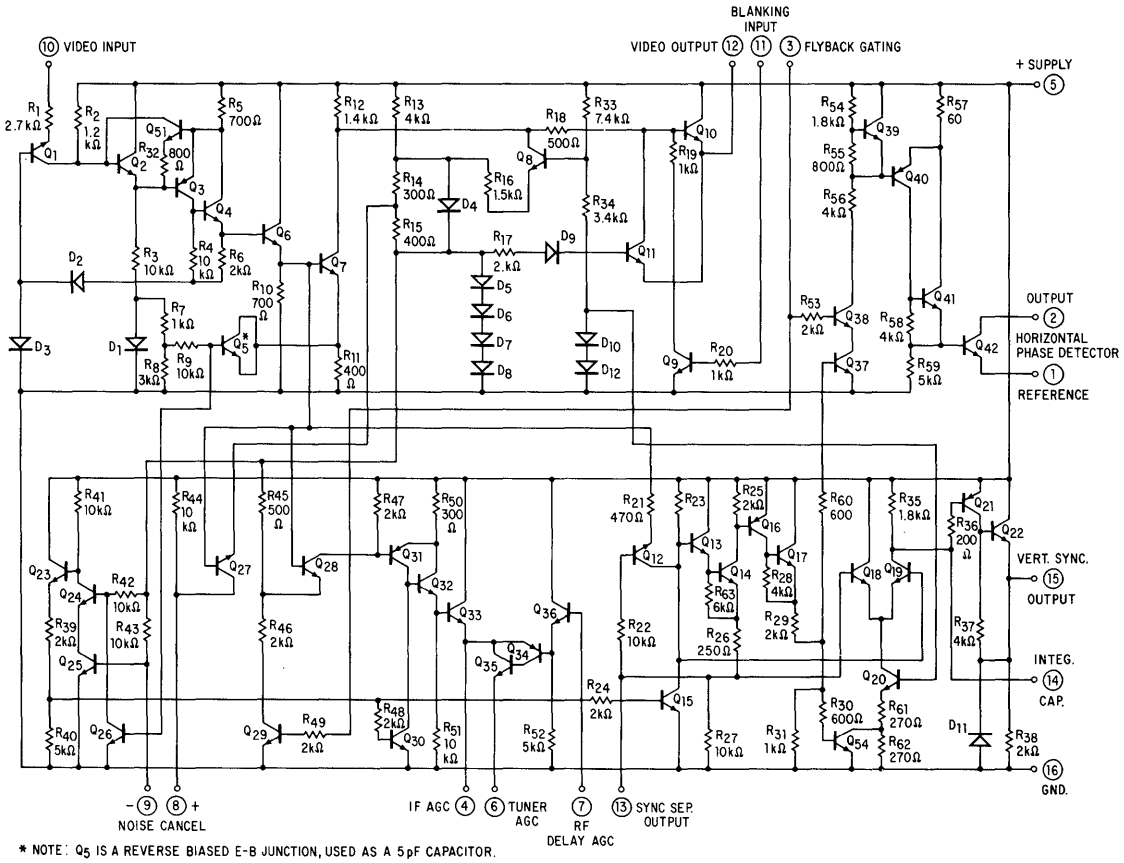
VIDEO DC OUTPUT VOLTAGE VS. TEMPERATURE



TEST CIRCUIT 1

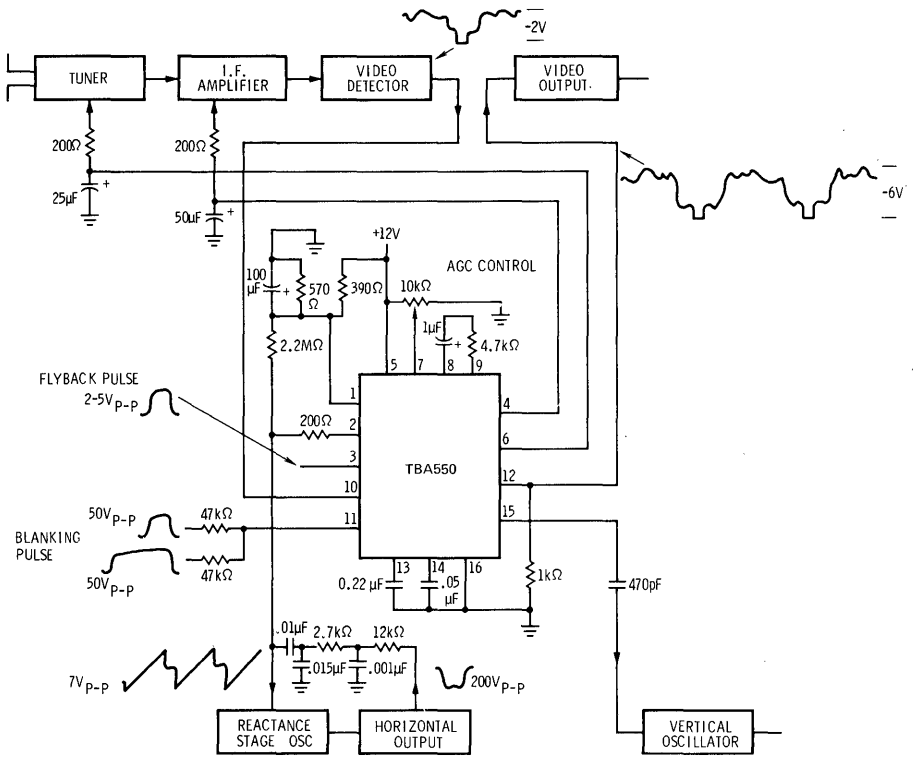


EQUIVALENT CIRCUIT



* NOTE: Q_5 IS A REVERSE BIASED E-B JUNCTION, USED AS A 5pF CAPACITOR.

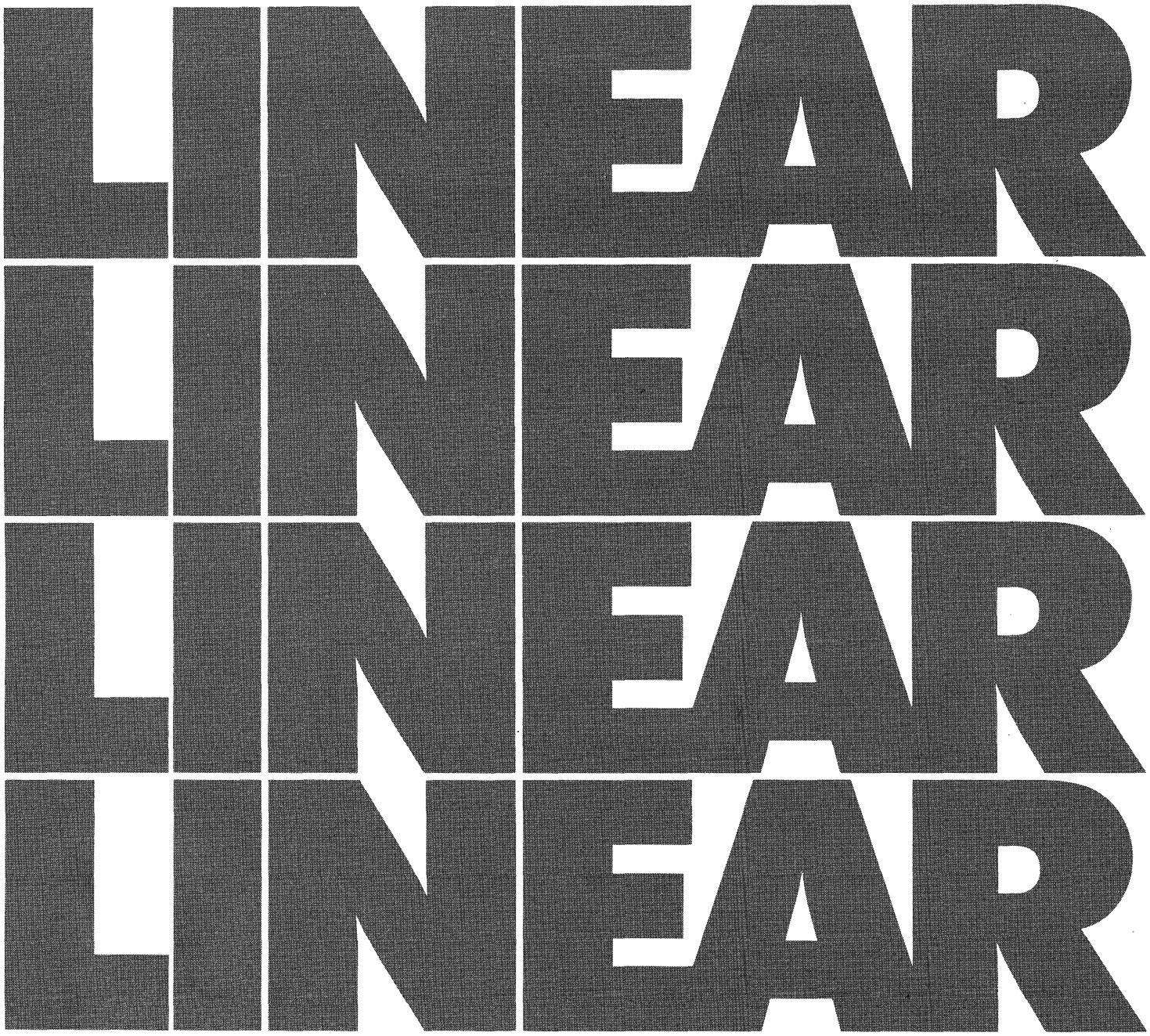
TYPICAL TV RECEIVER APPLICATION



For Complete Ordering Information See Page 304

Planned New Products

Consumer Products
Interface Elements
Voltage Comparators
Operational Amplifiers

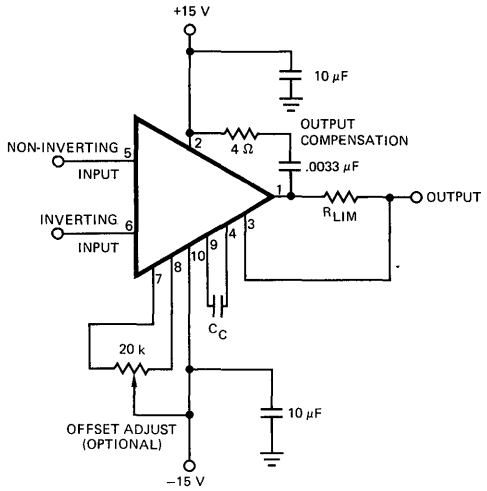


μA791
HIGH POWER OPERATIONAL AMPLIFIER

DESCRIPTION – The μA791 is a high performance monolithic operational amplifier intended for use in a wide variety of applications including audio amplifiers, servo amplifiers, and power supplies. The high gain and high output power capability provide superior performance wherever an operational amplifier/power booster combination is required.

- **CURRENT OUTPUT TO 1 AMP**
- **SHORT CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **NO LATCH-UP**
- **LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGES**

BLOCK DIAGRAM



TBA 641B
AUDIO AMPLIFIER

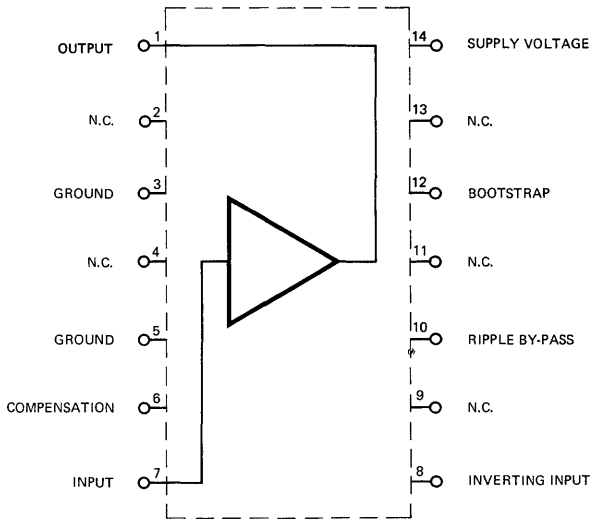
DESCRIPTION – The TBA 641B is a monolithic integrated circuit particularly designed for use as audio power amplifier in car radio and television receivers and in industrial applications which require high output power, low distortion and high reliability performance.

Special features of the circuit include a low quiescent current, self centering bias for operation at supply voltage ranging from 6 V to 16 V, direct coupling of the input.

The circuit requires a minimum number of external components.

- **OUTPUT POWER 4.5 W (14 V – 4 Ω)**
- **LOW DISTORTION**
- **LOW QUIESCENT CURRENT**
- **SELF CENTERING BIAS**
- **HIGH INPUT IMPEDANCE**
- **LOW SUPPLY VOLTAGE RANGE EXCELLENT FOR CAR RADIO APPLICATION**

BLOCK DIAGRAM



CA3075
FM IF AMPLIFIER-LIMITER, DETECTOR, AND AUDIO PREAMPLIFIER

DESCRIPTION – The CA3075 is an integrated circuit which provides, in a single monolithic chip, an FM IF subsystem for Communications and High-Fidelity Receivers. This device, consists of a multistage IF amplifier-limiter section with a Zener regulated power supply, an FM detector stage, and an AF preamplifier section.

The three-stage, emitter-follower-coupled IF amplifier section provides a 60 dB typical voltage gain at an operating frequency of 10.7 MHz and features, because of its transistor constant-current sink, an output stage with exceptionally good limiting characteristics.

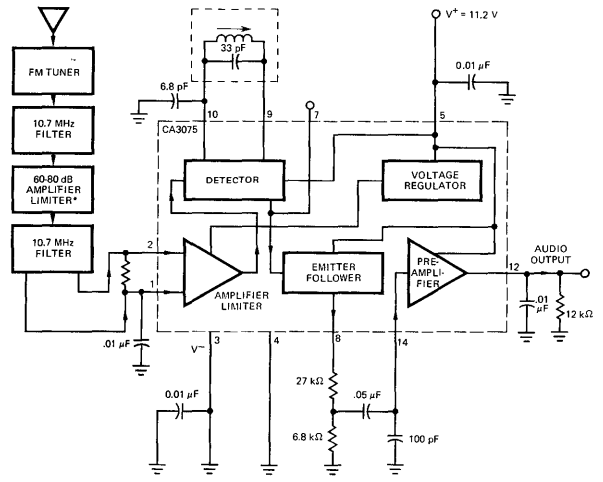
The FM detector section, which utilizes a differential-peak-detection circuit, requires only a single coil in the associated outboard detector circuit; hence, tuning the detector circuit is a simple procedure.

The audio preamplifier circuit provides a 21 dB voltage gain with low output impedance for driving subsequent audio amplifier stages.

The CA3075 utilizes a 14-lead dual in-line package.

- **GOOD SENSITIVITY: INPUT LIMITING VOLTAGE (KNEE) = 250 μV TYPICAL AT 10.7 MHz**
- **EXCELLENT AM REJECTION: 55 dB TYPICAL AT 10.7 MHz**
- **INTERNAL ZENER DIODE REGULATION FOR THE IF AMPLIFIER SECTION**
- **LOW HARMONIC DISTORTION**
- **DIFFERENTIAL PEAK DETECTION: PERMITS SIMPLIFIED SINGLE-COIL TUNING**
- **AUDIO PREAMPLIFIER VOLTAGE GAIN: 21 dB TYPICAL**
- **MINIMUM NUMBER OF EXTERNAL PARTS REQUIRED**
- **FM IF AMPLIFIER APPLICATIONS UP TO 20 MHz**

BLOCK DIAGRAM



CA3076
HIGH-GAIN WIDE-BAND IF AMPLIFIER-LIMITER

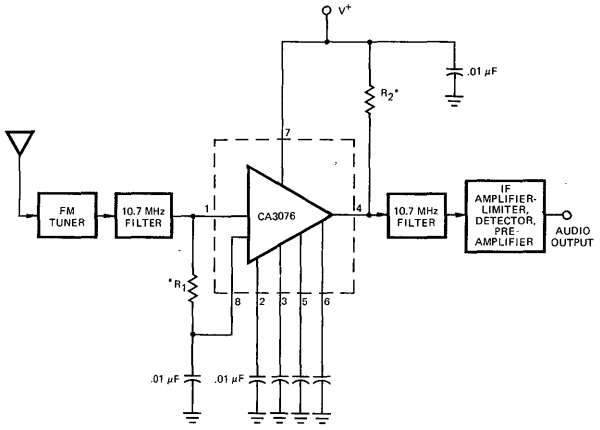
DESCRIPTION – The CA3076 monolithic integrated circuit is a high-gain wide-band amplifier-limiter for use in the IF sections of Communications and High-Fidelity FM Receivers. The CA3076 consists of a four stage IF amplifier-limiter section with a voltage regulator section.

The four-stage emitter-follower-coupled IF amplifier section provides an 80 dB voltage gain with a 2 kΩ load at a frequency of 10.7 MHz. The output stage has exceptionally good limiting characteristics because of its transistor constant-current sink. The voltage regulator section provides zener-regulated, decoupled voltages for the IF amplifier.

The CA3076 utilizes an hermetically-sealed 8-lead TO-5 type package.

- **EXCEPTIONALLY GOOD SENSITIVITY: INPUT LIMITING VOLTAGE (KNEE) = 50 μV TYPICAL AT 10.7 MHz**
- **HIGH GAIN: 80 dB WITH 2 kΩ LOAD**
- **INTERNAL VOLTAGE SUPPLY REGULATOR**
- **WIDE FREQUENCY CAPABILITY: >20 MHz**

BLOCK DIAGRAM



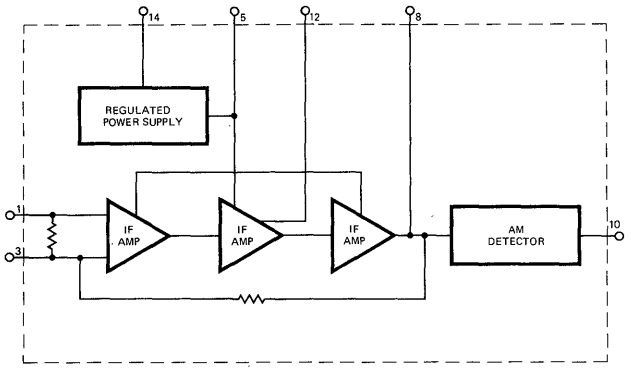
*R_1, R_2 selected for proper filter matching.

ULN2131
FM IF AMPLIFIER

DESCRIPTION – The type ULN-2131 FM Gain Block linear monolithic integrated circuit is designed for use in communications and high fidelity FM receivers. This device consists of a three-stage limiting amplifier section, a regulated power supply, an AM detector and 330 Ω input and output terminations with 7 pF shunting capacitance required for 10.7 MHz ceramic filters. Gain can be adjusted without effect on input and output conditions by addition of a fixed resistor between pins 5 and 12. The device is housed in an eight pin Mini DIP, ideally suited for saving space in the receiver.

- **THREE-STAGE LIMITING AMPLIFIER**
- **HIGH VOLTAGE GAIN**
- **REGULATED POWER SUPPLY**
- **AM DETECTOR**

BLOCK DIAGRAM

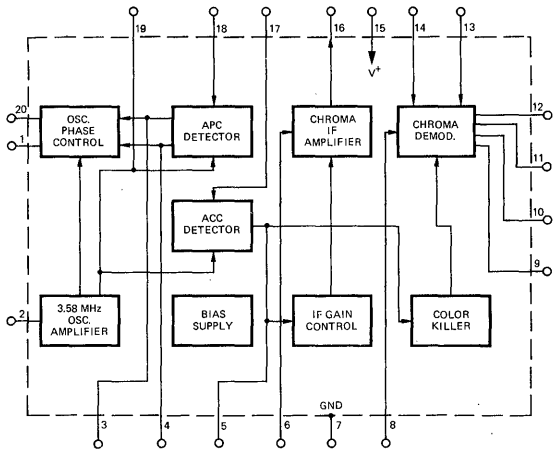


μA782
COLOR TV CHROMA PROCESSOR

DESCRIPTION – The μA782 monolithic integrated circuit performs the entire chroma processing function in a color TV receiver and provides four (4) demodulated chroma outputs. With a resistor matrix added externally to the outputs to obtain the R-Y, B-Y and G-Y signals the outputs may be used to drive direct coupled a color difference output amplifier or an RGB type output amplifier.

- **CHROMA DEMODULATION**
- **COLOR KILLING**
- **GAIN CONTROLLED CHROMA IF AMPLIFICATION**
- **SYNCHRONOUS ACC DETECTION**
- **PHASE LOCKED 3.58 MHz OSCILLATOR**
- **SYNCHRONOUS APC DETECTION**
- **BURST GATING PLUS OSCILLATOR OUTPUT BLANKING**
- **INTERNAL BIASING**
- **EXTERNAL COMPONENT COUNT GREATLY REDUCED**

BLOCK DIAGRAM



CA3066/CA3067
TELEVISION CHROMA SYSTEM

DESCRIPTION – The CA3066 and CA3067 are monolithic silicon integrated circuits that constitute a complete chroma system for color television receivers. The CA3066 provides subcarrier regeneration and total chroma signal processing prior to demodulation; the CA3067 performs the demodulation and tint control functions. Each device utilizes a 16-lead quad-in-line plastic package.

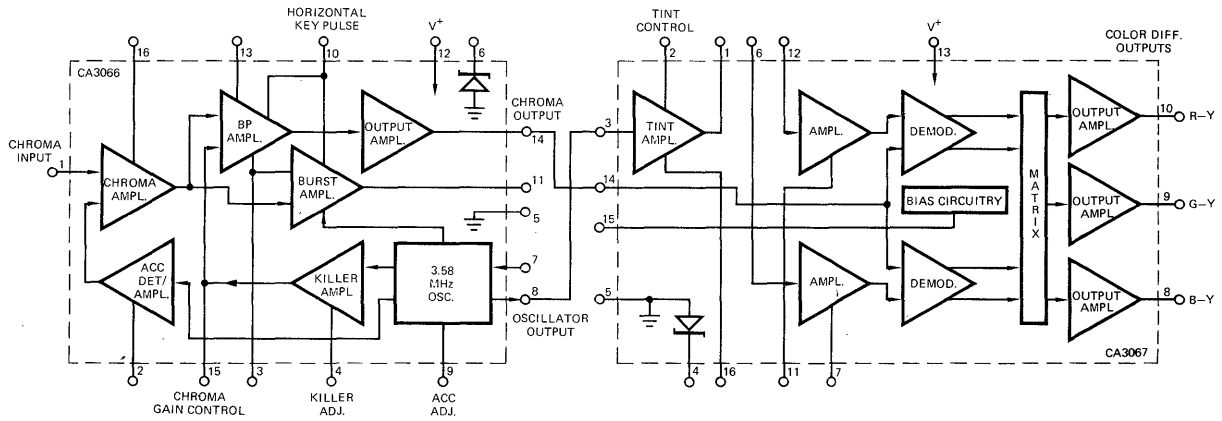
CA3066

- COMPLETE COLOR SYNC CIRCUIT
- BLANKED CHROMA AMPLIFIER
- CHROMA BAND-PASS AMPLIFIER
- LOW OUTPUT IMPEDANCE CHROMA DRIVER
- ACC DETECTOR-AMPLIFIER
- KILLER DETECTOR-AMPLIFIER
- DC CHROMA GAIN CONTROL
- ZENER DIODE FOR REGULATED VOLTAGE REFERENCE
- SHORT-CIRCUIT PROTECTION ON ALL TERMINALS

CA3067

- BALANCED CHROMA DEMODULATORS
- COLOR DIFFERENCE MATRIX
- DC TINT CONTROL
- THREE LOW OUTPUT IMPEDANCE DRIVERS FOR DIRECT COUPLING
- REFERENCE SUBCARRIER LIMITER
- ZENER DIODE FOR REGULATED VOLTAGE REFERENCE
- INTERNAL RF FILTERING

BLOCK DIAGRAM



CA3068
TELEVISION VIDEO IF SYSTEM

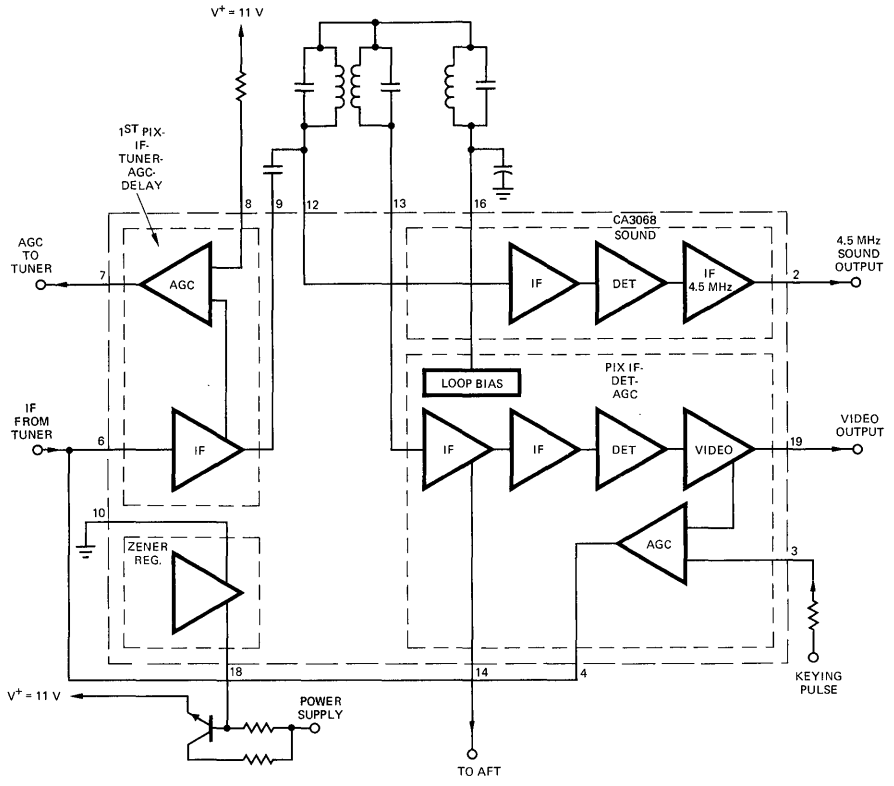
DESCRIPTION – The CA3068 is a monolithic integrated circuit that incorporates an entire video TV-IF subsystem on a single chip. Circuit innovations make it ideally suited for use in color and black-and-white TV receivers.

The primary functions performed by the IF subsystem are video IF amplification, linear detection, video output amplification, AGC from a keyed supply, AGC delay for tuner, sound carrier detection, sound carrier amplification, and a buffered AFT output. The advanced circuit design of the CA3068 also includes secondary functions for improved noise immunity and minimal airplane flutter. An isolated zener reference diode, incorporated in the IC, provides a convenient and economical means for controlling the regulated voltage supply. The inherent wide bandwidth capability (10-70 MHz) and high overall gain (87 dB) make the CA3068 suitable for other AM IF applications whose frequencies range within this bandwidth.

The CA3068 utilizes a unique 20-lead quad in-line plastic package. This package also includes a wrap-around shield that serves to minimize interlead capacitances.

- **HIGH-GAIN WIDE-BAND IF AMPLIFIER: 75 dB TYPICAL AT 45 MHz**
- **GAIN REDUCTION WITH EXCELLENT STABILITY: 50 dB TYPICAL AT 45 MHz**
- **VIDEO DETECTOR WITH LINEAR CHARACTERISTICS**
- **VIDEO AMPLIFIER; 12 dB GAIN**
- **IMPULSE NOISE LIMITER**
- **KEYED AGC WITH NOISE IMMUNITY CIRCUITS**
- **DELAYED AGC FOR TUNER**
- **BUFFERED AFT OUTPUT**
- **SEPARATE SOUND IF INTERCARRIER AMPLIFICATION**
- **SOUND CARRIER DETECTOR**
- **4.5 MHz SOUND CARRIER AMPLIFIER**
- **ISOLATED ZENER REFERENCE DIODE FOR REGULATED VOLTAGE SUPPLY**

BLOCK DIAGRAM

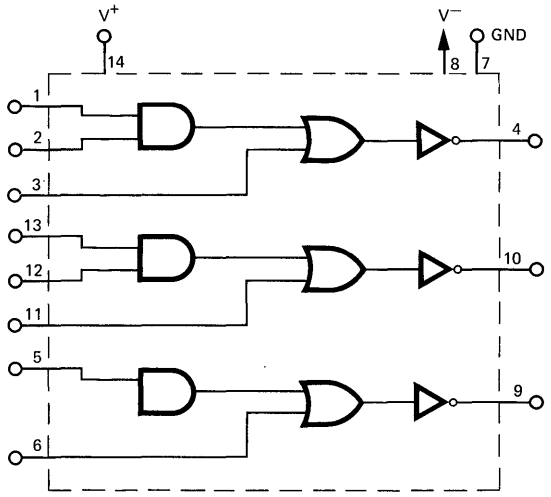


μA9616
TRIPLE EIA RS-232-C LINE DRIVER

DESCRIPTION – The μA9616 is a Triple EIA RS-232-C Line Driver which meets the specifications of EIA RS-232-C and CCIT V.24. External capacitors have been eliminated by internal slew rate limiting. All outputs are protected against RS-232-C fault conditions. A true inhibit function as required by the user has been provided. All inputs including the inhibit function are TTL compatible.

- **THREE CHANNELS PER PACKAGE**
- **NO EXTERNAL CAPACITORS REQUIRED FOR SLEW RATE LIMITING**
- **MEETS ALL RS-232-C SPECIFICATIONS**
- **TRUE INHIBIT FUNCTION**
- **MULTIPLE INPUTS**
- **MEETS CCITT V-24 SPECIFICATIONS**

BLOCK DIAGRAM

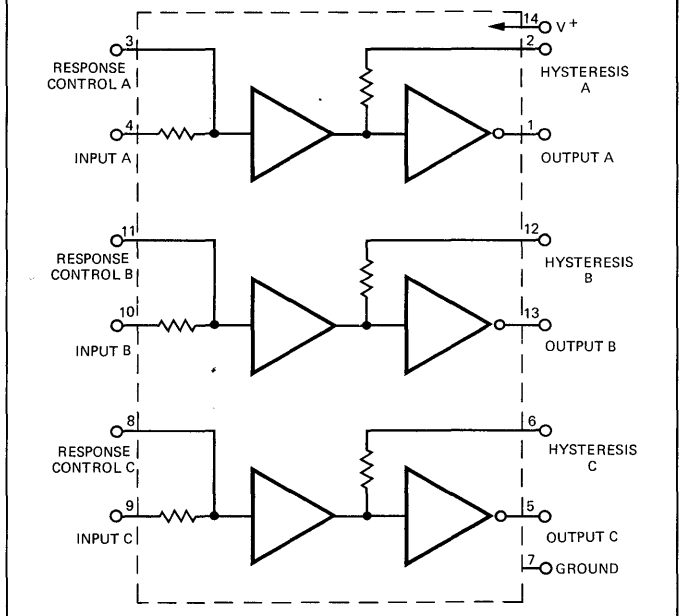


μA9617
TRIPLE EIA RS-232-C LINE RECEIVER

DESCRIPTION – The μA9617 is a triple line receiver designed to meet the terminator electrical requirements of EIA RS-232-C and CCITT V.24. It receives line signals produced by the μA9616, an EIA/CCIT driver, and converts them to TTL compatible logic levels. The inputs have a resistance between 3 kΩ and 7 kΩ and can withstand ±25 V. Each receiver can operate in either hysteresis or non-hysteresis (slicing) modes, and each receiver provides fail-safe operation as defined by Section 2.5 of RS-232-C. Noise immunity may be increased by connecting a capacitor between the response control pin and ground.

- **MEETS ALL EIA RS-232-C AND CCITT V.24 SPECIFICATIONS**
- **FAIL-SAFE OPERATION**
- **HYSTERESIS OR NON-HYSTERESIS MODE**
- **INDIVIDUAL RESPONSE CONTROLS**
- **TTL COMPATIBLE OUTPUT**
- **SINGLE +5 V SUPPLY**

BLOCK DIAGRAM

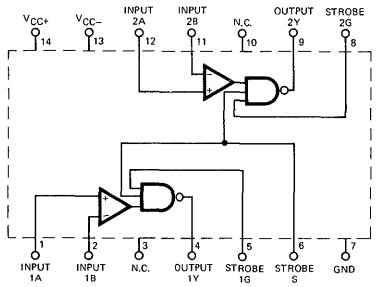


SN55/75107
SN55/75108
DUAL LINE RECEIVERS

DESCRIPTION — The SN55/75107 and SN55/75108 are high-speed, two channel line receivers with common voltage supply and ground terminals. They are designed to detect input signals of 25 mV (or greater) amplitude and convert the polarity of the signal into appropriate TTL-compatible output logic levels. They feature high input impedance and low input currents which induce very little loading on the transmission line making these devices ideal for use in party line systems. The receiver input common mode voltage range is ±3 V but can be increased to ±15 V by the use of input attenuators. Separate or common strobes are available. The SN55/75107 circuit features an active pull-up (totem pole output). The SN55/75108 circuit features an open collector output configuration that permits wired-OR connections. The receivers are designed to be used with the SN55/75109 and SN55/75110 line drivers. The SN55/75107 and SN75108 line receivers are useful in high-speed balanced, unbalanced and party line transmission systems and as data comparators.

- HIGH SPEED
- STANDARD SUPPLY VOLTAGES
- DUAL CHANNELS
- HIGH COMMON-MODE REJECTION RATIO
- HIGH INPUT IMPEDANCE
- HIGH INPUT SENSITIVITY
- INPUT COMMON-MODE VOLTAGE RANGE OF ±3 V
- SEPARATE OR COMMON STROBES
- TTL OR DTL DRIVE CAPABILITY
- WIRED-OR OUTPUT CAPABILITY
- HIGH D-C NOISE MARGINS

BLOCK DIAGRAM



SN55/75109
SN55/75110
DUAL LINE DRIVERS

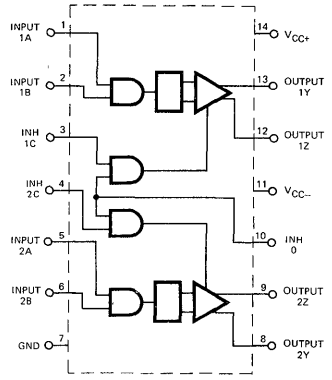
DESCRIPTION — The SN55/75109 and SN55/75110 are dual line drivers featuring independent channels with common voltage supply and ground terminals. The significant difference between the two drivers is in the output-current specification. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by appropriate logic levels on the inhibit inputs. The otuput current is nominally 6 mA for the SN55/75109 and 12 mA for the SN55/75110. System design determines which driver is best suited to a particular application.

The inhibit feature is provided so the circuits can be used in party-line or data-bus applications. A strobe or inhibitor, common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode, $I_{O(off)}$, is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The otuput impedance of the driver in the inhibited mode is very high—the output impedance of a transistor biased to cutoff.

The driver otuputs have a common-mode voltage range of −3 volts to +10 volts, allowing common-mode voltage on the line without affecting driver performance.

- HIGH SPEED
- STANDARD SUPPLY VOLTAGES
- DUAL CHANNELS
- TTL INPUT COMPATIBILITY
- CURRENT-MODE OUTPUT
  (6 mA or 12 mA TYPICAL)
- HIGH OUTPUT IMPEDANCE
- HIGH COMMON-MODE OUTPUT VOLTAGE RANGE
  (−3 V TO 10 V)
- INHIBITOR AVAILABLE FOR DRIVER SELECTION

BLOCK DIAGRAM



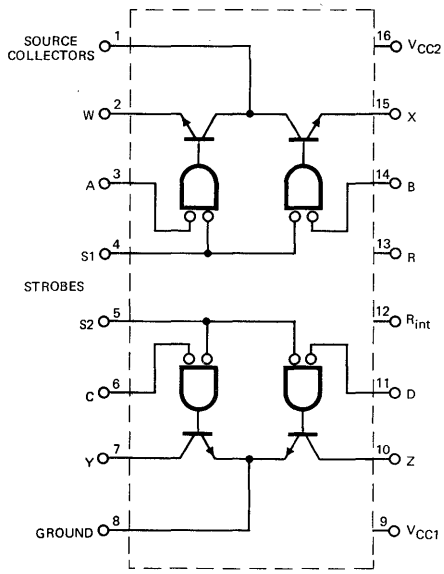
SN75325
MEMORY DRIVER

DESCRIPTION - The SN77325 is a monolithic integrated circuit memory driver with logic inputs and is designed for use with magnetic memories.

The devices contain two 600 mA source-switch pairs and two 600 mA sink-switch pairs. Source selection is determined by one of two logic inputs, and source turn-on is determined by the source strobe. Likewise, sink selection is determined by one of two logic inputs, and sink turn-on is determined by the sink strobe. This arrangement allows selection of one of the four switches and its subsequent turn-on with minimum time skew of the output current rise.

- **600 mA OUTPUT CAPABILITY**
- **FAST SWITCHING TIMES**
- **OUTPUT SHORT-CIRCUIT PROTECTION**
- **DUAL SINK AND DUAL SOURCE OUTPUTS**
- **MINIMUM TIME SKEW BETWEEN ADDRESS AND OUTPUT CURRENT RISE**
- **24 VOLT OUTPUT CAPABILITY**
- **SOURCE BASE DRIVE EXTERNALLY ADJUSTABLE**
- **TTL OR DTL COMPATIBILITY**
- **INPUT CLAMPING DIODES**
- **TRANSFORMER COUPLING ELIMINATED**
- **RELIABILITY INCREASED**
- **DRIVE-LINE LENGTHS REDUCED**
- **USE OF EXTERNAL COMPONENTS MINIMIZED**

LOGIC DIAGRAM



SN75451
DUAL PERIPHERAL DRIVERS

DESCRIPTION – The SN75451 is a versatile general purpose dual interface driver circuit that employs TTL or DTL logic. The SN75451 features two standard series 74 TTL gates and two high current, high voltage transistors which offer the system designer the flexibility to tailor the circuit to his application. The power output transistor is internally connected to the TTL gate but the collector remains uncommitted for high voltage applications. The SN75451 is useful in high speed logic buffers, power drivers, lamp drivers, relay drivers, line drivers, MOS drivers, clock drivers and memory drivers. The SN75451 is offered in a low cost mini-DIP package.

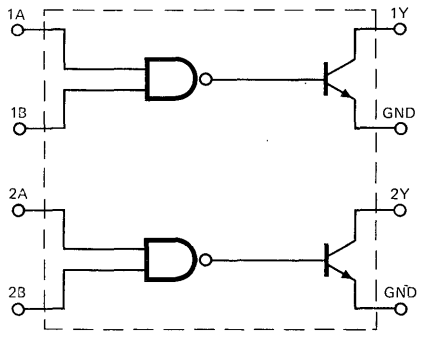
- **HIGH SPEED**
- **300 mA CURRENT CAPABILITY**
- **HIGH VOLTAGE CAPABILITY**
- **TTL OR DTL INPUT COMPATIBILITY**

TRUTH TABLE

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

H = High Level, L = Low Level

LOGIC DIAGRAM

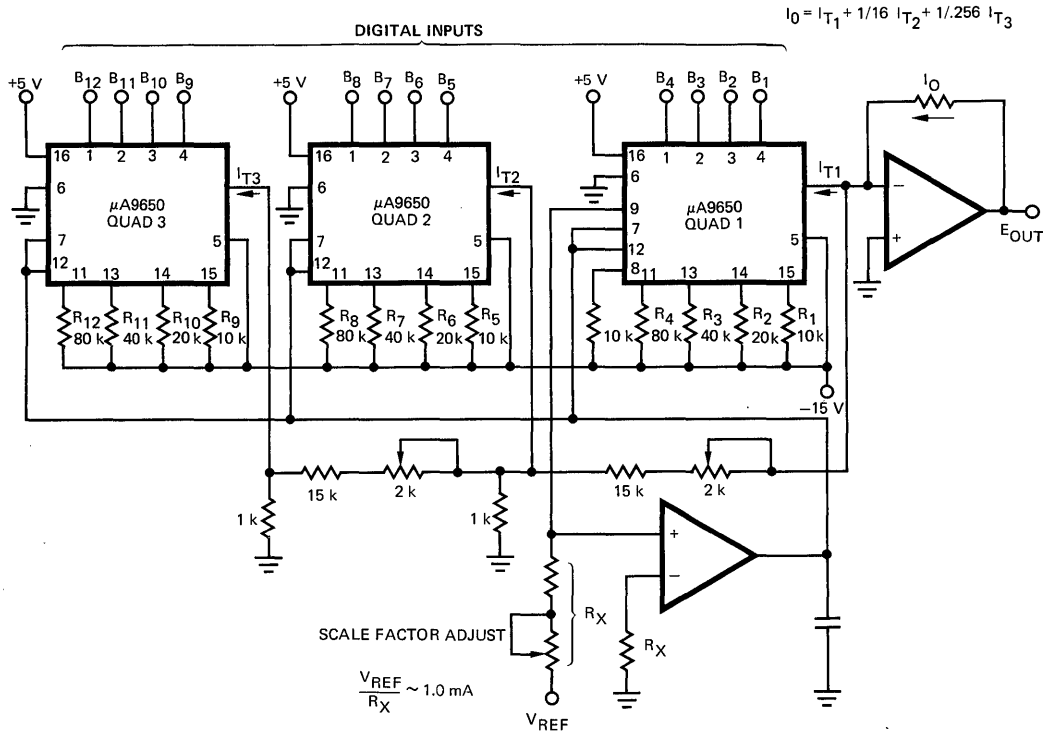


μA9650
4-BIT D/A AND A/D CURRENT SOURCE

DESCRIPTION – The μA9650 is a high speed, 4-bit precision current source, intended for use in D/A and A/D converters with up to 12-bit accuracy. It consists of a reference transistor and 4 logic operated precision current sources connected to a single output summing line. Logic inputs are fully TTL compatible.

- **200 ns SETTLING TIME (12 ± 1/2 LSB)**
- **STANDARD SUPPLY LEVELS**
- **VARIABLE BIT CURRENTS**
- **REFERENCE COMPENSATION**
- **TTL COMPATIBLE**

TYPICAL 12 - BIT DIGITAL-TO-ANALOG CONVERTER



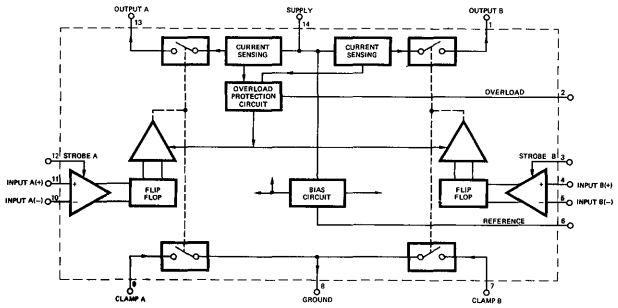
μA750
DUAL HIGH CURRENT COMPARATOR

DESCRIPTION – The μA750 is a dual high current comparator. The two comparators function completely independent; each has strobing capability, built-in hysteresis for positive switching, output current sinking capability and a high current source. The dual comparator operates over a wide supply range, has a separate reference voltage available for external circuitry bias and has adjustable excess current and chip temperature protection.

The device is designed for systems requiring dual comparator functions such as air conditioners, two-direction position controls and window detectors. Although primarily intended for systems with high load currents, the device will reduce package count in all systems using more than one comparator. Both comparator and strobe inputs are TTL compatible.

- **HIGH OUTPUT SOURCING CURRENT CAPABILITY**
- **POSITIVE SWITCHING BY MEANS OF BUILT-IN HYSTERESIS**
- **OUTPUT CURRENT SINKING CAPABILITY**
- **THERMAL AND EXCESS-CURRENT PROTECTIVE SHUT-DOWN, RESETTABLE BY INTERRUPTING SUPPLY CURRENT**
- **WIDE SUPPLY VOLTAGE RANGE**
- **REFERENCE VOLTAGE OUTPUT FOR ADDED CONVENIENCE**
- **OPERATES FROM SINGLE SUPPLY**

BLOCK DIAGRAM

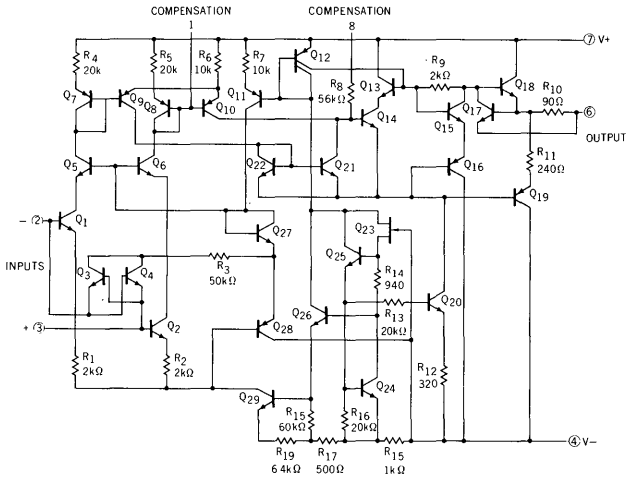


LM108/108A SERIES
HIGH PRECISION OPERATIONAL AMPLIFIER

DESCRIPTION – The LM108 series are high-precision operational amplifiers. Extremely high input impedance coupled with low noise input offsets and temperature drift are made possible through use of high-beta processing, making the device suitable for applications requiring high accuracy and low drift performance. The LM108A series is specially selected for extremely low offset voltage and drift, and high common mode rejection, making possible superior performance in applications where offset nulling is undesirable. Increased slew rate without performance compromise is available through use of feedforward compensation techniques, maximizing performance in high speed sample-and-hold circuits and precision high speed summing amplifiers, while the wide supply range and excellent supply voltage rejection assure maximum flexibility in voltage follower, summing, and general feedback applications.

- **GUARANTEED LOW INPUT CHARACTERISTICS**
- **HIGH INPUT IMPEDANCE**
- **LOW OFFSET CURRENT – 400 pA MAXIMUM**
- **LOW BIAS CURRENTS – 3.0 nA MAXIMUM**
- **OPERATION OVER WIDE SUPPLY RANGE**

EQUIVALENT CIRCUIT



Dice

LINEAR INTEGRATED CIRCUIT DICE POLICY

General Information

Fairchild Linear Integrated Circuits is proud to offer the most complete line of circuits in dice form in the industry. All are constructed using the Fairchild Planar* Epitaxial process. The chips are identical to those used in standard Fairchild assembled products.

These linear dice can be conveniently used in hybrid or module designs where size and cost savings are required.

Electrical Characteristics

Each chip is electrically tested at 25°C to DC parameters as evidenced by the probe marks on the bonding pads.

Quality Assurance

All Fairchild linear dice are visually inspected and conform to MIL-STD-883 Method 2010.1 Condition B as a minimum to a quality control level of 1-1/2% AQL.

As an aid to die attach, each die is gold backed. For protection in handling and assembly, each die has a glassivated coating over the metalization. Only the bonding pads are exposed.

Chip geometries and manufacturing processes may be improved periodically. However, such changes will not affect the electrical characteristics of the circuits.

Shipping Packages

Linear dice are packaged in containers with an anti-static sheet inserted between the lid and the dice. This anti-static sheet guards against electrostatic damage during shipment and storage.

The clear plastic carrier allows visual inspection of all the packaged dice. Each carrier is heat sealed within a transparent bag. A small piece of dehydrator paper with humidity indicating color is inserted in each bag prior to sealing.

Ordering Information

Minimum order quantity is 100 chips. All orders above 100 peices must be in 100 piece multiples.

Each Linear Integrated Circuit chip has its own 10 digit product code which completely describes the family, device type, and device number. The meaning of the digits and their position are as follows:

1. Generic Device Type — UXX7741XXD — Microcircuit
2. Microcircuit Family — UXX7741XXD — Linear Device
3. Device Number — UXX7741XXD — Device Type
4. Dice Indicator — UXX7741XXD — Dice

Note: The XX designation replaces the package type and temperature range.

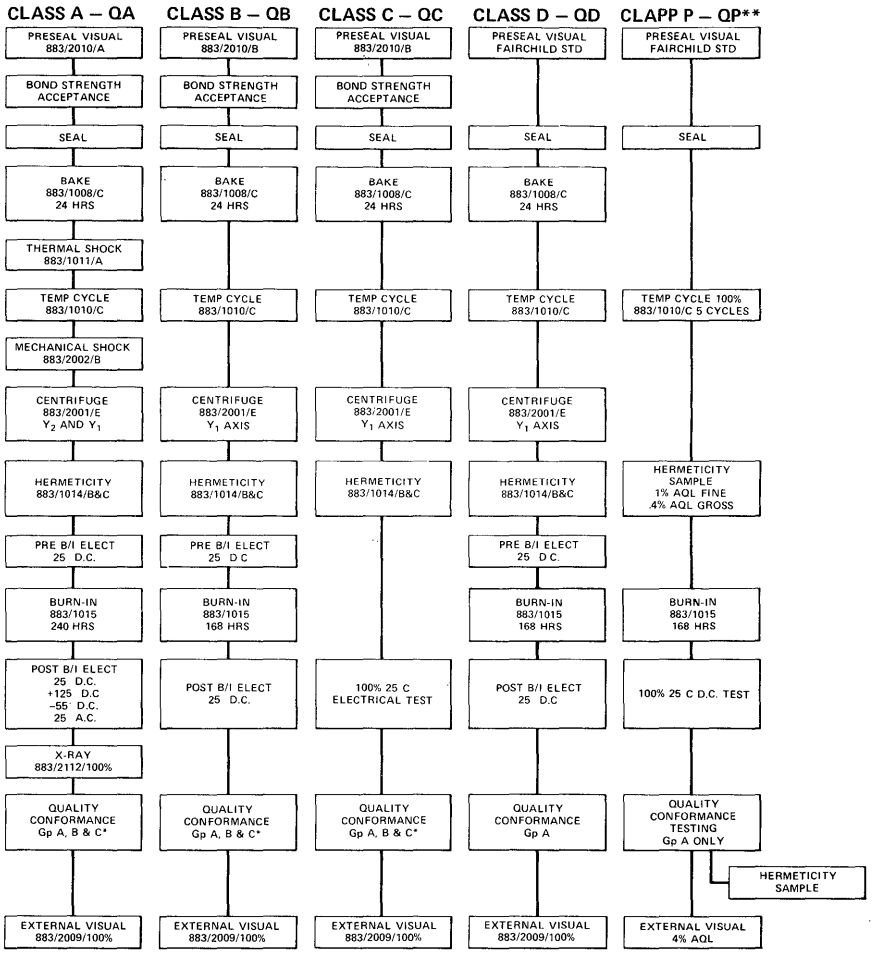
*Planar is a patented Fairchild process.

PRODUCT AVAILABLE IN DICE FORM

μA702	μA715	μA725	μA732	μA746	μA757	μA796	μA9622	CA3018	CA3045
μA703	μA716	μA726	μA733	μA747	μA777	μA9614	μA9624	CA3019	CA3054
μA709	μA719	μA727	μA734	μA748	μA780	μA9615	μA9625	CA3026	LM101A
μA710	μA722	μA729	μA739	μA749	μA781	μA9620	μA9626	CA3036	SN7525
μA711	μA723	μA730	μA741	μA754	μA792	μA9621	μA9627	CA3039	

Hi-Rel Unique 38510

PROCESS SUMMARY



* Group "B" is performed by generic type every 6 weeks.
Group "C" is performed by generic type every 12 weeks.

** "QP" devices are essentially Fairchild Standard product with 168 hr burn-in.
Fine leak is performed to an LTPD of "10" and gross leak is performed to an LTPD of "3". Flatpak have the following additional processing: Bake 883/1008/C 24 hrs and Centrifuge 883/2001/E.

The UNIQUE 38510 Program is written in accordance with MIL-M-38510 and MIL-STD-883. The Program establishes quality and reliability screening requirements to match the particular screening level required by the application.

The UNIQUE 38510 General Specification establishes the controls and reliability assurance levels for product screening. Five levels – QA, QB, QC, QD, and QP – of product screening are available.

Detailed electrical and specific device characteristics are specified for each family of devices in the Detail Specification.

FAMILY	DETAIL SPECIFICATION
Operational Amplifier	UNIQUE 38510/A1
Comparators	UNIQUE 38510/A2
Voltage Regulators	UNIQUE 38510/A3
Interface Circuits	UNIQUE 38510/12

The UNIQUE 38510 General Specification and Detail Specification are available upon request.

Devices available on the Program and marking are detailed on Page 302. For other LIC products that can be processed per the UNIQUE 38510 Program, check with your local Fairchild Sales Office.

QB and QP processed product is stocked for immediate delivery. Check with your local Fairchild Distributor or Fairchild Sales Office for delivery.

Qualified Products Code:

1st	Digit	Q	Indicates Qualified Line
2nd	Digit	A	Indicates Class A part
		B	Indicates Class B part
		C	Indicates Class C part
		D	Indicates Class D part (see para. 6.5)
		P	Indicates Class D Part (see para 6.5.1)
3rd	Digit	X	Part of four-digit code indicating die type
4th	Digit	X	
5th	Digit	X	
6th	Digit	X	

Number Options: These options apply to operations performed on each unit delivered:

OPTION 1	Lead form to dimensions in detail specification, followed by hermetic seal tests.
OPTION 2	Hot solder dip finish
OPTION 3	Read and record critical parameters before and after burn-in.
OPTION 4	Initial qualification, Group B&C quality conformance not required.
OPTION 5	Radiographic inspection shall be performed on all devices.
OPTION 6	Special marking required.
OPTION 7	Non-conforming variation—refer to procurement documents for details (must be negotiated with factory).

Letter Options: These options apply once per Purchase Order or line item and are considered Test Charges:

OPTION A	Group B testing shall be performed on customer's parts.
OPTION B	Group C testing shall be performed on customer's parts.
OPTION C	Generic data to be supplied from the latest completed lot.
OPTION D	UNIQUE 38510 program plan, pertinent to the device family being purchased, shall be supplied.

UNIQUE PROGRAM DEVICE PART NUMBER–MARKING CROSS REFERENCE

Product Code	Part Number & Marking	Product Code	Part Number & Marking
U5B7101311	Q/A17101BC	U6A7733312	Q/A17733BA
U6A7101311	Q/A17101BA	U3F7741312	Q/A17741BF
U3F7702312	Q/A17702BF	U5B7741312	Q/A17741BC
U5B7702312	Q/A17702BC	U6A7741312	Q/A17741BA
U3F7709312	Q/A17709BF	U5F7747312	Q/A17747BA
U5B7709312	Q/A17709BC	U7A7747312	Q/A17747BA
U6A7709312	Q/A16609BA	U6A7749312	Q/A17749BA
U3F7710312	Q/A27710BF	U4L961451X	Q/I29614BL
U5B7710312	Q/A27710BC	U7B961451X	Q/I29614BB
U6A7710312	Q/A27710BA	U4L961551X	Q/I29615BL
U3F7711312	Q/A27711BF	U7B961551X	Q/I29615BB
U5F7711312	Q/A27711BG	U3I962051X	Q/I29620BI
U5F7715312	Q/A17715BG	U6A962051X	Q/I29620BA
U6A7715312	Q/A17715BA	U3I962151X	Q/I29621BI
U5R7723312	Q/A37723BR	U6A962151X	Q/I29621BA
U6A7723312	Q/A37723BA	U3I962251X	Q/I29622BI
U5T7725312	Q/A17725BT	U6A962251X	Q/I29622BA
U3F7733312	Q/A17733BF	U3I962451X	Q/I29624BI
U5F7733312	Q/A17733BG	U6A962451X	Q/I29624BA

Application Information

The following is a list of selected linear integrated circuit application notes. For your convenience, they are organized by application note number and product type. The latest, complete Fairchild Semiconductor Application Literature Index is available from:

Fairchild Semiconductor
Technical Information Center
P.O. Box 880A
Mountain View, California 94040

SELECTED LIC APPLICATION NOTE INDEX BY NUMBER

SELECTED LIC APPLICATION NOTE INDEX BY PRODUCT

Ordering Information

DEVICE	PACKAGE See outline drawing section, page 309 ff.	ORDER NUMBER			
		0°C to +70°C	−55°C to +85°C	−20°C to +85°C	DICE (+25°C)
μA702	3F		U3F7702312		
	5B	U5B7702393	U5B7702312		
	6A	U6A7702393	U6A7702312		
	DICE				UXX7703XXD
μA703	5Z	U5Z7703394			
	DICE				UXX7703XXD
μA709	3F		U3F7709311 U3F7709312		
	5B	U5B7709393	U5B7709311 U5B7709312		
	6A	U6A7709393	U6A7709311 U6A7709312		
	DICE				UXX7709XXD
μA710	3F		U3F7710312		
	5B	U5B7710393	U5B7710312		
	6A	U6A7710393	U6A7710312		
	DICE				UXX7710XXD
μA711	3F		U3F7711312		
	5F	U5F7711393	U5F7711312		
	6A	U6A7711393	U6A7711312		
	DICE				UXX7711XXD
μA715	5F	U5F7715393	U5F7715312		
	6A	U6A7715393	U6A7715312		
	DICE				UXX7715XXD
μA716	5B	U5B7716393			
	DICE				UXX7716XXD
μA722	3M			U3M7722333 U3M7722334	
	DICE				UXX7722XXD
μA723	5R	U5R7723393	U5R7723312		
	6A	U6A7723393	U6A7723312		
	9A	U9A7723393			
	DICE				UXX7723XXD

DEVICE	PACKAGE See outline drawing section, page 309 ff.	ORDER NUMBER			
		0°C to +70°C	−55°C to +125°C	−20°C to +85°C	DICE (+25°C)
μA725	5T	U5T7725393	U5T7725312	U5T7725333	
	6A	U6A7725393	U6A7725312	U6A7725333	
	DICE				UXX7725XXD
		(0° TO +85°C)			
μA726	5U	U5U7726323	U5U7726312		
	DICE				UXX7726XXD
μA727	5U		U5U7727312	U5U7727333	
	DICE				UXX7727XXD
μA729	6A	U6A7729394			
	DICE				UXX7729XXD
μA730	5B	U5B7730393	U5B7730312		
	DICE				UXX7730XXD
μA732	6A	U6A7732394			
	DICE				UXX7732XXD
μA733	3F		U3F7733312		
	5F	U5F7733393	U5F7733312		
	6A	U6A7733393	U6A7733312		
	DICE				UXX7733XXD
μA734	5F	U5F7734393	U5F7734312		
	6A	U6A7734393	U6A7734312		
	9A	U9A7734393			
	9T	U9T7734393			
	DICE				UXX7734XXD
μA739	6A	U6A7739393			
	DICE				UXX7739XXD
μA740	5B	U5B7740393	U5B7740312		
μA741	3F		U3F7741312		
	5B	U5B7741393	U5B7741312		
	6A	U6A7741393	U6A7741312		
	9A	U9A7741393			
	9T	U9T7741391			
	DICE				UXX7741XXD
μA742	6A	U6A7742393			
μA746	5E	U5E7746394			
	6A	U6A7746394			
	DICE				UXX7746XXD
μA747	5F	U5F7747393	U5F7747312		
	7A	U7A7747393	U7A7747312		
	DICE				UXX7747XXD
μA748	3F		U3F7748312		
	5B	U5B7748393	U5B7748312		
	6A	U6A7748393	U6A7748312		
	9T	U9T7748393			
	DICE				UXX7748XXD

DEVICE	PACKAGE See outline drawing section, page 309 ff.	ORDER NUMBER			
		0°C to +70°C	−55°C to +125°C	−20°C to +85°C	DICE (+25°C)
μA749	5B 6A DICE	U5B7749394 U6A7749393	U6A7749312		UXX7749XXD
μA754	5E 6A DICE	U5E7754394 U6A7754394			UXX7754XXD
μA757	6A DICE	U6A7757393	U6A7757312		UXX7757XXD
μA760	5B 6A 9T DICE	U5B7760393 U6A7760393 U9T7760393	U5B7760312 U6A7760312		UXX77603XXD
μA767	6A	U6A7767394			
μA776	5B 6A	U5B7776393 U6A7776393	U5B7776312 U6A7776312		
μA777	5B 6A 9T DICE	U5B7777393 U6A7777393 U9T7777393	U5B7777312 U6A7777312		UXX7777XXD
μA780	6B DICE	U6B7780394			UXX7780XXD
μA781	6A DICE	U6A7781394			UXX7781XXD
μA795	6A	U6A7795393			
μA796	5E 6A DICE	U5E7796393 U6A7796393	U5E7796312 U6A7796312		UXX7796XXD
μA7805	GH GJ	UGH7805393 UGJ7805393			
μA7806	GH GJ	UGH7806393 UGJ7806393			
μA7808	GH GJ	UGH7808393 UGJ7808393			
μA7812	GH GJ	UGH7812393 UGJ7812393			
μA7815	GH GJ	UGH7815393 UGJ7815393			
μA7818	GH GJ	UGH7818393 UGJ7818393			
μA7824	GH GJ	UGH7824393 UGJ7824393			

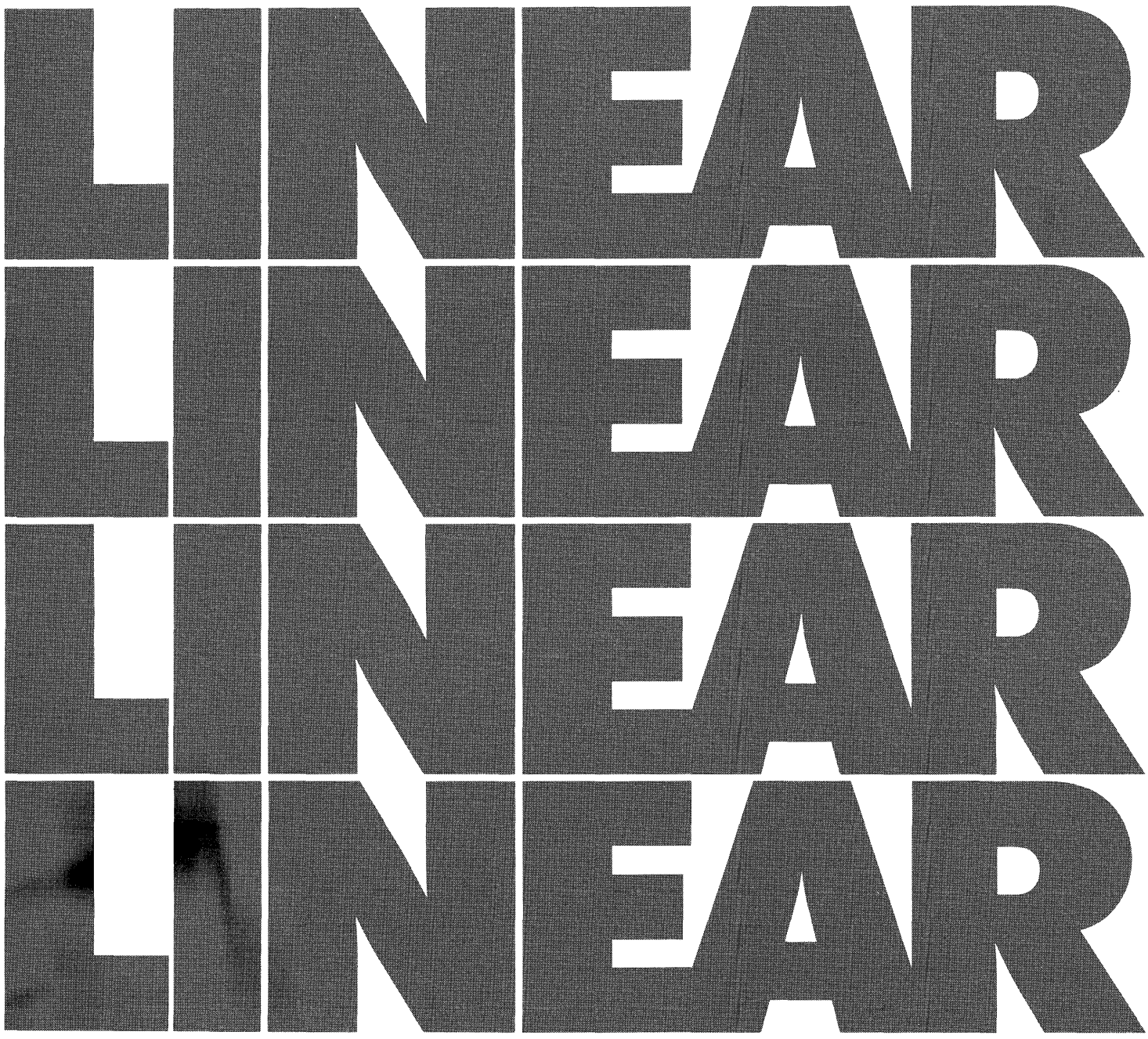
DEVICE	PACKAGE See outline drawing section, page 309 ff.	ORDER NUMBER			
		0°C to +75°C	−55°C to +125°C	−40°C to +85°C	DICE (+25°C)
μA9614	4L 7B DICE	U4L961459X U7B961459X	U4L961451X U7B961451X		UXX9614XXD
μA9615	4L 7B DICE	U4L961559X U7B961559X	U4L961551X U7B961551X		UXX9615XXD
μA9620	3I 6A DICE	U3I962059X U6A962059X	U3I962051X U6A962051X		UXX9620XXD
μA9621	3I 6A DICE	U3I962159X U6A962159X	U3I962151X U6A962151X		UXX9621XXD
μA9622	3I 6A DICE	U3I962259X U6A962259X	U3I962251X U6A962251X		UXX9622XXD
μA9624	3I 6A DICE	U3I962459X U6A962459X	U3I962451X U6A962451X		UXX9624XXD
μA9625	3I 6A DICE	U3I962559X U6A962559X	U3I962551X U6A962551X		UXX9625XXD
μA9644	7B	U7B964459X	U7B964451X		

DEVICE	PACKAGE See outline drawing section, page 309 ff.	ORDER NUMBER			
		0°C to +70°C	−55°C to +125°C	−40°C to +85°C	DICE (+25°C)
CA3018	5G DICE		CA3018		UXX7018XXD
CA3018A	5G		CA3018A		
CA3019	5E DICE		CA3019		UXX7019XXD
CA3026	5G DICE		CA3026		UXX7026XXD
CA3036	5E DICE		CA3036		UXX7036XXD
CA3039	5G DICE		CA3039		UXX7039XXD
CA3045	6A DICE		CA3045		UXX7045XXD

DEVICE	PACKAGE See outline drawing section, page 309 ff.	ORDER NUMBER			
		0°C to +70°C	−55°C to +125°C	−40°C to +85°C	DICE (+25°C)
CA3046	6A	CA3046			
CA3054	6A DICE	CA3054			UXX7054XXD
CA3064	5A			CA3064/5A	
CA3065	7F			CA3065/7F	
LM101D	6A		LM101D		
LM101H	5B		LM101H		
LM101AD	6A		LM101AD		
LM101AF	3F		LM101AF		
LM101AH	5B		LM101AH		
LM201D	6A	LM201D			
LM201H	5B	LM201H			

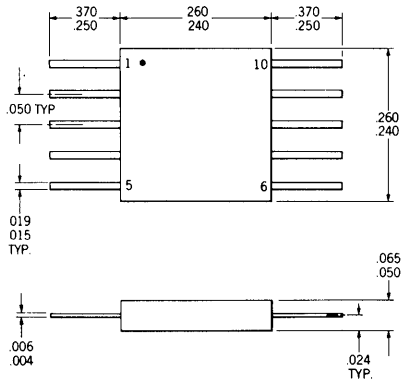
DEVICE	PACKAGE See outline drawing section, page 309 ff.	ORDER NUMBER			
		0°C to +70°C	−55°C to +125°C	−20°C to +85°C	DICE (+25°C)
LM201AD	6A			LM201AD	
LM201AF	3F			LM201AF	
LM201AH	5B			LM201AH	
LM301A	DICE				UXX7101XXD
LM301AD	6A	LM301AD			
LM301AH	5B	LM301AH			
LM301AN	9T	LM301AN			
LM109K	GJ		LM109K		
LM209K	GJ			LM209K	
LM309K	GJ	LM309K			
SN7524J	7B	SN7524J			
SN7525	DICE				UXX7525XXD
SN7525J	7B	SN7525J			
SN75450J	6A	SN75450J			
TAA630 (Formerly μA786)	6A 7F	TAA630/6A TAA630/7F			
TAA640 (Formerly μA784)	6A 7F	TAA640/6A TAA640/7F			
TBA550 (Formerly μA785/TAA700)	6B 7H	TBA550/6B TBA550/7H			

Package Outlines



3F

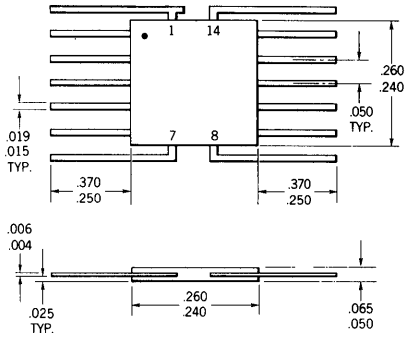
in accordance with JEDEC (TO-91) outline 10 Lead Cerpak



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.26 gram

3I

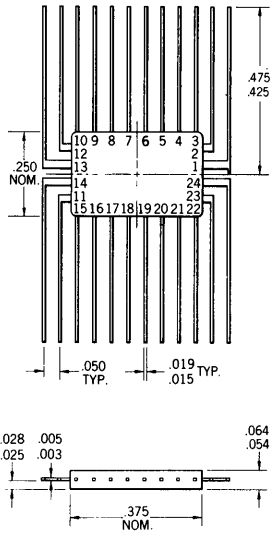
in accordance with JEDEC (TO-86) outline 14 Lead Cerpak



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.26 gram
Lead 1 orientation may be either tab or dot

3M

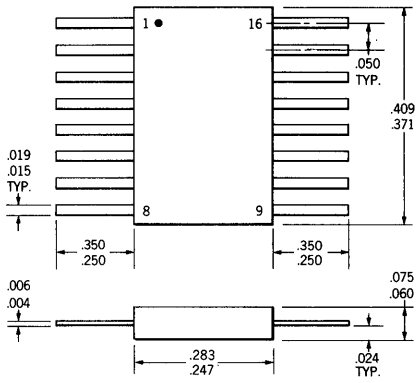
24 Lead Flat Pak



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.8 gram

4L

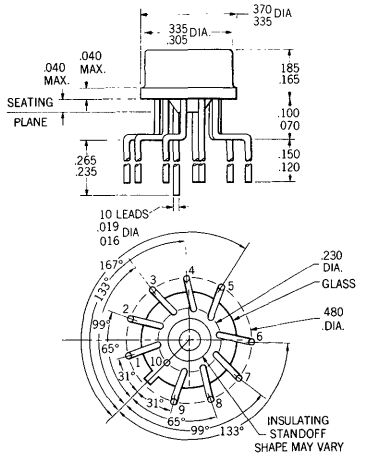
16 Lead BeO Cerpak



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.4 gram

5A

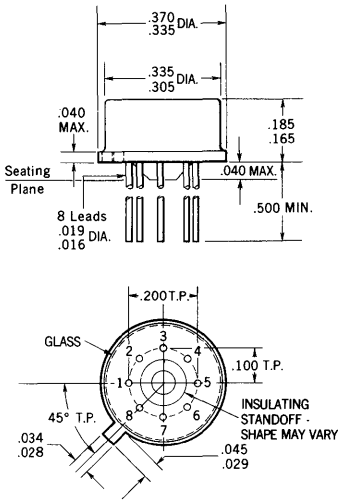
Similar* to JEDEC (TO-100) outline (15 mil kovar header)



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.22 gram
*This is a 5E package with the leads formed in assembly

5B

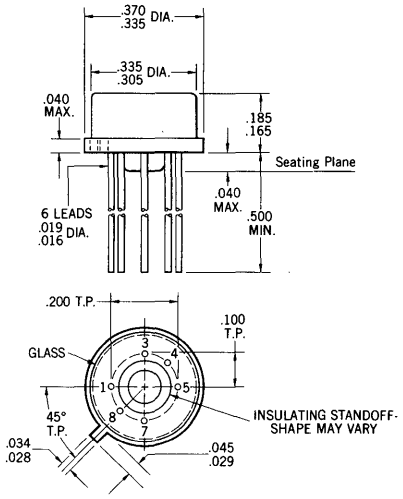
in accordance with JEDEC (TO-99) outline (15 mil kovar header)



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.22 gram
Seven leads through, lead No. 4 connected to case

5D

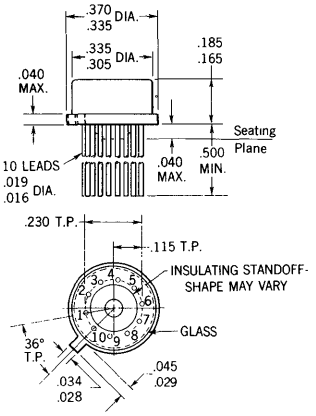
in accordance with JEDEC (TO-99) outline (15 mil kovar header)



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.12 gram
Five leads through, lead No. 4 is connected to case and leads No. 2 and 6 are omitted

5E

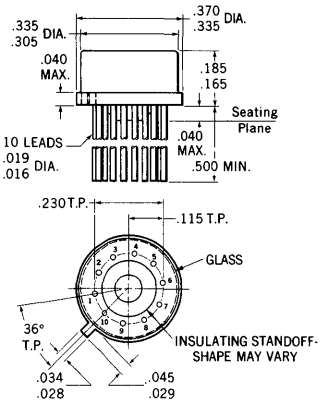
in accordance with JEDEC (TO-100) outline (15 mil kovar header)



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 gram
Ten leads through

5F

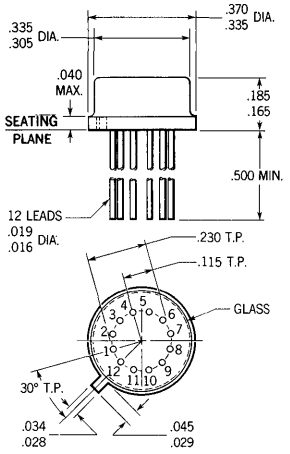
in accordance with JEDEC (TO-100) outline (15 mil kovar header)



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 gram
Nine leads through, lead No. 5 is connected to case

5G

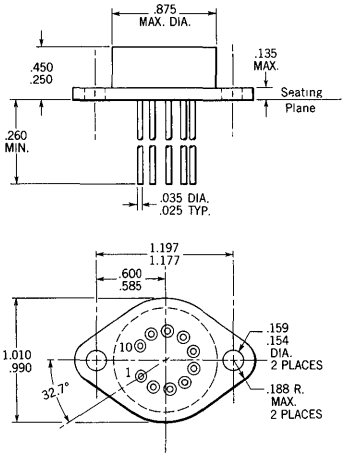
Similar* to JEDEC (TO-101) outline (15 mil kovar header)



NOTES
All dimensions in inches
Leads are gold-plated kovar
Similar to JEDEC 10-T01 except for no standoff
Package weight is 1.03 gram

5H

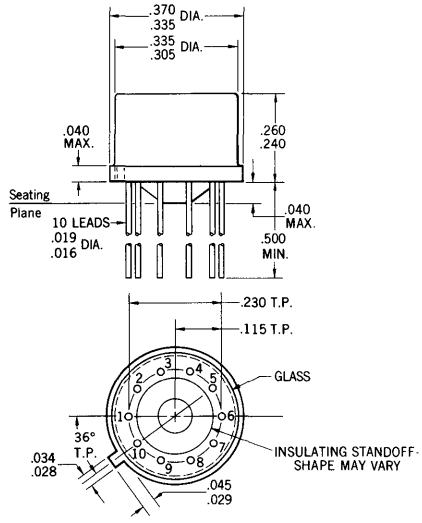
Similar* to JEDEC (TO-3) outline



NOTES
All dimensions in inches
Similar to JEDEC TO-3 except for 10 pins on 11 pin circle

5R

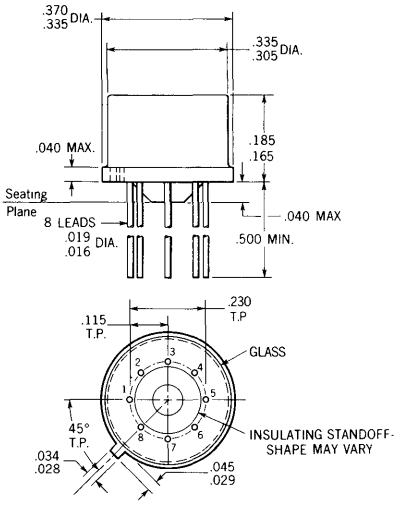
Similar* to JEDEC (TO-96) outline (15 mil kovar header)



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 gram
Nine leads through, lead No. 5 is connected to case
*Dimensions similar to JEDEC TO-96 except for standoff

5T

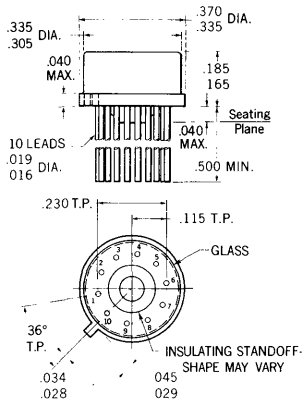
Similar* to JEDEC (TO-100) outline (15 mil kovar header)



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.22 gram
*Dimensions similar to JEDEC TO-100 except for 8 leads spaced 45° apart
Eight leads through

5U

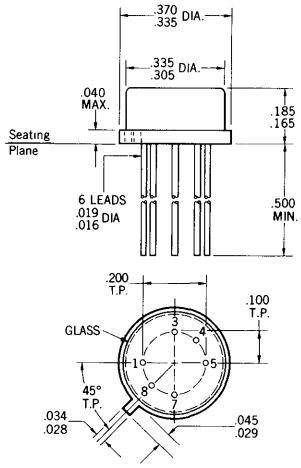
in accordance with JEDEC (TO-100) outline (15 mil kovar header)



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 gram
High RTH package
Ten leads through

5Z

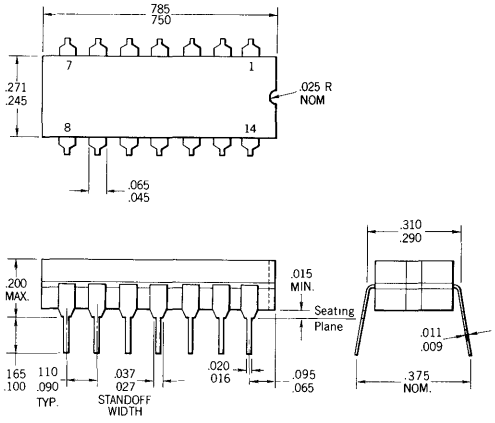
in accordance with JEDEC (TO-78) outline (50 mil kovar header)



NOTES
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.95 gram

6A DG

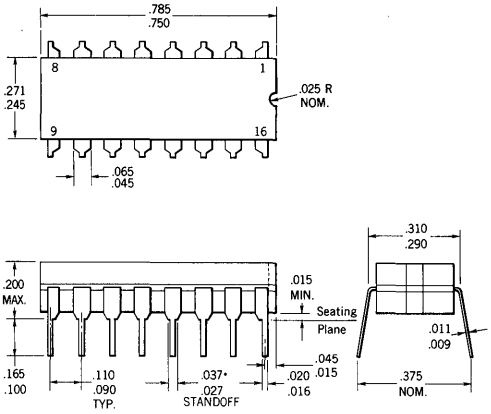
in accordance with JEDEC (TO-116) outline 14 Lead SSI Dual In-line



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams

16 Lead SSI Dual In-line

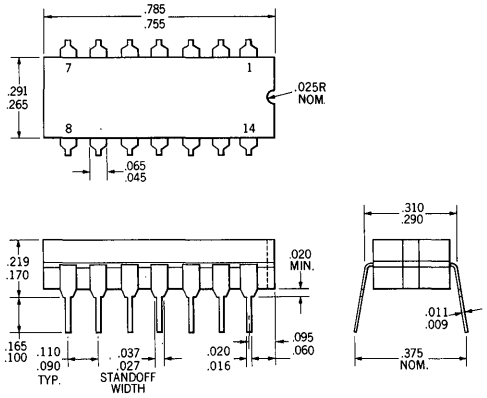
6B



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
*The .027/.037 dimension does not apply to the corner leads

Similar* to JEDEC (TO-116) outline 14 Lead MSI Dual In-line

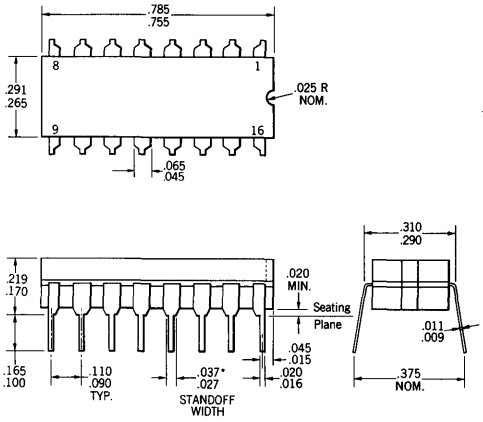
7A



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
*Similar to JEDEC TO-116 except for package width

16 Lead MSI Dual In-line

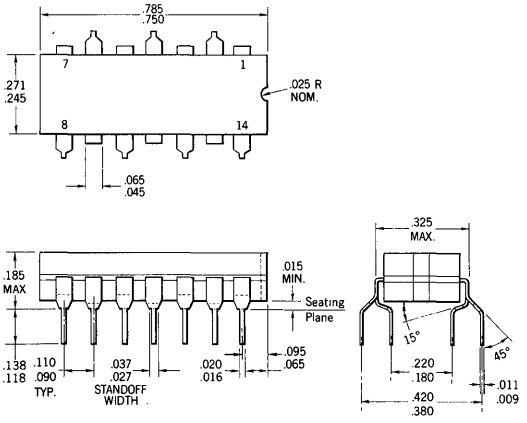
7B



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.2 grams
The .037/.027 dimension does not apply to the corner leads

Similar * to JEDEC (TO-116) outline 14 Lead SSI Quad In-Line

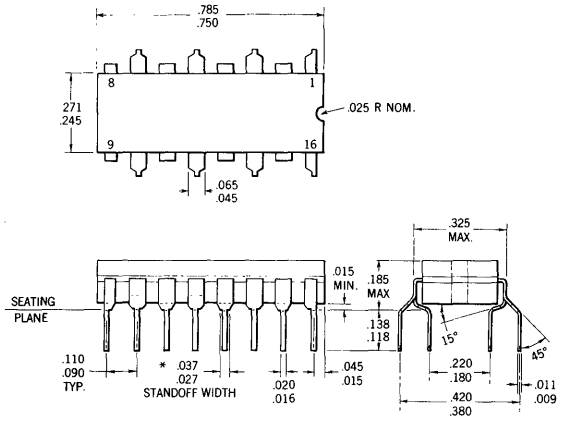
7F



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
*This is a 6A package with the leads formed in assembly

16 Lead SSI Quad** In-Line

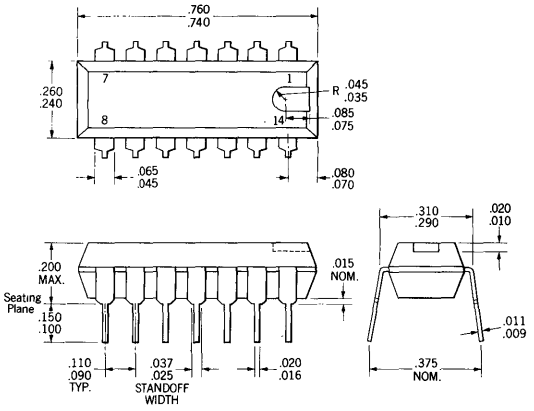
7H



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 2.0 grams
*The .037/.027 dimension does not apply to the corner leads
**This is a 6B package with the leads formed in assembly

in accordance with JEDEC (TO-116) outline 14 Lead Silicone Dual In-line

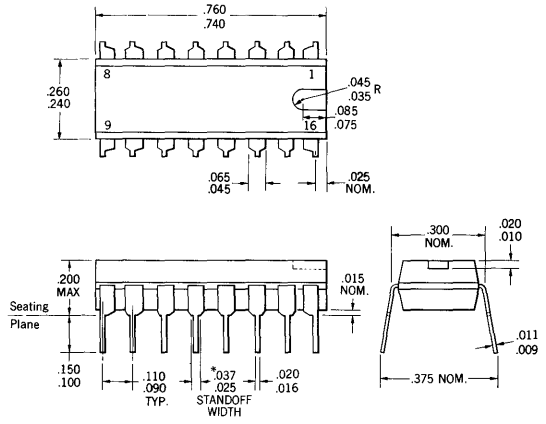
9A



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 0.9 gram

16 Lead Silicone Dual In-line

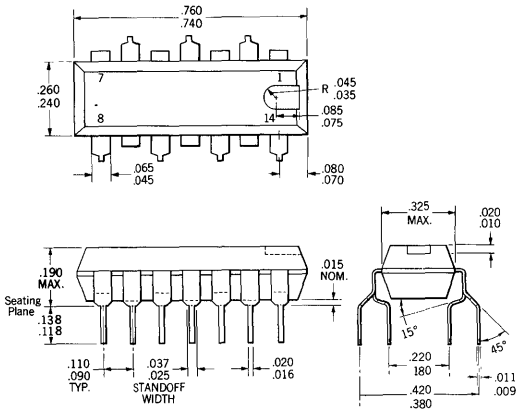
9B



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 0.9 gram
*The .037/.027 dimension does not apply to the corner leads

Similar* to JEDEC (TO-116) Outline 14 Lead Silicone Quad In-line

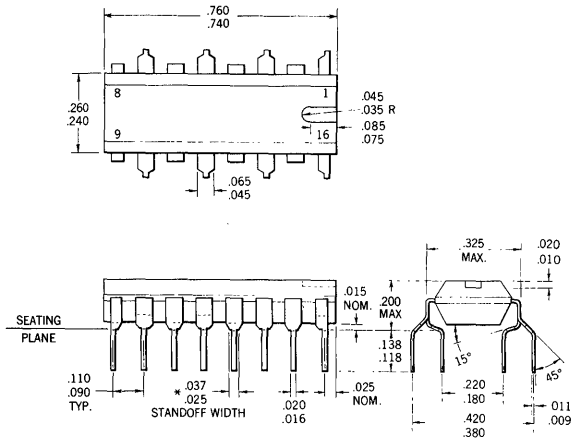
9C



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 0.9 gram
*This is a 9A package with the leads formed in assembly

16 Lead Silicone Quad** In-line

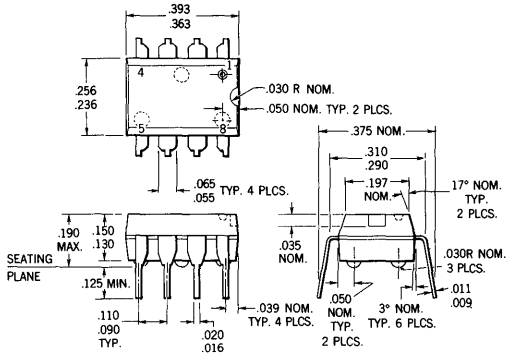
9D



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Leads are tin-plated kovar
Package weight is 0.9 gram
*The .037/.027 dimension does not apply to the corner leads
**This is a 9B package with the leads formed in assembly

8 Lead Plastic Dual In-line

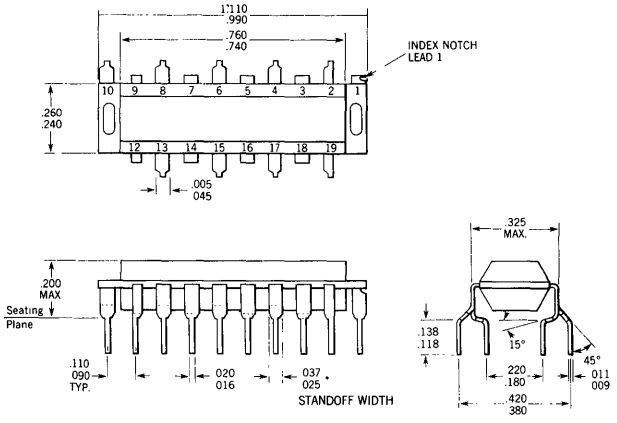
9T



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .300" centers
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 inch diameter lead
Package weight is 0.6 gram
Leads are tin or gold-plate kovar

20 Lead Plastic Quad In-line with RF Shield

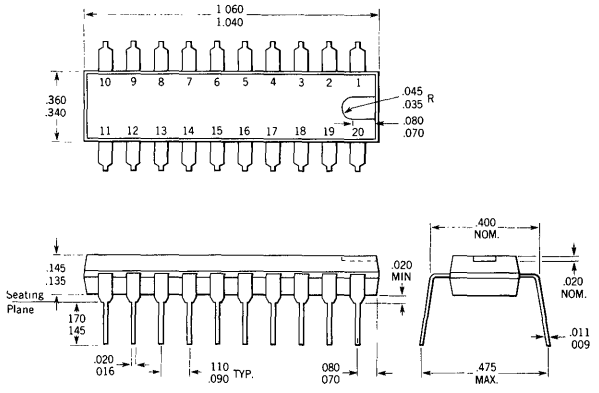
9Y



NOTES
All dimensions in inches
This is a 9B package with an extended lead frame, leads formed in assembly, and a wrap around RF shield
Leads 11 and 20 are omitted
Board-drilling dimensions should equal your practice for a .020 diameter lead
Leads are tin-plated kovar
Package weight is 1.5 grams
*The .037/.027 dimension does not apply to leads 1,2,9,10,12 and 19

20 Lead Plastic Dip

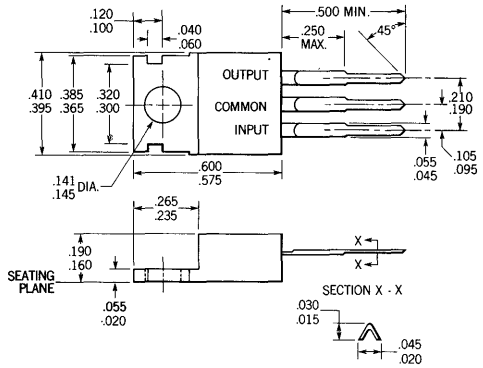
9Z



NOTES
All dimensions in inches
Leads are intended for insertion in hole rows on .400" centers.
They are purposely shipped with "positive" misalignment to facilitate insertion
Board-drilling dimensions should equal your practice for .020 diameter lead
Leads are tin-plated kovar

GH

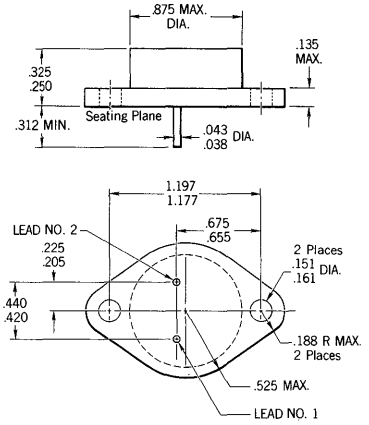
in accordance with JEDEC (TO-220) outline Plastic Power Package



NOTES
All dimensions in inches
Mounting tab is electrically connected to COMMON
Package is plastic with nickel-plated copper tab and leads
Package weight is 2.1 grams

GJ

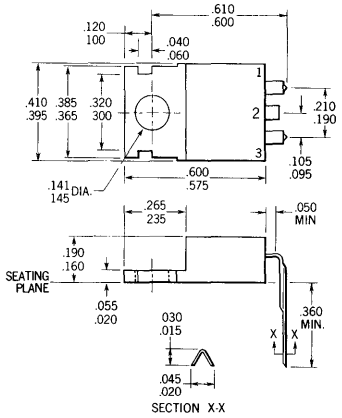
in accordance with JEDEC (TO-3) outline



NOTES
All dimensions in inches
Leads 1 and 2 electrically isolated from case
Case is third electrical connection (COMMON)
Leads are gold-plated copper cored kovar
Package weight is 7.4 grams

GM

in accordance with JEDEC (TO-220) outline Plastic Power Package



NOTES
All dimensions in inches
Center lead is in electrical contact with the mounting tab
Package is silicon plastic with nickel-plated copper tab and leads
Mechanically interchangeable with TO-66
Package weight is 2.1 grams

Glossary

FAIRCHILD LINEAR INTEGRATED CIRCUIT GLOSSARY

ABSOLUTE ERROR – The worst-case deviation from a straight line drawn through zero and the 25°C value of the full-scale output current.

ACC DETECTOR SENSITIVITY – The ratio of the incremental differential DC voltage change at the ACC Detector Output Terminals to the incremental change in peak-to-peak voltage at the ACC Detector Input Terminal for a specified burst input level, with the local oscillator locked.

ACQUISTION TIME – The time from change of input until last time output exceeds specified percent of final value.

APC DETECTOR SENSITIVITY – The ratio of the incremental differential DC voltage change at the APC Detector Output Terminals to the incremental change in relative phase at the APC Detector Input Terminal for a specified burst input level.

AVERAGE INPUT OFFSET CURRENT DRIFT – The change in input offset current divided by the change in ambient temperature producing it.

AVERAGE INPUT OFFSET VOLTAGE DRIFT – The change in input offset voltage divided by the change in ambient temperature producing it.

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET CURRENT – The ratio of the change in Input Offset Current over the operating temperature range to the temperature range.

AVERAGE TEMPERATURE COEFFICIENT OF INPUT OFFSET VOLTAGE – The ratio of the change in Input Offset Voltage over the operating temperature range to the temperature range.

AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE – The percentage change in output voltage for a specified change in ambient temperature.

BANDWIDTH – The frequency at which the differential gain is 3 dB below its low frequency value.

CLOSED LOOP VOLTAGE GAIN ERROR – Deviation from the theoretical closed loop voltage gain due to finite open loop voltage gain and input resistance, and non-zero output resistance.

COLOR-DIFFERENCE DEMODULATION ANGLE – A color-difference demodulation angle is defined as the instantaneous phase of the (+) Chroma input signal which produces the most positive voltage at the respective color-difference output with the phase of Reference "A" taken at 3 degrees and the phase of Reference "B" taken at 106 degrees.

(+) CHROMA INPUT – A composite chroma signal containing the burst at a phase of 180 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (+) Chroma input.

(–) CHROMA INPUT – A composite chroma signal containing the burst at a phase of 0 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (–) Chroma input.

COMMON MODE FIRING VOLTAGE – The CM input voltage that exceeds the dynamic range of the inputs with strobe enabled resulting in the output switching states.

COMMON MODE GAIN – A ratio of the differential output voltage to the change in applied input common mode voltage.

COMMON MODE INPUT RESISTANCE – The resistance looking into both inputs tied together.

COMMON MODE RECOVERY TIME – The time from the turn off of the CM signal to the analog input threshold of the earliest sense line pulse signal that can be processed normally. Processed normally refers to bi-polar signals greater than or less than the input threshold with a corresponding proper output.

DIFFERENTIAL INPUT VOLTAGE RANGE – The range of voltage between the input terminals for which operation within specifications is assured.

DIFFERENTIAL LOAD REJECTION – The ratio of the change in input offset voltage to the change in differential load current producing it.

DIFFERENTIAL INPUT RESISTANCE – The resistance looking into either input terminal with the other grounded.

DIFFERENTIAL OUTPUT VOLTAGE SWING – The peak differential output swing that can be obtained without clipping.

DIFFERENTIAL VOLTAGE GAIN – The ratio of the change in differential output voltage to the change in differential input voltage producing it.

DROPOUT VOLTAGE – The input-output voltage differential at which the circuit ceases to regulate against further reductions in input voltage.

EQUIVALENT INPUT COMMON MODE NOISE VOLTAGE – The change in input offset voltage due to common mode input noise.

EQUIVALENT INPUT RIPPLE VOLTAGE – The change in input offset voltage due to ripple on the applied supply voltage.

FULL SCALE OUTPUT CURRENT – The output current for all bits turned on.

GAIN MAXIMUM AVAILABLE (GMA) – This gain figure is the theoretical maximum power gain of an amplifier with conjugate matching at both the input and the output terminals and assumes no reverse transadmittance (feedback component) in the amplifier.

GAIN MAXIMUM STABLE (GMS) – This gain figure gives the maximum possible gain based on stability criteria only. This gain figure does not necessarily represent the realizable power gain of an amplifier. For unneutralized amplifiers, the maximum power gain realizable based on normal circuit tolerance is either (GMS - 6.0 dB) or GMA, whichever is smaller.

INPUT BIAS CURRENT – The average of the two input currents.

INPUT CAPACITANCE – The capacitance looking into either input terminal with the other grounded.

INPUT COMMON MODE REJECTION RATIO – The ratio of the input voltage range to the maximum change in input offset voltage over this range.

INPUT NOISE VOLTAGE – The square root of the mean square narrow-band noise voltage at the output divided by the measurement system gain with low source resistance.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals with the output at zero volts.

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT-OUTPUT VOLTAGE DIFFERENTIAL – The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operate.

INPUT RESISTANCE – The resistance looking into either input terminal with the other grounded.

INPUT VOLTAGE RANGE – The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

LARGE-SIGNAL VOLTAGE GAIN – The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

LINEARITY ERROR – The deviation from the theoretical response.

LINE REGULATION – The percentage change in output voltage for a specified change in input voltage.

LOAD REGULATION – The percentage change in output voltage for a specified change in load current.

LOGIC INPUT HIGH VOLTAGE – The minimum voltage allowed at a bit control gate to hold the bit off.

LOGIC INPUT LOW VOLTAGE – The maximum voltage allowed at a bit control gate to hold the bit on.

LONG TERM STABILITY – Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and power dissipation.

MAXIMUM POWER DISSIPATION – The maximum total device dissipation for which the regulator will operate within specifications.

NEGATIVE OUTPUT LEVEL – The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE SUPPLY CURRENT – The current required from the negative power supply to operate the device with no load.

OSCILLATOR CONTROL SENSITIVITY – The ratio of the incremental change in oscillator free running frequency to the incremental change in the differential DC voltage at the APC Detector Output Terminals.

OUTPUT COMMON MODE VOLTAGE – The average of the voltages at the two output terminals.

OUTPUT OFFSET VOLTAGE – The difference between the voltages at the two output terminals with the inputs grounded.

OUTPUT NOISE VOLTAGE – The rms output noise voltage with constant load and no input ripple.

OUTPUT RESISTANCE – The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

OUTPUT SHORT-CIRCUIT CURRENT – The maximum output current available from the amplifier with the output shorted to ground or to either supply.

OUTPUT SINK CURRENT – The maximum negative current that can be delivered by the comparator.

OUTPUT VOLTAGE RANGE – The range of output voltage over which the regulator will operate.

OUTPUT VOLTAGE SWING – The peak output swing, referred to zero, that can be obtained without clipping.

PEAK OUTPUT CURRENT – The maximum current that may flow into the output load without causing damage to the comparator.

POSITIVE OUTPUT LEVEL – The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

POSITIVE SUPPLY CURRENT – The current required from the positive power supply to operate the device with no load.

POWER CONSUMPTION – The DC power required to operate the amplifier with the output at zero and with no load current.

PROPAGATION DELAY – The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

QUIESCENT CURRENT – That part of input current to the regulator that is not delivered to the load.

REFERENCE VOLTAGE – The output of the reference amplifier measured with respect to the negative supply.

RESPONSE TIME – The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage overdrive.

RIPPLE REJECTION – The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

RISE TIME – The time required for an output voltage step to change from 10% to 90% of its final value.

SENSE VOLTAGE – The voltage between current sense and current limit terminals necessary to cause current limiting.

SETTING TIME – The time from output first reaching final value until last time output exceeds specified percent of final value.

SHORT CIRCUIT CURRENT LIMIT – The output current of the regulator with the output shorted to the negative supply.

SLEW RATE – The maximum rate of change of output under large signal condition.

STANDBY CURRENT DRAIN – The supply current drawn by the regulator with no output load and no reference voltage load.

STROBE CURRENT – The maximum current drawn by the strobe terminals when it is at the zero logic level.

STROBE DELAY – The time delay measured from strobe to output threshold with a signal present exceeding the input threshold.

STROBE RELEASE TIME – The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

STROBED OUTPUT LEVEL – The DC output voltage, independent of input voltage, with the voltage on the strobe terminal equal to or less than a minimum specified amount.

SUPPLY CURRENT – The current required from the power supply to operate the amplifier with no load and the output at zero.

SUPPLY REGULATION – The change in voltage at the Supply Terminal for a specified change in the V^+ voltage.

SUPPLY VOLTAGE REJECTION RATIO – The ratio of the change in input offset voltage to the change in supply voltage producing it.

SWITCHING SPEED – The time required to turn on the least significant bit.

TEMPERATURE STABILITY OF VOLTAGE GAIN – The maximum variation of the voltage gain over the specified temperature range.

THRESHOLD UNCERTAINTY – With all sense amps sharing the same input threshold less the uncertainty as a "0". This includes unit to unit, power supply and temperature variations.

THRESHOLD VOLTAGE – The typical referred to input voltage which determines whether an input is a "1" or a "0". A signal whose magnitude is greater than the threshold level is sensed as a logic "1" and a signal whose magnitude is less as a "0".

TOTAL HARMONIC DISTORTION – The ratio of the sum of the amplitudes of all signals harmonically related to the fundamental, and the amplitude of the fundamental signal.

ZERO SCALE OUTPUT CURRENT – The output current for all bits turned off.