Field Effect Transistors

Analog Switches
Amplifiers
Epoxy

FIELD EFFECT TRANSISTORS NUMERICAL INDEX

ANALOG SWITCHES SELECTION GUIDE

Type Number	Mode and Construction	Polarity	$I_{D(on)}$ mA (min)	$I_{D(on)}$ mA (max)	$I_{D(off)}$ nA (typ)	$R_{ds(on)}$ ohms (max)	Comments
2N4381	D J/FET	P	3	12	—	350	Direct complement to FT0654.
2N4382	D J/FET	P	10	30	—	350	
2N5020	D J/FET	P	.3	1.2	—	1000	Low current, low pinch-off
2N5021	D J/FET	P	1	3.5	—	1000	applications.
FT0654A	D J/FET	N	10	40	—	250	50 volt BV_{GSS}.
FT0654C	D J/FET	N	3	12	—	350	50 volt BV_{GSS}.
FT0654E	D J/FET	N	1	4	—	600	50 volt BV_{GSS}.
FT0655A	D J/FET	N	50	—	.1	25	Low on-resistance switch.
FT0655B	D J/FET	N	15	—	.1	50	Low on-resistance switch.
FT0655E	D J/FET	N	3	—	.1	100	Low on-resistance switch.

E = Enhancement Mode
D = Depletion Mode

ANALOG SWITCHES NUMERICAL INDEX

AMPLIFIERS — LOW AND HIGH FREQUENCY SELECTION GUIDE

Type Number	Mode and Construction	Polarity	Y_{fs} (min) mmhos	I_{GSS} nA (max)	$I_{DSS}/I_{D(on)}$ mA (min)	$I_{DSS}/I_{D(on)}$ mA (max)	Comments
2N3277	D J/FET	P	.1	.4	.15	.5	Low gain at low current.
2N3278	D J/FET	P	.15	.4	.4	.9	
2N4381	D J/FET	P	2.0	1.0	3	12	Low noise audio amplifier.
2N4382	D J/FET	P	4.0	1.0	10	30	
2N5020	D J/FET	P	1.0	1.0	.3	1.2	Low noise at low current.
2N5021	D J/FET	P	1.5	1.0	1	3.5	
FT0654A	D J/FET	N	4.5	.1	10	40	Low noise audio amplifier.
FT0654C	D J/FET	N	3.5	.1	3	12	Low noise audio amplifier.
FT0654E	D J/FET	N	2.0	1.0	1	4	Low noise audio amplifier.
FT0655A-F	D J/FET	N	10.0	1.0	—	—	Extremely high gain amp.

E = Enhancement Mode
D = Depletion Mode

AMPLIFIERS NUMERICAL INDEX

EPOXY FET'S SELECTION GUIDE

Type Number	Mode and Construction	Polarity	I_{DSS} mA (min)	I_{DSS} mA (max)	Y_{fs} (min) mmhos	$R_{ds(on)}$ (max) ohms	Comments
2N4342	D J/FET	P	4	12	4.0	350	Low noise audio amplifier.
2N4343	D J/FET	P	10	30	2.0	700	Low noise audio amplifier.
2N4360	D J/FET	P	3	30	2.0	700	Low cost FET.
2N5033	D J/FET	P	.3	3.5	1.0	1300	Low current, low pinch off applications.
2N5163	D J/FET	N	1	40	2.0	500	Low cost FET.
FE0654A	D J/FET	N	10	40	4.5	250	Low noise audio amplifier.
FE0654B	D J/FET	N	3	12	3.5	300	Low noise audio amplifier.
FE0654C	D J/FET	N	1	4	2.0	500	Low current, low pinch off applications.
FE0655A	D J/FET	N	50	—	40.0*	25	Extremely high gain, general purpose amplifier.
FE0655B	D J/FET	N	15	—	20.0*	50	General purpose, low frequency amplifier.
FE0655C	D J/FET	N	3	—	10.0*	100	General purpose, low frequency amplifier.

* = Typical Y_{fs}
E = Enhancement Mode
D = Depletion Mode
GP = Gate Protected MOS/FET

EPOXY FET'S NUMERICAL INDEX

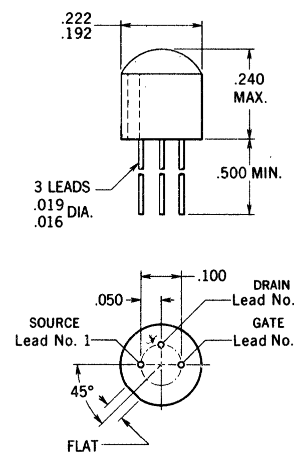
FE0654A • FE0654B • FE0654C

N-CHANNEL FIELD-EFFECT TRANSISTORS

DIFFUSED SILICON PLANAR* II TRANSISTORS

- **LOW COST EPOXY PACKAGE**
- **LOW NOISE** . . . . $e_n = 50\ nV/\sqrt{Hz}$ **(MAX.) AT 1.0 kHz**
- **HIGH GAIN**
  - **FE0654A** . . . . $Y_{fs} > 4{,}500; < 9{,}000\ \mu mhos$
- **LOW LEAKAGE**
  - **FE0654A** . . . . $I_{GSS} < 10\ nA$
- **HIGH VOLTAGE** . . . . $BV_{GSS} > 25$ **VOLTS**
- **LOW ON-RESISTANCE**
  - **FE0654A** . . . . $r_{ds(on)} < 250\ \Omega$
- **NARROW CURRENT RANGES**
  - **FE0654A** . . . . $I_{DSS} = 10$ **mA (MIN.) 40 mA (MAX.)**
  - **FE0654B** . . . . $I_{DSS} = 3.0$ **mA (MIN.) 12 mA (MAX.)**
  - **FE0654C** . . . . $I_{DSS} = 1.0$ **mA (MIN.) 4.0 mA (MAX.)**

PHYSICAL DIMENSIONS
In accordance with JEDEC (TO-106) outline



NOTES: All dimensions in inches
All leads electrically isolated from case
Package weight is 0.31 gram. Package is electrically non-conductive material

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

Storage Temperature	−55°C to +125°C
Operating Junction Temperature	+125°C
Lead Temperature (Soldering, 10 second time limit)	+260°C

Maximum Power Dissipation (Note 2)

Total Dissipation at 25°C Ambient Temperature	0.2 Watt

Maximum Voltages and Current

V_{SG}	Source to Gate Voltage	25 Volts
V_{DS}	Drain to Source Voltage	25 Volts
V_{DG}	Drain to Gate Voltage	25 Volts
I_G	Gate Current	50 mA

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTICS	FE0654A MIN.	FE0654A TYP.	FE0654A MAX.	FE0654B MIN.	FE0654B TYP.	FE0654B MAX.	FE0654C MIN.	FE0654C TYP.	FE0654C MAX.	UNIT	TEST CONDITIONS
Y_{fs}	Forward Transadmittance (f = 1.0 kHz)	4,500	6,100	9,000	3,500	5,100	8,000	2,000	4,900	6,000	μmhos	$V_{DS} = 15$ V, $V_{GS} = 0$
e_n	Equivalent Input Noise Voltage (f = 1.0 kHz, BW = 150 Hz)		10	50		10	50			50	$nV/\sqrt{Hz}$	$V_{DS} = 15$ V, $I_D = 1.0$ mA
$r_{ds(on)}$	Drain "ON" Resistance (f = 1.0 kHz)		155	250		220	350		300	600	Ohms	$V_{GS} = 0$, $I_D = 0$
I_{DSS}	Drain Current	10	16.5	40	3.0	7.8	12	1.0	2.75	4.0	mA	$V_{DS} = 15$ V, $V_{GS} = 0$
$V_{GS(off)}$	Gate to Source Cutoff Voltage		−4.3	−8.0		−2.5	−4.0		−1.0	−2.5	Volts	$V_{DS} = 15$ V, $I_D = 1.0\ \mu A$
C_{iss}	Input Capacitance (f = 1.0 MHz)		11	20		11	20		11	20	pF	$V_{DS} = 15$ V, $V_{GS} = 0$
Y_{OS}	Output Admittance (f = 1.0 kHz)		52			27			24		μmhos	$V_{DS} = 15$ V, $V_{GS} = 0$
BV_{GSS}	Gate to Source Breakdown Voltage	−25			−25			−25			Volts	$I_G = 1.0\ \mu A$, $V_{DS} = 0$
C_{rss}	Reverse Transfer Capacitance (f = 1.0 MHz)		2.0	5.0		2.0	5.0		2.0	5.0	pF	$V_{DS} = 15$ V, $V_{GS} = 0$
I_{GSS}	Gate Reverse Current			10			10			10	nA	$V_{GS} = -15$ V, $V_{DS} = 0$

Additional Electrical Characteristics on page 2

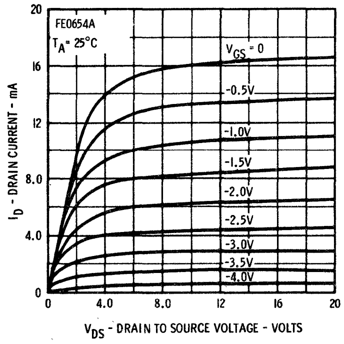
*Planar is a patented Fairchild process.

NOTES:
(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
(2) This rating gives a maximum junction temperature of 125°C and junction to ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).

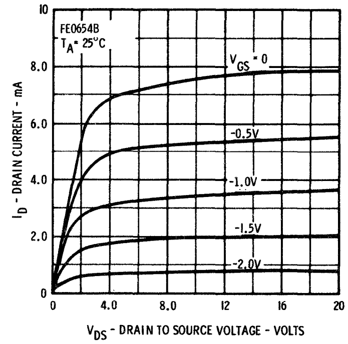
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

TYPICAL ELECTRICAL CHARACTERISTICS

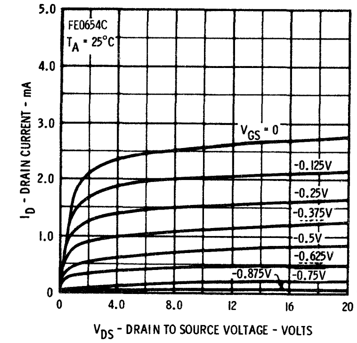
DRAIN CHARACTERISTICS



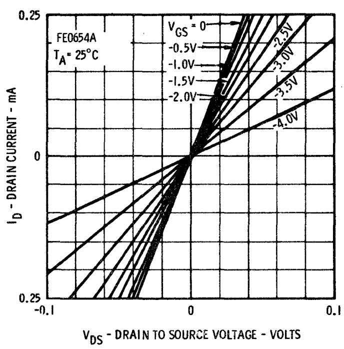
DRAIN CHARACTERISTICS



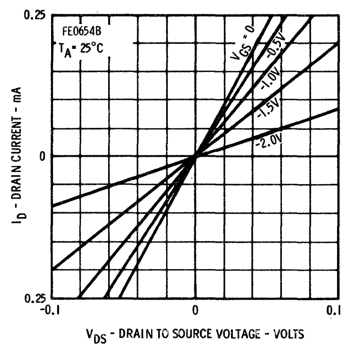
DRAIN CHARACTERISTICS



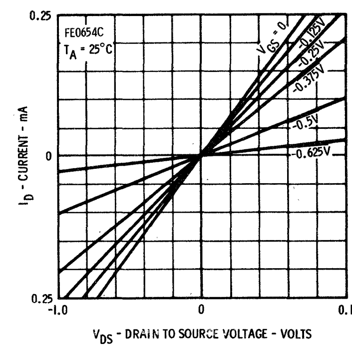
LOW VOLTAGE DRAIN CHARACTERISTICS



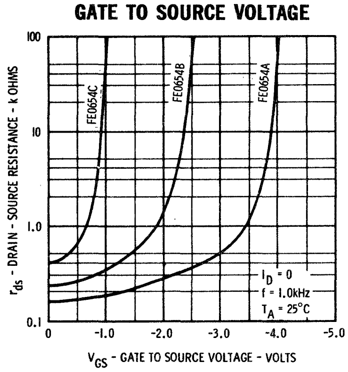
LOW VOLTAGE DRAIN CHARACTERISTICS



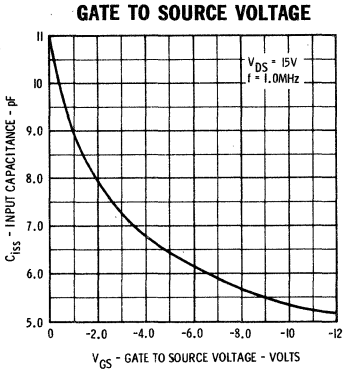
LOW VOLTAGE DRAIN CHARACTERISTICS



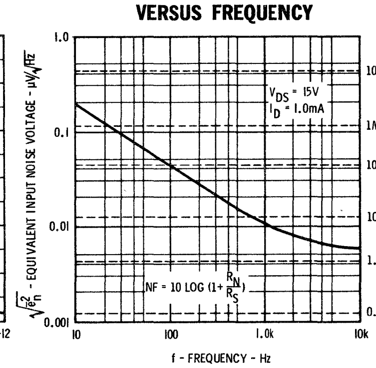
DRAIN-SOURCE RESISTANCE VERSUS GATE TO SOURCE VOLTAGE



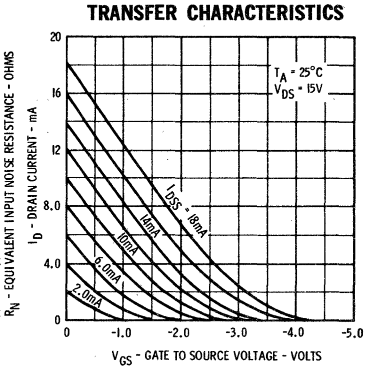
INPUT CAPACITANCE VERSUS GATE TO SOURCE VOLTAGE



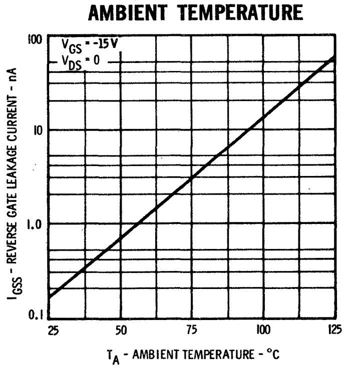
EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



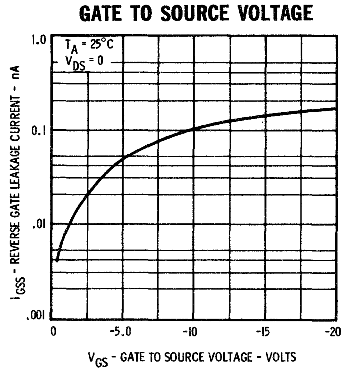
TRANSFER CHARACTERISTICS



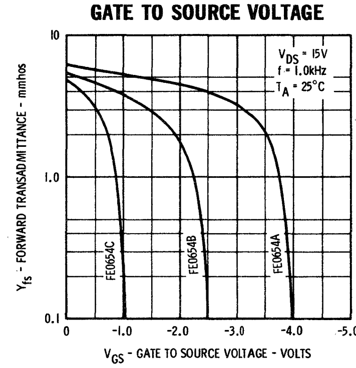
REVERSE GATE LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE



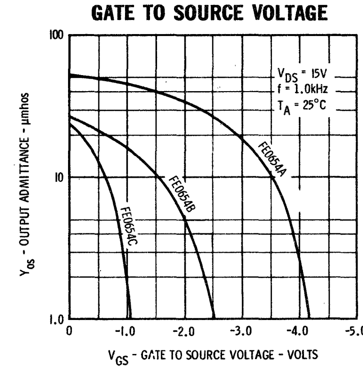
REVERSE GATE LEAKAGE CURRENT VERSUS GATE TO SOURCE VOLTAGE



FORWARD TRANSADMITTANCE VERSUS GATE TO SOURCE VOLTAGE



OUTPUT ADMITTANCE VERSUS GATE TO SOURCE VOLTAGE



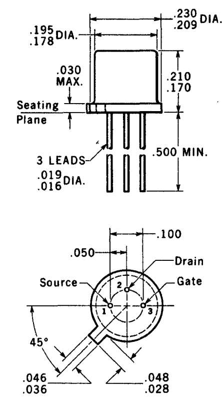
FT0654A THROUGH FT0654E

N-CHANNEL FIELD-EFFECT TRANSISTORS

DIFFUSED SILICON PLANAR* II TRANSISTORS

- **LOW NOISE . . . . $e_n = 50\ nV/\sqrt{Hz}$ (MAX.) AT 1.0 kHz**
- **HIGH GAIN**
  - **FT0654A & B . . . . $Y_{fs} > 4{,}500; < 9{,}000\ \mu mhos$**
- **LOW LEAKAGE**
  - **FT0654A & C . . . . $I_{GSS} < 100\ pA$**
- **HIGH VOLTAGE . . . . $BV_{GSS} > 50$ VOLTS**
- **LOW ON-RESISTANCE**
  - **FT0654A & B . . . . $r_{ds(on)} < 250\ \Omega$**
- **NARROW CURRENT RANGES**
  - **FT0654A & B . . . . $I_{DSS} = 10$ mA (MIN.) 40 mA (MAX.)**
  - **FT0654C & D . . . . $I_{DSS} = 3.0$ mA (MIN.) 12 mA (MAX.)**
  - **FT0654E . . . . $I_{DSS} = 1.0$ mA (MIN.) 4.0 mA (MAX.)**

PHYSICAL DIMENSIONS
in accordance with
JEDEC (TO-18) outline



NOTES: All dimensions in inches
Leads are gold-plated kovar
Gate internally connected to case
Package weight is 0.43 gram

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+175°C
Lead Temperature (Soldering, 10 second time limit)	+260°C

Maximum Power Dissipation (Note 2)

Total Dissipation at 25°C Ambient Temperature	0.3 Watt

Maximum Voltages and Current

V_{SG}	Source to Gate Voltage	50 Volts
V_{DS}	Drain to Source Voltage	50 Volts
V_{DG}	Drain to Gate Voltage	50 Volts
I_G	Gate Current	50 mA

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTICS	FT0654A & FT0654B MIN.	TYP.	MAX.	FT0654C & FT0654D MIN.	TYP.	MAX.	FT0654E MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Y_{fs}	Forward Transadmittance (f = 1.0 kHz)	4,500	6,100	9,000	3,500	5,100	8,000	2,000	4,900	6,000	μmhos	$V_{DS} = 20$ V, $V_{GS} = 0$
e_n	Equivalent Input Noise Voltage (f = 1.0 kHz, BW = 150 Hz)		10	50		10	50			50	$nV/\sqrt{Hz}$	$V_{DS} = 20$ V, $I_D = 1.0$ mA
$r_{ds(on)}$	Drain "ON" Resistance (f = 1.0 kHz)		155	250		220	350		300	600	Ohms	$V_{GS} = 0$, $I_D = 0$
I_{DSS}	Drain Current	10	16.5	40	3.0	7.8	12	1.0	2.75	4.0	mA	$V_{DS} = 20$ V, $V_{GS} = 0$
$V_{GS(off)}$	Gate to Source Cutoff Voltage		−4.3	−8.0		−2.5	−4.0		−1.0	−2.5	Volts	$V_{DS} = 20$ V, $I_D = 1.0\ \mu A$
C_{iss}	Input Capacitance (f = 1.0 MHz)		11	20		11	20		11	20	pF	$V_{DS} = 20$ V, $V_{GS} = 0$
Y_{os}	Output Admittance (f = 1.0 kHz)		52			27			24		μmhos	$V_{DS} = 20$ V, $V_{GS} = 0$
BV_{GSS}	Gate to Source Breakdown Voltage	−50			−50			−50			Volts	$I_G = 1.0\ \mu A$, $V_{DS} = 0$
C_{rss}	Reverse Transfer Capacitance (f = 1.0 MHz)		2.0	5.0		2.0	5.0		2.0	5.0	pF	$V_{DS} = 20$ V, $V_{GS} = 0$
I_{GSS}	Gate Reverse Current (FT0654A & C only)			0.1			0.1				nA	$V_{GS} = -25$ V, $V_{DS} = 0$
I_{GSS}	Gate Reverse Current (FT0654B, D & E only)			1.0			1.0			1.0	nA	$V_{GS} = -25$ V, $V_{DS} = 0$

Additional Electrical Characteristics on page 2

*Planar is a patented Fairchild process.

NOTES:

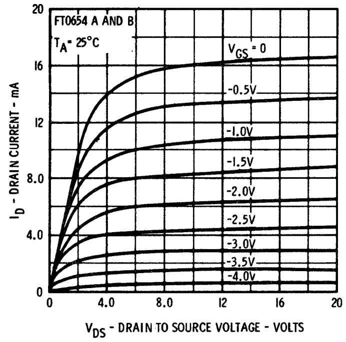
(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) This rating gives a maximum junction temperature of 175°C and junction to ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).

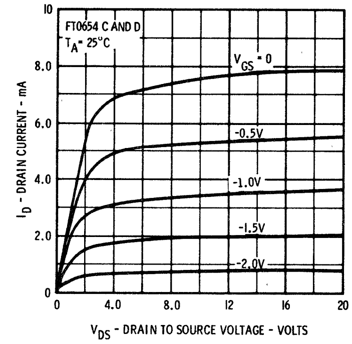
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

TYPICAL ELECTRICAL CHARACTERISTICS

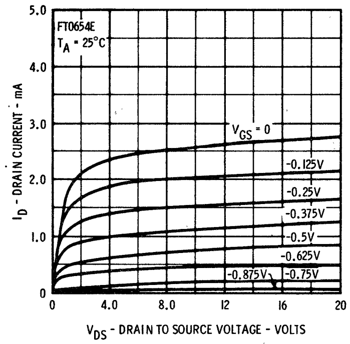
DRAIN CHARACTERISTICS



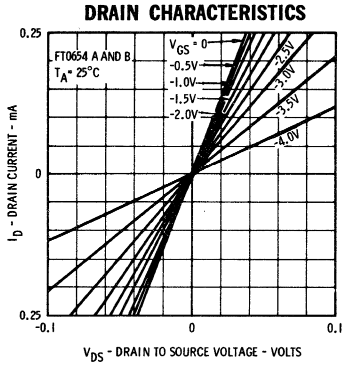
DRAIN CHARACTERISTICS



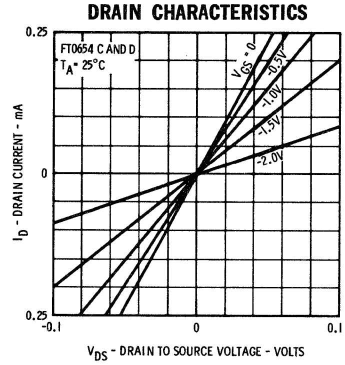
DRAIN CHARACTERISTICS



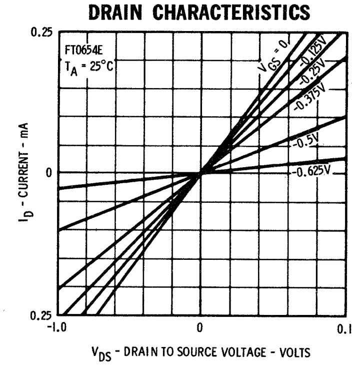
LOW VOLTAGE DRAIN CHARACTERISTICS



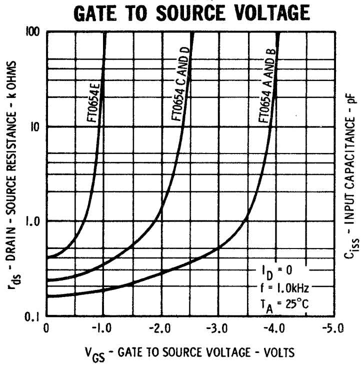
LOW VOLTAGE DRAIN CHARACTERISTICS



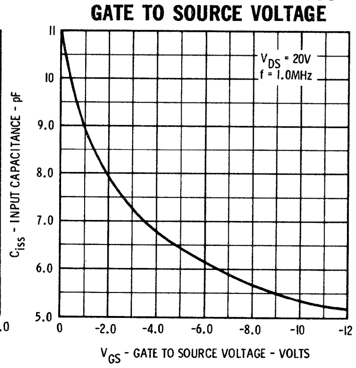
LOW VOLTAGE DRAIN CHARACTERISTICS



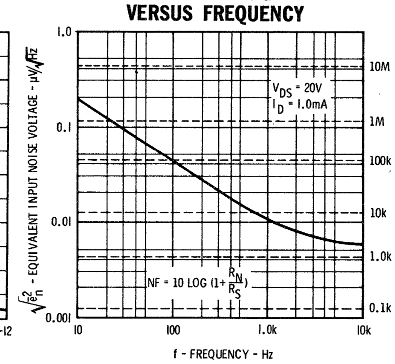
DRAIN-SOURCE RESISTANCE VERSUS GATE TO SOURCE VOLTAGE



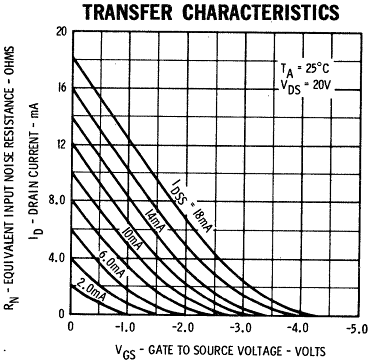
INPUT CAPACITANCE VERSUS GATE TO SOURCE VOLTAGE



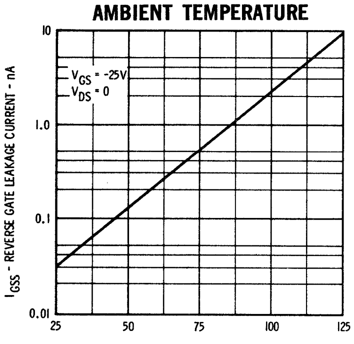
EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



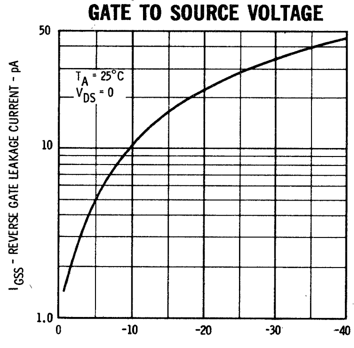
TRANSFER CHARACTERISTICS



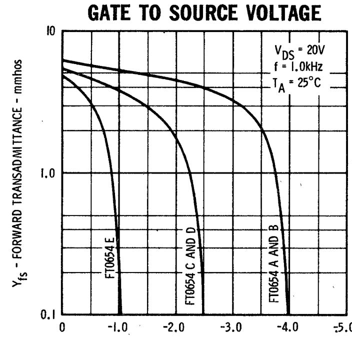
REVERSE GATE LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE



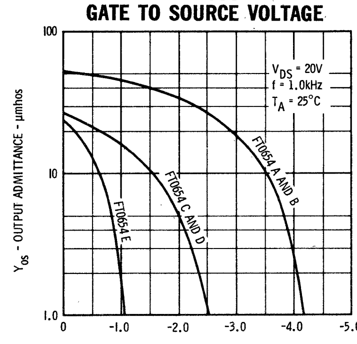
REVERSE GATE LEAKAGE CURRENT VERSUS GATE TO SOURCE VOLTAGE



FORWARD TRANSADMITTANCE VERSUS GATE TO SOURCE VOLTAGE



OUTPUT ADMITTANCE VERSUS GATE TO SOURCE VOLTAGE



2N2609

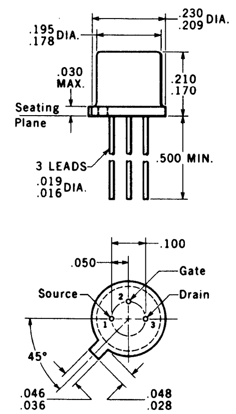
P-CHANNEL FIELD-EFFECT TRANSISTOR

DIFFUSED SILICON PLANAR* DEVICE

FOR IMPROVED PERFORMANCE SEE FAIRCHILD 2N4381

GENERAL DESCRIPTION - The 2N2609 is a silicon Planar* P-channel field-effect transistor designed primarily for low power audio-frequency applications in industrial service.

PHYSICAL DIMENSIONS
in accordance with
JEDEC (TO-18) outline



NOTES: All dimensions in inches
Leads are gold-plated kovar
Gate internally connected to case
Package weight is 0.43 gram

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

Operating Junction Temperature	175°C
Storage Temperature	-65°C to +200°C
Soldering Temperature (10 seconds time limit)	260°C

Maximum Power Dissipation

Total Dissipation at 25°C Ambient Temperature (Note 2)	0.3 Watt

Maximum Voltages

V_{SG}	Source to Gate Voltage	-30 Volts
V_{DS}	Drain to Source Voltage	-30 Volts
V_{DG}	Drain to Gate Voltage	-30 Volts

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

Symbol	Characteristic	Min.	Max.	Units	Test Conditions	
BV_{GSS}	Gate to Source Breakdown Voltage	30		Volts	I_G = 1.0 μA	V_{DS} = 0
I_{DSS}	Drain Current	2.0	10	mA	V_{DS} = -5.0 V	V_{GS} = 0
I_{GSS}	Gate Reverse Current		30	nA	V_{DS} = 0	V_{GS} = 5.0 V
V_P (V_{GS} off)	Gate to Source Pinch-off Voltage	1.0	4.0	Volts	V_{DS} = -5.0 V	I_D = 1.0 μA
Y_{fs}	Forward Transadmittance (f = 1.0 kHz)	2500		μmhos	V_{DS} = -5.0 V	V_{GS} = 0
C_{iss}	Input Capacitance (f = 140 kHz)		30	pF	V_{DS} = -5.0 V	V_{GS} = 1.0 V
I_{GSS} (150°C)	Gate Reverse Current		30	μA	V_{DS} = 0	V_{GS} = 5.0 V
NF	Spot Noise Figure (f = 1.0 kHz)		3.0	dB	V_{DS} = -5.0 V	V_{GS} = 0
					R_S = 1.0 MΩ	BW = 160 Hz

*Planar is a patented Fairchild process.

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) This rating gives a maximum junction temperature of 175°C and junction to ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FT 3820

P-CHANNEL FIELD EFFECT TRANSISTOR

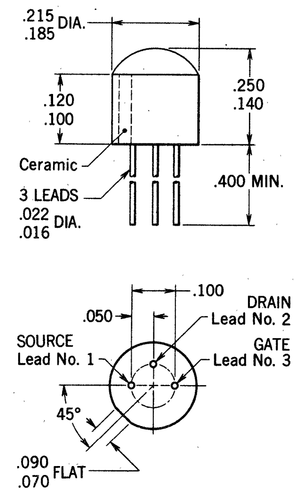
DIFFUSED SILICON PLANAR* DEVICE

FOR IMPROVED PERFORMANCE SEE FAIRCHILD 2N4342

GENERAL DESCRIPTION - The FT3820 is a silicon Planar* P-channel field effect transistor designed primarily for low power audio frequency applications.

The FT3820 is an electrical replacement for the 2N3820.

PHYSICAL DIMENSIONS



NOTES: All dimensions in inches
All leads electrically isolated from case
Package weight is 0.31 gram

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

Storage Temperature	-55°C to +125°C
Operating Junction Temperature	+125°C
Soldering Temperature (10 seconds time limit)	+260°C

Maximum Power Dissipation

Total Dissipation at 25°C Ambient Temperature (Note 2)	0.2 Watt

Maximum Voltages and Current

V_{SG}	Source to Gate Voltage	-20 Volts
V_{DS}	Drain to Source Voltage	-20 Volts
V_{DG}	Drain to Gate Voltage	-20 Volts
I_G	Gate Current	10 mA

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

Symbol	Characteristics	Min.	Max.	Units	Test Conditions
y_{fs}	Forward Transadmittance (f = 1.0 kHz)	0.8	5.0	mmhos	V_{DS} = -10 V V_{GS} = 0
I_{DSS}	Drain Current	0.3	15	mA	V_{DS} = -10 V V_{GS} = 0
$V_{GS(off)}$	Gate to Source Cutoff Voltage		8.0	Volts	V_{DS} = -10 V I_D = 10 μA
I_{GSS}	Gate Reverse Current		20	nA	V_{GS} = 10 V V_{DS} = 0
y_{os}	Output Admittance (f = 1.0 kHz)		200	μmhos	V_{DS} = -10 V V_{GS} = 0
C_{iss}	Input Capacitance (f = 1.0 MHz)		32	pF	V_{DS} = -10 V V_{GS} = 0
C_{rss}	Reverse Transfer Capacitance (f = 1.0 MHz)		16	pF	V_{DS} = -10 V V_{GS} = 0
I_{GSS}(100°C)	Gate Reverse Current		2.0	μA	V_{GS} = 10 V V_{DS} = 0
V_{GS}	Gate to Source Voltage	0.3	7.9	Volts	V_{DS} = -10 V I_D = 30 μA
y_{fs}	Forward Transadmittance (f = 10 MHz)	700		μmhos	V_{DS} = -10 V V_{GS} = 0
BV_{GSS}	Gate Source Breakdown Voltage	20		Volts	V_{DS} = 0 I_G = 10 μA

NOTES:

*Planar is a patented Fairchild process.

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) This rating gives a maximum junction temperature of 175°C and junction to ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FT 3909

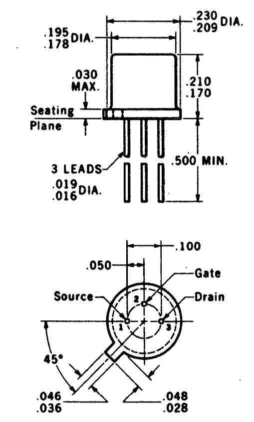
P-CHANNEL FIELD-EFFECT TRANSISTOR

DIFFUSED SILICON PLANAR* DEVICE

FOR IMPROVED PERFORMANCE SEE FAIRCHILD 2N4381

GENERAL DESCRIPTION - The FT3909 is a silicon Planar* P-channel field effect transistor designed primarily for low power audio frequency applications in the industrial service. The FT3909 is an electrical replacement for the 2N3909.

PHYSICAL DIMENSIONS
in accordance with
JEDEC (TO-18) outline



NOTES: All dimensions in inches
Leads are gold-plated kovar
Gate internally connected to case
Package weight is 0.43 gram

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

Storage Temperature	-65°C to +200°C
Operating Junction Temperature	+175°C
Soldering Temperature (10 seconds time limit)	+260°C

Maximum Power Dissipation

Total Dissipation at 25°C Ambient Temperature (Note 2)	0.3 Watt

Maximum Voltages and Current

V_{SG}	Source to Gate Voltage	-20 Volts
V_{DS}	Drain to Source Voltage	-20 Volts
V_{DG}	Drain to Gate Voltage	-20 Volts
I_G	Gate Current	10 mA

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

Symbol	Characteristic	Min.	Max.	Units	Test Conditions	
y_{fs}	Forward Transadmittance (f = 1.0 kHz)	1.0	5.0	mmhos	V_{DS} = -10 V	V_{GS} = 0
I_{DSS}	Drain Current	0.3	15	mA	V_{DS} = -10 V	V_{GS} = 0
$V_{GS(off)}$	Gate to Source Cutoff Voltage		8.0	Volts	V_{DS} = -10 V	I_D = 10 μA
I_{GSS}	Gate Reverse Current		10	nA	V_{GS} = 10 V	V_{DS} = 0
BV_{GSS}	Gate to Source Breakdown voltage	20		Volts	I_G = 10 μA	V_{DS} = 0
V_{GS}	Gate to Source Voltage	0.3	7.9	Volts	V_{DS} = -10 V	I_D = 30 μA
y_{os}	Output Admittance (f = 1.0 kHz)		100	μmhos	V_{DS} = -10 V	V_{GS} = 0
C_{iss}	Input Capacitance (f = 1.0 MHz)		32	pF	V_{DS} = -10 V	V_{GS} = 0
C_{rss}	Reverse Transfer Capacitance (f = 1.0 MHz)		16	pF	V_{DS} = -10 V	V_{GS} = 0
I_{GSS}(100°C)	Gate Reverse Current		1.0	μA	V_{GS} = 10 V	V_{DS} = 0
y_{fs}	Forward Transadmittance (f = 10 MHz)	900		μmhos	V_{DS} = -10 V	V_{GS} = 0

NOTES:

*Planar is a patented Fairchild process

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
(2) This rating gives a maximum junction temperature of 175°C and junction to ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

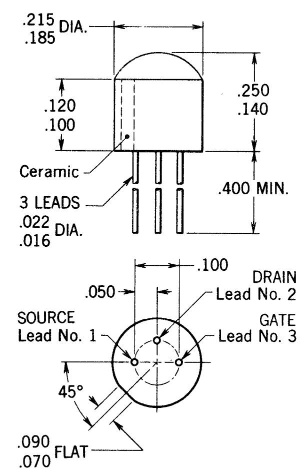
2N4342 • 2N4343 • 2N4360

P-CHANNEL FIELD-EFFECT TRANSISTORS

DIFFUSED SILICON PLANAR* TRANSISTORS

- **LOW NOISE VOLTAGE -- 0.08 $\mu V/\sqrt{Hz}$ (MAX) @ 100 Hz**
- **HIGH Y_{fs} -- 4000 µmhos (MIN)**
- **LOW r_{DS} (on) -- 350 Ω (MAX)**
- **LOW COST EPOXY PACKAGE**

PHYSICAL DIMENSIONS



NOTES: All dimensions in inches
All leads electrically isolated from case
Package weight is 0.31 gram

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

Operating Junction Temperature	125°C
Storage Temperature	-55°C to +125°C
Soldering Temperature (10 seconds time limit)	260°C

Maximum Power Dissipation

Total Dissipation at 25°C Case Temperature (Note 2)	0.5 Watt
at 65°C Case Temperature (Note 2)	0.3 Watt
at 25°C Ambient Temperature (Note 2)	0.2 Watt

Maximum Voltages

		2N4360	2N4342 **2N4343**
BV_{SGO}	Source to Gate Breakdown Voltage	-20 Volts	-25 Volts
BV_{DSO}	Drain to Source Breakdown Voltage	-20 Volts	-25 Volts
BV_{DGO}	Drain to Gate Breakdown Voltage	-20 Volts	-25 Volts

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

		2N4360			2N4342			**2N4343**				
Symbol	Characteristic	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units	Test Conditions
e_n	**Equivalent Input Noise Voltage** (f = 100 Hz)		0.02	0.08		0.02	0.08		**0.02**	**0.08**	**$\mu V/\sqrt{Hz}$**	V_{DS} = -10 V V_{GS} = 0
NF	Noise Figure (f = 100 Hz)		0.1	1.5		0.1	1.5		0.1	1.5	dB	V_{DS} = -10 V V_{GS} = 0 R_G = 1.0 MΩ BW = 15 Hz
Y_{fs}	**Forward Transadmittance** (f = 1.0 kHz)	2000	4000	8000	2000	3500	6000	**4000**	**6000**	**8000**	**µmhos**	V_{DS} = -10 V V_{GS} = 0
Y_{os}	Output Admittance (f = 1.0 kHz)		35	100		25	75		35	100	µmhos	V_{DS} = -10 V V_{GS} = 0
BV_{GSS}	Gate to Source Breakdown Voltage	20			25			25			Volts	I_G = 10 µA V_{DS} = 0
I_{DSS}	**Drain Current**	3.0	10	30	4.0	7.0	12	**10**	**18**	**30**	**mA**	V_{DS} = -10 V V_{GS} = 0
V_{GS}	Gate to Source Voltage	0.7	5.0	9.0							Volts	V_{DS} = -10 V I_D = 0.3 mA
V_{GS}	Gate to Source Voltage				0.7	3.0	5.0				Volts	V_{DS} = -10 V I_D = 0.4 mA
V_{GS}	Gate to Source Voltage							1.8	6.0	9.0	Volts	V_{DS} = -10 V I_D = 1.0 mA
V_{GS} (off)	**Gate to Source Cutoff Voltage**			10			5.5			**10**	**Volts**	V_{DS} = -10 V I_D = 1.0 µA
I_{GSS}	Gate Reverse Current		0.15	10		0.15	10		0.15	10	nA	V_{GS} = 15 V V_{DS} = 0
I_{GSS}(65°C)	Gate Reverse Current		.002	0.5		0.002	0.5		0.002	0.5	µA	V_{GS} = 15 V V_{DS} = 0
C_{iss}	Input Capacitance (f = 1.0 MHz)		15	20		15	20		15	20	pF	V_{DS} = -10 V V_{GS} = 0
C_{rss}	Reverse Transfer Capacitance (f = 1.0 MHz)		3.0	5.0		3.0	5.0		3.0	5.0	pF	V_{DS} = -10 V V_{GS} = 0
r_{DS}(on)	**Drain "On" Resistance** (f = 1.0 kHz)		350	700		300	700		**180**	**350**	**Ohms**	I_D = 0 V_{GS} = 0
$R_e(Y_{fs})$	Forward Transconductance (f = 1.0 MHz)	1500	3000		1500	2500		3000	5500		µmhos	V_{DS} = -10 V V_{GS} = 0

NOTES:

*Planar is a patented Fairchild process.

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

(2) These ratings give a maximum junction temperature of 125°C and junction to case thermal resistance of 200°C/Watt (derating factor of 5.0 mW/°C); junction to ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).

(3) Both 2N4342 and 2N4343 typical curves apply to 2N4360.

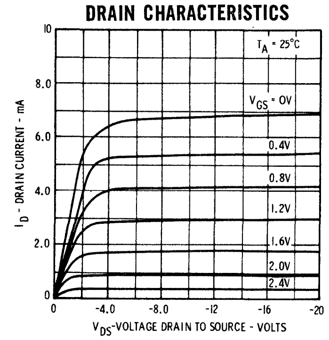
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

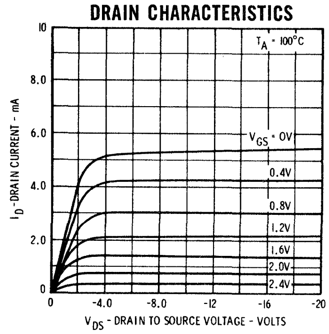
TYPICAL ELECTRICAL CHARACTERISTICS (Note 3)

2N4342

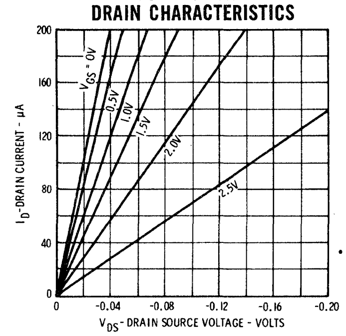
DRAIN CHARACTERISTICS



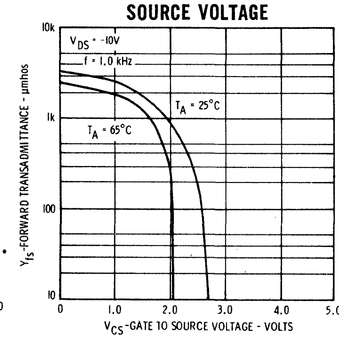
DRAIN CHARACTERISTICS



LOW VOLTAGE DRAIN CHARACTERISTICS

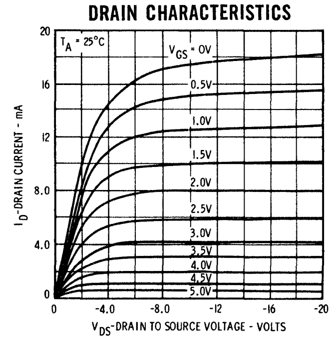


FORWARD TRANSADMITTANCE VERSUS GATE TO SOURCE VOLTAGE

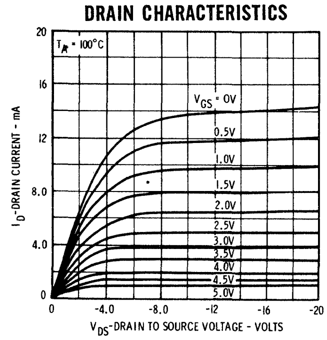


2N4343

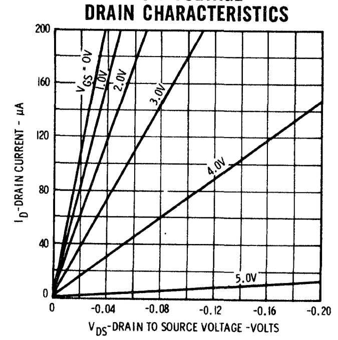
DRAIN CHARACTERISTICS



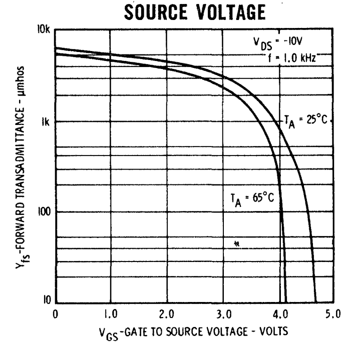
DRAIN CHARACTERISTICS



LOW VOLTAGE DRAIN CHARACTERISTICS

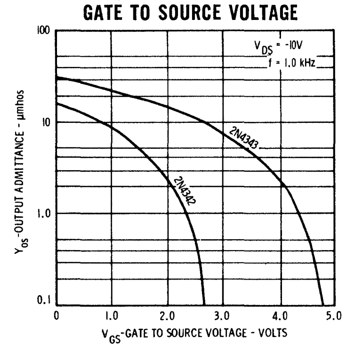


FORWARD TRANSADMITTANCE VERSUS GATE TO SOURCE VOLTAGE

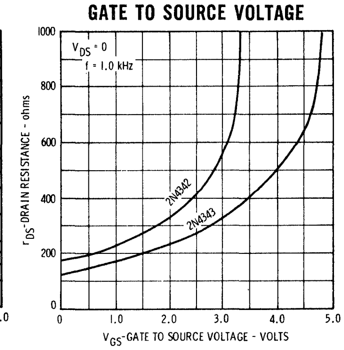


2N4342-2N4343

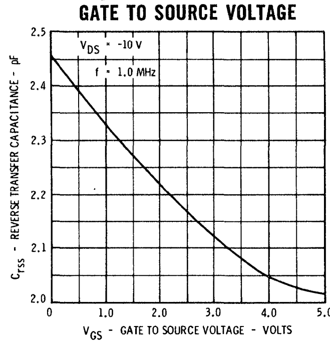
OUTPUT ADMITTANCE VERSUS GATE TO SOURCE VOLTAGE



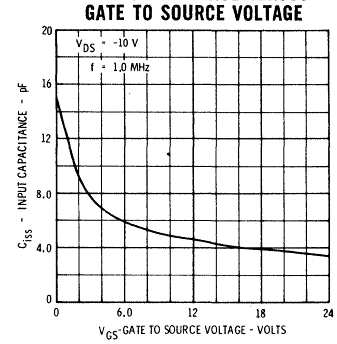
DRAIN RESISTANCE VERSUS GATE TO SOURCE VOLTAGE



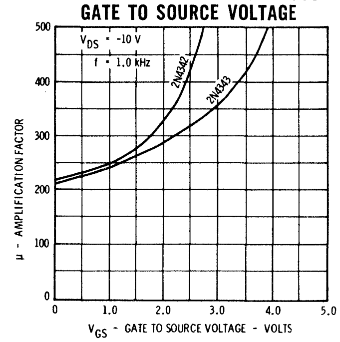
REVERSE TRANSFER CAPACITANCE VERSUS GATE TO SOURCE VOLTAGE



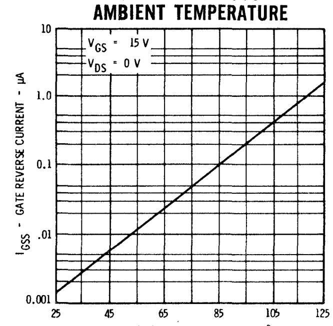
INPUT CAPACITANCE VERSUS GATE TO SOURCE VOLTAGE



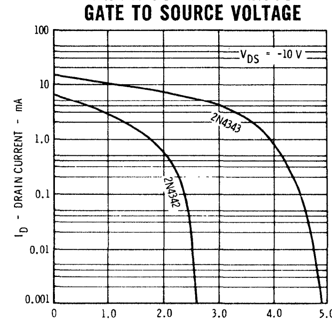
AMPLIFICATION FACTOR VERSUS GATE TO SOURCE VOLTAGE



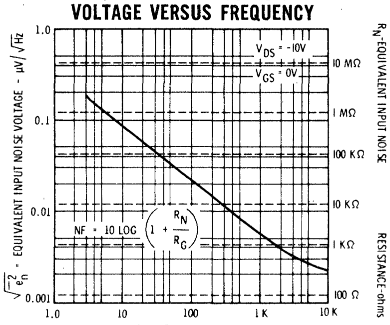
GATE REVERSE CURRENT VERSUS AMBIENT TEMPERATURE



DRAIN CURRENT VERSUS GATE TO SOURCE VOLTAGE



EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



2N4360 • 2N5033

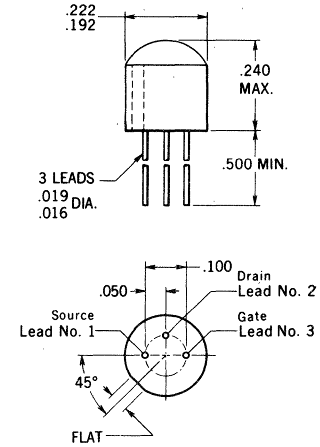
P-CHANNEL FIELD-EFFECT TRANSISTORS

DIFFUSED SILICON PLANAR* II TRANSISTORS

- **LOW COST EPOXY PACKAGE**
- **LOW PINCH-OFF . . . $V_{GS(off)} = 0.3 - 2.5$ V**
- **LOW NOISE . . . . . . $e_n = 0.1\ \mu V/\sqrt{Hz}$ (MAX) AT 1.0 kHz**
- **LOW NOISE . . . . . . 1.0 kHz NF = 2.0 dB (MAX) AT 1.0 MΩ**
- **LOW CURRENT . . . . $I_{DSS} = 0.3 - 3.5$ mA**
- **HIGH GAIN . . . . . . $y_{fs} = 1,000 - 5,000\ \mu$mhos**

PHYSICAL DIMENSIONS

In accordance with JEDEC (TO-106) outline



NOTES: All dimensions in inches
All leads electrically isolated from case
Package weight is 0.31 gram Package
is electrically non-conductive material

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures		
Storage Temperature		−55°C to +125°C
Operating Junction Temperature		+125°C
Lead Temperature (Soldering, 10 second time limit)		+260°C
Maximum Power Dissipation (Note 2)		
Total Dissipation at 25°C Case Temperature		0.5 Watt
at 65°C Case Temperature		0.3 Watt
at 25°C Ambient Temperature		0.2 Watt
Maximum Voltages and Current		
V_{SG}	Source to Gate Voltage	−20 Volts
V_{DS}	Drain to Source Voltage	−20 Volts
V_{DG}	Drain to Gate Voltage	−20 Volts
I_G	Gate Current	50 mA

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTICS	2N4360 MIN.	2N4360 TYP.	2N4360 MAX.	2N5033 MIN.	2N5033 TYP.	2N5033 MAX.	UNITS	TEST CONDITIONS	
$V_{GS(off)}$	**Gate to Source Cutoff Voltage**	0.7	4.0	10	**0.3**	**0.9**	**2.5**	**Volts**	$V_{DS} = -10$ V	$I_D = 1.0\ \mu A$
V_{GS}	Gate to Source Voltage	0.4	3.0	9.0				Volts	$V_{DS} = -10$ V	$I_D = 300\ \mu A$
V_{GS}	Gate to Source Voltage					0.8	2.3	Volts	$V_{DS} = -10$ V	$I_D = 30\ \mu A$
y_{fs}	**Forward Transadmittance (f = 1.0 kHz)**	2,000	5,500	8,000	**1,000**	**3,000**	**5,000**	**μmhos**	$V_{DS} = -10$ V	$V_{GS} = 0$ V
$R_e(y_{fs})$	Forward Transconductance (f = 1.0 MHz)	1,500	5,500		900	3,000		μmhos	$V_{DS} = -10$ V	$V_{GS} = 0$ V
e_n	Equivalent Input Noise Voltage		0.05	0.19				$\mu V/\sqrt{Hz}$	$V_{DS} = -10$ V	$I_D = 1.0$ mA
	(f = 100 Hz, BW = 15 Hz)					0.07		$\mu V/\sqrt{Hz}$	$V_{DS} = -10$ V	$V_{GS} = 0$ V
e_n	**Equivalent Input Noise Voltage**		0.02					$\mu V/\sqrt{Hz}$	$V_{DS} = -10$ V	$I_D = 1.0$ mA
	(f = 1.0 kHz, BW = 150 Hz)					**0.025**	**0.1**	$\mu V/\sqrt{Hz}$	$V_{DS} = -10$ V	$V_{GS} = 0$ V
NF	Noise Figure (f = 100 Hz,		0.6	5.0				dB	$V_{DS} = -10$ V	$I_D = 1.0$ mA
	$R_G = 1.0$ MΩ, BW = 15 Hz)					1.2		dB	$V_{DS} = -10$ V	$V_{GS} = 0$ V
NF	**Noise Figure (f = 1.0 kHz,**		0.15					dB	$V_{DS} = -10$ V	$I_D = 1.0$ mA
	$R_G = 1.0$ MΩ, BW = 150 Hz)					**0.2**	**2.0**	**dB**	$V_{DS} = -10$ V	$V_{GS} = 0$ V
I_{DSS}	**Drain Current**	3.0	11	30	**0.3**	**1.6**	**3.5**	**mA**	$V_{DS} = -10$ V	$V_{GS} = 0$ V
I_{GSS}	Gate Reverse Current		0.8	10		0.8	10	nA	$V_{GS} = 15$ V	$V_{DS} = 0$ V
I_{GSS}(65°C)	Gate Reverse Current		0.015	0.5		0.015	0.5	μA	$V_{GS} = 15$ V	$V_{DS} = 0$ V
$r_{ds(on)}$	Drain "On" Resistance (f = 1.0 kHz)		200	700		375	1,300	Ω	$V_{GS} = 0$ V	$I_D = 0$
C_{rss}	Reverse Transfer Capacitance (f = 1.0 MHz)		3.0	5.0		2.5	7.0	pF	$V_{DS} = -10$ V	$V_{GS} = 0$ V
C_{iss}	Input Capacitance (f = 1.0 MHz)		15	20		17	25	pF	$V_{DS} = -10$ V	$V_{GS} = 0$ V
Y_{os}	Output Admittance (f = 1.0 kHz)		25	100		2.5	20	μmhos	$V_{DS} = -10$ V	$V_{GS} = 0$ V
BV_{GSS}	Gate to Source Breakdown Voltage	20			20			Volts	$V_{DS} = 0$ V	$I_G = 10\ \mu A$

Notes on page 2.

*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

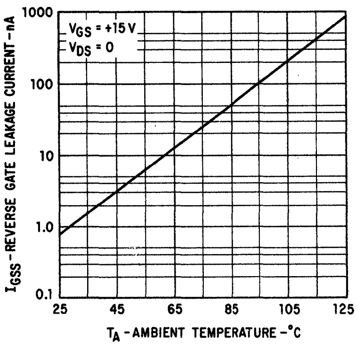
NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

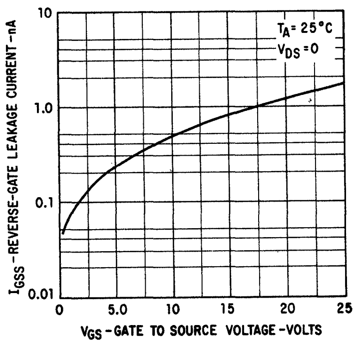
(2) These ratings give a maximum junction temperature of 125°C and junction to case thermal resistance of 200°C/watt (derating factor of 5.0 mW/°C); junction to ambient thermal resistance of 500°C/watt (derating factor of 2.0 mW/°C).

TYPICAL ELECTRICAL CHARACTERISTICS

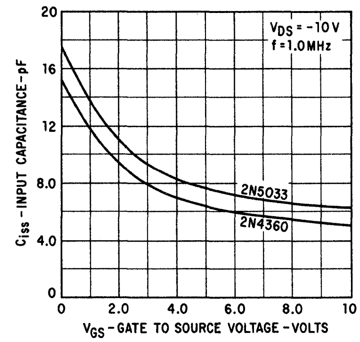
REVERSE GATE LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE



REVERSE GATE LEAKAGE CURRENT VERSUS GATE TO SOURCE VOLTAGE

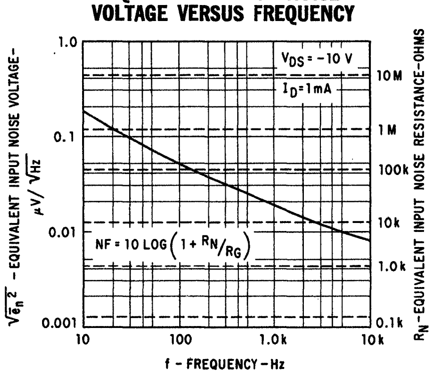


INPUT CAPACITANCE VERSUS GATE TO SOURCE VOLTAGE

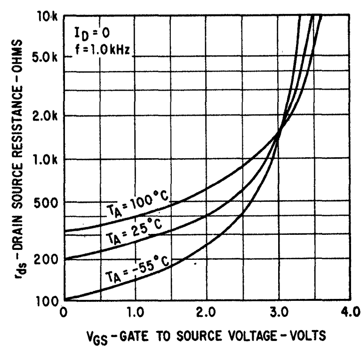


2N4360

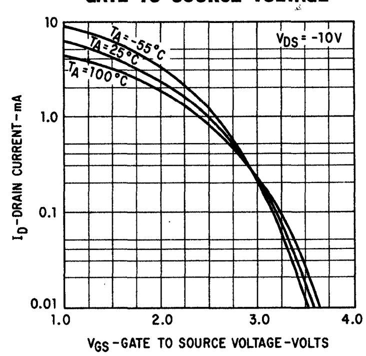
EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



DRAIN-SOURCE RESISTANCE VERSUS GATE TO SOURCE VOLTAGE

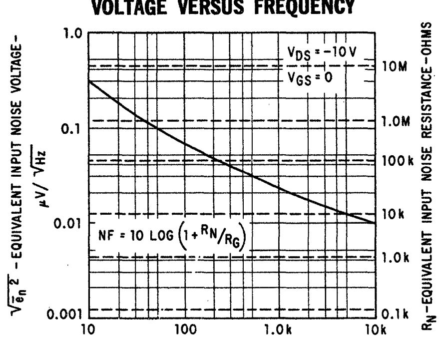


DRAIN CURRENT VERSUS GATE TO SOURCE VOLTAGE

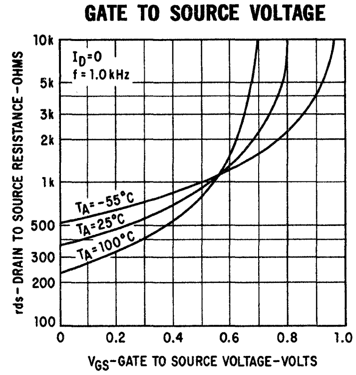


2N5033

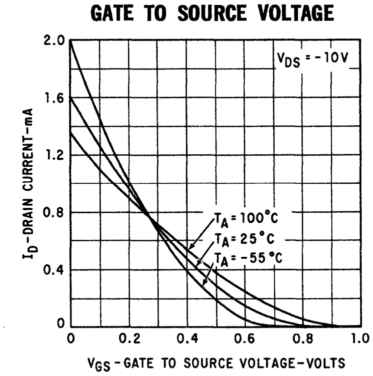
EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



DRAIN-SOURCE RESISTANCE VERSUS GATE TO SOURCE VOLTAGE

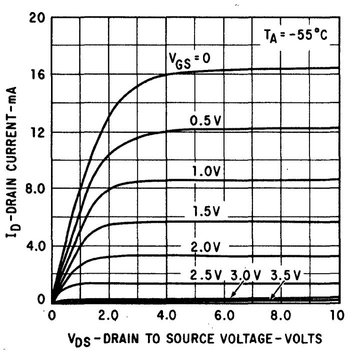


DRAIN CURRENT VERSUS GATE TO SOURCE VOLTAGE

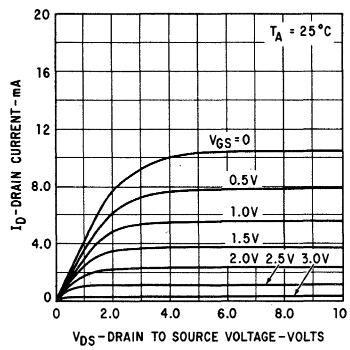


TYPICAL ELECTRICAL CHARACTERISTICS (2N4360 ONLY)

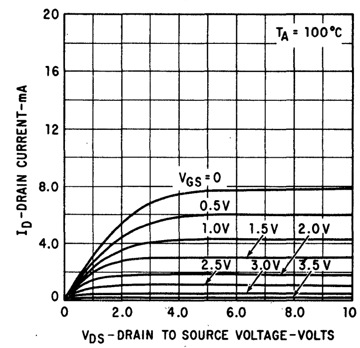
DRAIN CHARACTERISTICS



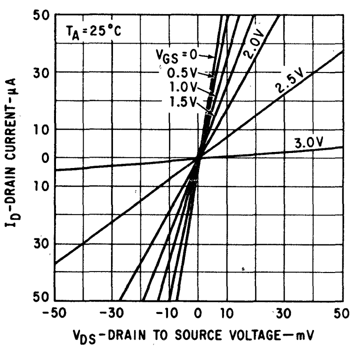
DRAIN CHARACTERISTICS



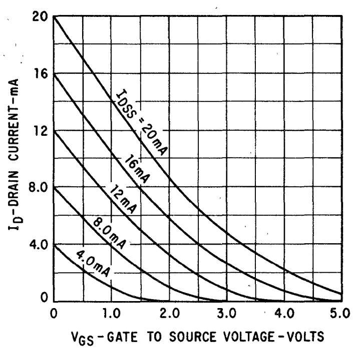
DRAIN CHARACTERISTICS



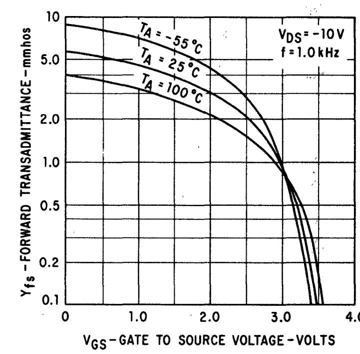
LOW VOLTAGE DRAIN CHARACTERISTICS



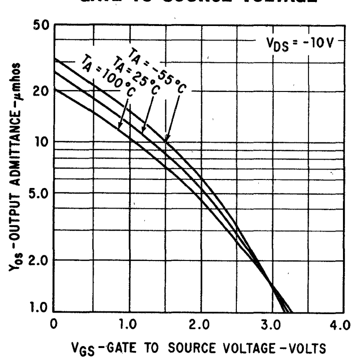
TRANSFER CHARACTERISTICS



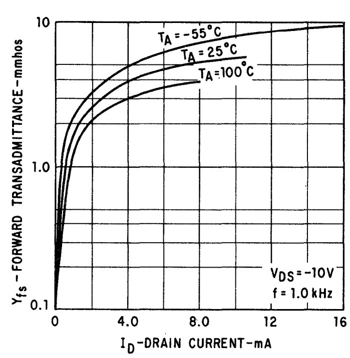
FORWARD TRANSADMITTANCE VERSUS GATE TO SOURCE VOLTAGE



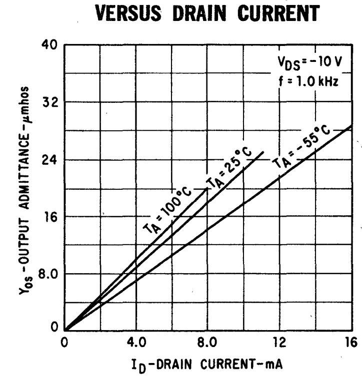
OUTPUT ADMITTANCE VERSUS GATE TO SOURCE VOLTAGE



FORWARD TRANSADMITTANCE VERSUS DRAIN CURRENT

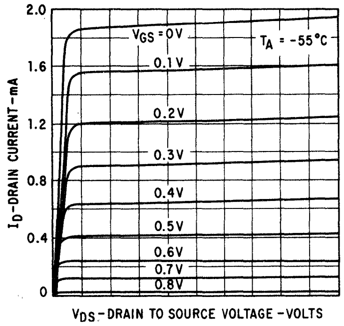


OUTPUT ADMITTANCE VERSUS DRAIN CURRENT

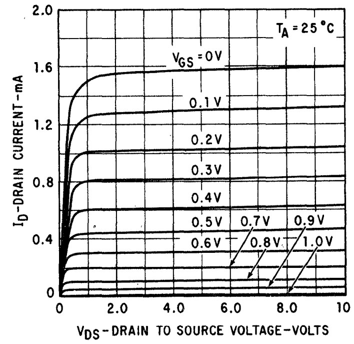


TYPICAL ELECTRICAL CHARACTERISTICS
(2N5033 ONLY)

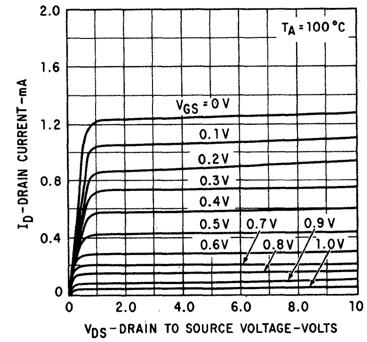
DRAIN CHARACTERISTICS



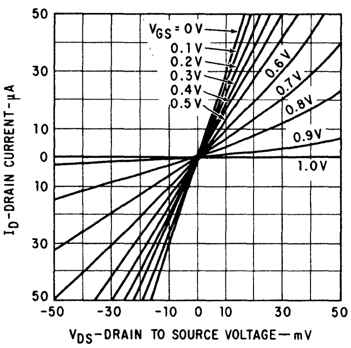
DRAIN CHARACTERISTICS



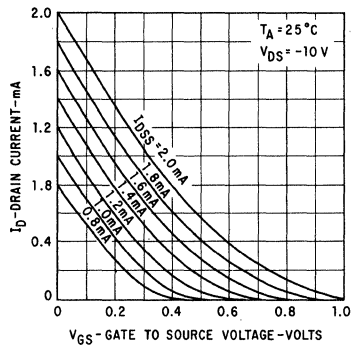
DRAIN CHARACTERISTICS



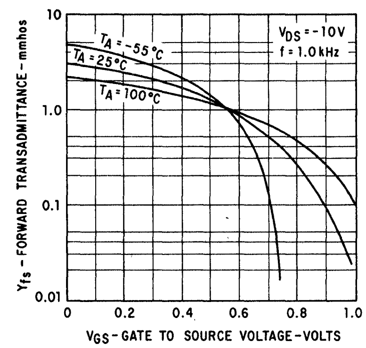
LOW VOLTAGE DRAIN CHARACTERISTICS



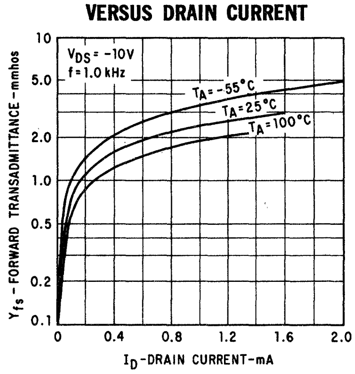
TRANSFER CHARACTERISTICS



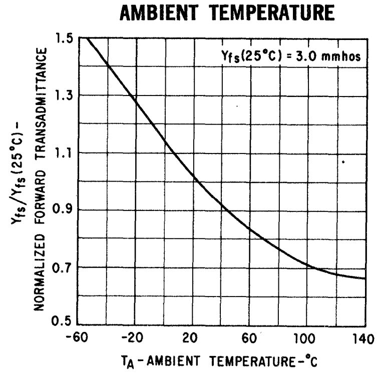
FORWARD TRANSADMITTANCE VERSUS GATE TO SOURCE VOLTAGE



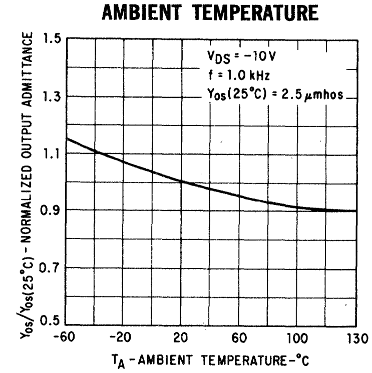
FORWARD TRANSADMITTANCE VERSUS DRAIN CURRENT



NORMALIZED FORWARD TRANSADMITTANCE VERSUS AMBIENT TEMPERATURE



NORMALIZED OUTPUT ADMITTANCE VERSUS AMBIENT TEMPERATURE



2N4381 • 2N4382

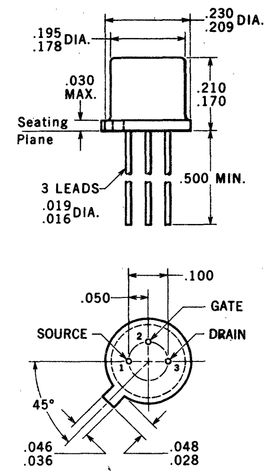
P-CHANNEL FIELD-EFFECT TRANSISTORS

DIFFUSED SILICON PLANAR* DEVICES

EATURES

- **HIGH Y_{fs} -- 4,000 μmhos (MIN)**
- **LOW NOISE -- $e_n = 0.08\ \mu V/\sqrt{Hz}$ (MAX) @ 100 Hz**
- **LOW LEAKAGE -- $I_{GSS} = 1.0$ nA (MAX)**
- **LOW ON-RESISTANCE -- $r_{ds}(on) = 350\Omega$ (MAX)**

PHYSICAL DIMENSIONS
in accordance with
JEDEC (TO-18) outline



NOTES: All dimensions in inches
Leads are gold-plated kovar
Gate internally connected to case
Package weight is 0.43 gram

BSOLUTE MAXIMUM RATINGS [Note 1]

Maximum Temperatures

Operating Junction Temperature	175°C
Storage Temperature	−65°C to +200°C
Soldering Temperature (10 seconds time limit)	260°C
Maximum Power Dissipation	
Total Dissipation at 25°C Ambient Temperature [Note 2]	0.3 Watt
Maximum Voltages	
V_{SGO} Source to Gate Breakdown Voltage	−25 Volts
V_{DSO} Drain to Source Breakdown Voltage	−25 Volts
V_{DGO} Drain to Gate Breakdown Voltage	−25 Volts

LECTRICAL CHARACTERISTICS (25°C Free Air Temperature Unless Otherwise Noted)

Symbol	Characteristic	2N4381 Min.	2N4381 Typ.	2N4381 Max.	2N4382 Min.	2N4382 Typ.	2N4382 Max.	Units	Test Conditions	
Y_{fs}	**Forward Transadmittance (f = 1.0 kHz)**	2000	3500	6000	**4000**	**6000**	**8000**	**μmhos**	**$V_{DS} = -15$ V**	**$V_{GS} = 0$**
e_n	**Equivalent Input Noise Voltage (f = 100 Hz)**		0.04	0.08		**0.04**	**0.08**	**$\mu V/\sqrt{Hz}$**	**$V_{DS} = -15$ V**	**$V_{GS} = 2.0$ V, PBW = 15 Hz**
e_n	Equivalent Input Noise Voltage (f = 1.0 kHz)		0.009	0.02		0.009	0.02	$\mu V/\sqrt{Hz}$	$V_{DS} = -15$ V	$V_{GS} = 2.0$ V, PBW = 150 Hz
e_n	Equivalent Input Noise Voltage (f = 10 kHz)		0.003	0.007		0.003	0.007	$\mu V/\sqrt{Hz}$	$V_{DS} = -15$ V	$V_{GS} = 2.0$ V, PBW = 1.5 kHz
r_{ds} (on)	**Drain to Source "ON" Resistance (f = 1.0 kHz)**		300	700		**180**	**350**	**Ohms**	**$I_D = 0$**	**$V_{GS} = 0$**
I_{GSS}	**Gate Reverse Current**		0.45	1.0		**0.45**	**1.0**	**nA**	**$V_{DS} = 0$**	**$V_{GS} = 15$ V**
BV_{GSS}	Gate to Source Breakdown Voltage	25			25			Volts	$I_G = 1.0\ \mu A$	$V_{DS} = 0$
I_{DSS}	**Drain Current**	3.0	6.8	12	**10**	**17**	**30**	**mA**	**$V_{DS} = -15$ V**	**$V_{GS} = 0$**
C_{iss}	Input Capacitance (f = 1.0 MHz)		13	20		13	20	pF	$V_{DS} = -15$ V	$V_{GS} = 0$
C_{rss}	Reverse Transfer Capacitance (f = 1.0 MHz)		3.0	5.0		3.0	5.0	pF	$V_{DS} = -15$ V	$V_{GS} = 0$

Additional Electrical Characteristics on page 2

* Planar is a patented Fairchild process.

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
(2) This rating gives a maximum junction temperature of 175°C and junction to ambient thermal resistance of 500°C/watt (derating factor of 2.0 mW/°C).

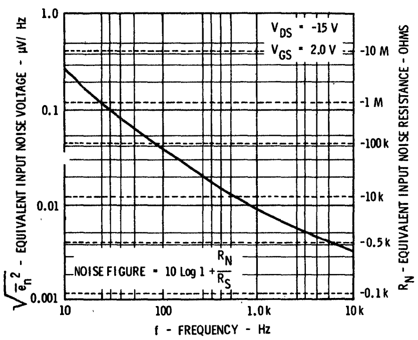
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

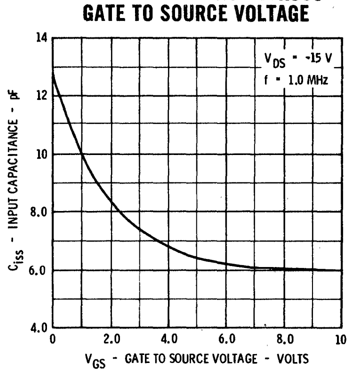
Symbol	Characteristic	2N4381 Min.	2N4381 Typ.	2N4381 Max.	2N4382 Min.	2N4382 Typ.	2N4382 Max.	Units	Test Conditions
V_{GS}	Gate to Source Voltage	1.0	3.5	5.0				Volts	$V_{DS} = -15$ V, $I_D = 0.3$ mA
V_{GS}	Gate to Source Voltage				2.5	6.5	9.0	Volts	$V_{DS} = -15$ V, $I_D = 1.0$ mA
NF	Spot Noise Figure (f = 100 Hz)		1.5	3.0		1.5	3.0	dB	$V_{DS} = -15$ V, $V_{GS} = 2.0$ V, $R_S = 400$ kΩ, PBW = 15 Hz
NF	Spot Noise Figure (f = 1.0 kHz)		1.5	3.0		1.5	3.0	dB	$V_{DS} = -15$ V, $V_{GS} = 2.0$ V, $R_S = 15$ kΩ, PBW = 150 Hz
NF	Spot Noise Figure (f = 10 kHz)		1.5	3.0		1.5	3.0	dB	$V_{DS} = -15$ V, $V_{GS} = 2.0$ V, $R_S = 3.0$ kΩ, PBW = 1.5 kHz
V_{GS} (off)	Gate to Source Cutoff Voltage	1.0	3.0	5.0	2.5	6.0	9.0	Volts	$V_{DS} = -15$ V, $I_D = 1.0$ μA
I_{GSS} (125°C)	Gate Reverse Current		0.4	1.0		0.4	1.0	μA	$V_{GS} = 15$ V, $V_{DS} = 0$
Y_{fs} (100°C)	Forward Transadmittance (f = 1.0 kHz)	1200	2300		2500	4000		μmhos	$V_{DS} = -15$ V, $V_{GS} = 0$
Y_{os}	Output Admittance (f = 1.0 kHz)		19	75		30	100	μmhos	$V_{DS} = -15$ V, $V_{GS} = 0$

TYPICAL ELECTRICAL CHARACTERISTICS
2N4381 • 2N4382

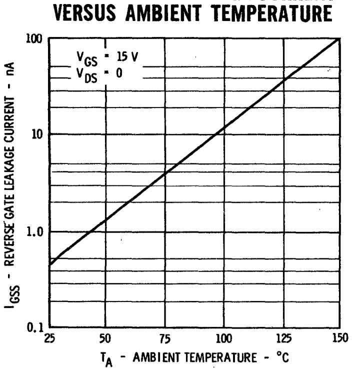
EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



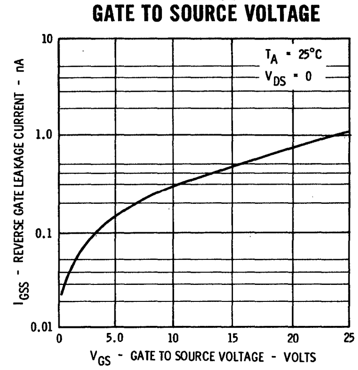
INPUT CAPACITANCE VERSUS GATE TO SOURCE VOLTAGE



REVERSE GATE LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE

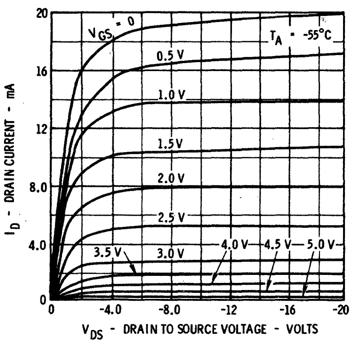


REVERSE GATE LEAKAGE CURRENT VERSUS GATE TO SOURCE VOLTAGE

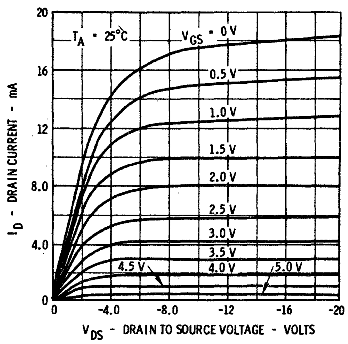


TYPICAL ELECTRICAL CHARACTERISTICS
2N4382

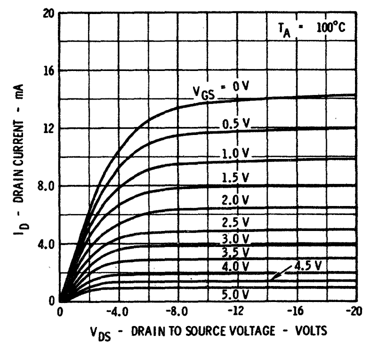
DRAIN CHARACTERISTICS



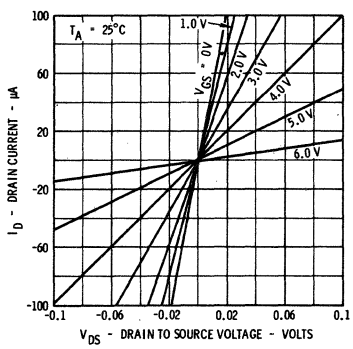
DRAIN CHARACTERISTICS



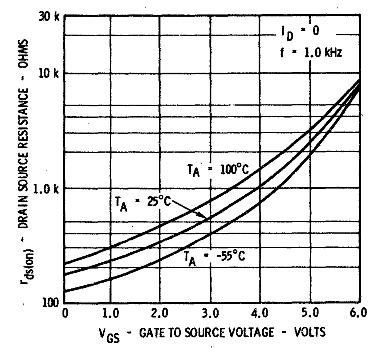
DRAIN CHARACTERISTICS



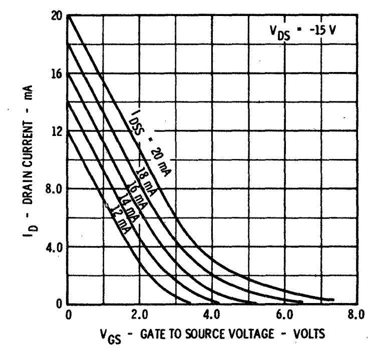
LOW VOLTAGE DRAIN CHARACTERISTICS



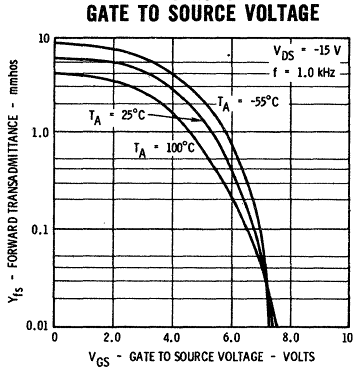
DRAIN-SOURCE ON RESISTANCE VERSUS GATE TO SOURCE VOLTAGE



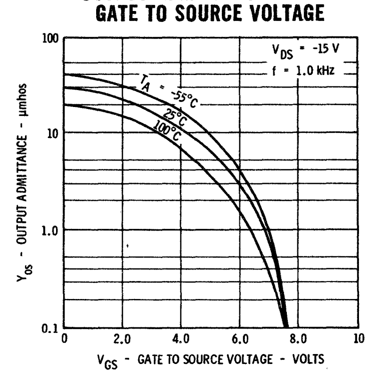
TRANSFER CHARACTERISTICS



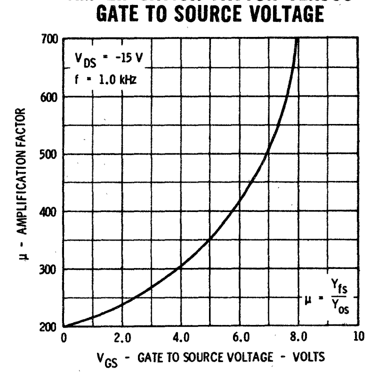
FORWARD TRANSADMITTANCE VERSUS GATE TO SOURCE VOLTAGE



OUTPUT ADMITTANCE VERSUS GATE TO SOURCE VOLTAGE

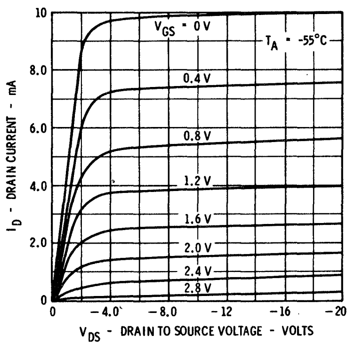


AMPLIFICATION FACTOR VERSUS GATE TO SOURCE VOLTAGE

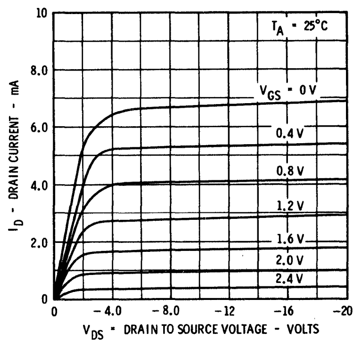


TYPICAL ELECTRICAL CHARACTERISTICS
2N4381

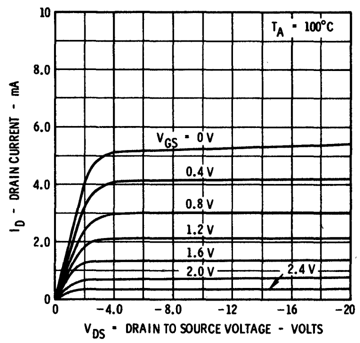
DRAIN CHARACTERISTICS



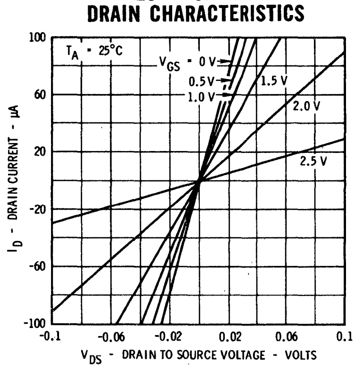
DRAIN CHARACTERISTICS



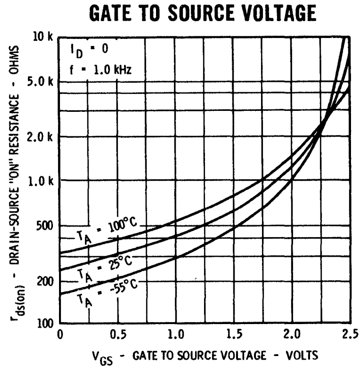
DRAIN CHARACTERISTICS



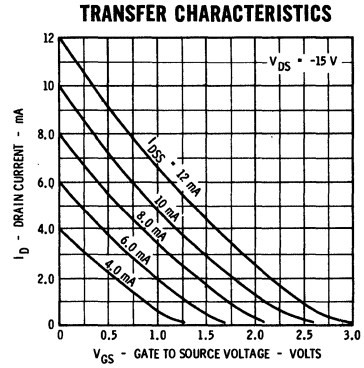
LOW VOLTAGE DRAIN CHARACTERISTICS



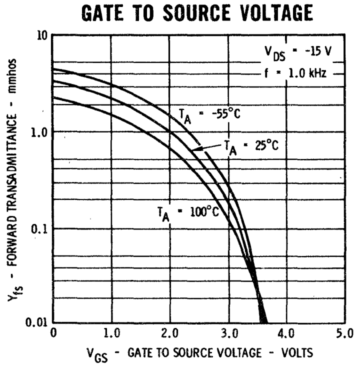
DRAIN-SOURCE ON RESISTANCE VERSUS GATE TO SOURCE VOLTAGE



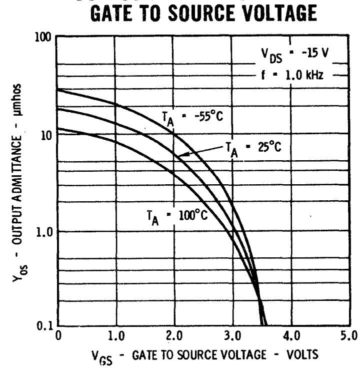
TRANSFER CHARACTERISTICS



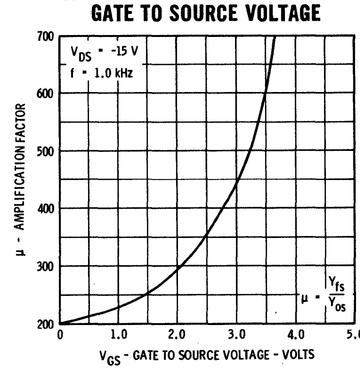
FORWARD TRANSADMITTANCE VERSUS GATE TO SOURCE VOLTAGE



OUTPUT ADMITTANCE VERSUS GATE TO SOURCE VOLTAGE



AMPLIFICATION FACTOR VERSUS GATE TO SOURCE VOLTAGE



FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

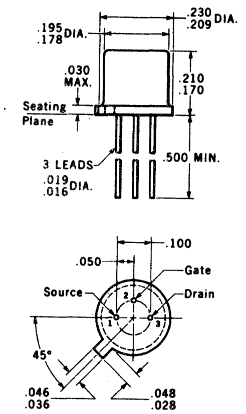
2N5020 • 2N5021

P-CHANNEL FIELD-EFFECT TRANSISTORS

DIFFUSED SILICON PLANAR* II TRANSISTORS

- **LOW PINCH-OFF . . . $V_{GS(off)} = 0.3 - 1.5$ V AT 1.0 μA**
- **LOW NOISE . . . . . . $e_n = 0.1\ \mu V/\sqrt{Hz}$ (MAX) AT 100 Hz**
  . . . . . . 100 Hz N.F. = 0.9 dB (TYP) AT 1.0 MΩ
- **LOW CURRENT . . . . $I_{DSS} = 0.3 - 1.2$ mA**
- **HIGH GAIN . . . . . . $Y_{fs} = 1{,}000 - 3{,}500\ \mu$mhos**

PHYSICAL DIMENSIONS
in accordance with
JEDEC (TO-18) outline



NOTES: All dimensions in inches
Leads are gold-plated kovar
Gate internally connected to case
Package weight is 0.43 gram

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

Operating Junction Temperature	175°C
Storage Temperature	−65°C to +200°C
Soldering Temperature (10 second time limit)	260°C

Maximum Power Dissipation

Total Dissipation at 25°C Ambient Temperature (Note 2)	0.3 Watt

Maximum Voltages and Current

V_{SG}	Source to Gate Voltage	−25 Volts
V_{DS}	Drain to Source Voltage	−25 Volts
V_{DG}	Drain to Gate Voltage	−25 Volts
I_G	Gate Current	50 mA

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTICS	2N5020 MIN.	2N5020 TYP.	2N5020 MAX.	2N5021 MIN.	2N5021 TYP.	2N5021 MAX.	UNITS	TEST CONDITIONS	
$V_{GS(off)}$	**Gate to Source Cutoff Voltage**	**0.3**	**0.5**	**1.5**	0.5	1.2	2.5	**Volts**	$V_{DS} = -15$ V	$I_D = 1.0\ \mu$A
V_{GS}	Gate to Source Voltage		0.4	1.3				Volts	$V_{DS} = -15$ V	$I_D = 30\ \mu$A
V_{GS}	Gate to Source Voltage					1.0	2.3	Volts	$V_{DS} = -15$ V	$I_D = 100\ \mu$A
y_{fs}	**Forward Transadmittance (f = 1.0 kHz)**	**1,000**	**2,500**	**3,500**	1,500	3,500	5,000	**μmhos**	$V_{DS} = -15$ V	$V_{GS} = 0$
y_{fs}(+100°C)	Forward Transadmittance (f = 1.0 kHz)	600	1,800		900	2,500		μmhos	$V_{DS} = -15$ V	$V_{GS} = 0$
$R_e(y_{fs})$	Forward Transconductance (f = 1.0 MHz)	900	2,500		1,300	3,500		μmhos	$V_{DS} = -15$ V	$V_{GS} = 0$
e_n	**Equivalent Input Noise Voltage (f=100 Hz, BW=15 Hz)**		**0.06**	**0.1**		0.06	0.1	**$\mu V/\sqrt{Hz}$**	$V_{DS} = -15$ V	$V_{GS} = 0$
e_n	Equivalent Input Noise Voltage (f=1.0 kHz, BW=150 Hz)		0.018	0.03		0.018	0.03	$\mu V/\sqrt{Hz}$	$V_{DS} = -15$ V	$V_{GS} = 0$
e_n	Equivalent Input Noise Voltage (f=10 kHz, BW=1.5 kHz)		0.005	**0.01**		0.005	**0.01**	$\mu V/\sqrt{Hz}$	$V_{DS} = -15$ V	$V_{GS} = 0$
NF	**Noise Figure (f = 100 Hz, R_G = 600 kΩ, BW = 15 Hz)**		**1.5**	**3.0**		**1.5**	**3.0**	**dB**	$V_{DS} = -15$ V	$V_{GS} = 0$
NF	Noise Figure (f = 1.0 kHz, R_G = 55 kΩ, BW = 150 Hz)		1.5	3.0		1.5	3.0	dB	$V_{DS} = -15$ V	$V_{GS} = 0$
NF	Noise Figure (f = 10 kHz, R_G = 6.0 kΩ, BW = 1.5 kHz)		1.5	3.0		1.5	3.0	dB	$V_{DS} = -15$ V	$V_{GS} = 0$
I_{DSS}	**Drain Current**	**0.3**	**0.65**	**1.2**	1.0	1.8	3.5	**mA**	$V_{DS} = -15$ V	$V_{GS} = 0$
I_{GSS}	Gate Reverse Current		0.4	1.0		0.4	1.0	nA	$V_{GS} = 15$ V	$V_{DS} = 0$
I_{GSS}(+125°C)	Gate Reverse Current		0.4	1.0		0.4	1.0	μA	$V_{GS} = 15$ V	$V_{DS} = 0$
$r_{ds(on)}$	Drain "On" Resistance (f = 1.0 kHz)		600	1,300		350	1,000	Ω	$V_{GS} = 0$	$I_D = 0$
C_{rss}	Reverse Transfer Capacitance (f = 1.0 MHz)		3.2	7.0		3.2	7.0	pF	$V_{DS} = -15$ V	$V_{GS} = 0$
C_{iss}	Input Capacitance (f = 1.0 MHz)		18	25		18	25	pF	$V_{DS} = -15$ V	$V_{GS} = 0$
y_{os}	Output Admittance (f = 1.0 kHz)		1.2	20		2.0	20	μmhos	$V_{DS} = -15$ V	$V_{GS} = 0$
BV_{GSS}	Gate to Source Breakdown Voltage	25			25			Volts	$V_{DS} = 0$	$I_G = 1.0\ \mu$A

NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
(2) This rating gives a maximum junction temperature of 175°C and junction to ambient thermal resistance of 500°C/watt (derating factor of 2.0 mW/°C).

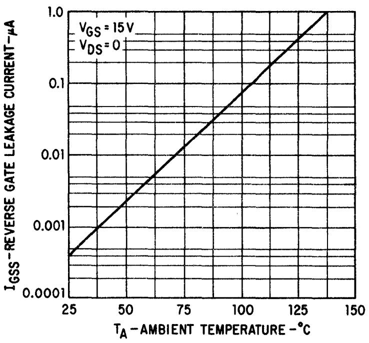
*Planar is a patented Fairchild process.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

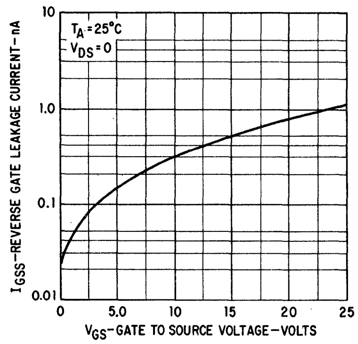
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

TYPICAL ELECTRICAL CHARACTERISTICS

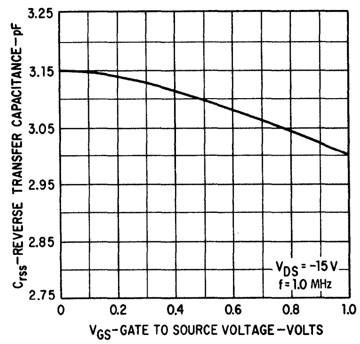
REVERSE GATE LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE



REVERSE GATE LEAKAGE CURRENT VERSUS GATE TO SOURCE VOLTAGE

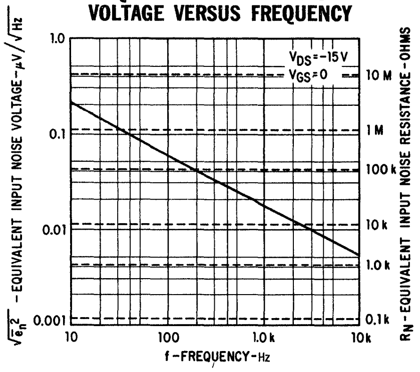


REVERSE TRANSFER CAPACITANCE VERSUS GATE TO SOURCE VOLTAGE

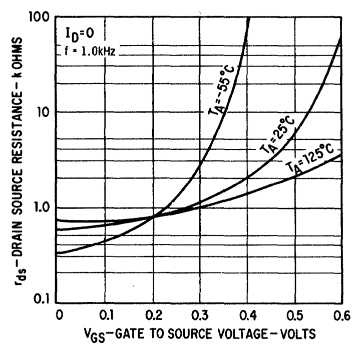


2N5020

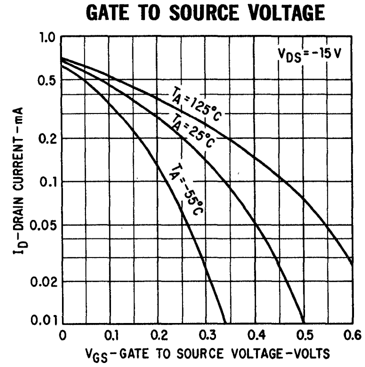
EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



DRAIN TO SOURCE RESISTANCE VERSUS GATE TO SOURCE VOLTAGE

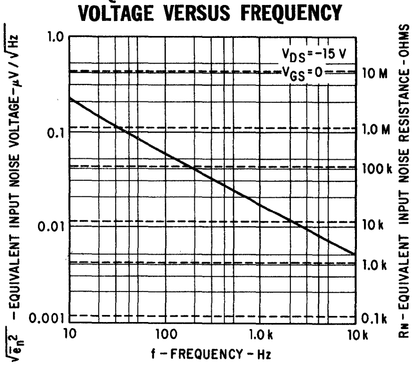


DRAIN CURRENT VERSUS GATE TO SOURCE VOLTAGE

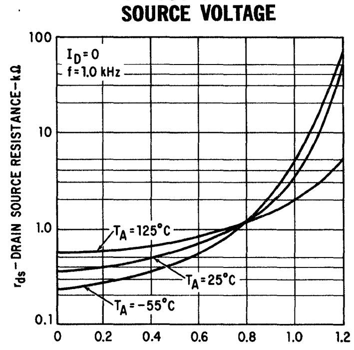


2N5021

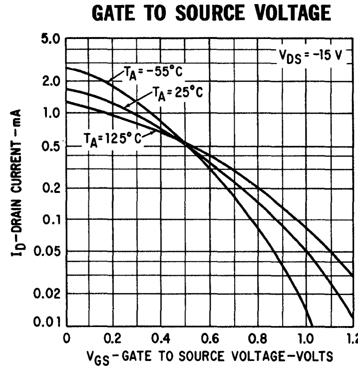
EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



DRAIN TO SOURCE RESISTANCE VERSUS GATE TO SOURCE VOLTAGE

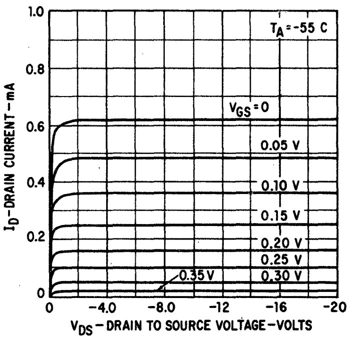


DRAIN CURRENT VERSUS GATE TO SOURCE VOLTAGE

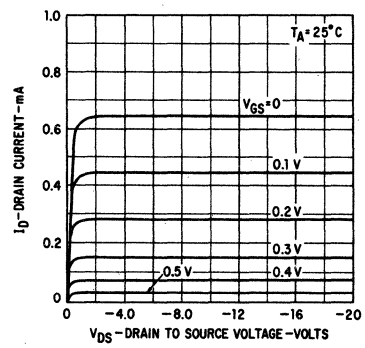


TYPICAL ELECTRICAL CHARACTERISTICS
(2N5020 ONLY)

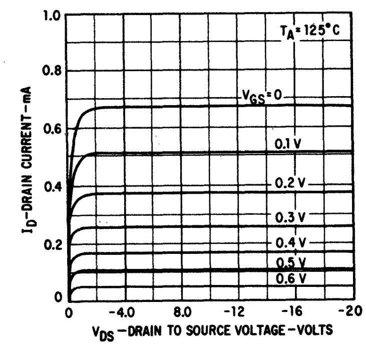
DRAIN CHARACTERISTICS



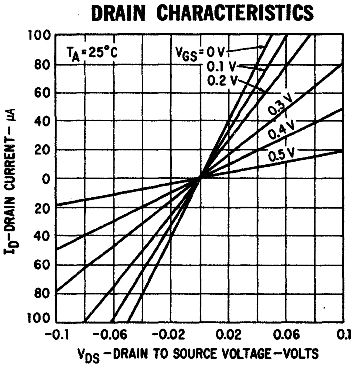
DRAIN CHARACTERISTICS



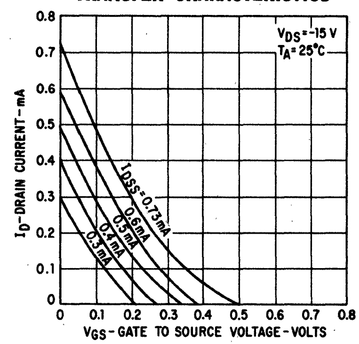
DRAIN CHARACTERISTICS



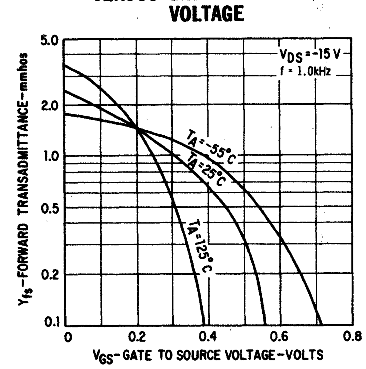
LOW VOLTAGE DRAIN CHARACTERISTICS



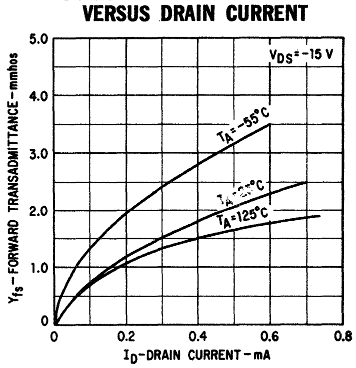
TRANSFER CHARACTERISTICS



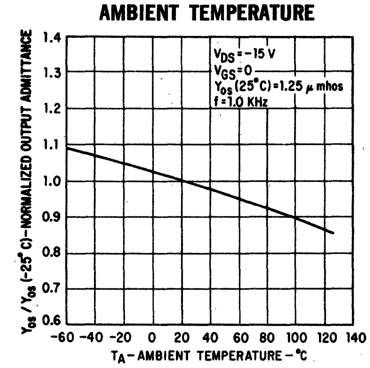
FORWARD TRANSADMITTANCE VERSUS GATE TO SOURCE VOLTAGE



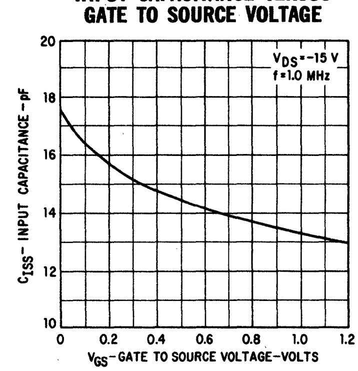
FORWARD TRANSADMITTANCE VERSUS DRAIN CURRENT



NORMALIZED OUTPUT ADMITTANCE VERSUS AMBIENT TEMPERATURE



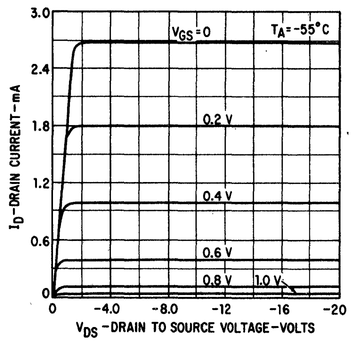
INPUT CAPACITANCE VERSUS GATE TO SOURCE VOLTAGE



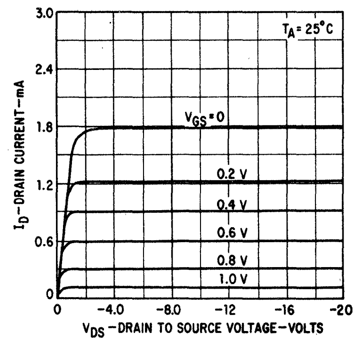
TYPICAL ELECTRICAL CHARACTERISTICS

(2N5021 ONLY)

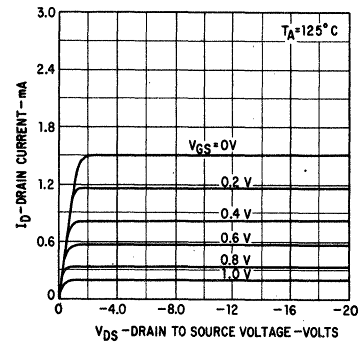
DRAIN CHARACTERISTICS



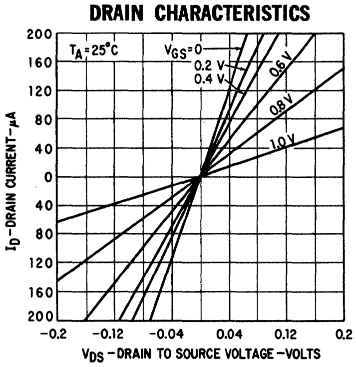
DRAIN CHARACTERISTICS



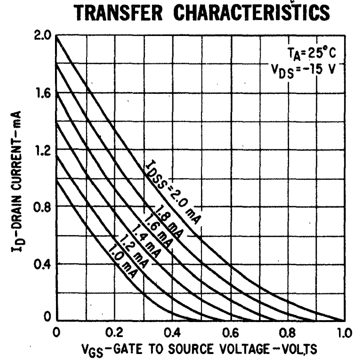
DRAIN CHARACTERISTICS



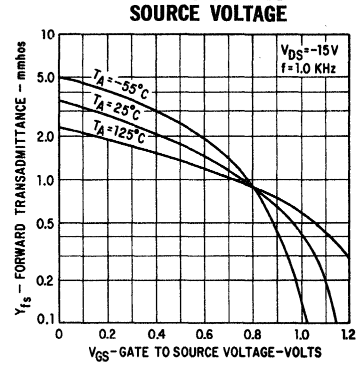
LOW VOLTAGE DRAIN CHARACTERISTICS



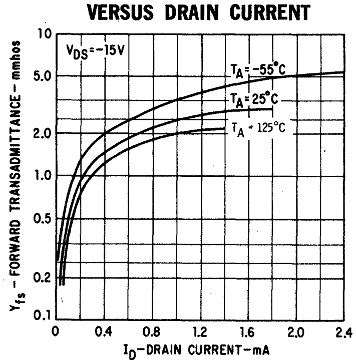
TRANSFER CHARACTERISTICS



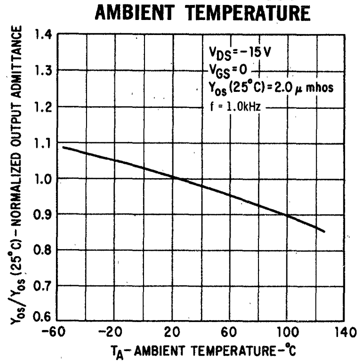
FORWARD TRANSADMITTANCE VERSUS GATE TO SOURCE VOLTAGE



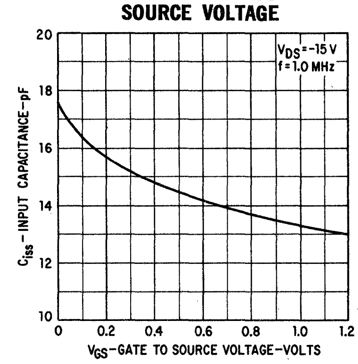
FORWARD TRANSADMITTANCE VERSUS DRAIN CURRENT



NORMALIZED OUTPUT ADMITTANCE VERSUS AMBIENT TEMPERATURE



INPUT CAPACITANCE VERSUS GATE TO SOURCE VOLTAGE



FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

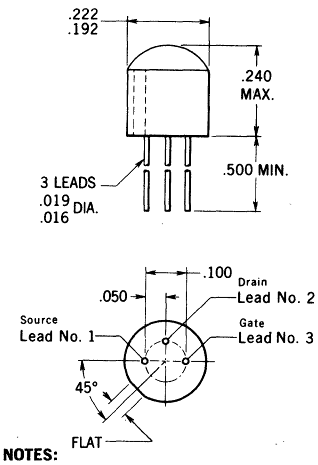
2N5163

N-CHANNEL FIELD-EFFECT TRANSISTOR

DIFFUSED SILICON PLANAR* II TRANSISTOR

- **LOW-COST EPOXY PACKAGE**
- **VERY LOW NOISE . . . . $e_n = 50\ nV/\sqrt{Hz}$ (MAX) AT 1.0 kHz**
  . . . . 1.0 kHz NF = 0.1 dB (TYP) AT 1.0 MΩ
- **HIGH GAIN . . . . $y_{fs} = 2{,}000 - 9{,}000\ \mu mhos$**
- **LOW "ON" RESISTANCE . . . $r_{ds(on)} = 500\ \Omega$ (MAX)**
- **LOW LEAKAGE . . . . $I_{GSS} = 10\ nA$ (MAX)**

PHYSICAL DIMENSIONS
In accordance with JEDEC (TO-106) outline



NOTES:
All dimensions in inches
All leads electrically isolated from case
Package weight is 0.31 gram. Package is electrically non-conductive material

ABSOLUTE MAXIMUM RATINGS (Note 1)

Maximum Temperatures

Operating Junction Temperature	125°C
Storage Temperature	−55°C to +125°C
Soldering Temperature (10 second time limit)	260°C

Maximum Power Dissipation

Total Dissipation at 25°C Ambient Temperature (Note 2)	0.2 Watt

Maximum Voltages

V_{SG}	Source to Gate Voltage	25 Volts
V_{DS}	Drain to Source Voltage	25 Volts
V_{DG}	Drain to Gate Voltage	25 Volts
I_G	Gate Current	50 mA

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
Y_{fs}	**Forward Transadmittance (f = 1.0 kHz)**	**2,000**	**6,000**	**9,000**	**μmhos**	**$V_{DS} = 15$ V**	**$V_{GS} = 0$**
$Re(y_{fs})$	Forward Transconductance (f = 1.0 MHz)	1,800	5,500		μmhos	$V_{DS} = 15$ V	$V_{GS} = 0$
e_n	**Equivalent Input Noise Voltage (f = 1.0 kHz, BW = 150 Hz)**		**12**	**50**	**$nV/\sqrt{Hz}$**	**$V_{DS} = 15$ V**	**$I_D = 1.0$ mA**
NF	Noise Figure (f = 1.0 kHz, R_G = 150 kΩ, BW = 150 Hz)			3.0	dB	$V_{DS} = 15$ V	$I_D = 1.0$ mA
NF	**Noise Figure (f = 1.0 kHz, R_G = 1.0 MΩ, BW = 150 Hz)**		**<0.1**		**dB**	**$V_{DS} = 15$ V**	**$I_D = 1.0$ mA**
$r_{ds(on)}$	**Drain "On" Resistance** (f = 1.0 kHz)		**125**	**500**	**ohms**	**$V_{GS} = 0$**	**$I_D = 0$**
I_{DSS}	Drain Current	1.0	14	40	mA	$V_{DS} = 15$ V	$V_{GS} = 0$
$V_{GS(off)}$	**Gate to Source Cutoff Voltage**	**−0.4**	**−3.7**	**−8.0**	**Volts**	**$V_{DS} = 15$ V**	**$I_D = 1.0\ \mu A$**
V_{GS}	Gate to Source Voltage		−3.5	−7.5	Volts	$V_{DS} = 15$ V	$I_D = 100\ \mu A$
I_{GSS}	**Gate Reverse Current**		**0.1**	**10**	**nA**	**$V_{GS} = -15$ V**	**$V_{DS} = 0$**
I_{GSS}(85°C)	Gate Reverse Current		0.03	0.6	μA	$V_{GS} = -15$ V	$V_{DS} = 0$
C_{rss}	Reverse Transfer Capacitance (f = 1.0 MHz)		1.3	3.0	pF	$V_{DS} = 15$ V	$V_{GS} = 0$
C_{iss}	Input Capacitance (f = 1.0 MHz)		8.7	12	pF	$V_{DS} = 15$ V	$V_{GS} = 0$
Y_{os}	Output Admittance (f = 1.0 kHz)		60	200	μmhos	$V_{DS} = 15$ V	$V_{GS} = 0$
BV_{GSS}	Gate to Source Breakdown Voltage	−25			Volts	$V_{DS} = 0$	$I_G = 10\ \mu A$

NOTES:

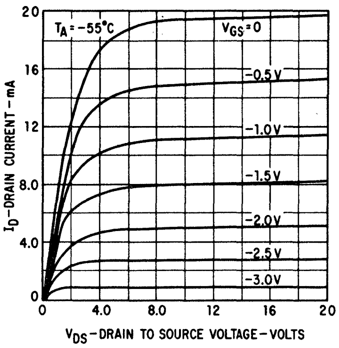
*Planar is a patented Fairchild process.

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
(2) These ratings give a maximum junction temperature of 125°C and junction to ambient thermal resistance of 500°C/Watt (derating factor of 2.0 mW/°C).

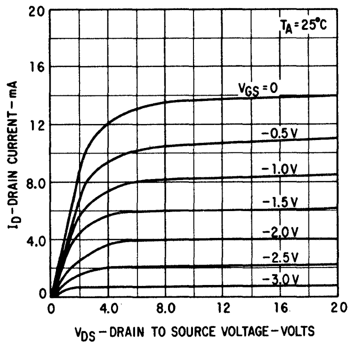
FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

TYPICAL ELECTRICAL CHARACTERISTICS

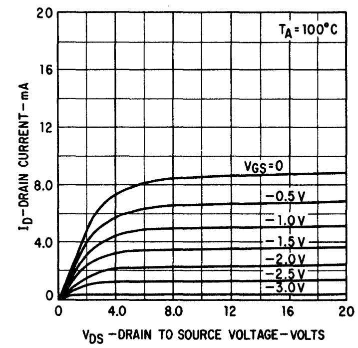
DRAIN CHARACTERISTICS



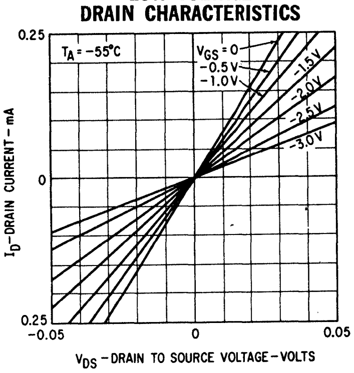
DRAIN CHARACTERISTICS



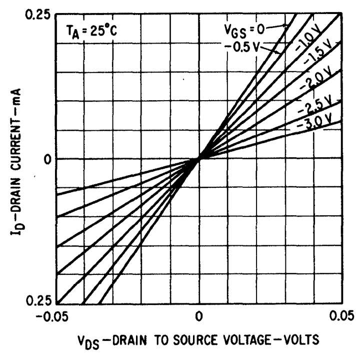
DRAIN CHARACTERISTICS



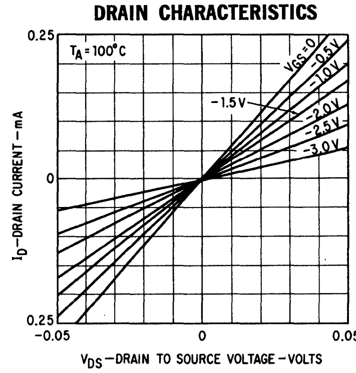
LOW VOLTAGE DRAIN CHARACTERISTICS



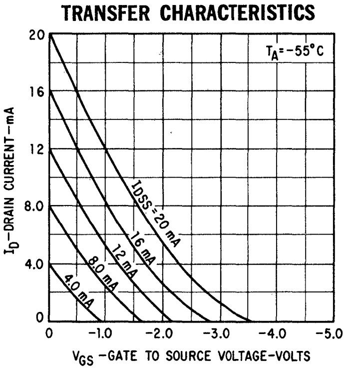
LOW VOLTAGE DRAIN CHARACTERISTICS



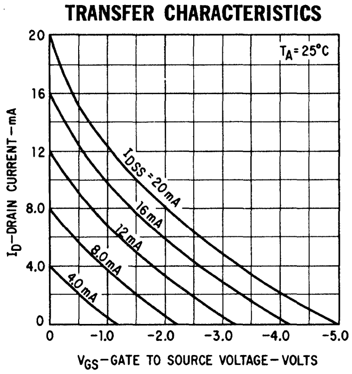
LOW VOLTAGE DRAIN CHARACTERISTICS



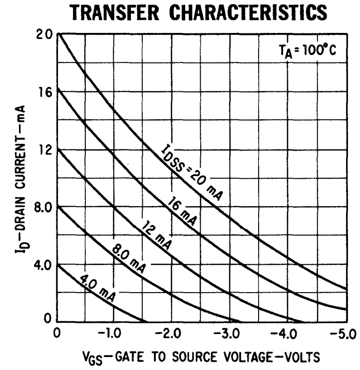
TRANSFER CHARACTERISTICS



TRANSFER CHARACTERISTICS

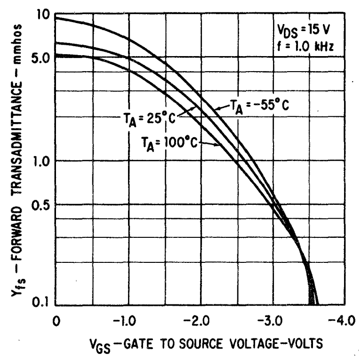


TRANSFER CHARACTERISTICS

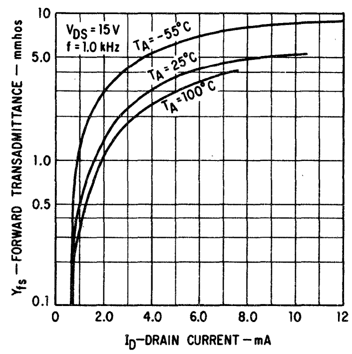


TYPICAL ELECTRICAL CHARACTERISTICS

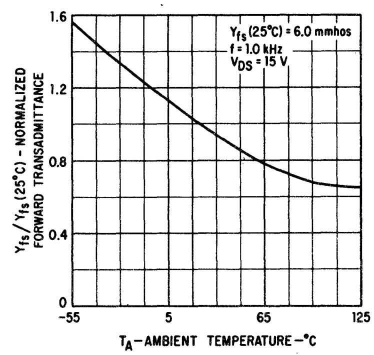
FORWARD TRANSADMITTANCE VERSUS GATE TO SOURCE VOLTAGE



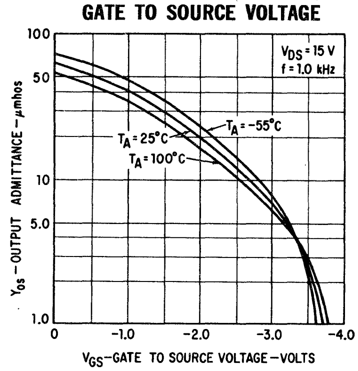
FORWARD TRANSADMITTANCE VERSUS DRAIN CURRENT



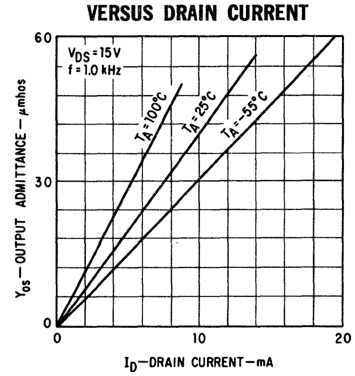
NORMALIZED FORWARD TRANSADMITTANCE VERSUS AMBIENT TEMPERATURE



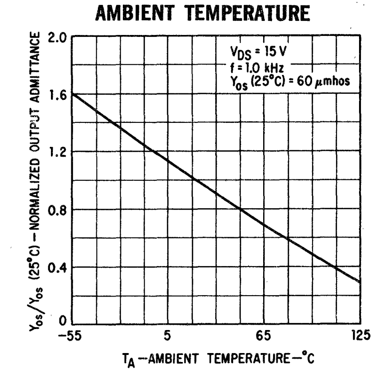
OUTPUT ADMITTANCE VERSUS GATE TO SOURCE VOLTAGE



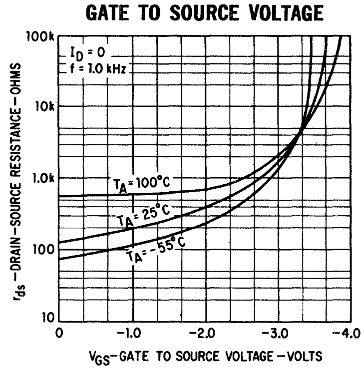
OUTPUT ADMITTANCE VERSUS DRAIN CURRENT



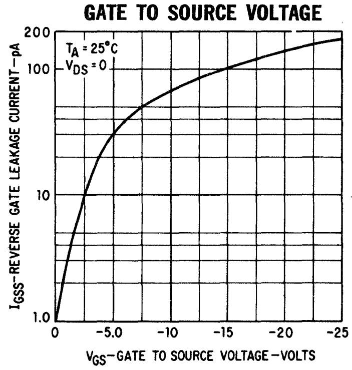
NORMALIZED OUTPUT ADMITTANCE VERSUS AMBIENT TEMPERATURE



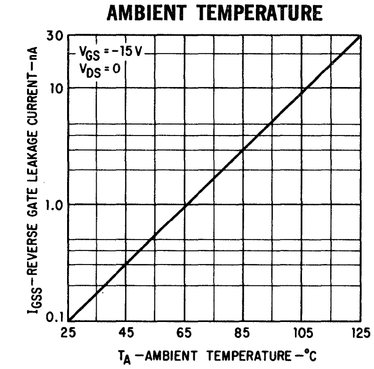
DRAIN SOURCE RESISTANCE VERSUS GATE TO SOURCE VOLTAGE



REVERSE GATE LEAKAGE CURRENT VERSUS GATE TO SOURCE VOLTAGE

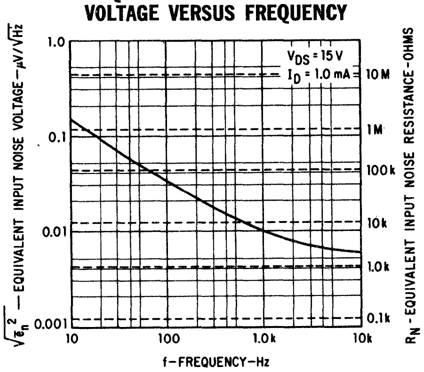


REVERSE GATE LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE

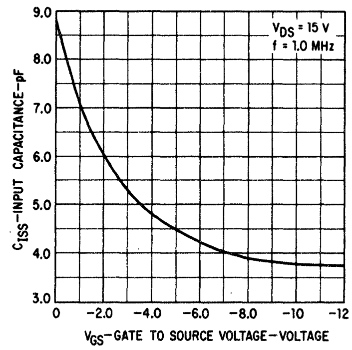


TYPICAL ELECTRICAL CHARACTERISTICS

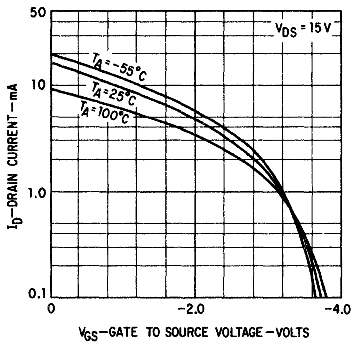
EQUIVALENT INPUT NOISE VOLTAGE VERSUS FREQUENCY



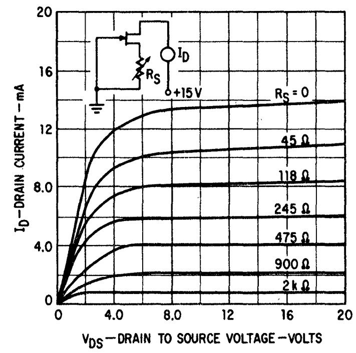
INPUT CAPACITANCE VERSUS GATE TO SOURCE VOLTAGE



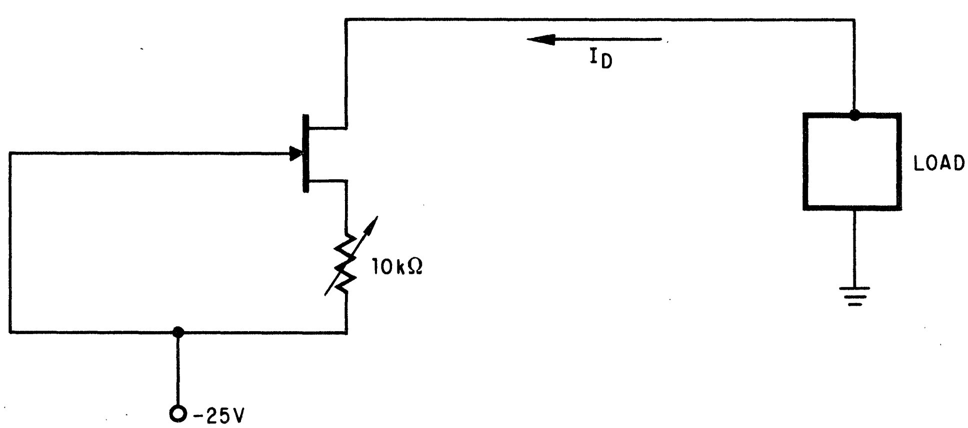
DRAIN CURRENT VERSUS GATE TO SOURCE VOLTAGE



DRAIN CURRENT VERSUS DRAIN TO SOURCE VOLTAGE WITH SOURCE RESISTANCE



CONSTANT CURRENT SOURCE



FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION