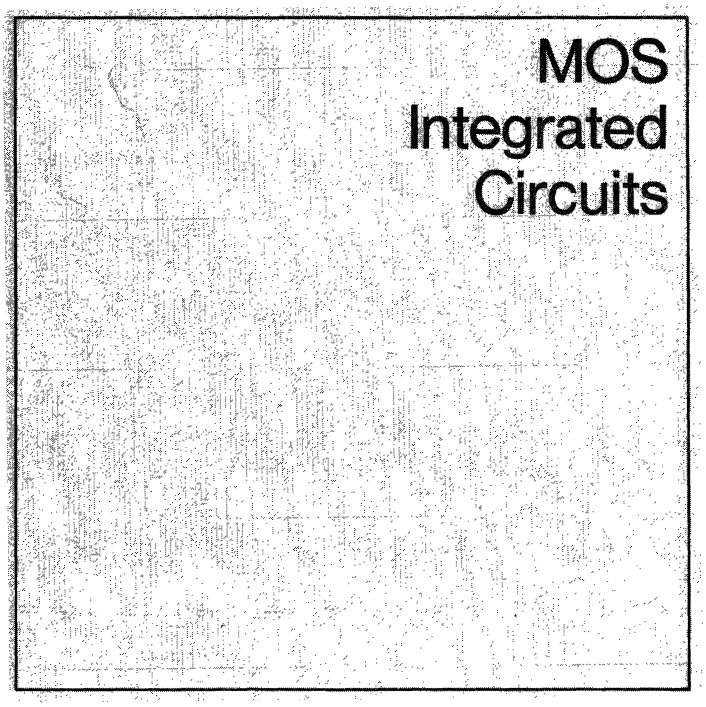

MOS
Integrated
Circuits

MOS INTEGRATED CIRCUITS NUMERICAL INDEX

MOS CROSS REFERENCE

Function	TO-5	Flat Pack	DIP
MOS			
Building Blocks			
*3100 — Dual 5-Input Gate			X
*3101 — Dual J-K Flip-Flop			X
*3102 — 3-Input Breadboard Gate	X		
Display Subsystems			
3250 — CRT Numeric Display Gen.			X
Shift Register — Static			
*3300 — 25-Bit Static Shift Regis.	X		
*3304 — Dual 16-Bit Static Shift Register 2	X		
*3305 — Quad 16-Bit Static Shift Register			X
*3306 — Dual 16-Bit Single 32-Bit Static Shift Register	X		
*3801 — 10-Bit Ser/Para-Para/Ser			X
Shift Register — Dynamic			
*3303 — Dual 25-Bit Dynamic Shift Register	X		
*3320 — 64-Bit, 4-Phase Dynamic Shift Register	X		
3321 — Dual 256-Bit, 4-Phase Dynamic Shift Register			
Memory — Read-Only			
*3500 — 256-Bit Read-Only Memory			
*3501 — 1024-Bit Read-Only Memory			X
Multiplex Switches			
*3700 — 4-Channel Multiplex Switch			
*3701 — 6-Channel Multiplex Switch			
*3705 — 8-Channel Multiplex Switch			X
Converters			
*3750 — 10-Bit D/A Converter		X	X
*3751 — 12-Bit A/D Converter		X	X
*3801 — Same as Shift Reg. Static			
Logic Subsystems			
*3800 — 8-Bit Accumulator			X

*Products with asterisks have data sheets available, those without — data sheets will be out in the near future.

3100
FIVE-INPUT GATE
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3100 dual five-input gate is a MOS monolithic integrated circuit. This device can be utilized as a logic block in an all MOS system, or as a breadboarding gate in designing customer integrated circuits. Input protection is provided on all inputs.

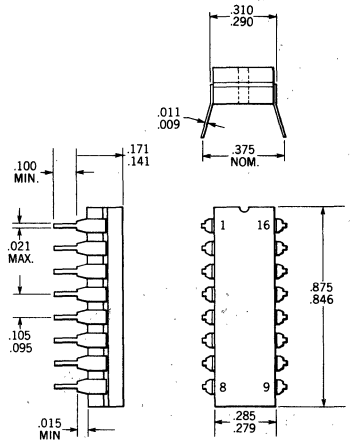
FEATURES

- **GATE PROTECTION**
- **INVERTED AND NON-INVERTED OUTPUT BUFFERS**
- **AND/OR, NAND/NOR CAPABILITY**

ABSOLUTE MAXIMUM RATINGS (Notes 2 & 3)

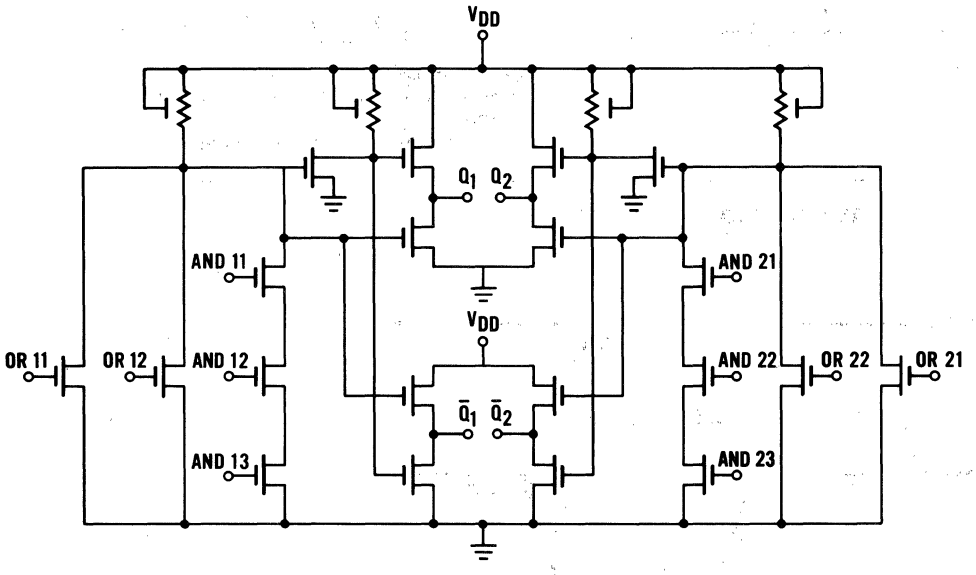
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Power Dissipation at +25°C	200 mW
Positive Voltage on any pin	+0.3 V
Negative Voltage on any pin	−30 V

PHYSICAL DIMENSIONS
16 Lead Dual In-Line

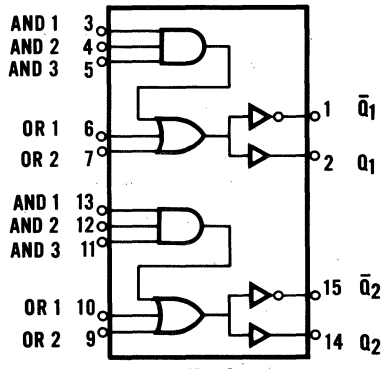


ORDER PART NO. A6J310014X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



NOTE: Polarity indicators (o) external to the solid box conform to MIL-STD-806B where 0 indicates the less positive state is active. Internal to the box and in the remainder of this data sheet conventional MOS polarities are used, where HI = "1" ≃ −10V and LO = "0" ≃ Gnd.

NOTES:
(1) These ratings are limiting values above which serviceability may be impaired.
(2) Voltage levels are with respect to GND Pin.

Electrical Characteristics on Page 2

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

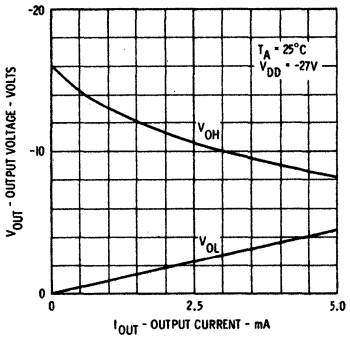
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD MOS INTEGRATED CIRCUIT • 3100

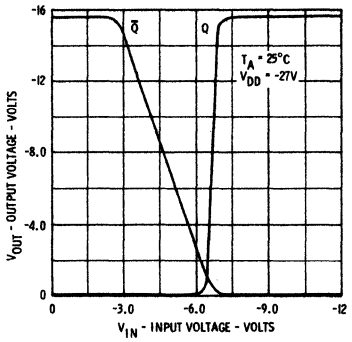
ELECTRICAL CHARACTERISTICS ($V_{DD} = -27 \pm 2$ Volts, Load = 10 MΩ, 10 pF, $T_A = +25°C$ unless otherwise specified)

CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Output Impedance to Ground		1.0	1.5	kΩ	$I_{OUT} = 100\ \mu A$
Input Leakage Current			1.0	μA	$V_{IN} = -20$ V
Input Capacitance		5.0		pF	$V_{IN} = 0$ V
Input Logic Levels					
"0" Level	0		−2.0	Volts	
"1" Level	−9.0			Volts	
Input Data Pulse Width	0.5			μs	
Output Logic Levels					
"0" Level			−1.0	Volts	
"1" Level	−10			Volts	
t_{pd+} (Q)		0.4		μs	
t_{pd-} (Q)		0.4		μs	
t_{pd+} ($\bar{Q}$)		0.4		μs	
t_{pd-} ($\bar{Q}$)		0.6		μs	
Power Consumption		60		mW	

TYPICAL OUTPUT CHARACTERISTIC



TYPICAL TRANSFER CHARACTERISTICS



TRUTH TABLE

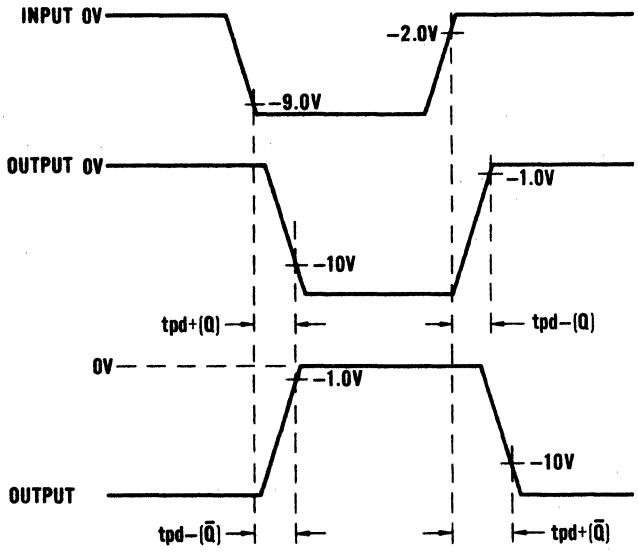
A OR_1	B OR_2	C AND_1	D AND_2	E AND_3	Q	$\bar{Q}$
0	0	0	0	0	0	1
0	0	0	0	1	0	1
0	0	0	1	0	0	1
0	0	0	1	1	0	1
0	0	1	0	0	0	1
0	0	1	0	1	0	1
0	0	1	1	0	0	1
0	0	1	1	1	1	0
0	1	X	X	X	1	0
1	0	X	X	X	1	0
1	1	X	X	X	1	0

Logical '1' is more negative than −9.0 V
Logical '0' is more positive than −2.0 V and ≤ 0 V
X is either '1' or '0'

BOOLEAN FUNCTION: $Q = \overline{A + B + C \cdot D \cdot E}$

$\bar{Q} = \overline{A + B + C \cdot D \cdot E}$

TYPICAL PROPAGATION DELAY



3101
DUAL JK FLIP-FLOP
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3101 dual JK flip-flop is a MOS monolithic integrated circuit utilizing P-Channel enhancement technology. This device can be utilized as a logic block in an all MOS system, or as a breadboarding flip-flop in designing custom integrated circuits. Input protection is provided on all inputs.

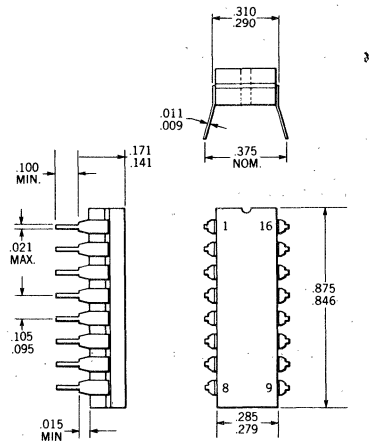
FEATURES

- **INPUT PROTECTION**
- **BUFFERED OUTPUTS**
- **ASYNCHRONOUS SET AND CLEAR**
- **SEPARATE CLOCK LINES**

ABSOLUTE MAXIMUM RATINGS (Notes 1 & 2)

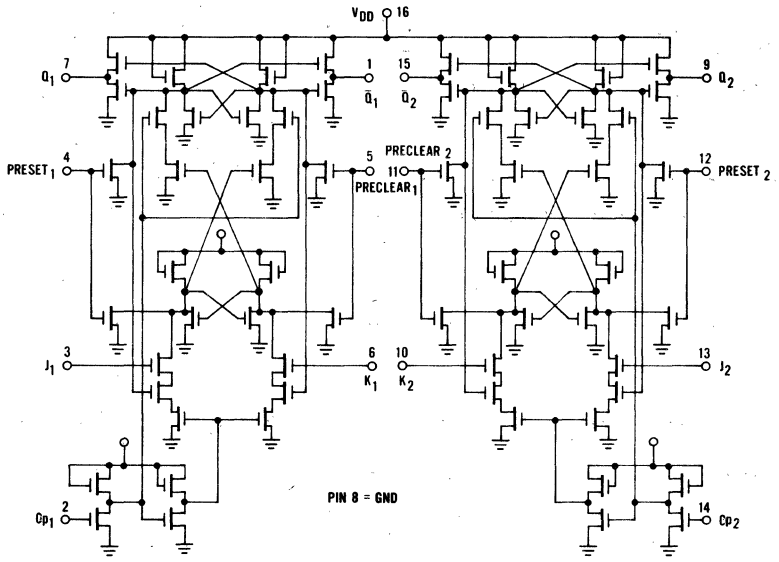
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Power Dissipation at +25°C	200 mW
Positive Voltage on any pin	+0.3 V
Negative Voltage on any input pin	−30 V

PHYSICAL DIMENSIONS
16 Lead Dual In-Line

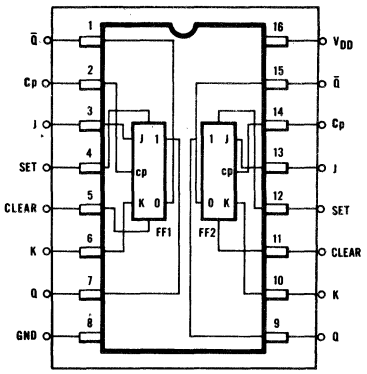


ORDER PART NO. A6J310114X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



NOTE: Polarity indicators (o) external to the solid box conform to MIL-STD-806B where 0 indicates the less positive state is active. Internal to the box and in the remainder of this data sheet conventional MOS polarities are used, where HI = "1" ≃ −10V and LO = "0" ≃ Gnd.

NOTES:
(1) These ratings are limiting values above which serviceability may be impaired.
(2) Voltage levels are with respect to the GND Pin.

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ELECTRICAL CHARACTERISTICS ($V_{DD} = -27 \pm 2$ Volts, $T_A = 25°C$ unless otherwise specified)

CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Clock Frequency	DC		250	kHz	$V_{DD} = -26$ V
Clock Amplitude	−9.0			Volts	
Clock Pulse Width	1.0			μs	
Input Leakage Current			1.0	μA	$V_{IN} = -20$ V
Input Capacitance		5.0		pF	$V_{IN} = 0$ V
Input Logic Levels					
"0" Level	0		−2.0	Volts	
"1" Level	−9.0			Volts	
Input Data Pulse Width	1.0			μs	
Output Impedance to Ground			1.0	kΩ	
Output Logic Levels					
"0" Level			−1.0	Volts	
"1" Level	−10			Volts	
t_{setup}		0.5		μs	
$t_{release}$		0.5		μs	
t_{pd+}		1.0		μs	
t_{pd-}		0.5		μs	
Power Consumption		75		mW	

TRUTH TABLE

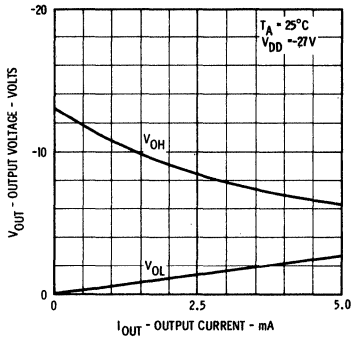
J	K	Q
t = n		t = n + 1
0	0	X^n
0	1	0
1	0	1
1	1	$\overline{X}^n$

Logical '1' is more negative than −9.0 V

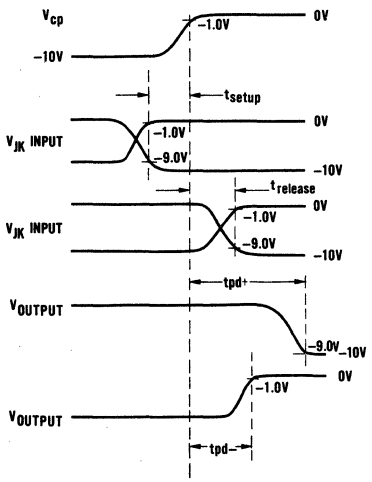
Logical '0' is more positive than −2.0 V and ≤ 0

X^n is the output state at time n

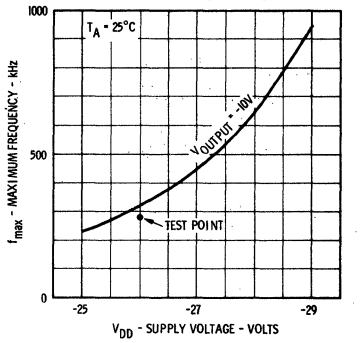
TYPICAL OUTPUT CHARACTERISTICS



TYPICAL SWITCHING WAVEFORMS



MAXIMUM FREQUENCY VERSUS SUPPLY VOLTAGE



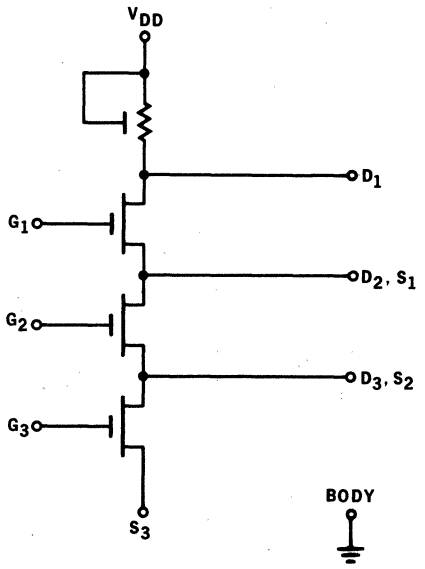
3102
3 INPUT GATE
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3102 is a MOS Monolithic 3-Input Gate Integrated Circuit. This device can be utilized as a vehicle in gaining familiarity with MOS integrated circuit logic versatility, as a building block in an all MOS system, or as a breadboarding gate in designing complex custom integrated circuits. Input protection is provided on all gate inputs.

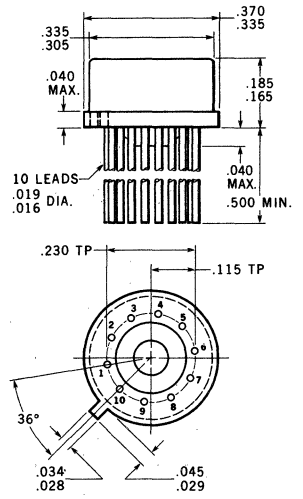
ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Positive Voltage on any Pin ($V_{Body} = 0$)	+0.3 Volt
Negative Voltage on any Pin ($V_{Body} = 0$)	−35 Volts
Power Dissipation at $T_A = 25°C$	≤200 mW

SCHEMATIC DIAGRAM



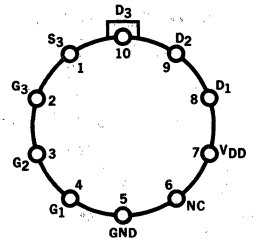
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO-100)



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART NO. A5F3102XXX

CONNECTION DIAGRAM



TOP VIEW

NOTES:
(1) These ratings are limiting values above which serviceability of the device may be impaired.

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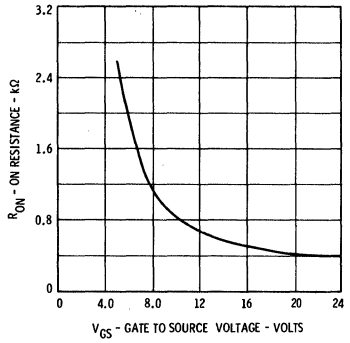
ELECTRICAL CHARACTERISTICS ($V_{Body} = 0$; $T_A = 25°C$)

CHARACTERISTICS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
R_{Load}	$V_{DD} = -27\ V \pm 2.0\ V$ $V_{D1} = Gnd$		140		kΩ
R_{ON}(See Figure 1)	$V_{IN} = -20\ V$		500		Ω
Input Leakage Current	$V_{IN} = -25\ V$			1.0	μA
Threshold Voltage (V_{TH})	$V_D = V_G$, $I_D = -10\ \mu A$	−2.0		−5.5	V
Input Capacitance			4.0		pF
Power Consumption	$V_{DD} = -30\ V$, $V_{IN} = -10\ V$		6.0		mW

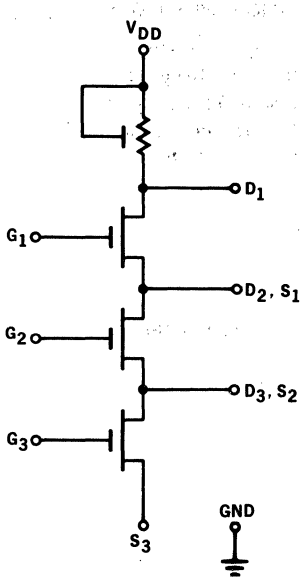
FIG. 1
TYPICAL "ON" RESISTANCE



RESISTANCE CHARACTERISTIC

Parameters	Conditions	TYP.
R_{Load}	$V_{DD} = -25\ V$ $V_{D1} = 0\ V$	140 kΩ
R_{ON}	$V_{GS} = -20\ V$ $V_{DS} \leq -1.0\ V$ $V_{D2} = 0\ V$	500 Ω
R_{ON}	$V_{GS} = -9.0\ V$ $V_{DS} \leq -1.0\ V$ $V_{D2} = 0\ V$	800 Ω

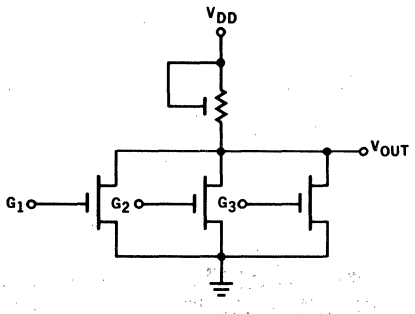
SCHEMATIC DIAGRAM



NOR GATE CONFIGURATION

Pin 8 = Pin 10 = V_{OUT}
Pin 1 = Pin 9 = GND
$V_{DD} = -27\ V \pm 2.0\ V$

	LOGIC LEVEL	VOLTAGE LEVEL MIN.	VOLTAGE LEVEL MAX.
V_{IH}	1	−9.0 V	
V_{IL}	0		−2.0 V
V_{OH}	1	−10 V	
V_{OL}	0		−1.0 V



NAND GATE CONFIGURATION

Pin 5 = GND
Pin 8 = OUTPUT
$V_{DD} = -27\ V \pm 2.0\ V$

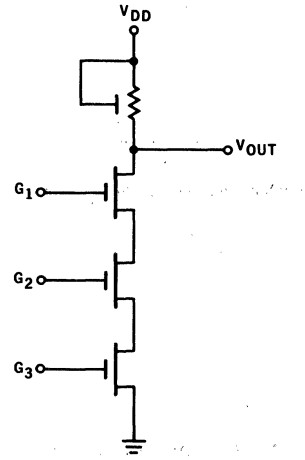


FIG. 2
TYPICAL DRAIN TO SOURCE CHARACTERISTICS

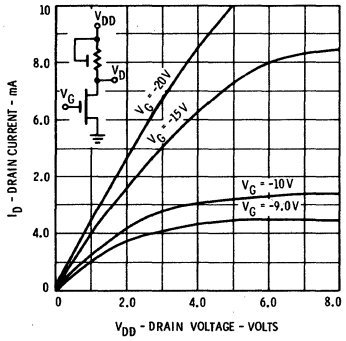
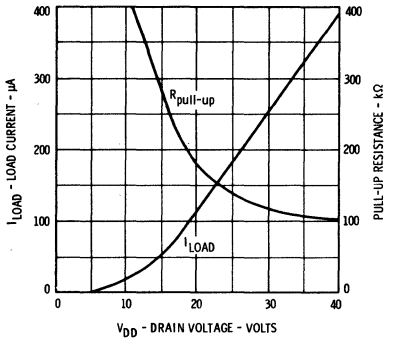
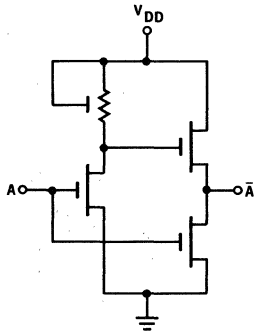


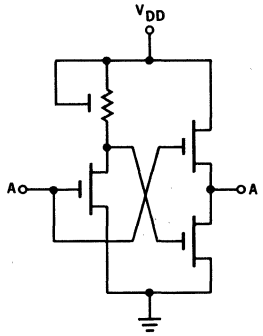
FIG. 3
TYPICAL PULL-UP RESISTANCE



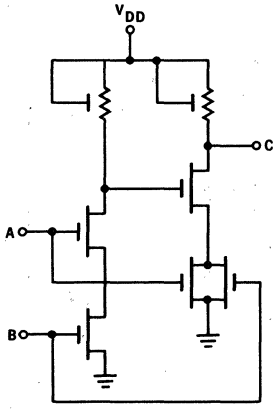
APPLICATIONS — MOS logic will provide the versatility to build many different functions. The following circuits show how to build the functions using one or two 3102 packages.



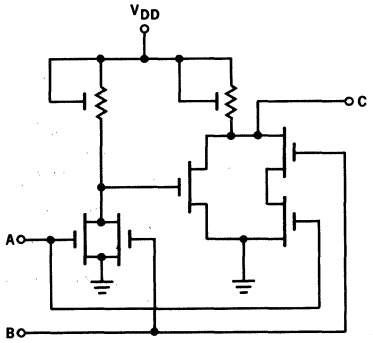
INVERTING BUFFER



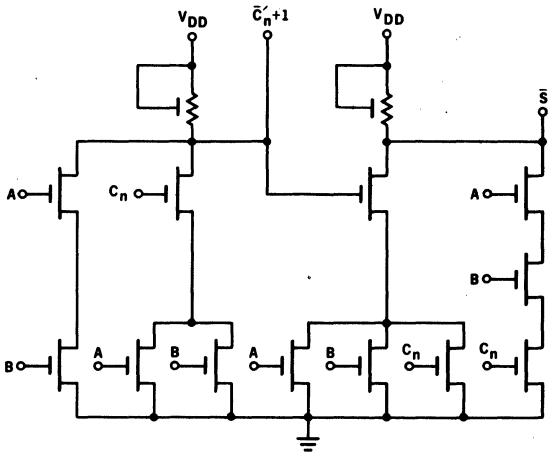
NON-INVERTING BUFFER



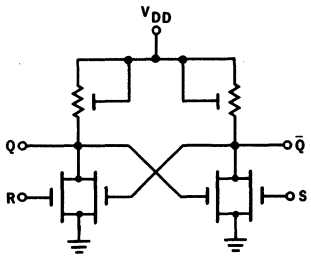
$C = AB + \bar{A}\bar{B}$
EXCLUSIVE NOR



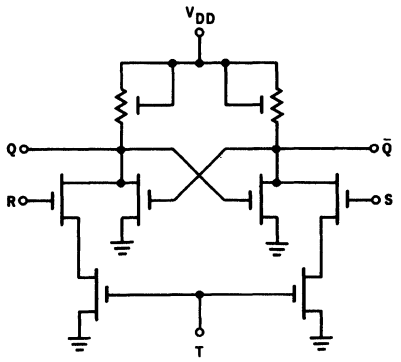
$C = \bar{A}B + \bar{B}A$
EXCLUSIVE OR



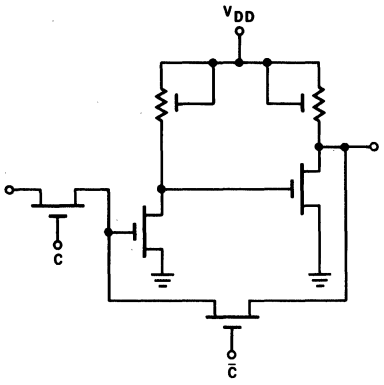
$C'_{n+1} = AB + C_n(A + B)$
$S = (A+B+C_n)\,C'_{n+1} + ABC_n$
FULL ADDER



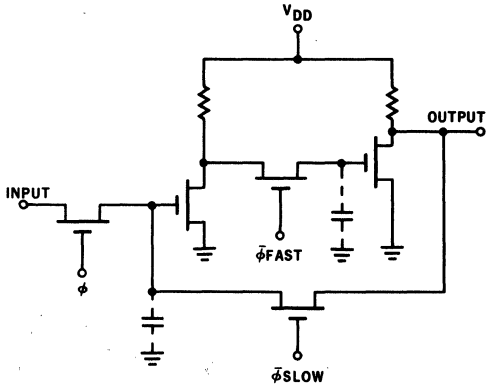
RS FLIP-FLOP



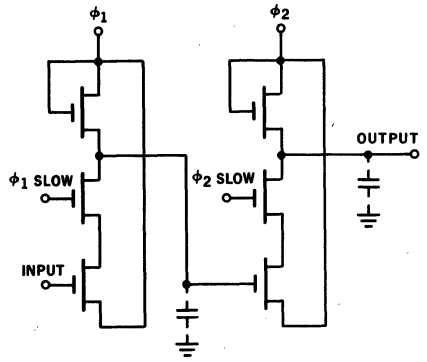
RST FLIP-FLOP



TYPE D FLIP-FLOP



STATIC (DC) SHIFT REGISTER BIT



DYNAMIC 4-PHASE (4 ϕ) SHIFT REGISTER BIT

3300

25 BIT STATIC SHIFT REGISTER

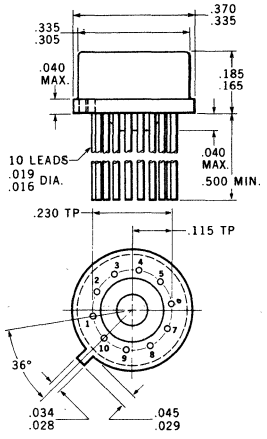
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION—The 3300 is a 25 bit Static Shift Register. It is a monolithic integrated circuit utilizing Planar II*, P-channel enhancement mode MOS technology. Input and output access is made available in 16, 8 and 1 bit increments. This device was designed for use in single phase clock sequential digital systems as a delay line or memory element.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Power Dissipation at $T_A = 25°C$	200 mW
Voltage On Clock, Inputs and Supply Pins	−35 V to +0.3 V

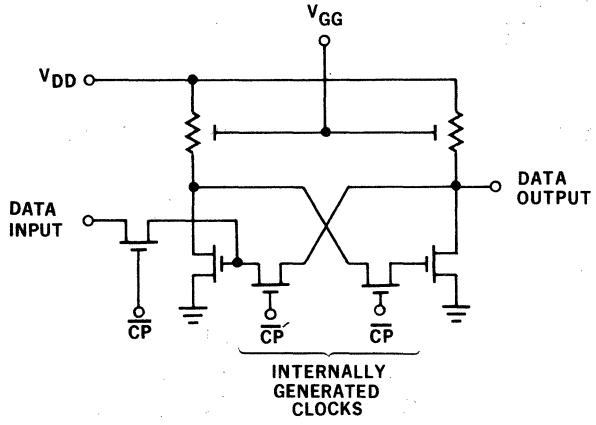
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO−100)



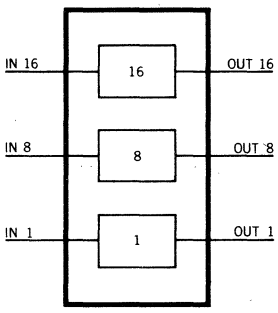
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER CODE A5F330014X

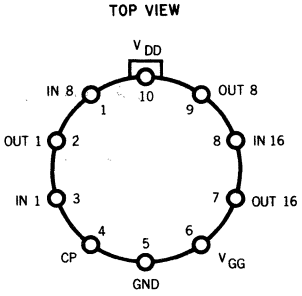
SCHEMATIC DIAGRAM
(ONE BIT)



BLOCK DIAGRAM



CONNECTION DIAGRAM



*Planar is a patented Fairchild process.

NOTE: These ratings are limiting values above which the serviceability of the device may be impaired.

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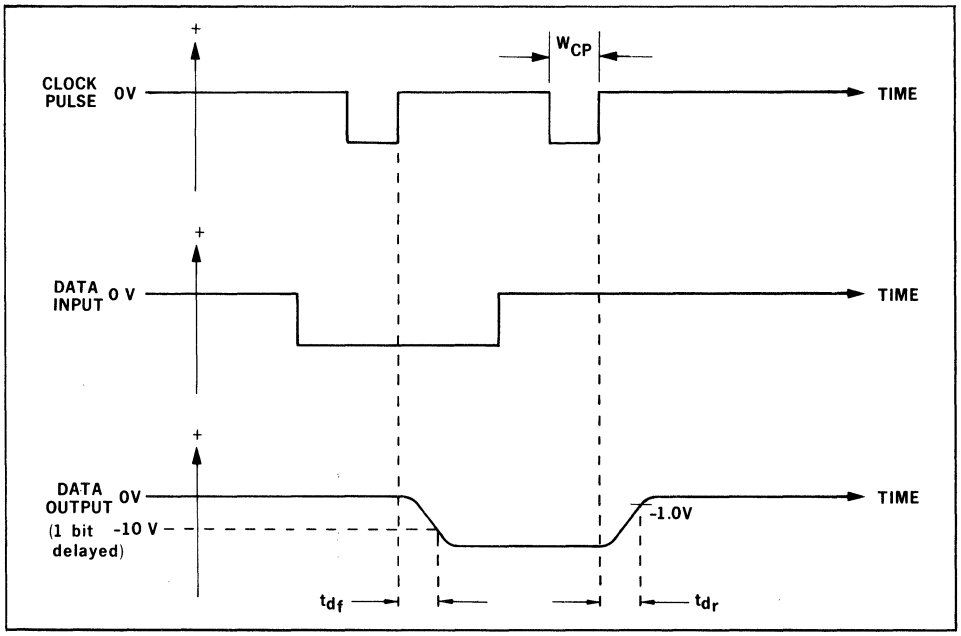
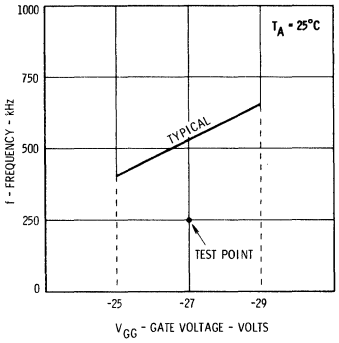
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, V_{GG} (Pin 6) $= -27 \pm 2$ V, V_{DD} (Pin 10) $= -13 \pm 2$ V, unless otherwise specified)

SYMBOL	CHARACTERISTICS		MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
	Power Consumption			50		mW	$V_{clock} = 0$ V
	Operating Frequency		0		250	kHz	$V_{GG} = -27$ V
V_{CP}	Clock Pulse Amplitude	"0" level			−2.0	Volts	
		"1" level	−9.0			Volts	
W_{CP}	Clock Pulse Width		1.0		100	μs	
	Clock Pulse Rise and Fall Time				10	μs	
	Clock Capacitance			3.0		pF	$V_{CP} = 0$ V
I_{CL}	Clock Leakage Current				−1.0	μA	$V_{CP} = -20$ V
V_{IL}	Input Amplitude	"0" level			−2.0	Volts	
V_{IH}		"1" level	−9.0			Volts	
C_{in}	Input Capacitance			2.5		pF	$V_{in} = 0$ V
I_{IL}	Input Leakage Current				−1.0	μA	$V_{in} = -20$ V
V_{OL}	Output Levels	"0" level			−1.0	Volts	$I_{out} = -10$ μA
V_{OH}		"1" level	−10			Volts	$I_{out} = -10$ μA
t_{df}	Time Delay-Fall			1.0		μs	
t_{dr}	Time Delay-Rise			1.2		μs	

TIMING DIAGRAM



TYPICAL OPERATING FREQUENCY VERSUS GATE VOLTAGE



3303

MOS DUAL 25 BIT DYNAMIC SHIFT REGISTER

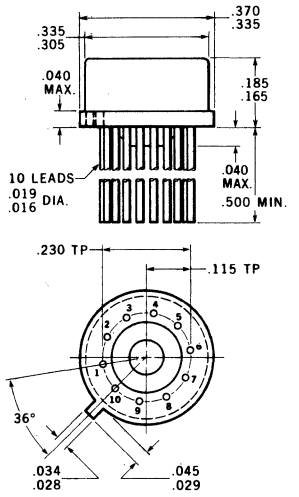
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3303 is a Dual 25 Bit Dynamic Shift Register. It is a monolithic integrated circuit utilizing Planar* II, P-Channel enhancement mode MOS technology. A two phase clock is used to reduce power consumption and increase speed.

ABSOLUTE MAXIMUM RATINGS (Note 1)

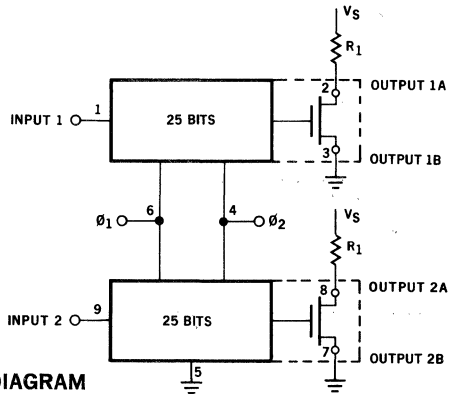
Clock Voltages ($V_{\phi_1} = V_{\phi_2}$)	−30 V to +0.3 V
Data Input Voltage (V_{in})	−30 V to +0.3 V
Supply Voltage	−30 V to +0.3 V
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C

PHYSICAL DIMENSIONS
(In accordance with JEDEC TO−100)



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

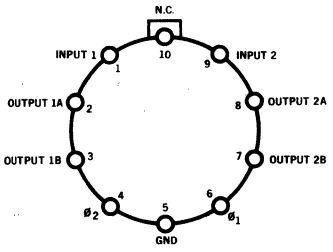
ORDER PART NO. A5F330314X



LOGIC DIAGRAM

The output device requires an external resistor (R_1), ground and power supply (V_S) and can be used either as an inverter or source follower (inverter shown).

CONNECTION DIAGRAM



TOP VIEW

NOTE:
(1) These ratings are limiting values above which the serviceability of the device may be impaired.

Electrical Characteristics on Page 2

*Planar is a patented Fairchild process.

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ELECTRICAL CHARACTERISTICS

STANDARD CONDITIONS (unless otherwise specified)

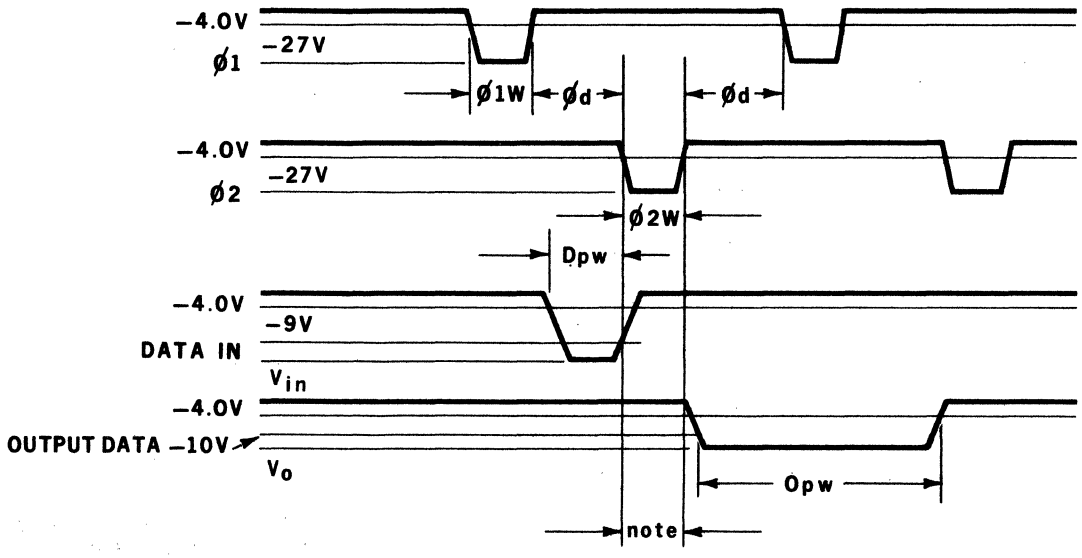
Load . . . 10 MΩ and 10 pF

$V_S = -15\ V \pm 1.0\ V, V\phi = -27\ V \pm 1.0\ V$

$R_l = 20\ k\Omega$, $T_A = -55°C$ to $+85°C$

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
ϕ_1, ϕ_2	Clock Repetition Rate	10		500	kHz	
ϕ_{1w}, ϕ_{2w}	Clock Pulse Width	0.4		45	μs	
ϕ_d	Clock Delay	0.4			μs	
$V\phi$	Clock Pulse Amplitude					
	"0" Level	0		−0.5	Volts	
	"1" Level	−26		−28	Volts	
	Clock Pulse Rise and Fall Time (10% - 90%)			100	ns	
V_{in}	Data Input Logic Levels					
	Logic "0"	0		−2.0	Volts	
	Logic "1"	−9.0			Volts	$\phi_1 = 0.4\ \mu s$
D_{pw}	Data Pulse Width	200			ns	$\phi_2 = 0.4\ \mu s$
V_o	Output Logic Levels					
	Logic "0"			−1.0	Volts	
	Logic "1"	−10			Volts	
	Output Fall Time			550	ns	
O_{pw}	Output Pulse Width	1.0			μs	
R_o	Output Impedance to Ground			1000	Ω	
I_{CL}	Clock Input Leakage Current			100	μA	$V\phi = -26\ V$
	Data Input Capacitance		4.0		pF	$V\phi = 0\ V$
	Clock Input Capacitance		20		pF	$V\phi = 0\ V$
	Fan In			1.0		
	Fan Out			5.0		

TYPICAL WAVEFORMS



Note: Delayed 50 Bit Times

3304

DUAL 16-BIT STATIC SHIFT REGISTER

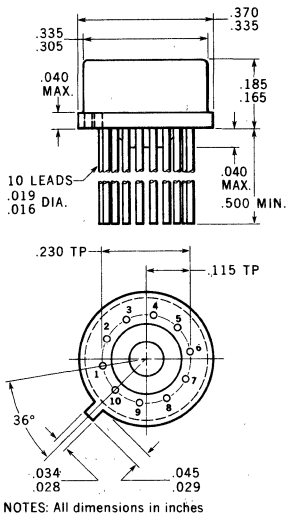
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3304 is a Dual 16-Bit Static Shift Register. It is a monolithic integrated circuit utilizing Planar II*, P-Channel Enhancement Mode MOS Technology. It is designed to operate on a two phase clock in delay line or in serial binary or BCD data storage applications. For DC storage conditions, it is important that ϕ_1 is a logic "0" and ϕ_2 is a logic "1".

ABSOLUTE MAXIMUM RATINGS (Note 1)

Drain Voltage (V_{DD})	−30 V to +0.3 V
Gate Voltage (V_{GG})	−30 V to +0.3 V
Clock and Data Input Voltages	−30 V to +0.3 V
Storage Temperature	−55°C to +150°C
Operating Temperature Range	−55°C to +85°C
	0°C to +70°C
Power Dissipation at $T_A = 25°C$	200 mW

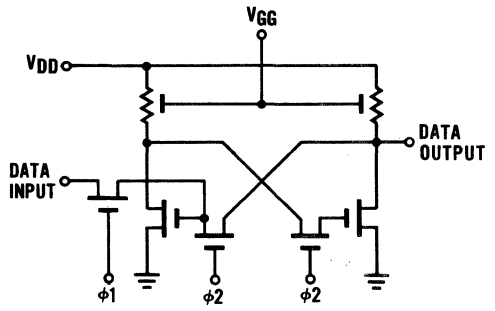
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO−100)



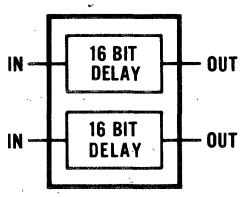
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART # A5F330414X (−55°C to +85°C)
ORDER PART # A5F330419X (0°C to +70°C)

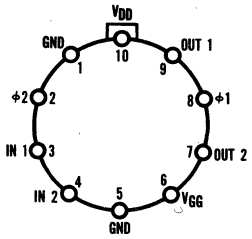
SCHEMATIC DIAGRAM
(ONE BIT)



BLOCK DIAGRAM



CONNECTION DIAGRAM
TOP VIEW



NOTE:
(1) These ratings are limiting values above which the serviceability of the device may be impaired.

*Planar is a patented Fairchild process.

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ELECTRICAL CHARACTERISTICS

(V_{DD} = −13 Volts ±1 Volt, V_{GG} = −27 Volts ± 1 Volt, Load = 10 MΩ and 10 pF, T_A = −55°C to +85°C, unless otherwise specified)

CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Clock Repetition Rate	D.C.		1.0	MHz	
Clock Pulse Widths					
ϕ_1 pw	0.4		10	μs	See Figure 1
ϕ_2 pw	0.4			μs	See Figure 1
Clock Delay (ϕd)	0.01		10	μs	See Figure 1
Clock Pulse Rise and Fall Time (10% to 90%)			5.0	μs	See Figure 1
Clock Pulse Logic Levels (ϕ_1 & ϕ_2)					
Logic "0"			−2.0	Volts	
Logic "1"	−26		−28	Volts	
Clock Pulse Input Capacitance (ϕ_1 & ϕ_2)		4.0		pF	$\phi_1 = \phi_2$ = 0 Volt
Data Pulse Width (Dpw)	0.4			μs	
Data Input Capacitance		2.0		pF	V_{IN} = 0 Volt
Data Input Logic Levels					
Logic "0"			−2.0	Volts	
Logic "1"	−9.0			Volts	
Data Input Leakage Current			1.0	μA	V_{IN} = −20 Volts
Clock Input Leakage Current			100	μA	V_{IN} = −26 Volts
Clock (ϕ_2) Input Impedance	60			kΩ	ϕ_1 = −26 Volts ϕ_2 = 0 Volt
Output Logic Levels					
Logic "0"		−0.5	−1.0	Volts	
Logic "1"	−10	−11		Volts	
Output Impedance to Ground		2.0	3.0	kΩ	Output at Logic "0"
Output Drive Capability	−5.0			Volts	R_L = 4.0 kΩ to Ground
Power Supply Current Drain V_{DD}			10	mA	V_{DD} = −13 Volts
Power Supply Current Drain V_{GG}			2.0	mA	V_{GG} = −27 Volts

TIMING DIAGRAMS

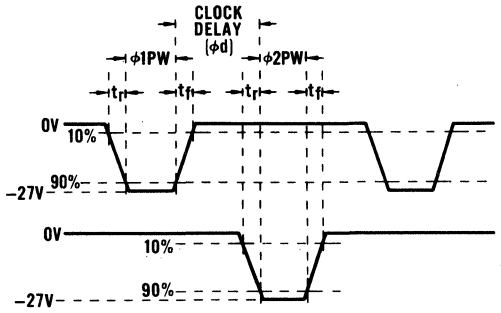


Figure 1

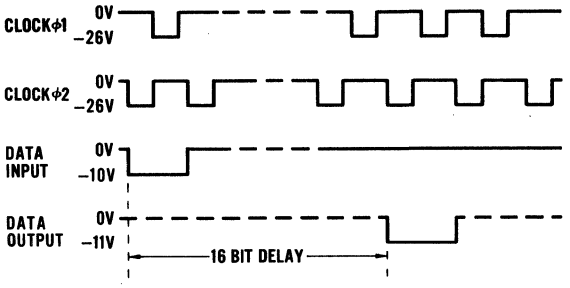
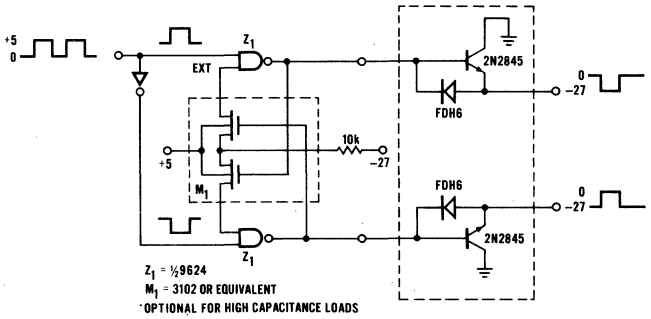


Figure 2



Z_1 = ½9624
M_1 = 3102 OR EQUIVALENT
*OPTIONAL FOR HIGH CAPACITANCE LOADS

2 PHASE-NON-OVERLAPPING CLOCK DRIVER

3320

64 BIT-4Ø-SHIFT REGISTER

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3320 is a 64 bit dynamic shift register plus logic for loading or recirculating information within the circuit. It is a monolithic integrated circuit utilizing Planar* II, P-channel enhancement mode MOS technology.

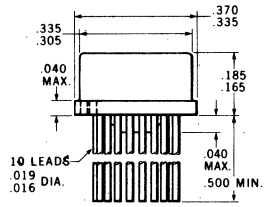
ABSOLUTE MAXIMUM RATINGS

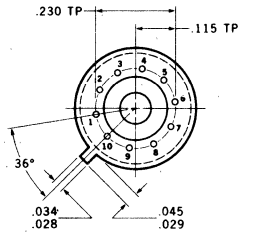
- **CLOCK VOLTAGES ($\phi_1, \phi_2, \phi_3, \phi_4$) . . . —30 V to +0.3 V**
- **DATA INPUT AND STORE VOLTAGES . . . —30 V to +0.3 V**
- **STORAGE TEMPERATURE . . . . . —55°C to +150°C**
- **OPERATING TEMPERATURE RANGE . . . —55°C to +85°C**

FEATURES

- **LOW POWER — 200 μW/BIT AT 2.0 MHz**
- **INPUT STORE AND ENTER CONTROL LOGIC**
- **DATA AND DATA COMPLEMENT OUTPUT**
- **INPUT GATE PROTECTION**
- **TYPICALLY 3.0 VOLT NOISE MARGIN**

PHYSICAL DIMENSIONS
(In accordance with JEDEC TO-100)

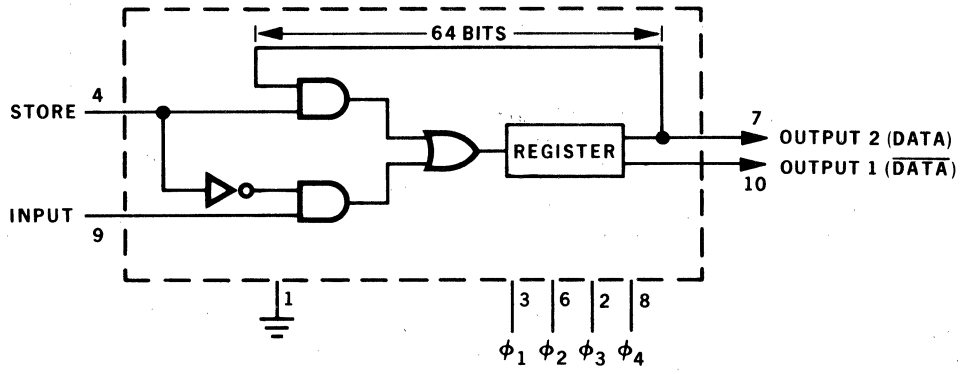


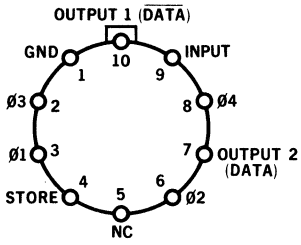


NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART NO. A5F332014X

CONNECTION DIAGRAM





TOP VIEW

*Planar is a patented Fairchild process.

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ELECTRICAL CHARACTERISTICS Standard Conditions (unless otherwise specified)
Load = 10 MΩ and 10 pF, $T_A = -55°C$ to $+85°C$

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Clock Repetition Rate	0.01		2.0	MHz	
	Clock Pulse Width (ϕ_1 & ϕ_3)	100			ns	at −24 Volts } See
	Clock Pulse Width (ϕ_2 & ϕ_4)	200			ns	at −24 Volts } Figure 1
V_{CP}	Clock Logic Levels					
	Logic "0"	+0.3		−1.0	Volts	
	Logic "1"	−24		−27	Volts	
V_{IN}	Data and Store Input Logic Levels					
	Logic "0"	0		−2.0	Volts	
	Logic "1"	−10		−24	Volts	
	Data Input Pulse Width	100			ns	Stable During t_{mp} See Figure 1
	Store Pulse Width	200			ns	Stable During t_{sr} See Figure 1
C_C	Clock Input Capacitance					
	ϕ_1, ϕ_3		15		pF	
	ϕ_2, ϕ_4		10		pF	Plus Output Capacitive Load
C_{IN}	Data and Store Input Capacitance		2.0		pF	
I_{LCP}	Input Leakage to Ground					
	ϕ_1, ϕ_2, ϕ_3, ϕ_4			100	μA	$V_C = -27$ V
I_{LX}	Data and Store Terminals			1.0	μA	$V_{IN} = -20$ V
	Output Logic Levels					
V_{OL}	Logic "0"	0		−2.0	Volts	
V_{OH}	*Logic "1"	−11		−24	Volts	
	Power Per Bit**		0.2		mW	at 2.0 MHz
	Power Per Output Buffer		10		mW	at 2.0 MHz and 10 pF Load

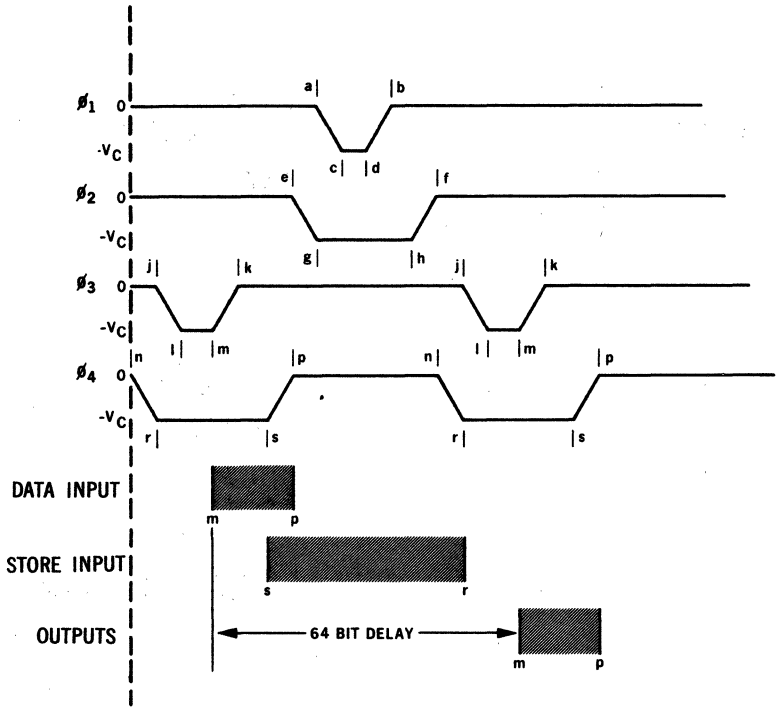
*NOTE: A resistive load to ground will have the effect of discharging the output level (Logic "1") to ground with a time constant equivalent to the RC time constant of the external load.

**NOTE: The power dissipation of each of these stages decreases proportionally with frequency.

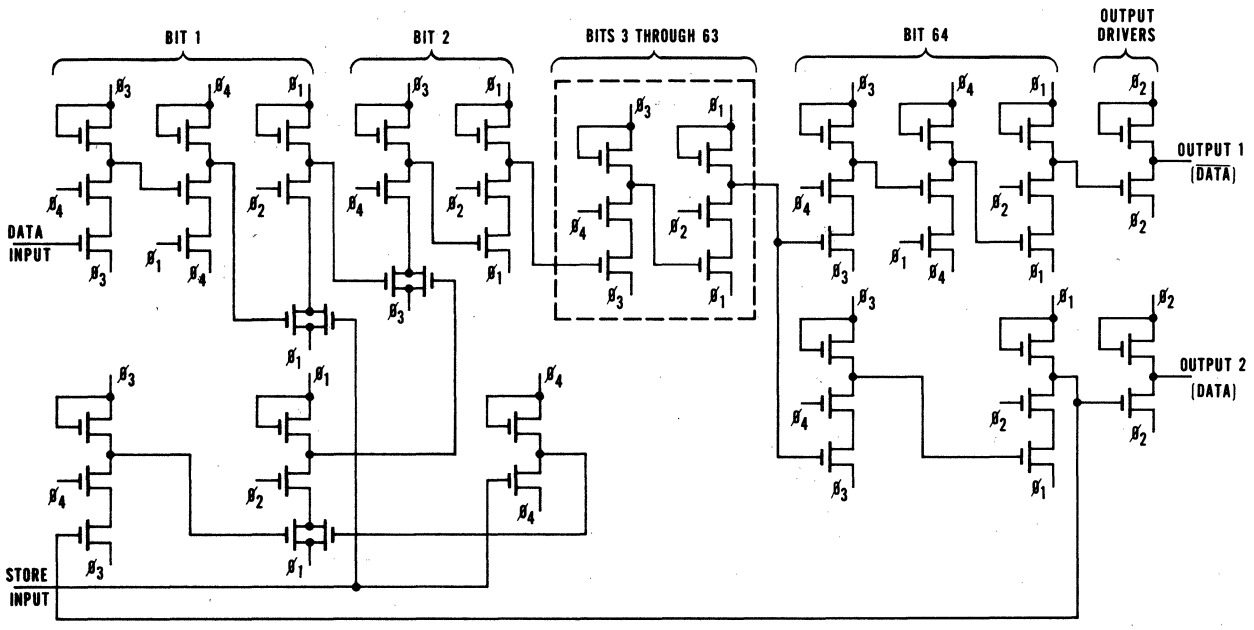
MINIMUM CLOCK REQUIREMENTS

CHARACTERISTIC	SYMBOL	MIN. VALUE (ns)	MAX. VALUE (μs)
ϕ_1 Pulse Width	t_{cd}	100	
ϕ_3 Pulse Width	t_{lm}	100	
ϕ_2 Pulse Width	t_{gh}	200	
ϕ_4 Pulse Width	t_{rs}	200	1.0
Sampling Width 1	t_{bh}	100	
Sampling Width 2	t_{ks}	100	
ϕ_4 - ϕ_1 Overlap	t_{pa}	0	
ϕ_2 - ϕ_3 Overlap	t_{fj}	0	
ϕ_2 - ϕ_4 Overlap	t_{fn}	0	1.0
ϕ_4 - ϕ_2 Overlap	t_{pe}	0	
ϕ_3 Precharge Time	t_{rm}	100	
ϕ_1 Precharge Time	t_{gd}	100	

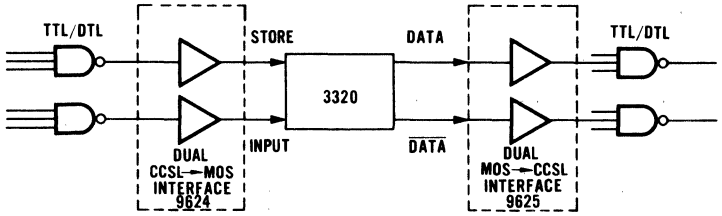
FIG. 1 — TYPICAL WAVEFORMS

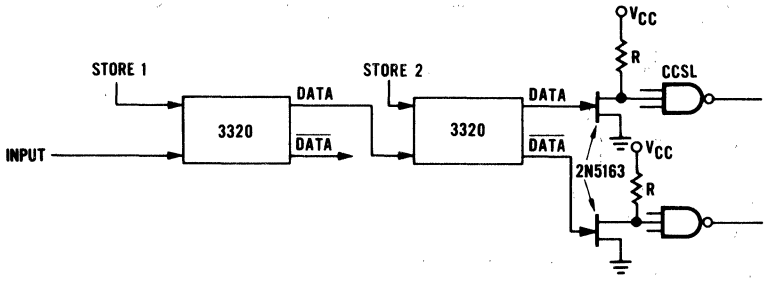


SCHEMATIC DIAGRAM



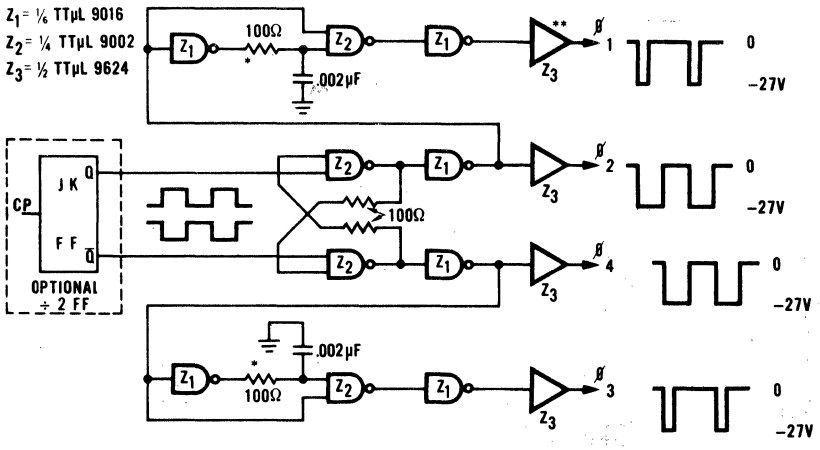
TYPICAL INTERFACE AND INTERCONNECTION DIAGRAM



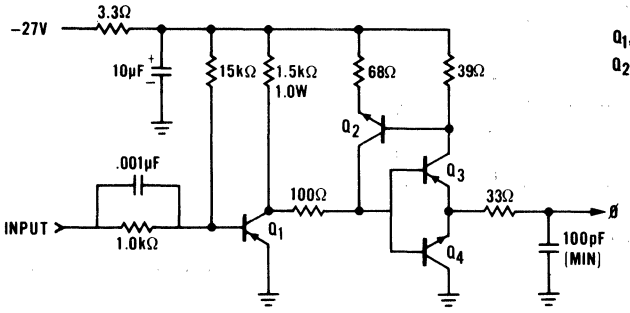


EXTERNAL R≥ 10kΩ
FOR IMPROVED NOISE MARGIN
TO CCSL.

4ø CLOCK GENERATOR



* PRECHARGE ONE SHOTS WITH R = 100 Ω & C = .002 µF FOR ~ 80 ns PRECHARGE PULSE.



**OPTIONAL BIPOLAR TO MOS INTERFACE WHERE HEAVY DRIVE CAPABILITY IS REQUIRED.

3501

1024-BIT STATIC READ-ONLY MEMORY

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3501 is a 1024-bit read-only memory in a 128 word by 8 bit format. It is a MOS monolithic integrated circuit utilizing P-channel enhancement mode technology. The fixed program memory must be specified by the customer and is customized by modifying one mask in the fabrication process. This results in a fast turn-around, low cost custom memory.

FEATURES:

- **CHIP SELECT**
- **ACCESS TIME — 2.5 μs TYP.**
- **STATIC OPERATION**
- **LOW POWER CONSUMPTION — 120 mW TYP.**
- **BIPOLAR COMPATIBLE OUTPUTS**

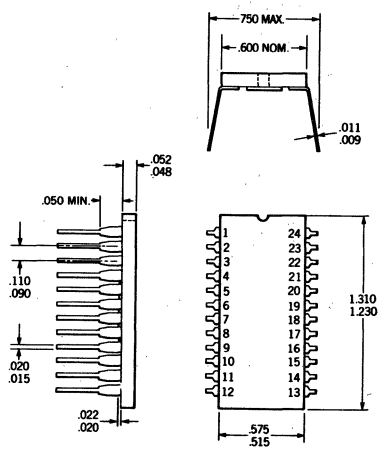
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

All Voltages and Data Input Lines	−30 V to +0.3 V
Power Dissipation	250 mW
Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +85°C
	0°C to +70°C

APPLICATIONS:

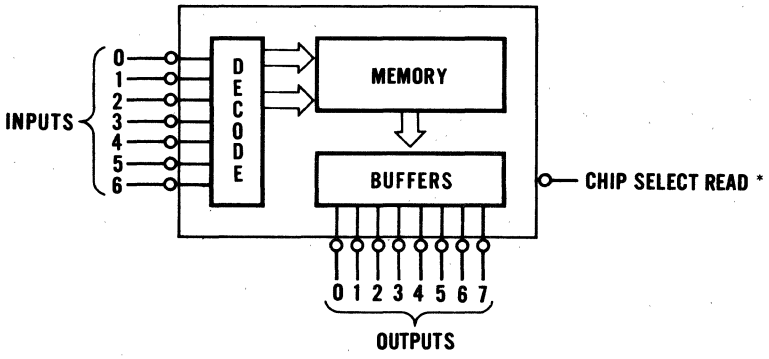
Micro Programming
Code Conversion
Table Lookup
Control Logic

PHYSICAL DIMENSION



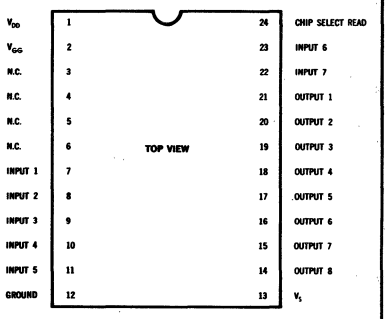
ORDER PART NO. A6G3501X4X (−55°C to +85°C)
A6G3501X9X (0°C to +70°C)

LOGIC DIAGRAM (MIL STD 806B)



*WHEN CHIP SELECT READ IS AT GROUND THE OUTPUTS ARE FLOATING.

PIN CONFIGURATION



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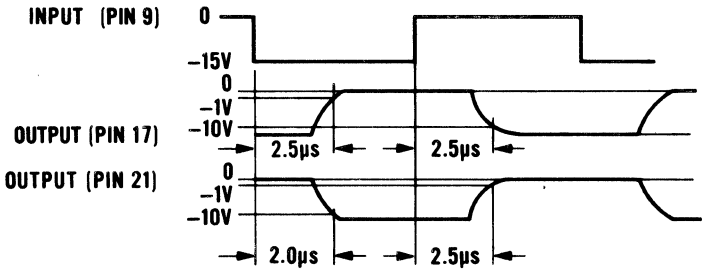
ELECTRICAL CHARACTERISTICS Standard Conditions (unless otherwise specified)
$V_{DD} = -13\ V \pm 1\ V$, $V_{GG} = -27\ V \pm 2\ V$, $V_S = -27\ V \pm 2\ V$
Load 10 MΩ, 10 pF, $T_A = 25°C$

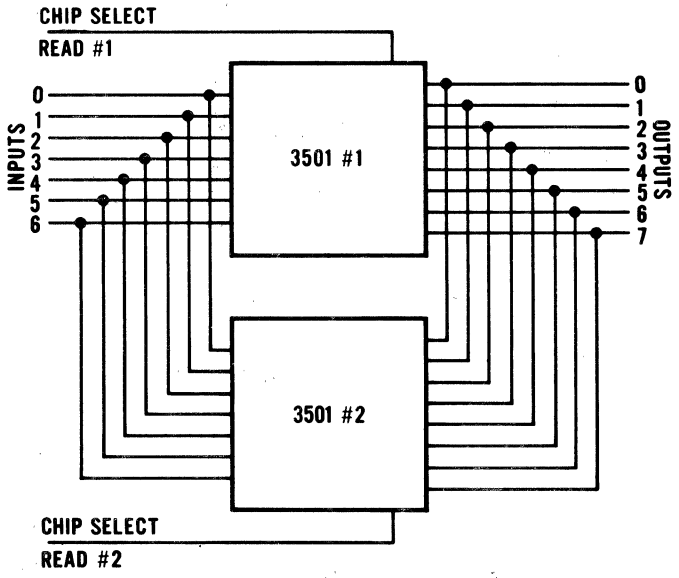
CHARACTERISTIC	MIN.	TYP	MAX.	UNITS	CONDITIONS
Input Logic Levels					
Logic 0	0		−2.0	Volts	
Logic 1	−9.0			Volts	
Output Pulse Delay		2.5	4.0	μs	
Output Logic Levels					
Logic 0	0		−1.0	Volts	
Logic 1	−10			Volts	
Logic 1	−5.0	−7.0		Volts	$R_L = 4.0\ k\Omega$, $V_S = -15\ V$
Output Capacitance		5.0		pF	
Input Capacitance		7.0		pF	
Input Leakage			5.0	μA	$V_{IN} = -20\ V$
Supply Current Drain					
I_{DD}			6.5	mA	
I_{GG}			4.0	mA	
Power Consumption		120		mW	

TIMING DIAGRAM (TYPICAL)



INPUT PINS 7, 8, 10, 11, 22, 23, GROUND
WORST CASE CONDITION INPUT 0 OUTPUT 0

TYPICAL EXPANDED MEMORY



CONNECTION FOR 256 WORDS 8 BITS

3700

MOS MONOLITHIC 4 CHANNEL SWITCH

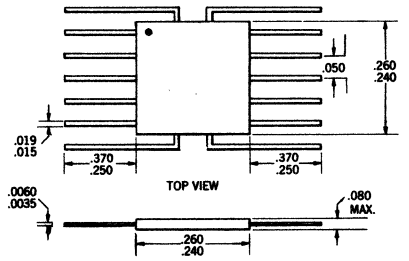
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3700 is a four-channel multiplex switch with all channel blanking. It is a monolithic integrated circuit utilizing Planar* II, P-Channel enhancement mode MOS technology. Control logic has been included on the chip to make the 3700 NPN bipolar compatible. The HLLDTμL 9112 High Level Hex Inverter can be used to directly interface the 3700 with CCSL logic levels. This device is intended for use in A/D Converters, Multiplexing, Analog or Digital Data Transmission Systems, and other airborne or ground instrumentation signal routing applications.

FEATURES:

- **BIPOLAR COMPATIBLE INPUT LOGIC LEVELS**
- **HIGH ON/OFF RATIO**
- **ALL CHANNEL BLANKING CONTROL**
- **PLANAR II STABILITY**
- **INPUT GATE PROTECTION**
- **LOW LEAKAGE CURRENT**
- **ZERO OFFSET VOLTAGE**

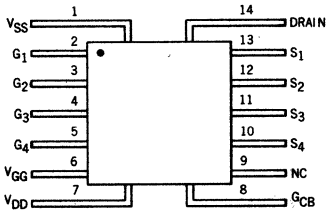
PHYSICAL DIMENSIONS



ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Storage Temperature		−65°C to +150°C
Operating Temperature	A3J370011X	−55°C to +125°C
	A3J370019X	0°C to +70°C
Positive Voltage on Any Pin		+0.3 V
Negative Voltage on Digital and Analog Input pins		
Analog Output pins		−30 V
Negative Voltage on V_{DD} and V_{GG} pins		
A3J3700112/192		−50 V
A3J3700113/193		−35 V
Total Power Dissipation in package ($T_A = 25°C$)		200 mW

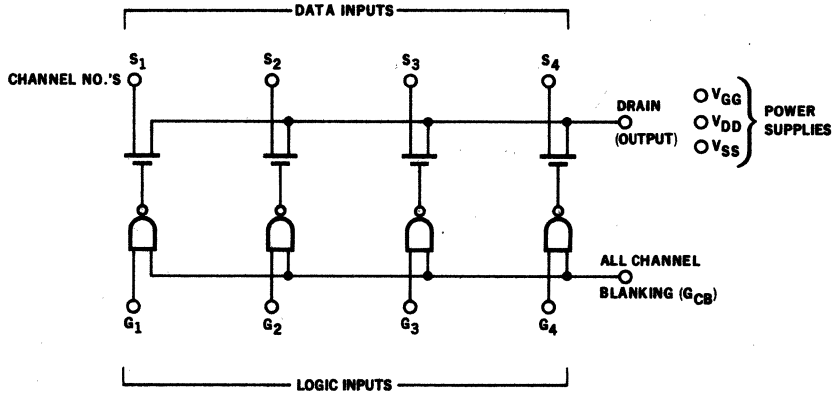
PIN CONFIGURATION IN 14 PIN CERPAK II



ORDERING INFORMATION — The 3700 is available for use in two signal ranges. (See electrical characteristics for supply voltage requirements.)

+5.0 to −5.0 volts signal applications, Order A3J3700112/192
0 to +5.0 volts signal applications, Order A3J3700113/193

LOGIC DIAGRAM



NOTES:

(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
(2) Voltage ratings are all referenced to pin 1 (V_{SS}).

*Planar is a patented Fairchild process.

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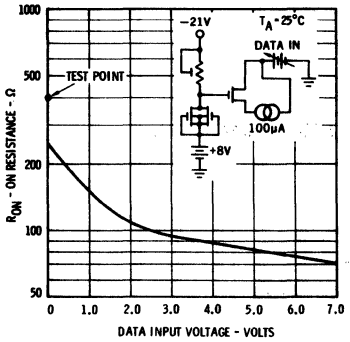
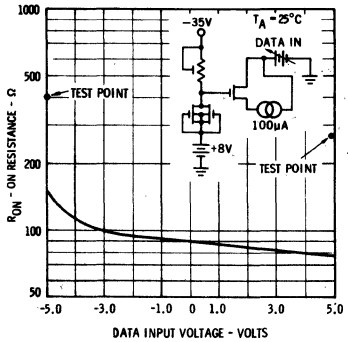
TYPICAL CHARACTERISTICS

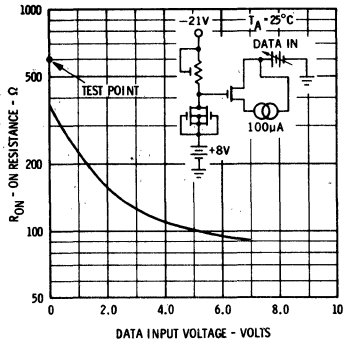
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3700 113 ONLY)



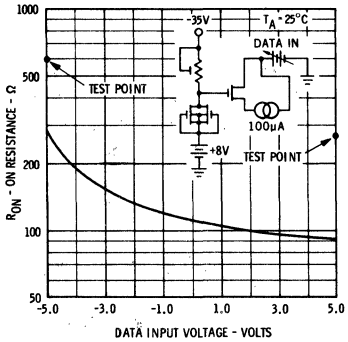
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3700 112 ONLY)



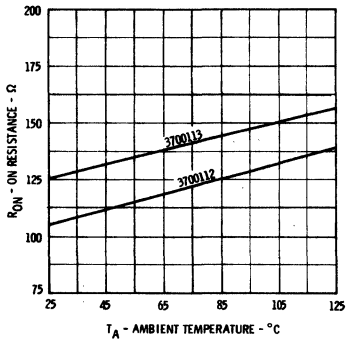
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3700 193 ONLY)



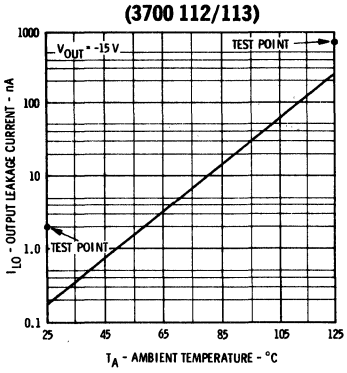
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3700 192 ONLY)



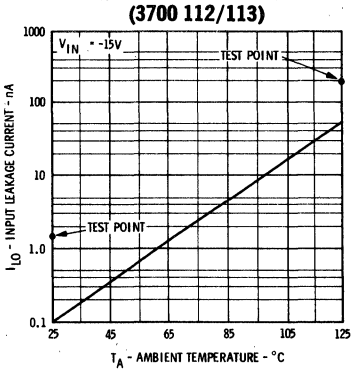
ON RESISTANCE VERSUS AMBIENT TEMPERATURE

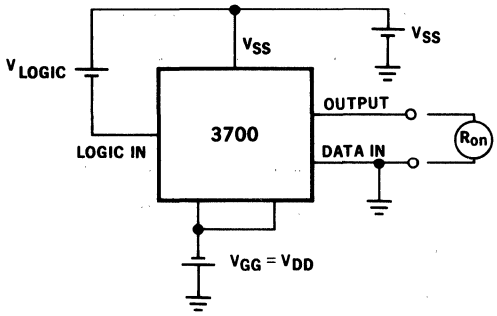


OUTPUT LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE (3700 112/113)



DATA INPUT LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE (3700 112/113)





Voltage levels between semiconductor electrodes are normally referenced to one of the electrodes. In MOS, this electrode is the Substrate (body). The voltages can be translated to an equivalent level and referenced to another electrode. In order to measure the ON resistance of the data channel accurately, the data input is at ground potential and all other terminals are changed correspondingly to test worst case conditions.

The following sets of bias conditions are equivalent

	Condition 1	Condition 2	Condition 3
Data in	+5.0 V	−3.0 V	0 V
V_{SS}	+8.0 V	0 V	+3.0 V
$V_{DD} = V_{GG}$	−21 V	−29 V	−26 V
Logic in			
1 Level	+7.0 V	−1.0 V	+2.0 V
0 Level	+1.5 V	−6.5 V	−3.5 V

The logic input levels are V_{SS} - 30 V < "0" level < V_{SS} - 7.5 V to turn a data channel off
V_{SS} - 1.5 V < "1" level < V_{SS} to turn a data channel on.

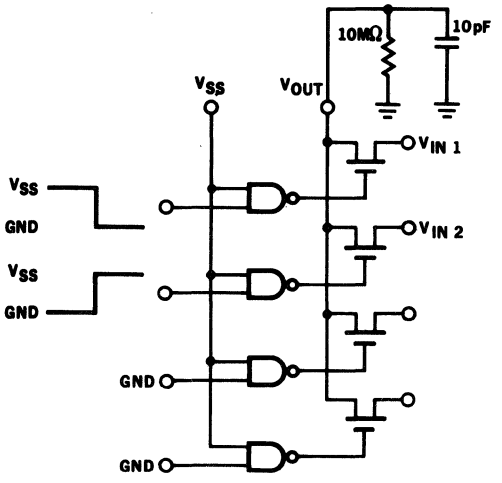
ELECTRICAL CHARACTERISTICS

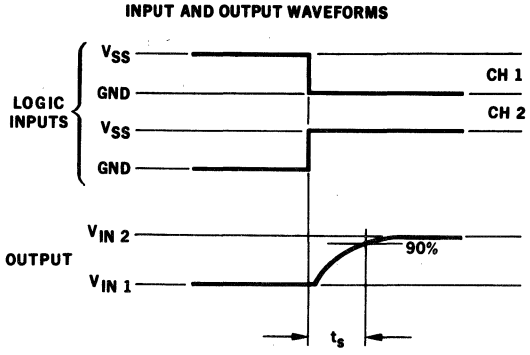
FOR 3700112/192: $-5.0\ V < V_{OUT} < +5.0\ V$, $T_A = 25°C$, $V_{DD} = V_{GG} = -35\ V \pm 10\%$, $V_{SS} = +8.0\ V \pm 10\%$ unless otherwise specified.

FOR 3700113/193: $0\ V \leq V_{OUT} \leq +5.0\ V$, $T_A = 25°C$, $V_{DD} = V_{GG} = -21\ V \pm 10\%$, $V_{SS} = +8.0\ V \pm 10\%$ unless otherwise specified.

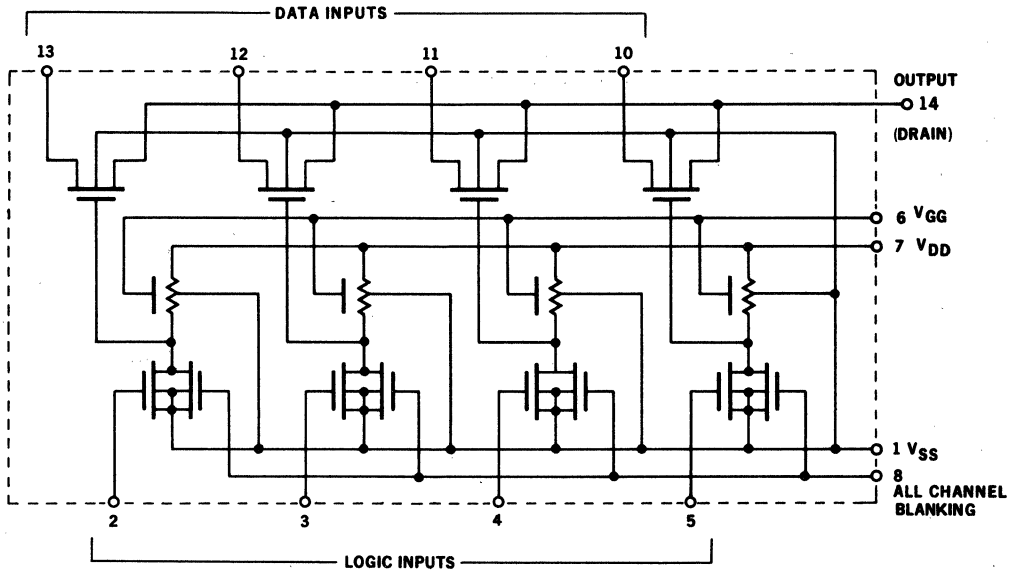
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS	
R_{ON}	Channel "ON" Resistance			270	Ω	$V_{OUT} = V_{SS}$	$I_{OUT} = -100\ \mu A$
	A3J3700112			400	Ω	$V_{OUT} = -5.0\ V$	$I_{OUT} = -100\ \mu A$
	A3J3700113			400	Ω	$V_{OUT} = 0\ V$	$I_{OUT} = -100\ \mu A$
	A3J3700192			600	Ω	$V_{OUT} = -5.0\ V$	$I_{OUT} = -100\ \mu A$
	A3J3700193			600	Ω	$V_{OUT} = 0\ V$	$I_{OUT} = -100\ \mu A$
	A3J3700112 @ +125°C			650	Ω	$V_{OUT} = -5.0\ V$	$I_{OUT} = -100\ \mu A$
	A3J3700113 @ +125°C			650	Ω	$V_{OUT} = 0\ V$	$I_{OUT} = -100\ \mu A$
R_{OFF}	Channel "OFF" Resistance	1.5			GΩ	$V_{SS} - V_{OUT} = 15\ V$	$V_G = Gnd$
	A3J3700112/113 @ +125°C	2.1			MΩ	$V_{SS} - V_{OUT} = 15\ V$	$V_G = Gnd$
I_{LO}	Output Leakage Current						
	A3J3700112/113			2.0	nA	$V_{SS} - V_{OUT} = +15\ V$	$V_G = Gnd$
	A3J3700192/193			10	nA	$V_{SS} - V_{OUT} = +15\ V$	$V_G = Gnd$
	A3J3700112/113 @ +125°C			700	nA	$V_{SS} - V_{OUT} = +15\ V$	$V_G = Gnd$
I_{LI}	Data Input Leakage Current			1.5	nA	$V_{SS} - V_{IN} = 15\ V$	$V_G = Gnd$
	A3J3700112/113 @ +125°C			200	nA	$V_{SS} - V_{IN} = 15\ V$	$V_G = Gnd$
V_{IH}	Logic Gate Input "1" Level	$V_{SS} - 1.5$		V_{SS}	V		
V_{IL}	Logic Gate Input "0" Level	$V_{SS} - 7.5$		$V_{SS} - 30$	V		
t_s	Channel Switching Time (see Fig. 1)		1.0		μs		
C_{db}	Output Capacitance		25		pF	$V_{SS} - V_{OUT} = 0\ V$	f = 1.0 MHz
C_{is}	Data Input Capacitance		9.0		pF	$V_{SS} - V_{IN} = 0\ V$	f = 1.0 MHz
C_{ig}	Logic Input Capacitance		3.5		pF	$V_{SS} - V_G = 0\ V$	f = 1.0 MHz
C_{it}	Channel Blanking Input Capacitance		10		pF	$V_{SS} - V_G = 0\ V$	f = 1.0 MHz

FIG. 1
SWITCHING TIME TEST CIRCUIT



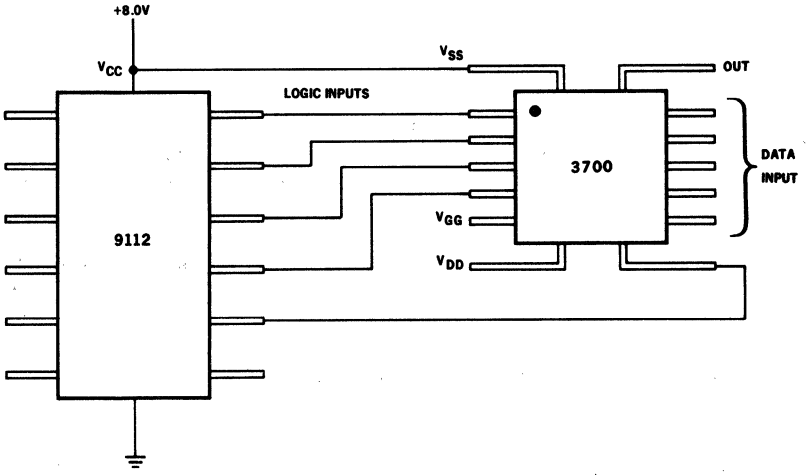


SCHEMATIC DIAGRAM



TYPICAL CIRCUIT CONFIGURATION

Typical circuit configuration showing the 3700 driven by bipolar Diode-Transistor Logic such as the Fairchild HLLDTμL 9112.



3701

MOS MONOLITHIC 6-CHANNEL SWITCH

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3701 is a P-channel enhancement mode Monolithic MOS six-channel, single output switch. This device can be used as a basic switching element for airborne or ground instrumentation, telemetry or other signal routing applications.

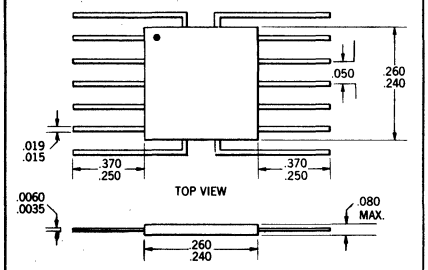
FEATURES

- **GATE PROTECTION**
- **ZERO OFFSET VOLTAGE**
- **LOW LEAKAGE CURRENT**
- **GUARANTEED OPERATIONS OVER −55°C TO +125°C**
- **PLANAR* II STABILITY**

ABSOLUTE MAXIMUM RATINGS (Note 1)

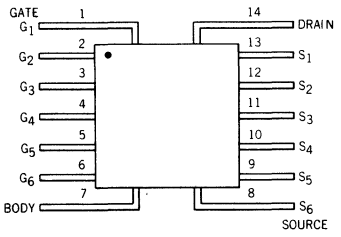
Storage Temperature		−65°C to +150°C
Operating Temperature	A3J370111X	−55°C to +125°C
	A3J370119X	0°C to +70°C
Power Dissipation at +25°C		200 mW
Positive Voltage on any pin ($V_{BODY} = 0$)		+0.3 Volt
Negative Gate Voltage ($V_{BODY} = 0$)		−35 Volts
Negative Source or Drain Voltage ($V_{BODY} = 0$)		−30 Volts

PHYSICAL DIMENSIONS



ORDER PART NO. A3J370111X/19X

PIN CONFIGURATION IN 14 PIN CERPAK II



ELECTRICAL CHARACTERISTICS ($V_{BODY} = 0$ Volt, $T_A = 25°C$ unless otherwise specified)

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
R_{ON}	Channel "ON" Resistance					
	A3J370111X		210	375	Ω	$V_S = 0$ V, $V_G = -30$ V, $I_D = -100$ μA
	A3J370111X (125°C)		310	550	Ω	$V_S = 0$ V, $V_G = -30$ V, $I_D = -100$ μA
	A3J370119X		300	500	Ω	$V_S = 0$ V, $V_G = -30$ V, $I_D = -100$ μA
R_{OFF}	Channel "OFF" Resistance					
	A3J370111X	10	200		GΩ	$V_D = -20$ V, $V_G = 0$, $V_S = 0$ V
	A3J370111X (125°C)	100	250		MΩ	$V_D = -20$ V, $V_G = 0$, $V_S = 0$ V
	A3J370119X	4.0	200		GΩ	$V_D = -20$ V, $V_G = 0$, $V_S = 0$ V
$V_{GS(TH)}$	Gate Threshold Voltage			−5.5	Volts	$V_S = 0$ V, $V_G = V_D$, $I_D = -10$ μA
I_{SL}	Input Leakage					
	A3J370111X			1.0	nA	$V_S = -20$ V, $V_D = 0$ V, $V_G = 0$ V
	A3J370111X (125°C)			150	nA	$V_S = -20$ V, $V_D = 0$ V, $V_G = 0$ V
	A3J370119X			1.0	nA	$V_S = -20$ V, $V_D = 0$ V, $V_G = 0$ V

*Planar is a patented Fairchild process.

NOTE:
(1) These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.

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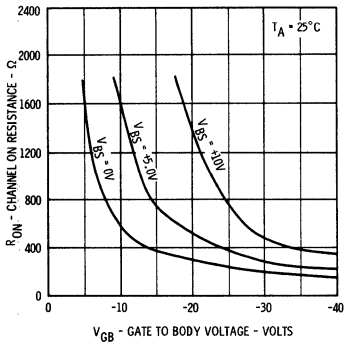
FAIRCHILD MOS INTEGRATED CIRCUIT 3701

ELECTRICAL CHARACTERISTICS (V_{BODY} = 0 Volt, T_A = 25°C unless otherwise specified)

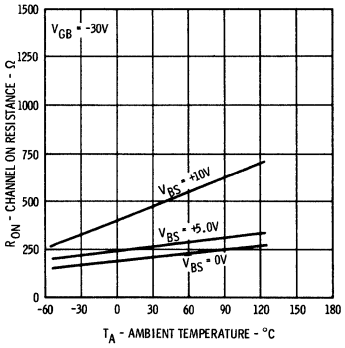
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
I_{DL}	Output Leakage					
	A3J370111X			2.0	nA	$V_D = -20$ V, $V_S = V_G = 0$ V
	A3J370111X (125°C)			200	nA	$V_D = -20$ V, $V_S = V_G = 0$ V
	A3J370119X			5.0	nA	$V_D = -20$ V, $V_S = V_G = 0$ V
I_{GL}	Gate Leakage			1.0	nA	$V_G = -20$ V, $V_D = V_S = 0$ V
C_S	Input Capacitance		4.0		pF	$V_S = 0$ V, $V_D = 0$ V, $V_G = 0$ V
C_S	Input Capacitance		3.0		pF	$V_S = -10$ V, $V_D = 0$ V, $V_G = 0$ V
C_D	Output Capacitance		13		pF	$V_S = 0$ V, $V_D = 0$ V, $V_G = 0$ V
C_D	Output Capacitance		7.0		pF	$V_S = 0$ V, $V_D = -10$ V, $V_G = 0$ V
C_G	Gate Capacitance		4.0		pF	$V_S = 0$ V, $V_D = 0$ V, $V_G = 0$ V
C_{GS} or C_{GD}	Gate-Source or Gate-Drain Capacitance		1.0		pF	$V_S = 0$ V, $V_D = 0$ V, $V_G = 0$ V

A3J370111X

TYPICAL CHANNEL ON RESISTANCE VERSUS GATE TO BODY VOLTAGE WITH BODY TO SOURCE VOLTAGE AS PARAMETER

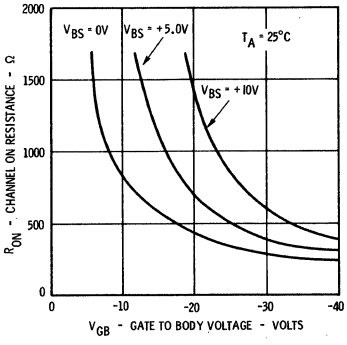


TYPICAL CHANNEL ON RESISTANCE VERSUS AMBIENT TEMPERATURE WITH BODY TO SOURCE VOLTAGE AS PARAMETER

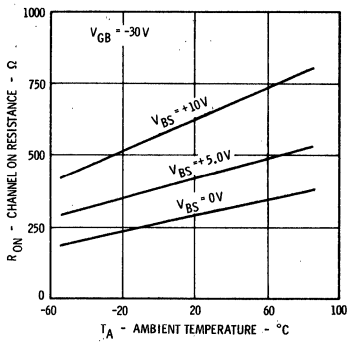


A3J370119X

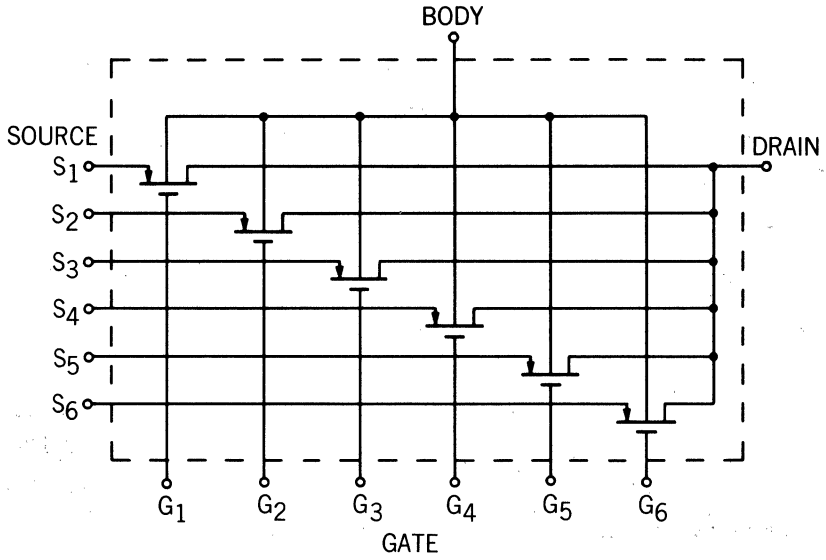
TYPICAL CHANNEL ON RESISTANCE VERSUS GATE TO BODY VOLTAGE WITH BODY TO SOURCE VOLTAGE AS PARAMETER



TYPICAL CHANNEL ON RESISTANCE VERSUS AMBIENT TEMPERATURE WITH BODY TO SOURCE VOLTAGE AS PARAMETER



SCHEMATIC DIAGRAM



3705

MOS MONOLITHIC 8 CHANNEL MULTIPLEX SWITCH

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3705 is an eight-channel multiplex switch with output enable control and one-out-of-eight decoder included on the chip. It is a monolithic integrated circuit utilizing Planar* II, P-channel enhancement Mode MOS technology. The logic input lines of the 3705 are NPN bipolar compatible and can be used directly with CCSL 5.0 volt logic levels with no level-shifting interface required. This device is intended for use in A/D converters, multiplexing in analog or digital data transmission systems, and other airborne or ground instrumentation signal routing applications.

FEATURES

- **CCSL COMPATIBLE INPUT LOGIC LEVELS**
- **ONE-OUT-OF-EIGHT DECODER ON THE CHIP**
- **HIGH ON/OFF RATIO**
- **OUTPUT ENABLE CONTROL**
- **PLANAR II STABILITY**
- **INPUT GATE PROTECTION**
- **LOW LEAKAGE CURRENT**
- **ZERO OFFSET VOLTAGE**

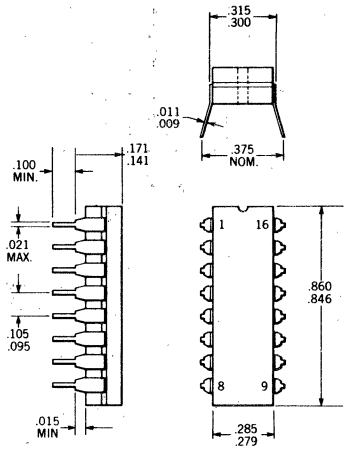
ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Positive Voltage on any pin	+0.3 V
Negative Voltage on digital and analog input pins	−35 V
Negative Voltage on digital and analog output pins	−35 V
Negative Voltage on V_{DD} pin	−35 V
Total power dissipation in package ($T_A = 25°C$)	200 mW

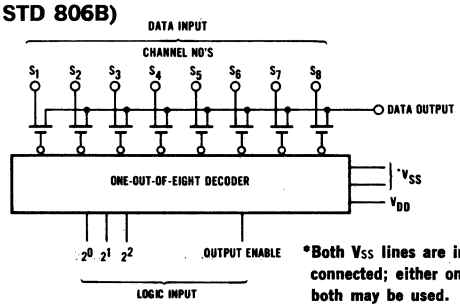
ORDERING INFORMATION — The 3705 is available for use in two signal ranges

−5.0 to +5.0 volts signal applications, Order A6J3705142
0 to +5.0 volts signal applications, Order A6J3705143

PHYSICAL DIMENSIONS
16 Lead Dual In-Line



SYMBOLIC DIAGRAM
(MIL STD 806B)

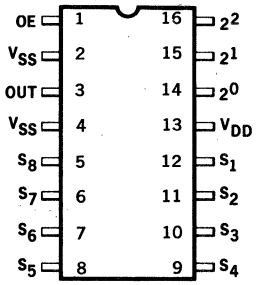


*Both V_{SS} lines are internally connected; either one or both may be used.

TRUTH TABLE

LOGIC INPUTS				CHANNEL
2^0	2^1	2^2	OE	'ON'
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

PIN CONFIGURATION
(16 lead DIP)



TOP VIEW

NOTES:

(1) These ratings are limiting values above which the serviceability of the device may be impaired.
(2) Voltage ratings are all referenced to pins 2 and 4 (V_{SS}).

*Planar is a patented Fairchild process.

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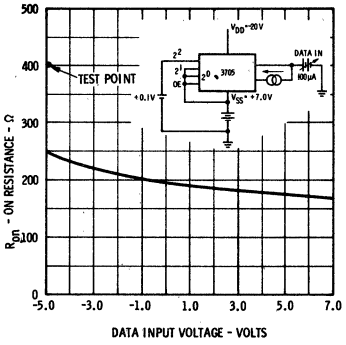
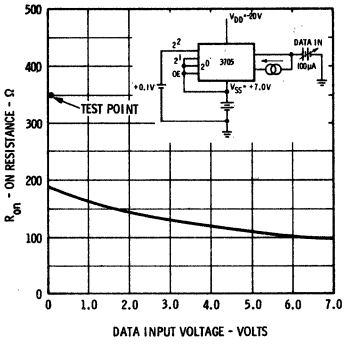
TYPICAL DEVICE CHARACTERISTICS

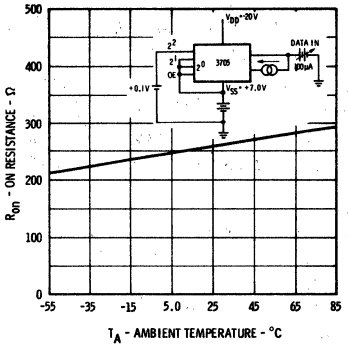
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3705 142 ONLY)



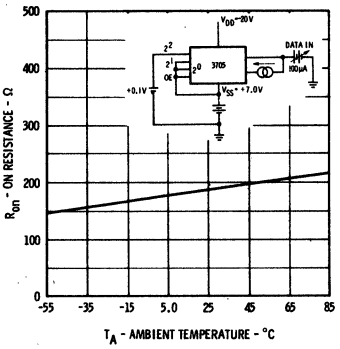
ON RESISTANCE VERSUS DATA INPUT VOLTAGE (3705 143 ONLY)



ON RESISTANCE VERSUS AMBIENT TEMPERATURE (3705 142 ONLY)



ON RESISTANCE VERSUS AMBIENT TEMPERATURE (3705 143 ONLY)



OUTPUT LEAKAGE CURRENT VERSUS AMBIENT TEMPERATURE

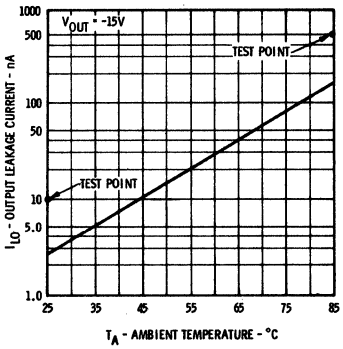
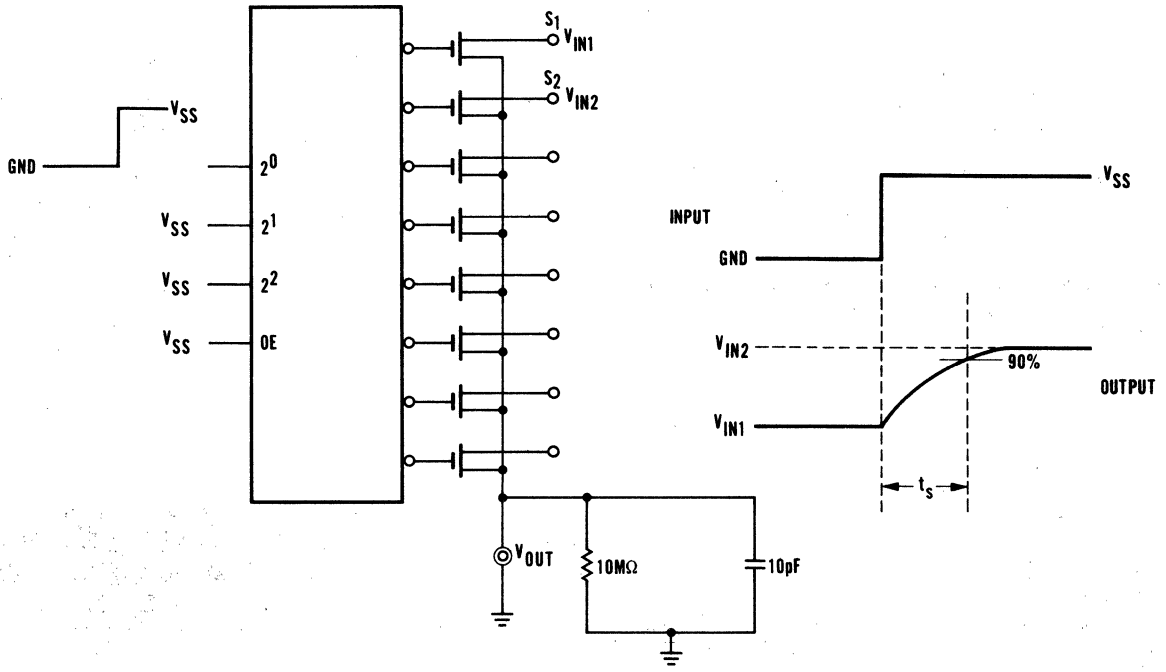


FIG. 1

SWITCHING TIME TEST CIRCUIT



ELECTRICAL CHARACTERISTICS

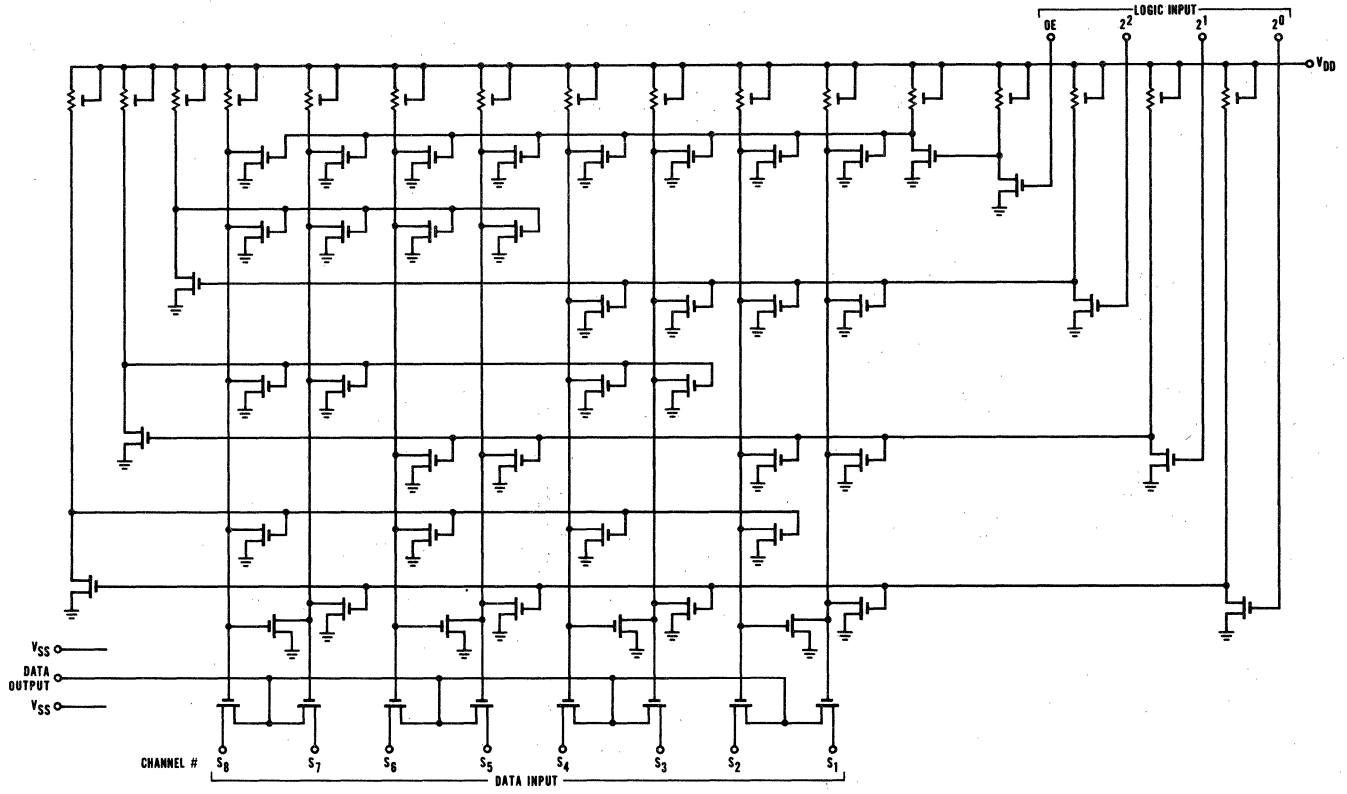
For 3705142: $-5.0\ V < V_{OUT} < +5.0\ V$, $T_A = 25°C$, $-20\ V < V_{DD} < -24\ V$, $5.0\ V < V_{SS} < 7.0\ V$ unless otherwise specified

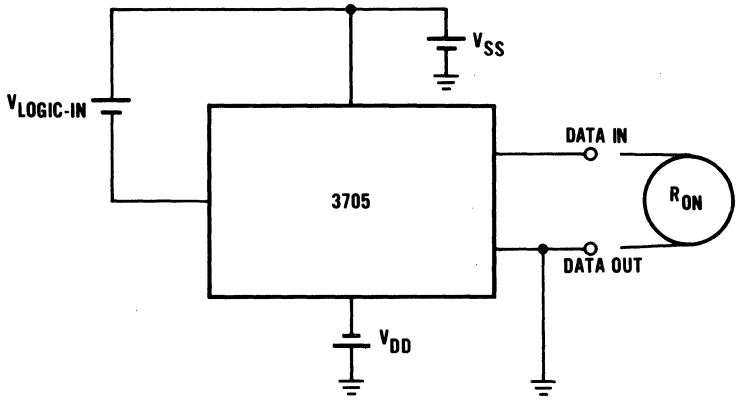
For 3705143: $0\ V < V_{OUT} < +5.0\ V$, $T_A = 25°C$, $-20\ V < V_{DD} < -24\ V$, $5.0\ V < V_{SS} < 7.0\ V$ unless otherwise specified

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
R_{ON}	Data Channel "ON" Resistance					
	142		250	400	Ω	$V_{OUT} = -5.0\ V$, $I_{OUT} = -100\ \mu A$
	143		190	350	Ω	$V_{OUT} = 0\ V$, $I_{OUT} = -100\ \mu A$
R_{OFF}	Data Channel "OFF" Resistance	1.5			GΩ	$V_{SS} - V_{OUT} = 15\ V$
I_{LO}	Output Leakage Current			10	nA	$V_{SS} - V_{OUT} = 15\ V$
$I_{LO}(85°C)$	Output Leakage Current			500	nA	$V_{SS} - V_{OUT} = 15\ V$
I_{LDI}	Data Input Leakage Current					
	142			3.0	nA	$V_{SS} - V_{IN} = 15\ V$
	143			2.0	nA	$V_{SS} - V_{IN} = 10\ V$
I_{LI}	Logic Input Leakage Current			1.0	μA	$V_{SS} - V_{LOGIC\text{-}IN} = 15\ V$
*V_{IL}	Logic Gate Input "Low" Level	V_{DD}		+0.2	V	
*V_{IH}	Logic Gate Input "High" Level	$V_{SS} - 1.5$		V_{SS}	V	
t_S	Channel Switching Time (See Fig. 1)		1.0		μS	
C_{db}	Output Capacitance		40		pF	$V_{SS} - V_{OUT} = 0\ V$, $f = 1.0\ MHz$
C_{is}	Data Input Capacitance		7.5		pF	$V_{SS} - V_{IN} = 0\ V$, $f = 1.0\ MHz$
C_{ig}	Logic Input Capacitance		5.5		pF	$V_{SS} - V_{LOGIC\text{-}IN} = 0\ V$, $f = 1.0\ MHz$
P_D	Power Dissipation		130	175	mW	$V_{DD} = -31\ V$, $V_{SS} = 0\ V$

*When driven by CCSL elements, avoid excessive D.C. loading of CCSL elements to insure 3705 logic levels under maximum fan-out conditions.

SCHEMATIC DIAGRAM



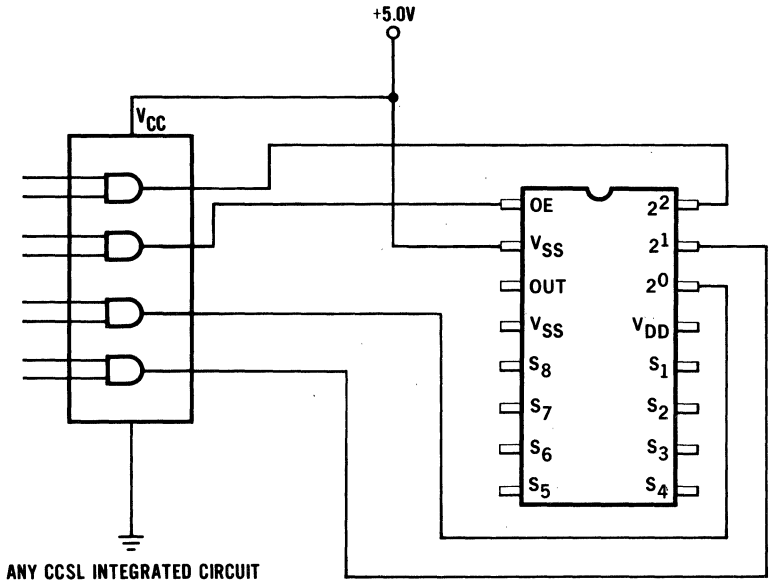


Voltage levels between semiconductor electrodes are normally referenced to one of the electrodes. In MOS, this electrode is the substrate (body or V_{SS}). The voltages can be translated to an equivalent level and referenced to another electrode. In order to measure the 'ON' resistance of the data channel accurately, the data output is at ground potential and all other terminals are changed correspondingly to test worst case conditions.

The following sets of bias conditions are equivalent:

	CONDITION 1	CONDITION 2
DATA IN	+5.0 V	0 V
V_{SS}	+7.0 V	+2.0 V
V_{DD}	−20 V	−25 V
LOGIC IN		
"Low" Level	+0.2 V	−4.8 V
"High" Level	+5.5 V	+0.5 V

TYPICAL CONTROL CIRCUIT



3750
10-BIT D/A CONVERTER
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3750 is a monolithic MOS/LSI ten bit digital to analog converter using P-channel enhancement mode MOS technology. The digital word can be entered serially or in parallel. If desired, the word is available in serial form through an output buffer in either an 8 or 10 bit format. The converter output data is available thru 10 single pole double throw (SPDT) MOS switches. The holding register retains the state of the previous digital input word and drives the output switches. Transfer gates are used to isolate the holding register from the input register while new data is being entered. The 'on' resistance of the MOS switches is weighted to provide the necessary accuracy and stability for a ten bit conversion.

FEATURES

- **8 AND 10 BIT DATA LENGTHS**
- **SERIAL AND PARALLEL OPERATION**
- **250 kHz SERIAL BIT RATE**
- **500 kHz PARALLEL WORD RATE**
- **250 Ω TYPICAL 'ON' RESISTANCE OF TWO MSB's**
- **500 Ω TYPICAL 'ON' RESISTANCE OF REMAINING EIGHT BITS**
- **110 mW POWER DISSIPATION**
- **ZERO AND FULL SCALE CALIBRATION LOGIC**

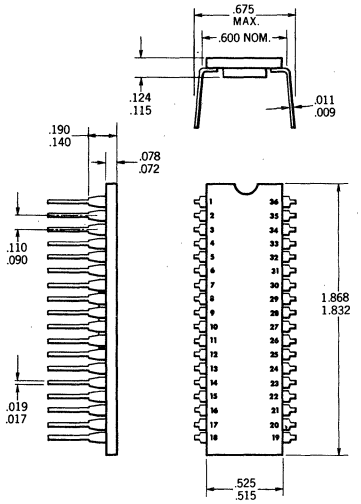
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Input Voltages	−30 to +0.3 Volts
Power Supply	−29 Volts
Storage Temperature	−55°C to +150°C
Operation Temperature	−55°C to +85°C

APPLICATIONS

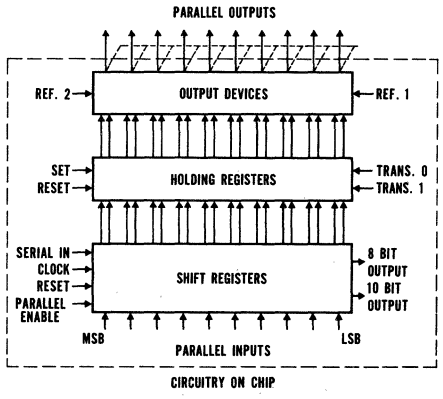
D/A Converters
- Telemetry
- Analog data plotters
- Industrial process control
- Servo systems

PHYSICAL DIMENSION
36 PIN
DUAL IN-LINE PACKAGE

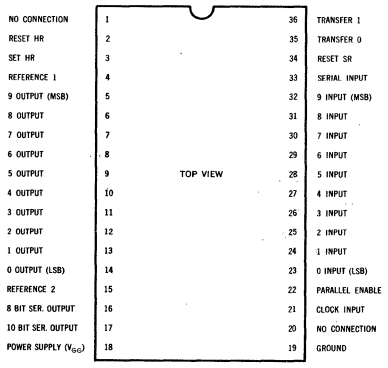


ORDER PART NO. A6H375014X

BLOCK DIAGRAM



PIN CONFIGURATION



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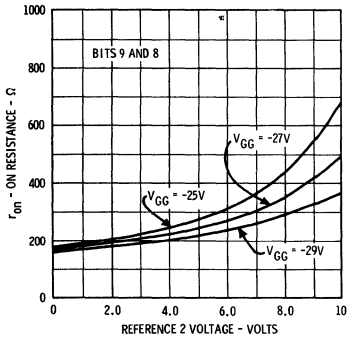
ELECTRICAL CHARACTERISTICS $V_{GG} = -27 \pm 2.0$ Volts, $R_L = 10\ M\Omega$, $C_L = 10$ pF (unless otherwise specified)

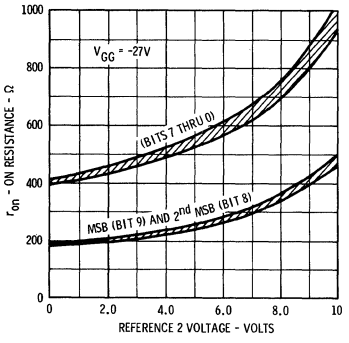
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Logic Inputs					
	"0"	0		−2.0	Volts	
	"1"	−9.0		−30	Volts	
	Logic Outputs					
	"0"	0		−1.0	Volts	
	"1"	−10		−30	Volts	
	Clock					
	Amplitude	−9.0		−30	Volts	
	Width	1.0		10	μs	
f_{max}	Frequency					
	Serial	DC		250	kHz	
	Parallel	DC		500	kHz	
r_{on}	MOS Switches					
	"9"	150	250	500	ohms	$V_{REF} = -5.0$ V
	"8"	150	250	500	ohms	$V_{GG} = -27$ V
	"7" thru "0"	325	550	1000	ohms	
Δr_{on}	Switch Mismatch					
	"9"		70	150	ohms	$V_{REF_2} = -5.0$ V
	"8"		70	150	ohms	$V_{REF_1} = 0$ V
	"7" thru "0"		120	250	ohms	
t_{df}	Serial Delay,		0.6		μs	
t_f	rise and fall		0.2		μs	
t_{dr}	times		0.5		μs	
t_r			0.5		μs	
t_{df}	Parallel Delay,		0.55		μs	
t_f	rise and fall		0.35		μs	
t_{dr}	times		0.4		μs	
t_r			0.3		μs	
C_{in}	Data and Control Input Capacitance		7.0		pF	
I_{max}	Power Supply Current Drain		4.5	7.0	mA	$V_{GG} = -27$ V
P_{max}	Power Dissipation		120	190	mW	$V_{GG} = -27$ V
	Temperature Coefficient of Switches		0.3		%/°C	
	Temperature Coefficient Tracking		0.03		%/°C	
I_{LX}	Input Leakage Current			5.0	μA	$V_{in} = -20$ V
t_{dd}	Data Delay Time	250			ns	

TYPICAL ELECTRICAL CHARACTERISTICS

ON RESISTANCE VERSUS POWER SUPPLY VOLTAGE (V_{GG}) OUTPUT VOLTAGE (REF. 2)

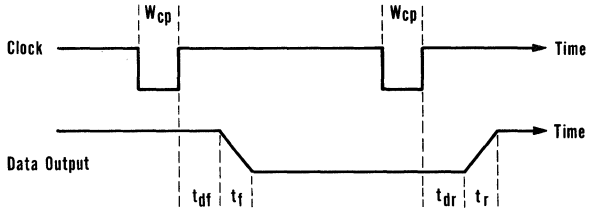


ON RESISTANCE VERSUS OUTPUT VOLTAGE (REF. 2)

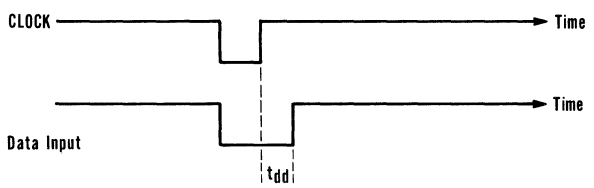


TIMING DIAGRAM

OUTPUT DELAY, RISE AND FALL TIMES

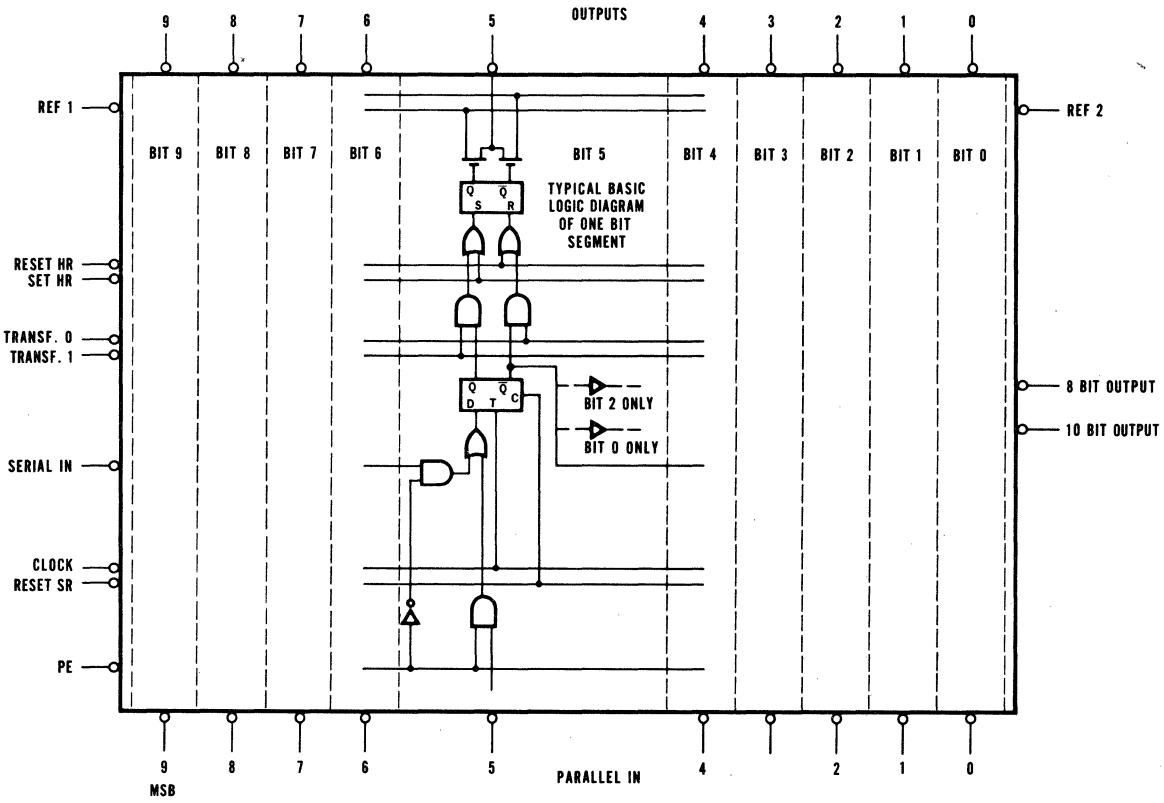


DATA BIT TIMING

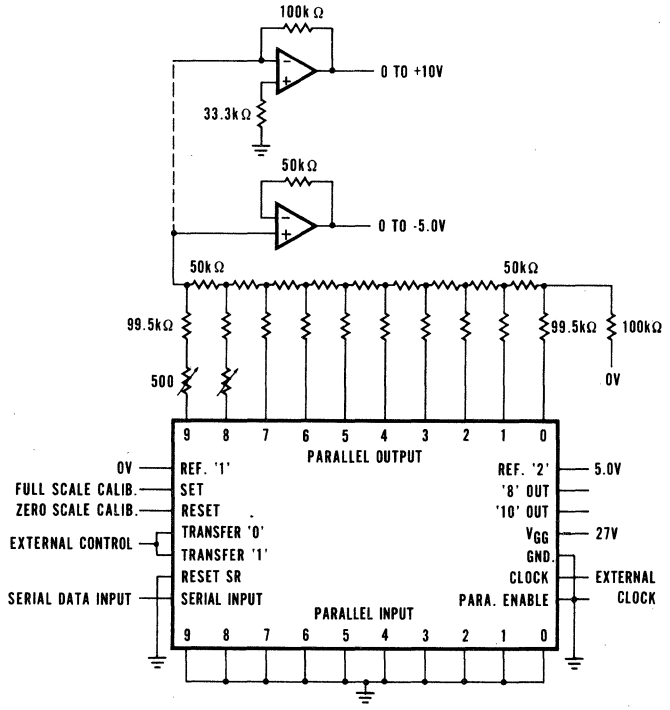


TIMING DIAGRAMS

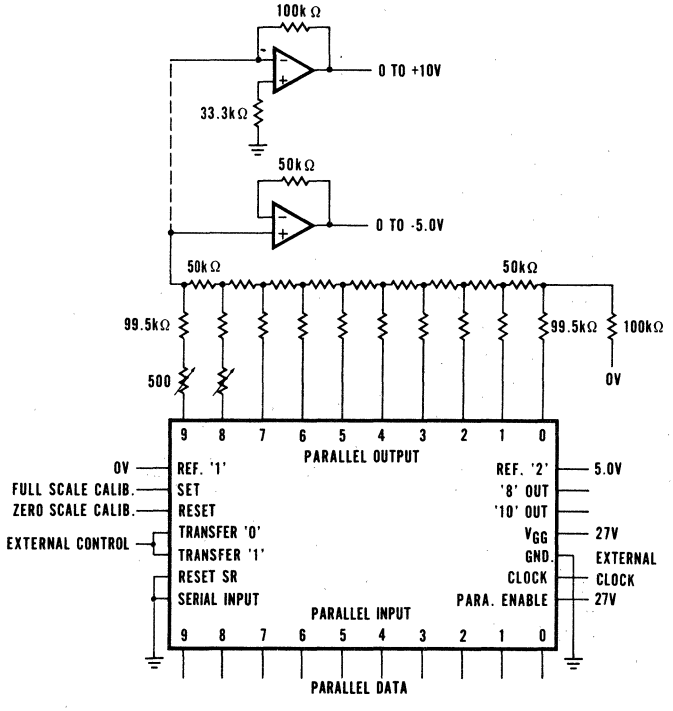
LOGIC DIAGRAM

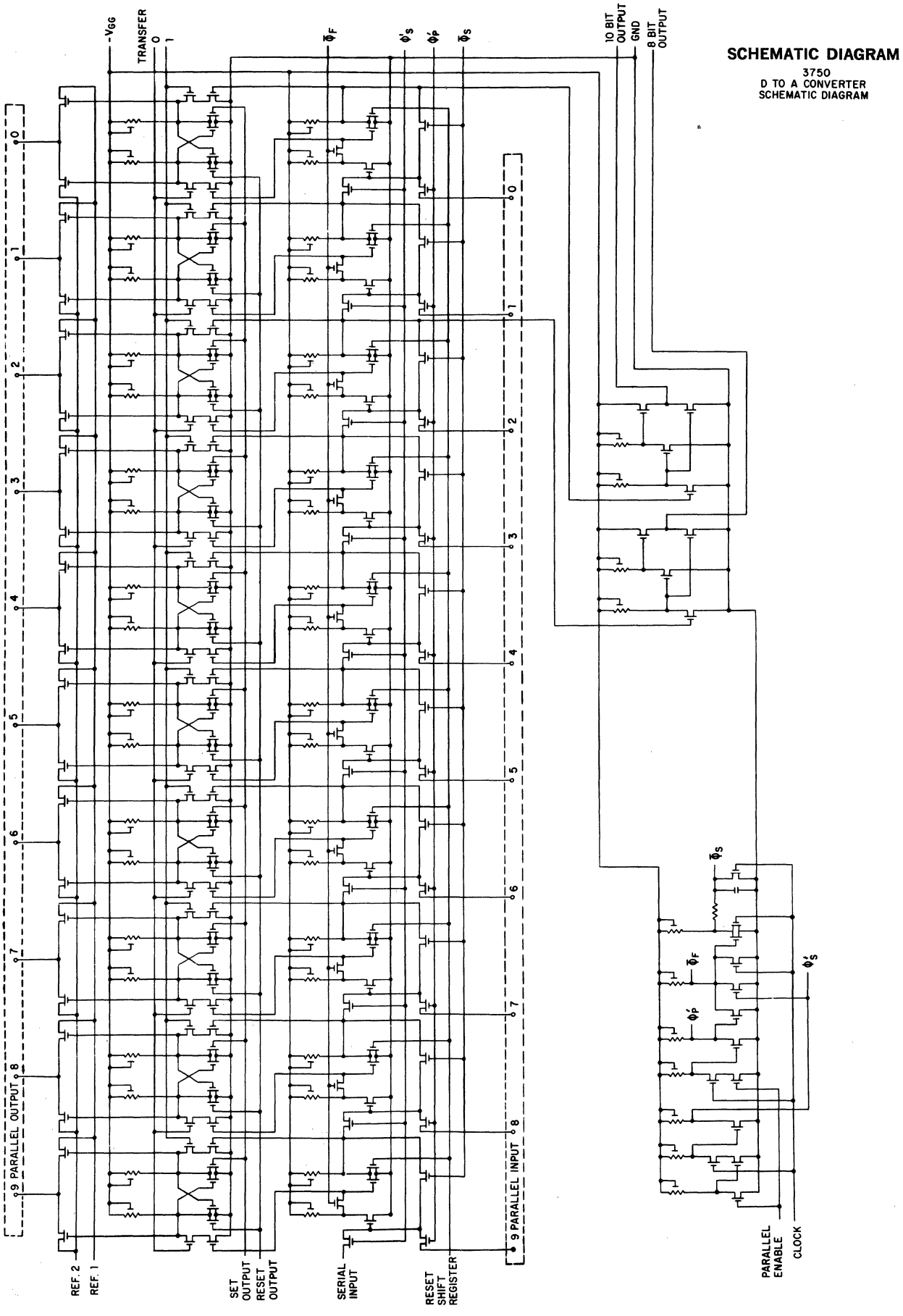


SERIAL OPERATION



PARALLEL OPERATION




SCHEMATIC DIAGRAM
3750
D TO A CONVERTER
SCHEMATIC DIAGRAM
-VGG
TRANSFER
0
1
10 BIT OUTPUT
GND
8 BIT OUTPUT
9 PARALLEL OUTPUT
9 PARALLEL INPUT
REF. 2
REF. 1
SET OUTPUT
RESET OUTPUT
SERIAL INPUT
RESET SHIFT REGISTER
PARALLEL ENABLE
CLOCK

3751
12-BIT A/D CONVERTER
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3751 is a twelve bit analog to digital converter using P channel enhancement mode MOS/LSI technology. The conversion is accomplished by the successive approximation technique. The word length is variable for eight, nine, ten or twelve bits by applying a DC potential to each of two control pins. The 3751 provides all the A/D system control functions such as: master timing, automatic start and recycle, and RZ or NRZ format control. By choosing the appropriate ladder network, the output will be in either a binary or binary coded decimal digital format.

FEATURES

- **8, 9, 10, OR 12 BIT WORD LENGTH**
- **RZ OR NRZ DIGITAL FORMAT**
- **COMPLETE LOGIC AND SYSTEM TIMING CIRCUITS INCLUDED ON THE CHIP**
- **BCD OVERVOLTAGE FLAG**
- **200 Ω TYPICAL "ON" RESISTANCE FOR THE TWO MSB**
- **500 Ω TYPICAL "ON" RESISTANCE FOR THE REMAINING TEN SWITCHES**
- **150 mW POWER DISSIPATION**
- **AUTOMATIC RESTART CIRCUITS**

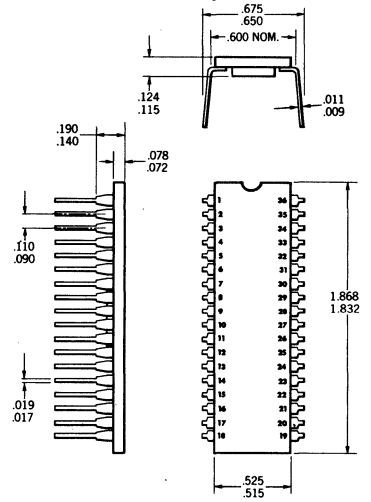
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Input Voltages	−30 to +0.3 Volts
Power Supply	−30 Volts
Storage Temperature	−55°C to +150°C
Operation Temperature	−55°C to +85°C

APPLICATIONS

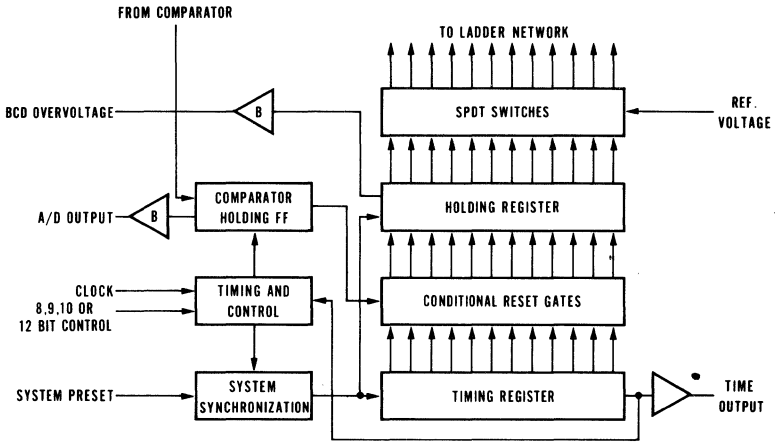
A/D Converters
Three Digit DVM's
Telemetry
Industrial Control
Computer Interface

PHYSICAL DIMENSIONS
36 PIN
DUAL IN-LINE PACKAGE

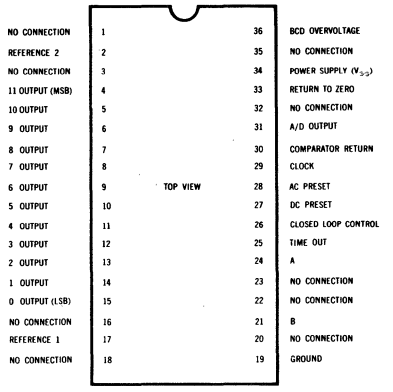


ORDER PART NO. A6H375114X

BLOCK DIAGRAM



PIN CONFIGURATION



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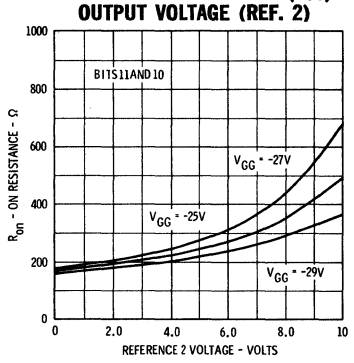
ELECTRICAL CHARACTERISTICS ($V_{GG} = -27 \pm 2.0$ Volts, $R_L = 10\ M\Omega$, $C_L = 10$ pF unless otherwise specified)

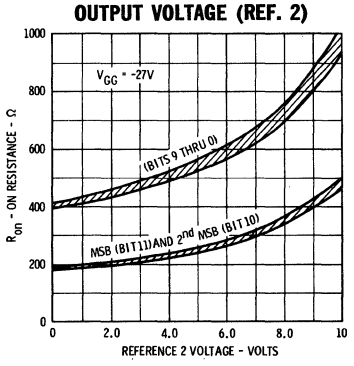
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Logic Inputs					
	"0"	0		−2.0	Volts	
	"1"	−9.0		−30	Volts	
	Logic Outputs					
	"0"	0		−1.0	Volts	
	"1"	−10		−30	Volts	
W_{cp}	Clock					
	Amplitude	−9.0		−30	Volts	
	Width	1.0		10	μs	
f_{max}	Bit Frequency	DC		250	kHz	
R_{ON}	MOS Switches					
	"11"	150	250	500	Ω	
	"10"	150	250	500	Ω	
	"9" thru "0"	325	550	1000	Ω	
ΔR_{ON}	Switch Mismatch					
	"11"		70	150	Ω	
	"10"		70	150	Ω	
	"9" thru "0"		120	250	Ω	
C_{IN}	Data and Control Input Capacitance		7.0		pF	
I_{max}	Power Supply Current Drain		4.5	7.0	mA	$V_{GG} = -27$ V
P_{max}	Power Dissipation		120	190	mW	$V_{GG} = -27$ V
	Temperature Coefficient of Switches		0.3		%/°C	
	Temperature Coefficient of Tracking		0.03		%/°C	
I_{LX}	Input Leakage Current			5.0	μA	$V_{IN} = -20$ V
	Analog Switch Delay,					
t_{df}	rise and fall times		0.7		μs	$V_{GG} = -27$ V
t_f	(10% to 90% points)		0.5		μs	
t_{dr}			1.1		μs	
t_r			0.25		μs	

TYPICAL ELECTRICAL CHARACTERISTICS

ON RESISTANCE VERSUS POWER SUPPLY VOLTAGE (V_{GG}) OUTPUT VOLTAGE (REF. 2)

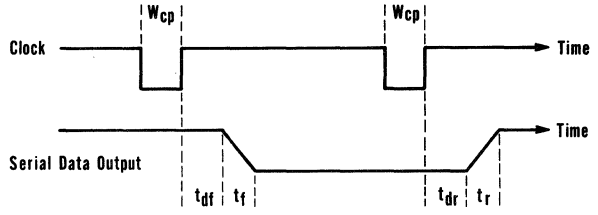


ON RESISTANCE VERSUS OUTPUT VOLTAGE (REF. 2)



TIMING DIAGRAM

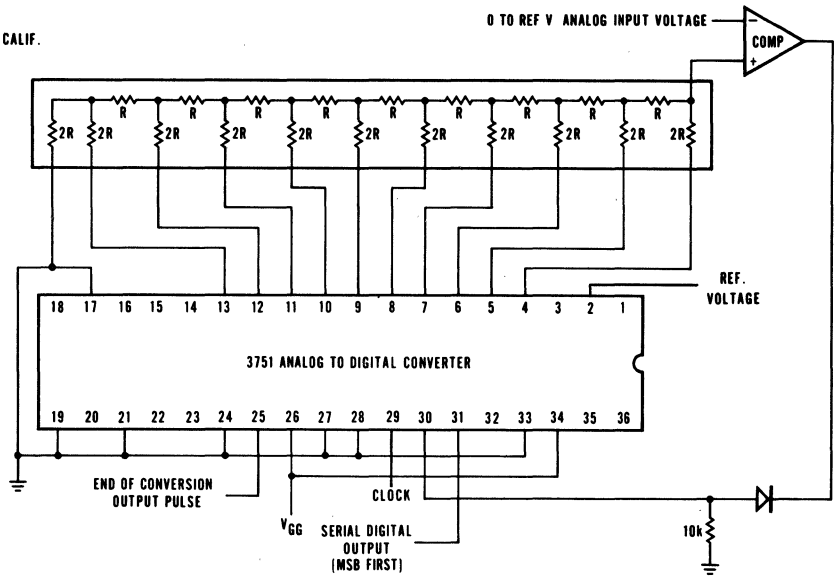
OUTPUT DELAY, RISE AND FALL TIMES



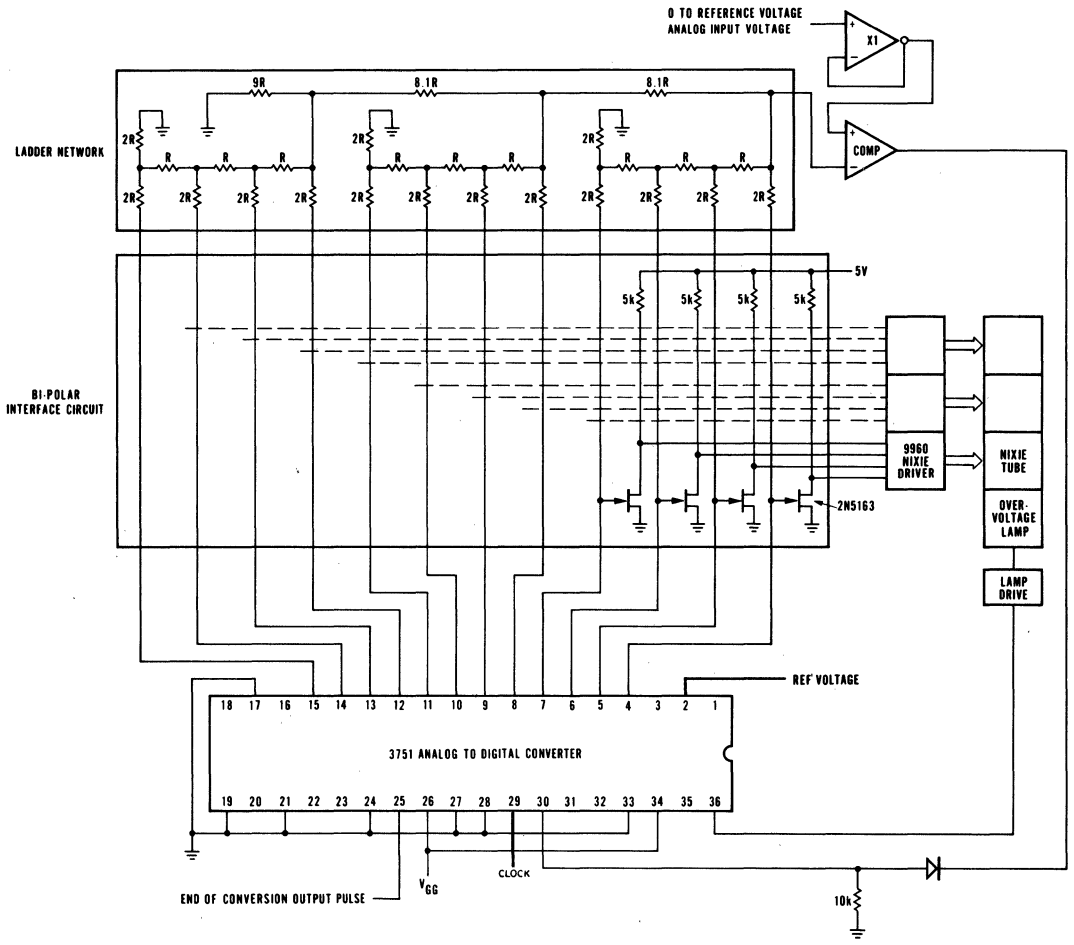
TEN BIT A/D CONVERTER

NO. OF BITS	R VALUE
8	12.5k
9	25k
10	50k
12	200k

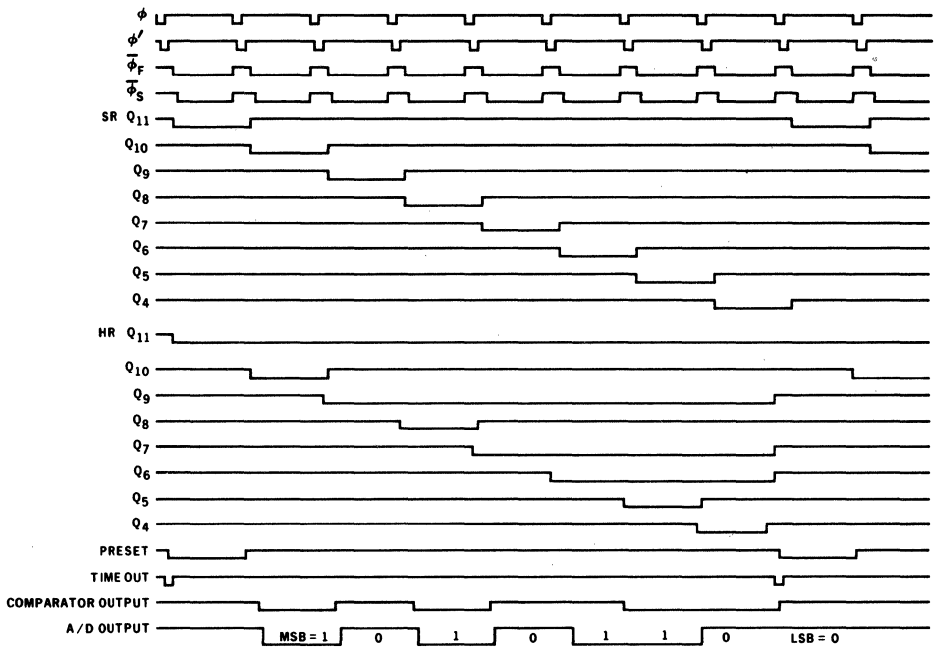
LADDER NETWORK MFGR'S
MEGADYNE CORP., ROCHESTER, N.Y.
ANGSTROM PRECISION INC., VAN NUYS, CALIF.



THREE DIGIT BCD A/D CONVERTER



TYPICAL TIMING DIAGRAM



8 BIT FORMAT
ANALOG INPUT = −3.369 V = 10101100
REFERENCE VOLTAGE = −5.000 V
FIGURE 3

DESCRIPTION OF PIN FUNCTION

PIN NO.

24, 21 A, B: These two pins are connected as shown in the truth table below to control the length of the digital word.

	8	9	10	12
A	1	0	1	0
B	1	1	0	0

25 TIME OUT: A synchronous pulse with the clock is applied at this output at the end of each conversion. This pulse may be used to step a multiplexer or otherwise notify the system of the readiness of the A/D to start another conversion.

26 CLOSED LOOP CONTROL: A '1' voltage level continuously applied to this input will put the A/D in an automatic mode of operation. The time output pulse is internally gated to cause a preset at the end of each conversion and initiate a new conversion. The automatic start circuitry presets the circuit and restarts the conversion if a bit has been dropped in this mode of operation.

27 D.C. PRESET: A '1' voltage level applied to this input will cause an immediate preset and the unit will stay preset until this input is returned to a '0' voltage level.

28 A.C. PRESET: When a '1' level is applied to this input, the A/D is preset on the next clock pulse. The unit will continue to be preset on each clock pulse until the '1' level is removed from the input.

31 A/D OUTPUT: The serial digital conversion is available at this pin in a most significant bit (MSB) first format. The data output is delayed by one bit time.

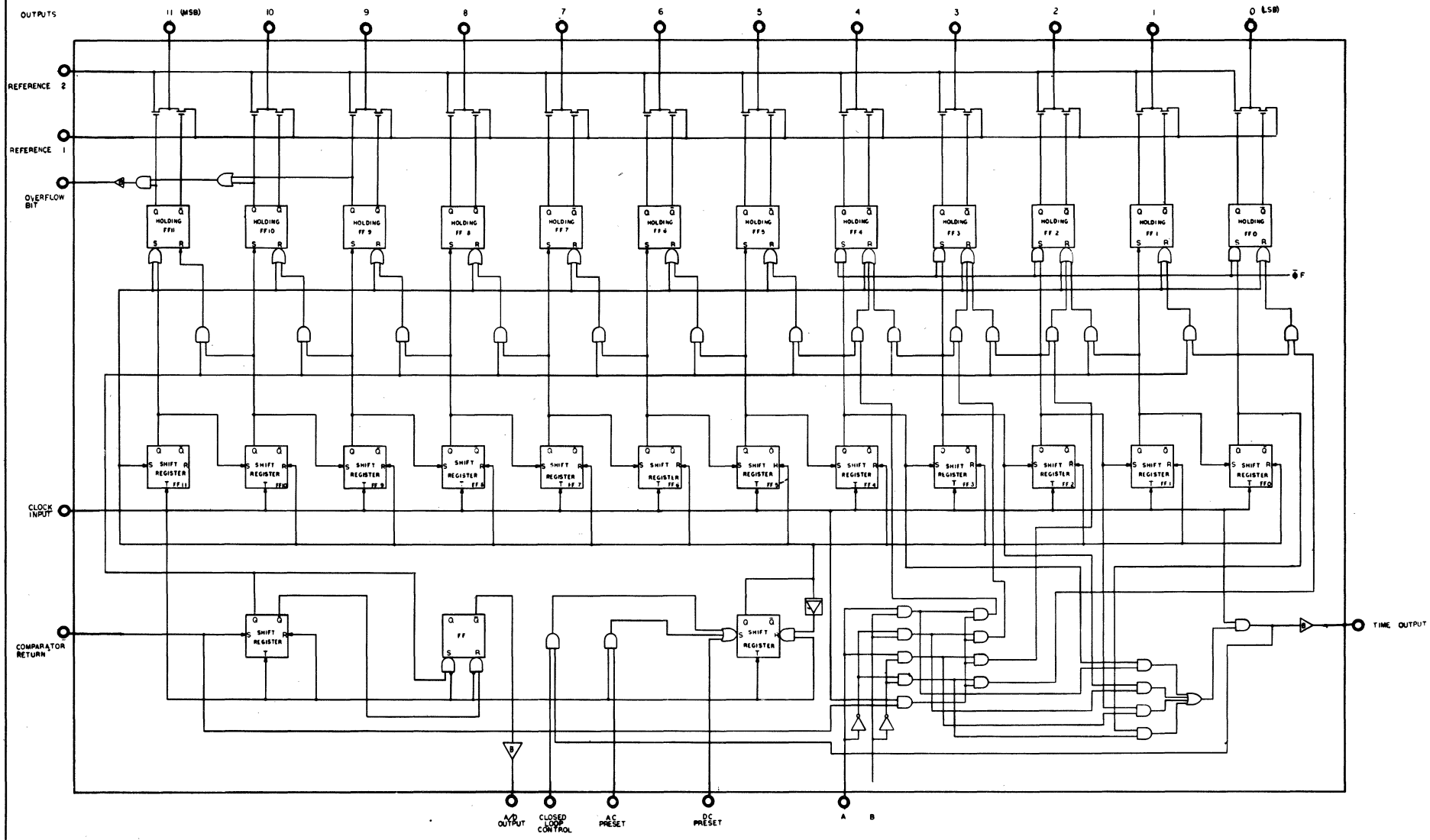
36 BCD OVERVOLTAGE: This output is used when a three digit analog to binary coded decimal (BCD) conversion is being made. If the binary equivalent of the most significant digit is greater than 9, a '1' voltage level is applied on this output.

33 RETURN-TO-ZERO: This input modifies the digital code format from non-return-to-zero (NRZ) to return-to-zero (RZ) if used. When tied to the clock line, the digital output will return to zero during each clock pulse. The RZ duty cycle can be varied by controlling the length of time that a '1' level is applied to this input.

30 COMPARATOR RETURN: The comparator output should be connected to this input. The input must be prevented from going positive with respect to substrate (ground). The output SPDT MOS switches are successively toggled to the reference voltage. This input will cause these switches to be conditionally reset if the ladder network output voltage is greater than the signal voltage.

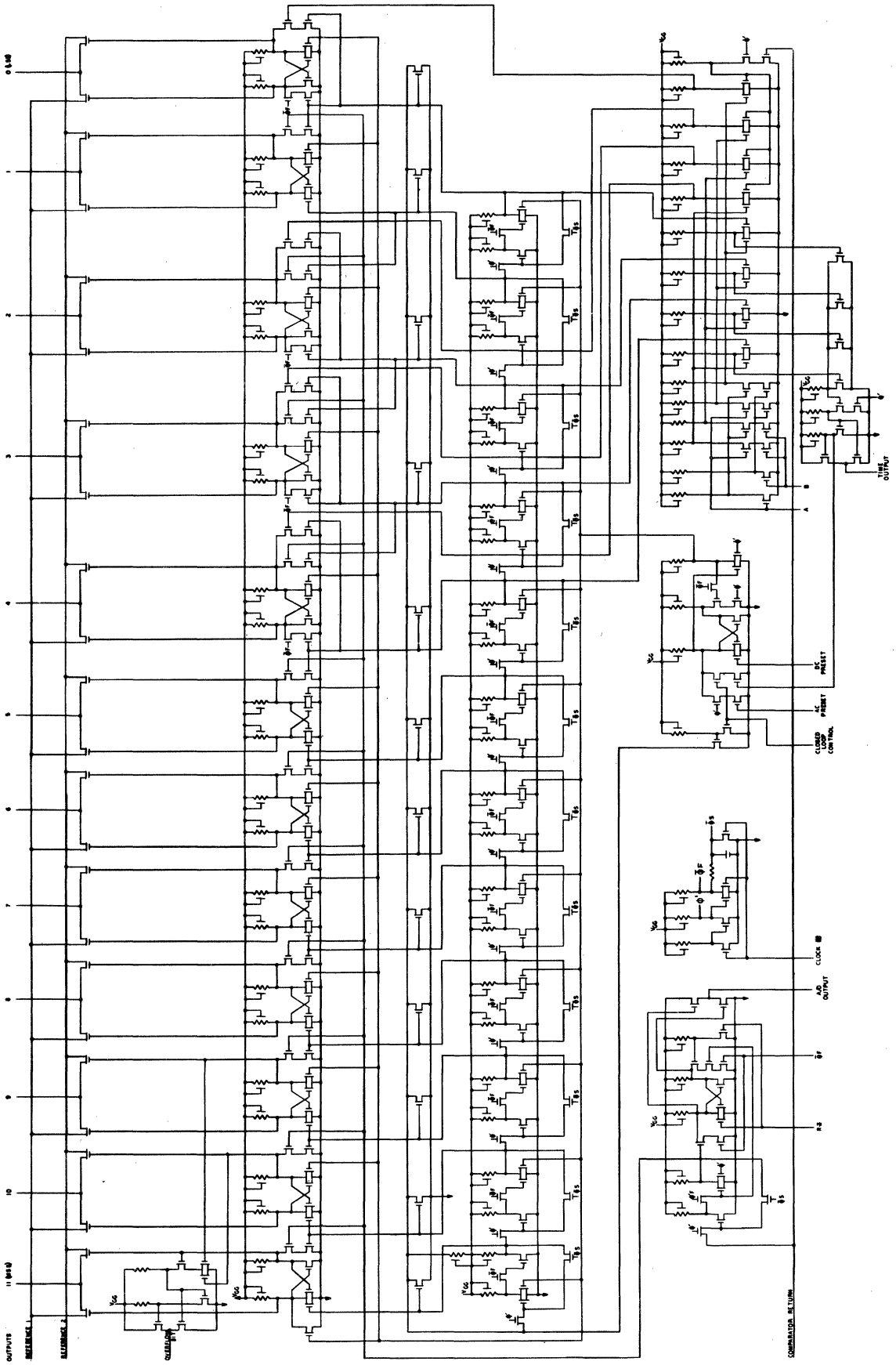
2, 17 REFERENCES 1 & 2: Reference 1 is normally connected to ground and reference 2 to −5.0 volts. However, they may each be connected anywhere between 0 and −5.0 volts D.C. for special applications.

LOGIC BLOCK DIAGRAM



NOTE: Polarity indicators (0) external to the solid box conform to MIL-STD-806B where 0 indicates the less positive state is active. Internal to the box and in the remainder of this data sheet conventional MOS polarities are used, where HI = "1" ≈ −10 V and 1.0 = "0" ≈ Gnd.

SCHEMATIC DIAGRAM



3800

8-BIT PARALLEL ACCUMULATOR

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3800 is a LSI-MOS integrated circuit containing approximately 200 gates. It functions as an eight bit slice of an arithmetic unit, which may be connected to form any word length. It is capable of parallel addition and subtraction, and by simultaneously shifting the sum or difference right or left, multiplication and division algorithms. A direct subtraction capability eliminates the need for the usual carry input to the LSB during subtraction, thus allowing operands to be located anywhere in the truly variable word length accumulator. The parallel data organization of the 3800 improves speed and greatly reduces the amount of random control logic when compared to the same function performed serially.

FEATURES

- **DIRECT SUBTRACTION USED TO PROVIDE VARIABLE WORD LENGTH CAPABILITY**
- **STROBED OUTPUTS FOR HARD WIRE COMMON BUS SYSTEMS**
- **DC TO 200 kHz ADD AND SHIFT RATE**
- **3.0 μs, 8 STAGE CARRY PROPAGATION TIME**
- **LOW POWER — 180 mW**

APPLICATIONS

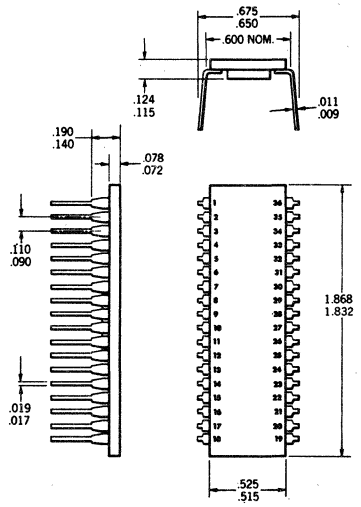
Basic Accumulator Block
Index Register
$>, =, <$ Comparator
General Logic Control
Up-Down Counter
Divide By N Counter

ABSOLUTE MAXIMUM RATINGS

Input Voltages	−30 V to +0.3 V
V_{GG} and V_{DD} Supply Lines	−30 V to +0.3 V
Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +85°C

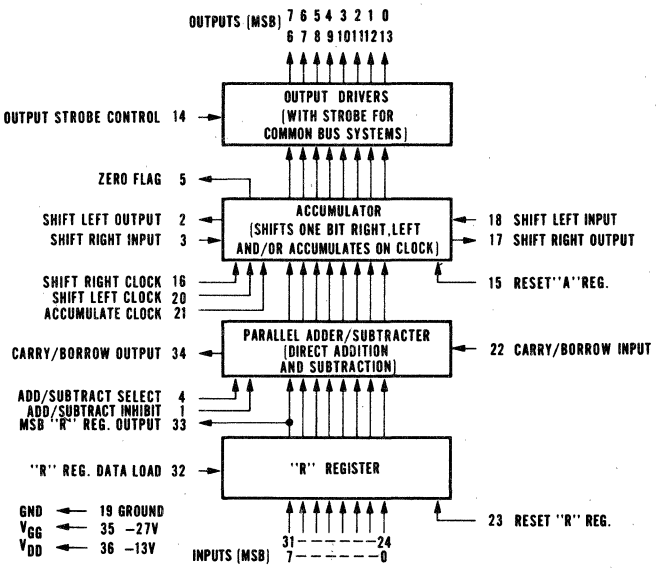
PHYSICAL DIMENSIONS

36-Pin
Dual In-Line Package

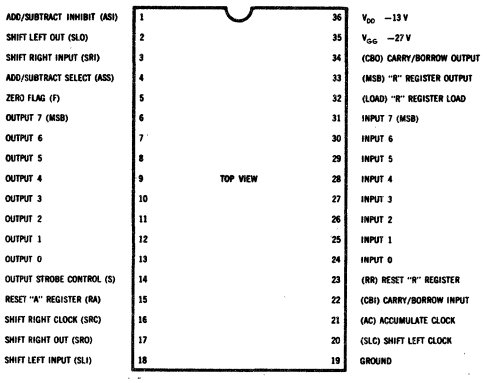


ORDER PART NO. A6H380014X (−55°C to +85°C)
A6H380019X (0°C to 70°C)

BLOCK DIAGRAM



PIN CONFIGURATION



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313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD MOS INTEGRATED CIRCUIT 3800

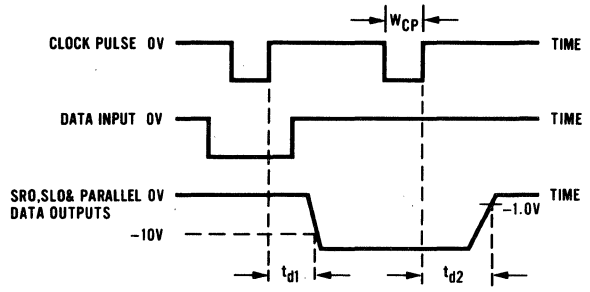
ELECTRICAL CHARACTERISTICS $V_{GG} = -27\ V \pm 1\ V$, $V_{DD} = -13\ V \pm 1\ V$, $R_L = 10\ M\Omega$, $C_L = 10\ pF$ (unless otherwise specified)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Logic inputs					
	Logic "0"	0		−2.0	Volts	$V_{GG} = -27\ V$
	Logic "1"	−10		−30	Volts	$V_{GG} = -27\ V$
	Clocks					
	Amplitude	−10		−30	Volts	
	Width	1.0		10	μs	
	Shift frequency	DC		300	kHz	
	Shift & add frequency	DC		200	kHz	
	Delay Times					
t_{CB}	8 stage carry		3.0	5.0	μs	See Figure 1
t_{d1} & t_{d2}	Output delay		1.0	3.0	μs	See Figure 1
I_{LX}	Input leakage current			5.0	μA	$V_{IN} = -20\ V$
	Logic outputs					
	Logic "0"	0	−0.5	−1.0	Volts	
	Logic "1"	−11	−12		Volts	
	Logic "1"	−10	−11		Volts	$R_L = 40\ k\Omega$
	Supply current drain					
	V_{DD}			7.0	mA	$V_{GG} = -27\ V$, $V_{DD} = -13\ V$
	V_{GG}			5.0	mA	$V_{GG} = -27\ V$, $V_{DD} = -13\ V$
	Network dissipation		180		mW	

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	Add/subtract inhibit	ASI	When ASI is a logic "1", no addition or subtraction will occur when the ACC, SRC or SLC clock are pulsed. The accumulator register will shift right or left normally however. The carry/borrow through line is not affected, allowing numbers to be shifted and compared when the subtract mode is selected.
2	Shift left output	SLO	SLO is the MSB output of the ACC and may be connected directly to the SLI input of the next eight bit section of the accumulator. Shift and add function normally.
3	Shift right input	SRI	SRI accepts the SRO output of a higher order, 8 bit slice. Shift and add function normally.
4	Add/Subtract select	ASS	When ASS is a logic "1", addition is performed, and when ASS is a logic "0", subtraction is performed.
5	Zero flag	F	The zero flag output is a logic "1" only if the accumulator register contains all zeros. This output is independent of the strobe control.
6-13	Outputs	7-0	When the strobe control STR is a logic "0", all outputs represent the contents of the accumulator register.
14	Output strobe control	STR	When STR is a logic "1", all parallel outputs, 0-7, are disconnected from the power and ground lines allowing them to float. Thus several similar outputs may be hard wired together for a common buss system.
15	Reset Accum. register	RA	When RA = logic "1", the accumulator is reset to zero. This asynchronous signal overrides all others.
16	Shift right clock	SRC	Pulsing the SRC with a logic "1" shifts the contents of the accumulator one bit position to the right. If the add/subtract controls are enabled, the sum or difference of the accumulator register and the "R" register is shifted one bit to the right and written into the accumulator.
17	Shift right output	SRO	SRO is the LSB end of the 8 bit accumulator and may be connected directly to the SRI of an adjacent 8 bit slice.
18	Shift left input	SLI	The SLI accepts the SLO output from a lower order, 8 bit slice.
19	Ground	GND	Circuit common and substrate ground are both connected to this pin.
20	Shift left clock	SLC	Pulsing the SLC with a logic "1" shifts the contents of the accumulator one bit position to the left. If the add/subtract controls are enabled, the sum or difference of the accumulator and the "R" register is shifted one bit to the right and written into the accumulator.
21	Accumulate clock	AC	Pulsing the AC input adds the contents of the accumulator and the "R" register if ASS = logic "1". The "R" register is subtracted from the accumulator if ASS = "0". If ASI = "1", no action occurs.
22	Carry/borrow input	CBI	A logic "1" on CBI enters a carry or borrow into the LSB position of the add/subtract logic.
23	Reset "R" register	RR	Placing a logic "1" on RR asynchronously resets the "R" register.
24-31	Inputs	0-7	Inputs are entered into the "R" register asynchronously when RL is activated.
32	"R" register data load	RL	When RL is a logic "1", data presented at the inputs are loaded into the "R" register. RL may be permanently a logic "1", effectively bypassing the R register during normal operation. Note that RR overrides the data inputs regardless of the load command.
33	MSB "R" register output	MSB	It shows the MSB of the "R" register. When the "R" register is used to temporarily hold operands during multiply, divide, etc., the MSB output indicates the sign of the stored operand.
34	Carry/borrow output	CBO	The CBO is the asynchronous carry or borrow output from the MSB of the add/subtract logic. It is not affected by the ASI control.
35	V_{GG} power supply	V_{GG}	−27 V supply.
36	V_{DD} power supply	V_{DD}	−13 V supply.

SHIFT COMMAND TIMING DIAGRAM



CARRY/BORROW 8 STAGE PROPAGATION TIME

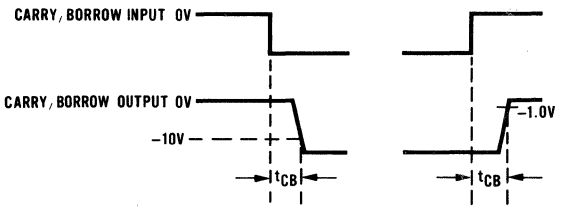
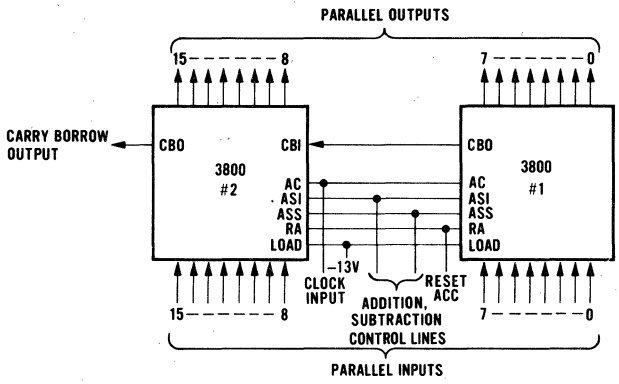


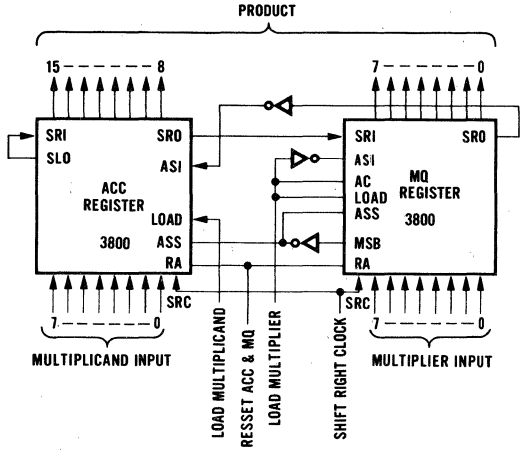
FIGURE 1

STANDARD CONNECTIONS FOR ADDITION AND SUBTRACTION



SIXTEEN BIT PARALLEL ADDITION (SUBTRACTION)*: The addition (subtraction) operation begins by resetting the accumulator, then transferring the augend (subtrahend) through the "R" register into the accumulator by pulsing the AC clock line. The operation is completed by loading the addend (minuend) into or through the "R" register, then adding (or subtracting if ASS = logic "0") it from the accumulator by again pulsing the AC clock. Multiple addition and subtraction or combinations of both operations may be performed by repeating the last operation. Thus a running total may be kept in the accumulator.

STANDARD CONNECTIONS FOR MULTIPLICATION

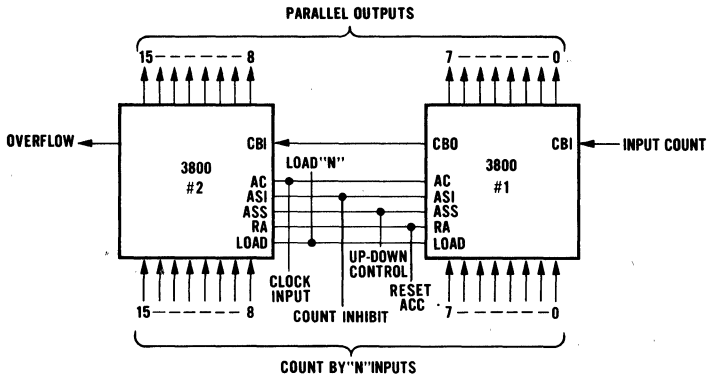


MULTIPLICATION: The multiplication operation, shown above, begins by clearing the ACC and MQ registers, then loading the multiplier into the MQ "R" register. If the MSB of the MQ's "R" register is a "1", ie. the multiplier is negative, the ACC and MQ subtract lines are enabled before the multiplier is transferred into the MQ. Thus the multiplier in the MQ is always positive. However, the multiplicand, which has been loaded into the ACC "R" register for temporary storage, will be subtracted from the partial product in the ACC if the multiplier was negative. The multiplicand is added to or subtracted from the partial product and shifted one bit to the right each time the LSB of the MQ register is a "1". If it is a "0", only a shift right occurs. Neither the multiplicand nor the resulting product require any further sign corrections as the answers will automatically be in two's complement.

DIVISION: The division algorithm is similar to the multiply and is described in detail in The Logic of Computer Arithmetic by Flores. The most straightforward way to perform division is to convert both the divisor and dividend to sign magnitude numbers the same way the multiplier was converted in multiplication. Then proceed through a successive subtraction division. The resulting positive quotient must however then be corrected to two's complement rotation if the signs of the dividend and the divisor were not the same.

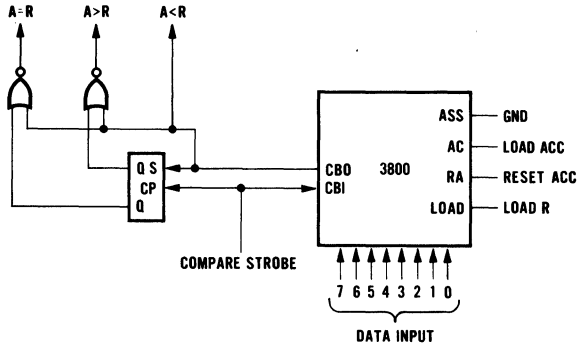
NOTES: 1. Input logic levels may be selected by referring to the list of Pin Function Descriptions.
2. All unused input or control pins should be grounded.
3. All operands are in two's complement notation.
4. All diagrams are BASIC BLOCK DIAGRAMS and no electrical levels are indicated. See Logic Diagram for correct 806B notation.

APPLICATIONS



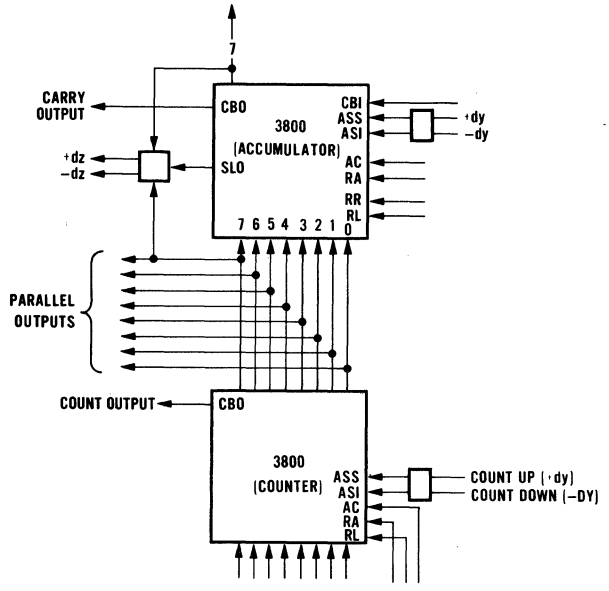
UP-DOWN COUNTER

SIXTEEN STAGE UP-DOWN COUNTER: Operation begins by resetting the registers and enabling ASS, which determines the count direction. Counting by one may be accomplished by enabling CBI or INPUT "0". To count by n, set n into the "R" register.



L, = > COMPARATOR

COMPARE OPERATION: To compare two numbers, simply insert the first into a previously cleared accumulator by pulsing AC. Enabling the subtract control will immediately indicate whether R>A, as a borrow output will appear. If the borrow output follows a pulse on the borrow input, the numbers are equal. If neither, then R<A. The logic is shown above.

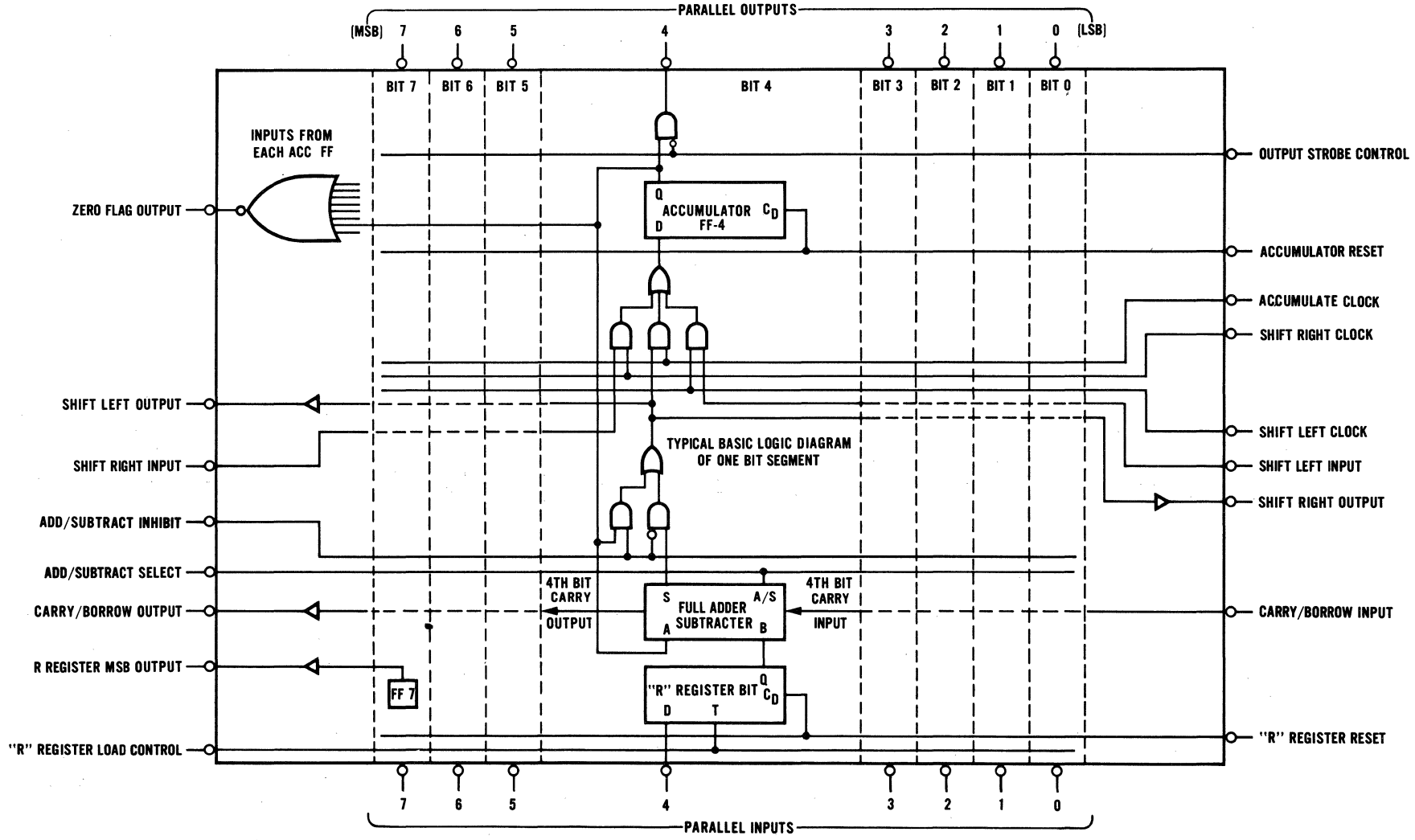


INITIAL CONDITION INPUTS

DDA CONNECTIONS

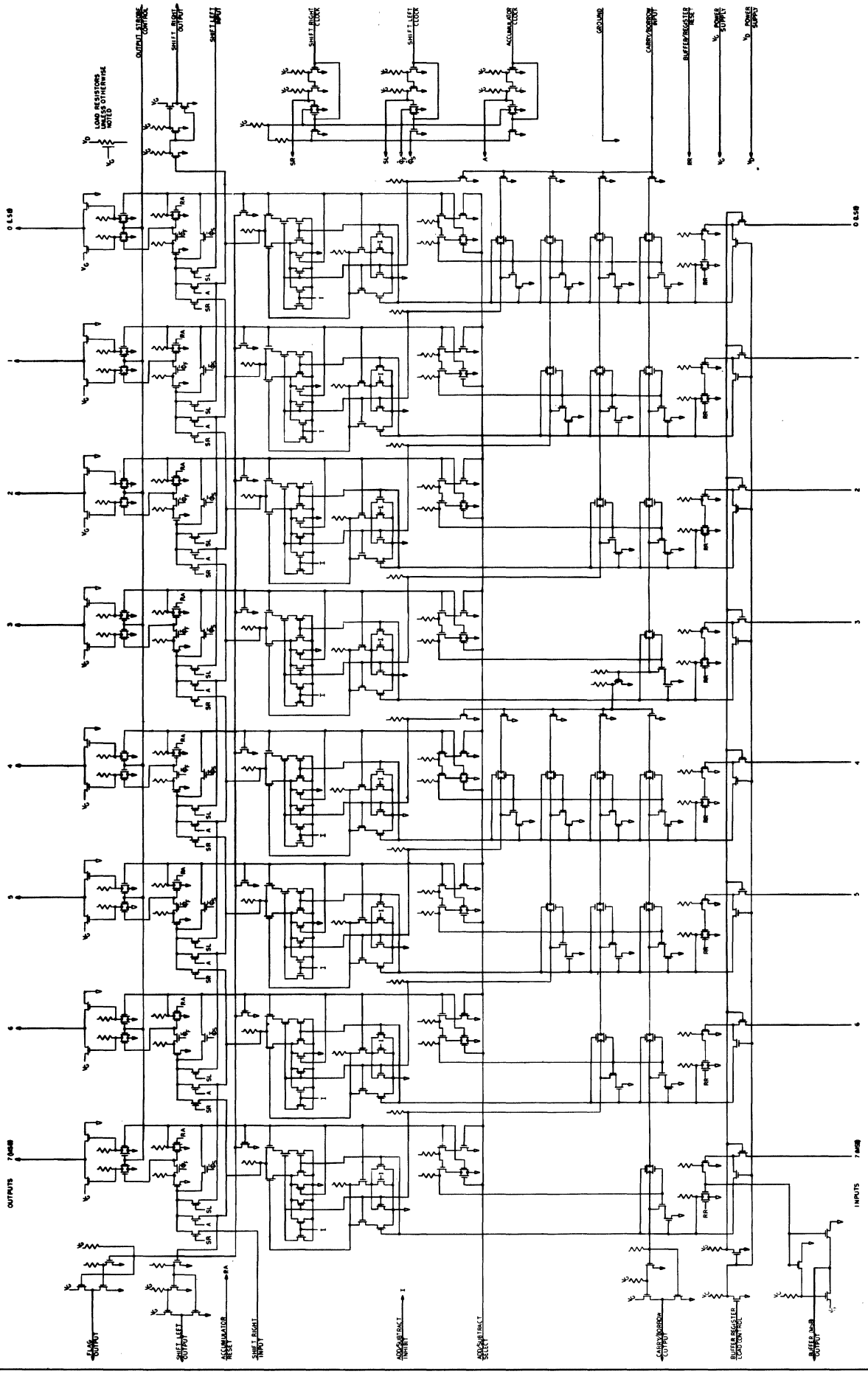
The DDA shown above utilizes one 3800 for a remainder register and a second 3800 for a y accumulator counter.

LOGIC BLOCK DIAGRAM



NOTE: Polarity indicators (0) external to the solid box conform to MIL-STD-806B where 0 indicates the less positive state is active. Internal to the box and in the remainder of this data sheet conventional MOS polarities are used, where HI = "1" ≈—10 V and LO = "0" ≈ Gnd.

SCHEMATIC DIAGRAM



3801

10-BIT SERIAL/PARALLEL-PARALLEL/SERIAL CONVERTER

MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3801 is a monolithic MOS/LSI ten bit serial/parallel - parallel/serial converter utilizing P-Channel Enhancement mode MOS technology. The device has the capability of serial or parallel input and serial or parallel output. A holding register included on the chip is isolated from the shift register by transfer gates. In serial to parallel applications data may be stored in the holding register while new data is being entered into the shift register.

FEATURES

- **8 AND 10 BIT SERIAL OUTPUT**
- **250 kHz SERIAL TO PARALLEL OPERATION**
- **500 kHz PARALLEL TO PARALLEL OPERATION**
- **120 mW POWER DISSIPATION**
- **INPUT GATE PROTECTION**
- **SET AND RESET OF HOLDING REGISTER**
- **OUTPUT STROBE CONTROL**
- **SINGLE PHASE CLOCK**
- **RESET OF SERIAL REGISTER**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

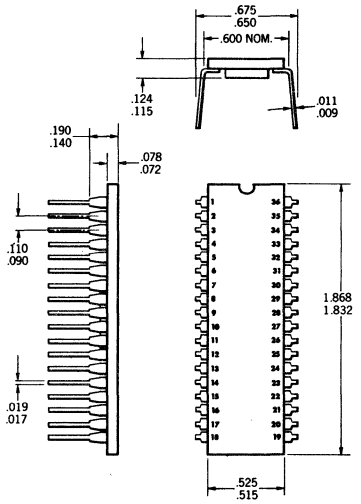
Input Voltages	−30 to +0.3 Volts
Power Supply	−30 Volts
Storage Temperature	−55°C to +150°C
Operation Temperature (A6H380114X)	−55°C to +85°C
(A6H380119X)	0°C to +70°C

APPLICATIONS

Serial and Parallel Data Conversion in

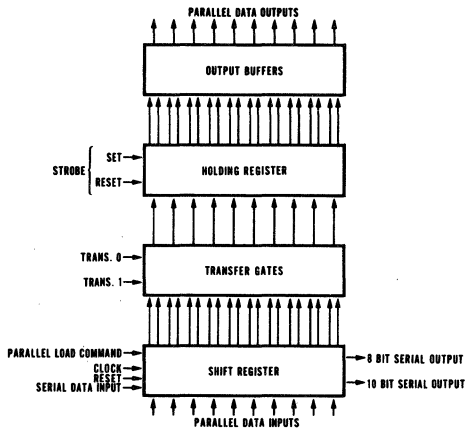
- Process Control
- Data Terminals
- Computer Peripheral Equipment
- Data Acquisition

PHYSICAL DIMENSION
36 PIN
DUAL IN-LINE PACKAGE

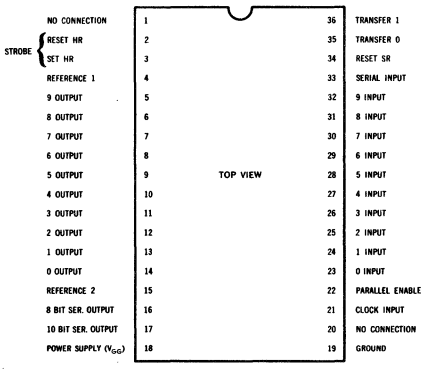


ORDER PART NO. A6H380114X
A6H380119X

BLOCK DIAGRAM



PIN CONFIGURATION



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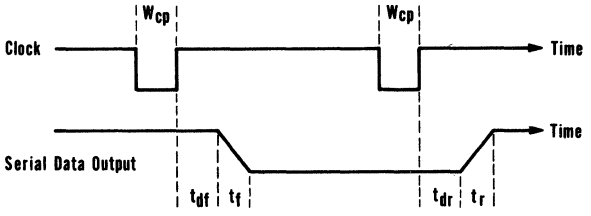
ELECTRICAL CHARACTERISTICS ($V_{GG} = -27 \pm 2.0$ Volts, $R_L = 10M\Omega$, $C_L = 10$ pF unless otherwise specified)

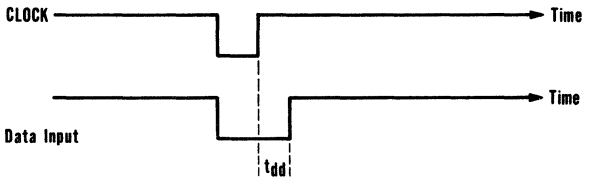
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
	Logic Inputs					
	"0"	0		−2.0	Volts	
	"1"	−9.0		−30	Volts	
	Logic Outputs					
	"0"	0		−1.0	Volts	
	"1"	−10	−11		Volts	$R_L = 40$ kΩ
	"1"	−11	−12		Volts	
	Clock					
	Amplitude	−9.0		−30	Volts	
	Width	1.0		10	μs	
f_{max}	Frequency					
	Serial	DC		250	kHz	
	Parallel	DC		500	kHz	
t_{df}	Serial Delay,		0.6		μs	
t_f	rise and fall		0.2		μs	
t_{dr}	times		0.5		μs	
t_r			0.5		μs	
t_{df}	Parallel Delay,		0.55		μs	
t_f	rise and fall		0.35		μs	
t_{dr}	times		0.4		μs	
t_r			0.3		μs	
C_{in}	Data and Control Input Capacitance		7.0		pF	
I_{max}	Power Supply Current Drain		4.5	7.0	mA	$V_{GG} = -27$ V
P_{max}	Power Dissipation		120	190	mW	$V_{GG} = -27$ V
I_{LX}	Input Leakage Current			5.0	μA	$V_{in} = -20$ V
t_{dd}	Data Delay Time	250			ns	

TIMING DIAGRAM

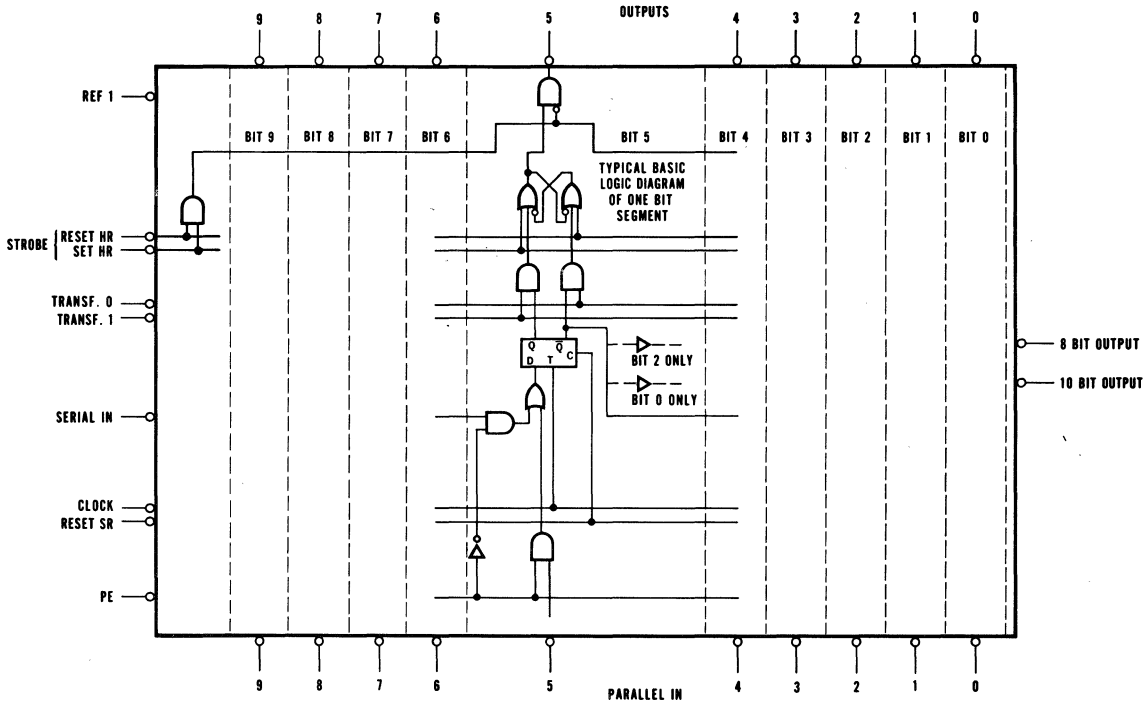
OUTPUT DELAY, RISE AND FALL TIMES



DATA BIT TIMING

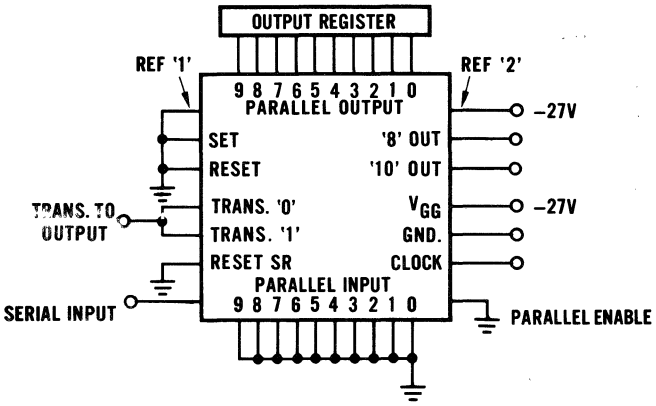


LOGIC DIAGRAM

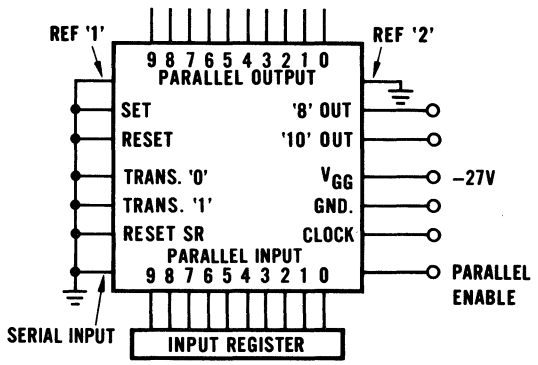


APPLICATIONS (Basic Logic Representation)

SERIAL TO PARALLEL CONVERTER



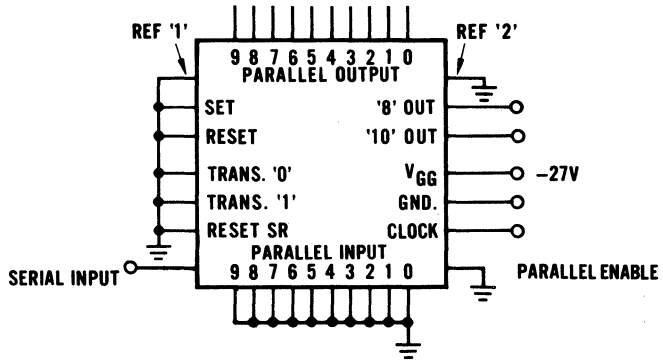
PARALLEL TO SERIAL CONVERTER



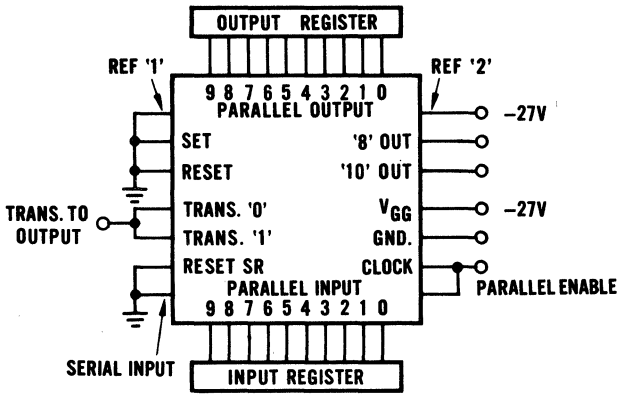
APPLICATIONS

(Basic Logic Representation)

SERIAL TO SERIAL BUFFER REGISTER



PARALLEL TO PARALLEL BUFFER REGISTER



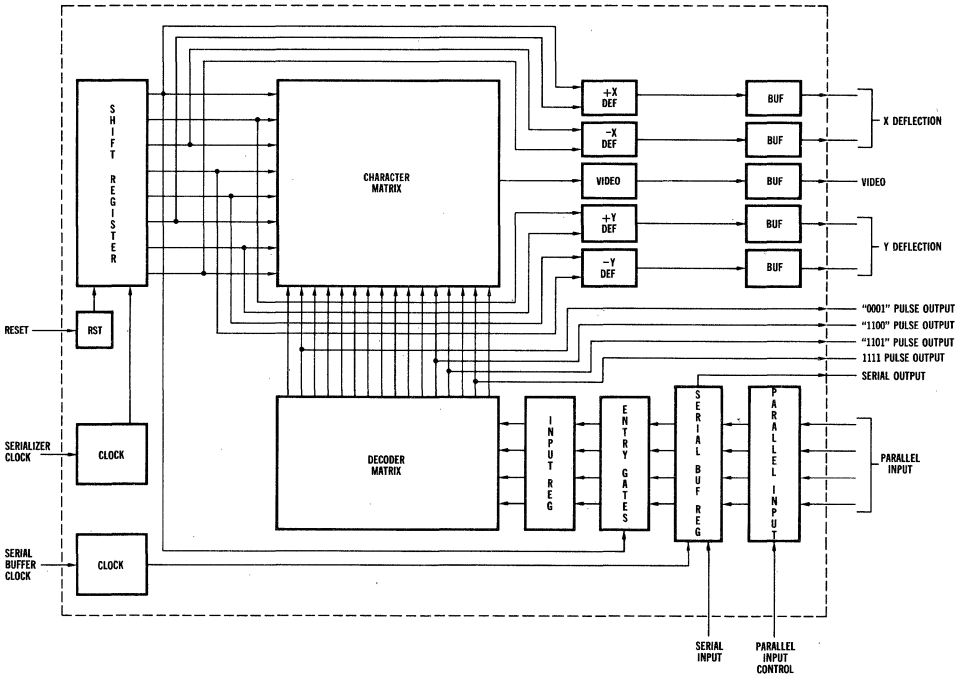
FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

3250 CRT NUMERIC CHARACTER GENERATOR

The 3250 is a numeric character generator subsystem on a single chip. It is designed to be used in conjunction with a cathode ray tube to display numeric information. Deflection pulses are provided to sweep the beam through a seven segment character in eight clock pulses. Video pulses, synchronized with the deflection pulses, are provided to blank the appropriate segments needed to form numerals. Approximately 520 characters may be displayed at a 60 cps refresher rate. Systems applications are simplified by enabling parallel data entry from a keyboard directly into a serial shift register on the chip.

FEATURES:

- Direct Keyboard Entry
- BCD Input
- Low Power Consumption—160 mW Typical
- Serial on parallel storage buffer entry
- 250 kHz Segment Rate
- Special outputs for "1" offset and decimal point



3305 QUAD 16 BIT STATIC SHIFT REGISTER

The 3305/6 is a 64-bit 1ϕ static shift register. The 3305 is a Quad 16 in a DIP package and the 3306 is a Dual 16, Single 32 in a TO-100 package. It is a monolithic integrated circuit utilizing Planar II*, P-channel Enhancement Mode Technology.

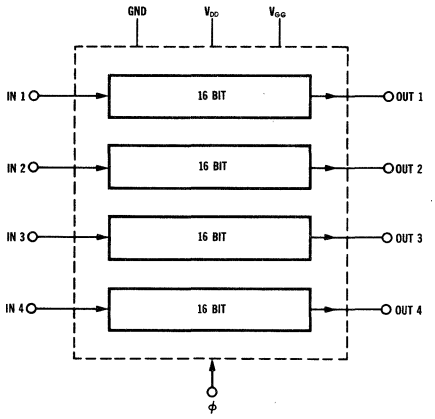
FEATURES:

- Single Phase Clock
- Low Power Consumption less than 3 mW/bit
- High Speed Operation—DC to 1.0 MHz

APPLICATIONS:

Delay line and binary or BCD storage in

- Calculators
- Peripheral Equipment
- Data Acquisition
- Telemetry
- Computers & Business Machines
- Machine Control



3321 — DUAL 256 BIT SHIFT REGISTER

The 3321 is a Dual 256 bit Dynamic, serial in-serial out shift Register utilizing a 4 phase (0) clock. The 4 input clock lines are used to enhance the speed and power characteristics of MOS technology and can be operated at frequencies from 10kHz to 2 MHz.