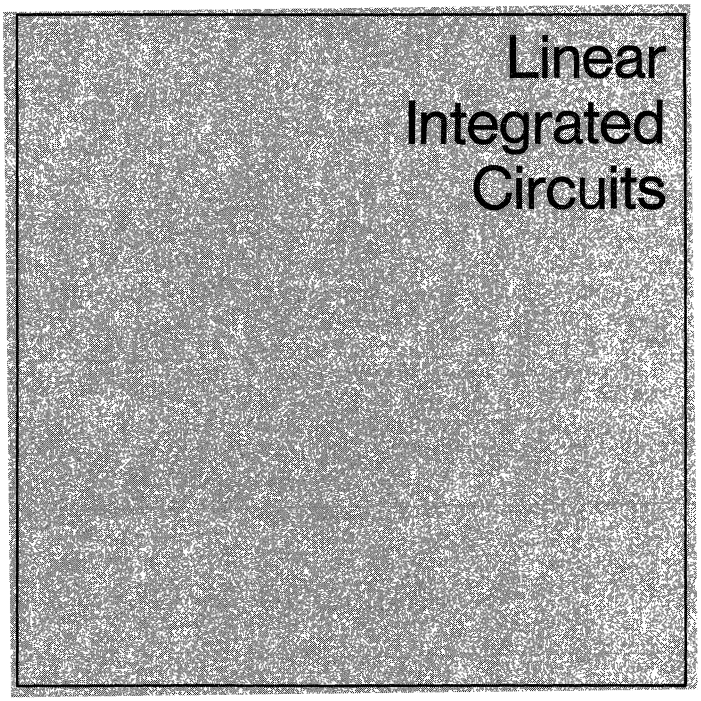

Linear
Integrated
Circuits

LINEAR INTEGRATED CIRCUITS NUMERICAL INDEX

LINEAR APPLICATIONS/PRODUCTS CROSS REFERENCE

Differential Input, Differential Output Amplifiers	μA727, μA730, μA733
Operational Amplifiers	
General Purpose —	
Summing, Subtracting, Integrate, Differentiate, Impedance Transformer Analog Computers	μA702, μA709, μA715, μA739, μA740 and μA741
Instrumentation —	
Low drift, Chopper stabilized, Strain gage, Thermocouple	μA726, μA727
High Input Impedance —	
Active filters, Buffer amps, Transducers, Integrators	μA727, μA740, μA715
Low Power Consumption —	
Battery powered, Airborne, Spaceborne, portable, low weight systems	μ741
High Speed —	
Phase-locked loops, A/D & D/A converters, pulse height analyzers, multiplexed analog gates, sample and holds, integrators, and differentiators	μA702, μA715, μA740
Temperature Stabilized —	
Bridge amplifiers, process control, precision measurements, instrumentation amps.	μA726, μA727
Power/Driver Amplifiers	
Audio Preamp —	
Low noise, magnetic tape, phono	μA730, μA739
Medium Power —	
Telephone Systems, head sets	μA716
Power Driver —	
Servos, Audio	μA716
High Speed Video —	μA715
Comparators	
High Speed —	
Level detectors, Schmitt triggers, Go-No-GO detectors, Window detector, pulse height discriminator, line receivers	μA710, μA711, μA731
Precision —	
Digital volt-meters, A/D and D/A converters, pulse width modulators, phase locked loops, precision measuring equipment.	μA715, μA727, μA740
High Frequency/Communications	
IF Amplifiers —	
Microwave, radar, AM & FM IF strips, TV	μA703, μA717, μA719
Video Amplifiers —	μA702, μA715, μA733
Audio Amplifier —	μA716
Demodulators —	μA737
AGC IF Amps —	μA719
Oscillators	
Audio —	
Telemetry phase detector reference, servo systems	μA709, μA740, μA741
High Frequency —	
Radar, communications receivers and transmitters, radio, TV	μA702, μA703, μA715, μA733

LINEAR APPLICATIONS/PRODUCTS INDEX CROSS REFERENCE

Linear-Digital Interface	
Line Receivers —	μA710, μA711, μA731
Analog to Digital —	
Telemetry, Maintance monitor, process control	μA710, μA715, μA722
Digital to Analog —	
Telemetry, Process Control, displays	μA715, μA722
Television	
Sound —	μA703, AμA717, μA716, μA719
Chroma Oscillator —	μA703
IF Amplifiers —	μA703, μA717, μA719
Chroma Demodulator —	μA737
Digital Computer Systems	
Core Memories —	μA710, μA711, μA731
Other Memories —	
Film, Plated wire, magnetic tape, Disc. file	μA702, μA710, μA733
Displays —	μA715, μA722
Hybrid Computers —	μA722
Power Supplies	
Series Voltage Regulators —	μA723
Switching Voltage Regulators —	μA710, μA711, μA723
Precision Low Drift Voltage Reference —	μA726
Active Filters	μA702, μA709, μA715 μA716, μA739, μA740 μA741
Special Functions	
Digitally Controlled Function Generators —	μA722
Voltage Controlled Function Generator	μA715, μA722, μA741
D.C. Logarithmic Amp	μA726
IF Logarithmic Amp	μA703
Multiplier	μA726, μA737
Dividers	μA726
Product Detector	μA737
Scaler	μA722
Trigonometric Function Generators	μA709, μA726, μA739 μA740, μA741
Medical Electronics	μA727, μA739, μA740 μA741

μA702A

HIGH GAIN, WIDEBAND DC AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

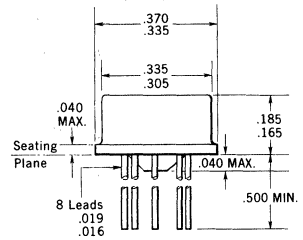
- **IMPROVED SPECIFICATIONS**
- **2 mV MAXIMUM OFFSET VOLTAGE**
- **2500 MINIMUM VOLTAGE GAIN**
- **10 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

GENERAL DESCRIPTION — The μA702A is a complete DC amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for use as an operational amplifier in high speed analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from DC to 30 MHz.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	21 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	+1.5 Volts to −6.0 V
Internal Power Dissipation	
TO-99 [Note 1]	300 mW
Flat Package [Note 2]	200 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C

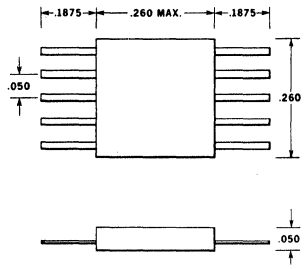
PHYSICAL DIMENSIONS
in accordance with
JEDEC(TO-99) outline



NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

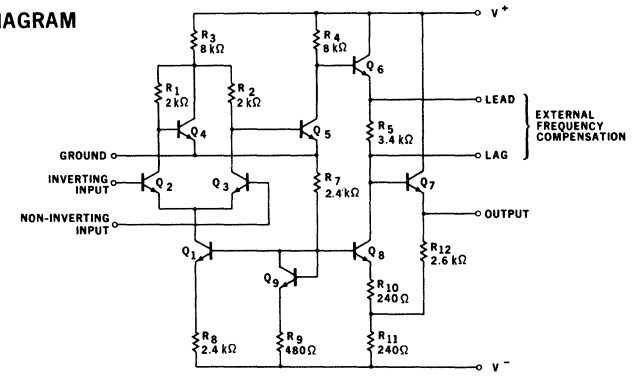
ORDER PART NO. U5B770231X†

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)

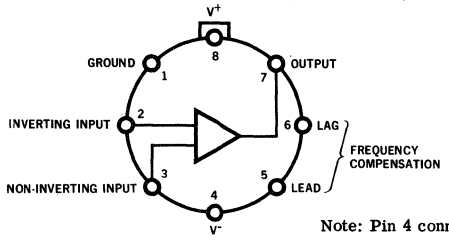


ORDER PART NO. U3H770231X

SCHEMATIC DIAGRAM

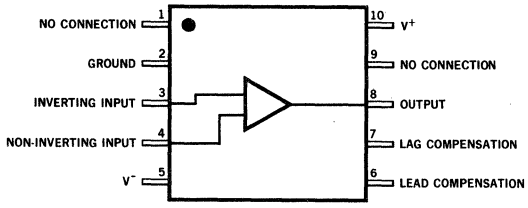


TO-99 CONNECTION DIAGRAM (TOP VIEW)



Note: Pin 4 connected to case.

FLAT PACKAGE CONNECTION DIAGRAM (TOP VIEW)



Notes on page 2

* Planar is a patented Fairchild process.
† Equivalent to U5B77123IX and U3H77123IX

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

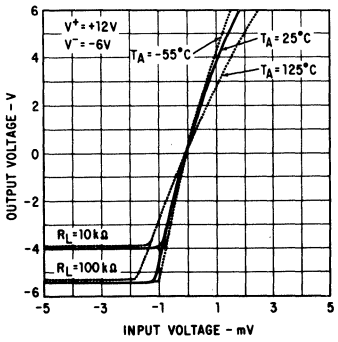
PARAMETER (see definitions)	CONDITIONS	V^+ = 12.0 V, V^- = −6.0 V MIN.	TYP.	MAX.	V^+ = 6.0 V, V^- = −3.0 V MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 2\ k\Omega$		0.5	2.0		0.7	3.0	mV
Input Offset Current			180	500		120	500	nA
Input Bias Current			2.0	5.0		1.2	3.5	μA
Input Resistance		16	40		22	67		kΩ
Input Voltage Range		−4.0		+0.5	−1.5		+0.5	V
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, $f \leq 1$ kHz	80	100		80	100		dB
Large-Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 5.0$ V	2500	3600	6000				
	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 2.5$ V				600	900	1500	
Output Resistance			200	500		300	700	Ω
Supply Current	$V_{out} = 0$		5.0	6.7		2.1	3.3	mA
Power Consumption	$V_{out} = 0$		90	120		19	30	mW
Transient Response (unity-gain)	$C_1 = 0.01\ \mu F$, $R_1 = 20\ \Omega$, $R_L \geq 100\ k\Omega$, $V_{in} = 10$ mV							
Risetime			25	120				ns
Overshoot	$C_L \leq 100$ pF		10	50				%
Transient Response (×100 gain)	$C_3 = 50$ pF, $R_L \geq 100\ k\Omega$, $V_{in} = 1$ mV							
Risetime			10	30				ns
Overshoot			20	40				%
The following specifications apply for $-55°C \leq T_A \leq +125°C$:								
Input Offset Voltage	$R_S \leq 2\ k\Omega$			3.0			4.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = 25°C$ to $T_A = +125°C$		2.5	10		3.5	15	μV/°C
	$R_S = 50\ \Omega$, $T_A = 25°C$ to $T_A = -55°C$		2.0	10		3.0	15	μV/°C
Input Offset Current	$T_A = +125°C$		80	500		50	500	nA
	$T_A = -55°C$		400	1500		280	1500	nA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +125°C$		1.0	5.0		0.7	4.0	nA/°C
	$T_A = 25°C$ to $T_A = -55°C$		3.0	16		2.0	13	nA/°C
Input Bias Current	$T_A = -55°C$		4.3	10		2.6	7.5	μA
Input Resistance		6.0			8.0			kΩ
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, $f \leq 1$ kHz	70	95		70	95		dB
Supply Voltage Rejection Ratio	$V^+ = 12$ V, $V^- = -6$ V to $V^+ = 6$ V, $V^- = -3$ V, $R_S \leq 2\ k\Omega$		75	200		75	200	μV/V
Large-Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 5.0$ V	2000		7000				
	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 2.5$ V				500		1750	
Output Voltage Swing	$R_L \geq 100\ k\Omega$	±5.0	±5.3		±2.5	±2.7		V
	$R_L \geq 10\ k\Omega$	±3.5	±4.0		±1.5	±2.0		V
Supply Current	$T_A = +125°C$, $V_{out} = 0$		4.4	6.7		1.7	3.3	mA
	$T_A = -55°C$, $V_{out} = 0$		5.0	7.5		2.1	3.9	mA
Power Consumption	$T_A = +125°C$, $V_{out} = 0$		80	120		15	30	mW
	$T_A = -55°C$, $V_{out} = 0$		90	135		19	35	mW

NOTES:

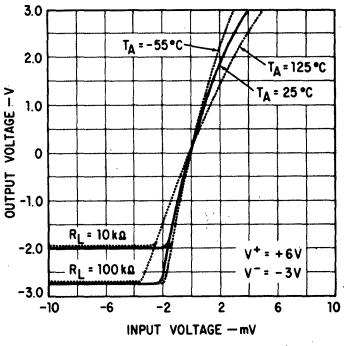
(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +105°C.
(2) Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.

TYPICAL PERFORMANCE CURVES

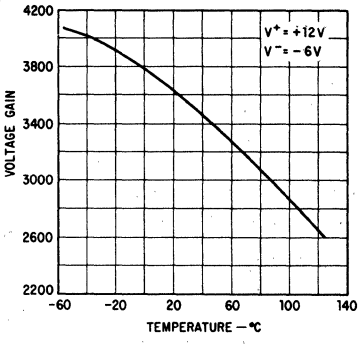
VOLTAGE TRANSFER CHARACTERISTIC



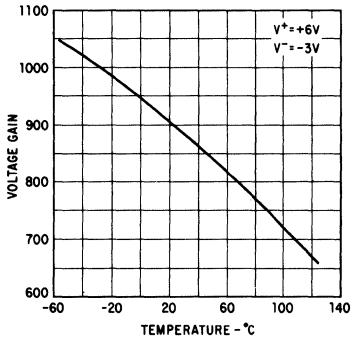
VOLTAGE TRANSFER CHARACTERISTIC



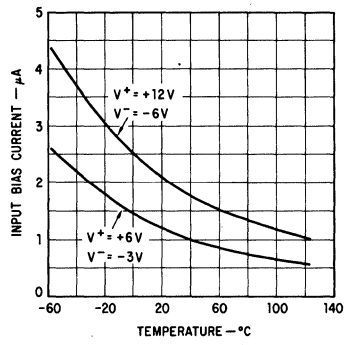
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



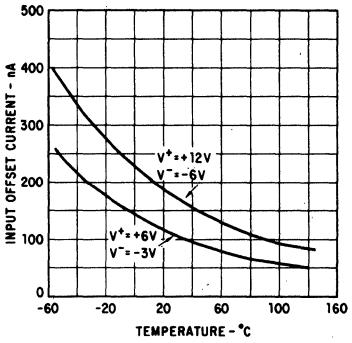
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



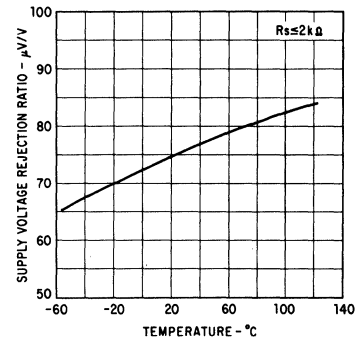
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



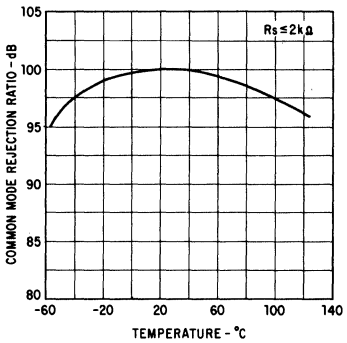
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



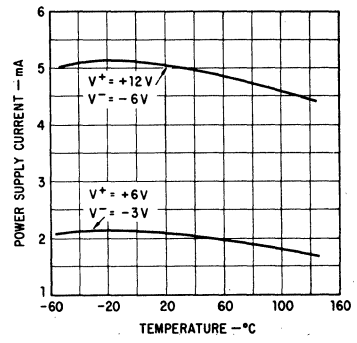
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



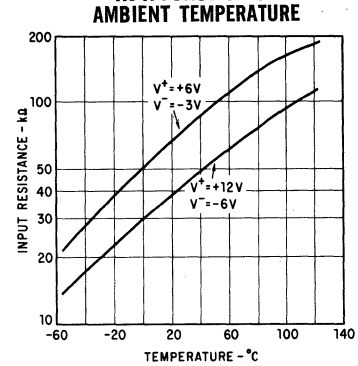
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



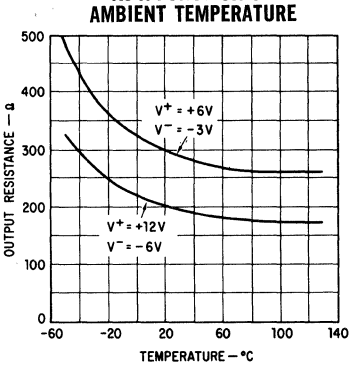
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



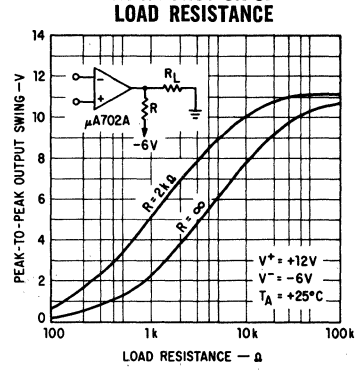
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

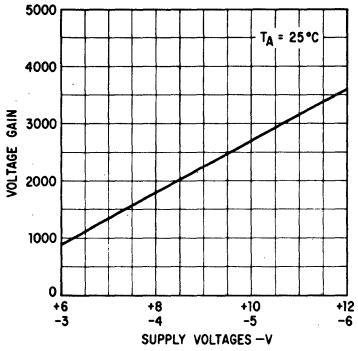


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

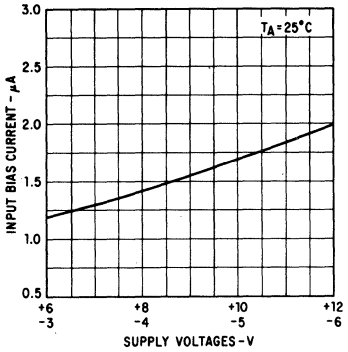


TYPICAL PERFORMANCE CURVES

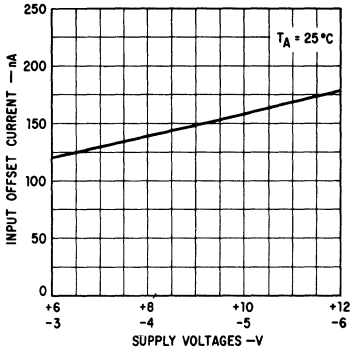
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



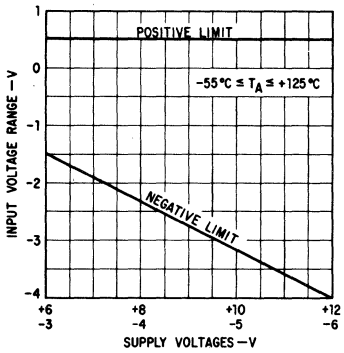
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



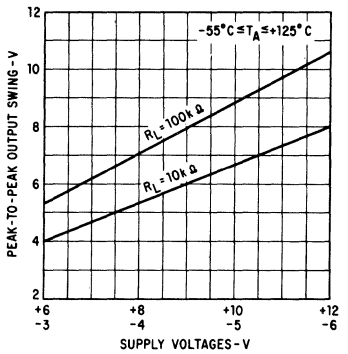
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



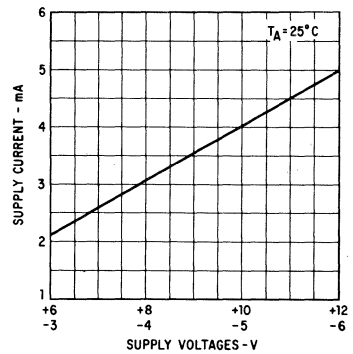
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES



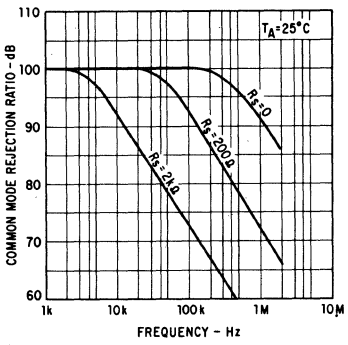
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES



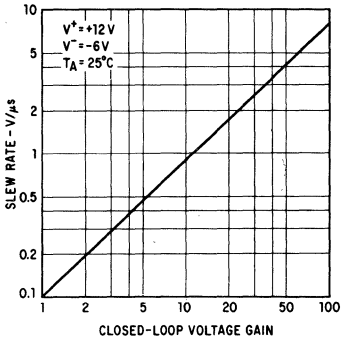
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



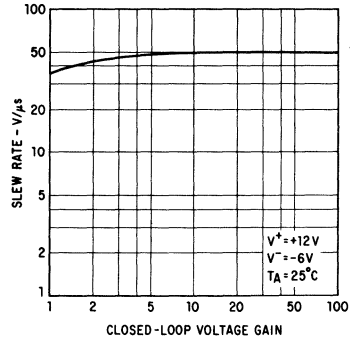
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)

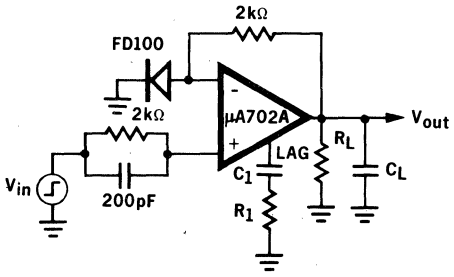


SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)

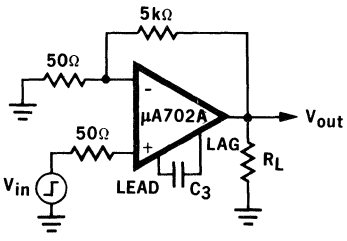


TRANSIENT RESPONSE TEST CIRCUITS

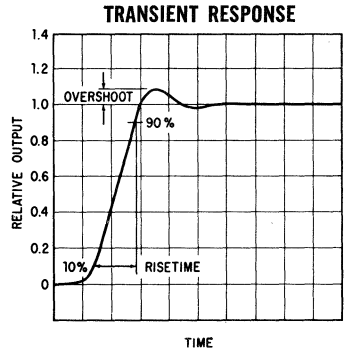
UNITY-GAIN AMPLIFIER (LAG COMPENSATION)



X100 AMPLIFIER (LEAD COMPENSATION)



TRANSIENT RESPONSE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

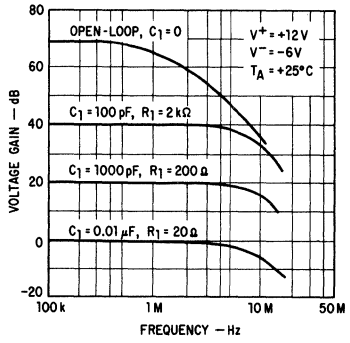
POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

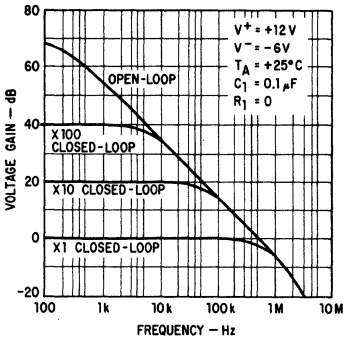
PEAK OUTPUT CURRENT — The maximum current that may flow in the output load without causing damage to the unit.

TYPICAL PERFORMANCE CURVES

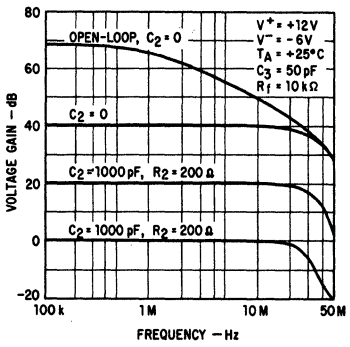
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



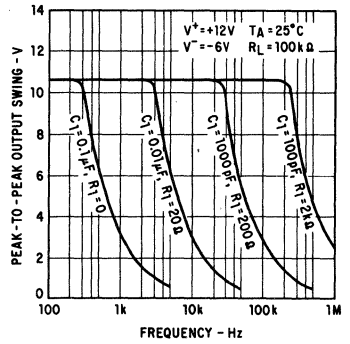
FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK



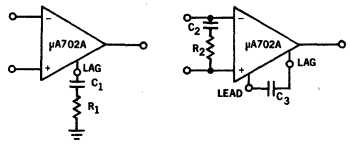
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS

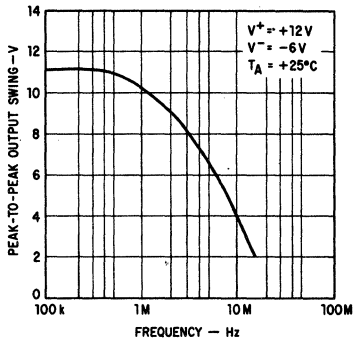


FREQUENCY COMPENSATION CIRCUITS
(Refer to Fairchild APP-117 for further details.)



LAG COMPENSATION **LEAD-LAG COMPENSATION**

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY WITH LEAD-LAG COMPENSATION



μA702B

HIGH GAIN, WIDEBAND DC AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **5 mV MAXIMUM OFFSET VOLTAGE**
- **2000 MINIMUM VOLTAGE GAIN**
- **20 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

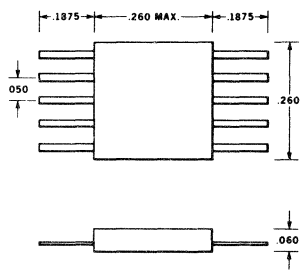
GENERAL DESCRIPTION — The μA702B is a complete DC amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for use as an operational amplifier in miniaturized analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from DC to 30 MHz.

For improved specifications, see μA702A data sheet.

ABSOLUTE MAXIMUM RATINGS

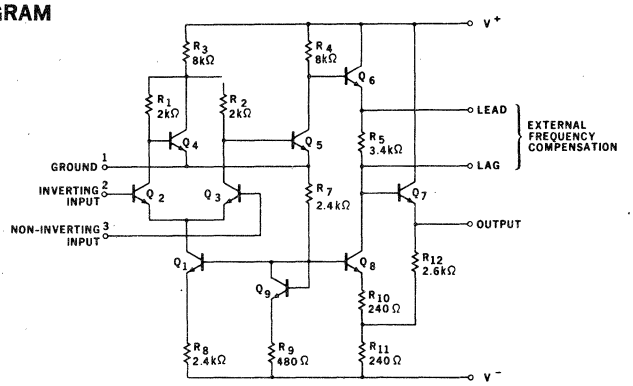
Voltage Between V^+ and V^- Terminals	21 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	+1.5 V to −6.0 V
Internal Power Dissipation (Note 1)	200 mW
Operating Temperature Range	−55° C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)

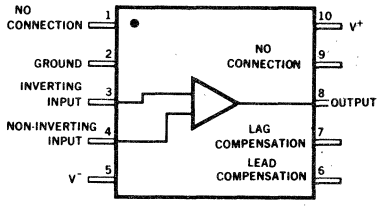


ORDER PART NO.
U3H7702313

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



(TOP VIEW)

NOTE 1: Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

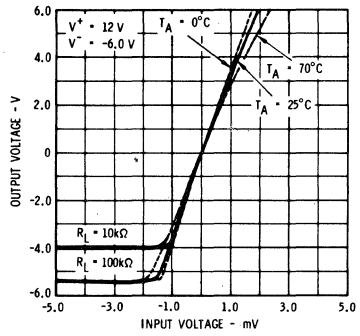
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

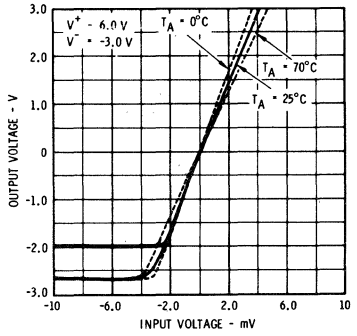
PARAMETER (see definitions)	CONDITIONS	V^+ = 12.0 V, V^- = −6.0 V MIN.	TYP.	MAX.	V^+ = 6.0 V, V^- = −3.0 V MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 2\ k\Omega$		1.5	5.0		1.7	6.0	mV
Input Offset Current			0.5	2.0		0.3	2.0	μA
Input Bias Current			2.5	7.5		1.5	5.0	μA
Input Resistance		10	32		16	55		kΩ
Input Voltage Range		−4.0		+0.5	−1.5		+0.5	V
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, $f \leq 1$ kHz	70	92		70	92		dB
Large-Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 5.0$ V	2000	3400	6000				
	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 2.5$ V				500	800	1500	
Output Resistance			200	600		300	800	Ω
Supply Current	$V_{out} = 0$		5.0	6.7		2.1	3.3	mA
Power Consumption	$V_{out} = 0$		90	120		19	30	mW
Transient Response (unity gain)	$C_1 = 0.01\ \mu F$, $R_1 = 20\Omega$, $R_L \leq 100\ k\Omega$, $V_{in} = 10$ mV							
Risetime			25	120				ns
Overshoot	$C_L \leq 100$ pF		10	50				%
Transient Response (×100 gain)	$C_3 = 50$ pF, $R_L \geq 100\ k\Omega$, $V_{in} = 1$ mV							
Risetime			10	30				ns
Overshoot			20	40				%
The following specifications apply for 0°C ≤ T_A ≤ +70°C:								
Input Offset Voltage	$R_S \leq 2\ k\Omega$			6.5			7.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\ \Omega$, $T_A = +70°C$ to $T_A = 0°C$		5.0	20		7.5	25	μV/°C
Input Offset Current				2.5			2.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +70°C$		4.0	10		3.0	8.0	nA/°C
	$T_A = 25°C$ to $T_A = 0°C$		6.0	20		5.5	18	nA/°C
Input Bias Current	$T_A = 0°C$		4.0	12		2.7	8	μA
Input Resistance		6.0	18		9.0	27		kΩ
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, $f \leq 1$ kHz	65	86		65	86		dB
Supply Voltage Rejection Ratio	$V^+ = 12$ V, $V^- = 6$ V to $V^+ = 6$ V, $V^- = 3$ V, $R_S \leq 2\ k\Omega$		90	300		90	300	μV/V
Large-Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 5.0$ V	1500		7000				
	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 2.5$ V				400		1750	
The following specifications apply for −55°C ≤ T_A ≤ +125°C:								
Input Offset Voltage	$R_S \leq 2\ k\Omega$			7.5			8.0	mV
Input Offset Current	$T_A = +125°C$		0.2	2.0		0.14	2.0	μA
	$T_A = -55°C$		1.2	4.0		0.8	4.0	μA
Input Bias Current	$T_A = -55°C$		5.5	20		3.4	15	μA
Input Resistance		3.0			4.0			kΩ
Common Mode Rejection Ratio	$R_S \leq 2\ k\Omega$, $f \leq 1$ kHz	60	80		60	80		dB
Large Signal Voltage Gain	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 5.0$ V	1200						
	$R_L \geq 100\ k\Omega$, $V_{out} = \pm 2.5$ V				300			
Output Voltage Swing	$R_L \geq 100\ k\Omega$	±5.0	±5.3		±2.5	±2.7		V
	$R_L \geq 10\ k\Omega$	±3.5	±4.0		±1.5	±2.0		V
Supply Current	$T_A = +125°C$, $V_{out} = 0$		4.4	6.7		1.7	3.3	mA
	$T_A = -55°C$, $V_{out} = 0$		5.0	7.5		2.1	3.9	mA
Power Consumption	$T_A = +125°C$, $V_{out} = 0$		80	120		15	30	mW
	$T_A = -55°C$, $V_{out} = 0$		90	135		19	35	mW

TYPICAL PERFORMANCE CURVES

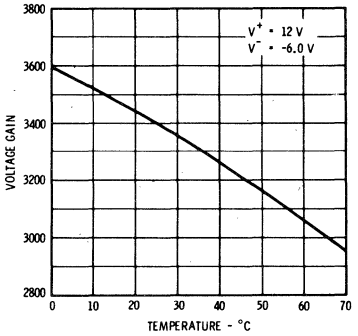
VOLTAGE TRANSFER CHARACTERISTIC



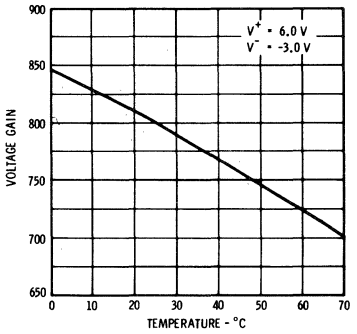
VOLTAGE TRANSFER CHARACTERISTIC



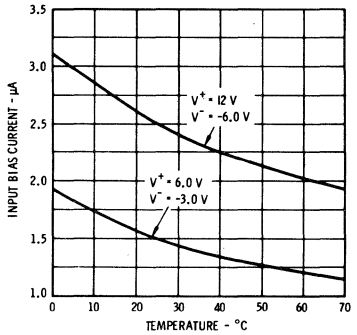
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



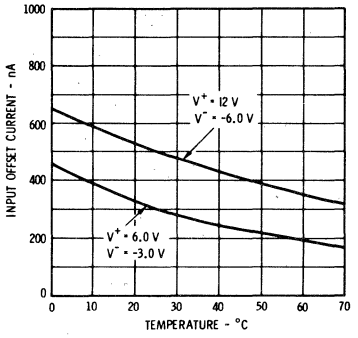
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



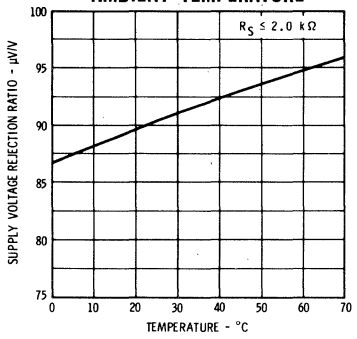
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



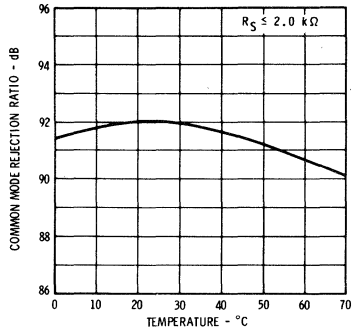
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



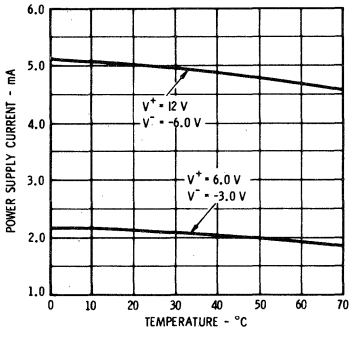
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



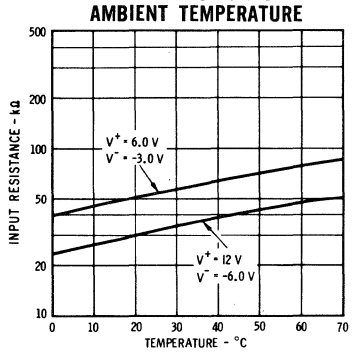
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



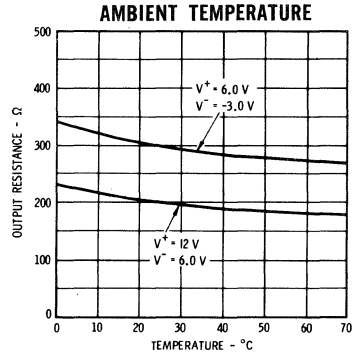
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



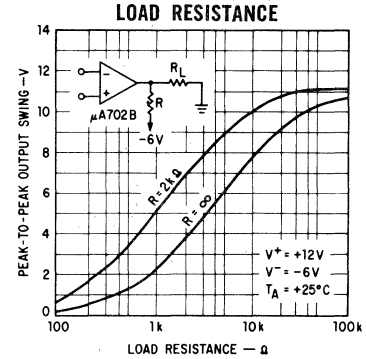
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

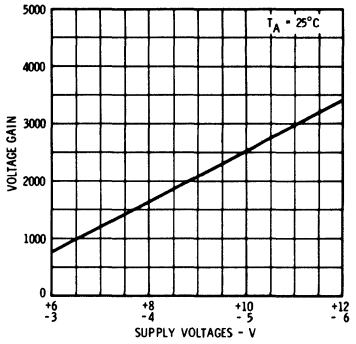


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

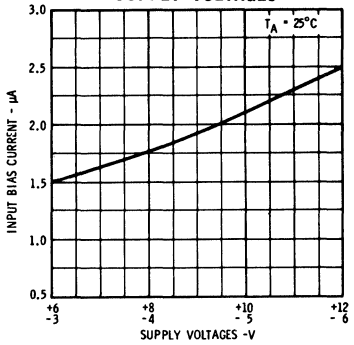


TYPICAL PERFORMANCE CURVES

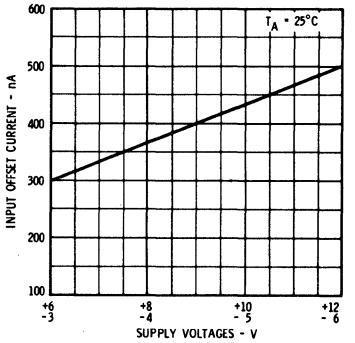
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



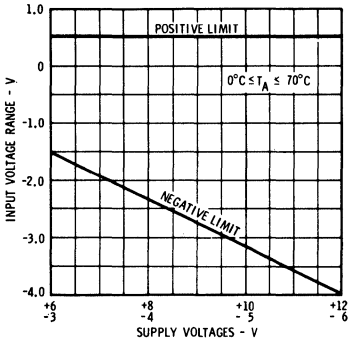
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



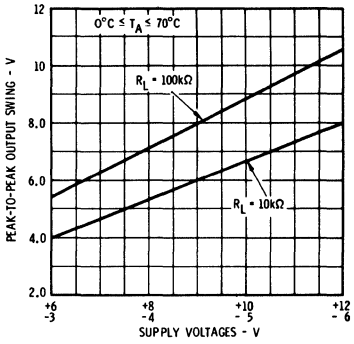
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



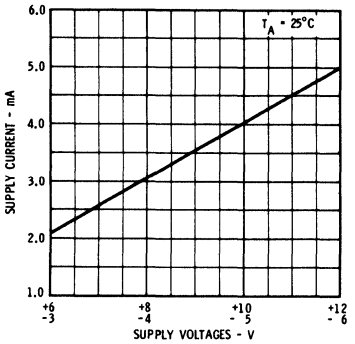
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES



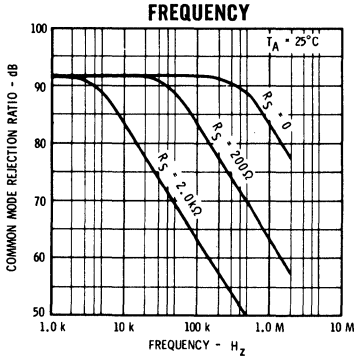
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES



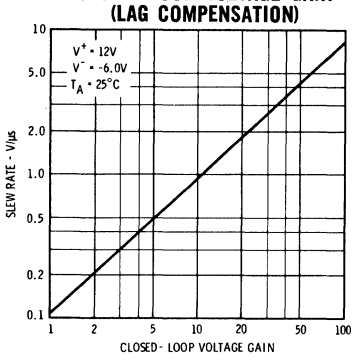
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



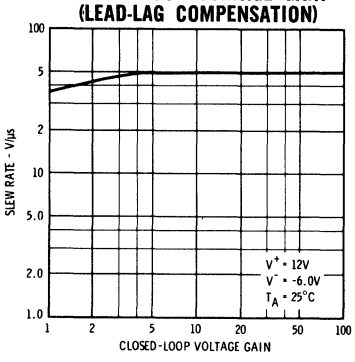
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)

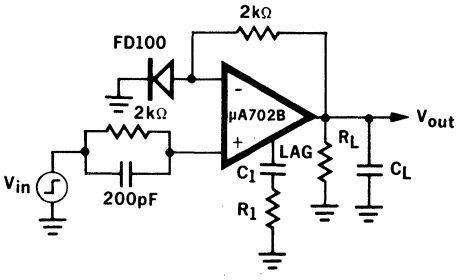


SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)

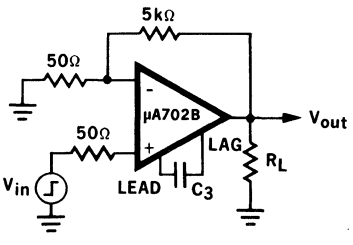


TRANSIENT RESPONSE TEST CIRCUITS

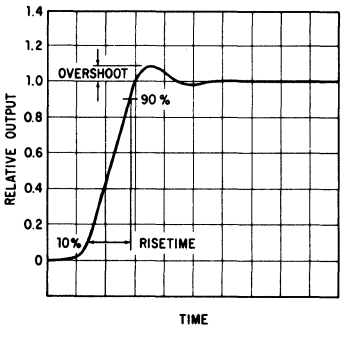
UNITY-GAIN AMPLIFIER (LAG COMPENSATION)



X100 AMPLIFIER (LEAD COMPENSATION)



TRANSIENT RESPONSE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

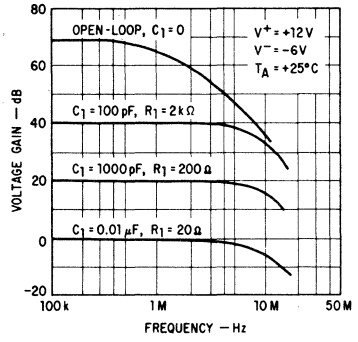
POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

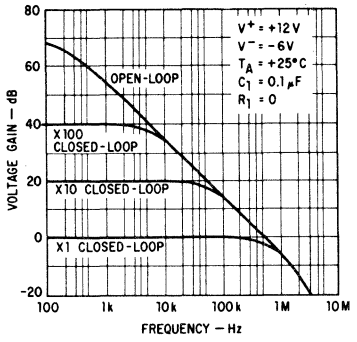
PEAK OUTPUT CURRENT — The maximum current that may flow in the output load without causing damage to the unit.

TYPICAL PERFORMANCE CURVES

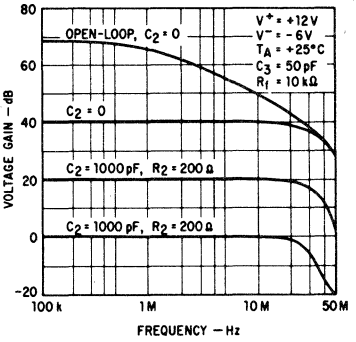
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



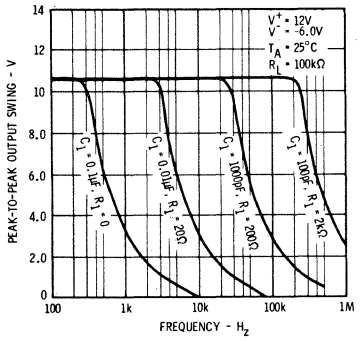
FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK



FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)

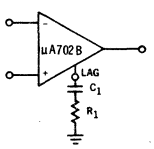


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS

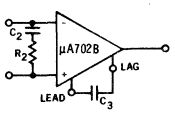


FREQUENCY COMPENSATION CIRCUITS

(Refer to Fairchild APP-117 for further details)

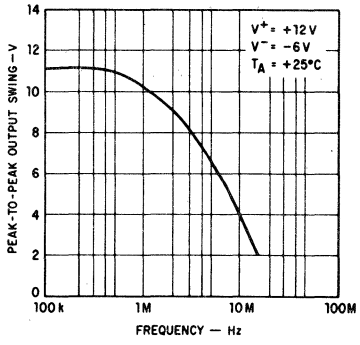


LAG COMPENSATION



LEAD-LAG COMPENSATION

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY WITH LEAD-LAG COMPENSATION



μA702C

HIGH GAIN, WIDEBAND DC AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **IMPROVED SPECIFICATIONS**
- **5 mV MAXIMUM OFFSET VOLTAGE**
- **2000 MINIMUM VOLTAGE GAIN**
- **20 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

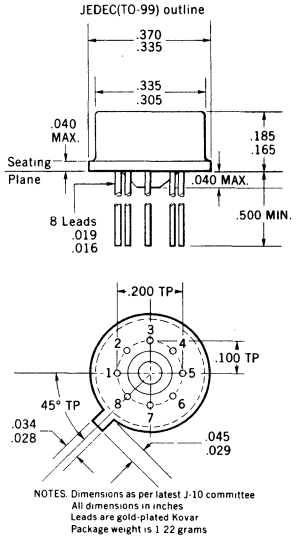
GENERAL DESCRIPTION — The μA702C is a complete DC amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for use as an operational amplifier in miniaturized analog computers, as a precision instrumentation amplifier, or in other applications requiring a feedback amplifier useful from DC to 30 MHz.

For full temperature range operation (−55°C to +125°C) see μA702A data sheet.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	21 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	+1.5 V to −6.0 V
Internal Power Dissipation [Note 1]	
TO-99	300 mW
Flat Package	200 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

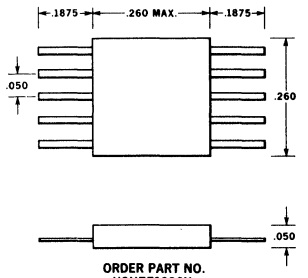
PHYSICAL DIMENSIONS
in accordance with
JEDEC(TO-99) outline



NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

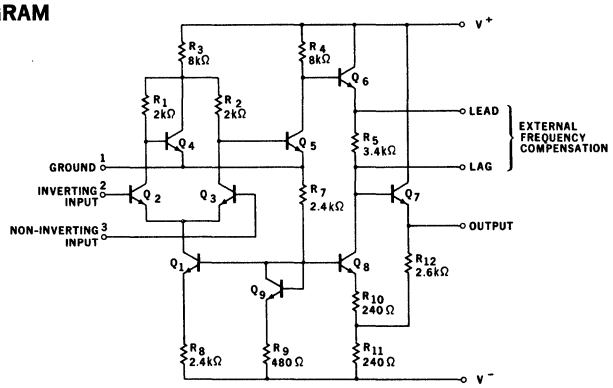
ORDER PART NO.U5B771239X

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)

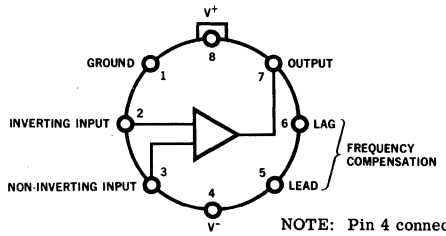


ORDER PART NO.
U3H771239X

SCHEMATIC DIAGRAM

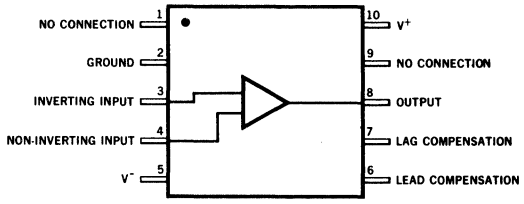


TO-99 CONNECTION DIAGRAM (TOP VIEW)



NOTE: Pin 4 connected to can.

FLAT PACKAGE CONNECTION DIAGRAM (TOP VIEW)



NOTE 1: Rating applies for ambient temperatures to +70°C.

* Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

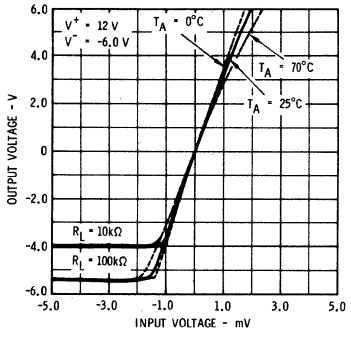
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

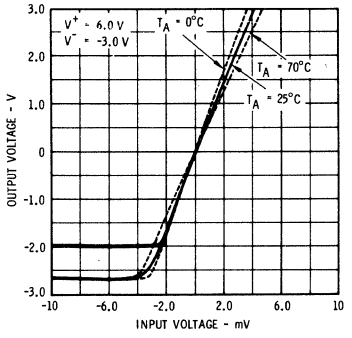
PARAMETER (see definitions)	CONDITIONS	V^+ = 12.0 V, V^- = −6.0 V MIN.	TYP.	MAX.	V^+ = 6.0 V, V^- = −3.0 V MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 2$ kΩ		1.5	5.0		1.7	6.0	mV
Input Offset Current			0.5	2.0		0.3	2.0	μA
Input Bias Current			2.5	7.5		1.5	5.0	μA
Input Resistance		10	32		16	55		kΩ
Input Voltage Range		−4.0		+0.5	−1.5		+0.5	V
Common Mode Rejection Ratio	$R_S \leq 2$ kΩ, $f \leq 1$ kHz	70	92		70	92		dB
Large-Signal Voltage Gain	$R_L \geq 100$ kΩ, $V_{out} = \pm 5.0$ V	2000	3400	6000				
	$R_L \geq 100$ kΩ, $V_{out} = \pm 2.5$ V				500	800	1500	
Output Resistance			200	600		300	800	Ω
Supply Current	$V_{out} = 0$		5.0	6.7		2.1	3.3	mA
Power Consumption	$V_{out} = 0$		90	120		19	30	mW
Transient Response (unity gain)	$C_l = 0.01$ μF, $R_l = 20$Ω, $R_L \leq 100$ kΩ, $V_{in} = 10$ mV							
Risetime			25	120				ns
Overshoot	$C_L \leq 100$ pF		10	50				%
Transient Response (×100 gain)	$C_3 = 50$ pF, $R_L \geq 100$ kΩ, $V_{in} = 1$ mV							
Risetime			10	30				ns
Overshoot			20	40				%
The following specifications apply for 0°C ≤ T_A ≤ +70°C:								
Input Offset Voltage	$R_S \leq 2$ kΩ			6.5			7.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50$ Ω, $T_A = +70$°C to $T_A = 0$°C		5.0	20		7.5	25	μV/°C
Input Offset Current				2.5			2.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25$°C to $T_A = +70$°C		4.0	10		3.0	8.0	nA/°C
	$T_A = 25$°C to $T_A = 0$°C		6.0	20		5.5	18	nA/°C
Input Bias Current	$T_A = 0$°C		4.0	12		2.7	8	μA
Input Resistance		6.0	18		9.0	27		kΩ
Common Mode Rejection Ratio	$R_S \leq 2$ kΩ, $f \leq 1$ kHz	65	86		65	86		dB
Supply Voltage Rejection Ratio	$V^+ = 12$ V, $V^- = 6$ V to $V^+ = 6$ V, $V^- = 3$ V, $R_S \leq 2$ kΩ		90	300		90	300	μV/V
Large-Signal Voltage Gain	$R_L \geq 100$ kΩ, $V_{out} = \pm 5.0$ V	1500		7000				
	$R_L \geq 100$ kΩ, $V_{out} = \pm 2.5$ V				400		1750	
Output Voltage Swing	$R_L \geq 100$ kΩ	±5.0	±5.3		±2.5	±2.7		V
	$R_L \geq 10$ kΩ	±3.5	±4.0		±1.5	±2.0		V
Supply Current	$V_{out} = 0$		5.0	7.0		2.1	3.9	mA
Power Consumption	$V_{out} = 0$		90	125		19	35	mW

TYPICAL PERFORMANCE CURVES

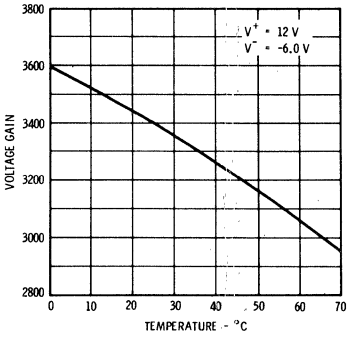
VOLTAGE TRANSFER CHARACTERISTIC



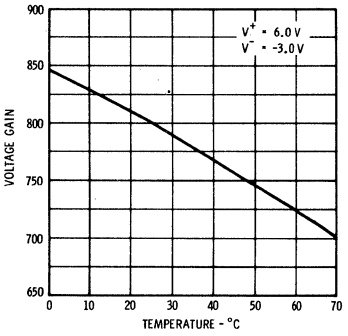
VOLTAGE TRANSFER CHARACTERISTIC



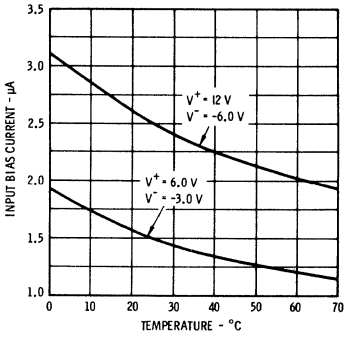
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



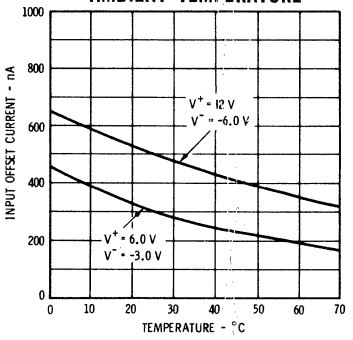
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



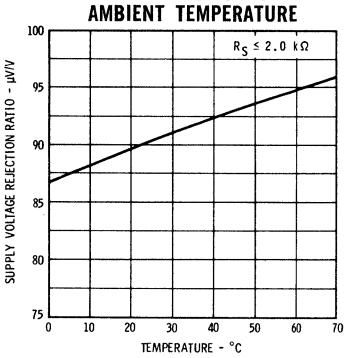
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



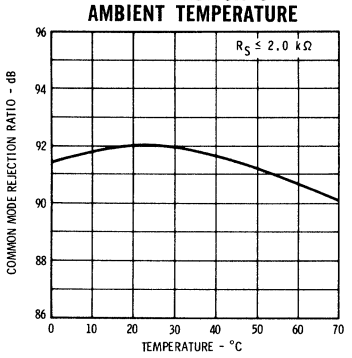
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



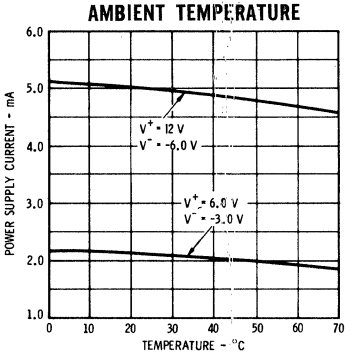
SUPPLY VOLTAGE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



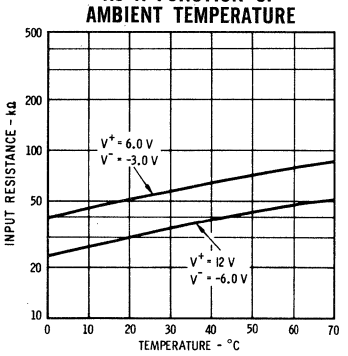
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



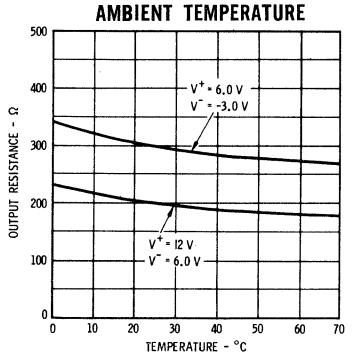
POWER SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



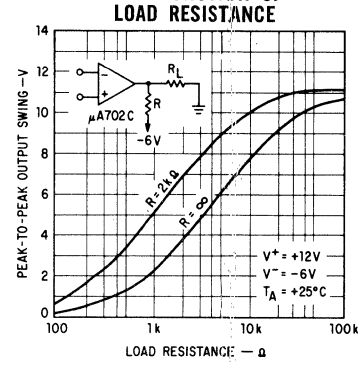
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

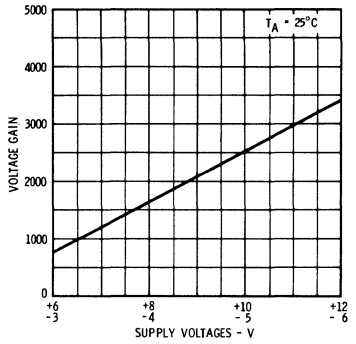


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

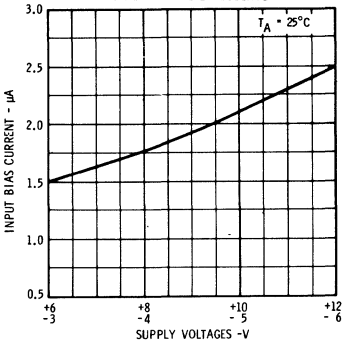


TYPICAL PERFORMANCE CURVES

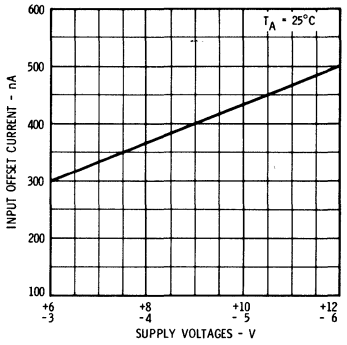
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



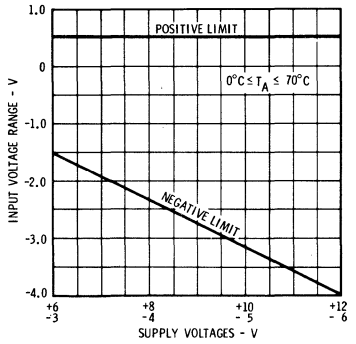
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



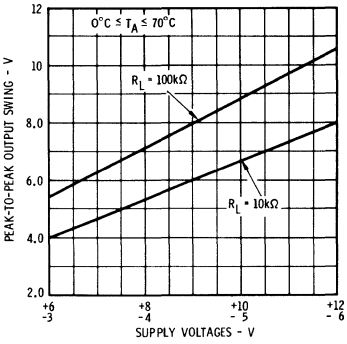
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



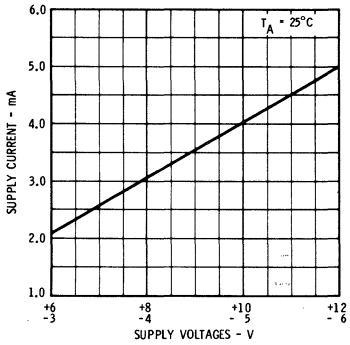
INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGES



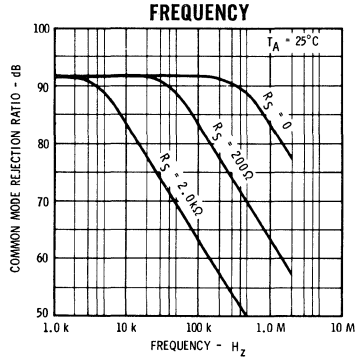
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGES



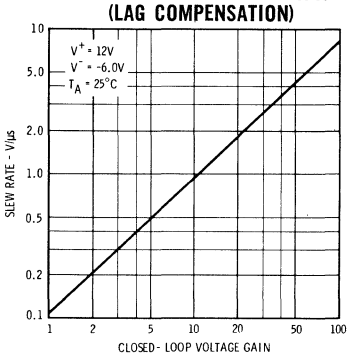
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGES



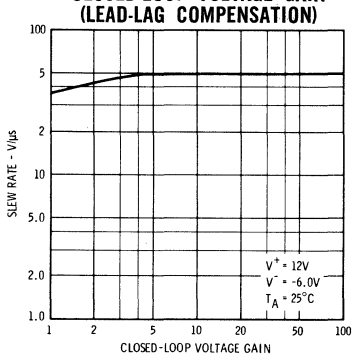
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LAG COMPENSATION)

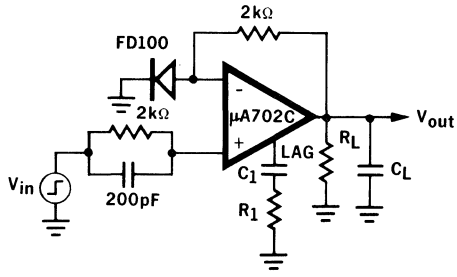


SLEW RATE AS A FUNCTION OF CLOSED-LOOP VOLTAGE GAIN (LEAD-LAG COMPENSATION)

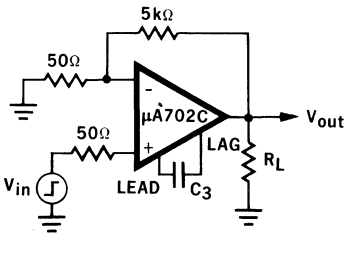


TRANSIENT RESPONSE TEST CIRCUITS

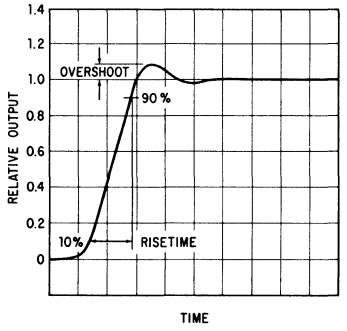
UNITY-GAIN AMPLIFIER (LAG COMPENSATION)



X100 AMPLIFIER (LEAD COMPENSATION)



TRANSIENT RESPONSE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

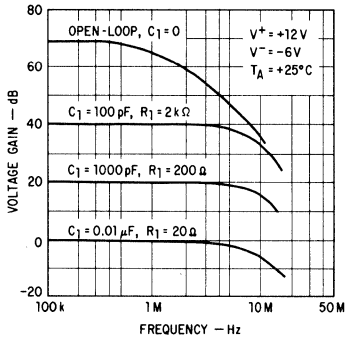
POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

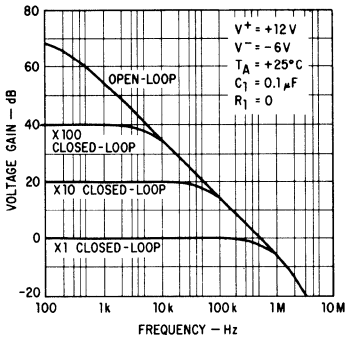
PEAK OUTPUT CURRENT — The maximum current that may flow in the output load without causing damage to the unit.

TYPICAL PERFORMANCE CURVES

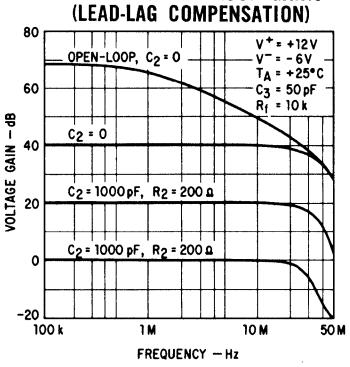
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LAG COMPENSATION)



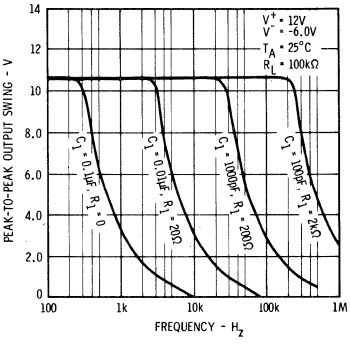
FREQUENCY RESPONSE WITH CONSERVATIVE COMPENSATION NETWORK



FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS (LEAD-LAG COMPENSATION)

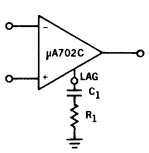


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS LAG COMPENSATION NETWORKS

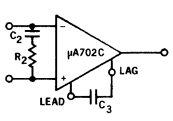


FREQUENCY COMPENSATION CIRCUITS

(Refer to Fairchild APP-117 for further details)

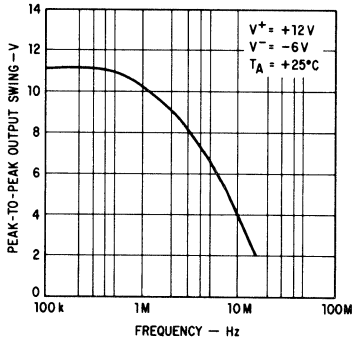


LAG COMPENSATION



LEAD-LAG COMPENSATION

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY WITH LEAD-LAG COMPENSATION



μA703

RF-IF AMPLIFIER

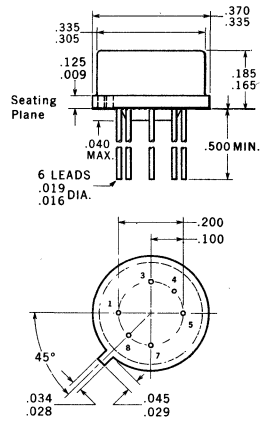
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The μA703 is an RF-IF amplifier constructed on a single silicon chip and is intended for use as a limiting or nonlimiting amplifier, harmonic mixer, or oscillator to 150 MHz. The low internal feedback of the device insures a higher stability-limited gain than that available from conventional circuitry. Including the biasing network in the same package reduces the number of external components required, thereby increasing the reliability and versatility of the device.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	20 V
Output Collector Voltage	24 V
Voltage Between Input Terminals	±5.0 V
Internal Power Dissipation (Note 1)	200 mW
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering - 60 seconds)	300°C

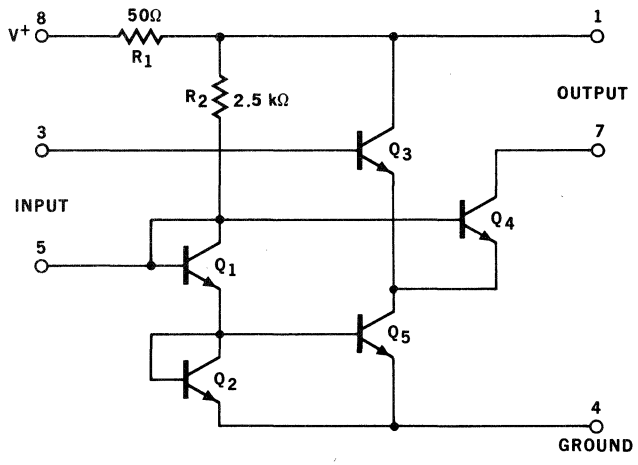
PHYSICAL DIMENSIONS
(in accordance with JEDEC TO-99 outline)



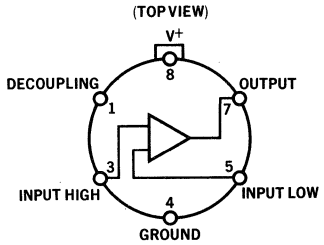
NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.27 grams

ORDER PART NO. U5D770331X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



NOTE: Pin 4 connected to case.

NOTE 1: Rating applies for ambient temperatures to 125°C.

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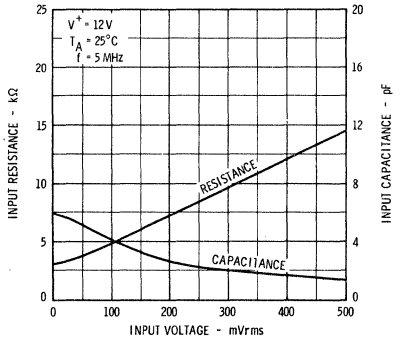
FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12 V unless otherwise specified)

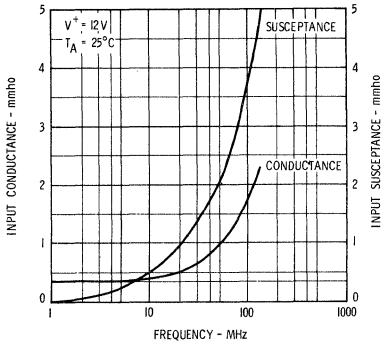
Parameter	Conditions	Min.	Typ.	Max.	Units
Power Consumption	e_{in} = 0		110	170	mW
Quiescent Output Current	e_{in} = 0	2.1	2.5	3.1	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms, f = 1 kHz	4.0			mA
Output Saturation Voltage				1.7	V
Forward Transadmittance	e_{in} = 10 mV rms, f ≤ 5 MHz	29	35		mmho
Input Conductance	e_{in} < 10 mV rms, f ≤ 5 MHz		0.30	0.43	mmho
Input Capacitance	e_{in} < 10 mV rms, f ≤ 5 MHz		7.0	9.0	pF
Output Capacitance	f ≤ 5 MHz		2.0	3.0	pF
Output Conductance	f ≤ 5 MHz		0.02	0.04	mmho
Noise Figure	f = 30 MHz, R_s = 500 Ω		6.5		dB
	f = 100 MHz, R_s = 500 Ω		8.0		dB
The following specifications apply for -55°C ≤ T_A ≤ +125°C					
Quiescent Output Current	e_{in} = 0	1.7		3.1	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms, f = 1 kHz	3.2			mA
Output Saturation Voltage				1.8	V
Forward Transadmittance	e_{in} = 10 mV rms, f ≤ 5 MHz	21			mmho
Input Conductance	e_{in} < 10 mV rms, f ≤ 5 MHz			1.2	mmho
Output Conductance	f ≤ 5 MHz			0.05	mmho

TYPICAL PERFORMANCE CURVES

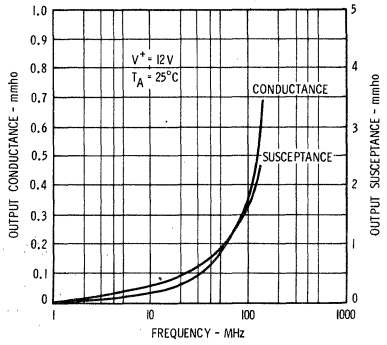
INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE



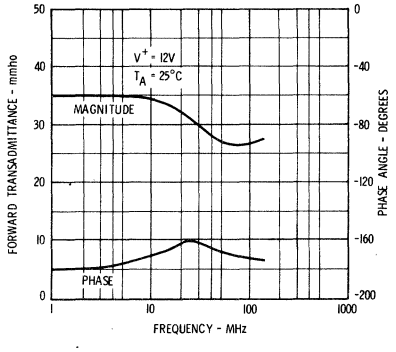
INPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



OUTPUT ADMITTANCE AS A FUNCTION OF FREQUENCY

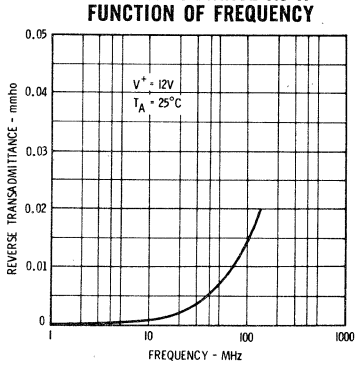


FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY

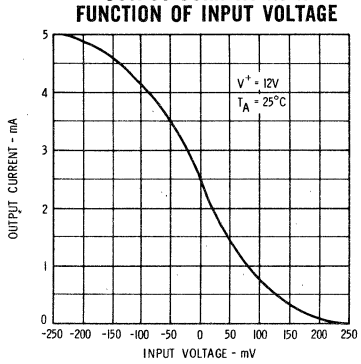


TYPICAL PERFORMANCE CURVES

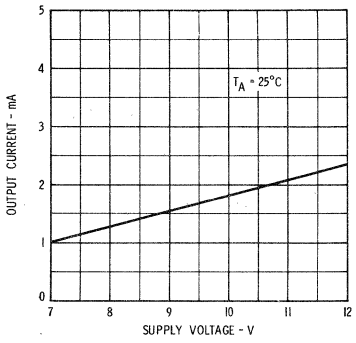
MAXIMUM REVERSE TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



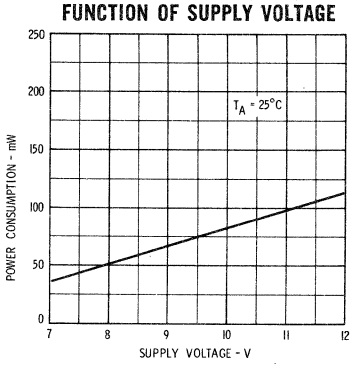
OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



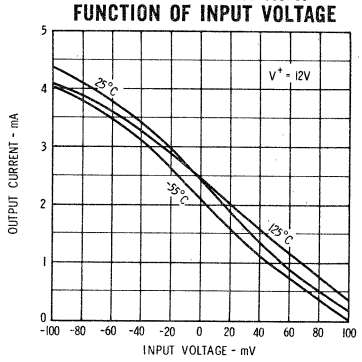
OUTPUT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



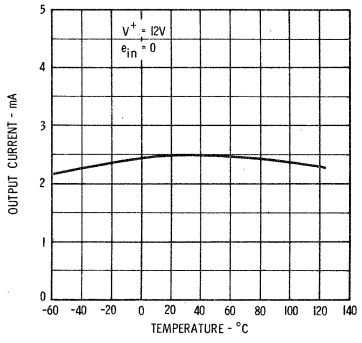
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



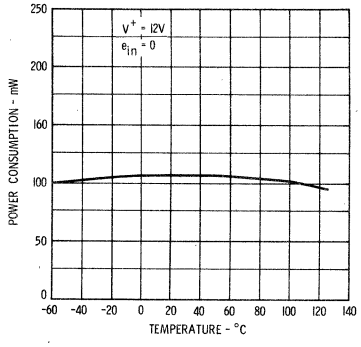
OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



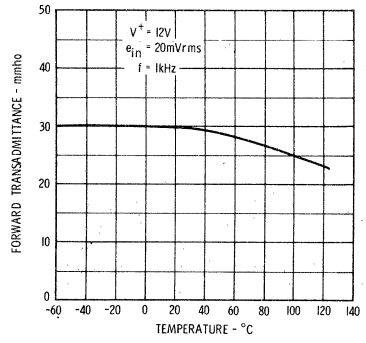
OUTPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



TRANSADMITTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



DEFINITION OF TERMS

POWER CONSUMPTION - The DC power required to operate the device with no signal applied.

QUIESCENT OUTPUT CURRENT - The DC current delivered to the load with the input terminals short-circuited.

PEAK-TO-PEAK OUTPUT CURRENT - The short-circuit output current excursion for a large-signal input voltage.

OUTPUT SATURATION VOLTAGE - The minimum voltage to which the output collector may be reduced without degrading circuit performance.

TRANSADMITTANCE - The ratio of the output current to the input voltage.

INPUT ADMITTANCE - The admittance between the input terminals with the output short-circuited.

OUTPUT ADMITTANCE - The admittance between the output terminals with the input short-circuited.

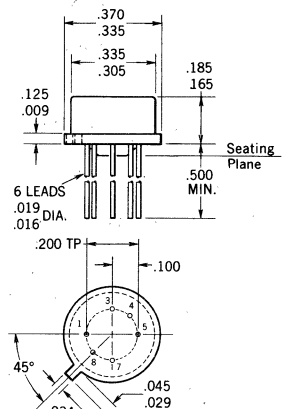
μA703C
RF-IF AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The μA703C is an RF-IF amplifier constructed on a single silicon chip and is intended for use as a limiting or non-limiting amplifier, harmonic mixer, or oscillator to 150 MHz. The low internal feedback of the device insures a higher stability-limited gain than that available from conventional circuitry. Including the biasing network in the same package reduces the number of external components required, thereby increasing the reliability and versatility of the device. For full range operation (-55°C to +125°C) see μA703 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	20 V
Output Collector Voltage	24 V
Voltage Between Input Terminals	±5.0 V
Internal Power Dissipation (Note 1)	200 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering - 60 second)	300°C

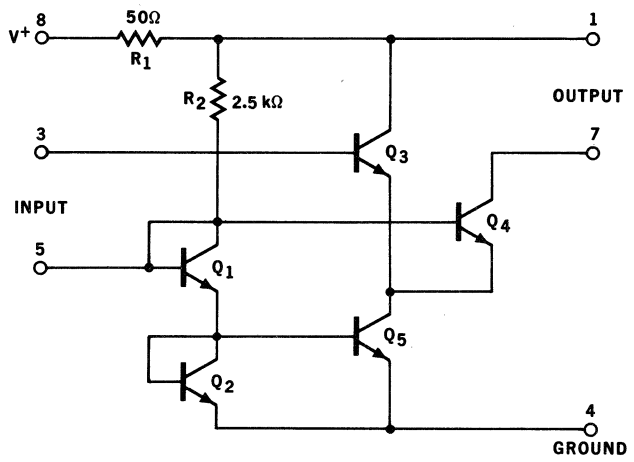
PHYSICAL DIMENSIONS



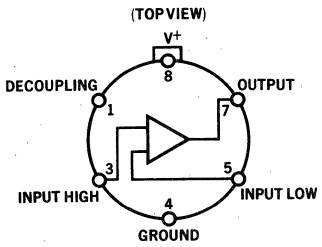
NOTES: All dimensions in inches
Dimensions as per latest J-10 committee
Weight is 1.27 grams

ORDER PART NO. U5D770339X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



NOTE: Pin 4 connected to case.

NOTE 1: Rating applies for ambient temperatures to 70°C.

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FAIRCHILD SEMICONDUCTOR
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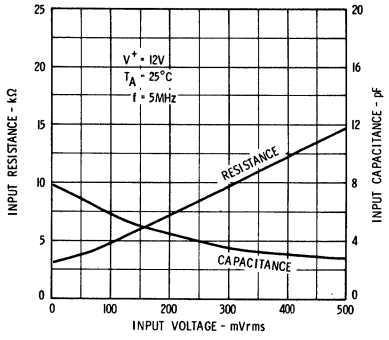
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12 V unless otherwise specified)

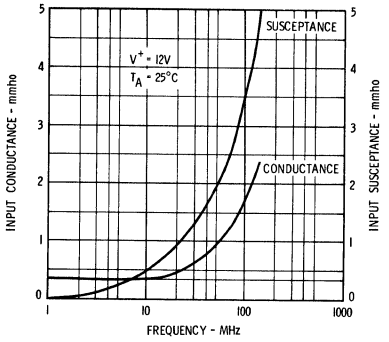
Parameter	Conditions	Min.	Typ.	Max.	Units
Power Consumption	e_{in} = 0		110	170	mW
Quiescent Output Current	e_{in} = 0	1.9	2.5	3.3	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms, f = 1 kHz	3.6			mA
Output Saturation Voltage				1.7	V
Forward Transadmittance	e_{in} = 10 mV rms, f $\leq$ 5 MHz	23	33		mmho
Input Conductance	e_{in} < 10 mV rms, f $\leq$ 5 MHz		0.35	0.50	mmho
Input Capacitance	e_{in} < 10 mV rms, f $\leq$ 5 MHz		9.0	11.0	pF
Output Capacitance	f $\leq$ 5 MHz		2.0	3.0	pF
Output Conductance	f $\leq$ 5 MHz			0.05	mmho
Noise Figure	f = 30 MHz, R_S = 500 Ω		6.5		dB
	f = 100 MHz, R_S = 500 Ω		8.0		dB
The following specifications apply for 0°C $\leq T_A \leq$ 70°C:					
Quiescent Output Current	e_{in} = 0	1.7		3.5	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms, f = 1 kHz	3.2			mA
Output Saturation Voltage				1.8	V
Forward Transadmittance	e_{in} = 10 mV rms, f $\leq$ 5 MHz	22			mmho
Input Conductance	e_{in} < 10 mV rms, f $\leq$ 5 MHz			0.71	mmho
Output Conductance	f $\leq$ 5 MHz			0.06	mmho

TYPICAL PERFORMANCE CURVES

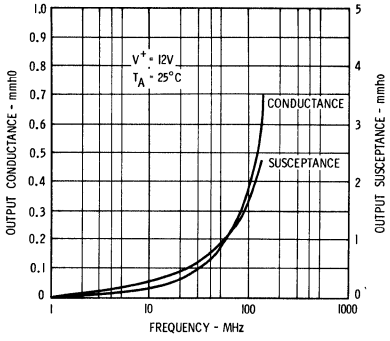
INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE



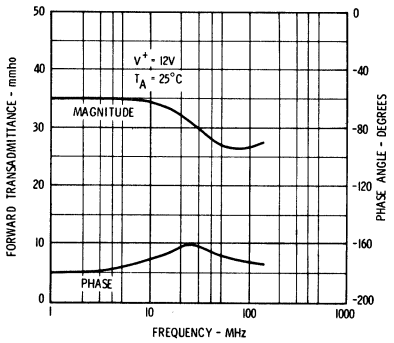
INPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



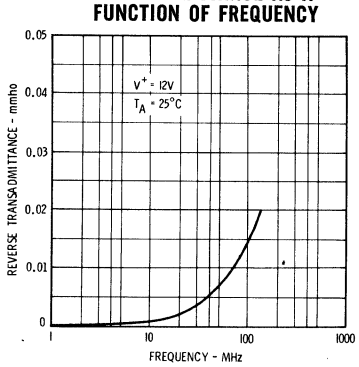
OUTPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



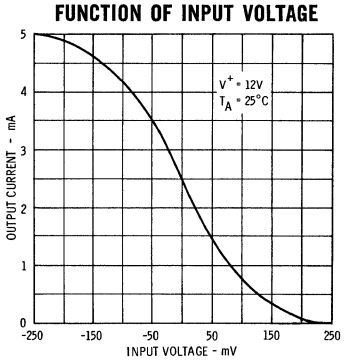
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



MAXIMUM REVERSE TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE



μA703E
RF-IF AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

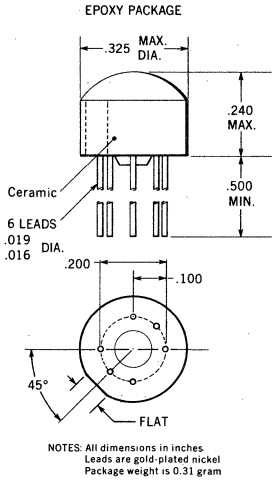
GENERAL DESCRIPTION - The μA703E is a linear integrated circuit with useful unneutralized power gain to frequencies in excess of 100 MHz. It features the capability of nonsaturating limiter operation with a suitable output load, making it ideally suited for FM-IF limiter applications.

Applications include FM-IF limiter-amplifier, TV sound IF amplifier, chroma reference oscillator for color TV, and fixed-gain amplifiers to 100 MHz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	20 V
Output Collector Voltage	24 V
Voltage Between Input Terminals	±5.0 V
Internal Power Dissipation (Note 1)	200 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering - 60 seconds)	300°C

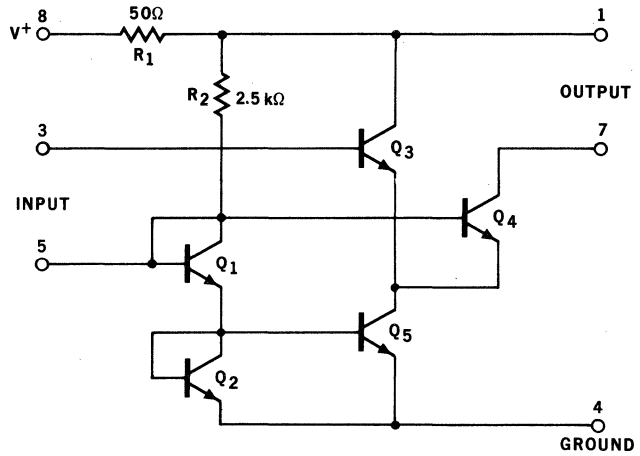
PHYSICAL DIMENSIONS



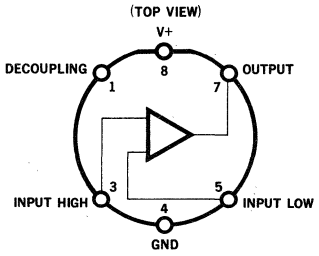
NOTES: All dimensions in inches.
Leads are gold-plated nickel
Package weight is 0.31 gram

ORDER PART NO. U8B7703394

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



NOTE 1: Rating applies for ambient temperatures to +70°C.

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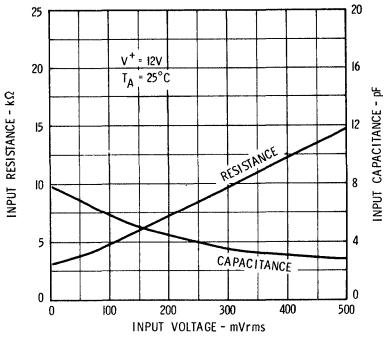
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12 V, f = 10.7 MHz unless otherwise specified)

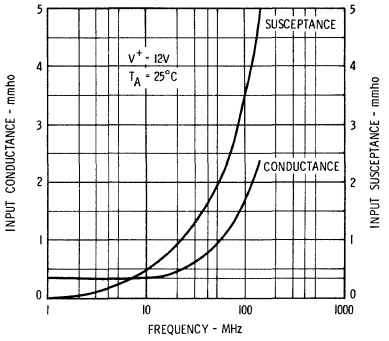
Parameter	Conditions	Min.	Typ.	Max.	Units
Power Consumption	e_{in} = 0		110	170	mW
Quiescent Output Current			2.5	3.3	mA
Peak-to-Peak Output Current	e_{in} = 400 mV rms	3.0	5.0		mA
Output Saturation Voltage			1.4	1.7	Volts
Forward Transadmittance	e_{in} = 10 mV rms	24	35		mmhos
Reverse Transadmittance			0.002		mmho
Input Conductance	e_{in} < 10 mV rms		.33	1.0	mmho
Input Capacitance	e_{in} < 10 mV rms		9.0	12.5	pF
Output Conductance			0.03	0.05	mmho
Output Capacitance			2.6	4.0	pF
Noise Figure	R_S = 500 Ω		6.0		dB
	R_S = 500 Ω, f = 100 MHz		8.0		dB
Maximum Stable Gain			40		dB

TYPICAL PERFORMANCE CURVES

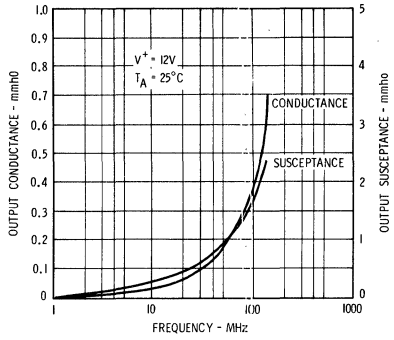
INPUT RESISTANCE AND CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE



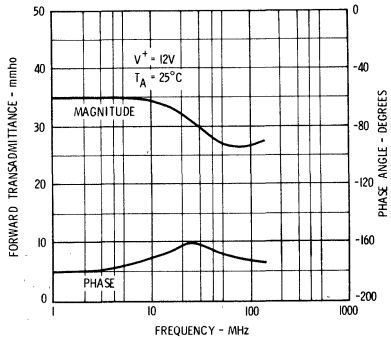
INPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



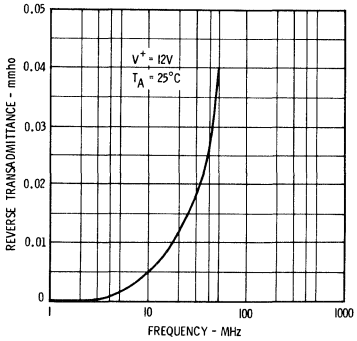
OUTPUT ADMITTANCE AS A FUNCTION OF FREQUENCY



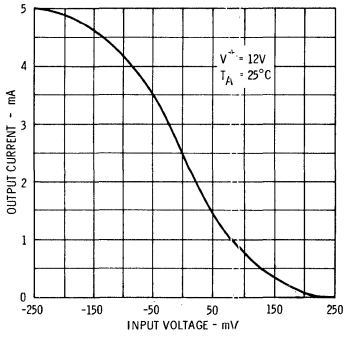
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



MAXIMUM REVERSE TRANSADMITTANCE AS A FUNCTION OF FREQUENCY

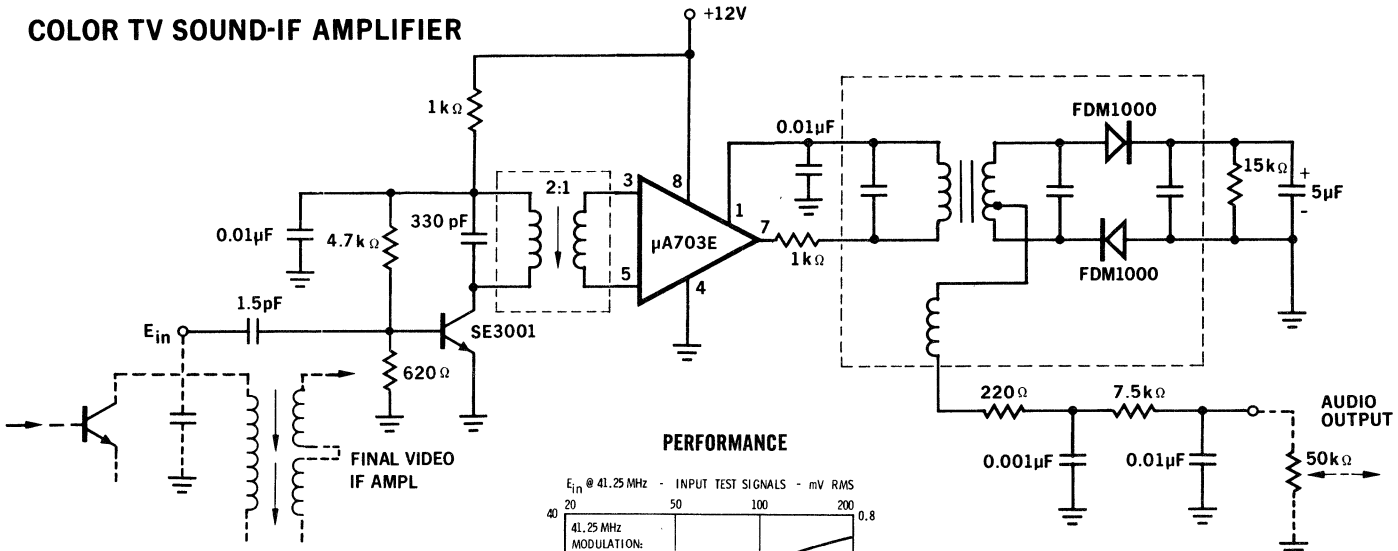


OUTPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

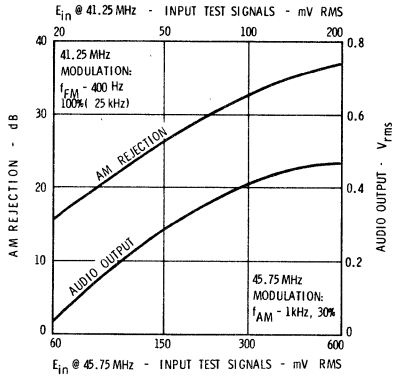


TYPICAL CIRCUIT APPLICATIONS

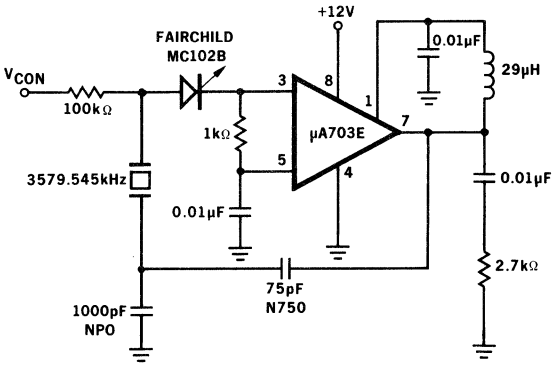
COLOR TV SOUND-IF AMPLIFIER



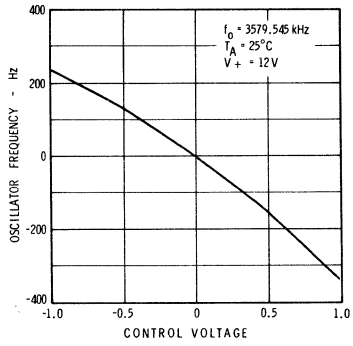
PERFORMANCE



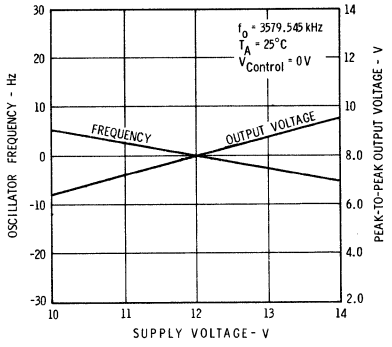
3.58-MHz VOLTAGE-CONTROLLED OSCILLATOR



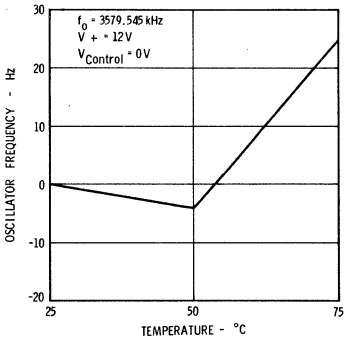
NORMALIZED OSCILLATOR FREQUENCY AS A FUNCTION OF CONTROL VOLTAGE



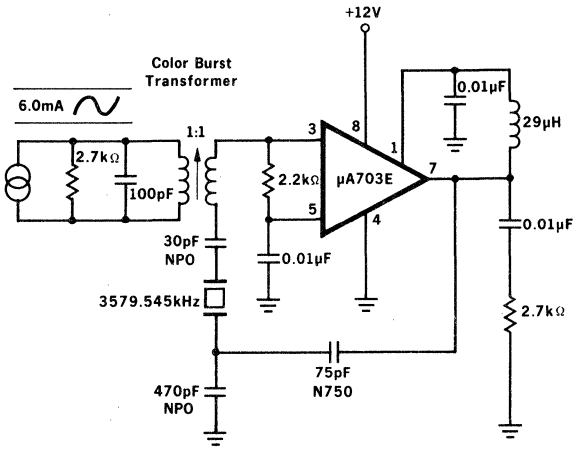
NORMALIZED OSCILLATOR FREQUENCY AND OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



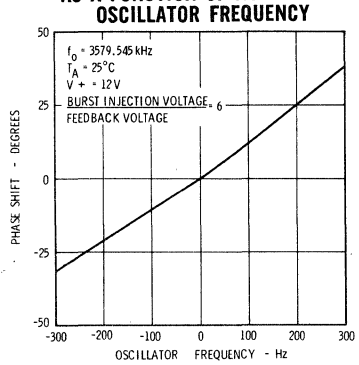
NORMALIZED OSCILLATOR FREQUENCY AS A FUNCTION OF AMBIENT TEMPERATURE



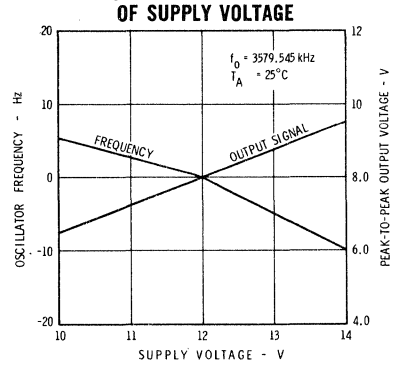
3.58-MHz INJECTION-LOCKED OSCILLATOR



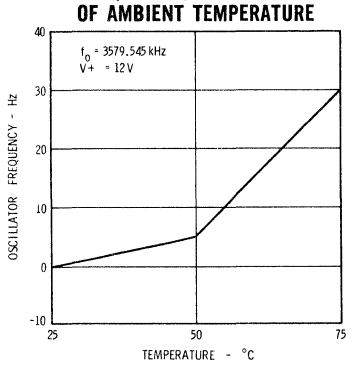
NORMALIZED PHASE SHIFT AS A FUNCTION OF NORMALIZED OSCILLATOR FREQUENCY



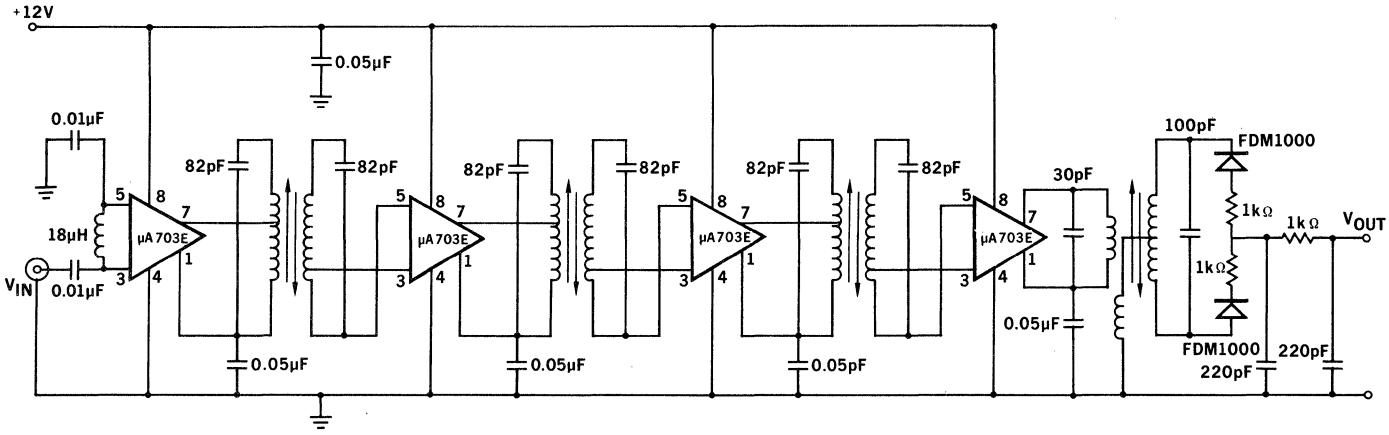
NORMALIZED OSCILLATOR FREQUENCY AND OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



NORMALIZED OSCILLATOR FREQUENCY AS A FUNCTION OF AMBIENT TEMPERATURE



FOUR-STAGE FM-IF AMPLIFIER



Full limiting with $V_{in} < 50\mu V$.

Current consumption 27 mA.

Power gain / stage 26.5 dB.

Peak-to-Peak separation of detector 800 kHz.

THD < 0.8% with ±75 kHz deviation @ 400 Hz.

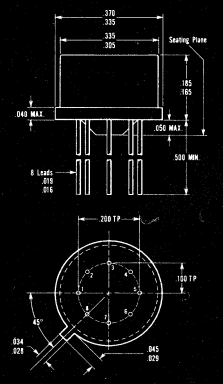
μA709

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTIONS - The μA709 is a high-gain operational amplifier constructed on a single silicon chip using the Fairchild Planar epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions.

PHYSICAL DIMENSIONS
(SIMILAR TO TO-5)



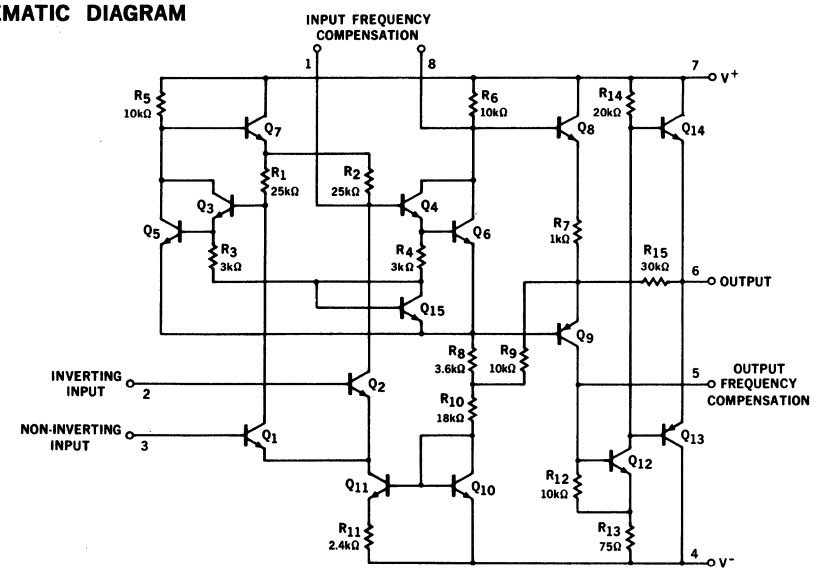
NOTES: Dimensions as per latest JS-10 committee.
All dimensions in inches.
Leads are gold-plated kovar.
Package weight is 1.12 grams.

ORDER PART NO.
U5B770931X

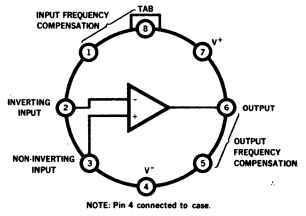
ABSOLUTE MAXIMUM RATINGS

Supply Voltage		± 18 V
Internal Power Dissipation	(Note 1)	300 mW
Differential Input Voltage		± 5.0 V
Input Voltage		± 10 V
Output Short-Circuit Duration	(T_A = 25°C)	5 sec
Storage Temperature Range		-65°C to + 150°C
Operating Temperature Range		-55°C to + 125°C
Lead Temperature (Soldering, 60 sec)		300°C

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



NOTE: Pin 4 connected to case.

(Top View)

NOTE 1: Rating applies for case temperatures to + 125°C; derate linearly at 5.6 mW/°C for ambient temperatures above + 95°C.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

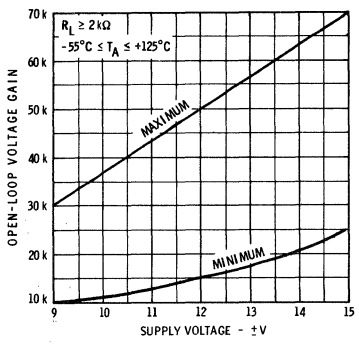
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (T_A = +25°C, ±9 V ≤ V_S ≤ ±15 V unless otherwise specified)

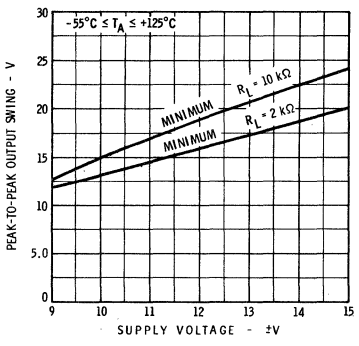
Parameter (see definitions)	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	$R_S \leq 10\,k\Omega$		1.0	5.0	mV
Input Offset Current			50	200	nA
Input Bias Current			200	500	nA
Input Resistance		150	400		kΩ
Output Resistance			150		Ω
Power Consumption	V_S = ±15 V		80	165	mW
Transient Response	V_{in} = 20 mV, R_L = 2 kΩ,				
Risetime	C_1 = 5000 pF, R_1 = 1.5 kΩ, C_2 = 200 pF, R_2 = 50 Ω		0.3	1.0	μs
Overshoot	$C_L \leq 100$ pF		10	30	%
The following specifications apply for -55°C ≤ T_A ≤ +125°C:					
Input Offset Voltage	$R_S \leq 10$ kΩ			6.0	mV
Average Temperature Coefficient of Input Offset Voltage	R_S = 50 Ω		3.0		μV/°C
	$R_S \leq 10$ kΩ		6.0		μV/°C
Large-Signal Voltage Gain	V_S = ±15 V, $R_L \geq 2$ kΩ, V_{out} = ±10 V	25,000	45,000	70,000	
Output Voltage Swing	V_S = ±15 V, $R_L \geq 10$ kΩ	±12	±14		V
	V_S = ±15 V, $R_L \geq 2$ kΩ	±10	±13		V
Input Voltage Range	V_S = ±15 V	±8.0	±10		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		25	150	μV/V
Input Offset Current	T_A = +125°C		20	200	nA
	T_A = -55°C		100	500	nA
Input Bias Current	T_A = -55°C		0.5	1.5	μA
Input Resistance		40	100		kΩ

GUARANTEED ELECTRICAL CHARACTERISTICS

VOLTAGE GAIN

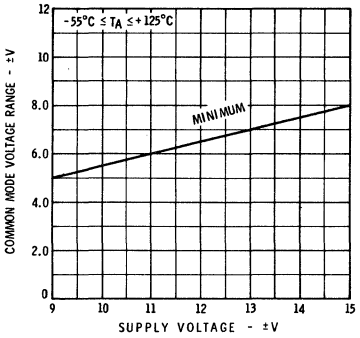


OUTPUT VOLTAGE SWING

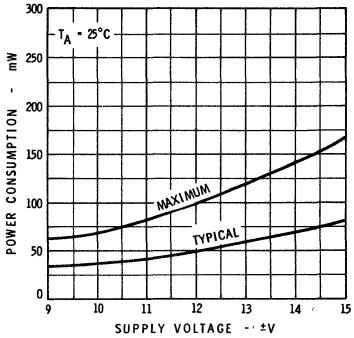


GUARANTEED ELECTRICAL CHARACTERISTICS (CONT'D)

INPUT COMMON MODE VOLTAGE RANGE

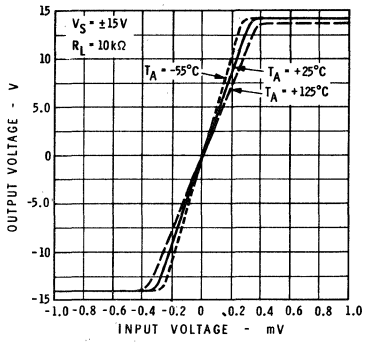


POWER CONSUMPTION

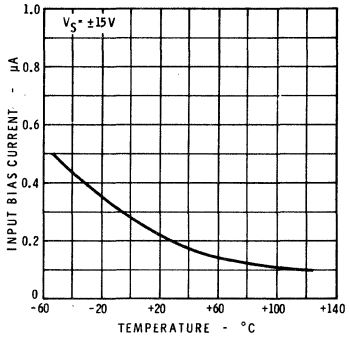


TYPICAL PERFORMANCE CURVES

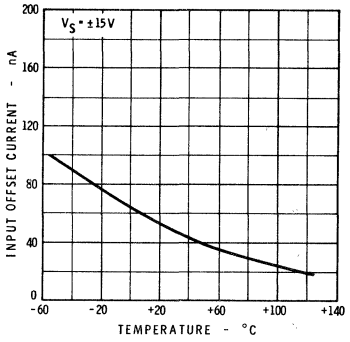
VOLTAGE TRANSFER CHARACTERISTIC



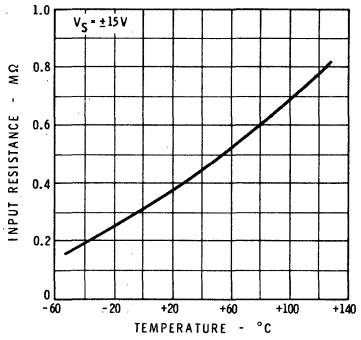
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



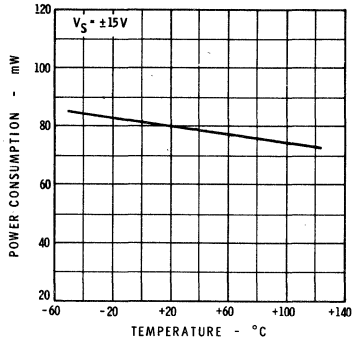
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



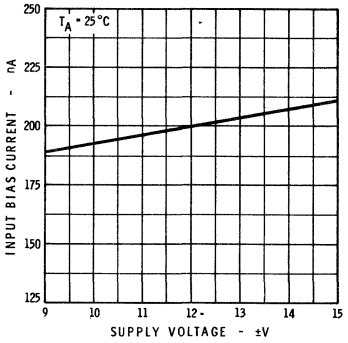
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



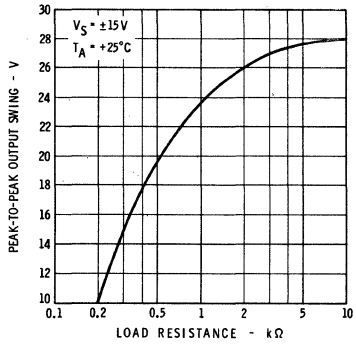
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



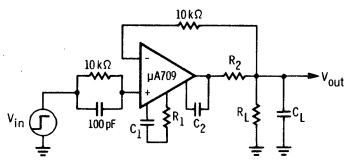
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



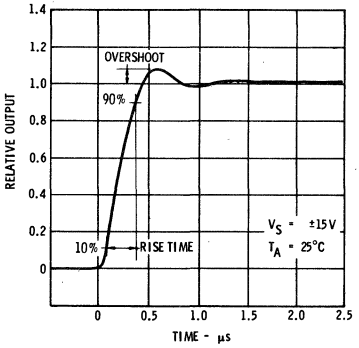
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



TRANSIENT RESPONSE TEST CIRCUIT



TRANSIENT RESPONSE



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE - That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT - The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE - The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT - The average of the two input currents.

INPUT VOLTAGE RANGE - A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO - The ratio of the input voltage range to the maximum change in input offset voltage over this range.

LARGE-SIGNAL VOLTAGE GAIN - The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING - The peak output swing, referred to zero, that can be obtained without clipping.

OUTPUT RESISTANCE - The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

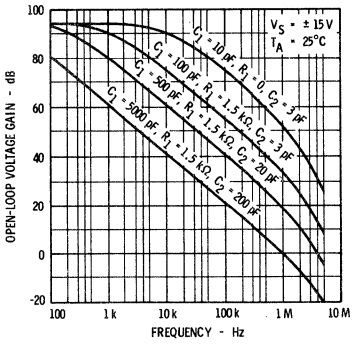
POWER CONSUMPTION - The DC power required to operate the amplifier with the output at zero and with no load current.

SUPPLY VOLTAGE REJECTION RATIO - The ratio of the change in input offset voltage to the change in supply voltage producing it.

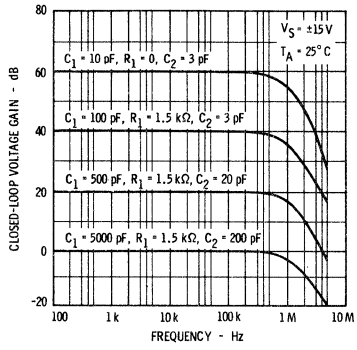
TRANSIENT RESPONSE - The closed-loop step function response of the amplifier under small-signal conditions.

TYPICAL PERFORMANCE CURVES

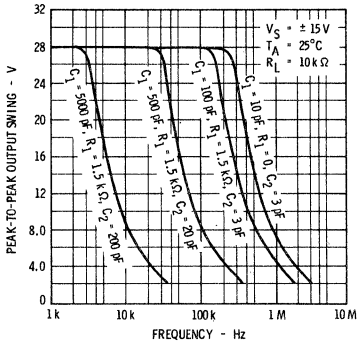
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



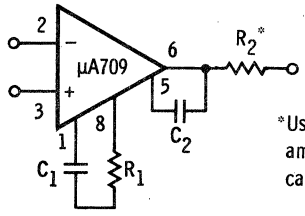
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



FREQUENCY COMPENSATION CIRCUIT



*Use R_2 = 50 Ω when the amplifier is operated with capacitive loading.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

μA709A

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **2 mV MAXIMUM OFFSET VOLTAGE**
- **50 nA MAXIMUM OFFSET CURRENT**
- **GUARANTEED DRIFT CHARACTERISTICS**

GENERAL DESCRIPTION — The μA709A is a high-gain operational amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load, and low power consumption. The device displays exceptional temperature stability and will operate over a 14-36 V range of total supply voltage with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, low-level instrumentation applications, and for the generation of special linear and nonlinear transfer functions. Although it features improved performance, the μA709A is a direct plug-in replacement for the μA709 operational amplifier.

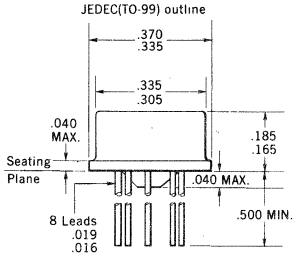
ABSOLUTE MAXIMUM RATINGS

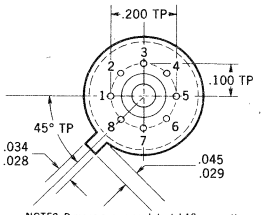
Total Supply Voltage	36 V
Internal Power Dissipation (Note 1)	300 mW
Differential Input Voltage	±5.0 V
Input Voltage	±10 V
Output Short-Circuit Duration ($T_A = +25°C$)	5 sec
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C

NOTES:
(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +95°C.

PHYSICAL DIMENSIONS

in accordance with JEDEC(TO-99) outline

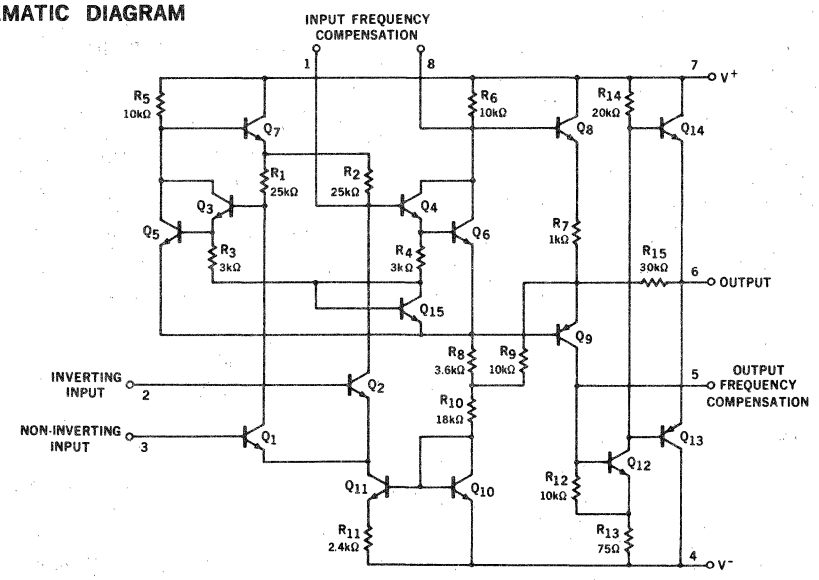




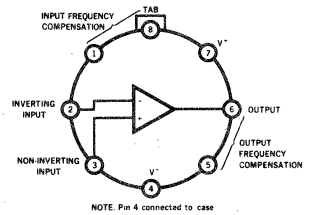
NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

† **ORDER PART NO. U5B7709311**

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



NOTE: Pin 4 connected to case

(Top View)

† This device is also available in the Flat Package. Order Part Number U3A7709311.

*Planar is a patented Fairchild process.

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

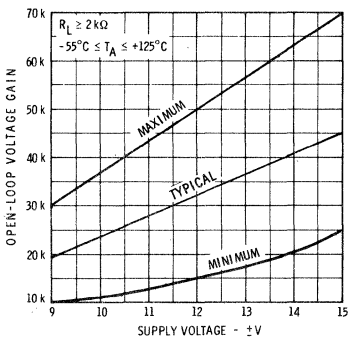
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS ($T_A = +25°C$, $\pm 9\,V \leq V_S \leq \pm 15\,V$ unless otherwise specified)

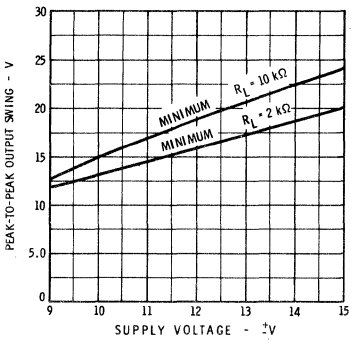
PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10\,k\Omega$		0.6	2.0	mV
Input Offset Current			10	50	nA
Input Bias Current			100	200	nA
Input Resistance		350	700		kΩ
Output Resistance			150		Ω
Supply Current	$V_S = \pm 15\,V$		2.5	3.6	mA
Power Consumption	$V_S = \pm 15\,V$		75	108	mW
Transient Response	$V_S = \pm 15\,V$, $V_{in} = 20\,mV$, $R_L = 2\,k\Omega$, $C_1 = 5\,nF$, $R_1 = 1.5\,k\Omega$, $C_2 = 200\,pF$, $R_2 = 50\,\Omega$				
Risetime				1.5	μs
Overshoot	$C_L \leq 100\,pF$			30	%
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10\,k\Omega$			3.0	mV
Average Temperature Coefficient	$R_S = 50\,\Omega$, $T_A = +25°C$ to $T_A = +125°C$		1.8	10	μV/°C
of Input Offset Voltage	$R_S = 50\,\Omega$, $T_A = +25°C$ to $T_A = -55°C$		1.8	10	μV/°C
	$R_S = 10\,k\Omega$, $T_A = +25°C$ to $T_A = +125°C$		2.0	15	μV/°C
	$R_S = 10\,k\Omega$, $T_A = +25°C$ to $T_A = -55°C$		4.8	25	μV/°C
Input Offset Current	$T_A = +125°C$		3.5	50	nA
	$T_A = -55°C$		40	250	nA
Average Temperature Coefficient	$T_A = +25°C$ to $T_A = +125°C$		0.08	0.5	nA/°C
of Input Offset Current	$T_A = +25°C$ to $T_A = -55°C$		0.45	2.8	nA/°C
Input Bias Current	$T_A = -55°C$		300	600	nA
Input Resistance	$T_A = -55°C$	85	170		kΩ
Input Voltage Range	$V_S = \pm 15\,V$	±8.0			V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	80	110		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$		40	100	μV/ V
Large-Signal Voltage Gain	$V_S = \pm 15\,V$, $R_L \geq 2\,k\Omega$, $V_{out} = \pm 15\,V$	25,000		70,000	
Output Voltage Swing	$V_S = \pm 15\,V$, $R_L \geq 10\,k\Omega$	±12	±14		V
	$V_S = \pm 15\,V$, $R_L \geq 2\,k\Omega$	±10	±13		V
Supply Current	$T_A = +125°C$, $V_S = \pm 15\,V$		2.1	3.0	mA
	$T_A = -55°C$, $V_S = \pm 15\,V$		2.7	4.5	mA
Power Consumption	$T_A = +125°C$, $V_S = \pm 15\,V$		63	90	mW
	$T_A = -55°C$, $V_S = \pm 15\,V$		81	135	mW

GUARANTEED ELECTRICAL CHARACTERISTICS

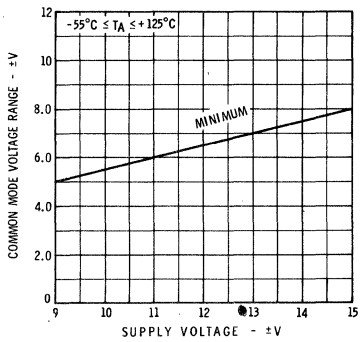
VOLTAGE GAIN



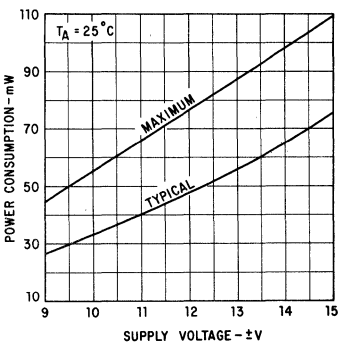
OUTPUT VOLTAGE SWING



INPUT COMMON MODE VOLTAGE RANGE

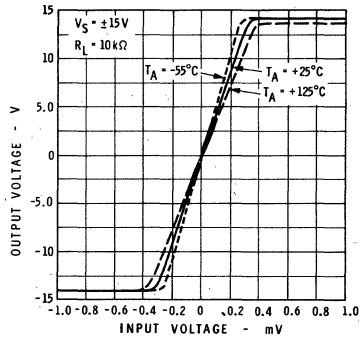


POWER CONSUMPTION

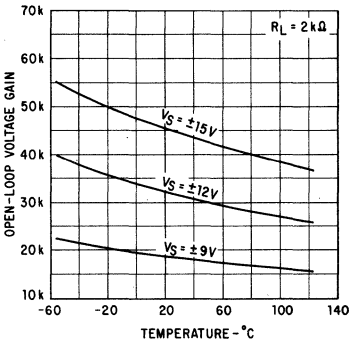


TYPICAL PERFORMANCE CURVES

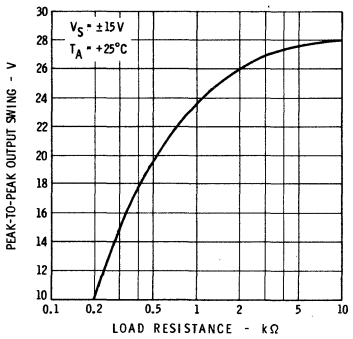
VOLTAGE TRANSFER CHARACTERISTIC



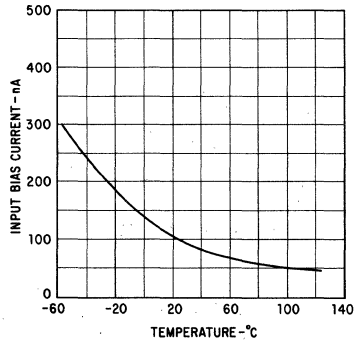
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



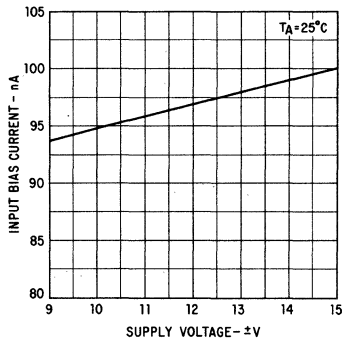
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



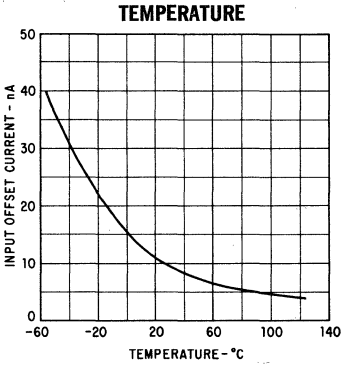
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



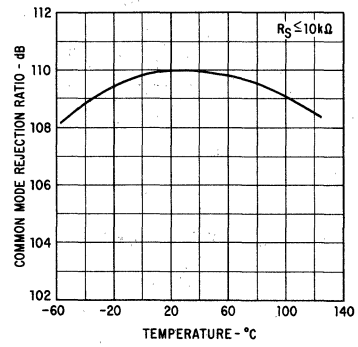
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



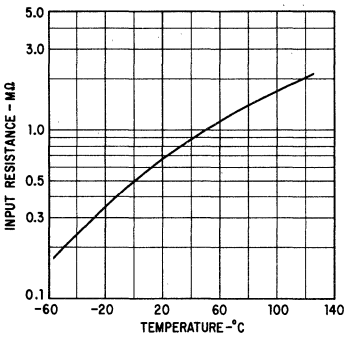
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



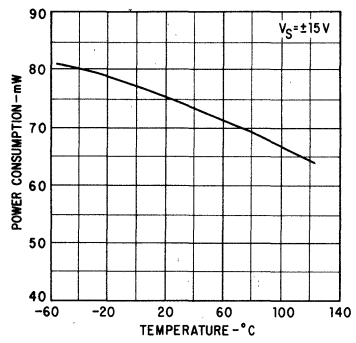
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



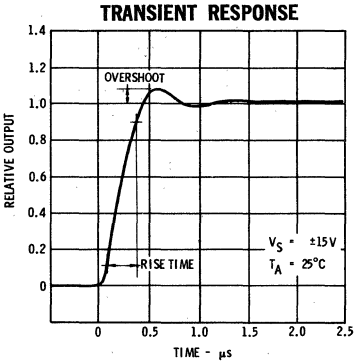
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



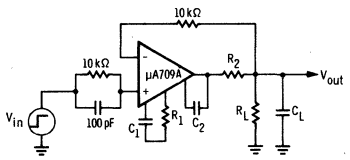
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



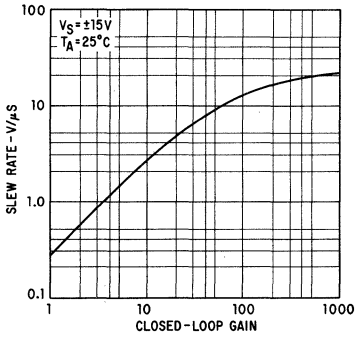
TRANSIENT RESPONSE



TRANSIENT RESPONSE TEST CIRCUIT



SLEW RATE AS A FUNCTION OF CLOSED-LOOP GAIN USING RECOMMENDED COMPENSATION NETWORKS



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at zero volts.

INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.

LARGE-SIGNAL VOLTAGE GAIN — The ratio of the maximum output voltage swing with load to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT VOLTAGE SWING — The peak output swing, referred to zero, that can be obtained without clipping.

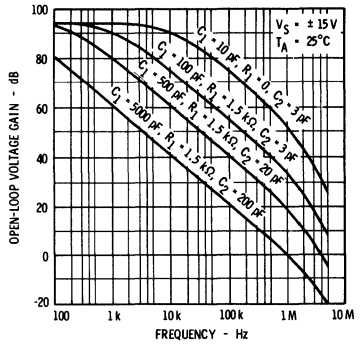
OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

POWER CONSUMPTION — The DC power required to operate the amplifier with the output at zero and with no load current.

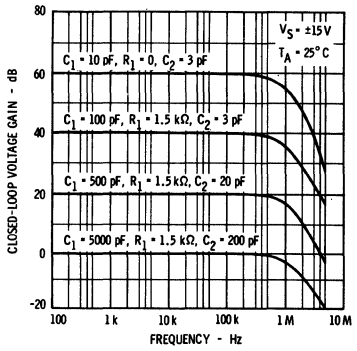
TRANSIENT RESPONSE — The closed-loop step-function response of the amplifier under small-signal conditions.

TYPICAL PERFORMANCE CURVES

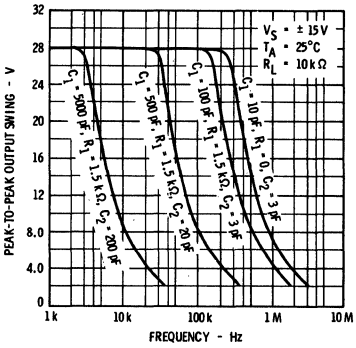
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



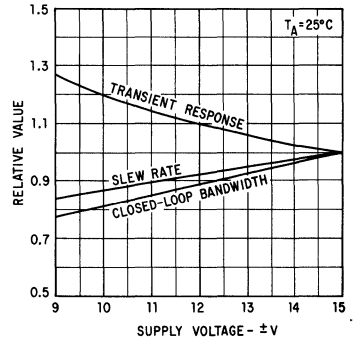
FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



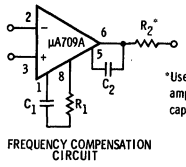
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY FOR VARIOUS COMPENSATION NETWORKS



FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



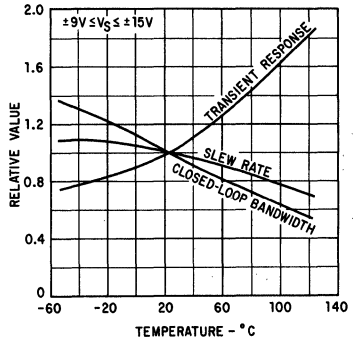
FREQUENCY COMPENSATION CIRCUIT



FREQUENCY COMPENSATION CIRCUIT

*Use R_2 = 50 Ω when the amplifier is operated with capacitive loading.

FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

μA709B

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

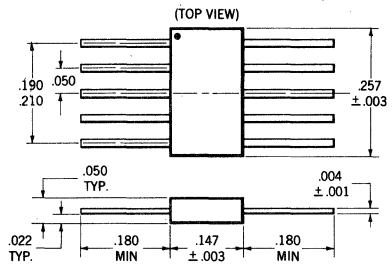
GENERAL DESCRIPTION — The μA709B is a high-gain operational amplifier constructed on a single silicon chip using the Fairchild Planar* epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions. For improved specifications, see μA709A or μA709 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	250 mW
Differential Input Voltage	±5.0 V
Input Voltage	±10 V
Output Short-Circuit Duration ($T_A = 25°C$)	5 sec
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 second time limit)	300°C

PHYSICAL DIMENSIONS

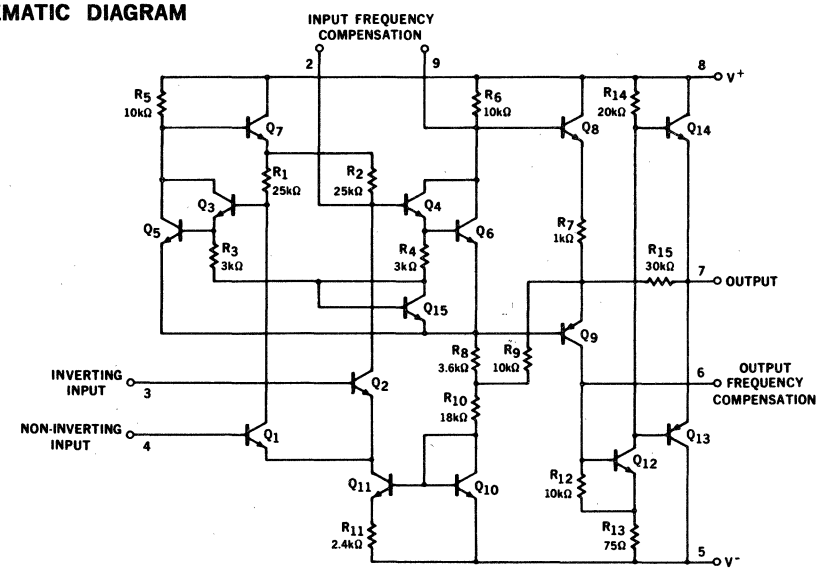
(TYPICAL FLAT PACKAGE)



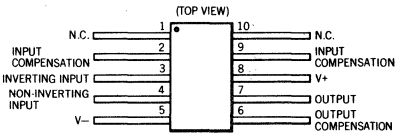
Note: All dimensions in inches

ORDER PART NO.
U3T7709313

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



Note: Pin 5 connected to case.

*Planar is a patented Fairchild process.

NOTES:
(1) Rating applies for case temperatures to +125°C; derate linearly at 2.5 mW/°C for ambient temperatures above +60°C.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

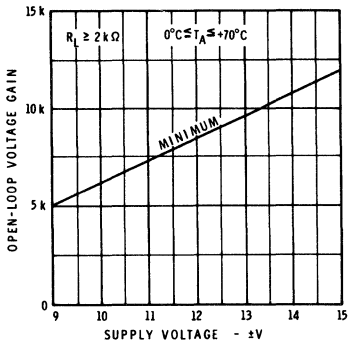
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

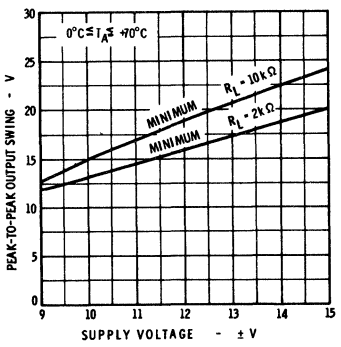
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ, ± 9 V $\leq V_S \leq \pm 15$ V		2.0	7.5	mV
Input Offset Current			100	500	nA
Input Bias Current			0.3	1.5	μA
Input Resistance		50	250		kΩ
Output Resistance			150		Ω
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	15,000	45,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Input Voltage Range		±8.0	±10		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	65	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		25	200	μV/V
Power Consumption			80	200	mW
Transient Response	$V_{in} = 20$ mV, $R_L = 2$ kΩ,				
Risetime	$C_1 = 5000$ pF, $R_1 = 1.5$ kΩ,		0.3		μs
	$C_2 = 200$ pF, $R_2 = 50$ Ω				
Overshoot	$C_L \leq 100$ pF		10		%
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ, ± 9 V $\leq V_S \leq \pm 15$ V			10	mV
Input Offset Current				750	nA
Input Bias Current				2.0	μA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	12,000			
Input Resistance		35			kΩ
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ, ± 9 V $\leq V_S \leq \pm 15$ V			12.5	mV
Input Offset Current				1.2	μA
Input Bias Current				3.0	μA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	10,000			

GUARANTEED ELECTRICAL CHARACTERISTICS

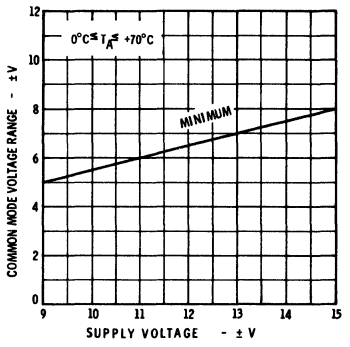
VOLTAGE GAIN



OUTPUT VOLTAGE SWING

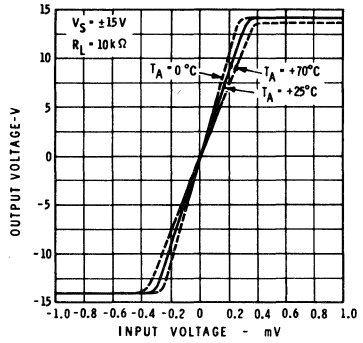


INPUT COMMON MODE VOLTAGE RANGE

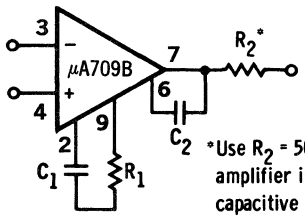


TYPICAL PERFORMANCE CURVES

VOLTAGE TRANSFER CHARACTERISTIC

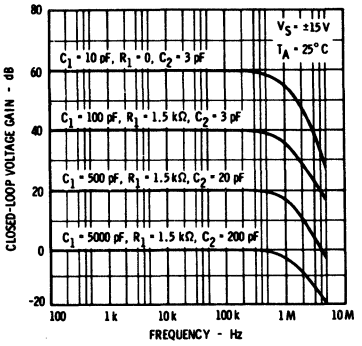


FREQUENCY COMPENSATION CIRCUIT



*Use R_2 = 50 Ω when the amplifier is operated with capacitive loading.

FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



μA709C

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

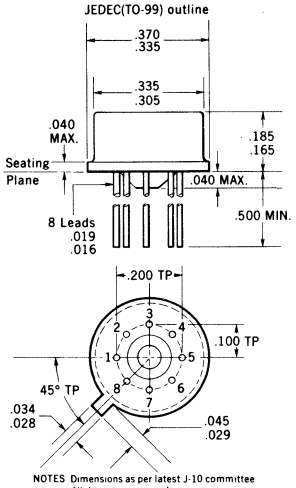
GENERAL DESCRIPTION - The μA709C is a high-gain operational amplifier constructed on a single silicon chip using the Fairchild Planar epitaxial process. It features low offset, high input impedance, large input common mode range, high output swing under load and low power consumption. The device displays exceptional temperature stability and will operate over a wide range of supply voltages with little degradation of performance. The amplifier is intended for use in DC servo systems, high impedance analog computers, in low-level instrumentation applications and for the generation of special linear and nonlinear transfer functions. For full temperature range operation (-55°C to +125°C) see μA709 or μA709A data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		± 18 V
Internal Power Dissipation	(Note 1)	250 mW
Differential Input Voltage		± 5.0 V
Input Voltage		± 10 V
Output Short-Circuit Duration	(T_A = 25°C)	5 sec
Storage Temperature Range		-65°C to +150°C
Operating Temperature Range		0°C to +70°C
Lead Temperature (Soldering, 60 sec)		300°C

PHYSICAL DIMENSIONS

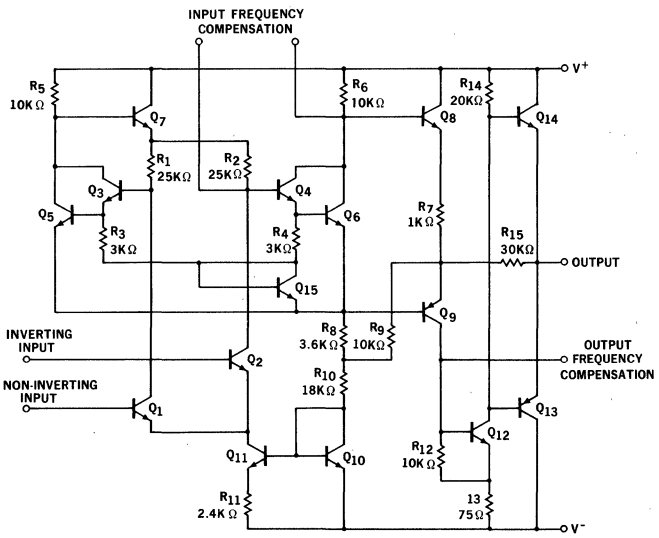
in accordance with JEDEC(TO-99) outline



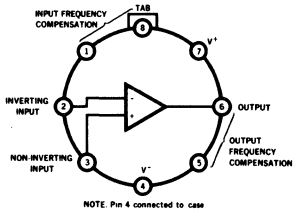
NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO.
U5B770939X

SCHEMATIC DIAGRAM



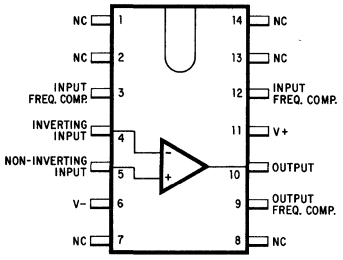
CONNECTION DIAGRAM



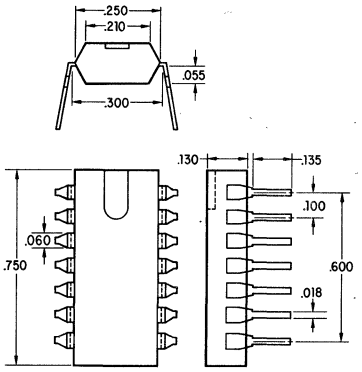
NOTE: Pin 4 connected to case

(Top View)

CONNECTION DIAGRAM



PHYSICAL DIMENSIONS



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows, .300 centers

ORDER PART NO.
U6E770939J

NOTE 1: Rating applies for ambient temperatures to +70°C.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

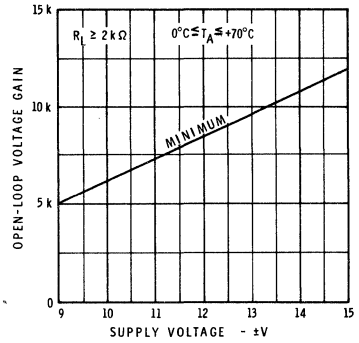
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C unless otherwise specified)

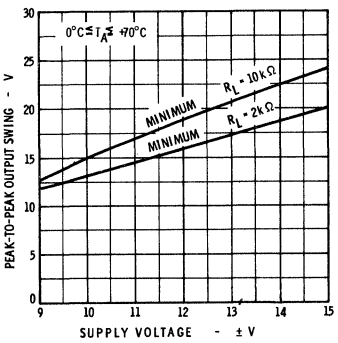
Parameter	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	$R_S \leq 10\,k\Omega$, ±9 V $\leq V_S \leq$ ±15 V		2.0	7.5	mV
Input Offset Current			100	500	nA
Input Bias Current			0.3	1.5	μA
Input Resistance		50	250		kΩ
Output Resistance			150		Ω
Large-Signal Voltage Gain	$R_L \geq 2\,k\Omega$, V_{out} = ±10 V	15,000	45,000		
Output Voltage Swing	$R_L \geq 10\,k\Omega$	±12	±14		V
	$R_L \geq 2\,k\Omega$	±10	±13		V
Input Voltage Range		±8.0	±10		V
Common Mode Rejection Ratio	$R_S \leq 10\,k\Omega$	65	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\,k\Omega$		25	200	μV/V
Power Consumption			80	200	mW
Transient Response	V_{in} = 20 mV, R_L = 2 kΩ,				
Risetime	C_1 = 5000 pF, R_1 = 1.5 kΩ, C_2 = 200 pF, R_2 = 50 Ω		0.3		μs
Overshoot	$C_L \leq 100$ pF		10		%
The following specifications apply for 0°C $\leq T_A \leq$ +70°C					
Input Offset Voltage	$R_S \leq 10k\Omega$, ±9 V $\leq$ ±15 V			10	mV
Input Offset Current				750	nA
Input Bias Current				2.0	μA
Large-Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{out} = ±10 V	12,000			
Input Resistance		35			kΩ

GUARANTEED ELECTRICAL CHARACTERISTICS

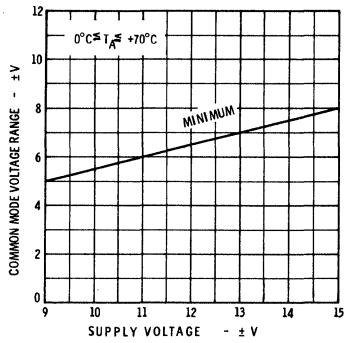
VOLTAGE GAIN



OUTPUT VOLTAGE SWING

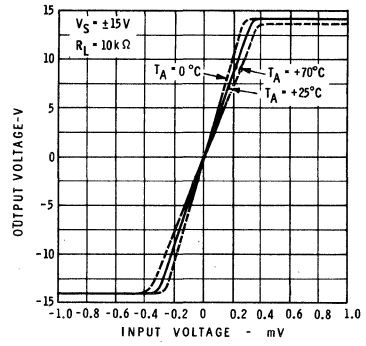


INPUT COMMON MODE VOLTAGE RANGE

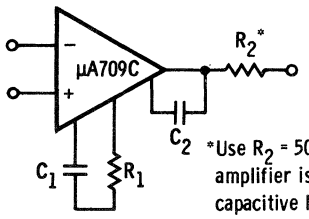


TYPICAL PERFORMANCE CURVES

VOLTAGE TRANSFER CHARACTERISTIC

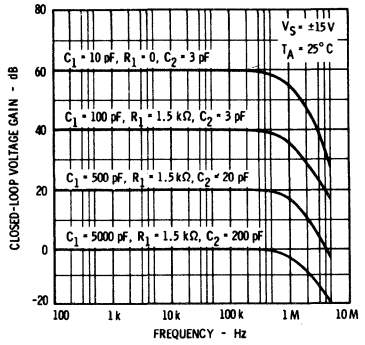


FREQUENCY COMPENSATION CIRCUIT



*Use R_2 = 50 Ω when the amplifier is operated with capacitive loading.

FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS



μA710

HIGH-SPEED DIFFERENTIAL COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

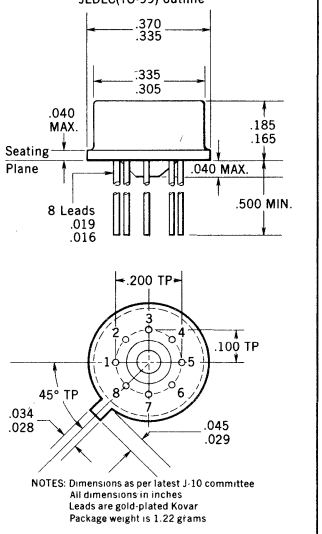
- **IMPROVED SPECIFICATIONS**
- **2 mV MAXIMUM OFFSET VOLTAGE**
- **3 μA MAXIMUM OFFSET CURRENT**
- **1250 MINIMUM VOLTAGE GAIN**
- **10 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

GENERAL DESCRIPTION — The μA710 is a differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device is useful as a variable threshold Schmidt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage		+14.0 V
Negative Supply Voltage		−7.0 V
Peak Output Current		10 mA
Differential Input Voltage		±5.0 V
Input Voltage		±7.0 V
Internal Power Dissipation		
TO-99	[Note 1]	300 mW
Flat Package	[Note 2]	200 mW
Operating Temperature Range		−55°C to +125°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)		300°C

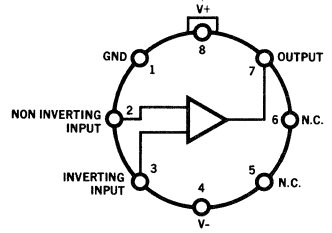
PHYSICAL DIMENSIONS
in accordance with
JEDEC(TO-99) outline



NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

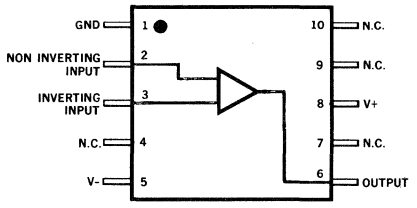
ORDER PART NO.
U5B771031X

TO-99 CONNECTION DIAGRAM
(TOP VIEW)

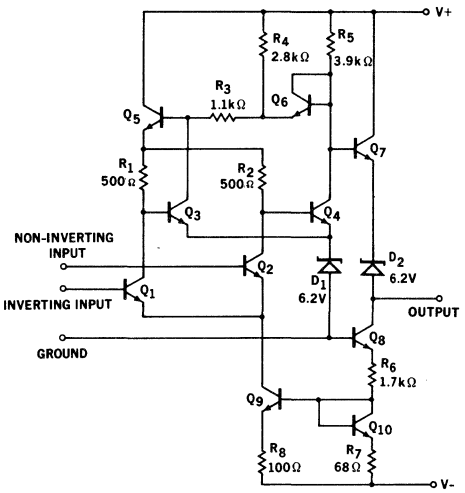


Note: Pin 4 connected to case.

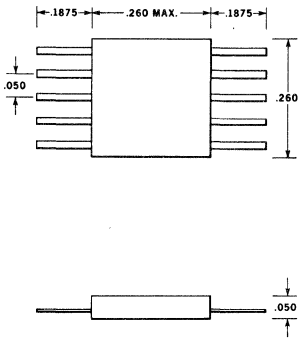
FLAT PACKAGE CONNECTION DIAGRAM
(TOP VIEW)



SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)



ORDER PART NO.
U3H771031X

Notes on page 2

* Planar is a patented Fairchild process.

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS ($T_A = +25°C$, $V^+ = 12.0V$, $V^- = -6.0V$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS (Note 4)	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		0.6	2.0	mV
Input Offset Current			0.75	3.0	μA
Input Bias Current			13	20	μA
Voltage Gain		1250	1700		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	2.0	2.5		mA
Response Time [Note 3]			40		ns
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 200\Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$ to $T_A = +125°C$ $R_S = 50\Omega$, $T_A = 25°C$ to $T_A = -55°C$		3.5 2.7	10 10	μV/°C μV/°C
Input Offset Current	$T_A = +125°C$		0.25	3.0	μA
	$T_A = -55°C$		1.8	7.0	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +125°C$ $T_A = 25°C$ to $T_A = -55°C$		5.0 15	25 75	nA/°C nA/°C
Input Bias Current	$T_A = -55°C$		27	45	μA
Input Voltage Range	$V^- = -7.0V$	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\Omega$	80	100		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		1000			
Positive Output Level	$\Delta V_{in} \geq 5$ mV, $0 \leq I_{out} \leq 5.0$ mA	2.5	3.2	4.0	V
Negative Output Level	$\Delta V_{in} \geq 5$ mV	−1.0	−0.5	0	V
Output Sink Current	$T_A = +125°C$, $\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	0.5	1.7		mA
	$T_A = -55°C$, $\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	1.0	2.3		mA
Positive Supply Current	$V_{out} \leq 0$		5.2	9.0	mA
Negative Supply Current			4.6	7.0	mA
Power Consumption			90	150	mW

NOTES:

(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +105°C.

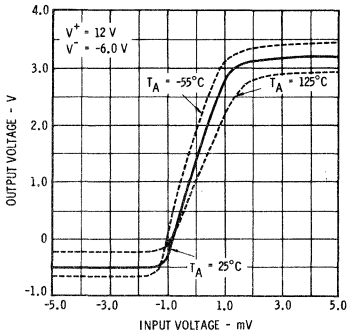
(2) Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.

(3) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

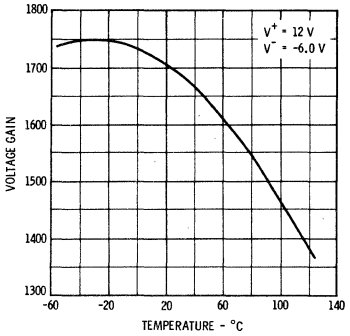
(4) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.4V at +25°C and 1.0V at +125°C.

TYPICAL PERFORMANCE CURVES

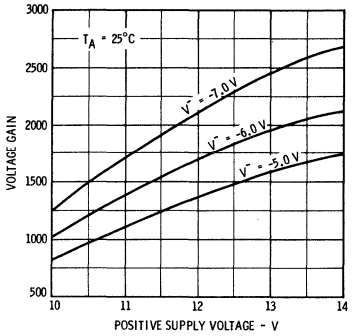
VOLTAGE TRANSFER CHARACTERISTIC



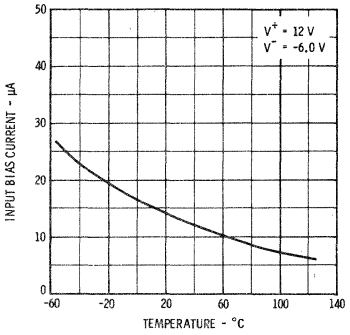
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



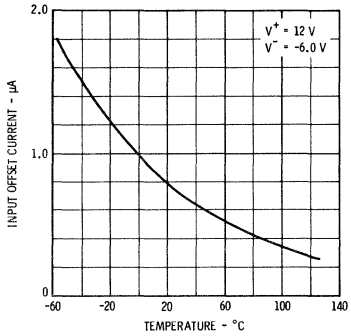
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



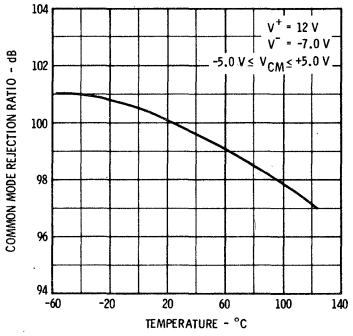
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



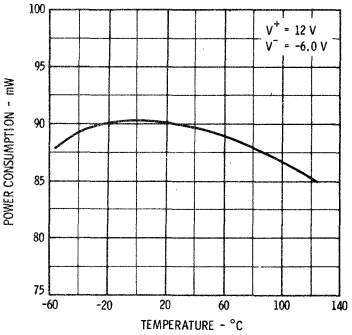
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



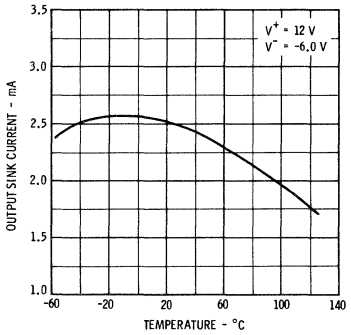
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



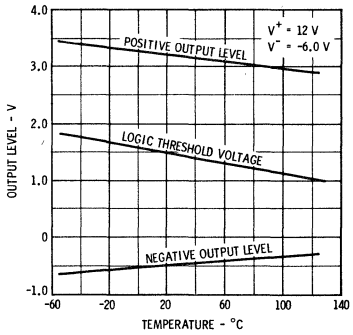
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



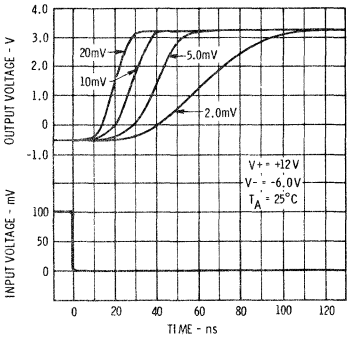
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



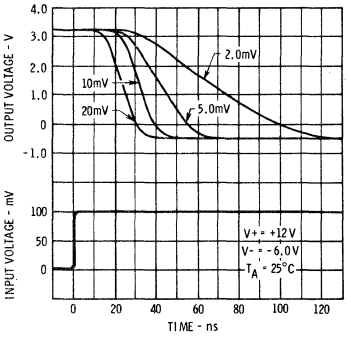
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



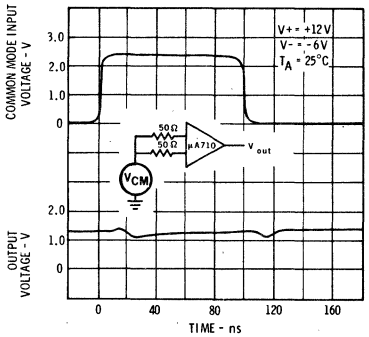
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



COMMON MODE PULSE RESPONSE



DEFINITIONS

LOGIC THRESHOLD VOLTAGE — The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE — The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage on the input terminals for which the comparator will operate within specifications.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL INPUT VOLTAGE RANGE — The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN — The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

POSITIVE OUTPUT LEVEL — The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL — The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT — The maximum negative current than can be delivered by the comparator.

PEAK OUTPUT CURRENT — The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

POWER CONSUMPTION — The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

μA710B

HIGH-SPEED DIFFERENTIAL COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **5 mV MAXIMUM OFFSET VOLTAGE**
- **5 μA MAXIMUM OFFSET CURRENT**
- **1000 MINIMUM VOLTAGE GAIN**
- **20 μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

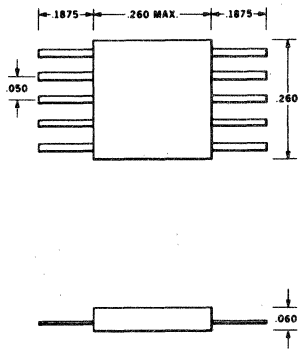
GENERAL DESCRIPTION — The μA710B is a differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device is useful as a variable threshold Schmidt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

For improved specifications, see μA710 data sheet.

ABSOLUTE MAXIMUM RATINGS

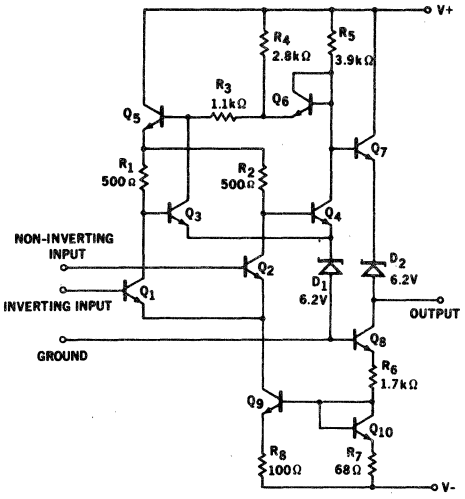
Positive Supply Voltage	+14.0 V
Negative Supply Voltage	−7.0 V
Peak Output Current	10 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Internal Power Dissipation (Note 1)	200 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)

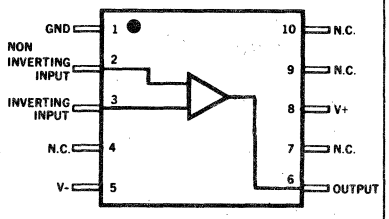


ORDER PART NO.
U3H7710313

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



(TOP VIEW)

*Planar is a patented Fairchild process.

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FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12.0V$, $V^- = -6.0V$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS (Note 3)	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\,\Omega$		1.6	5.0	mV
Input Offset Current			1.8	5.0	μA
Input Bias Current			16	25	μA
Voltage Gain		1000	1500		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	1.6	2.5		mA
Response Time (Note 2)			40		ns
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 200\,\Omega$			6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\,\Omega$, $T_A = 0°C$ to $T_A = +70°C$		5.0	20	μV/°C
Input Offset Current				7.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +70°C$		15	50	nA/°C
	$T_A = 25°C$ to $T_A = 0°C$		24	100	nA/°C
Input Bias Current	$T_A = 0°C$		25	40	μA
Voltage Gain		800			
Output Sink Current	$\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	0.5			mA
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 200\,\Omega$			7.5	mV
Input Offset Current	$T_A = +125°C$		0.9	5.0	μA
	$T_A = -55°C$		3.8	15	μA
Input Bias Current	$T_A = -55°C$		34	80	μA
Input Voltage Range	$V^- = -7.0$ V	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\,\Omega$	70	98		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		500			
Positive Output Level	$\Delta V_{in} \geq 5$ mV, $0 \leq I_{out} \leq 5.0$ mA	2.5	3.2	4.0	V
Negative Output Level	$\Delta V_{in} \geq 5$ mV	−1.0	−0.5	0	V
Positive Supply Current	$V_{out} \leq 0$		5.2	9.0	mA
Negative Supply Current			4.6	7.0	mA
Power Consumption			90	150	mW

NOTES:

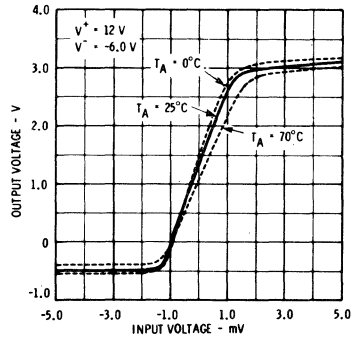
(1) Derate linearly at 4.4 mW/°C for case temperatures above +115°C; derate linearly at 3.3 mW/°C for ambient temperatures above +100°C.

(2) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

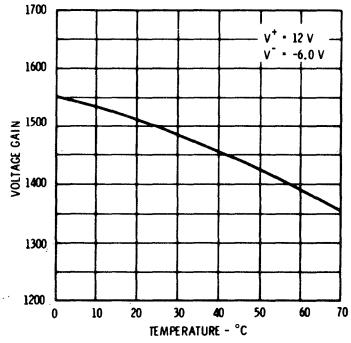
(3) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at −55°C, 1.5V at 0°C, 1.4V at +25°C, 1.2V at +70°C, and 1.0V at +125°C.

TYPICAL PERFORMANCE CURVES

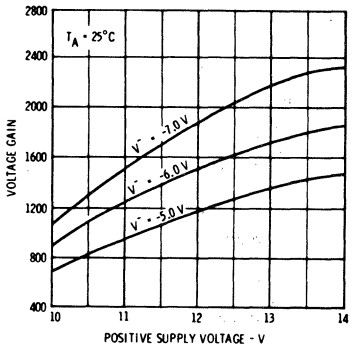
VOLTAGE TRANSFER CHARACTERISTIC



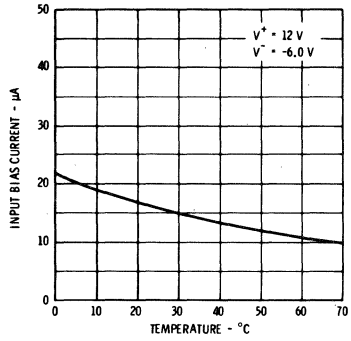
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



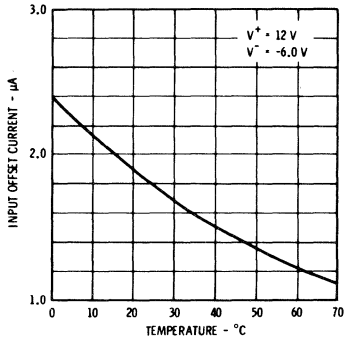
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



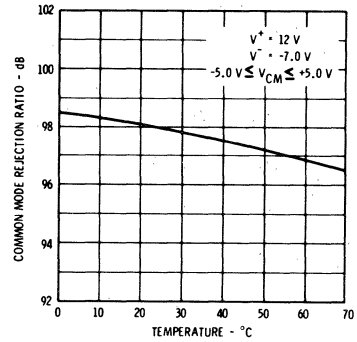
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



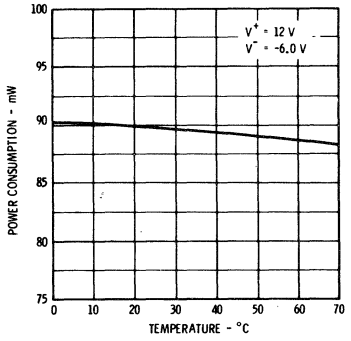
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



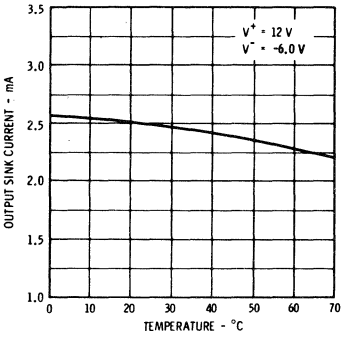
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



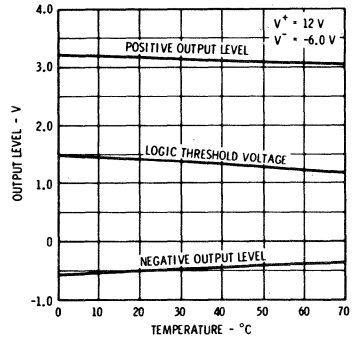
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



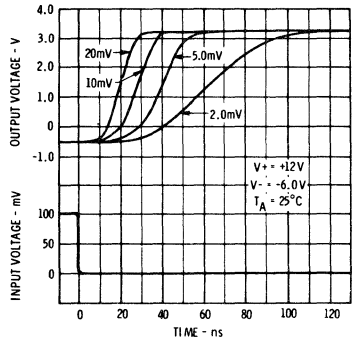
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



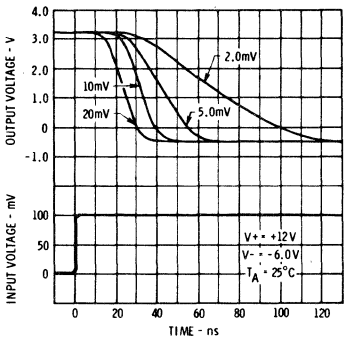
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



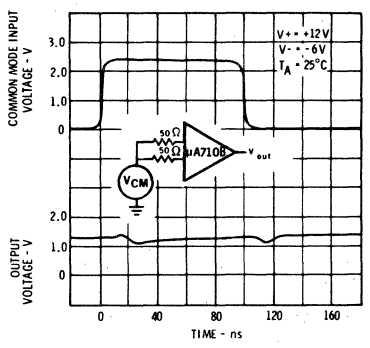
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



COMMON MODE PULSE RESPONSE



DEFINITIONS

LOGIC THRESHOLD VOLTAGE — The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE — The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage on the input terminals for which the comparator will operate within specifications.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL INPUT VOLTAGE RANGE — The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN — The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

POSITIVE OUTPUT LEVEL — The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL — The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT — The maximum negative current than can be delivered by the comparator.

PEAK OUTPUT CURRENT — The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

POWER CONSUMPTION — The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

μA710C

HIGH-SPEED DIFFERENTIAL COMPARATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

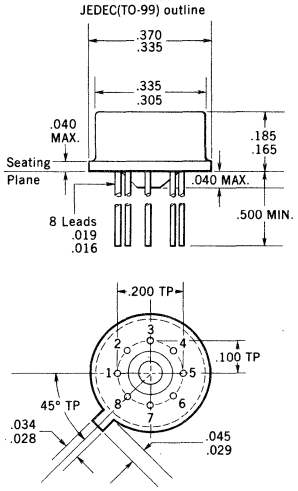
- **IMPROVED SPECIFICATIONS**
- **5mV MAXIMUM OFFSET VOLTAGE**
- **5μA MAXIMUM OFFSET CURRENT**
- **1000 MINIMUM VOLTAGE GAIN**
- **20μV/°C MAXIMUM OFFSET VOLTAGE DRIFT**

GENERAL DESCRIPTION— The μA710C is a differential voltage comparator intended for applications requiring high accuracy and fast response times. It is constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device is useful as a variable threshold Schmidt trigger, a pulse height discriminator, a voltage comparator in high-speed A-D converters, a memory sense amplifier or a high-noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.
For full temperature range operation (−55°C to +125°C) see μA710 data sheet.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+14.0 V
Negative Supply Voltage	−7.0 V
Peak Output Current	10 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Internal Power Dissipation [Note 1]	
TO-99	300 mW
Flat Package	200 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

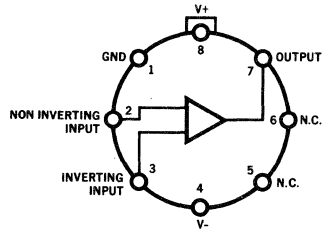
PHYSICAL DIMENSIONS
in accordance with
JEDEC(TO-99) outline



NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

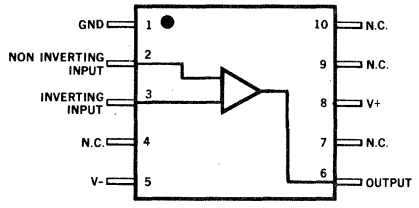
ORDER PART NO.U5B771039X

TO-99 CONNECTION DIAGRAM
(TOP VIEW)

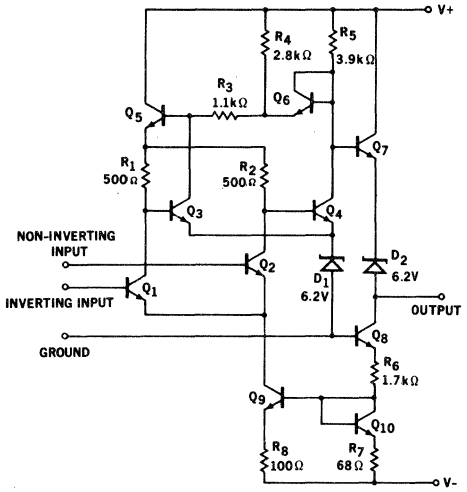


Note: Pin 4 connected to case.

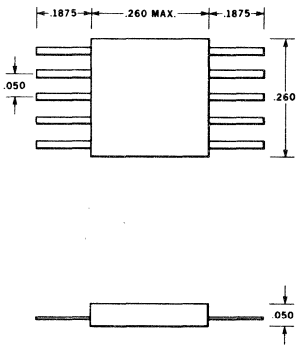
FLAT PACKAGE CONNECTION DIAGRAM
(TOP VIEW)



SCHEMATIC DIAGRAM



PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)



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U3H771039X

Notes on page 2

* Planar is a patented Fairchild process.

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313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12.0V$, $V^- = -6.0V$ unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS (Note 3)	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 200\Omega$		1.6	5.0	mV
Input Offset Current			1.8	5.0	μA
Input Bias Current			16	25	μA
Voltage Gain		1000	1500		
Output Resistance			200		Ω
Output Sink Current	$\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	1.6	2.5		mA
Response Time [Note 2]			40		ns
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 200\Omega$			6.5	mV
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$, $T_A = 0°C$ to $T_A = +70°C$		5.0	20	μV/°C
Input Offset Current				7.5	μA
Average Temperature Coefficient of Input Offset Current	$T_A = 25°C$ to $T_A = +70°C$ $T_A = 25°C$ to $T_A = 0°C$		15 24	50 100	nA/°C nA/°C
Input Bias Current	$T_A = 0°C$		25	40	μA
Input Voltage Range	$V^- = -7.0V$	±5.0			V
Common Mode Rejection Ratio	$R_S \leq 200\Omega$	70	98		dB
Differential Input Voltage Range		±5.0			V
Voltage Gain		800			
Positive Output Level	$\Delta V_{in} \geq 5$ mV, $0 \leq I_{out} \leq 5.0$ mA	2.5	3.2	4.0	V
Negative Output Level	$\Delta V_{in} \geq 5$ mV	−1.0	−0.5	0	V
Output Sink Current	$\Delta V_{in} \geq 5$ mV, $V_{out} = 0$	0.5			mA
Positive Supply Current	$V_{out} \leq 0$		5.2	9.0	mA
Negative Supply Current			4.6	7.0	mA
Power Consumption			90	150	mW

NOTES:

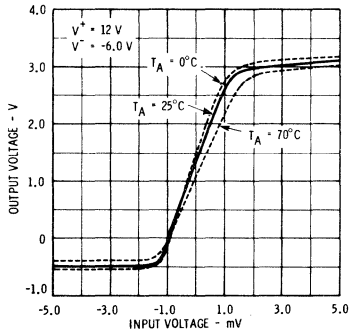
(1) Ratings apply for ambient temperatures to +70°C.

(2) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

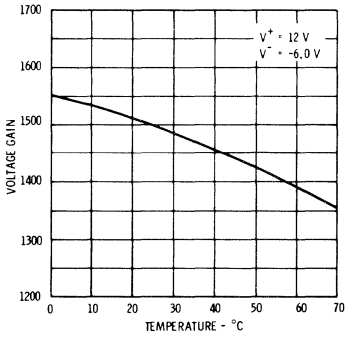
(3) The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.5V at 0°C, 1.4V at +25°C and 1.2V at +70°C.

TYPICAL PERFORMANCE CURVES

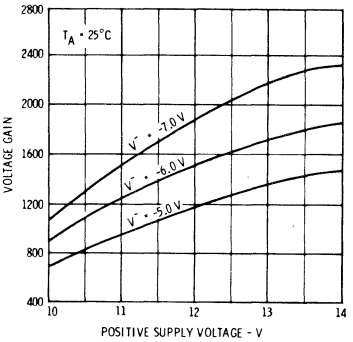
VOLTAGE TRANSFER CHARACTERISTIC



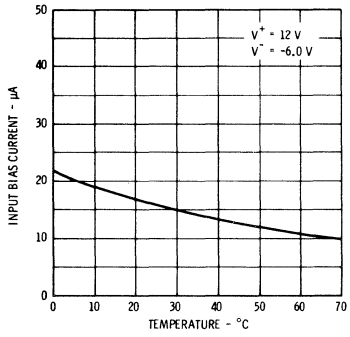
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



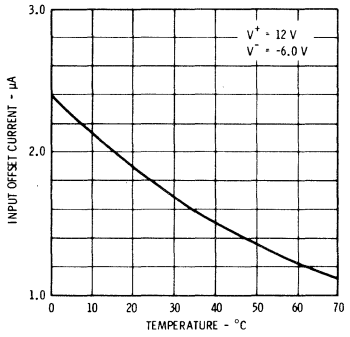
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



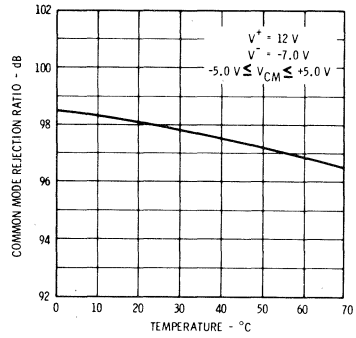
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



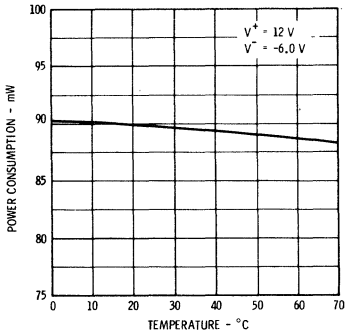
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



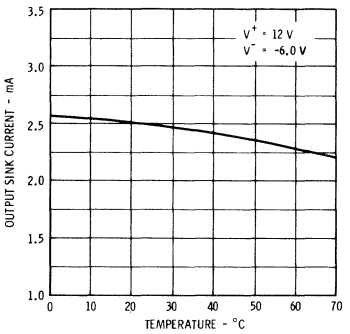
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



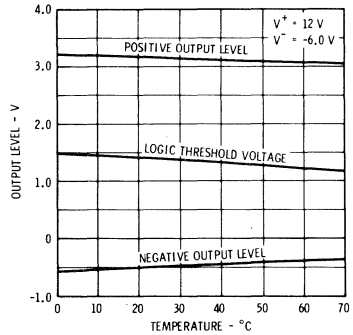
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



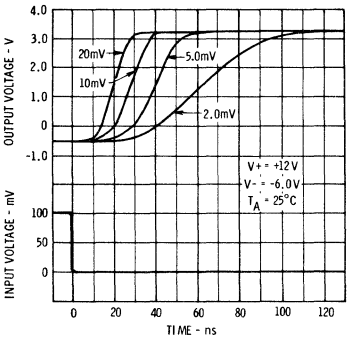
OUTPUT SINK CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



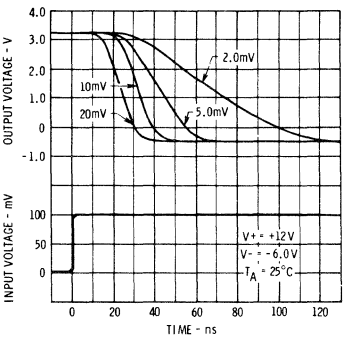
OUTPUT VOLTAGE LEVELS AS A FUNCTION OF AMBIENT TEMPERATURE



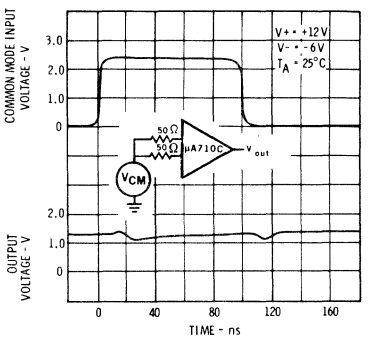
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



COMMON MODE PULSE RESPONSE



DEFINITIONS

LOGIC THRESHOLD VOLTAGE — The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE — The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT — The average of the two input currents.

INPUT VOLTAGE RANGE — The range of voltage on the input terminals for which the comparator will operate within specifications.

INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.

DIFFERENTIAL INPUT VOLTAGE RANGE — The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN — The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME — The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

POSITIVE OUTPUT LEVEL — The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL — The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT — The maximum negative current than can be delivered by the comparator.

PEAK OUTPUT CURRENT — The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

POWER CONSUMPTION — The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

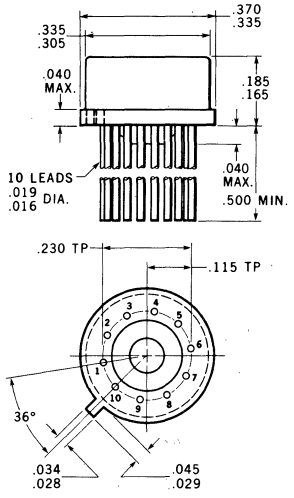
μA711
DUAL COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The μA711 is a dual, differential voltage comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double-ended limit detector for automatic Go/No-go test equipment. The μA711, which is similar to the μA710 differential comparator, is constructed on a 40-mil square silicon chip using the Fairchild Planar* epitaxial process.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage	+14.0 V
Negative Supply Voltage	-7.0 V
Peak Output Current	50 mA
Differential Input Voltage	±5.0 V
Input Voltage	±7.0 V
Strobe Voltage	0 to +6.0 V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

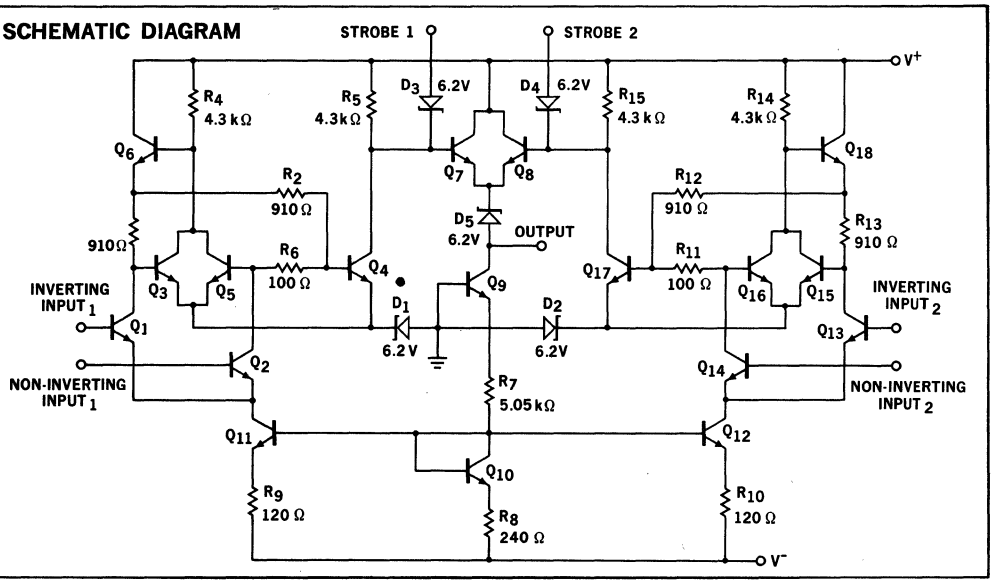
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO-100)



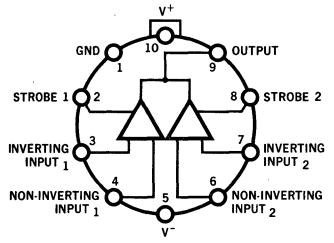
NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams

ORDER PART NO.
U5F771131X

SCHEMATIC DIAGRAM



TO-5 CONNECTION DIAGRAM (TOP VIEW)



Note: Pin 5 connected to case

Notes on page 2

* Planar is a patented Fairchild process.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12.0 V, V^- = -6.0 V unless otherwise specified)

Parameter (see definitions)	Conditions	Min.	Typ.	Max.	Units
Input Offset Voltage	V_{out} = +1.4 V, $R_S \leq 200\,\Omega$, V_{CM} = 0		1.0	3.5	mV
	V_{out} = +1.4 V, $R_S \leq 200\,\Omega$		1.0	5.0	mV
Input Offset Current	V_{out} = +1.4 V		0.5	10.0	μA
Input Bias Current			25	75	μA
Voltage Gain		750	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	V^- = -7.0 V	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Positive Output Level	$V_{in} \geq 10$ mV		4.5	5.0	V
Loaded Positive Output Level	$V_{in} \geq 10$ mV, I_O = 5 mA	2.5	3.5		V
Negative Output Level	$V_{in} \geq 10$ mV	-1.0	-0.5	0	V
Strobed Output Level	$V_{strobe} \leq 0.3$ V	-1.0		0	V
Output Sink Current	$V_{in} \geq 10$ mV, $V_{out} \geq 0$	0.5	0.8		mA
Strobe Current	V_{strobe} = 100 mV		1.2	2.5	mA
Positive Supply Current	$V_{out} \leq 0$		8.6		mA
Negative Supply Current			3.9		mA
Power Consumption			130	200	mW
The following specifications apply for -55°C $\leq T_A \leq$ +125°C:					
Input Offset Voltage (Note 3)	$R_S \leq 200\,\Omega$, V_{CM} = 0			4.5	mV
	$R_S \leq 200\,\Omega$			6.0	mV
Input Offset Current (Note 3)				20	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

NOTES:

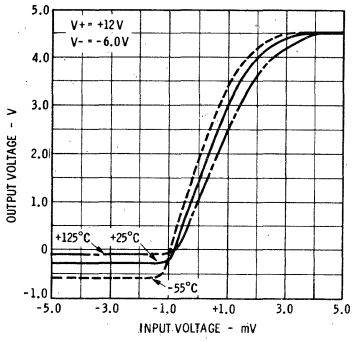
(1) Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above 105°C.

(2) The response time specified (see definitions) is for a 100-mV input step with 5-mV overdrive.

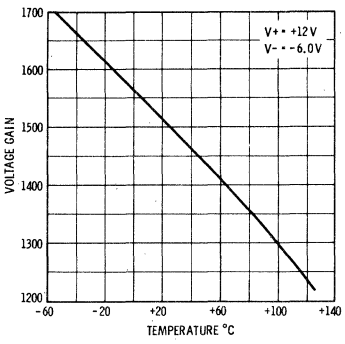
(3) The input offset voltage (see definitions) is specified for a logic threshold voltage of 1.8 V at -55°C, 1.4 V at +25°C and 1.0 V at +125°C.

TYPICAL PERFORMANCE CURVES

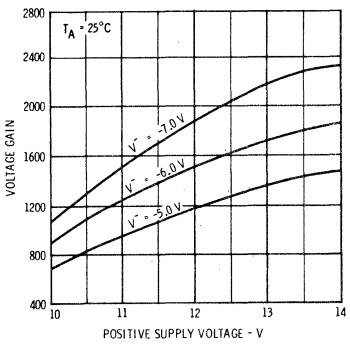
VOLTAGE TRANSFER CHARACTERISTIC



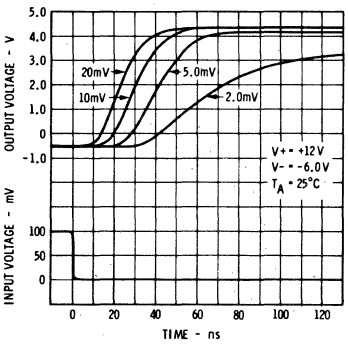
VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



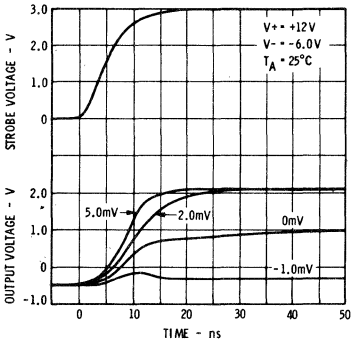
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGES



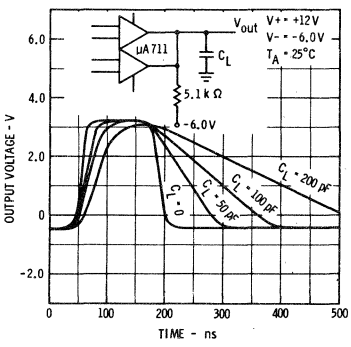
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



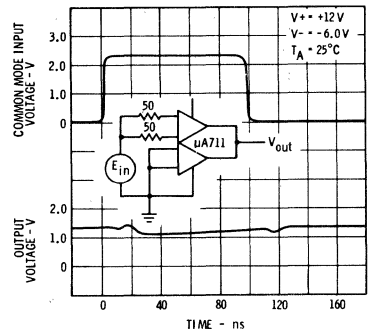
STROBE RELEASE TIME FOR VARIOUS INPUT OVERDRIVES



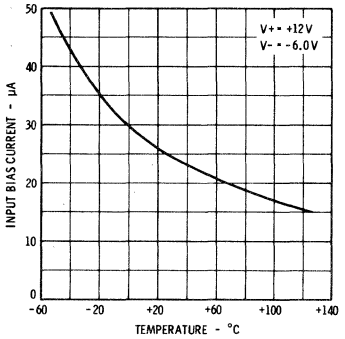
OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING



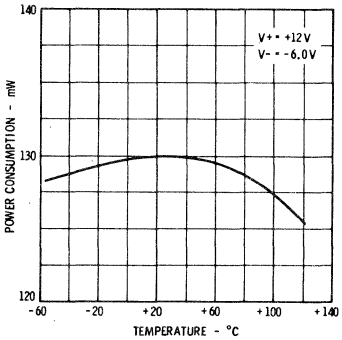
COMMON MODE PULSE RESPONSE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



DEFINITIONS

LOGIC THRESHOLD VOLTAGE - The approximate voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

INPUT OFFSET VOLTAGE* - The voltage between the input terminals when the output is at the logic threshold voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT OFFSET CURRENT* - The difference in the currents into the two input terminals with the output at the logic threshold voltage.

INPUT BIAS CURRENT* - The average of the two input currents.

INPUT VOLTAGE RANGE* - The range of voltage on the input terminals for which the comparator will operate within specifications.

DIFFERENTIAL INPUT VOLTAGE RANGE* - The range of voltage between the input terminals for which operation within specifications is assured.

VOLTAGE GAIN* - The ratio of the change in output voltage to the change in voltage between the input terminals producing it with the DC output level in the vicinity of the logic threshold voltage.

RESPONSE TIME* - The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

STROBE RELEASE TIME* - The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

POSITIVE OUTPUT LEVEL* - The DC output voltage in the positive direction with the input voltage equal to or greater than a minimum specified amount.

NEGATIVE OUTPUT LEVEL* - The DC output voltage in the negative direction with the input voltage equal to or greater than a minimum specified amount.

OUTPUT SINK CURRENT - The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT - The maximum current that may flow into the output load without causing damage to the comparator.

OUTPUT RESISTANCE* - The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

STROBED OUTPUT LEVEL* - The DC output voltage, independent of input voltage, with the voltage on the strobe terminal equal to or less than a minimum specified amount.

STROBE CURRENT - The maximum current drawn by the strobe terminal when it is at the zero logic level.

POWER CONSUMPTION - The DC power into the amplifier with no output load. The DC power will vary with signal level, but is specified as a maximum for the entire range of input-signal conditions.

*These definitions apply for either side with the other disabled with the strobe.

μA711C
DUAL COMPARATOR
FAIRCHILD LINEAR INTEGRATED CIRCUITS

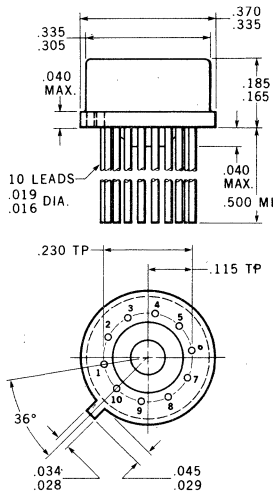
GENERAL DESCRIPTION - The μA711C is a dual, differential voltage comparator intended primarily for core-memory sense amplifier applications. The device features high accuracy, fast response times, large input voltage range, low power consumption and compatibility with practically all integrated logic forms. When used as a sense amplifier, the threshold voltage can be adjusted over a wide range, almost independent of the integrated circuit characteristics. Independent strobing of each comparator channel is provided, and pulse stretching on the output is easily accomplished. Other applications of the dual comparator include a window discriminator in pulse height detectors and a double-ended limit detector for automatic Go/No-go test equipment. The μA711C, which is similar to the μA710C differential comparator, is constructed on a 40-mil square silicon chip using the Fairchild Planar epitaxial process.

For full temperature range operation (-55°C to +125°C) see μA711 data sheet.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage		+14.0 V
Negative Supply Voltage		-7.0 V
Peak Output Current		50 mA
Differential Input Voltage		±5.0 V
Input Voltage		±7.0 V
Strobe Voltage		0 to +6.0 V
Internal Power Dissipation	(Note 1)	300 mW
Operating Temperature Range		0°C to +70°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

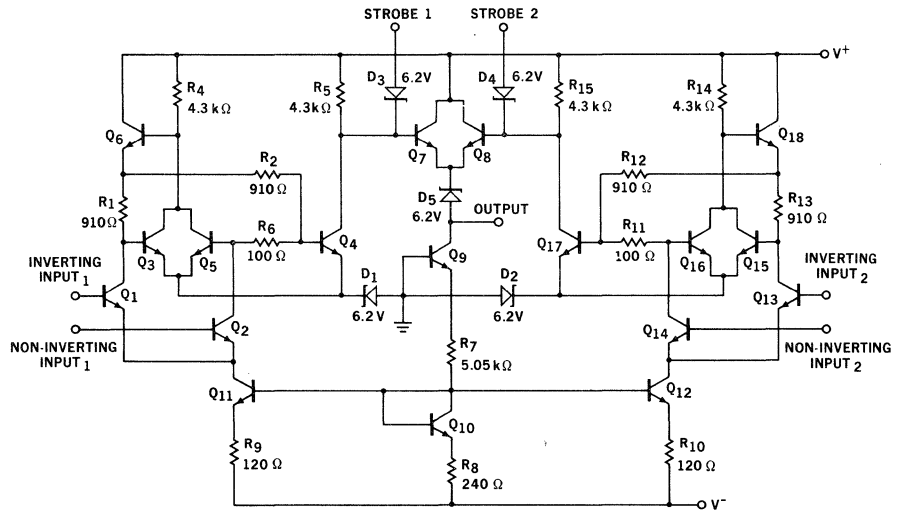
PHYSICAL DIMENSIONS
In accordance with JEDEC (TO-100) outline



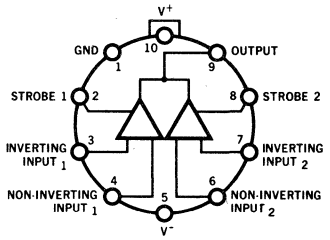
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART NO.
U5F771139X

SCHEMATIC DIAGRAM



TO-100 CONNECTION DIAGRAM (TOP VIEW)



Note Pin 5 connected to case

Notes on page 2

* Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = 12.0 V, V^- = -6.0 V unless otherwise specified)

Parameter	Conditions	Min.	Typ.	Max	Units
Input Offset Voltage	V_{out} = +1.4 V, $R_S \leq 200\,\Omega$, V_{CM} = 0		1.0	5.0	mV
	V_{out} = +1.4 V, $R_S \leq 200\,\Omega$		1.0	7.5	mV
Input Offset Current	V_{out} = +1.4 V		0.5	15	μA
Input Bias Current			25	100	μA
Voltage Gain		700	1500		
Response Time (Note 2)			40		ns
Strobe Release Time			12		ns
Input Voltage Range	V^- = -7.0 V	±5.0			V
Differential Input Voltage Range		±5.0			V
Output Resistance			200		Ω
Positive Output Level	$V_{in} \geq 10$ mV		4.5	5.0	V
Loaded Positive Output Level	$V_{in} \geq 10$ mV, I_O = 5 mA	2.5	3.5		V
Negative Output Level	$V_{in} \geq 10$ mV	-1.0	-0.5	0	V
Strobed Output Level	$V_{strobe} \leq 0.3$ V	-1.0		0	V
Output Sink Current	$V_{in} \geq 10$ mV, $V_{out} \geq 0$	0.5	0.8		mA
Strobe Current	V_{strobe} = 100 mV		1.2	2.5	mA
Positive Supply Current	$V_{out} \leq 0$		8.6		mA
Negative Supply Current			3.9		mA
Power Consumption			130	230	mW
The following specifications apply for 0°C ≤ T_A ≤ +70°C:					
Input Offset Voltage (Note 3)	$R_S \leq 200\,\Omega$, V_{CM} = 0			6.0	mV
	$R_S \leq 200\,\Omega$			10	mV
Input Offset Current (Note 3)				25	μA
Input Bias Current				150	μA
Temperature Coefficient of Input Offset Voltage			5.0		μV/°C
Voltage Gain		500			

NOTES:

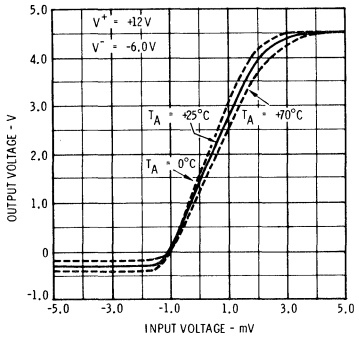
(1) Rating applies for ambient temperatures to +70°C.

(2) The response time specified is for a 100-mV input step with 5-mV overdrive.

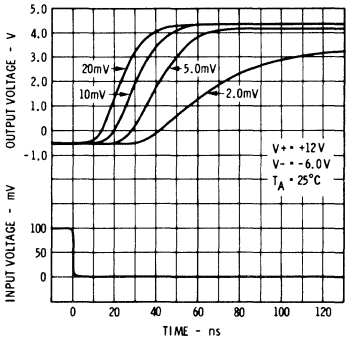
(3) The input offset voltage is specified for a logic threshold voltage of 1.5 V at 0°C, 1.4 V at +25°C and 1.2 V at +70°C.

TYPICAL ELECTRICAL CHARACTERISTICS

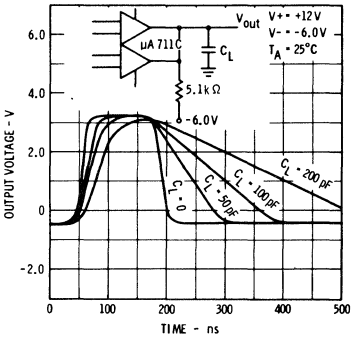
VOLTAGE TRANSFER CHARACTERISTIC



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



OUTPUT PULSE STRETCHING WITH CAPACITIVE LOADING



μA716

FIXED-GAIN, LOW DISTORTION AMPLIFIER

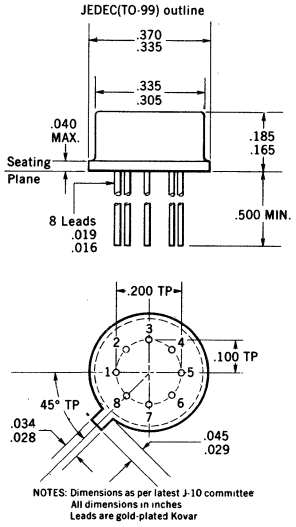
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA716 is a fixed-gain, medium power amplifier intended for use as a telephone system channel amplifier, headset amplifier or a general-purpose audio preamplifier. It provides medium output current capability, low distortion, excellent gain stability, and wide bandwidth. Fixed voltage gains of 10, 20, 100, and 200 are available by selecting external taps.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	27 V
Internal Power Dissipation (Note 1)	400 mW
Input Voltage	± 5 V
Peak Output Current ($T_A = 25°C$)	100 mA
Storage Temperature Range	− 65°C to + 150°C
Operating Temperature Range	− 55°C to + 125°C
Lead Temperature (soldering, 60 seconds)	300°C

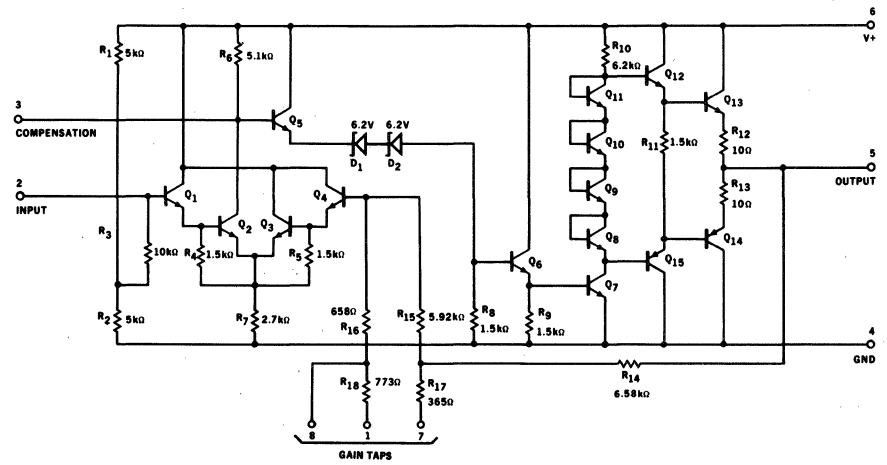
PHYSICAL DIMENSIONS
similar to
JEDEC(TO-99) outline



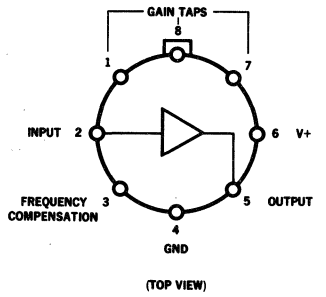
NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar

ORDER PART NO. U5K7716312

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



NOTE: Pin 4 internally connected to case.

NOTE 1: Rating applies for case temperatures to +125°C; derate linearly at 8.4 mW/°C for ambient temperature above +110°C.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

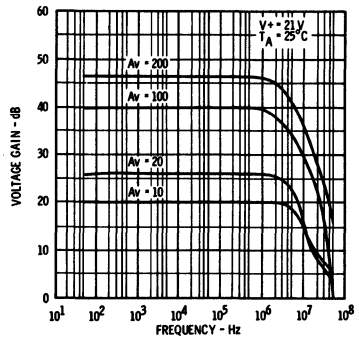
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq +125°C$, V+ = 21 V unless otherwise specified)

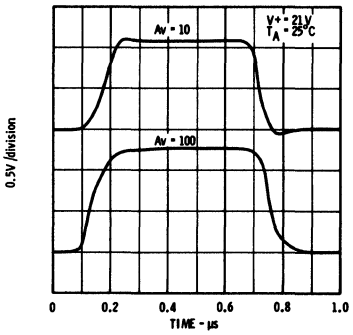
PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Quiescent Power Consumption	$T_A = 25°C$		286	298	mW
	$T_A = 125°C$		244	256	mW
Total Harmonic Distortion	f = 1 kHz, A_V = 10, P_O = 50 mW, $R_L = 150\Omega$		0.01	0.05	%
	f = 1 kHz, A_V = 100, P_O = 50 mW, $R_L = 150\Omega$		0.10	0.50	%
Input Noise Voltage	$R_S = 600\Omega$, $T_A = 25°C$, B_n = 16 Hz to 150 kHz		8.0		μV_{rms}
Output Voltage Swing	$R_L = 150\Omega$	10	12		V p-p
	$R_L \geq 5\ k\Omega$	15	17		V p-p
Input Resistance		9.0	11		kΩ
Output Resistance			1.0		Ω
Voltage Gain					
10x	See Table 1	9.0	10	11	
20x	See Table 1	18	20	22	
100x	See Table 1	95	105	115	
200x	See Table 1	185	205	225	
Bandwidth	$T_A = 25°C$		2.0		MHz
Temperature Stability of Voltage Gain	$T_{ref} = 25°C$				
10x				±0.50	dB
20x				±0.50	dB
100x				±0.50	dB
200x				±0.65	dB

TYPICAL PERFORMANCE CURVES

VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

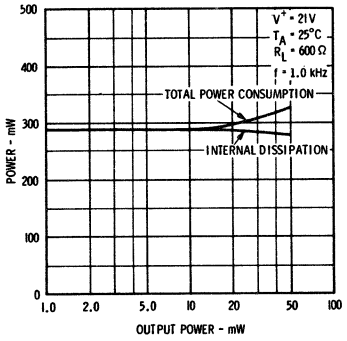


TRANSIENT RESPONSE

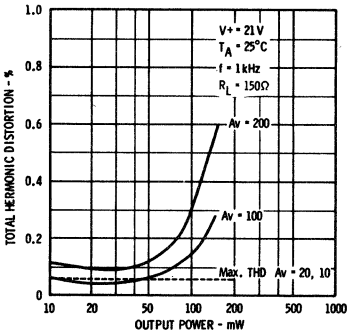


TYPICAL PERFORMANCE CURVES

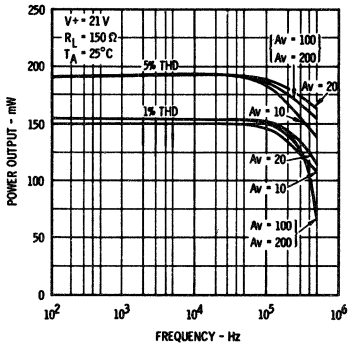
TOTAL POWER CONSUMPTION AND INTERNAL DEVICE DISSIPATION AS A FUNCTION OF OUTPUT POWER



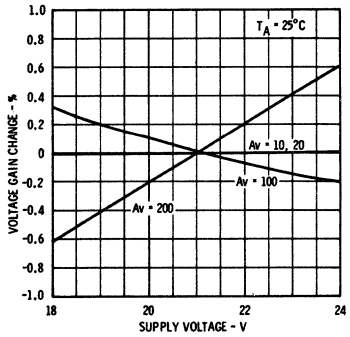
TOTAL HARMONIC DISTORTION AS A FUNCTION OF OUTPUT POWER



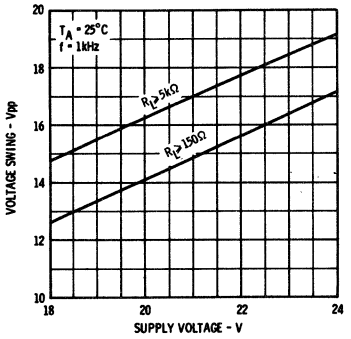
POWER OUTPUT AS A FUNCTION OF FREQUENCY 5% AND 1% TOTAL HARMONIC DISTORTION



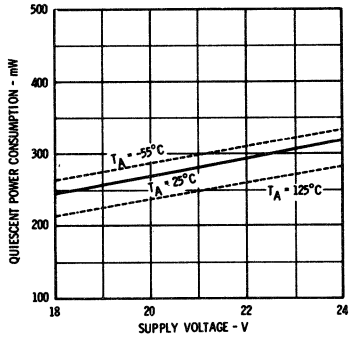
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



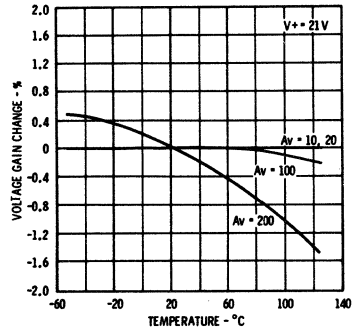
VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



QUIESCENT POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



CONNECTION DIAGRAM AND COMPONENT TABLE FOR AVAILABLE GAIN OPTIONS

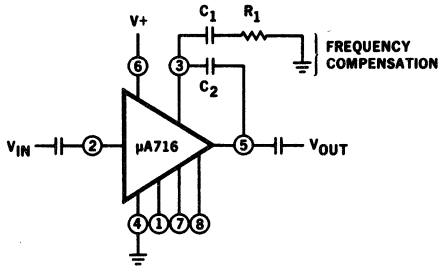


TABLE I

Voltage Gain	C_1	C_2	R_1	Decouple Pins:
10	68 pF	39 pF	75 Ω	1
20	50 pF	27 pF	75 Ω	8
100	None	3 pF	None	1, 7
200	None	3 pF	None	7, 8

DEFINITION OF TERMS

Quiescent Power Consumption — The DC power required to operate the amplifier with no signal applied at the input and the load current equal to zero.

Total Harmonic Distortion — The ratio of the sum of the amplitudes of all signals harmonically related to the fundamental, and the amplitude of the fundamental signal.

Input Noise Voltage — The noise voltage at the output of the amplifier, divided by the amplifier voltage gain.

Output Voltage Swing — The maximum output voltage that may be obtained at the output of the amplifier before saturation occurs.

Input Resistance — The small-signal resistance seen looking into the input terminal of the amplifier.

Voltage Gain — The ratio of the small-signal output voltage to the input voltage of the amplifier.

Temperature Stability of Voltage Gain — The maximum variation of the voltage gain over the specified temperature range.

μA716C

FIXED-GAIN, LOW DISTORTION AMPLIFIER

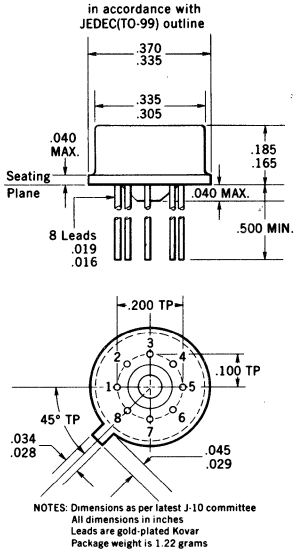
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA716C is a fixed-gain, medium power amplifier intended for use as a telephone system channel amplifier, headset amplifier or general purpose audio amplifier. It provides medium output current capability, low distortion, excellent gain stability, and wide bandwidth. Fixed voltage gains of 10, 20, 100 and 200 are available by selecting external taps.

ABSOLUTE MAXIMUM RATINGS:

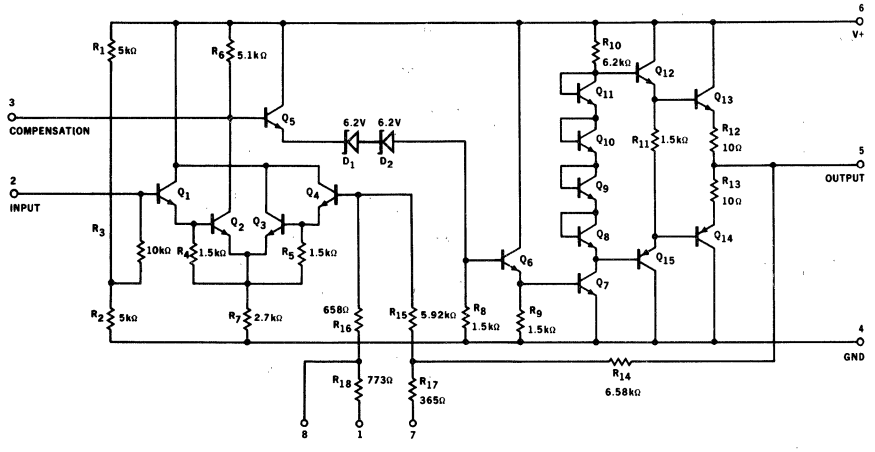
Supply Voltage	27 V
Internal Power Dissipation	600 mW
Input Voltage	±5 V
Peak Output Current ($T_A = 25°C$)	100 mA
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C

PHYSICAL DIMENSIONS

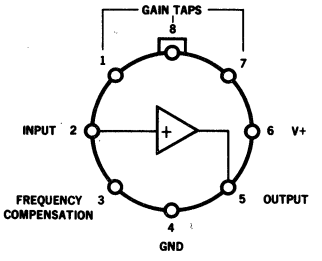


ORDER PART NO.U5B771639X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



(TOP VIEW)

NOTE: Lead No. 4 internally connected to case

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

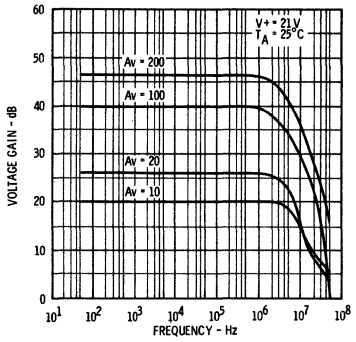
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$, $V^+ = 21V$ unless otherwise specified)

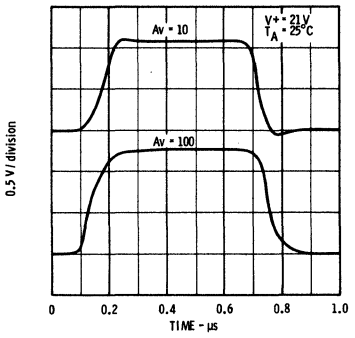
PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Quiescent Power Consumption	$T_A = 25°C$		280	350	mW
Total Harmonic Distortion	$A_V = 10$, $f = 1$ kHz, $P_O = 50$ mW, $R_L = 150\ \Omega$		0.01	0.05	%
	$A_V = 100$, $f = 1$ kHz, $P_O = 50$ mW, $R_L = 150\ \Omega$		0.10	0.50	%
Input Noise Voltage	$R_S = 600\ \Omega$, $T_A = 25°C$, $B_n = 16$ Hz to 150 kHz		8.0		μV_{rms}
Output Voltage Swing	$R_L = 150\ \Omega$	10	14		V_{p-p}
	$R_L \geq 5k\ \Omega$	15	17		V_{p-p}
Input Resistance		9.0	11		kΩ
Output Resistance			1.0		Ω
Voltage Gain	See Table I				
10x		9.0	10	11	
20x		18	20	22	
100x		95	105	115	
200x		185	205	225	
Bandwidth	$T_A = 25°C$		2.0		MHz
Temperature Stability of Voltage Gain	$T_{ref} = 25°C$				
10x			±0.02	±0.25	dB
20x			±0.02	±0.25	dB
100x			±0.02	±0.25	dB
200x			±0.05	±0.50	dB

TYPICAL PERFORMANCE CURVES

VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

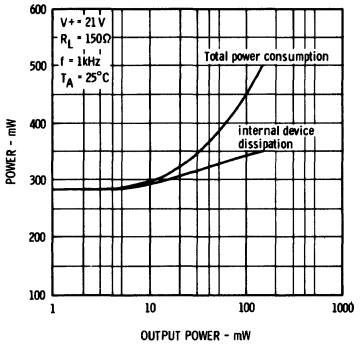


TRANSIENT RESPONSE

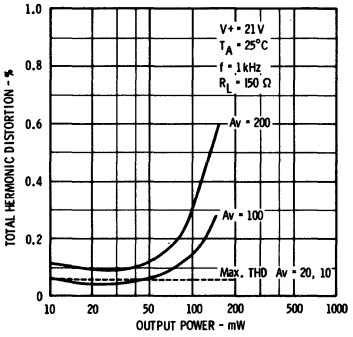


TYPICAL PERFORMANCE CURVES

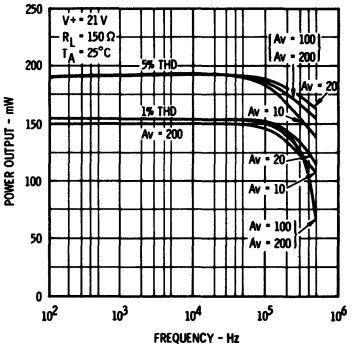
TOTAL POWER CONSUMPTION AND INTERNAL DEVICE DISSIPATION AS A FUNCTION OF OUTPUT POWER



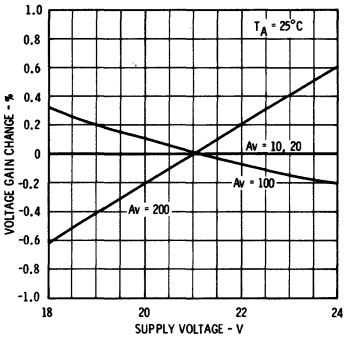
TOTAL HARMONIC DISTORTION AS A FUNCTION OF OUTPUT POWER



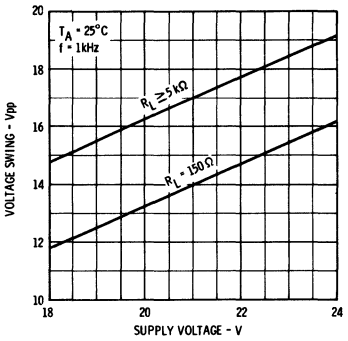
POWER OUTPUT AS A FUNCTION OF FREQUENCY 5% AND 1% THD



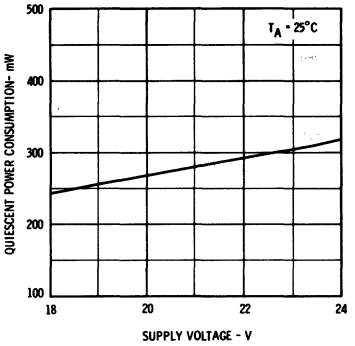
RELATIVE VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



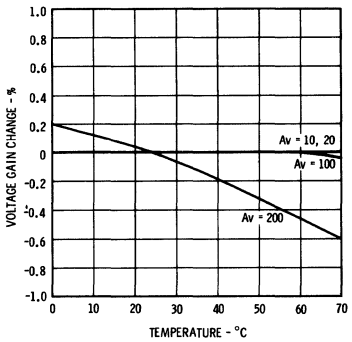
VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



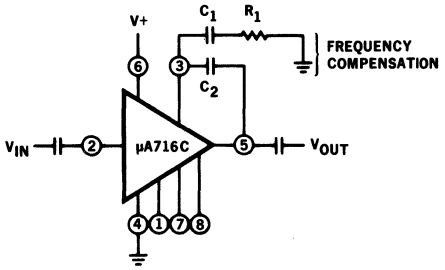
QUIESCENT POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



RELATIVE VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



CONNECTION DIAGRAM AND COMPONENT TABLE FOR AVAILABLE GAIN OPTIONS



Voltage Gain	C_1	C_2	R_1	Decouple Pins:
10	68 pF	39 pF	75 Ω	1
20	50 pF	27 pF	75 Ω	8
100	None	3 pF	None	1, 7
200	None	3 pF	None	7, 8

TABLE I

DEFINITION OF TERMS

Quiescent Power Consumption — The DC power required to operate the amplifier with no signal applied at the input and the load current equal to zero.

Total Harmonic Distortion — The ratio of the sum of the amplitudes of all signals harmonically related to the fundamental, and the amplitude of the fundamental signal.

Input Noise Voltage — The noise voltage at the output of the amplifier, divided by the amplifier voltage gain.

Output Voltage Swing — The maximum output voltage that may be obtained at the output of the amplifier before saturation occurs.

Input Resistance — The small-signal resistance seen looking into the input terminal of the amplifier.

Voltage Gain — The ratio of the small-signal output voltage to the input voltage of the amplifier.

Temperature Stability of Voltage Gain — The maximum variation of the voltage gain over the specified temperature range.

μA717E

MULTI-PURPOSE AMPLIFIER

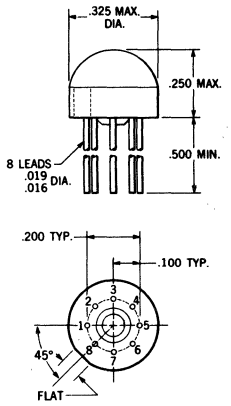
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA717E is a multi-purpose circuit designed primarily for TV sound systems and general FM-audio applications. In TV sound systems it functions as a 4.5 MHz amplifier, limiter and FM detector (simple quadrature type), audio preamplifier and driver. Special features of the μA717E include (a) operation at supply voltages from 6 to 15 volts with simple rebiasing by the use of an external resistor, and (b) the option of using the microcircuit without the quadrature detector as a high gain amplifier from 100 kHz to 50 MHz.

ABSOLUTE MAXIMUM RATINGS:

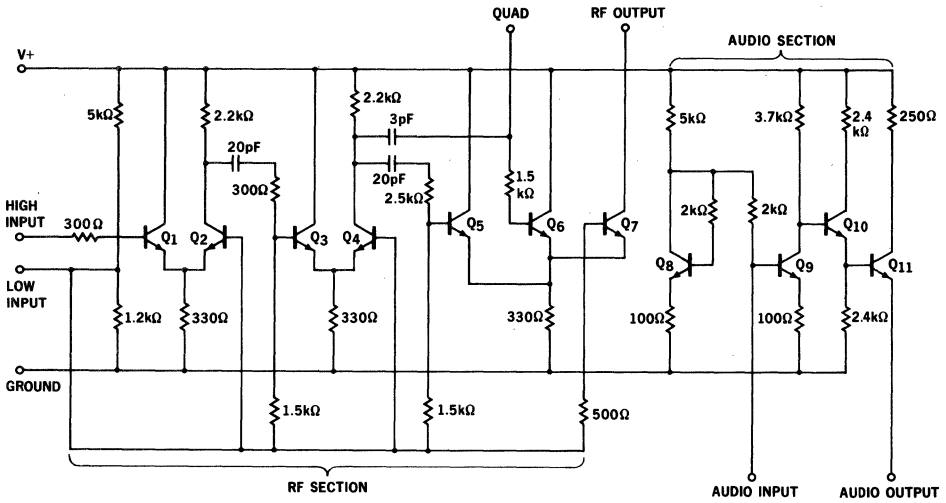
Supply Voltage	15 V
Output Collector Voltage (RF Section)	20 V
Voltage Between "High Input" and "Low Input" Terminals	±5 V
Power Dissipation (Note 1)	350 mW
Maximum Internal Temperature (Note 2)	125°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 10 second time limit)	300°C

PHYSICAL DIMENSIONS

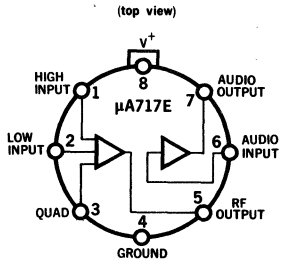


ORDER PART NO. U8A771739X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



NOTES:
(1) Rating applies for ambient temperatures from 0°C to +70°C.
(2) Derate maximum dissipation by 6.4 mW/°C above 70°C.

FAIRCHILD SEMICONDUCTOR
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313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

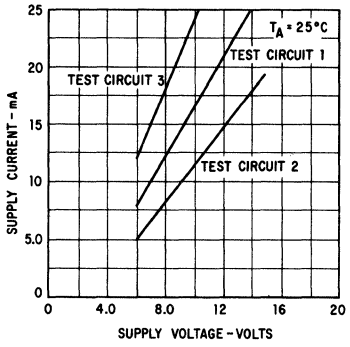
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12V$, Test Circuit 4 unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Total Supply Current			21		mA
Power Consumption			250	350	mW
Audio Output D-C Bias Voltage		2.0	2.6	3.2	V
Voltage Gain of Audio Section			35		
Audio Output Drive Current (clipping)	Audio output load 250Ω applied between pin 7 and ground		20		mA peak
Input Voltage for −3 dB Limiting	f = 4.5 MHz Test Circuit 9		1.5	5.0	mV rms
Noise Figure	$R_S = 1k\Omega$, f = 4.5 MHz Test Circuit 10		7.0		dB
Noise Figure	$R_S = 1k\Omega$, f = 10.7 MHz Test Circuit 10		7.0		dB

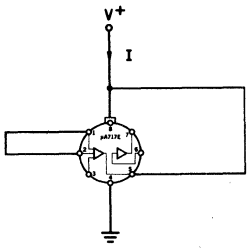
PARAMETER	TEST CONDITION		@ f = 4.5 MHz MIN.	TYP.	MAX.	@ f = 10.7 MHz MIN.	TYP.	MAX.	UNITS
Input Conductance	$e_{in} \leq 20$ mV rms	Test Circuit 5		0.21			0.35		mmho
Input Capacitance	$e_{in} \leq 20$ mV rms	Test Circuit 5		12			10		pF
Output Conductance		Test Circuit 6		0.05			0.1		mmho
Output Capacitance		Test Circuit 6		6.0			5.0		pF
Forward Transadmittance		Test Circuit 8		2200			1200		mmho
Gain Maximum Stable (GMS)		Test Circuit 10		80			80		dB
Gain Maximum Available (GMA)		Test Circuit 10		81			71		dB
Quadrature Conductance	$e_{in} \leq 20$ mV rms	Test Circuit 7		0.22			0.35		mmho
Quadrature Capacitance	$e_{in} \leq 20$ mV rms	Test Circuit 7		9.5			8.0		pF

TYPICAL PERFORMANCE CURVES

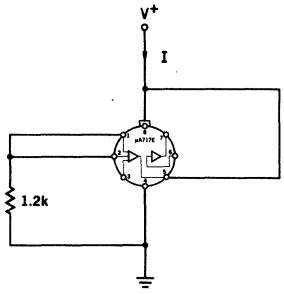
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



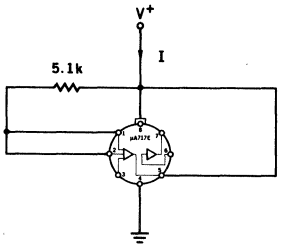
TEST CIRCUIT 1



TEST CIRCUIT 2



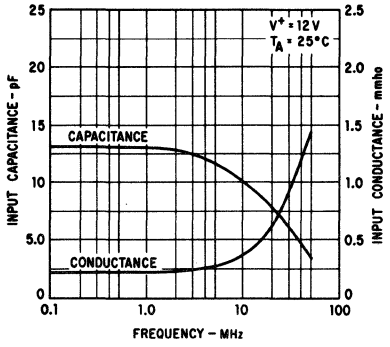
TEST CIRCUIT 3



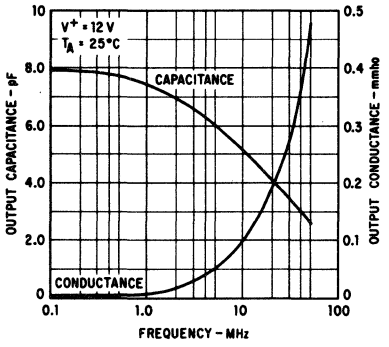
TOTAL SUPPLY CURRENT

TYPICAL PERFORMANCE CURVES

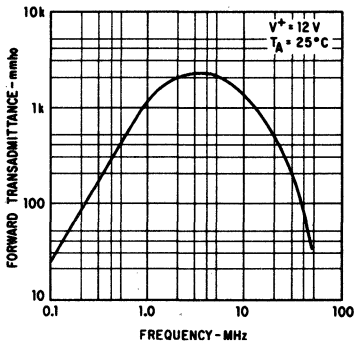
INPUT CONDUCTANCE AND CAPACITANCE AS A FUNCTION OF FREQUENCY



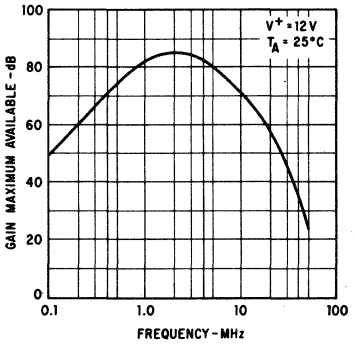
OUTPUT CONDUCTANCE AND CAPACITANCE AS A FUNCTION OF FREQUENCY



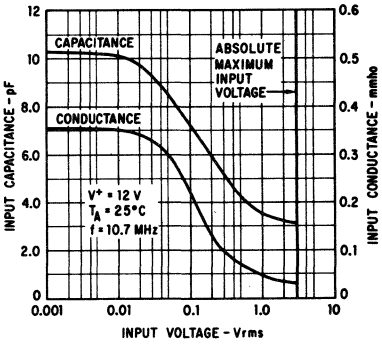
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



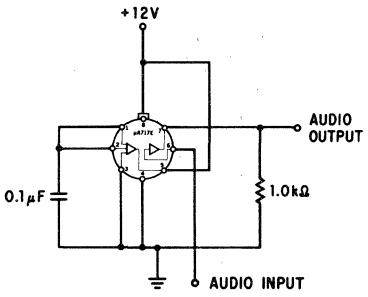
GAIN MAXIMUM AVAILABLE (GMA) AS A FUNCTION OF FREQUENCY



INPUT CONDUCTANCE AND CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE

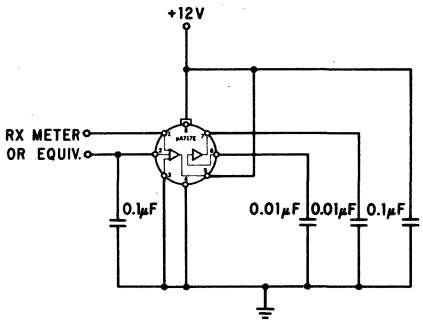


TEST CIRCUIT 4



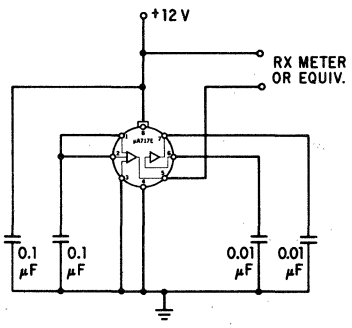
DC AND AUDIO GAIN TEST CIRCUIT

TEST CIRCUIT 5



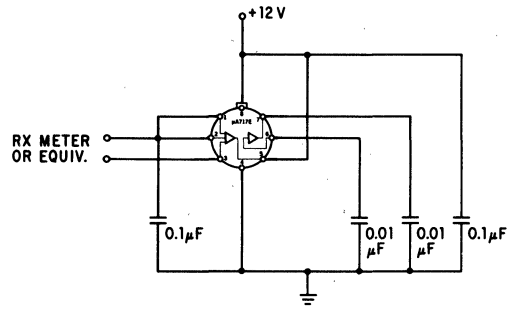
INPUT CONDUCTANCE AND CAPACITANCE MEASUREMENT CIRCUIT

TEST CIRCUIT 6



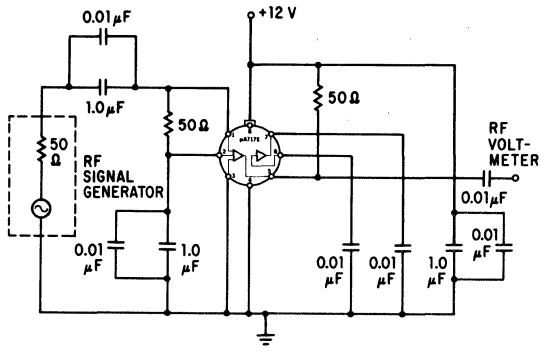
OUTPUT CONDUCTANCE AND CAPACITANCE MEASUREMENT CIRCUIT

TEST CIRCUIT 7



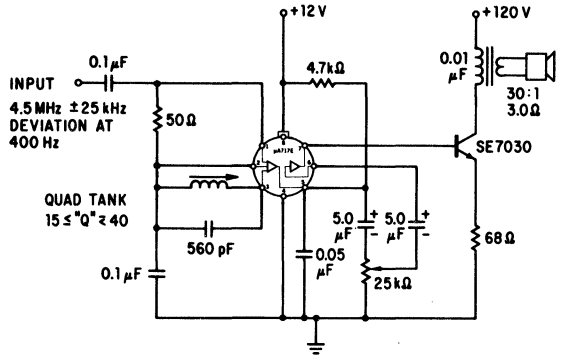
QUADRATURE CONDUCTANCE AND CAPACITANCE MEASUREMENT CIRCUIT

TEST CIRCUIT 8



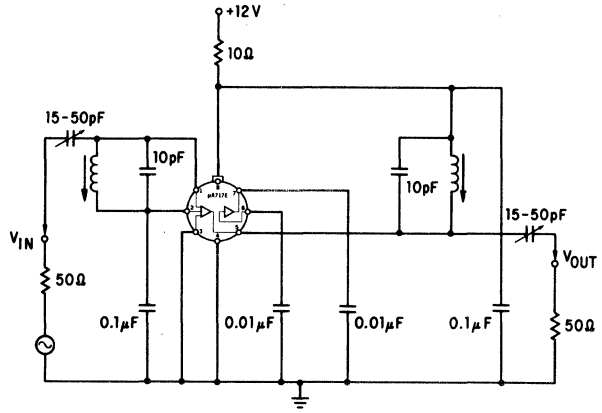
FORWARD TRANSADMITTANCE MEASUREMENT CIRCUIT

TEST CIRCUIT 9



TV SOUND SYSTEM

TEST CIRCUIT 10



MEASUREMENT CIRCUIT
NOISE FIGURE
GAIN MAXIMUM STABLE
GAIN MAXIMUM AVAILABLE

DEFINITION OF TERMS

POWER CONSUMPTION — The total power consumption of Test Circuit 1.

GAIN MAXIMUM STABLE (GMS) — This gain figure gives the maximum possible gain based on stability criteria only. This gain figure does not necessarily represent the realizable power gain of an amplifier. For unneutralized amplifiers, the maximum practical power gain realizable based on normal circuit tolerances is either (GMS – 6 dB) or GMA, whichever is smaller.

GAIN MAXIMUM AVAILABLE (GMA) — This gain figure is the theoretical maximum power gain of an amplifier with conjugate matching at both the input and terminals and assumes no reverse transadmittance (feedback component) in the amplifier.

INPUT LIMITING VOLTAGE — Referring to Test Circuit 9; set 25 kilohm potentiometer to give 1 watt audio output power into speaker with an input signal of 50 mV rms. The –3 dB input limiting voltage is defined as the value of the input voltage when the audio output power has fallen to 0.5 watt. For further information on the μA717E refer to Fairchild Application Bulletin No. 158, — "Two High Performance Monolithic Microcircuits For FM Sound Systems." by David Bingham.

μA719

HIGH GAIN RF AMPLIFIER/FM DETECTOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

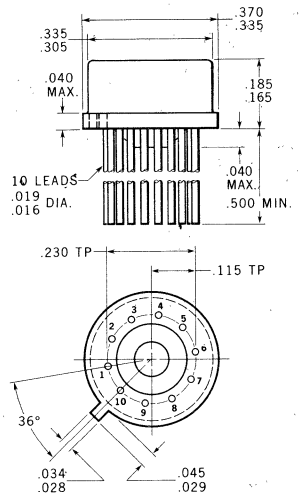
- **HIGH GAIN AT 10.7 MHz**
- **AGC RANGE > 30 dB**
- **TWO SEPARATE AMPLIFIERS**
- **SUPPLY VOLTAGE 5 TO 15 VOLTS**
- **OPTIONAL FM QUADRATURE DETECTOR**

GENERAL DESCRIPTION — The μA719 is a high gain RF amplifier/FM detector which contains two independent amplifier sections designed for IF systems to 50 MHz. Section 1 utilizes three cascaded emitter coupled amplifiers having high gain and a reverse AGC capability. In addition, Section 1 may be used as an amplifier limiter and quadrature detector for FM systems. Section 2 is a single stage amplifier useful from DC to 50 MHz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	15 V
Output Collector Voltage (Section 1)	20 V
Voltage between "High Input 1" and "Low Input 1" Terminals	±5.0 V
Voltage between "Quad" and "Ground" Terminals	0 to +4.0 V
Voltage between "Input 2" and "Ground" Terminals	±2.0 V
Power Dissipation (Note 1)	350 mW
Maximum Chip Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 second time limit)	300°C

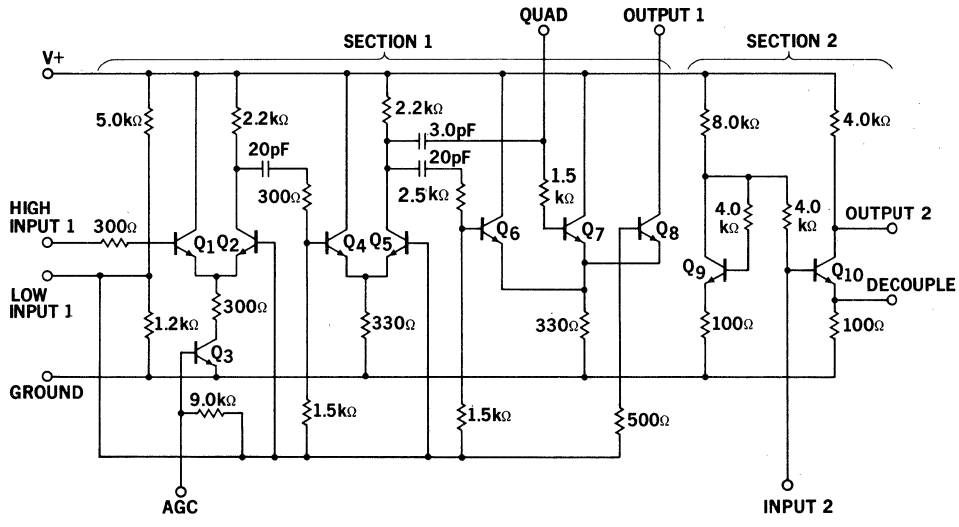
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO−100)



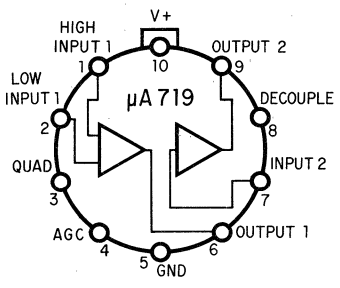
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART NO.
U5F7719312

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



NOTE:

(1) Rating applies for ambient temperatures to +125°C if the package case to ambient thermal resistance is lowered to 40°C/Watt by the addition of a heat dissipator. Derate linearly 5.6 mW/°C for ambient temperatures above 87°C.

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313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

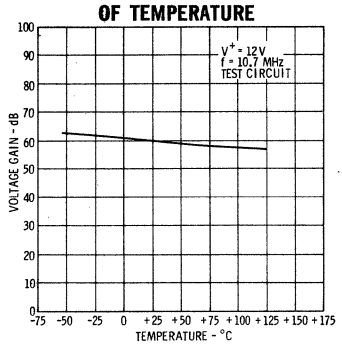
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12$ V, Test Circuit 1 unless otherwise specified)

PARAMETER (See Definitions)	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$T_A = +25°C$	12	18	25	mA
	$T_C = -55°C$		17.5		mA
	$T_C = +125°C$		17		mA
Supply Current	$V^+ = 9.0$ V,	6.0	12.5	18.5	mA
Power Dissipation	$T_A = +25°C$	144	216	300	mW
	$T_C = -55°C$		210		mW
	$T_C = +125°C$		204		mW
Power Dissipation	$V^+ = 9.0$ V,	54	113	167	mW
Section 1 Quiescent Output Current		1.0	2.5	4.0	mA
Section 1 DC Voltage at AGC Terminal		0.55	0.73	1.25	V
Section 1 AGC Current For 30 dB AGC	f = 10.7 MHz, Test Circuit 3		170	250	μA
Section 1 Output Current	f = 1.0 MHz, Test Circuit 8		4.4		mA_{p-p}
Section 1 Voltage Gain	f = 10.7 MHz, Test Circuit 3				
	$T_A = +25°C$	53	60		dB
	$T_C = -55°C$		63		dB
	$T_C = +125°C$		58		dB
Section 1 Voltage Gain	f = 10.7 MHz, Test Circuit 3, $V^+ = 9.0$ V		53		dB
Section 1 Input Voltage For −3.0 dB Limiting	f = 4.5 MHz, Test Circuit 4		1.5	4.0	mV
Section 1 Noise Figure	$R_S = 1.0$ kΩ, Test Circuit 5				
	f = 4.5 MHz		7.0		dB
	f = 10.7 MHz		7.0		dB
Section 2 DC Voltage at Output 2		5.2	6.3	7.4	V
Section 2 Voltage Gain	f = 1.0 kHz, Test Circuit 2	22	31		dB
Section 2 Voltage at Output 2 Without Clipping	f = 1.0 kHz, Test Circuit 2		10		V_{p-p}

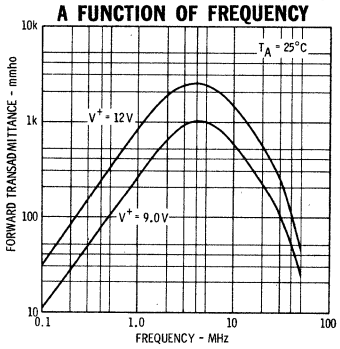
PARAMETERS (See Definitions)	TEST CONDITIONS	f = 4.5 MHz TYP.	f = 10.7 MHz TYP.	UNITS
SECTION 1				
Input Conductance	$e_{IN} \leq 20$ mV Test Circuit 6	170	300	μmho
Input Capacitance	$e_{IN} \leq 20$ mV Test Circuit 6	7.5	6.3	pF
Output Conductance	Test Circuit 7	50	130	μmho
Output Capacitance	Test Circuit 7	6.7	5.4	pF
Forward Transadmittance	Test Circuit 8	2200	1400	mmho
Forward Transadmittance	Test Circuit 8 $V^+ = 9.0$ V	1000	600	mmho
Quad Conductance	Test Circuit 9	200	330	μmho
Quad Capacitance	Test Circuit 9	8.0	7.0	pF
Gain Maximum Available (GMA)	Test Circuit 5	83	71	dB
Gain Maximum Stable (GMS)	Test Circuit 5	85	78	dB
SECTION 2				
Input Conductance	Test Circuit 10			
	Pin #8 Unbypassed	300	300	μmho
	Pin #8 Bypassed	360	460	μmho
Input Capacitance	Test Circuit 10			
	Pin #8 Unbypassed	3.3	3.3	pF
	Pin #8 Bypassed	10.4	8.7	pF
Output Conductance	Test Circuit 11			
	Pin #8 Unbypassed	250	260	μmho
	Pin #8 Bypassed	270	340	μmho
Output Capacitance	Test Circuit 11			
	Pin #8 Unbypassed	5.2	5.2	pF
	Pin #8 Bypassed	8.9	8.0	pF
Forward Transadmittance	Test Circuit 12			
	Pin #8 Unbypassed	8.0	8.0	mmho
	Pin #8 Bypassed	34	34	mmho
Gain Maximum Available (GMA)	Pin #8 Unbypassed	24	24	dB
	Pin #8 Bypassed	35	32	dB

TYPICAL PERFORMANCE CURVES

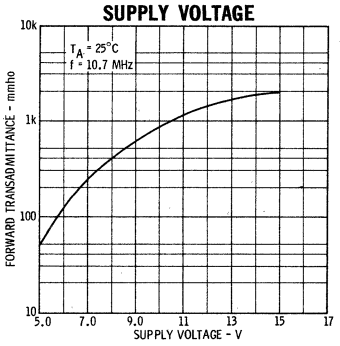
SECTION 1
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



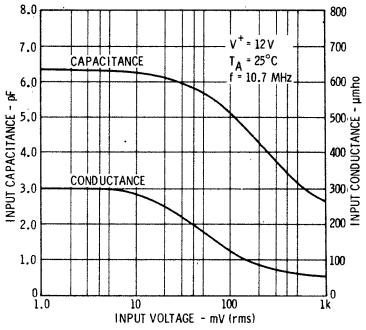
SECTION 1
FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



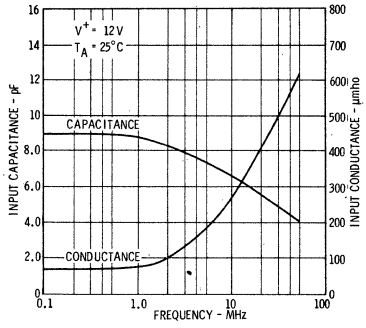
SECTION 1
FORWARD TRANSADMITTANCE AS A FUNCTION OF SUPPLY VOLTAGE



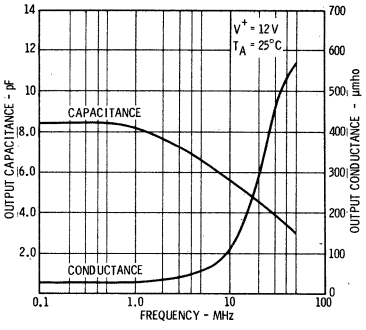
SECTION 1
INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE



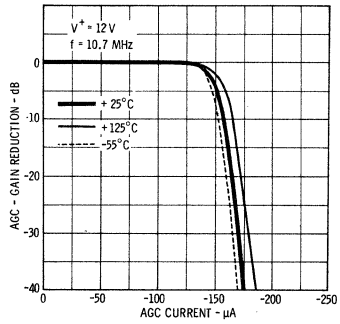
SECTION 1
INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



SECTION 1
OUTPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



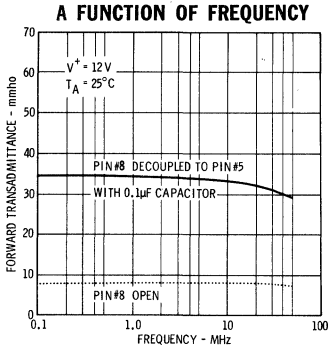
SECTION 1
AGC AS A FUNCTION OF AGC CURRENT



TYPICAL PERFORMANCE CURVES

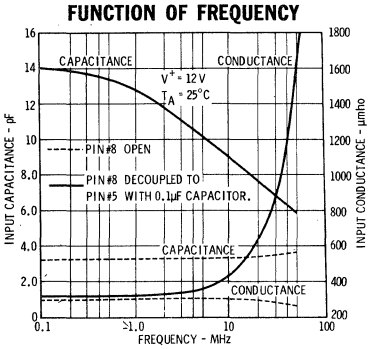
SECTION 2

FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



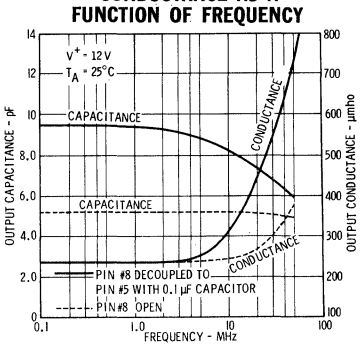
SECTION 2

INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY

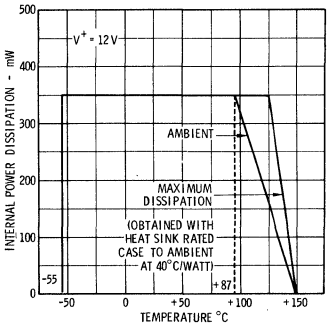


SECTION 2

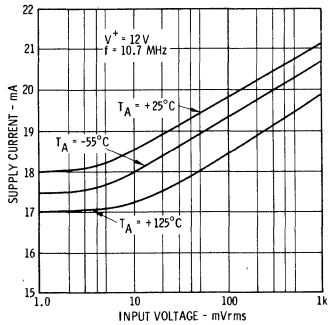
OUTPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



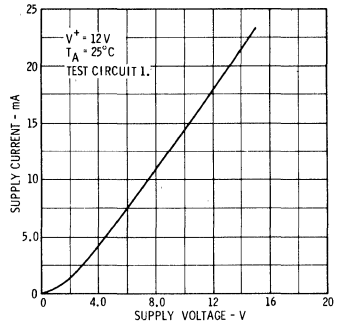
MAXIMUM INTERNAL DISSIPATION AS A FUNCTION OF EITHER AMBIENT OR CASE TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF INPUT 1 SIGNAL VOLTAGE



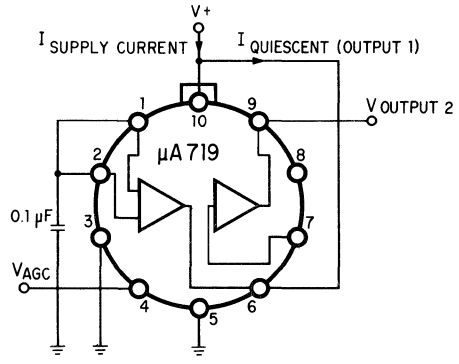
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



TEST CIRCUITS

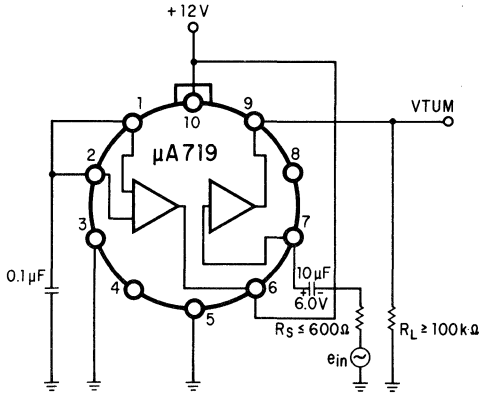
TEST CIRCUIT 1

DC MEASUREMENTS



TEST CIRCUIT 2

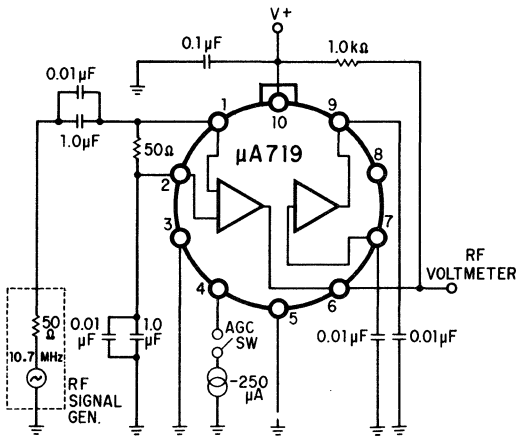
SECTION 2 GAIN AND OUTPUT VOLTAGE SWING



TEST CIRCUITS

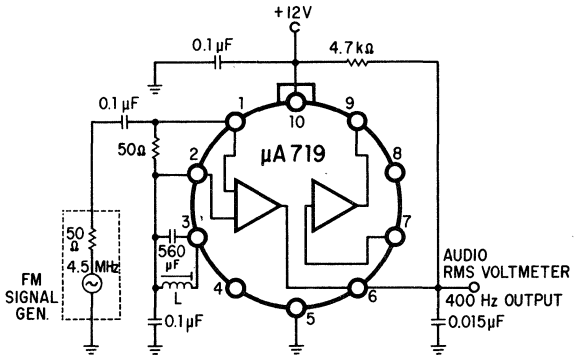
TEST CIRCUIT 3

10.7 MHz VOLTAGE GAIN AND AGC



TEST CIRCUIT 4

-3.0 dB LIMITING AT 4.5 MHz USING A QUADRATURE DETECTOR*

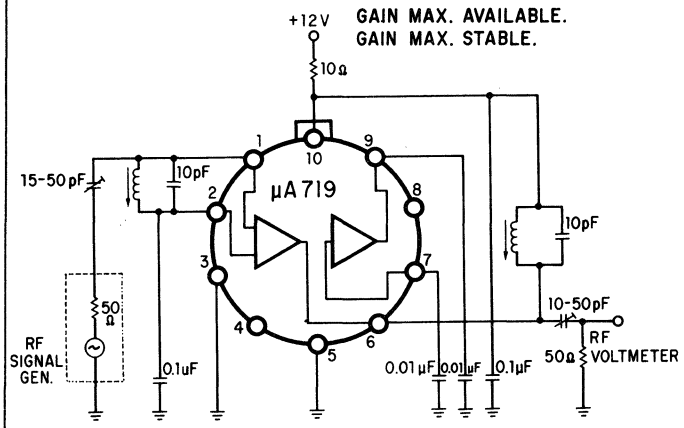


INPUT SIGNAL 4.5 MHz 25kHz DEVIATION AT 400 Hz. UNLOADED QUALITY FACTOR OF QUADRATURE TANK INDUCTOR IS 65.

*SEE DEFINITIONS

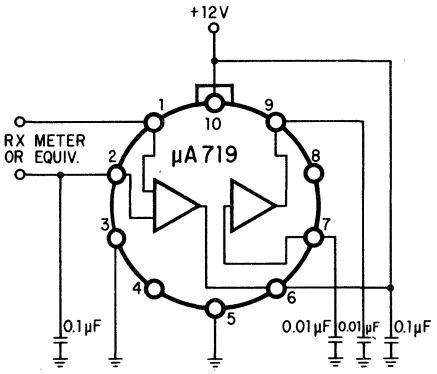
TEST CIRCUIT 5

SECTION 1: NOISE FIGURE.
GAIN MAX. AVAILABLE.
GAIN MAX. STABLE.



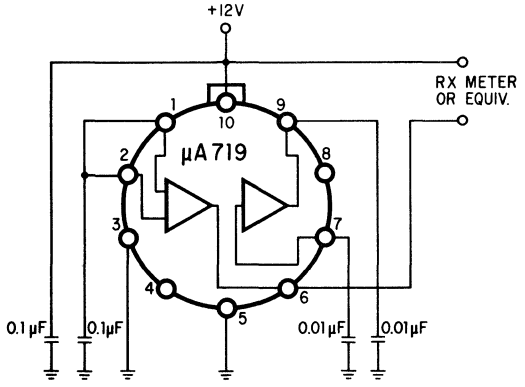
TEST CIRCUIT 6

SECTION 1 INPUT PARAMETERS



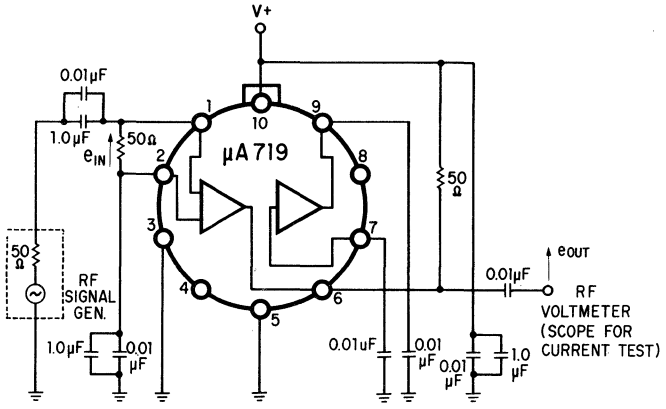
TEST CIRCUIT 7

SECTION 1 OUTPUT PARAMETERS



TEST CIRCUIT 8

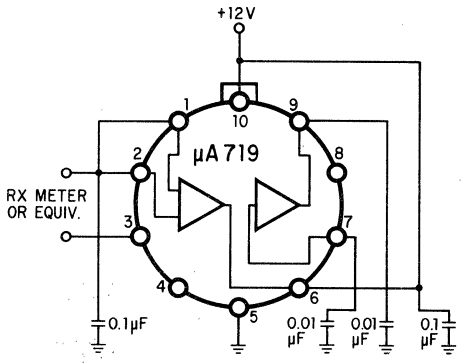
SECTION 1 FORWARD TRANSADMITTANCE OUTPUT CURRENT



FORWARD TRANSADMITTANCE = $\frac{e_{OUT}}{e_{IN}} \cdot \frac{1}{50} \cdot 10^3$ mmho

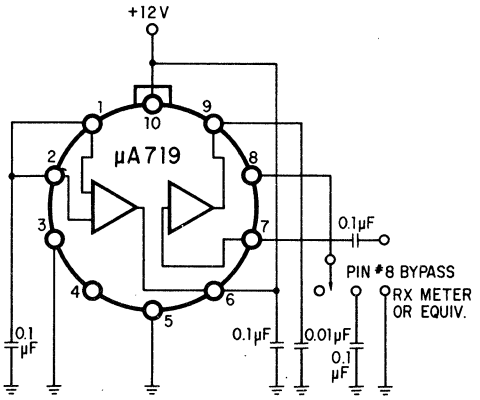
TEST CIRCUIT 9

SECTION 1 QUAD PARAMETERS



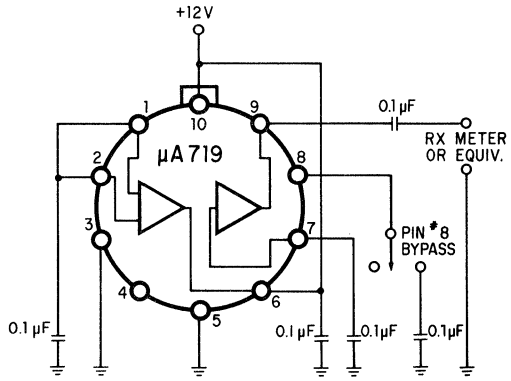
TEST CIRCUIT 10

SECTION 2 INPUT PARAMETERS



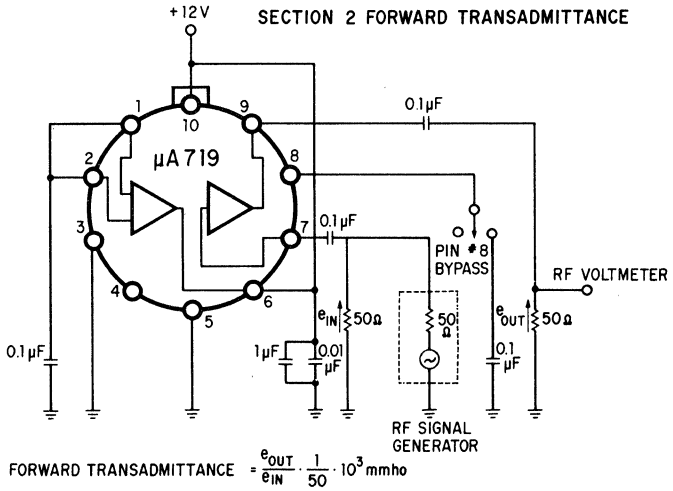
TEST CIRCUIT 11

SECTION 2 OUTPUT PARAMETERS



TEST CIRCUIT 12

SECTION 2 FORWARD TRANSADMITTANCE



FORWARD TRANSADMITTANCE $= \frac{e_{OUT}}{e_{IN}} \cdot \frac{1}{50} \cdot 10^3$ mmho

DEFINITION OF TERMS

Gain Maximum Available (GMA) — This gain figure is the theoretical maximum power gain of an amplifier with conjugate matching at both the input and the output terminals and assumes no reverse transadmittance (feedback component) in the amplifier.

$$GMA = \frac{|\text{forward transadmittance}|^2}{4 \times \text{input conductance} \times \text{output conductance}}$$

Gain Maximum Stable (GMS) — This gain figure gives the maximum possible gain based on stability criteria only. This gain figure does not necessarily represent the realizable power gain of an amplifier. For unneutralized amplifiers, the maximum power gain realizable based on normal circuit tolerances is either (GMS - 6.0 dB) or GMA, whichever is smaller.

$$GMS = \frac{|\text{forward transadmittance}|}{|\text{reverse transadmittance}|}$$

Input Voltage For —3.0 dB Limiting — Refer to Test Circuit 4 which shows the μA719 being used as an amplifier, limiter, and FM detector (simple quadrature type with the LC tank circuit connected between pins No. 3 and No. 2). An input FM signal (carrier frequency 4.5 MHz, ±25 kHz deviation at 400 Hz) of 50 mV rms is applied to the μA719 and the value of the recovered audio output signal (400 Hz) at pin No. 6 is noted. The —3.0 dB input limiting voltage is defined as the value of the input voltage to produce an output voltage 3dB below the output level obtained with 50 mV rms of input signal.

μA719C

HIGH GAIN RF AMPLIFIER/FM DETECTOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

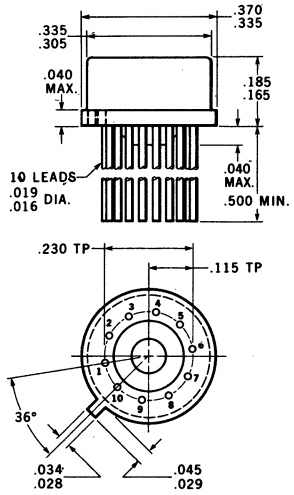
- **HIGH GAIN AT 10.7 MHz**
- **AGC RANGE > 30 dB**
- **TWO SEPARATE AMPLIFIERS**
- **SUPPLY VOLTAGE 5 TO 15 VOLTS**
- **OPTIONAL FM QUADRATURE DETECTOR**

GENERAL DESCRIPTION — The μA719C is a high gain RF amplifier/FM detector which contains two independent amplifier sections designed for IF systems to 50 MHz. Section 1 utilizes three cascaded emitter coupled amplifiers having high gain and a reverse AGC capability. In addition, Section 1 may be used as an amplifier limiter and quadrature detector for FM systems. Section 2 is a single stage amplifier useful from DC to 50 MHz.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	15 V
Output Collector Voltage (Section 1)	20 V
Voltage between "High Input 1" and "Low Input 1" Terminals	±5.0 V
Voltage between "Quad" and "Ground" Terminals	0 to +4.0 V
Voltage between "Input 2" and "Ground" Terminals	±2.0 V
Power Dissipation	350 mW
Maximum Chip Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 second time limit)	300°C

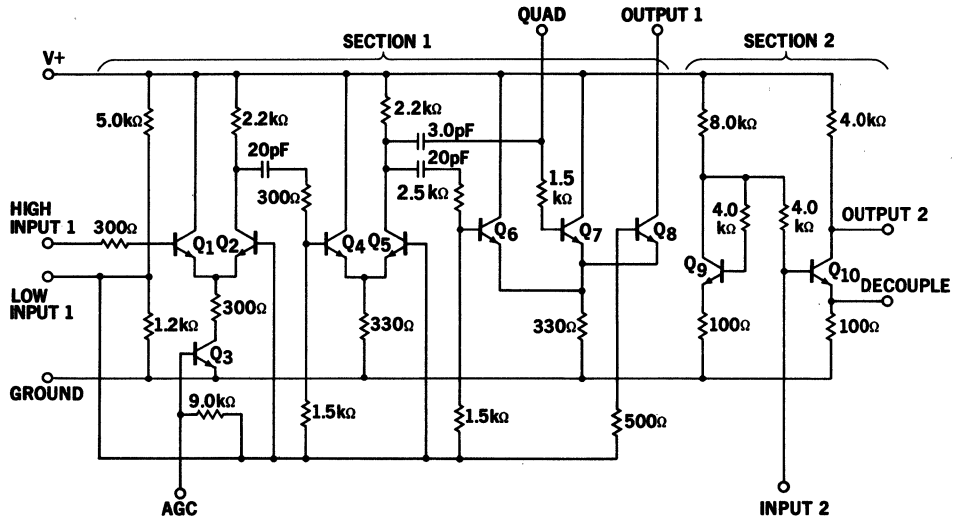
PHYSICAL DIMENSIONS
(In accordance with JEDEC TO—100)



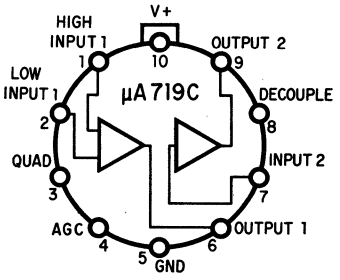
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

ORDER PART NO.
U5F7719393

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



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FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

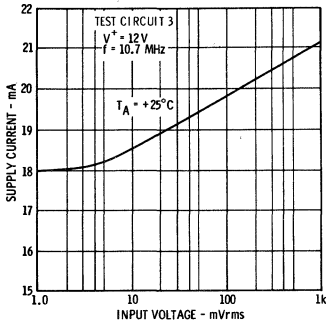
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 12$ V, Test Circuit 1 unless otherwise specified)

PARAMETER (See Definitions)	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$T_A = +25°C$	12	18	25	mA
	$T_A = 0°C$	10	17.5	27	mA
	$T_A = +70°C$	10	17	25	mA
Supply Current	$V^+ = 9.0$ V	6.0	12.5	18.5	mA
Supply Current	$V^+ = 6.0$ V, $70°C \leq T_A \leq 0°C$	3.0	6.0	10	mA
Power Dissipation	$T_A = +25°C$	144	216	300	mW
	$T_A = 0°C$	120	210	324	mW
	$T_A = +70°C$	120	204	300	mW
Power Dissipation	$V^+ = 9.0$ V	54	113	167	mW
Power Dissipation	$V^+ = 6.0$ V, $70°C \leq T_A \leq 0°C$	18	36	60	mW
Section 1 Quiescent Output Current		1.0	2.5	4.0	mA
Section 1 DC Voltage at AGC Terminal		0.55	0.73	1.25	V
Section 1 AGC Current For 30 dB AGC	f = 10.7 MHz, Test Circuit 3		170	250	μA
Section 1 Output Current	f = 1.0 MHz, Test Circuit 8		4.4		mA_{p-p}
Section 1 Voltage Gain	f = 10.7 MHz, Test Circuit 3				
	$T_A = +25°C$	50	60	70	dB
	$T_A = 0°C$	50	61	70	dB
	$T_A = +70°C$	48	59	70	dB
Section 1 Voltage Gain	f = 10.7 MHz, Test Circuit 3, $V^+ = 9.0$ V		53		dB
Section 1 Voltage Gain	f = 10.7 MHz, Test Circuit 3, $V^+ = 6.0$ V		38		dB
Section 1 Input Voltage For −3.0 dB Limiting	f = 4.5 MHz, Test Circuit 4		1.5	6.5	mV
Section 1 Noise Figure	$R_S = 1.0$ kΩ, Test Circuit 5				
	f = 4.5 MHz		7.0		dB
	f = 10.7 MHz		7.0		dB
Sections 1 and 2 Cascaded Voltage Gain	f = 10.7 MHz, Test Circuit 13				
	$V^+ = 6.0$ V, R = 3.0 kΩ				
	Pin #8 Unbypassed		51		dB
	Pin #8 Bypassed		56		dB
Section 2 DC Voltage at Output 2		5.2	6.3	7.4	V
Section 2 Voltage Gain	f = 1.0 kHz, Test Circuit 2	22	31	40	dB
Section 2 Voltage at Output 2 Without Clipping	f = 1.0 kHz, Test Circuit 2	7.0	10	11.5	V_{p-p}

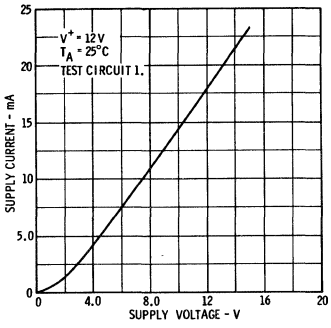
PARAMETERS (See Definitions)	TEST CONDITIONS	f = 4.5 MHz TYP.	f = 10.7 MHz TYP.	UNITS
SECTION 1				
Input Conductance	Test Circuit 6, $e_{IN} \leq 20$ mV	170	300	μmho
Input Capacitance	Test Circuit 6, $e_{IN} \leq 20$ mV	7.5	6.3	pF
Output Conductance	Test Circuit 7	50	130	μmho
Output Capacitance	Test Circuit 7	6.7	5.4	pF
Forward Transadmittance	Test Circuit 8	2200	1400	mmho
Forward Transadmittance	Test Circuit 8, $V^+ = 9.0$ V	1000	600	mmho
Forward Transadmittance	Test Circuit 8, $V^+ = 6.0$ V	180	100	mmho
Quad Conductance	Test Circuit 9	200	330	μmho
Quad Capacitance	Test Circuit 9	8.0	7.0	pF
Gain Maximum Available (GMA)	Test Circuit 5	83	71	dB
Gain Maximum Stable (GMS)	Test Circuit 5	85	78	dB
SECTION 2	Test Circuit 10			
Input Conductance	Pin #8 Unbypassed	300	300	μmho
	Pin #8 Bypassed	360	460	μmho
Input Capacitance	Test Circuit 10			
	Pin #8 Unbypassed	3.3	3.3	pF
	Pin #8 Bypassed	10.4	8.7	pF
Output Conductance	Test Circuit 11			
	Pin #8 Unbypassed	250	260	μmho
	Pin #8 Bypassed	270	340	μmho
Output Capacitance	Test Circuit 11			
	Pin #8 Unbypassed	5.2	5.2	pF
	Pin #8 Bypassed	8.9	8.0	pF
Forward Transadmittance	Test Circuit 12			
	Pin #8 Unbypassed	8.0	8.0	mmho
	Pin #8 Bypassed	34	34	mmho
Gain Maximum Available (GMA)	Pin #8 Unbypassed	24	24	dB
	Pin #8 Bypassed	35	32	dB

TYPICAL PERFORMANCE CURVES

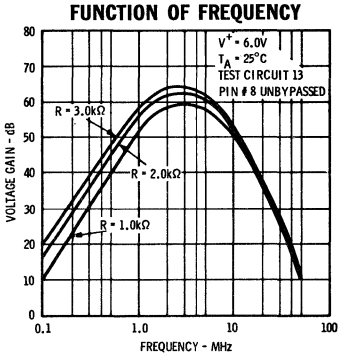
SECTIONS 1 AND 2 SUPPLY CURRENT AS A FUNCTION OF INPUT 1 SIGNAL VOLTAGE



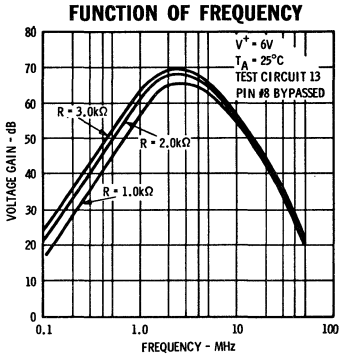
SECTIONS 1 AND 2 SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



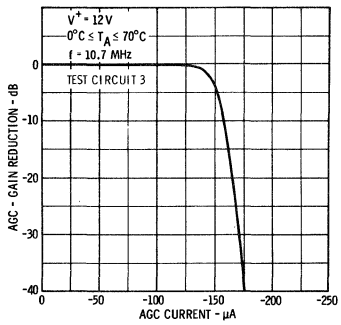
SECTIONS 1 AND 2 CASCADED VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



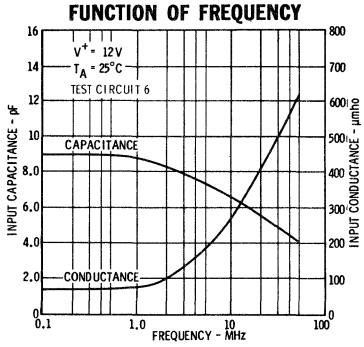
SECTIONS 1 AND 2 CASCADED VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



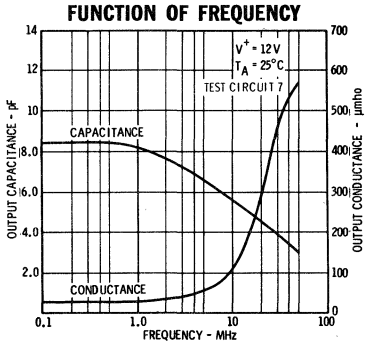
SECTION 1 AGC AS A FUNCTION OF AGC CURRENT



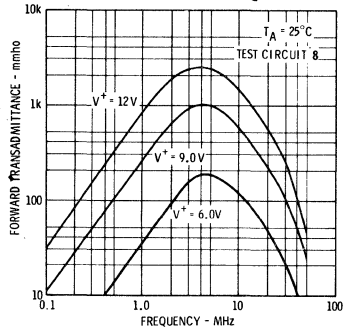
SECTION 1 INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



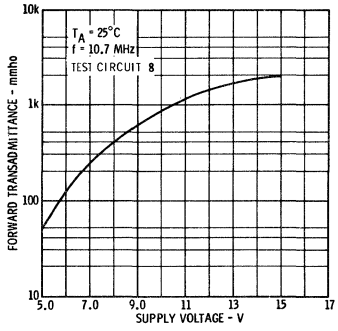
SECTION 1 OUTPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



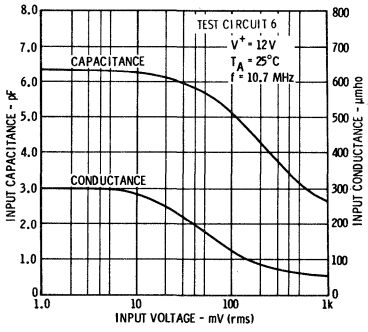
SECTION 1 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



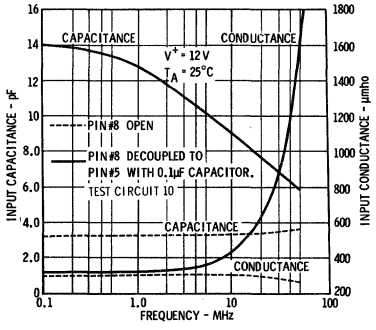
SECTION 1 FORWARD TRANSADMITTANCE AS A FUNCTION OF SUPPLY VOLTAGE



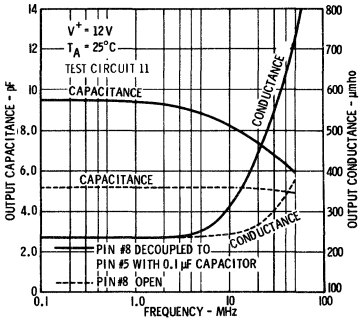
SECTION 1 INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF INPUT SIGNAL VOLTAGE



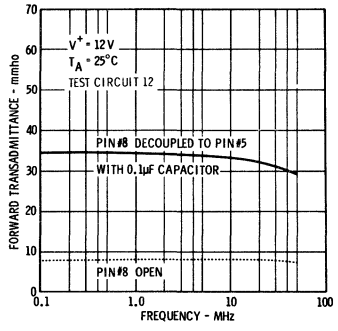
SECTION 2 INPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



SECTION 2 OUTPUT CAPACITANCE AND CONDUCTANCE AS A FUNCTION OF FREQUENCY



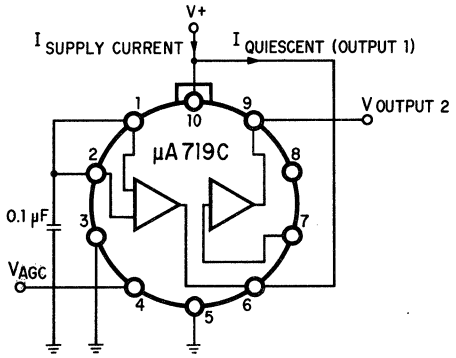
SECTION 2 FORWARD TRANSADMITTANCE AS A FUNCTION OF FREQUENCY



TEST CIRCUITS

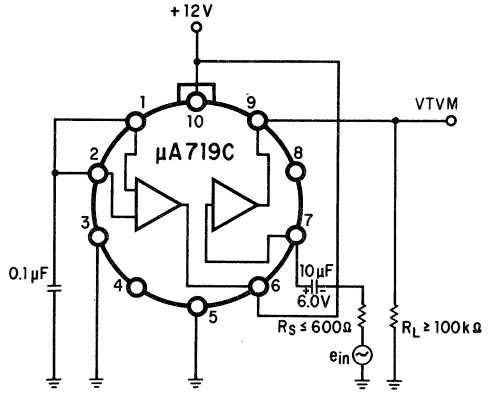
TEST CIRCUIT 1

DC MEASUREMENTS



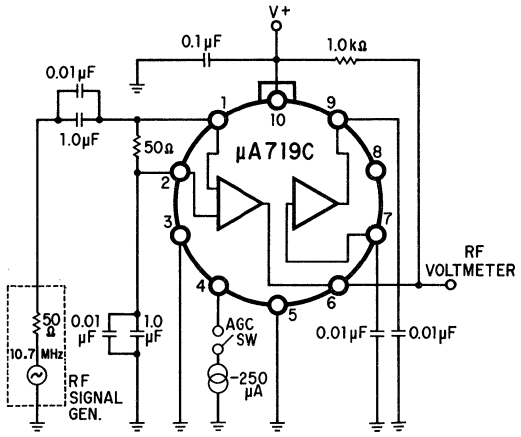
TEST CIRCUIT 2

SECTION 2 GAIN AND OUTPUT VOLTAGE SWING



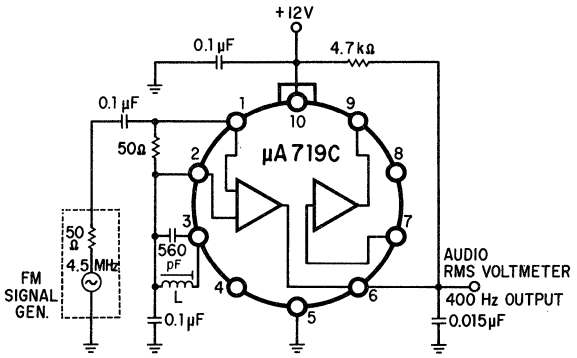
TEST CIRCUIT 3

10.7 MHz VOLTAGE GAIN AND AGC



TEST CIRCUIT 4

-3.0dB LIMITING AT 4.5 MHz USING A QUADRATURE DETECTOR*

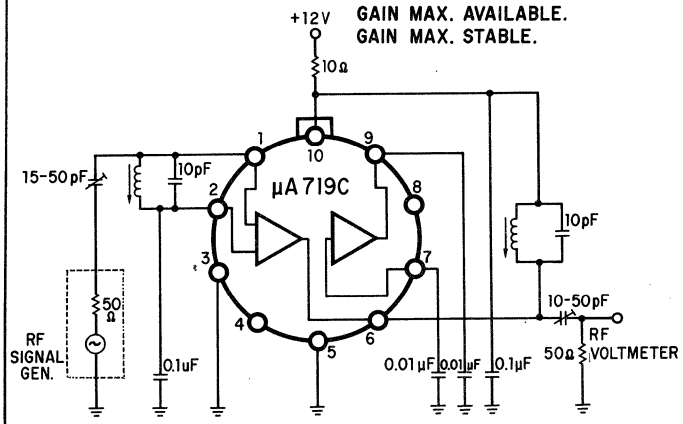


INPUT SIGNAL 4.5 MHz 25kHz DEVIATION AT 400 Hz. UNLOADED QUALITY FACTOR OF QUADRATURE TANK INDUCTOR IS 22.

*SEE DEFINITIONS

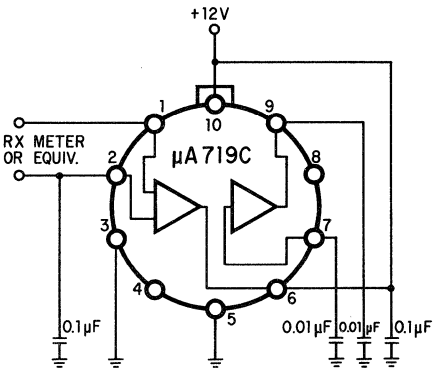
TEST CIRCUIT 5

SECTION 1: NOISE FIGURE.
GAIN MAX. AVAILABLE.
GAIN MAX. STABLE.



TEST CIRCUIT 6

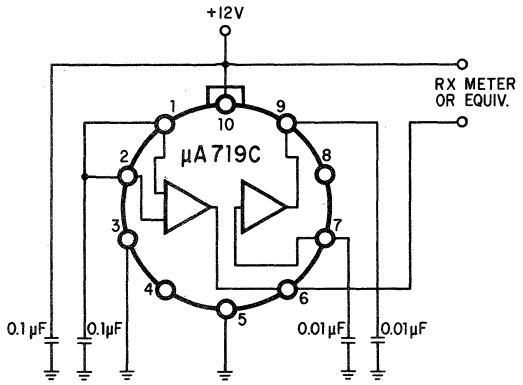
SECTION 1 INPUT PARAMETERS



TEST CIRCUITS

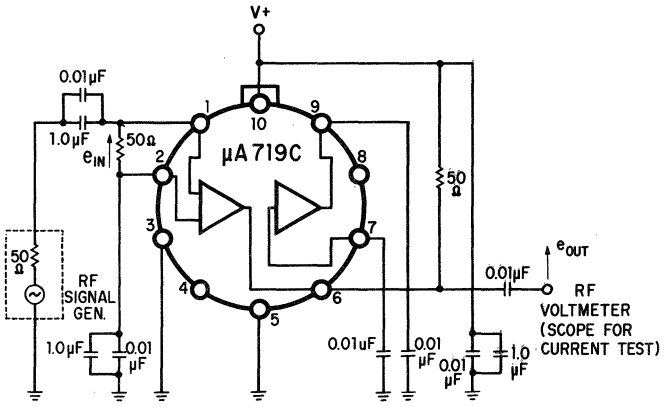
TEST CIRCUIT 7

SECTION 1 OUTPUT PARAMETERS



TEST CIRCUIT 8

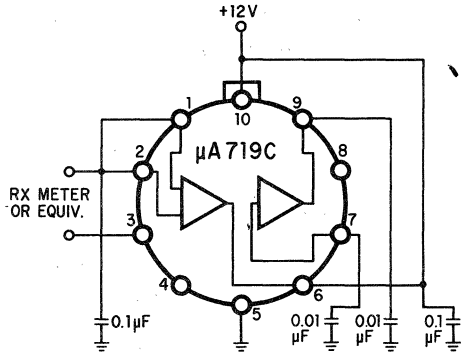
SECTION 1 FORWARD TRANSADMITTANCE OUTPUT CURRENT



FORWARD TRANSADMITTANCE = $\frac{e_{OUT}}{e_{IN}} \cdot \frac{1}{50} \cdot 10^3$ mmho

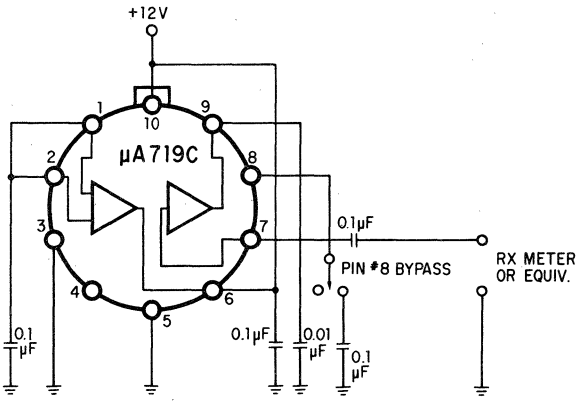
TEST CIRCUIT 9

SECTION 1 QUAD PARAMETERS



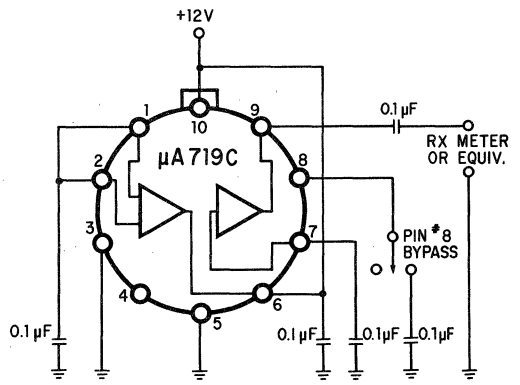
TEST CIRCUIT 10

SECTION 2 INPUT PARAMETERS



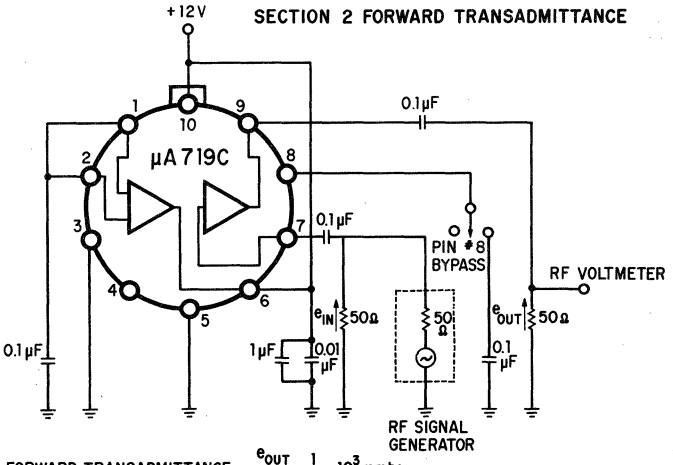
TEST CIRCUIT 11

SECTION 2 OUTPUT PARAMETERS



TEST CIRCUIT 12

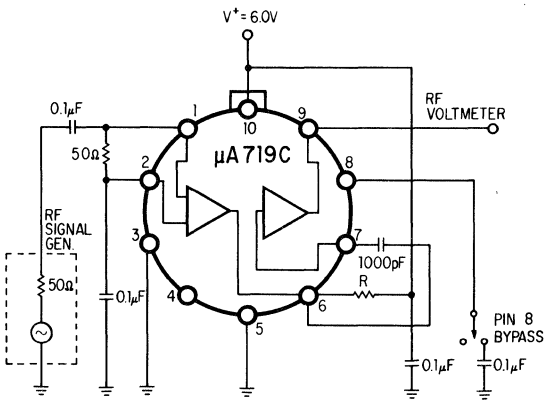
SECTION 2 FORWARD TRANSADMITTANCE



FORWARD TRANSADMITTANCE = $\frac{e_{OUT}}{e_{IN}} \cdot \frac{1}{50} \cdot 10^3$ mmho

TEST CIRCUIT 13

SECTION 1 AND 2 CASCADED VOLTAGE GAIN



DEFINITION OF TERMS

Gain Maximum Available (GMA) — This gain figure is the theoretical maximum power gain of an amplifier with conjugate matching at both the input and the output terminals and assumes no reverse transadmittance (feedback component) in the amplifier.

$$GMA = \frac{|\text{forward transadmittance}|^2}{4 \times \text{input conductance} \times \text{output conductance}}$$

Gain Maximum Stable (GMS) — This gain figure gives the maximum possible gain based on stability criteria only. This gain figure does not necessarily represent the realizable power gain of an amplifier. For unneutralized amplifiers, the maximum power gain realizable based on normal circuit tolerances is either (GMS - 6.0 dB) or GMA, whichever is smaller.

$$GMS = \frac{|\text{forward transadmittance}|}{|\text{reverse transadmittance}|}$$

Input Voltage For —3.0 dB Limiting — Refer to Test Circuit 4 which shows the μA719C being used as an amplifier, limiter, and FM detector (simple quadrature type with the LC tank circuit connected between pins No. 3 and No. 2). An input FM signal (carrier frequency 4.5 MHz, ±25 kHz deviation at 400 Hz) of 50 mV rms is applied to the μA719C and the value of the recovered audio output signal (400 Hz) at pin No. 6 is noted. The —3.0 dB input limiting voltage is defined as the value of the input voltage to produce an output voltage 3dB below the output level obtained with 50 mV rms of input signal.

μA722

10-BIT CURRENT SOURCE

FAIRCHILD LINEAR INTEGRATED CIRCUITS

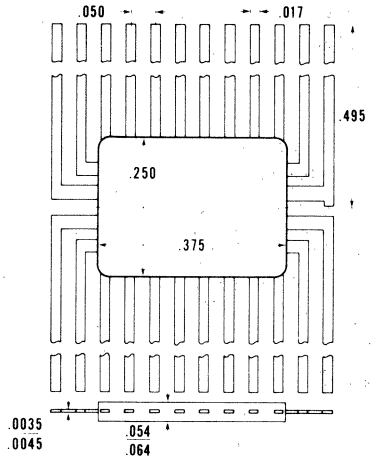
- **8 ± ½ BIT ACCURACY FROM 0°C TO +55°C**
- **7±½ BIT ACCURACY FROM −20°C TO +85°C**
- **600 ns SWITCHING SPEED**
- **INTERNAL PRECISION REFERENCE**
- **CCSL COMPATIBLE**

GENERAL DESCRIPTION — The μA722 is a high-speed, 10-bit precision current source intended for use in current-summing digital-to-analog converters or as the feedback element in successive approximation analog-to-digital converters. It is constructed on a single silicon chip, using the Fairchild Planar* epitaxial process, and consists of a reference supply, 10 current sources connected to a single output summing line, and associated logic switches. The full-scale current and coding format are set by an external resistor array, which may be preselected and fixed for general usage or trimmed for greater accuracy. The μA722 is compatible with the Fairchild families of linear and digital circuits.

ABSOLUTE MAXIMUM RATINGS

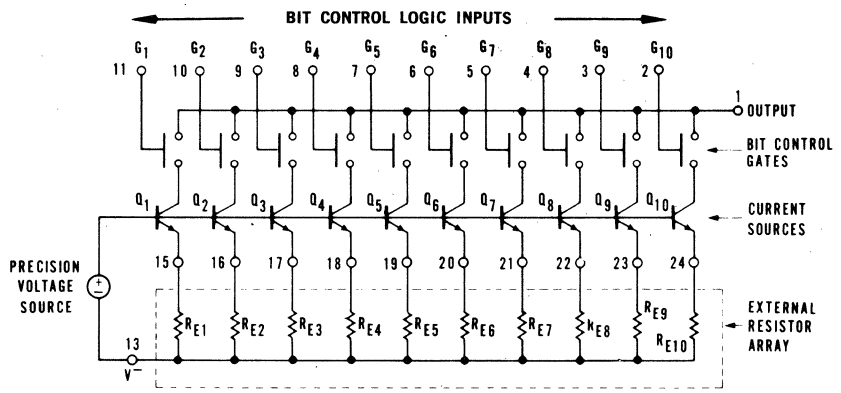
Voltage from V^+ to V^-	−0.5 V to +18 V
Voltage from Output to V^+	−12 V to +6 V
Voltage from Output to V^-	0 V to +12 V
Voltage from Logic Inputs to Output	−9 V to +7 V
Voltage from Logic Inputs to V^+	−18 V to 0 V
Voltage from Logic Inputs to V^-	0 V to +12 V
Internal Power Dissipation (Note 1)	450 mW
Operating Temperature Range	−20°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)

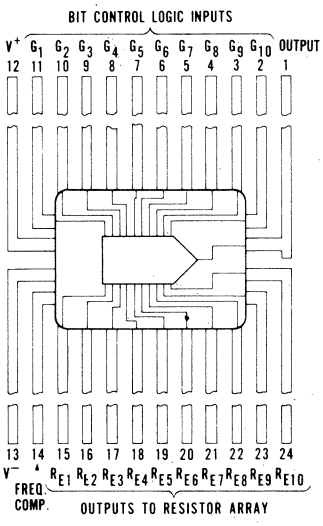


ORDER PART NO. U3M7722333

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



NOTE: PIN 13 INTERNALLY CONNECTED TO CASE.

Notes on Page 2

*Planar is a patented Fairchild process.

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ELECTRICAL CHARACTERISTICS

PARAMETER (See Definitions)	CONDITIONS (Note 2)	MIN.	TYP.	MAX.	UNITS
Resolution				10	Bits
Absolute Error	$T_A = 25°C$		±.07	±.20	%
	$0°C \leq T_A \leq +55°C$		±.10	±.20	%
	$-20°C \leq T_A \leq +85°C$		±.13	±.39	%
Output Current					
Full-Scale	Logic Inputs = 0.4 V	2160	2560	3000	μA
Zero-Scale	Logic Inputs = 2.5 V		±.002	±.25	μA
Power Supply Rejection	$\Delta V^+ = \Delta V^- = \pm 5\%$		±.06	±0.1	%/%
Output Resistance		0.2	1.2		MΩ
Switching Speed			600		ns
Logic Input High Voltage		2.1	2.5		V
Logic Input Low Voltage			0.4	0.7	V
Power Consumption			165	250	mW

NOTES:

(1) Rating applies for ambient temperatures to +85°C.
(2) Unless otherwise specified, $T_A = 25°C$, $V^+ = 6.0$ V ±.01 V, $V^- = -6.0$ V ±.01 V, $V_{out} = 0$ V, $C_I = 200$ pF, and external resistor array as per Table 1.
(3) In Table 1, the maximum absolute value tolerance for $R_{E1} = \pm 10\%$.

TYPICAL FULL-SCALE OUTPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

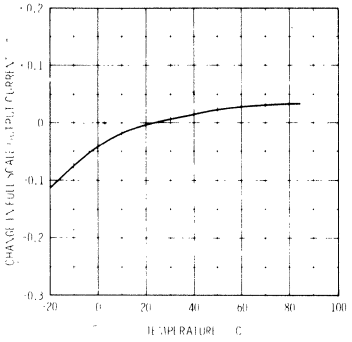
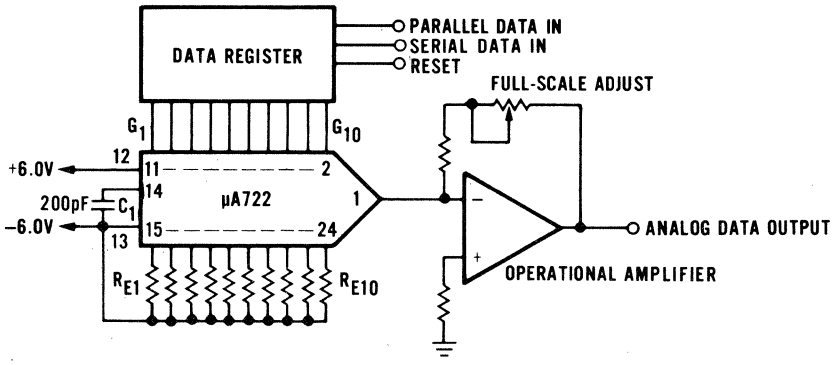


TABLE 1

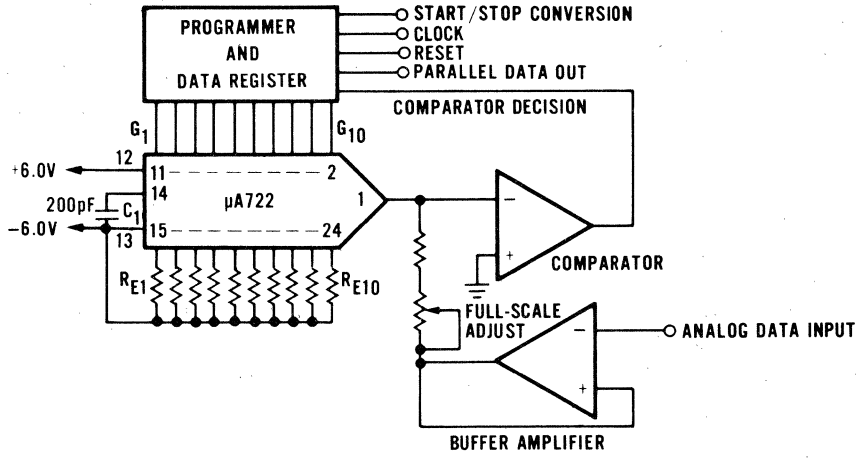
BINARY CODE RESISTOR ARRAY FOR 8 ± ½ BIT ACCURACY

Resistor Number (R_{EJ})	Nominal Value (kΩ)	Nominal Ratio (R_{EJ}/R_{E1})	Max. Ratio Tolerance ($T_A = 25°C$) (%)	Max. Ratio Temp. Coeff. (ppm/°C)
R_{E1}	2.547	1.000	Note 3	±5
R_{E2}	5.094	2.000	±0.02	±5
R_{E3}	10.245	4.022	±0.05	±10
R_{E4}	20.60	8.088	±0.10	±20
R_{E5}	41.43	16.265	±0.20	±20
R_{E6}	81.93	32.17	±0.20	±50
R_{E7}	163.4	64.16	±0.50	±100
R_{E8}	325.7	127.9	±1.0	±200
R_{E9}	644.9	253.2	±2.0	±500
R_{E10}	1275	500.8	±2.0	±500

TYPICAL DIGITAL-TO-ANALOG CONVERTER



TYPICAL ANALOG-TO-DIGITAL CONVERTER



DEFINITION OF TERMS

FULL SCALE OUTPUT CURRENT — The output current for all bits turned on.

ZERO SCALE OUTPUT CURRENT — The output current for all bits turned off.

ABSOLUTE ERROR — The worst-case deviation from a straight line drawn through zero and the 25°C value of the full-scale output current.

POWER SUPPLY REJECTION — The ratio of the percentage change in full-scale output current to the percentage change in supply voltage producing it.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at virtual ground and all bits turned on.

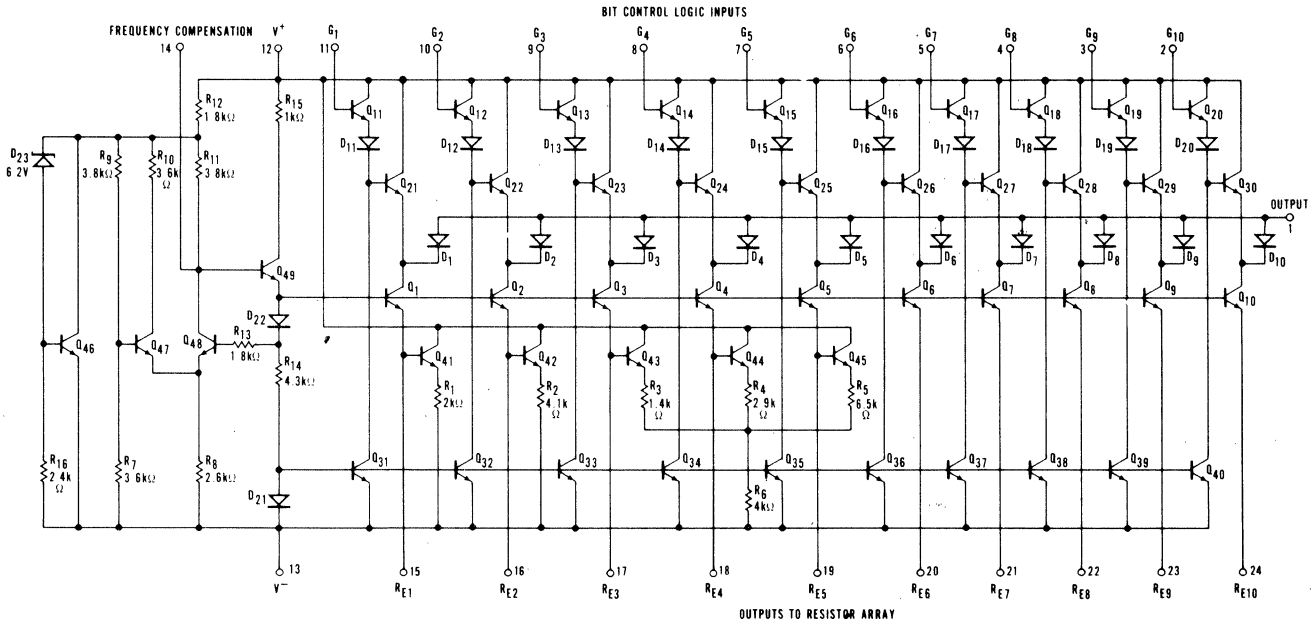
SWITCHING SPEED — The time required to turn on the least significant bit.

LOGIC INPUT HIGH VOLTAGE — The minimum voltage allowed at a bit control gate to hold the bit off.

LOGIC INPUT LOW VOLTAGE — The maximum voltage allowed at a bit control gate to hold the bit on.

POWER CONSUMPTION — The DC power required to operate the device; the power will vary with logic condition, but is specified as a maximum for the entire range of signal conditions.

SCHEMATIC DIAGRAM



μA722B

10-BIT CURRENT SOURCE

FAIRCHILD LINEAR INTEGRATED CIRCUITS

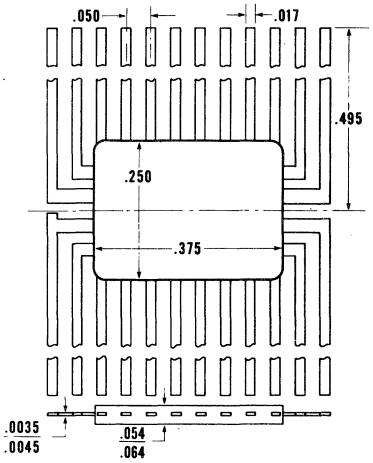
- **7 ±½ BIT ACCURACY FROM 0°C TO +55°C**
- **6 ± ½ BIT ACCURACY FROM −20°C TO +85°C**
- **600 ns SWITCHING SPEED**
- **INTERNAL PRECISION REFERENCE**
- **CCSL COMPATIBLE**

GENERAL DESCRIPTION — The μA722B is a high-speed, 10-bit precision current source intended for use in current-summing digital-to-analog converters or as the feedback element in successive approximation analog-to-digital converters. It is constructed on a single silicon chip, using the Fairchild Planar* epitaxial process, and consists of a reference supply, 10 current sources connected to a single output summing line, and associated logic switches. The full-scale current and coding format are set by an external resistor array, which may be preselected and fixed for general usage or trimmed for greater accuracy. The μA722B is compatible with the Fairchild families of linear and digital circuits. For higher accuracy, see μA722 data sheet.

ABSOLUTE MAXIMUM RATINGS

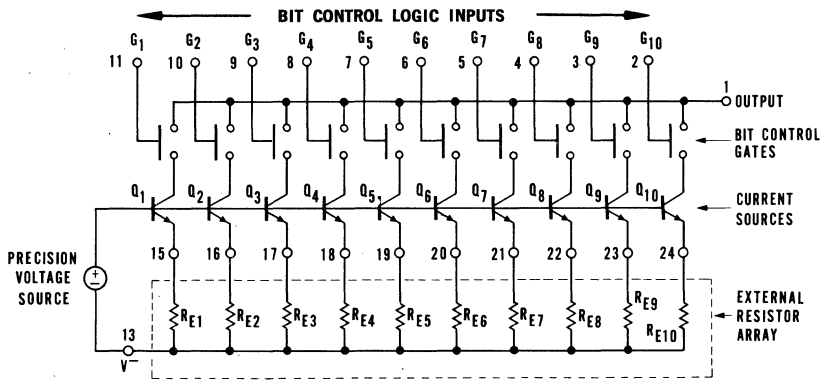
Voltage from V^+ to V^-	−0.5 V to +18 V
Voltage from Output to V^+	−12 V to +6 V
Voltage from Output to V^-	0 V to +12 V
Voltage from Logic Inputs to Output	−9 V to +7 V
Voltage from Logic Inputs to V^+	−18 V to 0 V
Voltage from Logic Inputs to V^-	0 V to +12 V
Internal Power Dissipation (Note 1)	450 mW
Operating Temperature Range	−20°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

PHYSICAL DIMENSIONS
(TYPICAL FLAT PACKAGE)
(TOP VIEW)

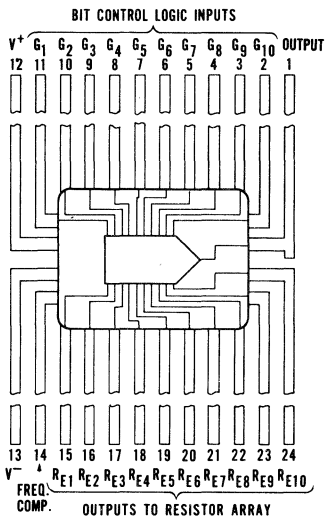


ORDER PART NO. U3M7722334

EQUIVALENT CIRCUIT



CONNECTION DIAGRAM
(TOP VIEW)



NOTE: PIN 13 INTERNALLY CONNECTED TO CASE.

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*Planar is a patented Fairchild process.

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ELECTRICAL CHARACTERISTICS

PARAMETER (See Definitions)	CONDITIONS (Note 2)	MIN.	TYP.	MAX.	UNITS
Resolution				10	Bits
Absolute Error	$T_A = 25°C$		±.08	±.39	%
	$0°C \leq T_A \leq +55°C$		±.17	±.39	%
	$-20°C \leq T_A \leq +85°C$		±.22	±.78	%
Output Current					
Full-Scale	Logic Inputs = 0.4 V	2160	2560	3000	μA
Zero-Scale	Logic Inputs = 2.5 V		±.002	±.25	μA
Power Supply Rejection	$\Delta V^+ = \Delta V^- = \pm 5\%$		±.06	±0.1	%/%
Output Resistance		0.2	1.2		MΩ
Switching Speed			600		ns
Logic Input High Voltage		2.1	2.5		V
Logic Input Low Voltage			0.4	0.7	V
Power Consumption			165	250	mW

NOTES:

(1) Rating applies for ambient temperatures to +85°C.
(2) Unless otherwise specified, $T_A = 25°C$, $V^+ = 6.00\ V \pm .01\ V$, $V^- = -6.00\ V \pm .01\ V$, $V_{out} = 0\ V$, $C_l = 200\ pF$, and external resistor array as per Table 1.
(3) In Table 1, the maximum absolute value tolerance for $R_{E1} = \pm 10\%$.

TYPICAL FULL-SCALE OUTPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

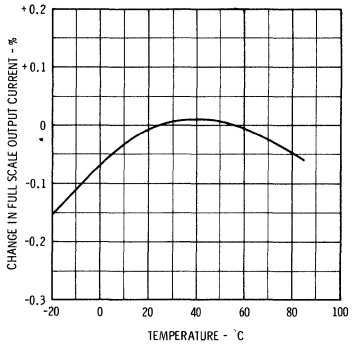
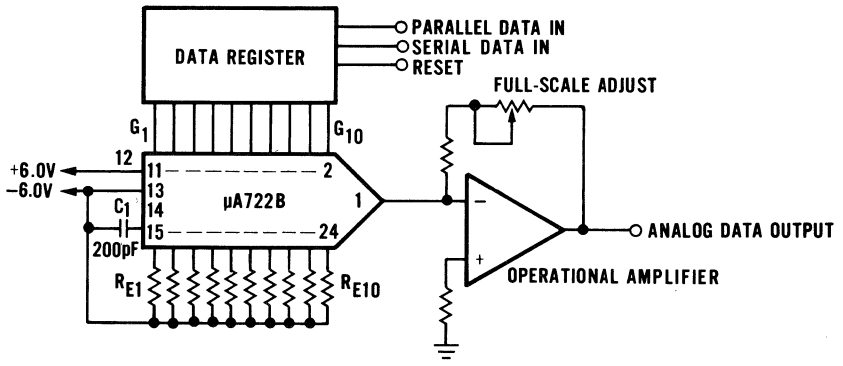


TABLE 1

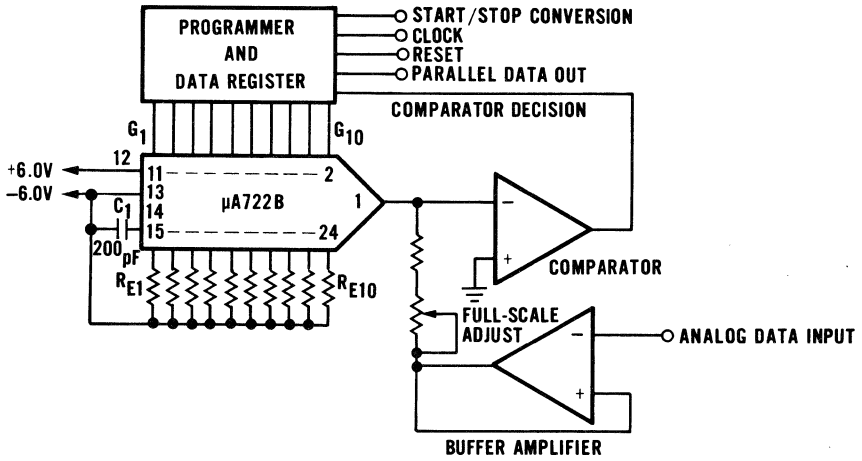
BINARY CODE RESISTOR ARRAY FOR 6 ± ½ BIT ACCURACY

Resistor Number (R_{EJ})	Nominal Value (kΩ)	Nominal Ratio (R_{EJ}/R_{E1})	Max. Ratio Tolerance ($T_A = 25°C$) (%)	Max. Ratio Temp. Coeff. (ppm/°C)
R_{E1}	2.547	1.000	Note 3	±20
R_{E2}	5.094	2.000	±0.10	±20
R_{E3}	10.245	4.022	±0.20	±50
R_{E4}	20.60	8.088	±0.20	±50
R_{E5}	41.43	16.265	±0.50	±100
R_{E6}	81.93	32.17	±0.50	±100
R_{E7}	163.4	64.16	±1.0	±500
R_{E8}	325.7	127.9	±1.0	±500
R_{E9}	644.9	253.2	±5.0	±1000
R_{E10}	1275	500.8	±5.0	±1000

TYPICAL DIGITAL-TO-ANALOG CONVERTER



TYPICAL ANALOG-TO-DIGITAL CONVERTER



DEFINITION OF TERMS

FULL SCALE OUTPUT CURRENT — The output current for all bits turned on.

ZERO SCALE OUTPUT CURRENT — The output current for all bits turned off.

ABSOLUTE ERROR — The worst-case deviation from a straight line drawn through zero and the 25°C value of the full-scale output current.

POWER SUPPLY REJECTION — The ratio of the percentage change in full-scale output current to the percentage change in supply voltage producing it.

OUTPUT RESISTANCE — The resistance seen looking into the output terminal with the output at virtual ground and all bits turned on.

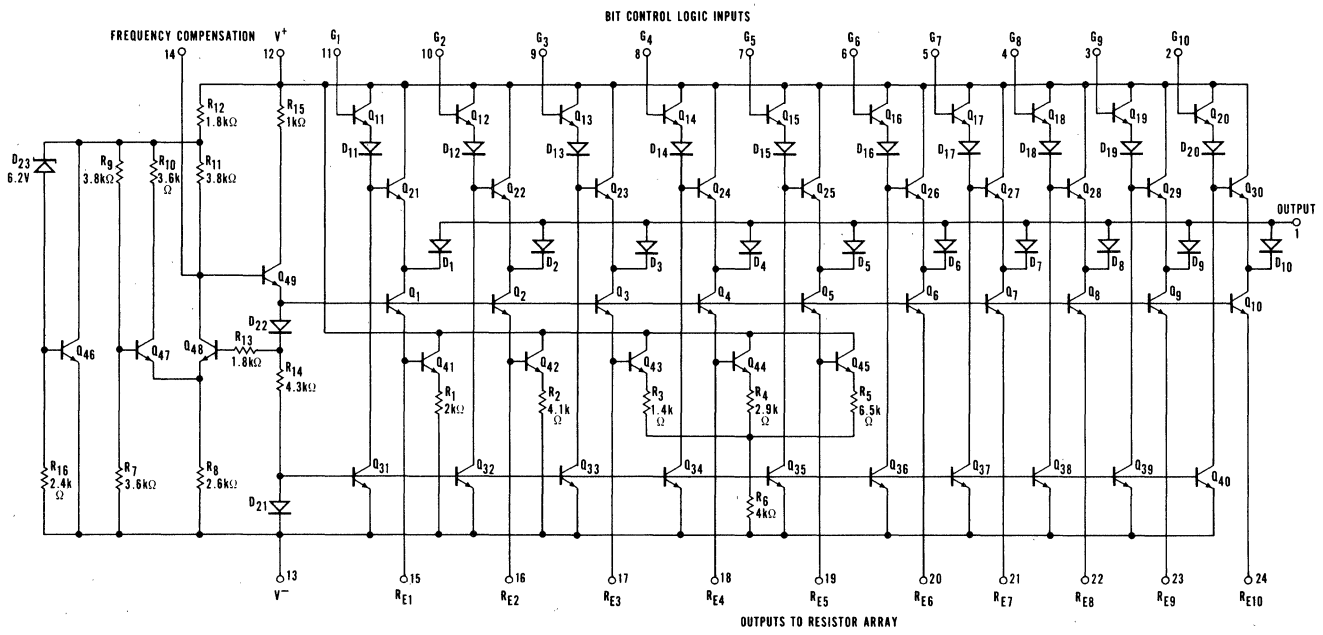
SWITCHING SPEED — The time required to turn on the least significant bit.

LOGIC INPUT HIGH VOLTAGE — The minimum voltage allowed at a bit control gate to hold the bit off.

LOGIC INPUT LOW VOLTAGE — The maximum voltage allowed at a bit control gate to hold the bit on.

POWER CONSUMPTION — The DC power required to operate the device; the power will vary with logic condition, but is specified as a maximum for the entire range of signal conditions.

SCHEMATIC DIAGRAM



μA723C

PRECISION VOLTAGE REGULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

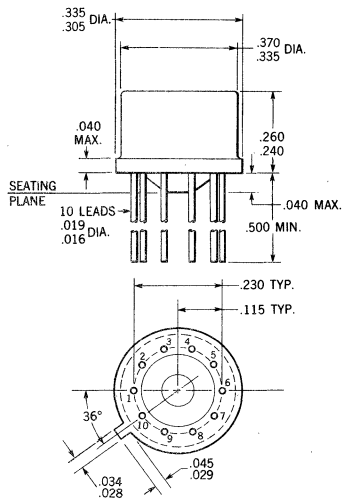
- **POSITIVE OR NEGATIVE SUPPLY OPERATION**
- **SERIES, SHUNT, SWITCHING OR FLOATING OPERATION**
- **.01% LINE AND LOAD REGULATION**
- **OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37 VOLTS**
- **OUTPUT CURRENT TO 150 mA WITHOUT EXTERNAL PASS TRANSISTOR**

GENERAL DESCRIPTION — The μA723C is a monolithic voltage regulator constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The μA723C is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems and in other power supplies for digital and linear circuits. For full temperature range operation (−55°C to +125°C), see μA723 data sheet.

ABSOLUTE MAXIMUM RATINGS

Voltage from V^+ to V^-	40 V
Input-Output Voltage Differential	40 V
Maximum Output Current	150 mA
Current from V_Z	25 mA
Internal Power Dissipation (Note 1)	800 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range (Metal Can)	−65°C to +150°C
Storage Temperature Range (DIP)	−55°C to +125°C
Lead Temperature (Soldering, 60 sec.)	300°C

PHYSICAL DIMENSIONS



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

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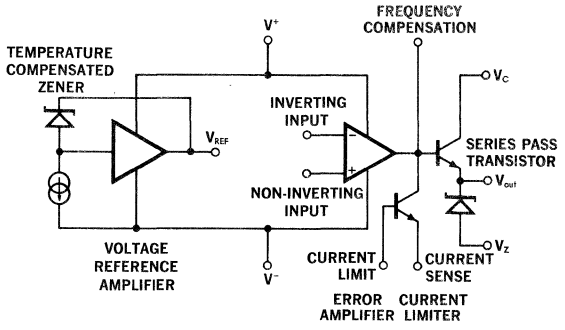
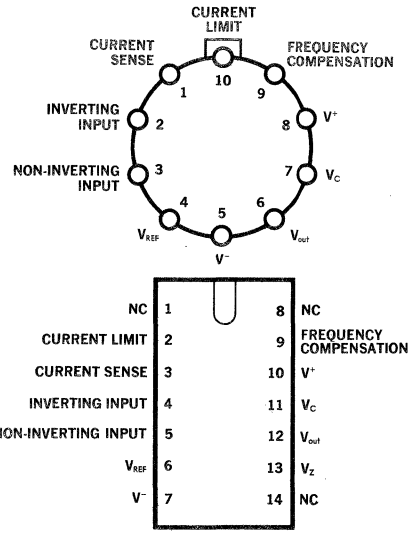
EQUIVALENT CIRCUIT



CONNECTION DIAGRAMS

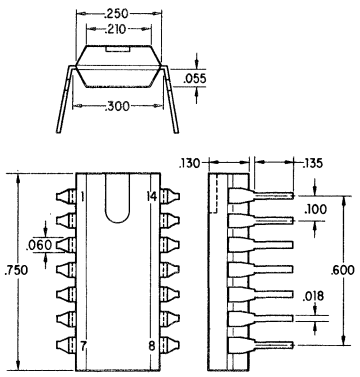
TOP VIEWS



NC	1	8	NC
CURRENT LIMIT	2	9	FREQUENCY COMPENSATION
CURRENT SENSE	3	10	V^+
INVERTING INPUT	4	11	V_C
NON-INVERTING INPUT	5	12	V_{out}
V_{REF}	6	13	V_Z
V^-	7	14	NC

Note: On metal can, pin 5 is connected to case

TYPICAL DUAL IN-LINE PACKAGE



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows, .300 centers

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Notes on Page 2.

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
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ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Line Regulation	$V = 12\ V$ to $V = 15\ V$		.01	0.1	% V_{OUT}
	$V_{IN} = 12\ V$ to $V_{IN} = 40\ V$		0.1	0.5	% V_{OUT}
	$0°C \leq T_A \leq 70°C$, $V_{IN} = 12\ V$ to $V_{IN} = 15\ V$			0.3	% V_{OUT}
Load Regulation	$I_L = 1\ mA$ to $I_L = 50\ mA$		.03	0.2	% V_{OUT}
	$0°C \leq T_A \leq 70°C$, $I_L = 1\ mA$ to $I_L = 50\ mA$			0.6	% V_{OUT}
Ripple Rejection	$f = 50\ Hz$ to $10\ kHz$, $C_{REF} = 0$		74		dB
	$f = 50\ Hz$ to $10\ kHz$, $C_{REF} = 5\ \mu F$		86		dB
Average Temperature Coefficient of Output Voltage	$0°C \leq T_A \leq 70°C$		.003	.015	%/°C
Short Circuit Current Limit	$R_{SC} = 10\ \Omega$, $V_{OUT} = 0$		65		mA
Reference Voltage		6.80	7.15	7.50	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, $C_{REF} = 0$		20		μV_{rms}
	BW = 100 Hz to 10 kHz, $C_{REF} = 5\ \mu F$		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	$I_L = 0$, $V_{IN} = 30\ V$		2.3	4.0	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input-Output Voltage Differential		3.0		38	V

DEFINITION OF TERMS

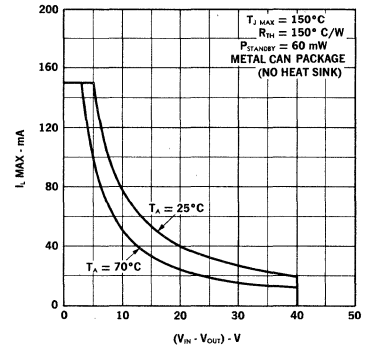
LINE REGULATION — The percentage change in output voltage for a specified change in input voltage.
LOAD REGULATION — The percentage change in output voltage for a specified change in load current.
RIPPLE REJECTION — The ratio of the peak to peak input ripple voltage to the peak to peak output ripple voltage.
AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE — The percentage change in output voltage for a specified change in ambient temperature.
SHORT CIRCUIT CURRENT LIMIT — The output current of the regulator with the output shorted to the negative supply.
REFERENCE VOLTAGE — The output of the reference amplifier measured with respect to the negative supply.
OUTPUT NOISE VOLTAGE — The rms output noise voltage with constant load and no input ripple.
STANDBY CURRENT DRAIN — The supply current drawn by the regulator with no output load and no reference voltage load.
INPUT VOLTAGE RANGE — The range of supply voltage over which the regulator will operate.
OUTPUT VOLTAGE RANGE — The range of output voltage over which the regulator will operate.
INPUT-OUTPUT VOLTAGE DIFFERENTIAL — The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operate.
SENSE VOLTAGE — The voltage between current sense and current limit terminals necessary to cause current limiting.
TRANSIENT RESPONSE — The closed-loop step function response of the regulator under small-signal conditions.

NOTES:

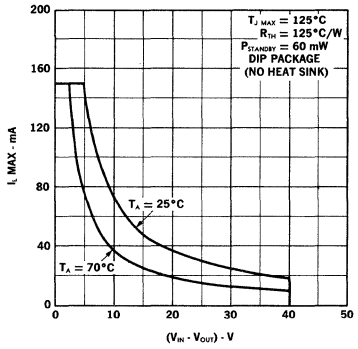
(1) Derate metal can package at 6.8 mW/°C and dual in-line package at 8 mW/°C for operation at ambient temperatures above 25°C.
(2) Unless otherwise specified, $T_A = 25°C$, $V_{IN} = V^+ = V_C = 12\ V$, $V^- = 0$, $V_{out} = 5\ V$, $I_L = 1\ mA$, $R_{SC} = 0$, $C_1 = 100\ pF$ and divider impedance as seen by the error amplifier $\leq 10\ K\Omega$.
(3) For metal can applications where V_Z is required, an external 6.2 zener should be connected in series with V_{out}.
(4) Figures in parentheses may be used if R_1/R_2 divider is placed on opposite of error amp.
(5) Replace R_1/R_2 in figures with divider shown in figure 13.
(6) V^+ and V_C must be connected to a +3 V or greater supply.
(7) L_1 is 40 turns of #20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009" air gap.

TYPICAL PERFORMANCE CURVES

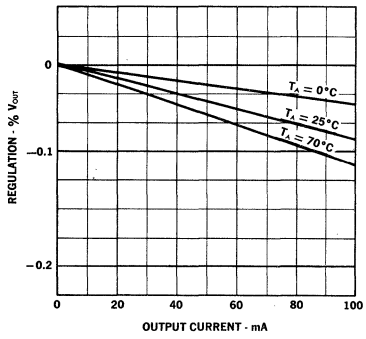
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



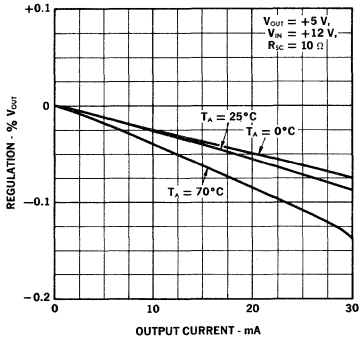
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



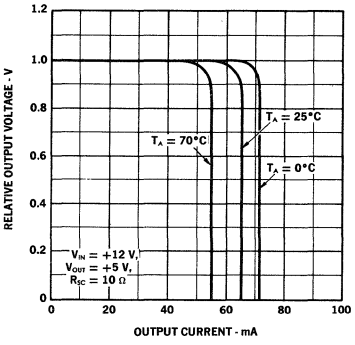
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



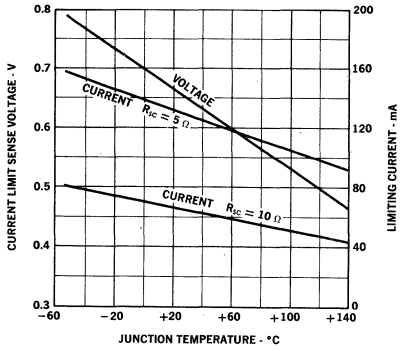
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



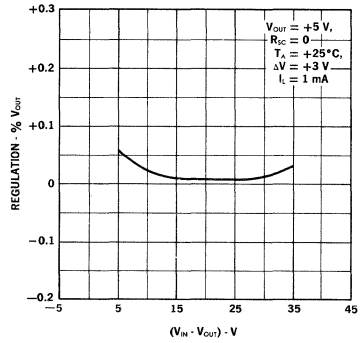
CURRENT LIMITING CHARACTERISTICS



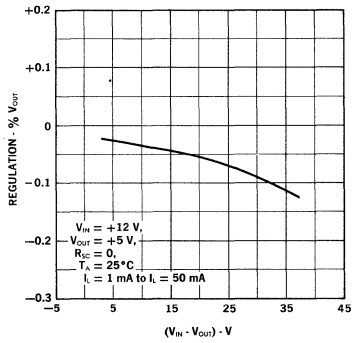
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



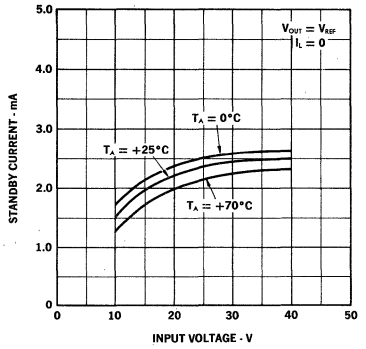
LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



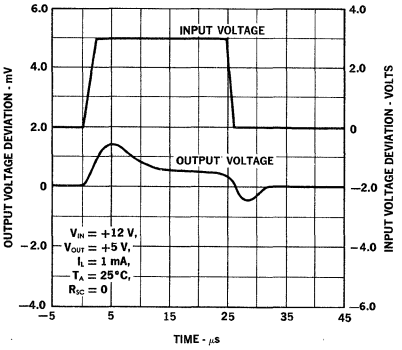
LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



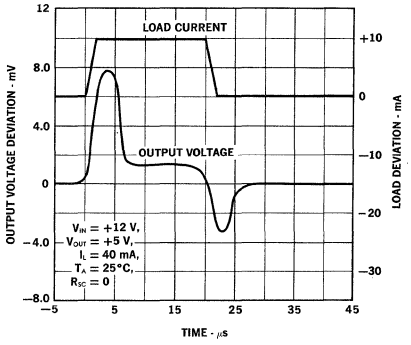
STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE



LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

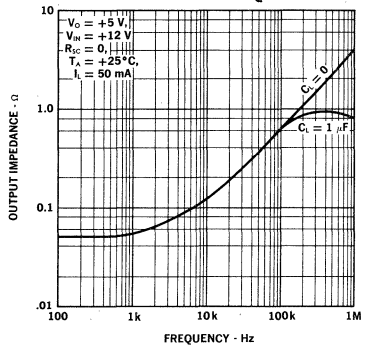


TABLE I
RESISTOR VALUES (KΩ) FOR STANDARD OUTPUT VOLTAGES

POSITIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (Note 5)			NEGATIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		5% OUTPUT ADJUSTABLE ±10%		
	(Note 4)	R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	.75	0.5	2.2	−6 (note 6)	3, (10)	3.57	2.43	1.2	0.5	.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 12, 9)	1.87	7.15	.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

TABLE II
FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts
[Figures 1, 5, 6, 9, 12, (4)]

$$V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$$

Outputs from +4 to +250 volts
[Figure 7]

$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_2 - R_1}{R_1}]\ ;\ R_3 = R_4$$

Current Limiting

$$I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}}$$

Outputs from +7 to +37 volts
[Figures 2, 4, (5, 6, 9, 12)]

$$V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$$

Outputs from −6 to −250 volts
[Figures 3, 8, 10]

$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}]\ ;\ R_3 = R_4$$

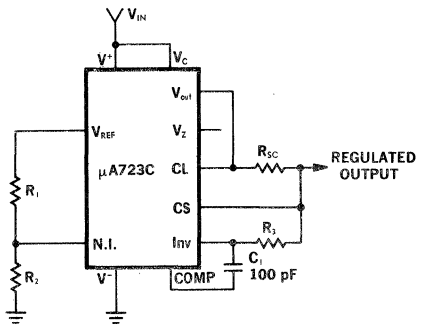
Foldback Current Limiting

$$I_{KNEE} = [\frac{V_{OUT}\, R_3}{R_{SC}\, R_4} + \frac{V_{SENSE}\,(R_3 + R_4)}{R_{SC}\, R_4}]$$

$$I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{SC}} \times \frac{R_3 + R_4}{R_4}]$$

Figure 1

BASIC LOW VOLTAGE REGULATOR
(V_{out} = 2 to 7 Volts)



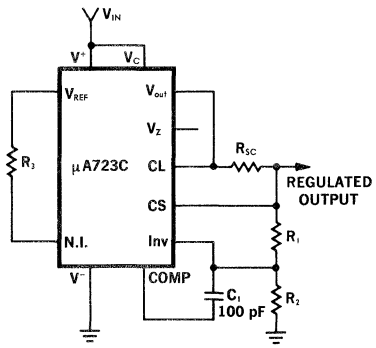
TYPICAL PERFORMANCE

Regulated Output Voltage	5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Note: $R_3 = \frac{R_1\, R_2}{R_1 + R_2}$ for minimum temperature drift.
R_3 may be eliminated for minimum component count.

Figure 2

BASIC HIGH VOLTAGE REGULATOR
(V_{out} = 7 to 37 Volts)



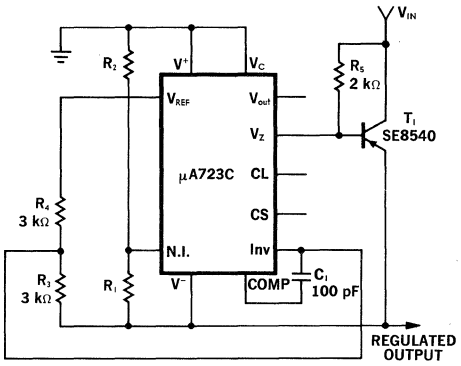
TYPICAL PERFORMANCE

Regulated Output Voltage	15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5 mV
Load Regulation (ΔI_L=50 mA)	4.5 mV

Note: $R_3 = \frac{R_1\, R_2}{R_1 + R_2}$ for minimum temperature drift.
R_3 may be eliminated for minimum component count.

Figure 3

NEGATIVE VOLTAGE REGULATOR



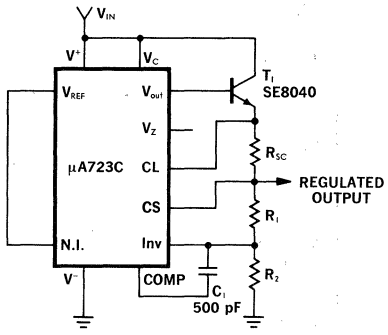
TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1 mV
Load Regulation ($\Delta I_L = 100$ mA)	2 mV

Note 3

Figure 4

POSITIVE VOLTAGE REGULATOR (External NPN Pass Transistor)

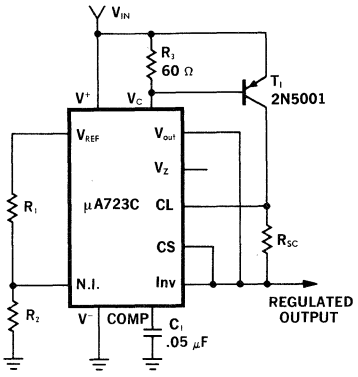


TYPICAL PERFORMANCE

Regulated Output Voltage	+15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1.5 mV
Load Regulation ($\Delta I_L = 1$ amp)	15 mV

Figure 5

POSITIVE VOLTAGE REGULATOR (External PNP Pass Transistor)

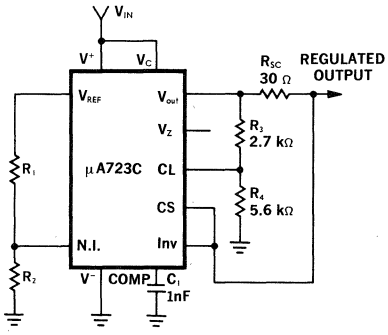


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 1$ amp)	5 mV

Figure 6

FOLDBACK CURRENT LIMITING

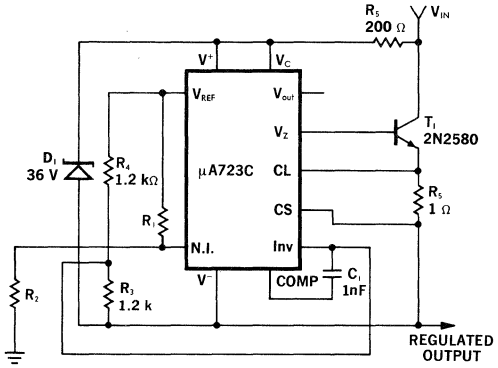


TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 10$ mA)	1 mV
Current Limit Knee	20 mA

Figure 7

POSITIVE FLOATING REGULATOR



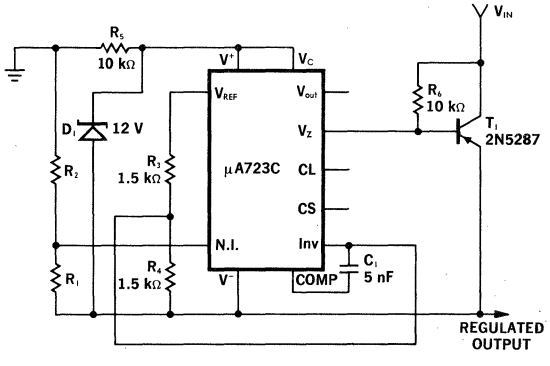
TYPICAL PERFORMANCE

Regulated Output Voltage	+100 V
Line Regulation ($\Delta V_{IN} = 20$ V)	15 mV
Load Regulation ($\Delta I_L = 50$ mA)	20 mV

Note 3

Figure 8

NEGATIVE FLOATING REGULATOR



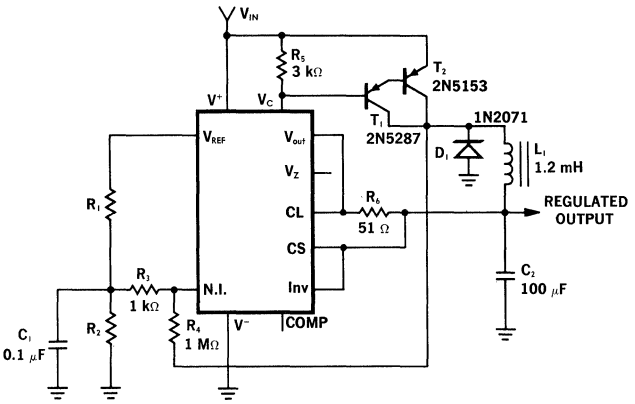
TYPICAL PERFORMANCE

Regulated Output Voltage	−100 V
Line Regulation ($\Delta V_{IN} = 20$ V)	30 mV
Load Regulation (ΔI_L=100 mA)	20 mV

Note 3

Figure 9

POSITIVE SWITCHING REGULATOR



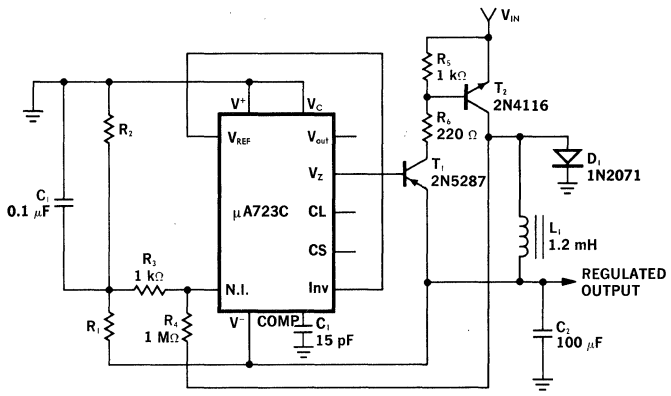
TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 30$ V)	10 mV
Load Regulation (ΔI_L=2 amps)	80 mV

Note 7

Figure 10

NEGATIVE SWITCHING REGULATOR



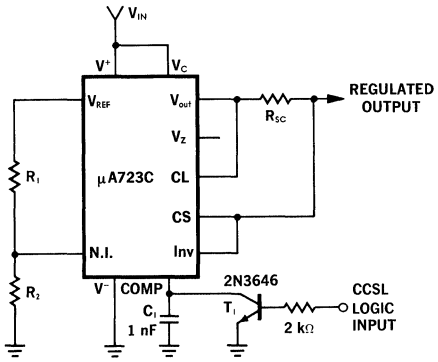
TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 20$ V)	8 mV
Load Regulation ($\Delta I_L = 2$ amps)	6 mV

Note 3
Note 7

Figure 11

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING



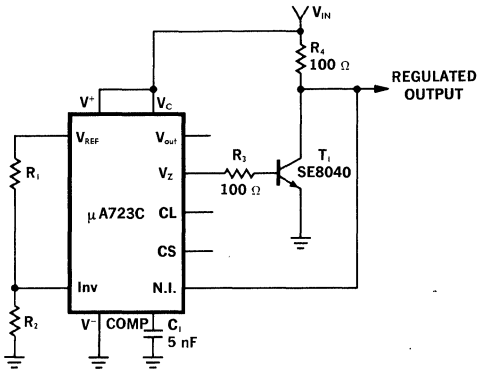
TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Note: Current limit transistor may be used for shutdown if current limiting is not required.

Figure 12

SHUNT REGULATOR



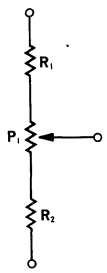
TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 10$ V)	2 mV
Load Regulation (ΔI_L=100 mA)	5 mV

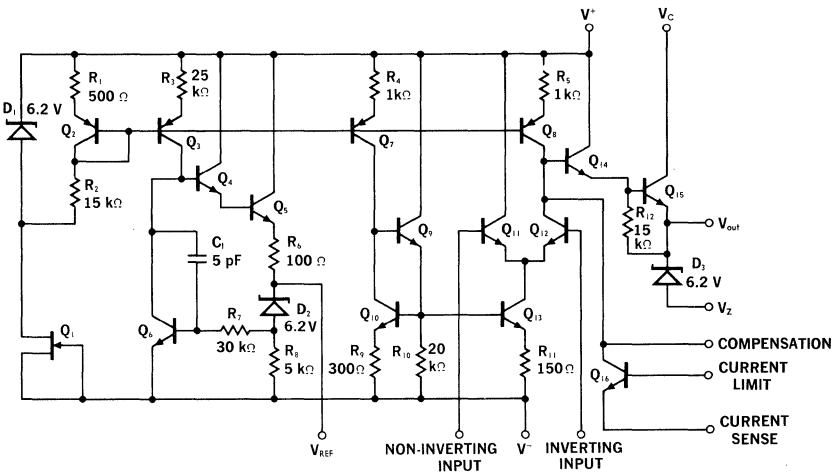
Note 3

Figure 13

OUTPUT VOLTAGE ADJUST



SCHEMATIC DIAGRAM



μA726

TEMPERATURE-CONTROLLED DIFFERENTIAL PAIR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA726 is a monolithic transistor pair in a high thermal-resistance package, held at a constant temperature by active temperature regulator circuitry. The transistor pair displays the excellent matching, close thermal coupling, and fast thermal response inherent in monolithic construction. The high gain and low standby dissipation of the regulator circuit permits tight temperature control over a wide range of ambient temperatures. It is intended for use as an input stage in very-low-drift dc amplifiers, replacing complex chopper-stabilized amplifiers; it is also useful as the nonlinear element in logarithmic amplifiers and multipliers where the highly predictable exponential relation between emitter-base voltage and collector current is employed. The device is constructed on a single silicon chip using the Fairchild Planar* process.

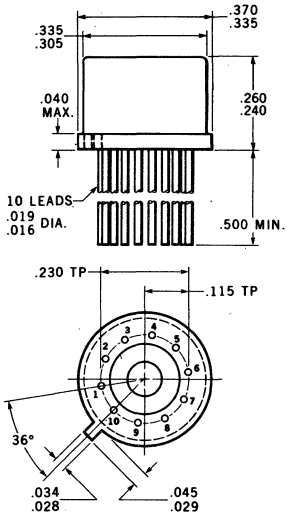
ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 seconds)	300°C
Supply Voltage	±18 V

MAXIMUM RATINGS FOR EACH TRANSISTOR

Maximum collector-to-substrate voltage	40 V
BV_{CBO}	40 V
LV_{CEO} [Note 1]	30 V
BV_{EBO}	5 V
Collector Current	5 mA

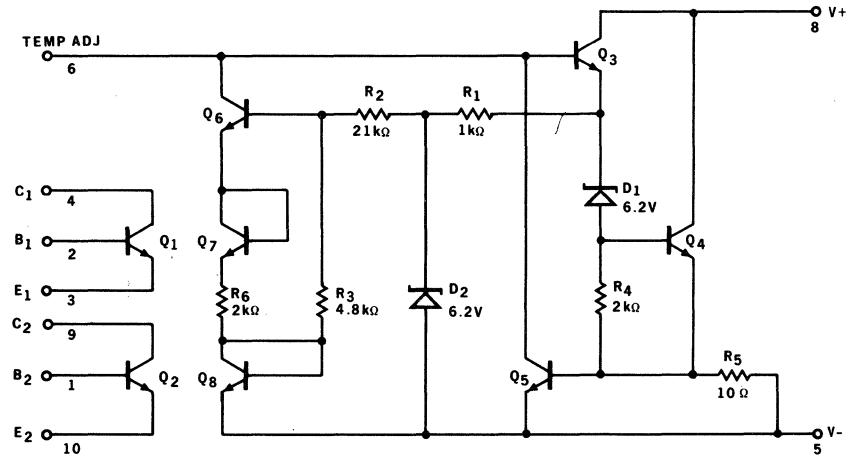
PHYSICAL DIMENSIONS



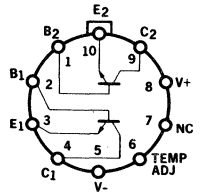
NOTES: All dimensions in inches
Leads are gold-plated kovar
Package weight is 1.32 grams

ORDER PART NO. U5J772631X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



TOP VIEW

Note 1: Measured at 1 mA collector current.

* Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

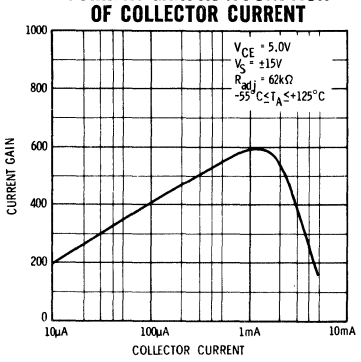
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq +125°C$, $V_S = \pm 15$ V, $R_{adj} = 62$ kΩ unless otherwise specified)

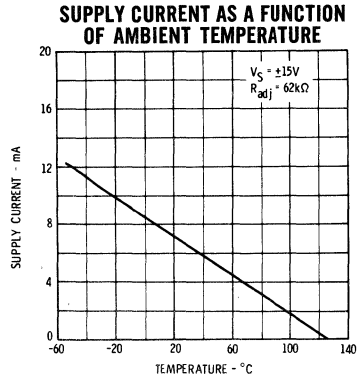
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$10\ \mu A \leq I_C \leq 100\ \mu A$ $V_{CE} = 5$ V, $R_S \leq 50\Omega$		1.0	2.5	mV
Input Offset Current	$I_C = 10\ \mu A$, $V_{CE} = 5$ V		10	50	nA
Input Offset Current	$I_C = 100\ \mu A$, $V_{CE} = 5$ V		50	200	nA
Average Input Bias Current	$I_C = 10\ \mu A$, $V_{CE} = 5$ V		50	150	nA
Average Input Bias Current	$I_C = 100\ \mu A$, $V_{CE} = 5$ V		250	500	nA
Offset Voltage Change	$I_C = 10\ \mu A$, $5\text{ V} \leq V_{CE} \leq 25$ V, $R_S \leq 100$ kΩ		0.3	6.0	mV
Offset Voltage Change	$I_C = 100\ \mu A$, $5\text{ V} \leq V_{CE} \leq 25$ V, $R_S \leq 10$ kΩ		0.3	6.0	mV
Input Offset Voltage Drift	$10\ \mu A \leq I_C \leq 100\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, $+25°C \leq T_A \leq +125°C$		0.2	1.0	μV/°C
Input Offset Voltage Drift	$10\mu A \leq I_C \leq 100\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, $-55°C \leq T_A \leq +25°C$		0.2	1.0	μV/°C
Input Offset Current Drift	$I_C = 10\ \mu A$, $V_{CE} = 5$ V		10		pA/°C
Input Offset Current Drift	$I_C = 100\ \mu A$, $V_{CE} = 5$ V		30		pA/°C
Supply Voltage Rejection Ratio	$10\mu A \leq I_C \leq 100\ \mu A$, $R_S \leq 50\Omega$,		25		μV/V
Low-Frequency Noise	$I_C = 10\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$ BW = .001 Hz to 0.1 Hz		4.0		μV pp
Broadband Noise	$I_C = 10\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$ BW = 0.1 Hz to 10 kHz		10		μV pp
Long-term Drift	$10\ \mu A \leq I_C \leq 100\ \mu A$, $V_{CE} = 5$ V, $R_S \leq 50\Omega$, $T_A = 25°C$		5.0		μV/week
High Frequency Current Gain	f = 20 MHz, $I_C = 100\ \mu A$, $V_{CE} = 5$ V	1.5	3.5		
Output Capacitance	$I_E = 0$, $V_{CB} = 5$ V		1.0		pF
Emitter Transition Capacitance	$I_E = 100\ \mu A$		1.0		pF
Collector Saturation Voltage	$I_B = 100\ \mu A$, $I_C = 1$ mA		0.5	1.0	V

TYPICAL PERFORMANCE CURVES

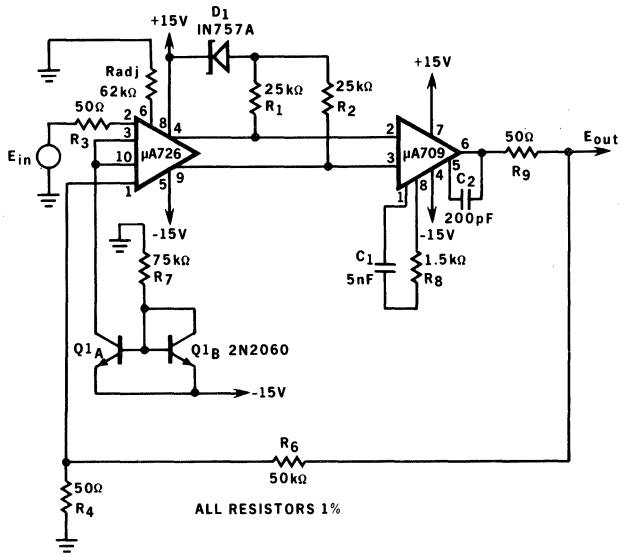
CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL X1000 CIRCUIT



μA726C

TEMPERATURE-CONTROLLED DIFFERENTIAL PAIR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION—The μA726C is a monolithic transistor pair in a high thermal-resistance package, held at a constant temperature by active temperature regulator circuitry. The transistor pair displays the excellent matching, close thermal coupling, and fast thermal response inherent in monolithic construction. The high gain and low standby dissipation of the regulator circuit permits tight temperature control over a wide range of ambient temperatures. It is intended for use as an input stage in very-low-drift dc amplifiers, replacing complex chopper-stabilized amplifiers; it is also useful as the nonlinear element in logarithmic amplifiers and multipliers where the highly predictable exponential relation between emitter-base voltage and collector current is employed. The device is constructed on a single silicon chip using the Fairchild Planar* process. For full temperature range (−55°C to +125°C) see μA726 data sheet.

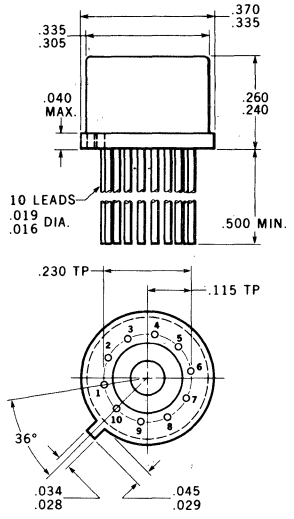
ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	0°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	300°C
Supply Voltage	±18V

MAXIMUM RATINGS FOR EACH TRANSISTOR

Maximum collector-to-substrate voltage	40V
BV_{CBO}	40V
LV_{CEO} (Note 1)	30V
BV_{EBO}	5V
Collector Current	5 mA

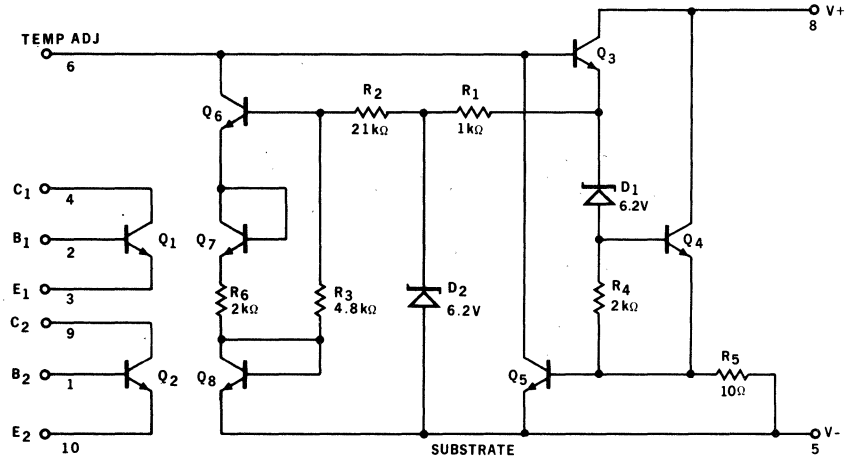
PHYSICAL DIMENSIONS



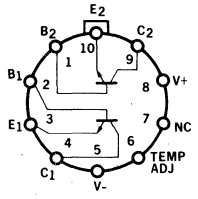
NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

ORDER PART NO. U5J772632X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM



TOP VIEW

NOTE: (1) Measured at 1 mA collector current.

*Planar is a patented Fairchild process.

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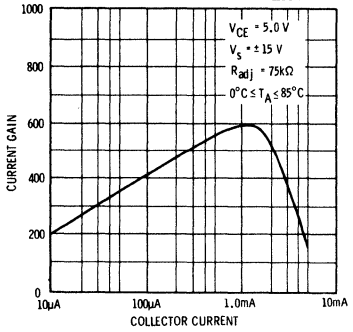
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq +85°C$, $V_S = \pm 15V$, $R_{adj} = 75\,k\Omega$ unless otherwise specified)

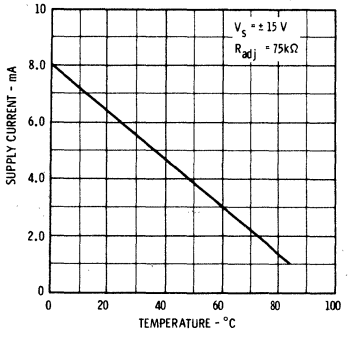
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$10\,\mu A \leq I_C \leq 100\,\mu A$ $V_{CE} = 5V$, $R_S \leq 50\Omega$		1.0	3.0	mV
Input Offset Current	$I_C = 10\,\mu A$, $V_{CE} = 5V$		10	100	nA
Input Offset Current	$I_C = 100\,\mu A$, $V_{CE} = 5V$		50	400	nA
Average Input Bias Current	$I_C = 10\,\mu A$, $V_{CE} = 5V$		50	300	nA
Average Input Bias Current	$I_C = 100\,\mu A$, $V_{CE} = 5V$		250	1000	nA
Offset Voltage Change	$I_C = 10\,\mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 100\,k\Omega$		0.3	6.0	mV
Offset Voltage Change	$I_C = 100\,\mu A$, $5V \leq V_{CE} \leq 25V$, $R_S \leq 10\,k\Omega$		0.3	6.0	mV
Input Offset Voltage Drift	$I_C = 100\,\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$		0.2	2.0	μV/°C
Input Offset Current Drift	$I_C = 10\,\mu A$, $V_{CE} = 5V$		10		pA/°C
Input Offset Current Drift	$I_C = 100\,\mu A$, $V_{CE} = 5V$		30		pA/°C
Supply Voltage Rejection Ratio	$I_C = 100\,\mu A$, $R_S = 50\Omega$		25		μV/V
Low-Frequency Noise	$I_C = 10\,\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, BW = 0.001 Hz to 0.1 Hz		4.0		μV pp
Broadband Noise	$I_C = 10\,\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, BW = 0.1 Hz to 10 kHz		10		μV pp
Long-Term Drift	$I_C = 100\,\mu A$, $V_{CE} = 5V$, $R_S \leq 50\Omega$, $T_A = 25°C$		5.0		μV/week
High-Frequency Current Gain	f = 20 MHz, $I_C = 100\,\mu A$, $V_{CE} = 5V$	1.5	3.5		
Output Capacitance	$I_E = 0$, $V_{CB} = 5V$		1.0		pF
Emitter Transition Capacitance	$I_E = 100\,\mu A$		1.0		pF
Collector Saturation Voltage	$I_B = 100\,\mu A$, $I_C = 1$ mA		0.5	1.0	V

TYPICAL PERFORMANCE CURVES

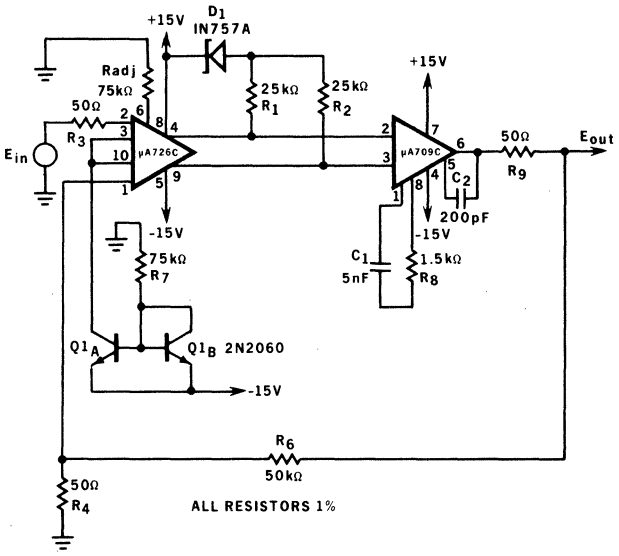
CURRENT GAIN AS A FUNCTION OF COLLECTOR CURRENT



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



TYPICAL X1000 CIRCUIT



μA727

TEMPERATURE-CONTROLLED DIFFERENTIAL PREAMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES

- **VERY LOW OFFSET DRIFTS**
- **HIGH INPUT IMPEDANCE**
- **WIDE COMMON MODE RANGE**

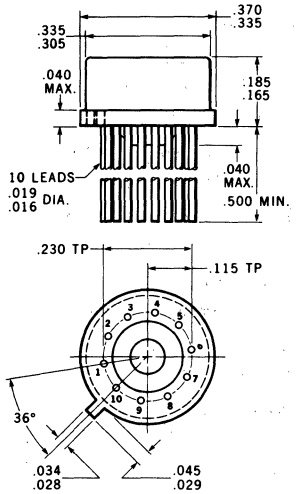
GENERAL DESCRIPTION — The μA727 is a monolithic, fixed gain, differential-input differential-output amplifier, constructed with the Fairchild Planar* epitaxial process, mounted in a high thermal-resistance package, and held at constant temperature by active regulator circuitry. The high gain and low standby dissipation of the regulator circuit give tight temperature control over a wide ambient temperature range. The device is intended for use as a self-contained input stage in very low-drift DC amplifiers, replacing complex chopper-stabilized amplifiers in such applications as thermo-couple bridges, strain gage transducers, and A to D converters.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 second time limit)	300°C
Supply Voltage (Amplifier and Heater)	±18 V
Differential Input Voltage	±10 V
Common Mode Input Voltage	±15 V

PHYSICAL DIMENSIONS

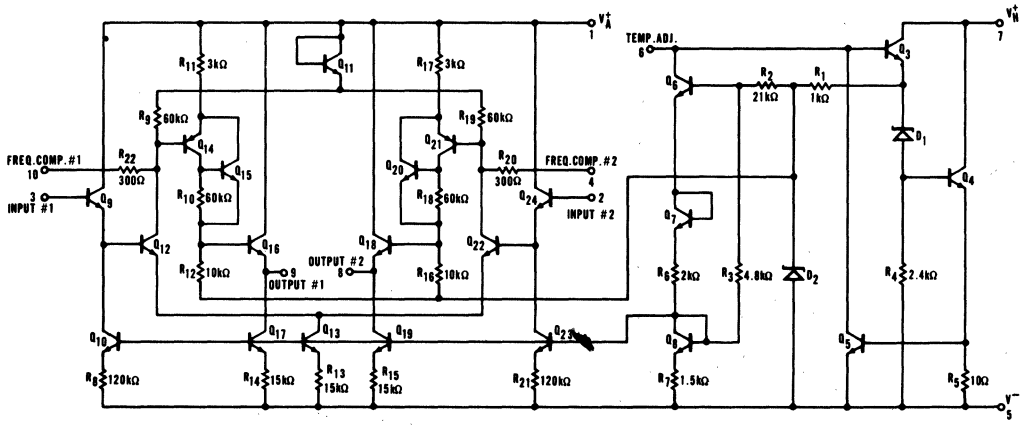
(In accordance with JEDEC TO-100)



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

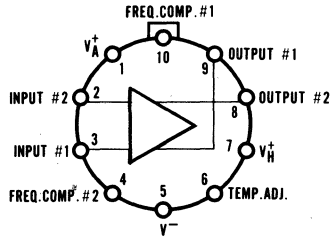
ORDER PART NO. U5J7727312

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM

(Top View)



*Planar is a patented Fairchild process.

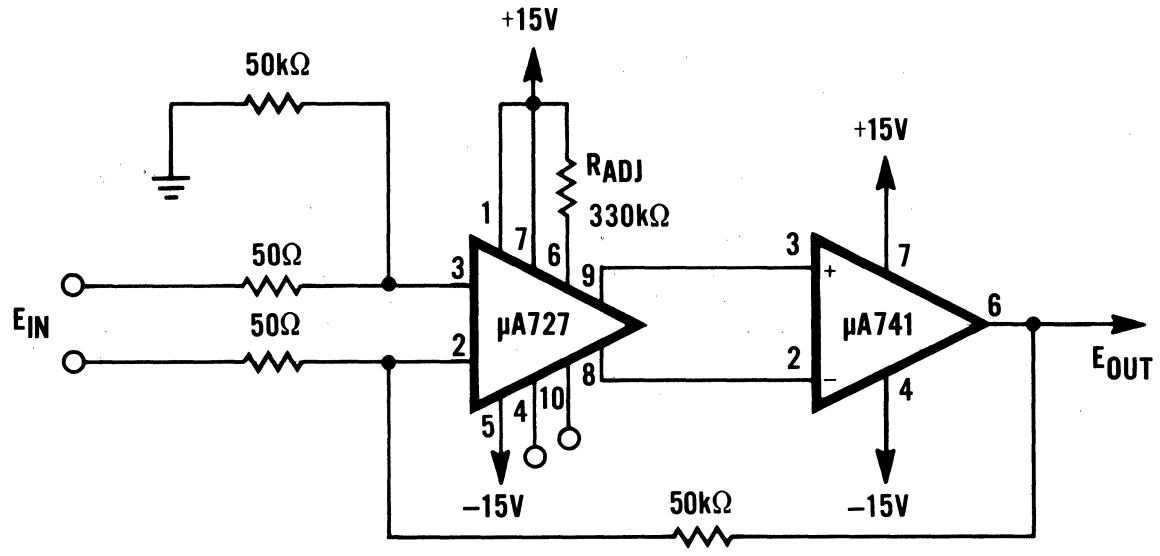
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq +125°C$, $V_H^+ = V_A^+ = +15\ V$, $V^- = -15\ V$, $R_{ADJ} = 330\ k\Omega$, unless otherwise specified)

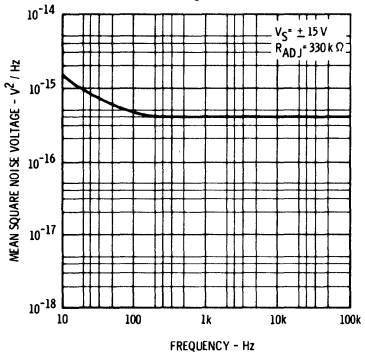
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\ \Omega$		2.0	10	mV
Input Offset Current			2.5	15	nA
Input Bias Current			12	40	nA
Input Offset Voltage Drift	$R_S \leq 50\ \Omega$, $+25°C \leq T_A \leq +125°C$		0.6	1.5	μV/°C
	$R_S \leq 50\ \Omega$, $-55°C \leq T_A \leq +25°C$		0.6	1.5	μV/°C
Input Offset Current Drift	$+25°C \leq T_A \leq +125°C$		2.0		pA/°C
	$-55°C \leq T_A \leq +25°C$		2.0		pA/°C
Input Bias Current Drift	$-55°C \leq T_A \leq +125°C$		15		pA/°C
Differential Input Resistance			300		MΩ
Common Mode Input Resistance			1000		MΩ
Input Voltage Range		±12	±13		V
Supply Voltage Rejection Ratio	$R_S \leq 100\ k\Omega$		80		μV/V
Common Mode Rejection Ratio	$R_S \leq 100\ k\Omega$	80	100		dB
Output Resistance			1.0	4.0	kΩ
Output Common Mode Voltage		−6.0	−5.0	−4.0	V
Differential Output Voltage Swing		±5.0	±7.0	±10	V
Output Sink Current		10	30	80	μA
Differential Load Rejection			5.0	10	μV/μA
Differential Voltage Gain		60	100	250	
Low Frequency Noise	BW = 10 Hz to 500 Hz, $R_S \leq 50\ \Omega$		3.0		μVrms
Long Term Drift	$R_S \leq 50\ \Omega$		5.0		μV/week
Amplifier Supply Current	$T_A = +25°C$		1.0	2.0	mA
Heater Supply Current	$T_A = +25°C$		10	15	mA

TYPICAL X1000 CIRCUIT

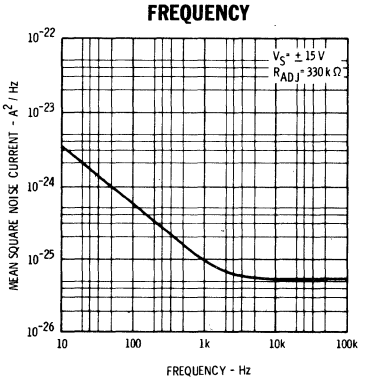


TYPICAL PERFORMANCE CURVES

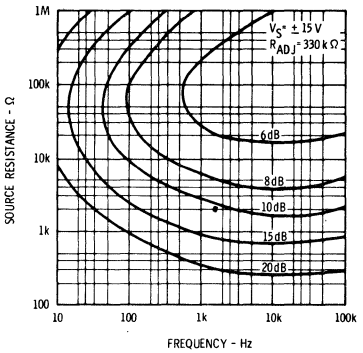
NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



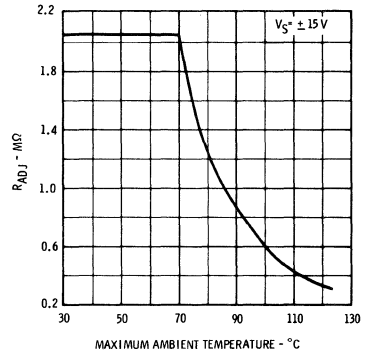
NOISE CURRENT AS A FUNCTION OF FREQUENCY



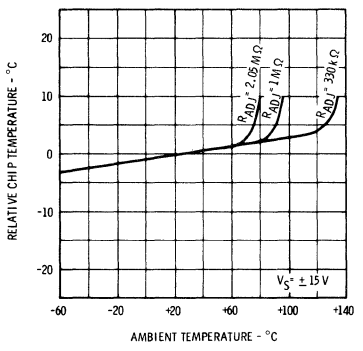
SPOT NOISE FIGURE CONTOURS



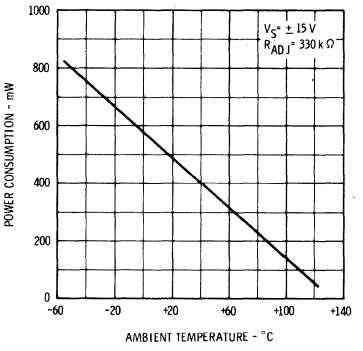
RECOMMENDED R_{ADJ} AS A FUNCTION OF MAXIMUM AMBIENT TEMPERATURE



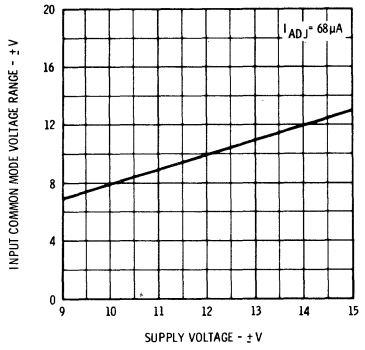
RELATIVE CHIP TEMPERATURE AS A FUNCTION OF AMBIENT TEMPERATURE



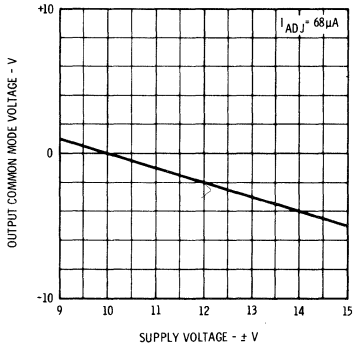
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



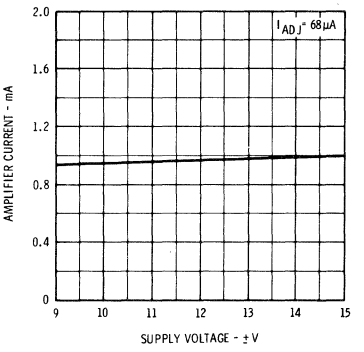
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



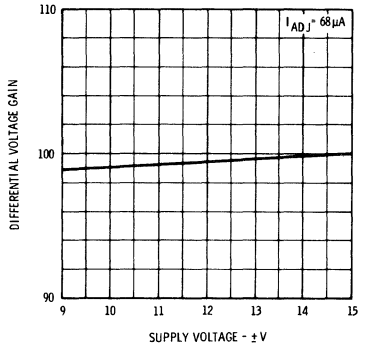
OUTPUT COMMON MODE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



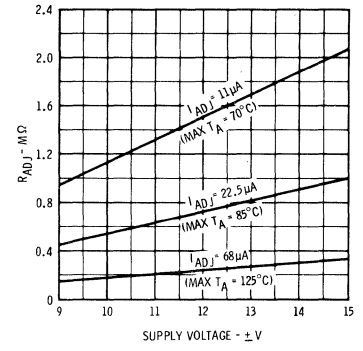
AMPLIFIER CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



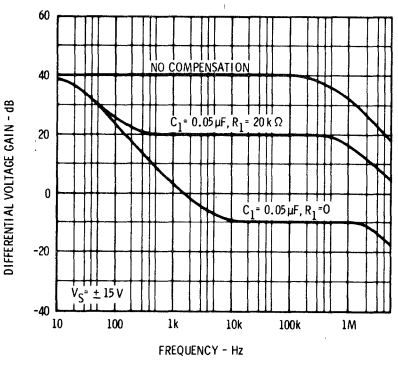
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



REQUIRED R_{ADJ} FOR CONSTANT I_{ADJ} AS A FUNCTION OF SUPPLY VOLTAGE



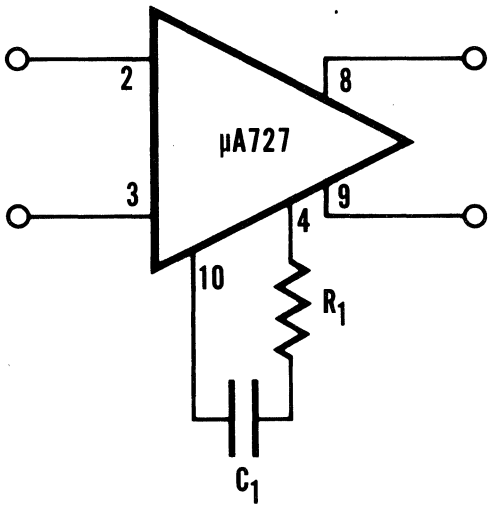
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF COMPENSATION



DEFINITION OF TERMS

INPUT OFFSET VOLTAGE — That voltage which must be applied between the input terminals to obtain zero differential output voltage.
INPUT OFFSET CURRENT — The difference in the currents into the two input terminals with the differential output at zero.
DIFFERENTIAL INPUT RESISTANCE — The resistance looking into either input terminal with the other grounded.
COMMON MODE INPUT RESISTANCE — The resistance looking into both inputs tied together.
INPUT BIAS CURRENT — The average of the two input currents.
INPUT VOLTAGE RANGE — A range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.
INPUT COMMON MODE REJECTION RATIO — The ratio of the input voltage range to the maximum change in input offset voltage over this range.
DIFFERENTIAL VOLTAGE GAIN — The ratio of the change in differential output voltage to the change in differential input voltage producing it.
DIFFERENTIAL OUTPUT VOLTAGE SWING — The peak differential output swing that can be obtained without clipping.
OUTPUT RESISTANCE — The resistance seen looking into either output terminal with the differential output at zero.
SUPPLY VOLTAGE REJECTION RATIO — The ratio of the change in input offset voltage to the change in supply voltage producing it.
OUTPUT COMMON MODE VOLTAGE — The average voltage at the two output terminals referred to ground.
OUTPUT SINK CURRENT — The maximum negative current that can be supplied by each output.
DIFFERENTIAL LOAD REJECTION — The ratio of the change in input offset voltage to the change in differential load current producing it.
I_{ADJ} — The current into terminal 6.

FREQUENCY COMPENSATION CIRCUIT



FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

μA727B

TEMPERATURE-CONTROLLED DIFFERENTIAL PREAMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

FEATURES

- **VERY LOW OFFSET DRIFTS**
- **HIGH INPUT IMPEDANCE**
- **WIDE COMMON MODE RANGE**

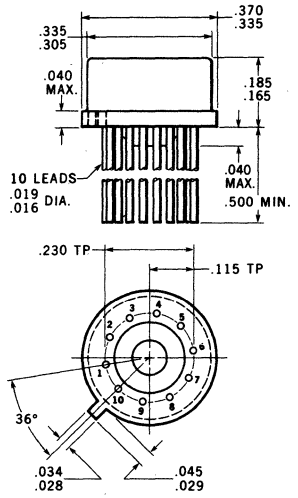
GENERAL DESCRIPTION — The μA727B is a monolithic, fixed gain, differential-input differential-output amplifier, constructed with the Fairchild Planar* epitaxial process, mounted in a high thermal-resistance package, and held at constant temperature by active regulator circuitry. The high gain and low standby dissipation of the regulator circuit give tight temperature control over a wide ambient temperature range. The device is intended for use as a self-contained input stage in very low-drift DC amplifiers, replacing complex chopper-stabilized amplifiers in such applications as thermo-couple bridges, strain gage transducers, and A to D converters. For full temperature range operation (−55°C to +125°C) see μA727 data sheet.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−20°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 second time limit)	300°C
Supply Voltage (Amplifier and Heater)	±18 V
Differential Input Voltage	±10 V
Common Mode Input Voltage	±15 V

PHYSICAL DIMENSIONS

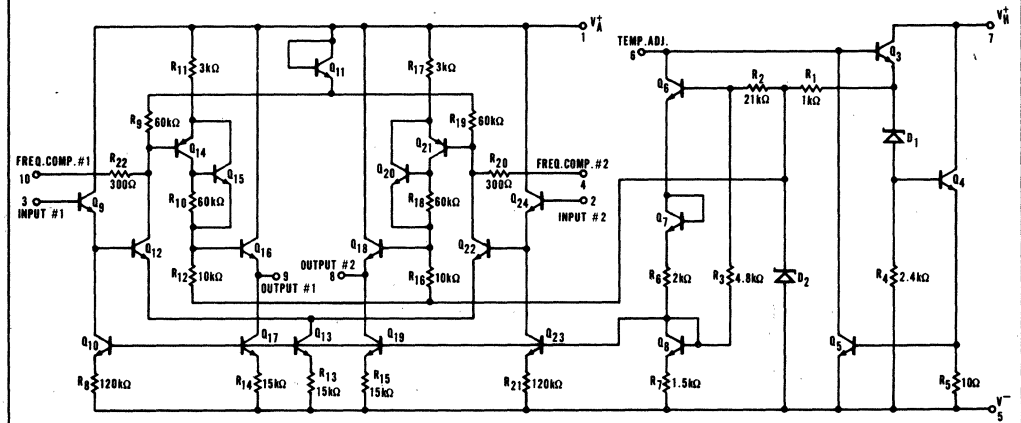
(in accordance with JEDEC TO-100)



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

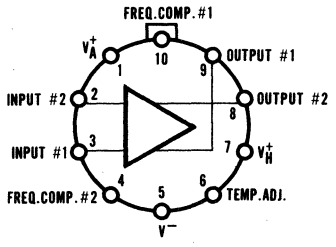
ORDER PART NO. U5J7727333

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM

(top view)



*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
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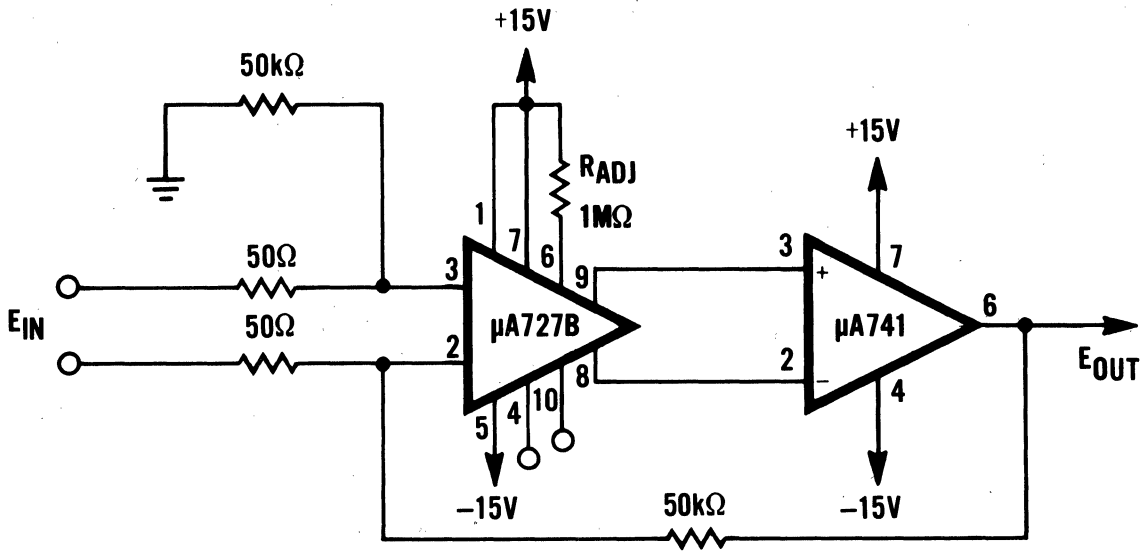
ELECTRICAL CHARACTERISTICS ($-20°C \leq T_A \leq +85°C$, $V_H^+ = V_A^+ = +15$ V, $V^- = -15$ V, $R_{ADJ} = 1M\Omega$, unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\ \Omega$		2.0		mV
Input Offset Current			2.5		nA
Input Bias Current			12		nA
Input Offset Voltage Drift	$R_S \leq 50\ \Omega$		0.6		μV/°C
Input Offset Current Drift			2.0		pA/°C
Input Bias Current Drift			15		pA/°C
Differential Input Resistance			300		MΩ
Common Mode Input Resistance			1000		MΩ
Input Voltage Range			±13		V
Supply Voltage Rejection Ratio	$R_S \leq 100$ kΩ		80		μV/V
Common Mode Rejection Ratio	$R_S \leq 100$ kΩ		100		dB
Output Resistance			1.0		kΩ
Output Common Mode Voltage			−5.0		V
Differential Output Voltage Swing			±7.0		V
Output Sink Current			30		μA
Differential Load Rejection			5.0		μV/μA
Differential Voltage Gain			100		
Low Frequency Noise	BW = 10 Hz to 500 Hz, $R_S \leq 50\ \Omega$		3.0		μV_{rms}
Long Term Drift	$R_S \leq 50\ \Omega$		5.0		μV/week
Amplifier Supply Current	$T_A = +25°C$		1.0		mA
Heater Supply Current	$T_A = +25°C$		10		mA

TYPICAL X1000 CIRCUIT



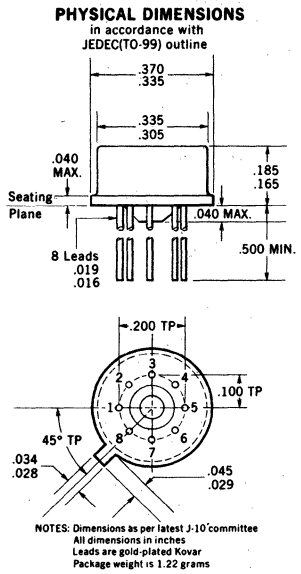
μA730
DIFFERENTIAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA730 is a differential amplifier constructed on a single silicon-chip using the Fairchild Planar* epitaxial process. This device has a wide range of applications since it has both a differential input and output; any combination of single-ended or differential configurations can be employed at its input and output. The emitter follower output stage gives this device a low output impedance making it useful as a preamplifier.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	15 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	2.5 to 5.5 V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

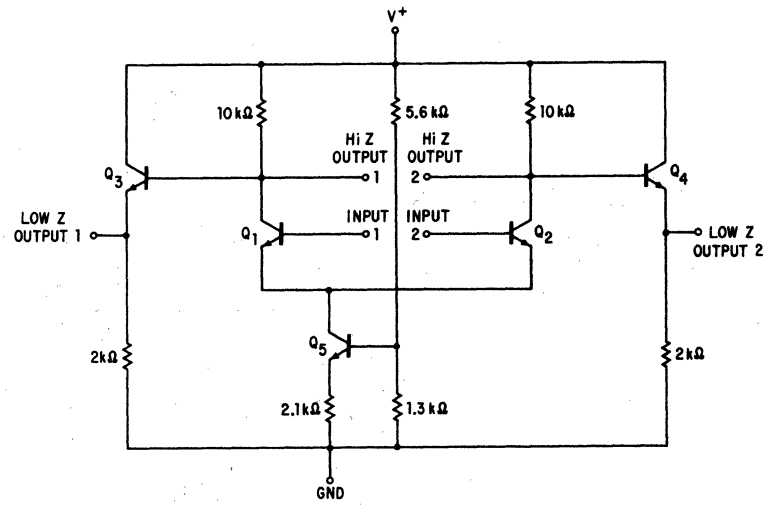
PHYSICAL DIMENSIONS
in accordance with
JEDEC(TO-99) outline



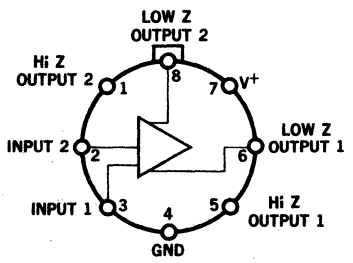
NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

Order Part No. U5B773031X

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top View)



Note: Pin 4 connected to case

NOTES:
(1) Rating applies for case temperature to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +105°C.

*Planar is a patented Fairchild process.

FAIRCHILD
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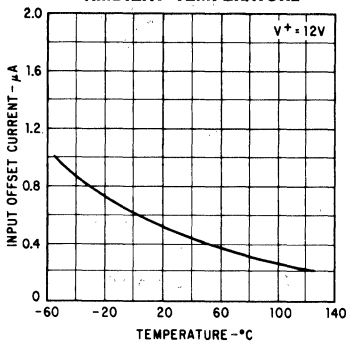
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V+ = 12.0$ V, and $V_{CM} = 3.5$ V unless otherwise specified)

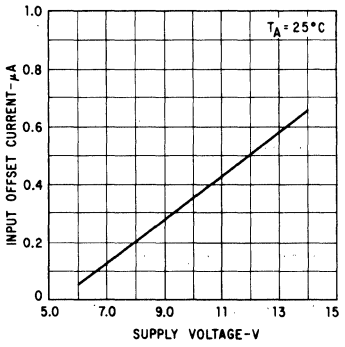
PARAMETER (See Definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		1.0	2.5	mV
Input Offset Current			0.5	1.5	μA
Input Bias Current			3.5	7.5	μA
Input Resistance		5.0	20		kΩ
Differential Voltage Gain	$R_L \geq 100$ kΩ	100	145	160	
Differential Distortion	$R_L \geq 100$ kΩ		80	300	mVpp
Bandwidth		1.0	1.5		MHz
Single-Ended Output Resistance			70	500	Ω
Output Voltage Swing	$R_L \geq 100$ kΩ	5.0	8.0		Vpp
Supply Current	$R_L \geq 100$ kΩ		9.5	13	mA
Power Consumption	$R_L \geq 100$ kΩ		114	156	mW
The following specifications apply for $-55°C \leq T_A \leq 125°C$:					
Input Offset Voltage	$R_S \leq 50\Omega$			3.5	mV
Input Offset Current	$T_A = +125°C$		0.2	1.5	μA
	$T_A = -55°C$		1.0	3.0	μA
Input Bias Current	$T_A = -55°C$		6.5	15	μA
Input Resistance		0.9			kΩ
Input Voltage Range		3.5		5.2	V
Common Mode Rejection Ratio	$R_S \leq 50\Omega$, $f \leq 1.0$ kHz, $+3.5\,V \leq V_{CM} \leq +5.2\,V$	70	85		dB
Differential Voltage Gain	$R_L \geq 100$ kΩ	90		175	
Common Mode Output Voltage		5.5	7.0	7.75	V
Output Resistance				600	Ω
Output Voltage Swing		4.5	6.8		Vpp
Supply Current	$T_A = -55°C$		10	15	mA
	$T_A = 125°C$		8.0	11	mA
Power Consumption	$T_A = -55°C$		120	180	mW
	$T_A = 125°C$		96	121	mW

TYPICAL PERFORMANCE CURVES

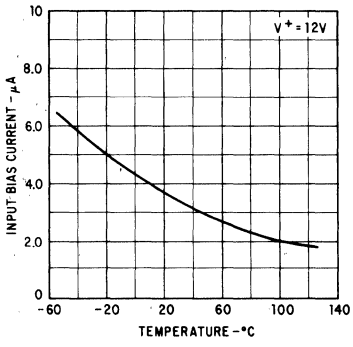
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

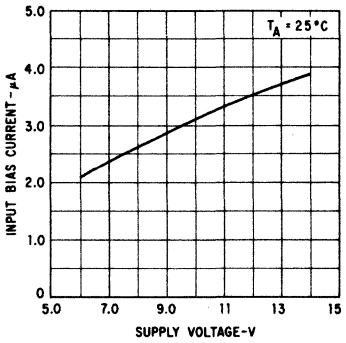


INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

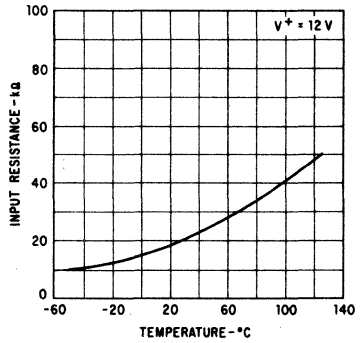


TYPICAL PERFORMANCE CURVES

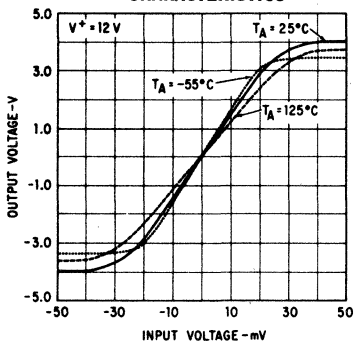
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



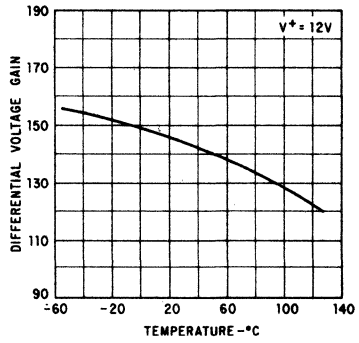
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



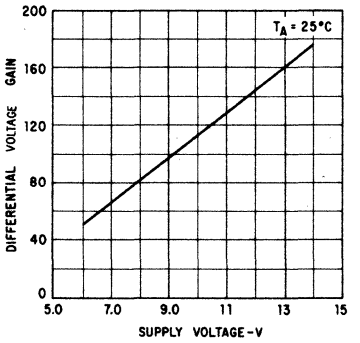
VOLTAGE TRANSFER CHARACTERISTICS



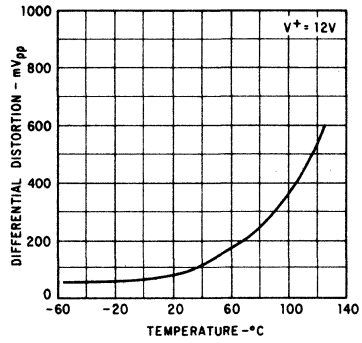
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



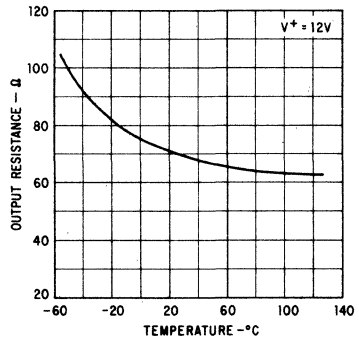
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



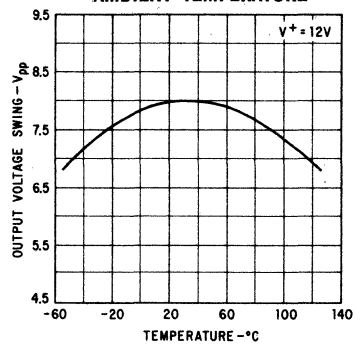
DIFFERENTIAL DISTORTION AS A FUNCTION OF AMBIENT TEMPERATURE



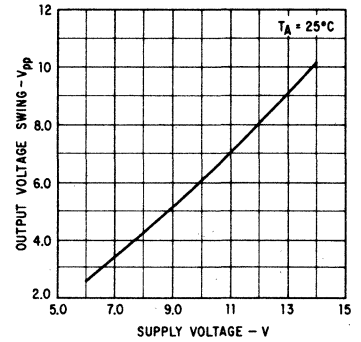
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



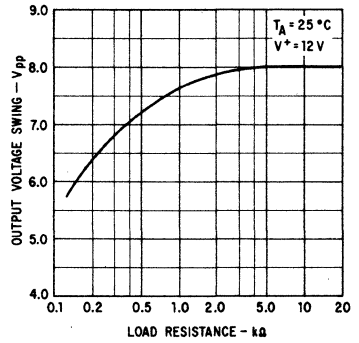
OUTPUT VOLTAGE SWING AS A FUNCTION OF AMBIENT TEMPERATURE



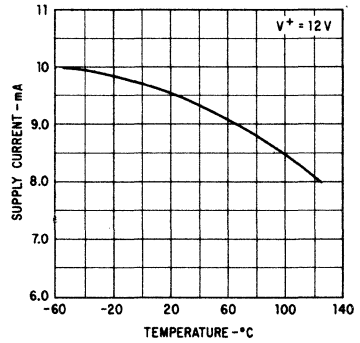
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



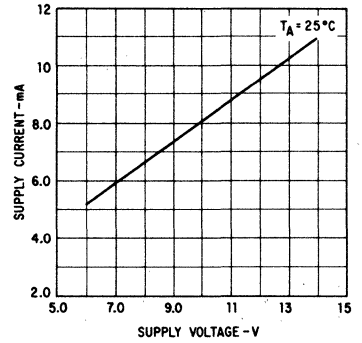
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

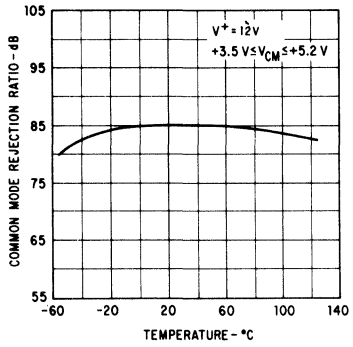


DEFINITION OF TERMS

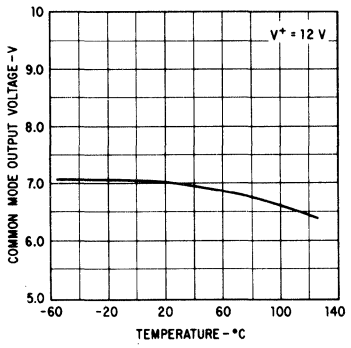
INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals to obtain zero differential output voltage.
INPUT OFFSET CURRENT—The difference in the currents into the two input terminals with the output at zero differential volts.
INPUT BIAS CURRENT—The average of the two input currents.
INPUT BIAS RESISTANCE—The resistance looking into either input terminal with the other grounded.
INPUT VOLTAGE RANGE—The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.
COMMON MODE REJECTION RATIO—The ratio of the input voltage range to the maximum change in input offset voltage over this range.
DIFFERENTIAL VOLTAGE GAIN—The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.
DIFFERENTIAL DISTORTION—The A.C. unbalance in the output common mode voltage produced by unsymmetrical output voltage swings.
BANDWIDTH—The frequency at which the differential voltage gain is 3 dB below its low frequency value.
OUTPUT RESISTANCE—The resistance seen looking into either output terminal with the output at differential null.
COMMON MODE OUTPUT VOLTAGE—The average voltage at the two output terminals referred to ground.
OUTPUT VOLTAGE SWING—The peak-to-peak output swing that can be obtained without clipping.
SUPPLY CURRENT—The current required from the power supply to operate the device with no load.
POWER CONSUMPTION—The DC power required to operate the amplifier with no load current.

TYPICAL PERFORMANCE CURVES

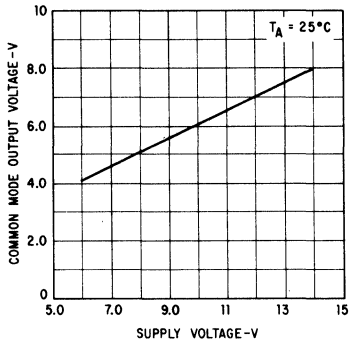
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

μA730C
DIFFERENTIAL AMPLIFIER
FAIRCHILD LINEAR INTEGRATED CIRCUITS

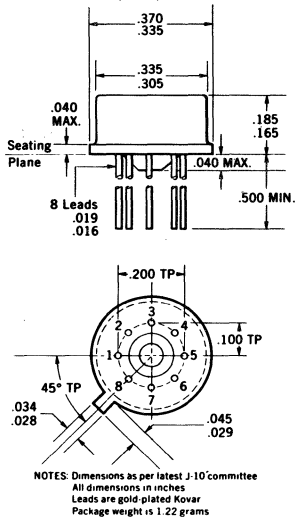
GENERAL DESCRIPTION – The μA730C is a differential amplifier constructed on a single silicon-chip using the Fairchild Planar* epitaxial process. This device has a wide range of applications since it has both a differential input and output; any combination of single-ended or differential configurations can be employed at its input and output. The emitter follower output stage gives this device a low output impedance making it useful as a preamplifier.

For full temperature range operation (−55°C to +125°C), see μA730 data sheet.

ABSOLUTE MAXIMUM RATINGS

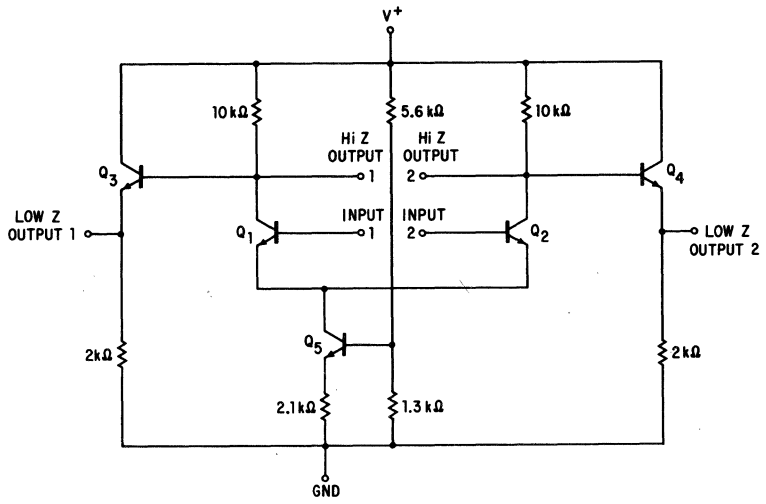
Supply Voltage	15 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	2.5 to 5.5 V
Internal Power Dissipation (Note 1)	300 mW
Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 seconds)	+300°C

PHYSICAL DIMENSIONS
in accordance with
JEDEC(TO-99) outline

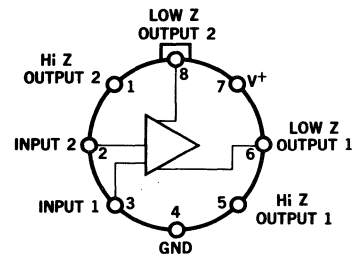


Order Part No. U5B7730393

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(Top View)



Note: Pin 4 connected to case

NOTES:
(1) Rating applies for ambient temperatures to +70°C.

*Planar is a patented Fairchild process.

FAIRCHILD
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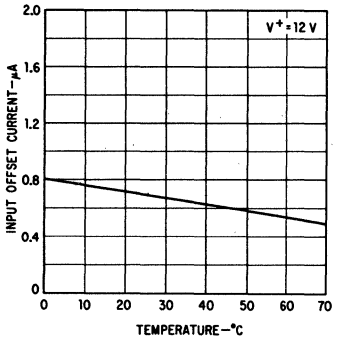
ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V+ = 12.0$ V, and $V_{CM} = 3.5$ V unless otherwise specified)

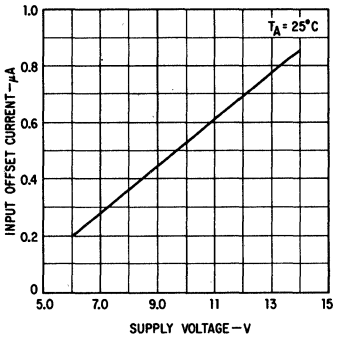
PARAMETER (See Definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 50\Omega$		2.0	5.0	mV
Input Offset Current			0.7	3.0	μA
Input Bias Current			4.5	16.0	μA
Input Resistance		2.5	15		kΩ
Differential Voltage Gain	$R_L \geq 100$ kΩ	100	135	160	
Differential Distortion	$R_L \geq 100$ kΩ		85	300	mVpp
Bandwidth		1.0	1.5		MHz
Single-Ended Output Resistance			70	500	Ω
Output Voltage Swing	$R_L \geq 100$ kΩ	5.0	8.0		Vpp
Supply Current	$R_L \geq 100$ kΩ		9.5	13	mA
Power Consumption	$R_L \geq 100$ kΩ		114	156	mW
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage	$R_S \leq 50\Omega$			7.5	mV
Input Offset Current	$T_A = +70°C$		0.5	3.0	μA
	$T_A = 0°C$		0.8	5.0	μA
Input Bias Current	$T_A = 0°C$		5.0	20	μA
Input Resistance		1.8			kΩ
Input Voltage Range		+3.5		+5.2	
Common Mode Rejection Ratio	$R_S \leq 50\Omega$, $f \leq 1.0$ kHz, $+3.5\text{ V} \leq V_{CM} \leq +5.2\text{ V}$	60	80		dB
Differential Voltage Gain	$R_L \geq 100$ kΩ	80		190	
Common Mode Output Voltage		5.0	7.0	8.0	V
Output Resistance				600	Ω
Output Voltage Swing		4.5	7.5		Vpp
Supply Current	$T_A = 0°C$		10	15	mA
	$T_A = +70°C$		8.8	13	mA
Power Consumption	$T_A = 0°C$		120	180	mW
	$T_A = +70°C$		106	156	mW

TYPICAL PERFORMANCE CURVES

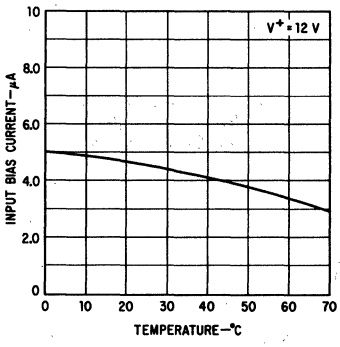
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

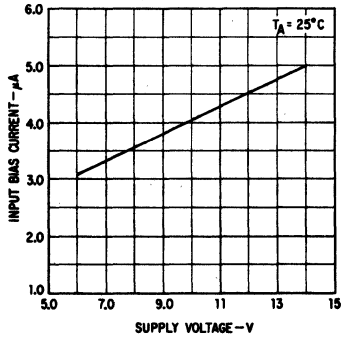


INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

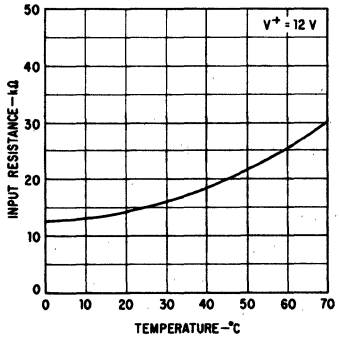


TYPICAL PERFORMANCE CURVES

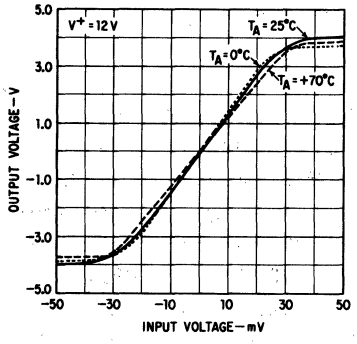
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



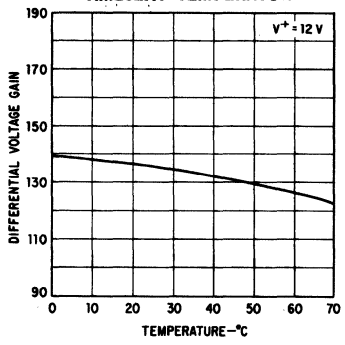
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



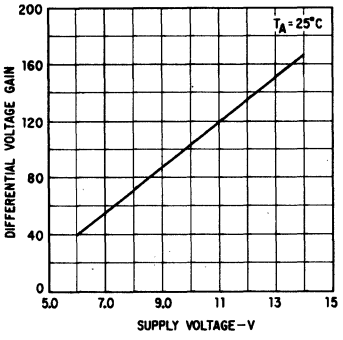
VOLTAGE TRANSFER CHARACTERISTICS



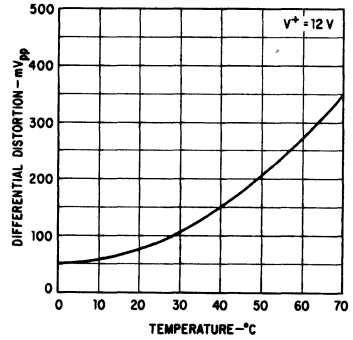
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



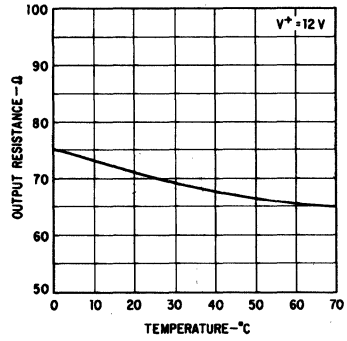
DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



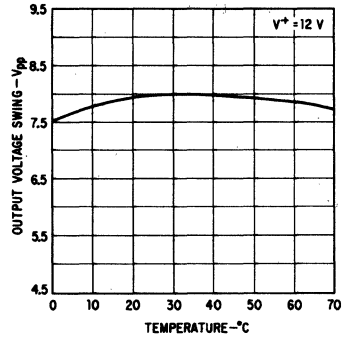
DIFFERENTIAL DISTORTION AS A FUNCTION OF AMBIENT TEMPERATURE



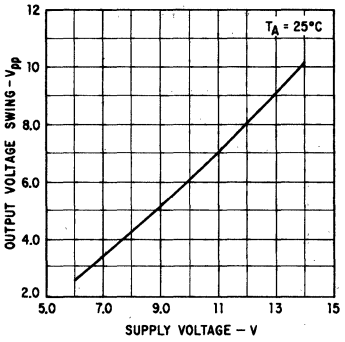
OUTPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



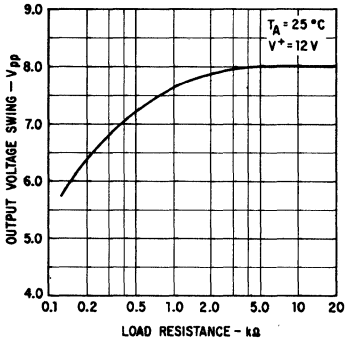
OUTPUT VOLTAGE SWING AS A FUNCTION OF AMBIENT TEMPERATURE



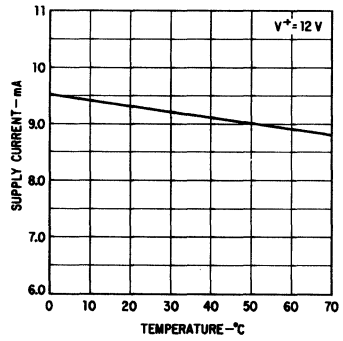
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



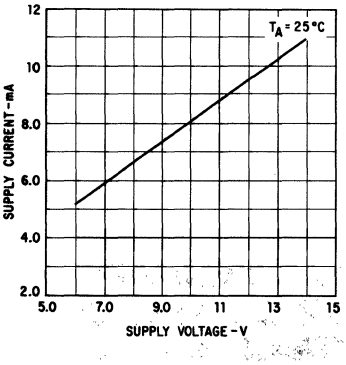
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

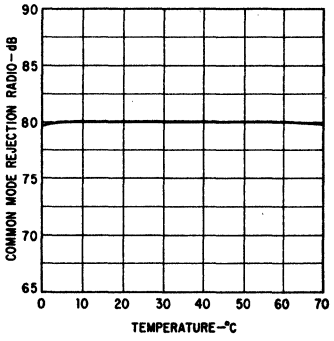


DEFINITION OF TERMS

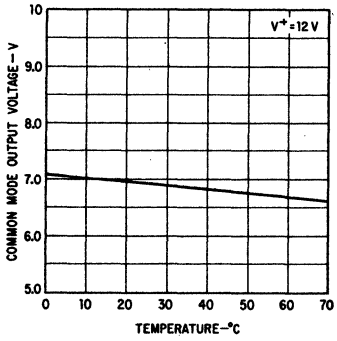
INPUT OFFSET VOLTAGE—That voltage which must be applied between the input terminals to obtain zero differential output voltage.
INPUT OFFSET CURRENT—The difference in the currents into the two input terminals with the output at zero differential volts.
INPUT BIAS CURRENT—The average of the two input currents.
INPUT BIAS RESISTANCE—The resistance looking into either input terminal with the other grounded.
INPUT VOLTAGE RANGE—The range of voltage which, if exceeded on either input terminal, could cause the amplifier to cease functioning properly.
COMMON MODE REJECTION RATIO—The ratio of the input voltage range to the maximum change in input offset voltage over this range.
DIFFERENTIAL VOLTAGE GAIN—The ratio of the change in the differential output voltage to the change in voltage between the input terminals producing it.
DIFFERENTIAL DISTORTION—The A.C. unbalance in the output common mode voltage produced by unsymmetrical output voltage swings.
BANDWIDTH—The frequency at which the differential voltage gain is 3 dB below its low frequency value.
OUTPUT RESISTANCE—The resistance seen looking into either output terminal with the output at differential null.
COMMON MODE OUTPUT VOLTAGE—The average voltage at the two output terminals referred to ground.
OUTPUT VOLTAGE SWING—The peak-to-peak output swing that can be obtained without clipping.
SUPPLY CURRENT—The current required from the power supply to operate the device with no load.
POWER CONSUMPTION—The DC power required to operate the amplifier with no load current.

TYPICAL PERFORMANCE CURVES

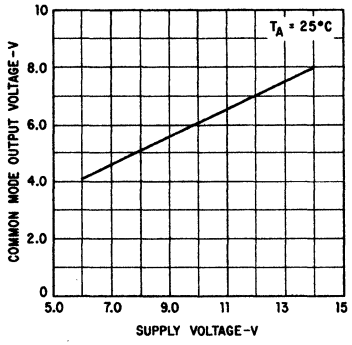
COMMON MODE REJECTION RATIO AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



COMMON MODE OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



FAIRCHILD
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μA737E

COLOR TV CHROMA DEMODULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA737E is a monolithic silicon integrated circuit which demodulates the chroma subcarrier information contained in a color television video signal and provides color-difference signals at the outputs.

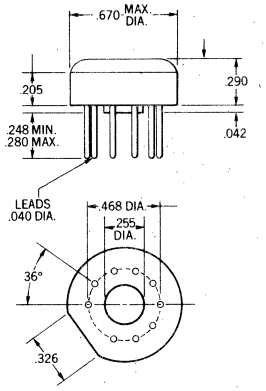
FEATURES

- **DOUBLY BALANCED DEMODULATION**
- **INTERNAL COLOR-DIFFERENCE MATRIX FOR NTSC COLOR TV**
- **10 VOLT PEAK-TO-PEAK E_B - E_Y OUTPUT**
- **PLUGS INTO A STANDARD 9-PIN MINIATURE TUBE SOCKET OR SOLDERS INTO A PRINTED BOARD**

ABSOLUTE MAXIMUM RATINGS

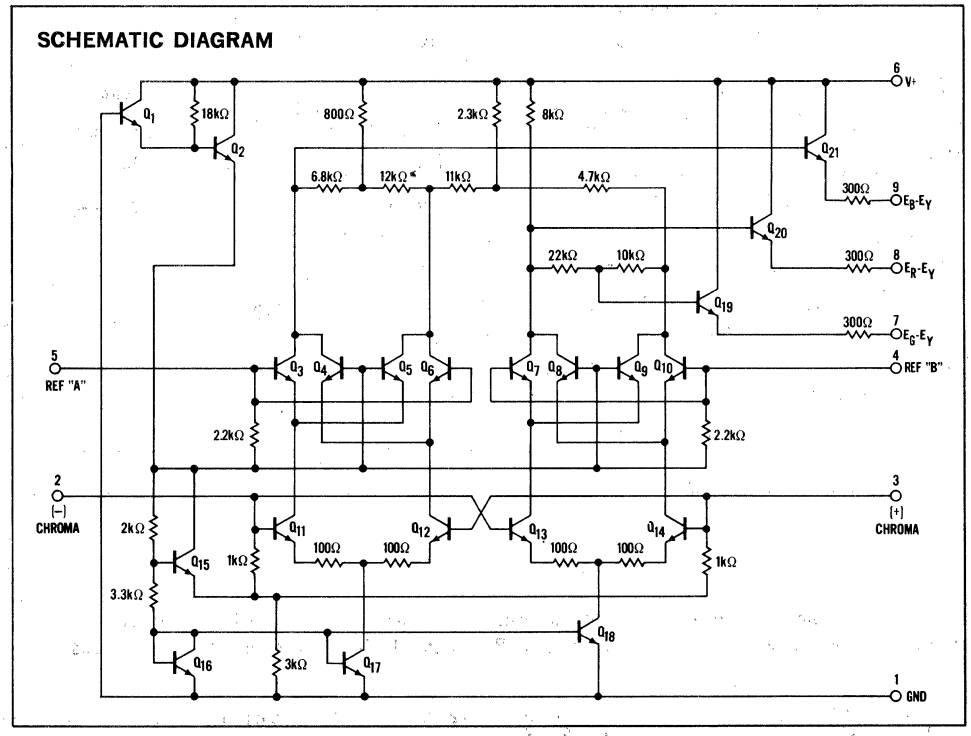
Supply Voltage	+28 V
Minimum Load Resistance	3 kΩ
Peak-to-Peak Reference Input Voltage	5 V
Peak-to-Peak Chroma Input Voltage	5 V
Internal Power Dissipation	450 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 seconds)	+260°C

PHYSICAL DIMENSIONS

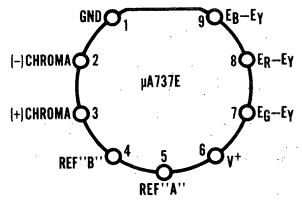


ORDER PART NO. U8F7737394

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



FAIRCHILD SEMICONDUCTOR
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313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = 24$ V, Test Circuit 1 unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	$e_C = 0$, $R_L = 1\ M\Omega$	4.5	8.0	11.5	mA
	$e_C = 0$, $R_L = 1\ M\Omega$, $T_A = 70°C$		8.0	12.0	mA
	$e_C = 0$	16.5	21	25.5	mA
	$e_C = 0$, $T_A = 70°C$		21		mA
Internal Power Dissipation	$e_C = 0$		320	410	mW
	$e_C = 0$, $T_A = 70°C$		320	420	mW
DC Voltage at any Output Terminal	$e_C = 0$	12.5	14.7	16.5	V
	$e_C = 0$, $T_A = 70°C$	12.0	14.3		V
Absolute Value of DC Difference Voltage between any Two Outputs	$e_C = 0$		0.2	1.0	V
DC Voltage at either Reference Terminal	$e_A = e_B = e_C = 0$		5.8		V
DC Voltage at either Chroma Terminal	$e_C = 0$		3.2		V
Reference Input Resistance	$e_C = 0$		1.7		kΩ
Reference Input Capacitance	$e_C = 0$		6.0		pF
Chroma Input Resistance			0.8		kΩ
Chroma Input Capacitance			5.0		pF
Peak-to-Peak Chroma Input Voltage	$E_B - E_Y = 5$Vp-p		0.4	0.7	V
Peak-to-Peak $E_R - E_Y$ Output Voltage	$E_B - E_Y = 5$Vp-p	3.5	3.8	4.2	V
Peak-to-Peak $E_G - E_Y$ Output Voltage	$E_B - E_Y = 5$Vp-p	0.75	1.0	1.25	V
Maximum Peak-to-Peak $E_B - E_Y$ Output Voltage	$e_C = 1.5$Vp-p	8.0	10		V
$E_B - E_Y$ Demodulation Angle	$E_B - E_Y = 5$Vp-p		3		Degrees
$E_R - E_Y$ Demodulation Angle	$E_B - E_Y = 5$Vp-p		109		Degrees
$E_G - E_Y$ Demodulation Angle	$E_B - E_Y = 5$Vp-p		259		Degrees
$E_R - E_Y$ Demodulation Angle relative to $E_B - E_Y$ Demodulation Angle	$E_B - E_Y = 5$Vp-p	101	106	111	Degrees
$E_B - E_Y$ Demodulation Angle relative to $E_G - E_Y$ Demodulation Angle	$E_B - E_Y = 5$Vp-p	96	104	112	Degrees
Highest Peak-to-Peak Demodulator AC Unbalance Voltage at any Output Terminal	$e_C = 0$		0.3	0.8	V

DEFINITIONS

Color-Difference Demodulation Angle — A color-difference demodulation angle is defined as the instantaneous phase of the (+) Chroma input signal which produces the most positive voltage at the respective color-difference output with the phase of Reference "A" taken at 3 degrees and the phase of Reference "B" taken at 106 degrees.

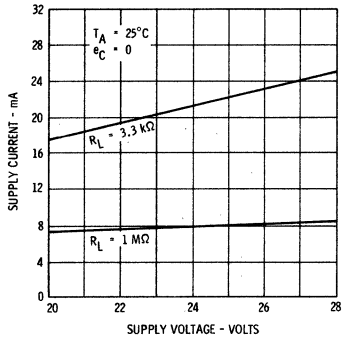
(+) Chroma Input — A composite chroma signal containing the burst at a phase of 180 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (+) Chroma input.

(—) Chroma Input — A composite chroma signal containing the burst at a phase of 0 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (—) Chroma input.

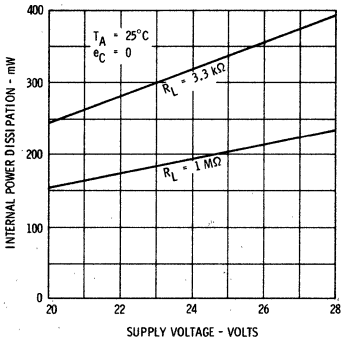
TYPICAL ELECTRICAL CHARACTERISTICS

(TEST CIRCUIT 1 UNLESS OTHERWISE SPECIFIED)

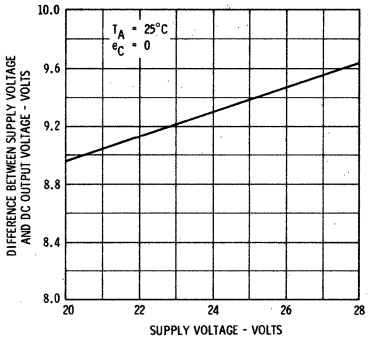
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



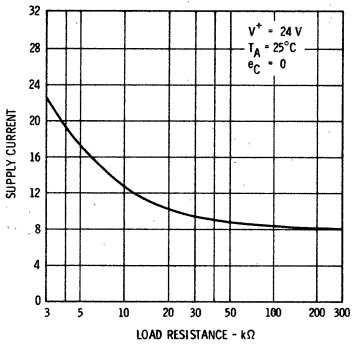
INTERNAL POWER DISSIPATION VERSUS SUPPLY VOLTAGE



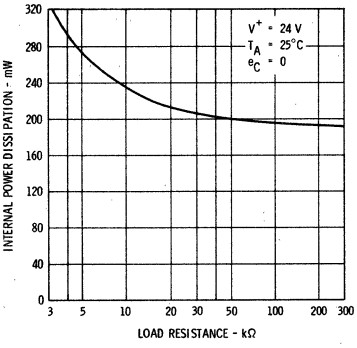
DIFFERENCE BETWEEN THE SUPPLY VOLTAGE AND THE DC VOLTAGE AT ANY OUTPUT VERSUS SUPPLY VOLTAGE



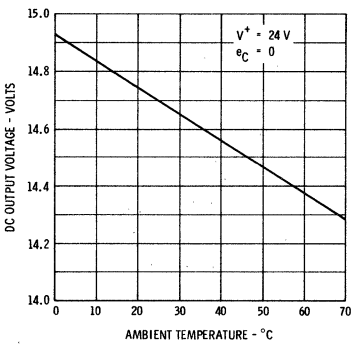
SUPPLY CURRENT VERSUS LOAD RESISTANCE



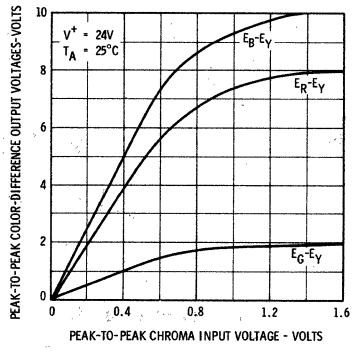
INTERNAL POWER DISSIPATION VERSUS LOAD RESISTANCE



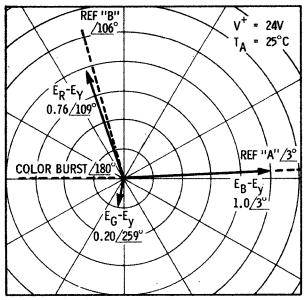
DC VOLTAGE AT ANY OUTPUT VERSUS AMBIENT TEMPERATURE



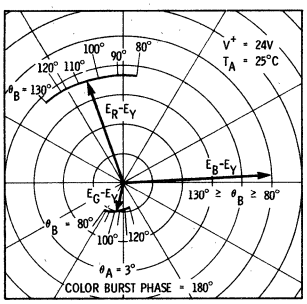
DEMODULATION LINEARITY



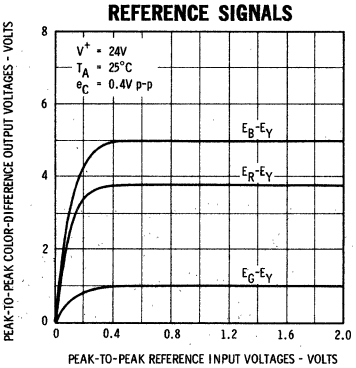
DEMODULATION ANGLES AND RELATIVE GAINS



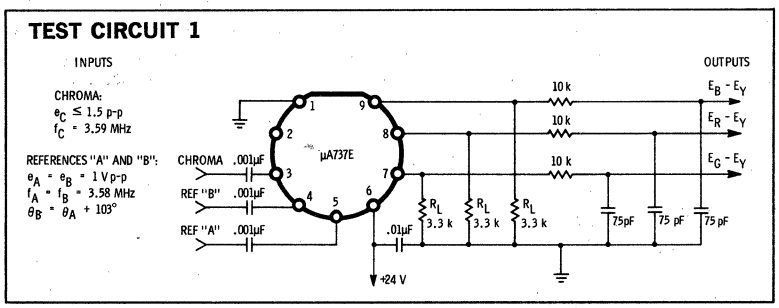
DEMODULATION SENSITIVITY TO RELATIVE PHASING OF REFERENCE SIGNALS



DEMODULATION SENSITIVITY TO AMPLITUDE OF REFERENCE SIGNALS



TEST CIRCUIT 1



μA741

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

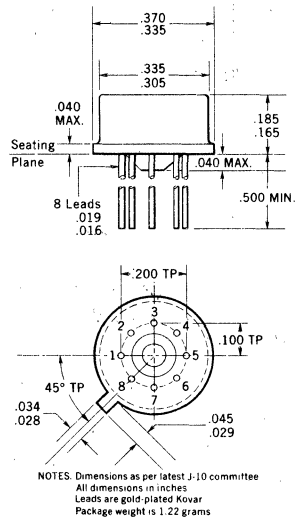
GENERAL DESCRIPTION — The μA741 is a high performance monolithic operational amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the μA741 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The μA741 is short-circuit protected, has the same pin configuration as the popular μA709 operational amplifier, but requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

PHYSICAL DIMENSIONS

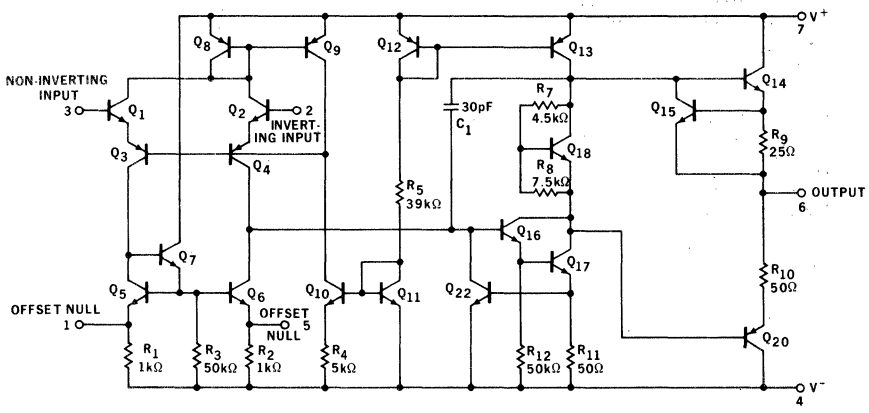
in accordance with JEDEC (TO-99) outline



NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

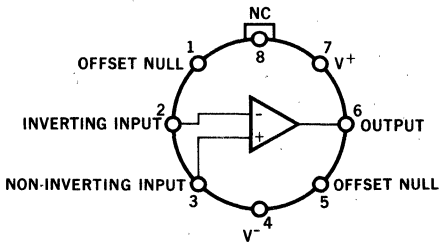
ORDER PART NO. U5B7741312

SCHEMATIC DIAGRAM



CONNECTION DIAGRAM

(TOP VIEW)



NOTE: PIN 4 CONNECTED TO CASE

NOTES:

(1) Rating applies for case temperatures to 125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.

(2) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.

(3) Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

*Planar is a patented Fairchild process.

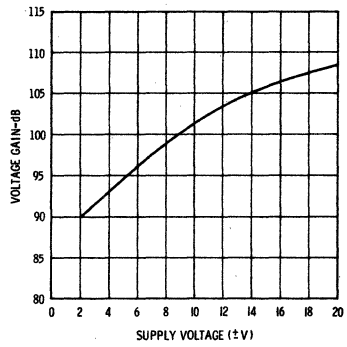
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

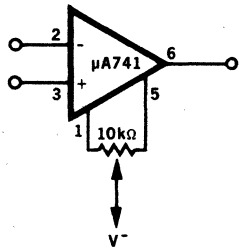
ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current			30	200	nA
Input Bias Current			200	500	nA
Input Resistance		0.3	1.0		MΩ
Large-Signal Voltage Gain	$R_L \geq 2$kΩ, $V_{out} = \pm 10$ V	50,000	200,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate (unity gain)	$R_L \geq 2$ kΩ		0.5		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ			6.0	mV
Input Offset Current				500	nA
Input Bias Current				1.5	μA
Large-Signal Voltage Gain	$R_L \geq 2$kΩ, $V_{out} = \pm 10$ V	25,000			
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V

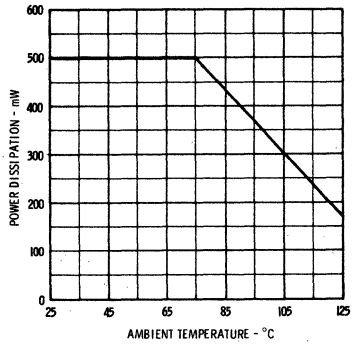
OPEN LOOP VOLTAGE GAIN



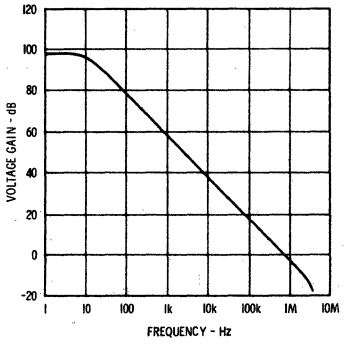
VOLTAGE OFFSET NULL CIRCUIT



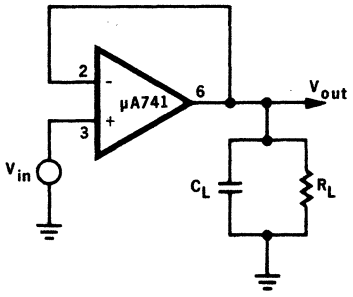
ABSOLUTE MAXIMUM POWER DISSIPATION



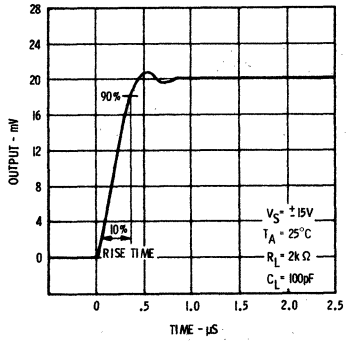
OPEN LOOP FREQUENCY RESPONSE



TRANSIENT RESPONSE TEST CIRCUIT



TRANSIENT RESPONSE



μA741C

HIGH PERFORMANCE OPERATIONAL AMPLIFIER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

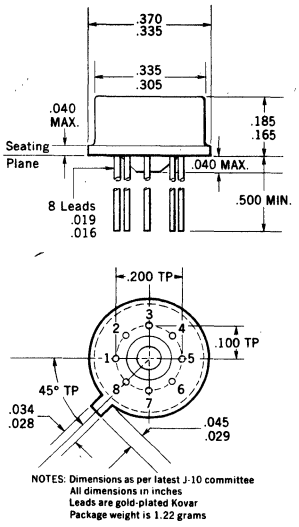
- **NO FREQUENCY COMPENSATION REQUIRED**
- **SHORT-CIRCUIT PROTECTION**
- **OFFSET VOLTAGE NULL CAPABILITY**
- **LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES**
- **LOW POWER CONSUMPTION**
- **NO LATCH UP**

GENERAL DESCRIPTION — The μA741C is a high performance monolithic operational amplifier constructed on a single silicon chip, using the Fairchild Planar* epitaxial process. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the μA741C ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The μA741C is short-circuit protected, has the same pin configuration as the popular μA709 operational amplifier, but requires no external components for frequency compensation. The internal 6dB/octave roll-off insures stability in closed loop applications. For full temperature range operation (−55°C to +125°C) see μA741 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 1)	±15 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 sec)	300°C
Output Short-Circuit Duration (Note 2)	Indefinite

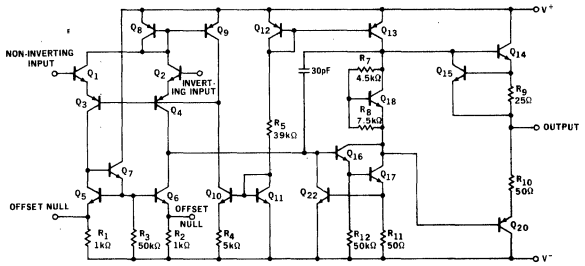
PHYSICAL DIMENSIONS
in accordance with
JEDEC (TO-99) outline



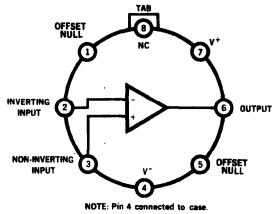
NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.22 grams

ORDER PART NO. U5B7741393

SCHEMATIC DIAGRAM

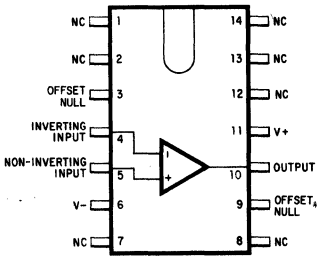


CONNECTION DIAGRAMS

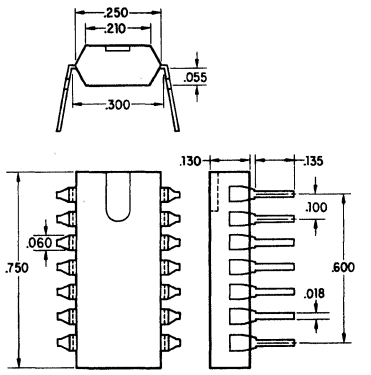


NOTE: Pin 4 connected to case.

(TOP VIEW)



TYPICAL DUAL IN-LINE PACKAGE



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows, .300 centers

ORDER PART NO. U6E7741393

NOTES:
(1) For supply voltages less than ±15 V, the absolute maximum input voltage is equal to the supply voltage.
(2) Short circuit may be to ground or either supply.

*Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
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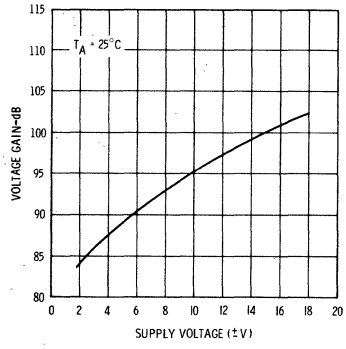
ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise specified)

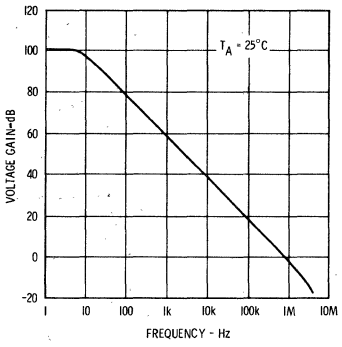
PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		2.0	6.0	mV
Input Offset Current			30	200	nA
Input Bias Current			200	500	nA
Input Resistance		0.3	1.0		MΩ
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	20,000	100,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10$ kΩ		30	150	μV/V
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L = 2$ kΩ				
	$C_L \leq 100$ pF				
Risetime			0.3		μs
Overshoot			5.0		%
Slew Rate (unity gain)	$R_L \geq 2$ kΩ		0.5		V/μs
The following specifications apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 10$ kΩ			7.5	mV
Input Offset Current				300	nA
Input Bias Current				800	nA
Large-Signal Voltage Gain	$R_L \geq 2$ kΩ, $V_{out} = \pm 10$ V	15,000			
Output Voltage Swing	$R_L \geq 2$ kΩ	±10			V

TYPICAL PERFORMANCE CURVES

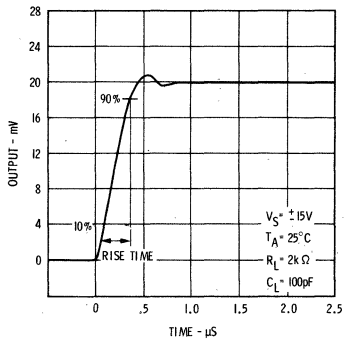
OPEN LOOP VOLTAGE GAIN



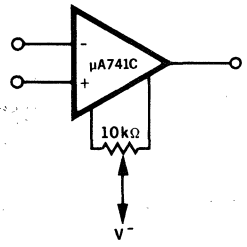
OPEN LOOP FREQUENCY RESPONSE



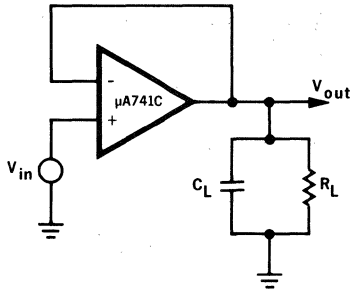
TRANSIENT RESPONSE



VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



LINEAR INTEGRATED CIRCUITS COMING SOON

Type	Function	Type	Function
μA715	High Speed Operational Amplifier	μA733	Video Amplifier
μA731	High Speed Dual Channel Sense Amplifier	μA739	Low Noise Dual Channel Amplifier
		μA740	Field Effect Operational Amplifier

μA715 — HIGH SPEED OPERATIONAL AMPLIFIER

DESCRIPTION

The μA715 is a monolithic, high speed, high gain, operational amplifier featuring high slew rate, low settling time, low offsets, high input impedance, wide common mode range, high output swing, and zero adjust. It is useful in A to D and D to A converters, phase locked loops, video amplifiers, sample and holds, and multiplexed analog gates where moderate speeds and bandwidths from D.C. to 30 MHz are required.

FEATURES

Input Impedance	10 MΩ
Open Loop Gain	45,000
Slew Rate at Unity Gain	20V/μS
SUPPLY VOLTAGES	±5 to ±18 V
TEMPERATURE RANGES	−55 to +125°C
	0 to +70°C
PACKAGES	TO-5, FLATPACK, and DIP

μA731 — HIGH SPEED DUAL CHANNEL SENSE AMPLIFIER

DESCRIPTION

The μA731 is designed for high speed core memories operating at cycle times down to 400 nS. The device will accept inputs from two sense lines and consists of two preamplifiers OR'd into a thresholding circuit which drives the output logic which can be used as a memory data resistor. The device features fast response time, tight threshold accuracy and CCSL output logic.

FEATURES

Threshold Accuracy	2 mV*
Threshold Range	0 to 50 mV
Propogation Delay	30 nS
Strobe Release Time Variation	±5 nS
SUPPLY VOLTAGES	±6 Volts
TEMPERATURE RANGE	−55 to +125°C
	0 to +70°C
PACKAGES	DIP and FLATPACK

*Worst case for unit to unit, 5% power supplies and 0 to +70°C temperature range.

μA733 — VIDEO AMPLIFIER

DESCRIPTION

The μA733 is a monolithic high speed differential input and output amplifier useful from D.C. to 75 MHz. It features fixed gain options, low phase shifts and high CMRR at high frequencies. It is useful as a pre-amplifier in magnetic type and disc files and in woven or plated wire or thin or thick film memories as well as general purpose video applications.

FEATURES

Voltage Gain	10,100 or 500*
Input Impedance	20 KΩ
Output Swing	±3 Volts
Bandwidth	75 MHz
SUPPLY VOLTAGES	±4 to ±8 Volts
TEMPERATURE RANGE	−55 to +125°C
	0 to +70°C
PACKAGES	TO-5, FLATPACK, and DIP

*Adjustable to intermediate values with single external pot.

μA739 — LOW NOISE DUAL CHANNEL AMPLIFIER

DESCRIPTION

The μA739 is a monolithic low noise dual channel preamplifier for magnetic stereo phonographs and tapes and for other applications requiring a dual operational amplifier. It features wide common mode range, moderate input resistance, compensation points to provide RIAA band shape and continuous short circuit protection.

FEATURES

Input Impedance	50 KΩ
Open Loop Gain	20,000
Output Swing	±13 V
Output Noise Voltage (RIAA 40 dB)	400 μV
SUPPLY VOLTAGE	±6 to ±18
TEMPERATURE RANGE	−55 to +125°C
	0 to +70°C
PACKAGE	DIP and FLATPACK

μA740 FIELD EFFECT OPERATIONAL AMPLIFIER

DESCRIPTION

The μA740 is a monolithic FET input high performance operational amplifier featuring ultra high input impedance, low input current, wide common mode range, short circuit protection, and zero adjust. It is internally compensated for unity gain, and is useful as an integrator, active filter, and other applications requiring high input impedance and low input currents.

FEATURES

Input Impedance	10^{11} Ω
Input Offset Current	50 pA
Open Loop Voltage Gain	100 dB
Slew Rate	8 V/μS
Output Swing	±13 V
SUPPLY VOLTAGES	±5 to ±20
TEMPERATURE RANGE	−55 to +125°C
	0 to +70°C
PACKAGE	TO-5, FLATPACK, and DIP