Special Circuits

SPECIAL CIRCUITS NUMERICAL INDEX

NOTE: The Special Circuits Cross Reference is included in CCSL Cross Reference.

9620
DUAL DIFFERENTIAL LINE RECEIVER
FAIRCHILD INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 9620 is a dual differential line receiver designed to receive differential digital data from transmission lines and operate over the military and industrial temperature ranges. It can receive ±500 mV of differential data in the presence of high level (±15 V) common mode voltages and deliver undisturbed CCSL logic to the output. In addition to line reception the 9620 can perform many functions, a few of which are presented in the applications section. It can interface with nearly all input logic levels including CML, CTμL, HLLDTμL, RTμL and CCSL. HLLDTμL logic can be provided by tieing the output to V_{CC2}(+12 V) through a resistor. The outputs can also be wire OR'ed. The 9620 offers the advantages of logic compatible voltages (+5 V, +12 V), CCSL output characteristics, and a flexible input array with a high common mode range. The direct inputs are provided in addition to the attenuated inputs (normally used) to allow the input attenuation and response time to be changed by use of external components.

FEATURES:

- **CCSL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE VOLTAGE RANGE**
- **WIRED-OR CAPABILITY**
- **DIRECT INPUTS (A_D, B_D)**
- **FULL MILITARY TEMPERATURE RANGE**
- **LOGIC COMPATIBLE SUPPLY VOLTAGES**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

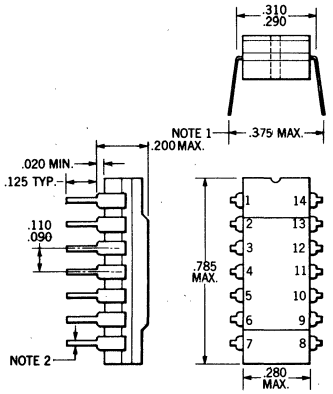
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC1} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage Referred to Ground (Attenuator Inputs)	±20 V
Voltage Applied to Outputs for High Output State	−0.5 V to +13.2 V
V_{CC2} Pin Potential to Ground Pin	V_{CC1} to +15 V

ORDER INFORMATION

Specify U6A9620XXX for 14 pin Dual In-Line package or U3I9620XXX for 14 pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

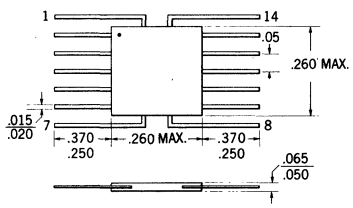
TYPICAL DUAL IN-LINE PACKAGE

In Accordance With
JEDEC (TO-116) Outline

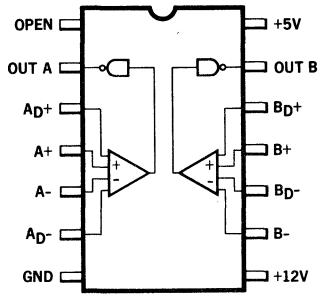


NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

14-PIN FLAT PACKAGE



LOGIC DIAGRAM



313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

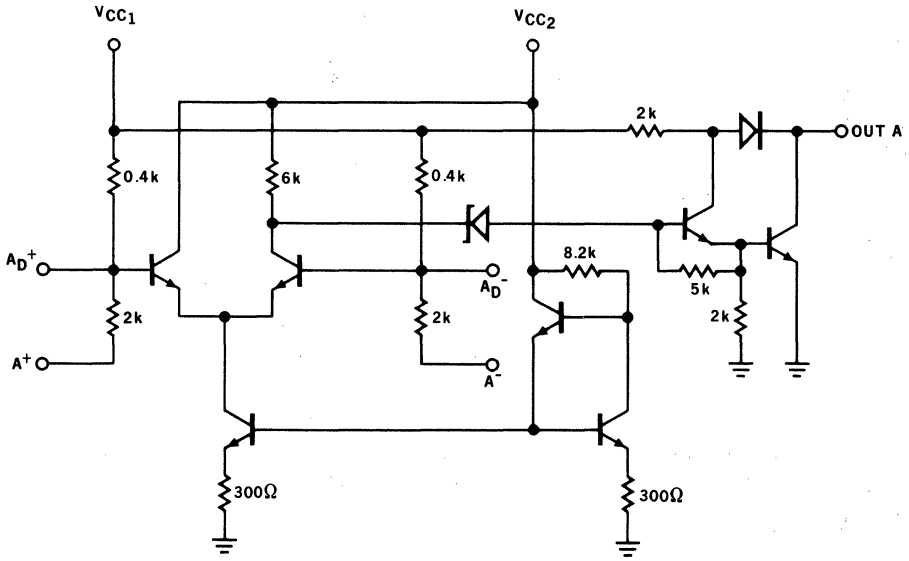
FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

ELECTRICAL CHARACTERISTICS (Temperature Range −55°C to +125°C, $V_{CC1} = 5.0\ V \pm 10\%$, $V_{CC2} = 12.0\ V \pm 10\%$)

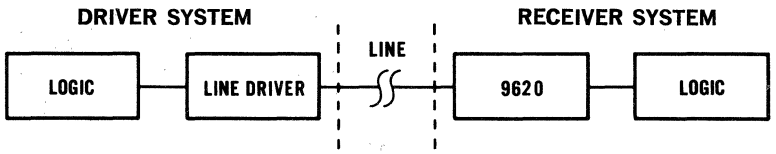
SYMBOL	CHARACTERISTIC	LIMITS −55°C MIN.	−55°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+125°C MIN.	+125°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OL}	Output Low Voltage		0.40		0.25	0.40		0.45	Volts	$V_{CC1} = 4.5\ V$ $I_{OL} = 15.0\ mA$	$V_{CC2} = 10.8\ V$ $*V_{DIFF} = 0.5\ V$
V_{OH}	Output High Voltage	2.8		3.0	3.3		2.9		Volts	$V_{CC1} = 4.5\ V$ $I_{OH} = -0.2\ mA$	$V_{CC2} = 10.8\ V$ $*V_{DIFF} = -0.5\ V$
I_{CEX}	Output Leakage Current		50			100		200	μA	$V_{CEX} = 13.2\ V$	
I_{SC}	Output Shorted Current			−1.4	−2.15	−3.1			mA	$V_{CC1} = 5.0\ V$	$V_{CC2} = 12.0\ V$
I_F	Input Forward Current		−3.1		−2.1	−3.0		−3.0	mA	$V_{CC1} = 5.0\ V$	$V_{CC2} = 12.0\ V$
†V_{TH}	Differential Input Threshold Voltage		500		120	500		500	mV	$V_{CC1} = 5.0\ V$	$V_{CC2} = 12.0\ V$
†V_{CM}	Common Mode Voltage	−15	15	−15	±17.5	15	−15	15	Volts	$V_{CC1} = 5.0\ V$ $*V_{DIFF} = 2.0\ V$	$V_{CC2} = 12.0\ V$
I_{VCC1}	5 V Supply Current		13		8.2	13		13	mA	$V_{CC1} = 5.5\ V$ $V_{CC2} = 13.2\ V$	+Input = 5.5 V −Input = 0 V
I_{VCC2}	12 V Supply Current		8.0		5.6	8.0		8.0	mA	$V_{CC1} = 5.5\ V$ $V_{CC2} = 13.2\ V$	+Input = 5.5 V −Input = 0 V
t_{pd+}	Turn-off Time				35	50			ns	$R_L = 3.9\ k\Omega$	$C_L = 30\ pF$
t_{pd-}	Turn-on Time				20	50			ns	$R_L = 390\ \Omega$	$C_L = 30\ pF$

†All input voltages are referred to the attenuated inputs (A^+, A^-, B^+, B^-)
*V_{DIFF} is a differential input voltage referred from A+ to A− and from B+ to B−.

Fig. 1 — SCHEMATIC DIAGRAM



STANDARD USAGE

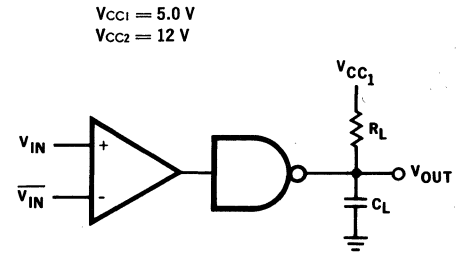


ELECTRICAL CHARACTERISTICS (Temperature Range 0°C to +75°C, $V_{CC1} = 5.0\ V \pm 5\%$, $V_{CC2} = 12.0\ V \pm 5\%$)

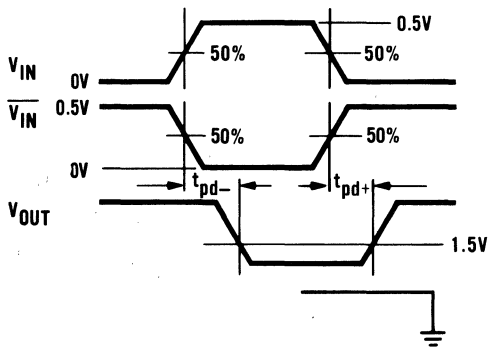
SYMBOL	CHARACTERISTIC	LIMITS 0°C MIN.	0°C MAX.	+25°C MIN.	+25°C TYP.	+25°C MAX.	+75°C MIN.	+75°C MAX.	UNITS	CONDITIONS & COMMENTS	
V_{OL}	Output Low Voltage		0.45		0.25	0.45		0.50	Volts	$V_{CC1} = 4.75\ V$ $I_{OL} = 15.0\ mA$	$V_{CC2} = 11.4\ V$ $*V_{DIFF} = 0.5\ V$
V_{OH}	Output High Voltage	2.8		3.0	3.3		2.9		Volts	$V_{CC1} = 4.75\ V$ $I_{OH} = -0.2\ mA$	$V_{CC2} = 12.6\ V$ $*V_{DIFF} = -0.5\ V$
I_{CEX}	Output Leakage Current		50			100		200	μA	$V_{CEX} = 5.25\ V$	
I_{SC}	Output Shorted Current			−1.4	−2.15	−3.1			mA	$V_{CC1} = 5.0\ V$	$V_{CC2} = 12.0\ V$
I_F	Input Forward Current		−3.1		−2.1	−3.0		−3.0	mA	$V_{CC1} = 5.0\ V$	$V_{CC2} = 12.0\ V$
†V_{TH}	Differential Input Threshold Voltage		500		120	500		500	mV	$V_{CC1} = 4.75\ V$	$V_{CC2} = 12.6\ V$
†V_{CM}	Common Mode Voltage	−12	12	−12	±17.5	12	−12	12	Volts	$V_{CC1} = 5.0\ V$ $*V_{DIFF} = 2.0\ V$	$V_{CC2} = 12.0\ V$
I_{VCC1}	5 V Supply Current		13.5		8.2	13.5		13.5	mA	$V_{CC1} = 5.25\ V$ $V_{CC2} = 12.6\ V$	+Input = 5.25 V −Input = 0 V
I_{VCC2}	12 V Supply Current		8.5		5.6	8.5		8.5	mA	$V_{CC1} = 5.25\ V$ $V_{CC2} = 12.6\ V$	+Input = 5.25 V −Input = 0 V
t_{pd+}	Turn-off Time				35	75			ns	$R_L = 3.9\ k\Omega$	$C_L = 30\ pF$
t_{pd-}	Turn-on Time				20	75			ns	$R_L = 390\ \Omega$	$C_L = 30\ pF$

†All input voltages are referred to the attenuated inputs (A^+, A^-, B^+, B^-)
*V_{DIFF} is a differential input voltage referred from A+ to A— and from B+ to B—.

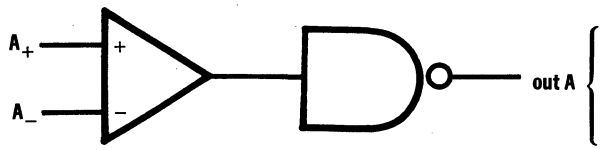
Fig. 2 — SWITCHING TIME TEST CIRCUIT

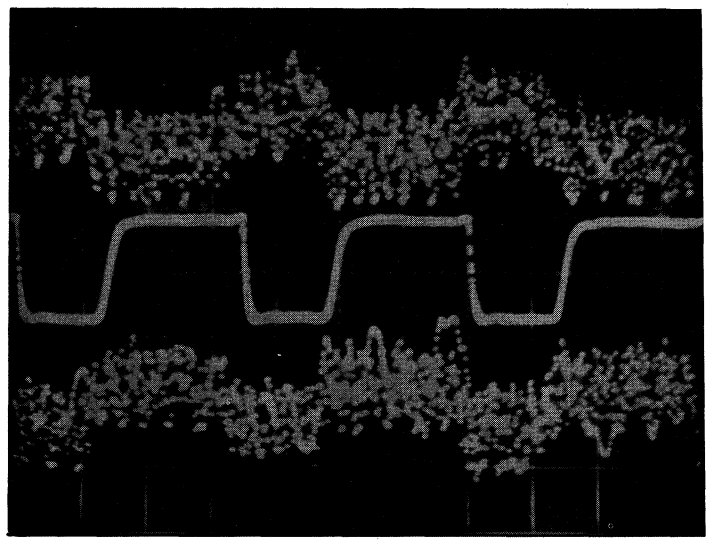


WAVEFORMS



Photograph of a 9620 switching differential data in the presence of high common mode noise.

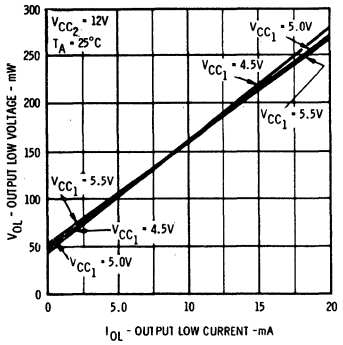




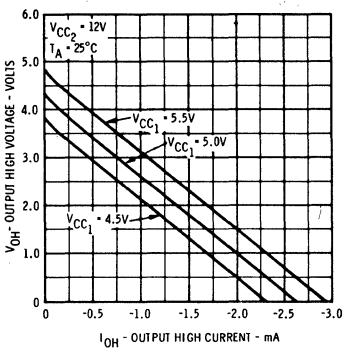
VERT = 2.0 V/div. HORIZ = 50 ns/div.

TYPICAL ELECTRICAL CHARACTERISTICS

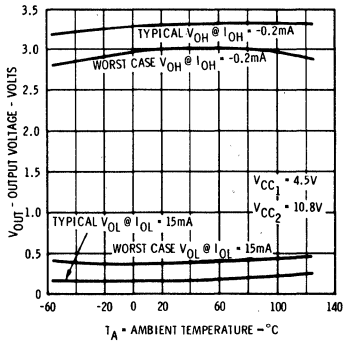
TYPICAL OUTPUT LOW VOLTAGE VERSUS OUTPUT LOW CURRENT



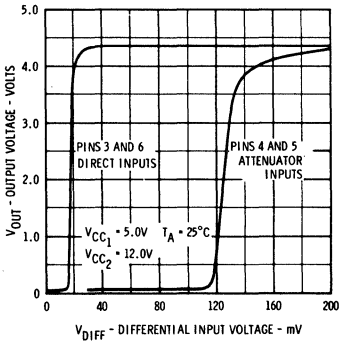
TYPICAL OUTPUT HIGH VOLTAGE VERSUS OUTPUT HIGH CURRENT



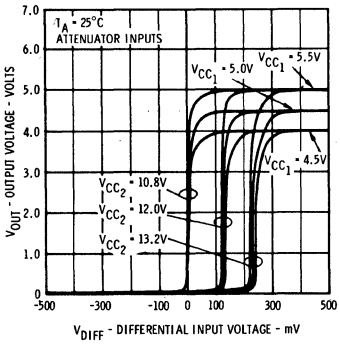
LOGIC LEVELS VERSUS AMBIENT TEMPERATURE



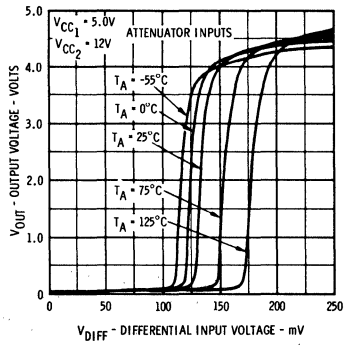
TYPICAL V_{out} VERSUS V_{DIFF} TRANSFER CHARACTERISTIC



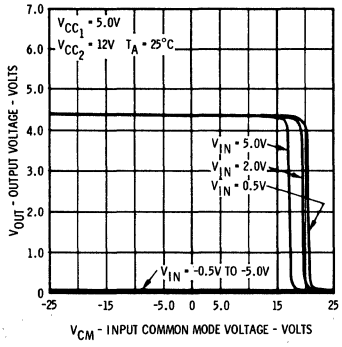
TYPICAL V_{out} VERSUS V_{DIFF} TRANSFER CHARACTERISTIC



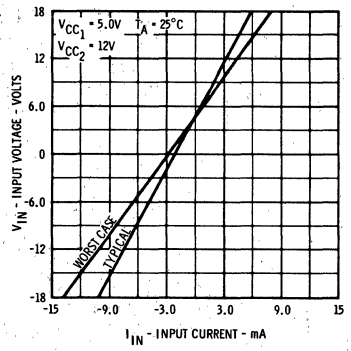
TYPICAL V_{out} VERSUS V_{DIFF} TRANSFER CHARACTERISTIC



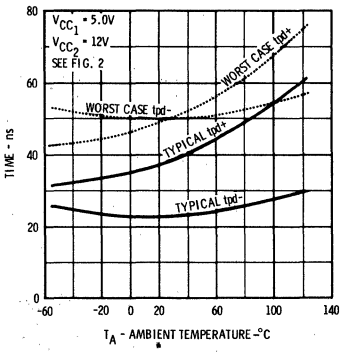
TYPICAL V_{out} VERSUS V_{CM} CHARACTERISTICS



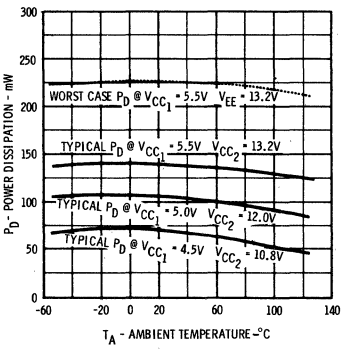
INPUT VOLTAGE VERSUS INPUT CURRENT



SWITCHING TIME VERSUS AMBIENT TEMPERATURE

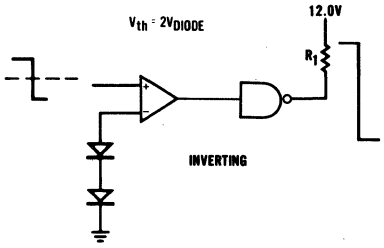


POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



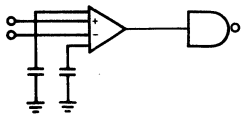
APPLICATIONS

DIGITAL COMPARATOR WITH DIODE REFERENCE AND HIGH LEVEL LOGIC OUT

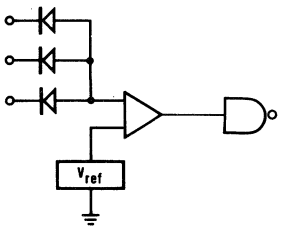


$R_1 \geq 750\ \Omega$

DIGITAL DIFFERENTIAL LINE RECEIVER WITH INPUTS ROLLED OFF

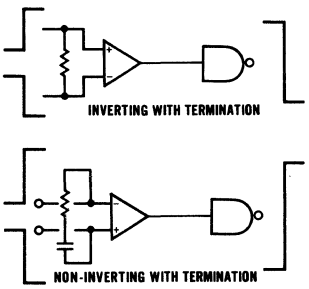


EXPANDED INTERFACE

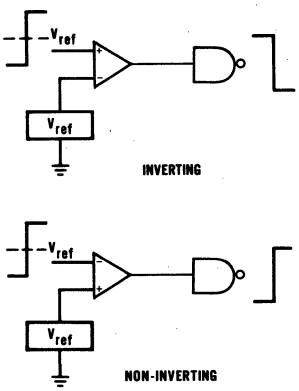


V_{ref} = Resistor, Diodes, or Supply

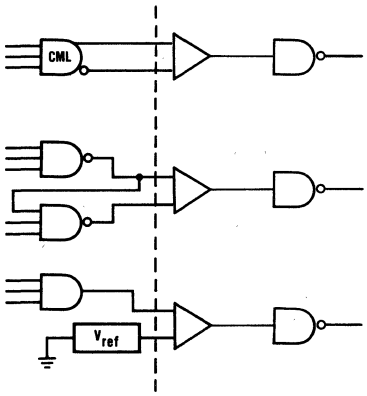
DIGITAL DIFFERENTIAL AMPLIFIER (Line Receiver)



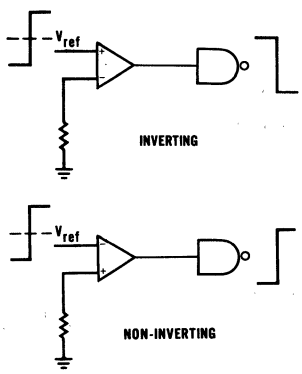
DIGITAL COMPARATOR



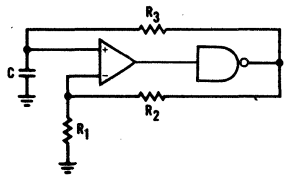
INTERFACING METHODS



DIGITAL COMPARATOR WITH RESISTIVE DIVIDER AS REFERENCE

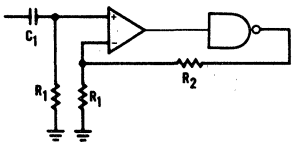


MULTIVIBRATOR



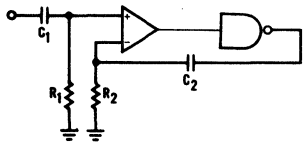
TYPICALLY
$R_1 = 1.6\ k\Omega$, $R_2 = 2.7\ k\Omega$, $T = 1.3\ R_3C$

A.C. COUPLED DIGITAL AMPLIFIER WITH HYSTERESIS



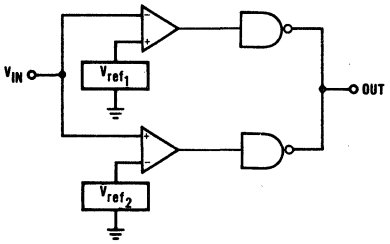
TYPICALLY
$R_1 = 1.6\ k\Omega$, $R_2 = 2.7\ k\Omega$

MONOSTABLE MULTIVIBRATOR NEGATIVE EDGE TRIGGERING



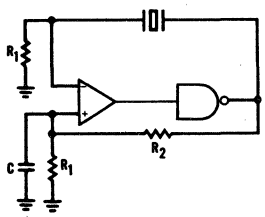
TYPICALLY
$C_1 = 0.1\ \mu F$, $R_1 = 1.2\ k\Omega$, $R_2 = 1.0\ k\Omega$
Pulse Width $= 50\ ns + 3.15 \times 10^3\ C_2$

DOUBLE-ENDED COMPARATOR



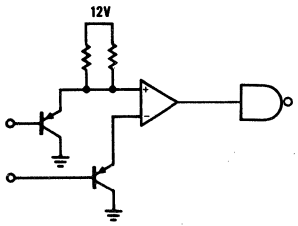
$V_{OH} = V_{Ref1} < V_{IN} < V_{Ref2}$

CRYSTAL CONTROLLED MULTIVIBRATOR



TYPICALLY
$R_1 = 1.6\ k\Omega$, $R_2 = 2.7\ k\Omega$, $C = \frac{R_2}{1000}$

HIGH INPUT IMPEDANCE LINE RECEIVER (Positive Signals Only)



9621
DUAL-LINE DRIVER
FAIRCHILD INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 9621 was designed to drive transmission lines in either a differential or a single-ended mode. Output clamp diodes and back-matching resistors for 130Ω twisted pair are provided. The output has the capability of driving high capacitance loads. It can typically switch >200 mA during transients.

FEATURES

- **CCSL COMPATIBILITY**
- **TRANSMISSION LINE BACK-MATCHING**
- **OUTPUT CLAMP DIODES**
- **HIGH CAPACITANCE DRIVE**
- **HIGH OUTPUT VOLTAGE**
- **MILITARY TEMPERATURE RANGE**

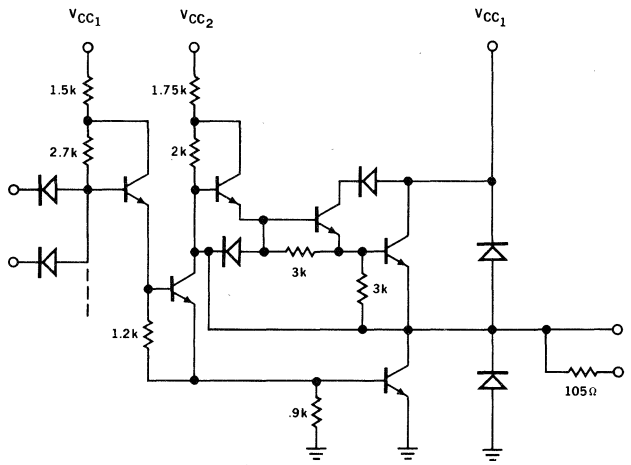
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC1} Pin Potential to Ground Pin	+3.8 V to +8 V
Input Voltage	−.5 V to +15 V
Voltage Applied to Outputs	−2 V to $+V_{CC1}$ + 1 V
V_{CC2} Pin Potential to Ground Pin	V_{CC1} to +15 V

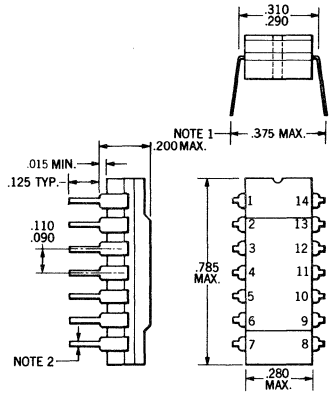
ORDER INFORMATION

Specify U6A9621XXX for 14 pin Dual In-Line Package or U319621XXX for 14 pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

SCHEMATIC DIAGRAM

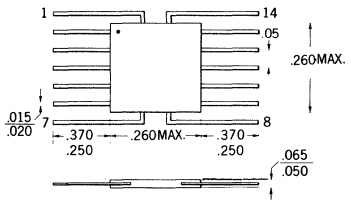


TYPICAL DUAL IN-LINE PACKAGE
Similar to
JEDEC (TO-116) Outline

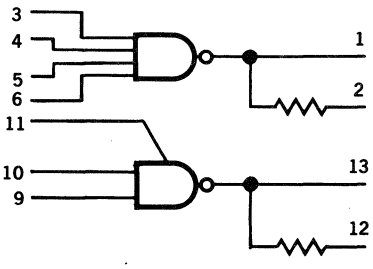


NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

14 PIN FLAT PACKAGE



LOGIC DIAGRAM



V_{CC_1}=14
V_{CC_2}=8
GND=7

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

ELECTRICAL CHARACTERISTICS
MILITARY TEMPERATURE RANGE −55°C to +125°C (UXX962151X)

SYMBOL	NOTES	CHARACTERISTICS	LIMITS							UNITS	CONDITIONS & COMMENTS	
			−55°C		+25°C			+125°C				
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OL}		Output Low Voltage		350		200	350		400	mV	I_{OL} = 20 mA	V_{CC1} = 4.5 V V_{CC2} = 10.8 V
V_{OH}		Output High Voltage	4.0		4.0	4.3		4.0		V	I_{OH} = −20 mA	V_{CC1} = 4.5 V V_{CC2} = 10.8 V
I_{SC}	1	Output "Short Circuit" Current			−180	−300				mA	V_{OUT} = 0 V	V_{CC1} = 4.5 V V_{CC2} = 10.8 V
I_{OL}	1	Output Low Current			150	200				mA	V_{OUT} = 5.0 V	V_{CC1} = 4.5 V V_{CC2} = 10.8 V
I_F		Input Forward Current		1.8		1.15	1.8		1.8	mA	V_F = 0 V	V_{CC1} = 5.5 V V_{CC2} = 13.2 V
I_R		Input Reverse Current		2.0		<1.0	2.0		5.0	μA	V_R = 5.5 V	V_{CC1} = 5.5 V V_{CC2} = 13.2 V
V_{OLR}	2	Resistive Output Low Voltage				380	500			V	I_{OL} = 2.8 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OHR}	2	Resistive Output High Voltage			4.0	4.2				V	I_{OH} = −2.3 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OLC}	3	Clamped Output Low Voltage				−1.0	−2.0			V	I_{OL} = −20 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OHC}	3	Clamped Output High Voltage				6.0	7.0			V	I_{OH} = 20 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
I_{CC1}		+5 V Supply Current		7.0		4.7	7.0		7.3	mA	Inputs Open	V_{CC1} = 5.5 V V_{CC2} = 13.2 V
I_{CC2}		+12 V Supply Current		9.8		6.5	9.8		9.8	mA		
t_{pd+}	4	Turn-Off Time				30	150			ns	C_L = 5000 pF	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
t_{pd-}	4	Turn-On Time				80	150			ns		
t_{pd+}		Turn-Off Time				13	25			ns	C_L = 30 pF	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
t_{pd-}		Turn-On Time				9	25			ns		
V_{IL}		Input Low Voltage		1.3		1.5	1.0		0.7	V	V_{CC1} = 5.5 V V_{CC2} = 10.8 V	
V_{IH}		Input High Voltage	2.2		2.0	1.7		1.8		V	V_{CC1} = 4.5 V V_{CC2} = 13.2 V	

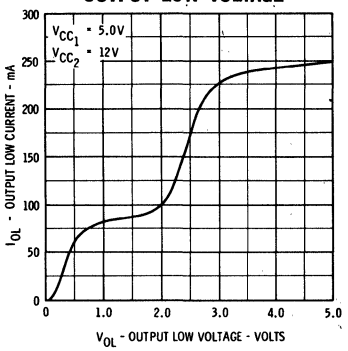
NOTES:
(1) Pulse tests to insure transient current handling (test time = 3 seconds maximum — one side only).
(2) Test output resistance including 105Ω output resistor.
(3) Tests output clamp diodes.
(4) With both sides loaded at T_A = +125°C, maximum frequency = 500 kHz for Dual In-Line package (θ_{JA} = 95°C/W) or 300 kHz for Ceramic Flat Pak (θ_{JA} = 165°C/W).

ELECTRICAL CHARACTERISTICS
INDUSTRIAL TEMPERATURE RANGE 0°C to +75°C (UXX962159X)

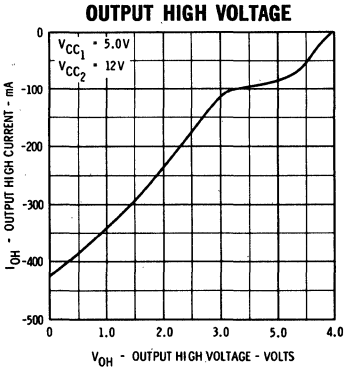
SYMBOL	NOTES	CHARACTERISTICS	LIMITS							UNITS	CONDITIONS & COMMENTS	
			0°C		+25°C			+75°C				
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.			
V_{OL}		Output Low Voltage		400		200	400		450	mV	I_{OL} = 20 mA	V_{CC1} = 4.75 V V_{CC2} = 11.4 V
V_{OH}		Output High Voltage	4.2		4.2	4.4		4.2		V	I_{OH} = −20 mA	V_{CC1} = 4.75 V V_{CC2} = 11.4 V
I_{SC}	1	Output "Short Circuit" Current			−100	−300				mA	V_{OUT} = 0 V	V_{CC1} = 4.75 V V_{CC2} = 11.4 V
I_{OL}	1	Output Low Current			75	200				mA	V_{OUT} = 5.0 V	V_{CC1} = 4.75 V V_{CC2} = 11.4 V
I_F		Input Forward Current		1.8		1.15	1.8		1.8	mA	V_F = 0 V	V_{CC1} = 5.25 V V_{CC2} = 12.6 V
I_R		Input Reverse Current		5.0		<1.0	5.0		10.0	μA	V_R = 5.5 V	V_{CC1} = 5.25 V V_{CC2} = 12.6 V
V_{OLR}	2	Resistive Output Low Voltage				380	500			V	I_{OL} = 2.8 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OHR}	2	Resistive Output High Voltage			4.0	4.2				V	I_{OH} = −2.3 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OLC}	3	Clamped Output Low Voltage				−1.0	−2.0			V	I_{OL} = −20 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
V_{OHC}	3	Clamped Output High Voltage				6.0	7.0			V	I_{OH} = 20 mA	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
I_{CC1}		+5 V Supply Current		7.0		4.7	7.0		7.3	mA	Inputs Open	V_{CC1} = 5.25 V V_{CC2} = 12.6 V
I_{CC2}		+12 V Supply Current		9.8		6.5	9.8		9.8	mA		
t_{pd+}	4	Turn-Off Time				30	200			ns	C_L = 5000 pF	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
t_{pd-}	4	Turn-On Time				80	200			ns		
t_{pd+}		Turn-Off Time				13	40			ns	C_L = 30 pF	V_{CC1} = 5.0 V V_{CC2} = 12.0 V
t_{pd-}		Turn-On Time				9	40			ns		
V_{IL}		Input Low Voltage		1.3		1.5	1.0		0.7	V	V_{CC1} = 5.25 V V_{CC2} = 12.6 V	
V_{IH}		Input High Voltage	2.2		2.0	1.7		1.8		V	V_{CC1} = 4.75 V V_{CC2} = 11.4 V	

NOTES:
(1) Pulse tests to insure transient current handling (test time = 3 seconds maximum — one side only).
(2) Test output resistance including 105Ω output resistor.
(3) Tests output clamp diodes.
(4) Maximum frequency = 500 kHz with both sides loaded at T_A = +75°C for both Dual In-Line package and Ceramic Flat Pak.

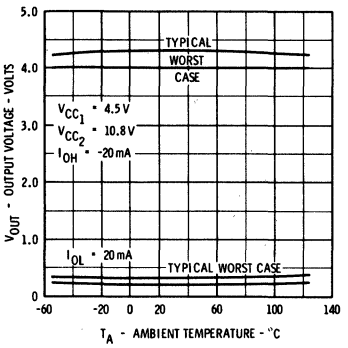
TYPICAL OUTPUT LOW CURRENT VERSUS OUTPUT LOW VOLTAGE



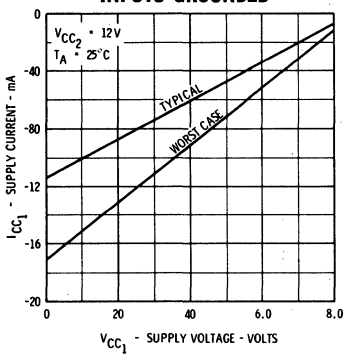
TYPICAL OUTPUT HIGH CURRENT VERSUS OUTPUT HIGH VOLTAGE



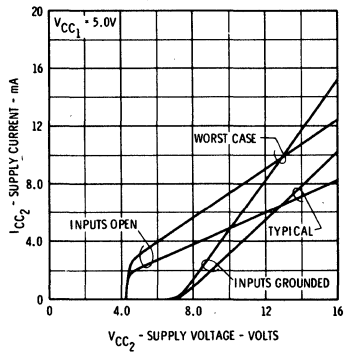
LOGIC LEVELS VERSUS AMBIENT TEMPERATURE



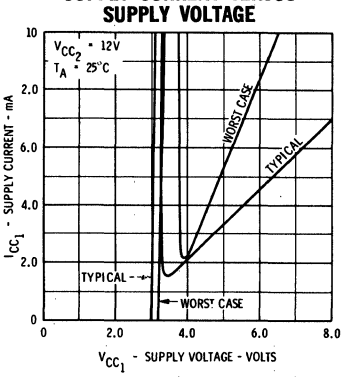
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE INPUTS GROUNDED



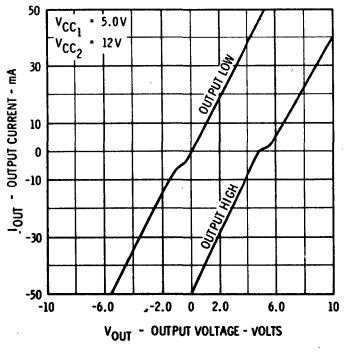
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE INPUTS OPEN



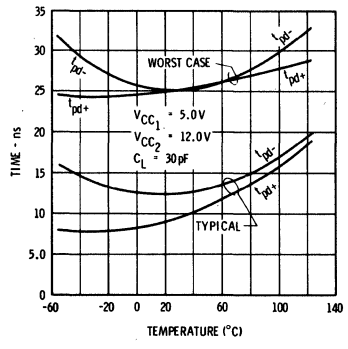
SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



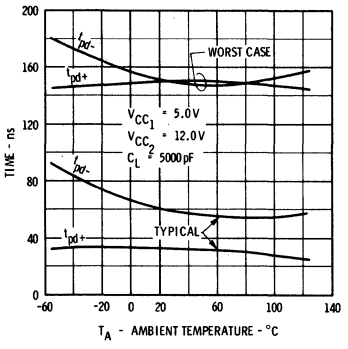
TYPICAL OUTPUT IMPEDANCE WITH BACK MATCHING RESISTORS



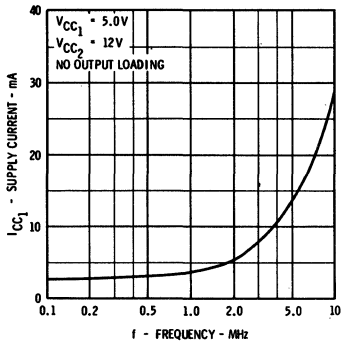
SWITCHING TIME VERSUS TEMPERATURE



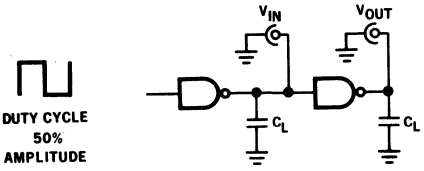
SWITCHING TIME VERSUS TEMPERATURE



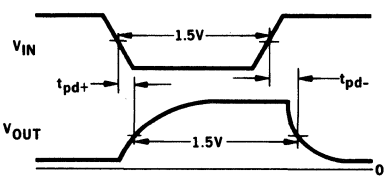
TYPICAL SUPPLY CURRENT VERSUS FREQUENCY



SWITCHING TIME TEST CIRCUIT



WAVEFORMS



DESCRIPTION OF REFLECTION DIAGRAM USAGE

The reflections on any line may be found by using the following procedure:

1. Draw the driver output characteristics for both the "high state" and the "low state" on an I - V graph in the same manner as the reflection diagram.
2. Draw the receiver input characteristic on the same graph. The two points of intersection of the receiver and driver characteristics are the two DC operating points.
3. Choose to analyze either the reflections for the output going low or high. In the example chosen the negative transition is analyzed.
4. Draw a line with a slope equal to the impedance of the line to be used, ($Z_0 = 100\Omega$ in the example), from the "high state" operating point (labeled A on our graph) to the "low state" output device characteristic (B_1). B_1 equals the conditions at the driver output immediately after turn-on.
5. Reverse the slope of Z_0 and sketch it from B_1 to the receiver input characteristic (C_1). C_1 equals the conditions at the receiver when the wavefront B_1 first reaches it.
6. By continuing this procedure of reversing the slope of Z_0 at each node all the reflections (B_1, C_1, B_2, C_2, B_3, C_3 - - - B_N, C_N), where B_X is the voltage at the driver and C_X is the voltage at the receiver, can be found.

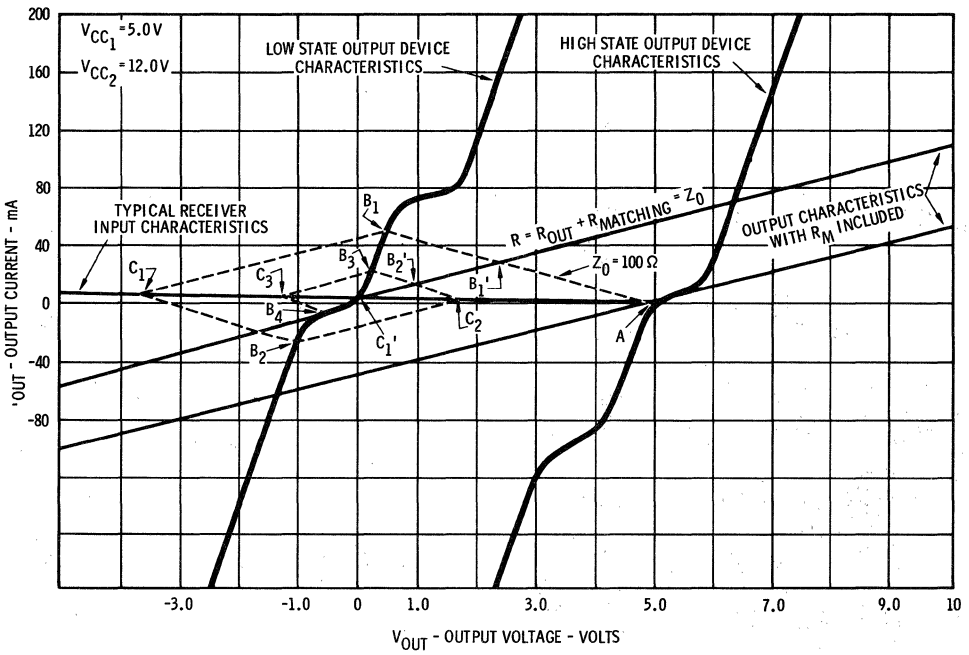
The same procedure is used to check the reflections when switching the output high.

BACK-MATCHING, also referred to as reverse termination, offers several advantages to the user. It reduces the system power by not requiring the high current for resistive termination and it reduces the DC line losses because IR drops in the line become minimum.
To back-match any line (output switching low):

1. Measure the output resistance, R_{out}, from the "low state" operating point to B_1.
2. Subtract R_{out} from Z. ($R_{out} + R_M = Z_0$). This value R_M, is the required back-matching resistance.
3. Place R_M in series with the output of driver.
4. The reflections that occur on the line with R_M inserted can be treated in the same manner as the general case. The results are B_1' and C_1' and the receiver will not see any reflections.

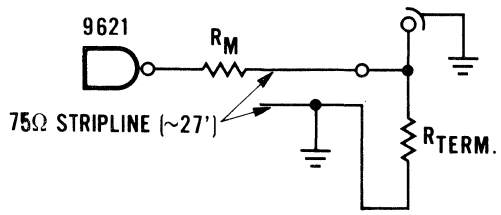
When switching the line differentially $R_M + R_{out} = Z_0/_2$. The matched output characteristics of the 9621 make it possible to back-match effectively and require analysis of switching only one state.

TYPICAL REFLECTION DIAGRAM*



* GRAPHICAL ANALYSIS
First Presented by John B. James of I.C.T. (Eng.) LTD.

REFLECTION TEST CIRCUIT

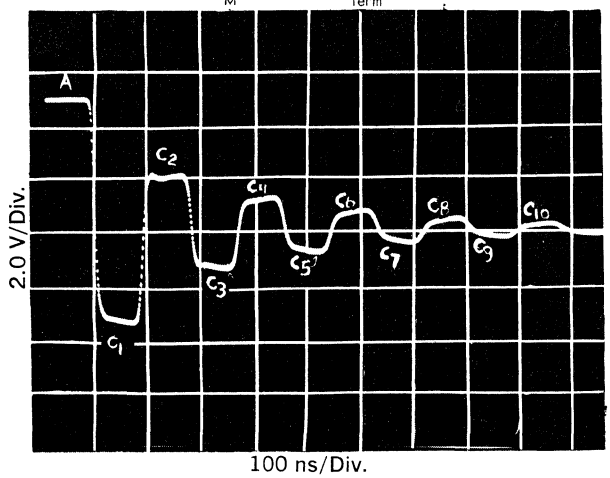


The reflections are two delay's of the line wide. R_{term} is the total impedance seen at the receiving end.

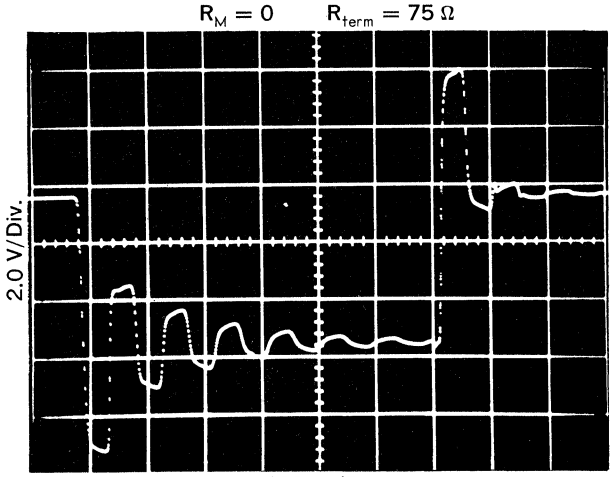
BACK MATCHING TABLE

Z_O	R_M when used single ended	R_M when used differentially
50 Ω	32 Ω	16 Ω
75 Ω	62 Ω	30 Ω
92 Ω	82 Ω	41 Ω
100 Ω	90 Ω	45 Ω
130 Ω	120 Ω	60 Ω
300 Ω	290 Ω	145 Ω
600 Ω	590 Ω	295 Ω

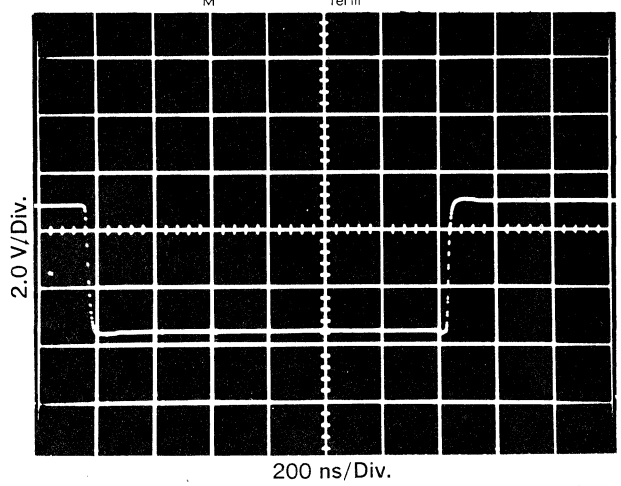
$R_M = 0$ $R_{term} = \infty$



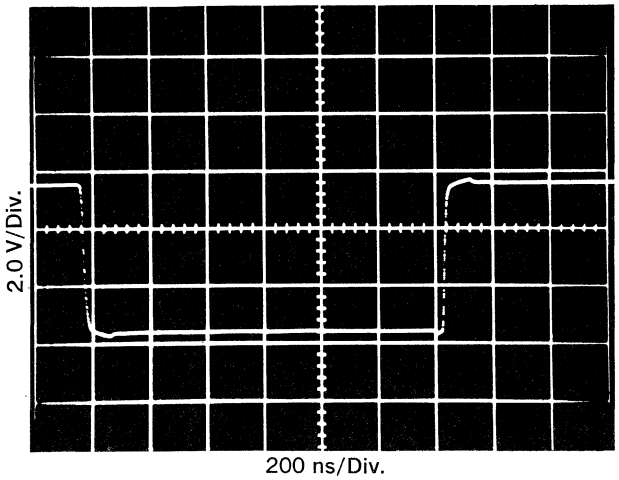
$R_M = 0$ $R_{term} = 75\ \Omega$



$R_M = 0$ $R_{term} = 75\Omega$



$R_M = 62\ \Omega$ $R_{term} = \infty$



9624 • 9625

DUAL CCSL, MOS INTERFACE ELEMENTS

FAIRCHILD INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 9624 is a dual two-input CCSL compatible interface gate specifically designed to drive MOS. The output swing is adjustable and will allow it to be used as a data driver, clock driver or discrete MOS driver. It has an active output for driving medium capacitive loads.

The 9625 is a dual MOS to CCSL level converter. It is designed to convert standard negative MOS logic levels to CCSL levels. The 9625 features a high input impedance which allows preservation of the driving MOS logic level.

Both the 9624 and 9625 are available in the 14-pin ceramic Dual In-Line package and the ¼ x ¼ Flat Pak.

FEATURES

- **CCSL COMPATIBLE INPUTS/OUTPUT**
- **MOS COMPATIBLE OUTPUT/INPUTS**
- **LOW POWER**

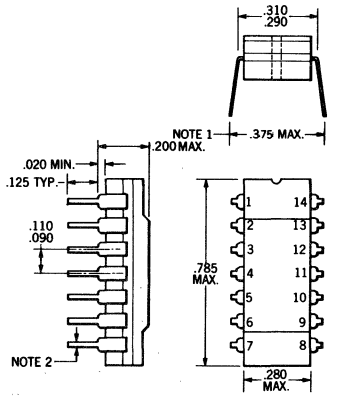
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	V_{DD} to +10 V
Voltage Applied to Outputs for high output state (9624)	V_{DD} to $+V_{CC}$ value
Voltage Applied to Outputs for high output state (9625)	−0.5 V to V_{CC} value
Input Voltage (D.C.) (9624)	−0.5 V to +5.5 V
Input Voltage (D.C.) (9625)	V_{CC} to V_{DD}
V_{DD} Pin Potential to Ground Pin	−30 V to +0.5 V
V_{DD} Pin Potential to Tap Pin (9624)	−30 V to +0.5 V

ORDER INFORMATION

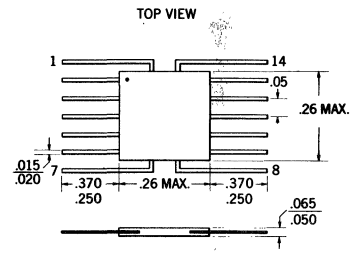
Specify U6A9624XXX and U6A9625XXX for 14-pin TO-116 Dual In-Line package or U3I9624XXX and U3I9625XXX for 14-pin Flat Package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to +75°C temperature range.

TYPICAL DUAL IN-LINE PACKAGE
In Accordance With
JEDEC (TO-116) Outline

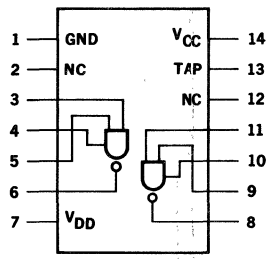


NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.375) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

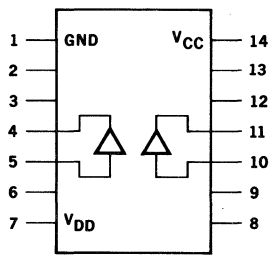
14-PIN FLAT PACKAGE



9624



9625



313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

TABLE I —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS
		−55°C		+25°C			+125°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.		
V_{OH1}	Output High Voltage	−1.0		−1.0	−0.5		−1.0	Volts	$V_{CC} = 4.5\ V$, $V_{DD} = -28\ V$, $V_{TAP} = 0\ V$ $I_{OH} = -10\ \mu A$
V_{OH2}	Output High Voltage	+3.5		+3.5	+4.0		+3.5		$V_{CC} = 5.5\ V$, $V_{DD} = -20\ V$, $V_{TAP} = 5.5\ V$ Inputs at threshold voltages (V_{IL}) $I_{OH} = -10\ \mu A$
V_{OL}	Output Low Voltage			See Note 1				Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 10\ mA$, $V_{DD} = -11$ to $-28\ V$ @ V_{IH}, $0 \leq V_{TAP} \leq V_{CC}$
V_{IH}	Input High Voltage	2.1		1.9			1.7	Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.4			1.1	0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.40			−1.25	−1.13	mA	$V_{CC} = 5.5\ V$, $V_F = 0.4\ V$ $V_{DD} = -11$ to $-28\ V$
I_R	Input Leakage Current		2.0			2.0	5.0	μA	$V_{CC} = 5.5\ V$, $V_R = 4.0\ V$ $V_{DD} = -11$ to $-28\ V$
I_{CEX}	Output Leakage Current					50		μA	$V_{CC} = 5.5\ V$, $V_{TAP} = 0\ V$ $V_{DD} = -28\ V$, $V_{OUT} = 0\ V$
I_{SC}	Output Short Circuit Current	−12	−31	−14		−32	−11 −28	mA	$V_{CC} = 4.5\ V$, $V_{TAP} = 0\ V$, $V_{IN} = 0\ V$ $V_{DD} = -11\ V$, $V_{OUT} = -11\ V$
I_{VCC}	V_{CC} Supply Current					6.1		mA	$V_{CC} = 5.5V$, $V_{DD} = -15\ V$, $V_{TAP} = 0\ V$ Inputs Open
I_{MAX}	Max. Current					10		mA	$V_{CC} = 10\ V$, $V_{DD} = -30\ V$, Inputs Open $V_{TAP} = 0\ V$
t_{pd+}	Switching Speed				190	250		ns	$V_{CC} = 5.0\ V$, See Figure 2
t_{pd-}	Switching Speed				50	100		ns	$V_{DD} = -13\ V$, $V_{TAP} = 0\ V$

Note 1: Max = V_{DD} +1.0 V over Temperature Range
Typ = V_{DD} +0.2 V over Temperature Range

SCHEMATIC DIAGRAM

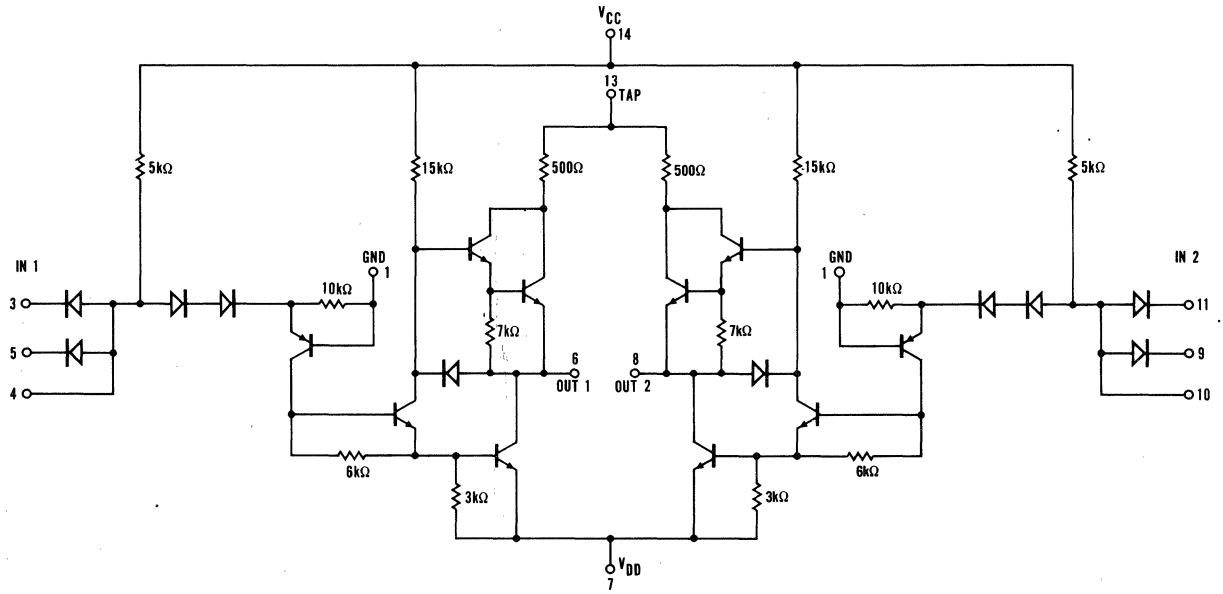


Fig. 1

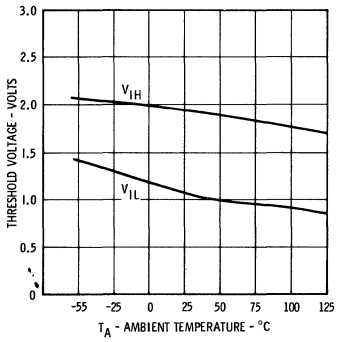
TABLE II —
ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH1}	Output High Voltage	−1.0		−1.0	−0.5		−1.0		Volts	$V_{CC} = 4.75\ V$, $V_{DD} = -28\ V$, $V_{TAP} = 0\ V$ $I_{OH} = -10\ \mu A$
V_{OH2}	Output High Voltage	+3.25		+3.25	+3.75		+3.25		Volts	$V_{CC} = 5.25\ V$, $V_{DD} = -20\ V$, $V_{TAP} = 5.25\ V$ $I_{OH} = -10\ \mu A$ Inputs at threshold voltages (V_{IL} or V_{IH})
V_{OL}	Output Low Voltage				See Note 1				Volts	$V_{CC} = 4.5\ V$, $I_{OL} = 10\ mA$, $V_{DD} = -11$ to $-28\ V$ @ $0 \leq V_{TAP} \leq V_{CC}$
V_{IH}	Input High Voltage	2.0		1.9			1.8		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		1.2			1.1		0.95	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		−1.32			−1.25		−1.20	mA	$V_{CC} = 5.25\ V$, $V_F = 0.45\ V$
I_R	Input Leakage Current		5.0			5.0		10	μA	$V_{CC} = 5.25\ V$, $V_R = 4.5\ V$
I_{CEX}	Output Leakage Current					100			μA	$V_{CC} = 5.25\ V$, $V_{TAP} = 0\ V$ $V_{DD} = -28\ V$, $V_{OUT} = 0\ V$
I_{SC}	Output Short Circuit Current	−12	−31	−14		−32	−12	−31	mA	$V_{CC} = 4.75\ V$, $V_{TAP} = 0\ V$, $V_{IN} = 0\ V$ $V_{DD} = -11\ V$, $V_{OUT} = -11\ V$
I_{VCC}	V_{CC} Supply Current					6.1			mA	$V_{CC} = 5.25\ V$, $V_{DD} = -15\ V$, $V_{TAP} = 0\ V$ Input Open
I_{MAX}	Max. Current					10			mA	$V_{CC} = 10\ V$, $V_{DD} = -30\ V$, $V_{TAP} = 0\ V$ Input Open
t_{pd+}	Switching Speed				190	250			ns	$V_{CC} = 5.0\ V$, See Figure 2
t_{pd-}	Switching Speed				50	100			ns	$V_{DD} = -13\ V$, $V_{TAP} = 0\ V$

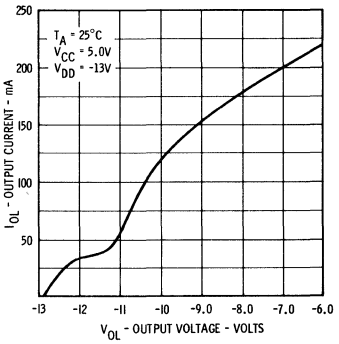
Note 1: Max = V_{DD} +1.0 V over Temperature Range
Typ = V_{DD} +0.2 V over Temperature Range

ELECTRICAL CHARACTERISTICS • 9624

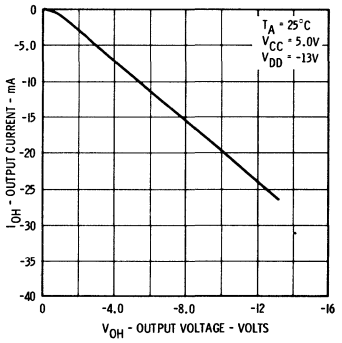
THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



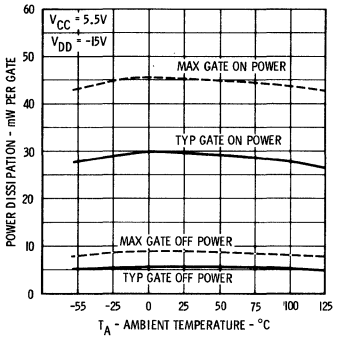
TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)



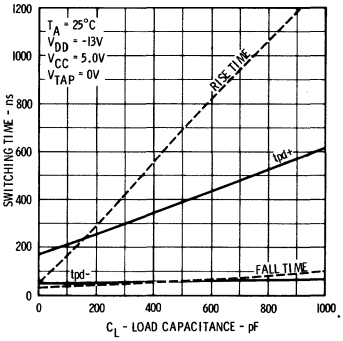
TYPICAL OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (HIGH STATE)



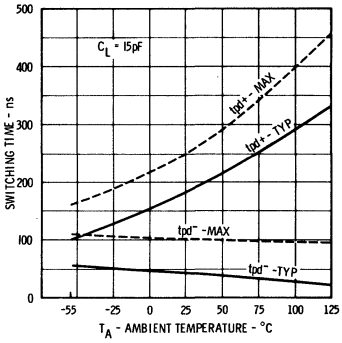
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE



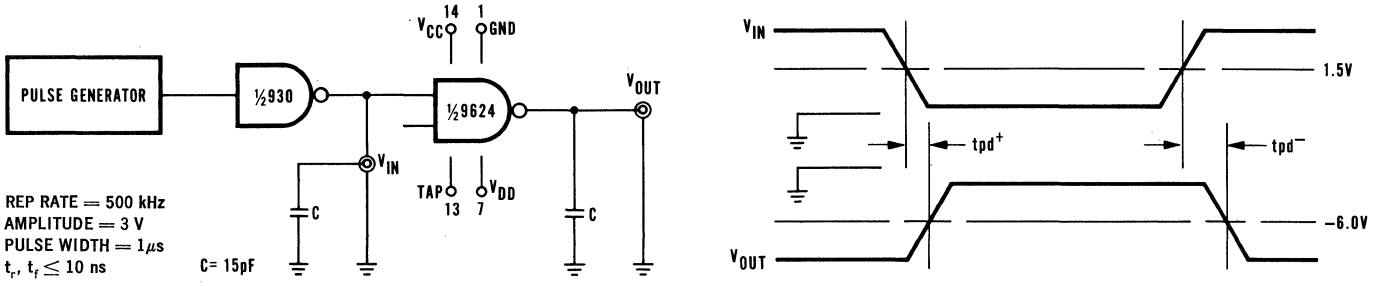
TYPICAL SWITCHING TIME VERSUS LOAD CAPACITANCE



SWITCHING TIME VERSUS AMBIENT TEMPERATURE



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS
9624



TESTS	CONDITIONS			
	T_A (°C)	V_{CC} (Volts)	V_{DD} (Volts)	Tap Voltage
t_{pd}^+, t_{pd}^-	25	5.0	−13	0

Fig. 2

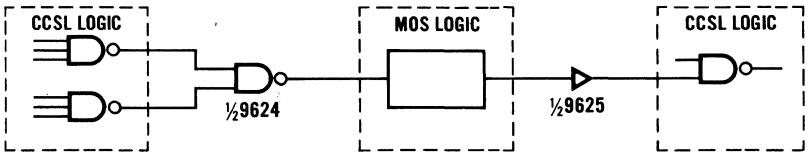
LOADING RULES:

*The extender pin allows the number of inputs to be extended by adding diodes or the DTμL 933 extender.

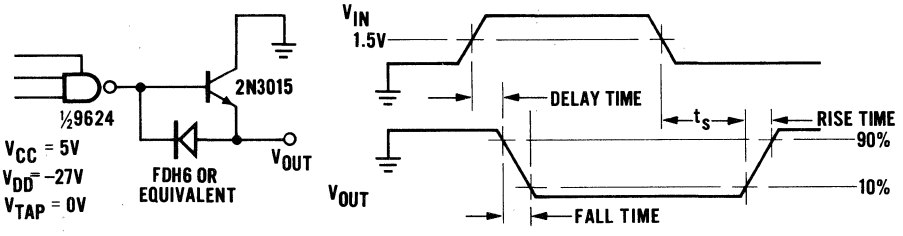
Note 1: Fan out into MOS is limited only by MOS leakage currents.

Note 2: $I_{IN} = +210\ \mu A$

APPLICATION:



CLOCK DRIVING (using a high capacitance drive scheme)



TYPICAL SWITCHING TIMES VERSUS LOAD CAPACITANCE

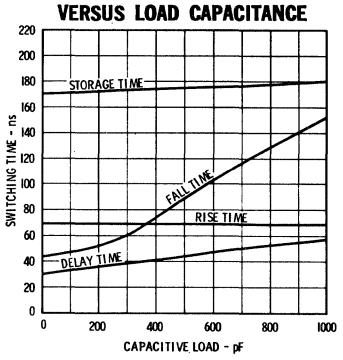


TABLE III —
ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS						UNITS	CONDITIONS
		−55°C		+25°C			+125°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.		
V_{OH}	Output High Voltage	2.5		2.6			2.5	Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -60\ \mu A$ $V_{DD} = -11\ V$ Inputs at threshold voltages (V_{IH})
V_{OL}	Output Low Voltage		0.5			0.5	0.5	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 1.5\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 1.2\ mA$ $V_{DD} = -11\ V$ Inputs at threshold voltages (V_{IL})
V_{IH}	Input High Voltage	−3.0				−3.0	−3.0	Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage	−9.0		−9.0			−9.0	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current		210			210	210	μA	$V_{CC} = 5.0\ V$, $V_F = -3.0\ V$, $V_{DD} = -13\ V$
I_{CEX}	Output Leakage Current					50		μA	$V_{CC} = V_{CEX} = 4.5\ V$, $V_{DD} = -13\ V$
I_{VCCL}	Supply Current					4.8		mA	$V_{CC} = 5.5\ V$, $V_{DD} = -15\ V$, $V_{IN} = -10\ V$
I_{VCCH}	Supply Current					2.1			$V_{CC} = 5.5\ V$, $V_{DD} = -15\ V$, $V_{IN} = 0\ V$
I_{VDD}	V_{DD} Supply Current					−9.0		mA	$V_{CC} = 5.5\ V$, $V_{DD} = -15\ V$ Input open or gnd
I_{MAX}	Max. V_{DD} Supply Current					−25		mA	$V_{CC} = 8.0\ V$, $V_{DD} = -20\ V$, $V_{IN} = 0\ V$
t_{pd+}	Switching Speed				55	100		ns	$V_{CC} = 5.0\ V$, $V_{DD} = -13\ V$
t_{pd-}	Switching Speed				90	150		ns	See Figure 4

SCHEMATIC DIAGRAM

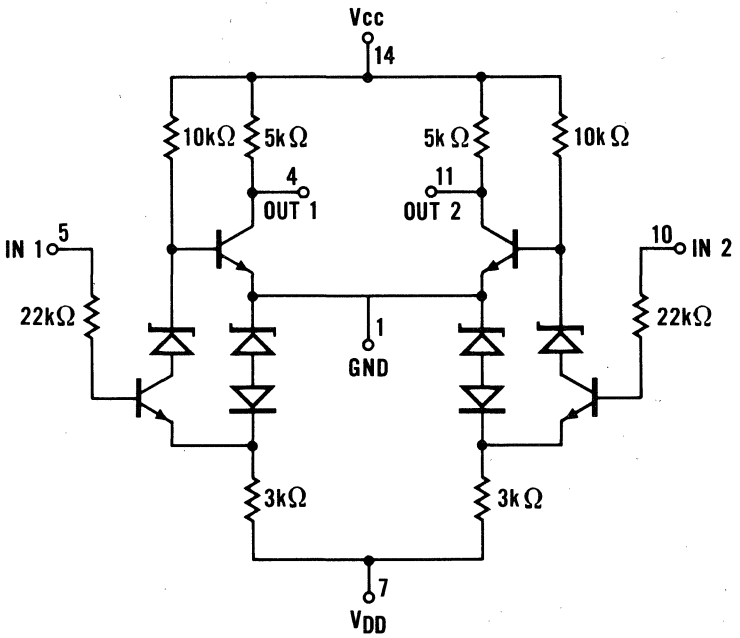
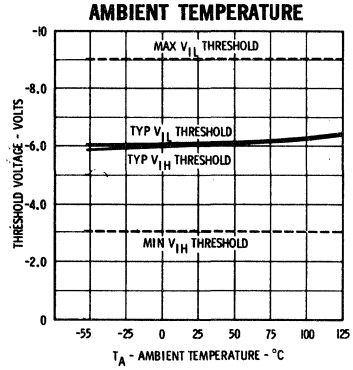


Fig. 3

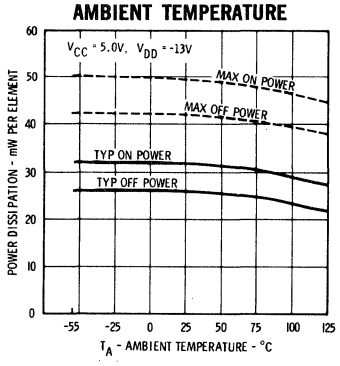
TABLE IV —
ELECTRICAL CHARACTERISTICS (T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.5		2.6			2.5		Volts	V_{CC} = 4.75 V, I_{OH} = −60 μA V_{DD} = −11 V Inputs at threshold voltages (V_{IH})
V_{OL}	Output Low Voltage		0.5			0.5		0.5	Volts	V_{CC} = 5.25 V, I_{OL} = 1.52 mA V_{CC} = 4.75 V, I_{OL} = 1.33 mA Inputs at threshold voltages (V_{IL})
V_{IH}	Input High Voltage	−3.0				−3.0		−3.0	Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage	−9.0		−9.0			−9.0		Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current	210				210	210		μA	V_{CC} = 5.0 V, V_F = −3.0 V, V_{DD} = −13 V
I_{CEX}	Output Leakage Current					100			μA	V_{CC} = V_{CEX} = 4.75 V, V_{DD} = −13 V
I_{VCCL}	Supply Current					4.8			mA	V_{CC} = 5.25 V, V_{DD} = −15 V, V_{IN} = −10 V
I_{VCCH}	Supply Current					2.1			mA	V_{CC} = 5.25 V, V_{DD} = −15 V, V_{IN} = 0 V
I_{VDD}	V_{DD} Supply Current					−9.0			mA	V_{CC} = 5.5 V, V_{DD} = −15 V Input open or gnd
I_{MAX}	Max. V_{DD} Supply Current					−25			mA	V_{CC} = 8.0 V, V_{DD} = −20 V, V_{IN} = 0 V
t_{pd+}	Switching Speed				55	100			ns	V_{CC} = 5.0 V, V_{DD} = −13 V
t_{pd-}	Switching Speed				90	150			ns	See Figure 4

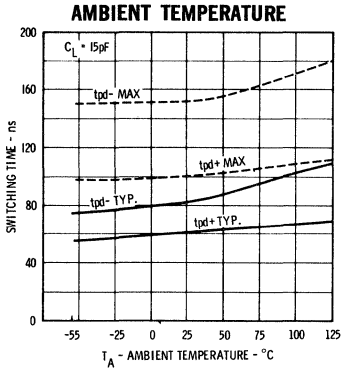
THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE



POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

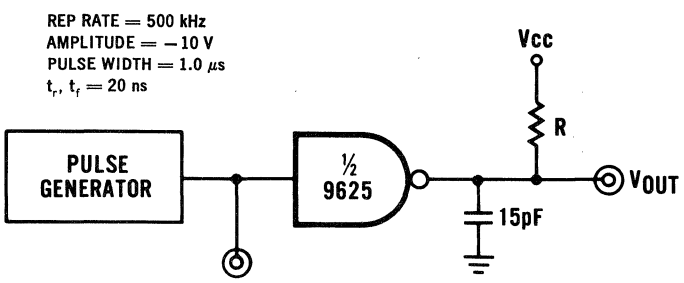


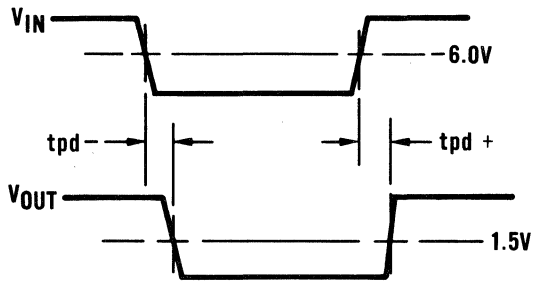
SWITCHING TIME VERSUS AMBIENT TEMPERATURE



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

REP RATE = 500 kHz
AMPLITUDE = −10 V
PULSE WIDTH = 1.0 μs
t_r, t_f = 20 ns





TESTS	CONDITIONS T_A (°C)	V_{CC} (Volts)	V_{DD} (Volts)	R (kΩ)
t_{pd}^+, t_{pd}^-	25	5.0	−13	3.75

Fig. 4

RTμL COMPOSITE DATA SHEET

INDUSTRIAL MICROLOGIC® INTEGRATED CIRCUITS

OPERATING TEMPERATURE RANGE: 0°C to +70°C (METAL PACKAGE)
15°C to 55°C (EPOXY)

GENERAL DESCRIPTION — The Fairchild Industrial Resistor-Transistor Micrologic® (RTμL) integrated circuit family consists of a number of medium and low power compatible integrated circuits made up by resistor-transistor logic and capable of performing logic functions for use in digital electronic equipment.

The elements of this family are manufactured using the familiar Fairchild Planar* epitaxial process by which all the individual transistors and resistors are diffused into a single silicon wafer, thus assuring a high degree of reliability.

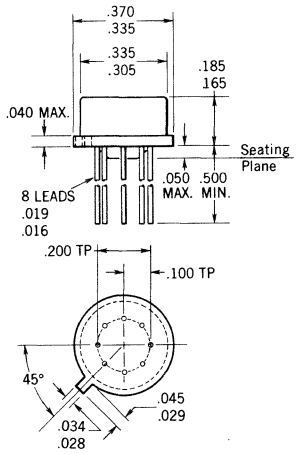
*Planar is a patented Fairchild process.

Some of the important features of the RTμL integrated circuit family are the following:

- Guaranteed operation over the specified temperature range.
- System operates with one power supply (3.6 V±10%).
- Trade-off between fan-out and temperature (permitted).
- RTL uses positive NOR or negative NAND logic.
- High noise immunity — 300 mV.
- Very low propagation delays — typical 12 nanoseconds for medium power gate and 40 nanoseconds for low power gate.
- Power dissipation of typically 2mW per gate for the low power elements.
- Low cost.
- Medium power buffer 9900, dual two-input gate 9914 and JK flip-flop9923 available in epoxy for additional cost advantages.
- Mixing medium and low power elements optimizes fan-out and power dissipation.
- Application briefs, notes and thorough individual data sheets available.

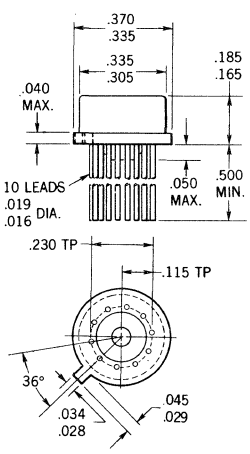
PHYSICAL DIMENSIONS (TO-5 TYPES)

TO-99
(8 pin package)



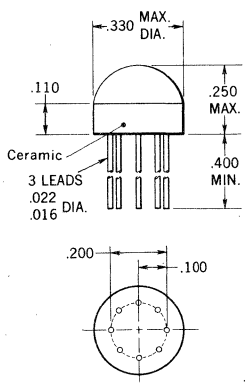
NOTES: All dimensions in inches
Dimensions as per latest J-10 committee
Leads are gold-plated kovar
Weight is 1 12 grams

TO-100
(10 pin package)



NOTES: All dimensions in inches
Leads are gold-plated kovar
Lead No. 1 internally connected to case
Package weight is 1.32 grams

EPOXY PACKAGE
(similar to TO-5)



NOTES: All dimensions in inches
Leads are gold-plated nickel

PURCHASING INFORMATION

Purchasing Agent please note:

To order part, the following numbering system should be used to expedite handling. The complete number will be a nine-digit number with the designations as follows:

A B C D E F G H I

A = U for all elements
BC = 5B for 8-pin (TO-99) pkg.
= 5F for 10-pin (TO-100) pkg.
= 8A for 8-pin epoxy

DEFG = The four-digit number denoting the specific element desired
H = 2 for all elements
I = 9 for 0°C to 70°C for metal packages
= 8 for 15°C to 55°C epoxy pkg.

Note: All elements are available in a metal TO-5 type package, but not necessarily in epoxy. Consult your sales representative for details.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

LOADING RULES

Industrial Resistor-Transistor Micrologic® (RTμL) integrated circuits consist of low and medium power devices. The primary difference between a low and a medium power element lies in the values of the base and collector resistors associated with each element. The medium power elements have base and collector resistors of 450 Ω and 640 Ω typical, whereas the low power elements have typical base and collector resistors of 1.5 kΩ and 3.6 kΩ respectively.

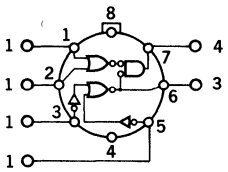
As a result of these differences in resistance values, the input load and output drive factors (maximum input current and minimum output available current) are higher for the medium, and lower for the low power elements.

For purposes of simplification, all input load and output drive factors have been normalized using as a basis the current required to turn on a low-power gate transistor. As a result of this normalization, the input load factor of the 9914 element is 3 and the input load factor of the 9910 element is 1, thus, the 9914 requires three times as much input current. For the output drive factors, the 9910 has an output drive factor four times less than that of the 9914.

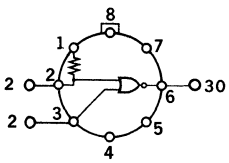
The number of elements (bases) that may be driven by an output terminal may consist of any combination of low and medium power elements as long as the sum of all the input load factors does not exceed the output drive factor of the driving element.

LOADING CHART

LOW POWER ELEMENTS:



9908



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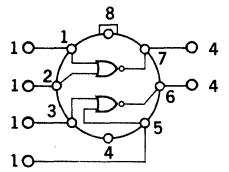

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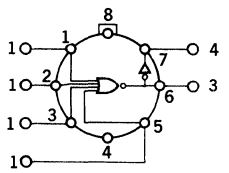

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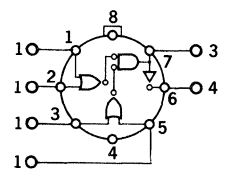

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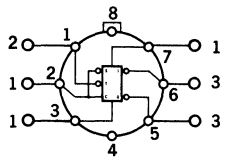

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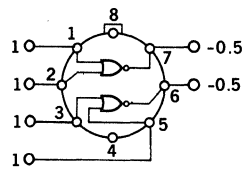

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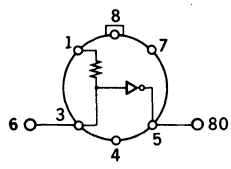
MEDIUM POWER ELEMENTS:



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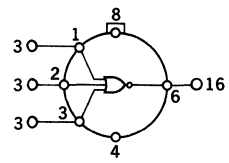

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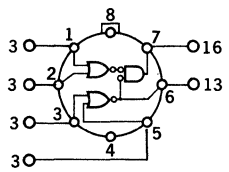

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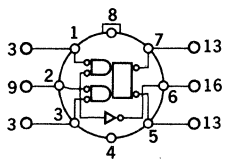

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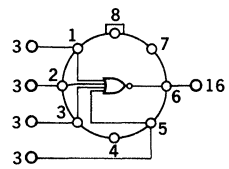

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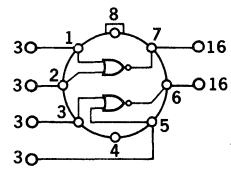

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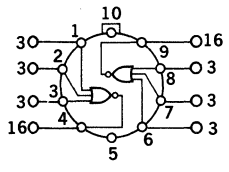

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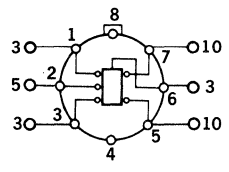

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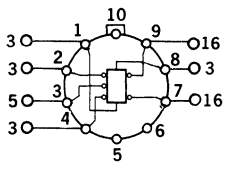

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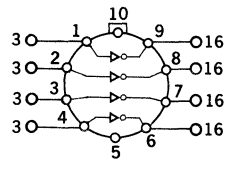


9927

PARALLELING AND OTHER RULES:

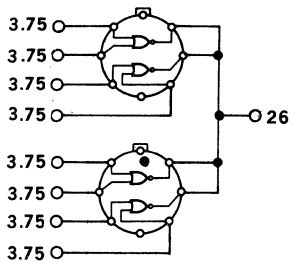
1. All unused input pins should be grounded.

2. On all 8-pin lead devices, V_{CC} is connected to pin 8 and pin 4 is grounded. On 10-pin lead devices, pins 10 and 5 are V_{CC} and Ground pins respectively.

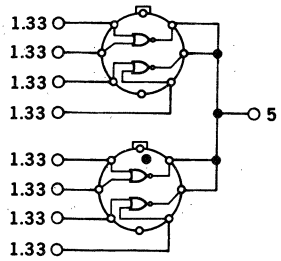
3. For each medium power gate output terminal tied to another medium power gate output terminal (and V_{CC} open on all gates but one) the output drive factor should be reduced by 2 loads.

4. For each low-power gate output terminal tied to another low power gate output terminal (and V_{CC} open on all gates but one) the output drive factor should be reduced by one load.

5. By increasing the input load requirement by 0.75 load for medium power and 0.33 for low power to cover any reduction in base-emitter impedance, any number of gates may be placed in parallel as shown below:



PARALLELING MEDIUM POWER ELEMENTS

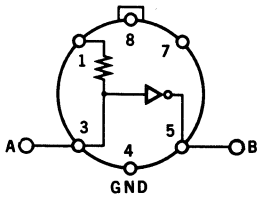


PARALLELING LOW POWER ELEMENTS

● = NO V_{CC} CONNECTED

9900 MEDIUM POWER BUFFER*

The Buffer element is a low-impedance inverting driver circuit. Because of its very low source impedance the element can supply substantially more output current than the basic circuit. As a consequence, the Buffer element is valuable in driving heavily loaded circuits or minimizing rise-time deterioration due to capacitive loading. A resistor is internally connected to the Buffer element input which may be returned to the supply voltage if capacitive coupling is desired. Typical applications of this type connection are astable and monostable multivibrators, and for the differentiation of pulses.

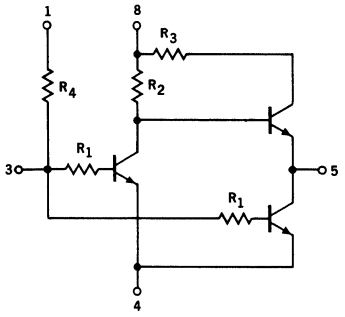


FUNCTIONS

POSITIVE LOGIC:
$B = \overline{A}$

NEGATIVE LOGIC:
$B = \overline{A}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

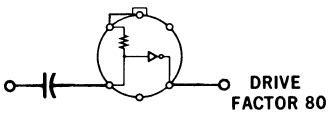
$R_1 = 450\Omega$
$R_2 = 1000\Omega$
$R_3 = 100\Omega$
$R_4 = 1000\Omega$

LOADING RULES

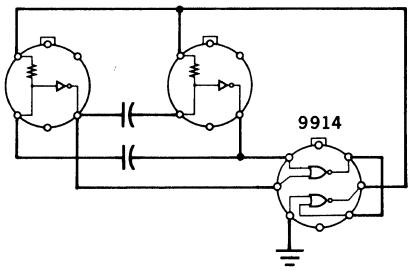
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
3	6	5	80

Note: For more information on loading rules and for parallel combination of elements, see page 2.

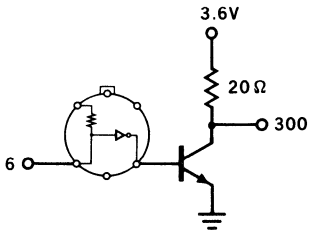
TYPICAL APPLICATIONS



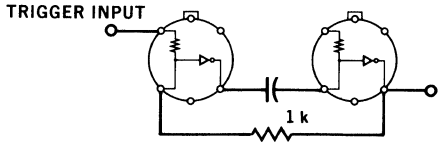
ONE SHOT MULTIVIBRATOR



ASTABLE MULTIVIBRATOR



HIGH FAN-OUT EXTENSION



MONOSTABLE CIRCUIT

* This element also available in the epoxy package.

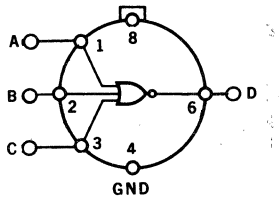
9903 MEDIUM POWER THREE INPUT GATE

The Gate element is a three-input resistor-transistor-logic circuit, one of four similar-basic NAND/NOR gates produced by Fairchild. The versatility of the NAND/NOR function permits the generation of any logic function through the exclusive use of gate elements. Individual gate elements may be paralleled to increase the number of inputs to a single output node (subject to loading rules), or combined with other Micrologic® integrated circuits to augment their logic functions.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE



FUNCTIONS

POSITIVE LOGIC: $D = \overline{A + B + C}$

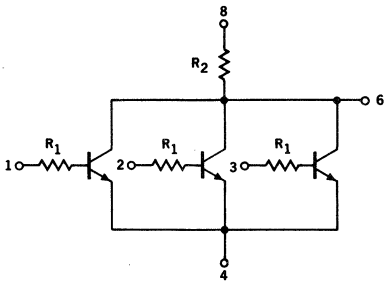
$= \overline{A}\,\overline{B}\,\overline{C}$

NEGATIVE LOGIC: $D = \overline{A\,B\,C}$

$= \overline{A} + \overline{B} + \overline{C}$

Note: Pins 5 and 7 omitted.

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 450\Omega$
$R_2 = 650\Omega$

TRUTH TABLE

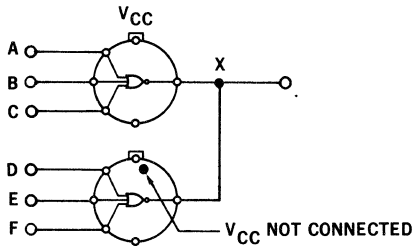
A	B	C	D
H	H	H	L
H	H	L	L
H	L	H	L
H	L	L	L
L	H	H	L
L	H	L	L
L	L	H	L
L	L	L	H

LOADING RULES

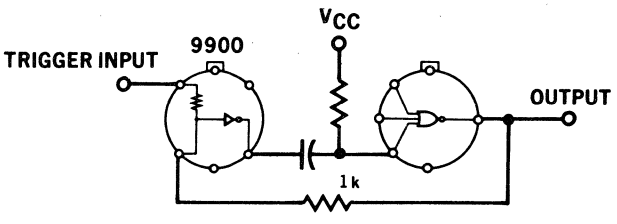
INPUT PIN	LOAD FACTORS	OUTPUT PIN	DRIVE FACTORS
1	3	6	16
2	3		
3	3		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



SIX INPUT GATE



MONOSTABLE CIRCUIT

POSITIVE LOGIC:
$\overline{A + B + C + D + E + F} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E} \cdot \overline{F}$

NEGATIVE LOGIC:
$\overline{A \cdot B \cdot C \cdot D \cdot E \cdot F} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F}$

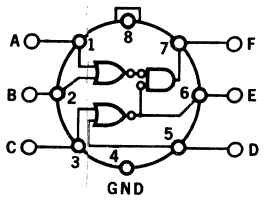
9904 MEDIUM POWER HALF ADDER

The Half-Adder element is a multipurpose combination of three basic circuits. The configuration is well-suited as a complete half-adder, an exclusive OR gate, or any other similar logic construction. Output No. 7 is a noninverting function of the four inputs, whereas output No. 6 may be considered as either a NAND or a NOR gate.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE



FUNCTIONS

POSITIVE LOGIC: $E = \overline{C + D}$
$F = (A + B)(C + D)$

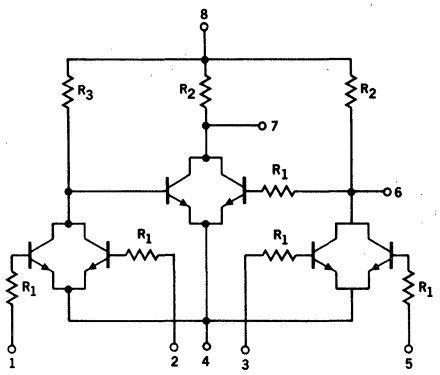
NEGATIVE LOGIC: $E = \overline{C}\,\overline{D}$
$F = AB + CD$

IF $C = \overline{A}$ and $D = \overline{B}$

POSITIVE LOGIC: $E = AB$
$F = A\overline{B} + \overline{A}B$

NEGATIVE LOGIC: $E = A + B$
$F = AB + \overline{C}\,\overline{D}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 450\Omega$
$R_2 = 640\Omega$
$R_3 = 800\Omega$

TRUTH TABLE

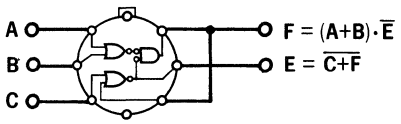
INPUTS				OUTPUTS	
1	2	3	5	7	6
H	H	H	H	H	L
L	H	H	H	H	L
H	L	H	H	H	L
H	H	L	H	H	L
H	H	H	L	H	L
L	L	H	H	L	L
L	H	L	H	H	L
L	H	H	L	H	L
H	L	L	H	H	L
H	L	H	L	H	L
H	H	L	L	L	H
L	L	L	H	L	L
L	H	L	L	L	H
L	L	H	L	L	L
H	L	L	L	L	H
L	L	L	L	L	H

LOADING RULES

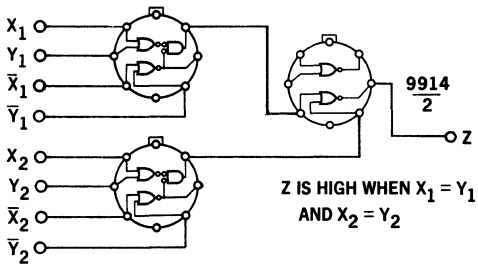
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTORS
1	3	6	16
2	3	7	13
3	3		
5	3		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



GATED FLIP - FLOP



PARALLEL COMPARISON

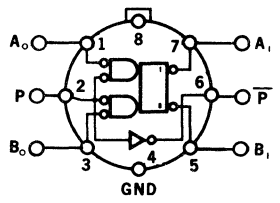
9905 MEDIUM POWER HALF SHIFT REGISTER

The Half Shift Register element is a gated input storage element composed of five basic gate circuits. Internal cross-connection of the two output gate circuits provides memory. The input gating signal is applied to the remaining three gate circuits. Two of these control the logic inputs, while the third provides the complement of the gating signal at an output pin. Because of the two cascaded internal logic levels, the unit changes state in response to near-ground input signals. Consequently, from a terminal standpoint, the unit should be regarded as requiring NAND input logic levels. Concurrent near-ground signals at all three inputs will cause near-ground signals at both outputs.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

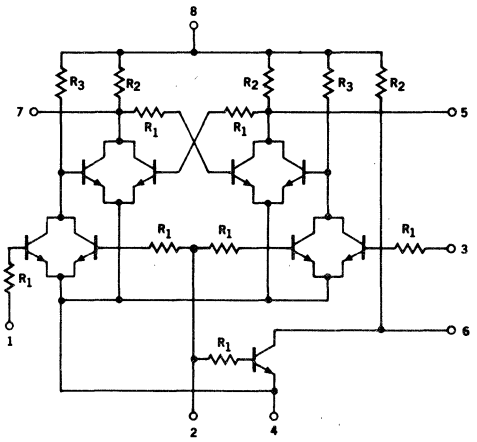


FUNCTIONS

POSITIVE LOGIC: $A_1 = \overline{B_1}\,(A_0 + P)$, $B_1 = \overline{A_1}\,(B_0 + P)$

NEGATIVE LOGIC: $A_1 = \overline{B_1} + A_0P$, $B_1 = \overline{A_1} + B_0P$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 450\Omega$
$R_2 = 640\Omega$
$R_3 = 800\Omega$

TRUTH TABLE

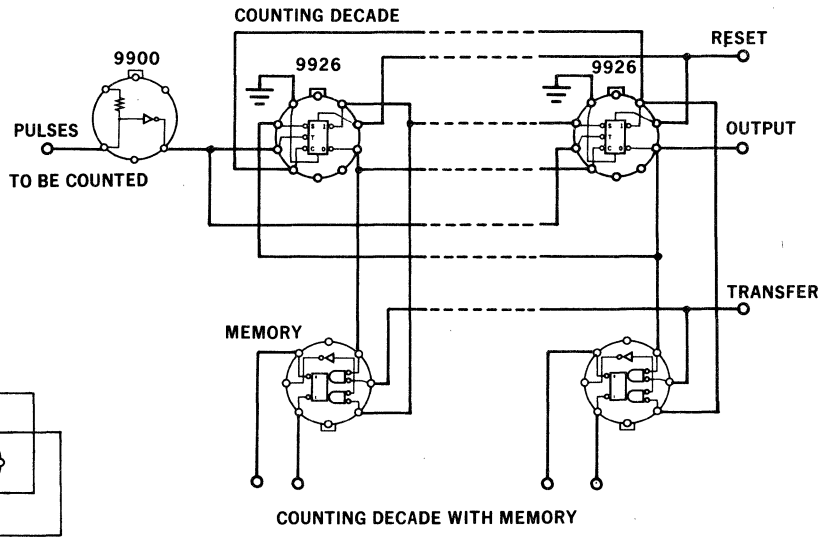
INPUT			OUTPUT	
A_0	P	B_0	A_1	B_1
H	H	H	H	L
H	H	L	H	L
H	L	H	H	L
H	L	L	H	L
L	H	H	L	H
L	H	L	L	H
L	L	H	L	H
L	L	L	L	L

LOADING RULES

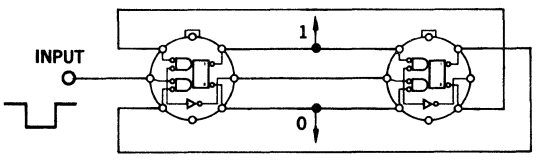
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	3	5	13
2	9	6	16
3	3	7	13

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



COUNTING DECADE WITH MEMORY



COMPLEMENTARY FLIP-FLOP

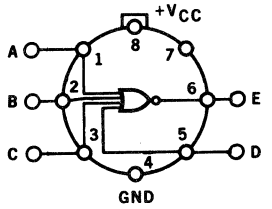
9907 MEDIUM POWER FOUR INPUT GATE

The Four-Input Gate element is a four-input resistor-transistor-logic circuit, one of four similar NAND/NOR gates produced by Fairchild. The versatility of the NAND/NOR function permits the generation of any logic-function through the exclusive use of four-input gate elements. Individual four-input gate elements may be paralleled to increase the number of inputs to a single output node (subject to loading rules), or combined with other Micrologic® integrated circuits to augment their logic functions. This element performs the AND and exclusive OR function. It is also used to select one of two data streams under control of a single gate signal.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

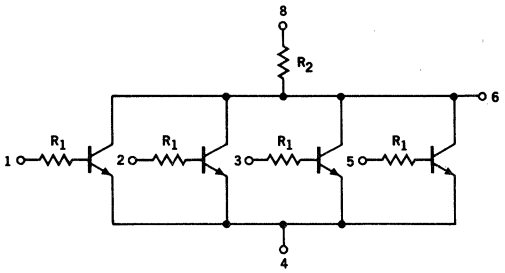


FUNCTIONS

POSITIVE LOGIC: $E = \overline{A + B + C + D}$

NEGATIVE LOGIC: $E = \overline{A\,B\,C\,D} = \overline{A} + \overline{B} + \overline{C} + \overline{D}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 450\Omega$
$R_2 = 640\Omega$

TRUTH TABLE

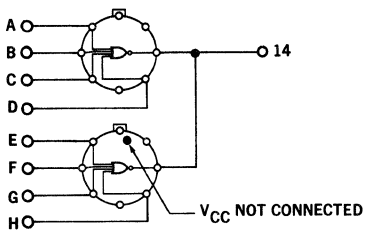
INPUTS				OUTPUT
A	B	C	D	E
H	H	H	H	L
H	H	H	L	L
H	H	L	H	L
H	H	L	L	L
H	L	H	H	L
H	L	H	L	L
H	L	L	H	L
H	L	L	L	L
L	H	H	H	L
L	H	H	L	L
L	H	L	H	L
L	H	L	L	L
L	L	H	H	L
L	L	H	L	L
L	L	L	H	L
L	L	L	L	H

LOADING RULES

INPUT PIN	LOAD FACTORS	OUTPUT PIN	DRIVE FACTORS
1	3	6	16
2	3		
3	3		
5	3		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



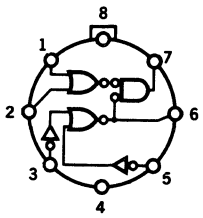
EIGHT INPUT GATE

POSITIVE LOGIC:
$\overline{A + B + C + D + E + F + G + H} = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D}\,\overline{E}\,\overline{F}\,\overline{G}\,\overline{H}$

NEGATIVE LOGIC:
$\overline{A\,B\,C\,D\,E\,F\,G\,H} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$

9908 LOW POWER ADDER

This element performs the AND and exclusive OR function. It is also used to select one of two data streams under control of a single gate signal.



H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

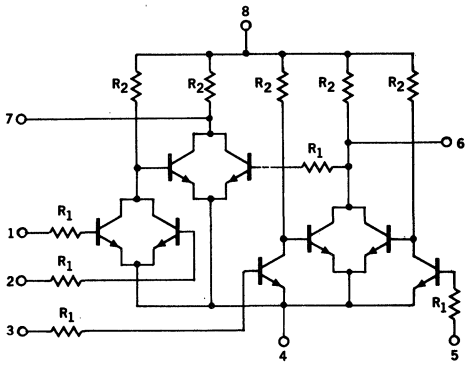
NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

FUNCTIONS

POSITIVE LOGIC:
$6 = (\overline{3} + \overline{5}) = 3 \cdot 5$
$7 = (1 + 2)(\overline{3} + \overline{5})$

NEGATIVE LOGIC:
$6 = (\overline{3} \cdot \overline{5}) = 3 + 5$
$7 = 1 \cdot 2 + \overline{3} \cdot \overline{5}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 1.5k\Omega$
$R_2 = 3.6k\Omega$

TRUTH TABLE

I, Output "6"

3	5	6
L	L	L
L	H	L
H	L	L
H	H	H

II, Output "7"

1	2	6	7
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	H
H	H	H	L

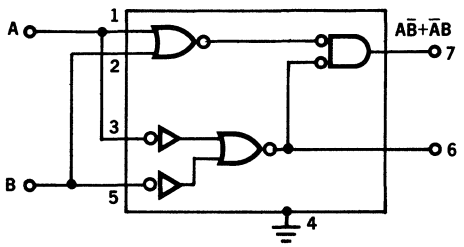
LOADING RULES

INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	1	6	3
2	1	7	4
3	1		
5	1		

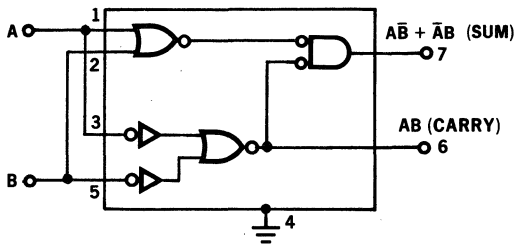
* For loading rule explanations see page 10.

Note: For more information on loading rules and for parallel combination of elements, see page 2.

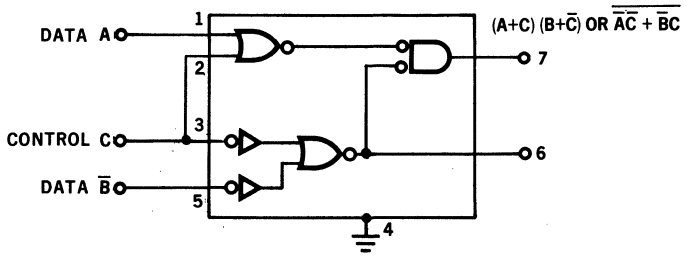
TYPICAL APPLICATIONS (POSITIVE LOGIC)



EXCLUSIVE OR GATE



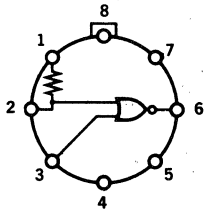
HALF ADDER



DATA STREAM SWITCH

9909 LOW POWER BUFFER

This element is a low-output impedance, two-input inverting driver. It can supply substantially more output current than the basic circuit to provide higher fan-out or drive capacitive loads. A resistor is connected internally to one of the inputs which may be returned to the supply voltage if capacitive coupling is desired.

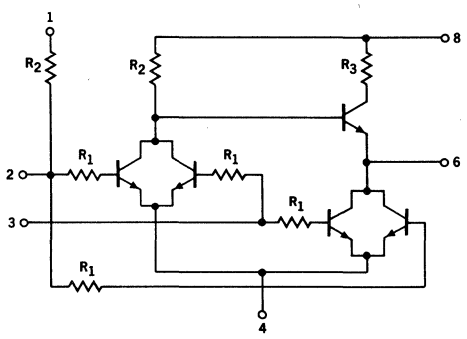


FUNCTIONS

POSITIVE LOGIC:
$6 = \overline{2 + 3}$

NEGATIVE LOGIC:
$6 = \overline{2 \cdot 3}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

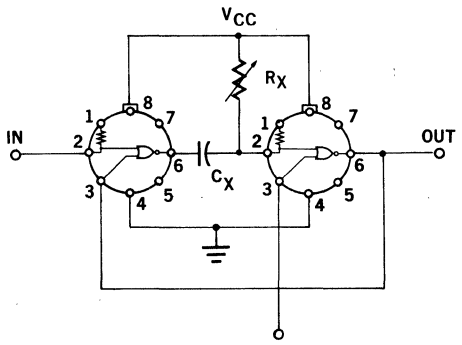
$R_1 = 1.5k\Omega$
$R_2 = 3.6k\Omega$
$R_3 = 100\Omega$

LOADING RULES

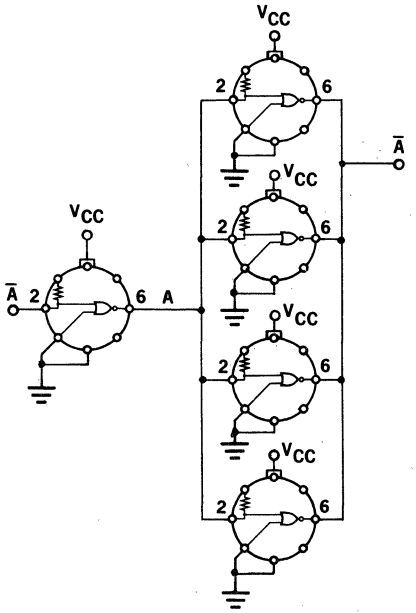
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
2	2	6	30
3	2		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

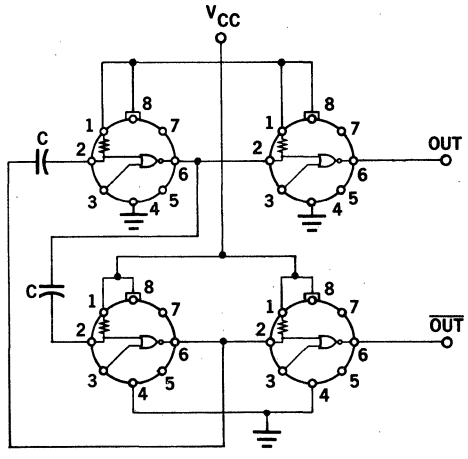
TYPICAL APPLICATIONS



ONE SHOT MULTIVIBRATOR



PARALLEL PULSE DRIVER



FOUR BUFFERS CONNECTED AS FREE RUNNING MULTIVIBRATOR

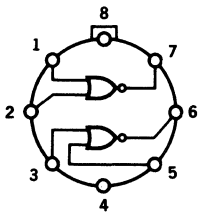
9910 LOW POWER DUAL GATE

This element can be used on a NOR gate, Double Inverter RS flip-flop or as a pair of Inverters. It can also be used with the gate expander to increase its fan-in capacity.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

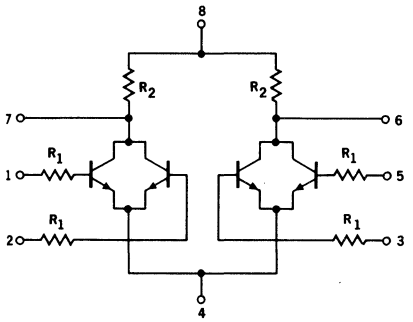


FUNCTIONS

POSITIVE LOGIC:
$7 = \overline{1 + 2}$
$6 = \overline{3 + 5}$

NEGATIVE LOGIC:
$7 = \overline{1 \cdot 2}$
$6 = \overline{3 \cdot 5}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 1.5k\Omega$
$R_2 = 3.6k\Omega$

TRUTH TABLE

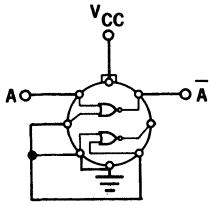
OUTPUT 7			OUTPUT 6		
1	2	7	3	5	6
L	L	H	L	L	H
L	H	L	L	H	L
H	L	L	H	L	L
H	H	L	H	H	L

LOADING RULES

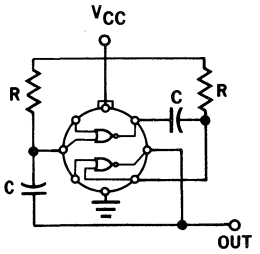
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	1	6	4
2	1	7	4
3	1		
5	1		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

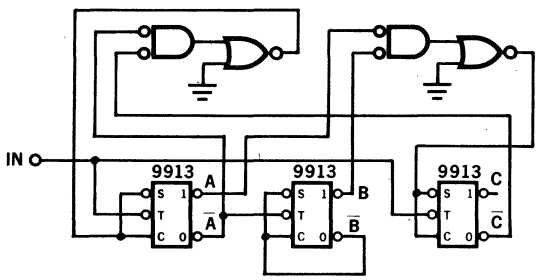
TYPICAL APPLICATIONS



SIMPLE INVERTER

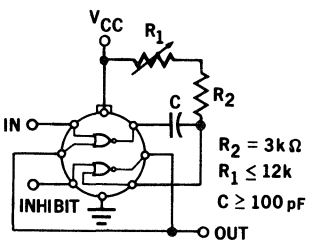


SINGLE DUAL GATE AS
FREE-RUNNING MULTIVIBRATOR



MOD - 5 BINARY COUNTER

Function: To count to a Modulo of 5 using a 1-2-4 code, or to divide an input frequency by a factor of 5.



SINGLE DUAL GATE USED AS
A ONE-SHOT MULTIVIBRATOR

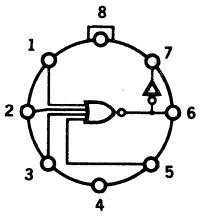
9911 LOW POWER DUAL GATE WITH INVERTER

This element is a general purpose four-input gate with inverter for NOR, OR functions and can also be used as an amplifier-inverter.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE



FUNCTIONS

POSITIVE LOGIC:

$7 = \overline{1 + 2 + 3 + 5}$

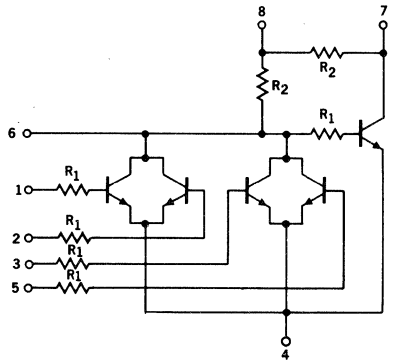
$6 = \overline{1 + 2 + 3 + 5}$

NEGATIVE LOGIC:

$7 = \overline{1 \cdot 2 \cdot 3 \cdot 5}$

$6 = \overline{1 \cdot 2 \cdot 3 \cdot 5}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 1.5k\Omega$
$R_2 = 3.6k\Omega$

TRUTH TABLE

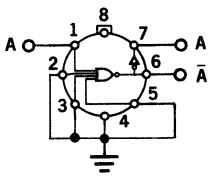
1	2	3	5	6	7
L	L	L	L	H	L
L	L	L	H	L	H
L	L	H	L	L	H
L	L	H	H	L	H
L	H	L	L	L	H
L	H	L	H	L	H
L	H	H	L	L	H
L	H	H	H	L	H
H	L	L	L	L	H
H	L	L	H	L	H
H	L	H	L	L	H
H	L	H	H	L	H
H	H	L	L	L	H
H	H	L	H	L	H
H	H	H	L	L	H
H	H	H	H	L	H

LOADING RULES

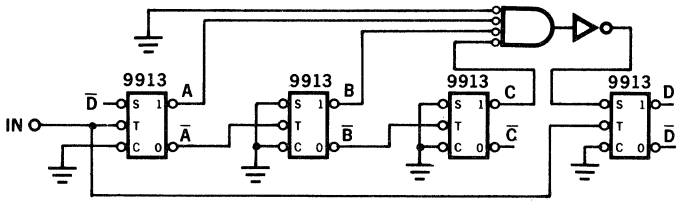
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	1	6	3
2	1	7	4
3	1		
5	1		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



CONNECTED AS INVERTER-AMPLIFIER



MODULO 9 BINARY COUNTER

Function: To count to a Modulo of 9 using 1-2-4-8 code, or to divide an input frequency by a factor of 9.

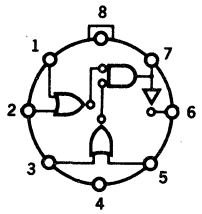
9912 LOW POWER HALF ADDER

This element is a multipurpose combination of three basic circuits that can be used as a complete half adder, an exclusive OR gate, gated-set flip-flop or any other similar logic construction.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

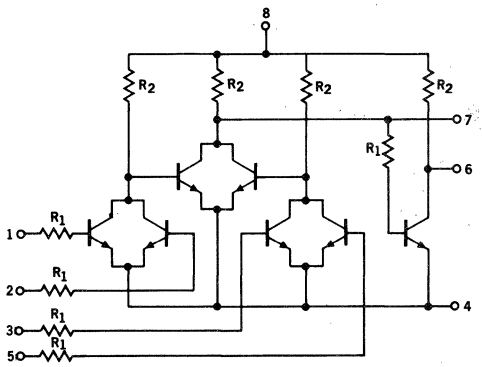


FUNCTIONS

POSITIVE LOGIC:
$7 = (1 + 2) \cdot (3 + 5)$
$6 = \overline{1} \cdot \overline{2} + \overline{3} \cdot \overline{5}$

NEGATIVE LOGIC:
$7 = 1 \cdot 2 + 3 \cdot 5$
$6 = (\overline{1} + \overline{2}) \cdot (\overline{3} + \overline{3})$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 1.5k\Omega$
$R_2 = 3.6k\Omega$

TRUTH TABLE

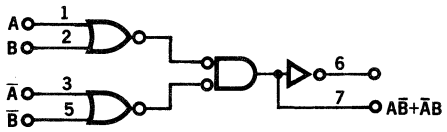
1	2	3	5	6	7
L	L	L	L	H	L
L	L	L	H	H	L
L	L	H	L	H	L
L	L	H	H	H	L
L	H	L	L	H	L
L	H	L	H	L	H
L	H	H	L	L	H
L	H	H	H	L	H
H	L	L	L	H	L
H	L	L	H	L	H
H	L	H	L	L	H
H	L	H	H	L	H
H	H	L	L	H	L
H	H	L	H	L	H
H	H	H	L	L	H
H	H	H	H	L	H

LOADING RULES

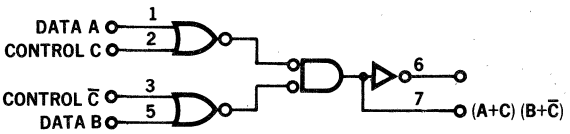
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	1	6	4
2	1	7	3
3	1		
5	1		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

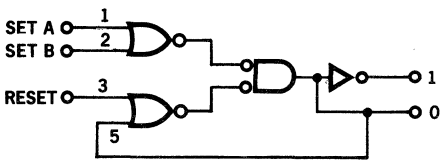
TYPICAL APPLICATIONS (POSITIVE LOGIC)



EXCLUSIVE OR GATE OR HALF ADDER



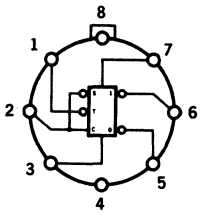
DATA STREAM SWITCH



GATED R-S FLIP-FLOP

9913 LOW POWER TYPE D FLIP FLOP

The 9913 is a gated flip-flop very suitable for shift registers and control circuitry. The state of the input at pin 2 is stored in the element when the input at pin 1 changes from logical "1" to logical "0." The element can be reset only when pin 1 is maintained at a logical "1" during the time that pin 7 undergoes a change from a logical "0" to a logical "1."

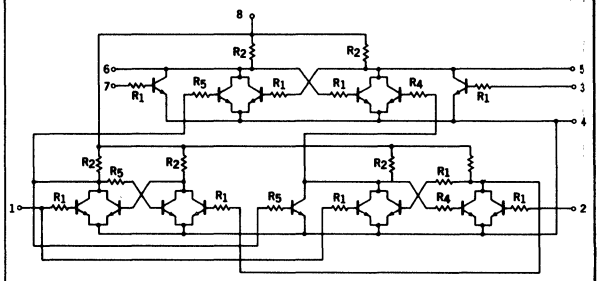


FUNCTIONS

DIRECT INPUTS[1]				GATED INPUT[3]		
				t = n	t = n + 1	
3	7	6	5	2	6	5
L	L	NC	NC[2]	H	H	L
L	H	L	H	L	L	H
H	L	H	L			
H	H	L	L			

(1) Pin 1 must be high.
(2) NC = No change.
(3) Pins 3 and 7 must be low.

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 1.5k\Omega$
$R_2 = 3.6k\Omega$
$R_4 = 180\Omega$
$R_5 = 480\Omega$

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

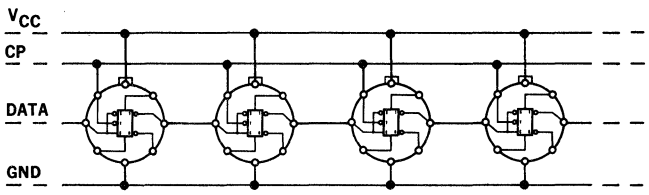
NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

LOADING RULES

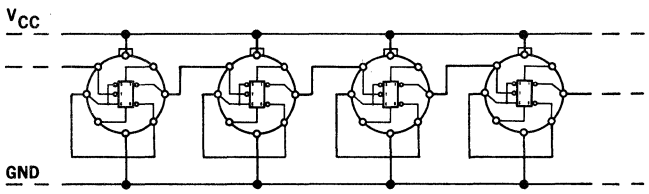
INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	2	5	3
2	1	6	3
3	1		
7	1		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

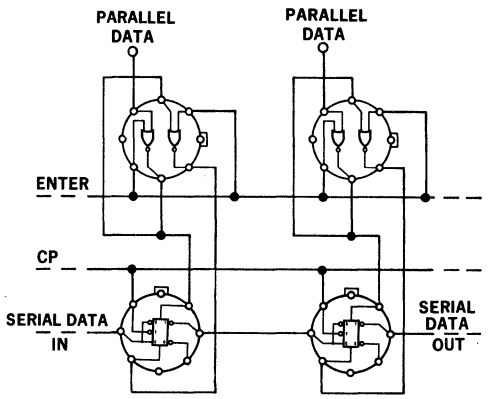
TYPICAL APPLICATIONS



SHIFT REGISTER STAGES USING TYPE D FLIP-FLOP



BINARY RIPPLE CARRY COUNTER STAGES USING TYPE D FLIP-FLOP



METHOD OF PARALLEL ENTRY OF DATA INTO SHIFT REGISTER
V_{CC} AND GROUND CONNECTIONS ARE NOT SHOWN

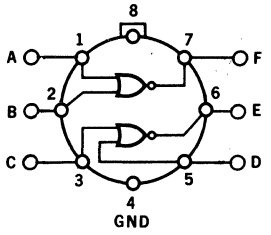
9914 MEDIUM POWER DUAL TWO INPUT GATE*

The Dual Two-Input Gate element is a dual combination of two-input resistor-transistor-logic circuits, one of four similar basic NAND/NOR gates produced by Fairchild. The versatility of the NAND/NOR function permits the generation of any logic-function through the exclusive use of dual two-input gate elements. In addition to the applications of other gate-type elements, the dual two-input gate element circuits may be cross-connected to form a flip-flop, or in tandem to form noninverting gates.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

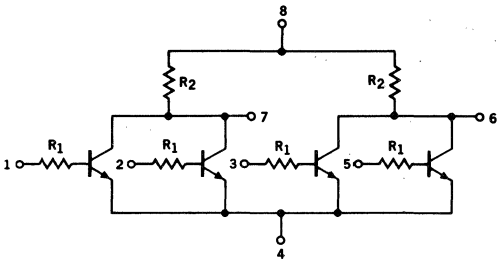


FUNCTIONS

POSITIVE LOGIC:
$F = \overline{A + B} = \overline{A}\,\overline{B}$
$E = \overline{C + D} = \overline{C}\,\overline{D}$

NEGATIVE LOGIC:
$F = \overline{A}\,\overline{B} = \overline{A} + \overline{B}$
$E = \overline{C}\,\overline{D} = \overline{C} + \overline{D}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES
$R_1 = 450\Omega$
$R_2 = 640\Omega$

TRUTH TABLE

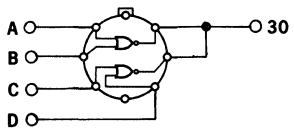
A	B	F
H	H	L
H	L	L
L	H	L
L	L	H

LOADING RULES

INPUT PIN	LOAD FACTORS	OUTPUT PIN	DRIVE FACTOR
1	3	6	16
2	3	7	16
3	3		
5	3		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

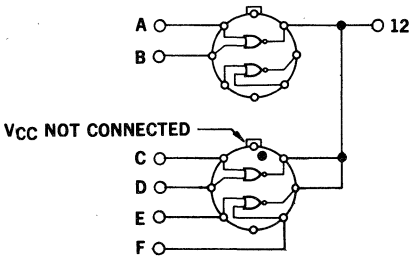
TYPICAL APPLICATIONS



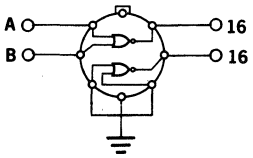
FOUR INPUT GATE

POSITIVE LOGIC:
$\overline{A + B + C + D} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$

NEGATIVE LOGIC:
$\overline{A\,B\,C\,D} = \overline{A} + \overline{B} + \overline{C} + \overline{D}$



SIX INPUT GATE



TWO INPUT GATE

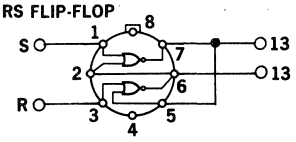
POSITIVE LOGIC:
$\overline{A + B} = \overline{A} \cdot \overline{B}$

NEGATIVE LOGIC:
$\overline{A \cdot B} = \overline{A} + \overline{B}$

PIN NUMBERS			
INPUT		OUTPUT	
1	3	6	7
L	L	NC	NC
L	H	L	H
H	L	H	L
H	H	NOT ALLOWED	

NC = No change.

RS FLIP-FLOP



* This element also available in the epoxy package.

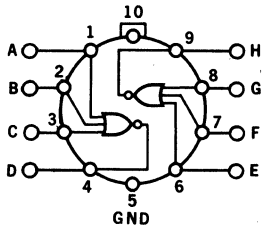
9915 MEDIUM POWER DUAL THREE INPUT GATE

The Dual Three-Input Gate element is a dual combination of three-input resistor-transistor-logic circuits, one of four similar basic NAND/NOR gates produced by Fairchild. The versatility of the NAND/NOR function permits the generation of any logic-function through the exclusive use of dual three-input gate elements. In addition to the applications of other gate-type elements, the dual three-input gate element circuits may be cross-connected to form a flip-flop with 2 set and 2 reset inputs, or in tandem to form non-inverting gates.

H = HIGH
L = LOW

POSITIVE LOGIC: H = 1 = TRUE
L = 0 = FALSE

NEGATIVE LOGIC: L = 1 = TRUE
H = 0 = FALSE

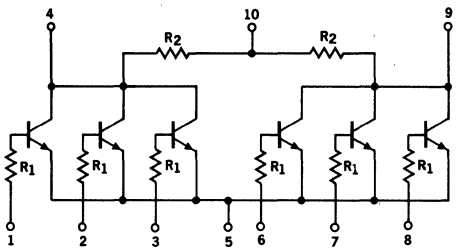


FUNCTIONS

POSITIVE LOGIC:
$D = \overline{A + B + C} = \overline{A}\,\overline{B}\,\overline{C}$
$H = \overline{E + F + G} = \overline{E}\,\overline{F}\,\overline{G}$

NEGATIVE LOGIC:
$D = \overline{A}\,\overline{B}\,\overline{C} = \overline{A + B + C}$
$H = \overline{E}\,\overline{F}\,\overline{G} = \overline{E + F + G}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 450\Omega$
$R_2 = 640\Omega$

TRUTH TABLE

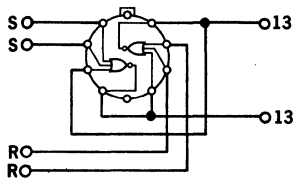
A	B	C	D
H	H	H	L
H	H	L	L
H	L	H	L
H	L	L	L
L	H	H	L
L	H	L	L
L	L	H	L
L	L	L	H

LOADING RULES

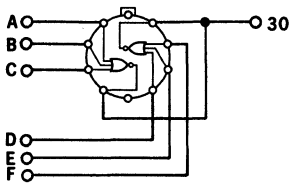
INPUT PIN	LOAD FACTORS	OUTPUT PIN	DRIVE FACTORS
1	3	4	16
2	3	9	16
3	3		
6	3		
7	3		
8	3		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



RS FLIP-FLOP



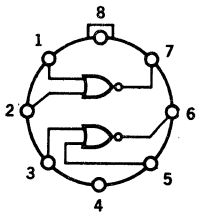
SIX INPUT GATE

POSITIVE LOGIC:
$\overline{A + B + C + D + E + F} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} \cdot \overline{E} \cdot \overline{F}$

NEGATIVE LOGIC:
$\overline{A \cdot B \cdot C \cdot D \cdot E \cdot F} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F}$

9921 LOW POWER GATE EXPANDER

This element is a double gate without the node resistors. Its output terminals may be connected in parallel to those of the 9910 or 9911 elements to increase the fan-in capability of the circuit. Pin 8 of the element must always be connected to V_{CC}.



FUNCTIONS

POSITIVE LOGIC:

$7 = \overline{1 + 2}$

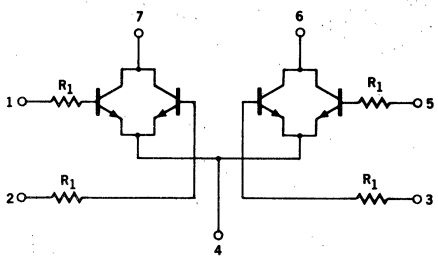
$6 = \overline{3 + 5}$

NEGATIVE LOGIC:

$7 = \overline{1 \cdot 2}$

$6 = \overline{3 \cdot 5}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

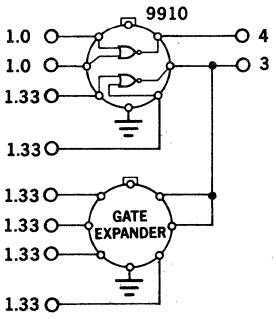
$R_1 = 1.5k\Omega$

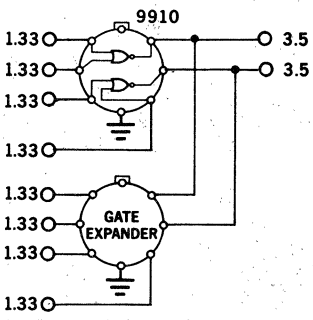
LOADING RULES

INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTORS
1	1	6	–0.5
2	1	7	–0.5
3	1		
5	1		

Note: For more information on loading rules and for parallel combination of elements, see page 2.

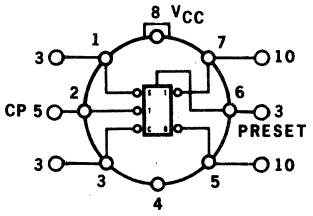
TYPICAL APPLICATIONS





9923 MEDIUM POWER JK FLIP FLOP*

The 9923 Industrial Flip-Flop is a fully integrated, monolithic circuit. This element is designed for use in industrial shift-register and binary counting applications. The 9923 JK Flip-Flop is compatible with the basic Industrial Micrologic® integrated circuit family and is guaranteed to operate at a frequency of 2.0 MHz minimum over the 0°C to 70°C temperature range.

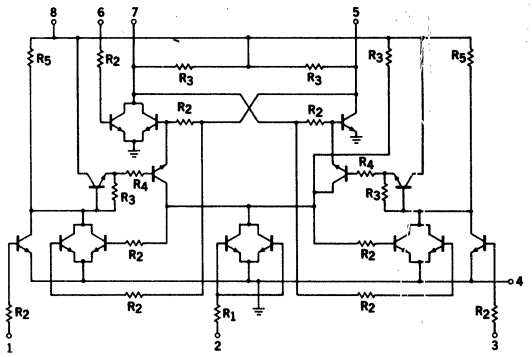


FUNCTIONS

SET (1)	CLEAR (3)	OUTPUT (7)
	t = n	t = n +1
H	H	X^n
H	L	H
L	H	L
L	L	$\overline{X^n}$

H = HIGH
L = LOW
X IS THE OUTPUT STATE AT TIME n
A HIGH ON PIN 6 WILL PRESET OUTPUT PIN 7 LOW

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

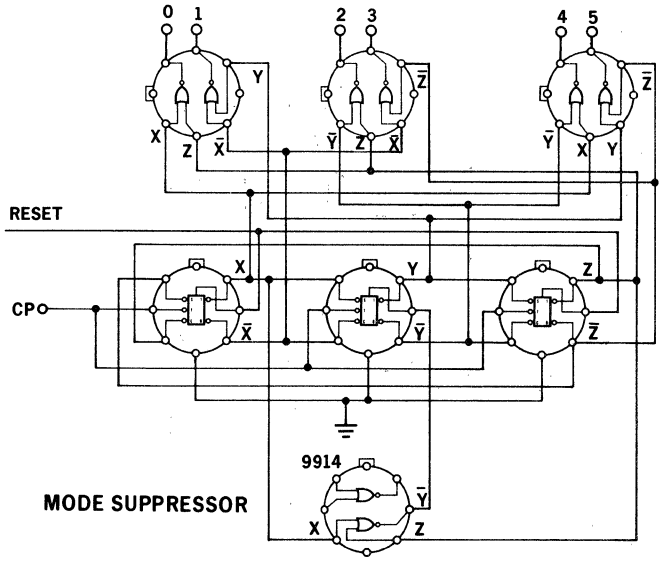
$R_1 = 260\Omega$ $R_4 = 300\Omega$
$R_2 = 450\Omega$ $R_5 = 700\Omega$
$R_3 = 640\Omega$

LOADING RULES

INPUT PIN	LOAD FACTOR	OUTPUT PIN	DRIVE FACTOR
1	3	5	10
2	5	6	3
3	3	7	10

Note: For more information on loading rules and for parallel combination of elements, see page 2.

TYPICAL APPLICATIONS



MOD 6 SHIFT REGISTER COUNTER WITH DECODING

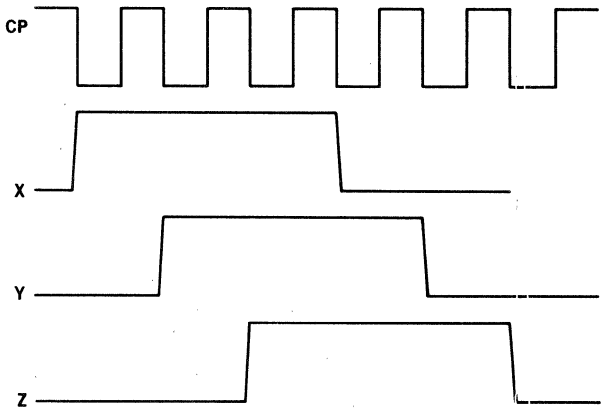
TRUTH TABLE

CT	X	Y	Z
0	L	L	L
1	H	L	L
2	H	H	L
3	H	H	H
4	L	H	H
5	L	L	H

DECODING

1	2
X	Z
$\overline{X}$	Y
$\overline{Y}$	Z
$\overline{X}$	$\overline{Z}$
X	$\overline{Y}$
Y	$\overline{Z}$

TIME DIAGRAM:



* This element also available in the epoxy package.

9926 MEDIUM POWER JK FLIP FLOP

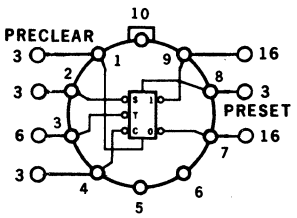
The Fairchild JK Flip-Flop is a complete, general-purpose, storage element suitable for use in shift registers, counters or any type of control function.

The JK Flip-Flop differs from ordinary RS Flip-Flops in that no ambiguous output state can result from simultaneous one inputs. In the JK Flip-Flop simultaneous ones on both the set and clear inputs cause the output state to toggle (reverse). This feature enhances the operation of the JK Flip-Flop in binary counters, as no external feedback connections are required. The toggling action can also be used to advantage for minimizing the logic structure of control units.

The unique input triggering circuit permits the JK Flip-Flop to respond to negative clock pulse transitions as short as 1 nanosecond or as long as 100 nanoseconds.

Asynchronous preset and preclear inputs are included for presetting counters, inserting parallel data in registers, and similar applications.

This element is guaranteed to operate at a frequency of 8.0 MHz minimum (20.0 MHz typical) over the 0°C to 70°C temperature range.

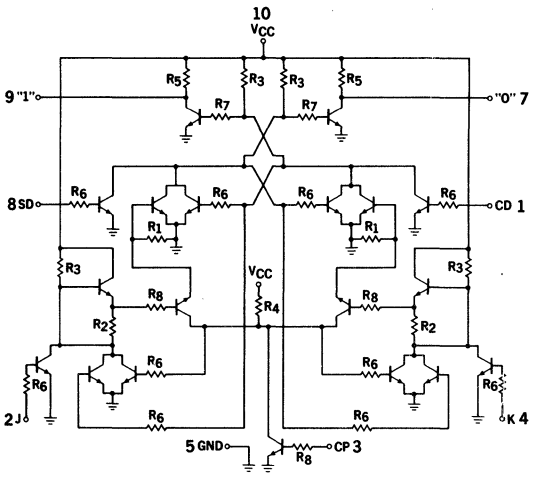


FUNCTIONS

SET (2)	CLEAR (4)	OUTPUT (9)
t = n		t = n +1
H	H	X^n
H	L	H
L	H	L
L	L	$\overline{X^n}$

H = HIGH
L = LOW
X IS THE OUTPUT STATE AT TIME n

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

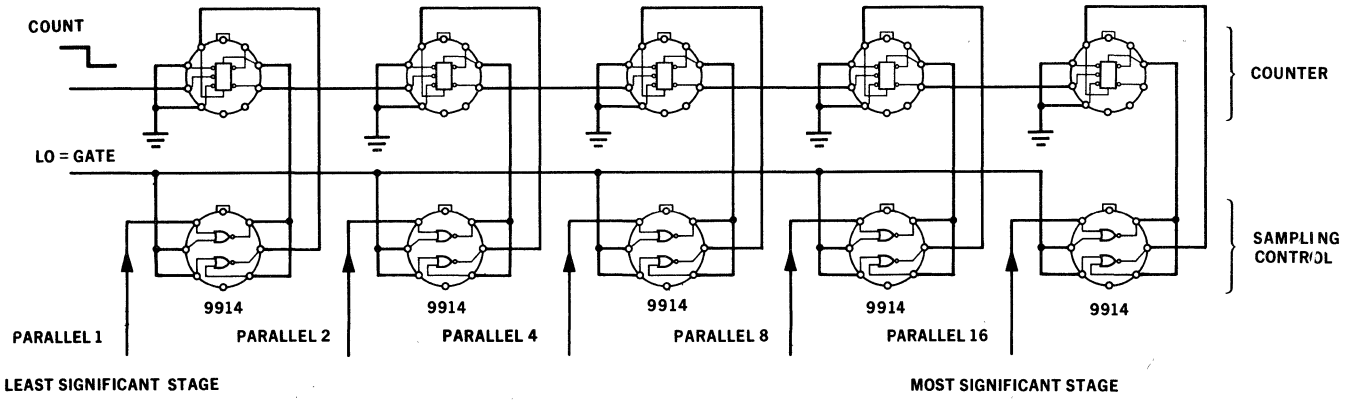
$R_1 = 3k\Omega$ $R_3 = 900\Omega$ $R_5 = 640\Omega$ $R_7 = 550\Omega$
$R_2 = 1.0k\Omega$ $R_4 = 700\Omega$ $R_6 = 600\Omega$ $R_8 = 300\Omega$

LOADING RULES

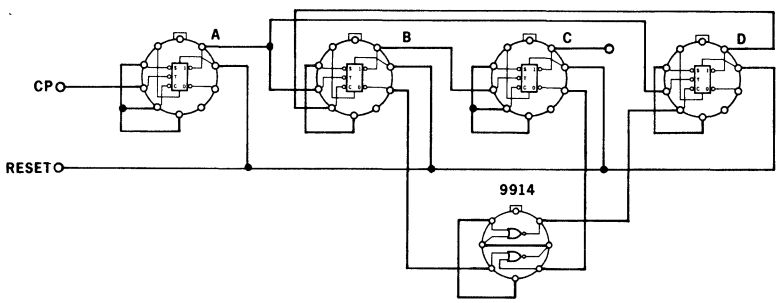
INPUT PIN	LOAD FACTORS	OUTPUT PIN	DRIVE FACTOR
1	3	7	16
2	3	8	3
3	6	9	16
4	3		

Pin configurations for TO-5, Cerpak and Flatpack are identical.

TYPICAL APPLICATIONS



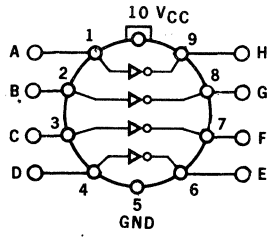
BINARY COUNTER AND SAMPLING CONTROL



1-2-4-8, MOD 10, COUNT UP COUNTER (POSITIVE LOGIC)

9927 MEDIUM POWER QUAD INVERTER

The Quad Inverter element is a four-input resistor-transistor-logic inverter circuit. This circuit is very useful where a complement of several signals is desired simultaneously.

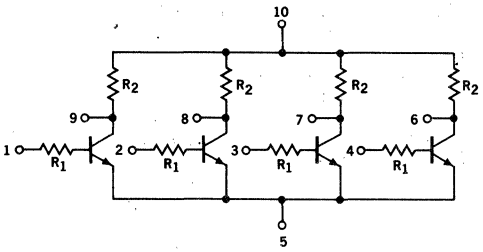


FUNCTIONS

POSITIVE AND NEGATIVE LOGIC:

$H = \overline{A}$
$G = \overline{B}$
$F = \overline{C}$
$E = \overline{D}$

SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

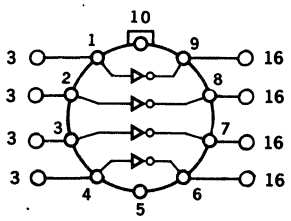
$R_1 = 450\Omega$
$R_2 = 640\Omega$

LOADING RULES

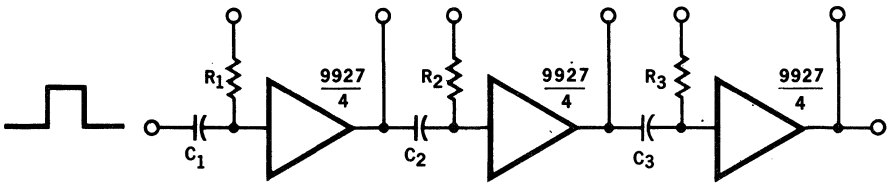
INPUT PIN	LOAD FACTORS	OUTPUT PIN	DRIVE FACTOR
1	3	6	16
2	3	7	16
3	3	8	16
4	3	9	16

Note:
For more information on loading rules and for parallel combination of elements, see page 2.

LOADING CHART



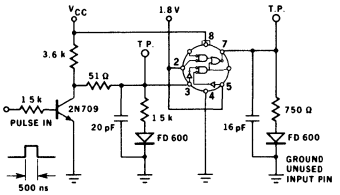
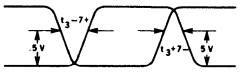
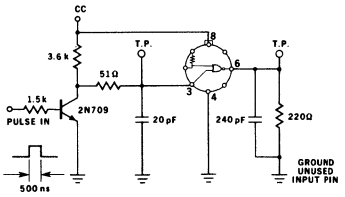
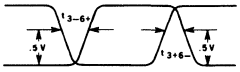
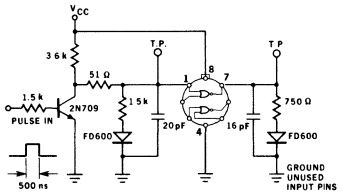
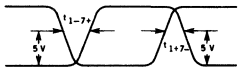
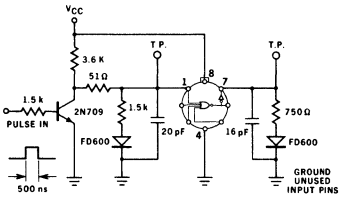
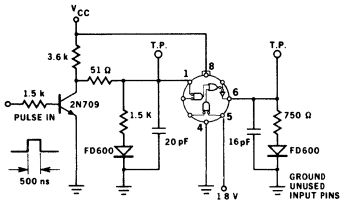
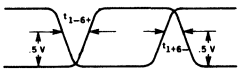
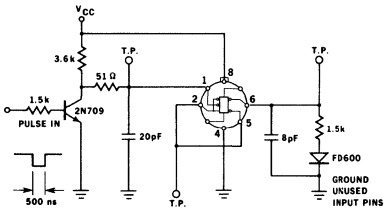
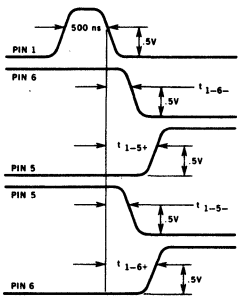
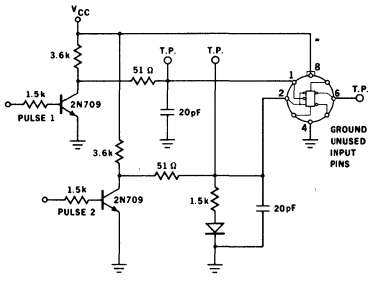
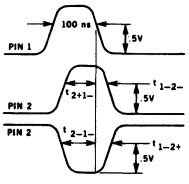
TYPICAL APPLICATIONS



DELAY INTRODUCED IN EACH STAGE IS A FUNCTION OF RC TIME CONSTANT

PULSE DELAY/SHAPER CIRCUIT

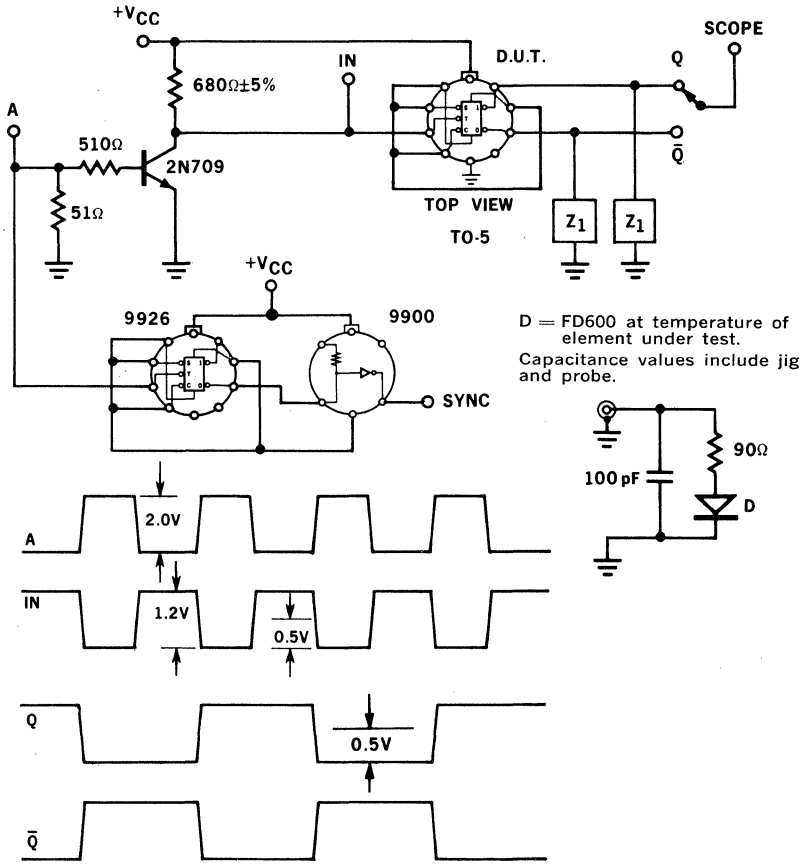
LOW POWER ELEMENTS -- PROPAGATION DELAY GUARANTEED LIMITS

ELEMENT		ns(max)		
9908	t_{3-7+} t_{3+7-}	80 100		
9909	t_{3+6-} t_{3-6+}	90 70		
9910	t_{1-7+} t_{1+7-}	40 50		
9911	t_{1-7-} t_{1+7+}	70 90		
9912	t_{1+6-} t_{1-6+}	100 80		
9913	t_{1-5-}, t_{1-6-} t_{1-5+}, t_{1-6+}	80 120		
	t_{2+1-}, t_{1-2+} t_{1-2-}, t_{2-1-}	60 min 30 min		

MEDIUM POWER ELEMENTS -- PROPAGATION DELAY GUARANTEED LIMITS

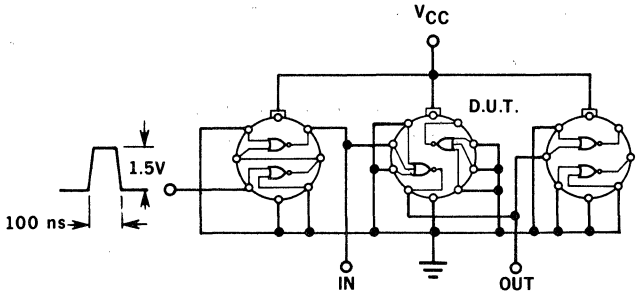
ELEMENT		MAX.
9900	t_{3-5-}	32 ns
	t_{3+5-}	32 ns
9903	t_{2+6-}	20 ns
	t_{2-6+}	32 ns
9905	t_{2+6-}	30 ns
	t_{2-6+}	26 ns
	t_{1+7+}	42 ns
	t_{1-7-}	42 ns
9904	t_{3+6-}	20 ns
	t_{3-6+}	32 ns
	t_{1+7+}	38 ns
	t_{1-7-}	38 ns
9907	t_{2+6-}	20 ns
	t_{2-6+}	32 ns
9914	t_{1+7-}	20 ns
	t_{1-7+}	32 ns
9915	t_{2+4-}	20 ns
	t_{2-4+}	32 ns
9923	t_{2-7+}	80 ns
	t_{2-7-}	50 ns
	t_{2-5+}	80 ns
	t_{2-5-}	50 ns
9926	t_{3-9+}	60 ns
	t_{3-9-}	60 ns
	t_{3-7+}	60 ns
	t_{3-7-}	60 ns
9927	t_{2+8-}	20 ns
	t_{2-8+}	32 ns

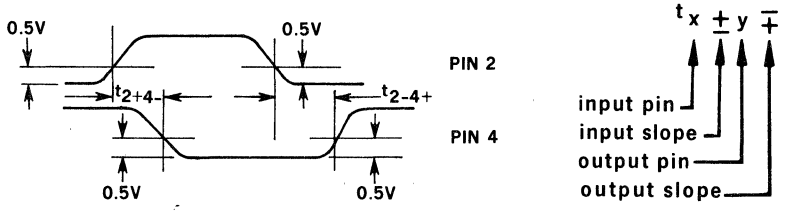
PROPAGATION DELAY AND TOGGLE TEST CIRCUIT FOR JK 9923 OR 9926



D = FD600 at temperature of element under test.
Capacitance values include jig and probe.

SWITCHING TIME TEST CIRCUIT: (FOR A GATE TYPE DEVICE)





Switching time test circuit shown above is for μL 9915, but the input and output loading circuit shown is the same for Micrologic 9900, 9903, 9904, 9905, 9907, 9914, and 9927 elements. By appropriately connecting the input and output pins of the device under test (D.U.T.) in the circuit above, switching speeds could be measured in any of the said elements.

LOW POWER RTμL

PLANAR* EPITAXIAL LOW POWER RESISTOR—TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

WHAT IS LOW POWER RTμL?

Fairchild Low Power RTμL Integrated Circuits are a set of compatible, integrated logic building blocks. The elements are manufactured using the Fairchild Planar* epitaxial process by which all the necessary transistors and resistors are diffused into a single silicon wafer. The individual RTL gates within the logic blocks are interconnected by metal over oxide.

SPEED AND POWER

Low Power RTμL is characterized by very low propagation delays at low DC power dissipation. Typical propagation delay for the basic RTL circuit is 40 nanoseconds, and its power dissipation is typically 2 mW.

ABSOLUTE MAXIMUM RATINGS (25°C Free Air Temperature)

Maximum voltage applied to pin 8 (continuous)	8 V
Maximum voltage applied to any input pin	±4.0 volts
Storage Temperature	−65°C to +150°C
Maximum Power Dissipation	250 mW
Maximum Voltage applied to pin 8 (Pulsed, ≤1 second)	12 V

PURCHASING INFORMATION

Purchasing Agent please note:

To order part, the following numbering system should be used to expedite handling. The complete number will be a seven digit number with the designations as follows.

ABCDEFG

A = 9 for all elements.

B = 5 for the TO-5 package. 1 for the flat package.

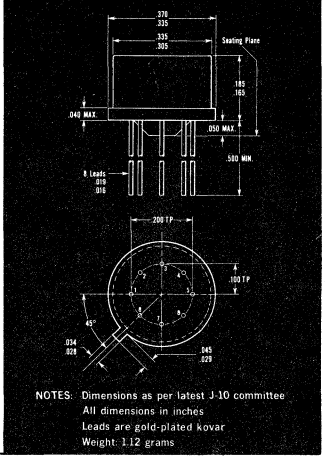
CDE = the four digit number denoting the specific element desired (i.e. the buffer) would be 9909.

F = 2 for Planar epitaxial material.

G = 1 for −55°C to +125°C operation.

PHYSICAL DIMENSIONS

(SIMILAR TO TO-5)



NOTES: Dimensions as per latest J-10 committee
All dimensions in inches
Leads are gold-plated kovar
Weight: 1.12 grams

AMBIENT TEMPERATURE OPERATION

Low Power RTμL Integrated Circuits may be used in accordance with the Loading Chart below through the full military temperature range of −55°C to +125°C. Nominal Supply voltage is 3.00 Volts. The Loading Chart below is valid for V_{CC} = 3.00 Volts ±10%. Improved speed and Noise Immunity will result if V_{CC} is increased above 3.00 Volts to a maximum of 3.66 Volts at +125°C with maximum V_{CC} increasing linearly to 4.5 Volts at −55°C.

ELEMENTS

The 9908 Element (ADDER) performs MOD 2 Addition, the exclusive OR function, and control of 2 data streams (pins 1 and 5) by tying pins 2 and 3 together to control.

The 9909 Element (BUFFER) is a 2 input, high fan-out, inverting gate, with internal timing resistor.

The 9910 Element (DUAL GATE) is a dual, 2 input gate.

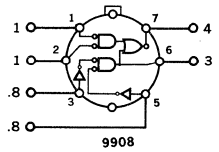
The 9911 Element (GATE) is a 4 input gate with added inverter for the output to generate OR, NOR, AND, and NAND functions.

The 9912 Element (HALF-ADDER) is a two-level AND-OR gate with added output inverter.

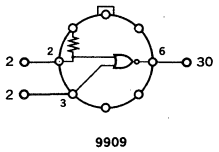
The 9913 Element (TYPE D FLIP-FLOP) is a gated D-Flip-Flop with asynchronous set and reset inputs suitable for shifting and counting. The 9913 was previously known as an R, Register, or Full Shift Register Eelement.

The 9921 Element (EXPANDER) is a dual 2 input gate without node resistors, to be used when increased fan-in is required.

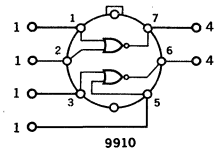
LOW POWER RTμL LOADING CHART valid for system operation from −55°C to +125°C (symbols shown top view)



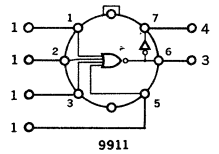
9908



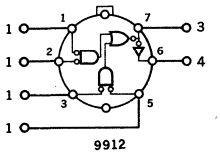
9909



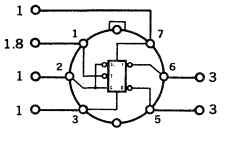
9910



9911



9912



9913

* Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

GENERAL RULES

The number of elements that may be driven by an output terminal may consist of any combination of elements whose summation of input loading does not exceed the output terminal driving capability.

Unused input pins should be tied to ground.

See expander element (9921) for paralleling.

FIG. 1
TYPICAL POWER DISSIPATION VS. V_{CC}

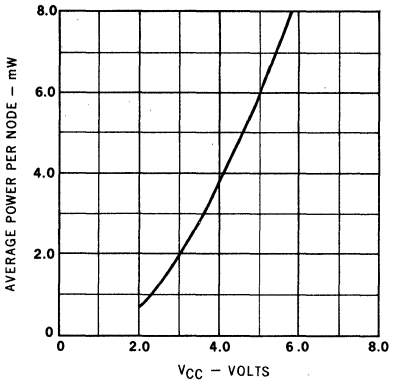


FIG. 2a
TYPICAL SIGNAL LEVEL VS. TEMPERATURE
V_{CC} = 3.0V

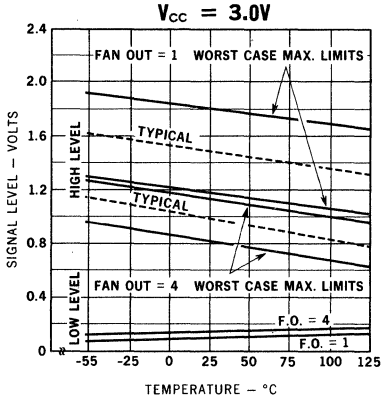


FIG. 2b
TYPICAL SIGNAL LEVEL VS. TEMPERATURE
V_{CC} = 4.0V

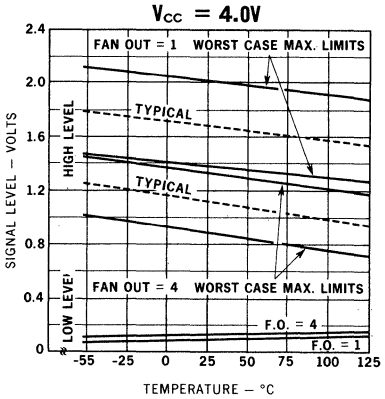
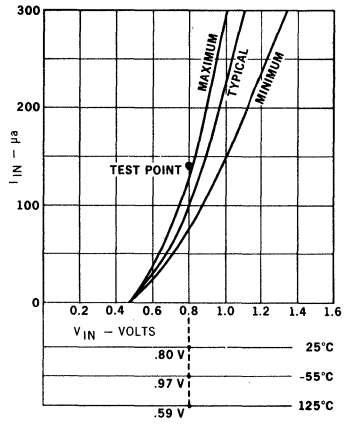
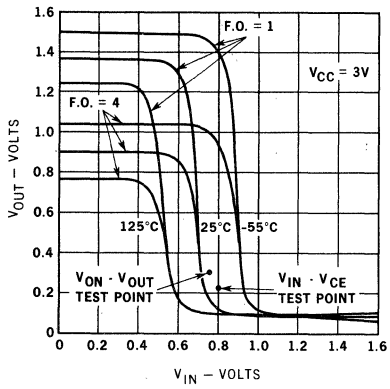


FIG. 3
TYPICAL INPUT CHARACTERISTICS



Note: This curve will apply as V_{CC} is increased from 3 V to 5 V with small decrease in I_{IN} for same V_{IN}.

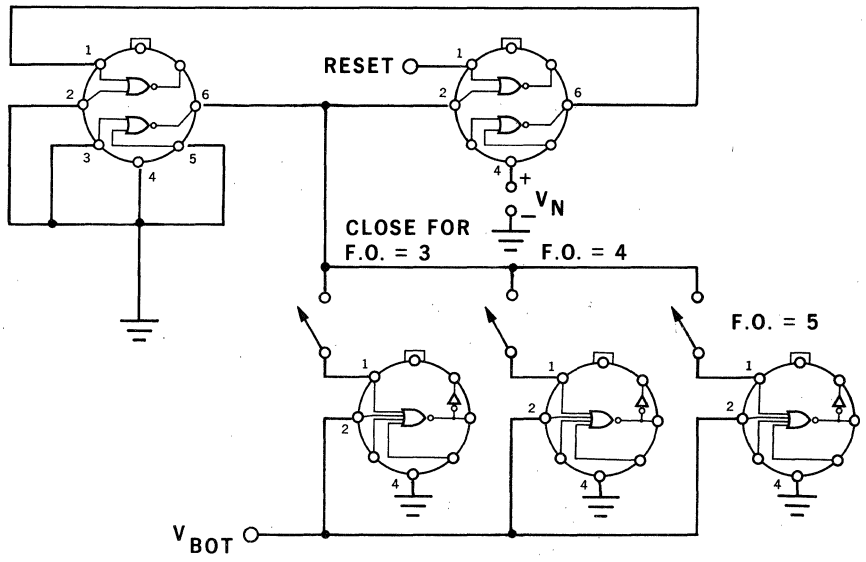
FIG. 4
TRANSFER CHARACTERISTICS



TYPICAL V_{ON} VS. V_{CC}

	−55°C	+25°C	+125°C
V_{CC} = 3 V	.890	.680	.530
V_{CC} = 4 V	.940	.710	.550
V_{CC} = 5 V	.990	.750	.575

FIG. 5 TEST CIRCUIT FOR NOISE THRESHOLD MEASUREMENTS



V_{CC}	V_{BOT}
3 V	1.8 V
4 V	2.0 V
5 V	2.4 V
6 V	2.9 V

Note that elements with specified fan-out = 4 have good immunity to worst case ground noise in a test circuit when used in a fan-out = 5 configuration.

FIG. 6
DC NOISE THRESHOLD VS. V_{CC}

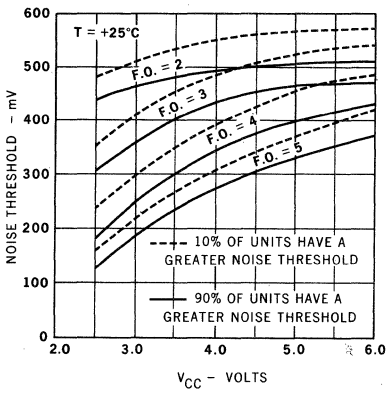


FIG. 7
DC NOISE THRESHOLD VS. V_{CC}

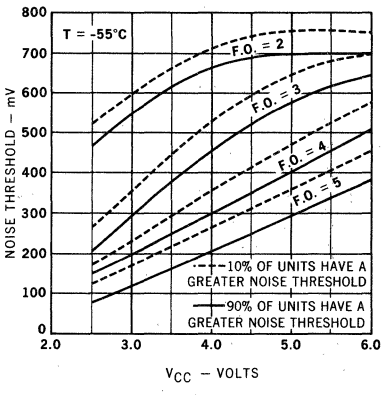


FIG. 8
DC NOISE THRESHOLD VS. V_{CC}

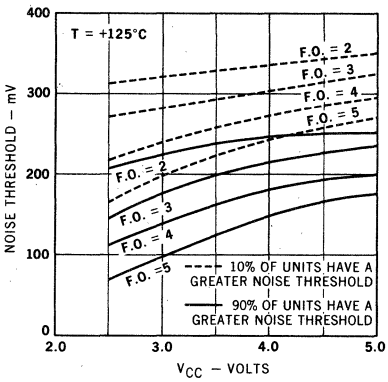


FIG. 9
TYPICAL PULSED NOISE THRESHOLD VERSUS PULSE WIDTH

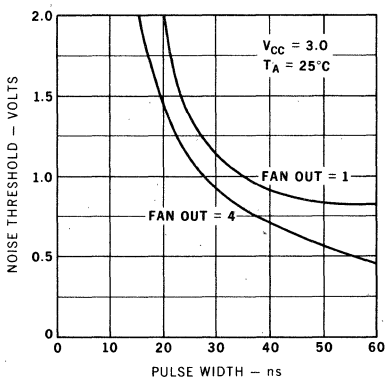


FIG. 10
TYPICAL PULSED NOISE THRESHOLD VERSUS PULSE WIDTH

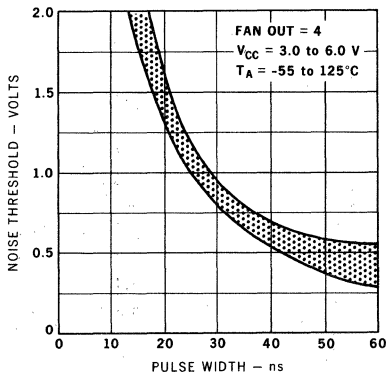
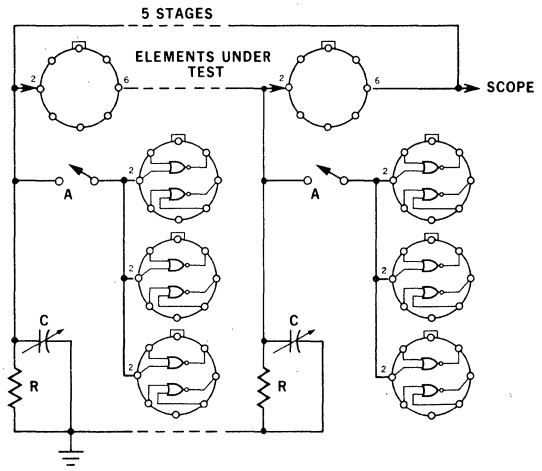


FIG. 11 TEST CIRCUIT AND TABLE FOR TYPICAL t_{pd} MEASUREMENTS



Connect pin 8 to V_{CC}
Connect pin 4 to ground.
Connect all unused input pins to ground

$$\text{AVERAGE } t_{pd} = \frac{1}{f_{osc}} \times \frac{1}{10}$$

ELEMENT	R	INPUT PIN NO.	OUTPUT PIN NO.	OTHER INPUTS	NOTE
9908 ADDER	∞	3	7	PINS 2 & 5 TO 1.8 V	2
9909 BUFFER	220 Ω	3	6	—	1
9910 DUAL GATE	∞	1	7	2, 3, & 5 TO GND	2
9912 HALF ADDER	∞	2	6	PIN 3 TO 1.8 V	2

TEST FOR 9909 ELEMENTS

1. All "A" switches left open in t_{pd} test for 9909 element.
2. For curves shown, fan-out = 1 corresponds to switch "A" open; and for fan-out = 4, switch "A" closed.

AVERAGE PROPAGATION DELAY VERSUS CAPICITANCE

FIG. 12

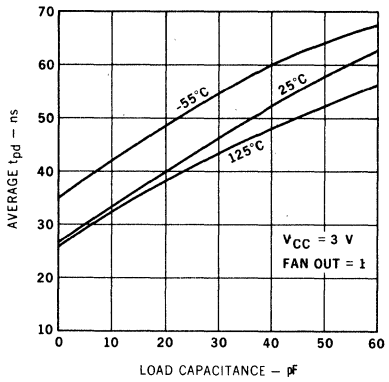


FIG. 13

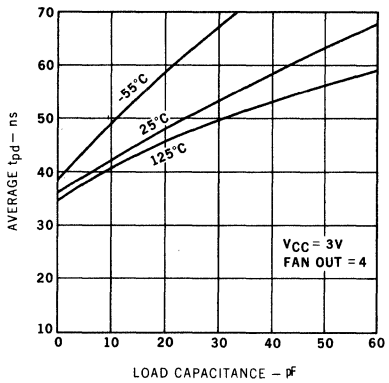


FIG. 14

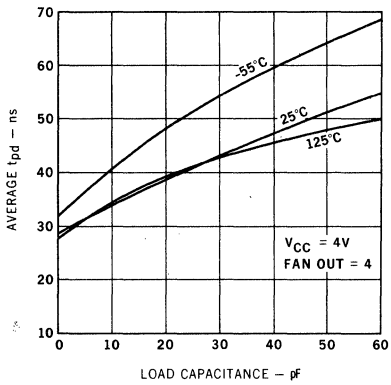


FIG. 15

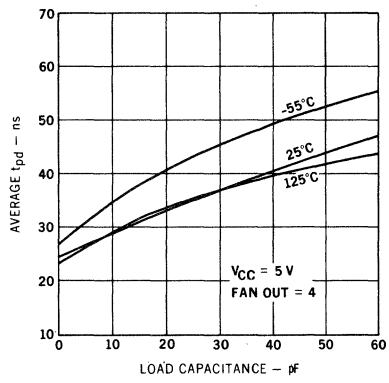


FIG. 16

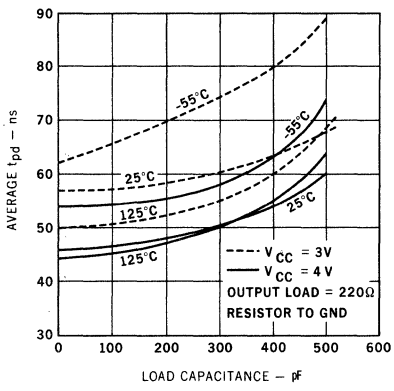
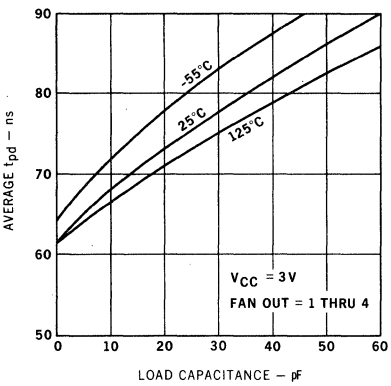


FIG. 17



9908 LOW POWER RTμL ADDER

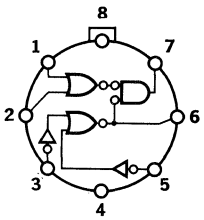
THE LOW POWER RTμL ADDER PERFORMS THE **MOD 2** ADDITION OR EXCLUSIVE **OR** FUNCTION; IT ALSO IS USED TO SELECT ONE OF TWO DATA STREAMS UNDER CONTROL OF A SINGLE GATE SIGNAL.

AVERAGE POWER DISSIPATION (25°C)

10 mW

LOGIC SYMBOL AND FUNCTIONS

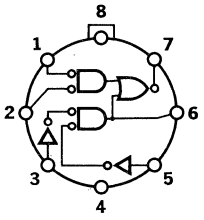
POSITIVE LOGIC



$6 = \overline{(\bar{3}+\bar{5})} = 3 \cdot 5$

$7 = (1+2)\ (\bar{3}+\bar{5})$

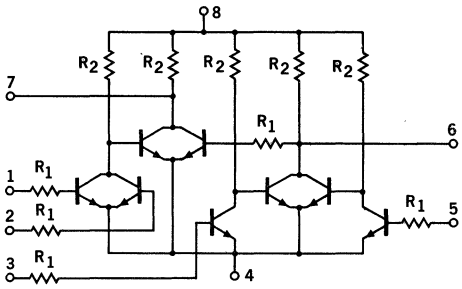
NEGATIVE LOGIC



$6 = \overline{(\bar{3} \cdot \bar{5})} = 3+5$

$7 = 1 \cdot 2 + \bar{3} \cdot \bar{5}$

CIRCUIT DIAGRAM

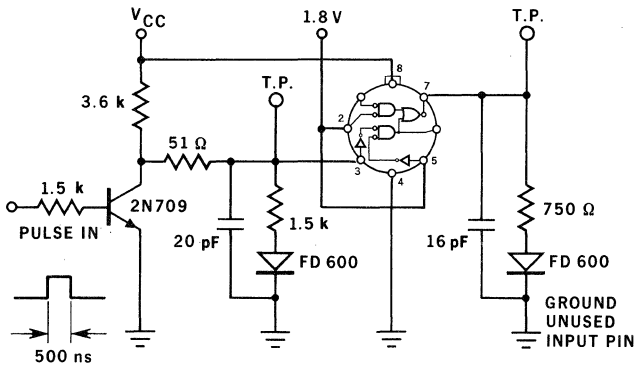


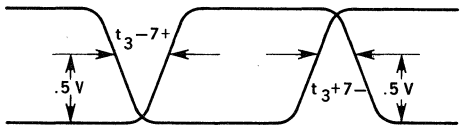
Typical Resistors

$R_1 = 1.5\,k\Omega$

$R_2 = 3.6\,k\Omega$

SWITCHING TIME TEST CIRCUIT





Test No.	Test	Note	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	MIN.	MAX.
1	I_3		GND	GND	V_{IN}	GND	GND			V_{CC}		$.81_{IN}$
2	I_5		GND	GND	GND	GND	V_{IN}			V_{CC}		$.81_{IN}$
3	I_1		V_{IN}	V_{BOT}	GND	GND	GND			V_{CC}		I_{IN}
4	I_2		V_{BOT}	V_{IN}	GND	GND	GND			V_{CC}		I_{IN}
5	I_6		GND	GND	V_{ON}	GND	V_{ON}	V_{IN}		V_{CC}	I_{A3}	
6	I_7		V_{ON}	GND	V_{OFF}	GND	V_{OFF}		V_{IN}	V_{CC}	I_{A4}	
7	I_7		GND	V_{ON}	V_{OFF}	GND	V_{OFF}		V_{IN}	V_{CC}	I_{A4}	
8	V_6		GND	GND	V_{BOT}	GND	V_{OFF}			V_{CC}		V_{CE}
9	V_6		GND	GND	V_{OFF}	GND	V_{BOT}			V_{CC}		V_{CE}
10	V_7		V_{OFF}	V_{OFF}	GND	GND	GND			V_{CC}		V_{CE}
11	V_7		V_{BOT}	V_{BOT}	V_{BOT}	GND	V_{BOT}	V_{IN}		V_{CC}		V_{CE}
12	V_7		V_{BOT}	V_{BOT}	V_{BOT}	GND	V_{BOT}	V_{ON}		V_{CC}		V_{OUT}
13	I_8		GND	GND	GND	GND	GND			V_{LL}		I_L
14	t_{3-7+}		GND	V_{BOT}	Pulse in	GND	V_{BOT}		Pulse out	V_{CC}		80 ns
15	t_{3+7-}		GND	V_{BOT}	Pulse in	GND	V_{BOT}		Pulse out	V_{CC}		100 ns

9909 LOW POWER RTμL BUFFER

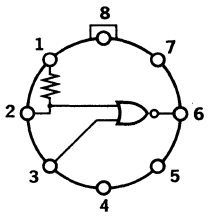
THE LOW POWER RTμL BUFFER IS A LOW IMPEDANCE INVERTING DRIVER CIRCUIT. THE ELEMENT CAN SUPPLY SUBSTANTIALLY MORE OUTPUT CURRENT THAN THE BASIC **RTL** CIRCUIT. A RESISTOR IS INTERNALLY CONNECTED TO THE BUFFER ELEMENT INPUT WHICH MAY BE RETURNED TO THE SUPPLY VOLTAGE IF CAPACITIVE COUPLING IS DESIRED. TYPICAL APPLICATIONS OF THIS TYPE CONNECTION ARE ASTABLE AND MONOSTABLE MULTIVIBRATORS, AND FOR THE DIFFERENTIATION OF PULSES.

AVERAGE POWER DISSIPATION (25°C)
10 mW at 50% Duty Cycle

LOGIC SYMBOL AND FUNCTIONS

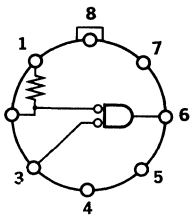
POSITIVE LOGIC

$6 = \overline{2+3}$

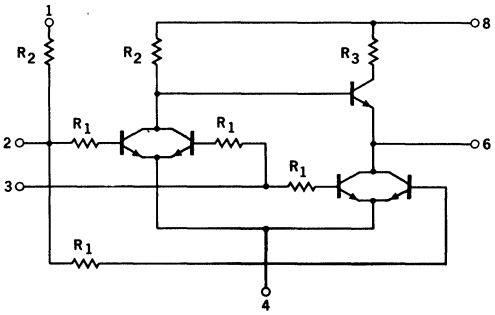


NEGATIVE LOGIC

$6 = \overline{2 \cdot 3}$



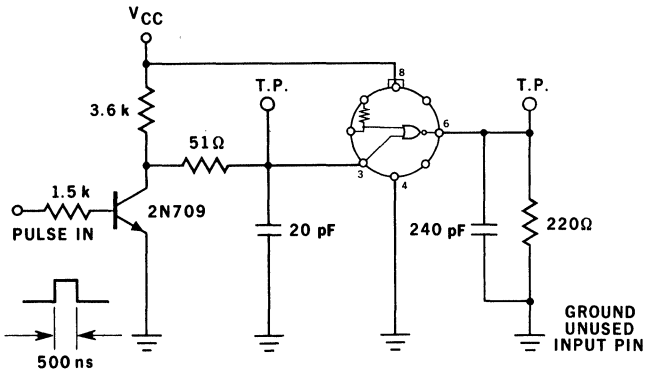
CIRCUIT DIAGRAM

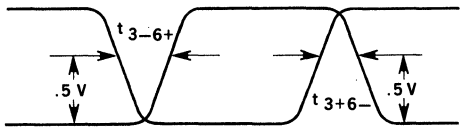


Typical Resistors

$R_2 = 3.6\,k\Omega$
$R_1 = 1.5\,k\Omega$
$R_3 = 100\Omega$

SWITCHING TIME TEST CIRCUIT





Test No.	Test	Note	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	MIN.	MAX.
1	I_2			V_{IN}	V_{BOT}	GND				V_{CC}		$2I_{IN}$
2	I_3			V_{BOT}	V_{IN}	GND				V_{CC}		$2I_{IN}$
3	V_6			V_{OFF}	V_{OFF}	GND		V_{IN}		V_{CC}	I_{AB}	
4	V_6			V_{ON}	GND	GND		V_{RH}		V_{CC}		V_{OUT}
5	V_6			GND	V_{ON}	GND		V_{RH}		V_{CC}		V_{OUT}
6	V_6			V_{IN}	GND	GND		V_{RH}		V_{CC}		V_{CE}
7	V_6			GND	V_{IN}	GND		V_{RH}		V_{CC}		V_{CE}
8	I_8			GND	GND	GND				V_{CC}		I_L
9	t_{3+6-}			GND	Pulse in	GND		Pulse out		V_{CC}		90 ns
10	t_{3-6+}			GND	Pulse in	GND		Pulse out		V_{CC}		70 ns

9910 LOW POWER RTμL DUAL GATE

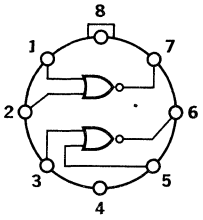
THE LOW POWER RTμL DUAL GATE MAY BE USED AS A PAIR OF NOR GATES, AS AN R-S FLIP-FLOP, AS A PAIR OF INVERTERS, OR AS A DOUBLE INVERTER. IT MAY ALSO BE USED WITH THE LOW POWER RTμL GATE EXPANDER TO INCREASE ITS FAN-IN CAPACITY.

AVERAGE POWER DISSIPATION (25°C)

4 mW

LOGIC SYMBOL AND FUNCTIONS

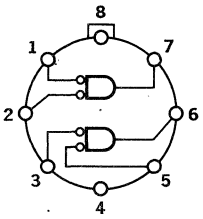
POSITIVE LOGIC



$7 = \overline{1+2}$

$6 = \overline{3+5}$

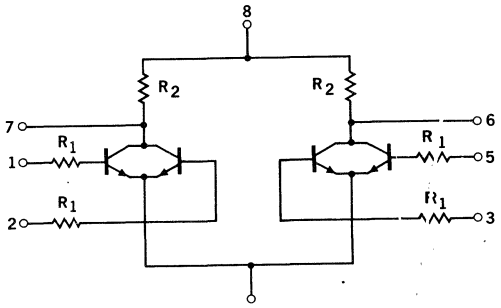
NEGATIVE LOGIC



$7 = \overline{1 \cdot 2}$

$6 = \overline{3 \cdot 5}$

CIRCUIT DIAGRAM

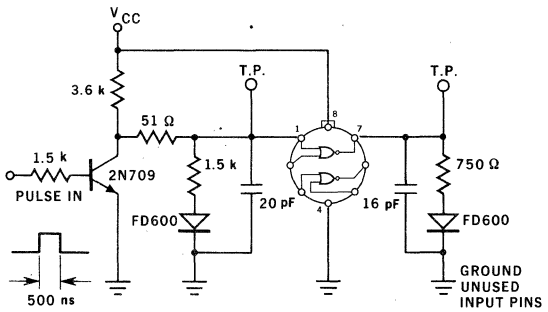


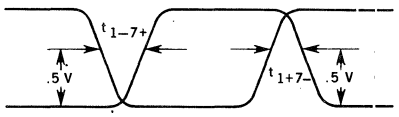
Typical Resistors

$R_1 = 1.5\,k$

$R_2 = 3.6\,k$

SWITCHING TIME TEST CIRCUIT





Test No.	Test	Note	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	MIN.	MAX.
1	I_1		V_{IN}	V_{BOT}	GND	GND	GND			V_{CC}		I_{IN}
2	I_2		V_{BOT}	V_{IN}	GND	GND	GND			V_{CC}		I_{IN}
3	I_3		GND	GND	V_{IN}	GND	V_{BOT}			V_{CC}		I_{IN}
4	I_5		GND	GND	V_{BOT}	GND	V_{IN}			V_{CC}		I_{IN}
5	I_7		V_{OFF}	V_{OFF}	V_{BOT}	GND	GND		V_{IN}	V_{CC}	I_{AM}	I_{AM}
6	I_6		GND	V_{BOT}	V_{OFF}	GND	V_{OFF}	V_{IN}		V_{CC}	I_{AM}	I_{AM}
7	V_7		V_{ON}	GND	GND	GND	GND			V_{CC}		V_{OUT}
8	V_7		GND	V_{ON}	GND	GND	GND			V_{CC}		V_{OUT}
9	V_6		GND	GND	V_{ON}	GND	GND			V_{CC}		V_{OUT}
10	V_6		GND	GND	GND	GND	V_{ON}			V_{CC}		V_{OUT}
11	V_6		GND	GND	V_{IN}	GND	GND			V_{CC}		V_{CE}
12	V_6		GND	GND	GND	GND	V_{IN}			V_{CC}		V_{CE}
13	V_7		V_{IN}	GND	GND	GND	GND			V_{CC}		V_{CE}
14	V_7		GND	V_{IN}	GND	GND	GND			V_{CC}		V_{CE}
15	I_8		GND	GND	GND	GND	GND			V_{CC}		I_L
16	t_{1-7+}		Pulse in	GND	GND	GND	GND		Pulse out	V_{CC}		40 nsec
17	t_{1+7-}		Pulse in	GND	GND	GND	GND		Pulse out	V_{CC}		50 nsec

9911 LOW POWER RTμL GATE

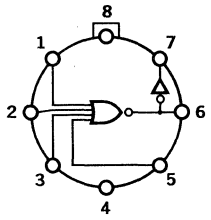
THE LOW POWER RTμL GATE MAY BE USED AS AN **OR** GATE BY APPLYING TRUE INPUTS; THE PIN 7 OUTPUT IS THEN THE TRUE **OR** FUNCTION OF THE INPUTS, AND THE PIN 6 OUTPUT IS THE INVERSE, OR **NOR.**

AVERAGE POWER DISSIPATION (25°C)

4 mW

LOGIC SYMBOL AND FUNCTIONS

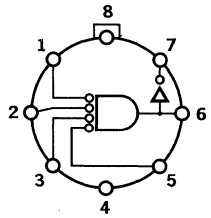
POSITIVE LOGIC



$7 = 1+2+3+5$

$6 = \overline{1+2+3+5}$

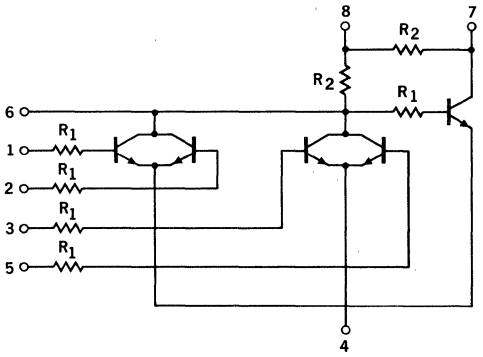
NEGATIVE LOGIC



$7 = 1 \cdot 2 \cdot 3 \cdot 5$

$6 = \overline{1 \cdot 2 \cdot 3 \cdot 5}$

CIRCUIT DIAGRAM

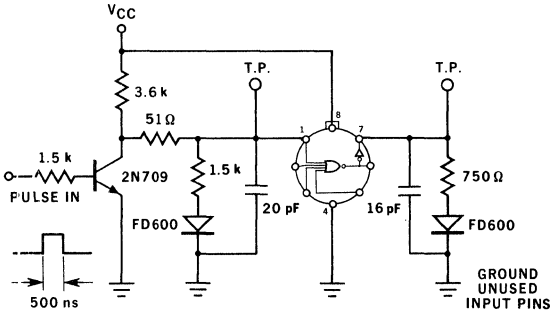


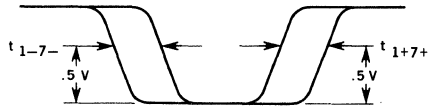
Typical Resistors

$R_1 = 1.5\,k\Omega$

$R_2 = 3.6\,k\Omega$

SWITCHING TIME TEST CIRCUIT





Test No.	Test	Note	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	MIN.	MAX.
1	I_1		V_{IN}	V_{BOT}	V_{BOT}	GND	V_{BOT}			V_{CC}		I_{IN}
2	I_2		V_{BOT}	V_{IN}	V_{BOT}	GND	V_{BOT}			V_{CC}		I_{IN}
3	I_3		V_{BOT}	V_{BOT}	V_{IN}	GND	V_{BOT}			V_{CC}		I_{IN}
4	I_5		V_{BOT}	V_{BOT}	V_{BOT}	GND	V_{IN}			V_{CC}		I_{IN}
5	I_6		V_{OFF}	V_{OFF}	V_{OFF}	GND	V_{OFF}	V_{IN}		V_{CC}	I_{A3}	
6	I_7		GND	GND	GND	GND	GND	V_{OFF}	V_{IN}	V_{CC}	I_{A4}	I_{AM}
7	V_6		V_{ON}	GND	GND	GND	GND			V_{CC}		V_{OUT}
8	V_6		GND	V_{ON}	GND	GND	GND			V_{CC}		V_{OUT}
9	V_6		GND	GND	V_{ON}	GND	GND			V_{CC}		V_{OUT}
10	V_6		GND	GND	GND	GND	V_{ON}			V_{CC}		V_{OUT}
11	V_6		V_{IN}	GND	GND	GND	GND			V_{CC}		V_{CE}
12	V_6		GND	V_{IN}	GND	GND	GND			V_{CC}		V_{CE}
13	V_6		GND	GND	V_{IN}	GND	GND			V_{CC}		V_{CE}
14	V_6		GND	GND	GND	GND	V_{IN}			V_{CC}		V_{CE}
15	V_7		GND	GND	GND	GND	GND	V_{ON}		V_{CC}		V_{OUT}
16	V_7		GND	GND	GND	GND	GND	V_{IN}		V_{CC}		V_{CE}
17	I_8		GND	GND	GND	GND	GND			V_{LL}		I_L
18	t_{1-7-}		Pulse in	GND	GND	GND	GND		Pulse out	V_{CC}		70 ns
19	t_{1+7+}		Pulse in	GND	GND	GND	GND		Pulse out	V_{CC}		90 ns

9912 LOW POWER RTμL HALF ADDER

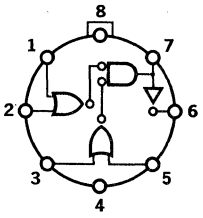
THE LOW POWER RTμL HALF-ADDER IS A MULTI-PURPOSE COMBINATION OF THREE BASIC **RTL** CIRCUITS. THE CONFIGURATION IS WELL SUITED AS A COMPLETE HALF-ADDER, AN EXCLUSIVE **OR** GATE, OR ANY OTHER SIMILAR LOGIC CONSTRUCTION.

AVERAGE POWER DISSIPATION (25°C)

8 mW

LOGIC SYMBOL AND FUNCTIONS

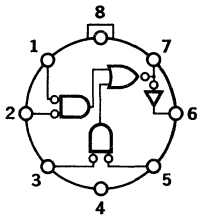
POSITIVE LOGIC



$7 = (1+2)\,(3+5)$

$6 = \bar{1}\cdot\bar{2}+\bar{3}\cdot\bar{5}$

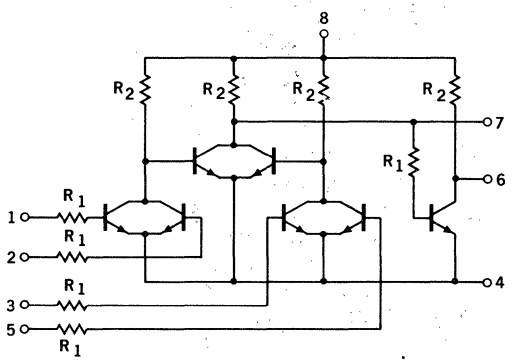
NEGATIVE LOGIC



$7 = 1\cdot2+3\cdot5$

$6 = (\bar{1}+\bar{2})\,(\bar{3}+\bar{5})$

CIRCUIT DIAGRAM

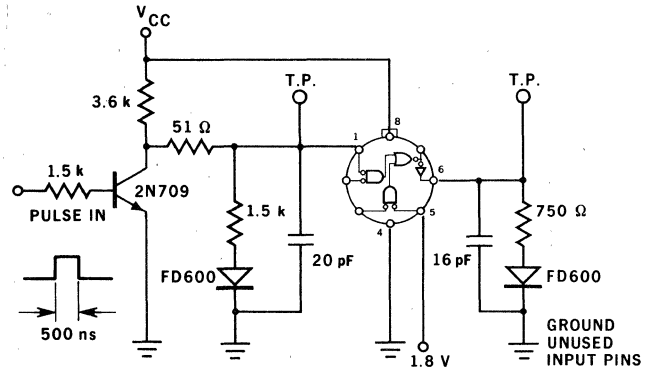


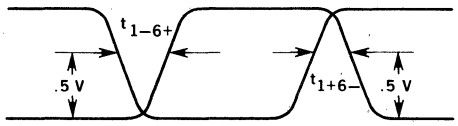
Typical Resistors

$R_1 = 1.5\,k\Omega$

$R_2 = 3.6\,k\Omega$

SWITCHING TIME TEST CIRCUIT





Test No.	Test	Notes	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Min.	MAX.
1	I_1		V_{IN}	V_{BOT}	GND	GND	GND			V_{CC}		I_{IN}
2	I_2		V_{BOT}	V_{IN}	GND	GND	GND			V_{CC}		I_{IN}
3	I_3		GND	GND	V_{IN}	GND	V_{BOT}			V_{CC}		I_{IN}
4	I_5		GND	GND	V_{BOT}	GND	V_{IN}			V_{CC}		I_{IN}
5	I_7		V_{ON}	GND	V_{ON}	GND	GND		V_{IN}	V_{CC}	I_{A3}	
6	I_7		GND	V_{ON}	GND	GND	V_{ON}		V_{IN}	V_{CC}	I_{A3}	
7	I_6		GND	GND	GND	GND	GND	V_{IN}		V_{CC}	I_{A4}	
8	V_6		V_{BOT}	V_{BOT}	V_{BOT}	GND	V_{BOT}		V_{ON}	V_{CC}		V_{OUT}
9	V_6		V_{BOT}	V_{BOT}	V_{BOT}	GND	V_{BOT}		V_{IN}	V_{CC}		V_{CE}
10	V_7		V_{OFF}	V_{OFF}	V_{BOT}	GND	V_{BOT}			V_{CC}		V_{CE}
11	V_7		V_{BOT}	V_{BOT}	V_{OFF}	GND	V_{OFF}			V_{CC}		V_{CE}
12	I_8		GND	GND	GND	GND	GND			V_{LL}		I_L
13	T_{1+6-}		Pulse in	GND	GND	GND	V_{BOT}	Pulse out		V_{CC}		100 ns
14	T_{1-6+}		Pulse in	GND	GND	GND	V_{BOT}	Pulse out		V_{CC}		80 ns

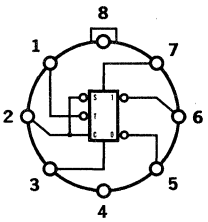
9913 LOW POWER RTμL TYPE D FLIP-FLOP

THE LOW POWER RTμL TYPE D FLIP-FLOP IS A COMPLETE, GENERAL PURPOSE STORAGE ELEMENT. THE STATE OF INPUT 2 IS STORED WHEN INPUT 1 CHANGES FROM HIGH TO LOW. A SUBSEQUENT CHANGE OF INPUT 2 WHILE INPUT 1 IS LOW HAS NO EFFECT. THE 9913 FLIP-FLOP HAS APPLICATION IN SHIFT REGISTERS, COUNTERS, AND CONTROL CIRCUITRY.

AVERAGE POWER DISSIPATION (25°C)

12 mW

LOGIC SYMBOL AND FUNCTIONS



DIRECT INPUTS[1]

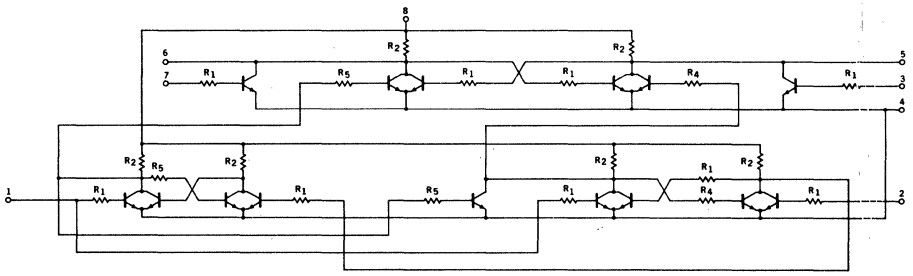
3	7	6	5
L	L	NC	NC[2]
L	H	L	H
H	L	H	L
H	H	L	L

GATED INPUT[3]

t = n	t = n + 1
2	6	5
H	H	L
L	L	H

1. Pin 1 must be high
2. NC = no change
3. Pins 3 and 7 must be low

CIRCUIT DIAGRAM

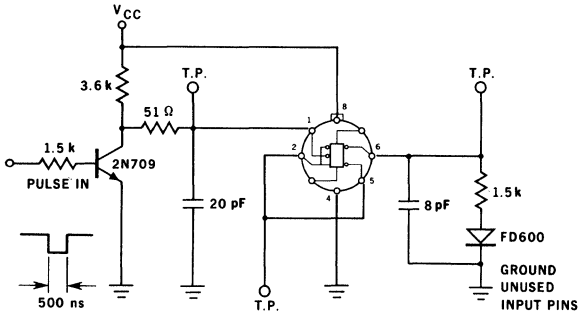


Typical Resistors $R_1 = 1.5k\Omega$ $R_4 = 180\Omega$
$R_2 = 3.6k\Omega$ $R_5 = 480\Omega$

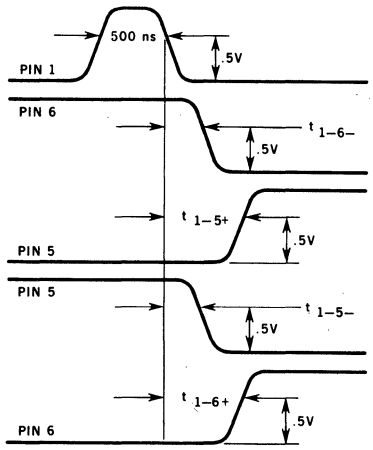
Test No.	Test	Note	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	MIN.	MAX.
1	V_5		V_{BOT}	GND	V_{ON}	GND			V_{BOT}	V_{CC}		V_{OUT}
2	V_6		V_{BOT}	GND	V_{BOT}	GND			V_{ON}	V_{CC}		V_{OUT}
3	V_5		V_{BOT}	GND	GND	GND		V_{ON}	GND	V_{CC}		V_{OUT}
4	V_6		V_{BOT}	GND	GND	GND	V_{ON}		GND	V_{CC}		V_{OUT}
5	V_5		V_{BOT}	GND	V_{IN}	GND			V_{BOT}	V_{CC}		V_{CE}
6	V_6		V_{BOT}	GND	V_{BOT}	GND			V_{IN}	V_{CC}		V_{CE}
7	V_5		V_{BOT}	GND	GND	GND		V_{IN}	GND	V_{CC}		V_{CE}
8	V_6		V_{BOT}	GND	GND	GND	V_{IN}		GND	V_{CC}		V_{CE}
9	I_1		V_{IN}	GND	GND	GND			GND	V_{CC}		1.8 I_{IN}
10	I_1		V_{IN}	V_{BOT}	GND	GND			GND	V_{CC}		1.8 I_{IN}
11	I_5		V_{ON}	V_{BOT}	V_{OFF}	GND	V_{IN}		V_{BOT}	V_{CC}	I_{A3}	
12	I_6		V_{ON}	GND	V_{BOT}	GND		V_{IN}	V_{OFF}	V_{CC}	I_{A3}	
13	I_5	1	V_{OFF}	GND	V_{OFF}	GND	V_{IN}		V_{BOT}	V_{CC}	I_{A3}	
14	I_6	1	V_{OFF}	V_{ON}	V_{BOT}	GND		V_{IN}	V_{OFF}	V_{CC}	I_{A3}	
15	I_2	1	V_{OFF}	V_{IN}	GND	GND			GND	V_{CC}		I_{IN}
16	I_3	1	V_{OFF}	V_{BOT}	V_{IN}	GND			GND	V_{CC}		I_{IN}
17	I_7	1	V_{OFF}	GND	GND	GND			V_{IN}	V_{CC}		I_{IN}
18	V_5	1	V_{OFF}	V_{ON}	GND	GND			V_{BOT}	V_{CC}		V_{CE}
19	V_6	1	V_{OFF}	V_{OFF}	V_{BOT}	GND			GND	V_{CC}		V_{CE}
20	I_8		GND	GND	GND	GND			GND	V_{LL}		I_L
21	t_{1-6-}		Pulse In	Tie to Pin 5	GND	GND		Pulse Out	GND	V_{CC}		80 ns
22	t_{1-6+}		Pulse In	Tie to Pin 5	GND	GND		Pulse Out	GND	V_{CC}		120 ns
23	t_{1-5-}		Pulse In	Tie to Pin 5	GND	GND	Pulse Out		GND	V_{CC}		80 ns
24	t_{1-5+}		Pulse In	Tie to Pin 5	GND	GND	Pulse Out		GND	V_{CC}		120 ns
25	t_{2+1-}		Pulse 1 In	Pulse 2 In	GND	GND		Pulse Out	GND	V_{CC}	60 ns	
26	t_{1-2-}		Pulse 1 In	Pulse 2 In	GND	GND		Pulse Out	GND	V_{CC}	30 ns	
27	t_{2-1-}		Pulse 1 In	Pulse 2 In	GND	GND		Pulse Out	GND	V_{CC}	60 ns	
28	t_{1-2+}		Pulse 1 In	Pulse 2 In	GND	GND		Pulse Out	GND	V_{CC}	30 ns	

Note 1: Voltage applied to Pin 1 changes from V_{RL} to specified value prior to making measurements.

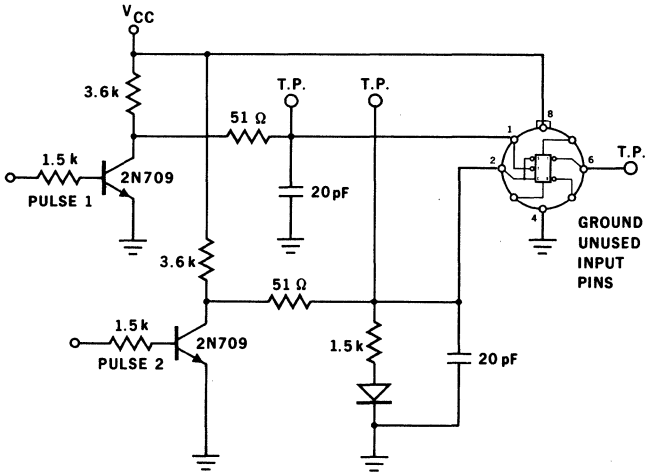
CIRCUIT FOR MEASURING T_{I-6+}, T_{I-6-}, T_{I-5+}, T_{I-5-}



PROPAGATION DELAY

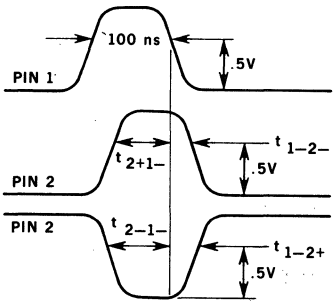


CIRCUIT FOR MEASURING MINIMUM INPUT PULSE WIDTH

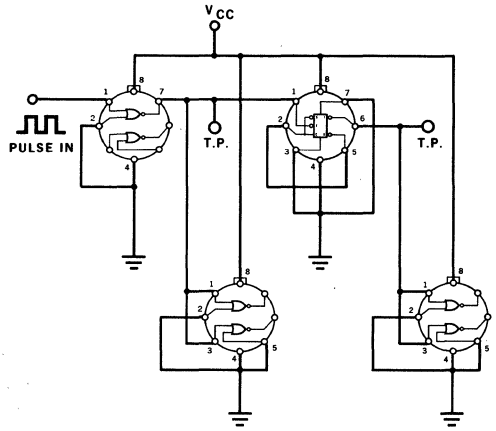


VARIABLE DELAY BETWEEN PULSE 1 AND PULSE 2

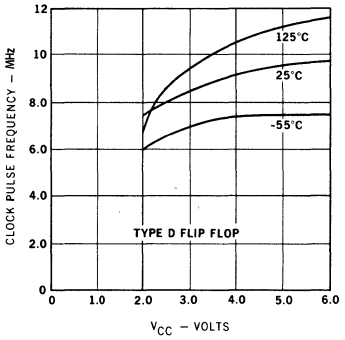
MINIMUM PULSE WIDTH

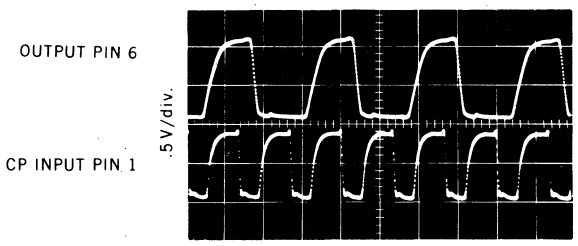


CONNECTED AS BINARY COUNTER



TYPICAL OPERATING CLOCK PULSE FREQUENCY VERSUS V_{CC}





9921 LOW POWER RTμL GATE EXPANDER

THE LOW POWER RTμL GATE EXPANDER IS A DOUBLE GATE WITHOUT THE NODE RESISTORS. ITS OUTPUT TERMINALS MAY BE CONNECTED IN PARALLEL TO THOSE OF A DUAL GATE OR A GATE TO INCREASE THE FAN-IN CAPABILITY OF THE CIRCUITS.

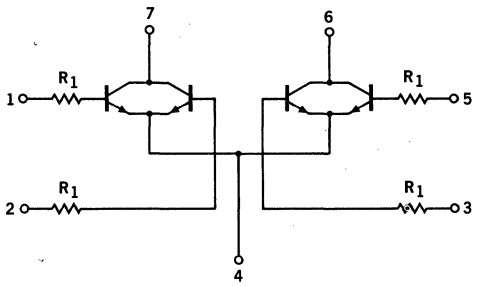
WHEN A DUAL GATE OR A GATE IS USED WITH THE EXPANDER, THE FOLLOWING RULES APPLY.

1) Pin 8 of the Expander must be connected to V_{CC}
2) The input load factor of the expanded gate is 1.33
3) The output drive factor of the expanded gate is decreased by .5 load for every node added.

AVERAGE POWER DISSIPATION (25°C)

No Power Flowing

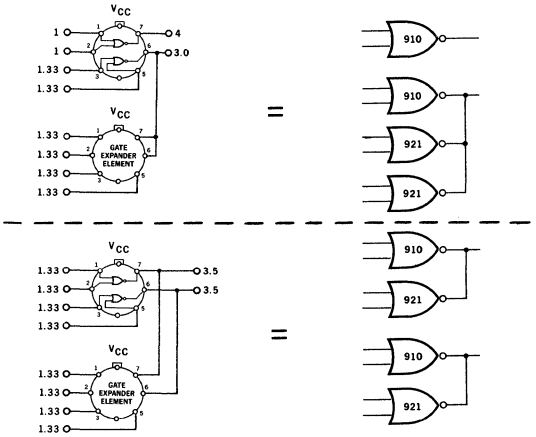
CIRCUIT DIAGRAM



Typical Resistor

$R_I = 1.5k\Omega$

DIAGRAM FOR USE OF GATE EXPANDER



Example of loading rules and logic symbols

Test No.	Test	Notes	TEST CONDITIONS								TEST LIMITS	
			Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	MIN.	MAX.
1	I_1		V_{IN}	V_{BOT}	GND	GND	GND		V_{RH}	V_{CC}		I_{IN}
2	I_2		V_{BOT}	V_{IN}	GND	GND	GND		V_{RH}	V_{CC}		I_{IN}
3	I_3		GND	GND	V_{IN}	GND	V_{BOT}	V_{RH}		V_{CC}		I_{IN}
4	I_5		GND	GND	V_{BOT}	GND	V_{IN}	V_{RH}		V_{CC}		I_{IN}
5	V_7		V_{ON}	GND	GND	GND	GND		V_{RL}	V_{CC}		V_{OUT}
6	V_7		GND	V_{ON}	GND	GND	GND		V_{RL}	V_{CC}		V_{OUT}
7	V_6		GND	GND	V_{ON}	GND	GND	V_{RL}		V_{CC}		V_{OUT}
8	V_6		GND	GND	GND	GND	V_{ON}	V_{RL}		V_{CC}		V_{OUT}
9	V_6		GND	GND	V_{IN}	GND	GND	V_{RL}		V_{CC}		V_{CE}
10	V_6		GND	GND	GND	GND	V_{IN}	V_{RL}		V_{CC}		V_{CE}
11	V_7		V_{IN}	GND	GND	GND	GND		V_{RL}	V_{CC}		V_{CE}
12	V_7		GND	V_{IN}	GND	GND	GND		V_{RL}	V_{CC}		V_{CE}
13	I_7		V_{OFF}	V_{OFF}	GND	GND	GND		V_{IN}	V_{CC}		I_{CEX}
14	I_6		GND	GND	V_{OFF}	GND	V_{OFF}	V_{IN}		V_{CC}		I_{CEX}
15	$I_{6,7,8}$		GND	GND	GND	GND	GND	V_{CC}	V_{CC}	V_{CC}		I_L

9926 JK FLIP-FLOP ELEMENT

TEMPERATURE RANGES —55°C TO +125°C (FULL RANGE)
0°C TO +100°C (MID RANGE)

FAIRCHILD PLANAR* EPITAXIAL MICROLOGIC® INTEGRATED CIRCUITS

JK FLIP-FLOP DESCRIPTION

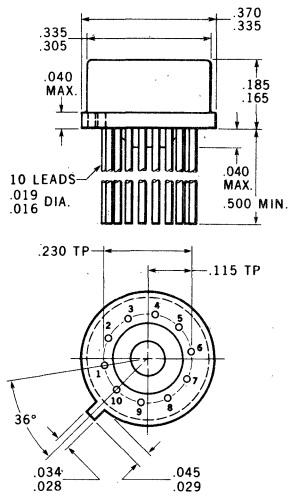
The Fairchild JK Flip-Flop is a complete, general purpose, storage element suitable for use in shift registers, counters or any type of control function.

The JK Flip-Flop differs from ordinary RS Flip-Flops in that no ambiguous output state can result from simultaneous one inputs. In this JK Flip-Flop simultaneous lows on both the set and clear inputs cause the output state to toggle (reverse). This feature enhances the operation of the JK Flip-Flop in binary counters, as no external feedback connections are required. The toggling action can also be used to advantage for minimizing the logic structure of control units.

The unique input triggering circuit permits the JK Flip-Flop to respond to negative clock pulse transition as short as 1 nanosecond or as long as 100 nanoseconds.

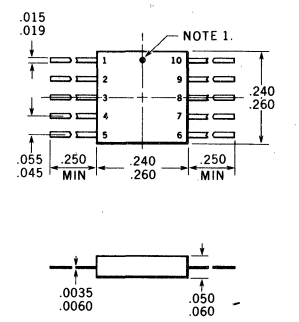
Asynchronous preset and preclear inputs are included for presetting counters, inserting parallel data in registers, and similar applications.

PHYSICAL DIMENSIONS
(In accordance with JEDEC TO—100)



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

CERPAK - FLAT PACKAGE
TOP VIEW



NOTE: 1. Alternate marking of dot in upper left hand corner is also acceptable.

POWER DISSIPATION (25°C) **TYPICAL** 56 mW

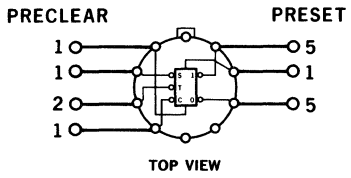
ABSOLUTE MAXIMUM RATINGS (25°C Ambient Temperature)

Maximum Voltage applied to pin 8	+12.0 Volts
Maximum Voltage applied to any input pin	±4.0 Volts
Storage Temperature	-65°C to +150°C
Power Dissipation	500 mW

OPERATING VOLTAGE RANGE

Collector Supply Voltage (V_{CC})	3.0 Volts ±10%

LOGIC SYMBOL AND LOAD FACTORS



TOP VIEW

SET (J) (2)	CLEAR (K) (4)	OUTPUT (9)
t = n		t = n + 1
H	H	X^n
H	L	H
L	H	L
L	L	$\overline{X^n}$

H is more positive than **L**.
X is the output state at time **n**.

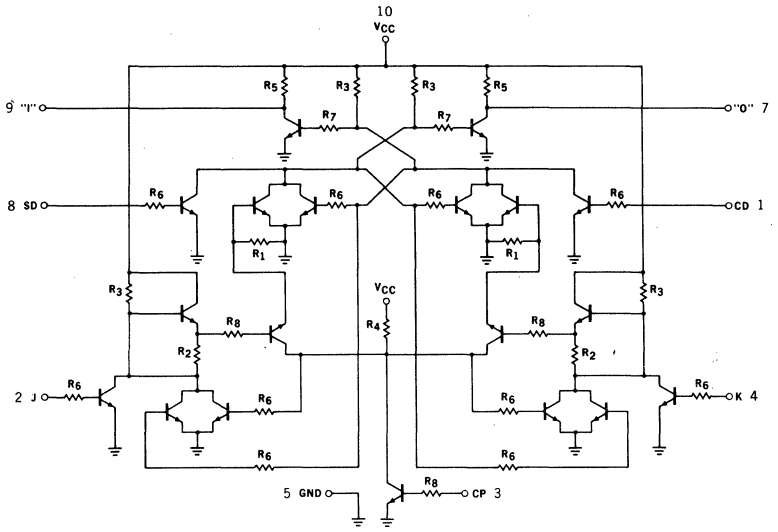
* Planar is a patented Fairchild process.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD MICROLOGIC® I.C. 9926 JK FLIP-FLOP

JK FLIP-FLOP SCHEMATIC DIAGRAM



TYPICAL RESISTOR VALUES

$R_1 = 3K\Omega$	$R_5 = 640\Omega$
$R_2 = 1K\Omega$	$R_6 = 600\Omega$
$R_3 = 900\Omega$	$R_7 = 550\Omega$
$R_4 = 700\Omega$	$R_8 = 300\Omega$

Pin configuration for TO-100, cerpak and flatpack are identical.

SWITCHING CHARACTERISTICS (−55°C to +125°C, V_{CC} = 3 V)

Symbol	Characteristic		Minimum	Typical	Maximum
TOGGLING MODE (See Fig. A)					
	Clock Frequency		8 MHz	20	--
	Clock Pulse Duty Cycle at 8 MHz		25%		75%
	Capacitive Load Per Output	(Note 4)			Unlimited
SWITCHING MODE (See Fig. B)					
t_{3-}		(Note 1)	1 ns		200 ns
t_{3-9-} or t_{3-7-}	Lightly Loaded		25 ns	40 ns	50 ns
	Heavily Loaded			45 ns	90 ns
	Heavily Loaded (25°C)	(Note 2)			60 ns
t_{3-9+} or t_{3-7+}	Lightly Loaded		25 ns	35 ns	50 ns
	Heavily Loaded			60 ns	90 ns
	Heavily Loaded (25°C)	(Note 2)			60 ns
t_{2+3-} or t_{4+3-}	(Setup Time)			20 ns	50 ns
t_{2-3-} or t_{4-3-}	(Setup Time			5 ns	30 ns
t_{3-2-} or t_{3-4-}	(Release Time)	(Note 5)		-5 ns	+5 ns
t_{3-2+} or t_{3-4+}	(Release Time)	(Note 5)		-15 ns	0 ns
t_{1} or 8+, output -	Heavily Loaded			40 ns	90 ns
t_{1} or 8+, output+	Heavily Loaded	(Note 3)		30 ns	70 ns

NOTES:

(1) Subscripts Denote Respectively: Input Pin, Input Slope, Output Pin, output Slope.

(2) This test is made on all acceptance lots to 4% combined AQL.

(3) If preset or preclear input is high and steering is opposite to preset or preclear, on negative going CP Trigger, the low output will be pulsed high for up to 80 nsec.

(4) Large capacitive loading may limit time of response of output to which capacitance is applied, however, the Flip-Flop will regenerate with any loading.

(5) Release time is defined as the time that the J and K inputs must be maintained after the negative CP transition. Negative release time means the inputs can change momentarily before the CP transition.

FIG. A TOGGLE MODE TEST CIRCUIT

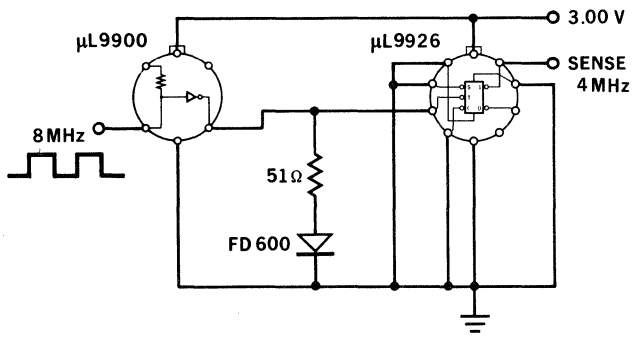
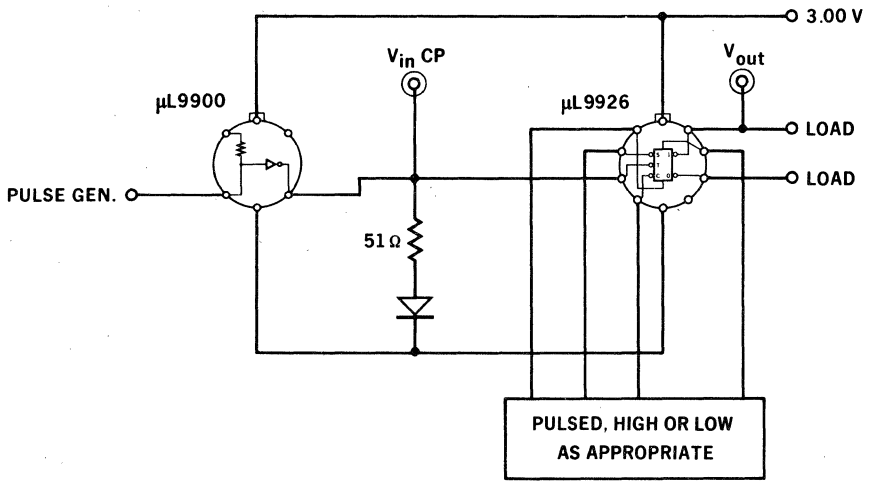
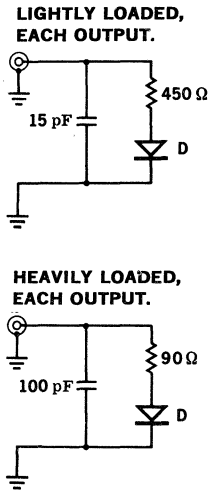


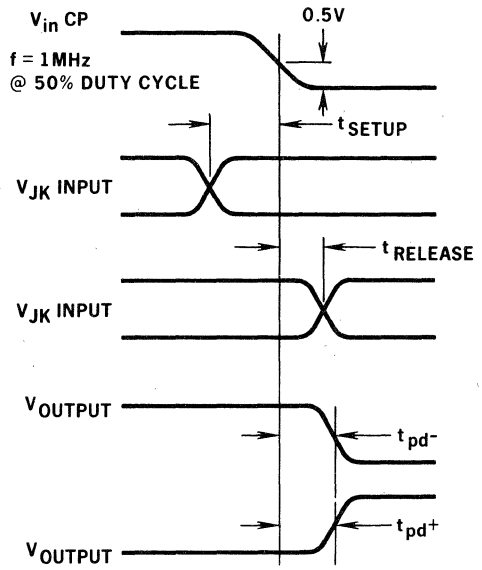
FIG. B SWITCHING MODE TEST CIRCUIT

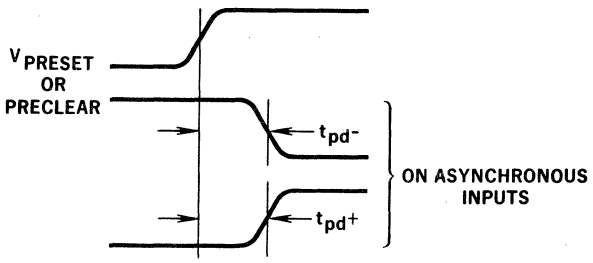




D = FD600 at temperature of element under test.

Capacitance values include jig and probe.





DC ACCEPTANCE TEST LIMITS FOR FULL-RANGE AND MID-RANGE ELEMENTS

Symbol	Test Tolerance	FULL RANGE -55°C ±2°C	FULL RANGE 25°C±2°C	FULL RANGE +125°C±2°C	MID RANGE 0°C ±2°C	MID RANGE 25°C±2°C	MID RANGE 100°C±2°C
V_{CC}	± .010 V	3.00 V	3.00 V	3.00 V	3.00 V	3.00 V	3.00 V
V_{IN}	± .002 V	1.014 V	.844 V	.674 V	.909 V	.844 V	.710 V
V_{ON}	± .002 V	1.014 V	.815 V	.674 V	.909 V	.844 V	.710 V
$V_{OD} = V_{BOT}$	± .010 V	1.50 V	1.50 V	1.50 V	1.50 V	1.50 V	1.50 V
V_{OFF}	± .002 V	.710 V	.565 V	.320 V	.574 V	.554 V	.370 V
V_{OUT}		.710 V	.300 V	.320 V	.574 V	.400 V	.370 V
V_{SAT}		.200 V	.210 V	.280 V	.290 V	.260 V	.340 V
I_{IN}		.495 mA	.435 mA	.470 mA	.504 mA	.450 mA	.450 mA
$2I_{IN}$		.990 mA	.870 mA	.940 mA	1.01 mA	.900 mA	.900 mA
I_A		2.47 mA	2.54 mA	2.35 mA	2.52 mA	2.38 mA	2.25 mA

DC ACCEPTANCE TEST CONDITIONS FOR FULL-RANGE AND MID-RANGE ELEMENTS

Test No.	Test Title	Units	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Test Limits Min.	Typ.	Max.
*1	I_1	mA	V_{IN}				GND					V_{CC}			I_{IN}
2	I_2	mA		V_{IN}			GND			V_{BOT}		V_{CC}			I_{IN}
*3	I_3	mA		V_{BOT}	V_{IN}	V_{BOT}	GND					V_{CC}			$2I_{IN}$
4	I_4	mA	V_{BOT}			V_{IN}	GND					V_{CC}			I_{IN}
5	I_8	mA					GND			V_{IN}		V_{CC}			I_{IN}
*6	I_9	mA	V_{ON}				GND			V_{BOT}	V_{ON}	V_{CC}	I_A		
7	I_7	mA	V_{BOT}				GND		V_{ON}	V_{ON}		V_{CC}	I_A		
*8	V_7	V	V_{ON}				GND			V_{OFF}		V_{CC}			V_{SAT}
9	V_9	V	V_{OFF}				GND			V_{ON}		V_{CC}			V_{SAT}
10	V_7	V		V_{ON}	⌐¯	V_{OFF}	GND			HI		V_{CC}			V_{SAT}
11	V_9	V	HI	V_{OFF}	⌐¯	V_{ON}	GND					V_{CC}			V_{SAT}
12	V_9	V		V_{ON}	⌐¯	V_{ON}	GND			HI		V_{CC}			V_{SAT}
13	V_7	V		V_{OFF}	⌐¯	V_{OFF}	GND			HI		V_{CC}			V_{SAT}
14	V_9	V	HI	V_{OFF}	⌐¯	V_{OFF}	GND					V_{CC}			V_{SAT}
15	V_7	V	HI	V_{ON}	⌐¯	V_{ON}	GND					V_{CC}			V_{SAT}

HI = A momentary application of V_{BOT} before the arrival of the negative going clock pulse.

NOTES:

(A) Purchasing information and Fairchild Assured Customer Test Programs are identical to latest issue Epitaxial μLogic Tentative Specifications.

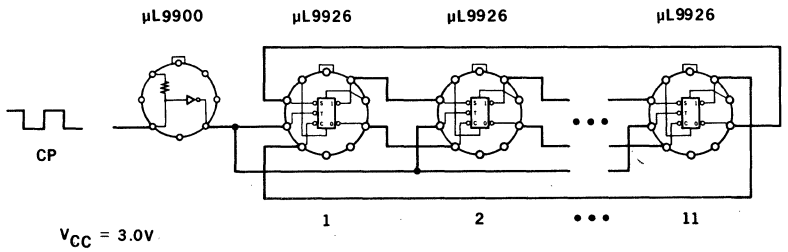
(B) JK926 is available in a TO-100 header with preclear removed and pin connections same as μL916; designated 974.

*FACT program end-point measurement parameter.

FAIRCHILD ASSURED COMPONENT TEST PROGRAM

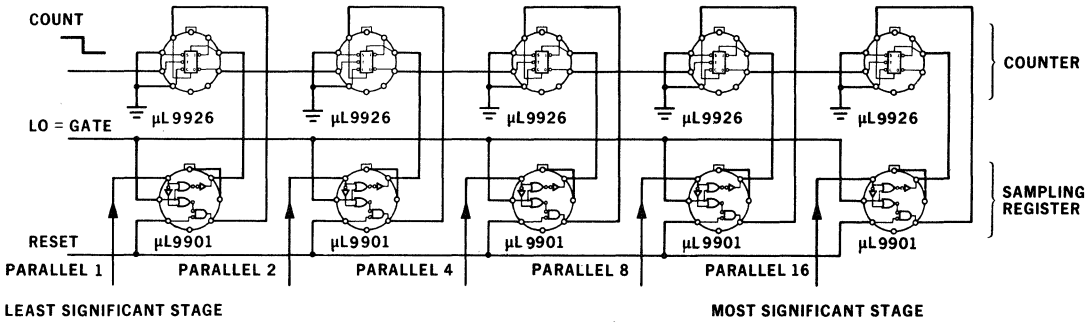
Test No.	25°C	-55 - +125°C	0 - +100°C
1	2a	3a	3a
2	2a	3a	3a
3	2a	3a	3a
4	2a	3a	3a
5	2a	3a	3a
6	2b	3b	3b
7	2b	3b	3b
8	2c	3c	3c
9	2c	3c	3c
10	4		
11	4		
12	4	For definitions refer to	
13	4	the latest FACT brochure.	
14	4		
15	4		

OPERATING LIFE CIRCUIT

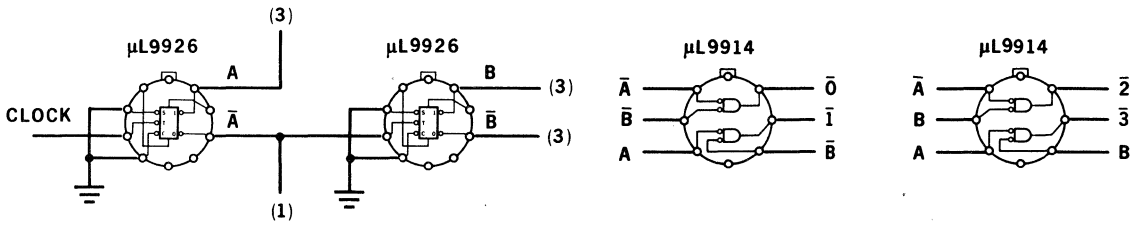


APPLICATIONS

BINARY COUNTER AND SAMPLING CONTROL



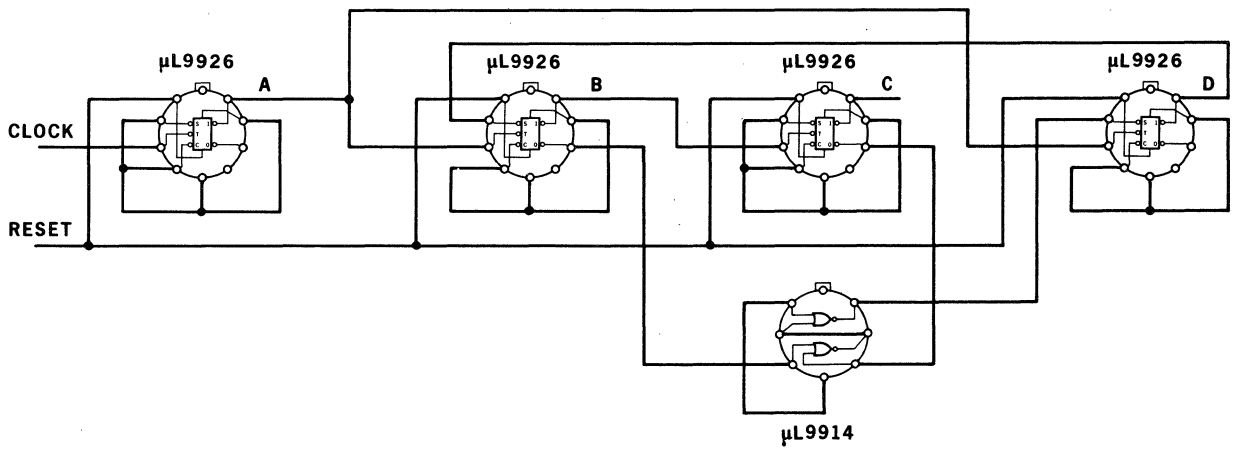
MODULO 4 COUNTER



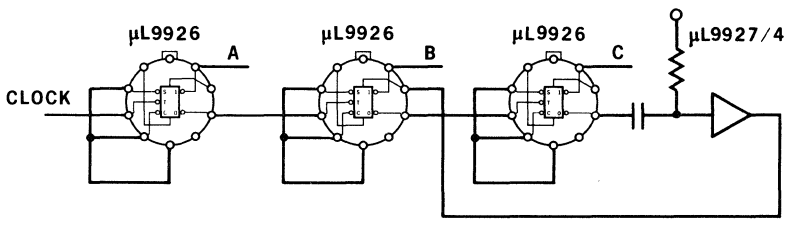
( ) INDICATES REMAINING FAN OUT

NEGATIVE LOGIC DECODE

1-2-4-8 MODULO 10, COUNT UP COUNTER (POSITIVE LOGIC)



MODULO 6 RIPPLE CARRY

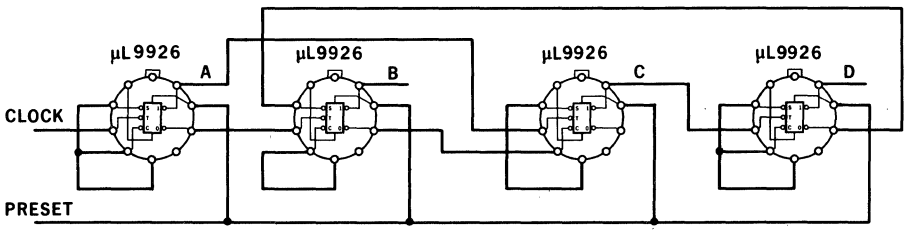


CODE

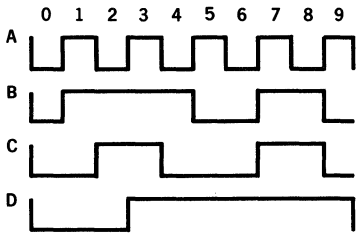
	A	B	C
0	0	1	0
1	1	1	0
2	0	0	1
3	1	0	1
4	0	1	1
5	1	1	1

APPLICATIONS

MODULO 10-MINIMUM HARDWARE

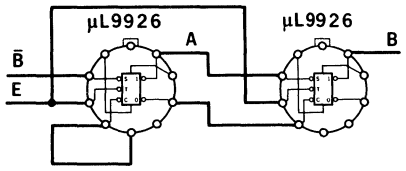


OUTPUT WAVEFORMS



MODULO 15 COUNTER (3x5)

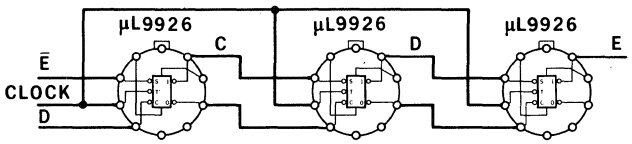
MODULO 3



CODE

	A	B
0	0	0
1	1	0
2	0	1

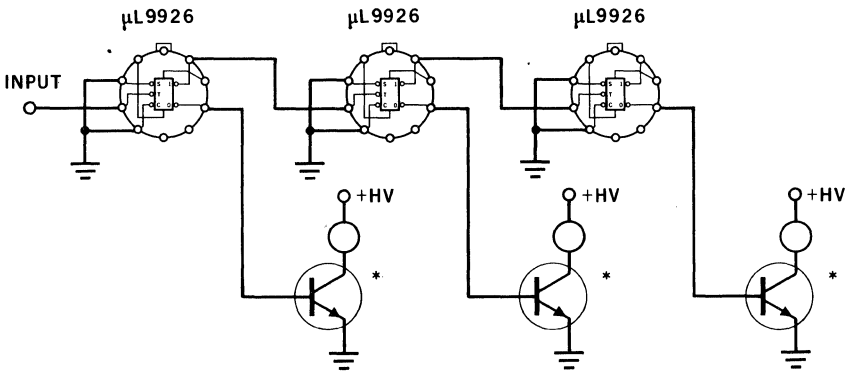
MODULO 5



CODE

	C	D	E
0	1	0	0
1	1	1	0
2	1	1	1
3	0	1	1
4	0	0	1

BINARY COUNTER, DIRECT READOUT



* 2N2368 INC AND RR COIL, HV ≤ 30VDC
2N1990 NEON AND NIXIE®, HV ≤ 110VDC

NIXIE® - REGISTERED TRADE MARK BURROUGHS CORPORATION.

PURCHASING INFORMATION

To order the 926, the following part numbers should be used to expedite handling.

UA99262BX

A is package designator

A = 3F for ¼ x ¼ Cerpak

A = 5F for Low Profile TO-5

B is operating temperature range designator

B = 1 −55°C to +125°C

B = 2 0°C to +100°C

B = 9 0°C to +70°C

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

μL927 QUAD INVERTER

INDUSTRIAL RTL MICROLOGIC® INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The Industrial RTL Microcircuit line, is a family of medium power and low power integrated building blocks. These elements are designed for a wide variety of commercial industrial equipment operating over a temperature range of +15°C to +55°C. By combining medium power and low power Micrologic® integrated circuits, high fan-out (>16), low power dissipation (<mW/Node), high speed (10 ns), and high noise immunity are possible. The loading chart shown below is guaranteed over the temperature range by a worst case specification.

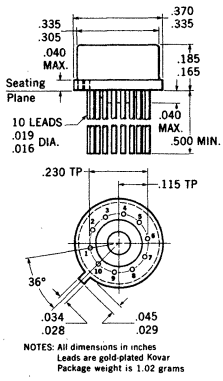
OPERATING VOLTAGE RANGE

V_{CC} - Collector Supply Voltage = 3.6 V ±10%

NOISE IMMUNITY	Typical	Worst Case
	300 mV	100 mV

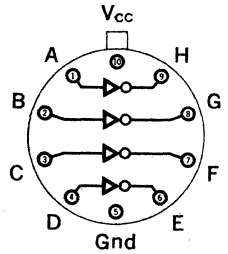
POWER DISSIPATION at 25°C, V_{CC} = 3.6 V = 20 mW/Node.

PHYSICAL DIMENSIONS



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.02 grams

QUAD INVERTER

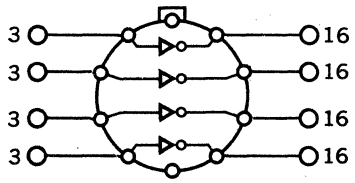


(TOP VIEW)

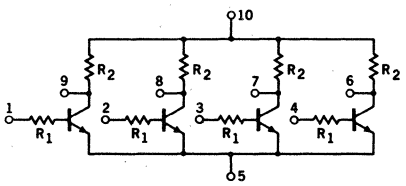
POSITIVE AND NEGATIVE LOGIC

$H = \overline{A}$
$G = \overline{B}$
$F = \overline{C}$
$E = \overline{D}$

LOADING CHART
[Note 1]



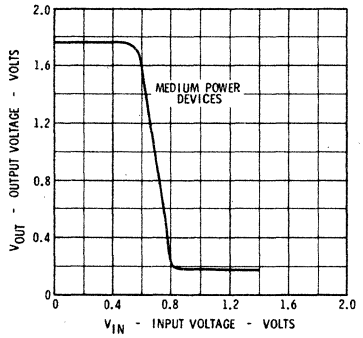
μL927 SCHEMATIC

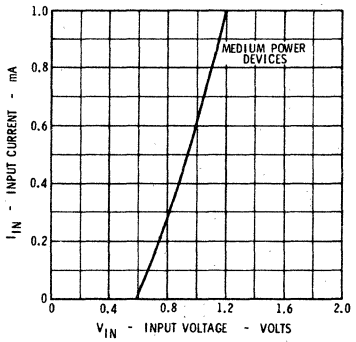


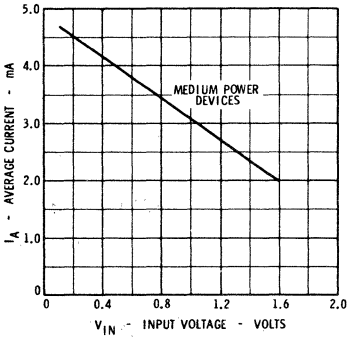
Typical Resistors

$R_1 = 450\,\Omega$
$R_2 = 650\,\Omega$

TYPICAL TRANSFER CHARACTERISTICS







Note:

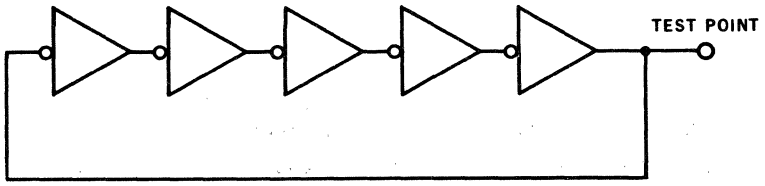
1) Valid for system operation over a temperature range of +15°C to +55°C, and V_{CC} = 3.6 V ±10%. This chart gives loading rules for intermixing of medium power and low power Micrologic® integrated circuits in a system.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

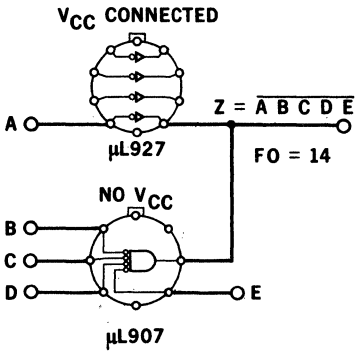
DESIGN INFORMATION

$T_{pd} = \frac{\text{PERIOD}}{2 \times 5}$ µL927 = 10 nsec

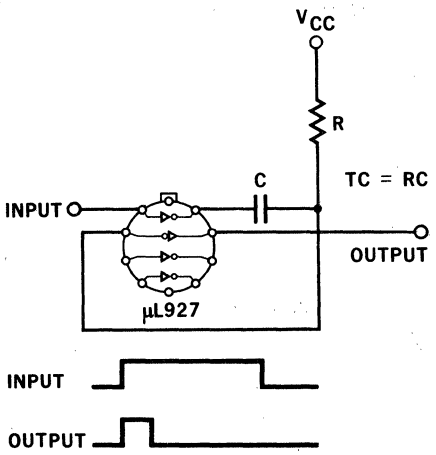


AVERAGE PROPAGATION DELAY
(Operating ring with 5 elements, at 25° C)

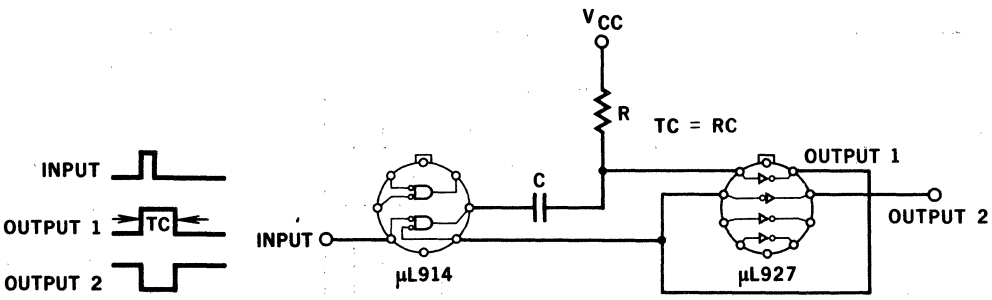
TYPICAL APPLICATIONS — NEGATIVE TRUE LOGIC



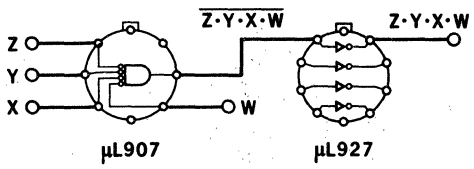
SUGGESTED INPUT
PARALLELING CONFIGURATION

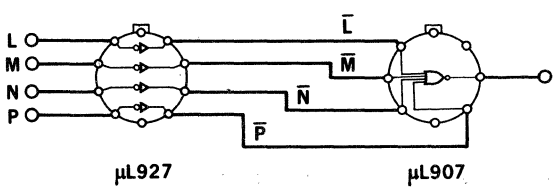


SINGLE SHOT
(Input longer than T C)



SINGLE SHOT
(Input narrower than T C)





L+M+N+P
(NEGATIVE TRUE LOGIC)

L·M·N·P
(POSITIVE TRUE LOGIC)

CTμL9952

DUAL 2-INPUT NOR GATE

COMPLEMENTARY TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

+15°C TO +55°C TEMPERATURE RANGE

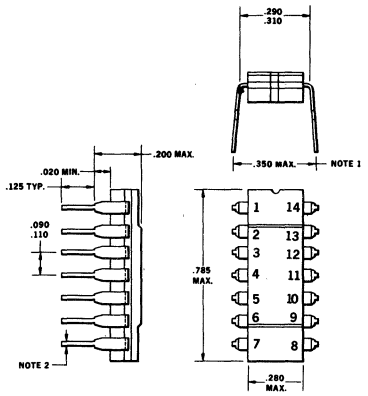
GENERAL DESCRIPTION–The CTμL 9952 Dual 2-Input Inverter Gate provides logic gating at its input and output terminals. Compatible with all other CTμL elements, the output can be tied to any other element to perform the wired OR function.

The 9952 may be used to set and restore the system logic levels; having a high noise immunity, it can drive and be driven by a number of cascaded CTμL AND-OR gates. The following data, stressing worst case conditions, plus 100% testing by Fairchild Semiconductor, will assure the designer of proper worst case performance in his own system.

The CTμL 9952 is designed for general purpose industrial and commercial usage where high speed logic is required. It is packaged in the versatile Dual-In-Line* package, which is a hermetically sealed ceramic package intended for low-cost insertion techniques.

TYPICAL DUAL IN-LINE* PACKAGE

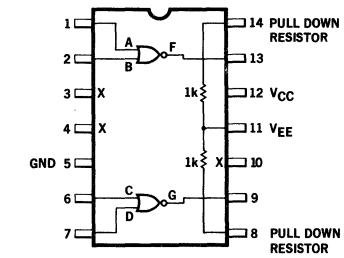
in accord with JEDEC (TO-116) outline



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

CONNECTION DIAGRAM

TOP VIEW



POSITIVE LOGIC $F = \overline{A+B}$, $G = \overline{C+D}$

NOTE: X = NOT CONNECTED

FEATURES

- **POWER SUPPLIES ARE +4.5 V ±10% AND −2.0 V ± 10%**
- **HIGH FAN-OUT CAPABILITY — 12**
- **TEMPERATURE RANGE — +15°C TO +55°C**
- **OPTIONAL PULLDOWN 1.0 k RESISTOR FOR OPTIMUM SPEED**
- **LOW POWER DISSIPATION**
- **LOW PROPAGATION DELAY — 7.0 ns TYPICAL**
- **LOGIC SWING OF 3.0 V**
- **HIGH NOISE IMMUNITY > 1.0 V AT FAN-OUT = 12**

PURCHASING INFORMATION

Use the ten-letter code U6A995279X for ordering purposes.

All units are marked CTμL-995279 and date code unless otherwise specified.

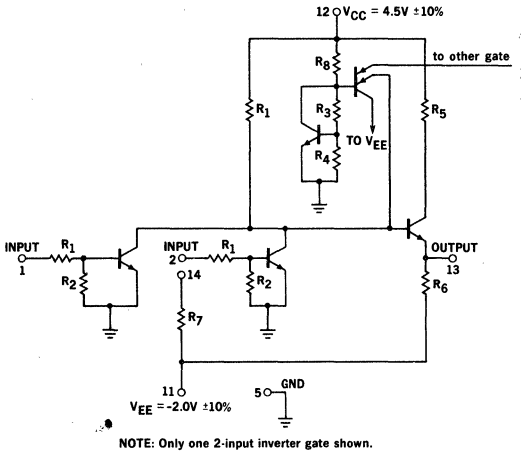
*Fairchild Patent Pending

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

CTμL-9952 COMPLEMENTARY TRANSISTOR MICROLOGIC® IC

SCHEMATIC DIAGRAM



NOTE: Only one 2-input inverter gate shown.

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

Maximum Current in or out of a pin	100 mA
Maximum Chip Temperature	+150°C
Maximum Power Dissipation	1.0 Watt
Maximum Voltage Applied to any Input Pin	10 Volts
Maximum Negative Voltage Applied to any Input Pin	−4.0 Volts
Maximum Voltage Applied to Output Pin	6.0 Volts

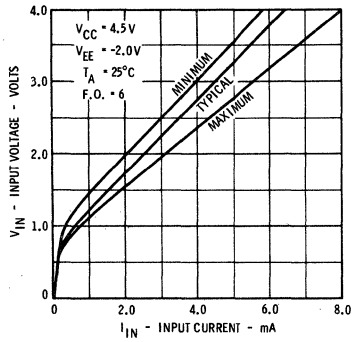
DC TESTS

TEST (at T_A = 25°C)	LIMITS				CONDITIONS			
	MIN.	TYP.	MAX.(1)	UNITS	V_{CC}	V_{EE}	LOAD TO V_{EE}	COMMENTS
Output ONE Level	2.35	2.50		Volts	4.05 V	−2.20 V	F.O.(2) = 12	Inputs to +0.8 V sequentially. Guarantees input low threshold >0.80 V; and output ONE level >2.35 V.
Output ZERO Level		−0.50	−0.36	Volt	4.95 V	−1.80 V	F.O. = 1	Inputs to 1.25 V sequentially. Guarantees input high threshold <1.25 V; output ZERO level <−0.36 V.
Output ONE Level		2.75	2.90	Volts	4.95 V	−1.80 V	F.O. = 1	Inputs to −0.70 V simultaneously. Guarantees output never more positive than 2.90 V.
Input Current	4.20	5.30	6.86	mA	4.05 V	−1.80 V	No load	Inputs to 3.5 V simultaneously. Guarantees input loading <1.5 AND gate loads.
Output Resistor	1.6 k	2.0 k	2.4 k	Ohms	4.05 V	−2.20 V	No load	Inputs to −0.7 V simultaneously. (Outputs to 3.5 V sequentially.) Guarantees output OR tie <1.0 AND-OR gate loads.
Input Pulldown Resistor	0.8 k	1.0 k	1.2 k	Ohms	4.05 V	−2.20 V	No load	Resistor to 3.50 V sequentially. Guarantees 1 k resistor available for input pulldown is within 20% of nominal value.
Output Falling Delay, t_{df}		6	12	ns	4.50 V	−2.00 V	F.O. = 12	See t_{PD} Test Circuit
Output Rising Delay, t_{dr}		8	14	ns	4.50 V	−2.00 V	F.O. = 12	See t_{PD} Test Circuit
Positive Supply Current	18.5	30	36.2	mA	4.95 V	−2.20 V	No load	Inputs to +3.50 V simultaneously. Tests internal resistors to be no more than ±20% from nominal.
Negative Supply Current	6.75	8	14.8	mA	4.95 V	−2.20 V	No load	Inputs to −0.70 V simultaneously. Test internal resistors to be no more than ±20% from nominal.

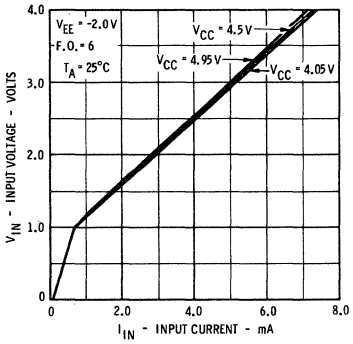
NOTES: (1) "Maximum" means "no more positive than"
(2) F.O. = Fan-Out: F.O. = 12 equivalent to 133 Ω to −2.20 V under worst case conditions.
F.O. = 1 equivalent to 2.4 kΩ to −1.80 V under worst case conditions.

INPUT CHARACTERISTICS

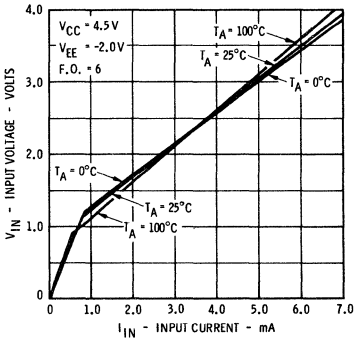
TOLERANCE VARIATION OF PARAMETERS



AS A FUNCTION OF COLLECTOR SUPPLY VOLTAGE

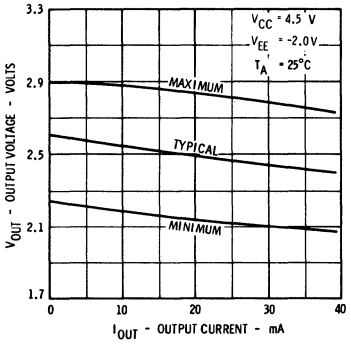


AS A FUNCTION OF TEMPERATURE

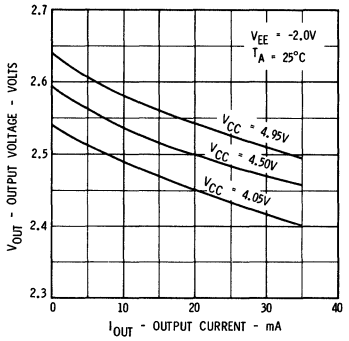


OUTPUT CHARACTERISTICS

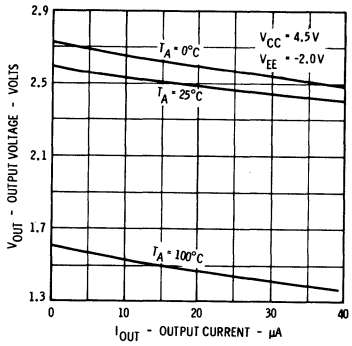
TOLERANCE VARIATION OF PARAMETERS



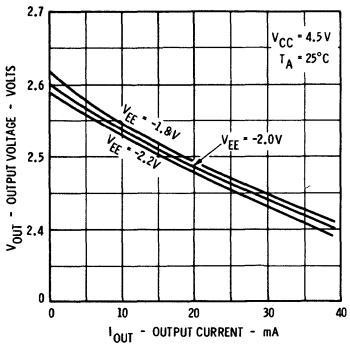
AS A FUNCTION OF COLLECTOR SUPPLY VOLTAGE



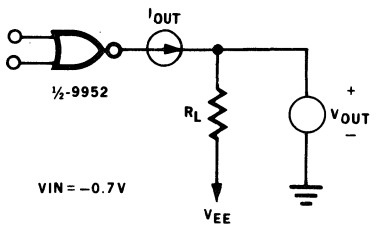
AS A FUNCTION OF TEMPERATURE



AS A FUNCTION OF NEGATIVE SUPPLY VOLTAGE

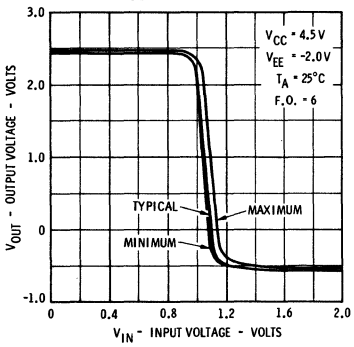


SCHEMATIC DIAGRAM

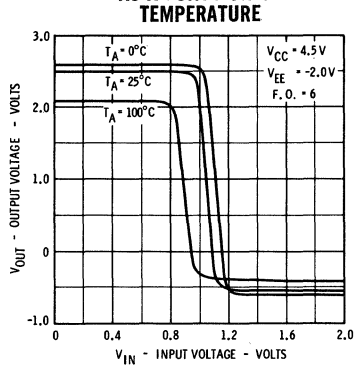


TRANSFER CHARACTERISTICS

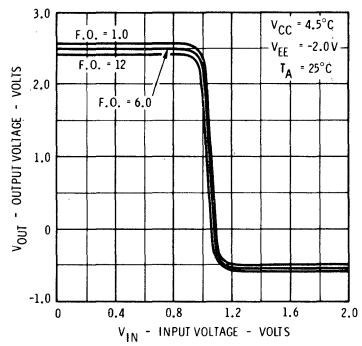
TOLERANCE VARIATION OF PARAMETERS



AS A FUNCTION OF TEMPERATURE

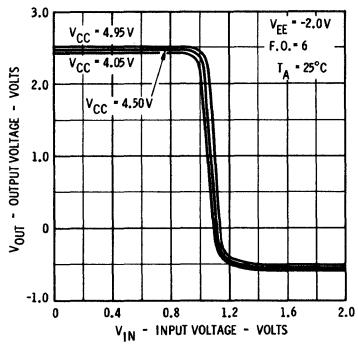


AS A FUNCTION OF FAN-OUT

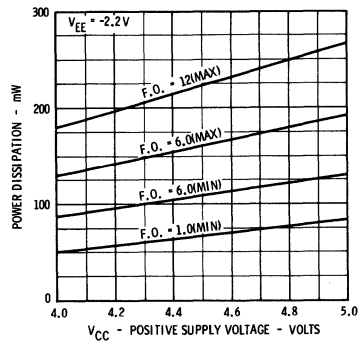


NOTE: Variation of V_{EE} does not alter transfer characteristics.

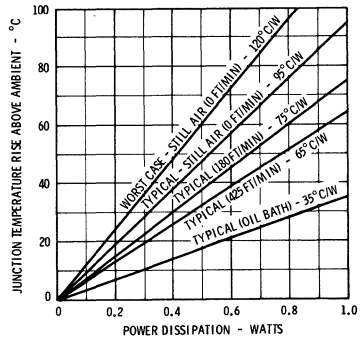
AS A FUNCTION OF POSITIVE SUPPLY VOLTAGE



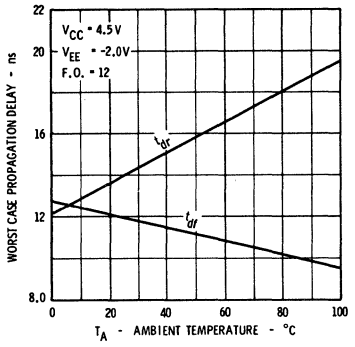
POWER DISSIPATION VERSUS POSITIVE SUPPLY VOLTAGE



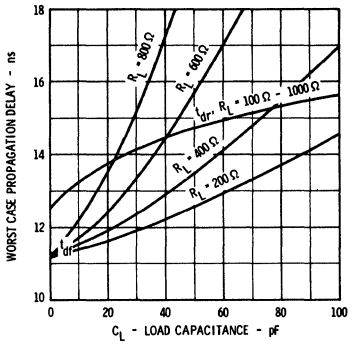
WORST CASE JUNCTION TEMPERATURE VERSUS POWER DISSIPATION



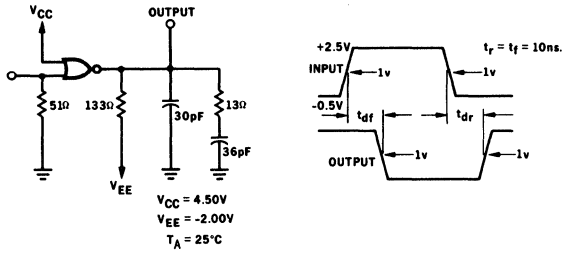
WORST CASE PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE



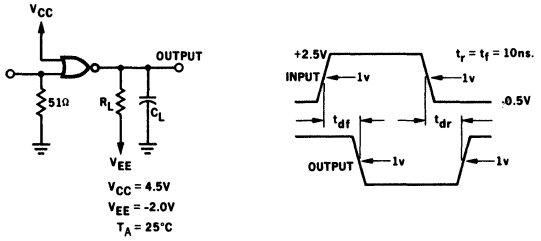
WORST CASE PROPAGATION DELAY VERSUS LOAD CAPACITANCE AS A FUNCTION OF LOAD RESISTANCE



t_{PD} TEST CIRCUIT



t_{PD} TEST CIRCUIT FOR ABOVE



APPLICATION INFORMATION

The electrical specification tests performed under the conditions set, emphasize the worst case results and should be considered as conservative limits. Throughout this data sheet, WORST CASE should be interpreted as using power supplies, internal resistors, transistor parameters and external loads having extreme loads chosen in a manner to guarantee proper operation under worst case conditions.

LOADING RULES: Each input to the CTμL 9952 represents 1.5 unit loads.
(One unit load is defined as an input to the CTμL AND-OR gate.)

a) Connecting the 1.0 kΩ pulldown resistor to the input adds two unit loads to the fan-in.

b) Connecting the 1.0 kΩ pulldown resistor to the output reduces the fan-out by two unit loads.

c) Each wired-OR connection reduces the fan-out by one.

PULLDOWN RESISTOR: Two pulldown 1.0 kΩ resistors are built into the package with one end tied to the negative power supply (V_{EE}). Connecting the 1.0 kΩ resistor to the CTμL 9952 input will improve the turn-off characteristics and speed up the output rising propagation delay. When the input of the CTμL 9952 is driven by four or more AND-OR gates, there is no advantage in connecting the 1.0 kΩ resistor to the same input. The pulldown resistor may also be connected to the CTμL 9952 output. This will improve the output falling propagation delay when low fan-out is used.

WIRED OR: A powerful feature of the CTμL 9952 inverter is that the output may be tied together with the output of any other element in the CTμL family to form the positive OR function at the tie point, thus achieving two logic functions without additional propagation delay.

INTERFACING: The CTμL 9952 inverter gate serves as an excellent interfacing link between external signals coming from other logic forms or peripheral equipment and the CTμL family.

NOISE IMMUNITY: The CTμL 9952, having excellent noise immunity under maximum loading and worst case conditions, is used primarily to restore logic levels degraded after passing through several CTμL AND-OR gates.

HIGH SPEED CONSIDERATIONS: The high-speed logic operation available using CTμL requires that care be exercised in packaging and interconnection techniques. Normally logic circuits using emitter followers as drivers have a tendency to oscillate when driven by high-speed pulse signals. Each CTμL 9952 includes a clamping network so designed that it reduces ringing at high-speed operation. These features eliminate the necessity for the use of strip lines or coaxial cables for all but the longest lines. However, care must still be exercised in the layout of printed circuit boards. Any one line over 12" in length tied to a gate output should be terminated in a 200 Ω resistor to ground. Such a 200 Ω resistor approximates the characteristic impedance of the back panel wiring and is considered equivalent to a fan-out of 4.

SHORT CIRCUIT PROTECTION: The CTμL 9952 inverter gate output is protected by a limiting resistor at the output and may sustain prolonged short circuit to ground with V_{CC} not greater than 5.0 V. Excessive destructive heat may develop when more than one output in a single package is short circuited to ground. In general, short circuiting the output should be avoided.

CTμL 9953-9955 • 9964-9966 • 9971-9972 AND-OR GATES

COMPLEMENTARY TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

+15°C TO +55°C TEMPERATURE RANGE

GENERAL DESCRIPTION — The Fairchild CTμL AND-OR gate is a PNP-NPN complementary logic circuit which provides the system designer with the basic tools for designing extremely fast, proven, low cost synchronous systems.

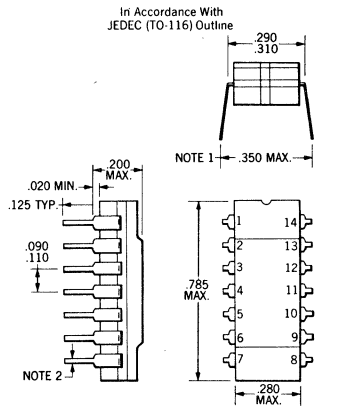
The following data, stressing worst case conditions, plus 100% testing by Fairchild for a minimum fanout of 11 and a maximum propagation delay of 4.5 nseconds at full fanout at 25°C, will assure the designer of proper worst case performance in his own system.

The AND-OR gate is basically a cascade connected PNP-NPN complementary non-saturating transistor pair. The output transistor is an emitter follower having virtually no threshold level. Therefore, there is no delay in output response due to input charging to threshold voltage, no stored charge to remove, negligible emitter-base transition charge and no collector-base transition capacity multiplication. Thus, typically 3 nseconds delays are obtainable at full fanout without the necessity of fast rise and fall time. This means conventional back panel wiring may be used with substantial reduction in inductive and capacitive noise usually generated by threshold circuits. The emitter follower low output impedance coupled with the high input impedance contributes to the large fanout and exceptional performance in the presence of stray capacitance.

CTμL circuits are packaged in the versatile JEDEC TO-116 DUAL-IN-LINE packages which are hermetically sealed ceramic units intended for low cost insertion techniques.

PHYSICAL DIMENSIONS

TYPICAL DUAL IN-LINE PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

FEATURES:

- **Power supplies are 4.5 V ±10% and −2.0 V ±10%.**
- **High fanout capability**
- **Temperature range +15°C to +55°C**
- **Low power dissipation**
- **Low propagation delay — 3.0 ns typical**
- **Logic swing of 3.0 V**

PURCHASING INFORMATION:

Description	Code	Marking
CTμL9953 — 2-2-3 Input AND-OR Gate (three gates in one package)	U6A995379X	CTμL95379
CTμL9954 — Dual 4-Input AND-OR Gate (two gates in one package)	U6A995479X	CTμL95479
CTμL9955 — Dual Output 8-Input AND-OR Gate	U6A995579X	CTμL95579
CTμL9964 — 3-3-1 Input AND-OR Gate (three gates in one package)	U6A996479X	CTμL96479
CTμL9965 — Quad 1-Input AND-OR Gate	U6A996579X	CTμL96579
CTμL9966 — Quad 2-Input AND-OR Gate (with three outputs)	U6A996679X	CTμL96679
CTμL9971 — Quad 2-Input AND-OR Gate (with two outputs)	U6A997179X	CTμL97179
CTμL9972 — Quad 2-Input AND-OR Gate (with three outputs, all pull down resistors omitted)	U6A997279X	CTμL97279

Use the ten letter code for ordering purposes.
All units are marked as above unless otherwise specified.

*Planar is a patented Fairchild process.

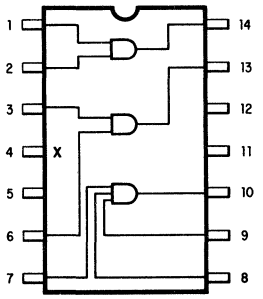
FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

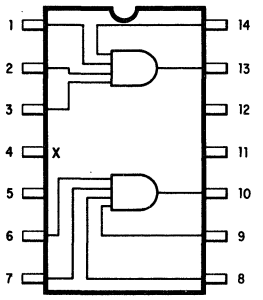
FAIRCHILD COMPLEMENTARY TRANSISTOR MICROLOGIC® IC

PIN CONFIGURATION AND LOGIC DIAGRAM
(TOP VIEW)

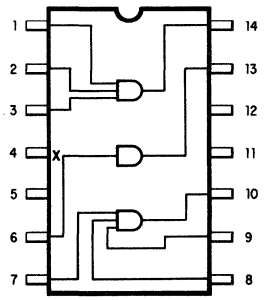
CTμL9953



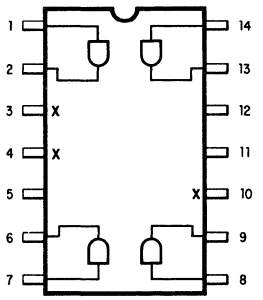
CTμL9954



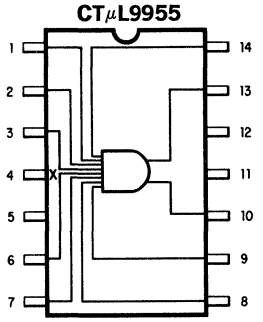
CTμL9964



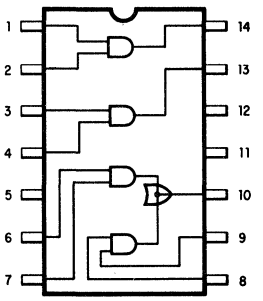
CTμL9965



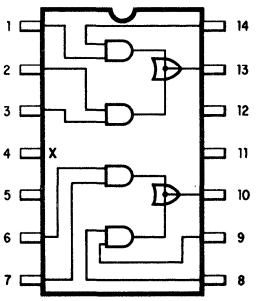
CTμL9955



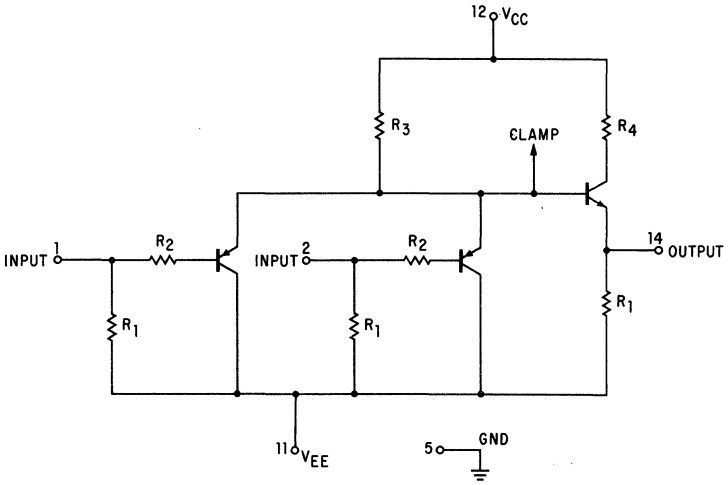
CTμL9966/9972[1]



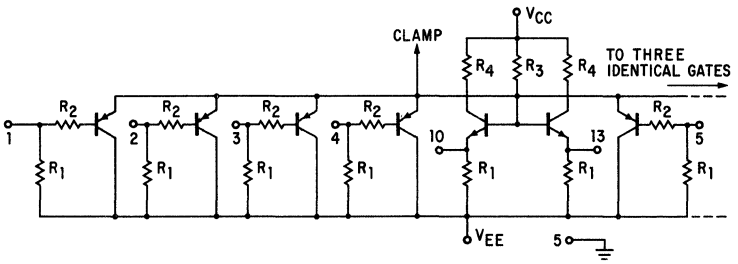
CTμL9971

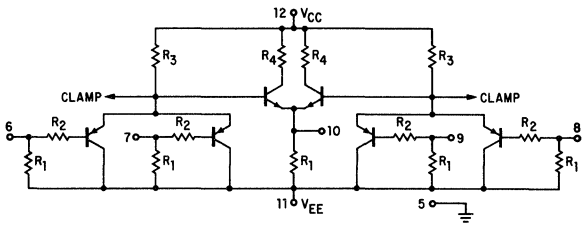


CIRCUIT DIAGRAM

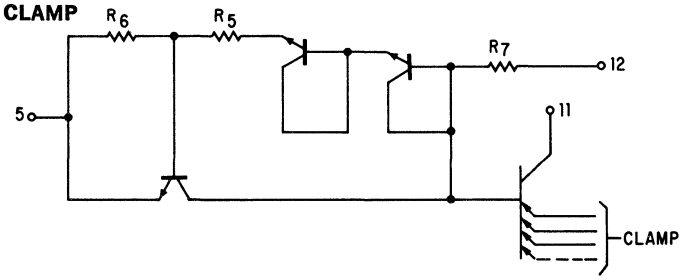


NOTE: Only one representative AND-OR gate shown.





NOTE: One AND/OR gate shown.



NOTES:
(1) R_1 deleted for CTμL 19972
X = Not connected.

Pin 12: $V_{CC} = 4.5\ V \pm 10\%$
Pin 11: $V_{EE} = -2.0\ V \pm 10\%$
Pin 5: Ground

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

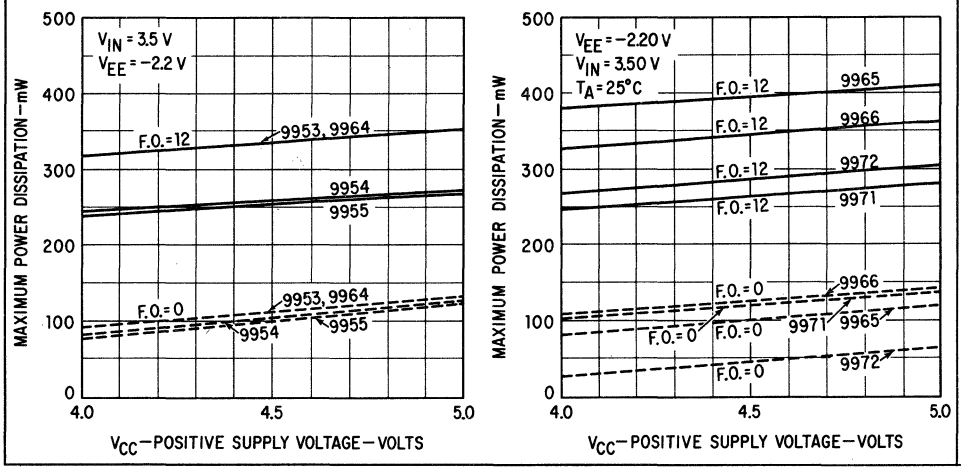
Maximum current in or out of a pin	100 mA	Maximum negative voltage applied to any input pin (output open)	−8.0 Volts
Maximum chip temperature	150°C		
Maximum power dissipation	1.0 Watt	Maximum voltage applied to output pin (input grounded)	5.0 Volts
Maximum voltage applied to any input pin	10 Volts		

D.C. TESTS

TESTS (at $T_A = 25°C$)	LIMITS				CONDITIONS			
	MIN.	TYP.	MAX.(1)	UNITS	V_{CC}	V_{EE}	LOAD TO V_{EE}	COMMENTS
ONE level offset		200	270	mV	4.05	−2.20	F.O. = 11(2)	Inputs sequentially to +2.25 V, other inputs to 3.5 V, pin 5 open. Worst case offset assuming ±10% supplies and W.C. parameters. Gates with lower input voltage will have smaller offsets; see fig. 12.
ZERO level offset		−120	−195	mV	4.95	−1.80	F.O. = 1	Worst case offset assuming ±10% supplies and min. fanout. Inputs sequentially to −0.36 V, other inputs to 3.50 V; pin 5 to GND.
Clamp level	2.10	2.30		Volts	4.05	−2.20	F.O. = 11	Inputs simultaneously at 3.5 V, pin 5 to GND. Tests minimum clamp level.
Clamp level		2.60	2.90	Volts	4.95	−1.80	No load	Inputs simultaneously to 3.5 V, pin 5 to GND. Tests max. possible clamp level to check existence of clamp.
Input resistors	1.6 k	2.0 k	2.4 k	Ω	4.05	−1.80	No load	Inputs to 3.5 V sequentially, other inputs to −0.7 V, sense input current. Tests min. R for max. loading, max. R for adequate turn-off and line termination.
Output resistors	1.6 k	2.0 k	2.4 k	Ω	4.05	−1.80	No load	Outputs to 3.5 V sequentially, inputs to −0.7 V, sense output current. Tests min. R for max. wired OR loading, max. R for adequate turn off.
Positive supply current, I_{PS}		I_{PS}	$I_{PS\ max}$	mA	4.95	−2.20	No load	Inputs to −0.7 V simultaneously.
Negative supply current, I_{NS}		$-I_{NS}$	$-I_{NS\ max}$	mA	4.95	−1.80	No load	Inputs to +3.5 V simultaneously.
Rising Propagation Delay, t_{dr}		3.5	4.5	ns	4.50	−2.00	F.O. = 12	See t_{pd} test circuit, page 6.
Falling Propagation Delay, t_{df}		3.0	4.0	ns	4.50	−2.00	F.O. = 12	See t_{pd} test circuit, page 6.

NOTES: (1) "Maximum" means "no more positive than"
(2) F.O. = Fan-Out: F.O. = 11 equivalent to 145 Ω to −2.20 V under worst case conditions
F.O. = 1 equivalent to 2.4 k to −1.80 V under worst case conditions

MAXIMUM POWER DISSIPATION VS. POSITIVE SUPPLY VOLTAGE

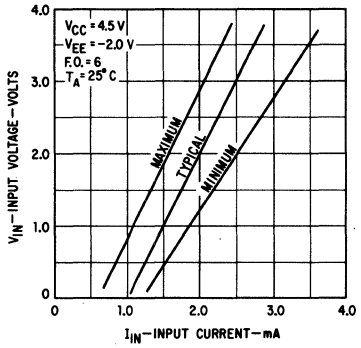


POSITIVE AND NEGATIVE CURRENT DRAIN

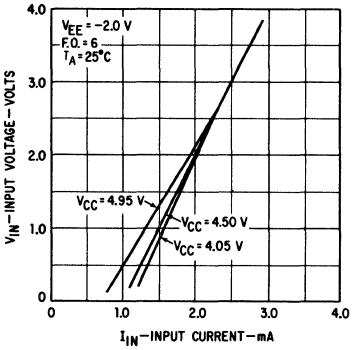
CTμL Element	$I_{PS\ typ}$	$I_{PS\ max}$	$I_{NS\ typ}$	$I_{NS\ max}$	UNITS
9953	22.0	27.7	33.0	41.4	mA
9954	16.5	20.5	33.0	39.6	mA
9955	11.5	14.3	30.0	37.1	mA
9964	22.0	27.7	33.0	41.4	mA
9965	28.0	34.9	29.0	36.0	mA
9966	27.0	33.9	38.0	47.5	mA
9971	26.0	32.9	36.0	44.6	mA
9972	12.0	20.0	5.0	10.0	mA

INPUT CHARACTERISTICS

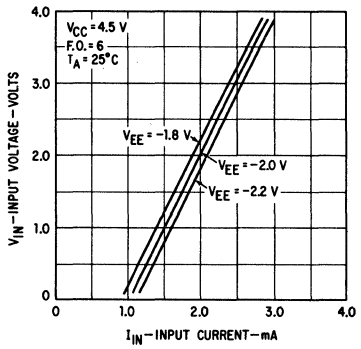
TOLERANCE VARIATION



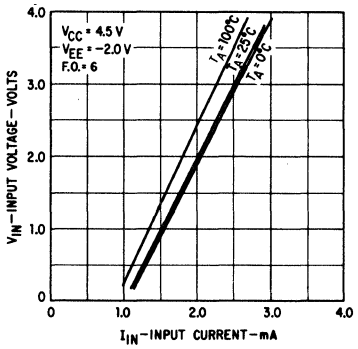
AS A FUNCTION OF V_{CC}



AS A FUNCTION OF V_{EE}

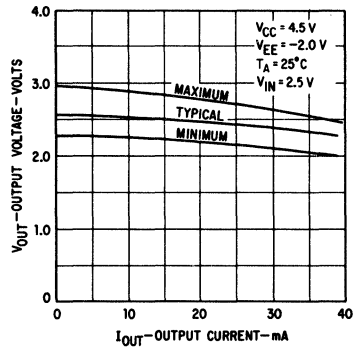


AS A FUNCTION OF TEMPERATURE

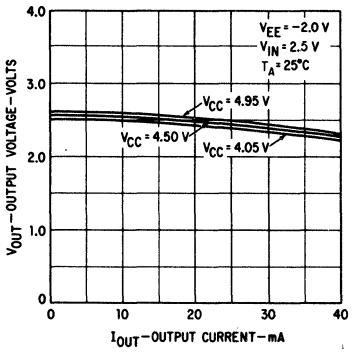


OUTPUT CHARACTERISTICS

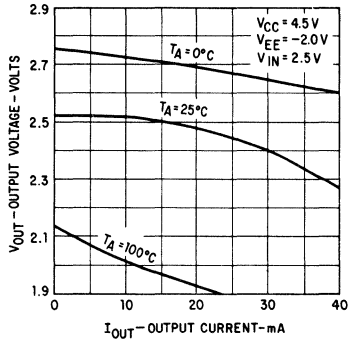
TOLERANCE VARIATION



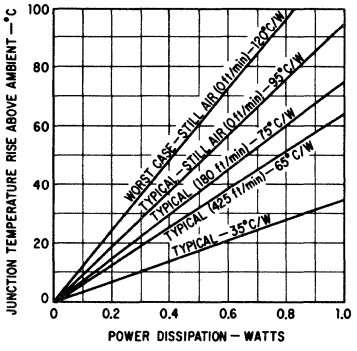
AS A FUNCTION OF V_{CC}



AS A FUNCTION OF TEMPERATURE

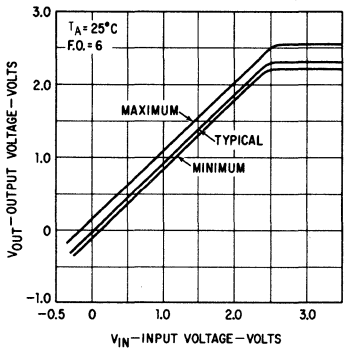


WORST CASE JUNCTION TEMPERATURE VERSUS POWER DISSIPATION

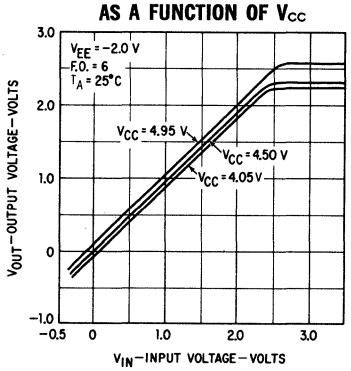


TRANSFER CHARACTERISTICS

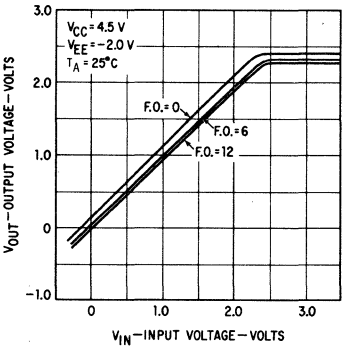
TOLERANCE VARIATION



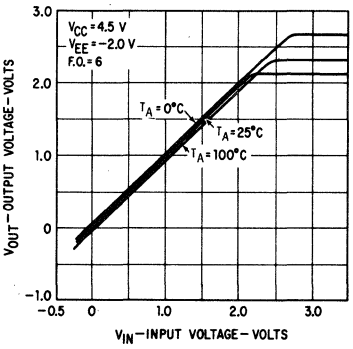
AS A FUNCTION OF V_{CC}



AS A FUNCTION OF FAN OUT

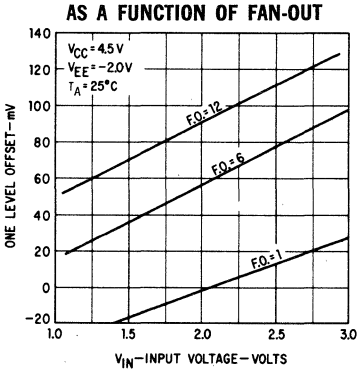


AS A FUNCTION OF TEMPERATURE

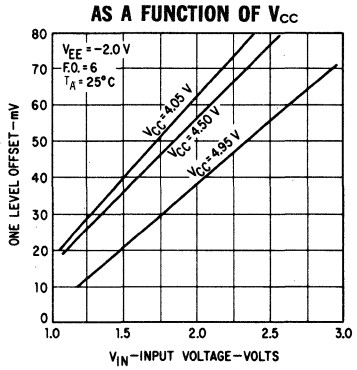


"ONE" LEVEL OFFSET

AS A FUNCTION OF FAN-OUT

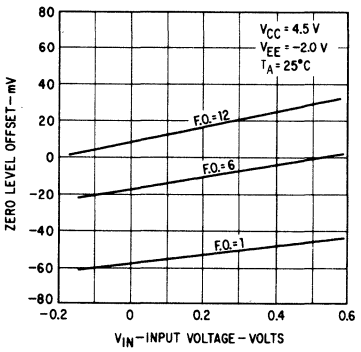


AS A FUNCTION OF V_{CC}

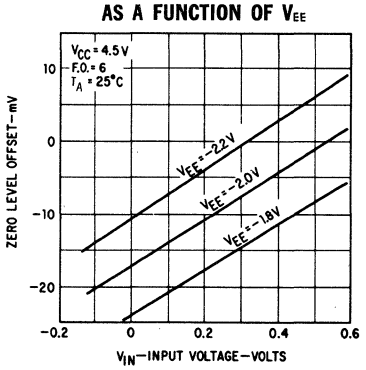


"ZERO" LEVEL OFFSET

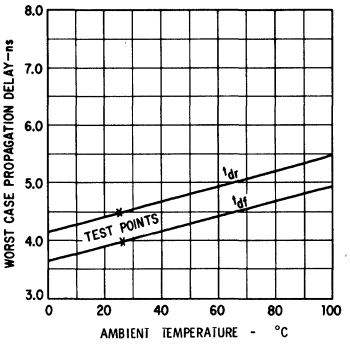
AS A FUNCTION OF FAN-OUT



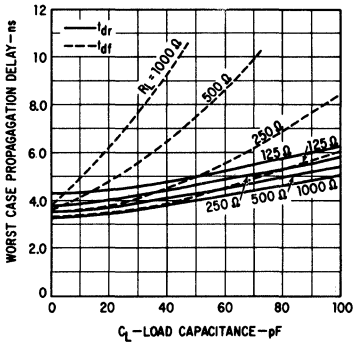
AS A FUNCTION OF V_{EE}



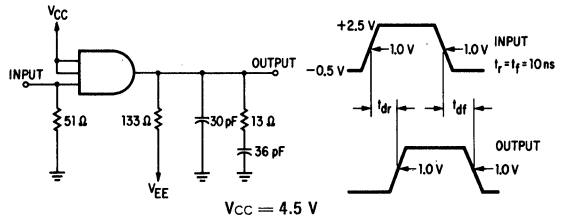
WORST CASE PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE



WORST CASE PROPAGATION DELAY VERSUS C_L AS A FUNCTION OF R_L

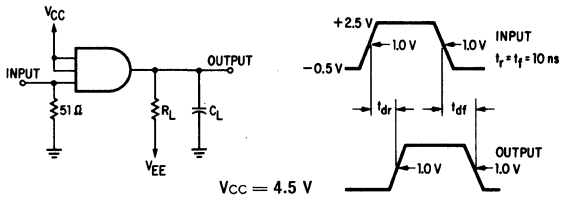


t_{PD} TEST CIRCUIT



$V_{CC} = 4.5$ V
$V_{EE} = -2.0$ V
$T_A = 25°C$

t_{PD} TEST CIRCUIT FOR ABOVE



$V_{CC} = 4.5$ V
$V_{EE} = -2.0$ V
$T_A = 25°C$

APPLICATION INFORMATION:

Greatest system speed will be realized by performing most of the logic with the use of the ultra-fast AND-OR gates. Consideration, however, must be given to level shifting, loading effects, impedance matching and ringing, which are inherent in fast switching systems. The AND-OR gates have built-in capability to overcome these problems. A few rules are outlined below to assist in solving these problems.

The electrical specification tests are performed under conditions chosen to emphasize the worst case results, and could be considered as conservative limits. For initial steps in designing new systems, typical values and data from graphs may be consulted for a realistic design. The different diagrams for each parameter are correlated through the nominal curve. To arrive at the worst case performance under a given set of conditions, deviation from nominal curve must be added or subtracted as the case may be.

INTERFACING — The AND-OR Gate should always be driven from another CTμL element. When interfacing from another logic form, or from a test signal generator, the signal should be introduced via a CTμL inverter, buffer, or flip-flop and then into the AND-OR Gate.

WIRED-OR — A powerful feature of the AND-OR Gates is that two or more outputs may be wired together to form the positive OR function at the output tie point, thus achieving two logic decisions in a maximum of 4.5 ns. Subtract 1 unit fanout for each OR added gate.

OFFSET LEVEL - NOISE IMMUNITY — The AND-OR Gate may be looked upon as a non-inverting amplifier having a gain of less than one. Thus, the output levels are offset from the input. The amount of offset is a function of loading, positive and negative power supplies, temperature, and input voltage and could be determined from the One and Zero level offset curves. When cascading AND-OR Gates, it should be noted that the offset of the first element has the largest offset and is decreasing sequentially on the following elements, due to smaller input level. It is recommended that noise-immunity levels be re-established by inserting such CTμL elements as the 952 Inverter, 956 Buffer, or 967 Flip-Flop after several offsets.

HIGH FREQUENCY RINGING — Each AND-OR Gate is internally equipped with a clamp circuit designed to reduce output ringing at high speed operation, at low fanout and moderate speed, the clamp may be released by leaving pin 5 open.

Any one length over 12″ long connected to the output should be terminated with a 200 Ω resistor to ground at the output. The 200 Ω approximates the characteristic impedance of back panel wiring. The 200 Ω termination is considered as a fanout of 4.

Regular equal spacing of AND-OR along a single path should be avoided as they tend to appear to the driving gate as a set of similarly tuned tank circuits and may induce ringing. When unavoidable, 200 Ω resistor to ground along the path will eliminate the ringing.

Large capacitive loads may cause ringing at the AND-OR Gate output and should be driven from a CTμL inverter or buffer.

UNUSED INPUTS — Unused inputs to the AND-OR Gate will effectively inhibit the gate output, and therefore, must be tied to the most positive voltage level. The unused input may be tied directly to $+V_{CC}$ or through a resistor not greater than 600 Ω. Unused inputs may be tied to active inputs at a cost of reduced fanout.

SHORT CIRCUIT PROTECTION — The AND-OR Gate output is protected by a limiting resistor at the output and may sustain prolonged short circuit to ground at V_{CC} not greater than 5 volts. Excessive destructive heat may develop when more than one output in a single package is short circuited to ground. Short circuiting the output to the —2 volts supply should be avoided.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

CTμL9956

DUAL 2-INPUT BUFFER

COMPLEMENTARY TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

+15°C TO +55°C TEMPERATURE RANGE

GENERAL DESCRIPTION — The CTμL 9956 dual 2-input power AND gate is a low impedance non-inverting level setting circuit intended to drive high fanout, and may be used as a 50Ω line driver. The input threshold and output levels are compatible with any other CTμL elements. The output of the CTμL 9956 may be tied with any other CTμL element to perform the wired OR function.

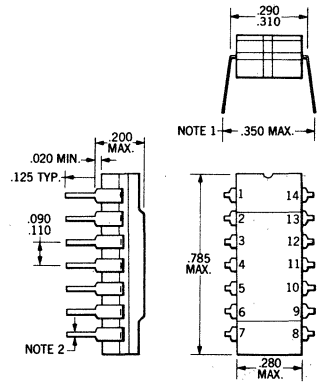
CTμL 9956 is packaged in the versatile Jedec TO-116 Dual In-Line Package* which is a hermetically sealed ceramic package intended for low cost insertion techniques.

CTμL 9956 is designed to operate over a commercial ambient temperature range of +15 to +55°C. Power supplies are 4.5 volts ± 10% and −2 volts ± 10%. Typical power dissipation per gate is 60 mW and is designed to increase with fanout. Typical propagation delay 14 ns.

*Fairchild patent pending.

PHYSICAL DIMENSIONS

TYPICAL DUAL IN-LINE PACKAGE
In Accordance With
JEDEC (TO-116) Outline

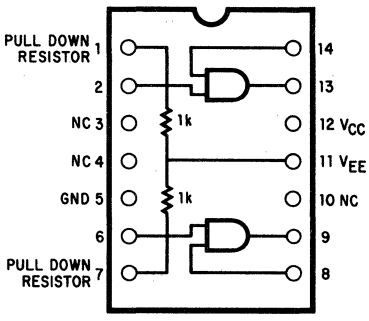


NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

FEATURES:

- Power Supplies are +4.50 V ±10% and −2.00 V ±10%.
- High Fan-Out Capability . . . 25.
- Two Optional Pull Down 1.0 k Resistors for Optimum Speed.
- Low Power Dissipation.
- Low Propagation Delay.
- Logic Swing of 3.0 V.

CONNECTION DIAGRAM



TOP VIEW

PURCHASING INFORMATION

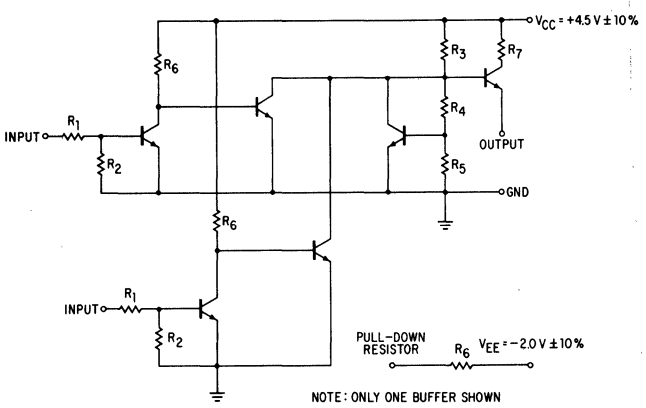
- Use the ten letter code U6A995679X for ordering purposes.
- All units are marked CTμL 995679 and date code, unless otherwise specified.

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD COMPLEMENTARY TRANSISTOR MICROLOGIC® IC

SCHEMATIC DIAGRAM



NOTE: ONLY ONE BUFFER SHOWN

ABSOLUTE MAXIMUM RATINGS
(above which the useful life may be impaired)

Maximum Current in or out of a Pin	100 mA
Maximum Chip Temperature	150°C
Maximum Power Dissipation	1.0 Watt
Maximum Voltage Applied to any Input Pin	10 Volts
Maximum Negative Voltage Applied to any Input Pin	−4.0 Volts
Maximum Voltage Applied to Output Pin	6.0 Volts

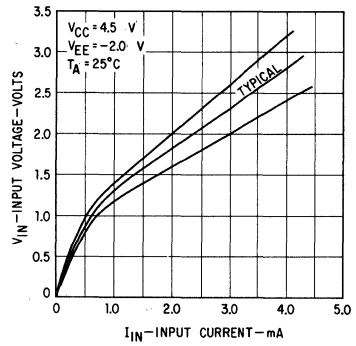
DC TESTS

TEST (at T_A = 25°C)	LIMITS				CONDITIONS			
	MIN.	TYP.	MAX.	UNITS	V_{CC}	V_{EE}	LOAD TO V_{EE}	COMMENTS
ONE Level Output	2.25	2.60		Volts	4.05	Note 1	[2]F.O. = 25	Inputs simultaneously to 1.25 V
ONE Level Output	2.46			Volts	4.95	Note 1	F.O. = 1	Inputs simultaneously to 1.25 V
ONE Level Output		2.70	3.20	Volts	4.95	Note 1	Internal 1 k	Inputs simultaneously to 3.5 V
ZERO Level Output		−0.45	−0.36	Volts	4.05	−1.8 V	F.O. = 1	Inputs to 0.8 V sequentially, unused input to 3.5 V
Input Current		5.30	6.40	mA	4.05	Note 1	No Load	Inputs to 3.5 V simultaneously, guarantees input loading ≤ 1.5 AND-OR gate loads
Input Pull Down Resistor	0.8	1.0	1.2	kΩ	4.05	−2.2 V	No Load	3.5 V applied to pull down resistor
Positive Supply Current			69.2	mA	4.95	−2.2 V	No Load	One input to 3.5 V, other inputs to GND.
Output Rising Delay, t_{dr}		12.0	18.0	ns	4.50	Note 1	F.O. = 25	See t_{pd} test circuit, page 4
Output Falling Delay, t_{df}		12.0	18.0	ns	4.50	Note 1	F.O. = 25	See t_{pd} test circuit, page 4

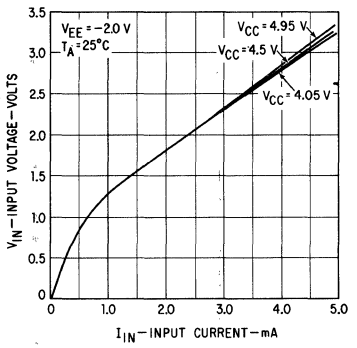
NOTES:
(1) Value of V_{EE} is non-critical: $-2.20\ V \leq V_{EE} \leq -1.80\ V$
(2) F.O. = Fan Out; F.O. = 25 equivalent to 64 Ω to −2.20 V under worst case conditions
F.O. = 1 equivalent to 2.4 kΩ to −1.80 V under worst case conditions

INPUT CHARACTERISTICS

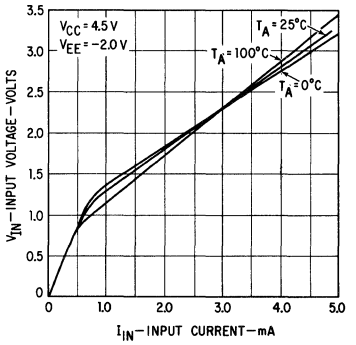
TOLERANCE VARIATION OF PARAMETERS



AS A FUNCTION OF POSITIVE SUPPLY VOLTAGE

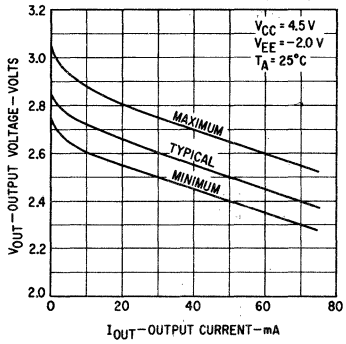


AS A FUNCTION OF TEMPERATURE

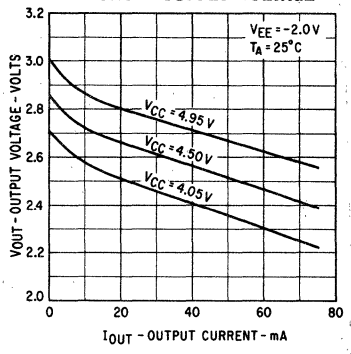


OUTPUT CHARACTERISTICS

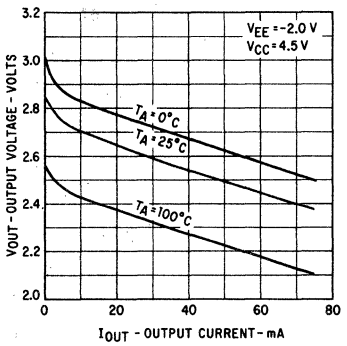
TOLERANCE VARIATION OF PARAMETERS



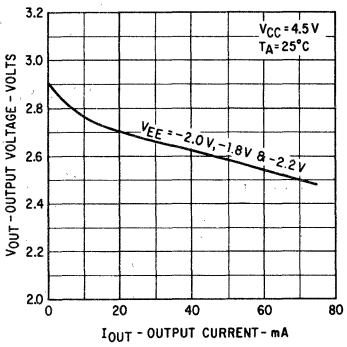
AS A FUNCTION OF POSITIVE SUPPLY VOLTAGE



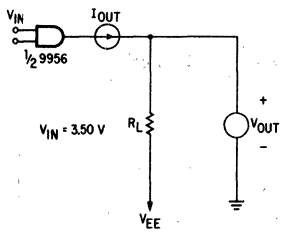
AS A FUNCTION OF TEMPERATURE



AS A FUNCTION OF NEGATIVE SUPPLY VOLTAGE

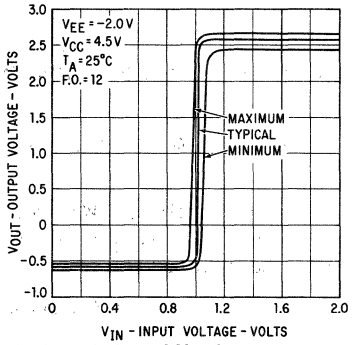


SCHEMATIC DIAGRAM



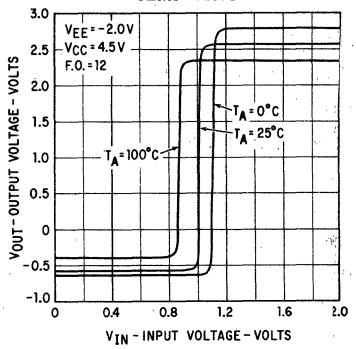
TRANSFER CHARACTERISTICS

TOLERANCE VARIATION OF PARAMETERS

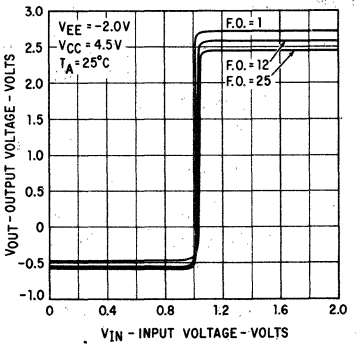


NOTE: Variation of V_{EE} does not alter transfer characteristics.

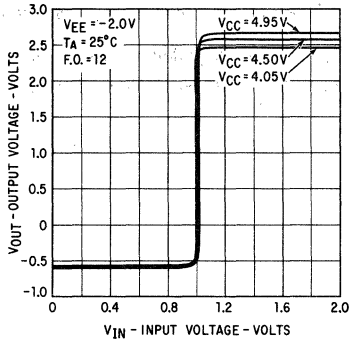
AS A FUNCTION OF TEMPERATURE



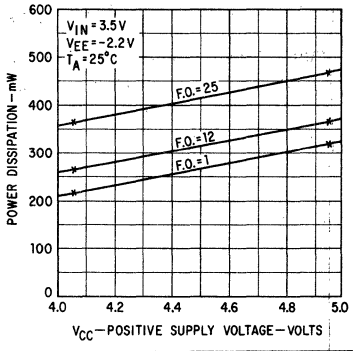
AS A FUNCTION OF FAN-OUT



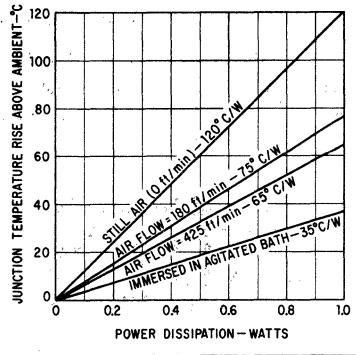
AS A FUNCTION OF POSITIVE SUPPLY VOLTAGE



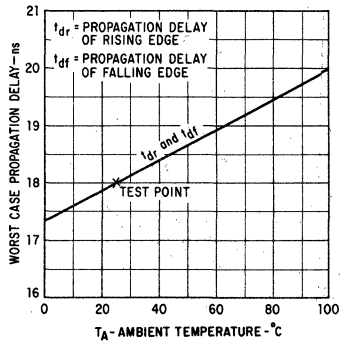
WORST CASE POWER DISSIPATION VERSUS POSITIVE SUPPLY VOLTAGE



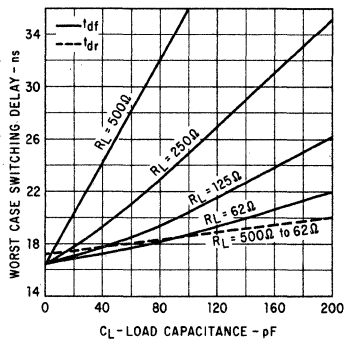
WORST CASE JUNCTION TEMPERATURE VERSUS POWER DISSIPATION



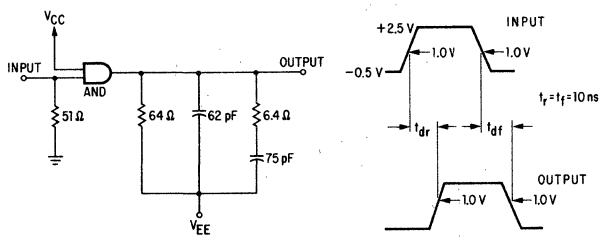
WORST CASE PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE



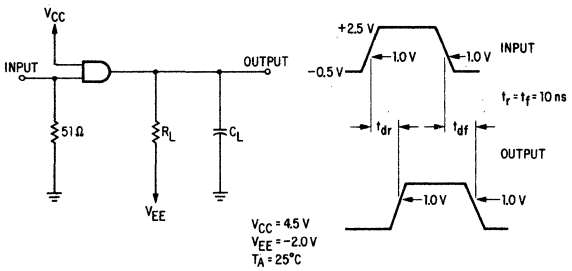
WORST CASE PROPAGATION DELAY VERSUS LOAD CAPACITANCE AS A FUNCTION OF LOAD RESISTANCE



t_{PD} TEST CIRCUIT



t_{PD} TEST CIRCUIT FOR ABOVE



APPLICATION INFORMATION

The electrical specification tests are performed under conditions chosen to emphasize the worst case results and could be considered as conservative limits. The output ONE level at worst case is guaranteed to drive a fanout of 25 AND-OR gates. The maximum input current assures that 9956 input presents a load of not more than 1.5 AND-OR gate input.

INTERFACING — The CTμL 9956 buffer could serve as an excellent interfacing link between external signals coming from other logic forms or peripheral equipments and the CTμL Family logic.

PULL DOWN RESISTORS — Two pull down 1 kΩ resistors are built into the package with one end tied to the negative power supply (V_{EE}). When the 9956 input is driven by a single AND-OR gate, the 1 kΩ resistors should be connected to the same input pin. This will improve the 9956 output rise and fall time. The pull-down resistor may be also connected to the CTμL 9956 output, which will improve the output falling delay when the fanout is low.

LINE DRIVER — The CTμL 9956 could be used as a line driver. To drive a 50 Ω line, a 68 Ω resistor should be connected from the output to ground. This will reduce the fanout capability by 15.

WIRED-OR — A powerful feature of the CTμL 9956 Buffer is that the output may be tied together with the output of any other element in the CTμL family to form the positive OR function at the tie point. When two or more CTμL 9956 outputs are tied for the OR function, a pull-down resistor must be used.

UNUSED INPUTS — Unused inputs to the AND-OR Gate will effectively inhibit the gate output, and therefore, must be tied to the most positive voltage level. The unused input may be tied directly to $+V_{CC}$ or through a resistor not greater than 600 Ω. Tying an unused input to an active input is not recommended.

SHORT CIRCUIT PROTECTION — The CTμL 9956 Gate output is protected by a limiting resistor at the output and may sustain prolonged short circuit to ground at V_{CC} not greater than 5 volts. Excessive destructive heat may develop when more than one output in a single package is short circuited to ground. Short circuiting the output to the −2 volts supply should be avoided.

CTμL 9957•9967
FLIP-FLOPS
COMPLEMENTARY TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS
+15°C TO +55°C TEMPERATURE RANGE

CTμL 9967 FLIP-FLOP GENERAL DESCRIPTION

The CTμL 9967 dual rank J-K Flip-Flop is a high speed directly coupled multi-purpose storage element useful for shift registers, counters, and other control functions.

Operation of the CTμL 9967 is based on the "master-slave" principle whereby information is entered into the "master" when the clock pulse goes high and is transferred to "slave" and outputs when the clock pulse goes low. DC coupling throughout makes the Flip-Flop input insensitive to rise and fall times.

The CTμL 9967 employs the PNP-NPN complementary logic to achieve fast response with typical toggling rate of 35 MHz. The emitter follower outputs are compatible with all other elements in the CTμL family.

Two phase clock outputs at half the clock input frequency is available when the CTμL 9967 is operated as a binary counter. Typical power dissipation is 420 mW and is designed to increase with fanout.

CTμL 9957 GENERAL DESCRIPTION

The CTμL 9957 is a basic dual-rank R-S Flip-Flop intended for storage and control function. Logic and clock inputs are omitted for additional flexibility. J-K operation with either two-phase or single-phase clocking can be exercised by adding AND-OR gates to the inputs. Wired OR ties within the flip-flop reduce typical through propagation delays to 14 ns.

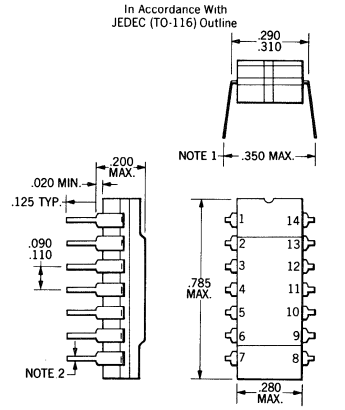
The CTμL 9957 is DC coupled throughout. The inputs respond exclusively to voltage levels and are insensitive to rise and fall times. Emitter follower outputs, compatible with all other CTμL elements, provide efficient drive capability into long line and capacitive loads.

The CTμL 9967 and CTμL 9957 are packaged in the versatile Dual In-Line Package which is hermetically sealed ceramic package intended for low cost insertion techniques.

Both flip-flops are designed to operate over a commercial ambient temperature range of +15°C to +55°C. Power supplies are 4.5 volts ±10% and −2 volts ±10%.

PHYSICAL DIMENSIONS

TYPICAL DUAL IN-LINE PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

PURCHASING INFORMATION

DESCRIPTION	CODE	MARKING
CTμL 9957	U6A995779X	CTμL 95759
CTμL 9967	U6A996779X	CTμL 96779

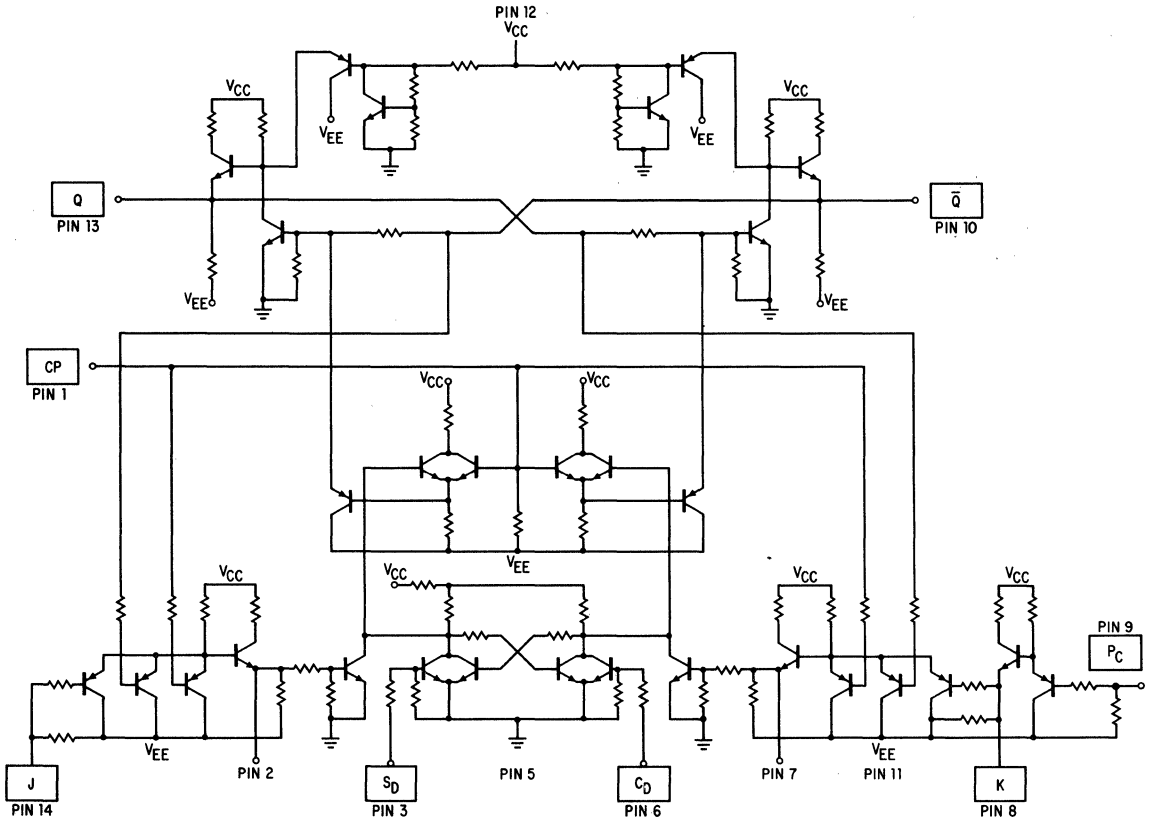
Use the ten letter code for ordering purposes.
All units marked as above unless otherwise specified.

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

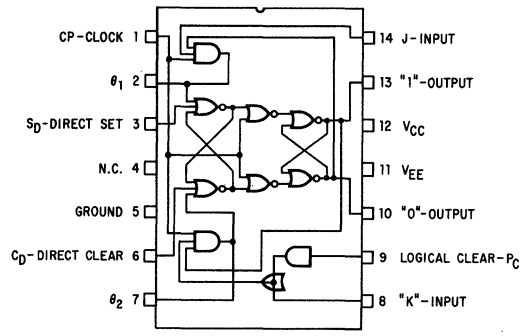
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

CTμL 9967 COMPLEMENTARY TRANSISTOR MICROLOGIC® IC

SCHEMATIC DIAGRAM



PIN & LOGIC DIAGRAM CTμL9967 - JK FLIP FLOP



V_{CC} = 4.50 V
V_{EE} = −2.00 V
N.C. = NOT CONNECTED

TRUTH TABLE

SYNCHRONOUS ENTRY					ASYNCHRONOUS ENTRY			
		t_n		$t_n + 1$	Inputs		Outputs	
J	K	SD	CD	output (Q)	SD	CD	"1"	"0"
L	L	L	L	Q_n	L	L	NC	NC
L	H	L	L	L	L	H	L	H
H	L	L	L	H	H	L	H	L
H	H	L	L	$\bar{Q}_n$	H	H	H	H
L	L	L	H	H	Clock Input Low			
L	L	H	L	L				
L	L	H	H	Undetermined				

LOADING RULES

FLIP-FLOP INPUTS	LOADING*
CP	2.0
J, K	1.0
S_D, C_D,	1.5
P_C	1.0
OUTPUTS	**FAN OUT**
Q, Q̄	12

*1 Load = 1 CTμL AND-OR Gate Input Load

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Maximum current in or out of a pin	100 mA
Maximum chip temperature	150°C
Maximum power dissipation	1.0 Watt
Maximum voltage applied to any input pin	10 Volts
Maximum negative voltage applied to any input pin	−4.0 Volts
Maximum voltage applied to output pin	6.0 Volts

CTμL 9967 COMPLEMENTARY TRANSISTOR MICROLOGIC® IC

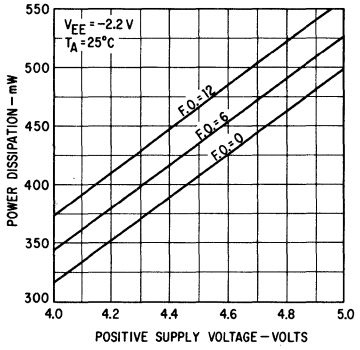
ELECTRICAL CHARACTERISTICS

9967 DC TESTS

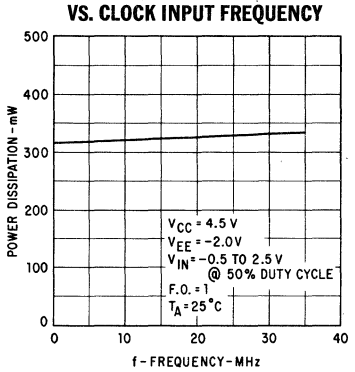
TESTS (at $T_A = 25°C$)	LIMITS				CONDITIONS			
	MIN.	TYP.	MAX.[5]	UNITS	V_{CC}	V_{EE}	Load to V_{EE}	COMMENTS
ONE Level Output	2.35	2.50		Volts	4.05	NOTE 1	[3]F.O. = 12	Untested output to 3.50 V; logic input to 1.33 V; clock inputs to pulse (Note 4)
ONE Level Output	2.56			Volts	4.95	NOTE 1	No Load	Untested output to 3.50 V; logic input to 1.33 V; clock inputs to pulse (Note 4)
ONE Level Output	2.56			Volts	4.95	NOTE 1	No Load	Untested direct input to 3.50 V; tested direct input to 1.25 V; clock input to −0.70 V.
ONE Level Output			3.20	Volts	4.95	−1.80	F.O. = 1	Corresponding direct input is 3.50 V.
ZERO Level Output		−0.50	−0.36	Volts	NOTE 2	−1.80	F.O. = 1	Direct input to 3.50 V; other direct input to 0.80 V; logic inputs to 3.50 V; clock input to 0.47 V.
ONE Level Offset		200	270	mV	4.05	−2.20	F.O. = 4	Trigger and logic inputs sequentially to 2.25 V; untested inputs and outputs to 3.50 V.
ZERO Level Offset		120	195	mV	4.95	−1.80	F.O. = 1	Clock and logic inputs sequentially to −0.36 V. Untested inputs and outputs to 3.50 V.
Logic Input Pull-down Resistor	1.6 k	2.0 k	2.4 k	Ω	NOTE 2	−1.80	No Load	Logic input is 3.50 V.
Clock Input Pull-down Resistor	0.8 k	1.0 k	1.2 k	Ω	NOTE 2	−1.80	No Load	Clock input to 3.50 V.
Input Current		6.1	7.67	mA	NOTE 2	−1.80	No Load	Terminals 2 and 7 to 3.50 V.
Input Current		2.0	3.27	mA	4.05	−1.80	No Load	Direct set and clear inputs to 3.50 V.
Positive Supply Current		51.0	64.0	mA	4.95	−2.20	No Load	Clock input to −0.47 V.
Negative Supply Current		55.0	68.7	mA	4.95	−2.20	No Load	Clock, logic inputs and "1" outputs to 3.50 V simultaneously.
Clock Pulse Width - t_{PW}	25	16.0		ns	4.50	−2.00	F.O. = 12	Min. required pulse width to trigger 967.
Output Rising Delay - t_{dr}		10.0	15.0	ns	4.50	−2.00	F.O. = 12	See t_{df}, t_{dr} test circuit, page 4
Output Falling Delay - t_{df}		16.0	25.0	ns	4.50	−2.00	F.O. = 12	See t_{df}, t_{dr} test circuit, page 4
Direct Through Rising Delay - t_{sr}		17.0	25.0	ns	4.50	−2.00	F.O. = 12	See t_{sr}, t_{sf} test circuit, page 5
Direct Through Falling Delay - t_{sf}		25.0	38.0	ns	4.50	−2.00	F.O. = 12	See t_{sr}, t_{sf} test circuit, page 5

NOTES:
(1) Value of V_{EE} non-critical, $-1.80\ V \leq V_{EE} < -2.20\ V$.
(2) Value of V_{CC} non-critical, $4.05\ V \leq V_{CC} \leq 4.95\ V$.
(3) F.O. = Fan-Out: F.O. = 12 equivalent to 133Ω to −2.20 V under worst case conditions.
F.O. = 4 equivalent to 400Ω to −2.20 V under worst case conditions.
F.O. = 1 equivalent to 2.4 k to −1.80 V under worst case conditions.
(4) Pulse is a positive pulse of non-critical amplitude and width.
(5) "Maximum" means "no more positive than."

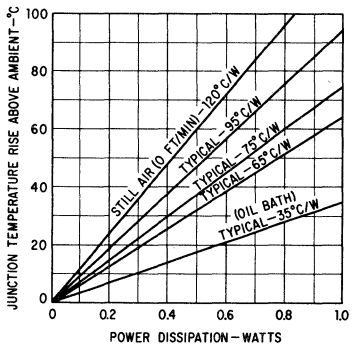
WORST CASE POWER DISSIPATION VS. POSITIVE SUPPLY VOLTAGE



WORST CASE POWER DISSIPATION VS. CLOCK INPUT FREQUENCY



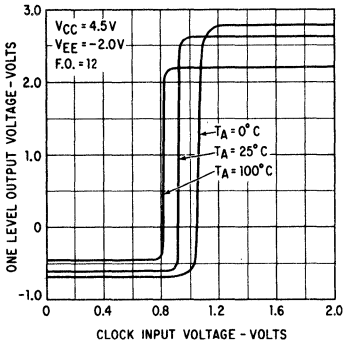
WORST CASE JUNCTION TEMPERATURE VS. POWER DISSIPATION



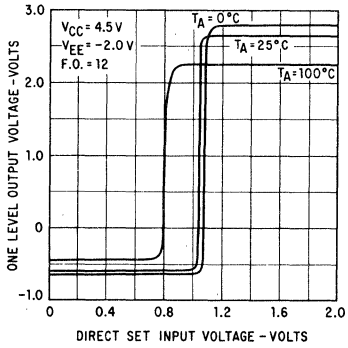
CTμL 9967 COMPLEMENTARY TRANSISTOR MICROLOGIC® IC

TRANSFER CHARACTERISTICS

CLOCK-ONE LEVEL VERSUS TEMPERATURE

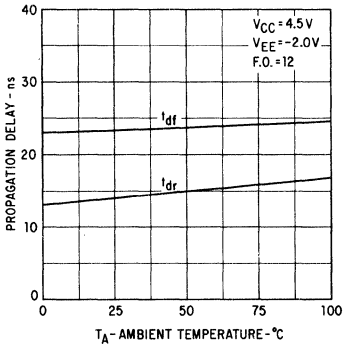


DIRECT SET/DIRECT CLEAR VERSUS TEMPERATURE

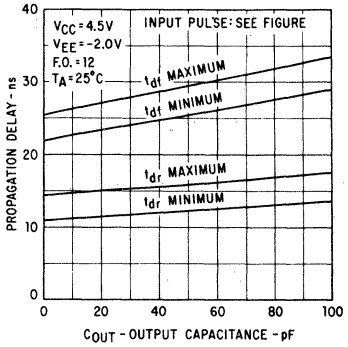


SWITCHING CHARACTERISTICS

PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE

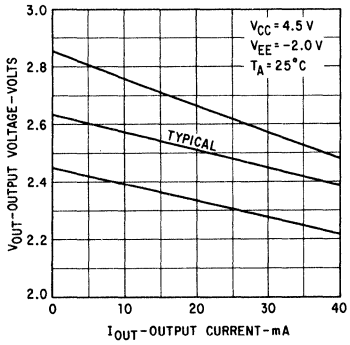


INCREASE IN PROPAGATION DELAY DUE TO OUTPUT CAPACITANCE

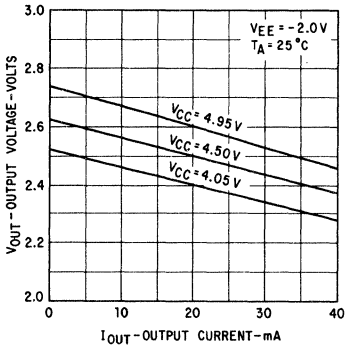


OUTPUT CHARACTERISTICS

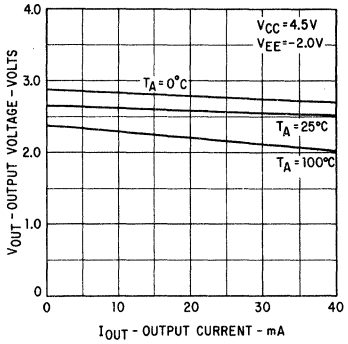
TOLERANCE VARIATION OF PARAMETERS



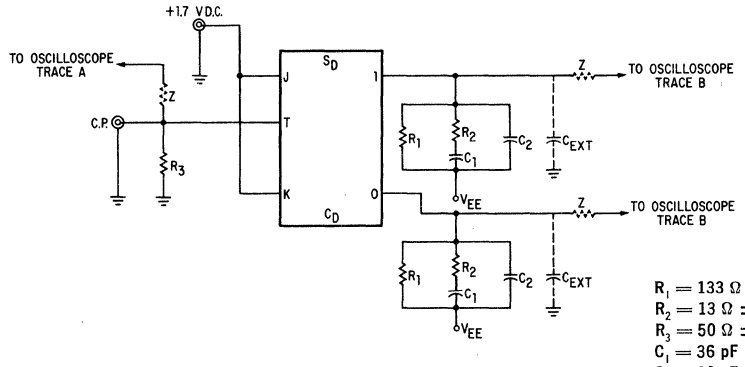
AS A FUNCTION OF COLLECTOR SUPPLY VOLTAGE



AS A FUNCTION OF TEMPERATURE



t_{df} and t_{dr} SWITCHING TIME TEST CIRCUIT



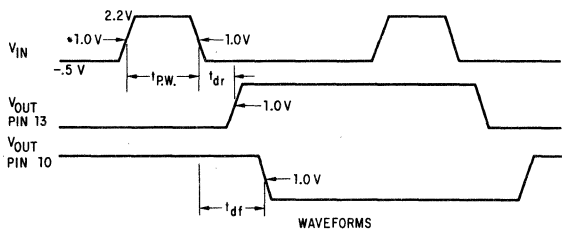
$R_1 = 133\ \Omega \pm 1\%$
$R_2 = 13\ \Omega \pm 1\%$
$R_3 = 50\ \Omega \pm 1\%$
$C_1 = 36$ pF $\pm 2\%$
$C_2 = 30$ pF $\pm 2\%$
Z = Probe Impedance $\geq$ 5k

SWITCHING NOTES:

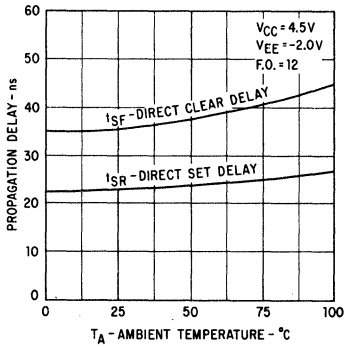
(1) Input Pulse
Frequency: 10 Hz to 10 MHz
Pulse Width (t_{PW}) = 25 ns
Rise Time = 10 ns
Fall Time = 10 ns
at 10% to 90% pts.

(2) The load capacitance indicated in the test circuit includes the capacitance of the probe and jig.

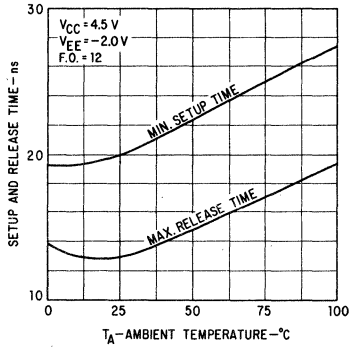
(3) $V_{CC} = 4.50$ V; $V_{EE} = -2.00$ V



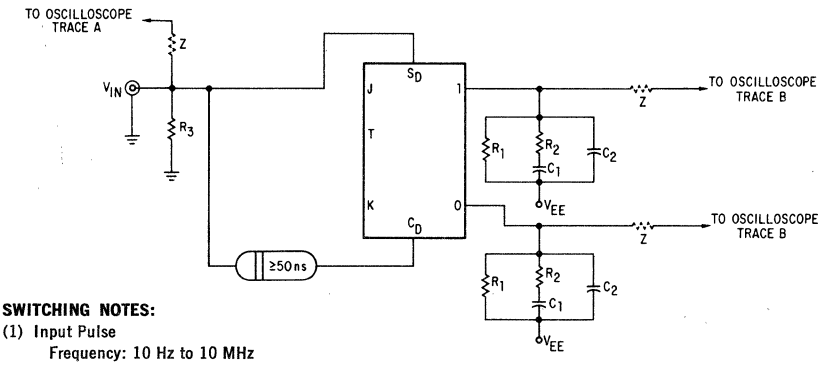
DIRECT SET AND DIRECT CLEAR PROPAGATION DELAY VERSUS TEMPERATURE



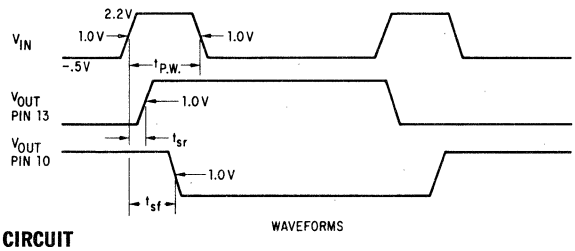
WORST CASE SETUP AND RELEASE TIME VERSUS TEMPERATURE



DIRECT SET & DIRECT CLEAR SWITCHING TIME TEST CIRCUIT



$R_1 = 133\ \Omega \pm 1\%$
$R_2 = 13\ \Omega \pm 1\%$
$R_3 = 50\ \Omega \pm 1\%$
$C_1 = 36$ pF $\pm 2\%$
$C_2 = 30$ pF $\pm 2\%$
Z = Probe Impedance $\geq 5k$



WAVEFORMS

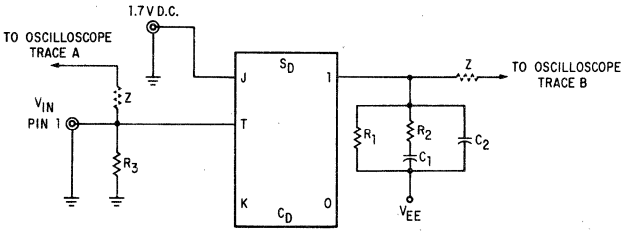
SWITCHING NOTES:

(1) Input Pulse
Frequency: 10 Hz to 10 MHz
Pulse Width = 25 ns
Rise Time = 10 ns
Fall Time = 10 ns
at 10% to 90% pts.

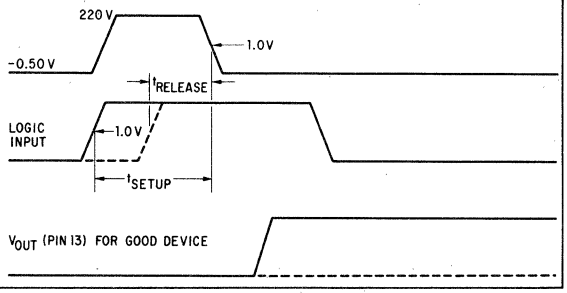
(2) The load capacitance indicated in the test circuit includes the capacitance of the probe and jig.

(3) $V_{CC} = 4.50$ V; $V_{EE} = -2.00$ V

$t_{SET\text{-}UP}$ & $t_{RELEASE}$ SWITCHING TIME TEST CIRCUIT



$R_1 = 133\ \Omega \pm 1\%$
$R_2 = 13\ \Omega \pm 1\%$
$R_3 = 50\ \Omega \pm 1\%$
$C_1 = 36$ pF $\pm 2\%$
$C_2 = 30$ pF $\pm 2\%$
Z = Probe Impedance $\geq 5k$



SWITCHING NOTES:

(1) Input Pulse
Rise Time = 10 ns
Fall Time = 10 ns
Amplitude = 2.10 V
at 10% to 90% pts.

(2) The load capacitance indicated in the test circuit includes the capacitance of the probe and the jig.

(3) $V_{CC} = 4.50$ V; $V_{EE} = -2.00$ V.

(4) Similar tests may be made at "O" output if logic input is the "K" input.

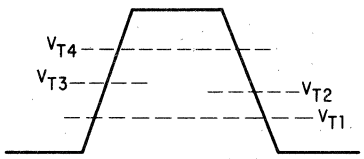
(5) $t_{SET\text{-}UP}$ is defined as the minimum time required for a "ONE" to be present at either iogic input prior to a clock transition from a high to a low in order for the flip-flop to respond. $t_{RELEASE}$ is defined as the maximum time required for a ONE to be present at either logic input prior to clock transition from a high to a low in order for the flip-flop not to respond.

OPERATION OF FLIP-FLOP

The CTμL 9967 is directly coupled throughout and hence, its inputs are not sensitive to rise times. It responds exclusively to input voltage levels with definite, separated thresholds for both high and low voltage levels.

As the clock input rises from ZERO level, above V_{T1}, the transfer gates between the master and the slave are inhibited and the slave is isolated from the master. Above V_{T3}, the logic input gates are enabled and the master is set. Above V_{T4}, the master is sure to be set under the worst case condition and clock input is reaching the ONE level. As the clock input falls from the ONE level below V_{T4}, it inhibits the logic input gates and assures no further change in the master flip-flop. Below V_{T2}, the transfer gates are enabled, the slave and outputs are set according to information stored in the master. Below V_{T1}, the transfer gates are sure to be enabled under the worst case condition. The clock input reaches the ZERO level.

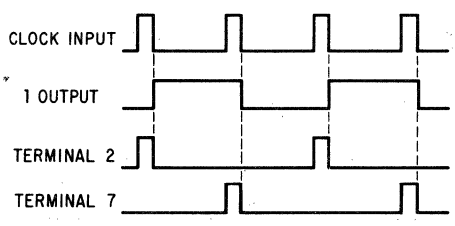
CLOCK INPUT VOLTAGE



Synchronous entry of information is done at the J and K inputs while the clock input is high.

Asynchronous information is entered at the S_D and C_D Direct Set and Direct Clear. A high level ONE is applied to the appropriate asynchronous input while the clock input is at the ZERO (low) level. Sufficient time must be allowed for the flip-flop to change state before the clock goes high.

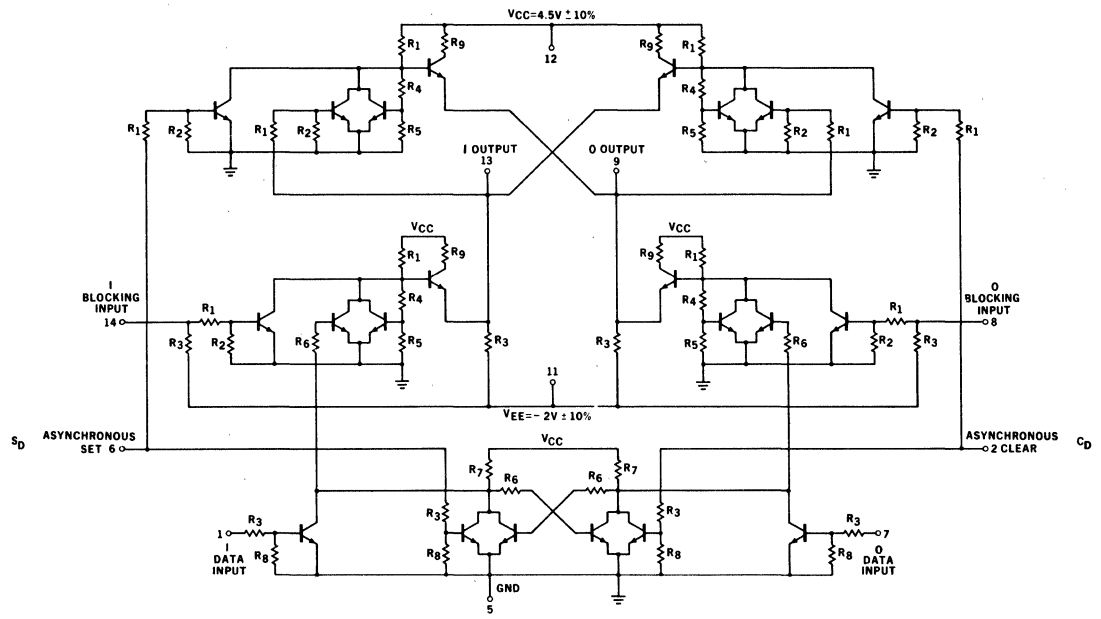
Pins 2 and 7 may serve as an output for a two phase clock having the same pulse duration as the clock input. Each output has a repetition rate of half the clock input frequency. (Fig. 1, Wired OR)



Pin 9, designated as a Logical Clear, may be used to block information from entering the J input without inhibiting the internal AND gate. It may also serve as an additional isolated J input.

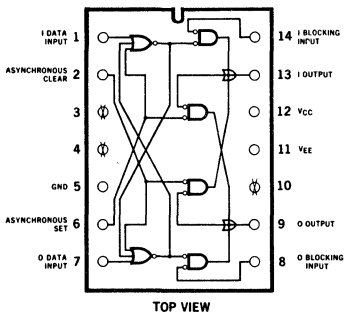
CTμL 9957 COMPLEMENTARY TRANSISTOR MICROLOGIC® IC

SCHEMATIC DIAGRAM



LOGIC DIAGRAM

(POSITIVE LOGIC)



TOP VIEW

TRUTH TABLE

S_n	C_n	Qnt + 1
0	0	Qn
0	1	0
1	0	1
1	1	Undetermined

NOTES:
(1) Connect pin 1 to pin 14 and pin 7 to pin 8
(2) Flip-Flop changes state on negative transition of input waveforms
(3) For asynchronous entry use pins 2 and 6

LOADING RULES

FLIP-FLOP UNITS	LOADING*
Data	1.0
SA, CA	2.0
Blocking	3.5
OUTPUTS	**FAN OUT**
Q, $\overline{Q}$	9.5

*1 Load = 1 CTμL AND-OR Gate Input Load

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Maximum current in or out of a pin	100 mA
Maximum chip temperature	150°C
Maximum power dissipation	1.0 Watt
Maximum voltage applied to any input pin	10 Volts
Maximum negative voltage applied to any input pin	—4.0 Volts
Maximum voltage applied to output pin	6.0 Volts

DC TESTS

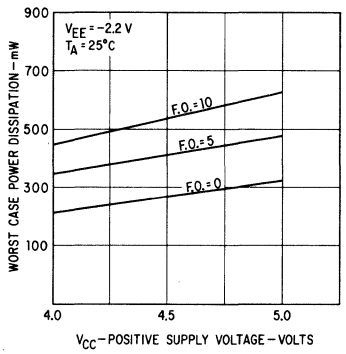
TESTS (at $T_A = 25°C$)	LIMITS				CONDITIONS			
	MIN.	TYP.	MAX.	UNITS	V_{CC}	V_{EE}	Load to V_{EE}	COMMENTS
ONE Level Output			3.20 V	Volts	4.50	−2.00	No Load	Pulse note (1) to pin 3.
ONE Level Output	2.20			Volts	4.05	−2.20	(2)F.O. = 9.5	0.8 V to Pins 1 and 6, 2.5 V to Pin 8; Pulse to Pin 2. Guarantees min. ONE level output.
ONE Level Output	2.20			Volts	4.05	−2.20	F.O. = 9.5	2.5 V to Pins 2 and 6, 0.8 V to Pin 8.
ZERO Level Output			−0.36	Volts	4.95	−1.80	No Load	Pulse to Pin 6, 1.25 V to Pin 7.
ZERO Level Output			−0.36	Volts	4.95	−1.80	No Load	Pulse to Pin 2, 1.25 V to Pin 6, 2.5 V to Pin 14.
ZERO Level Output			−0.36	Volts	4.95	−1.80	No Load	1.25 V to Pin 8, 2.5 V to Pins 6 and 7.
ZERO Level Output			−0.36	Volts	4.95	−1.80	No Load	2.5 V to Pins 2, 8, 14; 1.25 V to Pin 13.
Input Current Data Input	1.5		2.25	mA	4.50	−2.0	No Load	2.5 V to Pins 1 and 7 sequentially.
Input Current Async. Input			6.75	mA	4.5	−2.0	No Load	2.5 V to Pins 2 and 6 sequentially. Guarantees asynchronous input loading.
Input Current Blocking Input			10.13	mA	4.5	−2.0	No Load	2.5 V to Pins 8 and 14 sequentially.
Output Resistor	6.75		10.13	mA	4.5	−2.0	No Load	2.5 V to Pins 6 and 9, Pins 2 and 13 sequentially.
Propagation Delay, t_{DR}		10	15	ns	4.5	−2.0	F.O. = 9.5	See Fig.
Propagation Delay, t_{DF}		17	30	ns	4.5	−2.0	F.O. = 9.5	See Fig.

NOTES:

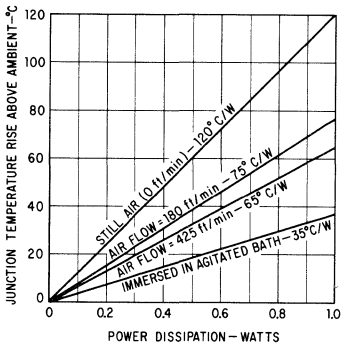
(1) Pulse, positive pulse of non-critical amplitude and width.
(2) F.O. = Fan-Out: F.O. = 9.5 equivalent to 168Ω to −2.20 V under worst case conditions.

ELECTRICAL CHARACTERISTICS

WORST CASE POWER DISSIPATION VERSUS POSITIVE SUPPLY VOLTAGE

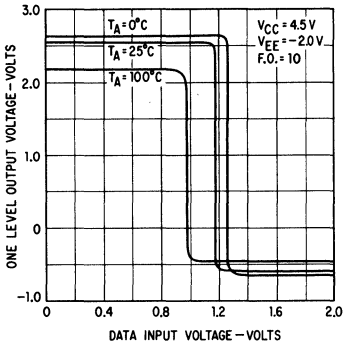


WORST CASE JUNCTION TEMPERATURE VERSUS POWER DISSIPATION

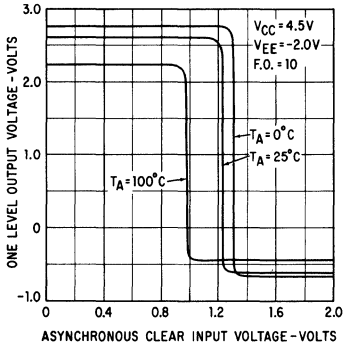


TRANSFER CHARACTERISTICS

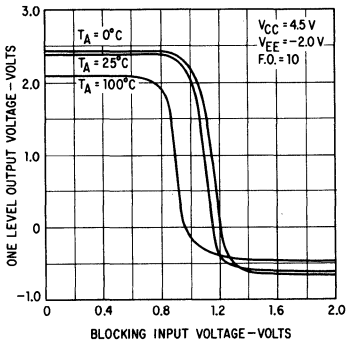
DATA INPUT - ONE LEVEL OUTPUT VOLTAGE VERSUS TEMPERATURE



ASYNCHRONOUS SET/CLEAR-ONE LEVEL OUTPUT VOLTAGE VERSUS TEMPERATURE

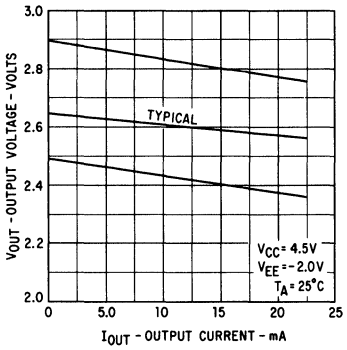


BLOCKING INPUT - ONE LEVEL OUTPUT VOLTAGE VERSUS TEMPERATURE

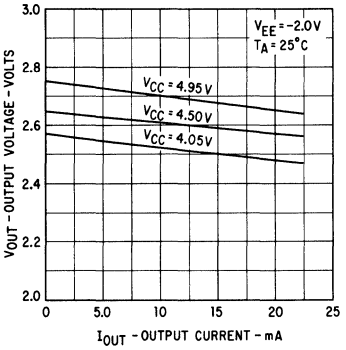


OUTPUT CHARACTERISTICS

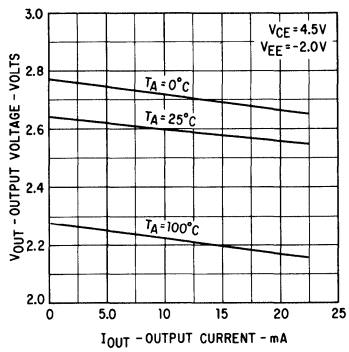
TOLERANCE VARIATION OF PARAMETERS



AS A FUNCTION OF COLLECTOR SUPPLY VOLTAGE

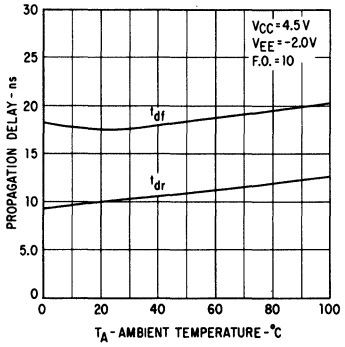


AS A FUNCTION OF TEMPERATURE

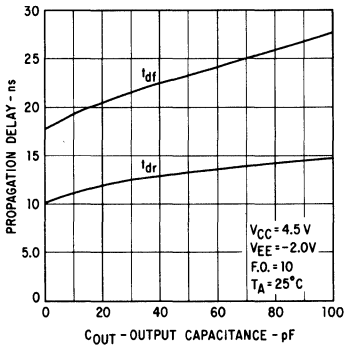


SWITCHING CHARACTERISTICS

PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE

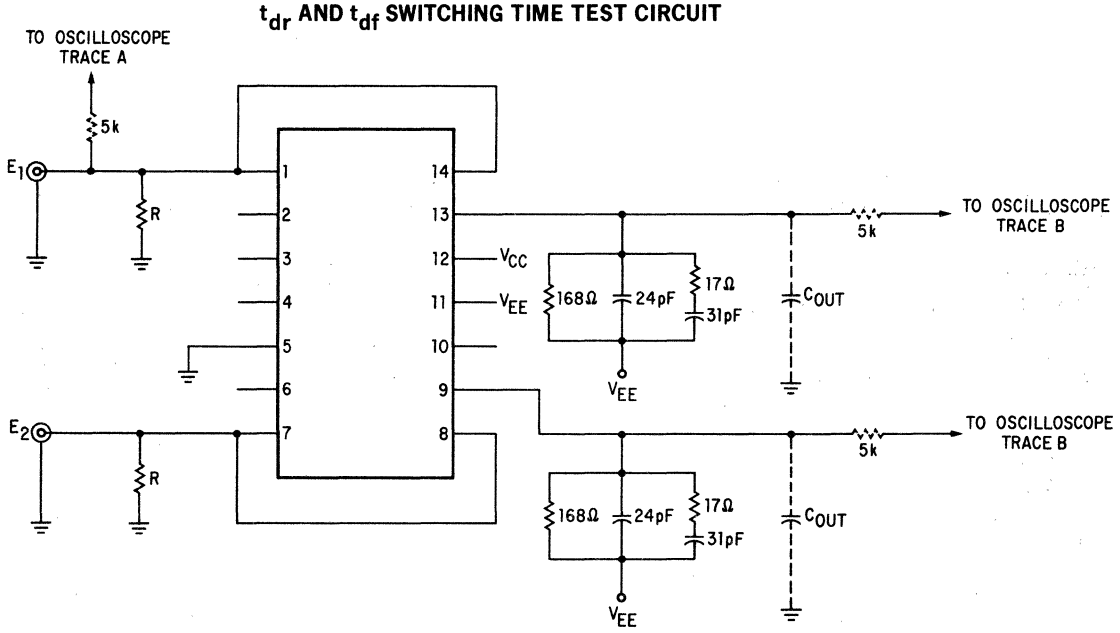


INCREASE IN PROPAGATION DELAY DUE TO OUTPUT CAPACITANCE

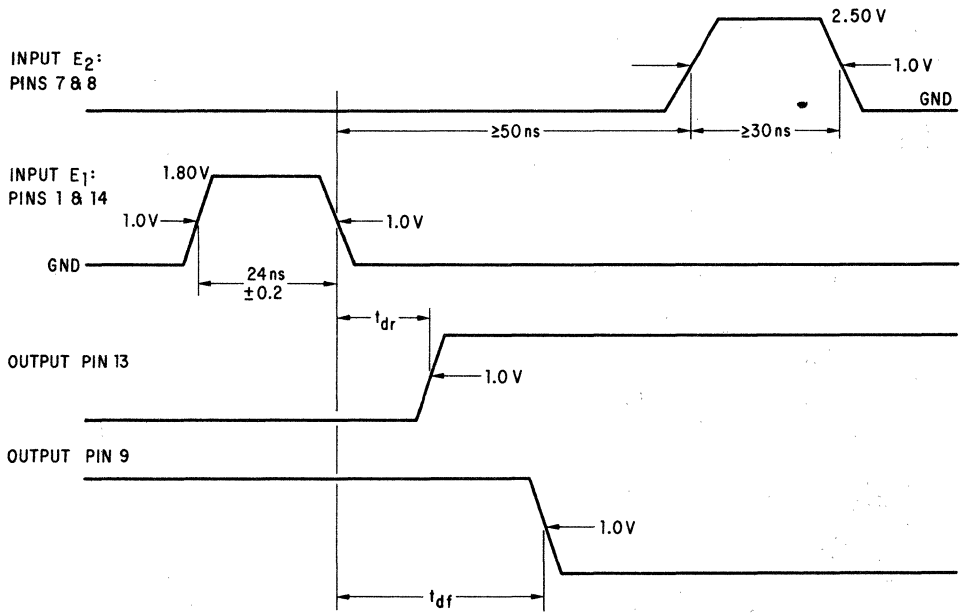


SWITCHING CHARACTERISTICS

t_{dr} AND t_{df} SWITCHING TIME TEST CIRCUIT



WAVEFORMS



SWITCHING NOTES:

(1) $V_{CC} = 4.50\ V \pm 10\%$
$V_{EE} = 2.00\ V \pm 10\%$
Select proper capacitor to provide adequate bypassing.

(2) Select R to provide proper termination for pulse generator used.

(3) Use oscilloscope with at least 5 k input impedance.

(4) Rise & Fall Times:
$t_f = t_r = 5ns$ measured at 10% to 90% points.

OPERATION OF FLIP-FLOP

The CTμL 9957 is a dual-rank directly-coupled R-S Flip-Flop. The first rank or "master" consists of two cross-coupled NOR gates similar to the CTμL 9952. The second rank or "slave" employs OR ties as shown in the functional logic diagram, thereby minimizing through delay. Two NAND gates provide feedback inversion, while the other two provide gating between "master" and "slave."

The primary data inputs to the Flip-Flop are through pins 1 and 7. These inputs work directly from AND gate outputs, allowing OR ties and multiple inputs to each Flip-Flop.

To take advantage of the dual-rank principle, mutually exclusive active inputs should be applied to the gating to "master" and "slave" so that only one or the other can change at any particular instant. This is easily accomplished in the CTμL 9957 due to the difference in active polarity of the two gates. Thus, what appears as a logic 1 to CTμL gates of the Flip-Flop data inputs is a logic 0 to the "slave" gates, and vice versa.

These observations lead to the connection of pin 1 to pin 14 and pin 7 to pin 8 as shown in Fig. 2. Although both "slave" gates are not necessarily inhibited when a change takes place, the output cannot change unless both data inputs are logic 0. Therefore, this connection is the usual one, tending to minimize the loading of timing circuits.

In case phased timing signals are advantageous, pins 8 and 14 may be used independently as long as they are never active (low) while their corresponding data inputs are high.

Direct inputs to both "master" and "slave" appear on pins 2 and 6. A logic (high) on either input sets or resets the "master" and simultaneously inhibits a feedback NAND gate in the "slave." The net effect is that both "master" and "slave" move to the desired condition during the presence of the direct input signal.

The response of the Flip-Flop to concurrent inputs tending to set opposite output conditions is ambiguous. That is, simultaneous logic 1 inputs must be avoided for well-defined operation.

APPLICATION

FIG. 1 DUAL RANK FLIP-FLOP CONNECTED FOR TWO-PHASE CLOCKING, J-K MODE

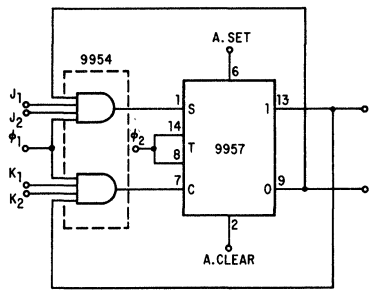


FIG. 2 DUAL RANK FLIP-FLOP CONNECTED FOR SINGLE-PHASE CLOCKING, J-K MODE

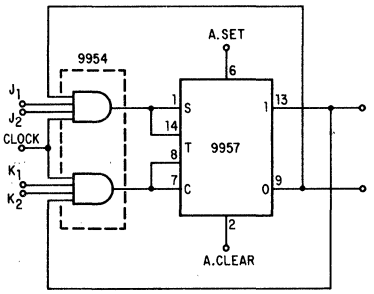


FIG. 3 SERIAL BINARY COUNTER

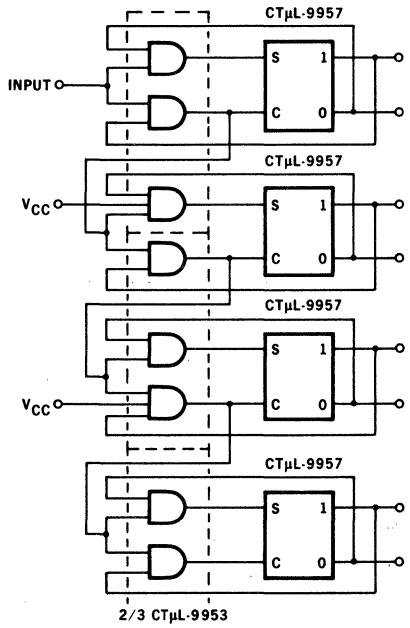
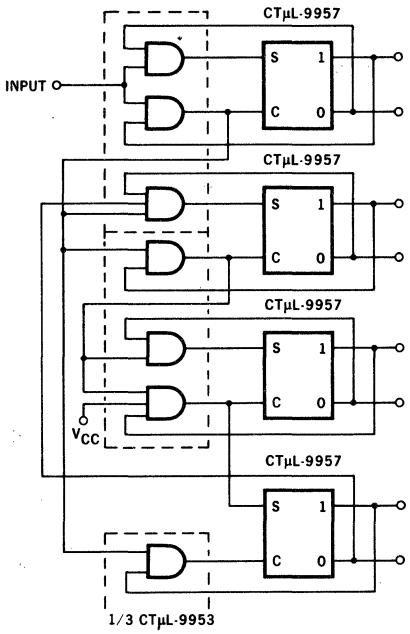


FIG. 4 1-2-4-8 DECADE



NOTES:
1. On all CTμL 9957's, tie pins 1-14 and 7-8.
2. All gates are CTμL 9953's.

CμL 9958
DECADE COUNTER
COUNTER MICROLOGIC® INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The CμL9958 is a complete Decade Counter consisting of four cascaded binary triggered flip-flops modified by a feedback loop to count in the familiar 8-4-2-1 code. Provision is made for clearing and presetting any one of the possible decimal states. The monolithic structure employs only resistors and transistors and is manufactured with Fairchild Planar* Epitaxial process to assure maximum performance and reliability.

The Decade Counter is designed to operate in the 0° to +75°C temperature range with nominal power supply voltage of 3.3 to 5.5 volts. It is also available in the -55°C to +125°C temperature range with power supply voltage of 4.0 to 4.4 volts.

The CμL9985 is available in the hermetically sealed 14 pin Dual In-line ceramic package, and in the 8 pin modified TO-5 metal can.

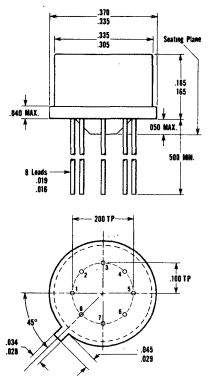
ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	-55°C to +150°C
Voltage at pin 7 (0°C 14 on Dip (0°C to +75°C)	+6.0 V
Count Input Pin Voltage	+4.0 V, -2.0 V
Reset Input Pin Voltage	+4.0 V, -2.0 V
Current into Each Output Terminal	± 5.0 mA

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

Parameter	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	3.3		5.5		
Count Input-Low			0.45	V	
Count Input-High	1.2			V	
Count Input Pulse Width-High	150			ns	
Count Input Slope-Positive Going	1.0			V/μs	
Maximum Count Input Frequency			2.0	MHz	
Reset Input-Low			0.45	V	
Reset Input-High	1.2			V	
Output-Low			0.35	V	I_{out} = 0.4 mA V_{CC} = 4.0 V
Output-High	1.4			V	I_{out} = -0.7 mA V_{CC} = 3.6 V
Power Consumption		140		mW	V_{CC} = 4.0 V
Count Input Impedance		2 kΩ in series with a transistor base-emitter diode			
Reset Input Impedance		300 Ω in series with a transistor base-emitter diode			
Maximum Delay from Count Input to Z_8 Output (count 7 to 8)		300 ns (Load: 2 kΩ parallel with 50 pF from each output to ground)			

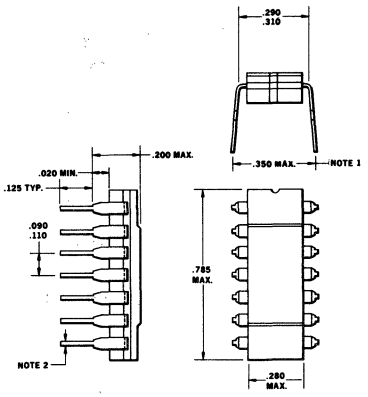
PHYSICAL DIMENSIONS
(SIMILAR TO TO-5)



NOTES: Dimensions as per latest JS-10 committee.
All dimensions in inches.
Leads are gold-plated kovar.
Package weight is 1.12 grams.

(PRODUCT CODE: U5B995879X)

TYPICAL DUAL IN-LINE PACKAGE



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

(PRODUCT CODE: U6A995879X)

*Planar is a patented Fairchild process.

NOTE:
(1) These ratings are limiting values above which serviceability of unit may be impaired.

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SEMICONDUCTOR
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RESET/PRESET

The circuit is reset to count 0 (all outputs high) with a high level at the reset input pin.

To preset an arbitrary count:

1. Reset to count 0 and then return the reset pin to a low level.
2. Ground (below 0.45 V) the appropriate outputs.

TO-5 CONNECTION DIAGRAM

(Top View)

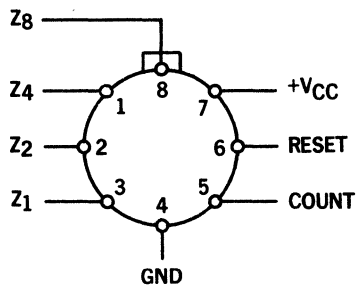
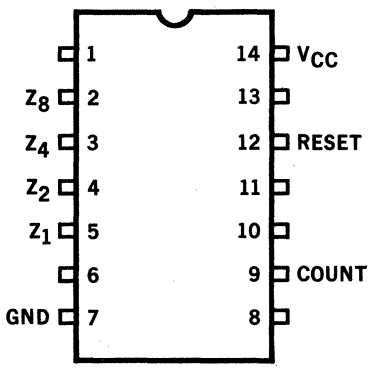


TABLE OF OUTPUT STATES

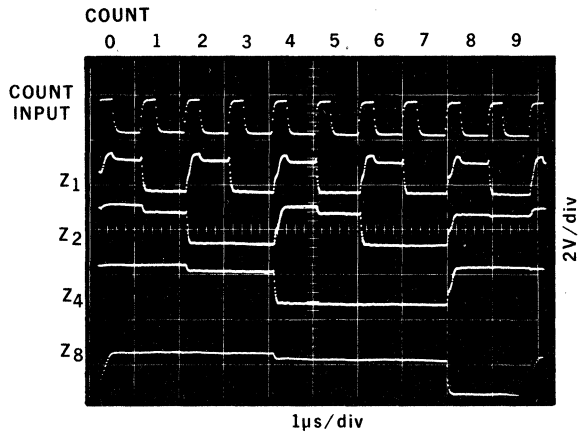
COUNT	0	1	2	3	4	5	6	7	8	9
Z_1	H	L	H	L	H	L	H	L	H	L
Z_2	H	H	L	L	H	H	L	L	H	H
Z_4	H	H	H	H	L	L	L	L	H	H
Z_8	H	H	H	H	H	H	H	H	L	L

(H=High, L=Low)

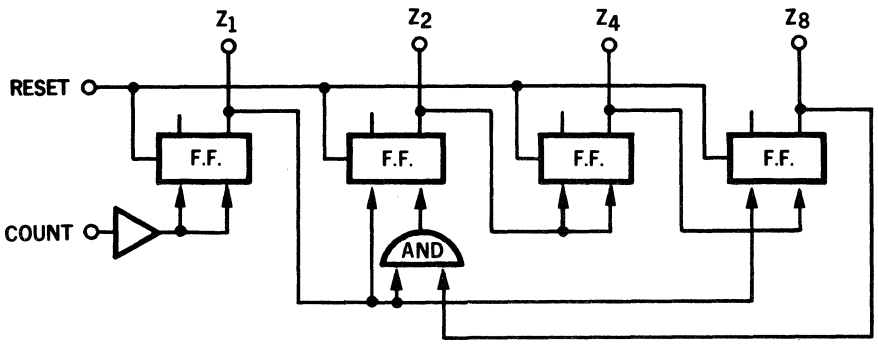
14 PIN DUAL IN-LINE CONNECTION DIAGRAM (TOP VIEW)



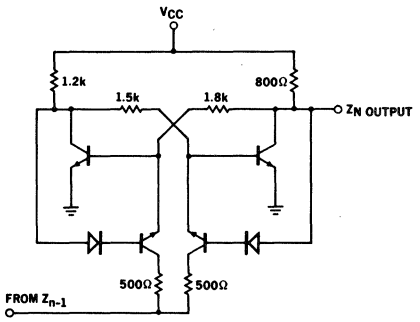
OUTPUT WAVEFORMS



BLOCK DIAGRAM

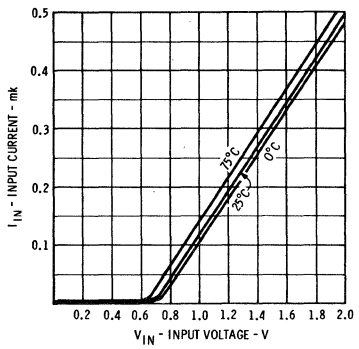


SCHEMATIC DIAGRAM OF DECADE FLIP-FLOP

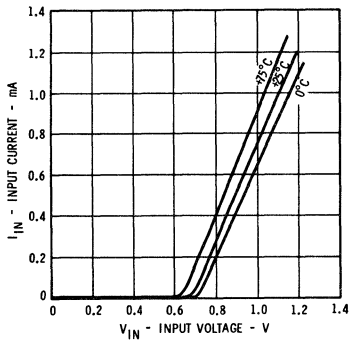


TYPICAL ELECTRICAL CHARACTERISTICS

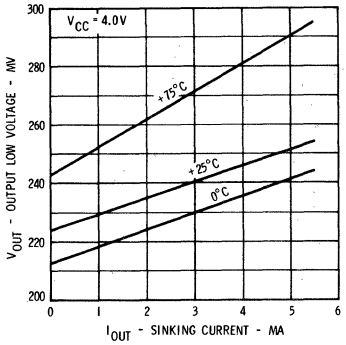
COUNT INPUT CHARACTERISTIC



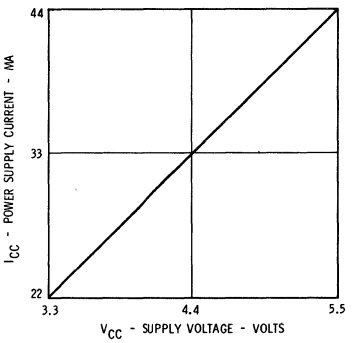
RESET INPUT CHARACTERISTIC



OUTPUT CHARACTERISTICS (OUTPUT LOW)



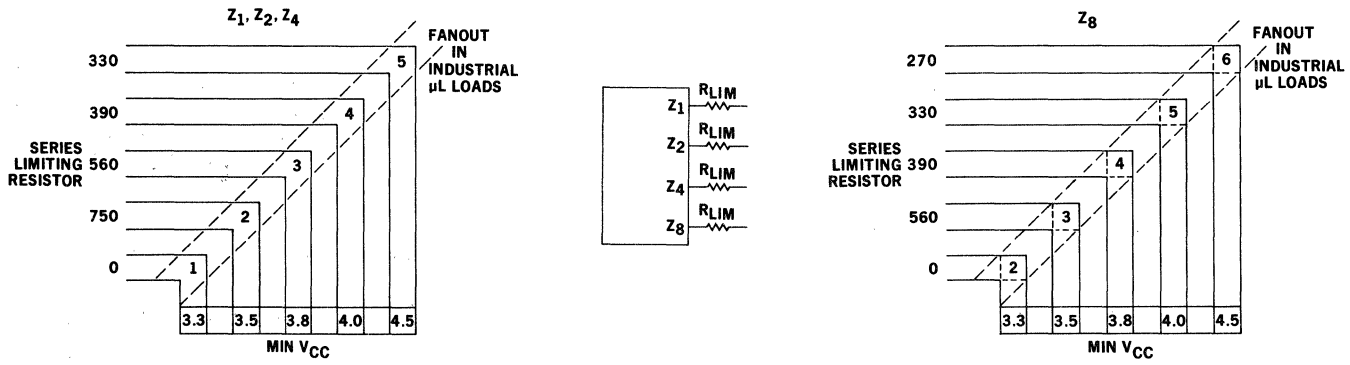
POWER SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



LOADING RULES

DRIVING DEVICE	AT V_{CC} OF	CAN DRIVE
CμL 9958:		
Z_1, Z_2, Z_4	3.3 Min.	1 CμL 9959
Z_8	3.3 Min.	1 CμL9959 plus 1 CμL 9958 Count Input
Z_1, Z_2, Z_4	4.0 Min.	2 CμL 9959
Z_8	4.0 Min.	2 CμL9959 plus 1 CμL 9958 Count Input
Z_1, Z_2, Z_4	4.0 V Min. and one 390 Ω current limiting resistor in series with each output	4 CμL 9959
Z_8	4.0 V Min. and one 330 Ω current limiting resistor in series with Z_8 output	4 CμL9959 plus 1 CμL 9958 Count Input
Z_1, Z_2, Z_4	3.3 Min.	1 CμL 9960
Z_8	3.3 Min.	1 CμL9960 plus 1 CμL 9958 Count Input
Z_1, Z_2, Z_4	4.0 Min.	2 CμL 9960
Z_8	4.0 Min.	2 CμL9960 plus 1 CμL 9958 Count Input
Z_1, Z_2, Z_4	4.0 Min. and one 330 Ω current limiting resistor in series with each output	5 CμL 9960
Z_8	4.0 Min. and one 270 Ω current limiting resistor in series with Z_8 output	5 CμL9960 plus 1 CμL 9958 Count Inputs
Industrial Range Milliwatt RTL:	3.6 V ± 10%	1 CμL9958 Count Input
Industrial Range RTL:	3.6 V ± 10%	6 CμL9958 Count Inputs, or 1 CμL 9958 Reset Input
Industrial Range DTL 6k Family:	4.5 Min.	1 CμL9958 Count Input
Industrial Range DTL 2k Family:	4.5 Min.	3 CμL9958 Count Inputs, or 1 CμL 9958 Reset Input

CμL 9958 FAN-OUT VERSUS V_{CC} AND SERIES LIMITING RESISTORS



FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

CμL9959

BUFFER - STORAGE ELEMENT

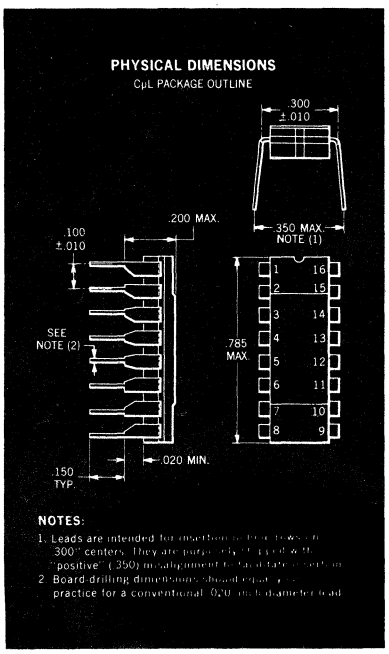
COUNTING MICROLOGIC® INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The CμL 9959 Buffer-Storage unit consists of four gated-latch circuits, and a common gate driver, diffused into a single silicon substrate. Information which is present at the four data inputs enters the latches throughout the interval of a load command applied to the gate input terminal. With gate high, information is stored until a subsequent load command permits a change.

The unit has eight output terminals (both true and complement for each storage position).

RULES FOR USE OF CμL9959

The principal intended use of the CμL9959 is with industrial and ground support systems, with operating V_{CC} from 3.3 to 5.0 volts, and from 0°C to +75°C ambient temperature. This temperature range may be extended to -55°C by raising minimum V_{CC} to 4.0 Volts or it may be extended to +125°C by lowering maximum V_{CC} to 4.4 Volts.



ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature	-55°C to +150°C
Supply Voltage (0°C to +75°C)	6.0 V
Gate Input and Data Input Pin Voltage	+4.0 V, -2.0 V
Current into Each Output Terminal	+15 mA
Voltage Applied to an Output Terminal	+6.0 V, -0.3 V

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

Characteristic	Min.	Typ.	Max.	Units	Conditions
Supply Voltage	3.3	3.8	5.0	V	
Power Consumption		115		mW	V_{CC} = 3.8 V Gate High
Power Consumption		135		mW	V_{CC} = 3.8 V Gate Low
Gate Input High	1.1			V	
Gate Input Low			0.5	V	
Data Input High	1.0			V	
Data Input Low			0.5	V	
Output Low			0.4	V	I_{OUT} = 3.0 mA, V_{CC} = 5.0 V
Output Low		0.6		V	I_{OUT} = 10 mA
Load Current	-0.4			mA	V_{OUT} = 1.5 V, V_{CC} = 3.3 V
Max. Sampling Rate		>5.0		MHz	
Sampling Pulse Width (Gate)	100			ns	

NOTES:

(1) These ratings are limiting values above which severiceability of unit may be impaired.

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TRUTH TABLE

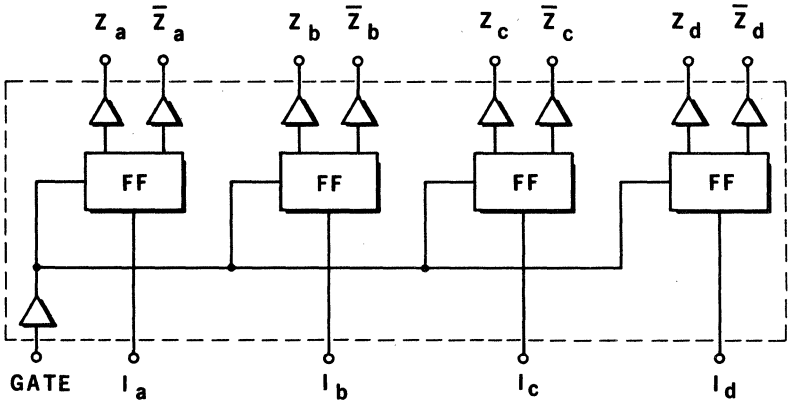
GATE	I	Z	$\overline{Z}$
L	L	L	H
L	H	H	L
H	ANY	Q	$\overline{Q}$

H = HIGH

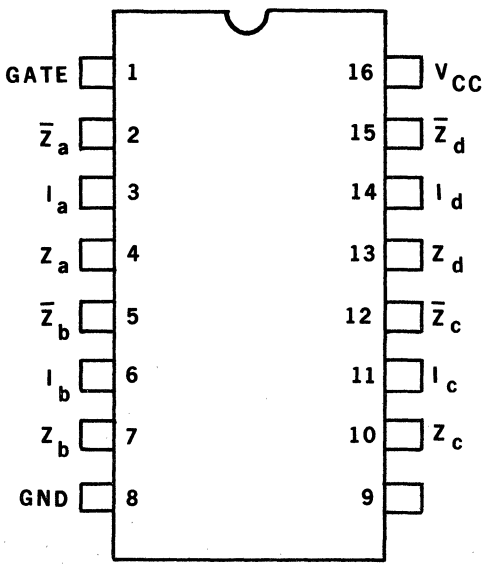
L = LOW

Q = THE STATE ASSUMED PRIOR TO "GATE HIGH" IS MAINTAINED.

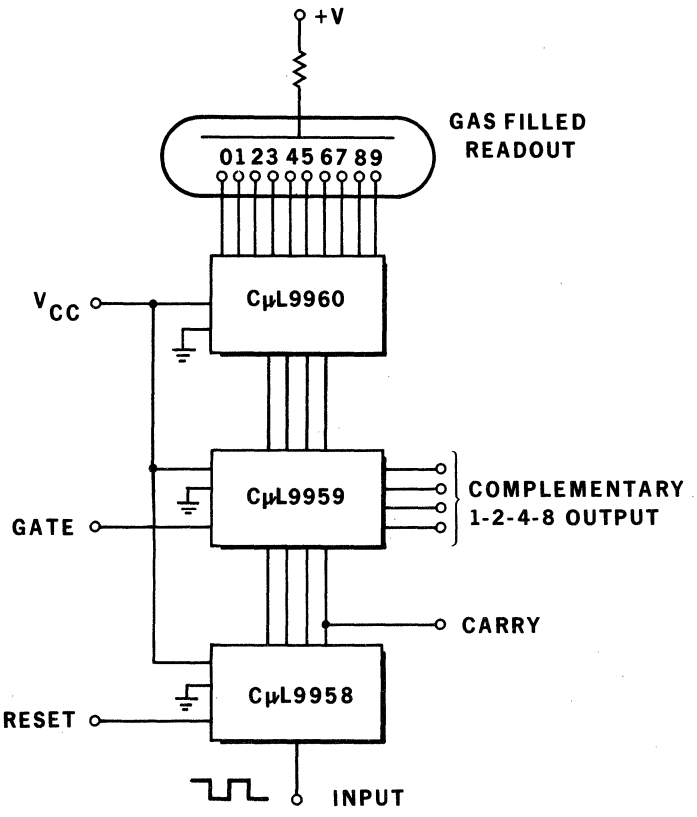
BLOCK DIAGRAM



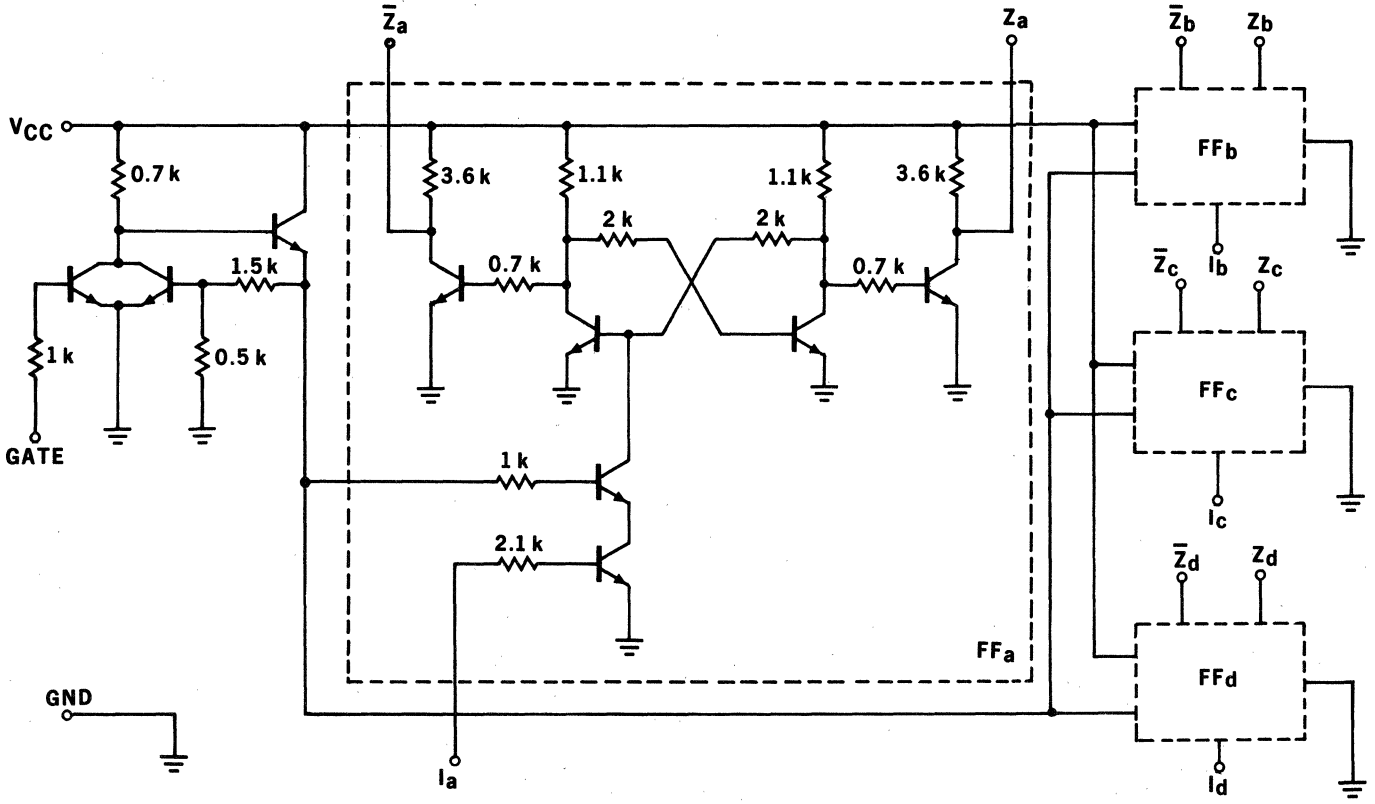
16 PIN DUAL IN-LINE PACKAGE (TOP VIEW)



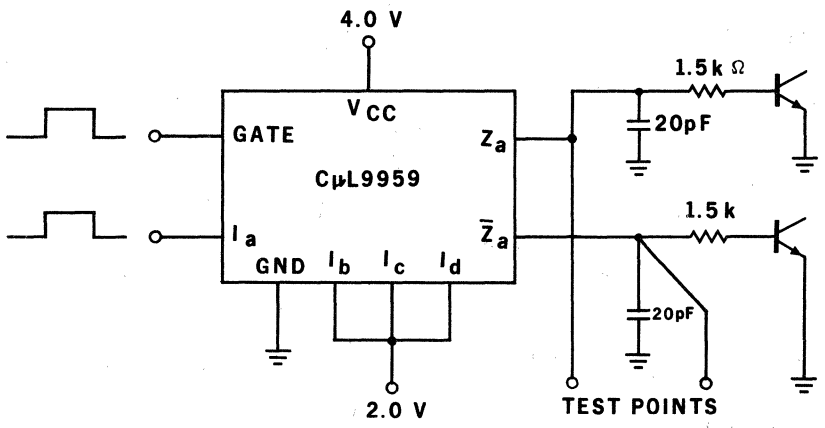
TYPICAL APPLICATION



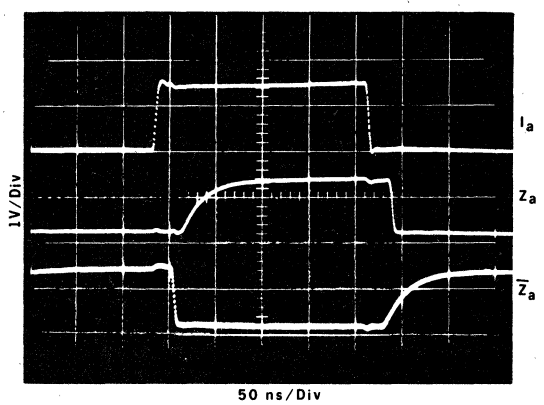
SCHEMATIC DIAGRAM OF BUFFER STORAGE UNIT



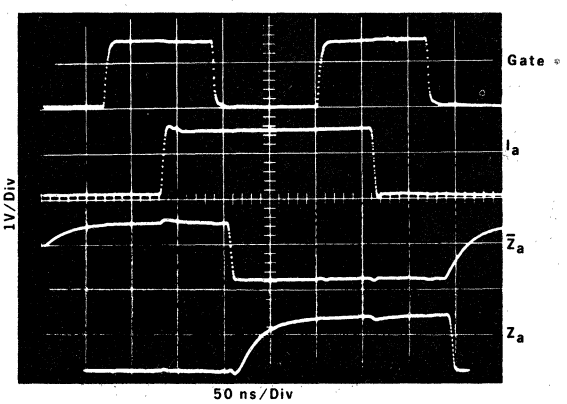
PROPAGATION DELAY



Delay from data Input to Output (Gate input low)

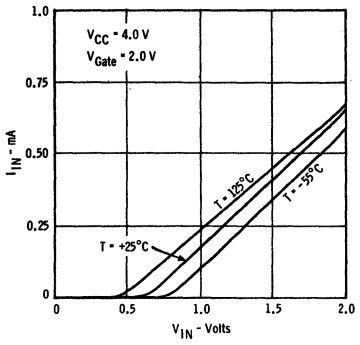


Delay from Gate Input to Output

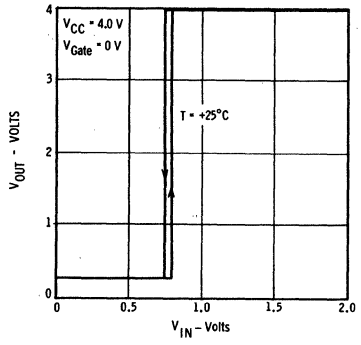


TYPICAL ELECTRICAL CHARACTERISTICS

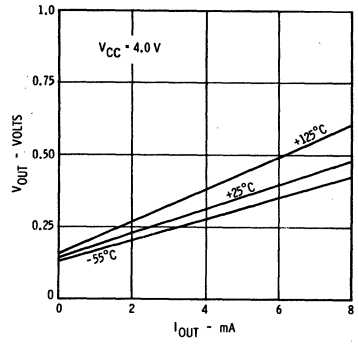
DATA INPUT CHARACTERISTIC



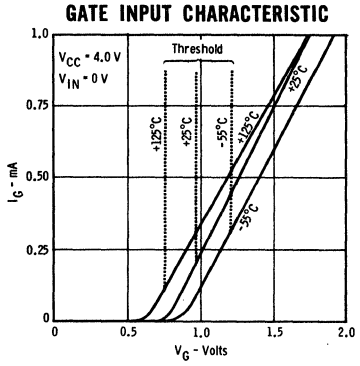
TRANSFER CHARACTERISTIC



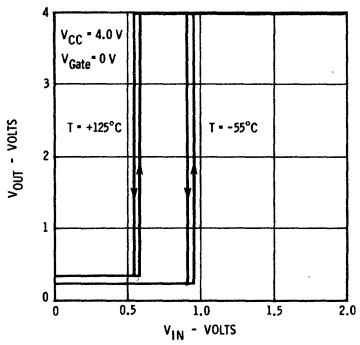
OUTPUT CHARACTERISTIC (OUTPUT LOW)



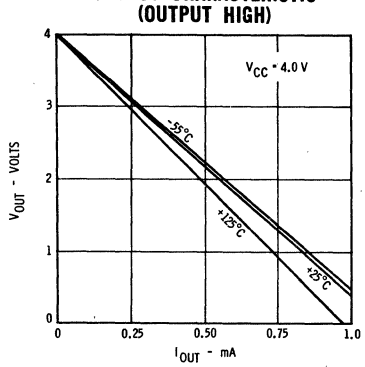
GATE INPUT CHARACTERISTIC



TRANSFER CHARACTERISTIC



OUTPUT CHARACTERISTIC (OUTPUT HIGH)



LOADING RULES FOR CμL9959

Driving Device	At V_{CC} of	Can Drive:
9959	3.3 to 5.0 V	2 9960 inputs ts
9959	3.3 to 5.0 V	4 Low Power RTμL loads
9959	3.3 to 5.0 V	1 RTμL load
9959	3.3 to 5.0 V	2 DTμL loads
9958	3.6 to 4.0 V	2 9959 data inputs
Full Range Low Power RTμL	4.0 V Min.* at -55°C	3 9959 data inputs or 1 9959 gate input
Industrial Range Low Power RTμL	3.6 V ± 10%	2 9959 data inputs
Full Range RTμL	3.0 ± 10%	10 9959 data inputs or 3 9959 gate inputs
Industrial Range RTμL	3.6 ± 10%	13 9959 data inputs or 5 9959 gate inputs
Full Range DTμL 6 K Family	4.5 V Min.	2 9959 data inputs or 1 9959 gate input
Full Range DTμL 2 K Family	4.5 V Min.	6 9959 data inputs or 2 9959 gate inputs

*See Low Power RTμL data sheet for details.

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CμL9960

DECIMAL DECODER/DRIVER

COUNTING MICROLOGIC® INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The CμL 9960 Decoder/Driver is a monolithic silicon circuit which accepts 1-2-4-8 binary coded decimal inputs at integrated circuit signal levels and produces ten mutually exclusive outputs which can directly control the ionizing potentials of many gas filled cold cathode indicator tubes. The CμL 9960 is designed specifically for use with the CμL 9958 Decade Counter or CμL 9959 Buffer-Storage, but can be used with other integrated circuit types. Only true values are required as inputs thereby simplifying the connection with counters or other information sources.

RULES FOR USE OF CμL 9960

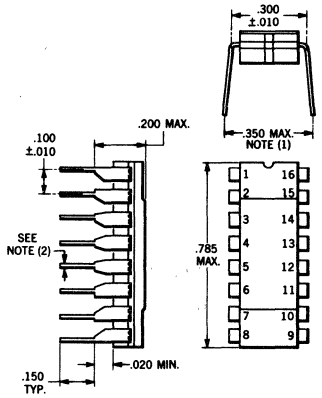
The principal intended use of the CμL 9960 is with industrial and ground support systems, from 0°C to +75°C ambient, and with operating V_{CC} from 3.3 to 5.5 volts. The lower limit of the temperature range may be extended to −55°C by raising the minimum V_{CC} to 4.0 volts.

ABSOLUTE MAXIMUM RATINGS (Note 1)

	Storage Temperature	−55°C to +125°C
	Operating Temperature	0°C to +75°C
	Supply Voltage (0°C to +75°C)	6 V
	Input Voltage	+4 V, −2 V
I_{OL}	Current into each Output Terminal (In the ON State)	15 mA
I_{OH}	Current into each Output Terminal (In the OFF State) (Notes 2 and 3)	0.6 mA

PHYSICAL DIMENSIONS

CμL PACKAGE OUTLINE



NOTES:

1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

PRODUCT CODE: U6B996079X

ELECTRICAL CHARACTERISTICS (25°C Free Air Temperature unless otherwise noted)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Conditions
V_{CC}	Power Supply (Note 4)	3.3		5.5	V	
P_D	Power Consumption		45		mW	V_{CC} = 4.0 V Input High
V_{IH}	Input High	1.0			V	
V_{IL}	Input Low			0.4	V	
V_{OL}	ON Output Voltage (Note 2)			4.0	V	V_{IH} = 1.0 V, I_{OL} = 3 mA
V_{OH}	OFF Output Voltage	55			V	I_{OH} = 0.2 mA
I_{CO}	OFF Output Leakage Current			50	μA	V_{OUT} = 0.2 mA

NOTES:

(1) These ratings are limiting values above which serviceability of unit may be impaired.

(2) Outputs in the OFF state Must not be left floating, they should be tied to V_{CC} through 10kΩ if they are not connected to the cathodes of a readout tube.

(3) Total current through all 9 outputs in the OFF state must not exceed 1.5 mA.

(4) For operation using gas filled readout tubes requiring 6 to 10mA ON current, V_{CC} Min. = 4.0 V.

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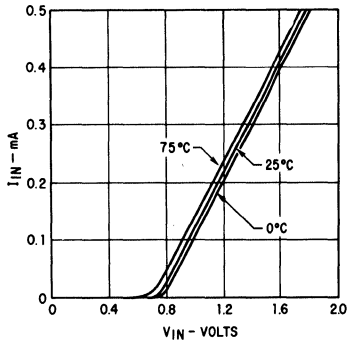
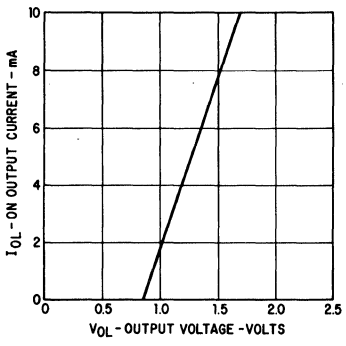
TYPICAL ELECTRICAL CHARACTERISTICS

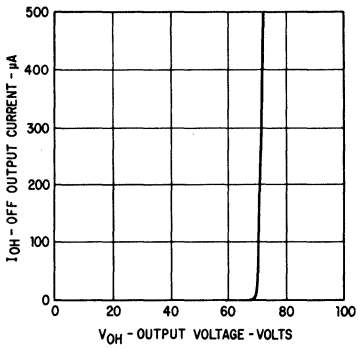
INPUT CHARACTERISTICS



ON OUTPUT CURRENT VERSUS OUTPUT VOLTAGE



OFF OUTPUT CURRENT VERSUS OUTPUT VOLTAGE



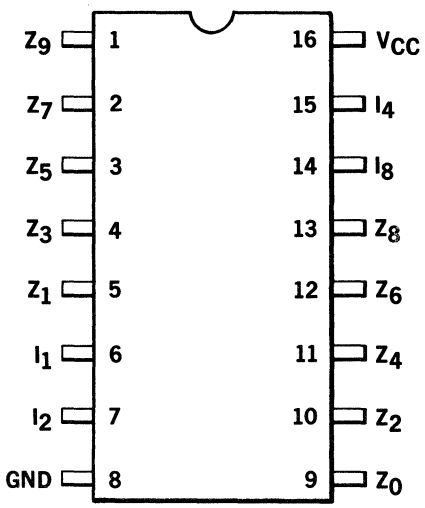
TRUTH TABLE

With the coding shown in the table only one of the outputs will be low or On at any time.

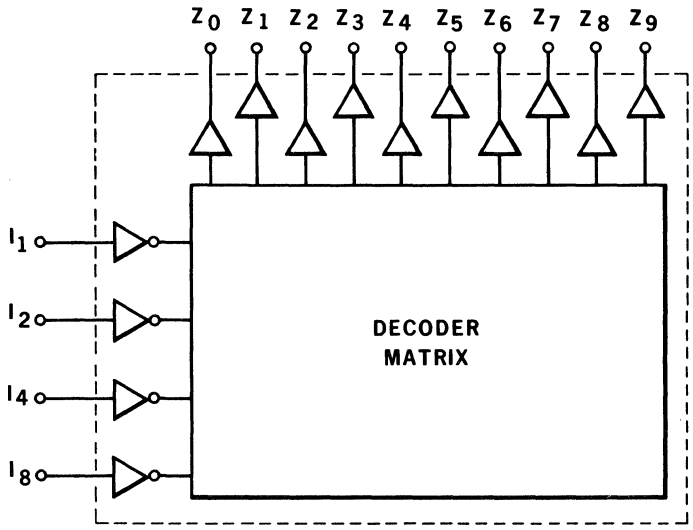
I_1	H	L	H	L	H	L	H	L	H	L
I_2	H	H	L	L	H	H	L	L	H	H
I_4	H	H	H	H	L	L	L	L	H	H
I_8	H	H	H	H	H	H	H	H	L	L
ON Output	Z_0	Z_1	Z_2	Z_3	Z_4	Z_5	Z_6	Z_7	Z_8	Z_9

L = Low
H = High

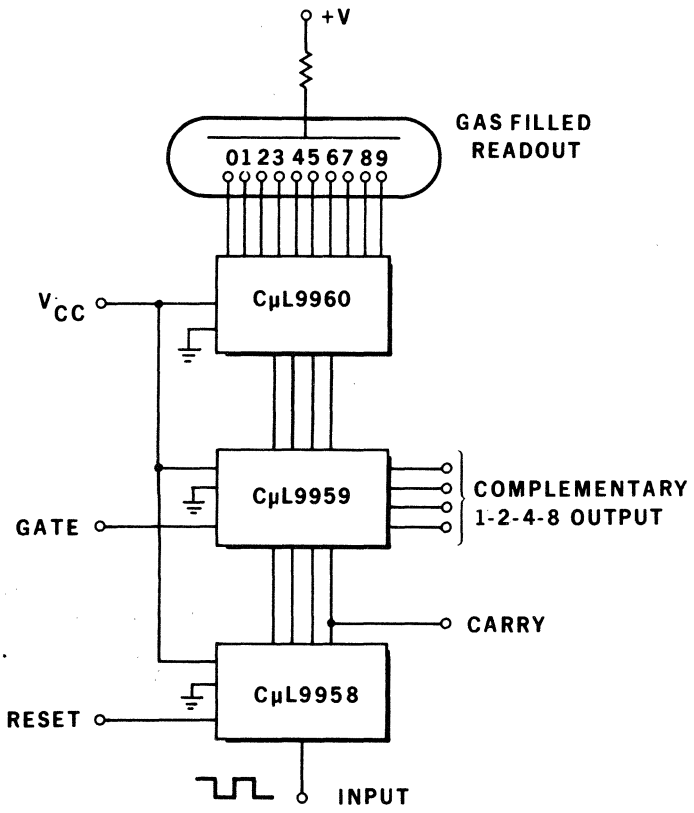
16 PIN DUAL IN-LINE PACKAGE
(Top View)

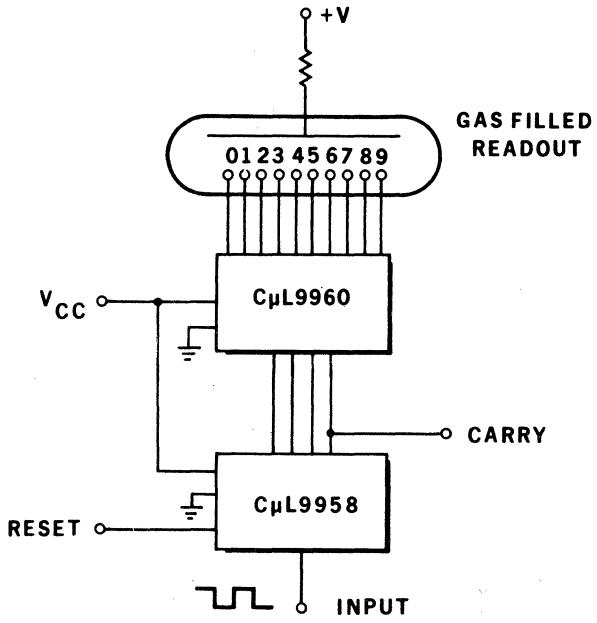


BLOCK DIAGRAM



TYPICAL APPLICATIONS





* The CμL9960 is suitable for driving all commercial available numeric gas filled readout tubes in which ON Cathode current does not exceed 10mA and **total** OFF Cathode leakages do not exceed 1.5mA. The Values of +V and R may be chosen following the readout tube manufacturers' specifications.

LOADING RULES FOR CμL9960

Driving Device	At V_{CC} of	
CμL9959	3.3 to 5.5 V	2 CμL9960 inputs
CμL9958	3.3 to 5.5 V	1 CμL9960 plus 1 CμL9958 Count Input
Industrial Range Milliwatt RTL	3.6 V ±10%	1 CμL9960
Industrial Range RTL	3.6 ±10%	6 CμL9960
Industrial Range DTμL 6K Family	4.5 V Min.	1 CμL9960
Industrial Range DTμL 2K Family	4.5 V Min.	3 CμL9960

CμL9989

4-BIT BINARY COUNTER

COUNTING MICROLOGIC® INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The CμL9989 is a Ripple Counter using 8421 binary weighted count sequence consisting of four cascaded binary triggered flip-flops. Provision is made for clearing and pre-setting any one of the possible binary states. The monolithic structure employs only resistors and transistors and is manufactured with Fairchild Planar* Epitaxial process to assure maximum performance and reliability.

The CμL9989 counter is designed to operate in the 0°C to 75°C temperature range with nominal power supply voltage of 3.6 to 5.5 volts.

The CμL9989 is available in the hermetically sealed 14 pin Dual In-Line ceramic package (TO-116), and in the 8 pin modified TO-5 metal can (TO-99).

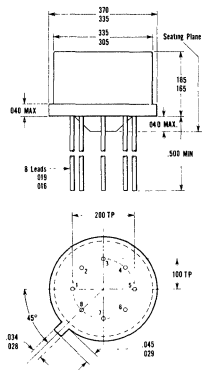
ABSOLUTE MAXIMUM RATINGS (above which useful life may be impaired)

Storage Temperature	−55°C to +150°C
Voltage at pin 7 (0°C to +75°C) (TO-99)	+6.0 V
Count Input Pin Voltage	+4.0 V, −2.0 V
Reset Input Pin Voltage	+4.0 V, −2.0 V
Current into Each Output Terminal	±5.0 mA

ELECTRICAL CHARACTERISTICS (0 - 75°C Free Air Temperature unless otherwise stated)

PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Supply Voltage—V_{CC}	3.6		5.5	Volts	See Loading Rules
Power Dissipation		300	385	mW	V_{CC} = 5.5 Volts, 25°C
Power Dissipation		132		mW	V_{CC} = 4.0 Volts, 25°C
Count Input—Low—V_{ILC}			0.45	Volts	75°C
Count Input—High—V_{IHC}	1.2			Volts	25°C
Count Input Current		210	330	μA	25°C, V_{IHC} = 1.2 Volts
Count Input Pulse Width—High	40			ns	25°C
Count Input Slope—Positive Going		1.0		v/μs	25°C
Max. Freq. of Input Count Pulses	10	15		MHz	Z_1, Z_2, Z_4, One Standard Load
					Z_8, Two Standard Loads
Reset Input—Low—V_{ILR}			0.45	Volts	75°C
Reset Input—High—V_{IHR}	1.2			Volts	25°C
Reset Input Current		1.45	2.30	mA	25°C, V_{IHR} = 1.2 Volts
Reset Input Pulse Width—High		220		ns	Z_1, Z_2, Z_4, One Standard Load
					Z_8, Two Standard Loads, V_{CC} = 5.5 Volts
Output—Low—V_{OL}			0.45	Volts	V_{CC} = 5.5 Volts, I_{OL} = 0.4 mA Load
Output—High—V_{OH}	1.2			Volts	V_{CC} = 3.5 Volts, I_{OH} = −0.7 mA
Max. Delay From Count Input To Z_8 Output		90	120	ns	V_{CC} = 4.0 Volts, Z_1, Z_2, Z_4 One Standard Load, Z_8 Two Standard Loads 25°C

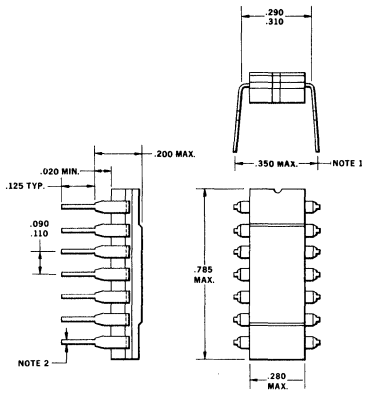
PHYSICAL DIMENSIONS
(TO-99)



NOTES. Dimensions as per latest JS-10 committee
All dimensions in inches
Leads are gold-plated kovar
Package weight is 0.95 grams.

(PRODUCT CODE U5B998979X)

TYPICAL DUAL IN-LINE PACKAGE
(TO-116)



NOTES:
1 Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2 Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

(PRODUCT CODE U6A998979X)

*Planar is a patented Fairchild process.

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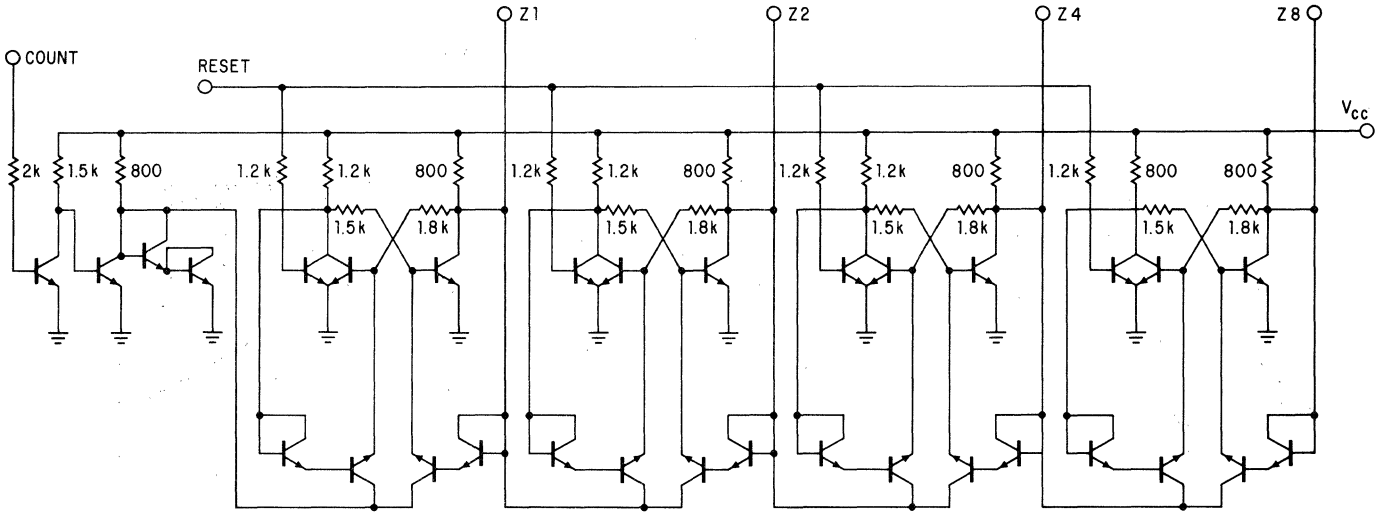
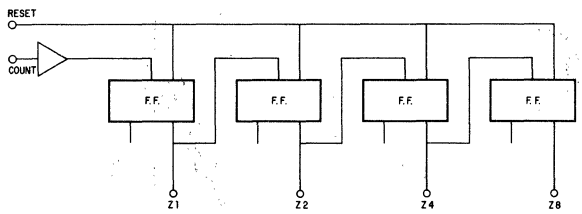
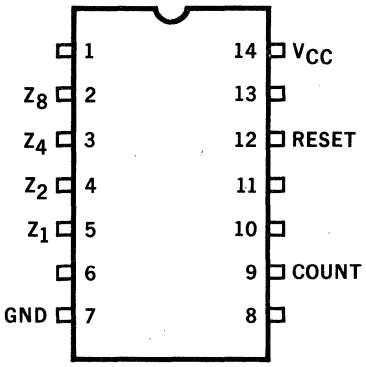
SCHEMATIC DIAGRAM



LOGIC DIAGRAM



14 PIN DUAL IN-LINE CONNECTION DIAGRAM (Top View)



TO-99 CONNECTION DIAGRAM (Top View)

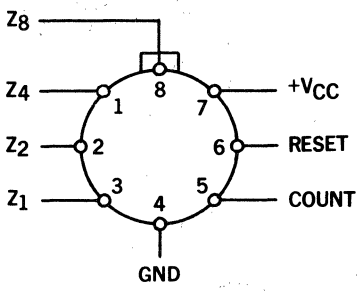
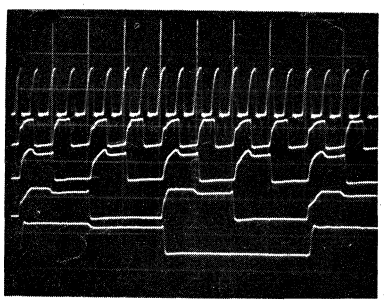


TABLE OF OUTPUT STATES

COUNT (H = High, L = Low)

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Z_1	H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
Z_2	H	H	L	L	H	H	L	L	H	H	L	L	H	H	L	L
Z_4	H	H	H	H	L	L	L	L	H	H	H	H	L	L	L	L
Z_8	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L

INPUT/OUTPUT WAVEFORM



RESET/PRESET

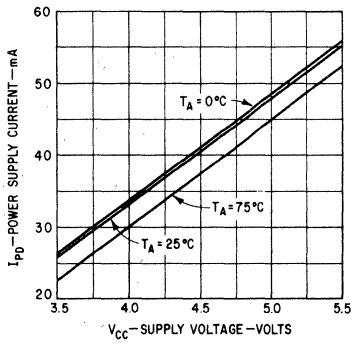
The circuit is reset to count 0 (all outputs high) with a high level at the reset input pin.

To preset an arbitrary count:

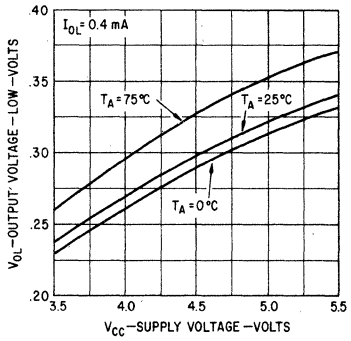
1. Reset to count 0 and then return the reset pin to a low level.
2. Ground (below 0.45 V) the appropriate outputs.

TYPICAL ELECTRICAL CHARACTERISTICS

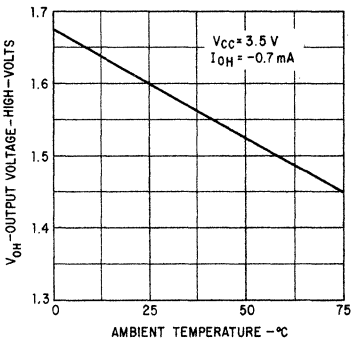
POWER SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



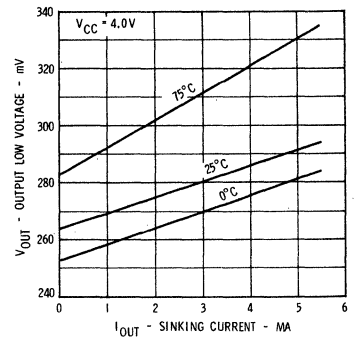
OUTPUT VOLTAGE—LOW VERSUS SUPPLY VOLTAGE



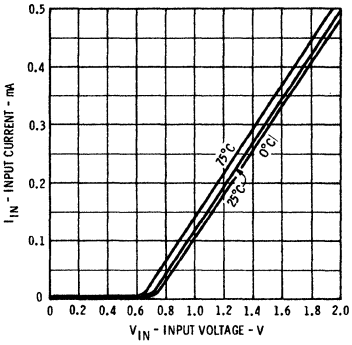
OUTPUT VOLTAGE—HIGH VERSUS TEMPERATURE



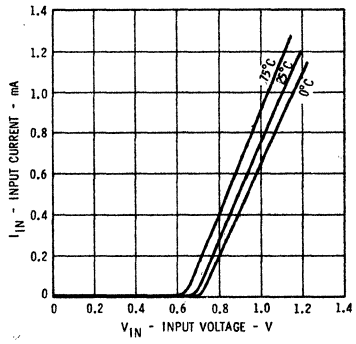
OUTPUT CHARACTERISTICS (OUTPUT LOW)



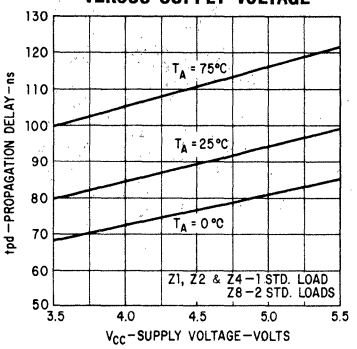
COUNT INPUT CHARACTERISTIC



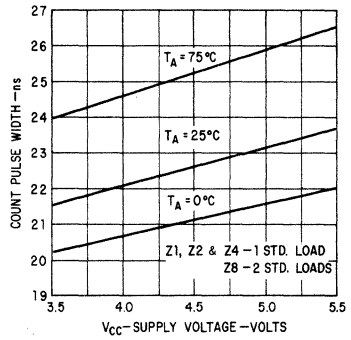
RESET INPUT CHARACTERISTIC



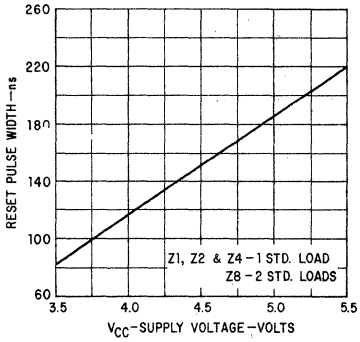
PROPAGATION DELAY—t_{pd} VERSUS SUPPLY VOLTAGE



COUNT PULSE WIDTH VERSUS SUPPLY VOLTAGE



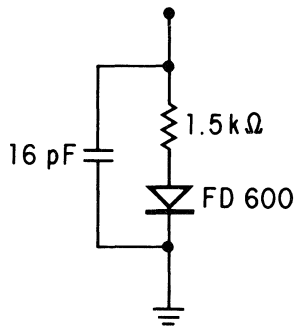
RESET PULSE WIDTH VERSUS SUPPLY VOLTAGE



LOADING RULES

DRIVING DEVICE	CAN DRIVE	AT V_{CC} RANGE OF
CμL9989		
Z_1, Z_2, Z_4	Open	
Z_8	1 Standard Load	3.6 to 5.5 Volts
CμL9989		
Z_1, Z_2, Z_4	1 Standard Load	
Z_8	2 Standard Loads	4.0 to 5.5 Volts
CμL9989		
Z_1, Z_2, Z_4	2 Standard Loads	
Z_8	4 Standard Loads	5.0 to 5.5 Volts
Industrial Range		
Milliwatt RTL	1 CμL9989 Count	3.6 to 3.96 Volts
Industrial Range	6 CμL9989 Count	
RTL	1 CμL9989 Reset	3.6 to 3.96 Volts
Industrial Range		
DTL 6K Family	1 CμL9989 Count	4.5 to 5.5 Volts
Industrial Range	3 CμL9989 Count	
DTL 2K Family	1 CμL9989 Reset	4.5 to 5.5 Volts

One Standard Load, worst case, is defined for testing purposes as shown in the figure below.



The following are defined as One Standard Load:

CμL9989 Count Input
CμL9958 Count Input
CμL9959 Data Input
CμL9960 Data Input
LP-RTL GATE INPUT

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

9997 FOUR BIT SHIFT REGISTER

INDUSTRIAL MICROLOGIC® INTEGRATED CIRCUIT

OPERATING TEMPERATURE RANGE 0°C TO 70°C

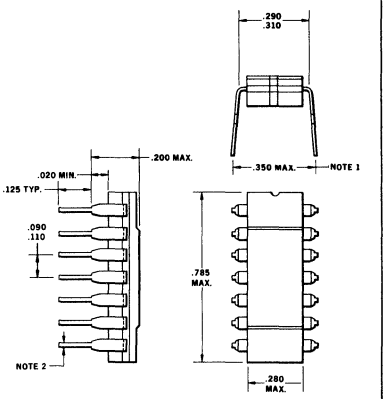
GENERAL DESCRIPTION — The Micrologic® Integrated Circuit Four-Bit Shift Register is a fully integrated, monolithic digital circuit which is manufactured using the patented Fairchild Planar* epitaxial process.

THE 9997 FOUR-BIT SHIFT REGISTER consists of four series connected Flip-Flops and the circuitry required for triggering and resetting the Flip-Flops. Each Flip-Flop has a common reset input, a parallel (asynchronous) input, data input, and a non-inverted, buffered output which receives power from a separate voltage supply (V_{CC}') that is common to all outputs.

The separate voltage supply (V_{CC}') is independent of the V_{CC} terminal, i.e., the circuit will operate with $V_{CC} = 5.5V$ and $V_{CC}' = 3.3V$ or $V_{CC} = 3.3V$ and $V_{CC}' = 5.5V$, etc.

Typical applications include: Serial shifting, parallel shifting (static storage register), serial input-parallel output, parallel input-serial output, and shift counters.

TYPICAL DUAL IN-LINE PACKAGE
(In accordance with JEDEC TO—116)



NOTES:
1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

PURCHASING INFORMATION:

To order this device specify U6A999729X.

FEATURES

- **SERIAL OPERATION WITH PARALLEL ENTRY TO ALL BITS**
- **ASYNCHRONOUS GANGED RESET CAPABILITY**
- **WIDE V_{CC} RANGE — COMPATIBLE OPERATION WITH SEVERAL LOGIC FAMILIES**
- **OUTPUTS CAN BE GATED**
- **SINGLE LINE SERIAL INPUT**
- **HANDLES BLOCKS OF FOUR BITS OF DATA COMMON TO MANY PARALLEL/SERIAL AND SERIAL/PARALLEL OPERATIONS**
- **CAN DRIVE 40 CCSL UNIT LOADS**

ELECTRICAL CHARACTERISTICS

Operating Voltage Range	3.3 to 5.5 Volts
Minimum Shifting Rate	D.C. to 5.0 MHz
Typical Shifting Rate	D.C. to 7.0 MHz
Maximum Power Dissipation ($V_{CC}' = V_{CC}$)	380 mW
Maximum Power Dissipation (V_{CC}' = open)	260 mW

NORMAL OPERATION

SERIAL SHIFTING — A high to low voltage transition at the trigger input (T) initiates the following simultaneous state transfers: $D \rightarrow Q_1$, $Q_1 \rightarrow Q_2$, $Q_2 \rightarrow Q_3$, and $Q_3 \rightarrow Q_4$.

RESET AND PARALLEL ENTRY — A high voltage level at the reset input (R) overrides all other inputs and causes all four Flip-Flops to be reset such that the Q_1, Q_2, Q_3, and Q_4 outputs assume a high voltage level and remain high after removal of the reset signal. After removal of the reset signal, a high voltage level at a set input (S_1 through S_4) will cause each Flip-Flop to be set such that its corresponding output (Q_1 through Q_4) will be at a low voltage level. No change of state will occur if a set input is at a low signal level.

Note that since the buffered outputs receive power from a separate voltage supply they can be gated (or enabled) by gating the voltage applied to Pin 13. This feature is useful from a logical viewpoint, as well as a power conservation consideration. The gated emitter-follower circuit shown on the back of this sheet is recommended.

* Planar is a patented Fairchild process.

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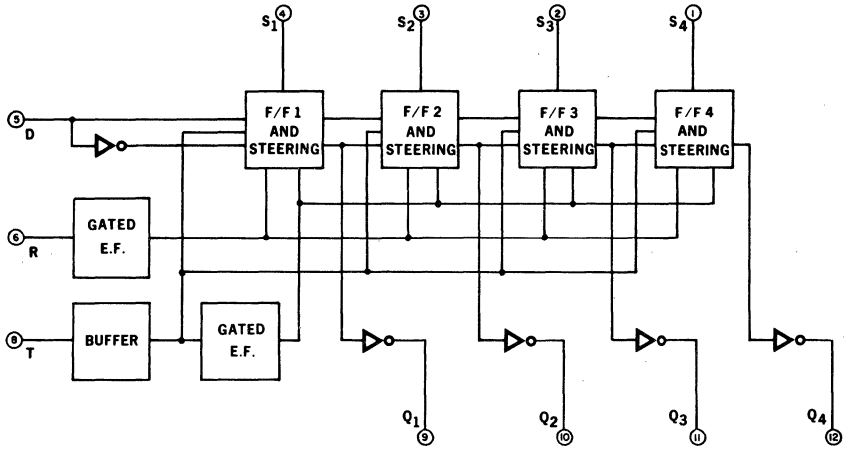
313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

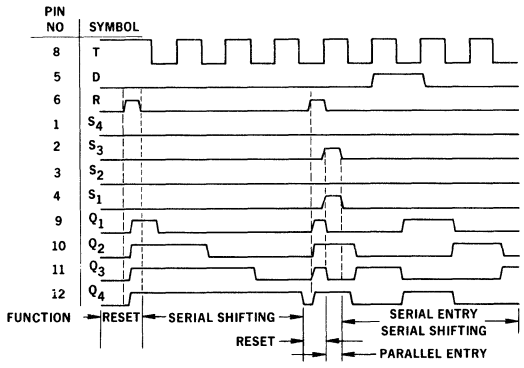
9997 FOUR BIT SHIFT REGISTER

BLOCK DIAGRAM

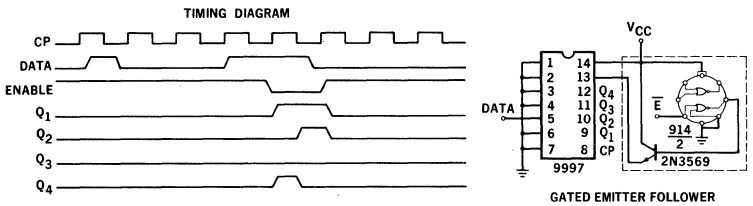


FOUR BIT SHIFT REGISTER (PRODUCT CODE 9997) BLOCK DIAGRAM

TYPICAL TIMING DIAGRAM

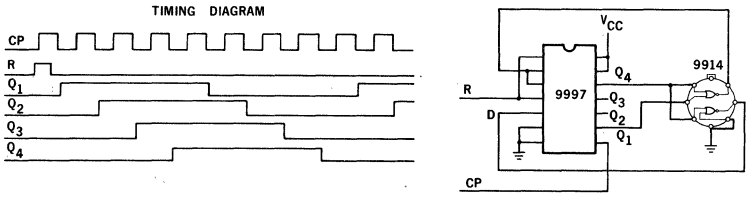


SERIAL SHIFT REGISTER WITH GATED OUTPUTS.



GATED EMITTER FOLLOWER

MODULO 8 SHIFT REGISTER COUNTER
(Shifting Rate Test Circuit)



MμL9030

8-BIT MEMORY CELL

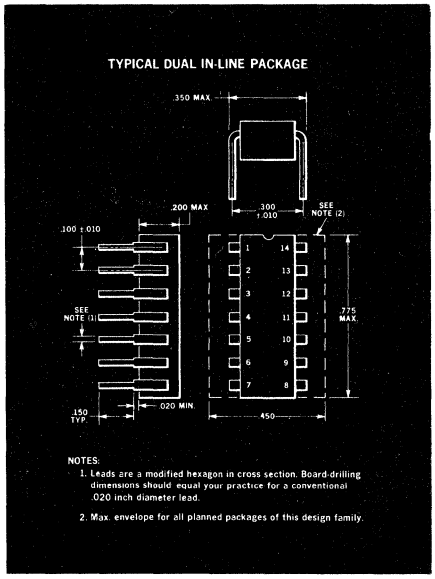
MEMORY MICROLOGIC® INTEGRATED CIRCUITS

GENERAL DESCRIPTION - The MμL9030 is a Planar* epitaxial integrated 8-bit (non-destructive readout) memory cell consisting of four 2-bit words. The cell is addressable by word. It is permissible to write into one word while reading another. The same information may also be written in two words simultaneously. The "Write" time for a cell is 45 nanoseconds maximum and the "Read" delay is 25 nanoseconds.

The element is fully compatible with Fairchild CTμL Circuits. The "Read" and "Data" inputs are the equivalent of 1.5 CTμL gate loads, and the "Write" inputs, 3 CTμL gate loads. The outputs can drive 3 CTμL gate loads.

For applications where faster "Readout" speed is essential, the users are encouraged to investigate the properties of the CTμL968 Integrated Dual Latch.

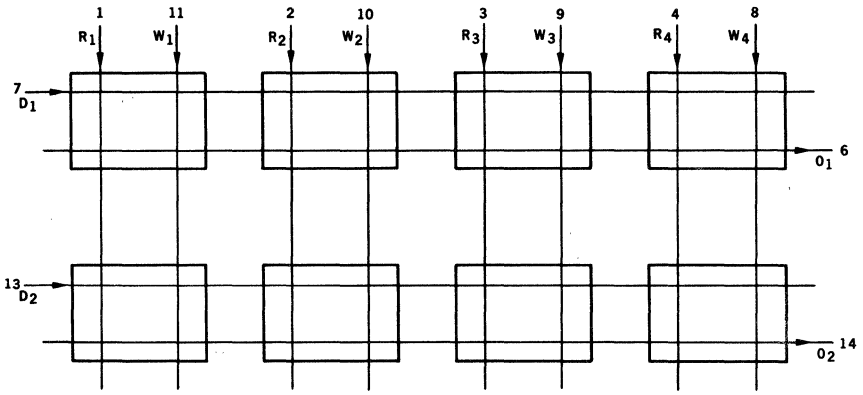
*Planar is a Patented Fairchild Process.



LOGIC DIAGRAM AND PIN ARRANGEMENTS

D_1, D_2: DATA INPUTS
R_1, R_2, R_3, R_4: READ INPUTS
W_1, W_2, W_3, W_4: WRITE INPUTS
O_1, O_2: OR–ABLE OUTPUTS

V_{CC} = PIN 12
GND = PIN 5



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D.C. TESTS (V_{CC} = 4.5 V, T = 25°C)

DESCRIPTION	TEST	CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS	EQUIV CTμL LOAD
Read Input Current	I_1, I_2, I_3, I_4	V_1, V_2, V_3, V_4 = 2.5 V		4.4	mA ea.	1.5
Data Input Current	I_7, I_{13}	V_7, V_{13} = 2.5 V		4.4	mA ea.	1.5
Write Input Current	I_8, I_9, I_{10}, I_{11}	V_8, V_9, V_{10}, V_{11} = 2.5 V		8.8	mA ea.	3
Output Voltage (High State)	V_6, V_{14}	I_6, I_{14} = -10 mA	2.35		V	
Output Voltage (Low State)	V_6, V_{14}	I_6, I_{14} = -1 mA		-0.36	V	
Output Leakage	I_6, I_{14}	V_6, V_{14} = 4 V		5	μA	
Output Capacitance	C_6, C_{14}	V_6, V_{14} = 0 Boonton Bridge		8	pF	

INPUT LEVEL: Maximum permissible "low" level = 0.8 V. Maximum required "high" level: 1.25 V.

RECOMMENDED OPERATING CONDITIONS:

The above test specifications characterize the terminal properties of the circuit under one set of conditions. They in no way limit the circuit to be used under different conditions where certain advantages may be achieved. In general, excessive heat generated in the circuit presents the largest factor in degrading the performance of the circuit. For noise immunity greater than 0.5 V and operating speed within 20% of 25°C speed, junction temperature must be kept within 0-125°C. The circuit dissipates 350 mW with V_{CC} = 4.5 V ± 10% and full load. (F/O = 3 CTμL Gates.)

Maximum thermal resistances of the package from junction to air are:

100°C/W in still air 65°C/W with 200 feet/min air flow 50°C/W with 400 feet/min air flow

For example, the circuit may be operated in still air at T_A = 90°C with V_{CC} = 4.5 V ± 10%. Higher ambient temperatures are possible in moving air, as can be calculated from the data above.

The outputs of the MμL 9030 may be "OR-ed" with the outputs of different words. Each output terminal represents 8 pF capacitance and 5 μA leakage current. The limit on OR-tying outputs is the degradation of switching speed that the user can tolerate due to added capacitance.

Fan-out of the MμL 9030 can be increased to 15 with only a slight increase in delay by buffering with the CTμL 965.

SWITCHING TIME:

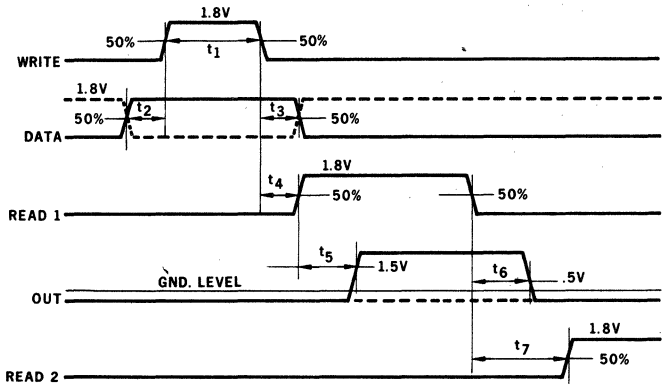
Load Resistance: 1 k to -2 V — Load Capacitance: 10 pF probe and jig capacitance — Input waveform rise and fall time: 6 ns

These tests are for correlations only. While t_1 through t_4 do not change with varied loads, t_5, t_6, and t_7 may differ under different output loading conditions.

SWITCHING TIME:

t_1: 25 ns MIN.
t_2: 10 ns MIN.
t_3: 10 ns MIN.
t_4: 10 ns MIN.
t_5: 25 ns MAX.
t_6: 25 ns MAX.
t_7: 25 ns MIN.

NOTE:
1) DOTTED LINES REPRESENT CELL STORING "LOW" LEVEL.
2) t_7 REPRESENTS TIME INTERVAL BETWEEN READ PULSES FOR ERROR-FREE READOUT.



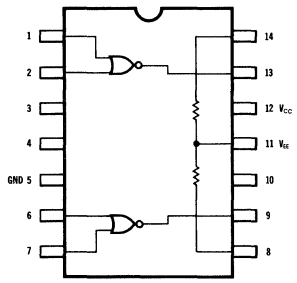
SPECIAL CIRCUITS COMING SOON

Type	Function	Type	Function
CTL9852	Dual NOR Gate	CTL9871	Quad 2 Input AND Gates, W/OR Tied Pairs
CTL9853	Triple AND Gate	CTL9872	Same as 9866 but without 2K Load or Input Resistors
CTL9854	Dual 4-Input AND Gate		
CTL9855	8-Input AND Gate	CTL MSI	1 Out of 8 Decoder
CTL9856	Dual Buffer	CTL MSI	4 Bit Comparator
CTL9864	Dual 3 & Single Input AND Gate	CTL MSI	4 Bit Multiplexer
CTL9865	Quad Single Input AND Gate	CTL MSI	4 Bit Latch
CTL9866	Quad 2 Input AND Gates, One Pair W/OR Tie	CTL MSI	Dual Full Adder

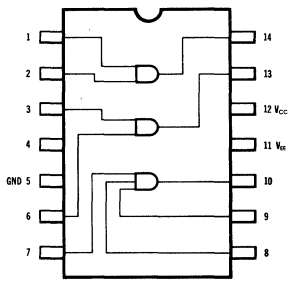
CTL II

The first CTL II circuits to be announced will be pin-for-pin replacements for the present CTL gates, buffer and inverter. The gates will be 3 nsec max, and buffer and inverter will be 8 nsec max. The circuits are as follows:

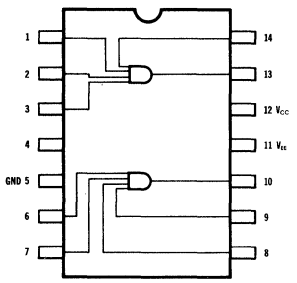
9852 Dual NOR gate
9853 Triple AND gate
9854 Dual four-input AND gate
9855 Eight-input AND gate
9856 Dual buffer
9864 Dual three-and single-input AND gate
9865 Quad single-input AND gate
9866 Quad two-input AND gates, one pair with OR-tie
9871 Quad two-input AND gates, with OR-tied pairs
9872 Same as 9866 but without 2K load or input resistors



9852



9853



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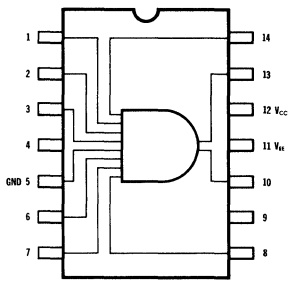

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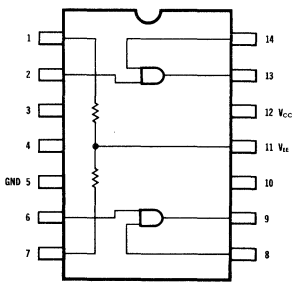

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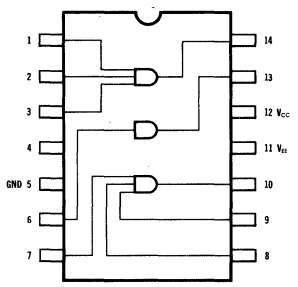
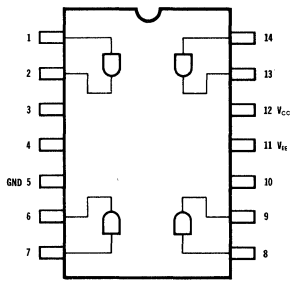
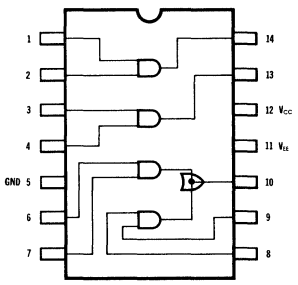


9864



9865



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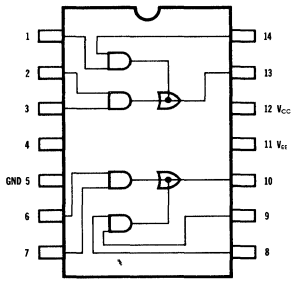

9871

CTL MSI

Following the above CTL II will be CTL MSI. The first six CTL circuits will be:

1 out of 8 Decoder
4 Bit Comparator
4 Bit Multiplexer
4 Bit Latch
Dual Full-Adder
4 Bit Shift Register