

SPC7221F0A

SCSI-2 & CD-ROM Decoder

- Supporting SCSI-2 specification ANSI X3.131
- 20-times speed CD-ROM decoding operation

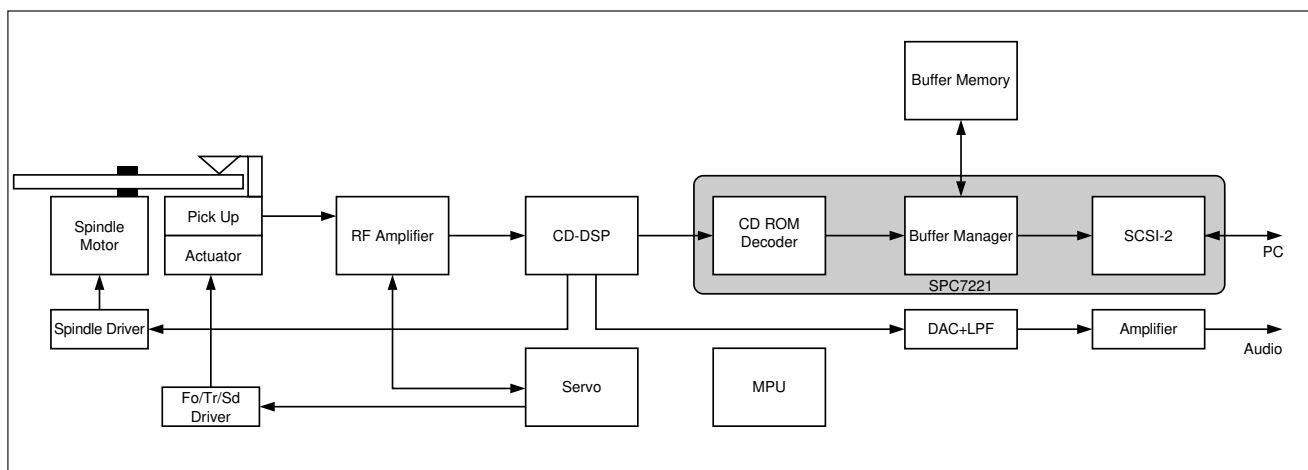
■ OUTLINE

SPC7221F0A is LSIs of CD-ROM decoder and host interface. It supports decoding of 20-times speed and interface of the SCSI-2 protocol function. It is supporting CD-ROM media conforming to CD-DA, CD-ROM and CD-ROM XA format.

■ FEATURES

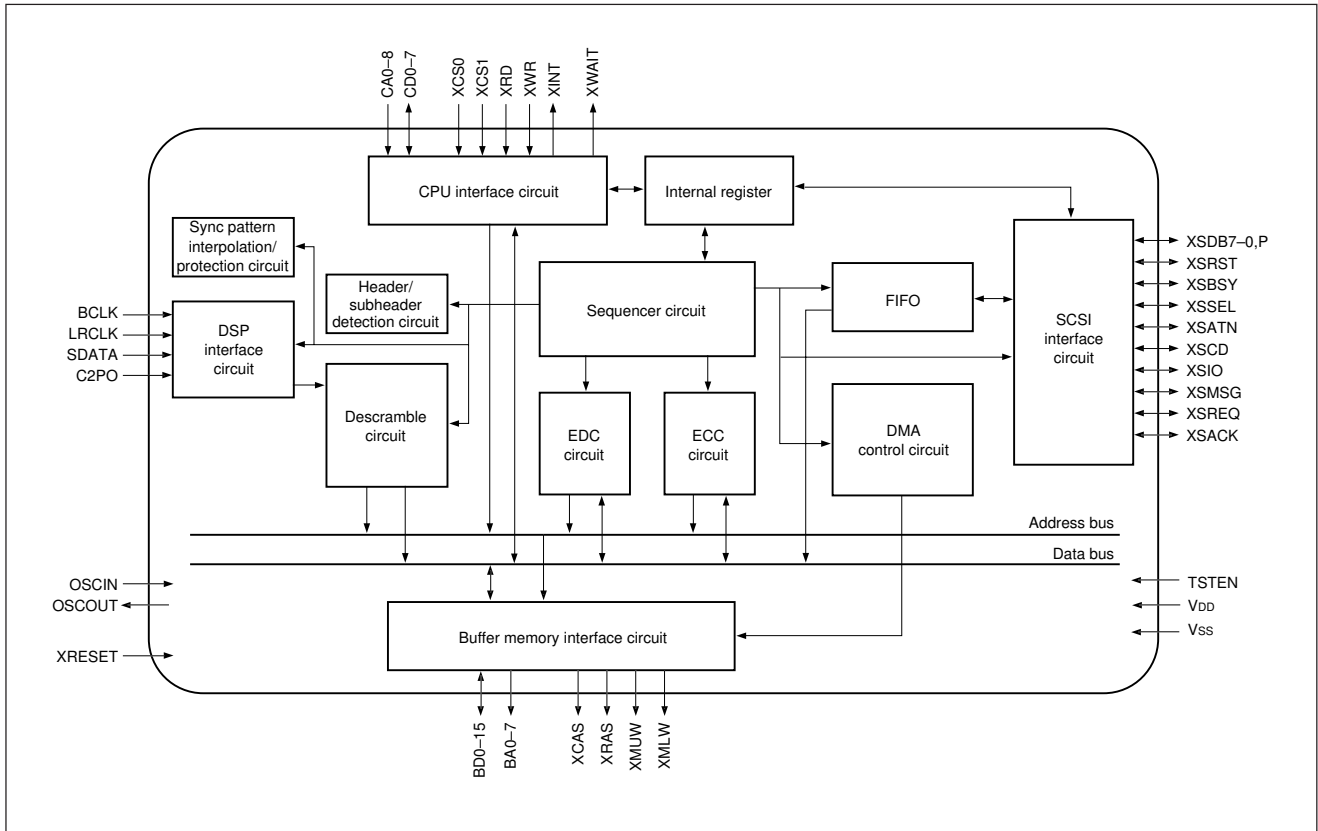
- Fully compatible with SCSI-2 specification ANSI X3.131.
- Supports both synchronous and asynchronous data transmission mode.
Sync transmission mode 8.5Mbyte/s Async transmission mode 4.2Mbyte/s
- 20-times speed decoding operations.
- Supports PnP SCSI SCAM level 1 (Built-in SCAM selection register)
- Realtime CD-ROM ECC P-1word, Q-1word.
- Supports various CD-DSP device interface.
- Supports high speed 8bit MPU interface.
- Direct Addressing 64kword × 16bit DRAM.
- Built-in oscillation circuit 33.8688MHz.
- Supply voltage 5.0V ± 10%
- Package QFP5-128pin

■ BLOCK DIAGRAM (CD-ROM Drives)



SPC7221F0A

■ BLOCK DIAGRAM



SPC7221F0A

■ PIN DESCRIPTION

"X" preceding a pin name indicates that the control signal is low active.

| Pin No. | Pin names | I/O | Function |
|---------|-----------|-------|---|
| 1 | BA5 | O | Buffer memory address bus Bit 5 |
| 2 | BA6 | O | Buffer memory address bus Bit 6 |
| 3 | Vss | P | GND pin |
| 4 | VDD | P | Power supply pin |
| 5 | BA7 | O | Buffer memory address bus Bit 7 |
| 6 | N.C. | | |
| 7 | XRAS | O | Buffer memory low address strobe signal |
| 8 | XCAS | O | Buffer memory column address strobe signal |
| 9 | XMUW | O | Buffer memory write strobe signal (high-order byte) |
| 10 | XMLW | O | Buffer memory write strobe signal (low-order byte) |
| 11 | Vss | P | GND pin |
| 12 | XRESET | I | Reset signal |
| 13 | N.C. | | |
| 14 | N.C. | | |
| 15 | N.C. | | |
| 16 | N.C. | | |
| 17 | VDD | P | Power supply pin |
| 18 | C2PO | I | SDATA signal C2 pointer signal |
| 19 | SDATA | I | Serial data input from DSP |
| 20 | BCLK | I | Bit clock input for SDATA signal strobe |
| 21 | LRCLK | I | LR channel clock |
| 22 | Vss | P | GND pin |
| 23 | OSCOUT | O | Built-in oscillation circuit output pin |
| 24 | OSCIN | I | Built-in oscillation circuit input |
| 25 | VDD | P | Power supply pin |
| 26 | CD0 | Ipu/O | CPU data bus Bit 0 |
| 27 | CD1 | Ipu/O | CPU data bus Bit 1 |
| 28 | CD2 | Ipu/O | CPU data bus Bit 2 |
| 29 | CD3 | Ipu/O | CPU data bus Bit 3 |
| 30 | Vss | P | GND pin |
| 31 | CD4 | Ipu/O | CPU data bus Bit 4 |
| 32 | CD5 | Ipu/O | CPU data bus Bit 5 |
| 33 | CD6 | Ipu/O | CPU data bus Bit 6 |
| 34 | CD7 | Ipu/O | CPU data bus Bit 7 |
| 35 | Vss | P | GND pin |
| 36 | VDD | P | Power supply pin |
| 37 | CA0 | I | CPU Address bus Bit 0 |
| 38 | CA1 | I | CPU Address bus Bit 1 |
| 39 | CA2 | I | CPU Address bus Bit 2 |
| 40 | CA3 | I | CPU Address bus Bit 3 |
| 41 | CA4 | I | CPU Address bus Bit 4 |
| 42 | CA5 | I | CPU Address bus Bit 5 |
| 43 | CA6 | I | CPU Address bus Bit 6 |
| 44 | CA7 | I | CPU Address bus Bit 7 |
| 45 | CA8 | I | CPU Address bus Bit 8 |
| 46 | XWR | I | CPU write signal |
| 47 | XRD | I | CPU read signal |
| 48 | XCS0 | I | Built-in register access Chip select signal |
| 49 | XCS1 | I | Buffer memory access Chip select signal |
| 50 | XINT | O | Interrupt request signal |

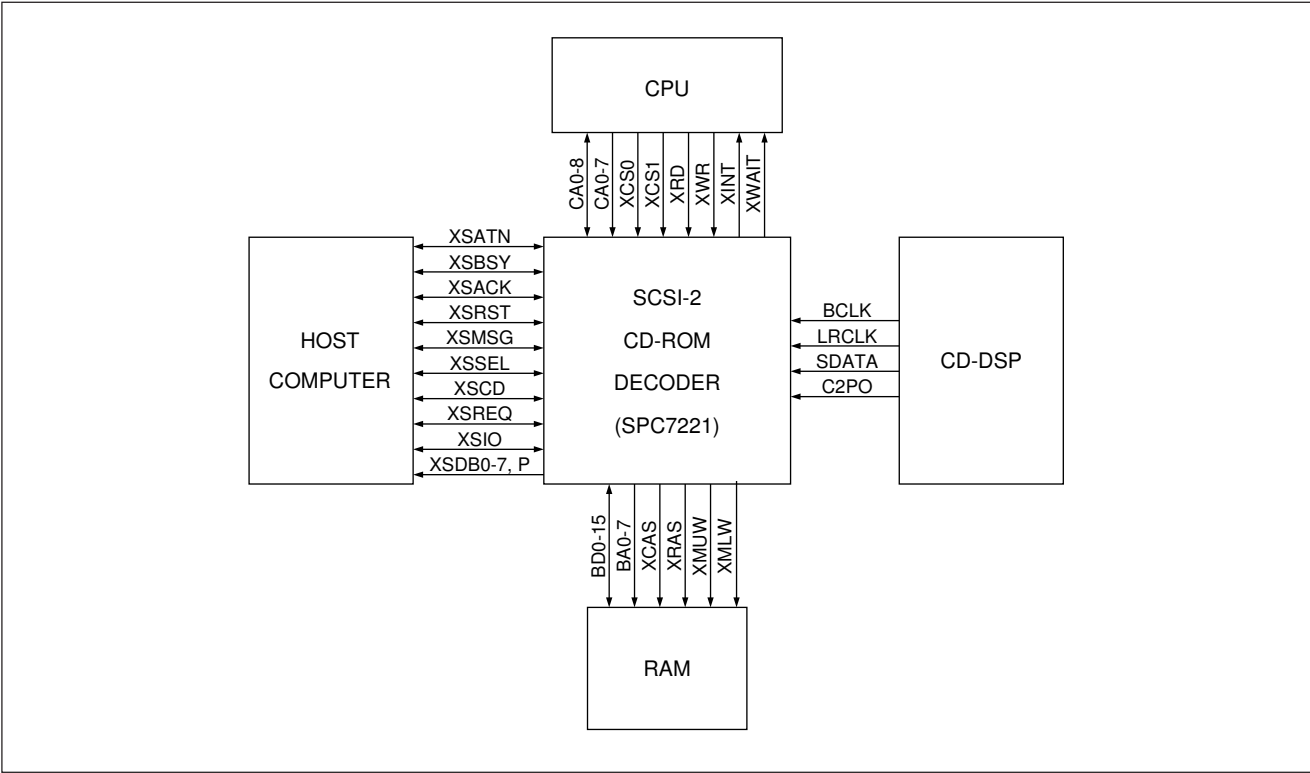
| Pin No. | Pin names | I/O | Function |
|---------|-----------|-------|----------------------------------|
| 51 | XWAIT | Ood | Wait request signal |
| 52 | VDD | P | Power supply signal |
| 53 | CLKO | O | Clock output |
| 54 | Vss | P | GND pin |
| 55 | TSTEN | lpd | Test input enable (normally LOW) |
| 56 | TEST1 | I | Test input (normally LOW) |
| 57 | TEST2 | I | Test input (normally LOW) |
| 58 | TEST3 | I | Test input (normally LOW) |
| 59 | VDD | P | Power supply signal |
| 60 | Vssc | P | GND pin |
| 61 | N.C. | | |
| 62 | XSIO | I/Ood | SCSI I/O |
| 63 | VDD | P | Power supply signal |
| 64 | Vssc | P | GND pin |
| 65 | XSREQ | I/Ood | SCSI REQ |
| 66 | XSCD | I/Ood | SCSI C/D |
| 67 | VDD | P | Power supply signal |
| 68 | Vssc | P | GND pin |
| 69 | N.C. | | |
| 70 | XSSEL | I/Ood | SCSI SEL |
| 71 | VDD | P | Power supply signal |
| 72 | Vssc | P | GND pin |
| 73 | XSMMSG | I/Ood | SCSI MSG |
| 74 | XSRST | I/Ood | SCSI RST |
| 75 | N.C. | | |
| 76 | VDD | P | Power supply signal |
| 77 | Vssc | P | GND pin |
| 78 | XSACK | I/Ood | SCSI ACK |
| 79 | XSBSY | I/Ood | SCSI BSY |
| 80 | VDD | P | Power supply signal |
| 81 | Vssc | P | GND pin |
| 82 | XSATN | I/Ood | SCSI ATN |
| 83 | XSDBP | I/Ood | SCSI data parity (odd parity) |
| 84 | N.C. | | |
| 85 | VDD | P | Power supply signal |
| 86 | Vssc | P | GND pin |
| 87 | XSDB7 | I/Ood | SCSI data buses Bit 7 |
| 88 | XSDB6 | I/Ood | SCSI data buses Bit 6 |
| 89 | N.C. | | |
| 90 | VDD | P | Power supply signal |
| 91 | Vssc | P | GND pin |
| 92 | XSDB5 | I/Ood | SCSI data buses Bit 5 |
| 93 | XSDB4 | I/Ood | SCSI data buses Bit 4 |
| 94 | VDD | P | Power supply signal |
| 95 | Vssc | P | GND pin |
| 96 | XSDB3 | I/Ood | SCSI data buses Bit 3 |
| 97 | XSDB2 | I/Ood | SCSI data buses Bit 2 |
| 98 | N.C. | | |
| 99 | Vss | P | GND pin |
| 100 | VDD | P | Power supply signal |

SPC7221F0A

| Pin No. | Pin names | I/O | Function |
|---------|-----------|-------|---------------------------------|
| 101 | XSDB1 | I/Ood | SCSI data bus Bit 1 |
| 102 | XSDB0 | I/Ood | SCSI data bus Bit 0 |
| 103 | VDD | P | Power supply pin |
| 104 | BD0 | I/Opu | Buffer memory data bus Bit 0 |
| 105 | BD1 | I/Opu | Buffer memory data bus Bit 1 |
| 106 | BD2 | I/Opu | Buffer memory data bus Bit 2 |
| 107 | BD3 | I/Opu | Buffer memory data bus Bit 3 |
| 108 | Vss | P | GND pin |
| 109 | BD4 | I/Opu | Buffer memory data bus Bit 4 |
| 110 | BD5 | I/Opu | Buffer memory data bus Bit 5 |
| 111 | BD6 | I/Opu | Buffer memory data bus Bit 6 |
| 112 | BD7 | I/Opu | Buffer memory data bus Bit 7 |
| 113 | VDD | P | Power supply pin |
| 114 | BD8 | I/Opu | Buffer memory data bus Bit 8 |
| 115 | BD9 | I/Opu | Buffer memory data bus Bit 9 |
| 116 | BD10 | I/Opu | Buffer memory data bus Bit 10 |
| 117 | BD11 | I/Opu | Buffer memory data bus Bit 11 |
| 118 | Vss | P | GND pin |
| 119 | BD12 | I/Opu | Buffer memory data bus Bit 12 |
| 120 | BD13 | I/Opu | Buffer memory data bus Bit 13 |
| 121 | BD14 | I/Opu | Buffer memory data bus Bit 14 |
| 122 | BD15 | I/Opu | Buffer memory data bus Bit 15 |
| 123 | VDD | P | Power supply pin |
| 124 | BA0 | O | Buffer memory address bus Bit 0 |
| 125 | BA1 | O | Buffer memory address bus Bit 1 |
| 126 | BA2 | O | Buffer memory address bus Bit 2 |
| 127 | BA3 | O | Buffer memory address bus Bit 3 |
| 128 | BA4 | O | Buffer memory address bus Bit 4 |

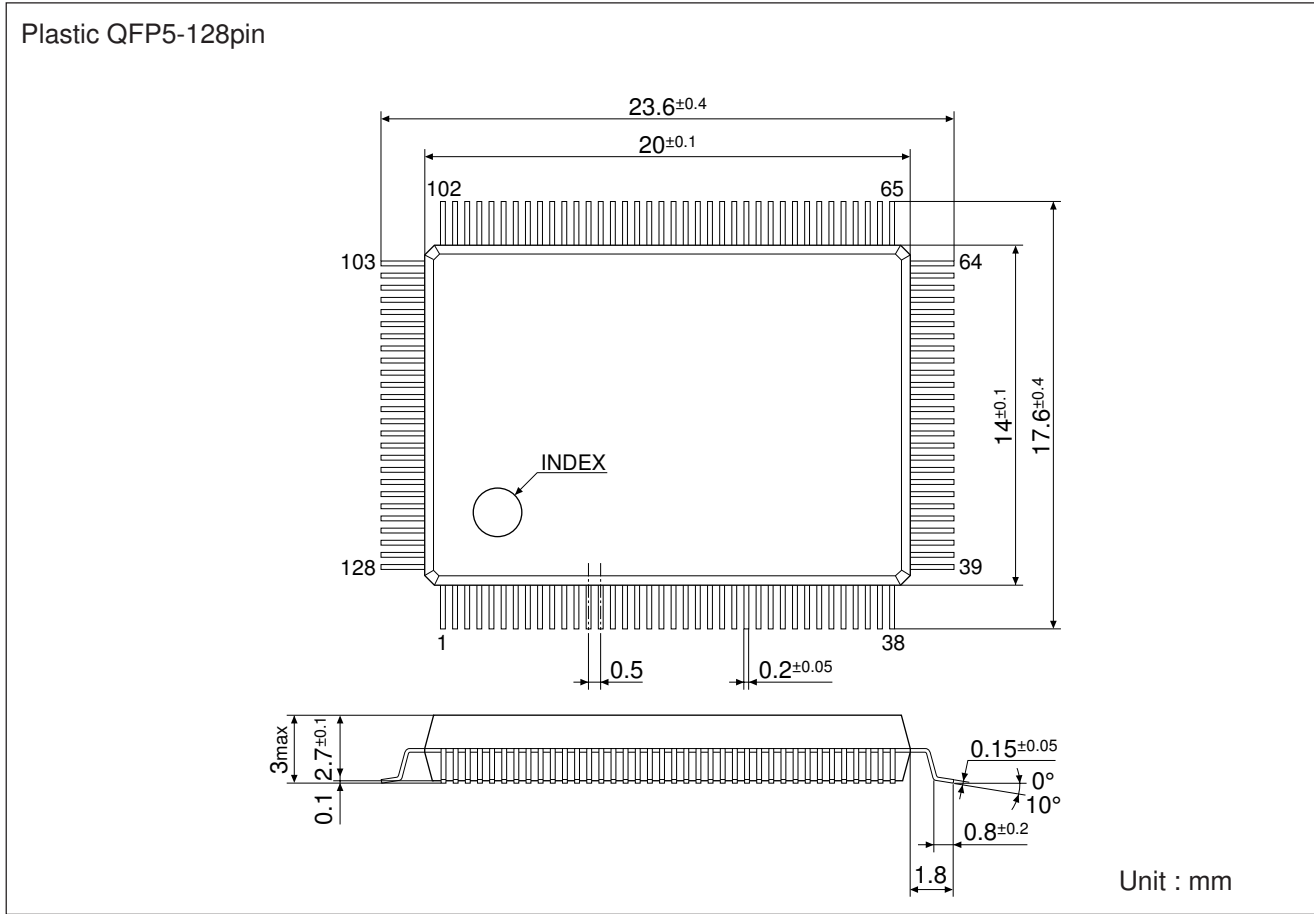
Note: I : Input
 Ipu : Pull-up input
 Ipd : Pull-down input
 O : Output
 Ood : Open drain output
 Ots : 3-state output

■ BASIC EXTERNAL CONNECTION DIAGRAM



SPC7221F0A

■ PACKAGE DIMENSIONS



NOTICE:

No part of this material may be reproduced or duplicated in any form or by any means without the written permission of Seiko Epson. Seiko Epson reserves the right to make changes to this material without notice. Seiko Epson does not assume any liability of any kind arising out of any inaccuracies contained in this material or due to its application or use in any product or circuit and, further, there is no representation that this material is applicable to products requiring high level reliability, such as, medical products. Moreover, no license to any intellectual property rights is granted by implication or otherwise, and there is no representation or warranty that anything made in accordance with this material will be free from any patent or copyright infringement of a third party. This material or portions thereof may contain technology or the subject relating to strategic products under the control of the Foreign Exchange and Foreign Trade Control Law of Japan and may require an export license from the Ministry of International Trade and Industry or other approval from another government agency.

© Seiko Epson Corporation 1996 All right reserved.

SEIKO EPSON CORPORATION

ELECTRONIC DEVICE MARKETING DEPARTMENT

IC Marketing & Engineering Group

421-8 Hino, Hino-shi, Tokyo 191, JAPAN
Phone: 0425-87-5816 FAX: 0425-87-5624

International Marketing Department I (Europe, U.S.A.)

421-8 Hino, Hino-shi, Tokyo 191, JAPAN
Phone: 0425-87-5812 FAX: 0425-87-5564

International Marketing Department II (Asia)

421-8 Hino, Hino-shi, Tokyo 191, JAPAN
Phone: 0425-87-5814 FAX: 0425-87-5110

First issue May 1995, printed Sep. 1996 in Japan ©