CS4340

24-Bit, 96 kHz Stereo DAC for Audio

Features

- Complete Stereo DAC System: Interpolation, D/A, Output Analog Filtering
- 100 dB Dynamic Range
- 88 dB THD+N
- Low Clock Jitter Sensitivity
- +3 V to +5 V Power Supply
- Filtered Line Level Outputs
- On-Chip Digital De-emphasis for 32, 44.1, and 48 kHz
- 30 mW with 3 V supply
- Control of Clicks and Pops

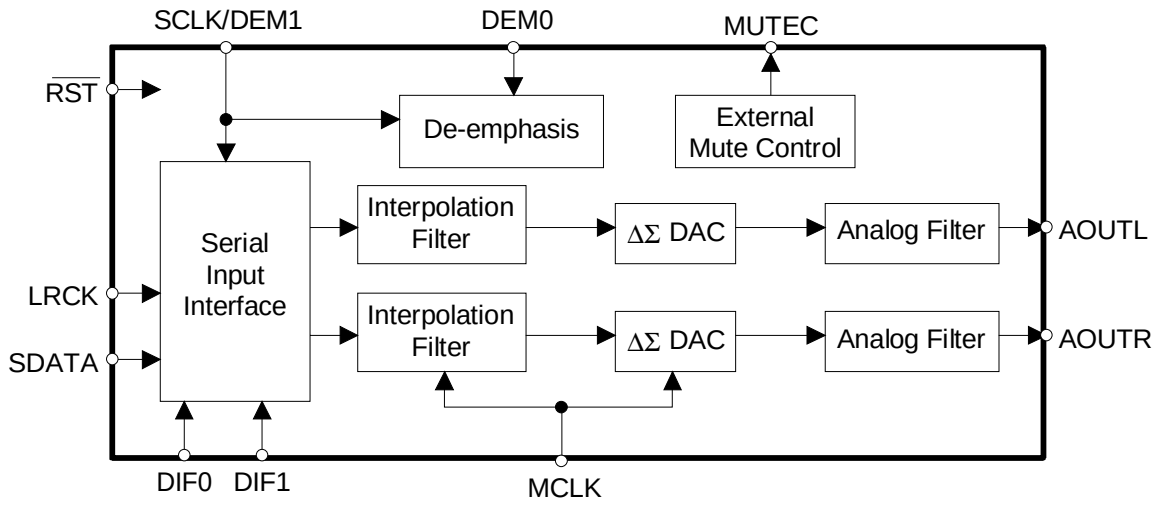
Description

The CS4340 is a complete stereo digital-to-analog system including digital interpolation, fourth-order delta-sigma digital-to-analog conversion, digital de-emphasis and switched capacitor analog filtering. The advantages of this architecture include: ideal differential linearity, no distortion mechanisms due to resistor matching errors, no linearity drift over time and temperature and a high tolerance to clock jitter.

The CS4340 accepts data at audio sample rates from 2 kHz to 100 kHz, consumes very little power, and operates over a wide power supply range. The features of the CS4340 are ideal for DVD players, CD players and set-top box systems.

ORDERING INFORMATION

CS4340-KS	16-pin SOIC, -10 to 70 °C
CDB4340	Evaluation Board



Preliminary Product Information | This document contains information for a new product.
Cirrus Logic reserves the right to modify this product without notice.

CIRRUS LOGIC®
P.O. Box 17847, Austin, Texas 78760
(512) 445 7222 FAX: (512) 445 7581
http://www.cirrus.com

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1. FEATURES

The CS4340 includes a unique set of tools to deal with the extraneous signal artifacts that can occur in any single supply system as well as muting and conversion errors.

1.1 Power On/Off Quiescent Voltage Ramp

The Power On/Off Quiescent Voltage Ramp allows the quiescent voltage to slowly ramp to and from 0 volts to the quiescent voltage during power-on or power-off. Please refer to the *Applications* section for details of implementing this feature.

1.2 External Mute Control

The Mute Control pin goes high during power-up initialization, reset, muting, master clock to left/right clock frequency ratio errors or power-down. The Mute Control output will go active following the reception of 8192 consecutive audio samples of static 0 or -1. A single sample of non-static data will release the mute. The quiescent voltage on the output will be retained while the Mute Control pin is active during the Auto-Mute period. Use of Mute Control is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops.

2. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS (T_A = 25 °C; Logic "1" = VA = 5 V; Logic "0" = AGND;Full-Scale Output Sine Wave, 997 Hz; MCLK = 12.288 MHz; Fs for Base-rate Mode = 48 kHz, SCLK = 3.072 MHz, Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified; Fs for High-Rate Mode = 96 kHz, SCLK = 6.144 MHz, Measurement Bandwidth 10 Hz to 40 kHz, unless otherwise specified. Test load R_L = 10 kΩ, C_L = 10 pF (see Figure 13)

Parameter	Symbol	Base-rate Mode Min	Base-rate Mode Typ	Base-rate Mode Max	High-Rate Mode Min	High-Rate Mode Typ	High-Rate Mode Max	Unit
Dynamic Performance for VA = 5 V								
Specified Temperature Range	T_A	-10	-	70	-10	-	70	°C
Dynamic Range (Note 1)								
18 to 24-Bit unweighted		92	97	-	91	96	-	dB
A-Weighted		96	101	-	95	100	-	dB
16-Bit unweighted		-	95	-	-	94	-	dB
A-Weighted		-	99	-	-	98	-	dB
Total Harmonic Distortion + Noise (Note 1)	THD+N							
18 to 24-Bit 0 dB		-	-89	-84	-	-89	-84	dB
-20 dB		-	-77	-72	-	-74	-69	dB
-60 dB		-	-37	-32	-	-36	-31	dB
16-Bit 0 dB		-	-88	-	-	-89	-	dB
-20 dB		-	-75	-	-	-73	-	dB
-60 dB		-	-35	-	-	-34	-	dB
Interchannel Isolation (1 kHz)		-	100	-	-	100	-	dB
Dynamic Performance for VA = 3 V								
Specified Temperature Range	T_A	-10	-	70	-10	-	70	°C
Dynamic Range (Note 1)								
18 to 24-Bit unweighted		89	94	-	87	92	-	dB
A-Weighted		92	97	-	91	96	-	dB
16-Bit unweighted		-	93	-	-	91	-	dB
A-Weighted		-	96	-	-	96	-	dB
Total Harmonic Distortion + Noise (Note 1)	THD+N							
18 to 24-Bit 0 dB		-	-94	-89	-	-92	-87	dB
-20 dB		-	-74	-69	-	-72	-67	dB
-60 dB		-	-34	-29	-	-32	-27	dB
16-Bit 0 dB		-	-93	-	-	-91	-	dB
-20 dB		-	-73	-	-	-71	-	dB
-60 dB		-	-33	-	-	-31	-	dB
Interchannel Isolation (1 kHz)		-	100	-	-	100	-	dB

Notes: 1. One-half LSB of triangular PDF dither is added to data.

ANALOG CHARACTERISTICS (Continued)

Parameters	Symbol	Min	Typ	Max	Units
Analog Output					
Full Scale Output Voltage		0.63•VA	0.7•VA	0.77•VA	Vpp
Quiescent Voltage	V_Q	-	0.5•VA	-	VDC
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Drift		-	100	-	ppm/°C
AC-Load Resistance (Note 2)	R_L	3	-	-	kΩ
Load Capacitance (Note 2)	C_L	-	-	100	pF

Parameter	Symbol	Base-rate Mode Min	Typ	Max	High-Rate Mode Min	Typ	Max	Unit
Combined Digital and On-chip Analog Filter Response (Note 3)								
Passband (Note 4)								
to -0.05 dB corner		0	-	.4535	-	-	-	Fs
to -0.1 dB corner		-	-	-	0	-	.4621	Fs
to -3 dB corner		0	-	.4998	0	-	.4982	Fs
Frequency Response 10 Hz to 20 kHz		-.02	-	+.08	-0.06	-	0	dB
StopBand		.5465	-	-	.577	-	-	Fs
StopBand Attenuation (Note 5)		50	-	-	55	-	-	dB
Group Delay	tgd	-	9/Fs	-	-	4/Fs	-	s
Passband Group Delay Deviation 0 - 40 kHz		-	-	-	-	±1.39/Fs	-	s
0 - 20 kHz		-	±0.36/Fs	-	-	±0.23/Fs	-	s
De-emphasis Error Fs = 32 kHz		-	-	+.2/-.1				dB
(Relative to 1 kHz) Fs = 44.1 kHz		-	-	+.05/-.14		(Note 6)		dB
Fs = 48 kHz		-	-	+0/-.22				dB

Notes:
2. Refer to Figure 14.
3. Filter response is guaranteed by design.
4. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 5-12) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.
5. For Base-Rate Mode, the measurement bandwidth is 0.5465 Fs to 3 Fs.
   For High-Rate Mode, the measurement bandwidth is 0.577 Fs to 1.4 Fs.
6. De-emphasis is not available in High-Rate Mode.

POWER AND THERMAL CHARACTERISTICS

Parameters		Symbol	Min	Typ	Max	Units
Power Supplies						
Power Supply Current VA = 5 V	normal operation power-down state	I_A I_A	- -	15 60	17 -	mA µA
Power Dissipation VA = 5 V	(Note 7) normal operation power-down		 - -	 75 0.3	 85 -	 mW mW
Power Supply Current VA = 3 V	normal operation power-down state	I_A I_A	- -	10 30	14 -	mA µA
Power Dissipation VA = 3 V	(Note 7) normal operation power-down		 - -	 30 0.09	 42 -	 mW mW
Package Thermal Resistance		θ_{JA}	-	110	-	°C/Watt
Power Supply Rejection Ratio (1 kHz)	(Note 8) (60 Hz)	PSRR	- -	60 40	- -	dB dB

Notes: 7. Refer to Figure 15.

8. Valid with the recommended capacitor values on FILT+ and VQ as shown in Figure 1. Increasing the capacitance will also increase the PSRR.

DIGITAL CHARACTERISTICS (T_A = 25°C; VA = 2.7 V - 5.5 V)

Parameters		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	VA = 5 V VA = 3 V	V_{IH}	2.0 2.0	- -	- -	V V
Low-Level Input Voltage	VA = 5 V VA = 3 V	V_{IL}	- -	- -	0.8 0.8	V V
Input Leakage Current		I_{in}	-	-	±10	µA
Input Capacitance			-	8	-	pF
Maximum MUTEC Drive Current			-	3	-	mA

ABSOLUTE MAXIMUM RATINGS (AGND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply	VA	-0.3	6.0	V
Input Current, Any Pin Except Supplies	I_{in}	-	±10	mA
Digital Input Voltage	V_{IND}	-0.3	VA+0.4	V
Ambient Operating Temperature (power applied)	T_A	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND = 0V; all voltages with respect to ground.)

Parameters	Symbol	Min	Typ	Max	Units
DC Power Supply	VA	2.7	5.0	5.5	V

SWITCHING CHARACTERISTICS (T_A = -10 to 70°C; VA = 2.7 V - 5.5 V; Inputs: Logic 0 = 0 V, Logic 1 = VA, CL = 20 pF)

Parameters	Symbol	Min	Typ	Max	Units
Input Sample Rate	Fs	2	-	100	kHz
MCLK Pulse Width High MCLK/LRCK = 512		10	-	1000	ns
MCLK Pulse Width Low MCLK/LRCK = 512		10	-	1000	ns
MCLK Pulse Width High MCLK / LRCK = 384 or 192		21	-	1000	ns
MCLK Pulse Width Low MCLK / LRCK = 384 or 192		21	-	1000	ns
MCLK Pulse Width High MCLK / LRCK = 256 or 128		31	-	1000	ns
MCLK Pulse Width Low MCLK / LRCK = 256 or 128		31	-	1000	ns
External SCLK Mode					
LRCK Duty Cycle (External SCLK only)		40	50	60	%
SCLK Pulse Width Low	t_{sclkl}	20	-	-	ns
SCLK Pulse Width High	t_{sclkh}	20	-	-	ns
SCLK Period MCLK / LRCK = 512, 256 or 384	t_{sclkw}	$\frac{1}{(128)Fs}$	-	-	ns
SCLK Period MCLK / LRCK = 128 or 192	t_{sclkw}	$\frac{1}{(64)Fs}$	-	-	ns
SCLK rising to LRCK edge delay	t_{slrd}	20	-	-	ns
SCLK rising to LRCK edge setup time	t_{slrs}	20	-	-	ns
SDATA valid to SCLK rising setup time	t_{sdlrs}	20	-	-	ns
SCLK rising to SDATA hold time	t_{sdh}	20	-	-	ns
Internal SCLK Mode					
LRCK Duty Cycle (Internal SCLK only) (Note 9)		-	50	-	%
SCLK Period (Note 10)	t_{sclkw}	$\frac{1}{SCLK}$	-	-	ns
SCLK rising to LRCK edge	t_{sclkr}	-	$\frac{tsclkw}{2}$	-	µs
SDATA valid to SCLK rising setup time	t_{sdlrs}	$\frac{1}{(512)Fs} + 10$	-	-	ns
SCLK rising to SDATA hold time MCLK / LRCK = 512, 256 or 128	t_{sdh}	$\frac{1}{(512)Fs} + 15$	-	-	ns
SCLK rising to SDATA hold time MCLK / LRCK = 384 or 192	t_{sdh}	$\frac{1}{(384)Fs} + 15$	-	-	ns

Notes: 9. In Internal SCLK Mode, the Duty Cycle must be 50% +/– 1/2 MCLK Period.

10. The SCLK / LRCK ratio may be either 32, 48, or 64. This ratio depends on part type and MCLK/LRCK ratio. (See figures 16-19)

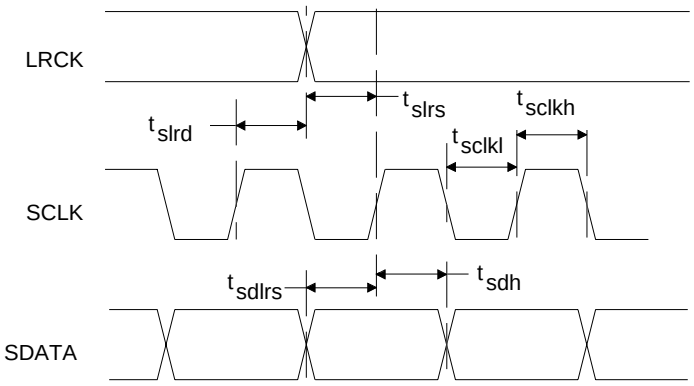


Figure 1. External Serial Mode Input Timing

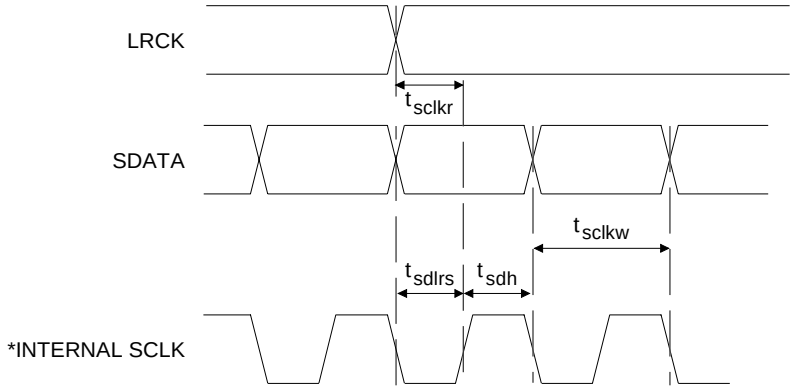


Figure 2. Internal Serial Mode Input Timing
*The SCLK pulses shown are internal to the CS4340.

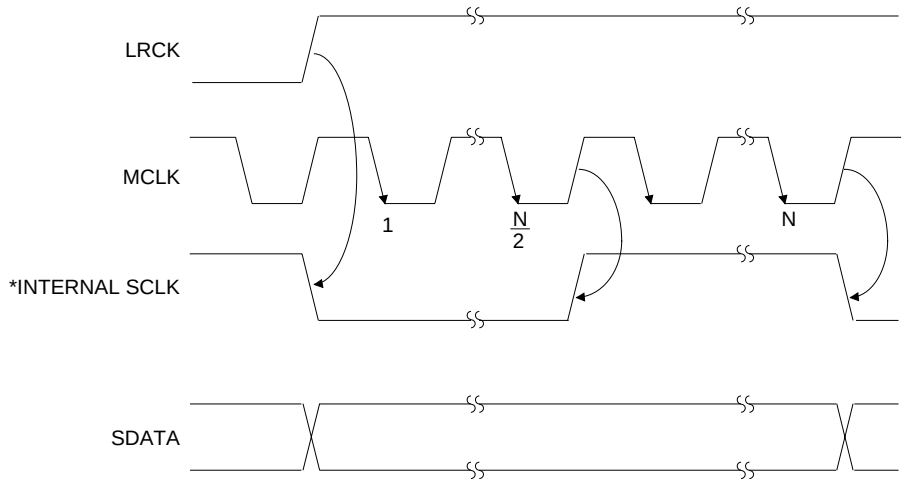


Figure 3. Internal Serial Clock Generation
* The SCLK pulses shown are internal to the CS4340.
N equals MCLK divided by SCLK

3. TYPICAL CONNECTION DIAGRAM

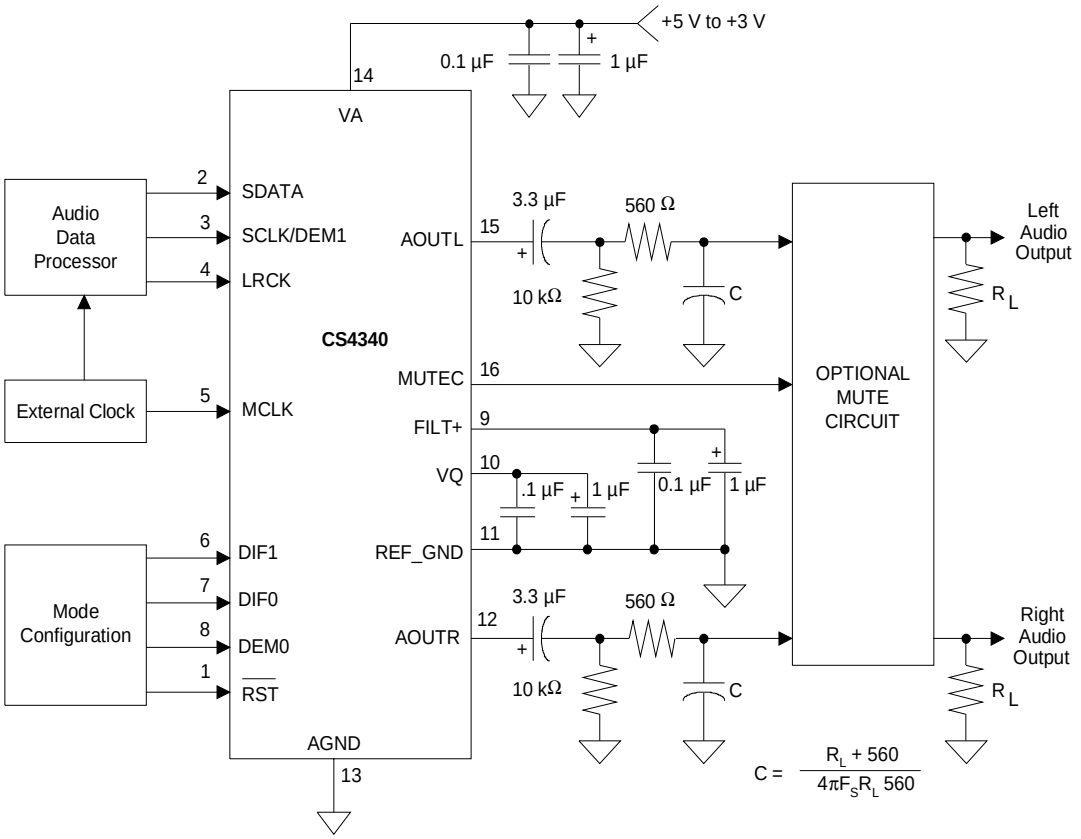
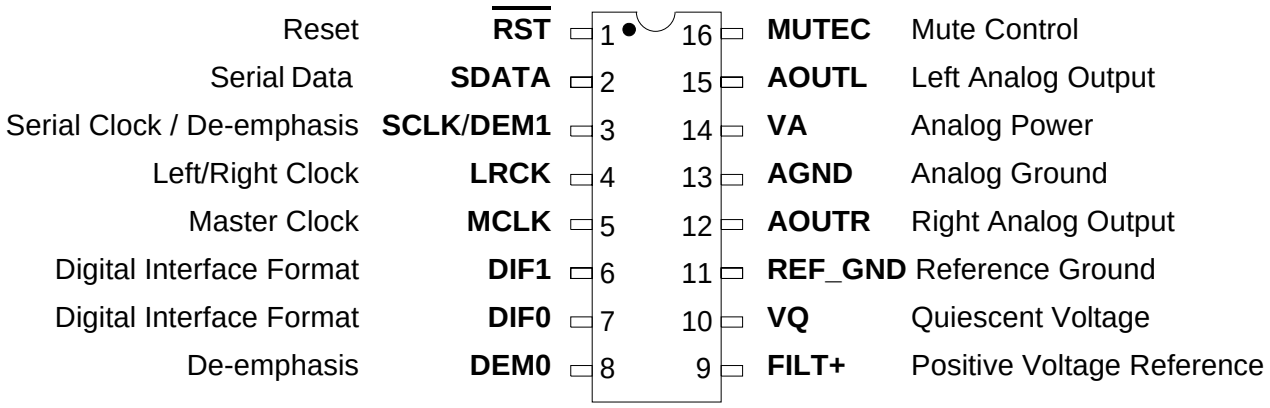


Figure 4. Typical Connection Diagram

4. PIN DESCRIPTION



Analog Power - VA

Pin 14, Input

Function:

Analog power supply. Typically 3 to 5VDC.

Analog Ground - AGND

Pin 13, Input

Function:

Analog ground reference.

Analog Output - AOUTL and AOUTR

Pins 12 and 15, Output

Function:

The full scale analog output level is specified in the Analog Characteristics specifications table.

Reference Ground - REF_GND

Pin 11, Input

Function:

Ground reference for the internal sampling circuits. Must be connected to analog ground.

Positive Voltage Reference - FILT+

Pin 9, Output

Function:

Positive reference for internal sampling circuits. External capacitors are required from FILT+ to analog ground, as shown in Figure 4. The recommended values will provide 60 dB of PSRR at 1 kHz and 40 dB of PSRR at 60 Hz. FILT+ is not intended to supply external current. FILT+ has a typical source impedence of 250 kΩ and any current drawn from this pin will alter device performance.

Quiescent Voltage - VQ

Pin 10, Output

Function:

Filter connection for internal quiescent reference voltage, typically 50% of VA. Capacitors must be connected from VQ to analog ground, as shown in Figure 4. VQ is not intended to supply external current. VQ has a typical source impedence of 250 kΩ and any current drawn from this pin will alter device performance.

Master Clock - MCLK

Pin 5, Input

Function:

The master clock frequency must be either 256x, 384x or 512x the input sample rate in Base Rate Mode (BRM) and either 128x or 192x the input sample rate in High Rate Mode (HRM). Table 1 illustrates several standard audio sample rates and the required master clock frequencies.

Sample Rate (kHz)	MCLK (MHz)				
	HRM		BRM		
	128x	192x	256x	384x	512x
32	4.0960	6.1440	8.1920	12.2880	16.3840
44.1	5.6448	8.4672	11.2896	16.9344	22.5792
48	6.1440	9.2160	12.2880	18.4320	24.5760
64	8.1920	12.2880	-	-	-
88.2	11.2896	16.9344	-	-	-
96	12.2880	18.4320	-	-	-

Table 1. Common Clock Frequencies

Left/Right Clock - LRCK

Pin 4, Input

Function:

The Left/Right clock determines which channel is currently being input on the serial audio data input, SDATA. The frequency of the Left/Right clock must be at the input sample rate. Audio samples in Left/Right sample pairs will be simultaneously output from the digital-to-analog converter whereas Right/Left pairs will exhibit a one sample period difference. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format pins and the options are detailed in Figures 16-19.

Serial Audio Data - SDATA

Pin 2, Input

Function:

Two's complement MSB-first serial data is input on this pin. The data is clocked into SDATA via the serial clock and the channel is determined by the Left/Right clock. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format pins and the options are detailed in Figures 16-19.

Serial Clock - SCLK

Pin 3, Input

Function:

Clocks the individual bits of the serial data into the SDATA pin. The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format pins and the options are detailed in Figures 16-19.

The CS4340 supports both internal and external serial clock generation modes. The Internal Serial Clock Mode eliminates possible clock interference from an external SCLK. Use of the Internal Serial Clock Mode is always preferred.

Internal Serial Clock Mode

In the Internal Serial Clock Mode, the serial clock is internally derived and synchronous with the master clock and left/right clock. The SCLK/LRCK frequency ratio is either 32, 48, or 64 depending upon data format, as shown in Figures 16-19. Operation in this mode is identical to operation with an external serial clock synchronized with LRCK.

External Serial Clock Mode

The CS4340 will enter the External Serial Clock Mode whenever 16 low to high transitions are detected on the SCLK pin during any phase of the LRCK period. The device will revert to Internal Serial Clock Mode if no low to high transitions are detected on the SCLK pin for 2 consecutive periods of LRCK

Reset - $\overline{\text{RST}}$

Pin 1, Input

Function:

The device enters a low power mode and all internal state machines are reset to the default settings when low. $\overline{\text{RST}}$ should be held low during power-up until the power supply, master and left/right clocks are stable.

Digital Interface Format - DIF1 and DIF0

Pins 6 and 7, Input

Function:

The required relationship between the Left/Right clock, serial clock and serial data is defined by the Digital Interface Format and the options are detailed in Figures 16-19.

DIF1	DIF0	DESCRIPTION	FORMAT	FIGURE
0	0	I^2S, up to 24-bit data	0	16
0	1	Left Justified, up to 24-bit data	1	17
1	0	Right Justified, 24-bit Data	2	18
1	1	Right Justified, 16-bit Data	3	19

Table 2. Digital Interface Format

De-emphasis Control - DEM0 and DEM1

Pins 3 and 8, Input

Function:

Implementation of the standard 15µs/50µs digital de-emphasis filter response, Figure 20, requires reconfiguration of the digital filter to maintain the proper filter response for 32, 44.1 or 48 kHz sample rates. When using Internal Serial Clock Mode, as described above, Pin 3 is available for de-emphasis control, DEM1, and all de-emphasis filters are available, Table 3. When using External Serial Clock Mode, as described above, Pin 3 is not available for de-emphasis use and only the 44.1 kHz de-emphasis filter is available, Table 4. NOTE: De-emphasis is not available in High-Rate Mode.

DEM1	DEMO	DESCRIPTION
0	0	Disabled
0	1	44.1kHz
1	0	48kHz
1	1	32kHz

Table 3. Internal Serial Clock Mode

DEMO	DESCRIPTION
0	Disabled
1	44.1kHz

Table 4. External Serial Clock Mode

Mute Control - MUTEC

Pin 16, Output

Function:

The Mute Control pin goes high during power-up initialization, reset, muting, master clock to left/right clock frequency ratio is incorrect or power-down. This pin is intended to be used as a control for an external mute circuit to prevent the clicks and pops that can occur in any single supply system. Use of Mute Control is not mandatory but recommended for designs requiring the absolute minimum in extraneous clicks and pops.

5. APPLICATIONS

5.1 Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4340 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 4 shows the recommended power arrangement with VA connected to a clean supply. Decoupling capacitors should be located as close to the device package as possible.

5.2 Oversampling Modes

The CS4340 operates in one of two oversampling modes. Base Rate Mode supports input sample rates up to 50 kHz while High Rate Mode supports input sample rates up to 100 kHz. The devices operate in Base Rate Mode (BRM) when MCLK/LRCK is 256, 384 or 512 and in High Rate Mode (HRM) when MCLK/LRCK is 128 or 192.

5.3 Recommended Power-up Sequence

$\overline{\text{RST}}$ should be held low until the power supply, master and left/right clocks are stable.

5.4 Use of the Power ON/OFF Quiescent Voltage Ramp

The CS4340 uses a novel technique to minimize the effects of output transients during power-up and power-down. This technique, when used with external DC-blocking capacitors in series with the audio outputs, minimizes the audio transients commonly produced by single-ended single-supply converters.

When the device is initially powered-up, the audio outputs, AOUTL and AOUTR, are clamped to AGND. Following a delay of approximately 1000 sample periods, each output begins to ramp toward the quiescent voltage. Approximately 10,000 left/right clock cycles later, the outputs reach V_Q and audio output begins. This gradual voltage ramping allows time for the external DC-blocking capacitor to charge to the quiescent voltage, minimizing the power-up transient.

To prevent transients at power-down, the device must first enter its power-down state by setting the $\overline{\text{RST}}$ pin low. When this occurs, audio output ceases and the internal output buffers are disconnected from AOUTL and AOUTR. In their place, a soft-start current sink is substituted which allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off and the system is ready for the next power-on.

To prevent an audio transient at the next power-on, it is necessary to ensure that the DC-blocking capacitors have fully discharged before turning off the power or exiting the power-down state. If not, a transient will occur when the audio outputs are initially clamped to AGND. The time that the device must remain in the power-down state is related to the value of the DC-blocking capacitance. For example, with a 3.3 µF capacitor, the minimum power-down time will be approximately 0.4 seconds.

Use of the Mute Control function is recommended for designs requiring the absolute minimum in extraneous clicks and pops. Also, use of the Mute Control function can enable the system designer to achieve idle channel noise/signal-to-noise ratios which are only limited by the external mute circuit.

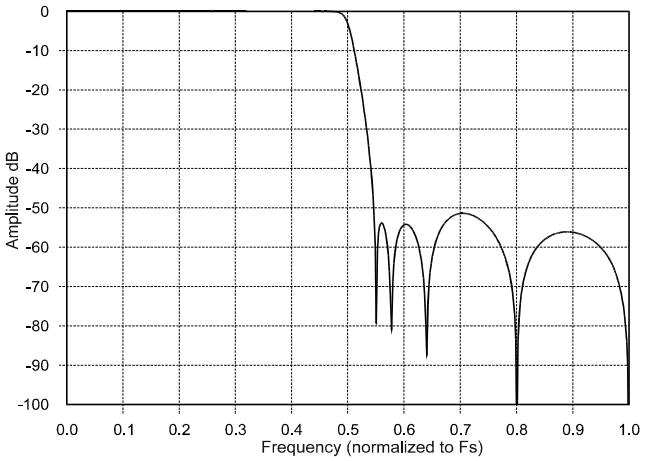


Figure 5. Base-Rate Stopband Rejection

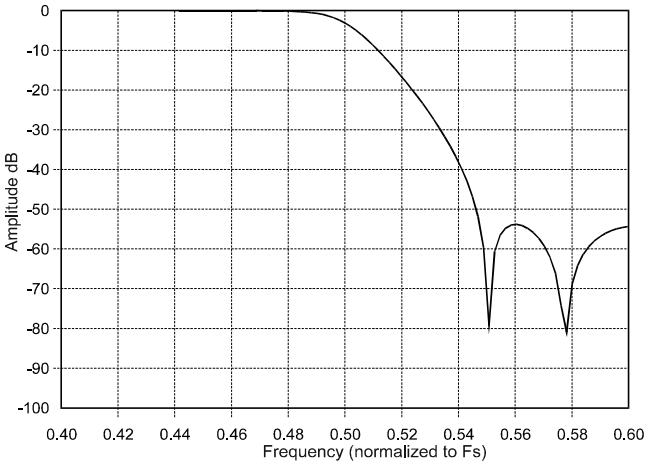


Figure 6. Base-Rate Transition Band

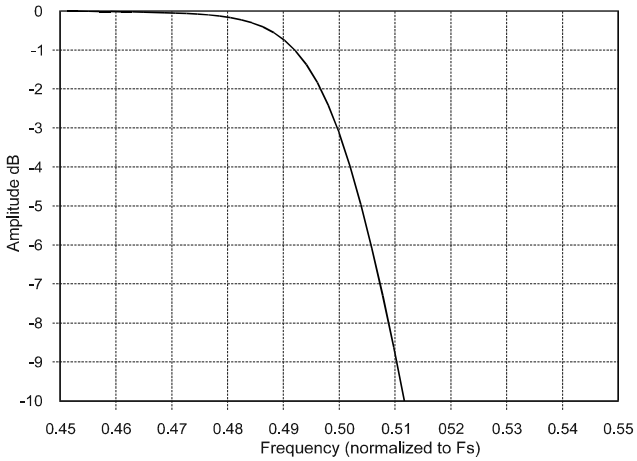


Figure 7. Base-Rate Transition Band (Detail)

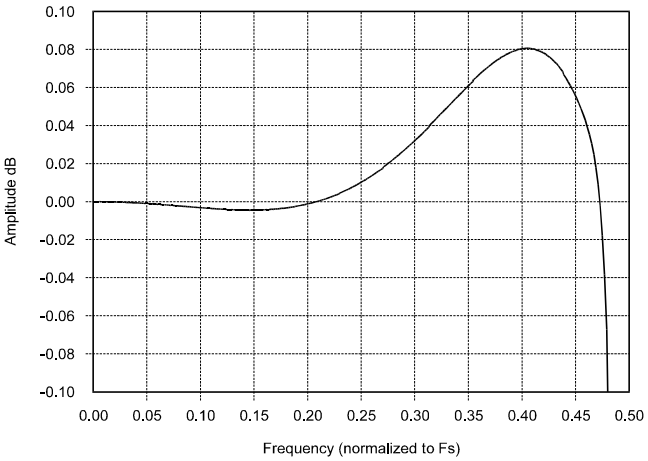


Figure 8. Base-Rate Passband Ripple

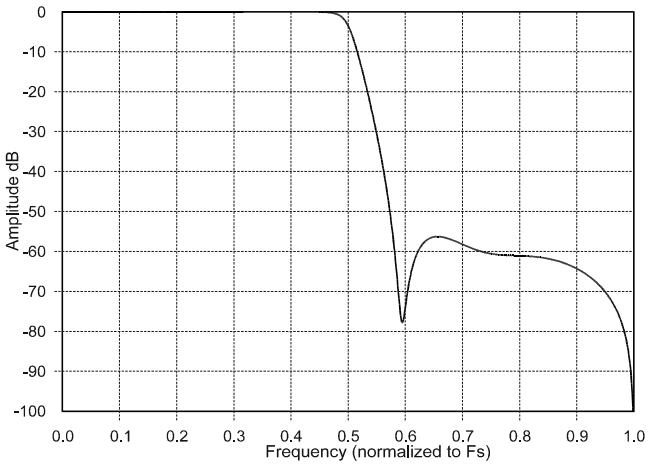


Figure 9. High-Rate Stopband Rejection

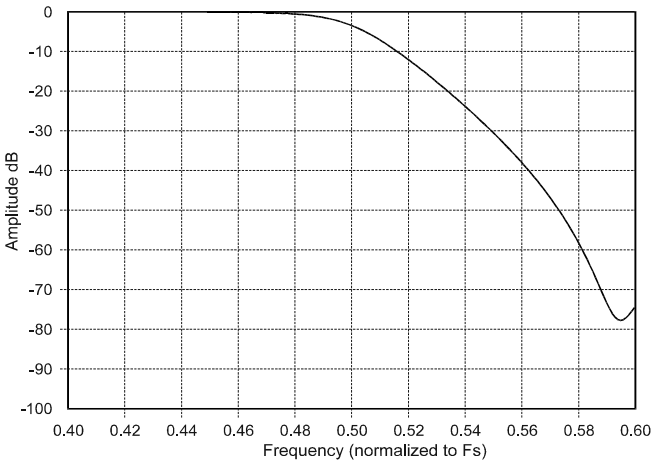


Figure 10. High-Rate Transition Band

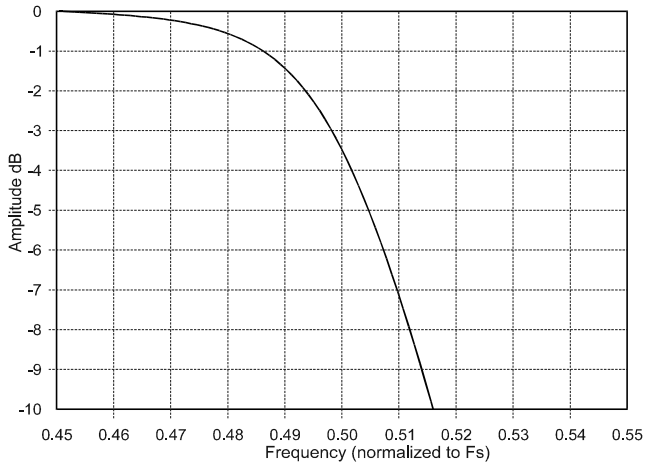


Figure 11. High-Rate Transition Band (Detail)

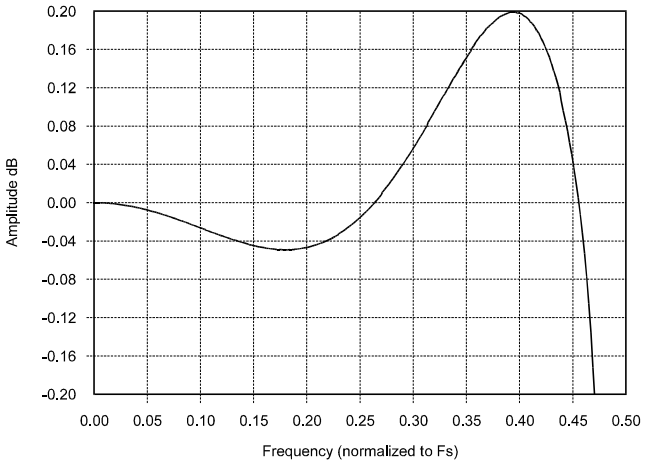


Figure 12. High-Rate Passband Ripple

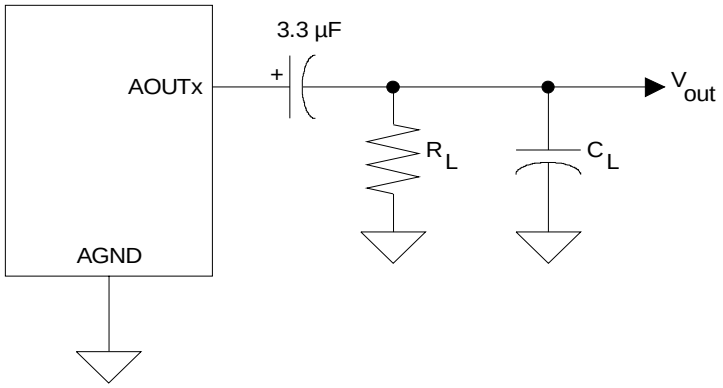


Figure 13. Output Test Load

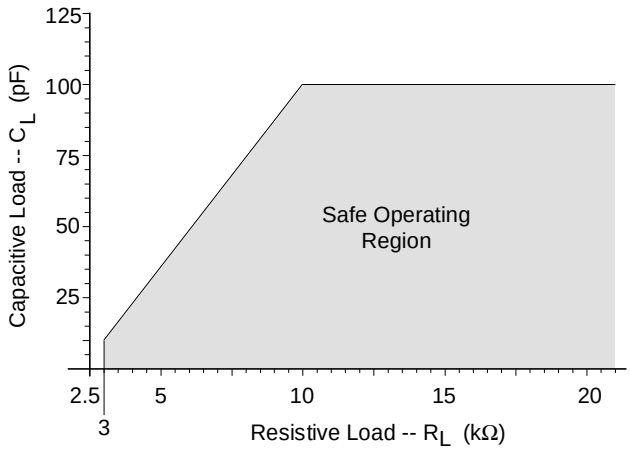


Figure 14. Maximum Loading

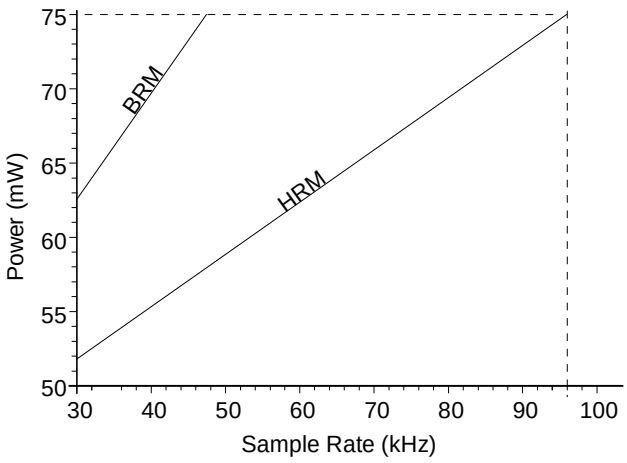
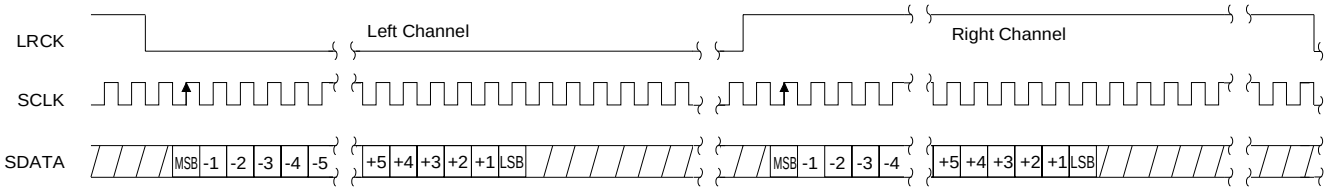
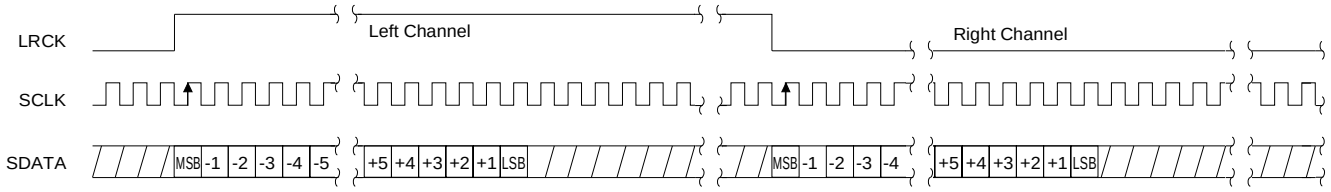


Figure 15. Power vs. Sample Rate (VA = 5V)



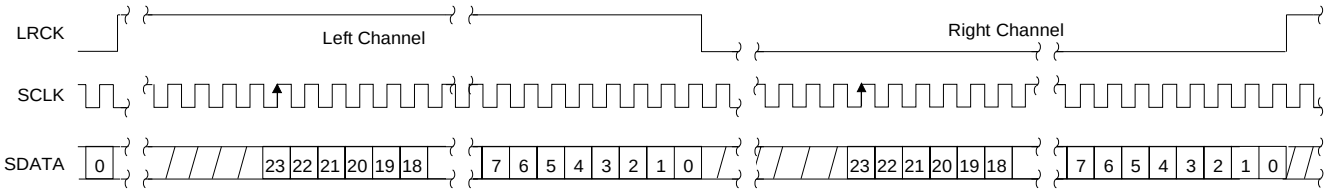
Internal SCLK Mode	External SCLK Mode
I^2S, 16-Bit data and INT SCLK = 32 Fs if MCLK/LRCK = 512, 256 or 128 I^2S, up to 24-Bit data and INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	I^2S, up to 24-Bit Data Data Valid on Rising Edge of SCLK

Figure 16. CS4340 Format 0 (I^2S)



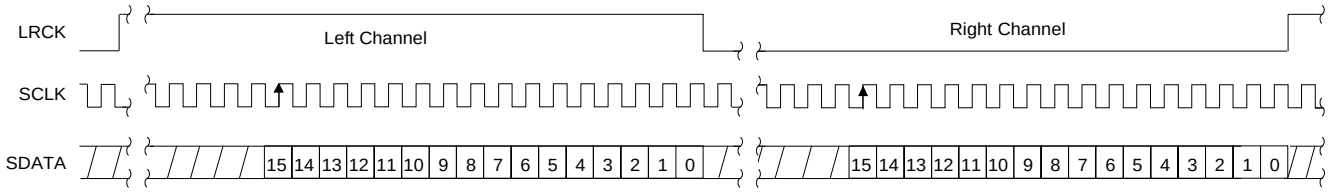
Internal SCLK Mode	External SCLK Mode
Left Justified, up to 24-Bit Data INT SCLK = 64 Fs if MCLK/LRCK = 512, 256 or 128 INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	Left Justified, up to 24-Bit Data Data Valid on Rising Edge of SCLK

Figure 17. CS4340 Format 1



Internal SCLK Mode	External SCLK Mode
Right Justified, 24-Bit Data INT SCLK = 64 Fs if MCLK/LRCK = 512, 256 or 128 INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	Right Justified, 24-Bit Data Data Valid on Rising Edge of SCLK SCLK Must Have at Least 48 Cycles per LRCK Period

Figure 18. CS4340 Format 2



Internal SCLK Mode	External SCLK Mode
Right Justified, 16-Bit Data INT SCLK = 32 Fs if MCLK/LRCK = 512, 256 or 128 INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	Right Justified, 16-Bit Data Data Valid on Rising Edge of SCLK SCLK Must Have at Least 32 Cycles per LRCK Period

Figure 19. CS4340 Format 3

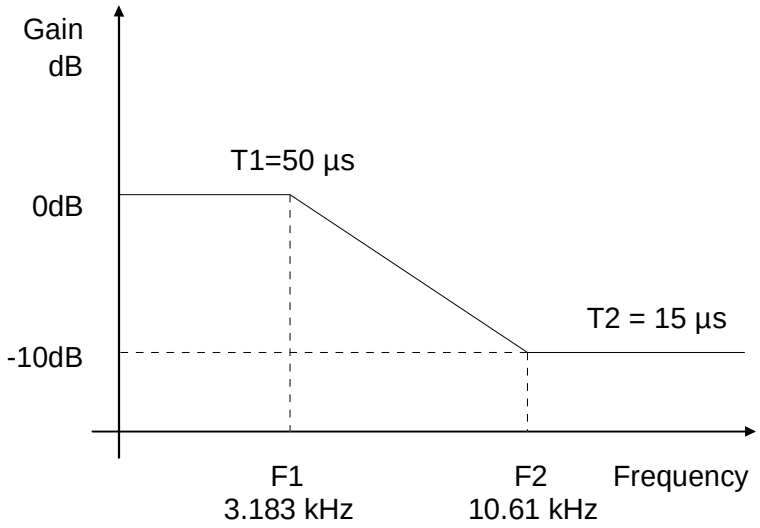


Figure 20. De-Emphasis Curve

6. PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10Hz to 20kHz), including distortion components. Expressed in decibels.

Dynamic Range

The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation

A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channels. Units in decibels.

Gain Error

The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift

The change in gain value with temperature. Units in ppm/°C.

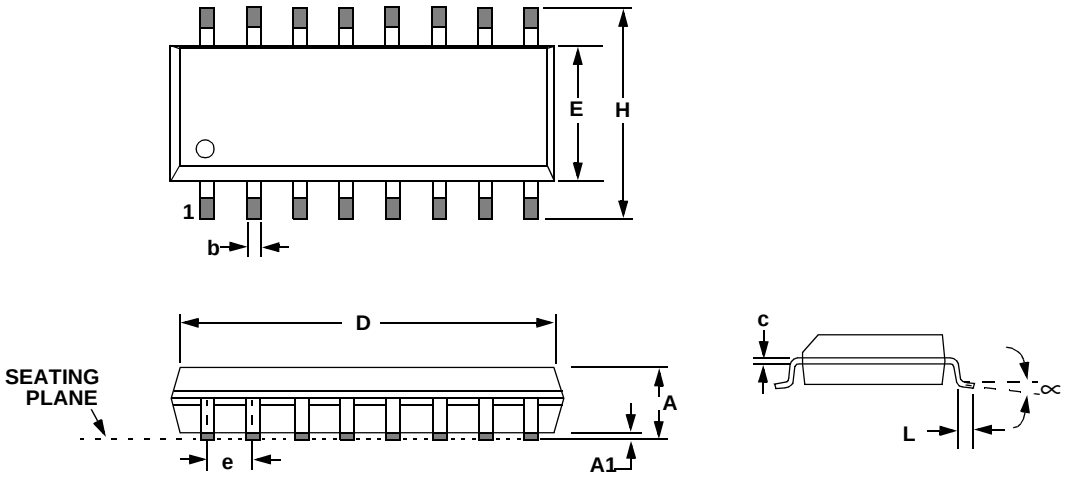
7. REFERENCES

1) "How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters" by Steven Harris. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.

2) CDB4340 Evaluation Board Datasheet

8. PACKAGE DIMENSIONS

16L SOIC (150 MIL BODY) PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	**MIN**	**MAX**	**MIN**	**MAX**
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.386	0.394	9.80	10.00
E	0.150	0.157	3.80	4.00
e	0.040	0.060	1.02	1.52
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
µ	0°	8°	0°	8°

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