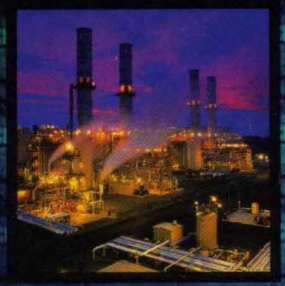
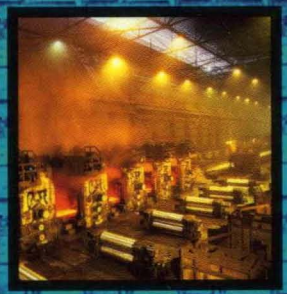
1995

CRYSTAL SEMICONDUCTOR DATA ACQUISITION DATABOOK

CRYSTAL SEMICONDUCTOR
DATA ACQUISITION DATABOOK

CRYSTAL





CRYSTAL

MODEL INDEX

Crystal Semiconductor Corporation

Data Acquisition Products
Data Book

March 1995

TRADEMARKS

Crystal Semiconductor Corporation has made every effort to supply trademark information about company names, products, and services mentioned in this book. Trademarks indicated below are derived from various sources.

"*C*" (stylized) is a registered trademark of Crystal Semiconductor Corporation.

CRYSTAL, SMART *Analog*, Crystal Clear, and CrystalWare are trademarks of Crystal Semiconductor Corporation.

Other trademarks in this book belong to their respective companies.

PATENTS

Products in this book may be covered by one or more of the following patents. Additional patents are pending.

USA

4,709,225; 4,746,899; 4,748,418; 4,804,863; 4,805,198; 4,849,662; 4,851,841; 4,918,454; 4,939,516; 4,941,156; 4,943,807; 4,988,954; 5,012,244; 5,039,989; 5,055,846; 5,061,925; 5,068,660; 5,079,550; 5,087,914; 5,088,107; 5,111,451; 5,117,200; 5,121,080; 5,140,279; 5,150,386; 5,157,395; 5,172,115; 5,187,390; 5,196,850; 5,198,782; 5,208,597; 5,212,659; 5,220,483; 5,239,210; 5,245,344; 5,247,210; 5,248,970; 5,257,026; 5,258,758; 5,268,651; 5,274,375; 5,319,319; 5,319,370; 5,339,067; 5,351,050; 5,376,936

GERMANY

P3642070.0; P3733682.7; P3736735.8; P3737279.3; P3933552.6; P4002871.2; P4200745.3; P4202180.4

GREAT BRITAIN

2184621; 2195848; 2198305; 2198306; 2223879; 2232547; 2247370; 2252459; 2252829; 2253754; 2253756; 2254504; 2261561

FRANCE

8617487; 8713769; 8715552; 8715553

JAPAN

1684670; 1736807; 1747931; 4-25778

CONTENTS

COMPANY INFORMATION

Crystal's proprietary SMART Analog™ design technique, incorporating analog and digital circuitry in monolithic CMOS devices, represents a powerful new technology in the semiconductor industry. This innovative approach to design eliminates many of the sources of inconsistent performance in traditional analog circuitry.

Maximum system performance is built-in from initial research on end-user requirements through product definition. Product quality and reliability is designed into the device architecture and is further assured through rigorous standards for fabrication, assembly and testing. Crystal's part numbering scheme is as follows:

CSLXXXX - TPNNH/R

DEVICE REVISION: DOES NOT APPEAR HERE ON PACKAGE MARK.
REVISION IS COVERED IN DATE CODE STAMP.
USED ONLY FOR ORDERING/TRACKING.

SPECIAL HANDLING ,ALPHA ONLY — A-COMMERCIAL HIGH-REL; B-MILITARY 883B REV. C PROCESSING

ELECTRICAL OR SPEED SPECIFICATION. (OPTIONAL) UP TO 2 NUMERIC DIGITS. NO ALPHA CHARACTERS. SEE DATA SHEET

PACKAGE CODE -REQUIRED ,ALPHA CHARACTER ONLY,NO NUMERICS

P = PLASTIC DIP	S= 0.3" SOIC
C = CERAMIC SIDEBRAZE	E= CERAMIC LCC
D = CERDIP	J= J-LEAD CERAMIC CHIP CARRIER
L = PLASTIC LEADED CHIP CARRIER,J LEAD	G= GULLWING CERAMIC CHIP CARRIER
U= UNPACKAGED DIE	Q= PLASTIC QUAD FLATPACK

TEMPERATURE SPECIFICATION - REQUIRED,ALPHA CHARACTER ONLY
SIGNAL CONDITIONING/COMMUNICATION:

C = 0°C to 70°C
I = -40°C to 85°C
M = -55°C to 125°C

TEMPERATURE/ACCURACY - REQUIRED,ALPHA CHARACTER ONLY
DATA ACQUISITION:

TEMPERATURE	ACCURACY		
	GOOD	BETTER	BEST
0°C to 70°C	J	K	L
-40°C to 85°C	A	B	C
-55°C to 125°C	S	T	U

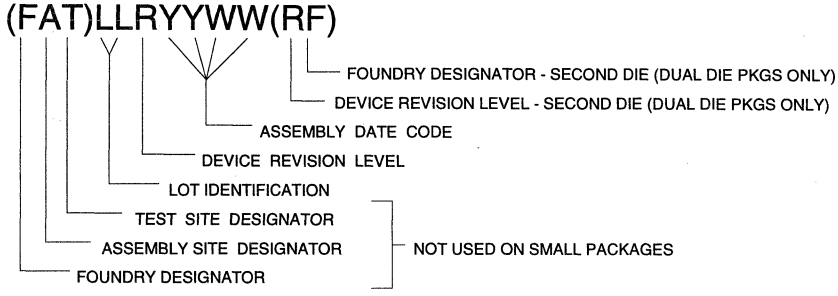
UP TO FOUR ALPHANUMERIC DIGITS COMPRISE REMAINDER OF BASIC PART NUMBER

CRYSTAL PRODUCT LINE (PROPRIETARY PARTS; SECOND-SOURCE PARTS HAVE EXCEPTIONS):
3 = DATA ACQ. SUPPORT CIRCUITS
42 = CODECS
43 = D/A CONVERTERS
5 = A/D CONVERTERS
6 = TELECOMMUNICATIONS
7 = SIGNAL CONDITIONING
8 = DATACOMMUNICATIONS

CRYSTAL SEMICONDUCTOR
"CS" = ALL CRYSTAL PRODUCTS;EXCEPT FOR
"CXT" = QUARTZ CRYSTALS
"CDB" = EVALUATION BOARD
"CX" = CUSTOM PRODUCTS

REV5

In addition to the part number, all Crystal parts have a second line of marking, which can be decoded as follows:



LOT CODE IDENTIFIER - TWO DIGIT ALPHA CHARACTER. IDENTIFIER SEQUENCE WILL BEGIN WITH AA,AB,AC, ETC. EACH LOT WILL RECEIVE A UNIQUE IDENTIFIER REGARDLESS OF DEVICE OR START DATE. SEQUENCE BEGINS AGAIN WITH AA WHEN ZZ HAS BEEN UTILIZED.

COMPANY BACKGROUND

Crystal Semiconductor Corporation was founded in 1984 with the goal of supplying the industry with high-performance, mixed analog/digital CMOS circuits. In 1991, Crystal became a wholly owned subsidiary of Cirrus Logic.

To meet its objectives, Crystal recruited a staff of renowned CMOS analog design engineers, a scarce resource in the industry, and teamed them with designers trained in system architecture development.

By coupling this design staff with highly qualified application and test engineers and seasoned management, Crystal has achieved several industry firsts. Systems designers now benefit from the performance and cost savings of Crystal breakthroughs such as self-calibrating ADCs, monolithic T1 interfaces and the industry's first implementations of "delta sigma" oversampling A-to-D converters.

Headquartered in Austin, Texas, Crystal sells its products worldwide through a network of manufacturer's representatives. Crystal's entire marketing and sales organization is committed to providing quality products and reliable, rapid service.

QUALITY AND RELIABILITY INFORMATION

Crystal Semiconductor is committed at every level of the company to the highest possible standards of quality and reliability in its products. This commitment is evident in all phases of operations: initial product definition, design, fabrication, assembly, test, qualification and customer service. Product quality and reliability are active concerns of each Crystal employee. Quality is ingrained in every operation throughout the product life cycle. Some of the key operations are discussed below.

In Product Definition

To ensure maximum system performance, Crystal works with users to identify and quantify the parameters, including quality and reliability issues, that best serve customer needs. Quality and reliability become part of the design goals, along with electrical performance and cost.

In Design

Conservative CMOS design rules are the basis for all current Crystal products. In addition, extensive use is made of proven standard cells to drastically reduce the possibility of design errors.

Each pin in every SMART *Analog* product is designed to meet ESD levels of at least 2500V when tested per MIL STD 883C, Method 3015. Each pin is also designed to withstand more than 200mA of DC latch-up current.

Crystal SMART *Analog* design architectures provide quality and reliability comparable to leading digital devices and memories. This is far superior to traditional analog ICs and hybrids. Designs which use digital error correction achieve stable performance over time and temperature by taking advantage of digital controls that are insensitive to parametric analog problems such as leakages and shifts in threshold voltage. Using Crystal devices, designers have fewer error sources to consider. The result is a less complicated, more reliable system.

In Fabrication and Assembly

Crystal ensures reliable delivery of quality parts by accessing established foundries in multiple locations worldwide. Each fabrication facility is qualified by Crystal. Assembly is performed both domestically and offshore under carefully documented and well-controlled conditions.

Wafer fabrication and assembly processes undergo in-line quality inspections. Wafers are inspected optically to guidelines based on MIL STD 883C, Method 2010. Each die is electrically tested using proprietary test circuits that verify key parameters. Following assembly, packages are subjected to a variety of mechanical inspections to verify integrity and insure high quality. (For example, x-ray inspection is one of the standard production tests.)

In Test

In a break from traditional analog components, Crystal's SMART Analog products include basic test capabilities designed into each chip. Crystal's in-process quality assurance program uses this designed-in testability to monitor and track the performance and quality of these complex circuits. Finished packaged components are tested 100 percent electrically, over temperature where critical parameters are involved. With these extensive quality programs, Crystal guarantees outgoing electrical quality levels on all data sheet specifications to a 0.065 percent AQL level over the full specified temperature range.

Throughout the assembly and test phases, traceability to the original wafer lot is carefully maintained.

In Product Qualification

Before any Crystal product is released to production and shipped in volume, it must undergo a thorough qualification program. Crystal has separate qualification criteria to address both long-term reliability and infant mortality so that the sources of failure are identified and eliminated. Crystal uses military specifications as the guidelines for reliability tests, methods and procedures. (See Qualification Criteria Table)

To ensure reliability of the design and processes, full qualification requires that three non-consecutive lots are used during the qualification program. Fabrication and assembly facilities are audited every six months and routinely monitored. Any major design or process changes are re-qualified.

These steps guarantee that Crystal products maintain the high standards of reliability designed-in from the start.

In Customer Service

Compliance with purchasing requirements is ensured through the use of Crystal's computerized system "Compass" (Crystal Online Marketing, Production, and Sales System). This processing system ensures that all orders are entered correctly, scheduled properly, produced according to schedule, and shipped with zero discrepancies.

All systems and procedures at Crystal Semiconductor are aimed at continuously improving the quality and reliability of our products and services to meet the needs of our customers.

Crystal's philosophy on quality is to anticipate problems and develop systems and controls to alleviate possible problems. It is a well stated fact by Juran and Deming, two of the nation's foremost experts on quality, that 85% of all quality problems are system related and 15% are worker related. Therefore, Crystal devotes its major quality efforts toward preventing system related quality problems.

Crystal has a very aggressive audit program in place. Monthly internal audits are performed to insure compliance to the extensive documentation of instructions and criteria for testing and inspection. Semi-annual vendor audits are performed on the assembly and fabrication foundries. Vendor audits insure the adequacy and compliance of specifications, product flow, training, process controls and cleanliness. All internal and external audits have provisions for ratings and a system for corrective action requirements. These frequent audits by assembly, fabrication and quality engineers maximize system quality compliance.

As an added measure of continued high quality from assembly and fabrication foundries, thorough incoming inspections are performed. Wafer level optical inspection is based upon guidelines of MIL STD 883C, METHOD 2010. Test die or scribe line monitors are electrically tested to verify compliance to key process parameters based upon design rule specifications. These electrical parameters include threshold voltages, breakdown voltages, material resistance, and contact resistance. Assembly packaging inspection includes external visual, marking permanency, solderability, x-ray, hermeticity, die shear, wirepull and internal visual.

Preventive measures are very much in force in the final test area. Equipment calibration and preventive maintenance procedures are strictly adhered to. Handling procedures for Electrostatic Discharge are in place throughout the test areas. Non-conforming material is segregated until disposition by a material review board. There are controlled procedures for releasing new test programs and new test equipment to the production environment. In summary, Crystal Semiconductor is committed to meet the quality requirements of its customers.

Qualification Criteria Table

	Method	Production Level III	Production Level II	World Class Level I	Units
Quality Performance					
Outgoing Quality (elec./vis-mech/ship.)	Crystal Spec.	1000	500	100	DPM
Fault Coverage (Digital)		n/a	n/a	95%	%
Datasheet Test Coverage (Digital)	Datasheet	100%	100%	100%	%
Datasheet Test Coverage (Analog)	Datasheet	100%	100%	100%	%
ESD - Human Body Model	MIL 3015	1500	2000	4000	V
ESD - Machine Model	MIL3015	--	--	300	V
Latchup - Power Supply[1]	JEDEC 17	Vcc+1V	Vcc+50%	Vcc+50%	V
Latchup - I/O[1]	JEDEC 17	±50	±100	±200	mA
Reliability Performance					
Infant Mortality (48hrs@125°C or equiv.)[2]	MIL 1005	--	--	1000	DPM
Early Life (168hrs@125°C or 1yr. equiv.)[3]	MIL 1005	1/167[4]	500	300	FITS
Operating Life (1000hrs@125°C or 10yr, equiv.)[3]	MIL 1005	500	300	100	FITS
Moisture Performance					
Moisture Resistance - THB (plastic pkgs)	JEDEC 22B	500/5%	1k/5%	1k/3%	hrs/%LTPD per lot[5]
Autoclave (plastic pkgs)	JEDEC 22B	96/5%	144/5%	144/3%	hrs/%LTPD per lot[5]
Mechanical Performance					
Temp Cycle (plastic pkgs)	MIL 1010	500/5%	1k/5%	1k/3%	#cy/%LTPD per lot[5]
Thermal Shock (plastic pkgs)	MIL1011	200/5%	500/5%	1k/3%	#cy/%LTPD per lot[5]
Temp Cycle w/ Hermeticity (hermetic pkgs)	MIL1010/14	500/5%	1k/5%	1k/3%	#cy/%LTPD per lot[5]
Thermal Shock w/ Hermeticity (hermetic pkgs)	MIL 1011/14	200/5%	500/5%	1k/3%	#cy/%LTPD per lot[5]
Soak &VPR (surface mount plastic pkgs)	Crystal Spec.	3/5%	3/3%	3/1%	#cy/%LTPD per lot[5]
Xray	Crystal Spec.	2.50%	2.50%	0.65%	%AQL per lot[5]
Dimensions	MIL 2016	2.50%	2.50%	0.65%	%AQL per lot[5]
Solderability	MIL 2003	2.50%	2.50%	0.65%	%AQL per lot[5]
Lead Integrity & Lead Pull	MIL 2004	2.50%	2.50%	0.65%	%AQL per lot[5]
Mark Permanency	MIL2015	2.50%	2.50%	0.65%	%AQL per lot[5]
Product Integrity					
Design Rule and LVS Checks	Crystal Spec.	yes	yes	yes	
Design for Reliability & Packaging	Crystal Spec.	yes	yes	yes	
Product Characterization	Crystal Spec.	limited	full	statistical	
Test guardbands	Crystal Spec.	some	100%	100%	
Construction Analysis					
Wafer cross section & topo	Crystal Spec.	yes	yes	yes	
SEM metallization	MIL 2018	yes	yes	yes	
Package	Crystal Spec.	yes	yes	yes	

Notes:
1. at High Temperatures (exc. Lev.IV)
2. Point Estimate
3. 55°C, 0.7eV, 60%UCL
4. #accept/n
5. LTPD and AGL criteria in table above apply to each lot tested. CUM LTPD and AQL numbers are also required for Level II:

Individual Lot	Cum Lot Requirement
5% LTPD	3% LTPD
3% LTPD	1% LTPD
2.5% AQL	1.0% AQL

• Notes •

GENERAL PURPOSE A/D CONVERTERS

CS5317 16-bit Voice Band ADC

The CS5317 is well suited for a wide range of voice-band applications, from speech recognition to passive sonar. An on-chip PLL/Clock generator makes the part perfect for high-performance modems. The device features a 20 kHz word rate, a 10 kHz bandwidth, 84 dB dynamic range and 80 dB THD.

CS5012A, CS5014, CS5016 SAR Family

The CS5012A, CS5014 and CS5016 converters have 12, 14 & 16 bits of resolution respectively, with conversion times of 7 µs to 16 µs. On-chip self-calibration ensures that linearity, offset and full-scale errors remain within specification, with no missing codes.

CS5102A 16-bit 20 kHz Low Power ADC

The CS5102A is a low power version of the CS5101A. Requiring only 44 mW from ±5 V supplies, along with a 1 mW power down mode, the CS5102A is ideal for battery powered applications.

CS5101A, CS5126 16-bit 100 kHz ADC

The CS5101A is a 16-bit ADC capable of converting in 8 µs, yielding sample rates of 100 kHz. A 2-channel analog input mux is included. The CS5126 is a low-cost version of the CS5101A, intended for signal processing applications.

CS5030, CS5031, CS5032 12-bit 500kHz ADCs

The CS5030/1 feature a 1 ppm/°C on-chip reference. This yields a 12-bit ADC which has a total unadjusted error (including reference error) of <±0.5 LSB over the military temperature range. The CS5032 is a low cost version with a 60 ppm/°C reference.

CS7870, CS7875 12-bit 100 kHz Sampling ADC

The CS7870 and CS7875 are complete monolithic CMOS ADCs providing 100 kHz throughput. Conversion results are available in either 12-bit parallel, two 8-bit bytes, or serial data. The CS7870 has a ±3V analog input range while the CS7875 accepts input signals from 0V to +5V.

Specifications	CS5317	CS5012A CS5014 CS5016	CS5102A	CS5101A CS5126	CS5030 CS5031 CS5032	CS7870 CS7875
Resolution (bits)	16	12/14/16	16	16	12	12
Application	Modem	GP	GP	GP	GP	GP
Throughput (kHz)	20	100/56/50	20	100	500	100
Conversion Time (µs)	-	7/14/16	40	8	2	10
Integral Non-Linearity	-	.006/.002/ .001%	.0015%	.0015%	.25 LSB	0.25 LSB
Differential (±LSB) Non-Linearity	NMC	0.25/0.25/ NMC	NMC	NMC	0.5	0.5
No Missing Codes	16	12/14/16	16	16	12	12
Total Harmonic Distortion (%)	.007	.008/.003/ .001	.001	.001	.01	.01
Signal-to-Noise plus Distortion (dB)	80	73/83/92	92	92	72	72
Dynamic Range (dB)	84	73/83/92	92	92	72	73
Power Needed (mW)	220	150	44	280	85	88
Conversion Method	Delta Sigma	Succ. Approx.	Succ. Approx.	Succ. Approx.	Succ. Approx.	Succ. Approx.
Power Down Mode	-	-	✓	✓	-	-
On-Chip Sample and Hold	✓	✓	✓	✓	✓	✓
On-Chip V. Ref	✓	-	-	-	✓	✓
Statically Tested	-	✓	✓	✓	✓	✓
Dynamically Tested	✓	✓	✓	✓	✓	✓
Temperature Range	Com Ind	Com Ind Mil	Com Ind Mil	Com Ind Mil	Ind Mil	Ind Mil
Number of Pins (DIP)	18	40	28	28	24	24
Packages	DIP SOIC	DIP PLCC LCC	DIP PLCC LCC	DIP PLCC LCC	DIP SOIC	DIP PLCC

NMC = No Missing Codes GP = General Purpose

INDUSTRIAL MEASUREMENT AND SEISMIC A/D CONVERTERS

CS5501, CS5503 16/20-bit DC Measurement ADC

The CS5501 and CS5503 feature an on-chip, 6-pole, low-pass filter, with adjustable corner frequencies from 0.1 Hz to 10 Hz. The ADC's achieve linearity errors of 0.0007%, with no missing codes. A highly flexible serial interface, along with 25 mW power consumption, all in a 20 pin package, make the parts ideal for weigh scale and process control applications.

CS5504/5/6/7/8/9 1, 2 & 4-channel, 16/20-bit DC Measurement ADC

Very low power consumption of 1.7 mW, along with an optional 1, 2, or 4-channel input mux, make this part ideal for process control and hand held meter applications. These ADC's are available in 16 or 20 bit versions.

CS5516, CS5520 16/20-bit Bridge Transducer ADC

The CS5516 and CS5520 are complete solutions for digitizing low level signals from strain gauges, load cells and pressure transducers. The devices offer an on-chip software programmable instrumentation amplifier, choice of AC or DC bridge excitation, software selectable reference and signal demodulation.

CS5321, CS5322, CS5323, CS5324 24-bit Variable Bandwidth ADC

The CS5321 or CS5323 modulator, combined with the CS5322 digital filter, offers >120 dB dynamic range in the DC to 500 Hz frequency band. Seven different filter corner frequencies and output update rates are offered, allowing the ADC to be optimized for different types of seismic measurements. The CS5324 includes a modulator and the first stage of digital filtering, allowing users to implement their own final filter stage.

CS5542, CS5543, 22-bit, 8-channel Data Acquisition System

The CS5542 is a 2-channel, 5th order delta-sigma modulator intended for direct digitization of transducer currents. The CS5543 is an 8-channel digital FIR filter. Up to four CS5542's may be connected with one CS5543 to form an 8-channel data acquisition system. The output word rate is 1000 Hz per channel.

Specifications	CS5501 CS5503	CS5504 CS5507 CS5505 CS5508 CS5506 CS5509	CS5516 CS5520	CS5321 CS5323 CS5322 CS5324	CS5542 CS5543
Input Bandwidth	10 Hz	10 Hz	12 Hz	500 Hz	250/500 Hz
Resolution (bits)	16/20	16/20	16/20	24	22
Application	DC Measurement			Seismic	DC Measurement
Throughput (kHz)	4	100/200Hz	60Hz	-	1KHz
Integral Non-Linearity	.0007%	.0015%	.0007%	-	.001%
Differential (±LSB) Non-Linearity	0.125/ NMC	0.125	0.5	NMC	0.5
Total Harmonic Distortion (%)	-	-	-	.0003	-
Dynamic Range (dB)	-	-	-	120	113
Power Needed (mW)	25	3	40	150	80/75
Conversion Method	Delta Sigma	Delta Sigma	Delta Sigma	Delta Sigma	Delta Sigma
Power Down Mode	✓	✓	✓	✓	✓
On-Chip Sample and Hold	✓	✓	✓	✓	✓
On-Chip V. Ref	-	✓	-	-	-
On-Chip Filtering	✓	✓	✓	✓	✓
Temperature Range	Ind, Mil	Ind	Ind	Ind	Ind
Number of Pins (DIP)	20	20/24	24	28	28/44
Packages	DIP SOIC	DIP SOIC	DIP SOIC	PLCC	PLCC

NMC = No Missing Codes

HIGH SPEED A/D CONVERTERS

CS5412 12-bit 1 MHz ADC

Using a 2-step flash approach, the CS5412 achieves 12-bit performance at a 1 MHz sample rate. Self calibration ensures accuracy over time and the military temperature range. Available in both DIP and J-lead LCC packages, with on-chip S/H, the IC offers a very compact ADC solution.

CS5480, CS5481 10-bit 40/20 MHz ADC

The CS5480 is a monolithic CMOS 10-bit sampling ADC capable of 40 Msps conversion rates. The CS5481 is a 10-bit sampling ADC capable of 20 Msps conversion rates. Digital inputs are CMOS and TTL compatible, and the digital outputs are CMOS compatible. Output data is available in offset binary format.

CS5490 12-bit 20MHz ADC

The CS5490 is a 12-bit sampling ADC capable of 20 Msps conversion rates. Digital inputs are CMOS and TTL compatible, and the digital outputs are CMOS compatible. Output data is available in offset binary format.

CDBCAPTURE SYSTEM

Data Capture and Interface Board for a PC

The CAPTURE interface board is a development tool that can be easily interface to Crystal Semiconductor Evaluation boards. Application software, developed with Lab Windows, adjusts the CAPTURE interface board for the appropriate signal timing and polarity, coding format and number of bits.

Specifications	CS5412	CS5480	CS5481	CS5490
Input Bandwidth	4 MHz	200 MHz	200 MHz	200 MHz
Resolution (bits)	12	10	10	12
Application	GP Fast	High Speed	High Speed	High Speed
Throughput	1 MHz	40 MHz	20 MHz	20 MHz
Integral Non-Linearity (±LSB)	1	1	1	1
Differential Non-Linearity (±LSB)	0.9	0.5	0.5	0.5
No Missing Codes	12	10	10	12
Total Harmonic Distortion	-78 dB	-54 dB	-54 dB	-63 dB
Signal-to-Noise plus Distortion (dB)	70	58	58	62
Dynamic Range (dB)	70	62	62	70
Power Needed (mW)	750	375	225	225
Conversion Method	2-Step Flash	Pipeline	Pipeline	Pipeline
On-Chip Sample and Hold	✓	✓	✓	✓
On-Chip V. Ref	-	✓	✓	✓
Temperature Range	Com Ind Mil	Ind	Ind	Ind
Number of Pins	40/44	28	28	44
Packages	DIP JLCC	PLCC	PLCC	PLCC

NMC = No Missing Codes GP = General Purpose

DATA ACQUISITION PRODUCTS

• Notes •

16, 14 & 12-Bit, Self-Calibrating A/D Converters

Features

- Monolithic CMOS A/D Converters
  - Microprocessor Compatible
  - Parallel and Serial Output
  - Inherent Track/Hold Input
- True 12, 14 and 16-Bit Precision
- Conversion Times:
  - CS5016 16.25 µs
  - CS5014 14.25 µs
  - CS5012A 7.20 µs
- Self Calibration Maintains Accuracy Over Time and Temperature
- Low Power Dissipation: 150 mW
- Low Distortion

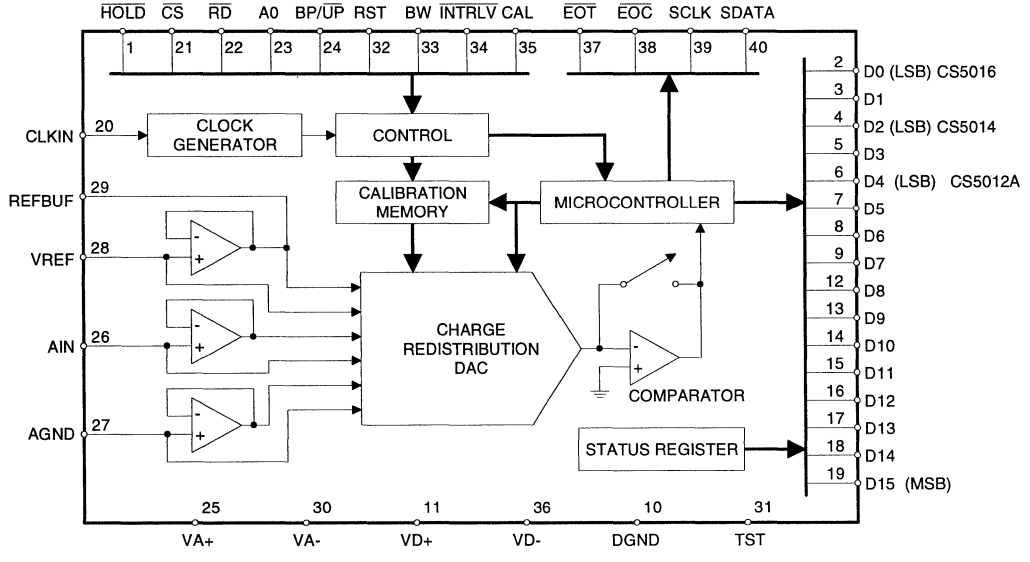
General Description

The CS5012A/14/16 are 12, 14 and 16-bit monolithic analog to digital converters with conversion times of 7.2µs, 14.25µs and 16.25µs. Unique self-calibration circuitry insures excellent linearity and differential non-linearity, with no missing codes. Offset and full scale errors are kept within 1/2 LSB (CS5012A/14) and 1 LSB (CS5016), eliminating the need for calibration. Unipolar and bipolar input ranges are digitally selectable.

The pin compatible CS5012A/14/16 consist of a DAC, conversion and calibration microcontroller, oscillator, comparator, microprocessor compatible 3-state I/O, and calibration circuitry. The input track-and-hold, inherent to the devices' sampling architecture, acquires the input signal after each conversion using a fast slewing on-chip buffer amplifier. This allows throughput rates up to 100 kHz (CS5012A), 56 kHz (CS5014) and 50 kHz (CS5016).

An evaluation board (CDB5012/14/16) is available which allows fast evaluation of ADC performance.

ORDERING INFORMATION: Pages 2-45, 2-46, & 2-47



CS5012A ANALOG CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 2.5V to 4.5V; f_{clk} = 6.4 MHz for -7, 4 MHz for -12; Analog Source Impedance = 200Ω)

Parameter*		CS5012A-K Min	CS5012A-K Typ	CS5012A-K Max	CS5012A-B Min	CS5012A-B Typ	CS5012A-B Max	CS5012-T Min	CS5012-T Typ	CS5012-T Max	Units
Specified Temperature Range			0 to +70			-40 to +85			-55 to +125		°C
Accuracy											
Linearity Error	(Note 1)		±1/4	±1/2		±1/4	±1/2		±1/4	±1/2	LSB_{12}
Drift	(Note 2)		±1/8			±1/8			±1/8		ΔLSB_{12}
Differential Linearity	(Note 1)		±1/4	±1/2		±1/4	±1/2		±1/4	±1/2	LSB_{12}
Drift	(Note 2)		±1/32			±1/32			±1/32		ΔLSB_{12}
Full Scale Error	(Note 1)		±1/4	±1/2		±1/4	±1/2		±1/4	±1/2	LSB_{12}
Drift	(Note 2)		±1/16			±1/16			±1/8		ΔLSB_{12}
Unipolar Offset	(Note 1)		±1/4	±1/2		±1/4	±1/2		±1/4	±1/2	LSB_{12}
Drift	(Note 2)		±1/16			±1/16			±1/16		ΔLSB_{12}
Bipolar Offset	(Note 1)		±1/4	±1/2		±1/4	±1/2		±1/4	±1/2	LSB_{12}
Drift	(Note 2)		±1/16			±1/16			±1/16		ΔLSB_{12}
Bipolar Negative Full-Scale Error	(Note 1)		±1/4	±1/2		±1/4	±1/2		±1/4	±1/2	LSB_{12}
Drift	(Note 2)		±1/16			±1/16			±1/16		ΔLSB_{12}
Total Unadjusted Error	(Note 1)		±1/4			±1/4			±1/4		LSB_{12}
Drift	(Note 2)		±1/4			±1/4			±1/4		ΔLSB_{12}
Dynamic Performance (Bipolar Mode)											
Peak Harmonic or Spurious Noise	(Note 1)										
Full Scale, 1 kHz Input		84	92		84	92		84	92		dB
Full Scale, 12 kHz Input		84	88		84	88		84	88		dB
Total Harmonic Distortion			0.008			0.008			0.008		%
Signal-to-Noise Ratio	(Note 1)										
1 kHz, 0 dB Input		72	73		72	73		72	73		dB
1 kHz, -60 dB Input			13			13			13		dB
Noise	(Note 3)										
Unipolar Mode			45			45			45		μV_{rms}
Bipolar Mode			90			90			90		μV_{rms}

Notes: 1. Applies after calibration at any temperature within the specified temperature range.
2. Total drift over specified temperature range since calibration at power-up at 25 °C
3. Wideband noise aliased into the baseband. Referred to the input.

* Refer to *Parameter Definitions* (immediately following the pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

CS5012A ANALOG CHARACTERISTICS (continued)

Parameter*	CS5012A-K Min	CS5012A-K Typ	CS5012A-K Max	CS5012A-B Min	CS5012A-B Typ	CS5012A-B Max	CS5012-T Min	CS5012-T Typ	CS5012-T Max	Units
Specified Temperature Range		0 to +70			-40 to +85			-55 to +125		°C
Analog Input										
Aperture Time		25			25			25		ns
Aperture Jitter		100			100			100		ps
Input Capacitance (Note 4)										
Unipolar Mode CS5012		275	375		275	375		275	375	pF
CS5012A		103	137		103	137		103	137	pF
Bipolar Mode CS5012		165	220		165	220		165	220	pF
CS5012A		72	96		72	96		72	96	pF
Conversion & Throughput										
Conversion Time -7 (Notes 5 and 6)			7.2			7.2				µs
-12			12.25			12.25			12.25	µs
Acquisition Time -7 (Note 6)		2.5	2.8		2.5	2.8				µs
-12		3.0	3.75		3.0	3.75		3.0	3.75	µs
Throughput -7 (Note 6)	100			100						kHz
-12	62.5			62.5			62.5			kHz
Power Supplies										
DC Power Supply Currents (Note 7)										
I_{A+}		12	19		12	19		12	19	mA
I_{A-}		-12	-19		-12	-19		-12	-19	mA
(CS5012) I_{D+}		3	6		3	6		3	6	mA
(CS5012A) I_{D+}		6	7.5		6	7.5				mA
I_{D-}		-3	-6		-3	-6		-3	-6	mA
Power Dissipation (Note 7)		150	250		150	250		150	250	mW
Power Supply Rejection (Note 8)										
Positive Supplies		84			84			84		dB
Negative Supplies		84			84			84		dB

Notes:
4. Applies only in track mode. When converting or calibrating, input capacitance will not exceed 15 pF.
5. Measured from falling transition on $\overline{HOLD}$ to falling transition on $\overline{EOC}$.
6. Conversion, acquisition, and throughput times depend on CLKIN, sampling, and calibration conditions. The numbers shown assume sampling and conversion is synchronized with the CS5012A/14/16 's conversion clock, interleave calibrate is disabled, and operation is from the full-rated, external clock. Refer to the section *Conversion Time/Throughput* for a detailed discussion of conversion timing.
7. All outputs unloaded. All inputs CMOS levels.
8. With 300 mV p-p, 1 kHz ripple applied to each analog supply separately in bipolar mode. Rejection improves by 6 dB in the unipolar mode to 90 dB. Figure 13 shows a plot of typical power supply rejection versus frequency.

CS5014 ANALOG CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 4.5V; CLKIN = 4 MHz for -14, 2 MHz for -28; Analog Source Impedance = 200Ω)

Parameter*			CS5014-K Min	CS5014-K Typ	CS5014-K Max	CS5014-B Min	CS5014-B Typ	CS5014-B Max	CS5014-S, T Min	CS5014-S, T Typ	CS5014-S, T Max	Units
Specified Temperature Range				0 to +70			-40 to +85			-55 to +125		°C
Accuracy												
Linearity Error	K, B, T	(Note 1)		±1/4	±1/2		±1/4	±1/2		±1/4	±1/2	LSB_{14}
	S									±1/2	±1.5	LSB_{14}
Drift		(Note 2)		±1/8			±1/8			±1/8		ΔLSB_{14}
Differential Linearity		(Note 1)		±1/4	±1/2		±1/4	±1/2		±1/4	±1/2	LSB_{14}
Drift		(Note 2)		±1/32			±1/32			±1/32		ΔLSB_{14}
Full Scale Error		(Note 1)		±1/2	±1		±1/2	±1		±1/2	±1	LSB_{14}
Drift		(Note 2)		±1/4			±1/4			±1/2		ΔLSB_{14}
Unipolar Offset	K, B, T	(Note 1)		±1/4	±3/4		±1/4	±3/4		±1/4	±3/4	LSB_{14}
	S										±1	LSB_{14}
Drift		(Note 2)		±1/4			±1/4			±1/2		ΔLSB_{14}
Bipolar Offset	K, B, T	(Note 1)		±1/4	±3/4		±1/4	±3/4		±1/4	±3/4	LSB_{14}
	S										±1	LSB_{14}
Drift		(Note 2)		±1/4			±1/2			±1/2		ΔLSB_{14}
Bipolar Negative Full-Scale Error		(Note 1)										
	K, B, T			±1/2	±1		±1/2	±1		±1/2	±1	LSB_{14}
	S										±1.5	LSB_{14}
Drift		(Note 2)		±1/4			±1/4			±1/2		ΔLSB_{14}
Total Unadjusted Error		(Note 1)		±1			±1			±1		LSB_{14}
Drift		(Note 2)		±1/2			±1			±1		ΔLSB_{14}
Dynamic Performance (Bipolar Mode)												
Peak Harmonic or Spurious Noise		(Note 1)										
Full Scale, 1 kHz Input	K, B, T		94	98		94	98		94	98		dB
	S								85			dB
Full Scale, 12 kHz Input	K, B, T		84	87		84	87		84	87		dB
	S								80			dB
Total Harmonic Distortion				0.003			0.003			0.003		%
Signal-to-Noise Ratio		(Notes 1 and 9)										
1 kHz, 0 dB Input	K, B, T		82	84		82	84		82	84		dB
	S								80			dB
1 kHz, -60 dB Input				23			23			23		dB
Noise		(Note 3)										
Unipolar Mode				45			45			45		μV_{rms}
Bipolar Mode				90			90			90		μV_{rms}

Notes: 9. A detailed plot of S/(N+D) vs. input amplitude appears in Figure 26 for the CS5014 and Figure 28 for the CS5016.

* Refer to *Parameter Definitions* (immediately following the pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

CS5014 ANALOG CHARACTERISTICS (continued)

Parameter*	CS5014-K Min	CS5014-K Typ	CS5014-K Max	CS5014-B Min	CS5014-B Typ	CS5014-B Max	CS5014-S, T Min	CS5014-S, T Typ	CS5014-S, T Max	Units
Specified Temperature Range		0 to +70			-40 to +85			-55 to +125		°C
Analog Input										
Aperture Time		25			25			25		ns
Aperture Jitter		100			100			100		ps
Input Capacitance (Note 4)										
Unipolar Mode		275	375		275	375		275	375	pF
Bipolar Mode		165	220		165	220		165	220	pF
Conversion & Throughput										
Conversion Time -14 (Notes 5 and 6)			14.25			14.25			14.25	µs
-28			28.5			28.5			28.5	µs
Acquisition Time -14 (Note 6)		3.0	3.75		3.0	3.75		3.0	3.75	µs
-28		4.5	5.25		4.5	5.25		4.5	5.25	µs
Throughput -14 (Note 6)	55.6			55.6			55.6			kHz
-28	27.7			27.7			27.7			kHz
Power Supplies										
DC Power Supply Currents (Note 7)										
I_{A+}		9	19		9	19		9	19	mA
I_{A-}		-9	-19		-9	-19		-9	-19	mA
I_{D+}		3	6		3	6		3	6	mA
I_{D-}		-3	-6		-3	-6		-3	-6	mA
Power Dissipation (Note 7)		120	250		120	250		120	250	mW
Power Supply Rejection (Note 8)										
Positive Supplies		84			84			84		dB
Negative Supplies		84			84			84		dB

CS5016 ANALOG CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 4.5V; CLKIN = 4 MHz for -16, 2 MHz for -32; Analog Source Impedance = 200Ω; Synchronous Sampling.)

Parameter*			CS5016-J, K Min	CS5016-J, K Typ	CS5016-J, K Max	CS5016-A, B Min	CS5016-A, B Typ	CS5016-A, B Max	CS5016-S, T Min	CS5016-S, T Typ	CS5016-S, T Max	Units
Specified Temperature Range				0 to +70			-40 to +85			-55 to +125		°C
Accuracy												
Linearity Error	J, A, S	(Note 1)		0.002	0.003		0.002	0.003		0.002	0.0076	%FS
	K, B, T			0.001	0.0015		0.001	0.0015		0.001	0.0015	%FS
Drift		(Note 2)		±1/4			±1/4			±1/4		ΔLSB_{16}
Differential Linearity		(Note 10)	16			16			16			Bits
Full Scale Error	J, A, S	(Note 1)		±2	±3		±2	±3		±2	±4	LSB_{16}
	K, B, T			±2	±3		±2	±3		±2	±3	LSB_{16}
Drift		(Note 2)		±1			±1			±2		ΔLSB_{16}
Unipolar Offset	J, A, S	(Note 1)		±1	±2		±1	±3		±1	±4	LSB_{16}
	K, B, T			±1	±3/2		±1	±3		±1	±3	LSB_{16}
Drift		(Note 2)		±1			±1			±2		ΔLSB_{16}
Bipolar Offset	J, A, S	(Note 1)		±1	±2		±1	±2		±1	±4	LSB_{16}
	K, B, T			±1	±3/2		±1	±2		±1	±2	LSB_{16}
Drift		(Note 2)		±1			±2			±2		ΔLSB_{16}
Bipolar Negative Full-Scale Error		(Note 1)										
	J, A, S			±2	±3		±2	±3		±2	±5	LSB_{16}
	K, B, T			±2	±3		±2	±3		±2	±3	LSB_{16}
Drift		(Note 2)		±1			±2			±2		ΔLSB_{16}
Dynamic Performance (Bipolar Mode)												
Peak Harmonic or Spurious Noise		(Note 1)										
Full Scale, 1 kHz Input		J, A, S	96	100		96	100		92	100		dB
		K, B, T	100	104		100	104		100	104		dB
Full Scale, 12 kHz Input		J, A, S	85	88		85	88		82	88		dB
		K, B, T	85	91		85	91		85	91		dB
Total Harmonic Distortion		J, A, S		0.002			0.002			0.002		%
Full Scale, 1 kHz Input		K, B, T		0.001			0.001			0.001		%
Signal-to-Noise Ratio		(Notes 1 and 9)										
1 kHz, 0 dB Input		J, A, S	87	90		87	90		84	90		dB
		K, B, T	90	92		90	92		90	92		dB
1 kHz, -60 dB Input		J, A, S		30			30			30		dB
		K, B, T		32			32			32		dB
Noise		(Note 3)										
Unipolar Mode				35			35			35		μV_{rms}
Bipolar Mode				70			70			70		μV_{rms}

Notes: 10. Minimum resolution for which no missing codes is guaranteed

* Refer to *Parameter Definitions* (immediately following the pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

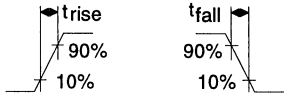
CS5016 ANALOG CHARACTERISTICS (continued)

Parameter*	CS5016-J, K Min	CS5016-J, K Typ	CS5016-J, K Max	CS5016-A, B Min	CS5016-A, B Typ	CS5016-A, B Max	CS5016-S, T Min	CS5016-S, T Typ	CS5016-S, T Max	Units
Specified Temperature Range		0 to +70			-40 to +85			-55 to +125		°C
Analog Input										
Aperture Time		25			25			25		ns
Aperture Jitter		100			100			100		ps
Input Capacitance (Note 4)										
Unipolar Mode		275	375		275	375		275	375	pF
Bipolar Mode		165	220		165	220		165	220	pF
Conversion & Throughput										
Conversion Time -16 (Notes 5 and 6)			16.25			16.25			16.25	µs
-32			32.5			32.5			32.5	µs
Acquisition Time -16 (Note 6)		3.0	3.75		3.0	3.75		3.0	3.75	µs
-32		4.5	5.25		4.5	5.25		4.5	5.25	µs
Throughput -16 (Note 6)	50			50			50			kHz
-32	26.5			26.5			26.5			kHz
Power Supplies										
DC Power Supply Currents (Note 7)										
I_{A+}		9	19		9	19		9	19	mA
I_{A-}		-9	-19		-9	-19		-9	-19	mA
I_{D+}		3	6		3	6		3	6	mA
I_{D-}		-3	-6		-3	-6		-3	-6	mA
Power Dissipation (Note 7)		120	250		120	250		120	250	mW
Power Supply Rejection (Note 8)										
Positive Supplies		84			84			84		dB
Negative Supplies		84			84			84		dB

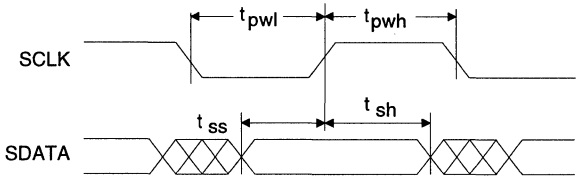
SWITCHING CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+ = 5V ±10%; VA-, VD- = -5V ±10%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF, BW = VD+)

Parameter			Symbol	Min	Typ	Max	Units
CS5012A CLKIN Frequency:			f_{CLK}				
	Internally Generated:			1.75	-	-	MHz
	Externally Supplied:	-7		100 kHz	-	6.4	MHz
		-12		100 kHz	-	4.0	MHz
CS5014/5016 CLKIN Frequency:			f_{CLK}				
	Internally Generated:	-14, -16		1.75	-	-	MHz
		-28, -32		1	-	-	MHz
	Externally Supplied:	-14, -16		100 kHz	-	4	MHz
		-28, -32		100 kHz	-	2	MHz
CLKIN Duty Cycle				40	-	60	%
Rise Times:		Any Digital Input	t_{rise}	-	-	1.0	µs
		Any Digital Output		-	20	-	ns
Fall Times:		Any Digital Input	t_{fall}	-	-	1.0	µs
		Any Digital Output		-	20	-	ns
$\overline{HOLD}$ Pulse Width			t_{hpw}	$1/f_{CLK}+50$	-	t_c	ns
Conversion Time:		CS5012A	t_c	$49/f_{CLK}+50$	-	$53/f_{CLK}+235$	ns
		CS5014		$57/f_{CLK}$	-	$61/f_{CLK}+235$	ns
		CS5016		$65/f_{CLK}$	-	$69/f_{CLK}+235$	ns
Data Delay Time			t_{dd}	-	40	100	ns
$\overline{EOC}$ Pulse Width		(Note 11)	t_{epw}	$4/f_{CLK}-20$	-	-	ns
Set Up Times:	CAL, $\overline{INTRLV}$ to $\overline{CS}$ Low		t_{cs}	20	10	-	ns
	A0 to $\overline{CS}$ and $\overline{RD}$ Low		t_{as}	20	10	-	ns
Hold Times:	$\overline{CS}$ or $\overline{RD}$ High to A0 Invalid		t_{ah}	50	30	-	ns
	$\overline{CS}$ High to CAL, $\overline{INTRLV}$ Invalid		t_{ch}	50	30	-	ns
Access Times:	$\overline{CS}$ Low to Data Valid	A, B, J, K	t_{ca}	-	90	120	ns
		S, T		-	115	150	ns
	$\overline{RD}$ Low to Data Valid	A, B, J, K	t_{ra}	-	90	120	ns
		S, T		-	90	150	ns
Output Float Delay:		K, B	t_{fd}	-	90	110	ns
	$\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z	T		-	90	140	ns
Serial Clock	Pulse Width Low		t_{pwl}	-	$2/f_{CLK}$	-	ns
	Pulse Width High		t_{pwh}	-	$2/f_{CLK}$	-	ns
Set Up Times:	SDATA to SCLK Rising		t_{ss}	$2/f_{CLK}-50$	$2/f_{CLK}$	-	ns
Hold Times:	SCLK Rising to SDATA		t_{sh}	$2/f_{CLK}-100$	$2/f_{CLK}$	-	ns

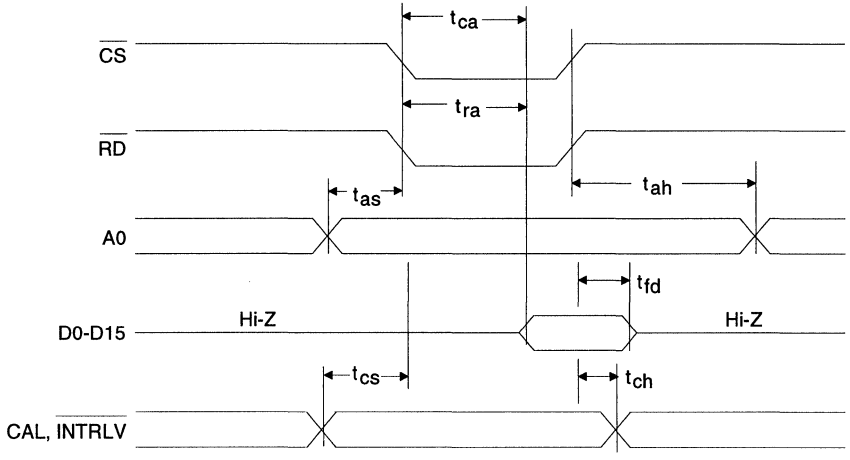
Notes: 11. $\overline{EOC}$ remains low 4 CLKIN cycles if $\overline{CS}$ and $\overline{RD}$ are held low. Otherwise, it returns high within 4 CLKIN cycles from the start of a data read operation or a conversion cycle.



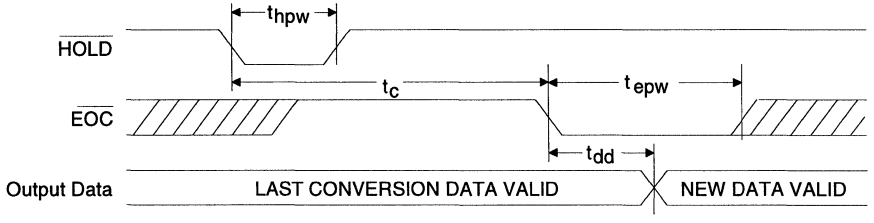
Rise and Fall Times



Serial Output Timing



Read and Calibration Control Timing



Conversion Timing

DIGITAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+ = 5V ±10%; VA-, VD- = -5V ±10%)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage		V_{IH}	2.0	-	-	V
Low-Level Input Voltage		V_{IL}	-	-	0.8	V
High-Level Output Voltage	(Note 12)	V_{OH}	(VD+) - 1.0V	-	-	V
Low-Level Output Voltage	I_{out} = 1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	-	10	µA
3-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

Notes: 12. I_{out} = -100 µA. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{out} = -40 µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see Note 13)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	-4.5	-5.0	-5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	-4.5	-5.0	-5.5	V
Analog Reference Voltage		VREF	2.5	4.5	(VA+) - 0.5	V
Analog Input Voltage:	(Note 14)					
Unipolar		V_{AIN}	AGND	-	VREF	V
Bipolar		V_{AIN}	-VREF	-	VREF	V

Notes: 13. All voltages with respect to ground.
14. The CS5012A/14/16 can accept input voltages up to the analog supplies (VA+ and VA-). It will output all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with repect to ground.)

WARNING: Operation at or beyond these limits may reult in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Parameter			Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	(Note 15)	VD+	-0.3	6.0	V
	Negative Digital		VD-	0.3	-6.0	V
	Positive Analog		VA+	-0.3	6.0	V
	Negative Analog		VA-	0.3	-6.0	V
Input Current, Any Pin Except Supplies		(Note 16)	I_{in}	-	±10	mA
Analog Input Voltage	(AIN and VREF pins)		V_{INA}	(VA-) - 0.3	(VA+) + 0.3	V
Digital Input Voltage			V_{IND}	-0.3	(VA+) + 0.3	V
Ambient Operating Temperature			T_A	-55	125	°C
Storage Temperature			T_{stg}	-65	150	°C

Notes: 15. In addition, VD+ should not be greater than (VA+) + 0.3V.
16. Transient currents of up to 100 mA will not cause SCR latch-up.

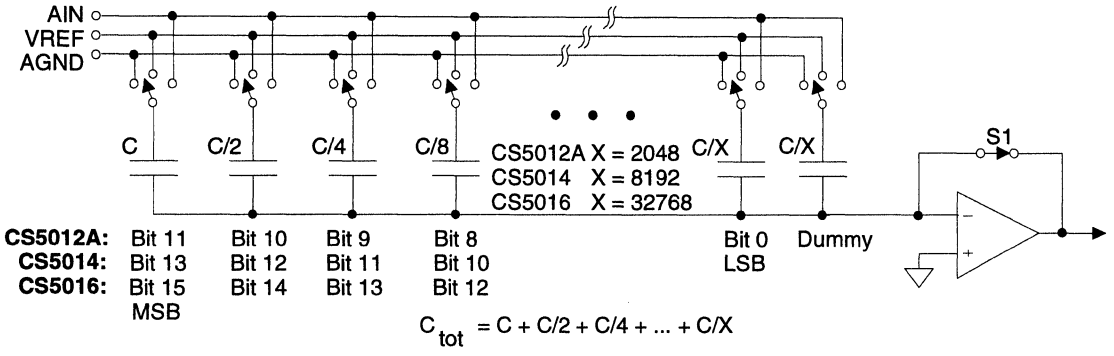


Figure 1. Charge Redistribution DAC

THEORY OF OPERATION

The CS5012A/14/16 family utilize a successive approximation conversion technique. The analog input is successively compared to the output of a D/A converter controlled by the conversion algorithm. Successive approximation begins by comparing the analog input to the DAC output which is set to half-scale (MSB on, all other bits off). If the input is found to be below half-scale, the MSB is reset to zero and the input is compared to one-quarter scale (next MSB on, all others off). If the input were above half-scale, the MSB would remain high and the next comparison would be at three-quarters of full scale. This procedure continues until all bits have been exercised.

A unique charge redistribution architecture is used to implement the successive approximation algorithm. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. All capacitors in the array share a common node at the comparator's input. Their other terminals are capable of being connected to AIN, AGND, or VREF (Figure 1). When the device is not calibrating or converting, all capacitors are tied to AIN forming C_{tot}. Switch S1 is closed and the charge on the array, Q_{in}, tracks the input signal V_{in} (Figure 2a).

When the conversion command is issued, switch S1 opens as shown in Figure 2b. This traps charge Q_{in} on the comparator side of the capacitor array and creates a floating node at the comparator's input. The conversion algorithm operates on this fixed charge, and the signal at the analog input pin is ignored. In effect, the entire DAC capacitor array serves as analog memory

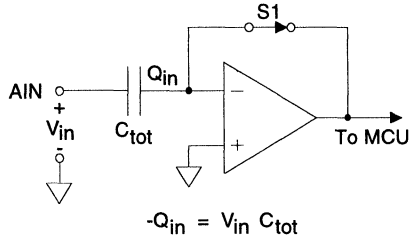


Figure 2a. Tracking Mode

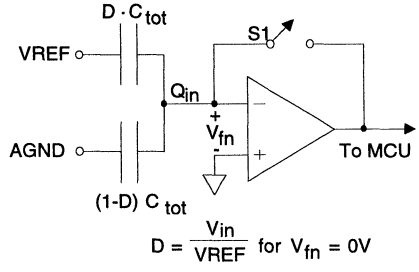


Figure 2b. Convert Mode

during conversion much like a hold capacitor in a sample/hold amplifier.

The conversion consists of manipulating the free plates of the capacitor array to VREF and AGND to form a capacitive divider. Since the charge at the floating node remains fixed, the voltage at that point depends on the proportion of capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance, termed D in Figure 2b, which when connected to the reference will drive the voltage at the floating node (V_{fn}) to zero. That binary fraction of capacitance represents the converter's digital output.

This charge redistribution architecture easily supports bipolar input ranges. If half the capacitor array (the MSB capacitor) is tied to VREF rather than AIN in the track mode, the input range is doubled and is offset half-scale. The magnitude of the reference voltage thus defines both positive and negative full-scale (-VREF to +VREF), and the digital code is an offset binary representation of the input.

Calibration

The ability of the CS5012A/14/16 to convert accurately clearly depends on the accuracy of their comparator and DAC. The CS5012A/14/16 utilize an "auto-zeroing" scheme to null errors introduced by the comparator. All offsets are stored on the capacitor array while in the track mode and are effectively subtracted from the input signal when a conversion is initiated. Auto-zeroing enhances power supply rejection at frequencies well below the conversion rate.

To achieve complete accuracy from the DAC, the CS5012A/14/16 use a novel self-calibration scheme. Each bit capacitor, shown in Figure 1, actually consists of several capacitors which can be manipulated to adjust the overall bit weight. An on-chip microcontroller adjusts the subarrays to precisely ratio the bits. Each bit is adjusted to just balance the sum of all less significant bits plus one dummy LSB (for example, 16C = 8C + 4C + 2C + C + C). Calibration resolution for the array is a small fraction of an LSB resulting in nearly ideal differential and integral linearity.

DIGITAL CIRCUIT CONNECTIONS

The CS5012A/14/16 can be applied in a wide variety of master clock, sampling, and calibration conditions which directly affect the devices' conversion time and throughput. The devices also feature on-chip 3-state output buffers and a complete interface for connecting to 8-bit and 16-bit digital systems. Output data is also available in serial format.

Master Clock

The CS5012A/14/16 operate from a master clock (CLKIN) which can be externally supplied or internally generated. The internal oscillator is activated by externally tying the CLKIN input low. Alternatively, the CS5012A/14/16 can be synchronized to the external system by driving the CLKIN pin with a TTL or CMOS clock signal.

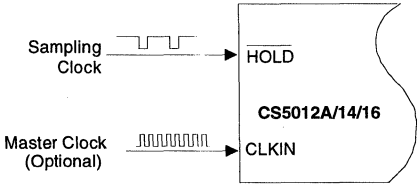


Figure 3a. Asynchronous Sampling

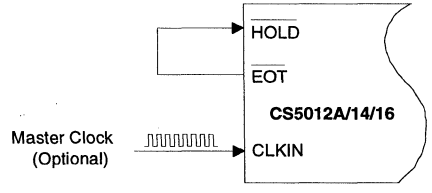


Figure 3b. Synchronous Sampling

All calibration, conversion, and throughput times directly scale to CLKIN frequency. Thus, throughput can be precisely controlled and/or maximized using an external CLKIN signal. In contrast, the CS5012A/14/16's internal oscillator will vary from unit-to-unit and over temperature. The CS5012A/14/16 can typically convert with CLKIN as low as 10 kHz at room temperature.

Initiating Conversions

A falling transition on the $\overline{\text{HOLD}}$ pin places the input in the hold mode and initiates a conversion cycle. Upon completion of the conversion cycle, the CS5012A/14/16 automatically return to the track mode. In contrast to systems with separate track-and-holds and A/D converters, a sampling clock can simply be connected to the $\overline{\text{HOLD}}$ input (Figure 3a). The duty cycle of this clock is not critical. It need only remain low at least one CLKIN cycle plus 50 ns, but no longer than the minimum conversion time or an additional conversion cycle will be initiated with inadequate time for acquisition.

Microprocessor-Controlled Operation

Sampling and conversion can be placed under microprocessor control (Figure 4) by simply gating the devices' decoded address with the write strobe for the $\overline{\text{HOLD}}$ input. Thus, a write cycle to the CS5012A/14/16's base address will initiate a conversion. However, the write cycle must be to the odd address (A0 high) to avoid initiating a software controlled reset (see *Reset* below).

The calibration control inputs, CAL, and $\overline{\text{INTRLV}}$ are inputs to a set of transparent latches. These signals are internally latched by $\overline{\text{CS}}$ returning high. They must be in the appropriate state whenever the chip is selected during a read or write cycle. Address lines A1 and A2 are shown connected to CAL and $\overline{\text{INTRLV}}$ in Figure 4 placing calibration under microprocessor control as well. Thus, any read or write cycle to the CS5012A/14/16's base address will initiate or terminate calibration. Alternatively, A0, $\overline{\text{INTRLV}}$, and CAL may be connected to the microprocessor data bus.

Conversion Time/Throughput

Upon completing a conversion cycle and returning to the track mode, the CS5012A/14/16 require time to acquire the analog input signal before another conversion can be initiated. The acquisition time is specified as six CLKIN cycles plus 2.25 µs (1.32 µs for the CS5012A -7 version only). This adds to the conversion time to define the converter's maximum throughput. The conversion time of the CS5012A/14/16, in turn, depends on the sampling, calibration, and CLKIN conditions.

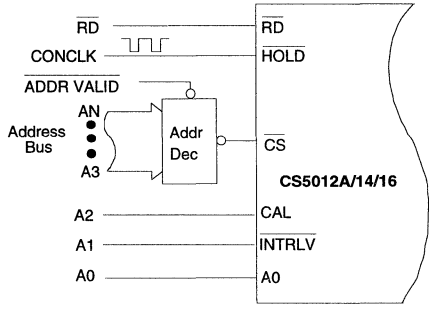


Figure 4a. Conversions Asynchronous to CLKIN

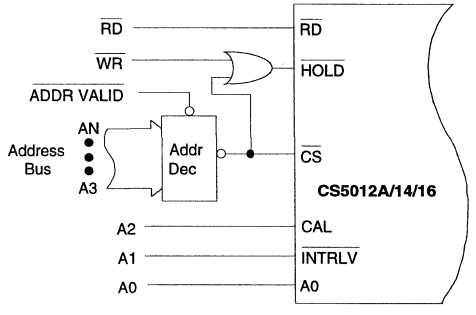


Figure 4b. Conversions under Microprocessor Control

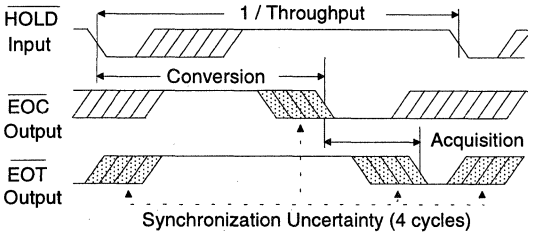


Figure 5a. Asynchronous Sampling (External Clock)

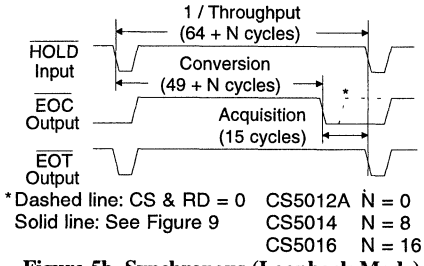


Figure 5b. Synchronous (Loopback Mode)

Asynchronous Sampling

The CS5012A/14/16 internally operate from a clock which is delayed and divided down from CLKIN ($f_{CLK}/4$). If sampling is not synchronized to this internal clock, the conversion cycle may not begin until up to four clock cycles after $\overline{HOLD}$ goes low *even though the charge is trapped immediately.* In this asynchronous mode (Figure 3a), the four clock cycles add to the minimum 49, 57 and 65 clock cycles (for the CS5012A/14/16 respectively) to define the maximum conversion time (see Figure 5a and Table 1).

Synchronous Sampling

To achieve maximum throughput, sampling can be synchronized with the internal conversion clock by connecting the End-of-Track ($\overline{EOT}$) output to $\overline{HOLD}$ (Figure 3b). The $\overline{EOT}$ output falls 15 CLKIN cycles after $\overline{EOC}$ indicating the analog input has been acquired to the CS5012A/14/16's specified accuracy. The $\overline{EOT}$ output is synchronized to the internal conversion clock, so the four clock cycle synchronization uncertainty is removed yielding throughput at $[1/64]f_{CLK}$ for the CS5012A, $[1/72]f_{CLK}$ for CS5014 and $[1/80]f_{CLK}$ for CS5016 where f_{CLK} is the CLKIN frequency (see Figure 5b and Table 1).

Sampling Mode	Conversion Time Min	Conversion Time Max	Throughput Time Min	Throughput Time Max
CS5012A				
Synchronous (Loopback)	49 t_{clk}	49 t_{clk}	64 t_{clk}	64 t_{clk}
Asynchronous -7	49 t_{clk}	53 t_{clk} + 235 ns	N/A	59 t_{clk} + 1.32 µs
Asynchronous -12,-24	49 t_{clk}	53 t_{clk} + 235 ns	N/A	59 t_{clk} + 2.25 µs
CS5014				
Synchronous (Loopback)	57 t_{clk}	57 t_{clk}	72 t_{clk}	72 t_{clk}
Asynchronous	57 t_{clk}	61 t_{clk} + 235 ns	N/A	67 t_{clk} + 2.25 µs
CS5016				
Synchronous (Loopback)	65 t_{clk}	65 t_{clk}	80 t_{clk}	80 t_{clk}
Asynchronous	65 t_{clk}	69 t_{clk} + 235 ns	N/A	75 t_{clk} + 2.25 µs

Table 1. Conversion and Throughput Times (t_{clk} = Master Clock Period)

Also, the CS5012A/14/16's internal RC oscillator exhibits jitter (typically ± 0.05% of its period), which is high compared to crystal oscillators. If the CS5012A/14/16 is configured for synchronous sampling while operating from its internal oscillator, this jitter will directly affect sampling purity. The user can obtain best sampling purity while synchronously sampling by using an external crystal-based clock.

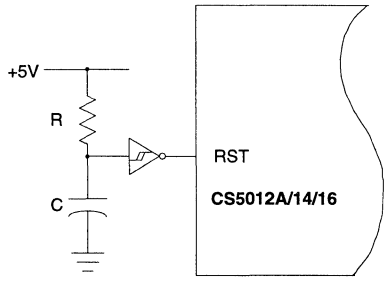


Figure 6. Power-on Reset Circuit

Reset

Upon power up, the CS5012A/14/16 must be reset to guarantee a consistent starting condition and initially calibrate the devices. Due to the CS5012A/14/16's low power dissipation and low temperature drift, no warm-up time is required before reset to accommodate any self-heating effects. However, the voltage reference input should have stabilized to within 5%, 1% or 0.25% of its final value, for the CS5012A/14/16 respectively, before RST falls to guarantee an accurate calibration. Later, the CS5012A/14/16 may be reset at any time to initiate a single full calibration. Reset overrides all other functions. If reset, the CS5012A/14/16 will clear and initiate a new calibration cycle mid-conversion or mid-calibration.

Resets can be initiated in hardware or software. The simplest method of resetting the CS5012A/14/16 involves strobing the RST pin high for at least 100 ns. When RST is brought high all internal logic clears. When it returns low, a full calibration begins which takes 58,280 CLKIN cycles for the CS5012A (approximately 9.1 ms with a 6.4 MHz clock) and 1,441,020 CLKIN cycles for the CS5016, CS5014 and CS5012 (approximately 360 ms with a 4 MHz CLKIN). A simple power-on reset circuit can be built using a resistor and capacitor, and a Schmitt-trigger inverter to prevent oscillation (see Figure 6). The CS5012A/14/16 can also be reset in software when under microprocessor control. The CS5012A/14/16 will reset whenever $\overline{CS}$, A0, and $\overline{HOLD}$ are taken low simultaneously. See the *Microprocessor Interface* section (below) to eliminate the possibility of inadvertent software reset. The $\overline{EOC}$ output remains high throughout the calibration operation and will fall upon its completion. It can thus be used to generate an interrupt indicating the CS5012A/14/16 is ready for operation. While calibrating, the $\overline{HOLD}$ input is ignored until $\overline{EOC}$ falls. After $\overline{EOC}$ falls, six CLKIN cycles plus 2.25 µs (1.32 µs for the CS5012A -7 version only) must be allowed for signal acquisition before $\overline{HOLD}$ is activated. Under microprocessor-independent operation ($\overline{CS}$, $\overline{RD}$ low; A0 high) the CS5014's and CS5016's $\overline{EOC}$ output will not fall at the completion of the calibration cycle, but $\overline{EOT}$ will fall 15 CLKIN cycles later.

Initiating Calibration

All modes of calibration can be controlled in hardware or software. Accuracy can thereby be insured at any time or temperature throughout operating life. After initial calibration at power-up, the CS5012A/14/16's charge-redistribution design yields better temperature drift and more graceful aging than resistor-based technologies, so calibration is normally only required once, after power-up.

The first mode of calibration, reset, results in a single full calibration cycle. The second type of calibration, "burst" cal, allows control of partial calibration cycles. *Due to an unforeseen condidtion inside the part, asynchronous termination of calibration may result in a sub-optimal result. Burst cal should not be used.*

The reset calibration always works perfectly, and should be used instead of burst mode. The CS5012's and CS5012A/14/16's very low drift over temperature means that, under most circumstances, calibration will only need to be performed at power-up, using reset.

The CS5012A/14/16 feature a background calibration mode called "interleave." Interleave appends a single calibration experiment to each conversion cycle and thus requires no dead time for calibration. The CS5012A/14/16 gathers data between conversions and will adjust its transfer function once it completes the entire sequence of experiments (one calibration cycle per 2,014 conversions in the CS5012A and one calibration per 72,051 conversions in the CS5012, CS5014 and CS5016). Initiated by bringing both the $\overline{\text{INTRLV}}$ input and $\overline{\text{CS}}$ low (or hard-wiring $\overline{\text{INTRLV}}$ low), interleave extends the CS5012A/14/16's effective conversion time by 20 CLKIN cycles. Other than reduced throughput, interleave is totally transparent to the user. Interleave calibration should not be used intermittently.

The fact that the CS5012A/14/16 offer several calibration modes is not to imply that the devices need to be recalibrated often. The devices are very stable in the presence of large temperature changes. Tests have indicated that after using a single reset calibration at 25 °C most devices exhibit very little change in offset or gain when exposed to temperatures from -55 to +125 °C. The data indicated 30 ppm as the typical worst case total change in offset or gain over this temperature range. Differential linearity remained virtually unchanged. System error sources outside of the A/D converter, whether due to changes in temperature or to long-term aging, will generally dominate total system error.

Microprocessor Interface

The CS5012A/14/16 feature an intelligent microprocessor interface which offers detailed status information and allows software control of the self-calibration functions. Output data is available in either 8-bit or 16-bit formats for easy interfacing to industry-standard microprocessors.

Strobing both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low enables the CS5012A/14/16's 3-state output buffers with either output data or status information depending on the status of A0. An address bit can be connected to A0 as shown in Figure 4b thereby memory mapping the status register and output data. Conversion status can be polled in software by reading the status register ($\overline{\text{CS}}$ and $\overline{\text{RD}}$ strobed low with A0 low), and masking status bits S0-S5 and S7 (by logically AND'ing the status word with 01000000) to determine the value of S6. Similarly, the software routine can determine calibration status using other status bits (see Table 2). *Care must be taken not to read the status register (A0 low) while $\overline{\text{HOLD}}$ is low, or a software reset will result* (see *Reset* above).

Alternatively, the End-of-Convert ($\overline{\text{EOC}}$) output can be used to generate an interrupt or drive a DMA controller to dump the output directly into memory after each conversion. The $\overline{\text{EOC}}$ pin falls as each conversion cycle is completed and data is valid at the output. It returns high within four CLKIN cycles of the first subsequent data read operation or after the start of a new conversion cycle.

PIN	STATUS BIT	STATUS	DEFINITION
D0	S0	END OF CONVERSION	Falls upon completion of a conversion, and returns high on the first subsequent read.
D1	S1	RESERVED	Reserved for factory use.
D2	S2	LOW BYTE/HIGH BYTE	When data is to be read in an 8-bit format (BW=0), indicates which byte will appear at the output next.
D3	S3	END OF TRACK	When low, indicates the input has been acquired to the devices specified accuracy.
D4	S4	RESERVED	Reserved for factory use.
D5	S5	TRACKING	High when the device is tracking the input.
D6	S6	CONVERTING	High when the device is converting the held input.
D7	S7	CALIBRATING	High when the device is calibrating.

Table 2. Status Pin Definitions

To interface with a 16-bit data bus, the BW input to the CS5012A/14/16 should be held high and all data bits (12, 14 and 16 for the CS5012A, CS5014 and CS5016 respectively) read in parallel on pins D4-D15 (CS5012A), D2-D15 (CS5014), or D0-D15 (CS5016). With an 8-bit bus, the converter's result must be read in two portions. In this instance, BW should be held low and the 8 MSB's obtained on the first read cycle following a conversion. The second read cycle will yield the remaining LSB's (4, 6 or 8 for the CS5012A/14/16 respectively) with 4, 2 or 0 trailing zeros. Both bytes appear on pins D0-D7. The upper/lower bytes of the same data will continue to toggle on subsequent reads until the next conversion finishes. Status bit S2 indicates which byte will appear on the next data read operation.

The CS5012A/14/16 internally buffer their output data, so data can be read while the devices are tracking or converting the next sample. Therefore, retrieving the converters' digital output requires no reduction in ADC throughput. Enabling the 3-state outputs while the CS5012A/14/16 is converting will not introduce conversion errors. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

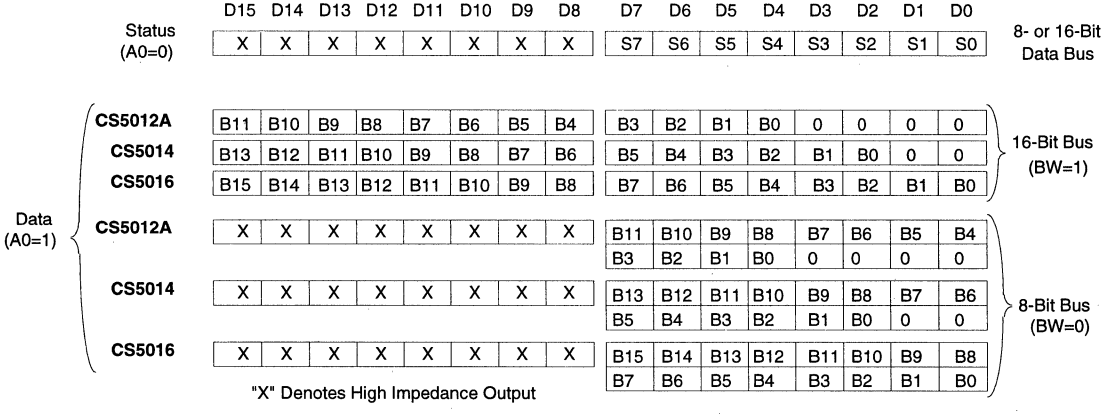


Figure 7. CS5012A/14/16 Data Format

Microprocessor Independent Operation

The CS5012A/14/16 can be operated in a stand-alone mode independent of intelligent control. In this mode, $\overline{CS}$ and $\overline{RD}$ are hard-wired low. This permanently enables the 3-state output buffers and allows transparent latch inputs (CAL and $\overline{INTRLV}$) to be active. A free-running condition is established when BW is tied high, CAL is tied low, and $\overline{HOLD}$ is continually strobed low or tied to $\overline{EOT}$. The CS5012A/14/16's $\overline{EOC}$ output can be used to externally latch the output data if desired. With $\overline{CS}$ and $\overline{RD}$ hard-wired low, $\overline{EOC}$ will strobe low for four CLKIN cycles after each conversion. Data will be unstable up to 100 ns after $\overline{EOC}$ falls, so it should be latched on the rising edge of $\overline{EOC}$.

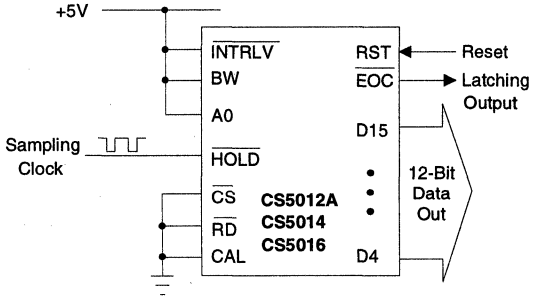


Figure 8. Microprocessor-Independent Connections

Serial Output

All successive-approximation A/D converters derive their digital output serially starting with the MSB. The CS5012A/14/16 present each bit to the SDATA pin four CLKIN cycles after it is derived and can be latched using the serial clock output, SCLK. Just subsequent to each bit decision SCLK will fall and return high once the bit information on SDATA has stabilized. Thus, the rising edge of the SCLK output should be used to clock the data from the CS5012A/14/16 (See Figure 9).

ANALOG CIRCUIT CONNECTIONS

Most popular successive-approximation A/D converters generate dynamic loads at their analog connections. The CS5012A/14/16 internally buffer all analog inputs (AIN, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

Reference Considerations

An application note titled "*Voltage References for the CS501X Series of A/D Converters*" is available for the CS5012A/14/16. In addition to working through a reference circuit design example, it offers several built-and-tested reference circuits.

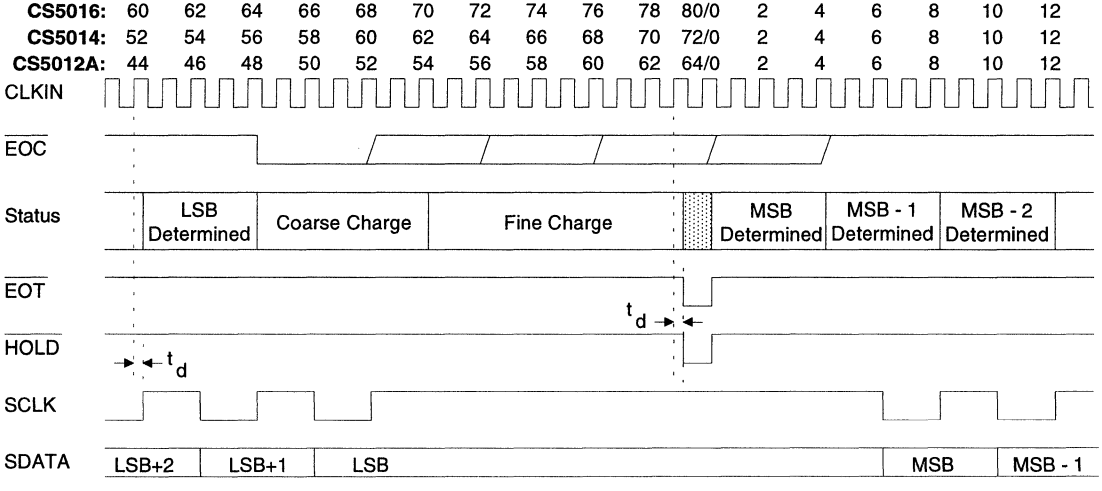
During conversion, each capacitor of the calibrated capacitor array is switched between VREF and AGND in a manner determined by the successive-approximation algorithm. The charging and discharging of the array results in a current load at the reference. The CS5012A/14/16 include an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to pre-charge the array thereby providing the bulk of the necessary charge. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer.

The external reference circuitry need only provide the residual charge required to fully charge the array after pre-charging from the buffer. This creates an ac current load as the CS5012A/14/16 sequence through conversions. The reference circuitry must have a low enough output impedance to drive the requisite current without changing its output voltage significantly. As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Therefore, the external reference must not exhibit significant

peaking in its output impedance characteristic at signal frequencies or their harmonics.

A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum, while almost all precision references exhibit extremely low output impedance at dc.

The magnitude of the current load on the external reference circuitry will scale to the CLKIN frequency. At full speed, the reference must supply a maximum load current of 10 µA peak-to-peak (1 µA typical). For the CS5012A an output impedance of 15 Ω will therefore yield a maximum error of 150 mV. With a 2.5V reference and LSB size of 600 mV, this would insure better than 1/4 LSB accuracy. A 1 µF capacitor exhibits an impedance of less than 15 Ω at frequencies greater than 10 kHz. Similarly, for the CS5014 with a 4.5V reference (275µV/LSB), better than 1/4 LSB accuracy can be insured with an output impedance of 4Ω or less (maximum error of 40 µV). A 2.2 µF capacitor exhibits an impedance of less than 4Ω at frequencies greater than 5kHz. For the CS5016 with a 4.5V reference (69µV/LSB), better than 1/4 LSB accuracy can be insured with an output impedance of less than 2Ω (maximum error of 20 µV). A 20 µF capacitor exhibits an impedance of less than 2Ω at frequencies greater than 16 kHz. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.



Notes: 1. Synchronous (loopback) mode is illustrated. After $\overline{EOC}$ falls the converter goes into coarse charge mode for 6 CLKIN cycles, then to fine charge mode for 9 cycles, then $\overline{EOT}$ falls. In loopback mode, $\overline{EOT}$ trips $\overline{HOLD}$ which captures the analog sample. Conversion begins on the next rising edge of CLKIN. If operated asynchronously, $\overline{EOT}$ will remain low until after $\overline{HOLD}$ is taken low. When $\overline{HOLD}$ occurs the analog sample is captured immediately, but conversion may not begin until four CLKIN cycles later. $\overline{EOT}$ will return high when conversion begins.

2. Timing delay t_d (relative to CLKIN) can vary between 135 ns to 235 ns over the military temperature range and over ± 10% supply variation

3. $\overline{EOC}$ returns high in 4 CLKIN cycles if A0 = 1 and $\overline{CS}$ = $\overline{RD}$ = 0 (Microprocessor Independent Mode); within 4 CLKIN cycles after a data read (Microprocessor Mode); or 4 CLKIN cycles after $\overline{HOLD}$ = 0 is recognized on a rising edge of CLKIN/4.

Figure 9. Serial Output Timing

Peaking in the reference's output impedance can occur because of capacitive loading at its output. Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors (Figure 10). The equation in Figure 10 can be used to help calculate the optimum value of R for a particular reference. The term "f_{peak}" is the frequency of the peak in the output impedance of the reference before the resistor is added.

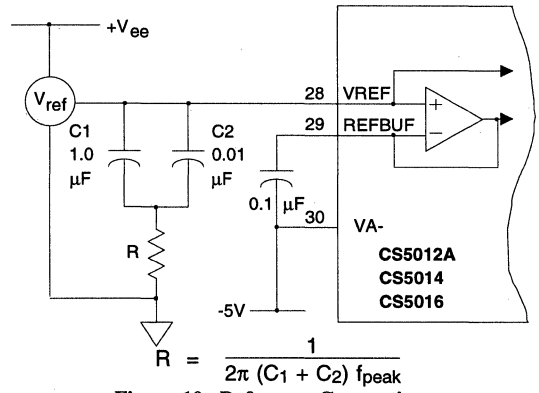


Figure 10. Reference Connections

The CS5012A/14/16 can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is between 2.5 and 4.5 V for the CS5012A and 4.5 V for the CS5014/16. The CS5012A/14/16 can actually accept reference voltages up to the positive analog supply. However, the buffer's offset may increase as the reference voltage approaches VA+ thereby increasing external drive requirements at VREF. A 4.5V reference is the maximum reference voltage recommended. This allows 0.5V headroom for the internal reference buffer. Also, the buffer enlists the aid of an external 0.1 µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. For more information on references, consult the application note: Voltage References for the CS501X Series of A/D Converters. For an example of using the CS5012A/14/16 with a 5 volt reference, see the application note: A Collection of Application Hints for the CS501X Series of A/D Converters.

Analog Input Connection

The analog input terminal functions similarly to the VREF input after each conversion when switching into the track mode. During the first six CLKIN cycles in the track mode, the buffered version of the analog input is used for pre-charging the capacitor array. An additional period is required for fine-charging directly from AIN to

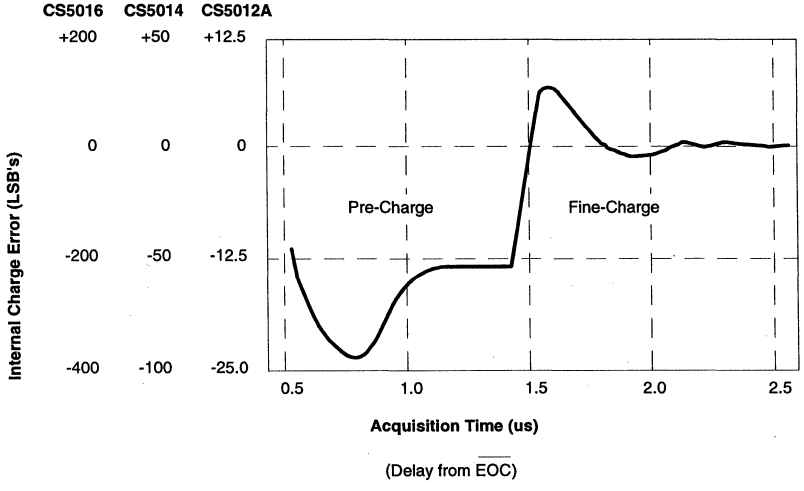


Figure 11. Internal Acquisition Time

obtain the specified accuracy. Figure 11 illustrates this operation. During pre-charge the charge on the capacitor array first settles to the buffered version of the analog input. This voltage is offset from the actual input voltage. During fine-charge, the charge then settles to the accurate unbuffered version.

The acquisition time of the CS5012A/14/16 depends on the CLKIN frequency. This is due to a fixed pre-charge period. For instance, operating the CS5012A -12, CS5014 -14 or CS5016 -16 version with an external 4 MHz CLKIN results in a 3.75 µs acquisition time: 1.5 µs for pre-charging (6 clock cycles) and 2.25 µs for fine-charging. Fine-charge settling is specified as a maximum of 2.25 µs for an analog source impedance of less than 200 Ω. (For the CS5012A -7 version it is specified as 1.32 µs.) In addition, the comparator requires a source impedance of less than 400 Ω around 2 MHz for stability, which is met by practically all bipolar op amps. Large dc source impedances can be accommodated by adding capacitance from AIN to ground (typically 200 pF) to decrease source impedance at high frequencies. However, high dc source resistances will increase the input's RC time constant and extend the necessary acquisition time. For more information on input applications, consult the application note: *Input Buffer Amplifiers for the CS501X Family of A/D Converters.*

During the first six clock cycles following a conversion (pre-charge) in unipolar mode, the CS5012A is capable of slewing at 20V/µs and the CS5014/16 can slew at 5V/µs. In bipolar mode, only half the capacitor array is connected to the analog input so the CS5012A can slew at 40V/µs, and the CS5014/16 can slew at 10V/µs. After the first six CLKIN cycles, the CS5012A will slew at 1.25V/µs in unipolar mode and 3.0V/µs in bipolar mode, and the CS5014/16 will slew at 0.25V/µs in unipolar mode and 0.5V/µs in bipolar mode. Acquisition of fast slewing signals (step functions) can be hastened if the step occurs during or immediately following the conversion cycle. For instance, channel selection in multiplexed applications should occur while the CS5012A/14/16 is converting (see Figure 12). Multiplexer settling is thereby removed from the overall throughput equation, and the CS5012A/14/16 can convert at full speed.

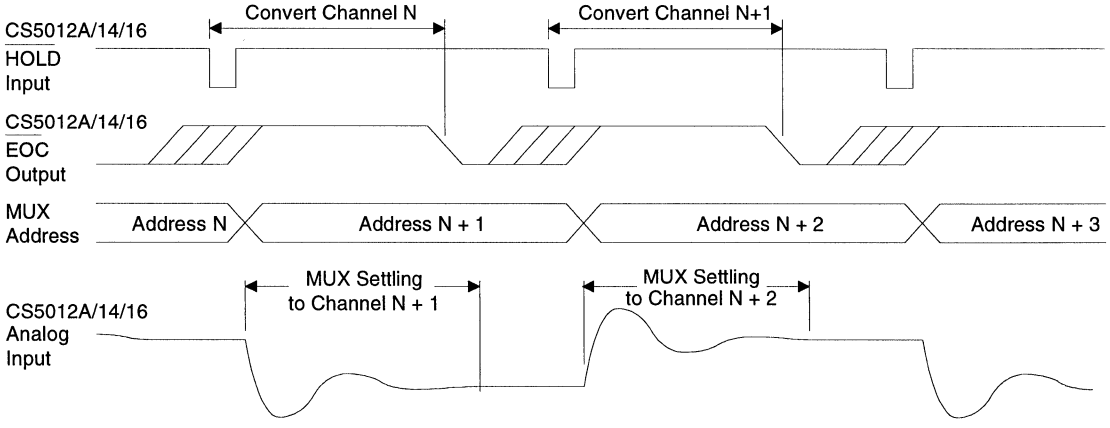


Figure 12. Pipelined MUX Input Channels

Analog Input Range/Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/$\overline{UP}$ low), the first code transition occurs 0.5 LSB above AGND, and the final code transition occurs 1.5 LSB's below VREF. Coding is in straight binary format. In the bipolar configuration (BP/$\overline{UP}$ high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSB's below +VREF. Coding is in an offset-binary format. Positive full scale gives a digital output of all ones, and negative full scale gives a digital output of all zeros.

The BP/$\overline{UP}$ mode pin may be switched after calibration without having to recalibrate the converter. However, the BP/$\overline{UP}$ mode should be changed during the previous conversion cycle, that is, between $\overline{HOLD}$ falling and $\overline{EOC}$ falling. If BP/$\overline{UP}$ is changed at any other time, one dummy conversion cycle must be allowed for proper acquisition of the input.

Grounding and Power Supply Decoupling

The CS5012A/14/16 use the analog ground connection, AGND, only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both the analog input and reference voltage should be referred to the AGND pin, which should be used as the entire system's analog ground reference point.

The digital and analog supplies to the CS5012A/14/16 are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1 µF ceramic capacitors. If significant low-frequency noise is present on the supplies, 1 µF tantalum capacitors are recommended in parallel with the 0.1 µF capacitors.

The positive digital power supply of the CS5012A/14/16 must never exceed the positive analog supply by more than a diode drop or the device could experience permanent damage. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagram in Figure 36 shows a decoupling scheme which allows the CS5012A/14/16 to be powered from a single set of ± 5V rails.

As with any high-precision A/D converter, the CS5012A/14/16 require careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the device. The CDB5012/14/16 evaluation board is available for the CS5012A/14/16, which avoids the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CS5012A/14/16, and can be quickly reconfigured to simulate any combination of sampling, calibration, CLKIN, and analog input range conditions.

Power Supply Rejection

The CS5012A/14/16's power supply rejection performance is enhanced by the on-chip self-calibration and an "auto-zero" process. Drifts in power supply voltages at frequencies less than the calibration rate have negligible effect on the CS5012A/14/16's accuracy. This is because the CS5012A/14/16 adjust their offset to within a small fraction of an LSB during calibration. Above the calibration frequency the excellent power supply rejection of the internal amplifiers is augmented by an auto-zero process. Any offsets are stored on the capacitor array and are effectively subtracted once conversion is initiated. Figure 13 shows power supply rejection of the CS5012A/14/16 in the bipolar mode with the analog input grounded and a 300 mVp-p ripple applied to each supply. Power supply rejection improves by 6 dB in the unipolar mode.

The plot in Figure 13 shows worst-case rejection for all combinations of conversion rates and input conditions in the bipolar mode.

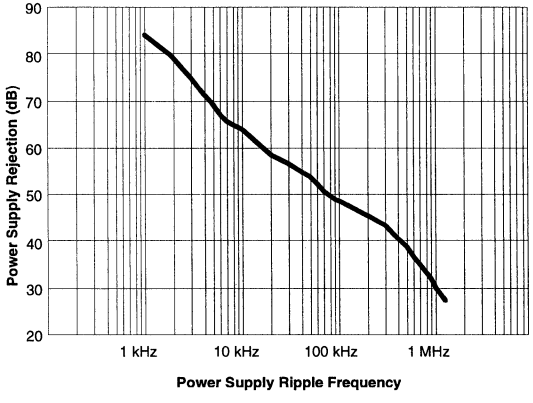


Figure 13. Power Supply Rejection

CS5012A/14/16 PERFORMANCE

Differential Nonlinearity

One source of nonlinearity in A/D converters is bit weight errors. These errors arise from the deviation of bits from their ideal binary-weighted ratios, and lead to nonideal widths for each code. If DNL errors are large, and code widths shrink to zero, it is possible for one or more codes to be entirely missing. The CS5012A/14/16 calibrate all bits in the capacitor array to a small fraction of an LSB resulting in nearly ideal DNL. Histogram plots of typical DNL of the CS5012A/14/16 can be seen in Figures 14, 16, 17. Figure 15 illustrates the DNL of the CS5012 for comparison with the CS5012A (Figure 14).

A histogram test is a statistical method of deriving an A/D converter's differential nonlinearity. A ramp is input to the A/D and a large number of samples are taken to insure a high confidence level in the test's result. The number of occurrences for each code is monitored and stored. A perfect A/D converter would have all codes of equal size and therefore equal numbers of occurrences. In the histogram test a code with the average number of occurrences will be considered ideal (DNL = 0). A code with more or less occurrences than average will appear as a DNL of greater or less than zero LSB. A missing code has zero occurrences, and will appear as a DNL of -1 LSB.

Integral Nonlinearity

Integral Nonlinearity (INL; also termed Relative Accuracy or just Nonlinearity) is defined as the deviation of the transfer function from an ideal straight line. Bows in the transfer curve generate harmonic distortion. The worst-case condition of bit-weight errors (DNL) has traditionally also defined the point of maximum INL.

Bit-weight errors have a drastic effect on a converter's ac performance. They can be analyzed as step functions superimposed on the input signal.

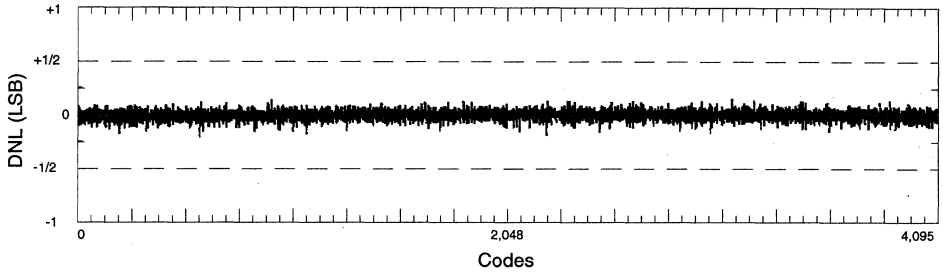


Figure 14. CS5012A Differential Nonlinearity Plot

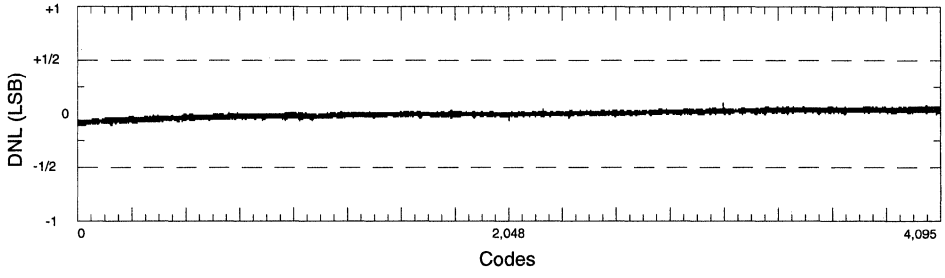


Figure 15. CS5012 Differential Nonlinearity Plot

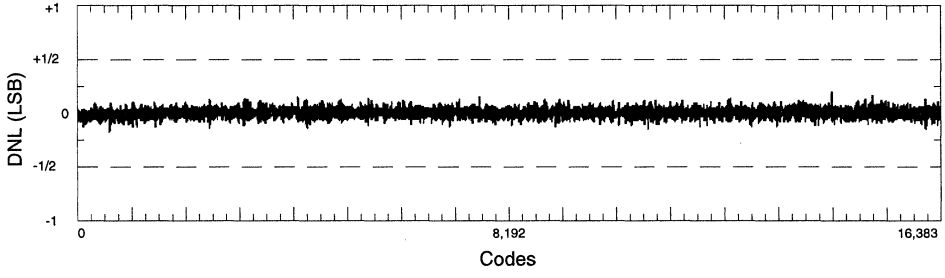


Figure 16. CS5014 Differential Nonlinearity Plot

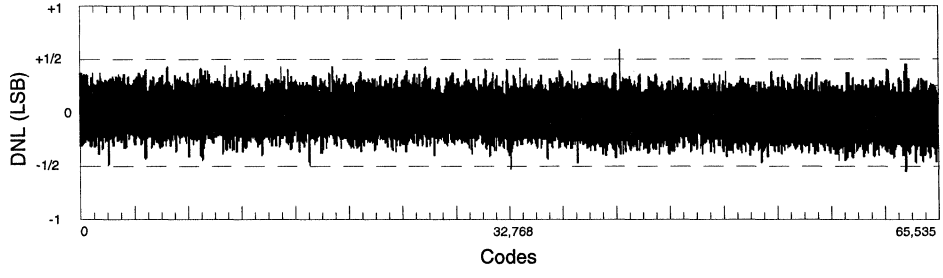


Figure 17. CS5016 Differential Nonlinearity Plot

Since bits (and their errors) switch in and out throughout the transfer curve, their effect is signal dependent. That is, harmonic and intermodulation distortion, as well as noise, can vary with different input conditions. Designing a system around characterization data is risky since transfer curves can differ drastically unit-to-unit and lot-to-lot.

The CS5012A/14/16 achieves repeatable signal-to-noise and harmonic distortion performance using an on-chip self-calibration scheme. The CS5012A calibrates its bit weight errors to a small fraction of an LSB at 12-bits yielding peak distortion below the noise floor (see Figure 19). The CS5014 calibrates its bit weights to within ±1/16 LSB at 14-bits (±0.0004% FS) yielding peak distortion as low as -105 dB (see Figure 22). The CS5016 calibrates its bit weights to within ±1/4 LSB at 16-bits (±0.0004% FS) yielding peak distortion as low as -105 dB (see Figure 24). Unlike traditional ADC's, the linearity of the CS5012A/14/16 are not limited by bit-weight errors; their performance is therefore extremely repeatable and independent of input signal conditions.

Quantization Noise

The error due to quantization of the analog input ultimately dictates the accuracy of any A/D converter. The continuous analog input must be represented by one of a finite number of digital codes, so the best accuracy to which an analog input can be known from its digital code is ±1/2 LSB. Under circumstances commonly encountered in signal processing applications, this quantization error can be treated as a random variable. The magnitude of the error is limited to ±1/2 LSB, but any value within this range has equal probability of occurrence. Such a probability distribution leads to an error "signal" with an rms value of 1 LSB/$\sqrt{12}$. Using an rms signal value of FS/$\sqrt{8}$ (amplitude = FS/2), this relates to ideal 12, 14 and 16-bit signal-to-noise ratios of 74, 86 and 98 dB respectively.

Equally important is the spectral content of this error signal. It can be shown to be approximately white, with its energy spread uniformly over the band from dc to one-half the sampling rate. Advantage of this characteristic can be made by judicious use of filtering. If the signal is bandlimited, much of the quantization error can be filtered out, and improved system performance can be attained.

FFT Tests and Windowing

In the factory, the CS5012A/14/16 are tested using Fast Fourier Transform (FFT) techniques to analyze the converter's dynamic performance. A pure sinewave is applied to the CS5012A/14/16, and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins." Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and dc can only be due to quantization effects and errors in the CS5012A/14/16.

If sampling is not synchronized to the input sinewave, it is highly unlikely that the time record will contain an integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a window function prior to performing the FFT. The window function smoothly forces the endpoints of the time record to zero, thereby removing the discontinuities. The effect of the window in the frequency-domain is to convolute the spectrum of the window with that of the actual input.

Figure 18 shows an FFT computed from an ideal 12-bit sinewave. The quality of the window used for harmonic analysis is typically judged by its highest side-lobe level. The Blackman-Harris window used for testing the CS5014 and CS5016 has a maximum side-lobe level of -92 dB. Fig-

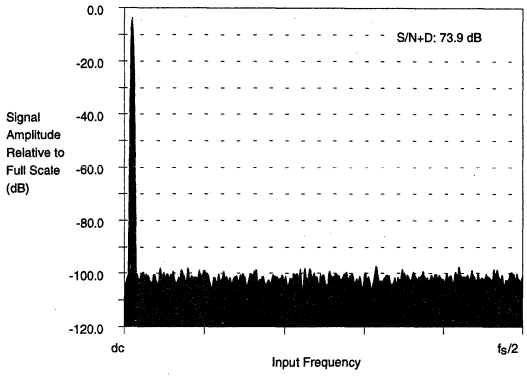


Figure 18. Plot of Ideal 12-bit ADC

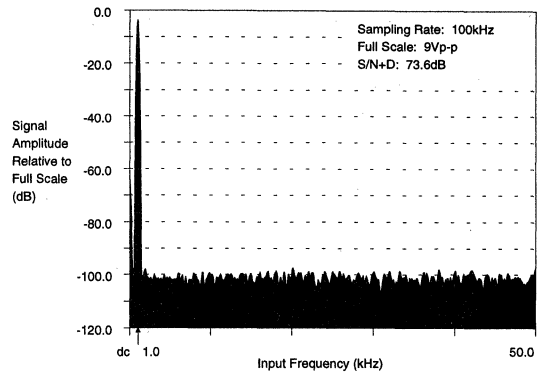


Figure 19. Plot of CS5012A with 1 kHz Full Scale Input

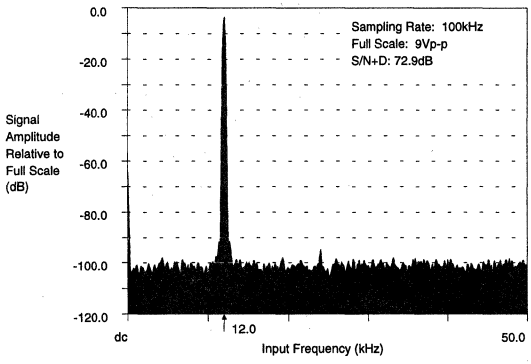


Figure 20. FFT Plot of CS5012A with 12 kHz Full-Scale Input

ures 21 and 23 show FFT plots computed from an ideal 14 and 16-bit sinewave multiplied by a Blackman-Harris window. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that quantization noise is white. All FFT plots in this data sheet were derived by averaging the FFT results from ten 1024 point time records. This filters the spectral variability that can arise from capturing finite time records without disturbing the total energy outside the fundamental. All harmonics which exist above the noise floor and the -92 dB side-lobes from the Blackman-Harris window are therefore clearly visible in the plots. For more information on FFT's and windowing refer to: F.J. HARRIS, "On the use of windows for harmonic

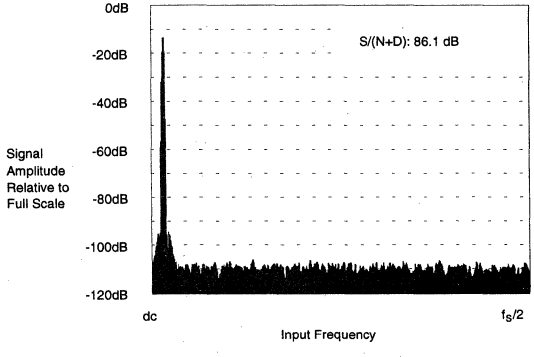


Figure 21. Plot of Ideal 14-bit ADC

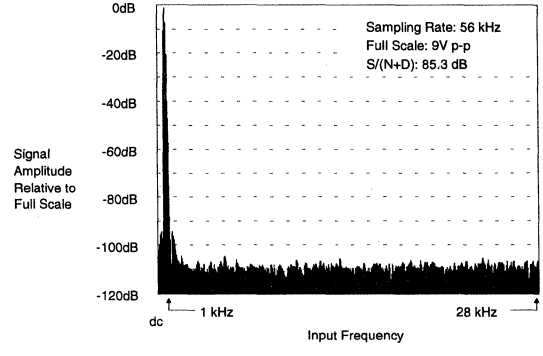


Figure 22. CS5014 FFT plot with 1 kHz Full Scale Input

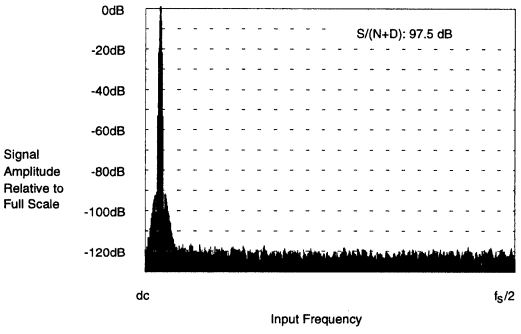


Figure 23. Plot of Ideal 16-bit ADC

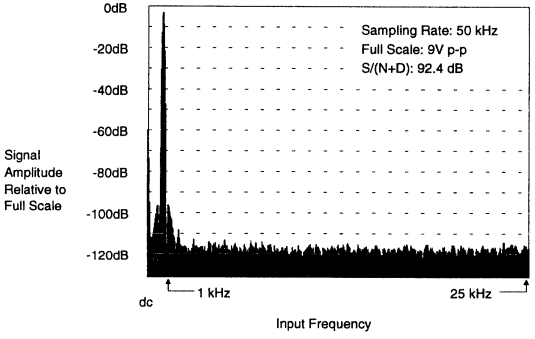


Figure 24. CS5016 FFT plot with 1 kHz Full Scale Input

analysis with the Discrete Fourier Transform", Proc. IEEE, Vol. 66, No. 1, Jan 1978, pp.51-83. This is available on request from Crystal Semiconductor.

Figures 19, 22, and 24 show the performance of the CS5012A/14/16 with 1kHz full scale inputs. Figure 20 shows CS5012A performance with 12kHz full scale inputs. Notice that the performance CS5012A/14/16 closely approaches that of the corresponding ideal ADC.

CS5012A High Frequency Performance

The CS5012A performs very well over a wide range of input frequencies as shown in Figure 25. The figure depicts the CS5012A-KP7 tested under four different conditions. The conditions include tests with the voltage reference set at 4.5 and at 2.5 volts with input signals at 0.5 dB down from full scale and 6.0 dB down from full scale. The sample rate is at 100 kHz for all cases. The plots indicate that the part performs very well even with input frequencies above the Nyquist rate. Best performance at the higher frequencies is achieved with a 2.5 volt reference.

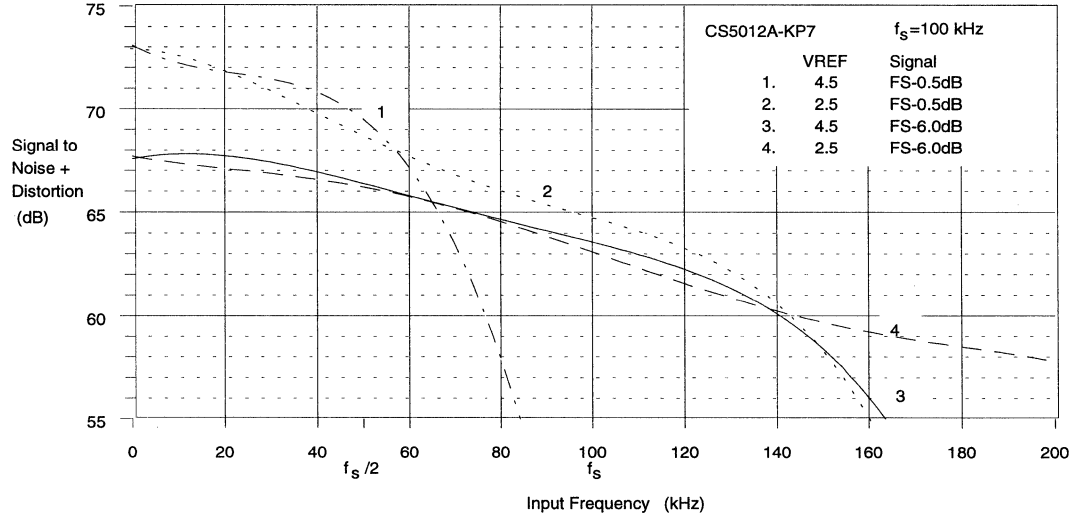


Figure 25. CS5012A High Frequency Input Performance

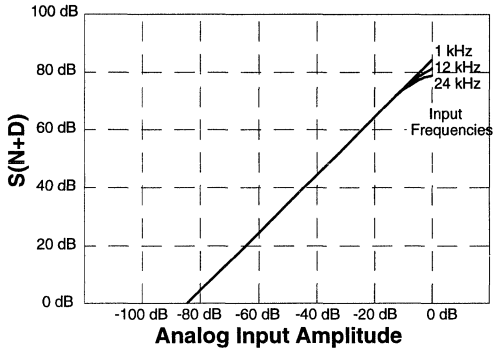


Figure 26. CS5014 S/(N+D) vs. Input Amplitude (9Vp-p Full-Scale Input)

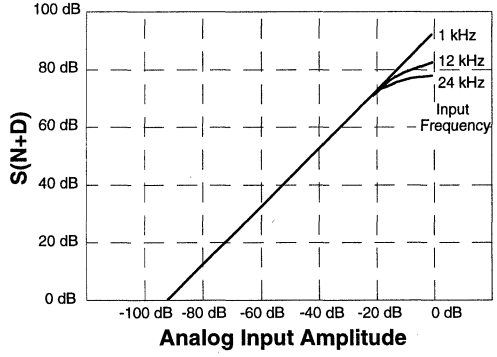


Figure 28. CS5016 S/(N+D) vs. Input Amplitude (9Vp-p Full-Scale Input)

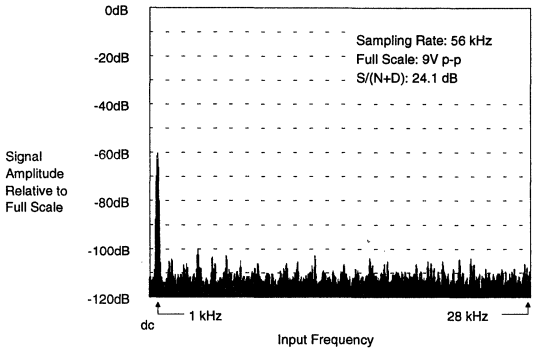


Figure 27. CS5014 FFT plot with 1 kHz -60 dB Input

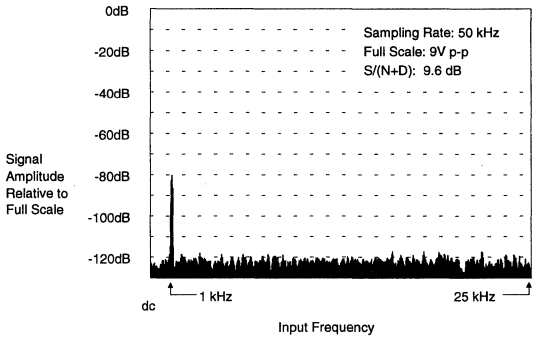


Figure 29. CS5016 FFT plot with 1 kHz -80 dB Input

Signal to Noise + Distortion vs Signal Level

As illustrated in Figures 26 - 29, the CS5014/16's on-chip self-calibration provides very accurate bit weights which yield no degradation in quantization noise with low-level input signals. In fact, quantization noise remains below the noise floor in the CS5016, which dictates the converter's signal-to-noise performance.

CS5016 Noise Considerations

All analog circuitry in the CS5016 is wideband in order to achieve fast conversions and high throughput. Wideband noise in the CS5016 integrates to 35 µV rms in unipolar mode (70 µV rms in bipolar mode). This is approximately 1/2 LSB rms with a 4.5V reference in both modes. Figure 30 shows a histogram plot of output code occurrences obtained from 5000 samples taken from a CS5016 in the bipolar mode. Hexadecimal code 80CD was arbitrarily selected and the analog input was set close to code center. With a noiseless converter, code 80CD would always appear. The histogram plot of the CS5016 has a "bell" shape with all codes other than 80CD due to internal noise.

In a sampled data system all information about the analog input applied to the sample/hold appears in the baseband from dc to one-half the sampling rate. This includes high-frequency components which alias into the baseband. Low-pass (anti-alias) filters

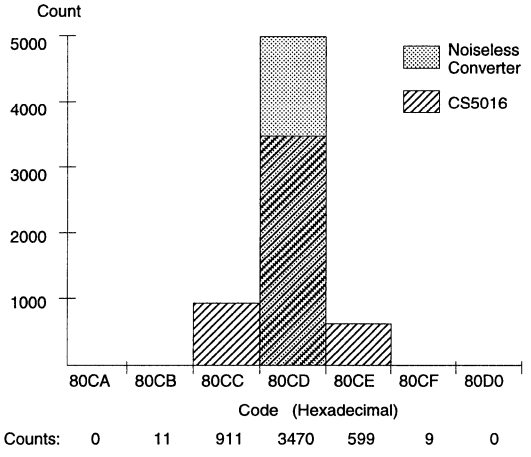


Figure 30. Histogram Plot of 5000 Conversion Inputs from the CS5016

are therefore used to remove frequency components in the input signal which are above one-half the sample rate. However, all wideband noise introduced by the CS5016 still aliases into the baseband. This "white" noise is evenly spread from dc to one-half the sampling rate and integrates to 35 µV rms in unipolar mode.

Noise can be reduced by sampling at higher than the desired word rate and averaging multiple samples for each word. Oversampling spreads the CS5016's noise over a wider band (for lower noise density), and averaging applies a low-pass response which filters noise above the desired signal bandwidth. In general, the CS5016's noise performance can be maximized in any application by always sampling at the maximum specified rate of 50 kHz (for lowest noise density) and digitally filtering to the desired signal bandwidth.

CS5014 and CS5016 Sampling Distortion

The ultimate limitation on the CS5014/16's linearity (and distortion) arises from nonideal sampling of the analog input voltage. The calibrated capacitor array used during conversions is also used to track and hold the analog input signal. The conversion is not performed on the analog input voltage per se, but is actually performed on the charge trapped on the capacitor array at the moment the $\overline{\text{HOLD}}$ command is given. The charge on the array is ideally related to the analog input voltage by $Q_{in} = -V_{in} \times C_{tot}$ as shown in Figure 2. Any deviation from this ideal relationship will result in conversion errors even if the conversion process proceeds flawlessly.

At dc, the DAC capacitor array's voltage coefficient dictates the converter's linearity. This variation in capacitance with respect to applied signal voltage yields a nonlinear relationship between charge Q_{in} and the analog input voltage V_{in} and places a bow or wave in the transfer function. This is the dominant source of distortion at low input frequencies (Figures 22 and 24).

The ideal relationship between Q_{in} and V_{in} can also be distorted at high signal frequencies due to nonlinearities in the internal MOS switches. Dynamic signals cause ac current to flow through the switches connecting the capacitor array to the analog input pin in the track mode. Nonlinear on-resistance in the switches causes a nonlinear voltage drop. This effect worsens with increased signal frequency as shown in Figures 26 and 28 since the magnitude of the steady state current increases. First noticeable at 1 kHz, this distortion assumes a linear relationship with input frequency. With signals 20 dB or more below full-scale, it no longer dominates the converter's overall S/(N+D) performance (Figures 31-34).

This distortion is strictly an ac sampling phenomenon. If significant energy exists at high frequencies, the effect can be eliminated using an external track-and-hold amplifier to allow the array's charge current to decay, thereby eliminating any voltage drop across the switches. Since the CS5014/16 has a second sampling function on-chip, the external track-and-hold can return to the track mode once the converter's $\overline{\text{HOLD}}$ input falls. It need only acquire the analog input by the time the entire conversion cycle finishes.

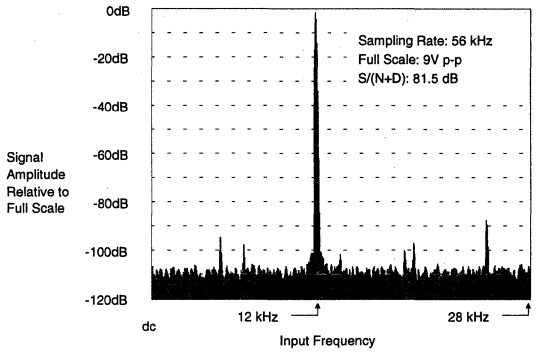


Figure 31. CS5014 FFT plot with 12 kHz Full Scale Input

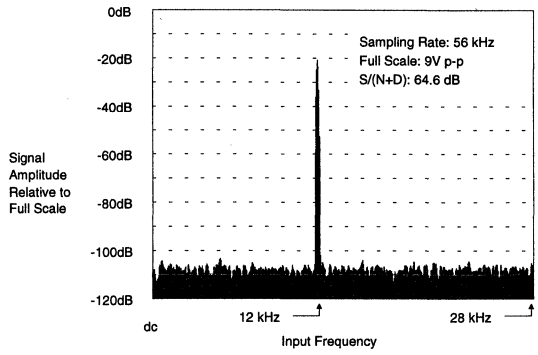


Figure 32. CS5014 FFT plot with 12 kHz -20 dB Input

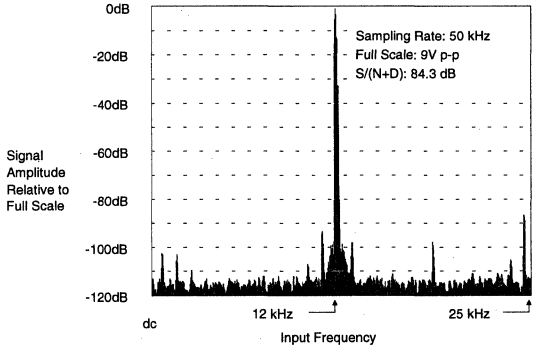


Figure 33. CS5016 FFT plot with 12 kHz Full Scale Input

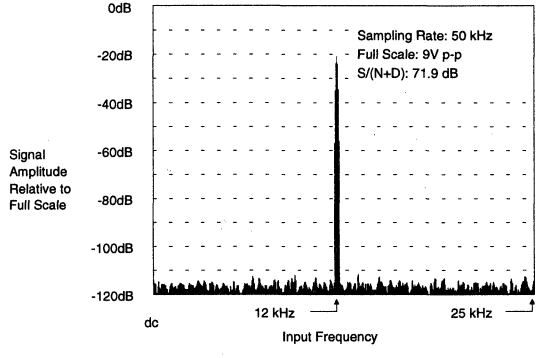


Figure 34. CS5016 FFT plot with 12 kHz -20 dB Input

Clock Feedthrough in the CS5014 and CS5016

Maintaining the integrity of analog signals in the presence of digital switching noise is a difficult problem. The CS5014/16 can be synchronized to the digital system using the CLKIN input to avoid conversion errors due to asynchronous interference. However, digital interference will still affect sampling purity due to coupling between the CS5014/16's analog input and master clock.

The effect of clock feedthrough depends on the sampling conditions. If the sampling signal at the $\overline{\text{HOLD}}$ input is synchronized to the master clock, clock feedthrough will appear as a dc offset at the CS5014/16's output. The offset could theoretically reach the peak coupling magnitude (Figure 35), but the probability of this occurring is small since the peaks are spikes of short duration.

Master Clock		Analog Input	Clock Feedthrough	
Int/Ext	Freq	Source Impedance	RMS	Peak-to-Peak
Internal	2MHz	50 Ω	15uV	70uV
External	2MHz	50 Ω	25uV	110uV
External	4MHz	50 Ω	40uV	150uV
External	4MHz	25 Ω	25uV	110uV
External	4MHz	200Ω	80uV	325uV

Figure 35. Examples of Measured Clock Feedthrough

If sampling is performed asynchronously with the master clock, clock feedthrough will appear as an ac error at the CS5014/16's output. With a fixed

sampling rate, a tone will appear as the clock frequency aliases into the baseband. The tone frequency can be calculated using the equation below and could be selectively filtered in software using DSP techniques.

$$f_{tone} = (N f_s - f_{clk})$$

where $N = f_{clk}/f_s$ rounded to the nearest integer

The magnitude of clock feedthrough depends on the master clock conditions and the source impedance applied to the analog input. When operating with the CS5014/16's internally generated clock, the CLKIN input is grounded and the dominant source of coupling is through the device's substrate. As shown in Figure 35, a typical CS5014/16 operating with their internal oscillator at 2 MHz and 50 Ω of analog input source impedance will exhibit only 15 µV rms of clock feedthrough. However, if a 2 MHz external clock is applied to CLKIN under the same conditions, feedthrough increases to 25 µV rms. Feedthrough also increases with clock frequency; a 4 MHz clock yields 40 µV rms.

Clock feedthrough can be reduced by limiting the source impedance applied at the analog input. As shown in Figure 35, reducing source impedance from 50 Ω to 25 Ω yields a 15 µV rms reduction in feedthrough. Therefore, when operating the CS5014/16 with high-frequency external master clocks, it is important to minimize source impedance applied to the CS5014/16's input.

Also, the overall effect of clock feedthrough can be minimized by maximizing the input range and LSB size. The reference voltage applied to VREF can be maximized, and the CS5014/16 can be operated in bipolar mode which inherently doubles the LSB size over the unipolar mode.

Differences between the CS5012A and the CS5012

The differences between the CS5012A and the CS5012 are tabulated in Table 3. The CS5012 is a short-cycled version of the CS5016 A/D converter and includes the same 18-bit calibration circuitry. This calibration circuitry sets the calibration resolution of the CS5012 at 1/64th of an LSB and achieves the near perfect differential linearity performance illustrated by the CS5012 DNL plot in Figure 15. The CS5012A calibration circuitry was modified to provide calibration to 15-bit resolution therefore achieving calibration to 1/8 of an LSB. This reduction in calibration resolution for the CS5012A reduces the time required to calibrate the device (see Table 3) and reduces the size of the total array capacitance. The reduced array capacitance improves the high frequency performance by allowing higher slew rate in the input circuitry.

Table 3 documents some other improvements included in the CS5012A. The burst mode calibration was made functional, although it should not be used. The device was also modified so the $\overline{EOC}$ signal goes low at the end of a reset calibration in either microprocessor or microprocessor-independent mode. The CS5012A was modified to maintain a throughput rate of 64 CLKIN cycles in loopback mode for all frequencies of CLKIN.

	CS5012A	CS5012
Calibration resolution	15 bits. Results in DNL calibration to 1/8 LSB at 12 bits.	18 bits. Results in DNL calibration to 1/64 LSB at 12 bits.
Calibration time reset: interleave: burst:	 58,280 CLKIN cycles 2,014 conversions fully functional	 1,441,020 CLKIN cycles 72,051 conversions not functional
End of calibration indicator	$\overline{EOC}$ falls in either microprocessor or microprocessor-independent mode at the completion of a RESET calibration cycle.	$\overline{EOC}$ falls at the completion of a RESET calibration cycle in microprocessor mode only. In microprocessor-independent mode $\overline{EOT}$ must be used. $\overline{EOT}$ falls 15 CLKIN cycles after completion of a RESET calibration.
Throughput rate in loopback mode	The device acquires and converts a sample in 64 CLKIN cycles for all CLKIN frequencies when in loopback.	The device acquires and converts in 64 CLKIN cycles for CLKIN=4MHz, but will require 68 CLKIN cycles at 100kHz throughput. This is due to excess delay on $\overline{EOT}$.
Input capacitance in fine-charge mode	103pF typical, unipolar mode 72pF typical, bipolar mode	275pF typical, unipolar mode 165pF typical, bipolar mode
Slew Rate Unipolar Coarse charge Fine charge Bipolar Coarse charge Fine charge	 20V/us 1.5V/us 40V/us 3.0V/us	 5V/us 0.25V/us 10V/us 0.5V/us

Table 3. Differences Between the CS5012A and CS5012

$\overline{HOLD}$	$\overline{CS}$	CAL	$\overline{INTRLV}$	$\overline{RD}$	A0	RST	Function
↓	X	X	X	X	*	0	Hold and Start Convert
X	0	1	X	X	*	0	Initiate Burst Calibration
1	0	0	X	X	*	0	Stop Burst Cal and Begin Track
X	0	X	0	X	*	0	Initiate Interleave Calibration
X	0	X	1	X	*	0	Terminate Interleave Cal
X	0	X	X	0	1	0	Read Output Data
1	0	X	X	0	0	0	Read Status Register
X	1	X	X	X	*	X	High Impedance Data Bus
X	X	X	X	1	*	X	High Impedance Data Bus
X	X	X	X	X	X	1	Reset
0	0	X	X	X	0	X	Reset

* The status of A0 is not critical to the operation specified. However, A0 should not be low with $\overline{CS}$ and $\overline{HOLD}$ low, or a software reset will result.

Table 4. CS5012A/14/16 Truth Table

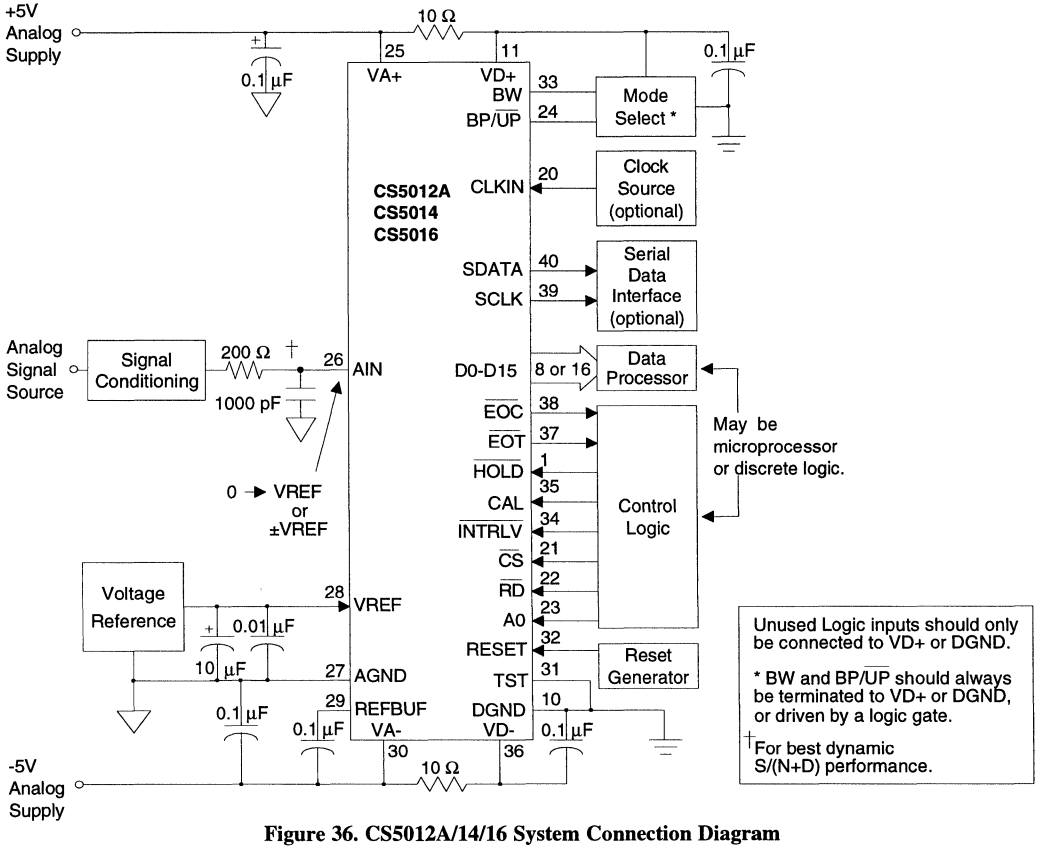
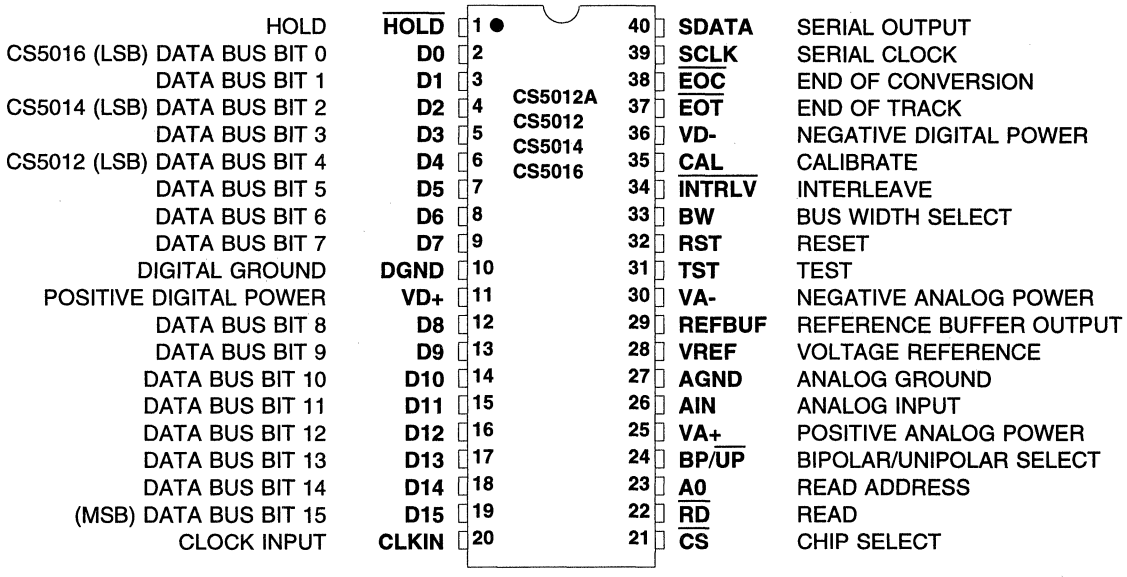
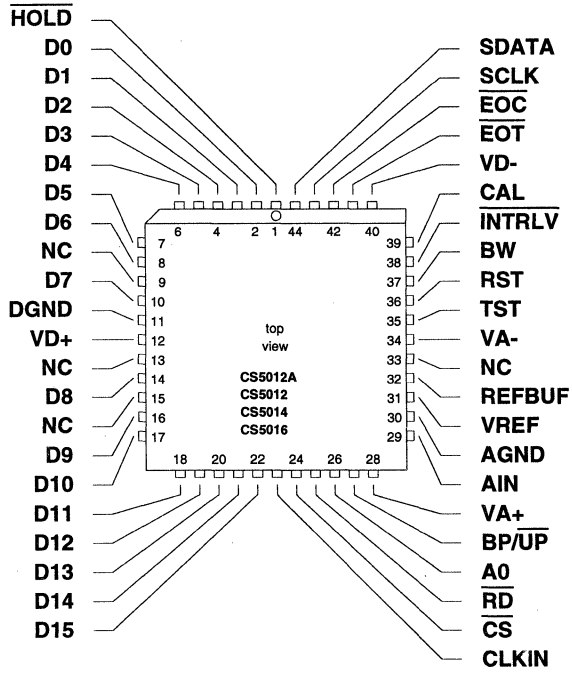


Figure 36. CS5012A/14/16 System Connection Diagram





NOTE: All pin references in this data sheet refer to the 40-pin DIP package numbering. Use this figure to determine pin numbers for 44-pin package.

PIN DESCRIPTIONS

Power Supply Connections

VD+ – Positive Digital Power, PIN 11.
Positive digital power supply. Nominally +5 volts.

VD- – Negative Digital Power, PIN 36.
Negative digital power supply. Nominally -5 volts.

DGND – Digital Ground, PIN 10.
Digital ground.

VA+ – Positive Analog Power, PIN 25.
Positive analog power supply. Nominally +5 volts.

VA- – Negative Analog Power, PIN 30.
Negative analog power supply. Nominally -5 volts.

AGND – Analog Ground, PIN 27.
Analog ground.

Oscillator

CLKIN – Clock Input, PIN 20.
All conversions and calibrations are timed from a master clock which can either be supplied by driving this pin with an external clock signal, or can be internally generated by tying this pin to DGND.

Digital Inputs

$\overline{\text{HOLD}}$ – Hold, PIN 1.
A falling transition on this pin sets the CS5012A/14/16 to the hold state and initiates a conversion. This input must remain low at least one CLKIN cycle plus 50 ns.

$\overline{\text{CS}}$ – Chip Select, PIN 21.
When high, the data bus outputs are held in a high impedance state and the input to CAL and $\overline{\text{INTRLV}}$ are ignored. A falling transition initiates or terminates burst or interleave calibration (depending on the status of CAL and $\overline{\text{INTRLV}}$) and a rising transition latches both the CAL and $\overline{\text{INTRLV}}$ inputs. If $\overline{\text{RD}}$ is low, the data bus is driven as indicated by BW and A0.

$\overline{\text{RD}}$ – Read, PIN 22.
When $\overline{\text{RD}}$ and $\overline{\text{CS}}$ are both low, data is driven onto the data bus. If either signal is high, the data bus outputs are held in a high impedance state. The data driven onto the bus is determined by BW and A0.

A0 – Read Address, PIN 23.

Determines whether data or status information is placed onto the data bus. When high during the read operation, converted data is placed onto the data bus; when low, the status register is driven onto the bus.

BP/$\overline{UP}$ – Bipolar/Unipolar Input Select, PIN 24.

When high, the device is configured with a bipolar transfer function ranging from -VREF to +VREF. Encoding is in an offset binary format, with the mid-scale code 100...0000 centered at AGND. When low, the device is configured for a unipolar transfer function from AGND to VREF. Unipolar encoding is in straight binary format. Once calibration has been performed, either bipolar or unipolar mode may be selected without the need to recalibrate.

RST – Reset, PIN 32.

When taken high for at least 100 ns, all internal digital logic is reset. Upon being taken low, a full calibration sequence is initiated.

BW – Bus Width Select, PIN 33.

When hard-wired high, all 12 data bits are driven onto the bus simultaneously during a data read cycle. When low, the bus is in a byte wide format. On the first read following a conversion, the eight MSB's are driven onto D0-D7. A second read cycle places the four LSB's with four trailing zeros on D0-D7. Subsequent reads will toggle the higher/lower order byte. Regardless of BW's status, a read cycle with A0 low yields the status information on D0-D7.

$\overline{INTRLV}$ – Interleave, PIN 34.

When latched low using $\overline{CS}$, the device goes into interleave calibration mode. A full calibration will complete every 2,014 conversions in the CS5012A, and every 72,051 conversions in the CS5014/16. The effective conversion time extends by 20 clock cycles.

CAL – Calibrate, PIN 35. (See Addendum appending this data sheet))

When latched high using $\overline{CS}$, burst calibration results. The device cannot perform conversions during the calibration period which will terminate only once CAL is latched low again. Calibration picks up where the previous calibration left off, and calibration cycles complete every 58,280 CLKIN cycles in the CS5012A, and every 1,441,020 CLKIN cycles in the CS5014/16 . If the device is converting when a calibration is signaled, it will wait until that conversion completes before beginning.

Analog Inputs

AIN – Analog Input, PIN 26.

Input range in the unipolar mode is zero volts to VREF. Input range in bipolar mode is -VREF to +VREF. The output impedance of buffer driving this input should be less than or equal to 200 Ω.

VREF – Voltage Reference, PIN 28.

The analog reference voltage which sets the analog input range. It represents positive full scale for both bipolar and unipolar operation, and its magnitude sets negative full scale in bipolar mode.

Digital Outputs

D0 through D15 – Data Bus Outputs, PINS 2 thru 9, 12 thru 19.

3-state output pins. Enabled by $\overline{CS}$ and $\overline{RD}$, they offer the converter's output in a format consistent with the state of BW if A0 is high. If A0 is low, bits D0-D7 offer status register data.

$\overline{EOT}$ – End Of Track, PIN 37.

If low, indicates that enough time has elapsed since the last conversion for the device to acquire the analog input signal.

$\overline{EOC}$ – End Of Conversion, PIN 38.

This output indicates the end of a conversion or calibration cycle. It is high during a conversion and will fall to a low state upon completion of the conversion cycle indicating valid data is available at the output. Returns high on the first subsequent read or the start of a new conversion cycle.

SDATA – Serial Output, PIN 40.

Presents each output data bit after it is determined by the successive approximation algorithm. Valid on the rising edge of SCLK, data appears MSB first, LSB last, and each bit remains valid until the next bit appears.

SCLK – Serial Clock Output, PIN 39.

Used to clock converted output data serially from the CS5012A/14/16. Serial data is stable on the rising edge of SCLK.

Analog Outputs

REFBUF – Reference Buffer Output, PIN 29.

Reference buffer output. A 0.1 µF ceramic capacitor must be tied between this pin and VA-.

Miscellaneous

TST – Test, PIN 31.

Allows access to the CS5012A/14/16's test functions which are reserved for factory use. Must be tied to DGND.

PARAMETER DEFINITIONS

Linearity Error

The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in % Full-Scale.

Differential Linearity

Minimum resolution for which no missing codes is guaranteed. Units in bits.

Full Scale Error

The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSB's.

Unipolar Offset

The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/UP low). Units in LSB's.

Bipolar Offset

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSB's.

Bipolar Negative Full-Scale Error

The deviation of the first code transition from the ideal when in bipolar mode (BP/$\overline{UP}$ high). The ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSB's.

Peak Harmonic or Spurious Noise (More accurately, Signal to Peak Harmonic or Spurious Noise)

The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Expressed in decibels.

Total Harmonic Distortion

The ratio of the rms sum of all harmonics to the rms value of the signal. Units in percent.

Signal-to-Noise Ratio

The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels.

Aperture Time

The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter

The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

NOTE: Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

CS5012A Ordering Guide

Model	Throughput	Conversion Time	Maximum DNL	Temp. Range	Package
CS5012A-KP12	63 kHz	12.25 µs	±1/2 LSB	0 to 70 °C	40-Pin Plastic DIP
CS5012A-KP7	100 kHz	7.20µs	±1/2 LSB	0 to 70 °C	40-Pin Plastic DIP
CS5012A-KL12	63 kHz	12.25 µs	±1/2 LSB	0 to 70 °C	44-Pin PLCC
CS5012A-KL7	100 kHz	7.20 µs	±1/2 LSB	0 to 70 °C	44-Pin PLCC
CS5012A-BP12	63 kHz	12.25 µs	±1/2 LSB	-40 to +85 °C	40-Pin Plastic DIP
CS5012A-BP7	100 kHz	7.20 µs	±1/2 LSB	-40 to +85 °C	40-Pin Plastic DIP
CS5012A-BL12	63 kHz	12.25 µs	±1/2 LSB	-40 to +85 °C	44-Pin PLCC
CS5012A-BL7	100 kHz	7.20 µs	±1/2 LSB	-40 to +85 °C	44-Pin PLCC
5962-8967901QA	63 kHz	12.25 µs	±1/2 LSB	-55 to +125 °C	40-Pin CerDIP
5962-8967901XA	63 kHz	12.25 µs	±1/2 LSB	-55 to +125 °C	44-Pin Ceramic LCC

The CS5012A is recommended for new designs. The following is a list of upgraded part numbers.

Discontinued Part Number	Equivalent Recommended Device.
CS5012-KP24	CS5012A-KP12
CS5012-KP12	CS5012A-KP12
CS5012-KP7	CS5012A-KP7
CS5012-KL24	CS5012A-KL12
CS5012-KL12	CS5012A-KL12
CS5012-KL7	CS5012A-KL7
CS5012-BD24	CS5012A-BP12
CS5012-BD12	CS5012A-BP12
CS5012-BD7	CS5012A-BP7
CS5012-BL24	CS5012A-BL12
CS5012-BL12	CS5012A-BL12
CS5012-BL7	CS5012A-BL7
CS5012-TD24B	5962-897901QA
CS5012-TD12B	5962-897901QA
CS5012-TE24B	5962-897901XA
CS5012-TE12B	5962-897901XA

CS5014 Ordering Guide

Model	Throughput	Conversion Time	Linearity	Temp. Range	Package
CS5014-KP28	28 kHz	28.50 µs	±0.5 LSB	0 to 70 °C	40-Pin Plastic DIP
CS5014-KP14	56 kHz	14.25 µs	±0.5 LSB	0 to 70 °C	40-Pin Plastic DIP
CS5014-KL28	28 kHz	28.50 µs	±0.5 LSB	0 to 70 °C	44-Pin PLCC
CS5014-KL14	56 kHz	14.25 µs	±0.5 LSB	0 to 70 °C	44-Pin PLCC
CS5014-BP28	28 kHz	28.50 µs	±0.5 LSB	-40 to +85 °C	40-Pin Plastic DIP
CS5014-BP14	56 kHz	14.25µs	±0.5 LSB	-40 to +85 °C	40-Pin Plastic DIP
CS5014-BL28	28 kHz	28.50 µs	±0.5 LSB	-40 to +85 °C	44-Pin PLCC
CS5014-BL14	56 kHz	14.25 µs	±0.5 LSB	-40 to +85 °C	44-Pin PLCC
CS5014-SD14	56 kHz	14.25 µs	±1.5 LSB	-55 to +125 °C	40-Pin CerDIP
CS5014-TD14	56 kHz	14.25 µs	±0.5 LSB	-55 to +125 °C	40-Pin CerDIP
CS5014-SE14	56 kHz	14.25 µs	±1.5 LSB	-55 to +125 °C	44-Pin Ceramic LCC
CS5014-TE14	56 kHz	14.25 µs	±0.5 LSB	-55 to +125 °C	44-Pin Ceramic LCC
5962-8967401QA	56 kHz	14.25 µs	±1.5 LSB	-55 to +125 °C	40-Pin CerDIP
5962-8967402QA	56 kHz	14.25 µs	±0.5 LSB	-55 to +125 °C	40-Pin CerDIP
5962-8967401XA	56 kHz	14.25 µs	±1.5 LSB	-55 to +125 °C	44-Pin Ceramic LCC
5962-8967402XA	56 kHz	14.25 µs	±0.5 LSB	-55 to +125 °C	44-Pin Ceramic LCC

The following is a list of upgraded part numbers.

Discontinued Part Number	Equivalent Recommended Device
CS5014-SD14B	5962-8967401QA
CS5014-TD14B	5962-8967402QA
CS5014-SE14B	5962-8967401XA
CS5014-TE14B	5962-8967402XA

CS5016 Ordering Guide

Model	Linearity	Signal to Noise Ratio	Conversion Time	Temp. Range	Package
CS5016-JP32	.0030%	87 dB	32.50 µs	0 to 70 °C	40-Pin Plastic DIP
CS5016-JP16	.0030%	87 dB	16.25 µs	0 to 70 °C	40-Pin Plastic DIP
CS5016-KP32	.0015%	90 dB	32.50 µs	0 to 70 °C	40-Pin Plastic DIP
CS5016-KP16	.0015%	90 dB	16.25 µs	0 to 70 °C	40-Pin Plastic DIP
CS5016-JL32	.0030%	87 dB	32.50 µs	0 to 70 °C	44-Pin PLCC
CS5016-JL16	.0030%	87 dB	16.25 µs	0 to 70 °C	44-Pin PLCC
CS5016-KL32	.0015%	90 dB	32.50 µs	0 to 70 °C	44-Pin PLCC
CS5016-KL16	.0015%	90 dB	16.25 µs	0 to 70 °C	44-Pin PLCC
CS5016-AP32	.0030%	87 dB	32.50 µs	-40 to +85 °C	40-Pin Plastic DIP
CS5016-AP16	.0030%	87 dB	16.25 µs	-40 to +85 °C	40-Pin Plastic DIP
CS5016-BP32	.0015%	90 dB	32.50 µs	-40 to +85 °C	40-Pin Plastic DIP
CS5016-BP16	.0015%	90 dB	16.25 µs	-40 to +85 °C	40-Pin Plastic DIP
CS5016-AL32	.0030%	87 dB	32.50 µs	-40 to +85 °C	44-Pin PLCC
CS5016-AL16	.0030%	87 dB	16.25 µs	-40 to +85 °C	44-Pin PLCC
CS5016-BL32	.0015%	90 dB	32.50 µs	-40 to +85 °C	44-Pin PLCC
CS5016-BL16	.0015%	90 dB	16.25 µs	-40 to +85 °C	44-Pin PLCC
CS5016-SD16	.0076%	87 dB	16.25 µs	-55 to +125 °C	40-Pin CerDIP
CS5016-TD16	.0015%	90 dB	16.25 µs	-55 to +125 °C	40-Pin CerDIP
CS5016-SE16	.0076%	87 dB	16.25 µs	-55 to +125 °C	44-Pin Ceramic LCC
CS5016-TE16	.0015%	90 dB	16.25 µs	-55 to +125 °C	44-Pin Ceramic LCC
5962-8967601QA	.0076%	87 dB	16.25 µs	-55 to +125 °C	40-Pin CerDIP
5962-8967602QA	.0015%	90 dB	16.25 µs	-55 to +125 °C	40-Pin CerDIP
5962-8967601XA	.0076%	87 dB	16.25 µs	-55 to +125 °C	44-Pin Ceramic LCC
5962-8967602XA	.0015%	90 dB	16.25 µs	-55 to +125 °C	44-Pin Ceramic LCC

The following is a list of upgraded part numbers.

Discontinued Part Number	Equivalent Recommended Device
CS5016-SD16B	5962-8967601QA
CS5016-TD16B	5962-8967602QA
CS5016-SE16B	5962-8967601XA
CS5016-TE16B	5962-8967602XA

Semiconductor Corporation

CDB5012 CDB5012A CDB5014 CDB5016

Evaluation Board for CS5012, CS5012A, CS5014, CS5016 ADC's

Features

- Compatible with CS5012, CS5012A, CS5014, CS5016
- PC/µP-Compatible Header Connection
  - 16-Bit Parallel Data
  - End-of-Conversion Output
  - CS, RD, and A0 Control Inputs
- DIP-Switch Selectable:
  - Unipolar/Bipolar Input Range
  - Burst & Interleave Calibration Modes
  - Continuous Conversion
- Adjustable Voltage Reference
- Serial Data and Clock BNC Connections
- Operation from Internally-Generated or Externally-Supplied Master Clock

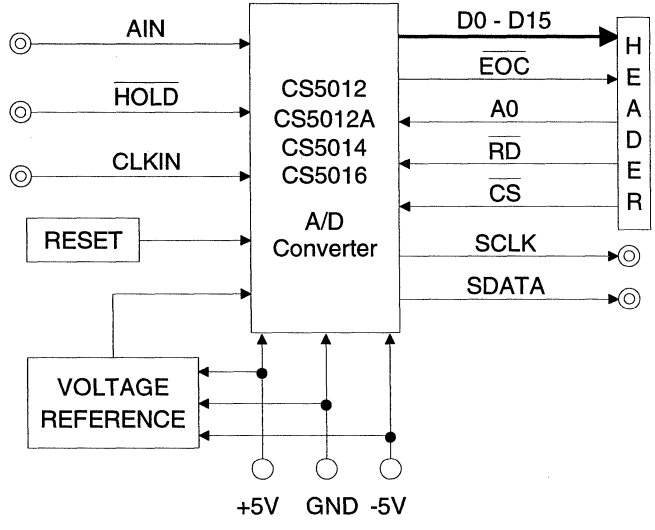
General Description

The CDB5012/4/6 is an evaluation board that eases the laboratory characterization of any of the CS5012, CS5012A, CS5014 and CS5016 A/D converters. The board can be easily reconfigured to simulate any combination of sampling, master clock, calibration, and input range conditions.

The converter's parallel output data are available at a 40 pin strip header allowing easy interfacing to PC's or microprocessor busses. Output data is also available in serial form at SCLK and SDATA coaxial BNC connectors.

Evaluation can also be performed over a wide range of input spans using the on-board reference circuitry. Furthermore, the CDB5012, CDB5012A, CDB5014, CDB5016 features DIP-switch selectable unipolar/bipolar input ranges and the interleave calibration mode. Calibration can be initiated at any time by momentarily depressing a reset pushbutton.

ORDERING INFORMATION: CDB5012, CDB5012A, CDB5014, CDB5016



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Analog Input

The analog input to the A/D converter is supplied through the BNC coaxial connector labeled AIN. Analog input polarity is controlled by the first position switch on the DIP-switch, SW-1. If it is on, the input is unipolar ranging from GND to VREF. If the switch is off, the input range is bipolar with the magnitude of the reference voltage defining both zero- and full-scale (±VREF).

The A/D converter's internal analog input buffer requires a source impedance of less than 400 Ω at 1MHz for stability. Acquisition and throughput are specified assuming a dc source impedance of less than 200 Ω. Infinitely large dc source impedances can be accommodated by adding capacitance (typically 1000pF) from the analog input to ground. However, high dc source resistances degrade acquisition time and consequently throughput.

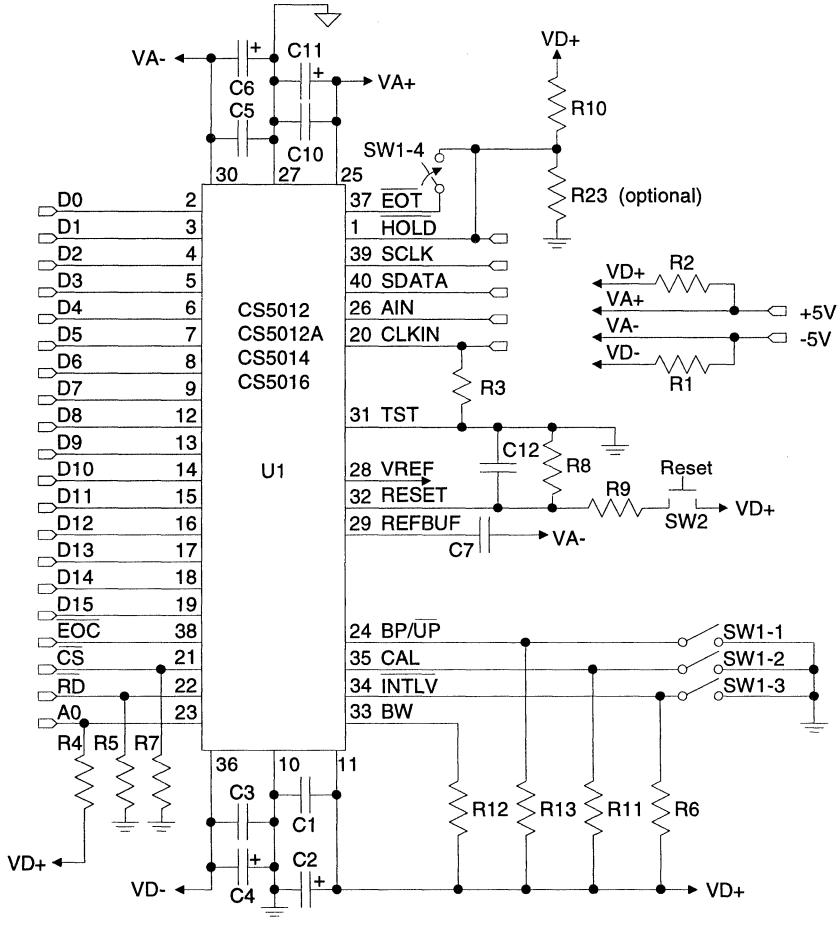


Figure 1. CDB5012, CDB5012A, CDB5014, CDB5016 Schematic (Reference Circuitry Appears in Figure 3)

	OFF	ON
Position 1	Bipolar	Unipolar
Position 2	Burst Cal *	Normal Operation
Position 3	Normal	Interleaved Cal
Position 4	Normal	Continuous Conversion

* NOTE: Use of BURST CAL is not recommended.

Figure 2. DIP-Switch Definitions

Initiating Conversions

A negative transition on the converter's $\overline{\text{HOLD}}$ pin places the device's analog input into the hold mode and initiates a conversion cycle. On the CDB5012, CDB5012A, CDB5014, CDB5016, this input can be generated by one of two means. First, it can be supplied through the BNC coaxial connector appropriately labeled $\overline{\text{HOLD}}$. Alternatively, switch position 4 of the DIP-switch can be placed in the on position, thus looping the converter's $\overline{\text{EOT}}$ output back to $\overline{\text{HOLD}}$. This results in continuous conversions at a fraction of the master clock frequency (see "synchronous operation" in the converter's data sheet).

The A/D converter's $\overline{\text{EOT}}$ output is an indicator of its acquisition status; it falls when the analog input has been acquired to the specified accuracy. If an external sampling clock is applied to the $\overline{\text{HOLD}}$ BNC connector, care must similarly be taken to obey the converter's acquisition and maximum sampling rate requirements. A more detailed discussion of acquisition and throughput can be found in the converter's data sheet.

The CDB5012, CDB5012A, CDB5014, CDB5016 is shipped from the factory without the $\overline{\text{HOLD}}$ BNC input terminated for operation with an external sampling clock. However, location R23 is reserved for the insertion of a 51 Ω resistor to eliminate reflections of the incoming clock signal.

Voltage Reference Circuitry

The CDB5012, CDB5012A, CDB5014, CDB5016 features an adjustable voltage reference which allows characterization over a wide range of reference voltages. The circuitry consists of a 2.5V voltage reference (1403) and an adjustable gain block with a discrete output stage (Figure 3). The output stage minimizes the output's headroom requirements allowing the reference voltage to come within 300mV of the positive supply.

The coarse and fine trim potentiometers are factory calibrated to a reference voltage of 4.5V (a table of output code values for a reference voltage of 4.5V appears in the CS5012, CS5012A, CS5014, CS5016 data sheets). When calibrating the reference, the voltage should be measured directly at the VREF input (pin 28) or at the ungrounded lead of decoupling capacitor C9.

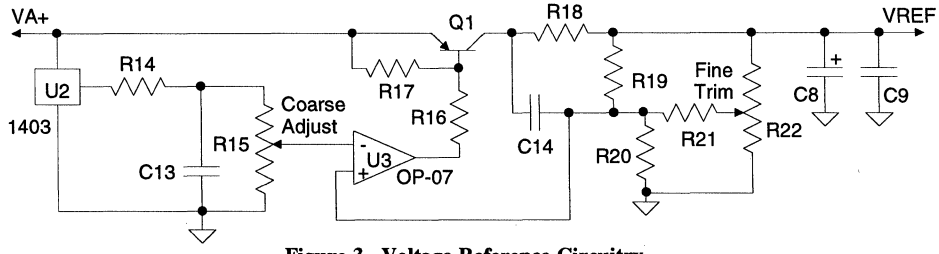


Figure 3. Voltage Reference Circuitry

Reset/Self-Calibration Modes

The A/D converter will usually reset itself upon power-up. Since this function is not guaranteed, the converter must be reset upon power-up in system operation. The converter can be reset on the CDB5012, CDB5012A, CDB5014, CDB5016 board by momentarily depressing push-button SW-2 thus initiating a full calibration cycle; 1,443,840 master clock cycles later the converter is ready for normal operation.

The converters also feature two other calibration modes: burst and interleave. The use of Burst calibration is not recommended. Interleave can be initiated by setting switch position 3 to the on position. In the interleave mode ($\overline{\text{INTRLV}}$ low), the converter appends one small portion of a calibration cycle (20 master clock cycles) to each conversion cycle. Thus, a full calibration cycle completes every 72,192 conversion cycles. The Interleave calibration mode should not be used intermittently.

A more detailed discussion of the converters' calibration modes and capabilities can be found in their data sheets.

Parallel Output Data/Microprocessor Interface

The converter's outputs D0-D15, its $\overline{\text{CS}}$, $\overline{\text{RD}}$, and A0 inputs, and its $\overline{\text{EOC}}$ output are available at the 40 pin header. The $\overline{\text{CS}}$ and $\overline{\text{RD}}$ inputs are pulled low through 10 kΩ resistors placing the converter in a microprocessor-independent mode. Control input A0 is pulled up, insuring the converter's output word, rather than the status register, appears at the header.

The converter's 3-state output buffers and microprocessor interface can be exercised by driving the $\overline{\text{CS}}$ and/or $\overline{\text{RD}}$ inputs at the header. Similarly, the converter's 8-bit status register can be obtained on D0-D7 by driving A0 low.

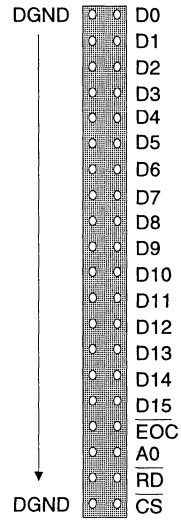


Figure 4. Header Pin Definitions

The converter's $\overline{\text{EOC}}$ and data outputs are not buffered on the CDB5012, CDB5012A, CDB5014, CDB5016. Therefore, careful attention should be paid to the load presented by any cabling, especially if the 3-state output buffers are to be exercised at speed. Twisted ribbon cable is typically specified at 10pF/ft, so several feet can generally be accommodated.

Serial Output Data

Serial output data is available at the two BNC connections SCLK and SDATA. Data appears MSB first, LSB last, and is valid on the rising edge of SCLK.

Master Clock

The A/D converter operates from a master clock which can either be internally-generated or externally-supplied. For operation with an external clock, the BNC connector labeled CLKIN should be driven with a TTL clock signal. The CDB5012, CDB5012A, CDB5014, CDB5016 is shipped from the factory with the CLKIN input

terminated by a 51 Ω resistor to eliminate line reflections of the incoming clock. If the CLKIN BNC input is left floating, this resistor pulls the converter's clock input down to ground, thus activating its internal oscillator.

Decoupling

The CDB5012, CDB5012A, CDB5014, CDB5016's decoupling scheme was designed to insure accurate evaluation of the converter's performance independent of the quality of the power supplies. Each supply is decoupled at the converter with a 10µF electrolytic capacitor to filter low frequency noise and a 0.1µF ceramic capacitor to handle higher frequencies. The auto-zeroing action of the converter's comparator provides extremely good power supply rejection at low frequencies. Depending on the quality of the system's power supplies, the decoupling scheme could be relaxed in actual use.

COMPONENT LIST

10 Ω resistor	R1, R2
51 Ω resistor	R3
4.7 Ω resistor	R18
1 kΩ resistor	R9, R14
560 Ω resistor	R17
10 kΩ resistor	R4, R5, R6, R7, R8, R10, R11, R12, R13
2.43 kΩ resistor	R19, R20
3.3 kΩ resistor	R16
240 kΩ resistor	R21
50 kΩ potentiometer	R15
50 kΩ potentiometer	R22
0.068 µF capacitor	C14
0.1 µF capacitor	C1, C3, C5, C7, C9, C10, C12
10 µF capacitor	C2, C4, C6, C8, C11, C13
CS501X/511X A/D converter	U1
1403 2.5V reference	U2
OP07 op amp	U3
2N2907A transistor	Q1
4 pos. SPST DIP switch	SW1
N.O. SPST push-button	SW2
20 pin header	CON1
bulkhead BNC	CON2, CON3, CON4, CON5, CON6
red banana jack	CON7
black banana jack	CON8
green banana jack	CON9
1" 4-40 spacer	POST1, POST2, POST3, POST4, POST5, POST6
3/8" 4-40 screw	SC1, SC2, SC3, SC4, SC5, SC6

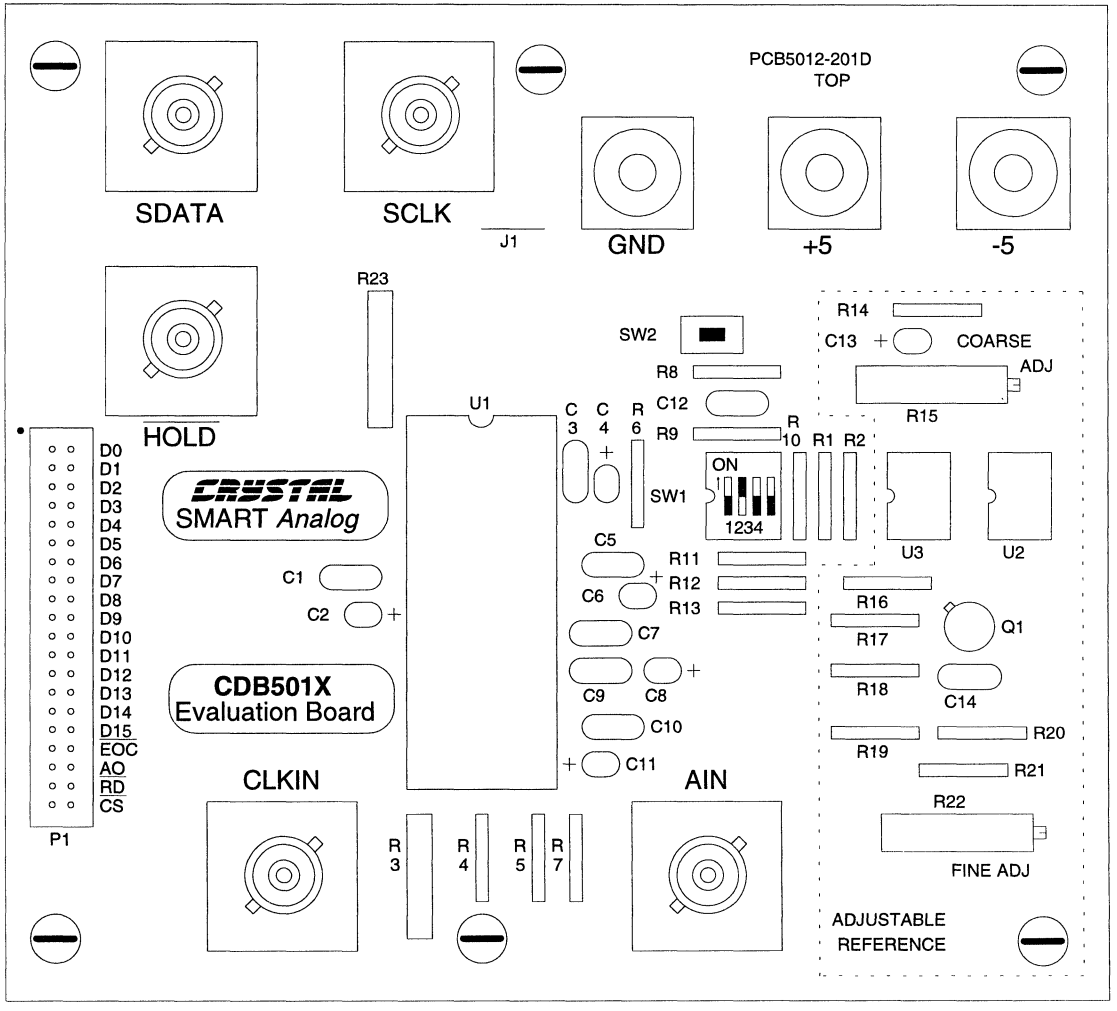


Figure 5. Board Layout

• Notes •

12-Bit, 500kSPS, Sampling A/D Converters

Features

- Monolithic CMOS A/D Converter
  - 0.3 µs Track/Hold Amplifier
  - 1.7 µs A/D Converter
  - 2.5 V Voltage Reference
  - Flexible Parallel, Serial and Byte interface
- 12-Bit ADC and Reference Accuracy
  - Total Unadjusted Error: 0.5 LSB
  - Ref Tempco: 1 ppm/°C
- Low Distortion
  - Signal-to-Noise Ratio: 72.8 dB
  - Total Harmonic Distortion: 0.01 %
  - Spurious-Free-Dynamic-Range: -80dBc
- Low Power: 88 mW

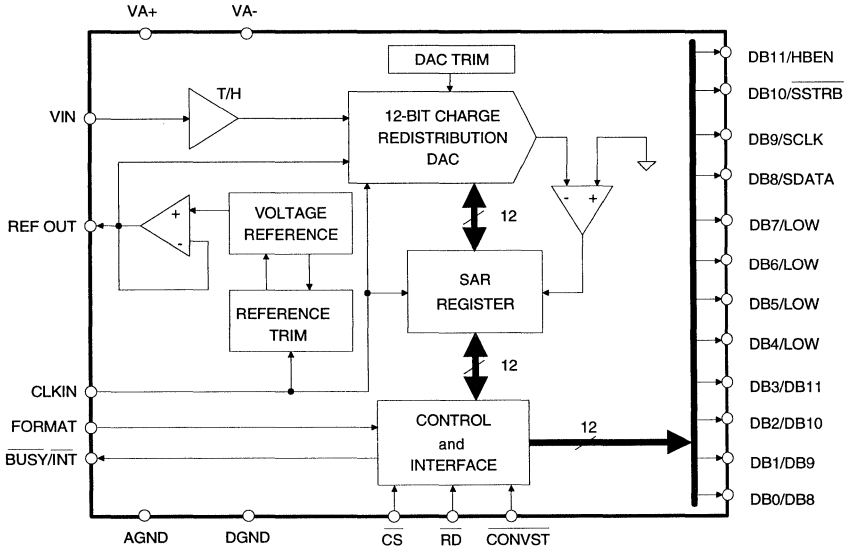
General Description

The CS5030, and CS5031 are complete monolithic CMOS analog-to-digital converters providing 500kSPS throughput. On-chip calibration circuitry achieves true 12-bit accuracy for the ADC and on-chip reference, over the full operating temperature range, without external adjustments.

The CS5030/CS5031 have a high speed digital interface with three-state data outputs and standard control inputs allowing easy interfacing to common microprocessors and digital signal processors. Conversion results are available in either 12-bit parallel, two 8-bit bytes, or serial data.

The CS5030/CS5031 are available in a 24-pin, 0.3" plastic dual-in-line package (PDIP), Cerdip and small outline (SOIC) package.

ORDERING INFORMATION: Page 2-77



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

ANALOG CHARACTERISTICS (VA+ = +5V±5%; VA- = -5V±5%; AGND = DGND = 0V; CLKIN = 10MHz, unless otherwise specified. $T_A = T_{MIN}$ to T_{MAX})

Parameter*		Symbol	B Min	B Typ	B Max	T Min	T Typ	T Max	Units
Specified Temperature Range	(Note 1)		-40 to +85			-55 to +125			°C
Accuracy									
Total Unadjusted Error	(Note 2)	TUE	-	0.5	1.0	-	0.5	1.0	LSB
Differential Nonlinearity		DNL	-	-	0.5	-	-	0.5	LSB
Integral Nonlinearity		INL	-	0.25	0.5	-	0.25	0.5	LSB
Unipolar Offset Error		V_{UP}	-	0.25	0.5	-	0.25	0.5	LSB
Bipolar Offset Error		V_{BP}	-	0.25	0.5	-	0.25	0.5	LSB
Positive Full Scale Error	(Note 3)	FSE_P	-	0.25	0.5	-	0.25	0.5	LSB
Bipolar Negative Full Scale Error	(Note 3)	FSE_N	-	0.25	0.5	-	0.25	0.5	LSB
Dynamic Performance	(Note 4)								
Signal-to-Noise Ratio		SNR	71.5	72.8	-	71	72.8	-	dB
Signal-to-Noise-and-Distortion	(Note 5)	SINAD	70	72	-	70	72	-	dB
Total Harmonic Distortion	(Note 6)	THD	-	-	0.01	-	-	0.01	%
Spurious-Free-Dynamic-Range	(Note 6)	SFDR	- -80	- -	0.01 -	- -80	- -	0.01 -	% dBc
Intermodulation Distortion Second Order Third Order	(Note 7)	IMD	 -80 -80	 - -	 - -	 -80 -80	 - -	 - -	 dBc dBc
Analog Input									
Input Voltage Range CS5030 CS5031		V_{IN}	 -2.5 0	 - -	 +2.5 +5	 -2.5 0	 - -	 +2.5 +5	 V V
Aperture Delay		t_{apd}	-	-	25	-	-	25	ns
Aperture Jitter		t_{apj}	-	-	100	-	-	100	ps
Input Capacitance		A_{cin}	-	-	10	-	-	10	pF

Notes:
1. All parameters guaranteed by design, test, and/or characterization.
2. TUE is measured using the on-chip reference.
3. Measured with respect to internal reference and includes bipolar offset error.
4. V_{IN} = ±2.5Vpp (CS5030), ... 0V to 5V (CS5031).
5. V_{IN} = 10kHz Sine Wave, f_{SAMPLE} = 500kSPS. Typically 71.5dB for 10kHz<V_{IN}<200kHz.
6. V_{IN} = 10kHz Sine Wave, f_{SAMPLE} = 500kSPS. Typically -80dB for 0<V_{IN}<200kHz.
7. fa = 9kHz, fb = 9.8kHz, f_{SAMPLE} = 500kSPS.

* Parameter definitions are given at the end of this datasheet prior to the package outline information.

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	B Min	B Typ	B Max	T Min	T Typ	T Max	Units
Specified Temperature Range		-40 to +85			-55 to +125			°C
Reference Output								
Output Voltage	V_R	2.49	-	2.51	2.49	-	2.51	V
REF OUT Tempco		0	-	1	-	-	1	ppm/°C
Load Regulation (Note 8)	$\Delta V_R/\Delta I$	-	0.6	1	-	0.6	1	mV
Output Noise Voltage	e_N	-	100	-	-	100	-	μV_{RMS}
Output Current Drive								
Source Current	I_{SOURCE}	-	500	-	-	500	-	µA
Sink Current	I_{SINK}	-	100	-	-	100	-	µA
Conversion & Throughput								
Conversion Time								
External Clock (CLKIN = 10MHz)	tconv	-	-	1.7	-	-	1.7	µs
Internal Clock		1.4	-	1.8	1.4	-	1.8	µs
Acquisition Time	t_{acq}	-	-	0.3	-	-	0.3	µs
Throughput	f_{tp}	500	-	-	500	-	-	kSPS
Power Supplies								
Positive Supply Current	I_{A+}	-	9.5	10	-	9.5	10	mA
Negative Supply Current	I_{A-}	-	7	10	-	7	10	mA
Power Dissipation	P_D	-	88	100	-	88	100	mW

Notes: 8. Reference Load Current Change (0-500 µA). Reference Load should not be changed during conversion.

LSB	%FS	ppm FS	mV
0.25	.0061	61	0.31
0.50	.0122	122	0.61
1.00	.0244	244	1.22
2.00	.0488	488	2.44
4.00	.0976	976	4.88

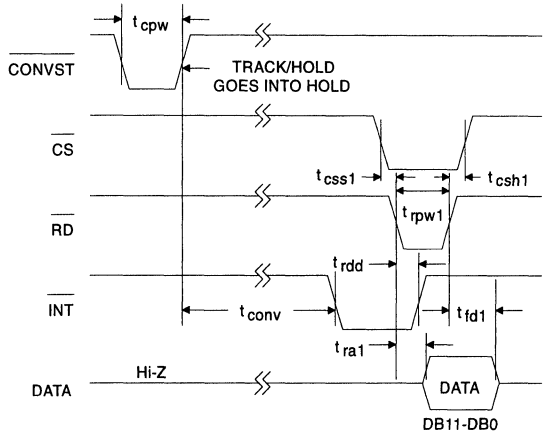
Unit Conversion Factors: CS5030 (V_{IN} = ±2.5V), CS5031 (V_{IN} = 0V to +5V)

SWITCHING CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+ = +5V±5%, VA- = -5V±5%; AGND = DGND = 0V, (Note 9))

Parameter		Symbol	B Min	B Typ	B Max	T Min	T Typ	T Max	Units
Specified Temperature Range			-40 to +85			-55 to +125			°C
CLKIN	Period	t_{clk}	100	-	400	100	-	400	ns
CLKIN	Low Time	t_{clkl}	0.4	-	0.6	0.4	-	0.6	MCC*
CLKIN	High Time	t_{clkh}	0.4	-	0.6	0.4	-	0.6	MCC*
Rise Times	Any Digital Input	t_{rise}	-	-	20	-	-	20	ns
	Any Digital Output	t_{rise}	-	20	-	-	20	-	ns
Fall Times	Any Digital Input	t_{fall}	-	-	20	-	-	20	ns
	Any Digital Output	t_{fall}	-	20	-	-	20	-	ns
Mode 1 Timing									
Conversion Time		t_{conv}	-	-	17	-	-	17	MCC*
CONVST Pulse Width		t_{cpw}	50	-	-	50	-	-	ns
$\overline{CS}$ Active to $\overline{RD}$ Active		t_{css1}	0	-	-	0	-	-	ns
$\overline{RD}$ Pulse Width		t_{rpw1}	60	-	-	75	-	-	ns
$\overline{RD}$ Inactive to $\overline{CS}$ Inactive		t_{csh1}	0	-	-	0	-	-	ns
$\overline{RD}$ Active to $\overline{INT}$ Inactive Delay		t_{rdd}	-	-	70	-	-	70	ns
Data Access Time after $\overline{RD}$	(Note 10)	t_{ra1}	-	-	57	-	-	70	ns
Output Float Delay: RD Rising to Hi-Z	(Note 11)	t_{fd1}	5	-	50	5	-	50	ns
HBEN to $\overline{RD}$ Active		t_{hrs}	0	-	-	0	-	-	ns
$\overline{RD}$ Inactive to HBEN Hold Time		t_{hrh}	0	-	-	0	-	-	ns
Serial Clock Timing									
SCLK to $\overline{SSTRB}$ Falling Time	(Note 12)	t_{sss}	25	-	-	25	-	-	ns
Serial Clock	Pulse Width High	t_{pwh}	0.4	-	0.6	0.4	-	0.6	MCC*
	Pulse Width Low	t_{pwl}	0.4	-	0.6	0.4	-	0.6	MCC*
SCLK rising to Data Valid	(Note 13)	t_{ss}	-	-	30	-	-	30	ns
SCLK rising to $\overline{SSTRB}$ Inactive		t_{ssr}	10	-	25	10	-	25	ns
SCLK rising to SDATA Hold Time		t_{sh}	10	-	25	10	-	25	ns

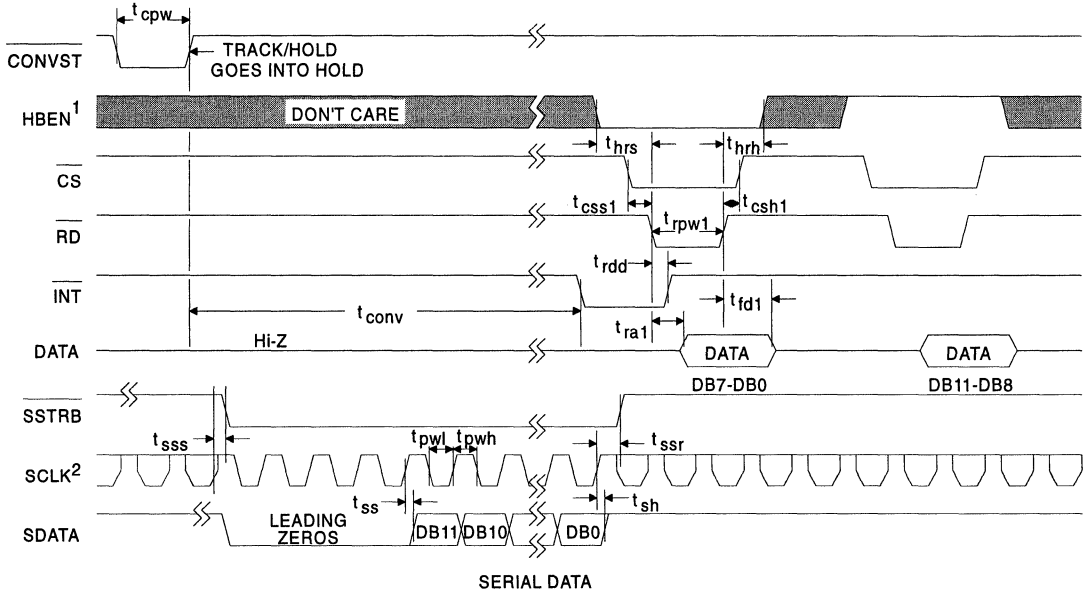
*MCC = Master Clock Cycles, 1 MCC = t_{clk}.

Notes:
9. All input signals are specified with $t_{rise} = t_{fall}$ = 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.
10. Measured with the load circuits of Figure 5 and defined as the time required for an output to cross 0.8V or 2.4V.
11. Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 6.
12. t_{sss} = MCC/2 - 25ns. t_{sss} = 25ns for t_{clk} = 100ns.
13. CL = 35pF. SDATA will drive higher capacitive loads but this will add to t_{ss}.



NOTE: FORMAT = +5V

Figure 1. Mode 1 Timing Diagram, 12-Bit Parallel Read



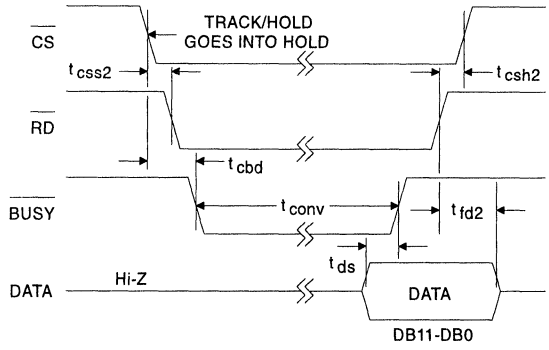
NOTES: 1. Times t_{css1}, t_{rpw1}, t_{csh1}, t_{hrs}, and t_{hrh} are the same for a high byte read as for a low byte read.
2. Continuous SCLK (Dashed ling) when FORMAT = -5V
Noncontinuous when FORMAT = 0V

Figure 2. Mode 1 Timing Diagram, Byte or Serial Read

SWITCHING CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+ = +5V±5%, VA- = -5V±5%; AGND = DGND = 0V, (Note 9))

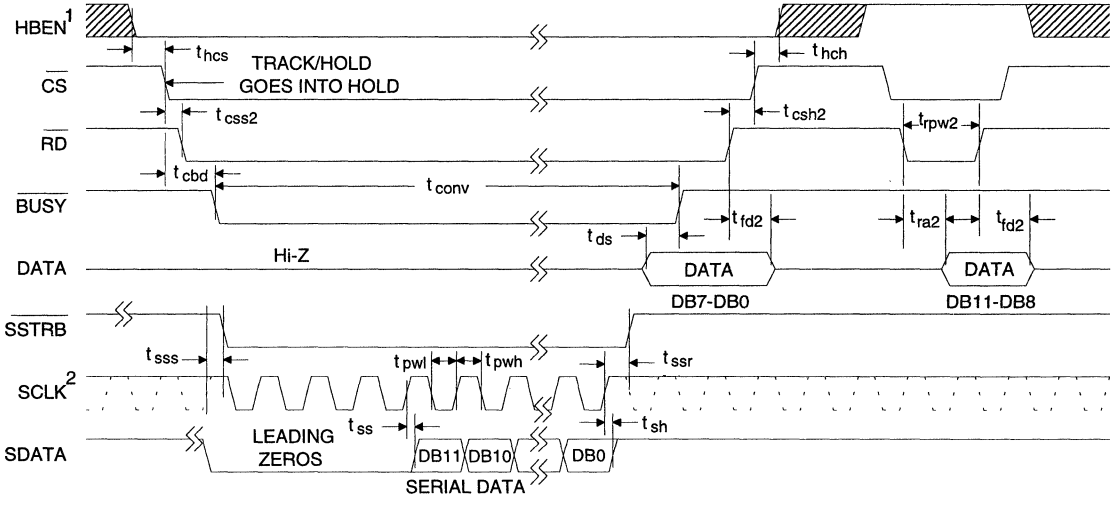
Parameter	Symbol	B Min	B Typ	B Max	T Min	T Typ	T Max	Units
Specified Temperature Range		-40 to +85			-55 to +125			°C
Mode 2 Timing								
Conversion Time	t_{conv}	-	-	17	-	-	17	MCC*
$\overline{CS}$ Active to $\overline{RD}$ Active	t_{css2}	0	-	-	0	-	-	ns
$\overline{CS}$ Active to $\overline{BUSY}$ Active	t_{cbd}	-	-	75	-	-	75	ns
Data Valid to $\overline{BUSY}$ Rising	t_{ds}	50	-	-	50	-	-	ns
$\overline{RD}$ Inactive to $\overline{CS}$ Inactive	t_{csh2}	0	-	-	0	-	-	ns
Output Float Delay: $\overline{RD}$ Rising to Hi-Z	t_{fd2}	5	-	50	5	-	50	ns
HBEN Low to $\overline{CS}$ Active	t_{hcs}	0	-	-	0	-	-	ns
$\overline{CS}$ Inactive to HBEN HIGH	t_{hch}	0	-	-	0	-	-	ns
$\overline{RD}$ Pulse Width	t_{rpw2}	60	-	-	75	-	-	ns
Data Access Time After $\overline{RD}$ (Note 10)	t_{ra2}	-	-	57	-	-	70	
Serial Clock Timing								
Serial Clock Pulse Width High	t_{pwh}	0.4	-	0.6	0.4	-	0.6	MCC*
Pulse Width Low	t_{pwl}	0.4	-	0.6	0.4	-	0.6	MCC*
SCLK rising to $\overline{SSTRB}$ Falling Time (Note 12)	t_{sss}	25	-	-	25	-	-	ns
SCLK rising to Data Valid (Note 13)	t_{ss}	-	-	30	-	-	30	ns
SCLK rising to $\overline{SSTRB}$ Inactive	t_{ssr}	10	-	25	10	-	25	ns
SCLK rising to SDATA Hold Time	t_{sh}	10	-	25	10	-	25	ns

*MCC = Master Clock Cycles, 1 MCC = t_{clk}.



NOTE: FORMAT = +5V.

Figure 3. Mode 2 Timing Diagram, 12-Bit Parallel Read



NOTES: 1. Times t_{hcs}, t_{css2}, t_{csh2} and t_{hch} are the same for a high byte read as for a low byte read.
2. Continuous SCLK (Dashed line) when FORMAT = -5V
Noncontinuous when FORMAT = 0V

Figure 4. Mode 2 Timing Diagram, Byte or Serial Read

DIGITAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}: VA+ = 5V±5%; VA- = -5V±5%)

Parameter		Symbols	Min	Typ	Max	Units
Logic Inputs						
High-level Input Voltage		V_{IH}	3.3	-	-	V
Low-level Input Voltage		V_{IL}	-	-	0.8	V
Input leakage current		I_{in}	-	-	50	µA
Input Capacitance		C_{in}	-	-	10	pF
Logic Outputs						
High-level Output Voltage	(Note 14)	V_{OH}	4.0	-	-	V
Low-level Output Voltage	(Note 15)	V_{OL}	-	-	0.4	V
DB11-DB0 Floating State leakage Current		I_{OZ}	-	-	50	µA
DB11-DB0 Output Capacitance		C_{out}	-	-	15	pF

Notes: 14. I_{source} = -40 µA
15. I_{sink} = 1.6 mA

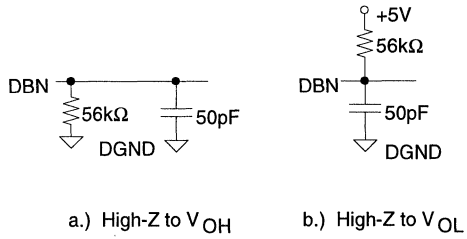


Figure 5. Load Circuits for Access Time

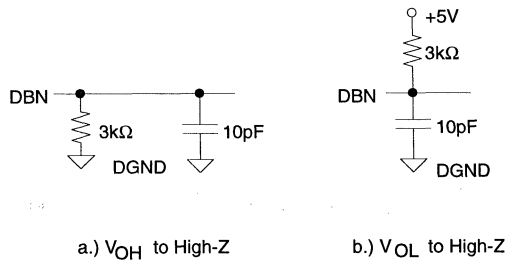


Figure 6. Load Circuits for Output Float Delay

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V. All voltages with respect to ground)

Parameter	Symbol	Min	Typ	Max	Units
Positive Analog Supply	VA+	4.75	5.0	5.25	V
Negative Analog Supply	VA-	-4.75	-5.0	-5.25	V
Analog Input Voltage	V_{IN}				V
CS5030		-2.5	-	+2.5	
CS5031		AGND	-	5	
FORMAT Input Voltage Range		VA-, OV, VA+			V
CLKIN Input Voltage Range		0	-	VA+	V
Other Digital Input Voltage Range		0	-	VA+	V
External Clock Frequency		-	10	-	MHz
External Clock Jitter		-	-	80	ps
AGND to DGND Voltage Differential		-	-	±10	mV

ABSOLUTE MAXIMUM RATINGS* (AGND = 0V, All voltages with respect to ground)

Parameter	Symbol	Min	Typ	Max	Units
Positive Analog Supply	VA+	-0.3	-	6.0	V
Negative Analog Supply	VA-	0.3	-	-6.0	V
Analog Input Voltage	V_{IN}		-		V
CS5030		(VA-)-0.3		(VA+)+0.3	
CS5031		(VA-)-0.3		(VA+)+0.3	
FORMAT Input Voltage Range		(VA-)-0.3	-	(VA+)+0.3	V
CLKIN Input Voltage Range		(VA-)-0.3	-	(VA+)+0.3	V
Other Digital Input Voltage Range		-0.3	-	(VA+)+0.3	V
REF OUT Current		-	-	10	mA
Digital Output Current		-	-	5	mA
AGND to DGND Voltage Differential		-		100	mV
Operating Temperature Range					
CS5030/5031-BP/BS		-40	-	+85	°C
CS5030/5031-TD		-55	-	+125	°C
Storage Temperature Range		-65	-	+150	ÉC
Lead Solder Temperature (10sec duration)		-	-	+300	°C

* WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

NOTE: Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

GENERAL DESCRIPTION

The CS5030 and CS5031 are complete 12-bit 500 kSPS sampling ADCs, utilizing a successive approximation architecture. Factory calibration ensures 12-bit conversion accuracy over industrial and military temperature ranges. The CS5030 analog input range is ±2.5 V (0 V to +5 V for the CS5031), with the output data provided in parallel, byte or serial formats. The internal capacitor array DAC acts as an inherent sample-and-hold, and forms the heart of the CS5030/CS5031. The on-chip +2.5 V reference is available at the REFOUT pin. Additionally, an on-chip 10 MHz clock oscillator can be used to control converter operations.

OPERATIONAL OVERVIEW

Track-and-Hold Operation

Track-and-hold operation within the CS5030/CS5031 is transparent to the user. The capacitor array DAC acts as the hold capacitor. During tracking mode all elements of the capacitor array DAC are switched to the analog input for charging. The load capacitance of the entire array during tracking mode is typically 5 pF. The input bandwidth of the track-and-hold is typically 2 MHz. The ADC goes into hold mode on the rising edge of $\overline{\text{CONVST}}$.

Capacitor Array DAC Calibration

To achieve 12-bit accuracy from the capacitor array DAC, the CS5030/CS5031 uses a novel calibration scheme. Each bit capacitor consists of several capacitors that are trimmed to optimize the overall bit weighting with an internal resolution of 14-bits, resulting in nearly ideal differential and integral linearity.

The calibration coefficients for the capacitive bit weights are stored in an on-chip EEPROM during the factory calibration. When the converter is subsequently powered-up these coefficients are applied to the capacitor array DAC. The low temperature coefficient of the capacitor array easily maintains 12-bit accuracy over the full temperature range.

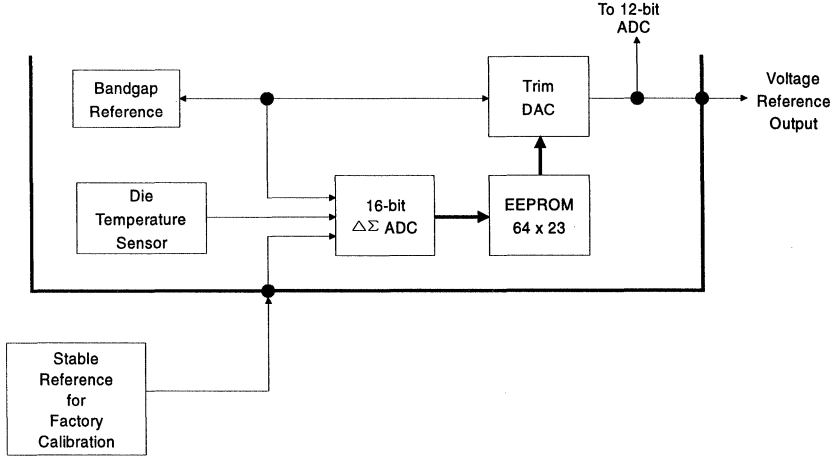


Figure 7. Reference Temperature Control Block

Reference Calibration

The CS5030/CS5031 employs an internal reference calibration circuit to maintain less than 200 µV of error. A first order corrected low-drift band-gap reference is the foundation of the reference trim block (Figure 7). This reference is combined with an on-chip temperature sensor and an EEPROM-based look-up table to provide unmatched reference accuracy.

During normal operation of the device, a 16-bit delta-sigma (Δ–Σ) ADC independently monitors the chip's temperature every 800 ms. As the temperature varies a segment of the EEPROM is selected based on the Δ–Σ converter's output word. The EEPROM output is used to control the trim DAC which compensates the bandgap reference voltage. This trim circuit maintains the output reference voltage to the ADC and REF OUT pin to within ±200 µV of 2.5 V over the full temperature range.

During factory calibration the 16-bit Δ-Σ converter takes measurements at several temperature points to establish a profile of the bandgap reference temperature drift (Figure 8). At each temperature point the Δ–Σ converter calculates the error voltage between a stable external 2.5 V reference and the actual bandgap reference voltage. Additionally, the Δ–Σ converter also measures the absolute temperature of the chip (from an on-chip sensor) as well as it's own offset and gain errors. All of these results are uniquely stored in the device EEPROM to be accessed during final test.

During final test the four 16-bit words associated with each temperature point are read by the tester. The test system performs a trapezoidal approximation in software for each of the temperature segments. Digital words representing temperature, slope and intercept are then downloaded from the test system back into the EEPROM on the chip (Figure 9).

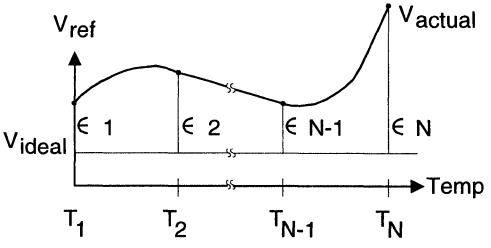


Figure 8. Untrimmed Reference Voltage versus Temperature

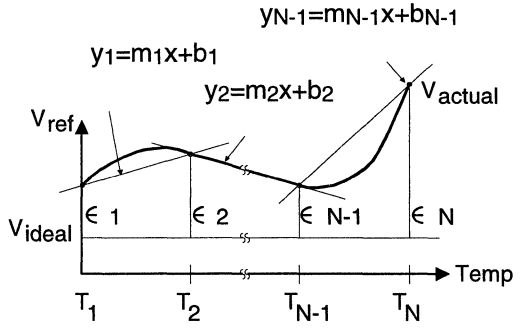


Figure 9. Slopes and Intercepts are Calculated for the Intermediate Temperatures

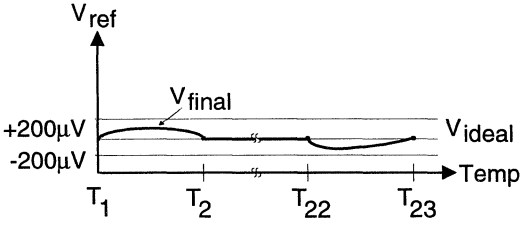


Figure 10. The Adjusted Reference Error is Within 200µV of 2.5V

When the converter is in normal operation, the on-chip bandgap reference trim circuit is trimmed over temperature. Depending on the temperature of the chip, the Δ–Σ converter selects the appropriate temperature segment stored in EEPROM. Using the corresponding slope and intercept data for the temperature in question, the appropriate correction factor is provided by the trim DAC to maintain the output voltage reference error within ±200 µV of the ideal 2.5 V (Figure 10).

The reference voltage is available at the REF OUT pin and is capable of sourcing 500 µA to peripheral devices. This pin must be decoupled with a parallel combination of a +10 µF tantalum capacitor and a 0.1 µF ceramic capacitor to AGND.

Full accuracy of the reference is achieved within 1.1 sec of power-up, after the trim circuitry has completed the calibration of the reference.

Analog Input

The CS5030 provides a ±2.5 V analog input voltage range, 0 V to +5 V for the CS5031. The equivalent analog input circuit is illustrated in Figure 11 (shown in track mode). During hold mode the input impedance to the device is typically 10 MΩ, and the various elements of the capacitor array DAC are connected to either AGND or VREF. In switching back from hold mode to track mode, some elements in the capacitor array must be charged by the analog input. For the CS5030, the worst case charging current occurs when the analog input changes from +2.5 V to -2.5 V. For the CS5031, the worst transition occures from +5 V to 0 V input changes.

To ensure that the capacitor array DAC has settled to within 0.25 LSB during the allowed acquisition time, the external source resistance should be less than 4 kΩ.

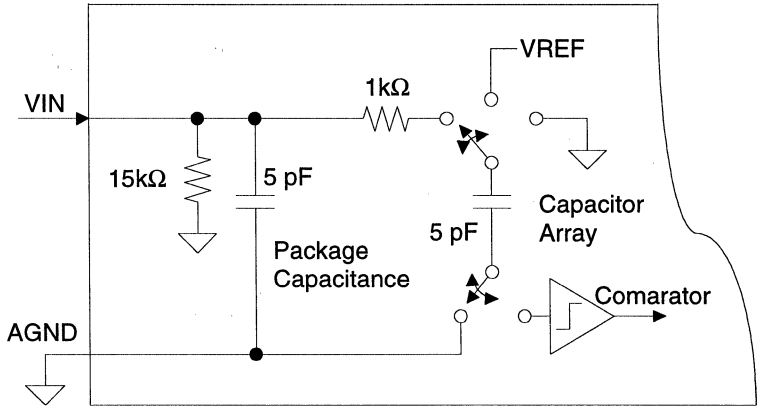


Figure 11. Analog Input Model.

Output Coding

The digital output coding ...

CS5030 Input	2's Complement Output
+2.5V	0111 1111 1111
0V	0000 0000 0000
-2.5V	1000 0000 0000

CS5031 Input	Binary Output
+5V	1111 1111 1111
+2.5V	0111 1111 1111
0V	0000 0000 0000

High-Speed System Clock

The CS5030/CS5031 employs a high-speed clock (typically 10 MHz) to control internal operations. This high-speed clock can be generated internally with the on-chip oscillator, or it can be supplied from an external CMOS source. Connecting a CMOS clock signal to the CLKIN pin allows the converter to operate from an external clock. Alternatively, connecting the CLKIN pin to VA- activates the internal clock oscillator.

External Clock ..... CLKIN = External Clock Source
Internal Clock ..... CLKIN = VA-

CONVERT Clock Considerations

When digitizing time varying signals, it is possible to create additional noise sources over and above those resulting from quantization noise and thermal noise. This is particularly true when high-speed conversion rates, or high-frequency analog input frequencies are involved. Special care must be taken to see that $\overline{\text{CONVST}}$ clock jitter does not undermine high-speed signal processing applications by introducing noise into the conversion process.

Simple quantization noise is a direct result of the finite LSB size, which is itself related to the number of digital output bits. Quantization noise places a hard limit on SNR for a 12-bit ADC according to the following equation.

$$SNR_{MAXQuantization} = (6.02dB)(\#\ of\ Bits) + 1.76dB$$

$$\ldots\ SNR_{MAXQuantization} = 74\ dB$$

Although SNR can never be better than the theoretical limit, it can certainly be worse. Jitter between the $\overline{\text{CONVST}}$ clock and the analog input signal is often one of the largest contributors to decreased SNR, particularly as frequencies increase.

To be considered insignificant, noise related to jitter ($SNR_{MAXjitter}$) should be at least 12 dB below the other dominant noise sources, such as quantization noise ($SNR_{MAXQuantization}$). The 12 dB target is somewhat arbitrary, but yields less than 4 % additional noise. In terms of the CS5030/CS5031, a 250 kHz analog input signal requires less than 80 ps of jitter between the $\overline{\text{CONVST}}$ clock and the analog input signal to achieve full performance. The use of low-jitter $\overline{\text{CONVST}}$ clock source is the most common means of reducing the effects of jitter. Lower conversion rates and lower analog input frequencies are significantly less sensitive to jitter effects.

$$SNR_{MAX} = \sqrt{SNR_{MAXjitter}^{2} + SNR_{MAXQuantization}^{2}}$$

$$SNR_{MAXjitter}\ (dB) = 20Log\left[\frac{V_{peak}}{2\pi f_{IN}\ jitter_{RMS}}\right]$$

$$jitter_{RMS} = \sqrt{clock\ jitter_{RMS}^{2} + analog\ jitter_{RMS}^{2}}$$

Digital Output Formats

The CS5030/CS5031 provides three digital output formats. These include 12-bit parallel, two 8-bit bytes, and a serial output mode. The output data format is controlled by the level applied to the FORMAT pin. All three of the digital output formats can be used with either of the convert start timing modes ... Mode 1 and Mode 2, which are described in the next two section.

FORMAT	Digital Outputs
+VA	12-Bit Parallel
GND	Byte; Serial w/Non-Continuous SCLK
-VA	Byte; Serial /Continuous SCLK

Figure 12 shows the schematic for the CS5030/CS5031 in 12-bit parallel mode. The twelve bits of data are output simultaneously on DB11/(MSB) through DB0 (LSB).

In byte mode, two 8-bit read operations (four leading zeros with 4 data bits ... plus 8 more data bits) are required to collect the data as shown in figure 13. In byte mode, the DB11/HBEN pin defers to the HBEN function, selecting the high or low byte of data to be read from the ADC. The lower eight bits of data are placed on the data bus when HBEN is held low. To access the four MSBs of data, HBEN must be held high. The 4 MSBs of the 12-bit data word are right

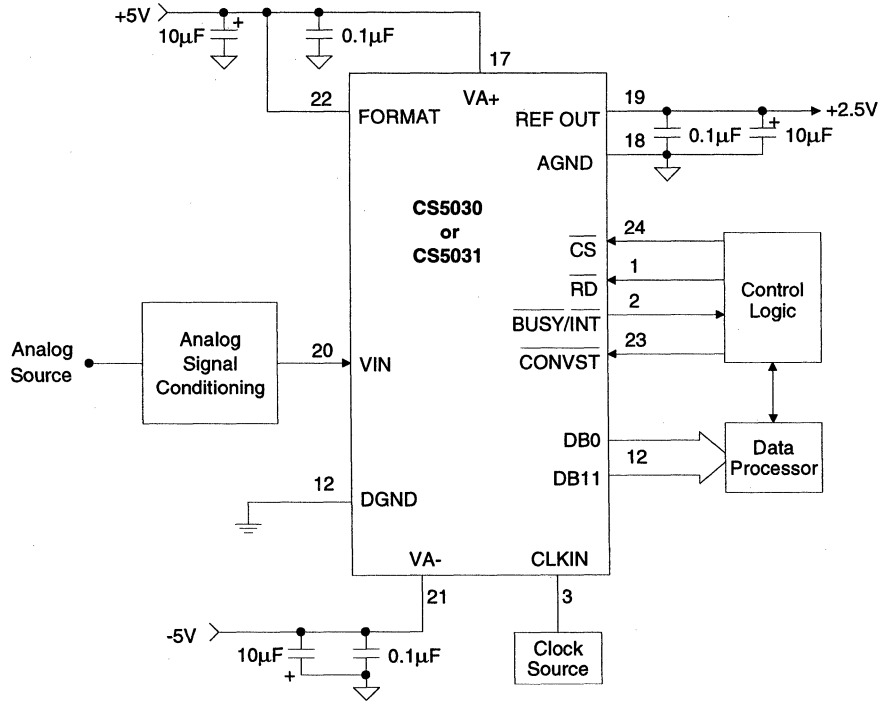


Figure 12. System Connection Diagram: Parallel Data Format

justified with zeros in the upper nibble of the high byte.

In serial mode, DB8/SDATA, DB9/SCLK and DB10/$\overline{SSTRB}$ defer to their serial functions. The serial strobe pin $\overline{SSTRB}$ provides a framing signal for serial data. Serial data is available at the SDATA pin when $\overline{SSTRB}$ falls low. $\overline{SSTRB}$ falls low within three clock cycles of $\overline{CONVST}$. A total of sixteen bits (four leading zeros and twelve data bits starting with the MSB) are clocked out on the SDATA pin on the rising edge of SCLK. The data bits become valid no more than t_{ss} after the rising edge of SCLK. $\overline{SSTRB}$ goes low during data transmission and automatically returns high when the LSB has been clocked out on the SDATA line. Serial data operation is identical for MODE 1 and MODE 2 timing control (see next two sections). For serial operation, 0V on the FORMAT pin causes the serial clock to run only when data is being clocked out of the device; SCLK goes high after data transmission is completed. If the FORMAT is connected to -VA, the SCLK output will run continuously, independent of data transmission.

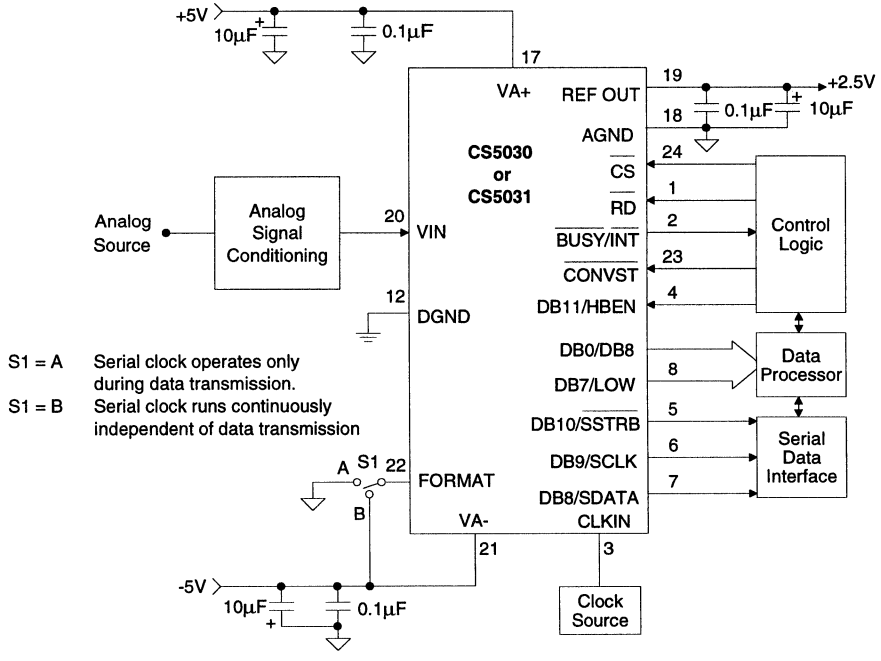


Figure 13. System Connection Diagram: Serial and Byte Data format

MODE 1 Operation

The rising edge of $\overline{\text{CONVST}}$ is used to put the device into hold mode and initiate a conversion. At the end of conversion the device returns to it's tracking mode. MODE 1 timing is primarily used in DSP type applications where precise control of $\overline{\text{CONVST}}$ timing is required.

Conversion begins on the rising edge of $\overline{\text{CONVST}}$ provided that $\overline{\text{CS}}$ is high. The $\overline{\text{BUSY/INT}}$ line performs the $\overline{\text{INT}}$ function and can be used to interrupt the microprocessor. $\overline{\text{INT}}$ is normally high and goes low at the end of conversion. The ADC returns to track mode when $\overline{\text{INT}}$ goes low. Bringing $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low allows data to be read from the ADC, and also resets $\overline{\text{INT}}$ high. $\overline{\text{CONVST}}$ must be high when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are brought low for the ADC to operate correctly in this mode. Data cannot be read during a conversion cycle because the output data latches are disabled while a conversion is in progress.

MODE 1 - 12-Bit Parallel Read

Figure 14 shows the MODE 1 timing diagram for 12-bit parallel operation (FORMAT = +VA). A data read operation performed at the end of conversion will read all twelve bits of data at the same time.

MODE 1 - Byte Read

Figure 15 shows the MODE 1 timing diagram for byte operation. At the end of conversion when INT goes low, either the low byte or the high byte of data can be read, depending on the status of HBEN. Bringing $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low allows data to be read from the ADC and also resets $\overline{\text{INT}}$ high.

MODE 1 - Serial Read

The MODE 1 timing diagram for serial operation is shown in figure 16. Conversion begins on the rising edge of $\overline{\text{CONVST}}$, and data is clocked out on SDATA immediately upon the falling edge of $\overline{\text{SSTRB}}$. The data is output as four leading zeroes followed by the twelve data bits with the MSB first. The first zero should be latched into the external receiving circuitry on the first falling edge of SCLK after $\overline{\text{SSTRB}}$ goes low. A total of sixteen falling SCLK edges will latch all sixteen bits of output data. $\overline{\text{SSTRB}}$ automatically returns high after the last bit of data has been clocked out of the device.

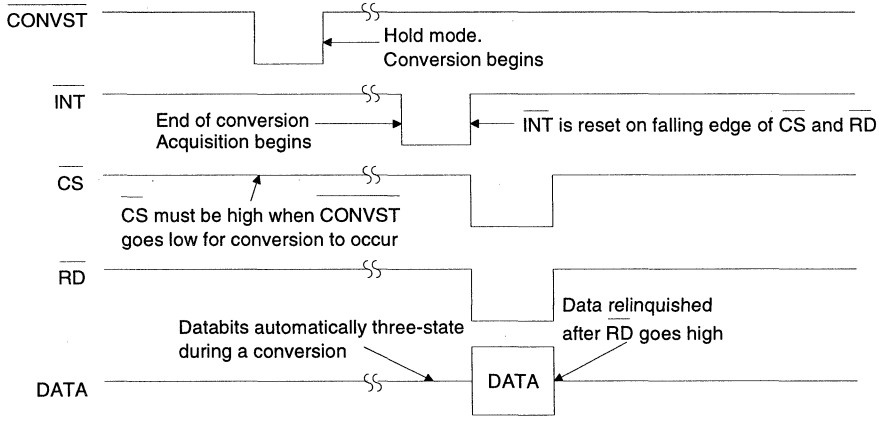
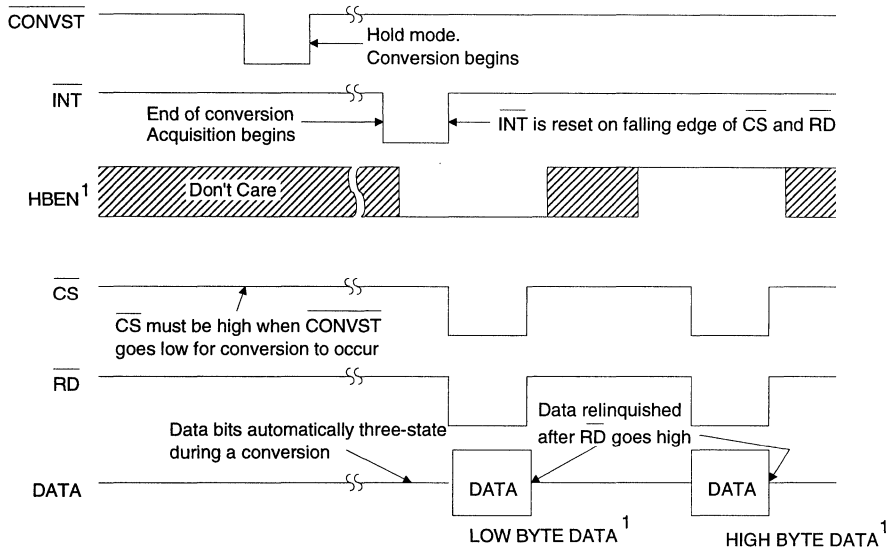


Figure 14. Mode 1 Timing Diagram, 12-bit Parallel Read



NOTE: 1. In the above diagram HBEN is exercised to read the low byte first (DB7-DB0) and then the high byte (DB11-DB8). To change the order in which the bytes are read, simply invert the HBEN signal shown above.

Figure 15. Mode 1 Timing Diagram, Byte Read

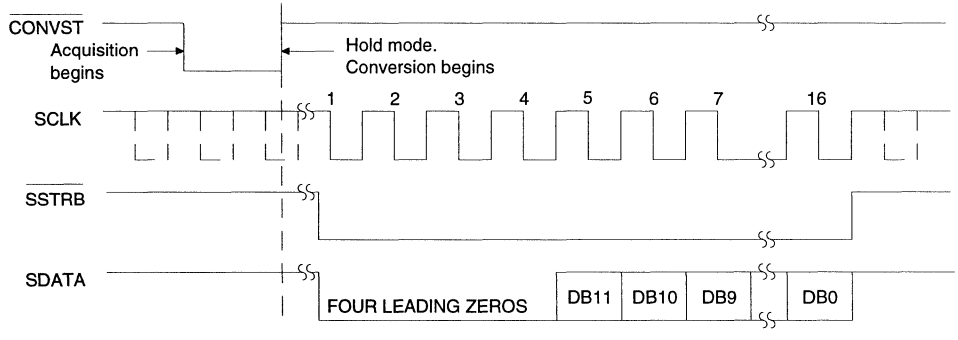


Figure 16. Mode 1 Timing Diagram - Serial Read

MODE 2 Operation

Mode 2 operation allows the ADC conversion to be initiated by a read operation from a µC. The $\overline{BUSY}$ signal can be used in this mode to halt µC operations by placing the µC in a WAIT state until the conversion is complete. This avoids having to handle interrupts and timing delays, assuring that the conversion cycle is complete before any attempted data read.

In this mode, $\overline{CONVST}$ must be held permanently low. Bringing $\overline{CS}$ low (while $\overline{HBEN}$ is low) puts the device into hold mode and initiates a conversion. The $\overline{BUSY}/\overline{INT}$ pin defers to the $\overline{BUSY}$ function such that $\overline{BUSY}$ goes low at the start of conversion and returns high at the end of conversion.

MODE 2 - 12-Bit Parallel Read

The MODE 2 timing diagrams for the parallel data output format are shown in figure 17. This mode of operation forces the µC into a WAIT state until the conversion has been completed. It removes the risk of inadvertently reading invalid data before the conversion cycle has been completed.

MODE 2 - Byte Read

Figure 18 shows the timing diagram for byte operation in MODE 2. Since $\overline{HBEN}$ must be low to initiate a conversion, the lower byte of data will be accessed first during the two-byte read operation. This is followed by a second byte read operation (with $\overline{HBEN}$ high) to complete the data transfer.

MODE 2 - Serial Read

The timing diagram for MODE 2 serial operation is shown in figure 19. The device goes into hold mode on the falling edge of $\overline{CS}$ and conversion begins when $\overline{BUSY}$ goes low. The data is clocked out similarly as for MODE 1 serial operation. Upon clocking of the final data bit $\overline{BUSY}$ returns high indicating end of conversion.

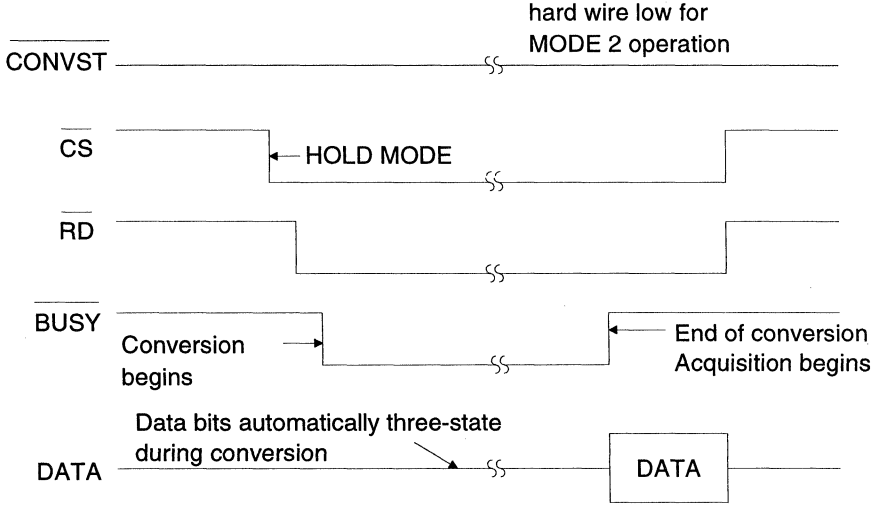


Figure 17. Mode 2 Timing Diagram, 12-bit Parallel Read

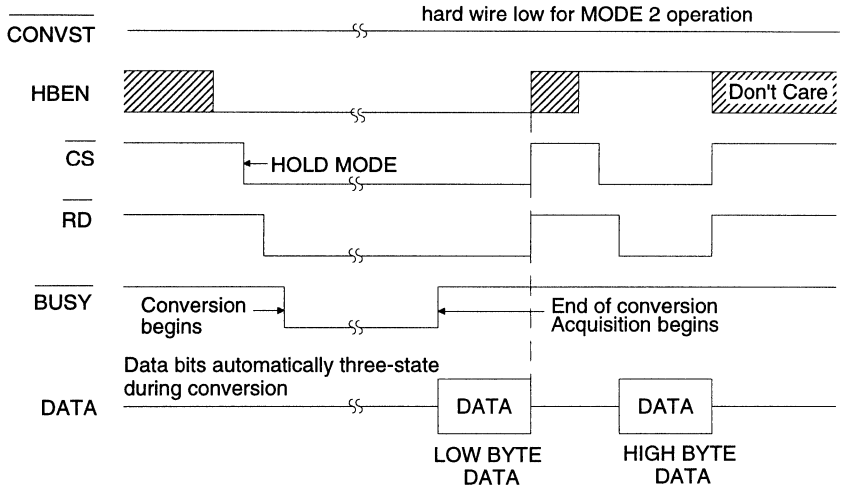


Figure 18. Mode 2 Timing Diagram, Byte Read

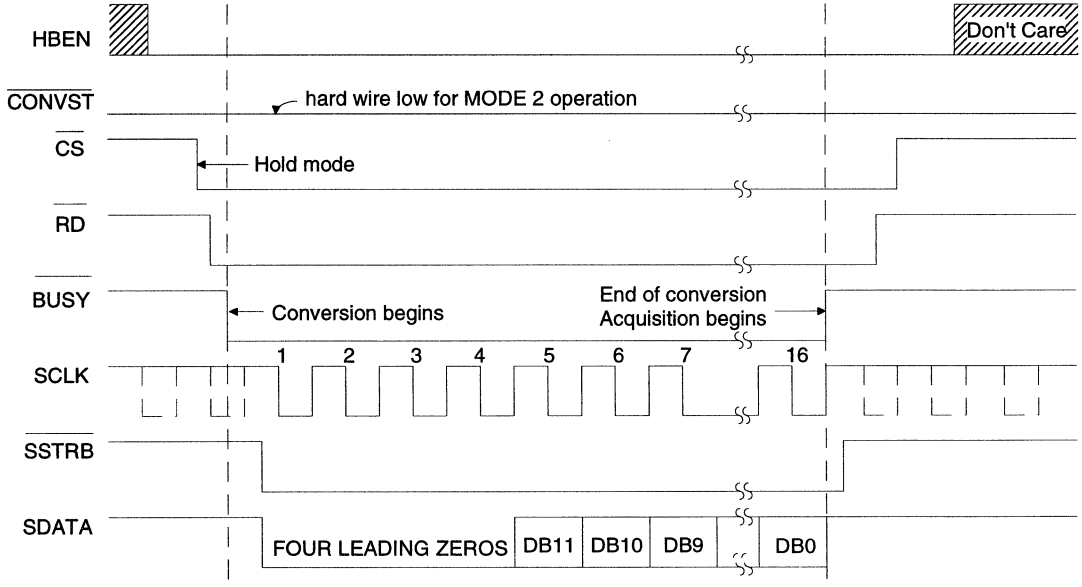


Figure 19. Mode 2 Timing Diagram, Serial Read

STAND-ALONE OPERATION

The CS5030/CS5031 supports stand-alone conversion when used in MODE 2 parallel interface operation as shown in Figure 20. Conversion is initiated by pulse to the $\overline{CS}$ input of the ADC. The duration of the pulse must be longer than the ADC conversion time. The $\overline{BUSY}$ output drives the $\overline{RD}$ input and data is latched on the rising edge of $\overline{BUSY}$ to an external latch.

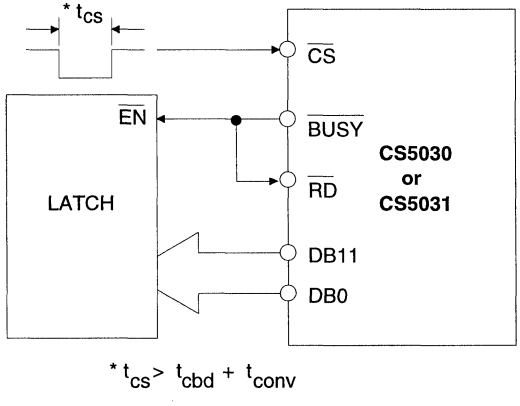


Figure 20. Stand-Alone Operation

Power Supplies, AGND, and DGND

Figure 12 illustrates the recommended power supply decoupling scheme with a 0.1µF ceramic and a +10µF tantalum capacitor for both the VA+ and the VA- pins. The capacitors should be located as close as practical to the supply pins. AGND is the power supply current return, and is also the preferred ground reference for the decoupling capacitors.

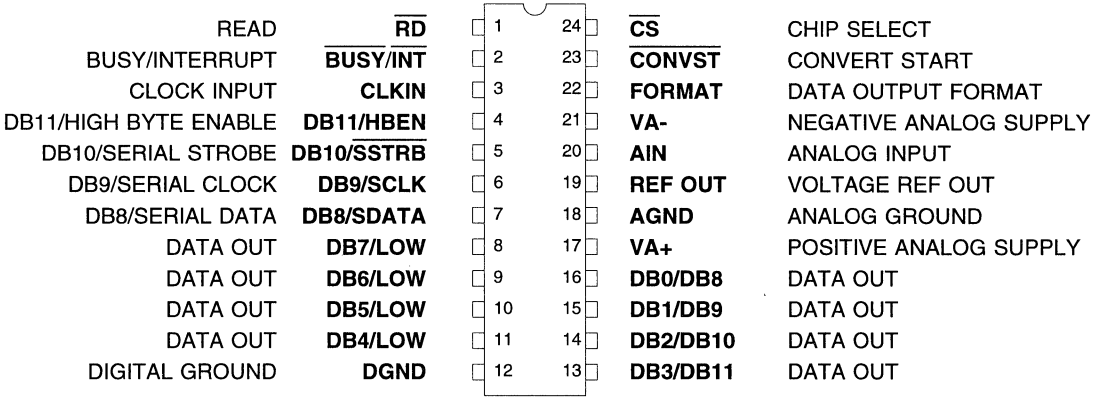
Typically a low-impedance ground plane is used around and under the ADC, with connections to both AGND and DGND. If a split ground is used, DGND is the ground reference for any digital circuits that follow the CS5030/CS5031. When split grounds are used, the AGND to DGND voltage differential should be kept below ±10mV for best operation.

If the power supply voltage is dropped below 3V, the ADC may need to be reset by switching power off and then back on.

Layout considerations

The CS5030/CS5031 is a high-speed component which requires adherence to standard high-frequency printed circuit board layout techniques to maintain optimum performance. These include proper supply decoupling, minimum length circuit traces, and physical separation of digital and analog components and circuit traces. See the CDB5032 evaluation board data sheet for more details.

PIN DESCRIPTIONS



Pinout applies to both DIP and SOIC packages.

Power Supply Connections

VA+ – Positive Supply, PIN 17.
+5V±5%.

VA- – Negative Supply, PIN 21.
-5V±5%.

DGND – Digital Ground, PIN 12.
Ground reference for digital circuitry.

AGND – Analog Ground, PIN 18.
Ground reference for track-and-hold, reference and DAC.

Oscillator

CLKIN – Clock Input, PIN 3.
An external 10 MHz (CMOS compatible) clock is applied at this pin. Connecting this pin to VA- enables the internal clock oscillator.

Digital Inputs

$\overline{CS}$ – Chip Select, PIN 24.
Active low logic input. The device is selected when this input is active. With $\overline{CONVST}$ tied low, a new conversion is initiated when $\overline{CS}$ goes low.

$\overline{RD}$ – Read, PIN 1.

Active low logic input. This input is used in conjunction with $\overline{CS}$ low to enable the data outputs.

FORMAT – Output Mode Selection, PIN 22.

Defines the output data format and serial clock format. With FORMAT at +5V, the output data format is 12-bit parallel only. With FORMAT at 0V, either byte or serial data is available and SCLK is not continuous. With FORMAT at -5V, byte or serial data is again available but SCLK is now continuous.

$\overline{CONVST}$ – Convert Start, PIN 23.

A low to high transition on this input puts the track-and-hold into its hold mode and starts conversion. This input is asynchronous to the CLKIN and independent of $\overline{CS}$ and $\overline{RD}$.

Digital Outputs

$\overline{BUSY}/\overline{INT}$ – Busy/Interrupt, PIN 2.

Active low logic output indicating converter status. See timing diagrams.

DB11/HBEN – Data Bit 11/High Byte Enable, PIN 4.

The function of this pin is dependent on the state of the FORMAT input (see above). When 12-bit parallel data is selected, this pin provides the DB11 output. When byte data is selected, this pin becomes the HBEN logic input. HBEN is used for 8-bit bus interfacing. When HBEN is low, DB7/LOW to DB0/DB8 become DB7 to DB0. With HBEN high, DB7/LOW to DB0/DB8 are used for the upper byte of data (see Table 1).

DB10/$\overline{SSTRB}$ – Data Bit 10/Serial Strobe, PIN 5.

The function of this pin is dependent on the state of the FORMAT input (see above). When 12-bit parallel data is selected, this pin provides the DB10 output. If FORMAT is at either 0V or -5V, $\overline{SSTRB}$ provides a strobe or framing pulse for the serial data.

DB9/SCLK – Data Bit 9/Serial Clock, PIN 6.

The function of this pin is dependent on the state of the FORMAT input (see above). When 12-bit parallel data is selected, this pin provides the DB9 output. SCLK is the gated serial clock output derived from the internal or external ADC clock. If FORMAT is at -5V, then SCLK runs continuously. If FORMAT is at 0V, then SCLK goes high after serial transmission is complete.

DB8/SDATA – Data Bit 8/Serial Data, PIN 7.

The function of this pin is dependent on the state of the FORMAT input (see above). When 12-bit parallel data is selected, this pin provides the DB8 output. SDATA is used with SCLK and $\overline{SSTRB}$ for serial data transfer. Serial data is valid on the falling edge of SCLK while $\overline{SSTRB}$ is low.

DB7/LOW, DB6/LOW, DB5/LOW, DB4/LOW – Three-state data outputs, PINS 8, 9, 10, 11.

The outputs of these pins are controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the FORMAT and HBEN inputs. With FORMAT high, they are always DB7-DB4. With FORMAT low or -5V, their function is controlled by HBEN (see Table 1).

DB3/DB11, DB2/DB10, DB1/DB9, DB0/DB8 – Three-state data outputs, PINS 13, 14, 15, 16.

The outputs of these pins are controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the FORMAT and HBEN inputs. With FORMAT high, they are always DB3-DB0. With FORMAT low or -5V, their function is controlled by HBEN (see Table 1).

HBEN	DB7/LOW	DB6/LOW	DB5/LOW	DB4/LOW	DB3/DB11	DB2/DB10	DB1/DB9	DB0/DB8
HIGH	LOW	LOW	LOW	LOW	DB11/(MSB)	DB10	DB9	DB8
LOW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0/(LSB)

Table 1. Output Data for Byte Interfacing

Analog Output

REF OUT - Voltage Reference Output, PIN 19.

The internal 2.5V reference is provided at this pin. The external load capability is 500µA. This pin should be decoupled to AGND with a +10µF tantalum and a 0.1µF ceramic capacitor. The REF OUT voltage has a settling time of approximately 1.1 sec.

Analog Input

V_{IN} - Analog Input, PIN 20.

The analog input range for the CS5030 is ±2.5V, and unipolar 0 to +5V for the CS5031.

Ordering Guide

Model Number	Throughput (kSPS)	Input Range (V)	Total Unadjusted Error (LSB)	Temp. Range (°C)	Package
CS5030-BP	500	±2.5	1	-40 to +85	24-Pin 0.3" PDIP
CS5030-BS	500	±2.5	1	-40 to +85	24-Pin 0.3" SOIC
CS5030-TD	500	±2.5	1	-55 to +125	24-Pin 0.3" CERDIP
CS5031-BP	500	0V to +5	1	-40 to +85	24-Pin 0.3" PDIP
CS5031-BS	500	0V to +5	1	-40 to +85	24-Pin 0.3" SOIC
CS5031-TD	500	0V to +5	1	-55 to +125	24-Pin 0.3" CERDIP

PARAMETER DEFINITIONS

Total Unadjusted Error - TUE

Total Unadjusted Error includes offset, gain, linearity, and reference errors.

REF OUT Tempco

REF OUT Tempco is the worst case slope that is calculated from the change in reference value at +25°C to the value at T_{MIN} or T_{MAX}

i.e. REF OUT Tempco = (V_{ref} @ 25°C - V_{ref} @ T_{MAX})/(T_{MAX} - 25°C) or

REF OUT Tempco = (V_{ref} @ 25°C - V_{ref} @ T_{MIN})/(25°C - T_{MIN}).

Differential Nonlinearity - DNL

The deviation of a code's width from the ideal width. Units in LSBs.

Positive Full-Scale Error - FSE_P

The deviation of the last code transition from the ideal (VREF-3/2LSB's). Units in LSB's.

Unipolar Offset (CS5031) - V_{UP}

The deviation of the first code transition from the ideal (1/2 LSB above AGND). Units in LSB's.

Bipolar Offset (CS5030) - V_{BP}

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below AGND). Units in LSB's.

Bipolar Negative Full-Scale Error (CS5030) - FSE_N

The deviation of the first code transition from the ideal. The ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSB's.

Spurious-Free-Dynamic-Range - SFDR

The ratio of the rms value of the signal, to the rms value of the next largest spectral component (excepting dc). This component is often an aliased harmonic. Units in percent and dBc (decibels relative to the carrier).

Total Harmonic Distortion - THD

The ratio of the rms sum of the significant (2^{ND} thru 5^{TH}) harmonics, to the rms value of the signal. Units in percent.

Signal-to-Noise Ratio (s/n) - SNR

The ratio of the rms value of the signal, to the rms sum of all other spectral components (excepting dc and distortion). Expressed in decibels.

Signal-to-Noise-and-Distortion (s/[n+d]) - SINAD

The ratio of the rms value of the signal, to the rms sum of all other spectral components (excepting dc), including distortion components. Expressed in decibels.

Intermodulation Distortion - IMD

The ratio of the rms value of the larger of the two test frequencies, which are each 6dB down from full-scale, to the rms value of the largest 2^{ND} order and 3^{RD} order intermodulation components. Units in decibels relative to carrier.

Aperture Delay Time - t_{apd}

The time required after the $\overline{CONVST}$ goes low, for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Unit in nanoseconds.

Aperture Jitter - t_{apj}

The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy.

To ensure that jitter does not affect the quantized signal quality, the jitter induced noise ($SNR_{MAXjitter}$) must be at least 12dB below other substantial noise sources, such as quantization noise, see *Clock Considerations*. Units in picoseconds.

$$SNR_{MAXjitter}\,(dB) = 20Log\left[\frac{V_{peak}}{2\pi f_{IN}\,jitter_{RMS}}\right]$$

$$jitter_{RMS} = \sqrt{clock\ jitter_{RMS}^{2} + analog\ jitter_{RMS}^{2}}$$

• Notes •

12-Bit, 500kSPS, Sampling A/D Converter

Features

- Monolithic CMOS A/D Converter
  - 0.4 µs Track/Hold Amplifier
  - 1.6 µs A/D Converter
  - 2.5 V Voltage Reference
  - Parallel, Serial and Byte Interface.
- 12-Bit ADC Linearity Error: 0.5 LSB
- Low Distortion
  - Signal-to-Noise Ratio: 72.8 dB
  - Total Harmonic Distortion: 0.01 %
  - Spurious-Free-Dynamic-Range: -80dBc
- Low Power: 85 mW
- 60 ppm/°C Reference Drift

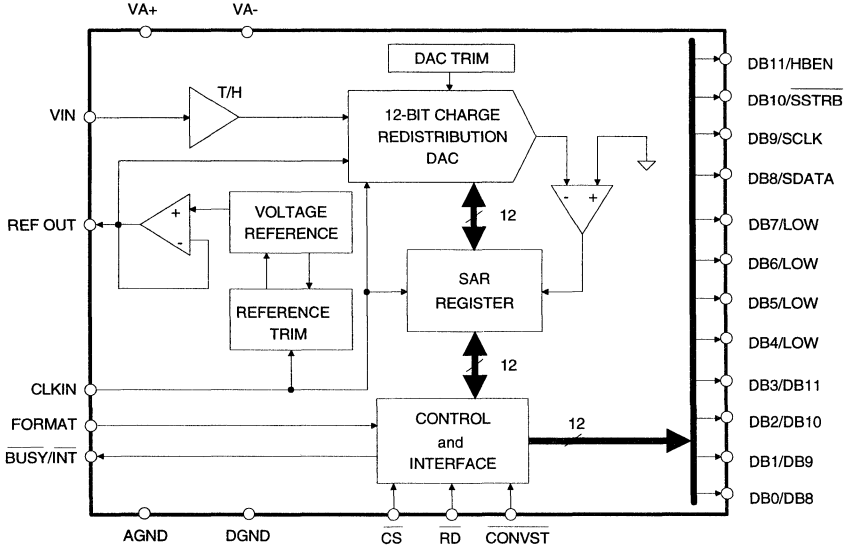
General Description

The CS5032 is a complete monolithic CMOS analog-to-digital converter providing 500kSPS throughput. The part has an internal sample-and-hold, voltage reference, and can operate with an internal or external clock.

The CS5032 has a high-speed digital interface with three-state data outputs and standard control inputs allowing easy interfacing to common microprocessors and digital signal processors. Digital output data is available in either 12-bit parallel, two 8-bit bytes, or serial formats.

The CS5032 is available in a 24-pin, 0.3" plastic dual-in-line package (PDIP), Cerdip and small outline (SOIC) package.

ORDERING INFORMATION: Page 2-101



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

ANALOG CHARACTERISTICS (VA+ = +5V±5%; VA- = -5V±5%; AGND = DGND = 0V; CLKIN = 10MHz, unless otherwise specified. $T_A = T_{MIN}$ to T_{MAX})

Parameter	(Note 1)	Symbol	B Min	B Typ	B Max	T Min	T Typ	T Max	Units
Specified Temperature Range			-40 to +85			-55 to +125			°C
Accuracy									
Integral Nonlinearity		INL	-	0.25	0.5	-	0.25	0.5	LSB
Differential Nonlinearity		DNL	-	-	0.5	-	-	0.5	LSB
Unipolar Offset Error		V_{UP}	-	0.25	0.5	-	0.25	0.5	LSB
Bipolar Zero Error		V_{BP}	-	0.25	0.5	-	0.25	0.5	LSB
Positive Full Scale Error	(Note 2)	FSE_P	-	0.25	0.5	-	0.25	0.5	LSB
Bipolar Negative Full Scale Error	(Note 2)	FSE_N	-	0.25	0.5	-	0.25	0.5	LSB
Dynamic Performance	(Note 3)								
Signal-to-Noise-and-Distortion	(Note 4)	SINAD	70	72	-	70	72	-	dB
Signal-to-Noise Ratio		SNR	70.5	72.8	-	70.5	72.8	-	dB
Total Harmonic Distortion		THD	-	-	0.01	-	-	0.01	%
Spurious-Free-Dynamic-Range	(Note 5)	SFDR	- -80	- -	0.01 -	- -80	- -	0.01 -	% dB_C
Intermodulation Distortion Second Order Third Order	(Note 6)	IMD	 -80 -80	 - -	 - -	 -80 -80	 - -	 - -	 dB_C dB_C
Analog Input									
Input Voltage Range		AIN	-2.5	-	+2.5	-2.5	-	+2.5	V
Aperture Delay		t_{apd}	-	-	25	-	-	25	ns
Aperture Jitter		t_{apj}	-	-	100	-	-	100	ps
Input Capacitance		A_{cin}	-	-	10	-	-	10	pF

Notes:
1. All parameters are guaranteed by design, test, and/or characterization.
2. Measured with respect to internal reference and includes bipolar offset error.
3. $A_{IN} = \pm 2.5V_{pp}$
4. A_{IN} = 10kHz Sine Wave, f_{SAMPLE} = 500kSPS. Typically 71.5dB for 10kHz<A_{IN}<250kHz.
5. A_{IN} = 10kHz Sine Wave, f_{SAMPLE} = 500kSPS. Typically -80dB for 0<A_{IN}<250kHz.
6. fa = 9kHz, fb = 9.8kHz, f_{SAMPLE} = 500kSPS.

* Parameter definitions are given at the end of this data sheet prior to the package outline information.

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	B Min	B Typ	B Max	T Min	T Typ	T Max	Units
Specified Temperature Range		-40 to +85			-55 to +125			°C
Reference Output								
Output Voltage	V_R	2.49	-	2.51	2.49	-	2.51	V
REF OUT Tempco		-	60	-	-	60	-	ppm/°C
Load Regulation (Note 7)	$\Delta VR/\Delta I$	-	0.6	1	-	0.6	1	mV
Output Noise Voltage	e_N	-	100	-	-	100	-	μV_{rms}
Output Current Drive								
Source Current	I_{SOURCE}	-	500	-	-	500	-	µA
Sink Current	I_{SINK}	-	100	-	-	100	-	µA
Conversion & Throughput								
Conversion Time	tconv							MMC*
External Clock ($CLKIN$ = 10MHz)		-	-	1.6	-	-	1.6	µs
Internal Clock		1.4	-	1.8	1.4	-	1.8	
Acquisition Time	t_{acq}	-	-	0.4	-	-	0.4-	µs
Throughput	ftp	500	-	-	500	-	-	kSPS
Power Supplies								
Positive Supply Current	I_{A+}	-	9.5	10.0	-	9.5	10.0	mA
Negative Supply Current	I_{A-}	-	7.0	10.0	-	7.0	10.0	mA
Power Dissipation	P_D	-	85	100	-	85	100	mW

Note: 7. Reference Load Current Change (0-500 µA). Reference Load should not be changed during conversion

LSB	%FS	ppm FS	mV
0.25	.0061	61	0.31
0.50	.0122	122	0.61
1.00	.0244	244	1.22
2.00	.0488	488	2.44
4.00	.0976	976	4.88

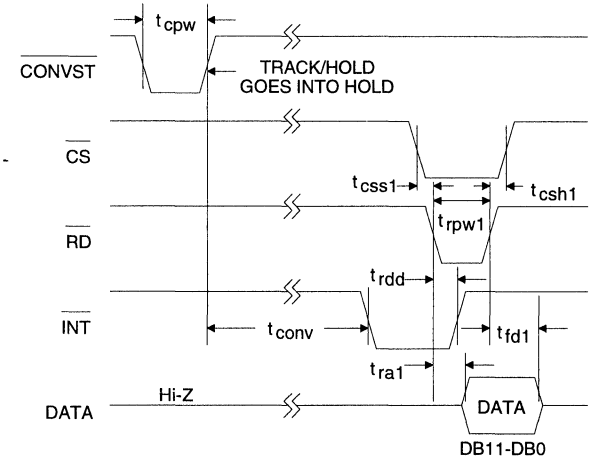
Unit Conversion Factors: VIN = ±2.5V

SWITCHING CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+ = +5V±5%, VA- = -5V±5%; AGND = DGND = 0V, (Note 8)

Parameter		Symbol	B Min	B Typ	B Max	T Min	T Typ	T Max	Units
Specified Temperature Range			-40 to +85			-55 to +125			°C
CLKIN	Period	t_{clk}	100	-	400	100	-	400	
CLKIN	Low Time	t_{clkl}	0.4	-	0.6	0.4	-	0.6	MMC*
CLKIN	High Time	t_{clkh}	0.4	-	0.6	0.4	-	0.6	ns
Rise Times	Any Digital Input	t_{rise}	-	-	20	-	-	20	ns
	Any Digital Output	t_{rise}	-	20	-	-	20	-	
Fall Times	Any Digital Input	t_{fall}	-	-	20	-	-	20	ns
	Any Digital Output	t_{fall}	-	20	-	-	20	-	ns
Mode 1 Timing									
Conversion Time		t_{conv}	-	-	16	-	-	16	ns
CONVST Pulse Width		t_{cpw}	50	-	-	50	-	-	
$\overline{CS}$ Active to $\overline{RD}$ Active		t_{css1}	0	-	-	0	-	-	
$\overline{RD}$ Pulse Width		t_{rpw1}	60	-	-	75	-	-	
$\overline{RD}$ Inactive to $\overline{CS}$ Inactive		t_{csh1}	0	-	-	0	-	-	
$\overline{RD}$ Active to $\overline{INT}$ Inactive		t_{rdd}	-	-	70	-	-	70	ns
Data Access Time after $\overline{RD}$	(Note 9)	t_{ra1}	-	-	57	-	-	70	
Output Float Delay: $\overline{RD}$ Rising to Hi-Z	(Note 10)	t_{fd1}	5	-	50	5	-	50	ns
HBEN to $\overline{RD}$ Active		t_{hrs}	0	-	-	0	-	-	ns
$\overline{RD}$ Inactive to HBEN Hold Time		t_{hrh}	0	-	-	0	-	-	
Serial Clock Timing									
SCLK to $\overline{SSTRB}$ Falling Time	(Note 11)	t_{ss}	25	-	25	25	-	-	
Serial Clock	Pulse Width High	t_{pwh}	0.4	-	0.6	0.4	-	0.6	MCC*
	Pulse Width Low	t_{pwl}	0.4	-	0.6	0.4	-	0.6	MCC*
SCLK rising to Data Valid	(Note 12)	t_{ssl}	-	-	30	-	-	30	ns
SCLK rising to $\overline{SSTRB}$ Inactive		t_{ssrl}	10	-	25	10	-	25	ns
SCLK rising to SDATA Hold Time		t_{sh}	10	-	25	10	-	25	ns

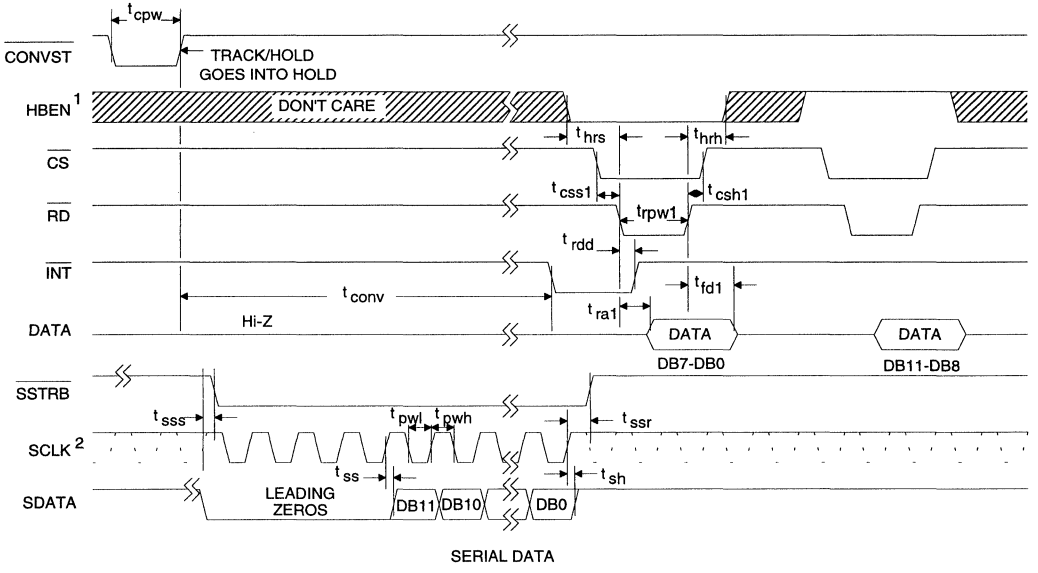
MCC = Master Clock Cycles, 1 MCC = t_{clk}

Notes:
8. All input signals are specified with $t_{rise} = t_{fall}$ = 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.
9. Measured with the load circuits of Figure 5 and defined as the time required for an output to cross 0.8V or 2.4V.
10. Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 6.
11. t_{sss} = MCC/2 - 25ns. t_{sss} = 25ns for t_{clk} = 100ns.
12. CL = 35pF. SDATA will drive higher capacitive loads but this will add to tss.



NOTE: FORMAT = +5V

Figure 1. Mode 1 Timing Diagram, 12-Bit Parallel Read



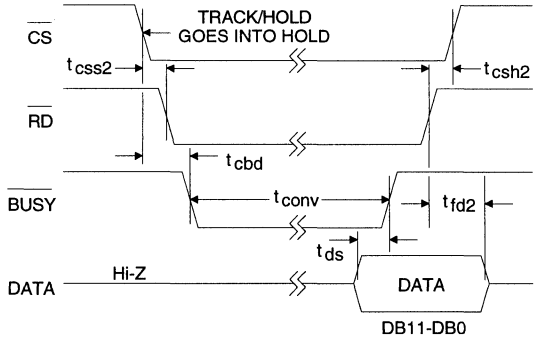
NOTES: 1. Times t_{css1}, t_{rpw1}, t_{csh1} and t_{hrh} are the same for a high byte read as for a low byte read.
2. Continuous SCLK(Dashed line) when FORMAT = -5V
Noncontinuous when FORMAT = 0V.

Figure 2. Mode 1 Timing Diagram, Byte or Serial Read

SWITCHING CHARACTERISTICS (Continued)

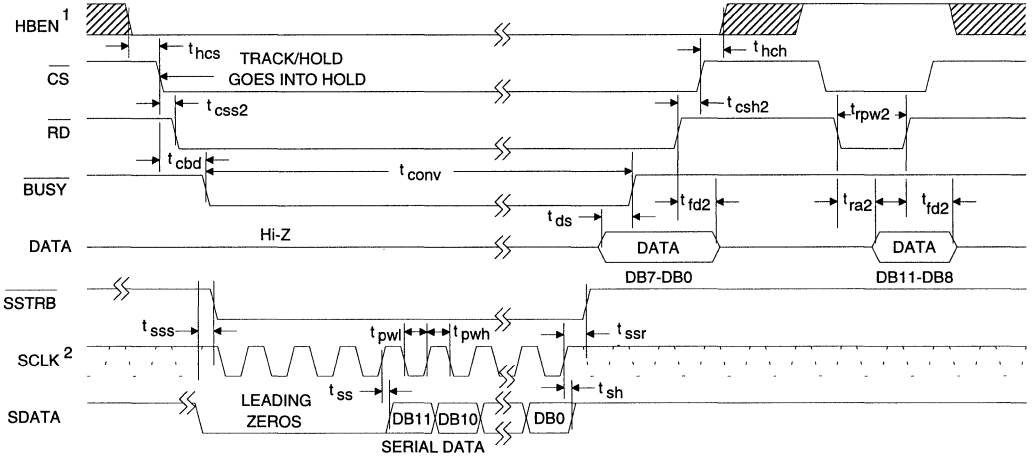
Parameter	Symbol	B Min	B Typ	B Max	T Min	T Typ	T Max	Units
Specified Temperature Range		-40 to +85			-55 to +125			°C
Mode 2 Timing								
Conversion Time	t_{conv}	-	-	16	-	-	16	MMC*
$\overline{CS}$ Active to $\overline{RD}$ Active	t_{css2}	10	-	-	10	-	-	ns
$\overline{CS}$ Active to $\overline{BUSY}$ Active	t_{cbd}	-	-	75	-	-	75	ns
Data Setup Time to $\overline{BUSY}$ Inactive	t_{ds}	50	-	-	50	-	-	ns
$\overline{RD}$ Inactive to $\overline{CS}$ Inactive	t_{csh2}	0	-	-	0-	-	-	ns
Output Float Delay: $\overline{RD}$ Rising to Hi-Z	t_{fd2}	5	-	50	5	-	50	ns
HBEN Low to $\overline{CS}$ Active Setup Time	t_{hcs}	0	-	-	0-	-	-	ns
$\overline{CS}$ Inactive to HBEN Hold Time	t_{hch}	0	-	-	0	-	-	ns
$\overline{RD}$ Pulse Width	t_{rpw2}	60	-	-	75	-	-	ns
Data Access Time After $\overline{RD}$ (Note 10)	t_{ra2}	-	-	57	-	-	70	ns
Serial Clock Timing								
Serial Clock Pulse Width High	t_{pwh}	0.4	-	0.6	0.4	-	0.6	MCC*
Pulse Width Low	t_{pwl}	0.4	-	0.6	0.4	-	0.6	MCC*
SCLK to $\overline{SSTRB}$ Falling Time (Note 12)	t_{sss}	25	-	-	25	-	-	ns
SCLK rising to Data Valid (Note 13)	t_{ss}	-	-	30	-	-	30	ns
SCLK rising to $\overline{SSTRB}$ Inactive	t_{ssr}	10	-	25	10	-	25	ns
SCLK rising to SDATA Hold Time	t_{sh}	10	-	25	10	-	25	ns

*MCC = Master Clock Cycles, 1 MCC = t_{clk}



NOTE: FORMAT = +5V.

Figure 3. Mode 2 Timing Diagram, 12-Bit Parallel Read



NOTES: 1.Times t_{hcs}, t_{css2}, t_{csh2} and t_{hch} are the same for a high byte read as for a low byte read.
2. Continuous SCLK(Dashed line) when FORMAT = -5V
Noncontinuous when FORMAT = 0V.

Figure 4. Mode 2 Timing Diagram, Byte or Serial Read

DIGITAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}: VA+ = +5V±5%; VA- = -5V±5%)

Parameter		Symbol	Min	Typ	Max	Units
Logic Inputs						
High-level Input Voltage		V_{IH}	3.3			V
Low-level Input Voltage		V_{IL}			0.8	V
Input leakage current		I_{in}			50	µA
Input Capacitance		C_{in}			10	pF
Logic Outputs						
High-level Output Voltage	(Note 13)	V_{OH}	4.0			V
Low-level Output Voltage	(Note 14)	V_{OL}			0.4	V
DB11-DB0 Floating State leakage Current		I_{OZ}			10	µA
DB11-DB0 Output Capacitance		C_{out}			15	pF

Notes: 13. I_{source} = -40µA
14. I_{sink} = 1.6 mA

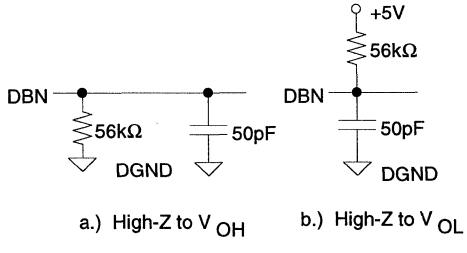


Figure 5. Load Circuits for Access Time

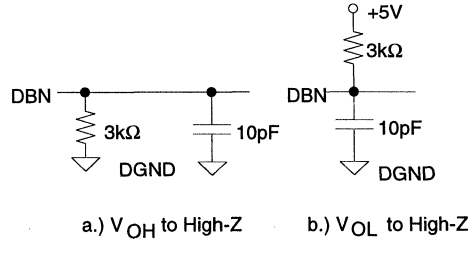


Figure 6. Load Circuits for Output Float Delay

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V. All voltages with respect to ground)

Parameter	Symbol	Min	Typ	Max	Units
Positive Analog Supply	VA+	4.75	5.0	5.25	V
Negative Analog Supply	VA-	4.75	5.0	5.25	V
Analog Input Voltage	A_{in}	-2.5		+2.5	V
FORMAT Input Voltage Range		VA-, 0V, VA+			V
CLKIN Input Voltage Range		0		VA+	V
Other Digital Input Voltage Ranges		0		VA+	V
External Clock Frequency			10		MHz
External Clock Jitter				65	ps
AGND to DGND Voltage Differential				10	mV

ABSOLUTE MAXIMUM RATINGS (AGND = 0V, All voltages with respect to ground)

Parameter	Symbol	Min	Typ	Max	Units
Positive Analog Supply	VA+	-0.3		6.0	V
Negative Analog Supply	VA-	0.3		6.0	V
Analog Input Voltage	A_{in}	(VA-)-0.3		(VA+)+0.3	V
FORMAT Input Voltage Range		(VA-)-0.3		(VA+)+0.3	V
CLKIN Input Voltage Range		(VA-)-0.3		(VA+)+0.3	V
Other Digital Input Voltage Ranges		(VA-)-0.3		(VA+)+0.3	V
REF OUT Current				10	mA
Sustained Digital Output Current				5	mA
AGND to DGND Voltage Differential				100	mV
Operating Temperature Range CS5032-BP/BS CS5032-TD		 -40 -55		 +85 +125	 °C
Storage Temperature Range		-65		+150	°C
Lead Solder Temperature				+300	°C

* WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes

GENERAL DESCRIPTION

The CS5032 is a complete 12-bit 500 kSPS sampling ADC utilizing a successive approximation architecture. Factory calibration ensures 12-bit conversion accuracy over industrial and military temperature ranges. The analog input range is ±2.5 V, with the output data provided in parallel, byte or serial formats. The internal capacitor array DAC acts as an inherent sample-and-hold, and forms the heart of the CS5032. The on-chip +2.5 V reference is available at the REFOUT pin. Additionally, an on-chip 10 MHz clock oscillator can be used to control converter operations.

OPERATIONAL OVERVIEW

Track-and-Hold Operation

Track-and-hold operation within the CS5032 is transparent to the user. The capacitor array DAC acts as the hold capacitor. During tracking mode all elements of the capacitor array DAC are switched to the analog input for charging. The load capacitance of the entire array during tracking mode is typically 5 pF. The input bandwidth of the track-and-hold is typically 2 MHz. The ADC goes into hold mode on the rising edge of $\overline{\text{CONVST}}$.

Capacitor Array DAC Calibration

To achieve 12-bit accuracy from the capacitor array DAC, the CS5032 uses a novel calibration scheme. Each bit capacitor consists of several capacitors that are trimmed to optimize the overall bit weighting with an internal resolution of 14-bits, resulting in nearly ideal differential and integral linearity.

The calibration coefficients for the capacitive bit weights are stored in an on-chip EEPROM during the factory calibration. When the converter is subsequently powered-up these coefficients are applied to the capacitor array DAC. The low temperature coefficient of the capacitor array easily maintains 12-bit accuracy over the full temperature range without recalibration.

Reference Operation

The reference voltage is available at the REF OUT pin and is capable of sourcing 500 µA to peripheral devices. This pin must be decoupled with a parallel combination of a +10 µF tantalum capacitor and a 0.1 µF ceramic capacitor. The reference voltage is calibrated on power-up, with full accuracy achieved after 1.1 sec.

Analog Input

The CS5032 provides a ±2.5 V analog input voltage range. The equivalent analog input circuit is illustrated in Figure 7 (shown in track mode). During hold mode the input impedance to the device is typically 10 MΩ, and the various elements of the capacitor array DAC are connected to either AGND or VREF. In switching back from hold mode to track mode, some elements in the capacitor array must be charged by the analog input. For the CS5032, the worst case charging current occurs when the analog input changes from +2.5 V to -2.5 V.

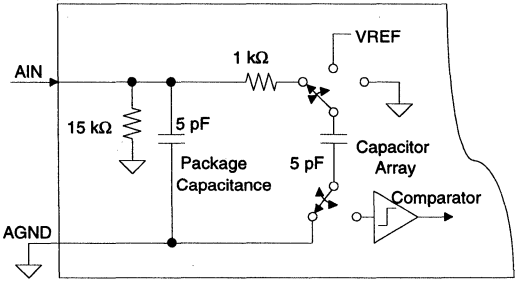


Figure 7. Analog Input Model.

To ensure that the capacitor array DAC has settled to within 0.25 LSB during the allowed acquisition time, the external source resistance should be less than 4 kΩ.

Output Coding

The digital output coding is 2's complement.

Input Level	2's Complement Output
+2.5 V	0111 1111 1111
0 V	0000 0000 0000
-2.5 V	1000 0000 0000

High-Speed System Clock

The CS5032 employs a high-speed clock (typically 10 MHz) to control internal operations. This high-speed clock can be generated internally with the on-chip oscillator, or it can be supplied from an external CMOS source. Connecting a CMOS clock signal to the CLKIN pin allows the converter to operate from an external clock. Alternatively, connecting the CLKIN pin to VA- activates the internal clock oscillator.

External Clock.....CLKIN = External Clock Source
Internal Clock.....CLKIN = VA-

CONVERT Clock Considerations

When digitizing time varying signals, it is possible to create additional noise sources over and above those resulting from quantization noise and thermal noise. This is particularly true when high-speed conversion rates, or high-frequency analog input frequencies are involved. Special care must be taken to see that $\overline{\text{CONVST}}$ clock jitter does not undermine high-speed signal processing applications by introducing noise into the conversion process.

Simple quantization noise is a direct result of the finite LSB size, which is itself related to the number of digital output bits. Quantization noise places a hard limit on SNR for a 12-Bit ADC according to the following equation.

$$SNR_{MAXQuantization} = (6.02dB)(\#\ of\ Bits) + 1.76dB$$

$$\therefore\ SNR_{MAXQuantization} = 74\ dB$$

Although SNR can never be better than the theoretical limit, it can certainly be worse. Jitter between the $\overline{\text{CONVST}}$ clock and the analog input signal is often one of the largest contributors to decreased SNR, particularly as frequencies increase.

To be considered insignificant, noise related to jitter ($SNR_{MAXjitter}$) should be at least 12 dB below the other dominant noise sources, such as quantization noise ($SNR_{MAXQuantization}$). The 12 dB target is somewhat arbitrary, but yield less than 4 % additional noise. In terms of the CS5032, a 250 kHz analog input signal requires less than 80 ps of jitter between the $\overline{\text{CONVST}}$ clock and the analog input signal to achieve full performance. The use of low-jitter $\overline{\text{CONVST}}$ clock source is the most common means of reducing the effects of jitter. Lower conversion rates and lower analog input frequencies are significantly less sensitive to jitter effects.

Digital Output Formats

The CS5032 provides three digital output formats. These include 12-bit parallel, two 8-bit bytes, and a serial output mode. The output data

$$SNR_{MAX} = \sqrt{SNR_{MAXjitter}^{2} + SNR_{MAXQuantization}^{2}}$$

$$SNR_{MAXjitter}\ (dB) = 20\ Log\left[\frac{1}{2\pi f_{IN}\ jitter_{RMS}}\right]$$

$$jitter_{RMS} = \sqrt{clock\ jitter_{RMS}^{2} + analog\ jitter_{RMS}^{2}}$$

format is controlled by the level applied to the FORMAT pin. All three of the digital output formats can be used with either of the convert start timing modes ... Mode 1 and Mode 2, which are described in the next two sections.

FORMAT	Digital Outputs
+VA	12-Bit Parallel
GND	Byte; Serial w/Non-Continuous SCLK
-VA	Byte; Serial w/Continuous SCLK

Figure 8 shows the schematic for the CS5032 in 12-bit parallel mode. The twelve bits of data are output simultaneously on DB11/(MSB) through DB0 (LSB).

In byte mode, two 8-bit read operations (four leading zeros with 4 data bits ... plus 8 more data bits) are required to collect the data as shown in Figure 9. In byte mode, the DB11/HBEN pin defers to the HBEN function, selecting the high or low byte of data to be read from the ADC. The lower eight bits of data are placed on the data bus when HBEN is held low. To access the four MSBs of data, HBEN must be held high. The 4 MSBs of the 12-bit data word are right justified with zeros in the upper nibble of the high byte.

In serial mode, DB8/SDATA, DB9/SCLK and DB10/$\overline{\text{SSTRB}}$ defer to their serial functions. The serial strobe pin $\overline{\text{SSTRB}}$ provides a framing sig-

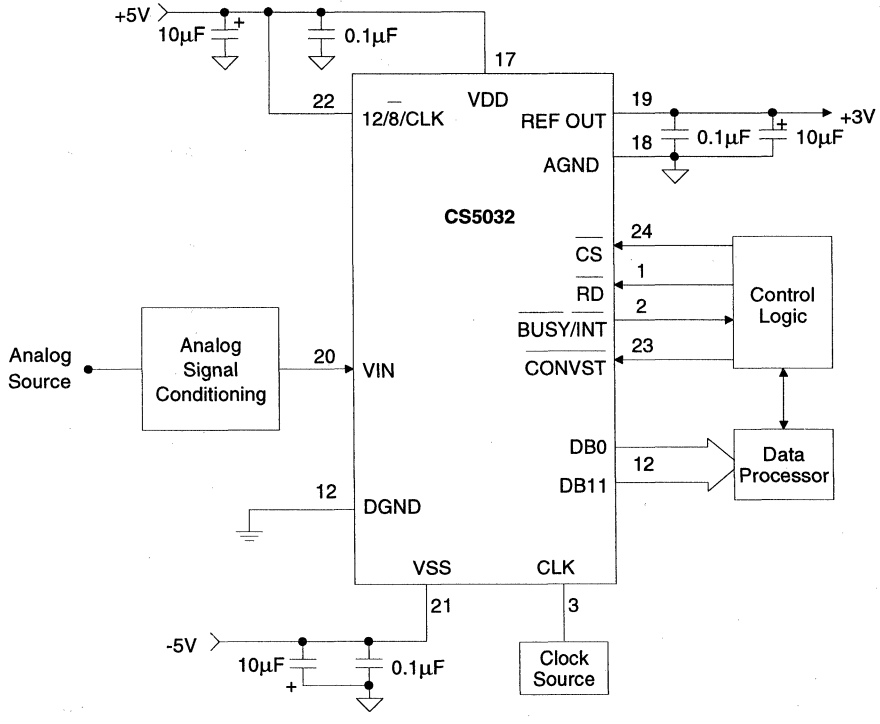


Figure 8. System Connection Diagram: Parallel Data Format

nal for serial data. Serial data is available at the SDATA pin when $\overline{SSTRB}$ falls low. $\overline{SSTRB}$ falls low within three clock cycles of $\overline{CONVST}$. A total of sixteen bits (four leading zeros and twelve data bits starting with the MSB) are clocked out on the SDATA pin on the rising edge of SCLK. The data bits become valid no more than t_{ss} after the rising edge of SCLK. $\overline{SSTRB}$ goes low during data transmission and automatically returns high when the LSB has been clocked out on the SDATA line. For serial operation, 0V on the FORMAT pin causes the serial clock to run only when data is being clocked out of the device; SCLK goes high after data transmission is completed. If the FORMAT is connected to -VA, the SCLK output will run continuously, independent of data transmission. Serial data operation is identical for MODE 1 and MODE 2 timing control (see next two sections).

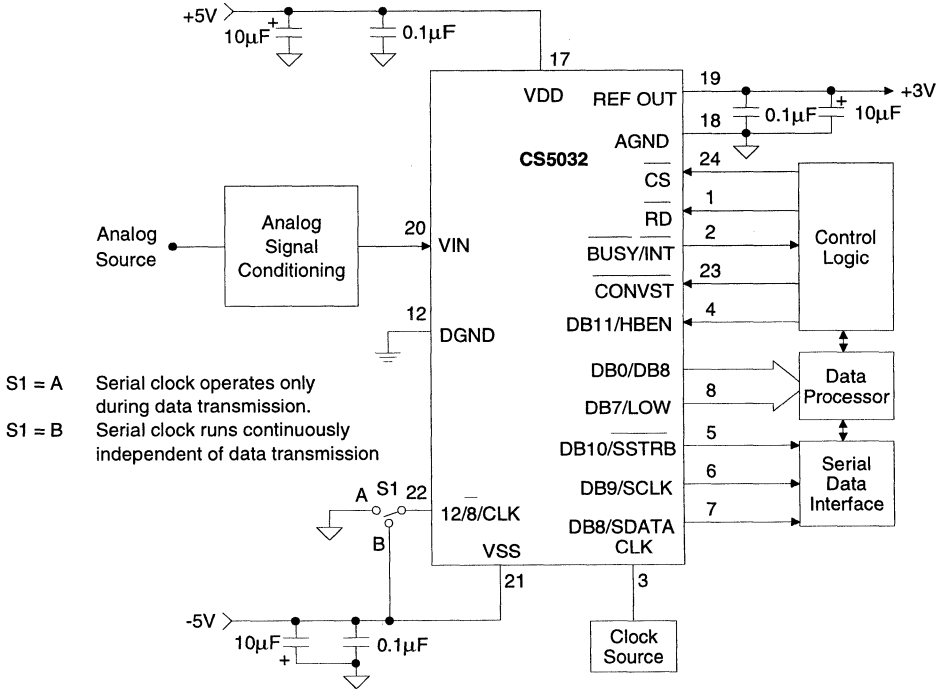


Figure 9. System Connection Diagram: Serial and Byte Data format

MODE 1 Operation

The rising edge of $\overline{\text{CONVST}}$ signal is used to put the device into hold mode and initiate a conversion. At the end of conversion the device returns to it's tracking mode. MODE 1 timing is primarily used in DSP type applications where precise control of $\overline{\text{CONVST}}$ timing is required.

Conversion begins on the rising edge of $\overline{\text{CONVST}}$ provided that $\overline{\text{CS}}$ is high. The $\overline{\text{BUSY/INT}}$ line performs the $\overline{\text{INT}}$ function and can be used to interrupt the microprocessor. $\overline{\text{INT}}$ is normally high and goes low at the end of conversion. The ADC returns to track mode when $\overline{\text{INT}}$ goes low. Bringing $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low allows data to be read from the ADC, and also resets $\overline{\text{INT}}$ high. $\overline{\text{CONVST}}$ must be high when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are brought low for the ADC to operate correctly in this mode. Data cannot be read during a conversion cycle because the output data latches are disabled while a conversion is in progress.

MODE 1 - 12-Bit Parallel Read

Figure 10 shows the MODE 1 timing diagram for 12-bit parallel operation (FORMAT = +VA). A data read operation performed at the end of conversion will read all twelve bits of data at the same time.

MODE 1 - Byte Read

Figure 11 shows the MODE 1 timing diagram for byte operation. At the end of conversion when INT goes low, either the low byte or the high byte of data can be read, depending on the status of HBEN. Bringing $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low allows data to be read from the ADC and also resets $\overline{\text{INT}}$ high.

MODE 1 - Serial Read

The MODE 1 timing diagram for serial operation is shown in Figure 12. Conversion begins on the rising edge of $\overline{\text{CONVST}}$, and data is clocked out on SDATA immediately upon the falling edge of $\overline{\text{SSTRB}}$. The data is output as four leading zeroes followed by the twelve data bits with the MSB first. The first zero should be latched into the external receiving circuitry on the first falling edge of SCLK after $\overline{\text{SSTRB}}$ goes low. A total of sixteen falling SCLK edges will latch all sixteen bits of output data. $\overline{\text{SSTRB}}$ automatically returns high after the last bit of data has been clocked out of the device.

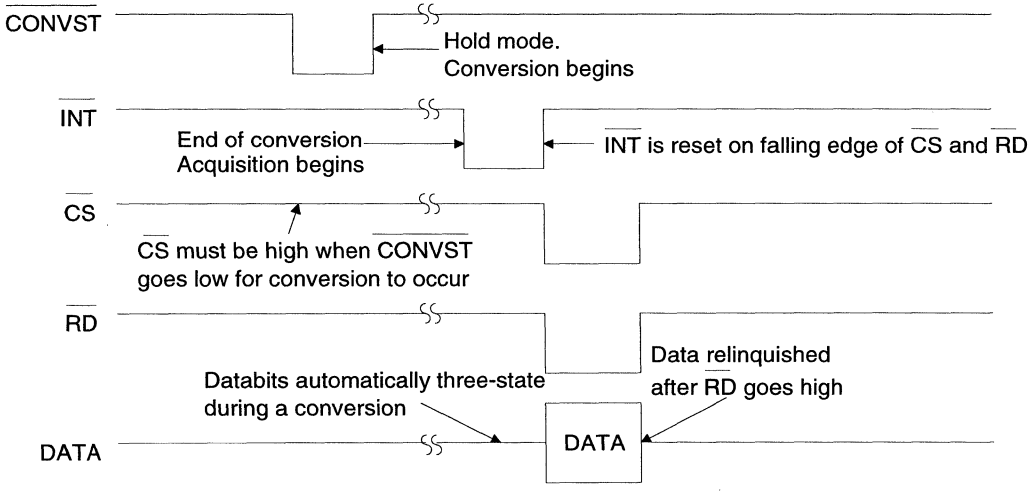
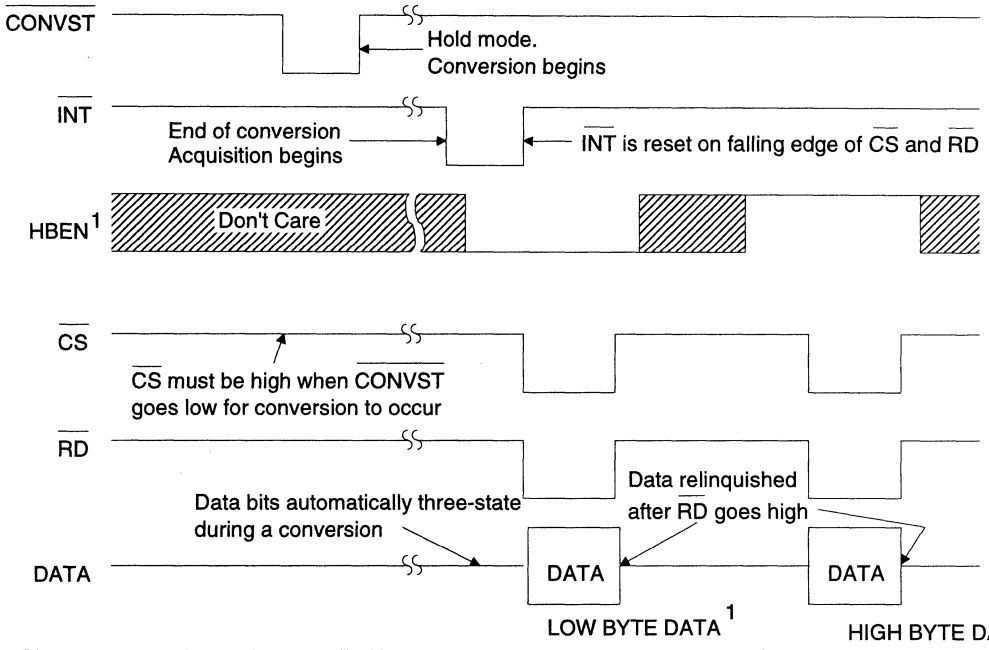


Figure 10. Mode 1 Timing Diagram, 12-bit Parallel Read



NOTES: 1. In the above diagram HBEN is exercised to read the low byte first (DB7-DB0) and then the high byte (DB11-DB8). To change the order in which the bytes are read, simply invert the HBEN signal shown above.

Figure 11. Mode 1 Timing Diagram, Byte Read

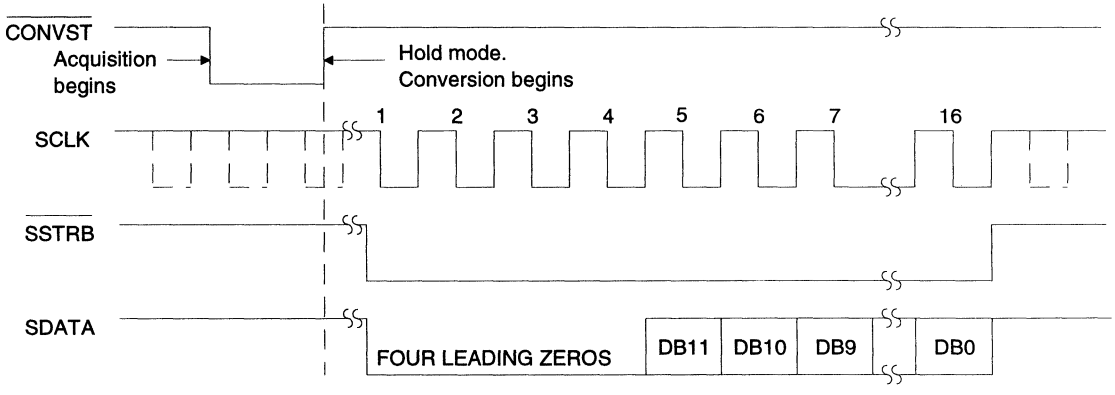


Figure 12. Mode 1 Timing Diagram - Serial Read

MODE 2 Operation

Mode 2 operation allows the ADC conversion to be initiated by a read operation from a µC. The $\overline{BUSY}$ signal can be used in this mode to halt µC operations by placing the µC in a WAIT state until the conversion is complete. This avoids having to handle interrupts and timing delays, assuring that the conversion cycle is complete before any attempted data read.

In this mode, $\overline{CONVST}$ must be held permanently low. Bringing $\overline{CS}$ low (while $\overline{HBEN}$ is low) puts the device into hold mode and initiates a conversion. The $\overline{BUSY}/\overline{INT}$ pin defers to the $\overline{BUSY}$ function such that $\overline{BUSY}$ goes low at the start of conversion and returns high at the end of conversion.

MODE 2 - 12-Bit Parallel Read

The MODE 2 timing diagrams for the parallel data output format are shown in Figure 13. This mode of operation forces the µC into a WAIT state until the conversion has been completed. It removes the risk of inadvertently reading invalid data before the conversion cycle has been completed.

MODE 2 - Byte Read

Figure 14 shows the timing diagram for byte operation in MODE 2. Since $\overline{HBEN}$ must be low to initiate a conversion, the lower byte of data will be accessed first during the two-byte read operation. This is followed by a second byte read operation (with $\overline{HBEN}$ high) to complete the data transfer.

MODE 2 - Serial Read

The timing diagram for MODE 2 serial operation is shown in Figure 15. The device goes into hold mode on the falling edge of $\overline{CS}$ and conversion begins when $\overline{BUSY}$ goes low. The data is clocked out similarly as for MODE 1 serial operation. Upon clocking of the final data bit $\overline{BUSY}$ returns high indicating end of conversion.

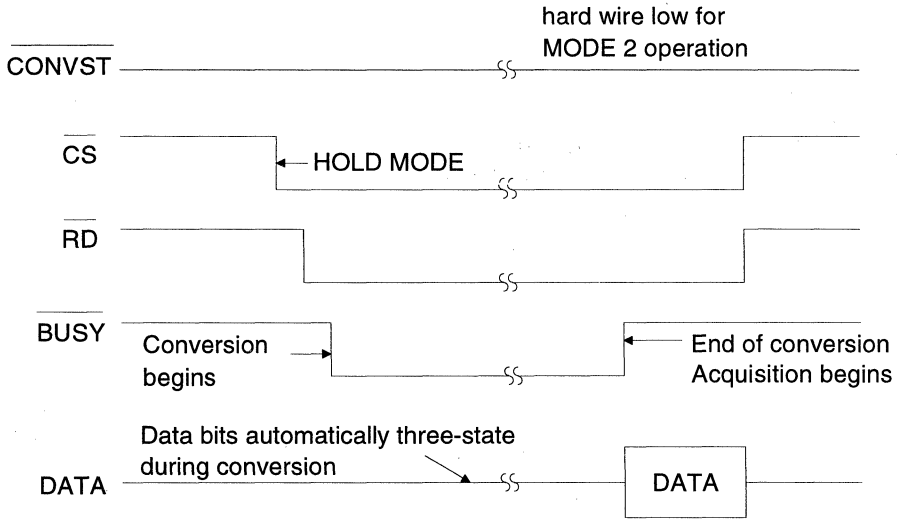


Figure 13. Mode 2 Timing Diagram, 12-bit Parallel Read

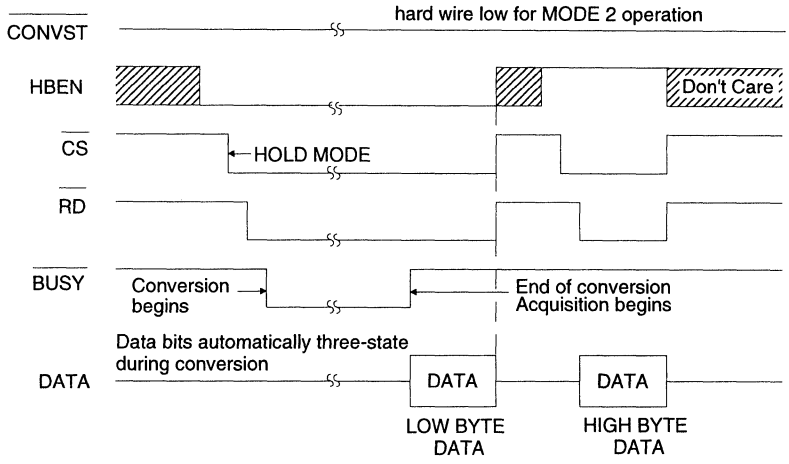


Figure 14. Mode 2 Timing Diagram, Byte Read

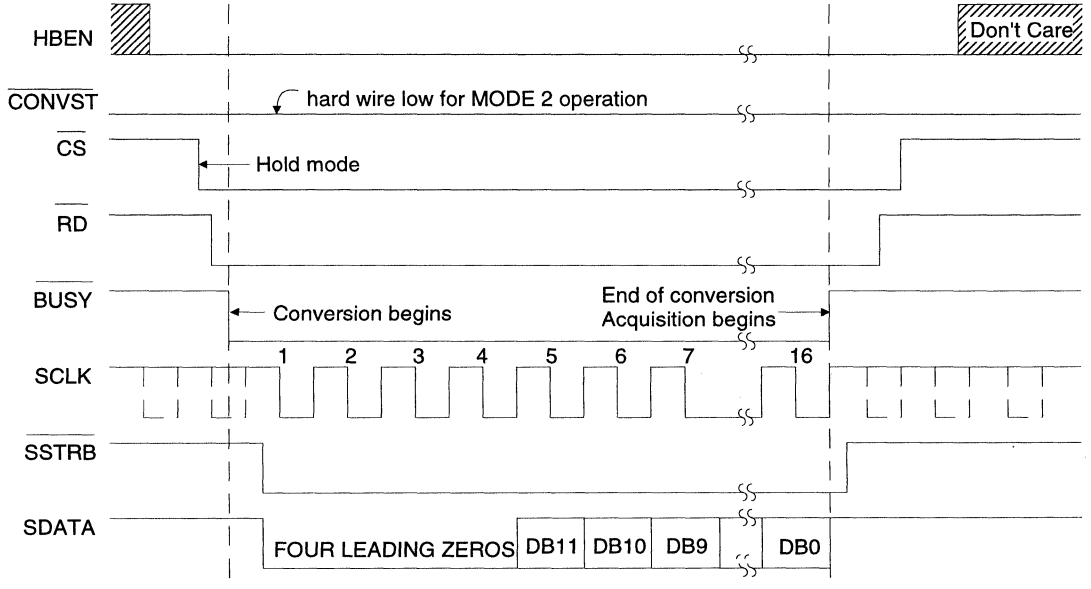


Figure 15. Mode 2 Timing Diagram, Serial Read

STAND-ALONE OPERATION

The CS5032 supports stand-alone conversion when used in MODE 2 parallel interface operation as shown in Figure 16. Conversion is initiated by pulse to the $\overline{CS}$ input of the ADC. The duration of the pulse must be longer than the ADC conversion time. The $\overline{BUSY}$ output drives the $\overline{RD}$ input and data is latched on the rising edge of $\overline{BUSY}$ to an external latch.

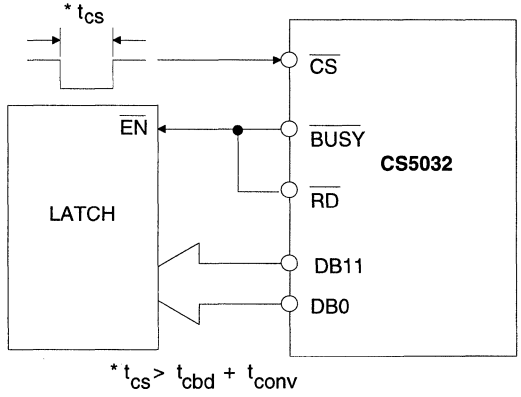


Figure 16. Stand-Alone Operation

Power Supplies, AGND, and DGND

Figure 8 illustrates the recommended power supply decoupling scheme with a 0.1 µF ceramic and a +10 µF tantalum capacitor for both the VA+ and the VA- pins. The capacitors should be located as close as practical to the supply pins. AGND is the power supply current return, and is also the preferred ground reference for the decoupling capacitors.

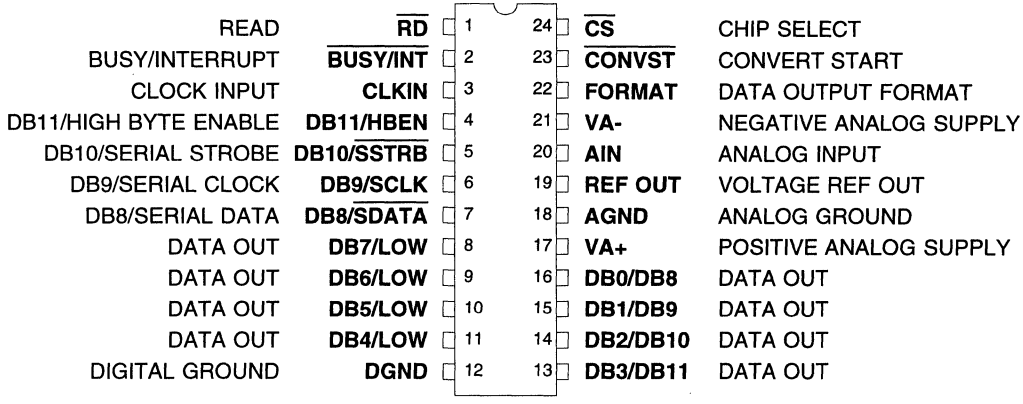
Typically a low-impedance ground plane is used around and under the ADC, with connections to both AGND and DGND. If a split ground is used, DGND is the ground reference for any digital circuits that follow the CS5032. When split grounds are used, the AGND to DGND voltage differential should be kept below ±10 mV for best operation.

If the power supply voltage is dropped below 3 V, the ADC may need to be reset by switching power off and then back on.

Layout considerations

The CS5032 is a high-speed component which requires adherence to standard high-frequency printed circuit board layout techniques to maintain optimum performance. These include proper supply decoupling, minimum length circuit traces, and physical separation of digital and analog components and circuit traces. See the CDB5032 evaluation board data sheet for more details.

PIN DESCRIPTIONS



Pinout applies to both DIP and SOIC packages.

Power Supply Connections

VA+ – Positive Supply, PIN 17.
+5V±5%.

VA- – Negative Supply, PIN 21.
-5V±5%.

DGND – Digital Ground, PIN 12.
Ground reference for digital circuitry.

AGND – Analog Ground, PIN 18.
Ground reference for track-and-hold, reference and DAC.

Oscillator

CLKIN – Clock Input, PIN 3.
An external 10MHz (CMOS compatible) clock is applied at this pin. Connecting this pin to VA- enables the internal clock oscillator.

Digital Inputs

$\overline{CS}$ – Chip Select, PIN 24.
Active low logic input. The device is selected when this input is active. With $\overline{CONVST}$ tied low, a new conversion is initiated when $\overline{CS}$ goes low.

$\overline{RD}$ – Read, PIN 1.

Active low logic input. This input is used in conjunction with $\overline{CS}$ low to enable the data outputs.

FORMAT – Output Mode Selection, PIN 22.

Defines the output data format and serial clock format. With FORMAT at +5V, the output data format is 12-bit parallel only. With FORMAT at 0V, either byte or serial data is available and SCLK is not continuous. With FORMAT at -5V, byte or serial data is again available but SCLK is now continuous.

$\overline{CONVST}$ – Convert Start, PIN 23.

A low to high transition on this input puts the track-and-hold into its hold mode and starts conversion. This input is asynchronous to the CLKIN and independent of $\overline{CS}$ and $\overline{RD}$.

Digital Outputs

$\overline{BUSY}/\overline{INT}$ – Busy/Interrupt, PIN 2.

Active low logic output indicating converter status. See timing diagrams.

DB11/HBEN – Data Bit 11/High Byte Enable, PIN 4.

The function of this pin is dependent on the state of the FORMAT input (see above). When 12-bit parallel data is selected, this pin provides the DB11 output. When byte data is selected, this pin becomes the HBEN logic input. HBEN is used for 8-bit bus interfacing. When HBEN is low, DB7/LOW to DB0/DB8 become DB7 to DB0. With HBEN high, DB7/LOW to DB0/DB8 are used for the upper byte of data (see Table 1).

DB10/$\overline{SSTRB}$ – Data Bit 10/Serial Strobe, PIN 5.

The function of this pin is dependent on the state of the FORMAT input (see above). When 12-bit parallel data is selected, this pin provides the DB10 output. If FORMAT is at either 0V or -5V, $\overline{SSTRB}$ provides a strobe or framing pulse for serial data.

DB9/SCLK – Data Bit 9/Serial Clock, PIN 6.

The function of this pin is dependent on the state of the FORMAT input (see above). When 12-bit parallel data is selected, this pin provides the DB9 output. SCLK is the gated serial clock output derived from the internal or external ADC clock. If FORMAT is at -5V, then SCLK runs continuously. If FORMAT is at 0V, then SCLK goes high after serial transmission is complete.

DB8/SDATA – Data Bit 8/Serial Data, PIN 7.

The function of this pin is dependent on the state of the FORMAT input (see above). When 12-bit parallel data is selected, this pin provides the DB8 output. SDATA is used with SCLK and $\overline{SSTRB}$ for serial data transfer. Serial data is valid on the falling edge of SCLK while $\overline{SSTRB}$ is low.

DB7/LOW, DB6/LOW, DB5/LOW, DB4/LOW – Three-state data outputs, PINS 8, 9, 10, 11.

The outputs of these pins are controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the FORMAT and HBEN inputs. With FORMAT high, they are always DB7-DB4. With FORMAT low or -5V, their function is controlled by HBEN (see Table 1).

DB3/DB11, DB2/DB10, DB1/DB9, DB0/DB8 – Three-state data outputs, PINS 13, 14, 15, 16.

The outputs of these pins are controlled by $\overline{CS}$ and $\overline{RD}$. Their function depends on the FORMAT and HBEN inputs. With FORMAT high, they are always DB3-DB0. With FORMAT low or -5V, their function is controlled by HBEN (see Table 1).

HBEN	DB7/LOW	DB6/LOW	DB5/LOW	DB4/LOW	DB3/DB11	DB2/DB10	DB1/DB9	DB0/DB8
HIGH	LOW	LOW	LOW	LOW	DB11/(MSB)	DB10	DB9	DB8
LOW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0/(LSB)

Table 1. Output Data for Byte Interfacing

Analog Output

REF OUT - Voltage Reference Output, PIN 19.

The internal 2.5V reference is provided at this pin. The external load capability is 500µA. This pin should be decoupled to AGND with a +10µF tantalum and a 0.1µF ceramic capacitor. The REF OUT voltage has a settling time of approximately 1.1 sec.

Analog Input

AIN - Analog Input, PIN 20.

The analog input range for the CS5032 is ±2.5V.

Ordering Guide

Model Number	Throughput (kSPS)	Input Range (V)	Linearity Error (LSB)	Temp. Range (°C)	Package
CS5032-BP	500	±2.5	±0.5	-40 to +85	24-Pin 0.3" PDIP
CS5032-BS	500	±2.5	±0.5	-40 to +85	24-Pin 0.3" SOIC
CS5032-TD	500	±2.5	±0.5	-55 to +125	24-Pin 0.3" CERDIP

PARAMETER DEFINITIONS

Integral Non-Linearity Error - INL

The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code.

REF OUT Tempco

REF OUT Tempco is the worst case slope that is calculated from the change in reference value at +25°C to the value at T_{MIN} or T_{MAX}

i.e. REF OUT Tempco = (V_{ref} @ 25°C - V_{ref} @ T_{MAX})/(T_{MAX} - 25°C) or

REF OUT Tempco = (V_{ref} @ 25°C - V_{ref} @ T_{MIN})/(25°C - T_{MIN}).

Differential Nonlinearity - DNL

The deviation of a code's width from the ideal. Units in LSBs.

Full-Scale Error - FSE_P

The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSB's.

Bipolar Offset - V_{BP}

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND). Units in LSB's.

Bipolar Negative Full-Scale Error - FSE_N

The deviation of the first code transition from the ideal. The ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSB's.

Spurious-Free-Dynamic-Range - SFDR

The ratio of the rms value of the signal, to the rms value of the next largest spectral component (excepting dc). This component is often an aliased harmonic. Units in percent and dBc (decibels relative to the carrier).

Total Harmonic Distortion - THD

The ratio of the rms sum of the significant (2^{nd} thru 5^{th}) harmonics, to the rms value of the signal. Units in percent.

Signal-to-Noise-and-Distortion (s/n) - SNR

The ratio of the rms value of the signal, to the rms sum of all other spectral components (excepting dc and distortion terms). Expressed in decibels.

Signal-to-Noise-and-Distortion (s/[n+d]) - SINAD

The ratio of the rms value of the signal, to the rms sum of all other spectral components (excepting dc), including distortion components. Expressed in decibels.

Intermodulation Distortion - IMD

The ratio of the rms value of the larger of the two test frequencies, which are each 6dB down from full-scale, to the rms value of the largest 2^{nd} order and 3^{rd} order intermodulation component. Units in decibles relative to carrier.

Aperture Delay Time - t_{apd}

The time required, after the converter goes into hold mode, for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Unit in nanoseconds.

Aperture Jitter - t_{apj}

The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy.

$$SNR_{MAXjitter}\,(dB) = 20Log\left[\frac{1}{2\pi f_{IN}\,jitter_{RMS}}\right]$$

$$jitter_{RMS} = \sqrt{clock\,jitter_{RMS}^{\,2} + analog\,jitter_{\,RMS}^{\,2}}$$

To ensure that jitter does not affect the quantized signal quality, the jitter induced noise ($SNR_{MAXjitter}$) must be at least 12dB below other substantial noise sources, such as quantization noise, see *Clock Considerations*. Units in picoseconds.

Semiconductor Corporation

CDB5030 CDB5031 CDB5032

Evaluation Boards for CS5030, CS5031 & CS5032

Features

- Throughput rates up to 500kHz.
- Operation with on-board or off-board clocks.
- Buffered serial data, 12-bit parallel word, or two 8-bit bytes
- Digital and Analog Patch Areas
- CS5030 ±2.5V input
  CS5031 0V to +5V input
  CS5032 ±2.5V input

General Description

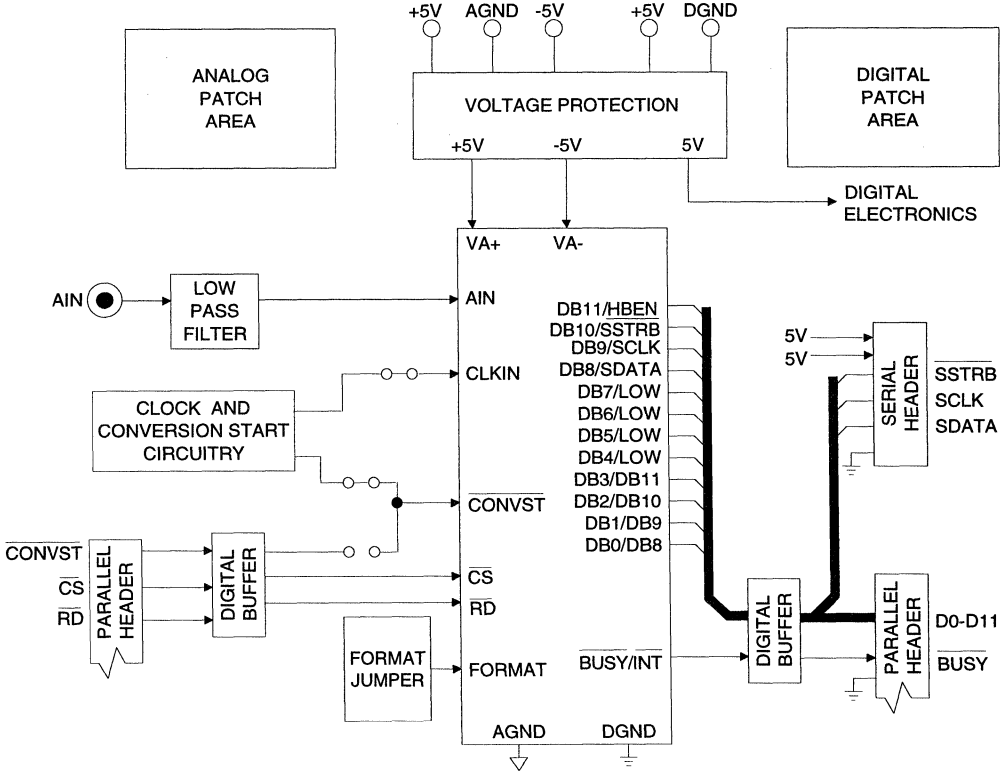
The CDB5030/31/32 Evaluation Boards allow fast evaluation of the CS5030, CS5031 & CS5032 12-bit, 500kHz, sampling A/D Converters.

The board provides a convenient platform for easy circuit development and evaluation. A versatile tool that can simplify design and reduce the design cycle resulting in a quicker time to market.

Analog input is via a BNC connector. Buffered digital outputs are available from the ADC in serial, 12-bit parallel word, or two 8-bit bytes formats.

Ordering Information

CDB5030 Evaluation Board with CS5030-BP Installed
CDB5031 Evaluation Board with CS5031-BP Installed
CDB5032 Evaluation Board with CS5032-BP Installed



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Introduction

The CDB5030, CDB5031, and CDB5032 evaluation boards provide a tool for testing and designing with the CS5030/1/2 series of A/D Converters. The boards are configured for operation from ±5V analog and +5V digital power supplies. A BNC connector is provided for the analog input signal. An on-board jumper selects the output data and serial clock formats. Parallel and serial connectors provide an interface to the digital logic.

Power Supplies

Figure 1 shows the power supply arrangements. ±5V is required to operate the ADC and analog portion of the board. Zener diodes are provided for over-voltage protection. A separate +5V digital supply is required for the digital logic. At least one individual decoupling capacitor is provided for each IC.

Analog Input Circuit

The analog input signal is brought on the evaluation board via the BNC connector J8 (figure 2). Diodes D1 and D2 provide protection against over voltage. R4 and C13 make a low pass filter, whose corner frequency is 318 kHz. Notice that no external trim components are required. R6 is a 10 kΩ terminating resister which provides a load for the signal source. R6 can be changed to match the analog input source impedance if required. The footprint is large enough to accommodate a 50 Ω, 0.5 W resistor.

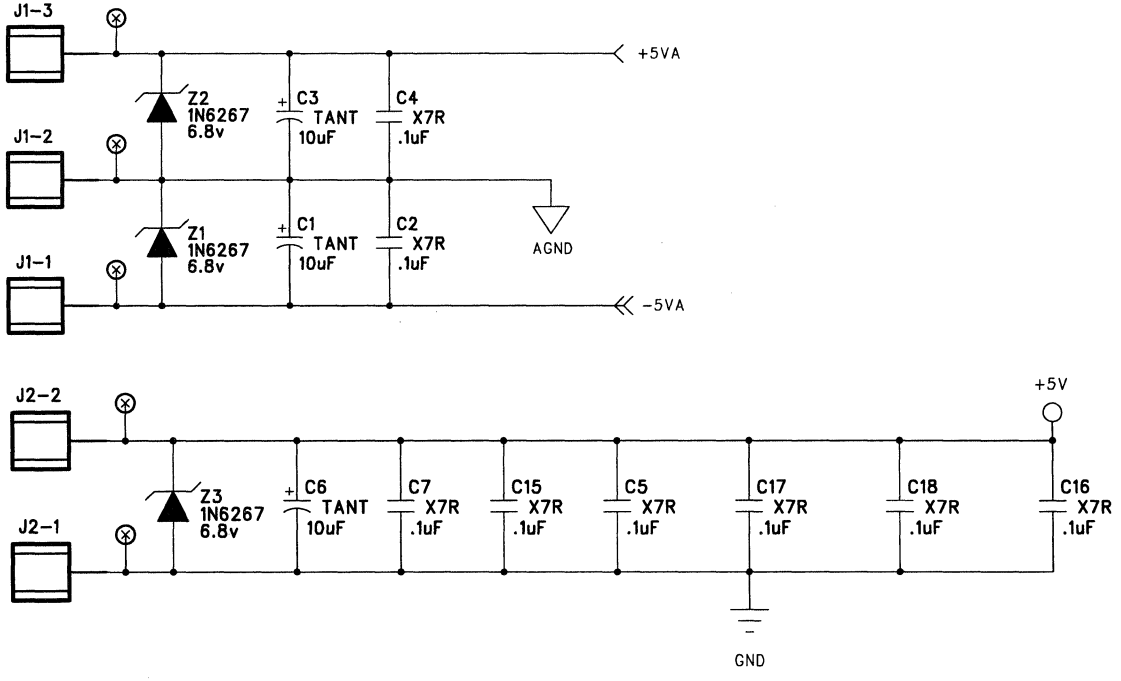


Figure 1. Power Supplies

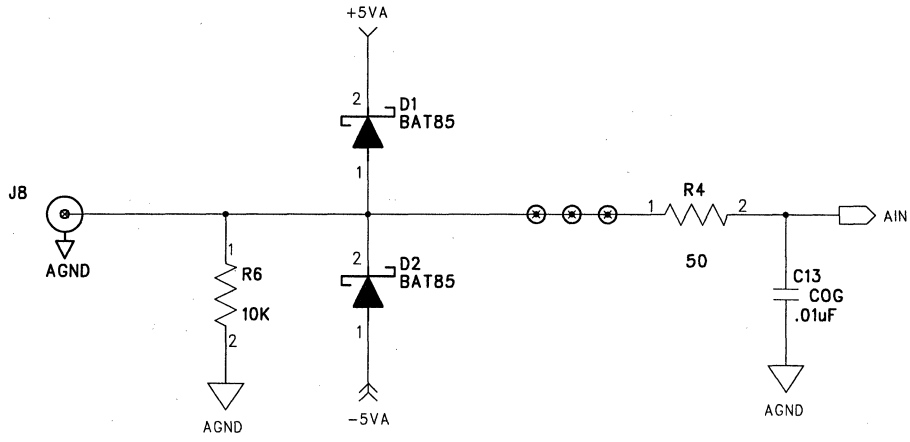


Figure 2. Analog Input Circuit

Clock and Conversion

Figure 3 shows the on-board clock and conversion control circuitry. The evaluation board is designed to run off the on-board 10 MHz oscillator (U4). The ADC can also operate from an internal clock oscillator, by connecting the CLKIN pin to -5VA. Test points are provided to easily implement the internal oscillator.

The $\overline{\text{CONVST}}$ signal on the evaluation board is derived from the on-board 10 MHz clock oscillator. The 10 MHz is divided by 20, providing a 500 kHz signal. External signals can be used by breaking the $\overline{\text{CONVST}}$ jumper at the test points and attaching the external signal at pin 6 of connector J4.

Digital Output Data

The CS5030/31/32 ADCs support three digital output data formats. These include 12-bit parallel, 8-bit byte, and serial interface formats. Several of the ADC output pins have dual roles or modes of operation (see the CS5030/31 or CS5032 data sheets). The position of the "FORMAT" jumper determines which output format is active, with all three formats available through the 40-pin header J4. Serial output data is also available through the 10-pin header J3.

12-Bit Parallel Operation
Selecting the "+" position for the "FORMAT" jumper places the board in 12-bit parallel mode. All parallel output signals are buffered by U1 and U3, and are available on header J4 (figure 4). The rising edge of the $\overline{\text{BUSY}}$ signal, available on pin-40 of J4, can be used to latch the 12-bit parallel data into subsequent digital circuitry.

8-Bit Byte Operation
Selecting the "0" or the "-" position for the "FORMAT" jumper places the board in 8-bit byte mode. The data is available on D0 to D7 of header J4 in two separate read operations. The lower byte is read with HBEN low. The four more significant bits are read with HBEN high. The high byte word includes four leading zeros (D4 to D7) to fill out the remaining four significant bits from the ADC. All byte output signals are buffered by U1 and U3.

Serial Operation
Selecting the "0" or the "-" position for the "FORMAT" jumper also places the board in se-

rial mode. In the "-" position, the serial clock SCLK operates continuously; in the "0" jumper position, the serial clock SCLK is active only when the ADC is outputting serial data. The rising edge of SCLK can be used to latch serial data into subsequent circuitry. The serial data and control lines are available on J3, and the DATA8 (SDATA), DATA9(SCLK), and DATA10 ($\overline{\text{SSTRB}}$) lines of J4. All serial output signals are buffered by U1.

Convert Start Operation

MODE 1 Operation

The $\overline{\text{CONVST}}$ signal is used to put the ADC into hold mode and initiate a conversion. At the end of the conversion, the ADC returns to its tracking mode. Conversion begins on the rising edge of the $\overline{\text{CONVST}}$, provided that $\overline{\text{CS}}$ is high (note that external pull-up resistors on $\overline{\text{CS}}$ and $\overline{\text{RD}}$ default both to logic high if no external logic signal is present for these pins on the J4 header). The $\overline{\text{BUSY}}$ line on J4, which goes low when the output data becomes available, can be used as a microprocessor interrupt. Bringing $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low allows data to be read from the ADC and also resets $\overline{\text{BUSY}}$ high. $\overline{\text{CONVST}}$ must be high when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are brought low in this mode. Data cannot be read during the conversion cycle because the ADC output latches are disabled during this process.

MODE 2 Operation

In this mode, $\overline{\text{CONVST}}$ is held permanently low (Break $\overline{\text{CONVST}}$ jumper at the test points and add jumper between $\overline{\text{CONST\_BUF}}$ and $\overline{\text{CONVST}}$. Ground the $\overline{\text{HOLD}}$ signal J4-6). Bringing $\overline{\text{CS}}$ low (while HBEN is low) through the J4 header, puts the ADC into hold mode and initiates a conversion. The $\overline{\text{BUSY}}$ line on J4 goes low at the start of the conversion and returns high at the end of conversion.

FORMAT JUMPER	
+	12-bit parallel mode
0	8-bit byte or serial (16 bit SCLK))
-	8-bit byte or serial (continuous SCLK)

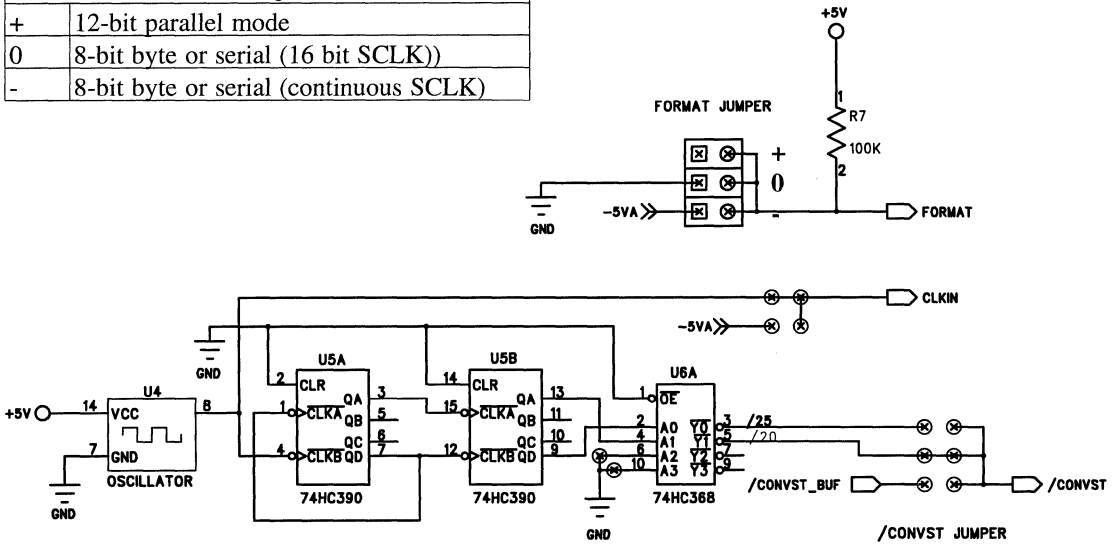


Figure 3. Clock and Convert Start Circuitry

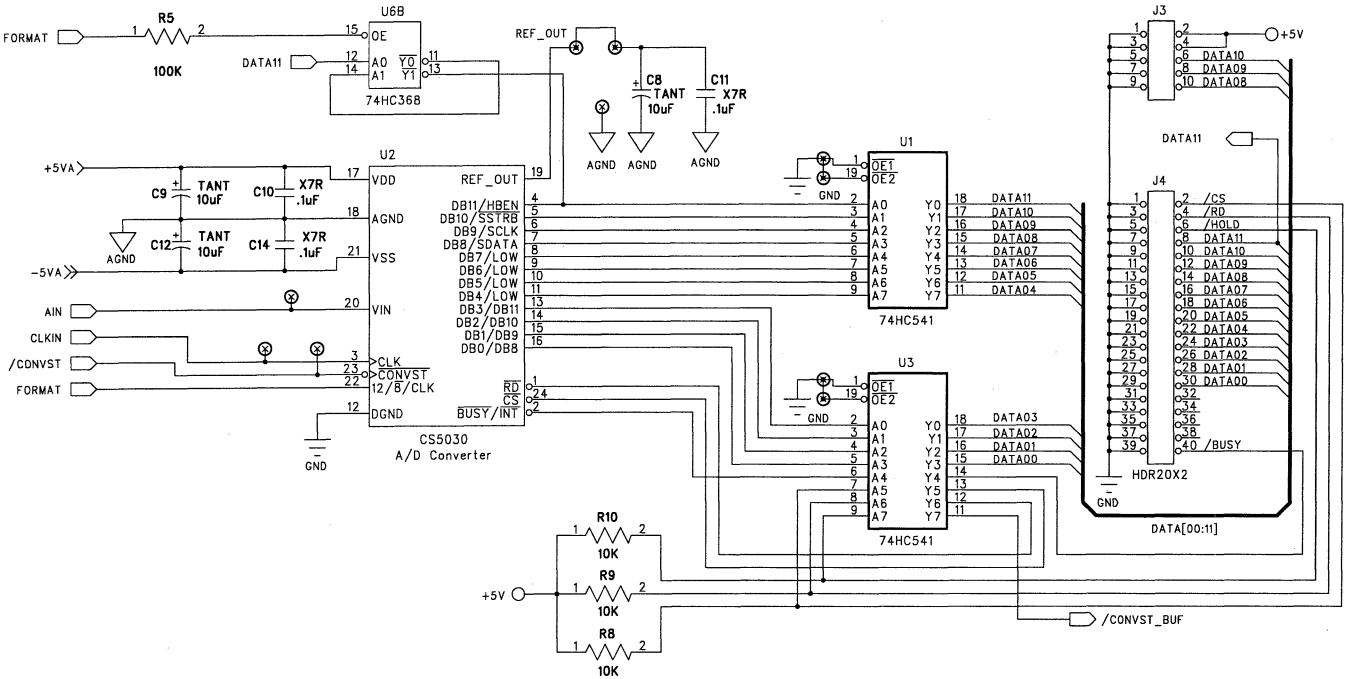


Figure 4. ADC Connections and Digital Output

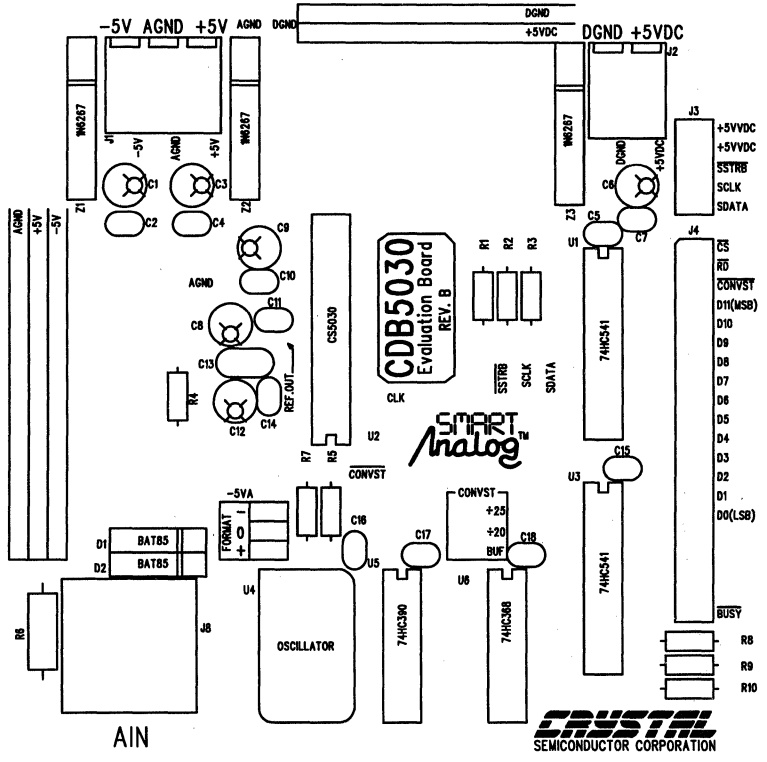


Figure 5. CDB5030/CDB5031/CDB5032 Component Layout

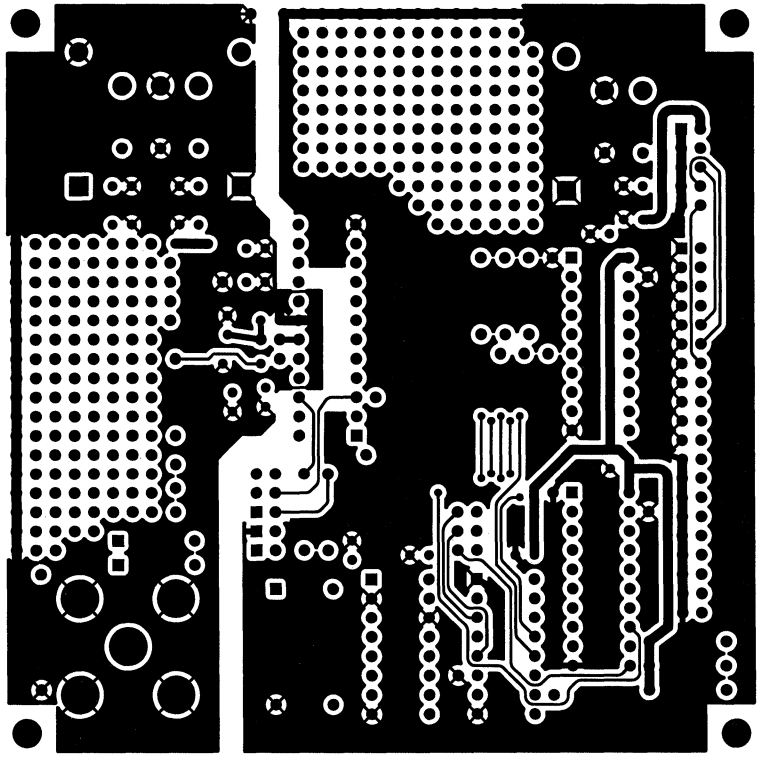


Figure 6. Top Ground Plane Layer (NOT TO SCALE)

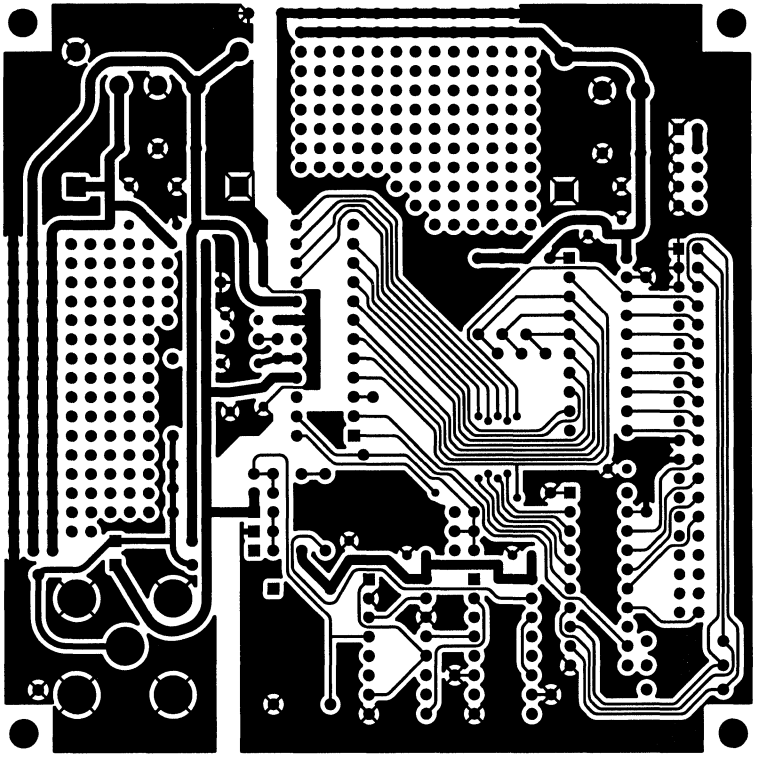


Figure 7. Bottom Trace Layer (NOT TO SCALE)

• Notes •

16-Bit, 100 kHz/20 kHz A/D Converters

Features

- Monolithic CMOS A/D Converters
  - Inherent Sampling Architecture
  - 2-Channel Input Multiplexer
  - Flexible Serial Output Port
- Ultra-Low Distortion
  - S/(N+D): 92 dB
  - THD: 0.001%
- Conversion Time
  - CS5101A: 8 µs
  - CS5102A: 40 µs
- Linearity Error: ± 0.001% FS
  - Guaranteed No Missing Codes
- Self-Calibration Maintains Accuracy Over Time and Temperature
- Low Power Consumption
  - CS5101A: 320 mW
  - CS5102A: 44 mW
  - Power-down Mode: < 1 mW
- Evaluation Board Available

General Description

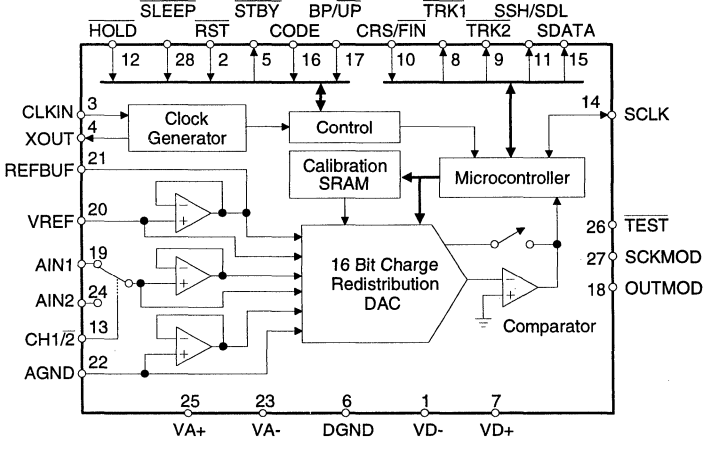
The CS5101A and CS5102A are 16-bit monolithic CMOS analog-to-digital converters capable of 100 kHz (5101A) and 20 kHz (5102A) throughput. The CS5102A's low power consumption of 44 mW, coupled with a power down mode, makes it particularly suitable for battery powered operation.

On-chip self-calibration circuitry achieves nonlinearity of ±0.001% of FS and guarantees 16-bit no missing codes over the entire specified temperature range. Superior linearity also leads to 92 dB S/(N+D) with harmonics below -100 dB. Offset and full-scale errors are minimized during the calibration cycle, eliminating the need for external trimming.

The CS5101A and CS5102A each consist of a 2-channel input multiplexer, DAC, conversion and calibration microcontroller, clock generator, comparator, and serial communications port. The inherent sampling architecture of the device eliminates the need for an external track and hold amplifier.

The converters' 16-bit data is output in serial form with either binary or 2's complement coding. Three output timing modes are available for easy interfacing to microcontrollers and shift registers. Unipolar and bipolar input ranges are digitally selectable.

ORDERING INFORMATION: Page 2-148



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

ANALOG CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 4.5V; Full-Scale Input Sinewave, 1 kHz; CLKIN = 4 MHz for -16, 8 MHz for -8; f_s = 50 kHz for -16, 100 kHz for -8; Bipolar Mode; FRN Mode; AIN1 and AIN2 tied together, each channel tested separately; Analog Source Impedance = 50 Ω with 1000 pF to AGND unless otherwise specified)

Parameter*			CS5101A-J,K Min	CS5101A-J,K Typ	CS5101A-J,K Max	CS5101A-A,B Min	CS5101A-A,B Typ	CS5101A-A,B Max	CS5101A-S,T Min	CS5101A-S,T Typ	CS5101A-S,T Max	Units
Specified Temperature Range			0 to +70			-40 to +85			-55 to +125			°C
Accuracy												
Linearity Error	-J,A,S	(Note 1)	-	0.002	0.003	-	0.002	0.003	-	0.002	0.004	%FS
	-K,B,T		-	0.001	0.002	-	0.001	0.002	-	0.001	0.003	%FS
	Drift	(Note 2)	-	± 1/4	-	-	± 1/4	-	-	± 1/2	-	ΔLSB
Differential Linearity		(Notes 3, 4)	16	-	-	16	-	-	16	-	-	Bits
Full Scale Error	-J,A,S	(Note 1)	-	± 1	± 4	-	± 1	± 4	-	± 2	± 5	LSB
	-K,B,T		-	± 1	± 3	-	± 1	± 3	-	± 2	± 4	LSB
	Drift	(Note 2)	-	± 1	-	-	± 1	-	-	± 2	-	ΔLSB
Unipolar Offset	-J,A,S	(Note 1)	-	± 2	± 5	-	± 2	± 5	-	± 2	± 5	LSB
	-K,B,T		-	± 2	± 4	-	± 2	± 4	-	± 2	± 4	LSB
	Drift	(Note 2)	-	± 1	-	-	± 1	-	-	± 2	-	ΔLSB
Bipolar Offset	-J,A,S	(Note 1)	-	± 2	± 5	-	± 2	± 5	-	± 2	± 5	LSB
	-K,B,T		-	± 2	± 3	-	± 2	± 3	-	± 2	± 3	LSB
	Drift	(Note 2)	-	± 1	-	-	± 2	-	-	± 2	-	ΔLSB
Bipolar Negative Full-Scale Error												
	-J,A,S	(Note 1)	-	± 1	± 4	-	± 1	± 4	-	± 1	± 5	LSB
	-K,B,T		-	± 1	± 3	-	± 1	± 3	-	± 1	± 3	LSB
	Drift	(Note 2)	-	± 1	-	-	± 1	-	-	± 2	-	ΔLSB
Dynamic Performance (Bipolar Mode)												
Peak Harmonic or Spurious Noise (Note 1)												
1 kHz Input	-J,A,S		96	100	-	96	100	-	94	100	-	dB
	-K,B,T		98	102	-	98	102	-	98	102	-	dB
12 kHz Input	-J,A,S		85	88	-	85	88	-	83	88	-	dB
	-K,B,T		85	91	-	85	91	-	85	91	-	dB
Total Harmonic Distortion	-J,A,S		-	0.002	-	-	0.002	-	-	0.002	-	%
	-K,B,T		-	0.001	-	-	0.001	-	-	0.001	-	%
Signal-to-Noise Ratio		(Note 1)										
0dB Input	-J,A,S		87	90	-	87	90	-	87	90	-	dB
	-K,B,T		90	92	-	90	92	-	90	92	-	dB
-60 dB Input	-J,A,S		-	30	-	-	30	-	-	30	-	dB
	-K,B,T		-	32	-	-	32	-	-	32	-	dB
Noise		(Note 5)										
	Unipolar Mode		-	35	-	-	35	-	-	35	-	μV_{rms}
	Bipolar Mode		-	70	-	-	70	-	-	70	-	μV_{rms}

Notes: 1. Applies after calibration at any temperature within the specified temperature range. At temp
2. Total drift over specified temperature range after calibration at power-up at 25 °C.
3. Minimum resolution for which no missing codes is guaranteed over the specified temperature range.
4. Clock speeds of less than 1.0 MHz, at temperatures >100°C will degrade DNL performance.
5. Wideband noise aliased into the baseband. Referred to the input.

*Refer to *Parameter Definitions* (immediately following the pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (continued)

Parameter*	Symbol	CS5101A -J,K Min	Typ	Max	CS5101A -A,B Min	Typ	Max	CS5101A -S,T Min	Typ	Max	Units
Specified Temperature Range	-	0 to +70			40 to +85			55 to +125			°C
Analog Input											
Aperture Time	-	-	25	-	-	25	-	-	25	-	ns
Aperture Jitter	-	-	100	-	-	100	-	-	100	-	ps
Input Capacitance (Note 6)											
Unipolar Mode	-	-	320	425	-	320	425	-	320	425	pF
Bipolar Mode	-	-	200	265	-	200	265	-	200	265	pF
Conversion & Throughput											
Conversion Time (Note 7)											
-8	t_c	-	-	8.12	-	-	8.12	-	-	8.12	µs
-16	tc	-	-	16.25	-	-	16.25	-	-	16.25	µs
Acquisition Time (Note 8)											
-8	t_a	-	-	1.88	-	-	1.88	-	-	2.88	µs
-16	ta	-	2.6	3.75	-	2.6	3.75	-	2.6	3.75	µs
Throughput (Note 9)											
-8	f_{tp}	100	-	-	100	-	-	100	-	-	kHz
-16	f_{tp}	50	-	-	50	-	-	50	-	-	kHz
Power Supplies											
Power Supply Current (Note 10)											
Positive Analog	I_{A+}	-	21	28	-	21	28	-	21	28	mA
Negative Analog	I_{A-}	-	-21	-28	-	-21	-28	-	-21	-28	mA
($\overline{SLEEP}$ High) Positive Digital	I_{D+}	-	11	15	-	11	15	-	11	15	mA
Negative Digital	I_{D-}	-	-11	-15	-	-11	-15	-	-11	-15	mA
Power Consumption (Notes 10, 11)											
($\overline{SLEEP}$ High)	P_{do}	-	320	430	-	320	430	-	320	430	mW
($\overline{SLEEP}$ Low)	P_{ds}	-	1	-	-	1	-	-	1	-	mW
Power Supply Rejection: (Note 12)											
Positive Supplies	PSR	-	84	-	-	84	-	-	84	-	dB
Negative Supplies	PSR	-	84	-	-	84	-	-	84	-	dB

Notes:
6. Applies only in the track mode. When converting or calibrating, input capacitance will not exceed 30 pF.
7. Conversion time scales directly to the master clock speed. The times shown are for synchronous, internal loopback (FRN mode) with 8.0 MHz CLKIN. In PDT, RBT, and SSC modes, asynchronous delay between the falling edge of $\overline{HOLD}$ and the start of conversion may add to the apparent conversion time. This delay will not exceed 1.5 master clock cycles + 10 ns. In PDT, RBT, and SSC modes, CLKIN can be increased as long as the $\overline{HOLD}$ sample rate is 100 kHz max.
8. The CS5101A requires 6 clock cycles of coarse charge, followed by a minimum of 1.125 µs of fine charge. FRN mode allows 9 clock cycles for fine charge which provides for the minimum 1.125 µs with an 8 MHz clock, however; in PDT, RBT, or SSC modes, at clock frequencies of 8 MHz or less, fine charge may be less than 9 clock cycles. This reflects the typ. specification (6 clock cycles + 1.125 µs).
9. Throughput is the sum of the acquisition and conversion times. It will vary in accordance with conditions affecting acquisition and conversion times, as described above.
10. All outputs unloaded. All inputs at VD+ or DGND.
11. Power consumption in the sleep mode applies with no master clock applied (CLKIN held high or low).
12. With 300 mV p-p, 1 kHz ripple applied to each supply separately in the bipolar mode. Rejection improves by 6 dB in the unipolar mode to 90 dB. Figure 23 shows a plot of typical power supply rejection versus frequency.

SWITCHING CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

Parameter		Symbol	Min	Typ	Max	Units
CLKIN Period	(Note 4)					
	-8	t_{clk}	108	-	10,000	ns
	-16	t_{clk}	250	-	10,000	ns
CLKIN Low Time		t_{clkl}	37.5	-	-	ns
CLKIN High Time		t_{clkh}	37.5	-	-	ns
Crystal Frequency	(Note 13)					
	-8	f_{xtal}	2.0	-	9.216	MHz
	-16	f_{xtal}	2.0	-	4.0	MHz
$\overline{SLEEP}$ Rising to Oscillator Stable	(Note 14)	-	-	2	-	ms
$\overline{RST}$ Pulse Width		t_{rst}	150	-	-	ns
$\overline{RST}$ to $\overline{STBY}$ Falling		t_{drrs}	-	100	-	ns
$\overline{RST}$ Rising to $\overline{STBY}$ Rising		t_{cal}	-	11,528,160	-	t_{clk}
CH1/$\overline{2}$ Edge to $\overline{TRK1}$, $\overline{TRK2}$ Rising	(Note 15)	t_{drsh1}	-	80	-	ns
CH1/$\overline{2}$ Edge to $\overline{TRK1}$, $\overline{TRK2}$ Falling	(Note 15)	t_{dfsh4}	-	-	$68t_{clk}$+260	ns
$\overline{HOLD}$ to SSH Falling	(Note 16)	t_{dfsh2}	-	60		ns
$\overline{HOLD}$ to $\overline{TRK1}$, $\overline{TRK2}$, Falling	(Note 16)	t_{dfsh1}	$66t_{clk}$	-	$68t_{clk}$+260	ns
$\overline{HOLD}$ to $\overline{TRK1}$, $\overline{TRK2}$, SSH Rising	(Note 16)	t_{drsh}	-	120	-	ns
$\overline{HOLD}$ Pulse Width	(Note 17)	t_{hold}	$1t_{clk}$+20	-	$63t_{clk}$	ns
$\overline{HOLD}$ to CH1/$\overline{2}$ Edge	(Note 16)	t_{dhlri}	15	-	$64t_{clk}$	ns
$\overline{HOLD}$ Falling to CLKIN Falling	(Note 17)	t_{hcf}	95	-	$1t_{clk}$+10	ns

Notes: 13. External loading capacitors are required to allow the crystal to oscillate. Maximum crystal frequency is 8.0 MHz in FRN mode (100 kHz sample rate).

14. With a 8 MHz crystal, two 10 pF loading capacitors and a 10 MΩ parallel resistor (see Figure 8).

15. These times are for FRN mode.

16. SSH only works correctly if $\overline{HOLD}$ falling edge is within +15 to +30 ns of CH1/$\overline{2}$ edge or if CH1/$\overline{2}$ edge occurs after $\overline{HOLD}$ rises to 64 t_{clk} after $\overline{HOLD}$ has fallen. These times are for PDT and $\overline{RBT}$ modes.

17. When $\overline{HOLD}$ goes low, the analog sample is captured immediately. To start conversion, $\overline{HOLD}$ must be latched by a falling edge of CLKIN. Conversion will begin on the next rising edge of CLKIN after $\overline{HOLD}$ is latched. If $\overline{HOLD}$ is operated synchronous to CLKIN, the $\overline{HOLD}$ pulse width may be as narrow as 150 ns for all CLKIN frequencies if CLKIN falls 95 ns after $\overline{HOLD}$ falls. This ensures that the $\overline{HOLD}$ pulse will meet the minimum specification for t_{hcf}.

ANALOG CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 4.5V; Full-Scale Input Sinewave, 200 Hz; CLKIN = 1.6 MHz; f_S = 20 kHz; Bipolar Mode; FRN Mode; AIN1 and AIN2 tied together, each channel tested separately; Analog Source Impedance = 50 Ω with 1000pF to AGND unless otherwise specified)

Parameter*			CS5102A-J,K Min	CS5102A-J,K Typ	CS5102A-J,K Max	CS5102A-A,B Min	CS5102A-A,B Typ	CS5102A-A,B Max	CS5102A-S,T Min	CS5102A-S,T Typ	CS5102A-S,T Max	Units
Specified Temperature Range			0 to +70			-40 to +85			-55 to +125			°C
Accuracy												
Linearity Error	-J,A,S	(Note 1)	-	0.002	0.003	-	0.002	0.003	-	0.002	0.004	%FS
	-K,B,T		-	0.001	0.0015	-	0.001	0.0015	-	0.001	0.002	%FS
	Drift	(Note 2)	-	± 1/4	-	-	± 1/4	-	-	± 1/2	-	ΔLSB
Differential Linearity		(Notes 3, 18)	16	-	-	16	-	-	16	-	-	Bits
Full Scale Error	-J,A,S	(Note 1)	-	± 2	± 4	-	± 2	± 4	-	± 2	± 5	LSB
	-K,B,T		-	± 2	± 3	-	± 2	± 3	-	± 2	± 3	LSB
	Drift	(Note 2)	-	± 1	-	-	± 1	-	-	± 2	-	ΔLSB
Unipolar Offset	-J,A,S	(Note 1)	-	± 1	± 4	-	± 1	± 4	-	± 1	± 5	LSB
	-K,B,T		-	± 1	± 3	-	± 1	± 3	-	± 1	± 3	LSB
	Drift	(Note 2)	-	± 1	-	-	± 1	-	-	± 2	-	ΔLSB
Bipolar Offset	-J,A,S	(Note 1)	-	± 1	± 4	-	± 1	± 4	-	± 1	± 5	LSB
	-K,B,T		-	± 1	± 3	-	± 1	± 3	-	± 1	± 3	LSB
	Drift	(Note 2)	-	± 1	-	-	± 2	-	-	± 2	-	ΔLSB
Bipolar Negative Full-Scale Error	-J,A,S	(Note 1)	-	± 2	± 4	-	± 2	± 4	-	± 2	± 5	LSB
	-K,B,T		-	± 2	± 3	-	± 2	± 3	-	± 2	± 3	LSB
	Drift	(Note 2)	-	± 1	-	-	± 2	-	-	± 2	-	ΔLSB
Dynamic Performance (Bipolar Mode)												
Peak Harmonic or Spurious Noise	-J,A,S	(Note 1)	96	100	-	96	100	-	94	100	-	dB
	-K,B,T		98	102	-	98	102	-	98	102	-	dB
Total Harmonic Distortion	-J,A,S		-	0.002	-	-	0.002	-	-	0.002	-	%
	-K,B,T		-	0.001	-	-	0.001	-	-	0.001	-	%
Signal-to-Noise Ratio		(Note 1)										
0dB Input	-J,A,S		87	90	-	87	90	-	87	90	-	dB
	-K,B,T		90	92	-	90	92	-	90	92	-	dB
-60 dB Input	-J,A,S		-	30	-	-	30	-	-	30	-	dB
	-K,B,T		-	32	-	-	32	-	-	32	-	dB
Noise		(Note 5)										
	Unipolar Mode		-	35	-	-	35	-	-	35	-	μV_{rms}
	Bipolar Mode		-	70	-	-	70	-	-	70	-	μV_{rms}

Note: 18. Clock speeds of less than 1.6 MHz, at temperatures >100°C will degrade DNL performance.

*Refer to *Parameter Definitions* (immediately following the pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (continued)

Parameter*	Symbol	CS5102A -J,K Min	Typ	Max	CS5102A -A,B Min	Typ	Max	CS5102A -S,T Min	Typ	Max	Units
Specified Temperature Range	-	0 to +70			-40 to +85			-55 to +125			°C
Analog Input											
Aperture Time	-	-	30	-	-	30	-	-	30	-	ns
Aperture Jitter	-	-	100	-	-	100	-	-	100	-	ps
Input Capacitance (Note 6)	-	-	320	425	-	320	425	-	320	425	pF
Unipolar Mode	-	-	200	265	-	200	265	-	200	265	pF
Bipolar Mode											
Conversion & Throughput											
Conversion Time (Note 19)	t_c	-	-	40.625	-	-	40.625	-	-	40.625	µs
Acquisition Time (Note 20)	t_a	-	-	9.375	-	-	9.375	-	-	9.375	µs
Throughput (Note 21)	f_{tp}	20	-	-	20	-	-	20	-	-	kHz
Power Supplies											
Power Supply Current (Note 22)											
Positive Analog	I_{A+}	-	2.4	3.5	-	2.4	3.5	-	2.4	3.5	mA
Negative Analog	I_{A-}	-	-2.4	-3.5	-	-2.4	-3.5	-	-2.4	-3.5	mA
($\overline{SLEEP}$ High) Positive Digital	I_{D+}	-	2.5	3.5	-	2.5	3.5	-	2.5	3.5	mA
Negative Digital	I_{D-}	-	-1.5	-2.5	-	-1.5	-2.5	-	-1.5	-2.5	mA
Power Consumption (Notes 11, 22)											
($\overline{SLEEP}$ High)	P_{do}	-	44	65	-	44	65	-	44	65	mW
($\overline{SLEEP}$ Low)	P_{ds}	-	1	-	-	1	-	-	1	-	mW
Power Supply Rejection: (Note 23)											
Positive Supplies	PSR	-	84	-	-	84	-	-	84	-	dB
Negative Supplies	PSR	-	84	-	-	84	-	-	84	-	dB

Notes: 19. Conversion time scales directly to the master clock speed. The times shown are for synchronous, internal loopback (FRN mode). In PDT, RBT, and SSC modes, asynchronous delay between the falling edge of $\overline{HOLD}$ and the start of conversion may add to the apparent conversion time. This delay will not exceed 1 master clock cycle + 140 ns.

20. The CS5102A requires 6 clock cycles of coarse charge, followed by a minimum of 5.625 µs of fine charge. FRN mode allows 9 clock cycles for fine charge which provides for the minimum 5.625 µs with an 1.6 MHz clock, however; in PDT, RBT, or SSC modes, at clock frequencies less than 1.6 MHz, fine charge may be less than 9 clock cycles.

21. Throughput is the sum of the acquisition and conversion times. It will vary in accordance with conditions affecting acquisition and conversion times, as described above.

22. All outputs unloaded. All inputs at VD+ or DGND. See table below for power dissipation vs. clock frequency.

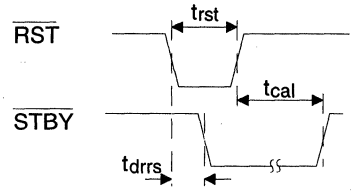
23. With 300 mV p-p, 1 kHz ripple applied to each supply separately in the bipolar mode. Rejection improves by 6 dB in the unipolar mode to 90 dB. Figure 23 shows a plot of typical power supply rejection versus frequency.

Typ. Power (mW)	CLKIN (MHz)
34	0.8
37	1.0
39	1.2
41	1.4
44	1.6

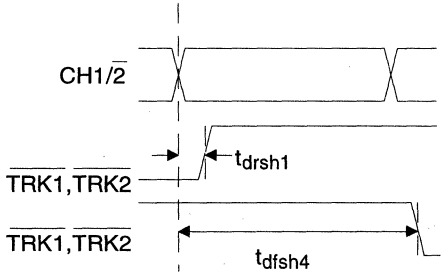
SWITCHING CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX};
VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

Parameter		Symbol	Min	Typ	Max	Units
CLKIN Period	(Note 18,24)	t_{clk}	0.5	-	10	µs
CLKIN Low Time		t_{clkl}	200	-	-	ns
CLKIN High Time		t_{clkh}	200	-	-	ns
Crystal Frequency	(Note 24, 25)	f_{xtal}	0.9	1.6	2.0	MHz
$\overline{SLEEP}$ Rising to Oscillator Stable	(Note 26)	-	-	20	-	ms
$\overline{RST}$ Pulse Width		t_{rst}	150	-	-	ns
$\overline{RST}$ to $\overline{STBY}$ Falling		t_{drrs}	-	100	-	ns
$\overline{RST}$ Rising to $\overline{STBY}$ Rising		t_{cal}	-	2,882,040	-	t_{clk}
CH1/$\overline{2}$ Edge to $\overline{TRK1}$, $\overline{TRK2}$ Rising	(Note 27)	t_{drsh1}	-	80	-	ns
CH1/$\overline{2}$ Edge to $\overline{TRK1}$, $\overline{TRK2}$ Falling	(Note 27)	t_{dfsh4}	-	-	$68t_{clk}$+260	ns
$\overline{HOLD}$ to SSH Falling	(Note 28)	t_{dfsh2}	-	60		ns
$\overline{HOLD}$ to $\overline{TRK1}$, $\overline{TRK2}$, Falling	(Note 28)	t_{dfsh1}	$66t_{clk}$	-	$68t_{clk}$+260	ns
$\overline{HOLD}$ to $\overline{TRK1}$, $\overline{TRK2}$, SSH Rising	(Note 28)	t_{drsh}	-	120	-	ns
$\overline{HOLD}$ Pulse Width	(Note 29)	t_{hold}	$1t_{clk}$+20	-	$63t_{clk}$	ns
$\overline{HOLD}$ to CH1/$\overline{2}$ Edge	(Note 28)	t_{dhlri}	15	-	$64t_{clk}$	ns
$\overline{HOLD}$ Falling to CLKIN Falling	(Note 29)	t_{hcf}	55	-	$1t_{clk}$+10	ns

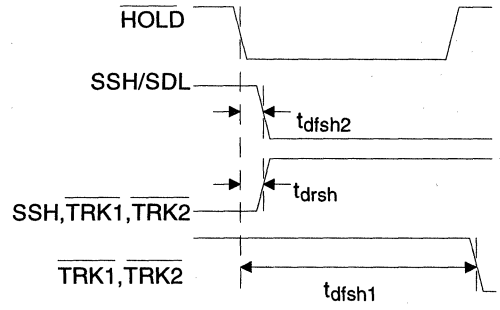
Note: 24. Minimum CLKIN period is 0.625 µs in FRN mode (20 kHz sample rate). At temperatures >+85 °C, and with clock frequencies <1.6 MHz, analog performance may be degraded.
25. External loading capacitors are required to allow the crystal to oscillate. Maximum crystal frequency is 1.6 MHz in FRN mode (20 kHz sample rate).
26. With a 2.0 MHz crystal, two 33 pF loading capacitors and a 10 MΩ parallel resistor (see Figure 8).
27. These times are for FRN mode.
28. SSH only works correctly if $\overline{HOLD}$ falling edge is within +15 to +30 ns of CH1/$\overline{2}$ edge or if CH1/$\overline{2}$ edge occurs after $\overline{HOLD}$ rises to 64 t_{clk} after $\overline{HOLD}$ has fallen. These times are for PDT and RBT modes.
29. When $\overline{HOLD}$ goes low, the analog sample is captured immediately. To start conversion, $\overline{HOLD}$ must be latched by a falling edge of CLKIN. Conversion will begin on the next rising edge of CLKIN after $\overline{HOLD}$ is latched. If $\overline{HOLD}$ is operated synchronous to CLKIN, the $\overline{HOLD}$ pulse width may be as narrow as 150 ns for all CLKIN frequencies if CLKIN falls 55 ns after $\overline{HOLD}$ falls. This ensures that the $\overline{HOLD}$ pulse will meet the minimum specification for t_{hcf}.



Reset and Calibration Timing

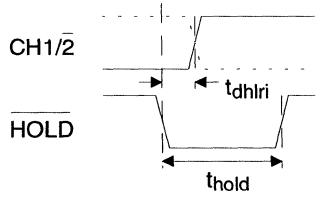


a. FRN Mode

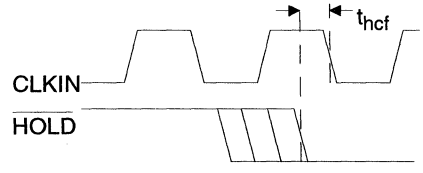


b. PDT, RBT Mode

Control Output Timing



Channel Selection Timing



Start Conversion Timing

SWITCHING CHARACTERISTICS (Continued)

Parameter		Symbol	Min	Typ	Max	Units
PDT and RBT Modes						
SCLK Input Pulse Period		t_{sclk}	200	-	-	ns
SCLK Input Pulse Width Low		t_{sclkl}	50	-	-	ns
SCLK Input Pulse Width High		t_{sclkh}	50	-	-	ns
SCLK Input Falling to SDATA Valid		t_{dss}	-	100	150	ns
$\overline{HOLD}$ Falling to SDATA Valid	PDT Mode	t_{dhs}	-	140	230	ns
$\overline{TRK1}$, $\overline{TRK2}$ Falling to SDATA Valid	(Note 30)	t_{dts}	-	65	125	ns
FRN and SSC Modes						
SCLK Output Pulse Width Low		t_{slkl}	-	$2t_{clk}$	-	t_{clk}
SCLK Output Pulse Width High		t_{slkh}	-	$2t_{clk}$	-	t_{clk}
SDATA Valid Before Rising SCLK		t_{ss}	$2t_{clk}$-100	-	-	ns
SDATA Valid After Rising SCLK		t_{sh}	$2t_{clk}$-100	-	-	ns
SDL Falling to 1st Rising SCLK		t_{rsclk}	-	$2t_{clk}$	-	ns
Last Rising SCLK to SDL Rising	CS5101A CS5102A	t_{rsdl} t_{rsdl}	- -	$2t_{clk}$ $2t_{clk}$	$2t_{clk}$+165 $2t_{clk}$+200	ns ns
$\overline{HOLD}$ Falling to 1st Falling SCLK	CS5101A CS5102A	t_{hfs} thfs	6tclk $6t_{clk}$	- -	$8t_{clk}$+165 $8t_{clk}$+200	ns ns
CH1/$\overline{2}$ Edge to 1st Falling SCLK		t_{chfs}	-	7tclk	-	t_{clk}

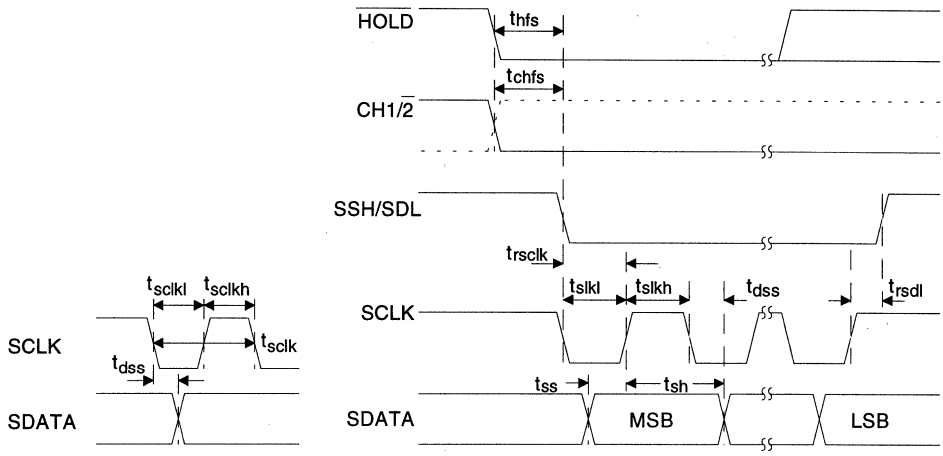
Note: 30. Only valid for $\overline{TRK1}$, $\overline{TRK2}$ falling when SCLK is low. If SCLK is high when $\overline{TRK1}$, $\overline{TRK2}$ falls, then SDATA is valid t_{dss} time after the next falling SCLK.

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

Parameter		Symbol	Min	Typ	Max	Units
Calibration Memory Retention Power Supply Voltage VA+ and VD+	(Note 31)	V_{MR}	2.0	-	-	V
High-Level Input Voltage		V_{IH}	2.0	-	-	V
Low-Level Input Voltage		V_{IL}	-	-	0.8	V
High-Level Output Voltage	(Note 32)	V_{OH}	(VD+)-1.0	-	-	V
Low-Level Output Voltage	I_{OUT} = 1.6 mA	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	-	10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

Notes: 31. VA- and VD- can be any value from zero to -5V for memory retention. Neither VA- or VD- should be allowed to go positive. AIN1, AIN2 or VREF must not be greater than VA+ or VD+. This parameter is guaranteed by characterization.

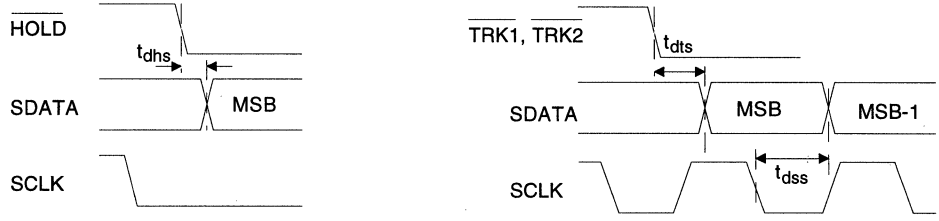
32. I_{OUT} = -100 µA. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ Iout = -40 µA).



a. SCLK input (RBT and PDT mode)

b. SCLK output (SSC and FRN modes)

Serial Data Timing



a. Pipelined Data Transmission (PDT)

b. Register Burst Transmission (RBT) Mode

Data Transmission Timing

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see Note 33)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	-4.5	-5.0	-5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	-4.5	-5.0	-5.5	V
Analog Reference Voltage		VREF	2.5	4.5	(VA+)-0.5	V
Analog Input Voltage:	(Note 34)					
	Unipolar	V_{AIN}	AGND	-	VREF	V
	Bipolar	V_{AIN}	-VREF	-	VREF	V

Notes: 33. All voltages with respect to ground.
34. The CS5101A and CS5102A can accept input voltages up to the analog supplies (VA+ and VA-). They will produce an output of all 1's for inputs above VREF and all 0's for inputs below AGND in unipolar mode and -VREF in bipolar mode, with binary coding (CODE = low).

ABSOLUTE MAXIMUM RATINGS* (AGND, DGND = 0V, all voltages with respect to ground)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital (Note 35)	VD+	-0.3	-	6.0	V
	Negative Digital	VD-	0.3	-	-6.0	V
	Positive Analog	VA+	-0.3	-	6.0	V
	Negative Analog	VA-	0.3	-	-6.0	V
Input Current, Any Pin Except Supplies	(Note 36)	I_{in}	-	-	±10	mA
Analog Input Voltage	(AIN and VREF pins)	V_{INA}	(VA-)-0.3	-	(VA+)+0.3	V
Digital Input Voltage		V_{IND}	-0.3	-	(VA+)+0.3	V
Ambient Operating Temperature		T_A	-55	-	125	°C
Storage Temperature		T_{stg}	-65	-	150	°C
Ambient Operating Temperature		T_A	-55	-	125	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes: 35. In addition, VD+ must not be greater than (VA+) +0.3V
36. Transient currents of up to 100 mA will not cause SCR latch-up.

*WARNING: Operation beyond these limits may result in permanent damage to the device.

GENERAL DESCRIPTION

The CS5101A and CS5102A are 2-channel, 16-bit A/D converters. The devices include an inherent sample/hold and an on-chip analog switch for 2-channel operation. Both channels can thus be sampled and converted at rates up to 50 kHz each (CS5101A) or 10 kHz each (CS5102A). Alternatively, each of the devices can be operated as a single channel ADC operating at 100 kHz (CS5101A) or 20 kHz (CS5102A).

Both the CS5101A and CS5102A can be configured to accept either unipolar or bipolar input ranges, and data is output serially in either binary or 2's complement coding. The devices can be configured in 3 different output modes, as well as an internal, synchronous loopback mode. The CS5101A and CS5102A provide coarse charge/fine charge control, to allow accurate tracking of high-slew signals.

THEORY OF OPERATION

The CS5101A and CS5102A implement the successive approximation algorithm using a charge redistribution architecture. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. All capacitors in the array share a common node at the comparator's input. As shown in Figure 1, their other terminals are capable of being connected to AGND, VREF, or AIN (1 or 2). When the device is not calibrating or converting, all capacitors are tied to AIN. Switch S1 is closed and the charge on the array, tracks the input signal.

When the conversion command is issued, switch S1 opens. This traps the charge on the comparator side of the capacitor array and creates a floating node at the comparator's input. The conversion algorithm operates on this fixed charge, and the signal at the analog input pin is ignored. In effect, the entire DAC capacitor array serves as analog memory during conversion much like a hold capacitor in a sample/hold amplifier.

The conversion consists of manipulating the free plates of the capacitor array to VREF and AGND to form a capacitive divider. Since the charge at the floating node remains fixed, the voltage at that point depends on the proportion of capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance, which when connected to the reference will drive the voltage at the floating node to zero. That binary fraction of capacitance represents the converter's digital output.

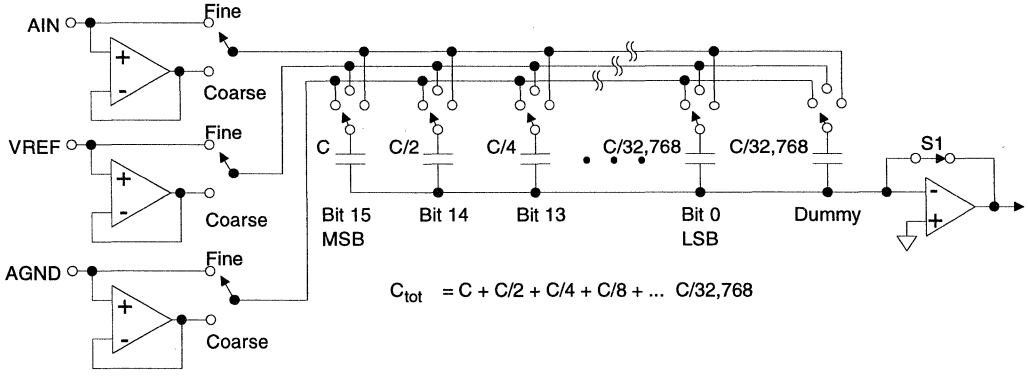


Figure 1. Coarse Charge Input Buffers and Charge Redistribution DAC

Calibration

The ability of the CS5101A or the CS5102A to convert accurately to 16-bits clearly depends on the accuracy of its comparator and DAC. Each device utilizes an "auto-zeroing" scheme to null errors introduced by the comparator. All offsets are stored on the capacitor array while in the track mode and are effectively subtracted from the input signal when a conversion is initiated. Auto-zeroing enhances power supply rejection at frequencies well below the conversion rate.

To achieve 16-bit accuracy from the DAC, the CS5101A and CS5102A use a novel self-calibration scheme. Each bit capacitor shown in Figure 1 actually consists of several capacitors in parallel which can be manipulated to adjust the overall bit weight. An on-chip micro controller precisely adjusts each capacitor with a resolution of 18 bits.

The CS5101A and CS5102A should be reset upon power-up, thus initiating a calibration cycle. The device then stores its calibration coefficients in on-chip SRAM. When the CS5101A and CS5102A are in power-down mode ($\overline{SLEEP}$ low), they retain the calibration coefficients in memory, and need not be recalibrated when normal operation is resumed.

OPERATION OVERVIEW

Monolithic design and inherent sampling architecture make the CS5101A and CS5102A extremely easy to use.

Initiating Conversions

A falling transition on the $\overline{HOLD}$ pin places the input in the hold mode and initiates a conversion cycle. The charge is trapped on the capacitor array the instant $\overline{HOLD}$ goes low. The device will complete conversion of the sample within 66 master clock cycles, then automatically return to the track mode. After allowing a short time for acquisition, the device will be ready for another conversion.

In contrast to systems with separate track-and-holds and A/D converters, a sampling clock can simply be connected to the $\overline{HOLD}$ input. The duty cycle of this clock is not critical. The $\overline{HOLD}$ input is latched internally by the master clock, so it need only remain low for $1/f_{clk}$ + 20 ns, but no longer than the minimum conversion time minus two master clocks or an additional conversion cycle will be initiated with inadequate time for acquisition. In Free Run mode, SCKMOD = OUTMOD = 0, the device will convert at a rate of CLKIN/80, and the $\overline{HOLD}$ input is ignored.

As with any high-resolution A-to-D system, it is recommended that sampling is synchronized to the master system clock in order to minimize the effects of clock feedthrough. However, the CS5101A and CS5102A may be operated entirely asynchronous to the master clock if necessary.

Tracking the Input

Upon completing a conversion cycle the CS5101A and CS5102A immediately return to the track mode. The CH1/$\overline{2}$ pin directly controls the input switch, and therefore directly determines which channel will be tracked. Ideally, the CH1/$\overline{2}$ pin should be switched during the conversion cycle, thereby nullifying the input mux switching time, and guaranteeing a stable input at the start of acquisition. If, however, the CH1/$\overline{2}$ control is changed during the acquisition phase, adequate coarse charge and fine charge time must be allowed before initiating conversion.

When the CS5101A or the CS5102A enters tracking mode, it uses an internal input buffer amplifier to provide the bulk of the charge on the capacitor array (coarse-charge), thereby reducing the current load on the external analog circuitry. Coarse-charge is internally initiated for 6 clock

cycles at the end of every conversion. The buffer amplifier is then bypassed, and the capacitor array is directly connected to the input. This is referred to as fine-charge, during which the charge on the array is allowed to accurately settle to the input voltage (see Figure 10).

With a full scale input step, the coarse-charge input buffer of the CS5101A will charge the capacitor array within 1% in 650 ns. The converter timing allows 6 clock cycles for coarse charge settling time. When the CS5101A switches to fine-charge mode, its slew rate is somewhat reduced. In fine-charge, the CS5101A can slew at 2 V/µs in unipolar mode. In bipolar mode, only half the capacitor array is connected to the analog input, so the CS5101A can slew at 4V/µs.

With a full scale input step, the coarse-charge input buffer of the CS5102A will charge the capacitor array within 1% in 3.75 µs. The converter timing allows 6 clock cycles for coarse charge settling time. When in fine-charge mode, the CS5102A can slew at 0.4 V/µs in unipolar mode; and at 0.8 V/µs in bipolar mode.

Acquisition of fast slewing signals can be hastened if the voltage change occurs during or immediately following the conversion cycle. For instance, in multiple channel applications (using either the device's internal channel selector or an external MUX), channel selection should occur while the CS5101A or the CS5102A is converting. Multiplexer switching and settling time is thereby removed from the overall throughput equation.

If the input signal changes drastically during the acquisition period (such as changing the signal source), the device should be in coarse-charge for an adequate period following the change. The CS5101A and CS5102A can be forced into coarse-charge by bringing CRS/$\overline{\text{FIN}}$ high. The buffer amplifier is engaged when CRS/$\overline{\text{FIN}}$ is high, and may be switched in any number of times during tracking. If CRS/$\overline{\text{FIN}}$ is held low, the CS5101A and CS5102A will only coarse-charge for the first 6 clock cycles following a conversion, and will stay in fine-charge until $\overline{\text{HOLD}}$ goes low. To get an accurate sample using the CS5101A, at least 750 ns of coarse-charge, followed by 1.125 µs of fine-charge is required before initiating a conversion. If coarse charge is not invoked, then up to 25 µs should be allowed after a step change input for proper acquisition. To get an accurate sample using the CS5102A, at least 3.75 µs of coarse-charge, followed by 5.625 µs of fine-charge is required before initiating a conversion (see Figure 2). If coarse charge is not invoked, then up to 125 µs should be allowed after a step change input for proper acquisition. The CRS/$\overline{\text{FIN}}$ pin must be low prior to $\overline{\text{HOLD}}$ becoming active and be held low during conversion.

Master Clock

The CS5101A and CS5102A can operate either from an externally-supplied master clock, or from their own crystal oscillator (with a crystal). To enable the internal crystal oscillator, simply tie a crystal across the XOUT and CLKIN pins and add 2 capacitors and a resistor, as shown on the system connection diagram in Figure 8.

Calibration and conversion times directly scale to the master clock frequency. The CS5101A-8 can operate with clock or crystal frequencies up to 9.216 MHz (8.0 MHz in FRN mode). This allows maximum throughput of up to 50 kHz per channel in dual-channel operation, or 100 kHz in a single channel configuration. The CS5101A-16 can accept a maximum clock speed of 4 MHz, with corresponding throughput of 50 kHz. The CS5102A can operate with clock or crystal frequencies up to 2.0 MHz (1.6 MHz in FRN mode). This allows maximum throughput of up to 10 kHz per channel in dual-channel operation, or 20 kHz in a single channel configuration. For 16 bit performance

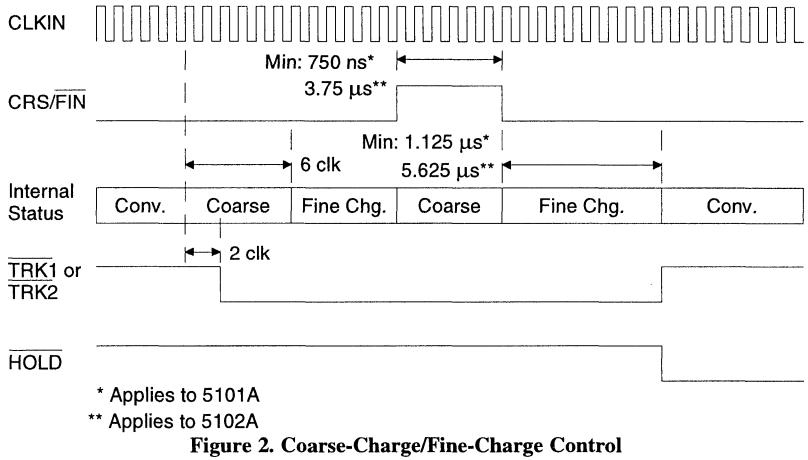


Figure 2. Coarse-Charge/Fine-Charge Control

a 1.6 MHz clock is recommended. This 1.6 MHz clock yields a maximum throughput of 20 kHz in a single channel configuration.

Asynchronous Sampling Considerations

When $\overline{\text{HOLD}}$ goes low, the analog sample is captured immediately. The $\overline{\text{HOLD}}$ signal is latched by the next falling edge of CLKIN, and conversion then starts on the subsequent rising edge. If $\overline{\text{HOLD}}$ is asynchronous to CLKIN, then there will be a 1.5 CLKIN cycle uncertainty as to when conversion starts. Considering the CS5101A with an 8 MHz CLKIN, with a 100 kHz HOLD signal, then this 1.5 CLKIN uncertainty will result in a 1.5 CLKIN period possible reduction in fine charge time for the next conversion.

Unipolar Input Voltage	Offset Binary	Two's Complement	Bipolar Input Voltage
>(VREF-1.5 LSB)	FFFF	7FFF	>(VREF-1.5 LSB)
VREF-1.5 LSB	FFFF FFFE	7FFF 7FFE	VREF-1.5 LSB
VREF/2-0.5 LSB	8000 7FFF	0000 FFFF	-0.5 LSB
+0.5 LSB	0001 0000	8001 8000	-VREF+0.5 LSB
<(+0.5 LSB)	0000	8000	<(-VREF+0.5 LSB)

Table 1. Output Coding

This reduced fine charge time will be less than the minimum specification. If the CLKIN frequency is increased slightly (for example, to 8.192 MHz) then sufficient fine charge time will always occur. The maximum frequency for CLKIN is specified at 9.216 MHz; it is recommended that for asynchronous operation at 100 kHz, CLKIN should be between 8.192 MHz and 9.216 MHz.

Analog Input Range/Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration ($\text{BP}/\overline{\text{UP}}$ low), the first code transition occurs 0.5 LSB above AGND, and the final code transition occurs 1.5 LSB's below VREF. In the bipolar configuration ($\text{BP}/\overline{\text{UP}}$ high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSB's below +VREF.

The CS5101A and CS5102A can output data in either 2's complement, or binary format. If the CODE pin is high, the output is in 2's complement format with a range of -32,768 to +32,767. If the CODE pin is low, the output is in binary format with a range of 0 to +65,535. See Table 1 for output coding.

MODE	SCKMOD	OUTMOD	SCLK	CH1/$\overline{2}$	$\overline{\text{HOLD}}$
PDT	1	1	Input	Input	Input
RBT	1	0	Input	Input	Input
SSC	0	1	Output	Input	Input
FRN	0	0	Output	Output	X

Table 2. Serial Output Modes

Output Mode Control

The CS5101A and CS5102A can be configured in three different output modes, as well as an internal, synchronous loop-back mode. This allows great flexibility for design into a wide variety of systems. The operating mode is selected by setting the states of the SCKMOD and OUTMOD pins. In all modes, data is output on SDATA, starting with the MSB. Each subsequent data bit is updated on the falling edge of SCLK.

When SCKMOD is high, SCLK is an input, allowing the data to be clocked out with an external serial clock at rates up to 5 MHz. Additional clock edges after #16 will clock out logic '1's on SDATA. Tying SCKMOD low reconfigures SCLK as an output, and the converter clocks out each bit as it's determined during the conversion process, at a rate of 1/4 the master clock speed. Table 2 shows an overview of the different states of SCKMOD and OUTMOD, and the corresponding output modes.

Pipelined Data Transmission (PDT)

PDT mode is selected by tying both SCKMOD and OUTMOD high. In PDT mode, the SCLK pin is an input. Data is registered during conversion, and output during the following conversion cycle. $\overline{\text{HOLD}}$ must be brought low, initiating another conversion, before data from the previous conversion is available on SDATA. If all the data has not been clocked out before the next falling edge of $\overline{\text{HOLD}}$, the old data will be lost (Figure 3).

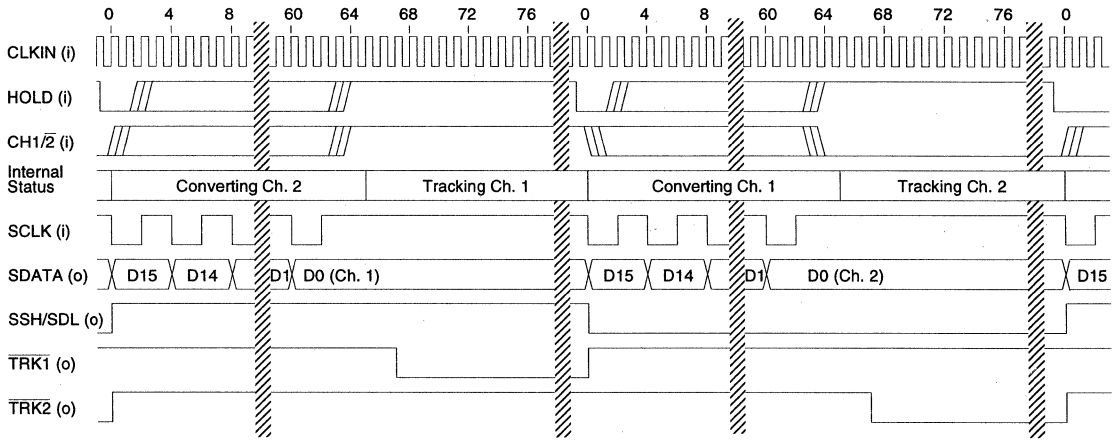


Figure 3. Pipelined Data Transmission Mode (PDT)

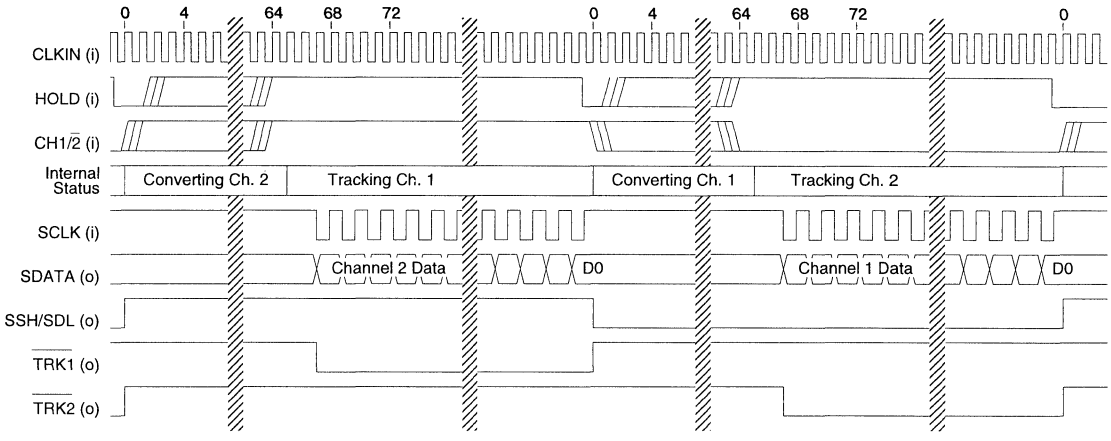


Figure 4. Registered Burst Transmission Mode (RBT)

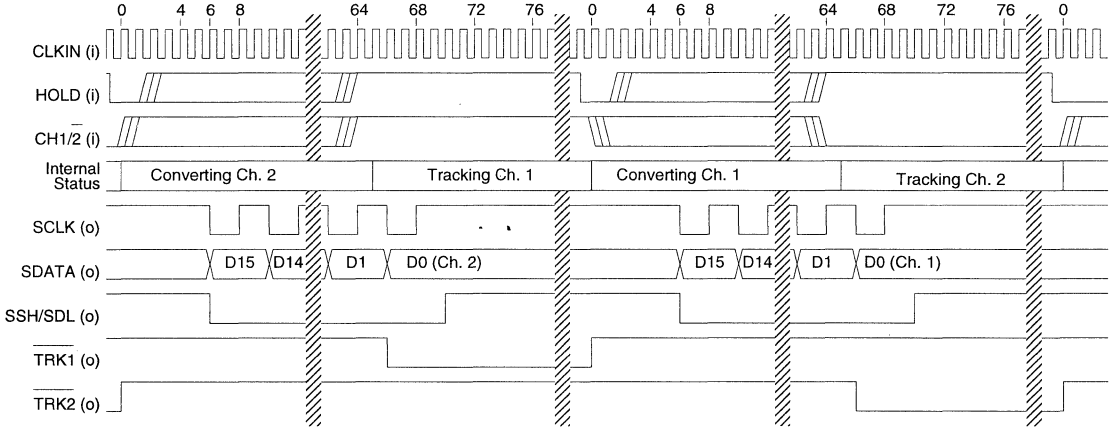


Figure 5. Synchronous Self-Clocking Mode (SSC)

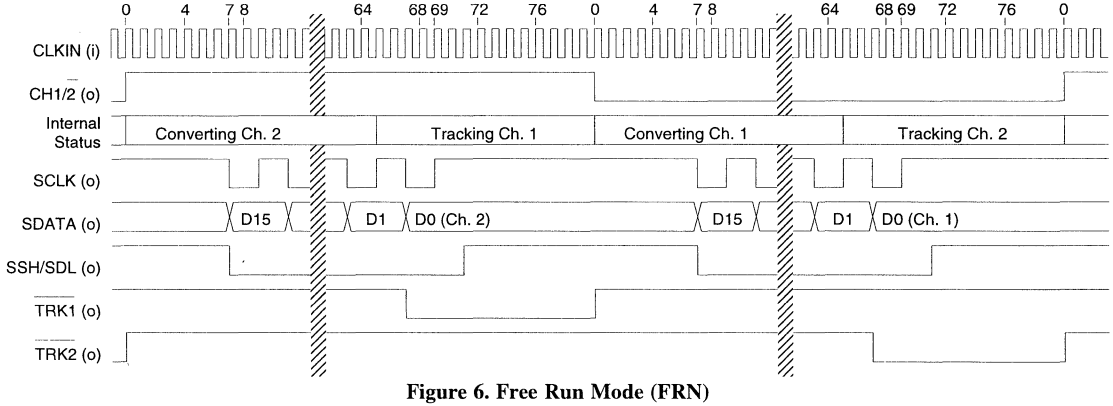


Figure 6. Free Run Mode (FRN)

Registered Burst Transmission (RBT)

RBT mode is selected by tying SCKMOD high, and OUTMOD low. As in PDT mode, SCLK is an input, however data is available immediately following conversion, and may be clocked out the moment $\overline{TRK1}$ or $\overline{TRK2}$ falls. *The falling edge of $\overline{HOLD}$ clears the output buffer*, so any unread data will be lost. A new conversion may be initiated before all the data has been clocked out if the unread data bits are not important (Figure 4).

Synchronous Self-Clocking (SSC)

SSC mode is selected by tying SCKMOD low, and OUTMOD high. In SSC mode, SCLK is an output, and will clock out each bit of the data as it's being converted. SCLK will remain high between conversions, and run at a rate of 1/4 the master clock speed for 16 low pulses during conversion (Figure 5).

The SSH/SDL goes low coincident with the first falling edge of SCLK, and returns high 2 CLKIN cycles after the last rising edge of SCLK. This signal frames the 16 data bits and is useful for interfacing to shift registers (e.g. 74HC595) or to DSP serial ports.

Free Run (FRN)

Free Run is the internal, synchronous loopback mode. FRN mode is selected by tying SCKMOD and OUTMOD low. SCLK is an output, and operates exactly the same as in the SSC mode. In Free Run mode, the converter initiates a new conversion every 80 master clock cycles, and alternates between channel 1 and channel 2. $\overline{HOLD}$ is disabled, and should be tied to either VD+ or DGND. CH1/$\overline{2}$ is an output, and will change at the start of each new conversion cycle, indicating which channel will be tracked after the current conversion is finished (Figure 6).

The SSH/SDL goes low coincident with the first falling edge of SCLK, and returns high 2 CLKIN cycles after the last rising edge of SCLK. This signal frames the 16 data bits and is useful for interfacing to shift registers (e.g. 74HC595) or to DSP serial ports.

SYSTEM DESIGN WITH THE CS5101A AND CS5102A

Figure 7 shows a general system connection diagram for the CS5101A and CS5102A.

Digital Circuit Connections

When TTL loads are utilized the potential for crosstalk between digital and analog sections of the system is increased. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

System Initialization

Upon power up, the CS5101A and CS5102A must be reset to guarantee a consistent starting condition and initially calibrate the device. Due to each device's low power dissipation and low temperature drift, no warm-up time is required before reset to accommodate any self-heating effects. However, the voltage reference input should have stabilized to within 0.25% of its final value before $\overline{RST}$ rises to guarantee an accurate calibration. Later, the CS5101A and CS5102A may be reset at any time to initiate a single full calibration.

When $\overline{RST}$ is brought low all internal logic clears. When $\overline{RST}$ returns high on the CS5101A, a calibration cycle begins which takes 11,528,160 master clock cycles to complete (approximately 1.4 seconds with an 8 MHz master clock). The calibration cycle on the CS5102A takes 2,882,040 master clock cycles to complete (ap-

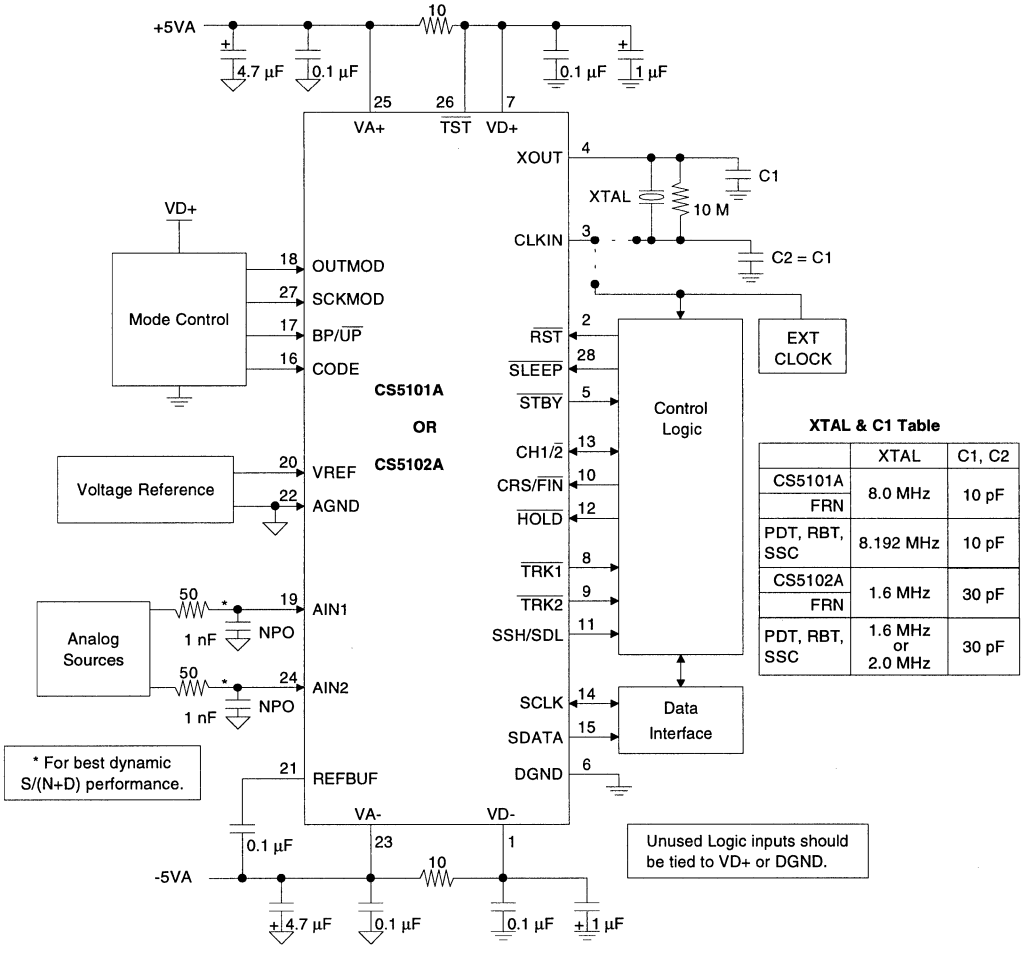


Figure 7. CS5101A/CS5102A System Connection Diagram

proximately 1.8 seconds with a 1.6 MHz master clock). The CS5101A's and CS5102A's $\overline{\text{STBY}}$ output remains low throughout the calibration sequence, and a rising transition indicates the device is ready for normal operation. While calibrating, the CS5101A and CS5102A will ignore changes on the $\overline{\text{HOLD}}$ input.

To perform the reset function, a simple power-on reset circuit can be built using a resistor and capacitor as shown in Figure 8. The resistor should be less than or equal to 10 kΩ. The system power supplies, voltage reference, and clock should all be established prior $\overline{\text{RST}}$ rising.

Single-Channel Operation

The CS5101A and CS5102A can alternatively be used to sample one channel by tying the CH1/$\overline{2}$ input high or low. The unused AIN pin should be tied to the analog input signal or to AGND. (If operating in free run mode, AIN1 and AIN2 must be tied to the same source, as CH1/$\overline{2}$ is reconfigured as an output.)

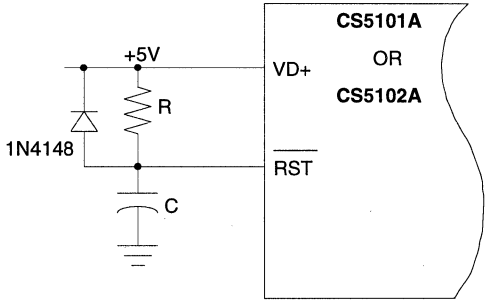


Figure 8. Power-up Reset Circuit

ANALOG CIRCUIT CONNECTIONS

Most popular successive approximation A/D converters generate dynamic loads at their analog connections. The CS5101A and CS5102A internally buffer all analog inputs (AIN1, AIN2, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

Reference Considerations

An application note titled "*Voltage References for the CS501X Series of A/D Converters*" is available for the CS5101A and CS5102A. In addition to working through a reference circuit design example, it offers several built-and-tested reference circuits.

During conversion, each capacitor of the calibrated capacitor array is switched between VREF and AGND in a manner determined by the successive-approximation algorithm. The charging and discharging of the array results in a current load at the reference. The CS5101A and CS5102A each include an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to coarse-charge the array thereby providing the bulk of the necessary charge. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer.

The external reference circuitry need only provide the residual charge required to fully charge the array after coarse-charging from the buffer. This creates an ac current load as the CS5101A and CS5102A sequence through conversions. The reference circuitry must have a low enough output impedance to drive the requisite current without changing its output voltage significantly. As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Therefore, the external reference must not exhibit significant peaking in its output impedance characteristic at signal frequencies or their harmonics.

A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum, while almost all precision references exhibit extremely low output impedance at dc. The presence of large capacitors on the output of some voltage references, however, may cause peaking in the output impedance at intermediate frequencies. Care should be exercised to ensure that significant peaking does not exist or that some form of compensation is provided to eliminate the effect.

The magnitude of the current load on the external reference circuitry will scale to the master clock frequency. At the full-rated 9.216 MHz clock (CS5101A), the reference must supply a maximum load current of 20 µA peak-to-peak (2 µA typical). An output impedance of 2 Ω will therefore yield a maximum error of 40 µV. At the full-rated 2.0 MHz clock (CS5102A), the reference must supply a maximum load current of 5 µA peak-to-peak (0.5 µA typical). An output impedance of 2 Ω will therefore yield a maxi-

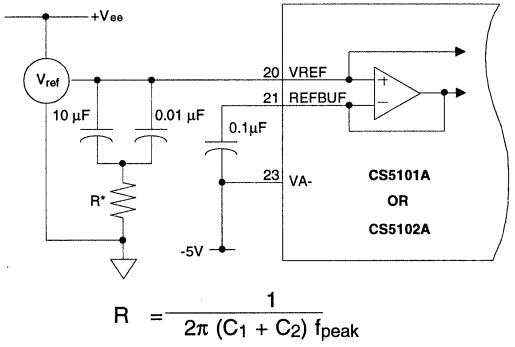


Figure 9. Reference Connections

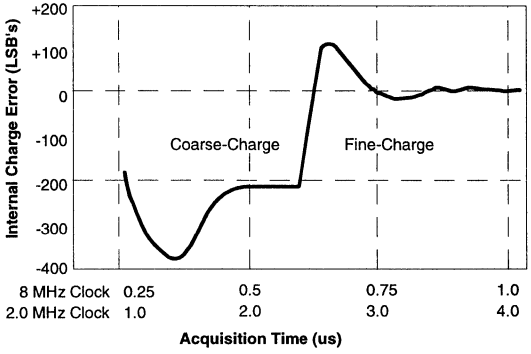


Figure 10. Charge Settling Time (8 and 2.0 MHz Clocks)

mum error of 10.0 µV. With a 4.5 V reference and LSB size of 138 µV this would insure approximately 1/14 LSB accuracy. A 10 µF capacitor exhibits an impedance of less than 2 Ω at frequencies greater than 16 kHz. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.

Peaking in the reference's output impedance can occur because of capacitive loading at its output. Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors. The equation in Figure 9 can be used to help calculate the optimum value of R for a particular reference. The term "f_{peak}" is the frequency of the peak in the output impedance of the reference before the resistor is added.

The CS5101A and CS5102A can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is 4.5 volts. The CS5101A and CS5102A can actually accept reference voltages up to the positive analog supply. However, the buffer's offset may increase as the reference voltage approaches VA+ thereby increasing external drive requirements at VREF. A 4.5V reference is the maximum reference voltage recommended. This allows 0.5V headroom for the internal reference buffer. Also, the buffer enlists the aid of an external 0.1 µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. For more information on references, consult "Application Note: *Voltage References for the CS501X Series of A/D Converters*".

Analog Input Connection

The analog input terminal functions similarly to the VREF input after each conversion when switching into the track mode. During the first six master clock cycles in the track mode, the buffered version of the analog input is used for coarse-charging the capacitor array. An additional period is required for fine-charging directly from AIN to obtain the specified accuracy. Figure 10 shows this operation. During coarse-charge the charge on the capacitor array first settles to the buffered version of the analog input. This voltage may be offset from the actual input voltage. During fine-charge, the charge then settles to the accurate unbuffered version.

Fine-charge settling is specified as a maximum of 1.125 µs (CS5101A) or 5.625 µs (CS5102A) for an analog source impedance of less than 50 Ω. In

addition, the comparator requires a source impedance of less than 400 Ω around 2 MHz for stability. The source impedance can be effectively reduced at high frequencies by adding capacitance from AIN to ground (typically 200 pF). However, high dc source resistances will increase the input's RC time constant and extend the necessary acquisition time. For more information on input amplifiers, consult the application note: *Buffer Amplifiers for the CS501X Series of A/D Converters.*

$\overline{\text{SLEEP}}$ Mode Operation

The CS5101A and CS5102A include a $\overline{\text{SLEEP}}$ pin. When $\overline{\text{SLEEP}}$ is active (low) each device will dissipate very low power to retain its calibration memory when the device is not sampling. It does not require calibration after $\overline{\text{SLEEP}}$ is made inactive (high). When coming out of $\overline{\text{SLEEP}}$, sampling can begin as soon as the oscillator starts (time will depend on the particular oscillator components) and the REFBUF capacitor is charged (which takes about 3 ms for the CS5101A, 50 ms for the CS5102A). To achieve minimum start-up time, use an external clock and leave the voltage reference powered-up. Connect a resistor (2 kΩ) between pins 20 and 21 to keep the REFBUF capacitor charged. Conversion can then begin as soon as the A/D circuitry has stabilized and performed a track cycle.

To retain calibration memory while $\overline{\text{SLEEP}}$ is active (low) VA+ and VD+ must be maintained at greater than 2.0V. VA- and VD- can be allowed to go to 0 volts. The voltages into VA- and VD- cannot just be "shut-off" as these pins cannot be allowed to float to potentials greater than AGND/DGND. If the supply voltages to VA- and VD- are removed, use a transistor switch to short these to the power supply ground while in $\overline{\text{SLEEP}}$ mode.

Grounding and Power Supply Decoupling

The CS5101A and CS5102A use the analog ground connection, AGND, only as a reference voltage. No dc power currents flow through the AGND connection, and it is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both the analog input and reference voltage should be referred to the AGND pin, which should be used as the entire system's analog ground reference.

The digital and analog supplies are isolated within the CS5101A and CS5102A and are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1 µF ceramic capacitors. If significant low-frequency noise is present on the supplies, tantalum capacitors are recommended in parallel with the 0.1 µF capacitors.

The positive digital power supply of the CS5101A and CS5102A must never exceed the positive analog supply by more than a diode drop or the CS5101A and CS5102A could experience permanent damage. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagram (Figure 7) shows a decoupling scheme which allows the CS5101A and CS5102A to be powered from a single set of ± 5V rails. The positive digital supply is derived from the analog supply through a 10 Ω resistor to avoid the analog supply dropping below the digital supply. If this scheme is utilized, care must be taken to insure that any digital load currents (which flow through the 10 Ω resistors) do not cause the magnitude of digital supplies to drop below the analog supplies by more than 0.5 volts. Digital supplies must always remain above the minimum specification.

As with any high-precision A/D converter, the CS5101A and CS5102A require careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the devices. The CDB5101A evaluation board is available for the CS5101A, and the CDB5102A evaluation board is available for the CS5102A. The availability of these boards avoids the need to design, build, and debug a high-precision PC board to initially characterize the part. Each board comes with a socketed CS5101A or CS5102A, and can be reconfigured to simulate any combination of sampling, calibration, master clock, and analog input range conditions.

CS5101A AND CS5102A PERFORMANCE

Differential Nonlinearity

The self-calibration scheme utilized in the CS5101A and CS5102A features a calibration resolution of 1/4 LSB, or 18-bits. This ideally yields DNL of ±1/4 LSB, with code widths ranging from 3/4 to 5/4 LSB's.

Traditional laser trimmed ADC's have significant differential nonlinearities. Appearing as wide and narrow codes, DNL often causes entire sections of the transfer function to be missing. Although their affect is minor on S/(N+D) with high amplitude signals, DNL errors dominate performance with low-level signals. For instance, a signal 80 dB below full-scale will slew past only 6 or 7 codes. Half of those codes could be missing with a conventional 16-bit ADC which achieves only 14-bit DNL.

The most common source of DNL errors in conventional ADC's is bit weight errors. These can arise due to accuracy limitations in factory trim stations, thermal or physical stresses after calibration, and/or drifts due to aging or temperature variations in the field. Bit-weight errors have a drastic effect on a converter's ac performance. They can be analyzed as step functions superimposed on the input signal. Since bits (and their errors) switch in and out throughout the transfer curve, their effect is signal dependent. That is, harmonic and intermodulation distortion, as well as noise, can vary with different input conditions.

Differential nonlinearities in successive-approximation ADC's also arise due to dynamic errors in the comparator. Such errors can dominate if the converter's throughput/sampling rate is too high. The comparator will not be allowed sufficient time to settle during each bit decision in the successive-approximation algorithm. The worst-case codes for dynamic errors are the major transitions (1/2 FS; 1/4, 3/4 FS; etc.). Since DNL effects are most critical with low-level signals, the codes around mid-scale (1/2 FS) are most important. Yet those codes are worst-case for dynamic DNL errors!

With all linearity calibration performed on-chip to 18-bits, the CS5101A and CS5102A maintain accurate bit weights. DNL errors are dominated by residual calibration errors of ±1/4 LSB rather than dynamic errors in the comparator. Furthermore, *all* DNL effects on S/(N+D) are buried by white broadband noise. (See Figures 17 and 19).

Figure 11 illustrates the DNL histogram plot of a typical CS5101A at 25°C. Figure 12 illustrates the DNL of the CS5101A at 138°C ambient after calibration at 25°C ambient. Figures 13 and 14 illustrate the DNL of the CS5102A at 25°C and 138°C ambient, respectively. A histogram test is a statistical method of deriving an A/D converter's differential nonlinearity. A ramp is input to the A/D and a large number of samples are taken to insure a high confidence level in the test's result. The number of occurrences for each code is monitored and stored. A perfect A/D converter would have all codes of equal size and therefore equal numbers of occurrences. In the histogram test a code with the average number of occurrences will be considered ideal (DNL = 0). A

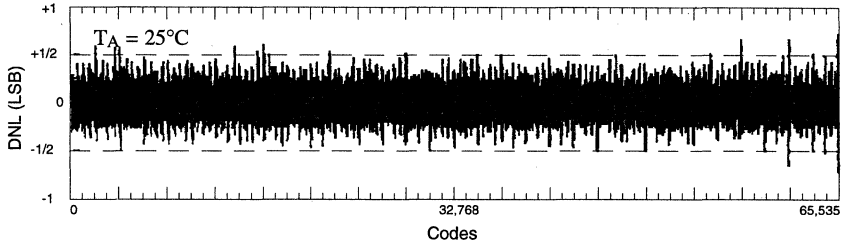


Figure 11. CS5101A DNL Plot; Ambient Temperature at 25°C

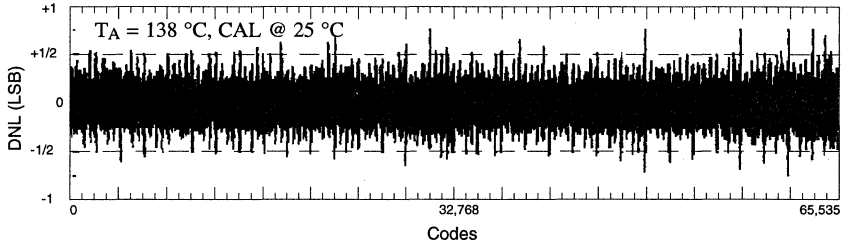


Figure 12. CS5101A DNL Plot; Ambient Temperature at 138°C

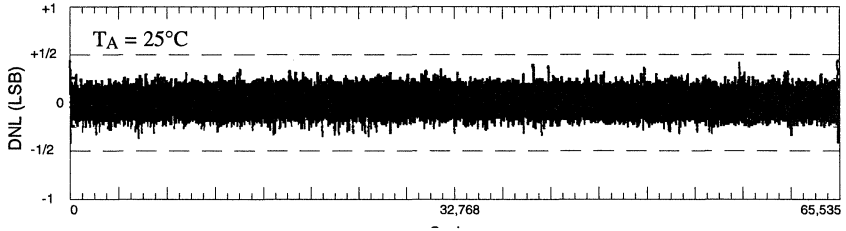


Figure 13. CS5102A DNL Plot; Ambient Temperature at 25°C

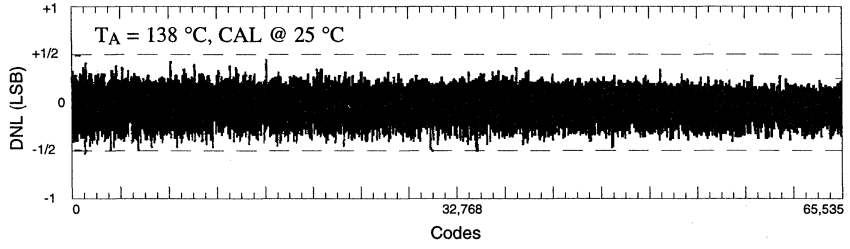


Figure 14. CS5102A DNL Plot; Ambient Temperature at 138°C

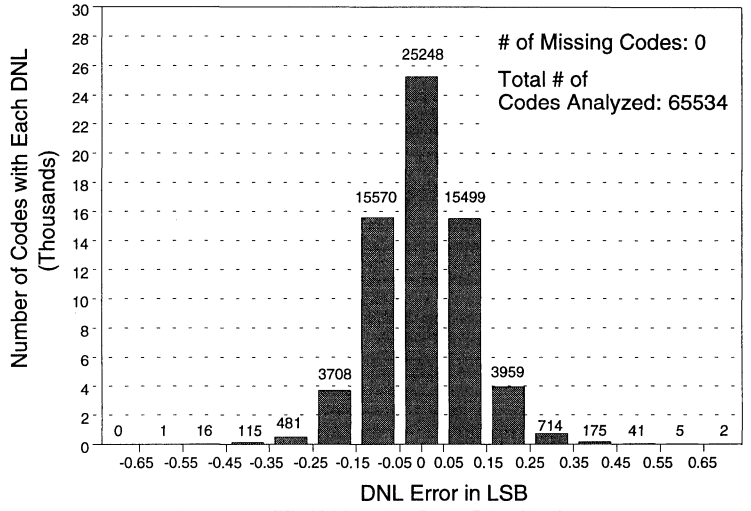


Figure 15. CS5101A DNL Error Distribution

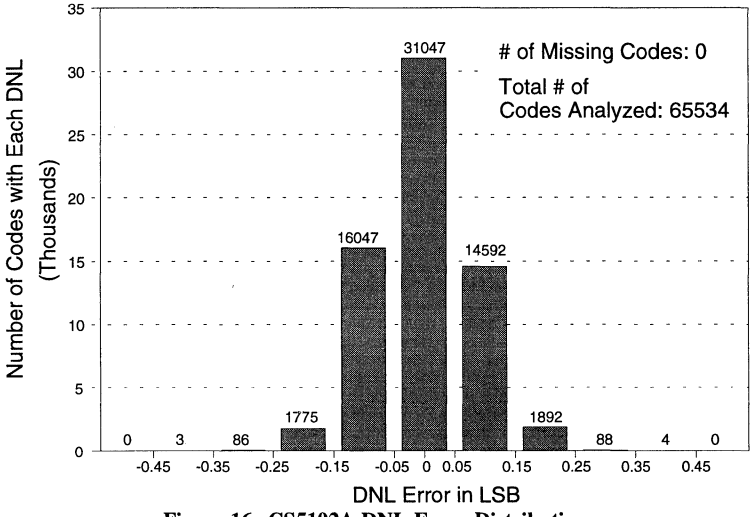


Figure 16. CS5102A DNL Error Distribution

code with more or less occurrences than average will appear as a DNL of greater or less than zero LSB. A missing code has zero occurrences, and will appear as a DNL of -1 LSB.

Figures 15 and 16 illustrate the code width distribution of the DNL plots shown in Figures 11 and 13 respectively. The DNL error distribution plots indicate that the CS5101A and CS5102A calibrate the majority of their codes to tighter tolerance than the DNL plots in Figures 11 and 13 appear to indicate.

FFT Tests and Windowing

In the factory, the CS5101A and CS5102A are tested using Fast Fourier Transform (FFT) techniques to analyze the converters' dynamic performance. A pure sinewave is applied to the device, and a "time record" of 1024 samples is

captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins." Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and dc can only be due to quantization effects and errors in the CS5101A and CS5102A.

If sampling is not synchronized to the input sinewave, it is highly unlikely that the time record will contain an integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a window function prior to performing the FFT. The window function smoothly forces the endpoints of the time record to zero, thereby removing the discontinuities. The effect of the window in the frequency-domain is to convolute the spectrum of the window with that of the actual input.

The quality of the window used for harmonic analysis is typically judged by its highest side-lobe level. A five term window is used in FFT testing of the CS5101A and CS5102A. This windowing algorithm attenuates the side-lobes to below the noise floor. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that quantization noise is white. Averaging the FFT results from ten time records filters the spectral variability that can arise from capturing finite time records without disturbing the total energy outside the fundamental. All harmonics are visible in the plots. For more information on FFT's and windowing refer to: F.J. HARRIS, "On the use of windows for harmonic analysis with the Discrete Fourier Transform", Proc. IEEE, Vol. 66, No. 1, Jan 1978, pp.51-83. This is available on request from Crystal Semiconductor.

As illustrated in Figure 17, the CS5101A typically provides about 92 dB S/(N+D) and 0.001% THD at 25°C. Figure 18 illustrates only minor degradation in performance when the ambient temperature is raised to 138°C. Figure 19 and 20 illustrate that the CS5102A typically yields >92 dB S/(N+D) and 0.001% THD even with a large change in ambient temperature. Unlike conventional successive-approximation ADC's, the signal-to-noise and dynamic range of the CS5101A and CS5102A are not limited by differential nonlinearities (DNL) caused by calibration errors. Rather, the dominant noise source is broadband thermal noise which aliases into the baseband. This *white* broadband noise also appears as an idle channel noise of 1/2 LSB (rms).

Sampling Distortion

Like most discrete sample/hold amplifier designs, the inherent sample/hold of the CS5101A and CS5102A exhibits a frequency-dependent distortion due to nonideal sampling of the analog input voltage. The calibrated capacitor array used during conversions is also used to track and hold the analog input signal. The conversion is not performed on the analog input voltage per se, but is actually performed on the charge trapped on the capacitor array at the moment the $\overline{\text{HOLD}}$ command is given. The charge on the array ideally assumes a linear relationship to the analog input voltage. Any deviation from this linear relationship will result in conversion errors even if the conversion process proceeds flawlessly.

At dc, the DAC capacitor array's voltage coefficient dictates the converter's linearity. This variation in capacitance with respect to applied signal voltage yields a nonlinear relationship between the charge on the array and the analog input voltage and places a bow or wave in the transfer function. This is the dominant source of distortion at low input frequencies (Figures 17,18,19, and 20).

The ideal relationship between the charge on the array and the input voltage can also be distorted

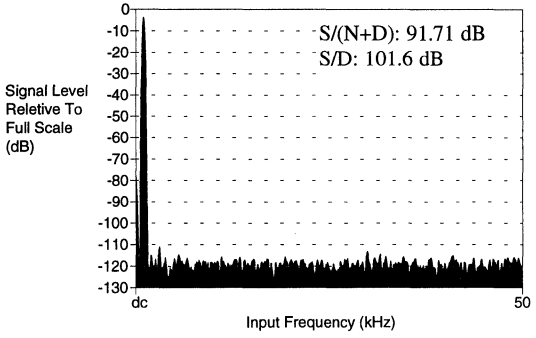


Figure 17. CS5101A FFT (SSC Mode, 1-Channel)

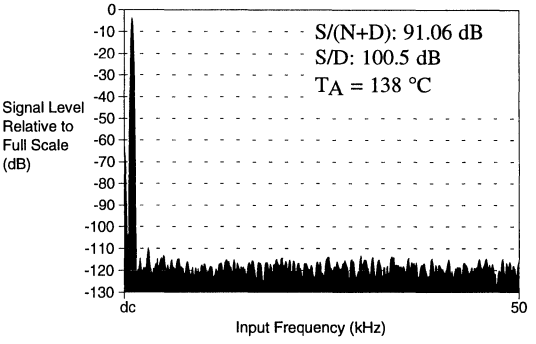


Figure 18. CS5101A FFT (SSC Mode, 1-Channel)

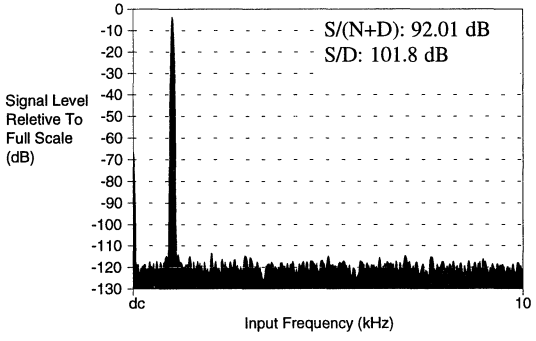


Figure 19. CS5102A FFT (SSC Mode, 1-Channel)

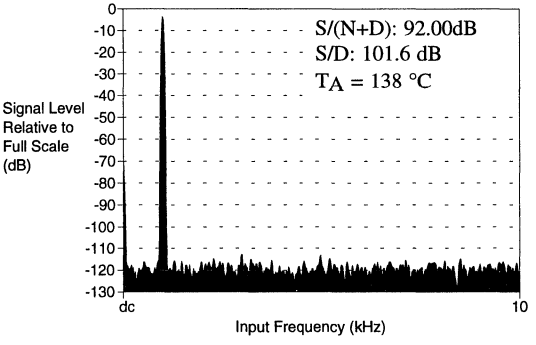


Figure 20. CS5102A FFT (SSC Mode, 1-Channel)

at high signal frequencies due to nonlinearities in the internal MOS switches. Dynamic signals cause ac current to flow through the switches connecting the capacitor array to the analog input pin in the track mode. Nonlinear on-resistance in the switches causes a nonlinear voltage drop. This effect worsens with increased signal frequency and slew rate. This distortion is negligible at signal levels below -10 dB of full-scale.

Noise

An A/D converter's noise can be described like that of any other analog component. However, the converter's output is in digital form so any filtering of its noise must be performed in the digital domain. Digitized samples of analog inputs are often considered individual, static snapshots in time with no uncertainty or noise. In reality, the result of each conversion depends on the analog input level and the instantaneous value of noise sources in the ADC. If sequential samples from the ADC are treated as a "waveform", simple filtering can be implemented in software to improve noise performance with minimal processing overhead.

All analog circuitry in the CS5101A and CS5102A is wideband in order to achieve fast conversions and high throughput. Wideband noise in the CS5101A and CS5102A integrates to 35 µV rms in unipolar mode (70 µV rms in bipolar mode). This is approximately 1/2 LSB rms with a 4.5V reference in both modes. Figure 21 shows a

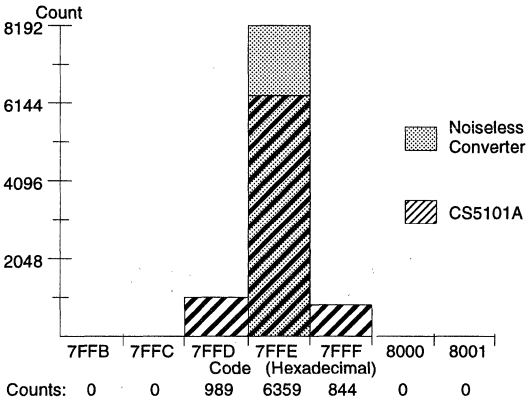


Figure 21. 5101A Histogram Plot of 8192 Conversion Inputs

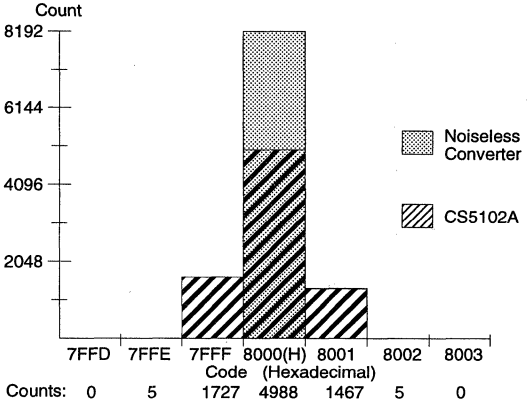


Figure 22. 5102A Histogram Plot of 8192 Conversion Inputs

histogram plot of output code occurrences obtained from 8192 samples taken from a CS5101A in the bipolar mode. Hexadecimal code 7FFE was arbitrarily selected and the analog input was set close to code center. With a noiseless converter, code 7FFE would always appear. The histogram plot of the device has a "bell" shape with all codes other than 7FFE due to internal noise. Figure 22 illustrates the noise histogram of the CS5102A.

In a sampled data system all information about the analog input applied to the sample/hold appears in the baseband from dc to one-half the sampling rate. This includes high-frequency components which alias into the baseband. Low-pass (anti-alias) filters are therefore used to remove frequency components in the input signal which are above one-half the sample rate. However, all wideband noise introduced by the CS5101A and CS5102A still aliases into the baseband. This "white" noise is evenly spread from dc to one-half the sampling rate and integrates to 35 μV rms in unipolar mode.

Noise in the digital domain can be reduced by sampling at higher than the desired word rate and averaging multiple samples for each word. Oversampling spreads the device's noise over a wider band (for lower noise density), and averaging applies a low-pass response which filters noise above the desired signal bandwidth. In general, the device's noise performance can be maximized in any application by always sampling at the maximum specified rate of 100 kHz (CS5101A) or 20 kHz (CS5102A) (for lowest noise density) and digitally filtering to the desired signal bandwidth.

Aperture Jitter

Track-and-hold amplifiers commonly exhibit two types of aperture jitter. The first, more appropriately termed "aperture window", is an input voltage dependent variation in the aperture delay. Its signal-dependency causes distortion at high frequencies. The proprietary architecture of the CS5101A and CS5102A avoids applying the input voltage across a sampling switch, thus avoiding any "aperture window" effects. The second type of aperture jitter, due to component noise, assumes a random nature. With only 100 ps peak-to-peak aperture jitter, the CS5101A and CS5102A can process full-scale signals up to

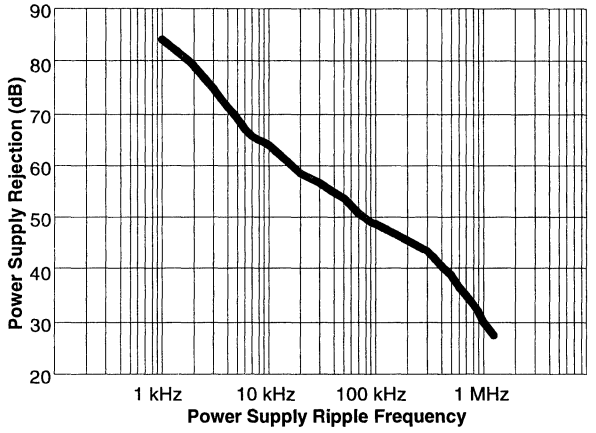


Figure 23. Power Supply Rejection

1/2 the throughput frequency without significant errors due to aperture jitter.

Power Supply Rejection

The power supply rejection performance of the CS5101A and CS5102A is enhanced by the on-chip self-calibration and an "auto-zero" process. Drifts in power supply voltages at frequencies less than the calibration rate have negligible effect on the device's accuracy. This is because the CS5101A and CS5102A adjust their offset to within a small fraction of an LSB during calibration. Above the calibration frequency the excellent power supply rejection of the internal amplifiers is augmented by an auto-zero process. Any offsets are stored on the capacitor array and are effectively subtracted once conversion is initiated. Figure 23 shows power supply rejection of the CS5101A and CS5102A in the bipolar mode with the analog input grounded and a 300 mV p-p ripple applied to each supply. Power supply rejection improves by 6 dB in the unipolar mode.

CS5101A/CS5102A Improvements Over Earlier CS5101/CS5102

The CS5101A/CS5102A are improved versions of the earlier CS5101/CS5102 devices. Primary improvements are:

1) Improved DNL at high temperature (>70 °C)

2) Improved input slew rate, yielding improved full scale settling between conversions.

3) Modifying the previous SSH pin to SSH/SDL (Simultaneous Sample Hold/Serial Data Latch). The SSH/SDL new function provides a logic signal which frames the 16 data bits in SSC and FRN serial modes. This signal is ideal for easy interface to serial to parallel shift registers (74HC595) and to DSP serial ports.

Table 3 summarizes all the improvements.

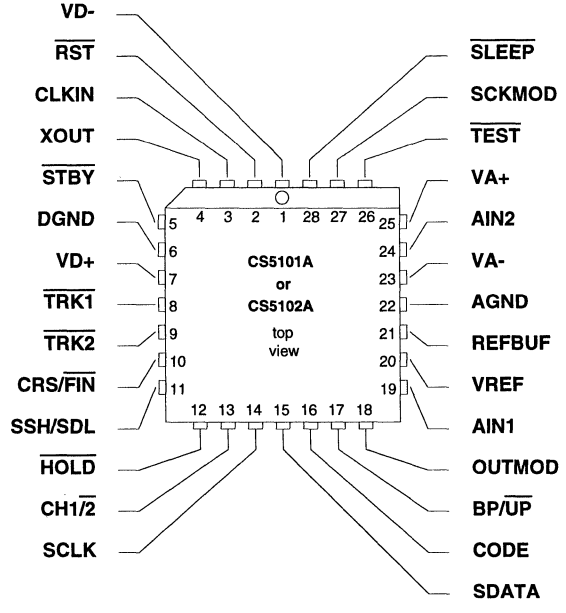
Function	CS5101A/CS5102A	CS5101/CS5102
Better DNL	No missing codes at +125 °C	Some missed codes at +125 °C
Faster Fine Charge Slew Rate (V/µs)	CS5101A / CS5102A Unipolar/Fine: 2 / 0.4 Bipolar/Fine: 4 / 0.8	CS5101 / CS5102 Unipolar/Fine: 1.3 / 0.1 Bipolar/Fine: 2.6 / 0.2
Improved Serial Interface	Has serial data latch signal (SSH/SDL).	Does not have serial data latch (SDL) signal.
CLKIN Rate	CS5101A maximum CLKIN is 9.216 MHz CS5102A maximum CLKIN is 2.0 MHz	CS5101 maximum CLKIN is 8.0 MHz CS5102 maximum CLKIN is 1.6 MHz
Code and BP/$\overline{UP}$ Pin Function	Independent setting of 2's complement or offset binary coding (CODE) and bipolar or unipolar input range (BP/$\overline{UP}$)	Selecting unipolar input range forces offset binary operation, independent of the CODE pin state
CRS/$\overline{FIN}$ Pin	Can be high or low during calibration	CRS/$\overline{FIN}$ must be held low during calibration

Table 3. CS5101A/CS5102A Improvements over CS5101/CS5102

PIN DESCRIPTIONS

NEGATIVE DIGITAL POWER	VD-	1	28	SLEEP	SLEEP (LOW POWER) MODE
RESET & INITIATE CALIBRATION	RST	2	27	SCKMOD	SERIAL CLOCK MODE SELECT
MASTER CLOCK INPUT	CLKIN	3	26	TEST	TEST
CRYSTAL OUTPUT	XOUT	4	25	VA+	POSITIVE ANALOG POWER
STANDBY (CALIBRATING)	STBY	5	24	AIN2	CHANNEL 2 ANALOG INPUT
DIGITAL GROUND	DGND	6	23	VA-	NEGATIVE ANALOG POWER
POSITIVE DIGITAL POWER	VD+	7	22	AGND	ANALOG GROUND
TRACKING CHANNEL 1	TRK1	8	21	REFBUF	REFERENCE BUFFER
TRACKING CHANNEL 2	TRK2	9	20	VREF	VOLTAGE REFERENCE
COARSE/FINE CHARGE CONTROL	CRS/FIN	10	19	AIN1	CHANNEL 1 ANALOG INPUT
SIMULTANEOUS S/H / SERIAL DATA LATCH	SSH/SDL	11	18	OUTMOD	OUTPUT MODE SELECT
HOLD & CONVERT	HOLD	12	17	BP/UP	BIPOLAR/UNIPOLAR SELECT
INPUT CHANNEL SELECT	CH1/2	13	16	CODE	BINARY/2's COMPLEMENT SELECT
SERIAL DATA CLOCK	SCLK	14	15	SDATA	SERIAL DATA OUTPUT

CS5101A or CS5102A



Power Supply Connections

VD+ - Positive Digital Power, PIN 7.
Positive digital power supply. Nominally +5 volts.

VD- - Negative Digital Power, PIN 1.
Negative digital power supply. Nominally -5 volts.

DGND - Digital Ground, PIN 6.
Digital ground [reference].

VA+ - Positive Analog Power, PIN 25.
Positive analog power supply. Nominally +5 volts.

VA- - Negative Analog Power, PIN 23.
Negative analog power supply. Nominally -5 volts.

AGND - Analog Ground, PIN 22.
Analog ground reference.

Oscillator

CLKIN - Clock Input, PIN 3.
All conversions and calibrations are timed from a master clock which can be externally supplied by driving CLKIN [this input TTL-compatible, CMOS recommended].

XOUT - Crystal Output, PIN 4.
The master clock can be generated by tying a crystal across the CLKIN and XOUT pins. If an external clock is used, XOUT must be left floating.

Digital Inputs

$\overline{\text{HOLD}}$ - Hold, PIN 12.
A falling transition on this pin sets the CS5101A or CS5102A to the hold state and initiates a conversion. This input must remain low for at least 1/tclk + 20 ns. When operating in Free Run Mode, $\overline{\text{HOLD}}$ is disabled, and should be tied to DGND or VD+.

CRS/$\overline{\text{FIN}}$ - Coarse Charge/Fine Charge Control, PIN 10.
When brought high during acquisition time, CRS/$\overline{\text{FIN}}$ forces the CS5101A or CS5102A into coarse charge state. This engages the internal buffer amplifier to track the analog input and charges the capacitor array much faster, thereby allowing the CS5101A or CS5102A to track high slewing signals. In order to get an accurate sample, the last coarse charge period before initiating a conversion (bringing $\overline{\text{HOLD}}$ low) must be longer than 0.75 µs (CS5101A) or 3.75 µs (CS5102A). Similarly, the fine charge period immediately prior to conversion must be at least 1.125 µs (CS5101A) or 5.625 µs (CS5102A). The CRS/$\overline{\text{FIN}}$ pin must be low during conversion time. For normal operation, CRS/$\overline{\text{FIN}}$ should be tied low, in which case the CS5101A or CS5102A will automatically enter coarse charge for 6 clock cycles immediately after the end of conversion.

CH1/$\overline{2}$ - Left/Right Input Channel Select, PIN 13.

Status at the end of a conversion cycle determines which analog input channel will be acquired for the next conversion cycle. When in Free Run Mode, CH1/$\overline{2}$ is an output, and will indicate which channel is being sampled during the current acquisition phase.

$\overline{\text{SLEEP}}$ - Sleep, PIN 28.

When brought low causes the CS5101A or CS5102A to enter a power-down state. All calibration coefficients are retained in memory, so no recalibration is needed after returning to the normal operating mode. If using the internal crystal oscillator, time must be allowed after $\overline{\text{SLEEP}}$ returns high for the crystal oscillator to stabilize. $\overline{\text{SLEEP}}$ should be tied high for normal operation.

CODE - 2's Complement/Binary Coding Select, PIN 16.

Determines whether output data appears in 2's complement or binary format. If high, 2's complement; if low, binary.

BP/$\overline{\text{UP}}$ - Bipolar/Unipolar Input Range Select, PIN 17.

When low, the CS5101A or CS5102A accepts a unipolar input range from AGND to VREF. When high, the CS5101A or CS5102A accepts bipolar inputs from -VREF to +VREF.

SCKMOD - Serial Clock Mode Select, PIN 27.

When high, the SCLK pin is an input; when low, it is an output. Used in conjunction with OUTMOD to select one of 4 output modes described in Table 2.

OUTMOD - Output Mode Select, PIN 18.

The status of SCKMOD and OUTMOD determine which of four output modes is utilized. The four modes are described in Table 2.

SCLK - Serial Clock, PIN 14.

Serial data changes status on a falling edge of this input, and is valid on a rising edge. When SCKMOD is high SCLK acts as an input. When SCKMOD is low the CS5101A or CS5102A generates its own serial clock at one-fourth the master clock frequency and SCLK is an output.

$\overline{\text{RST}}$ - Reset, PIN 2.

When taken low, all internal digital logic is reset. Upon returning high, a full calibration sequence is initiated which takes 11,528,160 CLKIN cycles (CS5101A) or 2,882,040 CLKIN cycles (CS5102A) to complete. During calibration, the $\overline{\text{HOLD}}$ input will be ignored. The CS5101A or CS5102A must be reset at power-up for calibration, however; calibration is maintained during $\overline{\text{SLEEP}}$ mode, and need not be repeated when resuming normal operation.

Analog Inputs

AIN1, AIN2 - Channel 1 and 2 Analog Inputs, PINS 19 and 24.

Analog input connections for the left and right input channels.

VREF - Voltage Reference, PIN 20.

The analog reference voltage which sets the analog input range. In unipolar mode VREF sets full-scale; in bipolar mode its magnitude sets both positive and negative full-scale.

Digital Outputs

$\overline{\text{STBY}}$ - Standby (Calibrating), PIN 5.

Indicates calibration status after reset. Remains low throughout the calibration sequence and returns high upon completion.

SDATA - Serial Output, PIN 15.

Presents each output data bit on a falling edge of SCLK. Data is valid to be latched on the rising edge of SCLK.

SSH/SDL - Simultaneous Sample/Hold / Serial Data Latch, PIN 11.

Used to control an external sample/hold amplifier to achieve simultaneous sampling between channels. In FRN and SSC modes (SCLK is an output), this signal provides a convenient latch signal which forms the 16 data bits. This can be used to control external serial to parallel latches, or to control the serial port in a DSP.

$\overline{\text{TRK1}}$, $\overline{\text{TRK2}}$ - Tracking Channel 1, Tracking Channel 2, PINS 8 and 9.

Falls low at the end of a conversion cycle, indicating the acquisition phase for the corresponding channel. The $\overline{\text{TRK1}}$ or $\overline{\text{TRK2}}$ pin will return high at the beginning of conversion for that channel.

Analog Outputs

REFBUF - Reference Buffer Output, PIN 21.

Reference buffer output. A 0.1 µF ceramic capacitor must be tied between this pin and VA-.

Miscellaneous

$\overline{\text{TEST}}$ - Test, PIN 26.

Allows access to the CS5101A's and the CS5102A's test functions which are reserved for factory use. Must be tied to VD+.

PARAMETER DEFINITIONS

Linearity Error

The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in % Full-Scale.

Differential Linearity

Minimum resolution for which no missing codes is guaranteed. Units in bits.

Full Scale Error

The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSB's.

Unipolar Offset

The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/UP low). Units in LSB's.

Bipolar Offset

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSB's.

Bipolar Negative Full-Scale Error

The deviation of the first code transition from the ideal when in bipolar mode (BP/$\overline{UP}$ high). The ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSB's.

Signal to Peak Harmonic or Noise

The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Expressed in decibels.

Total Harmonic Distortion

The ratio of the rms sum of all harmonics to the rms value of the signal. Units in percent.

Signal-to-(Noise + Distortion)

The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels.

Aperture Time

The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter

The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

CS5101A Ordering Guide

Model	Conversion Time	Throughput	Linearity	Temperature	Package
CS5101A-JP8	8.13 µs	100 kHz	0.003%	0 to 70 °C	28-Pin Plastic DIP
CS5101A-KP8	8.13 µs	100 kHz	0.002%	0 to 70 °C	28-Pin Plastic DIP
CS5101A-JP16	16.25 µs	50 kHz	0.003%	0 to 70 °C	28-Pin Plastic DIP
CS5101A-JL8	8.13 µs	100 kHz	0.003%	0 to 70 °C	28-Pin PLCC
CS5101A-KL8	8.13 µs	100 kHz	0.002%	0 to 70 °C	28-Pin PLCC
CS5101A-JL16	16.25 µs	50 kHz	0.003%	0 to 70 °C	28-Pin PLCC
CS5101A-AP8	8.13 µs	100 kHz	0.003%	-40 to 85 °C	28-Pin Plastic DIP
CS5101A-BP8	8.13 µs	100 kHz	0.002%	-40 to 85 °C	28-Pin Plastic DIP
CS5101A-AL8	8.13 µs	100 kHz	0.003%	-40 to 85 °C	28-Pin PLCC
CS5101A-BL8	8.13 µs	100 kHz	0.002%	-40 to 85 °C	28-Pin PLCC
CS5101A-SD8	8.13 µs	100 kHz	0.004%	-55 to 125 °C	28-Pin CerDIP
CS5101A-TD8	8.13 µs	100 kHz	0.003%	-55 to 125 °C	28-Pin CerDIP
CS5101A-SE8	8.13 µs	100 kHz	0.004%	-55 to 125 °C	28-Pin LCC
CS5101A-TE8	8.13 µs	100 kHz	0.003%	-55 to 125 °C	28-Pin LCC
5962-9169101MXA	8.13 µs	100 kHz	0.004%	-55 to 125 °C	28-Pin CerDIP
5962-9169102MXA	8.13 µs	100 kHz	0.003%	-55 to 125 °C	28-Pin CerDIP
5962-9169101M3A	8.13 µs	100 kHz	0.004%	-55 to 125 °C	28-Pin LCC
5962-9169102M3A	8.13 µs	100 kHz	0.003%	-55 to 125 °C	28-Pin LCC

Discontinued Part Number	Equivalent Recommended Device
CS5101A-SD8B	5962-9169101MXA
CS5101A-TD8B	5962-9169102MXA
CS5101A-SE8B	5962-9169101M3A
CS5101A-TE8B	5962-9169102M3A

CS5102A Ordering Guide

Model	Conversion Time	Throughput	Linearity	Temperature	Package
CS5102A-JP	40 µs	20 kHz	0.003%	0 to 70 °C	28-Pin Plastic DIP
CS5102A-KP	40 µs	20 kHz	0.0015%	0 to 70 °C	28-Pin Plastic DIP
CS5102A-JL	40 µs	20 kHz	0.003%	0 to 70 °C	28-Pin PLCC
CS5102A-KL	40 µs	20 kHz	0.0015%	0 to 70 °C	28-Pin PLCC
CS5102A-AP	40 µs	20 kHz	0.003%	-40 to 85 °C	28-Pin Plastic DIP
CS5102A-BP	40 µs	20 kHz	0.0015%	-40 to 85 °C	28-Pin Plastic DIP
CS5102A-AL	40 µs	20 kHz	0.003%	-40 to 85 °C	28-Pin PLCC
CS5102A-BL	40 µs	20 kHz	0.0015%	-40 to 85 °C	28-Pin PLCC
CS5102A-SD	40 µs	20 kHz	0.004%	-55 to 125 °C	28-Pin CerDIP
CS5102A-TD	40 µs	20 kHz	0.002%	-55 to 125 °C	28-Pin CerDIP
CS5102A-SE	40 µs	20 kHz	0.004%	-55 to 125 °C	28-Pin LCC
CS5102A-TE	40 µs	20 kHz	0.002%	-55 to 125 °C	28-Pin LCC
5962-9169201MXA	40 µs	20 kHz	0.004%	-55 to 125 °C	28-Pin CerDIP
5962-9169202MXA	40 µs	20 kHz	0.002%	-55 to 125 °C	28-Pin CerDIP
5962-9169201M3A	40 µs	20 kHz	0.004%	-55 to 125 °C	28-Pin LCC
5962-9169202M3A	40 µs	20 kHz	0.002%	-55 to 125 °C	28-Pin LCC

Discontinued Part Number	Equivalent Recommended Device
CS5102A-SDB	5962-9169201MXA
CS5102A-TDB	5962-9169202MXA
CS5102A-SEB	5962-9169201M3A
CS5102A-TEB	5962-9169202M3A

Semiconductor Corporation

CDB5101A/5102A

Evaluation Board for CS5101A & CS5102A

Features

- Serial to Parallel Conversion
- Adjustable Voltage Reference
- ± 5 V Regulators
- Digital and Analog Patch Areas

General Description

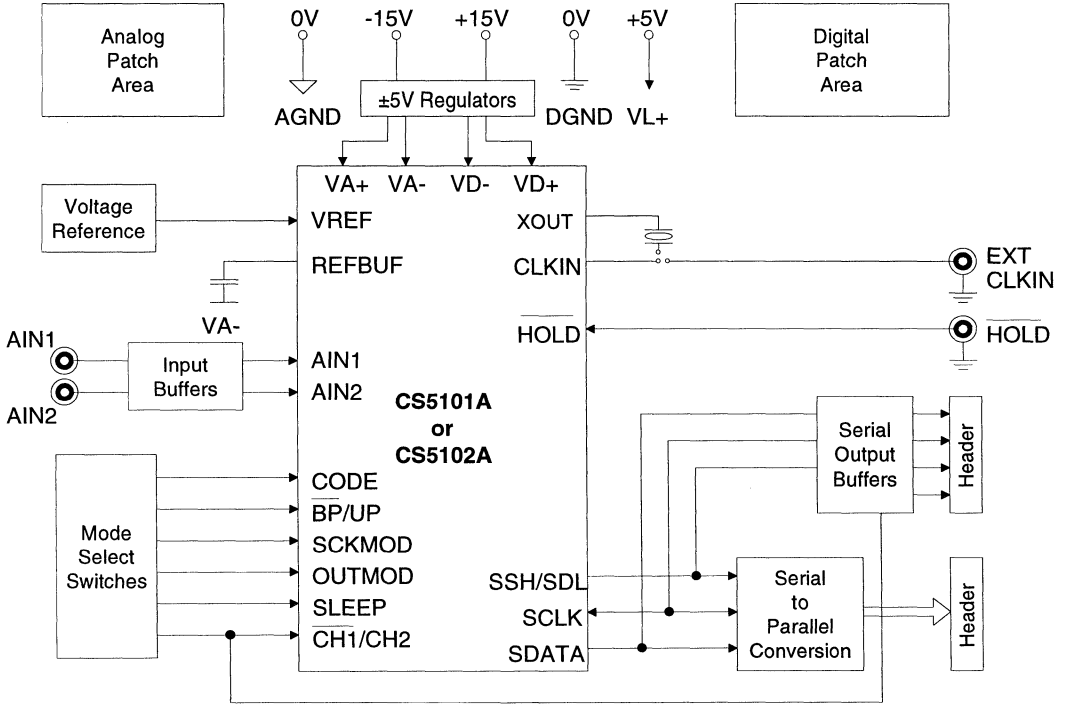
The CDB5101A/5102A Evaluation Board allows fast evaluation of the CS5101A and CS5102A 2-Channel, 16-bit Analog-to-Digital Converters.

Analog inputs are via BNC connectors. Digital outputs are available both directly from the ADC in serial form, and in 16 bit parallel form.

An adjustable monolithic voltage reference is included.

Ordering Information

CDB5101A
CDB5102A



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Power Supplies

Figure 1 shows the power supply arrangements. The analog section of the board is powered by ± 12/15 volts, which is regulated down to ± 5V for the ADC. A separate +5V digital supply is required to power the discrete logic.

Analog Input

The CS5101A/02A converters have a two-channel multiplexer input. Separate amplifiers (see Figure 2) are provided on the evaluation board to drive each input independently. If the converter is used in FRN mode, the multiplexer "ping-pongs" between channels. If only one signal is to be digitized in FRN mode at full speed, the AIN1 and AIN2 pins on the converter should be shorted together. Then the amplifier circuitry for the unused channel should be disconnected. For example, if only Analog Input one is used (in FRN mode) as the input, short the AIN1 and AIN2 pins of the converter and remove R15 and C15.

If you do not want to use the on-board amplifiers, connect your signal to TP27 for channel 1 and TP32 for channel 2. Use TP28 and TP31 to break the connection to the output of the on-board buffers. Your own buffer amplifiers may be installed in the 2 analog patch areas. For critical 2 channel applications, keep the signal path for the 2 channels identical.

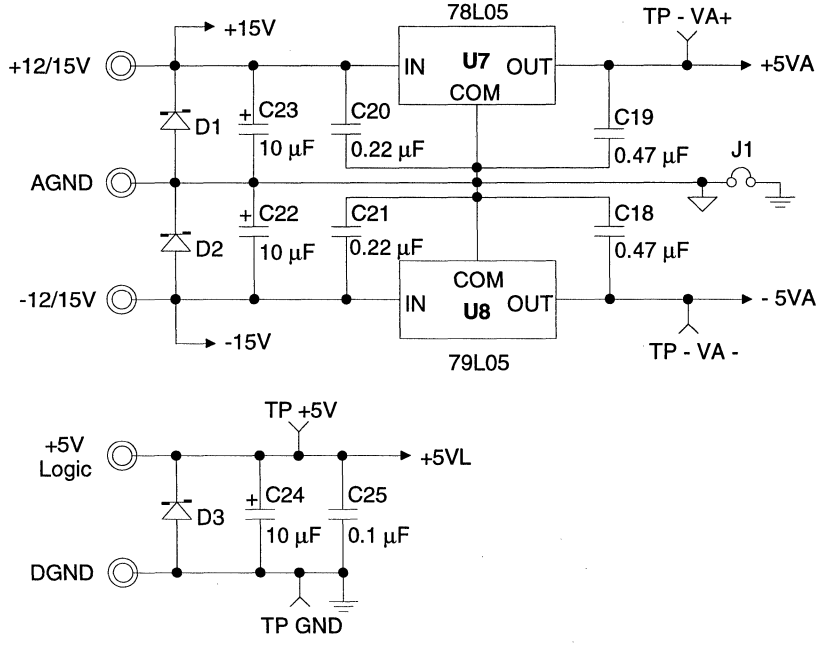


Figure 1. Power Supplies

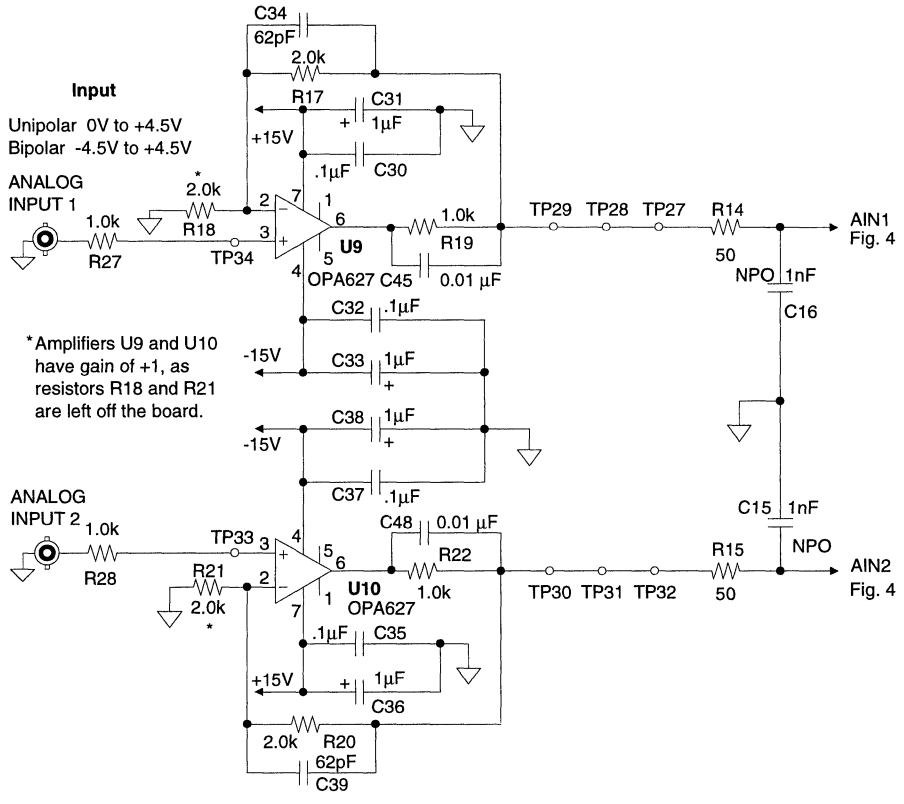


Figure 2. Input Buffer Circuit.

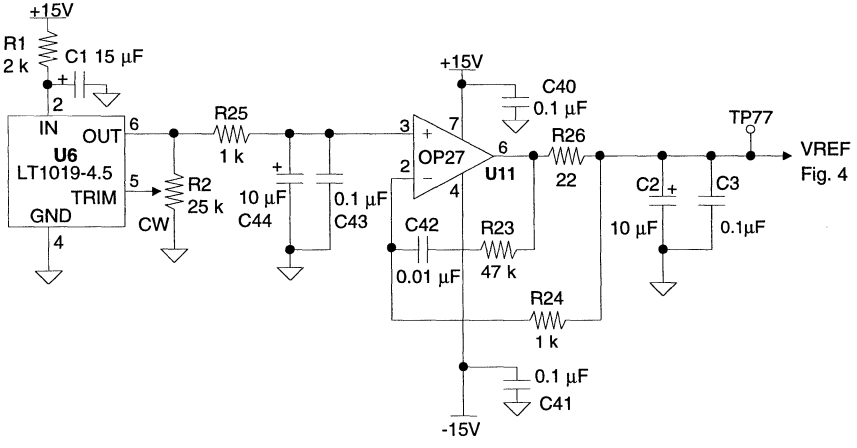


Figure 3. Voltage Reference

Voltage Reference

Figure 3 shows the LTI019-4.5 voltage reference, which is buffered and filtered to reduce output impedance and noise.

Master Clock

Figure 4 shows the local connections to the CS5101A or CS5102A. The appropriate crystal components are installed at the factory, which utilize the on-chip oscillator. For use with an external clock, cut Jumper J00 and drive a CMOS level compatible clock into the CLKIN BNC connector. R30 is an optional 50Ω terminating resistor if a pulse generator is used.

Sampling Clock ($\overline{\text{HOLD}}$) Generation

The evaluation board is shipped in FRN mode, which requires no externally generated $\overline{\text{HOLD}}$ signal. Alternate modes may be selected using DIP switch 3 and 4 (See Table 2). An external

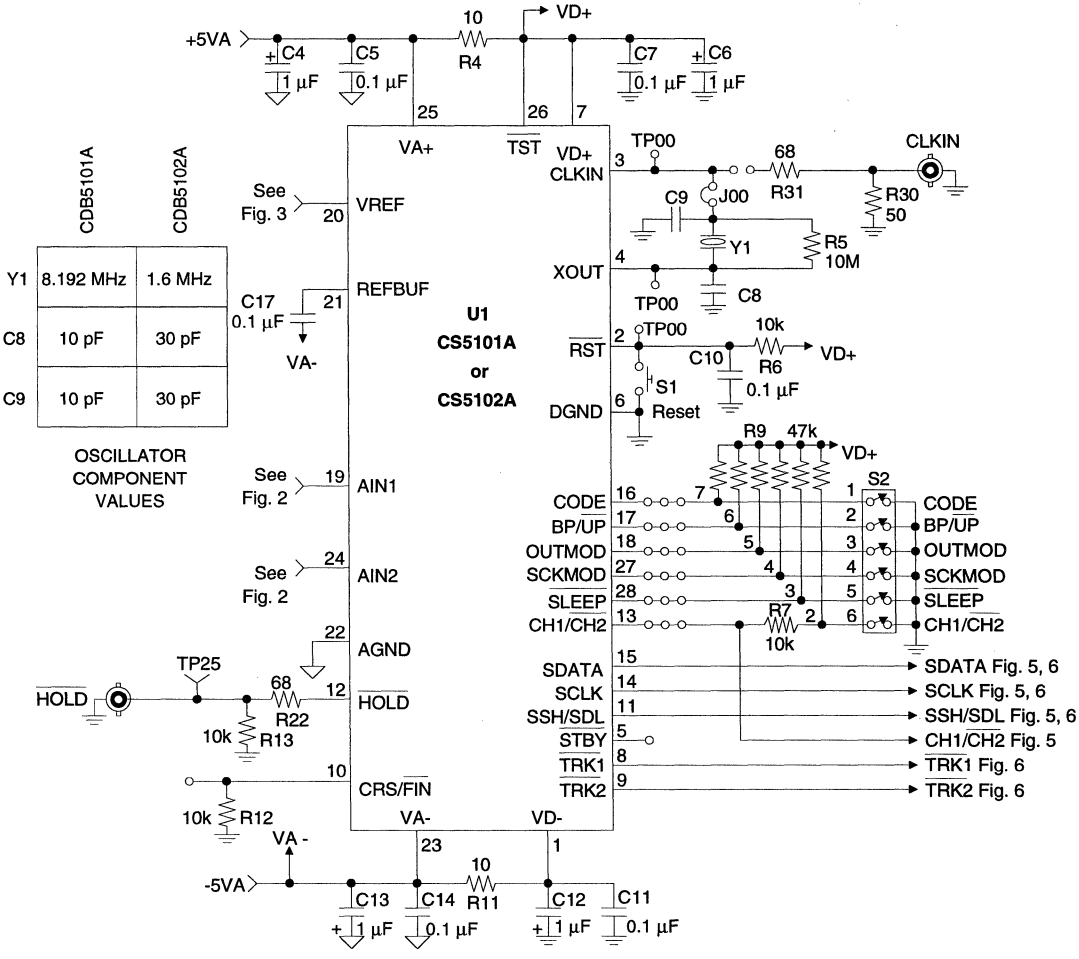


Figure 4. ADC Connections

$\overline{\text{HOLD}}$ may be connected using the $\overline{\text{HOLD}}$ BNC connector.

Control Signals

Figure 5 shows 2 headers are provided for serial data output and control signals. JP3 provides SDATA and SSH/SDL outputs. It also allows access to SCLK & CH1/$\overline{\text{CH2}}$ which may be inputs or outputs depending on the serial mode selected by the DIP switches. Jumpers J10, J11, J12, & J13 must be set to correspond with the appropriate directions of SCLK and CH1/$\overline{\text{CH2}}$.

JP5 provides output only access to the +5V logic supply, SCLK, SDATA and SLATCH, the serial to parallel latching control.

Serial to Parallel Conversion

When operating in the FRN or SSC serial port modes, the CS5101A/02A readily provides the three signals (SCLK, SDATA, and SSH/SDL) to support serial to parallel conversion of its output data.

Figure 6 Shows 2 74HC595's provided to convert the serial output of the ADC to parallel. A handshake flip-flop, U3, is provided for the parallel interface if required. When parallel data is available to read, $\overline{\text{DRDY}}$ goes low. The computer reads the data and sets DACK high and then low. This resets the flip-flop for the next word. JP4 selects whether both CH1 and CH2 data appears alternately, or CH1 only, or CH2 only.

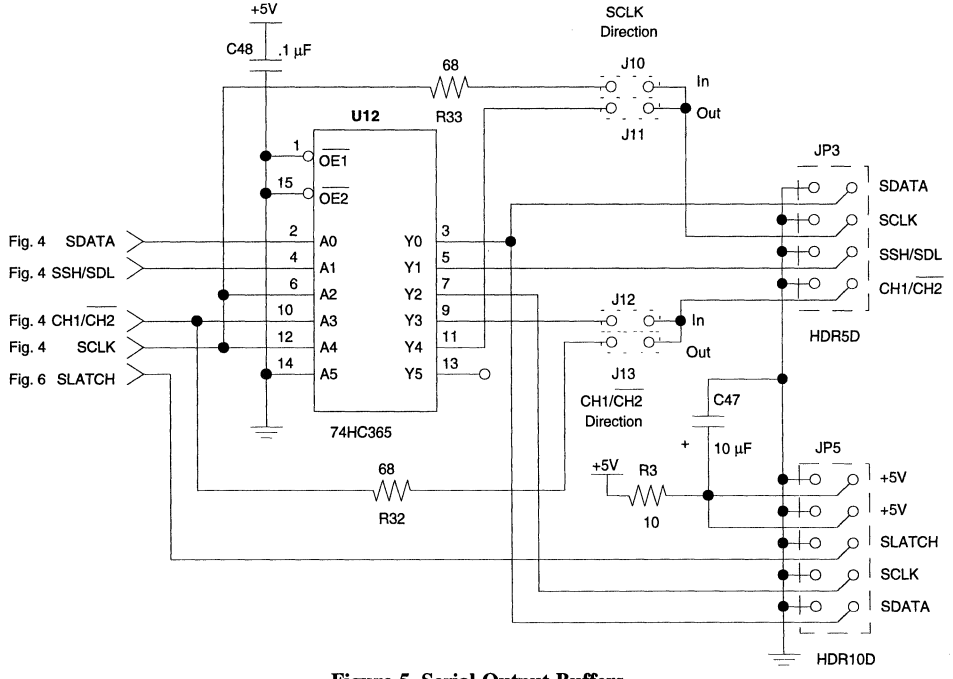


Figure 5. Serial Output Buffers

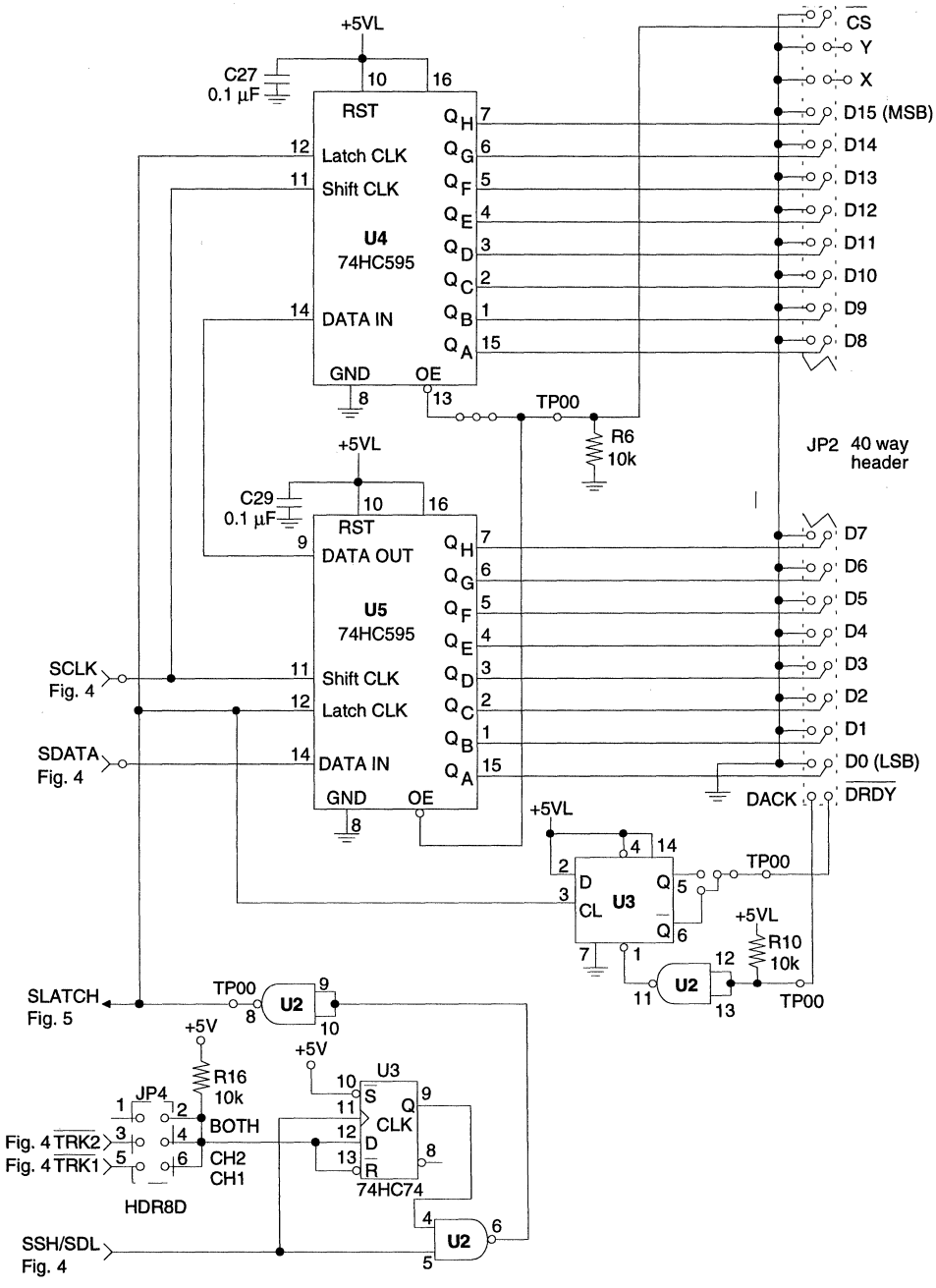
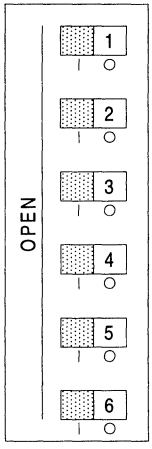


Figure 6. Serial to Parallel Converter



		OPEN	CLOSE
1	CODE	2's Complement	Binary
2	BP/$\overline{UP}$	Bipolar	Unipolar
3	OUTMOD	Selects Serial Port	
4	SCKMOD	Mode. See Table 2.	
5	$\overline{SLEEP}$	Normal Mode	Sleep Mode
6	CH1/$\overline{CH2}$*	AIN1	AIN2

*SW6 is not active when the converter is operating in the FRN mode.

Table 1. DIP Switch Selections

SCKMOD (SW4)	OUTMOD (SW3)	CS5101A/CS5102A Output Mode
CLOSE	CLOSE	(FRN) Free Run
CLOSE	OPEN	(SSC) Synchronous Self Clocking
OPEN	CLOSE	(RBT) Registered Burst Transmission
OPEN	OPEN	(PDT) Pipelined Data Transmission

NOTE: CLOSED = LOW = 0; OPEN = HIGH = 1.

Table 2. Output Mode Selections

DIP Switches

Tables 1 and 2 show the DIP switch settings.

Miscellaneous Hints on Using the Evaluation Board

Always depress the reset button after powering up the board. The CS5101A & CS5102A are self calibrating ADC's which require a reset to initiate the internal calibration procedure.

Crystal Semiconductor has software, available on request, which allows the evaluation board to be connected to a Metrabyte PIO12 parallel I/O card (which uses an Intel 8255 PIO chip), which is plugged into an IBM PC or compatible computer. The software is assembly language drivers to read the data from the board. Also included is source code, in Fortran, of an FFT routine.

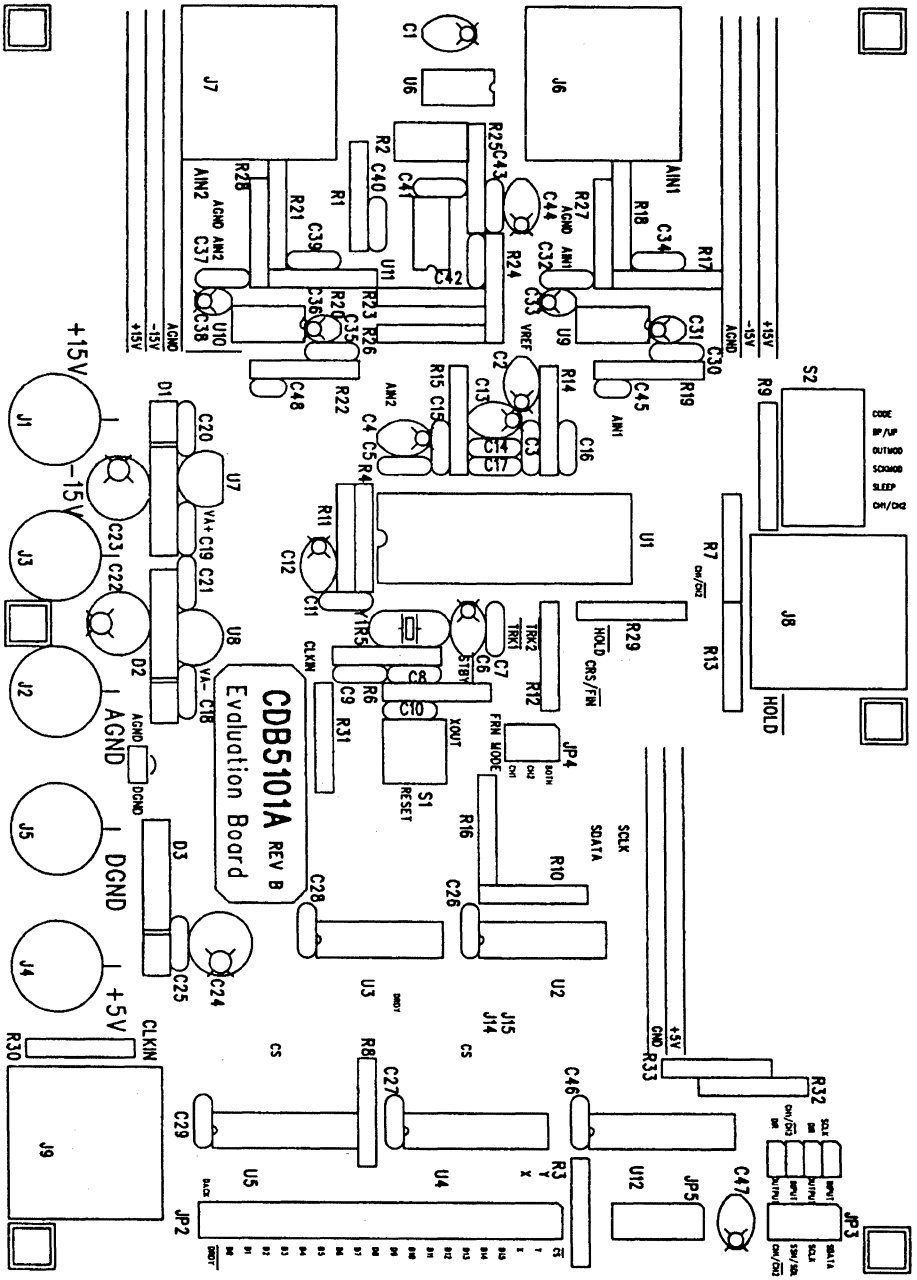


Figure 7. CDB5101A/02A Rev. B Layout

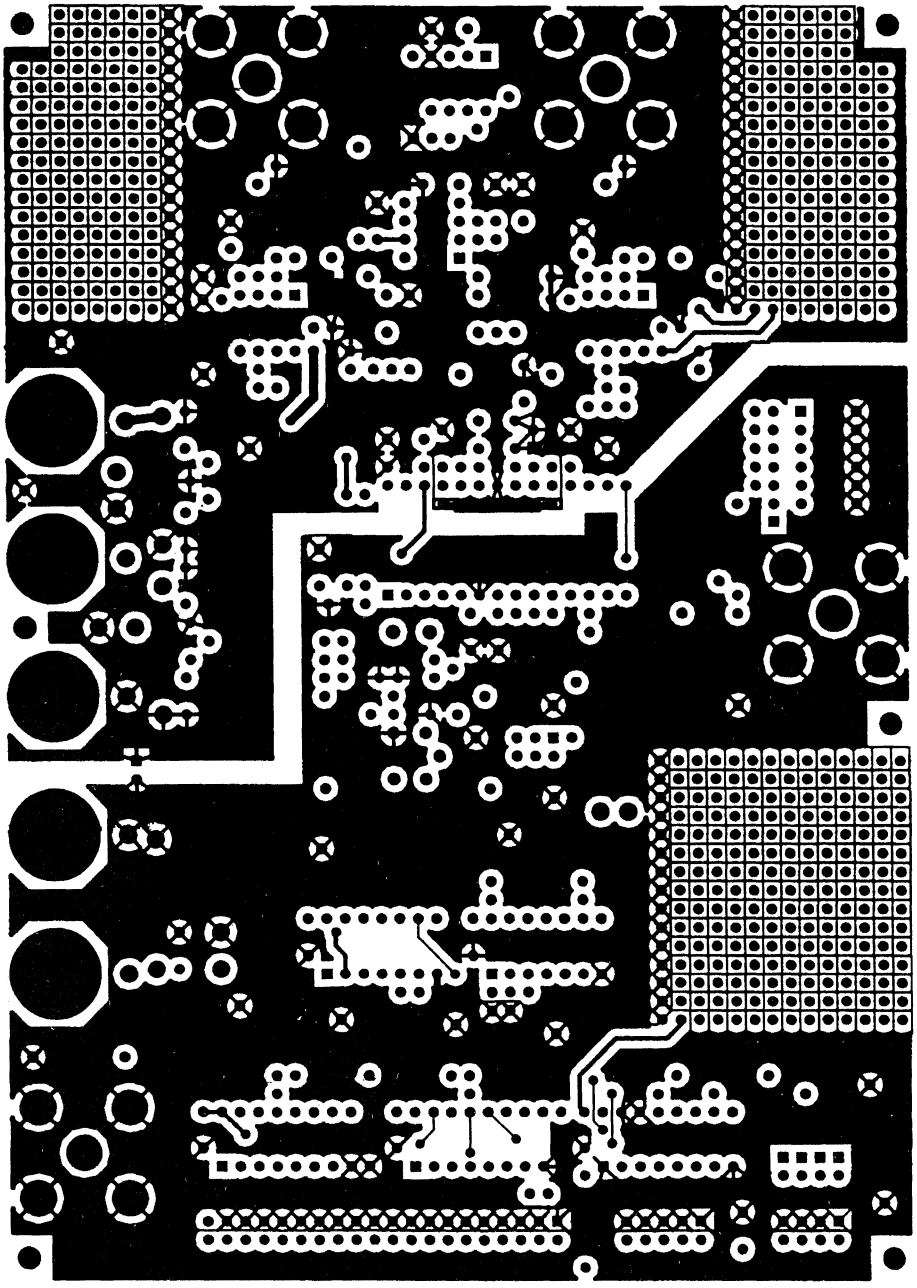


Figure 8. CDB5101A/02A Rev. B Component Side

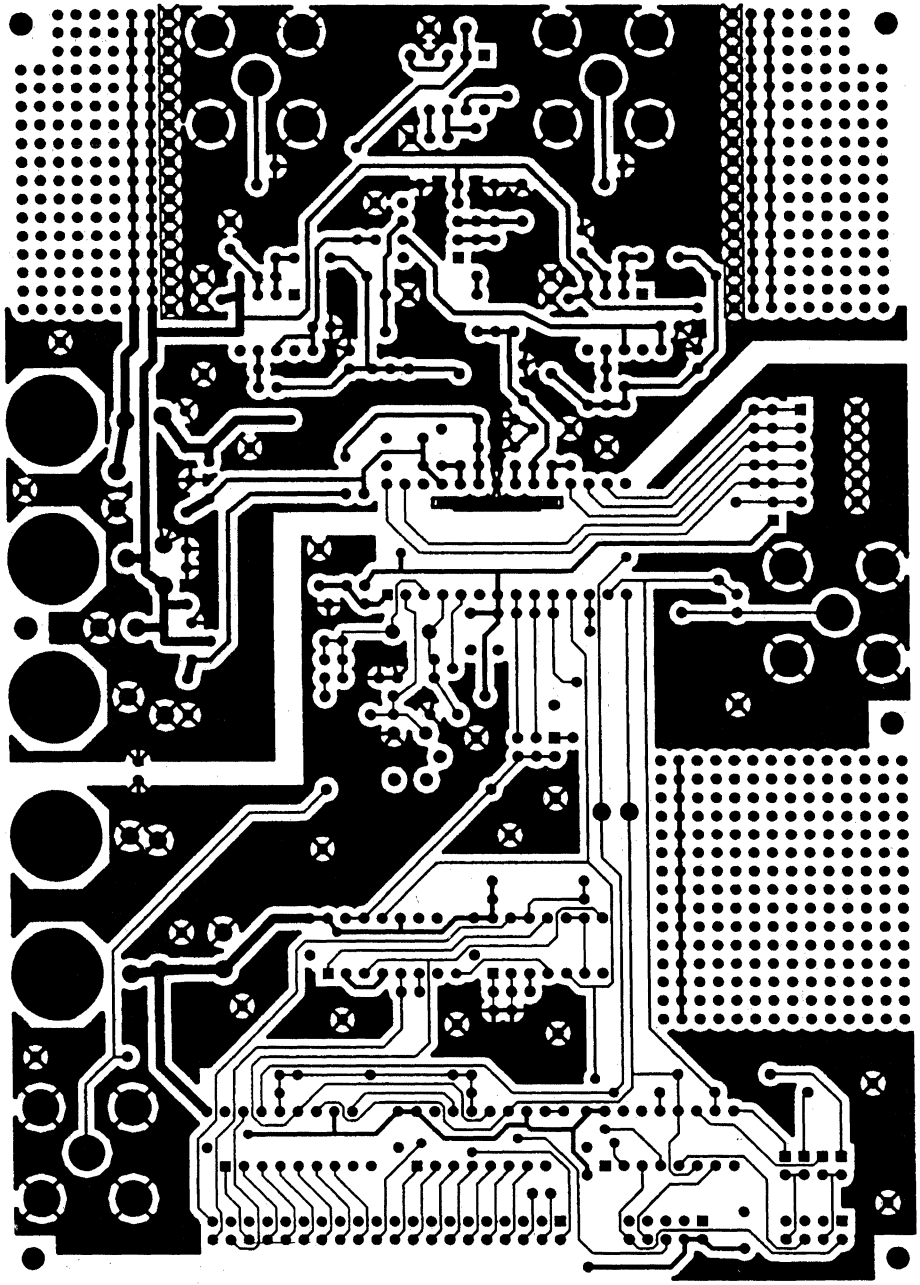


Figure 9. CDB5101A/02A Rev. B Solder Side

16-Bit, Stereo A/D Converter for Digital Audio

Features

- Monolithic CMOS A/D Converter
  - Inherent Sampling Architecture
  - Stereo or Monaural Capability
  - Serial Output
- Monaural Sampling Rates up to 100 kHz
  - 50 kHz/Channel Stereo Sampling
- Signal-to-(Noise+Distortion): 92 dB
- Dynamic Range: 92 dB
  - 95dB in 2X Oversampling Schemes
- Interchannel Isolation: 90 dB
- 2's Complement or Binary Coding
- Low Power Dissipation: 260 mW
  - Power Down Mode for Portable Applications
- Evaluation Board Available

General Description

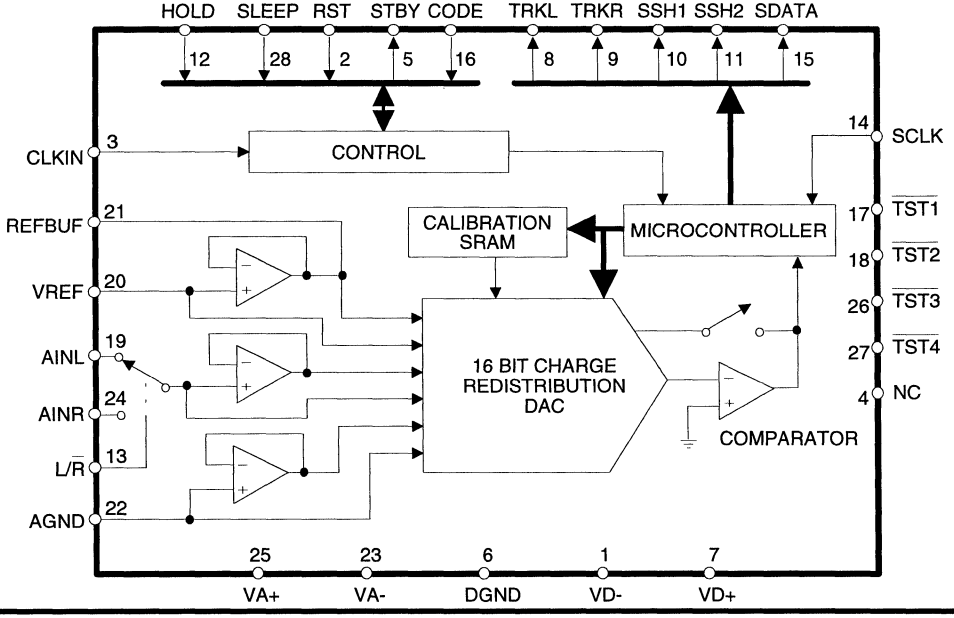
The CS5126 CMOS analog-to-digital converter is an ideal front-end for stereo or monaural digital audio systems. The CS5126 can be configured to handle two channels at up to 50kHz sampling per channel, or it can be configured to sample one channel at rates up to 100kHz.

The CS5126 executes a successive approximation algorithm using a charge redistribution architecture. On-chip self-calibration circuitry has 18-bit resolution thus avoiding any degradation in performance with low-level signals. The charge redistribution technique also provides an inherent sampling function which avoids the need for external sample/hold amplifiers.

Signal-to-(noise+distortion) in stereo operation is 92dB, and is dominated by internal broadband noise (1/2 LSB rms). When the CS5126 is configured for 2X oversampling, digital post-filtering bandlimits this white noise to 20kHz, increasing dynamic range to 95dB.

ORDERING INFORMATION:

CS5126-KP	0 °C to 70 °C	28-Pin Plastic DIP
CS5126-KL	0 °C to 70 °C	28-Pin PLCC



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

ANALOG CHARACTERISTICS (T_A = 25°C; VA+, VD+ = 5V; VA-, VD- = -5V; Full-Scale Input Sinewave, 1kHz; f_{clk} = 24.576MHz; VREF = 4.5V; Analog Source Impedance = 200Ω; Stereo operation, L/$\overline{R}$ toggling at 48 kHz unless otherwise specified.)

Parameter*			Symbol	Min	Typ	Max	Units
Resolution				-	-	16	Bits
Dynamic Performance							
Signal-to-(Noise plus Distortion)			S/(N+D)				
VIN = ±FS	(10 Hz to 20 kHz)			90	92	-	dB
VIN = -20dB	(f = 20 kHz)			70	72	-	dB
Total Harmonic Distortion			THD	-	0.001	-	%
Dynamic Range	Stereo Mode		DR	90	92	-	dB
	Monaural (20 kHz BW)			-	95	-	dB
Idle Channel Noise			$V_{n(ic)}$	-	1/2	-	LSB_{rms}
Interchannel Isolation		(Note 1)	I_{ic}	88	90	-	dB
Interchannel Mismatch			M_{ic}	-	0.01	-	dB
dc Accuracy							
Full-Scale Error			FSE	-	±4	-	LSB
Bipolar Offset Error			BPO	-	±4	-	LSB
Analog Input							
Aperture Time			t_{apt}	-	30	-	ns
Aperture Jitter			t_{ajt}	-	100	-	ps
Input Capacitance		(Note 2)	C_{in}	-	200	-	pF
Power Supplies							
Power Supply Current	Positive Analog	(Note 3)	I_{A+}	-	18	23	mA
	Negative Analog		I_{A-}	-	-18	-23	mA
($\overline{SLEEP}$ High)	Positive Digital		I_{D+}	-	8	12	mA
	Negative Digital		I_{D-}	-	-8	-12	mA
Power Dissipation	($\overline{SLEEP}$ High)	(Notes 3, 4)	P_{do}	-	260	350	mW
	($\overline{SLEEP}$ Low)		P_{ds}	-	1	-	mW
Power Supply Rejection	Positive Supplies	(Note 5)	PSR	-	84	-	dB
	Negative Supplies			-	84	-	dB

Notes:
1. One input grounded; dc to 20kHz, Full Scale input on the other channel. Guaranteed by characterization.
2. Applies only in the track mode. When converting or calibrating, input capacitance will typically be 10 pF.
3. All outputs unloaded. All inputs CMOS levels.
4. Power dissipation in sleep mode applies with no master clock applied (CLKIN high or low).
5. With 300mV p-p, 1kHz ripple applied to each supply separately. A plot of typical power supply rejection appears in the *Analog Circuit Connections* section.

* Refer to *Parameter Definitions* at the end of this data sheet.

Specifications are subject to change without notice.

DIGITAL CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+, VD+ = 5V±10%; VA-,VD- = -5V±10%)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage		V_{IH}	2.0	-	-	V
Low-Level Input Voltage		V_{IL}	-	-	0.8	V
High-Level Output Voltage	(Note 6)	V_{OH}	(VD+)-1.0V	-	-	V
Low-Level Output Voltage	I_{out} = 1.6 mA	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	-	10	µA

Notes: 6. I_{OUT} = -100 µA. This specification guarantees that each digital output will drive one TTL load (V_{OH} = 2.4V @ I_{OUT} = -40 µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 7.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	-4.5	-5.0	-5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	-4.5	-5.0	-5.5	V
Analog Reference Voltage		VREF	2.5	4.5	(VA+)-0.5	V
Analog Input Voltage	(Note 8)	V_{AIN}	-VREF	-	VREF	V

Notes: 7. All voltages with respect to ground.
8. The CS5126 can accept input voltages up to the analog supplies (VA+, VA-). It will produce an output of all 1's for inputs above VREF and all 0's for inputs below -VREF.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	-0.3	(VA+)+0.3	V
	Negative Digital	VD-	0.3	-6.0	V
	Positive Analog	VA+	-0.3	6.0	V
	Negative Analog	VA-	0.3	-6.0	V
Input Current, Any Pin Except Supplies	(Note 9)	I_{in}	-	±10	mA
Analog Input Voltage	(AIN and VREF pins)	V_{INA}	(VA-)-0.3	(VA+)+0.3	V
Digital Input Voltage		V_{IND}	-0.3	(VD+)+0.3	V
Ambient Temperature	(power applied)	T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C

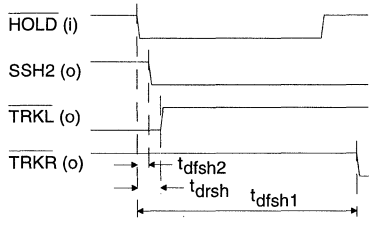
Notes: 9. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

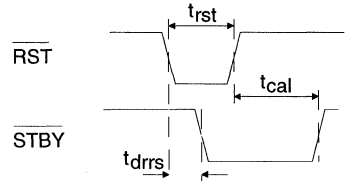
SWITCHING CHARACTERISTICS (T_A = 25 °C; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

Parameter		Symbol	Min	Typ	Max	Units
Master Clock Period		t_{clk}	40	-	-	ns
$\overline{HOLD}$ to SSH2 Falling	(Note 10)	t_{dfsh2}	-	80	-	ns
$\overline{HOLD}$ to $\overline{TRKL}$, $\overline{TRKR}$	SSH1 Falling	t_{dfsh1}	$198t_{clk}$	-	$214t_{clk}+50$	ns
$\overline{HOLD}$ to $\overline{TRKL}$, $\overline{TRKR}$	SSH1, SSH2 Rising	t_{drsh}	-	80	-	ns
$\overline{RST}$ Pulse Width		t_{rst}	150	-	-	ns
$\overline{RST}$ to $\overline{STBY}$ Falling		t_{drrs}	-	100	-	ns
$\overline{RST}$ Rising to $\overline{STBY}$ Rising		t_{cal}	-	34,584,480	-	t_{clk}
$\overline{HOLD}$ Pulse Width		t_{hold}	$2t_{clk}+50$	-	$192t_{clk}$	ns
$\overline{HOLD}$ to L/$\overline{R}$ Edge	(Note 10)	t_{dhlri}	-30	-	$192t_{clk}$	ns
SCLK period		t_{sclk}	200	-	-	ns
SCLK Pulse Width Low		t_{sclkl}	50	-	-	ns
SCLK Pulse Width High		t_{sclkh}	50	-	-	ns
SCLK Falling to SDATA Valid		t_{dss}	-	100	140	ns
$\overline{HOLD}$ Falling to SDATA Valid		t_{dhs}	-	140	200	ns

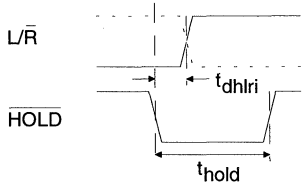
Notes: 10. SSH2 only works correctly if $\overline{HOLD}$ falling edge is within ±30ns of L/$\overline{R}$ edge OR if $\overline{HOLD}$ falling edge occurs between 30ns before $\overline{HOLD}$ rises to 192 t_{clk} after $\overline{HOLD}$ falls.



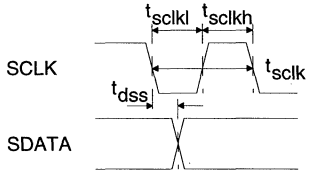
Control Output Timing



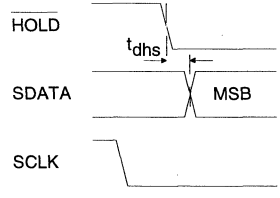
Reset and Calibration Timing



Channel Selection Timing



Serial Data Timing



Data Transmit Start Timing

GENERAL DESCRIPTION

The CS5126 is a 2-channel, 100kHz A/D converter designed specifically for stereo digital audio. The device includes an inherent sample/hold and an on-chip analog switch for stereo operation. Both left and right channels can thus be sampled and converted at rates up to 50kHz per channel. Alternatively, the CS5126 can be implemented in 2X oversampling schemes for improved dynamic range and distortion.

Output data is available in serial form with either binary or 2's complement coding. Control outputs are also supplied for use with an external sample/hold amplifier to implement simultaneous sampling.

THEORY OF OPERATION

The CS5126 implements a standard successive approximation algorithm using a charge-redistribution architecture. Instead of the traditional resistor network, the DAC is an array of binary-weighted capacitors. When not converting, the CS5126 tracks the analog input signal. The input voltage is applied across each leg of the DAC capacitor array, thus performing a voltage-to-charge conversion.

When the conversion command is issued, the charge is trapped on the capacitor array and the analog input is thereafter ignored. In effect, the entire DAC capacitor array serves as analog memory during conversion much like a hold capacitor in a sample/hold amplifier.

The conversion consists of manipulating the binary-weighted legs of the capacitor array to the voltage reference and analog ground. All legs share one common node at the input to the converter's comparator. This forms a binary-weighted capacitive divider. Since the charge at the comparator's input remains fixed, the voltage at that point depends on the proportion of capacitance tied to VREF versus AGND. The successive-approximation algorithm is used to find the proportion of capacitance which will drive the voltage to the comparator's trip point. That binary fraction of capacitance represents the converter's digital output.

2

Calibration

The ability of the CS5126 to convert accurately clearly depends on the accuracy of its DAC. The CS5126 uses an on-chip self-calibration scheme to insure low distortion and excellent dynamic range *independent of input signal conditions.*

Each binary-weighted bit capacitor actually consists of several capacitors which can be manipulated to adjust the overall bit weight. During calibration, an on-chip microcontroller manipulates the sub-arrays to precisely ratio the bits. Each bit is adjusted to just balance the sum of all less significant bits plus one dummy LSB (for example, 16C = 8C + 4C + 2C + C + C). The result is typical differential nonlinearity of ±1/4 LSB. That is, codes typically range from 3/4 to 5/4 LSB's wide.

The CS5126 should be reset upon power-up, thus initiating a calibration cycle which takes 1.4 seconds to complete. The CS5126 then stores its calibration coefficients in on-chip SRAM, and can be recalibrated at any later time.

SYSTEM DESIGN WITH THE CS5126

All timing and control inputs to the CS5126 can be easily generated from a master system clock. The CS5126 outputs serial data and a variety of digital outputs which can be used to control an external sample/hold amplifier for simultaneous sampling. The actual circuit connections depend on the system architecture (stereo or monaural 2X oversampling), and on the sampling characteristics (simultaneous or sequential sampling between channels).

System Initialization

Upon power up, the CS5126 must be reset to guarantee a consistent starting condition and initially calibrate the device. Due to the CS5126's low power dissipation and low temperature drift, no warm-up time is required before reset to accommodate any self-heating effects. However, the voltage reference input should have stabilized to within 0.25% of its final value before $\overline{RST}$ rises to guarantee an accurate calibration. Later, the CS5126 may be reset at any time to initiate a single full calibration. Reset overrides all other functions. If reset, the CS5126 will clear and initiate a new calibration cycle mid-conversion or midcalibration.

When $\overline{RST}$ is brought low all internal logic clears. When it returns high a calibration cycle begins which takes 34,584,480 master clock cycles to complete (approximately 1.4 seconds with a standard 24MHz master clock). The CS5126's $\overline{STBY}$ output remains low throughout the calibration sequence, and a rising transition indicates the device is ready for normal operation.

A simple power-on reset circuit can be built using a resistor and capacitor as shown in Figure 1. The RC time constant must be long enough to guarantee the rest of the system is fully powered up and stable by the end of reset.

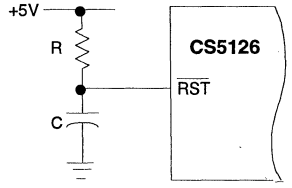


Figure 1. Power-On Reset Circuit

Master Clock

The CS5126 operates from an externally-supplied master clock. In stereo operation, the master clock frequency is set at 512 times the per-channel sampling rate (256 in 2X oversampling schemes). The CS5126 can accept master clocks up to 24.576 MHz for 48kHz stereo sampling or 96kHz monaural oversampling.

All timing and control inputs for channel selection, sampling, and serial data transmission may be divided down from the master clock. This yields a completely synchronous system, avoiding sampling and conversion errors due to asynchronous digital noise.

CIRCUIT CONNECTIONS

Stereo Operation

Figure 2 shows the standard circuit connections for operating the CS5126 in its stereo mode. The $\overline{HOLD}$, L/$\overline{R}$, and SCLK inputs are derived from the master clock using a binary divider string. A 24.576 MHz master clock is required for a sampling rate of 48kHz per channel.

For 48kHz stereo sampling, the CS5126 must sample and convert at a 96kHz rate to handle both channels. The master clock is divided by 256 and applied to the $\overline{HOLD}$ input. A falling transition on the $\overline{HOLD}$ pin places the input in the hold mode and initiates a conversion cycle. The $\overline{HOLD}$ input is latched internally by the master clock, so it can return high anytime after one master clock cycle plus 50ns.

In stereo operation the CS5126 alternately samples and converts the left and right input channels. This alternating channel selection is achieved by dividing the $\overline{HOLD}$ input by two (that is, dividing the master clock by 512) and applying it to the L/$\overline{R}$ input. Upon completion of each conversion cycle, the CS5126 automatically returns to the track mode. The status of L/$\overline{R}$ as

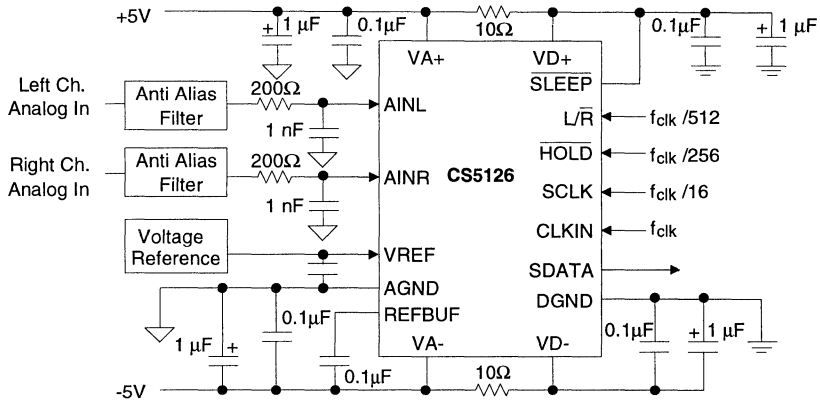


Figure 2. Stereo Mode Connection Diagram

each conversion finishes determines which channel is acquired and tracked. The L/$\overline{R}$ input must remain valid at least until 30ns before the next falling transition on $\overline{HOLD}$.

As shown in the timing diagram in Figure 3, the CS5126 uses pipelined data transmission. That is, data from a particular conversion transmits during the *next* conversion cycle. The serial clock input, SCLK, is derived by dividing the master clock by 16. The MSB (most-significant-bit) will be stable on the first rising edge of SCLK after a falling transition on HOLD. With a serial clock of $f_{clk}/16$, transmission of all 16 output bits will span an entire conversion and acquisition cycle.

STEREO MODE PERFORMANCE

As illustrated in Figure 4, the CS5126 typically provides 92dB S/(N+D) and 0.001% THD. Unlike conventional successive-approximation ADC's, the CS5126's signal-to-noise and dynamic range are not limited by differential nonlinearities (DNL) caused by calibration errors. Rather, the dominant noise source is broadband thermal noise which aliases into the baseband. This *white* broadband noise also appears as an idle channel noise of 1/2 LSB (rms).

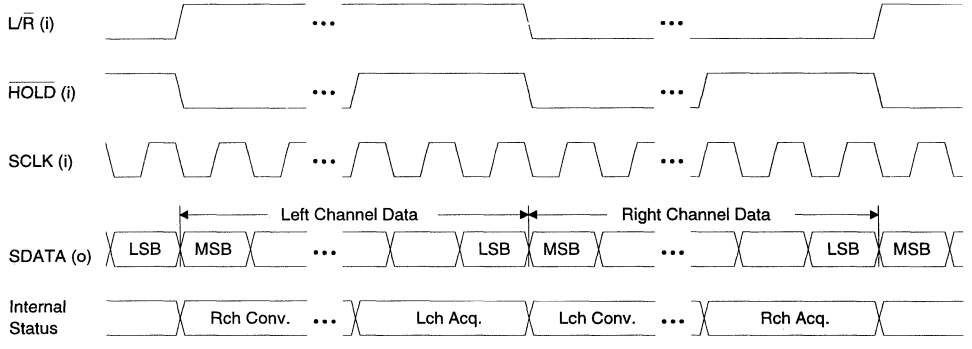


Figure 3. Stereo Mode Timing

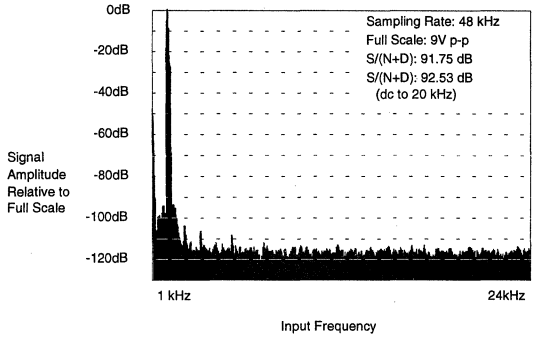


Figure 4. FFT Plot of CS5126 in Stereo Mode (Left Channel with 1 kHz, Full-Scale Input)

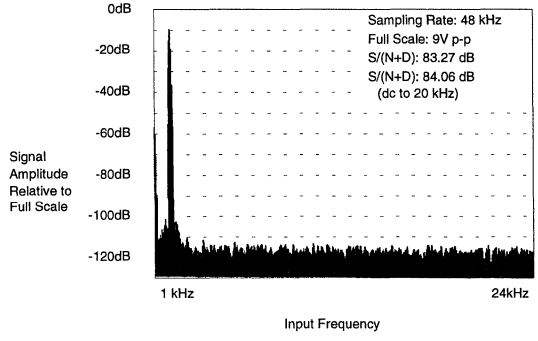
Differential Nonlinearity

The self-calibration scheme utilized in the CS5126 features a calibration resolution of 1/4 LSB, or 18-bits. This ideally yields DNL of ±1/4 LSB, with code widths ranging from 3/4 to 5/4 LSB's. This insures consistent sound quality independent of signal level.

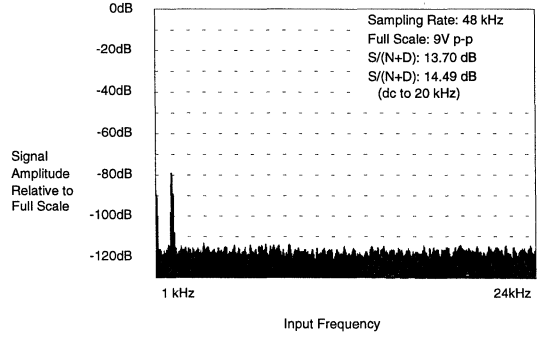
Traditional laser trimmed ADC's have significant differential nonlinearities which are disastrous to sound quality with low-level signals. Appearing as wide and narrow codes, DNL often causes entire sections of the transfer function to be missing. Although their affect is minor on S/(N+D) with high amplitude signals, DNL errors dominate performance with low-level signals. For instance, a signal 80dB below full-scale will slew past only 6 or 7 codes. Half of those codes could be missing with a conventional hybrid ADC capable of only 14-bit DNL.

The most common source of DNL errors in conventional ADC's is bit weight errors. These can arise due to accuracy limitations in factory trim stations, thermal or physical stresses after calibration, and/or drifts due to aging or temperature variations in the field. Bit-weight errors have a drastic effect on a converter's ac performance. They can be analyzed as step functions superimposed on the input signal. Since bits (and their errors) switch in and out throughout the transfer curve, their effect is signal dependent. That is, harmonic and intermodulation distortion, as well as noise, can vary with different input conditions.

Differential nonlinearities in successive-approximation ADC's also arise due to dynamic errors in the comparator. Such errors can dominate if the converter's throughput/sampling rate is driven too high. The comparator will not be allowed sufficient time to settle during each bit decision in the successive-approximation algo-



a. Left Channel with 1 kHz, -10 dB Input



b. Left Channel with 1 kHz, -80 dB Input

Figure 5. FFT Plots of CS5126 in Stereo Mode

rithm. The worst-case codes for dynamic errors are the major transitions (1/2 FS; 1/4, 3/4 FS; etc.). Since DNL effects are most critical with low-level signals, the codes around in mid-scale, (that is, 1/2 FS), are most important. Yet those codes are worst-case for dynamic DNL errors!

With all linearity calibration performed on-chip to 18-bits, the CS5126 maintains accurate bit weights. DNL errors are dominated by residual calibration errors of ±1/4 LSB rather than dynamic errors in the comparator. Furthermore, *all* DNL effects on S/(N+D) are buried by white broadband noise. This yields excellent sound quality *independent of signal level.*
(See Figure 5)

Sampling Distortion

Like most discrete sample/hold amplifier designs, the CS5126's inherent sample/hold exhibits a frequency-dependent distortion due to nonideal sampling of the analog input voltage. The calibrated capacitor array used during conversions is also used to track and hold the analog input signal. The conversion is not performed on the analog input voltage per se, but is actually performed on the charge trapped on the capacitor array at the moment the $\overline{\text{HOLD}}$ command is given. The charge on the array ideally assumes a linear relationship to the analog input voltage. Any deviation from this linear relationship will result in conversion errors even if the conversion process proceeds flawlessly.

At dc, the DAC capacitor array's voltage coefficient dictates the converter's linearity. This variation in capacitance with respect to applied signal voltage yields a nonlinear relationship between the charge on the array and the analog input voltage and places a bow or wave in the transfer function. This is the dominant source of distortion at low input frequencies (Figure 4).

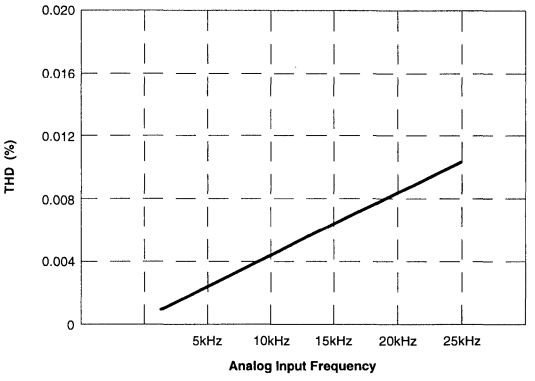


Figure 6. THD vs Input Frequency (9V p-p Full-Scale Input)

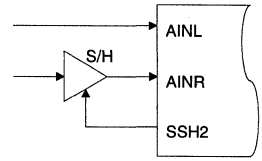
The ideal relationship between the charge on the array and the input voltage can also be distorted at high signal frequencies due to nonlinearities in the internal MOS switches. Dynamic signals cause ac current to flow through the switches connecting the capacitor array to the analog input pin in the track mode. Nonlinear on-resistance in the switches causes a nonlinear voltage drop. This effect worsens with increased signal frequency and slew rate as shown in Figure 6 since the magnitude of the steady state current increases. First noticeable at 1kHz, this distortion assumes a linear relationship with input frequency. *With signals 20dB or more below full-scale, it no longer dominates the converter's overall S/(N+D) performance.*

This distortion is strictly an ac sampling phenomenon. If significant energy exists at high frequencies, the effect can be eliminated using an external track-and-hold amplifier to allow the array's charge current to decay, thereby eliminating any voltage drop across the switches. Since the CS5126 has a second sampling function on-chip, the external track-and-hold can return to the track mode once the converter's $\overline{\text{HOLD}}$ input falls. It need only acquire the analog input by the time the entire conversion cycle finishes.

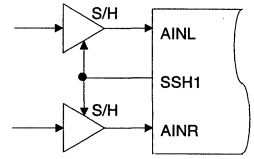
Simultaneous Sampling

The CS5126 offers four digital output signals, SSH1, SSH2, $\overline{\text{TRKL}}$, and $\overline{\text{TRKR}}$ which can be used to control external sample/hold amplifiers to achieve simultaneous sampling and/or reduce sampling distortion.

Figure 7 shows the timing relationships for SSH1, SSH2, $\overline{\text{TRKL}}$, and $\overline{\text{TRKR}}$. In the stereo configuration shown in Figure 1 the CS5126 samples the left and right channels 180° out of phase. Simultaneous sampling between the left and right channels can be achieved as shown in Figure 8a using the CS5126's SSH2 output. The external sample/hold will freeze the right channel analog signal as the CS5126 freezes the left channel input at AINL. It will hold that signal valid at AINR until the CS5126 begins a right channel conversion. Once that conversion begins, the sample/hold returns to the sample mode. The acquisition time for the external sample/hold amplifier must not exceed the CS5126's minimum conversion time of 192 master clock cycles (7.8µs for 48kHz stereo sampling).



a. Standard Connections



b. High-Slew Conditions

Figure 8. Simultaneous Sampling Connections

The CS5126's sampling distortion with high-frequency, high-amplitude input signals may be improved if a low distortion sample/hold amplifier is used as shown in Figure 8a. The right channel input at AINR will appear as dc to the CS5126 resulting in *no ac current* flowing through the internal MOS switches. Sampling distortion can likewise be improved for *both channels* using the SSH1 output as shown in Figure 8b. Simi-

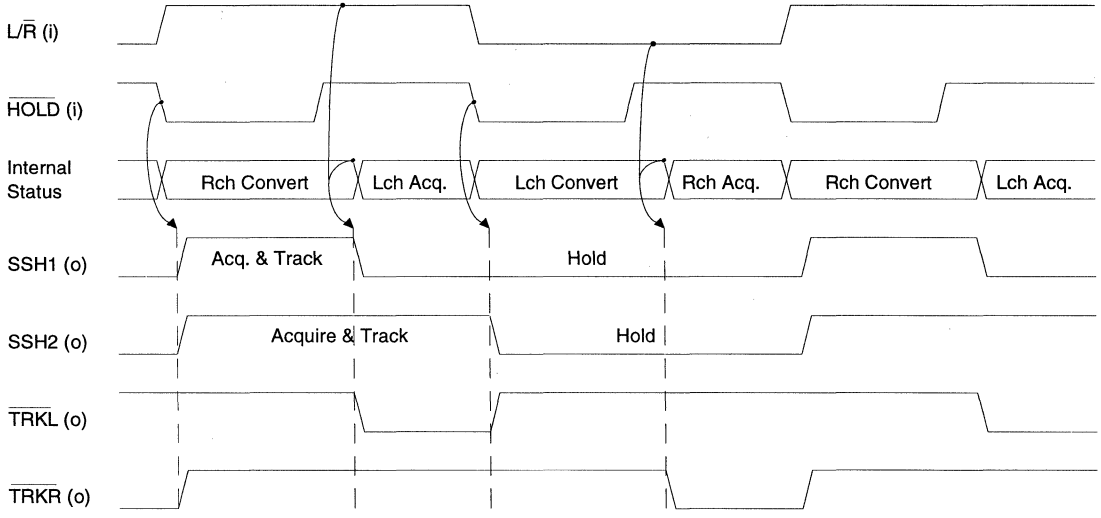


Figure 7. External Sampling Control Output Timing

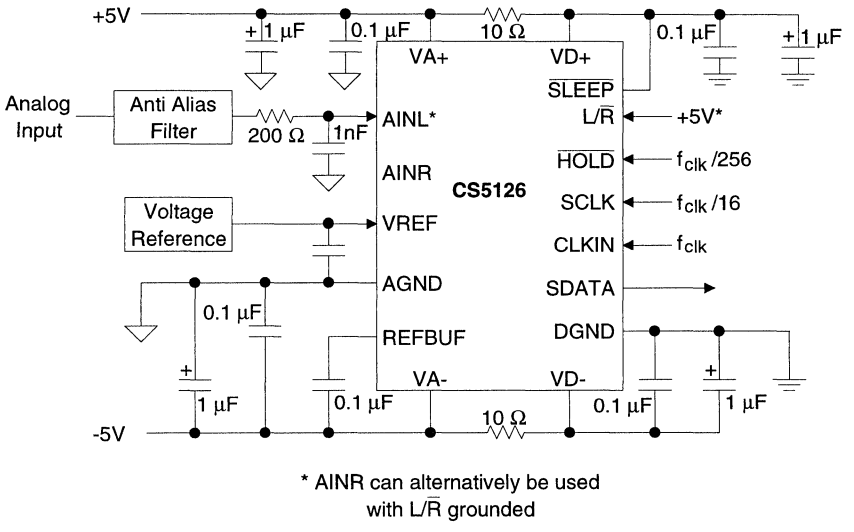


Figure 9. Monaural 2X Oversampling Connections

larly, the acquisition time for the external sample/hold amplifiers must not exceed the minimum conversion time of 192 master clock cycles (7.8µs for 48kHz stereo sampling).

Oversampling

The CS5126 can alternatively be used to oversample *one channel* (monaural) by 2X simply by tying the L/$\overline{R}$ input high or low. This moves much of the anti-alias burden from analog filters to digital post-filtering. The analog filters' corner can be pushed out in frequency with lower roll-off, allowing lower passband ripple and more linear phase in the audioband. Digital FIR filtering, meanwhile, can be used to implement high roll-off filters with ultra-low passband ripple and perfectly linear phase.

Oversampling not only improves system-level filtering performance, but it also enhances the ADC's dynamic range and distortion characteristics. All noise energy in a sampled, digital signal aliases into the baseband between dc and one-half the sampling rate. For an *ideal* successive-approximation ADC the noise spectral content is white. Therefore, in a 2X oversampling scheme such as 96kHz sampling the ADC's noise will be be spread *uniformly* from dc to 48kHz. Digital post-filtering then rejects noise outside of the 20kHz or 22kHz bandwidth, resulting in improved signal-to-noise and dynamic range. For a white noise spectrum, a 2X reduction in bandwidth yields a 3dB improvement in dynamic range.

Due to its on-chip self-calibration scheme, the CS5126's dynamic range is limited only by *white* broadband noise rather than signal-dependent DNL errors. Therefore, the CS5126 picks up a full 3dB improvement in dynamic range to 95dB when implemented in 2X oversampling schemes.

Oversampling and digital filtering also enhance the ADC's distortion performance. Consider for example a full-scale 15kHz input signal to the CS5126 sampling at 96kHz. Sampling distortion produces THD of approximately 0.005% (86dB) at the converter's output. Most of the distortion energy resides in the second and third harmonics

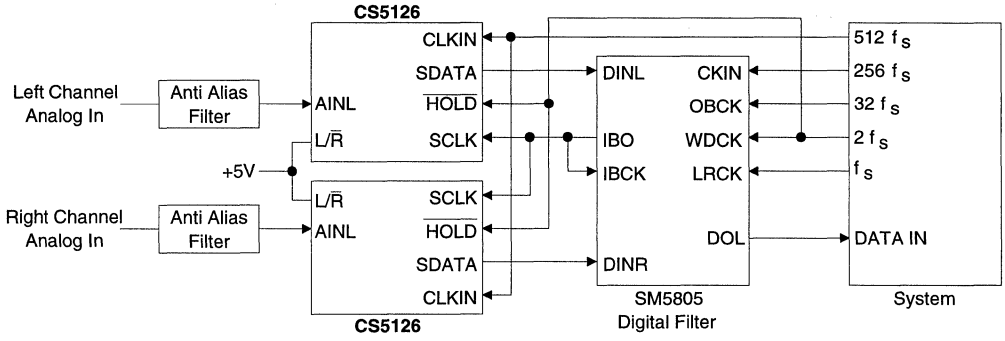


Figure 10. Example Oversampling System Diagram

at 30kHz and 45kHz. Meanwhile, digital filters such as the SM5805 shown in Figure 10 will roll-off rapidly from 22kHz to 28kHz and reject distortion energy in the second, third, and fourth harmonics. Clearly, oversampling results in superior system-level distortion.

Still, if the CS5126's distortion performance with high-frequency, high-amplitude signals must be enhanced in 2X oversampling schemes, the $\overline{\text{TRKL}}$ or $\overline{\text{TRKR}}$ outputs can be used. Either $\overline{\text{TRKL}}$ or $\overline{\text{TRKR}}$ will fall at the end of each conversion cycle depending on which channel is being acquired. The AINL and $\overline{\text{TRKL}}$ connections (or AINR and $\overline{\text{TRKR}}$) can be used as shown in Figure 11 to control an external low-distortion sample/hold to create an effective dc input for the CS5126 and remove sampling distortion.

Digital Circuit Connections

When TTL loads are utilized the potential for crosstalk between digital and analog sections of the system is increased. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

The CS5126 has a power down mode, initiated by bringing $\overline{\text{SLEEP}}$ low. During power down, the A/D Converter's calibration information is retained. The CS5126 may be used for conversion immediately after $\overline{\text{SLEEP}}$ is brought high.

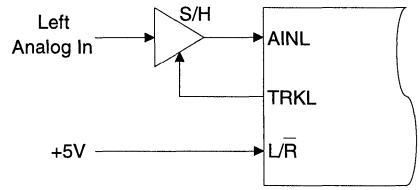


Figure 11. High-Slew Monaural Connections

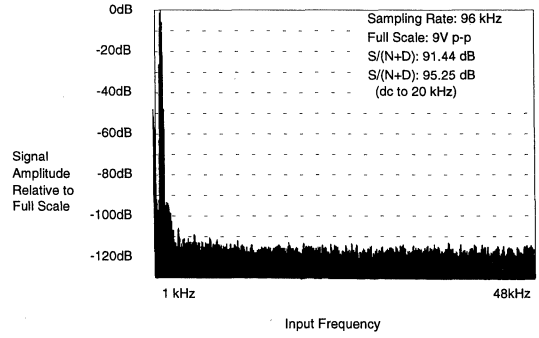


Figure 12. FFT Plot of CS5126 in Monaural 2X Oversampling Mode

ANALOG CIRCUIT CONNECTIONS

Most popular successive-approximation A/D converters generate dynamic loads at their analog connections. The CS5126 internally buffers all analog inputs (AIN, VREF, and AGND) to ease the demands placed on external circuitry. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

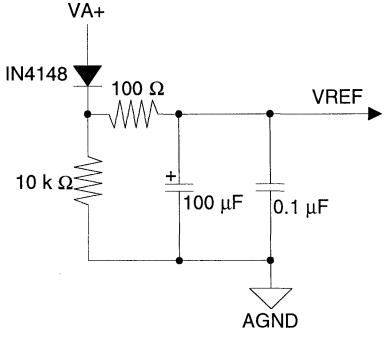
Reference Considerations

An application note titled "*Voltage references for the CS501X/CSZ511X Series of A/D Converters*" is available which describes the dynamic load conditions presented by the VREF input on Crystal's self-calibrating SAR A/D converters (including the CS5126). As the CS5126 sequences through bit decisions it switches portions of the capacitor array to the VREF pin in accordance with the successive-approximation algorithm. For proper operation, the source impedance at the VREF pin must remain low at frequencies up to 1MHz.

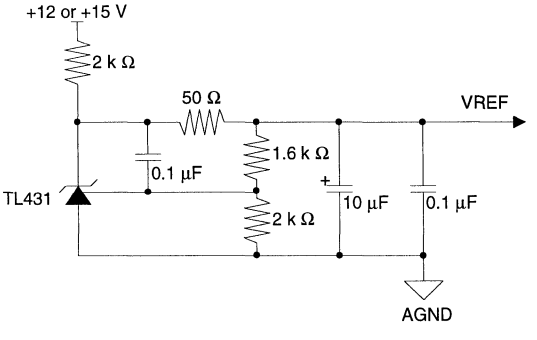
A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the frequencies of interest, so the reference voltage can simply be derived as shown in Figure 13a. Although very low cost, this reference has almost no power supply rejection from the VA+ line.

Alternatively, a more stable and precise reference can be generated using a TL431 shunt reference from T.I. or Motorola, as shown in Figure 13b.

The magnitude of the current load on the external reference circuitry will scale to the master clock frequency. At the full-rated 24 MHz clock the reference must supply a maximum load current of 20µA peak-to-peak (2µA typical). An output impedance of 2Ω will therefore yield a maximum error of 40mV. With a 4.5V reference and LSB size of 138mV this would insure approximately 1/4 LSB accuracy. A 10µF capacitor exhibits an impedance of less than 2Ω at frequencies greater than 16kHz. A high-quality tantalum capacitor in parallel with a smaller ceramic capacitor is recommended.



a. Simple Reference



b. Low-cost Shunt Reference

Figure 13. Suggested Voltage Reference Circuits

The CS5126 can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. The recommended reference voltage is 4.5 volts. The CS5126 can actually accept reference voltages up to the positive analog supply. However, as the reference voltage approaches VA+ the external drive requirements may increase at VREF.

An internal reference buffer is used to protect the external reference from current transients during conversion. This internal buffer enlists the aid of an external 0.1µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-.

Analog Input Connection

Each time the CS5126 finishes a conversion cycle it switches the internal capacitor array to the appropriate analog input pin, AINL or AINR. This creates a minor dynamic load at the sampling frequency. All throughput specifications apply for maximum analog source impedances of 200Ω at AINL and AINR. In addition, the comparator requires source impedances of less than 400Ω around 2MHz for stability, which is met by practically all bipolar op amps. For more information, see our Application Note: "*Input Buffers for the CS501X/CSZ511X Series of A/D Converters*"

Analog Input Range/Coding Format

The CS5126 features a bipolar input range with the reference voltage applied to VREF defining both positive and negative full-scale. The coding format is set by the state of the CODE input. If high, coding is 2's complement; if low, the CS5126's output is in offset-binary format.

Grounding and Power Supply Decoupling

The CS5126 uses the analog ground connection, AGND, only as a reference voltage. *No dc power or signal currents flow through the AGND connection*, thus minimizing the potential for interchannel crosstalk. Also, AGND is completely independent of DGND. However, any noise riding on the AGND input relative to the system's analog ground will induce conversion errors. Therefore, both analog inputs and the reference voltage should be referred to the AGND pin, which should be used as the entire system's analog ground. The digital and analog supplies are isolated within the CS5126 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. All four supplies should be decoupled to their respective grounds using 0.1 µF ceramic capacitors. If significant low frequency noise is present on the supplies, 1 µF tantalum capacitors are recommended in parallel with the 0.1 µF capacitors.

The positive digital power supply of the CS5126 must never exceed the positive analog supply by more than a diode drop or the CS5126 could experience permanent damage. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. The system connection diagrams in figures 2 and 9 show a decoupling scheme which allows the CS5126 to be powered from a single set of ± 5V rails. The positive digital supply is derived from the analog supply through a 10Ω resistor to avoid the analog supply dropping below the digital supply. If this scheme is utilized, care must be taken to insure that any digital load currents (which flow through the 10 Ω resistors) do not cause the magnitude of digital supplies to drop below the analog supplies by more than 0.5 volts. Digital supplies must always remain above the minimum specification.

As with any high-precision A/D converter, the CS5126 requires careful attention to grounding and layout arrangements. However, no unique layout issues must be addressed to properly apply the CS5126. The CDB5126 evaluation board is available for the CS5126, which avoids the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CS5126, and can be quickly reconfigured to simulate any combination of sampling and master clock conditions.

Power Supply Rejection

The CS5126 features a fully differential comparator design, resulting in superior power supply rejection. Rejection is further enhanced by the on-chip self-calibration and "auto-zero" process. Figure 14 shows worst-case rejection for all combinations of conversion rates and input conditions.

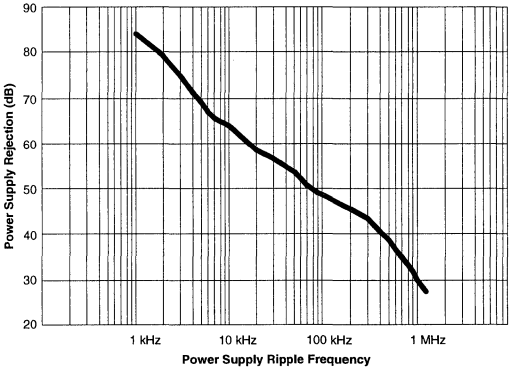
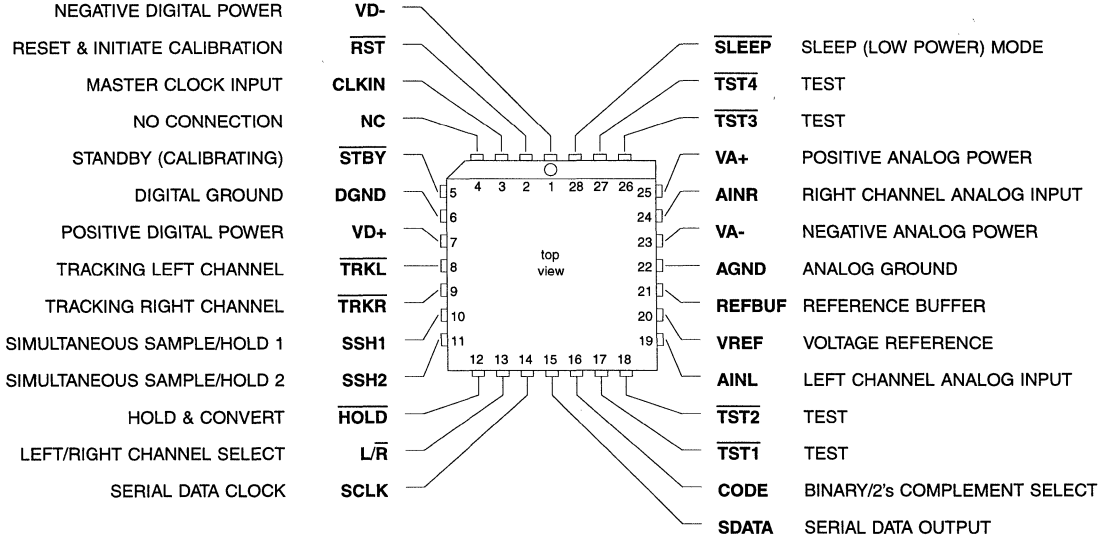


Figure 14. Power Supply Rejection

PIN DESCRIPTIONS

NEGATIVE DIGITAL POWER	VD-	1	28	SLEEP	SLEEP (LOW POWER) MODE
RESET & INITIATE CALIBRATION	RST	2	27	TST4	TEST
MASTER CLOCK INPUT	CLKIN	3	26	TST3	TEST
NO CONNECTION	NC	4	25	VA+	POSITIVE ANALOG POWER
STANDBY (CALIBRATING)	STBY	5	24	AINR	RIGHT CHANNEL ANALOG INPUT
DIGITAL GROUND	DGND	6	23	VA-	NEGATIVE ANALOG POWER
POSITIVE DIGITAL POWER	VD+	7	22	AGND	ANALOG GROUND
TRACKING LEFT CHANNEL	TRKL	8	21	REFBUF	REFERENCE BUFFER
TRACKING RIGHT CHANNEL	TRKR	9	20	VREF	VOLTAGE REFERENCE
SIMULTANEOUS SAMPLE/HOLD 1	SSH1	10	19	AINL	LEFT CHANNEL ANALOG INPUT
SIMULTANEOUS SAMPLE/HOLD 2	SSH2	11	18	TST2	TEST
HOLD & CONVERT	HOLD	12	17	TST1	TEST
LEFT/RIGHT CHANNEL SELECT	L/R	13	16	CODE	BINARY/2's COMPLEMENT SELECT
SERIAL DATA CLOCK	SCLK	14	15	SDATA	SERIAL DATA OUTPUT



Power Supply Connections

VD+ - Positive Digital Power, PIN 7.
Positive digital power supply. Nominally +5 volts.

VD- - Negative Digital Power, PIN 1.
Negative digital power supply. Nominally -5 volts.

DGND - Digital Ground, PIN 6.
Digital ground reference.

VA+ - Positive Analog Power, PIN 25.
Positive analog power supply. Nominally +5 volts.

VA- - Negative Analog Power, PIN 23.
Negative analog power supply. Nominally -5 volts.

AGND - Analog Ground, PIN 22.
Analog ground reference.
Oscillator

CLKIN - Clock Input, PIN 3.
All conversions and calibrations are timed from a master clock which must be externally supplied.

Digital Inputs

$\overline{\text{HOLD}}$ - Hold, PIN 12.
A falling transition on this pin sets the CS5126 to the hold state and initiates a conversion. This input must remain low at least one master clock cycle plus 50ns.

L/$\overline{\text{R}}$ - Left/Right Input Channel Select, PIN 13.
Status at the end of a conversion cycle determines which analog input channel will be acquired for the next conversion cycle.

$\overline{\text{SLEEP}}$ - Sleep, PIN 28.
When brought low causes the CS5126 to enter a low-power quiescent state. All calibration coefficients are retained in memory, so no recalibration is needed after returning to the normal operating mode.

CODE - 2's Complement/Binary Coding Select, PIN 16.
Determines whether data appears in 2's complement or offset-binary format. If high, 2's complement; if low, offset-binary.

SCLK - Serial Clock, PIN 14.
Serial data changes status on a falling edge of this input, and is valid on a rising edge.

$\overline{\text{RST}}$ - Reset, PIN 32.
When taken low, all internal digital logic is reset. Upon returning high, a full calibration sequence is initiated which takes 34,584,480 master clock cycles to complete.

Analog Inputs

AINL, AINR - Left and Right Channel Analog Inputs, PINS 19 and 24.
Analog input connections for the left and right input channels.

VREF - Voltage Reference, PIN 20.
The analog reference voltage which sets the analog input range. Its magnitude sets both positive and negative full-scale.

Digital Outputs

$\overline{\text{STBY}}$ - Standby (Calibrating), PIN 5.
Indicates calibration status after reset. Remains low throughout the calibration sequence and returns high upon completion.

SDATA - Serial Output, PIN 15.
Presents each output data bit on a falling edge of the SCLK input. Data is valid to be latched on the rising edge of SCLK.

SSH1, SSH2 - Simultaneous Sample/Hold 1 and 2, PINS 10 and 11.
Used to control external sample/hold amplifier(s) to achieve simultaneous stereo sampling.

$\overline{\text{TRKL}}$, $\overline{\text{TRKR}}$ - Tracking Left, Tracking Right, PINS 8 and 9.
Indicate the end of a conversion cycle. Either $\overline{\text{TRKL}}$ or $\overline{\text{TRKR}}$ falls at the end of a conversion cycle depending on the status of L/$\overline{\text{R}}$ and which channel is to be tracked.

Analog Outputs

REFBUF - Reference Buffer Output, PIN 21.
Reference buffer output. A 0.1µF ceramic capacitor must be tied between this pin and VA-.

Miscellaneous

NC - No Connection, PIN 4.
Must be left floating for proper operation.

$\overline{\text{TST1}}$, $\overline{\text{TST2}}$, $\overline{\text{TST3}}$, $\overline{\text{TST4}}$ - Test, PINS 17, 18, 26, 27.
Allow access to the CS5126's test functions which are reserved for factory use. Must be tied to VD+.

PARAMETER DEFINITIONS

Total Harmonic Distortion - The ratio of the rms sum of all harmonics up to 20 kHz to the rms value of the signal. Units in percent.

Signal-to-Noise plus Distortion Ratio - The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels.

Dynamic Range - Full-scale Signal-to-Noise plus Distortion with the input signal 60dB below full-scale. Units in decibels.

Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with the input under test grounded and a full-scale signal applied to the other channel. Units in decibels.

Full Scale Error - The deviation of the last code transition from the ideal (VREF-3/2 LSB's) after all offsets have been externally compensated. Units in decibels relative to full scale.

Bipolar Offset - The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND). Units in microvolts.

Interchannel Mismatch - The difference in output codes between the left and right channels with the same analog input applied. Units expressed in decibels relative to full scale. Tested at full scale input.

Aperture Time - The time required after the hold command for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter - The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

Semiconductor Corporation

CDB5126

Evaluation Board for CS5126

Features

- Serial to Parallel Conversion
- All Timing Signals Provided
- Adjustable Voltage Reference
- ± 5 V Regulators
- Digital and Analog Patch Areas

General Description

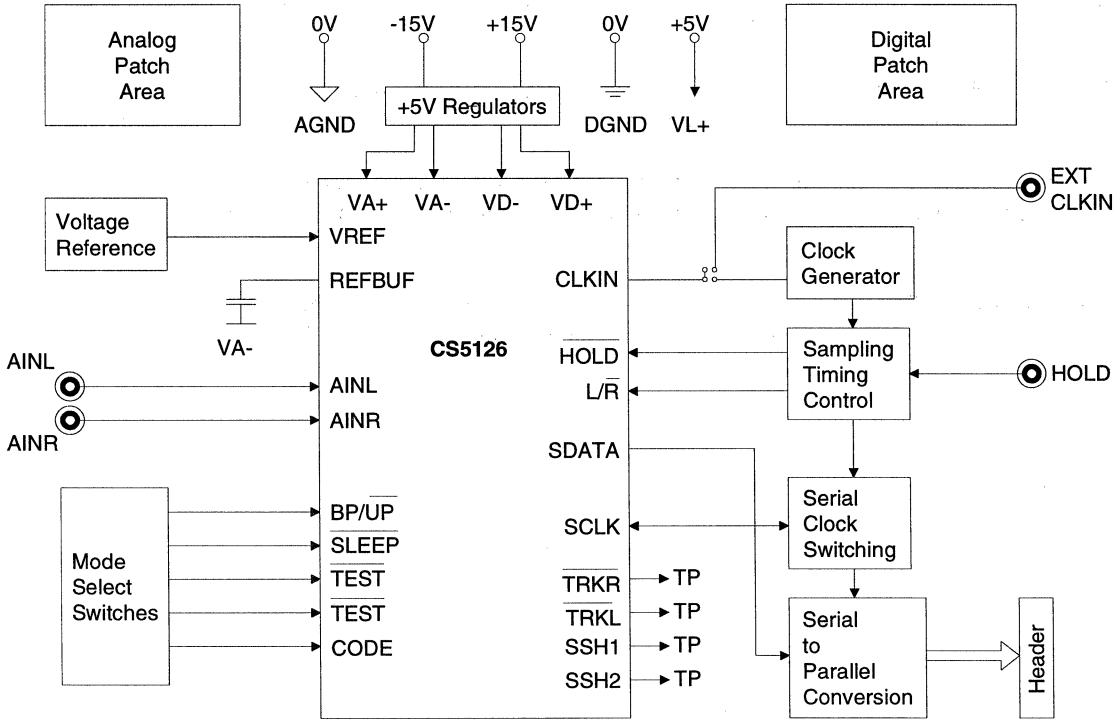
The CDB5126 Evaluation Board allows fast evaluation of the CS5126 2-Channel, 16-bit Analog-to-Digital Converter.

Analog inputs are via BNC connectors. Digital outputs are available both directly from the ADC in serial form, and in 16 bit parallel form.

An adjustable monolithic voltage reference is included.

ORDERING INFORMATION

CDB5126



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax:(512) 445 7581

Power Supplies

Figure 1 shows the power supply arrangements. The analog section of the board is powered by ± 15 volts, which is regulated down to ± 5 V for the ADC. A separate +5 V digital supply is required to power the discrete logic. Be sure to switch on the ± 15 V at the same time as, or before, the + 5 V logic supply. This will make sure that the CLK and other logic signal are not driving the part before it is powered.

Analog Input

The analog input range is either ± V_{ref} in the bipolar mode or 0 V to +V_{ref} in the unipolar mode. The voltage reference is factory set to the recommended value of +4.5 volts, so the typical input signal ranges become ± 4.5 volts or 0 V to +4.5 V.

The source driving the analog inputs should have a low (< 200 Ω at high frequency) output impedance. Be careful not to overdrive the inputs outside the power supplies of the ADC (± 5 V). Figure 2 shows the buffer circuit used at the Crystal factory to drive the ADC when performing FFT testing. See the CS5126 data sheet for example FFT test results.

Voltage Reference

As shown in Figure 3, an LT1019-5 voltage reference provides a stable 4.5 V reference for the ADC. An optional OP27 buffer filters out excess reference noise and provides a very low output impedance. To try the unbuffered LT1019-5 directly, solder in J2 and cut the VREF trace. Alternatively the shunt reference based reference schematic given in the CS5126 data sheet can be evaluated by adding it to the analog patch area.

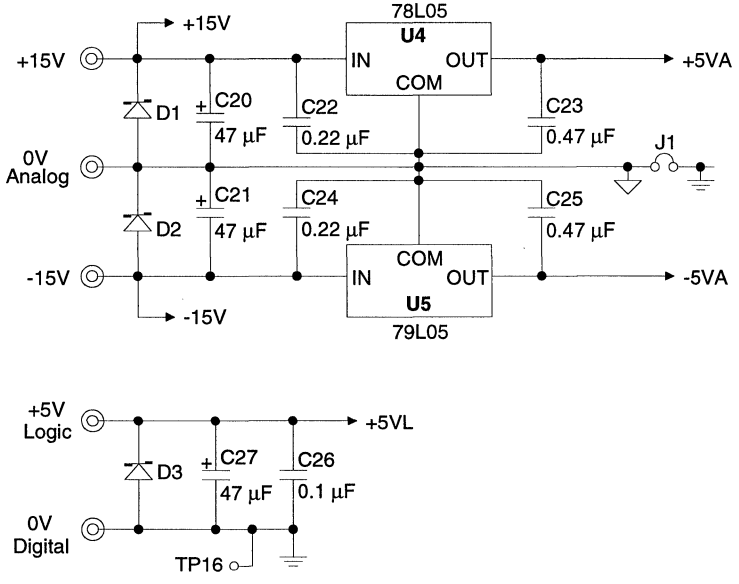


Figure 1. Power Supplies

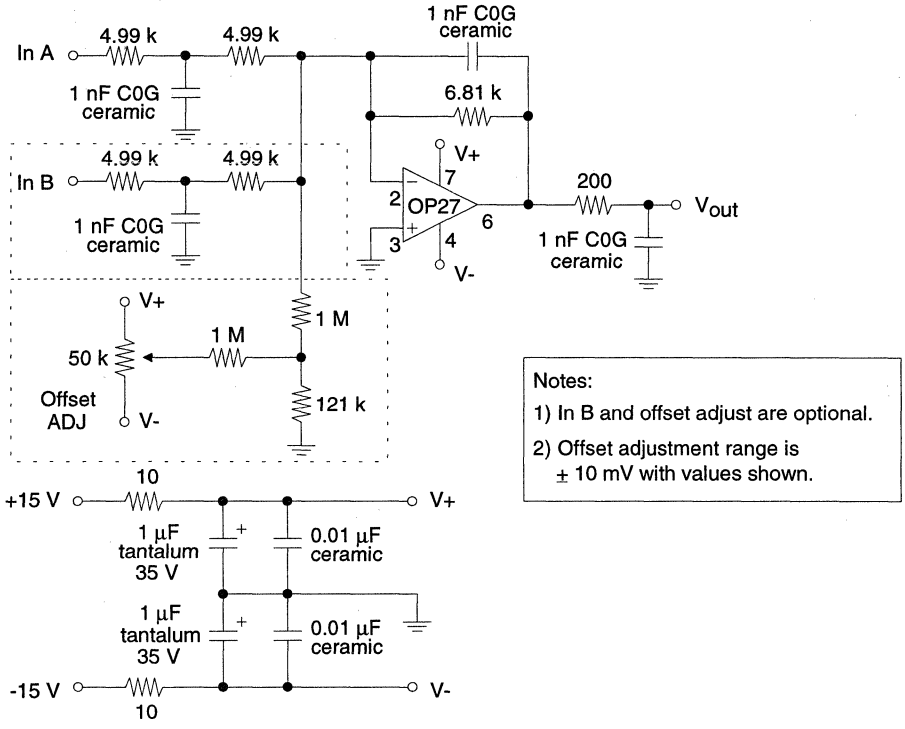


Figure 2. Example Input Buffer Circuit (not provided on the CDB5126 evaluation board)

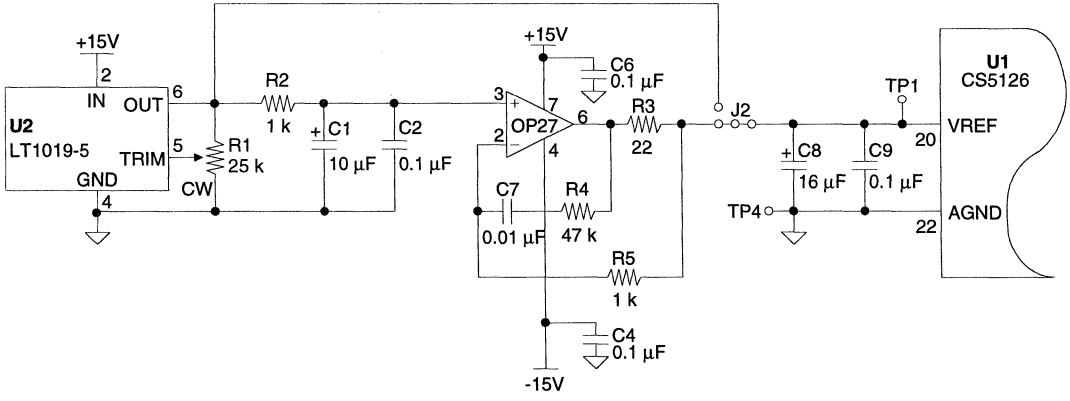


Figure 3. Voltage Reference

A 5 volt reference can be used provided the supplies to the ADC are elevated to ± 5.3 volts. This can be done by inserting 22 Ω resistors in series with the regulator (U4 and U5) common leads.

Master Clock

The CS5126 requires an external 24.576 MHz clock for a 96 kHz sample rate. A 24.576 MHz clock oscillator module (U6) is provided. An external clock can also be selected by P1, via a BNC connector. R15 is an optional 75 Ω terminating resistor for the external clock BNC.

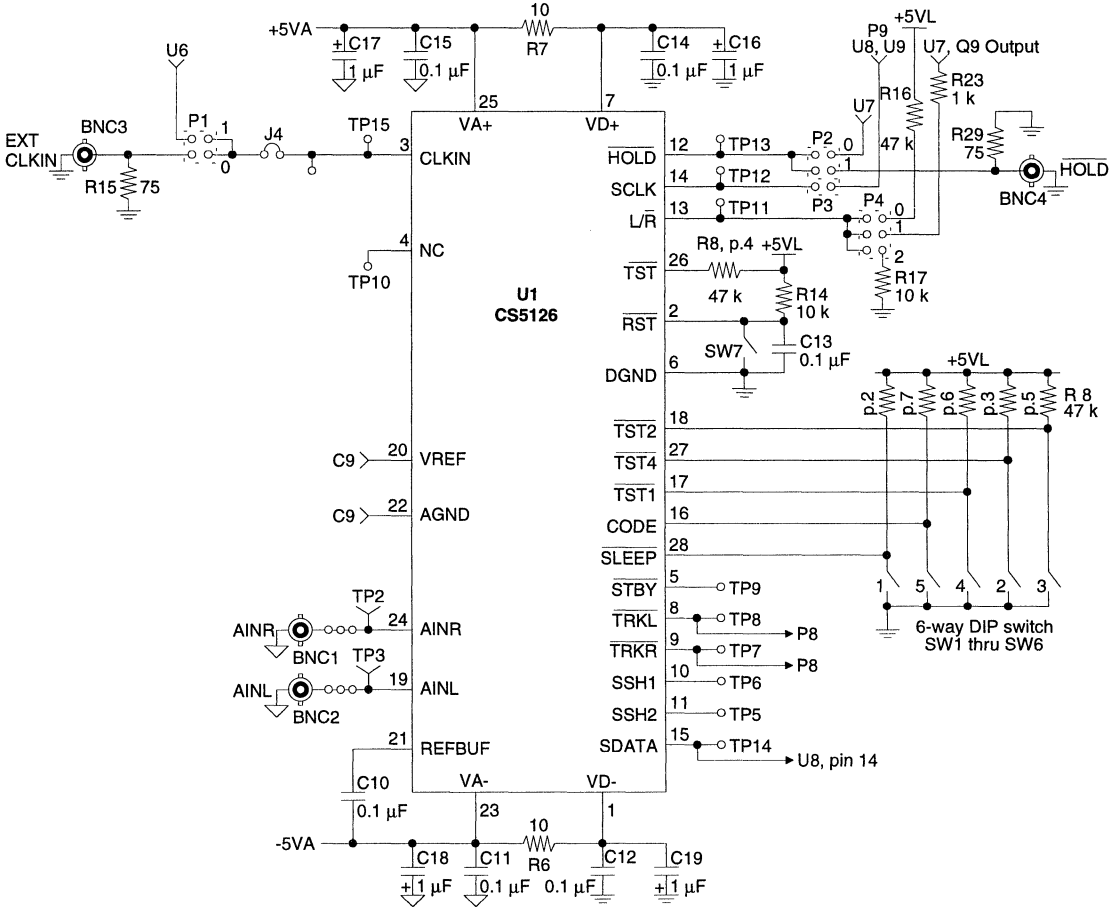


Figure 4. ADC Connections

Sampling Clock Generation Logic

The CS5126 requires an external serial clock to clock out the data. The CDB5126 board has the logic necessary to generate the master clock, $\overline{\text{HOLD}}$, L/$\overline{\text{R}}$, and SCLK to allow fast evaluation of the ADC. In most systems, these timing signals will be available from the main timing section, typically generated by a logic array of some variety. $\overline{\text{HOLD}}$ may be brought in externally via a BNC, optionally terminated by R29. SCLK and L/$\overline{\text{R}}$ select may be brought in externally via test points and removing jumpers.

Figure 5 shows the on-board clock generation circuitry. U7 (74HC4040) produces binary divided ratios of the 24.576 MHz master clock. Q4 generates a 1.5 MHz clock, which is used for SCLK. Q8 generates a 96 kHz clock, used for $\overline{\text{HOLD}}$, and Q9 generates a 48 kHz clock, optionally used to toggle L/$\overline{\text{R}}$ select. This set of clocks causes the CS5126 to continuously convert, generating a continuous stream of serial data bits. To correctly identify the last bit of each word, U12 produces a pulse only when Q4, Q5, Q6, Q7, Q8, and optionally Q9 are all high. This state is latched by U10A to prevent any glitches, and the resulting signal (attached to TP18) is used to latch the U8-U9 shift registers.

Serial to Parallel Conversion

Figure 6 shows the serial to parallel conversion circuit. Two 74HC595 shift register/latches connected in series with SDATA assemble 16-bit, parallel words, clocked by SCLK. As discussed above, the outputs are latched inside the 74HC595 at the end of each 16-bit word. The outputs are brought out to a 40-way header (P5). Only low capacitance, twisted pair, ribbon cable should be used.

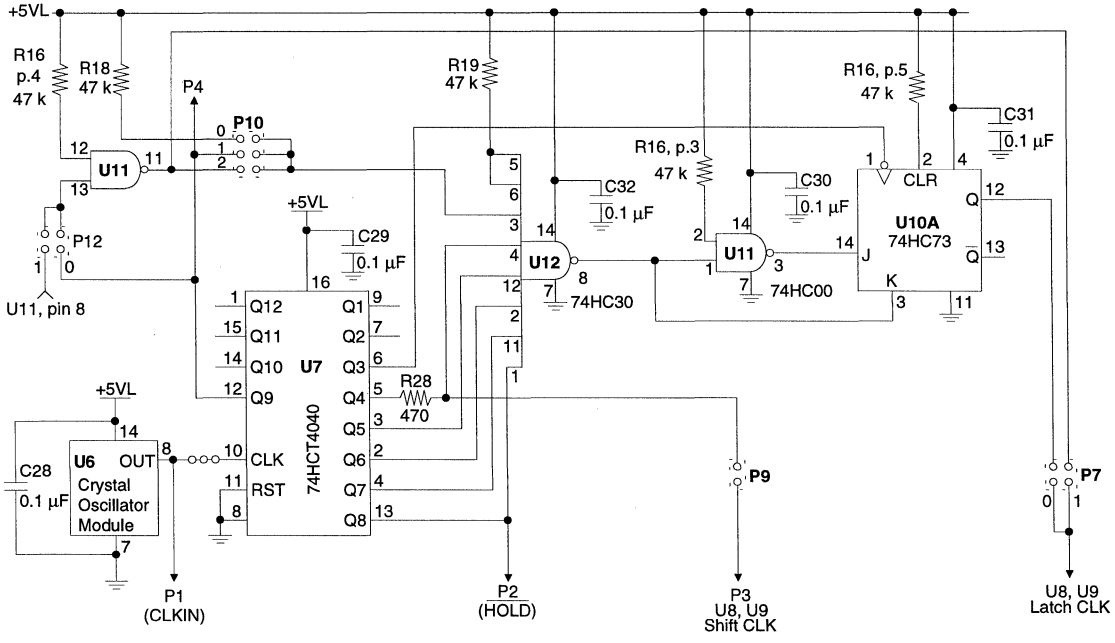


Figure 5. Timing Generator

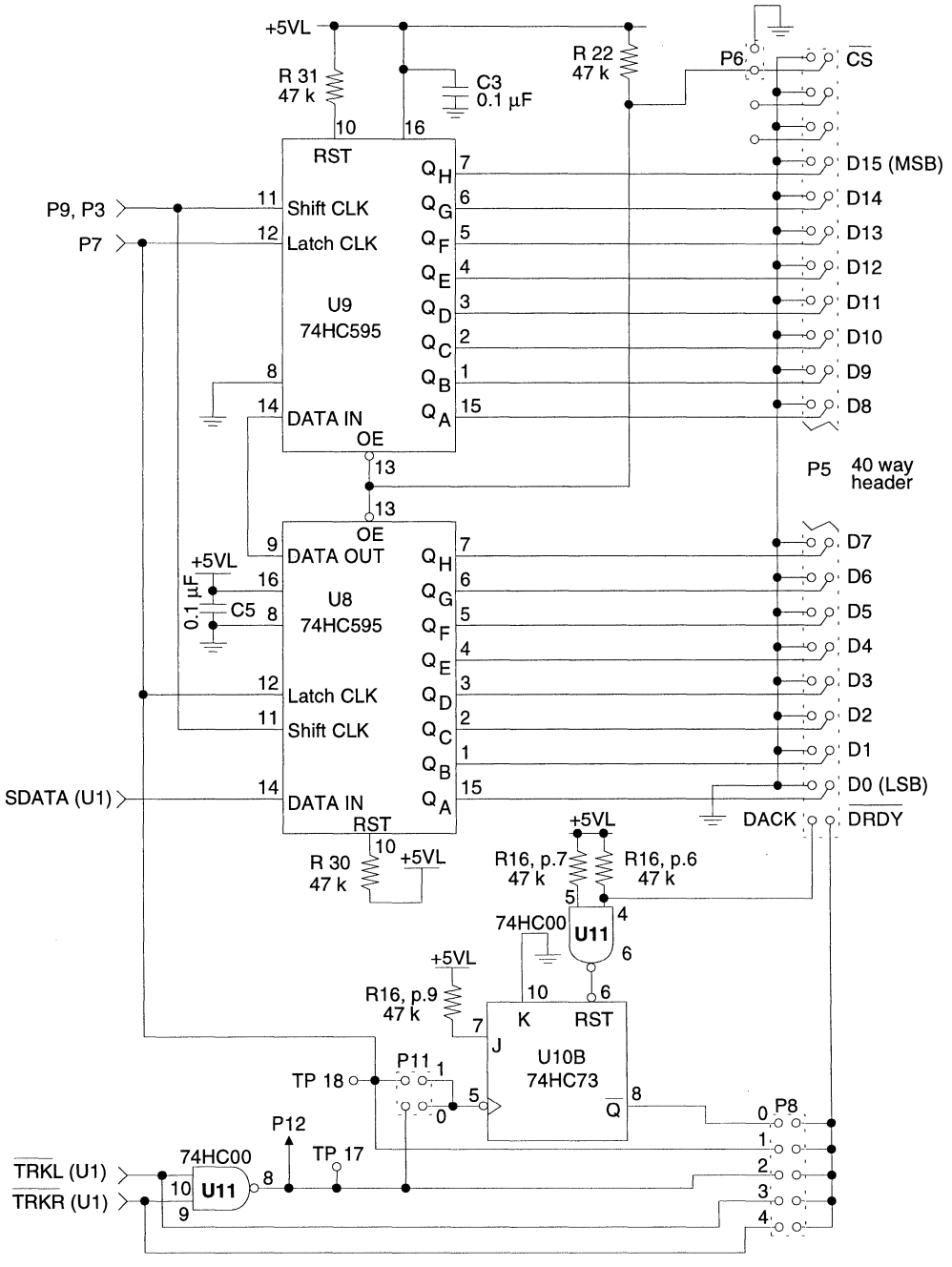


Figure 6. Serial to Parallel Converter

J1	-	Joins analog ground to digital ground on the board.
J2	-	Joins LT1019-5 reference directly to the VREF pin on the ADC. Before doing this, break the connection between R3 and the ADC VREF pin by using a twist drill to remove the central feedthrough. This option allows evaluation of different reference configurations.
J4	-	Connects an external clock to CLKIN on the ADC.

Table 1. Solder Link Options

P1		0 -	Select external clock via BNC connector
	*	1 -	Select on-board clock generated by U6.
P2	*	0 -	Select on-board generated $\overline{\text{HOLD}}$.
		1 -	Select external $\overline{\text{HOLD}}$ via BNC connector.
P3	*		Connect SCLK to on-board shift registers.
P4	*	0 –	Pull L/$\overline{\text{R}}$ select pin high, selecting the left channel only.
		1 -	Drive L/$\overline{\text{R}}$ select at 48 kHz from the on-board timing generator.
		2 -	Pull L/$\overline{\text{R}}$ select pin low, selecting the right channel only.
P6	*		Connect the $\overline{\text{OE}}$ pins of the shift registers to ground. Permanently enables the 3-state output buffers.
P7	*	0 -	Connects the on-board Data Ready signal to the shift registers.
		1 -	Connects the NAND gate outputs (U11, pin 11) to the shift registers.
P8	*	1 -	Connects the un-latched on-board Data Ready signal to P5.
		2 -	Connects $\overline{\text{TRKL}}$ and $\overline{\text{TRKR}}$ *ANDED* together to P5. This signal can be used as an "End of Convert" indicator.
		3 -	Connects $\overline{\text{TRKL}}$ to P5.
		4 -	Connects $\overline{\text{TRKR}}$ to P5.
P9	*		Connects the on-board generated SCLK to the rest of the on-board circuitry.
P10	*	0 -	Causes the on-board Data Ready generating circuit to flag data ready every conversion.
		1 -	Causes the on-board Data Ready generating circuit to flag data ready every left conversion. P4 must be in position 1 for this to work.
		2 -	Causes the on-board Data Ready generating circuit to flag data ready every right conversion. P4 must be in position 1 for this to work.
P11		0 -	Connects $\overline{\text{TRKL}}$ & $\overline{\text{TRKR}}$ to U10B, the handshake flip-flop.
	*	1 -	Connects the on-board data ready signal to U10B.
P12	*	0 -	Allows selection of the $\overline{\text{DRDY}}$ signals for alternate channels.
		1 -	Connects the $\overline{\text{TRKL}}$ & $\overline{\text{TRKR}}$ to U11, pin 13.
*		*Factory default state for CS5126*	

Table 2. Shorting Plug Selectable Options

U10B (74HC73) is used as a handshake flip-flop with the computer system attached to the evaluation board. The board brings $\overline{\text{DRDY}}$ low. The computer reads the data and then sets DACK momentarily high. This resets U10B for the next word. This handshake can be disabled by setting P8 jumper to position 1.

DIP Switches

Figure 7 and Table 3 shows the DIP switch selectable options.

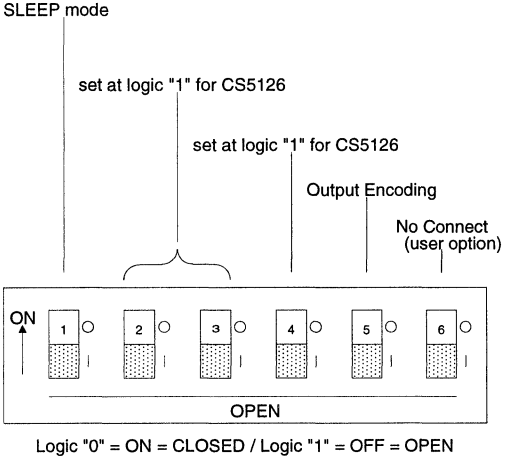


Figure 7. DIP switch configuration

Switch	Logic	Mode
1	0	SLEEP mode
	1	Normal mode
2, 3, 4		set to "1" for CS5126
5	0	Offset binary output code
	1	2's complement output code
6		Unconnected. Available for user's applications

Table 3. DIP Switch Selection Options

Test Points

Table 4 is a list of the test points provided on the Evaluation Board.

	CS5126
TP1	VREF
TP2	AINR
TP3	AINL
TP4	AGND
TP5	SSH2
TP6	SSH1
TP7	$\overline{\text{TRKR}}$
TP8	$\overline{\text{TRKL}}$
TP9	$\overline{\text{STBY}}$
TP10	NC
TP11	L/$\overline{\text{R}}$
TP12	SCLK
TP13	$\overline{\text{HOLD}}$
TP14	SDATA
TP15	CLKIN
TP16	DGND
TP17	$\overline{\text{TRKL}}$ + $\overline{\text{TRKR}}$
TP18	Latch Clock for the 74HC595 shift registers

Table 4. CDB5126 Test Points

Miscellaneous Hints on Using the Evaluation Board

Always hit the reset button after powering-up the board. The CS5126 is self calibrating and require the reset signal to initiate the calibration procedure.

P4 controls the ADC input mux. This is used to set the mux to be continuously connected to one channel, or to be toggling between two channels. This is very useful for evaluating oversampled vs. regular sampling digital audio.

P10 controls the Data Ready pulses from the on-board logic. To cause every data sample to be read, select option 0. If you wish to read only every alternate sample, then select option 1 or 2, depending on whether you wish to read every left channel value, or every right channel value. This is useful for evaluating the part with a test system which does not separate alternate values.

CDBCAPTURE Interface

Figure 8 illustrates the CDBCAPTURE interface that can be constructed in the digital patch area. A 2-row, 10 pin stake header is wired as shown.

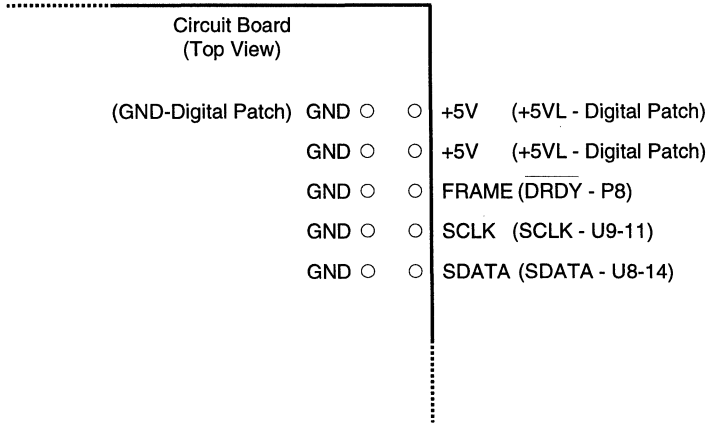


Figure 8. CDBCAPTURE Header Signal Pattern

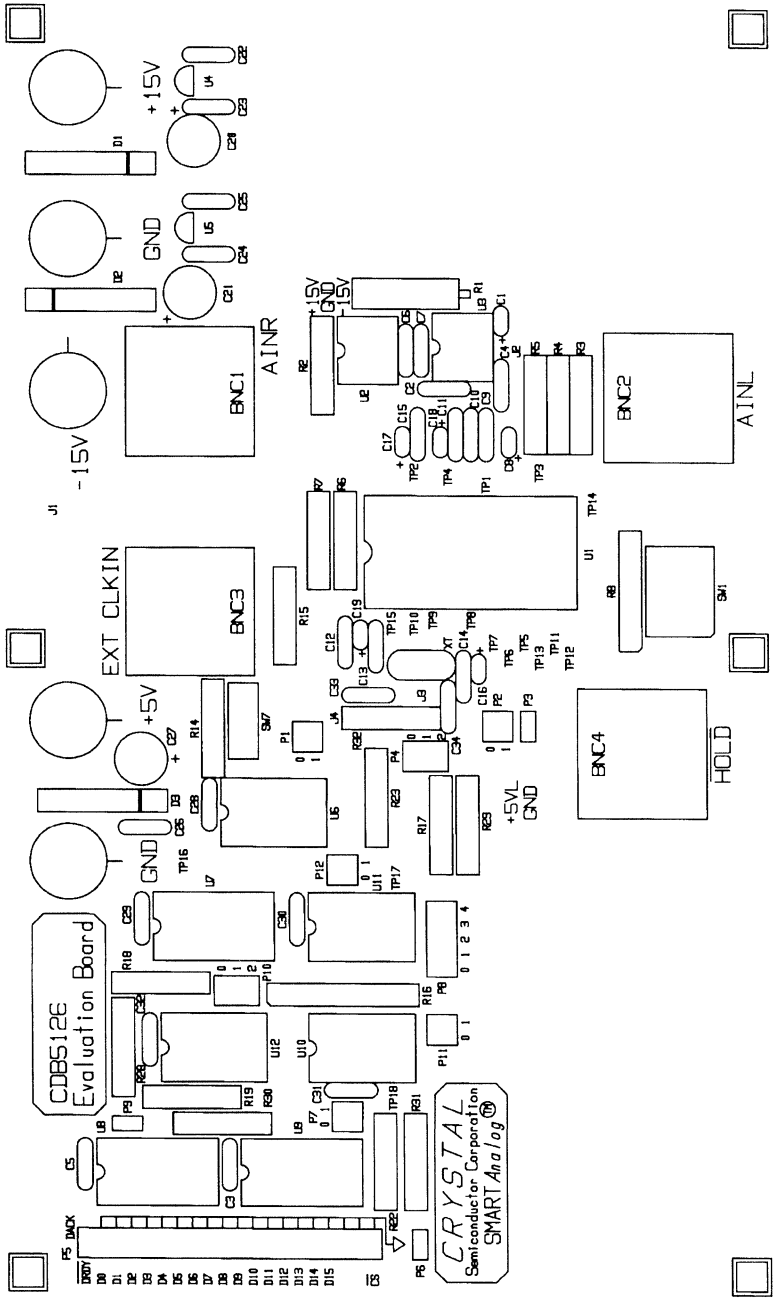


Figure 9. CDB5126 Component Layout

• Notes •

16-Bit, 20 kHz Oversampling A/D Converter

Features

- Complete Voiceband DSP Front-End
  - 16-Bit A/D Converter
  - Internal Track & Hold Amplifier
  - On-Chip Voltage Reference
  - Linear-Phase Digital Filter
- On-Chip PLL for Simplified Output Phase Locking in Modem Applications
- 84 dB Dynamic Range
- 80 dB Total Harmonic Distortion
- Output Word Rates up to 20 kHz
- DSP-Compatible Serial Interface
- Low Power Dissipation: 220 mW

General Description

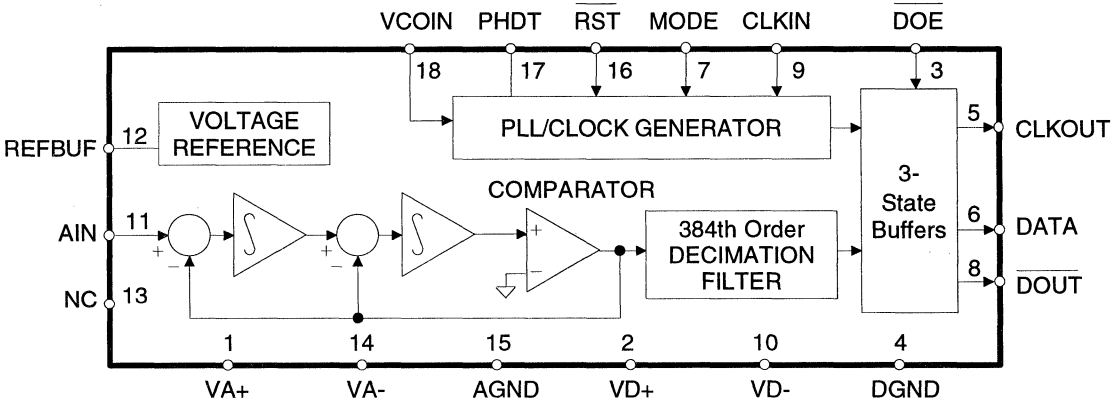
The CS5317 is an ideal analog front-end for voiceband signal processing applications such as high-performance modems, passive sonar, and voice recognition systems. It includes a 16-bit A/D converter with an internal track & hold amplifier, a voltage reference, and a linear-phase digital filter.

An on-chip phase-lock loop (PLL) circuit simplifies the CS5317's use in applications where the output word rate must be locked to an external sampling signal.

The CS5317 uses delta-sigma modulation to achieve 16-bit output word rates up to 20 kHz. The delta-sigma technique utilizes oversampling followed by a digital filtering and decimation process. The combination of oversampling and digital filtering greatly eases antialias requirements. Thus, the CS5317 offers 84 dB dynamic range and 80 dB THD and signal bandwidths up to 10 kHz at a fraction of the cost of hybrid and discrete solutions.

The CS5317's advanced CMOS construction provides low power consumption of 220 mW and the inherent reliability of monolithic devices.

ORDERING INFORMATION: Page 2-208



ANALOG CHARACTERISTICS ($T_A = T_{MIN}$ - T_{MAX}; VA+, VD+ = 5V ±10%; VA-, VD- = -5V ±10%; CLKIN = 4.9152 MHz in CLKOR mode; 1kHz Input Sinewave; with 1.2 kΩ, .01 µF antialiasing filter.)

Parameter*		Min	Typ	Max	Units
Specified Temperature Range			0 to 70		°C
Resolution		16	-	-	Bits
Dynamic Performance					
Dynamic Rnage	(Note 1)	78	84	-	dB
Total Harmonic Distortion		72	80	-	dB
Signal to Intermodulation Distorition		-	84	-	dB
dc Accuracy					
Differential Nonlinearity	(Note2)	-	±0.4	-	LSB
Positive Full-Scale Error		-	±150	-	mV
Positive Full-Scale Drift		-	±500	-	µV/°C
Bipolar Offset Error		-	±10	-	mV
Bipolar Offset Drift		-	±50	-	µV/°C
Filter Characteristics					
Absolute Group Delay	(Note 3)	78.125	-	-	µs
Passband Frequency	(Note 4)	-	5	-	kHz
Input Characteristics					
AC Input Impedance	(1kHz)	-	80	-	kΩ
Analog Input Full Scale Signal Level		±2.75	-	-	V
Power Supplies					
Power Dissipation	(Note5)	-	220	300	mW

Notes:
1. Measured over the full 0 to 9.6kHz band with a -20dB input and extrapolated to full-scale. Since this includes energy in the stopband above 5kHz, additional post-filtering at the CS5317's output can typically achieve 88dB dynamic range by improving rejection above 5kHz. This can be increased to 90dB by bandlimiting the output to 2.5kHz.
2. No missing codes is guaranteed by design.
3. Group delay is constant with respect to input analog frequency; that is, the digital FIR filter has linear phase. Group delay is determined by the formula D_{grp} = 384/CLKIN in CLKOR mode, or 192/CLKOUT in any mode.
4. The digital filter's frequency response scales with the master clock. Its -3dB point is determined by f_{-3dB} = CLKIN/977.3 in CLKOR mode, or CLKOUT/488.65 in any mode.
5. All outputs unloaded. All inputs CMOS levels.

* Refer to the *Parameter Definitions* section after the Pin Description section.

ANALOG CHARACTERISTICS (continued)

Parameter			Min	Typ	Max	Units
Power Supply Rejection	VA+	(Note 6)	-	60	-	dB
	VA-		-	45	-	dB
	VD+		-	60	-	dB
	VD-		-	55	-	dB
Specified Temperature Range			0 to 70			°C
Phase-Lock Loop Characteristics						
VCO Gain Constant, Ko		(Note 7)	-4	-10	-30	Mrad/Vs
VCO Operating Frequency			1.28	-	5.12	MHz
Phase Detector Gain Control, Kd			-3	-8	-12	µA/rad
Phase Detector Prop. Delay		(Note 8)	-	50	100	ns

Notes: 6. With 300mV p-p, 1kHz ripple applied to each supply separately.
7. Over 1.28 MHz to 5.12 MHz VCO output range, where VCO frequency = 2 * CLKOUT.
8. Delay from an input edge to the phase detector to a response at the PHDT output pin.

DIGITAL CHARACTERISTICS ($T_A = T_{MIN}$ - T_{MAX}; VA+, VD+ = 5V±10%; VA-, VD- = -5V±10%)

All measurements performed under static conditions.

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage		V_{IH}	2.0	-	-	V
Low-Level Input Voltage		V_{IL}	-	-	0.8	V
High-Level Output Voltage	(Note 9)	V_{OH}	(VD+)-1.0V	-	-	V
Low-Level Output Voltage	I_{OUT} = 1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	-	10	µA
3-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

Note: 9. I_{out}=-100µA. This specification guarantees the ability to drive one TTL load (V_{OH}=2.4V @ I_{out}=-40µA.).

RECOMMENDED OPERATING CONDITIONS (DGND, AGND = 0V, see Note 10.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	5.5	V
	Negative Digital	VD-	-4.5	-5.0	-5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	-4.5	-5.0	-5.5	V
Master Clock Frequency		f_{clk}	0.01	-	5.12	MHz

Note: 10. All voltages with respect to ground.

Specifications are subject to change without notice.

SWITCHING CHARACTERISTICS ($T_A = T_{MIN}$-T_{MAX}; C_L=50 pF; VD+ = 5V±10%; VD- = -5V±10%)

Parameter			Symbol	Min	Typ	Max	Units
Master Clock Frequency:	CLKIN						
	CLKG1 Mode		f_{clkg1}	-	-	20	kHz
	CLKG2 Mode		f_{clkg2}	-	-	10	kHz
	CLKOR Mode		f_{clkor}	-	-	5.12	MHz
Output Word Rate:	$\overline{DOUT}$		f_{dout}	-	-	20	kHz
Rise Times:	Any Digital Input		t_{risein}	-	20	1000	ns
	Any Digital Output		$t_{riseout}$	-	15	20	ns
Fall Times:	Any Digital Input		t_{fallin}	-	20	1000	ns
	Any Digital Output		$t_{fallout}$	-	15	20	ns
CLKIN Duty Cycle							
CLKG1 and CKLG2 Modes		Pulse Width Low	t_{pwl1}	200	-	-	ns
		Pulse Width High	t_{pwh1}	200	-	-	ns
CLKOR Mode		Pulse Width Low	t_{pwl1}	45	-	-	ns
		Pulse Width High	t_{pwh1}	45	-	-	ns
$\overline{RST}$ Pulse Width Low			t_{pwr}	400	-	-	ns
Set Up Times:	$\overline{RST}$ High to CLKIN High		t_{su1}	40	-	-	ns
	CLKIN High to $\overline{RST}$ High		t_{su2}	40	-	-	ns
Propagation Delays:							
$\overline{DOE}$ Falling to Data Valid			t_{phl1}	-	-	150	ns
CLKIN Rising to $\overline{DOUT}$ Falling		(Note 11)	t_{phl2}	-	1	-	CLKOUT
$\overline{DOE}$ Rising to Hi-Z Output			t_{plh1}	-	-	80	cycles
CLKOUT Rising to $\overline{DOUT}$ Falling			t_{plh2}	-	-	60	ns
CLKOUT Rising to $\overline{DOUT}$ Rising			t_{plh3}	-	-	60	ns
CLKOUT Rising to Data Valid			t_{plh4}	-	-	100	ns
CLKIN Rising to CLKOUT Falling		(Note 12)	t_{plh5}	-	-	200	ns
CLKIN Rising to CLKOUT Rising		(Note 12)	t_{plh6}	-	-	200	ns

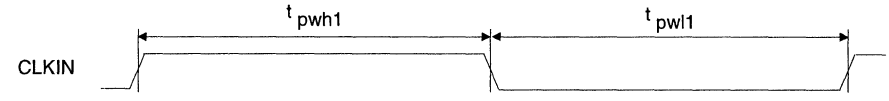
Notes: 11. CLKIN only pertains to CLKG1 and CLKG2 modes.
12. Only valid in CLKOR mode.

ABSOLUTE MAXIMUM RATINGS (DGND, AGND = 0V, all voltages with repect to groung)

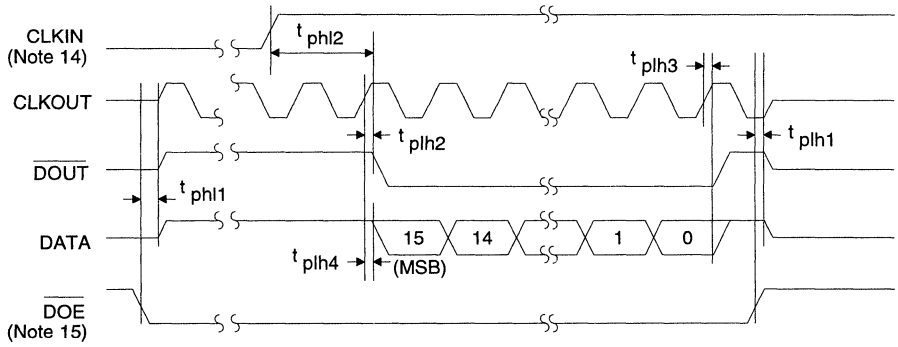
Parameter			Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital		VD+	-0.3	(VA+) + 0.3	V
	Negative Digital		VD-	0.3	-6.0	V
	Positive Analog		VA+	-0.3	6.0	V
	Negative Analog		VA-	0.3	-6.0	V
Input Current, Any Pin Except Supplies		(Note 13)	I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)			V_{INA}	(VA-) - 0.3	(VA+) + 0.3	V
Digital Input Voltage			V_{IND}	-0.3	(VD+) + 0.3	V
Ambient Operating Temperature			T_A	-55	125	°C
Storage Temperature			T_{stg}	-65	150	°C

Notes: 13. Transient currents up to 100mA will not cause SCR latch-up.
WARNING:Operating this device at or beyond these extremes may result in permanent damage to the device. Normal operation of the part is not guaranteed at these extremes.

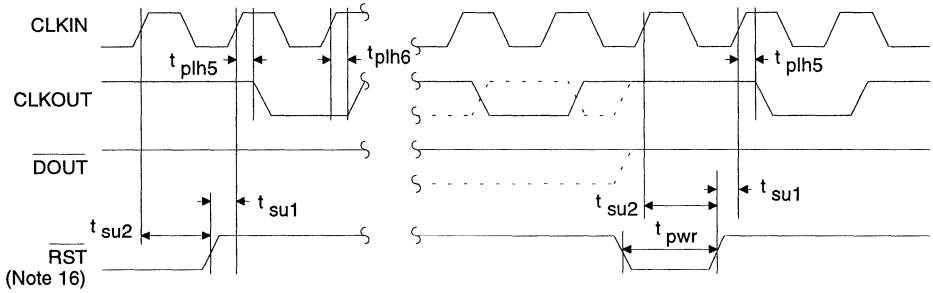
Rise and Fall Times



CLKIN Timing



Serial Output Timing



Reset Timing

Notes: 14. CLKIN only pertains to CLKG1 and CLKG2 modes.
15. If $\overline{DOE}$ is brought high during serial data transfer, CLKOUT, $\overline{DOUT}$, and DATA will immediately 3-state and the rest of the serial data is lost.
16. $\overline{RST}$ must be held high except in the clock override (CLKOR) mode where it can be used to align the phases of all internal clocks.

GENERAL DESCRIPTION

The CS5317 functions as a complete data conversion subsystem for voiceband signal processing. The A/D converter, sample/hold, voltage reference, and much of the antialiasing filtering are performed on-chip. The CS5317's serial interface offers its 16-bit, 2's complement output in a format which easily interfaces with industry-standard micro's and DSP's.

The CS5317 also includes a phase-locked loop that simplifies the converter's application in systems which require sampling to be locked to an external signal source. The CS5317 continuously samples its analog input at a rate set by an external clock source. On-chip digital filtering, an integral part of the delta-sigma ADC, processes the data and updates the 16-bit output register at up to 20 kHz. The CS5317 can be read at any rate up to 20 kHz.

The CS5317 is a CS5316 with an on-chip sampling clock generator. As such, it replaces the CS5316 and should be considered for all new designs. In addition, a CS5316 look-alike mode is included, allowing a CS5317 to be dropped into a CS5316 socket.

THEORY OF OPERATION

The CS5317 utilizes the delta-sigma technique of executing low-cost, high-resolution A/D conversions. A delta-sigma A/D converter consists of two basic blocks: an analog modulator and a digital filter.

Conversion

The analog modulator consists of a 1-bit A/D converter (that is, a comparator) embedded in an analog negative feedback loop with high open-loop gain. The modulator samples and converts the analog input at a rate well above the bandwidth of interest (2.5 MHz for the CS5317). The modulator's 1-bit output conveys information in the form of duty cycle. The digital filter then processes the 1-bit signal and extracts a high resolution output at a much lower rate (that is, 16-bits at a 20 kHz word rate with a 5 kHz input bandwidth).

An elementary example of a delta-sigma A/D converter is a conventional voltage-to-frequency converter and counter. The VFC's 1-bit output conveys information in the form of frequency (or duty-cycle), which is then filtered (averaged) by the counter for higher resolution. In comparison, the CS5317 uses a more sophisticated multi-order modulator and more powerful FIR filtering to extract higher word rates, much lower noise, and more useful system-level filtering.

Filtering

At the system level, the CS5317's digital filter can be modeled exactly like an analog filter with a few minor differences. First, digital filtering resides *behind* the A/D conversion and can thus reject noise injected during the conversion process (i.e. power supply ripple, voltage reference noise, or noise in the ADC itself). Analog filtering cannot.

Also, since digital filtering resides behind the A/D converter, noise riding unfiltered on a near-full-scale input could potentially saturate the ADC. In contrast, analog filtering removes the noise before it ever reaches the converter. To address this issue, the CS5317's analog modulator and digital filter reserve headroom such that the device can process signals with 100mV "excursions" above full-scale and still output accurately converted and filtered data. Filtered input signals above full-scale still result in an output of all ones.

An Application Note called "Delta Sigma Overview" contains more details on delta-sigma conversion and digital filtering.

SYSTEM DESIGN WITH THE CS5317

Like a tracking ADC, the CS5317 continuously samples and converts, always tracking the analog input signal and updating its output register at a 20 kHz rate. The device can be read at any rate to create any system-level sampling rate desired up to 20kHz.

Clocking

Oversampling is a critical function in delta-sigma A/D conversion. Although system-level *output* sample rates typically remain between 7kHz and 20kHz in voiceband applications, the CS5317 actually samples and converts the analog input at rates up to 2.56 MHz. This *internal* sampling rate is typically set by a master clock which is on the order of several megahertz. See Table1 for a complete description of the clock relationships in the various CS5317 operating modes.

Some systems such as echo-canceling modems, though, require the *output* sampling rate to be locked to a sampling signal which is 20 kHz or below. For this reason the CS5317 includes an on-chip phase-lock loop (PLL) which can generate its requisite 5.12 MHz master clock from a 20 kHz sampling signal.

The CS5317 features two modes of operation which utilize the internal PLL. The first, termed *Clock Generation 1* (CLKG1), accepts a sampling clock up to 20 kHz at the CLKIN pin and internally generates the requisite 5.12 MHz clock. The CS5317 then processes samples updating its output register at the rate defined at CLKIN, typically 20 kHz. For a 20 kHz clock input the digital filter's 3 dB corner is set at 5.239 kHz, so *CLKG1 provides a factor of 2X oversampling at the system level* (20 kHz is twice the minimum possible sampling frequency needed to reconstruct a 5 kHz input). The CLKG1 mode is initiated by tying the MODE input to +5V.

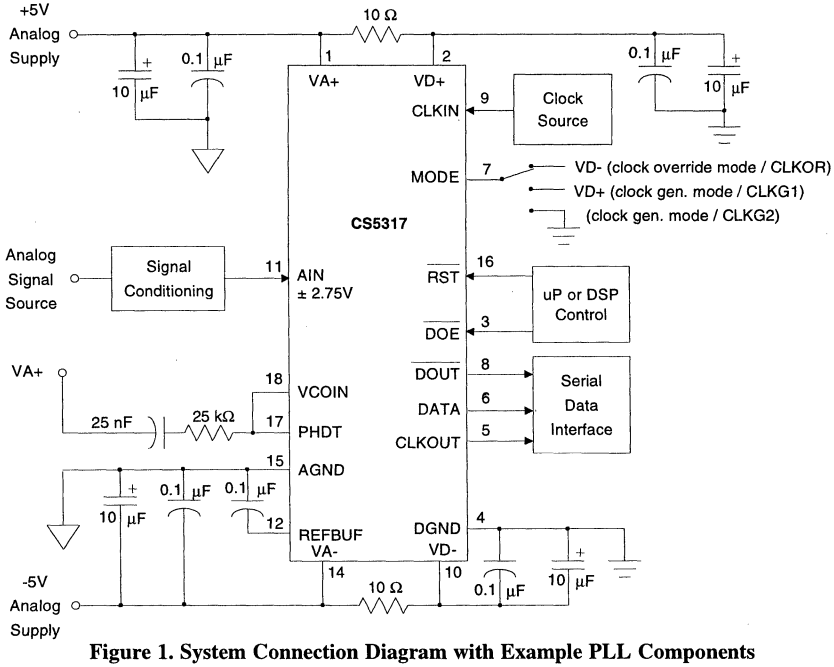


Figure 1. System Connection Diagram with Example PLL Components

Mode	Symbol	Mode Pin	RESET	Output Word Rate Provides System-level 2X Oversampling	CLKIN (kHz)	CLKOUT f_{sin} (MHz)	$\overline{DOUT}$ f_{sout} (kHz)	F (kHz)	t_{dcD}* (ns)
Clock Gen. 2	CLKG2	0V	HIGH	NO	7.2	1.8432	7.2	14.4	542.5
	CLKG2				9.6	2.4576	9.6	19.2	406.9
	CLKG2				10.0 (max)	2.56	10.0	20.0	390.6
Clock Gen. 1	CLKG1	+5V	HIGH	YES	14.4	1.8432	14.4	14.4	542.5
	CLKG1				19.2	2.4576	19.2	19.2	406.9
	CLKG1				20.0 (max)	2.56	20.0	20.0	390.6
Clock Override	CLKOR	-5V	SYNC	YES	3686.4	1.8432	14.4	14.4	N/A
	CLKOR				4915.2	2.4576	19.2	19.2	N/A
	CLKOR				5120.0 (max)	2.56	20.0	20.0	N/A
CS5316	CS5316	FSYNC	LOW	YES	5120.0 (max)	2.56	20.0	20.0	N/A

* t_{dcD} - Delay from CLKIN rising to $\overline{DOUT}$ falling = 1 CLKOUT cycle

Table 1. Mode Comparisons

The second PLL mode is termed *Clock Generation 2* (CLKG2) which generates its 5.12 MHz clock from a *10 kHz* external sampling signal. Again, output samples are available at the system sampling rate set by CLKIN, typically 10 kHz. For the full-rated 10 kHz clock CLKG2 still sets the filter's 3 dB point at 5 kHz. Therefore, *CLKG2 provides no oversampling* beyond the Nyquist requirement at the system level (10 kHz : 5 kHz) and its internal digital filter provides little anti-aliasing value. The CLKG2 mode is initiated by grounding the MODE pin.

The CS5317 features a third operating mode called *Clock Override* (CLKOR). Initiated by tying the MODE pin to -5V, CLKOR allows the 5.12 MHz master clock to be driven directly into the CLKIN pin. The CS5317 then processes samples updating its output register at $f_{clkin}/256$. Since all clocking is generated internally, the CLKOR mode includes a *Reset* capability which allows the output samples of multiple CS5317's to be synchronized.

The CS5317 also has a CS5316 compatible mode, selected by tying $\overline{RST}$ low, and using MODE (pin 7) as the FSYNC pin. See the CS5316 data sheet for detailed timing information.

Analog Design Considerations

DC Characteristics

The CS5317 was designed for signal processing. Its analog modulator uses CMOS amplifiers resulting in offset and gain errors which drift over temperature. If the CS5317 is being considered for low-frequency (< 10 Hz) measurement applications, Crystal Semiconductor recommends the CS5501, a low-cost, d.c. accurate, delta-sigma ADC featuring excellent 60 Hz rejection and a system-level calibration capability.

The Analog Input Range and Coding Format

The input range of the CS5317 is nominally ± 3V, with ± 250 mV possible gain error. Because of this gain error, analog input levels should be kept below ± 2.75V. The converter's serial output appears MSB-first in 2's complement format.

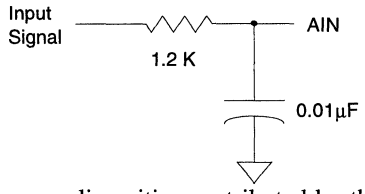
Antialiasing Considerations

In applying the CS5317, aliasing occurs during both the initial sampling of the analog input at $f_{s_{in}}$ (~2.5 MHz) and during the digital decimation process to the 16-bit output sample rate, $f_{s_{out}}$.

Initial Sampling

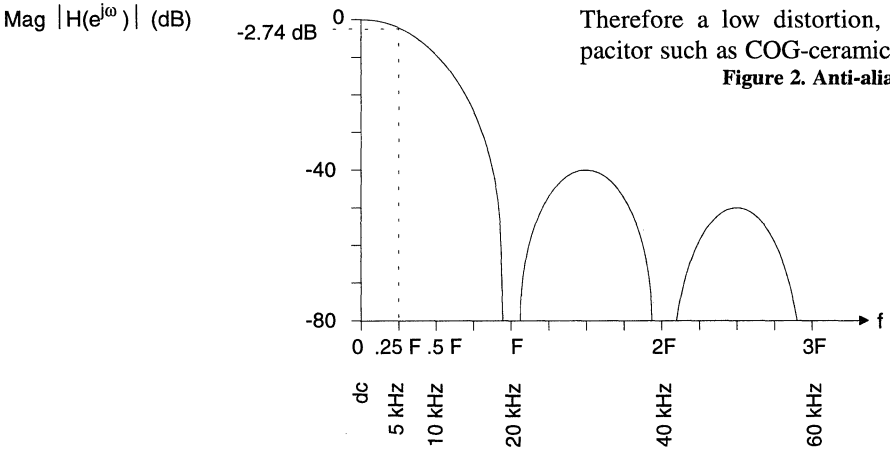
The CS5317 samples the analog input, AIN, at one-half the master clock frequency (~2.5 MHz max). The input sampling frequency, f_{sin}, appears at CLKOUT regardless of whether the master clock is generated on-chip (CLKG1 and CLKG2 modes) or driven directly into the CS5317 (CLKOR mode). The digital filter then processes the input signal at the input sample rate.

Like any sampled-data filter, though, the digital filter's passband spectrum repeats around integer multiples of the sample rate, f_{sin}. That is, when the CS5317 is operating at its full-rated speed any noise within ± 5 kHz bands around 2.5 MHz, 5 MHz, 7.5 MHz, etc. will pass unfiltered and alias into the baseband. Such noise can only be filtered by analog filtering *before the signal is sampled.* Since the signal is heavily oversampled (2.5 MHz : 5 kHz, or 500 : 1), a single-pole passive RC filter can be used as shown in Figure 2.



Note: Any nonlinearities contributed by this filter will be encoded as distortion by the CS5317. Therefore a low distortion, high frequency capacitor such as COG-ceramic is recommended.

Figure 2. Anti-alias Filter



$$\left|\left(\frac{\sin(128\pi fT)}{128\sin(\pi fT)}\right)^3\right| =$$ Magnitude where: $T = 1/f_{sin}$

f_{sin} = input sampling frequency = CLKOUT frequency for all modes
= CLKIN/2 in CLKOR mode
= CLKIN*128 in CLKG1 mode
= CLKIN*256 in CLKG2 mode
$F = f_{sin}/128$ for all modes
f = input frequency
$f_{sout} = f_{sin}/128$ = output data rate for CLKOR & CLKG1 = F
$f_{sout} = f_{sin}/256$ = output data rate for CLKG2 = F/2

Examples: For f_{sin} = 2.56 MHz at f = 5 kHz: Magnitude is -2.74 dB
For f_{sin} = 2.56 MHz at f = 10 kHz: Magnitude is -11.8 dB

Figure 3. CS5317 Low-Pass Filter Response

Decimation

Aliasing effects due to decimation are identical in the CLKOR and CLKG1 modes. Aliasing is different in the CLKG2 mode due to the difference in output sample rates (10 kHz vs. 20 kHz) and thus will be discussed separately.

Aliasing in the CLKOR and CLKG1 Modes

The delta-sigma modulator output is fed into the digital low-pass filter at the input sampling rate, $f_{s_{in}}$. The filter's frequency response is shown in Figure 3. In the process of filtering the digitized signal the filter *decimates* the sampling rate by 128 (that is, $f_{s_{out}} = f_{s_{in}}/128$). In its most elementary form, decimation simply involves ignoring - or selectively reading - a fraction of the available samples.

In the process of decimation the output of the digital filter is effectively *resampled* at $f_{s_{out}}$, the output word rate, *which has aliasing implications.* Residual signals *after filtering* at multiples of $f_{s_{out}}$ will alias into the baseband. For example, an input tone at 28 kHz will be attenuated by 39.9 dB. If $f_{s_{out}}$ = 20 kHz, the residual tone will alias into the baseband and appear at 8 kHz in the output spectrum.

If the input signal contains a large amount of out-of-band energy, additional analog and/or digital antialias filtering may be required. If digital post-filtering is used to augment the CS5317's rejection above $f_{s_{out}}/4$ (that is, above 5 kHz), the filtering will also reject residual quantization noise from the modulator. This will typically increase the converter's dynamic range to 88 dB. Further bandlimiting the digital output to $f_{s_{out}}/8$ (2.5 kHz at full speed) will typically increase dynamic range to 90 dB.

Aliasing in the CLKG2 Mode

Aliasing effects in the CLKG2 mode can be modeled exactly as those in the CLKG1 mode with the output decimated by two (from 20 kHz to 10 kHz). This is most easily achieved by ignoring every other sample. In the CLKG2 mode the ratio of the output sampling rate to the filter's -3 dB point is two, with no oversampling beyond the demands of the Nyquist criterion. Without the ability to roll-off substantially before $f_{s_{out}}/2$, the on-chip digital filter's antialiasing value is diminished.

The CLKG2 mode should therefore be used only when the output data rate must be minimized due to communication and/or storage reasons. In addition, adequate analog filtering must be provided prior to the A/D converter.

Digital Design Considerations

The CS5317 presents its 16-bit serial output MSB-first in 2's complement format. The converter's serial interface was designed to easily interface to a wide variety of micro's and DSP's. Appendix A offers several hardware interfaces to industry-standard processors.

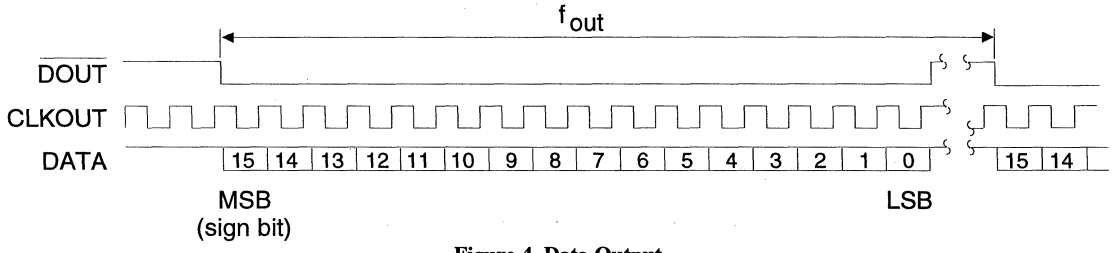


Figure 4. Data Output

Data Output Characteristics & Coding Format

As shown in Figure 4, the CS5317 outputs its 16-bit data word in a serial burst. The data appears at the DATA pin on the rising edge of the same CLKOUT cycle in which $\overline{DOUT}$ falls. Data changes on the rising edge of CLKOUT, and can be latched on the falling edge. The CLKOUT rate is set by the CLKIN input ($f_{clkin}/2$ in the CLKOR mode; $f_{clkin}*128$ in the CLKG1 mode; and $f_{clkin}*256$ in the CLKG2 mode). $\overline{DOUT}$ returns high after the last bit is transmitted. After transmitting the sixteen data bits, DATA will remain high until $\overline{DOUT}$ falls again, initiating the next data output cycle.

A 3-state capability is available for bus-oriented applications. The 3-state control input is termed Data Output Enable, $\overline{DOE}$, and is asynchronous with respect to the rest of the CS5317. If $\overline{DOE}$ is taken high at any time, even during a data burst, the DATA, $\overline{DOUT}$ and CLKOUT pins go to a high impedance state. Any data which would be output while $\overline{DOE}$ is high is lost.

Power Supplies

Since the A/D converter's output is digitally filtered in the CS5317, the device is more forgiving and requires less attention than conventional 16-bit A/D converters to grounding and layout arrangements. Still, care must be taken at the design and layout stages to apply the device properly. The CS5317 provides separate analog and digital power supply connections to isolate digital noise from its analog circuitry. Each supply pin should be decoupled to its respective ground, AGND or DGND. Decoupling should be accomplished with 0.1 µF ceramic capacitors. If significant low frequency noise is present in the supplies, 10 µF tantalum capacitors are recommended in parallel with the 0.1 µF capacitors.

The positive digital power supply of the CS5317 must never exceed the positive analog supply by more than a diode drop or the chip could be permanently damaged. If the two supplies are derived from separate sources, care must be taken that the analog supply comes up first at power-up. Figure 1 shows a decoupling scheme which allows the CS5317 to be powered from a single set of ± 5V rails. The digital supplies are derived from the analog supplies through 10 Ω resistors to prevent the analog supply from dropping below the digital supply.

PLL Characteristics

A phase-locked loop is included on the CS5317 and is used to generate the requisite high frequency A/D sampling clock. A functional diagram of the PLL is shown in Figure 5. The PLL consists of a phase detector, a filter, a VCO (voltage-controlled oscillator), and a counter/divider. The phase detector inputs are CLKIN (θ_1) and a sub-multiple of the VCO output signal (θ_2). The inputs to the phase detector are positive-edge triggered and therefore the duty cycle of the CLKIN signal is not significant. With this type of phase detector, the lock range of the PLL is equal to the capture range and is independent of the low pass filter. The output of the phase detector is input to an external low pass filter. The filter characteristics are used to determine the transient response of the loop. The output voltage from the filter functions as the input control voltage to the VCO. The output of the VCO is then divided in frequency to provide an input to the phase detector. The clock divider ratio is a function of the PLL mode which has been selected.

Phase Detector Gain (Kd)

A properly designed and operating phase-locked loop can be described using steady state linear analysis. Once in frequency lock, any phase difference between the two inputs to the phase detector cause a current output from the detector during the phase error. While either the +50 µA or the -50 µA current source may be turned on, the average current flow is:

$$i_{out_{avg}} = Kd(\theta_1 - \theta_2) \approx (-50\mu A/2\pi)\ (\theta_1 - \theta_2)$$

where θ_1 is the phase of IN1, θ_2 is the phase of IN2 and Kd is the phase detector gain. The factor 2π comes from averaging the current over a full CLKIN cycle. Kd is in units of micro-amperes/radian.

VCO Gain (Ko)

The output frequency from the VCO ranges from 1.28 MHz to 5.12 MHz. The frequency is a function of the control voltage input to the VCO. The VCO has a negative gain factor, meaning that as the control voltage increases more positively the output frequency decreases. The gain factor units are Megaradians per Volt per Second. This is equivalent to 2π Megahertz per volt. Changes in output frequency are given by:

$$\Delta\omega_{vco} = Ko\ \Delta VCO_{in} \quad [Ko \text{ is typ. } -10Mrad/Vs.]$$

Counter/Divider Ratio

The CS5317 PLL multiplies the CLKIN rate by an integer value. To set the multiplication rate, a counter/divider chain is used to divide the VCO output frequency to develop a clock whose frequency is compared to the CLKIN frequency in the phase detector. The binary counter/divider ratio sets the ratio of the VCO frequency to the CLKIN frequency. As illustrated in Figure 5, the VCO output is always divided by two to yield the CLKOUT signal which is identical in frequency to the delta-sigma modulator sampling clock. The CLKOUT signal is then further divided by either 128 in the CLKG1 mode or by 256 in the CLKG2 mode. When the divide by two stage is included, the divider ratio (N) for the PLL in the CLKG1 mode is effectively 256. In the CLKG2 mode the divider ratio (N) is 512.

Loop Transfer Function

As the phase-locked loop is a closed loop system, an equation can be determined which describes its closed loop response. Using the gain factors for the phase detector and the VCO, the filter arrangement and the counter/divider constant N, analysis will yield the following equation which describes the transfer function of the PLL:

$$\frac{\theta_2}{\theta_1} = \frac{\frac{KoKdR}{N}s + \frac{KoKd}{NC}}{s^2 + \frac{KoKdR}{N}s + \frac{KoKd}{NC}}$$

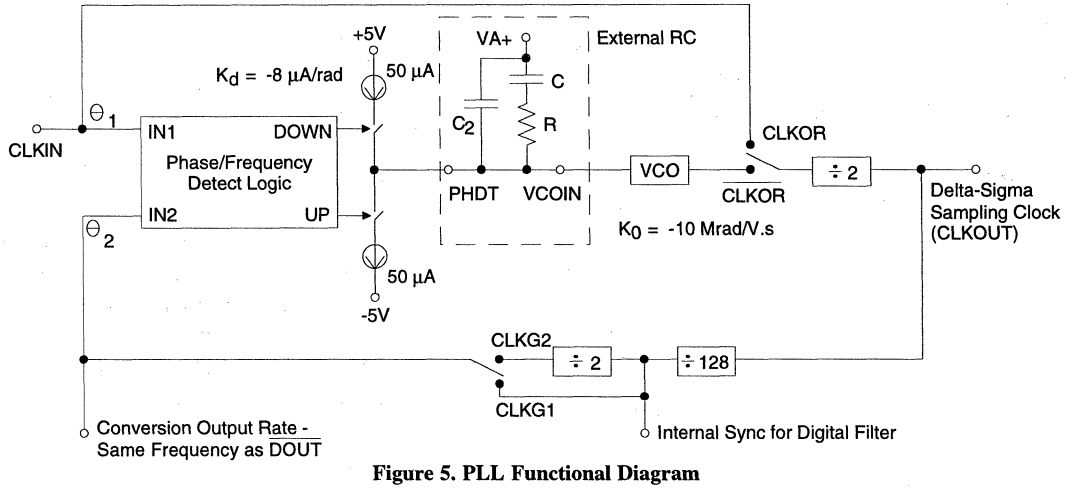


Figure 5. PLL Functional Diagram

This equation may be rewritten such that its elements correspond with the following characteristic form in which the damping factor, ζ, and the natural frequency, ω_n , are evident:

$$\frac{\theta_2}{\theta_1} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

Both the natural frequency and the damping factor are particularly important in determining the transient response of the phase-locked loop when subjected to a step input of phase or frequency. A family of curves are illustrated in Figure 6 that indicate the overshoot and stability of the loop as a function of the damping factor. Each response is plotted as a function of the normalized time, ω_n t. For a given ζ and lock time, t, the ω_n required can be determined. Alternatively, phase lock control loop bandwidth may be a specified parameter. In some systems it may be desirable to reduce the -3dB bandwidth of the PLL control loop to reduce the effects of jitter in the phase of the input clock. The 3 dB bandwidth of the PLL control loop is defined by the following equation:

$$\omega_{3dB} = \omega_n\sqrt{2\zeta^2 + 1 + \sqrt{(2\zeta^2 + 1)^2 + 1}}$$

The equations used to describe the PLL and the 3 dB bandwidth are valid only if the frequency of CLKIN is approximately 20 times greater than the 3 dB corner frequency of the control loop.

2

Filter Components

Using the equations which describe the transfer function of the PLL system, the following external filter component equations can be determined:

$$C = \frac{KoKd}{N\omega_n^2}$$

$$R = 2\zeta\omega_n \frac{N}{KoKd}$$

The gain factors (Ko, Kd) are specified in the Analog Characteristics table. In the event the system calls for very low bandwidth, hence a corresponding reduction in loop gain, the phase detector gain factor Kd can be reduced. A large series resistor (R1) can be inserted between the output of the detector and the filter. Then the 50 µA current sources will saturate to the supplies and yield the following gain factor:

$$Kd \approx \frac{-5V}{2\pi R_1}$$

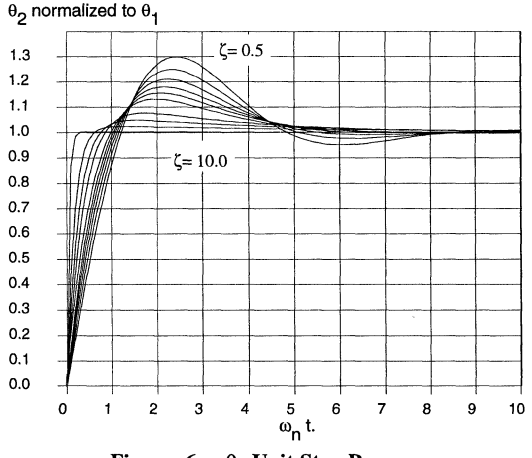


Figure 6a. θ_2 Unit Step Response

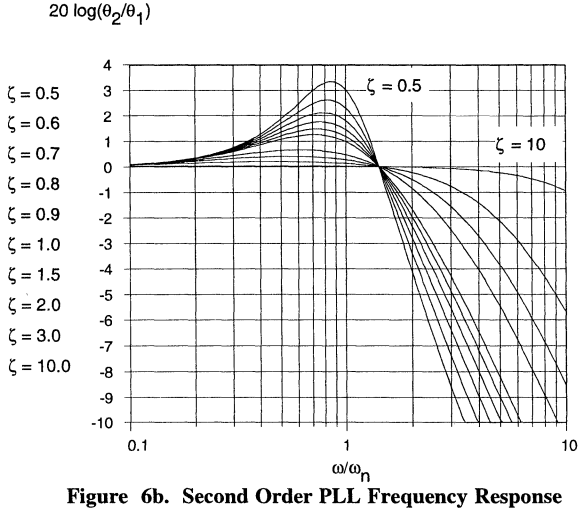


Figure 6b. Second Order PLL Frequency Response

In some applications additional filtering may be useful to eliminate any jitter associated with the discrete current pulses from the phase detector. In this case a capacitor whose value is no more than 0.1 C can be placed across the RC filter network (C_2 in Figure 5).

Filter Design Example

The following is a step by step example of how to derive the loop filter components. The CS5317 A/D sampling clock is to be derived from a 9600 Hz clock source. The application requires the signal passband of the CS5317 to be 4 kHz. The on-chip digital filter of the CS5317 has a 3 dB passband of CLKOUT/488.65 (see Note 4 in the data sheet specifications tables). The 4 kHz passband requirement dictates that the sample clock (CLKOUT) of the CS5317 be a minimum of 4000 X 488.65 = 1.954 MHz. This requires the VCO to run at 3.908 MHz. The 3.908 MHz rate is 407 times greater than the 9600 Hz PLL input clock. Therefore the CS5317 must be set up in mode CLKG2 with N = 512. If the CLKG1 mode were used (N = 256), too narrow of a signal bandwidth through the A/D would result.

Once the operating mode has been determined from the system requirements, a value for the damping factor must be chosen. Figure 6 illustrates the dynamic aspects of the system with a given damping factor. Damping factor is generally chosen to be between 0.5 and 2.0. The choice of 0.5 will result in an overshoot of 30 % to a step response whereas the choice of 2.0 will result in an overshoot of less than 5 %. For example purposes, let us use a damping factor of 1.0.

So, let us begin with the following variables :

Ko = - 10 Mradians/volt.sec
Kd = - 8 µA/radian
N = 512
$\zeta = 1.0$

To calculate values for the resistor R and capacitor C of the filter, we must first derive a value for ω_n. Using the general rule that the sample clock should be at least 20 times higher frequency than the 3dB bandwidth of the PLL control loop:

$$CLKIN \geq 20\ \omega_{3dB}$$

where CLKIN = 9600 Hz $= 2\pi\ 9600$ radians/sec.

So: $\omega_{3dB} = 2\pi\ 9600/20 = 3016$ radians/sec.

Knowing ω_{3dB} and the damping factor of 1.0, we can calculate the natural frequency, ω_n , of the control loop:

$$\omega_n = \omega_{3dB}\sqrt{2\zeta^2 + 1 + \sqrt{(2\zeta^2 + 1)^2 + 1}}$$

$$\omega_n = 3016\sqrt{2(1)^2 + 1 + \sqrt{(2(1)^2 + 1)^2 + 1}}$$

$$\omega_n = 1215 \quad 1/\text{sec}$$

Once the natural frequency, ω_n , is determined, values for R and C for the loop filter can be calculated:

$$R = 2\zeta\omega_n N/KoKd$$

$$R = 2(1)(1215\ 1/s)\ 512/(-10\text{Mrad/v.s.})(-8\ \mu\text{A/rad})$$

R = 15552 v/A = 15.55 kΩ. Use R = 15 kΩ.

$$C = KoKd/N\omega_n^2$$

$$C = (-10\ \text{Mrad/v.s})(-8\ \mu\text{A/rad})/512\ (1215\ 1/s)^2$$

$C = 105.8 \times 10^{-9}$ A.s/v = 105 nF. Use 0.1 µF.

The above example assumed typical values for Ko and Kd. Your application may require a worst case analysis which includes the minimum or maximum values. Table 2 shows some other example situations and R and C values.

CLKIN (Hz)	Mode	N	CLKOUT (MHz)	ζ	ω3dB	ωn	R * (kΩ)	C * (nF)
7200	CLKG2	512	1.8432	1.0	2262	911	11.6	187
9600	CLKG2	512	2.4576	1.0	3016	1215	15.5	106
14400	CLKG1	256	1.8432	1.0	4524	1822	11.6	94
19200	CLKG1	256	2.4576	1.0	6032	2430	15.5	52

* The values for R and C are as calculated using the described method. Component tolerances have not been allowed for. Notice that Ko and Kd can vary over a wide range, so using tight tolerances for R and C is not justified. Use the nearest conveniently available value.

Table 2 Example PLL Loop Filter R and C values

CS5317 PERFORMANCE

The CS5317 features 100% tested dynamic performance. The following section is included to illustrate the test method used for the CS5317.

FFT Tests and Windowing

The CS5317 is tested using Fast Fourier Transform (FFT) techniques to analyze the converter's dynamic performance. A pure sine wave is applied to the CS5317 and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the digital waveform and distributes its energy among 512 "frequency bins". Assuming an ideal sinewave, distribution of energy in bins outside of the fundamental and dc can only be due to quantization effects and errors in the CS5317.

If sampling is not synchronized to the input sinewave it is highly unlikely that the time record will contain an exact integer number of periods of the input signal. However, the FFT assumes that the signal is periodic, and will calculate the spectrum of a signal that appears to have large discontinuities, thereby yielding a severely distorted spectrum. To avoid this problem, the time record is multiplied by a window function prior to performing the FFT. The window function smoothly forces the endpoints of the time record to zero, removing the discontinuities. The effect of the "window" in the frequency domain is to convolute the spectrum of the window with that of the actual input.

The quality of the window used for harmonic analysis is typically judged by its highest side-lobe level. The Blackman-Harris window used to test the CS5317 has a maximum side-lobe level of -92 dB.

Figure 7 shows an FFT plot of a typical CS5317 with a 1 kHz sinewave input generated by an "ultra-pure" sine wave generator and the output multiplied by a Blackman-Harris window. Artifacts of windowing are discarded from the signal-to-noise calculation using the assumption that quantization noise is white. All FFT plots in this data sheet were derived by averaging the FFT results from ten time records. This filters the spectral variability that can arise from capturing finite time records, without disturbing the total energy outside the fundamental. All harmonics and the -92 dB side-lobes from the Blackman-Harris window are therefore clearly visible in the plots.

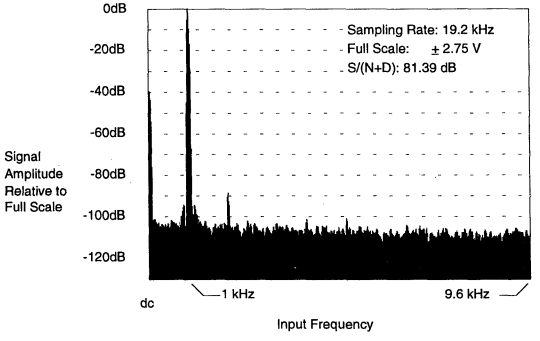


Figure 7. CS5317 Dynamic Performance

Full - scale signal - to - noise - plus - distortion [S/(N+D)] is calculated as the ratio of the rms power of the fundamental to the sum of the rms power of the FFT's other frequency bins, which include both noise and distortion. For the CS5317, signal-to-noise-plus-distortion is shown to be better than 81 dB for an input frequency range of 0 to 9.6 kHz (fs/2).

Harmonic distortion characteristics of the CS5317 are excellent at 80 dB full scale signal to THD (typical), as are intermodulation distortion characteristics, shown in Figure 8. Intermodulation distortion results from the modulation distortion of two or more input frequencies by a non-linear transfer function.

DNL Test

Figure 9 shows a plot of the typical differential non-linearity (DNL) of the CS5317. This test is done by taking a large number of conversion results, and counting the occurrences of each code. A perfect A/D converter would have all codes of equal size and therefore equal numbers of occurrences. In the DNL test, a code with the average number of occurrences is considered ideal and plotted as DNL = 0 LSB. A code with more or less occurrences than average will appear as a DNL of greater than or less than zero. A missing code has zero occurrences, and will appear as a DNL of -1 LSB.

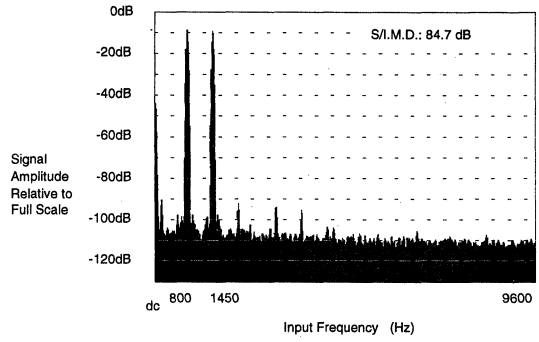


Figure 8. CS5317 Intermodulation Distortion

The plot below illustrates the typical DNL performance of the CS5317, and clearly shows the part easily achieves no missing codes.

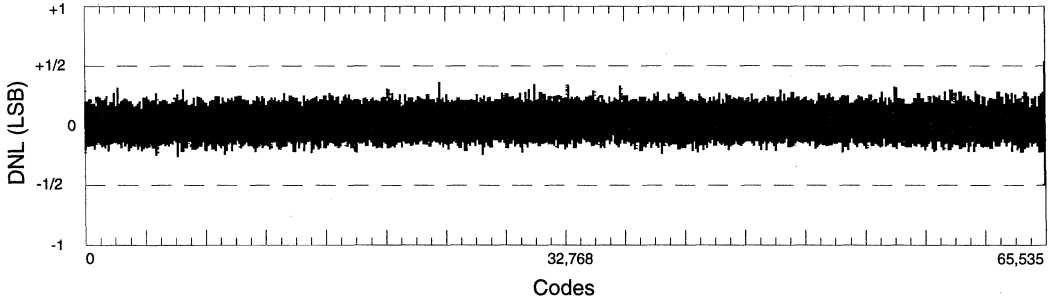
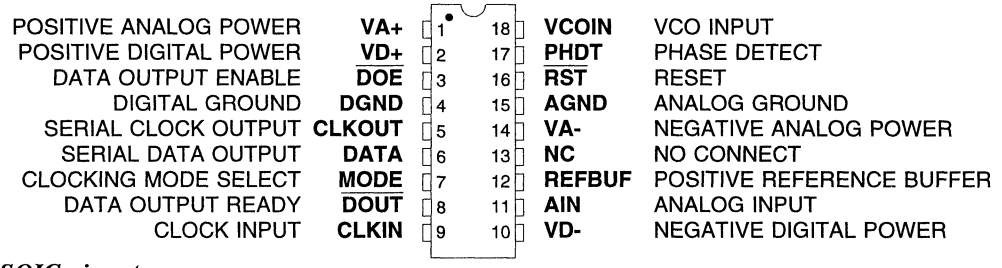


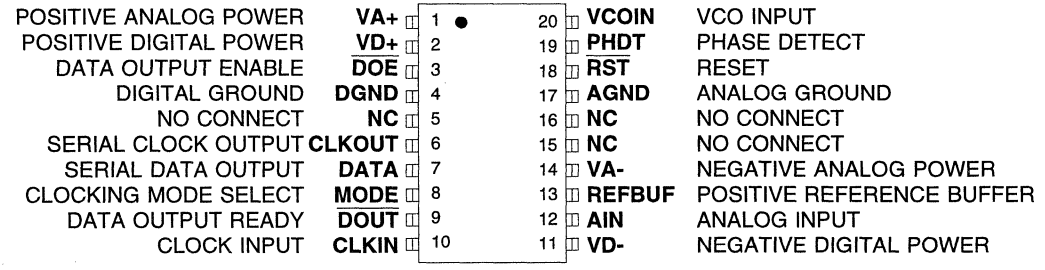
Figure 9. CS5317 DNL Plot

PIN DESCRIPTIONS (Pin numbers refer to the 18-pin DIP package)

18 pin DIP Pinout



20 pin SOIC pinout



Power Supplies

VD+ - Positive Digital Power, PIN 2.
Positive digital supply voltage. Nominally 5 volts.

VD- - Negative Digital Power, PIN 10.
Negative digital supply voltage. Nominally -5 volts.

DGND - Digital Ground, PIN 4.
Digital ground reference.

VA+ - Positive Analog Power, PIN 1.
Positive analog supply voltage. Nominally 5 volts.

VA- - Negative Analog Power, PIN 14.
Negative analog supply voltage. Nominally -5 volts.

AGND - Analog Ground, PIN 15.
Analog ground reference.

PLL/Clock Generator

CLKIN - Clock Input, PIN 9.
Clock input for both clock generation modes and the clock override mode (see MODE).

MODE - Mode Set, PIN 7.

Determines the internal clocking mode utilized by the CS5317. Connect to +5V to select CLKG1 mode. Connect to DGND to select CLKG2 mode. Connect to -5V to select CLKOR mode. This pin becomes equivalent to FSYNC in the CSZ5316 compatible mode.

VCOIN - VCO Input, PIN 18.

This pin is typically connected to PHDT. A capacitor and resistor in series connected between VA+ and this pin sets the filter response of the on-chip phase locked loop.

PHDT - Phase Detect, PIN 17.

This pin is typically connected to VCOIN. A capacitor and resistor in series connected between VA+ and this pin sets the filter response of the on-chip phase locked loop.

Inputs

AIN - Analog Input, PIN 11.

$\overline{\text{DOE}}$ - Data Output Enable, PIN 3.

Three-state control for serial output interface. When low, DATA, $\overline{\text{DOUT}}$, and CLKOUT are active. When high, they are in a high impedance state.

$\overline{\text{RST}}$ - Sample Clock Reset, PIN 16.

Sets phase of CLKOUT. Functions only in the clock override mode, CLKOR. Used to synchronize the output samples of multiple CS5317's. Must be kept high in CLKG1 or CLKG2 modes. Also, tying this pin low, with MODE not tied to - 5V, will place the CS5317 into CSZ5316 compatible mode.

Outputs

$\overline{\text{DOUT}}$ - Data Output Flag, PIN 8.

The falling edge indicates the start of serial data output on the DATA pin. The rising edge indicates the end of serial data output.

DATA - Data Output, PIN 6.

Serial data output pin. Converted data is clocked out on this pin by the rising edge of CLKOUT. Data is sent MSB first in two's complement format.

CLKOUT - Data Output Clock, PIN 5.

Serial data output clock. Data is clocked out on the rising edge of this pin. The falling edge should be used to latch data. Since CLKOUT is a free running clock, $\overline{\text{DOUT}}$ can be used to indicate valid data.

REFBUF - Positive Voltage Reference Noise Buffer, PIN 12.

Used to attenuate noise on the internal positive voltage reference. Must be connected to the analog ground through a 0.1µF ceramic capacitor.

PARAMETER DEFINITIONS

Resolution - The number of different output codes possible. Expressed as N, where 2^N is the number of available output codes.

Dynamic Range - The ratio of the largest allowable input signal to the noise floor.

Total Harmonic Distortion - The ratio of the rms sum of all harmonics to the rms value of the largest allowable input signal. Units in dB's.

Signal to Intermodulation Distortion - The ratio of the rms sum of two input signals to the rms sum of all discernible intermodulation and harmonic distortion products.

Linearity Error - The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in %FS.

Differential Nonlinearity - The deviation of a code's width from the ideal width. Units in LSB's.

Positive Full Scale Error - The deviation of the last code transition from the ideal, (VREF - 3/2 LSB). Units in mV.

Positive Full Scale Drift - The drift in effective, positive, full-scale input voltage with temperature.

Negative Full Scale Error - The deviation of the first code transition from the ideal, (-VREF + 1/2 LSB). Units in mV.

Negative Full Scale Drift - The drift in effective, negative, full-scale input voltage with temperature.

Bipolar Offset - The deviation of the mid-scale transition from the ideal. The ideal is defined as the middle transition lying on a straight line between actual positive full-scale and actual negative full-scale.

Bipolar Offset Drift - The drift in the bipolar offset error with temperature.

Absolute Group Delay - The delay through the filter section of the part.

Passband Frequency - The upper -3 dB frequency of the CS5317.

ORDERING GUIDE

Model Number	Temperature Range	Package
CS5317-KP	0 to 70°C	18 Pin Plastic DIP
CS5317-KS	0 to 70°C	20 Pin Plastic SOIC

APPENDIX A
APPLICATIONS

Figure A1 shows one method of converting the serial output of the CS5317 into 16-bit, parallel words. The associated timing is also shown.

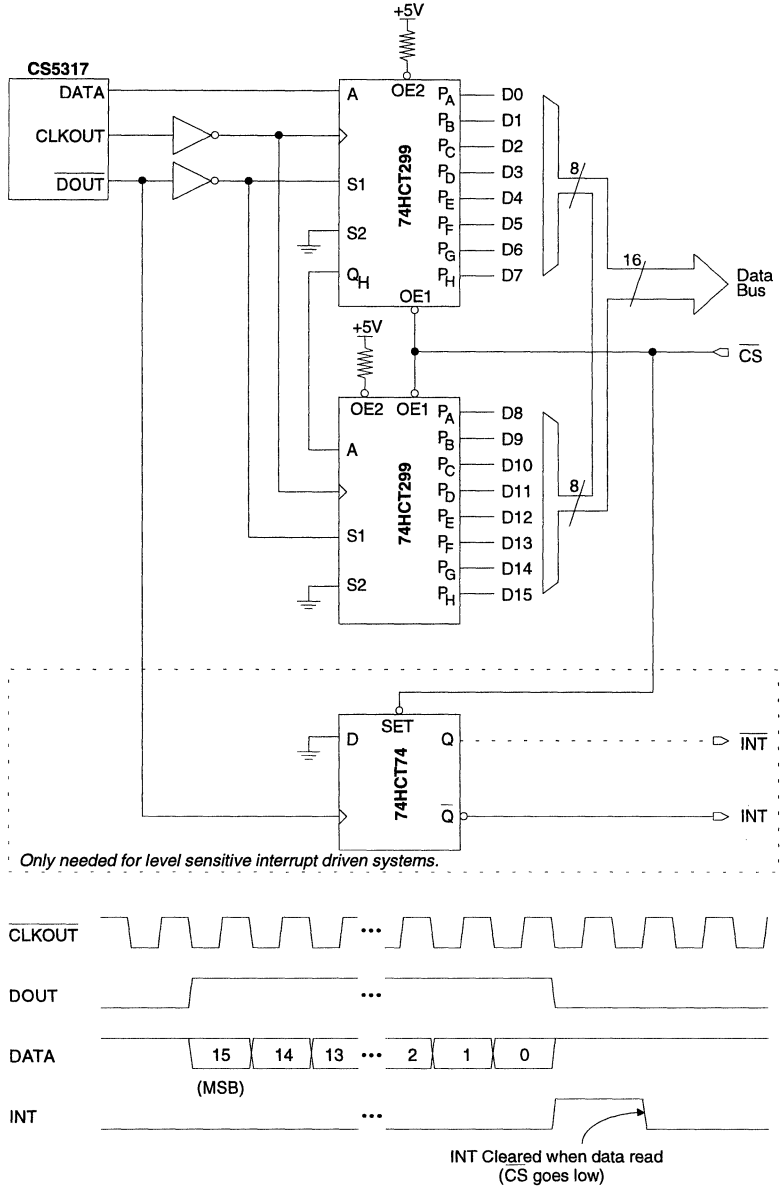


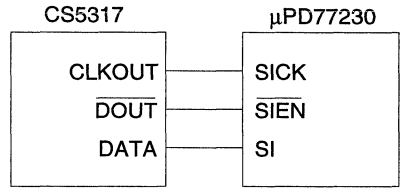
Figure A1. CS5317-to-Parallel Data Bus Interface

Figure A2 shows the interconnection and timing details for connecting a CS5317 to a NEC μPD7730 DSP chip.

Figure A3 shows the interconnection and timing details for connecting a CS5317 to a Motorola DSP 56000.

Status Register (SR)

Bit	Mnemonic	Setting	Meaning
9	SCI	0	External Clock
7, 6	SDLI	1, 0	16 bit data
3	SIF	0	MSB First



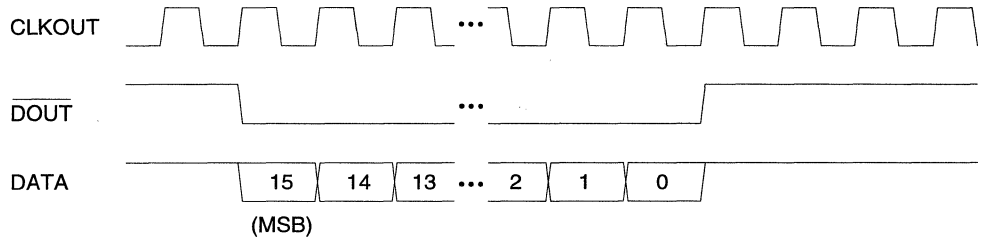
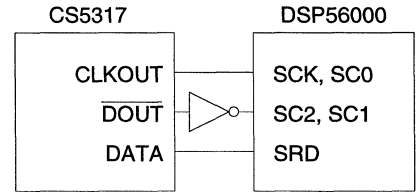


Figure A2. CS5317-to-NEC μPD77230 Serial Interface

SSI Control Reg. A CRA (X:FFEC)	
WL1 = 1, WL0 = 0	16 bits

	PINS	SYNC	ASYNC
SSI Control Reg. B CRB (X:FFED)	CLKOUT	SCK	SC0
	DOUT	SC2	SC1
	GCK	0	0
	SYN	1	0
	FSL	0	0
	SCKD	0	-
	SCD2	0	-
	SCD1	-	0
	SCD0	-	0



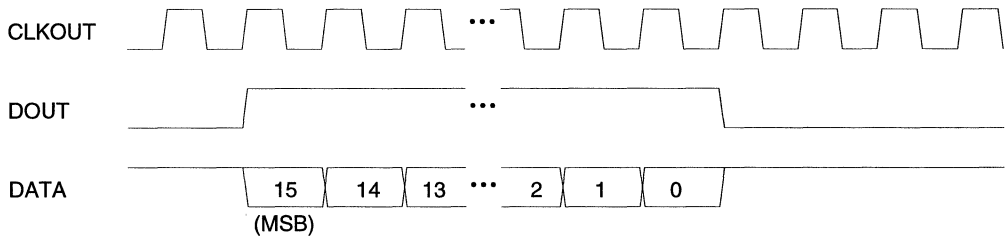


Figure A3. CS5317-to-Motorola DSP56000 Serial Interface

Figure A4 shows the interconnection and timing details for connecting a CS5317 to a WE DSP16 DSP chip.

Figure A5 shows the interconnection and timing details for connecting a CS5317 with TMS32020 and TMS320C25 DSP chips.

Serial I/O Control Register (SIOC)

Field	Value	Meaning
MSB	1	MSB input first
ILD	0	ILD is an input
ICK	0	ICK is an input
ILEN	0	16 bit input data

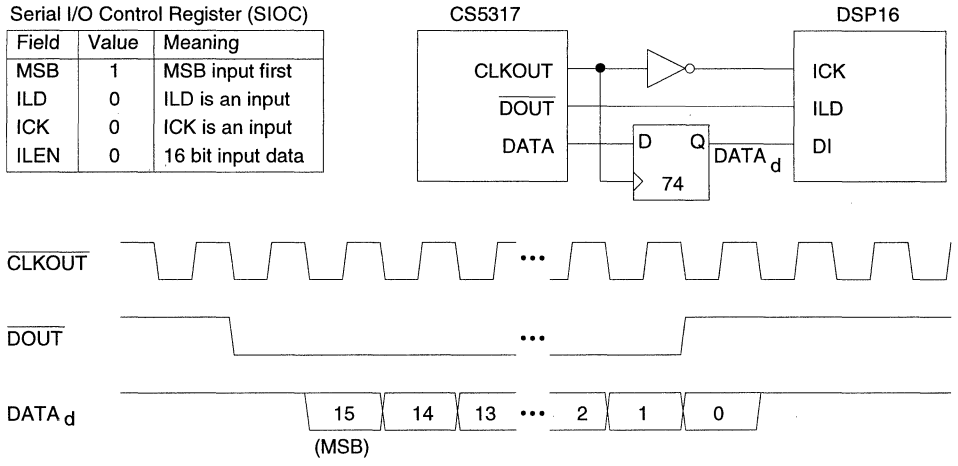


Figure A4. CS5317-to-WE DSP16 Serial Interface

TMS32020 Status Register (ST1):
F0 = 0 (16 bit data)
TMS320C25 Status Register (ST1):
F0 = 0 (16 bit data)
FSM = 1 (Frame Sync used)

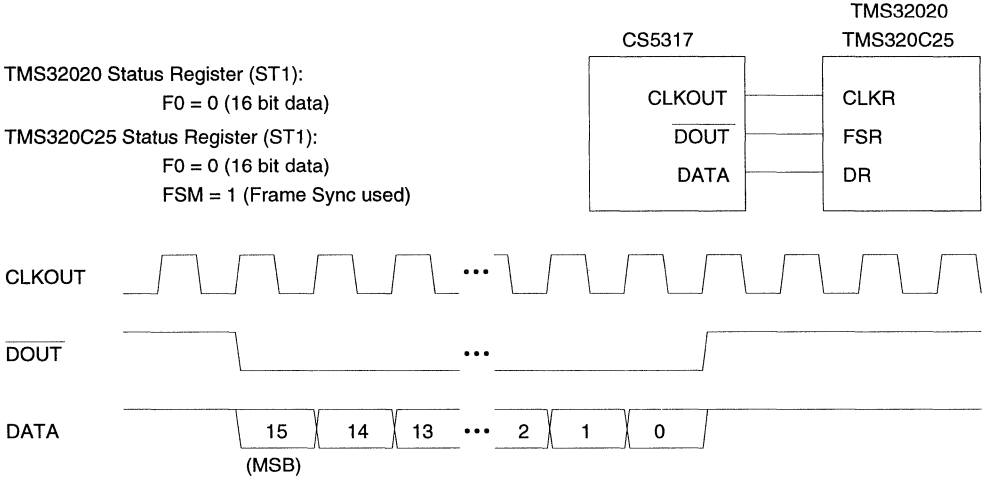


Figure A5. CS5317-to-TMS32020/TMS320C25 Serial Interface

Semiconductor Corporation

CDB5317

CDB5317 Evaluation Board

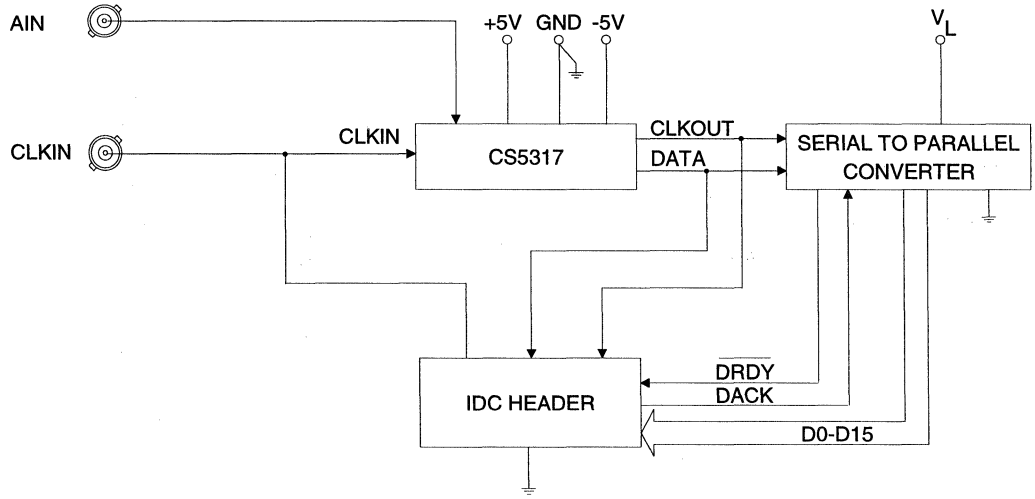
Features

- Easy to Use Digital Interface
  Parallel 16 Bits With Clock
  Serial Output With Clock
- Multiple Operating Modes
  Including Two PLL Modes
- IDC Header used to access Parallel Data, Serial Data, and Clock Input and Output

General Description

The CDB5317 Evaluation Board is designed to allow the user to quickly evaluate performance of the CS5317 Delta-Sigma Analog-to-Digital Converter. All that is required to use this board is an external power supply, a signal source, a clock source, and an ability to read either serial or parallel 16 bit data words.

ORDERING INFORMATION: CDB5317



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

GENERAL DESCRIPTION

The CDB5317 Evaluation Board is a stand-alone environment for easy lab evaluation of the CS5317 Delta-Sigma Analog-to-Digital Converter. Included on the board is a serial-to-parallel converter. The user can access output data in either parallel or serial form. When supplied with the necessary +5 V and -5 V power supplies, a CLKIN signal, and an analog signal source, the CDB5317 will provide converted data at the 40 pin header.

SUGGESTED EVALUATION METHOD

An efficient evaluation of the CS5317 using the CDB5317 may be accomplished as described below.

The following equipment will be required for the evaluation:

- The CDB5317 Evaluation Board.
- A power supply capable of supplying +5V and -5V.
- A clock source as the CLKIN signal of the CS5317.
- A spectrally pure sine wave generator such as the Krohn-Hite Model 4400A "Ultra-Low Distortion Oscillator".
- A PC equipped with a digital data acquisition board such as the Metrabyte Model PIO12 "24 Bit Parallel Digital I/O Interface".
- A software routine to collect the data and perform a Fast Fourier Transform (FFT).

The evaluation board includes filter components for the on-chip phase locked loop. The components are adequate for testing if the CLKIN signal has little or no phase-jitter. If the CDB5317 board is being tested as part of a system which generates a CLKIN which contains jitter, the PLL filter components may need to be optimized for your system (see the CS5317 data sheet).

Set-up for evaluation is straightforward. First decide the operating mode and place the jumper on the board for the proper selection. Then decide whether the filter components for the phase locked loop are adequate or whether they should be changed for your evaluation. The PLL will lock on a steady clock input with the filter as it is. Connect the necessary 5 V (CMOS compatible) CLKIN signal for the application. Use the sine-wave generator to supply the analog signal to the CDB5317. Apply the analog input and CLKIN signals only when the evaluation board is powered up. Converted data will then appear at the header on the CDB5317. The header should be connected to the digital data acquisition board in the PC through an IDC 40 pin connector and cable. The software routine should collect the data from the CDB5317 and run a standard 1024 point Fast Fourier Transform (FFT). Such an analysis results in a plot similar to Figure 1. This plot resulted from using a 1kHz input signal and a Blackman-Harris window for the FFT.

The signal to noise and signal to total harmonic distortion characteristics of the CS5317 may be easily measured in this way. The signal to total harmonic distortion value for a particular input is the ratio of the RMS value of the input signal and the sum of the RMS values of the harmonics shown in the diagram. The dynamic range of the CS5317 can be measured by reducing the input

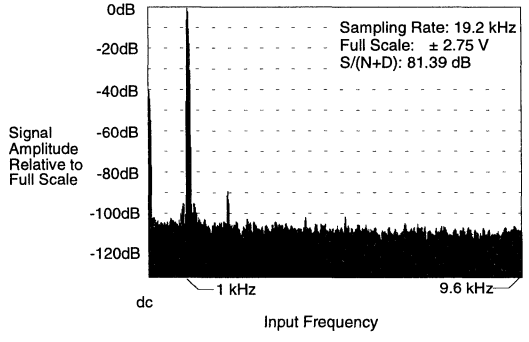


Figure 1. FFT Plot Example

amplitude so that distortion products become negligible. This allows an accurate measurement of the noise floor.

More complex analysis such as intermodulation distortion measurements can be accomplished with the addition of another sine-wave generator.

CIRCUIT DESCRIPTION

Figure 2 illustrates the CS5317 A/D converter IC circuit connections. The chip operates off of ±5V. These voltages are supplied from a power source external to the evaluation board. Binding posts are supplied on the board to connect the +5, -5, and ground power lines. A good quality low ripple, low noise supply will give the best performance. The +5 V supply can also be used for VL and should be connected between the VL board jack and the power supply, as opposed to connecting the VL jack straight to the +5V jack. The +5V jack is the positive power source for the CS5317 IC whereas the VL jack supplies power to all the digital ICs. Care should be taken that noise is not coupled between VL and +5V; however, supply noise is generally not a problem with the CS5317 since the on-chip decimation filter will remove any interference outside of its passband. The +5 and -5 V supply lines are filtered on

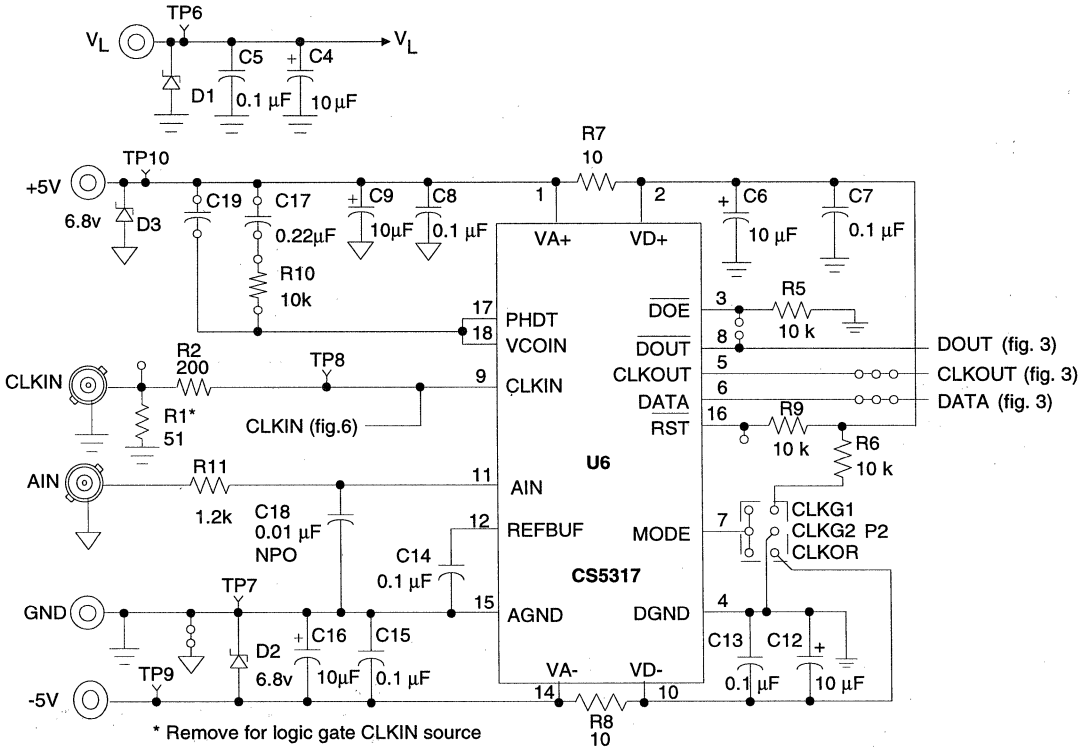


Figure 2. Analog-to-Digital Converter

the board and then connected to the V_A+ and V_A- supply pins of the chip. The +5 V and -5V are then connected by means of ten Ω resistors to the V_D+ and V_D- pins respectively. Capacitive filtering is provided on all supply pins of the chip. In addition there is a 0.1 µF filter capacitor connected from the REFBUF pin of the chip to the V_A- supply pin.

To properly operate, the CS5317 chip requires an external (5 V CMOS compatible) clock. A BNC connector labeled CLKIN is provided to connect the off-board clock signal to the board. The CLKIN signal is also available on the 40 pin header connector. The CLKIN signal is one input to the phase detector of the on-chip phase locked loop of the CS5317.

Header connector P2 (see Figure 2) is provided to allow mode selection for the CS5317 chip. The mode selection works together with the CLKIN signal to set the sample rate and the output word rate of the CS5317. See the CS5317 data sheet for details on mode selection. Two of the available modes (CLKG1 and CLKG2) utilize the on-chip phase locked loop to step up the CLKIN frequency to obtain the necessary sample rate clock for the A/D converter. Another mode (the CLKOR mode) does not use the on-chip PLL but instead drives the sample function directly. The

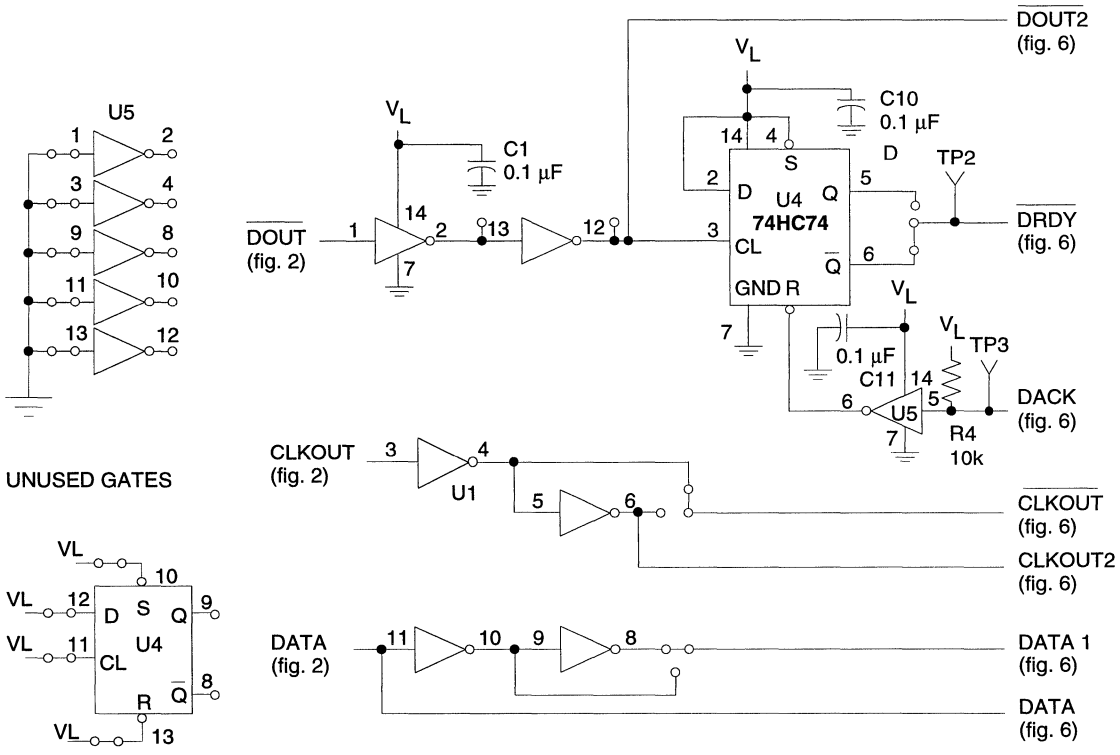
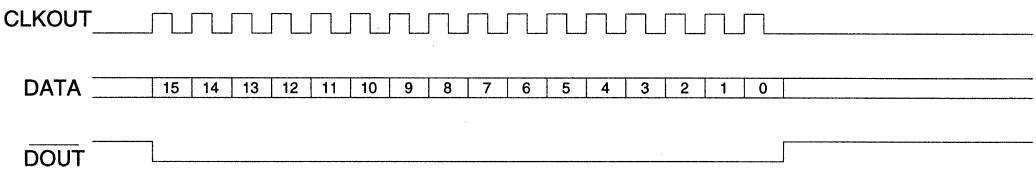


Figure 3. Buffers and Parallel Handshake Flip-Flop



Note: For a complete description of serial timing see the CS5317 Data Sheet

Figure 4 Serial Data Timing

two modes which use the phase locked loop will require appropriate low pass filter components on the Evaluation Board. The low pass filter components help determine the PLL control loop response, including its bandwidth and stability and therefore directly affect the transient response of the PLL control loop. Appropriate filter components should be installed if a particular dynamic response to changes of the CLKIN signal is desired.

The filter components which are installed on the board have been chosen for the following parameters: MODE: CLKG2; CLKIN: 7,200; N=512; damping factor: 1.0; Control loop -3 dB bandwidth: 2262 radians/second. These parameters yield R as 10 k Ω and C as 0.22 µF for the filter components.

The analog signal to be digitized is input to the AIN BNC connector. The digital output words from the CS5317 are buffered by HEX inverters as shown in Figure 3. The buffered versions of the CLKOUT and DATA signals are available on the header connector P1 in Figure 6. The serial data signals out of the CS5317 are illustrated in Figure 4. If remote control of the $\overline{\text{DOE}}$ line is desired, the trace on the PC Board can be opened and a wire connection can be soldered to the $\overline{\text{DOE}}$ input line. Remote control of the $\overline{\text{RST}}$ line of the CS5317 is also available if desired.

Figures 5 and 6 illustrate the serial to parallel shift registers including timing information. The DATA output signal from the CS5317 is input to the data input of the shift register. An inverted version of the CLKOUT signal is used to clock the DATA into the shift registers. The two 8-bit shift register ICs also include output latches. The rising edge

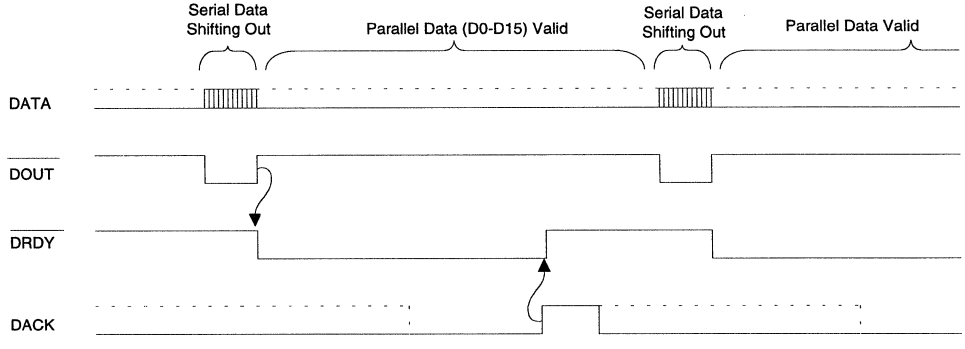


Figure 5. Parallel Data Timing

of the $\overline{\text{DOUT}}$ signal from the CS5317 is used to latch the data once it is input to the shift registers. The rising edge of $\overline{\text{DOUT}}$ is also used to toggle the $\overline{\text{DRDY}}$ flip flop (see Figure 3). The flip flop is used to signal a remote device whenever new data is latched into the output registers. The $\overline{\text{DRDY}}$ flip flop is reset whenever DACK occurs.

A component layout of the CDB5317 board is illustrated in Figure 7.

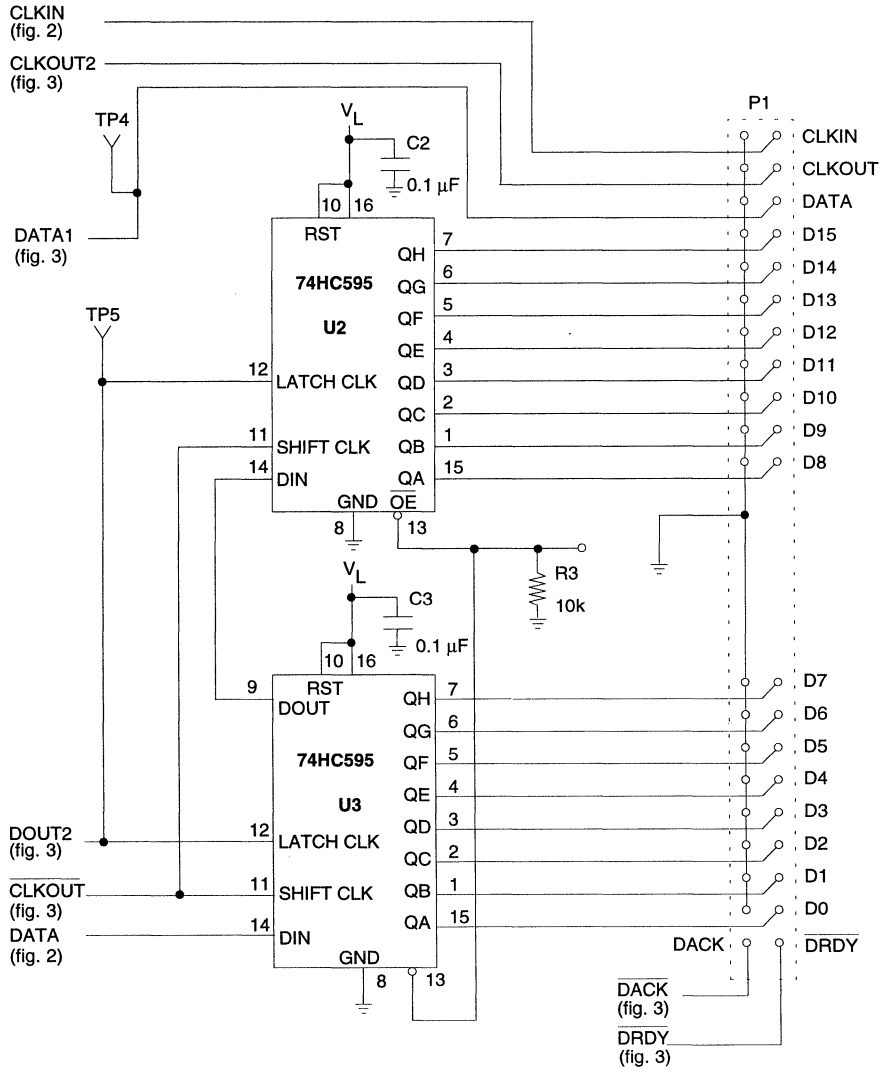


Figure 6.

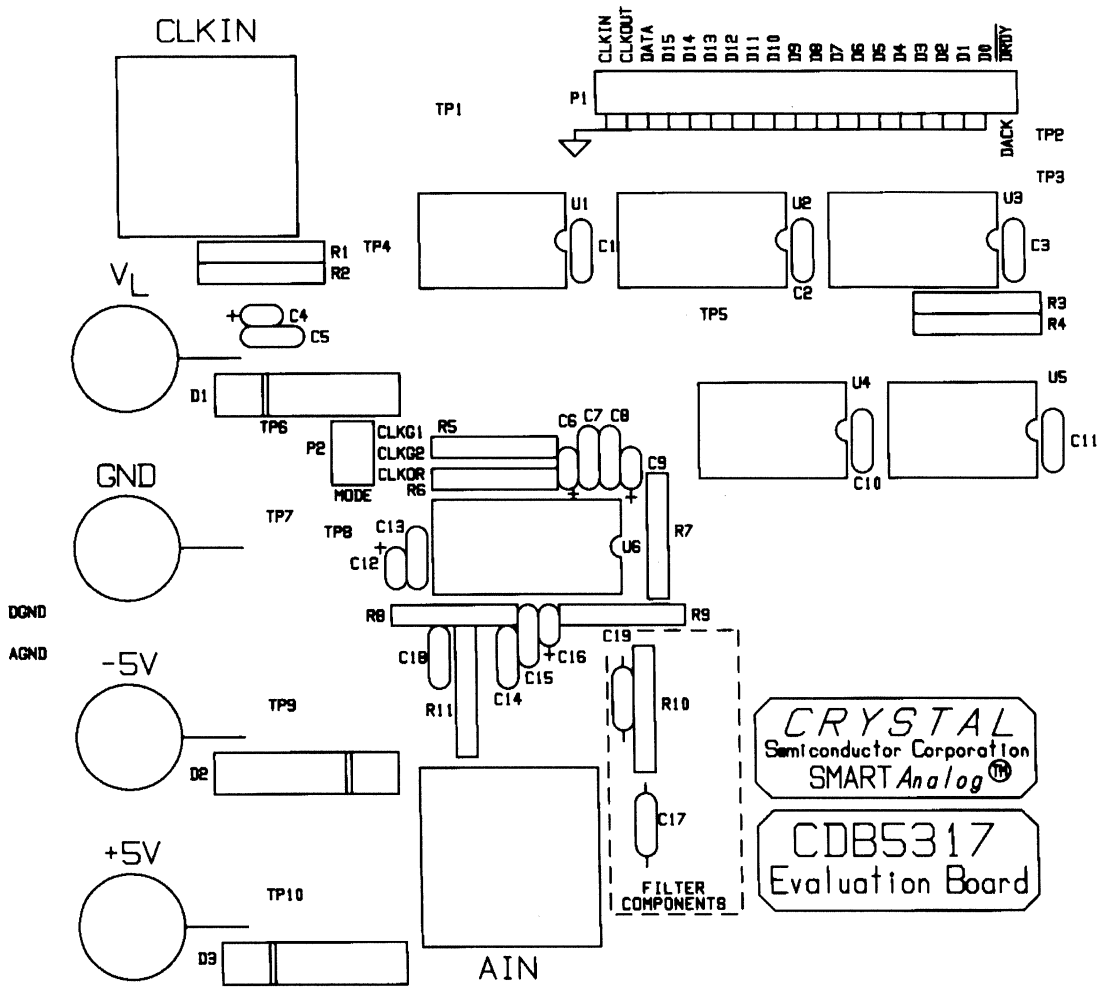


Figure 7. Bird's Eye View

Semiconductor Corporation

CS5321

High Dynamic Range Delta-Sigma Modulator

2

Features

- Delta-Sigma Architecture
  - Fourth-Order Modulator
  - Variable Sample Rate
  - Internal Track-and-Hold Amplifier
- Clock Jitter Tolerant Architecture
- Dynamic Range
  - 121 dB @ 411 Hz Bandwidth
  - 118 dB @ 822 Hz Bandwidth
- Signal-to-Distortion: 115 dB
- Input Range: ± 4.5V
- Improved offset drift, gain drift, and clock jitter immunity over CS5323

Description

The CS5321 is a high dynamic range, fourth-order delta-sigma modulator intended for geophysical and sonar applications. Used in combination with the CS5322 digital FIR filter, a unique high resolution A/D system results.

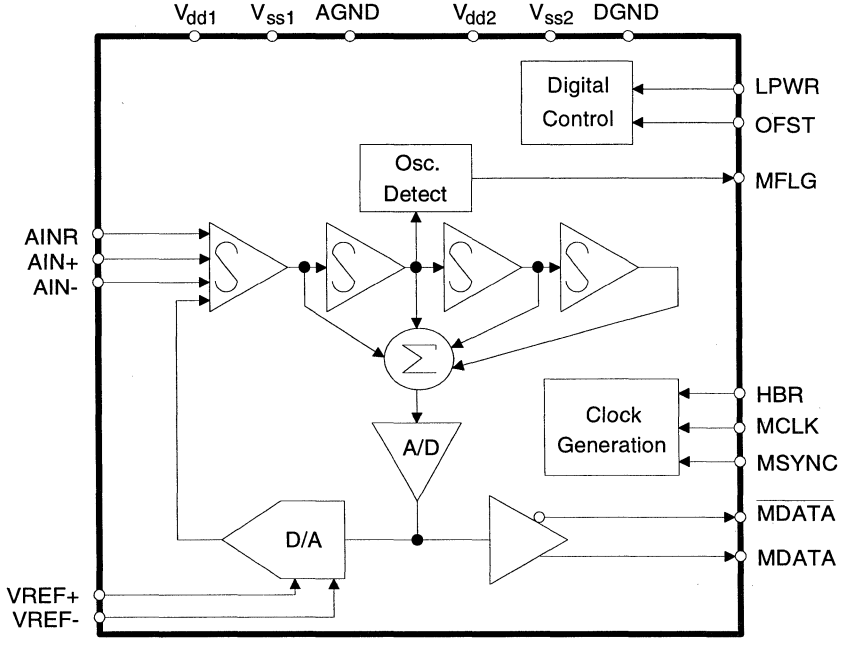
The CS5321 provides an oversampled serial bit stream at 256 kbits per second (HBR=1) and 128 kbits per second (HBR=0) operating with a clock rate of 1.024 MHz.

The monolithic CMOS design of the CS5321 insures high reliability while minimizing power dissipation.

The CS5321 can be operated in two power modes. In Normal mode (LPWR=0) power dissipation is 55 mW. In Low Power mode (LPWR=1) power dissipation is 30 mW.

ORDERING INFORMATION:

CS5321-BL	-55°C to +85°C	28-pin PLCC



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

ANALOG CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; V_{ss1}, V_{ss2} = -5V; V_{dd1}, V_{dd2} = 5V; GND=0V; MCLK=1.024 MHz; HBR=V_{dd}; LPWR=0; Device is connected as shown in Figure 3, the System Connection Diagram; unless otherwise specified. (Note 1))

Parameter*		Symbol	Min	Typ	Max	Units
Specified Temperature Range			-55	-	+85	°C
Dynamic Performance						
Dynamic Range	(Note 1)	DR				
HBR = 1:	fo = 4000 Hz		-	103	-	dB
OFST =1	fo = 2000 Hz		-	118	-	dB
	fo = 1000 Hz		116	121	-	dB
	fo = 500 Hz		-	124	-	dB
	fo = 250 Hz		-	127	-	dB
	fo = 125 Hz		-	129	-	dB
	fo = 62.5 Hz		-	130	-	dB
HBR = 0:	fo = 2000 Hz		-	99	-	dB
OFST = 1	fo = 1000 Hz		-	118	-	dB
	fo = 500 Hz		-	121	-	dB
	fo = 250 Hz		-	124	-	dB
	fo = 125 Hz		-	127	-	dB
	fo = 62.5 Hz		-	129	-	dB
	fo = 31.25 Hz		-	130	-	dB
Signal-to-Distortion:	MCLK = 1.024 MHz (Note 2)	SDR				
	HBR = 1		100	115	-	dB
	HBR = 0		110	120	-	dB
Intermodulation Distortion	(Note 3)	IMD	-	110	-	dB
dc Accuracy						
Full Scale Error	(Note 4)	FSE	-	1	-	%
Full Scale Drift	(Notes 4, 5)	TC_{FS}	-	5	-	ppm/°C
Offset	(Note 4)	V_{ZSE}	-	10	-	mV
Offset after Calibration	(Note 6)		-	±100	-	µV
Offset Calibration Range	(Note 7)		-	100	-	%F.S.
Offset Drift	(Note 4, 5)	TC_{ZSE}	-	60	-	µV/°C

Notes:
1. fo = CS5322 output word rate. Refer to the CS5322/CS5323 data sheet for details on the CS5322 FIR Filter.
2. Tested with full scale input signal of 50 Hz; f_{OWR} = 500 Hz; OFST = 0 or OFST = 1.
3. Tested with input signals of 30 Hz and 50 Hz, each 6 dB down from full scale f_{OWR} = 1000 Hz.
4. Specification is for the parameter over the specified temperature range and is for the CS5321 device only (VREF=+4.5V). It does not include the effects of external components, OFST = 0.
5. Drift specifications are guaranteed by design and/or characterization.
6. The offset after calibration specification applies to the effective offset voltage for a ± 4.5 volt input to the CS5321 modulator, but is relative to the output digital codes from the CS5322 after ORCAL and USEOR have been made active.
7. The CS5322 offset calibration is performed digitally and includes ± full scale (± 4.5 volts into CS5321). Calibration of offsets greater than ±5% of full scale will begin to subtract from the dynamic range.

* Refer to Parameter Definitions (immediately following pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter*		Symbol	Min	Typ	Max	Units
Specified Temperature Range			-55	-	+85	°C
Input Characteristics						
Input Signal Frequencies	(Note 8)	BW	dc	-	1500	Hz
Input Voltage Range	(Note 9)	V_{IN}	-4.5	-	+4.5	V
Input Overrange Voltage Tolerance	(Note 9)	I_{OVR}	-	-	5	%F.S.
Power Supplies						
DC Power Supply Currents	(Note 10)					
LPWR = 0	Positive Supplies		-	5.5	7.5	mA
	Negative Supplies		-	5.5	7.5	mA
LPWR = 1	Positive Supplies		-	3.0	4.5	mA
	Negative Supplies		-	3.0	4.5	mA
Power Consumption	(Note 10)					
Normal Operating Mode	(Note 11)	P_{DN}	-	55	75	mW
Lower Power Mode	(Note 12)	P_{DL}	-	30	45	mW
Power Down		P_D	-	2	-	mW
Power Supply Rejection	(dc to 128 kHz)(Notes 13, 14)	PSR	-	60	-	dB

Notes:
8. The upper bandwidth limit is determined by the CS5322 digital filter.
9. This input voltage range is for the configuration depicted in Figure 3, the System Connection Diagram, and applies to signal from dc to f3 Hz. Refer to CS5322 Filter Characteristics for the values of f3.
10. All outputs unloaded. All logic inputs forced to V_{dd} or GND respectively.
11. LPWR=0
12. The CS5321 power dissipation can be reduced under the following conditions:
    a) LPWR=1; MCLK=512kHz, HBR=1
    b) LPWR=1; MCLK=1.024MHz, HBR=0
13. Tested with a 100 mVp-p sine wave applied separately to each supply.
14. Refer to the CS5322/CS5323 Data Sheet for values of the Filter Characteristics of the CS5322.

* Refer to Parameter Definitions (immediately following pin descriptions at the end of this data sheet).

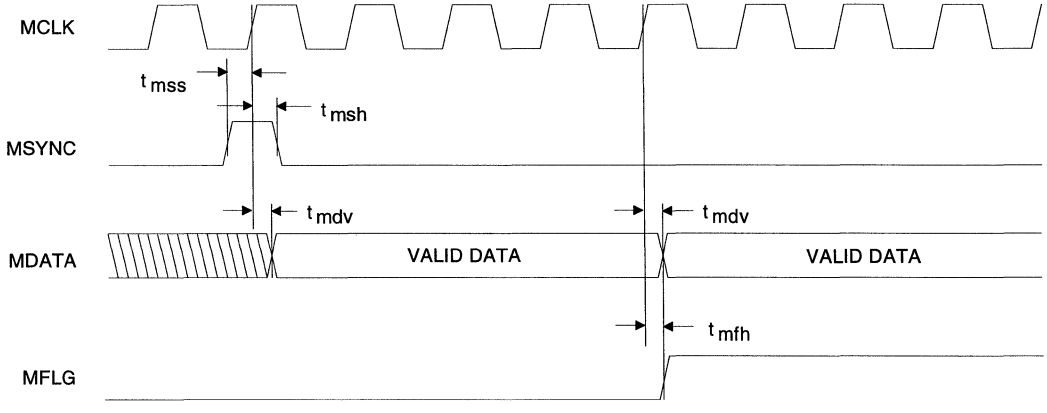
Specifications are subject to change without notice.

SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; V_{dd1}, V_{dd2} = 5V±5%; V_{ss1}, V_{ss2} = -5V±5%; Inputs: Logic 0 = 0V Logic 1 = V+; C_L = 50 pF (Note 15))

Parameter			Symbol	Min	Typ	Max	Units
MCLK Frequency		(Note 16)	f_c	0.250	1.024	1.2	MHz
MCLK Duty Cycle				40	-	60	%
MCLK Jitter (In-band)				-	-	300	ps
Rise Times:	Any Digital Input	(Note 17)	t_{risein}	-	-	100	ns
	Any Digital Output		$t_{riseout}$	-	50	200	ns
Fall Times:	Any Digital Input	(Note 17)	t_{fallin}	-	-	100	ns
	Any Digital Output		$t_{fallout}$	-	50	200	ns
MSYNC Setup Time to MCLK rising			t_{mss}	20	-	-	ns
MSYNC Hold Time after MCLK rising			t_{msh}	20	-	-	ns
MCLK rising to Valid MFLG			t_{mfh}	-	140	255	ns
MCLK rising to Valid MDATA			t_{mdv}	-	170	300	ns

Notes: 15. Guaranteed by design, characterization, or test.
16. If MCLK is removed, the CS5321 will enter a power down state.
17. Excludes MCLK input, MCLK should be driven with a signal having rise/fall times of 25ns or faster.

Rise and Fall Times



CS5321 Interface Timing, HBR=1

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; $V_{dd1} = V_{dd2} = 5V \pm 5\%$; GND = 0V; measurements performed under static conditions)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Drive Voltage	(Note 18)	V_{IH}	(V_{dd})-0.6	-	-	V
Low-Level Input Drive Voltage	(Note 18)	V_{IL}	-	-	1.0	V
High-Level Output Voltage I_{OUT} = -40 µA	(Note 19)	V_{OH}	(V_{dd})-0.3	-	-	V
Low-Level Output Voltage I_{OUT} = +40 µA	(Note 19)	V_{OL}	-	-	0.3	V
Input Leakage Current		I_{LKG}	-	-	±10	µA
Digital Input Capacitance		C_{IN}	-	9	-	pF
Digital Output Capacitance		C_{OUT}	-	9	-	pF

Notes: 18. Device is intended to be driven with CMOS logic levels.
19. Device is intended to be interfaced to CMOS logic. Resistive loads are not recommended on these pins.

RECOMMENDED OPERATING CONDITIONS (GND=0V, see Note 20)

Parameter		Symbol	Min	Typ	Max	Units
DC Supply:	Positive	V_{dd1}, V_{dd2}	4.75	5.0	5.25	V
	Negative	V_{ss1}, V_{ss2}	-4.75	-5.0	-5.25	V
Ambient Operating Temperature		T_A	-55	-	+85	°C

Notes: 20. All voltages with respect to ground.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Supply:	Positive	V_{dd1}, V_{dd2}	-0.3	6.0	V
	Negative	V_{ss1}, V_{ss2}	+0.3	-6.0	V
Input Current, Any Pin Except Supplies	(Note 21)	I_{in}	-	±10	mA
Output Current		I_{out}	-	25	mA
Total Power (all supplies and outputs)		P_t	-	1	W
Digital Input Voltage		V_{IND}	-0.3	(V_{dd})+0.3	V
Storage Temperature		T_{stg}	-65	150	°C

Notes: 21. Transient currents of up to 100 mA will not cause SCR latch up.

*WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

GENERAL DESCRIPTION

The CS5321 is a fourth-order CMOS monolithic analog modulator designed specifically for very high resolution measurement of signals between dc and 1500 Hz. Configuring the CS5321 with the CS5322 FIR filter results in a high resolution A/D converter system that performs sampling and A/D conversion with dynamic range exceeding 120 dB (Refer to the CS5322/CS5323 data sheet for specific details on the CS5322).

The CS5321 utilizes a fourth-order oversampling architecture to achieve high resolution A/D conversion. The modulator consists of a 1-bit A/D converter embedded in a negative feedback loop. The modulator provides an oversampled serial bit stream at 256 kbits per second (HBR=1) and 128 kbits per second (HBR=0) operating with a clock rate of 1.024 MHz.

The CS5321 offers improved performance, lower power consumption, and greater tolerance to clock jitter than the CS5323.

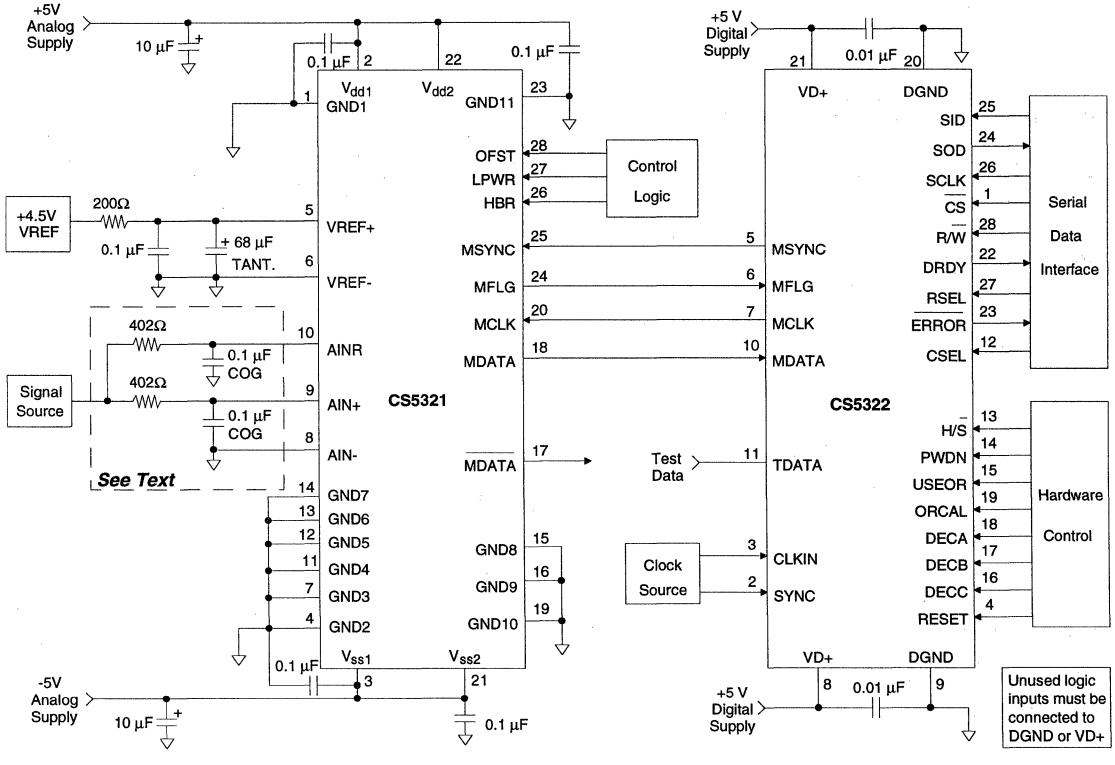


Figure 1. System Connection Diagram

Analog Input

The CS5321 A/D converter uses a switched capacitor architecture for its signal and voltage reference inputs. The signal input uses three pins; AINR, AIN+, and AIN-. The AIN- pin acts as the return pin for the AINR and AIN+ pins. The AINR pin is a switched capacitor "rough charge" input for the AIN+ pin. The input impedance for the rough charge pin (AINR) is 1/fC where f is the two times the modulator sampling clock rate and C is the internal sampling capacitor (about 40 pF). Using a 1.024 MHz master clock (HBR =1) yields an input impedance of about 1/(512 kHz)X(40pF) or about 50 kohms. Internal to the chip the rough charge input precharges the sampling capacitor used on the AIN+ input, therefore the effective input impedance on the AIN+ pin is orders of magnitude above the impedance seen on the AINR pin.

The analog input structure inside the VREF+ pin is very similar to the AINR pin but includes additional circuitry whose operating current can change over temperature and from device to device. Therefore, if gain accuracy is important, the VREF+ pin should be driven from a low source impedance. The current demand of the VREF+ pin will produce a voltage drop of approximately 45 mV across the 200 ohm source resistor of Figure 2-A with MCLK = 1.024 MHz, HBR = 1, and temperature = 25°C.

When the CS5321 modulator is operated with a 4.5 V reference it will accept a 9 V p-p input signal, but modulator loop stability can be adversely affected by high frequency out-of-band signals. Therefore, input signals must be bandlimited by an input filter. The -3 dB corner of the input filter must be equal to the modulator sampling clock divided by 64. The modulator sampling clock is MCLK/4 when HBR = 1 or MCLK/8 when HBR =0. With MCLK =1.024 MHz, HBR = 1, the modulator sampling clock is 256 kHz which requires an input filter with a -3 dB corner of 4 kHz. The bandlimiting may be accomplished in an amplifier stage ahead of the CS5321 modulator or with the RC input filter at the AIN+ and AINR input pins. The RC filter at the AIN+ and AINR pins is recommended to reduce the "charge kick" that the driving amplifier sees as the switched capacitor sampling is performed.

2

Figure 1 illustrates the CS5321/ CS5322 system connections. The input components on AINR and AIN+ should be identical values for optimum performance. In choosing the components the capacitor should be a minimum of 0.1 uF (C0G dielectric ceramic preferred). For minimum board space, the RC components on the AINR input can be removed, but this will force the driving amplifier to source the full dynamic charging current of the AINR input. This can increase distortion in the driving amplifier and reduce system performance. In choosing the RC filter components, increasing C and minimizing R is preferred. Increasing C reduces the instantaneous voltage change on the pin, but may require paralleling capacitors to maintain smaller size (the recommended 0.1 µF C0G ceramic capacitor is larger than other similar-valued capacitors with different dielectrics). Larger resistor values will increase the voltage drop across the resistor as the recharging current charges the switched capacitor input.

The OFST Pin

The CS5321 modulator can produce "idle tones" which occur in the passband when the input signal is steady state dc signal within about ±50 mV of bipolar zero. In the CS5321 these tones are about 135 dB down from full scale. The user can force these idle tones "out-of-band" by adding 100 mV of dc offset to the signal at the AIN input. Alternately, if the user circuitry has a low offset voltage such that the input signal is within ±50mV of bipolar zero when no AC signal is present, the OFST pin on the CS5321 can be activated. When OFST = 1, +100 mV of input

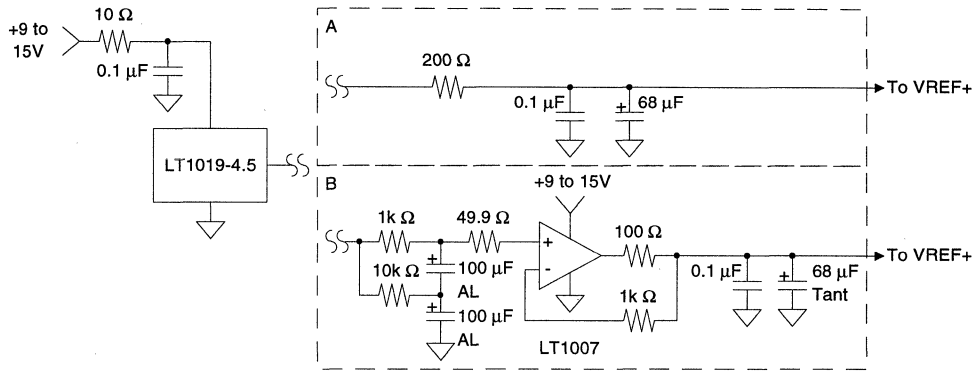


Figure 2. 4.5 Volt Reference with two filter options (see text)

referred offset will be added internal to the CS5321 and guarantee that any idle tones present will lie out-of-band. The user should be certain that when OFST is active (OFST =1) that the offset voltage generated by the user circuitry does not negate the offset added by the OFST pin.

Input Range and Overrange Conditions

The analog input is applied to the AIN+ and AINR pins with the AIN- pin connected to GND. The input is fully differential but for proper operation the AIN- pin must remain at GND potential.

The analog input span is defined by the voltage applied between the VREF+ and VREF- input pins. See the Voltage Reference section of this data sheet for voltage reference requirements.

The modulator is a fourth order delta-sigma and is therefore conditionally stable. The modulator may go into an oscillatory condition if the analog input is overranged. Input signals which exceed either plus or minus full scale by more than 5 % can introduce instability in the modulator. If an unstable condition is detected, the modulator will be reduced to a first order system until loop stability is achieved. If this occurs the MFLG pin will transition from a low to a high which will result in an error bit being set in the CS5322. The input signal must be reduced to within the full scale range of the converter for at least 32 MCLK cycles for the modulator to recover from this error condition.

Voltage Reference

The CS5321 is designed to operate with a voltage reference in the range of 4.0 to 4.5 volts. The voltage reference is applied to the VREF+ pin with the VREF- pin connected to the GND. A 4.5 V reference will result in the best S/N performance but most 4.5V references require a power supply voltage greater than 5.0 V for operation. A 4.0 V reference can be used for those applications which must operate from only 5.0 V supplies, but will yield a S/N slightly lower (1-2 dB) than when using a 4.5 V reference. The voltage reference should be designed to yield less than 2 µV rms of noise in band at the VREF+ pin of the CS5321. The CS5322 filter selection will determine the bandwidth over which the voltage reference noise will affect the CS5321/CS5322 dynamic range.

For a 4.5 V reference, the LT1019-4.5 voltage reference yields low enough noise if the output is filtered with a low pass RC filter as shown in Figure 2-A. The filter in Figure 2-A is acceptable for most spectral measurement applications, but a buffered version with lower source imped-

ance (Figure 2-B) may be preferred for dc-measurement applications.

Due to its dynamic (switched-capacitor) input the input impedance of the +VREF pin of the CS5321 will change any time MCLK or HBR is changed. Therefore the current required from the voltage reference will change any time MCLK or HBR is changed. This can affect gain accuracy due to the high source impedance of the filter resistor in Figure 2-A. If gain error is to be minimized, especially when MCLK or HBR is changed, the voltage reference should have lower output impedance. The buffer of Figure 2-B offers lower output impedance and will exhibit better system gain stability.

Clock Source

For proper operation, the CS5321 must be provided with a CMOS-compatible clock on the MCLK pin. The MCLK for the CS5321 is usually provided by the CS5322 filter. MCLK is usually 1.024 MHz to set the seven selectable output word rates from the CS5322. The MCLK frequency can be as low as 250 kHz and as high as 1.2 MHz. The choice of clock frequency can affect performance; see the Performance section of the data sheet. The clock must have less than 300 ps jitter to maintain data sheet performance from the device. The CS5321 is equipped with loss of clock detection circuitry which will cause the CS5321 to enter a powered-down state if the MCLK is removed or reduced to a very low frequency. The HBR pin on the CS5321 modifies the sampling clock rate of the modulator. When HBR=1, the modulator sampling clock will be at MCLK/4; with HBR =0 the modulator sampling clock will be at MCLK/8. The chip set will exhibit about 3 dB less S/N performance when the HBR pin is changed from a logic "1" to a logic "0" for the same output word rate from the CS5322.

Low Power Mode

The CS5321 includes a low power operating mode (LPWR =1). hen operated with LPWR = 1, the CS5321 modulator sampling clock must be restricted to rates of 128 kHz or less. Operating in low power mode with modulator sample rates greater than 128 kHz will greatly degrade performance.

Digital Interface and Data Format

The MCLK signal (normally 1.024 MHz) is divided by four, or by eight inside the CS5321 to generate the modulator oversampling clock. The HBR pin determines whether the clock divider inside the CS5321 divides by four (HBR =1) or by eight (HBR =0). The modulator outputs a ones density bit stream from its MDATA and $\overline{\text{MDATA}}$ pins proportional to the analog input signal, but at a bit rate determined by the modulator oversampling clock. For proper synchronization of the bitstream, the CS5321 must be furnished with an MSYNC signal prior to data conversion. The MSYNC signal, generated by the CS5322, resets the MCLK counter-divider in the CS5321 to the correct phase so that the bitstream can be properly sampled by the CS5322 digital filter.

When operated with the CS5322 digital filter the output codes from the CS5321/CS5322 will range from approximately decimal -5,242,880 to +5,242879 for an input to the CS5321 of ±4.5 V. Table 1 illustrates the output coding for various input signal amplitudes. Note that with a signal input defined as a full scale signal (4.5 V with VREF+ =4.5V) the CS5321/CS5322 chip does not output a full scale digital code of 8,388,607 but is scaled to a lower value to allow some overrange capability. Input signals can exceed the defined full scale by up to 5% and still be converted properly.

Modulator Input Signal	CS5322 Filter Output Code	
	HEX	Decimal
> (+VREF + 5%)	Error Flag Possible	
≈ (+VREF + 5%)	53FFFF(H)	+5505023
+VREF	4FFFFF(H)	+5242879
0V	000000(H)	0
-VREF	B00000(H)	-5242880
≈ - (+VREF + 5%)	AC0000(H)	-5505024
> - (+VREF + 5%)	Error Flag Possible	

Table 1. Output Coding for the CS5321 and CS5322 combination.

Performance

Figure 3, 4 and 5 illustrate the spectral performance of the CS5321/CS5322 when operating from a 1.024 MHz master clock. Ten 1024 point FFTs were averaged to produce the plots.

Figure 3 illustrates the chip set with a 100 Hz, -20 dB input signal. The sample rate was set at 1 kHz. Dynamic range is 122 dB.

The dynamic range calculated by the test software is reduced somewhat in Figures 4 and 5 because of jitter in the signal test oscillator. Jitter in the 100 Hz signal source is interpreted by the signal processing software to be increased noise.

The choice of master clock frequency will affect performance. The CS5321 will exhibit the best Signal/ Distortion performance with slower modulator sampling clock rates as slower sample rates allow more time for amplifier settling.

For lowest offset drift, the CS5321 should be operated with MCLK = 1.024 MHz and HBR =1. Slower modulator sampling clock rates will exhibit more offset drift. Changing MCLK to 512 kHz (HBR =1) or changing HBR to zero (MCLK =1.024 MHz) will cause the drift rate to double. Offset drift is not linear over temperature

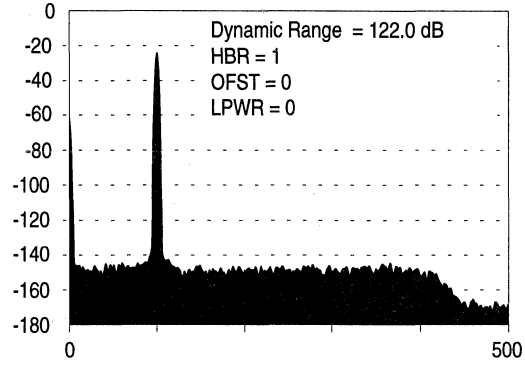


Figure 3. 1024 Point FFT Plot with -20 dB, 100 Hz Input, ten averages

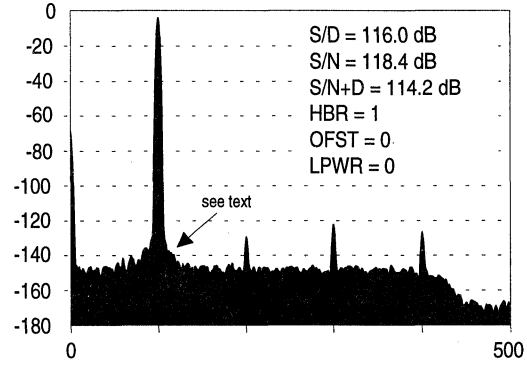


Figure 4. 1024 Point FFT Plot with Full Scale Input, 100 Hz, ten averages

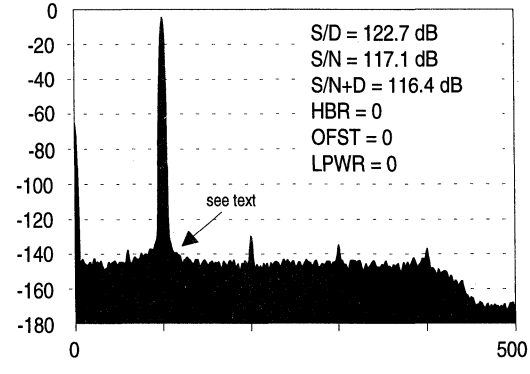


Figure 5. 1024 Point FFT Plot with Full Scale Input, 100 Hz, ten averages

so it is difficult to specify an exact drift rate. Offset drift characteristics vary from part to part and will vary as the power supply voltages vary. Therefore, if the CS5321 is to be used in precision dc measurement applications where offset drift is to be minimized, the power supplies should be well regulated. The CS5321 will exhibit about 6 ppm/°C of offset drift with MCLK = 1 and HBR =1.

Gain drift of the CS5321 itself is about 5 ppm/°C and is not affected by either modulator sample rate or by power supply variation.

Power Supply Considerations

The system connection diagram, Figure 1, illustrates the recommended power supply arrangements. There are two positive power supply pins for the CS5321 and two negative power supply pins. Power must be supplied to all four pins and each of the supply pins should be decoupled with a 0.1 uF capacitor to the nearest ground pin on the device.

When used with the CS5322 digital filter, the maximum voltage differential between the positive supplies of the CS5321 and the positive digital supply of the CS5322 must be less than 0.25 V. Operation beyond this constraint may result in loss of analog performance in the CS5321/ CS5322 system performance.

Many seismic or sonar systems are battery powered, and utilize dc-dc converters to generate the necessary supply voltages for the system. To minimize the effects of power supply interference, it is desirable to operate the dc-dc converter at a frequency which is rejected by the digital filter, or locked to the modulator sample clock rate.

A synchronous dc-dc converter, whose operating frequency is derived from the 1.024 MHz clock used to drive the CS5322, will minimize the potential for "beat frequencies" appearing in the passband between dc and the corner frequency of the digital filter.

Power Supply Rejection Ratio

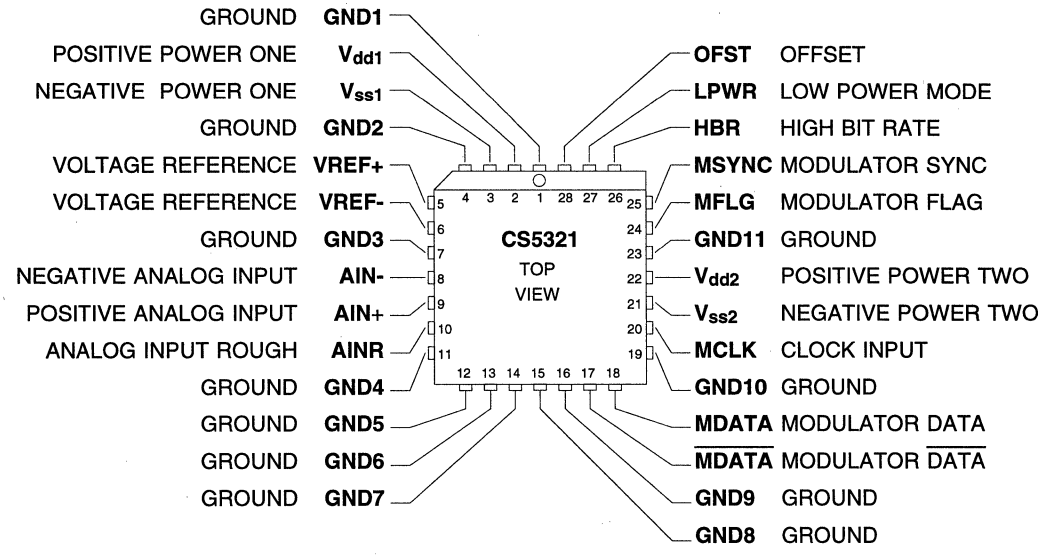
The PSRR of the CS5321 is frequency dependent. The CS5322 digital filter attenuation will aid in rejection of power supply noise for frequencies above the corner frequency setting of the CS5322. For frequencies between dc and the corner frequency of the digital filter, the PSRR is nearly constant at about 60 dB.

Board Layout Considerations

All of the 0.1 µF filter capacitors on the power supplies, AIN+, and AINR, should be placed very close to the chip and connect to the nearest ground pin on the device. The capacitors between VREF+ and VREF- should be located as close to the chip as possible.

The 0.1 µF capacitors on the AIN+ and AINR pins should be placed with their leads on the same axis, not side-by-side. If these capacitors are placed side-by-side their electric fields can interact and cause increased distortion.

The chip should be surrounded with a ground plane. Trace fill should be used around the analog input components. See the *Layout and Design Rules for Data Converters* application note in the Data Book.



CS5321 PIN DESCRIPTIONS

Power Supplies

V_{dd1} – Positive Power One, PIN 2
Positive supply voltage. Nominally +5 Volts.

V_{dd2} – Positive Power Two, PIN 22
Positive supply voltage. Nominally +5 Volts.

V_{ss1} – Negative Power One, PIN 3
Negative supply voltage. Nominally -5 Volts.

V_{ss2} – Negative Power Two, PIN 21
Negative supply voltage. Nominally -5 Volts.

GND1 through GND11 – Ground, PINS 1, 4, 7, 11, 12, 13, 14, 15, 16, 19, 23.
Ground reference.

Analog Inputs

AIN+ - Positive Analog Input, PIN 9
Nominally ± 4.5V

AIN- - Negative Analog Input, PIN 8
This pin is tied to ground.

AINR - Analog Input Rough, PIN 10

Allows a non-linear current to bypass the main external anti-aliasing filter which if allowed to happen, would cause harmonic distortion in the modulator. Please refer to the System Connection Diagram and the Analog Input and Voltage Reference section of the data sheet for recommended use of this pin.

VREF+ – Positive Voltage Reference Input, PIN 5

This pin accepts an external +4.5V voltage reference.

VREF- – Negative Voltage Reference Input, PIN 6

This pin is tied to ground.

Digital Inputs

MCLK – Clock Input, PIN 20

A CMOS-compatible clock input to this pin (nominally 1.024 MHz) provides the necessary clock for operation of the modulator, digital filter and data output portions of the A/D converter.

MSYNC – Modulator Sync, PIN 25

A transition from a low to high level on this input will re-initialize the CS5321. MSYNC resets a divider-counter to align the MDATA output bit stream from the CS5321 with the timing inside the CS5322.

OFST - Offset, PIN 28

When high, adds approximately 100mV of input referred offset to guarantee that any zero input limit cycles are out of band if present. When low, zero offset is added.

LPWR - Low Power Mode, PIN 27

The CS5321 power dissipation can be reduced from its nominal value of 60 mW to 30 mW under the following conditions:
LPWR=1; MCLK $\leq$ 512 kHz, HBR=1; or
LPWR=1; MCLK $\leq$ 1.024 MHz, HBR=0

HBR – High Bit Rate, Pin 26

Selects either $\frac{1}{4}$MCLK (HBR=1) or $\frac{1}{8}$MCLK (HBR=0) for the modulator sampling clock.

Digital Outputs

MDATA – Modulator Data Output, PIN 18

Data will be presented in a one-bit serial data stream at a bit rate of 256 kHz (HBR=1) or 128 kHz (HBR=0) with MCLK operating at 1.024MHz.

$\overline{\text{MDATA}}$ – Modulator $\overline{\text{Data}}$ Output, PIN 17

Inverse of the MDATA output.

MFLG – Modulator Flag, PIN 24

A transition from a low to high level signals that the CS5321 modulator is unstable due to an over-range on the analog input.

PARAMETER DEFINITIONS

Dynamic Range

The ratio of the full-scale (rms) signal to the broadband (rms) noise signal. Broadband noise is measured with the input grounded within the bandwidth of 1 Hz to $f_{OWR}/2$ Hz. Units in db.

Signal-to-Distortion

The ratio of the full-scale (rms) signal to the rms sum of all harmonics up to 1000 Hz. Units in dB.

Intermodulation Distortion

The ratio of the rms sum of the two test frequencies (30 and 50 Hz) which are each 6dB down from full-scale to the rms sum of all intermodulation components within the bandwidth of dc to 1000 Hz. Units in dB.

Full Scale Error

The ratio of the difference between the value of the voltage reference and analog input voltage to the full-scale span (two times the voltage reference value). The ratio is calculated after the effects of offset and the external bias components are removed and the analog input voltage is adjusted. Measurement of this parameter uses the circuit configuration illustrated in the System Connection Diagram. Units in %.

Full Scale Drift

The change in the Full Scale value with temperature. Units in ppm/°C

Offset

The difference between the analog ground and the analog voltage necessary to yield an output code from the CS5321/CS5322 of 000000(H). Measurement of this parameter uses the circuit configuration illustrated in the System Connection Diagram. Units in mV.

Offset Drift

The change in the Offset value with temperature. Measurement of this parameter uses the circuit configuration illustrated in the System Connection Diagram. Units in µV/°C

Semiconductor Corporation

CDB5321

Evaluation Board for CS5321 & CS5322

2

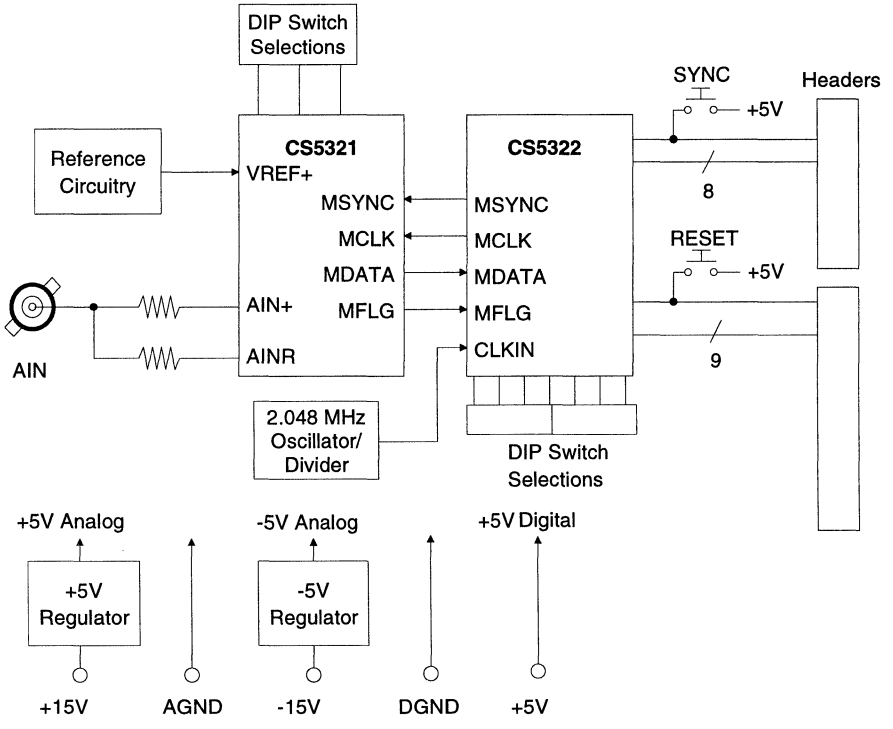
Features

- DIP switch control of all CS5322 logic pins
- Header control of all CS5322 logic pins
- Supports manual operation of RESET and SYNC

General Description

The CDB5321 is an evaluation board that allows laboratory characterization of the CS5321/CS5322 A/D converter chip-set. The chip-set supports seven different selectable word rates: 4 kHz, 2 kHz, 1 kHz, 500 Hz 250 Hz, 125 Hz and 62.5 Hz. Input to the board is 9 volts peak-to-peak. Output is via header connections to the CS5322 serial interface.

ORDERING INFORMATION: CDB5321



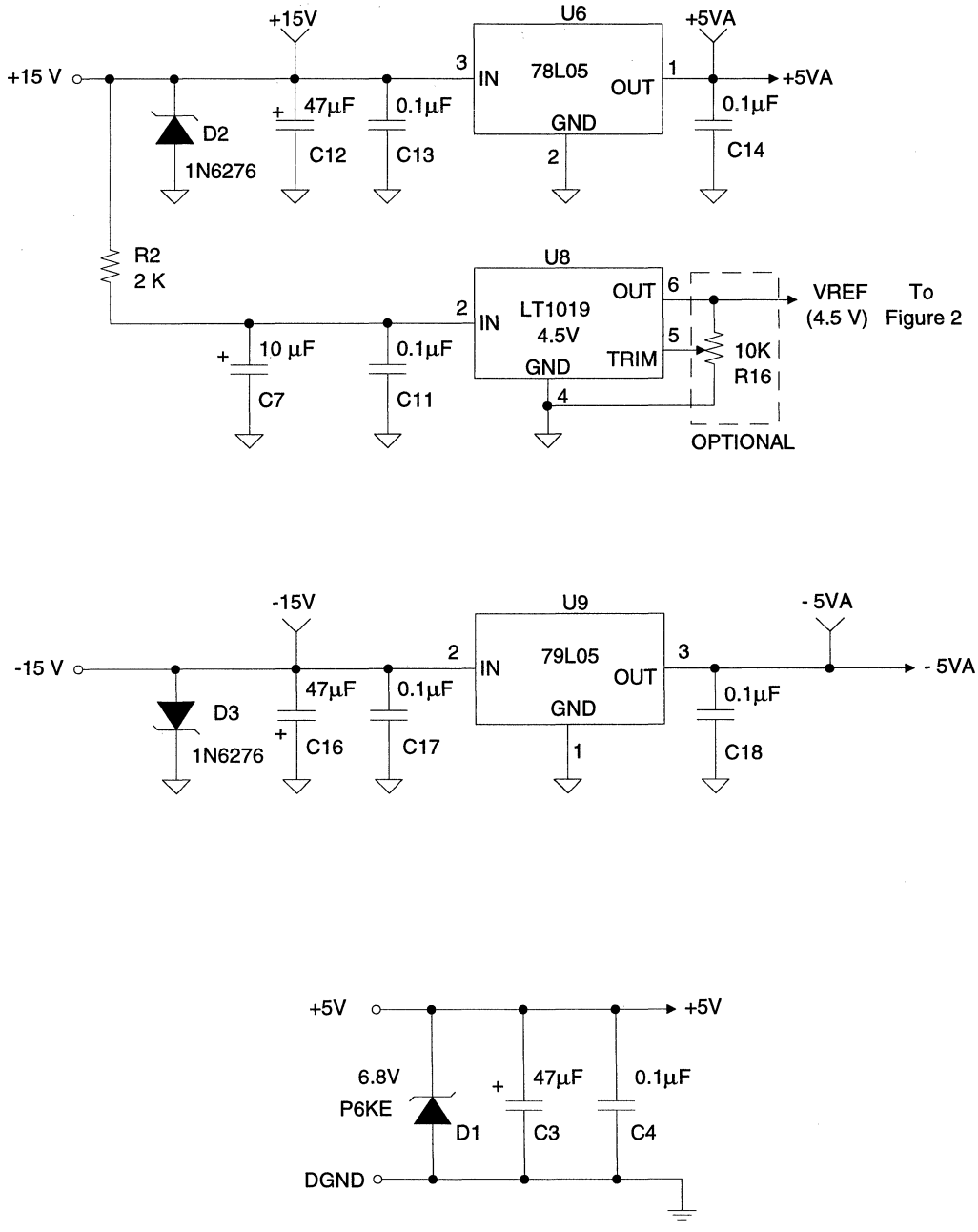


Figure 1. Power Supplies

OVERVIEW

The CDB5321 evaluation board requires three separate power supplies for proper operation. Figure 1 illustrates the power supply connections. The required power supply input voltages consist of +5V, +15V, and -15V. The CS5322 filter and logic support devices on the board operate from the +5V supply. The +15V and -15V inputs are regulated down to provide +5V and -5V supplies necessary for the CS5321 modulator. Figure 1 also illustrates the LT1019 4.5V reference used with the CS5321 modulator.

Figure 2 illustrates the CS5321 modulator circuitry, including the analog BNC input for the test signal source. Most often switch selections on S5 are set to HBR=1, LPWR=0, and

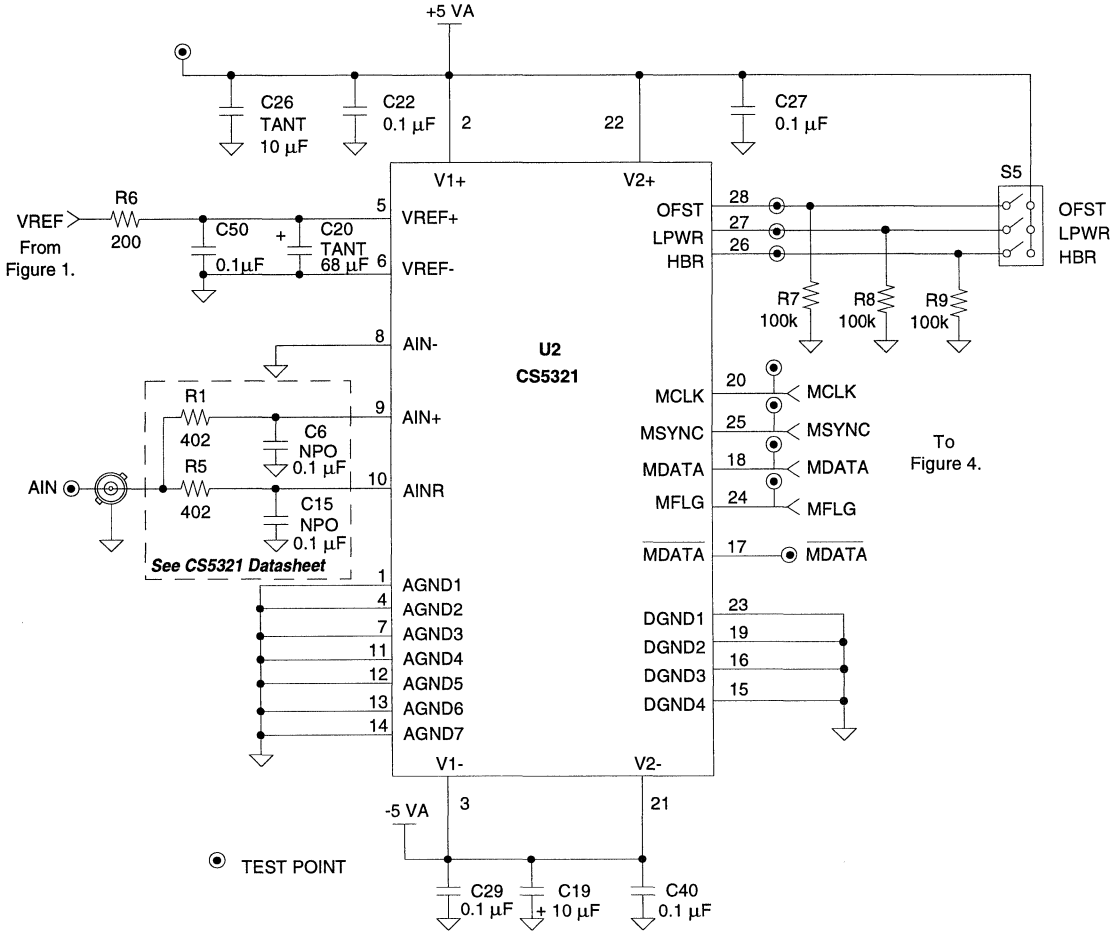


Figure 2. CS5321 Modulator Input Circuitry.

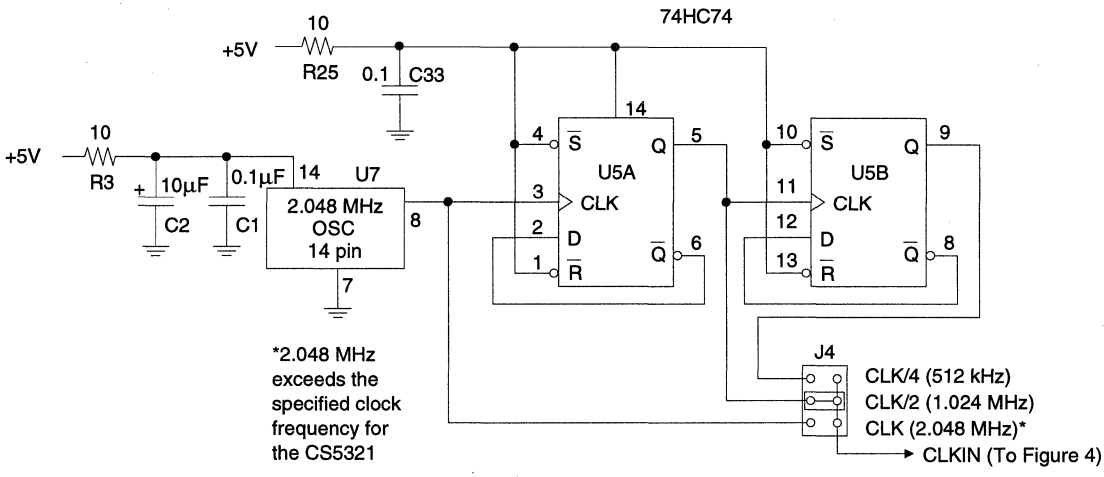


Figure 3. Oscillator / Divider

OFST=1. Figure 3 illustrates the 2.048 MHz oscillator and dual D flip flop clock divider. Note that both the oscillator and the divider are separately decoupled from the +5V supply to reduce clock jitter which can be introduced from noisy supplies. Jumper J4 should be set in the CLK/2 position to source 1.024 MHz to the CS5322 chip for normal operation. If operation from 512 kHz clock is desired, the J4 jumper should be changed to the CLK/4 position. The board can be tested at 512 kHz without modification.

The digital interface pins to the CS5322 filter chip are all available on the header connectors J1, J2, and J3 as shown in Figures 4, 5, and 6. Note that one row of pins on each of the headers is ground. It is advised that any connections made to control lines be done with twisted pair ribbon cable; with each twisted pair containing one signal and one ground connection. This minimizes radiated noise.

CAUTION!

Caution is advised when interfacing the evaluation board to any circuitry powered from another source. For example, when interfacing to a computer I/O card be sure that the evaluation board and the computer are both powered up before connecting to the evaluation board headers. Always disconnect header connections when powering down the board but not the computer. Failure to follow this advice may cause damage to either the computer I/O or to the CS5322, because the computer outputs try to power the CDB5321 board.

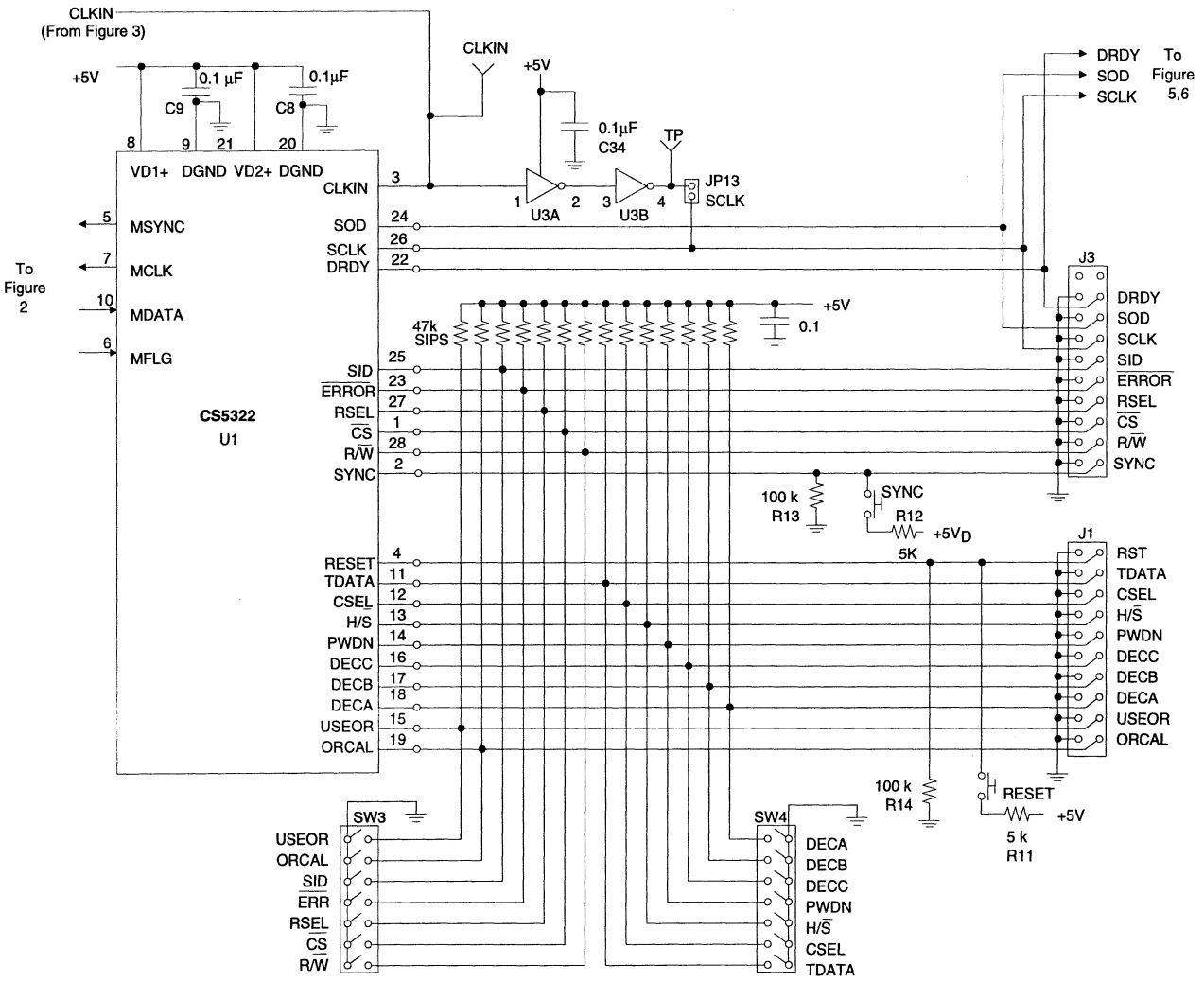


Figure 4. CS5322 Filter Interface

USEOR	ON*	Do not use offset register
	OFF	Use offset register
ORCAL	ON*	Disable offset register calibration
	OFF	Enable offset register calibration
SID	ON	Sets SID to Logic 0
	OFF*	Allows pull-up on SID line
ERR	ON	Sets ERR to logic 0
	OFF*	Allows CS5322 ERROR output
RSEL	ON	Select status register
	OFF*	Select conversion data register
CS	ON*	Chip select active
	OFF	Chip select inactive
R/$\overline{W}$	ON	Enables write mode via SID pin
	OFF*	Enables read mode via SOD pin

OFF = OPEN = 1

*Default to use Figure 6 interface.

Table 1. S3 DIP Switch Selections

DECA	Selection via hardware pins	ABC	Output Word Rate
DECB		0 0 0	62.5
DECC		1 0 0	125
		0 1 0	250
		1 1 0	500
		0 0 1	1000
		1 0 1	2000
		0 1 1	4000
PWDN	ON*	Normal Operation	
	OFF	Power down active	
H/$\overline{S}$	ON	Selects configuration register for operating mode	
	OFF*	Select hardware pins for operating mode	
CSEL	ON*	Selects MDATA from modulator	
	OFF	Selects TDATA as filter input	
TDATA	ON*	Sets TDATA input to logic 0	
	OFF	Enables TDATA from J1 header	

OFF = OPEN = 1

*Default to use Figure 6 interface.

Table 2. S4 DIP switch selections

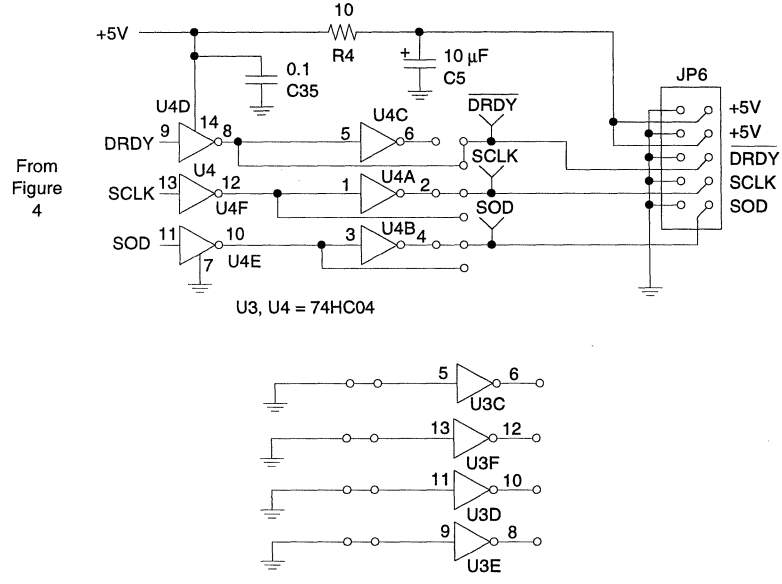


Figure 5. Serial Latch Interface on CDB5321 (Rev B) board

Figures 5 and 6 illustrate the logic used to drive connections at header JP6 (Rev. B Board) or J2 (Rev. C Board).

The Rev. C evaluation board can directly interface to the CDBCAPTURE board through connector J2. A D-type Flip-Flop must be added in the patch area of the Rev. B evaluation board to enable it to interface to the CDBCAPTURE board. The CDBCAPTURE can be used to perform FFT analysis and noise histograms.

Tables 1 and 2 illustrate the DIP switch positions of switches S3 and S4. The switch positions with asterisks indicate preferred settings for driving the interface on the CDBCAPTURE system.

The CS5322 filter should be set up for hardware mode (H/$\overline{S}$ on switch S4 open). DIP switch S4 can then be used to select the desired output word rate. After the selection on the DECA, DECB, and DECC positions of the S4 DIP switch, the S2 RESET switch must be activated, followed by the S1 SYNC switch (unless these signals are controlled via the J1 and J3 header signals).

Figure 7 illustrates the component layout of the board while figures 8 and 9 illustrate the board layout (not to scale).

2

Using the Evaluation Board

Connect the appropriate power supplies to the binding posts of the board. Twist the +5V digital supply lead with the digital ground lead from the board to the supply. Also twist the supply leads for the analog voltages. Use a high quality power supply which is low in noise and line frequency(50/60 Hz) interference.

Power up the supplies. Then connect a coaxial cable from the analog BNC to the signal source. Note that the performance of the A/D converter chip set will exceed the capability of most signal generators, with respect to noise, distortion, and line frequency interference.

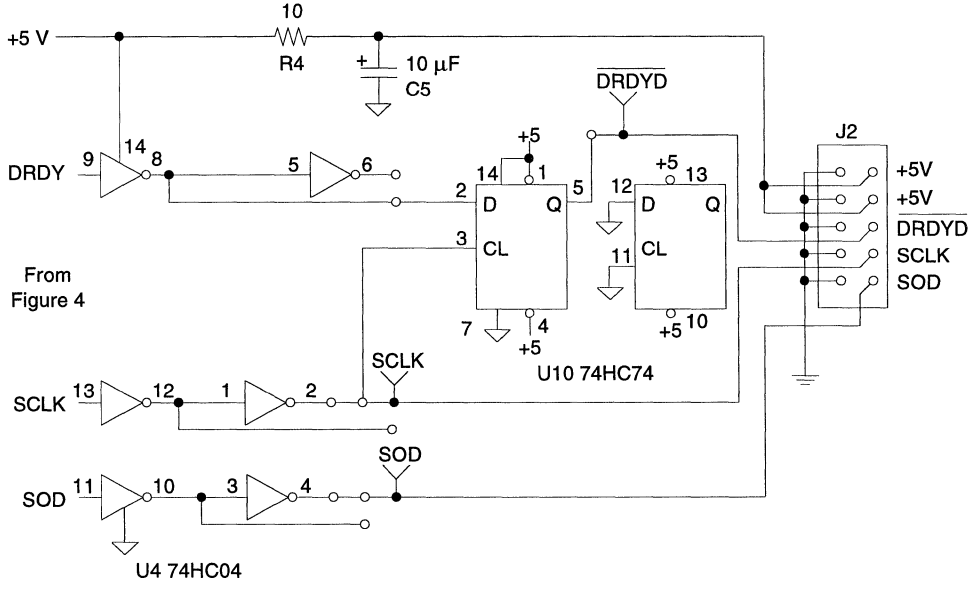


Figure 6. Serial Latch Interface on CDB5321 (Rev C) board.

Once power has been applied to the board, connect the ribbon cable to the appropriate headers (J1, J2, and/or J3). The reset and the sync signals to the CS5322 must be applied before normal operation can commence. This can be done by using the S2 RESET switch and the S1 SYNC switch or by interfacing to these signals via the J1 and J3 headers.

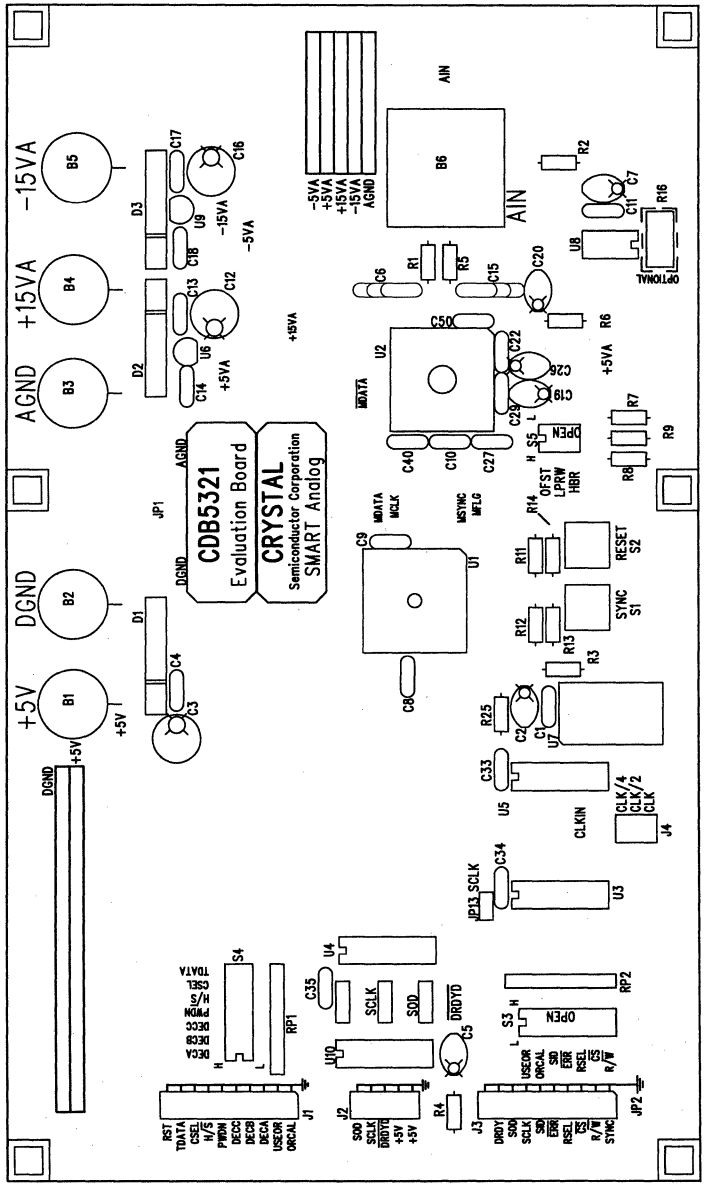


Figure 7. CDB5321 (Rev. C) Silk Screen Layout (Not to Scale)

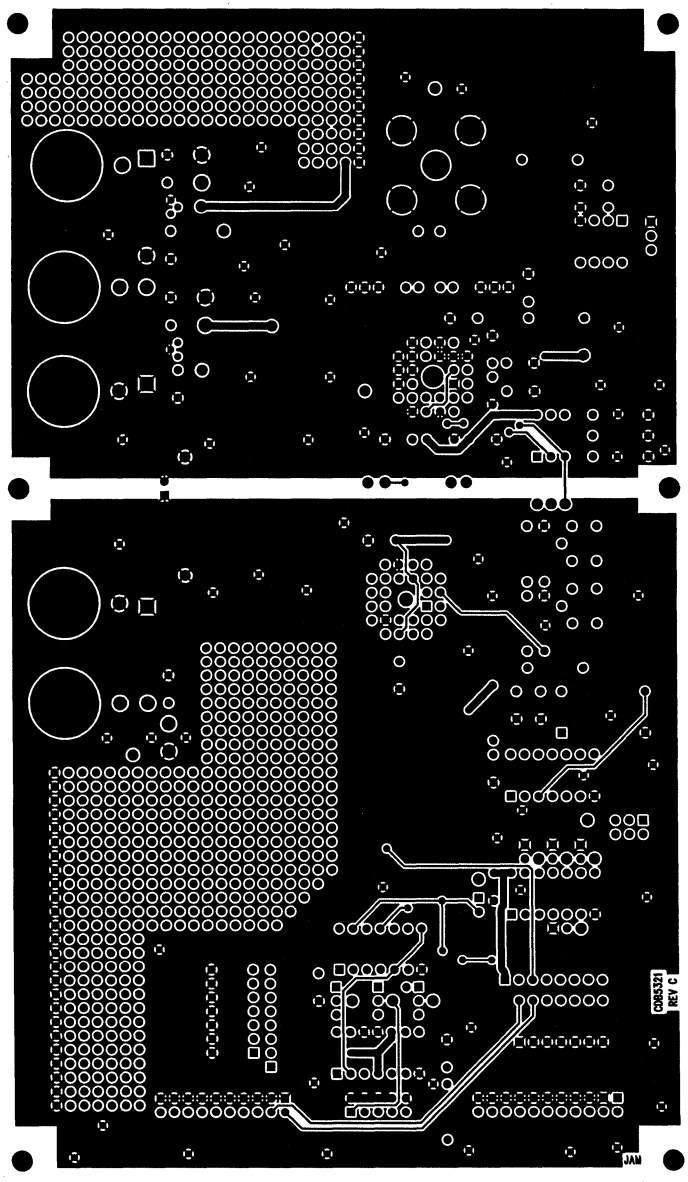


Figure 8. CDB5321 (Rev. C) Component Side Layer (Not to Scale)

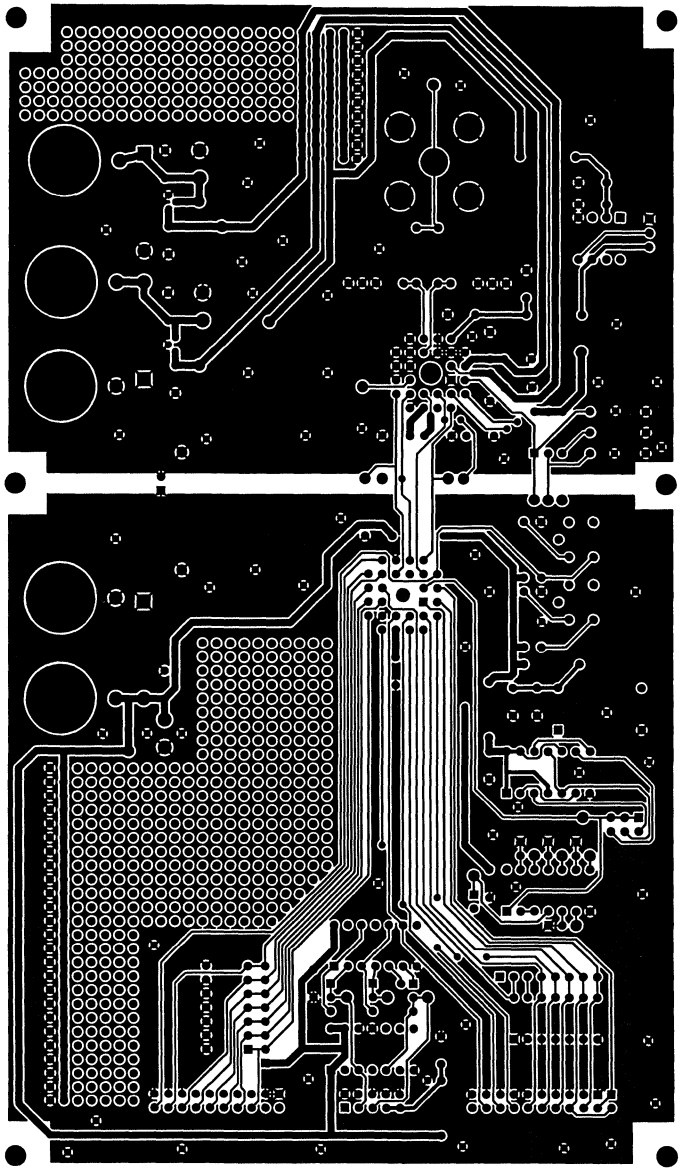


Figure 9. CDB5321 (Rev. C) Solder Side Layer (Not to Scale)

•Notes•

24-Bit Variable Bandwidth A/D Converter

Features

- Monolithic CMOS A/D Converter
- Dynamic Range
  - 130dB @ 25 Hz Bandwidth
  - 120dB @ 411 Hz Bandwidth
- Delta-Sigma Architecture
  - Variable Oversampling: 64X to 4096X
  - Internal Track-and-Hold Amplifier
- Flexible Filter Chip
  - Hardware or Software Selectable Options
  - Seven Selectable Filter Corner (-3dB) Frequencies: 25, 51, 102, 205, 411, 824 and 1650 Hz
- Low Power Dissipation: < 100mW

General Description

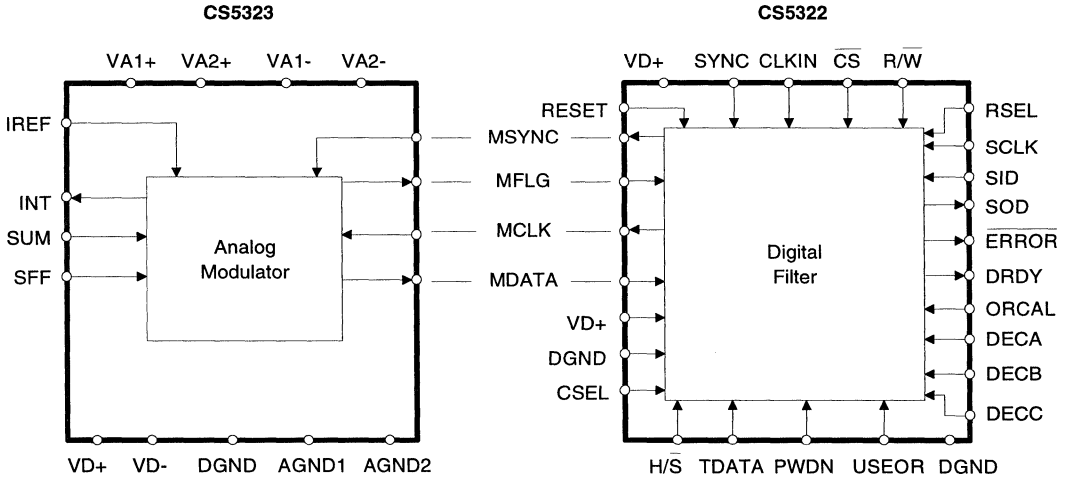
The CS5323 analog modulator and the CS5322 digital filter function together as a unique high resolution A/D converter intended for geophysical and other applications which require high dynamic range. The CS5323/CS5322 combination performs sampling, A/D conversion, and anti-alias filtering.

The pair use Delta-Sigma modulation to produce highly accurate conversions. The CS5323 oversamples, virtually eliminating the need for external anti-alias filters. The CS5322 linear-phase FIR digital filter decimates the output to any one of seven selectable update periods: 16, 8, 4, 2, 1, 0.5 and 0.25 milliseconds. Data is output from the digital filter in a 24-bit serial format.

The CMOS design of the CS5322/CS5323 achieves high reliability while minimizing power dissipation.

ORDERING INFORMATION

CS5322-KL	0 to +70 °C	28-pin PLCC
CS5322-BL	-40 to +85 °C	28-pin PLCC
CS5323-KL	0 to +70 °C	28-pin PLCC
CS5323-BL	-40 to +85 °C	28-pin PLCC



ANALOG CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA-, VD- = -5V; VA+, VD+ = 5V; AGND = 0V; CLKIN = 1.024 MHz; Device connected as shown in Figure 16; Logic 1 = VD+, Logic 0 = 0V; unless otherwise specified.)

Parameter*		Symbol	CS5323-K Min	CS5323-K Typ	CS5323-K Max	CS5323-B Min	CS5323-B Typ	CS5323-B Max	Units
Specified Temperature Range			0	-	+70	-40	-	+85	°C
Dynamic Performance									
Dynamic Range	(Note 1)	DR							
CLKIN = 1.024 MHz:	fO = 4000 Hz		-	103	-	-	103	-	dB
	fO = 2000 Hz		-	118	-	-	118	-	dB
	fO = 1000 Hz		116	121	-	116	121	-	dB
	fO = 500 Hz		-	124	-	-	124	-	dB
	fO = 250 Hz		-	127	-	-	127	-	dB
	fO = 125 Hz		-	129	-	-	129	-	dB
	fO = 62.5 Hz		-	130	-	-	130	-	dB
CLKIN = 512 kHz:	fO = 2000 Hz		-	99	-	-	99	-	dB
	fO = 1000 Hz		-	121	-	-	121	-	dB
	fO = 500 Hz		-	125	-	-	125	-	dB
	fO = 250 Hz		-	127	-	-	127	-	dB
	fO = 125 Hz		-	130	-	-	130	-	dB
	fO = 62.5 Hz		-	132	-	-	132	-	dB
	fO = 31.25 Hz		-	133	-	-	133	-	dB
Signal-to-Distortion:	(Note 2)	SDR							
	CLKIN = 1.024MHz		100	110	-	100	110	-	dB
	CLKIN = 512 kHz		-	120	-	-	120	-	dB
Intermodulation Distortion	(Note 3)	IMD	-	110	-	-	110	-	dB
dc Accuracy									
Full Scale Error	(Note 4)	FSE	-	-	4	-	-	4	%
Full Scale Drift	(Notes 4, 5)	TC_{FS}	-	0.005	-	-	0.005	-	%/°C
Offset	(Note 4)	V_{ZSE}	-	-	250	-	-	250	mV
Offset after Calibration	(Note 6)		-	±100	-	-	±100	-	µV
Offset Calibration Range	(Note 7)		-	100	-	-	100	-	%F.S.
Offset Drift	(Notes 4, 5)	TC_{ZSE}	-	500	-	-	500	-	µV/°C

Notes:
1. fo = CS5322 output word rate. Refer to CS5322 Filter Characteristics for details.
2. Tested with full scale input signal of 50 Hz; fo = 500 Hz.
3. Tested with input signals of 30 Hz and 50 Hz, each 6 dB down from full scale fo = 500 Hz.
4. Specification is for the parameter over the specified temperature range and is for the CS5323 device only (IREF = 1 mA). It does not include the effects of external components.
5. Drift specifications are guaranteed by design and characterization.
6. The offset after calibration specification applies to the effective offset voltage for a ±10 volt input to the CS5323 modulator, but is relative to the output digital codes from the CS5322 after ORCAL and USEOR have been made active.
7. The CS5322 offset calibration is performed digitally and includes ± full scale (±10 volts into CS5323). Calibration of offsets greater than ±10% of full scale will begin to subtract from the dynamic range.

* Refer to Parameter Definitions (immediately following pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA-, VD- = -5V; VA+, VD+ = 5V; AGND = 0V; CLKIN = 1.024 MHz; Device connected as shown in Figure 16; Logic 1 = VD+, Logic 0 = 0V; unless otherwise specified.)

Parameter*	Symbol	CS5323-K Min	CS5323-K Typ	CS5323-K Max	CS5323-B Min	CS5323-B Typ	CS5323-B Max	Units
Specified Temperature Range		0	-	+70	-40	-	+85	°C
Input Characteristics								
Input Signal Frequencies (Note 8)	BW	dc	-	1500	dc	-	1500	Hz
Input Voltage Range (Note 9)	V_{IN}	-10.0	-	+10.0	-10.0	-	+10.0	V
Input Overrange Voltage (Note 9)	I_{OVR}	-	-	10	-	-	10	%F.S.
Power Supplies								
DC Power Supply Currents (Note 10)								
Positive Supplies (IA+ and ID+)		-	7.0	10.0	-	7.0	10.0	mA
Negative Supplies (IA- and ID-)		-	8.4	10.0	-	8.4	10.0	mA
Power Consumption (Note 10)								
PWDN Low	P_{DN}	-	77	100	-	77	100	mW
PWDN High	P_{DS}	-	0.01	10	-	0.01	10	mW
Power Supply Rejection (Notes 11, 12) (dc to f1 Hz):	PSR							
VA+		-	60	-	-	60	-	dB
VA-		-	45	-	-	45	-	dB
VD+		-	45	-	-	45	-	dB
VD-		-	40	-	-	40	-	dB
(f1 Hz to 128 kHz):								
VA+		-	60	-	-	60	-	dB
VA-		-	60	-	-	60	-	dB
VD+		-	60	-	-	60	-	dB
VD-		-	60	-	-	60	-	dB

Notes:
8. The upper bandwidth limit is determined by the CS5322 digital filter.
9. This input voltage range is for the configuration shown in Figure 16, the System Connection Diagram, and applies to signal from dc to f3 Hz. Refer to CS5322 Filter Characteristics for the values of f3.
10. All outputs unloaded. All logic inputs forced to VA+ or GND respectively. Power down mode power consumption is with the signal source and the voltage reference source either grounded or floating.
11. Tested with a 100 mVp-p sine wave applied separately to each supply (VA1 and VA2 are considered as one input for this test).
12. Refer to CS5322 Filter Characteristics table for the values of f1.

* Refer to Parameter Definitions (immediately following pin descriptions at the end of this data sheet).

FILTER CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VD+ = 5V; GND = 0V; CLKIN = 1.024 MHz; transfer function shown in Figure 2; unless otherwise specified.)

Output Word Rate f_0 (Hz)	Passband f1 (Hz)	Passband Flatness R_{PB} (dB)	-3dB Freq. f2 (Hz)	Stopband f3 (Hz) (Note 13)	Group Delay (ms)
4000	1500	0.2	1652.5	2000	7.25
2000	750	0.04	824.3	1000	14.5
1000	375	0.08	411.9	500	29
500	187.5	0.1	205.9	250	58
250	93.8	0.1	102.9	125	116
125	46.9	0.1	51.5	62.5	232
62.5	23.4	0.1	25.7	31.25	464

Note: 13. G_{SB} = -130 dB for all Output Word Rates.

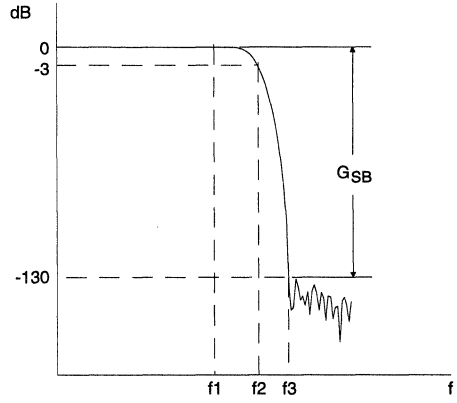


Figure 1. CS5322 Filter Response

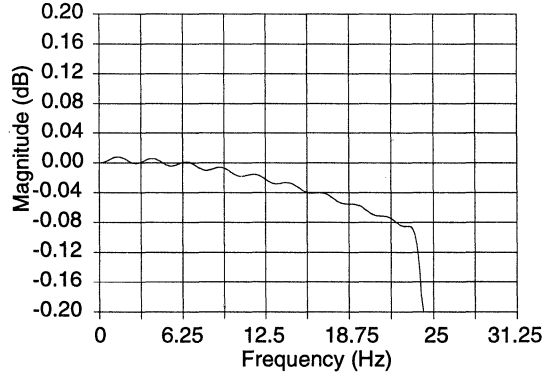


Figure 2. CS5322 Digital Filter Passband Ripple f_0 = 62.5 Hz

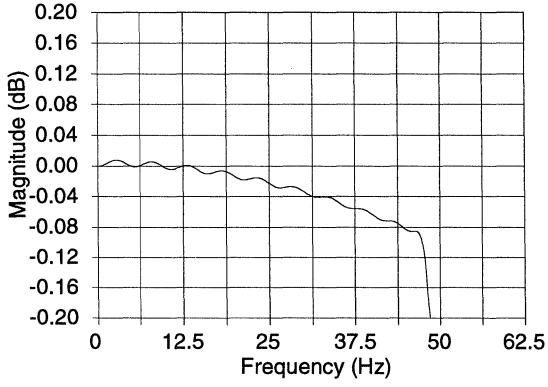


Figure 3. CS5322 Digital Filter Passband Ripple f_0 = 125 Hz

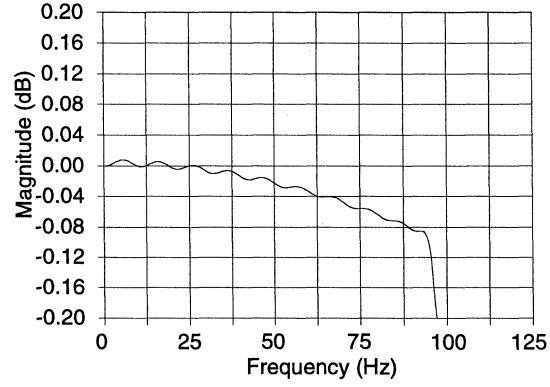


Figure 4. CS5322 Digital Filter Passband Ripple f_0 = 250 Hz

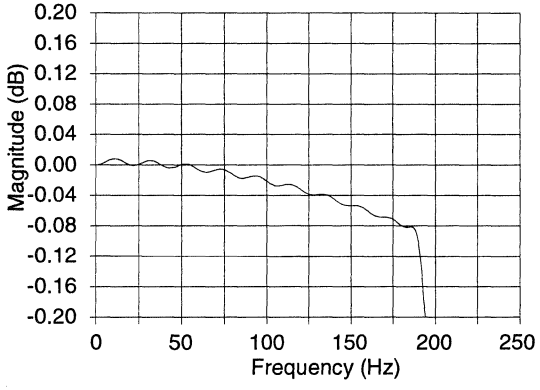


Figure 5. CS5322 Digital Filter Passband Ripple f_0 = 500 Hz

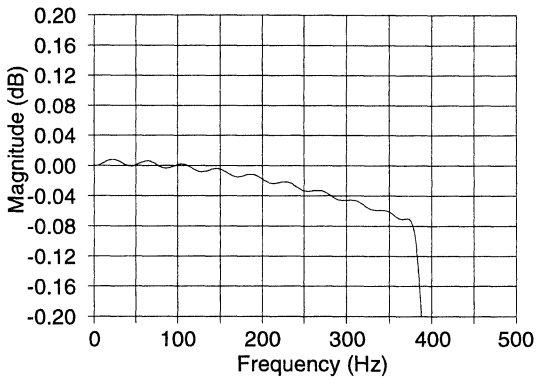


Figure 6. CS5322 Digital Filter Passband Ripple f_0 = 1000 Hz

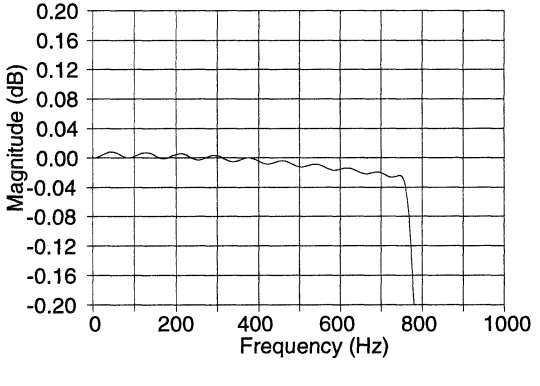


Figure 7. CS5322 Digital Filter Passband Ripple f_0 = 2000 Hz

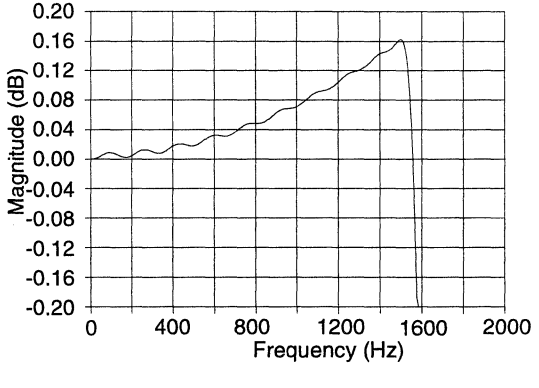


Figure 8. CS5322 Digital Filter Passband Ripple f_0 = 4000 Hz

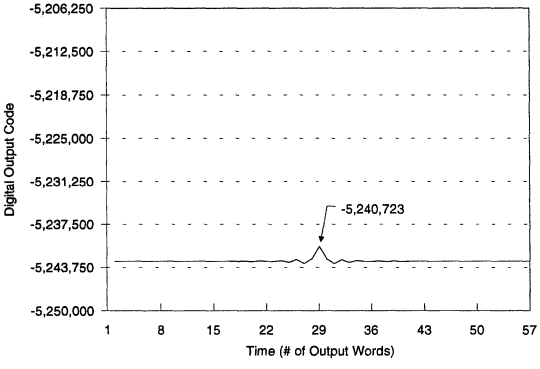


Figure 9. CS5322 Impulse Response, f_0 = 62.5 Hz

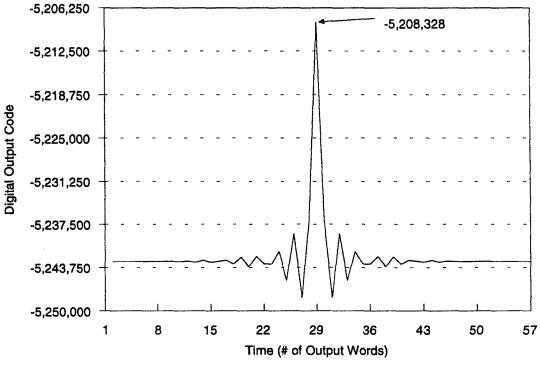


Figure 10. CS5322 Impulse Response, f_0 = 1000 Hz

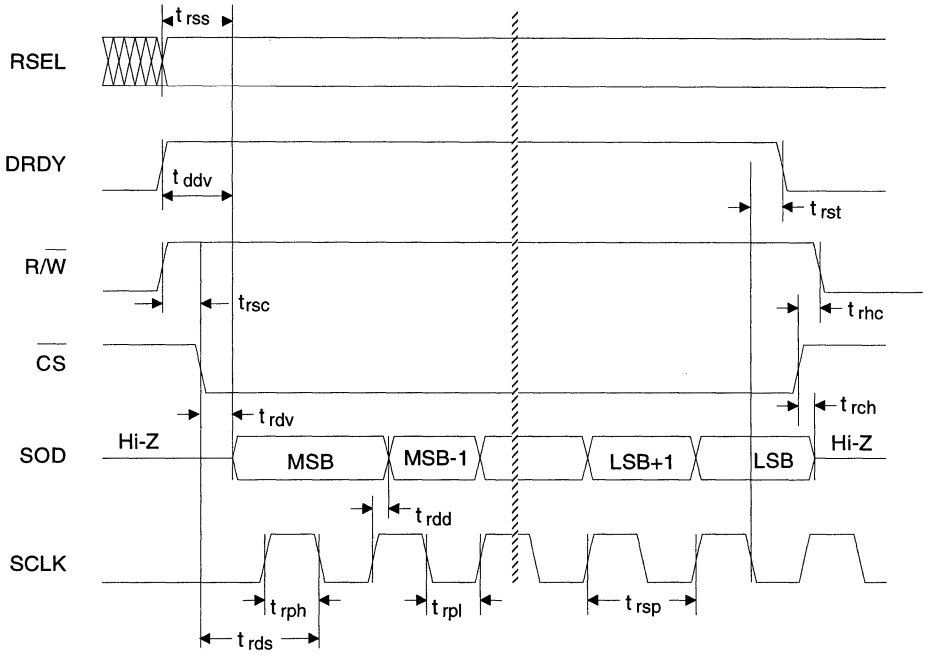
POWER SUPPLY (T_A = 25°C; VD+ = 5V; CLKIN = 1.024 MHz)

Parameter*		CS5322-K			CS5322-B			Units
		Min	Typ	Max	Min	Typ	Max	
Specified Temperature Range		0	-	+70	-40	-	+85	°C
Power Supply Current:	ID+ (Note 10)	-	2.2	4	-	2.2	4	mA
Power Dissipation:	(Note 10)							
	PWDN Low	-	11	20	-	11	20	mW
	PWDN High	-	0.6	2.5	-	0.6	2.5	mW

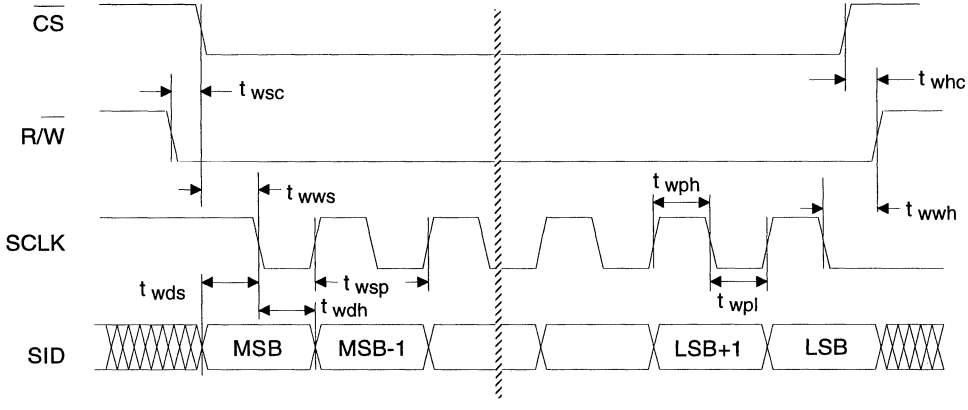
SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VD+ = 5V±5%; DGND = 0V; Inputs: Logic 0 = 0V Logic 1 = VD+; C_L = 50 pF (Note 14))

Parameter		Symbol	Min	Typ	Max	Units
CLKIN Frequency		f_c	0.512	1.024	1.1	MHz
CLKIN Duty Cycle			40	-	60	%
Rise Times:	Any Digital Input	t_{rise}	-	-	100	ns
	Any Digital Output		-	50	100	ns
Fall Times:	Any Digital Input	t_{fall}	-	-	100	ns
	Any Digital Output		-	50	100	ns
Serial Port Read Timing						
DRDY to Data Valid		t_{ddv}	-	-	25	ns
RSEL Setup Time before Data Valid		t_{rss}	50	-	-	ns
Read Setup Before $\overline{CS}$ Active		t_{rsc}	20	-	-	ns
Read Active to Data Valid		t_{rdv}	-	-	50	ns
SCLK rising to New SOD bit		t_{rdd}	-	-	50	ns
SCLK Pulse Width High		t_{rph}	30	-	-	ns
SCLK Pulse Width Low		t_{rpl}	30	-	-	ns
SCLK Period		t_{rsp}	100	-	-	ns
SCLK falling to DRDY falling		t_{rst}	-	-	50	ns
$\overline{CS}$ High to Output Hi-Z		t_{rch}	-	-	20	ns
Read Hold Time after $\overline{CS}$ Inactive		t_{rhc}	20	-	-	ns
Read Select Setup to SCLK falling		t_{rds}	20	-	-	ns
Serial Port Write Timing						
Write Setup Before $\overline{CS}$ Active		t_{wsc}	20	-	-	ns
SCLK Pulse Width Low		t_{wpl}	30	-	-	ns
SCLK Pulse Width High		t_{wph}	30	-	-	ns
SCLK Period		t_{wsp}	100	-	-	ns
Write Setup Time to First SCLK falling		t_{wws}	20	-	-	ns
Data Setup Time to First SCLK falling		t_{wds}	20	-	-	ns
Write Select Hold Time after SCLK falling		t_{wwh}	20	-	-	ns
Write Hold Time after $\overline{CS}$ Inactive		t_{whc}	20	-	-	ns
DATA Hold Time after SCLK falling		t_{wdh}	20	-	-	ns

Note: 14. Guaranteed by design, characterization and/or test.



SERIAL PORT READ TIMING (R/$\overline{W}$ = 1, CS = 0, RSEL = 1
* DRDY Does not toggle if reading status, RSEL = 0)

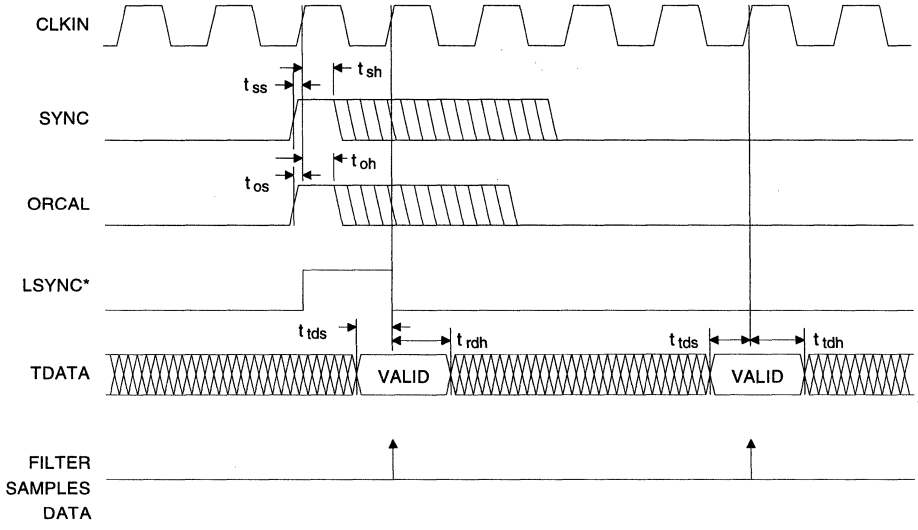


SERIAL PORT WRITE TIMING

Figure 11. CS5322 Serial Port

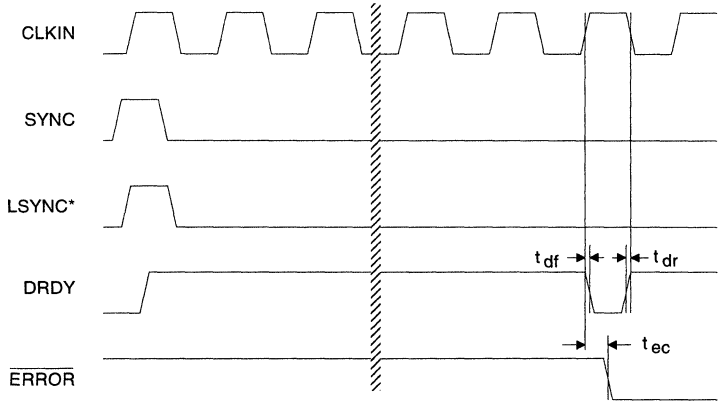
SWITCHING CHARACTERISTICS (continued)

Parameter	Symbol	Min	Typ	Max	Units
Test Data (TDATA) Timing					
SYNC Setup Time to CLKIN rising	t_{ss}	20	-	-	ns
SYNC Hold Time after CLKIN rising	t_{sh}	20	-	-	ns
TDATA Setup Time to CLKIN rising after SYNC	t_{tds}	-	20	-	ns
TDATA Hold Time after CLKIN rising	t_{tdh}	-	150	-	ns
ORCAL Setup Time to CLKIN rising	t_{os}	20	-	-	ns
ORCAL Hold Time after CLKIN rising	t_{oh}	20	-	-	ns
DRDY Timing					
CLKIN rising to DRDY falling	t_{df}	-	140	-	ns
CLKIN falling to DRDY rising	t_{dr}	-	150	-	ns
CLKIN rising to ERROR change	t_{ec}	-	140	-	ns
RESET Timing					
RESET Setup Time to CLKIN rising	t_{rs}	20	-	-	ns
RESET Hold Time after CLKIN rising	t_{rh}	20	-	-	ns
SYNC Setup Time to CLKIN rising	t_{ss}	20	-	-	ns
SYNC Hold Time after CLKIN rising	t_{sh}	20	-	-	ns



* Note: Internal timing signal generated in the CS5322

Figure 12. TDATA Setup/Hold Timing



*Note: For overwrite case, DRDY will remain high.

Figure 13. DRDY Timing

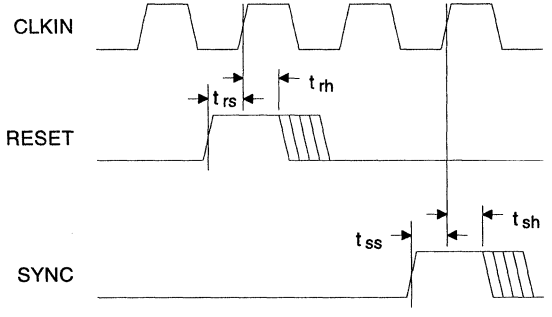
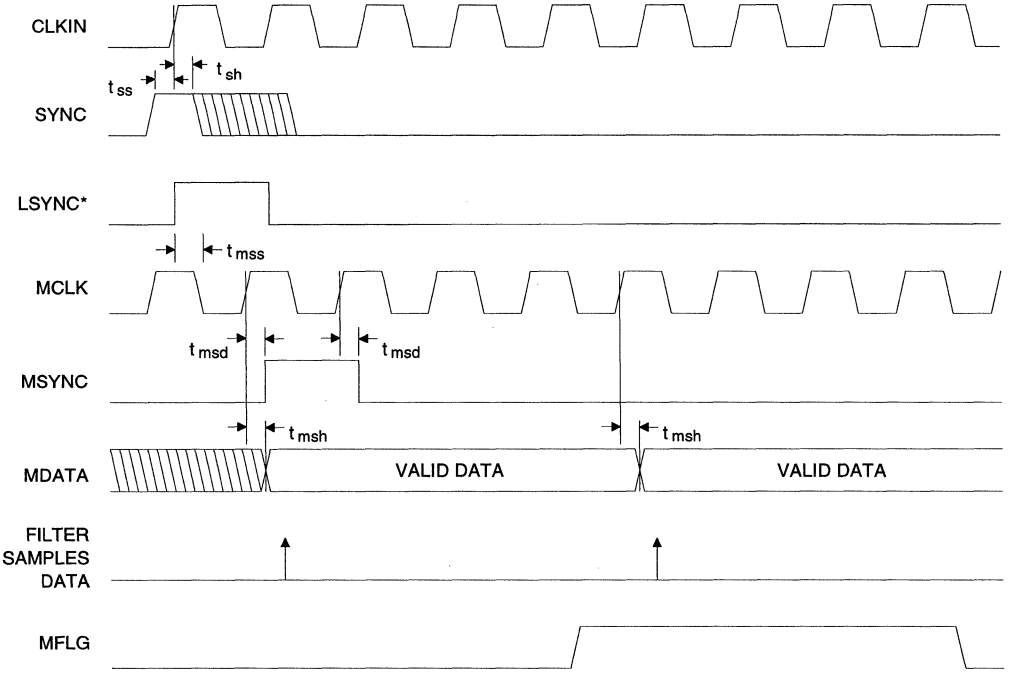


Figure 14. RESET Timing

SWITCHING CHARACTERISTICS (continued)

Parameter			Symbol	Min	Typ	Max	Units
MCLK Frequency		(Note 15)	f_c	0.512	1.024	1.1	MHz
MCLK Duty Cycle				40	-	60	%
Rise Times:	Any Digital Input	(Note 16)	t_{rise}	-	-	100	ns
	Any Digital Output			-	50	200	ns
Fall Times:	Any Digital Input	(Note 16)	t_{fall}	-	-	100	ns
	Any Digital Output			-	50	200	ns
SYNC Setup Time to CLKIN rising			t_{ss}	20	-	-	ns
SYNC Hold Time after CLKIN rising			t_{sh}	20	-	-	ns
CLKIN edge to MCLK edge			t_{mss}	-	30	-	ns
MCLK rising to Valid MDATA			t_{msh}	-	50	-	ns
MSYNC Delay from MCLK rising		(Note 17)	t_{msd}	-	90	-	ns

Notes: 15. If MCLK is removed, the device will enter the power down mode.
16. Excludes MCLK input. MCLK should be driven with a signal having rise and fall times of 25 ns or faster.
17. Only the rising edge of MSYNC relative to MCLK is used to synchronize the device. MSYNC can return low at any time as long as it remains high for at least one MCLK cycle.



* Internal timing signal generated in the CS5322

Figure 15. CS5322/CS5323 Interface Timing

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; VD+ = 5.0V±5%; GND = 0V; measurements performed under static conditions)

Parameter			Symbol	Min	Typ	Max	Units
High-Level Input Drive Voltage			V_{IH}	(VD+)-0.3	-	-	V
Low-Level Input Drive Voltage			V_{IL}	-	-	0.3	V
High-Level Input Threshold		(Note 18)		(VD+)-1.0	-	-	V
Low-Level Input Threshold		(Note 18)		-	-	1.0	V
High-Level Output Voltage	I_{OUT} = -40µA	(Note 19)	V_{OH}	(VD+)-0.6	-	-	V
Low-Level Output Voltage		(Note 19)	V_{OL}				
	I_{OUT} = +1.6mA	CS5322		-	-	0.4	V
	I_{OUT} = +40µA	CS5323		-	-	0.4	V
Input Leakage Current	All pins except MFLG, SOD		I_{LKG}	-	-	±10	µA
Three-State Leakage Current			I_{OZ}	-	-	±10	µA
Digital Input Capacitance			C_{IN}	-	9	-	pF
Digital Output Capacitance			C_{OUT}	-	9	-	pF

Notes: 18. Device is intended to be driven with CMOS logic levels.
19. Device is intended to be interfaced to CMOS logic. Resistive loads are not recommended on these pins.

RECOMMENDED OPERATING CONDITIONS (Voltages with respect to GND = 0V)

Parameter			Symbol	Min	Typ	Max	Units
DC Supply:		(Note 20)					
	Positive Analog		VA+	4.75	5.0	5.25	V
	Negative Analog		VA-	-4.75	-5.0	-5.25	V
	Positive Digital		VD+	4.75	5.0	5.25	V
	Negative Digital		VD-	-4.75	-5.0	-5.25	V
Ambient Operating Temperature		-KL	T_A	0	-	+70	°C
		-BL	T_A	-40	-	+85	°C

Notes: 20. The maximum voltage differential between the Positive Supply of the CS5323 and the Positive Digital Supply of the CS5322 must be less than 0.25V.

ABSOLUTE MAXIMUM RATINGS* (Voltages with respect to GND = 0V)

Parameter			Symbol	Min	Typ	Max	Units
DC Supply:		(Note 20)					
	Positive Analog		VA+	-0.3	-	6.0	V
	Negative Analog		VA-	0.3	-	-6.0	V
	Positive Digital		VD+	-0.3	-	(VA+)+0.3	V
	Negative Digital		VD-	0.3	-	-6.0	V
Input Current, Any Pin Except Supplies		(Note 21)	I_{in}	-	-	±10	mA
Digital Input Voltage	CS5322		V_{IND}	-0.3	-	(VD+)+0.3	V
	CS5323		V_{IND}	-0.3	-	(VA+)+0.3	V
Storage Temperature			T_{stg}	-65	-	150	°C

Notes: 21. Transient currents of up to 100 mA will not cause SCR latch up.

*WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

GENERAL DESCRIPTION

The CS5322 is a monolithic digital Finite Impulse Response (FIR) filter with programmable decimation. The CS5323 is a monolithic CMOS A/D converter designed specifically for very high resolution measurement of signals between dc and 1500 Hz. The CS5322 and CS5323 are intended to be used together to form a unique high resolution A/D system.

The CS5323 utilizes a fourth order oversampling architecture to achieve high resolution A/D conversion. The modulator consists of a 1-bit A/D converter embedded in a negative feedback loop. The first stage of the fourth order modulator uses discrete components external to the chip to maximize signal to noise. The modulator provides an oversampled serial bit stream at 256 Kbits per second (CLKIN = 1.024 MHz) to the CS5322 FIR decimation filter.

The CS5322 provides the digital anti-alias filter for the CS5323 modulator output. The CS5322 consists of: A multi-stage FIR filter, four registers (status, data, offset, and configuration), a flexible serial input and output port, and a 2-channel input data multiplexer that selects data from the CS5323 (MDATA) or user test data (TDATA). The CS5322 decimates (64X to 4096X) the output to any of seven selectable update periods: 16, 8, 4, 2, 1, 0.5 and 0.25 milliseconds. Data is output from the digital filter in a 24-bit serial format. Figure 16 illustrates the CS5322 Block Diagram.

CS5323 Signal Input and Current Reference

The CS5323 uses a number of external discrete components to achieve maximum rated performance. Figure 17 illustrates the recommended circuit configuration for the current reference and signal input components.

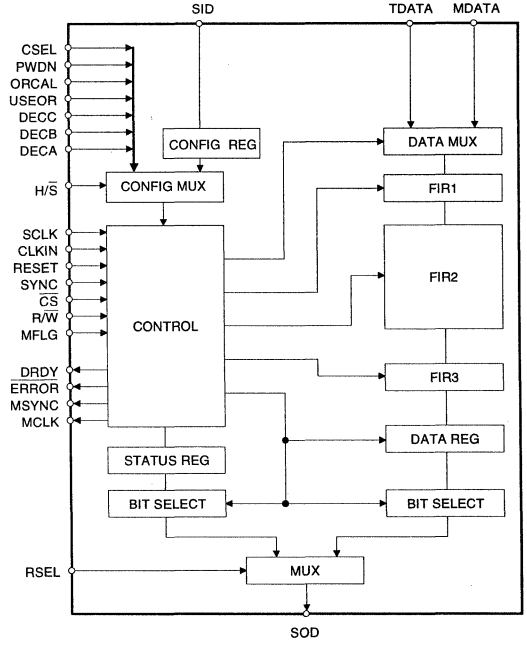


Figure 16. CS5322 Block Diagram

The CS5323 is designed to use a current reference of 1 mA into the IREF pin. A current reference rather than a voltage reference was chosen to achieve better noise performance. For optimum performance the dc source impedance at the IREF pin should be approximately 10 kΩ. This calls for a 10 volt reference source driving the 10 kΩ (R_6 + R_7) resistor to achieve the desired 1 mA current source. The IREF input sets the full scale gain of the A/D converter.

A current source 1/4 the size of the IREF input current must be sourced into the integrator summing junction at the SUM pin. This requires a 40 kΩ resistance (R_4 + R_5) be placed from the 10 volt reference to the SUM pin.

The 1 mA IREF current and the 250 µA sources have capacitive filtering to aid in reducing the broadband current noise from the voltage reference. These capacitors should be of quality construction. Particular attention should be paid to leakage current variation over the desired operating temperature, as this leakage will affect the system gain.

The signal input pin (SUM) of the CS5323 is the summing junction of the input integrator stage. This integrator is designed to use an external input resistor (R_1) and integrating capacitor (C_1). In addition, a capacitor (C_2) is required at this node for proper compensation of the integrator. The size of the input resistor (R_1) is determined

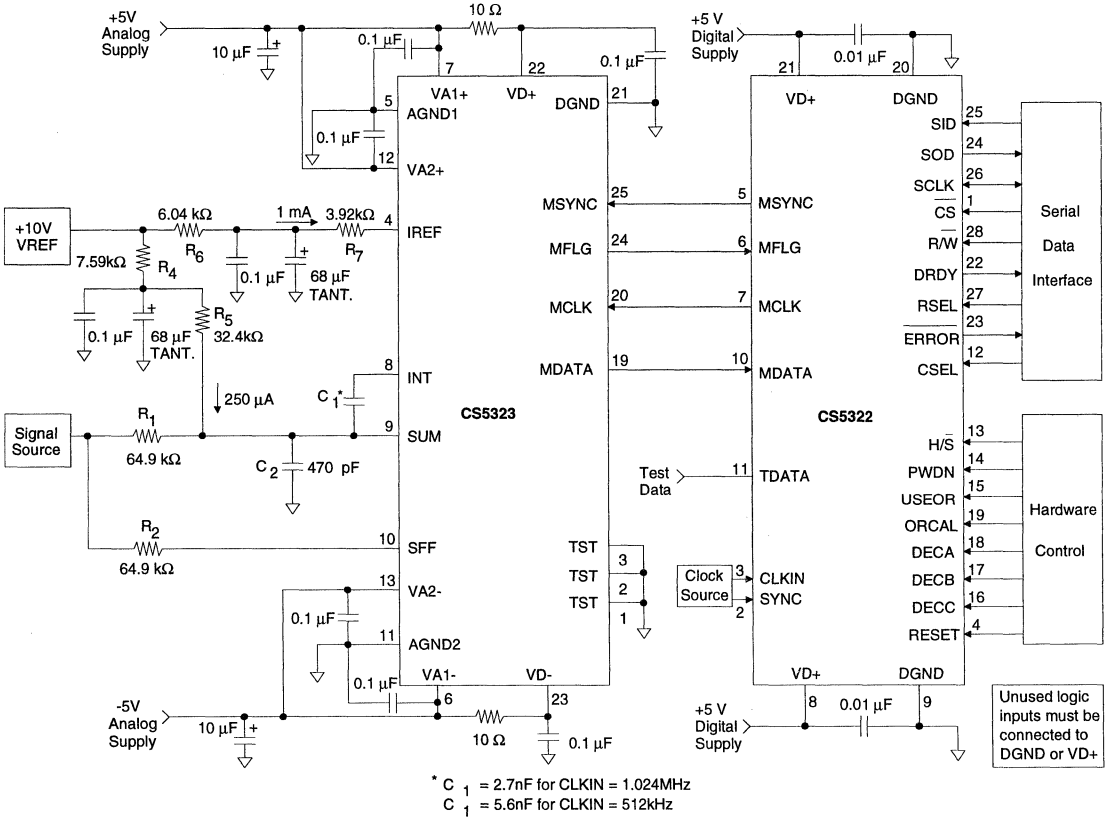


Figure 17. System Connection Diagram

by the magnitude of the signal current. With a maximum input voltage onto the resistor, the integrator input current must be set equal to approximately 0.15 the current value injected into the IREF pin. With a 1 mA IREF current, the full scale signal current should be about 150 µA. Additionally, to minimize current noise into the summing junction, the value of the effective input resistor should be above 8 kΩ. Using the 64.9 kΩ resistor for R_1 sets the full scale input voltage onto the integrating resistor to a value near 10 volts. The input signal then spans 20 V_{p-p}.

The integrator resistor and capacitor combination should yield a frequency ($f=1/(2\pi R_1 C_1)$) between 850 and 950 Hz to achieve maximum performance. This results in a capacitor value of 2.7 nF. The capacitor should be chosen to minimize leakage, dielectric absorption, and the voltage coefficient of capacitance. High quality film capacitors may be acceptable in many applications.

The signal into the SFF pin (Signal Feedforward) of the CS5323 bypasses the input stage of the input integrator and improves distortion performance in the passband. The resistor (R_2) used at this input should be identical in value and performance characteristics to that of the resistor on the input of the SUM pin (R_1).

Although the CS5323 (Figure 17) input is designed to accept 20 Vp-p, modulator loop stability can be adversely affected by high frequency out-of-band signals. Therefore, input signals above 8 kHz should be at least 6 dB below full scale to prevent oscillation in the modulator loop and to ensure proper conversion data.

RESET Operation

The RESET pin puts the CS5322 into a known initialized state. RESET is recognized on the next CLKIN rising edge after the RESET pin has been brought high (RESET=1). All internal logic is initialized when RESET is active.

Normal device operation begins on the second CLKIN rising edge after RESET is brought low. The CS5322 will remain in an idle state, not performing convolutions, until triggered by a SYNC event.

A RESET operation clears memory, sets the data output register, offset register, and status flags to all zeroes, and sets the configuration register to the the state of the corresponding hardware pins (PWDN, ORCAL, DECC, DECB, DECA, USEOR, and CSEL). The reset state is entered on power on, independent of the RESET pin. If RESET is low, the first CLKIN will exit the power on reset state.

Power-down Operation

The PWDN pin puts the CS5322 into the power-down state. The power-down state is entered on the first CLKIN rising edge after the PWDN pin is brought high. While in the power-down state, the MCLK and MSYNC signals to the CS5323 analog modulator are held low. The loss of the MCLK signal to the modulator causes it to power-down. The signals on the MDATA and MFLG pins are ignored. The serial interface of the CS5322 remains active allowing read and write operations. Information in the data register, offset register, configuration register, and convolution data memory are maintained during power-down. The internal controller requires 64 clock cycles after PWDN is asserted before CLKIN stops.

The CS5322 exits the power-down state on the first CLKIN rising edge after the PWDN pin is brought low. The CS5322 then enters an idle state until triggered by a SYNC event.

To avoid possible high current states while in the power down state, the following conditions apply:

1. CLKIN must be active for at least 64 clock cycles after PWDN entry.
2. CSEL and TDATA must not both be asserted high.

SYNC Operation

The SYNC pin is used to start convolutions and synchronize the CS5322 and CS5323 to an external sampling source or timing reference. The SYNC event is recognized on the first CLKIN rising edge after the SYNC pin goes high. SYNC may remain high indefinitely. Only the sequence of SYNC rising followed by CLKIN rising generates a SYNC event.

The SYNC event aligns the output sample and causes the filter to begin convolutions. The first SYNC event causes an immediate DRDY provided DRDY is low. Subsequent data ready events will occur at a rate determined by the decimation rate inputs DECC, DECB, and DECA. Multiple SYNC events can be applied with no effect on operation if they are perfectly timed according to the decimation rate. Any SYNC event not in step with the decimation rate will cause a re-alignment and loss of data.

Serial Read Operation

Serial read is used to obtain status or conversion data. The $\overline{CS}$, R/$\overline{W}$, SCLK, RSEL, and SOD pins control the read operation. The serial read operation is activated when $\overline{CS}$ goes low ($\overline{CS}$=0) with the R/$\overline{W}$ pin high (R/$\overline{W}$=1). The RSEL pin selects between conversion data (data register) or status information (status register). The selected serial bit stream is output on the SOD (Serial Output Data) pin.

On read select, SCLK can either be high or low, the first bit appears on the SOD pin and should be latched on the falling edge of SCLK. After the first SCLK falling edge, each SCLK rising edge shifts out a new bit. Status reads are 16 bits, and data reads are 24 bits. Both streams are supplied as MSB first, LSB last.

In the event more SCLK pulses are supplied than necessary to clock out the requested information, trailing zeroes will be output for data reads and trailing LSB's for status reads. If the read operation is terminated before all the bits are read, the internal bit pointer is reset to the MSB so that a re-read will give the same data as the first read, with one exception. The status error flags are cleared on read and will not be available on a re-read.

The status error flags must be read before entering the powerdown state. If an error has occurred before entering powerdown and the status bit (ERROR) has not been read, the status bits (ERROR, OVERWRITE, MFLG, ACC1 and ACC2) may not be cleared on status reads. Upon exiting the powerdown state and entering normal operation, the user may be flagged that an error is still present.

The SOD pin floats when read operation is deactivated (R/$\overline{W}$=1, $\overline{CS}$=1). This enables the SID and SOD pins to be tied together to form a bi-directional serial data bus. There is an internal nominal 100kΩ pull-up resistor on the SOD pin.

Serial Write Operation

Serial write is used to write data to the configuration register. The $\overline{CS}$, R/$\overline{W}$, SCLK and SID pins control the serial write operation. The serial write operation is activated when $\overline{CS}$ goes low ($\overline{CS}$=0) with R/$\overline{W}$ pin low (R/$\overline{W}$=0).

Serial input data on the SID pin is sampled on the falling edge of SCLK. The input bits are stored in a temporary buffer until either the write operation is terminated or 8 bits have been received. The data is then parallel loaded into the configuration register. If fewer than 8 bits are input before the write termination, the other bits may be indeterminate.

Note that a write will occur when $\overline{CS}$ = 0 and R/$\overline{W}$ = 0 even if SCLK is not toggled. Failure to clock in data with the appropriate number of SCLKs can leave the configuration register in an indeterminate condition.

The serial bit stream is received MSB first, LSB last. The order of the input control data is PWDN first, followed by ORCAL, USEOR, CSEL, Reserved, DECC, DECB, and DECA The configuration data bits are defined in Table 1. The configuration data controls device operation when only in the software mode, i.e., the H/$\overline{S}$ pin is low (H/$\overline{S}$=0). The Reserved configuration data bit must always be written low.

Offset Calibration Operation

The offset calibration routine computes the offset produced by the CS5323 modulator and stores this value in the offset register. The USEOR pin or bit determines if the offset register data is to be used to correct output words.

After power is applied to the chip set the CS5322 must be RESET. To begin an offset calibration, the CS5323 analog input must represent the offset value. Then in software mode (H/$\overline{S}$ = 0) the ORCAL bit must be toggled from a low to a high. In hardware mode the ORCAL pin must be toggled low for at least one CLKIN cycle, then taken high (except when ORCAL = 1 and the CS5322 is RESET as this toggles the ORCAL internally). After ORCAL has been toggled, the SYNC signal must be applied to the CS5322. The filter settles on the input value in 56 output words. The output word rate is determined by the state of the the decimation rate control pins, DECC, DECB, and DECA. On the 57th output word, the CS5322 issues the ORCALD status flag, outputs the offset data sample, and internally loads the offset register. During calibration, the offset register value is not used.

If USEOR is high (USEOR=1), subsequent samples will have the offset subtracted from the output. The state of USEOR must remain high for the complete duration of the convolution cy-

Input Bit #	Equivalent Hardware Function	Description
1 (MSB)	PWDN	Standby mode
2	ORCAL	Self-offset calibration
3	USEOR	Use Offset Register
4	CSEL	Channel Select
5	Reserved	Factory use only
6	DECC	Filter BW selection
7	DECB	Filter BW selection
8 (LSB)	DECA	Filter BW selection

Table 1. Configuration Data Bits

Output Bit #	Function	Description
1 (MSB)	ERROR	Detects one of the errors below
2	OVERWRITE Error	Overwrite Error
3	MFLG Error	Modulator Flag Error
4	ACC1 Error	Accumulator 1 Error
5	ACC2 Error	Accumulator 2 Error
6	DRDY	Data Ready
7	1SYNC	First sample after SYNC
8	ORCALD	Offset calibration done
9	PWDN	Standby mode
10	ORCAL	Self-offset calibration
11	USEOR	Use Offset Register
12	CSEL	Channel Select
13	Reserved	Factory use only
14	DECC	Bandwidth Selection Status
15	DECB	Bandwidth Selection Status
16	DECA	Bandwidth Selection Status

Table 2. Status Data (from the SOD Pin)

cle. If USEOR is low (USEOR=0), the output word is not corrected, but the offset register retains its value for later use. The results of the last calibration will be held in the offset register until the end of a new calibration, or until the CS5322 is reset using the RESET pin. USEOR does not alter the offset register value, only its usage.

To restart a calibration, ORCAL and SYNC must be taken low for at least one CLKIN cycle. ORCAL must then be taken high. The calibration will restart on the next SYNC event. If the ORCAL pin remains in a high state, only a single calibration will start on the first SYNC signal.

Status Bits

The Status Register is a 16-bit register which allows the user to read the flags and configuration settings of the CS5322. Table 2 documents the data bits of the Status Register.

The ERROR flag, $\overline{\text{ERROR}}$, is the OR'ed result of OVERWRITE, MFLG, ACC1, and ACC2. The ERROR bit is active high whenever any of the four error bits are set due to a fault condition. The $\overline{\text{ERROR}}$ output has a nominal 100KΩ internal pull-up resistor.

The OVERWRITE bit is set when new conversion data is ready to be loaded into the data register, but the previous data was not completely read out. This can occur on either of two conditions: a read operation is in progress or a read operation was started, then aborted, and not completed. These two conditions are data read attempts. The attempt is identified by the first SCLK low edge (MSB read) of a data register read. If a data register read is not attempted, the CS5322 assumes that data is not wanted and does not assert OVERWRITE, and the old data is over-written by the new data. On an OVERWRITE condition, the old partially read data is preserved, and the new data word is lost.

Status reads have no effect on OVERWRITE assert operations. The OVERWRITE bit is cleared on a status register read or RESET.

The MFLG error bit reflects the CS5323 MFLG signal. Any high level on the CS5322 MFLG pin will set the MFLG status bit. The bit is cleared on a status register read or RESET operation, only if the MFLG pin on the CS5322 has returned low. A internal nominal 100KΩ pull-down resistor is on the MFLG pin.

The accumulator error bits, ACC1 and ACC2, indicate that an underflow or overflow has occurred in the FIR1 filter for ACC1, or the FIR2 and FIR3 filters for ACC2. Both errors are cleared on a status read, provided the error conditions are no longer present. In normal operation the ACC1 error will only occur when the input data stream to FIR1 is all 1's for more than 32 bits. The ACC2 error cannot occur in normal operation.

The DRDY bit reflects the state of the DRDY pin. DRDY rising edge indicates that a new data word has been loaded into the data register and is available for reading. DRDY will fall after the SCLK falling edge that reads the data register LSB. If no data read attempt is made, DRDY will pulse low for 1/2 CLKIN cycle, providing a positive edge on the new data availability. In the OVERWRITE case, DRDY remains high because new data is not loaded at the normal end of conversion time.

The 1SYNC status bit provides an indication of the filter group delay. It goes high on the second output sample after SYNC and is valid for only that sample. For repetitive SYNC operations, SYNC must run at one fourth the output word rate or slower to avoid interfering with the 1SYNC operation. With these slower repetitive SYNC's or non-periodic SYNC's separated by at least three output words, 1SYNC will occur on the second output sample after SYNC.

ORCALD indicates that calibration of the offset register is complete and the offset sample is available in the output register. This flag is high only during that sample and is otherwise low.

The remaining eight status bits (PWDN, ORCAL, USEOR, CSEL, Reserved, DECC, DECB, AND DECA) provide configuration readback for the user. These bits echo the control source for the CS5322 such that in the hardware mode ($H/\overline{S}$=1), they follow the corresponding input pins. In host mode ($H/\overline{S}$=0) they follow the corresponding configuration bits.

A brief explanation of the eight bits are as follows:

PWDN - When high, indicates that the CS5322 is in the power-down state.

ORCAL - When high, indicates a potential calibration start.

USEOR - When high, indicates the Offset Register is used. During calibration, this bit will read zero indicating the offset register is not being used during calibration.

CSEL - When high, TDATA is selected as the filter source. When low, the MDATA output signal from the CS5323 is selected as the input source to the filter.

Reserved - Always reads low.

DECC, DECB, and DECA - Indicate the decimation rate of the filter and are defined in Table 3.

DECC	DECB	DECA	Output Word Rate (Hz)	Clocks Filter Output
0	0	0	62.5	16384
0	0	1	125	8192
0	1	0	250	4096
0	1	1	500	2048
1	0	0	1000	1024
1	0	1	2000	512
1	1	0	4000	256
1	1	1	Reserved	-

Table 3. Bandwidth Selection: Truth Table

Digital Output and Data Format

For proper operation the CS5322 must be provided with a CMOS-compatible clock into the CLKIN pin. The normal operating frequency is 1.024 MHz. This clock determines the input sample rate. The sample rate is CLKIN/4 while the output word rate is determined by the status of the DECC, DECB, and DECA input pins or configuration bits; depending whether in the hardware mode or host mode.

The CS5322 computes a serial 24-bit output word in two's complement format. The output codes range from decimal -5242880 to +5242879 for a ±10V sine wave input into the CS5323 modulator as shown in Table 4.

Modulator Input Signal	Digital Filter Output Code	
	HEX	Decimal
approx. +16V†	7FEFFF	+8384511
approx. +11V	57FFFF	+5767167
approx. +10V	4FFFFF	+5242879
0V	000000	0
approx. -10V	B00000	-5242880
approx. -11V	A00000	-5767168
approx. -16V†	800000	-8388608

† This is an overrange condition

Table 4. Output Coding for the CS5322 and CS5323 combination

Performance

The CS5322/23 A/D converter is intended for use in seismic and passive sonar applications. These applications require particularly high dynamic range capability. The CS5322/23 offers high dynamic range without compromising spectral purity. The CS5322/23 typically achieves 120 dB of dynamic range, while maintaining signal/distortion at 110 dB.

An A/D converter system using the CS5322/23 A/D converter as its core was tested using Fast Fourier Transform techniques. Data was collected from the CS5322/23 serially via a UART interface to a PC-compatible computer. The output from the CS5322 was submitted to a windowing algorithm and then to the FFT algorithm. Figure 18 illustrates the performance of the CS5322/23 when tested with a full scale 100 Hz signal for the 2 ms filter selection. The CS5322/23 exhibits some second harmonic but no third harmonic. The test frequency of 100 Hz was selected, as this was the center frequency of a bandpass filter constructed to reject harmonics and line frequencies present at the output of the signal generator. Figure 19 illustrates the performance of the CS5322/23 (100 Hz input signal) for the 1 ms filter selection. Note that the performance of the CS5322/23 will generally exceed the capability of most available sine wave test generators for frequencies between 2-500 Hz. The excess noise is due to the signal source.

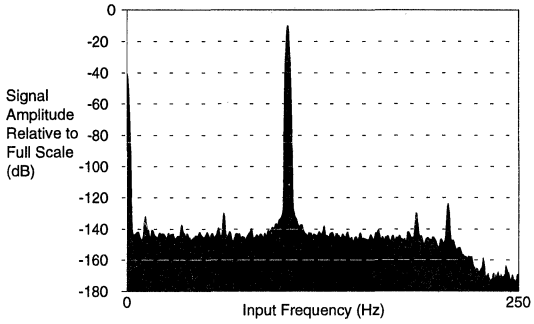


Figure 18. 1024 Point FFT Plot with Full Scale Input, 100 Hz.

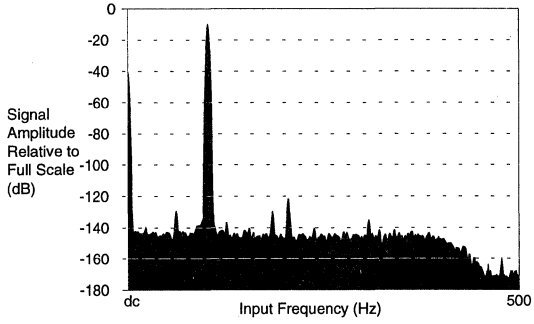


Figure 19. 1024 Point FFT Plot with Full Scale Input, 100 Hz.

Clock Source Considerations

To obtain maximum performance from the CS5322/CS5323 chip set requires a CLKIN signal with a very low level of clock jitter, i.e., less than 10 picoseconds of jitter. A well designed crystal-based clock is preferred. The clock oscillator should have a well-regulated supply, with local bypass capacitors at the oscillator. The output from the oscillator should pass through as few logic gates or counter-divider stages as possible. Excess clock jitter will reduce the signal/noise performance of the A/D converter.

Power Supply Rejection Ratio

The power supply rejection ratio of the CS5323 is frequency dependent. The rejection for frequencies between dc and f_1 Hz (CLKIN=1.024 MHz) is nearly constant. Above f_1 Hz, the CS5322 digital filter will aid in rejecting interference until the frequencies near CLKIN/21.3 (above 48 kHz for CLKIN=1.024 MHz). Power supply interference above this frequency may cause noise to be modulated into the passband (dc to f_1 Hz), degrading the performance of the A/D.

Power Supply Considerations

The system connection diagram, Figure 17, illustrates the recommended power supply arrangements. The CS5323 has two positive analog supply pins and two negative analog supply pins. Multiple pins are used to minimize the possibility of noise coupling on the chip. All six power supply pins should be decoupled to their respective grounds, with a 0.1 µF capacitor located near the device. The digital supplies are decoupled from the analog supplies with a 10Ω resistors to minimize the effects of digital noise in the converter.

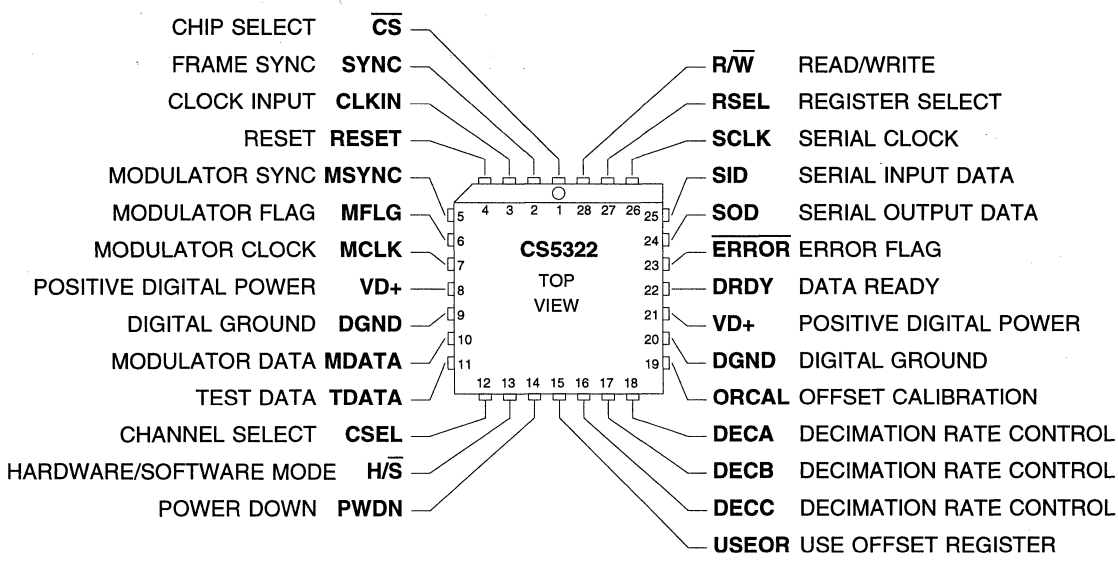
The positive digital power supply of the CS5323 must never exceed either positive analog supply by more than a diode drop, or the CS5323 could experience permanent damage. If separate supplies are used for the analog and digital sections of the chip, care must be taken that the analog supply comes up first at power-up. Additionally, the power supplies to the CS5323 should be active before the reference current generator supplies the IREF input current.

The maximum voltage differential between the positive digital supply of the CS5323 and the positive digital supply of the CS5322 must be less than 0.25V. Operation beyond this con-

straint may result in loss of analog performance in the CS5322 and CS5323 chip set.

Many seismic or sonar systems are battery powered, and utilize dc-dc converters to generate the necessary supply voltages for the system. To minimize the effects of power supply interference, it is desirable to operate the dc-dc converter at a frequency which is rejected by the digital filter.

To achieve maximum performance, the dc-dc converter operating frequency should be located below 48 kHz (see Power Supply Rejection). A synchronous dc-dc converter, whose operating frequency is derived from the 1.024 MHz clock used to drive the CS5322, will minimize the potential for "beat frequencies" appearing in the dc to f_1 Hz passband.



CS5322 PIN DESCRIPTIONS

Power Supplies

VD+ – Positive Digital Power, PIN 8,21

Positive digital supply voltage. Nominally +5 volts.

DGND – Digital Ground, PIN 9,20

Digital ground reference.

Digital Outputs

MCLK – Modulator Clock Output, PIN 7

A CMOS-compatible clock output (nominally 1.024 MHz) that provides the necessary clock for operation of the modulator.

MSYNC – Modulator Sync, PIN 5

The transition from a low to high level on this output will re-initialize the CS5323.

$\overline{\text{ERROR}}$ - Error Flag, PIN 23

This signal is the output of an open pull-up NOR gate with a nominal 100 kΩ pull-up resistor to which the error status data (OVERWRITE error, MFLG error, ACC1 error and ACC2 error) are inputs. When low, it notifies the host processor that an error condition exists. The $\overline{\text{ERROR}}$ signal can be wire OR'd together with other filters' outputs. The value of the internal pull-up resistor is 100 kΩ.

DRDY - Data Ready, PIN 22

When high, data is ready to be shifted out of the serial port data register.

SOD - Serial Output Data, PIN 24

The output coding is 2's complement with the data bits presented MSB first, LSB last. Data changes on the rising edge of SCLK. An internal nominal 100 kΩ pull-up resistor is included.

Digital Inputs

MDATA – Modulator Data, PIN 10

Data will be presented in a one-bit serial data stream at a bit rate of 256 KHz; (CLKIN = 1.024 MHz).

TDATA - Test Data, PIN 11

Input for user test data.

MFLG – Modulator Flag, PIN 6

A transition from a low to high level signals that the CS5323 modulator is unstable due to an over-range on the analog input. A Status Bit will be set in the digital filter indicating an error condition. An internal nominal 100 kΩ pull-down resistor included on the input pin.

RESET - Filter Reset, PIN 4

Performs a hard reset on the chip, all registers and accumulators are cleared. All signals to the device are locked out except CLKIN. The error flags in the Status Register are set to zero and the Data Register and Offset Register are set to zero. The configuration register is set to the values of the corresponding input pins. SYNC must be applied to resume convolutions after RESET deasserts.

CLKIN - Clock Input, PIN 3

A CMOS-Compatible clock input to this pin (nominally 1.024 MHz) provides the necessary clock for operation the modulator and filter.

SYNC - Frame Sync, PIN 2

Conversion synchronization input. This signal synchronizes the start of the filter convolution. More than one SYNC signal can occur with no effect on filter performance, providing the SYNC signals are perfectly timed at intervals equal to the output sample period.

CSEL - Channel Select, PIN 12

When high, information on the TDATA pin is presented to the digital filter. A low causes data on the MDATA input to be presented to the digital filter.

PWDN - Powerdown, PIN 14

Powers down the filter when taken high. Convolution cycles in the digital filter and the MCLK signal are stopped. The registers maintain their data and the serial port remains active. SYNC must be applied to resume convolutions after PWDN deasserts.

DECA - Decimation Rate Control , PIN 18

See Table 3.

DECB - Decimation Rate Control , PIN 17

See Table 3.

DECC - Decimation Rate Control, PIN 16

See Table 3.

H/$\overline{S}$ - Hardware/Software Mode Select, PIN 13

When high, the device pins control device operation; when low, the value entered by a prior configuration write controls device operation.

$\overline{CS}$ - Chip Select, PIN 1

When high, all signal activity on the SID, R/$\overline{W}$ and SCLK pins is ignored. The DRDY and $\overline{ERROR}$ signals indicate the status of the chip's internal operation.

R/$\overline{W}$ - Read/Write, PIN 28

Used in conjunction with $\overline{CS}$ such that when both signals are low, the filter inputs data from the SID pin on the falling edge of SCLK. If $\overline{CS}$ is low and R/$\overline{W}$ is high, the filter outputs data on the SOD pin on the rising edge of SCLK. R/$\overline{W}$ low floats the SOD pin allowing SID and SOD to be tied together, forming a bidirectional serial data bus.

SCLK - Serial Clock, PIN 26

Clock signal generated by host processor to either input data on the SID input pin, or output data on the SOD output pin. For write, data must be valid on the SID pin on the falling edge of SCLK. Data changes on the SOD pin on the rising edge of SCLK.

SID - Serial Data Input, PIN 25

Data bits are presented MSB first, LSB last. Data is latched on the falling edge of SCLK.

RSEL - Register Select, PIN 27

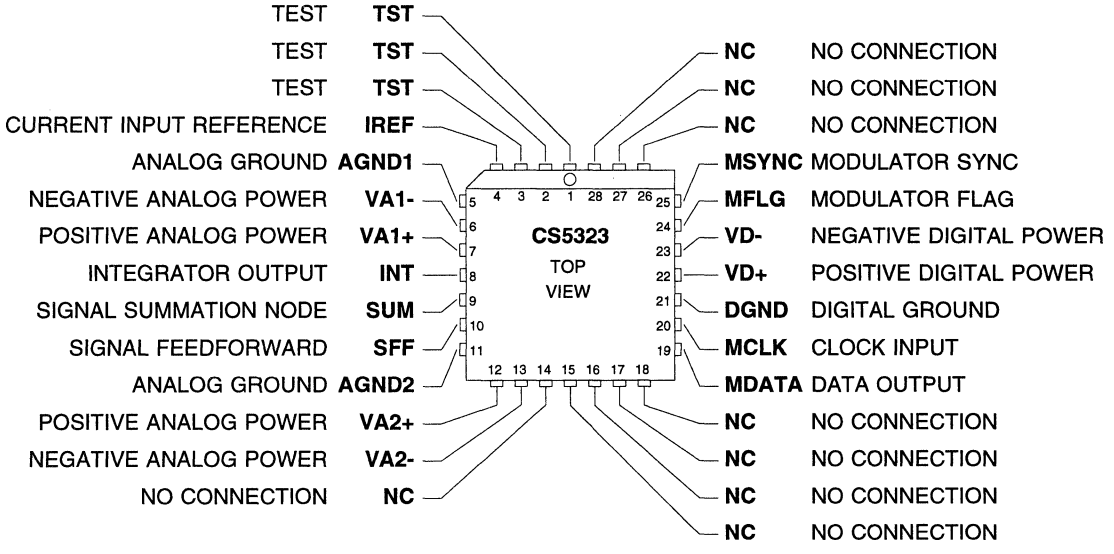
Selects conversion data when high, or status data when low.

USEOR - Use Offset Register, PIN 15

Use offset register value to correct output words when high. Output words will not be offset corrected when low.

ORCAL - Offset Register Calibrate, PIN 19

Initiates an offset calibration cycle when SYNC goes high after ORCAL has been toggled from low to high. The offset value is output on the 57th word following SYNC. Subsequent words will have their offset correction controlled by USEOR.



CS5323 PIN DESCRIPTIONS

Power Supplies

VA1+, VA2+ – Positive Analog Power, PINS 7, 12
Positive analog supply voltage. Nominally +5 Volts.

VA1-, VA2- – Negative Analog Power, PINS 6, 13
Negative analog supply voltage. Nominally -5 Volts.

AGND1, AGND2 – Analog Ground, PINS 5, 11
Analog ground reference.

VD+ – Positive Digital Power, PIN 22
Positive digital supply voltage. Nominally +5 Volts.

VD- – Negative Digital Power, PIN 23
Negative digital supply voltage. Nominally -5 Volts.

DGND – Digital Ground, PIN 21
Digital ground reference.

Analog Inputs

IREF – Current Input Reference Node, PIN 4

This node accepts a 1 mA reference current to set the signal gain of the A/D converter.

SFF – Signal Feedforward, PIN 10

The input signal is fed forward around the integrator input stage by means of this input pin. This maximizes signal performance.

SUM – Signal Summation node, PIN 9

This is the input integrator virtual ground summing junction. The external integrator input resistor and integrating capacitor are connected to this node, along with a 250 µA bias current network.

INT – Integrator Output, PIN 8

Output pin of the input integrator stage. The external integrating capacitor is connected to this pin for proper operation.

Digital Inputs

MCLK – Clock Input, PIN 20

A CMOS-compatible clock input to this pin (nominally 1.024 MHz) provides the necessary clock for operation of the modulator, digital filter and data output portions of the A/D converter.

MSYNC – Modulator Sync, PIN 25

A transition from a low to high level on this input will re-initialize the CS5323. MSYNC resets a divide-by-four counter to align the output bit stream from the CS5323 for proper input to the CS5322.

Digital Outputs

MDATA – Modulator Data Output, PIN 19

Data will be presented in a one-bit serial data stream at a bit rate of 256 kHz.

MFLG – Modulator Flag, PIN 24

A transition from a low to high level signals that the CS5323 modulator is unstable due to an over-range on the analog input. A Status Bit will be set in the digital filter indicating an error condition.

Miscellaneous

TST – Test, PINS 1,2,3

Reserved for production test facility. Should be tied to DGND for normal operation.

NC – No Connection, PINS 14,15,16,17,18,26,27,28

No internal connection. Tie to ground for optimum operation.

PARAMETER DEFINITIONS

Dynamic Range

The ratio of the full-scale (rms) signal to the broadband (rms) noise signal. Broadband noise is measured with the input grounded within the bandwidth of 1 Hz to f_3 Hz. Units in dB.

Signal-to-Distortion

The ratio of the full-scale (rms) signal to the rms sum of all harmonics up to f_3 Hz. Units in dB.

Intermodulation Distortion

The ratio of the rms sum of the two test frequencies (50 and 70 Hz) which are each 6 dB down from full-scale to the rms sum of all intermodulation components within the the bandwidth of dc to f_3 Hz. Units in dB.

Full Scale Error

The ratio of the difference between the value of the voltage reference and analog input voltage to the full scale span (two times the voltage reference value). This ratio is calculated after the effects of offset and the external bias components are removed and the analog input voltage is adjusted. Measurement of this parameter uses the circuitry illustrated in the System Connection Diagram. Units in %.

Full Scale Drift

The change in the Full Scale value with temperature. Units in %/°C.

Offset

The difference between the analog ground and the analog voltage necessary to yield an output code from the CS5323/22 of 000000(H). Measurement of this parameter uses the circuit configuration illustrated in the System Connection Diagram. Units in mV.

Offset Drift

The change in the Offset value with temperature. Measurement of this parameter uses the circuit configuration illustrated in the System Connection Diagram. Units in µV/°C.

Semiconductor Corporation

CDB5323

Evaluation Board for CS5323 & CS5322

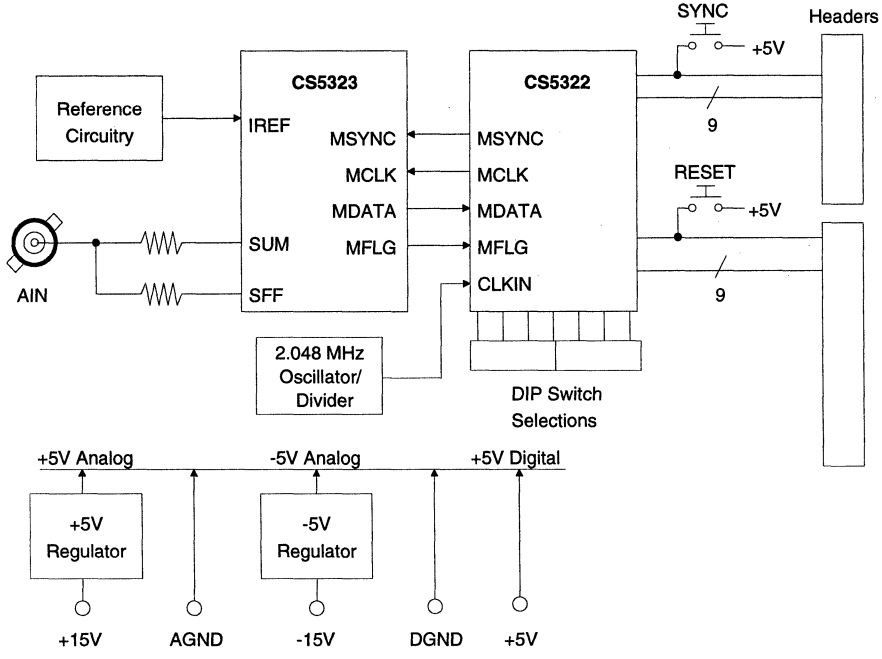
Features

- DIP switch control of all CS5322 logic pins
- Header control of all CS5322 logic pins
- Supports manual operation of RESET and SYNC

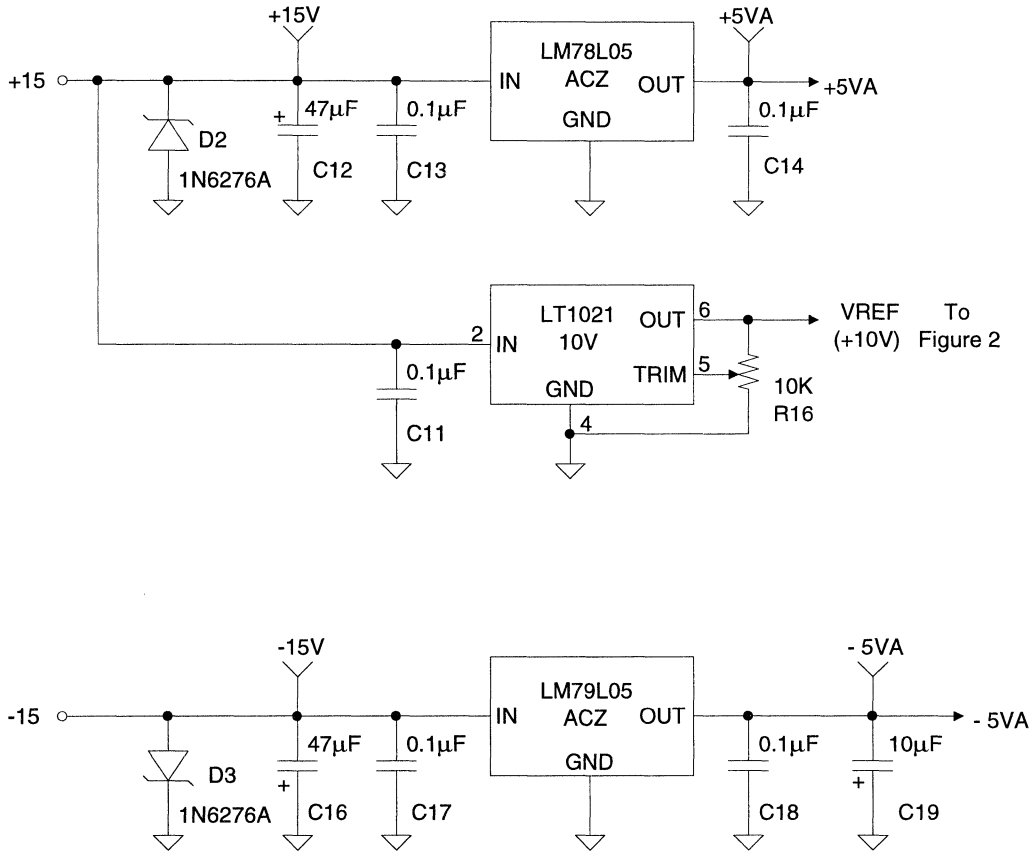
General Description

The CDB5323 is an evaluation board that allows laboratory characterization of the CS5322/CS5323 A/D converter chip-set. The chip-set supports seven different selectable word rates: 4 kHz, 2 kHz, 1 kHz, 500 Hz 250 Hz, 125 Hz and 62.5 Hz. Input to the board is 20 volts peak-to-peak. Output is via header connections to the CS5322 serial interface.

ORDERING INFORMATION: CDB5323



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581



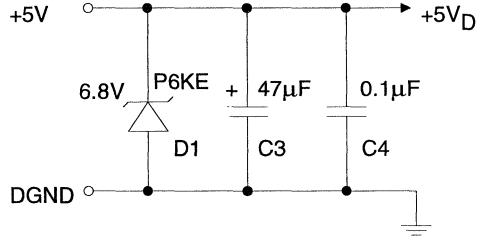


Figure 1. Power Supplies

OVERVIEW

The CDB5323 evaluation board requires three separate power supplies for proper operation. Figure 1 illustrates the power supply connections. The required power supply input voltages consist of +5V, +15V, and -15V. The +5V input supplies the CS5322 filter and logic support devices on the board. The +15V and -15V inputs are regulated down to provide +5V and -5V supplies necessary for the CS5323 modulator. Figure 1 also illustrates the LT1021 10V reference used with the CS5323 modulator.

Figure 2 illustrates the CS5323 modulator circuitry, including the analog BNC input for the test signal source. Figure 3 illustrates the 2.048 MHz oscillator and dual D flip flop clock

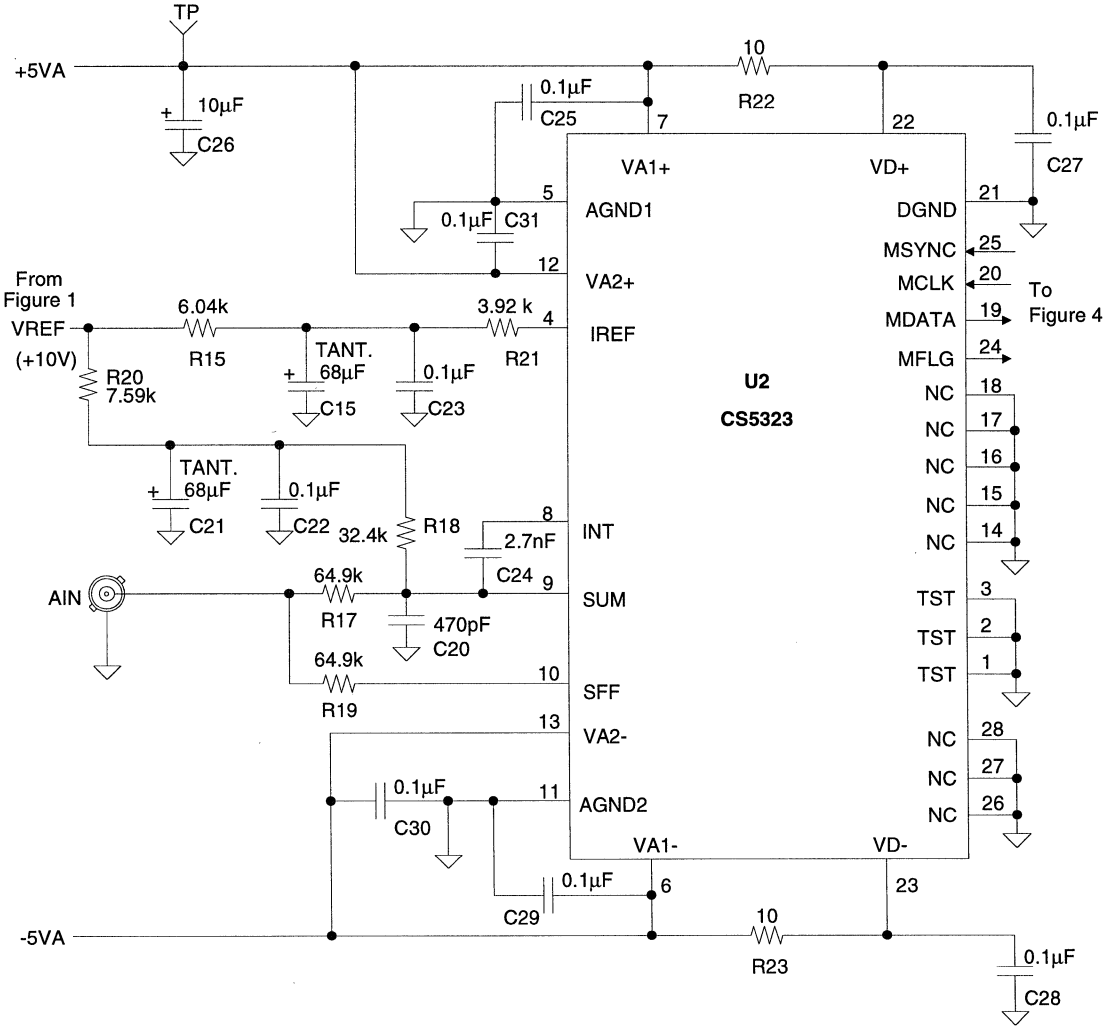


Figure 2. CS5323 Modulator Input Circuitry.

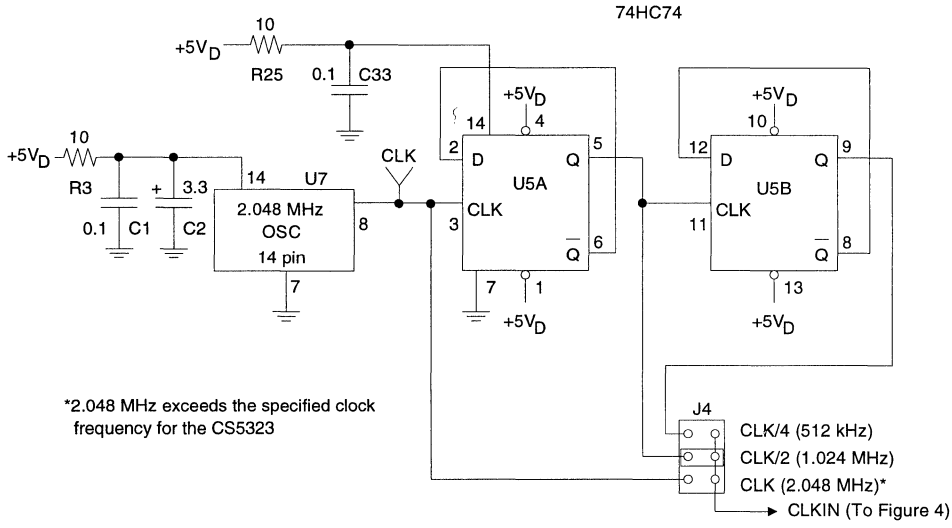


Figure 3. Oscillator / Divider

divider. Note that both the oscillator and the divider are separately decoupled from the +5V supply to reduce clock jitter which can be introduced from noisy supplies. Jumper J4 should be set in the CLK/2 position to source 1.024 MHz to the CS5322 chip for normal operation. If operation from 512 kHz clock is desired, the J4 jumper should be changed to the CLK/4 position. The board can be tested at 512 kHz without modification. In production applications, the CS5323 integrator capacitor (C24) should be doubled to 5.6 nF for 512 kHz operation to achieve optimum performance.

The digital interface pins to the CS5322 filter chip are all available on the header connectors J1, J2, and J3 as shown in Figures 4, and 5. Note that one row of pins on each of the headers is ground. It is advised that any connections made to control lines be done with twisted pair ribbon cable; with each twisted pair containing one signal and one ground connection. This minimizes radiated noise.

CAUTION!

Caution is advised when interfacing the evaluation board to any circuitry powered from another source. For example, when interfacing to a computer I/O card be sure that the evaluation board and the computer are both powered up before connecting to the evaluation board headers. Always disconnect header connections when powering down the board but not the computer. Failure to follow this advice may cause damage to either the computer I/O or to the CS5322, because the computer outputs try to power the CDB5322/23 board.

Tables 1 and 2 illustrate the DIP switch positions of switches S3 and S4. The switch positions with asterisks indicate preferred settings for driving the interface of Figure 6.

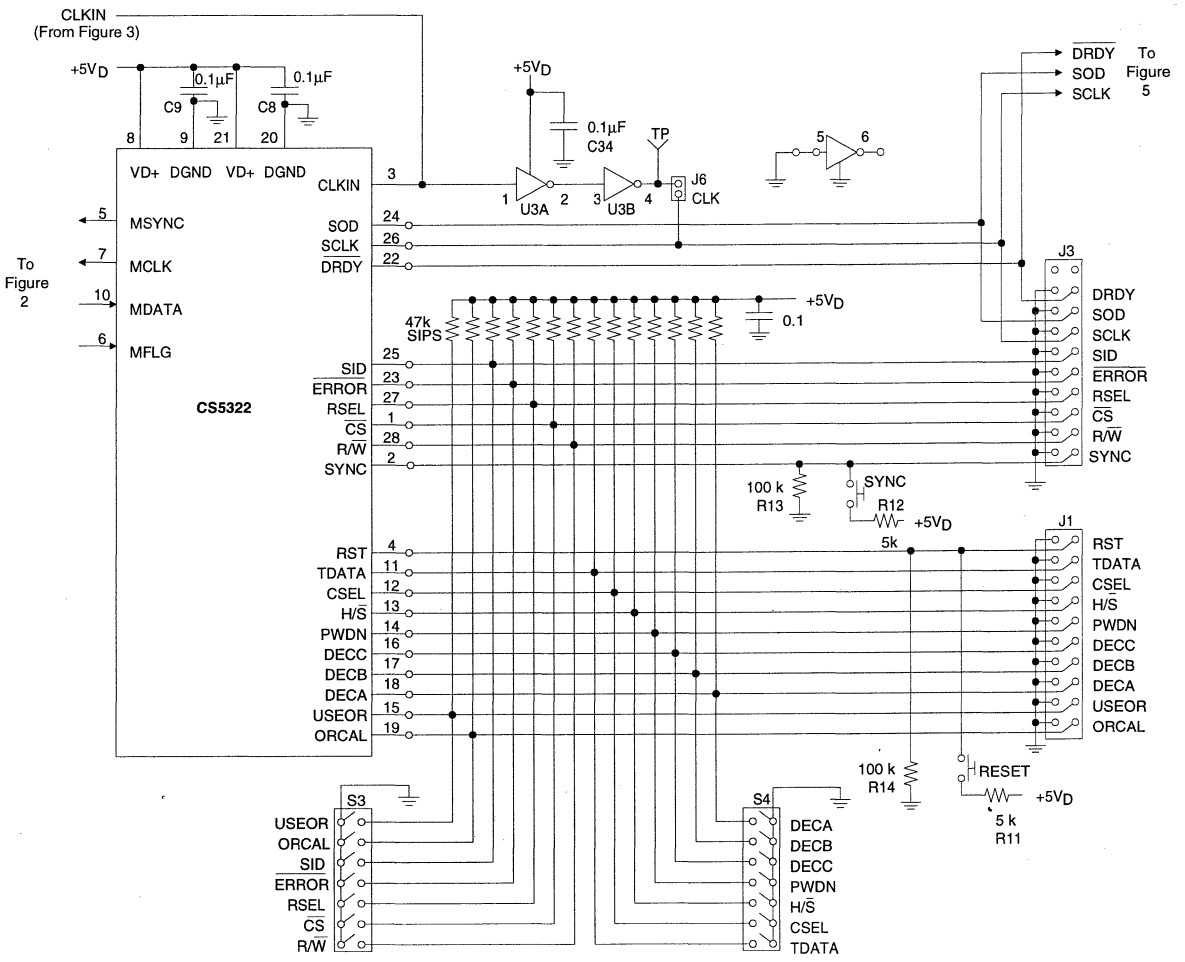


Figure 4. CS5322 Filter Interface

USEOR	ON*	Do not use offset register
	OFF	Use offset register
ORCAL	ON*	Disable offset register calibration
	OFF	Enable offset register calibration
SID	ON	Sets SID to Logic 0
	OFF*	Allows pull-up on SID line
ERR	ON	Sets ERR to logic 0
	OFF*	Allows CS5322 ERROR output
RSEL	ON	Select status register
	OFF*	Select conversion data register
CS	ON*	Chip select active
	OFF	Chip select inactive
R/$\overline{W}$	ON	Enables write mode via SID pin
	OFF*	Enables read mode via SOD pin

OFF = OPEN = 1

*Default to use Figure 6 interface.

Table 1. S3 DIP Switch Selections

DECA	Selection via hardware pins	**ABC**	**Output Word Rate**
DECB		0 0 0	62.5
DECC		1 0 0	125
		0 1 0	250
		1 1 0	500
		0 0 1	1000
		1 0 1	2000
		0 1 1	4000
PWDN	ON*	Normal Operation	
	OFF	Power down active	
H/$\overline{S}$	ON	Selects configuration register for operating mode	
	OFF*	Select hardware pins for operating mode	
CSEL	ON*	Selects MDATA from modulator	
	OFF	Selects TDATA as filter input	
TDATA	ON*	Sets TDATA input to logic 0	
	OFF	Enables TDATA from J1 header	

OFF = OPEN = 1

*Default to use Figure 6 interface.

Table 2. S4 DIP switch selections

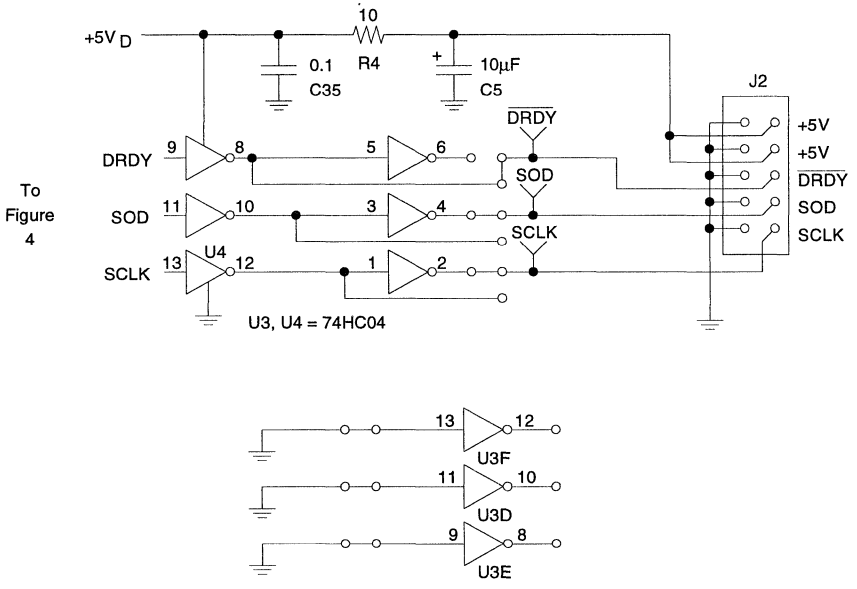


Figure 5. Serial Latch Interface

Figure 5 illustrates the logic used to drive connections at header J2.

By using the signals at header J2, the evaluation board can be set up to output its conversion words into three 74HC595 serial to parallel registers. This provides 24-bit parallel data. Figure 6 illustrates the circuitry which can be interfaced to the J2 connections to provide an isolated digital interface to three 74HC595 registers (the circuitry of Figure 6 is not provided on the board). Signals from connector J2 (+5 volts, GND, SCLK, SOD, and $\overline{\text{DRDY}}$) are interfaced to the GND1 side of the opto-isolated interface. The 74HC595 registers require SCLK rising to latch data bits and DRDY rising to parallel latch data. Jumpers must be placed to select the proper phase of these signals as the CS5322 provides data bits to be latched by the falling edge of SCLK and causes DRDY to fall when the last data bit is clocked out. A flip-flop is used to delay DRDY by one-half SCLK cycle before it is used to latch the parallel latch. Jumper J6 (CLK) is used to connect the 1.024 MHz clock as the SCLK signal to clock serial data from the chip. A second isolated +5 volts should be provided to the GND2 side of the interface. Opto-isolation eliminates any ground loop between the board and the computer interface.

The CS5322 filter should be set up for hardware mode (H/$\overline{\text{S}}$ on switch S4 open). DIP switch S4 can then be used to select the desired output word rate. After the selection on the DECA, DECB, and DECC positions of the S4 DIP switch, the S2 RESET switch must be activated, followed by the S1 SYNC switch (unless these signals are controlled via the J1 and J3 header signals).

Figure 7 illustrates the component layout of the board while figures 8 and 9 illustrate the board layout (not to scale).

Using the Evaluation Board

Connect the appropriate power supplies to the binding posts of the board. Twist the +5V digital supply lead with the digital ground lead from the board to the supply. Also twist the supply leads for the analog voltages. Use a high quality power supply which is low in noise and line frequency(50/60 Hz) interference.

Power up the supplies. Then connect a coaxial cable from the analog BNC to the signal source. Note that the performance of the A/D converter chip set will exceed the capability of most signal generators, especially with respect to noise and line frequency interference.

Once power has been applied to the board, connect the ribbon cable to the appropriate headers (J1, J2, and/or J3). The reset and the sync signals to the CS5322 must be applied before normal operation can commence. This can be done by using the S2 RESET switch and the S1 SYNC switch or by interfacing to these signals via the J1 and J3 headers.

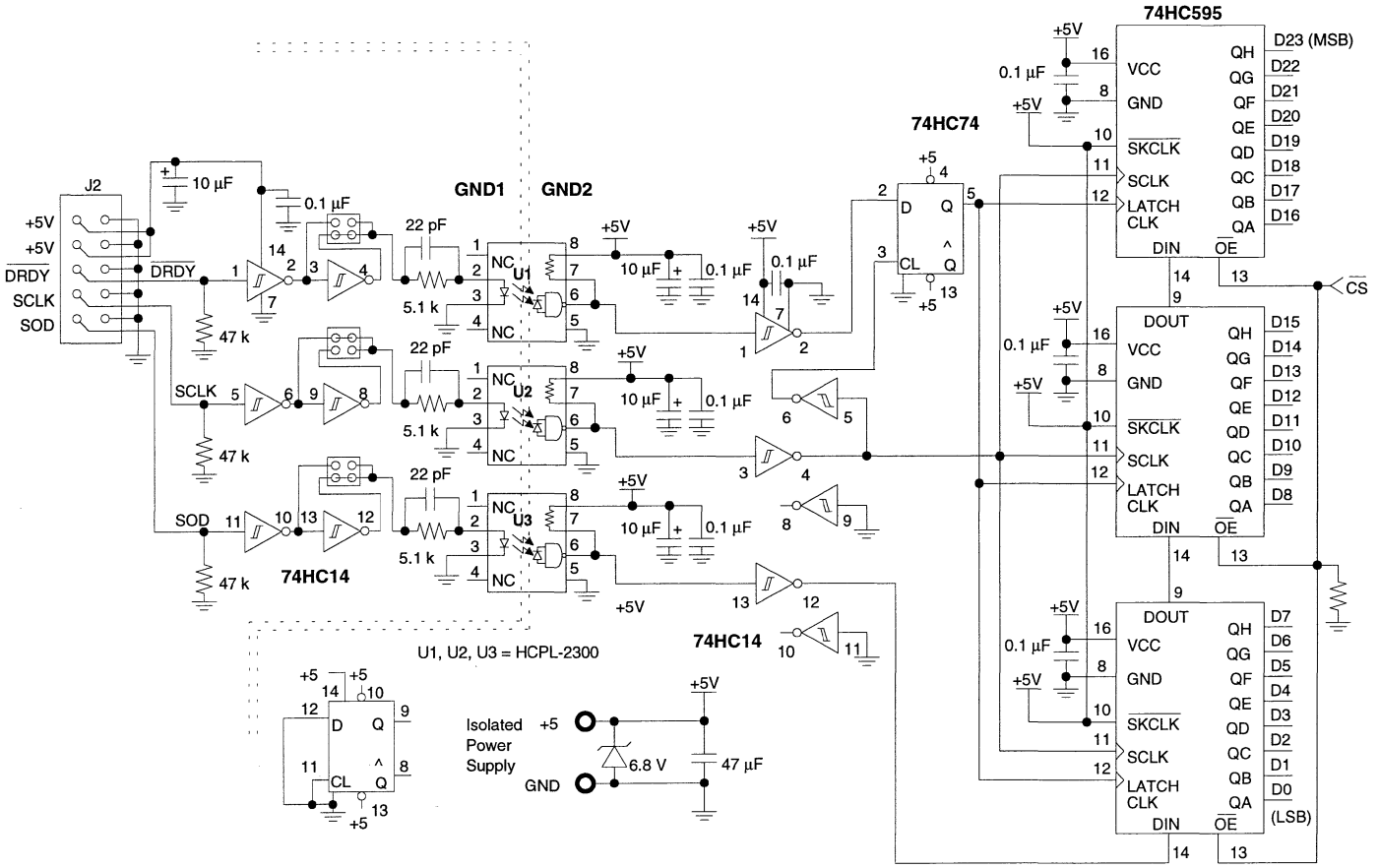


Figure 6. Suggested Opto-coupled Interface Between A/D and Serial-to-parallel Registers (Not Provided)

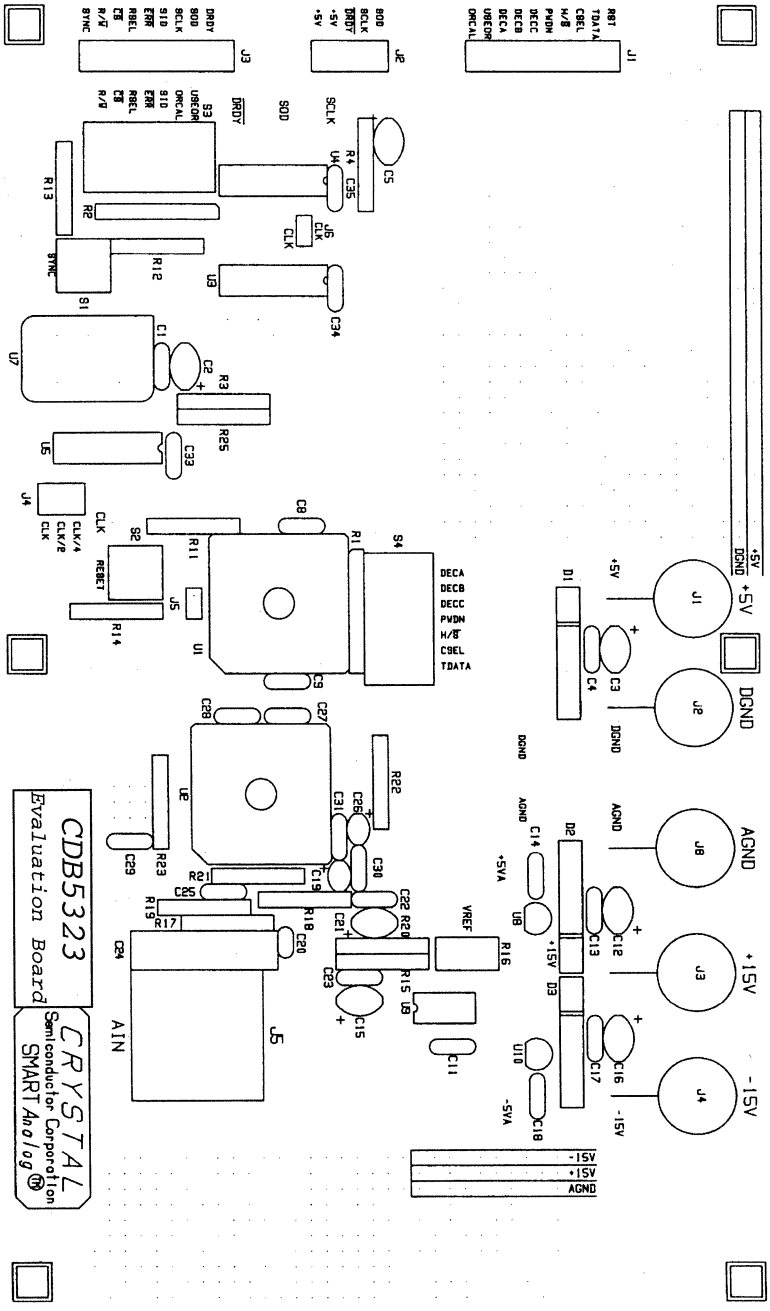


Figure 7. CDB5323 Component Layout (Not to Scale)

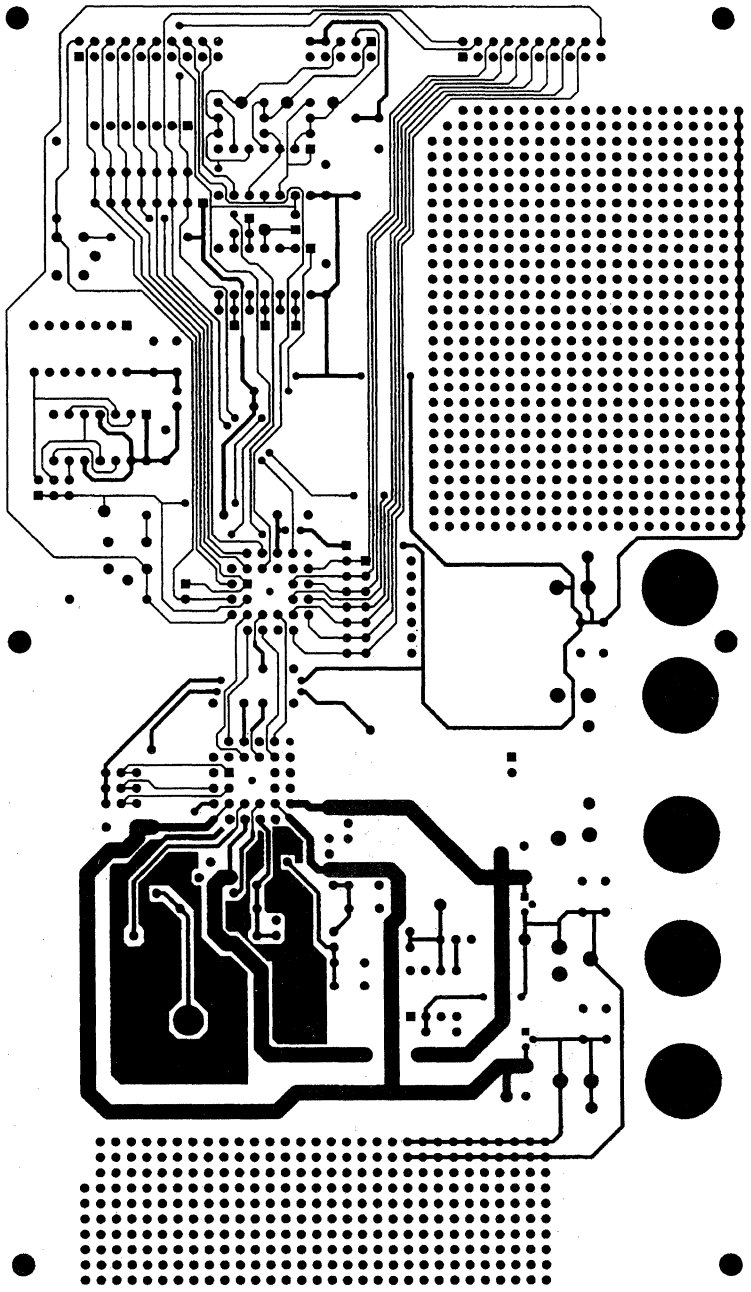


Figure 8. CDB5323 Solder Trace Layer (Not to Scale)

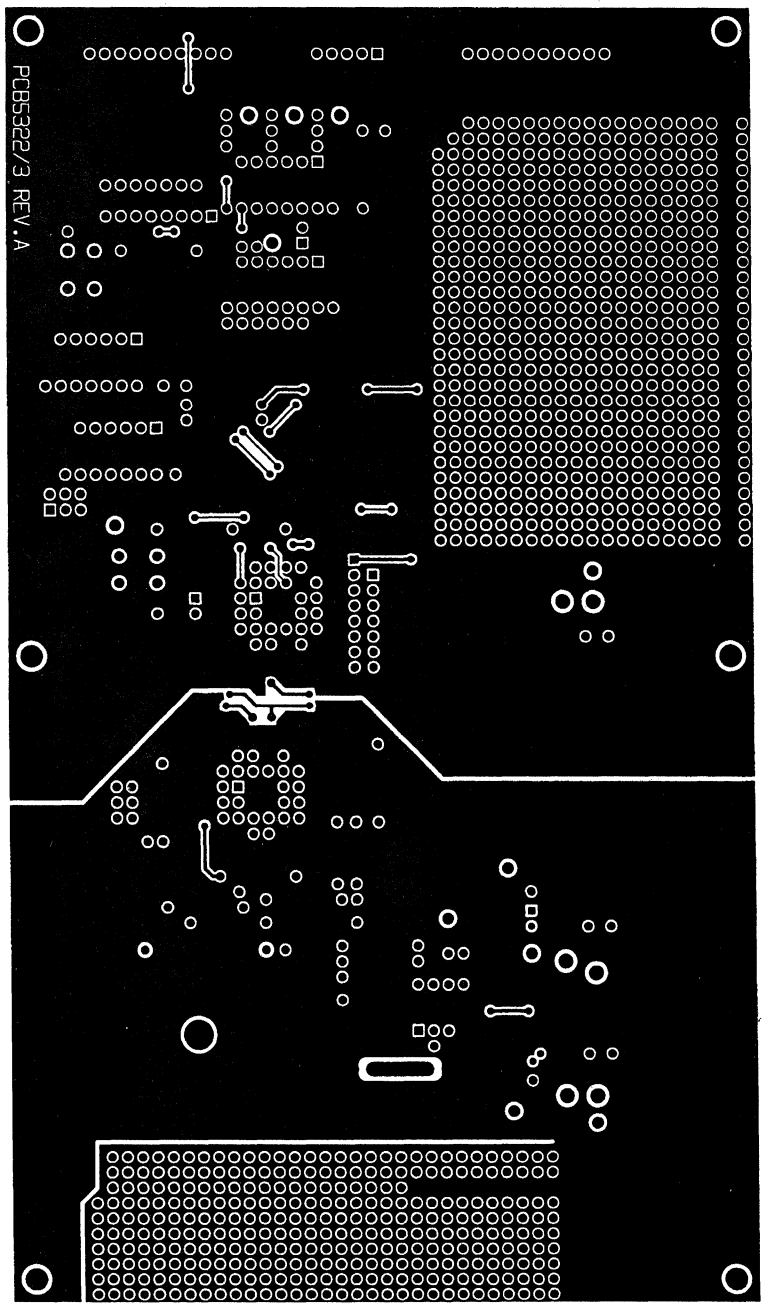


Figure 9. CDB5323 Ground Plane Layer (Not to Scale)

Semiconductor Corporation

CS5324

120 dB, 500 Hz Oversampling A/D Converter

Features

- Monolithic CMOS A/D converter
- 120dB Dynamic Range
- dc-500 Hz Bandwidth
- 110 dB Total Harmonic Distortion
- Internal Track-and-Hold Amplifier
- Delta-Sigma Architecture
  - —256X Oversampling
  - —Linear Phase Digital Filter
  - —Output Word Rate 32 kHz
- Low Power Dissipation: 150 mW
- Evaluation Board Available

General Description

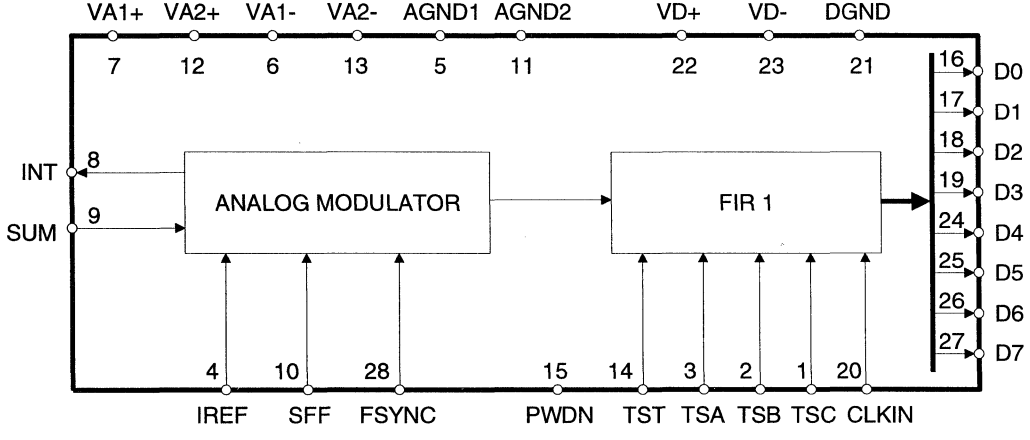
The CS5324 analog to digital converter is a unique, very high resolution A/D converter intended for geophysical and sonar applications. It is a complete analog front end to a Digital Signal Processor and provides the DSP with a low distortion digital input suitable for precision signal analysis. The CS5324 performs sampling, A/D conversion, and anti-alias filtering.

The CS5324 uses delta-sigma modulation to produce highly accurate conversions. The device oversamples at 256X, virtually eliminating the need for external anti-aliasing filters. An on-chip linear-phase FIR digital filter decimates the output to a 32 kHz output word rate. Data is transmitted to the DSP as two, 8-bit bytes. An additional FIR filter in the DSP further decimates the signal to achieve 120 dB dynamic range over 500 Hz bandwidth with signal-to-distortion of 110 dB.

The CMOS design of the CS5324 ensures high reliability and power dissipation of less than 180 mW.

ORDERING INFORMATION:

CS5324-BL -40° to +85°C 28-pin PLCC



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

ANALOG CHARACTERISTICS (T_A= T_{min} to T_{max} ; VA-=-5V; VA+= 5V; AGND=0V; CLKIN=1.024 MHz Device is connected as shown in Figure 1, the System Connection Diagram. Output data is further processed using off-chip filtering described in Appendix 1.)

Parameter*		Symbol	Min	Typ	Max	Units
Specified Temperature Range			-40	-	+85	°C
Dynamic Performance						
Dynamic Range		DR	116	120	-	dB
Signal-to-Distortion	(Note 1)	SDR	100	110	-	dB
Intermodulation Distortion	(Note 2)		-	110	-	dB
dc Accuracy						
Full Scale Error	(Note 3)		-	-	2	%
Full Scale Drift	(Note 3, 4)		-	0.003	0.006	%/°C
Offset	(Note 3)		-	-	250	mV
Offset Drift	(Note 3, 4)		-	500	750	µV/°C
Input Characteristics						
Input Signal Frequencies	(Note 5)	BW	dc	-	500	Hz
Input Voltage Range	(Note 6)	Vin	-10.0	-	+10.0	V
Power Supplies						
DC Power Supply Currents	(Note 7)					
Positive Supplies			-	12.5	18	mA
Negative Supplies			-	14.5	18	mA
Power Dissipation	(Note 7)					
PWDN Low			-	150	180	mW
PWDN High			-	5	10	mW
Power Supply Rejection						
(dc to 500 Hz) VA+	(Note 8)		-	55	-	dB
VA-			-	45	-	dB
VD+			-	48	-	dB
VD-			-	38	-	dB
(500 Hz to 128 kHz) VA+	(Note 9)		-	60	-	dB
VA-			-	60	-	dB
VD+			-	50	-	dB
VD-			-	55	-	dB

Notes:
1. Tested with full scale input signal of 50 Hz.
2. Tested with input signals of 50 Hz and 90 Hz, each 6 dB down from full scale.
3. Specification is for the parameter over the specified temperature range and is for the CS5324 device only. It does not include the effects of external components.
4. Drift specifications are guaranteed by design and characterization.
5. The upper bandwidth limit is determined by the off-chip digital filter.
6. This input voltage range is for the configuration depicted in Figure 1, the System Connection Diagram.
7. All outputs unloaded. All logic inputs forced to VA+ or GND.
8. Tested with a 100 mVp-p 120 Hz sine wave applied separately to each supply (VA1 and VA2 are considered as one input for this test).
9. Tested with a 100 mVp-p 120 kHz sine wave applied separately to each supply (VA1 and VA2 are considered as one input for this test).

* Refer to Parameter Definitions (immediately following pin descriptions at the end of this data sheet).

Specifications are subject to change without notice.

SWITCHING CHARACTERISTICS (T_A= T_{min} to T_{max} ; VA+,VD+=5V±5%; VA-, VD- =-5V±5%; Inputs: Logic 0 = 0V Logic 1 = VD+; C_L=50pF. See Note 10.)

Parameter			Symbol	Min	Typ	Max	Units
CLKIN Frequency		(Note 11)	f_c	0.9	1.024	1.1	MHz
CLKIN Duty Cycle				40	-	60	%
CLKIN Jitter				-	-	5	ps
Rise Times:	Any Digital Input Any Digital Output	(Note 12)	t_{rise}	- -	- 50	1.0 200	µs ns
Fall Times:	Any Digital Input Any Digital Output	(Note 12)	t_{fall}	- -	- 50	1.0 200	µs ns
CLKIN Rising Edge to FSYNC Rising		(Note 13)	t_{cf}	70	-	-	ns
FSYNC Rising to CLKIN Falling Edge			t_{fc}	150	-	-	ns
Output Data Delay: CLKIN Rising to Valid Data			t_{dd}	-	200	250	ns
Output Float Delay: CLKIN Rising to Hi-Z			t_{fd}	-	150	250	ns

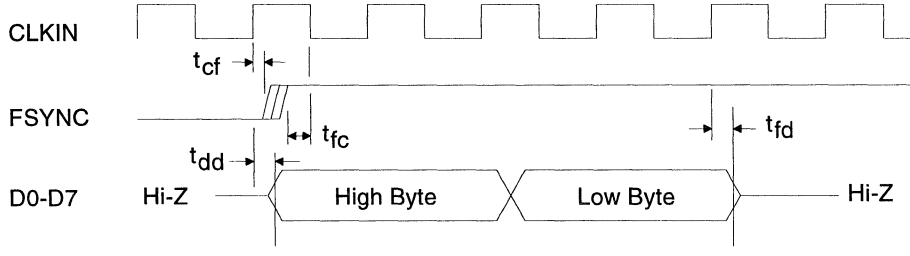
Notes: 10. Guaranteed by design, characterization and/or test.
11. If CLKIN is removed the device will enter the power down mode.
12. Excludes CLKIN input. CLKIN should be driven with a signal having rise and fall times of 25ns or faster.
13. Only the rising edge of FSYNC relative to CLKIN is used to synchronize the device. FSYNC can return low at any time as long as it remains high for at least one CLKIN cycle.

DIGITAL CHARACTERISTICS (T_A= T_{min} to T_{max} ; VA+,VD+ = 5V±5%; VA-,VD- = -5V±5%)

All measurements below are performed under static conditions.

Parameter			Symbol	Min	Typ	Max	Units
High-Level Input Voltage			V_{IH}	(VD+)-1.0V	-	-	V
Low-Level Input Voltage			V_{IL}	-	-	1.0	V
High-Level Output Voltage	I_{OUT} = -600 µA	(Note 14)	V_{OH}	(VD+)-0.4V	-	-	V
Low-Level Output Voltage	I_{OUT} = 800 µA	(Note 14)	V_{OL}	-	-	0.4	V
Input Leakage Current			I_{LKG}	-	-	±10	µA
Tri-State Leakage Current			I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance			C_{OUT}	-	9	-	pF

Notes: 14. The device is designed for low current output drive to minimize induced noise. CMOS interfacing is highly recommended.



Digital Timing Relationships

RECOMMENDED OPERATING CONDITIONS (DGND=0V; AGND=0V. All voltages measured with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Supply						
	Positive Analog	VA+	4.75	5.0	5.25	V
	Negative Analog	VA-	-4.75	-5.0	-5.25	V
	Positive Digital	VD+	4.75	5.0	5.25	V
	Negative Digital	VD-	-4.75	-5.0	-5.25	V

ABSOLUTE MAXIMUM RATINGS (DGND=0V; AGND=OV. All voltages measured with respect to ground.)

Parameter			Symbol	Min	Max	Units
DC Supply	Positive Digital		VD+	-0.3	(VA+)+0.3	V
	Negative Digital		VD-	0.3	-6.0	V
	Positive Analog		VA+	-0.3	6.0	V
	Negative Analog		VA-	0.3	-6.0	V
Input Current, Any Pin Except supplies		(Note 15)	I_{in}	-	±10	mA
Digital Input Voltage			V_{IND}	-0.3	(VA+)+0.3	V
Ambient Operating Temperature			T_A	-55	125	°C
Storage Temperature			T_{stg}	-65	150	°C

Note: 15. Transient currents up to 100 mA will not cause SCR latch-up.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

General Description

The CS5324 is a monolithic CMOS A/D converter designed specifically for very high resolution measurement of signals between dc and 500 Hz. The device consists of a fourth-order delta-sigma modulator followed by an on-chip digital decimation filter.

The modulator of the CS5324 samples the analog input signal at a 256X oversampling rate. This high oversampling rate, along with subsequent digital filtering, enables the CS5324 to achieve a dynamic range which exceeds 120dB. To achieve optimum performance, the CS5324 uses off-chip circuitry to develop the reference and operating currents necessary to set the gain and offset of the modulator portion of the A/D converter. Discrete components are also used for the first stage integrator input resistor and integration capacitor.

The CS5324 performs conversions continuously and outputs twelve data bits for further data decimation by an off-chip digital filter. A separate DSP chip can be utilized to perform the off-chip filtering. A single DSP chip can perform the filter function for several CS5324 devices. For this reason, the CS5324 was designed to output its data in a simple time-division multiplexing (TDM) format. This TDM architecture allows up to eight CS5324 devices to share the same data bus.

Theory of Operation

The CS5324 utilizes a fourth order oversampling delta-sigma architecture to achieve high-resolution A/D conversion. The converter consists of an analog modulator, along with an on-chip digital decimation filter. The modulator consists of a 1-bit A/D converter embedded in a negative feedback loop. The first stage of the fourth order modulator uses discrete components external to the chip to maximize signal performance relative to noise.

The modulator samples at 256 kHz (CLKIN = 1.024 MHz) which is 256X oversampling above two times the maximum signal frequency of 500 Hz. The modulator output is followed by a decimate by 8, fourth-order (sinx)/x filter. The result from this filter is a 12-bit word which is output from the chip at a 32 kHz rate. The 12-bit data is then further filtered by means of an off-chip digital filter. The off-chip filter can be implemented by either a DSP chip or an ASIC designed for this purpose. The exact characteristics of the on-chip filter and some recommended off-chip digital filters are discussed under the Filter Characteristics section of the data sheet. Upon reduction with the off-chip filtering, the data results in resolution which exceeds 20-bits. The final result yields a dynamic range exceeding 120 dB.

The architecture of the CS5324 was chosen to maximize performance. The input integrator uses off-chip discrete components. The chip is designed to use a current-source type reference, rather than a voltage source to minimize noise. In addition, the amount of on-chip digital filtering is minimized to reduce the possibility of the digital noise of the filter coupling into the analog sections of the chip. Configuring the chip to use additional off-chip digital filtering also allows the user maximum flexibility in implementing a filter appropriate to his system requirements.

Signal Input and Current Reference

The CS5324 uses a number of external discrete components to achieve maximum performance. Figure 1 illustrates the recommended circuit configuration for the current reference components and for the signal input components.

The CS5324 is designed to use a current reference of 2 mA into the IREF pin. A current reference rather than a voltage reference was chosen to achieve better noise performance. For optimum performance the dc source impedance at

the IREF pin should be approximately 5 kΩ. This calls for a 10 volt source driving the 5 kΩ (R_6+R_7) resistor to achieve the desired 2 mA current source. The IREF input sets the full scale gain of the A/D converter.

To properly bias the input integrator to a midrange operating point, a current source 1/4 the size of the IREF input current must be sourced into the integrator summing junction at the SUM pin. This requires a 20 kΩ resistance (R4+R5) be placed from the 10 V reference to the SUM pin.

Both the 2 mA IREF current and the 500 µA sources have capacitive filtering to aid in reducing the broadband current noise from the voltage reference. These capacitors should be of quality construction. Particular attention should be paid

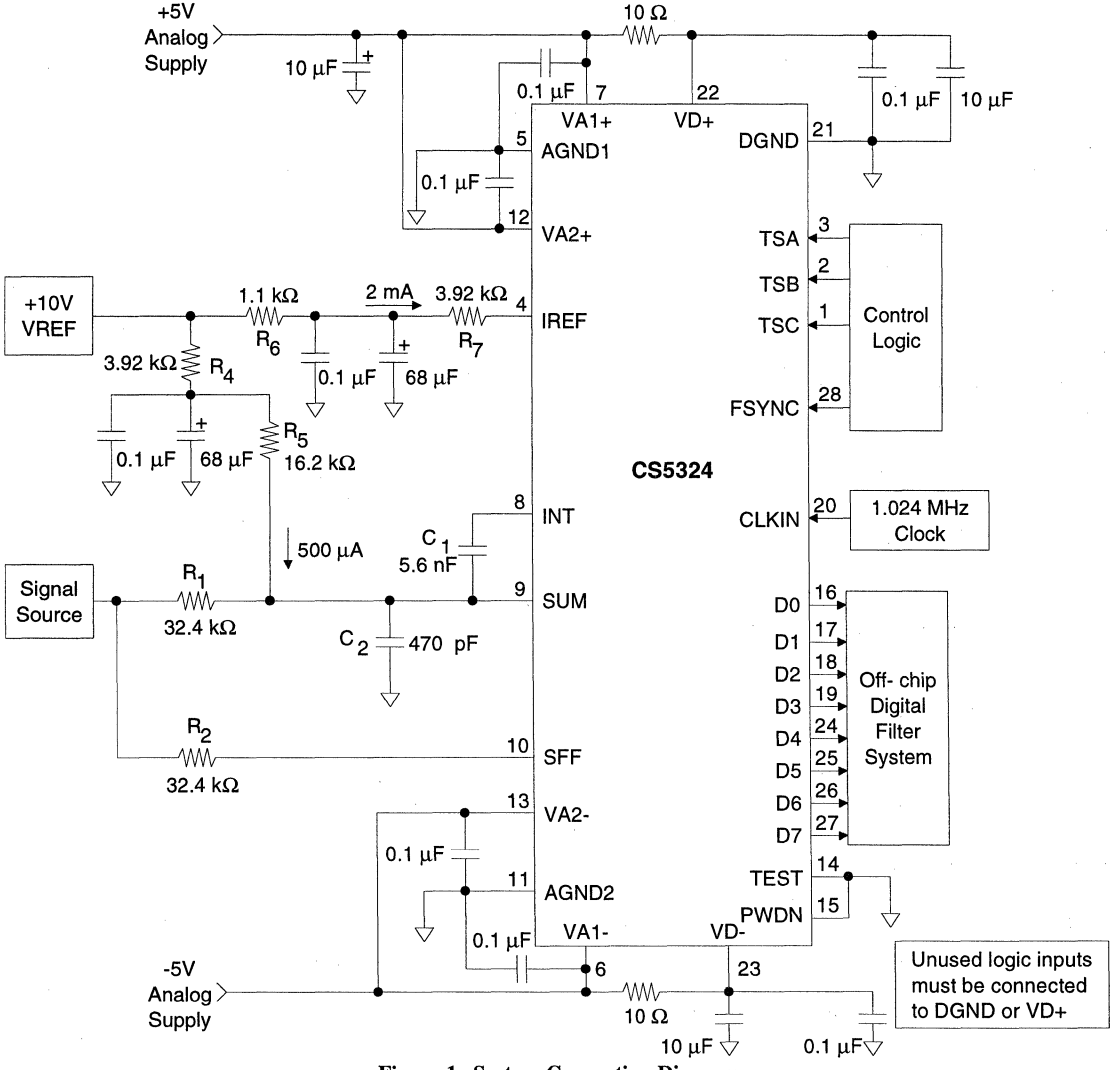


Figure 1. System Connection Diagram

to leakage current variation over the desired operating temperature, as this leakage will affect the system gain.

The signal input pin (SUM) of the CS5324 is the summing junction of the input integrator stage. This integrator is designed to use an external input resistor (R_1) and integrating capacitor (C_1). In addition, a capacitor (C_2) is required at this node for proper phase compensation. The size of the input resistor (R_1) is determined by the magnitude of the signal current. With a maximum input voltage into the resistor, the integrator input current must be set equal to approximately 0.15 the current value injected into the IREF pin. With a 2 mA IREF current, the full scale signal current should be about 300 µA. Additionally, to minimize current noise into the summing junction, the value of the effective input resistance should be above 8 kΩ. Using a 32.4 kΩ resistor for R_1 sets the full scale input voltage into the integrating resistor to a value near 10 volts. The input signal then spans 20 V_{p-p}.

Once the integrator input resistor is chosen, the integrator capacitor can be determined. The resistor and capacitor combination should yield a frequency ($f= 1/(2\pi R_1C_1)$) between 800 and 900 Hz to achieve maximum performance. This yields a capacitor value near 5.6 nF. The capacitor should be chosen for minimum leakage, minimum dielectric absorption, and minimum voltage coefficient of capacitance. While a teflon foilwrap capacitor is preferred, high quality film capacitors may be acceptable in many applications.

The CS5324 has a second signal input pin called the Signal Feedforward (SFF) pin. The signal into this pin bypasses the input stage of the input integrator, improving signal performance in the passband. The resistor (R_2) used at this input should be identical in value and performance characteristics to the input resistor (R_1).

2

Digital Output and Data Format

For proper operation the CS5324 must be provided with a CMOS-compatible clock into the CLKIN pin. The normal operating frequency is 1.024 MHz. This clock determines the input sample rate and the output word rate of the converter. The sample rate is CLKIN/4 while the output word rate is at CLKIN/32.

The CS5324 will compute a 12-bit output word at a 32 kHz rate (CLKIN = 1.024 MHz). The data is output from Data Output pins D7-D0 in the form of two eight bit bytes. The first byte is the high order byte with the MSB in the D7 position. The second 8-bit byte is the low order byte, and includes three status bits and an unused bit. The data is in two's complement format. Figure 2 illustrates the format of the output data.

For 12-bit two's complement data the codes range from -2048 to +2047. The output codes from the CS5324 will range from approximately -1280 to +1280 for a full scale sine wave input into the converter as shown in Table 1. There may be typically ±50 codes of noise (p-p) on the data in the 12-bit data output. Off-chip digital filtering is required to achieve the full dynamic range capability of the CS5324.

	D7	D6	D5	D4	D3	D2	D1	D0
Hi Byte	B11	B10	B9	B8	B7	B6	B5	B4
Lo Byte	B3	B2	B1	B0	0	OF	UF	ORST

Data is 2's complement with B11 as sign bit

Figure 2. Output Data Format

Input Signal	Output Code
approx. +16V	0111 1111 1111
+F.S. - 1.5 LSB (approx. +10V)	0101 0000 0000
0V	0000 0000 0000
-F.S. + 0.5 LSB (approx. -10V)	1011 0000 0000
approx. -16V	1000 0000 0000

Notes: 1. Output codes from the on-chip digital filter will typically exhibit ±50 LSB's of noise (p-p).
2. Table depicts output codes for circuit configuration of Figure 1.

Table 1. Output Coding

Status Bits

Three status bits are output from the CS5324. The three status bits are overflow, underflow, and oscillation reset. The overflow and underflow status bits indicate whenever the digital filter accumulator results in an overflow or underflow condition. With the present on-chip digital filter, the underflow condition will never occur. The overflow bit will go high indicating an accumulator overflow only if the input signal to the converter exceeds positive full scale by approximately 1.6X. Upon overflow, the accumulator will contain the value +2047 (or 2048 after underflow). The oscillation reset status bit indicates that output data may be in error. An oscillation detection circuit monitors the modulator loop to see if it is operating within its stable operating range. If the modulator is operating outside its normal operating range the output data may be corrupted. The ORST status bit may go high as a result of power-up, or, if the input signal exceeds the specified full scale input value. If ORST does occur, it will remain high for a total of four update cycles (of 32 kHz) to the output port, while the modulator and the digital filter are reset. Once ORST goes back low, output data will not be valid until the modulator and the digital filter(s) settle.

Initialization and Output Data Sequencing

The CS5324 updates its output register at a 32 kHz rate (CLKIN = 1.024 MHz). Between updates 32 CLKIN cycles occur. The CS5324 is designed such that eight data output time slots occur during these 32 CLKIN cycles. Each time slot lasts for 4 CLKIN cycles. The CS5324 is designed to allow eight devices to share the same 8-bit data bus when each device is set-up to output its data in an individual time slot. The exact time the CS5324 will output data is determined by the TSA, TSB, TSC, and FSYNC inputs. After power is applied to the devices, the FSYNC input must be brought high. When FSYNC is brought high (within the required timing specifications), each chip will be assigned to a data output time slot according to the logic levels of its TSA, TSB, and TSC inputs. Table 2 tabulates the decoding of these inputs.

If all the CS5324s in the system are initialized with the same FSYNC signal, they will all compute filter results in phase with each other and update their output registers at the same time. Only the time slot in which the data is output from the devices is different.

The FSYNC signal used to initialize the CS5324 need only be activated once after power up. In some systems, it may be preferable to have this

TSA	TSB	TSC	Time Slot
0	0	0	TS0
0	0	1	TS1
0	1	0	TS2
0	1	1	TS3
1	0	0	TS4
1	0	1	TS5
1	1	0	TS6
1	1	1	TS7

Table 2. Time - Slot Decoding

signal occur every 32 CLKIN cycles. Only the occurrence of the rising edge of FSYNC is significant in determining the system initialization. Figure 3 illustrates a system configuration using multiple CS5324s interfaced to the same DSP chip.

Four cycles of CLKIN occur during each time slot. During the time slot designated for a CS5324 to output its data, the high-order byte will be output for the first two CLKIN cycles of the time slot. The second byte will be output during the last two CLKIN cycles of the period.

If four or less CS5324's share the same data bus, it is preferable to use alternate time slots (i.e. TS0, TS2, TS4, TS6) to minimize the possibility of bus contention problems. Slight timing differences between chips may result in timing overlap if adjacent time slots are used.

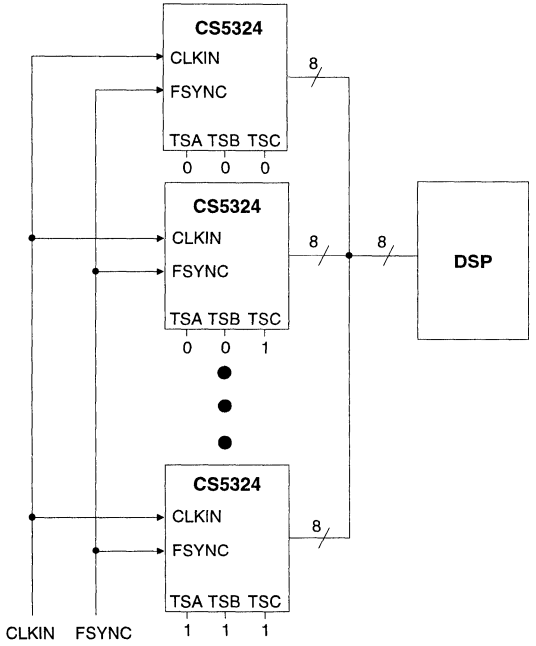


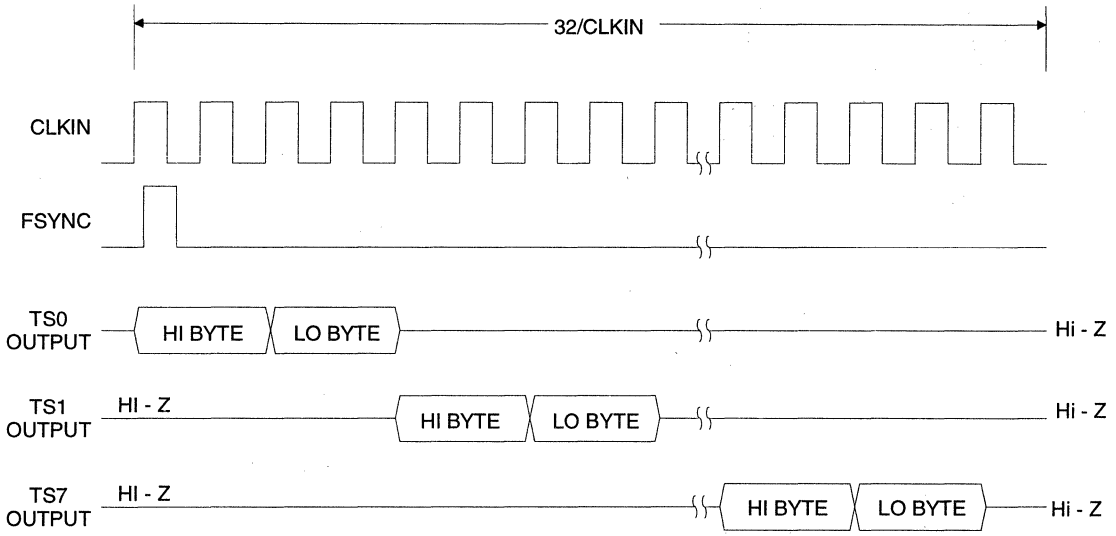
Figure 3. Multiple CS5324 to DSP Interface.

Filter Characteristics

The CS5324 utilizes a fourth-order delta-sigma modulator which has superb linearity. The full capability of the A/D conversion block can be obtained with an appropriate digital filter. Many applications, (seismic applications in particular) require the A/D conversion function to accurately reproduce the pulse shape of the input signal waveform, not just the spectral content. To accurately digitize the shape of the input signal requires a linear phase response in the signal processing system. Any non-linearities in the phase response of the signal processing system will corrupt the true waveshape information. For this reason, the design of the digital filtering to be used with the CS5324 should include particular attention to the phase characteristics of the filter function.

While the on-chip filter is fixed in its characteristics, the off-chip filter will be defined by the system requirements of the particular application. A low pass filter specification to be used with the CS5324 will include the following parameters: Passband ripple (or flatness); group delay or phase characteristics; transition band rolloff; stop band rejection; and filter complexity. All of these parameters are interrelated in any given filter design. There is no one particular solution to be used with the CS5324.

The CS5324 samples the input signal at 256 kHz (CLKIN = 1.024 MHz). With a signal bandwidth of 500 Hz, the output data rate from the A/D system (including the off-chip digital filtering) need only be 1 kHz to adequately represent the input signal. For this reason, it is desirable to decimate the 256 kHz sample rate to 1 kHz. To accomplish this while also providing the necessary low-pass filtering, three stages of filtering are utilized. The first of these is the on-chip filter. This filter is a decimate-by-8 function, and reduces the output word rate from the CS5324 chip to 32 kHz. Two additional filtering stages are to be implemented off-chip with either a DSP, a dedicated ASIC, or another computing device. The first off-chip stage



Note: Up to eight A/D converters can share the same digital output bus as long as each converter is assigned to put out its data in a different time slot with respect to all other converters on the bus.

Figure 4. Data Output Sequence for Multiple CS5324s.

is a decimate-by-8 function, which reduces the output word rate to 4 kHz. The last stage will be a decimate-by-4 function, which will reduce the word rate to 1 kHz. The filter stages are designed so that the first filter has zeroes in its transfer function, such that it rejects the aliased components, due to the first decimate-by-8. The second stage has zeroes such that it rejects the aliased components due to the second decimate-by-8. Neither the on-chip filter, nor the first off-chip stage really affect the passband, but instead, these two stages reduce the output data rate, while at the same time providing anti-alias filtering. The third stage provides the low-pass filtering function.

The CS5324 includes an on-chip 29th-order linear phase FIR (finite-impulse-response) filter and decimator. The response of this filter is illustrated in Figure 5. The filter coefficients are listed in Table 3. The filter performs a fourth-order sinc function, and has a monotonic rolloff in the passband. Attenuation at 500 Hz is 0.0137 dB. The minimum attenuation in the (n x 32 kHz) +/-500 Hz bands is 147 dB. The data output from the on-chip filter has been described in the Data Output and Data Format section above. Data is output at a 32 kHz rate.

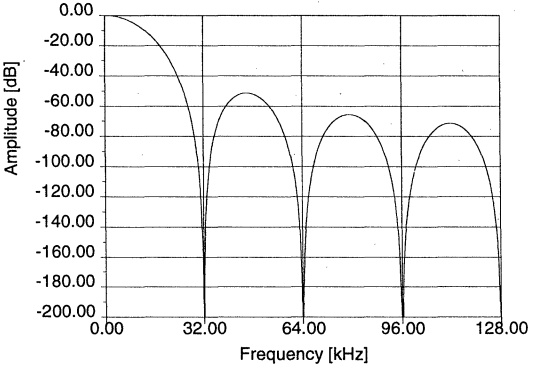


Figure 5. On-chip Filter Response

$$X(z) = \sum_{n=0}^{28} h(n+1)\, z^{-n}$$

Coefficient	Value
h(1) = h(29)	1.00
h(2) = h(28)	4.00
h(3) = h(27)	10.00
h(4) = h(26)	20.00
h(5) = h(25)	35.00
h(6) = h(24)	56.00
h(7) = h(23)	84.00
h(8) = h(22)	120.00
h(9) = h(21)	161.00
h(10) = h(20)	204.00
h(11) = h(19)	246.00
h(12) = h(18)	284.00
h(13) = h(17)	315.00
h(14) = h(16)	336.00
h(15)	344.00

Table 3. On-chip Filter Coefficients

The two proposed off-chip filter stages are as follows: The first off-chip stage is a 43rd-order modified sinc FIR filter. Its coefficients are listed in Appendix 1, along with a plot of its transfer function. Attenuation at 500 Hz (CLKIN = 1.024 MHz) is 1.47 dB. The minimum attenuation in the (n x 4 kHz) +/- 500 Hz bands is 132 dB.

The second off-chip filter stage is a 301st-order FIR filter that performs the necessary low-pass function, with less than 0.00016 dB ripple in the dc-400 Hz band. Attenuation in the region from 500 Hz to 2 kHz is typically greater than 130 dB. The coefficients for the second off-chip filter stage are listed in Appendix 1, along with a plot of its transfer function. An alternate final stage filter is also listed in Appendix 1. It is a 201st-order FIR filter and allows more passband ripple (0.07 dB).

If more ripple or less stop band rejection is acceptable, the off-chip filter complexity can be reduced. The filter examples given have been illustrated only as possible filters which can be utilized with the CS5324 to achieve quality performance from the A/D.

CS5324 Performance

The CS5324 A/D converter is intended for use in seismic and passive sonar applications. These applications require particularly high dynamic range capability. The CS5324 offers high dynamic range without compromising spectral purity. The CS5324 typically achieves 120 dB of dynamic range, while maintaining signal/distortion at 110 dB.

An A/D converter system using the CS5324 A/D converter as its core was tested using Fast Fourier Transform techniques. The CS5324 was connected using the components as shown in the system connection diagram, Figure 1. Data was collected from the CS5324 with the use of a parallel I/O card in a PC-compatible computer. Software was used to implement the two stage digital filtering function. The output from the digital filtering software was submitted to a windowing algorithm and then to the FFT algorithm. Figure 6 illustrates the performance of the CS5324 when tested with a full scale 113 Hz signal. The CS5324 exhibits some second harmonic but no third harmonic. The test frequency of 113 Hz was selected, as this was the center frequency of a bandpass filter, constructed to reject harmonics and line frequencies present at the output of the signal generator. Note that the performance of the CS5324 will generally exceed the capability of most available sine wave test generators for frequencies between 2-500 Hz, as is the case in Figure 6. The excess noise, in this case, is due to the signal source. Figure 7 illustrates the performance of the CS5324 with a -60 dB 100 Hz input signal. The CS5324 is capable of converting with minimal intermodulation distortion as depicted in Figure 8.

Clock Source Considerations

To obtain maximum performance from the CS5324 requires a CLKIN signal which has a low level of clock jitter, i.e., less than 5 picoseconds of jitter. A well-designed crystal-based clock is preferred. The clock oscillator should have a well-regulated supply, with local bypass capacitors at the oscillator. The output from the oscillator should pass through as few logic gates or counter-divider stages as possible, as these can add jitter. Excess clock jitter will reduce the signal/noise performance of the A/D converter.

Power Supply Rejection Ratio

The power supply noise rejection of the CS5324 is frequency dependent. The rejection for frequencies between dc and 500 Hz (CLKIN=1.024 MHz) is nearly constant. Above 500 Hz, the off-chip digital filter will aid in rejecting interference until the frequency of the interference approaches frequencies near CLKIN/21.3 (above 48 kHz for CLKIN=1.024 MHz). Power supply interference above this frequency may cause noise to be modulated into the passband (dc to 500 Hz), degrading the performance of the A/D.

Power Supply Considerations

The system connection diagram, Figure 1, illustrates the recommended power supply arrangements. The CS5324 has two positive analog supply pins and two negative analog supply pins. Multiple pins are used to minimize the possibility of noise coupling on the chip. All six power supply pins should be decoupled to their respective grounds, with a 0.1 uF capacitor located near the device. The digital supplies are decoupled from the analog supplies with 10 ohm resistors to minimize the effects of digital noise in the converter.

The positive digital power supply of the CS5324 must never exceed either positive analog supply by more than a diode drop, or the CS5324 could experience permanent damage. If separate supplies are used for the analog and digital sections of the chip, care must be taken that the analog supply comes up first at power-up. Additionally, the power supplies to the CS5324 should be active before the reference current generator supplies the IREF input current. For proper start-up, the CLKIN signal should be active before IREF is applied. The recommended filter capacitors, which filter the reference currents, will aid

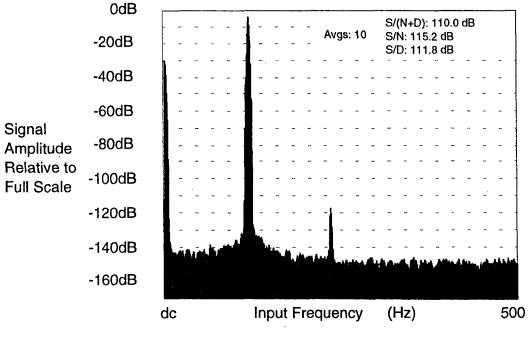


Figure 6. 1024 Point FFT Plot with Full Scale Input, 113 Hz.

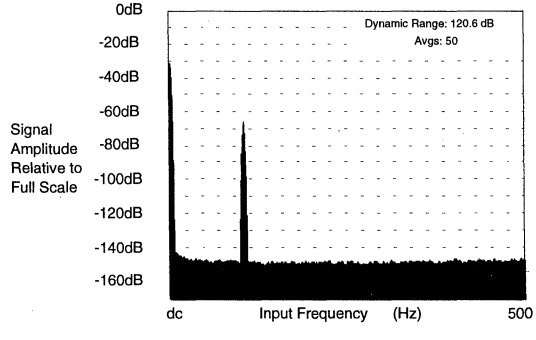
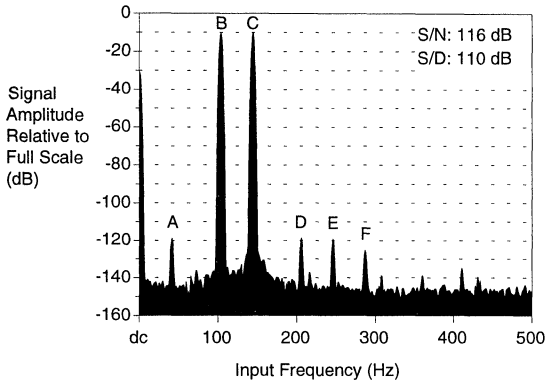


Figure 7. 1024 Point FFT Plot with -60 dB Input, 100 Hz.



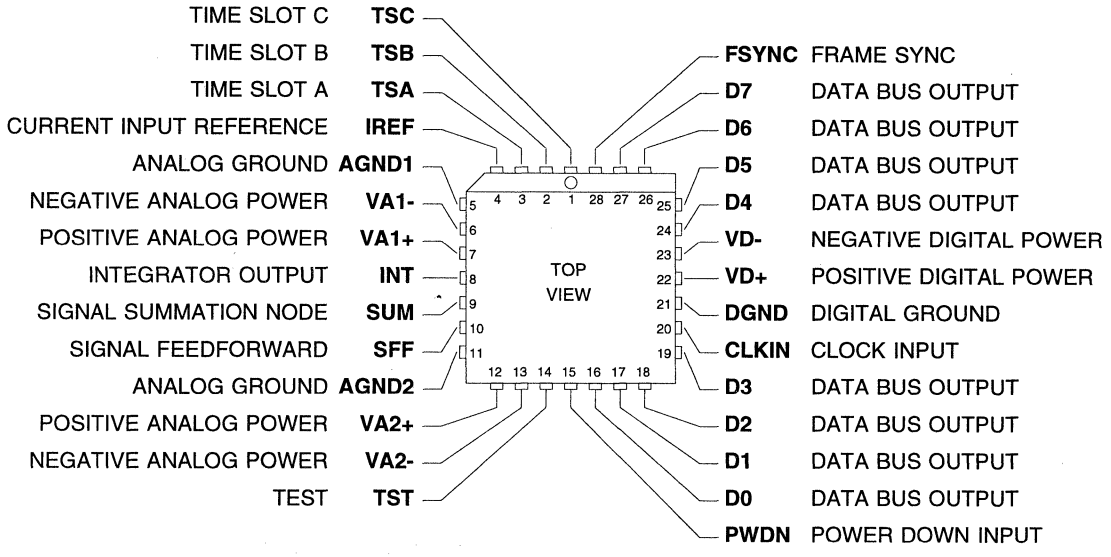
A – 40 Hz Intermodulation Distortion Term
B – 100 Hz Fundamental at 6 dB down
C – 140 Hz Fundamental at 6 dB down
D – 200 Hz Second Order Distortion Term
E – 240 Hz Intermodulation Distortion Term
F – 280 Hz Second Order Distortion Term

Note: S/N noise degradation is due to input signal source.

Figure 8. 1024 Point FFT Plot of Intermodulation Products.

in accomplishing these requirements. Use of good ground plane layout is recommended to achieve maximum performance.

Many seismic or sonar systems are battery powered, and utilize dc-dc converters to generate the necessary supply voltages for the system. To minimize the effects of power supply interference, it is desirable to operate the dc-dc converter at a frequency which is rejected by the digital filtering in the A/D converter. To achieve maximum benefit of the digital filter in the A/D, the dc-dc operating frequency should be located below 48 kHz (see Power Supply Rejection). A synchronous dc-dc converter, whose operating frequency is derived from the 1.024 MHz clock used to drive the CS5324, will minimize the potential for "beat frequencies" appearing in the dc to 500 Hz passband.



PIN DESCRIPTIONS

Power Supplies

VA1+, VA2+ – Positive Analog Power, PINS 7, 12
Positive analog supply voltage. Nominally +5 volts.

VA1-, VA2- – Negative Analog Power, PINS 6, 13
Negative analog supply voltage. Nominally -5 volts.

AGND1, AGND2 – Analog Ground, PINS 5, 11
Analog ground reference.

VD+ – Positive Digital Power, PIN 22
Positive digital supply voltage. Nominally +5 volts.

VD- – Negative Digital Power, PIN 23
Negative digital supply voltage. Nominally -5 volts.

DGND – Digital Ground, PIN 21
Digital ground reference.

Analog Inputs

IREF – Current Input Reference Node, PIN 4

This node accepts a 2 mA reference current to set the signal gain of the A/D converter.

SFF – Signal Feedforward, PIN 10

The input signal is fed forward around the integrator input stage by means of this input pin. This maximizes signal performance.

SUM – Signal Summation node, PIN 9

This is the input integrator virtual ground summing junction. The external integrator input resistor and integrating capacitor are connected to this node, along with a 500 uA bias current network.

INT – Integrator Output, PIN 8

Output pin of the input integrator stage. The external integrating capacitor is connected to this pin for proper operation.

Digital Inputs

CLKIN – Clock Input, PIN 20

A CMOS-compatible clock input to this pin (nominally 1.024 MHz) provides the necessary clock for operation of the modulator, digital filter and data output portions of the A/D converter.

PWDN – Power Down Input, PIN 15

When connected to +5 V (VD+) the CS5324 will enter a low-power state. For normal operation this pin should be tied to DGND.

TSA – Time Slot A, PIN 3

See TSC below.

TSB – Time Slot B, PIN 2

See TSC below.

TSC – Time Slot C, PIN1

The TSC input along with TSA and TSB select one of eight possible time periods in which data is output from the CS5324 in a time-multiplexed architecture. Table 2 indicates the decoding of the TSA, TSB, and TSC inputs.

FSYNC – Frame Sync, PIN 28

A transition from a low to high level on this input will re-initialize the CS5324. The digital filter will be initialized and the time-slot counter will be set to zero.

D0 through D7 – Data Bus Outputs, PINS 16-19, 24-27

3-state output pins. Data will be presented out of these pins in the form of two eight-bit bytes during a time slot selected by the TSA, TSB and TSC inputs. The high-order byte with eight data bits will be presented first followed by a second eight-bit byte, which consists of the four low-order data bits, three status bits, and one unused bit.

Miscellaneous

TST – Test, PIN 14

Reserved for production test facility. Should be tied to DGND for normal operation.

PARAMETER DEFINITIONS

Dynamic Range

The ratio of the full-scale (rms) signal to the broadband noise signal. Broadband noise is measured with the input grounded within the bandwidth of dc to 500 Hz. Units in dB.

Signal-to-Distortion

The ratio of the full-scale (rms) signal to the rms sum of all harmonics up to 500 Hz. Units in dB.

Intermodulation Distortion

The ratio of the rms sum of the two test frequencies (100 and 140 Hz) which are each 6 dB down from full-scale to the rms sum of all intermodulation components within the the bandwidth of dc to 500 Hz. Units in dB.

Full Scale Error

The ratio of the difference between the value of the voltage reference and analog input voltage to the full scale span (two times the voltage reference value). This ratio is calculated after the effects of offset and the external bias components are removed and the analog input voltage is adjusted to yield a code value of 1280 out of the CS5324. Measurement of this parameter uses the circuitry illustrated in the System Connection Diagram. Units in %.

Full Scale Drift

The change in the Full Scale value with temperature. Units in %/°C.

Offset

The difference between the analog ground and the analog voltage necessary to yield an output code from the CS5324 of 00(H). Measurement of this parameter uses the circuit configuration illustrated in the System Connection Diagram. Units in mV.

Offset Drift

The change in the Offset value with temperature. Units in µV/°C.

Appendix 1.

Off-chip Filter Stages

Two stages of off-chip filtering are recommended for use with the CS5324. The first stage is a decimate-by-8 modified-sinc filter with 43 coefficients. Its magnitude response is illustrated in Figure A1.1. Table A1.1 lists its coefficients.

The second filter stage is a 301st-order low-pass filter. Its magnitude plot is illustrated in Figure A1.2 with an expanded view of the passband ripple illustrated in Figure A1.3. Table A1.2 lists the coefficients for this filter.

An alternative second stage filter is also included. It has fewer coefficients, and therefore, is less complex than the previous second stage filter. The magnitude plot of the alternative filter is illustrated in Figure A1.4 with an expanded view of the passband ripple in Figure A1.5. Note that this low-pass function has slightly less out-of-band rejection and somewhat higher passband ripple. The filter coefficients for the alternative final stage are listed in Table A1.3.

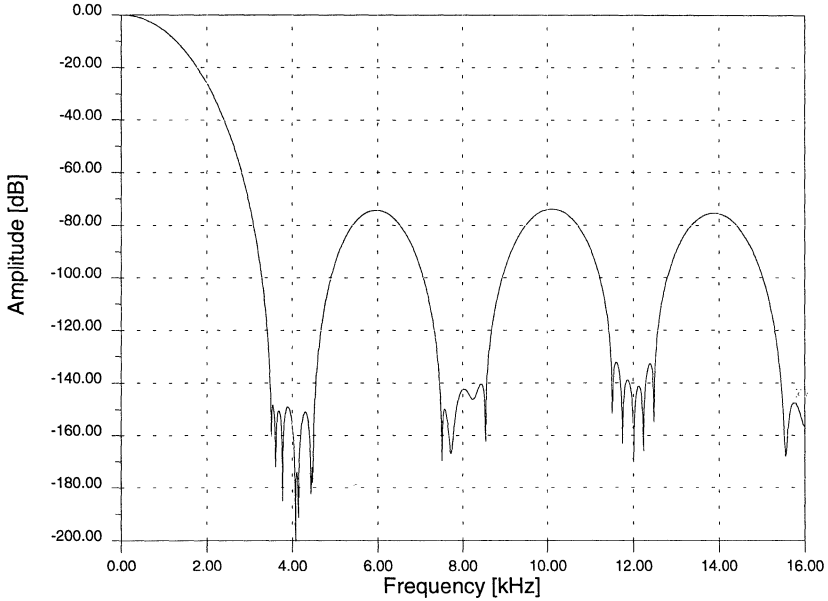


Figure A1.1. First Stage Off-chip Filter – Magnitude Plot

h(1)	=	h(43)	=	1623	h(12)	=	h(32)	=	1143595
h(2)	=	h(42)	=	5137	h(13)	=	h(31)	=	1494661
h(3)	=	h(41)	=	12950	h(14)	=	h(30)	=	1889251
h(4)	=	h(40)	=	28499	h(15)	=	h(29)	=	2315005
h(5)	=	h(39)	=	55210	h(16)	=	h(28)	=	2752059
h(6)	=	h(38)	=	99783	h(17)	=	h(27)	=	3185947
h(7)	=	h(37)	=	169332	h(18)	=	h(26)	=	3584677
h(8)	=	h(36)	=	272838	h(19)	=	h(25)	=	3926472
h(9)	=	h(35)	=	414146	h(20)	=	h(24)	=	4191616
h(10)	=	h(34)	=	604491	h(21)	=	h(23)	=	4354400
h(11)	=	h(33)	=	847470	h(22)	=			4410541

Table A1.1. First Stage Off-chip Filter – 43 Coefficients

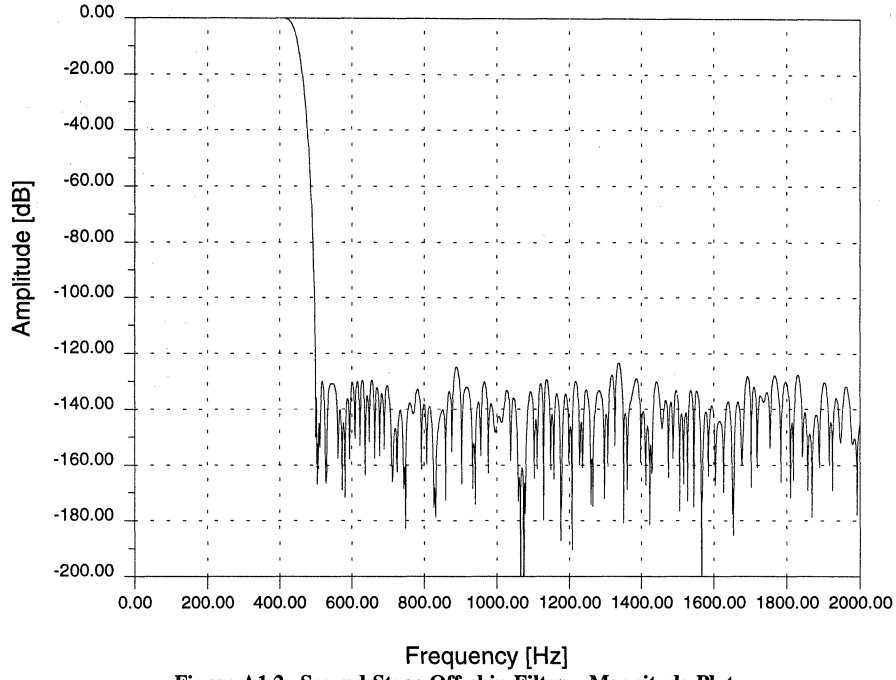


Figure A1.2. Second Stage Off-chip Filter – Magnitude Plot

h(1) = h(301) = 4	h(52) = h(250) = -1711	h(103) = h(199) = 124723
h(2) = h(300) = 6	h(53) = h(249) = -7104	h(104) = h(198) = 145121
h(3) = h(299) = 4	h(54) = h(248) = -9771	h(105) = h(197) = 96333
h(4) = h(298) = -6	h(55) = h(247) = -7963	h(106) = h(196) = -4251
h(5) = h(297) = -28	h(56) = h(246) = -1918	h(107) = h(195) = -112209
h(6) = h(296) = -58	h(57) = h(245) = 5964	h(108) = h(194) = -175323
h(7) = h(295) = -85	h(58) = h(244) = 12013	h(109) = h(193) = -158449
h(8) = h(294) = -93	h(59) = h(243) = 12943	h(110) = h(192) = -62339
h(9) = h(293) = -68	h(60) = h(242) = 7567	h(111) = h(191) = 73359
h(10) = h(292) = -7	h(61) = h(241) = -2315	h(112) = h(190) = 185878
h(11) = h(291) = 75	h(62) = h(240) = -12399	h(113) = h(189) = 217891
h(12) = h(290) = 146	h(63) = h(239) = -17689	h(114) = h(188) = 146090
h(13) = h(289) = 166	h(64) = h(238) = -14905	h(115) = h(187) = -4196
h(14) = h(288) = 108	h(65) = h(237) = -4360	h(116) = h(186) = -166796
h(15) = h(287) = -23	h(66) = h(236) = 9720	h(117) = h(185) = -263179
h(16) = h(286) = -185	h(67) = h(235) = 20798	h(118) = h(184) = -239689
h(17) = h(285) = -302	h(68) = h(234) = 22983	h(119) = h(183) = -96169
h(18) = h(284) = -300	h(69) = h(233) = 14065	h(120) = h(182) = 108776
h(19) = h(283) = -144	h(70) = h(232) = -2922	h(121) = h(181) = 280687
h(20) = h(282) = 130	h(71) = h(231) = -20553	h(122) = h(180) = 331861
h(21) = h(281) = 414	h(72) = h(230) = -30166	h(123) = h(179) = 224879
h(22) = h(280) = 565	h(73) = h(229) = -26027	h(124) = h(178) = -4045
h(23) = h(279) = 467	h(74) = h(228) = -8537	h(125) = h(177) = -255205
h(24) = h(278) = 106	h(75) = h(227) = 15226	h(126) = h(176) = -407467
h(25) = h(277) = -399	h(76) = h(226) = 34244	h(127) = h(175) = -375114
h(26) = h(276) = -826	h(77) = h(225) = 38558	h(128) = h(174) = -153475
h(27) = h(275) = -935	h(78) = h(224) = 24349	h(129) = h(173) = 169870
h(28) = h(274) = -594	h(79) = h(223) = -3468	h(130) = h(172) = 447384
h(29) = h(273) = 127	h(80) = h(222) = -32689	h(131) = h(171) = 536503
h(30) = h(272) = 947	h(81) = h(221) = -49042	h(132) = h(170) = 369619
h(31) = h(271) = 1468	h(82) = h(220) = -43038	h(133) = h(169) = -3865
h(32) = h(270) = 1359	h(83) = h(219) = -15194	h(134) = h(168) = -426733
h(33) = h(269) = 538	h(84) = h(218) = 23126	h(135) = h(167) = -696076
h(34) = h(268) = -725	h(85) = h(217) = 54160	h(136) = h(166) = -655325
h(35) = h(267) = -1882	h(86) = h(216) = 61841	h(137) = h(165) = -276498
h(36) = h(266) = -2320	h(87) = h(215) = 39925	h(138) = h(164) = 307141
h(37) = h(265) = -1673	h(88) = h(214) = -3894	h(139) = h(163) = 839720
h(38) = h(264) = -56	h(89) = h(213) = -50321	h(140) = h(162) = 1044525
h(39) = h(263) = 1898	h(90) = h(212) = -76781	h(141) = h(161) = 751372
h(40) = h(262) = 3264	h(91) = h(211) = -68222	h(142) = h(160) = -3724
h(41) = h(261) = 3239	h(92) = h(210) = -25304	h(143) = h(159) = -953887
h(42) = h(260) = 1580	h(93) = h(209) = 34332	h(144) = h(158) = -1671933
h(43) = h(259) = -1168	h(94) = h(208) = 83049	h(145) = h(157) = -1718209
h(44) = h(258) = -3814	h(95) = h(207) = 95832	h(146) = h(156) = -813868
h(45) = h(257) = -5004	h(96) = h(206) = 62860	h(147) = h(155) = 1027355
h(46) = h(256) = -3886	h(97) = h(205) = -4158	h(148) = h(154) = 3464481
h(47) = h(255) = -631	h(98) = h(204) = -75642	h(149) = h(153) = 5912858
h(48) = h(254) = 3478	h(99) = h(203) = -116939	h(150) = h(152) = 7722306
h(49) = h(253) = 6517	h(100) = h(202) = -104877	h(151) = h(151) = 8388608
h(50) = h(252) = 6784	h(101) = h(201) = -40254	
h(51) = h(251) = 3702	h(102) = h(200) = 50253	

Table A1.2. Second Stage Off-chip Filter – 301 Coefficients

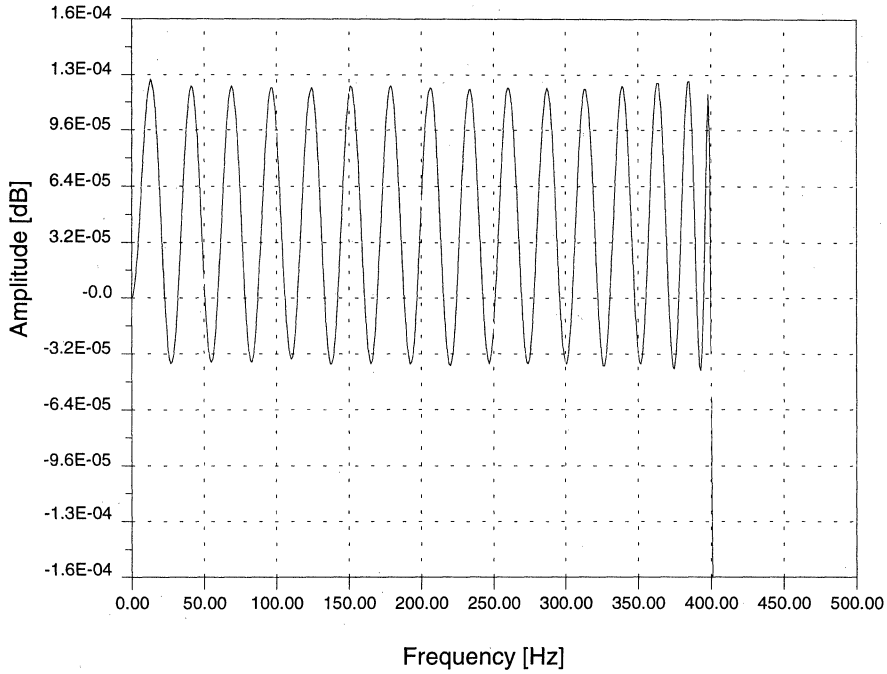


Figure A 1.3. Second Stage Off-chip Filter – Passband Ripple Plot

h(1) = h(201) = -68	h(35) = h(167) = 24059	h(69) = h(133) = 64893
h(2) = h(200) = -266	h(36) = h(166) = -1482	h(70) = h(132) = 229769
h(3) = h(199) = -681	h(37) = h(165) = -29822	h(71) = h(131) = 305309
h(4) = h(198) = -1350	h(38) = h(164) = -48300	h(72) = h(130) = 245984
h(5) = h(197) = -2192	h(39) = h(163) = -47054	h(73) = h(129) = 64260
h(6) = h(196) = -2938	h(40) = h(162) = -24000	h(74) = h(128) = -168625
h(7) = h(195) = -3124	h(41) = h(161) = 13122	h(75) = h(127) = -349221
h(8) = h(194) = -2181	h(42) = h(160) = 49003	h(76) = h(126) = -386474
h(9) = h(193) = 366	h(43) = h(159) = 66874	h(77) = h(125) = -245727
h(10) = h(192) = 4634	h(44) = h(158) = 56133	h(78) = h(124) = 28395
h(11) = h(191) = 10142	h(45) = h(157) = 18103	h(79) = h(123) = 323264
h(12) = h(190) = 15743	h(46) = h(156) = -33025	h(80) = h(122) = 502448
h(13) = h(189) = 19809	h(47) = h(155) = -75161	h(81) = h(121) = 466350
h(14) = h(188) = 20712	h(48) = h(154) = -87623	h(82) = h(120) = 203318
h(15) = h(187) = 17462	h(49) = h(153) = -60982	h(83) = h(119) = -193406
h(16) = h(186) = 10292	h(50) = h(152) = -2877	h(84) = h(118) = -554902
h(17) = h(185) = 889	h(51) = h(151) = 63451	h(85) = h(117) = -704448
h(18) = h(184) = -7915	h(52) = h(150) = 108121	h(86) = h(116) = -538246
h(19) = h(183) = -13029	h(53) = h(149) = 107776	h(87) = h(115) = -84243
h(20) = h(182) = -12292	h(54) = h(148) = 57300	h(88) = h(114) = 490248
h(21) = h(181) = -5542	h(55) = h(147) = -25620	h(89) = h(113) = 932553
h(22) = h(180) = 4957	h(56) = h(146) = -106083	h(90) = h(112) = 1005109
h(23) = h(179) = 15066	h(57) = h(145) = -146288	h(91) = h(111) = 595458
h(24) = h(178) = 20225	h(58) = h(144) = -122895	h(92) = h(110) = -209660
h(25) = h(177) = 17383	h(59) = h(143) = -39611	h(93) = h(109) = -1121850
h(26) = h(176) = 6584	h(60) = h(142) = 71441	h(94) = h(108) = -1730461
h(27) = h(175) = -8560	h(61) = h(141) = 161525	h(95) = h(107) = -1642084
h(28) = h(174) = -21921	h(62) = h(140) = 186220	h(96) = h(106) = -632318
h(29) = h(173) = -27236	h(63) = h(139) = 126698	h(97) = h(105) = 1247052
h(30) = h(172) = -20930	h(64) = h(138) = 1412	h(98) = h(104) = 3649798
h(31) = h(171) = -4177	h(65) = h(137) = -138356	h(99) = h(103) = 6019586
h(32) = h(170) = 16903	h(66) = h(136) = -228840	h(100) = h(102) = 7753188
h(33) = h(169) = 33304	h(67) = h(135) = -222225	h(101) = h(101) = 8388608
h(34) = h(168) = 36843	h(68) = h(134) = -110815	

Table A 1.3. Alternate Second Stage Off-chip Filter – 201 Coefficients

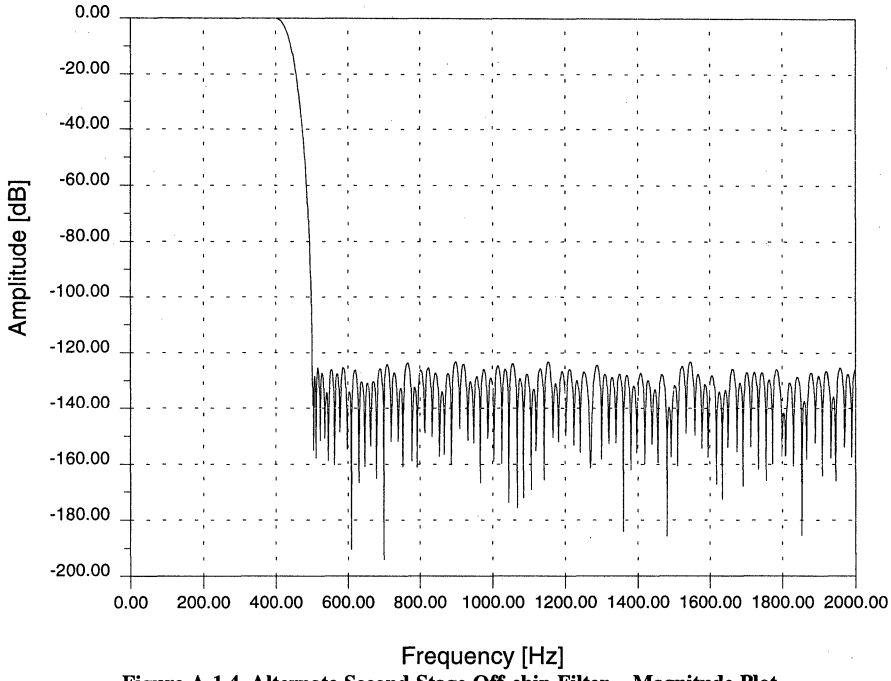


Figure A 1.4 Alternate Second Stage Off-chip Filter – Magnitude Plot

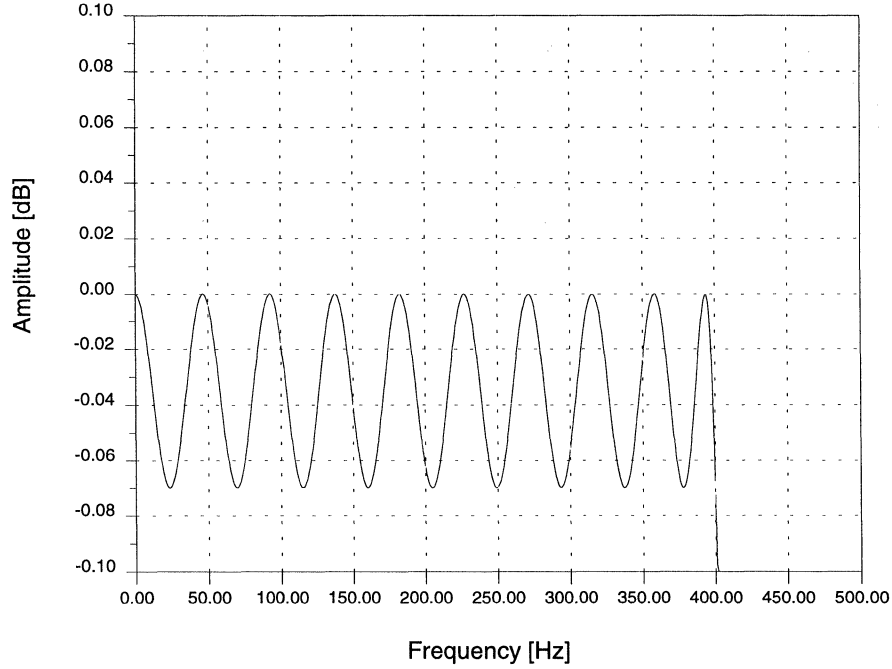


Figure A1.5 Alternate Second Stage Off-chip Filter – Passband Ripple Plot

Semiconductor Corporation

CDB5324

Evaluation Board for CS5324

2

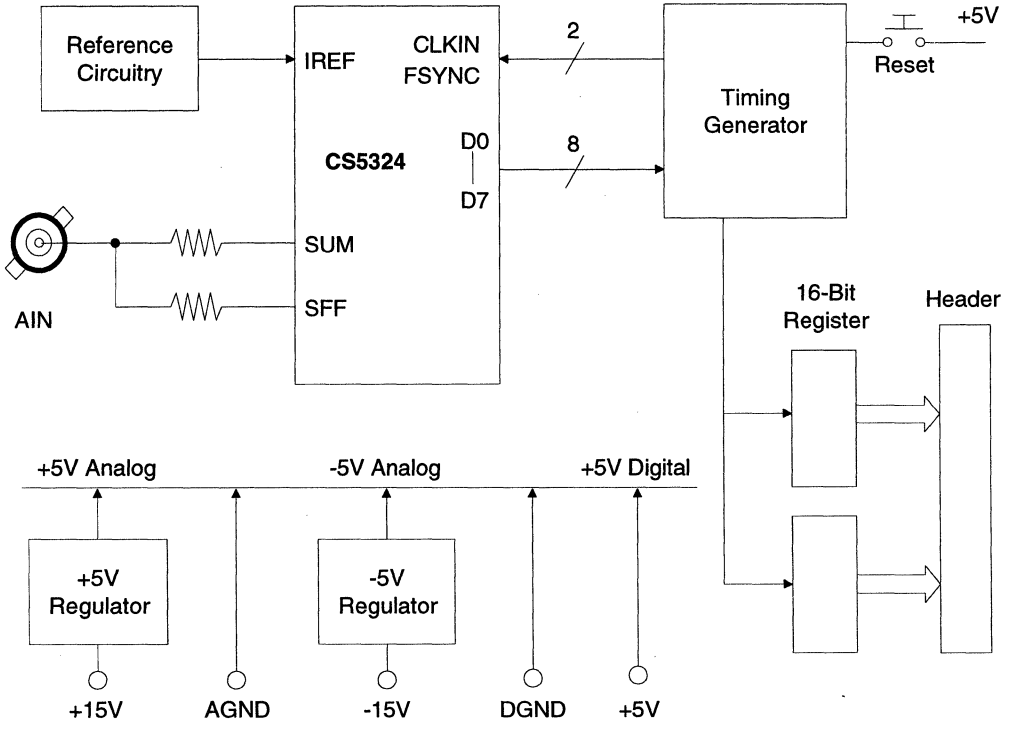
Features

- PC/µP-compatible Header Connection
  - 16 Bit Parallel Data
  - Three-State Output
  - Data Ready Signal
- Analog/Digital Patch Areas
- Analog BNC Input Connector

General Description

The CDB5324 is an evaluation board that allows the laboratory characterization of the CS5324 A/D converter. The CS5324 is a 120dB dynamic range, 500Hz bandwidth ADC intended for seismic applications. The board supports ±10 volt analog input signals and generates the timing signals which format the output data from the CS5324 into a single 16-bit parallel word.

ORDERING INFORMATION: CDB5324



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

Power Supplies and Voltage Reference

The CDB5324 evaluation board requires three separate input voltages for proper operation. Figure 1 illustrates the power supply connections. The required power supply input voltages consist of +5V, +15V, and -15V. The +5V input supplies power to the digital logic portion of the board. The +15V and -15V inputs are regulated down to provide the +5V and -5V supplies necessary for the CS5324. Also included in Figure 1 is a start-up circuit which allows a power-down signal to turn off both the CS5324 and the supply current to the LTC1021 voltage reference. An RC delay is added as part of the start-up circuitry to insure the the +5V digital supply is present before the LTC1021 voltage reference is turned on. The FSYNC and CLKIN signals to the CS5324 must

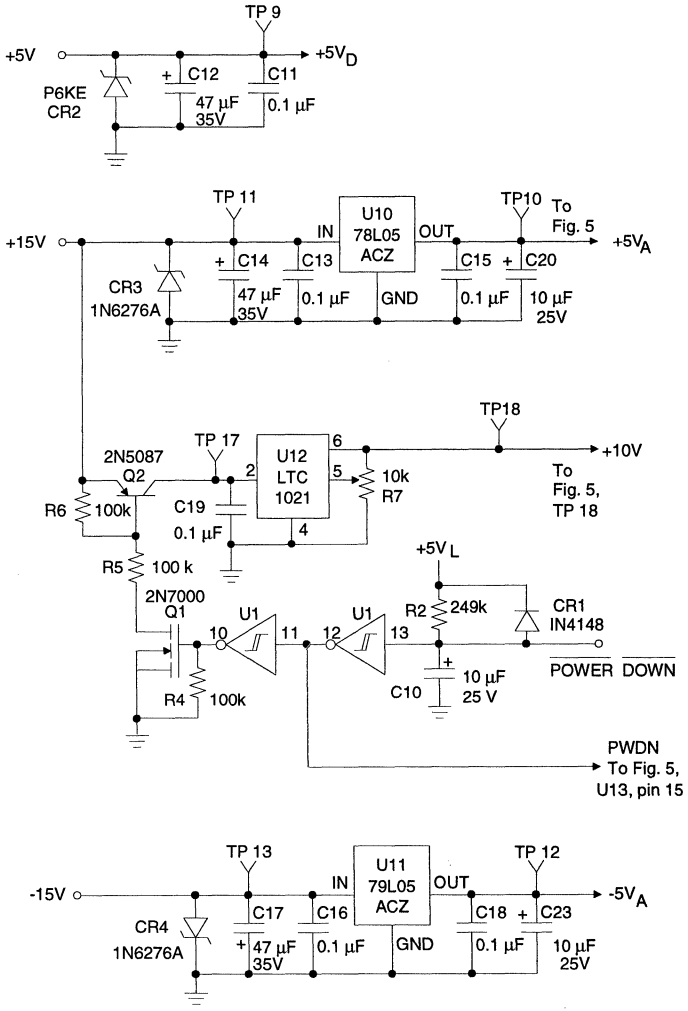


Figure 1. Voltage Regulators and +10V Reference

be furnished by the digital logic whenever the voltage reference is turned on to insure proper start-up of the device. This start-up circuitry is provided on the evaluation board to insure proper start-up of the CS5324 while using separate laboratory supplies which may then be turned on in any sequence. This circuitry is not required if all of the supplies are activated at the same time.

Clock Oscillator/Divider

Figure 2 illustrates the oscillator and clock divider circuitry used to generate the 1 MHz clock for the CS5324 A/D converter. This circuitry is in the digital patch area of the circuit card. The 1 MHz clock to the CS5324 must have low jitter. Jitter on the clock of any high resolution A/D converter

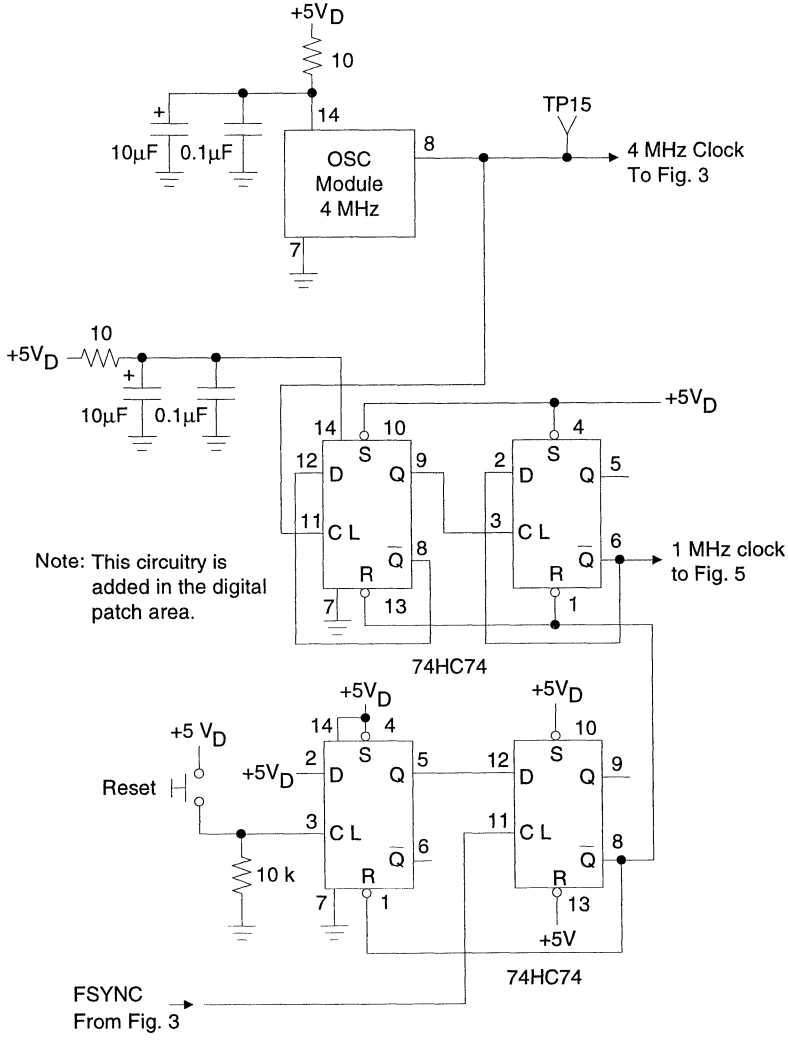


Figure 2. Clock Oscillator/Divider

will reduce the signal-to-noise capability of the device.

Note that both the oscillator and the dual D flip-flop used to divide the oscillator output are individually decoupled from the +5V logic supply. The second dual D flip-flop pair are used to synchronize the 1 MHz from the dual D divider to be in phase with the 1 MHz out of the 74HC590 counter. This synchronization is necessary to insure that the other timing signals derived from the 74HC590 outputs have the proper phase relationship to the 1 MHz clock in the CS5324.

Reset

To insure synchronization of the 1 MHz clock to the CS5324 with the other clock signals in the system, the reset button in the digital patch area of the board must be activated after power is applied to the system.

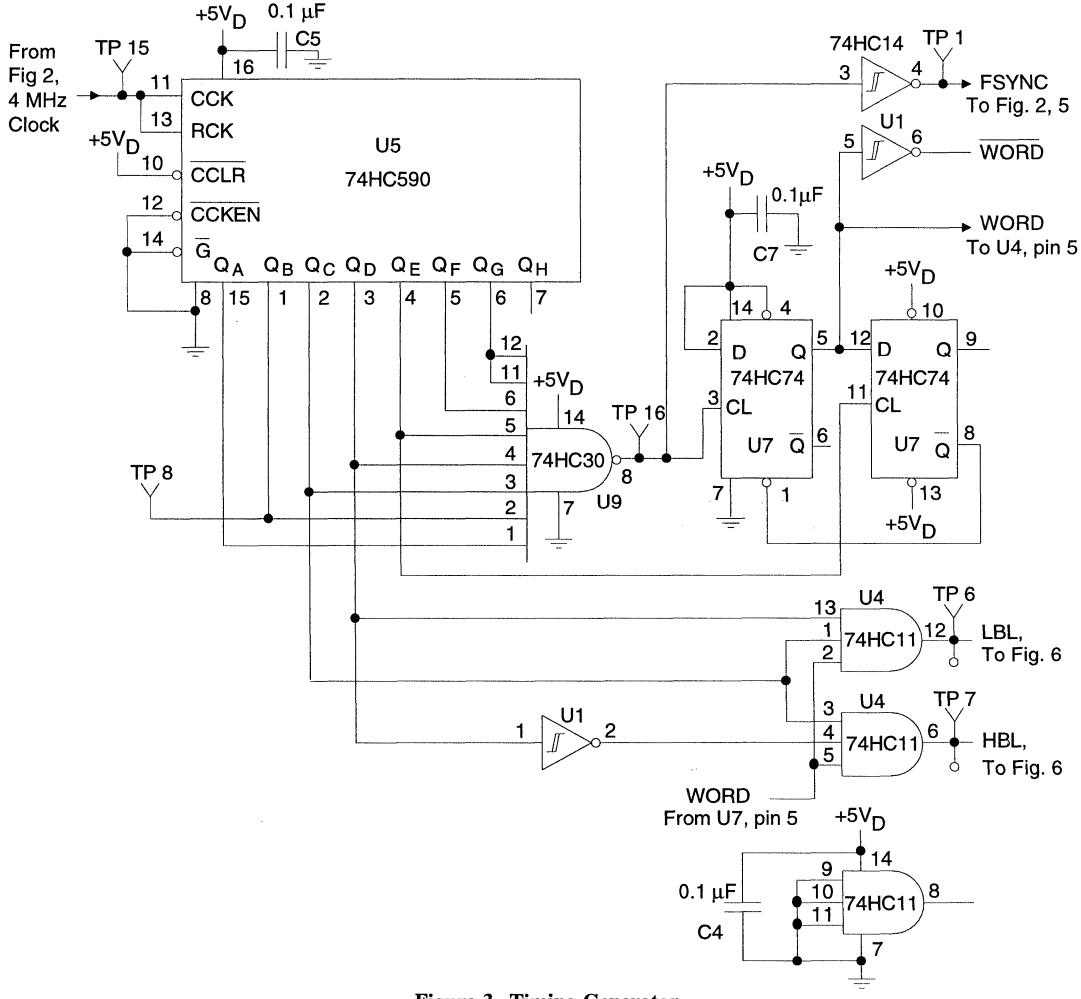


Figure 3. Timing Generator

Timing Generator

Figure 3 illustrates the logic circuitry which generates the timing signals used to latch the data coming out of the CS5324 A/D converter. The outputs from the 74HC590 counter are used to generate FSYNC, HBL (High Byte Latch), LBL (Low Byte Latch), and WORD. Figure 4 illustrates the timing relationships of these signals.

CS5324 A/D Converter

The connections to the CS5324 chip are illustrated in Figure 5. The analog and digital supply voltages are all decoupled close to the device. Included in the schematic are the discrete components used to develop the reference current and signal current inputs to the device. The AIN BNC is the signal input to the evaluation board. The input range is set for 20 volts p-p. Data from the CS5324 is output as two 8-bit bytes. These two bytes are latched into the output registers of Figure 6.

Output Registers/Header Connector

Data from the CS5324 A/D converter is latched into the two 74HC574 octal flip-flops by the HBL and LBL latch signals generated by the timing generator. The outputs of the 74HC574's are then connected to the 40-pin header Connector. Figure 7 identifies the pins on the 40-pin header.

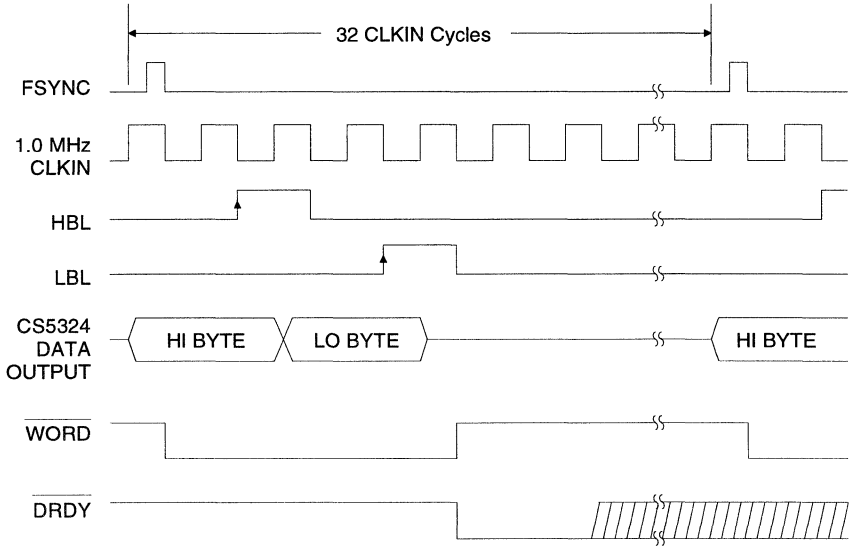


Figure 4. Timing Diagram

Note that each of the data output pins is adjacent to a ground pin on the header. In constructing a cable for interfacing to the evaluation board, twisted-pair ribbon cable (Beldon Vari-Twist 9V28040 or equivalent) should be used. Each twisted pair should include a ground line with the data signal as this minimizes radiated noise.

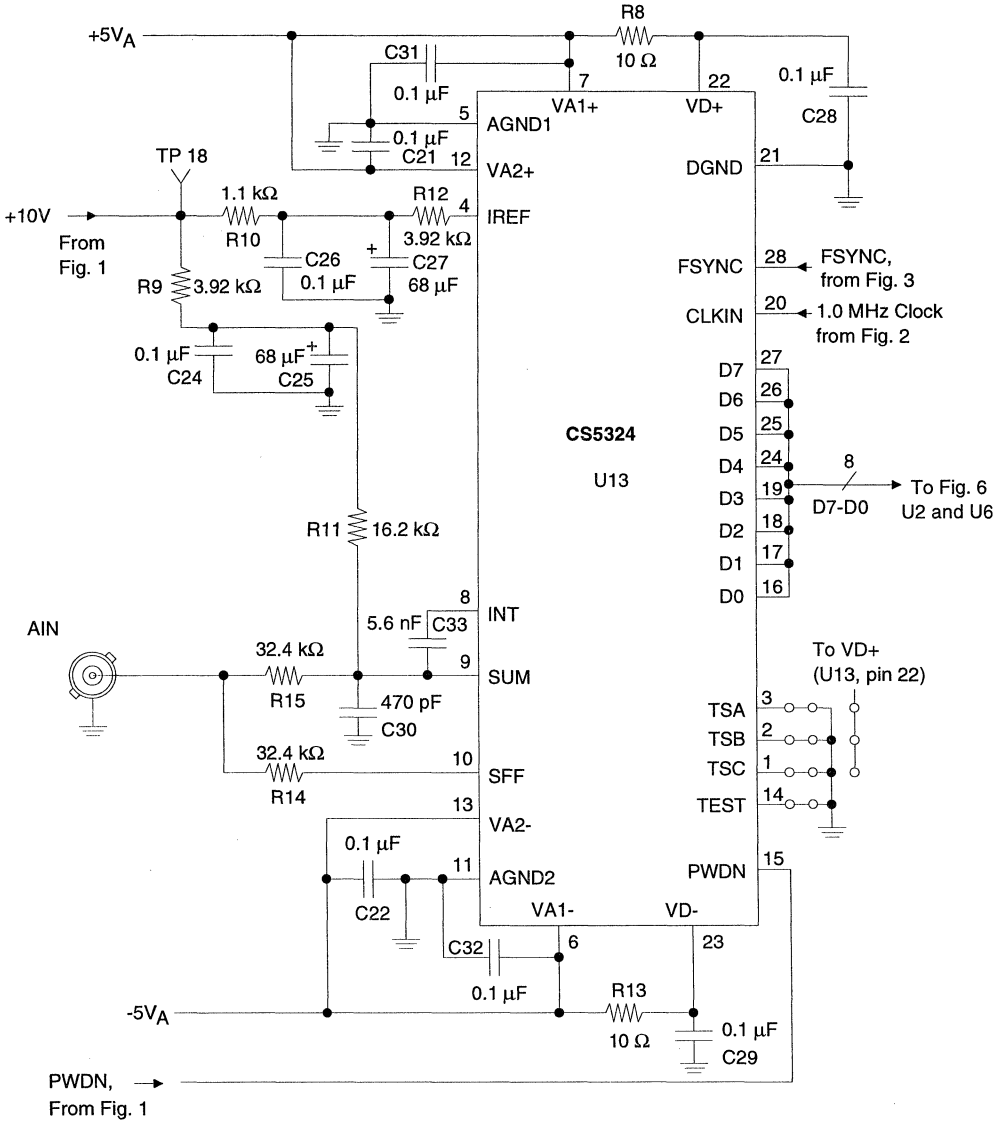


Figure 5. CS5324 A/D Converter

Using the Evaluation Board

Connect the appropriate power supply voltages to the binding posts of the board. Twist the +5V digital supply lead with the digital ground lead from the board to the supply. Also twist the supply leads for the analog voltages. Use a high quality power supply which is low in noise and line frequency (50/60 Hz) interference.

Connect a coaxial cable from the analog BNC to the signal source. Note that the performance of the A/D converter will exceed the capability of

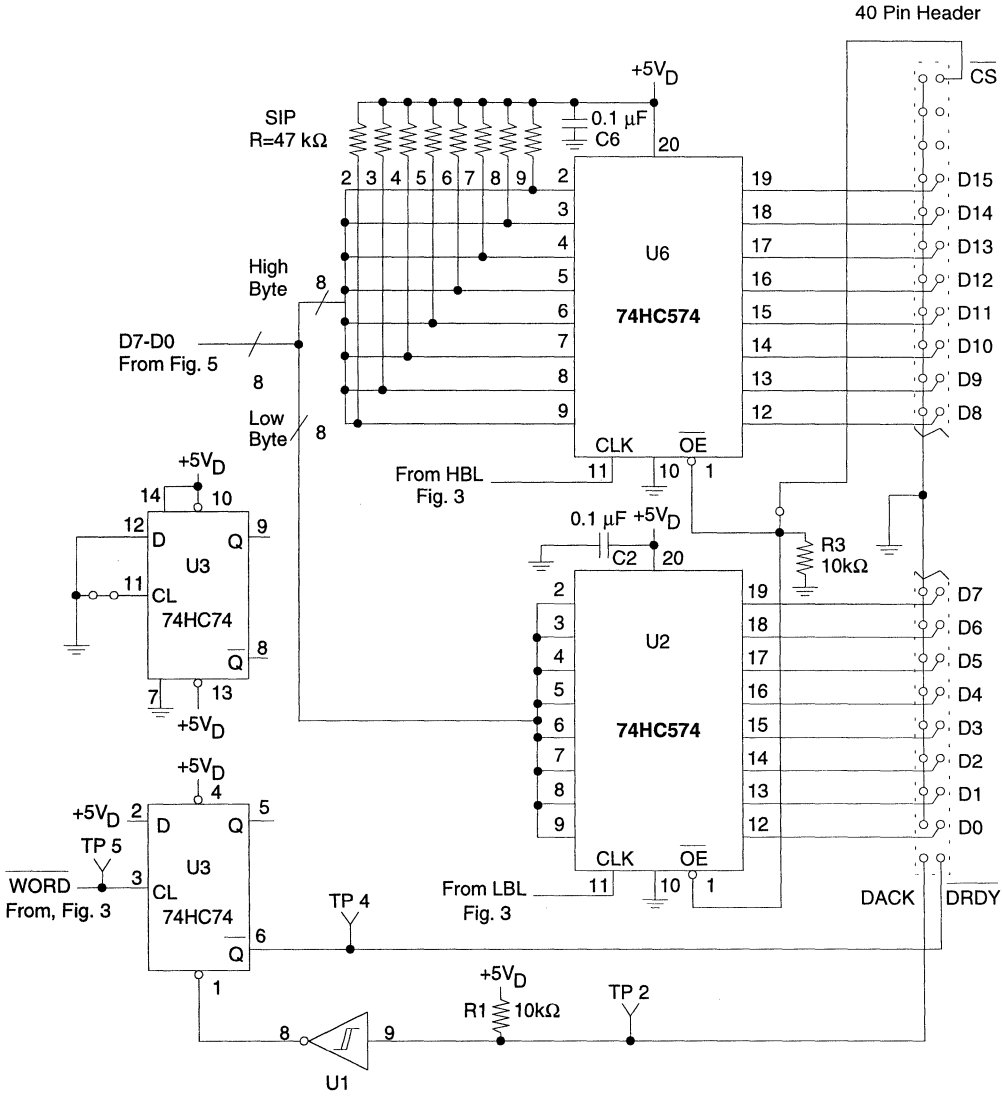


Figure 6. Output Registers/Header Connector

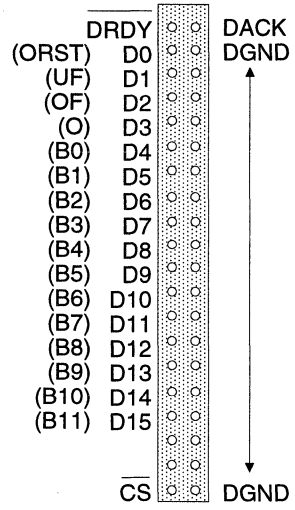


Figure 7. Header Pin Identification

most signal generators, especially with respect to noise and line frequency interference.

Power-up the evaluation board and activate the reset button (located in the digital patch area). The ribbon cable to the 40-pin header should remain disconnected until after power is applied to the board. This is a requirement only if power can be sourced from the data collection equipment to the evaluation board. (In the event that current is sourced through the ribbon cable into the evaluation board, and then power is applied, the evaluation board circuitry may not start-up properly).

Data from the evaluation board must be processed using digital filter functions, such as those found in the Appendix of the CS5324 data sheet to achieve the full 120 dB dynamic range of the A/D.

Evaluation Board Performance

To evaluate the performance of the evaluation board will require a quality signal source. A Khron-Hite 4400A low distortion oscillator can be used if an additional narrowband filter is used to filter out the line frequency interference and broadband noise which is part of the oscillator signal. Note that when using the Khron-Hite oscillator with a 60 Hz line frequency, interference components at 60, 120, 180 and 240 Hz show up as well as the oscillator fundamental. These interference components are generally 105 to 115 dB below full scale and will therefore show up in an FFT plot of the A/D's performance.

With a pure signal source provided to the AIN BNC input, output words are collected and filtered. The resulting data is then windowed and submitted to the FFT algorithm. The results can then be plotted. Performance plots for the CS5324 can be found in the CS5324 data sheet.

Component Layout

Figure 8 illustrates the component layout of the CDB5324 evaluation board. Note that this layout does not include the components added in the digital patch area. The components in the digital patch area are indicated in schematic diagram of Figure 2.

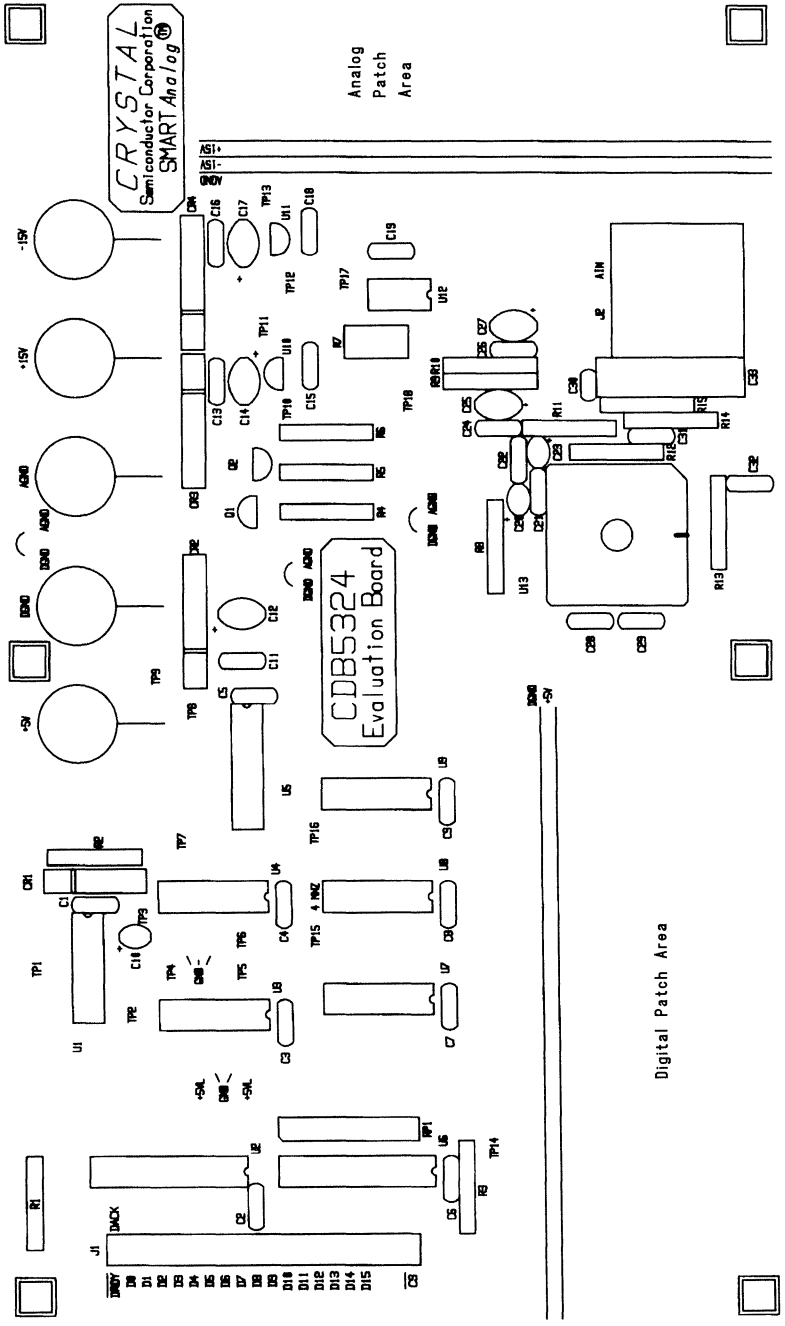


Figure 8. CDB5324 Component Layout

•Notes•

12-Bit, 1MHz Self-Calibrating A/D Converter

Features

- Monolithic CMOS Sampling ADC
  - On-Chip Track and Hold Amplifier
  - Microprocessor Interface
- Throughput Rates up to 1MHz
- True 12-Bit Accuracy over Temperature
  - Typical Nonlinearity: 3/4 LSB
  - No Missing Codes to 12 Bits
- Total Harmonic Distortion: 0.02%
- Dynamic Range: 72dB
- Self-Calibration Maintains Accuracy over Time and Temperature
- Low Power Dissipation: 750mW

General Description

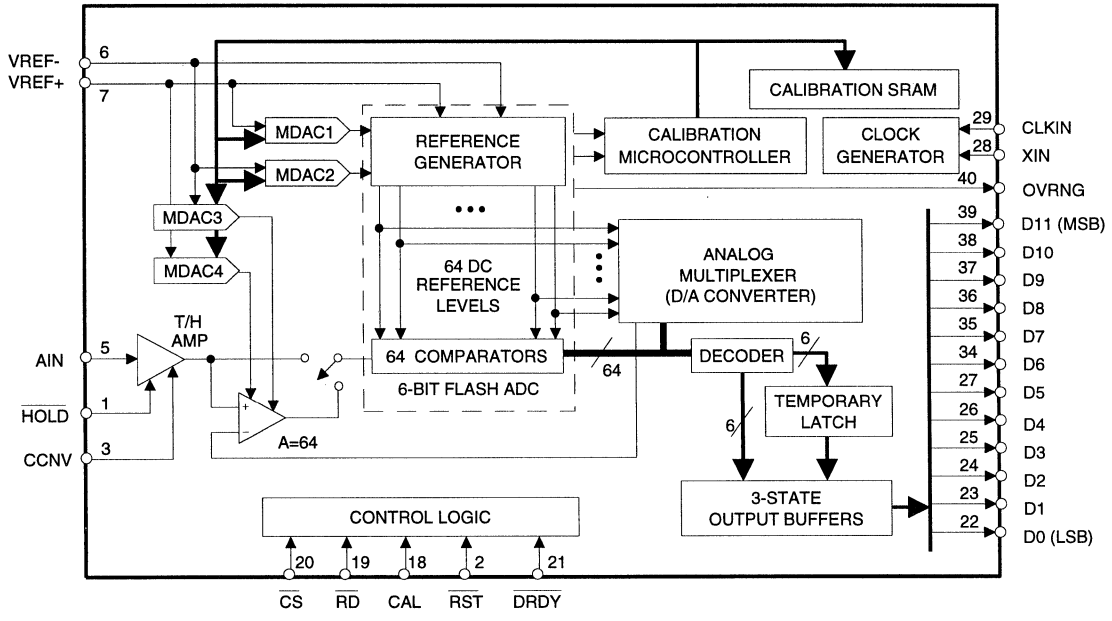
The CS5412 CMOS analog to digital converter provides a true 12-bit representation of an analog input signal at sampling rates up to 1MHz. To achieve high throughput, the CS5412 uses pipelined acquisition and settling times as well as overlapped conversion cycles.

Unique self-calibration circuitry insures 12-bit accuracy over time and temperature. Also, a background calibration process constantly adjusts the converter's linearity, thereby insuring superior harmonic distortion and signal-to-noise performance throughout operating life.

The CS5412's advanced CMOS construction provides low power consumption of 750mW and the inherent reliability of monolithic devices.

An evaluation board is available which allows fast confirmation of performance, as well as example ground and layout arrangements.

ORDERING INFORMATION: Page 2-334



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

ANALOG CHARACTERISTICS (T_A = 25°C (Note 1); All VA+ pins, VD+ = 5V; All VA- pins, VD- = -5V; VREF+ = +1.5V; VREF- = -1.5V; f_{CLK} = 8MHz for -1; 100 kHz Full Scale Input Sine-wave; Continuous Convert Mode unless otherwise specified)

Parameter*	CS5412-J, K			CS5412-A, B			CS5412-S, T			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Resolution T_{min} to T_{max}	12	-	-	12	-	-	12	-	-	Bits
Specified Temperature Range	0 to +70			-40 to +85			-55 to +125			°C
Dynamic Performance										
Peak Harmonic or Spurious Noise (Note1)										
T_{min} to T_{max} 100kHz Input	75	82	-	75	82	-	75	82	-	dB
490kHz Input	-	68	-	-	68	-	-	68	-	dB
Total Harmonic Distortion		0.0125			0.0125			0.0125		%
Signal-to-(Noise plus Distortion) (Note 1)										
0dB Input (Full Scale)										
T_{min} to T_{max} -J, A, S	65	71	-	65	71	-	65	71	-	dB
-K, B, T	68	71	-	68	71	-	68	71	-	dB
-40dB Input	-	32	-	-	32	-	-	32	-	dB
dc Accuracy										
Linearity Error (Notes 1, 2)										
T_{min} to T_{max} -J, A, S	-	±3/4	±2.0	-	±3/4	±2.0	-	±1	±3.0	LSB
T_{min} to T_{max} -K, B, T	-	±3/4	±1.0	-	±3/4	±1.0	-	±3/4	±2.0	LSB
Differential Linearity (Note 1)										
T_{min} to T_{max} -J, A, S	-	±1/2	NMC	-	±1/2	NMC	-	±1/2	NMC	LSB
T_{min} to T_{max} -K, B, T	-	±1/2	±0.9	-	±1/2	±0.9	-	±1/2	-0.9/ +1.25	LSB
Full Scale Error T_{min} to T_{max} (Note 1)	-	±2	±8	-	±2	±8	-	±3	±10	LSB
Offset Error T_{min} to T_{max} (Note 1)	-	±1.5	±3	-	±1.5	±3	-	±1.5	±4	LSB

NMC = No Missing Codes

Notes:
1. All T_{min} to T_{max} specifications apply after calibration at the temperature of interest. Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.
2. If the input voltage is static such that 128 consecutive conversions yield the same output code, then the transfer function may become non-monotonic.

* Refer to *Definitions* at the end of this data sheet.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter*	CS5412-J, K Min	CS5412-J, K Typ	CS5412-J, K Max	CS5412-A, B Min	CS5412-A, B Typ	CS5412-A, B Max	CS5412-S, T Min	CS5412-S, T Typ	CS5412-S, T Max	Units
Analog Input										
Aperture Time	-	35	-	-	35	-	-	35	-	ns
Aperture Jitter	-	50	-	-	50	-	-	50	-	ps, rms
Input Bandwidth										
Small Signal, -3dB (Note 3)	-	4	-	-	4	-	-	4	-	MHz
Full Power, -3dB	-	3.5	-	-	3.5	-	-	3.5	-	MHz
Analog Input Impedance at dc	-	10	-	-	10	-	-	10	-	MΩ
Input Capacitance VREF- pin	-	50	-	-	50	-	-	50	-	pF
AIN, VREF+ pins	-	10	-	-	10	-	-	10	-	pF
Conversion & Throughput										
Conversion Time (Note 4, 5)	1.25	-	1.5	1.25	-	1.5	1.25	-	1.5	µs
Throughput Rate	1	-	-	1	-	-	1	-	-	MHz
Acquisition Time (Note 6)	-	400	-	-	400	-	-	400	-	ns
Power Supplies										
Power Supply Current (Note 7)										
I_{A+}	-	70	90	-	70	90	-	70	90	mA
I_{A-}	-	-70	-90	-	-70	-90	-	-70	-90	mA
I_{D+}	-	5	10	-	5	10	-	5	10	mA
I_{D-}	-	-5	-10	-	-5	-10	-	-5	-10	mA
Power Consumption (Note 7)	-	750	1000	-	750	1000	-	750	1000	mW
Power Supply Rejection at dc										
Positive Supplies	-	50	-	-	50	-	-	50	-	dB
Negative Supplies	-	50	-	-	50	-	-	50	-	dB

Notes:
3. Input 40 dB below full scale.
4. Measured from falling transition on $\overline{\text{HOLD}}$ to falling transition on $\overline{\text{DRDY}}$.
5. Applies to conversions triggered externally. In Continuous Convert mode throughput proceeds at one-eighth the master clock frequency with a fixed 10 clock cycle conversion time.
6. The internal track-and-hold returns to the track mode on the fourth master clock cycle after the start of a conversion cycle. It is guaranteed to acquire a full-scale step to 12-bit accuracy while operating at full throughput.
7. All outputs unloaded. All inputs CMOS levels.

* Refer to *Definitions* at the end of this data sheet.

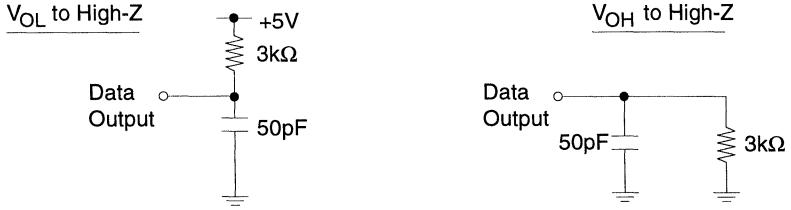
SWITCHING CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; All VA+ pins, VD+ = 5V ± 5%; All VA- pins, VD- = -5V ± 5%; Inputs: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

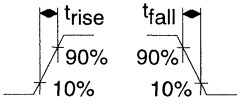
Parameter		Symbol	Min	Typ	Max	Units
Master Clock Frequency		f_{CLK}	3	-	8	MHz
Master Clock Duty Cycle			40	-	60	%
Rise Times: Any Digital Input	(Note 8)	t_{rise}	-	-	1.0	µs
Any Digital Output			-	20	-	ns
Fall Times: Any Digital Input	(Note 8)	t_{fall}	-	-	1.0	µs
Any Digital Output			-	20	-	ns
$\overline{HOLD}$/CLKIN Phase Relationship						
State 7 to $\overline{HOLD}$ Low		t_{ha}	62.5	-	-	ns
$\overline{HOLD}$ Low to State 0		t_{hb}	0	-	-	ns
State 0 to $\overline{HOLD}$ High		t_{hc}	75	-	-	ns
$\overline{HOLD}$ High to State 7		t_{hd}	30	-	-	ns
Conversion Time	(Note 9)	t_c	10	-	12	MCC*
$\overline{DRDY}$ Pulse Width		t_{dpw}	-	3	-	MCC*
Data Delay Time		t_{dd}	-	20	50	ns
Access Times: $\overline{CS}$ Low to Data Valid	(Note 10)	t_{csa}	-	55	110	ns
$\overline{RD}$ Low to Data Valid		t_{rda}	-	55	110	ns
Output Float Delay:		t_{fd}				
$\overline{CS}$ or $\overline{RD}$ High to Output Hi-Z			-	40	110	ns
Cal Pulse Width:	(Note 11)					
CAL High and $\overline{CS}$ Low		t_{csh}	2	-	-	MCC*
$\overline{RST}$ Pulse Width		t_{rpw}	2	-	-	MCC*

Notes:
8. $\overline{HOLD}$ and CLKIN should be driven with signals which have rise and fall times of 25 ns or faster.
9. Conversion time in the Continuous Convert mode is a fixed 10 clock cycles.
10. Data goes valid when both $\overline{CS}$ and $\overline{RD}$ are low simultaneously. Each access time assumes the other control input is already low or falls concurrently.
11. If CAL is brought low while $\overline{CS}$ is low, a calibration cycle will be initiated.

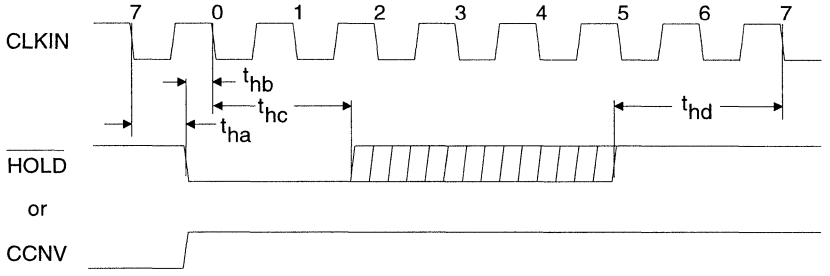
* MCC = Master Clock Cycles; 1 MCC = $1/f_{CLK}$

Float Delay Test Circuits

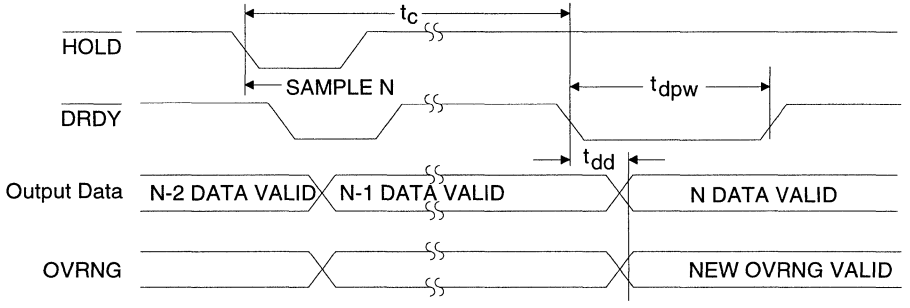




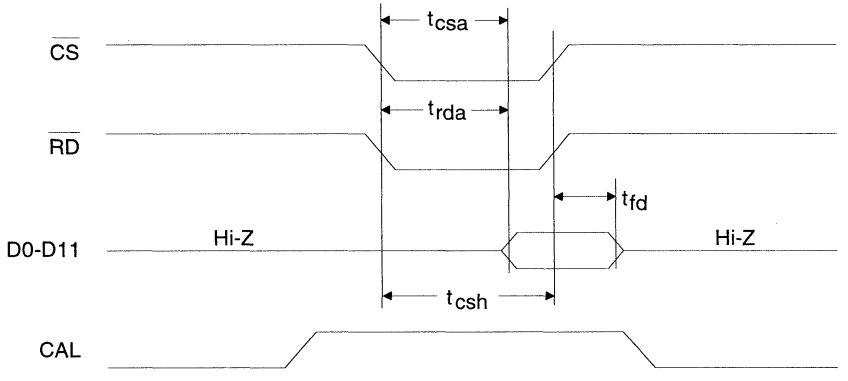
Rise and Fall Times



Hold/Master Clock Phase Relationship



Conversion Timing



Read and Calibration Control Timing

DIGITAL CHARACTERISTICS ($T_A = T_{min}$ to T_{max}; All VA+ pins, VD+ = 5V ± 5%; All VA- pins, VD- = -5V ± 5%) All measurements below are performed under static conditions.

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	(Note 12)	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	(Note 12)	V_{IL}	-	-	0.8	V
High-Level Output Voltage	(Note 13)	V_{OH}	(VD+)-1.0V	-	-	V
Low-Level Output Voltage	I_{out} = 1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-10	-	+10	µA
3-State Leakage Current		I_{OZ}	-10	-	+10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

Notes: 12. All pins except $\overline{HOLD}$ and CLKIN which require inputs of V_{IL} = 0.5V and V_{IH} = VD+ - 0.5V.
13. I_{out} = -100µA. This specification guarantees TTL compatibility (V_{OH} = 2.4V @ I_{out} = -40µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see note 14)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.75	5.0	VA2+, VA5+	V
	Negative Digital	VD-	-4.75	-5.0	-5.25	V
	Positive Analog	(VA1+) - (VA5+)	4.75	5.0	5.25	V
	Negative Analog	(VA1-) - (VA3-)	-4.75	-5.0	-5.25	V
Analog Input Voltage		V_{AIN}	VREF-	-	VREF+	V
Analog Reference Voltages						
	Unipolar Input Range	VREF+	20	-	3.0	V
		VREF-	-	AGND	-	V
	Bipolar Input Range	VREF+	1.0	-	1.5	V
		VREF-	-1.0	-	-1.5	V

Notes: 14. All voltages with respect to ground.

ABSOLUTE MAXIMUM RATINGS (AGND, DGND = 0V, see note 14)

Parameter		Symbol	Min	Max	Units
DC Power Supplies:					
Positive Digital		VD+	-0.3	VA2+, (VA5+)+0.3	V
Negative Digital		VD-	0.3	-6.0	V
Positive Analog	(Note 15)	(VA1+) - (VA5+)	-0.3	6.0	V
Negative Analog		(VA1-) - (VA3-)	0.3	-6.0	V
Input Current, Any Pin Exept Supplies	(Note 16)	I_{in}	-	+10	mA
Analog Input Voltage	(AIN and VREF pins)	V_{INA}	(VA1-)-(VA3-)-0.3	VA2+, (VA5+)+0.3	V
Digital Input Voltage		V_{IND}	-0.3	VA2+, (VA5+)+0.3	V
Ambient Operating Temperature		T_A	-55	125	°C
Storage Temperature		T_{stg}	-65	150	°C
Junction Temperature		T_J	-	160	°C
Junction to Ambient Tempco for CLCC Package		θ_{JA}	-	60	°C/W

Notes: 15. VA1+, VA3+, VA4+ must never exceed VA2+ and VA5+ by more than 0.3V.
16. Transient currents of up to 100mA will not cause SCR latch-up.

WARNING:Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

THEORY OF OPERATION

To achieve high speed and high accuracy, the CS5412 implements a standard 2-step flash A/D conversion using a self-calibrating architecture. Throughput is further maximized using pipelined acquisition and settling times as well as overlapped conversion cycles.

2-Step Flash A/D Conversion

The fastest method of performing A/D conversion is the brute-force single-step flash approach, for which an N-bit conversion involves comparing the analog input to 2^N-1 graduated voltage levels. The outputs from the 2^N-1 comparators are then processed and encoded into the proper binary format. The major limitation to this technique is that the number (and accuracy requirements) of comparators doubles with each additional bit of resolution. Thus, single-step flash converters are impractical today at greater than 8 or 10 bits of resolution.

The 2-step technique that the CS5412 uses employs slightly more complex sub-circuit blocks to achieve high resolution and results in negligible speed degradation. As shown in Figure 1, the CS5412 consists of a track-and-hold amplifier (*T/H1*), a 6-bit flash ADC, a 6-bit DAC, and a differential amplifier. When the convert command is issued, *T/H1* holds the analog input signal and the flash ADC converts the six MSB's (most-significant-bits) of the output word. The MSB's, once decoded, are latched. The flash converter's output is also loaded into the DAC. The DAC's output therefore represents the analog input less the quantization error of the first 6-bit flash conversion. This signal is then subtracted from the original analog input to yield the quantization error, which is then multiplied by 64 (2^6) and again applied to the flash ADC to yield the six LSB's (least-significant-bits). In effect, the first 6-bit flash forms the transfer function into 64 segments which are then filled in with 64 codes each by the second 6-bit flash. This yields a total of 4096 codes (64x64) for 12-bit resolution.

Calibration

The CS5412 uses several calibration techniques to insure 12-bit accuracy over time and temperature. A unique reference generating circuit provides the 64 graduated reference levels for the flash ADC and DAC. Critical to the CS5412's overall linearity, these references are continually adjusted to 12-bit accuracy during device operation. This background adjustment process is completely transparent to the user and results in less than ±1/2 LSB nonlinearity. Also, all comparators in the flash ADC are auto-zeroed to avoid differential linearity errors at the 64 segment boundaries due to noise and/or offsets in the comparators.

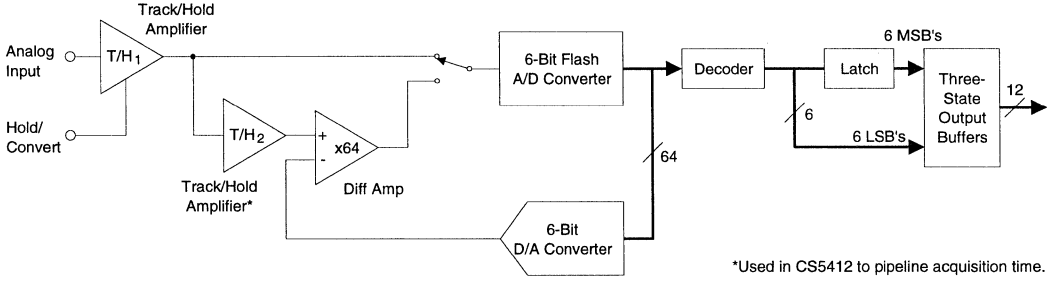


Figure 1 . Block Diagram of 2-Step Flash A/D Converter

The CS5412 also uses digital correction schemes. An on-chip microcontroller manipulates dedicated MDAC's to set the gain and offset of the 6-bit flash ADC; this insures less than ±1/2 LSB overall full-scale and offset errors in the CS5412. Gain and offset are similarly calibrated in the differential amplifier to avoid linearity errors at the 64 segment boundaries.

Upon power-up, the CS5412 is reset in hardware or software to initially calibrate the device. Calibration can be similarly initiated at any later time throughout operating life to insure 12-bit accuracy independent of environmental conditions.

Pipelined Timing

To achieve throughput rates up to 1MHz, the CS5412 pipelines settling times in both the sampling and conversion processes. The CS5412 can actually begin a conversion cycle while still operating on the previous sample. As shown in Figure 2, the *Hold and Convert* command for Sample N+1 can be issued before data from Sample N is valid at the output. By definition, the throughput time of the CS5412 is shorter than the conversion time due to the overlapped conversion cycles. Compared to a non-pipelined 1MHz ADC, the CS5412 provides the same 1MHz throughput, only the output data is delayed slightly in time (1.25µs delay through the ADC rather than 1µs).

The CS5412 also uses a second track-and-hold amplifier (termed *T/H2* in Figure 3) to pipeline the converter's acquisition time. As shown in Figure 3, *T/H2* holds the output from *T/H1* valid for the second flash conversion, *Flash 2*. This allows *T/H1* to release and acquire the analog input signal during the second flash conversion, allowing another *Hold & Convert* command to be issued even before the completion of *Flash 2*.

DIGITAL CIRCUIT CONNECTIONS

In addition to master clock and sampling connections which set the converter's timing, the CS5412 offers an *Overrange* output, 3-state output buffers, and flexible control interface. The CS5412 can therefore connect directly to a microprocessor's data and control busses or can be operated in a stand-alone mode.

Master Clock

The CS5412 operates from a master clock reference which must be supplied in the form of either a crystal or external clock. A crystal can be tied across the CLKIN and XIN pins, or alternatively, the CS5412 can be synchronized to the external system by driving CLKIN with a CMOS-compatible clock (XIN left floating). If the master clock is shut off while the CS5412 is powered up, an internal oscillator will start-up to keep all internal

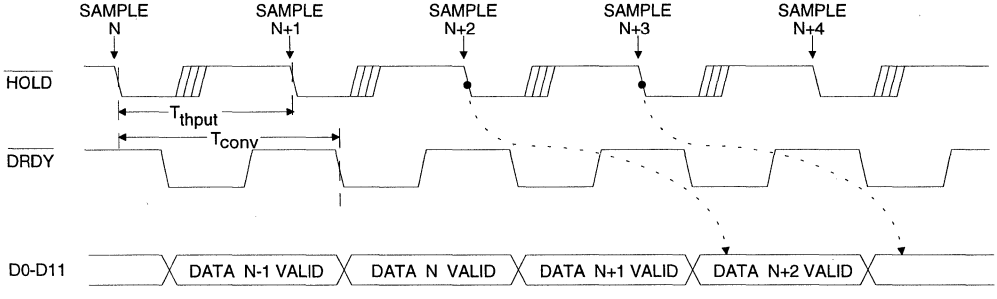


Figure 2. Pipelined Conversion Cycles

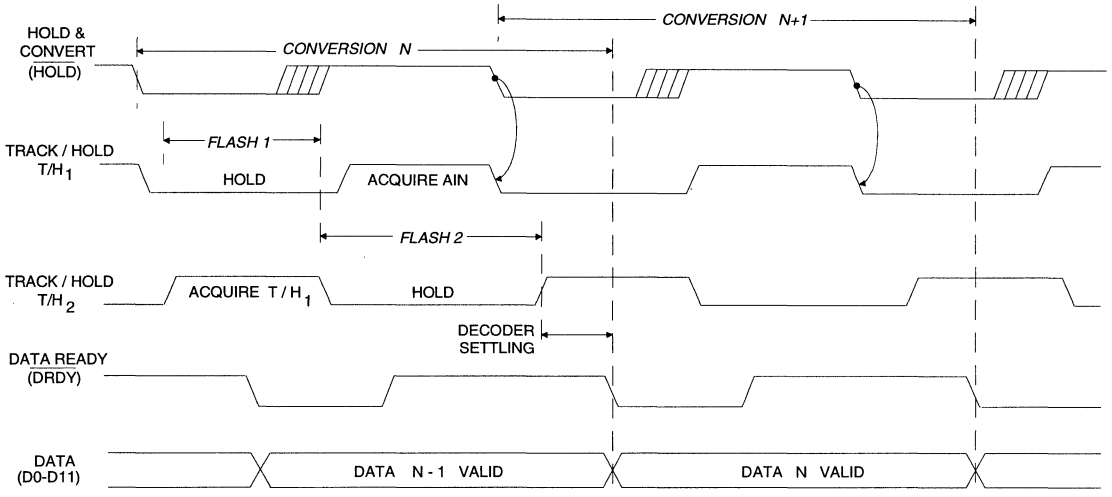


Figure 3. Pipelined Acquisition and Settling Times.

dynamic logic refreshed. This internal oscillator should not be used for conversions. Clock cycles can be selectively skipped at any time, but the clock's average frequency should never drop below the device's minimum specification (see Switching Characteristics).

Sampling/Initiating Conversions

There are two methods of controlling the CS5412's sampling/conversion timing. First, the CS5412 has a $\overline{\text{HOLD}}$ input which, on a falling edge, places the input track-and-hold amplifier in the hold state and initiates a conversion cycle. The CS5412 also features a *Continuous Convert* mode (CCNV and $\overline{\text{HOLD}}$ high) in which hold commands are internally generated every eight master clock cycles. The sampling/throughput rate is therefore controlled by adjusting the master clock frequency and there is no need to generate a sampling clock.

When CCNV is brought high with the proper relationship to CLKIN (shown in the timing diagrams), the next falling clock edge defines state 0.

Lower sampling rates can be created in the *Continuous Convert* mode by running the CS5412 at full throughput and decimating the output, selectively reading only a fraction of the available samples. Variable sampling rates can be implemented in this manner using a programmable divider on the $\overline{\text{DRDY}}$ output. When operating in the *Continuous Convert* mode, attention should be paid to jitter on the master clock, since jitter will directly affect sampling purity.

If the phase of sampling must be precisely controlled, the $\overline{\text{HOLD}}$ input must be used since the hold signal is internally-generated in the *Continuous Convert* mode. A falling edge on $\overline{\text{HOLD}}$ places the internal track-and-hold amplifier in the hold state and signals a conversion cycle to begin on the next falling edge of the master clock. The $\overline{\text{HOLD}}$ input was designed for minimum aperture jitter and therefore requires CMOS-compatible logic levels (not TTL-compatible).

Due to the CS5412's refreshing the 64 reference levels in the background, $\overline{\text{HOLD}}$ commands must be synchronized to the master clock and can only occur at intervals of 8 master clock cycles. The first $\overline{\text{HOLD}}$ command after the start of a reset or calibration cycle defines state 0 in the CS5412's

timing circuitry (see Figure 4). The sampling signal applied to $\overline{HOLD}$ must adhere to frequencies of $f_{clk}/8N$ such that subsequent $\overline{HOLD}$ commands will always fall between state 7 and state 0. If the sampling clock changes phase and a $\overline{HOLD}$ command occurs before state 7 or after state 0 the CS5412 may be thrown out of calibration, and 4288 clock cycles must be allowed for the converter to complete two full background refresh cycles. Likewise, conversion data should be considered invalid for 4288 clock cycles following the first $\overline{HOLD}$ command after the end of calibration to insure specified accuracy. If a normal, periodic, $\overline{HOLD}$ signal is applied during the entire calibration period, the data will be valid immediately after calibration, i.e. when OVRNG goes low.

Most often the sampling signal applied to $\overline{HOLD}$ can be derived from the master clock. In these cases, the master clock is divided by 8, 16, 24, 32, etc. If sampling must be locked to some external clock source, a phase-locked loop can be used to generate a master clock signal for CLKIN from the sampling signal. In this instance jitter on the $\overline{HOLD}$ input will directly affect sampling purity; however, the CS5412 will tolerate significant jitter on the master clock without loss of accuracy (assuming the $\overline{HOLD}$/CLKIN phase specifications are met).

Conversion Time/Throughput

In the *Continuous Convert* mode, throughput will proceed at one-eighth the master clock frequency and the delay through the CS5412 will be ten master clock cycles. When hold commands are generated externally at the $\overline{HOLD}$ pin, the analog input is held immediately as the $\overline{HOLD}$ input falls and the conversion cycle begins on the next falling edge of the master clock. The CS5412's conversion time will range from 10 to 11 clock cycles depending on the phase relationship of the $\overline{HOLD}$ signal to the master clock (see Figure 4). Throughput can still proceed at $f_{clk}/8$ independent of the conversion time. The pipelined overlap between conversion cycles will range from to 2 to 3 clock cycles.

Reset

Upon power-up, the CS5412 must be reset to guarantee a consistent starting condition and initially calibrate the device. A falling edge on the $\overline{RST}$ pin clears internal logic and a rising edge initiates a calibration cycle which takes 6,052,445 master clock cycles to complete. The $\overline{RST}$ input must remain low for at least 2 master clock cycles to be considered valid. A simple power-up reset circuit can be constructed by tying a capacitor from $\overline{RST}$ to DGND and a resistor from $\overline{RST}$ to VD+.

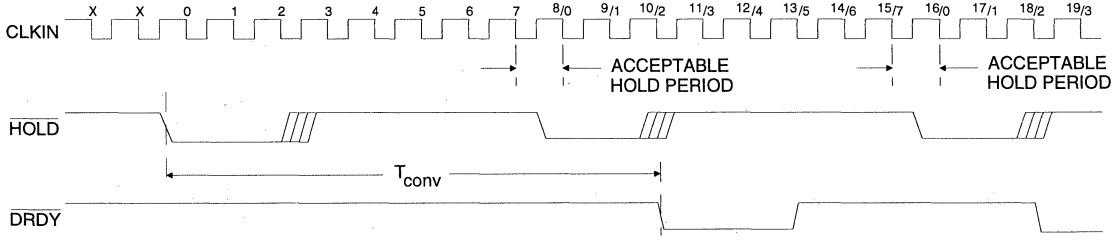


Figure 4. Hold / Conversion Timing.

Due to the CS5412's modest power dissipation and low temperature drift, no warm-up time is needed before reset to accommodate any self-heating effects. However, the voltage references (VREF+ and VREF-) should have stabilized to within their specified accuracies. The CS5412 can be reset later at any time during operation to initiate calibration. Reset overrides all other functions. If reset, the CS5412 will clear and initiate a new calibration cycle mid-conversion or mid-calibration.

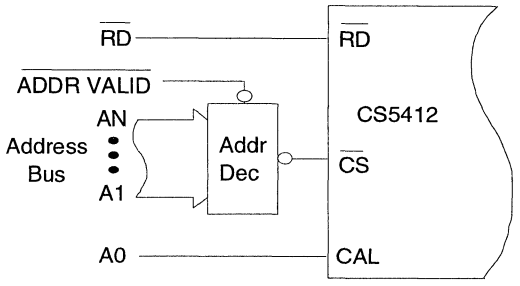


Figure 5. Microprocessor Controlled Operation.

Overrange

The CS5412 will flag an overrange input at the OVRNG pin whenever *the sampled analog input* exceeds either the positive or negative reference voltage. If the sampled input exceeds VREF+, OVRNG will go high as DRDY falls, and all ones will be loaded into the output buffers. Similarly, if the analog input is below VREF-, OVRNG will go high as all zeroes are loaded into the output buffers. OVRNG should be latched on the rising edge of $\overline{DRDY}$. The internal reference voltages are not affected by excursions of AIN outside the external reference voltages up to the supply voltages.

Thirteen clock cycles after $\overline{RST}$ or CAL transitions, OVRNG goes high. The OVRNG output remains high throughout a reset/calibration sequence and will return low after its completion. It can therefore be used to generate an interrupt indicating the CS5412 has completed calibration and is ready for operation.

Microprocessor Controlled Operation

The CS5412 features 3-state output buffers and a control interface which allow the device to connect directly to a microprocessor's data and control busses. Strobing both $\overline{CS}$ and $\overline{RD}$ low enables the CS5412's 3-state output buffers with the converter's 12-bit output word. As shown in Figure 5, a decoded address is normally applied to

$\overline{CS}$	$\overline{RD}$	CCNV	$\overline{HOLD}$	CAL	$\overline{RST}$	Function
0	0	X	X	0	1	Read Output Data
*	1	X	X	*	1	High Impedance Data Bus
1	X	X	X	X	1	High Impedance Data Bus
*	X	1	X	*	1	Continuous Convert Mode
*	X	0	↓	*	1	Hold and Start Convert
X	X	X	X	X	↑	Start Reset
0	X	X	X	↓	X	Start Reset

* Not critical to the operation specified. However, $\overline{CS}$ should not be low with CAL transitioning low or a software reset will result.

Table 1. CS5412 Truth Table.

$\overline{CS}$, and the $\overline{RD}$ input is derived from read and strobe signals from the microprocessor's control bus. The Data Ready ($\overline{DRDY}$) output can be used to generate an interrupt or drive a DMA controller to dump the CS5412's output directly into memory after each conversion. The $\overline{DRDY}$ output falls as new data is being loaded into the output buffers. Data should be latched on the rising edge of $\overline{DRDY}$ which occurs three master clock cycles after it falls.

The CS5412 internally buffers its output data, so data can be read while the device is tracking or converting the next sample. Therefore, retrieving the converter's digital output requires no reduction in ADC throughput. The CS5412 should be synchronized to the digital system via CLKIN to avoid potential errors due to enabling the 3-state output buffers while the part is converting. Using TTL loads also increases the potential for crosstalk between the digital and analog portions of the system. This crosstalk is due to high digital supply and signal currents arising from the TTL drive current required of each digital output. Connecting CMOS logic to the CS5412's digital outputs is recommended. Suitable logic families include 4000B, 74HC, 74AC, 74ACT, and 74HCT.

Initiating Calibration

In addition to the hardware reset, the CS5412 features a software calibration capability. Whenever CAL transitions low with $\overline{CS}$ low, or $\overline{CS}$ transitions high with CAL high, a calibration cycle will be initiated which is equivalent to the reset function. As shown in Figure 5, line A0 from the address bus can be connected to the CAL input when operating under microprocessor control. A read cycle from the CS5412's base address with A0 low will therefore retrieve output data while a read or write cycle with A0 high will initiate calibration. The CAL input is level sensitive, and like $\overline{RST}$, CAL overrides all other functions. Software-initiated calibrations can thus be used in lieu of a hardware reset at power-up.

Stand-Alone Operation

The CS5412 can be operated in a stand-alone mode independent of intelligent control. In this mode, $\overline{CS}$ and $\overline{RD}$ are hard-wired low, permanently enabling the 3-state output buffers. A free-running condition is established when CAL is tied low, and $\overline{HOLD}$ is continually strobed low or CCNV is held high. The CS5412's $\overline{DRDY}$ output can be used to externally latch the output data if desired. The $\overline{DRDY}$ output will strobe low for three master clock cycles after each conversion. Data will typically be unstable for 40ns after $\overline{DRDY}$ falls, so it should be latched on the rising edge of $\overline{DRDY}$. This results in a total delay of 13 master clock cycles through the CS5412.

ANALOG CIRCUIT CONNECTIONS

Like most 2-step flash A/D converters with internal track-and-hold amplifiers, the CS5412 offers a trivial load at its analog input compared to successive-approximation and single-step flash A/D converters. The reference connections similarly present high impedance loads. However, accurate system operation still requires careful attention to details at the design stage regarding source impedances as well as grounding and decoupling schemes.

Analog Input and Reference Connections

The CS5412's analog input range is defined by the voltages applied to the VREF- and VREF+ pins. The analog input (AIN) is referenced only to these reference voltages and is completely independent of the analog ground pins. The first code transition ideally occurs 1 LSB above VREF- and the last transition occurs 1 LSB below VREF+. The CS5412 can operate with a full-scale reference as low as 2.0V p-p, but signal-to-noise performance is maximized by using the full specified range of 3V p-p. Unipolar input ranges are achieved by tying VREF- to the system's analog ground and applying the reference voltage to VREF+. Bipolar input ranges are achieved by ap-

plying positive and negative voltages of equal magnitude to VREF+ and VREF- respectively. In this configuration, coding is in offset-binary format.

The CS5412's analog input (AIN) pin looks directly into the noninverting terminal of the track-and-hold amplifier resulting in over 10MΩ input impedance and less than 10pF input capacitance.

The reference voltages at the +VREF and -VREF inputs are dynamically sampled. This pulsed charge load requires each of the reference inputs to be decoupled with a 0.1µF ceramic capacitor in parallel with a 3.3µF tantalum capacitor. The tantalum capacitors should be chosen to maintain 3.3µF minimum capacitance over the operating temperature range. To maintain DC accuracy the reference(s) should have an output impedance of less than 5Ω at DC.

Grounding and Power Supply Decoupling

The CS5412 uses the analog ground connections, AGND1 and AGND2, only as stable, low impedance sources. No dc power currents flow through these connections, and they are completely independent of AIN and DGND. Still, AGND1 and AGND2 should be tied to the system's analog ground. The CS5412's analog input is referenced only to VREF+ and VREF-. Therefore, the analog input and reference voltages should be referred to the same ground potential (not necessarily AGND) which should be used as the entire system's analog ground. The optimal grounding configuration for the CS5412 utilizes one ground plane under the CS5412. Peripheral analog and digital circuitry should be partitioned on the circuit board and separate ground planes may or may not be used.

The digital and analog supplies are isolated within the CS5412 and are pinned out separately to minimize coupling between the analog and digital sections of the chip. The analog supplies also have multiple connections which minimize lead inductances and power separate portions of the converter's analog circuitry. The decoupling scheme shown in the *System Connection Diagram* in Figure 9 provides optimal decoupling between the CS5412's digital circuitry and the various analog sections of the chip. Ceramic capacitors are acceptable for all decoupling, and they should be placed as close to the supply pins as possible. If significant low-frequency noise is present on the supplies, 10µF tantalum capacitors are recommended in parallel with 0.1µF ceramic capacitors on the ±5V rails.

The positive digital power supply (VD+) should never exceed the positive analog supplies (VA2+ or VA5+) or the CS5412 could experience permanent damage. If the two supplies are derived from separate sources, care should be taken that the analog supply comes up first at power-up. The *System Connection Diagram* in Figure 8 shows a decoupling scheme which allows the CS5412 to be powered from a single set of ±5V rails. The positive digital supply is derived from the analog supplies though a 10Ω resistor to avoid the analog supply dropping below the digital supply. If this scheme is used, care must be taken to insure that any digital load currents (which flow through the 10Ω resistors) do not cause the magnitude of the digital supplies to drop below their minimum specification of 4.75V. The positive supplies must be active and stable prior to applying the negative supplies. The positive supplies should remain active and stable when the negative supply is removed at power-down.

The CDB5412 evaluation board is available for the CS5412, which eliminates the need to design, build, and debug a high-precision PC board to initially characterize the part. The board comes with a socketed CS5412 and can be quickly reconfigured to simulate any combination of sampling, calibration, and master clock conditions.

Performance

Two types of performance test results are presented here. With FFT based tests, a pure sine wave is input to the CS5412, and an FFT analysis is performed on the output data. Figure 6 shows the resulting plot with a 100 kHz input sine. Notice the absence of any harmonic distortion and the overall Signal to (Noise + Distortion) value of 70.3 dB.

Figure 7 shows the FFT plot when two sine waves are simultaneously applied to the input. Notice the lack of sum and difference products, indicating very good linearity.

A second test looks for variation in the code width of the CS5412, as the input moves from -Full Scale to +Full Scale. This is called the Differential Non Linearity (DNL) and is expressed as a deviation from the ideal (in LSB), with 0 being perfect. Figure 8 shows the CS5412's excellent DNL performance with most codes being within ± 0.1 LSB of perfect.

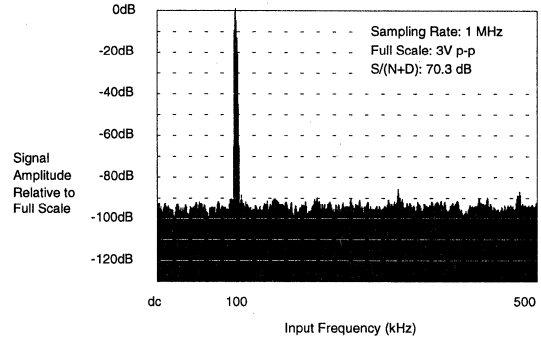


Figure 6. Typical CS5412 FFT Performance

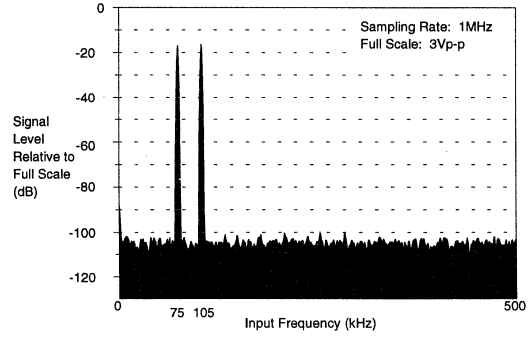


Figure 7. Intermodulation Distortion Performance

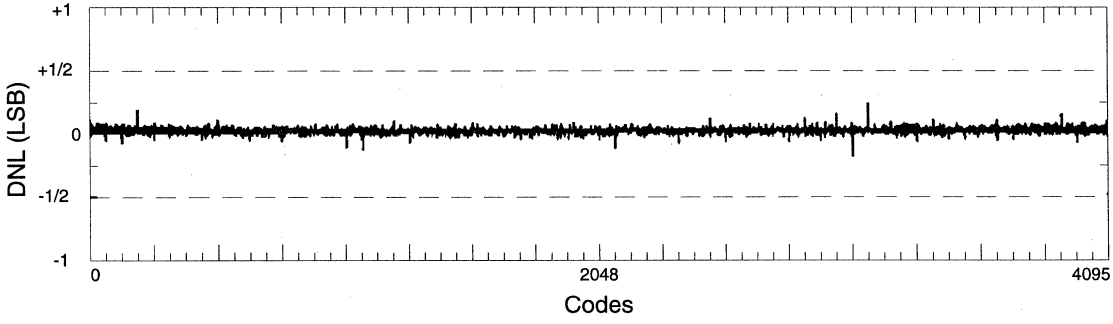
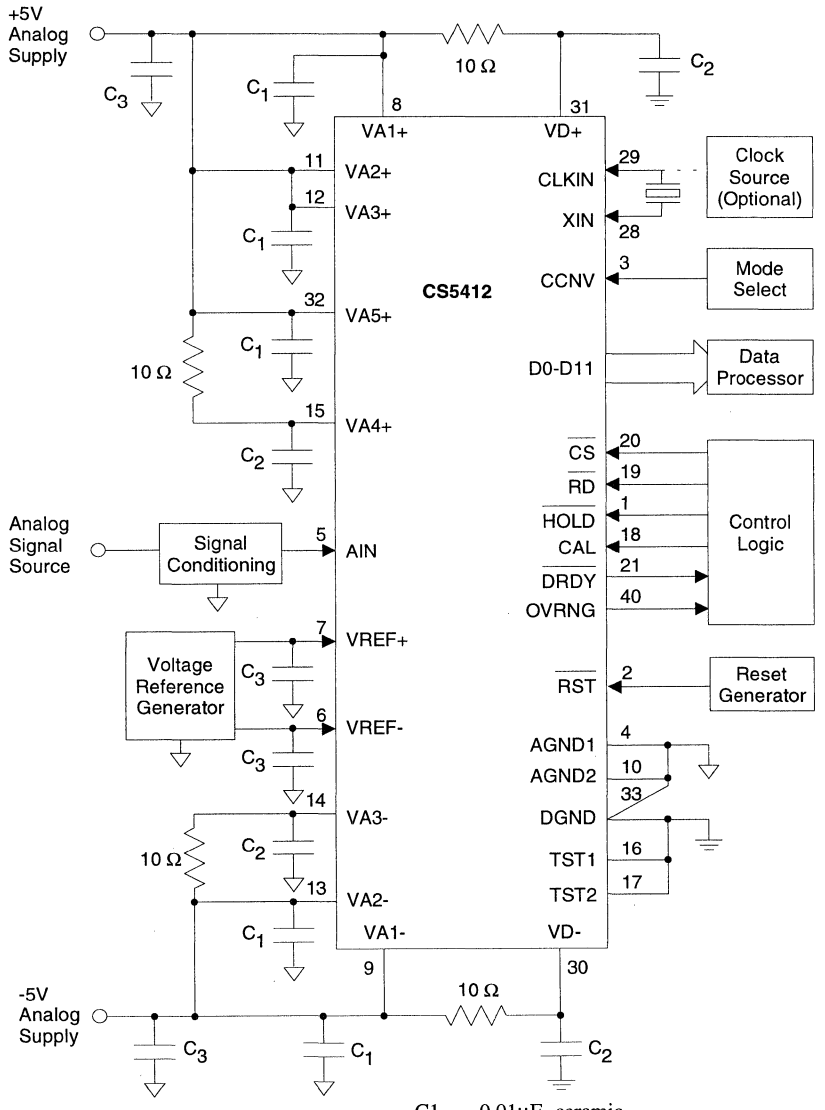


Figure 8. Typical CS5412 Differential Non-Linearity Plot

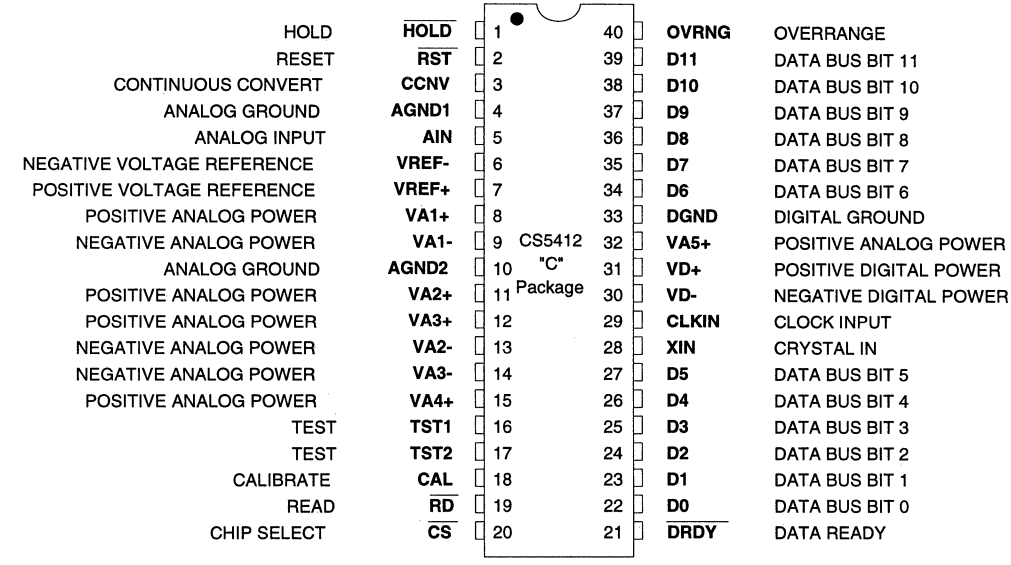


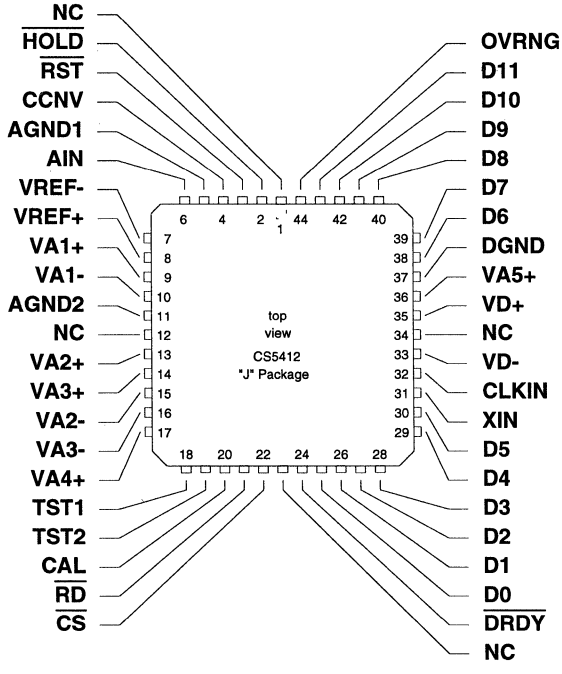
*VA2+ and VA5+ must be externally connected.

C1 - 0.01µF ceramic
C2 - 0.01µF in parallel with 0.1µF ceramic
C3 - 0.1µF ceramic in parallel with 3.3 µF tantalum

Figure 9. System Connection Diagram.

PIN DESCRIPTIONS





Power Supply Connections

VD+ - Positive Digital Power, PIN 31.
Positive digital supply voltage. Nominally +5 volts.

VD- - Negative Digital Power, PIN 30.
Negative digital supply voltage. Nominally -5 volts.

DGND - Digital Ground, PIN 33.
Digital ground reference.

VA+ - Positive Analog Power, PINS 8, 11, 12, 15, 32.
Positive analog supply voltage. Nominally +5 volts. Positive supplies must be active and stable prior to application of the negative supplies. Positive supplies must remain active and stable until negative supplies have been removed during power-down.

VA- - Negative Analog Power, PINS 9, 13, 14.
Negative analog supply voltage. Nominally -5 volts.

AGND - Analog Ground, PIN 4, 10.
Analog ground reference.

Oscillator

CLKIN; XIN - Clock In, PIN 29; Crystal In, PIN 28.
Used to generate the internal master clock. A crystal can be tied across the two pins or an external CMOS-compatible clock can be driven into CLKIN if XIN is left floating.

Digital Inputs

$\overline{\text{HOLD}}$ - Hold Input, PIN 1.
A negative transition on $\overline{\text{HOLD}}$ puts the track-and-hold amplifier into the hold state and initiates the conversion sequence. Conversions must be synchronized with the master clock at $f_{CLK}/8N$ where N = 1,2,3. The $\overline{\text{HOLD}}$ input is CMOS-compatible.

CCNV - Continuous Convert, PIN 3.
When held high throughput will proceed at $1/8^{th}$ the master clock frequency. The $\overline{\text{HOLD}}$ pin can be high or low but must not transition.

$\overline{\text{CS}}$ - Chip Select, PIN 20.
Activates the $\overline{\text{RD}}$ and CAL inputs. When $\overline{\text{CS}}$ is high, these inputs have no effect and the data bus (D0 through D11) is held in a high impedance state.

$\overline{\text{RD}}$ - Read, PIN 19.
When held low with $\overline{\text{CS}}$ also low, enables D0-D11.

Note: Pin numbers are for the DIP package.

$\overline{\text{RST}}$ - Reset, PIN 2.

When $\overline{\text{RST}}$ transitions from low to high a full calibration is started 13 master clock cycles later indicated by OVRNG going high. OVRNG will return low when calibration is finished. Calibration takes 6,052,445 master clock cycles.

CAL - Calibrate, PIN 18.

Same as $\overline{\text{RST}}$ except it it logically inverted and enabled by $\overline{\text{CS}}$ going low .

Analog Inputs

VREF+ - Positive Voltage Reference, PIN 7.

Represents positive full scale voltage. Typically +1.5V with respect to AGND (bipolar system) or +3V with respect to AGND and VREF- (unipolar system).

VREF- - Negative Voltage Reference, PIN 6.

Represents negative full scale voltage. Typically -1.5V with respect to AGND (bipolar system) or tied to AGND (unipolar system).

AIN - Analog Input, PIN 5.

Analog input to the track-and-hold amplifier.

Digital Outputs

OVRNG - Overrange, PIN 40.

Goes high if the sampled analog input voltage exceeds VREF+ or VREF-. OVRNG also goes high during calibration cycles and can therefore be used to indicate end of calibration.

$\overline{\text{DRDY}}$ - Data Ready, PIN 21.

Falls when new data is becoming available at the outputs. Returns high three master clock cycles later. Data should be retrieved on the rising edge of $\overline{\text{DRDY}}$.

Digital Input/Outputs

D0 through D11 - Data Bus, PINS 22 thru 27, 34 thru 39.

Three-state data bus where D11 is the MSB and D0 is the LSB. The output coding is binary for unipolar and offset binary for bipolar.

Miscellaneous Pins

TST1 - Test, PIN 16.

Reserved for factory use. Must be tied to DGND for proper device operation.

TST2 - Test, PIN 17.

Reserved for factory use. Must be tied to DGND for proper device operation.

Note: Pin numbers are for the DIP package.

DEFINITIONS

Peak Harmonic or Spurious Noise (More accurately, Signal to Peak Harmonic or Spurious Noise) - The ratio of the rms value of the signal to the rms value of the next largest spectral component below the Nyquist rate (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Expressed in decibels.

Total Harmonic Distortion - Ratio of the rms sum of all harmonics to the rms value of of the signal. Units in percent.

Signal-to-(Noise plus Distortion) - Ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (excepting dc). Expressed in decibels.

Linearity Error - The deviation of the worst code width center, out of all 4096 codes, from a straight line. The straight line is determined by using a least squares fit algorithm from the measured points. Units in LSB's.

Differential Nonlinearity - The deviation of a code's width from the ideal width. Units in LSB's.

Full Scale Error - The deviation of the last code transition from the ideal (VREF+ - 1 LSB). Units in LSB's.

Offset Error - The deviation of the first code transition from the ideal (VREF- + 1 LSB). Units in LSB's.

Aperture Time - The time required after the hold command is issued for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter - The range of variation in the aperture time. Effectively a "sampling window" which ultimately dictates the maximum input slew rate acceptable for a given accuracy. Units in picoseconds.

Ordering Guide

Model	Convert Rate	SINAD	Linearity Error	Temp Range	Package
CS5412-JC1	1 MHz	65 dB	± 2.0 LSB	0 to 70 °C	40-Pin Ceramic SB DIP
CS5412-JJ1	1 MHz	65 dB	± 2.0 LSB	0 to 70 °C	44-Pin J Lead CLCC
CS5412-KC1	1 MHz	68 dB	± 1.0 LSB	0 to 70 °C	40-Pin Ceramic SB DIP
CS5412-KJ1	1 MHz	68 dB	± 1.0 LSB	0 to 70 °C	44-Pin J Lead CLCC
CS5412-AC1	1 MHz	65 dB	± 2.0 LSB	-40 to +85 °C	40-Pin Ceramic SB DIP
CS5412-BC1	1 MHz	68 dB	± 1.0 LSB	-40 to +85 °C	40-Pin Ceramic SB DIP
CS5412-SC1	1 MHz	65 dB	± 3.0 LSB	-55 to +125 °C	40-Pin Ceramic SB DIP
CS5412-TC1	1 MHz	68 dB	± 2.0 LSB	-55 to +125 °C	40-Pin Ceramic SB DIP
5962-9095702MQA	1 MHz	65 dB	± 3.0 LSB	-55 to +125 °C	40-Pin Ceramic SB DIP
5962-9095701MQA	1 MHz	68 dB	± 2.0 LSB	-55 to +125 °C	40-Pin Ceramic SB DIP
5962-9095702MXA	1 MHz	65 dB	± 3.0 LSB	-55 to +125 °C	44-Pin J Lead CLCC
5962-9095701MXA	1 MHz	68 dB	± 2.0 LSB	-55 to +125 °C	44-Pin J Lead CLCC

The following is a list of upgraded part numbers.

Discontinued Part Number	Equivalent Recommended Device
CS5412-SC1B	5962-9095702MQA
CS5412-TC1B	5962-9095701MQA
CS5412-SJ1B	5962-9095702MXA
CS5412-TJ1B	5962-9095701MXA

Semiconductor Corporation

CDB5412

CS5412 Evaluation Board

2

Features

- Throughout Rates to 1MHz
- Jumper Selectable
  Unipolar/Bipolar Input Range
  Continuous Conversion
- Buffered 12-Bit Data
- Optional Phase-Locked-Loop to Synchronize to Sampling Signal
- Adjustable Voltage Reference
- PC/uP-Compatible Header Connection

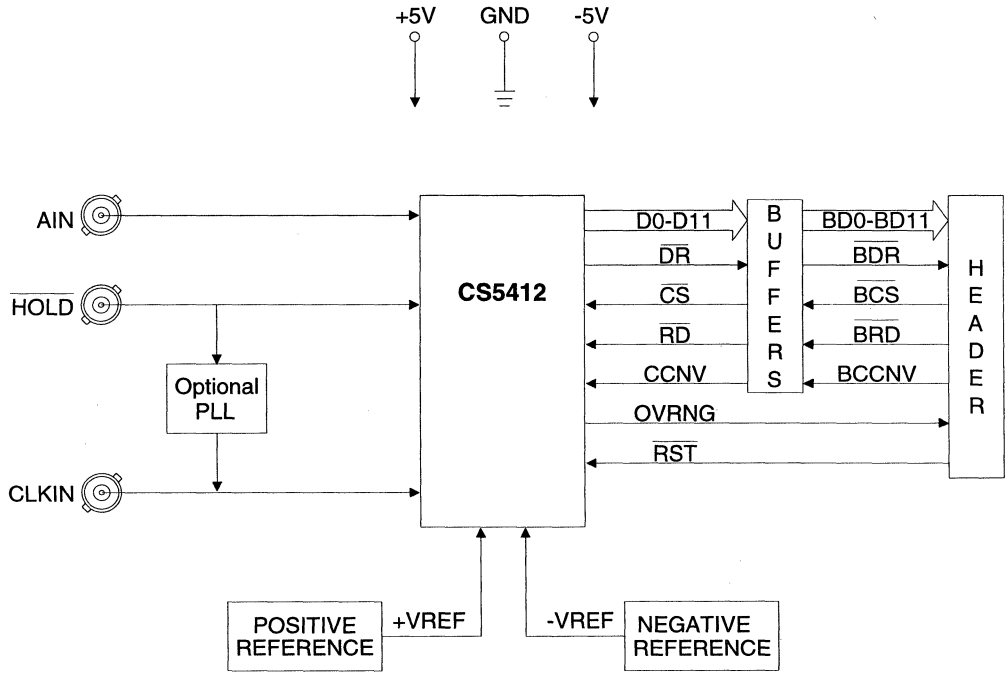
General Description

The CDB5412 is a completed, tested evaluation board for the CS5412 12-bit high-speed analog to digital converter. It includes a CS5412 and all of the components necessary to quickly and thoroughly verify the converter's performance under a wide variety of operating conditions.

On-board circuitry includes voltage references and clock circuitry, plus data buffers, so that the user need only supply power and an input signal to exercise the CS5412.

An on-board phase-locked-loop may be used to simulate systems that have a periodic sample clock not synchronized to a system clock, or where a clock 8 times the sampling clock is not available.

ORDERING INFORMATION: CDB5412



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

GENERAL DESCRIPTION

The CDB5412 Evaluation Board is a stand-alone environment for easy lab evaluation of the CS5412 High-Speed Analog-to-Digital Converter. Positive and negative references are included on the board and can be configured for ±1.5 volt bipolar or 0-to-3 volt unipolar operation. The digital output of the CS5412 is buffered and series terminated allowing the board to drive twisted-pair ribbon cable. The CDB5412 also includes an optional phase-locked-loop (PLL) that will generate the requisite master clock given a periodic sample clock. When supplied with the necessary +5 volt and -5 volt power supplies and an analog signal source, the CDB5412 will provide converted data at the 40 pin header.

The CDB5412 is designed to allow easy and thorough evaluation of the performance of the CS5412. The CDB5412 is a four layer board with one signal layer, two power planes, and a ground plane; the decoupling scheme is designed to insure accurate evaluation of the converter's performance for a wide variance in the quality of the power supplies.

The CDB5412 can also be used as a performance benchmark when designing your own system, and for ideas on appropriate layout schemes.

Before starting an evaluation, we strongly recommend reviewing the CS5412 data sheet. A thorough understanding of the CS5412 will make it easier to quickly and fully evaluate the part.

Suggested Evaluation Method

One efficient method of dynamically evaluating the CS5412 using the CDB5412 is to connect AIN to a spectrally pure sine wave and collecting a consecutive number of samples. FFT analysis can then be done on the samples to produce signal-to-noise and signal-to-distortion ratios.

Equipment needed consist of the following:

- CDB5412 Evaluation Board
- Good split power supply capable of supplying +5V and -5V.
- A spectrally pure sine wave generator such as the Krohn-Hite Model 4400A "Ultra-Low Distortion Oscillator"
- High-speed data storage
- Computer/PC capable of acquiring data from high-speed data storage
- A software routine to perform a Fast Fourier Transform (FFT)

The sine-wave generator supplies the analog signal, AIN, to the CDB5412. Converted data will appear at the header since the board is, by default, in the continuous convert mode.

The header is connected to the high-speed storage. This storage can consist of FIFO's, or static RAM and counters, or a logic analyzer with the ability to transfer data to a computer or PC. If FIFO's or static RAMs are employed, and a PC is the host computer, a data acquisition board such as the Metrabyte Model PIO12 "24 Bit Parallel Digital I/O Interface" can be used to transfer the data to the PC. If the input signal is not synchronized with the sample frequency so that an integer number of periods is acquired, the data must be windowed to avoid end point discontinuities. We use the Blackman-Harris window which forces the endpoints to zero. An FFT analysis on the resulting data will yield spectral information on the converter. Figure 1 graphically illustrates the results of such analysis. For Figure 1, 1024 consecutive samples were taken with the CDB5412 sampling a 100kHz sine wave input at 1 MHz. The samples were modified by the Blackman-Harris window before FFT analysis.

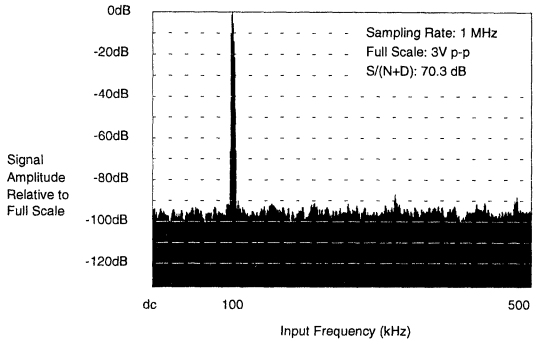


Figure 1. Typical CS5412 FFT Performance

References:
F.J. HARRIS, "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transfer", Proc. IEEE, Vol. 66, No. 1, Jan. 1978, pp. 51-83 .

G.D. BERGLAND & M.T. DOLAN, "Fast Fourier Transform Algorithms", Programs for Digital Signal Processing, IEEE Press: 0-87942-127-4, Section 1.2.

BOARD DESCRIPTION

MODES

Continuous Convert

The default mode for the CDB5412 is continuous convert (CCNV) active with the PLL inactive. Therefore, the CS5412 is always converting and the $\overline{\text{HOLD}}$ signal is not used. The part can be taken out of continuous convert mode in one of two ways, either by placing a strap jumper on J6 or by driving BCCNV at the stake header low. Once out of continuous convert mode, the $\overline{\text{HOLD}}$ signal must be driven. $\overline{\text{HOLD}}$ is described in greater detail in the "Inputs" section.

Unipolar/Bipolar

The CDB5412 board is factory calibrated for bipolar mode (AIN = ±1.5 Vpeak). In bipolar mode, strap jumpers are placed on J3 and J5 (both marked with a "B") which are located in the Negative Reference, Figure 2, and the Positive Reference, Figure 3.

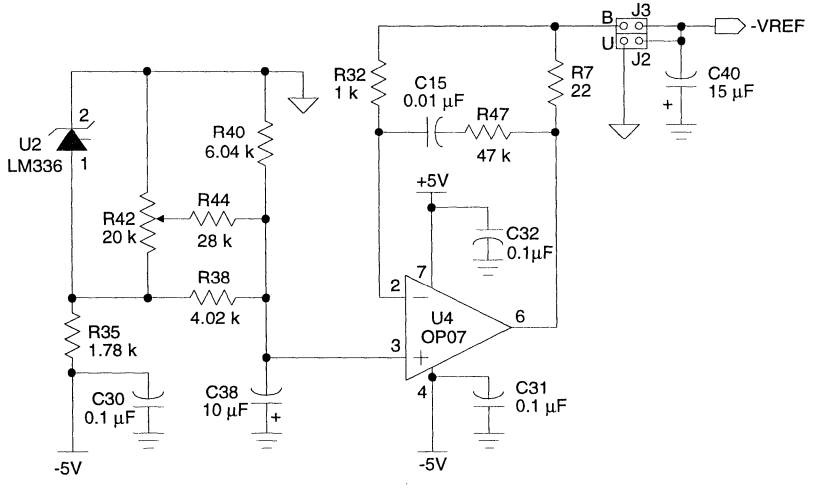


Figure 2. Negative Reference

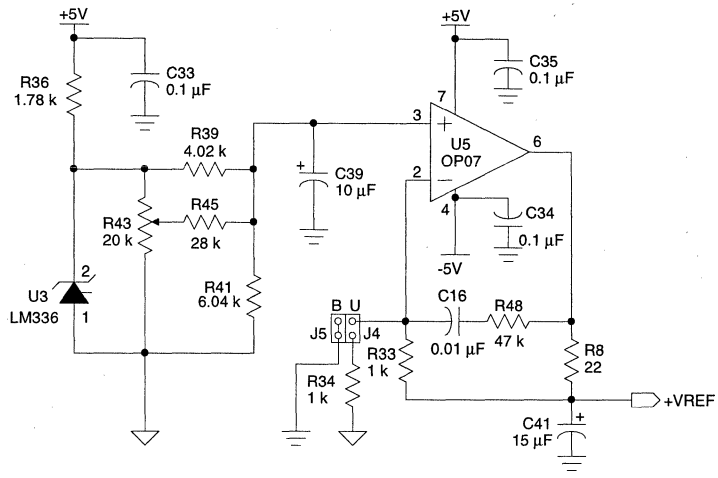


Figure 3. Positive Reference

To operate the board in unipolar mode (AIN = AGND to +3 Vpeak), move the strap jumpers to J2 and J4 (both marked with a "U"). The positive reference pot, R43, must be calibrated to +3.000 volts at +VREF (pin 7) of the CS5412 converter.

When receiving a new board, Crystal recommends that the reference voltages, +VREF and -VREF, be verified before operation. The pots located in their respective reference section may be tweaked to calibrate the voltage level which should be measured at the CS5412 converter.

Calibration

Since the Reset switch provides a means to calibrate the part, the CAL pin is hard-wired to ground through jumper J1. The reset signal is also available at the stake header and can be driven by any source that can drive a 1 kΩ resistor connected to +5 volts (see Figure 5).

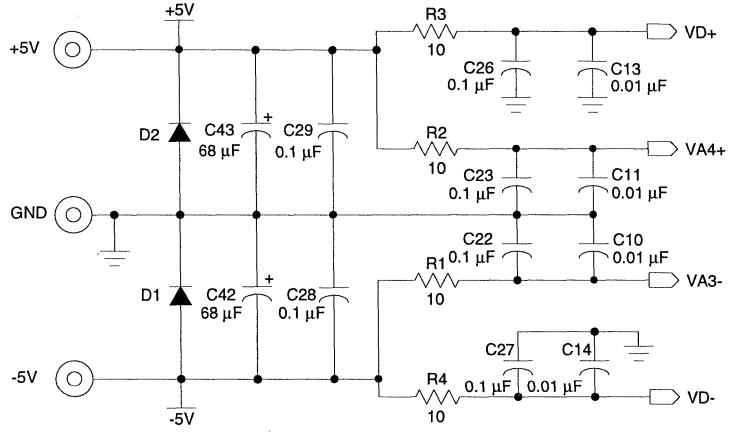


Figure 4. Power Supply

INPUTS

Power Supplies

A split supply should be used to generate +5 volts and -5 volts. These should be connected to their respective banana jacks on the board. A good quality low ripple, low noise supply will give the best performance.

Figure 4 depicts power supply decoupling for the CDB5412, along with decoupling for the digital supplies and the isolated analog supplies, both of which are low-pass filtered to prevent noise from coupling into the analog supplies. Since the digital supply is derived from the analog supply, the digital supply is guaranteed to be less than or equal to the analog supply as specified in the CS5412 data sheet.

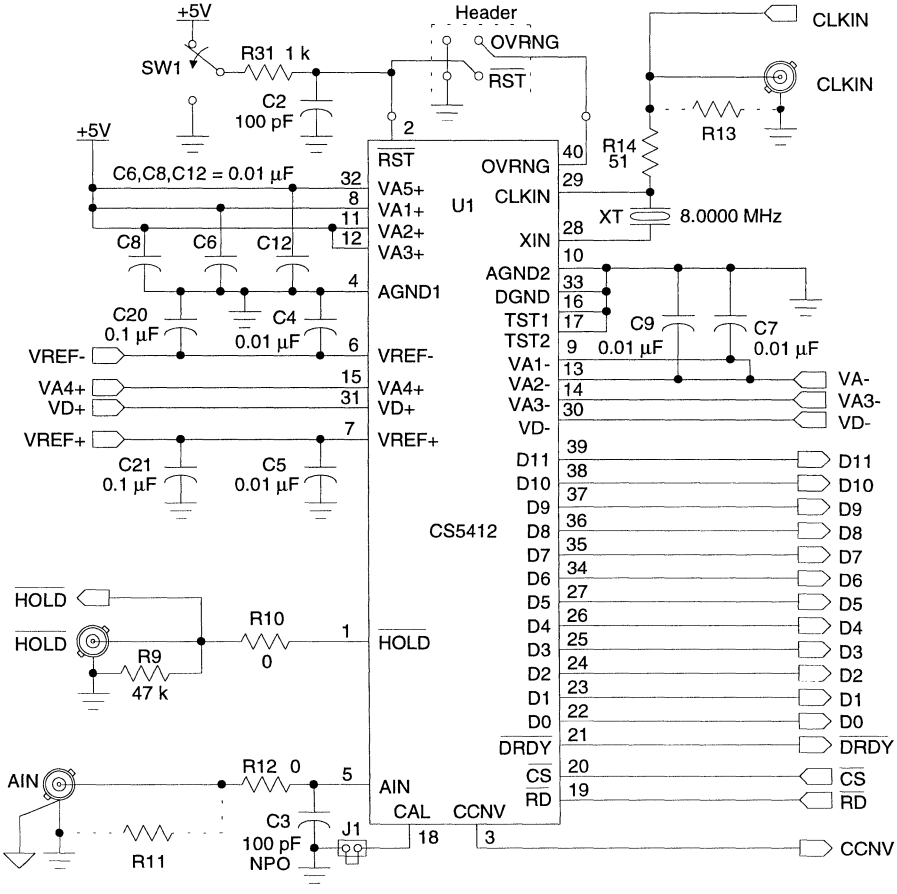


Figure 5. 5412 Flash A/D Converter

Analog In -AIN

The factory setting for AIN is a shorting wire in R12 and an NPO capacitor, C3, to ground. If the input signal is noisy, the shorting wire should be replaced with an appropriate resistor to low-pass filter the input noise.

In addition to the input filtering capability, R11 is available for impedance matching. If the source driving AIN has low impedance, an appropriate termination resistor should be soldered in R11. (see Figure 5.)

Clock -CLKIN

The CDB5412 has an 8.0000 MHz crystal installed at the factory which generates a sample frequency of 1 MHz. If another sample frequency is desired, either replace the crystal or remove the crystal from its socket and use the CLKIN BNC to generate other master clock frequencies. R14 provides series termination of 51 Ω. R13 may be used for parallel termination but must be left open for the crystal to oscillate (factory setting). CLKIN can also be generated by the on-board PLL. The PLL, when active, will generate a CLKIN frequency eight times the frequency of the $\overline{\text{HOLD}}$ signal. For more information on the PLL, see the "Phase-Locked- Loop" section.

Hold -$\overline{\text{HOLD}}$

As described in the Continuous Convert section, the CDB5412 is factory set not to use the $\overline{\text{HOLD}}$ input. Driving the $\overline{\text{HOLD}}$ input while the CS5412 is in the continuous convert mode will give erratic results. To use the $\overline{\text{HOLD}}$ signal, the CCNV signal must be driven low by placing a strap jumper on J6 or by driving the BCCNV signal at the stake header low. As described in the CS5412 data sheet, the $\overline{\text{HOLD}}$ signal must be modulo eight and synchronized to the master clock, CLKIN.

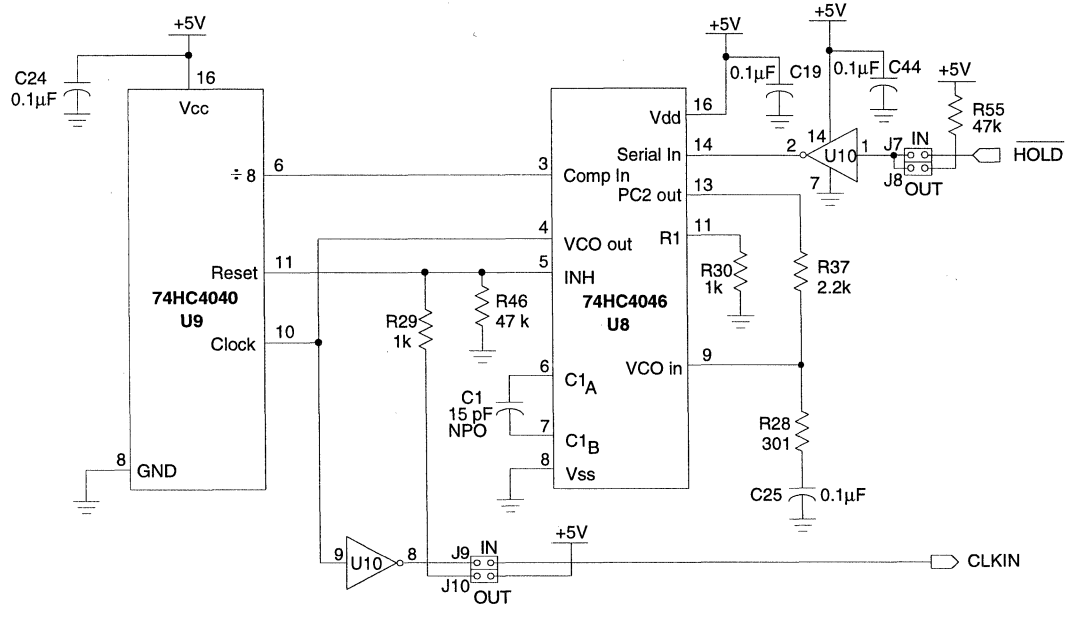


Figure 6. Phase-Locked-Loop

Since $\overline{\text{HOLD}}$ must not be left floating, the factory configuration is a shorting wire in R10 (series termination) and a 47k Ω resistor (R9) to ground. This configuration ties $\overline{\text{HOLD}}$ to ground (through R9) and provides fairly high impedance when driving $\overline{\text{HOLD}}$ externally.

If the signal source used to drive $\overline{\text{HOLD}}$ is low impedance, R9 should be replaced with the appropriate resistor. R10 can provide series termination.

Phase-Locked-Loop - (PLL)

The CDB5412 contains an optional Phase-Locked-Loop (PLL) which can be used by systems containing a periodic sampling clock, $\overline{\text{HOLD}}$, but no master clock, CLKIN. The PLL generates a clock eight times the frequency of $\overline{\text{HOLD}}$ and the PLL drives the CLKIN pin.

The schematic for the PLL is shown in Figure 6. Shorting jumpers on J8 and J10 (both marked "OUT") disable the PLL (factory setting). To enable the PLL move the jumpers from J8 and J10 to J7 and J9 (both marked "IN"). Since the CLKIN pin is driven by the PLL, the on-board crystal should be removed and the CLKIN BNC must not be driven or loaded by an external source.

The PLL will not work with a sampling signal, $\overline{\text{HOLD}}$, that is not periodic. The PLL is designed to work with a $\overline{\text{HOLD}}$ signal range of 300 kHz to 1 MHz. To redesign the PLL for other frequencies see the National Semiconductor 74HC4046 PLL Data Sheet.

OUTPUTS

The 12 data bits output from the CS5412 are buffered as shown in Figures 7 and 8, which minimize loading of the converters outputs. Series resistors are then used to minimize ringing when connected to twisted-pair ribbon cable. The +5 volt supply for the buffers is derived from the analog supply using the same low-pass RC network used on the digital supplies of the CS5412.

Three of the signals at the stake header are inputs to the board (Figure 8). B$\overline{\text{CS}}$ and B$\overline{\text{RD}}$ are pulled down to ground through a resistor allowing the CS5412 to continually output data as soon as it becomes available. The third input is a buffered continuous convert signal, BCCNV. By default this signal is pulled up to +5 volts through a resistor, which configures the CS5412 to convert at one eighth the master clock frequency. (The $\overline{\text{HOLD}}$ BNC must not be driven in this mode.)

The 20 stake header pins opposite the signal names are all tied to ground. Signals with a "B" prefix indicate buffered signals. The "X" and "Y" pins are unused and allow customization of the CDB5412 evaluation board.

Figure 9 illustrates the CDB5412 board layout to help in locating components.

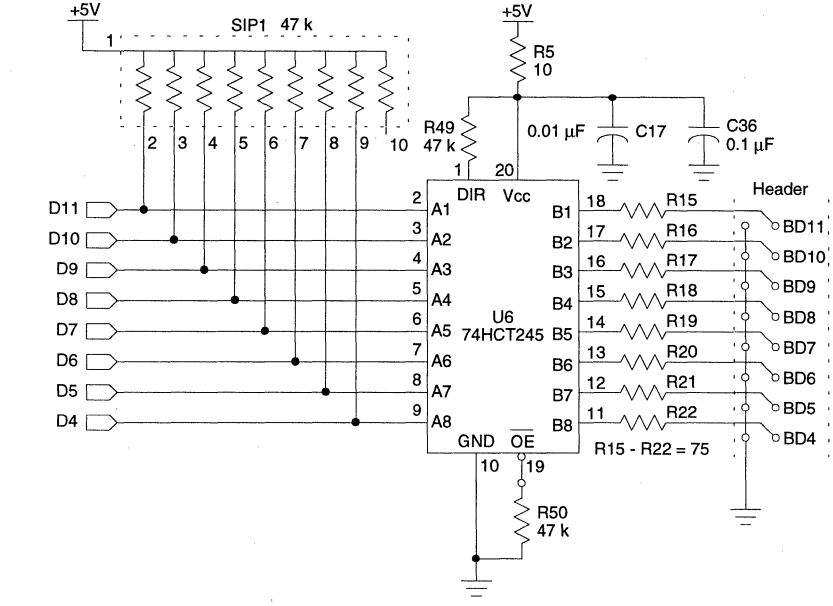


Figure 7. Upper Buffer

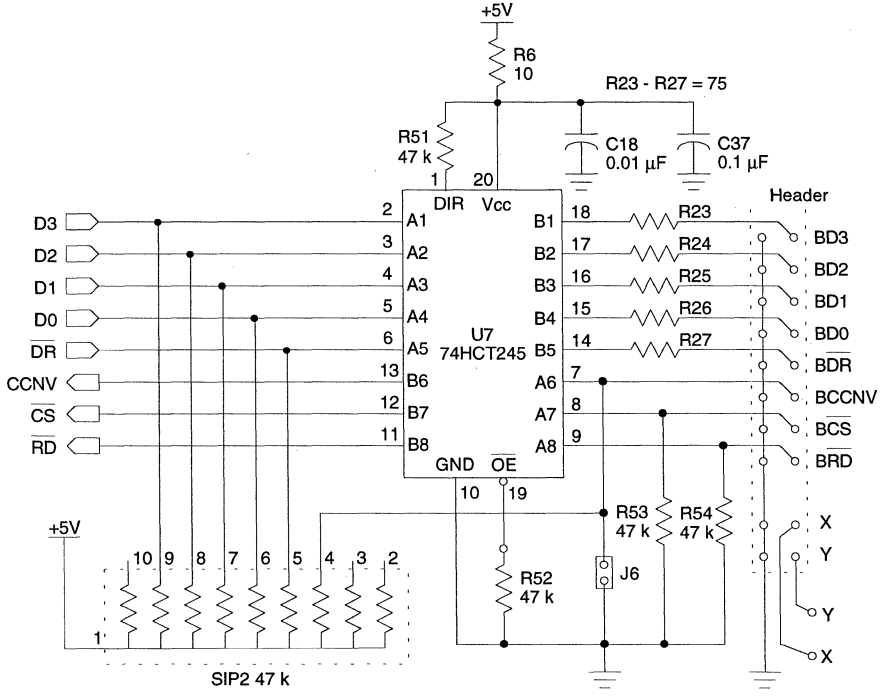


Figure 8. Lower Buffer

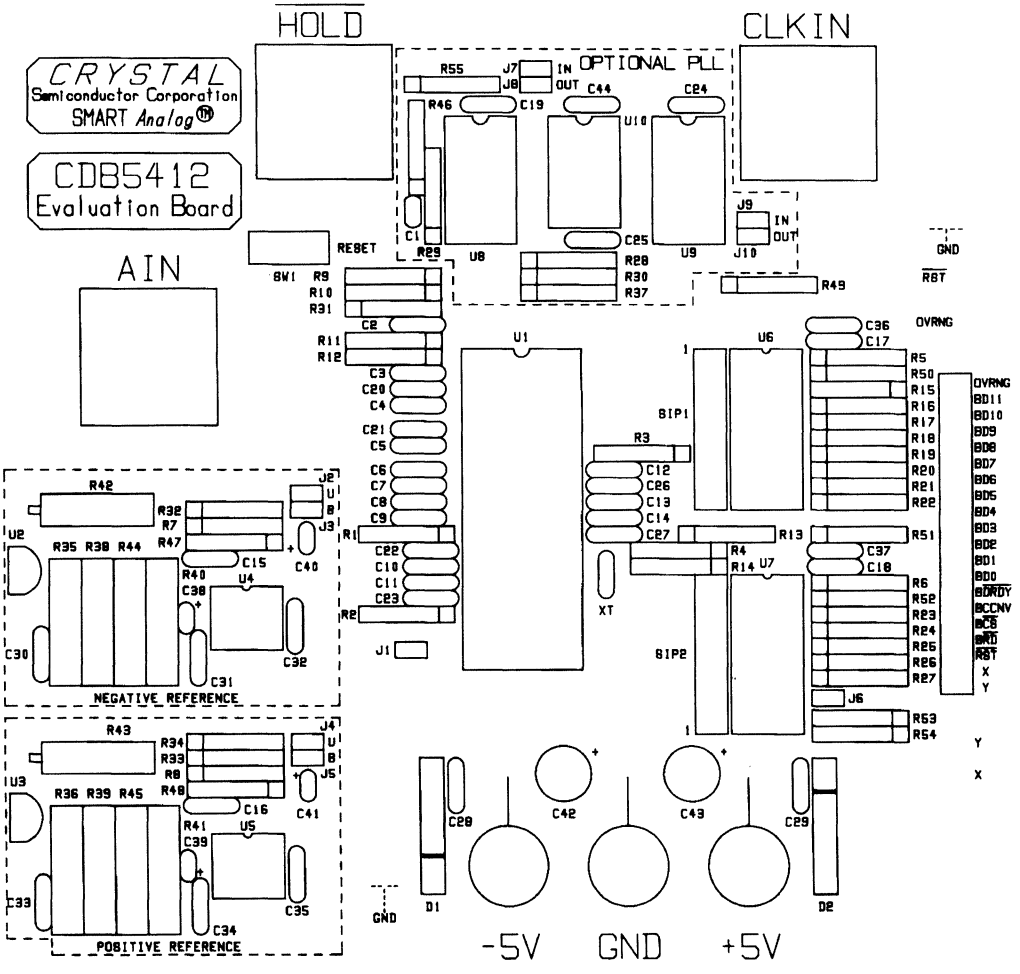


Figure 9. CDB5412 Board Layout

•Notes•

Semiconductor Corporation

CS5480

10-Bit, 40 MHz A/D Converter

2

Features

- Monolithic 40 MSPS CMOS ADC
  - On-chip Track/Hold
  - On-chip Voltage Reference
  - +5V Power Supply Only
- Dynamic performance (f_{in}=3.58MHz)
  - SNR: 56 dB
  - THD: 63 dB
  - SFDR: 68 dB
- Analog Input Range:
  - Single-ended Input: $1.2V_{p-p}$
  - Differential Input: $2.4V_{p-p}$
- Low Power: 375 mW

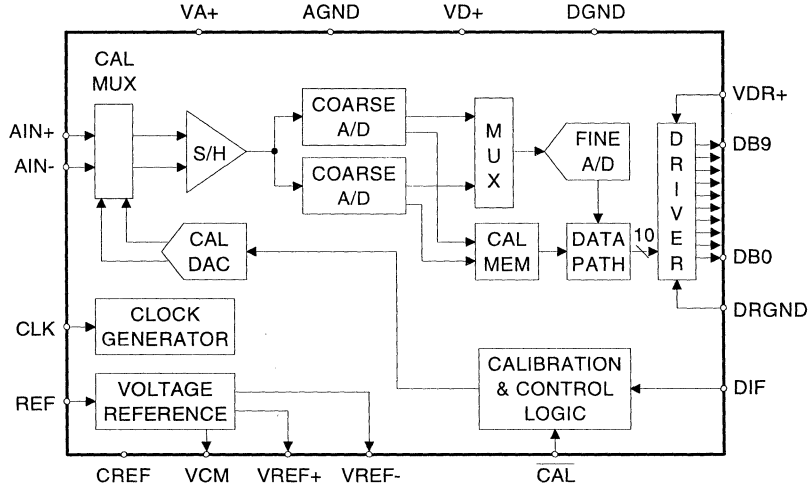
General Description

The CS5480 is a monolithic 10-bit sampling analog-to-digital converter capable of 40 MSPS conversion rate. To achieve high throughput, the CS5480 uses a fully pipelined architecture. Unique self-calibration circuitry ensures excellent linearity with no missing codes over the entire operating temperature range.

Digital inputs are CMOS and TTL compatible. Digital outputs are CMOS compatible. The analog input can be driven by either a differential 2.4 Vp-p signal, or a 1.2 Vp-p single-ended signal. Output data is available in offset binary format.

The CS5480 advanced CMOS construction provides low power consumption and the inherent reliability of monolithic devices.

For more information contact Crystal Semiconductor



Product Preview

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

ANALOG CHARACTERISTICS (T_A=T_{MIN} to T_{MAX}; VA+, VD+, VDR1+, VDR2+ = 5.0V; AGND=DGND=DRGND1=DRGND2=0V; CLK=40MHz; DIF=VD+; REF=+1.2V; C_L < 10pF)

Parameter*		Symbol	Min	Typ	Max	Units
Specified Temperature Range			-40	-	+85	°C
Resolution		RES	10	-	-	Bits
Accuracy						
Linearity Error	(Note 1)	INL	-	± 1	-	LSB
Differential Linearity Error	(Note 1)	DNL	-	± 1/2	-	LSB
No Missing Codes	(Note 1)	NMC	10	-	-	Bits
Offset Error	(Note 1)	V_{OS}	-	± 5	-	LSB
Full Scale Error	(Note 1)	FSE	-	± 1	-	% FS
Power Supplies						
DC Power Supply Currents	(Note 2)	IA+ ID+ IDR+	- - -	TBD TBD TBD	TBD TBD TBD	mA mA mA
Power Dissipation	(Note 2)	P_D	-	375	500	mW
Power Supply Rejection Ratio	(Note 3)	PSRR	-	70	-	dB
Analog Input						
Input Voltage Range	Single-ended Input Differential Input	AIN	- -	- -	1.2 2.4	V_{p-p} V_{p-p}
Input Capacitance		C_{IN}	-	10	-	pF
Analog Bandwidth		BW	-	200	-	MHz
Common Mode Rejection		CMR	-	40	-	dB
Reference Input						
Input Range		REF	0.6	1.2	1.3	V
Input Impedance		R_L	-	1	-	kΩ

Notes: 1. Applies after calibration at the temperature of interest
2. C_L=10pF typical.
3. f_{in}=1kHz

* Refer to the Specification Definitions immediately following the Pin Description section.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter*		Symbol	Min	Typ	Max	Units
Dynamic Performance						
Signal-to-(Noise plus Distortion)	(Note 1)	SINAD				
f_{in} = 1.24 MHz			-	57	-	dB
f_{in} = 3.58 MHz			-	56	-	dB
f_{in} = 10.3 MHz			-	54	-	dB
Total Harmonic Distortion	(Note 1)	THD				
f_{in} = 1.24 MHz			-	-63	-	dB
f_{in} = 3.58 MHz			-	-63	-	dB
f_{in} = 10.3 MHz			-	-60	-	dB
Effective Number of Bits	(Note 1)	ENOB				
f_{in} = 1.24 MHz			-	9.3	-	Bits
f_{in} = 3.58 MHz			-	9.0	-	Bits
f_{in} = 10.3 MHz			-	8.7	-	Bits
Signal-to-Noise	(Note 1)	SNR				
f_{in} = 1.24 MHz			-	58	-	dB
f_{in} = 3.58 MHz			-	56	-	dB
f_{in} = 10.3 MHz			-	54	-	dB
Spurious Free Dynamic Range	(Note 1)	SFDR	-	68	-	dBc
Differential Phase	(Note 1)	DP	-	1	-	°
Differential Gain	(Note 1)	DG	-	1	-	%
Intermodulation Distortion	(Notes 1, 4)	IMD	-	60	-	dB
2^{nd} Harmonic Distortion	(Note 1)					
f_{in} = 1.24 MHz			-	71	-	dB
f_{in} = 3.58 MHz			-	68	-	dB
f_{in} = 10.3 MHz			-	60	-	dB
3^{rd} Harmonic Distortion	(Note 1)					
f_{in} = 1.24 MHz			-	71	-	dB
f_{in} = 3.58 MHz			-	68	-	dB
f_{in} = 10.3 MHz			-	63	-	dB
Overvoltage Recovery Time		t_{ovr}	-	25	-	ns

Note: 4. Tested with input signals of 1MHz and 1.05MHz.

* Refer to the Specitication Definitions immediately following the Pin Description section.

Specifications are subject to change without notice.

DIGITAL CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+, VD+, VDR1+, VDR2+ = 5V± 5%; AGND=DGND=DRGND1=DRGND2=0V, Measurements performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage	V_{OH}	(VD+)-0.3	-	-	V
Low-Level Output Voltage	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{LKG}	-	-	± 10	µA
Digital Input Capacitance	C_{IN}	-	10	-	pF
Digital Output Capacitance	C_{OUT}	-	10	-	pF

RECOMMENDED OPERATING CONDITIONS (AGND, DGND, DRGND1, DRGND2 = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Analog	VA+	4.75	5.0	5.25	V
	Positive Digital	VD+	4.75	5.0	5.25	V
	Positive Driver	VDR+	4.75	5.0	5.25	V
Analog Input Voltage	Single-ended	AIN	-	-	1.2	V_{p-p}
	Differential		-	-	2.4	V_{p-p}
Reference Voltage		REF	0.6	1.2	1.3	V

ABSOLUTE MAXIMUM RATINGS (AGND, DGND,DRGND1,DRGND2 = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies	Positive Digital	VD+	-0.3	-	6.0	V
	Positive Driver	VDR+	-0.3	-	6.0	V
	Positive Analog	VA+	-0.3	-	6.0	V
Input Current, Any Pin Except Supplies	(Note 5)	I_{in}	-	-	±10	mA
Output Current		I_{out}	-	-	±25	mA
Power Dissipation (Total)	(Note 6)		-	-	1	W
Analog Input Voltage (AIN and VREF pins)		V_{INA}	(VA-)-0.3	-	(VA+)+0.3	V
Digital Input Voltage		V_{INL}	-0.3	-	(VL+)+0.3	V
Ambient Operating Temperature		T_A	-55	-	125	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes: 5. Transient currents of up to 100mA will not cause SCR latch-up. Maximum input current for a power supply pin is ± 50mA
6. Total power dissipation, including all input currents and output currents.

WARNING:Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+, VDR1+, VDR2+ = 5V± 5%; Input Levels: Logic 0 = 0V, Logic 1 = VL+; C_L <10pF

Parameter	Symbol	Min	Typ	Max	Units
Conversion Rate	$1/t_{conv}$	2	-	40	MHz
Clock Duty Cycle		40	-	60	%
Acquisition Time	t_{acq}	-	1	-	CLK
Pipeline Delay	t_{pd}	-	11	-	CLKs
Aperture Delay	t_{apd}	-	3	-	ns
Aperture Jitter	t_{apj}	-	5	-	ps_{rms}
Output Delay	t_{od}	-	10	-	ns
CLK falling to $\overline{CAL}$ falling	t_{sc}	2	-	-	CLKs
Start of Calibration to end of calibration	t_{cal}	-	800,000	-	CLKs

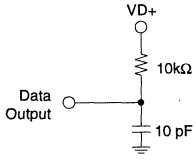


Figure 1. Load Circuit for timing tests

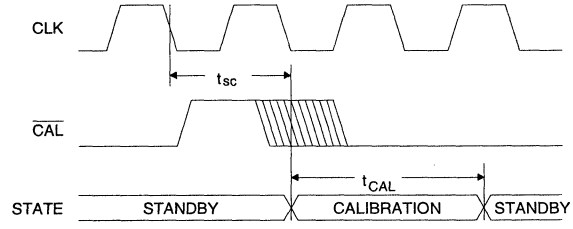


Figure 2. Calibration Timing

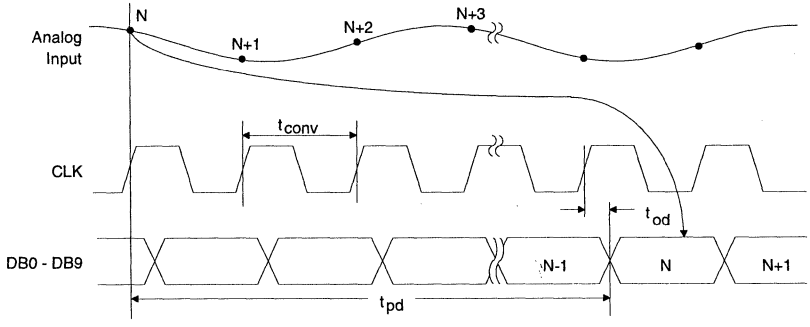
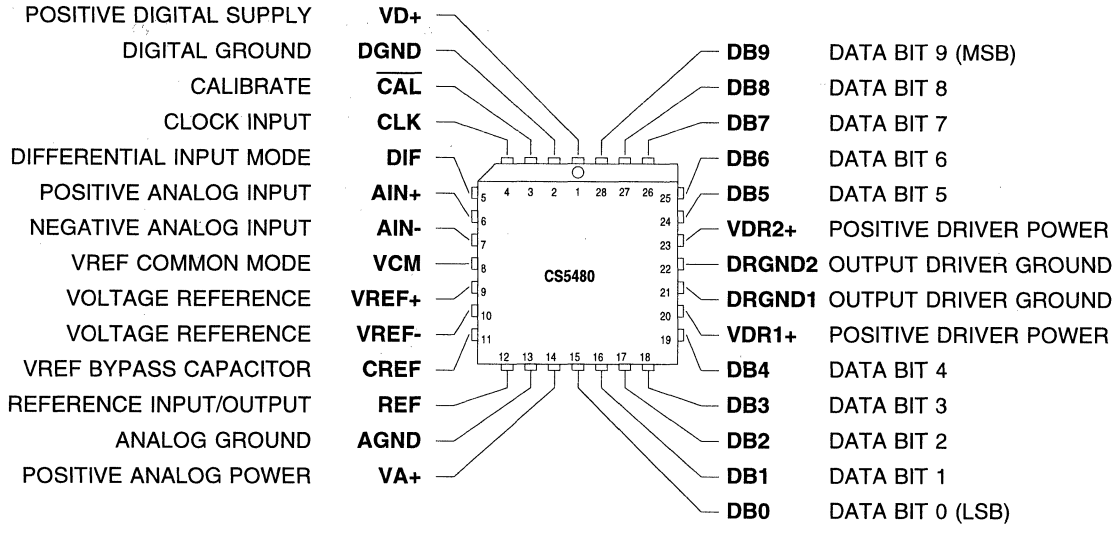


Figure 3. Timing Diagram

PIN DESCRIPTIONS



Power Supply Connections

VA+ - Positive Analog Power, PIN 14

Positive analog supply voltage. Nominally +5 volts.

VD+ - Positive Digital Power, PIN 1

Positive digital supply voltage. Nominally +5 volts.

VDR1+, VDR2+ - Positive Output Driver Power, PINS 20, 23

Positive output driver supply voltage. Nominally +5 volts.

AGND - Analog Ground, PIN 13

Analog ground reference.

DGND - Digital Ground, PIN 2

Digital ground reference.

DRGND1, DRGND2 - Output Driver Ground, PINS 21, 22

Output Driver ground reference.

Analog Inputs

AIN+, AIN- - Analog Input, PINS 6, 7

AIN+ is the positive analog input signal to the differential input of the T/H amplifier. AIN- is the negative analog input signal to the differential input of the T/H amplifier. AIN- is normally tied to VCM for single-ended operation.

Reference Connections

VCM - Voltage Reference Common Mode, PIN 8
Signal common, nominally 2.5 volts.

VREF+ - Positive Voltage Reference, PIN 9
Positive full-scale voltage, nominally 3.1 volts.

VREF- - Negative Voltage Reference, PIN 10
Negative full-scale voltage, nominally 1.9 volts.

CREF - Voltage Reference Bypass Capacitor, PIN 11
Internal voltage reference must be bypassed with a 0.1µF capacitor in parallel with a 1000pF ceramic chip capacitor to analog ground. No other external connection allowed.

REF - Reference Input/Output, PIN 12
Internal voltage reference output, or optional external voltage reference input. Taken with respect to AGND represents the full-scale input range. Nominally 1.2 volts.

Digital Inputs

$\overline{\text{CAL}}$ - Calibrate, PIN 3
Calibration command. If brought low for 1 clock cycle or more, the CS5480 will reset and initiate an internal calibration. Calibrates for differential input signal (DIF=1) and single-ended input (DIF=0). Any spurious glitch on this pin may inadvertently place the chip in the calibration mode.

DIF - Differential Input Mode, PIN 5
With the DIF pin low, the device is configured for single-ended operation. With the DIF pin high, the device is configured for differential input operation.

Digital Outputs

DB0 through DB9 - Data Bus Outputs, PINS 15-19, 24-28
Data Bit 0 (LSB) through Data Bit 9 (MSB).

Clock Generator

CLK - Clock Input, PIN 4
A CMOS compatible clock must be input to the CLK pin to serve as the master clock for the device. A master clock must be present at all times to ensure proper operation of the device.

DEFINITIONS

Linearity Error - INL

The deviation of a code from a straight line passing through the endpoints of the transfer function after zero and gain errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in LSB's.

Differential Nonlinearity Error - DNL

The minimum resolution for which no missing codes is guaranteed. Units in LSB's.

Offset Error - V_{OS}

The deviation of the first code transition from the ideal (VREF- + 1LSB). Units in LSB's.

Full Scale Error - FSE

The deviation of the last code transition from the ideal (VREF- - 1LSB). Units in LSB's.

Signal-to-Noise - SNR

The ratio of the rms value of the signal, to the rms sum of all other spectral components (excepting dc and distortion terms). Expressed in decibels (dB).

Signal-to- (Noise plus Distortion) - SINAD

The ratio of the rms value of the signal, to the rms sum of all other spectral components (excepting dc), including distortion components. Expressed in decibels (dB).

Total Harmonic Distortion - THD

The ratio of the rms sum of the significant (2^{nd} through 5^{th}) harmonics, to the rms value of the signal. Expressed in decibels (dB) or percent (%).

Intermodulation Distortion - IMD

The ratio of the rms value of the larger of the two test frequencies, which are each 6dB down from full-scale, to the rms value of the largest 2^{nd} order and 3^{rd} order intermodulation component. Expressed in decibels (dB).

Effective Number of Bits - ENOB

A measure of ac linearity and is calculated from: ENOB = [(SNR - 1.76)/6.02]

Spurious Free Dynamic Range - SFDR

The ratio of the rms value of the signal, to the rms value of the next largest spectral component (excepting dc). This component is often an aliased harmonic. Units in percent (%) and decibels relative to the carrier (dBc).

Differential Phase - DP

The difference in the output phase of a small high frequency sine wave at two stated levels of a low frequency signal on which it is superimposed. Units in degrees.

Differential Gain - DG

The difference between the output amplitudes of a small high frequency sine wave at two stated levels of a low frequency signal on which it is superimposed. Units in percent (%).

Overvoltage Recovery Time - t_{ovr}

The time required for the ADC to recover to full accuracy after an analog signal 150% of full scale is reduced to 50% of the full-scale value. Units in nanoseconds.

Aperture Delay - t_{apd}

The time delay between the falling edge and the actual start of the HOLD mode in a Track and Hold function. Units in nanoseconds.

Aperature Jitter - t_{apj}

The range of variation in the aperature time. Effectively a "sampling window" which ultimately dictates the maximum input slew rate acceptable for a given accuarcy. Units in picoseconds.

Pipeline Delay - t_{pd}

The number of clock cycles between the initiation of the conversion process and the associated output data bit being available. Expressed in clock cycles.

Full Power Bandwidth

The input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input.

• Notes •

Semiconductor Corporation

CS5481

10-Bit, 20 MHz A/D Converter

2

Features

- Monolithic 20 MSPS CMOS ADC
  - On-chip Track/Hold
  - On-chip Voltage Reference
  - +5V Power Supply Only
- Dynamic Performance (f_{in}= 1.24 MHz):
  - SNR: 58 dB
  - THD: 63 dB
  - SINAD: 57 dB
- CMOS Outputs
- Analog Input Range:
  - Single-ended Input: $1.2V_{p-p}$
  - Differential Input: $2.4V_{p-p}$
- Low Power: 200 mW

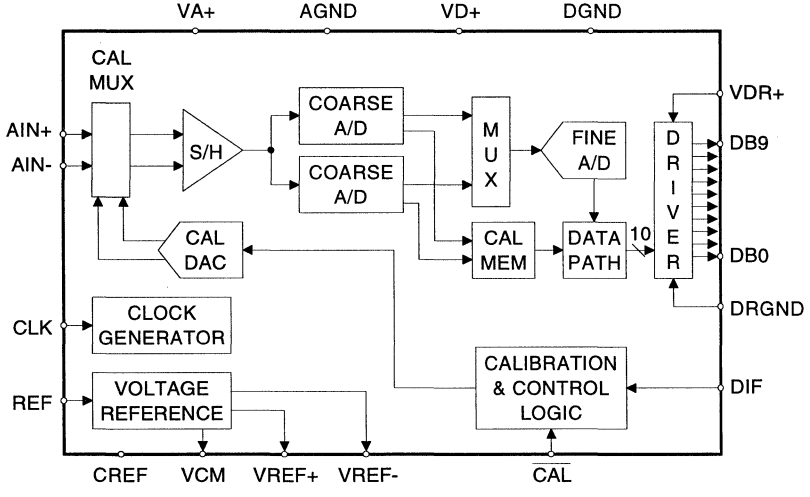
General Description

The CS5481 is a monolithic 10-bit sampling analog-to-digital converter capable of 20 MSPS conversion rate. To achieve high throughput, the CS5481 uses a fully pipelined architecture. Unique self-calibration circuitry ensures excellent linearity with no missing codes over the entire operating temperature range.

Digital inputs are CMOS and TTL compatible. Digital outputs are CMOS compatible. The analog input can be driven by either a differential 2.4 Vp-p signal, or a 1.2 Vp-p single-ended signal. Output data is available in offset binary format.

The CS5481 advanced CMOS construction provides low power consumption and the inherent reliability of monolithic devices.

For more information contact Crystal Semiconductor



Product Preview

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

ANALOG CHARACTERISTICS (T_A=T_{MIN} to T_{MAX}; VA+, VD+, VDR1+, VDR2+ = 5.0V; AGND=DGND=DRGND1=DRGND2=0V; CLK=20MHz; DIF=VD+; REF=+1.2V; C_L < 10pF)

Parameter*		Symbol	Min	Typ	Max	Units
Specified Temperature Range			-40	-	+85	°C
Resolution		RES	10	-	-	Bits
Accuracy						
Linearity Error	(Note 1)	INL	-	± 1	-	LSB
Differential Linearity	(Note 1)	DNL	-	± 1/2	-	LSB
No Missing Codes	(Note 1)	NMC	10	-	-	Bits
Offset Error	(Note 1)	V_{OS}	-	± 5	-	LSB
Full Scale Error	(Note 1)	FSE	-	± 1	-	% FS
Power Supplies						
DC Power Supply Currents	(Note 2)	IA+ ID+ IDR+	- - -	TBD TBD TBD	TBD TBD TBD	mA mA mA
Power Dissipation	(Note 2)	P_D	-	TBD	200	mW
Power Supply Rejection Ratio	(Note 3)	PSRR	-	70	-	dB
Analog Input						
Input Voltage Range	Single-ended Input Differential Input	AIN	- -	- -	1.2 2.4	V_{p-p} V_{p-p}
Input Capacitance		C_{IN}	-	10	-	pF
Analog Bandwidth		BW	-	200	-	MHz
Common Mode Rejection		CMR	-	40	-	dB
Reference Input						
Input Range		REF	0.6	1.2	1.3	V
Input Impedance		R_L	-	1	-	kΩ

Notes: 1. Applies after calibration at the temperature of interest
2. C_L=10pF typical.
3. f_{in}=1kHz

* Refer to the Specification Definitions immediately following the Pin Description section.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter*		Symbol	Min	Typ	Max	Units
Dynamic Performance						
Signal-to-(Noise plus Distortion)	(Note 1)	SINAD				
f_{in} = 1.24 MHz			-	57	-	dB
f_{in} = 3.58 MHz			-	56	-	dB
Harmonic Distortion	(Note 1)	THD				
f_{in} = 1.24 MHz			-	63	-	dB
f_{in} = 3.58 MHz			-	63	-	dB
Effective Number of Bits	(Note 1)	ENOB				
f_{in} = 1.24 MHz			-	9.2	-	Bits
f_{in} = 3.58 MHz			-	9.0	-	Bits
Signal-to-Noise	(Note 1)	SNR				
f_{in} = 1.24 MHz			-	58	-	dB
f_{in} = 3.58 MHz			-	56	-	dB
Spurious Free Dynamic Range	(Note 1)	SFDR	-	68	-	dBc
Differential Phase	(Note 1)	DP	-	1	-	°
Differential Gain	(Note 1)	DG	-	1	-	%
Intermodulation Distortion	(Notes 1, 4)	IMD	-	60	-	dB
Overvoltage Recovery Time		t_{ovr}	-	100	-	ns

Note: 4. Tested with input signals of 1MHz and 1.05MHz.

* Refer to the Specitication Definitions immediately following the Pin Description section.

Specitfications are subject to change without notice.

DIGITAL CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+, VD+, VDR1+, VDR2+ = 5V± 5%; AGND=DGND=DRGND1=DRGND2=0V, Measurements performed under static conditions.)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
High-Level Output Voltage	V_{OH}	(VD+)-0.3	-	-	V
Low-Level Output Voltage	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{LKG}	-	-	± 10	µA
Digital Input Capacitance	C_{IN}	-	10	-	pF
Digital Output Capacitance	C_{OUT}	-	10	-	pF

RECOMMENDED OPERATING CONDITIONS (AGND, DGND, DRGND1, DRGND2 = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies	Positive Analog	VA+	4.75	5.0	5.25	V
	Positive Digital	VD+	4.75	5.0	5.25	V
	Positive Driver	VDR+	4.75	5.0	5.25	V
Analog Input Voltage	Single-ended	AIN	-	-	1.2	V_{p-p}
	Differential		-	-	2.4	V_{p-p}
Reference Voltage		REF	0.6	1.2	1.3	V

ABSOLUTE MAXIMUM RATINGS (AGND, DGND,DRGND1,DRGND2 = 0V, all voltages with respect to ground.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies	Positive Digital	VD+	-0.3	-	6.0	V
	Positive Driver	VDR+	-0.3	-	6.0	V
	Positive Analog	VA+	-0.3	-	6.0	V
Input Current, Any Pin Except Supplies	(Note 5)	I_{in}	-	-	±10	mA
Output Current		I_{out}	-	-	±25	mA
Power Dissipation (Total)	(Note 6)		-	-	500	mW
Analog Input Voltage (AIN and VREF pins)		V_{INA}	(VA-)-0.3	-	(VA+)+0.3	V
Digital Input Voltage		V_{INL}	-0.3	-	(VL+)+0.3	V
Ambient Operating Temperature		T_A	-55	-	125	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Note: 5. Transient currents of up to 100mA will not cause SCR latch-up. Maximum input current for a power supply pin is ± 50mA
6. Total power dissipation, including all input currents and output curents.

WARNING:Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+, VDR1+, VDR2+ = 5V± 5%; Input Levels: Logic 0 = 0V, Logic 1 = VL+; C_L <10pF)

Parameter	Symbol	Min	Typ	Max	Units
Conversion Rate	$1/t_{conv}$	2	-	20	MHz
Clock Duty Cycle		40	-	60	%
Acquisition Time	t_{acq}	-	1	-	CLK
Pipeline Delay	t_{pd}	-	11	-	CLKs
Aperture Delay	t_{apd}	-	3	-	ns
Aperture Jitter	t_{apj}	-	5	-	ps_{rms}
Output Delay	t_{od}	-	10	-	ns
CLK falling to $\overline{CAL}$ falling	t_{sc}	2	-	-	CLKs
Start of Calibration to end of calibration	t_{cal}	-	800,000	-	CLKs

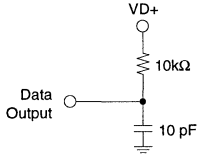


Figure 1. Load Circuit for timing tests

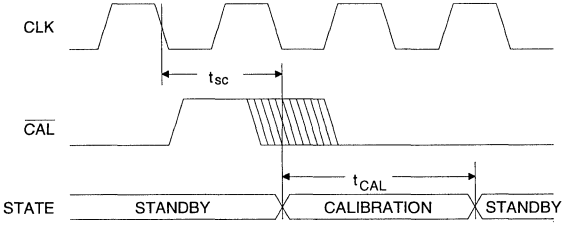


Figure 2. Calibration Timing

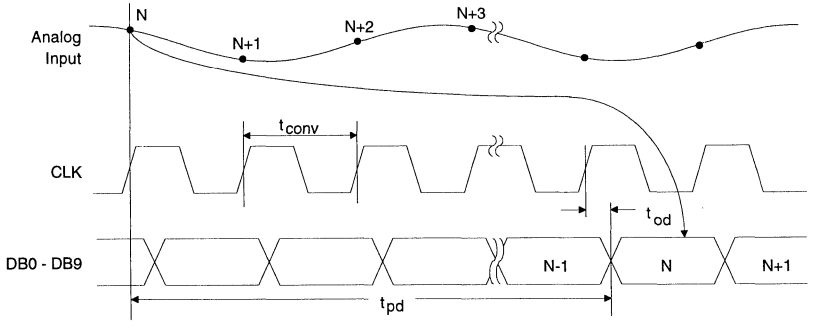
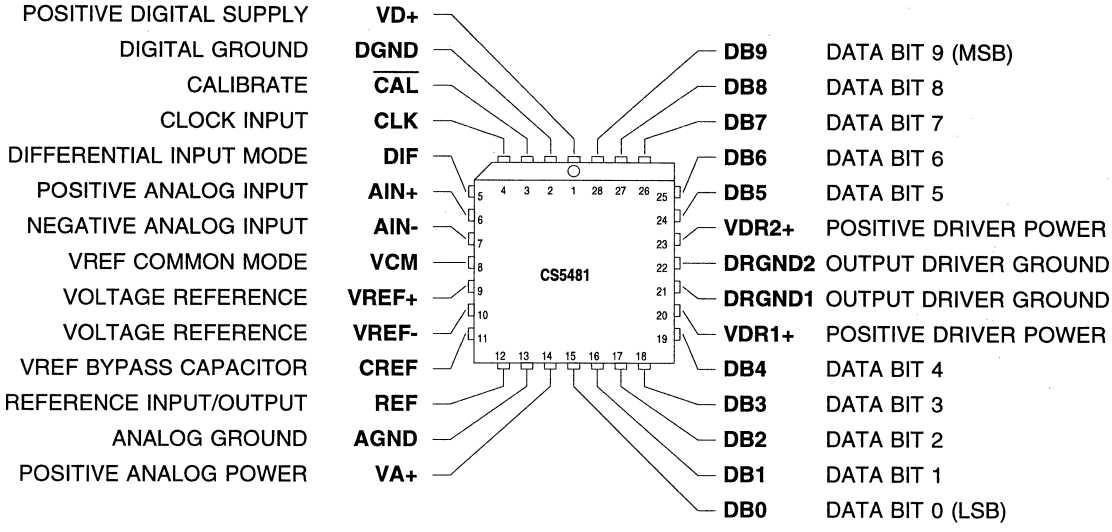


Figure 3. Timing Diagram

PIN DESCRIPTIONS



Power Supply Connections

VA+ - Positive Analog Power, PIN 14

Positive analog supply voltage. Nominally +5 volts.

VD+ - Positive Digital Power, PIN 1

Positive digital supply voltage. Nominally +5 volts.

VDR1+, VDR2+ - Positive Output Driver Power, PINS 20, 23

Positive output driver supply voltage. Nominally +5 volts.

AGND - Analog Ground, PIN 13

Analog ground reference.

DGND - Digital Ground, PIN 2

Digital ground reference.

DRGND1, DRGND2 - Output Driver Ground, PINS 21, 22

Output Driver ground reference.

Analog Inputs

AIN+, AIN- - Analog Input, PINS 6, 7

AIN+ is the positive analog input signal to the differential input of the T/H amplifier. AIN- is the negative analog input signal to the differential input of the T/H amplifier. AIN- is normally tied to VCM for single-ended operation.

Reference Connections

VCM - Voltage Reference Common Mode, PIN 8
Signal common, nominally 2.5 volts.

VREF+ - Positive Voltage Reference, PIN 9
Positive full-scale voltage, nominally 3.1 volts.

VREF- - Negative Voltage Reference, PIN 10
Negative full-scale voltage, nominally 1.9 volts.

CREF - Voltage Reference Bypass Capacitor, PIN 11
Internal voltage reference must be bypassed with a 0.1µF capacitor in parallel with a 1000pF ceramic chip capacitor to analog ground. No other external connections allowed.

REF - Reference Input/Output, PIN 12
Internal voltage reference output, or optional external voltage reference input. Taken with respect to AGND represents the full-scale input range. Nominally 1.2 volts.

Digital Inputs

$\overline{\text{CAL}}$ - Calibrate, PIN 3
Calibration command. If brought low for 1 clock cycle or more, the CS5481 will reset and initiate an internal calibration. Calibrates for differential input signal (DIF=1) or single-ended input (DIF=0). Any spurious glitch on this pin may inadvertently place the chip in the calibration mode.

DIF - Differential Input Mode, PIN 5
With the DIF pin low, the device is configured for single-ended operation. With the DIF pin high, the device is configured for differential input operation.

Digital Outputs

DB0 through DB9 - Data Bus Outputs, PINS 15-19, 24-28
Data Bit 0 (LSB) through Data Bit 9 (MSB).

Clock Generator

CLK - Clock Input, PIN 4
A CMOS compatible clock must be input to the CLK pin to serve as the master clock for the device. A master clock must be present at all times to insure proper operation of the device.

DEFINITIONS

Linearity Error - INL

The deviation of a code from a straight line passing through the endpoints of the transfer function after zero and gain errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code. Units in LSB's.

Differential Nonlinearity - DNL

The minimum resolution for which no missing codes is guaranteed. Units in LSB's.

Offset Error - V_{OS}

The deviation of the first code transition from the ideal (VREF- + 1LSB). Units in LSB's.

Full Scale Error - FSE

The deviation of the last code transition from the ideal (VREF- - 1LSB). Units in LSB's.

Signal-to-Noise - SNR

The ratio of the rms value of the signal, to the rms sum of all other spectral components (excepting dc and distortion terms). Expressed in decibels (dB).

Signal-to- (Noise plus Distortion) - SINAD

The ratio of the rms value of the signal, to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels (dB).

Total Harmonic Distortion - THD

The ratio of the rms sum of the significant (2^{nd} through 5^{th}) harmonics to the rms value of the signal. Expressed in decibels (dB) or percent (%).

Intermodulation Distortion - IMD

The ratio of the rms value of the larger of the two test frequencies, which are 6dB down from full-scale, to the rms value of the largest 2^{nd} order and 3^{rd} order intermodulation components. Expressed in decibels (dB).

Effective Number of Bits - ENOB

A measure of ac linearity and is calculated from: ENOB = [(SNR - 1.76)/6.02]

Spurious-Free-Dynamic-Range - SFDR

The ratio of the rms value of the signal, to the rms value of the next largest spectral component (excepting dc). This component is often an aliased harmonic. Units in percent (%) and decibels relative to the carrier (dBc).

Differential Phase - DP

The difference in the output phase of a small high frequency sine wave at two stated levels of a low frequency signal on which it is superimposed. Units in degrees.

Differential Gain - DG

The difference between the output amplitudes of a small high frequency sine wave at two stated levels of a low frequency signal on which it is superimposed. Units in percent (%).

Over voltage Recovery Time - t_{ovr}

The time required for the ADC to recover to full accuracy after an analog signal 150% of full scale is reduced to 50% of the full-scale value. Units in nanoseconds.

Aperture Delay - t_{apd}

The time delay between the falling edge and the actual start of the HOLD mode in a Track and Hold function. Units in nanoseconds.

Aperture Jitter - t_{apj}

The range of variation in the aperture time. Effectively a "sampling window" which ultimately dictates the maximum input slew rate acceptable for a given accuracy. Units in picoseconds.

Pipeline Delay - t_{pd}

The number of clock cycles between the initiation of the conversion process and the associated output data bit being available. Expressed in clock cycles.

Full Power Bandwidth

The input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input.

• Notes •

Semiconductor Corporation

CS5490

12-Bit, 20 MHz A/D Converter

Features

- Monolithic 20 MSPS CMOS ADC
  - On-chip Track/Hold
  - On-chip Voltage Reference
  - +5V Power Supply Only
- Dynamic Performance (f_{in}=4.97MHz):
  - SNR: 62 dB
  - THD: 66 dB
  - SFDR: 70 dB
- Analog Input Range:
  - Single-ended Input: $1.2V_{p-p}$
  - Differential Input: $2.4V_{p-p}$
- Low Power: 225 mW

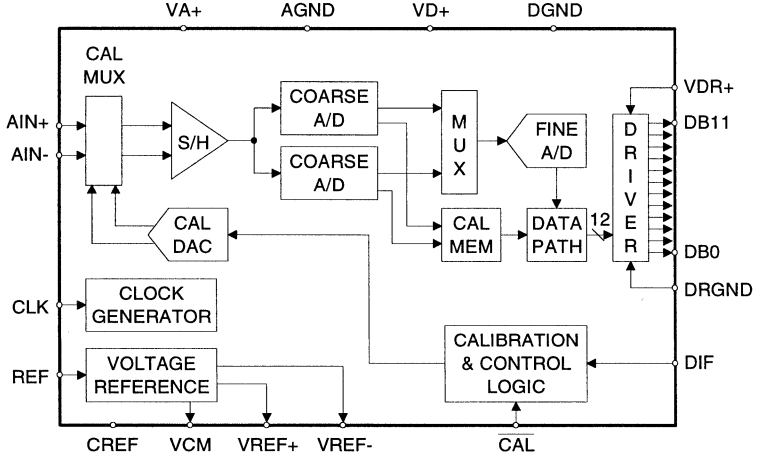
General Description

The CS5490 is a monolithic 12-bit sampling analog-to-digital converter capable of 20 MSPS conversion rate. To achieve high throughput, the CS5490 uses a fully pipelined architecture. Unique self-calibration circuitry ensures excellent linearity with no missing codes over the entire operating temperature range.

Digital inputs are CMOS and TTL compatible. Digital outputs are CMOS compatible. The analog input can be driven by either a differential 2.4 Vp-p signal, or a 1.2 Vp-p single-ended signal. Output data is available in offset binary format.

The CS5490 advanced CMOS construction provides low power consumption and the inherent reliability of monolithic devices.

For more information contact Crystal Semiconductor



Product Preview

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

• Notes •

Low-Cost, 16 & 20-Bit Measurement A/D Converter

Features

- Monolithic CMOS ADC with Filtering
  6-Pole, Low-Pass Gaussian Filter
- Up to 4kHz Output Word Rates
- On Chip Self-Calibration Circuitry
  - Linearity Error: ±0.0003%
  - Differential Nonlinearity:
    CS5501: 16-Bit No Missing Codes
    (DNL ±1/8LSB)
    CS5503: 20-Bit No Missing Codes
- System Calibration Capability
- Flexible Serial Communications Port
  - µC-Compatible Formats
  - 3-State Data and Clock Outputs
  - UART Format (CS5501 only)
- Pin-Selectable Unipolar/Bipolar Ranges
- Low Power Consumption: 25mW
  - 10µW Sleep Mode for Portable Applications
- Evaluation Boards Available

General Description

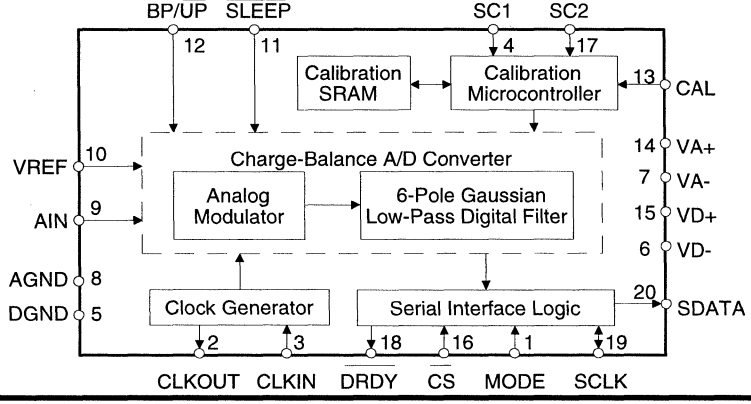
The CS5501 and CS5503 are low-cost CMOS A/D converters ideal for measuring low-frequency signals representing physical, chemical, and biological processes. They utilize charge-balance techniques to achieve 16-bit (CS5501) and 20-bit (CS5503) performance with up to 4kHz word rates at very low cost.

The converters continuously sample at a rate set by the user in the form of either a CMOS clock or a crystal. On-chip digital filtering processes the data and updates the output register at up to a 4kHz rate. The converters' low-pass, 6-pole Gaussian response filter is designed to allow corner frequency settings from .1Hz to 10Hz in the CS5501 and .5Hz to 10Hz in the CS5503. Thus, each converter rejects 50Hz and 60Hz line frequencies as well as any noise at spurious frequencies.

The CS5501 and CS5503 include on-chip self-calibration circuitry which can be initiated at any time or temperature to insure offset and full-scale errors of typically less than 1/2 LSB for the CS5501 and less than 4LSB for the CS5503. The devices can also be applied in system calibration schemes to null offset and gain errors in the input channel.

Each device's serial port offers two general purpose modes of operation for direct interface to shift registers or synchronous serial ports of industry-standard microcontrollers. In addition, the CS5501's serial port offers a third, UART-compatible mode of asynchronous communication.

ORDERING INFORMATION: Page 2-400



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: 512 445 7581

INDEX

CS5501 ANALOG CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 2.5V; CLKIN = 4.096MHz; Bipolar Mode; MODE = +5V; R_{source} = 750Ω with a 1nF to AGND at AIN (see Note 1); Digital Inputs: Logic 0 = GND; Logic 1 = VD+; unless otherwise specified.)

Parameter*		CS5501-A, B, C Min	Typ	Max	CS5501-S, T Min	Typ	Max	Units
Specified Temperature Range			-40 to +85			-55 to +125		°C
Accuracy								
Linearity Error	-A, S	-	0.0015	0.003	-	-	0.003	±%FS
	-B, T	-	0.0007	0.0015	-	0.0007	0.0015	±%FS
	-C	-	0.0003	0.0012				±%FS
Differential Nonlinearity	T_{MIN} to T_{MAX}	-	±1/8	±1/2	-	±1/8	±1/2	LSB_{16}
Full Scale Error	(Note 2)	-	±0.13	±0.5	-	±0.13	±0.5	LSB_{16}
Full Scale Drift	(Note 3)	-	±1.2	-	-	±2.3	-	LSB_{16}
Unipolar Offset	(Note 2)	-	±0.25	±1	-	±0.25	±1	LSB_{16}
Unipolar Offset Drift	(Note 3)	-	±4.2	-	-	+3.0 -25.0	-	LSB_{16}
Bipolar Offset	(Note 2)	-	±0.25	±1	-	±0.25	±1	LSB_{16}
Bipolar Offset Drift	(Note 3)	-	±2.1	-	-	+1.5 -12.5	-	LSB_{16}
Bipolar Negative Full Scale Error	(Note 2)	-	±0.5	±2	-	±0.5	±2	LSB_{16}
Bipolar Negative Full Scale Drift	(Note 3)	-	±0.6	-	-	±1.2	-	LSB_{16}
Noise (Referred to Output)		-	1/10	-	-	1/10	-	LSBrms

Notes:
1. The AIN pin presents a very high input resistance at dc and a minor dynamic load which scales to the master clock frequency. Both source resistance and shunt capacitance are therefore critical in determining the CS5501's source impedance requirements. For more information refer the text section *Analog Input Impedance Considerations*.
2. Applies after calibration at the temperature of interest.
3. Total drift over the specified temperature range since calibration at power-up at 25°C (see Figure 11). This is guaranteed by design and /or characterization. Recalibration at any temperature will remove these errors.

	Unipolar Mode			Bipolar Mode		
µV	LSB's	%FS	ppm FS	LSB's	%FS	ppm FS
10	0.26	0.0004	4	0.13	0.0002	2
19	0.50	0.0008	8	0.26	0.0004	4
38	1.00	0.0015	15	0.50	0.0008	8
76	2.00	0.0030	30	1.00	0.0015	15
152	4.00	0.0061	61	2.00	0.0030	30

CS5501 Unit Conversion Factors, VREF = 2.5V

* Refer to the Specification Definitions immediately following the Pin Description Section.

CS5503 ANALOG CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+, VD+ = 5V; VA-, VD- = -5V; VREF = 2.5V; CLKIN = 4.096MHz; Bipolar Mode; MODE = +5V; R_{source} = 750Ω with a 1nF to AGND at AIN (see Note 1): unless otherwise specified.)

Parameter*		CS5503-A, B, C Min	CS5503-A, B, C Typ	CS5503-A, B, C Max	CS5503-S, T Min	CS5503-S, T Typ	CS5503-S, T Max	Units
Specified Temperature Range			-40 to +85			-55 to +125		°C
Accuracy								
Linearity Error	-A, S -B, T -C	- - -	0.0015 0.0007 0.0003	0.003 0.0015 0.0012	- -	- 0.0007	0.003 TBD	±%FS ±%FS ±%FS
Differential Nonlinearity (Not Missing Codes)	T_{MIN} to T_{MAX}	-	20	-	-	20	-	Bits
Full Scale Error	(Note 2)	-	±4	±16	-	±4	±16	LSB_{20}
Full Scale Error Drift	(Note 3)	-	±19	-	-	±37	-	LSB_{20}
Unipolar Offset	(Note 2)	-	±4	±16	-	±4	±16	LSB_{20}
Unipolar Offset Drift	(Note 3)	-	±67	-	-	+48 -400	-	LSB_{20}
Bipolar Offset	(Note 2)	-	±4	±16	-	±4	±16	LSB_{20}
Bipolar Offset Drift	(Note 3)	-	±34	-	-	+24 -200	-	LSB_{20}
Bipolar Negative Full Scale Error	(Note 2)	-	±8	±32	-	±8	±32-	LSB_{20}
Bipolar Negative Full Scale Drift	(Note 3)	-	±10	-	-	±20	-	LSB_{20}
Noise (Referred to Output)		-	1.6	-	-	1.6	-	LSBrms (20)

	Unipolar Mode			Bipolar Mode		
µV	LSB's	%FS	ppm Fs	LSB's	%FS	ppm FS
0.596	0.25	0.0000238	0.24	0.13	0.0000119	0.12
1.192	0.50	0.0000477	0.47	0.26	0.0000238	0.24
2.384	1.00	0.0000954	0.95	0.50	0.0000477	0.47
4.768	2.00	0.0001907	1.91	1.00	0.0000954	0.95
9.537	4.000	0.0003814	3.81	2.00	0.0001907	1.91

CS5503 Unit Conversion Factors, VREF = 2.5V

* Refer to the Specification Definitions immediately following the Pin Description Section.

ANALOG CHARACTERISTICS (Continued)

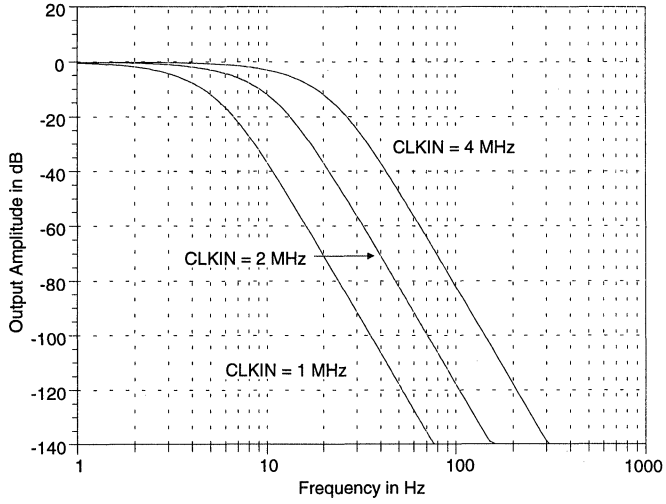
Parameter*		CS5501/3-A, B, C Min	Typ	Max	CS5501/3-S, T Min	Typ	Max	Units
Power Supplies								
DC Power Supply Currents								
IA+		-	2	3.2	-	2	3.2	mA
IA-		-	2	3.2	-	2	3.2	mA
ID+		-	1	1.5	-	1	1.5	mA
ID-	(Note 4)	-	0.03	0.1	-	0.03	0.1	mA
Power Dissipation								
$\overline{\text{SLEEP}}$ High		-	25	40	-	25	40	mW
$\overline{\text{SLEEP}}$ Low	(Note 4)	-	10	20	-	10	40	µW
Power Supply Rejection								
Positive Supplies		-	70	-	-	70	-	dB
Negative Supplies	(Note 5)	-	75	-	-	75	-	dB
Analog Input								
Analog Input Range								
Unipolar			0 to +2.5			0 to +2.5		V
Bipolar		-	±2.5	-	-	±2.5	-	V
Input Capacitance		-	20	-	-	20	-	pF
DC Bias Current	(Note 1)	-	1	-	-	1	-	nA
System Calibration Specifications								
Positive Full Scale Calibration Range			VREF+0.1			VREF+0.1		V
Positive Full Scale Input Overrange			VREF+0.1			VREF+0.1		V
Negative Full Scale Input Overrange			-(VREF+0.1)			-(VREF+0.1)		V
Maximum Offset Calibration Range	(Notes 6, 7)							
Unipolar Mode			-(VREF +0.1)			-(VREF +0.1)		V
Bipolar Mode			-40%VREF to +40%VREF			-40%VREF to +40%VREF		V
Input Span	(Note 8)	80% VREF		2VREF +0.2	80% VREF		2VREF +0.2	V

Notes:
4. All outputs unloaded.
5. 0.1Hz to 10Hz. PSRR at 60 Hz will exceed 120 dB due to the benefit of the digital filter.
6. In unipolar mode the offset can have a negative value (-VREF) such that the unipolar mode can mimic bipolar mode operation.
7. The specifications for Input Overrange and for Input Span apply additional constraints on the offset calibration range.
8. For Unipolar mode, Input Span is the difference between full scale and zero scale. For Bipolar mode, Input Span is the difference between positive and negative full scale points. When using less than the maximum input span, the span range may be placed anywhere within the range of ±(VREF + 0.1).

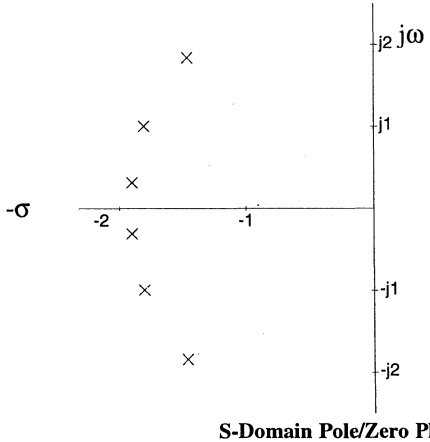
Specifications are subject to change without notice.

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Units
Sampling Frequency	f_s	CLKIN/ 256	Hz
Output Update Rate	f_{out}	CLKIN /1024	Hz
Filter Corner Frequency	f_{-3dB}	CLKIN /409,600	Hz
Settling Time to ±0.0007% FS (FS Step)	t_s	506,880/CLKIN	s



Frequency Response



$S_{1,2} = -1.4667 \pm j1.8199$

$S_{3,4} = -1.7559 \pm j1.0008$

$S_{5,6} = -1.8746 \pm j0.32276$

S-Domain Pole/Zero Plot (Continuous-Time Representation)

$$H(x) = [1 + 0.694x^2 + 0.241x^4 + 0.0557x^6 + 0.009664x^8 + 0.00134x^{10} + 0.000155x^{12}]^{-1/2}$$

where $x = f/f_{-3dB}$, f_{-3dB} = CLKIN/409,600, and f is the frequency of interest.

Continuous-Time Representation of 6-Pole Gaussian Filter

DIGITAL CHARACTERISTICS (T_A = T_{min} to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%)

Parameter	Symbol	Min	Typ	Max	Units
Calibration Memory Retention Power Supply Voltage (VD+ and VA+)	V_{MR}	2.0	-	-	V
High-Level Input Voltage All Except CLKIN	V_{IH}	2.0	-	-	V
High-Level Input Voltage CLKIN	V_{IH}	3.5	-	-	V
Low-Level Input Voltage All Except CLKIN	V_{IL}	-	-	0.8	V
Low-Level Input Voltage CLKIN	V_{IL}	-	-	1.5	V
High-Level Output Voltage (Note 9)	V_{OH}	(VD+)-1.0V	-	-	V
Low-Level Output Voltage Iout=1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	-	10	µA
3-State Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Notes: 9. I_{out} = -100 µA. This guarantees the ability to drive one TTL load. (V_{OH} = 2.4V @ I_{out} = -40 µA).

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Power Supplies:	Positive Digital	VD+	-0.3	(VA+)+0.3	V
	Negative Digital	VD-	0.3	-6.0	V
	Positive Analog	VA+	-0.3	6.0	V
	Negative Analog	VA-	0.3	-6.0	V
Input Current, Any Pin Except Supplies (Notes 10, 11)		I_{in}	-	±10	mA
Analog Input Voltage (AIN and VREF pins)		V_{INA}	(VA-)-0.3	(VA+)+0.3	V
Digital Input Voltage		V_{IND}	-0.3	(VA+)+0.3	V
Ambient Operating Temperature		T_A	-55	125	C°
Storage Temperature		T_{stg}	-65	150	C°

Notes: 10. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pin.
11. Transient currents of up to 100mA will not cause SCR latch-up. Maximum input current for a power supply pin is ± 50 mA.

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V) (Note 12)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	VA+	V
	Negative Digital	VD-	-4.5	-5.0	-5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	-4.5	-5.0	-5.5	V
Analog Reference Voltage		VREF	1.0	2.5	3.0	V
Analog Input Voltage:	(Note 13)					
	Unipolar	V_{AIN}	AGND	-	VREF	V
	Bipolar	V_{AIN}	-VREF	-	VREF	V

Notes: 12. All voltages with respect to ground.

13. The CS5501 and CS5503 can accept input voltages up to the analog supplies (VA+ and VA-). They will accurately convert and filter signals with noise excursions up to 100mV beyond |VREF|. After filtering, the devices will output all 1's for any input above VREF and all 0's for any input below AGND in unipolar mode and -VREF in bipolar mode.

SWITCHING CHARACTERISTICS (T_A = T_{min} to T_{max}; CLKIN=4.096 MHz; VA+, VD+ = 5V±10%; VA-, VD- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF; unless otherwise specified.)

Parameter		Symbol	Min	Typ	Max	Units
Master Clock Frequency:	Internal Gate Oscillator (See Table 1)	CLKIN	200	4096	5000	kHz
	Externally Supplied: (Note 14)					
	Maximum	CLKIN	-	-	5000	kHz
	Minimum (Note 15)	CLKIN	200	40	-	kHz
CLKIN Duty Cycle			20	-	80	%
Rise Times:	Any Digital Input	t_{rise}	-	-	1.0	µs
	Any Digital Output (Note 16)	t_{rise}	-	20	-	ns
Fall Times:	Any Digital Input	t_{fall}	-	-	1.0	µs
	Any Digital Output (Note 16)	t_{fall}	-	20	-	ns
Set Up Times:	SC1, SC2 to CAL Low	t_{scs}	100	-	-	ns
	$\overline{SLEEP}$ High to CLKIN High (Note 17)	t_{sls}	1	-	-	µs
Hold Time:	SC1, SC2 hold after CAL falls	t_{sch}	100	-	-	ns

Notes: 14. CLKIN must be supplied whenever the CS5501 or CS5503 is not in $\overline{SLEEP}$ mode. If no clock is present when not in $\overline{SLEEP}$ mode, the device can draw higher current than specified and possibly become uncalibrated.

15. The CS5501/CS5503 is production tested at 4.096 MHz. It is guaranteed by characterization to operate at 200 kHz.

16. Specified using 10% and 90% points on waveform of interest.

17. In order to synchronize several CS5501's or CS5503's together using the $\overline{SLEEP}$ pin, this specification must be met.

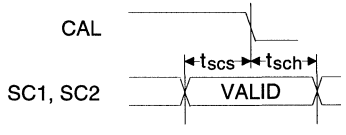
SWITCHING CHARACTERISTICS (continued) (T_A = T_{min} to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

Parameter		Symbol	Min	Typ	Max	Units
SSC Mode (Mode = VD+)						
Access Time	$\overline{CS}$ Low to SDATA Out	t_{csd1}	3/CLKIN	-	-	ns
SDATA Delay Time	SCLK Falling to New SDATA bit	t_{dd1}	-	25	100	ns
SCLK Delay Time (at 4.096 MHz)	SDATA MSB bit to SCLK Rising	t_{cd1}	250	380	-	ns
Serial Clock (Out)	Pulse Width High (at 4.096 MHz) Pulse Width Low	t_{ph1} t_{pl1}	- -	240 730	300 790	ns
Output Float Delay	SCLK Rising to Hi-Z	t_{fd2}	-	1/CLKIN + 100	1/CLKIN + 200	ns
Output Float Delay	$\overline{CS}$ High to Output Hi-Z (Note 18)	t_{fd1}	-	-	4/CLKIN +200	ns
SEC Mode (Mode = DGND)						
Serial Clock (In)		f_{sclk}	dc	-	4.2	MHz
Serial Clock (In)	Pulse Width High Pulse Width Low	t_{ph2} t_{pl2}	50 180	- -	- -	ns
Access Time	$\overline{CS}$ Low to Data Valid (Note 19)	t_{csd2}	-	80	160	ns
Maximum Data Delay Time	(Note 20) SCLK Falling to New SDATA bit	t_{dd2}	-	75	150	ns
Output Float Delay	$\overline{CS}$ High to Output Hi-Z	t_{fd3}	-	-	250	ns
Output Float Delay	SCLK Falling to Output Hi-Z	t_{fd4}	-	100	200	ns

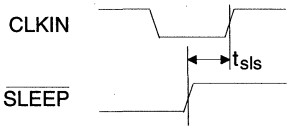
Notes: 18. If $\overline{CS}$ is returned high before all data bits are output, the SDATA and SCLK outputs will complete the current data bit and then go to high impedance.

19. If $\overline{CS}$ is activated asynchronously to $\overline{DRDY}$, $\overline{CS}$ will not be recognized if it occurs when $\overline{DRDY}$ is high for 4 clock cycles. The propagation delay time may be as great as 4 CLKIN cycles plus 160 ns. To guarantee proper clocking of SDATA when using asychronous $\overline{CS}$, SCLK(i) should not be taken high sooner than 4 CLKIN cycles plus 160ns after $\overline{CS}$ goes low.

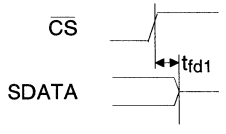
20. SDATA transitions on the falling edge of SCLK(i).



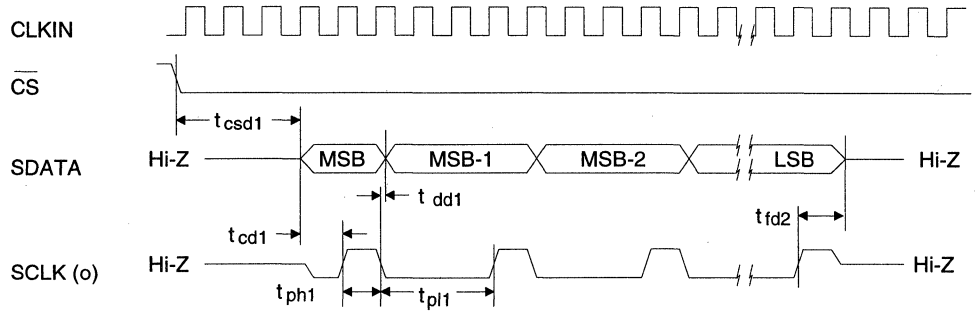
Calibration Control Timing



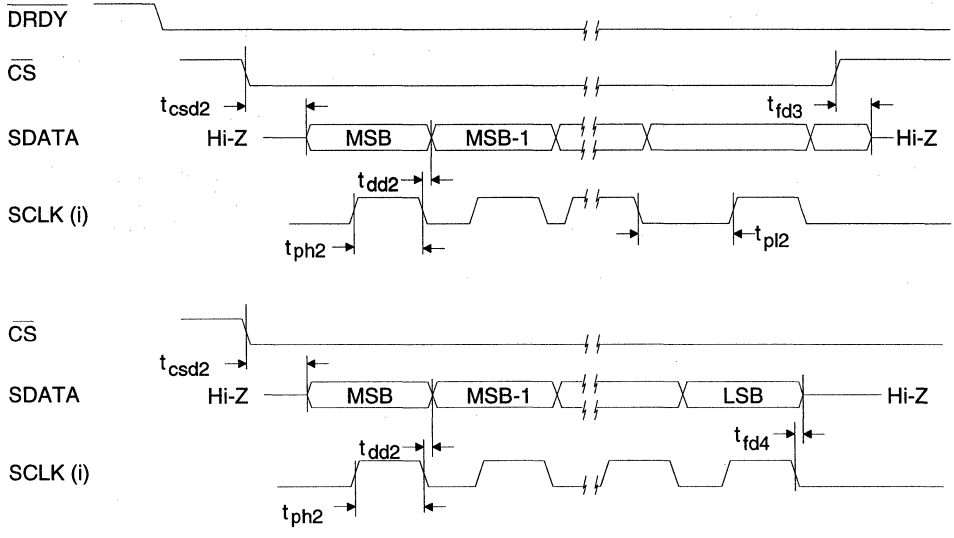
Sleep Mode Timing for Synchronization



Output Float Delay SSC Mode (Note 19)



SSC MODE Timing Relationships

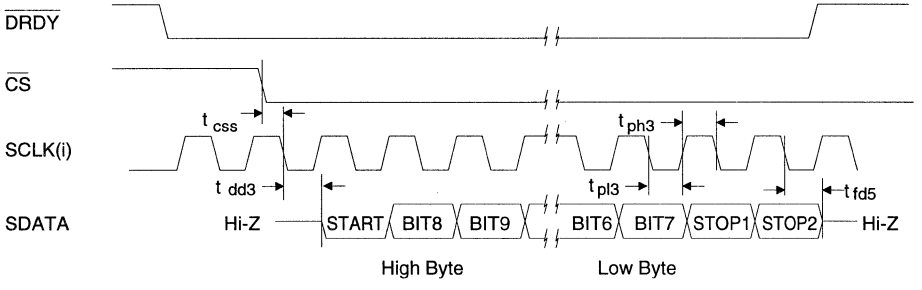


SEC MODE Timing Relationships

SWITCHING CHARACTERISTICS (continued) (T_A = T_{min} to T_{max}; VA+, VD+ = 5V ± 10%; VA-, VD- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

Parameter		Symbol	Min	Typ	Max	Units
AC Mode (Mode = VD-) CS5501 only						
Serial Clock (In)		f_{sclk}	dc	-	4.2	MHz
Serial Clock (In)	Pulse Width High Pulse Width Low	t_{ph3} t_{pl3}	50 180	- -	- -	ns ns
Set-up Time	$\overline{CS}$ Low to SCLK Falling	t_{css}	-	20	40	ns
Maximum Data Delay Time	SCLK Fall to New SDATA bit	t_{dd3}	-	90	180	ns
Output Float Delay	$\overline{CS}$ High to Output Hi-Z (Note 21)	t_{fd5}	-	100	200	ns

Notes: 21. If $\overline{CS}$ is returned high after an 11-bit data packet is started, the SDATA output will continue to output data until the end of the second stop bit. At that time the SDATA output will go to high impedance.



AC MODE Timing Relationships (CS5501 only)

GENERAL DESCRIPTION

The CS5501/CS5503 are monolithic CMOS A/D converters designed specifically for high resolution measurement of low-frequency signals. Each device consists of a charge-balance converter (16-Bit for the CS5501, 20-Bit for the CS5503), calibration microcontroller with on-chip SRAM, and serial communications port.

The CS5501/CS5503 A/D converters perform conversions continuously and update their output ports after every conversion (unless the serial port is active). Conversions are performed and the serial port is updated independent of external control. Both devices are capable of measuring either unipolar or bipolar input signals, and calibration cycles may be initiated at any time to ensure measurement accuracy.

The CS5501/CS5503 perform conversions at a rate determined by the master clock signal. The master clock can be set by an external clock or with a crystal connected to the pins of the on-chip gate oscillator. The master clock frequency determines:

1. The sample rate of the analog input signal.
2. The corner frequency of the on-chip digital filter.
3. The output update rate of the serial output port.

The CS5501/CS5503 design includes several self-calibration modes and several serial port interface modes to offer users maximum system design flexiblity.

The Delta-Sigma Conversion Method

The CS5501/CS5503 A/D converters use charge-balance techniques to achieve low cost, high resolution measurements. A charge-balance A/D converter consists of two basic blocks: an analog modulator and a digital filter. An elementary example of a charge-balance A/D converter is a conventional voltage-to-frequency converter and counter. The VFC's 1-bit output conveys information in the form of frequency (or duty cycle), which is then filtered (averaged) by the counter for higher resolution.

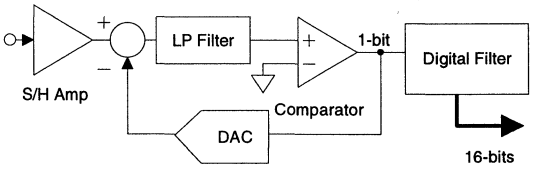
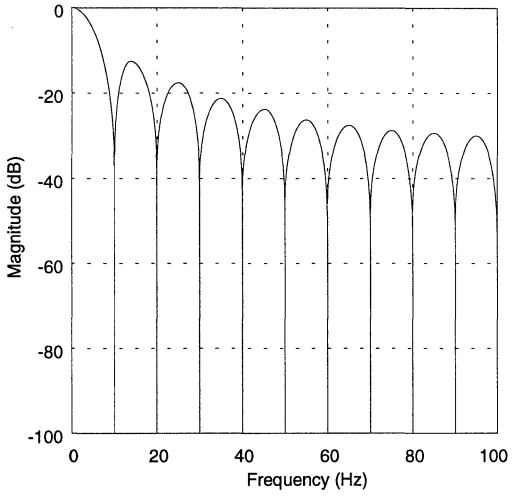


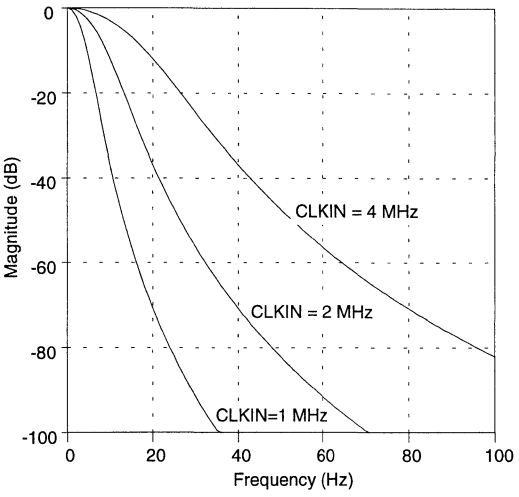
Figure 1. Charge Balance (Delta-Sigma) A/D Converter

The analog modulator of the CS5501/CS5503 is a multi-order delta-sigma modulator. The modulator consists of a 1-bit A/D converter (that is, a comparator) embedded in an analog feedback loop with high open loop gain (see Figure 1). The modulator samples and converts the input at a rate well above the bandwidth of interest. The 1-bit output of the comparator is sampled at intervals based on the clock rate of the part and this information (either a 1 or 0) is conveyed to the digital filter. The digital filter is much more sophisticated than a simple counter. The filter on the chip has a 6-pole low pass Gaussian response which rolls off at 120 dB/decade (36 dB/octave). The corner frequency of the digital filter scales with the master clock frequency. In comparison, VFC's and dual slope converters offer (sin x)/x filtering for high frequency rejection (see Figure 2 for a comparison of the characteristics of these two filter types). When operating from a 1 MHz master clock the digital filter in the CS5501/CS5503 offers better than 120 dB rejection of 50 and 60 Hz line frequencies and does not require any type of line synchronization to achieve this rejection. It should be noted that the CS5501/CS5503 will update its output port almost at 1000 times per second when operating from the 1 MHz clock. This is a much higher update rate (typically by a factor of at least 50 times) than either VFCs or dual-slope converters can offer.

For a more detailed discussion on the delta-sigma modulator see the Application note "Delta-Sigma



a. Averaging (Integrating) Filter Response (tavg = 100 ms)



b. 6-Pole Gaussian Filter Response

Figure 2. Filter Responses

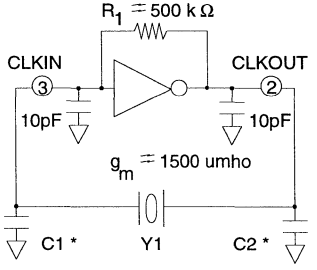
A/D Conversion Technique Overview" in the application note section of the data book. The application note discusses the delta-sigma modulator and some aspects of digital filtering.

OVERVIEW

As shown in the block diagram on the front page of the data sheet, the CS5501/CS5503 can be segmented into five circuit functions. The heart of the chip is the charge balance A/D converter (16-bit for the CS5501, 20-bit for the CS5503). The converter and all of the other circuit functions on the chip must be driven by a clock signal from the clock generator. The serial interface logic outputs the converted data. The calibration microcontroller along with the calibration SRAM (static RAM), supervises the device calibration. Each segment of the chip has control lines associated with it. The function of each of the pins is described in the pin description section of the data sheet.

Clock Generator

The CS5501/CS5503 both include gates which can be connected as a crystal oscillator to provide the master clock signal for the chip. Alternatively, an external (CMOS compatible) clock can be input to the CLKIN pin as the master clock for the device. Figure 3 illustrates a simple model of the on-chip gate oscillator. The gate has a typical transconductance of 1500 µmho. The gate model includes 10 pf capacitors at the input and output pins. These capacitances include the typical stray capacitance of the pins of the device. The on-chip



* See Table 1

Figure 3. On-chip Gate Oscillator Model

gate oscillator is designed to properly operate without additional loading capacitors when using a 4.096 MHz (or 4 MHz) crystal. If other crystal frequencies or if ceramic resonators are used, loading capacitors may be necessary for reliable operation of the oscillator. Table 1 illustrates some typical capacitor values to be used with selected resonating elements.

Resonators	C1	C2
Ceramic		
200 kHz	330pF	470pF
455 kHz	100pF	100pF
1.0 MHz	50pF	50pF
2.0 MHz	20pF	20pF
Crystals		
2.000 MHz	30pF	30pF
3.579 MHz	20pF	20pF
4.096 MHz	None	None

Table 1. Resonator Loading Capacitors

CLKOUT (pin 2) can be used to drive one external CMOS gate for system clock requirements. In this case, the external gate capacitance must be taken into account when choosing the value of C2.

Caution: A clock signal should always be present whenever the $\overline{\text{SLEEP}}$ is inactive ($\overline{\text{SLEEP}}$ = VD+). If no clock is provided to the part when not in $\overline{\text{SLEEP}}$, the part may draw excess current and possibly even lose its calibration data. This is because the device is built using dynamic logic.

Serial Interface Logic

The CS5501 serial data output can operate in any one of the following three different serial interface modes depending upon the MODE pin selection:

SSC (Synchronous Self-Clocking) mode;
MODE pin tied to VD+ (+5V).

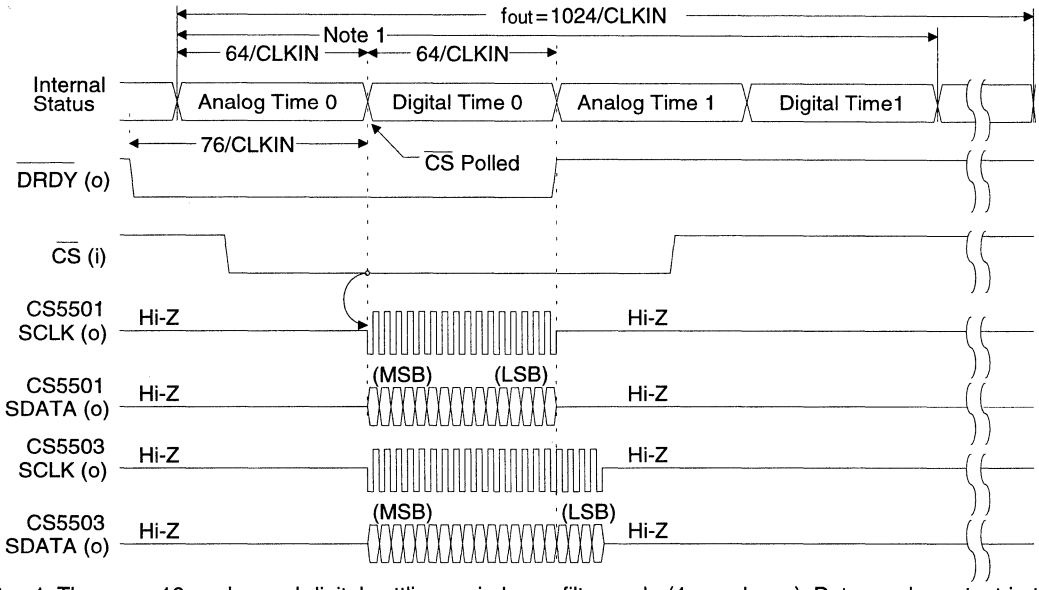
SEC (Synchronous External Clocking) mode;
MODE pin tied to DGND.

and AC (Asynchronous Communication) mode;
CS5501 only
MODE pin tied to VD- (-5V)

The CS5503 can only operate in the first two modes, SEC and SSC.

Synchronous Self-Clocking Mode

When operated in the SSC mode (MODE pin tied to VD+), the CS5501/CS5503 furnish both serial output data (SDATA) and an internally-generated serial clock (SCLK). Internal timing for the SSC mode is illustrated in Figure 4. Figure 5 shows detailed SSC mode timing for both the CS5501/CS5503. A filter cycle occurs every 1024 cycles of CLKIN. During each filter cycle, the status of $\overline{\text{CS}}$ is polled at eight specific times during the cycle. If $\overline{\text{CS}}$ is low when it is polled, the CS5501/CS5503 begin clocking the data bits out, MSB first, at a SCLK output rate of CLKIN/4. Once transmission is complete, $\overline{\text{DRDY}}$ rises and both SDATA and SCLK outputs go into a high impedance state. A filter cycle begins each time $\overline{\text{DRDY}}$ falls. If the $\overline{\text{CS}}$ line is not active, $\overline{\text{DRDY}}$ will return high 1020 clock cycles after it falls. Four clock cycles later $\overline{\text{DRDY}}$ will fall to signal that the serial port has been updated with new data and that a new filter cycle has begun. The first $\overline{\text{CS}}$ polling during a filter cycle occurs 76 clock cycles after $\overline{\text{DRDY}}$ falls (the rising edge of CLKIN on which $\overline{\text{DRDY}}$ falls is considered clock cycle number one). Subsequent pollings of $\overline{\text{CS}}$ occur at intervals of 128 clock cycles thereafter (76, 204, 332, etc.). The $\overline{\text{CS}}$ signal is polled at the beginning of each of eight data output windows which occur in a filter cycle. To transmit data during any one of the eight output windows, $\overline{\text{CS}}$ must be low at least three CLKIN cycles before it is polled. If $\overline{\text{CS}}$ does not meet this set-up time, data will not be transmitted during the window time. Furthermore, $\overline{\text{CS}}$ is not latched internally and therefore must be held low during the entire data transmission to obtain all of the data bits.



Note: 1. There are 16 analog and digital settling periods per filter cycle (4 are shown). Data can be output in the SSC mode in only 1 of the 8 digital time periods in each filter cycle.

Figure 4. Internal Timing

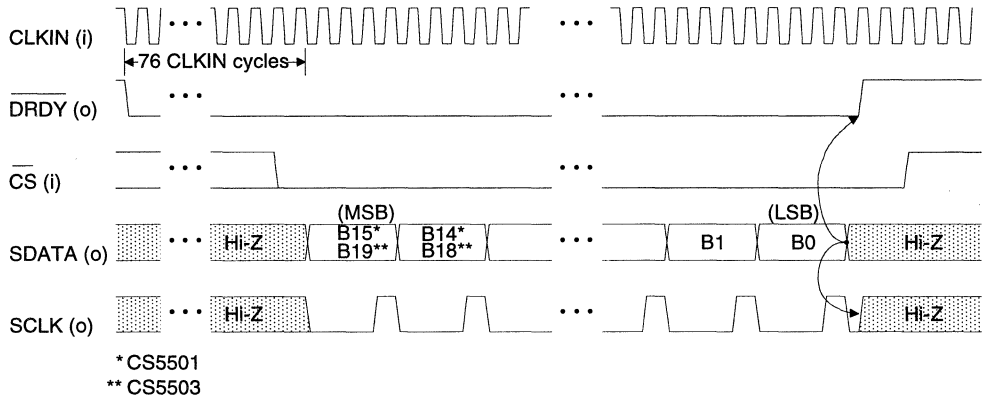


Figure 5. Synchronous Self-Clocking (SSC) Mode Timing

The eighth output window time overlaps the time in which the serial output port is to be updated. If the $\overline{CS}$ is recognized as being low when it is polled for the eighth window time, data will be output as normal, but the serial port will not be updated with new data until the next serial port update time. Under these conditions, the serial port will experience an update rate of only 2 kHz (CLKIN = 4.096 MHz) instead of the normal 4 kHz serial port update rate.

Upon completion of transmission of all the data bits, the SCLK and SDATA outputs will go to a high impedance state even with $\overline{CS}$ held low. In the event that $\overline{CS}$ is taken high before all data bits are output, the SDATA and SCLK outputs will

complete the current data bit output and go to a high impedance state when SCLK goes low.

Synchronous External Clocking Mode

When operated in the SEC mode (MODE pin tied to DGND), the CS5501/CS5503 outputs the data in its serial port at a rate determined by an external clock which is input into the SCLK pin. In this mode the output port will be updated every 1024 CLKIN cycles. $\overline{\text{DRDY}}$ will go low when new data is loaded into the output port. If $\overline{\text{CS}}$ is not active, $\overline{\text{DRDY}}$ will return positive 1020 CLKIN cycles later and remain so for four CLKIN cycles. If $\overline{\text{CS}}$ is taken low it will be recognized immediately unless it occurs while $\overline{\text{DRDY}}$ is high for the four clock cycles. As soon as $\overline{\text{CS}}$ is recognized, the SDATA output will come out of its high-impedance state and present the MSB data bit. The MSB data bit will remain present until a falling edge of SCLK occurs to advance the output to the MSB-1 bit. If the $\overline{\text{CS}}$ and external SCLK are operated asynchronously to CLKIN, errors can result in the output data unless certain precautions are taken. If $\overline{\text{CS}}$ is activated asynchronously, it may occur during the four clock cycles when $\overline{\text{DRDY}}$ is high and therefore not be recognized immediately. To be certain that data misread errors will not result if $\overline{\text{CS}}$ occurs at this time, the SCLK input should not transition high to latch the MSB until four CLKIN cycles plus 160 ns after $\overline{\text{CS}}$ is taken low. This insures that $\overline{\text{CS}}$ will be recognized and the MSB bit will become stable before the SCLK transitions positive to latch the MSB data bit.

When SCLK returns low the serial port will present the MSB-1 data bit on its output. Subsequent cycles of SCLK will advance the data output. When all data bits are clocked out, $\overline{\text{DRDY}}$ will then go high and the SDATA output will go into a high impedance state. If the $\overline{\text{CS}}$ input goes low and all of the data bits are not clocked out of the port, filter cycles will continue to occur but the output serial port will not be updated with new data ($\overline{\text{DRDY}}$ will remain low). If $\overline{\text{CS}}$ is taken high at any time, the SDATA output pin will go to a high impedance state. If any of the data bits in the serial port have not been clocked out, they will remain available until $\overline{\text{DRDY}}$ returns high for four clock cycles. After this $\overline{\text{DRDY}}$ will fall and the port will be updated with a new 16-bit word in the CS5501 or 20-bit word in the CS5503. It is acceptable to clock out less than all possible data bits if $\overline{\text{CS}}$ is returned high to allow the port to be updated. Figure 6 illustrates the serial port timing in the SEC mode.

Asynchronous Communication Mode (CS5501 Only)

In the CS5501, the AC mode is activated when the MODE pin is tied to VD- (-5 V). When operating in the AC mode the CS5501 is designed to

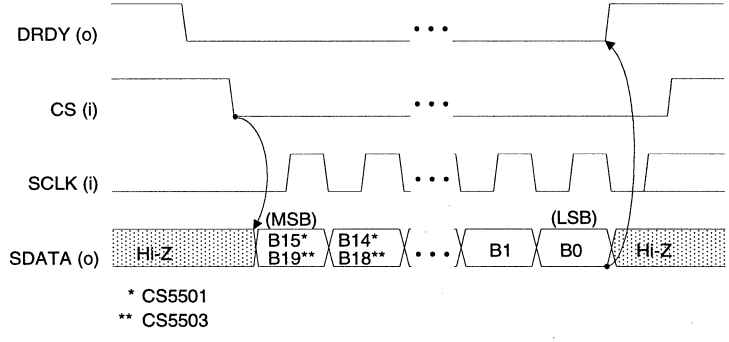


Figure 6. Synchronous External-Clocking (SEC) Mode Timing

provide data output in UART compatible format. The baud rate of the SDATA output will be determined by the rate of the SCLK input. The data which is output of the SDATA pin will be formatted such that it will contain two 11 bit data packets. Each packet includes one start bit, eight data bits, and two stop bits. The packet which carries the most-significant-byte data will be output first, with its lsb being the first data bit output after the start bit.

In this mode, $\overline{DRDY}$ will occur every 1024 clock cycles. If the serial port is not outputting a data byte, $\overline{DRDY}$ will return high after 1020 clock cycles and remain high for 4 clock cycles. $\overline{DRDY}$ will then go low to indicate that an update to the serial output port with a new 16 bit word has occurred. To initiate a transmission from the port the $\overline{CS}$ line must be taken low. Then SCLK, which is an input in this mode, must transition from a high to a low to latch the state of $\overline{CS}$ internal to the CS5501. Once $\overline{CS}$ is recognized and latched as a low, the port will begin to output data. Figure 7 details the timing for this output. $\overline{CS}$ can be returned high before the end of the 11-bit transmission and the transmission will continue until the second stop bit of the first 11-bit packet is output. The SDATA output will go into a high impedance state after the second stop bit is output. To obtain the second 11-bit packet $\overline{CS}$ must again be brought low before $\overline{DRDY}$ goes high or the second 11-bit data packet will be overwritten with a serial port update. For the second 11-bit packet, $\overline{CS}$ need only to go low for 50 ns; it need not be latched by a falling edge of SCLK. Alternately, the $\overline{CS}$ line can be taken low and held low until both 11-bit data packets are output. This is the preferred method of control as it will prevent losing the second 11-bit data packet if the port is updated. Some serial data rates can be quite slow compared to the rate at which the CS5501 can update its output port. A slow data rate will leave only a short period of time to start the second 11-bit packet if $\overline{CS}$ is returned high momentarily. If $\overline{CS}$ is held low continuously ($\overline{CS}$ hard-wired to DGND), the serial port will be updated only after all 22 bits have been clocked out of the port.

Upon the completion of a transmission of the two 11-bit data packets the SDATA output will go into a high impedance state. If at any time during transmission the $\overline{CS}$ is taken back high, the current 11-bit data packet will continue to be output. At the end of the second stop bit of the data packet, the SDATA output will go into a high impedance state.

Linearity Performance

The CS5501/CS5503 delta-sigma converters are like conventional charge-balance converters in that they have no source of nonmonotonicity. The devices therefore have no missing codes in their transfer functions. See Figure 8 for a plot of the

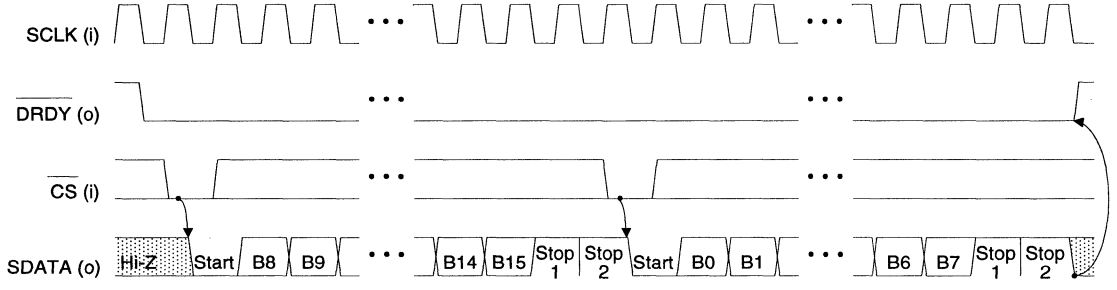


Figure 7. CS5501 Asynchronous (UART) Mode Timing

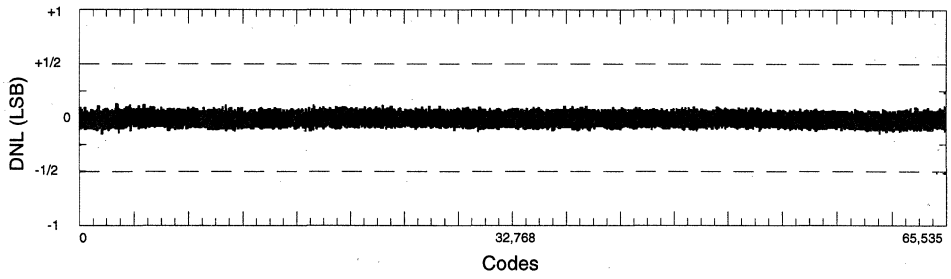


Figure 8. CS5501 Differential Nonlinearity Plot

excellent differential linearity achieved by the CS5501. The CS5501/CS5503 also have excellent integral linearity, which is accomplished with a well-designed charge-balance architecture. Each device also achieves low input drift through the use of chopper-stabilized techniques in its input stage. To assure that the CS5501/CS5503 achieves excellent performance over time and temperature, it uses digital calibration techniques to minimize offset and gain errors to typically within ±1/2 LSB at 16 bits in the CS5501 and ±4 LSB at 20 bits in the CS5503.

Converter Calibration

The CS5501/CS5503 offer both self-calibration and system level calibration capability. To understand the calibration features, a basic comprehension of the internal workings of the converter are helpful. As mentioned previously in this data sheet, the converter consists of two sections. First is the analog modulator which is a delta-sigma type charge-balance converter. This is followed by a digital filter. The filter circuitry is actually an arithmetic logic unit (ALU) whose architecture and instructions execute the filter function. The modulator (explained in more detail in the applications note "Delta-Sigma Conversion Technique Overview") uses the VREF voltage connected to pin 10 to determine the magnitude of the voltages used in its feedback DAC. The modulator accepts an analog signal at its input and produces a data stream of 1's and 0's as its output. This data stream value can change (from 1 to 0 or vice versa) every 256 CLKIN cycles. As the input voltage increases the ratio of 1's to 0's out of the modulator increases proportionally. The 1's density of the data stream out of the modulator therefore provides a digital representation of the analog input signal where the 1's density is defined as the ratio of the number of 1's to the number of 0's out of the modulator for a given period of time. The 1's density output of the modulator is also a function of the voltage on the VREF pin. If the voltage on the VREF pin increases in value (say, due to temperature drift), and the analog input voltage into the modulator remains constant, the 1's density output of the modulator will decrease (less 1's will occur). The analog input into the modulator which is necessary to produce a given binary output code from the converter is ratiometric to the voltage on the VREF pin. This means that if VREF increases by one per cent, the analog signal on AIN must also increase by one per cent to maintain the same binary output code from the converter.

For a complete calibration to occur, the calibration microcontroller inside the device needs to record the data stream 1's density out of the modulator for two different input conditions. First, a "zero scale" point must be presented to the modulator. Then a "full scale" point must be presented to the modulator. In unipolar self-cal mode the zero scale point is AGND and the full scale point is the voltage on the VREF pin. The calibration microcontroller then remembers the 1's density out of the modulator for each of these points and calculates a slope factor (LSB/μV). This slope factor

represents the gain slope for the input to output transfer function of the converter. In unipolar mode the calibration microcontroller determines the slope factor by dividing the span between the zero point and the full scale point by the total resolution of the converter (2^{16} for the CS5501, resulting in 65,536 segments or 2^{20} for the CS5503, resulting in 1,048,578 segments). In bipolar mode the calibration microcontroller divides the span between the zero point and the full scale point into 524,288 segments for the CS5503 and 32,768 segments for the CS5501. It then extends the measurement range 524,288 segments for the CS5503, 32,768 segments for the CS5501, below the zero scale point to achieve bipolar measurement capability. In either unipolar or bipolar modes the calculated slope factor is saved and later used to calculate the binary output code when an analog signal is present at the AIN pin during measurement conversions.

System calibration allows the A/D converter to compensate for system gain and offset errors (see Figure 9). System calibration performs the same slope factor calculations as self-cal but uses voltage values presented by the system to the AIN pin for the zero scale point and for the full scale point. Table 2 depicts the calibration modes available. Two system calibration modes are listed. The first mode offers system level calibration for system offset and for system gain. This is a two-step calibration. The zero scale point (system offset) must be presented to the converter first. The voltage that represents zero scale point must be input to the converter before the calibration step is initiated and must remain stable until the step is complete. The $\overline{DRDY}$ output from the converter will signal when the step is complete by going low. After the zero scale point is calibrated, the voltage representing the full scale point is input to the converter and the second calibration step is initiated. Again the voltage must remain stable throughout the calibration step.

This two-step calibration mode offers another calibration feature. After a two-step calibration

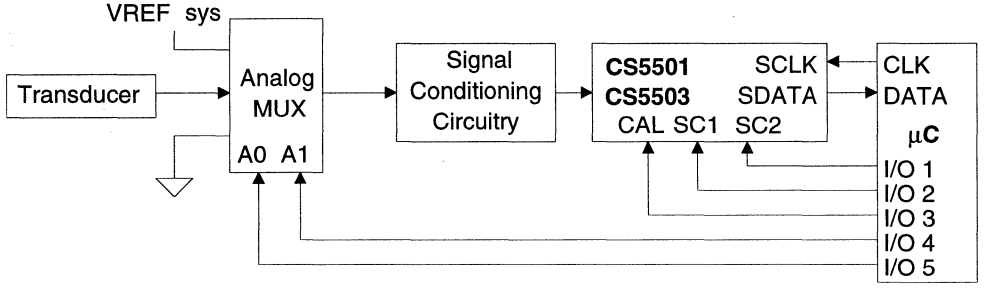


Figure 9. System Calibration

CAL	SC1	SC2	Cal Type	ZS Cal	FS Cal	Sequence	Calibration Time
↓	0	0	Self-Cal	AGND	VREF	One Step	3,145,655/f_{clk}
↓	1	1	System Offset & System Gain	AIN	-	1st Step	1,052,599/f_{clk}
↓	0	1		-	AIN	2nd Step	1,068,813/f_{clk}
↓	1	0	System Offset	AIN	VREF	One Step	2,117,389/f_{clk}

* $\overline{DRDY}$ remains high throughout the calibration sequence. In Self-Cal mode (SC1 and SC2 low) $\overline{DRDY}$ falls once the CS5501 or CS5503 has settled to the analog input. In all other modes $\overline{DRDY}$ falls immediately after the calibration term has been determined.

Table 2. Calibration Control

sequence (system offset and system gain) has been properly performed, additional offset calibrations can be performed by themselves to reposition the gain slope (the slope factor is not changed) to adjust its zero reference point to the new system zero reference value.

A second system calibration mode is available which uses an input voltage for the zero scale calibration point, but uses the VREF voltage as the full scale calibration point.

Whenever a system calibration mode is used, there are limits to the amount of offset and to the amount of span which can be accommodated. The range of input span which can be accommodated in either unipolar or bipolar mode is restricted to not less than 80% of the voltage on VREF and not more than 200% of (VREF + 0.1) V. The amount of offset which can be calibrated depends upon whether unipolar or bipolar mode is being used. In unipolar mode the system calibration modes can handle offsets as positive as 20% of VREF (this is restricted by the minimum span requirement of 80% VREF) or as negative as -(VREF + 0.1) V. This capability enables the unipolar mode of the CS5501/CS5503 to be calibrated to mimic bipolar mode operation.

In the bipolar mode the system offset calibration range is restricted to a maximum of ±40% of VREF. It should be noted that the span restrictions limit the amount of offset which can be calibrated. The span range of the converter in bipolar mode extends an equidistance (+ and -) from the voltage used for the zero scale point. When the zero scale point is calibrated it must not cause either of the two endpoints of the bipolar transfer function to exceed the positive or the negative input overrange points (+(VREF + 0.1) V or - (VREF + 0.1) V). If the span range is set to a minimum (80% VREF) the offset voltage can move ±40% VREF without causing the end points of the transfer function to exceed the overrange points. Alternatively, if the span range is set to 200% of VREF, the input offset cannot move more than +0.1 or - 0.1 V before an endpoint of the transfer function exceeds the input overrange limit.

Initiating Calibration

Table 2 illustrates the calibration modes available in the CS5501/CS5503. Not shown in the table is the function of the BP/$\overline{UP}$ pin which determines whether the converter is calibrated to measure bipolar or unipolar signals. A calibration step is initiated by bringing the CAL pin (13) high for at least 4 CLKIN cycles to reset the part and then bringing CAL low. The states of SC1 (pin 4) and SC2 (pin 17) along with the BP/$\overline{UP}$ (pin 12) will determine the type of calibration to be performed. The SC1 and SC2 inputs are latched when CAL goes low. The BP/$\overline{UP}$ input is not latched and therefore must remain in a fixed state throughout the calibration and measurement cycles. Any time the state of the BP/$\overline{UP}$ pin is changed, a new calibration cycle must be performed to enable the CS5501/CS5503 to properly function in the new mode.

When a calibration step is initiated, the $\overline{DRDY}$ signal will go high and remain high until the step is finished. Table 2 illustrates the number of clock cycles each calibration requires. Once a calibration step is initiated it must finish before a new calibration step can be executed. In the two step system calibration mode, the offset calibration step must be initiated before initiating the gain calibration step.

When a self-cal is completed $\overline{DRDY}$ falls and the output port is updated with a data word that represents the analog input signal at the AIN pin. When a system calibration step is completed, $\overline{DRDY}$ will fall and the output port will be updated with the appropriate data value (zero scale point, or full scale point). In the system calibration mode, the digital filter must settle before the output code will represent the value of the analog input signal.

Cal Mode	Zero Scale	Gain Factor	1LSB			
			Unipolar		Bipolar	
			CS5501	CS5503	CS5501	CS5503
Self-Cal	AGND	VREF	$\frac{VREF}{65,536}$	$\frac{VREF}{1,048,526}$	$\frac{2VREF}{65,536}$	$\frac{2VREF}{1,048,526}$
System Cal	SOFF	SGAIN	$\frac{SGAIN-SOFF}{65,536}$	$\frac{SGAIN-SOFF}{1,048,526}$	$\frac{2(SGAIN-SOFF)}{65,536}$	$\frac{2(SGAIN-SOFF)}{1,048,526}$

Table 3. Output Code Size After Calibration

Input Voltage, Unipolar Mode				Input Voltage, Bipolar Mode	
System-Cal	Self-Cal	Output Codes (Hex)		Self-Cal	System Cal
		CS5501	CS5503		
>(SGAIN - 1.5 LSB)	>(VREF - 1.5 LSB)	FFFF	FFFFF	>(VREF - 1.5 LSB)	>(SGAIN - 1.5 LSB)
SGAIN - 1.5 LSB	VREF - 1.5 LSB	FFFF FFFE	FFFFF FFFFE	VREF - 1.5 LSB	SGAIN - 1.5 LSB
(SGAIN - SOFF)/2 - 0.5 LSB	VREF/2 - 0.5 LSB	8000 7FFF	80000 7FFFF	AGND - 0.5 LSB	SOFF -0.5 LSB
SOFF + 0.5 LSB	AGND + 0.5 LSB	0001 0000	00001 00000	-VREF+ 0.5 LSB	-SGAIN + 2SOFF + 0.5 LSB
<(SOFF + 0.5 LSB)	<(AGND+0.5 LSB)	0000	00000	<(-VREF+0.5 LSB)	<(-SGAIN+2SOFF+0.5 LSB)

Table 4. Output Coding

Tables 3 and 4 indicate the output code size and output coding of the CS5501/CS5503 in its various modes. The calibration equations which represent the CS5501/CS5503 transfer function are shown in Figure 10.

DOUT = Slope (AIN - Unipolar Offset) + 0.5 LSB

a. Unipolar Calibration

CS5501

DOUT = Slope (AIN - Bipolar Offset) + 2^{15} + 0.5 LSB16

CS5503

DOUT = Slope(AIN - Bipolar Offset) + 2^{19} + 0.5 LSB20

b. Bipolar Calibration

Figure 10. Calibration Equations

Underrange And Overrange Considerations

The input signal range of the CS5501/CS5503 will be determined by the mode in which the part is calibrated. Table 4 indicates the input signal range in the various modes of operation. If the input signal exceeds the full scale point the converter will output all ones. If the signal is less than the zero scale point (in unipolar) or more negative in magnitude than minus the full scale point (in bipolar) it will output all zeroes.

Note that the modulator-filter combination in the chip CS5501/CS5503 is designed to accurately convert and filter input signals with noise excursions which extend up to 100 mV below the analog value which produces all zeros out or above the analog value which produces all ones out. Overrange noise excursions greater than 100 mV may increase output noise.

All pins of the CS5501/CS5503 include diodes which clamp the input signals to within the positive and negative supplies. If a signal on any pin (including AIN) exceeds the supply voltage (either

+ or -) a clamp diode will be forward-biased. Under these fault conditions the CS5501/CS5503 might be damaged. Under normal operating conditions (with the power supplies established), the device will survive transient currents through the clamp diodes up to 100 mA and continuous currents up to 10 mA. The drive current into the AIN pin should be limited to a safe value if an overvoltage condition is likely to occur. See the application note "Buffer Amplifiers for the CS501X Series of A/D Converters" for further discussion on the clamp diode input structure and on current limiting circuits.

System Synchronization

If more than one CS5501/CS5503 is included in a system which is operating from a common clock, all of the devices can be synchronized to sample and output at exactly the same time. This can be accomplished in either of two ways. First, a single CAL signal can be issued to all the CS5501/CS5503's in the system. To insure synchronization on the same clock signal the CAL signal should go low on the falling edge of CLKIN. Or second, a common $\overline{\text{SLEEP}}$ control signal can be issued. If the $\overline{\text{SLEEP}}$ signal goes positive with the appropriate set up time to CLKIN, all parts will be synchronized on the same clock cycle.

Analog Input Impedance Considerations

The analog input of the CS5501/CS5503 can be modeled as illustrated in Figure 11. A 20 pF capacitor is used to dynamically sample the input signal. Every 64 CLKIN cycles the switch alternately connects the capacitor to the output of the buffer and then directly to the AIN pin. Whenever the sample capacitor is switched from the output of the buffer to the AIN pin, a small packet of charge (a dynamic demand of current) will be required from the input source to settle the voltage on the sample capacitor to its final value. The voltage at the output of the buffer may differ up to 100 mV from the actual input voltage due to the

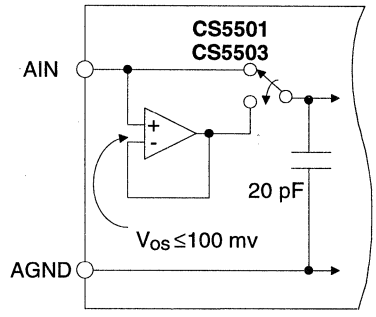


Figure 11. Analog Input Model

offset voltage of the buffer. Timing allows 64 cycles of master clock (CLKIN) for the voltage on the sample capacitor to settle to its final value. The equation which defines settling time is:

$$V_e = V_{max}\, e^{-t/RC}$$

Where Ve is the final settled value, V_{max} is the maximum error voltage value of the input signal, R is the value of the input source resistance, C is the 20 pF sample capacitor plus the value of any stray or additional capacitance at the input pin. The value of t is equal to 64/CLKIN.

V_{max} occurs the instance when the sample capacitor is switched from the buffer output to the AIN pin. Prior to the switch, AIN has an error estimated as being less than or equal to V_e. V_{max} is equal to the prior error (V_e) plus the additional error from the buffer offset. The estimate for V_{max} is:

$$V_{max} = V_e + 100mV\frac{20pF}{(20pF+C_{EXT})}$$

Where C_{EXT} is the combination of any external or stray capacitance.

From the equation which defines settling time, an equation for the maximum acceptable source resistance is derived

equation which defines settling time, an equation for the maximum acceptable source resistance is derived

$$Rs_{max} = \frac{-64}{CLKIN(20pF+C_{EXT})\ \ln\left[\frac{V_e}{V_e + \frac{20pF(100mv)}{(20pF+C_{EXT})}}\right]}$$

This equation assumes that the offset voltage of the buffer is 100 mV, which is the worst case. The value of Ve is the maximum error voltage which is acceptable.

For a maximum error voltage (Ve) of 10 µV in the CS5501 (1/4LSB at 16-bits) and 600 nV in the CS5503 (1/4LSB at 20-bits), the above equation indicates that when operating from a 4.096 MHz CLKIN, source resistances up to 84 kΩ in the CS5501 or 64 kΩ in the CS5503 are acceptable in the absence of external capacitance (C_{EXT} = 0). If higher input source resistances are desired the master clock rate can be reduced to yield a longer settling time for the 64 cycle period.

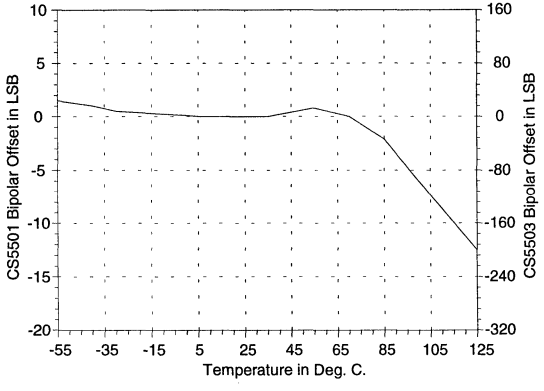


Figure 12. Typical Self-Cal Bipolar Offset vs. Temperature After Calibration at 25 °C

Analog Input Drift Considerations

The CS5501/CS5503 analog input uses chopper-stabilization techniques to minimize input offset drift. Charge injection in the analog switches and leakage currents at the sampling node are the primary sources of offset voltage drift in the converter. Figure 12 indicates the typical offset drift due to temperature changes experienced after calibration at 25 °C. Drift is relatively flat up to about 75 °C. Above 75 °C leakage current becomes the dominant source of offset drift. Leakage currents approximately double with each 10 °C of temperature increase. Therefore the offset drift due to leakage current increases as the temperature increases. The value of the voltage on the sample capacitor is updated at a rate determined by the master clock, therefore the amount of offset drift which occurs will be proportional to the elapsed time between samples. In conclusion, the offset drift increases with temperature and is inversely proportional to the CLKIN rate. To minimize offset drift with increased temperature, higher CLKIN rates are desirable. At temperatures above 100 °C, a CLKIN rate above 1 MHz is recommended. The effects of offset drift due to temperature changes can be eliminated by recalibrating the CS5501/CS5503 whenever the temperature has changed.

Gain drift within the converter depends predominately upon the temperature tracking of internal capacitors. Gain drift is not affected by leakage currents, therefore gain drift is significantly less than comparable offset errors due to temperature increases. The typical gain drift over the specified temperature range is less than 2.5 LSBs for the CS5501 and less than 40 LSBs for the CS5503 .

Measurement errors due to offset drift or gain drift can be eliminated at any time by recalibrating the converter. Using the system calibration mode can also minimize offset and gain errors in the signal conditioning circuitry. The CS5501/CS5503 can be recalibrated at any temperature to remove the effects of these errors.

Linearity and differential non linearity are not significantly affected by temperature changes.

Filtering

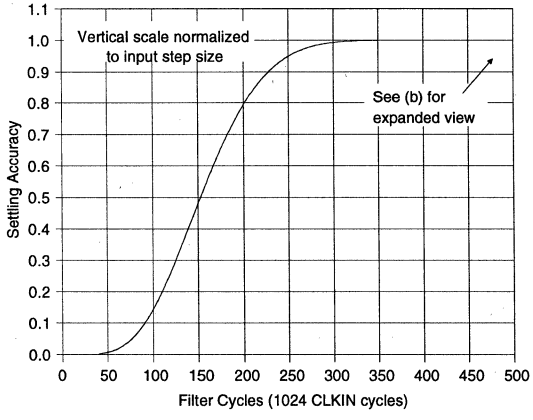
At the system level, the digital filter in the CS5501/CS5503 can be modeled exactly like an analog filter with a few minor differences. Digital filtering resides *behind* the A/D conversion and can thus reject noise injected during the conversion process (i.e. power supply ripple, voltage reference noise, or noise in the ADC itself). Analog filtering cannot.

Also, since digital filtering resides behind the A/D converter, noise riding unfiltered on a near-full-scale input could potentially overrange the ADC. In contrast, analog filtering removes the noise before it ever reaches the converter. To address this issue, the CS5501/CS5503 each contain an analog modulator and digital filter which reserve headroom such that the device can process signals with 100mV "excursions" above full-scale and still output accurately converted and filtered data. Filtered input signals above full-scale still result in an output of all ones.

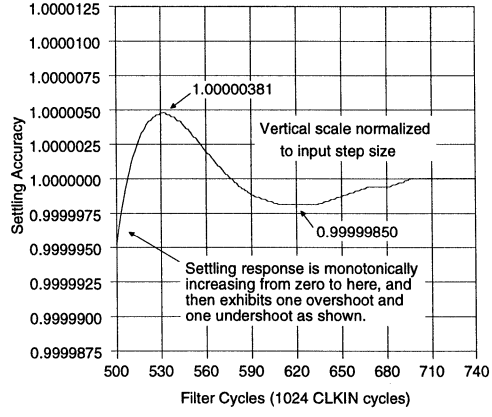
The digital filter's corner frequency occurs at CLKIN/409,600, where CLKIN is the master clock frequency. With a 4.096MHz clock, the filter corner is at 10Hz and the output register is updated at a 4kHz rate. CLKIN frequency can be reduced with a proportional reduction in the filter corner frequency and in the update rate to the output register. A plot of the filter response is shown in the specification tables section of this data sheet.

Both the CS5501/CS5503 employ internal digital filtering which creates a 6-pole Gaussian relationship. With the corner frequency set at 10Hz for minimized settling time, the CS5501/CS5503 offer approximately 55dB rejection at 60Hz to signals coming into either the AIN or VREF pins. With a 5Hz cut-off, 60Hz rejection increases to more than 90dB.

The digital filter (rather than the analog modulator) dominates the converters' settling for step-function inputs. Figure 13 illustrates the settling characteristics of the filter. The vertical axis is normalized to the input step size. The horizontal axis is in filter cycles. With a full scale input step (2.5 V in unipolar mode) the output will exhibit an overshoot of about 0.25 LSB_{16} in the CS5501 and 4 LSB_{20} in the CS5503.



(a) Settling Time Due to Input Step Change



(b) Expanded Version of (a)

Anti-Alias Considerations

The digital filter in the CS5501/CS5503 does not provide rejection around integer multiples of the oversampling rate [(N*CLKIN)/256, where N = 1,2,3,...]. That is, with a 4.096 MHz master clock the noise on the analog input signal within the narrow ±10 Hz bands around the 16 kHz, 32 kHz, 48 kHz, etc., passes unfiltered to the digital output. Most broadband noise will be very well filtered because the CS5501/CS5503 use a very high oversampling ratio of 800 (16 kHz: 2x10 Hz). Broadband noise is reduced by:

$$e_{out} = e_{in}\sqrt{2f_{-3dB}/f_s}$$
$$e_{out} = 0.035\ e_{in}$$

where e_{in} and e_{out} are rms noise terms referred to the input. Since f_{-3dB} equals CLKIN/409,600 and f_s equals CLKIN/256, the digital filter reduces white, broadband noise by 96.5% independent of the CLKIN frequency. For example, a typical operational amplifier's 50µV rms noise would be reduced to 1.75µV rms (0.035 LSB's rms at the 16-bit level in the CS5501 and 0.4 LSB's rms at the 20-bit level in the CS5503).

Simple high frequency analog filtering in the signal conditioning circuitry can aid in removing energy at multiples of the sampling rate.

Bits of Output Accuracy	Filter Cycles	CLKIN Cycles
9	340	348,160
10	356	364,544
11	389	398,336
12	435	445,440
13	459	470,016
14	475	486,400
15	486	497,664
16	495	506,880
17	500	512,000
18	504	516,096
19	506	518,144
20	507	519,168

Table 5. Settling Time of the 6 Pole Low Pass Filter in the CS5501 to 1/2 LSB Accuracy with a Full Scale Step Input

Post Filtering

Post filtering is useful to enhance the noise performance of the CS5503. With a constant input voltage the output codes from the CS5503 will exhibit some variation due to noise. The CS5503 has typically 1.6 LSB_{20} rms noise in its output codes. Additional variation in the output codes can arise due to noise from the input signal source and from the voltage reference. Post filtering (digital averaging) will be necessary to achieve less than 1 LSB p-p noise at the 20-bit level. The CS5503 has peak noise less than the 18-bit level without additional filtering if care is exercised in the design of the voltage reference and the input signal condition circuitry. Noise in the bandwidth from dc to 10 Hz on both the AIN and VREF inputs should be minimized to ensure maximum performance. As the amount of noise will be highly system dependent, a specific recommendation for post filtering for all applications cannot be stated. The following guidelines are helpful. Realize that the digital filter in the CS5503, like any other low pass filter, acts as an information storage unit. The filter retains past information for a period of time even after the input signal has changed. The implication of this is that immediately sequential 20-bit updates to the serial port contain highly correlated information. To most efficiently post filter the CS5503 output data, uncorrelated samples should be used. Samples which have sufficiently reduced correlation can be obtained if the CS5503 is allowed to execute 200 filter cycles between each subsequent data word collected for post filtering.

The character of the noise in the data will influence the post filtering requirements. As a general rule, averaging N uncorrelated data samples will reduce noise by $1/\sqrt{N}$. While this rule assumes that the noise is white (which is true for the CS5503 but not true for all real system signals between dc and 10Hz), it does offer a starting point for developing a post filtering algorithm for removing the noise from the data. The algorithm

will have to be empirically tested to see if it meets the system requirements. It is recommended that any testing include input signals across the entire input span of the converter as the signal level will affect the amount of noise from the reference input which is transferred to the output data.

Voltage Reference

The voltage reference applied to the VREF input pin defines the analog input range of the CS5501/CS5503. The preferred reference is 2.5V, but the device can typically accept references from 1V to 3V. Input signals which exceed 2.6V (+ or -) can cause some linearity degradation. Figure 14 illustrates the voltage reference connections to the CS5501/CS5503.

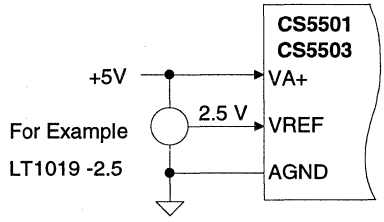


Figure 14. Voltage Reference Connections

The circuitry inside the VREF pin is identical to that as seen at the AIN pin. The sample capacitor (see Figure 12) requires packets of charge from the external reference just as the AIN pin does. Therefore the same settling time requirements apply. Most reference IC's can handle this dynamic load requirement without inducing errors. They exhibit sufficiently low output impedance and wide enough bandwidth to settle to within the necessary accuracy in the requisite 64 CLKIN cycles.

Noise from the reference is filtered by the digital filter, but the reference should be chosen to minimize noise below 10 Hz. The CS5501/CS5503 typically exhibit 0.1 LSB rms and 1.6 LSB rms noise respectively. This specification assumes a clean reference voltage. Many monolithic band-gap references are available which can supply 2.5 V for use with the CS5501/CS5503. Many of these devices are not specified for noise, especially in the 0.1 to 10 Hz bandwidth. Some of these devices may exhibit noise characteristics which degrade the performance of the CS5501/CS5503.

Power Supplies And Grounding

The CS5501/CS5503 use the analog ground connection, AGND, as a measurement reference node. It carries no power supply current. The AGND pin should be used as the reference node for both the analog input signal and for the reference voltage which is input into the VREF pin.

The analog and digital supply inputs are pinned out separately to minimize coupling between the analog and digital sections of the chip. To achieve maximum performance, all four supplies for the CS5501/CS5503 should be decoupled to their respective grounds using 0.1 µF capacitors. This is illustrated in the System Connection Diagram, Figure 15, at the beginning of this data sheet.

As CMOS devices, the CS5501/CS5503 require that the positive analog supply voltage always be greater than or equal to the positive digital supply voltage. If the voltage on the positive digital supply should ever become greater than the voltage on the positive analog supply, diode junctions in the CMOS structure which are normally reverse-biased will become forward-biased. This may cause the part to draw high currents and experience permanent damage. The connections shown in Figure 15 eliminate this possibility.

To ensure reliable operation, be certain that power is applied to the part before signals at AIN, VREF, or the logic input pins are present. If current is supplied into any pin before the chip is powered-up, latch-up may result. As a system, it is desirable to power the CS5501/CS5503, the volt-

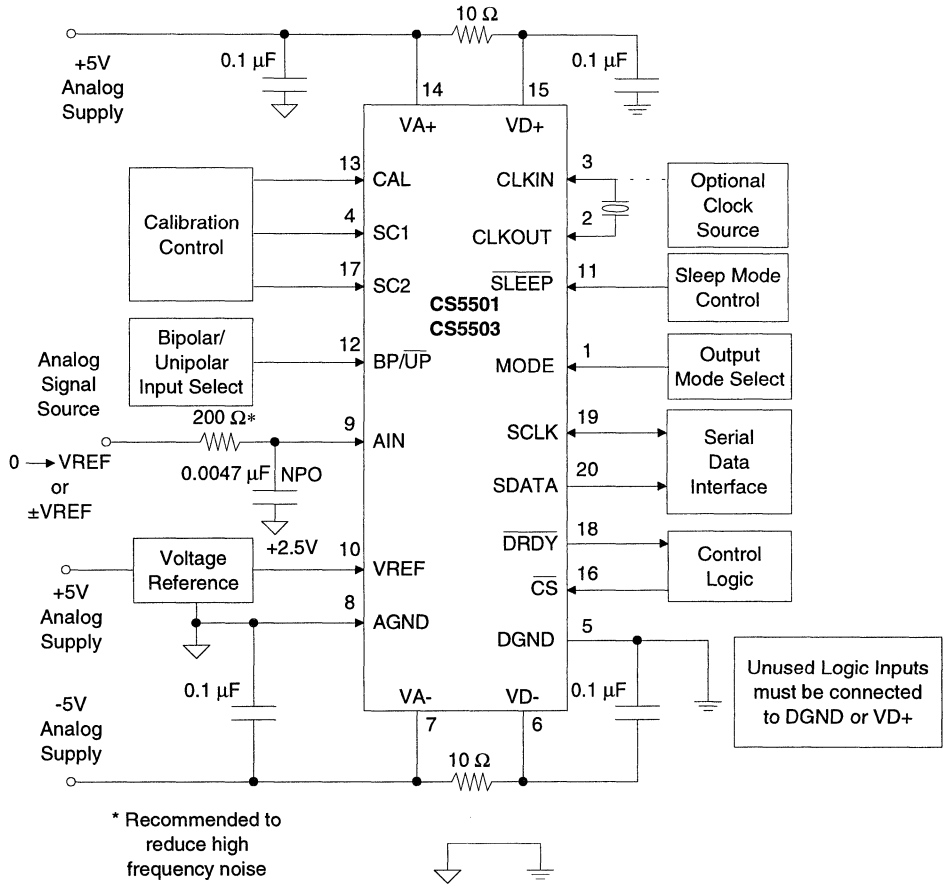


Figure 15. Typical Connection Diagram

age reference, and the analog signal conditioning circuitry from the same primary source. If separate supplies are used, it is recommended that the CS5501/CS5503 be powered up first. If a common power source is used for the analog signal conditioning circuitry as well as the A/D converter, this power source should be applied before application of power to the digital logic supply.

The CS5501/CS5503 exhibit good power supply rejection for frequencies within the passband (dc to 10 Hz). Any small offset or gain error caused by long term drift of the power supplies can be removed by recalibration. Above 10 Hz the digital filter will provide additional rejection. When the benefits of the digital filter are added to the regular power supply rejection the effects of line frequency variations (60 Hz) on the power supplies will be reduced greater than 120 dB. If the supply voltages for the CS5501/CS5503 are generated with a dc-dc converter the operating frequency of the dc-dc converter should not operate at the sampling frequency of the CS5501/CS5503 or at integer multiples thereof. At these frequencies the digital filter will not aid in power supply rejection. See *Anti-Alias Considerations* section of this data sheet.

The recommended system connection diagram for the CS5501/CS5503 is illustrated in Figure 15. Note that any digital logic inputs which are to be unused should be tied to either DGND or the VD+ as appropriate. They should not be left floating; nor should they be tied to some other logic supply voltage in the system.

Power-Up and Initialization

Upon power-up, a calibration cycle must be initiated at the CAL pin to insure a consistent starting condition and to initially calibrate the device. The CAL pin must be strobed high for a minimum of 4 clock cycles. The falling edge will initiate a calibration cycle. A simple power-on reset circuit can be built using a resistor and capacitor (see Figure 16). The resistor and capacitor values should allow for clock or oscillator startup time, and the voltage reference stabilization time.

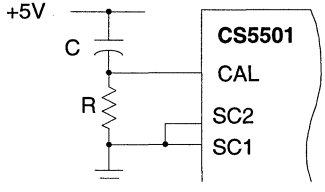


Figure 16. Power-On Reset Circuitry (Self-Calibration Only)

Due to the devices' low power dissipation and low temperature drift, no warm-up time is required to accommodate any self-heating effects.

Sleep Mode

The CS5501/CS5503 include a sleep mode ($\overline{\text{SLEEP}}$ = DGND) which shuts down the internal analog and digital circuitry reducing power consumption to less than 10 µW. All calibration coefficients are retained in memory such that no time is required after "awakening" for recalibration. Still, the CS5501/CS5503 will require time for the digital filter to settle before an accurate reading will occur after a rising edge on $\overline{\text{SLEEP}}$ occurs.

Battery Backed-Up Calibrations

The CS5501/CS5503 use SRAM to store calibration information. The contents of the SRAM will be lost whenever power is removed from the chip. Figure 17 shows a battery back-up scheme that can be used to retain the calibration memory during system down time and/or protect it against intermittent power loss. Note that upon loss of power, the $\overline{\text{SLEEP}}$ input goes low, reducing power consumption to just 10 µW. Lithium cells of 3.6 V are available which average 1750 mA-hours before they drop below the typical 2 V memory-retention specification of the CS5501/CS5503.

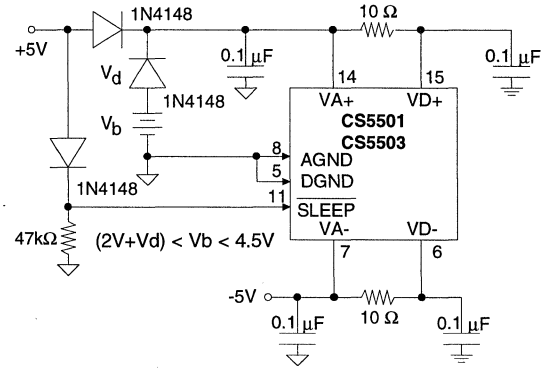


Figure 17. Example Calibration Memory Battery Back-Up Circuit

When $\overline{\text{SLEEP}}$ is active ($\overline{\text{SLEEP}}$ = DGND), both VD+ and VA+ must remain powered to no less than 2 V to retain calibration memory. The VD- and VA- voltages can be reduced to 0 V but must not be allowed to go above ground potential. The negative supply must exhibit low source impedance in the powered-down state as the current into the VA+ pin flows out the VA- pin. (AGND is only a reference node. No power supply current flows in or out of AGND.) Care should be taken

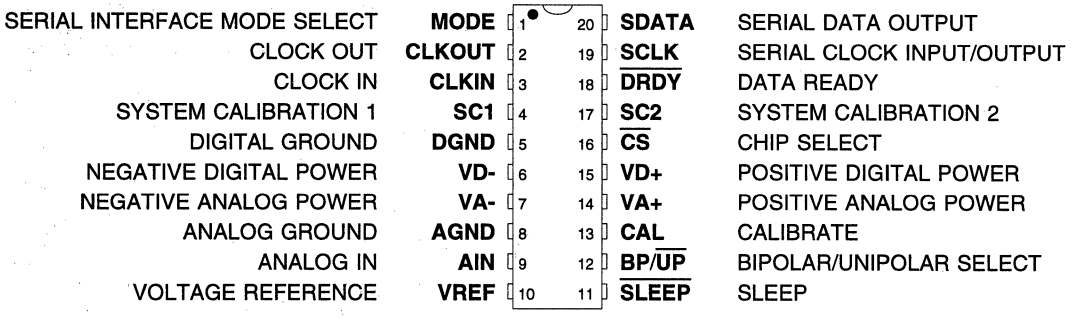
to ensure that logic inputs are maintained at either VD+ ar DGND potential when $\overline{\text{SLEEP}}$ is low.

Note that battery life could be shortened if the +5 V supply drops slowly during power-down. As the supply drops below the battery voltage but not yet below the logic threshold of the $\overline{\text{SLEEP}}$ pin, the battery will be supplying the CS5501/CS5503 at full power (typically 3 mA). Faster transitions at $\overline{\text{SLEEP}}$ can be triggered using a resistive divider or a simple resistor network to generate the $\overline{\text{SLEEP}}$ input from the +5 V supply.

Output Loading Considerations

To maximize performance of the CS5501/CS5503, the output drive currents from the digital output lines should be minimized. It is recommended that CMOS logic gates (4000B, 74HC, etc.) be used to provide minimum loading. If it is necessary to drive an opto-isolator the outputs of the CS5501/CS5503 should be buffered. An easy means of driving the LED of an opto-isolator is to use a 2N7000 or 2N7002 low cost FET.

PIN DESCRIPTIONS



* Pinout applies to both DIP and SOIC packages

Clock Generator

CLKIN; CLKOUT -Clock In; Clock Out, Pins 3 and 2.

A gate inside the CS5501/CS5503 is connected to these pins and can be used with a crystal or ceramic resonator to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock can be input to the CLKIN pin as the master clock for the device. When not in SLEEP mode, a master clock (CLKIN) should be present at all times.

Serial Output I/O

MODE -Serial Interface Mode Select, Pin 1.

Selects the operating mode of the serial port. If tied to VD- (-5V), the CS5501 will operate in the UART-compatible AC mode for Asynchronous Communication. The SCLK pin will operate as an *input* to set the data rate, and data will transmit *formatted* with one start and two stop bits. If MODE is tied to DGND, the CS5501/CS5503 will operate in the SEC (Synchronous External-Clocking) mode, with the SCLK pin operating as an *input* and the output appearing MSB-first. If MODE is tied to VD+ (+5V), the CS5501/CS5503 will operate in its SSC (Synchronous Self-Clocking) mode, with SCLK providing a serial clock *output* of CLKIN/4 (25% duty-cycle).

$\overline{\text{DRDY}}$ -Data Ready, Pin 18.

$\overline{\text{DRDY}}$ goes low every 1024 cycles of CLKIN to indicate that new data has been placed in the output port. $\overline{\text{DRDY}}$ goes high when all the serial port data is clocked out, when the serial port is being updated with new data, when a calibration is in progress, or when $\overline{\text{SLEEP}}$ is low.

$\overline{\text{CS}}$ -Chip Select, Pin 16.

An input which can be enabled by an external device to gain control over the serial port of the CS5501/CS5503.

SDATA -Serial Data Output, Pin 20.

Data from the serial port will be output from this pin at a rate determined by SCLK and in a format determined by the MODE pin. It furnishes a high impedance output state when not transmitting data.

SCLK -Serial Clock Input/Output, Pin 19.

A clock signal at this pin determines the output rate of the data from the SDATA pin. The MODE pin determines whether the SCLK signal is an input or output. SCLK may provide a high impedance output when data is not being output from the SDATA pin.

Calibration Control Inputs

SC1; SC2 -System Calibration 1 and 2, Pins 4 and 17.

Control inputs to the CS5501/CS5503's calibration microcontroller for calibration. The state of SC1 and SC2 determine which of the calibration modes is selected for operation (see Table 2).

BP/$\overline{UP}$ -Bipolar/Unipolar Select, Pin 12.

Determines whether the CS5501/CS5503 will be calibrated to measure bipolar (BP/$\overline{UP}$ = VD+) or unipolar (BP/$\overline{UP}$ = DGND) input signals. Recalibration is necessary whenever the state of BP/$\overline{UP}$ is changed.

CAL -Calibrate, Pin 13.

If brought high for 4 clock cycles or more, the CS5501/CS5503 will reset and upon returning low a full calibration cycle will begin. The state of SC1, SC2, and BP/$\overline{UP}$ when CAL is brought low determines the type and length of calibration cycle initiated (see Table 2). Also, a single CAL signal can be used to strobe the CAL pins high on several CS5501/CS5503's to synchronize their operation. Any spurious glitch on this pin may inadvertently place the chip in Calibration mode.

Other Control Input

$\overline{SLEEP}$ -Sleep, Pin 11.

When brought low, the CS5501/CS5503 will enter a low-power state. When brought high again, the CS5501/CS5503 will resume operation without the need to recalibrate. After $\overline{SLEEP}$ goes high again, the device's output will settle to within +0.0007% of the analog input value within $1.3/f_{-3dB}$, where f_{-3dB} is the passband frequency. The $\overline{SLEEP}$ input can also be used to synchronize sampling and the output updates of several CS5501/CS5503's.

Analog Inputs

VREF -Voltage Reference, Pin 10.

Analog reference voltage input.

AIN -Analog Input, Pin 9.

Power Supply Connections

VD+ -Positive Digital Power, Pin 15.
Positive digital supply voltage. Nominally +5 volts.

VD- -Negative Digital Power, Pin 6.
Negative digital supply voltage. Nominally -5 volts.

DGND -Digital Ground, Pin 5.
Digital ground.

VA+ -Positive Analog Power, Pin 14.
Positive analog supply voltage. Nominally +5 volts.

VA- -Negative Analog Power, Pin 7.
Negative analog supply voltage. Nominally -5 volts.

AGND -Analog Ground, Pin 8.
Analog ground.

SPECIFICATION DEFINITIONS

Linearity Error

The deviation of a code from a straight line which connects the two endpoints of the A/D Converter transfer function. One endpoint is located 1/2 LSB below the first code transition and the other endpoint is located 1/2 LSB beyond the code transition to all ones. Units in percent of full-scale.

Differential Linearity

The deviation of a code's width from the ideal width. Units in LSB's.

Full-Scale Error

The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSBs.

Unipolar Offset

The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in unipolar mode (BP/$\overline{UP}$ low). Units in LSBs.

Bipolar Offset

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND) when in bipolar mode (BP/$\overline{UP}$ high). Units in LSBs.

Bipolar Negative Full-Scale Error

The deviation of the first code transition from the ideal when in bipolar mode (BP/$\overline{UP}$ high). The Ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSBs.

Positive Full-Scale Input Overrange

The absolute maximum positive voltage allowed for either accurate system calibration or accurate conversions. Units in volts.

Negative Full-Scale Input Overrange

The absolute maximum negative voltage allowed for either accurate system calibration or accurate conversions. Units in volts.

Offset Calibration Range

The CS5501/CS5503 calibrate their offset to the voltage applied to the AIN pin when in system calibration mode. The first code transition defines Unipolar Offset when BP/$\overline{UP}$ is low and the mid-scale transition defines Bipolar Offset when BP/$\overline{UP}$ is high. The Offset Calibration Range specification indicates the range of voltages applied to AIN that the CS5501 or CS5503 can accept and still calibrate offset accurately. Units in volts.

Input Span

The voltages applied to the AIN pin in system-calibration schemes define the CS5501/CS5503 analog input range. The Input Span specification indicates the minimum and maximum input spans from zero-scale to full-scale in unipolar, or from positive full scale to negative full scale in bipolar, that the CS5501/CS5503 can accept and still calibrate gain accurately. Units in volts.

Ordering Guide

Model Number	No. of Bits	Linearity Error (Max)	Temperature Range	Package
CS5501-AS	16	0.003%	-40 to +85°C	20 Lead SOIC
CS5501-BS	16	0.0015%	-40 to +85°C	20 Lead SOIC
CS5501-AP	16	0.003%	-40 to +85°C	20 Pin Plastic DIP
CS5501-BP	16	0.0015%	-40 to +85°C	20 Pin Plastic DIP
CS5501-CP	16	0.0012%	-40 to +85°C	20 Pin Plastic DIP
CS5501-SD	16	0.003%	-55 to +125°C	20 Pin Cerdip
CS5501-TD	16	0.0015%	-55 to +125°C	20 Pin Cerdip
CS5503-AS	20	0.003%	-40 to +85°C	20 Lead SOIC
CS5503-BS	20	0.0015%	-40 to +85°C	20 Lead SOIC
CS5503-AP	20	0.003%	-40 to +85°C	20 Pin Plastic DIP
CS5503-BP	20	0.0015%	-40 to +85°C	20 Pin Plastic DIP
CS5503-CP	20	0.0012%	-40 to +85°C	20 Pin Plastic DIP
CS5503-SD	20	0.003%	-55 to +125°C	20 Pin Cerdip
CS5503-TD	20	0.0015%	-55 to +125°C	20 Pin Cerdip

APPENDIX A: APPLICATIONS

Parallel Interface

Figures A1 and A2 show two serial-to-parallel conversion circuits for interfacing the CS5501 in its SSC mode to 16- and 8-bit systems respectively. Each circuit includes an optional 74HCT74 flip-flop to latch $\overline{\text{DRDY}}$ and generate a level-sensitive interrupt.

Both circuits require that the parallel read process be synchronized to the CS5501's operation. That is, the system must not try to enable the registers' parallel output while they are accepting serial data from the CS5501. The CS5501's $\overline{\text{DRDY}}$ falls just prior to serial data transmission and returns high as the last bit shifts out. Therefore, the $\overline{\text{DRDY}}$ pin can be polled for a *rising* transition directly, or it can be latched as a level-sensitive interrupt.

With the $\overline{\text{CS}}$ input tied low the CS5501 will shift out every available sample (4kHz word rate with a 4MHz master clock). Lower output rates (and interrupt rates) can be generated by dividing down the $\overline{\text{DRDY}}$ output and applying it to $\overline{\text{CS}}$.

Totally asynchronous interfaces can be created using a *Shift Data* control signal from the system which enables the CS5501's $\overline{\text{CS}}$ input and/or the shift registers' S1 inputs. The $\overline{\text{DRDY}}$ output can then be used to disable serial data transmission once an output word has been fully registered.

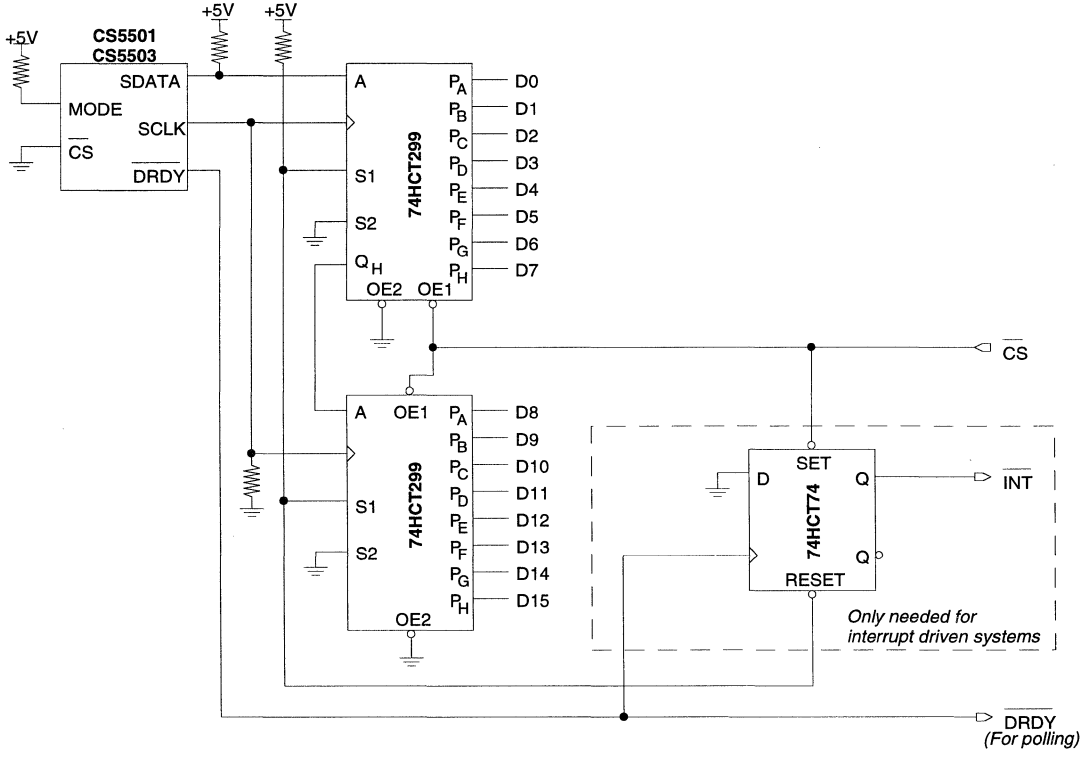


Figure A1. 16-bit Parallel Interface

In such asynchronous configurations the CS5501 is operated much like a successive-approximation converter with a *Convert* signal and a subsequent read cycle.

If it is required to latch the 16-bit data, then 2 74HC595 8-bit "shift register with latch" parts may be used instead of 74HC299's.

Serial Interfaces

Figures A3 to A8 offer both the hardware and software interfaces to several industry-standard microcontrollers using the CS5501's SEC and AC output modes. In each instance a system initialization routine is provided which configures the controller's I/O ports to accept the CS5501's serial data and clock outputs and/or generate its own serial clock. The routine also sets the CS5501 into a known state.

For each interface, a second subroutine is also provided which will collect one complete 16-bit output word from the CS5501. Figure A5 illustrates the detailed timing throughout the subroutine for one particular interface - the COPS family interface of Figure A4.

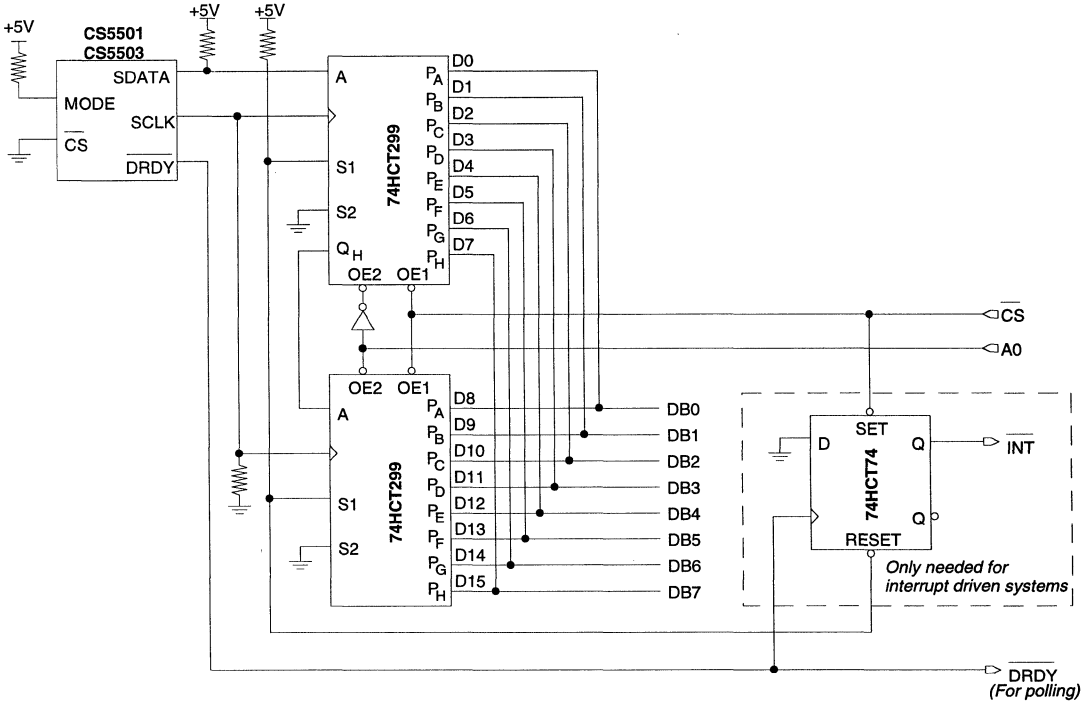


Figure A2. 8-Bit Parallel Interface

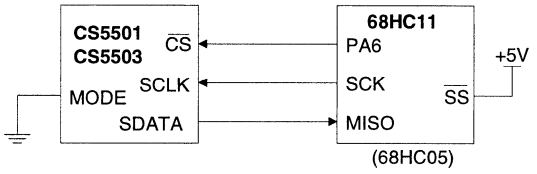


Figure A3. 68HC11/CS5501 Serial Interface

Notes:

1. CS5501 in *Synchronous External Clocking* mode.
2. Using 68HC11's SPI port. (Can use SCI and CS5501's Asynchronous mode.)
3. Maximum bit rate is 1.05 Mbps.

Assumptions:

1. PA6 used as $\overline{CS}$.
2. 68HC11 in single-chip mode.
3. Receive data via polling.
4. Normal equates for peripheral registers.
5. Data returned in register D.

Initial Code:

```
SPINIT: PSHA                ; Store temporary copy of A
        LDAA  #%x1xxxxxx    ; Bit 6 = 1, all others are don't cares
        STAA  PORTA         ; CS = 1, inactive; deselect CS5501
        LDAA  #$10          ;
        STAA  SPCR          ; Disable serial port
        LDAA  #%xx0110xx    ; SS-input, SCK-output,
                            ;  MOSI-output, MISO-input
        STAA  DDRD          ; Data direction register for port D
        LDAA  #$50          ; Enable serial port, CMOS outputs,
        STAA  SPCR          ;  master, highest clock rate (int. clk/2)
        LDAA  SPSR          ;
        LDAA  SPDR          ; Bogus read to clr port and SPIF flag
        PULA                ; Restore A
        RTS                 ;
```

Code to get word of data:

```
SP_IN:  LDAA  #%x0xxxxxx    ;
        STAA  PORTA         ; CS = 0, active; select CS5501
        STAA  SPDR          ; Put data in serial port to start clk
WAIT1:  LDAA  SPSR          ; Get port status
        BPL   WAIT1         ; If SPIF (MSB) 0, no data yet, wait
        LDAA  SPDR          ; Put most significant byte in A
        STAA  SPDR          ; Start serial port for second byte
WAIT2:  LDAB  SPSR          ; Get port status
        BPL   WAIT2         ; If SPIF (MSB) 0, no data yet, wait
        LDAB  #%x1xxxxxx    ;
        STAB  PORTA         ; CS = 1, inactive; deselect CS5501
        LDAB  SPDR          ; Put least significant byte in B
        RTS                 ;
```

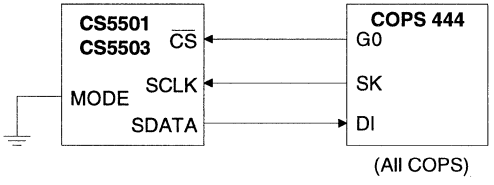


Figure A4. COPS/CS5501 Interface

Notes:

1. CS5501 in *Synchronous External Clocking* mode.
2. COPS 444 max baud = 62.5 kbps. (Others = 500 kbps)
3. See timing diagram for detailed timing.

Assumptions:

1. G0 used as $\overline{CS}$.
2. Register 0 (upper four nibbles) used to store 16-bit word.

Initial Code:

```
SPINIT: OGI   15            ; CS = 1, inactive; deselect CS5501
        RC                  ; Reset carry, used in next
        XAS                 ;  instruction to turn SK off
```

Code to get word of data:

```
SP_IN:  LBI   0,12          ; Point to start of data
                            ;  storage location
        SC                  ; Set carry - enables SK in
                            ;  XAS instruction
        OGI   14            ; CS = 0, active; select CS5501
        LEI   0             ; Shift register mode, S0 = 0
        XAS                 ; Start clocking serial port
        NOP                 ;
        NOP                 ; Wait for (first) M.S. nibble
GETNIB: NOP                 ;
        XAS                 ; Get nibble of data from SIO
        XIS                 ; Put nibble in memory, inc. pointer,
        JP    GETNIB        ;  if overflow, jump around this inst.
        RC                  ; Reset carry - disables SK in XAS
                            ;  instruction
        XAS                 ; Bogus read - stops SK
        OGI   15            ; CS = 1, inactive; deselect CS5501
        RET                 ;
```

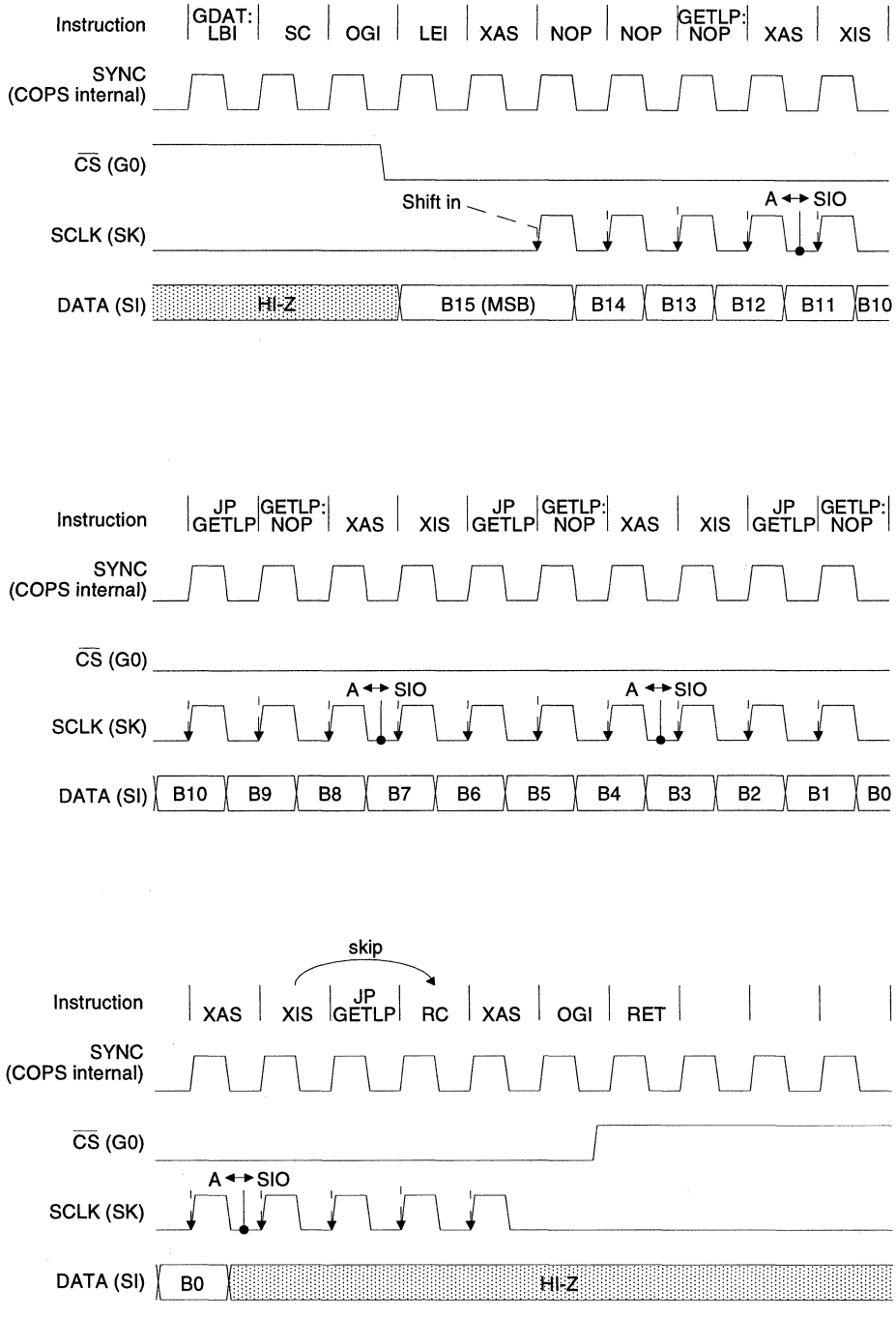


Figure A5. Serial Timing Example - COPS

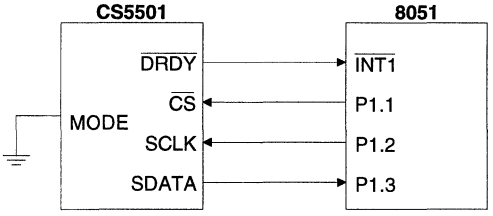


Figure A6. MCS51 (8051) /CS5501 Serial Interface

Notes:

1. CS5501 in *Synchronous External Clocking* mode.
2. Interrupt driven I/O on 8051 (For polling, connect DRDY to another port pin).

Assumptions:

1. INT1 external interrupt used.
2. Register bank 1, R6, R7 used to store data word, R7 MSbyte.
3. EA enabled elsewhere.

Initial Code:

```
CS      EQU   P1.1
SCLK    EQU   P1.2
DATA    EQU   P1.3
SPINIT: CLR   EX1          ; Disable INT1
        SETB  IT1          ; Set INT1 for falling edge triggered
        SETB  DATA         ; Set DATA to be input pin
        SETB  CS           ; CS = 1; deselect CS5501
        CLR   SCLK         ; SCLK low
        SETB  EX1          ; Enable INT1 interrupt
```

Code to get word of data:

```
        ORG 0003H
        LJMP  GETWD        ; Interrupt vector
GETWD:  PUSH  PSW          ; Save temp. copy
        PUSH  A            ; Save temp. copy
        MOV   PSW,#08      ; Set register bank 1 active
        MOV   R6,#8        ; number of bits in a byte
        CLR   CS           ; CS = 0; select CS5501
MSBYTE:SETB   SCLK         ; Toggle SCLK high
        MOV   C,DATA       ; Put bit of data into carry bit
        CLR   SCLK         ; Toggle SCLK low; next data bit
        RLC   A            ; Shift DATA bit into A register
        DJNZ  R6,MSBYTE    ; Dec. R6, if not 0, get another bit
        MOV   R7,A         ; Put MSbyte into R7
        MOV   R6,#8        ; Reset R6 to number of bits in byte
LSBYTE: SETB  SCLK         ; Toggle SCLK high
        MOV   C,DATA       ; Put bit of data into carry bit
        CLR   SCLK         ; Toggle SCLK low; next data bit
        RLC   A            ; Shift DATA bit into A register
        DJNZ  R6,LSBYTE    ; Dec. R6, if not 0, get another bit
        MOV   R6,A         ; Put LSbyte into R6
        SETB  CS           ; CS = 1; deselect CS5501
        POP   A            ; Restore original value
        POP   PSW          ; Restore original value
        RETI
```

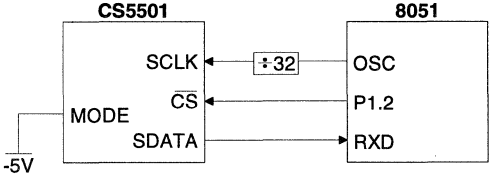


Figure A7. MCS51 (8051) /CS5501 UART Interface

Notes:

1. CS5501 in Asynchronous (UART-like) mode.
2. 8051 in mode 2, with OSC = 12 MHz, max baud = 375 kbps.

Assumptions:

1. P1.2 (port 1, bit 2) used as CS.
2. Using serial port mode 2, Baud rate = OSC/32.

(Assumptions cont.)

3. Word received put in A (ACC) and B registers, A = MSbyte.
4. No error checking done.
5. Equates used for peripheral names.

Initial Code:

```
SPINIT: SETB  SMOD         ; Set SMOD = 1, baud = OSC/32
        SETB  P1.2         ; CS = 1, inactive
        MOV   SCON,#1001000B    ; Enable serial port mode 2,
                           ;  receiver enabled, transmitter disabled
        CLR   ES           ; Disable serial port interrupts (polling)
        RET                ;
```

Code to get word of data:

```
SP_IN:  CLR   P1.2         ; CS = 0, active; select CS5501
        JNB   RI,$         ; Wait for first byte
        CLR   RI           ;
        MOV   A,SBUF       ; Put most significant byte in A
        JNB   RI,$         ; wait for second byte
        CLR   RI           ;
        MOV   B,SBUF       ; Put least significant byte in B
        SETB  P1.2         ; CS = 1, inactive; deselect CS5501
        RET                ;
```

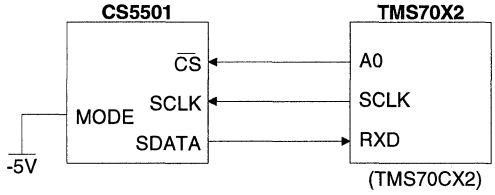


Figure A8. TMS70X2/CS5501 Serial Interface

Notes:

1. CS5501 in Asynchronous (UART-like) mode.
2. TMS70X2 in Isosynchronous mode.
3. TMS70X2 with 8 MHz master clock has max baud =1.0 Mbps.

Assumptions:

1. A0 used as $\overline{CS}$.
2. Receive data via polling.
3. Word received put in A and B upon return, A = MS byte.
4. No error checking done.
5. Normal equates for peripheral registers.

Initial Code:

```
SPINIT: DINT                    ;
        MOVP  %1,ADDR           ; A port is output
        MOVP  %1,APORT          ; A0 = 1, (CS is inactive)
        MOVP  %0,P17            ;
        MOVP  %>10,SCTLO        ; Resets port errors
        MOVP  %?x1x01101,SMODE  ; Set port for Isosync,
        MOVP  %?00x1110x,SCTLO  ;       8 bits, no parity
        MOVP  %07,T3DATA        ; Max baud rate
        MOVP  %?01000000,SCTL1  ; No multiprocessor;
                                ;       prescale = 4
        MOVP  %0,IOCNT1         ; Disable INT4 - will poll port
        PUSH  A                 ; Store original
        MOVP  RXBUF,A           ; Bogus read to clr receiver port flag
        POP   A                 ; Restore original
        EINT                    ;
        RET                     ;
```

Code to get word of data:

```
SP_IN:  MOVP  %0,APORT    ; CS active, select CS5501
WAIT1   BTJZP %2,SSTAT,WAIT1      ; Wait to receive first byte
        MOVP  RXBUF,A     ; Put most significant byte in reg. A
WAIT2   BTJZP %2,SSTAT,WAIT2      ; Wait to receive second byte
        MOVP  RXBUF,B     ; Put least significant byte in reg. B
        MOVP  %1,APORT    ; CS inactive, deselect CS5501
        RET               ;
```

Semiconductor Corporation

CDB5501/CDB5503

CS5501/CS5503 Evaluation Board

2

Features

- Operation with on-board clock generator, on-board crystal, or an off-board clock source.
- DIP switch selectable or micro port controllable:
  - Unipolar/Bipolar input range
  - Sleep Mode
  - All Cal Modes
- On-board Decimation Counter
- Multiple Data Output Interface Options:
  - RS-232 (CS5501)
  - Parallel Port (CS5501)
  - Micro Port (CS5501 & CS5503)

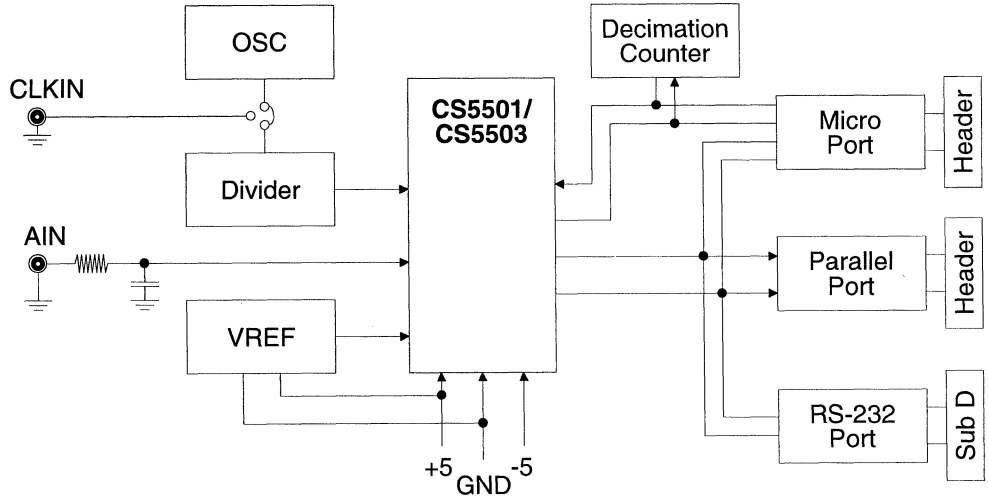
General Description

The CDB5501/CDB5503 is an evaluation board designed for maximum flexibility when evaluating the CS5501/CS5503 A/D converters. The board can easily be configured to evaluate all the features of the CS5501/CS5503, including changes in master clock rate, calibration modes, output decimation rates, and interface modes.

The evaluation board interfaces with most microcontrollers and allows full control of the features of the CS5501 or CS5503. DIP switch selectable control is also available in the event a microcontroller is not used. The evaluation board also offers computer data interfaces including RS-232 and parallel port outputs for evaluating the CS5501.

All calibration modes are selectable including Self-Cal, System Offset Cal, and System Offset and System Gain Cal. A calibration can be initiated at any time by pressing the CAL pushbutton switch.

ORDERING INFORMATION: CDB5501 or CDB5503



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

INTRODUCTION

The CDB5501/CDB5503 evaluation board provides maximum flexibility for controlling and interfacing to the CS5501/CS5503 A/D converters. The CS5501 or the CS5503 require a minimal amount of external circuitry. The devices can operate with a crystal (or ceramic resonator) and a voltage reference.

The evaluation board includes several clock source options, a 2.5 volt trimmable reference, and circuitry to support several data interface schemes. The board operates from +5 and -5 volt power supplies.

Evaluation Board Overview

The CDB5501/CDB5503 evaluation board includes extensive support circuitry to aid evaluation of the CS5501/CS5503. The support circuitry includes the following sections:

1) A clock generator which has an on-board oscillator and counter divider IC.
2) A 2.5 volt trimmable voltage reference.
3) A Decimation Counter.
4) A parallel output port (for CS5501 only).
5) An RS-232 interface (for CS5501 only).
6) A micro port (for CS5501 or CS5503).
7) DIP switch and CAL pushbutton.

Clock Generator

The CS5501/CS5503 can operate off its on-chip oscillator or an off-chip clock source. The evaluation board includes a 4.9152 MHz gate oscillator and counter-divider chain as the primary clock source for the CS5501/CS5503. The counter-divider outputs offer several jumper-selectable frequencies as clock inputs to the CS5501/CS5503. The 4.9152 MHz crystal frequency was chosen to allow the counter-divider chain to also provide the common serial data rates (1200, 2400, 4800, etc.) when the CDB5501 evaluation board is configured to provide RS-232 data output. If a different operating frequency for the CS5501/CS5503 is desired, three options exist. First, a BNC input is provided to allow an external CMOS (+5V) compatible clock to be used. Second, the crystal (Y1) in the on-board gate oscillator can be changed. Or, third, the on-chip oscillator of the CS5501/CS5503 can be used with a crystal connected in the Y2 position.

2. 5 Volt Reference

A 2.5 volt (LT1019CN8-2.5) reference is provided on the board. Potentiometer R9 allows the initial value of the reference to be accurately trimmed.

Decimation Counter

The CS5501/CS5503 updates its internal output register with a 16-bit word every 1024 clock cycles of the master clock. Each time the output register is updated the $\overline{\text{DRDY}}$ line goes low. Although output data is updated at a high rate it may be desirable in certain applications to activate the $\overline{\text{CS}}$ to read the data at a much lower rate. A decimation counter is provided on the board for this purpose. The counter reduces the rate at which the $\overline{\text{CS}}$ line of the CS5501 is activated by only allowing $\overline{\text{CS}}$ to occur at a sub-multiple of the $\overline{\text{DRDY}}$ rate.

Parallel Output Port (for CS5501 only)

The output data from the CS5501/CS5503 is in serial form. Some applications may require the data to be read in parallel format. Therefore the evaluation board includes two 8-bit shift registers with three-state outputs. Data from the CS5501 is shifted into the registers and then read out in 16-bit parallel fashion. The parallel port comes set up for 16-bit parallel output but can be reconfigured to provide two 8-bit reads. The parallel port supports the CS5501 only, since the CS5503 outputs 20-bit words.

RS-232 Port (for CS5501 only)

The CS5501 has a data output mode in which it formats the data to be UART compatible; each serial output byte is preceded by a start bit and terminated with two stop bits. Serial data in this format is commonly transferred using the RS-232 data interface. Therefore the evaluation board includes an RS-232 driver and output connector. The CS5503 does not provide this output mode.

Micro Port

The CS5501/CS5503 was designed to be compatible with many micro-controllers. Therefore the evaluation board provides access to all of the data output pins and the control pins of the CS5501/CS5503 on header connectors.

DIP Switch and CAL Pushbutton

Although all of the control lines to the CS5501/CS5503 are available on header connectors at the edge of the board, it is preferable to not require software control of all of these pins. Therefore DIP switch control is provided on some of these control lines. The CAL input to the CS5501/CS5503 is made available at a header pin for remote control, but pushbutton control of CAL is also provided.

Jumper Selections

The evaluation board has many jumper selectable options. This table describes the jumper selections available.

2

P1 Selects between the on-board 4.9152 MHz oscillator (INT) or an external (EXT) clock source as the input to the clock generator/ divider chain.

P2 Allows any of the counter/divider output clock rates to be selected as the input clock to the CS5501/CS5503.

P3 Allows selection of baud rate clocks when the CS5501 is in the UART compatible mode. When using the on-board 4.9152 MHz standard baud rates between 1200 and 19,200 are available.

P4 Selects the divide ratio of the Decimation Counter.

P5 Selects one of the three available output data modes of the CS5501 or one of two available output data modes of the CS5503.

P9 Enables the output of the Decimation Counter to control the $\overline{CS}$ line of the CS5501/CS5503.

P11 Connects the baud clock from the on-board clock divider as the input to the SCLK pin of the CS5501/CS5503.

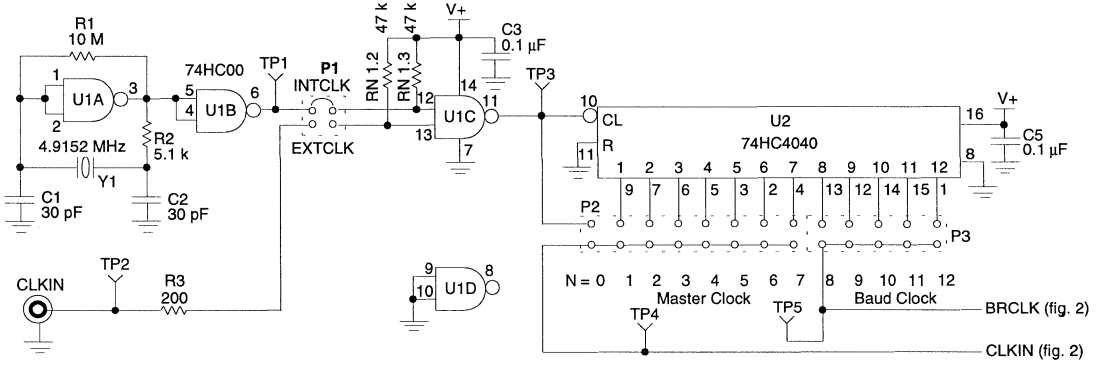


Figure 1. Clock Generator

Clock Options

Several clock source options are available. These include:

1) an external clock (+5 V CMOS-Compatible);
2) an on-board 4.9152 MHz crystal oscillator with a 2^n divider (n = 1, 2, ...7);
3) a 4.096 MHz crystal.

Connector P1 allows jumper selection of either an external clock or the on-board 4.9152 MHz crystal oscillator (See Figure 1 for schematic) as the clock source for the CLKIN signal on pin 3 of the CS5501/CS5503 (shown in Figure 2).

If the EXT position is selected, a CMOS-compatible clock signal (5 volt supply) should be input to the BNC connector labeled CLKIN. If the INT position is selected the 4.9152 MHz oscillator output is input to counter/divider IC U2. In either

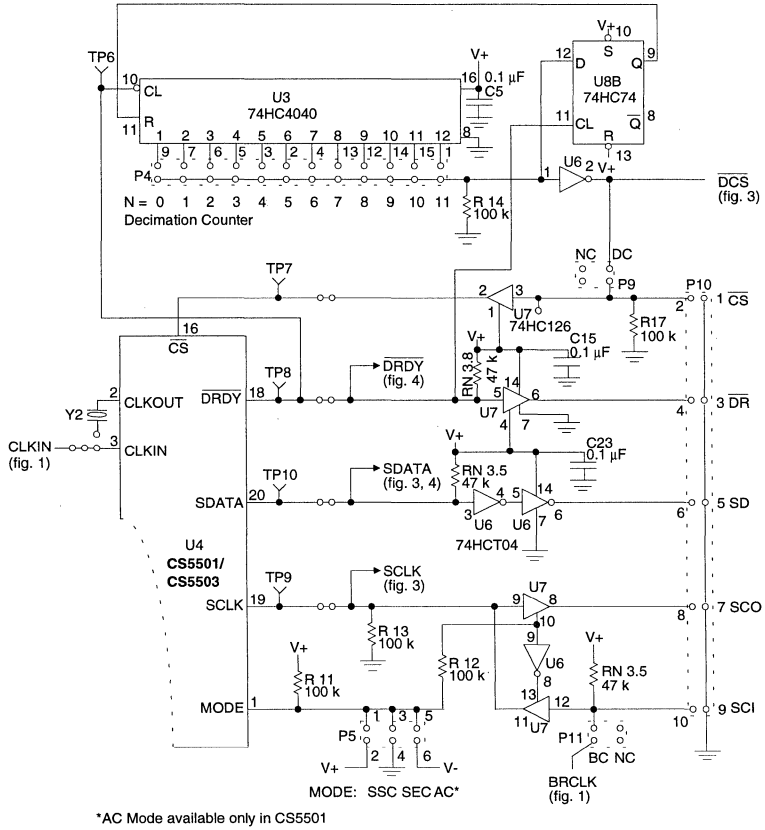


Figure 2. Decimation Counter / Microport

P-1	CLKIN Source to CS5501/CS5503
INT CLK	On-Board 4.9152 MHz OSC
EXT CLK	+5 CMOS CLKIN BNC

CLKIN Rate Selection (CLK/2^n) with INT CLK on P1 selected.
CLK = 4.9152 MHz

P-2	CLKIN Rate
0	4.9152 MHz
1	2.4576 MHz
2	1.2288 MHz
3	614.4 kHz
4	307.2 kHz
5	153.6 kHz+
6	76.8 kHz+
7	38.4 kHz* +

* Exceeds CLKIN Specifications of CS5501.
\+ Exceeds CLKIN specifications of CS5503.

Table 1. Clock Generator

case, the counter divides the input clock by 2n where n = 0, 1, ...7. Any of the binary sub-multiples of the counter input clock can be input to the CS5501/CS5503 by jumper selection on connector P2.

The CS5501/CS5503 contains its own on-chip oscillator which needs only an external crystal to function. Ceramic resonators can be used as well although ceramic resonators and low frequency crystals will require loading capacitors for proper operation.

To test the oscillator of the CS5501/CS5503 with a crystal (Y2) a jumper wire near crystal Y2 must be opened and another jumper wire soldered into the appropriate holes provided to connect the crystal to the chip. Additional holes are provided on the board for loading capacitors.

Data Output from the CS5501/CS5503

The CS5501 has three available data output modes (The CS5503 has two available data output modes). The operating mode of the part is determined by the input voltage level to the MODE (pin 1) pin of the device. Once a mode is selected, four other pins on the device are involved in data output. The first of these is the $\overline{\text{DRDY}}$ pin (pin 18). It is an output from the chip which signals whenever a new data word is available in the internal output register of the CS5501/CS5503. Data can then be read from the register, but only when the $\overline{\text{CS}}$ pin (pin 16) is low.

When $\overline{\text{CS}}$ is low, data bits are output in serial form on the SDATA pin (pin 20). In the Synchronous Self-Clocking mode of the CS5501/CS5503, the chip provides an output data clock from the SCLK pin (pin 19). This output clock is synchronous with the output data and can be used to clock the data into an external register.

In Synchronous External-Clocking and Asynchronous Communications modes of the CS5501, the SCLK pin is an input for an external clock which determines the rate at which data bits appear at the SDATA output pin. In the CS5503, only synchronous external-clocking mode is available.

The signals necessary for reading data from the CS5501/CS5503 are all available on connector P10 as shown in Figure 2.

P-5	Data Output Mode
SSC	Synchronous Self-Clocking
SEC	Synchronous External-Clocking
AC*	Asynchronous Communications

* Available in CS5501 only.

Table 2. Data Output Mode

CS5501/CS5503 Data Output Mode Selection

Connector P5 (see Figure 2) allows jumper selection of any one of the three data output modes. These modes are:

1) SSC (Synchronous Self-Clocking);
2) SEC (Synchronous External Clocking);
3) AC (Asynchronous Communication). (AC mode is available only in the CS5501)

SSC (Synchronous Self-Clocking) Mode

The SSC mode is designed for interface to those microcontrollers which allow external clocking of their serial inputs. The SSC mode also allows easy connection to serial-to-parallel conversion circuitry.

In the SSC mode serial data and serial clock are output from the CS5501/CS5503 whenever the $\overline{CS}$ line is activated. As illustrated in Figure 2, all of the signals are available at connector P10. If the $\overline{CS}$ signal is to be controlled remotely the jumper on P9 should be placed in the NC (No Connection) position. This removes the Decimation Counter output from controlling the $\overline{CS}$ line.

Data Output Interface: Parallel Port (for CS5501 evaluation only).

Whenever the CS5501 is operated in the SSC mode the 16-bit output data is clocked into two 8-bit shift registers. The registers have three-state parallel outputs which are available at P7 (see Figure 3). A flip-flop (U8A) is used to signal the remote reading device whenever the registers are updated. The $\overline{PDR}$ (Parallel Data Ready) signal from the flip-flop is available on P7. The Q-bar output from the flip-flop locks out any further updates to the registers until their data is read and a DACK (Data ACKnowledge) signal is received from the remote device.

Activation of the $\overline{CS}$ line determines the rate at which the CS5501 will attempt to update the output shift registers. Data will be shifted into the registers only if a DACK signal has occurred since the last update.

The $\overline{CS}$ line can be controlled remotely at P10 or by the output of the Decimation Counter. If $\overline{CS}$ is controlled remotely, the Decimation divide jumper on P4 should be placed in the "0" position. This insures that the $\overline{DCS}$ signal will occur at the same rate $\overline{CS}$ is activated. The positive going edge of $\overline{DCS}$ toggles the U8A flip-flop which signals an update to the parallel port.

The parallel registers are set up to be read in 16-bit parallel fashion but can be configured to be read separately as two 8-bit bytes on an 8-bit bus. To configure the board for byte-wide reads, the byte-wide jumpers must be soldered in place. In addition, for proper "one byte at a time" address selection, a connection on the circuit board needs to be opened and a jumper wire soldered in the proper place to determine which register is to be read when A0 is a "1" and vice versa. See Figure 3 for schematic details. The evaluation board component layout diagram, Figure 7, indicates the location of the byte-wide jumpers and A0 address selection jumpers.

After data is read from the registers a DACK (Data Acknowledge) signal is required from the off-board controller to reset flip-flop U8A. This enables the registers to accept data input once again.

The DRB and CSB signals on connector P10 should be used to monitor and control the CS5501 output to the serial to parallel conversion registers. Be aware that an arbitrarily timed DACK signal may cause the output data registers to be enabled in the middle of an output word if the $\overline{CS}$ signal to the CS5501 is not properly sequenced. This will result in incorrect data in the output registers.

If the Decimation Counter is used to control the output of the CS5501 (Jumper on P9 in the DC position), the CSB signal on P10 can be moni-

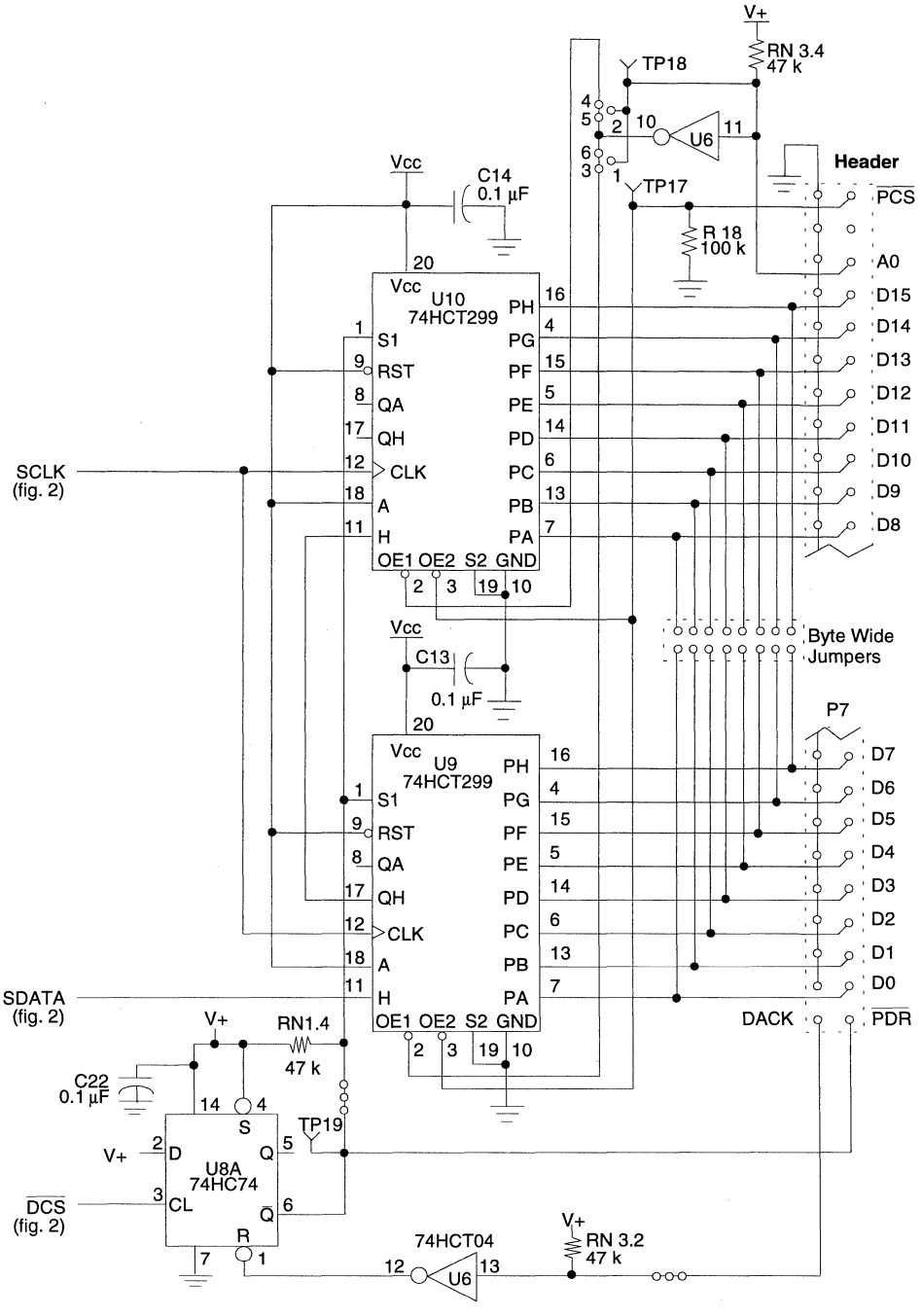


Figure 3. 16-Bit Parallel Port

tored to signal when data into the output registers is complete ($\overline{DCS}$ returns high). The DACK signal is not needed in this mode and the lockout signal to the the S1 inputs of registers U9 and U10 may be disabled by removing the connection on the circuit board. A place is provided on the board for this purpose. A pull-up resistor is provided on the S1 inputs of the registers if the connection is opened.

SEC (Synchronous External Clocking) Mode

The SEC mode enables the CS5501/CS5503 to be directly interfaced to microcontrollers which output a clock signal to synchronously input serial data to an input port. The CS5501/CS5503 will output its serial data at the rate determined by the clock from the microcontroller.

Connector P10 allows a microcontroller access to the CS5501/CS5503 signal lines which are necessary to operate in the SEC mode.

The CSB (chip select bar $\overline{CS}$) signal allows the microcontroller to control when the CS5501/CS5503 is to output data. The $\overline{DRB}$ (data ready bar) signal on P10 indicates to the microcontroller when data from the CS5501/CS5503 is available. Clock from the microcontroller is input into SCI (serial clock input) and data output from the CS5501/CS5503 is presented to the SD (serial data) pin of the P10 connector. Note that the jumpers on connectors P9 and P11 must be in the NC (no connection) position to allow the microcontroller full control over the signals on P10.

AC (Asynchronous Communication) Mode (for CS5501 evaluation only)

The AC mode enables the CS5501 to output data in a UART-compatible format. Data is output as two characters consisting of one start bit, eight data bits, and two stop bits each.

The output data rate can be set by a clock input to the SCI input at connector P10 (see Figure 2). The jumper on P11 must be in the NC position. Alternatively an output data bit rate can be selected as a sub-multiple of the external CLKIN signal to the board or as a sub-multiple of the on-board 4.9152 MHz oscillator. Counter IC U2 divides its input by 2n where n = 8, 9, ...12. One of these outputs can be jumper selected at connector P3 (see Figure 1). For example, if the 4.9152 MHz oscillator is selected as the input to IC U2 then a 1200 baud rate clock can be selected with the jumper at n = 12. Table 3 indicates the baud rates available at connector P3 when the 4.9152 MHz oscillator is used. If the on-board baud clock is to be used, the jumper on connector P11 should be in the BC (Baud Clock) position.

Data Output Interface: RS-232 (for CS5501 evaluation only).

The RS232 port is depicted in Figure 4. Sub-D connector P6 along with interface IC U11 provides the necessary circuitry to connect the CS5501 to an RS-232 input of a computer. For proper operation the AC (Asynchronous Communication) data output mode must be selected. In addition, an appropriate baud clock needs to be

Baud Rate Clock Divider ($CLK/2^n$) with INT CLK on P1 selected. CLK = 4.9152 MHz

P-3	Baud Rate CLK Divider
8	19.2 kHz
9	9.6 kHz
10	4.8 kHz
11	2.4 kHz
12	1.2 kHz

On-Board Baud Rate Clock Input to CS5501/CS5503 SCLK Input.

P-11	SCLK Input to CS5501/CS5503
NC	No Connection
BC	Baud Clock

Table 3. On-Board Baud Rate Generator

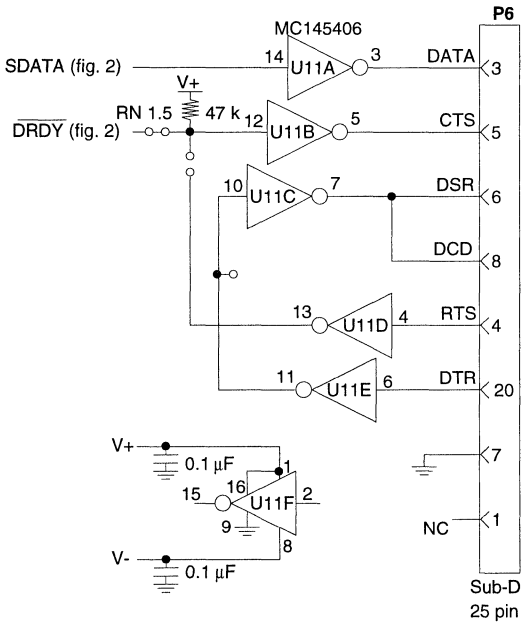


Figure 4. RS-232 Port

input to the CS5501. See AC (Asynchronous Communication) mode mentioned earlier for an explanation of the baud rate clock generator and the data format of the output data in the AC mode.

The $\overline{DRDY}$ output from the CS5501 signals the CTS (Clear To Send) line of the RS-232 interface when data is available. The Decimation Counter can be used to determine how frequently output data is to be transmitted.

The RS-232 interface on the evaluation card is functionally adequate but it is not compliant with the EIA RS-232 standard. When the MC145406 RS-232 receiver/driver chip is operated off of ± 5 volt supplies rather than ± 6 volts (see the MC145406 data sheet for details) its driver output swing is reduced below the EIA specified limits. In practical applications this signal swing limitation only reduces the length of cable the circuit is capable of driving.

DECIMATION COUNTER

Each time a data word is available for output from the CS5501/CS5503, the $\overline{DRDY}$ line goes low, provided the output port was previously emptied. If the $\overline{DRDY}$ line is directly tied to the $\overline{CS}$ input of the CS5501/CS5503, the converter will output data every time a data word is presented to the output pin. In some applications it is desirable to reduce the output word rate. The rate

Decimation Counter Accumulates 2^{n+1} $\overline{DRDY}$ Pulses Before $\overline{CS}$ is Enabled.

P-4	2^{n+1}
0	2
1	4
2	8
3	16
4	32
5	64
6	128
7	256
8	512
9	1024
10	2048
11	4096

P-9	DC Output to $\overline{CS}$
NC	No Connection
DC	Decimation Counter

Table 4. Decimation Counter Control

can be reduced by lowering the rate at which the $\overline{CS}$ line to the chip is enabled. The CDB5501/CDB5503 evaluation board uses a counter, IC U3 for this purpose. It is known as a decimation counter (see Figure 2). The outputs of the counter are available at connector P4. The counter accumulates 2n+1 counts (n = 0, 2, ...11) at which time the selected output enables the $\overline{CS}$ input to the CS5501/CS5503 (if the jumper in P9 is in the DC, Decimation Counter, position). The

Switch	ON	OFF
SW1-1	SC2 = 0	SC2 = 1
SW1-2	SC1 = 0	SC1 = 1
SW1-3	UNIPOLAR	BIPOLAR
SW1-4	SLEEP	AWAKE

Table 5. DIP Switch Selections

CAL	SC1	SC2	Cal Type	ZS Cal	FS Cal	Sequence
↴	0	0	Self-Cal	AGND	VREF	One Step
↴	1	1	System Offset	AIN	-	1st Step
↴	0	1	& System Gain	-	AIN	2nd Step
↴	1	0	System Offset	AIN	VREF	One Step

Table 6. Calibration Mode Table

"D" input to flip-flop U8B is enabled to a "1" at the same time $\overline{CS}$ goes low. When $\overline{DRDY}$ returns high flip-flop U8B is toggled and resets the counter back to zero which terminates the $\overline{CS}$ enable. The counter then accumulates counts until the selected output activates $\overline{CS}$ low once again.

DIP Switch Selections/Calibration Initiation

Several control pins of the CS5501/CS5503 can be level activated by DIP switch selection, or by microcontroller at P8, as shown in Figure 5. DIP switch SW1 selections are depicted in Tables 5 and 6. The CAL pushbutton is used to initiate a calibration cycle in accordance with DIP switch positions 1 and 2. The CAL pushbutton should be activated any time power is first applied to the board or any time the conversion mode (BP/$\overline{UP}$) is changed on the DIP switch. Remote control of the CAL signal is available on connector P8. Connector P8 also allows access to the DIP switch functions by a microcomputer/microcontroller. The DIP switches should be placed in the off position if off-board control of the signals on connector P8 is implemented.

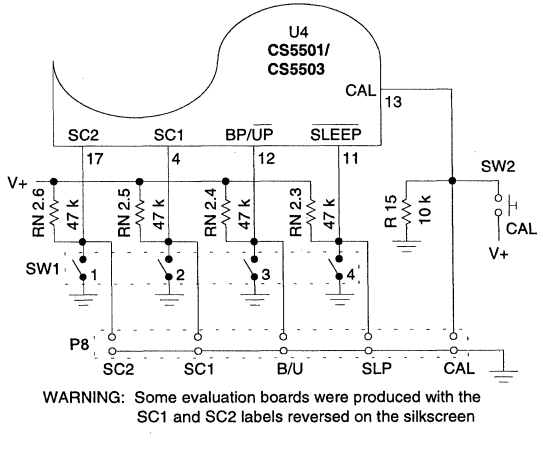


Figure 5. DIP Switch / Header Control Pin Selection

Voltage Reference

The evaluation board includes a 2.5 volt reference. Potentiometer R9 can be used to trim the reference output to a precise value.

Analog Input Range: Unipolar Mode

The value of the reference voltage sets the analog input signal range. In unipolar mode the analog input range extends from AGND to VREF. If the analog input goes above VREF the converter will output all "1's". If the input goes below AGND, the CS5501/CS5503 will output all "0's".

Analog Input Range: Bipolar Mode

The analog signal input range in the bipolar mode is set by the reference to be from +VREF to -VREF. If the input signal goes above +VREF, the CS5501/CS5503 will output all "1's". Input signals below -VREF cause the output data to be all "0's".

Analog Input: Overrange Precautions

In normal operation the value of the reference voltage determines the range of the analog input signal. Under abnormal conditions the analog signal can extend to be equal to the VA+ and VA- supply voltages. In the event the signal exceeds these supply voltages the input current should be limited to ± 10 mA as the analog input of the chip is internally diode clamped to both supplies. Excess current into the pin can damage the device. On the evaluation board, resistor R16 (see Figure 6) does provide some current limiting in the event of an overrange signal which exceeds the supply voltage.

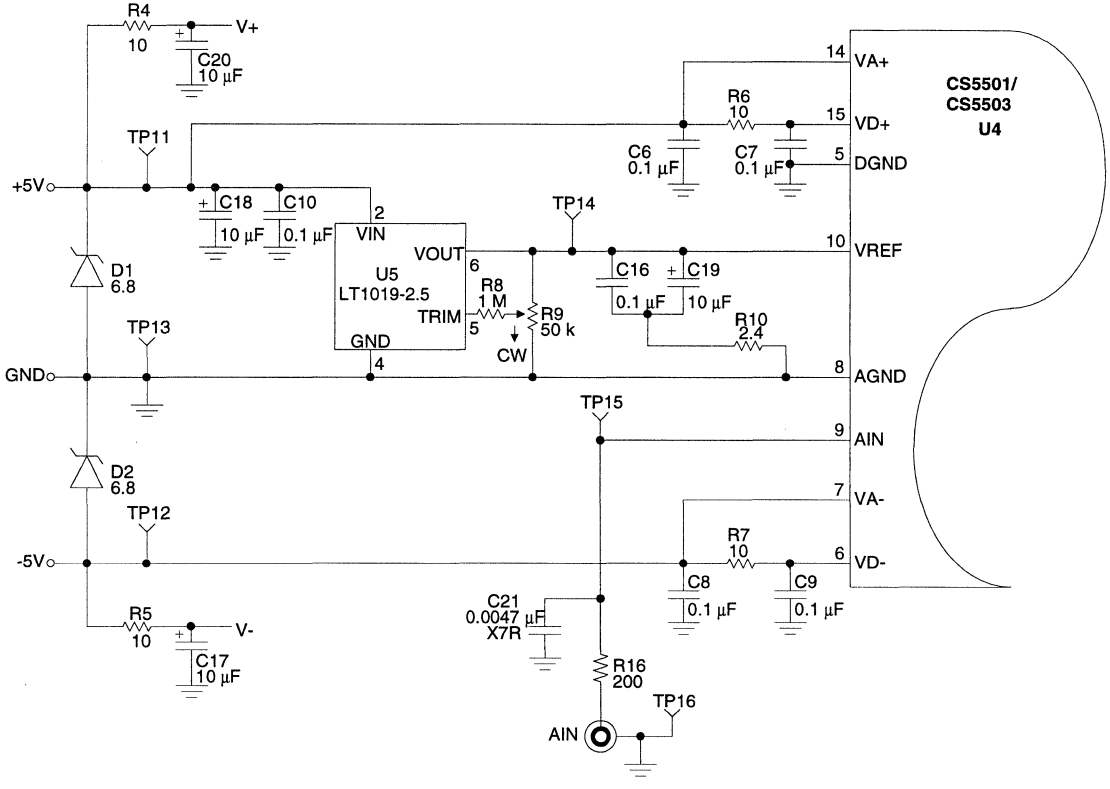


Figure 6. Voltage Reference / Analog Input

Oscilloscope Monitoring of SDATA

The output data from either the CS5501 or the CS5503 can be observed on a dual trace oscilloscope with the following hook-up. Set the evaluation board to operate in the SSC mode. Connect scope probes to TP9 (SCLK) and TP10 (SDATA). Use a third probe connected to TP8 ($\overline{\text{DRDY}}$) to provide the external trigger input to the scope (use falling edge of $\overline{\text{DRDY}}$ to trigger). With proper horizontal sweep, the SDATA output bits from the A/D converter can be observed. Note that if the input voltage to the CS5501 is adjusted to a mid-code value, the converter will remain stable on the same output code. This illustrates the low noise level of the CS5501. The CS5503 will exhibit a few LSB's of noise in its observed output in agreement with its noise specifications.

Evaluation Board Component Layout and Design Considerations

Figure 7 is a reproduction of the silkscreen component placement of the PC board.

The evaluation board includes design features to insure proper performance from the A/D converter chip. Separate analog and digital ground planes have been used on the board to insure good noise immunity to digital system noise.

Decoupling networks (R6, C7, and R7, C9 in Figure 6) have been used to eliminate the possibility of noise on the power supplies on the digital section from affecting the analog part of the A/D converter chip.

The RC network (R10, C16 and C19) on the output of the LT1019-2.5 reference may not be needed in all applications. It has been included to insure the best noise performance from the reference .

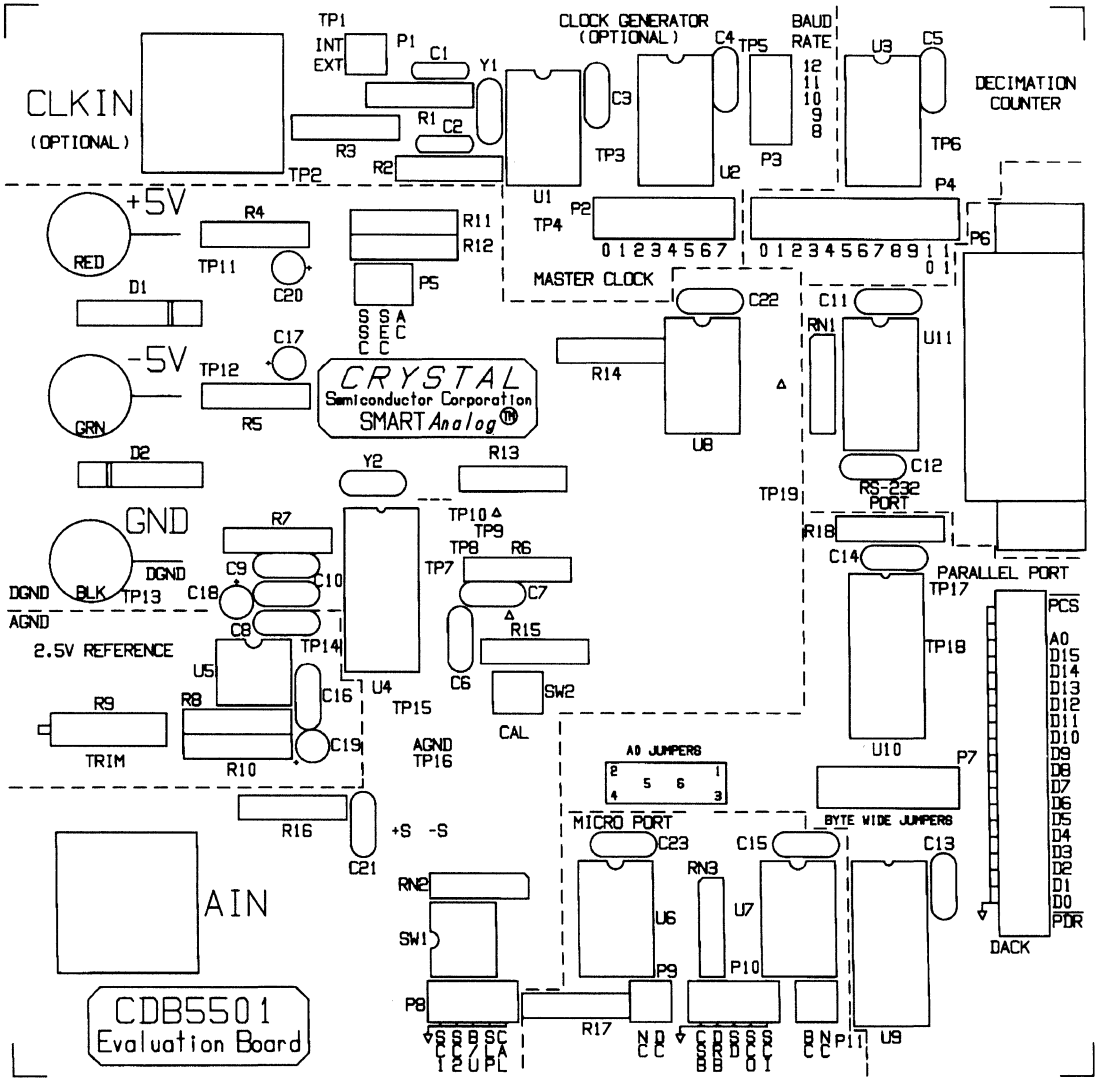


Figure 7. CDB5501/CDB5503 Component Layout

• Notes •

Semiconductor Corporation

CS5504

Low Power, 20-Bit A/D Converter

Features

- Delta-Sigma A/D Converter
  - 20-bit No Missing Codes
  - Linearity Error: ±0.0007%FS
- 2 Differential Inputs
  - Pin Selectable Unipolar/Bipolar Ranges
  - Common Mode Rejection
    - 105 dB @ dc
    - 120 dB @ 50, 60 Hz
- Either 5V or 3.3V Digital Interface
- On-chip Self-Calibration Circuitry
- Output Update Rates up to 200/second
- Low Power Consumption: 4.4 mW

General Description

The CS5504 is a 2-channel, fully differential 20-bit, serial-output CMOS A/D converter. The CS5504 uses charge-balanced (delta-sigma) techniques to provide a low cost, high resolution measurement at output word rates up to 200 samples per second.

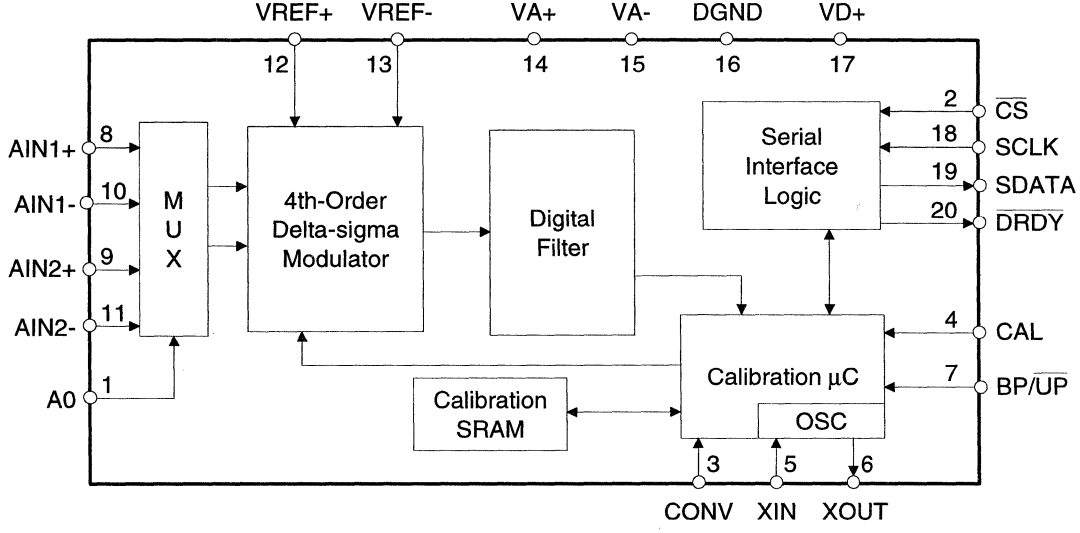
The on-chip digital filter offers superior line rejection at 50Hz and 60Hz when the device is operated from a 32.768 kHz clock (output word rate = 20 Hz.).

The CS5504 has on-chip self-calibration circuitry which can be initiated at any time or temperature to ensure minimum offset and full-scale errors.

Low power, high resolution and small package size make the CS5504 an ideal solution for loop-powered transmitters, panel meters, weigh scales and battery-powered instruments.

ORDERING INFORMATION:

CS5504-BP	-40°C to +85°C	20-pin PDIP
CS5504-BS	-40°C to +85°C	20-pin SOIC



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

ANALOG CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+ = 5V ± 10%; VA- = -5V ± 10%; VD+ = 3.3V ± 5%; VREF+ = 2.5V, VREF- = 0V; f_{CLK} = 32.768kHz; Bipolar Mode; R_{source} = 1kΩ with a 10nF to GND at AIN.) (Notes 1, 2)

Parameter*			Min	Typ	Max	Units
Specified Temperature Range				-40 to +85		°C
Accuracy						
Linearity Error			-	0.0007	0.0015	±%FS
Differential Nonlinearity		(No Missing Codes)	20	-	-	Bits
Full Scale Error		(Note 3)	-	±4	±32	LSB
Full Scale Drift		(Note 4)	-	±8	-	LSB
Unipolar Offset		(Note 3)	-	±8	±32	LSB
Unipolar Offset Drift		(Note 4)	-	±8	-	LSB
Bipolar Offset		(Note 3)	-	±4	±16	LSB
Bipolar Offset Drift		(Note 4)	-	±4	-	LSB
Noise (Referred to Output)			-	2.6	-	LSB_{rms}
Analog Input						
Analog Input Range:	Unipolar Bipolar	(Note 5)	- -	0 to +2.5 ±2.5	- -	V V
Common Mode Rejection:	dc 50, 60- Hz	(Note 2)	- 120	105 -	- -	dB dB
Off Channel Isolation			-	120	-	dB
Input Capacitance			-	15	-	pF
DC Bias Current		(Note 1)	-	5	-	nA
Power Supplies						
DC Power Supply Currents:	I_{Total} I_{Analog} $I_{Digital}$		- - -	465 425 40	600 - -	µA µA µA
Power Dissipation		(Note 6)	-	4.4	6.0	mW
Power Supply Rejection			-	80	-	dB

Notes:
1. Both source resistance and shunt capacitance are critical in determining the CS5504's source impedance requirements. Refer to the text section *Analog Input Impedance Considerations.*
2. Specifications guaranteed by design, characterization and/or test.
3. Applies after calibration at the temperature of interest.
4. Total drift over the specified temperature range since calibration at power-up at 25 °C
5. Common mode voltage may be at any value as long as AIN+ and AIN- remain within the VA+ and VA- supply voltages.
6. All outputs unloaded. All inputs CMOS levels.

* Refer to the Specification Definitions immediately following the Pin Description Section.

Specifications are subject to change without notice.

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Units
Modulator Sampling Frequency	f_s	$f_{clk}/2$	Hz
Output Update Rate (CONV = 1)	f_{out}	$f_{clk}/1622$	Hz
Filter Corner Frequency	f_{-3dB}	$f_{clk}/1928$	Hz
Settling Time to 1/2 LSB (FS Step)	t_s	$1/f_{out}$	s

5V DIGITAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+ = 5V ± 10%; VA- = -5V ± 10%; DGND = 0.) (Notes 2, 7)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage:	XIN	V_{IH}	3.5	-	-	V
	All Pins Except XIN	V_{IH}	2.0	-	-	V
Low-Level Input Voltage:	XIN	V_{IL}	-	-	1.5	V
	All Pins Except XIN	V_{IL}	-	-	0.8	V
High-Level Output Voltage	(Note 8)	V_{OH}	(VD+)-1.0	-	-	V
Low-Level Output Voltage	I_{out} = 1.6 mA	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	±1	±10	µA
3-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

Notes: 7. All measurements are performed under static conditions.
8. I_{out} = -100 µA. This guarantees the ability to drive one TTL load. (V_{OH} = 2.4V @ I_{out} = -40 µA).

3.3V DIGITAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+ = 5V ± 10%; VD+ = 3.3V ± 5%; VA- = -5V ±10%; GND = 0V.) (Notes 2, 7)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage:	XIN	V_{IH}	0.7VD+	-	-	V
	All Pins Except XIN	V_{IH}	0.6VD+	-	-	V
Low-Level Input Voltage:	XIN	V_{IL}	-	-	0.3VD+	V
	All Pins Except XIN	V_{IL}	-	-	0.16VD+	V
High-Level Output Voltage	I_{out} = -400 µA	V_{OH}	(VD+)-0.3	-	-	V
Low-Level Output Voltage	I_{out} = 400 µA	V_{OL}	-	-	0.3	V
Input Leakage Current		I_{in}	-	±1	±10	µA
3-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

5V SWITCHING CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+ = 5V ± 10%; VA- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF.) (Note 2)

Parameter		Symbol	Min	Typ	Max	Units
Master Clock Frequency	Internal Oscillator External Clock	XIN f_{clk}	30.0 30	32.768 -	53.0 330	kHz kHz
Master Clock Duty Cycle			40	-	60	%
Rise Times:	Any Digital Input (Note 9) Any Digital Output	t_{rise}	- -	- 50	1.0 -	µs ns
Fall Times:	Any Digital Input (Note 9) Any Digital Output	t_{fall}	- -	- 20	1.0 -	µs ns
Start-Up						
Power-On Reset Period	(Note 10)	t_{res}	-	10	-	ms
Oscillator Start-up Time	XTAL = 32.768 kHz (Note 11)	t_{osu}	-	500	-	ms
Wake-up Period	(Note 12)	t_{wup}	-	$1800/f_{clk}$	-	s
Calibration						
CONV Pulse Width (CAL=1)	(Note 13)	t_{ccw}	100	-	-	ns
CONV and CAL High to Start of Calibration		t_{scl}	-	-	$2/f_{clk}+200$	ns
Start of Calibration to End of Calibration		t_{cal}	-	$3246/f_{clk}$	-	s
Conversion						
Set Up Time	A0 to CONV High	t_{sac}	50	-	-	ns
Hold Time	A0 after CONV High	t_{hca}	100	-	-	ns
CONV Pulse Width		t_{cpw}	100	-	-	ns
CONV High to Start of Conversion		t_{scn}	-	-	$2/f_{clk}+200$	ns
Set Up Time	BP/$\overline{UP}$ stable prior to $\overline{DRDY}$ falling	t_{bus}	$82/f_{clk}$	-	-	s
Hold Time	BP/$\overline{UP}$ stable after $\overline{DRDY}$ falls	t_{buh}	0	-	-	ns
Start of Conversion to End of Conversion	(Note 14)	t_{con}	-	$1624/f_{clk}$	-	s

Notes:
9. Specified using 10% and 90% points on waveform of interest.
10. An internal power-on-reset is activated whenever power is applied to the device.
11. Oscillator start-up time varies with the crystal parameters. This specification does not apply when using an external clock source.
12. The wake-up period begins once the oscillator starts; or when using an external f_{clk}, after the power-on reset time elapses.
13. Calibration can also be initiated by pulsing CAL high while CONV=1.
14. Conversion time will be $1622/f_{clk}$ if CONV remains high continuously.

3.3V SWITCHING CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+ = 5V ± 10%; VD+ = 3.3V ± 5%; VA- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF.) (Note 2)

Parameter		Symbol	Min	Typ	Max	Units
Master Clock Frequency	Internal Oscillator External Clock	XIN f_{clk}	30.0 30	32.768 -	53.0 330	kHz kHz
Master Clock Duty Cycle			40	-	60	%
Rise Times:	Any Digital Input (Note 9) Any Digital Output	t_{rise}	- -	- 50	1.0 -	µs ns
Fall Times:	Any Digital Input (Note 9) Any Digital Output	t_{fall}	- -	- 20	1.0 -	µs ns
Start-Up						
Power-On Reset Period	(Note 10)	t_{res}	-	10	-	ms
Oscillator Start-up Time	XTAL = 32.768 kHz (Note 11)	t_{osu}	-	500	-	ms
Wake-up Period	(Note 12)	t_{wup}	-	$1800/f_{clk}$	-	s
Calibration						
CONV Pulse Width (CAL=1)	(Note 13)	t_{ccw}	100	-	-	ns
CONV and CAL High to Start of Calibration		t_{scl}	-	-	$2/f_{clk}+200$	ns
Start of Calibration to End of Calibration		t_{cal}	-	$3246/f_{clk}$	-	s
Conversion						
Set Up Time	A0 to CONV High	t_{sac}	50	-	-	ns
Hold Time	A0 after CONV High	t_{hca}	100	-	-	ns
CONV Pulse Widh		t_{cpw}	100	-	-	ns
CONV High to Start of Conversion		t_{scn}	-	-	$2/f_{clk}+200$	ns
Set Up Time	BP/$\overline{UP}$ stable prior to $\overline{DRDY}$ falling	t_{bus}	$82/f_{clk}$	-	-	s
Hold Time	BP/$\overline{UP}$ stable after $\overline{DRDY}$ falls	t_{buh}	0	-	-	ns
Start of Conversion to End of Conversion	(Note 14)	t_{con}	-	$1624/f_{clk}$	-	s

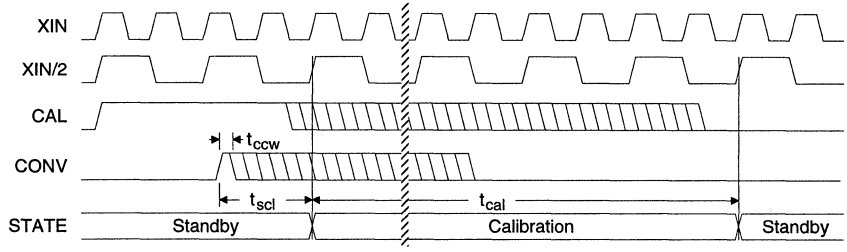


Figure 1. Calibration Timing (Not to Scale)

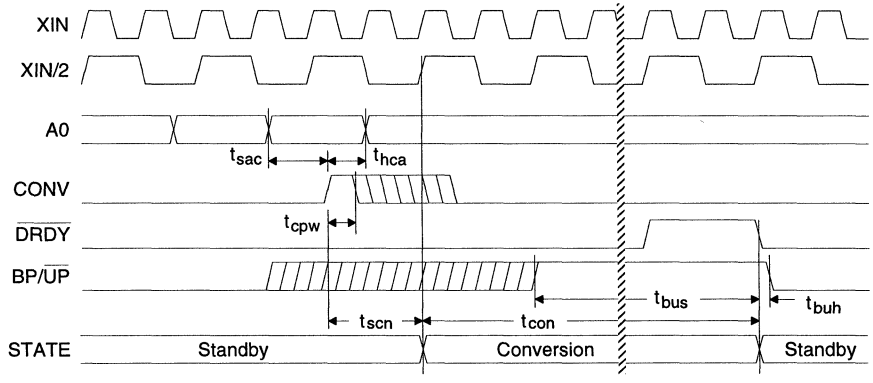


Figure 2. Conversion Timing (Not to Scale)

5V SWITCHING CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+ = 5V ± 10%; VA- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF.) (Note 2)

Parameter		Symbol	Min	Typ	Max	Units
Serial Clock		f_{sclk}	0	-	2.5	MHz
Serial Clock	Pulse Width High Pulse Width Low	t_{ph} t_{pl}	200 200	- -	- -	ns ns
Access Time:	$\overline{CS}$ Low to data valid (Note 15)	t_{csd}	-	60	200	ns
Maximum Delay Time:	(Note 16) SCLK falling to new SDATA bit	t_{dd}	-	150	310	ns
Output Float Delay:	$\overline{CS}$ high to output Hi-Z (Note 17) SCLK falling to Hi-Z	t_{fd1} t_{fd2}	- -	60 160	150 300	ns ns

Notes: 15. If $\overline{CS}$ is activated asynchronously to $\overline{DRDY}$, $\overline{CS}$ will not be recognized if it occurs when $\overline{DRDY}$ is high for 2 clock cycles. The propagation delay time may be as great as 2 f_{clk} cycles plus 200 ns. To guarantee proper clocking of SDATA when using asynchronous $\overline{CS}$, SCLK should not be taken high sooner than $2/f_{clk}$ + 200 ns after $\overline{CS}$ goes low.

16. SDATA transitions on the falling edge of SCLK. Note that a rising SCLK must occur to enable the serial port shifting mechanism before falling edges can be recognized.

17. If $\overline{CS}$ is returned high before all data bits are output, the SDATA output will complete the current data bit and then go to high impedance.

3.3V SWITCHING CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+ = 5V ± 10%; VD+ = 3.3V ± 5%; VA- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF.) (Note 2)

Parameter		Symbol	Min	Typ	Max	Units
Serial Clock		f_{sclk}	0	-	1.25	MHz
Serial Clock	Pulse Width High Pulse Width Low	t_{ph} t_{pl}	200 200	- -	- -	ns ns
Access Time:	$\overline{CS}$ Low to data valid (Note 15)	t_{csd}	-	100	200	ns
Maximum Delay Time:	(Note 16) SCLK falling to new SDATA bit	t_{dd}	-	400	600	ns
Output Float Delay:	$\overline{CS}$ high to output Hi-Z (Note 17) SCLK falling to Hi-Z	t_{fd1} t_{fd2}	- -	70 320	150 500	ns ns

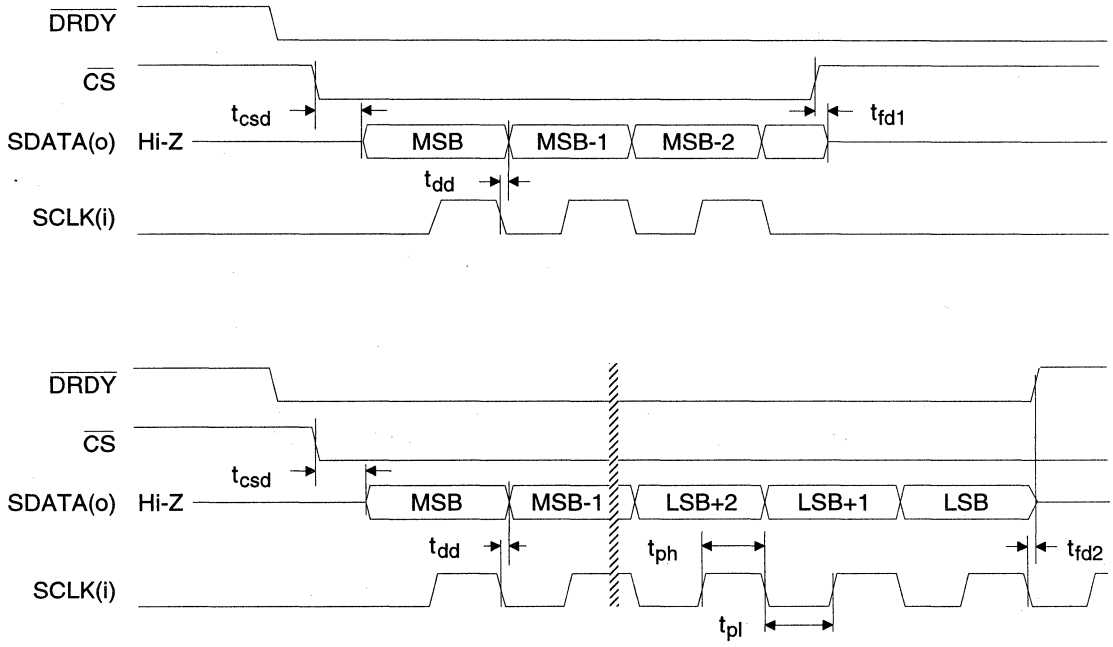


Figure 3. Timing Relationships; Serial Data Read (Not to Scale)

RECOMMENDED OPERATING CONDITIONS (DGND = 0V) (Note 18)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies:					
Positive Digital	VD+	3.15	5.0	5.5	V
(VA+) - (VA-)	V_{diff}	4.5	10	11	V
Positive Analog	VA+	4.5	5.0	11	V
Negative Analog	VA-	0	-5.0	-5.5	V
Analog Reference Voltage (Note 19)	(VREF+)-(VREF-)	1.0	2.5	3.6	V
Analog Input Voltage: (Note 20)					
Unipolar	VAIN	0	-	(VREF+)-(VREF-)	V
Bipolar	VAIN	-((VREF+)-(VREF-))	-	(VREF+)-(VREF-)	V

Notes: 18. All voltages with respect to ground.

19. The CS5504 can be operated with a reference voltage as low as 100 mV; but with a corresponding reduction in noise-free resolution. The common mode voltage of the voltage reference may be any value as long as +VREF and -VREF remain inside the supply values of VA+ and VA-.

20. The CS5504 can accept input voltages up to the analog supplies (VA+ and VA-). In unipolar mode the CS5504 will output all 1's if the dc input magnitude ((AIN+)-(AIN-)) exceeds ((VREF+)-(VREF-)) and will output all 0's if the input becomes more negative than 0 Volts. In bipolar mode the CS5504 will output all 1's if the dc input magnitude ((AIN+)-(AIN-)) exceeds ((VREF+)-(VREF-)) and will output all 0's if the input becomes more negative in magnitude than -((VREF+)-(VREF-)).

ABSOLUTE MAXIMUM RATINGS*

Parameter			Symbol	Min	Typ	Max	Units
DC Power Supplies:	Digital Ground	(Note 21)	DGND	-0.3	-	(VD+)-0.3	V
	Positive Digital	(Note 22)	VD+	-0.3	-	6.0 or VA+	V
	Positive Analog		VA+	-0.3	-	12	V
	Negative Analog		VA-	+0.3	-	-6.0	V
Input Current, Any Pin Except Supplies		(Notes 23, 24)	I_{in}	-	-	±10	mA
Output Current			I_{out}	-	-	±25	mA
Power Dissipation (Total)		(Note 25)		-	-	500	mW
Analog Input Voltage	AIN and VREF pins		V_{INA}	(VA-)-0.3	-	(VA+)+0.3	V
Digital Input Voltage			V_{IND}	-0.3	-	(VD+)+0.3	V
Ambient Operating Temperature			T_A	-40	-	85	°C
Storage Temperature			T_{stg}	-65	-	150	°C

Notes: 21. No pin should go more positive than (VA+)+0.3V.

22. VD+ must always be less than (VA+) +0.3V, and can never exceed +6.0 V.

23. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pin.

24. Transient currents of up to 100mA will not cause SCR latch-up. Maximum input current for a power supply pin is ± 50 mA.

25. Total power dissipation, including all input currents and output currents.

* WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

GENERAL DESCRIPTION

The CS5504 is a low power, 20-bit, monolithic CMOS A/D converter designed specifically for measurement of dc signals. The CS5504 includes a delta-sigma charge-balance converter, a voltage reference, a calibration micro controller with SRAM, a digital filter and a serial interface.

The CS5504 is optimized to operate from a 32.768 kHz crystal but can be driven by an external clock whose frequency is between 30 kHz and 330 kHz. When the digital filter is operated with a 32.768 kHz clock, the filter has zeros precisely at 50 and 60 Hz line frequencies and multiples thereof.

The CS5504 uses a "start convert" command to latch the input channel selection and to start a convolution cycle on the digital filter. Once the filter cycle is completed, the output port is updated. When operated with a 32.768 kHz clock the ADC converts and updates its output port at 20 samples/sec. The output port operates in a synchronous externally-clocked interface format.

THEORY OF OPERATION

Basic Converter Operation

The CS5504 A/D converter has three operating states. These are stand-by, calibration, and conversion. When power is first applied, an internal power-on reset delay of about 10 ms resets all of the logic in the device. The oscillator must then begin oscillating before the device can be considered functional. After the power-on reset is applied, the device enters the wake-up period for 1800 clock cycles after clock is present. This allows the delta-sigma modulator and other circuitry (which are operating with very low currents) to reach a stable bias condition prior to entering into either the calibration or conversion states. During the 1800 cycle wake-up period, the device can accept an input command. Execution of this command will not occur until the complete wake-up period elapses. If no command is given, the device enters the standby state.

Calibration

After the initial application of power, the CS5504 must enter the calibration state prior to performing accurate conversions. During calibration, the chip executes a two-step process. The device first performs an offset calibration and then follows this with a gain calibration. The two calibration steps determine the zero reference point and the full scale reference point of the converter's transfer function. From these points it calibrates the zero point and a gain slope to be used to properly scale the output digital codes when doing conversions.

The calibration state is entered whenever the CAL and CONV pins are high at the same time. The state of the CAL and CONV pins at power-on are recognized as commands, but will not be executed until the end of the 1800 clock cycle wake-up period.

If CAL and CONV become active (high) during the 1800 clock cycle wake-up time, the converter will wait until the wake-up period elapses before executing the calibration. If the wake-up time has elapsed, the converter will be in the standby mode waiting for instruction and will enter the calibration cycle immediately if CAL and CONV become active. The calibration lasts for 3246 clock cycles. Calibration coefficients are then retained in the SRAM (static RAM) for use during conversion.

The states of A0 and BP/$\overline{\text{UP}}$ are ignored during calibration but should remain stable throughout the calibration period to minimize noise.

When conversions are performed in unipolar mode or in bipolar mode, the converter uses the same calibration factors to compute the digital

output code. The only difference is that in bipolar mode the on-chip microcontroller offsets the computed output word by a code value of 8000H. This means that the bipolar measurement range is not calibrated from full scale positive to full scale negative. Instead it is calibrated from the bipolar zero scale point to full scale positive. The slope factor is then extended below bipolar zero to accommodate the negative input signals. The converter can be used to convert both unipolar and bipolar signals by changing the BP/$\overline{UP}$ pin. Recalibration is not required when switching between unipolar and bipolar modes.

At the end of the calibration cycle, the on-chip micro controller checks the logic state of the CONV signal. If the CONV input is low the device will enter the standby mode where it waits for further instruction. If the CONV signal is high at the end of the calibration cycle, the converter will enter the conversion state and perform a conversion on the input channel. The CAL signal can be returned low any time after calibration is initiated. CONV can also be returned low, but it should never be taken low and then taken back high until the calibration period has ended and the converter is in the standby state. If CONV is taken low and then high again with CAL high while the converter is calibrating, the device will interrupt the current calibration cycle and start a new one. If CAL is taken low and CONV is taken low and then high during calibration, the calibration cycle will continue as the conversion command is disregarded. The state of BP/$\overline{UP}$ is not important during calibrations.

If an "end of calibration" signal is desired, pulse the CAL signal high while leaving the CONV signal high continuously. Once the calibration is completed, a conversion will be performed. At the end of the conversion, $\overline{DRDY}$ will fall to indicate the first valid conversion after the calibration has been completed.

Conversion

The conversion state can be entered at the end of the calibration cycle, or whenever the converter is idle in the standby mode. If CONV is taken high to initiate a calibration cycle (CAL also high), and remains high until the calibration cycle is completed (CAL is taken low after CONV transitions high), the converter will begin a conversion upon completion of the calibration period. The device will perform a conversion on the input channel selected by A0 when CONV transitions high. Table 1 indicates the multiplexer channel selection truth table.

A0	Channel Addressed
0	AIN1
1	AIN2

Table 1. Multiplexer Truth Table

The A0 input is latched internal to the CS5504 when CONV rises. A0 has internal pull-down circuits which default the multiplexer to channel AIN1.

The BP/$\overline{UP}$ pin is not a latched input. The BP/$\overline{UP}$ pin controls how the output word from the digital filter is processed. In bipolar mode the output word computed by the digital filter is offset by 80000H (see Understanding Converter Calibration). BP/$\overline{UP}$ can be changed after a conversion is started as long as it is stable for 82 clock cycles of the conversion period prior to $\overline{DRDY}$ falling. If one wishes to intermix measurement of bipolar and unipolar signals on various input channels, it is best to switch the BP/$\overline{UP}$ pin immediately after $\overline{DRDY}$ falls and leave BP/$\overline{UP}$ stable until $\overline{DRDY}$ falls again.

The digital filter in the CS5504 has a Finite Impulse Response and is designed to settle to full accuracy in one conversion time.

If CONV is left high, the CS5504 will perform continuous conversions. The conversion time will be 1622 clock cycles. If conversion is initiated

from the standby state, there may be up to two XIN clock cycles of uncertainty as to when conversion actually begins. This is because the internal logic operates at one half the external clock rate and the exact phase of the internal clock may be 180° out of phase relative to the XIN clock. When a new conversion is initiated from the standby state, it will take up to two XIN clock cycles to begin. Actual conversion will use 1624 clock cycles before $\overline{DRDY}$ goes low to indicate that the serial port has been updated. See the Serial Interface Logic section of the data sheet for information on reading data from the serial port.

In the event the A/D conversion command (CONV going positive) is issued during the conversion state, the current conversion will be terminated and a new conversion will be initiated.

Voltage Reference

The CS5504 uses a differential voltage reference input. The positive input is VREF+ and the negative input is VREF-. The voltage between VREF+ and VREF- can range from 1 volt minimum to 3.6 volts maximum. The gain slope will track changes in the reference without recalibration, accommodating ratiometric applications.

Analog Input Range

The analog input range is set by the magnitude of the voltage between the VREF+ and VREF- pins. In unipolar mode the input range will equal the magnitude of the voltage reference. In bipolar mode the input voltage range will equate to plus and minus the magnitude of the voltage reference. While the voltage reference can be as great as 3.6 volts, its common mode voltage can be any value as long as the reference inputs VREF+ and VREF- stay within the supply voltages for the A/D. The differential input voltage can also have any common mode value as long as the maximum signal magnitude stays within the supply voltages.

The A/D converter is intended to measure dc or low frequency inputs. It is designed to yield accurate conversions even with noise exceeding the input voltage range as long as the spectral components of this noise will be filtered out by the digital filter. For example, with a 3.0 volt reference in unipolar mode, the converter will accurately convert an input dc signal up to 3.0 volts with up to 15% overrange for 60 Hz noise. A 3.0 volt dc signal could have a 60 Hz component which is 0.5 volts above the maximum input of 3.0 (3.5 volts peak; 3.0 volts dc plus 0.5 volts peak noise) and still accurately convert the input signal (XIN = 32.768 kHz). This assumes that the signal plus noise amplitude stays within the supply voltages.

The CS5504 converters output data in binary format when converting unipolar signals and in offset binary format when converting bipolar signals. Table 2 outlines the output coding for both unipolar and bipolar measurement modes.

Unipolar Input Voltage	Output Codes	**Bipolar Input Voltage**
>(VREF - 1.5 LSB)	**FFFFF**	>(VREF - 1.5 LSB)
VREF - 1.5 LSB	**FFFFF** ——— **FFFFE**	VREF - 1.5 LSB
VREF/2 - 0.5 LSB	**80000** ——— **7FFFF**	-0.5 LSB
+ 0.5 LSB	**00001** ——— **00000**	-VREF + 0.5 LSB
<(+ 0.5 LSB)	**00000**	<(VREF + 0.5 LSB)

Note: Table excludes common mode voltage on the signal and reference inputs.

Table 2. Output Coding

Converter Performance

The CS5504 A/D converter has excellent linearity performance. Calibration minimizes the errors in offset and gain. The CS5504 device has no missing code performance to 20-bits. The converter achieves Common Mode Rejection (CMR) at dc of 105 dB typical, and CMR at 50 and 60 Hz of 120 dB typical.

The CS5504 can experience some drift as temperature changes. The CS5504 uses chopper-stabilized techniques to minimize drift. Measurement errors due to offset or gain drift can be eliminated at any time by recalibrating the converter.

Analog Input Impedance Considerations

The analog input of the CS5504 can be modeled as illustrated in Figure 4 (the model ignores the multiplexer switch resistance). Capacitors (15 pF each) are used to dynamically sample each of the inputs (AIN+ and AIN-). Every half XIN cycle the switch alternately connects the capacitor to the output of the buffer and then directly to the AIN pin. Whenever the sample capacitor is switched from the output of the buffer to the AIN pin, a small packet of charge (a dynamic demand of current) is required from the input source to settle the voltage of the sample capacitor to its final value. The voltage on the output of the buffer may differ up to 100 mV from the actual input voltage due to the offset voltage of the buffer. Timing allows one half of a XIN clock cycle for the voltage on the sample capacitor to settle to its final value.

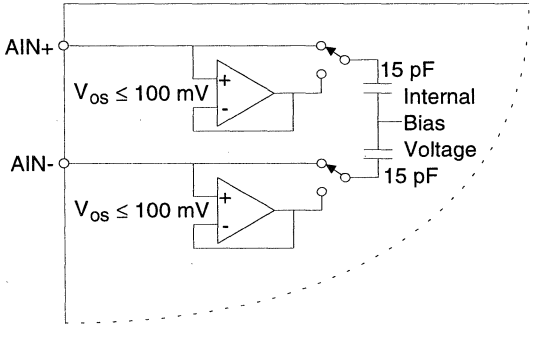


Figure 4. Analog Input Model

An equation for the maximum acceptable source resistance is derived.

$$Rs_{max} = \frac{-1}{2XIN\,(15pF + C_{EXT})\,\ln\left[\dfrac{V_e}{V_e + \dfrac{15pF(100mv)}{(15pF + C_{EXT})}}\right]}$$

This equation assumes that the offset voltage of the buffer is 100 mV, which is the worst case. The value of Ve is the maximum error voltage which is acceptable. C_{EXT} is the combination of any external or stray capacitance.

For a maximum error voltage (Ve) of 600 nV in the CS5504 (1/4LSB at 20-bits), the above equation indicates that when operating from a 32.768 kHz XIN, source resistances up to 84 kΩ in the CS5504 are acceptable in the absence of external capacitance (C_{EXT} = 0).

The VREF+ and VREF- inputs have nearly the same structure as the AIN+ and AIN- inputs. Therefore, the discussion on analog input impedance applies to the voltage reference inputs as well.

Digital Filter Characteristics

The digital filter in the CS5504 is the combination of a comb filter and a low pass filter. The comb filter has zeros in its transfer function which are optimally placed to reject line interference frequencies (50 and 60 Hz and their multiples) when the CS5504 is clocked at

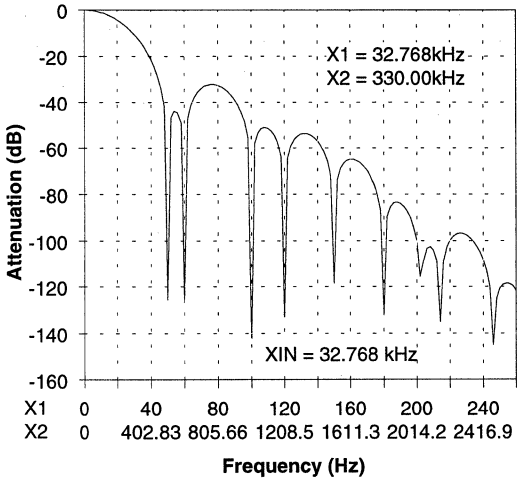


Figure 5. Filter Magnitude Plot to 260 Hz

Frequency (Hz)	Notch Depth (dB)	Frequency (Hz)	Minimum Attenuation (dB)
50	125.6	50±1%	55.5
60	126.7	60±1%	58.4
100	145.7	100±1%	62.2
120	136.0	120±1%	68.4
150	118.4	150±1%	74.9
180	132.9	180±1%	87.9
200	102.5	200±1%	94.0
240	108.4	240±1%	104.4

Table 3. Filter Notch Attenuation (XIN = 32.768 kHz)

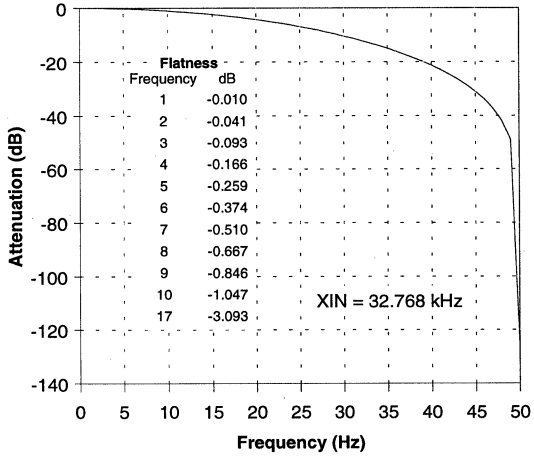


Figure 6. Filter Magnitude Plot to 50 Hz

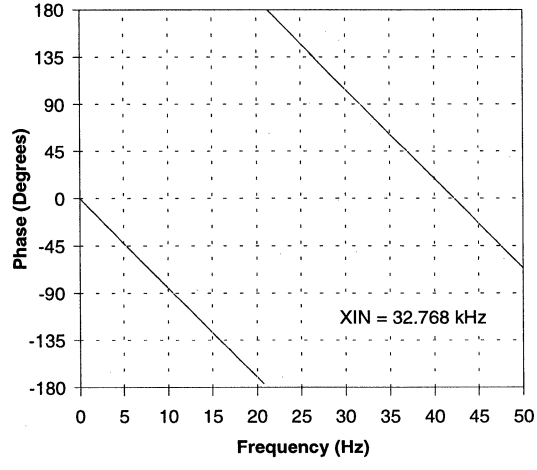


Figure 7. Filter Phase Plot to 50 Hz

32.768 kHz. Figures 5, 6 and 7 illustrate the magnitude and phase characteristics of the filter. Figure 5 illustrates the filter attenuation from dc to 260 Hz. At exactly 50, 60, 100, and 120 Hz the filter provides over 120 dB of rejection. Table 3 indicates the filter attenuation for each of the potential line interference frequencies when the converter is operating with a 32.768 kHz clock. The converter yields excellent attenuation of these interference frequencies even if the fundamental line frequency should vary ± 1% from its specified frequency. The -3dB corner frequency of the filter when operating from a 32.768 kHz clock is 17 Hz. Figure 7 illustrates that the phase characteristics of the filter are precisely linear phase.

If the CS5504 is operated at a clock rate other than 32.768 kHz, the filter characteristics, including the comb filter zeros, will scale with the operating clock frequency. Therefore, optimum rejection of line frequency interference will occur with the CS5504 running at 32.768 kHz.

Anti-Alias Considerations for Spectral Measurement Applications

Input frequencies greater than one half the output word rate (CONV = 1) may be aliased by the converter. To prevent this, input signals should be limited in frequency to no greater than one half the output word rate of the converter (when CONV =1). Frequencies close to the modulator sample rate (XIN/2) and multiples thereof may also be aliased. If the signal source includes spectral components above one half the output word rate (when CONV = 1) these components should be removed by means of low-pass filtering prior to the A/D input to prevent aliasing. Spectral components greater than one half the output word rate on the VREF inputs (VREF+ and VREF-) may also be aliased. Filtering of the reference voltage to remove these spectral components from the reference voltage is desirable.

Crystal Oscillator

The CS5504 is designed to be operated using a 32.768 kHz "tuning fork" type crystal. One end of the crystal should be connected to the XIN input. The other end should be attached to XOUT. Short lead lengths should be used to minimize stray capacitance.

Over the industrial temperature range (-40 to +85 °C) the on-chip gate oscillator will oscillate with other crystals in the range of 30 kHz to 53 kHz. The chip will operate with external clock frequencies from 30 kHz to 330 kHz over the industrial temperature range. The 32.768 kHz crystal is normally specified as a time-keeping crystal with tight specifications for both initial frequency and for drift over temperature. To maintain excellent frequency stability, these crystals are specified only over limited operating temperature ranges (i.e. -10 °C to +60 °C) by the manufacturers. Applications of these crystals with the CS5504 does not require tight initial tolerance or low tempco drift. Therefore, a lower cost crystal with looser initial tolerance and tempco will generally be adequate for use with the CS5504. Also check with the manufacturer about wide temperature range application of their standard crystals. Generally, even those crystals specified for limited temperature range will operate over much larger ranges if frequency stability over temperature is not a requirement. The frequency stability can be as bad as ±3000 ppm over the operating temperature range and still be typically better than the line frequency (50 Hz or 60 Hz) stability over cycle-to-cycle during the course of a day.

Serial Interface Logic

The digital filter in the CS5504 takes 1624 clock cycles to compute an output word once a conversion begins. At the end of the conversion cycle, the filter will attempt to update the serial port. Two clock cycles prior to the update $\overline{DRDY}$ will go high. When $\overline{DRDY}$ goes high just prior to a port update it checks to see if the port is either empty or unselected ($\overline{CS}$ = 1). If the port is empty or unselected, the digital filter will update the port with a new output word. When new data is put into the port $\overline{DRDY}$ will go low.

Reading Serial Data

SDATA is the output pin for the serial data. When $\overline{CS}$ goes low after new data becomes available ($\overline{DRDY}$ goes low), the SDATA pin comes out of Hi-Z with the MSB data bit present. SCLK is the input pin for the serial clock. If the MSB data bit is on the SDATA pin, the first rising edge of SCLK enables the shifting mechanism. This allows the falling edges of

SCLK to shift subsequent data bits out of the port. Note that if the MSB data bit is output and the SCLK signal is high, the first falling edge of SCLK will be ignored because the shifting mechanism has not become activated. After the first rising edge of SCLK, each subsequent falling edge will shift out the serial data. Once the LSB is present, the falling edge of SCLK will cause the SDATA output to go to Hi-Z and $\overline{DRDY}$ to return high. The serial port register will be updated with a new data word upon the completion of another conversion if the serial port has been emptied, or if the $\overline{CS}$ is inactive (high).

$\overline{CS}$ can be operated asynchronously to the $\overline{DRDY}$ signal. The $\overline{DRDY}$ signal need not be monitored as long as the $\overline{CS}$ signal is taken low for at least two XIN clock cycles plus 200 ns prior to SCLK being toggled. This ensures that $\overline{CS}$ has gained control over the serial port.

Power Supplies and Grounding

The analog and digital supply pins to the CS5504 are brought out on separate pins to minimize noise coupling between the analog and digital sections of the chip. Note that there is no analog ground pin. No analog ground pin is required because the inputs for measurement and for the voltage reference are differential and require no ground. In the digital section of the chip the supply current flows into the VD+ pin and out of the DGND pin. As a CMOS device, the CS5504 requires that the supply voltage on the VA+ pin always be more positive than the voltage on any other pin of the device. If this requirement is not met, the device can latch-up or be damaged. In all circumstances the VA+ voltage must remain more positive than the VD+ or DGND pins; VD+ must remain more positive than the DGND pin.

The following power supply options are possible:

VA+ = +5V to +10V,	VA- = 0V,	VD+ = +5V
VA+ = +5V,	VA- = -5V,	VD+ = +5V
VA+ = +5V,	VA- = 0V to -5V,	VD+ = +3.3V

The CS5504 cannot be operated with a 3.3V digital supply if VA+ is greater than +5.5V.

Figure 8 illustrates the System Connection Diagram for the CS5504 using a single +5V supply. Note that all supply pins are bypassed with 0.1 µF capacitors and that the VD+ digital supply is derived from the VA+ supply.

Figure 9 illustrates the CS5504 using dual supplies of +5 and -5V.

Figure 10 illustrates the CS5504 using dual supplies of +10V analog and +5V digital.

When using separate supplies for VA+ and VD+, VA+ must be established first. VD+ should never become more positive than VA+ under any operating condition. Remember to investigate transient power-up conditions, when one power supply may have a faster rise time.

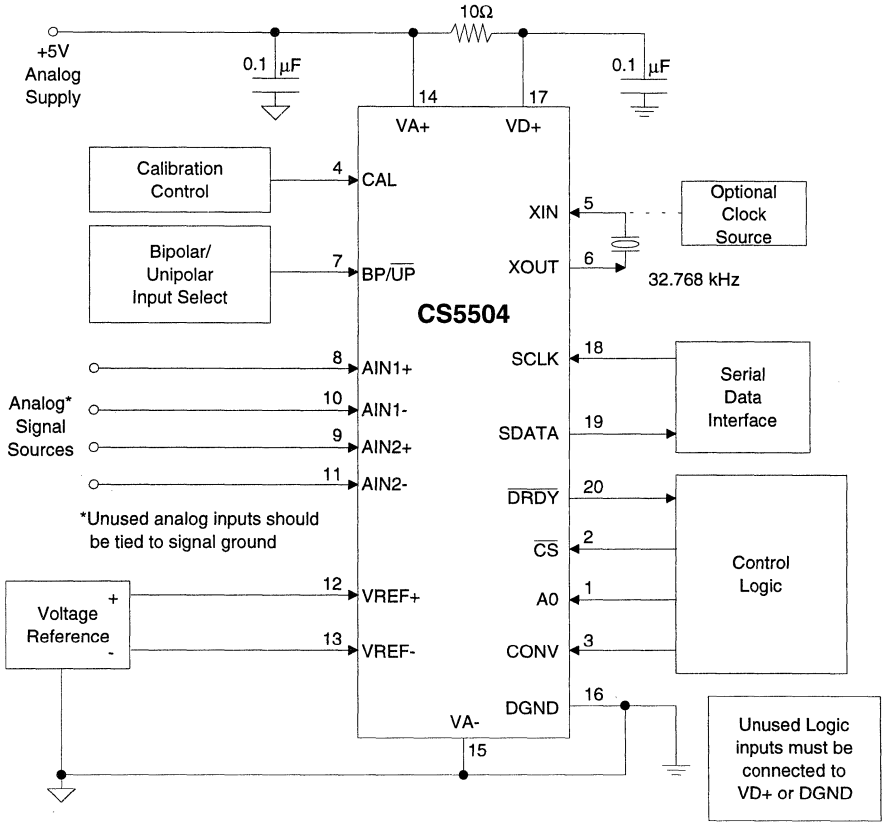


Figure 8. CS5504 System Connection Diagram Using Single Supply

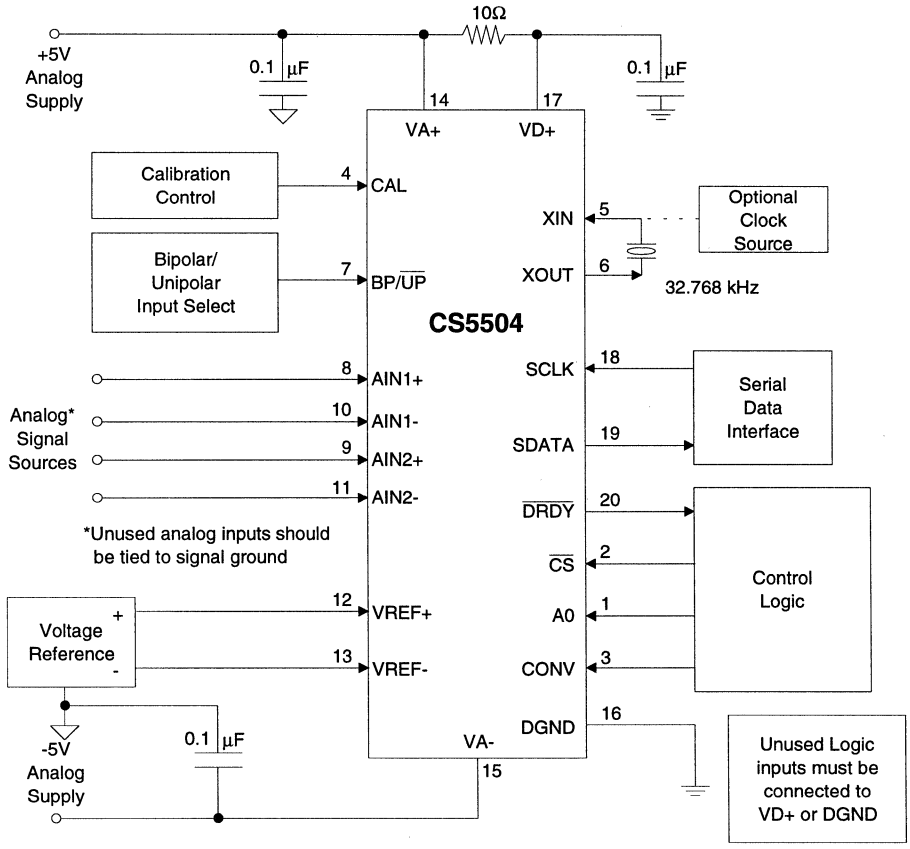


Figure 9. CS5504 System Connection Diagram Using Dual Supplies

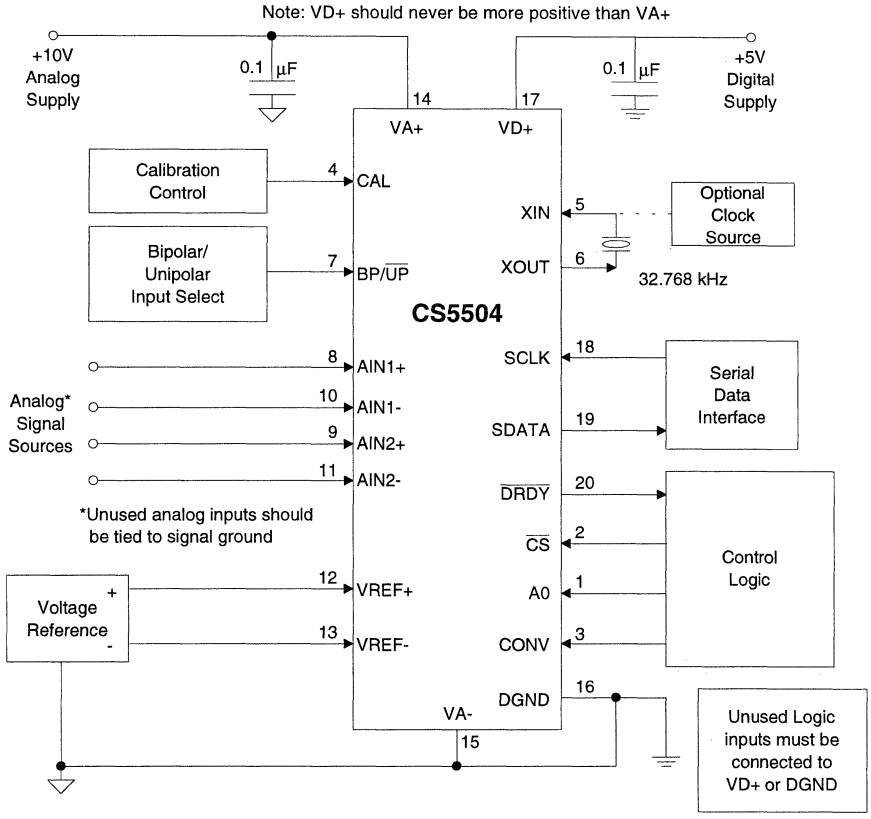


Figure 10. CS5504 System Connection Diagram Using Dual Supply, +10V Analog, +5V Digital

PIN DESCRIPTIONS*

MULTIPLEXER SELECTION INPUT	**A0**	1	20	**$\overline{\text{DRDY}}$**	DATA READY
CHIP SELECT	**$\overline{\text{CS}}$**	2	19	**SDATA**	SERIAL DATA OUTPUT
CONVERT	**CONV**	3	18	**SCLK**	SERIAL CLOCK INPUT
CALIBRATE	**CAL**	4	17	**VD+**	POSITIVE DIGITAL POWER
CRYSTAL IN	**XIN**	5	16	**DGND**	DIGITAL GROUND
CRYSTAL OUT	**XOUT**	6	15	**VA-**	NEGATIVE ANALOG POWER
BIPOLAR/UNIPOLAR	**BP/$\overline{\text{UP}}$**	7	14	**VA+**	POSITIVE ANALOG POWER
DIFFERENTIAL ANALOG INPUT	**AIN1+**	8	13	**VREF-**	VOLTAGE REFERENCE INPUT
DIFFERENTIAL ANALOG INPUT	**AIN2+**	9	12	**VREF+**	VOLTAGE REFERENCE INPUT
DIFFERENTIAL ANALOG INPUT	**AIN1-**	10	11	**AIN2-**	DIFFERENTIAL ANALOG INPUT

*Pinout applies to both PDIP and SOIC

Clock Generator

XIN; XOUT - Crystal In; Crystal Out, Pins 5, 6.

A gate inside the chip is connected to these pins and can be used with a crystal to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock can be supplied into the XIN pin to provide the master clock for the device. Loss of clock will put the device into a lower powered state (approximately 70% power reduction).

Serial Output I/O

$\overline{\text{CS}}$ - Chip Select, Pin 2.

This input allows an external device to access the serial port.

$\overline{\text{DRDY}}$ - Data Ready, Pin 20.

Data Ready goes low at the end of a digital filter convolution cycle to indicate that a new output word has been placed into the serial port. $\overline{\text{DRDY}}$ will return high after all data bits are shifted out of the serial port or two master clock cycles before new data becomes available if the $\overline{\text{CS}}$ pin is inactive (high).

SDATA - Serial Data Output, Pin 19.

SDATA is the output pin of the serial output port. Data from this pin will be output at a rate determined by SCLK. Data is output MSB first and advances to the next data bit on the falling edges of SCLK. SDATA will be in a high impedance state when not transmitting data.

SCLK - Serial Clock Input, Pin 18.

A clock signal on this pin determines the output rate of the data from the SDATA pin. This pin must not be allowed to float.

Control Input Pins

CAL - Calibrate, Pin 4.

When taken high the same time that the CONV pin is taken high the converter will perform a self-calibration which includes calibration of the offset and gain scale factors in the converter.

CONV - Convert, Pin 3.

The CONV pin initiates a calibration cycle if it is taken from low to high while the CAL pin is high, or it initiates a conversion if it is taken from low to high with the CAL pin low. If CONV is held high (CAL low) the converter will do continuous conversions.

BP/$\overline{UP}$ - Bipolar/Unipolar, Pin 7.

The BP/$\overline{UP}$ pin selects the conversion mode of the converter. When high the converter will convert bipolar input signals; when low it will convert unipolar input signals.

A0 - Multiplexer Selection Input, Pin 1.

Selects the input channel for conversion. A0=0=AIN1. A0 is latched when CONV transitions from low to high. This input has a pull-down resistor internal to the chip.

Measurement and Reference Inputs

AIN1+, AIN2+, AIN1-, AIN2- - Differential Analog Inputs, Pins 8, 9, 10, 11.

Analog differential inputs to the delta-sigma modulator.

VREF+, VREF- - Differential Voltage Reference Inputs, Pins 12, 13.

A differential voltage reference on these pins operates as the voltage reference for the converter. The voltage between these pins can be any voltage between 1.0 and 3.6 volts.

Power Supply Connections

VA+ - Positive Analog Power, Pin 14.

Positive analog supply voltage. Nominally +5 volts.

VA- - Negative Analog Power, Pin 15.

Negative analog supply voltage. Nominally -5volts.

VD+ - Positive Digital Power, Pin 17.

Positive digital supply voltage. Nominally +5 volts or +3.3 volts.

DGND - Digital Ground, Pin 16.

Digital Ground.

SPECIFICATION DEFINITIONS

Linearity Error

The deviation of a code from a straight line which connects the two endpoints of the A/D Converter transfer function. One endpoint is located 1/2 LSB below the first code transition and the other endpoint is located 1/2 LSB beyond the code transition to all ones. Units in percent of full-scale.

Differential Nonlinearity

The deviation of a code's width from the ideal width. Units in LSBs.

Full Scale Error

The deviation of the last code transition from the ideal [{(VREF+) - (VREF-)} - 3/2 LSB]. Units are in LSBs.

Unipolar Offset

The deviation of the first code transition from the ideal (1/2 LSB above the voltage on the AIN- pin.) when in unipolar mode (BP/$\overline{UP}$ low). Units are in LSBs.

Bipolar Offset

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below the voltage on the AIN- pin.) when in bipolar mode (BP/$\overline{UP}$ high). Units are in LSBs

APPENDIX

The following companies provide 32.768 kHz crystals in many package varieties and temperature ranges.

Fox Electronics
5570 Enterprise Parkway
Fort Meyers, FL 33905
(813) 693-0099

Micro Crystal Division / SMH
702 West Algonquin Road
Arlington Heights, IL 60005
(708) 806-1485

SaRonix
4010 Transport Street
Palo Alto, California 94303
(415) 856-6900

Statek
512 North Main
Orange, California 92668
(714) 639-7810

IQD Ltd.
North Street
Crewkerne
Somerset TA18 7AK
England
01460 77155

Mr. Pierre Hersberger
Microcrystal/DIV. ETA S.A.
Schild-Rust-Strasse 17
Grenchen CH-2540
Switzerland
065 53 05 57

Taiwan X'tal Corp.
5F. No. 16, Sec 2, Chung Yang S. RD.
Reitou, Taipei, Taiwan R. O. C.
Tel: 02-894-1202
Fax: 02-895-6207

Interquip Limited
24/F Million Fortune Industrial Centre
34-36 Chai Wan Kok Street, Tsuen Wan N T
Tel: 4135515
Fax: 4137053

S& T Enterprises, Ltd.
Rm 404 Blk B
Sea View Estate
North Point, Hong Kong
Tel: 5784921
Fax: 8073126

Mr. Darren Mcleod
Hy-Q International Pty. Ltd.
12 Rosella Road,
FRANKSON, 3199
Victoria, Australia
Tel: 61-3-783 9611
Fax: 61-3-783 9703

Semiconductor Corporation

CDB5504

Evaluation Board for CS5504 A/D Converter

Features

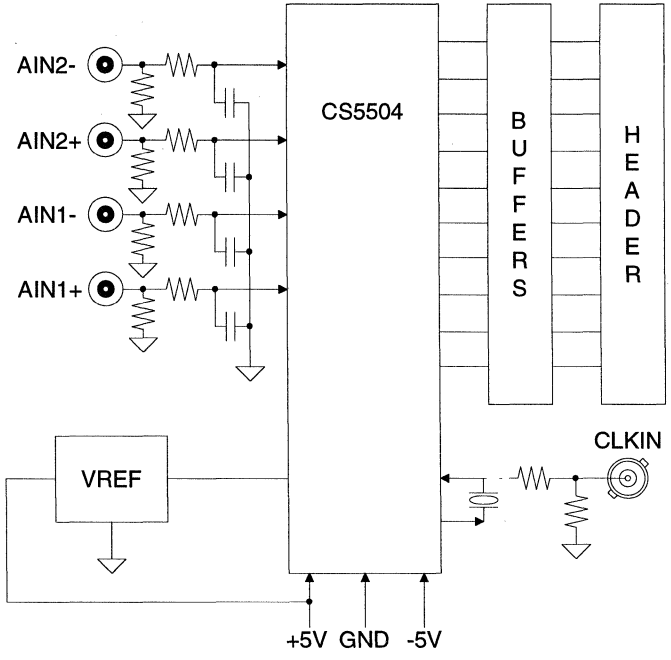
- Operation with on-board 32.768 kHz crystal or off-board clock source
- DIP Switch Selectable: BP/$\overline{UP}$ mode; Channel selection
- On-board precision voltage reference
- Access to all digital control pins

General Description

The CDB5504 is a circuit board designed to provide quick evaluation of the CS5504 A/D converter.

The board provides buffered digital signals, an on-board precision voltage reference, options for using an external clock, and a momentary switch to initiate calibration.

ORDERING INFORMATION: CDB5504



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Introduction

The CDB5504 evaluation board provides a quick means of testing the CS5504 A/D converter. The CS5504 converter require a minimal amount of external circuitry. The evaluation board comes configured with the A/D converter chip operating from a 32.768 kHz crystal and with an off-chip precision 2.5 volt reference. The board provides access to all of the digital interface pins of the CS5504 chip.

The board is configured for operation from +5 and -5 volt power supplies, but can be operated from a single +5 volt supply if the -5V binding post is shorted to the GND binding post.

Evaluation Board Overview

The board provides a complete means of making the CS5504 A/D converter chip function. The user must provide a means of taking the output data from the board in serial format and using it in his system.

Figure 1 illustrates the schematic for the board. The board comes configured for the A/D converter chip to operate from the 32.768 kHz watch crystal. A BNC connector for an external clock is provided on the board. To connect the external BNC source to the converter chip, a circuit trace must be cut. Then a jumper must be inserted in the proper holes to connect the XIN pin of the converter to the input line from the BNC. The BNC input is terminated with a 50Ω resistor. Remove this resistor if driving from a logic gate. See the schematic in Figure 1.

The board comes with the A/D converter VREF+ and VREF- pins hard-wired to the 2.5 volt bandgap voltage reference IC on the board.

All of the control pins of the CS5504 are available at the J1 header connector. Buffer ICs U2 and U3 are used to buffer the converter for interface to off-board circuits. The buffers are used on the evaluation board only because the exact loading and off-board circuitry is unknown. Most applications will not require the buffer ICs for proper operation.

To put the board in operation, select either bipolar or unipolar mode with DIP switch S2. Then press the CAL pushbutton after the board is powered up. This initiates calibration of the converter which is required before measurements can be taken.

To select an input, one of two channels, use DIP switch S2 to select the input for A0 (see Table 1). Once A0 is selected, the CONV switch (S2-3) must be switched on (closed) and then open to cause the CONV signal to transition low to high. This latches the A0 channel selection into the converter. With CONV high (S2-3 open) the converter will convert continuously.

Figure 3 illustrates the CAB5504 adapter board. The CAB5504 translates a CS5505 pinout to a CS5504 pinout.

Figures 4 and 5 illustrate the evaluation board layout while Figure 6 illustrates the component placement (silkscreen) of the evaluation board.

A0	Channel Addressed
0	AIN1
1	AIN2

Table 1. Multiplexer Truth Table

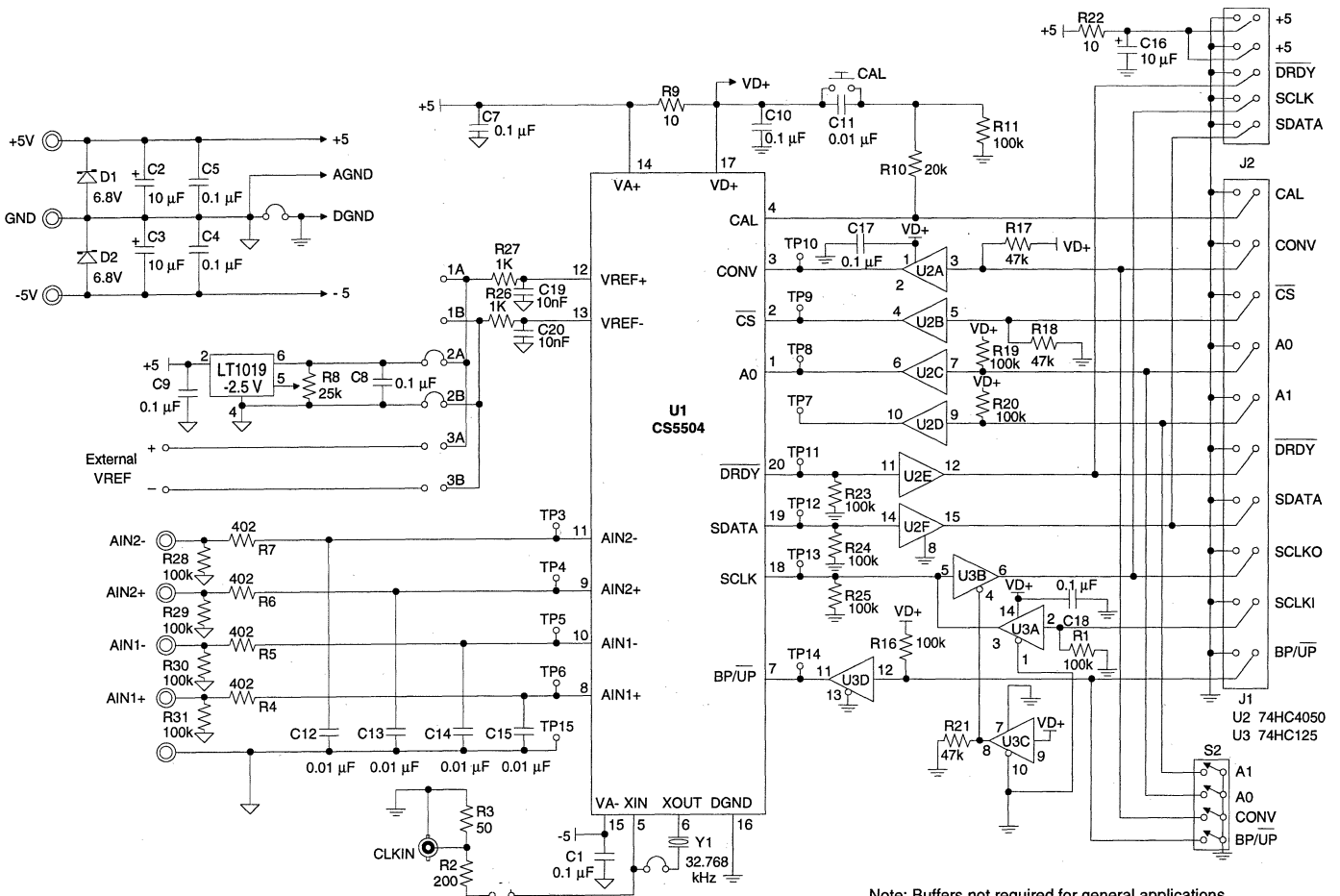


Figure 1. ADC Connections

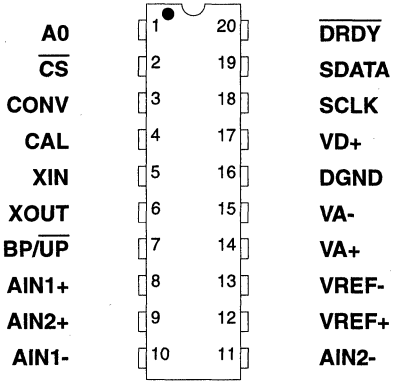


Figure 2. CS5504 Pin Layout

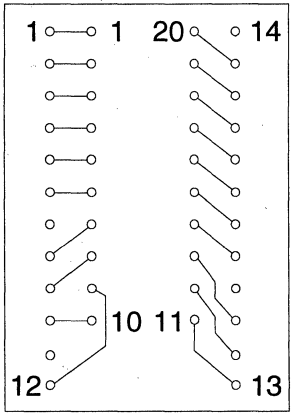


Figure 3. CAB5504 Adapter Board

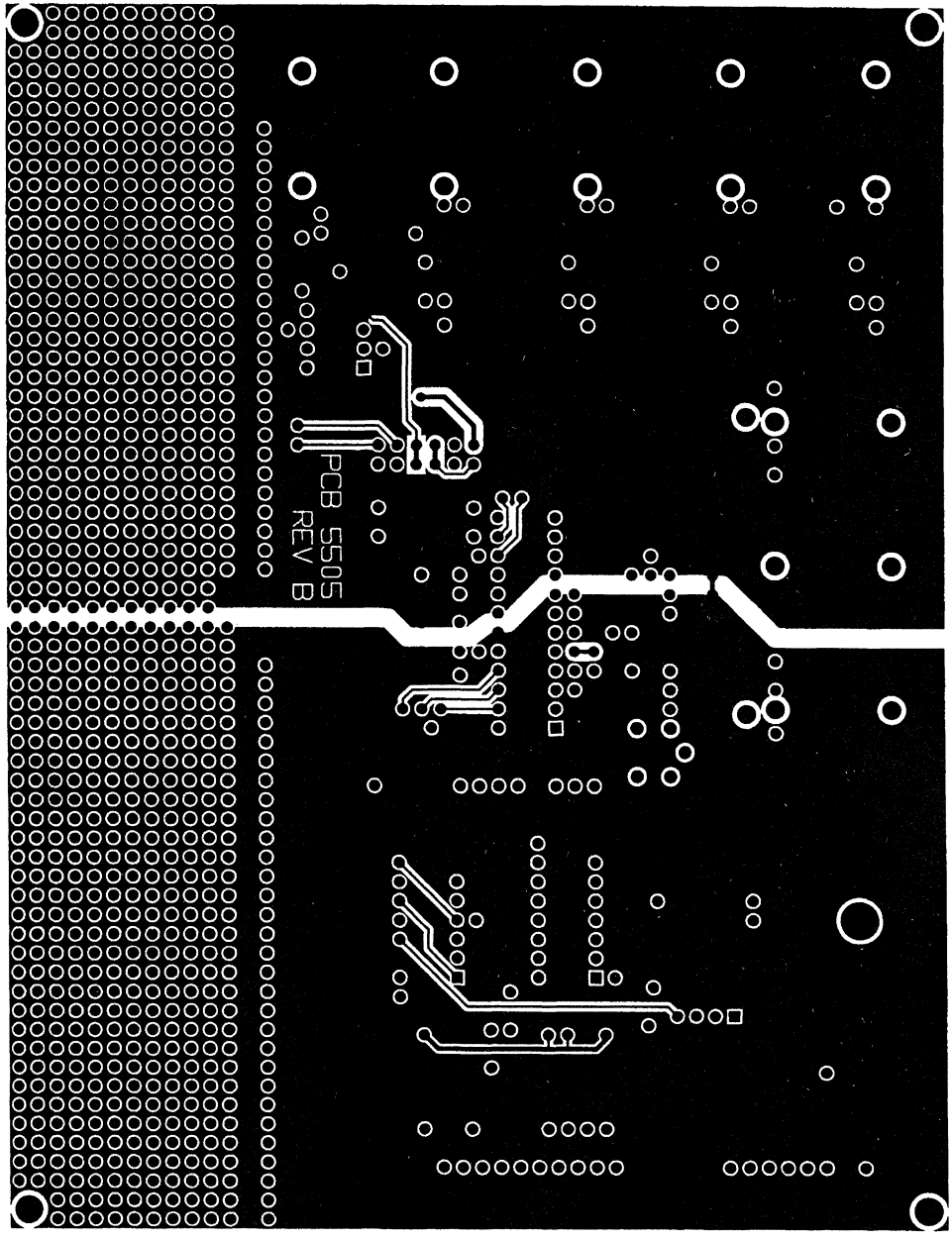


Figure 4. Top Ground Plane Layer (NOT TO SCALE)

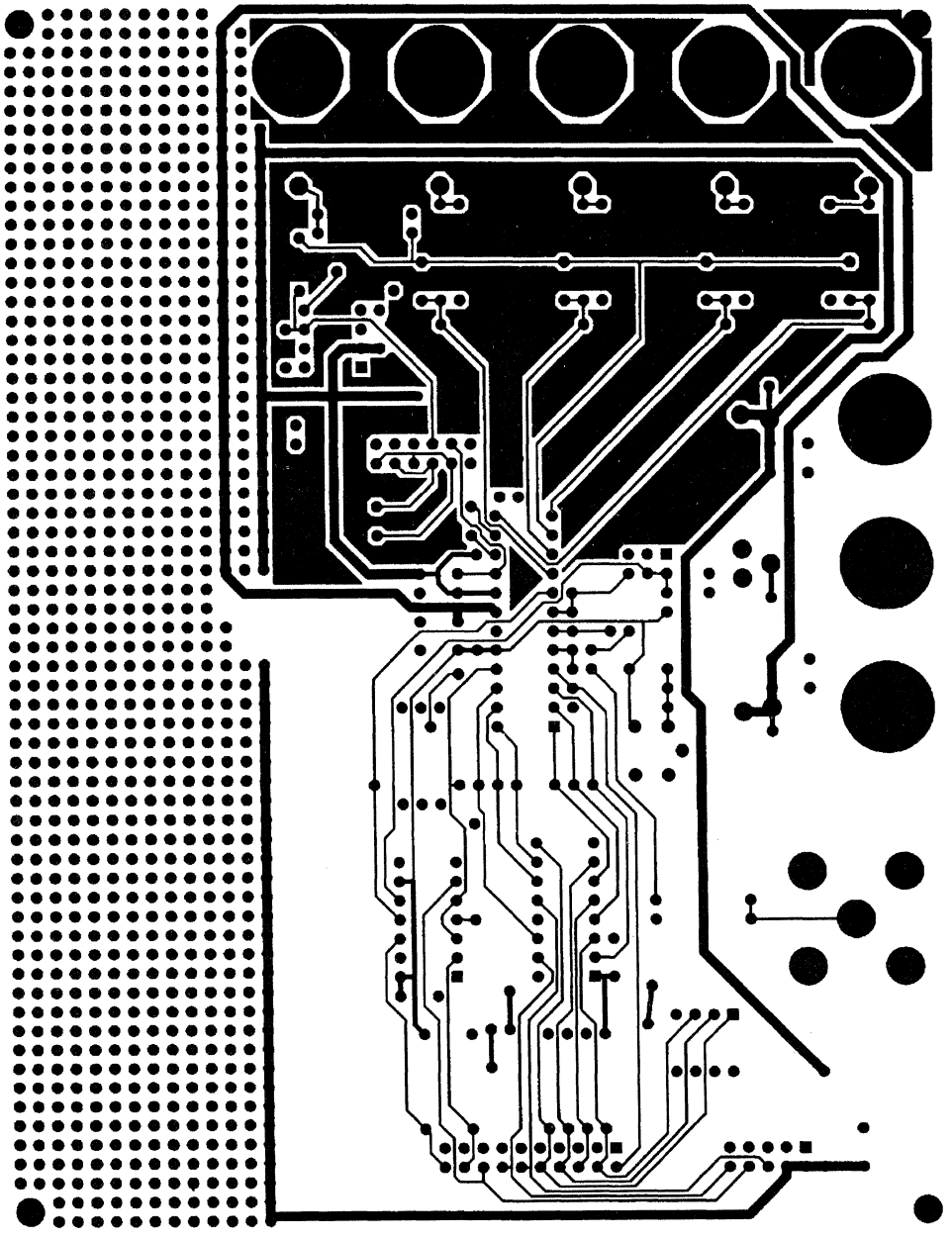


Figure 5. Bottom Trace Layer (NOT TO SCALE)

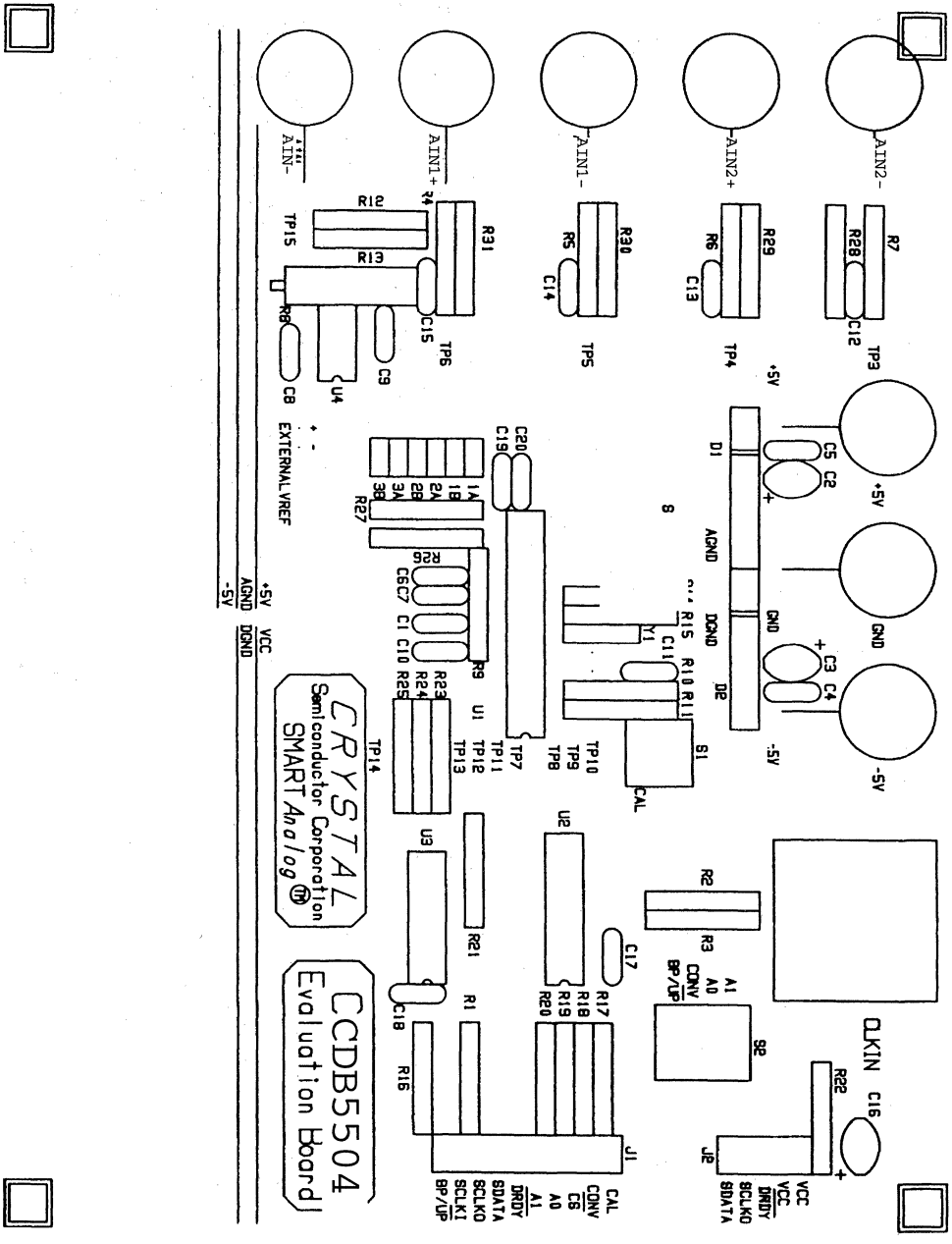


Figure 6. Silk Screen Layer (NOT TO SCALE)

Very Low Power, 16-Bit and 20-Bit A/D Converters

Features

- Very Low Power Consumption
  Single supply +5V operation: 1.7 mW
  Dual supply ±5V operation: 3.2 mW
- Offers superior performance to VFCs and multi-slope integrating ADCs
- Differential Inputs
  Single Channel (CS5507/8) and Four-Channel (CS5505/6) pseudo-differential versions
- Either 5V or 3.3V Digital Interface
- Linearity Error:
  ±0.0015% FS (16-bit CS5505/7)
  ±0.0007% FS (20-bit CS5506/8)
- Output update rates up to 100/second
- Flexible Serial Port
- Pin-Selectable Unipolar/Bipolar Ranges

General Description

The CS5505/6/7/8 are a family of low power CMOS A/D converters which are ideal for measuring low-frequency signals representing physical, chemical, and biological processes.

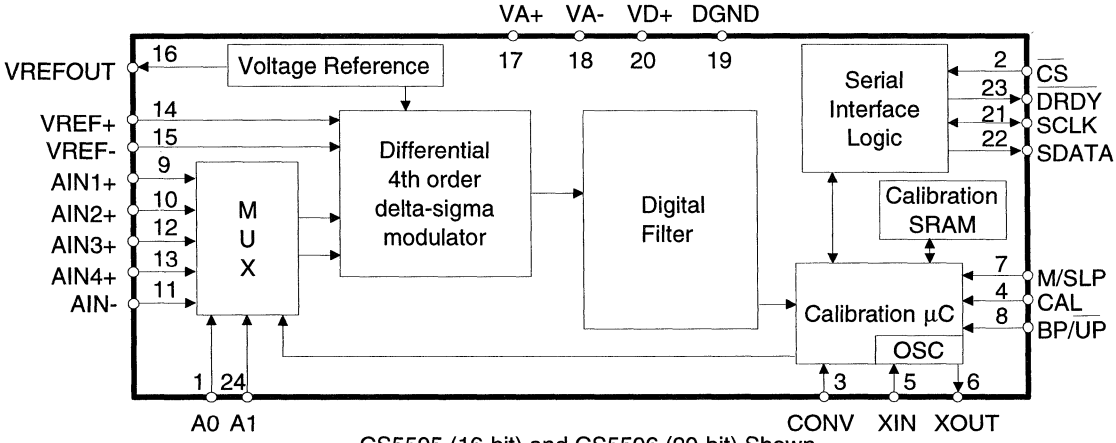
The CS5507/8 have single-channel differential analog and reference inputs while the CS5505/6 have four pseudo-differential analog input channels. The CS5505/7 have a 16-bit output word. The CS5506/8 have a 20-bit output word. The CS5505/6/7/8 sample upon command up to 100 output updates per second.

The on-chip digital filter offers superior line rejection at 50 and 60Hz when the device is operated from a 32.768 kHz clock (output word rate = 20 Hz.).

The CS5505/6/7/8 include on-chip self-calibration circuitry which can be initiated at any time or temperature to ensure minimum offset and full-scale errors.

The CS5505/6/7/8 serial port offers two general-purpose modes for the direct interface to shift registers or synchronous serial ports of industry-standard microcontrollers.

ORDERING INFORMATION: Page 2-480



CS5505 (16-bit) and CS5506 (20-bit) Shown

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

ANALOG CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+ = 5V ± 10%; VA- = -5V ± 10%; VD+ = 3.3V ± 5%; VREF+ = 2.5V(external); VREF- = 0V; f_{CLK} = 32.768kHz; Bipolar Mode; R_{source} = 1kΩ with a 10nF to AGND at AIN; Analog input channel AIN1+; AIN- = AGND; unless otherwise specified.) (Notes 1, 2)

Parameter*		CS5505/7-A Min	CS5505/7-A Typ	CS5505/7-A Max	CS5507-S Min	CS5507-S Typ	CS5507-S Max	Units
Specified Temperature Range			-40 to +85			-55 to +125		°C
Accuracy								
Linearity Error		-	0.0015	0.003	-	0.0015	0.003	±%FS
Differential Nonlinearity		-	±0.25	±0.5	-	±0.25	±0.5	LSB_{16}
Full Scale Error	(Note 3)	-	±0.25	±2	-	±0.5	±2	LSB_{16}
Full Scale Drift	(Note 4)	-	±0.5	-	-	±2	-	LSB_{16}
Unipolar Offset	(Note 3)	-	±0.5	±2	-	±1	±4	LSB_{16}
Unipolar Offset Drift	(Note 4)	-	±0.5	-	-	±1	-	LSB_{16}
Bipolar Offset	(Note 3)	-	±0.25	±1	-	±0.5	±2	LSB_{16}
Bipolar Offset Drift	(Note 4)	-	±0.25	-	-	±0.5	-	LSB_{16}
Noise (Referred to Output)		-	0.16	-	-	0.16	-	$LSB\text{-}rms_{16}$

Notes:
1. The AIN pin presents a very high input resistance at dc and a minor dynamic load which scales to the master clock frequency. Both source resistance and shunt capacitance are therefore critical in determining the CS5505/6/7/8's source impedance requirements. For more information refer to the text section *Analog Input Impedance Considerations.*
2. Specifications guaranteed by design, characterization and/or test.
3. Applies after calibration at the temperature of interest.
4. Total drift over the specified temperature range since calibration at power-up at 25°C. Recalibration at any temperature will remove these errors.

	Unipolar Mode			Bipolar Mode		
mV	LSB's	% FS	ppm FS	LSB's	% FS	ppm FS
10	0.26	0.0004	4	0.13	0.0002	2
19	0.50	0.0008	8	0.26	0.0004	4
38	1.00	0.0015	15	0.50	0.0008	8
76	2.00	0.0030	30	1.00	0.0015	15
152	4.00	0.0061	61	2.00	0.0030	30

VREF = 2.5V

CS5505/7; 16-Bit Unit Conversion Factors

* Refer to the Specification Definitions immediately following the Pin Description Section.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+ = 5V ± 10%; VA- = -5V ± 10%; VD+ = 3.3V ± 5%; VREF+ = 2.5V (external); VREF- = 0V; f_{CLK} = 32.768kHz; Bipolar Mode; R_{source} = 1kΩ with a 10nF to AGND at AIN; Analog input channel AIN1+; AIN- = AGND; unless otherwise specified.) (Notes 1, 2)

Parameter*		CS5506/8-B Min	CS5506/8-B Typ	CS5506/8-B Max	CS5508-S Min	CS5508-S Typ	CS5508-S Max	Units
Specified Temperature Range		-40 to +85			-55 to +125			°C
Accuracy								
Linearity Error		-	0.0007	0.0015	-	0.0015	0.003	±%FS
Differential Nonlinearity (No Missing Codes)		20	-	-	20	-	-	Bits
Full Scale Error	(Note 3)	-	±4	±32	-	±8	±32	LSB_{20}
Full Scale Drift	(Note 4)	-	±8	-	-	±32	-	LSB_{20}
Unipolar Offset	(Note 3)	-	±8	±32	-	±16	±64	LSB_{20}
Unipolar Offset Drift	(Note 4)	-	±8	-	-	±16	-	LSB_{20}
Bipolar Offset	(Note 3)	-	±4	±16	-	±8	±32	LSB_{20}
Bipolar Offset Drift	(Note 4)	-	±4	-	-	±8	-	LSB_{20}
Noise (Referred to Output)		-	2.6	-	-	2.6	-	$LSB\text{-}rms_{20}$

	Unipolar Mode			Bipolar Mode		
mV	LSB's	% FS	ppm FS	LSB's	% FS	ppm FS
0.596	0.25	0.0000238	0.24	0.13	0.0000119	0.12
1.192	0.50	0.0000477	0.47	0.26	0.0000238	0.24
2.384	1.00	0.0000954	0.95	0.50	0.0000477	0.47
4.768	2.00	0.0001907	1.91	1.00	0.0000954	0.95
9.537	4.00	0.0003814	3.81	2.00	0.0001907	1.91

VREF = 2.5V

CS5506/8; 20-Bit Unit Conversion Factors

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Units
Modulator Sampling Frequency	f_s	$f_{clk}/2$	Hz
Output Update Rate (CONV = 1)	f_{out}	$f_{clk}/1622$	Hz
Filter Corner Frequency	f_{-3dB}	$f_{clk}/1928$	Hz
Settling Time to ½ LSB (FS Step)	t_s	$1/f_{out}$	s

ANALOG CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+ = 5V ± 10%; VA- = -5V ± 10%; VD+ = 3.3V ± 5%; VREF+ = 2.5V (external); VREF- = 0V; f_{CLK} = 32.768kHz; Bipolar Mode; R_{source} = 1kΩ with a 10nF to AGND at AIN; Analog input channel AIN1+; AIN- = AGND; unless otherwise specified.) (Notes 1, 2)

Parameter*	CS5505/7-A CS5506/8-B Min	Typ	Max	CS5507/8-S Min	Typ	Max	Units
Specified Temperature Range		-40 to +85			-55 to +125		°C
Analog Input							
Analog Input Range: Unipolar		0 to +2.5			0 to +2.5		Volts
(VAIN+)-(VAIN-) Bipolar (Note 5)		±2.5			±2.5		Volts
Common Mode Rejection: dc	-	105	-	-	105	-	dB
50, 60 Hz (Note 6)	120	-	-	120	-	-	dB
Off Channel Isolation	-	120	-	-	120	-	dB
Input Capacitance	-	15	-	-	15	-	pF
DC Bias Current (Note 1)	-	5	-	-	5	-	nA
Voltage Reference (Output)							
VREFOUT Voltage	-	(VA+)-2.5	-	-	(VA+)-2.5	-	Volts
VREFOUT Voltage Tolerance	-	-	4.0	-	-	4.0	%
VREFOUT Voltage Temperature Coefficient	-	60	-	-	60	-	ppm/°C
VREFOUT Line Regulation	-	1.5	-	-	1.5	-	mV/Volt
VREFOUT Output Voltage Noise 0.1 to 10 Hz	-	50	-	-	50	-	μV_{p-p}
VREFOUT: Source Current	-	-	3	-	-	3	µA
Sink Current	-	-	50	-	-	50	µA
Power Supplies							
DC Power Supply Currents: I_{Total}	-	340	450	-	340	450	µA
I_{Analog}	-	300	-	-	300	-	µA
$I_{Digital}$	-	40	-	-	40	-	µA
Power Dissipation: (Note 7)							
SLEEP inactive	-	3.2	4.5	-	3.2	4.5	mW
SLEEP active	-	5	10	-	10	25	µW
Power Supply Rejection: Positive Supplies	-	80	-	-	80	-	dB
Negative Supplies	-	80	-	-	80	-	dB

Notes: 5. Common mode voltage may be at any value as long as AIN+ and AIN- remain within the VA+ and VA- supply voltages.
6. XIN = 32.768 kHz. Guaranteed by design and / or characterization.
7. All outputs unloaded. All inputs CMOS levels. SLEEP mode controlled by M/SLP pin. SLEEP active = M/SLP pin at (VD+)/2 input level.

5V DIGITAL CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+VD+ = 5V ± 10%; VA-= -5V ± 10%; DGND = 0.) All measurements below are performed under static conditions. (Note 2)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage:	XIN	V_{IH}	3.5	-	-	V
	M/SLP	V_{IH}	0.9VD+	-	-	V
	All Pins Except XIN and M/SLP	V_{IH}	2.0	-	-	V
Low-Level Input Voltage:	XIN	V_{IL}	-	-	1.5	V
	M/SLP	V_{IL}	-	-	0.1VD+	V
	All Pins Except XIN and M/SLP	V_{IL}	-	-	0.8	V
M/SLP SLEEP Active Threshold	(Note 8)	V_{SLP}	0.45VD+	0.5VD+	0.55VD+	V
High-Level Output Voltage	(Note 9)	V_{OH}	(VD+)-1.0	-	-	V
Low Level Output Voltage	I_{out} = 1.6 mA	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	1	10	µA
3-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

Notes: 8. Under normal operation this pin should be tied to VD+ or DGND. Anytime the voltage on the M/SLP pin enters the SLEEP active threshold range the device will enter the power down condition. Returning to the active state requires elapse of the power-on reset period, the oscillator to start-up, and elapse of the wake-up period.

9. I_{out} = -100 µA. This guarantees the ability to drive one TTL load. (V_{OH} = 2.4V @ I_{out} = -40 µA).

3.3V DIGITAL CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+ = 5V ± 10%; VD+ = 3.3V ± 5%; VA-= -5V ± 10%; DGND = 0.) All measurements below are performed under static conditions. (Note 2)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage:	XIN	V_{IH}	0.7VD+	-	-	V
	M/SLP	VIH	0.9VD+	-	-	V
	All Pins Except XIN and M/SLP	V_{IH}	0.6VD+	-	-	V
Low-Level Input Voltage:	XIN	V_{IL}	-	-	0.3VD+	V
	M/SLP	VIL	-	-	0.1VD+	V
	All Pins Except XIN and M/SLP	V_{IL}	-	-	0.16VD+	V
M/SLP SLEEP Active Threshold	(Note 8)	V_{SLP}	0.43VD+	0.45VD+	0.47VD+	V
High-Level Output Voltage	I_{out} = -400 µA	V_{OH}	(VD+)-0.3	-	-	V
Low Level Output Voltage	I_{out} = 400 µA	V_{OL}	-	-	0.3	V
Input Leakage Current		I_{in}	-	1	10	µA
3-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

5V SWITCHING CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+, VD+ = 5V ± 10%; VA- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF.) (Note 2)

Parameter			Symbol	Min	Typ	Max	Units
Master Clock Frequency:	Internal Oscillator:	-A,B	XIN	30.0	32.768	53.0	kHz
		-S	or	30.0	32.768	34.0	kHz
	External Clock:		f_{clk}	30	-	163	kHz
Master Clock Duty Cycle				40	-	60	%
Rise Times:	Any Digital Input	(Note 10)	t_{rise}	-	-	1.0	µs
	Any Digital Output			-	50	-	ns
Fall Times:	Any Digital Input	(Note 10)	t_{fall}	-	-	1.0	µs
	Any Digital Output			-	20	-	ns
Start-Up							
Power-On Reset Period		(Note 11)	t_{res}	-	10	-	ms
Oscillator Start-up Time	XTAL=32.768 kHz	(Note 12)	t_{osu}	-	500	-	ms
Wake-up Period		(Note 13)	t_{wup}	-	$1800/f_{clk}$	-	s
Calibration							
CONV Pulse Width (CAL = 1)		(Note 14)	t_{ccw}	100	-	-	ns
CONV and CAL High to Start of Calibration			t_{scl}	-	-	$2/f_{clk}+200$	ns
Start of Calibration to End of Calibration			t_{cal}	-	$3246/f_{clk}$	-	s
Conversion							
Set Up Time	A0, A1 to CONV High		t_{sac}	50	-	-	ns
Hold Time	A0, A1 after CONV High		t_{hca}	100	-	-	ns
CONV Pulse Width			t_{cpw}	100	-	-	ns
CONV High to Start of Conversion			t_{scn}	-	-	$2/f_{clk}+200$	ns
Set Up Time	BP/$\overline{UP}$ stable prior to $\overline{DRDY}$ falling		t_{bus}	$82/f_{clk}$	-	-	s
Hold Time	BP/$\overline{UP}$ stable after $\overline{DRDY}$ falls		t_{buh}	0	-	-	ns
Start of Conversion to End of Conversion		(Note 15)	t_{con}	-	$1624/f_{clk}$	-	s

Notes: 10. Specified using 10% and 90% points on waveform of interest.
11. An internal power-on-reset is activated whenever power is applied to the device, or when coming out of a SLEEP state.
12. Oscillator start-up time varies with the crystal parameters. This specification does not apply when using an external clock source.
13. The wake-up period begins once the oscillator starts; or when using an external f_{clk}, after the power-on reset time elapses.
14. Calibration can also be initiated by pulsing CAL high while CONV=1.
15. Conversion time will be $1622/f_{clk}$ if CONV remains high continuously.

3.3V SWITCHING CHARACTERISTICS (T_A = T_{MIN} to T_{MAX} VA+ = 5V ± 10%; VD+ = 3.3V ± 5%; VA- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; CL = 50 pF.) (Note 2)

Parameter			Symbol	Min	Typ	Max	Units
Master Clock Frequency:	Internal Oscillator:	-A,B	XIN	30.0	32.768	53.0	kHz
		-S	or	30.0	32.768	34.0	kHz
	External Clock:		f_{clk}	30	-	163	kHz
Master Clock Duty Cycle				40	-	60	%
Rise Times:	Any Digital Input	(Note 10)	t_{rise}	-	-	1.0	µs
	Any Digital Output			-	50	-	ns
Fall Times:	Any Digital Input	(Note 10)	t_{fall}	-	-	1.0	µs
	Any Digital Output			-	20	-	ns
Start-Up							
Power-On Reset Period		(Note 11)	t_{res}	-	10	-	ms
Oscillator Start-up Time	XTAL=32.768 kHz	(Note 12)	t_{osu}	-	500	-	ms
Wake-up Period		(Note 13)	t_{wup}	-	$1800/f_{clk}$	-	s
Calibration							
CONV Pulse Width (CAL = 1)		(Note 14)	t_{ccw}	100	-	-	ns
CONV and CAL High to Start of Calibration			t_{scl}	-	-	$2/f_{clk}+200$	ns
Start of Calibration to End of Calibration			t_{cal}	-	$3246/f_{clk}$	-	s
Conversion							
Set Up Time	A0, A1 to CONV High		t_{sac}	50	-	-	ns
Hold Time	A0, A1 after CONV High		t_{hca}	100	-	-	ns
CONV Pulse Width			t_{cpw}	100	-	-	ns
CONV High to Start of Conversion			t_{scn}	-	-	$2/f_{clk}+200$	ns
Set Up Time	BP/$\overline{UP}$ stable prior to $\overline{DRDY}$ falling		t_{bus}	$82/f_{clk}$	-	-	s
Hold Time	BP/$\overline{UP}$ stable after $\overline{DRDY}$ falls		t_{buh}	0	-	-	ns
Start of Conversion to End of Conversion		(Note 15)	t_{con}	-	$1624/f_{clk}$	-	s

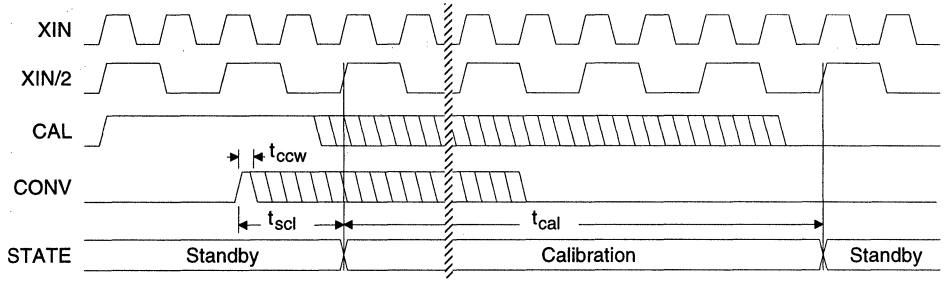


Figure 1. Calibration Timing (Not to Scale)

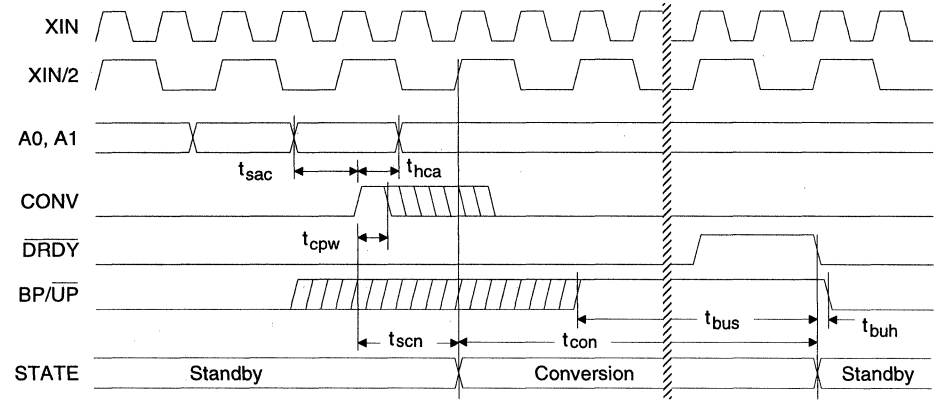


Figure 2. Conversion Timing (Not to Scale)

5V SWITCHING CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}; VA+, VD+ = 5V ± 10%; VA- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF.) (Note 2)

Parameter		Symbol	Min	Typ	Max	Units
SSC Mode (M/SLP = VD+)						
Access Time:	$\overline{CS}$ Low to SDATA out ($\overline{DRDY}$ = low) $\overline{DRDY}$ falling to MSB ($\overline{CS}$ = low)	t_{csd1} t_{dfd}	- -	- $2/f_{clk}$	$2/f_{clk}$ $3/f_{clk}$	ns ns
SDATA Delay Time:	SCLK falling to next SDATA bit	t_{dd1}	-	80	250	ns
SCLK Delay Time	SDATA MSB bit to SCLK rising	t_{cd1}	-	$1/f_{clk}$	-	ns
Serial Clock (Out)	Pulse Width High Pulse Width Low	t_{ph1} t_{pl1}	- -	$1/f_{clk}$ $1/f_{clk}$	- -	ns ns
Output Float Delay:	$\overline{CS}$ high to output Hi-Z (Note 16) SCLK rising to SDATA Hi-Z	t_{fd1} t_{fd2}	- -	- $1/f_{clk}$	$2/f_{clk}$ -	ns ns
SEC Mode (M/SLP = DGND)						
Serial Clock (In)		f_{sclk}	0	-	2.5	MHz
Serial Clock (In)	Pulse Width High Pulse Width Low	t_{ph2} t_{pl2}	200 200	- -	- -	ns ns
Access Time:	$\overline{CS}$ Low to data valid (Note 17)	t_{csd2}	-	60	200	ns
Maximum Delay time:	(Note 18) SCLK falling to new SDATA bit	t_{dd2}	-	150	310	ns
Output Float Delay:	$\overline{CS}$ high to output Hi-Z (Note 16) SCLK falling to SDATA Hi-Z	t_{fd3} t_{fd4}	- -	60 160	150 300	ns ns

Notes: 16. If $\overline{CS}$ is returned high before all data bits are output, the SDATA and SCLK outputs will complete the current data bit and then go to high impedance.

17. If $\overline{CS}$ is activated asynchronously to $\overline{DRDY}$, $\overline{CS}$ will not be recognized if it occurs when $\overline{DRDY}$ is high for 2 clock cycles. The propagation delay time may be as great as 2 f_{clk} cycles plus 200 ns. To guarantee proper clocking of SDATA when using asynchronous $\overline{CS}$, SCLK(i) should not be taken high sooner than 2 f_{clk} + 200 ns after $\overline{CS}$ goes low.

18. SDATA transitions on the falling edge of SCLK. Note that a rising SCLK must occur to enable the serial port shifting mechanism before falling edges can be recognized.

3.3V SWITCHING CHARACTERISTICS (T_A = T_{MIN} to T_{MAX} VA+ = 5V ± 10%; VD+ = 3.3V ± 5%; VA- = -5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF.) (Note 2)

Parameter		Symbol	Min	Typ	Max	Units
SSC Mode (M/SLP = VD+)						
Access Time:	$\overline{CS}$ Low to SDATA out ($\overline{DRDY}$ = low) $\overline{DRDY}$ falling to MSB ($\overline{CS}$ = low)	t_{csd1} t_{dfd}	- -	- 2/f_{clk}	2/f_{clk} 3/f_{clk}	ns ns
SDATA Delay Time:	SCLK falling to next SDATA bit	t_{dd1}	-	265	400	ns
SCLK Delay Time	SDATA MSB bit to SCLK rising	t_{cd1}	-	1/f_{clk}	-	ns
Serial Clock (Out)	Pulse Width High Pulse Width Low	t_{ph1} t_{pl1}	- -	1/f_{clk} 1/f_{clk}	- -	ns ns
Output Float Delay:	$\overline{CS}$ high to output Hi-Z (Note 16) SCLK rising to SDATA Hi-Z	t_{fd1} t_{fd2}	- -	- 1/f_{clk}	2/f_{clk} -	ns ns
SEC Mode (M/SLP = DGND)						
Serial Clock (In)		f_{sclk}	0	-	1.25	MHz
Serial Clock (In)	Pulse Width High Pulse Width Low	t_{ph2} t_{pl2}	200 200	- -	- -	ns ns
Access Time:	$\overline{CS}$ Low to data valid (Note 17)	t_{csd2}	-	100	200	ns
Maximum Delay time:	(Note 18) SCLK falling to new SDATA bit	t_{dd2}	-	400	600	ns
Output Float Delay:	$\overline{CS}$ high to output Hi-Z (Note 16) SCLK falling to SDATA Hi-Z	t_{fd3} t_{fd4}	- -	70 320	150 500	ns ns

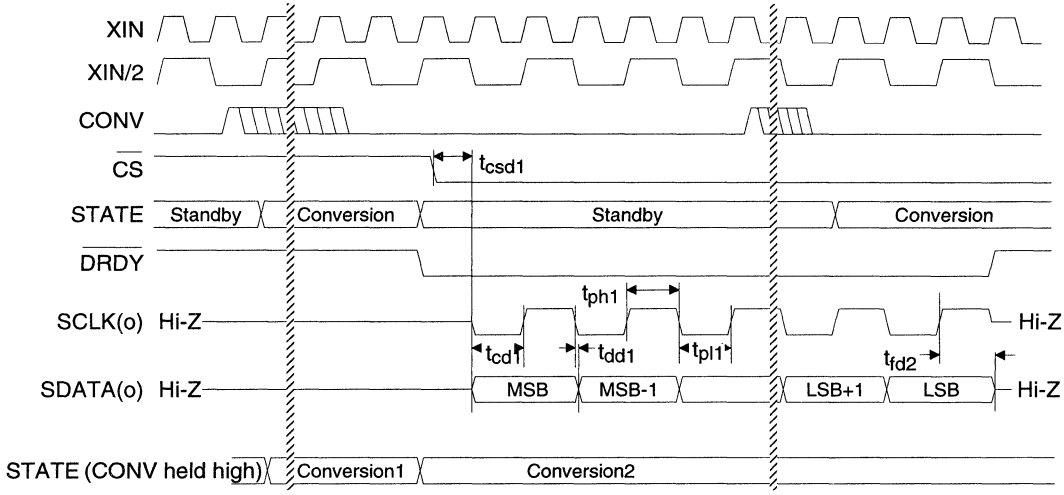


Figure 3. Timing Relationships; SSC Mode (Not to Scale)

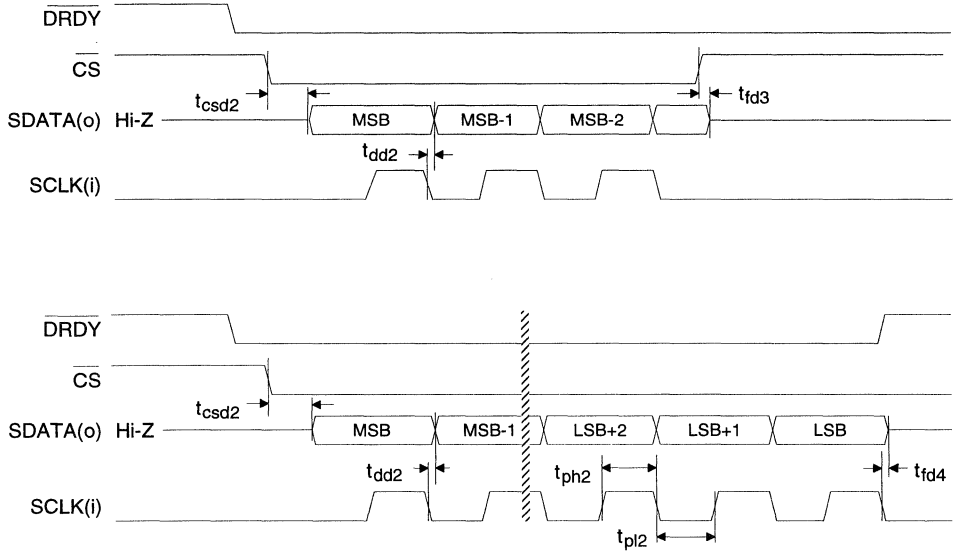


Figure 4. Timing Relationships; SEC Mode (Not to Scale)

RECOMMENDED OPERATING CONDITIONS (DGND = 0V) (Note 19)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive Digital	VD+	3.15	5.0	5.5	V
(VA+)-(VA-)	V_{diff}	4.5	10	11	V
Positive Analog	VA+	4.5	5.0	11	V
Negative Analog	VA-	0	-5.0	-5.5	V
Analog Reference Voltage (Note 20)	(VREF+)-(VREF-)	1.0	2.5	3.6	V
Analog Input Voltage: (Note 21)					
Unipolar	VAIN	0	-	(VREF+)-(VREF-)	V
Bipolar	VAIN	-((VREF+)-(VREF-))	-	+((VREF+)-(VREF-))	V

Notes: 19. All voltages with respect to ground.

20. The CS5505/6/7/8 can be operated with a reference voltage as low as 100 mV; but with a corresponding reduction in noise-free resolution. The common mode voltage of the voltage reference may be any value as long as +VREF and -VREF remain inside the supply values of VA+ and VA-.

21. The CS5505/6/7/8 can accept input voltages up to the analog supplies (VA+ and VA-). In unipolar mode the CS5505/6/7/8 will output all 1's if the dc input magnitude ((AIN+)-(AIN-)) exceeds ((VREF+)-(VREF-)) and will output all 0's if the input becomes more negative than 0 Volts.
In bipolar mode the CS5505/6/7/8 will output all 1's if the dc input magnitude ((AIN+)-(AIN-)) exceeds ((VREF+)-(VREF-)) and will output all 0's if the input becomes more negative in magnitude than -((VREF+)-(VREF-)).

ABSOLUTE MAXIMUM RATINGS*

Parameter			Symbol	Min	Typ	Max	Units
DC Power Supplies:	Digital Ground	(Note 22)	DGND	-0.3	-	(VD+)-0.3	V
	Positive Digital	(Note 23)	VD+	-0.3	-	6.0 or VA+	V
	Positive Analog		VA+	-0.3	-	12.0	V
	Negative Analog		VA-	+0.3	-	-6.0	V
	(VA+)-(VA-)		V_{diff1}	-0.3	-	12.0	V
	(VA+)-(VD+)		V_{diff2}	-0.3	-	12.0	V
Input Current, Any Pin Except Supplies		(Notes 24, 25)	I_{in}	-	-	±10	mA
Analog Input Voltage	AIN and VREF pins		V_{INA}	(VA-)-0.3	-	(VA+)+0.3	V
Digital Input Voltage			V_{IND}	-0.3	-	(VD+)+0.3	V
Ambient Operating Temperature			T_A	-55	-	125	°C
Storage Temperature			T_{stg}	-65	-	150	°C

Notes: 22. No pin should go more positive than (VA+)+0.3V.

23. VD+ must always be less than (VA+)+0.3 V,and can never exceed 6.0V.

24. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pin.

25. Transient currents of up to 100mA will not cause SCR latch-up. Maximum input current for a power supply pin is ± 50 mA.

* WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

GENERAL DESCRIPTION

The CS5505/6/7/8 are very low power monolithic CMOS A/D converters designed specifically for measurement of dc signals. The CS5505/7 are 16-bit converters (a four channel and a single channel version). The CS5506/8 are 20-bit converters (a four channel and a single channel version). Each of the devices includes a delta-sigma charge-balance converter, a voltage reference, a calibration microcontroller with SRAM, a digital filter and a serial interface. The CS5505 and CS5506 include a four channel pseudo-differential (all four channels have the same reference measurement node) multiplexer.

The CS5505/6/7/8 include an on-chip reference but can also utilize an off-chip reference for precision applications. The CS5505/6/7/8 can be used to measure either unipolar or bipolar signals. The devices use self-calibration to insure excellent offset and gain accuracy.

The CS5505/6/7/8 are optimized to operate from a 32.768 kHz crystal but can be driven by an external clock whose frequency is between 30 kHz and 163 kHz. When the digital filter is operated with a 32.768 kHz clock, the filter has zeros precisely at 50 and 60 Hz line frequencies and multiples thereof.

The CS5505/6/7/8 use a "start convert" command to latch the input channel selection and to start a convolution cycle on the digital filter. Once the filter cycle is completed, the output port is updated. When operated with a 32.768 kHz clock the ADC converts and updates its output port at 20 samples/sec. The throughput rate per channel is the output update rate divided by the number of channels being multiplexed. The output port includes a serial interface with two modes of operation.

The CS5505/6/7/8 can operate from dual polarity power supplies (+5 and -5), from a single +5 volt supply, or with +10 volts on the analog and +5 on the digital. They can also operate with dual polarity (+5 and -5), or from a single +5 volt supply on the analog and + 3.3 on the digital.

2

THEORY OF OPERATION FOR THE CS5505/6/7/8

The front page of this data sheet illustrates the block diagram of the CS5505/6.

Basic Converter Operation

The CS5505/6/7/8 A/D converters have four operating states. These are start-up, calibration, conversion and sleep. When power is first applied, the device enters the start-up state. The first step is a power-on reset delay of about 10 ms which resets all of the logic in the device. To proceed with start-up, the oscillator must then begin oscillating. After the power-on reset the device enters the wake-up period for 1800 clock cycles after clock is present. This allows the delta-sigma modulator and other circuitry (which are operating with very low currents) to reach a stable bias condition prior to entering into either the calibration or conversion states. During the 1800 cycle wake-up period, the device can accept an input command. Execution of this command will not occur until the complete wake-up period elapses. If no command is given, the device enters the standby mode.

Calibration

After the initial application of power, the CS5505/6/7/8 must enter the calibration state prior to performing accurate conversions. During calibration, the chip executes a two-step process. The device first performs an offset calibration and then follows this with a gain calibration. The two calibration steps determine the zero reference point and the full scale reference point of the converter's transfer function. From these points it calibrates the zero point and a gain

slope to be used to properly scale the output digital codes when doing conversions.

The calibration state is entered whenever the CAL and CONV pins are high at the same time. The state of the CAL and CONV pins at power-on and when coming out of sleep are recognized as commands, but will not be executed until the end of the 1800 clock cycle wake-up period. Note that any time CONV transitions from low to high, the multiplexer inputs A0 and A1 are latched internal to the CS5505 and CS5506 devices. These latched inputs select the analog input channel which will be used once conversion commences.

If CAL and CONV become active (high) during the 1800 clock cycle wake-up time, the converter will wait until the wake-up period elapses before executing the calibration. If the wake-up time has elapsed, the converter will be in the standby mode waiting for instruction and will enter the calibration cycle immediately. The calibration lasts for 3246 clock cycles. Calibration coefficients are then retained in the SRAM (static RAM) for use during conversion.

At the end of the calibration cycle, the on-chip microcontroller checks the logic state of the CONV signal. If the CONV input is low the device will enter the standby mode where it waits for further instruction. If the CONV signal is high at the end of the calibration cycle, the converter will enter the conversion state and perform a conversion on the input channel which was selected when CONV transitioned from low to high. The CAL signal can be returned low any time after calibration is initiated. CONV can also be returned low, but it should never be taken low and then taken back high until the calibration period has ended and the converter is in the standby state. If CONV is taken low and then high again with CAL high while the converter is calibrating, the device will interrupt the current calibration cycle and start a new one. If CAL is taken low and CONV is taken low and then high during calibration, the calibration cycle will continue as the conversion command is disregarded. The states of A0, A1 and BP/$\overline{UP}$ are not important during calibrations.

If an "end of calibration" signal is desired, pulse the CAL signal high while leaving the CONV signal high continuously. Once the calibration is completed, a conversion will be performed. At the end of the conversion, $\overline{DRDY}$ will fall to indicate the first valid conversion after the calibration has been completed.

See Understanding Converter Calibration for details on how the converter calibrates its transfer function.

Conversion

The conversion state can be entered at the end of the calibration cycle, or whenever the converter is idle in the standby mode. If CONV is taken high to initiate a calibration cycle (CAL also high), and remains high until the calibration cycle is completed (CAL is taken low after CONV transitions high), the converter will begin a conversion upon completion of the calibration period. The device will perform a conversion on the input channel selected by the A0 and A1 inputs when CONV transitioned high. Table 1 indicates the multiplexer channel selection truth table for A0 and A1.

A1	A0	Channel addressed
0	0	AIN1
0	1	AIN2
1	0	AIN3
1	1	AIN4

Table 1. Multiplexer Truth Table

The A0 and A1 inputs are latched internal to the 4-channel devices (CS5505/6) when CONV rises. A0 and A1 have internal pull-down circuits which default the multiplexer to channel AIN1.

The BP/$\overline{UP}$ pin is not a latched input. The BP/$\overline{UP}$ pin controls how the output word from the digital filter is processed. In bipolar mode the output word computed by the digital filter is offset by 8000H in the 16-bit CS5505/7 or 80000H in 20-bit CS5506/8 (see Understanding Converter Calibration). BP/$\overline{UP}$ can be changed after a conversion is started as long as it is stable for 82 clock cycles of the conversion period prior to $\overline{DRDY}$ falling. If one wishes to intermix measurement of bipolar and unipolar signals on various input channels, it is best to switch the BP/$\overline{UP}$ pin immediately after $\overline{DRDY}$ falls and leave BP/$\overline{UP}$ stable until $\overline{DRDY}$ falls again. If the converter is beginning a conversion starting from the standby state, BP/$\overline{UP}$ can be changed at the same time as A0 and A1.

The digital filter in the CS5505/6/7/8 has a Finite Impulse Response and is designed to settle to full accuracy in one conversion time. Therefore, the multiplexer can be changed at the conversion rate.

If CONV is left high, the CS5505/6/7/8 will perform continuous conversions on one channel. The conversion time will be 1622 clock cycles. If conversion is initiated from the standby state, there may be up to two XIN clock cycles of uncertainty as to when conversion actually begins. This is because the internal logic operates at one half the external clock rate and the exact phase of the internal clock may be 180° out of phase relative to the XIN clock. When a new conversion is initiated from the standby state, it will take up to two XIN clock cycles to begin. Actual conversion will use 1624 clock cycles before $\overline{DRDY}$ goes low to indicate that the serial port has been updated. See the Serial Interface Logic section of the data sheet for information on reading data from the serial port.

In the event the A/D conversion command (CONV going positive) is issued during the conversion state, the current conversion will be terminated and a new conversion will be initiated.

Voltage Reference

The CS5505/6/7/8 uses a differential voltage reference input. The positive input is VREF+ and the negative input is VREF-. The voltage between VREF+ and VREF- can range from 1 volt minimum to 3.6 volts maximum. The gain slope will track changes in the reference without recalibration, accommodating ratiometric applications.

The CS5505/6/7/8 include an on-chip voltage reference which outputs 2.5 volts on the VREFOUT pin. This voltage is referenced to the VA+ pin and will track changes relative to VA+. The VREFOUT output requires a 0.1 µF capacitor connected between VREFOUT and VA+ for stability. When using the internal reference, the VREFOUT signal should be connected to the VREF- input and the VREF+ pin should be connected to the VA+ supply. The internal voltage reference is capable of sourcing 3 µA maximum and sinking 50 µA maximum. If a more precise reference voltage is required, an external voltage reference should be used. If an external voltage reference is used, the VREFOUT pin of the internal reference should be connected directly to VA-. It cannot be left open unless the 0.1 µF capacitor is in place for stability.

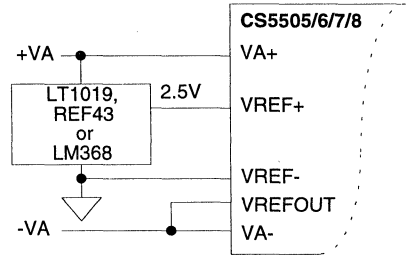


Figure 5. External Reference Connections

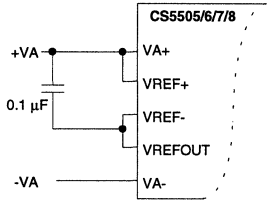


Figure 6. Internal Reference Connections

External reference voltages can range from 1.0 volt minimum to 3.6 volts maximum. The common mode voltage range of the external reference can allow the reference to lie at any voltage between the VA+ and VA- supply rails. Figures 5 and 6 illustrate how the CS5505/6/7/8 converters are connected for external and for internal voltage reference use, respectively.

Analog Input Range

The analog input range is set by the magnitude of the voltage between the VREF+ and VREF- pins. In unipolar mode the input range will equal the magnitude of the voltage reference. In bipolar mode the input voltage range will equate to plus and minus the magnitude of the voltage reference. While the voltage reference can be as great as 3.6 volts, its common mode voltage can be any value as long as the reference inputs VREF+ and VREF- stay within the supply voltages for the A/D. The differential input voltage can also have any common mode value as long as the maximum signal magnitude stays within the supply voltages.

The A/D converter is intended to measure dc or low frequency inputs. It is designed to yield accurate conversions even with noise exceeding the input voltage range as long as the spectral components of this noise will be filtered out by the digital filter. For example, with a 3.0 volt reference in unipolar mode, the converter will accurately convert an input dc signal up to 3.0 volts with up to 15% overrange for 60 Hz noise. A 3.0 volt dc signal could have a 60 Hz component which is 0.5 volts above the maximum input of 3.0 (3.5 volts peak; 3.0 volts dc plus 0.5 volts peak noise) and still accurately convert the input signal (XIN = 32.768 kHz). This assumes that the signal plus noise amplitude stays within the supply voltages.

The CS5505/6/7/8 converters output data in binary format when converting unipolar signals and in offset binary format when converting bipolar signals. Table 2 outlines the output coding for the 16-bit CS5505/7 and the 20-bit CS5506/8 in both unipolar and bipolar measurement modes.

CS5505 and CS5507 (16 Bit)			CS5506 and CS5508 (20 Bit)		
Unipolar Input Voltage	Output Codes	Bipolar Input Voltage	Unipolar Input Voltage	Output Codes	Bipolar Input Voltage
>(VREF - 1.5 LSB)	**FFFF**	>(VREF - 1.5 LSB)	>(VREF - 1.5 LSB)	**FFFFF**	>(VREF - 1.5 LSB)
VREF - 1.5 LSB	**FFFF** **FFFE**	VREF - 1.5 LSB	VREF - 1.5 LSB	**FFFFF** **FFFFE**	VREF - 1.5 LSB
VREF/2 - 0.5 LSB	**8000** **7FFF**	-0.5 LSB	VREF/2 - 0.5 LSB	**80000** **7FFFF**	-0.5 LSB
+0.5 LSB	**0001** **0000**	-VREF + 0.5 LSB	+0.5 LSB	**00001** **00000**	-VREF + 0.5 LSB
<(+0.5 LSB)	**0000**	<(-VREF + 0.5 LSB)	<(+0.5 LSB)	**00000**	<(-VREF + 0.5 LSB)

Note: VREF = (VREF+) - (VREF-); Table excludes common mode voltage on the signal and reference inputs.

Table 2. Output Coding

Understanding Converter Calibration

Calibration can be performed at any time. A calibration sequence will minimize offset errors and set the gain slope scale factor. The delta-sigma modulator in the converter is a differential modulator. To calibrate out offset error, the converter internally connects the modulator differential inputs to an internal VREF- voltage and measures the 1's density output from the modulator. It stores the digital code representation for this 1's density in SRAM and remembers this code as being the zero scale point for the A/D conversion. The converter then connects the negative modulator differential input to the VREF- input and the positive modulator differential input to the VREF+ voltage. The 1's density output from the modulator is then recorded. The converter uses the digital representation of this 1's density along with the digital code for the zero scale point and calculates a gain scale factor. The gain scale factor is stored in SRAM and used for calculating the proper output codes during conversions.

The states of A0, A1 and BP/$\overline{UP}$ are ignored during calibration but should remain stable throughout the calibration period to minimize noise.

When conversions are performed in unipolar mode or in bipolar mode, the converter uses the same calibration factors to compute the digital output code. The only difference is that in bipolar mode the on-chip microcontroller offsets the computed output word by a code value of 8000H (16-bit) or 80000H (20-bit) and multiplies the LSB size by two. This means that the bipolar measurement range is not calibrated from full scale positive to full scale negative. Instead it is calibrated from the bipolar zero scale point to full scale positive. The slope factor is then extended below bipolar zero to accommodate the negative input signals. The converter can be used to convert both unipolar and bipolar signals by changing the BP/$\overline{UP}$ pin. Recalibration is not required when switching between unipolar and bipolar modes.

Converter Performance

The CS5505/6/7/8 A/D converters have excellent linearity performance. Calibration minimizes the errors in offset and gain. The CS5505/7 devices have no missing code performance to 16-bits. The CS5506/8 devices have no missing code performance to 20-bits. Figure 7 illustrates the DNL of the 16-bit CS5505. The converters achieve Common Mode Rejection (CMR) at dc of 105 dB typical, and CMR at 50 and 60 Hz of 120 dB typical.

The CS5505/6/7/8 can experience some drift as temperature changes. The CS5505/6/7/8 use chopper-stabilized techniques to minimize drift. Measurement errors due to offset or gain drift can be eliminated at any time by recalibrating the converter.

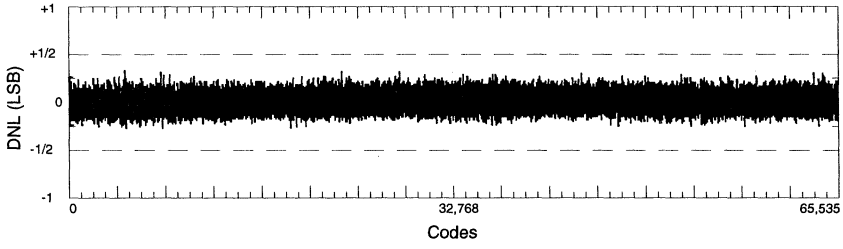


Figure 7. CS5505 Differential Nonlinearity plot.

Analog Input Impedance Considerations

The analog input of the CS5505/6/7/8 can be modeled as illustrated in Figure 8 (the model ignores the multiplexer switch resistance). Capacitors (15 pF each) are used to dynamically sample each of the inputs (AIN+ and AIN-). Every half XIN cycle the switch alternately connects the capacitor to the output of the buffer and then directly to the AIN pin. Whenever the sample capacitor is switched from the output of the buffer to the AIN pin, a small packet of charge (a dynamic demand of current) is required from the input source to settle the voltage of the sample capacitor to its final value. The voltage on the output of the buffer may differ up to 100 mV from the actual input voltage due to the offset voltage of the buffer. Timing allows one half of a XIN clock cycle for the voltage on the sample capacitor to settle to its final value. The equation which defines the settling time is:

$$V_e = V_{max}\, e^{-t/RC}$$

Where Ve is the final settled value, V_{max} is the maximum error voltage value of the input signal, R is the value of the input source resistance, C is the 15 pF sample capacitor plus the value of any stray or additional capacitance at the input pin. The value of t is equal to 1/(2XIN).

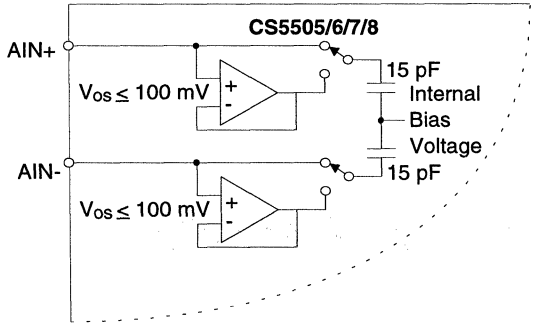


Figure 8. Analog Input Model

V_{max} occurs the instant the sample capacitor is switched from the buffer output to the AIN pin. Prior to switching, AIN has an error estimated as being less than or equal to V_e. V_{max} is equal to the prior error (V_e) plus the additional error from the buffer offset. The estimate for V_{max} is:

$$V_{max} = V_e + 100mV\,\frac{15pF}{(15pF + C_{EXT})}$$

Where C_{EXT} is the combination of any external or stray capacitance.

From the settling time equation, an equation for the maximum acceptable source resistance is derived.

$$Rs_{max} = \frac{-1}{2XIN\,(15pF + C_{EXT})\,\ln\left[\dfrac{V_e}{V_e + \dfrac{15pF(100mv)}{(15pF + C_{EXT})}}\right]}$$

This equation assumes that the offset voltage of the buffer is 100 mV, which is the worst case. The value of Ve is the maximum error voltage which is acceptable.

For a maximum error voltage (Ve) of 10 µV in the CS5505 (1/4LSB at 16-bits) and 600 nV in the CS5506 (1/4LSB at 20-bits), the above equation indicates that when operating from a 32.768 kHz XIN, source resistances up to 110 kΩ in the CS5505 or 84 kΩ in the CS5506 are acceptable in the absence of external capacitance (C_{EXT} = 0). If higher input source resistances are desired the master clock rate can be reduced to yield a longer settling time.

The VREF+ and VREF- inputs have nearly the same structure as the AIN+ and AIN- inputs. Therefore, the discussion on analog input impedance applies to the voltage reference inputs as well.

Digital Filter Characteristics

The digital filter in the CS5505/6/7/8 is the combination of a comb filter and a low pass filter. The comb filter has zeros in its transfer function which are optimally placed to reject line interference frequencies (50 and 60 Hz and their multiples) when the CS5505/6/7/8 is clocked at 32.768 kHz. Figures 9, 10 and 11 illustrate the magnitude and phase characteristics of the filter.

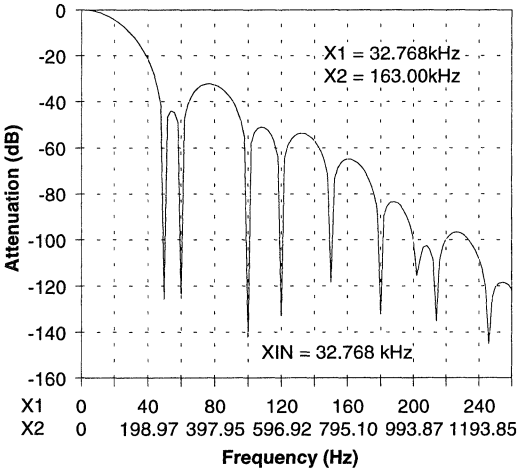


Figure 9. Filter Magnitude Plot to 260 Hz

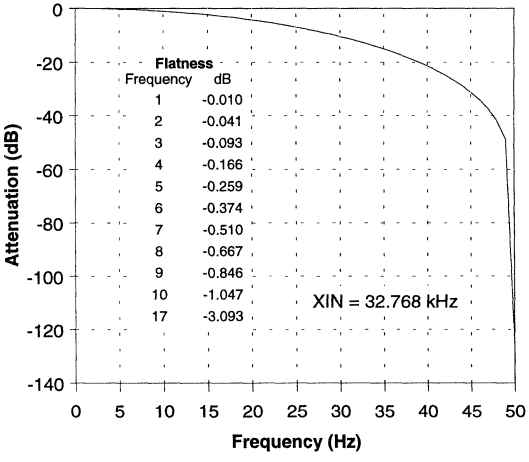


Figure 10. Filter Magnitude Plot to 50 Hz

Figure 9 illustrates the filter attenuation from dc to 260 Hz. At exactly 50, 60, 100, and 120 Hz the filter provides over 120 dB of rejection. Table 3 indicates the filter attenuation for each of the potential line interference frequencies when the converter is operating with a 32.768 kHz clock. The converter yields excellent attenuation of these interference frequencies even if the fundamental line frequency should vary ±1% from its specified frequency. The -3 dB corner frequency of the filter when operating from a 32.768 kHz clock is 17 Hz. Figure 11 illustrates that the phase characteristics of the filter are precisely linear phase.

Frequency (Hz)	Notch Depth (dB)	Frequency (Hz)	Minimum Attenuation (dB)
50	125.6	50±1%	55.5
60	126.7	60±1%	58.4
100	145.7	100±1%	62.2
120	136.0	120±1%	68.4
150	118.4	150±1%	74.9
180	132.9	180±1%	87.9
200	102.5	200±1%	94.0
240	108.4	240±1%	104.4

Table 3. Filter Notch Attenuation (XIN = 32.768 kHz)

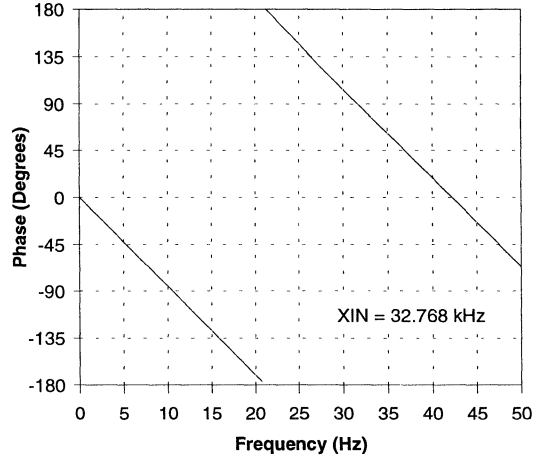


Figure 11. Filter Phase Plot to 50 Hz

If the CS5505/6/7/8 is operated at a clock rate other than 32.768 kHz, the filter characteristics, including the comb filter zeros, will scale with the operating clock frequency. Therefore, optimum rejection of line frequency interference will occur with the CS5505/6/7/8 running at 32.768 kHz. The CS5505/6/7/8 can be used with external clock rates from 30 kHz to 163 kHz.

Anti-Alias Considerations for Spectral Measurement Applications

Input frequencies greater than one half the output word rate (CONV = 1) may be aliased by the converter. To prevent this, input signals should be limited in frequency to no greater than one half the output word rate of the converter (when CONV =1). Frequencies close to the modulator sample rate (XIN/2) and multiples thereof may also be aliased. If the signal source includes spectral components above one half the output word rate (when CONV = 1) these components should be removed by means of low-pass filtering prior to the A/D input to prevent aliasing. Spectral components greater than one half the output word rate on the VREF inputs (VREF+ and VREF-) may also be aliased. Filtering of the reference voltage to remove these spectral components from the reference voltage is desirable.

Crystal Oscillator

The CS5505/6/7/8 is designed to be operated using a 32.768 kHz "tuning fork" type crystal. One end of the crystal should be connected to the XIN input. The other end should be attached to XOUT. Short lead lengths should be used to minimize stray capacitance. Figure 12 illustrates the gate oscillator, and a simplified version of the control logic used on the chip.

Over the industrial temperature range (-40 to +85 °C) the on-chip gate oscillator will oscillate with other crystals in the range of 30 kHz to

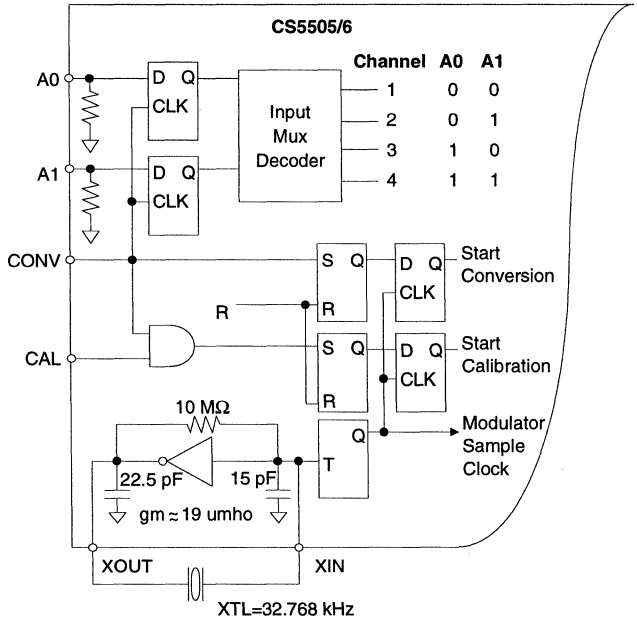


Figure 12. Gate Oscillator and Control Logic

53 kHz. Over the military temperature range (-55 to +125 °C) the on-chip gate oscillator is designed to work only with a 32.768 kHz crystal. The chip will operate with external clock frequencies from 30 kHz to 163 kHz over all temperature ranges. The 32.768 kHz crystal is normally specified as a time-keeping crystal with tight specifications for both initial frequency and for drift over temperature. To maintain excellent frequency stability, these crystals are specified only over limited operating temperature ranges (i.e. -10 to +60 °C) by the manufacturers. Applications of these crystals with the CS5505/6/7/8 do not require tight initial tolerance or low tempco drift. Therefore, a lower cost crystal with looser initial tolerance and tempco will generally be adequate for use with the CS5505/6/7/8 converters. Also check with the manufacturer about wide temperature range application of their standard crystals. Generally, even those crystals specified for limited temperature range will operate over much larger ranges if frequency stability over temperature is not a requirement. The frequency stability can be as bad as ±3000 ppm over the operating temperature range and still be typically better than the line frequency (50 or 60 Hz) stability over cycle to cycle during the course of a day. There are crystals available for operation over the military temperature range (-55 to +125 °C). See the Appendix for suppliers of 32.768 kHz crystals.

Serial Interface Logic

The digital filter in the CS5505/6/7/8 takes 1624 clock cycles to compute an output word once a conversion begins. At the end of the conversion cycle, the filter will attempt to update the serial port. Two clock cycles prior to the update $\overline{\text{DRDY}}$ will go high. When $\overline{\text{DRDY}}$ goes high just prior to a port update it checks to see if the port is either empty or unselected ($\overline{\text{CS}}$ = 1). If the port is empty or unselected, the digital filter will update the port with a new output word. When new data is put into the port $\overline{\text{DRDY}}$ will go low.

Data can be read from the serial port in either of two modes. The M/SLP pin determines which serial mode is selected. Serial port mode selection is as follows:

SSC (Synchronous Self-Clocking) mode; M/SLP = VD+, or SEC (Synchronous External Clocking) mode; M/SLP = DGND. Timing diagrams which illustrate the SSC and SEC timing are in the tables section of this data sheet.

Synchronous Self-Clocking Mode

The serial port operates in the SSC mode when the M/SLP pin is connected to the VD+ pin on the part. In SSC mode the CS5505/6/7/8 furnishes both the serial output data (SDATA) and the serial clock (SCLK). When the serial port is updated at the end of a conversion, $\overline{\text{DRDY}}$ falls. If $\overline{\text{CS}}$ is low, the SDATA and SCLK pins will come out of the high impedance state two XIN clock cycles after $\overline{\text{DRDY}}$ falls. The MSB data bit will be presented for two cycles of XIN clock. The SCLK signal will rise in the middle of the MSB data bit. When SCLK then returns low the (MSB - 1) bit will appear. Subsequent data bits will be output on each falling edge of SCLK until the LSB data bit is output. After the LSB data bit is output, the SCLK will fall at which time both the SDATA and SCLK outputs will return to the high impedance output state. $\overline{\text{DRDY}}$ will return high at this time.

If $\overline{\text{CS}}$ is taken low after $\overline{\text{DRDY}}$ falls, the MSB data bit will appear within two XIN clock cycles after $\overline{\text{CS}}$ is taken low. $\overline{\text{CS}}$ need not be held low for the entire data output. If $\overline{\text{CS}}$ is returned high during a data bit the port will complete the output of that bit and then go into the Hi-Z state. The port can be reselected any time prior to the completion of the next conversion ($\overline{\text{DRDY}}$ falling) to allow the remaining data bits to be output.

Synchronous External-Clocking Mode

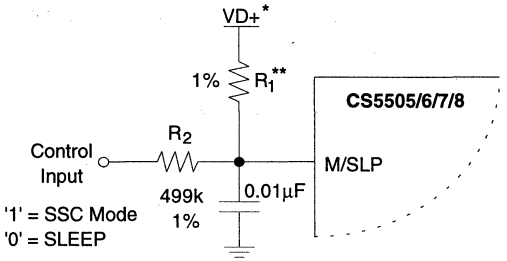
The serial port operates in the SEC mode when the M/SLP pin is connected to the DGND pin. SDATA is the output pin for the serial data. When $\overline{CS}$ goes low after new data becomes available ($\overline{DRDY}$ goes low), the SDATA pin comes out of Hi-Z with the MSB data bit present. SCLK is the input pin for the serial clock in the SEC mode. If the MSB data bit is on the SDATA pin, the first rising edge of SCLK enables the shifting mechanism. This allows the falling edges of SCLK to shift subsequent data bits out of the port. Note that if the MSB data bit is output and the SCLK signal is high, the first falling edge of SCLK will be ignored because the shifting mechanism has not become activated. After the first rising edge of SCLK, each subsequent falling edge will shift out the serial data. Once the LSB is present, the falling edge of SCLK will cause the SDATA output to go to Hi-Z and $\overline{DRDY}$ to return high. The serial port register will be updated with a new data word upon the completion of another conversion if the serial port has been emptied, or if the $\overline{CS}$ is inactive (high).

$\overline{CS}$ can be operated asynchronously to the $\overline{DRDY}$ signal. The $\overline{DRDY}$ signal need not be monitored as long as the $\overline{CS}$ signal is taken low for at least two XIN clock cycles plus 200 ns prior to SCLK being toggled. This ensures that $\overline{CS}$ has gained control over the serial port.

Sleep Mode

The CS5505/6/7/8 devices offer two methods of putting the device into a SLEEP condition to conserve power. Calibration words will be retained in SRAM during either sleep condition. The M/SLP pin can be put into the SLEEP threshold to lower the operating power used by the device to about 1% of nominal. Alternately, the clock into the XIN pin can be stopped. This will lower the power consumed by the converter to about 30% of nominal. In both cases, the converter must go through a wake-up sequence prior to conversions being initiated. This wake-up sequence includes the 10 msec. (typ.) power-on-reset delay, the start-up of the oscillator (unless an external clock is used), and the 1800 clock cycle wake-up delay after the clock begins. When coming out of the sleep condition, the converter will latch the A0 and A1 inputs.

Figure 13 illustrates how to use a gate and resistors to bias the M/SLP pin into the SLEEP threshold region when using the converter in the SSC mode. To use the SEC mode return resistor R1 to DGND instead of the supply. When in the SEC mode configuration the CS5505/6/7/8 will enter the SLEEP threshold when the logic control input is a logic 1 (VD+). Note that large resistors can be used to conserve power while in sleep. The input leakage of the pin is typically less than 1 µA even at 125 °C, although the worst case specification tables indicate a leakage of 10 µA maximum.



* Tie R_1 to DGND for SEC mode; control input logic inverts.

** R_1 = 499k, V_D+ = 5V; R_1 = 590k, V_D+ = 3.3V

Figure 13. Sleep Threshold Control

Power Supplies and Grounding

The analog and digital supply pins to the CS5505/6/7/8 are brought out on separate pins to minimize noise coupling between the analog and digital sections of the chip. Note that there is no analog ground pin. No analog ground pin is required because the inputs for measurement and

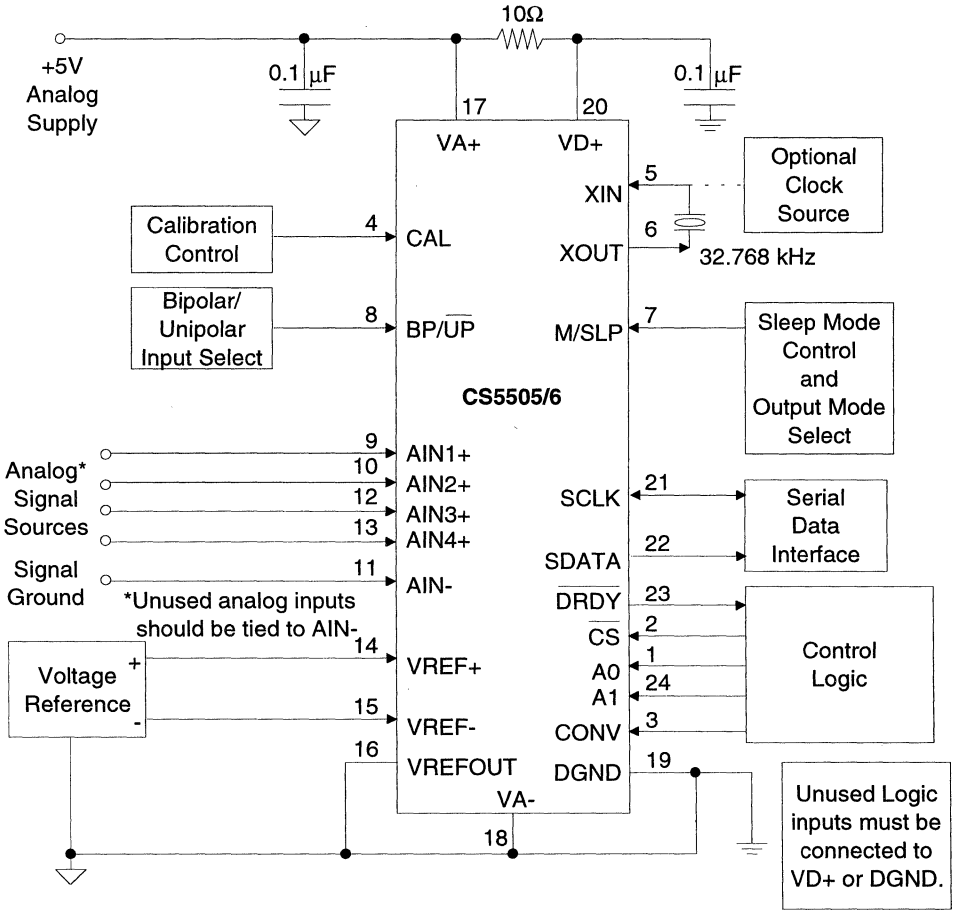
for the voltage reference are differential and require no ground. In the digital section of the chip the supply current flows into the VD+ pin and out of the DGND pin. As a CMOS device, the CS5505/6/7/8 requires that the supply voltage on the VA+ pin always be more positive than the voltage on any other pin of the device. If this requirement is not met, the device can latch-up or be damaged. In all circumstances the VA+ voltage must remain more positive than the VD+ or DGND pins; VD+ must remain more positive than the DGND pin.

The following power supply options are possible:

VA+ = +5V to +10V,	VA- = 0V,	VD+ = +5V
VA+ = +5V,	VA- = -5V,	VD+ = +5V
VA+ = +5V,	VA- = 0V to -5V,	VD+ = +3.3V

The CS5505/6/7/8 cannot be operated with a 3.3V digital supply if VA+ is greater than +5.5V.

Figure 14 illustrates the System Connection Diagram for the CS5505/6 using a single +5V supply. Note that all supply pins are bypassed



Note: To use the internal 2.5 volt reference see Figure 6.

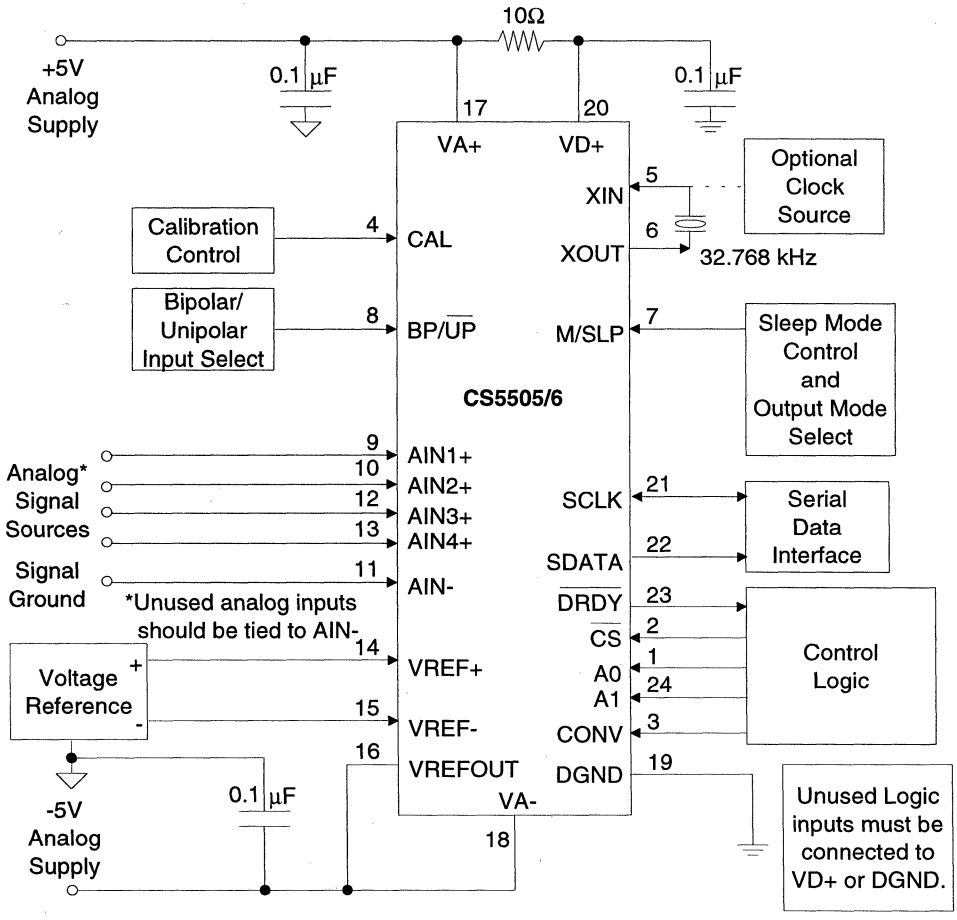
Figure 14. CS5505/6 System Connection Diagram Using External Reference, Single Supply

with 0.1 µF capacitors and that the VD+ digital supply is derived from the VA+ supply.

Figure 15 illustrates the CS5505/6 using dual supplies of +5 and -5V.

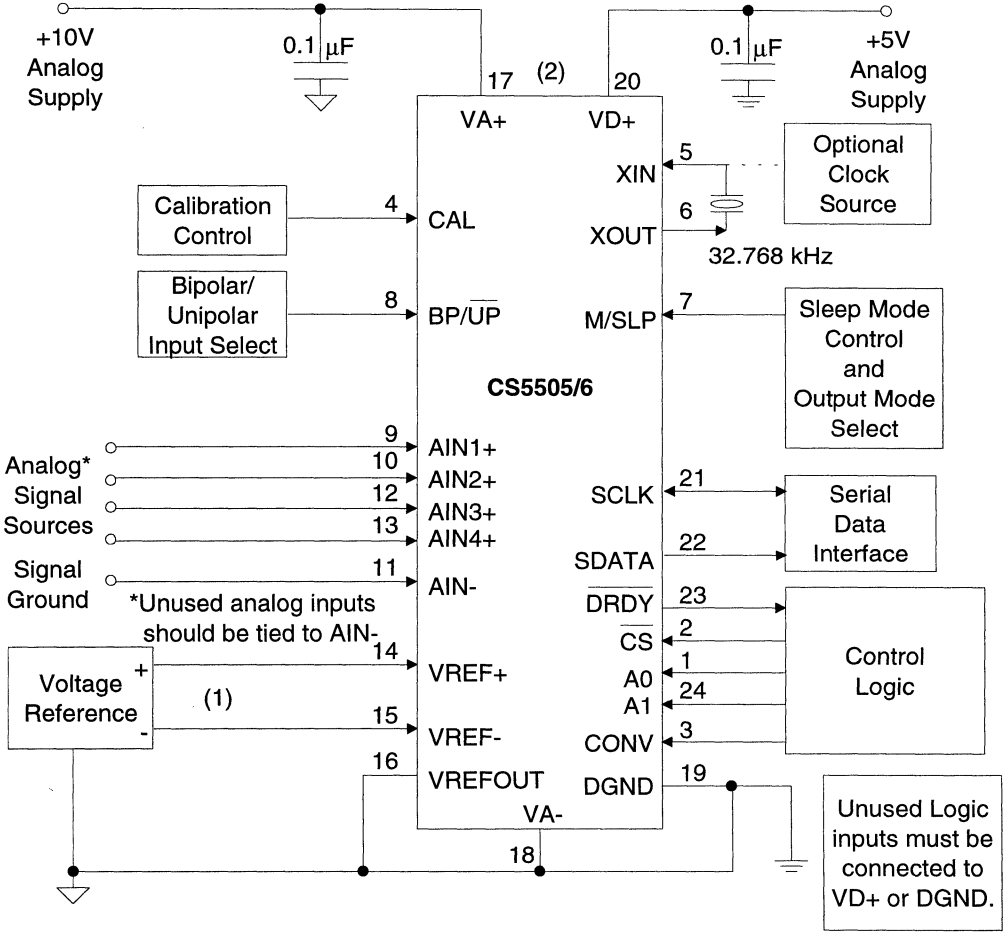
Figure 16 illustrates the CS5505/6 using dual supplies of +10V analog and +5V digital.

When using separate supplies for VA+ and VD+, VA+ must be established first. VD+ should never become more positive than VA+ under any operating condition. Remember to investigate transient power-up conditions, when one power supply may have a faster rise time.



Note: To use the internal 2.5 volt reference see Figure 6.

Figure 15. CS5505/6 System Connection Diagram Using External Reference, Dual Supplies

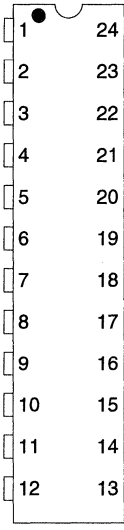


Note: (1) To use the internal 2.5 volt reference see Figure 6.
(2) VD+ must never exceed VA+. Examine power-up conditions.

Figure 16. CS5505/6 System Connection Diagram Using External Reference, Dual Supply, +10V Analog, +5V Digital

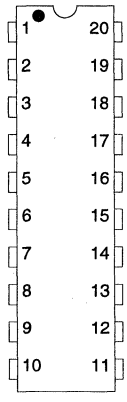
PIN CONNECTIONS*

CS5505/6



MULTIPLEXER SELECTION INPUT	**A0**	1	24	**A1**	MULTIPLEXER SELECTION INPUT
CHIP SELECT	**$\overline{CS}$**	2	23	**$\overline{DRDY}$**	DATA READY
CONVERT	**CONV**	3	22	**SDATA**	SERIAL DATA OUTPUT
CALIBRATE	**CAL**	4	21	**SCLK**	SERIAL CLOCK INPUT/OUTPUT
CRYSTAL IN	**XIN**	5	20	**VD+**	POSITIVE DIGITAL POWER
CRYSTAL OUT	**XOUT**	6	19	**DGND**	DIGITAL GROUND
SERIAL MODE/ SLEEP	**M/SLP**	7	18	**VA-**	NEGATIVE ANALOG POWER
BIPOLAR/UNIPOLAR	**BP/$\overline{UP}$**	8	17	**VA+**	POSITIVE ANALOG POWER
DIFFERENTIAL ANALOG INPUT	**AIN1+**	9	16	**VREFOUT**	VOLTAGE REFERENCE OUTPUT
DIFFERENTIAL ANALOG INPUT	**AIN2+**	10	15	**VREF-**	VOLTAGE REFERENCE INPUT
DIFFERENTIAL ANALOG RETURN	**AIN-**	11	14	**VREF+**	VOLTAGE REFERENCE INPUT
DIFFERENTIAL ANALOG INPUT	**AIN3+**	12	13	**AIN4+**	DIFFERENTIAL ANALOG INPUT

CS5507/8



CHIP SELECT	**$\overline{CS}$**	1	20	**$\overline{DRDY}$**	DATA READY
CONVERT	**CONV**	2	19	**SDATA**	SERIAL DATA OUTPUT
CALIBRATE	**CAL**	3	18	**SCLK**	SERIAL CLOCK INPUT/OUTPUT
CRYSTAL IN	**XIN**	4	17	**VD+**	POSITIVE DIGITAL POWER
CRYSTAL OUT	**XOUT**	5	16	**DGND**	DIGITAL GROUND
SERIAL MODE/ SLEEP	**M/SLP**	6	15	**VA-**	NEGATIVE ANALOG POWER
BIPOLAR/UNIPOLAR	**BP/$\overline{UP}$**	7	14	**VA+**	POSITIVE ANALOG POWER
DIFFERENTIAL ANALOG INPUT	**AIN+**	8	13	**VREFOUT**	VOLTAGE REFERENCE OUTPUT
NO CONNECTION	**NC**	9	12	**VREF-**	VOLTAGE REFERENCE INPUT
DIFFERENTIAL ANALOG INPUT	**AIN-**	10	11	**VREF+**	VOLTAGE REFERENCE INPUT

*Pinout applies to both DIP and SOIC

PIN DESCRIPTIONS

Pin numbers for four channel devices are in parentheses.

Clock Generator

XIN; XOUT - Crystal In; Crystal Out, Pins 4 (5) and 5 (6).

A gate inside the chip is connected to these pins and can be used with a crystal to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock can be supplied into the XIN pin to provide the master clock for the device. Loss of clock will put the device into a lower powered state (approximately 70% power reduction).

Serial Output I/O

M/SLP - Serial Interface Mode Select/ Sleep, Pin 6 (7).

Dual function pin which selects the operating mode of the serial port and provides a very low power sleep function. When M/SLP is tied to the VD+ pin the serial port will operate in the Synchronous Self-Clocking (SSC) mode. When M/SLP is tied to the DGND pin the serial port will operate in the Synchronous External Clocking (SEC) mode. When the M/SLP pin is tied half way between VD+ and DGND the chip will enter into a very low powered sleep mode in which its calibration data will be maintained.

$\overline{\text{CS}}$ - Chip Select, Pin 1 (2).

This input allows an external device to access the serial port.

$\overline{\text{DRDY}}$ - Data Ready, Pin 20 (23)

Data Ready goes low at the end of a digital filter convolution cycle to indicate that a new output word has been placed into the serial port. $\overline{\text{DRDY}}$ will return high after all data bits are shifted out of the serial port or two master clock cycles before new data becomes available if the $\overline{\text{CS}}$ pin is inactive (high).

SDATA - Serial Data Output, Pin 19 (22).

SDATA is the output pin of the serial output port. Data from this pin will be output at a rate determined by SCLK and in a format determined by the M/SLP pin. Data is output MSB first and advances to the next data bit on the falling edges of SCLK. SDATA will be in a high impedance state when not transmitting data.

SCLK - Serial Clock Input/Output, Pin 18 (21).

A clock signal on this pin determines the output rate of the data from the SDATA pin. The M/SLP pin determines whether SCLK is an input or and output. When used as an input, it must not be allowed to float.

Control Input Pins

CAL - Calibrate, Pin 3 (4).

When taken high the same time that the CONV pin is taken high the converter will perform a self-calibration which includes calibration of the offset and gain scale factors in the converter.

CONV - Convert, Pin 2 (3).

The CONV pin initiates a calibration cycle if it is taken from low to high while the CAL pin is high, or it initiates a conversion if it is taken from low to high with the CAL pin low. CONV latches the multiplexer selection when it transitions from low to high on the multiple channel devices. If CONV is held high (CAL low) the converter will do continuous conversions.

A0, A1 - Multiplexer Selection Inputs, Pins (1, 24).

A0 and A1 select the input channel for conversion on the multi-channel input devices. A0 and A1 are latched when CONV transitions from low to high. These two inputs have pull-down resistors internal to the chip.

BP/$\overline{\text{UP}}$ - Bipolar/Unipolar, Pin 7 (8).

The BP/$\overline{\text{UP}}$ pin selects the conversion mode of the converter. When high the converter will convert bipolar input signals; when low it will convert unipolar input signals.

Measurement and Reference Inputs

AIN+, AIN-, (AIN1+, AIN2+, AIN3+, AIN4+, AIN-) - Differential Analog Inputs, Pins 8, 10 (9, 10, 12, 13, 11).

AIN- in the CS5505/6 is a common measurement node for AIN1+, AIN2+, AIN3+ and AIN4+.

VREF+, VREF- - Differential Voltage Reference Inputs, Pins 11, 12 (14, 15).

A differential voltage reference on these pins operates as the voltage reference for the converter. The voltage between these pins can be any voltage between 1.0 and 3.6 volts.

Voltage Reference

VREFOUT - Voltage Reference Output, Pin 13 (16).

The on-chip voltage reference is output from this pin. The voltage reference has a nominal magnitude of 2.5 volts and is referenced to the VA+ pin on the converter.

Power Supply Connections

VA+ - Positive Analog Power, Pin 14 (17).

Positive analog supply voltage. Nominally +5 volts.

VA- - Negative Analog Power, Pin 15 (18).

Negative analog supply voltage. Nominally -5 volts when using dual polarity supplies; or 0 volts (tied to system analog ground) when using single supply operation.

VD+ - Positive Digital Power, Pin 17 (20).
Positive digital supply voltage. Nominally +5 volts or 3.3 volts.

DGND - Digital Ground, Pin 16 (19).
Digital Ground.

Other

NC - No Connection, Pin 9.
Pin should be left floating.

SPECIFICATION DEFINITIONS

Linearity Error
The deviation of a code from a straight line which connects the two endpoints of the A/D Converter transfer function. One endpoint is located 1/2 LSB below the first code transition and the other endpoint is located 1/2 LSB beyond the code transition to all ones. Units in percent of full-scale.

Differential Nonlinearity
The deviation of a code's width from the ideal width. Units in LSBs.

Full Scale Error
The deviation of the last code transition from the ideal [{(VREF+) - (VREF-)} - 3/2 LSB]. Units are in LSBs.

Unipolar Offset
The deviation of the first code transition from the ideal (1/2 LSB above the voltage on the AIN- pin.) when in unipolar mode (BP/$\overline{UP}$ low). Units are in LSBs.

Bipolar Offset
The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below the voltage on the AIN- pin.) when in bipolar mode (BP/$\overline{UP}$ high). Units are in LSBs

Ordering Guide

Model Number	# of Channels	Resolution	Linearity Error	Temperature Range (°C)	Package Type
CS5505-AP	4	16-Bits	0.0030%	-40 to +85	24-pin 0.3" Plastic DIP
CS5505-AS	4	16-Bits	0.0030%	-40 to +85	24-pin 0.3" SOIC
CS5506-BP	4	20-Bits	0.0015%	-40 to +85	24-pin 0.3" Plastic DIP
CS5506-BS	4	20-Bits	0.0015%	-40 to +85	24-pin 0.3" SOIC
CS5507-AP	1	16-Bits	0.0030%	-40 to +85	20-pin 0.3" Plastic DIP
CS5507-AS	1	16-Bits	0.0030%	-40 to +85	20-pin 0.3" SOIC
CS5507-SD	1	16-Bits	0.0030%	-55 to +125	20-pin 0.3" CerDIP
CS5508-BP	1	20-Bits	0.0015%	-40 to +85	20-pin 0.3" Plastic DIP
CS5508-BS	1	20-Bits	0.0015%	-40 to +85	20-pin 0.3" SOIC
CS5508-SD	1	20-Bits	0.0030%	-55 to +125	20-pin 0.3" CerDIP

APPENDIX

The following companies provide 32.768 kHz crystals in many package varieties and temperature ranges.

Fox Electronics
5570 Enterprise Parkway
Fort Meyers, FL 33905
(813) 693-0099

Micro Crystal Division / SMH
702 West Algonquin Road
Arlington Heights, IL 60005
(708) 806-1485

SaRonix
4010 Transport Street
Palo Alto, California 94303
(415) 856-6900

Statek
512 North Main
Orange, California 92668
(714) 639-7810

IQD Ltd.
North Street
Crewkerne
Somerset TA18 7AK
England
01460 77155

Mr. Pierre Hersberger
Microcrystal/DIV. ETA S.A.
Schild-Rust-Strasse 17
Grenchen CH-2540
Switzerland
065 53 05 57

Taiwan X'tal Corp.
5F. No. 16, Sec 2, Chung Yang S. RD.
Reitou, Taipei, Taiwan R. O. C.
Tel: 02-894-1202
Fax: 02-895-6207

Interquip Limited
24/F Million Fortune Industrial Centre
34-36 Chai Wan Kok Street, Tsuen Wan N T
Tel: 4135515
Fax: 4137053

S& T Enterprises, Ltd.
Rm 404 Blk B
Sea View Estate
North Point, Hong Kong
Tel: 5784921
Fax: 8073126

Mr. Darren Mcleod
Hy-Q International Pty. Ltd.
12 Rosella Road,
FRANKSON, 3199
Victoria, Australia
Tel: 61-3-783 9611
Fax: 61-3-783 9703

Semiconductor Corporation

CDB5505 CDB5506 CDB5507 CDB5508

Evaluation Board for CS5505/6/7/8 Series of ADC's

Features

- Operation with on-board 32.768 kHz crystal or off-board clock source
- Jumper selectable: SSC mode; SEC mode; Sleep
- DIP Switch Selectable: BP/$\overline{UP}$ mode; A0, & A1 channel selection
- On-board precision voltage reference
- Access to all digital control pins
- On-board patch area

General Description

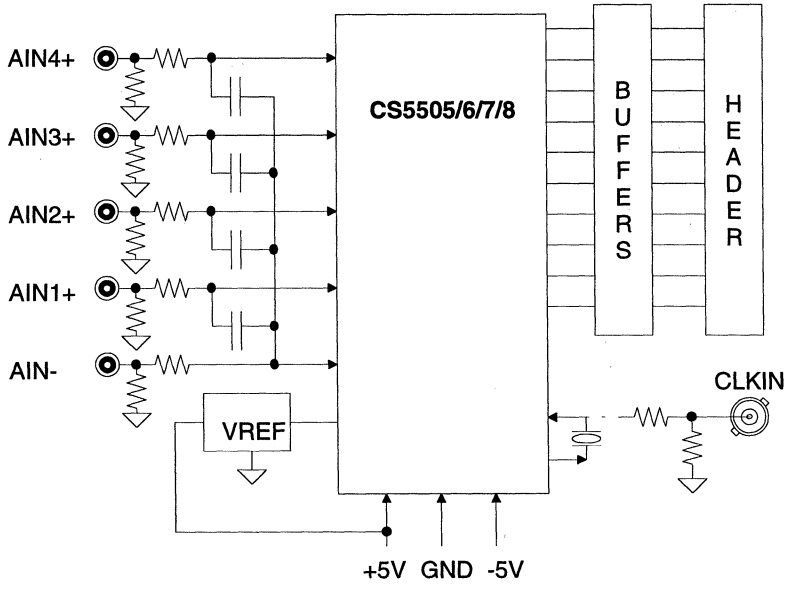
The CDB5505/5506/5507/5508 is a circuit board designed to provide quick evaluation of the CS5505/6/7/8 series of A/D converters. The board can be configured to evaluate the CS5505/6/7/8 in either SSC (Synchronous Self-Clocking) or SEC (Synchronous External-Clocking) serial port mode.

The board allows access to all of the digital interface pins of the CS5505/6/7/8 chip.

ORDERING INFORMATION

CDB5505 CDB5506

CDB5507 CDB5508



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Introduction

The CDB5505/6/7/8 evaluation board provides a quick means of testing the CS5505/6/7/8 series A/D converters. The CS5505/6/7/8 converters require a minimal amount of external circuitry. The evaluation board comes configured with the A/D converter chip operating from a 32.768 kHz crystal and with an off-chip precision 2.5 volt reference. The board provides access to all of the digital interface pins of the CS5505/6/7/8 chip.

The board is configured for operation from +5 and -5 volt power supplies, but can be operated from a single +5 volt supply if the -5V binding post is shorted to the GND binding post.

Evaluation Board Overview

The board provides a complete means of making the CS5505/6/7/8 A/D converter chip function. The user must provide a means of taking the output data from the board in serial format and using it in his system.

Figure 1 illustrates the schematic for the board. The board comes configured for the A/D converter chip to operate from the 32.768 kHz watch crystal. A BNC connector for an external clock is provided on the board. To connect the external BNC source to the converter chip, a circuit trace must be cut. Then a jumper must be inserted in the proper holes to connect the XIN pin of the converter to the input line from the BNC. The BNC input is terminated with a 50Ω resistor. Remove this resistor if driving from a logic gate. See the schematic in Figure 1.

The board comes with the A/D converter VREF+ and VREF- pins hard-wired to the 2.5 volt bandgap voltage reference IC on the board. The VREF+ and VREF- pins can be connected to either the on chip reference or an off-board reference if the connections (2A and 2B) to the bandgap IC are cut.

Note that the pin-out of the CS5505/6/7/8 series chips allows the 20-pin single channel devices to be plugged into the 24-pin, four channel footprint. See Figure 2 which illustrates the footprint compatibility.

Prior to powering up the board, select the serial port operating mode with the appropriate jumper on the M/SLP header. The device can be operated in either the SSC (Synchronous Self-Clocking) or the SEC (Synchronous External Clocking) mode. See the device data sheet for an explanation of these modes.

All of the control pins of the CS5505/6/7/8 are available at the J1 header connector. Buffer ICs U2 and U3 are used to buffer the converter for interface to off-board circuits. The buffers are used on the evaluation board only because the exact loading and off-board circuitry is unknown. Most applications will not require the buffer ICs for proper operation.

To put the board in operation, select either bipolar or unipolar mode with DIP switch S2. Then press the CAL pushbutton after the board is powered up. This initiates calibration of the converter which is required before measurements can be taken.

To select an input channel on the four channel devices, use DIP switch S2 to select the inputs for A0 and A1 (see Table 1). Once A0 and A1 are selected, the CONV switch (S2-3) must be switched on (closed) and then open to cause the

A1	A0	Channel addressed
0	0	AIN1
0	1	AIN2
1	0	AIN3
1	1	AIN4

Table 1. Multiplexer Truth Table

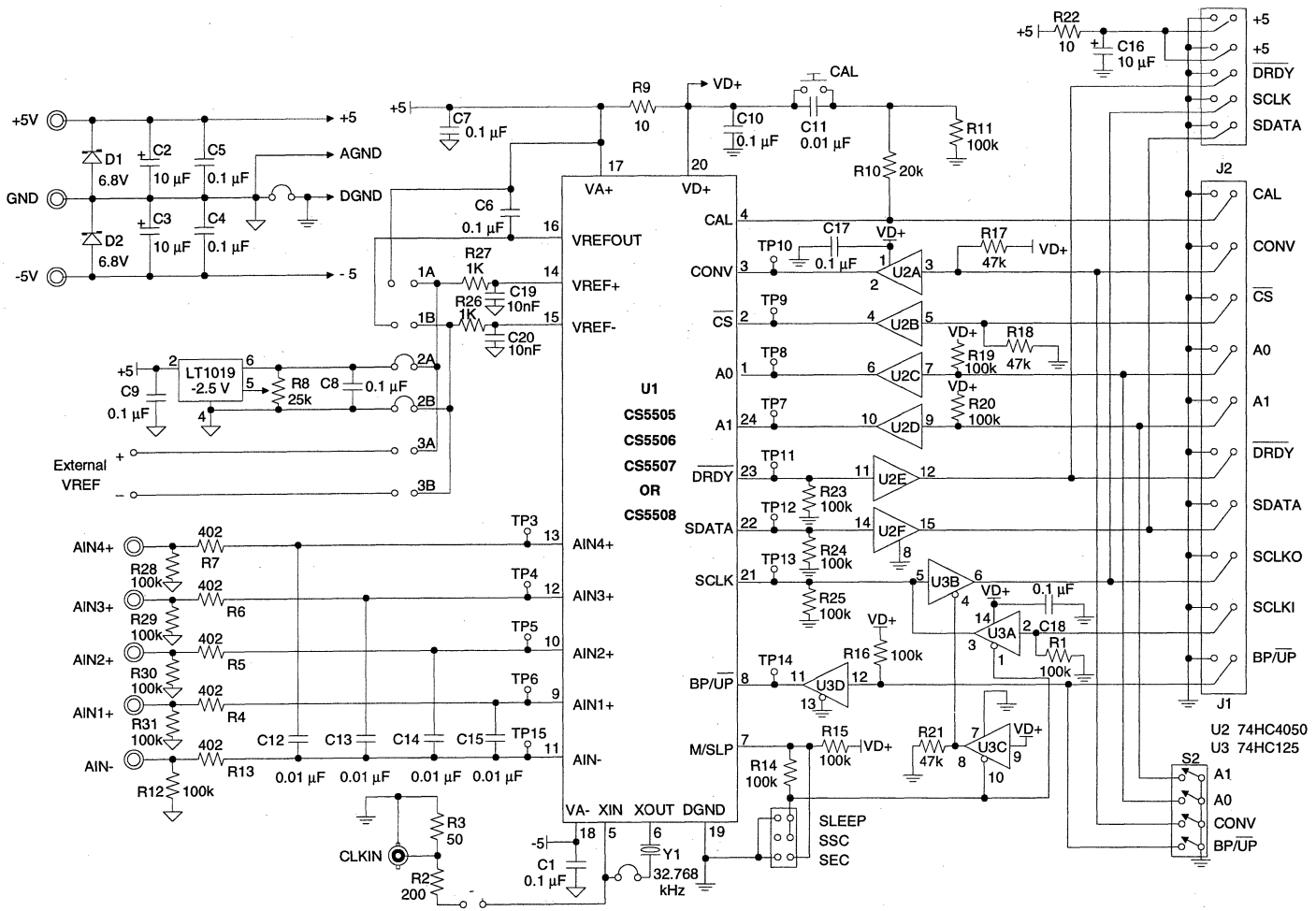


Figure 1. ADC Connections

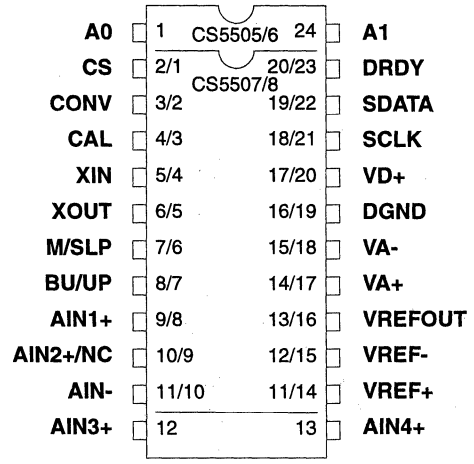


Figure 2. CS5505/6 and CS5507/8 Pin Layouts

CONV signal to transition low to high. This latches the A0 and A1 channel selection into the converter. With CONV high (S2-3 open) the converter will convert continuously.

Figures 3 and 4 illustrate the evaluation board layout while Figure 5 illustrates the component placement (silkscreen) of the evaluation board.

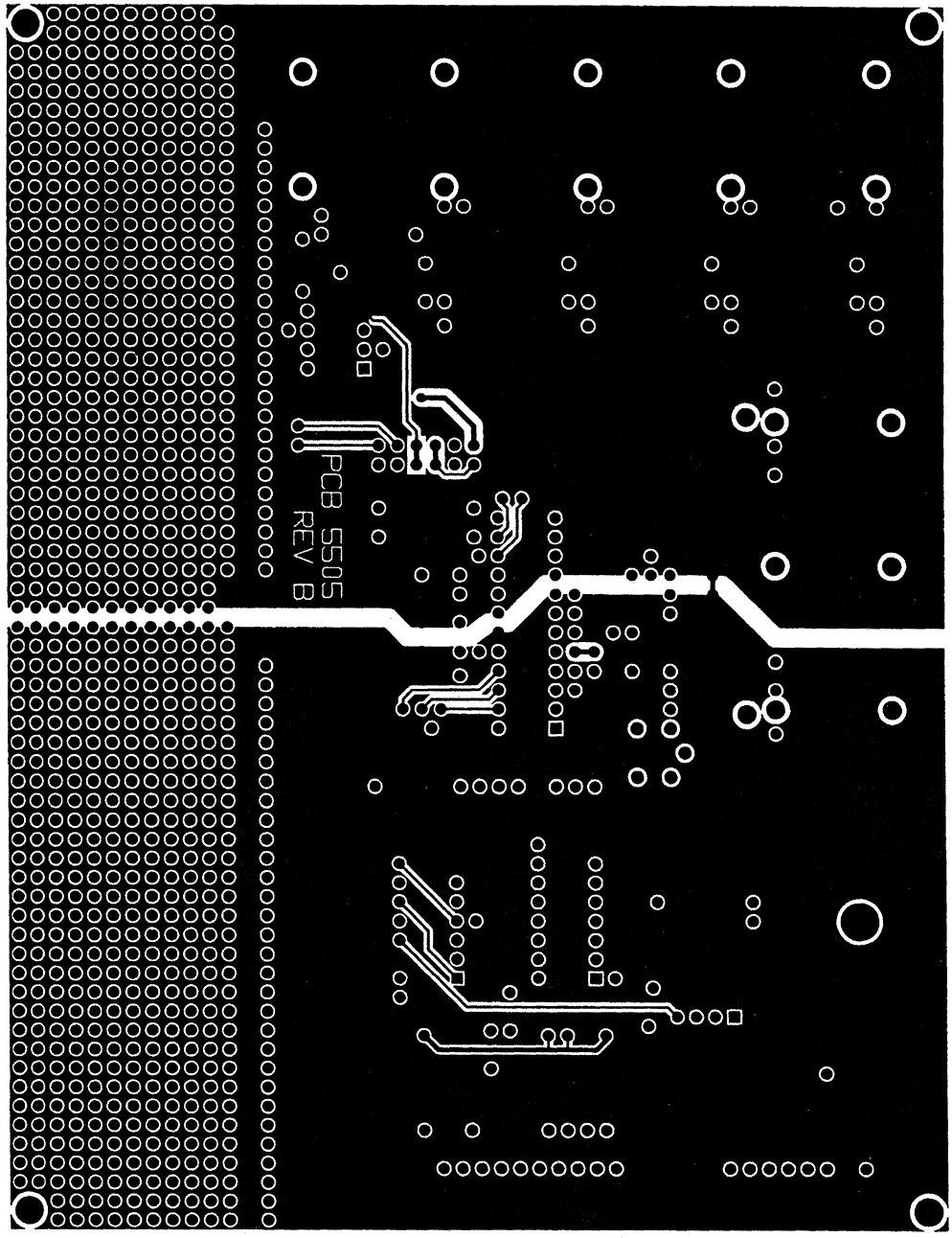


Figure 3. Top Ground Plane Layer (NOT TO SCALE)

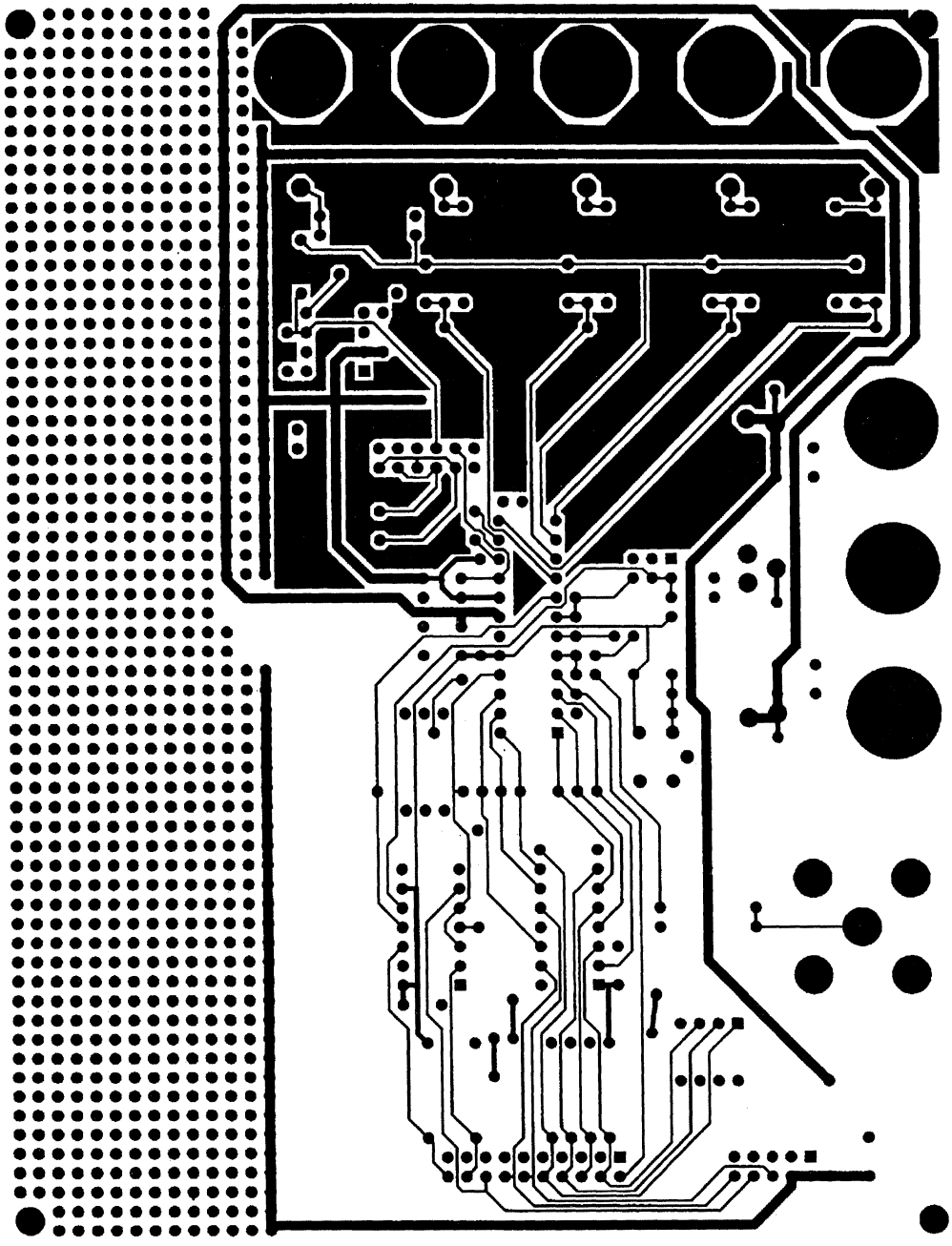


Figure 4. Bottom Trace Layer (NOT TO SCALE)

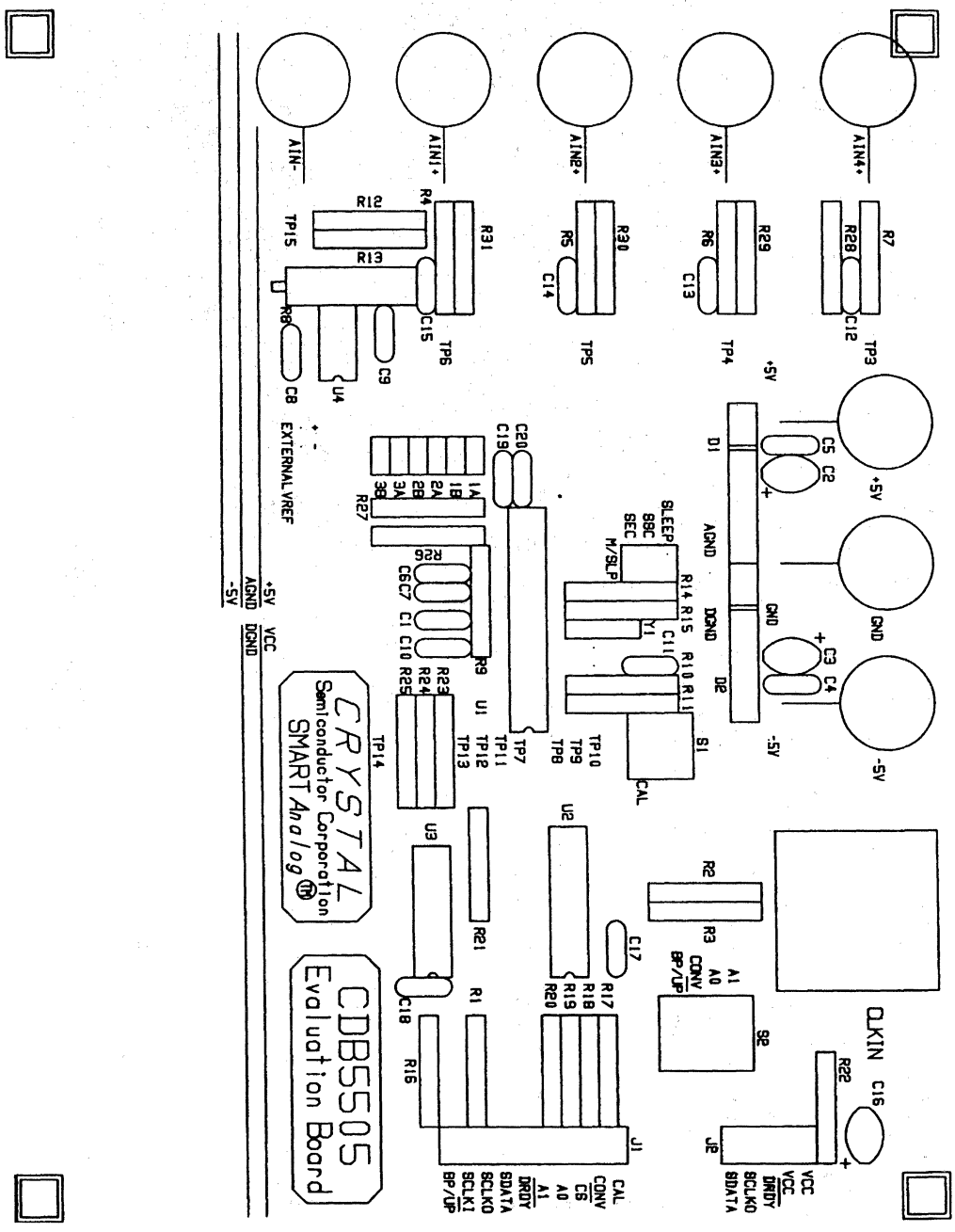


Figure 5. Silk Screen Layer (NOT TO SCALE)

Semiconductor Corporation

CS5509

Single Supply, 16-Bit A/D Converter

Features

- Delta-Sigma A/D Converter
  - 16-bit No Missing Codes
  - Linearity Error: ±0.0015%FS
- Differential Input
  - Pin Selectable Unipolar/Bipolar Ranges
  - Common Mode Rejection
    105 dB @ dc
    120 dB @ 50, 60 Hz
- Either 5V or 3.3V Digital Interface
- On-chip Self-Calibration Circuitry
- Output Update Rates up to 200/second
- Ultra Low Power: 1.7 mW

General Description

The CS5509 is a single supply, 16-bit, serial-output CMOS A/D converter. The CS5509 uses charge-balanced (delta-sigma) techniques to provide a low cost, high resolution measurement at output word rates up to 200 samples per second.

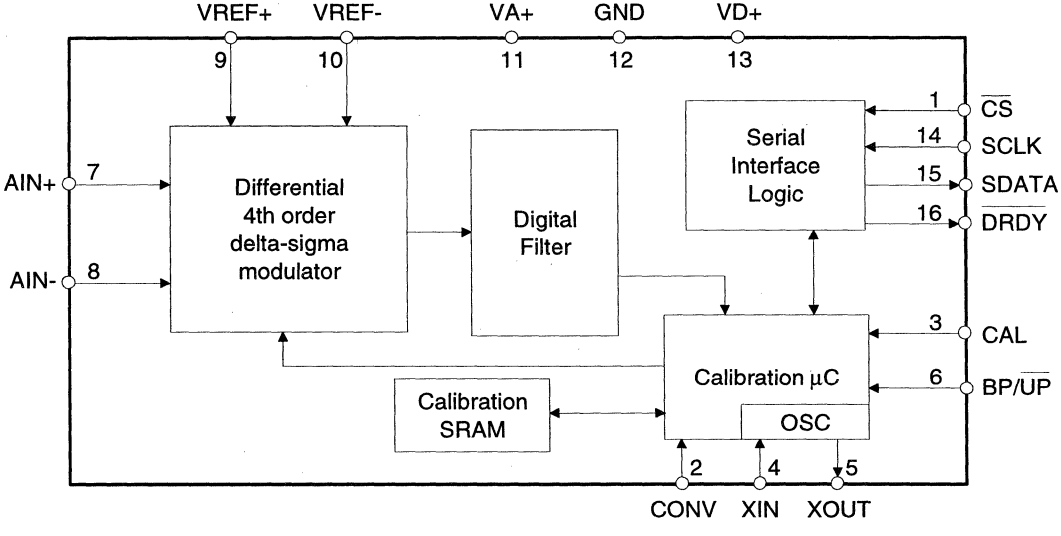
The on-chip digital filter offers superior line rejection at 50Hz and 60Hz when the device is operated from a 32.768 kHz clock (output word rate = 20 Hz.).

The CS5509 has on-chip self-calibration circuitry which can be initiated at any time or temperature to ensure minimum offset and full-scale errors.

Low power, high resolution and small package size make the CS5509 an ideal solution for loop-powered transmitters, panel meters, weigh scales and battery powered instruments.

ORDERING INFORMATION:

CS5509-AP	-40°C to +85°C	16-pin PDIP
CS5509-AS	-40°C to +85°C	16-pin SOIC



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

ANALOG CHARACTERISTICS (T_A = 25°C; VA+ = 5V ± 10%; VD+ = 3.3V ± 5%; VREF+ = 2.5V, VREF- = 0V; f_{CLK} = 330kHz; Bipolar Mode; R_{source} = 50Ω with a 10nF to GND at AIN; AIN- = 2.5V; unless otherwise specified.) (Notes 1, 2)

Parameter*			Min	Typ	Max	Units
Accuracy						
Linearity Error	f_{CLK} = 32.768 kHz		-	0.0015	0.003	±%FS
	f_{CLK} = 165 kHz		-	0.0015	0.003	±%FS
	f_{CLK} = 247.5 kHz		-	0.0015	0.003	±%FS
	f_{CLK} = 330 kHz		-	0.005	0.0125	±%FS
Differential Nonlinearity			-	±0.25	±0.5	LSB
Full Scale Error		(Note 3)	-	±0.25	±2	LSB
Full Scale Drift		(Note 4)	-	±0.5	-	LSB
Unipolar Offset		(Note 3)	-	±0.5	±2	LSB
Unipolar Offset Drift		(Note 4)	-	±0.5	-	LSB
Bipolar Offset		(Note 3)	-	±0.25	±1	LSB
Bipolar Offset Drift		(Note 4)	-	±0.25	-	LSB
Noise (Referred to Output)			-	0.16	-	LSB_{rms}
Analog Input						
Analog Input Range:	Unipolar		-	0 to +2.5	-	Volts
	Bipolar	(Note 5, 6)	-	±2.5	-	Volts
Common Mode Rejection:	dc		-	105	-	dB
f_{CLK} = 32.768kHz	50,60 Hz	(Note 2)	120	-	-	dB
Input Capacitance			-	15	-	pF
DC Bias Current		(Note 1)	-	5	-	nA
Power Supplies						
DC Power Supply Currents:	I_{Total}		-	360	450	µA
	I_{Analog}		-	300	-	µA
	$I_{Digital}$		-	60	-	µA
Power Dissipation		(Note 7)	-	1.7	2.25	mW
Power Supply Rejection			-	80	-	dB

Notes:
1. Both source resistance and shunt capacitance are critical in determining the CS5509's source impedance requirements. Refer to the text section *Analog Input Impedance Considerations.*
2. Specifications guaranteed by design, characterization and/or test.
3. Applies after calibration at the temperature of interest.
4. Total drift over the specified temperature range since calibration at power-up at 25°C.
5. The input is differential. Therefore, GND ≤ Signal + Common Mode Voltage ≤ VA+.
6. The CS5509 can accept input voltages up to the VA+ analog supply. In unipolar mode the CS5509 will output all 1's if the dc input magnitude ((AIN+)-(AIN-)) exceeds ((VREF+)-(VREF-)) and will output all 0's if the input becomes more negative than 0 Volts. In bipolar mode the CS5509 will output all 1's if the dc input magnitude ((AIN+)-(AIN-)) exceeds ((VREF+)-(VREF-)) and will output all 0's if the input becomes more negative in magnitude than -((VREF+)-(VREF-)).
7. All outputs unloaded. All inputs CMOS levels.

* Refer to the Specification Definitions immediately following the Pin Description Section.

Specifications are subject to change without notice.

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Units
Modulator Sampling Frequency	f_S	$f_{clk}/2$	Hz
Output Update Rate (CONV = 1)	f_{out}	$f_{clk}/1622$	Hz
Filter Corner Frequency	f_{-3dB}	$f_{clk}/1928$	Hz
Settling Time to 1/2 LSB (FS Step)	t_s	$1/f_{out}$	s

5V DIGITAL CHARACTERISTICS (T_A = 25°C; VA+, VD+ = 5V ± 10%; GND = 0.)

(Notes 2, 8)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage: XIN	V_{IH}	3.5	-	-	V
All Pins Except XIN	V_{IH}	2.0	-	-	V
Low-Level Input Voltage: XIN	V_{IL}	-	-	1.5	V
All Pins Except XIN	V_{IL}	-	-	0.8	V
High-Level Output Voltage (Note 9)	V_{OH}	(VD+)-1.0	-	-	V
Low-Level Output Voltage I_{out} = 1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	±1	±10	µA
3-State Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

Notes: 8. All measurements are performed under static conditions.

9. I_{out} = -100 µA. This guarantees the ability to drive one TTL load. (V_{OH} = 2.4V @ I_{out} = -40 µA).

3.3V DIGITAL CHARACTERISTICS (T_A = 25°C; VA+ = 5V ± 10%; VD+ = 3.3V ± 5%; GND = 0.)

(Notes 2, 8)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage: XIN	V_{IH}	0.7VD+	-	-	V
All Pins Except XIN	V_{IH}	0.6VD+	-	-	V
Low-Level Input Voltage: XIN	V_{IL}	-	-	0.3VD+	V
All Pins Except XIN	V_{IL}	-	-	0.16VD+	V
High-Level Output Voltage I_{out} = -400µA	V_{OH}	(VD+)-0.3	-	-	V
Low-Level Output Voltage I_{out} = 400µA	V_{OL}	-	-	0.3	V
Input Leakage Current	I_{in}	-	±1	±10	µA
3-State Leakage Current	I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance	C_{out}	-	9	-	pF

5V SWITCHING CHARACTERISTICS (T_A = 25°C; VA+, VD+ = 5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF.) (Note 2)

Parameter			Symbol	Min	Typ	Max	Units
Master Clock Frequency	Internal Oscillator:		XIN	30.0	32.768	53.0	kHz
	External Clock:		f_{clk}	30	-	330	kHz
Master Clock Duty Cycle				40	-	60	%
Rise Times:	Any Digital Input	(Note 10)	t_{rise}	-	-	1.0	µs
	Any Digital Output			-	50	-	ns
Fall Times:	Any Digital Input	(Note 10)	t_{fall}	-	-	1.0	µs
	Any Digital Output			-	20	-	ns
Start-Up							
Power-On Reset Period		(Note 11)	t_{res}	-	10	-	ms
Oscillator Start-up Time	XTAL=32.768 kHz	(Note 12)	t_{osu}	-	500	-	ms
Wake-up Period		(Note 13)	t_{wup}	-	$1800/f_{clk}$	-	s
Calibration							
CONV Pulse Width (CAL=1)		(Note 14)	t_{ccw}	100	-	-	ns
CONV and CAL High to Start of Calibration			t_{scl}	-	-	$2/f_{clk}$+200	ns
Start of Calibration to End of Calibration			t_{cal}	-	$3246/f_{clk}$	-	s
Conversion							
CONV Pulse Width			t_{cpw}	100	-	-	ns
CONV High to Start of Conversion			t_{scn}	-	-	$2/f_{clk}$+200	ns
Set Up Time	BP/$\overline{UP}$ stable prior to $\overline{DRDY}$ falling		t_{bus}	$82/f_{clk}$	-	-	s
Hold Time	BP/$\overline{UP}$ stable after $\overline{DRDY}$ falls		t_{buh}	0	-	-	ns
Start of Conversion to End of Conversion		(Note 15)	t_{con}	-	$1624/f_{clk}$	-	s

Notes: 10. Specified using 10% and 90% points on waveform of interest.
11. An internal power-on-reset is activated whenever power is applied to the device.
12. Oscillator start-up time varies with the crystal parameters. This specification does not apply when using an external clock source.
13. The wake-up period begins once the oscillator starts; or when using an external f_{clk}, after the power-on reset time elapses.
14. Calibration can also be initiated by pulsing CAL high while CONV=1.
15. Conversion time will be $1622/f_{clk}$ if CONV remains high continuously.

3.3V SWITCHING CHARACTERISTICS (T_A = 25°C; VA+ = 5V ± 10%; VD+ = 3.3V ± 5%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF.) (Note 2)

Parameter			Symbol	Min	Typ	Max	Units
Master Clock Frequency	Internal Oscillator: External Clock:		XIN f_{clk}	30.0 30	32.768 -	53.0 330	kHz kHz
Master Clock Duty Cycle				40	-	60	%
Rise Times:	Any Digital Input Any Digital Output	(Note 10)	t_{rise}	- -	- 50	1.0 -	µs ns
Fall Times:	Any Digital Input Any Digital Output	(Note 10)	t_{fall}	- -	- 20	1.0 -	µs ns
Start-Up							
Power-On Reset Period		(Note 11)	t_{res}	-	10	-	ms
Oscillator Start-up Time	XTAL=32.768 kHz	(Note 12)	t_{osu}	-	500	-	ms
Wake-up Period		(Note 13)	t_{wup}	-	$1800/f_{clk}$	-	s
Calibration							
CONV Pulse Width (CAL=1)		(Note 14)	t_{ccw}	100	-	-	ns
CONV and CAL High to Start of Calibration			t_{scl}	-	-	$2/f_{clk}+200$	ns
Start of Calibration to End of Calibration			t_{cal}	-	$3246/f_{clk}$	-	s
Conversion							
CONV Pulse Width			t_{cpw}	100	-	-	ns
CONV High to Start of Conversion			t_{scn}	-	-	$2/f_{clk}+200$	ns
Set Up Time	BP/$\overline{UP}$ stable prior to $\overline{DRDY}$ falling		t_{bus}	$82/f_{clk}$	-	-	s
Hold Time	BP/$\overline{UP}$ stable after $\overline{DRDY}$ falls		t_{buh}	0	-	-	ns
Start of Conversion to End of Conversion		(Note 15)	t_{con}	-	$1624/f_{clk}$	-	s

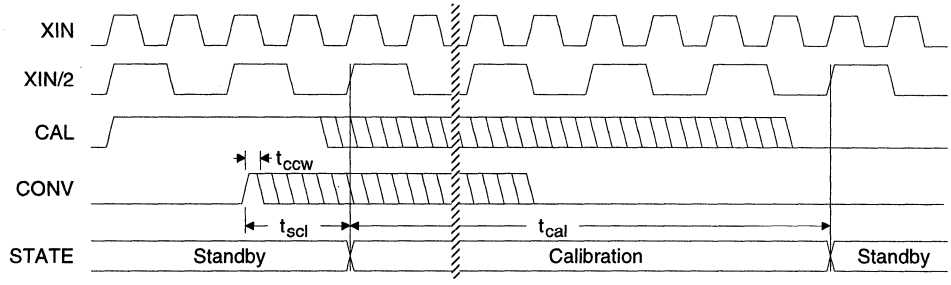


Figure 1. Calibration Timing (Not to Scale)

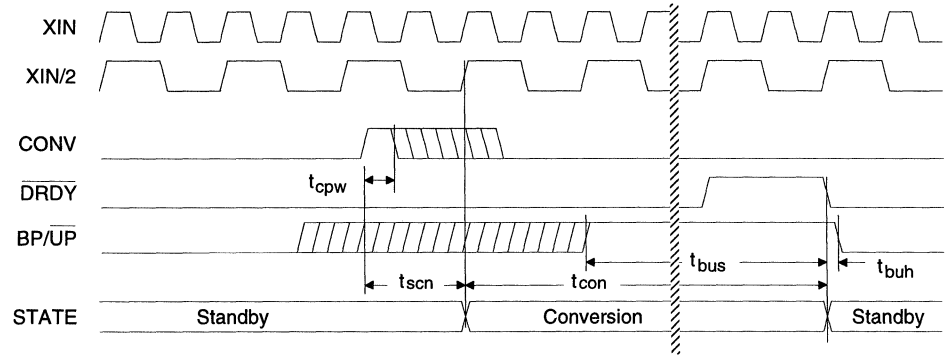


Figure 2. Conversion Timing (Not to Scale)

5V SWITCHING CHARACTERISTICS (T_A = 25°C; VA+, VD+ = 5V ± 10%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF.) (Note 2)

Parameter		Symbol	Min	Typ	Max	Units
Serial Clock		f_{sclk}	0	-	2.5	MHz
Serial Clock	Pulse Width High	t_{ph}	200	-	-	ns
	Pulse Width Low	t_{pl}	200	-	-	ns
Access Time:	$\overline{CS}$ Low to data valid (Note 16)	t_{csd}	-	60	200	ns
Maximum Delay Time:	SCLK falling to new SDATA bit (Note 17)	t_{dd}	-	150	310	ns
Output Float Delay	$\overline{CS}$ High to output Hi-Z (Note 18)	t_{fd1}	-	60	150	ns
	SCLK falling to Hi-Z	t_{fd2}	-	160	300	ns

Notes: 16. If $\overline{CS}$ is activated asynchronously to $\overline{DRDY}$, $\overline{CS}$ will not be recognized if it occurs when $\overline{DRDY}$ is high for 2 clock cycles. The propagation delay time may be as great as 2 f_{clk} cycles plus 200 ns. To guarantee proper clocking of SDATA when using asynchronous $\overline{CS}$, SCLK(i) should not be taken high sooner than 2 f_{clk} + 200 ns after $\overline{CS}$ goes low.

17. SDATA transitions on the falling edge of SCLK. Note that a rising SCLK must occur to enable the serial port shifting mechanism before falling edges can be recognized.

18. If $\overline{CS}$ is returned high before all data bits are output, the SDATA output will complete the current data bit and then go to high impedance.

3.3V SWITCHING CHARACTERISTICS (T_A = 25°C; VA+ = 5V ± 10%, VD+ = 3.3V ± 5%; Input Levels : Logic 0 = 0V, Logic 1 = VD+; C_L = 50pF.) (Note 2)

Parameter		Symbol	Min	Typ	Max	Units
Serial Clock		f_{sclk}	0	-	1.25	MHz
Serial Clock	Pulse Width High	t_{ph}	200	-	-	ns
	Pulse Width Low	t_{pl}	200	-	-	ns
Access Time:	$\overline{CS}$ Low to data valid (Note 16)	t_{csd}	-	100	200	ns
Maximum Delay Time:	SCLK falling to new SDATA bit (Note 17)	t_{dd}	-	400	600	ns
Output Float Delay	$\overline{CS}$ High to output Hi-Z (Note 18)	t_{fd1}	-	70	150	ns
	SCLK falling to Hi-Z	t_{fd2}	-	320	500	ns

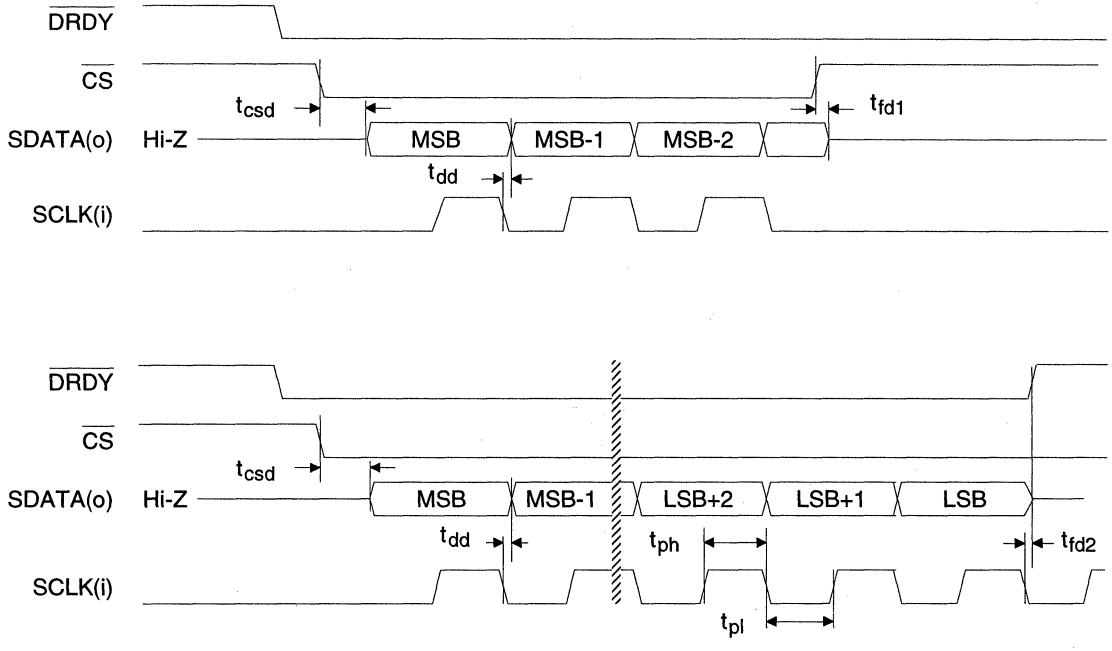


Figure 3. Timing Relationships (Not to Scale)

RECOMMENDED OPERATING CONDITIONS (DGND = 0V) (Note 19)

Parameter	Symbol	Min	Typ	Max	Units
DC Power Supplies: Positive Digital	VD+	3.15	5.0	5.5	V
Positive Analog	VA+	4.5	5.0	5.5	V
Analog Reference Voltage (Note 20)	(VREF+)-(VREF-)	1.0	2.5	3.6	V
Analog Input Voltage: (Note 6)					
Unipolar	VAIN	0	-	(VREF+)-(VREF-)	V
Bipolar	VAIN	-((VREF+)-(VREF-))	-	(VREF+)-(VREF-)	V

Notes: 19. All voltages with respect to ground.
20. The CS5509 can be operated with a reference voltage as low as 100 mV; but with a corresponding reduction in noise-free resolution. The common mode voltage of the voltage reference may be any value as long as +VREF and -VREF remain inside the supply values of VA+ and GND.

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies: Ground (Note 21)		GND	-0.3	-	(VD+)-0.3	V
Positive Digital (Note 22)		VD+	-0.3	-	6.0	V
Positive Analog		VA+	-0.3	-	6.0	V
Input Current, Any Pin Except Supplies (Notes 23 & 24)		I_{in}	-	-	±10	mA
Output Current		I_{out}	-	-	±25	mA
Power Dissipation (Total) (Note 25)			-	-	500	mW
Analog Input Voltage AIN and VREF pins		V_{INA}	-0.3	-	(VA+)+0.3	V
Digital Input Voltage		V_{IND}	-0.3	-	(VD+)+0.3	V
Ambient Operating Temperature		T_A	-40	-	85	°C
Storage Temperature		T_{stg}	-65	-	150	°C

Notes: 21. No pin should go more positive than (VA+)+0.3V.
22. VD+ must always be less than (VA+)+0.3V, and can never exceed +6.0 V.
23. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pin.
24. Transient currents of up to 100mA will not cause SCR latch-up. Maximum input current for a power supply pin is ± 50 mA.
25. Total power dissipation, including all input currents and output currents.

* WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

GENERAL DESCRIPTION

The CS5509 is a low power, 16-bit, monolithic CMOS A/D converter designed specifically for measurement of dc signals. The CS5509 includes a delta-sigma charge-balance converter, a voltage reference, a calibration microcontroller with SRAM, a digital filter and a serial interface.

The CS5509 is optimized to operate from a 32.768 kHz crystal but can be driven by an external clock whose frequency is between 30 kHz and 330 kHz. When the digital filter is operated with a 32.768 kHz clock, the filter has zeros precisely at 50 and 60 Hz line frequencies and multiples thereof.

The CS5509 uses a "start convert" command to start a convolution cycle on the digital filter. Once the filter cycle is completed, the output port is updated. When operated with a 32.768 kHz clock the ADC converts and updates its output port at 20 samples/sec. The output port operates in a synchronous externally-clocked interface format.

THEORY OF OPERATION

Basic Converter Operation

The CS5509 A/D converter has three operating states. These are stand-by, calibration, and conversion. When power is first applied, an internal power-on reset delay of about 10 ms resets all of the logic in the device. The oscillator must then begin oscillating before the device can be considered functional. After the power-on reset is applied, the device enters the wake-up period for 1800 clock cycles after clock is present. This allows the delta-sigma modulator and other circuitry (which are operating with very low currents) to reach a stable bias condition prior to entering into either the calibration or conversion states. During the 1800 cycle wake-up period, the device can accept an input command. Execution of this command will not occur until the complete wake-up period elapses. If no command is given, the device enters the standby state.

Calibration

After the initial application of power, the CS5509 must enter the calibration state prior to performing accurate conversions. During calibration, the chip executes a two-step process. The device first performs an offset calibration and then follows this with a gain calibration. The two calibration steps determine the zero reference point and the full scale reference point of the converter's transfer function. From these points it calibrates the zero point and a gain slope to be used to properly scale the output digital codes when doing conversions.

The calibration state is entered whenever the CAL and CONV pins are high at the same time. The state of the CAL and CONV pins at power-on are recognized as commands, but will not be executed until the end of the 1800 clock cycle wake-up period.

If CAL and CONV become active (high) during the 1800 clock cycle wake-up time, the converter will wait until the wake-up period elapses before executing the calibration. If the wake-up time has elapsed, the converter will be in the standby mode waiting for instruction and will enter the calibration cycle immediately if CAL and CONV become active. The calibration lasts for 3246 clock cycles. Calibration coefficients are then retained in the SRAM (static RAM) for use during conversion.

The state of BP/$\overline{UP}$ is ignored during calibration but should remain stable throughout the calibration period to minimize noise.

When conversions are performed in unipolar mode or in bipolar mode, the converter uses the same calibration factors to compute the digital

output code. The only difference is that in bipolar mode the on-chip microcontroller offsets the computed output word by a code value of 8000H. This means that the bipolar measurement range is not calibrated from full scale positive to full scale negative. Instead it is calibrated from the bipolar zero scale point to full scale positive. The slope factor is then extended below bipolar zero to accommodate the negative input signals. The converter can be used to convert both unipolar and bipolar signals by changing the BP/$\overline{UP}$ pin. Recalibration is not required when switching between unipolar and bipolar modes.

At the end of the calibration cycle, the on-chip microcontroller checks the logic state of the CONV signal. If the CONV input is low the device will enter the standby mode where it waits for further instruction. If the CONV signal is high at the end of the calibration cycle, the converter will enter the conversion state and perform a conversion on the input channel. The CAL signal can be returned low any time after calibration is initiated. CONV can also be returned low, but it should never be taken low and then taken back high until the calibration period has ended and the converter is in the standby state. If CONV is taken low and then high again with CAL high while the converter is calibrating, the device will interrupt the current calibration cycle and start a new one. If CAL is taken low and CONV is taken low and then high during calibration, the calibration cycle will continue as the conversion command is disregarded. The state of BP/$\overline{UP}$ is not important during calibrations.

If an "end of calibration" signal is desired, pulse the CAL signal high while leaving the CONV signal high continuously. Once the calibration is completed, a conversion will be performed. At the end of the conversion, $\overline{DRDY}$ will fall to indicate the first valid conversion after the calibration has been completed.

Conversion

The conversion state can be entered at the end of the calibration cycle, or whenever the converter is idle in the standby mode. If CONV is taken high to initiate a calibration cycle (CAL also high), and remains high until the calibration cycle is completed (CAL is taken low after CONV transitions high), the converter will begin a conversion upon completion of the calibration period.

The BP/$\overline{UP}$ pin is not a latched input. The BP/$\overline{UP}$ pin controls how the output word from the digital filter is processed. In bipolar mode the output word computed by the digital filter is offset by 8000H (see Understanding Converter Calibration). BP/$\overline{UP}$ can be changed after a conversion is started as long as it is stable for 82 clock cycles of the conversion period prior to $\overline{DRDY}$ falling. If one wishes to intermix measurement of bipolar and unipolar signals on various input signals, it is best to switch the BP/$\overline{UP}$ pin immediately after $\overline{DRDY}$ falls and leave BP/$\overline{UP}$ stable until $\overline{DRDY}$ falls again.

The digital filter in the CS5509 has a Finite Impulse Response and is designed to settle to full accuracy in one conversion time.

If CONV is left high, the CS5509 will perform continuous conversions. The conversion time will be 1622 clock cycles. If conversion is initiated from the standby state, there may be up to two XIN clock cycles of uncertainty as to when conversion actually begins. This is because the internal logic operates at one half the external clock rate and the exact phase of the internal clock may be 180° out of phase relative to the XIN clock. When a new conversion is initiated from the standby state, it will take up to two XIN clock cycles to begin. Actual conversion will use 1624 clock cycles before $\overline{DRDY}$ goes low to indicate that the serial port has been updated. See the Serial Interface Logic section of

the data sheet for information on reading data from the serial port.

In the event the A/D conversion command (CONV going positive) is issued during the conversion state, the current conversion will be terminated and a new conversion will be initiated.

Voltage Reference

The CS5509 uses a differential voltage reference input. The positive input is VREF+ and the negative input is VREF-. The voltage between VREF+ and VREF- can range from 1 volt minimum to 3.6 volts maximum. The gain slope will track changes in the reference without recalibration, accommodating ratiometric applications.

Analog Input Range

The analog input range is set by the magnitude of the voltage between the VREF+ and VREF- pins. In unipolar mode the input range will equal the magnitude of the voltage reference. In bipolar mode the input voltage range will equate to plus and minus the magnitude of the voltage reference. While the voltage reference can be as great as 3.6 volts, its common mode voltage can be any value as long as the reference inputs VREF+ and VREF- stay within the supply voltages VA+ and GND. The differential input voltage can also have any common mode value as long as the maximum signal magnitude stays within the supply voltages.

The A/D converter is intended to measure dc or low frequency inputs. It is designed to yield accurate conversions even with noise exceeding the input voltage range as long as the spectral components of this noise will be filtered out by the digital filter. For example, with a 3.0 volt reference in unipolar mode, the converter will accurately convert an input dc signal up to 3.0 volts with up to 15% overrange for 60 Hz noise. A 3.0 volt dc signal could have a 60 Hz component which is 0.5 volts above the maximum input of 3.0 (3.5 volts peak; 3.0 volts dc plus 0.5 volts peak noise) and still accurately convert the input signal (XIN = 32.768 kHz). This assumes that the signal plus noise amplitude stays within the supply voltages.

Unipolar Input Voltage	Output Codes	Bipolar Input Voltage
>(VREF - 1.5 LSB)	FFFF	>(VREF - 1.5 LSB)
VREF - 1.5 LSB	FFFF / FFFE	VREF - 1.5 LSB
VREF/2 - 0.5 LSB	8000 / 7FFF	-0.5 LSB
+0.5 LSB	0001 / 0000	-VREF +0.5 LSB
<(+0.5 LSB)	0000	<(-VREF +0.5 LSB)

Note: Table excludes common mode voltage on the signal and reference inputs.

Table 1. Output Coding

The CS5509 converters output data in binary format when converting unipolar signals and in offset binary format when converting bipolar signals. Table 1 outlines the output coding for both unipolar and bipolar measurement modes.

Converter Performance

The CS5509 A/D converter has excellent linearity performance. Calibration minimizes the errors in offset and gain. The CS5509 device has no missing code performance to 16-bits. Figure 4 illustrates the DNL of the CS5509. The converter achieves Common Mode Rejection (CMR) at dc of 105 dB typical, and CMR at 50 and 60 Hz of 120 dB typical.

The CS5509 can experience some drift as temperature changes. The CS5509 uses chopper-stabilized techniques to minimize drift. Measurement errors due to offset or gain drift can be eliminated at any time by recalibrating the converter.

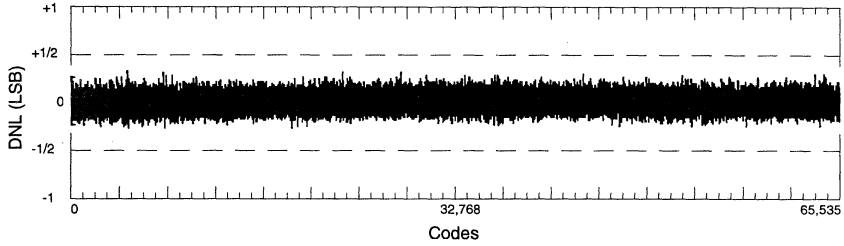


Figure 4. CS5509 Differential Nonlinearity plot.

Analog Input Impedance Considerations

The analog input of the CS5509 can be modeled as illustrated in Figure 5. Capacitors (15 pF each) are used to dynamically sample each of the inputs (AIN+ and AIN-). Every half XIN cycle the switch alternately connects the capacitor to the output of the buffer and then directly to the AIN pin. Whenever the sample capacitor is switched from the output of the buffer to the AIN pin, a small packet of charge (a dynamic demand of current) is required from the input source to settle the voltage of the sample capacitor to its final value. The voltage on the output of the buffer may differ up to 100 mV from the actual input voltage due to the offset voltage of the buffer. Timing allows one half of a XIN clock cycle for the voltage on the sample capacitor to settle to its final value.

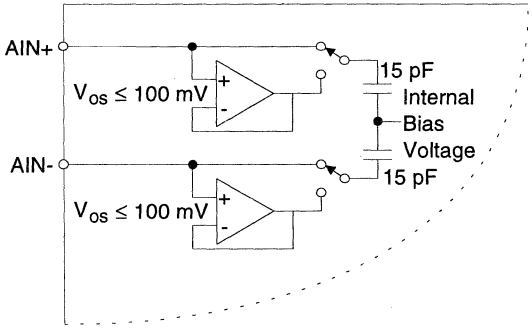


Figure 5. Analog Input Model

An equation for the maximum acceptable source resistance is derived.

$$Rs_{max} = \frac{-1}{2XIN\,(15pF + C_{EXT})\,\ln\left[\dfrac{V_e}{V_e + \dfrac{15pF(100mv)}{(15pF + C_{EXT}}}\right]}$$

This equation assumes that the offset voltage of the buffer is 100 mV, which is the worst case. The value of Ve is the maximum error voltage which is acceptable. C_{EXT} is the combination of any external or stray capacitance.

For a maximum error voltage (Ve) of 10 µV in the CS5509 (1/4LSB at 16-bits), the above equation indicates that when operating from a 32.768 kHz XIN, source resistances up to 110 kΩ are acceptable in the absence of external capacitance (C_{EXT} = 0).

The VREF+ and VREF- inputs have nearly the same structure as the AIN+ and AIN- inputs. Therefore, the discussion on analog input impedance applies to the voltage reference inputs as well.

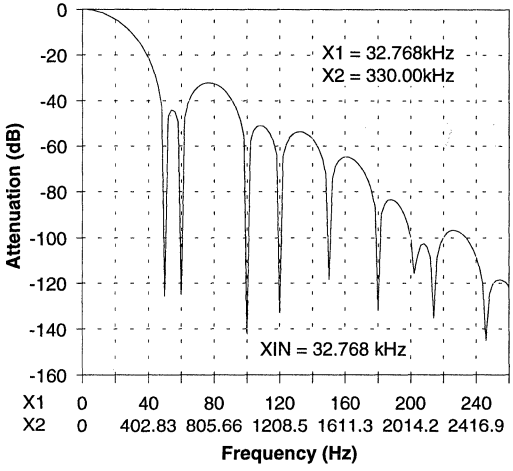


Figure 6. Filter Magnitude Plot to 260 Hz

Frequency (Hz)	Notch Depth (dB)	Frequency (Hz)	Minimum Attenuation (dB)
50	125.6	50±1%	55.5
60	126.7	60±1%	58.4
100	145.7	100±1%	62.2
120	136.0	120±1%	68.4
150	118.4	150±1%	74.9
180	132.9	180±1%	87.9
200	102.5	200±1%	94.0
240	108.4	240±1%	104.4

Table 2. Filter Notch Attenuation (XIN = 32.768 kHz)

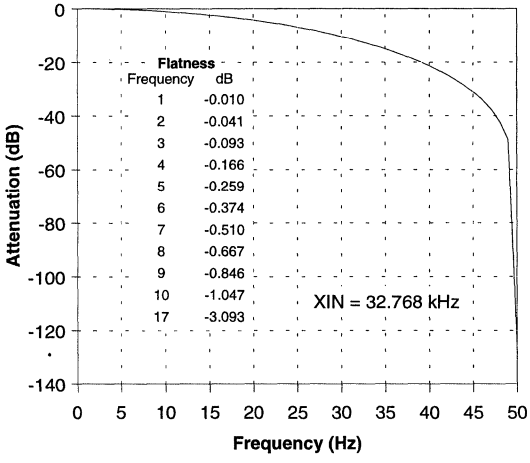


Figure 7. Filter Magnitude Plot to 50 Hz

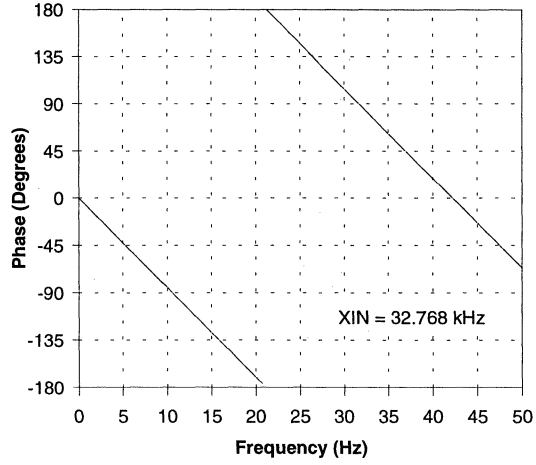


Figure 8. Filter Phase Plot to 50 Hz

Digital Filter Characteristics

The digital filter in the CS5509 is the combination of a comb filter and a low pass filter. The comb filter has zeros in its transfer function which are optimally placed to reject line interference frequencies (50 and 60 Hz and their multiples) when the CS5509 is clocked at 32.768 kHz. Figures 6, 7 and 8 illustrate the magnitude and phase characteristics of the filter.

Figure 6 illustrates the filter attenuation from dc to 260 Hz. At exactly 50, 60, 100, and 120 Hz the filter provides over 120 dB of rejection. Table 2 indicates the filter attenuation for each of the potential line interference frequencies when the converter is operating with a 32.768 kHz clock. The converter yields excellent attenuation of these interference frequencies even if the fundamental line frequency should vary ± 1% from

its specified frequency. The -3dB corner frequency of the filter when operating from a 32.768 kHz clock is 17 Hz. Figure 8 illustrates that the phase characteristics of the filter are precisely linear phase.

If the CS5509 is operated at a clock rate other than 32.768 kHz, the filter characteristics, including the comb filter zeros, will scale with the operating clock frequency. Therefore, optimum rejection of line frequency interference will occur with the CS5509 running at 32.768 kHz.

Anti-Alias Considerations for Spectral Measurement Applications

Input frequencies greater than one half the output word rate (CONV = 1) may be aliased by the converter. To prevent this, input signals should be limited in frequency to no greater than one half the output word rate of the converter (when CONV =1). Frequencies close to the modulator sample rate (XIN/2) and multiples thereof may also be aliased. If the signal source includes spectral components above one half the output word rate (when CONV = 1) these components should be removed by means of low-pass filtering prior to the A/D input to prevent aliasing. Spectral components greater than one half the output word rate on the VREF inputs (VREF+ and VREF-) may also be aliased. Filtering of the reference voltage to remove these spectral components from the reference voltage is desirable.

Crystal Oscillator

The CS5509 is designed to be operated using a 32.768 kHz "tuning fork" type crystal. One end of the crystal should be connected to the XIN input. The other end should be attached to XOUT. Short lead lengths should be used to minimize stray capacitance.

Over the industrial temperature range (-40 to +85 °C) the on-chip gate oscillator will oscillate with other crystals in the range of 30 kHz to 53 kHz. The chip will operate with external clock frequencies from 30 kHz to 330 kHz over the industrial temperature range. The 32.768 kHz crystal is normally specified as a time-keeping crystal with tight specifications for both initial frequency and for drift over temperature. To maintain excellent frequency stability, these crystals are specified only over limited operating temperature ranges (i.e. -10 °C to +60 °C) by the manufacturers. Applications of these crystals with the CS5509 does not require tight initial tolerance or low tempco drift. Therefore, a lower cost crystal with looser initial tolerance and tempco will generally be adequate for use with the CS5509. Also check with the manufacturer about wide temperature range application of their standard crystals. Generally, even those crystals specified for limited temperature range will operate over much larger ranges if frequency stability over temperature is not a requirement. The frequency stability can be as bad as ±3000 ppm over the operating temperature range and still be typically better than the line frequency (50 Hz or 60 Hz) stability over cycle-to-cycle during the course of a day.

Serial Interface Logic

The digital filter in the CS5509 takes 1624 clock cycles to compute an output word once a conversion begins. At the end of the conversion cycle, the filter will attempt to update the serial port. Two clock cycles prior to the update $\overline{\text{DRDY}}$ will go high. When $\overline{\text{DRDY}}$ goes high just prior to a port update it checks to see if the port is either empty or unselected ($\overline{\text{CS}}$ = 1). If the port is empty or unselected, the digital filter will update the port with a new output word. When new data is put into the port $\overline{\text{DRDY}}$ will go low.

Reading Serial Data

SDATA is the output pin for the serial data. When $\overline{CS}$ goes low after new data becomes available ($\overline{DRDY}$ goes low), the SDATA pin comes out of Hi-Z with the MSB data bit present. SCLK is the input pin for the serial clock. If the MSB data bit is on the SDATA pin, the first rising edge of SCLK enables the shifting mechanism. This allows the falling edges of SCLK to shift subsequent data bits out of the port. Note that if the MSB data bit is output and the SCLK signal is high, the first falling edge of SCLK will be ignored because the shifting mechanism has not become activated. After the first rising edge of SCLK, each subsequent falling edge will shift out the serial data. Once the LSB is present, the falling edge of SCLK will cause the SDATA output to go to Hi-Z and $\overline{DRDY}$ to return high. The serial port register will be updated with a new data word upon the completion of another conversion if the serial port has been emptied, or if the $\overline{CS}$ is inactive (high).

$\overline{CS}$ can be operated asynchronously to the $\overline{DRDY}$ signal. The $\overline{DRDY}$ signal need not be monitored as long as the $\overline{CS}$ signal is taken low for at least two XIN clock cycles plus 200 ns prior to SCLK being toggled. This ensures that $\overline{CS}$ has gained control over the serial port.

Power Supplies and Grounding

The analog and digital supply pins to the CS5509 are brought out on separate pins to minimize noise coupling between the analog and digital sections of the chip. In the digital section of the chip the supply current flows into the VD+ pin and out of the GND pin. As a CMOS device, the CS5509 requires that the supply voltage on the VA+ pin always be more positive than the voltage on any other pin of the device. If this requirement is not met, the device can latch-up or be damaged. In all circumstances the VA+ voltage must remain more positive than the VD+ or GND pins; VD+ must remain more positive than the GND pin.

Figure 9a illustrates the System Connection Diagram for the CS5509. Note that all supply pins are bypassed with 0.1 µF capacitors and that the VD+ digital supply is derived from the VA+ supply. Figure 9b illustrates the CS5509 operating from a +5V analog supply and +3.3V digital supply.

When using separate supplies for VA+ and VD+, VA+ must be established first. VD+ should never become more positive than VA+ under any operating condition. Remember to investigate transient power-up conditions, when one power supply may have a faster rise time.

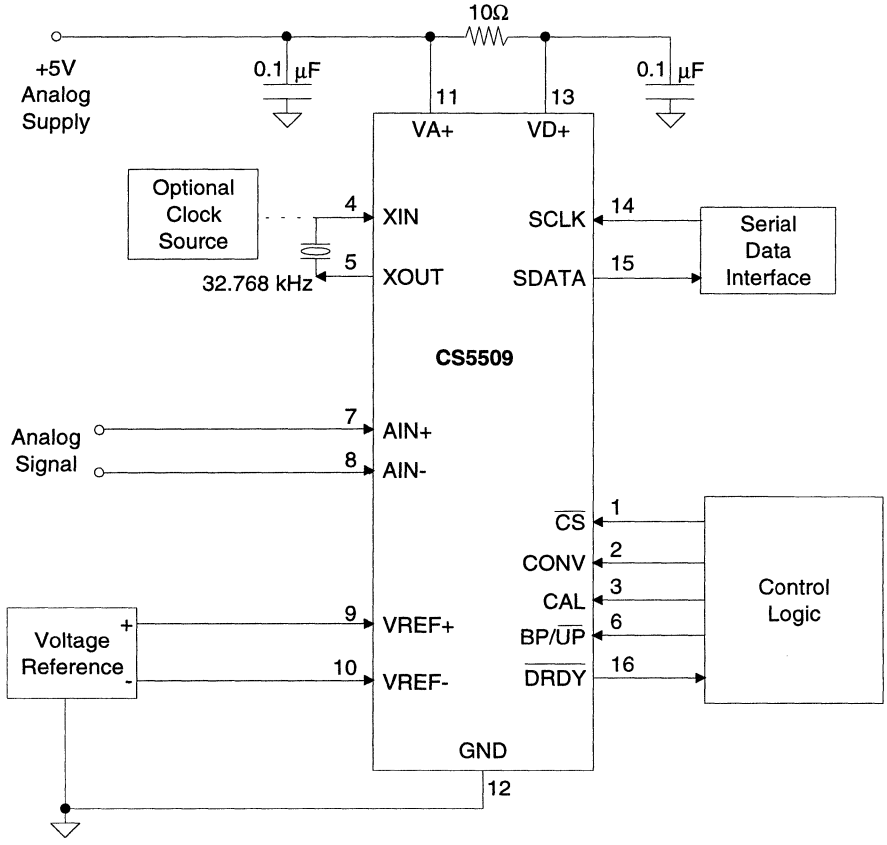


Figure 9a. System Connection Diagram Using a Single Supply

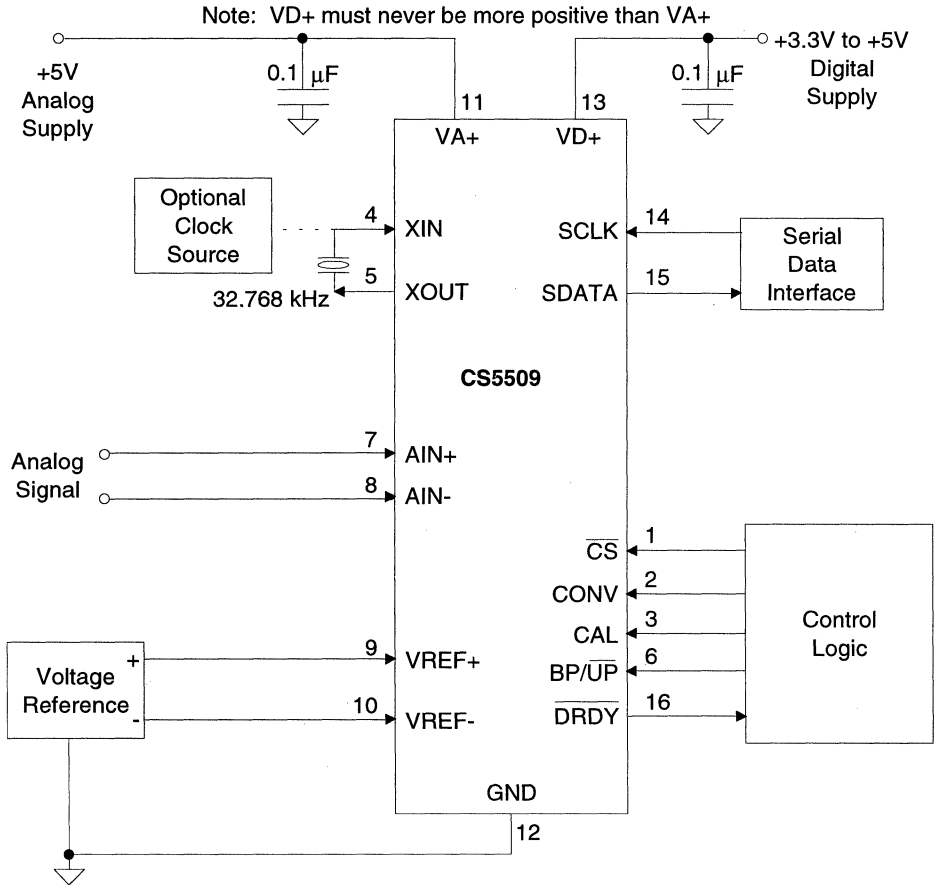
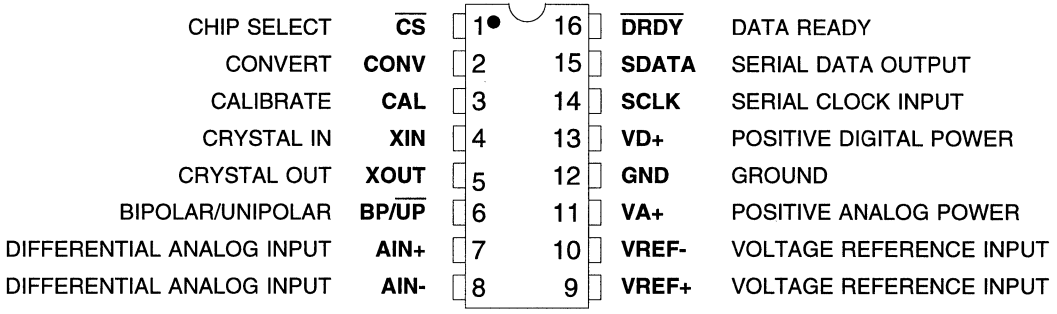


Figure 9b. System Connection Diagram Using Split Supplies

PIN DESCRIPTIONS*



*Pinout applies to both PDIP and SOIC

Clock Generator

XIN; XOUT - Crystal In; Crystal Out, Pins 4, 5.

A gate inside the chip is connected to these pins and can be used with a crystal to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock can be supplied into the XIN pin to provide the master clock for the device. Loss of clock will put the device into a lower powered state (approximately 70% power reduction).

Serial Output I/O

$\overline{\text{CS}}$ - Chip Select, Pin 1.

This input allows an external device to access the serial port.

$\overline{\text{DRDY}}$ - Data Ready, Pin 16.

Data Ready goes low at the end of a digital filter convolution cycle to indicate that a new output word has been placed into the serial port. $\overline{\text{DRDY}}$ will return high after all data bits are shifted out of the serial port or two master clock cycles before new data becomes available if the $\overline{\text{CS}}$ pin is inactive (high).

SDATA - Serial Data Output, Pin 15.

SDATA is the output pin of the serial output port. Data from this pin will be output at a rate determined by SCLK. Data is output MSB first and advances to the next data bit on the falling edges of SCLK. SDATA will be in a high impedance state when not transmitting data.

SCLK - Serial Clock Input, Pin 14.

A clock signal on this pin determines the output rate of the data from the SDATA pin. This pin must not be allowed to float.

Control Input Pins

CAL - Calibrate, Pin 3.

When taken high the same time that the CONV pin is taken high the converter will perform a self-calibration which includes calibration of the offset and gain scale factors in the converter.

CONV - Convert, Pin 2.

The CONV pin initiates a calibration cycle if it is taken from low to high while the CAL pin is high, or it initiates a conversion if it is taken from low to high with the CAL pin low. If CONV is held high (CAL low) the converter will do continuous conversions.

BP/$\overline{UP}$ - Bipolar/Unipolar, Pin 6.

The BP/$\overline{UP}$ pin selects the conversion mode of the converter. When high the converter will convert bipolar input signals; when low it will convert unipolar input signals.

Measurement and Reference Inputs

AIN+, AIN- - Differential Analog Inputs, Pins 7, 8.

Analog differential inputs to the delta-sigma modulator.

VREF+, VREF- - Differential Voltage Reference Inputs, Pins 9, 10.

A differential voltage reference on these pins operates as the voltage reference for the converter. The voltage between these pins can be any voltage between 1.0 and 3.6 volts.

Power Supply Connections

VA+ - Positive Analog Power, Pin 11.

Positive analog supply voltage. Nominally +5 volts.

VD+ - Positive Digital Power, Pin 13.

Positive digital supply voltage. Nominally +5 volts or +3.3 volts.

GND - Ground, Pin 12.

Ground.

SPECIFICATION DEFINITIONS

Linearity Error

The deviation of a code from a straight line which connects the two endpoints of the A/D Converter transfer function. One endpoint is located 1/2 LSB below the first code transition and the other endpoint is located 1/2 LSB beyond the code transition to all ones. Units in percent of full-scale.

Differential Nonlinearity

The deviation of a code's width from the ideal width. Units in LSBs.

Full Scale Error

The deviation of the last code transition from the ideal [{(VREF+) - (VREF-)} - $\frac{3}{2}$ LSB]. Units are in LSBs.

Unipolar Offset

The deviation of the first code transition from the ideal ($\frac{1}{2}$ LSB above the voltage on the AIN- pin.) when in unipolar mode (BP/$\overline{\text{UP}}$ low). Units are in LSBs.

Bipolar Offset

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal ($\frac{1}{2}$ LSB below the voltage on the AIN- pin.) when in bipolar mode (BP/$\overline{\text{UP}}$ high). Units are in LSBs

APPENDIX

The following companies provide 32.768 kHz crystals in many package varieties and temperature ranges.

Fox Electronics
5570 Enterprise Parkway
Fort Meyers, FL 33905
(813) 693-0099

Micro Crystal Division / SMH
702 West Algonquin Road
Arlington Heights, IL 60005
(708) 806-1485

SaRonix
4010 Transport Street
Palo Alto, California 94303
(415) 856-6900

Statek
512 North Main
Orange, California 92668
(714) 639-7810

IQD Ltd.
North Street
Crewkerne
Somerset TA18 7AK
England
01460 77155

Mr. Pierre Hersberger
Microcrystal/DIV. ETA S.A.
Schild-Rust-Strasse 17
Grenchen CH-2540
Switzerland
065 53 05 57

Taiwan X'tal Corp.
5F. No. 16, Sec 2, Chung Yang S. RD.
Reitou, Taipei, Taiwan R. O. C.
Tel: 02-894-1202
Fax: 02-895-6207

Interquip Limited
24/F Million Fortune Industrial Centre
34-36 Chai Wan Kok Street, Tsuen Wan N T
Tel: 4135515
Fax: 4137053

S& T Enterprises, Ltd.
Rm 404 Blk B
Sea View Estate
North Point, Hong Kong
Tel: 5784921
Fax: 8073126

Mr. Darren Mcleod
Hy-Q International Pty. Ltd.
12 Rosella Road,
FRANKSON, 3199
Victoria, Australia
Tel: 61-3-783 9611
Fax: 61-3-783 9703

Semiconductor Corporation

CDB5509

Evaluation Board for the CS5509 A/D Converter

Features

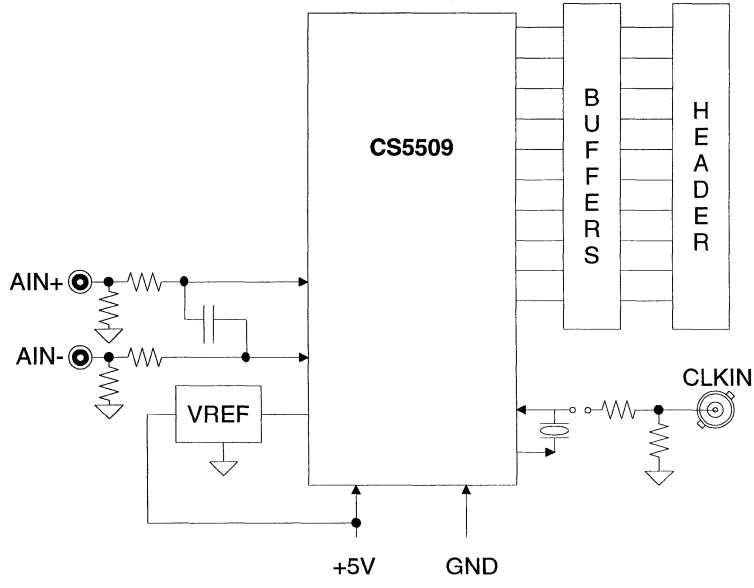
- Operation with on-board 32.768 kHz crystal or off-board clock source
- DIP Switch Selectable: BP/$\overline{UP}$ mode
- On-board precision voltage reference
- Access to all digital control pins

General Description

The CDB5509 is a circuit board designed to provide quick evaluation of the CS5509 A/D converter.

The board provides buffered digital signals, an on-board precision voltage reference, options for using an external clock, and a momentary switch to initiate calibration.

ORDERING INFORMATION: CDB5509



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Introduction

The CDB5509 evaluation board provides a quick means of testing the CS5509 A/D converter. The CS5509 converter requires a minimal amount of external circuitry. The evaluation board comes configured with the A/D converter chip operating from a 32.768 kHz crystal and with an off-chip precision 2.5 volt reference. The board provides access to all of the digital interface pins of the CS5509 chip.

Evaluation Board Overview

The board provides a complete means of making the CS5509 A/D converter chip function. The user must provide a means of taking the output data from the board in serial format and using it in his system.

Figure 1 illustrates the schematic for the board. The board comes configured for the A/D converter chip to operate from the 32.768 kHz watch crystal. A BNC connector for an external clock is provided on the board. To connect the external BNC source to the converter chip, a circuit trace must be cut. Then a jumper must be inserted in the proper holes to connect the XIN pin of the converter to the input line from the BNC. The BNC input is terminated with a 50Ω resistor. Remove this resistor if driving from a logic gate. See the schematic in Figure 1.

The board comes with the A/D converter VREF+ and VREF- pins hard-wired to the 2.5 volt bandgap voltage reference IC on the board.

All of the control pins of the CS5509 are available at the J1 header connector. Buffer ICs U2 and U3 are used to buffer the converter for interface to off-board circuits. The buffers are used on the evaluation board only because the exact loading and off-board circuitry is unknown. Most applications will not require the buffer ICs for proper operation.

To put the board in operation, select either bipolar or unipolar mode with DIP switch S2. Then press the CAL pushbutton after the board is powered up. This initiates calibration of the converter which is required before measurements can be taken. With CONV high (S2-3 open) the converter will convert continuously. Figure 3 illustrates the CAB5509 adapter board. The CAB5509 translates a CS5505 pinout to a CS5509 pinout.

Figures 4 and 5 illustrate the evaluation board layout while Figure 6 illustrates the component placement (silkscreen) of the evaluation board.

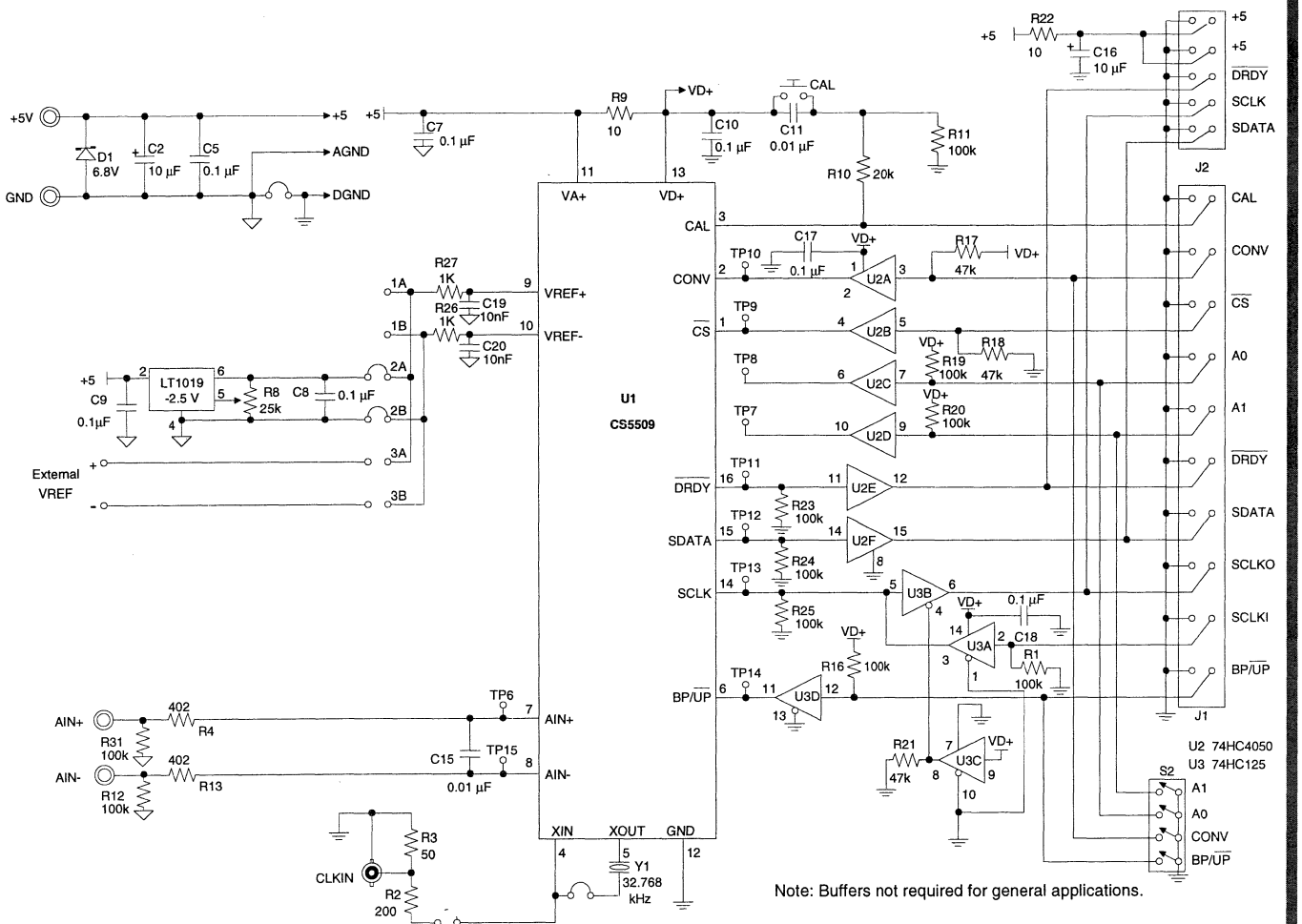


Figure 1. ADC Connections

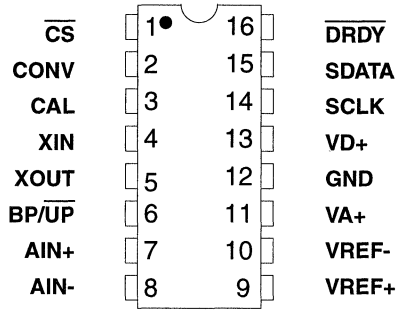


Figure 2. CS5509 Pin Layout

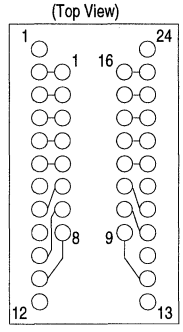


Figure 3. CAB5509 Adapter Board

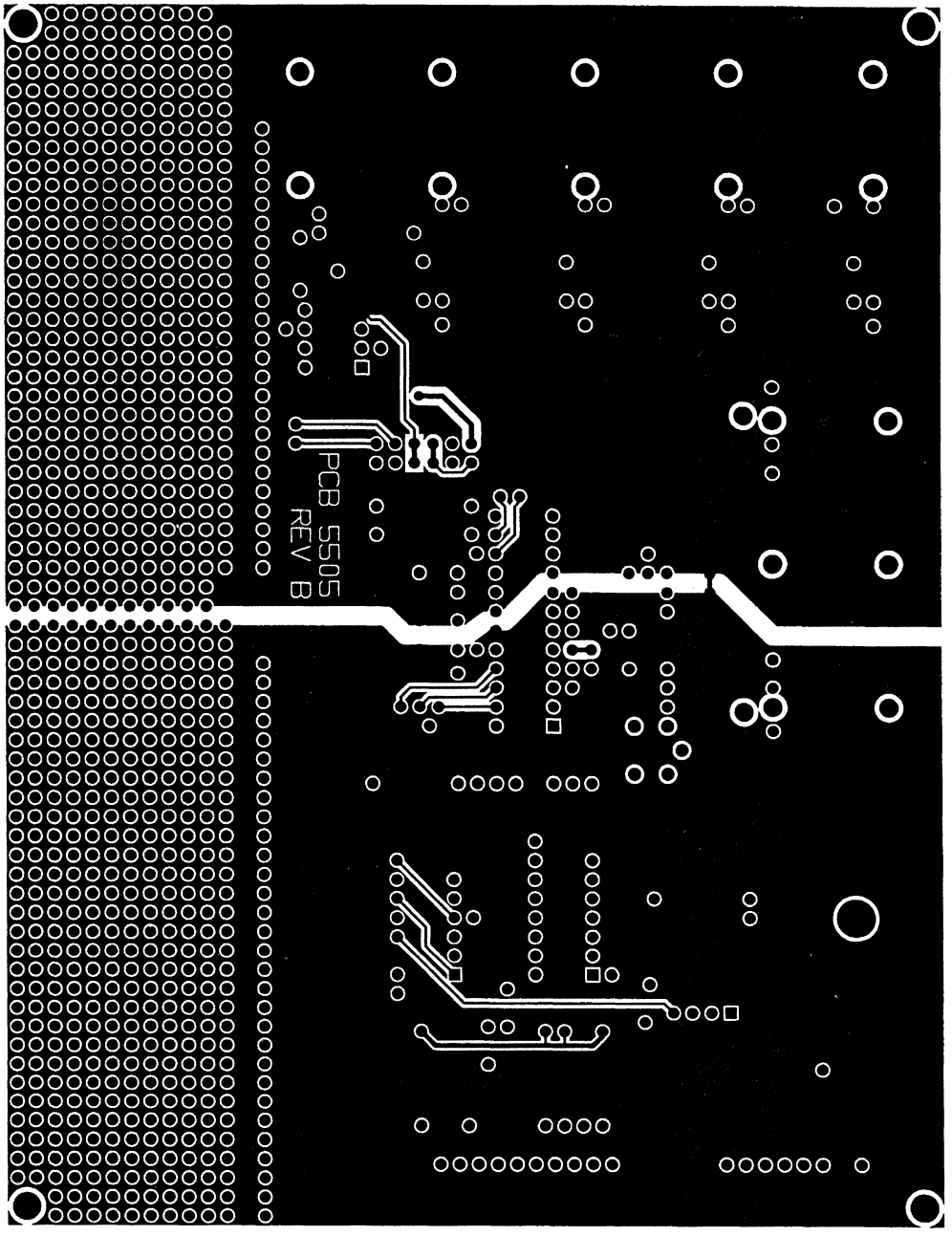


Figure 4. Top Ground Plane Layer (NOT TO SCALE)

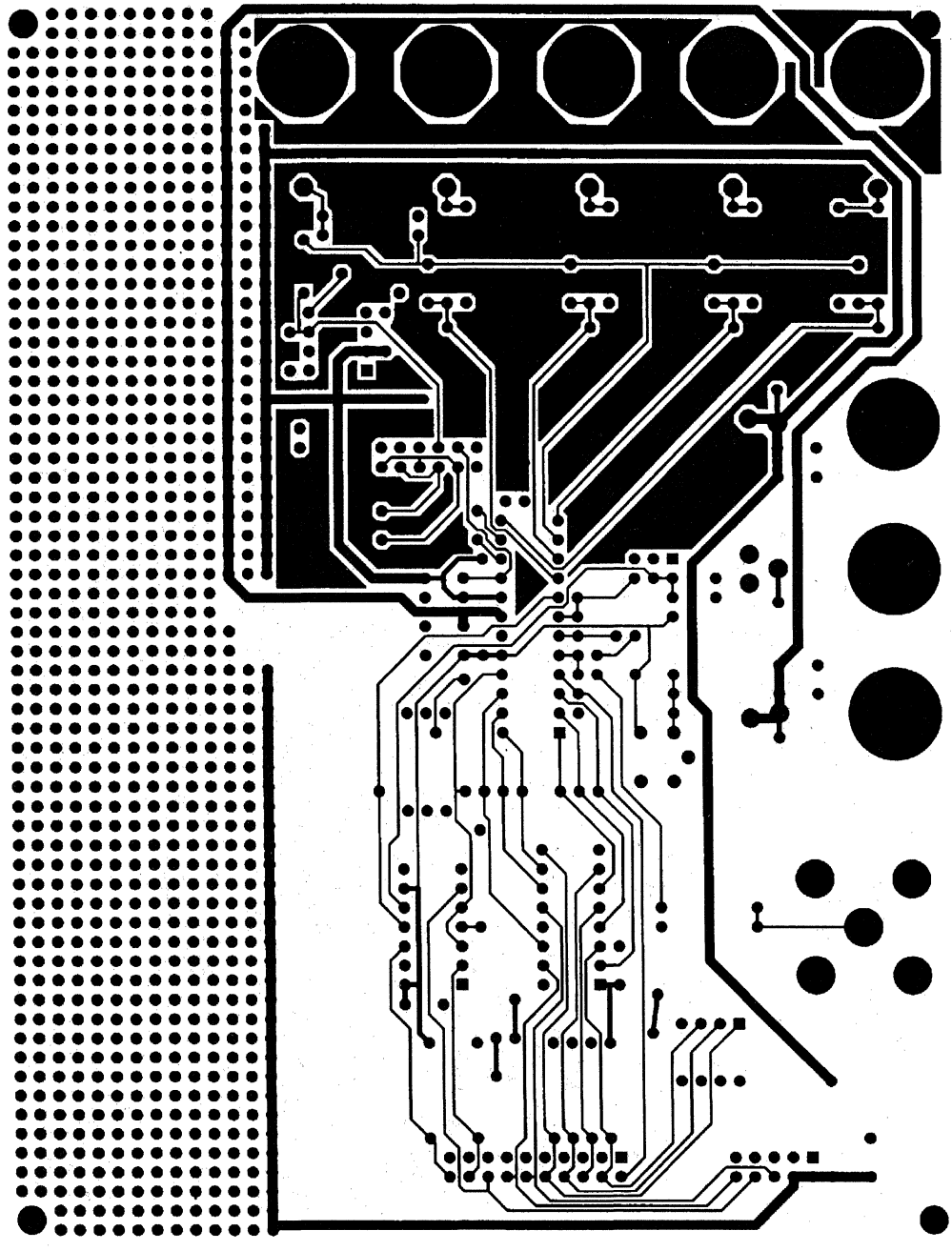


Figure 5. Bottom Trace Layer (NOT TO SCALE)

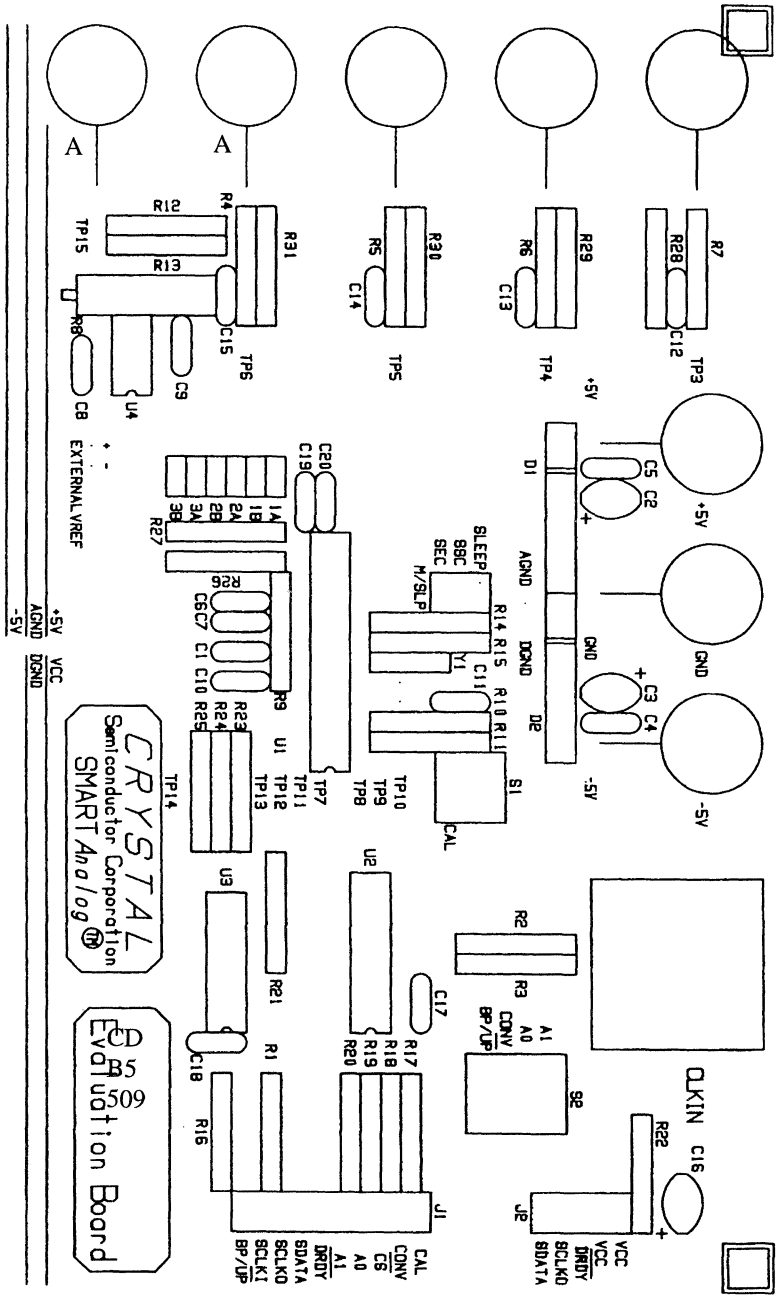


Figure 6. Silk Screen Layer (NOT TO SCALE)

•Notes•

16-Bit/20-Bit Bridge Transducer A/D Converters

Features

- On-chip Instrumentation Amplifier
- On-chip Programmable Gain Amplifier
- On-Chip 4-Bit D/A For Offset Removal
- Dynamic Excitation Options
- Linearity Error: ±0.0015% FS 20-Bit No Missing Codes
- CMRR at 50/60Hz >200dB
- System Calibration Capability with calibration read/write option
- 3, 4 or 5 wire Serial Communications Port
- Low Power Consumption: 40mW 10µW Standby Mode for Portable applications

General Description

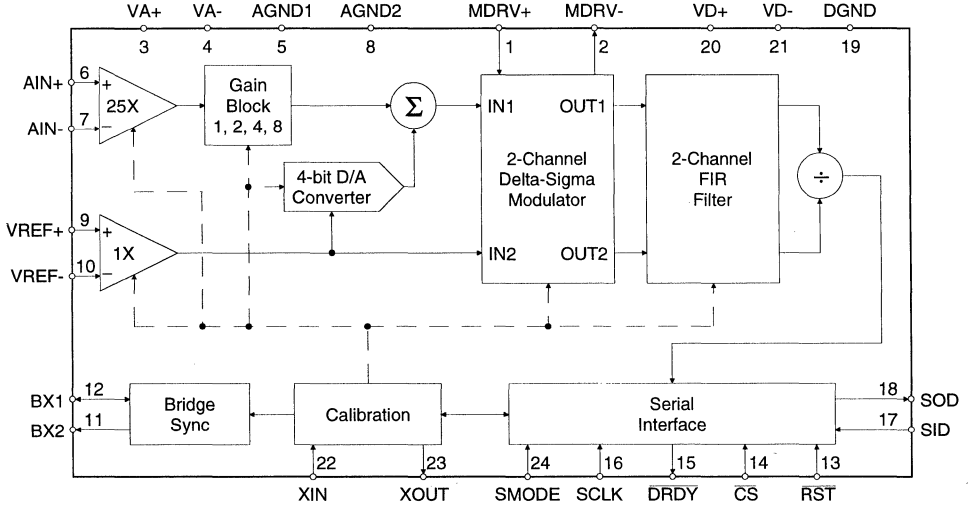
The CS5516 and CS5520 are complete solutions for digitizing low level signals from strain gauges, load cells, and pressure transducers. Any family of mV output transducers, including those requiring bridge excitation, can be interfaced directly to the CS5516 or CS5520. The devices offer an on-chip software programmable instrumentation amplifier block, choice of DC or AC bridge excitation, and software selectable reference and signal demodulation.

The CS5516 uses delta-sigma modulation to achieve 16-bit resolution at output word rates up to 60Hz. The CS5520 achieves 20-bit resolution at word rates up to 60Hz.

The CS5516 and CS5520 sample at a rate set by the user in the form of either an external CMOS clock or a crystal. On-chip digital filtering provides rejection of all frequencies above 12Hz for a 4.096 MHz clock.

The CS5516 and CS5520 include system calibration to null offset and gain errors in the input channel. The digital values associated with the system calibration can be written to, or read from, the calibration RAM locations at any time via the serial communications port. The 4-bit DC offset D/A converter, in conjunction with digital correction, is initially used to zero the input offset value.

ORDERING INFORMATION: Page 2-547



ANALOG CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+, MDRV+ = 5V; VA-, VD- = -5V; VREF= 2.5V(external differential voltage across VREF+ and VREF-); f_{CLK} = 4.9152 MHz; AC Excitation 300 Hz; Gain = 25; Bipolar Mode; R_{source} = 300Ω with a 4.7nF to AGND at AIN (see Note 1); unless otherwise specified.)

Parameter*		Min	Typ	Max	Units
Specified Temperature Range			-40 to +85		°C
Accuracy					
Linearity Error		-	0.0015	0.003	±%FS
Differential Nonlinearity		-	±0.25	±0.5	LSB_{16}
Unipolar Gain Error	(Note 2)	-	±8	±31	ppm
Bipolar Gain Error	(Note 2)	-	±8	±31	ppm
Unipolar/Bipolar Gain Drift		-	±1	-	ppm/°C
Unipolar Offset	(Note 2)	-	±1	±2	LSB_{16}
Bipolar Offset	(Note 2)	-	±1	±2	LSB_{16}
Offset Drift		-	±0.005	-	µV/°C
Noise (Referred to Input)	Gain = 25 (25 x 1)	-	250	-	nVrms
	Gain = 50 (25 x 2)	-	200	-	nVrms
	Gain = 100 (25 x 4)	-	150	-	nVrms
	Gain = 200 (25 x 8)	-	150	-	nVrms

Notes:
1. The AIN and VREF pins present a very high input resistance at dc and a minor dynamic load which scales to the master clock frequency. Both source resistance and shunt capacitance are therefore critical in determining the source impedance requirements of the CS5516 and CS5520 at these pins.
2. Applies after system calibration at the temperature of interest.

	Unipolar Mode			Bipolar Mode		
µV	LSB's	% FS	ppm FS	LSB's	% FS	ppm FS
0.4	0.26	0.0004	4	0.13	0.0002	2
0.76	0.50	0.0008	8	0.26	0.0004	4
1.52	1.00	0.0015	15	0.50	0.0008	8
3.04	2.00	0.0030	30	1.00	0.0015	15
6.08	4.00	0.0061	61	2.00	0.0030	30
	VREF = 2.5V			PGA gain = 1		

CS5516; 16-Bit Unit Conversion Factors

* Refer to the Specification Definitions immediately following the Pin Description Section.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (continued)

Parameter*		Min	Typ	Max	Units
Specified Temperature Range			-40 to +85		°C
Accuracy					
Linearity Error		-	0.0007	0.0015	±%FS
Differential Nonlinearity	(No Missing Codes)	20	-	-	Bits
Unipolar Gain Error	(Note 2)	-	±4	±24	ppm
Bipolar Gain Error	(Note 2)	-	±4	±24	ppm
Unipolar/Bipolar Gain Drift		-	±1	-	ppm/°C
Unipolar Offset	(Note 2)	-	±4	±8	LSB_{20}
Bipolar Offset	(Note 2)	-	±4	±8	LSB_{20}
Offset Drift		-	±0.005	-	µV/°C
Noise (Referred to Input)	Gain = 25 (25 x 1)	-	250	-	nVrms
	Gain = 50 (25 x 2)	-	200	-	nVrms
	Gain = 100 (25 x 4)	-	150	-	nVrms
	Gain = 200 (25 x 8)	-	150	-	nVrms

	Unipolar Mode			Bipolar Mode		
µV	LSB's	% FS	ppm FS	LSB's	% FS	ppm FS
0.025	0.26	0.0000238	0.25	0.13	0.0000119	0.125
0.047	0.50	0.0000477	0.50	0.26	0.0000238	0.25
0.095	1.00	0.0000954	1.0	0.50	0.0000477	0.50
0.190	2.00	0.0001907	2.0	1.00	0.0000954	1.0
0.380	4.00	0.0003814	4.0	2.00	0.0001907	2.0
		VREF = 2.5V			PGA gain = 1	

CS5520; 20-Bit Unit Conversion Factors

* Refer to the Specification Definitions immediately following the Pin Description Section.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (continued)

Parameter		Min	Typ	Max	Units
Specified Temperature Range			-40 to +85		°C
Analog Input					
Analog Input Range	Unipolar Bipolar		12.5, 25, 50, 100 ±12.5, ±25, ±50, ±100		mV mV
Common Mode Rejection	dc 50, 60 Hz	- -	165 200	- -	dB dB
Input Capacitance		-	5	-	pF
Input Bias Current	(Note 1)	-	100	-	pA
Instrumentation Amplifier					
Gain		-	25	-	
Bandwidth		-	200	-	kHz
Unity Gain Bandwidth		-	5	-	MHz
Output Slew Rate		-	1.5	-	V/µsec
Noise @ 10 Hz BW		-	100	-	nVrms
Power Supply Rejection @ 50/60 Hz	(Note 3)	-	120	-	dB
Common Mode Range	(Note 4)	-	±3	-	V
Chopping Frequency		-	XIN/128	-	Hz
Programmable Gain Amplifier					
Gain Tracking	(Note 5)	-	±1	-	%
4-Bit Offset Trim DAC					
Accuracy		-	±5	-	%
Voltage Reference Input					
Range	(Note 6)	2.0	2.5	3.8	V
Common Mode Rejection:	dc 50, 60 Hz	- -	60 200	- -	dB
Input Capacitance		-	15	-	pF
Input Bias Current	(Note 1)	-	10	-	nA

Notes:
3. This includes the on-chip digital filtering.
4. The maximum magnitude of the differential input voltage, Vdiff(in) is determined by the following:
   Vdiff(in) < 300 mV - IVcm/12.5 I and should never exceed 300mV.
   Vcm is the common mode voltage which is applied to the instrumentation amplifier inputs.
   The above equation should be used to calculate the allowable common mode voltage for a given differential voltage applied to the first gain stage inputs. This limit ensures that the instrumentation amplifier does not saturate.
5. Gain tracking accuracy can be significantly improved by uploading a calibrated gain word to the gain register for each PGA gain selection.
6. The common mode voltage on the Voltage Reference Input, plus the reference range, [(VREF+) - (VREF-)]/2, must not exceed ±3 volts.

ANALOG CHARACTERISTICS (continued)

Parameter		Min	Typ	Max	Units
Modulator Differential Voltage Reference					
Nominal Output Voltage		-	3.75	-	V
Initial Output Voltage Tolerance		-	±100	-	mV
Temperature Coefficient		-	100	-	ppm/°C
Line Regulation	(4.75V < VA < 5.25V)	-	0.5	-	mV/V
Output Voltage Noise	0.1 to 15 Hz	-	10	-	μV_{p-p}
Output Current Drive:	Source Current	-	-	20	µA
	Sink Current	-	-	20	µA
Power Supplies					
DC Power Supply Currents	I_{A+}	-	2.7	3.5	mA
	I_{A-}	-	-2.7	-3.5	mA
	I_{D+}	-	1.5	2.2	mA
	I_{D-}	-	-0.6	-0.8	mA
Power Dissipation:	(Note 7)				
	Normal Operation	-	37.5	-	mW
	Standby Mode	-	10	-	µW
Power Supply Rejection: dc	Positive Supplies	-	100	-	dB
dc	Negative Supplies	-	95	-	dB
System Calibration Specifications					
Positive Full Scale Calibration Range	(Note 8)				
	Unipolar Mode	0.8T	-	1.2T	V
	Bipolar Mode	0.8T	-	1.2T	V
Maximum Ratiometric Offset Calibration Range	(Note 8)				
	Unipolar Mode	-2T	-	+2T	V
	Bipolar Mode	-2T	-	+2T	V
Differential Input Voltage Range	(Notes 4, 8, 9, 10)				
	Unipolar Mode	Voffset + (1.2T)			V
	Bipolar	Voffset ± (1.2T)			V

Notes:
7. All outputs unloaded. All inputs CMOS levels.
8. T=VREF/(Gx25), where T is the full scale span, where VREF is the differential voltage across VREF+ and VREF- in volts, and G is the gain setting of the second gain block. G can be set to 1, 2, 4, 8. This sets the overall gain to 25, 50, 100, 200. The gain can then be fine tuned by using the calibration of the full scale point.
9. When calibrated.
10. V_{offset} is the offset corrected by the offset calibration routine. V_{offset} may be as large as 2T.

DYNAMIC CHARACTERISTICS

Parameter	Symbol	Ratio	Units
AIN and VREF Input Sampling Frequency	f_{is}	$f_{clk}/128$	Hz
Modulator Sampling Frequency	f_s	$f_{clk}/256$	Hz
Output Update Rate	f_{out}	$f_{clk}/81,920$	Hz
Filter Corner Frequency	f_{-3dB}	$f_{clk}/341,334$	Hz
Settling Time to ±0.0007% (FS Step)	t_s	$6/f_{out}$	s

DIGITAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+ = 5V ± 5%; VA-, VD- = -5V ± 5%; DGND = 0) All measurements below are performed under static conditions.

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage:	XIN	V_{IH}	4.5	-	-	V
	All Pins Except XIN	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	XIN	V_{IL}	-	-	0.5	V
	All Pins Except XIN	V_{IL}	-	-	0.8	V
High-Level Output Voltage	(Note 11)	V_{OH}	(VD+)-1.0	-	-	V
Low-Level Output Voltage	I_{out} = 1.6mA	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	1	10	µA
3-State Leakage Current		I_{OZ}	-	-	±10	µA
Digital Output Pin Capacitance		C_{out}	-	9	-	pF

Notes: 11. I_{out} = -100 µA. This guarantees the ability to drive one TTL load. (V_{OH} = 2.4V @ I_{out} = -40 µA).

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V, see Note 12.)

Parameter		Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	VD+	4.5	5.0	5.5	V
	Negative Digital	VD-	-4.5	-5.0	-5.5	V
	Positive Analog	VA+	4.5	5.0	5.5	V
	Negative Analog	VA-	-4.5	-5.0	-5.5	V
Differential Analog Reference Voltage		(VREF+) - (VREF-)	2.0	2.5	3.8	V
Analog Input Voltage:	(Note 13)					
	Unipolar	VAIN	0	-	+T	V
	Bipolar	VAIN	-T	-	+T	V

Notes: 12. All voltages with respect to ground.

13. The CS5516 and CS5520 can accept input voltages up to +T in unipolar mode and -T to +T in bipolar mode where T=VREF/(Gx25). G is the gain setting at the second gain block. When the inputs exceed these values, the CS5516 and CS5520 will output positive full scale for any input above T, and negative full scale for inputs below AGND in unipolar and -T in bipolar mode. This applies when the analog input does not exceed ±2T overrange.

ABSOLUTE MAXIMUM RATINGS* (AGND, DGND = 0V, all voltages with respect to ground.)

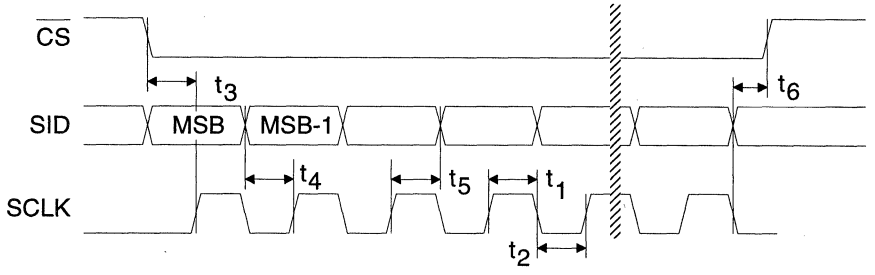
Parameter			Symbol	Min	Typ	Max	Units
DC Power Supplies:	Positive Digital	(Note 14)	VD+	-0.3	-	(VA+)+0.3	V
	Negative Digital		VD-	-0.3	-	-5.5	V
	Positive Analog		VA+	-0.3	-	5.5	V
	Negative Analog		VA-	+0.3	-	-5.5	V
Input Current, Any Pin Except Supplies		(Notes 15, 16)	I_{in}	-	-	±10	mA
Analog Input Voltage	AIN and VREF pins		V_{INA}	(VA-)-0.3	-	(VA+)+0.3	V
Digital Input Voltage			V_{IND}	-0.3	-	(VD+)+0.3	V
Ambient Operating Temperature			T_A	-55	-	125	°C
Storage Temperature			T_{stg}	-65	-	150	°C

Notes: 14. No pin should go more positive than (VA+)+0.3V. VD+ must always be less than (VA+)+0.3 V,and can never exceed 6.0V.

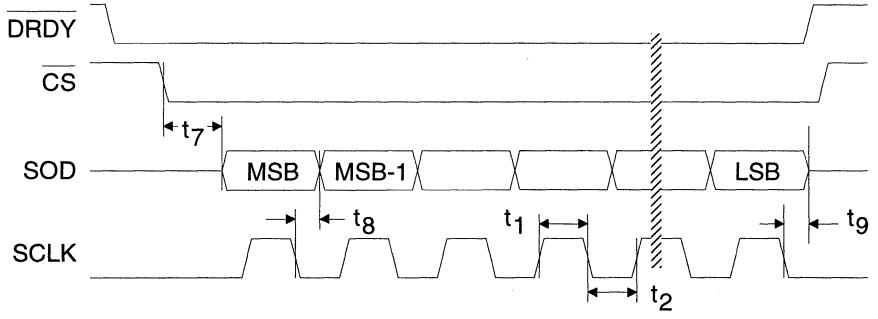
15. Applies to all pins including continuous overvoltage conditions at the analog input pins.

16. Transient currents of up to 100mA will not cause SCR latch-up. Maximum input current for a power supply pin is ± 50 mA.

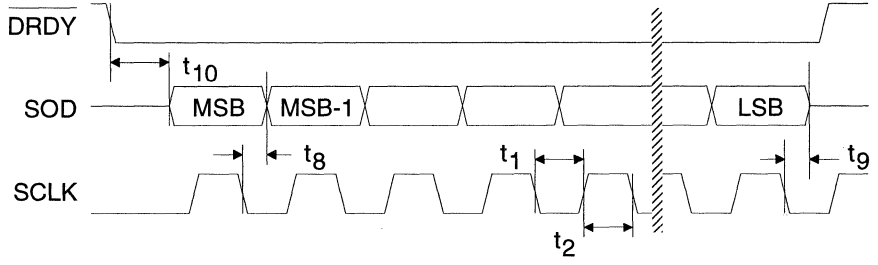
* WARNING: Operation beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.



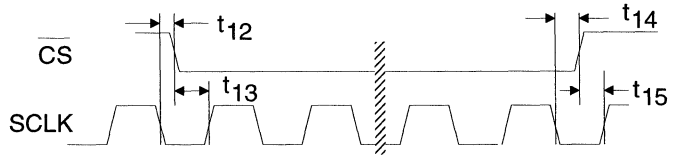
SID Write Timing (Not to Scale)



SOD Read Timing (Not to Scale)



SOD Read Timing with CS = 0 (Not to Scale)



$\overline{CS}$ with Continuous SCLK (Not to Scale)

SWITCHING CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; VA+, VD+ = 5V ± 5%; VA-, VD- = -5V±5%; Input Levels: Logic 0 = 0V, Logic 1 = VD+; C_L = 50 pF)

Parameter		Symbol	Min	Typ	Max	Units
Master Clock Frequency: Internal Oscillator / External Clock		XIN	1.0	4.096	5.0	MHz
Master Clock Duty Cycle			40	-	60	%
Rise Times	Any Digital Input (Note 18) Any Digital Output	t_{rise}	- -	- 50	1.0 -	µs ns
Fall Times	Any Digital Input (Note 18) Any Digital Output	t_{fall}	- -	- 50	1.0 -	µs ns
Startup						
Power-on Reset Period		t_{por}	-	100	-	ms
Oscillator Start-up Time	XTAL = 4.9152 MHz(Note 19)	t_{ost}	-	60	-	ms
$\overline{RST}$ Pulse Width		t_{res}	1/XIN	-	-	ns
Serial Port Timing						
Serial Clock Frequency		SCLK	-	-	2.4	MHz
Serial Clock	Pulse Width High Pulse Width Low	t_1 t_2	200 200	- -	- -	ns ns
SID Write Timing						
$\overline{CS}$ Enable to Valid Latch Clock		t_3	150	-	-	ns
Data Set-up Time prior to SCLK rising		t_4	50	-	-	ns
Data Hold Time After SCLK Rising		t_5	50	-	-	ns
SCLK Falling Prior to $\overline{CS}$ Disable		t_6	50	-	-	ns
SOD Read Timing						
CS to Data Valid		t_7	-	-	150	ns
SCLK Falling to New Data Bit		t_8	-	-	170	ns
SCLK Falling to SOD Hi-Z		t_9	-	-	200	ns
$\overline{DRDY}$ Falling to Valid Data	($\overline{CS}$ = 0)	t_{10}	-	-	150	ns
$\overline{CS}$ Rising to SOD Hi-Z		t_{11}	-	-	150	ns
$\overline{CS}$ Disable Hold Time		t_{12}	50	-	-	ns
$\overline{CS}$ Enable Set-up Time		t_{13}	150	-	-	ns
$\overline{CS}$ Enable Hold Time		t_{14}	50	-	-	ns
$\overline{CS}$ Disable Set-up Time		t_{15}	150	-	-	ns

Notes: 18. Specified using 10% and 90% points on waveform of interest. Output loaded with 50 pF.
19. Oscillator start-up time varies with crystal parameters. This specification does not apply when using an external clock source.

GENERAL DESCRIPTION

The CS5516 and CS5520 are monolithic CMOS A/D converters which include an instrumentation amplifier input, an on-chip programmable gain amplifier, and a DAC for offset trimming. While the devices are optimized for ratiometric measurement of Wheatstone bridge applications, they can be used for general purpose low-level signal measurement.

Each of the devices includes a two-channel differential delta-sigma modulator (the signal measurement input and the reference input are digitized independently before a digital output word is computed), a calibration microcontroller, a two-channel digital filter, a programmable instrumentation amplifier block, a 4-bit DAC for coarse offset trimming, circuitry for generation and demodulation of AC (actually switched DC) bridge excitation, and a serial port. The CS5516 outputs 16-bit words; the CS5520 outputs 20-bit words.

The CS5516/20 devices can measure either unipolar or bipolar signals. Self-calibration is utilized to maximize performance of the measurement system. To better understand the capabilities of the CS5516/20, it is helpful to examine some of the error sources in bridge measurement systems.

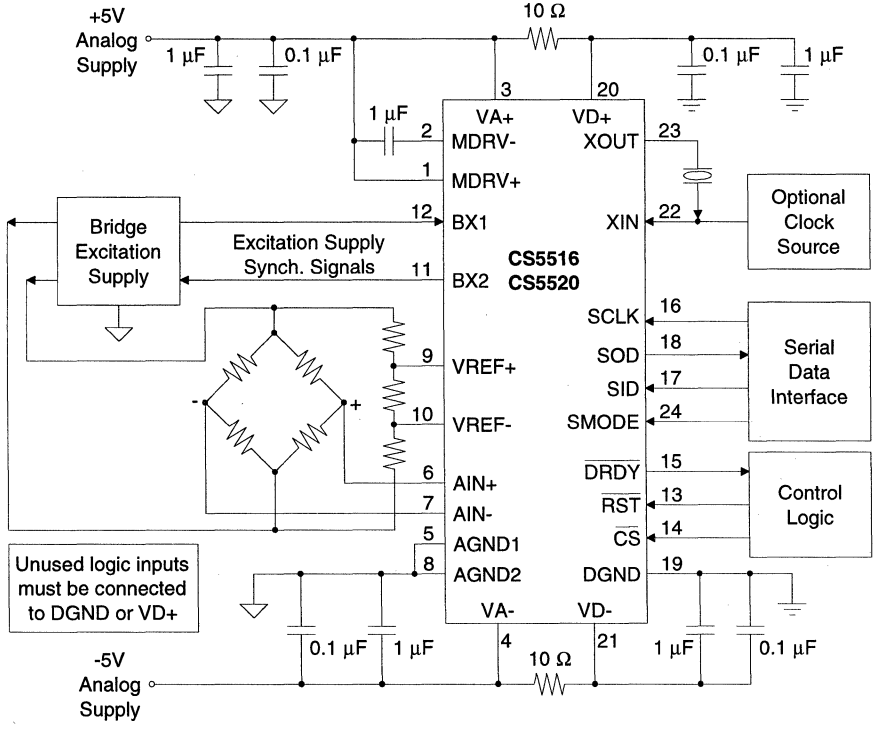


Figure 1. System Connection Diagram: AC Excitation Mode Using External Excitation

THEORY OF OPERATION

The front page of this data sheet illustrates the block diagram of the CS5516 and CS5520 A/D converter. The device includes an instrumentation amplifier with a fixed gain of 25. This chopper-stabilized instrumentation amplifier is followed by a programmable gain stage with gain settings of 1, 2, 4, and 8. The sensitivity of the input is a function of the programmable gain setting and of the reference voltage connected between the VREF+ and VREF- pins of the device. The full scale of the converter is VREF/(G x 25) in unipolar, or ±VREF/(G x 25) in bipolar, where VREF is the reference voltage between the VREF+ and VREF- pins, G is the gain setting of the programmable gain amplifier, and 25 is the gain of the instrumentation amplifier.

After the programmable gain block, the output of a 4-bit DAC is combined with the input signal. The DAC can be used to add or subtract offset from the analog input signal. Offsets as large as ±200 % of full scale can be trimmed from the input signal.

The CS5516 and CS5520 are optimized to perform ratiometric measurement of bridge-type transducers. The devices support dc bridge excitation or two modes of ac (switched dc) bridge excitation. In the switched-dc modes of operation the converter fully demodulates both the reference voltage and the analog input signal from the bridge.

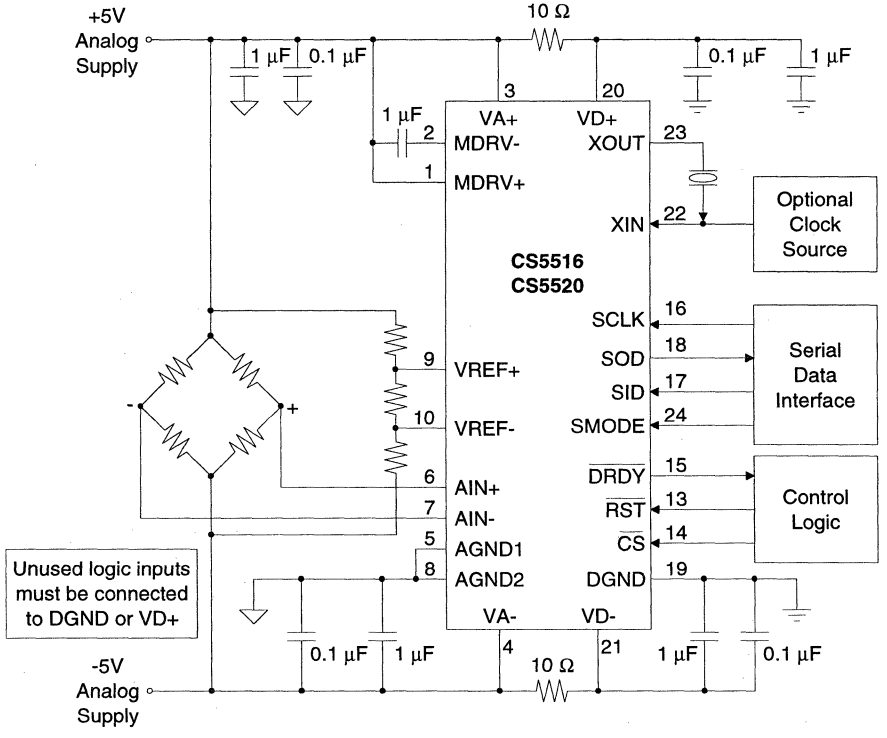


Figure 2. System Connection Diagram: DC Excitation Mode (EXC bit = 0), F1 = F0 = 0.

Command Register

D7	D6	D5	D4	D3	D2	D1	D0
1	**RSB2**	**RSB1**	**RSB0**	**R/$\overline{W}$**	**0**	**0**	**0**

BIT	NAME	VALUE	FUNCTION
D7	D7	1	Must always be logic 1
RSB2-0	Register Select Bit		Selects Register to be Read or Written per R/$\overline{W}$ bit
		000	CONVERSION DATA (read only)
		001	CONFIGURATION
		010	GAIN
		011	DAC
		100	RATIOMETRIC OFFSET
		101	NON-RATIOMETRIC OFFSET - AIN
		110	NON-RATIOMETRIC OFFSET - VREF
		111	NOT USED
R/$\overline{W}$	Read/$\overline{Write}$	0	Write to the register selected by the RSB2-0 bits
		1	Read from the register selected by the RSB2-0 bits
D2	D2	0	Not Used
D1	D1	0	Not Used
D0	D0	0	Not Used

Table 1. CS5516 and CS5520 Commands

The CS5516/20 includes a microcontroller which manages operation of the chip. Included in the microcontroller are eight different registers associated with the operation of the device. An 8-bit command register is used to interpret instructions received via the serial port. When power is applied, and the device has been reset, the serial port is initialized into the command mode. In this mode it is waiting to receive an 8-bit command via its serial port. The first 8 bits into the serial port are placed into the command register. Table 1 lists all the valid command words for reading from or writing to internal registers of the converter. Once a valid 8-bit command word has been received and decoded, the serial port goes into data mode. In data mode the next 24 serial clock pulses shift data either into or out of the serial port. When writing data to the port, the data may immediately follow the command word. When reading data from the port, the user must pause after clocking in the 8-bit command word to allow the microcontroller time to decode the command word, access the appropriate register to be read, and present its 24-bit word to the port. The microcontroller will signal when the 24-bit read data is available by causing the $\overline{DRDY}$ pin to go low.

The user must write or read the full 24-bit word except in the case of reading conversion data. In read data conversion mode, the user may read less than 24 bits if $\overline{CS}$ is then made inactive ($\overline{CS}$ = 1). $\overline{CS}$ going inactive releases user control over the port and allows new data updates to the port.

The user can instruct the on-chip microcontroller to perform certain operations via the configuration register. Whenever a new word is written to the 24-bit configuration register, the microcontroller then decodes the word and executes the configuration register instructions. Table 2 illustrates the bits of the configuration register. The bits in the configuration register will be discussed in various sections of this data sheet.

Configuration Register

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
Register	**DAC3**	**DAC2**	**DAC1**	**DAC0**	**EXC**	**F1**	**F0**	**D16**	**G1**	**G0**	**U/B**	**D12**
Reset (R)	0	0	0	0	0	0	0	0	0	0	0	0

	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register	**A/S**	**EC**	**D9**	**D8**	**CC3**	**CC2**	**CC1**	**CC0**	**D3**	**D2**	**D1**	**RF**
Reset (R)	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	VALUE		FUNCTION
DAC3	DAC Sign Bit	0 1	*R*[1]	Add Offset Subtract Offset — This bit is read only[2]
DAC2-0	DAC Bits	000 001 010 011 100 101 110 111	*R*	 25% Offset 50% Offset 75% Offset 100% Offset 125% Offset 150% Offset 175% Offset — These bits are read only[2]
EXC	Excitation: Internal External	0 1	*R*	BX1 and BX2 outputs are determined by bits F1 and F0 BX1 is an input which determines the phase of the demodulation clock and the BX2 output
F1-F0	Select Frequency	00 01 10 11	*R*	Excitation on BX1 & BX2 is dc. BX1=0 V, BX2=+5 V Excitation Frequency on BX1 & BX2 is XIN/8192 Hz Excitation Frequency on BX1 & BX2 is XIN/16384 Hz Excitation Frequency on BX1 & BX2 is XIN/4096 Hz
D16	D16	0	*R*	Must always be logic 0
G1-G0	Select PGA Gain	00 10 01 11	*R*	Gain = 1 (X25) Gain = 2 (X25) Gain = 4 (X25) Gain = 8 (X25)
U/B	Select Unipolar/Bipolar Mode	0 1	*R*	Bipolar Measurement Mode Unipolar Measurement Mode
D12	D12	0	*R*	Must always be logic 0
A/S	Awake/Sleep	0 1	*R*	Awake Mode Sleep Mode
EC	Execute Calibration	0 1	*R*	Calibration not active Perform calibration selected by CC3-CC0 bits. EC bit must be written back to "0" after calibration is completed
D9	D9	0	*R*	Must always be logic 0
D8	D8	0	*R*	Must always be logic 0
CC3-CC0	Calibration Control Bits	0000 1000 0100 0010 0001	*R*	No calibration to be performed Calibrate non-ratiometric offset, VREF Calibrate non-ratiometric offset, AIN Calibrate ratiometric offset, AIN Calibrate gain, AIN
D3	D3	0	*R*	Must always be logic 0
D2	D2	0	*R*	Must always be logic 0
D1	D2	0	*R*	Must always be logic 0
RF	Reset Filter	0 1	*R*	Normal operation Reset Filter

Notes: 1.Reset State

2.A write to these bits does not change the register bit values. These bits are just a mirror of the DAC register contents.

Table 2. Configuration Register

System Initialization

Whenever power is applied to the CS5516/CS5520 A/D converters, the devices must be reset to a known condition before proper operation can occur. The internal reset is applied after power is established and lasts for approximately 100 ms. The $\overline{RST}$ pin can also be used to establish a reset condition. The reset signal should remain low for at least one XIN clock cycle to ensure adequate reset time. It is recommended that the $\overline{RST}$ pin be used to reset the converter if the power supplies rise very slowly or with poor startup characteristics. The $\overline{RST}$ signal can be generated by a microcontroller output, or by use of an R-C circuit.

The reset function initializes the configuration register and all five of the calibration registers; and places the microcontroller in command mode ready to accept a command from the serial port. Whenever the device is reset the $\overline{DRDY}$ pin will be set to a logic 1 and the on-chip registers are initialized to the following states:

Configuration	000000(H)
Calibration registers:	
DAC	000000(H)
Gain	800000(H)
AIN Ratiometric Offset	000000(H)
AIN Non-ratiometric Offset	000000(H)
VREF Non-ratiometric Offset	000000(H)

CALIBRATION

After the CS5516/20 is reset, the device is functional and can perform measurements without being calibrated. The converter will utilize the initialized values of the calibration registers to calculate output words.

The converter uses the two outputs (AIN & VREF) of the dual channel converter along with the contents of the calibration registers to compute the conversion data word. The following equation indicates the computation.

$$R0 = R4\left[\left[\frac{D_{AIN} - R1}{D_{VREF} - R2}\right] - R3\right]$$

Where R0 is the output data, D_{AIN} and D_{VREF} are the digital output words from the AIN and VREF digital filter channels, and R1, R2, R3 and R4 are the contents of the following calibration registers:

R1 = AIN non-ratiometric offset
R2 = VREF non-ratiometric offset
R3 = AIN ratiometric offset
R4 = Gain

The computed output word, R0, is a two's complement number.

Calibration minimizes the errors in the converted output data. If calibration has not been performed, the measurements will include offset and gain errors of the entire system.

The converter may be calibrated each time it is powered up, or calibration words from a previous calibration may be uploaded into the appropriate calibration registers from some type of E^2PROM by the system microcontroller.

The converter uses five different registers to store specific calibration information. Each of the calibration registers stores information pertinent to correcting a specific source of error associated with either the converter or with the input transducer and its wiring. The method by

Configuration Register					CAL Type	Calibration Time
EC	CC3	CC2	CC1	CC0		
1	1	0	0	0	VREF Non-ratiometric Offset	573,440/fclk
1	0	1	0	0	AIN Non-ratiometric Offset	573,440/fclk
1	0	0	1	0	AIN Ratiometric Offset	2,211,840/fclk
1	0	0	0	1	AIN System Gain	573,440/fclk
1	1	1	0	0	VREF & AIN Non-ratiometric Offset	573,440/fclk
0	X	X	X	X	End Calibration	-

$\overline{DRDY}$ remains high through calibration sequence. In all modes, $\overline{DRDY}$ falls immediately upon completion of the calibration sequence.

Table 3. CS5516/CS5520 Calibration Control

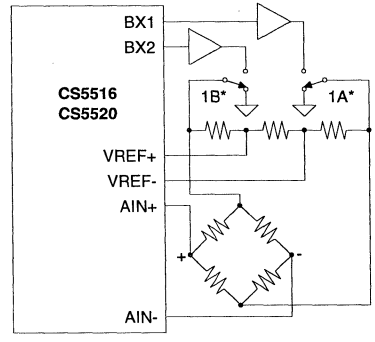
which calibration is initiated is common to each of the calibration registers. The configuration register controls the execution of the calibration process. Bits CC3--CC0 in the configuration register determine which type of calibration will be performed and which of the five calibration registers will be affected. On the falling edge of the 24th SCLK, the configuration word will be latched into the configuration register and the selected calibration will be executed. The time required to perform a calibration is listed in Table 3. The $\overline{DRDY}$ pin will remain a logic 1 during calibration, and will go low when the calibration step is completed.

The serial port should not be accessed while a calibration is in progress. The EC bit of the configuration register remains a logic 1 until it is overwritten by a new configuration word (EC = 0). Consequently, if EC is left active, any write (the falling edge of the 24th SCLK) to any register inside the converter will cause a re-execution of the calibration sequence. This occurs because the internal microcontroller executes the contents of the configuration register every time the 24th SCLK falls after writing a 24-bit word to any internal register. To be certain that calibrations will not be re-executed each time a new word is written or read via the serial port, the EC bit of the configuration register must be written back to a logic 0 after the final calibration step has been completed.

The CC3--CC0 bits of the configuration register determine the type of calibration to be performed. The calibration steps should be performed in the following sequence. If the user determines that non-ratiometric offset calibration is important, the non-ratiometric offset errors of the VREF and AIN input channels should be calibrated first. Then the ratiometric offset of the AIN channel should be calibrated. And finally, the AIN channel gain should be calibrated.

Non-ratiometric Errors

To calibrate out the VREF and AIN non-ratiometric errors, the input channels to the VREF path into the converter and the AIN path into the converter must be grounded (this may occur at the pins of the IC, or at the bridge excitation as shown in Figure 3.). Then the EC, CC2 and CC3 bits of the configuration register must be set to logic 1. The converter will then perform a non-ratiometric calibration and place the



*Note: The bridge can be grounded with a relay or with jumpers to perform non-ratiometric calibration.

Figure 3. Non-ratiometric System Calibration using Internal Excitation

proper 24 bit calibration words in the VREF and AIN non-ratiometric registers. Note that the two non-ratiometric offsets can be calibrated simultaneously or independently, but they must be calibrated prior to the other calibration steps if non-ratiometric offset calibration is to be used. If the effects of the non-ratiometric errors are not significant enough to affect the user application, they can be left uncalibrated (after a reset, the non-ratiometric offset registers will contain 000000(H)).

Ratiometric Offset

Once the non-ratiometric errors have been calibrated, the ratiometric offset error of the AIN channel should be calibrated next. To perform this calibration step, a reference voltage must be applied to the VREF+ and VREF- pins. Then, place "zero" weight on the scale platform. This will result in an offset voltage into the converter which will represent the offset of the bridge, the wiring, and the AIN input of the converter itself. A configuration word with the EC and CC1 bits set to logic 1 is then written into the configuration register. During the ratiometric offset calibration of AIN the microcontroller first uses a successive approximation algorithm to compute the correct values for the DAC3-DAC0 bits of the DAC register. This accommodates any large offsets on the AIN input signal. Once the four DAC bits are computed, this amount of offset is removed from the input signal. The microcontroller then computes the appropriate 24 bit number to place in the AIN ratiometric offset register to calibrate out the remaining offset not removed by the DAC.

Gain

After the AIN ratiometric offset has been calibrated, the next step is to perform a gain calibration. Gain calibration is performed with "full scale" weight on the scale platform. The EC and CC0 bits of the configuration register are set to logic 1. The gain calibration of the AIN channel is the final calibration step. After $\overline{\text{DRDY}}$ falls to signal the completion of this calibration step, the EC bit of the configuration register must be set back to logic 0 to terminate the calibration mode.

Limitations in Calibration Range

There are five calibration registers in the converter. There are two non-ratiometric offset calibration registers, one for the AIN input and one for the VREF input; one 4-bit offset trim DAC; one ratiometric offset calibration register for the AIN input; and one gain calibration register. After the non-ratiometric offsets are calibrated, an LSB in either of the 24-bit non-ratiometric calibration registers represents 2^{-23} proportion of an internally-scaled MDRV (Modulator Differential Reference Voltage). At the MDRV+ and MDRV- pins, the MDRV has a nominal value of 3.75 volts. This voltage is internally scaled to a nominal 2.5 volts (never less than 2.4 volts) for use with the non-ratiometric calibration. The two non-ratiometric calibration words are stored in 2's complement form with one count equal to slightly less than 300 nV at the input of the internal A/D converter. For the AIN channel this will be scaled down by the gain of the instrumentation amplifier (X25) and the PGA gain. For a PGA gain = 1, one count of a non-ratiometric register will represent slightly less than 12 nV. Non-ratiometric offset at the VREF input cannot exceed ± 2.4 volts to be within calibration range of the converter. Non-ratiometric offset to be calibrated by the AIN channel cannot exceed ± 2.4 volts divided by the channel gain. With a PGA gain = 1, the maximum non-ratiometric offset which can be calibrated on the AIN channel cannot exceed ± 96 mV.

When the ratiometric offset is calibrated, the 4-bit DAC coarsely trims offset from the analog signal. The ratiometric offset which remains is finely trimmed after the signal has been converted; using the contents of the ratiometric offset register for digital correction. The DAC

bits can be manipulated by the user to add or subtract offset up to 200 percent of the nominal input signal. The AIN ratiometric offset register can be manipulated to add or subtract offset equal to the maximum differential input signal into the X25 amplifier. An LSB in the ratiometric offset register represents 2^{-23} proportion of the voltage input across the VREF+ and VREF- pins at the internal input to the AIN channel A/D converter. This will be scaled down by the AIN channel gain when calculated relative to the instrumentation amplifier input. For example, with a VREF = 2.5 V, the PGA gain = 1, one count of the ratiometric offset register would represent about 12 nV at the instrumentation amplifier input. The proportion remains ratiometric even if the VREF voltage should change. The 24-bit register content is stored in 2's complement form.

Manipulation of the DAC or ratiometric offset register allows the user to shift the transfer function to allow for load cell creep or load cell zero drift.

The gain calibration is performed last. The contents of the gain register spans from 2^{-23} to 2 as shown in Table 4. After gain calibration has been performed, the numeric value in the gain register should not exceed the range of 0.8 to 1.2. The gain calibration range is ± 20 % of the nominal value of 1.0. The nominal value of 1.0 is for an input span dictated by the VREF voltage, the PGA gain, and the X25 instrumentation gain. The converter may operate with gain slope factors from 0.5 to 2.0 (decimal), but when the slope exceeds 1.2 the converter output code computation may lack adequate resolution and result in missing codes in the transfer function. Internal circuitry may saturate for large signals which would calibrate to a gain factor less than 0.8.

In a typical weigh scale application, the CS5516/CS5520 will be calibrated in combination with a load cell at the factory. Once calibrated, the calibration words are off-loaded from the converter and stored in E^2PROM. When powered-up in the field the calibration words are up-loaded into the appropriate registers. This is viable because the AIN and VREF input to the converter are "chopper-stabilized" and maintain excellent stability when subjected to changes in temperature.

2

Programmable Gain Amplifier

The programmable gain amplifier inside the CS5516/20 offers gains of 1, 2, 4, and 8. This is in addition to the fixed gain of × 25 in the input instrumentation amplifier. The gain tracking of the PGA is about one percent between ranges. The user can remove this error by performing a gain calibration at the factory with a full scale signal on each range. The gain calibration word for each gain range can be off-loaded into E^2PROM and uploaded into the gain register whenever a new gain setting is selected for the PGA. Gain stability over temperature for the converter itself is approximately 1 ppm/°C when the device is used ratiometrically.

Serial Interface Modes

The CS5516/20 support either 5, 4 or 3 pin serial interfacing. The SMODE pin sets the operating mode of the serial interface. With SMODE = 0, the device assumes the user is operating with either a 5 or 4 wire interface. The five wire mode includes SOD, SID, SCLK, $\overline{\text{DRDY}}$, and $\overline{\text{CS}}$. In the four wire mode, $\overline{\text{CS}}$ is connected to DGND as a logic 0. The user would then interface to the SOD, SID, SCLK, and $\overline{\text{DRDY}}$ pins.

AIN and VREF Non-Ratiometric Offset Registers

	MSB											LSB
Register	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	//	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}
Reset (R)	0	0	0	0	0	0		0	0	0	0	0	0

One LSB represents 2^{-23} proportion of the internal MDRV (≈2.5 Volts)

DAC Register

	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
Register	**DAC3**	**DAC2**	**DAC1**	**DAC0**	**EXC**	**F1**	**F0**	**D16**	**G1**	**G0**	**U/B**	**D12**
Reset (R)	0	0	0	0	0	0	0	0	0	0	0	0

	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register	**A/S**	**EC**	**D9**	**D8**	**CC3**	**CC2**	**CC1**	**CC0**	**D3**	**D2**	**D1**	**RF**
Reset (R)	0	0	0	0	0	0	0	0	0	0	0	0

BIT	NAME	VALUE		FUNCTION
DAC3	DAC Sign Bit	0 1	*R*[1]	Add Offset Subtract Offset
DAC2-0	DAC Bits	000 001 010 011 100 101 110 111	*R*	 25% Offset 50% Offset 75% Offset 100% Offset 125% Offset 150% Offset 175% Offset
Bits D19 to D0		0	*R*	These bits mirror the Configuration Register read only[2]

Note: 1. Reset State
2. A write to these bits does not change the register bit values.

AIN Ratiometric Offset Register

	MSB											LSB
Register	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	//	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}
Reset (R)	0	0	0	0	0	0		0	0	0	0	0	0

One LSB represents 2^{-23} proportion of the voltage [<(VREF+) - (VREF-)>/GAIN] where GAIN = 25 X PGA Gain

GAIN Register

	MSB											LSB
Register	2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	//	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}
Reset (R)	1	0	0	0	0	0		0	0	0	0	0	0

The gain register span from 0 to $(2\text{-}2^{-23})$. After Reset the MSB=1, all other bits are 0.

Table 4. Calibration Registers

Reading a register in the converter requires a command word to be written to the SID pin. For example, to read the conversion data register, the following command sequence should be performed. First, the command word 88(H) would be issued to the port. In the 5 wire interface mode, this would involve activating $\overline{CS}$ low, followed by 8 SCLKs (note that SCLK must always start low and transition from low to high to latch the transmit data, and then back low again) to input the 8-bit command word. $\overline{CS}$ must be low for the serial port to recognize SCLKs during a write or a read, but it is actually the first rising SCLK during command time that gives the user control over the port. After writing the command word, the user must pause and wait until the CS5520 presents the selected register data to the serial port. The $\overline{DRDY}$ signal will fall when the data is available. When reading the conversion data register, it may take up to 112,000 XIN clock cycles for $\overline{DRDY}$ to fall after the 88(H) command word is recognized. See Figure 4 for an illustration of command and data word timing.

The conversion data register is actually the accumulator of the post-processor which computes the output data. At the end of each filter convolution cycle, the internal microcontroller checks to see if a read conversion data register command has been interpreted. If so, it transfers the accumulator result to the serial port.

Whenever registers other than the conversion data register are read, the DRDY pin will fall within 256 XIN clock cycles (62.5 µs with XIN = 4.096 MHz) after the command word is recognized. When $\overline{DRDY}$ falls, 24 SCLKs are then issued to the port to read the 24-bit output data word. $\overline{DRDY}$ will return high after all 24 bits have been clocked out. The SOD pin will be in a Hi-Z state whenever $\overline{CS}$ is high, or after all 24 output data bits have been clocked out of the port.

The CS5516/20 is designed such that it can output conversion data words continuously, without issuing a new command word prior to each data read. Under the following circumstances, continuous conversion data can be read from the port after issuing only one 88(H) command word. Once the command to read the conversion data register is issued, $\overline{DRDY}$ must be allowed to go low, after which 24 SCLKs are issued to read the data. This will cause $\overline{DRDY}$ to return high.

The converter will continue to output conversion words at the update rate as long as a different command word is not started prior to $\overline{DRDY}$ falling again. The user is not required to read every output word to remain in the continuous update mode. $\overline{DRDY}$ will toggle high, and then low as each new output word becomes available. If a command word is issued immediately after a data word is read, the converter will end the read conversion mode. Figure 5 illustrates the continuous data mode.

The user should perform all data reads and command writes within 51,000 XIN clock cycles after $\overline{DRDY}$ falls to avoid ambiguity as to who controls the serial port.

If SMODE = 1 (tied to VD+), the interface operates as a 3 wire interface using only SOD, SID, and SCLK. In the 3 wire mode $\overline{CS}$ must be tied to DGND. $\overline{DRDY}$ operates normally but is not used. Instead, the $\overline{DRDY}$ signal modifies the behavior of the SOD signal, allowing it to signal to the user when data is available. To read data from the converter requires a command word to be written to the SID pin. The SOD output is normally high (never Hi-Z). When output data is available, the SOD signal will go low. The user would then issue 8 SCLKs to the SCLK pin to clear this data ready signal. On the falling edge of the 8th SCLK the SOD pin will present the first bit of the 24-bit output word. 24 SCLKs are then issued to read the data. Then SOD will go high. SID should remain low whenever the SID pin is not being written. When reading

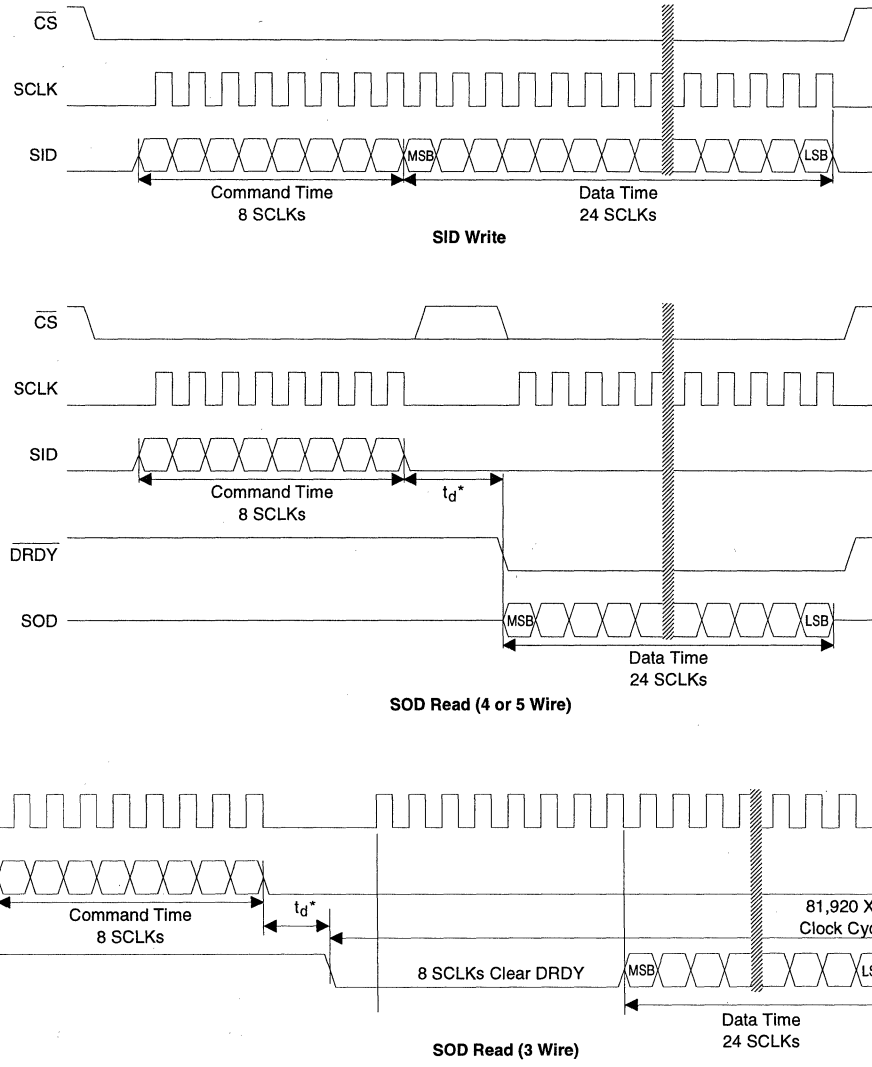


Figure 4. Command and Data Word Timing

*See text for t_d time.

SOD, SCLK cannot be continuous but must burst one clock cycle per bit.

The continuous read conversion data mode is also functional in the 3-wire interface mode. Issue one 88(H) command word to the converter. Then wait for SOD to go low. Issue 8 SCLKs to clear the data ready function. The MSB data bit will then appear on the SOD pin. Issue 24 SCLKs to read the conversion word. At the falling edge of the 24th SCLK SOD will return high. SOD will go low at the next $\overline{DRDY}$ falling time to indicate a new conversion word. Eight SCLKs must again be issued to clear the data ready function before clocking out the data conversion word. The SOD pin will continue to toggle low each time a word is available even if the conversion data is not read. To terminate the continuous conversion mode, input an 8-bit command word immediately after reading a conversion word.

The user should perform all data reads and command writes within 51,000 XIN clock cycles after SOD falls to avoid ambiguity as to who controls the serial port.

Serial Port Initialization

If for any reason the off-chip microcontroller fails to know whether the serial port of the CS5516/20 is in data mode or command mode, the following initialization procedure can be issued to the port to force the CS5516/20 into the command mode. Write 128 or more 1's to the SID pin. Then issue a single 0 to the SID pin. The port will then be initialized into the command mode and will be waiting for an 8-bit command word.

Bridge Excitation Options

The CS5516/CS5520 A/D converters are optimized for Wheatstone bridge applications. The converters support either dc or ac (switched dc) bridge excitation.

DC Bridge Excitation

The CS5516/CS5520 can be configured for dc bridge excitation in either of two ways. The EXC bit of the configuration register can be set for either internal or for external excitation. If set to internally-controlled mode (EXC = 0), the F1 and F0 bits must be set to logic 0s. In this condition, the bridge can be excited from a dc supply with a resistor divider to develop the appropriate reference voltage for the VREF+ and VREF- pins. Note that the bridge excitation should not be applied prior to the CS5516/CS5520 being powered-up. With EXC, F1, and F0 set to logic 0, the BX1 output will be

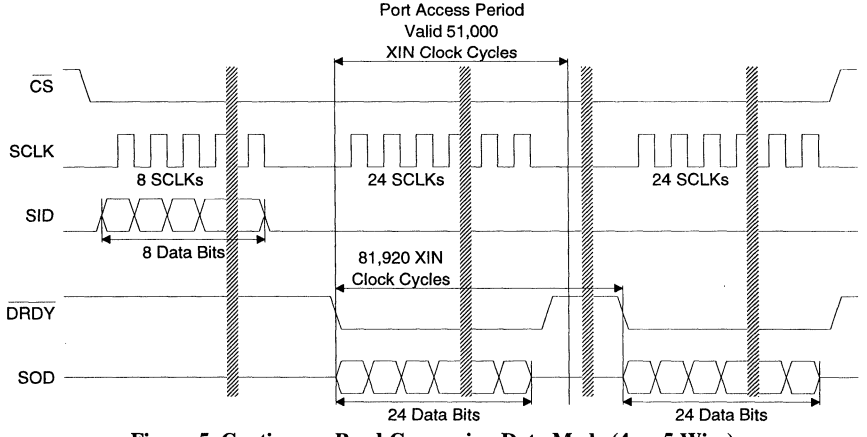


Figure 5. Continuous Read Conversion Data Mode (4 or 5 Wire)

logic 0 (0 volts) and the BX2 output will be a logic 1 (+5 volts).

A second method for configuring the converter for dc excitation is by setting EXC = 1, and pulling up BX1 (pin 12) to VD+ (pin 20) through a resistor. This sets the converter for use with external excitation which uses the BX1 pin as an input to set the excitation frequency. With BX1 = VD+, the external excitation frequency is zero, or dc.

AC Bridge Excitation

AC bridge excitation involves using a clock signal to generate a square wave which repetitively reverses the excitation polarity on the bridge. To excite the bridge dynamically requires some type of bridge driver external to the CS5516/CS5520 converter. This driver is driven by a square wave clock. The source of this clock depends upon whether the converter is set for internal excitation or for external excitation. Figure 6 illustrates a sample bridge drive circuit when operating in the internal AC excitation mode.

Using internal excitation involves setting the EXC bit of the configuration register to 0, and

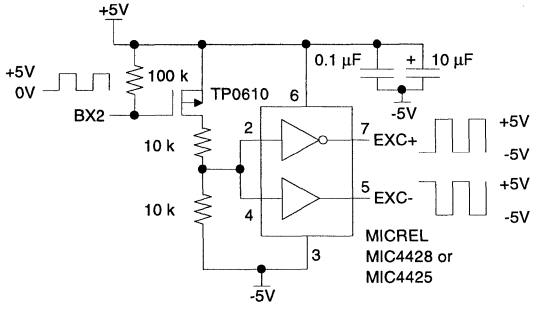
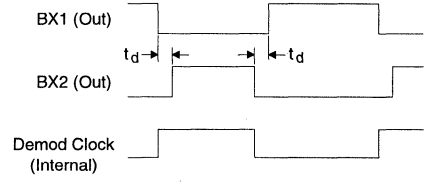


Figure 6. Sample AC Bridge Driver

setting the F1 and F0 bits to select the excitation frequency for the bridge. In this mode the excitation frequency is a sub-multiple of the XIN clock frequency. The excitation clock is output from the BX1 and BX2 pins of the converter in the form of a two-phase non-overlapping clock. The converter is capable of demodulating this clocked excitation. But only if the signals into the AIN+ and VREF+ pins of the converter are in phase with the demodulation clock inside the converter (see Figure 7). The non-overlapping clock signals from BX1 and BX2 are CMOS level outputs (0 to VD+ volts) and are capable of driving one TTL load. A buffer amplifier MUST be used to drive the bridge.

Whenever the internal mode is used for dynamic bridge excitation the signals are non-overlapping.



Note: The signals from the bridge into AIN+ and VREF+ of the converter must be in phase with the demodulation clock.
t_d is 1 cycle of XIN clock.

Figure 7. Internal Excitation Clock Phasing

The non-overlapping time is one XIN clock cycle.

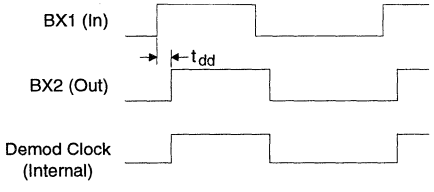
The converter can also be configured to provide dynamic bridge excitation when operating in the external-controlled bridge excitation mode. With the EXC bit of the configuration register set to logic 1, the BX1 pin becomes an input which determines the bridge excitation frequency and phase. BX1 should be near 50% duty cycle. The user can select the excitation frequency with the following restrictions. The excitation frequency must be synchronous with the XIN frequency of the converter and must be chosen using the following equation:

$$F_{exc} = (N \times XIN)/81{,}920$$

where N is an integer and lies in the range including 1 to 160. F_{exc} is the desired bridge excitation frequency. Other asynchronous frequencies are possible but may introduce a jitter component in the BX output signals. It is de-

sirable not to choose an excitation frequency where interference components are present, such as 50 Hz or 60 Hz or their harmonics. The XIN frequency can be divided down using a counter IC external to the A/D converter. F_{exc} would be input to the BX1 pin of the converter to synchronize the internal operations of the amplifiers and synchronous detection circuitry and to generate a clock output from the BX2 pin. The BX2 output is then used to drive the bridge amplifier with a signal of proper phase for detection by the converter. Figure 8 indicates the necessary phase of the signals to ensure proper demodulation.

Whenever the dynamic excitation clock output from either the BX1 and BX2 pins (during internal excitation) or from the BX2 pin (during external excitation) changes states, the converter waits 64 XIN cycles before sampling the AIN and VREF signal inputs. The delay allows some time for the signal to settle from the modulation event.



Note: The signals from the bridge into AIN+ and VREF+ of the converter must be in phase with the demodulation clock.
$t_{dd} \leq 64/XIN$

Figure 8. External Excitation Clock Phasing

Input Filtering

Some load cells are located a distance from the input to the converter. Under these conditions, separate twisted pair cabling is recommended for the excitation drive to the bridge, the excitation sense leads (if used), and for the AIN±/AIN– signal leads. If the AIN+/AIN- leads to the converter and the VREF+/VREF- leads to the converter are filtered, care should be exercised in the choice of components. With either dc or ac excitation, one should limit any input filtering resistors on AIN to below 1 kΩ. Values greater than this will degrade noise performance of the converter. In ac excitation applications, any filtering must be broadband enough that the switched dc excitation signal can settle within 10 µsecs. Failure to meet this settling requirement will affect measurement accuracy. Figure 9 illustrates acceptable filter components for ac excitation. If only differential filtering is required, a single capacitor can be placed between AIN+ and AIN- (and VREF+ and VREF-) in place of two capacitors to ground.

Voltage Reference Considerations

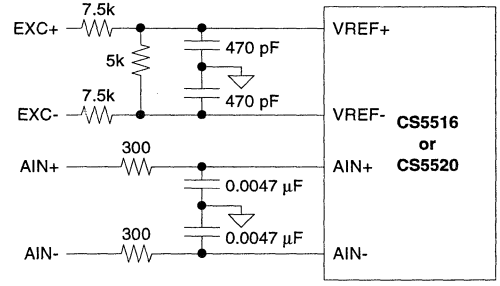


Figure 9. AIN and VREF Input Filter Components

The CS5516/20 include an on-chip voltage reference which is output on the MDRV- and referenced from the MDRV+ pin. The converter is designed to be operated as a ratiometric measurement device. The 2-channel delta-sigma converter uses the internal MDVR (Modulator Differential Voltage Reference) as its reference. Since the MDVR is used for converting both the AIN and VREF signals at the same time, the absolute value of the MDVR and its tempco are not important when the CS5516/20 is used in the ratiometric measurement mode. The voltage reference output, MDVR-, should be decoupled using a 1 µF capacitor which is connected to the MDRV+ supply line. Voltage reference decoupling is shown on the system connection diagrams.

If absolute measurements are to be made by the CS5516/20, then a precision reference should be input into the VREF+ and VREF- terminals.

Clock Generator

The CS5516/20 includes a gate which can be connected as a crystal oscillator to provide the master clock to run the chip. Alternatively, an external (CMOS compatible) clock can be input into the XIN pin. Figure 10 illustrates a simple model for the on-chip gate oscillator. The on-chip oscillator is designed to typically operate with crystal frequencies between 4.0 and 5.0 MHz without additional loading capacitors. If other crystal frequencies, or if ceramic resonators are used, additional loading capacitance may be necessary.

The XOUT pin can be used to drive one CMOS gate for system clock requirements. Be sure to include the gate's input capacitance and stray capacitance as part of the loading capacitance for the resonating element.

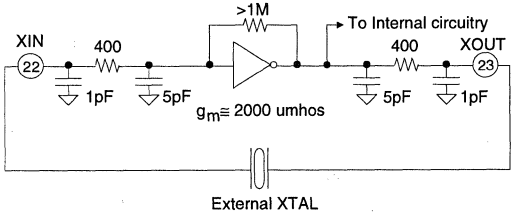


Figure 10. On-Chip Gate Oscillator Model

Digital Filter

The CS5516/20 is optimized to operate with clock frequencies of 4.096 MHz or 4.9152 MHz. These result in the filter having a 3dB bandwidth of 12 Hz or 15 Hz, with output word rates of 50 or 60Hz. The rejection at 50Hz ± 3Hz is 70 dB minimum with a 4.096 MHz clock. Similar rejection is obtained at 60 Hz with a 4.9152 MHz clock.

The digital filter has a deep notch in its transfer function at 50 Hz (XIN = 4.096 MHz) or 60 Hz (XIN = 4.9152 MHz) but other XIN frequencies can be used. The filter transfer function will scale proportionally. Figure 11 shows the transfer function of the filter when operated at three different frequencies. With a 3.579 MHz XIN, the filter offers greater than 90 dB rejection of both 50 and 60 Hz.

The output word rate of the converter scales with the XIN clock rate and is set by the ratio of XIN/81,920; or 50 Hz for XIN = 4.096 MHz. If very narrow signal bandwidths, such as 3 Hz, are desired, averaging of the output words is recommended.

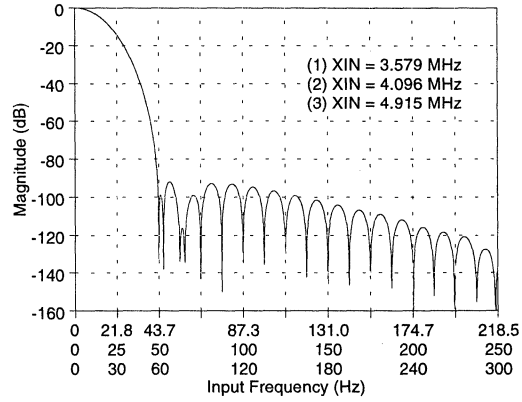


Figure 11. Filter Magnitude Response

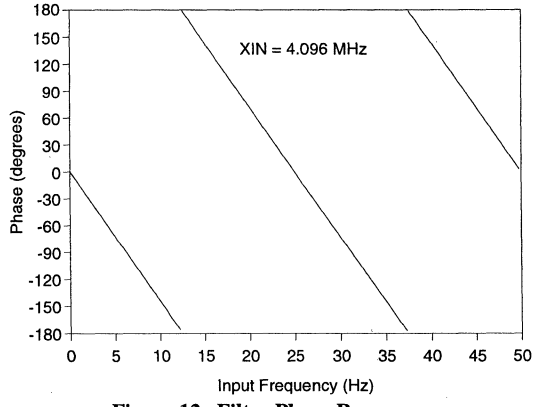


Figure 12. Filter Phase Response.

The digital filter computes a new output data word every 81,920 XIN clock cycles. If the input experiences a large change in amplitude, the PGA gain is changed, or the DAC calibration registers are changed, it may take up to six filter cycles (81,920 X 6 clock cycles) for the filter to compute an output word which is fully settled to the input signal.

Output Coding

The CS5516/20 converters output data in binary format when operating in unipolar mode and in two's complement when operating in bipolar mode. Table 5 illustrates the output coding for the converters. Note that when reading conversion data from the converter the data word is output MSB or sign bit first. Falling edges on SCLK advance the data word to the next lower bit.

The output conversion words from both the CS5516 and the CS5520 are 24 bits long. The CS5516 has 16 data bits followed by 8 flag bits (all identical). The CS5520 has 20 data bits followed by 4 flag bits (all identical). To read the conversion data, including the error flag information will require at least 17 SCLKs for the CS5516 and at least 21 SCLKs for the CS5520.

Under normal operating conditions, the flag bits will be zeroes. The flag bits will be set to all ones whenever an overrange condition exists. Under large overrange conditions where the input signal exceeds the nominal full scale input by approximately two times (for example: 50 mV input when the nominal full scale input is set-up for 25 mV), the converter may be unable to compute a proper output code. In this condition flag bits will be set to all 1s but the conversion data may be a value other than full scale plus or minus.

After the converter is first powered-up, a $\overline{\text{RST}}$ is issued, or the device comes out of the SLEEP mode, the first conversion data read may erroneously have its error flag bits set to "1".

Synchronizing Multiple Converters

Multiple converters can be made to output their conversion words at the same time if they are operated from the same clock signal at XIN. To synchronize multiple converters requires that they all have their RF bit of the configuration register written to a logic 1 and then back to 0. The filters will be allowed to start convolutions after the falling edge of the 24th SCLK used to write the RF bit to the configuration register.

Unipolar Input Voltage	Offset Binary	Bipolar Input Voltage	Two's Complement
>(VFS-1.5 LSB)	FFFF	>(VFS-1.5 LSB)	7FFF
VFS-1.5 LSB	FFFF ----- FFFF	VFS-1.5 LSB	7FFF ----- 7FFE
VFS/2-0.5 LSB	8000 ----- 7FFF	-0.5 LSB	0000 ----- FFFF
+0.5 LSB	0001 ----- 0000	-VFS+0.5 LSB	8001 ----- 8000
<(+0.5 LSB)	0000	<(-VFS+0.5 LSB)	8000

CS5516 Output Coding

Unipolar Input Voltage	Offset Binary	Bipolar Input Voltage	Two's Complement
>(VFS-1.5 LSB)	FFFFF	>(VFS-1.5 LSB)	7FFFF
VFS-1.5 LSB	FFFFF ----- FFFFE	VFS-1.5 LSB	7FFFF ----- 7FFFE
VFS/2-0.5 LSB	80000 ----- 7FFFF	-0.5 LSB	00000 ----- FFFFF
+0.5 LSB	00001 ----- 00000	-VFS+0.5 LSB	80001 ----- 80000
<(+0.5 LSB)	00000	<(-VFS+0.5 LSB)	80000

CS5520 Output Coding

Note: VFS in the table equals the full scale voltage between +VREF/(G x 25) and ground for unipolar mode; and between ±VREF/(G x 25) for bipolar mode. The signal input to the A/D section of the converter has been amplified by the instrumentation amplifier (x25) and the PGA gain, G (1, 2, 4, or 8). See text about error

Table 5. Output Coding for the CS5516/20 Converters.

The filter will start a new convolution on the next rising edge of the XIN clock after the 24th SCLK falls.

Sleep Mode

The CS5516/20 configuration register has an A/S bit which allows the users to put the device in a sleep condition to lower quiescent power. Upon reset the A/S bit device is set to a logic 0 which places the device in the 'awake' condition. Writing a 1 to the A/S bit will shutdown most of the chip, including the oscillator. It is desirable to use the following sequence when coming out of sleep. Write a logic 0 to the A/S bit of the configuration register. In the same configuration word write a logic 1 to the RF bit of the configuration register. Then wait until it is certain that the oscillator has started. After the oscillator has started or a clock present on the XIN pin, set the RF bit back to 0. The user should then wait at least 6 output word update periods before expecting a valid output data word.

Noise Performance

Typical noise performance for the converter is listed in the specification tables for each PGA gain. Figure 13 illustrates a noise histogram for 1000 output conversions from the CS5520. The data for the histogram was collected using the CDB5520 evaluation board; with VREF at 2.5 volts, PGA = 4, bipolar mode. The data shows the standard deviation of the data set is 3.2 LSBs. One LSB is equivalent to [VREF X 2(bipolar)]/ [Inst amp gain X PGA gain X number of codes] or (2.5 X 2)/ (25 X 4 X 2E20) = 47.7 nV. One standard deviation is equivalent to rms if the data is Normal or Gaussian. The rms noise presented by the plot is 153 nV, which is in good agreement with the typical noise specification of 150 nV for a PGA gain of 4.

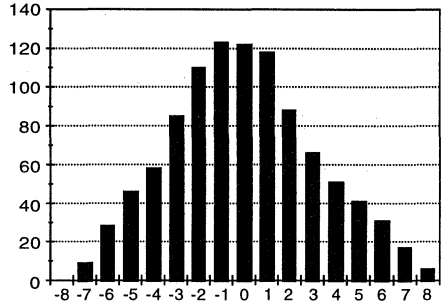
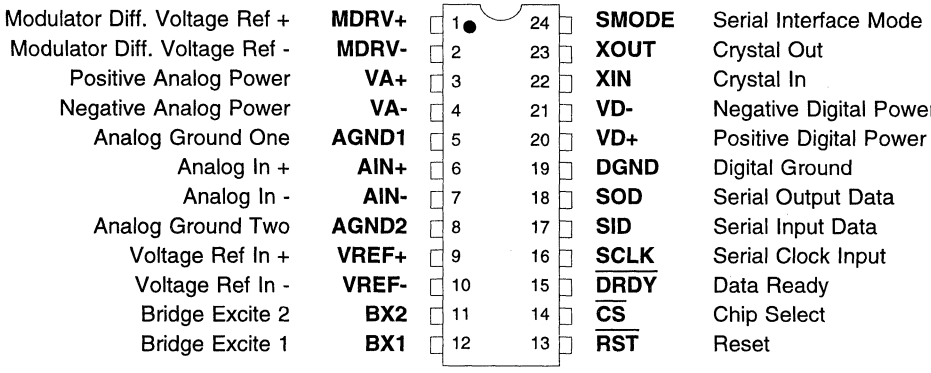


Figure 13. CS5520 Noise Histogram.

Applications

See the Application Notes section of the databook.

PIN DESCRIPTIONS



Power Supply Connections

VD+ - Positive Digital Power, PIN 20.
Positive digital supply voltage. Nominally +5 volts.

VD- - Negative Digital Power, PIN 21.
Negative digital supply voltage. Nominally -5 volts.

DGND - Digital Ground, PIN 19.
Digital ground.

VA+ - Positive Analog Power, PIN 3.
Positive analog supply voltage. Nominally +5 volts.

VA- - Negative Analog Power, PIN 4.
Negative analog supply voltage. Nominally -5 volts.

AGND1, AGND2 - Analog Ground, PINS 5, 8.
Analog ground.

Clock Generator

XIN; XOUT - Crystal In; Crystal Out, Pins 22, 23
An internal gate is connected to these pins enabling the use of either a crystal or a ceramic resonator to provide the master clock for the device. Alternatively, an external (CMOS compatible) clock can be input to the XIN pin as the master clock for the device.

Digital Inputs

$\overline{\text{RST}}$ - Reset, PIN 13.

Reset pin initializes all calibration registers to a known condition and places the serial port into the command mode.

$\overline{\text{CS}}$ - Chip Select, PIN 14.

An input which can be enabled by an external device to gain control over the serial port. When this pin is high, SOD is in a high impedance state if SMODE = 0.

SCLK - Serial Data Clock, PIN 16.

A clock signal at this pin determines the output rate of the data from the SOD pin and the input data rate on the SID pin.

SID - Serial Input Data, PIN 17.

This pin is used for inputting command and configuration words or inputting calibration words. Data is input at a rate determined by SCLK. SID is in a don't care state when no data is being clocked in.

SMODE - Serial Interface Mode, PIN 24.

Selects the operating mode of the serial port. When low the serial port operates in the 5 or 4 wire interface mode. When high the chip will enter the 3 wire interface mode.

Analog Inputs

AIN+ and AIN- - Analog Inputs, PINS 6, 7.

The analog input signals from the transducer. These are true differential inputs.

VREF+ and VREF- - Voltage Reference Inputs, PINS 9,10.

These are the differential analog reference voltage inputs.

MDRV+ - Modulator Differential Voltage Reference, PIN 1.

Positive terminal of the internal differential voltage reference which can be tied to the positive supply (VA+) or ground (AGND).

MDRV- - Modulator Differential Voltage Reference, PIN 2.

This is the -3.75V modulator differential voltage reference output and can be used to generate an analog reference. Note this is with reference to the MDRV+ pin.

Digital Outputs

BX1 and BX2 - AC Bridge Excitation Signals, PINS 12, 11.

These can be buffered to drive the transducer or used as synchronizing signals for a transducer drive circuit. BX1 and BX2 are 0 to +5V signals.

DRDY - Data Ready, PIN 15.

DRDY goes low every 81,920 cycles of XIN (when in read conversion data mode) to indicate that new data has been placed in the output port. $\overline{\text{DRDY}}$ goes high when all the serial port data is clocked out, when the serial port is being updated with new data, when a calibration is in progress, or when the device is in SLEEP.

SOD - Serial Output Data, PIN 18.

Data from the serial port will be output from this pin at a rate determined by SCLK . The data will either be conversion data, or, calibration values, dependent upon the command word that has been previously input on the SID pin. The SOD pin furnishes a high impedance output state when not transmitting data (SMODE = 0).

ORDERING GUIDE

Model Number	Linearity Error (Max)	Temperature Range	Package
CS5516-AP	0.003%	-40°C to +85°C	24-pin 0.3" Plastic DIP
CS5516-AS	0.003%	-40°C to +85°C	24-pin 0.3" SOIC
CS5520-BP	0.0015%	-40°C to +85°C	24-pin 0.3" Plastic DIP
CS5520-BS	0.0015%	-40°C to +85°C	24-pin 0.3" SOIC

SPECIFICATION DEFINITIONS

Linearity Error

The deviation of a code from a straight line which extends between two fixed points on the A/D converter transfer function. In unipolar mode, the straight line extends from one point located ½ LSB below the first code transition, one count above all zeros; to the second point located ½ LSB beyond the code transition to all ones. In bipolar mode, the straight line extends from one point located ½ LSB beyond the code transition to all ones, passing through a point ½ LSB below code 8000(H) (16-bit); 80000(H) (20-bit); extending to beyond negative full scale. Units are in percent of full-scale.

Differential Nonlinearity

The deviation of a code's width from the ideal width. Units in LSBs.

Full Scale Error

The deviation of the last code transition form the ideal [{(VREF+)-(VREF-)}-3½ LSB]. Units are in LSBs.

Unipolar Offset

The deviation of the first code transition from the ideal (½ LSB above AGND) when in unipolar mode (BP/$\overline{\text{UP}}$ low). Units are in LSBs.

Bipolar Offset

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (½ LSB below AGND) when in bipolar mode (BP/$\overline{\text{UP}}$ high). Units are in LSBs.

Semiconductor Corporation

CS5516 & CS5520 ADC Evaluation Board

Features

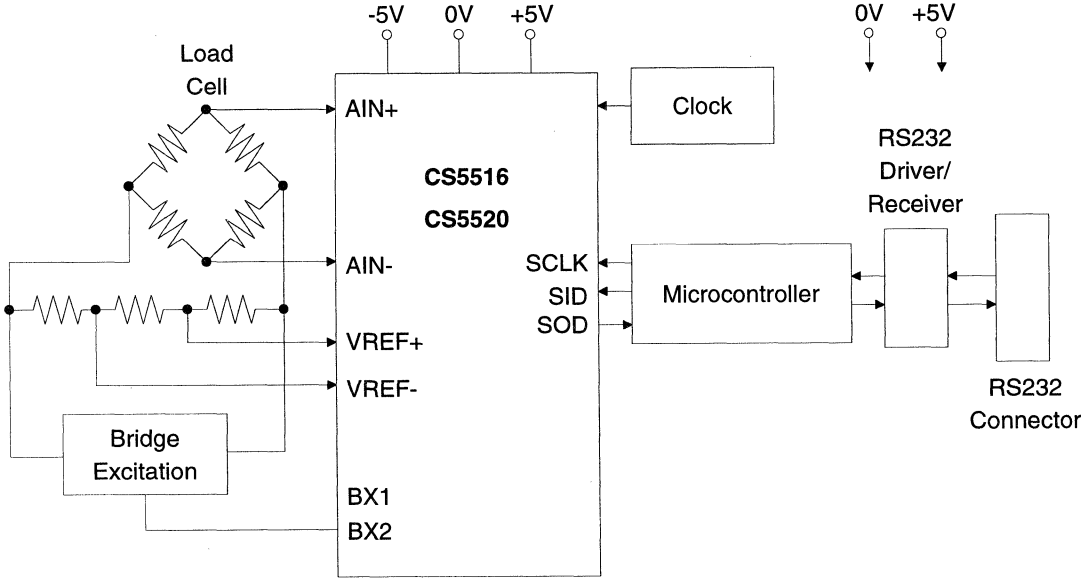
- On-board microcontroller
- RS232 Serial Communications with host PC
- Supports either AC or DC bridge drive
- On-board bridge driver
- Supports ratiometric or absolute measurements
- Evaluation software included

General Description

The CDB5516 and CDB5520 provide quick and easy evaluation of the CS5516 and CS5520 bridge transducer A/D converters. Direct connection of the bridge to the evaluation board is provided.

The board also contains a microcontroller, with firmware which allows the board to be controlled via simple serial commands, using the RS232 communications port of a PC.

ORDERING INFORMATION: CDB5516 or CDB5520



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

Introduction

The CDB5516/20 evaluation board provides a means of testing the CS5516 and CS5520 bridge transducer A/D converters. The board is designed to be interfaced to a PC-compatible computer via an RS-232 port. Software is supplied with the board which provides control of all registers in the CS5516 or the CS5520.

The board is configured to be operated from +5 and -5 volt power supplies. A bridge transducer or a bridge transducer simulator is required if the board is to be evaluated in the ratiometric operating mode.

Evaluation Board Overview

Figure 1 illustrates the schematic of the bridge driver and A/D converter portion of the circuit board. The converter operates from a 4 MHz crystal. This results in the converter outputting conversion words at a 50 Hz rate. The board comes configured to be interfaced to a bridge transducer via the 6-pin transducer terminal block. The sense lines on the transducer terminal block provide the reference voltage for the converter.

For absolute measurements, the user can connect either an external reference voltage (up to 3.8 volts) to the reference terminal block or connect the on-board 2.5 volt LT1019 reference as the voltage reference for the converter.

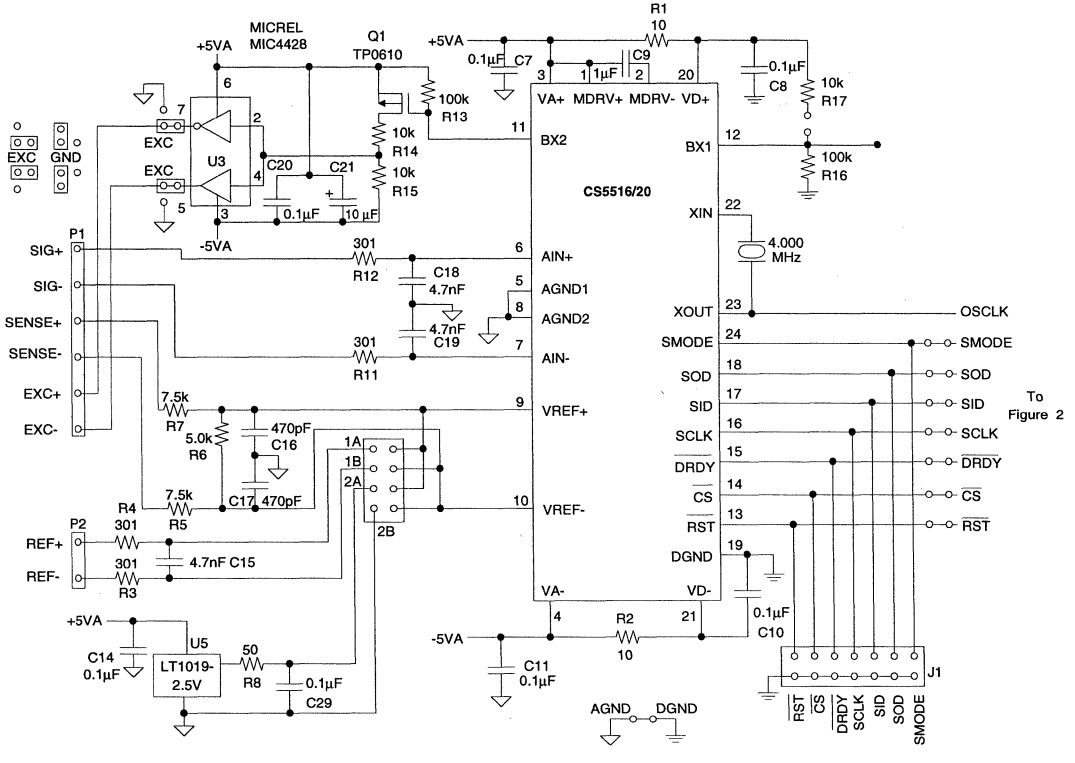


Figure 1. Bridge Driver and A/D Converter

bridge driver, composed of a Siliconix TP0610 transistor and a Micrel MIC4428 dual CMOS driver, is provided which allows the BX2 output from the CS5516 or CS5520 to provide either dc or ac excitation to the bridge.

The digital interface pins of the A/D converter connect to the microcontroller, or alternatively, these connections can be cut, or the on-board microcontroller can be removed, and the user's own microcontroller can be interfaced to J1 header connector.

Figure 2 illustrates the Motorola 68HC705C8 microcontroller which reads or writes data into the A/D converter and communicates with the PC-compatible computer via the RS-232 interface. The microcontroller derives its 4 MHz clock from the A/D converter clock. The microcontroller is configured to communicate over the RS-232 link at 4800 baud, no parity, 8-bit data, and 1 stop bit. A Motorola MC145407 RS-232 interface chip is used to send and recieve data to the PC-compatible computer via the 25-pin Sub-D connector.

Table 1 lists the commands sent to the microcontroller to write to or to read from the registers in the A/D converter. If software other than that provided with the evaluation board is used, the format of the data transmitted over the RS232 line is as follow: Write commands are com-

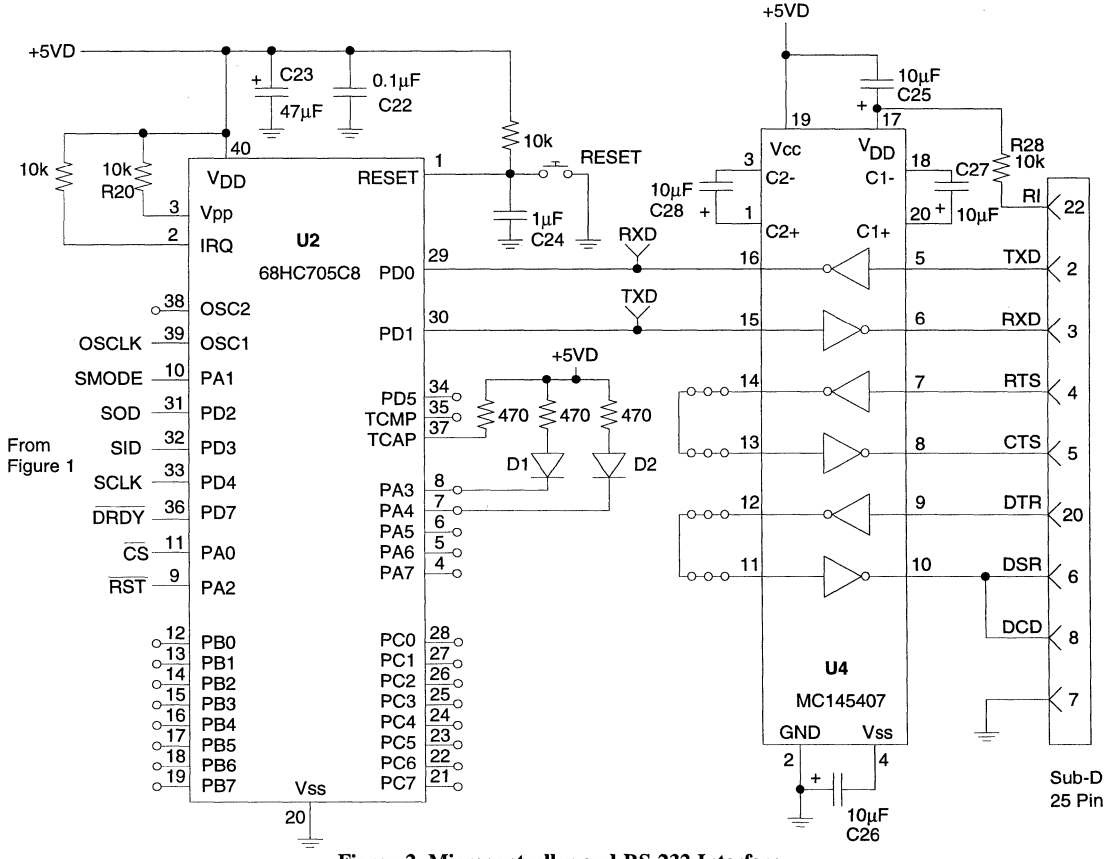


Figure 2. Microcontroller and RS-232 Interface

Register	Read	Write
Conversion Data Register	50(H)	
Configuration Register	51(H)	D1(H)
DAC Register	53(H)	D3(H)
Gain Register	52(H)	D2(H)
AIN Ratiometric Offset Register	54(H)	D4(H)
AIN Nonratiometric Offset Register	55(H)	D5(H)
VREF Nonratiometric Offset Register	56(H)	D6(H)

Table 1. Microcontroller commands via RS-232

posed of one byte for command which is transmitted with its LSB first. The command is followed by three data bytes which make up the 24-bit word to be written to the selected register of the A/D converter. The three bytes are transmitted lowest order byte first (bits 7 - 0) with the LSB of the byte transmitted first.

Figure 3 illustrates the power supply connections to the evaluation board. Voltages of +5 and -5 analog and +5 digital are required.

Using the Evaluation Board

Prior to using the board to evaluate the CS5516 or CS5520 A/D converter, a good understanding of the full potential of the converter is necessary. It is recommended that the CS5516/CS5520 device data sheet be thoroughly read prior to attempting to use the evaluation board. The CS5516 or CS5520 bridge transducer A/D converter actually contains two A/D converters. One of the converters is used to convert the VREF voltage input, and the other is used to convert the AIN signal input. Both converters utilize an on-chip voltage reference to perform conversions of their respective inputs. Since both converters use the same reference they track one another. The digital processing logic of the A/D converter depends on the presence of both signals to properly compute a digital output word. If the evaluation board is configured for bridge measurement, and no bridge (load cell or simulator) is connected to the bridge transducer terminal block, the converter will output a code of zero because no reference voltage is present between the VREF+ and VREF- pins.

The span of the AIN input signal is determined by a combination of the instrumentation amplifier gain (X25), the programmable gain amplifier (PGA) gain, the magnitude of the voltage between the VREF+ and VREF- input pins, and the calibration words for gain and offset. For exam-

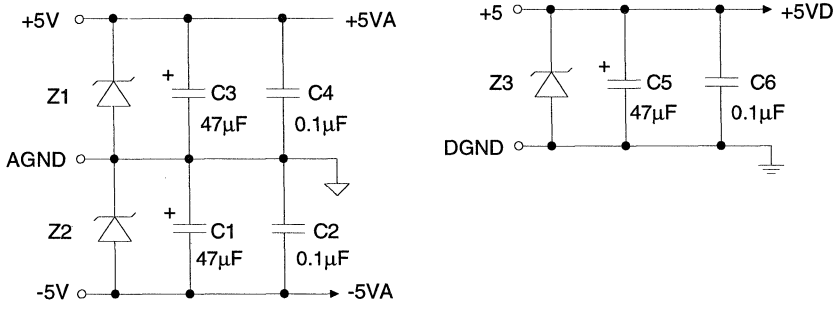


Figure 3. Power Supplies

ple, the board comes with a set of precision resistors which divide the excitation supply (nominally 10 volts total) down to 2.5 volts between the VREF+ and VREF- input pins. This sets the nominal full scale voltage into the A/D converter. The input span of the instrumentation amplifier can be calculated to by knowing the PGA gain setting, and that the gain of the instrumentation amplifier is X25. If the PGA is set for a gain of 8, then the input span to the instrumentation amplifier will be 2.5 volts (VREF+ - VREF-) divided by 8 X 25, or 2.5/(200) = 12.5 millivolt nominal in unipolar mode. The device can be then calibrated with an input voltage which is as low as 20% less than nominal or up to 20% greater than nominal. Therefore, with this VREF+ - VREF- voltage (2.5 volts) and a PGA gain of 8 the input span can be calibrated to handle a span from a low of 10 mV to a high of 15 mV. To modify the input span the user can either change the PGA gain or modify the resistor divider on the bridge sense voltage to yield an appropriate value in the range of 2.0 to 3.8 volts. This makes the A/D converter quite flexible in handling load cells with different output levels. Whenever configured as a bridge transducer device, the CS5516 or the CS5520 A/D converter operates in ratiometric measurement mode. Figures 4 and 5 illustrate how to connect 4-wire and 6-wire bridge transducers to the board.

Alternatively, the CS5516 or CS5520 can be configured for absolute measurement if a precision reference voltage is supplied between the VREF+ and VREF- pins of the A/D converter. The board can be modified to accept a reference into the voltage reference terminal block; or the on-board LT1019-2.5 volt reference can be used as the reference voltage for the A/D converter. To use either of these inputs will require that jumper wires be soldered in either 1A-1B to select the external voltage reference input, or 2A-2B to select the on-board LT1019-2.5. Figure 6 illustrates the connection of an external voltage reference to the evaluation board for absolute voltage measurement applications. To achieve an accurate reference voltage resistor R6

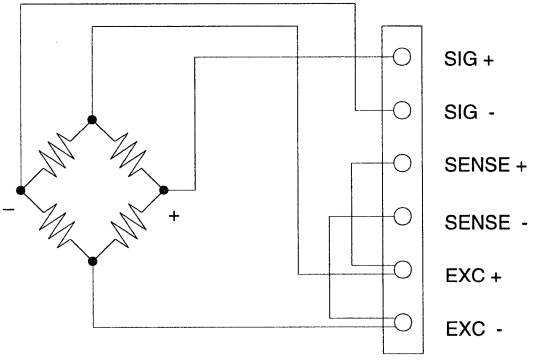


Figure 4. 4-Wire Bridge Connections

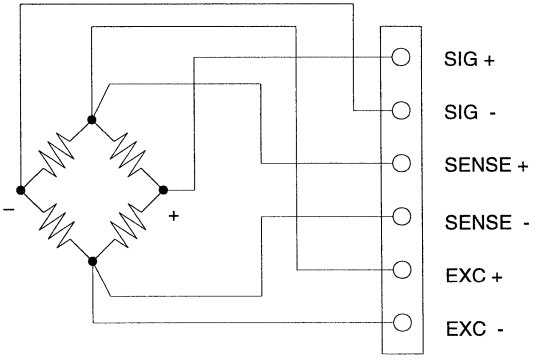


Figure 5. 6-Wire Bridge Connections

must be removed from between the +VREF and -VREF pins. It may be desirable to also remove R5, R7, C16, and C17 in some applications.

Calibrating the A/D Converter

As explained in the CS5516/CS5520 data sheet, the order in which the calibration steps are performed are important. If one chooses to use the non-ratiometric calibration capabilities of the converter, the non-ratiometric errors of the VREF and AIN channels should be calibrated first. The non-ratiometric calibration steps can be performed at the same time. Before the non-ratiometric offset calibration is initiated, the bridge should be grounded. This can be achieved on the evaluation board by moving the two jumpers at the output of the MIC4428 driver to the GND position (see Figure 1). The converter is then instructed via the configuration register bits to perform the non-ratiometric calibration steps. Once the non-ratiometric calibrations are completed, jumpers at the output of the MIC4428 driver should be returned to the EXC position.

After the non-ratiometric calibration steps are performed, the AIN ratiometric offset is then calibrated. With "zero weight" on the load cell, the converter is instructed via the configuration register to perform the AIN ratiometric offset calibration step. Finally, with "full scale weight" on the load cell, the converter is instructed to perform the gain calibration step.

The converter is then ready to perform conversions.

Software

The evaluation board comes with software and a RS-232 cable to interface the board to a RS-232 port of a PC-compatible computer. The software diskette contains a README.TXT file which explains its operation.

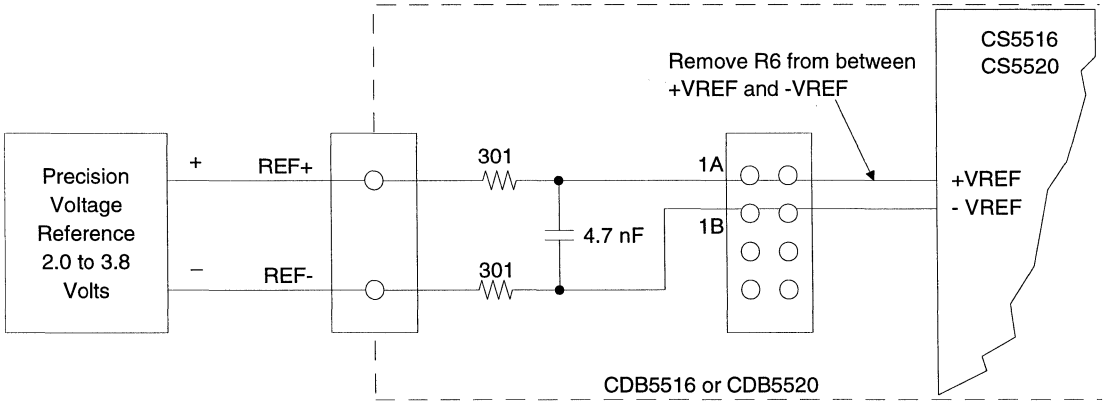


Figure 6. Using Off-board Voltage Reference

Figure 7 illustrates the software supplied with the CDB5516/CDB5520 evaluation board. The software allows the user to manipulate the registers of the converter and perform calibrations and conversions. It decodes the status of the configuration register and indicates the gain register scale factor. The software enables the user to collect data to a file, average samples and compute the average and standard deviation of the samples which have been collected.

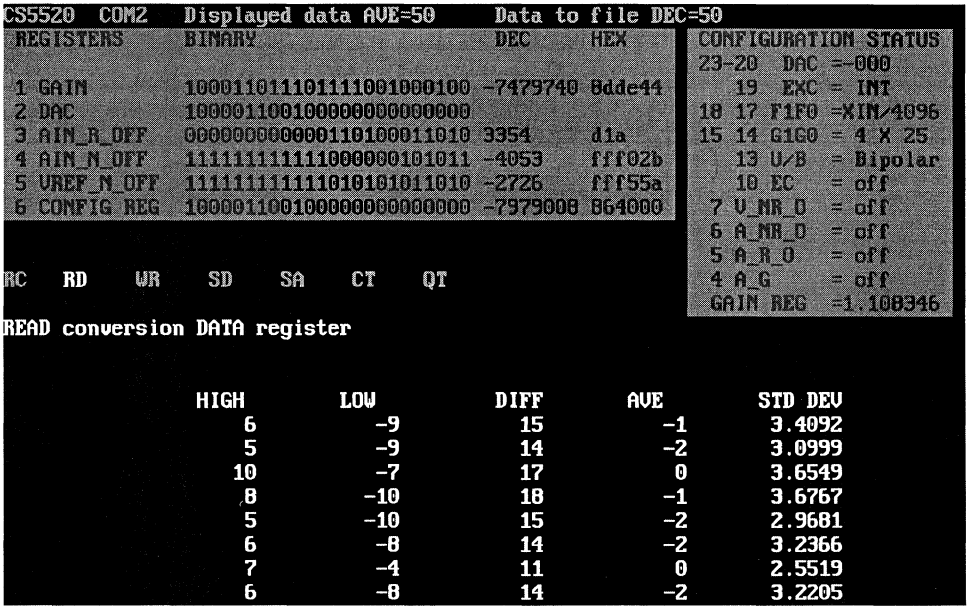


Figure 7. Screen for the CDB5516/CDB5520 Evaluation Board Software

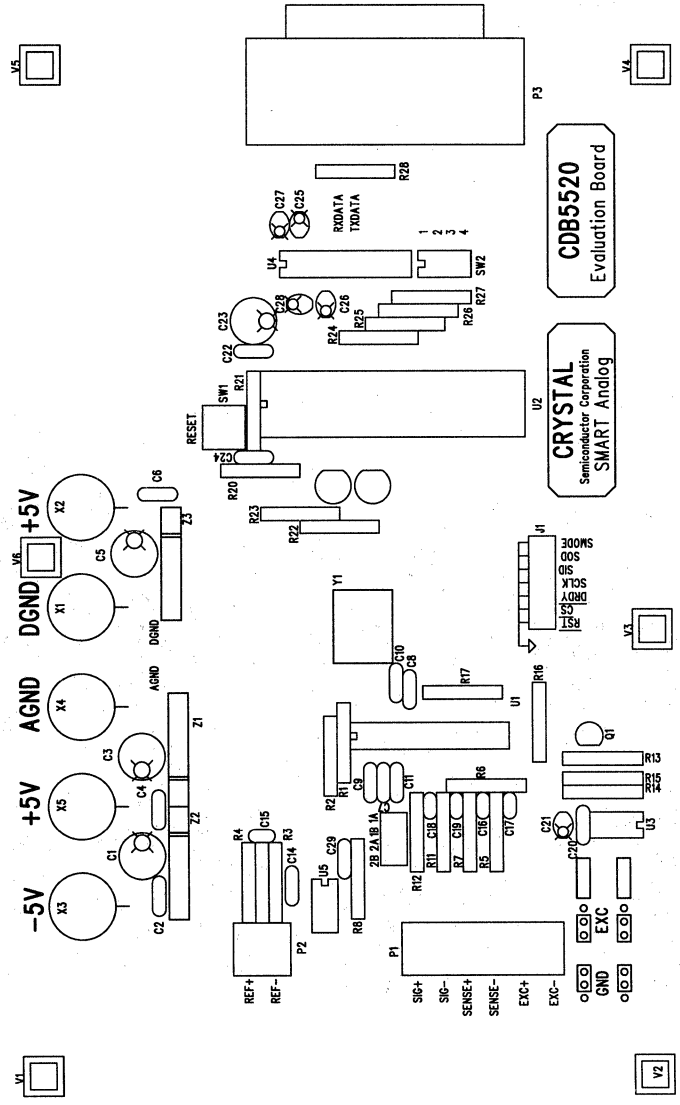


Figure 8. CDB5520 Silkscreen

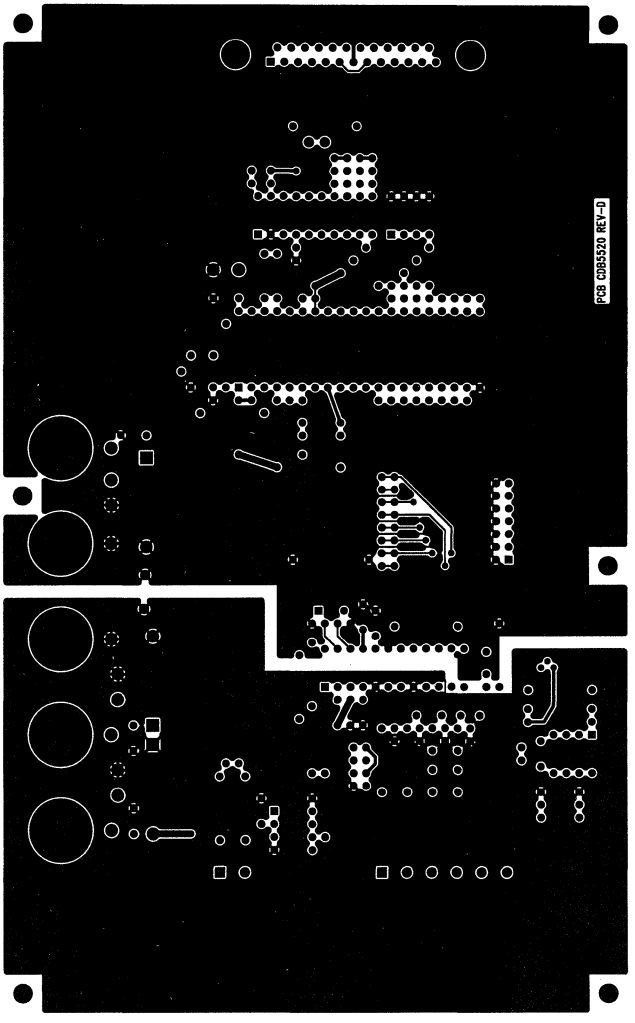


Figure 9. CDB5520 Top Ground Plane

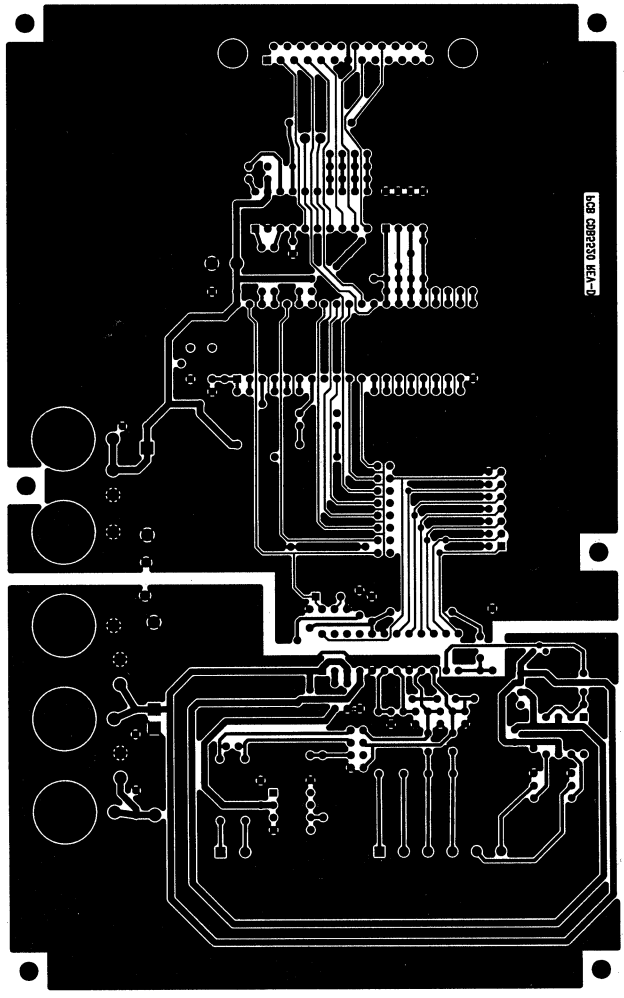


Figure 10. CDB5520 Solder Side Trace Layer

Semiconductor Corporation

CS5542

22-Bit, 2-Channel, Current-Input Modulator

2

Features

- Delta-Sigma Architecture:
  - 5th Order Modulator
  - Variable Sample Rate
  - 22-Bit Resolution
- dc Accuracy (f_{BW} = 250 Hz):
  - Integral Linearity: ± 0.001 %FS
  - Differential Linearity: ± 0.5 LSB's
  - Input Offset Noise: 1.8 pA_{RMS}
- Pin selectable input range:
  - I_{FS} = ± 806 nA
  - I_{FS} = ± 1228 nA
- Low Power: 80mW

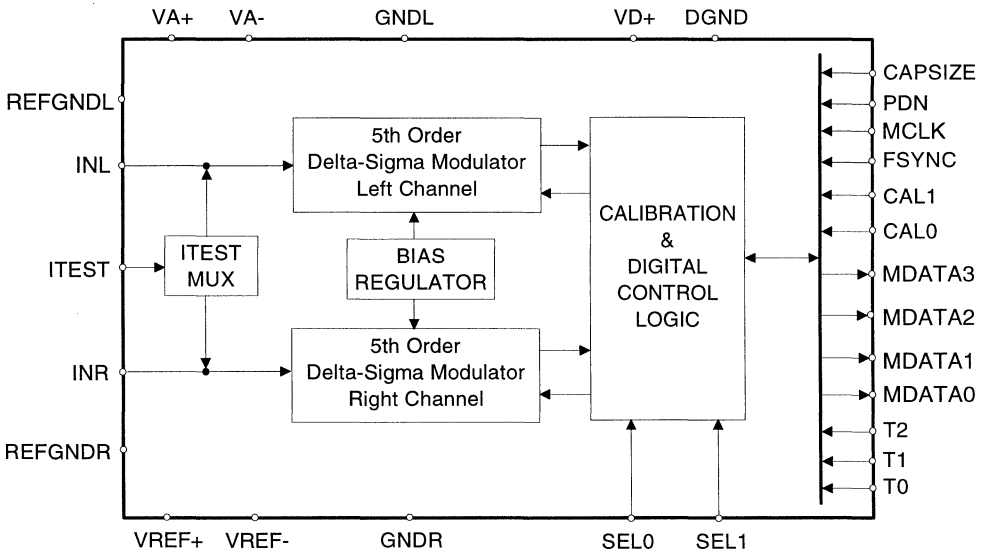
General Description

The CS5542 is a 22-Bit, 2-channel, 5th-order delta-sigma modulator intended for direct digitization of transducer currents. Up to four CS5542's may be connected together along with one CS5543 (8-channel decimation filter) to form an 8-channel data acquisition system. The CS5542 output word rate is 1000Hz per channel.

Potential applications for the CS5542 are environmental monitoring, process control systems (temperature measurement), color sensing, light measurement and control, and chemical analyzers.

The CMOS design of the CS5542 achieves high reliability while minimizing power dissipation. The device is supplied in a 28-pin PLCC package.

For more information contact Crystal Semiconductor



Product Preview

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

• Notes •

Semiconductor Corporation

CS5543

8-Channel Digital Decimation Filter

Features

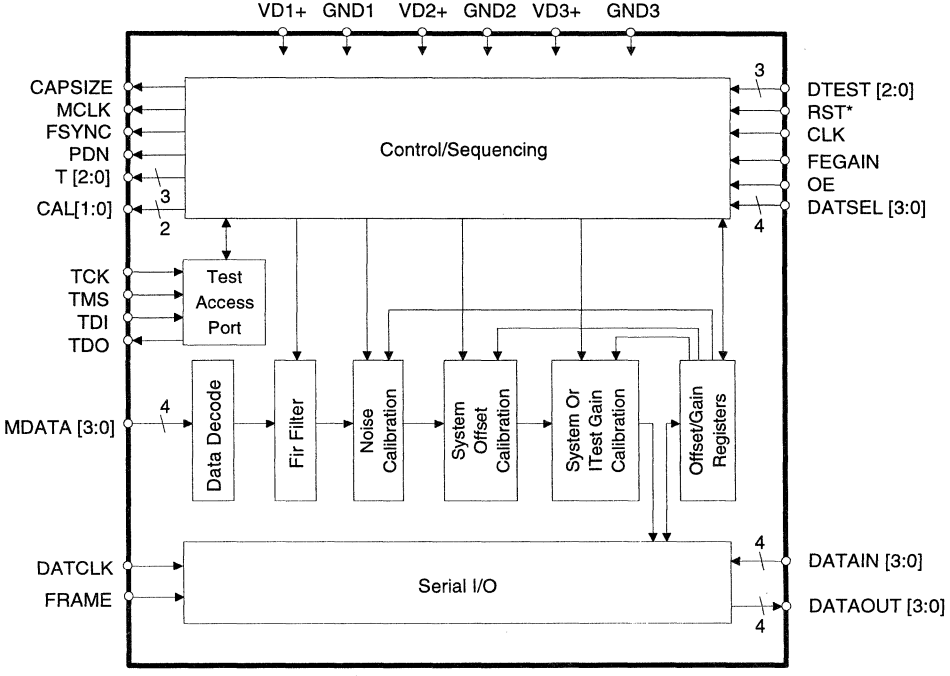
- 8-Channel Digital FIR Filter
- Pipelined Output Data Transmission Rates up to 9.6MHz
- Stop-band Attenuation: >120dB
- Self-calibration of Noise, Offset and Gain
- JTAG Boundary-Scan Capability
- Serial Digital Interface
- Low Power : 75mW

General Description

The CS5543 is a monolithic CMOS, 8-channel digital FIR filter designed to be used with four CS5542 (2-channel, 22-Bit modulator) to form an 8-channel data acquisition system. The CS5543 has four I/Ocontrol modes: normal operation, read/write calibration registers, tri-stating output pins, and test pattern generation. JTAG Boundary-scan capability is available in the CS5543 to facilitate self-test at the system level.

The CS5543 is supplied in a 44-pin PLCC package.

For more information contact Crystal Semiconductor



Product Preview

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

• Notes •

12-Bit, 100 kHz, Sampling A/D Converters

Features

- Mónolithic CMOS A/D Converter
  - 2 µs Track/Hold Amplifier
  - 8 µs A/D Converter
  - 3 V Voltage Reference
  - Internal Clock
  - Parallel, Serial and Byte Outputs
- 12-Bit ADC and Reference Accuracy
  - Linearity: 0.5 LSB
  - SINAD: 72 dB
- Input Ranges
  - ±3 V for CS7870
  - 0 to +5 V for CS7875
- Low Power: 88 mW

General Description

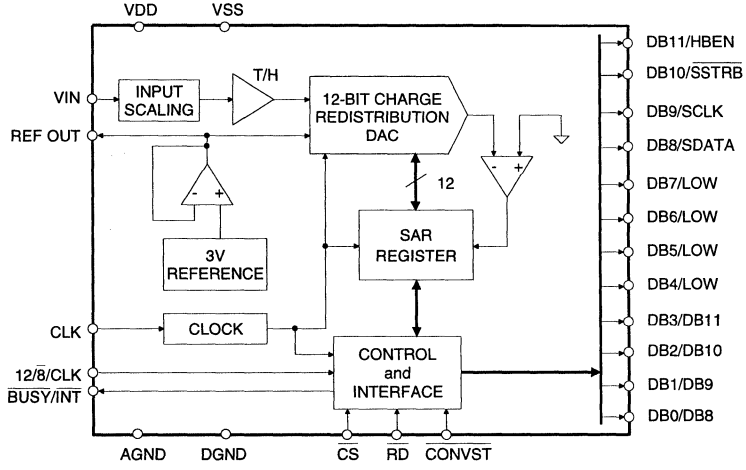
The CS7870 and CS7875 are complete monolithic CMOS analog-to-digital converters providing 100kHz throughput. The capacitive DAC has been calibrated at the factory to ensure 12-bit performance.

The CS7870/CS7875 have a high speed digital interface with three-state data outputs and standard control inputs allowing easy interfacing to common microprocessors and digital signal processors. Conversion results are available in either 12-bit parallel, two 8-bit bytes, or serial data.

The CS7870/CS7875 are available in a 24-pin, 0.3" plastic dual-in-line package (PDIP) or Cerdip. The CS7870 and CS7875 are also available in a 28-pin PLCC package.

The CS7870/CS7875 are pin compatible replacements for the AD7870/7875 with equal or better performance.

ORDERING INFORMATION: Page 2-585



Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

ANALOG CHARACTERISTICS (V_{DD} = +5V±5%; V_{SS} = -5V±5%; AGND = DGND = 0V; CLK = 2.5 MHz, unless otherwise specified. T_A = T_{MIN} to T_{MAX})

Parameter*		Symbol	B Min	B Typ	B Max	S Min	S Typ	S Max	Units
Specified Temperature Range	(Note 1)		-40 to +85			-55 to +125			°C
Dynamic Performance	***(Note 2)***								
Signal-to-Noise-and-Distortion	(Note 3)	SINAD	-	72.8	-	-	72.8	-	dB
Signal-to-Noise Ratio		SNR	-	73	-	-	73	-	dB
Total Harmonic Distortion	(Note 4)	THD	-80	-	-	-80	-	-	dB
Spurious-Free-Dynamic-Range	(Note 4)	SFDR	-80	-	-	-80	-	-	dBc
Intermodulation Distortion	(Note 5)	IMD							
Second Order Terms			-80	-	-	-80	-	-	dBc
Third Order Terms			-80	-	-	-80	-	-	dBc
Accuracy									
Integral Nonlinearity		INL	-	0.25	0.5	-	0.25	0.5	LSB
Differential Nonlinearity		DNL	-	-	0.5	-	-	0.5	LSB
Unipolar Offset Error	(CS7875)	VOS_U	-	0.5	1.0	-	0.5	1.0	LSB
Bipolar Zero Error	(CS7870)	VOS_B	-	0.5	1.0	-	0.5	1.0	LSB
Positive Full Scale Error	(Note 6)	FSE_P	-	0.5	1.0	-	0.5	1.0	LSB
Biploar Negative Full Scale Error	(Note 6) (CS7870)	FSE_N	-	0.5	1.0	-	0.5	1.0	LSB
Analog Input									
Input Voltage Range	(CS7870)	V_{IN}	-3	-	3	-3	-	3	V
	(CS7875)		0	-	5	0	-	5	V
Input Current			-	-	500	-	-	500	µA
Aperture Delay		t_{apd}	-	25	-	-	25	-	ns
Aperture Jitter		t_{apj}		100	-	-	100	-	ps

Notes:
1. All parameters guaranteed by design, test, and/or characterization.
2. V_{IN} = ±3Vpp for CS7870, and 0V to +5V for CS7875.
3. V_{IN} = 10kHz Sine Wave, f_{SAMPLE} = 100kHz. Typically 71.5dB for 10kHz<V_{IN}<50kHz.
4. V_{IN} = 10kHz Sine Wave, f_{SAMPLE} = 100kHz. Typically -80dBc for 0<V_{IN}<50kHz.
5. fa = 9kHz, fb = 9.8kHz, f_{SAMPLE} = 100kHz.
6. Measured with respect to internal reference and includes bipolar offset error.

* Parameter definitions are given at the end of this datasheet prior to the package outline information.

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	B Min	B Typ	B Max	S Min	S Typ	S Max	Units
Specified Temperature Rnage		-40 to +85			-55 to +125			°C
Reference Output								
Output Voltage	V_R	2.99	-	3.01	2.99	-	3.01	V
REF OUT Tempco		-	-	60	-	-	60	ppm/°C
Load Regulation (Note 7)	$\Delta V_R/\Delta I$	-	0.6	1	-	0.6	1	mV
Output Noise Voltage	eN	-	100	-	-	100	-	μV_{rms}
Output Current Drive Source Current	I_{SOURCE}	-	500	-	-	500	-	µA
Sink Current	I_{SINK}	-	500	-	-	500	-	µA
Conversion & Throughput								
Conversion Time	t_{conv}							
External Clock (CLKIN = 2.5 MHz)		-	-	8	-	-	8	µs
Internal Clock		7	-	9	7	-	9	µs
Acquisition Time	t_{acq}	-	-	2	-	-	2	µs
Throughput	f_{tp}	100	-	-	100	-	-	kHz
Power Supplies								
Positive Supply Current	I_{DD}	-	6.0	10.0	-	6.0	10.0	mA
Negative Supply Current	I_{SS}	-	5.0	7.5	-	5.0	7.5	mA
Power Dissipation	PD	-	-	88	-	-	88	mW

Notes: 7. Reference Load Current Change (0-500 µA). Reference Load should not be changed during conversion.

LSB	%FS	ppm FS	mV
0.25	0.0061	61	0.37
0.50	0.0122	122	0.73
1.00	0.0244	244	1.46
2.00	0.0488	488	2.92
4.00	0.0976	976	5.86

CS7870 Unit Conversion Factors: (V_{IN} = ±3V)

LSB	%FS	ppm FS	mV
0.25	0.0061	61	0.31
0.50	0.0122	122	0.61
1.00	0.0244	244	1.22
2.00	0.0488	488	2.44
4.00	0.0976	976	4.88

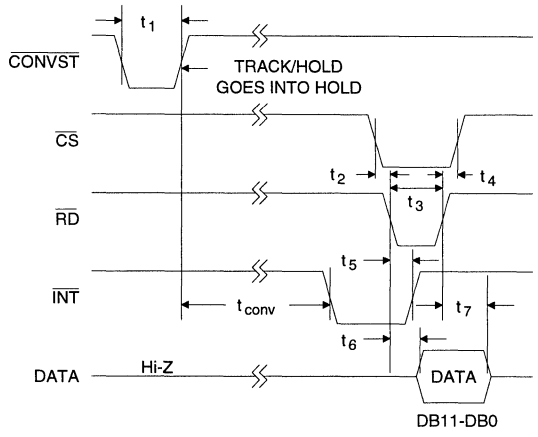
CS7875 Unit Conversion Factors: (V_{IN} = 0 to 5V)

SWITCHING CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; V_{DD} = +5V±5%, V_{SS} = -5V±5%; AGND = DGND = 0V, (Note 8))

Parameter		Symbol	B Min	B Typ	B Max	S Min	S Typ	S Max	Units
Specified Temperature Range			-40 to +85			-55 to +125			°C
CLKIN	Period	t_{clk}	370	-	-	370	-	-	ns
CLKIN	Low Time	t_{clkl}	0.4	-	0.6	0.4	-	0.6	MCC*
	High Time	t_{clkh}	0.4	-	0.6	0.4	-	0.6	MCC*
Rise Times	Any Digital Input	t_{rise}	-	-	20	-	-	20	ns
	Any Digital Output	t_{rise}	-	20	-	-	20	-	ns
Fall Times	Any Digital Input	t_{fall}	-	-	20	-	-	20	ns
	Any Digital Output	t_{fall}	-	20	-	-	20	-	ns
Mode 1 Timing									
Conversion Time		t_{conv}	-	-	20	-	-	20	MCC*
$\overline{CONVST}$ Pulse Width		t_1	50	-	-	50	-	-	ns
$\overline{CS}$ to $\overline{RD}$ Setup Time		t_2	0	-	-	0	-	-	ns
$\overline{RD}$ Pulse Width		t_3	60	-	-	75	-	-	ns
$\overline{CS}$ to $\overline{RD}$ Hold Time		t_4	0	-	-	0	-	-	ns
$\overline{RD}$ to $\overline{INT}$ Delay		t_5	-	-	70	-	-	70	ns
Data Access Time after $\overline{RD}$	(Note 9)	t_6	-	-	57	-	-	70	ns
Output Float Delay $\overline{RD}$ Rising to Hi-Z	(Note 10)	t_7	5	-	50	5	-	50	ns
HBEN to $\overline{RD}$ Setup Time		t_8	0	-	-	0	-	-	ns
HBEN to $\overline{RD}$ Hold Time		t_9	0	-	-	0	-	-	ns
Serial Clock Timing									
SCLK to $\overline{SSTRB}$ Falling Time	(Note 11)	t_{10}	100	-	-	100	-	-	ns
Serial Clock	Pulse Width High	t_{pwh}	0.4	-	0.6	0.4	-	0.6	MCC*
	Pulse Width Low	t_{pwl}	0.4	-	0.6	0.4	-	0.6	MCC*
SCLK rising to Valid Data	(Note 12)	t_{12}	-	-	135	-	-	150	ns
SCLK rising to $\overline{SSTRB}$		t_{13}	20	-	100	20	-	100	ns
Bus relinquish time after SCLK		t_{14}	10	-	100	10	-	100	ns

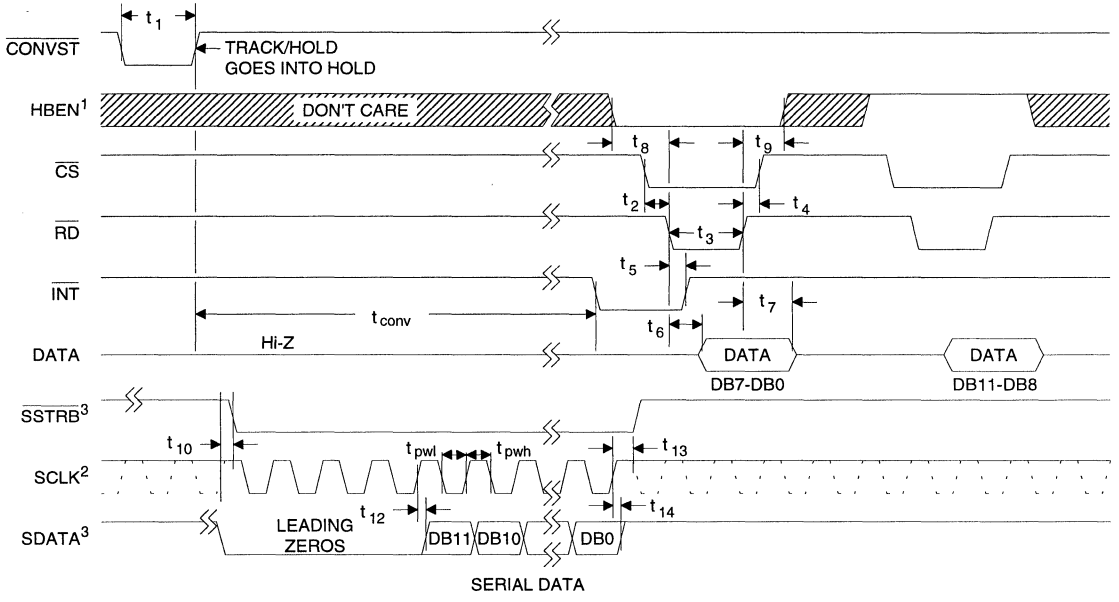
*MCC = Master Clock Cycles, 1 MCC = t_{clk}

Notes:
8. All input signals are specified with $t_{rise} = t_{fall}$ = 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.
9. Measured with the load circuits of Figure 5 and defined as the time required for an output to cross 0.8V or 2.4V.
10. Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 6.
11. t_{10} = MCC/2 - 25ns. t_{10} = 175ns for t_{clk} = 400ns.
12. CL = 35pF. SDATA will drive higher capacitive loads but this will add to t_{12}.



Note: 12/$\overline{8}$/CLK = +5V.

Figure 1. Mode 1 Timing Diagram, 12-Bit Parallel Read



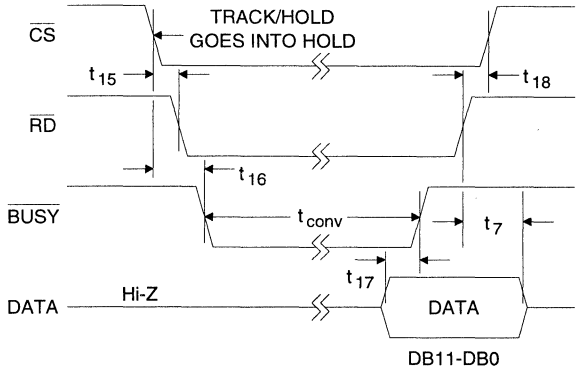
Notes:
1. Times t_2, t_3, t_4, t_8, and t_9 are the same for a high byte read as for a low byte read.
2. Continuous SCLK (Dashed line) when 12/$\overline{8}$/CLK = -5V
   Noncontinuous when 12/$\overline{8}$/CLK = 0V
   External 2kΩ pull-up resistor.
3. External 4.7kΩ pull-up resistor.

Figure 2. Mode 1 Timing Diagram, Byte or Serial Read

SWITCHING CHARACTERISTICS (Continued)

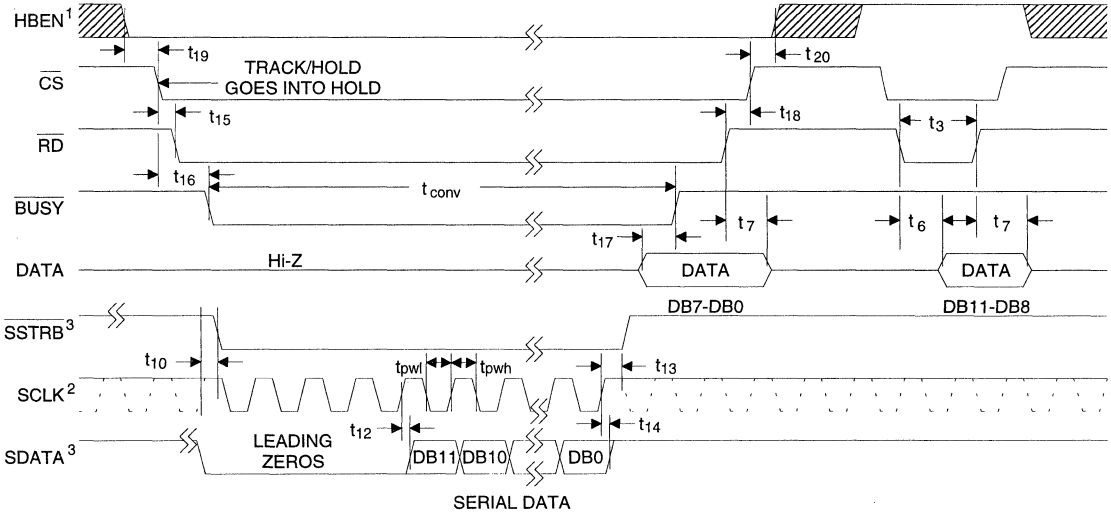
Parameter	Symbol	B Min	B Typ	B Max	S Min	S Typ	S Max	Units
Specified Temperature Range		-40 to +85			-55 to +125			°C
Mode 2 Timing								
Conversion Time	t_{conv}	-	-	20	-	-	20	MCC*
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{15}	60	-	-	60	-	-	ns
$\overline{CS}$ to Busy Delay	t_{16}	-	-	120	-	-	120	ns
Data Setup Time	t_{17}	200	-	-	200	-	-	ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{18}	0	-	-	0	-	-	ns
Output Float Delay $\overline{RD}$ Rising to Hi-Z (Note 10)	t_7	5	-	50	5	-	50	ns
HBEN to $\overline{CS}$ Setup Time	t_{19}	0	-	-	0	-	-	ns
HBEN to $\overline{CS}$ Hold Time	t_{20}	0	-	-	0	-	-	ns
$\overline{RD}$ Pulse Width	t_3	60	-	-	75	-	-	ns
Data Access Time after $\overline{RD}$ (Note 9)	t_6	-	-	57	-	-	70	ns
Serial Clock Timing								
Serial Clock Pulse Width High	t_{pwh}	0.4	-	0.6	0.4	-	0.6	MCC*
Pulse Width Low	t_{pwl}	0.4	-	0.6	0.4	-	0.6	MCC*
SCLK to $\overline{SSTRB}$ Falling Time (Note 11)	t_{10}	100	-	-	100	-	-	ns
SCLK rising to Valid Data (Note 12)	t_{12}	-	-	135	-	-	150	ns
SCLK rising to $\overline{SSTRB}$	t_{13}	20	-	100	20	-	100	ns
Bus relinquish time after SCLK	t_{14}	10	-	100	10	-	100	ns

*MCC = Master Clock Cycles, 1 MCC = t_{clk}



Note: 12/$\overline{8}$/CLK = +5V.

Figure 3. Mode 2 Timing Diagram, 12-Bit Parallel Read



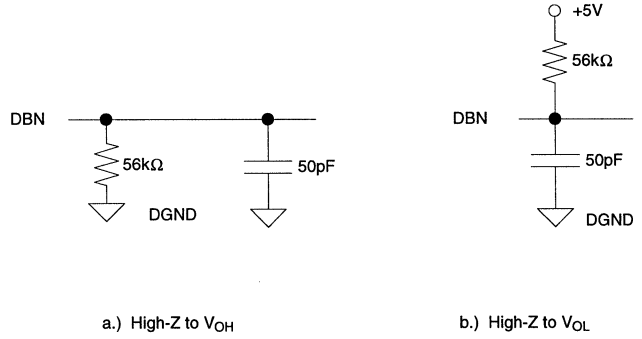
Notes:
1. Times t_{15}, t_{18}, t_{19}, and t_{20} are the same for a high byte read as for a low byte read.
2. Continuous SCLK (Dashed line) when 12/$\overline{8}$/CLK = -5V
   Noncontinuous when 12/$\overline{8}$/CLK = 0V
   External 2kΩ pull-up resistor.
3. External 4.7kΩ pull-up resistor.

Figure 4. Mode 2 Timing Diagram, Byte or Serial Read

DIGITAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}: V_{DD} = 5V±5%; V_{SS} = -5V±5%)

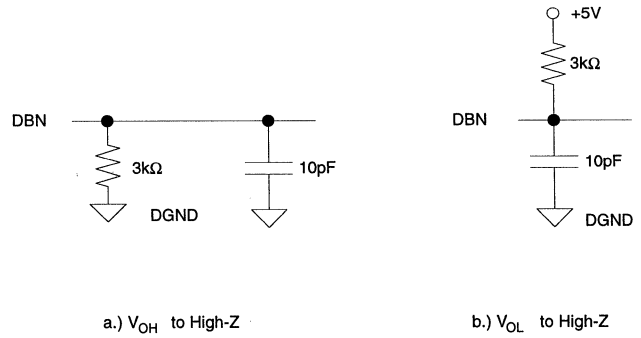
Parameter		Symbol	Min	Typ	Max	Units
Logic Inputs						
High-Level Input Voltage		V_{IH}	3.3	-	-	V
Low-Level Input Voltage		V_{IL}	-	-	0.8	V
Input Leakage Current		I_{in}	-	-	50	µA
Input Capacitance		C_{in}	-	-	10	pF
Logic Outputs						
High-Level Output Voltage	(Note 13)	V_{OH}	4.0	-	-	V
Low-Level Output Voltage	(Note 14)	V_{OL}	-	-	0.4	V
DB11-DB0 Floating State Leakage Current		I_{OZ}	-	-	50	µA
DB11-DB0 Output Capacitance		C_{out}	-	-	15	pF

Notes: 13. I_{SOURCE} = -40 µA
14. I_{SINK} = 1.6 mA



a.) High-Z to V_{OH} b.) High-Z to V_{OL}

Figure 5. Load Circuits for Access Time



a.) V_{OH} to High-Z b.) V_{OL} to High-Z

Figure 6. Load Circuits for Output Float Delay

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V. All voltages with respect to ground)

Parameter		Symbol	Min	Typ	Max	Units
Positive Analog Supply		VA+	4.75	5.0	5.25	V
Negative Analog Supply		VA-	-4.75	-5.0	-5.25	V
Analog Input Voltage	CS7870	V_{IN}	-3	-	+3	V
	CS7875	V_{IN}	0	-	+5	V
12/$\overline{8}$/CLK Input Voltage Range			VA-, 0V, VA+			V
CLKIN Input Voltage Range			0	-	VA+	V
Other Digital Input Voltage Ranges			0	-	VA+	V
AGND to DGND Voltage Differential			-	-	10	mV
Eternal Clock Frequency			-	2.5	-	MHz

ABSOLUTE MAXIMUM RATINGS (AGND = 0V, All voltages with respect to ground)

Parameter		Symbol	Min	Typ	Max	Units
Positive Analog Supply		VA+	-0.3	-	6.0	V
Negative Analog Supply		VA-	0.3	-	-6.0	V
Analog Input Voltage		V_{IN}	(VA-)-0.3	-	(VA+)+0.3	V
12/$\overline{8}$/CLK Input Voltage Range			(VA-)-0.3	-	(VA+)+0.3	V
CLKIN Input Voltage Range			(VA-)-0.3	-	(VA+)+0.3	V
Other Digital Input Voltage Ranges			-0.3	-	(VA+)+0.3	V
REF OUT Current			-	-	10	mA
Sustained Digital Output Current			-	-	5	mA
AGND to DGND Voltage Differential			-	-	100	mV
Operating Temperature Range	CS7870/75-BP/BL		-40	-	+85	°C
	CS7870/75-SD		-55	-	+125	°C
Storage Temperature Range			-65	-	+150	°C
Lead Solder Temperature			-	-	+300	°C

* WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

NOTE: Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

GENERAL DESCRIPTION

The CS7870 and CS7875 are complete 12-bit 100 kSPS sampling ADCs, utilizing a successive approximation architecture. Factory calibration ensures 12-bit conversion accuracy over industrial and military temperature ranges. The CS7870 analog input range is ±3 V (0 V to +5 V for the CS7875), with the output data provided in parallel, byte or serial formats. The internal capacitor array DAC acts as an inherent sample-and-hold, and forms the heart of the CS7870/CS7875. The on-chip +3 V reference is available at the REFOUT pin. An on-board 2.5 MHz clock oscillator is also available.

OPERATIONAL OVERVIEW

Track-and-Hold Operation

Track-and-hold operation within the CS7870/CS7875 is transparent to the user. The capacitor array DAC acts as the hold capacitor. During tracking mode all elements of the capacitor array DAC are switched to the analog input for charging. The load capacitance of the entire array during tracking mode is typically 5 pF. The input bandwidth of the track-and-hold is typically 2 MHz. The ADC goes into hold mode on the rising edge of $\overline{\text{CONVST}}$.

Capacitor Array DAC Calibration

To achieve 12-bit accuracy from the capacitor array DAC, the CS7870/CS7875 uses a novel calibration scheme. Each bit capacitor consists of several capacitors that are trimmed to optimize the overall bit weighting with an internal resolution of 14-bits, resulting in nearly ideal differential and integral linearity.

The calibration coefficients for the capacitive bit weights are stored in an on-chip EEPROM during the factory calibration. When the converter is subsequently powered-up these coefficients are applied to the capacitor array DAC. With the DAC calibration provided automatically on power-up, it is unnecessary to calibrate the DAC before using the converter. Additionally, the low temperature coefficient of the capacitor array easily maintains 12-bit accuracy over the full temperature range without recalibration.

Reference Operation

The reference voltage is available at the REF OUT pin and is capable of sourcing 500 µA to peripheral devices. This pin should normally be left open. If used, it can be directly decoupled to AGND with up to 50 pF of capacitance, or through a 200 Ω resistor to a +10 µF tantalum capacitor. The reference voltage is calibrated on power-up, with full accuracy achieved after 1.1 sec.

Analog Input

The CS7870 provides a ±3 V analog input voltage range (0 V to +5 V for the CS7875). The equivalent analog input circuit is illustrated in Figure 7 (shown in track mode). During hold mode the input impedance to the device is typically 10 MΩ, and the various elements of the capacitor array DAC are connected to either AGND or VREF. In switching back from hold mode to track mode, some elements in the capacitor array must be charged by the analog input. For the CS7870, the worst case charging current occurs when the analog input changes from +3V to -3V (+5V to 0V for the CS7875).

To ensure that the capacitor array DAC has settled to within 0.25 LSB during the allowed acquisition time, the source resistance should be less than 4 kΩ.

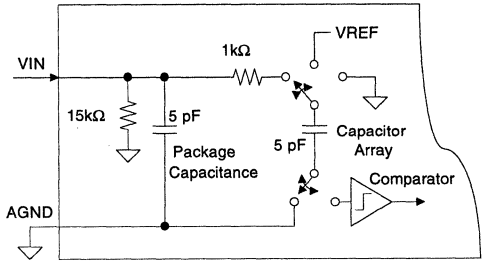


Figure 7. Analog Input Model (Track Mode).

Output Coding

The digital output coding ...

CS7870 Input	2's Complement Output		
+3V	0111	1111	1111
0V	0000	0000	0000
-3V	1000	0000	0000

CS7875 Input	Binary Output		
+5V	1111	1111	1111
+2.5V	111	1111	1111
0V	0000	0000	0000

High-Speed System Clock

The CS7870/CS7875 employs a high-speed clock (typically 2.5 MHz) to control internal operations. This high-speed clock can be generated internally with the on-board oscillator, or it can be supplied from an external CMOS source. Connecting a CMOS clock signal to the CLKIN pin allows the converter to operate from an external clock. Alternatively, connecting the CLKIN pin to VA- activates the internal clock oscillator.

External Clock.....CLKIN = External Clock Source
Internal Clock ... CLKIN = VA-

Digital Output Formats

The CS7870/CS7875 provides three digital output formats. These include 12-bit parallel, two 8-bit bytes, and serial modes. The output data format is controlled by the level applied to the 12/$\overline{8}$/CLK pin.

Figure 8 shows the schematic for the CS7870/CS7875 in 12-bit parallel mode. The twelve bits of data are output simultaneously on DB11/(MSB) through DB0 (LSB)..

12/$\overline{8}$/CLK	Digital Outputs
+VA	12-Bit Parallel
GND	Byte; Serial w/Non-Continuous SCLK
-VA	Byte; Serial /Continuous SCLK

In byte mode, two 8-bit read operations (four leading zeros with 4 data bits ... plus 8 more data bits) are required to collect the data as shown in Figure 9. In byte mode, the DB11/HBEN pin defers to the HBEN function, selecting the high or low byte of data to be read from the ADC. The lower eight bits of data are placed on the data bus when HBEN is held low. To access the four MSBs of data, HBEN must be held high. The 4 MSBs of the 12-bit data word are right justified with zeros in the upper nibble of the high byte.

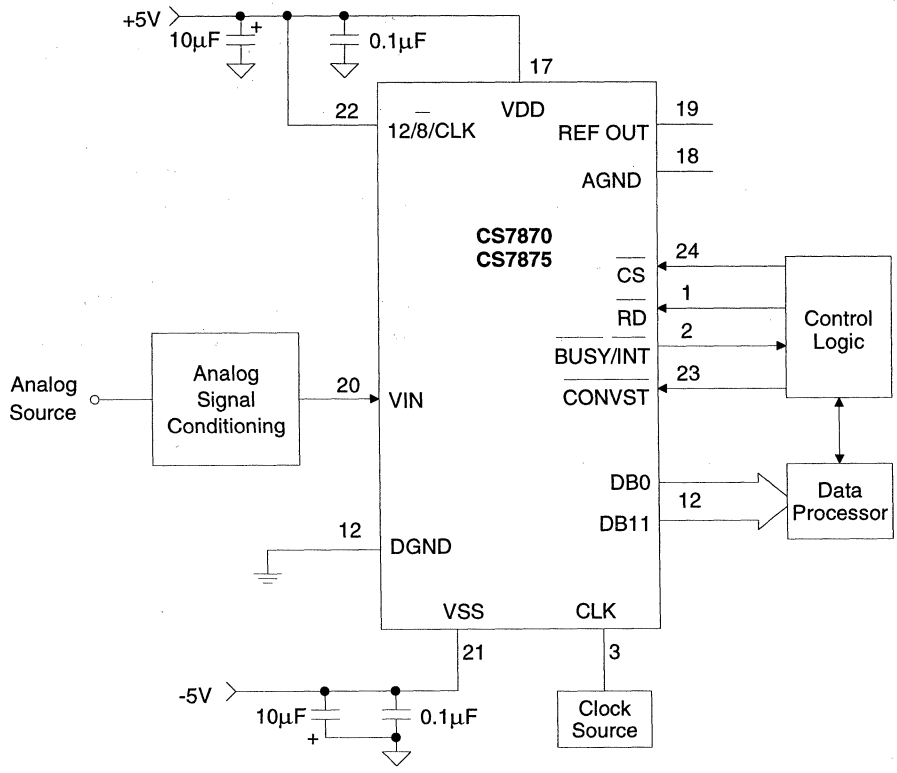


Figure 8. System Connection Diagram: Parallel Data Format

In serial mode, DB8/SDATA, DB9/SCLK and DB10/$\overline{\text{SSTRB}}$ defer to their serial functions. The serial strobe pin $\overline{\text{SSTRB}}$ provides a framing signal for serial data. Serial data is available at the SDATA pin when $\overline{\text{SSTRB}}$ falls low. $\overline{\text{SSTRB}}$ falls low within three clock cycles of $\overline{\text{CONVST}}$. A total of sixteen bits (four leading zeros and twelve data bits starting with the MSB) are clocked out on the SDATA pin on the rising edge of SCLK. The data bits become valid no more than t_{12} after the rising edge of SCLK. $\overline{\text{SSTRB}}$ goes low during data transmission and automatically returns high when the LSB has been clocked out on the SDATA line. Serial data operation is identical for MODE 1 and MODE 2 timing control (see next two sections). For serial operation, 0V on the 12/$\overline{8}$/CLK pin causes the serial clock to run only when data is being clocked out of the device; SCLK goes high after data transmission is completed. If the 12/$\overline{8}$/CLK is connected to -VA, the SCLK output will run continuously, independent of data transmission.

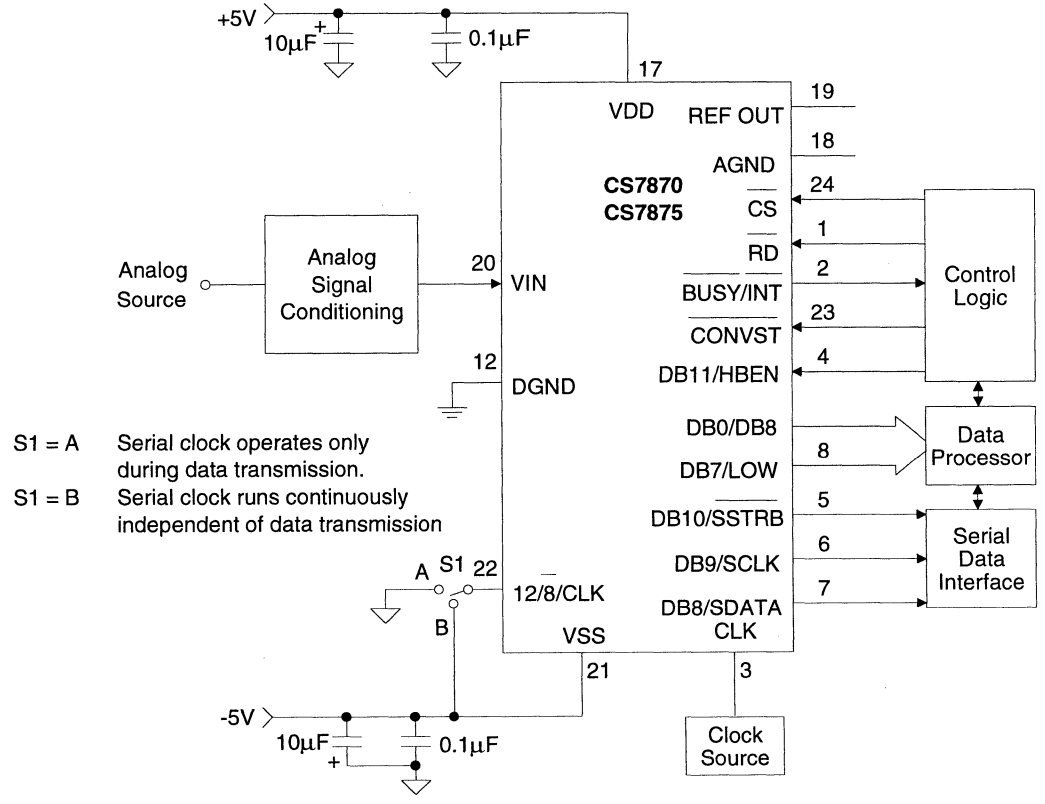


Figure 9. System Connection Diagram: Serial and Byte Data format

MODE 1 Operation

The CONVST signal is used to put the device into hold mode and initiate a conversion. At the end of conversion the device returns to it's tracking mode. MODE 1 timing is primarily used in DSP type applications where precise control of CONVST timing is required.

Conversion begins on the rising edge of CONVST provided that CS is high. The BUSY/INT line performs the INT function and can be used to interrupt the microprocessor. INT is normally high and goes low at the end of conversion. The ADC begins to acquire the analog input when INT goes low. Bringing CS and RD low allows data to be read from the ADC, and also resets INT high. CONVST must be high when CS and RD are brought low for the ADC to operate correctly in this mode. Data cannot be read during a conversion cycle because the output data latches are disabled while a conversion is in progress.

MODE 1 - 12-Bit Parallel Read

Figure 10 shows the MODE 1 timing diagram for 12-bit parallel operation (12/8/CLK = +VA). A data read operation performed at the end of conversion will read all twelve bits of data at the same time.

MODE 1 - Byte Read

Figure 11 shows the MODE 1 timing diagram for byte operation. At the end of conversion when INT goes low, either the low byte or the high byte of data can be read, depending on the status of HBEN. Bringing CS and RD low allows data to be read from the ADC and also resets INT high.

MODE 1 - Serial Read

The MODE 1 timing diagram for serial operation is shown in Figure 12. Conversion begins on the falling edge of CONVST, and data is clocked out on SDATA immediately upon the falling edge of SSTRB. The data is output as four leading zeroes followed by the twelve data bits with the MSB first. The first zero should be latched into the external receiving circuitry on the first falling edge of SCLK after SSTRB goes low. A total of sixteen falling SCLK edges will latch all sixteen bits of output data. SSTRB automatically returns high after the last bit of data has been clocked out of the device.

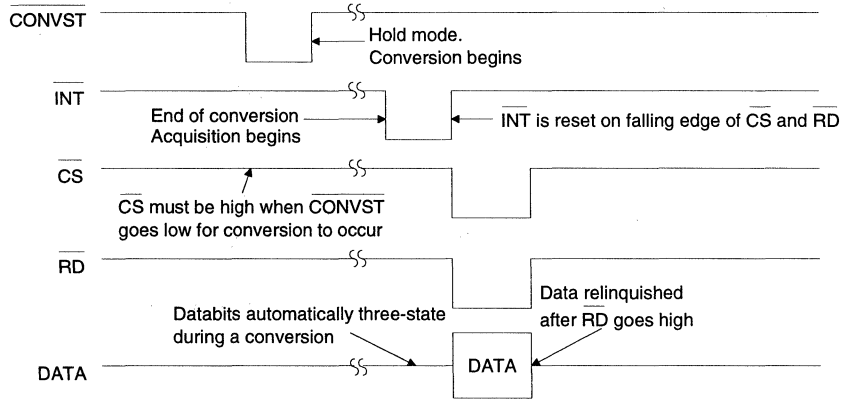
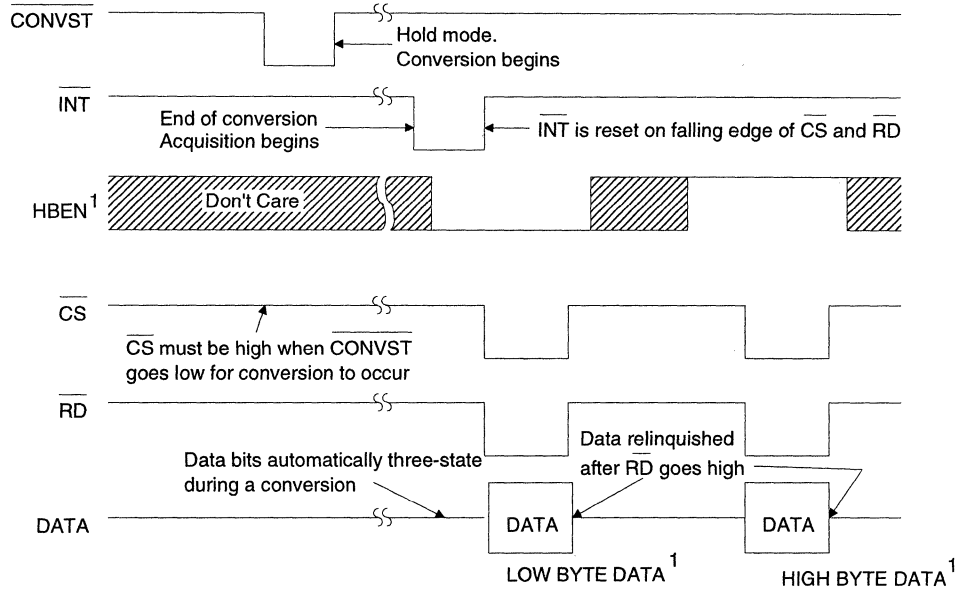


Figure 10. Mode 1 Timing Diagram, 12-bit Parallel Read



Note: 1. In the above diagram HBEN is exercised to read the low byte first (DB7-DB0) and then the high byte (DB11-DB8). To change the order in which the bytes are read, simply invert the HBEN signal shown above.

Figure 11. Mode 1 Timing Diagram, Byte Read

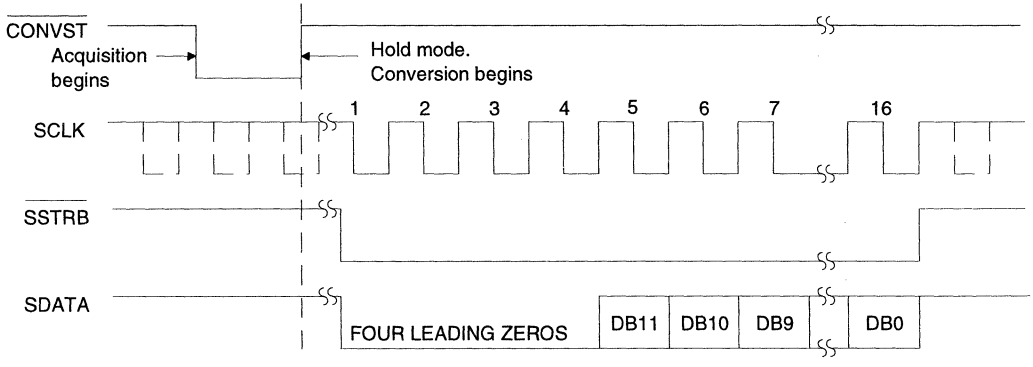


Figure 12. Mode 1 Timing Diagram - Serial Read

MODE 2 Operation

Mode 2 operation allows the ADC conversion to be initiated by a read operation from a µC. The $\overline{BUSY}$ signal can be used in this mode to halt µC operations by placing the µC in a WAIT state until the conversion is complete. This avoids having to handling interrupts and timing delays , assuring that the conversion cycle is complete before any attempted data read.

In this mode, $\overline{CONVST}$ must be held permanently low. Bringing $\overline{CS}$ low (while $\overline{HBEN}$ is low) puts the device into hold mode and initiates a conversion. The $\overline{BUSY}/\overline{INT}$ pin defers to the $\overline{BUSY}$ function such that $\overline{BUSY}$ goes low at the start of conversion and returns high at the end of conversion.

MODE 2 - 12-Bit Parallel Read

The MODE 2 timing diagrams for the parallel data output format are shown in Figure 13. This mode of operation forces the µC into a WAIT state until the conversion has been completed. It removes the risk of inadvertently reading invalid data before the conversion cycle has been completed.

MODE 2 - Byte Read

Figure 14 shows the timing diagram for byte operation in MODE 2. Since $\overline{HBEN}$ must be low to initiate a conversion, the lower byte of data will be accessed first during the two-byte read operation. This is followed by a second byte read operation (with $\overline{HBEN}$ high) to complete the data transfer.

MODE 2 - Serial Read

The timing diagram for MODE 2 serial operation is shown in Figure 15. The device goes into hold mode on the falling edge of $\overline{CS}$ and conversion begins when $\overline{BUSY}$ goes low. The data is clocked out similarly as for MODE 1 serial operation. Upon clocking of the final data bit $\overline{BUSY}$ returns high indicating end of conversion.

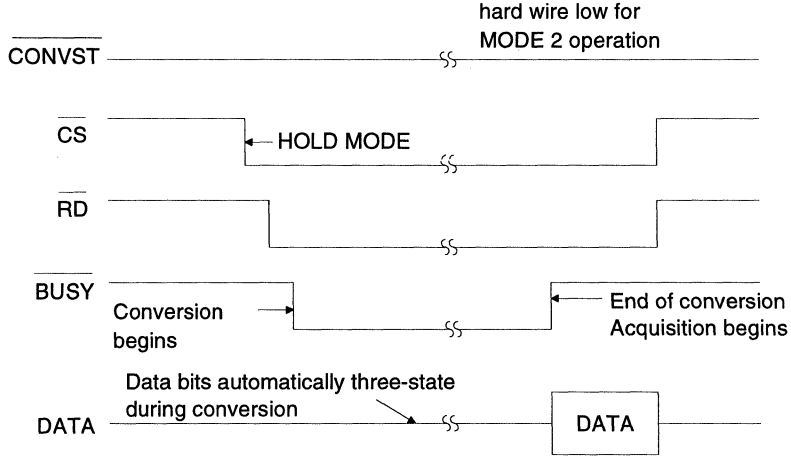


Figure 13 Mode 2 Timing Diagram, 12-bit Parallel Read

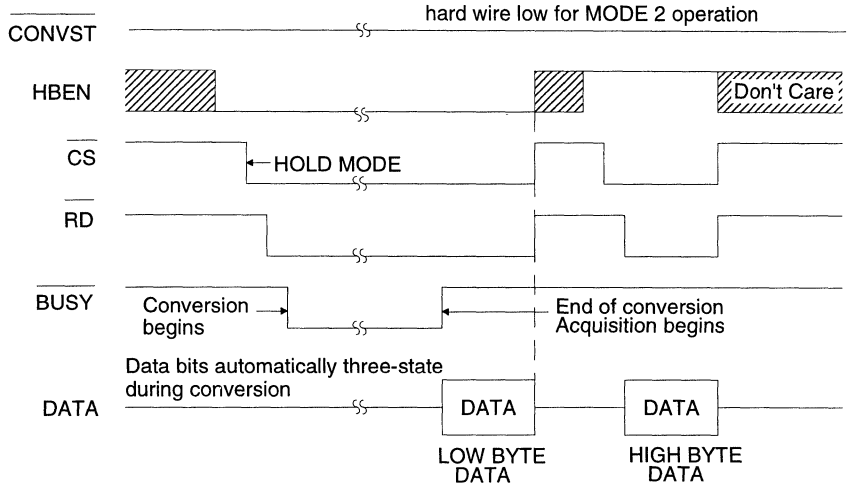


Figure 14. Mode 2 Timing Diagram, 12-bit Byte Read

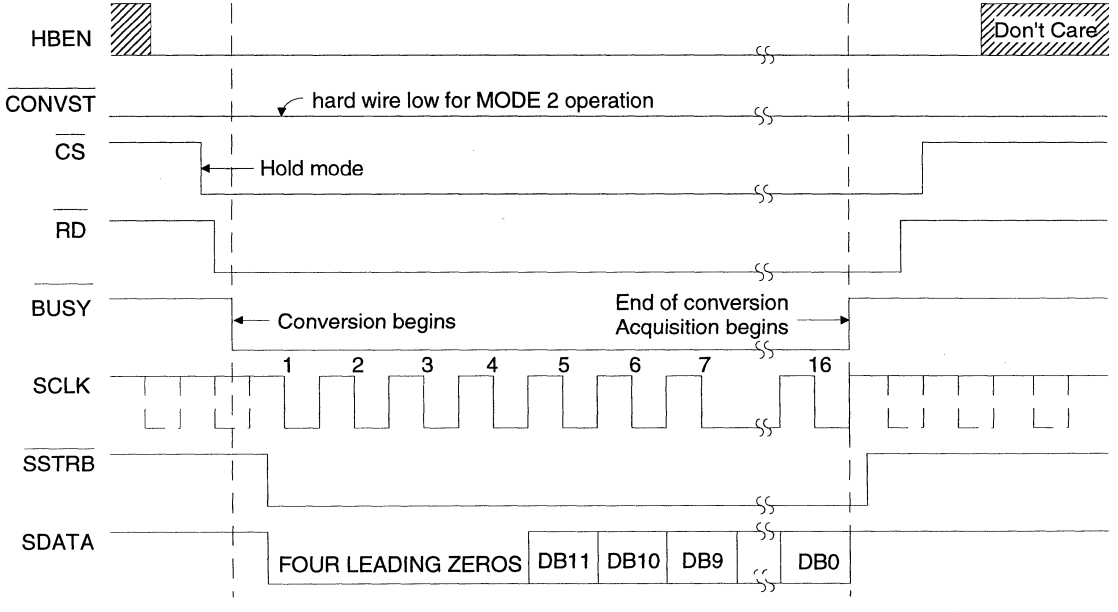


Figure 15. Mode 2 Timing Diagram, Serial Read

STAND-ALONE OPERATION

The CS7870/CS7875 supports stand-alone conversion when used in MODE 2 parallel interface operation as shown in Figure 16. Conversion is initiated by pulse to the $\overline{CS}$ input of the ADC. The duration of the pulse must be longer than the ADC conversion time. The $\overline{BUSY}$ output drives the $\overline{RD}$ input and data is latched on the rising edge of $\overline{BUSY}$ to an external latch.

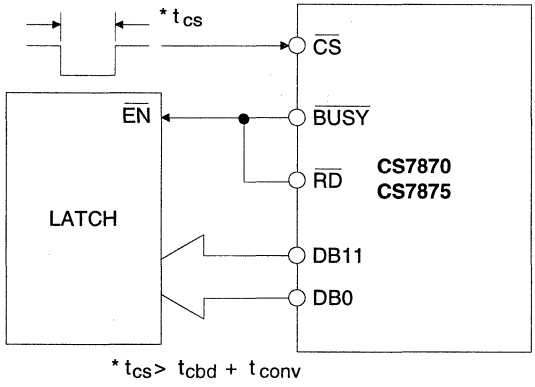


Figure 16. Stand-Alone Operation

Power Supplies, AGND, and DGND

Figure 8 illustrates the recommended power supply decoupling scheme with a 0.1µF ceramic and a +10µF tantalum capacitor for both the VA+ and the VA- pins. The capacitors should be located as close as practical to the supply pins. AGND is the power supply current return, and is also the preferred ground reference for the decoupling capacitors.

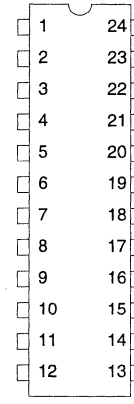
Typically a low-impedance ground plane is used around and under the ADC, with connections to both AGND and DGND. If a split ground is used, DGND is the ground reference for any digital circuits that follow the CS7870/CS7875. When split grounds are used, the AGND to DGND voltage differential should be kept below ±10mV for best operation.

If the power supply voltage is dropped below 3V, the ADC may need to be reset by switching power off and then back on.

Layout considerations

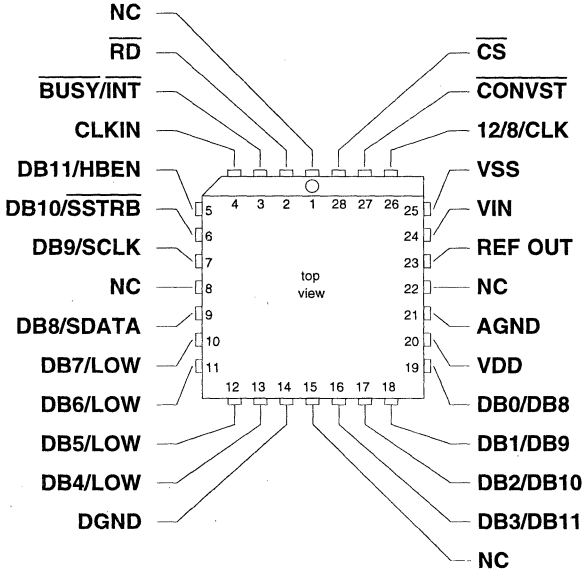
The CS7870/CS7875 is a high-speed component which requires adherence to standard high-frequency printed circuit board layout techniques to maintain optimum performance. These include proper supply decoupling, minimum length circuit traces, and physical separation of digital and analog components and circuit traces. See the CDB7870/75 evaluation board data sheet for more details.

PIN DESCRIPTIONS



READ	$\overline{RD}$	1	24	$\overline{CS}$	CHIP SELECT
BUSY/INTERRUPT	$\overline{BUSY}/\overline{INT}$	2	23	$\overline{CONVST}$	CONVERT START
CLOCK INPUT	CLKIN	3	22	12/$\overline{8}$/CLK	DATA OUTPUT FORMAT
DB11/HIGH BYTE ENABLE	DB11/HBEN	4	21	V_{SS}	NEGATIVE ANALOG SUPPLY
DB10/SERIAL STROBE	DB10/$\overline{SSTRB}$	5	20	V_{IN}	ANALOG INPUT
DB9/SERIAL CLOCK	DB9/SCLK	6	19	REF OUT	VOLTAGE REF OUT
DB8/SERIAL DATA	DB8/SDATA	7	18	AGND	ANALOG GROUND
DATA OUT	DB7/LOW	8	17	V_{DD}	POSITIVE ANALOG SUPPLY
DATA OUT	DB6/LOW	9	16	DB0/DB8	DATA OUT
DATA OUT	DB5/LOW	10	15	DB1/DB9	DATA OUT
DATA OUT	DB4/LOW	11	14	DB2/DB10	DATA OUT
DIGITAL GROUND	DGND	12	13	DB3/DB11	DATA OUT

28-Pin Plastic and Ceramic DIPs



28-Pin PLCC

Power Supply Connections

V_{DD} – Positive Supply, PIN 17.
+5V±5%.

V_{SS} – Negative Supply, PIN 21.
-5V±5%.

DGND – Digital Ground, PIN 12.
Ground reference for digital circuitry.

AGND – Analog Ground, PIN 18.
Ground reference for track-and-hold, reference and DAC.

Oscillator

CLK – Clock Input, PIN 3.
An external 2.5MHz (CMOS compatible) clock is applied at this pin. Connecting this pin to V_{SS} enables the internal clock oscillator.

Digital Inputs

$\overline{CS}$ – Chip Select, PIN 24.
Active low logic input. The device is selected when this input is active. With $\overline{CONVST}$ tied low, a new conversion is initiated when $\overline{CS}$ goes low.

$\overline{RD}$ – Read, PIN 1.
Active low logic input. This input is used in conjunction with $\overline{CS}$ low to enable the data outputs.

12/$\overline{8}$/CLK – Output Mode Selection, PIN 22.
Defines the output data format and serial clock format. With 12/$\overline{8}$/CLK at +5V, the output data format is 12-bit parallel only. With 12/$\overline{8}$/CLK at 0V, either byte or serial data is available and SCLK is not continuous. With 12/$\overline{8}$/CLK at -5V, byte or serial data is again available but SCLK is now continuous.

$\overline{CONVST}$ – Convert Start, PIN 23.
A low to high transition on this input puts the track-and-hold into its hold mode and starts conversion. This input is asynchronous to the CLK and independent of $\overline{CS}$ and $\overline{RD}$.

Digital Outputs

$\overline{BUSY}$/$\overline{INT}$ – Busy/Interrupt, PIN 2.
Active low logic output indicating converter status. See timing diagrams.

DB11/HBEN – Data Bit 11/High Byte Enable, PIN 4.

The function of this pin is dependent on the state of the 12/$\overline{8}$/CLK input. When 12-bit parallel data is selected, this pin provides the DB11 output. When byte data is selected, this pin becomes the HBEN logic input. HBEN is used for 8-bit bus interfacing. When HBEN is low, DB7/LOW to DB0/DB8 become DB7 to DB0. With HBEN high, DB7/LOW to DB0/DB8 are used for the upper byte of data (see Table 1).

DB10/$\overline{\text{SSTRB}}$ – Data Bit 10/Serial Strobe, PIN 5.

The function of this pin is dependent on the state of the 12/$\overline{8}$/CLK input. When 12-bit parallel data is selected, this pin provides the DB10 output. $\overline{\text{SSTRB}}$ provides a strobe or framing pulse for serial data.

DB9/SCLK – Data Bit 9/Serial Clock, PIN 6.

The function of this pin is dependent on the state of the 12/$\overline{8}$/CLK input. When 12-bit parallel data is selected, this pin provides the DB9 output. SCLK is the gated serial clock output derived from the internal or external ADC clock. If 12/$\overline{8}$/CLK is at -5V, then SCLK runs continuously. If 12/$\overline{8}$/CLK is at 0V, then SCLK goes high after serial transmission is complete.

DB8/SDATA – Data Bit 8/Serial Data, PIN 7.

The function of this pin is dependent on the state of the 12/$\overline{8}$/CLK input. When 12-bit parallel data is selected, this pin provides the DB8 output. SDATA is used with SCLK and $\overline{\text{SSTRB}}$ for serial data transfer. Serial data is valid on the falling edge of SCLK while $\overline{\text{SSTRB}}$ is low.

DB7/LOW, DB6/LOW, DB5/LOW, DB4/LOW – Three-state data outputs, PINS 8, 9, 10, 11.

The outputs of these pins are controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$. Their function depends on the 12/$\overline{8}$/CLK and HBEN inputs. With 12/$\overline{8}$/CLK high, they are always DB7-DB4. With 12/$\overline{8}$/CLK low or -5V, their function is controlled by HBEN (see Table 1).

DB3/DB11, DB2/DB10, DB1/DB9, DB0/DB8 – Three-state data outputs, PINS 13, 14, 15, 16.

The outputs of these pins are controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$. Their function depends on the 12/$\overline{8}$/CLK and HBEN inputs. With 12/$\overline{8}$/CLK high, they are always DB3-DB0. With 12/$\overline{8}$/CLK low or -5V, their function is controlled by HBEN (see Table 1).

HBEN	DB7/LOW	DB6/LOW	DB5/LOW	DB4/LOW	DB3/DB11	DB2/DB10	DB1/DB9	DB0/DB8
HIGH	LOW	LOW	LOW	LOW	DB11/(MSB)	DB10	DB9	DB8
LOW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0/(LSB)

Table 1. Output Data for Byte Interfacing

Analog Output

REF OUT - Voltage Reference Output, PIN 19.

The internal +3V reference is provided at this pin. The external load capability is 500µA. This pin should be left open. If used, it can be directly decoupled to AGND with up to 50pF, or through a 200Ω resistor to a +10µF tantalum and 0.1µF ceramic capacitors. REF OUT settling time is approximately 1.1 sec.

Analog Input

V_{IN} - Analog Input, PIN 20.

The analog input range for the CS7870 is ±3V, ... 0V to +5V for the CS7875.

Ordering Information

Model	Temp (°C)	Tempco (ppm/°C)	SINAD (dB)	INL (LSB)	Package
V_{IN} Range = ±3V					
CS7870-BP	-40/85	60	72	0.5	24-pin 0.3" PDIP
CS7870-BL	-40/85	60	72	0.5	28-pin PLCC
CS7870-SD	-55/125	60	72	0.5	24-pin 0.3" CerDIP
V_{IN} Range = 0V to +5V					
CS7875-BP	-40/85	60	72	0.5	24-pin 0.3" PDIP
CS7875-BL	-40/85	60	72	0.5	28-pin PLCC
CS7875-TD	-55/125	60	72	0.5	24-pin 0.3" CerDIP

Cross Reference List

Crystal Semiconductor	Analog Devices
V_{IN} = ±3V	
CS7870-BP	AD7870JN, AD7870KN
CS7870-BL	AD7870JP, AD7870KP
CS7870-SD	AD7870AQ, AD7870BQ, AD7870SQ
V_{IN} = 0V to +5V	
CS7875-BP	AD7875KN
CS7875-BL	AD7875KP
CS7875-TD	AD7875BQ, AD7875TQ

PARAMETER DEFINITIONS

REF OUT Tempco

REF OUT Tempco is the worst case slope that is calculated from the change in reference value at +25°C to the value at T_{MIN} or T_{MAX}

i.e. REF OUT Tempco = $(V_{ref}$ @ 25°C - V_{ref} @ $T_{MAX})/(T_{MAX}$ - 25°C) or

REF OUT Tempco = $(V_{ref}$ @ 25°C - V_{ref} @ $T_{MIN})/(25°C - T_{MIN})$.

Differential Linearity

The deviation of a code's width from ideal. Units in LSBs.

Integral Non-Linearity Error - INL

The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code.

Full-Scale Error - FSE_P

The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSB's.

Unipolar Offset (CS7875) - V_{UP}

The deviation of the first code transition from the ideal (1/2 LSB above AGND) when in. Units in LSB's.

Bipolar Offset (CS7870) - V_{BP}

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND). Units in LSB's.

Bipolar Negative Full-Scale Error (CS7870) - FSE_N

The deviation of the first code transition from the ideal. The ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSB's.

Spurious-Free-Dynamic-Range - SFDR

The ratio of the rms value of the signal, to the rms value of the next largest spectral component (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Units dBc (decibels relative to the carrier).

Total Harmonic Distortion - THD

The ratio of the rms sum of the significant harmonics (2^{nd} thru 5^{th}), to the rms value of the signal. Units in decibels.

Signal-to-Noise Ratio (s/n) - SNR

The ratio of the rms value of the signal, to the rms sum of all other spectral components below the Nyquist rate (excepting dc and distortion terms). Expressed in decibels

Signal-to-Noise-and-Distortion (s/[n+d]) - SINAD

The ratio of the rms value of the signal, to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels

Intermodulation Distortion - IMD

The ratio of the rms value of the larger of two test frequencies, which are each 6dB down from full-scale, to the rms value of the largest 2^{nd} and 3^{rd} order intermodulation components. Units in decibels relative to carrier.

Aperture Delay Time - t_{apd}

The time required after $\overline{\text{CONVST}}$ goes high for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter - t_{apj}

The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

Semiconductor Corporation

CDB7870
CDB7875

Evaluation Board for CS7870 & CS7875

Features

- Throughput rates up to 100kHz.
- Operation with on-board or off-board clocks.
- Buffered serial data, 12-bit parallel word, or two 8-bit bytes
- Digital and Analog Patch Areas
- CS7870 ±3V input
  CS7875 0V to +5V input

General Description

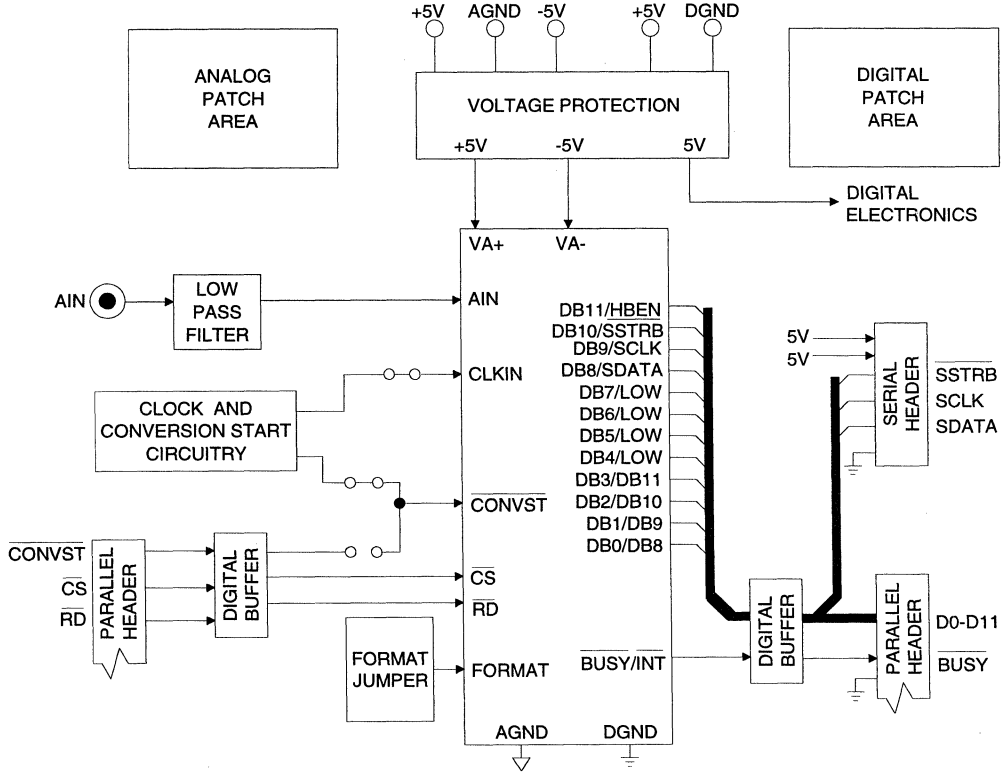
The CDB7870/5 Evaluation Boards allow fast evaluation of the CS7870 & CS7875 12-bit, 100kHz, sampling A/D Converters.

The board provides a convenient platform for easy circuit development and evaluation. A versatile tool that can simplify design and reduce the design cycle resulting in a quicker time to market.

Analog input is via a BNC connector. Buffered digital outputs are available from the ADC in serial, 12-bit parallel word, or two 8-bit bytes formats.

ORDERING INFORMATION

CDB7870 Evaluation Board with CS7870-BP Installed
CDB7875 Evaluation Board with CS7875-BP Installed



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Introduction

The CDB7870 and CDB7875 evaluation boards provide a tool for testing and designing with the CS7870/5 series of A/D Converters. The boards are configured for operation from ±5V analog and +5V digital power supplies. A BNC connector is provided for the analog input signal. An on-board jumper selects the output data and serial clock formats. Parallel and serial connectors provide an interface to the digital logic.

Power Supplies

Figure 1 shows the power supply arrangements. ±5V is required to operate the ADC and analog portion of the board. Zener diodes are provided for over-voltage protection. A separate +5V digital supply is required for the digital logic. At least one individual decoupling capacitor is provided for each IC.

Analog Input Circuit

The analog input signal is brought on the evaluation board via the BNC connector J8. Diodes D1 and D2 provide protection against over voltage. R4 and C13 make a low pass filter, whose corner frequency is 80 kHz. Notice that no external trim components are required. R6 is a 10 kΩ terminating resister which provides a load for the signal source. R6 can be changed to match the analog input source impedance if required. The footprint is large enough to accommodate a 50 Ω, 0.5 W resistor.

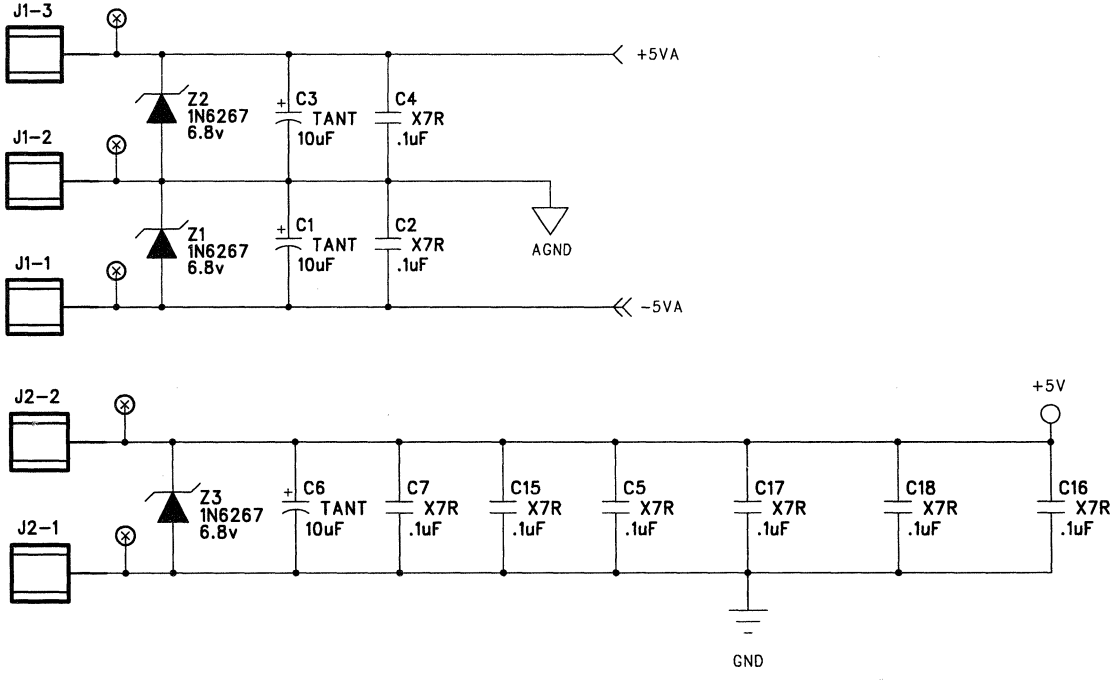


Figure 1. Power Supplies

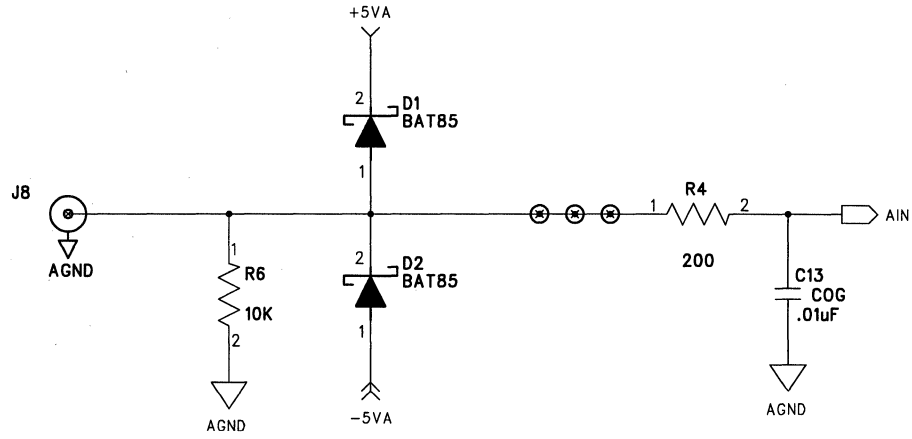


Figure 2. Analog Input Circuit

Clock and Conversion

Figure 3 shows the on-board clock and conversion control circuitry. The evaluation board is designed to run off the on-board 2.5MHz oscillator (U4). The ADC can also operate from an internal clock oscillator, by connecting the CLKIN pin to -5VA. Test points are provided to easily implement the internal oscillator.

The $\overline{\text{CONVST}}$ signal on the evaluation board is derived from the on-board 2.5MHz clock oscillator. The 2.5MHz is divided by 25, providing a 100 kHz signal. External signals can be used by breaking the $\overline{\text{CONVST}}$ jumper at the test points and attaching the external signal at pin 6 of connector J4.

Digital Output Data

The CS7870/5 ADCs support three digital output data formats. These include 12-bit parallel, 8-bit byte, and serial interface formats. Several of the ADC output pins have dual roles or modes of operation (see the CS7870/5 data sheets). The position of the "FORMAT" jumper determines which output format is active, with all three formats available through the 40-pin header J4. Serial output data is also available through the 10-pin header J3.

12-Bit Parallel Operation

Selecting the "+" position for the "FORMAT" jumper places the board in 12-bit parallel mode. All parallel output signals are buffered by U1 and U3, and are available on header J4 (Figure 4). The rising edge of the $\overline{\text{BUSY}}$ signal, available on pin-40 of J4, can be used to latch the 12-bit parallel data into subsequent digital circuitry.

8-Bit Byte Operation

Selecting the "0" or the "-" position for the "FORMAT" jumper places the board in 8-bit byte mode. The data is available on D0 to D7 of header J4 in two separate read operations. The lower byte is read with HBEN low. The four more significant bits are read with HBEN high. The high byte word includes four leading zeros (D4 to D7) to fill out the remaining four significant bits from the ADC. All byte output signals are buffered by U1 and U3.

Serial Operation

Selecting the "0" or the "-" position for the "FORMAT" jumper also places the board in serial mode. In the "-" position, the serial clock SCLK operates continuously; in the "0" jumper position, the serial clock SCLK is active only when the ADC is outputting serial data. The rising edge of SCLK can be used to latch serial data into subsequent circuitry. The serial data and control lines are available on J3, and the DATA8 (SDATA), DATA9(SCLK), and DATA10 ($\overline{\text{SSTRB}}$) lines of J4. All serial output signals are buffered by U1.

Convert Start Operation

MODE 1 Operation

The $\overline{\text{CONVST}}$ signal is used to put the ADC into hold mode and initiate a conversion. At the end of the conversion, the ADC returns to its tracking mode. Conversion begins on the rising edge of the $\overline{\text{CONVST}}$, provided that $\overline{\text{CS}}$ is high (note that external pull-up resistors on $\overline{\text{CS}}$ and $\overline{\text{RD}}$ default both to logic high if no external logic signal is present for these pins on the J4 header). The $\overline{\text{BUSY}}$ line on J4, which goes low when the output data becomes available, can be used as a microprocessor interrupt. Bringing $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low allows data to be read from the ADC and also resets $\overline{\text{BUSY}}$ high. $\overline{\text{CONVST}}$ must be high when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are brought low in this mode. Data cannot be read during the conversion cycle because the ADC output latches are disabled during this process.

MODE 2 Operation

In this mode, $\overline{\text{CONVST}}$ is held permanently low (Break $\overline{\text{CONVST}}$ jumper at the test points and add jumper between $\overline{\text{CONST\_BUF}}$ and $\overline{\text{CONVST}}$. Ground the $\overline{\text{HOLD}}$ signal J4-6). Bringing $\overline{\text{CS}}$ low (while HBEN is low) through the J4 header, puts the ADC into hold mode and initiates a conversion. The $\overline{\text{BUSY}}$ line on J4 goes low at the start of the conversion and returns high at the end of conversion.

FORMAT JUMPER	
+	12-bit parallel mode
0	8-bit byte or serial (16 bit SCLK)
-	8-bit byte or serial (continuous SCLK)

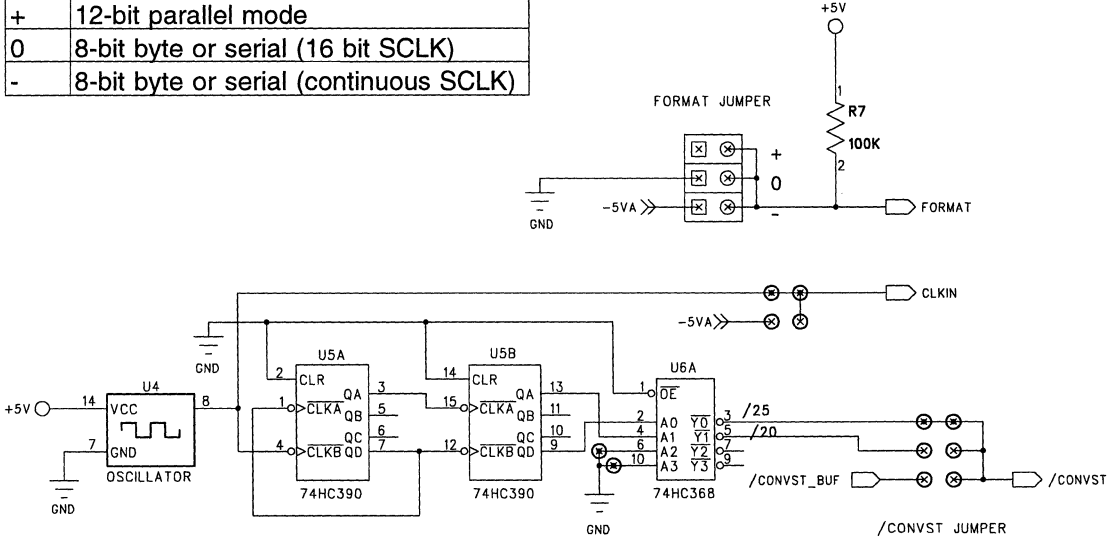


Figure 3. Clock and Convert Start Circuitry

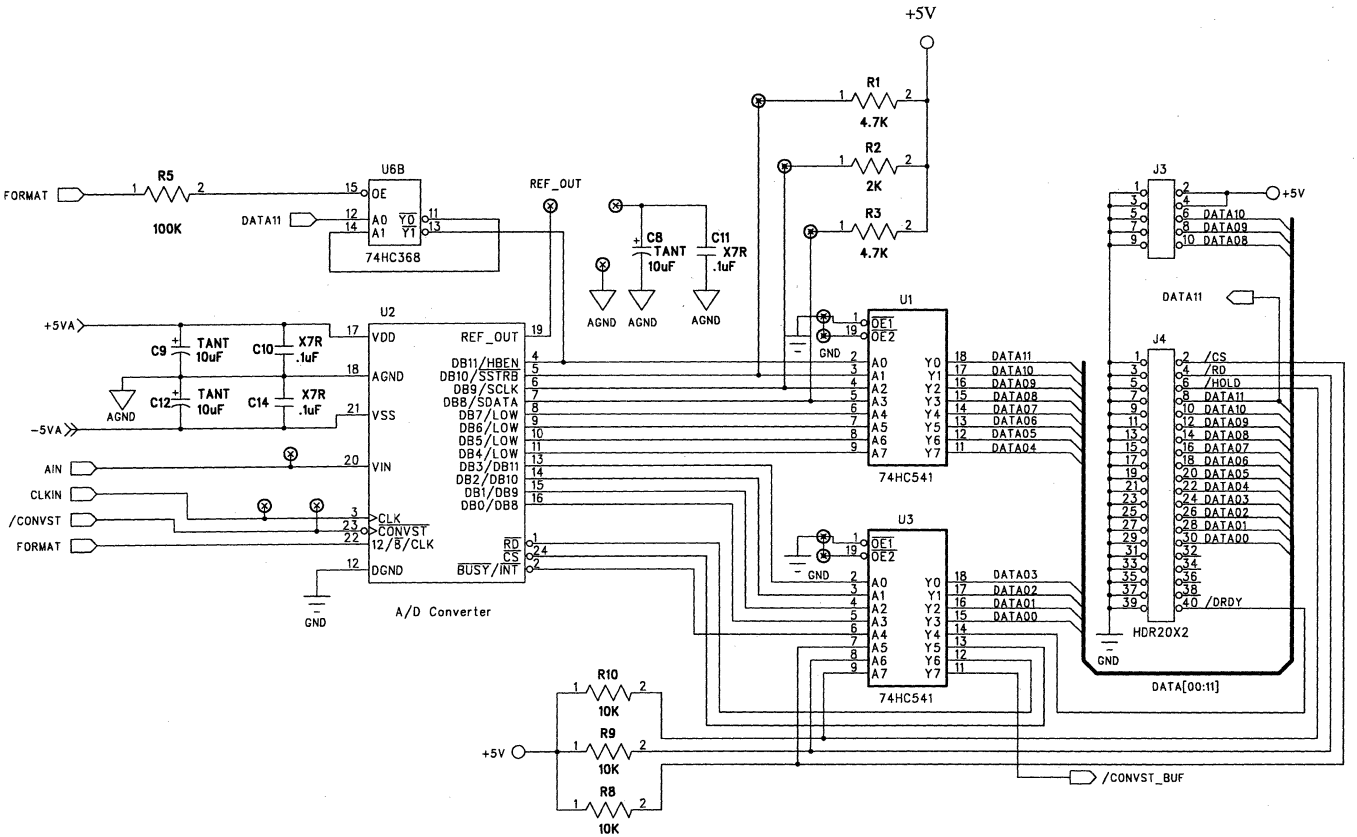


Figure 4. ADC Connections and Digital Output

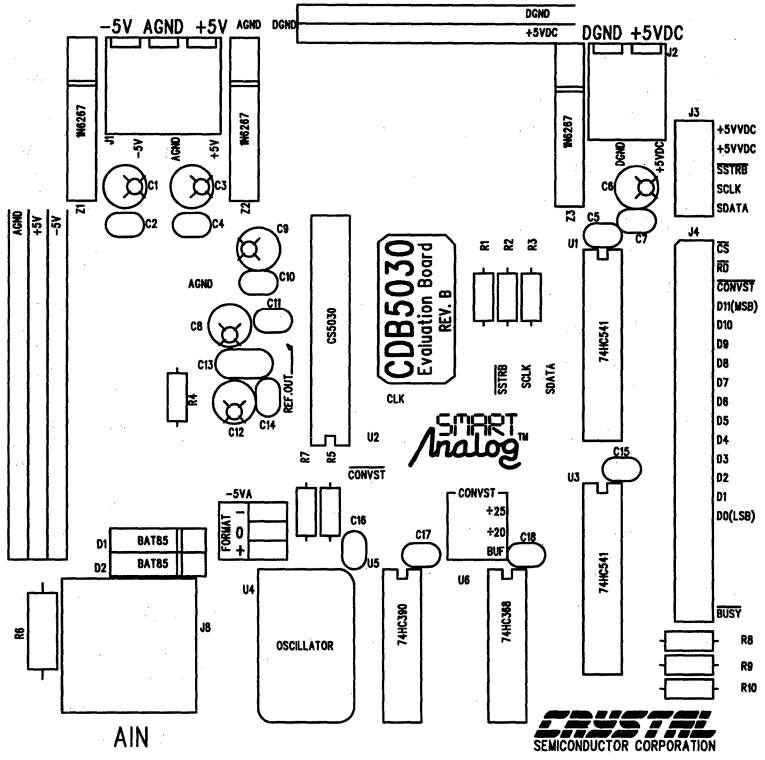


Figure 5. CDB7870/CDB7875 Component Layout

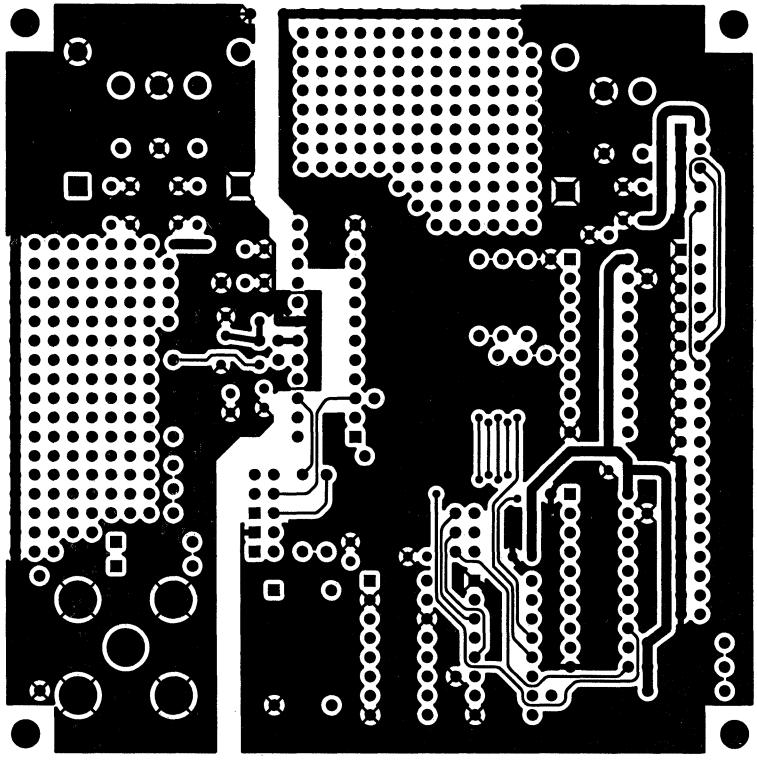


Figure 6. Top Ground Plane Layer (NOT TO SCALE)

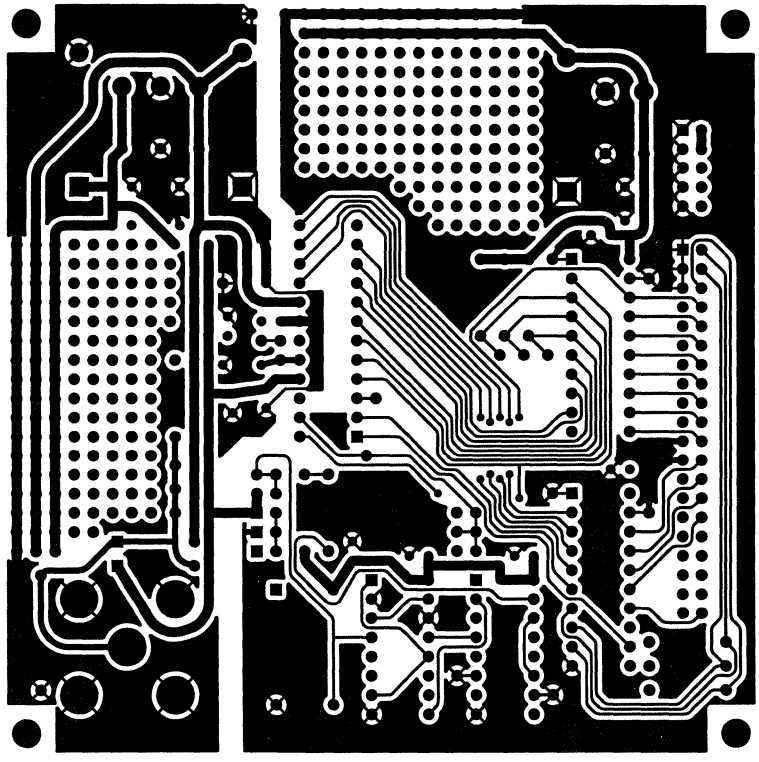


Figure 7. Bottom Trace Layer (NOT TO SCALE)

• Notes •

Semiconductor Corporation

CDBCAPTURE

Data Capture and Interface Board for a PC

Features

- Measurement Tool used for the evaluation of Crystal Semiconductor Analog to Digital Converters.
- Easy interface to a PC Compatible computer.
- LabWindows® based evaluation software for data analysis.
- Includes time domain, FFT, and noise distribution histograms.
- Can be used to evaluate the ADC in your equipment.

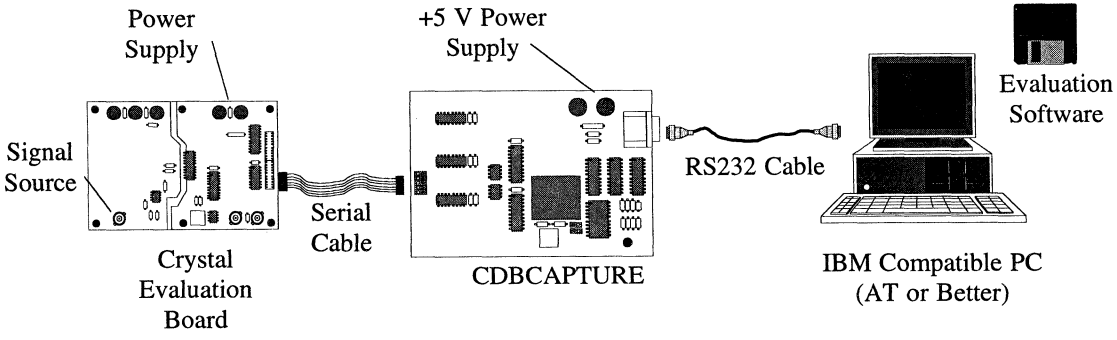
General Description

The CAPTURE interface board is a development tool that interfaces a Crystal Semiconductor analog to digital converter to a PC-compatible computer. Digital data is collected in a high speed digital FIFO, then transferred to the PC over a serial COM port. Evaluation software is included to analyze the data and demonstrate the analog to digital converter's performance.

The CAPTURE interface board is designed to be easily interfaced to Crystal Semiconductor Evaluation boards. Application software is loaded via the PC's serial COM port. The software adjusts the CAPTURE interface board for the appropriate signal timing and polarity, coding format and number of bits, thus allowing the same hardware to be used with a variety of Crystal Semiconductor ADCs.

Evaluation software is included with the CAPTURE interface board. The software is developed with LabWindows, a software development system for instrument control, data acquisition, and analysis applications. The evaluation software permits time domain, frequency domain and histogram analysis.

ORDERING INFORMATION: CDBCAPTURE



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

OVERVIEW

The CAPTURE interface board captures a block of A/D converter output data, which is then transferred to the PC. The CAPTURE board buffers the high speed digital data in a FIFO and transfers the data to the PC via the COM port. Figure 1 is a functional block diagram which illustrates the data acquisition process.

The setup for the CAPTURE board is simple. A serial cable is connected from the evaluation board to the CAPTURE board. An RS232 cable is connected from the CAPTURE board to a PC COM port. A +5V power supply is required. Upon reset, the microcontroller (µC) on the CAPTURE board begins executing boot code from its internal EPROM. The boot code monitors the µC's serial port for application software from the PC and stores the application software in SRAM. The application software is specific for the type of A/D converter being used. When the transfer is complete, the µC executes program code out of the SRAM and turns on the LED.

With the µC running the application software, the data collection process can begin. The collection process is started by a command sent from the PC to the CAPTURE board. When the collection command is received, the CAPTURE board synchronizes itself to the FRAME signal and begins capturing data from the ADC. The serial cable signals are optically isolated for optimum noise isolation. Data is stored in a serial FIFO. The writing to the FIFO is controlled by the µC and Counter/Control circuit.

The CAPTURE board collects one channel of data from the ADC. When the data sample set has been collected and stored in the serial FIFO, the µC reads the data out of the FIFO and converts the format to 2's complement if required. The data in 2's complement format is then transferred to the PC via the RS232 cable connected the PC's COMM port.

The evaluation software developed with LabWindows® performs post processing of the digitized signal (source code included). Time plots, FFT analysis and noise analysis are included. The software operates upon sample sets as large as 8192. For more sophisticated analysis, the LabWindows® development system can be purchased from National Instruments (512-794-0100).

CS5012A	CS5102A	CS5329	CS5390	CS5508
CS5014	CS5126	CS5336	CS5501	CS5509
CS5016	CS5317	CS5338	CS5503	CS7870
CS5030	CS5322	CS5339	CS5504	CS7875
CS5031	CS5326	CS5345	CS5505	
CS5032	CS5327	CS5349	CS5506	
CS5101A	CS5328	CS5389	CS5507	

Crystal Parts Supported by Capture Board
***Future products will be added with software updates.**

Packaging List: CDBCAPTURE Interface Board
Serial Cable
EIA232 Cable (RS232)
3.5" 1.44 MB Software Diskette

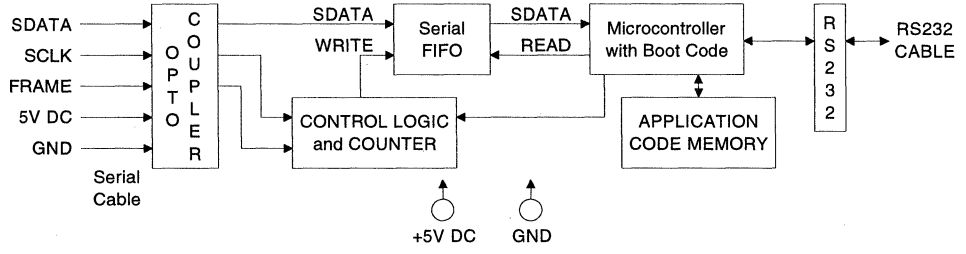


Figure 1. Functional Block Diagram

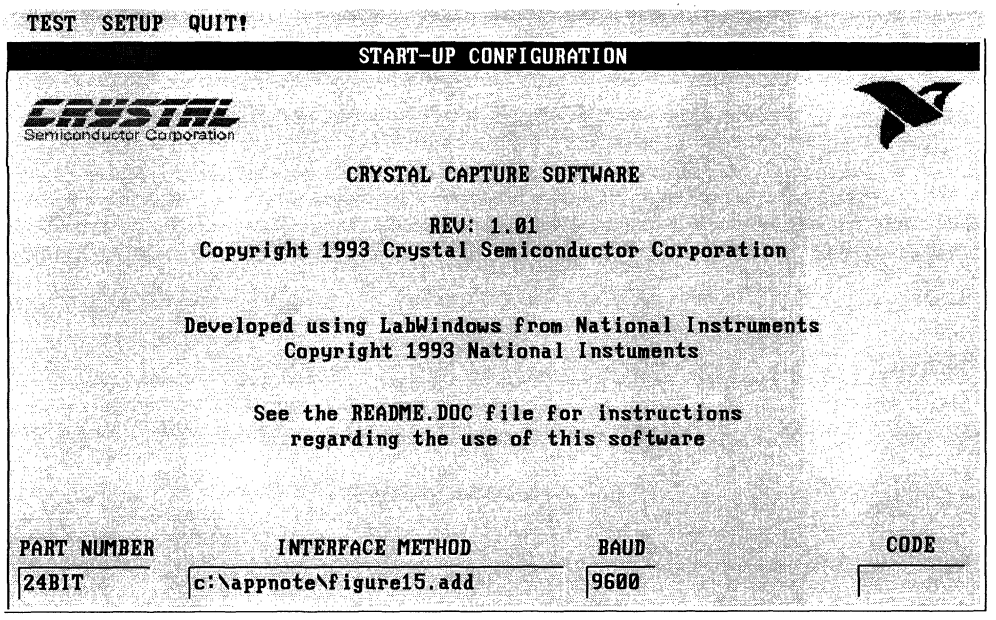


Figure 2. Main Menu

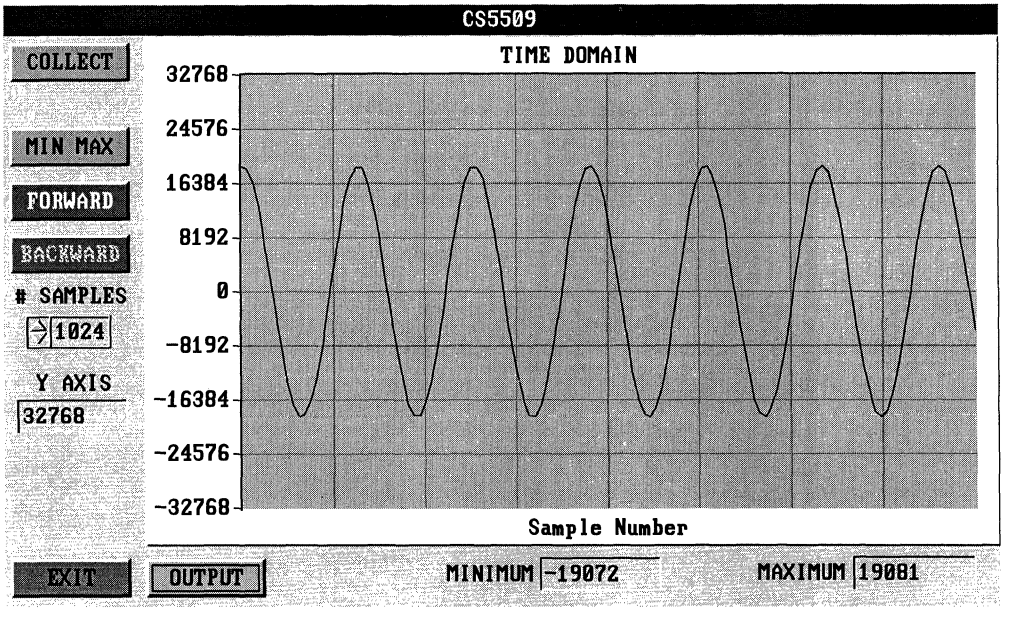


Figure 3. Time Domain Analysis

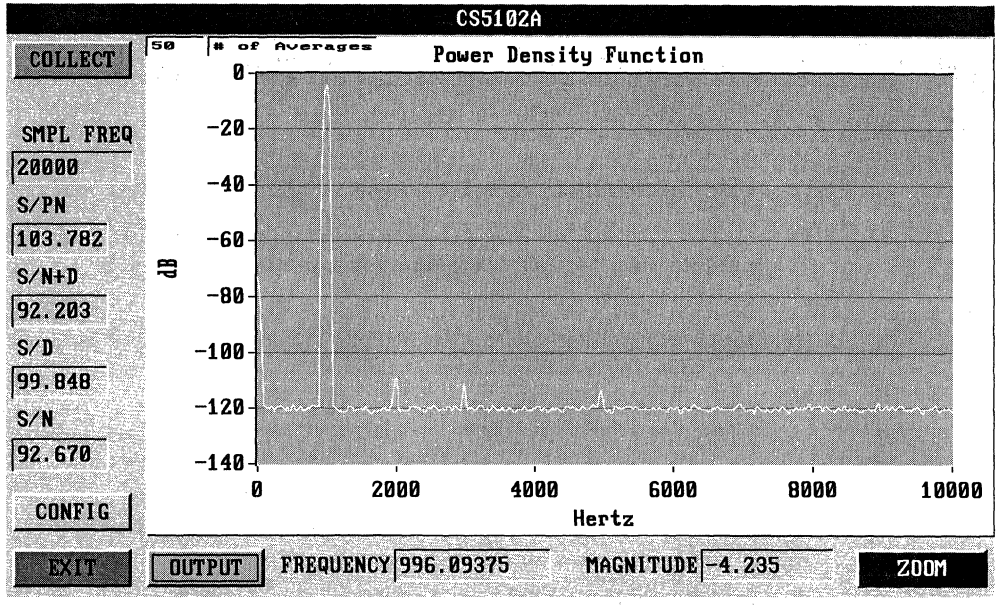


Figure 4. Frequency Domain Analysis

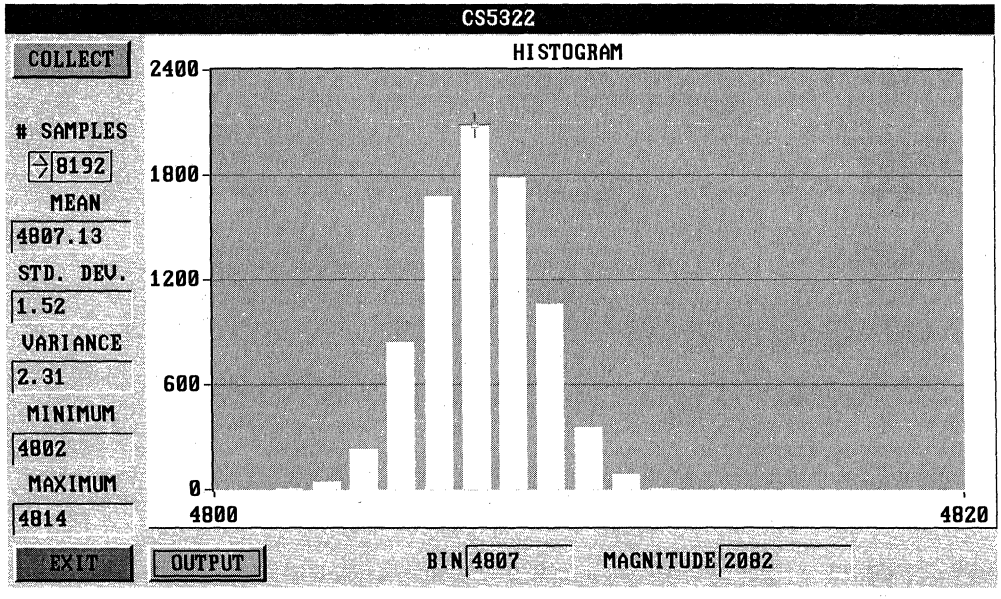


Figure 5. Histogram Analysis

CONSUMER/PROFESSIONAL

CS3310 Volume Control

The CS3310 is a stereo analog volume control, allowing volume level adjustment from -95.5dB to +31.5dB in 0.5dB steps. The volume level is changed via a simple serial digital control bus, which is cascadeable for multiple parts. Low glitch circuit design ensures no "zipper" noise during volume changes. Exceptionally low THD and noise allow use in consumer and professional applications.

CS4303 Digital to Analog Converter

The CS4303 is an all digital I.C. containing an 8X interpolation filter and overall 64X oversampling delta-sigma modulator. Addition of an external analog reconstruction filter yields 107 dB dynamic range with superb low level linearity.

CS4328 Digital to Analog Converter

The CS4328 is the industry's first complete stereo digital-to-analog output system. This 18-bit stereo D/A converter uses Crystal's well established oversampling converter techniques.

The CS4328 includes the major system elements of 8X interpolation filter, 64X delta-sigma modulator, 1-bit D/A converter and a 124 dB signal-to-noise ratio analog anti-imaging filter, all in one packaged, tested, solution. The device features patented delta-sigma architectures to maintain excellent distortion performance, even at low signal levels. The output anti-imaging filters are the first to be based on a mixed linear/switched capacitor architecture. This approach is particularly insensitive to clock jitter and allows the benefit of scaling the bandwidth proportionally to the system master clock. The CS4328 is therefore adjustable for both audio and voice band applications. The flexible digital interface makes with CD player circuitry, DAT recorders and DSP's.

CS4329 20-bit D/A converter

The CS4329 is a complete stereo digital-to-analog conversion system. The device includes interpolation, 128X delta-sigma modulation, 1-bit D/A conversion, and a switched-capacitor analog low pass filter. The on-chip switched capacitor filter provides a high tolerance to clock jitter. The device also features de-emphasis for 32kHz, 44.1kHz, and 48kHz, and independent hardware muting for the left and right output channels. This complete D/A system is offered in a 20-pin DIP and 20-pin SSOP package.

CS4330/1/3 Digital to Analog Converter

Packaged in an 8 pin SOIC, the CS4330 is the world's smallest stereo audio DAC. This 18-bit complete digital-to-analog output system contains interpolation filters, 128X oversampling delta-sigma modulators, 1-bit D/A converters, and analog filtering. De-emphasis is also included for CD applications.

CS5330 Low Power A/D Converter

The CS5330 is a single chip, 18-bit, stereo A/D converter requiring only 125mW of power from a single +5V supply. The part features two 128x oversampling delta-sigma modulators, two digital decimation filters and a voltage reference in an 8 pin SOIC package.

CS5336/8/9 Delta-Sigma Audio A/D Converters

This new class of device features 64X oversampling, using a delta-sigma architecture with resolutions of 16 or 18-bits. Output word rates can be from 1 kHz to 50 kHz. These stereo parts have 2 sample and holds, dual delta-sigma modulators,

two anti-aliasing and decimation filters, and a voltage reference, all in a 28-pin package. Performance measurements include 95 dB dynamic range in stereo mode, up to 100 dB in mono mode, along with 0.0015% THD.

CS5389 & CS5390 Professional Audio Analog to Digital Converters

The CS5389 offers dual differential inputs, with a special modulator design to yield a dynamic range of 107 dB. Excellent noise rejection and low idle tones yield a superbly performing A/D Converter.

The CS5390 is pin compatible with the CS5389, and offers increased dynamic range (112 dB) and 20-bit output data words.

CS8401A, CS8402A AES/EBU & S/PDIF Transmitters

The CS8401A & CS8402A accept digital audio in many standard formats and generate an AES/EBU or S/PDIF compatible data stream. The CS8401A is software programmable for mode and for channel status and user data. The CS8402A is pin programmable.

CS8411, CS8412 AES/EBU and S/PDIF Receivers

The CS8411 and CS8412 digital audio receivers accept AES/EBU or S/PDIF signals and generate digital audio in many standard formats. A low jitter PLL recovers a clean clock for system use. The CS8411 is software readable for channel status and user data. The CS8412 is pin programmable

CS8425 A-LAN - Audio Local Area Network Transceiver

The CS8425 is an S/PDIF transceiver with on-chip low jitter PLL. A ring of CS8425 devices forms an Audio Local Area Network, where user data bits may be used for system messages between nodes. Intended for automotive applications, the device finds use wherever audio and some additional low bandwidth information needs to be communicated between multiple devices.

Audio A/D Converter Comparison Table

Device	CS5330/1	CS5336	CS5338	CS5339	CS5389	CS5390
Number of Bits	18	16	16	16	18	20
Dynamic Range (dB)	94	95	95	95	107	112
SOIC Package	✓	✓	✓	✓	-	-
Filter Passband (kHz)	0-21.7	0-20	0-22	0-22	0-22	0-22
Filter Transition Band (kHz)	21.7-28	20-26	22-28	22-28	22-28	22-28
Stop Band Attenuation (dB)	-80	-80	-80	-80	-80	-100
Overrange Tag Bits	-	✓	✓	✓	-	-
Left/Right Tag Bits	-	✓	✓	✓	-	-
Master Clocking Mode	✓	✓	✓	✓	✓	✓
SCLK active edge	↓	↑	↑	↓	↓	↓
Master Clock Frequency (CFs)	256/384/512	256/384	256/384	256/384	256/384	256/384
Power Supply Voltages (V)	+3 or +5	±5	±5	±5	±5	±5
Operation < 30 kHz	✓	✓	✓	✓	✓	✓
Power Consumption mW	125	400	400	400	550	550

All frequencies are with an output word rate of 48 kHz

BROADCAST

CS4920A Multi-Standard Audio Decoder-DAC

The CS4920A combines a 12.2MIPS DSP with a stereo 16-bit Digital to Analog converter. In addition, a decompressed linear PCM coded digital output is available in industry standard S/PDIF format. An on-chip PLL allows very flexible clocking. DSP code for MPEG 1 & 2 decompression algorithms is provided. Targetted at TV set top audio decoder applications, this device is useful in any application where low-cost audio decompression is required. Hardware data flow control and synchronization circuitry simplify the interface of the CS4920A to a video circuit.

CS4921 MPEG 1 & 2 Audio Decoder-DAC

The CS4921 provides all of the functional blocks of the CS4920A. However, the CS4921 is ROM coded to support MPEG and does not support user programmability.

MULTIMEDIA

CS4215 Serial Interface Audio Codec

The CS4215 is a single 44 pin PLCC package containing 2 16-bit A/D converters, 2 16-bit D/A converters, adjustable input gain, and adjustable output level. Also included is a microphone preamplifier, stereo headphone driver, crystal oscillators and a mono monitoring output. The device requires only a +5V supply, and has a low power standby mode. Both digital audio and control information is communicated over a serial bus.

CS4216 Serial Interface Audio Codec

The CS4216 is a single 44 pin PLCC package containing 2 16-bit A/D converters, 2 16-bit D/A converters, adjustable input gain, and adjustable output level. The device requires only a +5V supply, and has a low power standby mode. Both digital audio and control information is communicated over a serial bus.

CS4225 Two ADC, Four DAC Codec

Intended for automotive and surround sound applications, the CS4225 includes two 16-bit ADCs and four 16-bit DACs. The analog inputs have level adjustment and the analog outputs include an output level attenuator. The device has many clocking modes, including using the on-chip PLL for locking onto an audio sample rate clock. The CS4225 runs from +5V and has a low power standby mode.

CS4231A PC ISA Bus Multimedia Audio Codec

The CS4231A is a single chip with 2 16-bit A/D converters, 2 16-bit D/A converters, adjustable input gain, and adjustable output level. Also included is ADPCM compression and decompression, MPC compatible mixer, timer register for audio/visual synchronization and 16 samples deep FIFOs for record and playback. The devices require only a +5V supply, and have a low power standby mode. Both digital audio and control information is communicated over a parallel bus which meets the PC-ISA bus standard.

CS4232 High-Integration Multimedia Audio

The CS4232 is a single chip audio codec and controller which provides compatibility with ISA Plug-and-Play, Windows Sound System™, SoundBlaster™, and SoundBlaster Pro games. The CS4243 incorporates a direct music synthesizer interface, CD-ROM interface and joystick interface with a MPU-401 compatible MIDI UART; all Plug-and-Play configurable and controlled through the CS4332. Additional features include an MPC Level II compliant mixer, hardware and software based management, full duplex opera-

tion, a serial audio data port and 24mA bus drive capability. Available in 100-pin PQFP and TQFP packages.

CS4248 PC ISA Bus Multimedia Audio Codec

The CS4248 is a single chip with 2 16-bit A/D converters, 2 16-bit D/A converters, adjustable input gain, and adjustable output level. The device requires only a +5V supply, and has a low power standby mode. Both digital audio and control information is communicated over a parallel bus which meets the PC-ISA bus standard.

CS9233 Wavetable Music Synthesizer and CS8905 Digital Effects Processor

The CS9233 is a music synthesis device capable of generating 32 simultaneous notes using high quality wavetable synthesis algorithms. The CS9233 integrates a specialized RISC-based signal processor core with a CISC-based microcontroller and interface logic to provide a low chip count solution. The only external components required for a complete synthesis system are one Program ROM, one SRAM, one PCM Sample ROM, and the CS4331 18-bit stereo oversampled DAC. Program ROM code and Sample ROMs for General MIDI (GM) and General Synthesizer (GS) solutions are available from Crystal. Digital reverb, chorus, and flange effects can be added by including the CS8905 effects processor and one SRAM device.

Software

To support the multimedia codec family, a wide range of software is available. Windows and NT drivers are available for the CS4231A and CS4248 multimedia codecs. A comprehensive diagnostics package assists in the debug of boards. In addition, voice recognition and text-to-speech synthesis software demonstrates some of the capabilities of an audio equipped PC.

CONSUMER/PROFESSIONAL

BROADCAST

MULTIMEDIA

Semiconductor Corporation

CS3310

Stereo Digital Volume Control

Features

- Complete Digital Volume Control
  - 2 Independent Channels
  - Serial Control
  - 0.5 dB Step Size
- Wide Adjustable Range
  - -95.5 dB Attenuation
  - +31.5 dB Gain
- Low Distortion & Noise
  - 0.001% THD+N
  - 116 dB Dynamic Range
- Noise Free Level Transitions
- Channel-to-Channel Crosstalk Better Than 110 dB

General Description

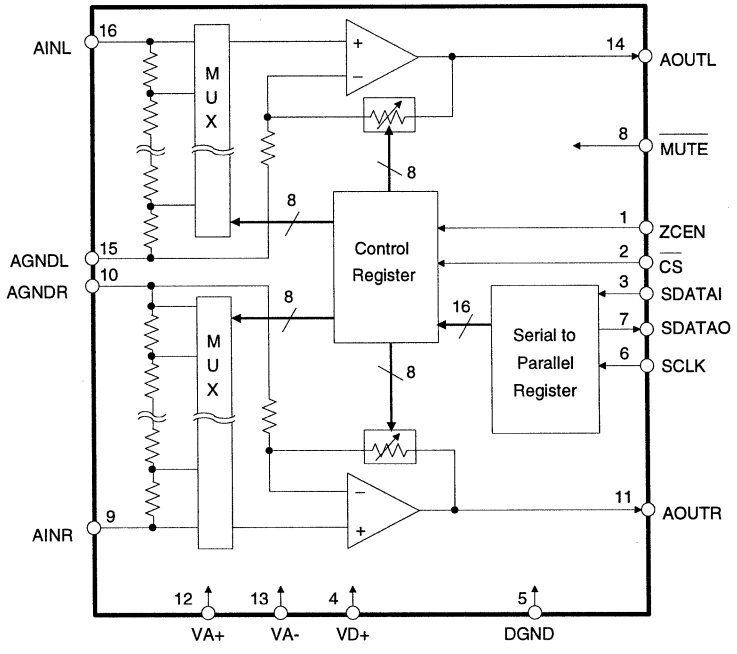
The CS3310 is a complete stereo digital volume control designed specifically for audio systems. It features a 16-bit serial interface that controls two independent, low distortion audio channels.

The CS3310 includes an array of well-matched resistors and a low noise active output stage that is capable of driving a 600 Ω load. A total adjustable range of 127 dB, in 0.5 dB steps, is achieved through 95.5 dB of attenuation and 31.5 dB of gain.

The simple 3-wire interface provides daisy-chaining of multiple CS3310's for multi-channel audio systems.

The device operates from ±5V supplies and has an input/output voltage range of ±3.75V.

For more information see the 1994 Audio Data Book



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Semiconductor Corporation

CS4303

107 dB, D/A Converter for Digital Audio

Features

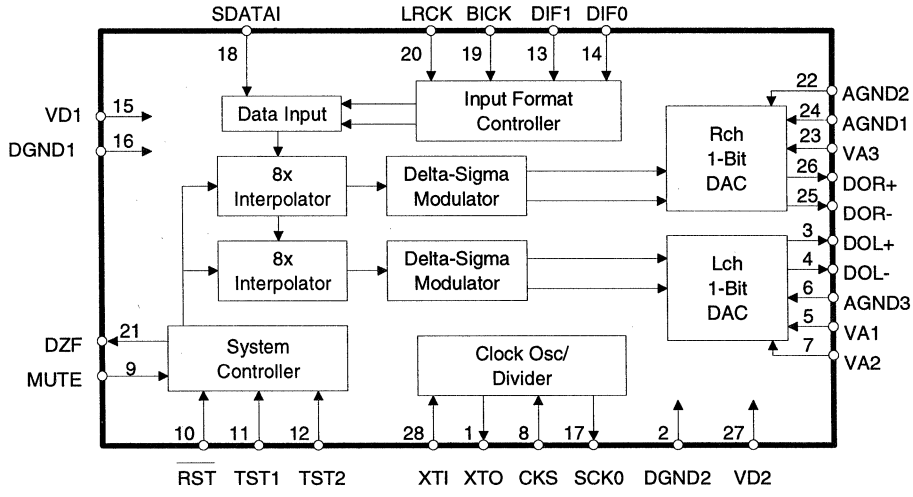
- Stereo Delta-Sigma D/A converter
  8× Interpolation Filter
  64× Delta-Sigma DAC
- Single +5V Operation
- Adjustable System sampling Rates including 32 kHz, 44.1 kHz and 48 kHz
- 107 dB Dynamic Range Over the Audio Bandwidth
- ±0.0002 dB Passband Ripple
- Flexible Serial Input Port
  Supports Multiple Input Formats
  16 or 18 Bit Input Words

General Description

The CS4303 is a high performance delta-sigma D/A converter for digital audio systems which require wide dynamic range. The CS4303 includes 8× interpolation and a 64× oversampled delta-sigma modulator that outputs a 1-bit signal to an external analog low pass filter. The 1's density of the 1-bit signal is proportional to the digital input.

The CS4303 has a configurable input serial port that provides four interface formats. The master clock rate can be either 256 or 384 times the input word rate, supporting various audio environments.

For more information see the 1994 Audio Data Book



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Semiconductor Corporation

CS4328

18-Bit, Stereo D/A Converter for Digital Audio

Features

- Complete Stereo DAC System
  - 8× Interpolation Filter
  - 64× Delta-Sigma DAC
  - Analog Post Filter
- Adjustable System Sampling Rates including 32kHz, 44.1kHz & 48kHz
- 120 dB Signal-to-Noise Ratio
- Low Clock Jitter Sensitivity
- Completely Filtered Line-Level Outputs
  - Linear Phase Filtering
  - Zero Phase Error Between Channels
  - No External Components Needed
- Flexible Serial Interface for Either 16 or 18 bit Input Data

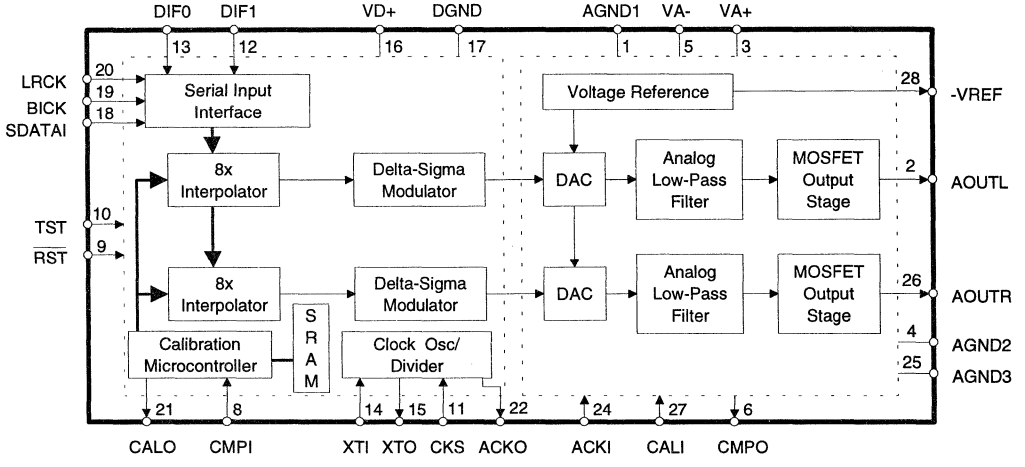
General Description

The CS4328 is a complete stereo digital-to-analog output system. In addition to the traditional D/A function, the CS4328 includes an 8× digital interpolation filter followed by a 64× oversampled delta-sigma modulator. The modulator output controls the reference voltage input to an ultra-linear analog low-pass filter. This architecture allows for infinite adjustment of sample rate between 1 kHz and 50 kHz while maintaining linear phase response simply by changing the master clock frequency.

The CS4328 also includes an extremely flexible serial port utilizing two select pins to support four different interface modes.

The master clock can be either 256 or 384 times the input word rate, supporting various audio environments.

For more information see the 1994 Audio Data Book



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Semiconductor Corporation

CS4329

20-Bit, Stereo D/A Converter for Digital Audio

Features

- 20-Bit Resolution
- Complete Stereo DAC System
  - 128X Interpolation Filter
  - Delta-Sigma DAC
  - Analog Post Filter
- Adjustable System Sampling Rates including 32kHz, 44.1kHz & 48kHz
- 105 dB Dynamic Range
- Low Clock Jitter Sensitivity
- Filtered Line-Level Outputs
  - Linear Phase Filtering
  - Zero Phase Error Between Channels
- Flexible Serial Interface for Either 16, 18 or 20 bit Input Data
- Digital De-emphasis for 32kHz, 44.1kHz & 48kHz

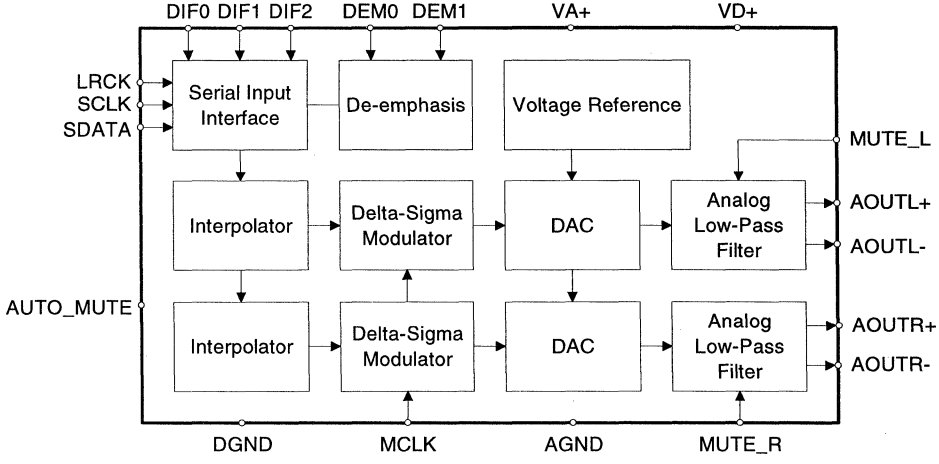
General Description

The CS4329 is a complete stereo digital-to-analog output system. In addition to the traditional D/A function, the CS4329 includes a digital interpolation filter followed by an 128X oversampled delta-sigma modulator. The modulator output controls the reference voltage input to an ultra-linear analog low-pass filter. This architecture allows for infinite adjustment of sample rate between 1 and 50 kHz while maintaining linear phase response simply by changing the master clock frequency.

The CS4329 also includes an extremely flexible serial port utilizing node select pins to support multiple interface modes.

The master clock can be either 256, 384, or 512 times the input word rate, supporting various audio environments.

For more information contact your sales representative (Chapter 7)



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

8-Pin Stereo D/A Converter for Digital Audio

Features

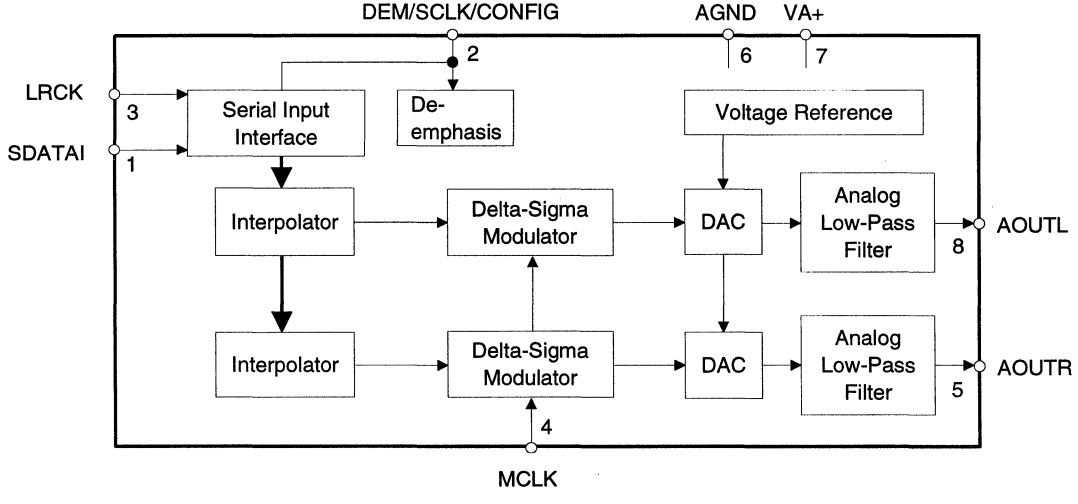
- Complete Stereo DAC System: Interpolation, D/A, Output Analog Filtering
- 18-Bit Resolution
- 94 dB Dynamic Range
- 0.003% THD
- Low Clock Jitter Sensitivity
- Single +3V or +5V Power Supply
- Completely Filtered Line Level Outputs Linear Phase Filtering
- On-Chip Digital De-emphasis

General Description

The CS4330, CS4331 and CS4333 are complete, stereo digital-to-analog output systems including interpolation, 1-bit D/A conversion and output analog filtering in an 8-pin package. These devices differ in the serial interface format used to input audio data. The CS4330, CS4331 and CS4333 are based on delta-sigma modulation where the modulator output controls the reference voltage input to an ultra-linear analog low-pass filter. This architecture allows for infinite adjustment of sample rate between 1 kHz and 50 kHz while maintaining linear phase response simply by changing the master clock frequency.

The CS4330, CS4331 and CS4333 contain on-chip digital de-emphasis, operate from a single +3V or +5V power supply and consume only 50 mW of power with a 3V power supply. These features make them ideal for portable CD players and other portable playback systems.

For more information contact your sales representative (Chapter 7)



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

Semiconductor Corporation

CS5330 CS5331

8-Pin, Stereo A/D Converter for Digital Audio

Features

- Single +3 V or +5 V Power Supply
- 18 Bit Resolution
- 94 dB Dynamic Range
- Linear Phase Digital Anti-Alias Filtering
  0.05dB Passband Ripple
  80dB Stopband Rejection
- Low Power Dissipation: 50 mW
  Power-Down Mode for Portable Applications
- Complete CMOS Stereo A/D System
  Delta-Sigma A/D Converters
  Digital Anti-Alias Filtering
  S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz

General Description

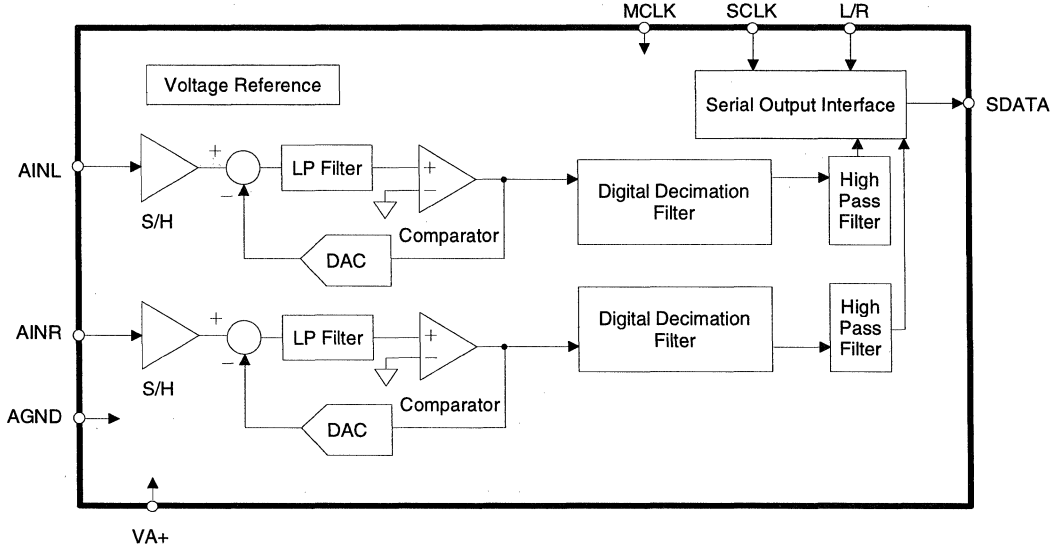
The CS5330/CS5331 are a complete stereo analog-to-digital converter which performs anti-alias filtering, sampling and analog-to-digital conversion generating 18-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

The CS5330/5331 operate from a single +3V or +5V supply and requires only 70 mW for normal operation, making it ideal for battery-powered applications.

The ADC uses delta-sigma modulation with 128X oversampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The linear-phase digital filter has a passband to 21.7 kHz, 0.05 dB passband ripple and >80 dB stopband rejection. The device also contains a high pass filter to remove DC offsets.

The device is available in a 0.208" wide 8-pin SOIC surface mount package.

For more information contact your sales representative (Chapter 7)



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Semiconductor Corporation

16-Bit, Stereo A/D Converters for Digital Audio

Features

- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz
- Low Noise and Distortion >90 dB S/(N+D)
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
  - 0.01dB Passband Ripple
  - 80dB Stopband Rejection
- Low Power Dissipation: 400 mW
  - Power-Down Mode for Portable Applications
- Evaluation Board Available

General Description

The CS5336, CS5338 & CS5339 are complete analog-to-digital converters for stereo digital audio systems. They perform sampling, analog-to-digital conversion and anti-aliasing filtering, generating 16-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

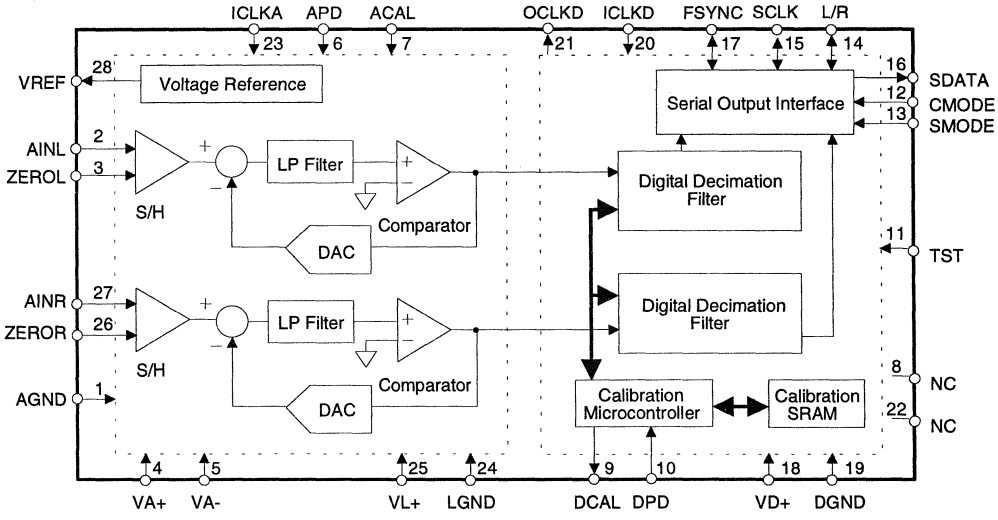
The ADCs use delta-sigma modulation with 64X over-sampling, followed by digital filtering and decimation, which removes the need for an external anti-alias filter.

The CS5336 & CS5338 have an SCLK which clocks out data on rising edges. The CS5339 has an SCLK which clocks out data on falling edges.

The CS5336 has a filter passband of dc to 22kHz. The CS5338 & CS5339 have a filter passband of dc to 24 kHz. The filters have linear phase, 0.01 dB passband ripple, and >80 dB stopband rejection.

The ADC's are housed in a 0.6" wide 28-pin plastic DIP, and also in a 0.3" wide 28-pin SOIC surface mount package. Extended temperature range versions of the CS5336 are also available.

For more information see the 1994 Audio Data Book



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Semiconductor Corporation

CS5389

18-Bit, Stereo A/D Converter for Digital Audio

Features

- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz
- 107 dB Dynamic Range (A-Weighted)
- Low Noise and Distortion
  - 100 dB THD + N
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
- Low Power Dissipation: 550 mW
  - Power-Down Mode
- Evaluation Board Available

General Description

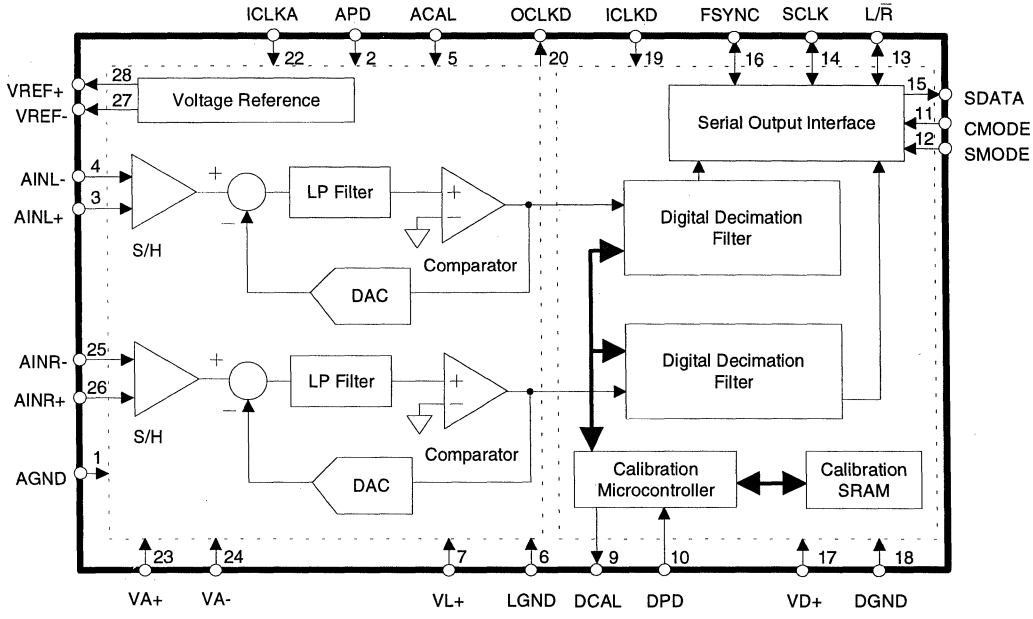
The CS5389 is a complete analog-to-digital converter for stereo digital audio systems. It performs sampling, analog-to-digital conversion and anti-alias filtering, generating 18-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

The CS5389 uses 5th-order, delta-sigma modulation with 64X oversampling followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The ADC uses a differential architecture which provides excellent noise rejection.

The CS5389 has a filter passband of dc to 24kHz. The filters have linear phase, 0.01 dB passband ripple, and >80 dB stopband rejection.

The CS5389 is targeted for the most demanding professional audio systems requiring wide dynamic range and low noise and distortion.

For more information see the 1994 Audio Data Book



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Semiconductor Corporation

CS5390

20-Bit, Stereo A/D Converter for Digital Audio

Features

- 112 dB Dynamic Range (A-Weighted)
- THD + N better than -103dB
- Adjustable System Sampling Rates including 32kHz, 44.1 kHz & 48kHz
- Complete CMOS Stereo A/D System
  - Delta-Sigma A/D Converters
  - Digital Anti-Alias Filtering
  - S/H Circuitry and Voltage Reference
- Internal 64X Oversampling
- Linear Phase Digital Anti-Alias Filtering
  - >100dB StopBand Attenuation
  - 0.005dB Passband Ripple
- Low Power Dissipation: 550 mW
  - Power-Down Mode
- Pin Compatible with CS5389
- Evaluation Board Available

General Description

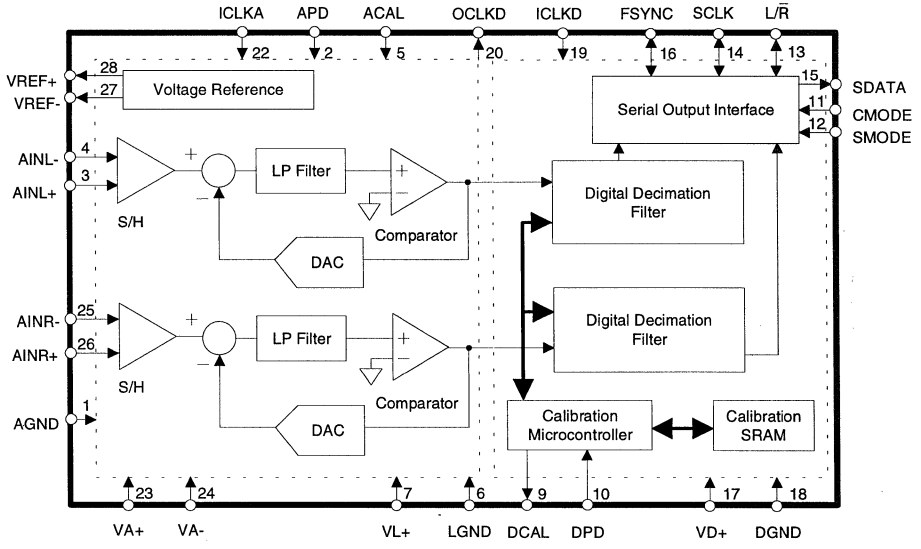
The CS5390 is a complete analog-to-digital converter for stereo digital audio systems. It performs sampling, analog-to-digital conversion and anti-alias filtering, generating 20-bit values for both left and right inputs in serial form. The output word rate can be up to 50 kHz per channel.

The CS5390 uses 5th-order, delta-sigma modulation with 64X oversampling followed by digital filtering and decimation, which removes the need for an external anti-alias filter. The ADC uses a differential architecture which provides excellent noise rejection.

The CS5390 has a filter passband of dc to 21.7kHz. The filters have linear phase, 0.005 dB passband ripple, and >100 dB stopband rejection.

The CS5390 is targeted for the highest performance professional audio systems requiring wide dynamic range, negligible distortion and low noise. Pin compatibility with the CS5389 allows a simple upgrade path without hardware changes.

For more information see the 1994 Audio Data Book



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Semiconductor Corporation

CS8401A CS8402A

Digital Audio Interface Transmitter

Features

- Monolithic Digital Audio Interface Transmitter
- Supports: AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340 Professional and Consumer Formats
- Host Mode and Stand Alone Modes
- Generates CRC Codes and Parity Bits
- On-Chip RS422 Line Driver
- Configurable Buffer Memory (CS8401A)
- Transparent Mode Allows Direct Connection of CS8402A and CS8412 or CS8401A and CS8411A

General Description

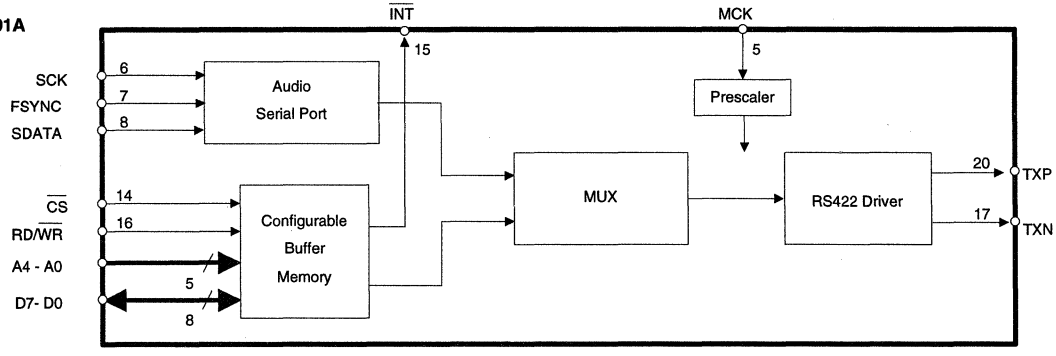
The CS8401/2A are monolithic CMOS devices which encode and transmit audio data according to the AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340 interface standards. The CS8401/2A accept audio and digital data, which is then multiplexed, encoded and driven onto a cable. The audio serial port is double buffered and capable of supporting a wide variety of formats.

The CS8401A has a configurable internal buffer memory, loaded via a parallel port, which may be used to buffer channel status, auxiliary data, and/or user data.

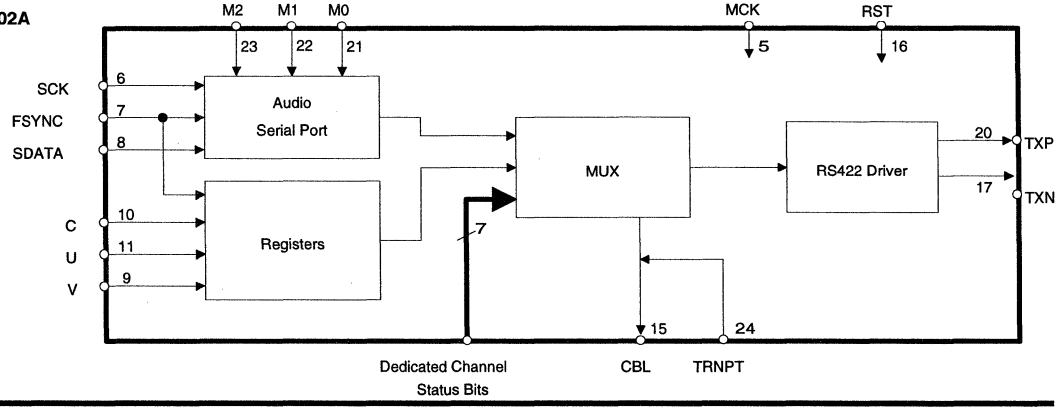
The CS8402A multiplexes the channel, user, and validity data directly from serial input pins with dedicated input pins for the most important channel status bits.

For more information see the 1994 Audio Data Book

CS8401A



CS8402A



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

CS8411 CS8412

Digital Audio Interface Receiver

Features

- Monolithic CMOS Receiver
- Low-Jitter, On-Chip Clock Recovery
  256×Fs Output Clock Provided
- Supports: AES/EBU, IEC 958,
  S/PDIF, & EIAJ CP-340
  Professional and Consumer Formats
- Extensive Error Reporting
  Repeat Last Sample on Error Option
- On-Chip RS422 Line Receiver
- Configurable Buffer Memory (CS8411)

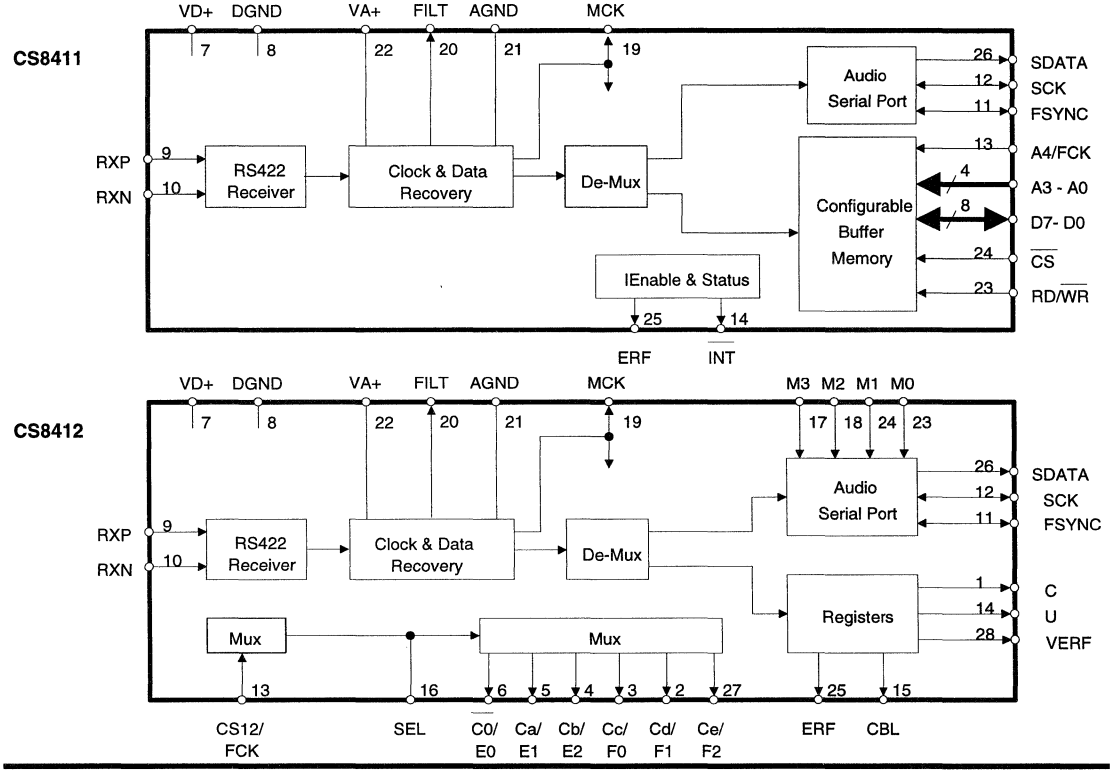
General Description:

The CS8411/12 are monolithic CMOS devices which receive and decode audio data according to the AES/EBU, IEC 958, S/PDIF, & EIAJ CP-340 interface standards. The CS8411/12 receive data from a transmission line, recover the clock and synchronization signals, and de-multiplex the audio and digital data. Differential or single ended inputs can be decoded.

The CS8411 has a configurable internal buffer memory, read via a parallel port, which may be used to buffer channel status, auxiliary data, and/or user data.

The CS8412 de-multiplexes the channel, user, and validity data directly to serial output pins with dedicated output pins for the most important channel status bits.

For more information see the 1994 Audio Data Book



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Semiconductor Corporation

CS8425

A-LAN - Audio Local Area Network Transceiver

Features

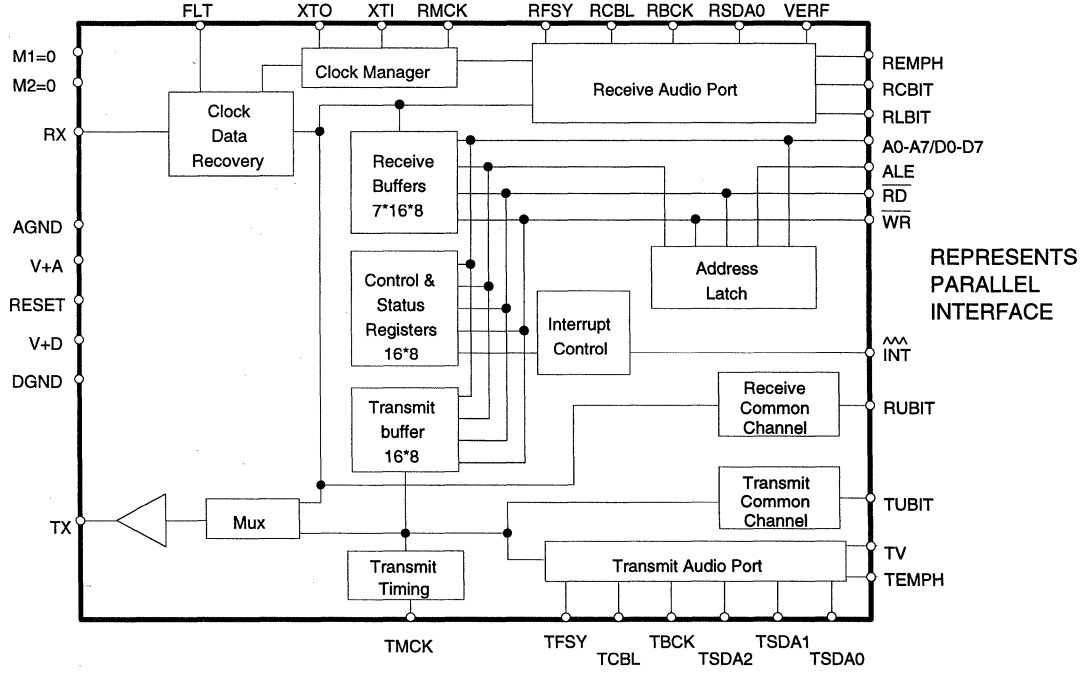
- Monolithic Digital Audio Transceiver for Point-to-Point Transmission of Audio Data
- Supports D2B OPTICAL
- User Channel Used for Communication of System Messages Between Nodes
- Configurable Interface Port Supports SPI, I²C Bus®, Parallel Interface, or the CS8425 Operates as Stand-alone Unit
- Supports Large Number of Nodes per Network
- Also Applicable as General Purpose IEC-958 Digital Audio Transceiver

General Description

The A-LAN chip is a monolithic CMOS circuit that implements the physical layer of an Audio Local Area Network. The A-LAN allows numerous pieces of audio equipment such as CD players, digital equalizers, digital tape decks, DACs, amps, etc. to be connected in a ring topology, sharing audio data from a designated source. Control and configuration messages are passed between nodes via a unique application of the user channel.

Audio data is transmitted using the format specified by IEC-958, and can be generated by any one of multiple nodes on the A-LAN. External drivers and receivers are required for interface to the transmission media.

For more information see the 1994 Audio Data Book



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

Semiconductor Corporation

CS4920A

Multi-Standard Audio Decoder - DAC

Features

- General Purpose Digital Signal Processor Optimized for Audio
  - -24 Bit Fixed Point
  - -48 Bit Accumulator
  - -12.2 MIPS @ 48kHz Sample Rate
- On-Chip Functional Blocks Include:
  - -CD Quality D/A Converter
  - -Programmable PLL Clock Multiplier
  - -AES/EBU - S/PDIF Compatible Digital AudioTransmitter
  - -Audio Serial Input Port
  - -Serial Control Port
- Applications Include:
  - -Audio Decompression
  - -MPEG1 & 2 Layers I, II for:
    - Elementary Streams
    - MPEG1 Packets
    - MPEG2 PES
- Standard 44 pin PLCC Package

General Description

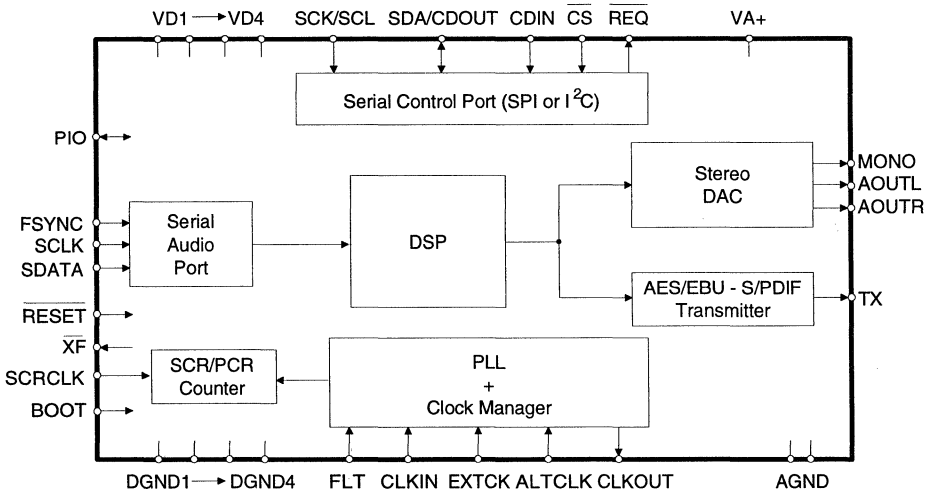
The CS4920A is a complete audio subsystem on a chip. The CS4920A is based on a programmable DSP core and is intended to support a wide variety of digital signal processing applications which include decoding compressed digital audio. Serial audio data broadcast on networks such as cable TV, direct broadcast satellite TV, or the telephone system can be decompressed and converted to standard analog or digital signals.

Both industry standard and proprietary DSP algorithms can be supported. Software which performs industry standard MPEG layers 1 and 2 with support for 48, 44.1, 32, 24, 22.05, and 16kHz sampling and a complete set of software development tools are available. These include an assembler, simulator, and debugger.

PC based software drivers for Windows and DOS are available.

For more information contact your sales representative (Chapter 7)

3



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

Semiconductor Corporation

CS4921

MPEG1,2 Audio Decoder - DAC

Features

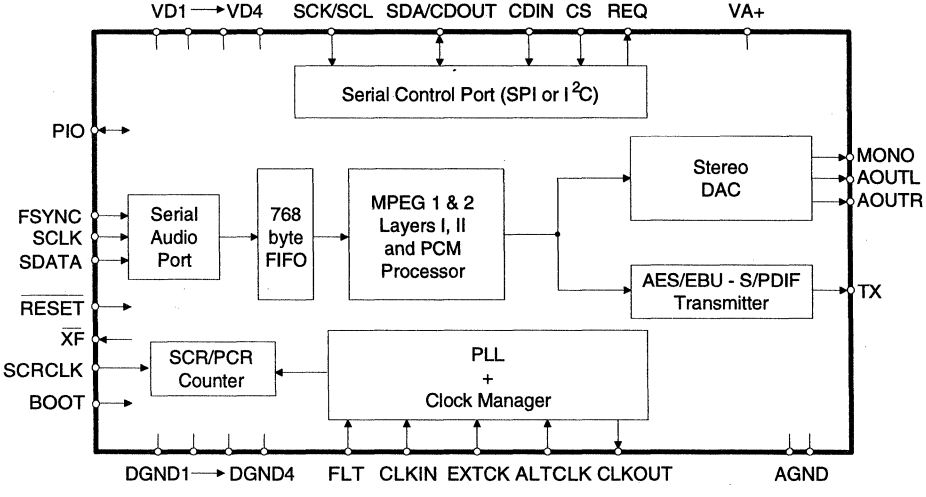
- Fully integrated ISO MPEG audio subsystem
- Supports MPEG Elementary Streams, MPEG1 Packets, MPEG2 PES, and PCM Audio Passthru
- Decompresses Mono, Dual mono, Stereo, Joint stereo
- Supports all samples rates and bit rates
- On-Chip Functional Blocks Include:
  - -CD Quality D/A Converter
  - -Programmable PLL Clock Multiplier
  - -AES/EBU - S/PDIF Compatible Digital AudioTransmitter
  - -Audio Serial Input Port
  - -Serial Control Port
- Standard 44 pin PLCC Package
- Pin Compatible with CS4920A

General Description

The CS4921 is a complete audio subsystem on a chip. This device decompresses the ISO MPEG Layers I and II audio streams with all compliant bit rates and sample rates (including half sample rates). The resulting audio samples are sent to the on-chip 16 bit stereo DAC and optionally to the AES-EBU - S/PDIF output. The internal resolution of the decompressed audio is in excess of 18 bits. This resolution may be realized through the 24 bit architecture of the S/PDIF interface.

The Clock Manager is a programmable PLL which is used to generate the oversample clock for the Delta Sigma DACs. Through this architecture, the CS4921 supports 48kHz, 44.1kHz, 32kHz, 24kHz, 22.05kHz, and 16kHz sample rates by reading the MPEG audio stream information and programming the PLL for the proper operation. This eliminates the requirement for external oscillators for data conversion. PCM sample rates as low as 7kHz are also supported.

For more information contact your sales representative (Chapter 7)



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

Semiconductor Corporation

CS4110
CS4111

Wavetable Sample ROMs for Music Synthesis

Features

- General MIDI compliant melodic instrument and percussion sets
- Sound Canvas™ compatible drum kits, special effects and instruments
- Upgradeable PCM sample set:
  - CS4110, General MIDI plus extras
  - CS4111, optional GS upgrade
  - combined, full Sound Canvas set
- PCM data for nearly 400 sounds (225 instrument sounds, 120 percussion sounds and 48 special effects)
- Compressed data, static, low-power CMOS operation, TTL-compatible I/O

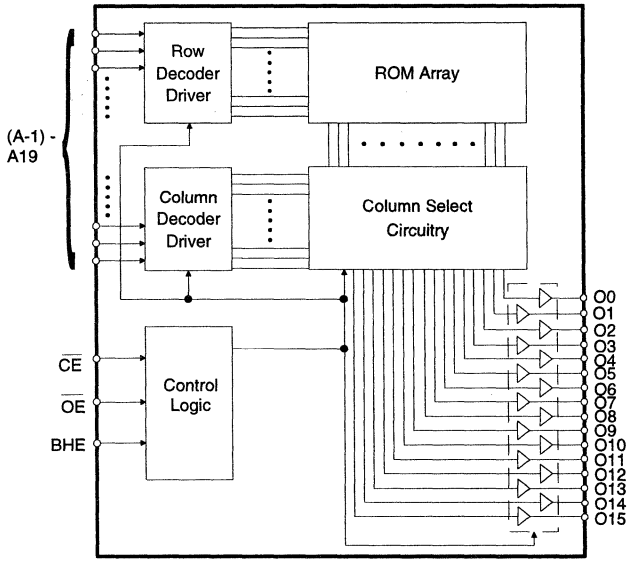
General Description

The CS4110 and CS4111 16-Mbit Read Only Memories (ROMs), contain PCM waveform data used by the Crystal family of wavetable music synthesizers, the CS9203 & CS9233 devices, to produce high fidelity music and special effects. Used with the apprpriate firmware, full General MIDI (GM) compliancy and Roland General Synthesis compatibility (as implemented in the Sound Canvas™) is acheived.

The base sample set is the CS4110; the CS4111 is an optional upgrade/expansion. Combined the devices contain 32-Mbits of PCM data. Proprietary compression and data reduction techniques were used to minimize storage requirements.

The CS4110 and CS4111 offer a power-down mode controlled by the Chip Enable $\overline{CE}$ input.

For more information contact your sales representative (Chapter 7)



GENERAL MIDI INSTRUMENT

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

Semiconductor Corporation

CS4112

Wavetable Sample ROM for Music Synthesis

Features

- General MIDI compliant melodic instrument and percussion sets
- Sound Canvas™ compatible drum kits and special effects sounds
- Compressed data may be used to generate up to 343 sounds (190 instrument sounds, 107 percussion sounds and 46 special effects)
- Low-power operation:
  Operating current: 15 mA (max.)
  Standby current: 100 µA (max.)
- Static CMOS operation, TTL-compatible I/O

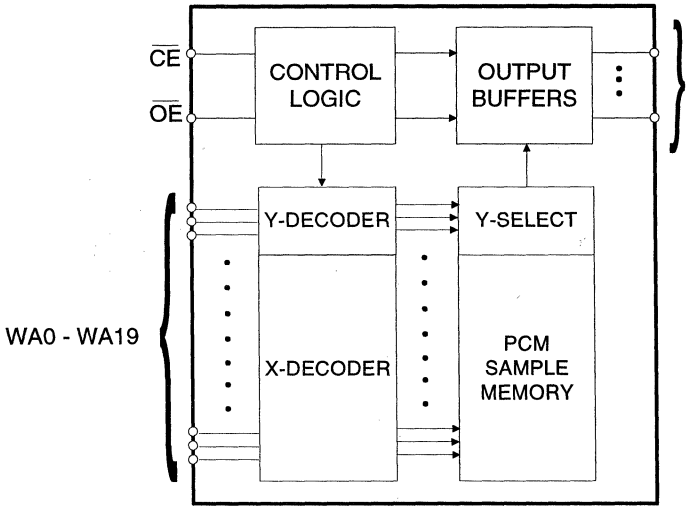
General Description

The CS4112 Read Only Memory (ROM), organized 1M x 8bits, contains PCM waveform data used by the CS9203/CS9233 family of wavetable music synthesizers and associated firmware to provide complete General MIDI (GM) compliant and Roland General Synthesis (GS) compatible instrument sound sets.

Proprietary compression and data reduction techniques were used to minimize stored data. When combined with Crystal's high-quality music synthesis algorithms (implemented in the CS9203/CS9233 devices) high fidelity music and special effects result.

The CS4112 offers a power-down mode controlled by the Chip Enable $\overline{CE}$ input.

For more information contact your sales representative (Chapter 7)



GENERAL MIDI INSTRUMENT

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 462 2723

Semiconductor Corporation

CS4215

16-Bit Multimedia Audio Codec

Features

- Sample Frequencies from 4 kHz to 50 kHz
- 16-bit Linear, 8-bit Linear, μ-Law, or A-Law Audio Data Coding
- Programmable Gain for Analog Inputs
- Programmable Attenuation for Analog Outputs
- On-chip Oscillators
- +5V Power Supply
- Microphone and Line Level Analog Inputs
- Headphone, Speaker, and Line Outputs
- On-chip Anti-Aliasing/Smoothing Filters
- Serial Digital Interface

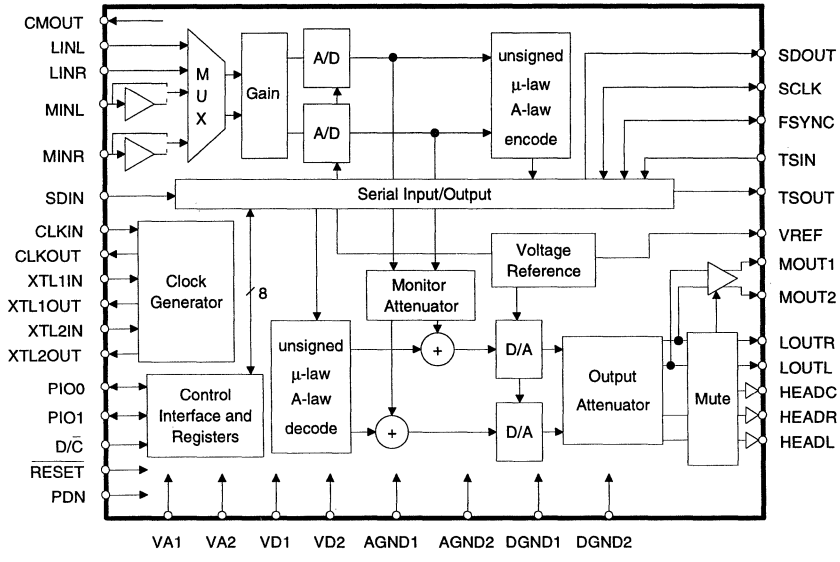
General Description

The CS4215 is a single-chip, stereo, CMOS multimedia codec that supports CD-quality music, FM radio-quality music, telephone-quality speech, and modems. The analog-to-digital and digital-to-analog converters are 64xoversampled delta-sigma converters with on-chip filters which adapt to the sample frequency selected.

The +5V only power requirement makes the CS4215 ideal for use in workstations and personal computers.

Integration of microphone and line level inputs, input and output gain setting, along with headphone and monitor speaker driver, results in a very small footprint.

For more information see the 1994 Audio Data Book



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Semiconductor Corporation

CS4216

16-Bit Stereo Audio Codec

Features

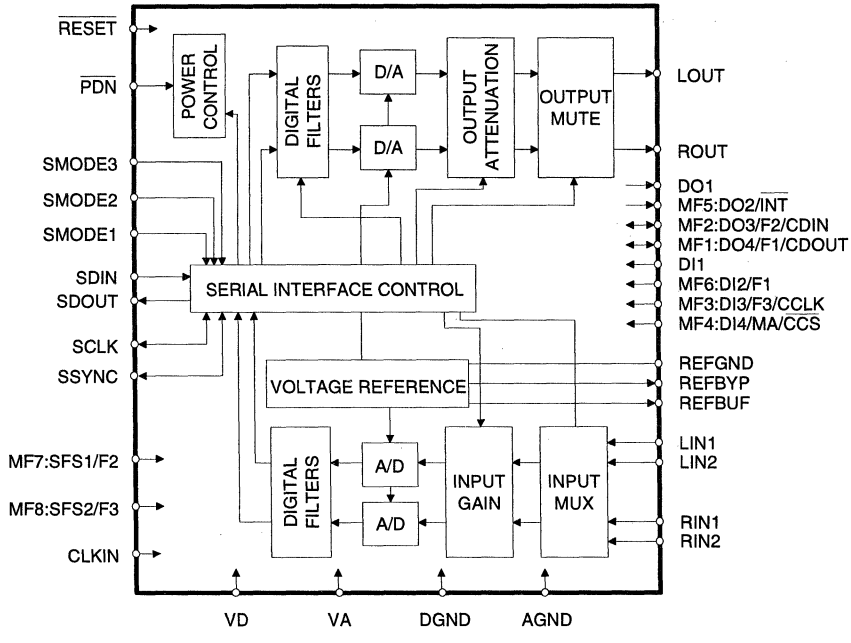
- CMOS Stereo Audio Input/Output System
  - Delta-Sigma A/D Converters
  - Delta-Sigma D/A Converters
  - Input Anti-Aliasing and Output Smoothing Filters
  - Programmable Input Gain and Output Attenuation
- Sample Frequencies of 4 kHz to 50 kHz
- CD Quality Noise and Distortion < 0.01 %THD
- Internal 64X Oversampling
- Low Power Dissipation: 80 mA
  1 mA Power-Down Mode

General Description

The CS4216 Stereo Audio Codec is a monolithic CMOS device for computer multimedia, automotive, and portable audio applications. It performs A/D and D/A conversion, filtering, and level setting, creating 4 audio inputs and 2 audio outputs for a digital computer system. The digital interfaces of left and right channels are multiplexed into a single serial data bus with word rates up to 50 kHz per channel. Up to 4 CS4216 devices can be attached to a single hardware bus.

Both the ADCs and the DACs use delta-sigma modulation with 64X oversampling. The ADCs include a digital decimation filter which eliminates the need for external anti-aliasing filters. The DACs include output smoothing filters on-chip.

For more information see the 1994 Audio Data Book



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Semiconductor Corporation

CS4225

Digital Audio Conversion System

Features

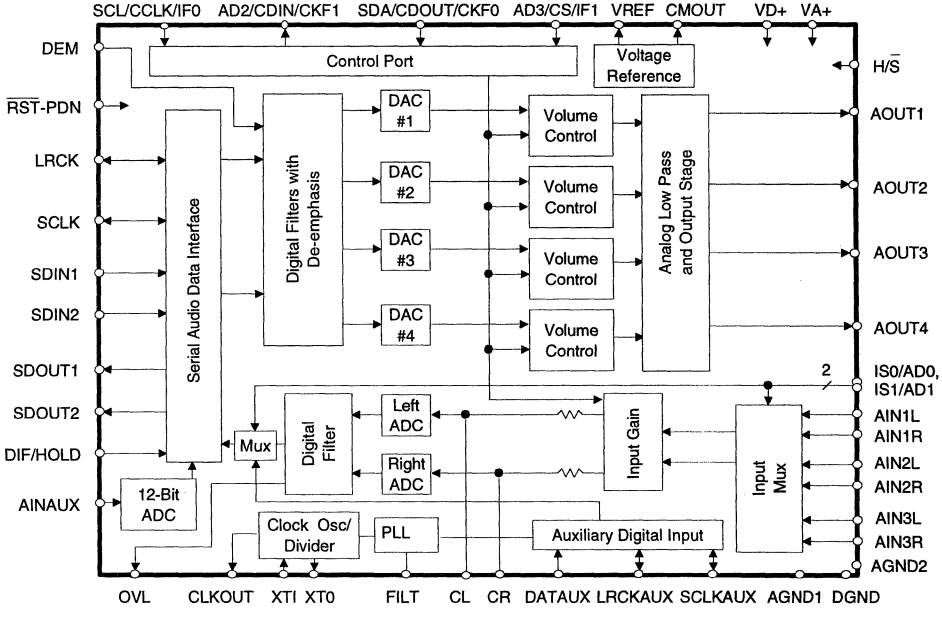
- Stereo 16-bit A/D Converters
- Quad 16-bit D/A Converters
- Sample Rates From 4kHz to 50kHz
- >100 dB DAC Signal-to-Noise Ratio
- Variable Bandwidth Auxiliary 12-bit A/D
- Programmable Input Gain & Output Attenuation
- +5V Power Supply
- On-chip Anti-aliasing and Output Smoothing Filters
- Error Correction and De-Emphasis

Description

The CS4225 is a single-chip, stereo analog-to-digital and quad digital-to-analog converter using delta-sigma conversion techniques. Applications include CD-quality music, FM radio quality music, telephone-quality speech. Four D/A converters make the CS4225 ideal for surround sound and automotive applications.

The CS4225 is supplied in a 44-pin plastic package with J-leads (PLCC).

For more information see the 1994 Audio Data Book



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Semiconductor Corporation

CS4231A

Parallel Interface, Multimedia Audio Codec

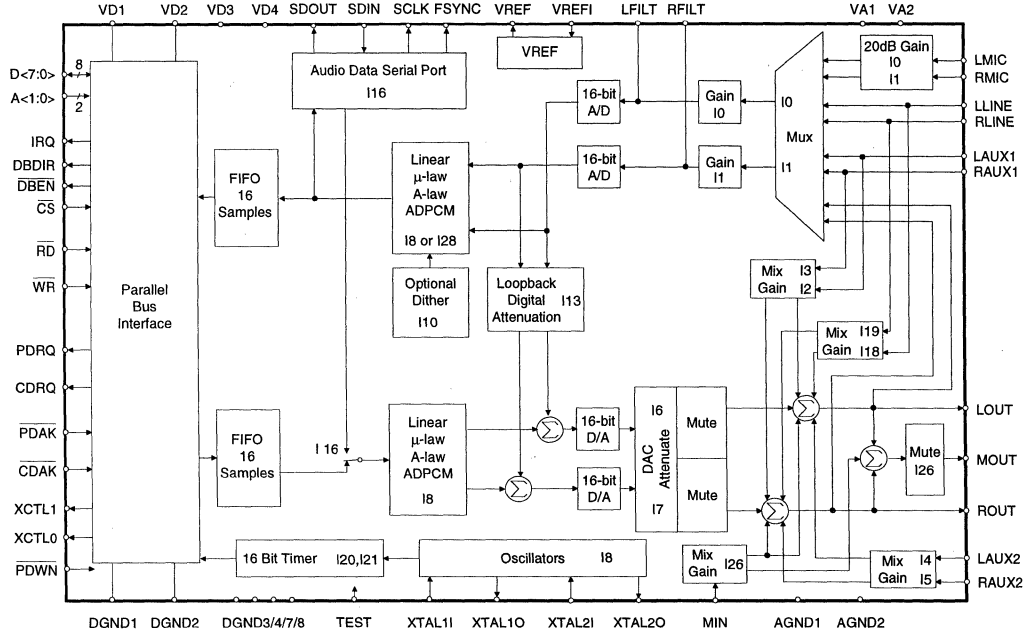
Features

- Windows Sound System™ Compatible Codec
- ADPCM Compression/Decompression
- Extensive Software Support
- MPC Level 2 Compatible Mixer
- Dual DMA Registers support Full Duplex Operation
- On-Chip FIFOs for higher performance
- Selectable Serial Audio Data Port
- Pin Compatible with CS4231/CS4248

General Description

The CS4231A includes stereo 16-bit audio converters and complete on-chip filtering for record and playback of 16-bit audio data. In addition, analog mixing and programmable gain and attenuation are included to provide a complete audio subsystem. A selectable serial port can pass audio data to and from DSPs or ASICs. High-performance software drivers for various operating systems are available that support all the CS4231A features including full duplex transfers. The CS4231A is a pin compatible upgrade to the CS4231 and CS4248.

For more information contact your sales representative (Chapter 7)



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

CRYSTAL
Semiconductor Corporation

CS4232

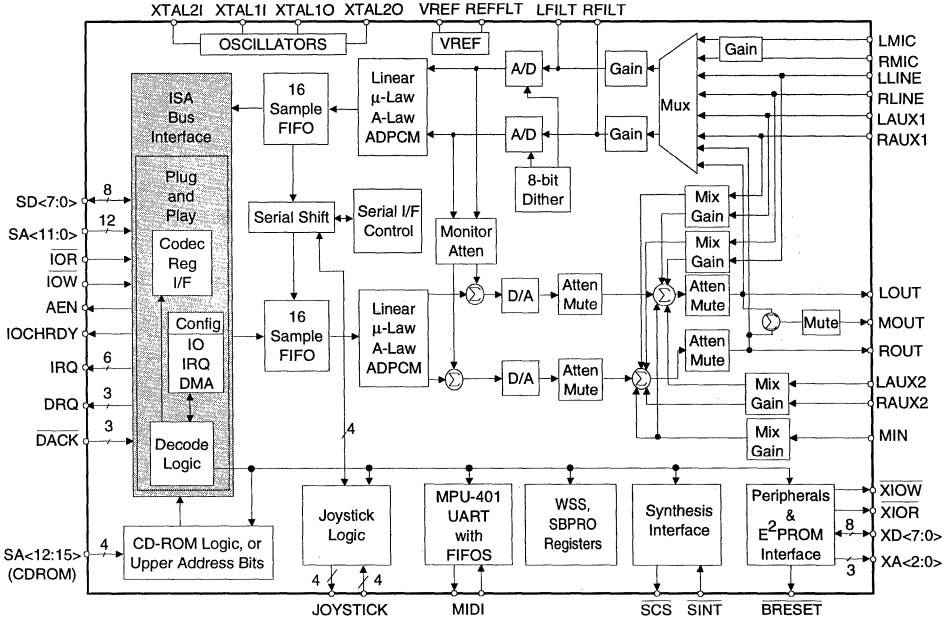
Games Compatible Plug-and-Play Audio System

- Compatible with Sound Blaster™, Sound Blaster Pro™, and Windows Sound System™
- Fully Plug and Play Compatible
- Industry Leading Delta-Sigma Data Converters
- ADPCM, μ-Law & A-Law Compression/Decompression
- Dual DMA Support w/FIFOs, Full Duplex Operation
- MPC Level-2 Compatible Mixer
- Joystick Port and MPU-401 Compatible MIDI Interface
- Optional CD-ROM Interface
- External FM and Wave Table Synthesizer Support
- Serial Audio Data Port
- 24 mA TTL Bus Drive Capability
- Software Programmable Power Management
- 16-Bit Address Decode Support
- CS4231/CS4248 Register Compatible

General Description

The CS4232 is a single chip multimedia audio system controller and codec that provides compatibility with ISA Plug and Play, the Microsoft Windows Sound System, and will run software written to the Sound Blaster and Sound Blaster Pro interfaces. The CS4232 integrates an advanced industry-standard Delta-Sigma codec with extended signal processing in a high-performance mixed-signal design. The CS4232 also contains expansive mixing capabilities, an MPU-401 UART, joystick logic, and interfaces for a music synthesizer and a CD-ROM.

For more information contact your sales representative (Chapter 7)



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

Semiconductor Corporation

CRD4232-1

16-bit Low-Cost Audio Adapter Reference Design

Features

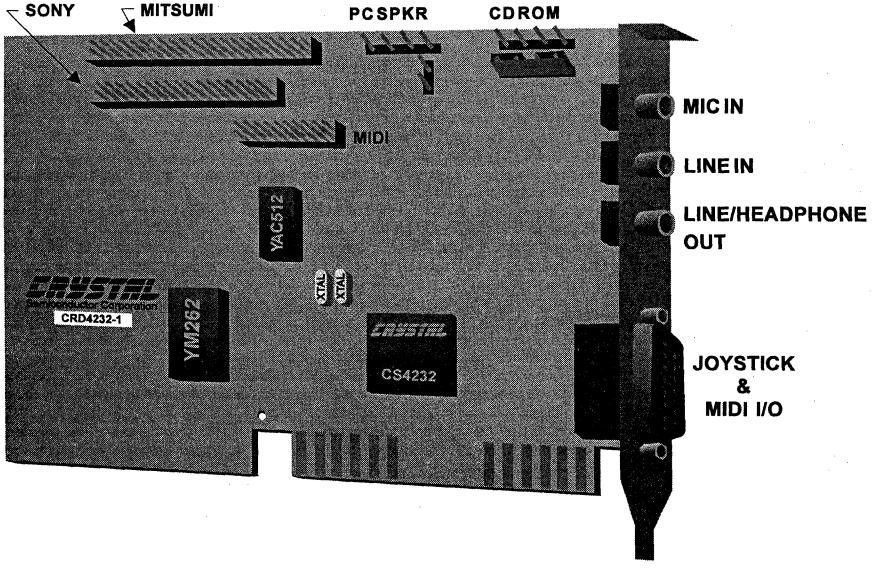
- MPC2 compliant (with enhancements), Windows Sound System™, DOS Games and AdLib™ compatible
- Low Cost Two-Sided Board that Sustains CS4232 Quality
- WaveBlaster™ compatible MIDI Interface & Joystick/MIDI Interface
- Extensive Stuffing Options:
  - Mono In / Mono Out
  - Headphone Drive
  - Microphone Preamp
  - CDROM

General Description

The CD-quality CRD4232-1 reference design is fully MPC2 compliant, Ad Lib, DOS Games and Windows Sound System compatible. The design is a half size two-sided ISA-bus PC adapter board, based on the CS4232 Multimedia Audio Codec and Yamaha's YM262 FM based music synthesizer (OPL3). Optionally the CRD9203 Wavetable Music Synthesizer Daughtercard may be installed on the design.

The CRD4232-1 supports many build options providing the OEM with flexability in cost verses functionality or performance.

For more information contact your sales representative (Chapter 7)



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

Semiconductor Corporation

CS4248

Parallel Interface, Multimedia Audio Codec

Features

- Integrated parallel interface to ISA and EISA buses
- Stereo Digital Audio at sample rates from 4 kHz to 50 kHz with 16-bit resolution.
- DMA Transfers with on-chip FIFOs
- Free Window™ Software Drivers
- Linear, μ-law, and A-law coding
- Pin compatible with the AD1848 (PLCC)

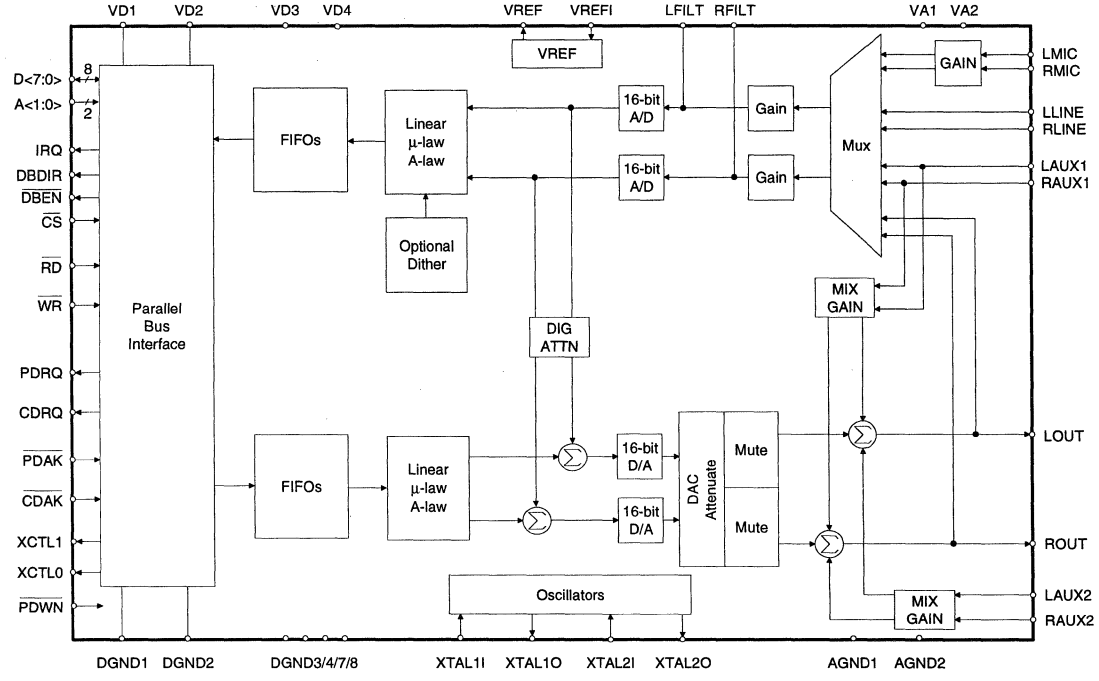
General Description

The CS4248 is an Mwave™ audio codec.

The CS4248 is a mixed signal integrated circuit that provides 16-bit audio for computer multimedia systems. The CS4248 includes stereo audio converters and complete on chip filtering for record and playback of 16-bit audio data. The CS4248 combines conversion, analog mixing, and programmable gain and attenuation to provide a complete audio subsystem in a single 68-pin PLCC or 100-pin TQFP package. The CS4248 includes an 8-bit parallel interface to the industry standard ISA bus.

For more information see the 1994 Audio Data Book

3



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

Semiconductor Corporation

CS8905C

GS Format Compliant Musical Effects Processor

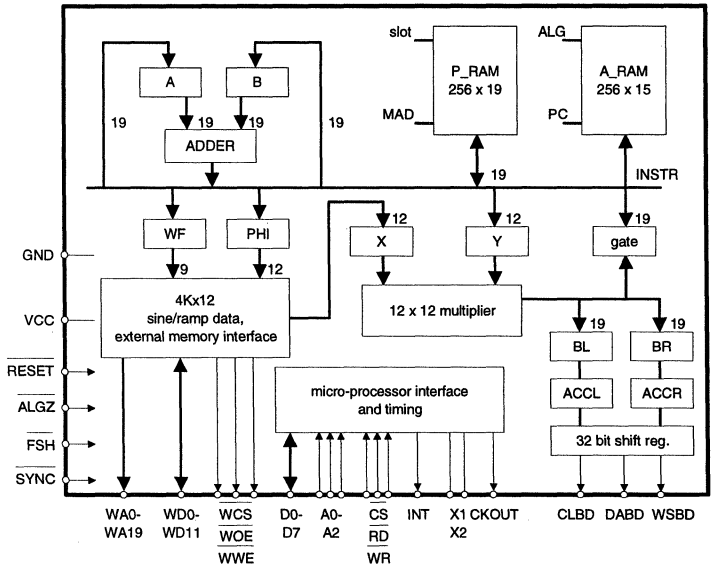
Features

- Upgrades the CS9233 Wavetable Syntheiszer with Effects
- Reverb, Chorus, Flange, etc.
- Improves subjective quality of music
- Full Roland GS format compliant
- 2x performance of original CS8905
- Stereo 16-bit digital audio output returned to CS9233 for mixing
- On-chip Algorithm and Parameter RAM, permits field upgrades
- 68 pin PLCC or 80-pin TQFP packages

General Description

The CS8905C is a high performance programmable signal processor, specially designed as a digital effects processing engine for music and sound generation applications. With the appropriate firmware, full General MIDI (GM) and General Synthesis (GS) compliant musical effects processing is possible. The Roland GS format has become the defacto world-wide standard for controlling effects processing in a MIDI environment. With effects, the subjective quality of music improves greatly. The CS8905C features 19-bit internal data paths, a 19-bit two's complement adder, a 12 x 12 two's complement multiplier, two 24-bit accumulators and a 32-bit output shift register, operating at a clock frequency of 64MHz. Complete refernce designs together with the CS9233 Integrated Wavetable Synthesizer are available.

For more information contact your sales representative (Chapter 7)



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 462 2723

Semiconductor Corporation

CS9233

Integrated Wavetable Music Synthesizer

Features

- Integrated synthesizer combines a RISC-based DSP and a flexible CISC micro-controller on a single chip
- 32-note polyphony, 32-part multi-timbral at 31.25kHz output rate
- Dos Games compatible synthesis
- 18-bit audio output directly supports the 96 dB CS4331 Stereo DAC
- Glueless interface to external ROM/DRAM for PCM samples
- Direct support for the optional CS8905 Programmable Effects Processor
- Independent control of reverb and chorus send levels for each voice

General Description

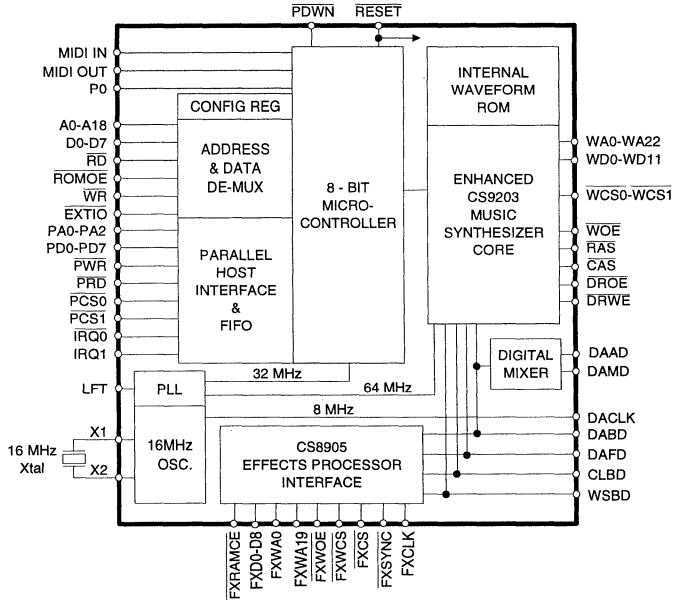
The CS9233 is a highly integrated music synthesizer circuit designed for PC multimedia, musical instrument, Karaoke, arcade game and set-top applications. Interface logic is included on-chip for glueless connections to external memory, DAC circuitry and an optional effects processor.

When the CS9233 is combined with PCM sample data and associated firmware, full General MIDI (GM), Roland General Synthesis (GS), Microsoft Windows, and MPC level 2 compliancy is acheived (including recommendations for enhanced multi-timbral synthesizers).

In addition to standard serial MIDI I/O, a parallel ISA-bus interface has been provided, permitting emulation of the common register sets (e.g. MPU-401 UART mode) needed for DOS games compatibility.

For more information contact your sales representative (Chapter 7)

3



GENERAL MIDI INSTRUMENT

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

Semiconductor Corporation

CRD9233-1

Wavetable Synthesizer w/ 16-bit Audio

Features

- General MIDI compliant, GS compatible (totals 343: instruments; variations; drum sets and special effects sounds) DRAM support for down-loadable fonts
- AdLib™ , SoundBlaster Pro™, Windows Sound System™, MT-32 and Roland Sound Canvas™ compatible. MPC2 compliant, Windows '95 ready
- Extensive feature list:
  Joystick/MIDI Interface
  PC Speaker I/O
  Line/Headphone Driver
  Microphone Preamp
  Phantom Power Support
  CDROM:IDE, Panasonic, Sony, Mitsumi

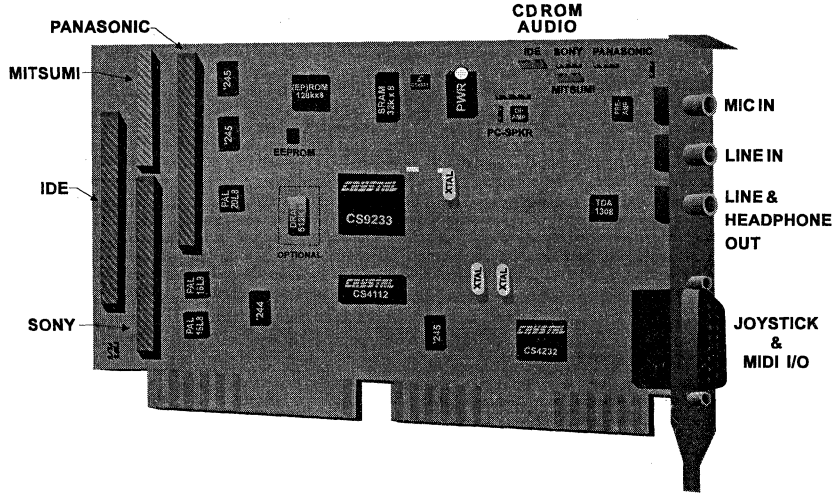
General Description

The CRD9233-1 Reference Design features outstanding sound-quality, high-compatibility and low-cost. The reference design integrates a fully General MIDI (GM) compliant, General Synthesis (GS) format compatible wavetable music synthesizer with an MPC2 compliant, Ad Lib, MT-32, Sound Blaster Pro and Windows Sound System compatible CD-quality audio design.

The board is a half size ISA-bus PC adapter, based on the CS9233 Integrated Wavetable and Algorithmic Music Synthesizer, the CS4112 CrystalClear™ Wavetable 8Mbit PCM sample ROM, the CS4331 18-bit Delta-Sigma DAC, and the CS4232 Plug-and-Play Games Compatible Multimedia Audio Sub-system.

The manufacturing kit includes: schematics; board layouts; bill of materials; user's manual; software technical manual; DOS utility software; Windows 3.1 driver object code (Win '95, NT & OS/2 in development); volume & mixing control applets; recorder/player applet, synthesizer control applet; MIDI drivers; etc.

For more information contact your sales representative (Chapter 7)



GENERAL MIDI INSTRUMENT

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 462 2723

Semiconductor Corporation

CRD9233-2

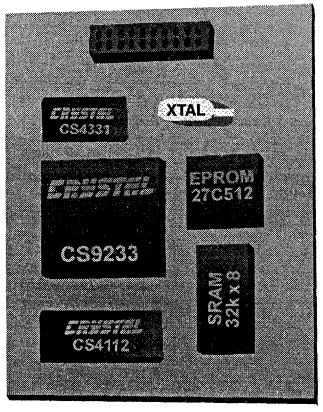
GS/GM Music Synthesizer Daughtercard

- Professional quality General MIDI music synthesis for the Multimedia PC
- Low-cost implementations with WaveBlaster™ compatible connector
- 32-note polyphony, 16-part multi-timbral, 31.25 kHz output sample rate
- Supports Roland GS bank select and GS envelope and filter controls
- 343 quality instrument sounds, w GS special effects and drum kits
- Complete manufacturing kits available

General Description

The CRD9233-2 is a low-cost wavetable synthesizer daughtercards based on the CS9233 Integrated Wavetable Synthesizer IC. This General MIDI synthesizer is implemented as a daughter card subsystem for a Personal Computer audio adapter (sound card). The host interface connector and pin-out is compatible with the Creative Labs Sound Blaster 16™ and Wave Blaster™ products. The CRD9233-2 plugs directly onto a host sound card, such as the Sound Blaster 16; Sound Galaxy NX Pro 16, AudioWave Platinum 16, or the CRD4231 reference design, to provide professional quality MIDI music synthesis in the PC environment. The exceptional sound quality of this design makes it an ideal choice for business multimedia, education, entertainment, computer games, or music composition applications.

For more information contact your sales representative (Chapter 7)



GENERAL MIDI INSTRUMENT

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 462 2723

Semiconductor Corporation

DRIVERS

CS4231A and CS4232 Device Drivers

Features

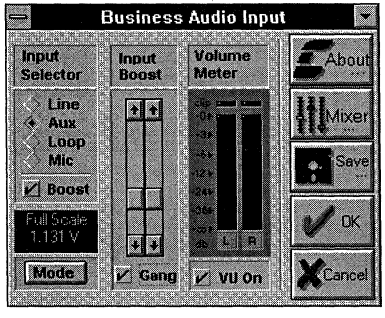
- Support wave audio capture, playback under Windows 3.1 & NT
- Highly optimized code for maximum throughput, minimum CPU utilization
- Input & Output volume/mixing control
- Support ADPCM compression & decompression
- Full Duplex audio capture & playback
- Complete with installation routines, documentation, etc.

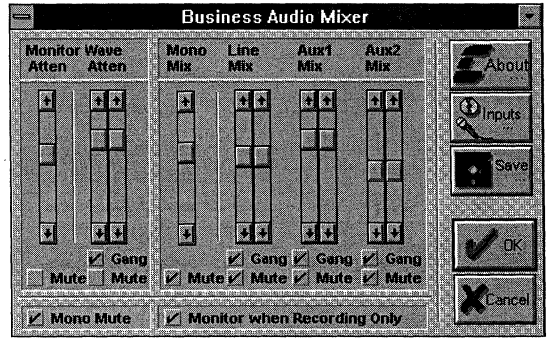
General Description

Crystal offers complete wave driver support for the Microsoft Windows 3.1 & NT environments. CS4231A and CS4232 drivers support full duplex operation -- i.e. simultaneous capture and playback. Full duplex permits voice recognition to control multimedia playback. Control panel applets are provided supporting all features of the Crystal codec devices. Functions include: 1) Input control panel used to select audio source and individually set the gain level, turn dither on/off, and visually monitor recording levels with a VU meter; 2) Output control panel used to control volume, mixer levels and loopback monitoring; 3) Recorder applet used to capture and playback .WAV files, at various sample frequencies, with compression & de-compression (ADPCM, ULaw & ALaw). The recorder is an OLE server.

All source code was developed in-house. Object code is provided without licensing fees directly by Crystal. Sample copies are available.

For more information contact your sales representative (Chapter 7)





Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

Multimedia Audio Codec Diagnostic Software

Features

- Development and manufacturing test support for the CS4248, CS4231A, & CS4232
- Control over every feature & function - automated board test features
- Measure Codec performance without need of an external signal source
- Record and playback .WAV files in the DOS environment
- Real-time FFT, time and frequency-response plots

General Description

The diagnostics program for the Crystal codecs assists in every phase of PC audio sub-system design. From initial board bring-up and functional testing to factory test and field service, the diagnostics provide in-depth information to the engineer regarding audio performance and function.

Detailed reporting capabilities aid in both burn-in and board debug. The diagnostics support communication through input and output files, as well as DOS exit codes, allowing it to be spawned by another program and return meaningful results. A system-level diagnostics/factory test system could thus use the program while retaining its' own user interface routines.

The diagnostics run under DOS, and are controlled by a command line interface optimized for minimum keystrokes. Sample 'C' source code is available detailing how to call the routines from inside a host program.

All source code was developed in-house by Crystal. Object code is provided to OEMs without charge. Sample copies are available.

For more information contact your sales representative (Chapter 7)

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

Semiconductor Corporation

CWDRGNTT

Talk→To Voice Recognition from Dragon Systems

Features

- World's foremost voice recognition
- Supports popular Windows apps.
- Hands free command & control in the Windows 3.1 environment
- Reduces typing for data entry
- Speaker independent - also supports regional dialects through training
- Supports 64 active commands; context sensitive for unlimited recognition

General Description

Talk→To is a powerful and flexible voice recognition package for the Microsoft Windows 3.1 environment. Voice recognition enhances productivity by allowing users to enter simple voice commands, instead of complicated keystrokes or multiple mouse movements, to choose menu and control options. Voice recognition redefines the human/computer interface, making it truly intuitive. Talk→To is highly speaker independent, yet may be quickly trained to support an individual's speaking style, thus handling regional or foreign accents.

Crystal Semiconductor has a strategic relationship with Dragon Systems to allow OEMs to integrate voice recognition capabilities into their products. Crystal licenses the products directly to OEMs.

Sample copies are available free of charge; license fees for production are volume dependent.

For more information contact your sales representative (Chapter 7)

Product Preview

This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

Semiconductor Corporation

CWMNLG

First Byte's Monologue for Windows

Features

- Monologue Text-To-Speech synthesis software from First Byte.
- Industry leading text-to-speech
- Allows Windows applications to speak
- Permits efficient proof-reading of text and numerical data
- Multilingual: French, German, Spanish and American available now; Italian, British and Japanese in development
- Transfer data through clipboard or direct DLL/DDE link

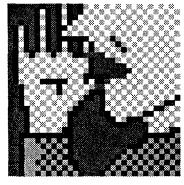
General Description

Monologue increases productivity in the business environment, allowing users to add speech capabilities to any Windows (or DOS) application. Any pronounceable combination of letters and numbers will be spoken clearly. No voice recording or speech training is necessary. Customizable speech parameters permit control of volume, pitch and speed. An exception dictionary allows the user to save preffered pronounciations of words and abbreviations.

Crystal Semiconductor has a strategic relationship with First Byte to allow OEMs to integrate speech capabilities into their products. Crystal licenses the products directly to OEMs.

Sample copies are available free of charge; license fees for production are volume dependent.

For more information contact your sales representative (Chapter 7)



Monologue
16-bit

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 Fax: (512) 445 7581

• Notes •

INFRARED TRANSCEIVER

CS8130 IrDA Transceiver

The CS8130 Multi-Standard Infrared Transceiver adds an IR port to a standard UART, and implements the IrDA (Infrared Data Association) physical-layer. Other standards supported are HP-SIR, ASK and TV remote. The computer data port is standard UART TxD and RxD compatible, and operates from 1200 to 115200 baud. The CS8130 uses an external PIN diode and transmit LED.

ECHO CANCELLERS

CS6400 Echo Cancelling Codec

The CS6400 is a low-cost voiceband echo cancellation product with integrated codec and program ROM. The CS6400 which can be used in full-duplex speakerphones, cellular phones, base stations, personal digital assistants, video-teleconferencing and long-distance telephone lines. This circuit contains an embedded, low-cost, application-specific DSP, and can cancel up to 64 ms of acoustic or network echo.

CS6401 Programmable Echo Canceller

The CS6401 is a general-purpose voiceband echo cancellation product. This circuit contains an embedded, low-cost, application-specific DSP, and can cancel up to 64 ms of acoustic or network echo. The program code is loaded from an external ROM, allowing Crystal to tailor functionality for specific applications.

COMMUNICATION CODECS

Crystal Semiconductor offers a broad variety of technology for processing voiceband and radio baseband signals. The CS645x series of products are representative of Crystal's ability to apply its delta-sigma converter technology to specific communication applications. Crystal will develop custom codec circuits for high-volume applications.

CS6450 I&Q Baseband Codec for IS-54

The CS6450 supports CDPD and TDMA cellular phones, and provides a baseband interface between a DSP and a radio module.

CS6453 Alternate Voice/data Codec

The CS6453 supports high-performance modems, and provides a voiceband interface between a DSP and a direct access arrangement.

ETHERNET/CHEAPERNET

CS83C92 Ethernet Transceiver

Crystal is the first company to bring the benefits of low-power CMOS technology to Ethernet/Cheapernet transceivers. The CS83C92C uses up to 40 percent less power than the DP8392A and DP8392B. This translates into increased reliability and compatibility with surface-mount technology. The CS83C92C is the first Ethernet transceiver that is fully compliant with ISO/IEEE 802.3

CS8900 Ethernet Controller

The CS8900 is a low-cost Ethernet LAN Controller optimized for ISA PC motherboards. Its highly-integrated design results in the industry's smallest-footprint solution. The small footprint results from the 14mm by 14mm 100-pin TQFP package, and through the elimination of external components. The CS8900 includes on-chip RAM, 10BASE-T transmit and receive filters, and a no-glue ISA-Bus interface with 24 mA drivers. In addition to saving cost and board space, the internal filters simplify the task of achieving FCC Part 15 Class B certification.

Crystal provides a complete set of certified CS8900 drivers for all major operating systems and network operating systems. Motherboard applications are further supported by the following leadership performance-oriented features: advanced power management, full-duplex operation, Stream Transfer™, and DMA-auto-switch. The CS8900's patented PacketPage™ architecture automatically adapts to changing network traffic patterns and available system resources. The result is increased system efficiency and minimized CPU overhead.

TELECOM

T1 Framer

Crystal Semiconductor's CS2180B T1 Framer is a perfect companion to our T1 line interface ICs. This device handles encoding and decoding of all T1 frame formats (SF, SLC-96 and T1DM and ESF). Serial interface and control registers make it simple to configure from a microprocessor, including per-channel control options. Packages available include 40-pin DIP or 44-lead PLCC.

While maintaining 100% compatibility, Crystal has improved on industry-standard 2180 designs:

- Support of SLC-96 & T1DM formats
- Compliance with TR-TSY-000191 AIS detection criteria
- Compliance with Bellcore Loss-of-Carrier detection criteria
- Buffered serial data interface, eliminating need for SDI to be valid for both edges of SCLK
- Industrial temperature operating range

Crystal also manufactures a CS2180A framer.

T1, E1 and ISDN Primary Rate Line Interface Circuits

Crystal Semiconductor offers a broad family of low-power CMOS PCM line interface circuits, with each device optimized for a unique system application. Since introducing the industry's first T1 (1.544 MHz) and E1 (2.048 MHz) line interface circuits (the CS61534 and CS61544), Crystal has shipped more CMOS PCM line interface ICs than any other vendor worldwide. Crystal Semiconductor's leadership continues with the best-in-class transmitter return loss, short-circuit current limiting, pulse shapes, jitter attenuation, jitter tolerance and low power consumption. The CS61304A, CS61305A, and CS61577 are upgraded devices for existing designs. The CS61535A, CS61574A, CS61575 and CS61584 are recommended for use in new designs.

CS61535A: Enhanced transmit-side jitter attenuator supports SONET VT1.5 and VT2, and other high speed transmission systems such as digital microwave radio and M13 multiplexers.

CS61574A: Receive-side jitter attenuation supports line cards in synchronous switching systems (such as central offices, PBXs and 0/1 digital cross connects).

CS61575: Receive-side jitter attenuation with extended FIFO length supports loop-timing in AT&T 62411 compatible customer-premises equipment.

CS61584: The industry's first 3.3V or 5V, dual Line Interface Unit. Intended for high-density line cards. Fully software configurable between T1 and E1 rates with no changes required to external components.

CS61304A and CS61305A: These ICs' low-impedance transmit drivers allow the ICs to be used in boards currently employing the LXT304A or LXT305A. Advantages over the LXT304/5A include lower power consumption, optional internal B8ZS/AMI/HDB3 coder and receive AIS detection.

CS61577: A 100% drop-in replacement for the CS61574 which uses the same transformers. Enhancements include transmitter short-circuit current limiting, driver immunity to reflected pulses, lower power consumption, optional B8ZS/AMI/HDB3 coder, and software selection between 75Ω and 120Ω E1 output options. The CS61577 also replaces the LXT300Z

Quartz Crystals

To complement our family of T1/E1 Line Interface circuits, Crystal Semiconductor supplies pullable quartz crystals. The CXT6176 (for T1 applications) and the CXT8192 (for E1 applications) are designed for 100% compatibility with Crystal's line interface units and jitter attenuators.

Table 1: Line Interface Units

Product	CS61535A	CS61574A	CS61575	CS61584
Number of Channels	1	1	1	2
Power Supply	5V	5V	5V	3.3V of 5V
Transmitter Matches Impedance of Line?	yes	yes	yes	yes
Transmitter Short-circuit Current Limiting?	yes	yes	yes	yes
Location of Jitter Attenuator	Transmit	Receive	Receive	Programmable (xmit, rcvr, none)
Jitter Attenuator FIFO length	32 bits	32 bits	192 bits	64 bits
Control Modes	Serial & hardware	Serial & hardware	Serial & hardware	Serial, parallel & hardware
100% software switchable between T1 & E1	-	-	-	yes
Optional B8ZS, HDB3, AMI Coder	yes	yes	yes	yes
Package	28-pin PDIP & PLCC	28-pin PDIP & PLCC	28-pin PDIP & PLCC	64-pin TQFP & 68-pin PLCC
JTAG	-	-	-	yes

CONTENTS

See the 1994 Crystal Communication Data Book
for the complete data sheets on the above products

Semiconductor Corporation

CS8130

Multi-Standard Infrared Transceiver

Features

- Adds IR port to standard UART
- IrDA, HPSIR, ASK (CW) & TV remote compatible
- 1200bps to 115kbps data rate
- Programmable Tx LED power
- Programmable Rx threshold level
- Power down modes
- Direct, no modulation, mode
- Tiny 5x7mm 20 pin SSOP package
- +2.7V to +5.5V supply

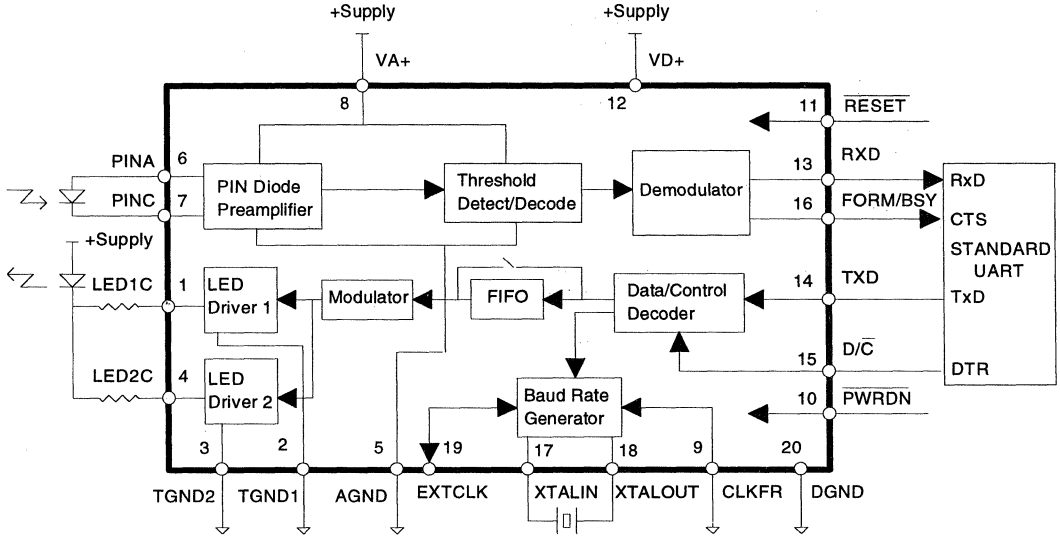
General Description

The CS8130 is an infrared transceiver integrated circuit. The receive channel includes on-chip high gain PIN diode amplifier, IrDA, HPSIR, ASK & TV remote compatible decoder, and data pulse stretcher. The transmit path includes IrDA, HPSIR, ASK & TV remote compatible encoder, and LED driver. The computer data port is standard UART TxD and RxD compatible, and operates from 1200 to 115200 baud.

External PIN diode and transmit LED are required. A control mode is provided to allow easy UART programming of different modes.

The CS8130 operates from power supplies of +2.7V to +5.5V.

For more information see the 1994 Communication Data Book



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

Semiconductor Corporation

CS6400

Echo-Cancelling Codec

Features

- Applicable in:
  - Digital-Cellular Hands-Free Phones
  - Analog-Cellular Hands-Free Phones
  - Office Speaker Phones
  - Desktop & Video Teleconferencing
  - Network/Base Stations
- Echo Cancellation
  - Up to 60 dB ERLE
  - 512 Tap (64 ms at 8 kHz Fs)
  - Split Mode For Two ECs
  - Cascadable For Longer Response
- Zero-Glue Serial Data/Control Interface
- On-Chip Codec
  - < 1% THD, 8Ω Load On Output
  - > 70 dB S/(N+D) on Input
  - 0-3600 Hz Bandwidth at 8 kHz Fs
  - 0-7200 Hz Bandwidth at 16 kHz Fs

General Description

The CS6400 is an application-specific digital signal processor optimized for acoustic echo and noise cancellation applications. A high-quality codec is integrated with the processor to provide a complete, low-cost echo-cancellation solution.

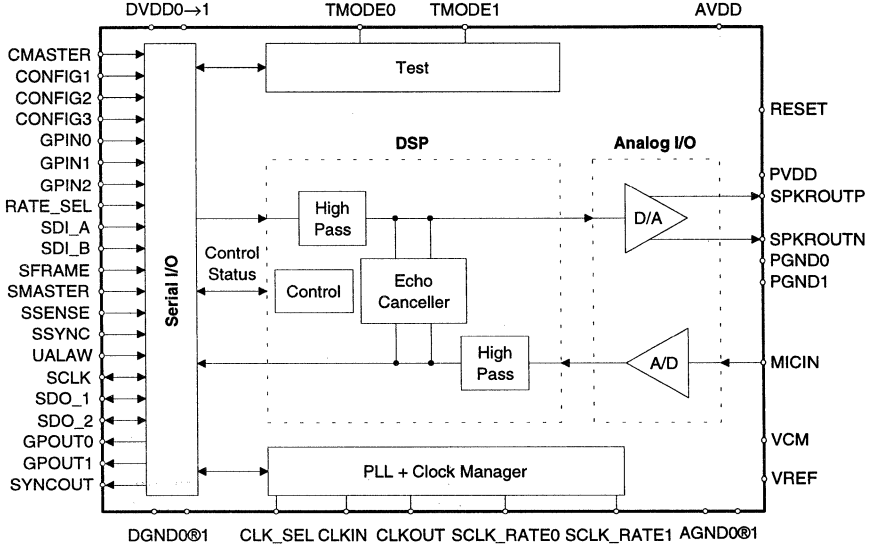
The CS6400 is a fully independent processor that requires no signal processing support to implement its cancellation functions. Volume control, mute, and sleep functions are also provided.

The on-chip A/D and D/A converters employ over-sampling technology, which eliminates the need for complex external anti-aliasing and reconstruction filters, further reducing system cost.

The CS6400 has a zero glue-logic serial interface that is compatible with most DSPs. Clock and sync lines control the transfer of serial data via the separate serial data-in and data-out pins. Both 15-bit audio data and control/status information may be multiplexed on this serial channel using a steering bit.

For more information see the 1994 Communication Data Book

4



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

Semiconductor Corporation

CS6401

Programmable Echo Canceller

Features

- For All Echo Canceller Applications
  - Digital Cellular Network Equipment
  - Analog Cellular Hands Free
  - Digital Cellular Hands Free
  - Office Speaker Phones
  - Desktop Teleconferencing
  - Long Distance Network Equipment
- Echo Cancellation
  - 8 kHz Sampling Rate
  - 512 tap (64 ms)
  - Split Mode for Two ECs (total taps = 512)

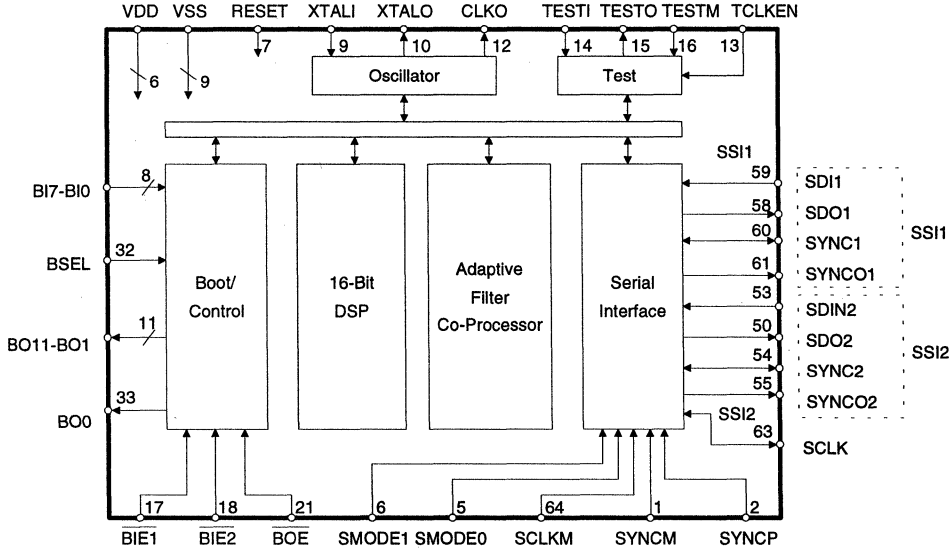
General Description

The CS6401 is a digital signal processor optimized for acoustic and/or network echo cancellation algorithms. The CS6401 implements all the adaptive filtering and control algorithms needed for high quality echo cancellation for a variety of applications. Crystal has developed the echo cancellation algorithms, and provides the DSP object code with the evaluation board. Custom algorithm development services are available from Crystal.

The CS6401 contains four main blocks:

- 16 MIPS, 16-Bit Programmable DSP
- 512-tap Adaptive FIR Filter Hardware Accelerator
- Data I-O Serial Interface
- Boot/Control Interface

For more information see the 1994 Communication Data Book



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 Fax: (512) 445-7581

CS6401 Echo-Canceller Code

FEATURES

- 30dB of ERLE
- Input high pass filters (HPF) (-3dB@300Hz) for noise reduction and offset removal
- Pre-emphasis (PE) filter for convergence speed and ERLE improvement
- Half-duplex mode on startup and for fall-back in adverse conditions
- Customizability

OVERVIEW

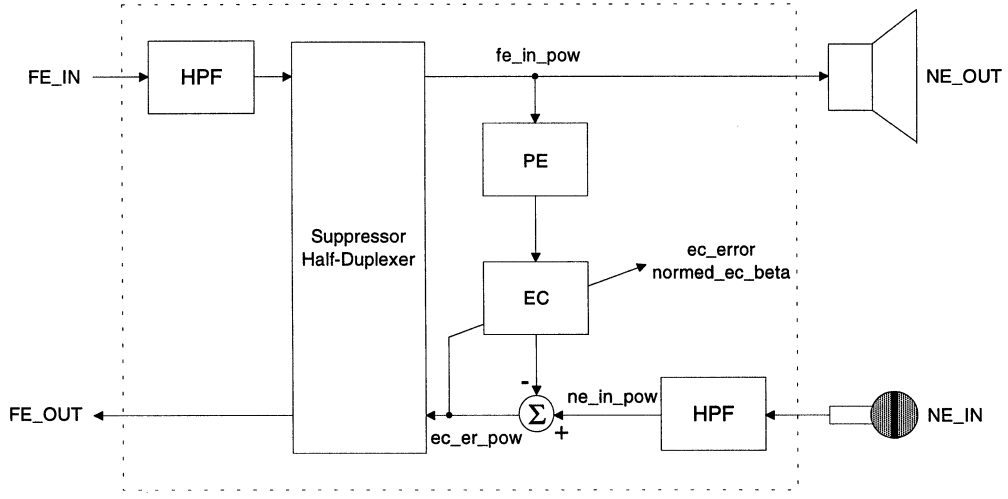
The CWECAXB version of application code for the CS6401 Programmable Echo-Canceller is optimized for acoustic echo-cancellation applications in noisy environments.

Version CWECAXB of the echo-canceller code contains advanced features:

- Support of hands-free audio at both ends of a communication link
- Support of a half-duplex fall-back mode
- Greater immunity to near-end noise

Version CWECAXB also provides the user some measure of customizability with modifiable threshold constants.

For more information see the 1994 Communication Data Book



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 Fax: (512) 445-7581

Semiconductor Corporation

CDB6401

CS6401 Evaluation Board

Features

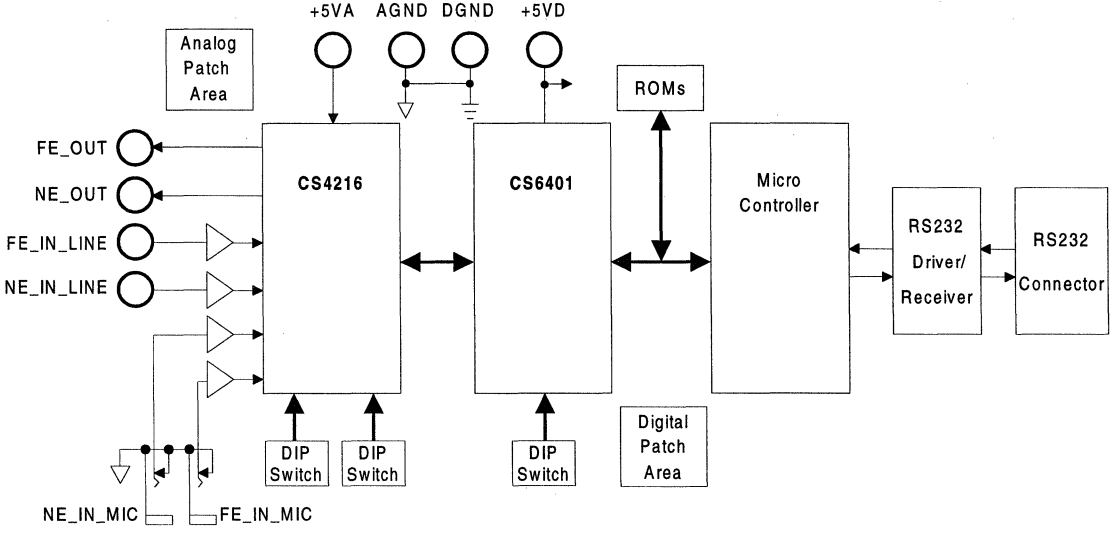
- On Board Microcontroller
- RS232 Serial Communications with Host PC
- High Quality Stereo Codec
- Microphone Pre-amplifiers
- Line Input Buffers
- Analog and Digital Patch Area

General Description

The CDB6401 allows an end-user to quickly integrate the CS6401 echo-canceller into a system and evaluate its performance. The board comes with a microcontroller and software to enable flexible setup and evaluation. Evaluation requires a +5V power supply and a Windows-capable personal computer with an available RS232 serial port. Connections for analog audio sources are provided on the board.

Also included is the CS4216 stereo audio codec which performs the data acquisition for the echo-canceller and which has such features as programmable gain and attenuation, clipping detectors, and a wide range of selectable sample rates.

For more information see the 1994 Communication Data Book



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 Fax: (512) 445-7581

CRYSTAL
Semiconductor Corporation

CS6450

TDMA/AMPS I&Q Baseband Codec

Features

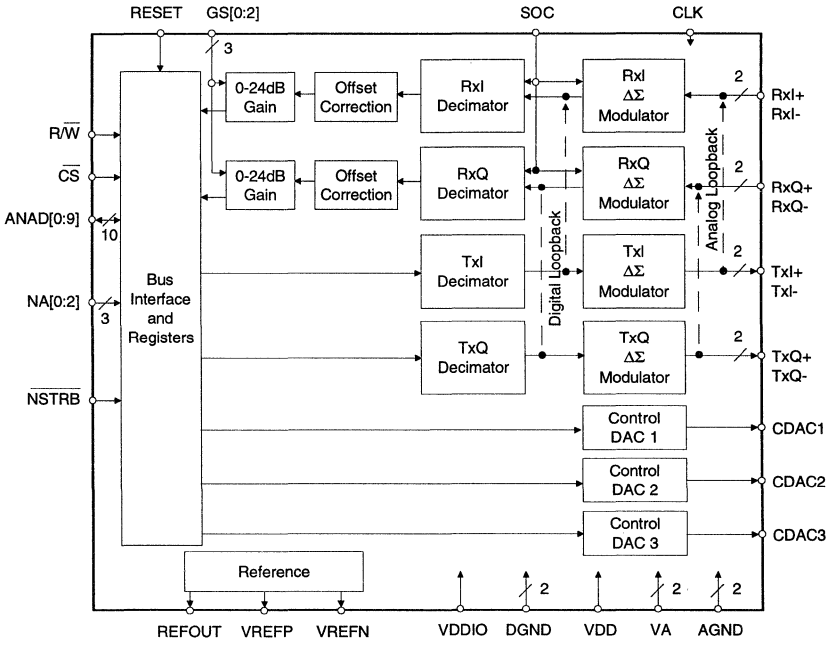
- Transmit I&Q Interface
  Two D/A converters: 10-bit, 194.4 kHz sample rate
- Receive I&Q Interface
  Two range-scaling A/D converters: 18-bit resolution, 97.2 kHz sample rate, 10-bit outputs
- Single +5V power supply; optional 3V digital I-O pins
- Three 8-bit auxiliary D/A converters for control
- Receive I & Q offset error correction

General Description

The CS6450 is a monolithic 15 kHz bandwidth I&Q baseband codec designed for use in AMPS and TDMA applications. The baseband codec provides the interfaces between a digital baseband subsystem and an analog radio subsystem. On the digital side, the codec interfaces to a digital sub-system through a parallel port. The codec includes 10-bit Delta-Sigma DAC's and ADC's for the I and Q signals. Three low speed 8-bit D/A converters can be used to control, for example, for frequency and gain of the radio sub-system. The baseband codec has efficient power management features, including the ability to power down individual transmit, receive and control channels.

For more information see the 1994 Communication Data Book

4



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 Fax: (512) 445-7581

Semiconductor Corporation

CS6453

Modem and Audio Analog Front End

Features

- Complete Voiceband DSP Front-End
  - 24-Bit A/D Converter
  - 18-Bit D/A Converter
- Minimum 84 dB Dynamic Range and 80 dB Signal-to-Distortion (at full scale)
- Supports telephone emulation
- Supports business audio
- On-chip speaker driver for modem monitoring
- Supports PCMCIA digital speaker signal
- 3.0 to 5.5V power supply range

General Description

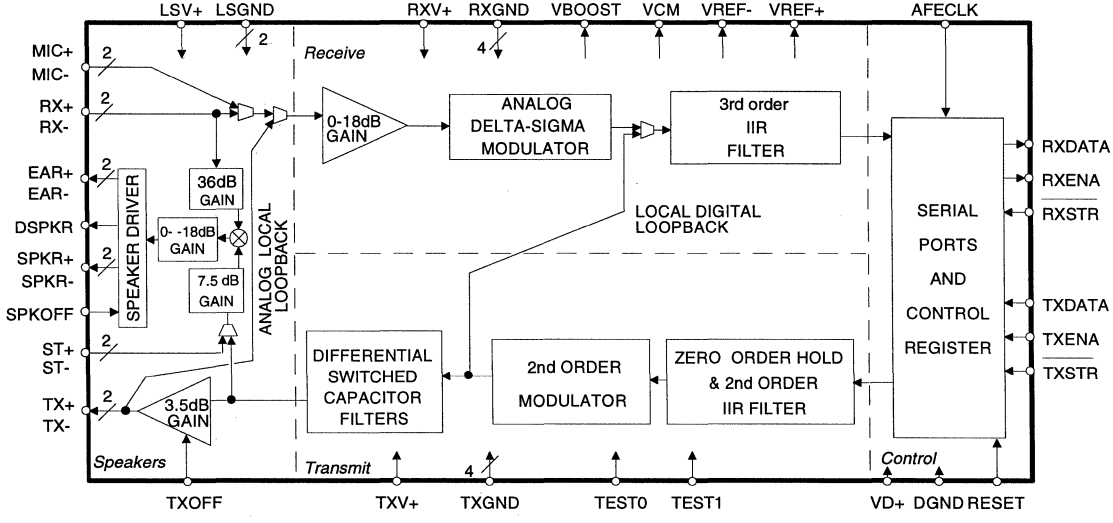
The CS6453 is a high-resolution analog-to-digital and digital-to-analog converter for V.fast, V.32bis, V.32 and other high performance modems.

The CS6453 also supports telephone emulation. In telephone emulation, the CS6453 and external DSP collectively implement both modem and telephone set capabilities. This allows an end-user to connect a handset to the "modem" card, and alternatively use the telephone connection for voice and data.

The CS6453 has 5 kHz bandwidth for modem and telephone applications, and 10 kHz bandwidth for business audio applications. The business audio capability allows the modem to playback and input audio files.

The CS6453 also supports the digital speaker signal of the PCMCIA interface standard. The modem can transfer the modem monitor signal via PCMCIA to the system speaker.

For more information see the 1994 Communication Data Book



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

Semiconductor Corporation

CS83C92A
CS83C92C

Coaxial Transceiver Interface

Features

- Implemented in High Voltage, Low Power CMOS
- Compatible with National's DP8392A
- CS83C92C is Compliant With ISO/IEEE 802.3 10Base5 (Ethernet) and 10Base2 (Cheapernet)
- All Transceiver Functions Integrated Except Signal and Power Isolation
- Squelch Circuitry Rejects Noise
- CD Heartbeat Externally Selectable Allowing Operation with IEEE 802.3 Compatible Repeaters
- Receive & Transmit Mode Collision Detection
- Standard 16-pin DIP Package & 28 pin PLCC

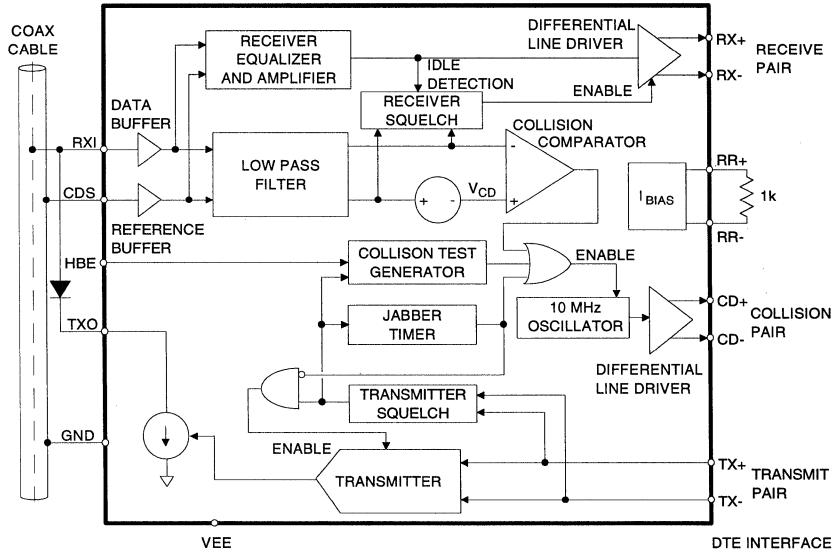
General Description

The CS83C92 Ethernet Transceiver interfaces an Ethernet or Cheapernet Local Area Network (LAN) to a LAN Adapter board, and may be located up to 50 meters from the station equipment. The Transceiver operates with the Crystal LAN components CS8005 Ethernet Data Link Controller and the CS8023A Manchester Code Converter. The CS83C92A is fully compatible with the DP8392A but the CS83C92A is built in CMOS technology (hence the 83"C"92). The CS83C92C is a higher performance grade which is compliant with IEEE 802.3 specifications.

For Ethernet applications, the CS83C92 is mounted on the COAX cable, and connects to the station equipment via an AUI cable. In a Cheapernet network, the CS83C92 is usually mounted on the LAN adapter card in the station equipment where it connects to the thin COAX through a BNC connector.

For more information see the 1994 Communication Data Book

4



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 Fax: (512) 445-7581

Semiconductor Corporation

CS8900

Highly-Integrated ISA Ethernet Controller

Features

- Single-Chip IEEE 802.3 Ethernet Controller with Direct ISA-Bus Interface
- Efficient PacketPage™ Architecture Operates in I/O and Memory Space, and as DMA Slave
- Full Duplex Operation
- On-Chip RAM Buffers Transmit & Receive Frames
- 10BASE-T Port with Analog Filters, Provides:
  - Automatic Polarity Detection and Correction
- AUI Port for 10BASE2, 10BASE5 and 10BASE-F
- Programmable Transmit Features:
  - Automatic Re-transmition on Collision
  - Automatic Padding and CRC Generation
- Programmable Receive Features:
  - StreamTransfer™ for Reduced CPU Overhead
  - Auto-Switch Between DMA and On-Chip Memory
  - Early Interrupts for Frame Pre-Processing
  - Automatic Rejection of Erroneous Packets
- EEPROM Support for Jumperless Configuration
- Boot PROM Support for Diskless Systems
- Boundary Scan and Loopback Test
- LED Drivers for Link Status and LAN Activity
- Standby and Suspend Sleep Modes

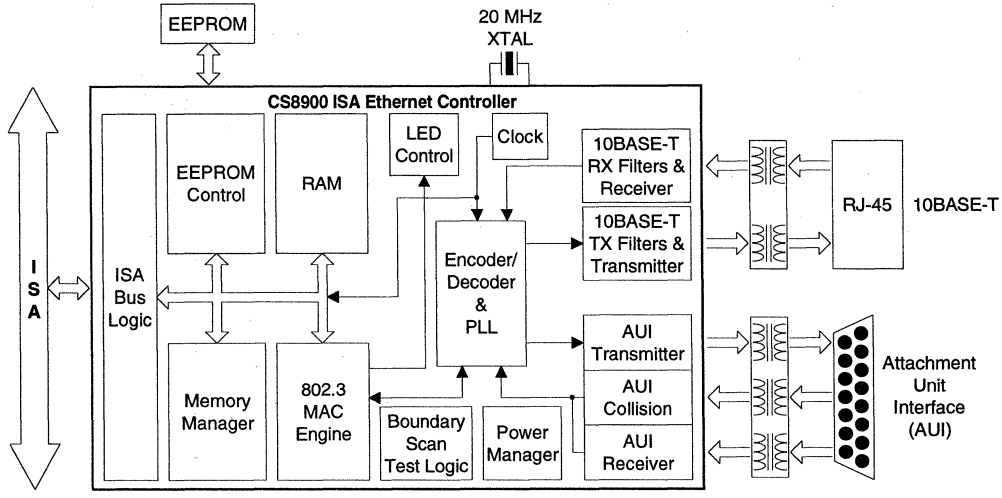
Description

The CS8900 is a low-cost Ethernet LAN Controller optimized for Industry Standard Architecture (ISA) Personal Computers. Its highly-integrated design eliminates the need for costly external components required by other Ethernet controllers. The CS8900 includes on-chip RAM, 10BASE-T transmit and receive filters, and a direct ISA-Bus interface with 24 mA Drivers.

In addition to high integration, the CS8900 offers a broad range of performance features and configuration options. Its unique PacketPage architecture automatically adapts to changing network traffic patterns and available system resources. The result is increased system efficiency and minimized CPU overhead.

The CS8900 is available in a thin 100-pin TQFP package ideally suited for small form-factor, cost-sensitive Ethernet applications, such as desktop and portable motherboards and adapters. With the CS8900, system engineers can design a complete Ethernet circuit that occupies less than 1.5 square inches (10 sq cm) of board space.

For more information see the 1994 Communication Data Book



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 Fax: (512) 445-7581

T1 Transceivers

Features

- Monolithic T1 Framing Device
- Both Transceivers support SF(D4®) and ESF framing formats
- CS2180B also supports SLC-96® and T1DM framing formats
- CS2180B has updated AIS and Carrier Loss detection criteria
- CS2180B is Pin Compatible with CS2180A, DS2180A and DS2180

General Description

The CS2180A and CS2180B are monolithic CMOS devices which encode and decode T1 framing formats. The devices support bit-seven and B8ZS zero suppression, and bit-robbed signaling. Clear channel mode can be selected on a per channel basis.

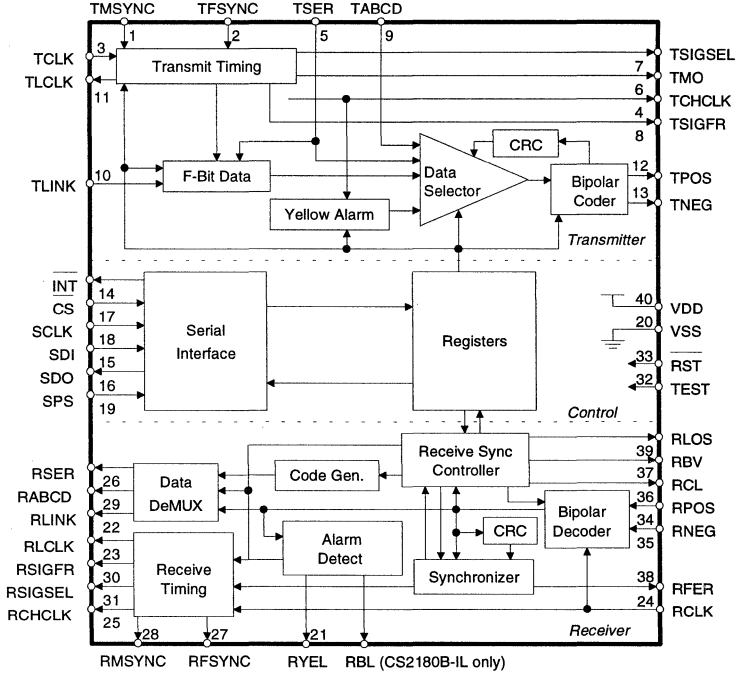
The serial interface has been enhanced to allow the CS2180A and CS2180B to share a chip select signal and register address space with the CS61535A, CS61574A and CS61575 PCM Line Interface ICs.

Applications

- T1 Line Cards
- ISDN Primary Rate Line Cards

For more information see the 1994 Communication Data Book

4



Semiconductor Corporation

CS61304A

T1/E1 Line Interface

Features

- Provides Analog Transmission Line Interface for T1 and E1 Applications
- Provides Line Driver, Jitter Attenuator and Clock Recovery Functions
- Fully Compliant with AT&T 62411 Stratum 4, Type II Jitter Requirements
- Low Power Consumption
- B8ZS/HDB3/AMI Encoder/Decoder
- 50 mA Transmitter Short-Circuit Current Limiting

General Description

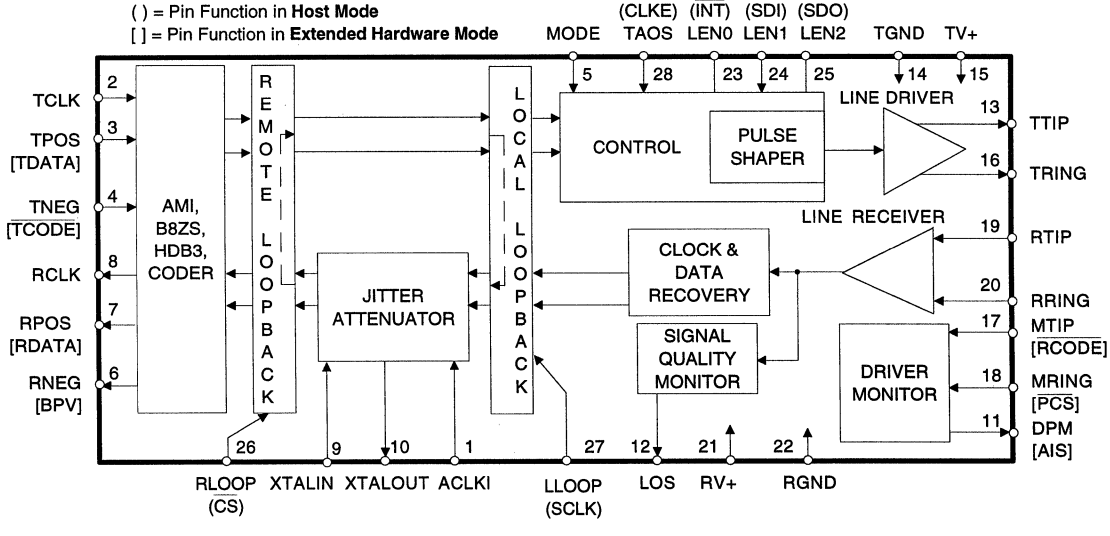
The CS61304A combines the complete analog transmit and receive line interface for T1 or E1 applications in a low power, 28-pin device operating from a +5V supply. The CS61304A is a pin-compatible replacement for the LXT304A.

The receiver uses a digital Delay-Locked-Loop which is continuously calibrated from a crystal reference to provide excellent stability and jitter tolerance. The CS61304A has a receiver jitter attenuator optimized for T1 CPE applications subject to AT&T 62411 and E1 ISDN PRI applications. The transmitter features internal pulse shaping and a low impedance output stage allowing the use of external resistors for transmitter impedance matching.

Applications

- Primary Rate ISDN Network/Termination Equipment
- Channel Service Units

For more information see the 1994 Communication Data Book



Crystal Semiconductor Corporation
P. O. Box 17847, Austin, Texas, 78760
(512) 445-7222 FAX:(512) 445-7581

Semiconductor Corporation

CS61305A

T1/E1 Line Interface

Features

- Provides Analog Transmission Line Interface for T1 and E1 Applications
- Provides Line Driver, Jitter Attenuator and Clock Recovery Functions
- Transmit Side Jitter Attenuation Starting at 6 Hz, with > 300 UI of Jitter Tolerance
- B8ZS/HDB3/AMI Encoders/Decoders
- Compatible with SONET, M13 , CCITT G.742, and Other Asynchronous Muxes
- 50 mA Transmitter Short-Circuit Current Limiting

General Description

The CS61305A combines the complete analog transmit and receive line interface for T1 or E1 applications in a low power, 28-pin device operating from a +5V supply. The CS61305A is a pin-compatible replacement for the LXT305A in most applications.

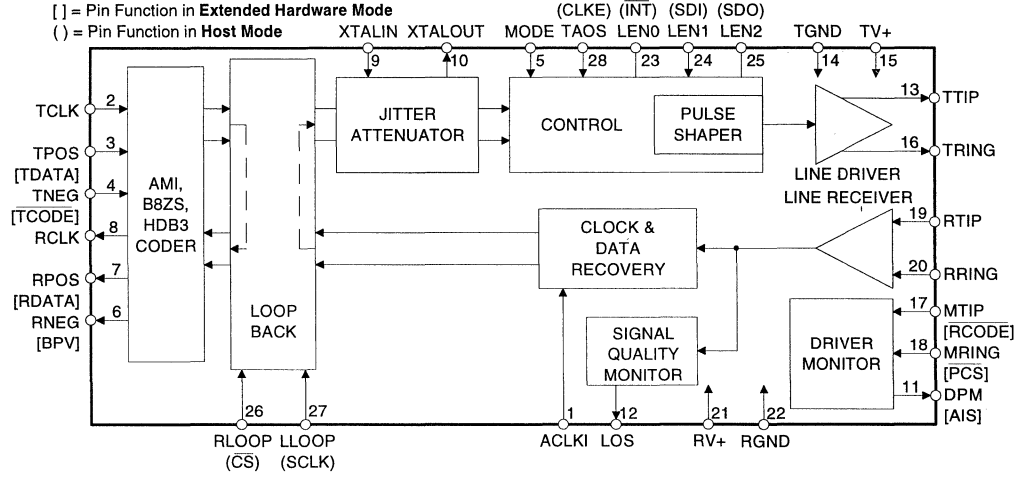
The CS61305A provides a transmitter jitter attenuator making it ideal for use in asynchronous multiplexor systems with gapped transmit clocks. The transmitter features internal pulse shaping and a low impedance output stage allowing the use of external resistors for transmitter impedance matching. The receiver uses a digital Delay-Locked-Loop clock and data recovery circuit which is continuously calibrated from a crystal reference to provide excellent stability and jitter tolerance.

Applications

- Interfacing network transmission equipment such as SONET multiplexor and M13 to a DSX-1 cross connect.
- Interfacing customer premises equipment to a CSU.

For more information see the 1994 Communication Data Book

4



Semiconductor Corporation

CS61535A
CS61535

T1/E1 Line Interface

Features

- Provides Analog PCM Line Interface for T1 and E1 Applications
- Provides Line Driver, and Data and Clock Recovery Functions
- Transmit Side Jitter Attenuation Starting at 6 Hz, with > 300 UI of Jitter Tolerance
- Low Power Consumption (typically 175 mW)
- B8ZS/HDB3/AMI Encoders/Decoders
- 14 dB of Transmitter Return Loss
- Compatible with SONET, M13 , CCITT G.742, and Other Asynchronous Muxes

General Description

The CS61535A and CS61535 combine the complete analog transmit and receive line interface for T1 or E1 applications in a low power, 28-pin device operating from a +5V supply. The CS61535A provides additional features and higher performance than the CS61535.

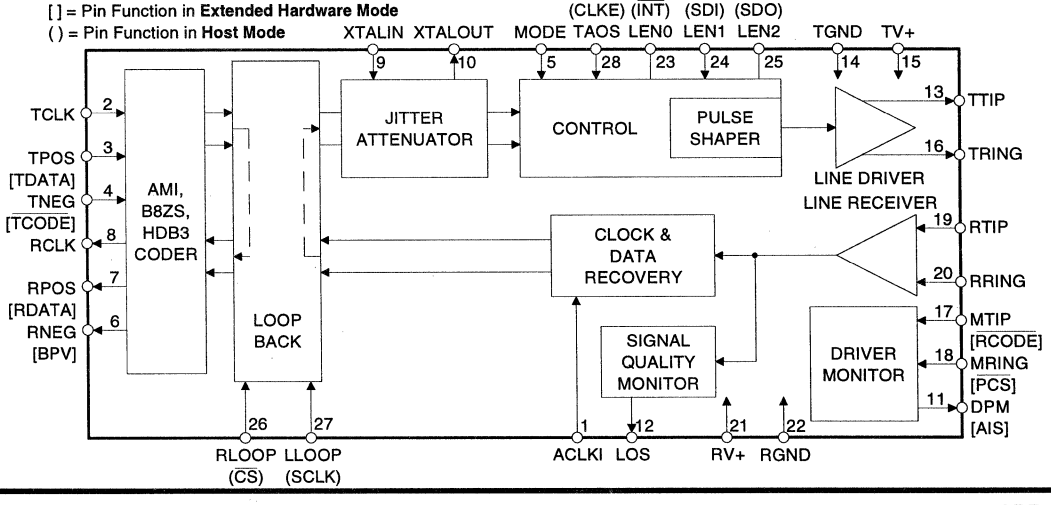
Both devices feature a transmitter jitter attenuator making them ideal for use in asynchronous multiplexor systems with gapped transmit clocks. The CS61535A provides a matched, constant impedance output stage to insure signal quality on mismatched, poorly terminated lines.

Both ICs use a digital Delay-Locked-Loop clock and data recovery circuit which is continuously calibrated from a crystal reference to provide excellent stability and jitter tolerance.

Applications

- Interfacing network transmission equipment such as SONET multiplexor and M13 to a DSX-1 cross connect.
- Interfacing customer premises equipment to a CSU.
- Interfacing to E1 links.

For more information see the 1994 Communication Data Book



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

Semiconductor Corporation

CS61574A CS61575

T1/E1 Line Interface

Features

- Provides Analog Transmission Line Interface for T1 and E1 Applications
- Provides Line Driver, Jitter Attenuator and Clock Recovery Functions
- Fully Compliant with AT&T 62411 Stratum 4 Jitter Requirements
- Low Power Consumption (typically 175 mW)
- B8ZS/HDB3/AMI Encoder/Decoder
- 14 dB of Transmitter Return Loss

General Description

The CS61574A and CS61575 combine the complete analog transmit and receive line interface for T1 or E1 applications in a low power, 28-pin device operating from a +5V supply. Both devices support processor-based or stand-alone operation and interface with industry standard T1 and E1 framers.

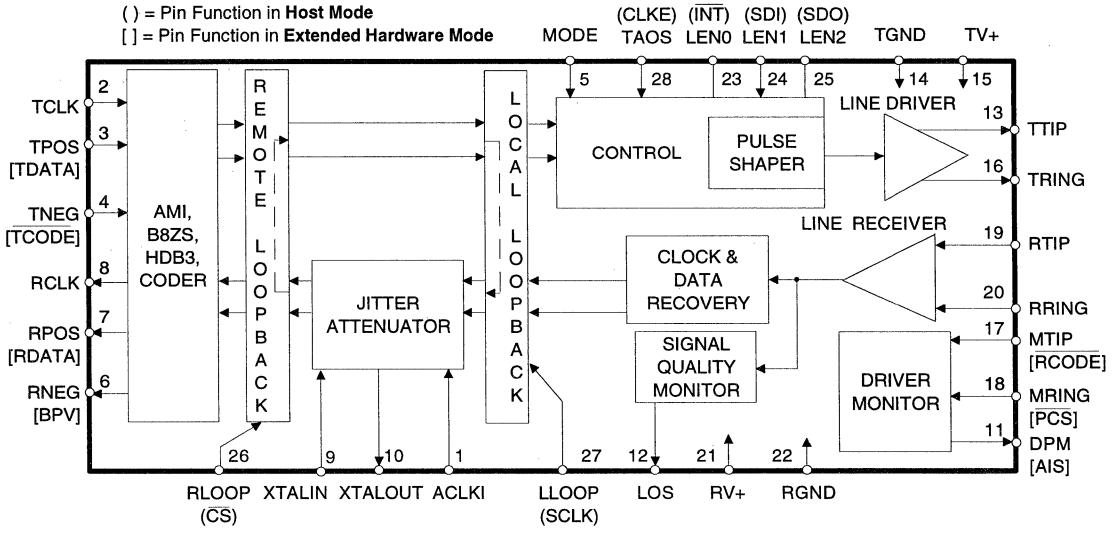
The receiver uses a digital Delay-Locked-Loop which is continuously calibrated from a crystal reference to provide excellent stability and jitter tolerance. The CS61574A has a receiver jitter attenuator optimized for minimum delay in switching and transmission applications, while the CS61575 attenuator is optimized for CPE applications subject to AT&T 62411 requirements. The transmitter features internal pulse shaping and a matched, constant impedance output stage to insure signal quality on mismatched, poorly terminated lines.

Applications

- Interfacing Network Equipment such as DACS and Channel Banks to a DSX-1 Cross Connect
- Interfacing Customer Premises Equipment to a CSU
- Building Channel Service Units

For more information see the 1994 Communication Data Book

4



CRYSTAL
Semiconductor Corporation

CS61577

T1/E1 Line Interface

Features

- Provides Analog Transmission Line Interface for T1 and E1 Applications
- Drop-in Replacement for CS61574 with the Following Enhancements:
  - Lower Power Consumption
  - Transmitter Short-Circuit Current Limiting
  - Greater Transmitter Immunity to Line Reflections
  - Software Selection Between 75Ω and 120Ω E1 Output Options
  - Internally Controlled E1 Pulse Width
  - B8ZS/HDB3/AMI Encoder/Decoder

General Description

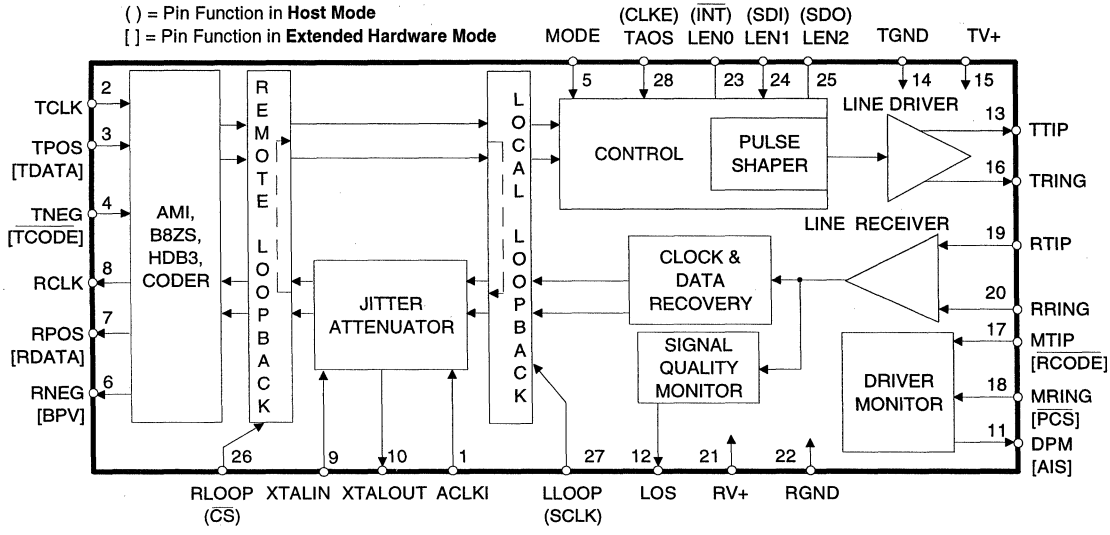
The CS61577 is a drop-in replacement for the CS61574, and combines the complete analog transmit and receive line interface for T1 or E1 applications in a low power, 28-pin device operating from a +5V supply. The CS61577 supports processor-based or stand-alone operation and interfaces with industry standard T1 and E1 framers.

The receiver uses a digital Delay-Locked-Loop which is continuously calibrated from a crystal reference to provide excellent stability and jitter tolerance. The receiver includes a jitter attenuator optimized for minimum delay in switching and transmission applications. The transmitter provides internal pulse shaping to insure compliance with T1 and E1 pulse template specifications.

Applications

- Interfacing Network Equipment such as DACS and Channel Banks to a DSX-1 Cross Connect
- Building Channel Service Units

For more information see the 1994 Communication Data Book



Crystal Semiconductor Corporation
P. O. Box 17847, Austin, Texas, 78760
(512) 445-7222 FAX:(512) 445-7581

Semiconductor Corporation

CS61584

Dual Low Power T1/E1 Line Interface

Features

- Provides Dual Analog PCM Line Interface for short-haul, T1 and E1 applications
- 3.3 Volt and 5 Volt Versions
- Low Power Consumption (typically 160 mW per Line Interface)
- Operating mode fully software configurable; same external components can be used for all modes. No external quartz crystal is required.
- User-customizable pulse shapes
- Support of JTAG boundary scan

General Description

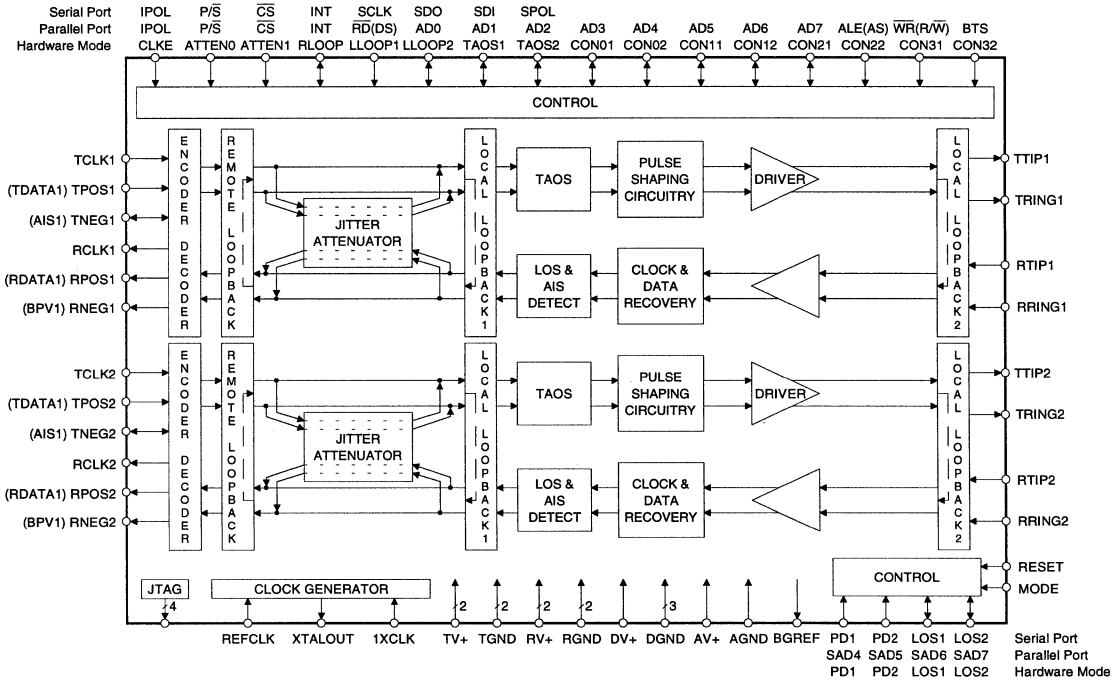
The CS61584 is a universal line interface for T1/E1 applications, designed for high-volume cards where low power, high density and universal operation is required. One board design can support all T1/E1 modes. Only the frequency of the reference clock input must change as software selects between T1 and E1.

The CS61584 is a low-power CMOS device available in 3.3 Volt and 5 Volt versions.

Transmitted pulse shapes are software-customizable, allowing non-standard line loads or protection circuits to be supported. Control is via either a serial port, parallel port or individual control lines.

For more information see the 1994 Communication Data Book

4



Crystal Semiconductor Corporation
P. O. Box 17847, Austin, Texas, 78760
(512) 445-7222 FAX:(512) 445-7581

Semiconductor Corporation

CXT6176
CXT8192

Pullable Quartz Crystals

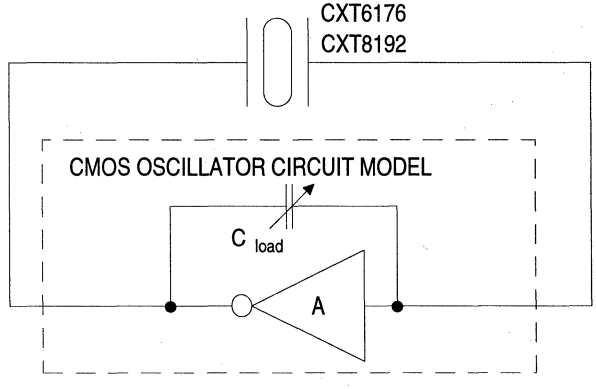
Features

- Complements CS61534, CS61535, CS61535A, CS61544, CS61574, CS61574A, and CS61575 PCM Line Interface integrated circuits and CS61600 PCM Jitter Attenuator.

Description

Crystal Semiconductor's line interface and jitter attenuator IC's require unique performance specifications for the crystals. The CXT6176 and CXT8192 are built to meet Crystal's specifications for T1 and PCM-30 applications respectively.

For more information see the 1994 Communication Data Book



Crystal Line Interface or Jitter Attenuator I.C.

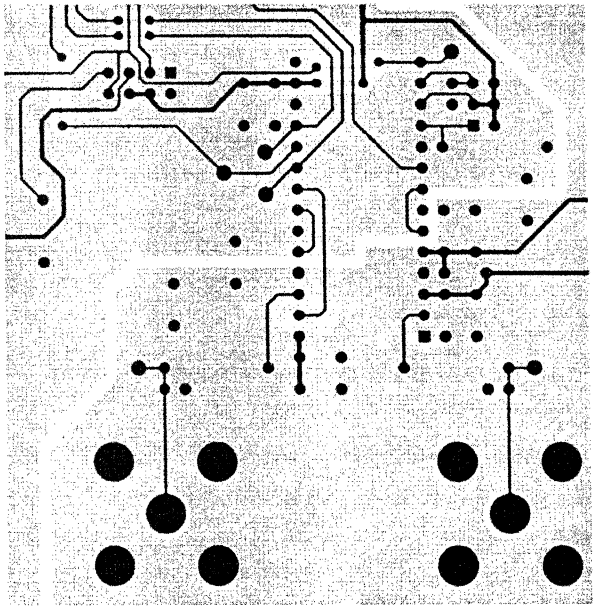
Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

CONTENTS

Application Note

Layout and Design Rules for Data Converters and Other Mixed Signal Devices

by
Ron Knapp & Steven Harris



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445 7581

Here is a list of guidelines for optimum printed circuit board layout for Crystal ADC's, DAC's, and codecs. Use these pages as a checklist during and after layout by checking the boxes when each line item is OK. Remember, Crystal offers a free schematic and layout review service. Try hard to use this service before building your first prototype board. Comments or additional items are very welcome.

☐ 1) Partition the board with all analog components grouped together in one area and all digital components in the other. Common power supply related components should be centrally located.

☐ 2) Have separate analog and digital ground planes on the same layer, with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes should be >1/8".

☐ 3) Mixed signal components, including the data converters, should bridge the partition in the ground plane with only analog pins in the analog area, and only digital pins in the digital area. Rotating the data converter can often make this task easier. Look at the evaluation board data sheet to see where the split should be located.

For our serial codecs, the device should be placed over the analog ground plane, positioned next to the ground plane split. The digital pins should be next to the split, with the digital traces crossing directly over into the digital region of the board. The analog ground pins and digital ground pins should be connected with zero impedence (same ground plane). See the CS4215 and CS4216, CDB4215 and CDB4216 data sheets for examples.

☐ 4) Analog and digital ground planes should only be connected at one point (in most cases). Have vias available in the board to allow alternative connection points.

☐ 5) Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane. These regions should not be left floating, which only make the interference worse. Using ground plane fill has been shown to reduce digital to analog coupling by up to 30 dB.

☐ 6) The analog to digital ground plane connection should be near to the power supply, or near to the power supply connections to the board, or near to the data converter. In the case of multiple converters, leave jumper options at each converter.

☐ 7) Analog power and analog signal traces should be over the analog ground plane.

☐ 8) Digital power and digital signal traces should be over the digital ground plane.

☐ 9) Keep digital signal traces, especially the clock, as far away from analog input and voltage reference pins as possible.

☐ 10) Bypassing and decoupling capacitors should be close to the IC pins, or positioned for the shortest connection to pins with wide traces to reduce impedance (for example, between pins 1 and 28 at the top end of the IC package in the case of the VREF decoupling capacitors for the CS5326 family, the CS5336 family and the CS4328).

☐ 11) If both large electrolytic and small ceramic capacitors are recommended, make the small ceramic capacitor closest to the IC pins. For multi-layer pc boards, make the connections to the converter and to the capacitors on the same layer (this avoids the additional impedence of vias).

☐ 12) All filtering capacitors in the signal path should be NP0/C0G dielectric. BX/X7R dielectric is OK for DC voltages where voltage coefficient is not a factor.

☐ 13) All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors are OK for DC voltages and the power supply path where voltage coefficient, temperature coefficient or noise are not a factor. Avoid wire wound resistors and potentiometers.

☐ 14) Avoid multiple crystal oscillators or asynchronous clocks. Best results are obtained when all circuits are synchronous to the A/D or D/A sampling clock.

☐ 15) When using converters with DSP IC's, operate everything from one crystal using dividers if necessary.

☐ 16) In systems requiring multiple crystals for selectable sampling frequencies, enable only one at a time. Shut off all other oscillators by removing power. Make sure other oscillators are off either with an active crowbar on Vcc or very high impedance switch. Often the leakage from a transistor or FET which is not completely off is sufficient for the oscillator to produce a low level output frequency.

☐ 17) When using DC-DC switching regulators, synchronize the switching frequency to the A/D if possible. This applies to CMOS chopper amplifiers as well.

☐ 18) Avoid connecting the clock source oscillator to the converter sampling clock input through analog multiplexers, PAL's, gate arrays, opto-couplers or circuits which can cause jitter.

☐ 19) Locate the crystal or oscillator close to the converter. Avoid overshoot and undershoot on the master clock for the converter. This is particularly important for the CS5326 family, where the master clock (CLKIN) goes directly into the analog modulator die.

☐ 20) Use buffers for digital signals directly to or from the converter to connectors which go off the board.

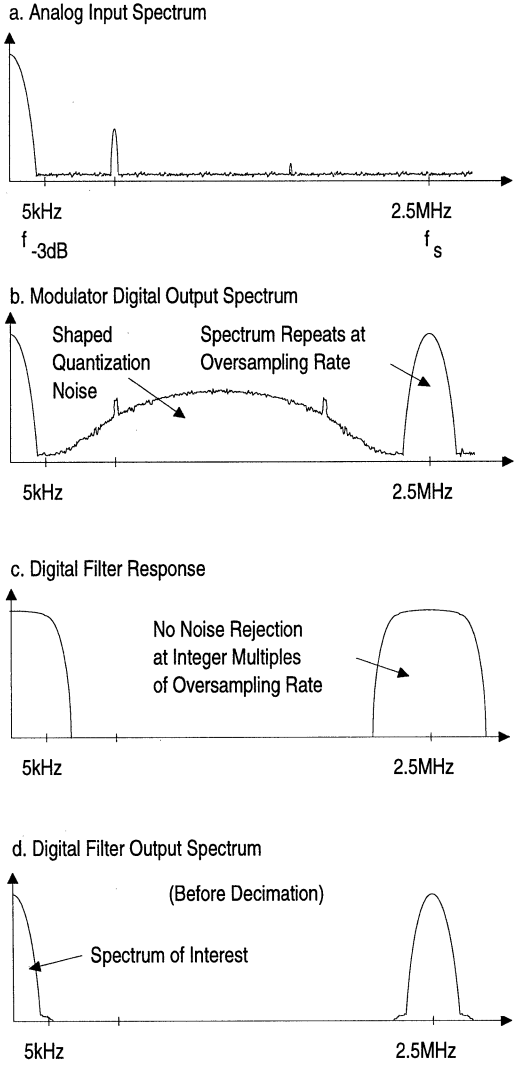
☐ 21) In the case of piggy-back boards, or boards which plug into a slot adjacent to other boards, consider the circuits which will be above or below the converter as sources of interference. A mu-metal screen may be required.

☐ 22) For delta sigma converters, make sure that potential interfering clocks are not in sensitive frequency regions. Sensitive regions are defined as ± passband either side of multiples of the input sample rate. Two examples are : a) for a CS5336 operating at 48 kHz word rate, the frequencies to avoid are (N X 3.072MHz) ±24 kHz. b) for a CS5501 with a 4 MHz crystal, the frequencies to avoid are (N X 16 kHz) ± 10 Hz. Frequencies which are synchronous to the input sample rate will not cause problems, since they will be converted to dc, and calibrated out.

- ☐ 23) For boards with more than 2 layers, do not overlap analog related and digital related planes. Do not have a plane which crosses the split between the analog ground plane region and the digital ground plane region.
- ☐ 24) For CS5326, CS5336 & CS5349 families, supply VD+ to the device via a separate trace connected to where the +5V digital supply enters the board. Connect no other logic to this trace. Alternatively, provide a 10 µH inductor in series with VD+, near to the ADC.
- ☐ 25) For boards with both A/D converters and D/A converters, provide a means for testing each function separately. Possible methods include providing a header to allow access to the digital data paths, and allowing for easy attachment of a CS8402 and CS8412 AES/EBU transmitter and receiver parts.
- ☐ 26) Terminate unused op-amps in dual and quad packs by grounding the + input and connecting the - input to the output.
- ☐ 27) Digital control lines which must cross into the analog region should be as short as possible and should be mostly static. For example, digital gain and analog mux control lines.
- ☐ 28) The pins of DIP or SOIC packages should not have ground plane in between adjacent pins.
- ☐ 29) In systems using a delta-sigma converter, then avoid the use of clocks (particularly the serial bit clock) at half the frequency of the input sample rate. If this frequency interferes with the voltage reference, then tones can occur.
- ☐ 30) Do not surround the analog region with digital components. Do not surround the digital region with the analog region

Application Note

Delta Sigma A/D Conversion Technique Overview



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 TWX: 910-874-1352

SECTION A

OVERVIEW: DELTA-SIGMA MODULATION

Although developed over two decades ago, delta-sigma modulation has only recently achieved commercial implementation. The technique utilizes oversampling and digital filtering to achieve high performance in both A/D conversion and filtering at low cost. The advent of commercial delta-sigma converters is due in most part to recent advances in mixed analog-digital VLSI technology. Precision analog circuitry can now be integrated on the same chip with powerful digital filters.

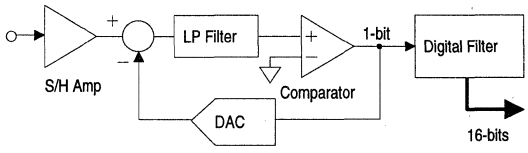


Figure A1. Delta-Sigma ADC

In a delta-sigma ADC, the same digital filter used in the A/D conversion process can perform system-level filtering with performance unachievable in analog form. Therefore, the first commercial delta-sigma converters have been targeted at applications demanding high-performance filtering (high-end modems, digital audio, geophysical exploration, etc).

This application note uses the CS5317 voice band A/D converter for examples. See the end of this application note for implementation details for the CS5317, CS5501, CS5326 A/D converters.

Fundamentals

A delta-sigma ADC consists of two basic blocks: an analog modulator and a digital filter (see Figure A1). The fundamental principle behind the modulator is that of a single-bit A/D converter embedded in an analog negative feedback loop with high open loop gain. The modulator loop oversamples and processes the analog input at a rate much higher than the bandwidth of interest. The modulator's output provides small packages of information (that is, 1-bit) at a very high rate and in a format that the digital filter can process to extract higher resolution (such as 16-bits) at a lower rate.

The delta-sigma converter's basic operation can be analyzed in either the time domain, or (more conventionally) in the frequency domain.

Time-Domain Analysis

The basic operation of a delta-sigma modulator can be understood more intuitively by demonstration. A simple, first-order modulator (that is, a conventional voltage-to-frequency converter) is shown in Figure A2. (Note: a modulator's order indicates the number of orders of analog filtering - or integration - in the loop). Full-scale inputs are ± 1V and three nodes are labeled V_1, V_2, and V_3. The output of the comparator, node V_3, is the output of the loop and is also converted by the 1-bit DAC into plus or minus full-scale (+1V or -1V).

At the differential amplifier, the +1V or -1V is subtracted from the analog input voltage. The result, the voltage at node V_1, is input to the integrator. The integrator acts as an analog accumulator; ie. the input voltage at node V_1 is added to the voltage on node V_2 which becomes the new voltage on node V_2. Node V_2 is then com-

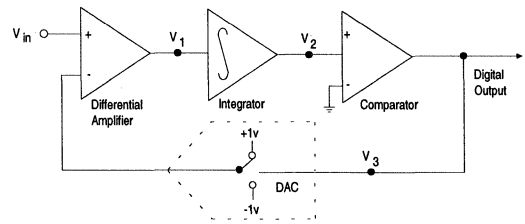


Figure A2. 1st-order Delta-Sigma Modulator

pared to ground. If it is greater than ground, node V_3 becomes +1V; if it is less than ground, V_3 becomes -1V. Each operation occurs once during each clock cycle.

In the example shown in Table A1, all nodes are initially set to zero, and the analog input voltage is assumed to be 0.6V. Since all nodes are identical in clock cycles two and seven, the period defined by cycles two to six will repeat if the analog input remains unchanged. The average value of modulator outputs (at node V_3) during that period, 0.6, yields a numerical representation of the analog input.

Clock Period	V_1	V_2	V_3	Period Avg
0	0	0	0	
1	0.6	0.6	1	
2	-0.4	0.2	1	
3	-0.4	-0.2	-1	
4	1.6	1.4	1	0.6
5	-0.4	1.0	1	
6	-0.4	0.6	1	
7	-0.4	0.2	1	
8	-0.4	-0.2	-1	

Table A1. Modulator Walk-Through

With conventional voltage-to-frequency converters a digital counter is used to extract the information in the VFC's 1-bit output. Pulses are counted over a specified period, effectively creating a digital averaging (or integrating) filter. The final count represents the average analog input value during the integrating period.

Advanced delta-sigma converters use higher-order modulators and more powerful digital filters. For example, the CS5317 uses a second-order modulator. The pattern of transitions in its 1-bit output provides more useful information regarding higher resolution at higher frequencies.

However, a more sophisticated digital filter than a counter is needed to interpret that information. A digital FIR filter is basically a rolling, weighted average of consecutive samples (see Appendix B). An averaging filter weights all samples equally. By applying a more sophisticated weighting function to the 1-bit signal, a digital FIR filter can assemble an N-bit output (with 2^N possible values) *without having to wait for 2^N samples.*

The Charge-Balance Name

Delta-sigma ADC's are also known by other names - sigma delta and charge-balance are two examples. The *Charge-Balance* name derives from the fact that the modulator tries to *balance* the analog input with the DAC's output in the negative feedback loop. The charge injected onto the integrator's capacitor from sampling the analog input (see Figure A2) is therefore balanced by the charge injected by the DAC's output. Modulators have been implemented in both switched-capacitor and continuous-time form.

Frequency-Domain Analysis

Since filtering plays a key role in a delta-sigma ADC, it is easier to understand the converter's operation by analyzing it in the frequency domain.

Overview

An A/D converter's resolution determines its dynamic range (or signal-to-noise ratio). Conversely, one can improve a converter's signal-to-noise ratio and thereby increase its effective resolution. The fundamental concept behind delta-sigma converters is to perform a simple, low-resolution A/D conversion and reduce the resulting "quantization noise" (without affecting the frequency band of interest) using analog and digital filtering.

Quantization Noise

The comparator in the delta-sigma modulator loop plays the role of a 1-bit A/D converter. Any A/D converter can represent a continuous analog input by one of only a *finite* number of codes, giving rise to an uncertainty, or quantization error, of up to ± 1/2 LSB. For a consecutive sequence of samples in a waveform, these quantization effects can be modeled as a random noise source under conditions commonly encountered in signal processing applications. (These conditions hold true for delta-sigma modulators). The rms value of the noise source relative to a full-scale input can be shown to equal - (6.02 N + 1.76) dB, for an N-bit resolution converter. Since this error "signal" is totally random (or uncorrelated with the input) it can be assumed to be white, with its energy spread uniformly over the band from dc to one-half the sampling rate.

As a 1-bit ADC, the comparator in a delta-sigma modulator offers (an almost comical) 7.78 dB signal-to-noise ratio. However, the input signal is grossly oversampled (2.5 MHz in the CS5317), thus spreading the quantization noise over a wide bandwidth (1.25 MHz). The noise density in the bandwidth of interest (5 kHz) is therefore reduced.

Noise Shaping

Analog filtering is used in the modulator loop to further reduce noise density in the frequency band of interest by shaping the quantization noise spectrum. The spectrum of the input signal, meanwhile, remains unaltered. Figure A3 shows a modulator loop with analog and digital circuit differences ignored. The comparator is simply shown as a (quantization) noise source, and the analog filtering, which is simply an integrator, assumes the filter response H(f). If the analog input equals zero, then

$$D_{out} = Q(n) - H(f)\, D_{out}$$

$$D_{out} = \frac{Q(n)}{1 + H(f)}$$

The quantization noise at the output is reduced by the open-loop gain of the integrator. At low frequency, the integrator is designed for high open-loop gain, so that quantization noise is reduced. As shown in Figure A4b, the integrator effectively pushes the quantization noise out of the bandwidth of interest and into higher frequencies. Digital lowpass filtering then removes the quantization noise at the higher frequencies without affecting the low-frequency spectrum of interest.

The spectral characteristics of the analog loop filtering dictates the delta-sigma converter's resolution/bandwidth ratio. Higher-order integrators improve noise shaping and allow for higher resolutions at wider bandwidths. The CS5317 uses a second-order modulator for superior noise shaping.

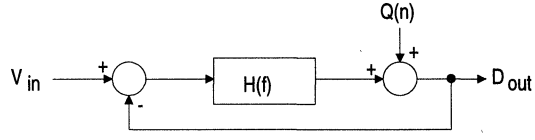


Figure A3. Analog Modulator Model

Digital Filtering

The spectral characteristics of the back-end digital filtering also affects the delta-sigma converter's resolution/bandwidth ratio. Faster roll-off and greater stopband rejection reduces residual quantization noise. Section B offers a detailed explanation of the theory behind digital filtering.

Anti-Alias Requirements

As shown in Figure A4, the input and digital filtering spectrum of any ADC repeats around integer multiples of its sampling rate. A delta-

sigma ADC thus does not provide noise rejection in the region around integer multiples of the sampling rate (± 5 kHz around 2.5 MHz, 5 MHz, 7.5 MHz...). If noise exists in the system in these narrow bands, analog filtering is needed to remove it at the converter's input otherwise it will alias and pass unfiltered to the converter's output.

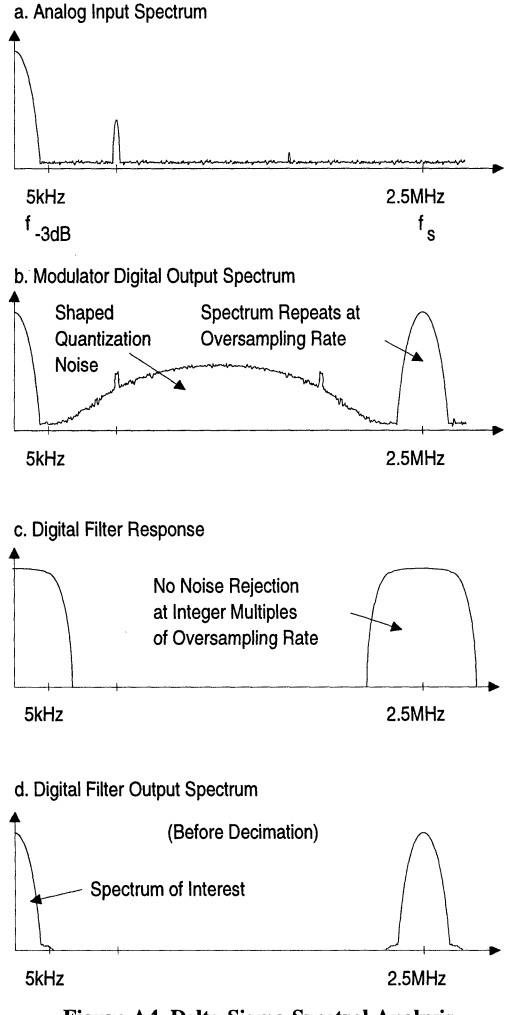


Figure A4. Delta-Sigma Spectral Analysis (Using frequencies taken from the CS5317 A/D Converter)

Since delta-sigma ADC's are grossly oversampled, anti-alias filtering requirements are often trivial. For instance, the CS5317 provides a factor of 500 of oversampling (2.5 MHz/5 kHz). A single-pole, passive RC filter at the CS5317's input is therefore sufficient in most applications.

Decimation

Even though the delta-sigma ADC oversamples and processes analog samples at a frequency well above the bandwidth of interest, it will generally offer its high-resolution output at a much-lower system sampling rate. Any reduction in sampling rate is termed *decimation*. The output can be further decimated at the system level by selectively reading a fraction of the available samples (for instance, every tenth sample). Independent of the decimation ratio, the converter's noise performance (and effective resolution) remains unchanged.

Conversion Accuracy/Performance

Like integrating ADC's and V/F converters, a delta-sigma ADC does not contain any source of nonmonotonicity and thereby offers "theoretically perfect" DNL with no missing codes. The ADC in the modulator is simply a comparator, and the DAC is the positive and negative voltage references. No precision ratio matching is needed as in other medium- or high-speed A/D conversion techniques such as successive-approximation. Useful resolution is limited only by residual quantization noise which, in turn, is determined by coarse analog and high-performance digital filtering.

Linearity error is limited only by imperfections in the input sample/hold. The CS5317 achieves typical nonlinearity of just ± 0.003 % through the use of high-quality on-chip silicon dioxide capacitors with low capacitor voltage coefficient.

SECTION B

OVERVIEW: DIGITAL FILTERING

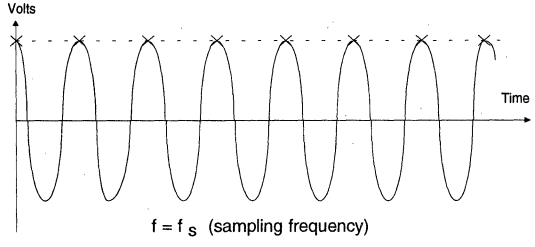
A conventional analog filter implements a mathematical equation using reactive components (capacitors and inductors). A digital filter can implement the same filter equation using two fundamental arithmetic operations: multiplication and addition (or accumulation). A digital filter considers a consecutive sequence of digitized samples a "waveform." It analyzes the relationship between samples, processes the data, and outputs an adjusted waveform.

Digital filters offer ideal stability, repeatability, and potentially perfect performance (linear phase, etc.). Digital filters also remain impervious to environmental conditions, thus providing superior reliability over time and temperature. The major difference compared to analog filters, though, is that digital filters operate on a signal in sampled form.

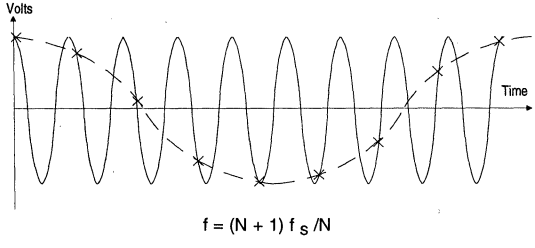
Sampled-Data Theory

A fundamental phenomenon in sampled-data systems is an effect called "aliasing." Basically, *once an analog signal is sampled, its frequency components are no longer uniquely distinguishable.* Figure B1a shows a special case called "dc aliasing." If a signal is sampled precisely at its fundamental frequency, it will always be sampled at the same point on the waveform. It thus becomes indistinguishable from a dc input. Likewise, a signal at twice the sampling frequency (or any integer multiple of f_S) would appear as dc as well. Figure B1b illustrates a more general case of aliasing. Again, two signals at different frequencies become indistinguishable once sampled.

The effect of aliasing in the frequency domain is illustrated in Figure B2. The baseband spectrum (dc to one-half the sampling rate) also "appears" around integer multiples of the sampling rate, *and vice-versa.* In signal processing applications,



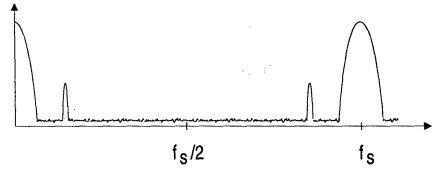
a. dc Aliasing



b. General Aliasing

Figure B1. Aliasing in Sampled-Data Systems

a. Continuous-Time Input Spectrum



b. Sampled-Data Spectrum

Figure B2. Sampled-Data Spectrum

anti-alias filtering is used to bandlimit the analog signal before it is sampled. This removes out-of-band components which could be mistaken for important information in the band of interest.

Aliasing is critical in digital filtering. A digital filter is incapable of distinguishing signals in its passband from signals aliasing from around its sampling frequency. Its passband spectrum therefore repeats around integer multiples of the sampling frequency. Take for instance the case of dc aliasing shown in Figure B1a. A digital low-pass filter would treat the signal at f_S as a dc input and pass it with no attenuation. Similarly, if the filter would attenuate the lower-frequency signal in Figure B1b by 10 dB, the higher-frequency signal would receive the same 10 dB of attenuation. The higher-frequency signals in both cases could be selectively filtered only by analog anti-alias filtering *before the signal is sampled.*

Sampling rates are usually set high enough that analog anti-alias requirements become trivial (or perhaps eliminated). Higher oversampling ratios offer greater bandwidth to roll off between the passband and sampling frequency. Noise in the digital domain can be analyzed just as it is in the analog domain. Limiting a system's bandwidth will reduce noise and improve dynamic range.

Digital Filtering

The most popular digital filtering technique is averaging. A sequence of digital samples are simply collected and averaged to produce an output. This reduces noise by limiting the effective noise bandwidth. Averaging yields a (sin x)/x (or sinc) filter response as shown in Figure B3. The zeroes of infinite rejection (at f_S/N, $2f_S/N$, $3f_S/N$, etc.) can be strategically placed by selecting f_S and the number of samples averaged, N, to average over an integral number of periods of critical frequencies (50 Hz, 60 Hz, etc.). Of course, this same principle lies at the heart of integrating ADC's, but the averaging is done in analog form. In both cases greater dynamic range (or resolution) can be achieved by increasing integration time. The trade-off is bandwidth.

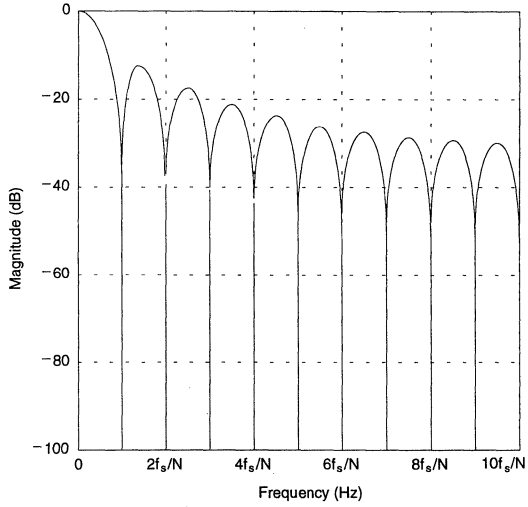


Figure B3. Averaging Filter Response

FIR Filters

Averaging is an elementary example of FIR, or *Finite Impulse Response*, digital filtering. Finite Impulse Response indicates that the filter considers only a *finite* number of inputs to calculate each output. The number of samples determines the *impulse response duration.* For example, a filter which averages ten samples has an impulse response duration of ten. Longer durations indicate more information is considered for each calculation, resulting in a more powerful filter response.

A digital filter's *impulse response* is what determines its filter function. It is basically a weighting function applied to the sequence of samples being considered. The averaging filter is an elementary example of an FIR filter because it uses equal weighting (weight = 1/N where N = # samples). More sophisticated impulse responses extract the information contained in the *relation-*

ship between samples. Averaging filters ignore this information.

Figure B4 illustrates how an FIR filter actually implements the impulse response. The two basic operations are multiplication (indicated by ⊗) and addition - or accumulation - (indicated by Σ). Filter coefficients a_0 to a_3 represent the impulse response. The three unit delay elements insure that each output is calculated using the current input sample and the three previous samples. The filter's input, x(n), and output, y(n), are digital words of any length. (For the CS5317, x(n) is 1-bit and y(n) is 16-bits). Each digital output requires one complete *convolution.* For the 4th-order filter shown in Figure B4, one convolution consists of four multiplications and the accumulation of the four products.

FIR filters are often described in terms of *taps.* This terminology hails back to analog transversal filters, which were basically analog implementations of the filter in Figure B4. The analog delay elements were termed taps. The number of taps indicated the filter's impulse duration. The longer the duration, the more powerful the filter.

Decimation

Digital filters often operate with input sampling rates well above the bandwidth of interest. This serves to minimize analog anti-alias filtering requirements. The filter's output rate, however, is generally dropped to a more manageable system sampling rate. Any reduction in sampling rate is termed *decimation.*

To illustrate the decimation process lets return to averaging. A filter which collects ten samples and then averages them to produce one output *decimates by ten.* That is, for an input rate of f_S, the output rate is $f_S/10$. Alternatively, one could use a "rolling average." For each input sample received, an output would be calculated using that sample and the nine previous samples. The sampling rate would therefore remain at f_S with no decimation.

The 4th-order FIR filter in Figure B5 exhibits the same filter response as that in Figure B4, but decimates by a factor of four. In this case, only one multiplication is performed per input cycle. Without any delay elements, the accumulator needs four input cycles to complete one convolution. Output samples are therefore produced at $f_S/4$. Decimation clearly relaxes computational complexity.

Decimation does not affect overall signal-to-noise or dynamic range. For this reason, one can decimate the CS5317's 20 kHz output (by selectively reading a fraction of the available samples) without affecting the converter's noise. However, a digital signal is normally not decimated if additional filtering is to be used to increase dynamic range (and resolution). All noise energy in a sampled signal lies between dc and one-half the

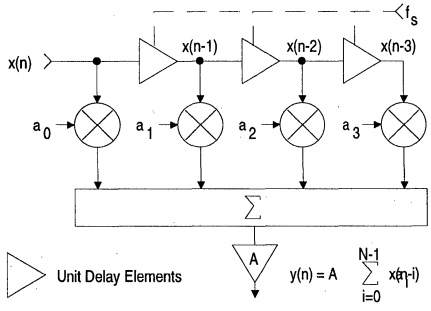


Figure B4. 4th-order FIR Filter

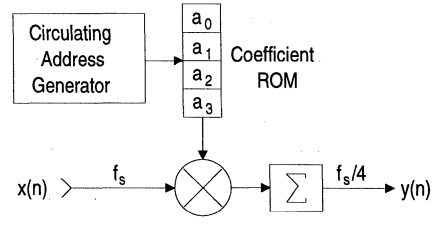


Figure B5. 4th-order FIR Filter with 4X Decimation

sampling rate. Lower sampling rates therefore exhibit larger noise *densities* in the bandwidth of interest for a given amount of noise energy due to aliasing.

FIR Characteristics

The only source of inaccuracy in digital filters is rounding errors due to finite word lengths in the computations. If properly designed, a digital filter will not induce linearity, offset, or gain errors.

Aside from their simplicity, FIR filters' most popular characteristic is their ability to implement perfectly linear phase filters. The effect of every input sample on the output is always seen a *fixed* number of cycles later. This processing delay from input to output is termed the filter's *group delay*, and can be shown to equal one-half the impulse response duration.

Unfortunately, FIR filters can only implement zeroes, no poles. Roll-off is therefore limited. Of course, this limitation can be overcome by cascading FIR filters to produce an extraordinarily long impulse duration. (Fortunately stability is not an issue with FIR filters). The trade-off, though, is an extraordinarily long group delay.

IIR Filters

Infinite Impulse Response filters, on the other hand, can implement zeroes *and poles* to achieve high roll-off. Unlike FIR filters, which use previous inputs to calculate an output, IIR filters also utilize *historical output information* to calculate each new output. In this manner, IIR filters can implement mathematical filter equations with variables in the denominator (that is, poles).

The only drawback to IIR filters is their computational complexity. Since their computations use historical information on their past outputs, *each output must be calculated.* That is, unlike FIR filters an IIR filter cannot decimate to reduce computational complexity. Therefore, IIR filters generally operate with lower sampling rates.

The CS5317 Voice-band A/D Converter Implementation

The CS5317 uses oversampling, decimation, and FIR filtering to implement its digital filter. The CS5317 samples its analog input at 2.5 MHz (for a full-rated 5 MHz master clock). This high oversampling ratio of 500:1 (2.5 MHz sampling/5 kHz bandwidth) reduces external analog anti-alias requirements.

The FIR filter decimates the sampling rate from 2.5 MHz to 20 kHz to reduce computational complexity. The filter features an impulse response duration of 384 x 2.5 MHz and a decimation ratio of 128 (2.5 MHz:20 kHz). Since the filter does not decimate by 384 as shown in Figure B5, multiple convolutions must be in process concurrently. To achieve this, the CS5317 uses three accumulators working from a single 384-word coefficient memory. The three convolutions are spaced to begin and end 128 samples apart. Thus, a new 16-bit output sample becomes available every 128 input samples (for a decimation ratio of 128) whereas each 16-bit output is calculated using 384 input samples (for an impulse response duration of 384).

The CS5501 dc Measurement A/D Converter Implementation

The CS5501 uses oversampling, decimation, and both FIR and IIR filtering to implement its 6-pole Gaussian filter. The CS5501 samples its analog input at 16kHz (for a full-rated 4.096MHz master clock). This high oversampling ratio of 1600:1 (16kHz sampling/10Hz bandwidth) reduces *and most often eliminates* external analog anti-alias requirements.

The FIR filter is used to decimate the sampling rate from 16kHz to 4kHz to reduce computational complexity in the subsequent IIR filter. The

FIR filter response is not especially critical. Its only goal is to reject energy within ±10Hz bands around integer multiples of 4kHz, the IIR filter's sampling rate.

The IIR filter is needed to implement the poles in the 6^{th}-order Gaussian filter and achieve high roll-off of 120dB/decade. Its baseband filter characteristics are shown on page 4. Note that the filter's entire frequency response can be scaled by adjusting the master clock. The converter's sampling rate simply scales accordingly. With its cut-off frequency set at 10Hz (4.096MHz master clock) for maximized settling, the CS5501 offers 55dB rejection at 60Hz. With a 5Hz cut-off, though, 60Hz rejection increases to greater than 90dB. Master clocks as low as 40.96kHz are acceptable, yielding cut-off frequencies as low as 0.1Hz.

The CS5326 Digital Audio A/D Converter Implementation

Linear-phase finite-impulse-response (FIR) filters are used for decimation. The 1-bit, 3.072 MHz outputs of the modulators are decimated in steps of 8, 4, and 2 to yield 16-bit, 48kHz results.

The decimation strategy includes two stages, FIR1 and FIR2, whose primary responsibility is attenuation of quantization noise prior to decimation and aliasing. Modulator out-of-band quantization noise spectral density is very high. FIR1 and FIR2 use 17 and 18-bit coefficients to attenuate this noise, and out-of-band input signals, into the converter noise floor. Filter orders are 27 and 30, respectively.

A third stage, FIR3, performs passband shaping and out-of-band signal attenuation. Passband frequency response errors introduced by the modulator, FIR1, and FIR2 are corrected by FIR3. Overall filter passband ripple is thus reduced to ±0.001dB from dc to 22kHz. The passband compensation function prevents the use of a half-band filter for FIR3. Data is truncated to 16 bits at the output, and this operation is the major noise contributor in the system.

FIR1, FIR2, and FIR3 also combine to provide antialiasing filtering. All analog input frequencies from 26kHz to 3046kHz are attenuated by at least 86dB. Phase response is precisely linear.

Application Note

The CS5504 Family Characteristics

The CS5504/5/6/7/8/9 are a series of A/D converters all derived from a high performance ΔΣ architecture. The CS5504 family members are based on a core architecture including both an analog modulator and a digital filter, with only subtle differences between the individual products. The digital filter has been optimized to attenuate ac line interference (50/60 Hz and their harmonics) when the devices are operated from a low-cost 32.768kHz crystal.

The use of a low-cost 32.768kHz clock provides 20 samples per second from the family. The CS5505/6/7/8 can achieve up to 100 samples/second with a 163kHz system clock, while the CS5504/9 can achieve up to 200 samples/second when operated from it's maximum input clock of 330 kHz. In achieving higher conversion rates, the CS5504 requires slightly higher operating currents than the CS5505/6/7/8. The CS5509 achieves the same high conversion rate as the CS5504 with lower power consumption, but pays a slight penalty in linearity.

Table 1 summarizes the similarities and differences of the CS5504 family.

The CS5504/9 come in smaller packages than the CS5505/6/7/8, however, the CS5505/6/7/8 have more functionality and flexibility. The CS5505/6/7/8 offer a sleep function, an on-chip voltage reference, and multiple serial communication modes.

Table 2 shows the CS5504 family's wide array of power supply options. Note: the CS5509 is single supply, however, the VA+ supply for all devices must always be the most positive operating voltage under all operating conditions, including start-up.

	VA+	VA-	VD+
CS5504/5/6/7/8	+5 to +10V	0V	+5V
	+5V	0 to -5V	+5V
	+5V	0 to -5V	+3.3V
CS5509	+5V	-	+5V
	+5V	-	+3.3V

Table 2. Power Supply Arrangements

5

	Resolution	#Channels	Max. Speed[3]	Linearity[4] (Typical)	Sleep	Power	On-chip VREF	Serial Port Modes[5]	Pin Count
CS5504	20-bits	2[1]	200	0.0007%	No	4.4 mW	No	SEC	20
CS5505	16-bits	4[2]	100	0.0015%	Yes	3 mW	Yes	SEC, SSC	24
CS5506	20-bits	4[2]	100	0.0007%	Yes	3 mW	Yes	SEC, SSC	24
CS5507	16-bits	1[1]	100	0.0015%	Yes	3 mW	Yes	SEC, SSC	20
CS5508	20-bits	1[1]	100	0.0007%	Yes	3 mW	Yes	SEC, SSC	20
CS5509	16-bits	1[1]	200	0.0015%	No	1.7 mW	No	SEC	16

Table 1. CS5504 Family Characteristics

Notes:
1. Fully-differential
2. Pseudo-differential
3. CS5509 is production tested at 330 kHz (200 samples/second)
   All others are production tested at 32.768 kHz for the best 50/60 Hz rejection.
4. These linearity specifications are based on a 20Hz output rate using a 32.768kHz crystal.
5. SEC is synchronous external clocking of the data out while SSC is synchronous self-clocking.

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX 445-7581

• Notes •

Application Note

CS5516 and CS5520: Overcoming Errors in Bridge Transducer Measurement

The CS5516 and CS5520 Bridge Transducer A/D converters address many of the common error sources encountered when digitizing bridge transducers. This application note describes many of these error sources and explains how to minimize their effects. Many of the features of the CS5516 and CS5520 which allow for the control of these error sources are also discussed. Some of the content of this application note was originally a portion of the CS5516 and CS5520 data sheet and was titled" Enemies of the Strain Gauge".

Strain gages are sensing devices which change resistance when subjected to mechanical stress. The amount of stress to which the gage is exposed is usually limited to minimize possible damage to the gage due to overstress. A strain gage is a passive electrical device. Most often gages are configured in a Wheatstone bridge configuration to enhance their sensitivity while minimizing the effects of drift. The bridge may be excited with either a voltage or a current. Excitation is supplied through connecting leads to the bridge. The connecting leads will include resistances (R_{p1} and R_{p2}) as shown in Figure 1. These resistances will affect the gain of the bridge:

$$A_V = \frac{AIN+ - AIN-}{VEXC+ - VEXC-}$$

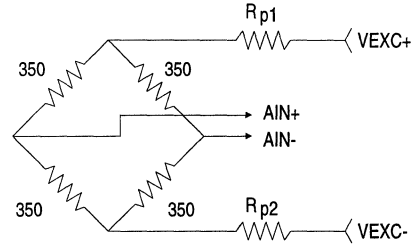


Figure 1. Four-Wire Bridge

When a bridge connected gage set is included as part of a mechanical assembly (often called a load cell), a connecting cable is often included. Manufacturers will include the errors due to R_{p1} and R_{p2} in the specification for the load cell assembly.

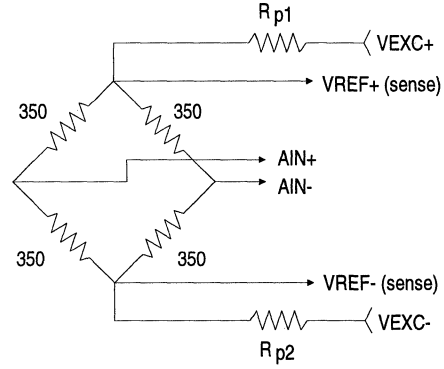


Figure 2. Six-Wire Bridge

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX 445-7581

A six-wire bridge, as shown in Figure 2, allows for force and sense (Kelvin connection) leads to measure the excitation directly at the bridge. This allows all errors due to R_{p1} and R_{p2} to be removed if a ratiometric measurement system (as provided by the CS5516 and CS5520) is employed.

Bridge Offsets

It is common for bridge configured load cells to have a zero offset specified to be as great as ±10% of the full scale output signal. In a typical digitizer this offset must be "trimmed out" by adjusting a potentiometer. This may be necessary to reduce the portion of the dynamic range of the measurement system which is consumed by the offset of the load cell. In some weighing systems, another source of offset which may consume dynamic range is the pan weight; sometimes called the tare weight. Prior to making a weighing, an empty pan is placed on the scale. Then a zero or tare button is activated and signals the digitizer to remove the offset produced by the empty container. After the offset due to the pan weight is removed, the actual item to be measured is then added to the pan. Pan weight can consume a large portion of the dynamic range of the digitizer depending upon the method by which it is removed from the measurement.

The CS5516 and CS5520 converters include a 4-bit offset trim DAC. The DAC allows the removal of up to ±200% of the selected range's full scale before the signal is digitized. This avoids the loss of resolution in the digitizer caused by load cell or pan weight offsets. The converters also include a ratiometric offset calibration register which can be calibrated or manipulated to add or subtract offsets from the digital output words after conversion has been performed. This allows the transfer function of the converter to be offset (either plus or minus) to accommodate load cell zero drift or load cell creep.

Of critical importance when removing offset is for the DAC output to remain ratiometric to the voltage reference if the voltage reference should change. The CS5516 and CS5520 converters are designed to perform ratiometric, non-reference sensitive offset removal.

50/60 Hz Pickup

It is common in some weighing applications for the load cell to be located some distance from the digitizer. The load cell leads can become exposed to radiated noise caused by line interference at 50 or 60 Hz. Twisted pair interconnections should always be used on the AIN+, AIN- and VREF+, VREF- pairs to minimize 50/60 Hz pickup. Nonetheless, some amount of line interference is inevitable.

The line interference may enter into the A/D converter circuitry by either the AIN signal input or the VREF input (Line interference may also appear on the power supply leads, in which the power supply rejection of the A/D converter is an important issue, but in this discussion the focus is on the interference picked up by the transducer leads).

When line interference enters the AIN and VREF inputs of a traditional A/D converter, the interference will most likely introduce errors into the output words of the converter. To understand why, assume that 60 Hz interference enters into the converter by means of both the AIN and VREF inputs. The AIN signal is:

$$AIN+ - AIN- = V_{IN} + b\cos(2\pi 60t)$$

Assuming the input and reference paths are well matched, the VREF input would be:

$$VREF+ - VREF- = V_{REF} + b\cos(2\pi 60t)$$

The A/D converter computes the ratio:

$$\frac{AIN}{VREF}$$

The dc component of the A/D output is obtained by averaging the ratio of AIN/VREF over a 60 Hz period of T = 16.7 msec. The AIN and VREF inputs include the interference component bcos(2π60t) as shown in the previous equations:

$$\frac{1}{T}\int_0^T \frac{AIN+ - AIN-}{VREF+ - VREF-}\,dt = 1 + \frac{V_{IN} - V_{REF}}{\sqrt{V_{REF}^2 - b^2}}$$

To develop a feel for this result, let's define some real input conditions as an example. Assume a typical converter has a full scale span of 2.5 volts (VREF = 2.5) and the input signal AIN is 0.6 volts. The converter would output a digital code which states that the input is a ratio of 0.6/2.5 or 0.240 of full scale. If there is no line interference on the AIN and VREF inputs, that is b = 0, (no interference pickup), the output result from the equation above is AIN/VREF= 0.6/2.5, or 0.240 as desired. If the interference is not zero, that is, b0, (let's say the line interference has a magnitude of 10 mV, that is 0.010) the output result will include an error caused by the interference. The result will be:

$$1 + \frac{V_{IN} - V_{REF}}{\sqrt{V_{REF}^2 - b^2}} = 1 + \frac{0.6 - 2.5}{\sqrt{2.5^2 - 0.010^2}}$$

or

$$1 + \frac{0.6 - 2.5}{2.499980} = 0.2399939$$

If we take the ratio 0.2399939/0.240 = 0.9999745

The result is 25.5 ppm less than it would have been, had the measurement not included the interference. 25.5 ppm is equivalent to about 26-27 counts error in a 20-bit A/D converter; or 1.66 counts error in a 16 bit A/D converter.

Note that the error when interference is present will be zero only if AIN = VREF, that is only if the AIN signal is a full scale input with the same magnitude (including line interference) as on the VREF input. This measurement condition is unlikely to occur.

We see that line interference can cause measurement errors. Interference into only the voltage reference input can introduce similar errors into the converter.

The CS5516 and CS5520 converters minimize errors due to line interference because the AIN and VREF inputs to the converter are actual independent A/D converters which use a common voltage reference which is internal to the converter chip. Each of the two signals (AIN and VREF) are converted and processed by independent digital filters before the AIN/VREF ratio is computed. With an appropriate choice of operating clock frequency for the converter, the digital filters remove 50 and 60 Hz (and their harmonics). The robustness of the conversion output is significantly enhanced when operating in harsh 50/60 Hz environments.

5

Non-Ratiometric Errors

A variety of offset sources can introduce errors into the measurement which do not scale with the excitation voltage; hence the name non-ratiometric errors. Amplifier offset voltages and parasitic thermocouples are two common non-ratiometric offsets. The measurement errors which can be caused by non-ratiometric offsets will be examined more closely and then parasitic thermocouples will be discussed more thoroughly.

The first offset to be considered is shown as V_{OS} in Figure 3. The ADC output is given by:

$$D_{OUT} = \frac{V_{IN}}{V_{REF}} = A_V + \frac{V_{OS}}{V_{REF}}$$

The sensitivity of D_{OUT} to changes in the excitation voltage will be termed S_1:

$$S_1 = \frac{\delta D_{OUT}}{\delta V_{REF}} \frac{V_{REF}}{D_{OUT}} = \frac{-V_{OS}}{A_V V_{REF} + V_{OS}}$$

Some practical values illustrate the significance of this equation. Suppose the sensitivity of the load cell is 2 mV/V (A_V = 0.002) and the excitation supply (VREF) is 10 V. Assume that V_{OS} = 20 µV and that it is a non-ratiometric offset generated by a parasitic thermocouple or by the offset of a precision amplifier. This yields a sensitivity S_1 = 0.001. Sensitivity factor S_1 is a measure of the sensitivity of the converter output code D_{OUT} to changes in the excitation supply. The excitation supply may drift due to temperature changes or due to limited line and load regulation. A typical regulator may change 1% over changing line, load, and temperature changes. With S_1 = 0.001 a typical 1% change in the excitation supply will cause a 0.0001% change, or a 10 ppm change in D_{OUT}. This 10ppm error is in addition to the error introduced by the 20 µV offset itself. This 10 ppm error is significant, being 10 counts in a 20-bit converter or 2/3 count in a 16-bit converter.

The above equation suggest three methods of reducing V_{OS}-induced errors:

1) Buy a gauge with a large A_V.
2) Use a large excitation voltage (VREF).
3) Measure V_{OS} and calibrate it out.

The CS5516 and CS5520 converters include the features necessary to calibrate out non-ratiometric offsets. Calibration is only effective if the non-ratiometric offsets are stable after being calibrated. The converters also support ac bridge excitation which removes the effects of non-ratiometric offsets (more on this later).

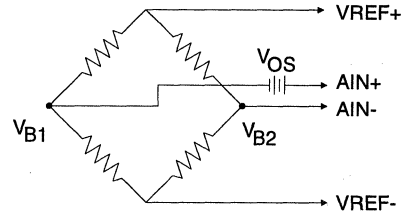


Figure 3. V_{OS} Offset

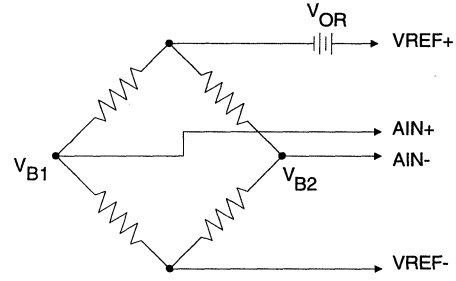


Figure 4. V_{OR} Offset

A second non-ratiometric error is shown as V_{OR} in Figure 4. Its sensitivity is given by:

$$S_2 = \frac{\delta D_{OUT} V_{REF}}{\delta V_{REF} D_{OUT}} = \frac{-V_{OR}}{V_{REF} - V_{OR}}$$

Not surprisingly, in this case increasing A_V doesn't help.

Sensitivities S_1 and S_2 simply confirm that, when non-ratiometric errors are present, the A/D converter output will vary as the excitation voltage changes. A zero tempco, zero aging, excitation supply with perfect line and load regulation can reduce this variation, but one major advantage of a ratiometric measurement system should be that a precise, stable reference is not necessary.

Again the non-ratiometric calibration capabilities of the CS5516 and CS5520 can remove the adverse effect of V_{OR}.

Thermocouples

A common source of non-ratiometric error is the parasitic thermocouple. Thermocouples result any time that two dissimilar metals are joined. Common tin-lead solder and copper traces of a PC board create a thermocouple junction with a thermal EMF (electro-motive force) of 3.1-3.4 μV/°C. It is common for components such as resistors to have wire leads composed of different metal alloys than the resistor element itself. Therefore each end of the resistor has a thermocouple junction as an integral part of the resistor. Soldering the leads to the circuit board traces creates more thermocouple junctions. It is imperative that low level measurement circuits have an identical number of junctions in the differential signal path and that differential inputs be routed next to each other. Interconnecting devices (connectors and IC sockets) and relays should be chosen to minimize thermocouple effects. A circuit board layout should optimize trace and junction placement, and component placement and orientation, to match the thermocouple effects of a differential signal path. While perfectly matched thermocouple chains produce zero differential inputs, thermal gradients exist in any "real world" measurement system. Temperature dependent non-ratiometric offsets result.

The use of non-ratiometric offset calibrations can substantially reduce thermocouple errors. Nonetheless, temperature gradient fluctuations are difficult to eliminate. In addition to non-ratiometric offset calibration of the AIN and VREF channels the CS5516 and CS5520 converters also support ac bridge excitation. AC bridge excitation can help minimize the errors caused by parasitic thermocouples.

AC excitation, as shown in Figure 5, alternately flips the excitation voltages at the top and bottom of the bridge.

With ac excitation, the desired signal flips in polarity as the excitation voltage flips. The analog input becomes a square wave at the excitation frequency as the excitation voltage flips. V_{OS} doesn't flip. When the CS5516/20 synchronously demodulates the square wave in ac excitation mode, V_{OS} is modulated up into the digital filter's rejection band. V_{OS} problems are just filtered away.

Any systems design that can exploit the benefits of ac excitation probably should. Accuracy fluctuations with temperature can be virtually eliminated. Any remaining non-ratiometric errors can still be attacked with non-ratiometric calibrations when ac excitation is used. The CS5516/20's BX1 and BX2 pins provide for both internally and externally controlled excitation signals.

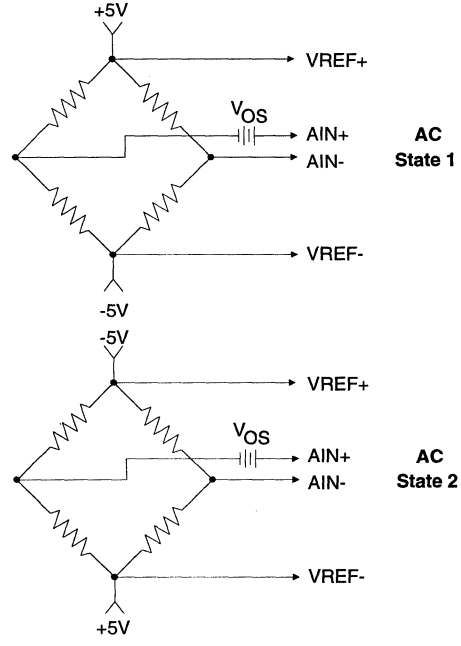


Figure 5. AC Excitation

Offsets due to leakages

Moisture or other contaminants in load cell cables or on the printed circuit board can cause current leakage paths, one of which is illustrated in Figure 6.

The current source model is appropriate since the resistance of the leakage path is often much larger than that of the gage. Comparison with Figure 5 reveals that both ac excitation and non-ratiometric calibration serve to reduce measurement errors due to these leakage current paths.

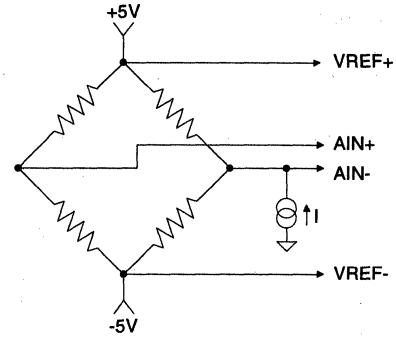


Figure 6. Leakage Effects Offset

Conclusion

This application note has presented some of the errors encountered in bridge transducer digitizers, and has indicated how the CS5516 and CS5520 A/D converters can overcome these errors.

Application Note

A Collection of Bridge Transducer Digitizer Circuits

by

Jerome Johnston

Introduction

Bridge transducers are common in instrumentation. This application note illustrates some bridge transducer digitizer circuits which use the CS5504/5/6/7/8/9 A/D converters and the CS5516/20 A/D converters.

The CS5504/5/6/7/8 converters can be operated with a variety of power supply arrangements; including operating from a single +5 V supply; operating from +5 and -5 analog supplies with +3.3 V or +5 V on the digital supply; or operating with an analog supply from +5 to +11 V and a digital supply of +5 V.

The CS5509 can operate with +5 V on its analog and digital supplies; or with +5 V analog and +3.3 V digital.

The CS5516 and CS5520 are A/D converters optimized for bridge transducer applications and are designed to operate from +5 and -5 V supplies. Several circuits which utilize these ADCs will be presented.

The application note is divided into two sections:

1. DC-excited bridge circuits.
2. AC-excited bridge circuits with a discussion of the benefits of AC excitation.

Bridge Transducers

Bridge transducers are manufactured with various technologies. The strain-sensing elements which make up the bridge may be made of diffused silicon, bonded silicon bars, deposited thin film, or bonded foil materials. The choice of technology will determine the performance of the transducer, including the sensitivity, the linearity, and the thermal stability. Silicon-based gages have good linearity with sensitivities between 3 mV/V and 20 mV/V, but tend to exhibit more drift as temperature changes. Metal foil or thin film gages have good linearity with sensitivities between 1 mV/V and 4 mV/V. Precision bridge transducers include some type of temperature compensation as part of the bridge.

Most bridge circuits are excited with a dc voltage, 10 volts being very common. With 10 V excitation, the full scale signals from the various transducers, can be as low as 10 mV to as high as several hundred millivolts. When digitizing these signals to high resolution (for discussion in this application note, high resolution means greater than 10,000 counts), one count can represent a very small voltage. It can be difficult to amplify and digitize these low level bridge transducer signals. Measurement performance can be hindered by such things as amplifier

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX 445-7581

offset drift, amplifier noise (both thermal and 1/f), amplifier finite open loop gain, and parasitic thermocouples. Parasitic thermocouples are introduced any time two dissimilar metals are connected. For example, using tin-lead solder to solder a wire to a copper PC trace can introduce an unwanted thermocouple junction which changes as much as 3 µV/°C when subjected to temperature gradients.

This application note will introduce some A/D converter circuits which illustrate a number of application ideas to the design engineer who uses bridge transducers. In the AC-excited bridge section, a number of design ideas will be introduced which offer very good solutions to some of the problems encountered in low level bridge measurement.

DC-EXCITED BRIDGE CIRCUITS

CS5507,8,9 Bridge Transducer Operating From a Single +5 V Supply, or with the Analog Supply at +5 V and Digital Supply at +3.3 V

Figure 1 illustrates the low cost CS5509 16-bit converter operating from +5 V. The A/D can operate in either unipolar or bipolar mode and yields 20 conversions/second when running from a low cost 32.768 kHz crystal. When operated at 32.768 kHz the digital filter in the converter notches out 50 and 60 Hz line interference.

The LTC1051 dual chopper amplifier is used as the bridge amplifier. Bandwidth is limited to about 3.8 Hz by the 100k and 0.47 µF feedback

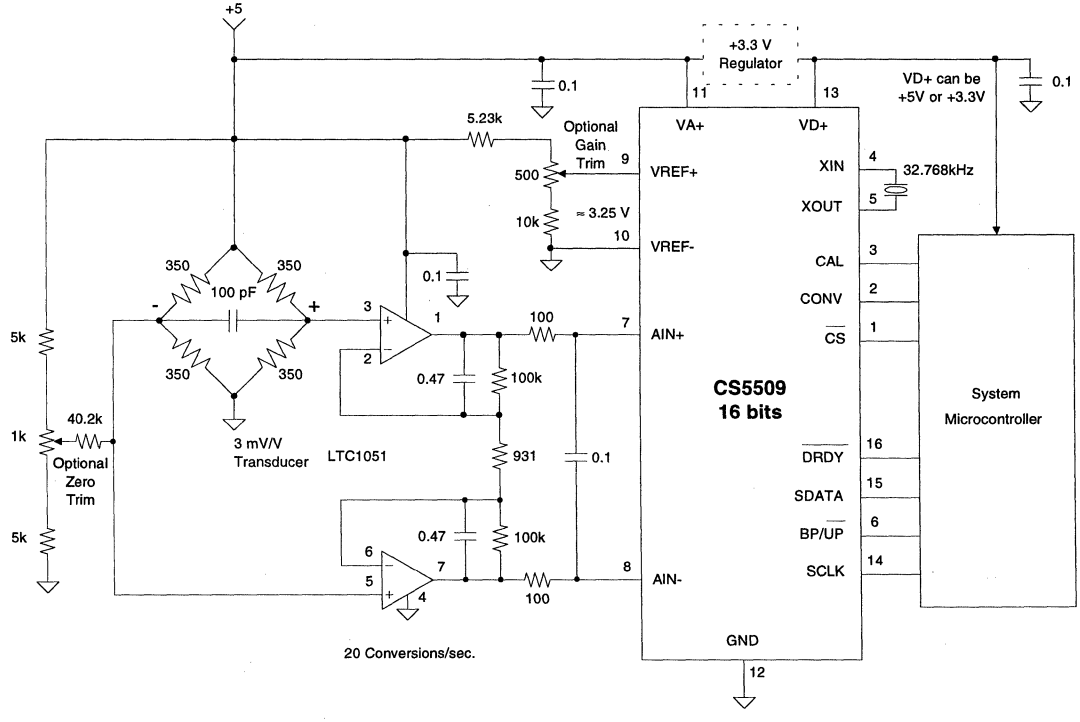


Figure 1. CS5507,8,9 Bridge Transducer Operating from a Single +5 V Supply, or with the Analog Supply at +5 V and Digital Supply at +3.3 V.

elements of the amplifier stage. Note that an instrumentation amplifier is not needed because the A/D input is fully differential. The dual amplifier functions as a differential in, differential out amplifier. The circuit yields about 9000 noise-free counts when measuring unipolar signals. Averaging 10 samples increases this to about 28,500 noise-free counts. "Noise-free counts" means full scale signal divided by six times the rms noise. Noise-free counts is good figure of merit for comparing A/D converters used in dc measurement applications. There is more discussion on this topic at the end of the application note.

The circuit illustrated uses a 3 mV/V transducer excited with +5 V for a full scale transducer output of 15 mV. The transducer output is amplified with a gain of about 216 to yield 3.25 V full scale. A dual stage amplifier, as shown in Figure 2 may be preferred to minimize errors due to limited loop gain. The A/D is operated in bipolar mode to achieve more μV/LSB. The reference voltage for the converter is derived from the +5 V excitation voltage. The measurement remains ratiometric should the +5 V excitation change.

Figure 1 includes potentiometers for offset and gain adjustment, as do a number of other circuits in this application note. Many system designers prefer to eliminate potentiometers and do all offset and gain correction in software. To

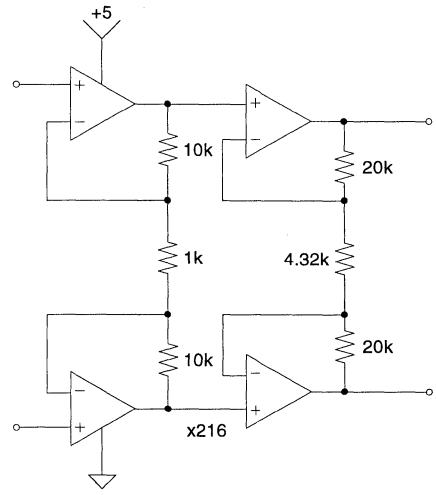
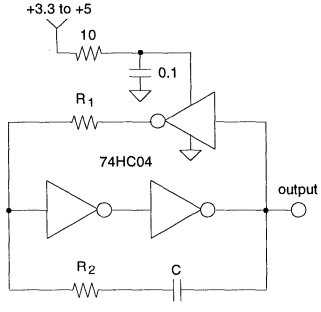


Figure 2. Dual Stage Amplifier

achieve this in some of the circuits may require changes to gain stages or voltage references, but potentiometers are shown for all the engineers who are more comfortable with screwdrivers than software.

The CS5509 in Figure 1 can run as fast as 200 conversions per second if operated with a 330kHz external clock. Figure 3 shows an RC gate oscillator which can produce stable frequencies, or a CMOS 555 timer can be used. The gate oscillator can be operated from either a +5 or +3.3 V supply and maintains fairly good frequency stability over temperature.

5



f	R_1	R_2	C
162kHz	10k	3.4k	330pF
200kHz	8.2k	2.7k	330pF
330kHz	5k	1.6k	330pF

$$f \approx \frac{1.44}{2(R_1 + R_2)C} \qquad R_2 \approx \frac{R_1}{3}$$

Figure 3. Temperature-Stable Gate Oscillator for +5 or +3.3 Volts.

All of the converters (CS5504-09) can be operated with a single +5 V supply. All of the converters can also be operated with +5 V analog supply and +3.3 V on the digital supply. If this dual supply arrangement is used, the digital supply should be derived from the analog supply to ensure proper operation. Under all conditions, including start-up, the voltage on the VA+ pin must be the more positive than any other pin on the device to ensure proper substrate biasing of the chip.

CS5507/8 with +10 V Analog Supply and +5 V Digital Supply

It is common for many weigh scales to be operated from batteries with a 12 V automotive-type battery being common. The CS5504/5/6/7/8 devices can be operated with higher supply voltage on the analog portion of the chip than on the digital portion (Note: the CS5509 is an exception and is specified with an analog supply of +5 V only). The analog supply (VA+) must always be the most positive voltage on the chip to ensure proper operation. Figure 4 illustrates the CS5507 operating from +10 V on the analog and +5 V on the digital. The bridge is excited with the +10 V and resistors are used to divide this excitation supply to obtain a ratiometric voltage reference of about 3.33 V for the converter. The circuit is designed to operate with the A/D in bipolar mode to yield more μV/count. The A/D is set-up for an input span of ± 3.33 V. A 200k pull down resistor forces a

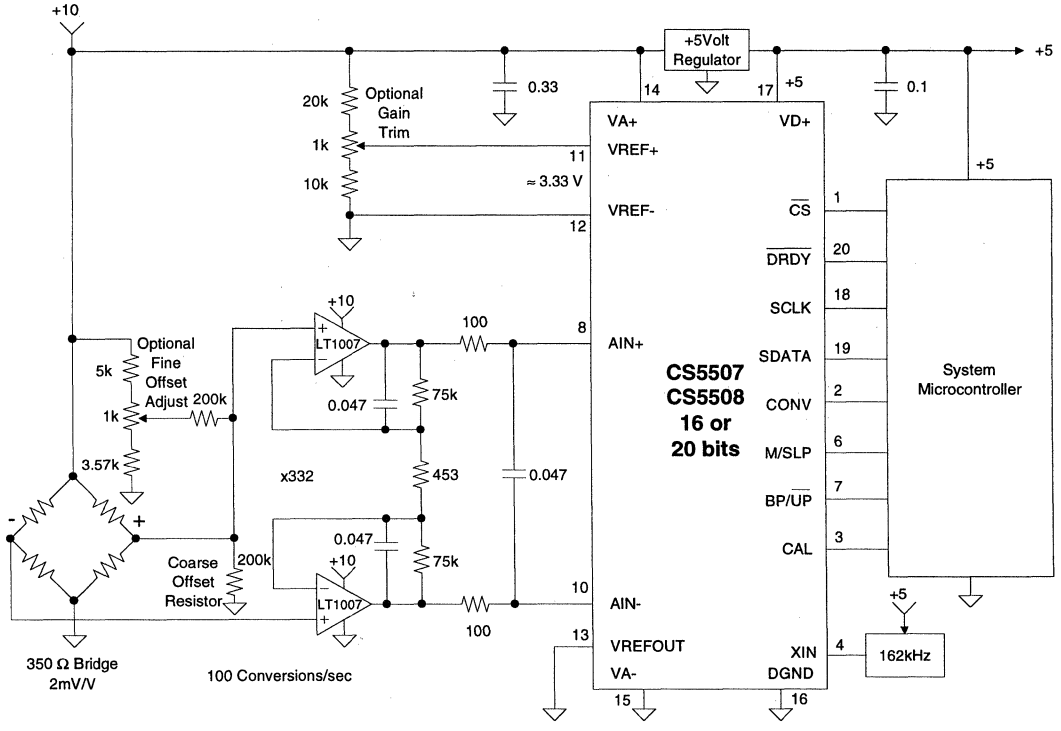


Figure 4. CS5507/8 with +10V Analog Supply and +5 V Digital Supply.

negative offset into the amplifier and the zero trim is used to finely adjust this offset. With zero weight on the scale, the zero trim is adjusted to yield -30,000 counts if the CS5507 16-bit A/D is used or to -500,000 counts if a 20-bit CS5508 is used. With full scale weight on the scale the gain trim is adjusted for +30,000 counts in the CS5507 or +500,000 counts in the CS5508 (Note that the CS5507 and CS5508 are pin compatible). This leaves some counts for both zero underflow and for overrange. The amplifier components set the bandwidth to 45 Hz. With the 45 Hz bandwidth, the circuit exhibits about 50,000 noise-free counts. With an external 162 kHz clock, the converter can operate at 100 conversions per second. If 20 conversion words from the CS5508 are averaged, the circuit will yield more than 200,000 noise-free counts. A limitation of this circuit is that the bipolar amplifiers can exhibit significant offset drift as the temperature changes. There are several circuits in this application note which will show how to overcome offset drift.

CS5505/6 Operating From ± 5 V Supplies

The CS5504/5/6/7/8 converters (not the CS5509) can be operated with ±5 V on the analog section of the converter, and with either +5 V or +3.3 V on the digital section.

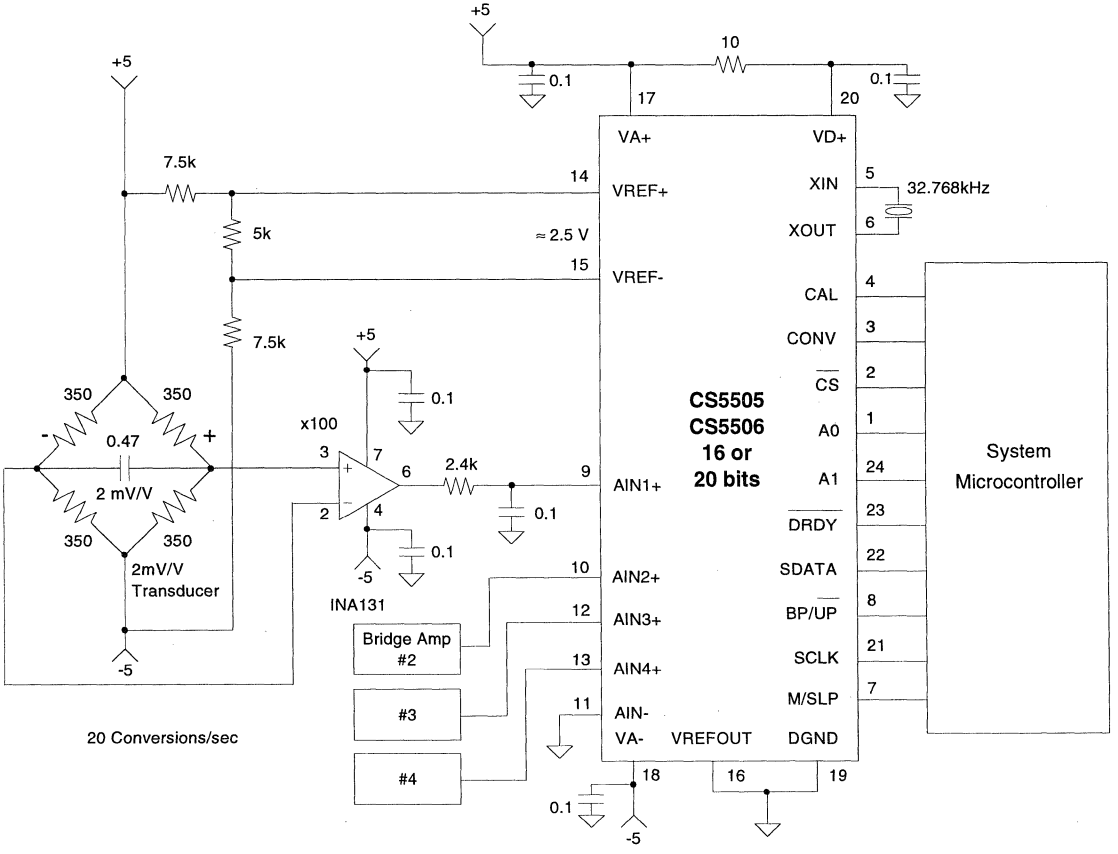


Figure 5. CS5505/6 Operating from ± 5V Supplies.

Figure 5 illustrates an application which uses an instrumentation amplifier to amplify and convert the differential bridge signal to a ground-referenced signal for the converter. Full scale for the converter is set by the divider resistors which determine the voltage reference input to the VREF+/- pins of the converter. The reference voltage in the figure is set to 2.5 V. The bridge sensitivity is 2 mV/V so the full scale bridge output is 20 mV. This is amplified by the 100 gain of the instrumentation amplifier to obtain 2.0 V into the converter. The converter can be operated in either unipolar or bipolar mode. Up to four load cells, each with its own amplifier, can be input to the CS5506. The measurement assumes the voltage reference will remain ratiometric across all four load cells.

CS5507 Switched-Bridge Low-power Digitizer with +10 V Excitation

Some applications call for reduced operating power. One method of significantly reducing the power consumption is to apply the supply voltage to the bridge transducer only when a

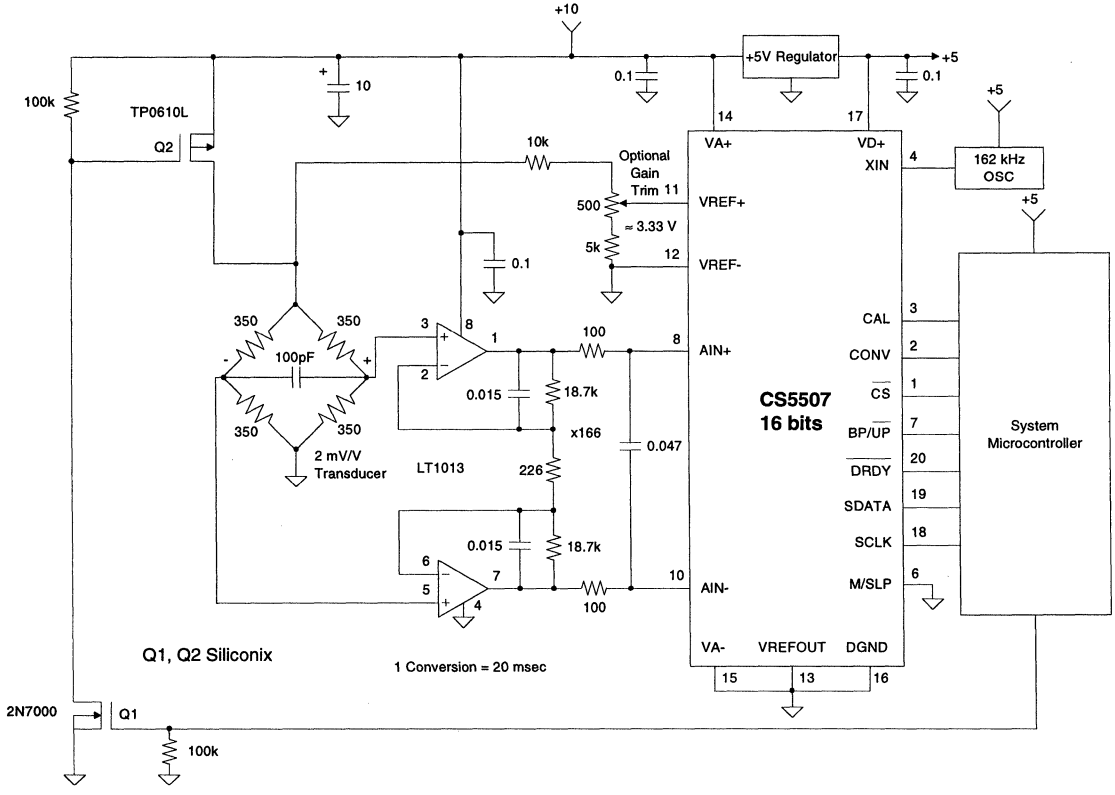


Figure 6. CS5507 Switched-Bridge Low-power Digitizer with +10 Volt Excitation.

measurement is required. Figure 6 illustrates an example circuit in which the power to the bridge transducer is switched on only when a measurement is desired.

The circuit as shown is optimized for a +10 V analog supply. The circuit can be modified (optimized) to operate from any analog supply from 11 V to 6.5 V (assuming the +5 V regulator needs 1.5 V of input/output differential) by changing the resistor values which determine the voltage reference to the converter and by changing the gain resistors in the amplifier to compensate for the change in the bridge output signal. The circuit shown illustrates a 2 mV/V transducer outputting 20 mV full-scale. A gain of 166 amplifies this to 3.32 V into the A/D. The full-scale of the A/D is set at 3.33 V by dividing down the excitation voltage.

In the power arrangement shown, the CS5507 A/D uses about 4 mW. The converter is clocked from an external gate oscillator clock (162 kHz) to yield a conversion time of 10 msec. When power is applied to the bridge, a delay must occur to allow the signal to settle before a valid conversion can be performed. Settling time to 16 bits after power is applied to the bridge takes about 3.3 msec. The microcontroller can use an internal timer to time about 4 msec. to allow for the delay or the microcontroller can perform a dummy conversion in the converter to allow for settling time. When the dummy conversion is finished (10 msec. later) the conversion data is discarded and a second conversion is then performed to make a valid measurement. After the second conversion is complete ($\overline{\text{DRDY}}$ falls the second time) power to the bridge is deactivated and the conversion word is clocked out of the converter's serial port.

Power consumed by the transducer dominates the power dissipated in the circuit. Average power consumption in the bridge can be reduced by a factor of at least fifty (<6 mW) if the bridge is powered for only 20 msec. for a reading each second. If even lower off power is desired, the supply to the LT1013 can also be switched along with the bridge excitation.

CS5509 Switched-Bridge Low-power Digitizer with +5 V Excitation

The circuit in Figure 7 is similar to the previous one, but operates from a single +5 V. The circuit shows a load cell with 3 mV/V sensitivity. A 2 mV/V transducer can be used if additional gain is added; or the voltage reference into the converter can be lowered to 1.67 V with some minor increase in noise. Average power consumption in the load cell is only 1.5 mW for one reading per second.

CS5516/CS5520 Using DC Bridge Excitation

The CS5516 (16-bit) and CS5520 (20-bit) A/D converters are designed for bridge measurement applications. They include an instrumentation amplifier with X25 gain, a PGA (programmable gain amplifier) with gains of 1, 2, 4, and 8, and a four bit DAC which can trim out offset up to ± 200% of the full scale signal magnitude. The input span can be adjusted by changing either the magnitude of the voltage at the VREF pins of the converter or by changing the PGA gain.

In the circuit shown in Figure 8, the bridge is excited with ± 5 volts. Resistors R1, R2, and R3 divide the excitation voltage to give a 2.5 V reference signal into the VREF pins. The input span at the AIN pins of the converter is determined by dividing the voltage at the VREF pins by the PGA gain and the X25 instrumentation amplifier gain. For example, with 2.5 V into the VREF pins, and the PGA set to a gain of 8, the input span at the AIN pins is 2.5/(8 X 25) = 12.5 mV in unipolar mode or ± 12.5 mV in bipolar mode. The converter offers several calibration features to remove offset and to calibrate the gain slope. The input span of

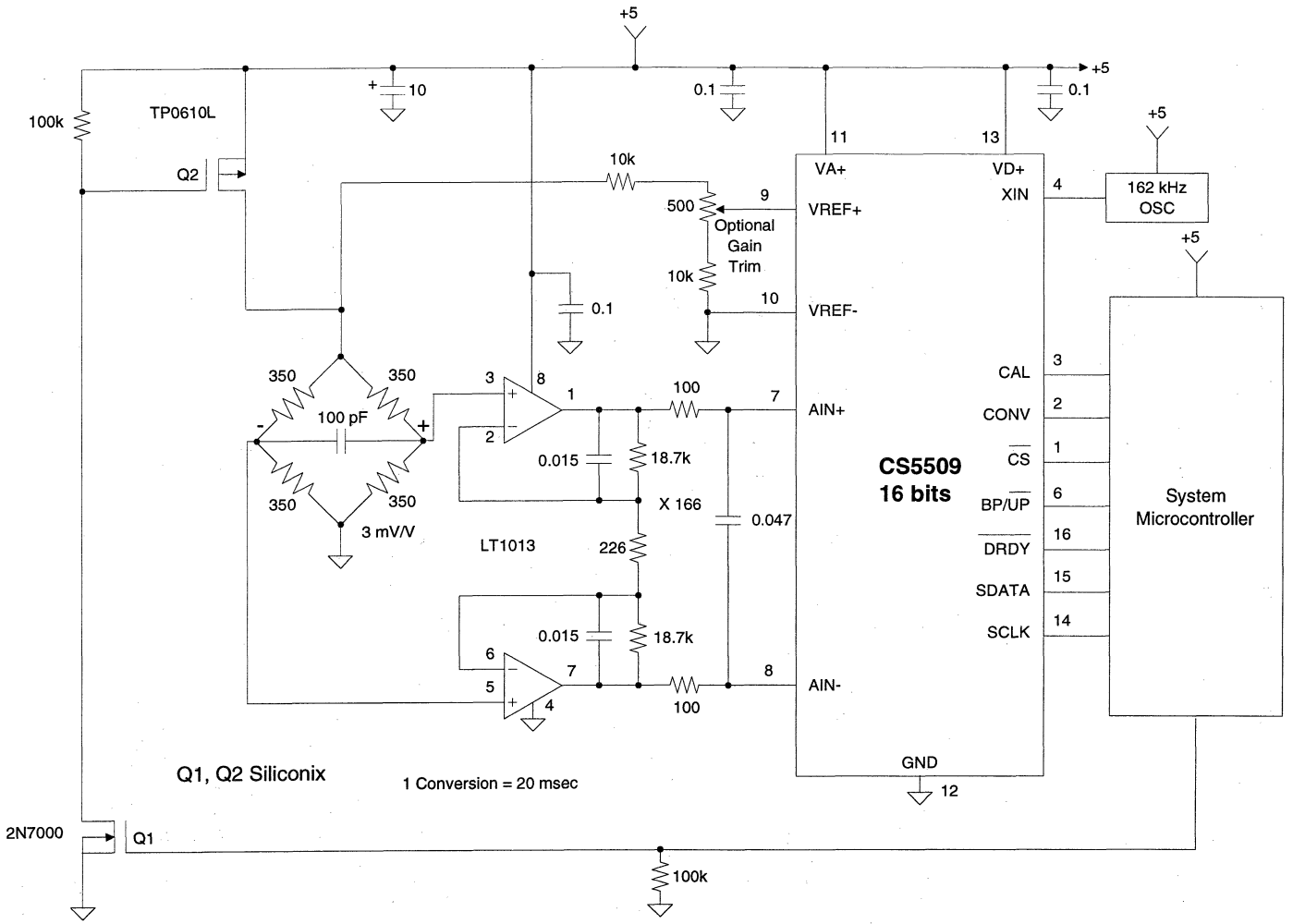


Figure 7. CS5509 Switched-Bridge Low-power Digitizer with +5 Volt Excitation.

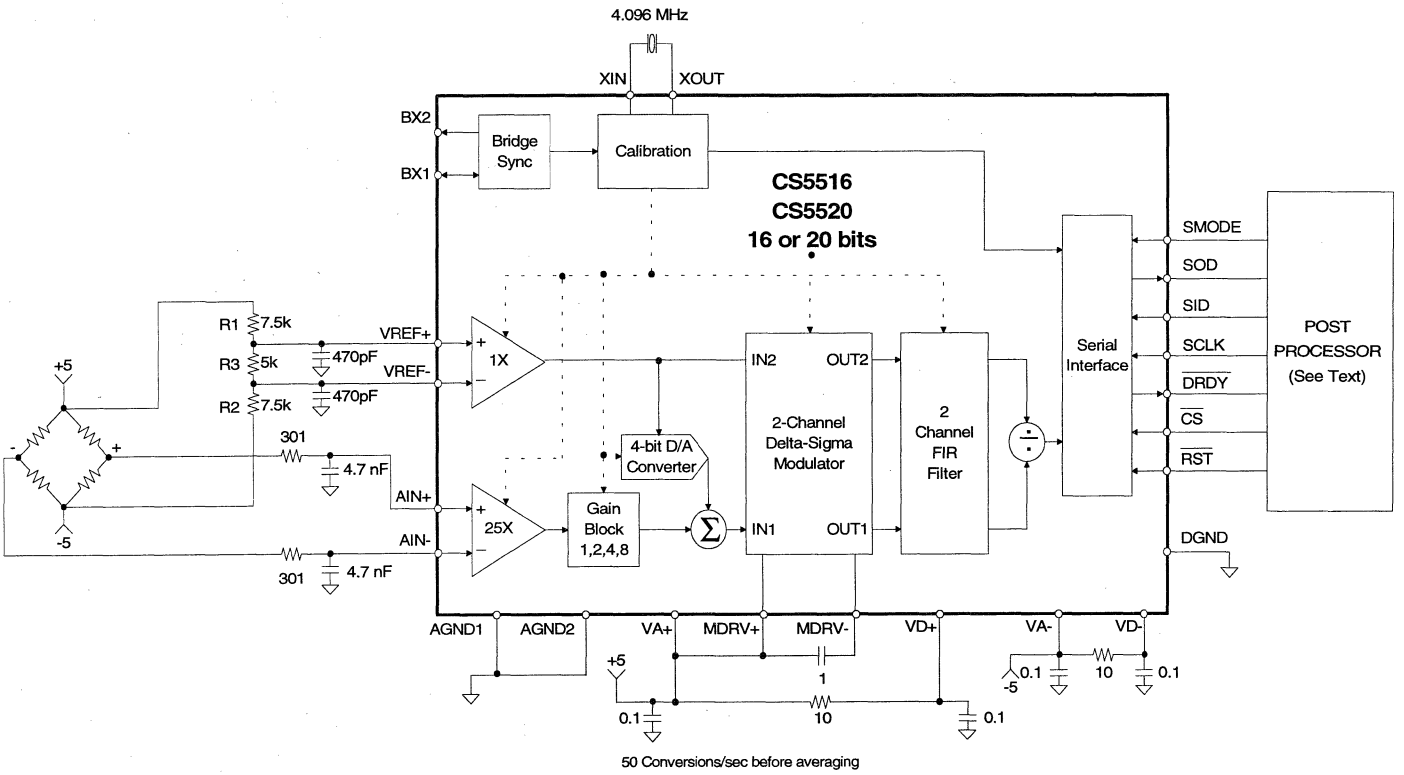


Figure 8. CS5516/CS5520 Using dc Bridge Excitation.

12.5 mV (considered the nominal value for this particular selection of PGA gain and VREF voltage) can be gain calibrated for input signals from 20 % less than or 20 % greater than the nominal 12.5 mV value. In other words, the gain can be calibrated with an input as low as 10 mV or as high as 15 mV when the nominal value is set for 12.5 mV. The nominal input can be changed by changing the PGA gain or by changing the divider resistors for the excitation voltage. The converter can accept a VREF input voltage of any value between 2.0 to 3.8 V.

The CS5516 and CS5520 can be operated on any clock frequency from 1.0 MHz to 5.0 MHz. the digital filter will give greater than 90 dB of attenuation to 50 and 60 Hz line interference if the input clock is 4.096 mHz or less. With a 4.096 MHz clock into the converter it will output conversion words at a 50 Hz rate. For optimal filtering it is desirable to average output words from the converter. If ten output words are averaged, the noise bandwidth is reduced to about 2.5 Hz.

The CS5516 and CS5520 support either dc or ac bridge excitation.

AC-EXCITED OR CHOPPED SIGNAL BRIDGE CIRCUITS

When measuring low level signals, measurement performance can be enhanced if the signal is "chopped". Chopper amplifiers are commonly used to minimize amplifier offset drift. The disadvantage of chopper amplifiers is that they are generally manufactured using CMOS technology and have higher thermal noise than bipolar amplifiers. Chopper amplifiers have low offset drift and the 1/f noise of the amplifier tends to be averaged out due to chopping. Still, CMOS integrated circuit chopper amplifiers tend to have noise performance somewhere between 45 $nV/\sqrt{Hz}$ to 250 $nV/\sqrt{Hz}$. This noise limits the measurement performance when used in a high resolution bridge digitizer. Another limitation of a chopper amplifier is that it corrects only its own offset errors and does not correct offsets or parasitic thermocouples external to itself, including those created when its own package leads connect to the circuit card traces.

There are several other approaches to chopping the signal which can be used to enhance performance. Circuits will illustrate a number of these approaches. Some chop the signal after it is output from the bridge. Others actually switch the polarity to the bridge itself. Either method can be used to remove amplifier offsets and parasitic thermocouple effects. Switching the bridge has the advantage that it enables any nonratiometric offset of the bridge to be removed. But caution is advised; some silicon gages can be damaged if the excitation supply is reversed. Check with the gage manufacturer to determine if a silicon gage bridge can be used with AC excitation.

Switching the bridge may not be practical in applications which have very long cables due to the large cable capacitance.

Bridge with Digital Offset Correction and Kelvin Reference Sensing.

One method of getting the lower noise of bipolar amplifiers and achieve good offset stability is to use digital offset correction. Figure 9 illustrates a circuit in which the input of the amplifier stage is periodically shorted and the offset measured with the A/D. The digital code is then used to correct readings from the converter when the signal is being measured. The schematic shows only the circuitry for one channel (the CS5504 has two input channels). Only one half of the DG303 is used per channel. LT1007 op amps are used for their low noise; but a dual LT1013 or quad LT1014 could be used if higher noise is acceptable. The LT1013 and LT1014 are capable of measuring signals with an input range which

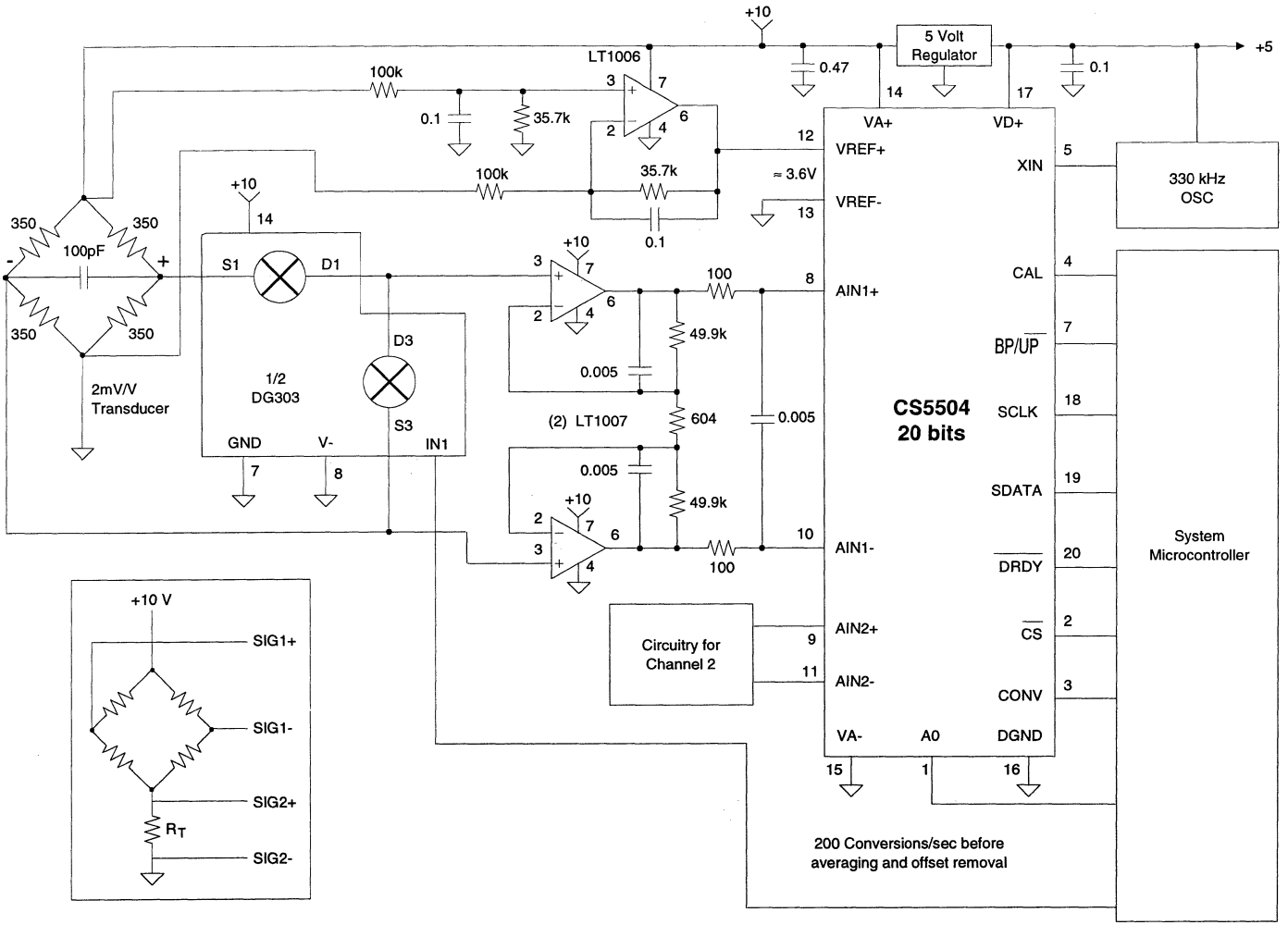


Figure 9. Bridge with Digital Offset Correction and Kelvin Reference Sensing.

includes the negative supply rail. One application for this may be for measuring a temperature compensating resistor in series with the bridge (see inset in Figure 9).

The converter in Figure 9 is set up in bipolar mode (use bipolar mode even if you want unipolar measurements as the bipolar setup provides less noise per code and allows for negative tempco drift of the zero reference point) and runs at 200 conversions a second. To correct offset and measurements on both channels, the following measurement sequence was used: Select the DG303 to short the inputs to both channel one and channel two. Use A0 on the converter to select channel one. Perform one conversion and discard the data to allow for settling. Perform a second conversion and keep the offset code for channel one. Change A0 to opposite state and measure the offset code for channel two. Switch the DG303 on both channels to measure the input signal and set A0 to measure channel one. Perform one dummy conversion and discard the data. Then perform a second conversion and keep the reading. Correct this reading with the offset reading taken for the same channel. Then change A0 and read channel two and correct it for offset. Each channel takes four conversions per result, so for two channels, outputs are available at 25 per second. A running average of 12 corrected words is recommended to improve noise performance. With 12 words averaged, the performance is greater than 150,000 noise-free counts with two updates per second for each channel.

If the circuit in Figure 9 is used at higher temperatures, one DG303 should be used for each amplifier stage with a switch (always on) included in the negative lead of the bridge circuit. With this configuration, the errors due to leakage currents and the on resistance of the switches will be more balanced on both the plus and minus leads of the bridge.

The voltage reference input to the A/D converter is buffered to reduce loading by the Kelvin sense leads. If the voltage reference Kelvin sensing lines are long, 50 and 60 Hz line interference may be picked up. The voltage reference input to the CS5504/5/6/7/8/9 should be filtered to prevent line interference if the devices are operated at a clock frequency other than 32.768 kHz.

Bridge with Signal Chopping Using CS5504

The load cell is often the dominant cost factor in many weighing systems. A lower cost load cell can be achieved by leaving out the temperature compensation gages and reducing testing during manufacturing. As long as the load cell temperature drift is repeatable, the entire system can be compensated with software in a microcontroller. In this type of system, a temperature sensor is usually embedded inside the load cell. The entire system is then characterized over temperature. A microcontroller reads the load cell and its temperature and uses a look-up table to correct the load cell output for drift over temperature. Figure 10 illustrates an example.

The circuit uses the CS5504 two channel fully differential A/D configured to convert at 200 samples per second. The analog portion of the A/D and the bridge are operated from +10 volts. The voltage reference for the A/D is developed from the bridge excitation. Channel two of the converter measures the output of a thermistor mounted in the load cell housing. The thermistor is excited with the same voltage as the bridge.

The output of the bridge is amplified by a buffer amplifier composed of two LT1007s. The CS5504 is operated in bipolar mode with ± 524,000 counts. A DG303 analog switch is used to reverse the polarity of the signal into the amplifier upon command from the microcontroller. A convert (CONV) command is

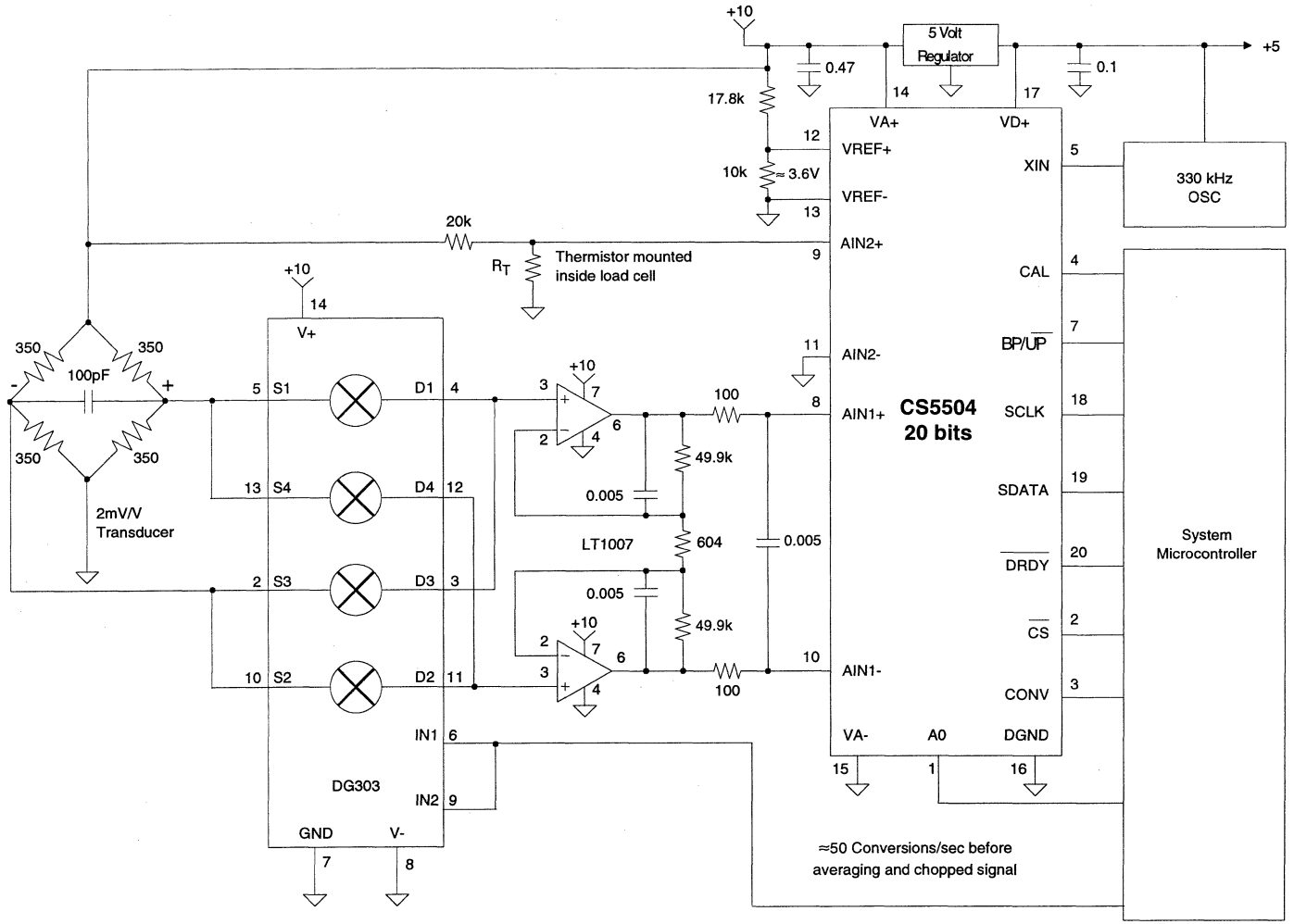


Figure 10. Bridge with Signal Chopping Using CS5504.

issued to the converter only after the DG303 switch has been switched to one position long enough for the buffer amplifier to have settled on the signal. With the DG303 in one position, the output of the amplifier will result in a positive voltage into the converter; when switched to the other position the output of the amplifier will be negative into the converter. The negative reading is then subtracted from the positive reading and then divided by two[(+answer - (-answer)]/2. The result will be a reading of the load cell signal with the offset of the amplifier removed. For example, let us assume the circuitry has +332 counts of offset and the signal from the bridge (the bridge itself has no offset for illustration purposes) should be 4700 counts. The reading from the converter with a positive input signal will be 5032 counts; the reading with the signal reversed will be -4368 counts. [5032 - (-4368)]/2 = 4700 counts, which is the answer with the offset averaged out. Note that dividing by two is really unnecessary as the number (9400) is representative of the signal magnitude. The converter can sample at 200 samples per second; performing a conversion every 5 msec. The converter has two channels but needs not to measure the temperature channel very often. The measurement sequence for channel one is follows: Switch the DG303 to condition one (switches 1 and 2 are on, switches 3 and 4 are off); perform a conversion but throw the data away as this conversion time is used to allow the amplifier to settle (the circuit shown takes less than 4 msec. to settle). Then perform a second conversion and keep the data. Switch the DG303 to condition two (switches 3 and 4 are on, 1 and 2 are off); perform a conversion but throw away the data to allow for settling. Then perform a second conversion, subtract the negative answer from the previous positive one (from switch condition one) and divide the answer by two (if you need the actual answer). Since it will take four conversion cycles to obtain one averaged answer, the converter will be able to update at a 50 Hz rate (assuming the temperature channel is not being read). The effects of noise in the output data can be reduced if words are averaged. An average of 20 of the final readings will result in a noise reduction of 4.4 times. Converting in this fashion will result in a converter with greater than 150,000 noise-free counts, and an update rate of about two and a half times per second. Chopping the signal lowers the input drift in the amplifier to about 125 nV peak-to-peak under slowly varying temperature conditions.

Switched Bridge with CS5504 Using +10 V Analog Supply

The previous circuit achieved offset stability by chopping the bridge output. In the circuit in Figure 11 the polarity of the excitation voltage to the bridge is periodically reversed. Channel one of the CS5504 is used to measure the amplified signal from the bridge. The second channel of the converter is used to measure the magnitude of the bridge excitation. The bridge excitation is measured because the driver exhibits some change in drive output over temperature. The measurement sequence is as follows. For notation let the bridge excitation be in position one when the top of the bridge is +10 V (the actual voltage will be about 9.5 to 9.8 V depending upon the driver source impedance). When switched to this position, the microcontroller pauses for a short delay (1 msec or so) before performing a conversion on channel two to ensure that the circuit has settled. Once the conversion is performed on channel two, the data is saved. Then the A0 line to the converter is switched to select channel one. The amplifier has settled during the time the conversion was performed on channel two. A conversion is performed on channel one and the data is saved. Then the bridge excitation is flipped to position two (the top of the bridge is grounded). After a 1 msec delay a conversion is performed on channel two; the negative answer is subtracted from the previously collected positive answer from channel two. Then A0 on

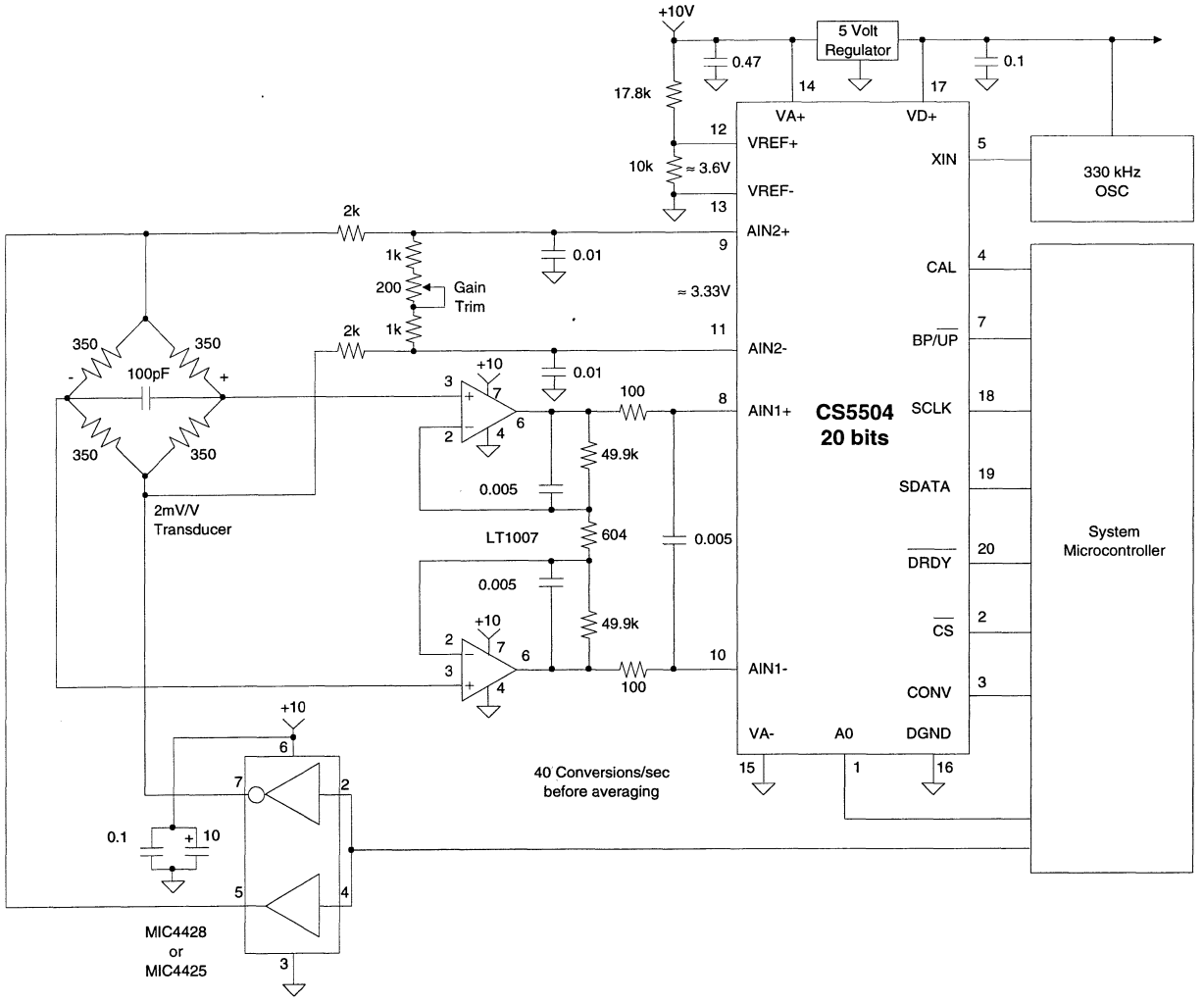


Figure 11. Switched Bridge with CS5504 Using +10 Volt Analog Supply

the converter is flipped and a conversion is performed on channel one of the converter. The negative answer for channel one is then subtracted from the previous positive reading from channel one.

The resultant readings from each channel can be averaged to reduce the effects of noise. Then the readings from the two channels are ratioed. The channel two data represents the value of the excitation on the bridge. Channel one data represents the output signal from the bridge as a proportion of the bridge voltage. By ratioing the data (AIN1/AIN2) any drift in the bridge excitation voltage (such as those caused by changes in the driver output impedance) is compensated.

The circuit can read both channels and calculate a final answer for the bridge signal in less than 25 msec.; which means an output word can be calculated at a rate of 40 times per second. If 20 output words are averaged the circuit will yield better than 100,000 noise-free counts with the offset drift of the digitizer being less than 50 nV over time.

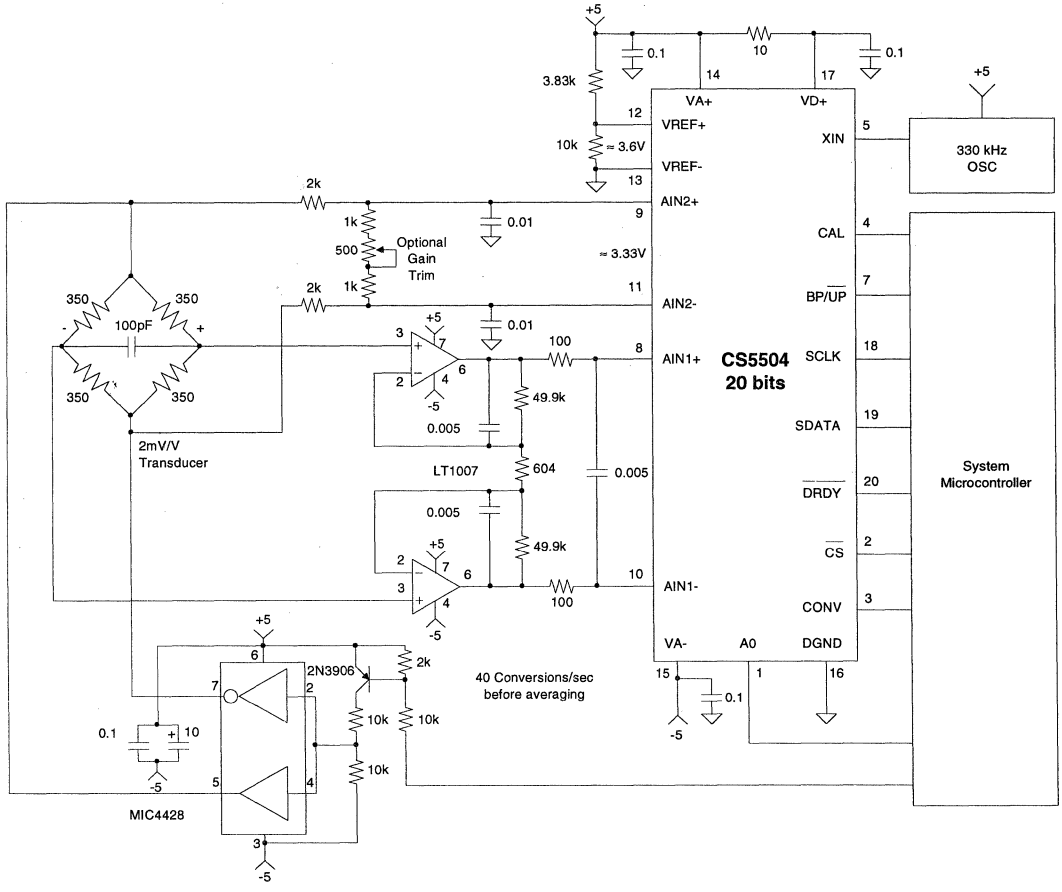


Figure 12. Switched Bridge with CS5504 Using ± 5 Volt Analog Supplies.

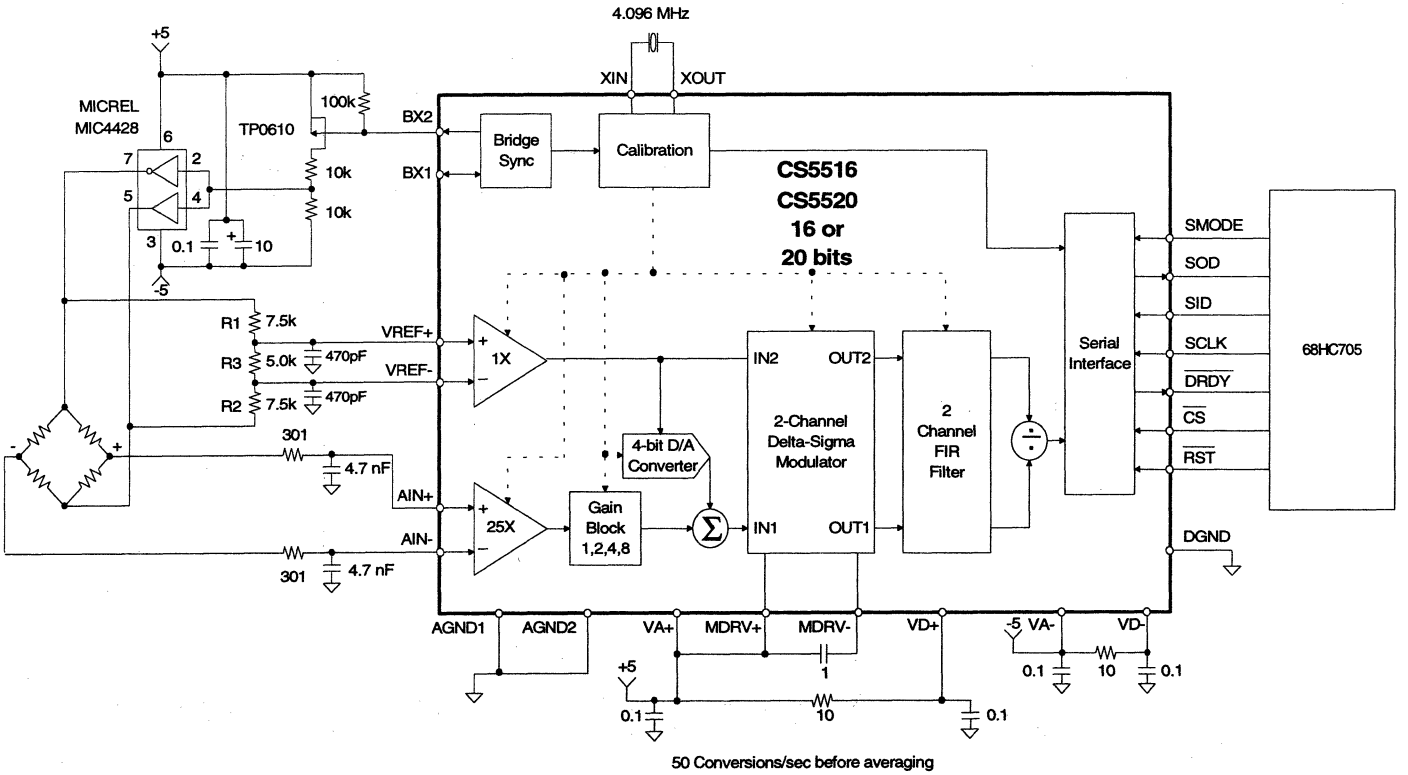


Figure 13. CDB5516/20 Evaluation Board Circuit.

Switched Bridge with CS5504 Using ± 5 V Analog Supplies

This circuit in Figure 12 is basically identical to the previous circuit, but is configured to run from ± 5 V on the analog supplies.

CDB5516/20 Evaluation Board Circuit

The CDB5516 and CDB5520 evaluation boards use the circuit in Figure 13. The CS5516 (16-bit) and CS5520 (20-bit) converters are optimized for bridge measurement applications. The evaluation board comes with software which runs on a PC-compatible computer. The evaluation board includes a microcontroller which communicates with the PC via the RS-232 serial port. The software allows the user to read and write all of the registers inside the CS5516/20 converter, perform conversions, save conversion data to a file, and perform some noise statistics on the captured data.

The CS5516 and CS5520 support both dc-excited bridges and ac-excited bridges. Figure 14 illustrates the benefit of AC excitation. In one of the plots in Figure 14, the CS5520 converter was set up for a bipolar input span of ± 12.5 mV and dc bridge excitation. Conversions were performed with a zero input signal from the bridge and data was collected for a one hour time interval. One LSB of the CS5520 was equivalent to about 25 nV. The data collected indicates that over the one hour period the average value of the data drifted as much as 1.25 µV, or about 50 counts. The drift is due to parasitic thermocouples in the components or wiring of the board. The evaluation board was open to the air. The data illustrates that the cycling of the air conditioner induced thermal gradients across the circuitry, changing the voltage effects of the parasitic thermocouples in the circuitry. The second plot in Figure 14 illustrates the stability of the data when the converter is set up for the same operating conditions, but with ac bridge excitation. The plot illustrates the normal thermal noise of the circuit but the average value remains stable over time.

The CS5516 (16-bit) and CS5520 (20-bit) A/D converters include an instrumentation amplifier with X25 gain, a PGA (programmable gain amplifier) with gains of 1, 2, 4, and 8, and a four bit DAC which can trim out offset up to ± 200% of the full scale signal magnitude. The input span can be adjusted by changing either the magnitude of the voltage at the VREF pins of the converter or by changing the PGA gain.

In the circuit shown in Figure 13, the bridge is excited with a 1 kHz square wave from the MIC4428 (or the Micrel MIC4425) driver. The driver outputs about ± 5 V. The 1 kHz drive signal is output from the BX2 pin of the CS5520. Control bits in a configuration register inside the chip have been set to select internal ac excitation with a frequency of 1 kHz (XIN = 4.096 MHz). The converter is designed to perform synchronous detection on the AIN and VREF input signals when operated in the ac excitation mode. This means that the converter measures the signal which is of the same frequency and phase as the excitation clock coming from the BX2 pin.

Resistors R1, R2, and R3 divide the excitation voltage to give a 2.5 V reference signal into the VREF pins. The input span at the AIN pins of the converter is determined by dividing the voltage at the VREF pins by the PGA gain and the X25 instrumentation amplifier gain. For example, with 2.5 V into the VREF pins, and the PGA set to a gain of 8, the input span at the AIN pins is 2.5/(8 X 25) = 12.5 mV in unipolar mode or ± 12.5 mV in bipolar mode. The converter offers several calibration features to remove offset and to adapt the gain. The nominal input span of 12.5 mV can be gain calibrated for input signals within ± 20% of

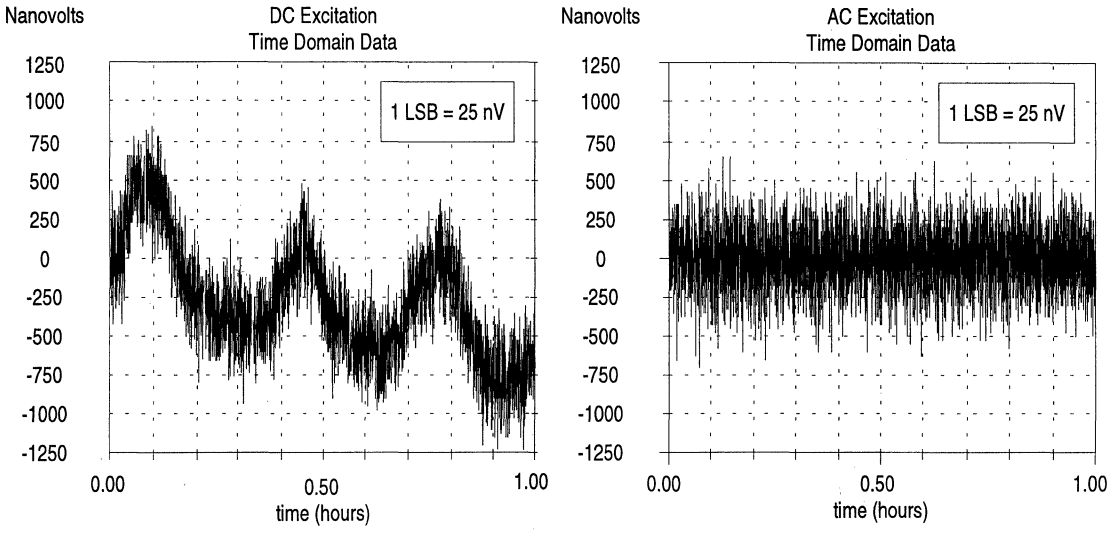


Figure 14. DC Versus AC Excitation.

nominal. In other words, the gain can be calibrated for an input as low as 10 mV or as high as 15 mV when the nominal value is set for 12.5 mV. The nominal input can be changed by changing the PGA gain or by changing the divider resistors for the excitation voltage. The converter can accept a VREF input voltage of any value between 2.0 to 3.8 V. The CS5516 and CS5520 can be operated on any clock frequency from 1.0 MHz to 5.0 MHz. The digital filter will give greater than 90 dB of attenuation to 50 and 60 Hz line interference if the input clock is 4.096 mHz or less. With a 4.096 MHz clock into the converter it will output conversion words at a 50 Hz rate. For optimal filtering it is desirable to average output words from the converter. If ten output words are averaged, the noise bandwidth is reduced to about 2.5 Hz.

CS5516 with External 25 Hz AC Excitation

The CS5516 and CS5520 support two ac bridge excitation modes; internal and external. In the internal excitation mode, the excitation clock is derived internal to the converter from the oscillator frequency on the chip and is output from the BX1 and BX2 pins. In the external excitation mode (selected by setting a bit in the configuration register of the converter), a square wave whose frequency is a sub-multiple of the XIN frequency to the converter (see the CS5516/20 data sheet for details) is input into the BX1 pin of the converter.

When using the CS5516 or CS5520 in the ac excitation mode, the AIN and VREF signals into the converter are sampled 64 XIN clock cycles after the excitation signal is switched. When the square wave excitation changes polarity, the circuitry, including the bridge, the load cell cable, and any filtering components must settle to at least 5 per cent accuracy within the 64 XIN clock cycles after the switching edge. This can be a limiting factor in using square wave ac excitation, especially with long cables which have a large capacitance.

The excitation frequency can be lowered to XIN/(10 X 2^{14}) if output words from the converter are averaged over several conversion cycles. For example, with a 4.096 MHz clock, a

decade divider (74HC4017) can be followed by a binary 2^{14} divider (74HC4020) to yield a 25 Hz excitation frequency. The converter will output conversion words at a 50 Hz rate, or two output words for each one cycle of the bridge excitation. The 25 Hz excitation reduces the switching frequency of the bridge so the circuit spends more time measuring and less time settling. This will improve measurement performance, but multiple output words (an even number of them) must be averaged to ensure equal samples for both polarities of the excitation clock. Figure 15 illustrates this circuit. Note that the details on connecting the clock divider chips have not been shown to simplify the schematic.

CS5516/CS5520 with AC-Excitation Controlled by a Microcontroller

If the load cell cables are very long, the capacitance may be so large that the circuit cannot settle and yield an accurate result with the 25 Hz circuit. Another option exist. Rather than use the counters in Figure 15 to control the BX1 signal and the drive polarity, one can use a microcontroller output line. With the converter set up in the external excitation mode, the microcontroller can control the polarity of the

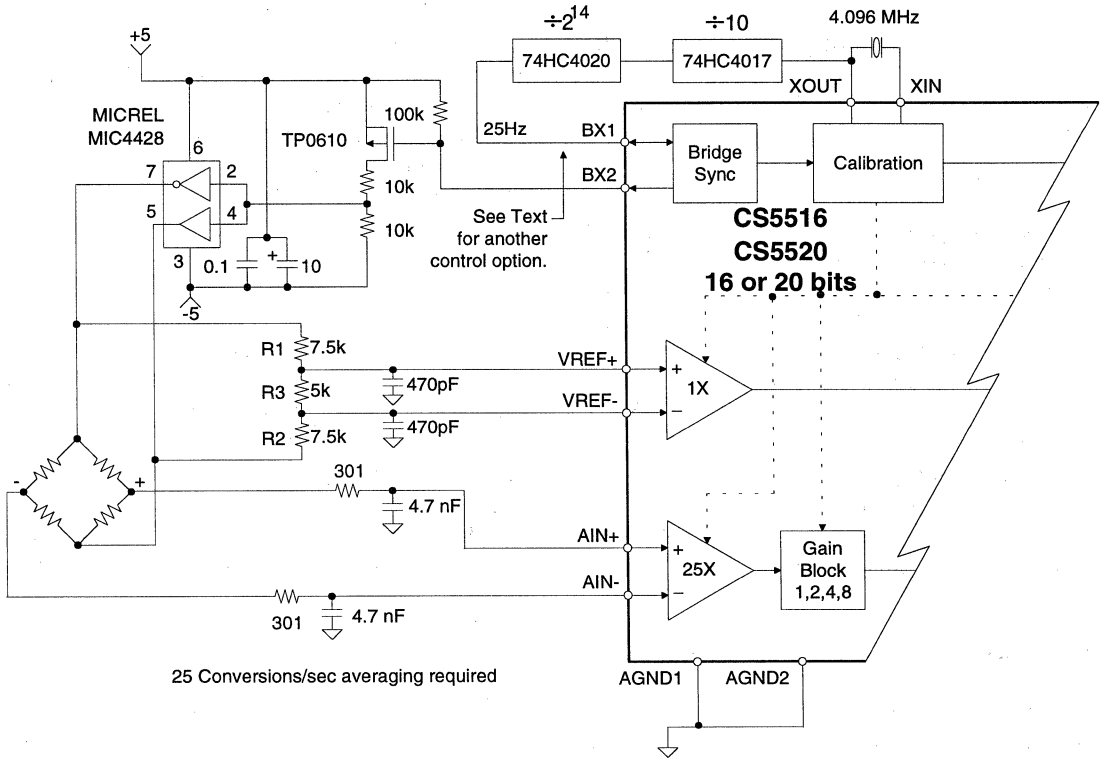


Figure 15. CS5516 with External 25 Hz AC Excitation.

excitation. In external excitation mode, the BX1 pin of the converter is an input and is used to determine the polarity of the excitation. The phase of the signal at BX1 controls the phase of the internal detection circuitry. Each time the polarity of the excitation is changed, the converter needs six conversion word periods for the internal digital filter to accurately settle on the input signal. To yield a proper result, the sixth conversion word for each of the excitation phases will need to be averaged together. For optimum throughput, the excitation polarity should be changed when the $\overline{\text{DRDY}}$ signal falls. The on-chip calibration features may not be usable directly when operating in this manner, but the user microcontroller can manipulate the gain and offset registers in the converter to optimize the the offset and gain adjustments for optimum operation. If the bridge polarity is reversed every six conversion words, an output result can be computed every twelve filter cycles. This will yield an effective conversion update rate of about four updates per second (XIN = 4.096 MHz).

CS5516 or CS5520 and a 1 mV/V AC-Excited Load Cell

Metal film or metal foil strain gages are generally configured to yield a sensitivity of 2 mV/V or 3 mV/V from a load cell. A load cell may be used at 1/2 or 1/3 its rated capacity to allow it to have greater overload capacity. A designer may trade sensitivity for overload capability. For example, using a 2 mV/V load cell at 1/2 capacity yields a 1 mV/V sensitivity, but with greater ruggedness. The lower sensitivity results in less output signal for a given excitation. The usable portion of the output signal may be further reduced because the load cell may be part of a system where the pan weight consumes a good portion of the signal span of the load cell output. For example, a scale designed to weigh 10 Kg (22 lbs.) may have a pan weight which weighs 5 Kg. (11 lbs.) and therefore the pan weight consumes half of the signal span out of the load cell. The application may require protection against high impact, such as when the items being weighed are dropped on the scale. A 2 mV/V load cell may be derated which results in lower output sensitivity (1 mV/V or so) to allow greater impact capacity for the load cell.

Figure 16 illustrates such an application. The signal to measured from the bridge is only 5 mV over the measurement range (the pan weight consumes 5 mV of the load cell span). The offset calibration capability of the CS5516/CS5520 converter can readily remove the offset due to the pan weight. If the converter was configured to measure the 5 mV signal without the additional buffer amplifier, the 5 mV signal would only use part of the converter's span. For example, if the VREF voltage is reduced to 2.0 V and the PGA gain inside the converter is set to 8, the input span expected by the converter would be 2.0/(25 X 8) = 10 mV. To calibrate the converter with only a 5 mV signal would force the gain register to a value outside the recommended range (1.2 to 0.8). This situation can be overcome by using an external buffer amplifier made up of two OP-27 op amps. The VREF voltage for the converter is set to 3.33 V by using three equal resistors for R1, R2, and R3. The PGA gain is set to 1 which makes the input sensitivity at the AIN pins of the converter to be 3.33/(25 X 1) = 133 mV. The buffer amplifies the usable portion of the load cell output signal (5 mV) by a gain of 26 to yield an input to the converter of 130 mV. Stability of the gain resistors is important but tight initial tolerance is not needed as the gain calibration feature of the CS5516/CS5520 can accommodate up to ± 20% gain scaling. AC excitation removes the offset of the OP-27s.

The circuit is operated with the load cell excited with a 1 kHz bridge drive frequency. When operating in bipolar mode, the CS5516 converter will yield about 27,000 noise-free counts over

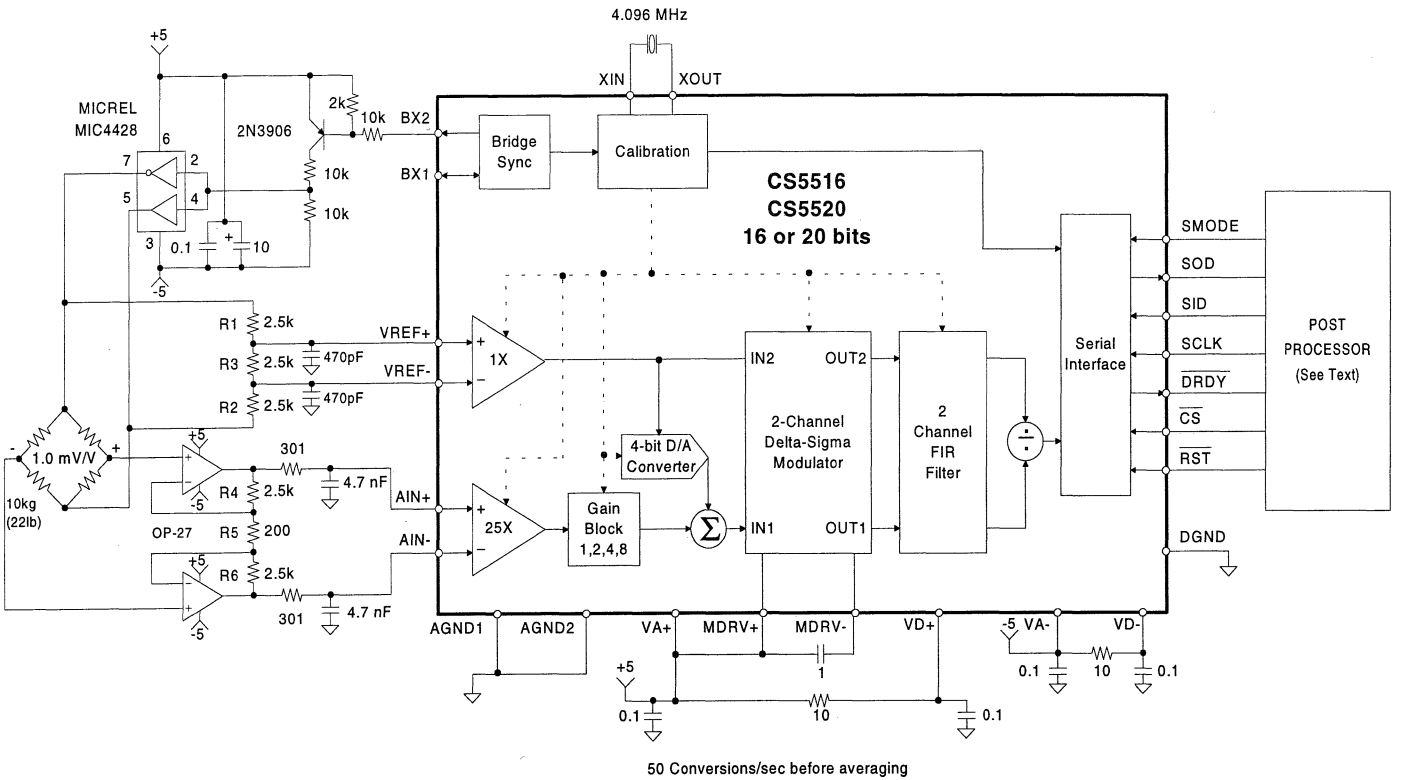


Figure 16. CS5516 or CS5520 and a 1 mV/V AC-Excited Load Cell.

the 5 mV span at a fifty samples per second update rate. The CS5520 should be used if higher resolution is desired at the 50 Hz update rate. Averaging 25 samples will yield an output with an effective 135,000 noise-free counts at two updates per second; this on a 5 mV signal span. The AIN ratiometric calibration register inside the converter can be used to add or subtract offset from the signal and give some counts for zero weight underflow (if used in unipolar mode) or some counts for full scale overrange (if bipolar mode is used). Averaging as many as fifty output words may be desirable in some applications where mechanical vibration is a problem.

CS5520 and an AC-Excited 1.9 mV/V Weigh Platform

Figure 17 illustrates another very high resolution digitizer. A GSE model 4444 "floating beam" platform is used as the weigh bridge. The model 4444 has a full scale capacity of 100 pounds and a sensitivity of 1.9 mV/V. The full-scale output signal from the bridge is (1.9 mV/V) X 9.5 volts excitation or about 18 mV. The 18 mV output signal is amplified by two LT1115 amplifiers configured as a high input impedance buffer amplifier with a fixed gain of 8. When the 18 mV signal is amplified by 8 it yields an input signal to the converter slightly above the nominal value determined by the voltage reference. The calibration features of the CS5520 enable it to accommodate input spans which are as much as 20 % above or 20 % below the nominal value set by the reference voltage. Vishay resistors (R4-R6) are used in the buffer amplifier to maintain a stable gain over temperature. The LT1115 was chosen for its low noise while sustaining a loop gain greater than one million. With a X8 closed loop gain, an open loop gain of 138 dB must be maintained. The operational amplifier must maintain its high open loop gain with reduced supply voltages (±5 V) and with environmental temperature changes. A loop gain greater than one million ensures that gain stability will be dictated by the gain-setting resistors and not by limited loop gain. Offset voltage, offset drift, bias current, and bias current drift are unimportant when ac excitation is used as these errors are modulated out-of-band and filtered out by the digital filter inside the CS5520. Thermal noise at the excitation frequency remains as the limitation to achieving high dynamic range. Although the LT1115 is a very low noise amplifier, the noise in the digitizer circuit is actually dominated by noise referred to the buffer amplifier's input from the A/D. (Note that a lower cost amplifier such as the LT1007 can be used with only a minor increase (5%) in peak-to-peak noise). The effects of the thermal noise can be reduced by averaging output conversion words. With the digitizer using the LT1115s for optimum performance, you can capture output conversion words from the digitizer and examine the noise content in the 50 Hz conversion words. You should capture at least 1000 conversion words from the CS5520 to have a large enough sample to minimize statistical uncertainty. The input to the digitizer should be held at a stable value while the conversion words are captured. Once the samples are captured, a frequency distribution of the samples is computed and plotted. Spreadsheets such as Lotus or Quattro can be used to compute and plot the frequency distribution of the data. Figure 18 illustrates the histogram of 1000 50 Hz output samples from the digitizer of Figure 17. The histogram illustrates that the 50 Hz output words from the converter have a peak-to-peak noise amplitude which is less than 6 LSBs (least significant bits) 99% of the time. The noise in the output codes has a Gaussian characteristic and therefore averaging can be used to reduce its value. Averaging samples which include Gaussian noise will reduce the noise amplitude in proportion to the square root of the number of samples which are averaged together. The post processor computes an average of 50 CS5520 output words to yield a post-filtered output word

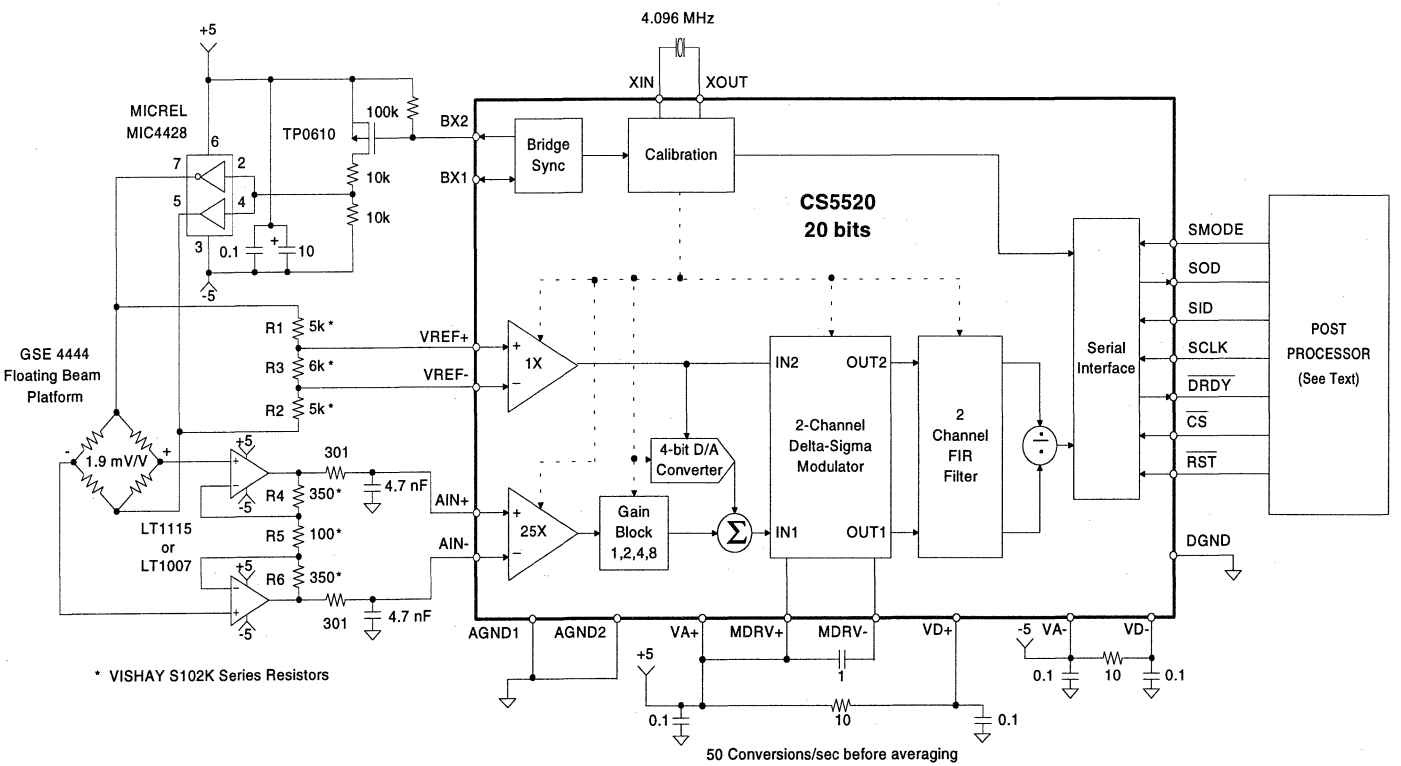


Figure 17. CS5520 and an AC-Excited 1.9 mV/V Weigh Platform.

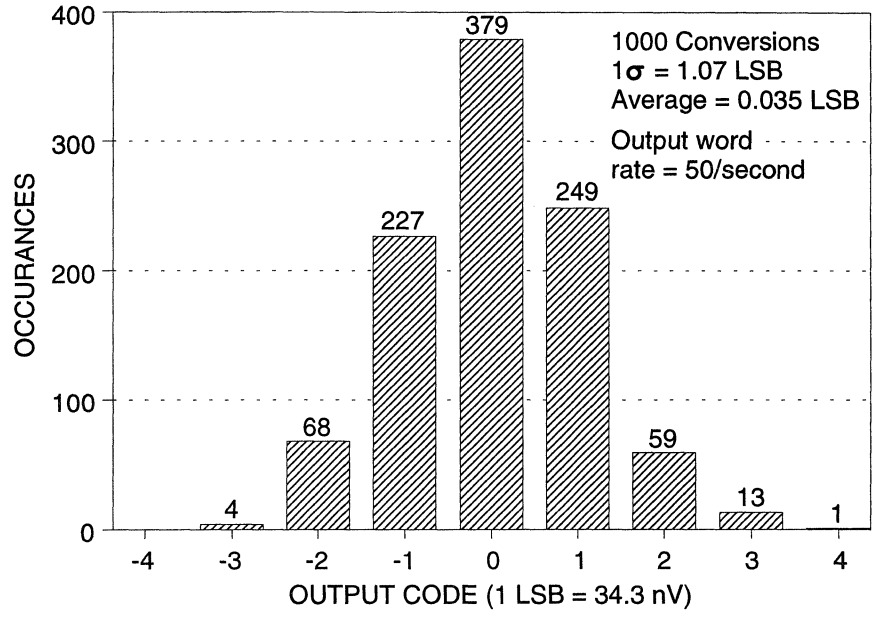


Figure 18. Noise Histogram of 1000 Conversions.

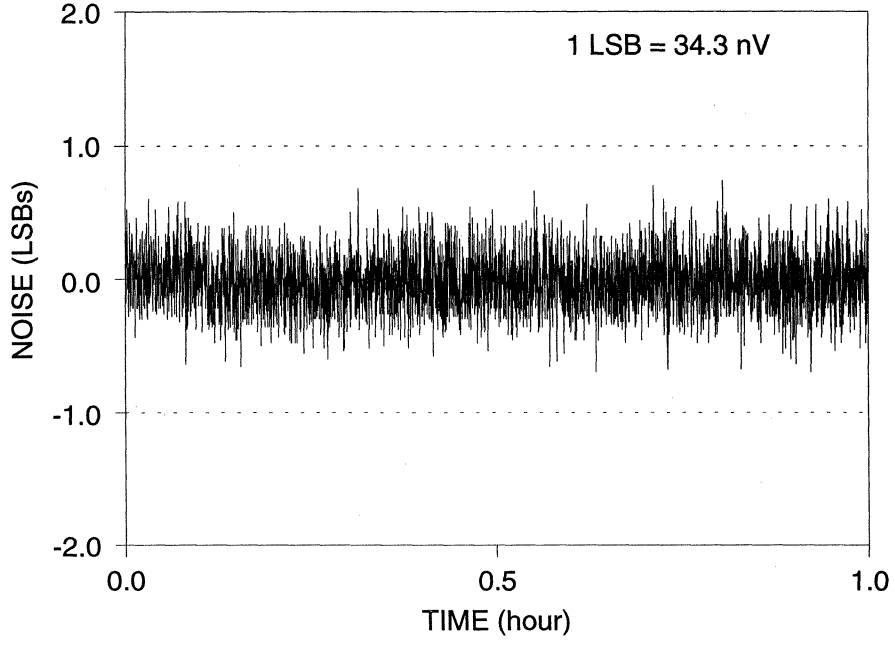


Figure 19. Digitizer Stability Over One Hour.

rate of 1/second. Averaging 50 words reduces the noise by $\sqrt{50}$, or by a factor of 7.07. Since the standard deviation, or rms value of the noise illustrated in Figure 18 is 1.07 LSB, the rms output noise in the post-filtered samples will be 1.07/7.07 = 0.151 LSB rms. You can use the rule of thumb that peak to peak noise is approximately 6 to 6.6 times greater than the rms value to predict the peak-to-peak noise in the post-processed output words. This results in a peak- to-peak noise in the post-filtered output words of less than ±1 LSB for greater than 99.9% of the post-filtered output words.

To illustrate the dc stability and noise of the post-filtered output words over time, the 1 Hz post-filtered output words were collected for a period of one hour. Note that for this test the input to the bridge amplifier was removed from the load cell and tied to ground through two 350 ohm resistors. This eliminates the load cell's sensitivity to vibration when studying the digitizer input noise characteristics.

Figure 19 illustrates the peak-to-peak noise of the digitizer over a one hour period. The plot indicates that the drift and noise are less than ±1 LSB for more than 99.9% of the output samples over the hour long period. This is superb performance and illustrates the benefit of synchronous detection. Figure 18 and Figure 19 indicate that the 50 Hz output data from the converter can averaged to yield a 1 Hz update rate which is stable to 1 count in ±524,000 when the converter is set up for bipolar mode. The CS5520 includes a DAC and a ratiometric offset register which can be used to offset the span in a negative direction by 500,000 counts. This allows the weigh scale to have 24,000 counts of underrange to accommodate any zero drift or creep in the load cell. The measurement span for the 18 mV load cell output would be over 524,287 counts, but above this would be another 500,000 counts which would allow the digitizer to accurately measure overranged weights. In this configuration the digitizer can accurately digitize an overrange signal, even up to 195% of full scale.

The GSE 4444 platform has mechanical stops which activate at approximately 120% of capacity, so the synchronous detection weigher will yield a noise-free 19-bit measurement, with a 20% overrange capacity. If the digitizer was used with a tension-compression load cell such as the BLH Electronics model LPT, the digitizer would yield better than ±500,000 noise-free counts.

Digitizer Noise And Averaging

As illustrated in the previous example circuit, it is good practice to evaluate the performance of a prototype digitizer. While many measures of performance should be investigated (linearity, stability over temperature, etc.), one of the primary factors which limits measurement resolution is noise in the digitizer circuit itself.

Investigating the noise performance of the digitizer should begin in the design phase. Analysis should yield an estimate of the amount of noise in the circuit. This discussion will not focus on the analysis but will instead be limited to evaluating the noise in the digitizer circuit.

One simple method of evaluating digitizer noise is to "ground" the input and collect enough samples to evaluate the noise statistically. "Grounding" the input involves connecting the signal + and signal - leads of the digitizer input amplifier to a quiet node which has a voltage equivalent to the common mode output of the bridge to be measured. In a system with load cell excitation of +5 V and -5 V the inputs can be tied to ground. If the load cell is excited with a single supply (for example, +5 V or +10 V), a quiet source with a common mode voltage compatible with the input of the amplifier should be generated. For example, if the circuit runs on

a single +5 V supply, use two 100 ohm resistors connected in series between +5 V and ground. Then connect the input of the digitizer circuit to the 2.5 V node of the resistor pair. While a load cell simulator may be used in many circumstances, this can be a source of some problems. Some simulators exhibit 1/f noise which can adversely affect the data output from a high resolution digitizer. And some simulators may not work well with the circuits which use ac-excitation. This is because some simulators use switches which rectify the ac excitation signal; therefore the actual signal to be measured is corrupted. This can result in greater noise than expected as well as a dc offset error.

The biggest difficulty in evaluating the noise performance of a circuit is that some means of getting the data out of the digitizer and into a computer must be designed into the circuit. For the CS5504/5/6/7/8/9 devices this can be accomplished by making the SCLK, SDATA and $\overline{\text{DRDY}}$ signals available on a header. The CDBCAPTURE system from Crystal has a standard 10 pin (two rows of 5 pins) stake header which can interface to the CS5504/5/6/7/8/9 products and capture data from these converters. Alternatively, a designer may include some other type of interface in his system to port data to a PC-compatible computer via the serial or parallel port.

Once an interface is available, it is a matter collecting enough conversion words to perform meaningful statistical analysis on the data. The CDBCAPTURE system enables the user to capture data from the CS5504/5/6/7/8/9 and to produce noise histograms. The CS5516 and CS5520 are not supported with the CDBCAPTURE system, but the CDB5516 or CDB5520 evaluation boards can be configured to collect data from these chips. Once data has been collected into a file on a computer, spreadsheets such as Quattro, Lotus, or Excel can be used to analyze the data using a frequency distribution function and statistical functions. The data should also be plotted as shown in Figure 18 to give the user an indication that the data actually follows a Gaussian (Normal) distribution. Thermal noise will have a "bell-shaped" histogram. If the data words represent thermal noise, one standard deviation is equivalent to the rms noise; while 99.9% of all the data should fall within ± 3.3 standard deviations of the mean. Therefore the peak-to-peak noise is approximately 6.6 times the rms noise. When performing statistical analysis on a digitizer's output, at least 500 to 1000 conversion words should be included to lower statistical uncertainty to an acceptable level.

Once the rms noise is known (by calculating the standard deviation of the data set), averaging can be used to improve system resolution if it has been confirmed that the noise follows a Gaussian distribution. Data may not follow a Gaussian distribution because it includes interference due to dc-dc converters or to clock coupling which is picked-up by the sensitive analog circuitry. In this case averaging output words may be deceptive. Averaging will reduce the peak-to-peak noise but the mean can be adversely affected by the interference which is included with the signal.

One additional noise test is to measure noise over the entire input span of the converter. If noise increases with higher signal amplitudes, it suggests the voltage reference input to the converter is excessively noisy.

Aliasing Considerations

The circuits depicted in figures 5, 6, 7, 9, 10, 11 and 12 use the CS5504/5/6/7/8/9 as a sampling converter whose input is not bandlimited. This is acceptable if the bridge output signal is a static (dc) signal. If the bridge output includes ac signals with frequencies above the effective nyquist rate of the sampler, aliasing may occur. This can degrade performance.

Conclusion

The circuits in this application note were designed, constructed, and tested with the intent of illustrating a wide variety of bridge digitizer solutions. The circuits demonstrate various power supply arrangements and various levels of measurement resolution; all with the intent of helping designers understand the flexibility of the A/D converters which have been used.

Application Note

CS5516 and CS5520: Answers to Application Questions

by
Jerome Johnston

What determines the input span for the converter?

The input span of the CS5516/CS5520 AIN input signal is determined by a combination of the instrumentation amplifier gain (X25), the programmable amplifier gain setting (1,2,4 or 8), and the magnitude of the voltage between the VREF+ and VREF- pins. The voltage into the VREF pins can range from 2.0 to 3.8 volts and is determined by the resistor divider ratio selection of the resistor network which divides down the bridge excitation voltage. The CDB5516 and CDB5520 evaluation boards come with resistors which divide the excitation supply (nominally 10 volts total) down to 2.5 volts between the VREF+ and VREF- input pins. This 2.5 volt reference input is divided by the PGA gain setting and by the X25 instrumentation amplifier gain to determine the nominal full scale input span to the converter. For example, if the PGA gain is set for a gain of 8, then the input span to the instrumentation amplifier will be 2.5 volts (VREF+ - VREF-) divided by 8 X 25, or 2.5/(200) = 12.5 mV nominal in unipolar mode, or ± 12.5 mV nominal in bipolar mode. The specified calibration range is ± 20 % of nominal, therefore the device can be gain calibrated to handle a full scale input from a low of 10 mV (20% below 12.5 mV) or to a high of 15 mV (20% greater than the 12.5 mV nominal). To modify the input span, the user can either change the PGA gain setting or modify the resistor divider ratio on the bridge sense voltage which determines the VREF input voltage.

What happens if the full scale span is greater or less than the nominal full scale span by more than ± 20 %?

The calibration range of the gain register spans from 2^{-23} to 2.0 in decimal, and the converter can calibrate with inputs as great as ± 50% of the nominal value, but missing codes can occur in the output transfer function if the calibration range is extended. The intent of the ± 20 % calibration range specification is to insure proper code computation with no missing codes in the output transfer function, and that the analog signal does not saturate any portion of the signal path inside the device (see later discussion on the block diagram model of the converter).

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX 445-7581

The resistor values shown in the data sheet for the excitation divider are too low in value and may cause gain error due to excessive loading of the excitation signal when used with remote transducers. How large can these resistors be?

The original data sheet showed the VREF divider resistors as 750 and 500 ohms. The current data sheet indicates these as 7500 and 5000 ohms if the associated filter capacitor is reduced to 470 pF. The AIN and VREF inputs to the converter are both switched-capacitor inputs. The RC-time constant associated with the inputs on the VREF+ and VREF- pins, and on the AIN+ and AIN- pins, should be such that the capacitor sampler settles to full accuracy in a sampling period. Figure 1 illustrates a simplified model of each of the pins for VREF+, VREF-, AIN+ and AIN-. The input has a dynamic current requirement based upon charging a sampling capacitor. The input current is a function of the sampling capacitor, the sampling clock, and the offset of the buffer. The offset of the buffer will not exceed 25 mV over the -55 to +125°C temperature range. Using this model, one can determine the value of the dynamic current and the effective input resistance. The model can be also be used to compute the errors contributed by external source impedances.

For example, the input current required by the AIN+ pin should be about 52nA plus leakage current when the converter is operated with XIN = 4.096MHz.

$$i_n = V_{os} f c_s = (25mV)(4.096MHz)(0.5pF) = 52nA$$

The application note *Switched-Capacitor A/D Converter Input Structures* explains the input current effects of the sampled capacitor circuit.

Can you provide an example of how the sense lines from a transducer can be buffered to reduce the loading effect of the reference divider resistors?

The sense lines from the bridge can be buffered as shown in figure 2 or figure 3. The drift in the amplifier offset is referenced to the VREF voltage, not to the input span of the converter and therefore will have a negligible effect on gain accuracy.

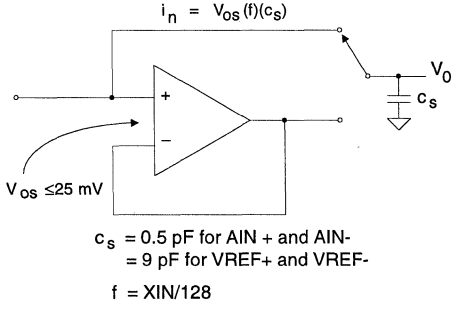


Figure 1. Simplified Model for AIN and VREF Inputs.

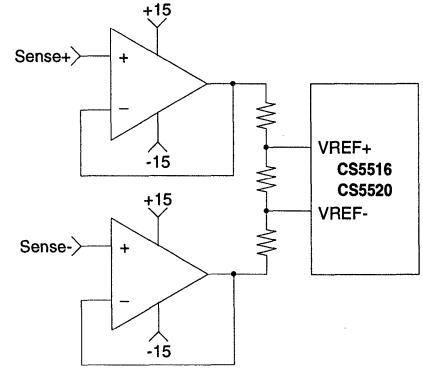


Figure 2. Using Op Amps to Buffer Sense Lines.

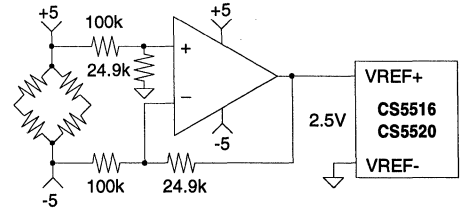


Figure 3. Single Op Amp Used to Buffer Sense Lines.

Explain the operating limitations of the CS5516/CS5520. For example, what happens if the bridge is excited with a single +5 volts rather than ± 5 volts?

Figure 4 illustrates the block diagram of the converter with some notes stating signal limitations at the various stages inside the converter. The instrumentation amplifier inside the CS5516/CS5520 has a differential gain of 25 (the amplifier is shown with a single-ended output in the figure; it actually has a differential output) and a common mode gain of 1. The easiest way to explain its signal limitations is to state that the output of the X25 instrumentation amplifier cannot exceed ± 3.75 volts; the maximum differential input signal must be less than 300 mV - | V_{cm}/12.5| where V_{cm} is the common mode voltage of the input signal. If the bridge is excited with only +5 volts (no -5V) then the common mode input to the instrumentation amplifier is +2.5 volts. So the maximum differential input signal is 300 mV - |2.5/12.5| = 100 mV. The common mode gain of one yields a common mode signal out of the X25 amplifier of 2.5 volts; the differential gain of 25 yields a differential signal out of the X25 amplifier of 2.5 volts differential, that is ± 1.25 volts. The 2.5 volts common mode plus the 1.25 volts differential together are at the limit of +3.75 volts.

The output of the gain block also has a saturation limitation of ± 3.75 volts, but the PGA does not amplify the common mode signal. The differential signal portion of the output of the X25 amplifier is ± 1.25 volts. Since the output of the PGA is limited to ± 3.75 volts maximum, gains of 1 or 2 can be used (if a gain of 2 is used, the gain calibration word will be outside the recommended range). Gains of 4 or 8 cannot be used, for in this example these would exceed the signal range limitation of the gain block output.

The actual input to the modulator is restricted to 5 volts total, that is ± 2.5 volts differential. Again the gain block, the DAC, and the modulator are all shown as single-ended, whereas they are actually fully-differential. The DAC must be used to trim any offset in the signal ensure that the span into the modulator does not exceed the ± 2.5 volts differential span. The DAC can trim up to ± 200 % of the maximum differential signal input into the X25 amplifier.

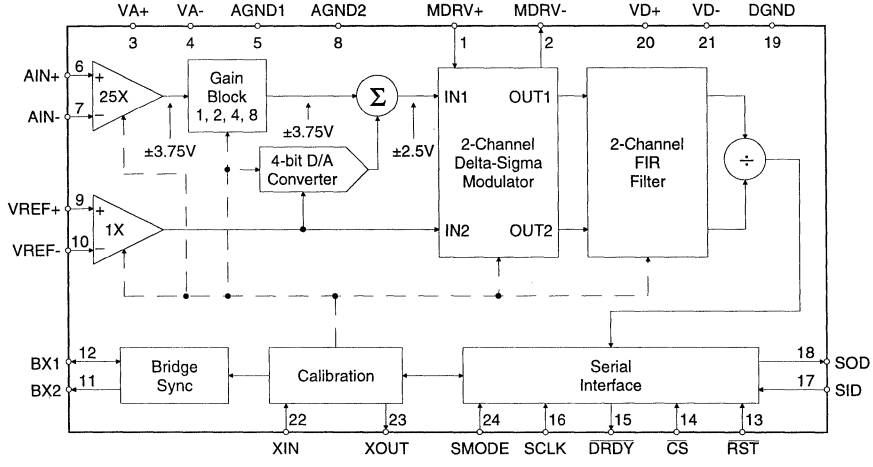


Figure 4. A/D Block Diagram Indicating Signal Path Limitations.

How does the XIN clock frequency affect the filter bandwidth?

The CS5516/CS5520 can be operated with any crystal between 1.0 MHz and 5.0 MHz with corresponding changes in the digital filter. The digital filter inside the converter is optimized to provide a very deep attenuation notch (-140 dB) at 50 Hz when using a 4.096 MHz crystal or a very deep filter notch at 60 Hz when operated from a 4.9152 MHz crystal. The device can be operated at other frequencies and still attain very good rejection (90 dB) attenuation at both 50 and 60 Hz. Figure 5 illustrates the magnitude plot of the digital filter. Note that the entire filter transfer function scales with a change in clock frequency. At frequencies above the first notch frequency, the out-of-band attenuation will be at least 90 dB for frequencies above the filter cut-off but below the modulator sampling frequency (XIN/256).

What is recommended if I need narrower bandwidth than provided by the on-chip digital filter?

The CS5516/CS5520 were designed to give high update rate (50 Hz with XIN = 4.096 MHz) with a 25 Hz usable bandwidth. The filter is designed to settle in less than six output words when the input changes in a transient manner. It is desirable in many weighing applications that the circuit have very low bandwidth (typically 1 to 4 Hz) to eliminate scale resonances and vibration. To accomplish this type of bandwidth with the CS5516/CS5520, the user should average several output words. Averaging 10 output words (XIN = 4.096 MHz) will result in a -3 dB filter bandwidth of about 2.5 Hz. This filtering was not included on the chip because many weigh scale designers prefer to design their own "adaptive" filter which can settle fast when the input signal changes in a transient manner, but implement more attenuation as the signal begins

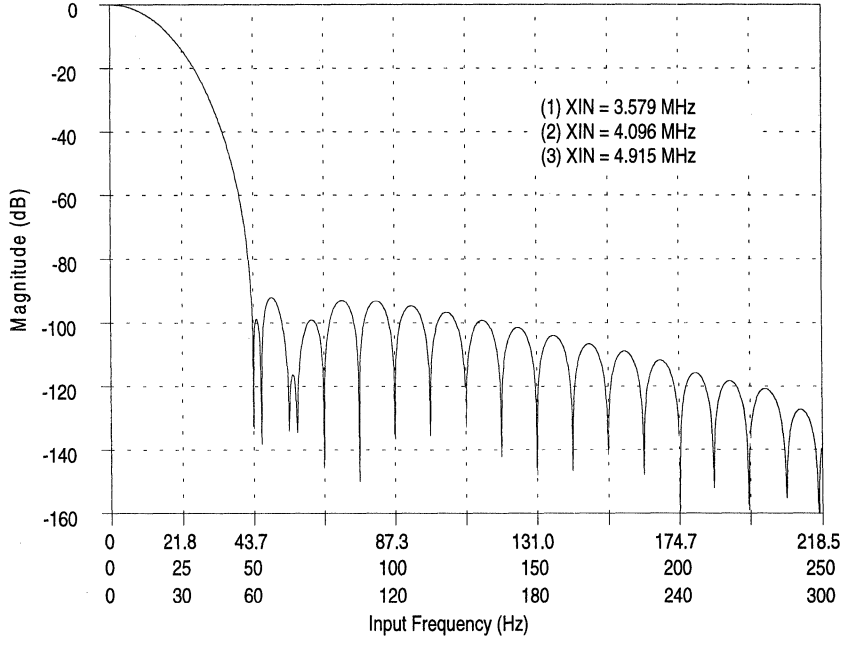


Figure 5. Filter Response at Various XIN Frequencies.

to settle. To accomplish this, use the 50 Hz update directly when the data suggest that the input signal is changing at a rapid rate (weight has just been placed on the scale). Then switch to averaging once the signal has settled to within a specified error band; typically some band slightly greater than the peak-to-peak noise of the signal. The exact requirements of the adaptive filter function will be dictated by the application; particularly the mechanical response of the weighing system.

The CDB5516 and CDB5520 evaluation boards include software which allows the user to read and write all registers in the converters, collect conversion data, perform averaging, save data to a file, and compute the standard deviation (one standard deviation is equivalent to the rms noise for gaussian type noise). The evaluation board may be of assistance in evaluating the amount of averaging to perform in your circuit.

Should I use a series or parallel type crystal?

Either crystal will work. Series or parallel designates the electrical configuration in which the crystal was calibrated. The CS5516/CS5520 converter uses a parallel configuration (Pierce oscillator). If a series crystal is used, it will oscillate reliably but its frequency will be slightly different than that of a parallel cut crystal (typically within 0.03% of the same frequency).

The converter seems to lock up or not respond to calibration instructions. Any suggestions?

When the device or the serial port is reset, the port is waiting for a command. Inside the port, there is a pointer register which counts SCLKs to keep track of whether the information being moved through the port is to be interpreted as a command or as calibration register data. After the converter is reset, the pointer will count the first 8 SCLKs and accept the data bits associated with these as a command. The pointer then counts the next 24 SCLKs and interprets the data bits associated with these as register data. The SCLKs must start low, transition high, and then return low to be counted properly. Problems can arise if the $\overline{CS}$ is released (returned high) before the falling edge of the last SCLK. The pointer will get confused and begin recognizing the bits of the commands words as data bits or vice versa. So watch your SCLKs.

When the CS5516/CS5520 is interfaced to a microcontroller, it is sometimes difficult to discern whether the converter is actually receiving commands. A simple way to assess whether the interface is working properly, is to reset the converter and then to transmit one 88(H) command (read conversion data) to the serial port. Do not attempt to read the data output, instead, use your oscilloscope to see if $\overline{DRDY}$ (pin 15) starts toggling. $\overline{DRDY}$ should start toggling if the interface is working properly.

When the converter is put in the read conversion data mode, it will output a conversion data word to its serial port register every 81,920 XIN clock cycles. Therefore, 81,920 XIN clock cycles elapse between $\overline{DRDY}$ falling, but the user must read the conversion data within 51,000 XIN clock cycles after $\overline{DRDY}$ falls. After the 51,000 XIN period, the converter is using its internal bus to perform calculations and to move data between registers. If a read is attempted during this time, the internal data bus can experience contention, which can cause the bus to lock up.

When reading the conversion data I get all zeroes no matter what the analog signal is. Please explain why.

Check your voltage reference between pins 9 and 10 (VREF+ and VREF-). If this voltage is zero, the converter will compute all zeros for the output conversion data. Remember an A/D converter computes a digital word which

represents the ratio of the input signal to the voltage reference. If the voltage reference is zero the output will be zero.

The conversion data out of the converter changes as the input signal changes, but is never correct. Any suggestions?

When the converter is configured for external bridge excitation, the BX1 input pin determines the phase of the internal detection circuitry for the AIN and the VREF input signals. For external dc excitation, the BX1 pin should be pulled up to +5 volts through a 10 k resistor to insure the proper phase of the input signals.

If ac excitation is used, be certain that the phase of the signals into the VREF and AIN pins is in phase with the BX2 signal. If either of the signals is not in phase with the BX2 signal the converter will not compute correct conversion data.

Is calibration required to use the converter? Must non-ratiometric calibration be performed?

When the CS5516/CS5520 is reset, the registers are set to known values. If the signal to be measured by the converter is within the nominal range, the converter can perform conversions without the need for calibrations. Some users apply their own calibration scheme using software and registers in their microcontroller.

After being reset, the CS5516/CS5520 will convert on the signal being measured. The only limitation of not using the converter's calibration functions is that the errors in the system remain present. This may be acceptable if the errors are insignificant to the measurement or if the errors are removed by some other means, such as software in the user microcontroller.

The CS5516/CS5520 offers a complete set of calibration features; non-ratiometric offset calibration, ratiometric offset calibration, and gain calibration. The converter can perform conversion without any calibration being performed. Just because the calibration feature is available does not mean the feature must be used. The user's application should dictate if calibration should be used to remove specific errors. It may be quite acceptable in a given application to not use the non-ratiometric calibration features of the converter. The user can evaluate the magnitude of the error source and its effects on the resulting conversion data by either analysis or by empirical investigation. The application note *Overcoming Errors in Bridge Measurement* discusses the various error sources and their contribution to the final error in the output data. Often the user can use the CDB5520 evaluation board to investigate these errors. The CDB5520 comes with PC-compatible software which allows the user to perform calibrations and read all of the registers in the converter. Once the calibrations are performed, the magnitudes of the numbers in the registers indicate an estimate of the magnitudes of the errors which have been calibrated.

How often do I need to recalibrate?

To answer this question one must ask: 1) What accuracy is required from the A/D converter? 2) What effects will temperature changes have upon the entire circuit, including components outside the A/D? Once power is applied to the converter, it will take about a minute for the chip to reach thermal equilibrium. It is best if calibration is performed after the chip has reached this stable operating temperature.

A higher accuracy measurement requirement will generally require calibration to occur more often, because, after the initial calibration has been performed, the converter is subject to some drift if the operating temperature changes. Typical offset drift (± 0.005 µV/°C) and gain drift (1 ppm/°C) are given in the data sheet tables. The

observed drift in the application circuit may be considerably greater due to parasitic thermocouple effects and gain drift caused by the limited tempco tracking of the VREF divider resistors. Once an estimate of drift is determined for the entire application circuit (drift will usually be dominated by error sources external to the converter), one can assess how this will affect measurement accuracy as temperature changes. Once the amount of drift is known, it can be determined if a new calibration is required. Using AC-excitation removes the effects of parasitic thermocouples and offset drifts and therefore will require less recalibration as the operating temperature changes.

The CS5516/CS5520 has been subjected to 1000 hour burn-in at 125°C to investigate the effects of aging. The converter was tested with a full scale signal using AC excitation mode with maximum PGA gain and maximum DAC offset. The devices showed drift over the test period of about 10 ppm, but it was inconclusive how much of the drift was attributable to the converter. The laboratory measurement equipment has limited stability over the 1000 hours also (6 1/2 digit voltmeters are only guaranteed to 10-20 ppm drift over a 90 day period at room temperature).

Explain the difference between non-ratiometric and ratiometric.

Load cells are ratiometric devices, meaning that their output signal is proportional to their excitation voltage. For example, if the excitation voltage increases by three per cent, then the output signal from the load cell will also increase by three per cent. A ratiometric offset is an offset, such as the offset of the load cell, which changes proportionally to the load cell excitation voltage. A non-ratiometric offset is one which does not change proportionally with changes in the load cell excitation voltage. The offset of an operational amplifier which amplifies the bridge signal is non-ratiometric; if the bridge excitation changes, the offset does not change in proportion to it. Non-ratiometric offsets become an issue if the magnitude of the bridge excitation voltage changes due to drift.

What do the numbers in the calibration registers actually mean?

There are two non-ratiometric offset calibration registers, one for the AIN input and one for the VREF input; one 4-bit offset trim DAC; one ratiometric offset calibration register for the AIN input; and one gain calibration register. When the calibrations are performed, they should be performed in the following sequence: The non-ratiometric offsets should be calibrated first (if you choose to calibrate them); then the ratiometric offset; followed by gain calibration.

When the non-ratiometric offsets are calibrated, an LSB in the 24-bit digital calibration words represents 2^{-23} proportion of an internally-scaled MDRV (Modulator Differential Reference Voltage). At the MDRV+ and MDRV- pins, the MDRV has a nominal value of 3.75 volts. This voltage is internally scaled to a nominal 2.5 volts for use with the non-ratiometric calibration. The 24-bit calibration word is stored in 2's complement form with one count equal to approximately 300 nV at the input of the internal A/D converter. For the AIN channel this will be scaled down by the gain of the instrumentation amplifier (X25) and the PGA gain. For a PGA gain = 1, one count will represent about 12 nV. Non-ratiometric offset to be calibrated by the VREF channel cannot exceed approximately ± 2.5 volts. Non-ratiometric offset to be calibrated by the AIN channel cannot exceed approximately ± 2.5 volts divided by the channel gain. With a PGA gain = 1, the maximum non-ratiometric offset which can be calibrated on the AIN channel cannot exceed approximately ± 100 mV.

When the ratiometric offset is calibrated, the 4-bit DAC coarsely trims offset from the analog

signal. The remaining ratiometric offset in the AIN channel is trimmed after the signal is converted using the digital word from the ratiometric offset register. The DAC allows the user to add or subtract offset up to 200 per cent of the nominal input signal. The AIN ratiometric offset register can be used to add or subtract offset equal to the nominal full scale input signal into the X25 amplifier. An LSB in the ratiometric offset register represents 2^{-23} proportion of the voltage input across the VREF+ and VREF- pins at the internal input to the AIN channel A/D converter. This will be scaled down by the AIN channel gain when calculated relative to the instrumentation amplifier input. For example, with a VREF = 2.5 V, and a PGA gain = 1, one count of the ratiometric offset register would represent about 12 nV at the instrumentation amplifier input. The proportion remains ratiometric even if the VREF voltage should change. The 24-bit register content is stored in 2's complement form.

All calibration registers can be read or written by the user. This allows the contents of the calibration registers to be read and stored in EEprom; or to be modified by the user. This is useful in the case of the ratiometric offset register as it allows the user to add or subtract small offsets from the transfer function after the calibration has been performed. This allows the user to shift the transfer function to allow for load cell creep or load cell zero shifting "below zero" when the converter is measuring in unipolar mode. It also allows the gain register to be modified as will be discussed in the next question.

The gain calibration is performed last. The contents of the gain register spans from 2^{-23} to 2. After gain calibration has been performed, the numeric value in the gain register should not exceed the range of 0.8 to 1.2 (decimal)[666666H to 999999H]. The gain calibration range is ± 20 % of the nominal value of 1.0. The nominal value of 1.0 is for an input span dictated by the VREF voltage, the PGA gain and the X25 instrumentation gain (see the previous discussion on setting the input span to the converter). The converter may operate, subject to internal amplifier saturation (discussed later) with gain slope factors from 0.5 to 2.0 (decimal) but when the slope exceeds 1.2 the converter output code computation may lack adequate resolution, giving results which may include missing codes.

How can the gain be calibrated if a full scale signal is not available?

Some scale manufacturers desire to calibrate gain using some weight other than full scale. For example, a truck scale may have a capacity of 100,000 lbs (45,400 Kg.). Who wants to carry around that much weight to calibrate the scale? Calibrating the scale with 10 per cent of full scale capacity isn't a simple task.

The CS5516 or CS5520 can be gain calibrated with some input signal other than full scale. Assume one wants to calibrate using an input which is 10 per cent of full scale capacity. The normal gain calibration procedure cannot be used. Instead, the user can increment or decrement the gain register until the converter arrives at the correct value, or the correction factor can be calculated. For example, when the converter is reset, the gain calibration word is 1.0. If a weight representing ten per cent of full scale reads three per cent less than it should, the value in the gain register can be scaled up by three per cent. Gain accuracy can be improved if output words are averaged while using this technique.

Caution is advised in using a calibration weight less than full scale. If the transfer function of the the load cell happens to have a major nonlinearity at the point at which calibration is being performed, this will cause the rest of the transfer function to be incorrect. Be certain you

understand the particular linearity characteristics of the load cell you are using.

The calibration word is not exactly the same each time I calibrate with the same input conditions. Why is this?

The calibration word is calculated using output words from the converter which include the thermal noise. Therefore the resulting calibration words can be affected by this peak-to-peak noise. This can be overcome by calibrating several times in succession using the same input conditions and averaging the results with an external microcontroller. The averaged answer is then written back into the calibration register. The calibration word will typically have the same magnitude of peak-to-peak noise that is seen in the output conversion data. By investigating the magnitude of this noise, one can determine how many calibration words to be averaged. Remember that Gaussian noise is reduced by the $\sqrt{N}$ when N samples are averaged.

Is a different calibration required for each PGA gain setting?

The PGA gain steps will have some tracking error, typically 1 per cent or so. The PGA actually uses different capacitor values to set the PGA gain. These capacitors have a ratio error due to processing which determines the gain error of the PGA gain steps. Calibrations of non-ratiometric offset for AIN, ratiometric offset, and gain should be performed with the PGA gain (1, 2, 4, or 8) set to the range which is going to be used in the application. If the PGA is going to be changed during measurements, calibration words should be performed and saved in EEprom for each PGA gain setting.

Therefore, to achieve good gain tracking when the PGA gain is changed, a gain calibration should be performed with each PGA gain selection. The following calibration method is preferred by some designers as it requires only one user adjustment for the input signal. Assume the converter is being gain calibrated with a 2.5 volt VREF. With the PGA gain set to 8, the full-scale input would be 12.5 mV. Input the signal intended for full scale (12.5 mV ± 20%) and calibrate the gain with the PGA set to 8. Save the gain calibration word. Then without changing the input signal, change the PGA gain to 4. Ideally the converter should output a half scale code. The actual output code may be lower or higher. Increment or decrement the gain register until the resulting conversion code is half scale. Calculate the offset required to modify the gain register when changing the PGA from a gain of 8 to a gain of 4. Save this offset word and use it to modify to gain register when PGA gain is changed from 8 to 4. Next, reload the gain register with the calibration word determined with the PGA gain of 8 and change the PGA gain to 2. The converter should output a code of one quarter of full scale. Increment or decrement the gain register to yield the correct output code. Calculate the offset required to modify the gain register when the PGA is switched from 8 to 2. Save this offset for future use. Reload the gain register with the gain word for a PGA gain of 8 and change the PGA gain to 1. This time the output code should be one eighth of full scale. Modify the gain register and save the offset as done in the previous calibration steps. While this example calls for saving the register offsets, one can choose to save the gain words themselves. This will depend upon the algorithm you choose to use in your microcontroller. The advantage of this calibration method is that it removes the error associated with the user adjusting the input signal to a new value. The method can be very accurate if some averaging of the output conversion words is performed during the calibration sequence as this removes uncertainty due to the thermal noise in the system.

Why is ac excitation better than dc excitation?

The CS5516/CS5520 converters are designed for bridge transducer signals. Bridge transducers output low level signals which can be adversely affected by amplifier offsets, amplifier bias current effects, noise (both thermal and 1/f), and parasitic thermocouples. Parasitic thermocouples exist in normal circuit wiring. Junctions such as tin-lead solder and copper PC board trace can introduce thermocouple effects of 3-4 µV/°C if thermal gradients exist across the circuit. In a dc-excited bridge circuit, there is no way to discern between the actual low level signal being generated by the bridge and the error signals introduced by amplifier offsets, amplifier bias current effects, 1/f noise, and parasitic thermocouples unless some method is used to separate the actual signal from these error sources. One method of separating the signal from the error sources is to use an ac-excited bridge system.

When the CS5516/CS5520 are configured for ac-excited bridge measurement, the converter measures the signal which is of the same phase and frequency as the excitation frequency. The CS5516/CS5520 converter actually use a polarity-switched square wave whose frequency is normally a sub-multiple of the XIN clock frequency to the converter.

Figure 6 illustrates the benefits of ac excitation versus dc excitation. In one of the plots in Figure 6, the CS5520 converter was configured to measure a bipolar signal with an input span of ± 12.5 mV with dc excitation. Conversions were performed with a zero input signal from the bridge and data was collected for a one hour time interval. One LSB (least significant bit) of the CS5520 was equivalent to about 25 nanovolts. The data collected indicates that over the one hour period the average value of the data drifted as much as 1.3 microvolt, or about 50 counts. The CDB5520 evaluation board was used for collecting the data and the drift was attributed to parasitic thermocouples in the components or the wiring of the board. The board was used in open air and the data illustrates the effects of thermal gradients introduced by the cycling of the air conditioner system. The second plot in Figure 6 illustrates the stability of the conversion system when the converter is set up for the same operating

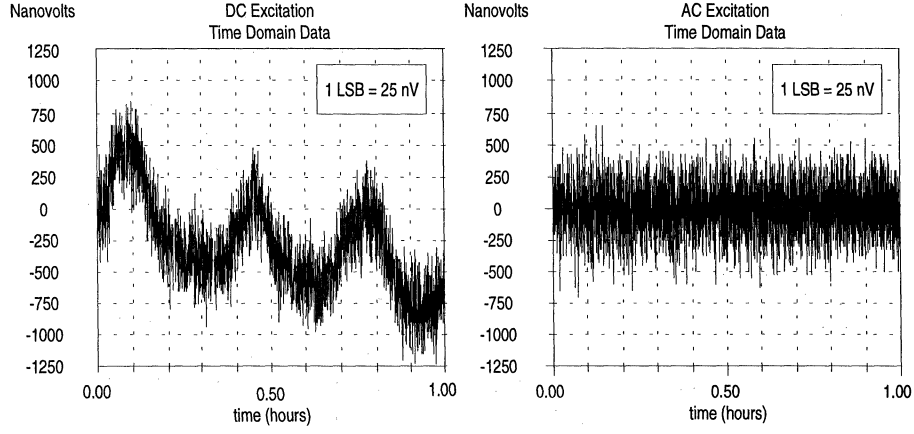


Figure 6. Stability Over One Hour using DC and AC Excitation.

conditions, but with ac bridge excitation. The plot illustrates the normal thermal noise of the circuit but the average value remains stable over time.

Are there disadvantages to ac-excitation?

The ac-excited bridge circuit must include some type of driver circuitry which can add some additional cost (The combination of a transistor and the MIC4428 is below $3.00 at 100 piece quantities (1994)). Another disadvantage is that service technicians must be educated about ac excitation; that troubleshooting with a dc meter isn't adequate; although the system can be configured for dc operation for basic troubleshooting tasks.

One must be cautious when using ac-excitation if the load cell uses a cable with a large capacitance. Since the converter uses a switched square wave to excite the bridge, the cable capacitance may adversely affect measurement accuracy if the square wave excitation signal does not settle adequately. The converter is designed to begin sampling the square wave signal at a time interval of 64 XIN clock cycles after the excitation signal changes polarity. The square wave should have settled to within ± 5% of its final value in the 64 XIN clock cycle period to ensure measurement accuracy. Note that this settling requirement must also be met by any filtering elements used in front of the converter on the AIN or the VREF signal inputs.

For very long cables, the CS5516/CS5520 can be configured for a switched bridge measurement configuration by setting the converter for dc excitation mode to measure bipolar signals and having the external microcontroller control the bridge polarity. When the polarity of the bridge excitation is changed, the external microcontroller then waits for at least six output words (the CS5516/CS5520 can take up to six filter cycles to settle whenever the input signal changes in a transient manner) from the converter before taking a final reading. By averaging a reading for one polarity of excitation with a reading with the opposite polarity of bridge excitation, the errors due to parasitic thermocouples can be averaged out. If this configuration is used, the normal calibration sequence for offset and gain would have to be modified. An algorithm to calibrate the offset and gain registers could be developed by the user.

BX1 and BX2 outputs are used for ac excitation. What logic level is output from these pins if the ac excitation is stopped? What are the logic outputs of BX1 and BX2 if the converter is put to sleep?

Internal excitation with the F1-F0 bits of the configuration register equal 0 sets BX2 = +5V, BX1 = 0V. If external excitation is used, BX1 will always control the BX2 output. In sleep BX1 = +5V and BX2 = 0V.

Explain the noise performance of the CS5516/CS5520.

The data sheet gives a typical noise specification for the CS5516/CS5520 at each gain when operating in bipolar mode with a VREF voltage of 2.5 volts. When operating in this mode one LSB of the converter is equal to (2 X 2.5)/(Gain X 2^{20}). For example, with a gain of 200 (8 X25) the noise specification is 150 nV rms. With a gain of 200, one LSB in the CS5520 converter (bipolar mode) is equivalent to about 23.8 nV, so the rms noise would be equivalent to 150 nV/23.8 nV or 6.3 counts. A rule of thumb says that peak-to-peak noise is 6 to 6.6 times greater than rms, so the peak-to-peak noise would be about 38 to 41 counts when operating in this mode. This calculation can be verified by capturing 1000 (the statistical uncertainty is reduced if a large number of samples are collected) conversion words into a file and computing the standard deviation of the data.

One standard deviation is equivalent to the rms noise if the data follows a Normal or Gaussian distribution. It is useful to plot a histogram of the data to verify that it has a Gaussian characteristic. The noise in the converter itself is Gaussian so the user can average output words to reduce the effects of noise. Averaging N samples reduces the noise in the averaged output words by the $\sqrt{N}$.

The CDB5516 and CDB5520 evaluation boards include software which allows the user to read and write all registers in the converters, collect conversion data, perform averaging, save data to a file, and compute the standard deviation of a group of output conversion words. The evaluation board and its software may be able to assist in evaluating the noise of the converter in your system.

My application circuit appears to have an excessive amount of noise. How do I determine the cause?

If the results from your circuit exceed the expected value (usually a computed estimate for the circuit based on sound engineering analysis), some steps can be taken to help determine the source of the excess noise. The first step is to remove the load cell from the circuit and ground the input signal leads as shown in figure 7. With the input grounded, collect at least 1000 samples (to remove statistical uncertainty) and perform a histogram analysis on the data. Figure 8 illustrates an example of a noise histogram which has been performed on data using Quattro which shows the "shape" of the data (Gaussian). Calculate the standard deviation of the data (one standard deviation is equivalent to the rms noise for gaussian type noise). The load cell has been disconnected so that the noise performance of the digitizer can be assessed by itself. If the converter is "quiet" with the input grounded, it suggest that noise is getting onto the cable or that the load cell is possibly sensitive to vibration. If the noise is still too high, try grounding the AIN+ and AIN- pins of the converter right at the converter itself and perform the test again. The input components to the converter may be picking up high frequency radiated noise from some digital circuitry on the board.

If the noise histogram plot does not appear to be Gaussian, suspect radiated interference from digital circuitry or from a dc-dc converter.

When testing for noise, be sure to ground the input signal leads to the signal ground; do NOT use a load cell simulator. See the next item.

Is a load cell simulator a good test tool for evaluating the CS5516 and CS5520?

It is helpful to know what limitations can exist if you are using a load cell simulator in place of an actual load cell. If you are trying to use the CS5520 to digitize a 10 to 20 mV signal to 20 bits, the output codes can drift around due to what is apparently 1/f noise in the simulator. A way to test this is to use two 348 ohm 1% metal film resistors tied from the AIN+ and AIN- inputs of the CS5520 to the signal ground. Examine to see if the drift remains when the simulator is disconnected and the signal source is signal ground.

A second problem which can be encountered when using a load cell simulator is that some simulators will not work well with AC excitation. It seems that the switch contacts in some simulators are made of materials which rectify the signal and therefore cause errors in the bridge output signal. Use a totally resistive bridge with no switches if you encounter this type of problem.

What benefit does an evaluation board offer?

The CDB5516 and CDB5520 evaluation boards save time and money over prototyping. The

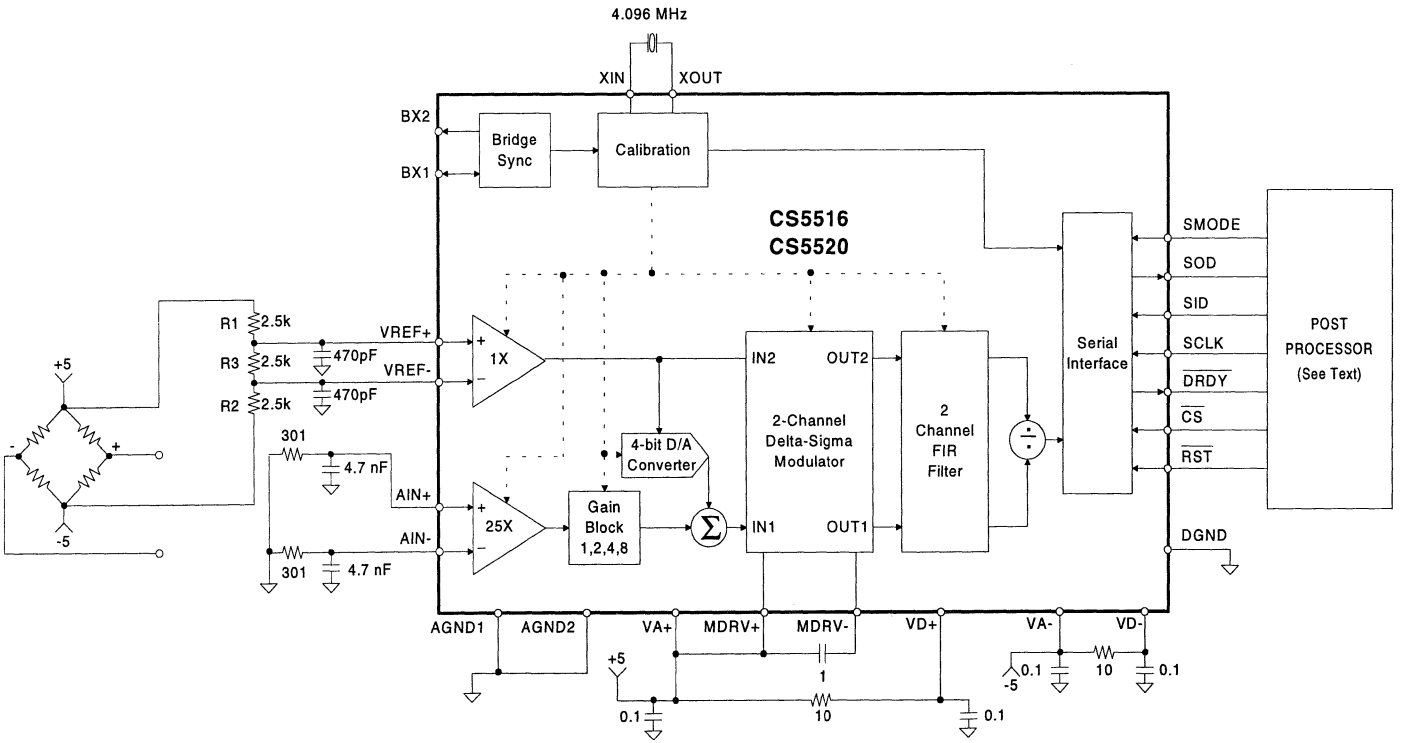


Figure 7. Ground Input Leads for Troubleshooting Noise.

preassembled and tested boards come with a serial cable to connect to a PC-compatible computer and include software which allows the user to manipulate the registers inside the CS5516 or CS5520. Calibrations can be performed and conversion data can be collected. The evaluation boards support dc or ac excitation of a bridge transducer (not supplied) which is connected to a terminal block on the circuit board.

The CDB5520 includes a CS5520; the CDB5516 includes a CS5516. Other than the converter which is socketed on the board, the evaluation boards are identical. Therefore, the board can be used to evaluate either converter chip. The software includes a menu selection for the type of converter (CS5516 or CS5520) to be tested.

The data sheet states that the converter uses about 3 mA of current. Mine draws about 30 mA. Any explanation for this?

Check your BX1 pin. One of the schematics in the first data sheet had this pin tied to +5 volts directly. It must be pulled up through a resistor as the BX1 pin has a low logic output when the converter first gets reset. If the circuit is configured for external dc excitation mode, cut the trace and use internal dc excitation; or pull up the pin with a resistor pull-up.

The MIC4428 and MIC4425 devices are used in applications with the CS5516/CS5520. What is the address of the company that makes these devices?

Micrel, Inc., 1849 Fortune Drive, San Jose, CA, 95131. (408) 944-0800, FAX (408) 944-0970.

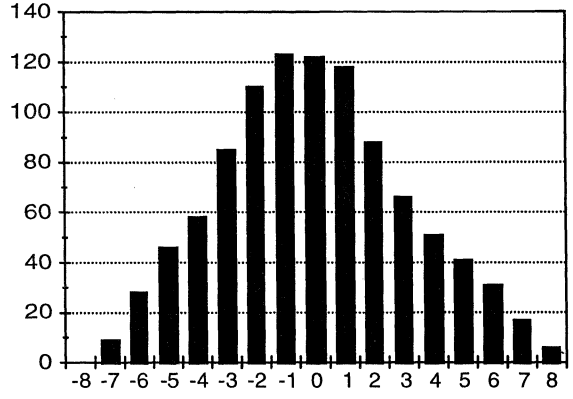


Figure 8. Example Noise Histogram for CS5520 Output Codecs VREF = 2.5V, PGA = 4, Bipolar mode.

Precision Temperature Measurement using RTDs (Resistance Temperature Detectors) with the CS5516 and CS5520 Bridge Transducer A/D Converters

by
Jerome Johnston

The CS5516/CS5520 bridge-measurement A/D converters can be configured for precise measurement of resistance using a ratiometric resistance measurement technique.

DC-Excited RTD Digitizer

Figure 1 illustrates the CS5516 16-bit A/D converter used as a digitizer for a platinum RTD. The RTD is excited with a 250 µA current generated by the LM334 programmable current source. The 1N457 diode offers some first order temperature compensation to the current source, but the exact value and temperature coefficient of the current source isn't important because the current is used in a ratiometric measurement configuration.

The current is used to develop both the voltage reference (2.5 V across R1) for the A/D and the signal voltage across the RTD. The initial accuracy of the reference resistor is not critical because the CS5516 offers gain calibration capability, but reference resistor R1 must have low temperature coefficient. The temperature drift of the reference resistor will affect the accuracy of the ratiometric measurement. A Vishay S102K resistor is recommended for the reference resistor to achieve optimal measurement accuracy.

The offset and gain accuracy of the circuit are ensured by self-calibration. Offset is calibrated with 0Ω connected in place of the RTD. Full scale is then calibrated with a known resistance whose value is ideally 400.00Ω connected in place of the RTD. Once the A/D is calibrated, the RTD resistance is measured as a proportion of the 400Ω. The range of resistance which can be measured is 0-400Ω. This range represents a temperature range of below -200 °C to greater than +800 °C when using a 100Ω platinum RTD. The resistance over the 400Ω span can be measured to an accuracy better than 0.025Ω. Linearization of the RTD and resistance-to-temperature conversion is then performed in the system microcontroller. Accuracy of the temperature measurement will depend on the RTD and its associated linearization algorithm.

AC-Excited RTD Digitizer

Synchronous detection techniques can greatly enhance measurement accuracy. In a synchronous detection system, the sensor is excited with a fixed frequency square wave. The

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 Fax: (512) 445-7581

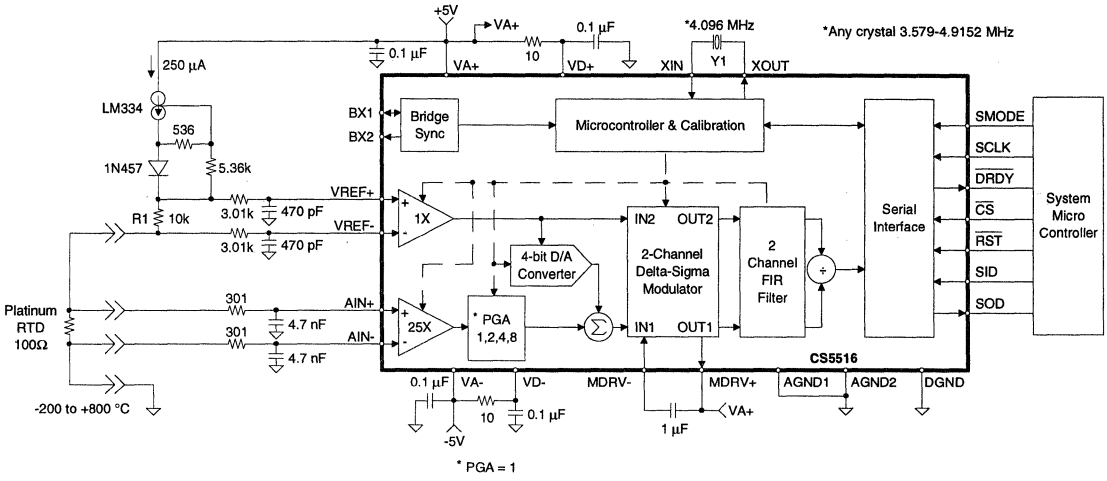


Figure 1. CS5516/20 RTD Digitizer - DC Excitation

detection system measures only the information which is of the same phase and frequency as the excitation frequency. This measurement method eliminates the dc errors introduced by parasitic thermocouples which lie between the sensor and the detection circuitry.

Figure 2 illustrates an RTD measurement system in which the RTD is excited with a switched-polarity current source. Resistor values are illustrated for two different current options. Less self-heating of the RTD occurs with lower excitation current. The majority of RTD measurement systems use a 1 mA direct current (dc) for excitation. The 1 mA current is chosen to produce a large enough output signal so that parasitic thermocouple errors are not a significant portion of the signal to be measured, but parasitic thermocouples will limit accuracy. The proposed ac-excited RTD digitizer uses only 100 µA excitation current. Using a 100 µA current for excitation will result in an output signal only one tenth of that produced by a 1 mA excitation but the self-heating effects of the RTD will be one hundred times less. Less signal output from the RTD is acceptable when synchronous detection is used because error voltages due to parasitic thermocouples are of no consequence.

The switched-polarity dc current source is developed by operational amplifiers U1A and U1B. The CS5520 is configured for internally-controlled AC excitation. The CS5520 is programmed to output a 1kHz square wave (XIN = 4.096 MHz) from its BX2 pin. Capacitor C1 is used to convert the output signal from 0-5 V logic to ±2.5 volts, which is then converted by the voltage-to-current converter to output either ±100 µA or ±400 µA depending upon the selection of resistors. The switched-polarity excitation current is then used to develop the reference voltage for the converter across resistor R7 and used to excite the RTD. A four wire Kelvin-connected RTD is used to maximize measurement accuracy. Reference resistor R7 will set the gain stability

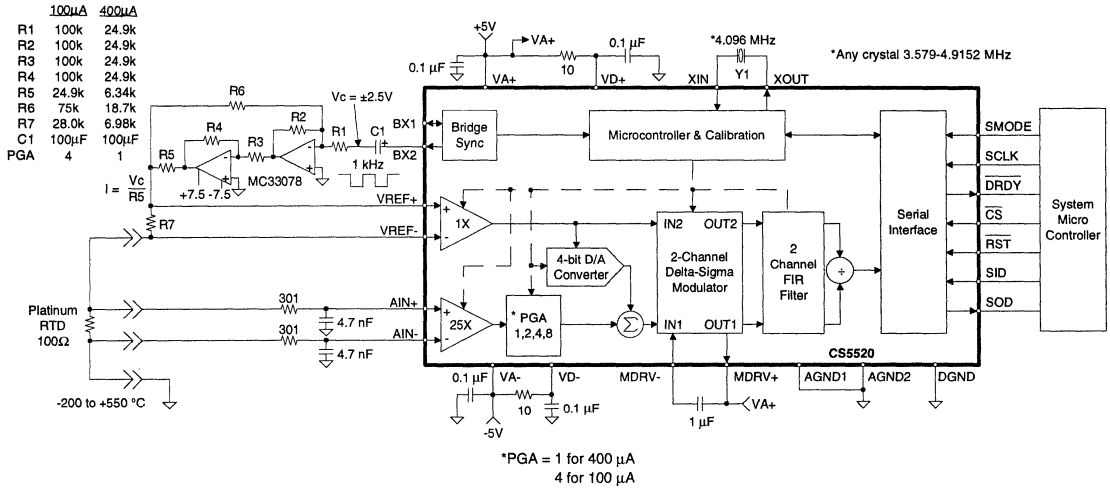


Figure 2. CS5516/20 RTD Digitizer - AC Excitation

of the measurement and therefore a Vishay-type S102K series resistor is highly recommended.

Note that the values indicated for the R7 reference resistor are the nominal suggested values. The converter has gain calibration capability capable of adjusting gain for gain spans æ 20 % of nominal. Therefore resistor R7 could be changed up to æ 15% of its stated value and still leave 5% of the gain calibration range capability available. For example, R7 could be set to 30 K (100 mA) or to 7.5 K (400 mA) to utilize more acceptable precision resistor values. The initial accuracy of R7 is not that important if gain calibration is used. Stability over temperature is the most important parameter for R7.

Resistors of 1% tolerance and 100 ppm tempco can be used in the voltage-to-current converter and not affect system accuracy. The resistance measurement is performed using ratiometric techniques, therefore the exact value of the drive current is not critical. Wirewound resistors should not be used in the switched-polarity current generator or for resistor R7.

When using 100 µA excitation, the PGA (Programmable Gain Amplifier) inside the CS5520 is set to a gain of 4. The internal instrumentation amplifier is fixed at 25; therefore the input span is nominally set to 28 mV ((100 µA X 28.0 k)/ (4 x 25) = 28 mV). The zero of the transfer function can be calibrated using a zero ohm resistor in place of the RTD. Gain calibration can be performed using a 300Ω resistor in place of the RTD. The resistance span will support temperature measurement over a temperature range of -200 °C to +550 °C. If higher temperatures need to be measured, that is, higher resistance than 300Ω, the gain calibration can be performed using a 600Ω resistor with the PGA set to a gain of 2.

Linearization of the RTD and resistance-to-temperature conversion is performed in the system microcontroller. Accuracy of the temperature measurement will depend on the RTD and its associated linearization algorithm.

• Notes •

Application Note

Infrared: A New Standard in Industry

by

Brent Wilson

A new communications standard has been developed for infrared data links. This standard's purpose is to facilitate universal connectivity in portable computing. The fact that the technology which supports the standard is low cost will serve as a catalyst for its incorporation into instrumentation and industrial data collection applications.

The increasing use of small portable digital devices like notebook PCs, personal digital assistants (PDAs) and digital handheld organizers generated a compelling need to develop a cheap wireless interface to enable these devices to communicate with each other. Toward that end, a standards group calling themselves the Infrared Data Association (IrDA) assembled in June of 1993. Formed from companies representing the very backbone of infrared and computer technologies, Hewlett-Packard, IBM, Sharp, Apple, Cirrus Logic (Crystal Semiconductor is a subsidiary of Cirrus Logic), and others, the IrDA published its first set of standards (Physical Layer, Link Access Layer, Link Management Layer, and Transport Layer) in June of 1994, just one year after its first assembly. Soon after, manufacturers of notebook and desktop PCs, PDAs, printers, infrared pods, and other digital equipment began implementing this infrared technology into their next-generation systems.

Why use wireless IR (infrared)?

The primary purpose is to achieve connectivity between devices without the inconvenience and the cost of a cabled system. Many systems which currently use a cable to achieve a serial data connection (typically RS-232) between devices can be readily adapted to use an IR link. The wireless link is most appropriate where the data link needs to be established only momentarily and only for a short distance (one to three meters). This facilitates portability. Wireless IR (per the IrDA standard) offers line-of-sight communications with very few regulatory issues (no FCC requirements like wireless RF).

What does the IrDA standard offer?

Using the IrDA protocol ensures interoperability with PCs, PDAs, and other digital IR equipment. Since the goal of the standard is to support portability, the data coding scheme is designed to minimize IR power-per-bit consumption. This maximizes battery life in portable systems. The IrDA standard supports an IR link of up to one meter in distance (three meters optional) between devices. The transmission distance is limited to minimize power consumption in the transmitter, again to maximize battery life. The IrDA standard supports point-to-point and point-to-multipoint architectures with baud rates of 2400, 9600, 19.2k, 38.4k, 57.6k and 115.2k. CRC-style error detection and frame-based error correction is also supported.

What IR solution does Crystal offer?

The CS8130 is a multi-standard infrared transceiver. The device supports several infrared communication formats; including IrDA (HP-SIR), Sharp ASK (Amplitude Shift Keying),

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX 445-7581

and TV remote. The chip is designed to interface to a standard UART or RS-232-like interface as shown in figure 1. The transmitter portion of the device contains LED drivers with programmable output power. The receiver portion of the chip includes a high-gain PIN diode receiver amplifier with programmable sensitivity. The transceiver runs on any supply from +2.7V to +5.5V with the digital interface designed to maintain TTL-compatible thresholds at all supply voltages. The CS8130 is available in a tiny 5 X 7 mm 20-pin SSOP package and operates over the industrial temperature range of -40°C to +85°C.

The IrDA standard enhances connectivity in the portable computer environment. What are some other applications for short range wireless IR?

The CS8130 can readily be adapted to applications which now use an RS-232 cable of 2 meters or less (The transmit drive can be increased with external transistor drivers and additional LEDs to achieve longer distances). Currently, there are a multitude of hand-held devices which store data for later transfer or accept operator-generated data to be input to a host computer: handheld terminals, barcode readers, remote data loggers, handheld datalogging multimeters, inventory checkers, process control calibrators, home automation and control, and keyless burglar alarm entry systems.

What support does Crystal offer for wireless IR?

The CDB8130 evaluation kit is available from Crystal. It comes with software necessary to link two PC-compatible computers using two CS8130 circuits.

Where do I get a copy of the IrDA standard?

The Infrared Data Association is located at P.O. Box 3883, Walnut Creek, California, 94598. Phone: 510-943-6546 Fax: 510-934-5241

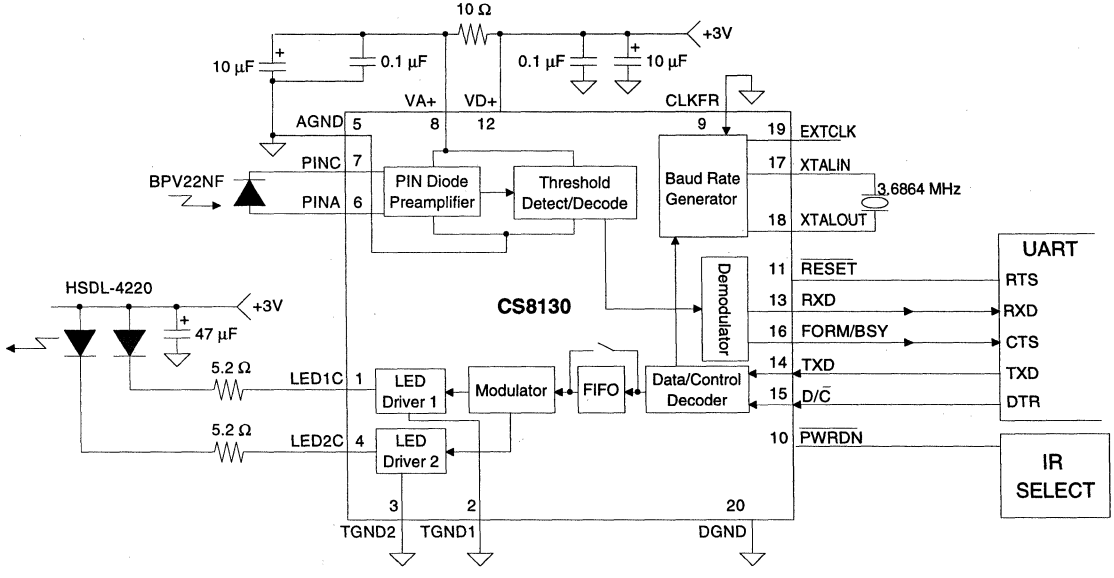
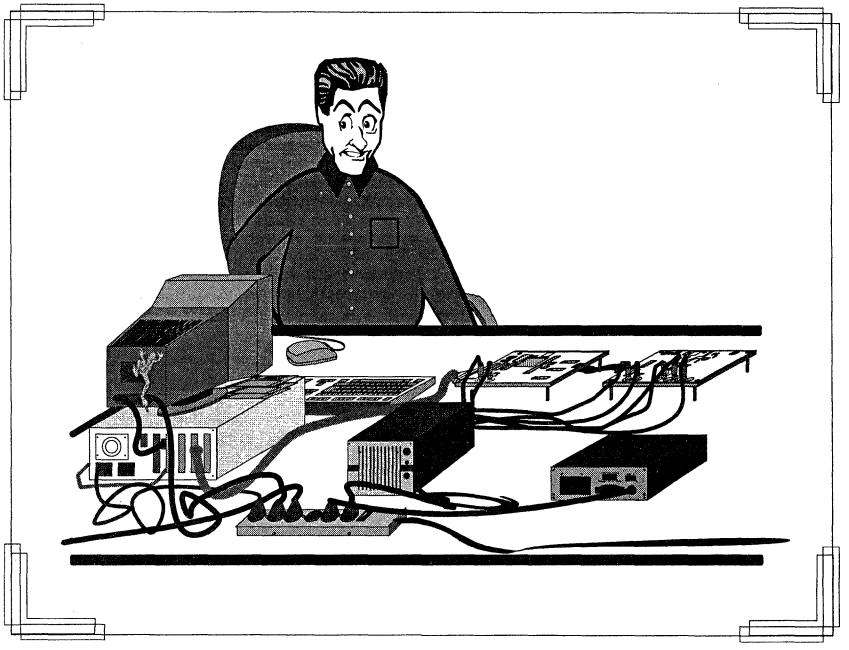


Figure 1. CS8130 Infared Transceiver Interface

Application Note

Using The Capture Evaluation System

By John Lis



The CAPTURE interface board is a development tool that interfaces a Crystal Semiconductor analog to digital converter to a PC-compatible computer. It is software adaptable to be used with a variety of Crystal Semiconductor ADCs. When operating, digital data is collected from the analog to digital converter, then transferred to the PC over a serial COM port. Once the data is in the PC, evaluation software is included to analyze the data and display the analog to digital converter's performance. The evaluation software permits time domain, frequency domain and noise histogram analysis.

The Crystal Semiconductor evaluation equipment is very easy to setup and use, and it will actually expedite system design and development. Setup time for the CDBCAPTURE evaluation system using a Crystal Semiconductor evaluation board is less than one hour. This includes clearing a work area, reading the instructions, and troubleshooting minor problems. Using the evaluation board, the performance of the analog to digital converter can be verified against data sheet specifications. As development continues, the evaluation system can then be used to measure system performance

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

and isolate noise sources. Later on, the evaluation software can be modified for production test.

INITIAL SETUP:

Setup of the CAPTURE evaluation system is very easy. The setup begins with installing the CAPTURE Evaluation software on the PC. Next the power and signal cables are connected to the CAPTURE board, evaluation board, PC, signal generator and power supplies. With the setup complete, evaluation and test can begin.

Before installing the CAPTURE software on the PC, read the INSTALL.DOC file on the CDBCAPTURE Evaluation software diskette. This file contains instructions on software installation. After the software installation is complete, read the README.DOC file in the PC's CAPTURE directory. The README.DOC file contains valuable information concerning hardware requirements, setup, evaluation board configuration, software operation, PC setup, and special notes.

The PC used for the CAPTURE evaluation system has to be a PC AT, PS/2 or compatible with at least four megabytes of Extended Memory. If the CAPTURE evaluation system does not operate properly upon setup, investigate the following items:

- Availability and configuration of Extended Memory on the PC (4 meg, VCPI compatible)
- Sufficient amount of disk space available on the PC (4 meg required)
- CONFIG.SYS proper modification (see README.DOC)
- EMM386 the only memory manager
- Run "CAPTURE -config" to adjust PC hardware
- Power supply voltage and current levels
- Carefully check all the power cables
- Carefully check all the signal cables
- Verify the appropriate COM port
- Possible hardware conflict among PC add-in circuit boards
- Evaluation board jumpers and DIP switch settings

CDBCAPTURE EVALUATION SOFTWARE:

Execution of the evaluation software begins by typing "CAPTURE<RTN>". The screen shown in Figure 1 is displayed, prompting the user to select a part number and interface method. This is done from "SETUP" on the menu bar. Note that "SETUP" and "QUIT" are the only options available on this screen. With the evaluation software running, select the appropriate part number and capture board COM port by pointing and clicking on "SETUP". This procedure will download configuration software to the CDBCAPTURE circuit board via the COM port. When the "SETUP" is properly configured, the "TEST" option becomes enabled, permitting Time Domain, FFT and Noise Histogram tests.

The first test to perform is TIME DOMAIN, found under the "TEST" menu bar. The time domain test is used to verify proper operation and adjust the signal from the generator to the evaluation board. A sinusoid input signal is used, with its frequency adjusted to about 1 percent of the analog to digital converter's output word rate. The "COLLECT" button is pressed, and data is collected. A sine wave should be observed if everything is working. The amplitude is adjusted until it is near full scale. Figure 2 shows a near full scale signal for a CS5101A analog to digital converter. Exceeding full scale will cause the signal to clip and distort.

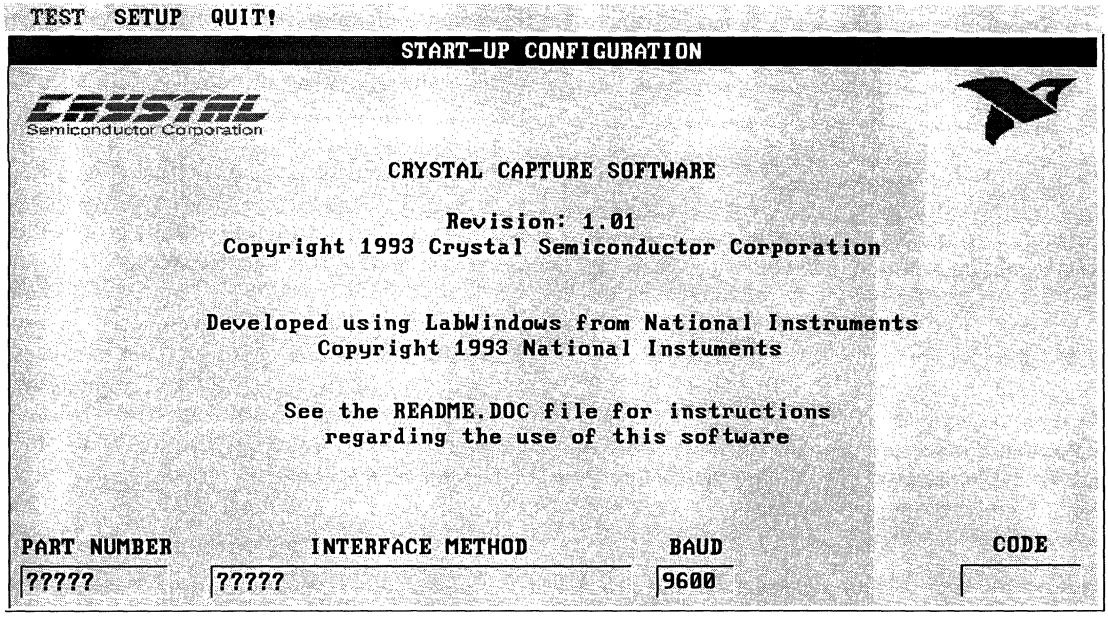


Figure 1

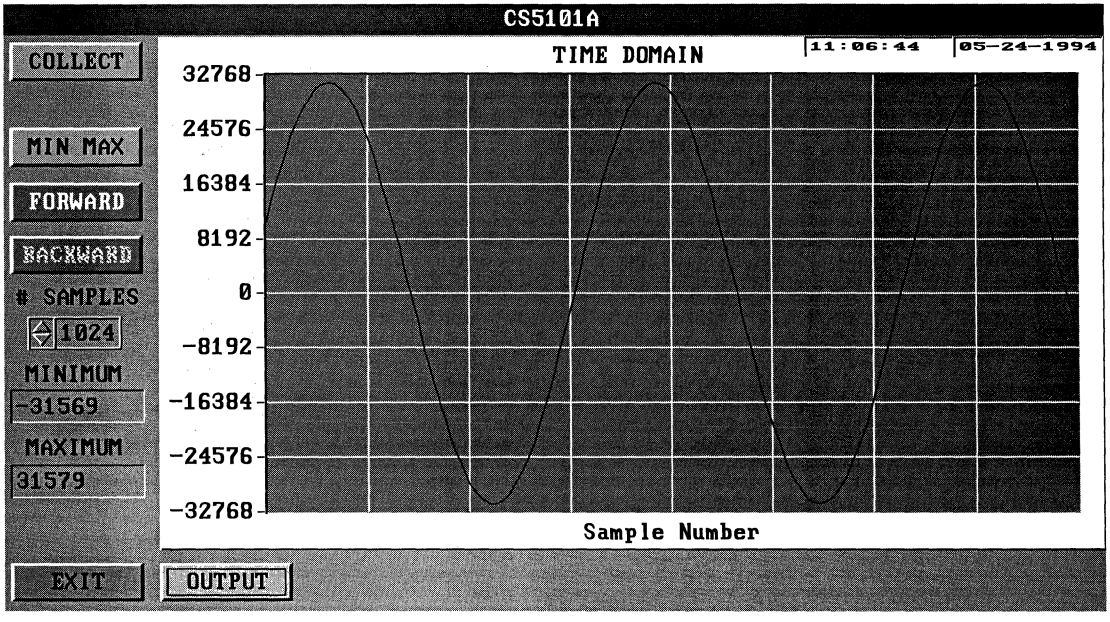


Figure 2.

With the amplitude of the input signal set to the desired value, the analog to digital converter can be tested in the frequency domain. Exit the "TIME DOMAIN" test and select the "FREQUENCY DOMAIN" test from the "TEST" menu bar. Adjust the frequency of the sinusoidal input to about 5 percent of the analog to digital converter's output rate. Figure 3 is an FFT of a 5kHz signal input to a CS5101A.

In Figure 3, the Signal to Noise Ratio (S/N) is 92.884 dB, this translates to 15.14 effective bits. The Signal to Distortion Ratio (S/D) of 95.146 dB is equivalent to 0.00175% Total Harmonic Distortion. These numbers reflect the performance of the entire system including the analog to digital converter, input filters, op-amps, and signal source.

The graph and statistics shown in Figure 3 are calculated from a sample set of data. These calculated values have an uncertainty that depends upon the variance of the sampled population. This uncertainty can be reduced by averaging multiple independent data sets. Figure 4 is an average of 25 FFTs and its uncertainty is five times less than the FFT in Figure 3. Notice how the noise floor at -120dB is much smoother.

1024 sample points of data were used in the FFTs shown in Figures 3 and 4. This translates to a frequency bin width of 50 Hz (Sample Rate/ Number of Samples =51200 Hz/1024). Collecting more samples (2048, 4096, 8192) for the FFT increases the frequency resolution. Figure 5 is a plot of an 8192 sample FFT averaged 25 times. Here the bin width decreased to 6.25 Hz, thus improving the resolution.

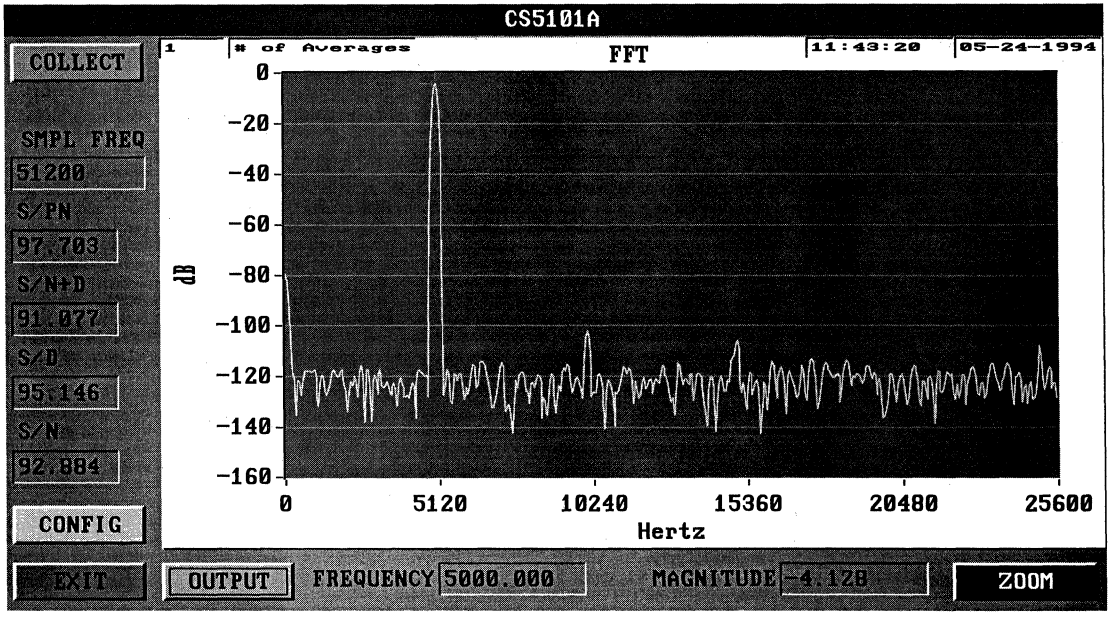


Figure 3.

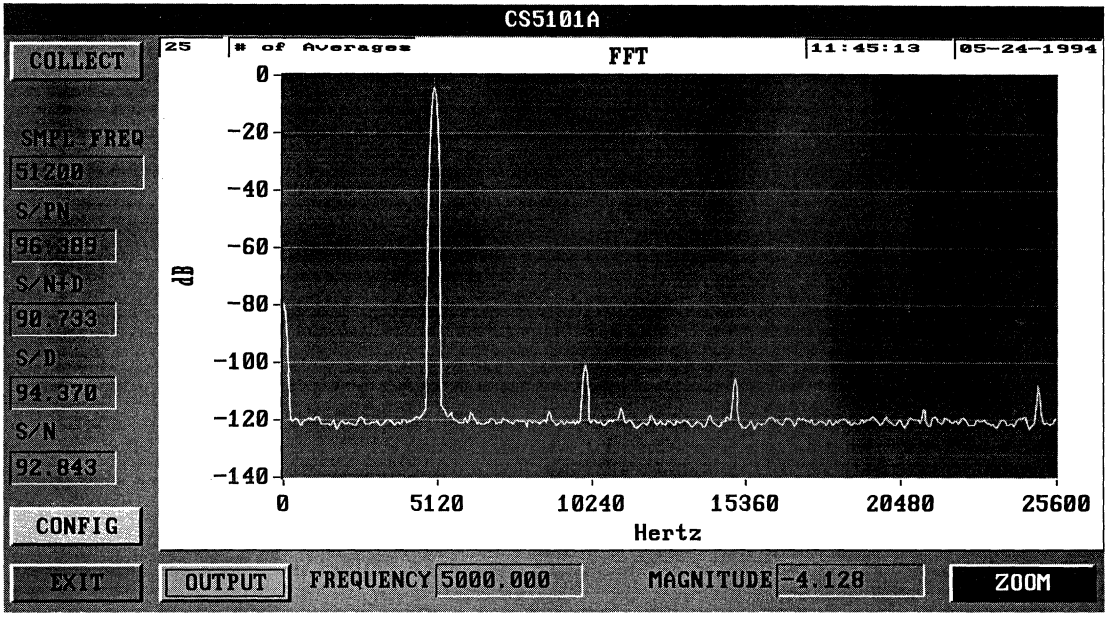


Figure 4.

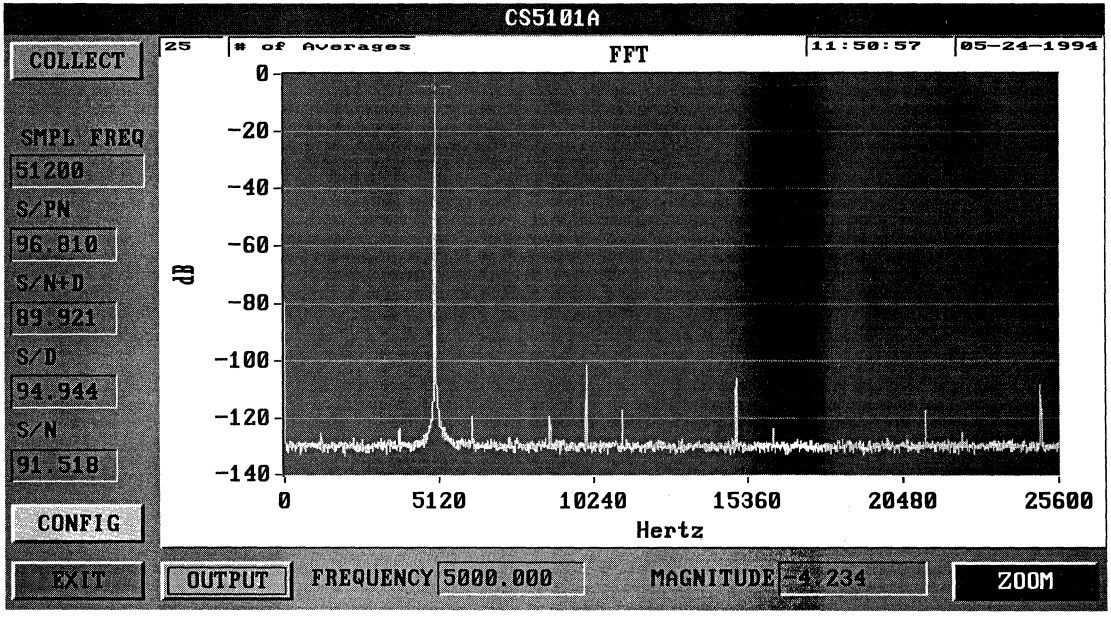


Figure 5.

Ideally, the signal to noise numbers in Figures 4 and 5 should match. However, the increased number of samples in Figure 5 has revealed new information. Notice that the base of the fundamental signal in Figure 5 is slightly smeared. This suggests jitter in either the signal source or sample clock. Also notice how the decrease in bin width from 50Hz to 6.25Hz reduced the spot noise floor by 9dB from -120dB to -129dB. Each doubling of the sample size yields a 3dB reduction in spot noise. Now more coherent noise sources are noticeable and knowledge of the frequency content can aid in isolating the source and improving performance. These noise sources were below the noise floor in Figure 4 and unnoticeable.

Increasing the number of samples from 1024 to 8192 doesn't reduce the uncertainty, so 25 FFTs are averaged for Figure 5. The additional information contained in the larger sample size goes toward higher frequency resolution. The number of averages used depends upon the amount of uncertainty acceptable and time available.

An analog to digital converter can also be tested with a DC signal. For this test, exit the "FREQUENCY DOMAIN" test and select "HISTOGRAM" test from the "TEST" menu bar. Histograms are used in the static testing of DC input signals. Here the input signal stays constant, and an ideal analog to digital converter would output only one code. Deviations from the ideal output are used to measure system performance.

Figure 6 is a Histogram of a CS5101A with its input grounded. The MEAN suggests that the analog to digital converter has an offset of -0.69 LSB. For a reference of 4.5 volts, and operating in bipolar mode, the offset translates to -94.8 microvolts. The standard deviation (STD DEV) is a measure of rms noise. Figure 6 has an STD DEV of 0.49 LSB which translates to 67.3 microvolts of rms noise. From Figure 4, the -120dB noise floor translates to 72 microvolts rms of noise. The STD DEV from the histogram test in Figure 6 indicates that the system rms noise increases by 4.7 microvolts when a signal source is included with the analog to digital converter.

The information presented in Figure 6 is again calculated from sampled data. Thus, there is uncertainty associated with each calculated value. This uncertainty is reduced by increasing the sample size of data. The sample size for the histogram in Figure 6 is 8192.

SUMMARY:

The CDBCAPTURE evaluation system is a valuable computer-aided engineering tool which assists in product development and evaluation. The CDBCAPTURE can quantify component and system performance. Histograms are available to measure the DC accuracy. From the histogram's statistics, the offset, gain error, and noise values can be estimated. FFTs are used with a sinusoidal input signal to measure dynamic performance. The FFT statistics estimate linearity and noise. Quantifying performance aids in system integration. This information can be used to identify noise sources and isolate performance issues to individual components. The result is a quicker time to market and reduced development costs.

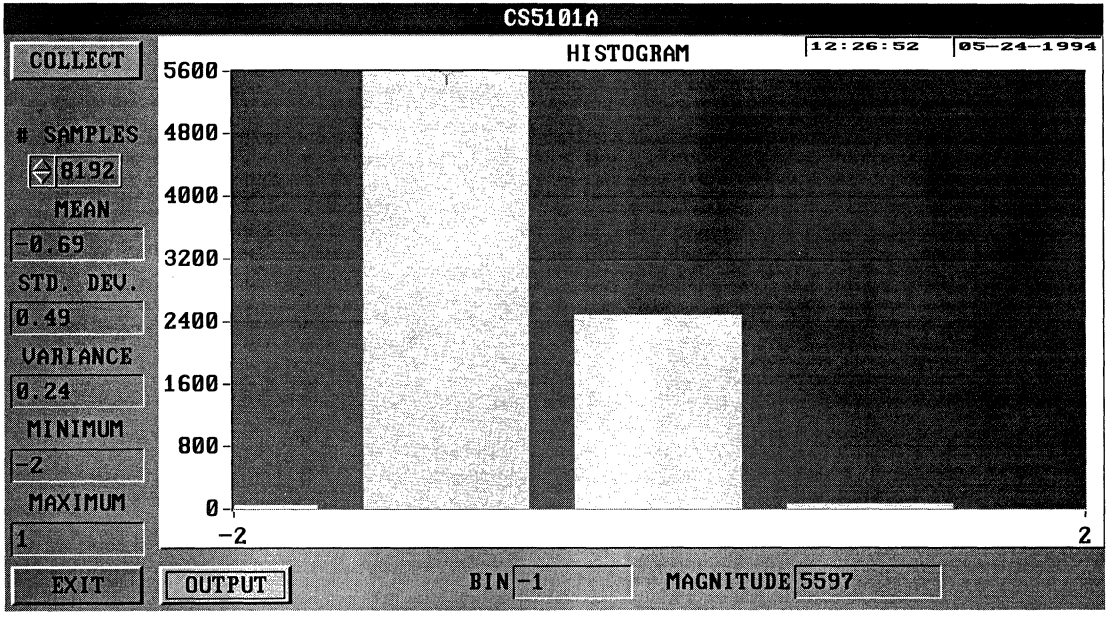

CS5101A
COLLECT
HISTOGRAM
12:26:52
05-24-1994
SAMPLES
8192
MEAN
-0.69
STD. DEV.
0.49
VARIANCE
0.24
MINIMUM
-2
MAXIMUM
1
5600
4800
4000
3200
2400
1600
800
0
-2
2
EXIT
OUTPUT
BIN -1
MAGNITUDE 5597

Figure 6.

• Notes •

Application Note

USING THE CDBCAPTURE SYSTEM WITH EMBEDDED A/D CONVERTERS

by
John Lis

INTRODUCTION

The CDBCAPTURE system can be used to collect data from embedded Analog to Digital Converters (ADCs). Thus system performance of the analog front end can be measured, analyzed and quantified. By analyzing the measured performance, noise sources can be identified, isolated, and corrective actions taken. Here CDBCAPTURE is used as an engineering tool, reducing development time during system test and integration. Another application could be using CDBCAPTURE in production for testing finished products and verifying system performance.

CDBCAPTURE

The CAPTURE interface board is a development tool that interfaces a Crystal Semiconductor ADC to a PC compatible computer. Digital data from the ADC is collected in a high speed digital FIFO, then transmitted to the PC over a serial COM port. Evaluation software is included to analyze the data and demonstrate the ADC's performance. The entire system consists of a CAPTURE interface board, serial cable, RS232 cable, and software.

The software included with the CDBCAPTURE system quantifies static and dynamic performance of ADC systems. Static testing includes Histogramming and calculation of the mean, standard deviation and variance. Dynamic testing includes Fast Fourier Transforms and analysis of the power spectrum. Here Signal to Noise Ratio (SNR), Signal to Noise plus Distortion (SINAD), Signal to Distortion Ratio (SDR), and Signal to Peak Noise (SPN) figures are calculated. Time domain plots are available to visualize signals in the time domain and confirm operation.

CDBCAPTURE WITH EMBEDDED ADCs

The CDBCAPTURE circuit board is designed to directly interface with most Crystal Semiconductor ADC evaluation boards. This permits a quick and easy method to quantify and verify the ADC's performance. However, it is often desirable to measure the ADC's performance in the actual system or to measure the overall system performance. To collect data from an embedded ADC, a special serial cable needs to be designed. This cable incorporates the digital interface circuitry which exists on the evaluation board. This cable is connected to the appropriate signals on the ADC.

To collect data from an embedded ADC, the digital interface circuitry on the evaluation board needs to be incorporated on a modified serial

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX 445-7581

cable. Figure 1 is a block diagram illustrating the process. On the top of Figure 1, the evaluation board CDBXXXX contains digital interface circuitry which translates signals from the ADC to three standard serial signals named FRAME, SCLK and SDATA. The timing and format of these signals vary from device type to device type.

In an embedded ADC application, the digital interface circuit, between the ADC and the CDBCPATURE circuit card, should be implemented on a small card attached to the serial cable as shown at the bottom of Figure 1. The appropriate digital input signals need to be identified. A method to connect to these signals from the embedded system to the cable is then implemented. The connection scheme varies for each application and is easy to implement.

The schematic for the digital interface circuitry is provided with the evaluation board data sheet. Locate the serial interface connector containing the signals: +5 V, GND, FRAME, SCLK, and SDATA on the schematic. Working from this connector, back to the ADC, identify the circuitry required to create the serial signals. This circuitry is implemented on a separate circuit board, attached to a 10 conductor ribbon cable with an IDC socket for its CDBCAPTURE interface. The ADC interface can be any connector scheme that is easy to implement. Possible alternatives include stake headers, test clips, circular connectors,or "D' style connectors.

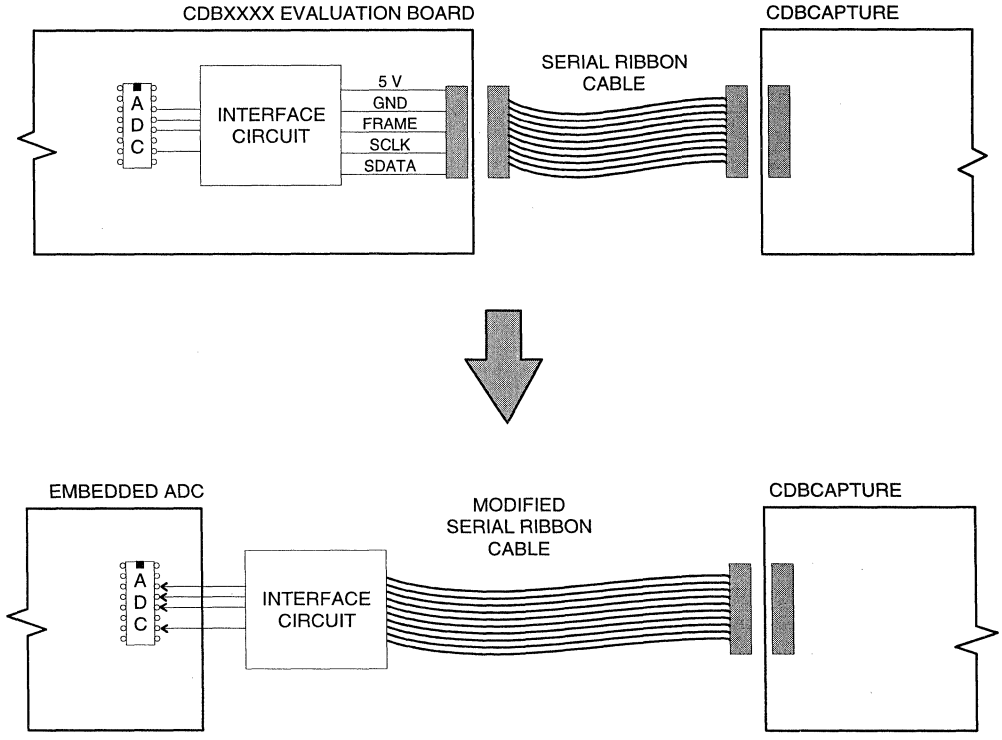


Figure 1. CDBCAPTURE INTERFACE

CS5508 EXAMPLE

The following example uses a CS5508 to illustrate the process of designing a modified serial cable. By examining the schematic for the CDB5508 evaluation board, the digital interface circuitry is identified. The schematic for the CDB5508 evaluation board is provided in Figure 1 of the CDB5505/6/7/8 data sheet. The digital interface portion is shown in Figure 2 below. Resistors R23, R24 and R25 are not required if the $\overline{CS}$ is always active. Also, U3B is always active when using the CAPTURE board, thus it can be changed to a general purpose buffer such as U2.

Figure 3 shows the schematic for the modified cable derived from Figure 2. The $\overline{DRDY}$, SCLK and SDATA signals are buffered to create the serial cable signals for the CAPTURE board. Five volt power is obtained from the embedded system and filtered by R1 and C1 before it is provided to the CAPTURE board. C2 is a bypass capacitor for U1.

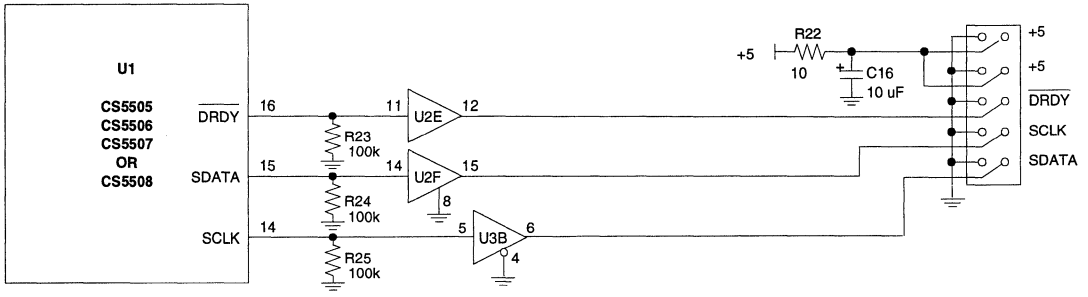


Figure 2. CDB5508 Evaluation Board Schematic for the Digital Interface

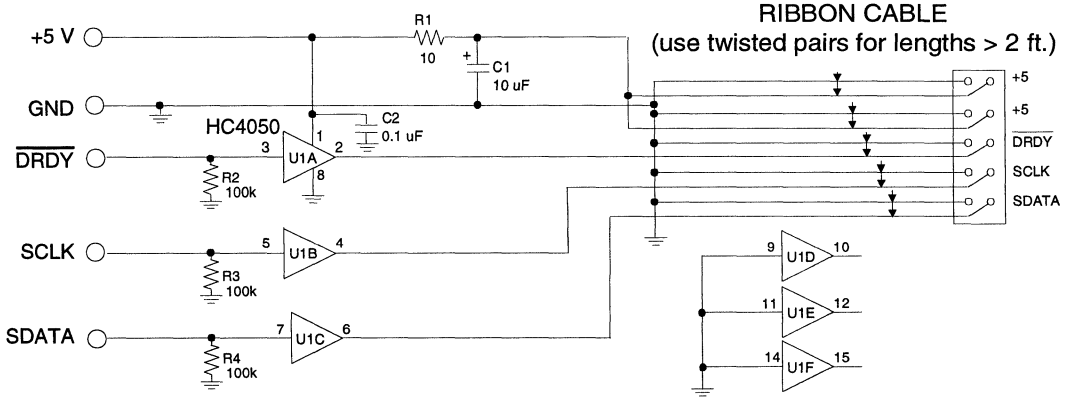


Figure 3. Modified Serial Cable Implementation of the Digital Interface

Figure 4 shows how the hardware can be implemented. The digital interface circuitry is built upon a small circuit board. A ribbon cable with a 10 circuit IDC socket is used for the CDBCAPTURE interface. Separate ground wires should be used for each signal return, and twisted pair ribbon cable used for lengths greater than two feet. The embedded interface uses color coded test clips. The test clips provide a means of interfacing an ADC without any special connectors designed in the system. However this method requires a little more setup time, since the appropriate signals need to be located on the circuit board.

CS5102A EXAMPLE

The CS5102A is used in the second example of an embedded application. The methodology for the cable design is the same as that in the first example using the CS5508. The digital interface circuitry is obtained from the CDB5101A/5102A evaluation board data sheet. This information is contained in the evaluation board's data sheet

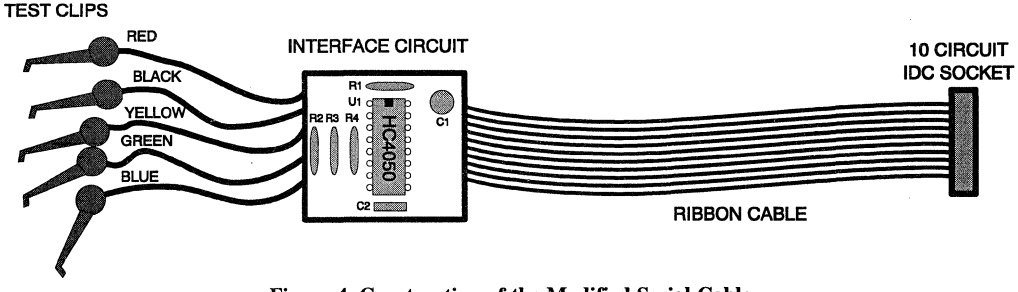


Figure 4. Construction of the Modified Serial Cable

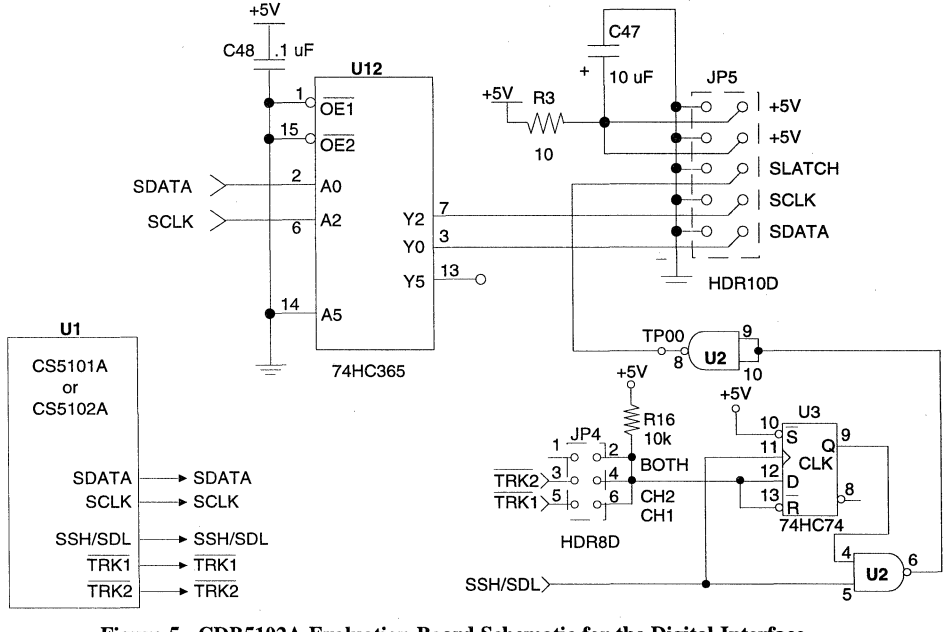


Figure 5. CDB5102A Evaluation Board Schematic for the Digital Interface

Figures 4, 5 and 6. The digital interface circuitry for the CS5102A is show in Figure 5.

Figure 6 is the way the digital circuitry is implemented on the modified serial cable.

Figure 7 is the hardware implementation of the modified serial cable shown in Figure 6. In this example, the embedded system is designed with a test connector. The modified serial cable is built with a connector which mates to the system test connector. The test connector provides a convenient and reliable means of interfacing the ADC.

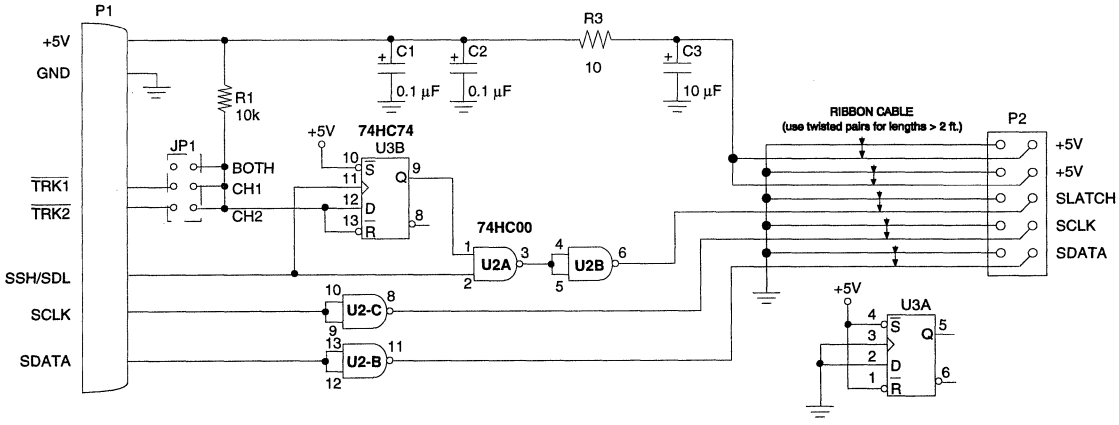


Figure 6. Modified Serial Cable Implementation of the Digital Interface

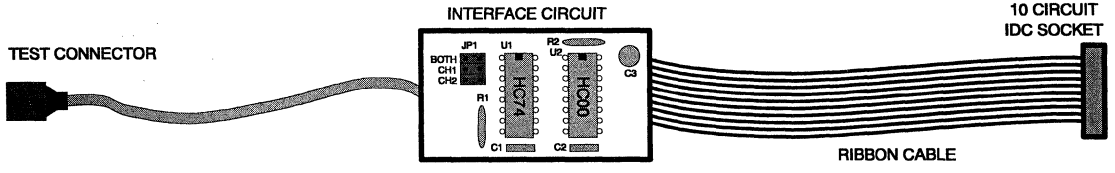


Figure 7. Construction of the Modified Serial Cable

Testing An Embedded ADC

System performance can be measured by interfacing the embedded ADC. The previous sections described the hardware modification required to interface a Crystal Semiconductor ADC with the CAPTURE board. Figures 8, 9, and 10 are the results of using the histogram test on a CS5101A in an embedded system.

Figure 8 is a histogram of a CS5101A operating in the bipolar mode with the analog input pin grounded right at the package. Data book performance is expected, if proper design practices have been used in developing the circuit and layout. In Figure 8, the mean is -0.69 counts, which is well within the typical specification of two counts for the bipolar offset. The standard deviation is 0.49 counts. This translates to 67 uVRMS (0.49×9 $volts/2^{16}$). The CS5101A data sheet specifies 70 uVRMS typical.

A buffer op-amp is integrated in the system and a data set is collected and displayed in Figure 9. Both the mean and standard deviation numbers changed with the addition of the op-amp. The op-amp added 0.66 counts to the offset or 91 uV. The RMS noise increased to 0.63 counts or 87 uV.

Figure 10 shows the histogram for the ADC, buffer op-amp, and signal source. The signal source output is set at zero volts. The histogram statistics indicate an offset of 1.59 counts or 218 uV and the RMS noise is at 218 uV. Note, that as more components are added to the system, the offset changes and the noise increases. These changes can be used to isolate and identify problems.

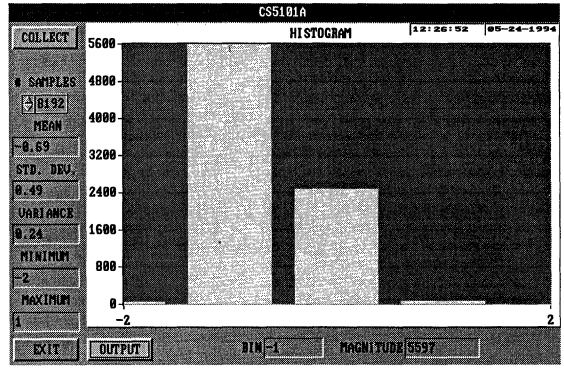


Figure 8. Histogram of a CS5101A with the Input Grounded

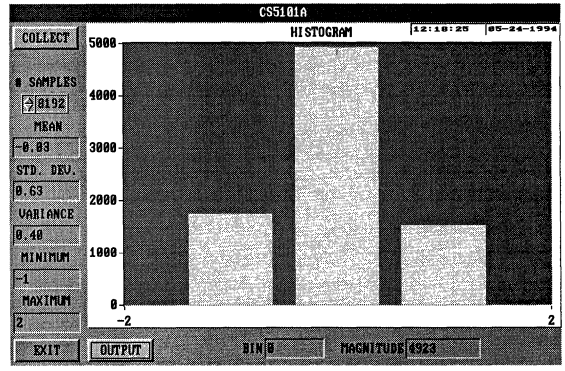


Figure 9. Histogram of a CS5101A with a Buffer Op-Amp

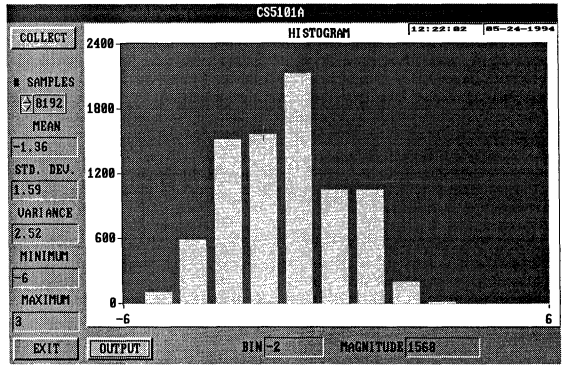


Figure 10. Histogram of a CS5101A with a Signal Source

CONCLUSION

The CDBCAPTURE system is designed to easily connect to most Crystal Semiconductor ADC evaluation boards. Digital circuitry is included on the evaluation boards to implement a standard serial data bus. The CAPTURE board is software reconfigurable to adjust for different ADCs and future products. The CDBCAPTURE system permits easy transfer of digital data to a PC for analysis.

Many times it is desirable to collect data from the ADC while it is operating inside a complete acquisition system. In this case, the digital interface circuitry for the CAPTURE board is implemented outside the system on a modified cable. The electrical system has to provide the appropriate interconnect scheme, using either connectors or test points to clip onto.

The modified serial cable allows the user to measure performance of the ADC while it is embedded in an electrical system. The ADC as well as the system performance can be measured and quantified. This information is used to isolate problems and investigate how certain subsystems interact with each other.

• Notes •

Application Note

CDB5504 Capture Interface

by

John Lis

The CDB5504 evaluation board requires a simple modification to interface with the CAPTURE board. The CAPTURE board requires an SCLK input signal to collect data. However, the SCLK pin on the CS5504 is a digital input only. For the CDB5504 to interface with the CAPTURE board, an SCLK signal needs to be created.

One possible solution is to derive the SCLK from the XOUT signal. The frequency of the XOUT pin is within the specifications for the SCLK signal and the serial port can accept a continuous clock. The CAPTURE board is designed to ignore extra clock signals on the SCLK line when using a continuous serial clock.

Using XOUT as the SCLK input signal is a simple modification of the evaluation board. It is easy to implement, requiring no extra components. The following steps describe the modifications.

The source of the SCLK signal is the XOUT pin on the CS5504. Install a jumper on the CS5504 from U1-6 to U1-18. (Make sure that adjustments are made for the CAB5504 adapter board. U1-18 translates to U1-21 on the bottom of the evaluation board.) The 100k resistor R25 needs to be removed to reduce the load upon XOUT.

Next the 74HC125 buffer needs to be modified. U3-3 is isolated from the circuit, so there aren't two devices driving the SCLK node. Finally U3-8 is isolated, allowing U3B to be active and able to drive the SCLK output signal to the CAPTURE board. Figure 1 is a schematic for the modified evaluation board.

The following check list summarizes the modifications.

◯ REMOVE R25

◯ JUMPER U1-6 to U1-18

◯ ISOLATE U3-3

◯ ISOLATE U3-8

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX 445-7581

MODIFICATIONS TO THE CDB5504 FOR INTERFACING TO CDBCAPTURE

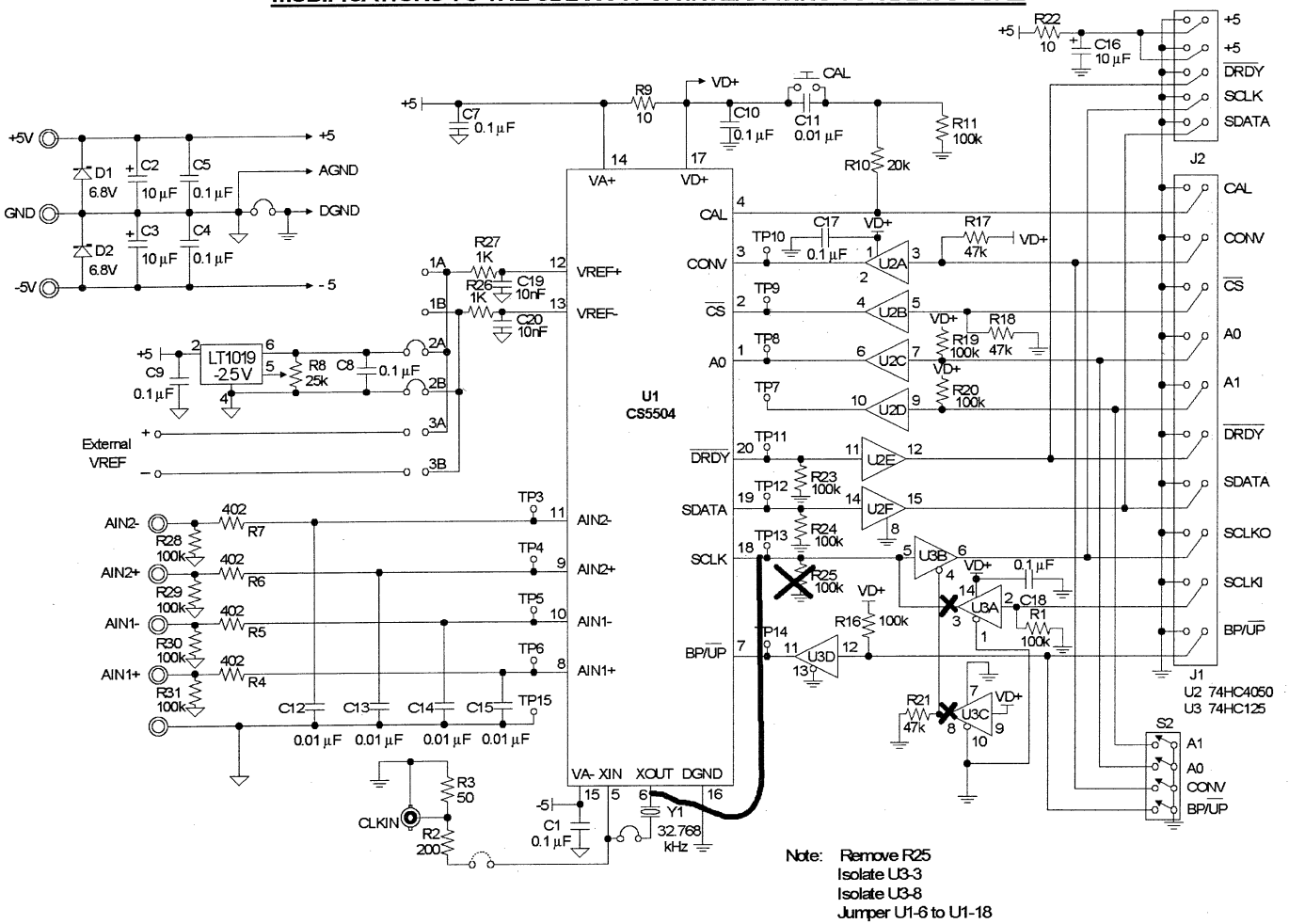


Figure 1. Schematic of CDB5504 Modified for the CAPTURE Interface

Application Note

CDB5509 Capture Interface

by

John Lis

The CDB5509 evaluation board requires a simple modification to interface with the CAPTURE board. The CAPTURE board requires an SCLK input signal to collect data. However, the SCLK pin on the CS5509 is a digital input only. For the CDB5509 to interface with the CAPTURE board, an SCLK signal needs to be created.

One possible solution is to derive the SCLK from the XOUT signal. The frequency of the XOUT pin is within the specifications for the SCLK signal and the serial port can accept a continuous clock. The CAPTURE board is designed to ignore extra clock signals on the SCLK line when using a continuous serial clock.

Using XOUT as the SCLK input signal is a simple modification of the evaluation board. It is easy to implement, requiring no extra components. The following steps describe the modifications.

The source of the SCLK signal is the XOUT pin on the CS5509. Install a jumper on the CS5509 from U1-5 to U1-14. (Make sure that adjustments are made for the CAB5509 adapter board. U1-5 translates to U1-6 and U1-14 translates to U1-21 on the bottom of the evaluation board.) The 100k resistor R25 needs to be removed to reduce the load upon XOUT.

Next the 74HC125 buffer needs to be modified. U3-3 is isolated from the circuit, so there aren't two devices driving the SCLK node. Finally U3-8 is isolated, allowing U3B to be active and able to drive the SCLK output signal to the CAPTURE board. Figure 1 is a schematic for the modified evaluation board.

The following check list summarizes the modifications.

◯ REMOVE R25

◯ JUMPER U1-5 to U1-14

◯ ISOLATE U3-3

◯ ISOLATE U3-8

5

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX 445-7581

MODIFICATIONS TO THE CDB5509 FOR INTERFACING TO CDBCAPTURE

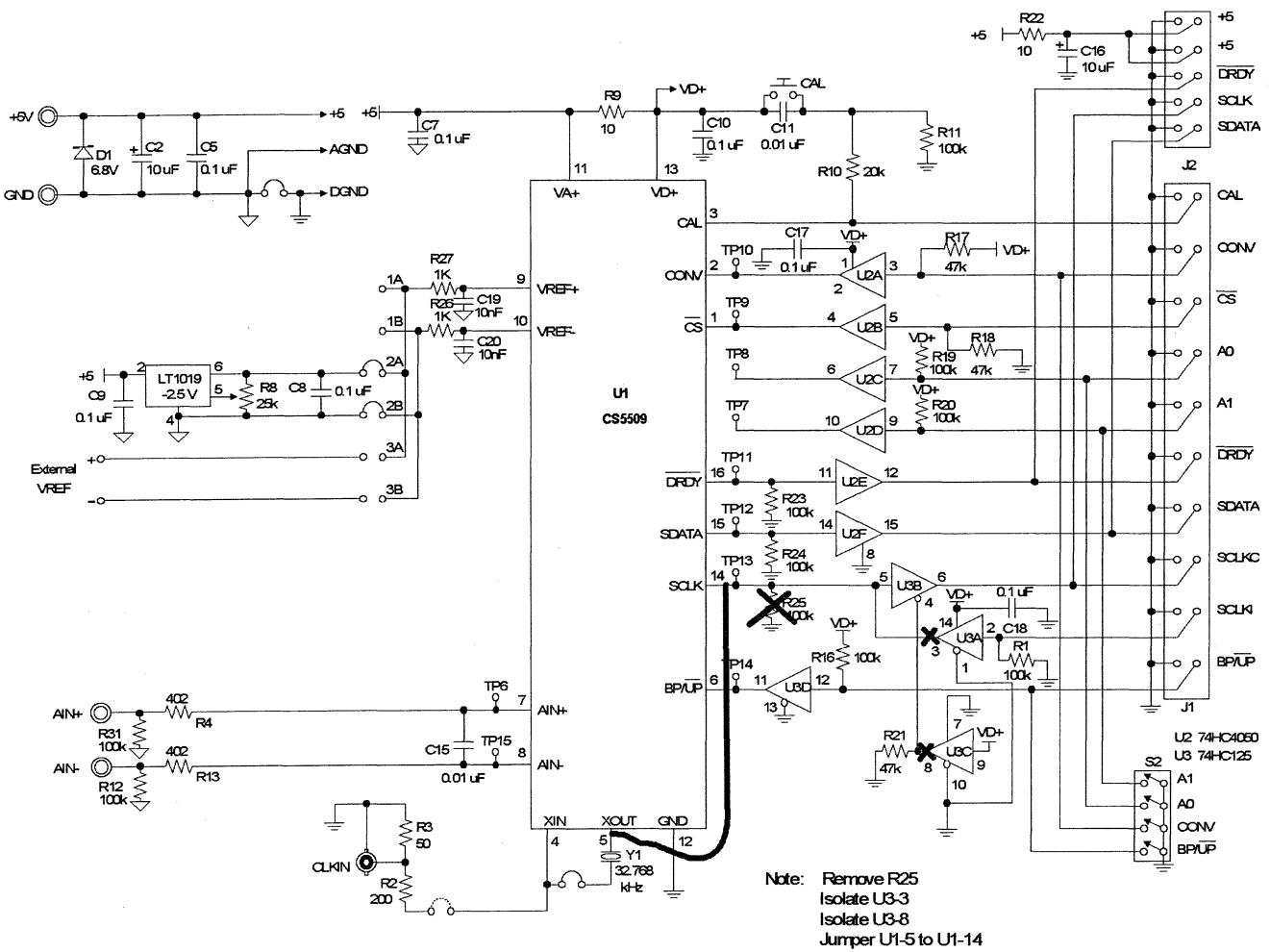
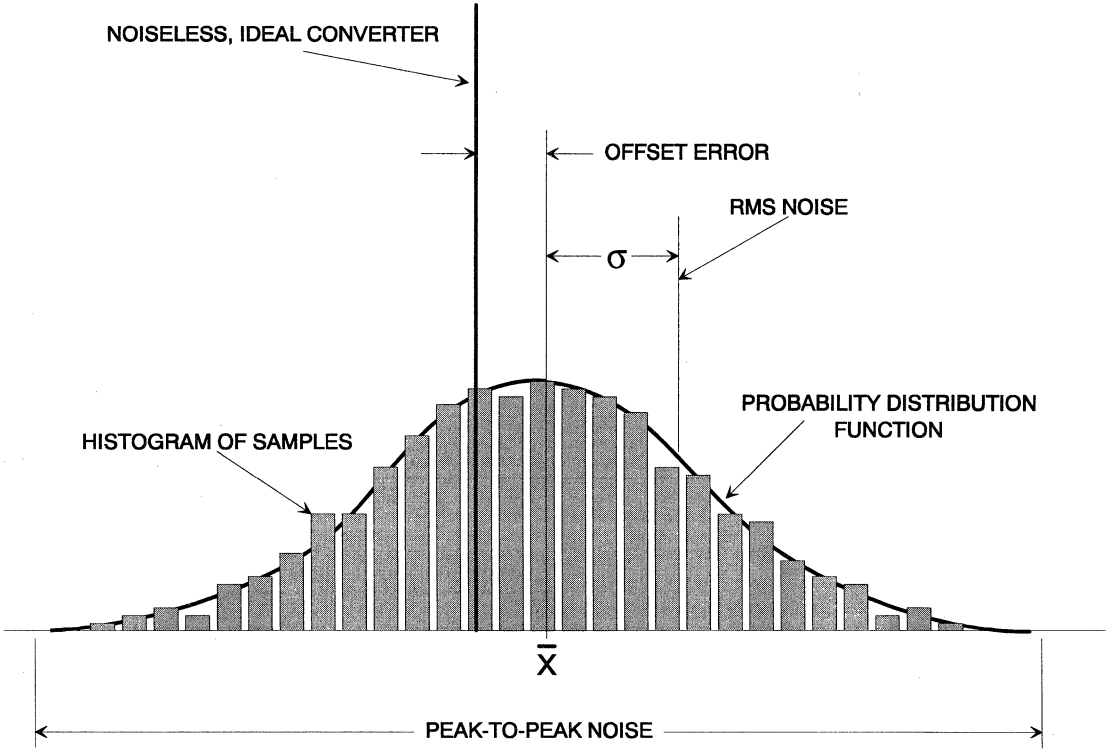


Figure 1. Schematic of CDB5509 Modified for the CAPTURE Interface

Application Note

Noise Histogram Analysis

by John Lis



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

INTRODUCTION

Many Analog-to-Digital Converters (ADC) are used to measure the level or magnitude of static signals. Applications include the measurement of weight, pressure, and temperature. These applications involve low-level signals which require high resolution and accuracy. An example is a weigh-scale that can handle up to a 5 kilogram load and yet resolve the measurement to 10 milligrams. The ratio of maximum load to lowest resolvable unit is five hundred thousand to one. This requires the weigh-scale's ADC to digitize a load cell's signal with a resolution of 500,000 counts.

When working with high resolution ADCs, an understanding of the error and noise associated with the conversion process is required. The goal for this application note is to show how histogram analysis is used to quantify static performance. Sample sets of data are collected and used to measure noise and offset. Statistical techniques are used to determine the "goodness" and confidence interval associated with the estimates. Averaging is addressed as a means of decreasing uncertainty and improving resolution.

In an ideal situation, the output of an ADC would be exact with no offset error, gain error, nor noise. However, the actual output from the ADC includes error and noise. Static testing methods can be used to evaluate the ADC's performance. A dc signal is applied to the ADC's input and the digital output words are collected. The signal's level is adjusted to measure offset and gain errors associated with deviations in the slope and intercept of the ADC's transfer function. Noise is measured as the variability of the output for a constant input.

Statistical techniques can be used to acquire performance measurements, assess the effects of noise, as well as compensate for the noise. An ADC's output varies for a constant input due to noise. The noise is defined by a Probability Density Function (PDF), which represents the probability of discrete events. Statistical parameters can be calculated from the PDF. The PDF's shape describes the certainty of the ADC's output and its noise characteristics.

Noise histogram analysis assumes that the noise is random with a Gaussian distribution. This means that the noise amplitude at a given instant is uncorrelated with the output amplitude at any other instant. A sample set of random noise produces a normal distribution which is used to estimate the PDF. If the noise is not random and does not have a normal distribution, the following histogram analysis would not apply. Examples of non-Gaussian noise include 1/f noise, clock coupling, switching power supply noise, and power line interference.

The ensuing sections discuss noise histogram analysis and the estimation of unknown parameters. The discussion addresses sampling requirements, statistics, and performance tradeoffs. Statistical methods are used to determine "goodness" and confidence intervals of parameters estimated from sampled data. Goodness relates to how well the sample set parameters correlate to the actual system. Averaging is discussed as a method of reducing uncertainty and improving resolution. This paper will lead to an understanding of sampling issues and the tradeoffs that can be made to improve performance and the consequences of the various choices among sample size, confidence level, and throughput.

NOISE HISTOGRAM DESCRIPTION

Usually the PDF describing the ADC noise is not specified. The PDF can be estimated by static testing. This estimated PDF is actually a histogram plot of the occurrences of a random variable versus the individual variations. For an ADC, the random variable is the resulting digital codes, so the frequency at which each code occurs is plotted against each discrete code.

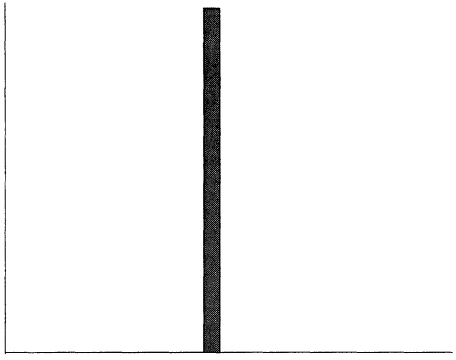


Figure 1. Histogram for a Noiseless ADC

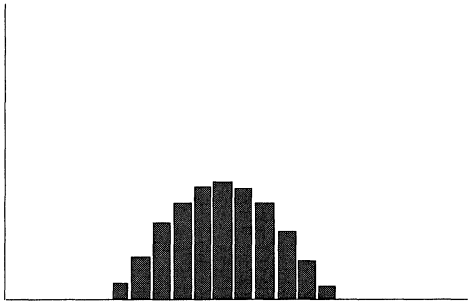


Figure 2. Histogram for an ADC with Noise

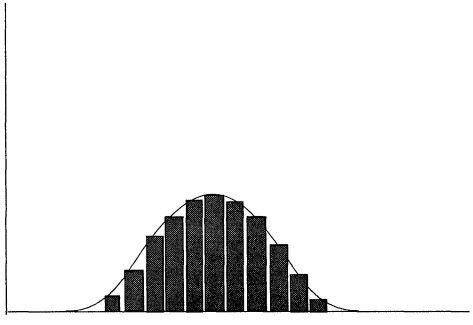


Figure 3. Histogram and Estimated PDF

In a noiseless ADC, the output code for a specific input voltage will always be the same value. The histogram plot for a noiseless converter is shown in Figure 1. If noise sources are present in the ADC, the histogram plot of the output codes contains more than one value. Figure 2 is a histogram plot of an ADC with internal noise. The histogram suggests that the output for a single input can be one of eleven possible codes.

Electrical noise resulting from random effects forms a Gaussian or normal distribution, which is a bell-shaped curve called a normal curve. The Gaussian PDF is continuous and completely determined with the specification of a mean (μ) and variance (σ^2). The Gaussian PDF is defined by the following equation:

$$p(x) = \frac{n}{\sqrt{2\pi}\ \sigma}\ e^{-(x-\mu)^2/2\sigma^2}$$

$n = 1$ for the actual PDF.

Other values for n scale the PDF to fit a sample set. The data presented in Figure 2 can be used to estimate the PDF. Figure 3 plots the histogram of an ADC with noise along with its estimated PDF. The mean and variance were estimated from the sample set of data. From these PDF parameters, the ADC's performance can be quantified. The mean is the expected or average value. It is used to measure offset errors. The variance describes the variability of the distribution about the mean. It is used as a measurement of uncertainty or noise. The square root of the variance is called the standard deviation (σ), and it is a measure of the effective or rms noise. The peak-to-peak noise can be determined from the rms noise value.

The Gaussian PDF can not be used to measure all types of noise. When using a normal or Gaussian distribution to estimate the PDF, the noise must be random. Figure 4 illustrates a histogram of non-random noise. Notice that the

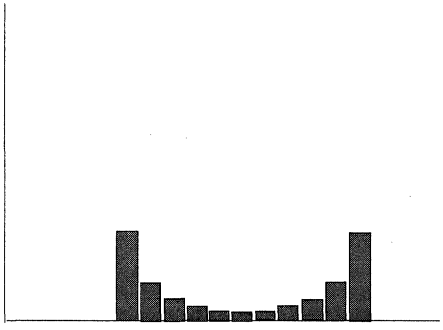


Figure 4. Non-random Noise Histogram

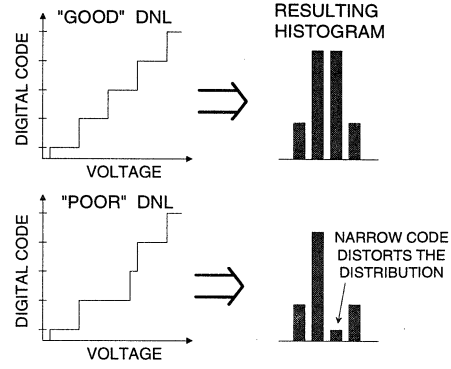


Figure 5. DNL Effects on a Noise Histogram

histogram distribution does not possess the familiar bell-shape. This histogram is possibly the result of 60 Hz line interference or other type of sinusoidal noise. The PDF resembles that of a sine wave, which has a "cusp-shaped" distribution.

Figure 5 is another example of a PDF not having a Gaussian shape. Here, the reason is due to the ADC's poor differential nonlinearity (DNL). Poor DNL results in uneven code widths, which skew the distribution. Delta-Sigma and self-calibrating ADCs possess good DNL specifications. Good DNL is very important for applications which use averaging to improve resolution.

The histogram must possess a bell-shape distribution or the estimated Gaussian PDF will not correlate to the actual system. It is good practice to view the noise distribution and verify that random noise is being analyzed. If the noise is not random, the Gaussian PDF equation can not be used to model the histogram.

EXAMPLE

Figure 6 is a noise histogram of a 20-bit ADC with a grounded analog input, and ± 2.5 volt input range. For an ideal, noise free system, the expected output would always be zero. However, the experimental 1024-sample set ranges from negative seven to positive five. Since the digital codes vary by more then one count, the system noise exceeds quantization error causing an uncertainty associated with the output. The range of code variations requires the histogram to contain at least thirteen discrete ranges or cells. Table 1 lists the number of occurrences of the fifteen cells used to create the histogram.

A PDF can be estimated by using statistical functions to characterize sampled data. Assuming the system noise is Gaussian, the noise can be measured by collecting a set of n samples from a normal population with mean (μ) and variance (σ^2) and calculating the sample mean ($\overline{X}$) and sample variance (S^2).

$$\overline{X} = \frac{1}{n}\sum_{i=1}^{n} X_i$$

$$S^2 = \frac{\sum_{i=1}^{n} (X_i - \overline{X})^2}{n-1}$$

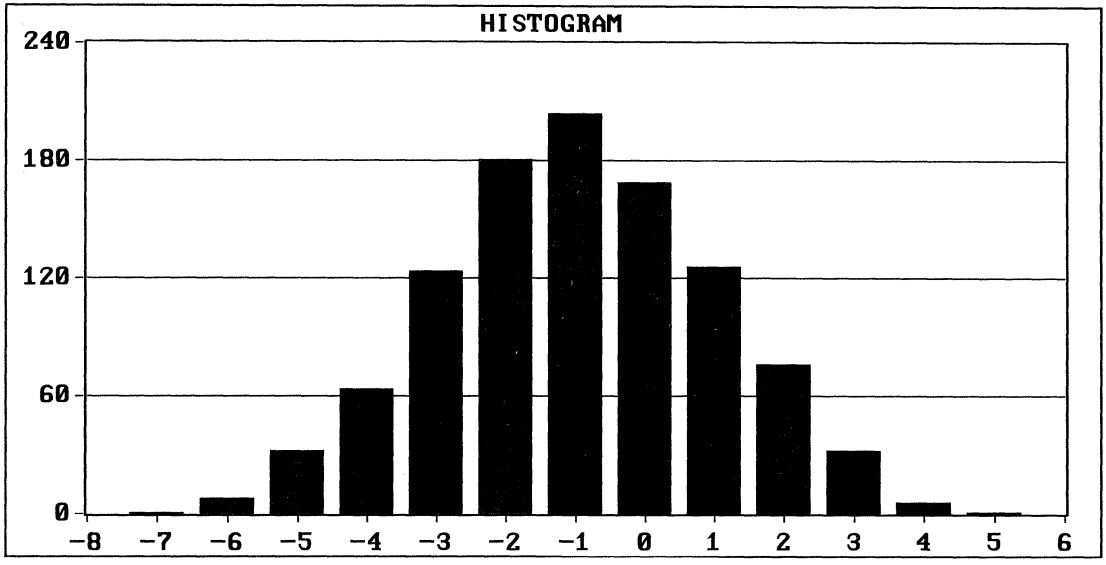


Figure 6. Noise Histogram for a 20-bit ADC

CELL	-8	-7	-6	-5	-4	-3	-2	-1	0	1	2	3	4	5	6
Occurrences	0	1	8	32	64	124	181	204	169	126	76	32	6	1	0

Table 1. Data for Histogram in Figure 6

$\overline{X}$ and S^2 are estimators for the system μ and σ^2. This information is used to create a mathematical model of the system's PDF. From the sample set of data used to create Figure 6, $\overline{X}$ = -0.98 and S^2 = 3.96. The PDF for Figure 6 can be modeled by substituting *n*, $\overline{X}$, and S^2 into the scaled Gaussian PDF equation.

$$p(x) = \frac{n}{\sqrt{2\pi}\ \sigma}\ e^{-(x-\mu)^2/2\sigma^2}$$

Substituting $\overline{X}$ for μ, S for σ, and S^2 for σ^2.

$$p(x) = \frac{1024}{\sqrt{2\pi}\ 1.99}\ e^{-(x+0.98)^2/(2 * 3.96)}$$

Figure 7 overlays the estimated PDF over the histogram of 1024 samples shown in Figure 6. Notice that the PDF and histogram are highly correlated and the estimated PDF seems to be a good model of the actual system.

Continuing with the assumption that the data in Figure 7 has a normal distribution, the performance of the ADC can be quantified using the measurements based on estimates for the mean and standard deviation.

The sample mean in Figure 7 is -0.98 counts. A perfect ADC, operating in the same mode with its input grounded, has a mean of zero. Such a mean deviation from ideal is called an offset. In terms of voltage, the ADC's Zero Offset in Figure 7 is -0.98 counts or -4.67 µV

5

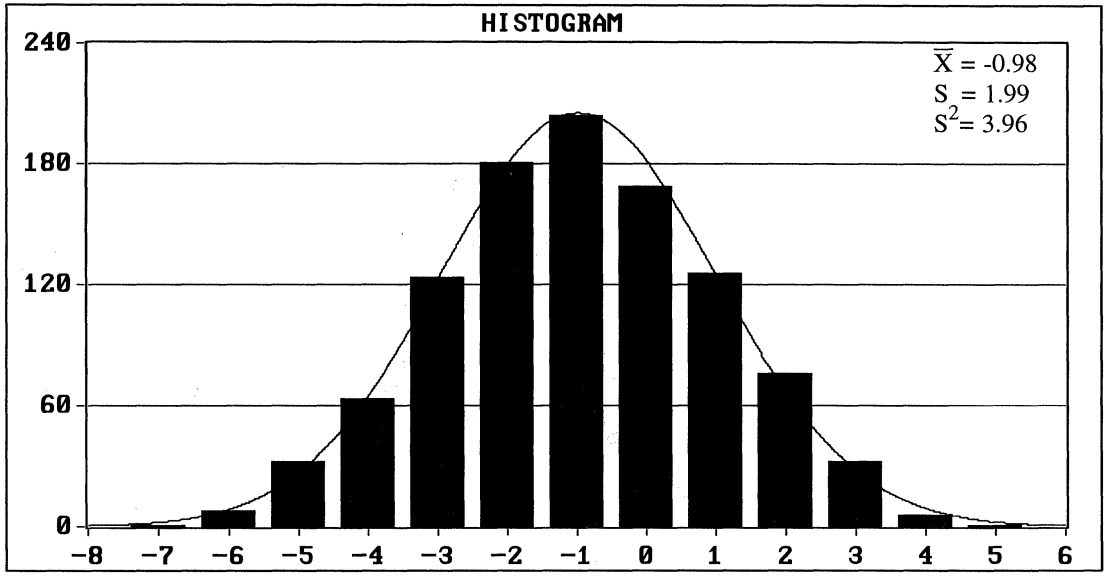


Figure 7. Histogram and Estimated PDF

(1 count = 5 volts /2^{20})) . The Full Scale Error is measured in a similar manner, by calculating a mean for a full-scale input signal.

The PDF's shape, which is used in noise calculations, is defined by the sample variance or its positive square root called the sample standard deviation (S). The standard deviation of a noise distribution is a measure of the rms or effective noise. In Figure 7, the rms noise is 1.99 counts or 9.49 µV. Additionally, the peak-to-peak noise can be calculated by using the standard deviation. Peak-to-peak noise is defined as the interval which contains six standard deviations. For a normal distribution, this interval represents 99.6% of the occurances. In Figure 7, the peak-to-peak noise is 11.94 counts or 56.93 µV.

CONFIDENCE INTERVAL ESTIMATE

In the preceding section, the performance of an ADC was quantified from a sample set of data. For the data in Figure 7, the offset is calculated at -4.67 µV, and the noise at 9.49 µV rms and 56.93 µV peak-to-peak. Since these values are calculated from sampled data, a degree of uncertainty is associated with the estimated performance.

Using statistics, confidence intervals can be calculated for the estimated performance values. First a confidence interval for σ^2 is described. The accuracy of the model derived from sampled data depends upon how well the sample set resembles the actual system. The sample distribution alone is not useful in determining how well the sample variance correlates to the actual variance. However, a confidence interval can be obtained from the sample data. If the degrees of freedom (v) and the actual system variance (σ^2) are included with S^2, then the random variable [$(n-1)S^2/\sigma^2$] has a chi-squared distribution with v degrees of freedom, where $v = n-1$ for n number of samples.

$$\chi^2 = (n-1)\frac{S^2}{\sigma^2}$$

By treating the variance as a chi-squared variable, the variance PDF becomes a function of the degrees of freedom. Now the chi-squared distribution can be used to determine the accuracy of S^2 and state σ^2 as a confidence interval.

Chi-squared percentiles can be obtained from statistics tables. Statistic tables may not be available for large sample sizes. Fortunately, as the number of samples or degrees of freedom increases, a chi-squared distribution approaches a normal distribution. A good approximation of a chi-squared percentile, $\chi^2(\alpha;\nu)$, in terms of a standard normal percentile [$z(\alpha)$] is given by:

$$\chi^2(\alpha;\nu) \approx 0.5\,(z(\alpha)+\sqrt{2\nu-1})^2 \quad , \nu > 100$$

In the above formula, $\chi^2$is a function of α = area under the left tail of the standard normal curve and ν = degrees of freedom.

For example, a 99% confidence interval is determined for χ^2 when n=1024:

Covering 99% of the total area leaves 1% uncovered, which is divided equally between the left and right tails. Thus the desired percentiles are α = 0.005 and α = 0.995. From a table for a Normal Distribution curve, the corresponding percentile points $z(\alpha)$ are -2.575 and 2.575 respectively. Thus 99% of the area under the standard Normal Distribution lies between -2.575 and 2.575.

Substituting values for $z(\alpha)$ and ν in the $\chi^2(\alpha;\nu)$ formula, a range of χ^2 values is calculated.

$$\chi^2(0.005\,;\,1023) = 909.37$$

$$\chi^2(0.995\,;\,1023) = 1142.26$$

From these numbers, it can be stated that χ^2 has a 0.5% possibility of being less than 909.37 and 99.5% possibility of being less than 1142.26. Combining these two conditions, χ^2 has a 99% possibility of being greater than 909.37 and less than 1142.26.

Finally, a 99% confidence interval for σ^2 is obtained by substituting $(n-1)\,s^2/\sigma^2$ for χ^2. Here the values $n = 1024$ and $S^2 = 3.96$ are used to further illustrate Figure 7.

$$909.37 < \chi^2 < 1142.26$$

$$909.37 < (n-1)\,s^2/\sigma^2 \text{ and } (n-1)\,s^2/\sigma^2 < 1142.26$$

$$\sigma^2 < (n-1)\frac{S^2}{909.37} \text{ and } (n-1)\frac{S^2}{1142.26} < \sigma^2$$

$$3.55 < \sigma^2 < 4.45$$

The calculated sample variance (S^2) is 3.96 LSB^2s. There is a 99% confidence that the actual system variance (σ^2) is between 3.55 and 4.45 LSB^2s. The uncertainty associated with 3.96 is less than a half LSB^2 (4.45 - 3.96 = 0.49). That is to say the maximum error is 0.49, with 99% confidence.

If the confidence interval or uncertainty is unacceptable, adjustments can be made. Notice that the interval width is effected by two variables $z(\alpha)$ and n. The interval width can be reduced by either increasing the sample set size or tolerating more uncertainty.

The following calculations using peak-to-peak noise show how $z(\alpha)$ and n affect the confidence interval. Peak-to-peak noise is the uncertainty associated with a single sample. Above, the 99% confidence interval was calculated for the variance. In Figure 7, the estimated variance is between 3.55 and 4.45 with 99% confidence.

Confidence	Number of Samples	α	$z(\alpha)$	χ^2	σ^2 Range	Peak-to-Peak Noise Range
99%	1024	0.005 0.995	z(0.005) = -2.575 z(0.995) = 2.575	909.37 1142.26	$3.55 < \sigma^2 < 4.45$	11.30 to 12.66
95%	1024	0.025 0.975	z(0.025) = -1.96 z(0.975) = 1.96	935.79 1113.06	$3.64 < \sigma^2 < 4.33$	11.45 to 12.49
99%	2048	0.005 0.995	z(0.005) = -2.575 z(0.995) = 2.575	1885.08 2214.55	$3.66 < \sigma^2 < 4.30$	11.48 to 12.44
95%	2048	0.025 0.975	z(0.025) = -1.96 z(0.975) = 1.96	1923.03 2173.81	$3.73 < \sigma^2 < 4.22$	11.59 to 12.33

Table 2. Degree of Confidence and Sample Size Effects on the Confidence Interval

This interval can be translated for peak-to-peak noise:

$$\text{peak-to-peak noise} = 3\sigma + 3\sigma = 6\sigma$$
$$6\sqrt{3.55} < \text{peak-to-peak noise} < 6\sqrt{4.45}$$
$$11.30 < \text{peak-to-peak noise} < 12.66$$
(99% Confidence Interval)

The width of this confidence interval is 12.66 - 11.30 = 1.36 counts. If the confidence is relaxed to 95%, $\chi^2(\alpha;\nu)$ is recalculated using $\alpha = 0.025$ and $\alpha = 0.975$. This results in the confidence interval width for peak-to-peak noise being reduced by 0.32 counts:

$$11.45 < \text{peak-to-peak noise} < 12.49$$
(95% Confidence Interval)

If the set is increased to 2048 samples and the sample variance remains at 3.96, $\chi^2(\alpha;\nu)$ is recalculated using $\nu = 2047$ and the 99% confidence interval becomes:

$$11.48 < \text{peak-to-peak noise} < 12.44$$
(99% Confidence Interval)

The original 99% confidence interval is reduced from 1.36 to 0.96 counts by increasing the sample set. As seen, thousands of samples may be required to reduce the peak-to-peak noise confidence interval to an acceptable width. The size of the sample set depends upon system capabilities and performance requirements. Large data sets are affected by memory size and processing capabilities of the data collection equipment, and ADC throughput. Table 2 indicates how the degree of confidence and number of samples affect the confidence interval.

AVERAGING

Once the ADC noise has been characterized, the effect of averaging can be analyzed. When samples are collected, the average or sample mean ($\overline{X}$) is an estimator of the population mean (μ). $\overline{X}$ is likely to estimate μ very closely when the sample size is large.

Again a confidence interval describes how closely $\overline{X}$ estimates μ, and the sample size governs the width of the interval. The distribution of $\overline{X}$ is Gaussian with a mean μ and variance $\frac{\sigma^2}{n}$. In the case where the ADC output is not Gaussian, the distribution of $\overline{X}$ will approach the above gaussian distribution as n gets large, by the Central Limit Theorem. The confidence interval for μ is:

$$\overline{X} - z(\alpha)\frac{\sigma}{\sqrt{n}} < \mu < \overline{X} + z(\alpha)\frac{\sigma}{\sqrt{n}}$$

where α is set by the confidence interval.

Note that $z(\alpha)\,\sigma$ is the peak noise and $2\,z(\alpha)\,\sigma$ is the peak-to-peak noise value. Restated, the actual mean differs from the sample mean by a range of the peak-to-peak noise divided by the square root of the number of samples. Thus averaging multiple samples reduces the error by $1/\sqrt{n}$.

$$\mu = \overline{X} \pm \frac{peak\text{–}noise}{\sqrt{n}}$$

The peak-to-peak noise of the sample set for Figure 7 is 11.94 counts. If one sample is taken, the 99.6% confidence interval is 11.94 counts or ± 5.97 counts. If all 1024 samples are averaged, the actual population mean is between -1.17 and -0.79 with a 99.6% confidence. The uncertainty is reduced to ± 0.19 counts. Note that the quantization error for an ideal ADC produces an error of ± 0.5 counts. Averaging 1024 samples improves this noisy 20-bit ADC's accuracy to better than 21 bits!

As shown above, averaging can reduce the effects of Gaussian distributed noise as well as quantization error. However, the tradeoff is in reduced throughput. To get the confidence interval to less than one count, $\sqrt{n}$ has to be greater than the peak-to-peak noise. For the sample set of data plotted in Figure 7, 143 samples (11.94^2) need to be acquired and averaged. Over 36,496 samples are required to create a 24-bit ADC with less than one count of peak-to-peak noise (reduce the uncertainty of a 20-bit converter to ±1/32 counts). This would reduce a 100kHz, ADC to an effective throughput of 2.74 Hz. Averaging sacrifices throughput for improved resolution and reduced uncertainty.

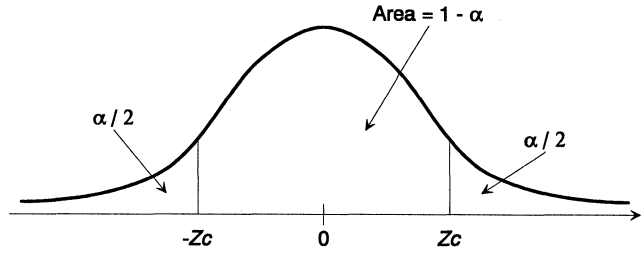
CONCLUSION

Statistical methods are available to measure the performance of an ADC. The testing involves inputting a noise free, accurate DC signal to the ADC and collecting a sample set of data points. The sample set is used to calculate estimators for the mean and standard deviation. More statistics are used to decide the "goodness" and confidence level associated with the estimates. Averaging was introduced for reducing uncertainty and improving resolution. However, averaging reduces the ADC's effective throughput. Figure 8 illustrates the tradeoff between reducing uncertainty and lowering the effective throughput.

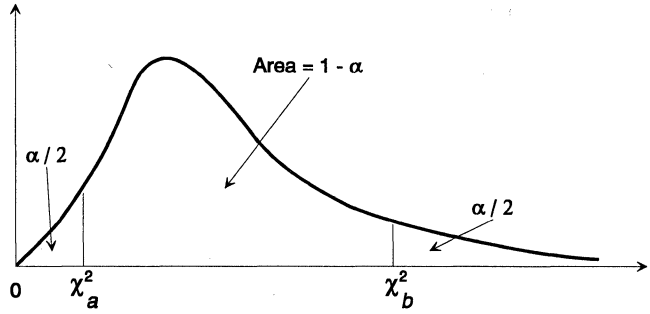
The same methods used to measure an ADC's performance can be used to measure the performance of an entire system which includes additional components containing multiple noise sources and offsets. During system integration or production test, tests can be performed as subsystems are added. This can be used to measure the performance of individual subsystems or isolate problems to a subsystem or component. The results can then be used with compensation techniques to improve system performance or to determine corrective actions.

TABLE OF VARIABLES

μ	mean
σ	standard deviation
σ^2	variance
$p(x)$	probability density function
$\overline{X}$	sample mean
S	sample standard deviation
S^2	sample variance
χ^2	chi-squared variable
n	number of samples
v	degrees of freedom.
α	area under the normalized curve
z	standard normal distribution



PDF for a Gaussian random variable. The area 1 - α is the confidence interval



PDF for a Chi-Square variable. The area 1 - α is the confidence interval

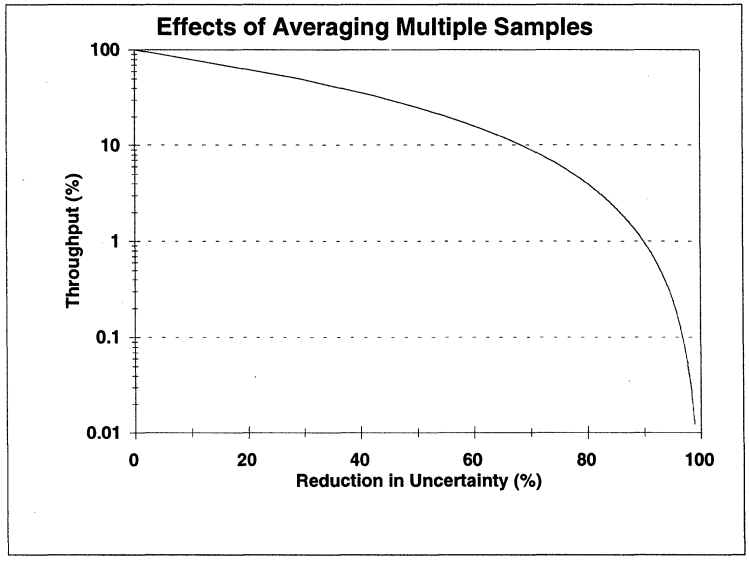


Figure 8. Tradeoff between Uncertainty and throughput

REFERENCES

[1] John Neter, William Wasserman, & G.A. Whitmore, "Applied Statistics" Allyn and Bacon, Inc.

[2] Ronald E. Walpole & Raymond H. Myers, "Probability and Statistics for Engineers and Scientists", Macmillan Publishing Co., Inc, New York, 1978.

[3] Richard H. Williams, "Electrical Engineering Probability", West Publishing Company.

[4] Ferrel G. Stremler, "Introduction to Communications Systems",Addison-Wesley Publishing Company, Inc. 1982.

• Notes •

Clock Options for A/D Converters

by
Jerome Johnston

Most A/D converters require a clock source for operation. Some converters, such as the CS5101A, CS5102A, CS5501/3, and the CS5504/5/6/7/8/9 include an on-chip gate oscillator as shown in Figure 1. A Pierce-oscillator architecture is commonly used. It is constructed with either on-chip loading capacitors (C2 and C3 in Figure 1) or it may require off-chip loading capacitors (C4 and C5) depending upon the crystal frequency. The data sheet for the particular A/D converter should give instructions regarding the size of any external loading capacitors.

System applications may require the A/D converter clock to drive other circuits; or the measurement system may require two or or more A/D converters to be driven from the same clock. It is always preferable for one common clock to be used for the entire system. With one system clock, any interference will be synchronous and will generally be less severe.

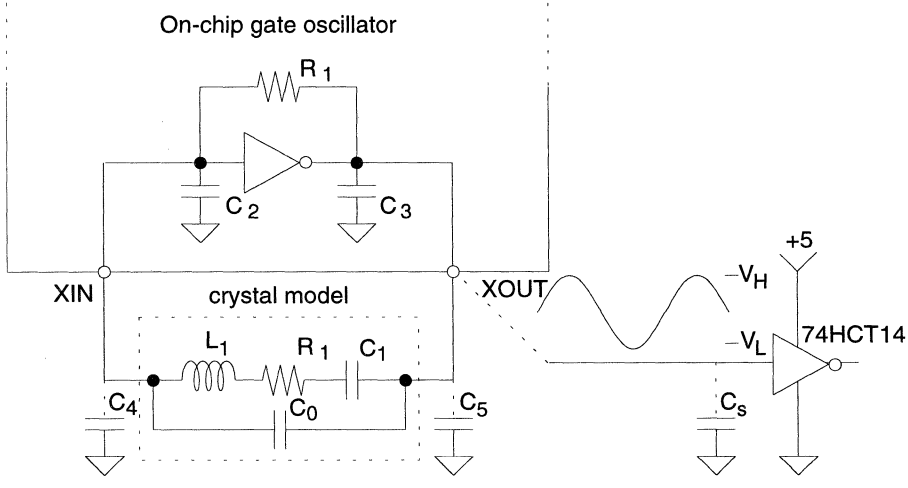


Figure 1. Using 74HCT14 Gate to Buffer Oscillator Output

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 Fax: (512) 445-7581

To drive external circuitry from the on-chip oscillator of an A/D converter use the XOUT or CLKOUT pin. Although the on-chip oscillator is shown as an inverter gate, this does not mean that it can drive external circuitry very well. The gate oscillator circuit is optimized for low gain to facilitate building a stable oscillator; and the circuit may be optimized to minimize power dissipation in the oscillator. For example, the on-chip oscillator of the CS5504/5/6/7/8/9 devices uses only 10 µA of supply current. It is therefore necessary to buffer the oscillator output with a high impedance gate input such as CMOS logic. The CS5504/5/6/7/8/9 devices work well with a 74HCT14-type gate. The HCT threshold is required as the oscillator output oscillates between 0 - 2.5 volts. The external gate should be located very near to the XOUT pin of the converter to minimize stray capacitance. The same technique can be used with the CS5101A/02A and CS5501/03 converters. When using external loading capacitors (C4 and C5 in Figure 1) and an external gate to buffer the oscillator output, the value of C5 should be lowered by the estimated input capacitance of the CMOS gate input and any additional stray capacitance. For example, the oscillator by itself may call for C5 to be 30 pF. But if the oscillator output is driving an external CMOS gate, the gate input may have 5-10 pF of input capacitance and there may be 1-4 pF of stray capacitance. Under these conditions the value of C5 should be lowered, say to 22 pF, so that the total capacitance seen at the output of the on-chip gate oscillator is maintained near 30 pF.

Some applications may use a central oscillator which is then distributed as shown in Figure 2. The oscillator may use a logic gate, a clock module, or an oscillator chip such as the Harris HA7210. Buffers are then used to drive the system circuitry. To minimize clock jitter, the power supply to the oscillator, whether it be a gate or a module, should be decoupled with an RC filter to keep any noise on the power supply from reaching the oscillator.

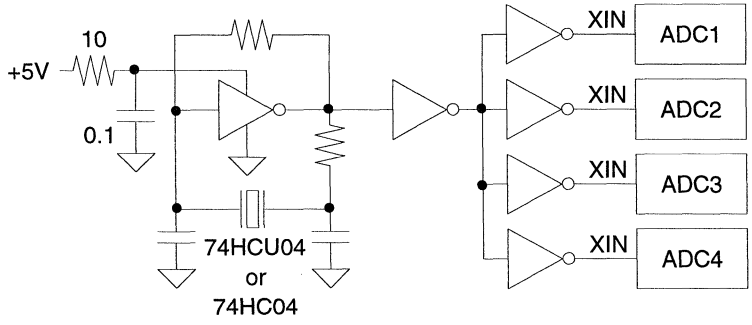


Figure 2. External Oscillator using Buffers for Distributed Clock

Working with gate oscillators can present some difficulties. For example, just looking at the output with a scope probe loads the oscillator with the probe capacitance. This can change the oscillator frequency, the signal amplitude, or even cause the oscillator to quit oscillating. Use a low capacitance or active probe if possible. A series resistance can be added between the circuit and a standard probe to minimize the effects of the scope capacitance as shown in figure 3. Choose R to be 5-10 times greater than the impedance of the output loading capacitor (at the frequency of oscillation).

Customers have asked whether the on-chip gate oscillators used in Crystal A/Ds call for series or parallel-type crystals. The only difference between series and parallel-type crystals is the method by which their fundamental frequency is calibrated. The frequency at which series crystals are calibrated to oscillate is a function of the crystal's internal inductance (L_1) and its internal series capacitance (C_1) of figure 4. These resonate in series to produce zero phase shift through the crystal network. Series-mode oscillators use non-inverting amplifiers.

Parallel-mode crystals are calibrated using the crystal's internal inductance and its internal parallel capacitance in parallel with external loading capacitors. Parallel-mode oscillators require an inverting amplifier which contributes 180 degrees phase shift along with the 180 degrees phase shift contributed by the network composed of the crystal and the loading capacitors.

All of the converter chips mentioned in this application note use parallel-mode oscillators, but either series or parallel mode crystals will

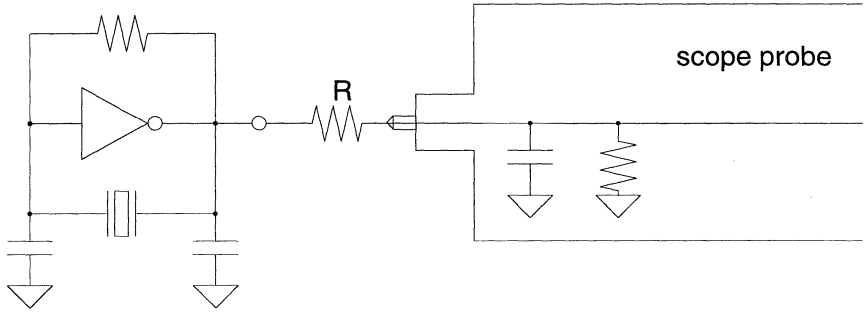
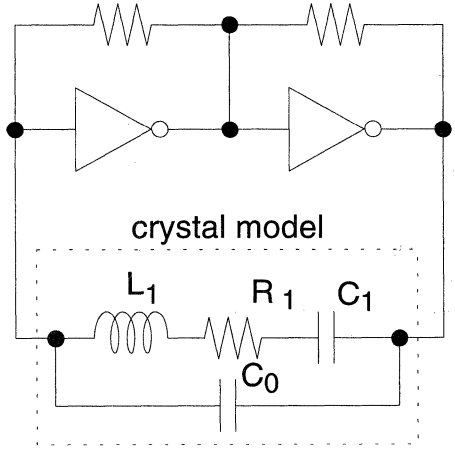


Figure 3. Isolate Scope Probe Capacitance to prevent Oscillator Loading.

5

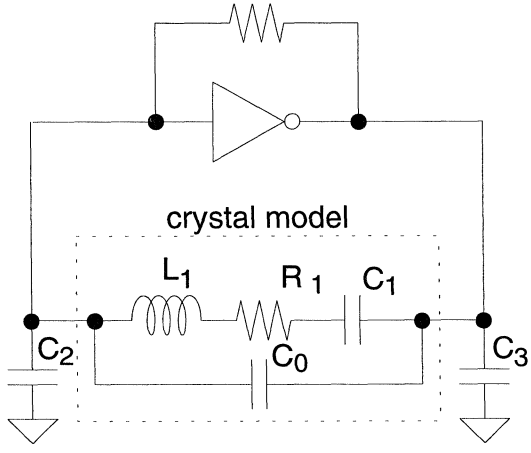
oscillate. When using a series-mode crystal in parallel mode, its oscillation frequency may be off a small percentage, never more than 0.5%. This will not cause problems unless the clock is used for time-keeping purposes.

Parallel resonant crystals always require a specified load capacitance. For example, a parallel crystal may be specified as 8.000 MHz (20 pF); meaning that the crystal will oscillate at exactly 8.000 MHz if loaded with exactly 20 pF. This would require C_2 and C_3 of figure 5 to be 2 X 20 pF (39 pF typical). This is because the capacitors are series-connected, which divides the effective capacitance.



$$f = \frac{1}{2\pi\sqrt{L_1 C_1}}$$

Figure 4. Series Resonant Crystal Oscillator.



$$f = \frac{1}{2\pi}\sqrt{\frac{1}{L_1 C_1} + \frac{1}{L_1 C_T}}$$

$$C_T = C_0 + \frac{C_2 \times C_3}{C_2 + C_3}$$

Figure 5. Parallel Resonant Crystal Oscillator.

Application Note

Switched-Capacitor A/D Converter Input Structures

by
Jerome Johnston

CMOS has become popular as the technology for many modern A/D converters. CMOS offers good analog switches, good capacitors (although size is limited), and high digital logic density. These features have been combined to achieve a number of different A/D converter architectures. Many SAR-type (Successive Approximation Register) CMOS A/D converters utilize ratio-weighted capacitors, all controlled by analog switches and digital logic, to achieve conversion. Delta-sigma converters use analog switches and small capacitors for sampling. Conversion in a CMOS delta-sigma A/D converter is performed using a switched-capacitor comparator which samples at a much higher speed than the bandwidth of the signal to be converted. The comparator then presents a stream of ones and zeros to be processed to the digital filter portion of the chip. High CMOS logic density allows the digital filter to be orders of magnitude more complex than an analog filter while being drift-free and exactly repeatable from chip to chip.

The analog input of most CMOS A/D converters is constructed with analog switches and capacitors. Figures 1, 2, and 3 illustrate input structures commonly found in CMOS or BiCMOS A/D circuits. These three structures are common to capacitive-type SAR converters and to delta-sigma converters.

Figure 1 illustrates an unbuffered capacitive sampler. The size of the sampling capacitor and the frequency of the switch closure will deter-

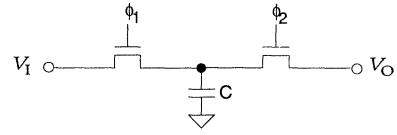


Figure 1. Unbuffered Capacitive Sampler

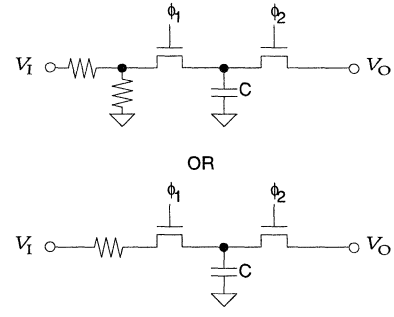


Figure 2. Unbuffered Capacitive Sampler with Resistor Input

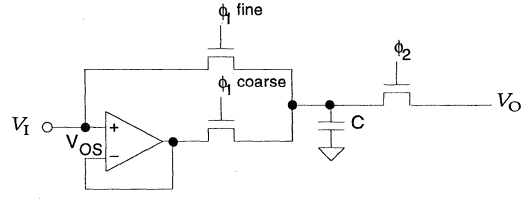


Figure 3. Coarse Charge Buffered Capacitive Sampler

5

mine the severity of the dynamic load seen by the driving amplifier.

Figure 2 illustrates a capacitive sampler with an input resistor added. Input resistors are used in some A/D converters to divide down the input signal; for example, reducing ±10 volts down to ±2.5 volts. The signal reduction allows the circuitry internal to the converter to be powered from ±5 volts and still handle high level input signals. The resistors may introduce gain errors over temperature because of their limited tempco tracking. One bit at 16 bits is only about 15 ppm. The closest tempco tracking of the best resistor technologies is about 2 ppm/°C.

Some converters may use a single resistor at the input. The resistor reduces the transient current impulse seen by the external driving amplifier. The resistor also enables the external drive amplifier to see a resistive load instead of a more capacitive load. This improves the amplifier phase margin and reduces the possibility of ringing. The resistor enables the transient load current from the sampler to be spread over time due to the RC time constant of the circuit. A series resistance is usually acceptable in 12-bit designs, but it can hinder performance in fast 16-bit converters. The settling time of the RC network can limit the speed at which the converter can operate properly or reduce the settling accuracy of the sampler.

Figure 3 illustrates a coarse charge (also called rough charge) buffered capacitive sampler. The on-chip coarse charge buffer reduces the dynamic current demanded from the signal source because the coarse charge buffer precharges the sampling capacitor to a voltage nearly equal to the input signal.

The input structures in Figure 1 and 3 are most common. To understand the drive requirements of these two circuits, the input current required by the unbuffered sampler will be examined and its effective input resistance will be determined. Then it will be compared to the input current and effective input resistance of the coarse charge buffered sampler.

In Figure 1 the sampling capacitor, C is switched at a fixed frequency, f. The capacitor transfers a specific amount of charge each time the capacitor is switched. This charge is furnished by the signal source outside of the chip.

The size of the sampling capacitor and the frequency at which it is switched will determine the input current, and therefore, the effective input resistance of the sampler. Using the fundamental equations:

$$i = \frac{q}{t} \qquad q=cV$$

The instantaneous current is equivalent to the charge per unit time and charge is equivalent to the product of the capacitance and voltage, an equation which defines the input current to the unbuffered sampler (figure 1) can be developed:

$$i = C\frac{dV}{dt}$$

$$i = C(V_O - V_I)/\Delta t = C(V_O - V_I)f$$

Rearranging the equation, the effective input resistance can be shown to be:

$$\frac{V}{i} = R = {}^{1}/_{fC}$$

From this equation it can be seen that the effective input resistance is inversely proportional to the sampling clock frequency. This indicates that if this sampler is part of an A/D converter which can operate over a wide range of clock frequencies, that as the device is operated at higher frequencies the input resistance goes down. This results in higher input current. Errors can be introduced because of the source impedance of the

external driving circuitry. Circuit behavior should be fully evaluated at whatever clock rate the circuit is going to be operated.

The coarse charge buffered sampler is shown in Figure 3. When the coarse switch is on (fine is off), the buffer coarse charges the capacitor to a voltage approximately equal to the input source voltage V_I. The advantage of the buffer is that the majority of the charging current needed to charge C is supplied by the coarse charge buffer and not by the signal source. This greatly reduces the current demand from the source outside the chip. The actual voltage output from the buffer will include whatever offset voltage exists in the buffer. When the coarse switch is off and the fine switch is on, the signal source will supply the current necessary to charge the sampling capacitor to its final value.

From the circuit the following equation can be derived for the input current:

$$i = V_{OS}/(1/fC) = fC\ V_{OS}$$

where 1/fC is the effective resistance of the switched capacitor circuit.

The equation indicates that the input current is independent of the input voltage and is a constant current which is a function of the sampling capacitor, the operating frequency, and the offset voltage of the buffer. Note that the polarity of the input current is affected by the polarity of the coarse charge buffer's offset voltage.

It is easy to see the advantage of a buffered sampler over an unbuffered sampler. In the buffered version of the sampling circuit, the signal source must furnish only enough charge to compensate for the offset of the buffer; whereas in the unbuffered sampling circuit (Figure 1), the signal source must furnish all of the charge necessary to charge the sampling capacitor.

This discussion has assumed that the sampling capacitor in each of the sampling circuits is fully discharged each time it is connected to the output circuit. Sometimes the output circuit is designed in such a way that it leaves the sampling capacitor charged at some particular voltage. This will affect the amount of charge that the unbuffered sampling circuit requires from the signal source.

The behavior of these sampling circuits will be affected if additional components are added between the outside driving amplifier and the input to the sampler. Two possible situations will be examined. First, the effect of adding a series resistance between the external drive amplifier and the A/D input will be investigated. Then the effect of adding a series resistor and a filter capacitor between the driving amplifier and the A/D input will be examined.

5

Effects of an External Resistor

Using the circuit illustrated in Figure 4, the behavior of the coarse charge buffered sampler will be examined with a resistor added between the output of the external signal source and the input

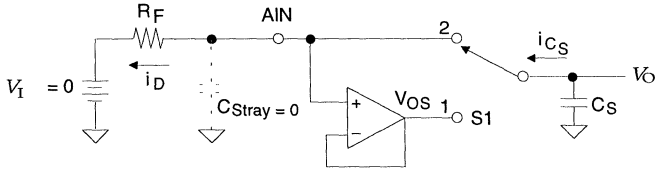


Figure 4. Buffered Sampler with External Source Resistance.

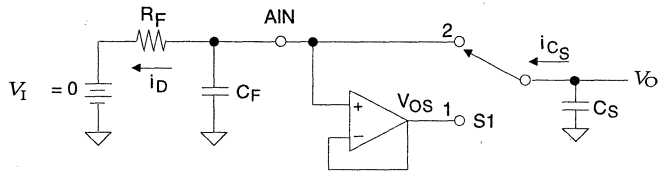


Figure 5. Buffered Sampler with External RC Filter.

to the sampler (Similar equations could be developed for the unbuffered sampler, but will not be done here). Assume that the input voltage $V_I = 0$ (the result will be the same for any constant input signal as the offset of the buffer is what dictates the charge requirement to settle the sampling capacitor to its final value). When the switch is in position 1, the sampling capacitor is charged to the voltage at the output of the internal buffer. Assume the offset of the buffer is such that the voltage on the sampling capacitor is a positive value, which will be called Vos. When switch S1 changes to position 2, the voltage on the sampling capacitor discharges to zero through the external source resistance (and the resistance of the switch if its value is significant relative to RF).

The internal sampling circuit will settle to full accuracy in the time that switch S1 is in position 2 if the external source resistance (R_F) is sufficiently low. The time available for settling is a function of the clock running the sampler. The sampler is usually connected to the input pin for one half clock cycle of the master clock. If the external resistance is too large, the sampling capacitor will be left with an error voltage when the sample time ends.

If the time that switch S1 is in position 2 is one half of a clock cycle, the voltage on C_S will discharge exponentially through source resistance R_F for t/2 where t is the period of one full clock cycle. The maximum source resistance for a given error voltage V_E is:

$$V_O = V_{OS}\, e^{-\frac{t}{2}/R_F C_S}$$

$$\ln\left(\frac{V_E}{V_{OS}}\right) = \frac{-t/2}{R_F C_S}$$

$$\ln\left(\frac{V_{OS}}{V_E}\right) = \frac{t/2}{R_F C_S}$$

$$R_{F_{max}} = \frac{1}{2f\, C_S \ln\left(\frac{V_{OS}}{V_E}\right)}$$

Effects of an External RC Filter

The case with an RC-filter placed at the input of the sampler will now be examined. Figure 5 illustrates this case.

The circuit will be analyzed with $V_I = 0$ (the result will be the same for any constant input signal as the offset of the buffer is what dictates the charge requirement to settle the sampling capacitor to its final value). When the switch is in position 1, the sampling capacitor is charged to the voltage at the output of the buffer. Assume the offset of the buffer is such that the voltage on the sampling capacitor is positive value called Vos. When at steady state

$V_{C_S} = V_{OS}$ S1 is in position 1.

$V_{C_S} = V_{C_F}$ S1 is in position 2.

The charge transfer rate from C_S to C_F during each clock cycle is

$$\Delta q = C_S(V_{OS} - V_{CF})$$

Since $i = \frac{\Delta q}{\Delta t}$, $i_{CS} = \frac{C_S (V_{OS} - V_{CF})}{\Delta t}$ and $\frac{1}{\Delta t} = f$;

Therefore $i_{CS} = f C_F(V_{OS} - V_{CF})$

In the steady state condition,

$$i_{CS} = i_D$$

Therefore

$$V_{CF}/R_F = f C_S(V_{OS} - V_{CF})$$

where V_{CF} is the error voltage V_E.

Therefore, for a given error voltage the maximum R_F should not exceed

$$R_F \leq \frac{V_E}{f C_S(V_{OS} - V_E)}$$

The equation applies only if

$$f >> \frac{1}{RC}$$

An external RC filter in front of the sampler lowers the bandwidth of the circuit and therefore reduces input noise. It also acts to isolate the transient current demand of the sampler from the external drive amplifier by allowing the sampler to draw its transient current out of the filter capacitor. This greatly reduces the transient current seen by the drive amplifier. Therefore, the amplifier is less likely to ring or overshoot due to the transient load. Adding an external RC filter can be detrimental if it has an excessively long time constant. This can cause the source resistance of the filter to introduce an offset error.

When an external amplifier drives either the unbuffered, or the buffered sampler directly, the amplifier may have difficulty with the transient load conditions. The transient load may cause the amplifier to exhibit ringing or oscillation. The behavior of the amplifier may vary as the signal amplitude changes; with the most common problems occurring with signals near zero crossover. A common symptom is for a user of a high speed A/D converter to suspect the converter of having a nonlinearity or of having missing codes in its transfer function; but the actual problem is that the driving amplifier is ringing and failing to settle at the proper signal level before the sample capacitor captures the signal. Some amplifiers will have more difficulty than others. An amplifier which exhibits peaking in its closed loop response will generally have more problems. To minimize the possibility of ringing, choose an amplifier which has gain rolloff which is linear for at least one decade of frequency above the frequency where the closed loop gain intersects with the open loop gain response. The amplifier circuit should be chosen or designed to achieve low output impedance at the sampling frequency of the capacitive sampler. A wideband amplifier with good drive current capability works best with a high speed A/D. The transient load seen by any amplifier can be reduced if an RC filter is added between the output of the operational amplifier and the input to the switched-capacitor sampler. The values for the resistor and capacitor are usually recommended by the A/D manufacturer. Making the time constant too large can reduce settling accuracy or produce an offset error in the circuit.

5

Other Circumstances Which Alter Input Behavior

Various A/D converter input structures have been discussed. It has been shown that the input seen by the external driver depends upon the size of the sampling capacitor, the sampling frequency, and whether or not the input is coarse charge buffered. The effect of an external source resis-

tance and the effect of an external RC filter have been discussed.

There are additional circumstances which can affect the input impedance. From the equation for the switched capacitor input impedance (R = 1/fC) it is readily understood that the dynamic load will change if the clock frequency to the sampler is changed. There are several conditions in which this can occur. The most common condition is that the master clock to the converter is modified. An example of this occurs in some applications of the CS5501/CS5503 converters. The CS5501/CS5503 converters include a low pass digital filter which has a -3 dB corner frequency of 10 Hz when operated with a master clock frequency of 4.096 MHz. If the clock frequency to the converter is lowered the corner frequency is reduced proportionately. Some measurement systems allow the user to select a slower converter clock to reduce the noise band width of the converter. This allows the converter bandwidth to be optimized for the noise conditions in the circuit. This change in clock rate will change the behavior of the input of the converter. This change in dynamic behavior can interact with the external driving circuitry and introduce errors in the measurement.

Input impedance can also change due to sampling clock changes which occur in converters that allow the user to modify the output word rate of the converter. Some first generation audio codecs would change the sample clock of the input stage whenever a different word rate was selected. Newer codecs keep the input stage sampling clock constant when the output word rate is changed.

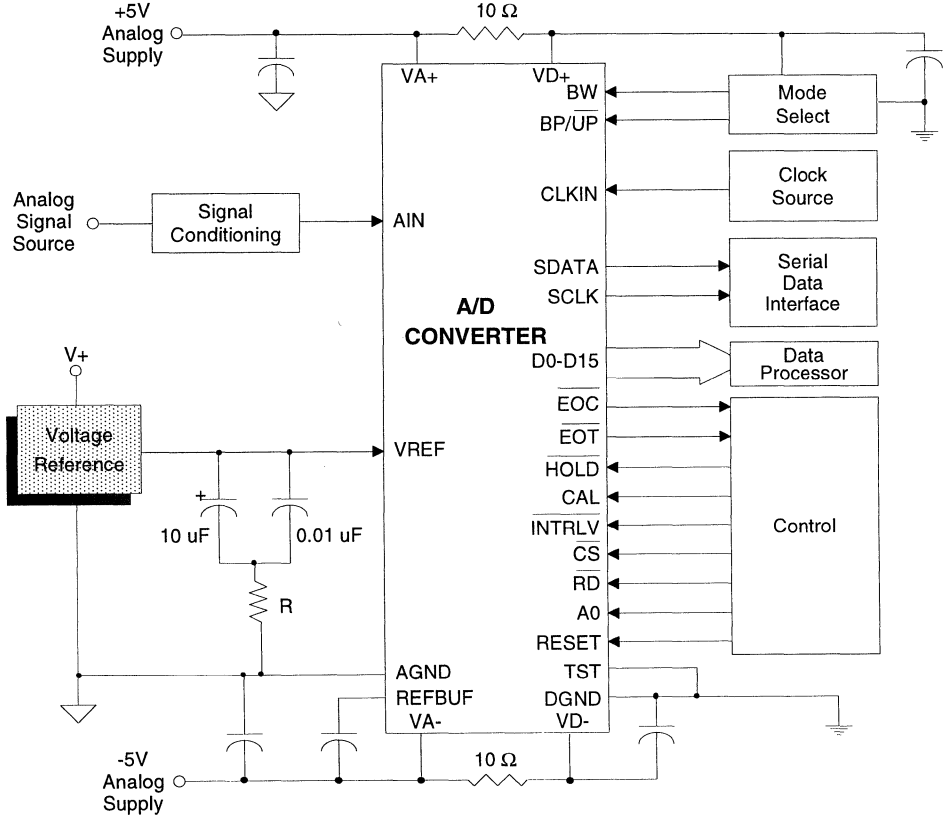
Another example of the converter's input impedance being affected, can occur in instrumentation converters which include a PGA (Programmable Gain Amplifier) stage as part of the input stage of the converter. These converters allow the gain to be modified by changing the size of the sampling capacitor, or by modifying the sample rate of the capacitor sampler. Either of these will alter the converter's input impedance if the gain change is performed at the input stage of the converter. The CS5516 and CS5520 include a PGA, but it is placed after an input instrumentation amplifier. The instrumentation amplifier input impedance remains constant when the PGA gain is changed. Products from other vendors modify the input stage to accomplish gain changes and therefore alter the input impedance of the converter.

This application note has discussed the drive requirements of CMOS A/D converters. While the discussion has been applied to the input for the signal to be converted, realize that this discussion can apply to the voltage reference input pins of the converter as well.

Application Note

Voltage References for the CS5012A / CS5014 / CS5016 / CS5101A/ CS5102A / CS5126 Series of A/D Converters

by
Bruce Del Signore & Steven Harris



5

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 462-2723

INTRODUCTION

This application note discusses voltage references for use with Crystal Semiconductor's successive approximation series of A/D converters. Reference design considerations, a design example and suggested reference circuits are explained in detail.

Voltage references provide accurate voltages for use in data acquisition systems in order to establish a basis for conversion. In a data acquisition system, the value of the reference sets the gain of the A/D stage since the digital output corresponds to the ratio of the analog input signal to the reference voltage.

In static applications, information is contained in the signal amplitude, therefore the absolute value of the reference voltage is important. In many signal processing applications, information is contained in the frequency and phase of the signal. Here, absolute value is not as important as the stability of the reference voltage during conversion.

Zener-diode Reference

There are two major varieties of voltage references. The first is the zener-diode based reference which uses a reverse-biased zener diode operated in its breakdown region. Most reference zeners breakdown at voltages between 6.0 and 7.0V, which limits the minimum supply voltage necessary for operation. When the diode is supplied with a constant current, it has a constant voltage drop. Zener references use a zener diode and an integrated feedback amplifier which provides constant current, gain, and buffering for the zener diode.

Zener diodes exhibit two types of breakdown. The first is zener breakdown which has a negative temperature coefficient and is dominant at low current levels. The second, avalanche breakdown, occurs at higher current levels and has a positive temperature coefficient. At some specific current level, these two effects cancel each other and the temperature coefficient of the zener breakdown voltage is zero. As the ambient temperature changes, one of the breakdown mechanisms becomes dominant and the the reverse-biased diode voltage will exhibit a temperature coefficient.

Bandgap Reference

The second major type of reference is the bandgap reference. This reference uses the base-emitter voltage (V_{be}) of a bipolar transistor as a basis for operation. The V_{be} has a negative temperature coefficient (-2mV/°C). This negative temperature coefficient is balanced by a voltage with a positive temperature coefficient of the same magnitude. This voltage is usually obtained by using the difference of two V_{be}'s of transistors operating at different current densities. When both voltages are scaled and summed together, the result is a voltage which is less sensitive to temperature. The headroom required for bias and support circuitry is only a few volts over the output voltage.

Reference Specifications

Voltage references have six important specifications. These are absolute accuracy, temperature coefficient, long-term reference drift, power supply sensitivity, output impedance, and output noise.

Absolute or untrimmed accuracy is the difference between the actual output voltage and the ideal output voltage. It is specified in millivolts.

Temperature coefficient describes the drift in the output voltage with temperature. Since this drift is nonlinear, curve fitting is often used for all temperatures between those actually tested. Voltage references are available with temperature coefficients as low as 1 ppm/°C. Inexpensive references are available with 10 to 50 ppm/°C drift

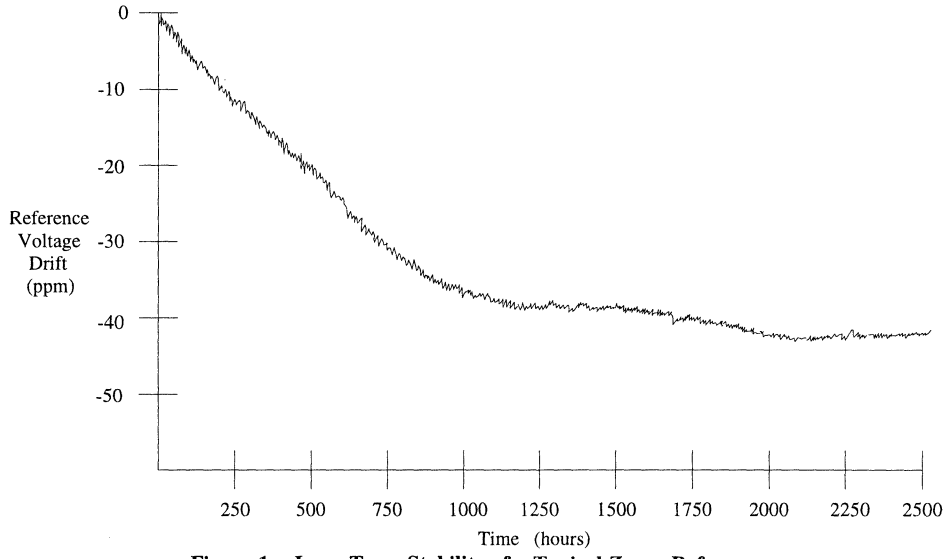


Figure 1. - Long Term Stability of a Typical Zener Reference

which is comparable to on-chip references of bipolar A/D converters. Temperature coefficient is specified in ppm/°C.

Long term stability is the drift in the reference voltage over time. Most references show minor deviations in voltage due to 1/f noise in circuit components. These deviations are usually small and are superimposed on a larger drift characteristic which is due to device aging. An example of this is seen in Figure 1. Long term drift is specified in ppm/1000 hrs.

Power supply sensitivity (line regulation) is the change in output voltage due to a change in power supply. Most references have good power supply rejection at dc, but ac power supply rejection is also important when power supplies are subject to high frequency coupling or noise spikes. PSRR (Power Supply Rejection Ratio) is the ratio of the change in power supply to the change in output voltage. It is specified in dB.

Output impedance is important because of the dynamic loads generated by successive-approximation A/D converters. When the reference is sourcing or sinking current, its output voltage will change due to non-zero output impedance. This impedance must be low enough at all frequencies of interest so the deviation in reference voltage when sourcing current is negligible. Output impedance is specified in ohms.

Output noise can lead to comparison errors in the A/D converter, and subsequently conversion errors. Reference noise is more evident with full scale inputs. It is specified in μV peak-to-peak.

5

Design Considerations

When interfacing a voltage reference to an A/D converter, the specifications should be robust enough so that the reference does not become a source of conversion error. During conversion, each capacitor of the calibrated capacitor array in the ADC is switched between VREF and AGND in a manner determined by the successive approximation algorithm. The charging and discharging of the array results in a current load at

the reference. The ADC's include an internal buffer amplifier to minimize the external reference circuit's drive requirement and preserve the reference's integrity. Whenever the array is switched during conversion, the buffer is used to pre-charge the array thereby providing the bulk of the necessary charge. This buffer enlists the aid of an external 0.1µF ceramic capacitor which must be tied between its output, REFBUF, and the negative analog supply, VA-. The appropriate array capacitors are then switched to the unbuffered VREF pin to avoid any errors due to offsets and/or noise in the buffer. The external reference circuitry need only provide the residual charge required to fully charge the array after pre-charging from the internal buffer. This creates an ac current load as the ADC sequences through conversions.

The reference circuitry must have a low enough output impedance to provide the requisite current without changing its output voltage significantly. As the analog input signal varies, the switching sequence of the internal capacitor array changes. The current load on the external reference circuitry thus varies in response with the analog input. Also with CS5012,4,6 converters, bits are converted at a 1MHz rate with a full speed (4MHz) clock. The reference must settle within one microsecond so that it will be accurate before the next bit is converted. Signal amplitude dependent loading and conversion settling time require the output impedance of the reference to remain low from dc to at least 1MHz in order to ensure good converter performance.

The CS5012,4,6 series of converters can operate with a wide range of reference voltages, but signal-to-noise performance is maximized by using as wide a signal range as possible. All CS5012,4,6 converters can actually accept reference voltages up to the positive analog supply. However, the internal buffer's offset may increase as the reference voltage approaches VA+. This increases external drive requirements at VREF. Allowing 250mV headroom for the internal reference buffer is recommended. If the supplies are regulated specifically for the converter, 5.0 volt references may be used if the supply voltages for the ADC are kept between ± 5.25 and ± 5.5 volts.

The magnitude of the current load presented to the external reference circuitry by the ADC's will vary with the master clock frequency. At full speed (4MHz clock), the ADC's require maximum load currents of 10µA peak-to-peak (1µA peak-to-peak typical). The voltage reference must supply this current and maintain adequate voltage regulation. The load currents scale proportionately with the master clock frequency. Slower clocks can be used to relax maximum output impedance specification of the reference.

When driving multiple A/D converters from the same reference circuit, load currents will scale proportionally to the number of converters. Distribute the required decoupling components such that each ADC is locally decoupled.

A reference with a maximum output impedance of 2 Ω will yield a maximum error of 20µV. This reference could drive a CS5016 (LSB=69µV with

Part # / f_{clk}	4MHz	2MHz	1MHz	500kHz
CS5012 (Vref=4.5V)	27	54	108	216
CS5012 (Vref=2.5V)	15	30	60	120
CS5014 (Vref=4.5V)	7	14	28	56
CS5016 (Vref=4.5V)	2	4	8	16

All units in ohms

Table 1. - Maximum Output Impedance for ≈ 1/4 LSB Reference Deviation

a 4.5V reference) and maintain approximately 1/4 LSB deviation during conversion. Similarly for the CS5014 (LSB=276µV with a 4.5V reference), and CS5012 (LSB=613µV with a 2.5V reference), maximum impedances of 7 and 15 Ω respectively will maintain adequate regulation. Table 1 defines maximum reference impedances allowed for each of the Crystal A/D's operating at different master clock frequencies in order to keep reference deviation approximately equal to 1/4 LSB.

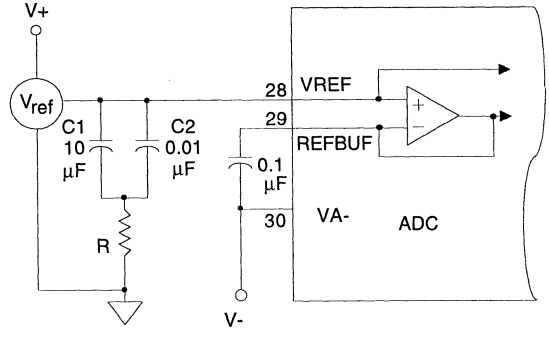
All precision references exhibit extremely low output impedance at dc. However, as frequency increases the impedance also increases. A large capacitor connected between VREF and AGND can provide sufficiently low output impedance at the high end of the frequency spectrum where the reference impedance is too high.

For example, the impedance of an ideal 10µF capacitor drops below 1 Ω at frequencies greater than 16kHz. However, actual capacitors behave differently due to their physical structure. Tantalum-foil electrolytic capacitors begin to appear inductive at frequencies around 100kHz and as a result their impedance begins to rise at frequencies above this. Aluminum electrolytic capacitors appear inductive at frequencies around 10kHz. Ceramic-disk capacitors behave much closer to ideal and begin to appear inductive at frequencies around 5MHz, but 10µF ceramic-disk capacitors are quite rare. Therefore, a high-quality tantalum capacitor (10µF) in parallel with a smaller (0.1µF) ceramic capacitor is recommended. This combination yields low impedance up to frequencies around 50MHz.

Peaking

The presence of large capacitors on the output of some voltage references may cause peaking in the output impedance at intermediate frequencies. Care should be exercised to ensure that significant peaking does not exist or that some form of compensation is provided to reduce it.

Most commercially available references use an integrated op-amp to buffer the actual reference generator. External capacitive loading will degrade performance of this op-amp. This degradation can be analyzed using classical analysis techniques. The open loop gain of an ideal op-amp is primarily determined by the internal compensation capacitor which generates a left-half-plane-pole (LHPP) at a very low frequency. The effect of this pole is to reduce the open loop gain by 20dB per decade and to add a -90 degree phase shift to the open loop transfer characteristic. Adding a capacitive load to the output of the op-amp generates another LHPP at a frequency inversely proportional to the capacitor's value. An additional 20dB per decade reduction in gain and -90 degree phase shift result from the second LHPP.



$$R = \frac{1}{2\pi (C_1 + C_2) f_{peak}}$$

Figure 2. - Reference Connections

The unity gain bandwidth of an op-amp (f_0), is the frequency at which the open loop gain goes to unity. If the total phase shift reaches -180 degrees before f_0 is reached the op-amp will become unstable. The closed loop frequency response peaks at f_0. As the total open loop phase shift at f_0 approaches -180 degrees, the closed loop peak at f_0 approaches infinity. The point of critical damping is the point where the peaking is precisely zero. Any phase shift less than this results in no peaking, and phase shift greater than this results in increased peaking.

Any peaking that might occur can be reduced by placing a small resistor in series with the capacitors (Figure 2). This resistor adds a left-half-plane-zero (LHPZ) to the open loop characteristic of the op-amp. This zero increases the gain by 20dB per decade, and adds a +90 degree phase shift. The resulting reduction in total phase shift at f_0 reduces peaking in the closed loop characteristic. The equation in Figure 2 can be used to help calculate the optimum value of R for a particular reference. The term "f_{peak}" is the frequency of the peak in the output impedance of the reference before the resistor is added.

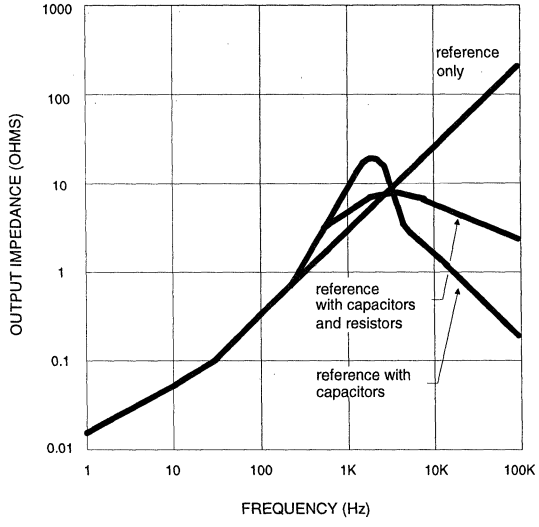


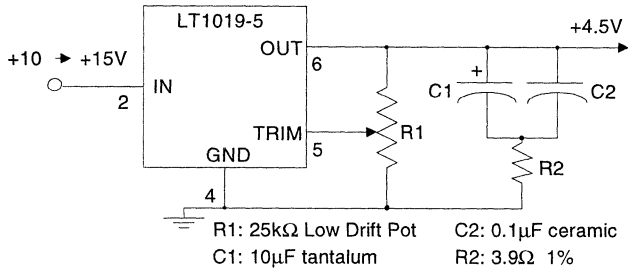
Figure 3. - Output Impedance Curves for LT1019-5

Design Example

Figure 3 shows the output impedance characteristic of an LT1019-5 reference trimmed to 4.5V. The three curves represent impedances of the stand-alone reference, the reference with a 10µF tantalum and a 0.1µF ceramic capacitor added in parallel to the output, and the reference with the capacitors and a 2.2 Ω resistor in series with them (See Figure 2). Without loading, the reference impedance rises above 100 Ω at 50kHz. Adding the capacitors, peaking can be seen, but the maximum impedance is about 13 Ω at 4kHz. As shown in Table 1, 13 Ω is sufficient for use with the 12-bit converters and for the 14 and 16-bit converters with slow master clocks. With the addition of the 2.2 Ω resistor, the peak is reduced to 6 Ω and the impedance approaches 2.2 Ω at high frequencies.

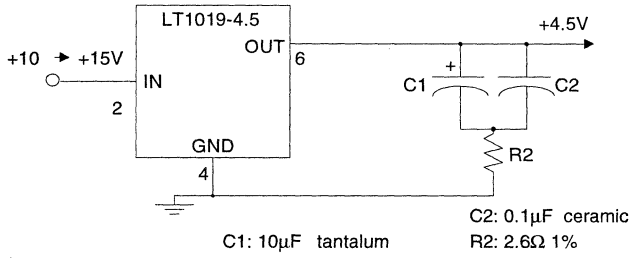
Suggested Voltage Reference Circuits

Nine reference circuits were characterized for use with the CS5012, CS5014, CS5016, CS5101, CS5102, CS5126 family of successive-approximation A/D converters. Important reference specifications such as output impedance and drift were measured for all references using standard test techniques. In addition, a Fast-Fourier Transform (FFT) test was performed to characterize the total dynamic performance of each reference circuit while driving a CS5016 converter. The same CS5016 was used for all tests yielding results which allow the comparison between different references. A summary of performance can be seen in the table at the end of this application note. During the FFT test, a pure sine wave is applied to the CS5016 and a "time record" of 1024 samples is captured and processed. The FFT algorithm analyzes the spectral content of the waveform and distributes its energy among 512 "frequency bins". Distribution of energy in bins outside of the fundamental and dc can be attributed to errors in the A/D converter's performance, the reference, or the input sine wave.



Reference Type	Bandgap
Untrimmed Accuracy	2.5mV
Max Impedance	6.5Ω @ 3.2KHz
Total Output Drift	5ppm / °C
PSRR (50Hz to 500Hz)	90dB
Long Term Stability	-
Output Noise (dc to 1MHz)	250µV p-p
S / (N+D) (100Hz)	89dB
S / (N+D) (1kHz)	89dB

Figure 4. LT1019-5 Reference Trimmable to 4.5V



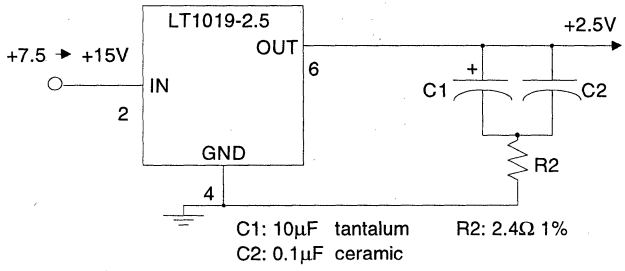
Reference Type	Bandgap
Untrimmed Accuracy	3.0mV
Max Impedance	3.1Ω @ 6.1KHz
Total Output Drift	5ppm / °C
PSRR (50Hz to 500Hz)	90dB
Long Term Stability	-
Output Noise (dc to 1MHz)	150µV p-p
S / (N+D) (100Hz)	91dB
S / (N+D) (1kHz)	90dB

Figure 5. LT1019-4.5 Reference

The result of the FFT test is the ratio of input signal amplitude to the combination of harmonic distortion and total integrated noise. It is referred to as S/(N+D) in all of the performance charts in Figures 4 to 10. This ratio is expressed in dB. If input sine wave distortion and the actual A/D converter's distortion and noise are assumed to be negligible, the S/(N+D) is due to the reference only. In reality, this assumption can not be made. In the case of the Great Reference (See Figure 11), performance matches or exceeds the capability of the test setup. S/(N+D) ratios of 72 and 82 dB are sufficient for the 12-bit and 14-bit converters. For the 16-bit converters, 88 to 94 dB is necessary.

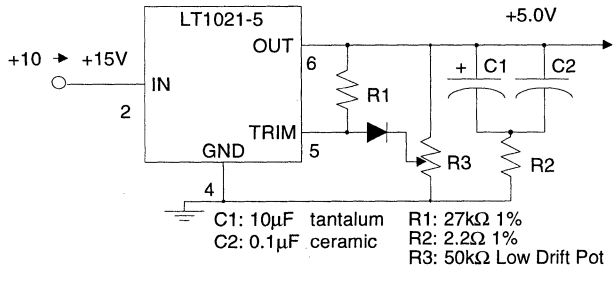
FFT tests were performed at 100Hz and 1kHz. The 100Hz test checks the output impedance of the reference chip itself which dominates at low frequencies. The 1kHz FFT test checks the output impedance at intermediate frequencies in the kHz range. The highest output impedance was seen in all references at these intermediate frequencies. Since the reference capacitors dominate the impedance at high frequencies, high frequency FFT tests were not necessary. Although not tested, the best reference is likely to yield the best DNL performance.

The least complicated reference circuit is the stand-alone reference chip with a passive compensation network. Its temperature drift and noise performance is equal to the reference chip itself since the compensation network does not change the dc output voltage. Keeping the output impedance low from dc to 1MHz is not trivial however, since there is no additional active circuitry added to perform this task. Five references were tested in the stand-alone configuration. Figures 4, 5, 6, 7, and 8 illustrate schematics and measured specifications for these references. All references are monolithic with the exception of the VRE104 reference which is a hybrid (available from Thaler (602) 742-5572). Notice that the VRE104 and the LT1019-4.5 require no trimming for 4.5V operation. The calculated value of R2 in each of



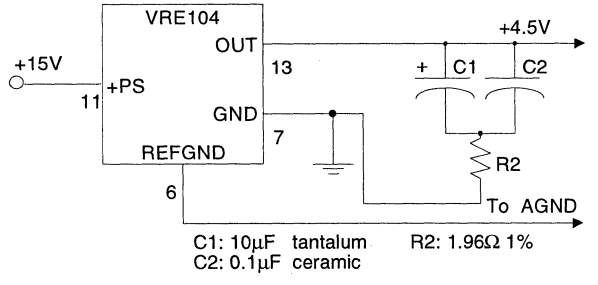
Reference Type	Bandgap
Untrimmed Accuracy	1.25mV
Max Impedance	4.0Ω @ 5.8KHz
Total Output Drift	5ppm / °C
PSRR (50Hz to 500Hz)	90dB
Long Term Stability	-
Output Noise (dc to 1MHz)	100µV p-p
S / (N+D) (100Hz)	87dB
S / (N+D) (1kHz)	89dB

Figure 6. LT1019-2.5 Reference



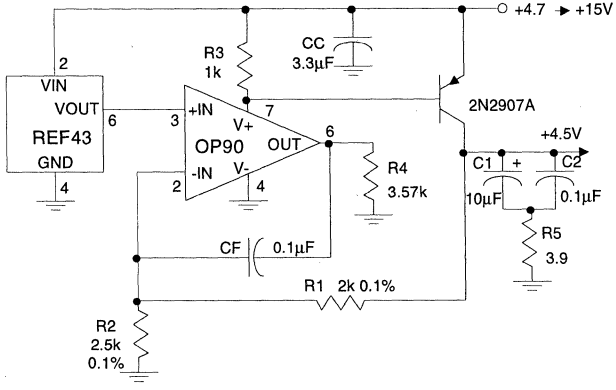
Reference Type	Zener
Untrimmed Accuracy	2.5mV
Max Impedance	3.8Ω @ 5.0KHz
Total Output Drift	3ppm / °C
PSRR (50Hz to 500Hz)	86dB
Long Term Stability	15ppm / 1000hr
Output Noise	60µV p-p
S / (N+D) (100Hz)	90dB
S / (N+D) (1kHz)	90dB

Figure 7. LT1021 Reference



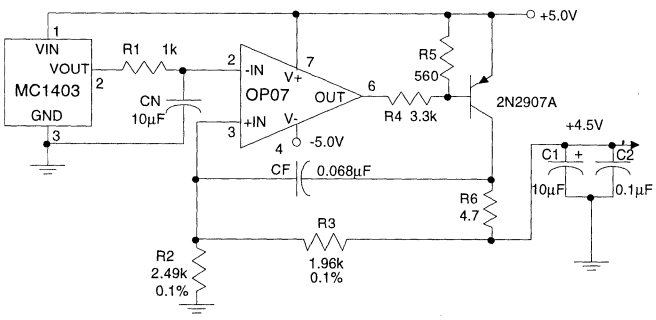
Reference Type	Zener
Untrimmed Accuracy	500µV
Max Impedance	2.5Ω @ 20KHz
Total Output Drift	0.5ppm / °C
PSRR (50Hz to 500Hz)	100dB
Long Term Stability	6ppm / 1000hr
Total Output Noise	80µV p-p
S / (N+D) (100Hz)	90dB
S / (N+D) (1kHz)	90dB

Figure 8. VRE104 Reference



Reference Type	Bandgap
Untrimmed Accuracy	1.5mV
Max Impedance	4.4Ω @ 1KHz
Total Output Drift	8.0ppm / °C
PSRR (50Hz to 500Hz)	60dB
Long Term Stability	-
Output Noise (dc to 1MHz)	400µV p-p
S / (N+D) (100Hz)	88dB
S / (N+D) (1kHz)	88dB

Figure 9. Low Power Supply Reference



Reference Type	Bandgap
Untrimmed Accuracy	50mV
Max Impedance	6.9Ω @ 2KHz
Total Output Drift	25ppm / °C
PSRR (50Hz to 500Hz)	80dB
Long Term Stability	-
Output Noise (dc to 1MHz)	30µV p-p
S / (N+D) (100Hz)	90dB
S / (N+D) (1kHz)	90dB

Figure 10. Low Headroom Reference

the references above will change slightly between units. Since the actual variation is small, picking the closest 1% tolerance resistor to the calculated value should give similar performance for all references of a particular manufacturer's model.

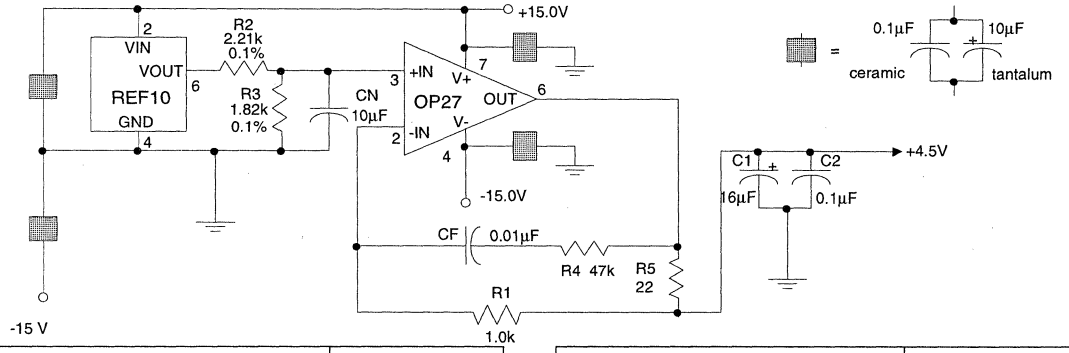
Other stand-alone voltage references with similar specifications include the AD584, REF02, REF03, REF10, and REF43. When designing with these references, the equation shown in Figure 2 should be used to calculate the appropriate value of R2 for each type of reference.

For applications which use ± 5.0 volt supplies, the reference in Figure 9 can be used. This reference circuit, designed by engineers at the former Precision Monolithics, takes advantage of a low power op-amp in a novel feedback configuration to achieve a 4.5 volt reference which operates from 4.7 to 15 volt supplies.

Since only a few microamps of quiescent current flows in the op-amp, it can be assumed that the only current flowing in R3 is the same as that flowing in R4. It can be shown that V6 = 3.57(Vin-V7). For an output of 4.5 volts, and a supply of 4.7 volts, the op-amp has a supply of approximately 4.0 volts and an output voltage of 2.14 volts. This output voltage is well within the maximum specification of the OP-90 op-amp. Other references can be substituted for the REF43 if different drift or noise specifications are required.

The reference shown in Figure 10 is a low noise reference with less than 30µV peak-to-peak of noise from dc to 1MHz. It uses a discrete output stage allowing Vref to come within 300mV of the positive supply. The filtering network R1,CN reduces the bandwidth of the reference and therefore reduces the total output noise. The OP-07 is a low noise op-amp which buffers the filtered reference. This op-amp contributes very little noise to the entire reference circuitry.

The temperature coefficient of this reference is primarily due to to the matching of the gain resistors R2 and R3, so low temperature drift resistors should be used. Long term drift is dominated by the MC1403's drift. Other 2.5 volt references can be used to improve this specification. The output voltage can be changed by adjusting R2 and R3 according to the following equation: Vref = Vout*((R2+R3)/R2). Resistors with 0.1% tolerance for R2 and R3 limit the reference's untrimmed accuracy only. Resistors with 1% or 5% tolerance can be used if untrimmed accuracy less than 50mV is not necessary. The supplies of the OP-07 should be bypassed with 0.1µF capacitors to ground.



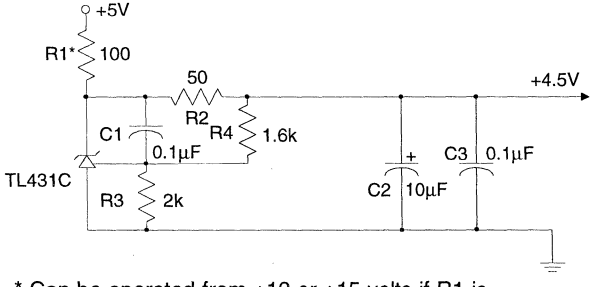
Reference Type	Bandgap
Untrimmed Accuracy	25mV
Max Impedance	0.5Ω @ 3kHz
Total Output Drift	9ppm / °C
PSRR (50Hz to 100Hz)	95dB

Long Term Stability	50ppm / 1000hr
Output Noise (dc to 1MHz)	5µV p-p
S / (N+D) (100Hz)	92dB
S / (N+D) (1kHz)	92dB

Figure 11. - Great Reference

The reference in Figure 11 exhibits very good noise, output impedance, and long term drift performance. It can be used in applications which have ± 15 volt supplies available. The reference has noise less than 10µV peak-to-peak from dc to 1MHz. The filtering network R2, R3, and CN filters noise components greater than 10Hz from the output of the REF10 reference. The OP-27 is a very low noise op-amp with excellent input offset drift over time and temperature.

The temperature coefficient of this reference is primarily due to the matching of the voltage divider R2 and R3, assuming that an appropriate low leakage capacitor is chosen for CN. Matched, low temperature drift resistors should be used when absolute accuracy is required. Temperature drift of the reference chip plus input offset drift of the op-amp is about 9ppm/°C. Other 10 volt references can be used in place of the REF10.



* Can be operated from +12 or +15 volts if R1 is changed to 2K.

Reference Type	Bandgap
Untrimmed Accuracy	30mV
Max Impedance	50 Ω @600Hz
Total Output Drift	30ppm/ ℃
PSRR (50Hz to 500Hz)	85dB
Long Term Stability	-
Output Noise (dc to 1MHz)	100uV p-p
S / (N + D) (100Hz)	92dB
S / (N + D) (1kHz)	91dB

Figure 12. -TL431 Shunt Reference

The reference voltage can be changed by adjusting R2 and R3 according to the following equation. Vref = Vout*(R3/(R2+R3)).

This circuit has no protection against accidentally applying ± 15V to the VREF pin. This could occur if the OP27 fails.

For applications where good dynamic performance is required, but only moderate dc accuracy, the TL431 shunt reference is an inexpensive solution. Figure 12 shows an example circuit, along with the excellent dynamic performance numbers.

Miscellaneous Applications Information

Noise from the voltage reference element may reduce system performance. Bandgap references tend to generate much more noise than zener diodes. To obtain the best noise performance from the reference element, it should be band-limited. Note the broadband noise for the LT1019-5 circuit (Figure 4, 250μV) versus the noise of a similar bandgap reference with additional circuitry to band-limit the noise as in the Great Reference (Figure 11, 10μV).

Thermal temperature gradients due to power dissipation on the voltage reference die can create output voltage shifts. Keeping the entire chip on an isothermal plane is helpful. Reference load conditions should be kept very close to those specified, or degraded temperature performance will result. Some references specify a thermal regulation in ppm/mW. This can be used to calculate voltage drift for a specific power dissipation due to loading.

Overall die temperature change can cause thermally induced output voltage variations which can exceed electrical effects. Shifts in power dissipation on the board level are the major contributor to this error. In critical applications, using a heat-sink is recommended to keep the reference temperature deviations small.

Thermocouple effects between package leads can also cause excessive output voltage drift and noise. Differences between materials in IC leads and PC-board traces can cause thermoelectric effects. Ambient air turbulence around the leads causes mismatches in the temperature between the package leads. The resulting thermoelectric voltage contributes to noise. Using dual in-line packages (DIPs) is recommended over using TO-5 type packages. The copper or Alloy 42 lead frames on DIPs are much less sensitive to thermocouple effects than the Kovar leads of the TO-5 packages. Using an enclosure such as a polysulfone shield which blocks the air flow over the reference package will also reduce the problem by reducing air movement around the package leads.

In reference circuits which have external gain setting resistors, tracking of the temperature coefficients of these resistors is vital. Wirewound resistors made of Evenohm or Mangamin have the lowest temperature coefficients. Ceramic film resistors such as Vishay are also good. Matching in resistor temperature coefficients as good as 0.4 ppm/°C can be achieved. Arranging these resistors in close proximity to one another also helps matching. SIP or DIP resistors by Beckman and Vishay exhibit the best matching since all resistors are processed on the same substrate.

Reference	Type	Untrimmed Accuracy	Maximum Impedance	Output Drift	PSRR (50Hz to 100Hz)
LT1019-5	Bandgap	2.5mV	6.5 Ω @ 3.2kHz	5ppm / °C	90dB
LT1019-4.5	Bandgap	3.0mV	3.1Ω @ 6.1kHz	5ppm / °C	90dB
LT1019-2.5	Bandgap	1.25mV	4.0Ω @ 5.8kHz	5ppm / °C	90dB
LT1021-5	Zener	2.5mV	3.8Ω @ 5.0kHz	3ppm / °C	86dB
VRE104	Zener	500µV	2.5Ω @ 20kHz	0.5ppm / °C	100dB
Low Supply	Bandgap	1.5mV	4.4Ω @ 1kHz	8ppm / °C	60dB
Low Headroom	Bandgap	50mV	6.9Ω @ 2kHz	25ppm / °C	80dB
Great	Bandgap	25mV	0.5Ω @ 3kHz	9ppm / °C	95dB
TL431 Shunt	Bandgap	30mV	50Ω @ 600Hz	30ppm / °C	85dB

Reference	Long Term Stability*	Output Noise (dc to 1MHz)	S/(N+D) (100Hz)	S/(N+D) (1kHz)
LT1019-5	-	250µV p-p	89dB	89dB
LT1019-4.5	-	150µV p-p	91dB	90dB
LT1019-2.5	-	100µV p-p	87dB	86dB
LT1021-5	15ppm / 1000hr	60µV p-p	90dB	90dB
VRE104	6ppm / 1000hr	80µV p-p	90dB	90dB
Low Supply	-	400µV p-p	88dB	88dB
Low Headroom	-	30µV p-p	90dB	90dB
Great	50ppm / 1000hr	10µV p-p	92dB	92dB
TL431 Shunt	-	100µV p-p	92dB	91dB

*Taken from reference data sheets. All other parameters were measured.

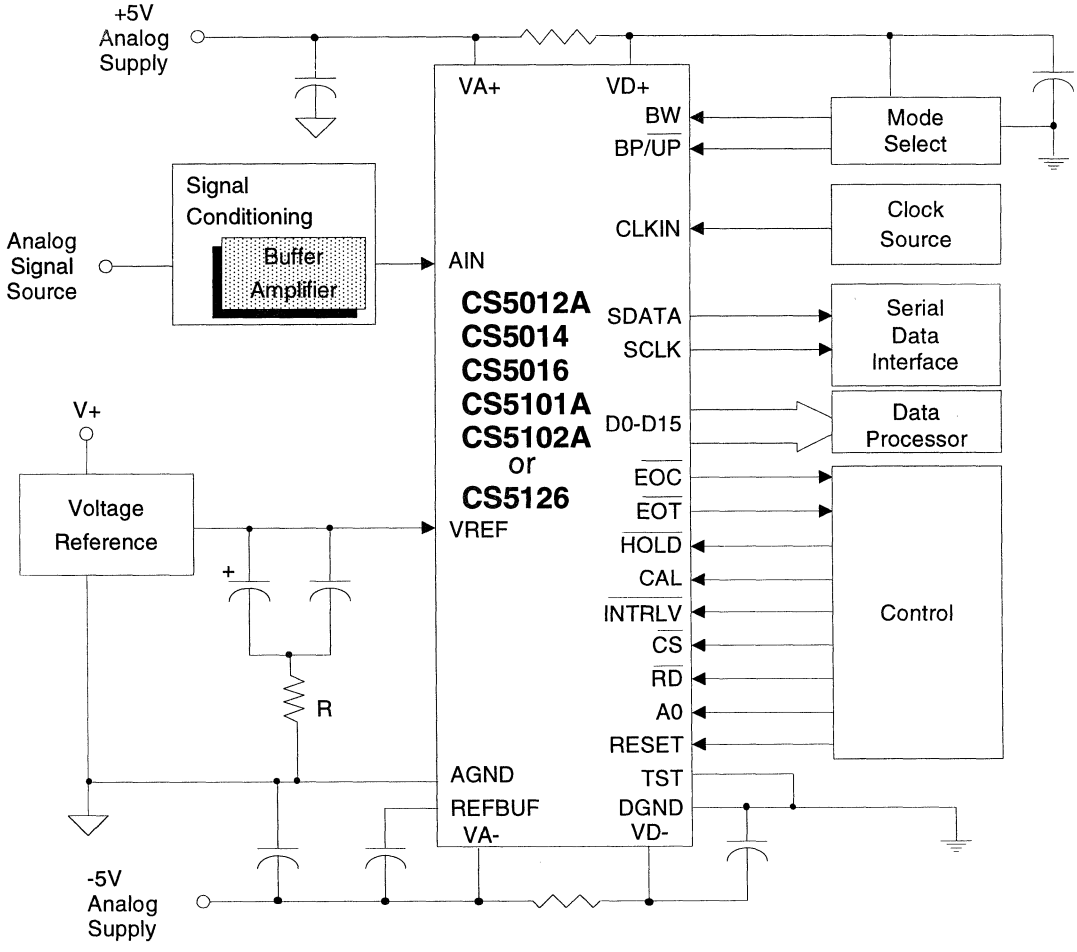
Performance Comparison Table

Semiconductor Corporation

Application Note

Buffer Amplifiers for the CS5012A/CS5014/CS5016/ CS5101A/CS5102A/CS5126 Series of A/D Converters

by
Jerome Johnston



5

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX 445-7581

TABLE OF CONTENTS

Introduction

This application note discusses buffer amplifiers for use with Crystal Semiconductor's CS5012, CS5014, CS5016, CS5101A, CS5102A or CS5126 A/D converters. Amplifier design considerations are discussed and several circuits are proposed.

Signal Requirements for Analog to Digital Converters

Crystal Semiconductor is a source for a variety of monolithic A/D Converters. While the type of design configuration of the converters may differ, their uses could be classified into two general categories: those which require specifications in static measurement applications; and those which require specifications for signal processing or dynamic signal measurement applications.

The capability of a converter to achieve a stated static measurement requirement is generally defined by its linearity error specifications, both integral and differential, and by its offset error and gain error specifications. To assess the total error in a static measurement, the effects of temperature on the offset, gain, and linearity errors must also be investigated. In static measurement systems, these same error sources need to be scrutinized in the signal conditioning circuitry as well.

When a converter is used in dynamic signal measurement applications (generically known as "signal processing"), its signal measurement capability is indicated by specifications such as total harmonic distortion, signal to noise ratio, and signal to peak harmonic or spurious noise. Signal processing designers generally evaluate the error contribution of the signal conditioning circuitry in terms of these same parameters.

Signal conditioning circuitry generally includes all circuitry from the transducer or the signal source up to the A/D converter. This application note will concern itself primarily with the requirements of the amplifier which immediately precedes the A/D converter. This amplifier will be called a buffer amplifier.

In the design of an A/D converter system, the buffer amplifier can be a source of significant errors. The significance of these errors can only be assessed if the circuit configuration is thoroughly analyzed for its total error contribution. A thorough analysis requires a good understanding of amplifier specifications, of the limitations of the different circuit configurations, and of the benefits and limitations of feedback. A good place to begin is with a review of feedback theory.

I. OPERATIONAL AMPLIFIERS: Review Of Theory

Feedback Control Theory

The goal in using feedback is to establish a closed-loop system whose operating characteristics are primarily determined by the choice of the feedback elements. The extent to which this goal can be accomplished is explained by feedback control theory. Figure 1 illustrates the

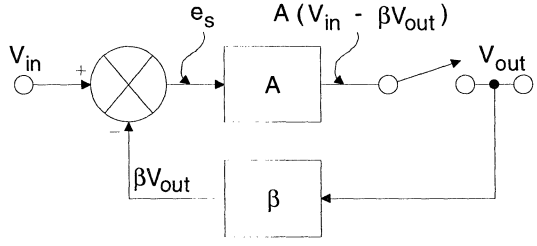


Figure 1. The Classic Feedback Control Loop

classical feedback control loop. The equations which describe this control loop are directly applicable to the noninverting operational amplifier circuit.

The control loop consist of an input voltage differencing section whose output is amplified by a positive gain section. A fractional part of the signal output is then returned to the negative terminal of the differencing section though the feedback network. The input differencing section, indicated by the circle with the X in it, determines the difference in the signals at the (+) and (-) inputs. The difference is indicated by an error signal of the quantity:

$$e_S = (V_{in} - \beta V_{out})$$

Equation 1

which is then amplified by the open-loop voltage gain of the amplifier:

$$A (V_{in} - \beta V_{out}) = V_{out}$$

Equation 2

The amplifier open-loop gain is represented in Figure 1 by the box with the A in it. The feedback portion of the loop is represented by the box with the β in it. β is defined as the feedback attenuation factor and its value is that fractional part of the output voltage which is fed back to the input. Equation 2 can be manipulated to give:

$$A_{CL} = \frac{V_{out}}{V_{in}} = \frac{A}{1 + A\beta}$$

Equation 3

This is the key equation in the feedback system. Equation 3 indicates that the closed-loop gain is dependent upon both the open-loop gain and the feedback factor, β. The product, Aβ, in the denominator is called the loop gain. Its name comes from the gain seen by a signal propagating around the loop through both the A and β networks.

Equation 3 can be manipulated to give:

$$A_{CL} = \frac{V_{out}}{V_{in}} = \frac{1}{\beta} \left[\frac{1}{1 + \frac{1}{A\beta}} \right]$$

Ideal Term — Error Multiplier

Equation 4

In equation 4 the ideal term, 1/β, determines the ideal closed-loop gain of the system. The value of 1/β is determined by the elements chosen for the feedback path. The intent is for these elements to determine the closed-loop characteristics of the feedback system. To the extent that this is accomplished is dependent upon the magnitude of the loop gain Aβ. The greater the magnitude of Aβ, the more closely the error multiplier term approaches unity, therefore allowing the ideal term 1/β to determine the closed-loop gain of the system. Said another way, the magnitude of the loop gain Aβ is the primary factor which determines how closely the closed-loop performance of a feedback system is determined by the feedback elements. The term 1/β is known as the noise gain and also determines the gain seen by amplifier input referred noise and other input referred errors (such as offsets and drift parameters). The noise gain of the system is used to determine closed loop amplifier performance with respect to these error parameters, not the signal gain. The noise gain of the two basic op amp configurations will be discussed later in this application note.

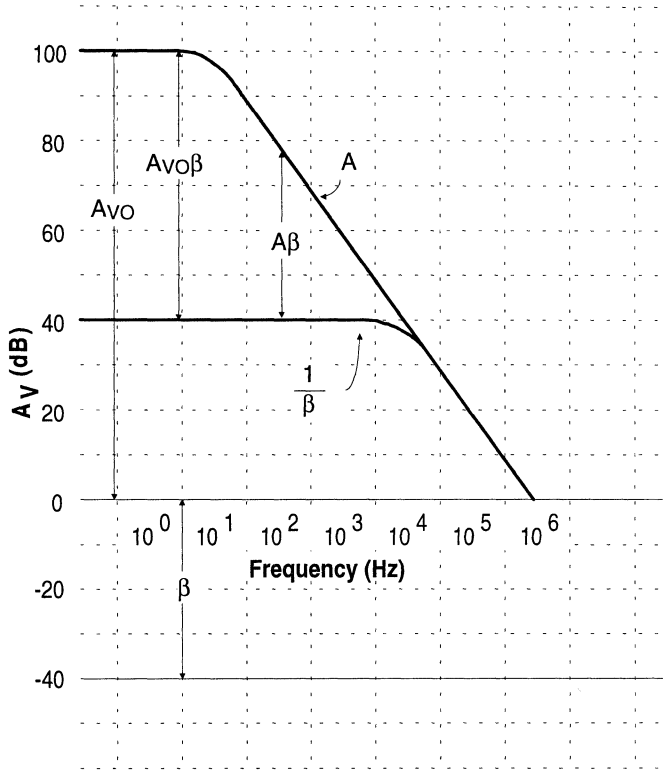


Figure 2. Bode plot illustrating the relationship of Avo, β, 1/β, and Avoβ

Feedback and the Operational Amplifier Bode Plot

The feedback parameters which have been discussed can be depicted graphically on a Bode plot. Figure 2 depicts the relationship between open-loop gain, the feedback attenuation factor, noise gain, and loop gain as a function of frequency for the noninverting circuit.

The Bode diagram shows a typical plot of the open-loop gain characteristic of an operational amplifier. At very low frequencies a typical operational amplifier may have a dc open-loop gain, (Avo) near 100 dB. A large number of amplifiers use dominant pole frequency compensation which simplifies the compensation requirements for the user. The dominant pole, located between 0.1 and 100 Hz on various amplifiers, causes the open-loop gain characteristic (A) to decrease in magnitude at a 20 dB/decade rate as the frequency is increased. In Figure 2 the logarithm of the feedback attenuation factor (β) is shown to be negative as it is a reduction in signal amplitude. The loop gain, the product of Aβ, (or Avoβ at dc), is depicted in the figure as the sum (+100 dB plus -40 dB = 60 dB at very low frequency) of the open-loop gain and the feedback attenuation factor, or the difference (+100 dB - (+40 dB) = 60 dB) between the open-loop gain and the noise gain (1/β). From the figure, one can observe that as frequency increases, the loop gain (Aβ) decreases for a set value of β. To obtain a greater amount of loop gain at higher frequencies

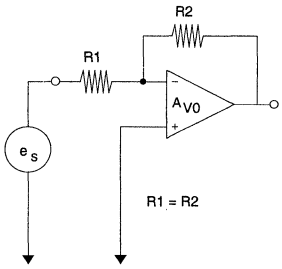


Figure 3A. Inverting: Gain of -1

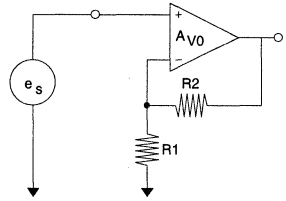


Figure 3B. Noninverting: Nonunity Gain

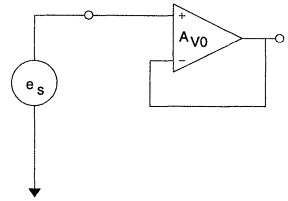


Figure 3C. Noninverting: Gain of +1

Closed Loop Signal Gain	$\{A_{CL} = \frac{-R2}{R1}\left[\frac{1}{1+\left[\frac{1}{A\beta}\right]}\right]$	$A_{CL} = \left[\frac{R1+R2}{R1}\right]\left[\frac{1}{1+\left[\frac{1}{A\beta}\right]}\right]$	$A_{CL} = 1\left[\frac{1}{1+\left[\frac{1}{A\beta}\right]}\right]$
Feedback Attenuation Factor	$\beta = \frac{R1}{R1+R2} = \frac{R}{2R} = 0.5$	$\beta = \frac{R1}{R1+R2}$	$\beta=1$
Loop Gain	$A_{VO}\beta$		
Noise Gain	$\frac{1}{\beta} = \frac{1}{0.5} = 2$	$\frac{1}{\beta}$	$\frac{1}{\beta} = 1$
Closed Loop Corner Frequency	$f_c = \frac{f_u}{\lvert A_{CL}\rvert + 1}$ note: $\lvert A_{CL}\rvert = \frac{1}{\beta} - 1$	$\frac{f_u}{\left[\frac{1}{\beta}\right]}$	$f_c = f_u$
Closed Loop Gain Stability	$\frac{\Delta A_{CL}}{A_{CL}} = \frac{\Delta A_{OL}}{A_{OL}}\left[\frac{1}{1+A\beta}\right]$		
Closed Loop Distortion and Nonlinearity	$THD_{CL} = THD_{OL}\left[\frac{1}{1+A\beta}\right]$		
Closed Loop Output Impedance	$Z_{CL} = Z_{OL}\left[\frac{1}{1+A\beta}\right]$		

Figure 3. Basic Circuit Configurations

a designer must either increase the open-loop gain of the amplifier or increase the feedback factor, β (decrease the noise gain). Remember that both the open-loop gain and the feedback attenuation factor are not constant, but instead are functions of frequency. Therefore the value of the loop gain is a function of frequency as well. The quantity of loop gain at the operating frequency is the key measure of how closely an amplifier configuration approaches the ideal.

Amplifier Configurations and Feedback

Figure 3 provides an overview of the inverting and noninverting voltage amplifier configurations. General equations for various parameters of the configurations are given with special emphasis on the unity gain configuration. Signal gain is set by the choice of resistors, but the gain error (assuming perfectly accurate resistors) is a function of the loop gain in the error multiplier term as previously stated in our discussion on feedback. The unity gain noninverting amplifier is just a special case of choosing the value of resistor R1 as being infinite and R2 being zero. Notice that the feedback attenuation factor, β, as derived for both circuits yields the same equation:

$$\beta = \frac{R1}{R1 + R2}$$

Equation 5

but for the unity gain inverting amplifier this results in a value of 0.5 whereas the unity gain noninverting amplifier results in a β of 1. These unequal values of β between the two unity-gain configurations yield further differences between the inverting and noninverting circuits. Loop gain for the unity-gain inverting circuit is half that of the noninverting unity-gain circuit. This results in the inverting circuit being more easily compensated for stability, but also yields greater errors in those parameters where loop gain is a factor. More will be said about these parameters later.

Reduced β for the inverting configuration results in greater noise gain (1/β). Error sources such as offset and noise are amplified by the noise gain and therefore the unity-gain inverting amplifier is more adversely affected by these error sources. Another negative factor of the unity-gain inverting stage is that its signal bandwidth is half that of the noninverting circuit with identical amplifiers. This bandwidth reduction is because bandwidth is a function of the noise gain, not the signal gain. Be aware of this fact when using low gain inverting stages.

The magnitude of the loop gain in a circuit affects many parameters in both the inverting and noninverting configurations. Closed loop gain stability is improved by increased loop gain as indicated in the equation:

$$\frac{\Delta A_{CL}}{A_{CL}} = \frac{\Delta A_{OL}}{A_{OL}}\left[\frac{1}{1 + A\beta}\right]$$

Equation 6

The effects of changes in the open-loop gain (such as a reduction due to increased temperature) are reduced proportionally to the amount of loop gain. Open loop distortion and nonlinearity are reduced by increased loop gain. This reduction in total harmonic distortion as indicated in the equation:

$$THD_{CL} = THD_{OL}\left[\frac{1}{1 + A\beta}\right]$$

Equation 7

5

The output impedance of a voltage amplifier is reduced with feedback as indicated in the equation:

$$Z_{CL} = Z_{OL}\left[\frac{1}{1 + A\beta}\right]$$

Equation 8

The input impedance of both amplifier configurations benefit from increased loop gain. Although increased loop gain is desirable in both circuit configurations the effect of feedback on the two configurations is different.

The noninverting amplifier utilizes voltage ratio feedback which increases the differential input impedance seen by the input signal. But the differential input impedance of the amplifier is shunted by the common mode input impedance of the amplifier. Because the common mode impedance cannot be increased by the use of feedback it is usually the limiting factor in increasing the input impedance.

The inverting amplifier configuration uses transadmittance feedback which decreases the impedance at the summing node of the input and feedback resistors. This decrease in impedance improves the virtual ground characteristic of the amplifier. In the inverting configuration the effect of a good virtual ground enables the effective value of the input impedance seen by the signal source to be set by the input resistor.

In both configurations the improvements to the respective impedances depend on the magnitude of loop gain. As the magnitude of loop gain generally decreases with increased frequency, all of the parameters normally improved by loop gain tend to degrade as the signal frequency increases. All real-world amplifiers have finite open loop gain and finite bandwidth, both of which affect the amount of loop gain available to a designer. A designer must make a prudent choice of amplifier and of the circuit configuration to minimize the errors due to loop gain limitations.

Some Other Error Sources

There are many sources of error in a given amplifier configuration. As already discussed, limited loop gain is a source of gain error which can affect DC accuracy. In addition to the DC gain error, there are the various offset errors which are contributed dependent upon the characteristics of the chosen amplifier. Sources of offset errors are the input offset voltage of the amplifier, the input bias and the input offset currents of the amplifier, limited power supply rejection and limited common-mode rejection.

Which of these errors is dominant will depend upon the choice of amplifier and its application configuration. It is a routine procedure to calculate the contribution of each source of error and this should be done as a matter of course. A few comments on each of these sources of error is appropriate.

All amplifiers have input offset voltage and input bias currents which result in errors in signal measurement. The input bias currents flow through the resistances on the (+) and (-) leads of the amplifier and produce an offset voltage error at each input. These offset voltages, and the voltage offset of the amplifier itself, are then amplified by the circuit to produce an error in the output signal. To reduce the errors due to the bias currents the standard practice has been to balance the value of resistance at the inverting and noninverting inputs to an amplifier. The purpose of making these two resistances equal has been to enable the bias currents at both inputs to produce equivalent values of offset voltage which could then be rejected by the common mode capability of the amplifier. This practice is an acceptable method of reducing error due to the bias currents and is recommended except with

modern amplifier designs which have internal bias current compensation circuitry. The bias current compensation circuitry tends to reduce the bias currents an order of magnitude or more, to the extent that they are reduced to the same order of magnitude as the amplifier's input offset currents. Adding a resistor to one input to achieve equal resistances at the two inputs of these types of amplifiers is not recommended. The added resistance is not effective in reducing the error due to the bias currents, but it will add another source of thermal noise.

Initial offset errors as well as gain errors generally can be reduced to zero with initial system calibration adjustments at room temperature. The effects of temperature-induced offset drift and gain drift remain unless a method of ongoing correction or recalibration is used to remove these effects. This correction may be accomplished with a computer after the analog signals are digitized and is recommended when maximum accuracy of measurement is demanded.

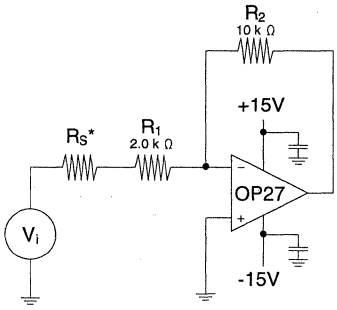
Even if the effects of temperature-induced offset errors are removed from the final data by software, it remains desirable to examine the total errors at each gain stage throughout the system. Voltage offsets due to temperature drift can be removed in software, but may still consume a significant portion of the dynamic range available to the signal. This is especially true in 16-bit converter systems with wide temperature range requirements such as required by some military specifications (-55 to +125 ° C).

Limited power supply rejection and limited common mode rejection are two more sources of errors. Most commercially-available amplifiers are designed such that the offset voltages induced by power supply variations or common-mode signals are very small; but these errors can be significant when amplifying very low level signals with high gain. It is therefore recommended to examine the error contribution of each of these sources.

Figure 4a shows an inverting amplifier circuit. The operational amplifier and the circuit components have been chosen for illustration purposes. The errors in the circuit due to the various amplifier parameters will be examined. Not included are those errors due to the signal source impedance (the impedance is assumed to be zero), output loading (which reduces open loop gain), resistor tolerance and temperature coefficient, and component long term drift effects.

A table in Figure 4a contains a selected subset of specifications for a "generic" OP-27C. No specific manufacturer is implied. The subset of data is for the total error band of the stated parameters over the -55° to +125°C temperature range. Manufacturers do not always specify temperature drift coefficients in their component data sheets. Instead, the specification sheets contain a table of data for the amplifier at room temperature (25° C) along with a table showing the total error band of the various parameters over a stated temperature span (say 55° to 125° C). Usually the specification data tables are supplemented by supporting graphs which indicate typical drift characteristics for the various parameters. These graphs can be very informative. For example, graphs in the manufacturer's data sheets (see the Precision Monolithics or the Linear Technology data book) for the OP-27 indicate that input bias currents and input offset currents show much more drift at temperatures approaching -55° C than at temperatures above 25° C. Another graph indicates that the direction of the input offset voltage drift in the OP-27 is unpredictable.

The normal procedure to calculate the error contribution of each of the operational amplifier drift parameters is to multiply the rate of drift times the temperature span over which the circuit is to be subjected. These errors due to drift are then added to the initial errors of each of the parame-



* Assumed to be zero.

$$R_e = \frac{R_2 R_1}{R_1 + R_2} = 1.667\ k\Omega$$

$$\text{Ideal Signal Gain} = \frac{-R_2}{R_1} = -5$$

$$\text{Feedback Attenuation Factor } \beta = \frac{R_1}{R_1 + R_2} = \frac{1}{6}$$

$$\text{Noise Gain} = \frac{1}{\beta} = 6$$

$$\text{Closed Loop Bandwidth } f_c = \frac{f_u}{|A_{CL}| + 1}\left[\frac{8 \times 10^6}{6}\right] = 1.33\ MHz$$

Generic OP-27 Specifications
Total Error Band for -55° to +125°C Temperature Span

		Typical	Worst Case
Input Offset Voltage	$V_{IO_{\Delta t}}$	70 µV	300 µV
Input Bias Current†	$I_{B_{\Delta t}}$	±35 nA	±150 nA
Large Signal Open Loop Gain	A_0	800×10^3 V/V	300×10^3 V/V
Power Supply Rejection Ratio	P.S.R.R.	4×10^{-6} V/V (108 dB)	51×10^{-6} V/V (86 dB)
Common Mode Rejection Ratio	C.M.R.R.	1.6×10^{-6} V/V (116 dB)	20×10^{-6} V/V (94 dB)

† Bias currents are usually of one polarity. Bias currents of both polarities indicate the use of bias current cancellation circuitry in the input stage.

Figure 4a. OP-27 Circuit and Total Error Band Specifications

	Gain	Input Offset Voltage	Input Bias Current	P.S.R.	C.M.R.	Noise
$V_o = -V_i$	$\left[\frac{R_2}{R_1}\right]\left[\frac{1}{1 + \frac{1}{A_0\beta}}\right]$	$+ V_{IO\Delta t}\left[\frac{1}{\beta}\right]$	$+ I_{B\Delta t}R_1\left[\frac{R_2}{R_1}\right]$	$+ \frac{2\Delta V_{IO}}{\Delta V_{SUP}}\left[\frac{1}{\beta}\right]$	$+ \frac{\Delta V_{IO}}{\Delta V_{CM}}\left[\frac{1}{\beta}\right]$	+ Noise
$V_o = -V_i$	$\left[\frac{R_2}{R_1}\right]\left[\frac{1}{1 + \frac{1}{(300x10^3)\frac{1}{6}}}\right]$	$+ (\pm 300x10^{-6})(6)$	$+ (\pm 150x10^{-9})(2x10^3)(5)$	$+ (2)(51x10^{-6})(100x10^{-3})(6)$	$+ (\approx 0)$	+ Noise
$V_o =$	-.99998 V_i	$\pm$ 1.8x10^{-3} V	$\pm$ 1.5x10^{-3} V	$\pm$ 61.2x10^{-6} V	$\pm \approx 0$	+ Noise
Worst Case Error % Full Scale Output‡						
	0.002%	+ 0.040%	+ 0.033%	+ 0,00136	+ ≈ 0%	+ Noise

‡ Based upon: 4.5 V FSO; 100 mV power supply change on each supply.

Figure 4b. Total Error Band Calculations

ters at the ambient operating temperature. Because amplifier manufacturers specify total error band rather than drift rates, the method of computing the error contribution of each parameter must be modified. The equation in Figure 4b illustrates the errors calculated using the total error band specifications on the OP-27C in Figure 4a. The calculations indicate the relative contribution of each source of error in the worst case with the exception of noise, which is yet to be discussed. As can be seen from the numbers, real world amplifiers can contribute significant errors in a high precision data acquisition system due to their non-ideal characteristics.

Noise and its Effects on Measurement

Noise can have a significant detrimental effect in high precision data acquisition systems. Although one can encounter many different sources of noise and of interference in system design, only certain noises made by the components themselves will be discussed here. Thermal noise, also called Johnson noise, is fundamental to all components. The thermal noise in a resistor can be calculated by use of the formula:

$$e_n = \sqrt{(4kTBR)}$$

Equation 9

where k = 1.38 x 10^{-23} Joules/ degree K (Boltzman's constant), T = Absolute temperature of the resistor, B = the effective "brick wall" Bandwidth over which the noise is to be measured, in Hz, R = Resistance value.

The amount of noise generated by a resistor can be made easier to calculate by remembering that the amount of noise generated by a 1 kΩ resistor in a 1 Hz bandwidth is 4 nV rms. The amount of noise per $\sqrt{Hz}$ generated by any other valued resistor can be computed from this normalized value:

$$e_r = \frac{4nV}{\sqrt{(Hz)}} \sqrt{\frac{R}{1k\Omega}}$$

Equation 10

This noise value assumes a one Hz bandwidth. The noise within a wider bandwidth can be computed by:

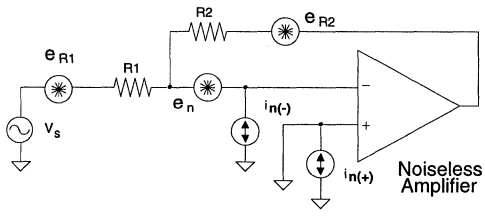
$$e_r = \frac{4nV}{\sqrt{(Hz)}} \sqrt{\frac{R}{1k\Omega} B}$$

Equation 11

Components other than resistors generate thermal noise. The OP-27 monolithic amplifier is classified by its manufacturers as a low noise amplifier. It is optimized for low voltage noise and requires low source impedances to achieve good noise performance. A plot of the OP-27 noise voltage and noise current characteristics is given in the manufacturer's data sheet. The amplifier's noise is uniform across the higher frequencies, but increases at frequencies approaching DC. This increase is called flicker noise, or 1/f noise.

A thermal noise model of the circuit of Figure 4a is shown in Figure 5. Five noise sources are shown in the model. The amplifier has a voltage noise source e_n and two current noise sources; one associated with each input of the amplifier. Each of the amplifier current noise sources will generate a corresponding noise voltage which is a function of the impedance seen by the current noise source. In addition to the voltage and current noise sources, each of the resistors has a noise voltage source associated with it. The amount of noise contributed at the input of the amplifier by the each of the resistor noise sources is reduced by the loading of the other resistor. For example, consider noise source e_{R2} as having resistor R2 as its source impedance with resistor R1 acting as the load. The noise seen at the input of the amplifier from source e_{R2} will be only

5



Noise Model of Amplifier in Figure 4a.

Effective Amplifier Bandwidth

OP-27 typical unity gain frequency = 8 MHz

$$\text{circuit bandwidth} = \frac{f_u}{|A_{CL}|+1} = \frac{8\text{x}10^6}{5+1} = 1.33 \text{ MHz}$$

effective noise bandwidth

$B = (1.33\text{x}10^6)(1.57)^{\dagger} = 2.1$ MHz

† The effective noise bandwidth of a single pole, lowpass filter is 1.57 times greater than the 3 dB corner frequency.

Noise Sources of the Model

Amplifier Noise Voltage e_n max (f_0 = 1 kHz) 25 °C = 4.5 nV/$\sqrt{\text{Hz}}$

Amplifier Noise Current i_n max (f_0 = 1 kHz) 25 °C = 0.6 pA/$\sqrt{\text{Hz}}$

} From data sheet specifications

$$e_{R1} = \frac{4.5 \text{ nV}}{\sqrt{\text{Hz}}}\sqrt{\frac{2 \text{ k}}{1 \text{ k}}} = \frac{5.65 \text{ nV}}{\sqrt{\text{Hz}}}$$

$$e_{R2} = \frac{4.5 \text{ nV}}{\sqrt{\text{Hz}}}\sqrt{\frac{10 \text{ k}}{1 \text{ k}}} = \frac{12.6 \text{ nV}}{\sqrt{\text{Hz}}}$$

Equivalent Input Referred Noise (Thermal)

$$e_t = \sqrt{(e_n)^2 + \left[i_{n(-)}\left[\frac{R_1 R_2}{R_1 + R_2}\right]\right]^2 + \left[i_{n(+)}(0)\right]^2 + \left[e_{R1}\left[\frac{R_2}{R_1 + R_2}\right]\right]^2 + \left[e_{R2}\left[\frac{R_1}{R_1 + R_2}\right]\right]^2}$$

$$e_t = \frac{6.8 \text{ nV}}{\sqrt{\text{Hz}}}$$

Total Output Noise (Thermal)

$$E_T = e_t\sqrt{B}\ \frac{1}{\beta} = \frac{6.8 \text{ nV}}{\sqrt{\text{Hz}}}\sqrt{2.1 \text{ x } 10^6}\ \frac{1}{1/6} = 59\ \mu\text{Vrms}$$

Peak Noise will be much greater.

Figure 5. Noise Calculations

that portion of its output which is developed across resistor R1 (assuming the input impedance of the op amp is very high). The noise generated by e_{R1} is reduced by the loading of resistor R2. The amount of noise generated at the input of the amplifier by each of the sources is tabulated in Figure 5. The two current sources each have the same value of current noise. Using the values of the noise sources, the effective input-referred voltage noise of the circuit has been calculated. It must be remembered that the noise sources are uncorrelated and therefore add in root-mean-square fashion. This equivalent noise source then represents the total input referred thermal noise. To obtain the value of the noise at the output of the amplifier which will be input to the A/D converter, the input referred noise is amplified by the noise gain of the amplifier while at the same time taking into consideration the effective noise bandwidth of the circuit.

Arriving at a value for the noise bandwidth of the OP-27 circuit is not as obvious as it might seem. If the noise gain of the circuit in Figure 4a is used to compute the 3 dB signal bandwidth the result will be 1.33 MHz. The effective noise bandwidth of a single pole filter is actually 1.57 times greater than the 3 dB corner frequency. But, above 1.33 MHz the OP-27 gain-phase characteristics are not those of a single pole system, but are more complex. The internal gain-phase compensation of the OP-27 will actually cause gain peaking in the circuit of Figure 4a. The gain peaking will occur at the point where the closed loop gain and open loop gain crossover. Also, at frequencies approaching the unity-gain-crossover of the OP-27, the amplifier gain will differ from the roll off of a single pole filter. The effects of the gain peaking and the complex gain-phase characteristics of the OP-27 above the 3 dB corner frequency make an accurate estimate of the resultant noise difficult. One can use the single pole filter characteristics and can approximate the noise bandwidth of the circuit as being 1.57 times the 1.33 MHz corner frequency (2.1 MHz), but the resultant noise calculation using this bandwidth will yield only a coarse approximation of the actual noise .

Using the assumption that the approximation is adequate, the noise at the output of amplifier has been calculated as shown in Figure 5. The calculated value is the amount of thermal noise in rms volts.

Thermal noise is both white and Gaussian. "White" describes the noise as having equal spectral density at all frequencies. "Gaussian" defines the probability density function which describes the amplitude characteristics of the noise. Gaussian noise follows the Normal Distribution. Therefore, once the rms value of the noise has been determined, the probability of occurrence of any value greater than a particular amplitude can be determined. The peak (+ and -) noise associated with a stated probability of occurrence is indicated in the following table:

Probability of Having a higher Amplitude Occurrence	Peak to Peak Amplitude
10 %	3.29 x RMS
1 %	5.15 x RMS
0.1 %	6.58 x RMS
.001 %	7.78 x RMS

Since the peak noise can adversely affect A/D measurements it should be investigated by both analysis and measurement.

Minimization of thermal noise in system design is accomplished with the application of three design principles. First, it is good practice to use the lowest resistor values possible (this assumes a voltage amplifier system) limited only by the constraints necessary to meet other system requirements. Second, choose an appropriate amplifier. Some amplifiers, such as the popular

LM324, do not include noise specifications in their data sheet. If low noise is a system requirement, amplifiers which have no noise specifications are not likely to be an appropriate choice. Also, choose an amplifier which is optimized to work with the source impedance requirements of the system. Bipolar-input amplifiers are generally optimized to work with low impedances as they have lower voltage noise than current noise while FET-input amplifiers are generally optimized for high impedances due to their lower current noise. The optimum choice of amplifier will depend not only on the amplifier, but its associated gain elements and circuit configuration. Analysis of the various possible configurations is necessary to disclose which will be optimum to meet design requirements. Third, one of the easiest ways to reduce the effects of noise is to restrict the bandwidth. System bandwidth should be restricted to only that amount necessary to meet system requirements. This should be done as a matter of good practice.

While only the effects of thermal noise have been discussed be aware of other noise sources (see the reference material at the end of this application note). Note that in the circuit of Figure 4a the effects of the 1/f noise were not investigated. If the system requirements demand the lowest noise possible the effects of the 1/f noise needs to be examined. The example calculations on thermal noise were done at room temperature. An increase in temperature to 125° C will result in about 1.3 dB greater noise.

Last of all, the calculated answers are only theoretical estimates. The calculations provide a theoretical minimum value but the final determinant of design should be in the evaluation of total system function and/or measurement of the actual amount of noise in the system. Remember that the value of the noise calculated provides only a reference point for the minimum amount of noise in the circuit; the actual amount present will never be less than the theoretical amount calculated, but can be more, due to other noise sources which have not been accounted for. For a more thorough discussion of noise as it applies to amplifier design see references 2 through 6 listed at the end of this application note.

Settling Time

Amplifier circuits have limitations which restrict just how quickly they can produce an accurate output signal at the application of a step change of the input signal. For small changes in signal amplitude, the ability of the amplifier to respond is dependent upon its 3 dB upper corner frequency. If the amplifier gain-phase characteristics approximate a single pole response above the 3 dB frequency the output signal will asymptotically approach a steady state output value Vs as defined by the equation:

$$V_o(t) = V_s\left[1-e^{\left(\frac{-t}{\tau_c}\right)}\right]$$

Equation 12

Where the time constant, τ_c, is given as a function of the corner frequency:

$$\tau_c = \frac{1}{2\pi f_c}$$

Equation 13

Settling time is defined as the elapsed time from when the input step voltage is applied until the output signal reaches and stays within a given error band of a steady state value.

If the input step change is large, the slew rate limit of the amplifier will restrict the speed at which its output can change. The limit at which an amplifier can slew is a function of how fast it can charge or discharge its compensation capacitor. The maximum frequency of a given

amplitude that can be faithfully reproduced by an amplifier with a stated slew rate is defined by the equation:

$$f_{max} = \frac{SR}{2\pi V_p}$$

Equation 14

where Vp is the peak output voltage.

When large changes of signal at the input occur, the settling time of the amplifier will be a combination of initial delay, slew rate limited excursion, and small signal settling time as indicated in Figure 6. Note that the small signal settling illustrated in Figure 6 is not that of a single pole system, but is instead representative of an actual wideband amplifier.

A first order approximation of settling time can be estimated for a circuit under the following conditions. First, the signal must not cause the amplifier to enter slew rate limiting. Second, the 3 dB corner frequency of the amplifier must be known and it's roll-off must be at 20dB/decade for at least a decade of frequency above the 3 dB corner frequency. Under these conditions the following equation yields a good approximation to the settling time:

$$t = -\frac{1}{2\pi f} \ln \left| \frac{V_o}{V_s} - 1 \right|$$

Equation 15

where f is the 3dB frequency. To settle to 1/2 LSB at N bits (N = 16 in a 16-bit A/D) the equation can be written as:

$$t = -\frac{1}{2\pi f} \ln \left| \frac{2^N - 0.5}{2^N} - 1 \right|$$

Equation 16

Which can be simplified to the following:

$$t = \frac{(1+N)\,(0.11)}{f}$$

Equation 17

Settling time is not readily predicted in other circumstances. It varies with signal amplitude and is as much dependent upon the circuit configuration and circuit components (including things like stray capacitance) as it is upon the amplifier characteristics. An assessment of circuit settling time is often best be obtained from observation of the circuit under applicable conditions.

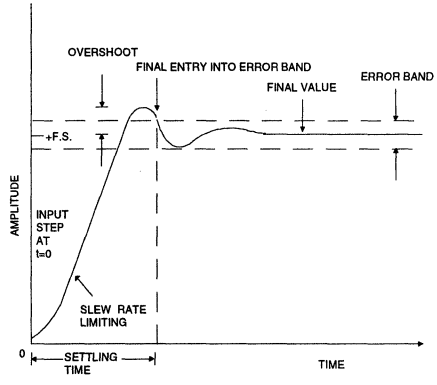
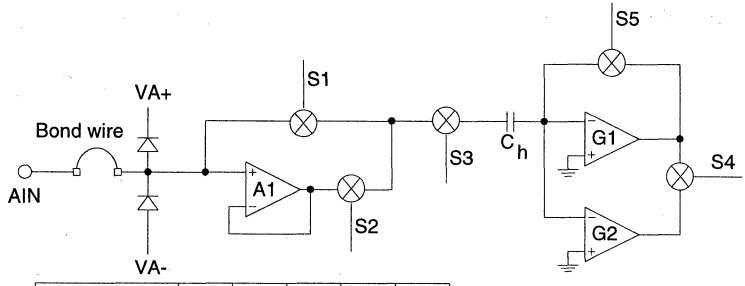


Figure 6.

II. THE CS5016 FAMILY A/D CONVERTER INPUT STRUCTURE

The analog input pin (AIN) of the CS5016 series converter acts as a load to the buffer amplifier output. A good understanding of the internal workings of this pin on the converter will help in the design of an appropriate buffer amplifier.

Figure 7a depicts a simplified circuit diagram of the circuitry internal to the A/D converter as seen from the AIN pin. From the metal pin of the



	S1	S2	S3	S4	S5
Coarse-charge	OFF	ON	ON	ON	ON
Fine-charge	ON	OFF	ON	OFF	ON
Conversion	OFF	OFF	OFF	OFF	OFF

$C_h = \begin{cases} C_A \text{ in Unipolar Mode} \\ C_{A/2} \text{ in Bipolar Mode} \end{cases}$

Figure 7a CS5016 Family Analog Signal Input Model

package a bond wire connects to the semiconductor chip. Clamp diodes on the chip connect to both of the supplies. Under abnormal conditions, excess signal amplitude may forward bias the diodes. The diodes protect the chip from voltage breakdown. Unless the current under such fault conditions is limited, the diodes may short out or the bonding wire may "blow its fuse". The current should be limited to under one hundred mA transient or under 10 mA steady state to eliminate any possibility of damage. Methods of limiting input current to the A/D converter are discussed below. Once the input signal travels beyond the protection circuitry, it sees a buffer amplifier A1, CMOS switches S1, S2, and S3, a hold capacitor C_h, and transconductance amplifiers G1 and G2. To accomplish a complete conversion cycle, the states of the CMOS switches are altered. These state changes cause the effective load at the AIN pin to change dynamically during the three different phases of the conversion cycle. These three phases are called coarse-charge, fine-charge and conversion. An understanding of the function of each of these three phases will explain the reasons for the dynamic change in loading. The conversion phase begins with the activation of the hold command ($\overline{HOLD}$ goes low).

When hold is activated, the "sample capacitor" of the track-and-hold section of the converter immediately traps a charge on the sample capacitor which is representative of the input signal. The binary representation of the value of the charge is then determined. The number of master clock cycles necessary for this determination to occur is a function of the number of bits of the converter and the particular mode of operation (loopback or asynchronous). The occurrence of the $\overline{EOC}$ (end of conversion) signal indicates that the conversion time is complete. The converter must then acquire a new sample of the input signal for the next conversion. The coarse-charge and fine-charge times accomplish this. First to occur is the coarse-charge phase. A buffered version of the analog input signal is first connected to the sample capacitor. The input impedance of the buffer is very high and therefore does not load the input signal source. The output of the buffer is connected via switches S2 and S3 to the sample capacitor (switch S1 is open). The buffer (Figure 7a, A1) furnishes the majority of the current necessary to charge the capacitor toward the new voltage value. The buffer therefore reduces the transient current demand from the signal source if the input signal has changed from the value previously stored on the sample capacitor. The sample capacitor is connected to the output of the buffer for six cycles of the master clock (CLKIN) frequency. At the end of the six cycles the coarse-charge phase is complete.

The sample capacitor is then directly connected to the analog input signal for the fine-charge phase (Switches S1 and S3 are closed, S2 is opened). Immediately before being connected for the fine-charge phase, the voltage on the sample capacitor may still differ slightly from the analog input value. This is due to the offset voltage of the buffer amplifier (A1). This offset voltage is typically 50 mV but may be up to 150 mV in the worst case. At the beginning of the fine-charge phase a small transient demand of current from the external signal source may occur as the capacitor charges to its final value. The fine-charge phase will last until the hold command becomes active again. In loopback mode the fine-charge phase lasts nine master clock cycles until the end of track ($\overline{EOT}$) signal reactivates the hold command. When the hold command is activated asynchronously, the fine-charge phase should last a minimum of nine master clock cycles and may continue indefinitely until the hold command is activated.

Simplified models of the impedances seen by the analog input signal are depicted in Figures 7b and 7c. For the conversion and coarse-charge phases, the impedance seen at the AIN pin is the input impedance of the buffer A1. This impedance is approximately 100 MΩ shunted by 15 pF. When in the coarse-charge phase the sample capacitor is charged by the buffer (A1) output. The speed at which the voltage on the sample capacitor can track the input signal is limited to the rate at which the buffer output current can charge the capacitor. The slew rate of the buffer is 5 V/µs when the converter is in unipolar mode and 10 V/µs when in the bipolar mode. The reason for the difference is that the sample capacitor in bipolar mode is only half the value of that in unipolar mode.

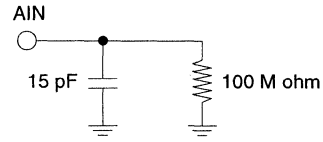
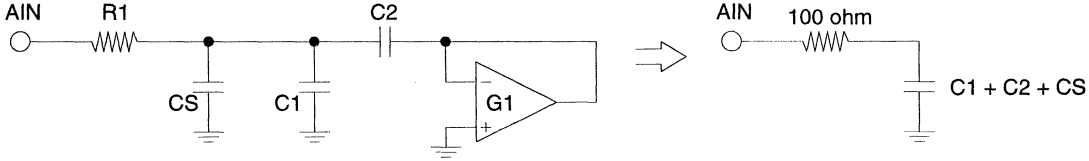


Figure 7b. Simplified Input Model During Coarse-charge / Conversion

The simplified model of the impedance seen in fine-charge is that of Figure 7c. Resistor R1 is the effective resistances of the S1 and S3 CMOS analog switches of Figure 7a. The sample capacitor consists of C2, whereas capacitor C1 and CS are stray capacitance. G1 is a transconductance amplifier with an effective input resistance of about 35 Ω at DC. The slew rate in the fine-charge mode is limited to the rate at which the output current of the transconductance amplifier



	C1	C2	CS	R1	Gin
Unipolar	170 pF	170 pF	20 pF	100 ohm	35 ohm
Bipolar	85 pF	85 pF	30 pF	100 ohm	35 ohm

Figure 7c Simplified Input Model During Fine-charge.

G1 can charge capacitor C2. In unipolar mode the slew rate is 0.25 V/µs. In bipolar mode when the capacitance of C2 is less, the slew rate increases to 0.5 V/µs. Acquisition of fast slewing signals (step functions) can be hastened if the step occurs during the conversion cycle or during the coarse-charge cycle since at these times the slew rate of the converter input is faster. It should be noted that in fine-charge, any external impedance on the AIN pin becomes part of the total network and will contribute to the settling time response characteristics.

Also, Figure 7a shows that when switches S1 and S3 are turned on (S2 is off) in the fine-charge phase, the source impedance of the external circuitry connected to the AIN pin actually becomes part of the feedback network of amplifier G1. The external circuitry should offer an impedance less than 400 Ω at frequencies greater than 2 MHz or amplifier G1 may oscillate.

The input circuitry of the analog front end of the A/D converter uses CMOS analog switches which are similar to analog switches available in individual integrated circuits. The resistances of the CMOS switches, such as shown in Figure 7c, exhibit non-linear effects with changes in signal amplitude and frequency. These dynamic changes in switch characteristics are a source of distortion at high frequencies.

III. EXAMPLE BUFFER CIRCUITS

Buffer Circuit Test Method

Several example buffer circuits have been constructed and tested. Evaluation was restricted to dynamic testing at room temperature (25° C). The testing was performed using a CDB5016 evaluation board connected to an IBM compatible computer via a 16-bit parallel I/O card. Signal processing software developed at Crystal was used to evaluate the data. The signal source was a Khron-Hite 4400A Low Distortion Oscillator modified to produce low broadband noise per the article in Reference 1 (Reprints available from Crystal upon request). The oscillator was adjusted to the appropriate full-scale value for each circuit. A frequency of 1.5 kHz was chosen as the test frequency.

The output data from the A/D converter was processed to yield three indicators of dynamic performance. These are:

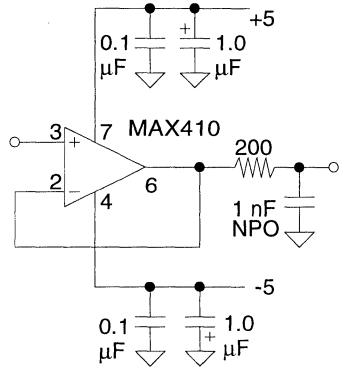
1) S/(N+D): The ratio of the rms value of the signal to the rms sum of all other spectral components below the Nyquist rate (except DC), including distortion components.

2) S/D: The ratio of the rms signal value to the ratio of the rms sum of all harmonics.

3) S/PN: The ratio of the rms signal value to the rms value of the next largest spectral component below the Nyquist rate (except DC).

Benefits of an RC Isolation Network

All of the example circuits show an RC network coupling the output of the buffer to the input of the A/D converter. The 200 Ω resistor and 1 nF capacitor network is recommended for the CS5012A, CS5014, CS5016, and CS5126. The 200 Ω resistor should be replaced with 50 Ω for the CS5101A and CS5102A. The RC filter enhances circuit operation in four ways. First, the network reduces the amount of broadband noise. Second, it decouples the input capacitance of the A/D converter from the amplifier. This reduces the possibility of the amplifier having stability problems driving a capacitive load. Third, the circuit isolates the output of the amplifier from the high frequency pulsed charge effects of the sampling front end of the A/D converter. And finally, the passive network offers a well-behaved low source impedance to the internal transconduc-



Gain	1
Input	1.5kHz, ±3.5Vpk
VREF	3.5 V
S(N+D)	90.54 dB
S/D	100.1 dB
S/PN	104.7 dB

Figure 8. MAX410 Noninverting Amplifier

tance amplifier, satisfying its stability needs. The component values are chosen to have a time constant of 200 ns to provide appropriate settling time when the converter (16 bits) is sampling at 50 kHz. The NPO dielectric characteristic minimizes the effect of voltage coefficient of capacitance which can adversely affect performance at the 16-bit level. Other dielectrics may be adequate while some may result in non-linear capacitance with signal level and therefore introduce distortion. Empirical testing may be necessary to insure whether a given dielectric is adequate for a particular application.

± 5 Volt Supply Op Amp Circuits

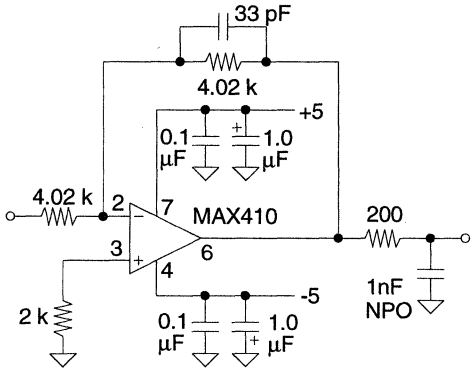
The first example circuit is a unity gain buffer circuit shown in Figure 8. The MAX410 op amp is designed for operation from ± 5 V power supplies. The input common mode range of the amplifier is specified as ± 3.5 V, therefore the reference voltage for the A/D converter was set to use +3.5 V as its full scale reference value. The circuit yields quite good results when the reduced signal level is considered.

The second circuit, Figure 9, configures the MAX410 in the inverting mode. The minimum output voltage swing for the MAX410 is specified as ± 3.6 V (2 kΩ load) with a typical range of ± 3.7 V. A 3.5 volt reference was used for the A/D converter. Performance was good using the 3.5 volt reference.

± 15 Volt Supply Op Amp Circuits

Most precision operational amplifiers are specified for operation from ± 15 V supplies. Figure 10 shows an OP-27 used to reduce signal levels of ± 10 V to ± 4.5 V. The performance is excellent. Figure 11 then shows the OP-27 in the non-inverting configuration.

The performance levels being achieved with the OP-27 result from operating the amplifier well within its specifications for input range and output amplitude capability. The Signetics NE5534A worked equally well in both circuit configurations (Figures 10 and 11). Note that low value resistors are used to minimize the component noise in the circuits.



Gain	-1
Input	1.5kHz, ±3.5 Vpk
VREF	3.5 V
S/(N+D)	90.1 dB
S/D	97.7 dB
S/PN	102.0 dB

Figure 9. MAX410 Inverting Amplifier

If an OP-27 type amplifier is used, the inverting circuit is preferred for signal processing applications. This is because some brands of OP-27 amplifiers exhibit much higher distortion at frequencies above 10 KHz or so when used in the non-inverting configuration. It may be that the internal bias current cancellation circuitry does not track the input stage well when subjected to the rapidly-varying (high frequency) common mode voltages such as those experienced by the positive gain configuration.

Achieving ± 4.5 Volt Output with ± 5 Volt Supplies

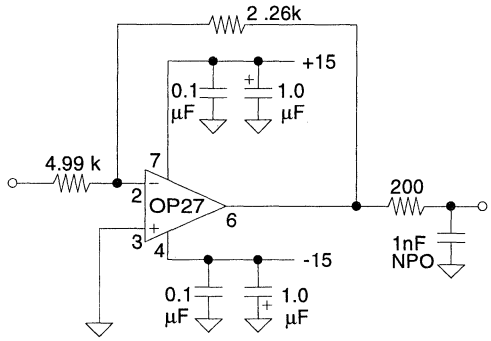
Some designs may require that the entire system operate from ±5V, but achieve the full dynamic range of the A/D converter when using a 4.5 V reference. The Signetics NE5534A op amp, known to be excellent for audio use, can be combined with a discrete transistor output stage to yield excellent results when using only ± 5 V supplies. Figure 12 illustrates the NE5534A in the inverting configuration, reducing a ± 10 V signal to ± 4.5 V. The OP-27 (without the external compensation capacitor) yielded similar noise and distortion results but had slightly slower rise time when tested with a transient input.

An Instrumentation Amplifier Circuit

Some systems require an instrumentation amplifier front end. One instrumentation amplifier was tested; the AD625C from Analog Devices. The data sheet specifies a maximum nonlinearity of 0.001%. Although the device may have good static linearity, its dynamic performance was well below 16-bit performance. The AD625C, shown in Figure 13, was tested with two different gains. The instrumentation amplifier was tested with a gain of one, and then with a gain of nine. The gain of nine configuration is with the 5 kΩ resistor connected to pins 2 and 15. The data indicates that the part actually has greater distortion (indicative of greater nonlinearity) in the lower gain configuration.

Signal Limiting Circuits

When utilizing op amps with ± 15 V supplies to drive A/D converters with ± 5 V supplies it is possible under certain input conditions for the

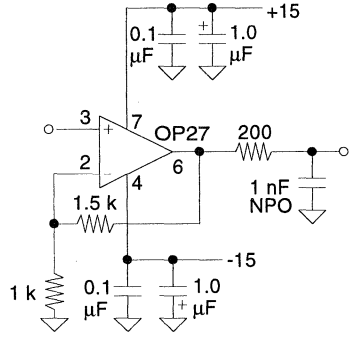


Gain	-0.45
Input	1.5kHz,±10Vpk
VREF	4.5 V
S(N+D)	91.8 dB
S/D	100.5 dB
S/PN	102.6 dB

Figure 10. OP-27 Inverting Amplifier

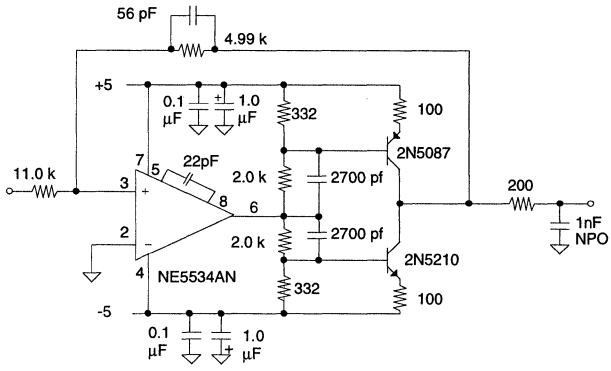
amplifier output voltage to attempt to exceed the supply rails of the converter. As described previously, the converter has protection diodes at the analog input and therefore will clamp the voltage whenever the signal forward biases the diodes. If high current amplifiers are used, excess current from the amplifier may damage the converter. If excess current is a possibility, then the voltage swing of the amplifier must be limited so as to not exceed the supplies of the converter; or some means of current-limiting must be used. Many amplifiers have current limiting circuitry as part of their output stage and will limit their output current if a fault condition exists. Even though the amplifier may protect itself in this manner it may not be desirable from a system performance point-of-view. System measurement accuracy can be degraded due to offset and gain errors which occur as a result of amplifier self-heating.

Several approaches to amplifier output limiting can be used. Zener or diode bounding circuits can be used. Some bounding/clamping circuits reduce the circuit gain by reducing the effective feedback resistance when an overvoltage signal exists. Others limit the signal by shunting it to ground when it exceeds the desired amplitude. Reference 6 documents some of these circuits and discusses their strengths and weaknesses.



Gain	+2.5
Input	1.5 kHz, ±1.8 Vpk
VREF	4.5 V
S(N+D)	90.7 dB
S/D	98.0 dB
S/PN	102.3 dB

Figure 11. OP27 Noninverting Amplifier



Gain	-0.45
Input	1.5 kHz, ±10Vpk
VREF	4.5 V
S (N+D)	91.7 dB
S/D	99.7 dB
S/PN	103.3 dB

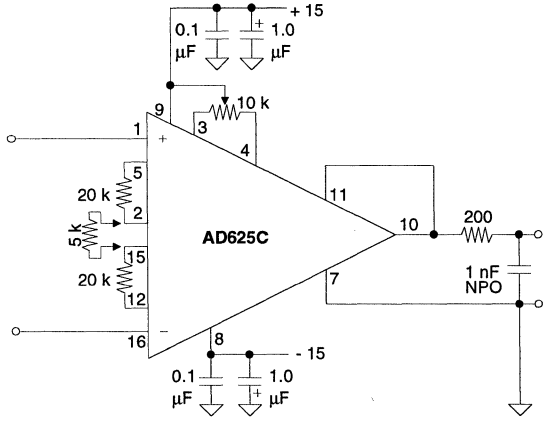
Figure 12. Op Amp with Transistor Buffer Stage

Voltage Clamping via the Compensation Pin

Figure 14 indicates a simple means of clamping available on some op amps. Illustrated is a Harris HA-2600 with diodes connected to its compensation pin (8). The ± 5 V supplies of the A/D converter provide the clamp voltage reference values for the diodes. The output stage of the HA-2600 has unity voltage gain but high current gain. The signal on pin 8 of the amplifier is a low current signal of identical amplitude to the output signal. Limiting of the output signal swing is accomplished by clamping the signal at pin 8 to the desired level. Even if the on voltage of the clamp diodes on the op amp exceed the on voltage of the clamp diodes inside the A/D, the 200 Ω resistor will limit the current to an acceptable level.

A Novel Method to Aid Current Limiting

Another method of protecting the A/D converter from excess signal conditions is illustrated in Figures 15 and 16. The circuits make use of



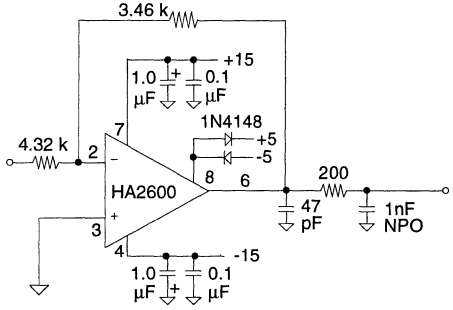
Gain	1
Input	1.5 kHz, ±4.5 Vpk
VREF	4.5 V
S/(N+D)	73.1 dB
S/D	81.5 dB*
S/PN	83.7 dB*

* Primarily 2nd harmonic

Gain	9*
Input	1.5 kHz, ±0.5 Vpk
VREF	4.5 V
S/(N+D)	74.1 dB
S/D	87.3 dB
S/PN	84.7 dB

* 5 K resistor connected

Figure 13. Instrumentation Amplifier

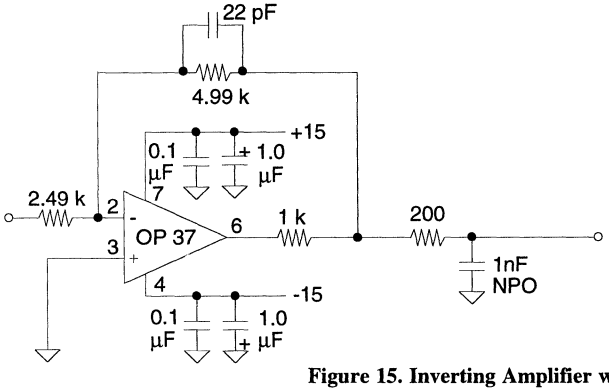


Gain	-0.8
Input	1.5 kHz,±5.6Vpk
VREF	4.5 V
S/(N+D)	90.5 dB
S/D	97.0 dB
S/PN	98.1 dB

Figure 14. Compensation Pin Clamping

additional series resistance between the op amp and the converter to limit the amount of signal current available. The resistor is placed inside of the feedback loop of the amplifier where the loop gain of the circuit reduces the effect of the 1 kΩ resistor under normal operating conditions. When a fault condition exists, the signal output from the amplifier may attempt to exceed the power supply rails of the A/D converter. Under this condition the current into the A/D converter input will be limited to less than 10 mA by the 1 kΩ resistor.

The added 1 kΩ resistor increases the open loop output impedance of the circuit. This increase in output impedance adversely affects the effective open loop gain of the circuit when driving lower impedance loads. Therefore, it is desirable to take advantage of op amps with higher open loop gains. Decompensated op amps offer greater gain-bandwidth products but with the restriction that they are generally specified to be stable only with higher gain configurations. For example, the OP-37 is specified for operation with a minimum gain of 5 but offers higher open loop gain than the OP-27 (about 15 dB higher at 10 kHz). The circuits in Figures 15 and 16 take advantage of the added open loop gain of the OP-37 yet still meet the requirements for stability demanded by the amplifier. At low frequencies (below 10 kHz) the loop gain of the circuit reduces the effect of the 1 kΩ resistor significantly. At the same time the effective load to the amplifier output (including the 1 kΩ output resistor) is dominated by the



Gain	-2
Input	1.5kHz,±9Vpk
VREF	4.5 V
S/(N+D)	91.2 dB
S/D	97.9 dB
S/PN	99.2 dB

Figure 15. Inverting Amplifier with current limiting

feedback resistor. At high frequencies (above 1 MHz) the impedance of the 1 nF capacitor in the output filter begins to look like a short circuit therefore the load seen by the op amp circuit is dominated by the 200 Ω resistor. At the higher frequencies the open loop gain of the op amp is decreasing. The corresponding reduction in loop gain allows the effect of 1 kΩ resistor to begin to take effect, increasing the output impedance to the feedback node. The combined effect of the higher output impedance due to the 1 kΩ resistor and the loading effect of the 200 Ω resistor causes an effective loop gain reduction of about 200/(1000 + 200) or a factor of 6. This gain reduction in combination with the phase compensation of the feedback capacitor allows the circuit to maintain stability while it also provides current limiting under fault conditions.

This application note has discussed the making of a good buffer circuit and has illustrated several examples with relevant test data. For further information on design and dynamic testing of amplifier circuits refer to the following references.

List of References

1. Harris, Steven: "Dynamic techniques test high-resolution ADCs on PCs," Electronic Design, September 3, 1987. (Reprint available from Crystal Semiconductor)

2. "Minimization of Noise in Operational Amplifier Applications," AN15, Precision Monolithics, Inc.

3. "Explanation of Noise," AN164, Signetics, Inc.

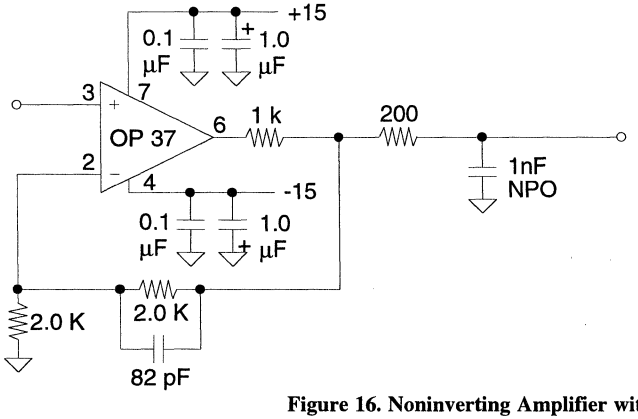
4. Whitehead, Richard: "Operational Amplifier Noise Prediction," AN519, Harris Semiconductor.

5. Sherwin, Jim: "Noise specs confusing?" AN104, National Semiconductor.

6. Frederiksen, Thomas: Intuitive Operational Amplifiers. McGraw-Hill, New York, 1988.

7. Roberge, James K.: Operational Amplifiers: Theory and Practice, John Wiley and Sons, New York, 1975.

8. Dostal, J.: Operational Amplifiers, 2nd Edition, Butterworth-Heinemann, Stoneham, MA, 1993.



Gain	+2
Input	1.5 kHz, ±2.25Vpk
VREF	4.5 V
S(N+D)	92.0 dB
S/D	100.4 dB
S/PN	102.8 dB

Figure 16. Noninverting Amplifier with Current Limiting

Application Note

A Collection of Application Hints for the CS501X Series of A/D Converters

By Jerome Johnston

- Jam ADC into Coarse Charge for High Slew Signals
- Single Control Input Acts as a "Start Convert" Command
- Synchronizing Multiple CS501X Series A/D Converters
- ±5V Input Signal Range Operation

Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445-7222 FAX: (512) 445-7581

Here are several application hints which extend the flexibility of the CS501X series of A/D converters.

Jam ADC Into Coarse Charge For High Slew Signals

The CS501X family of A/D converters have within their capacitor-based architecture a track-and-hold function. Upon completing a conversion the A/D converter immediately begins to track the input signal. The design is such that the input signal is buffered (internal to the A/D) from the capacitor array for six cycles of the master clock. Then the buffer is bypassed and the array is directly connected to the AIN pin of the converter. This allows the converter to settle to its final value within the accuracy specifications. The period of time that the buffer is connected is known as the coarse charge time. The time when the buffer is bypassed to sample the input signal directly is known as fine charge time. Slew rate capability during coarse charge time is much greater than the slew rate in fine charge. Any step changes of the input signal should occur either prior to or during the coarse charge time. Under normal operation, once the converter has completed the coarse charge time and entered into the fine charge time it will stay in the fine charge state until the $\overline{\text{HOLD}}$ input goes low. When $\overline{\text{HOLD}}$ goes low the charge on the capacitor array is immediately trapped and conversion begins.

In applications which exhibit step changes in the input signal, it is not desireable that the converter remain waiting in the fine charge mode (with its slower slew rate capability). Extending the coarse charge time allows the ADC to track high slew signals.

Figure 1 depicts the logic by which the master clock to the converter is stopped during the coarse charge time to lock the converter into coarse charge. At the end of each conversion the End of Conversion ($\overline{\text{EOC}}$) signal indicates the

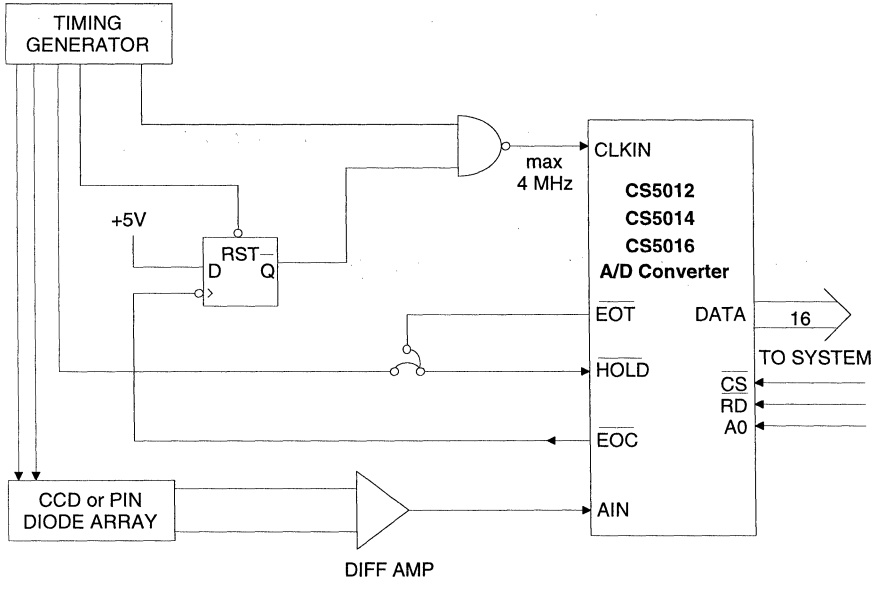


Figure 1. Sample Logic Jams Converter into High Slew Rate Mode

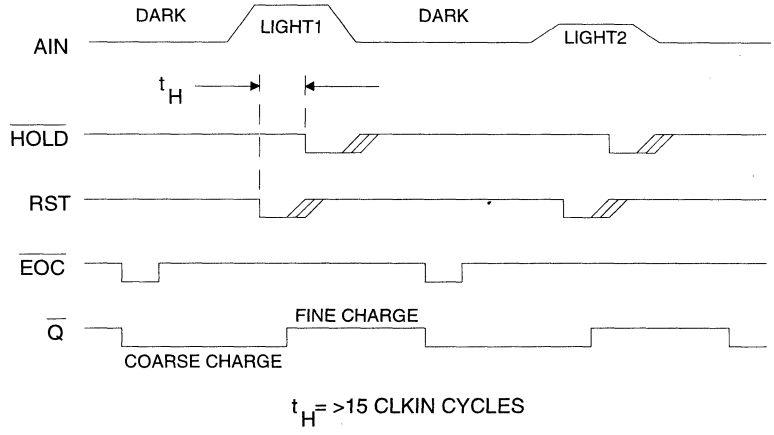


Figure 2. Extending Coarse Charge Time Allows Tracking of Dark to Light Transition

end of a conversion and the beginning of a coarse charge time. $\overline{EOC}$ falling toggles the flip-flop, causing its $\overline{Q}$ output to go low. This jams the NAND gate output high which locks the converter into the coarse charge mode until the timing generator circuitry resets the flip-flop.

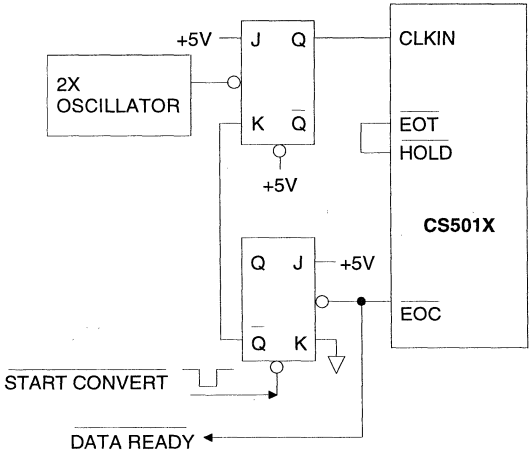


Figure 3.Coarse Charge Jamming with "StartConvert" Control

Figure 2 illustrates the timing of the various signals of the circuit in Figure 1. CCD or PIN diode array outputs exhibit step changes in their signal levels as each array element is selected for output. After each conversion the converter is stopped in the coarse charge mode until the video output signal from a particular element of the sensor array is stable. The clock to the A/D converter is then restarted. The converter then proceeds through the coarse and fine charge times and awaits a $\overline{HOLD}$ signal. If the $\overline{EOT}$ output of the converter is tied to the $\overline{HOLD}$ conversion will begin as soon as the track time is complete.

While this coarse charge jamming circuit is designed to operate with the CS501X series of converters, note that the CS5101 A/D converter offers a CRS/$\overline{FIN}$ (coarse/fine) pin as an input to allow user control of the tracking mode.

Creating a Single "Track, Hold, and Convert" Command

The coarse charge jamming circuitry of Figure 1 is altered to allow a single control line to initiate a sample and convert sequence. First, the $\overline{EOT}$ output from the converter must be directly tied to

$\overline{\text{HOLD}}$ input. This connection will enable the converter to initiate a conversion upon completion of 9 clock cycles of fine charge (the minimum fine charge time necessary for adequate settling).

At the end of each conversion the $\overline{\text{EOC}}$ signal will toggle the flip-flop and lock the converter in coarse charge. The converter will track the input signal in the coarse charge mode until the "start convert" input resets the flip-flop to restart the clock. With $\overline{\text{EOT}}$ tied to $\overline{\text{HOLD}}$ the converter will proceed through coarse charge, fine charge, and conversion at which time it will stop and await another "start convert" command. Data in the output port will remain available until a new start convert command is issued, but due to internal logic, the port cannot be read in the byte-wide (BW = 0) mode.

Figure 3 illustrates an example of the "start convert" circuitry using a dual J-K flip-flop. Note that the input clock is twice that required by the converter and that the low time of "start convert" pulse should be less than the conversion time of the converter. The "start convert" signal should be held low during calibration.

Synchronizing Multiple CS501X Series A/D Converters

Simultaneous sampling of several channels is often required. For example, in measurements of the outputs of three-axis magnetometers or three-axis inclinometers it is desireable that all three signals be simultaneously sampled and then converted. Because the CS501X converters offer very good repeatibility from part to part they can yield very good channel to channel measurement correlation even though each channel is converting with its own A/D converter.

Figure 4 illustrates how multiple CS501X series converters can be synchronized, allowing simultaneous sampling. The circuit uses a flip-flop to synchronize a reset (RST) signal common to all of the A/D converters such that the reset signal goes low on a falling edge of the master clock (CLKIN) to each converter. A common $\overline{\text{HOLD}}$ command can then be connected to all of the converters to initiate simultaneous sampling. Or, if the synchronous loopback mode of sampling is desired, the $\overline{\text{EOT}}$ output from one of the converters can be input to the $\overline{\text{HOLD}}$ inputs of all of the converters.

When several converters are galvanically isolated from the digital processing system, synchronazation is useful. The data is passed across the isolation barrier in serial form. If several converters are in the system, normally both SDATA and SCLK signals from each converter are passed across the isolation barrier. However, if the converters are synchronized, the SDATA outputs of several converters can be clocked into serial to parallel registers on the digital side by sending a single SCLK signal across the barrier.

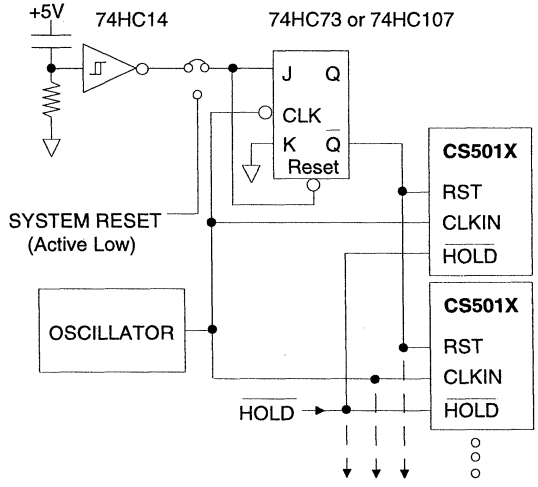


Figure 4. Controlled Reset for Synchronizatoin of Multiple Converters

± 5V Input Signal Range Operation

Some system specifications may require signal levels of ± 5 V. Operating the CS501X series of A/D converters with ± 5 V signals requires a 5 V reference and therefore the supplies have to be raised. The supplies should be adjusted to output voltages in the range from 5.3 to 5.5 volts. The positive and negative supplies should be of equal magnitude and the system connections recommended in the A/D converter data sheet should be maintained.

An easy means of achieving the proper supply voltages is to use LM317L and LM337L regulators. These devices are acceptable as the power requirements of the A/D converter are very low. See Figure 5 for the appropriate resistor values to set the regulator voltages. An alternative is to use LM78L05AC and LM79L05AC regulators with adjustment resistors to increase their output voltages. This is illustrated in Figure 6.

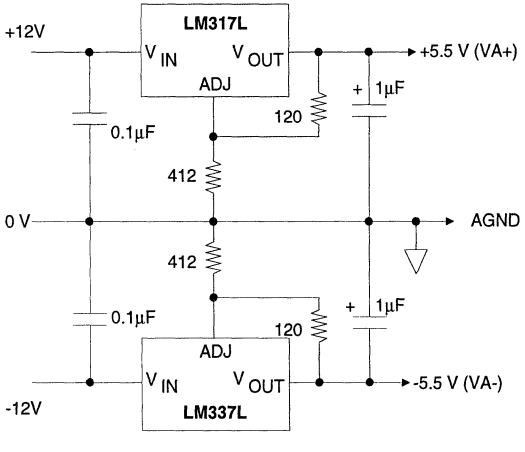


Figure 5. LM317L/LM337L Voltage Regulators

References which output 5 V require a minimum input voltage from 6.5 to 11 volts. This increased voltage is necessary to accommodate the 1 to 6 volt input to output voltage differential needed by the reference. Supply voltages of +12 V or +15 V are common. Care should be excercised to insure

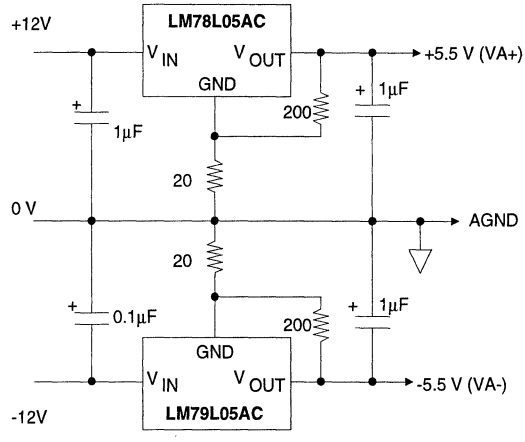
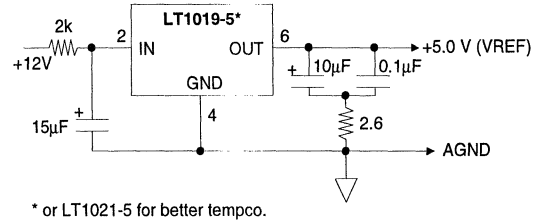


Figure 6. LM78L05/LM79L05 Voltage Regulators

that the voltage reference output does not source current into the A/D converter VREF pin before the power supplies on the A/D are established. One means of insuring this is to add an RC filter in front of the voltage reference as illustrated in Figure 7. This will delay the reference output until the regulated supplies (Figure 5 or 6) for the A/D are established.

With raised supply voltages on the A/D converter, the digital outputs will output logic 1's with a higher output voltage (V_{OH}). To accommodate this increase the digital logic in the system can use 74HC4049 or 74HC4050 logic level translators to restore the logic outputs back to the 5 V level. Alternatively, the logic system (if 74HC logic is used) can also use a supply voltage elevated to the value of the A/D supply. This problem is also eliminated if the ADC is isolated using opto-couplers.



* or LT1021-5 for better tempco.
or LT1019-4.5 for 4.5V output

Figure 7. 5Volt Reference with RC Input Delay

•Notes•

CONTENTS

PRODUCT CATEGORY LEVELS

Crystal's integrated circuit (IC) products are fabricated, assembled and tested either in-house or through one or more subcontractors. Qualification and manufacturability criteria are defined for each of four product category levels achievable during the product life cycle of an IC. Products are classified by the most stringent category level requirements met. Crystal's goal is to achieve Level I (World-Class) status for the majority of its product families. The product category levels are:

Level IV:	Engineering Prototype (EP) Release
Level III:	Production Level III
Level II:	Production Level II
Level I:	World Class

Level IV -- Engineering Prototype Qualification (EP)

Level IV is the first qualification level for IC products. It is used for early sampling and risk production builds. Qualification tests to achieve Level III begin shortly after the receipt of first functional devices. Level IV packaged devices are marked with an additional "EP".

Level III -- Production Level III

Level III is the second qualification level for IC products. This level is applicable to devices which are on track to achieving a Production Level II qualification and provides an interim reduction in the risk of substandard product shipments to customers. Comprehensive production test programs (with guardbands) are used for testing Level III products. Characterization of initial products is complete. Qualification tests have been completed per the criteria shown in the Qualification Criteria Table at the front of this databook.

Level II -- Production Level II

Level II is the high volume production qualification level for IC products. Level II products have met the goals for sustainable manufacturability and reliability by passing a comprehensive series of qualification tests, completing product documentation, and demonstrating product performance through detailed characterization.

Level I -- World Class Products

Level I is the highest level attainable for any product family. Qualification tests for Level I involve routine monitoring of ramped product families over a period of time to measure increasingly stringent reliability and quality levels that require a substantial number of devices and device-hours. Additionally, sources of variation throughout the manufacturing process (fab, assembly and test) are monitored and reduced over time following industry standard learning curves. This provides a statistical, pro-active approach to direct improvements in reliability performance and outgoing quality. It is the goal of every product family to achieve Level I status.

RELIABILITY METHODS

I. CONCEPT OF RELIABILITY

In general terms, the reliability of a semiconductor device is defined as the measure of the functional stability of the device with respect to time. Expressed in a more quantitative sense, it is the probability that the device will operate with a specified performance over a specified period of time under a given set of conditions.

Reliability characteristics are usually stated in reverse terms as the loss of ability to function, or failure rate. The reliability performance of a device can best be summarized by the reliability life or "bathtub" curve (Figure 1). The reliability performance is characterized by three phases: infant mortality, useful life, and wearout. Infant mortality failures can be reduced by proper manufacturing controls and screening techniques. The useful life period is typically a long period of time where only occasional random failures occur. During this time the failure rate is usually very low. The final period is aptly named wearout. Using proper design guidelines and device applications, this period is shifted well beyond the lifetime required by the user.

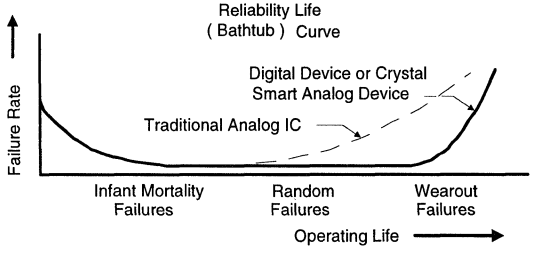


Figure 1.

An item of great importance in evaluating reported reliability characteristics is the definition of a failure. Crystal's definition of a failure is any device that fails to meet ANY data sheet parameter. Crystal's digital self-calibration techniques provide stable performance over temperature and life. Traditional Analog IC's and hybrids exhibit wearout mechanisms very early in the life of the product. One competitor's analog-to- digital converter's linearity error stability is specified at ± .00075 % per 1000 hours at 25 °C. Stability degradation at 70 °C is unspecified and is likely to be accelerated greatly as temperature increases. The dashed line of Figure 1 is typical of the wearout seen in a competitor's Analog IC or hybrid. As you can see, wearout begins much earlier than a digital device or a mixed analog and digital chip utilizing Crystal's SMART analog design architecture and CMOS wafer technology.

II. CRYSTAL SEMICONDUCTOR RELIABILITY STRESSING

These stresses are done on every new product, assembly house or fabrication subcontractor. Some of Crystal's acceptance criteria and goals are as described in the Qualification Criterion Table in section 1 of this data book.

Accelerated Operating Life Stress

Accelerated operating life stressing is performed to accelerate thermally-activated failure mechanisms through the application of extreme temperature and dynamic biasing conditions. The typical temperature and voltage conditions used in the stress are 125 °C with a bias level at the maximum data sheet specifications. Some devices may be stressed at an even higher voltage level to further stress the oxides of the device. All devices used in life stress are sampled directly from the production flow with no special processing or prescreening. Stressing is performed per MIL STD 883, method 1015, condition D (dynamic signals). These dynamic conditions simulate as much as possible actual operating conditions in an application.

Infant mortality (48 hrs at 125 °C), early operating life stress (168 hrs at 125 °C) and long term operating life (typically 1000 hrs at 125 °C) are reported . Infant mortality life simulates approximately 3-4 months in the field at 55 °C and is reported as a percent. Early and Long term life simulate the total failures seen in the field and are expressed in FITS (failures in time). 1 FIT = 1 failure per billion device-hours. Derating of early and long term operating life is done using Arrhenius thermal equations along with Weibull statistics. A 60 % upper confidence limit (UCL) and .7 electron volts (eV) activation energy are used in this calculation.

85 °C/85% R.H.

85 °C/ 85% R.H. is an environmental stress performed at a temperature of 85 °C and at a relative humidity of 85%. The test is designed to measure the moisture resistance of plastic encapsulated devices. A nominal-voltage static bias is applied, with minimum power consumption, to the device, to accelerate the electrolytic corrosion of the metallization. Failures are expressed in % /time with 168, 500, and 1000 hour cumulative results reported.

Autoclave

Autoclave is also an environmental stress which measures the moisture resistance of plastic encapsulated devices. Conditions for this test are 121 °C, 100% relative humidity, and 1 atmosphere of pressure (15 psig), with no bias applied to the circuit. Corrosion of the die is the expected failure mechanism. Stressing is usually performed for 144 hours. Failures are expressed in %/time with 48, 96, and 144 hour results reported.

Temperature Cycling

Temperature cycling typically accelerates the effects of the thermal expansion mismatch among the different components within a specific package and circuit. The stress is performed per MIL STD 883, method 1010, Condition B (-55 °C to +125 °C) or C (-65 °C to +150 °C). Stressing is done in an air environment. A cycle consists of ten minutes at -65 °C, five minutes transfer time, and ten minutes at +150 °C. Stressing is typically performed for 1000 cycles. Failures are expressed in %/cycles, with 100, 500, and 1000 cycle results reported.

Thermal Shock

The objective of thermal shock is basically the same as that of temperature cycling - to exercise the difference in thermal expansion coefficients within the integrated circuit package and die. Thermal shock provides additional stress as the device is exposed to a rapid change in temperature, due to a maximum transfer time of ten seconds, as well as the increased thermal conductivity of a liquid environment. This test is performed per MIL STD 883, method 1011, Condition B (-55 °C to +125 °C). In one cycle of thermal shock, devices are placed in a fluorocarbon bath cooled to -55 °C for five minutes, then transferred to an adjacent bath filled with fluorocarbon at 125 °C for five minutes. Stressing is performed for 500 cycles. Failures are expressed in %/cycles, with results reported at 100, 200, and 500 cycles.

Electrostatic Discharge

Electrostatic discharge testing is performed to determine the handling sensitivity of a semiconductor device. This test is performed per MIL STD 883 method 3015, which simulates the resistance (1500Ω) and capacitance (100 pF) of the human body. Also the machine model test is performed with a 0Ω resistance and a capacitance of 200 pF to simulate, as its name implies, a typical insertion tool, handler, etc. that comes in contact with the leads of a semiconductor device.

Latchup

Latchup testing is performed to ascertain whether a device can sustain SCR latchup due to a DC current input. The pin being tested has a DC current forced to it with the device power supplies at nominal voltage and inputs at ground state. Susceptibility of each input is tested with both a positive and negative DC current forced into it. This test is performed per the standard test procedure recognized by JEDEC.

C dv/dt Latchup Testing

This test is performed to evaluate the susceptibility of a CMOS device's power pin to instantaneous ESD discharge into a power supply pin or a rapid ramp of a power pin during power up. Positive and negative pulses are supplied to the power supply pins with a change in voltage of greater than 500 V/µs and a 0 to 5 V risetime of less than 15 ns. Ground, V_{SS}, and the pin under test are connected to ground. The supply current is monitored for excessive current.

III. FAILURE RATE CALCULATIONS

Failures during typical reliability stressing generally are in the infant mortality and random failure sections of the "bathtub" curve. Thermally accelerated failure rates can be derated to actual operating conditions by commonly accepted mathematical models.

Operating life stress is usually reported in the derated form. That is, operating life is performed at 125 °C and results are reported for an equivalent time at a typical operating stress temperature for an application, generally 25 °C, 55 °C, or 70 °C. Failure rates for other temperatures are calculated using a computed acceleration factor.

There are many probability models used in reliability analysis for calculating failure rates. The simplest form of calculating a failure rate (F.R.) would be to divide the number of failures observed after test (N) by the number of device-hours of stress.

$$F.R. = \frac{N}{D \bullet H} \quad (1)$$

where D is the number of devices stressed and H is the number of stress hours. If this number is multiplied by 10^9 we obtain the failure rate expressed as Failure In Time (FIT). FITS are expressed as failures per billion device operating hours.

$$FITS = (F.R.)(10^9) \quad (2)$$

However, using equation (1) allows only for a failure rate calculation at the stress temperature. In order to apply the equation to the desired use temperature we use the well-known Arrhenius relationship to determine the thermal acceleration factor, F_a. One hour of device operation at temperature T_1 is equivalent to F_a hours of operation at temperature T_2. The activation energy, EA, is an important parameter in the Arrhenius equation and is discussed below. The Arrhenius equation is:

$$F_a(T_1 \rightarrow T_2) = e^{-\frac{EA}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)} \quad (3)$$

where k = Boltzman's Constant (8.63×10^{-5} eV/°K) and T_1 is the accelerated stress junction temperature and T_2 is the desired use operating junction temperature in degrees Kelvin.

Junction temperatures, T_1 and T_2, should be used in determining acceleration factors. This temperature can be obtained from the equation below.

$$T_j = T_a + \theta_{ja} P_d \quad (4)$$

where T_a is the operating ambient temperature

and θ_{ja} is the package thermal dissipation (°C/ W) and P_d is the device power dissipation.

Crystal utilizes a low power CMOS process which typically raises the junction temperature about 7 to 15 °C, whereas analog bipolar IC's and hybrids can have power dissipations in the 1 W range. These differences in device junction operating temperatures can greatly affect the acceleration factors. For example, let's calculate the acceleration factors of a device with a power dissipation of 1 watt packaged in a 40 pin ceramic package. This is equivalent to a junction temperature change from 160 °C to 60 °C and from Table 2 the acceleration factor is 277. A typical Crystal device junction temperature is 10 °C higher than the ambient which results in a junction temperature change from 135 °C to 35 °C. This results in an acceleration factor of 636, as shown in Table 2. By comparing the results in Table 2 one can see how derating to a lower use temperature or failing to consider junction temperature when calculating acceleration factors can result in greatly differing failure rates.

TEMPERATURE CHANGE	TYPICAL ACCELERATION FACTOR (.7 E.A.)
125 → 70 °C	26.3
125 → 55 °C	77.5
125 → 25 °C	933.0
135 → 35 °C	636
160 → 60 °C	277

TABLE 2
ACCELERATION FACTORS FOR DIFFERENT TEMPERATURES (E.A. = .7 eV)

E.A.	ACCELERATION FACTOR
1.0	106.0
.9	66.7
.8	41.7
.7	26.3
.6	16.4
.5	10.3
.4	6.5
.3	4.1

TABLE 3
ACCELERATED FACTORS FOR DIFFERENT ACTIVATION ENERGIES (125 °C → 70 °C)

Table 3 compares acceleration factors for different activation energies. Using a 1.0 eV activation energy versus a .7 eV activation energy results in a factor of four increase in the acceleration factor. Crystal uses an activation energy of .7 eV, a conservative value, compared to the .8 eV to 1.0 eV used by some other analog IC vendors.

We now take the failure rate equation (1) at accelerated temperatures expressed in FITS and factor in the acceleration factors from the Arrhenius relationships considering junction temperatures and arrive at the equation below.

$$FITS = \frac{10^9 N}{DHF_a} \quad (5)$$

Using composite Crystal data through the 1st quarter of 1988, a failure rate at 25°C can be calculated by substituting in equation (5) above:

N = 108
D•H = 28,475,272
Fa = 641 (Assuming .7 eV and stress temperature of 125°C, using junction temperature derating)

D•H is the summation of the devices stressed at each readpoint multiplied by that number of stress hours.

Substituting we get:

$$FITS\ 25°C = \frac{(10^9)(108)}{(28{,}475{,}272)(641)} = 5.9\ FITS$$

The Weibull distribution is often used for product life predictions because it can describe increasing and decreasing failure rates. Also the Weibull distribution has both a shape parameter, β, and a scaling parameter, α. This is very useful in accurately describing the shape and scaling of the "bathtub" curve. These more accurate descriptions of the failure rate of the Weibull distribution make

this method superior to the uniform failure distribution described in Equation (1). The Weibull probability distribution function (PDF) f(t) is the probability of failure between time t and t + dt.

$$f(t) = \frac{\beta}{\alpha} t^{(\beta-1)} e^{-\left(\frac{t^{\beta}}{\alpha}\right)} \qquad (6)$$

The Weibull PDF can also be expressed as a function of the Reliability function, R(t), and the instantaneous failure rate function, h(t), therefore:

$$f(t) = h(t)R(t) \qquad (7)$$

The Reliability function is found by integrating the Weibull PDF from t to ∞. This function is the probability that a device will survive to time t.

$$R(t) = \int_{t}^{\infty} f(t')dt' = e^{-\left(\frac{t^{\beta}}{\alpha}\right)} \qquad (8)$$

The instantaneous failure rate function is the probability that a device will fail between time t and t+dt:

$$h(t) = -\frac{1}{R}\frac{dR}{dt} = \frac{\beta}{\alpha} t^{(\beta-1)} \qquad (9)$$

The Reliability function is used to calculate the shape parameter, β, and the time scale parameter, α. The shape parameter is the key function in shaping the infant mortality portion of the "bathtub" curve. A β of 1 indicates a uniform failure rate, β > 1 indicates wearout and β < 1 indicates a declining failure rate. To use Weibull statistics, failures that occur during operating life stresses are used to produce values of R(t). Failure times and R(t) values can be combined to estimate α and β. We first take the natural logarithm of both sides of equation (8).

$$\ln\left(\frac{1}{R(t)}\right) = \frac{t^{\beta}}{\alpha}$$

We again take the natural logarithm and obtain:

$$\ln\left[\ln\frac{1}{R(t)}\right] = \beta \ln(t) - \ln(\alpha) \qquad (10)$$

This last equation is now in the form of a linear function. Using linear regression techniques or Weibull plotting paper we obtain the Weibull shape and scale parameter. Some semiconductor manufacturers perform a burn-in screening on devices to insure that the end customer receives a population of devices that have minimal infant mortality and are from the useful life period of the reliability "bathtub" curve. It is very important to include this data for the entire lifetime of the device to obtain an accurate curve fit for obtaining α and β.

Once the parameters α and β for the Weibull distribution are known we utilize R(t) to calculate FITS. Crystal uses a 10 year lifetime in its FIT calculations and typically uses a 48 hour burn-in at 125 °C hence:

t_{10} = 10 yrs = 87,600 hours
t_1 = 48 hours

The number of devices that will fail in the ten year lifetime following burn-in is given by:

$$N = D\,[R(t_1) - R(t_1 + t_{10})] \qquad (11)$$

where D is the total number of devices stressed. The number of device-hours accumulated in 10 years can be estimated by counting the devices surviving after 10 years.

$$DH \geq D \bullet R(t_1+t_{10}) \bullet t_{10} \qquad (12)$$

Using equation (2) for expressed failures in FITS we obtain the equation below for a Weibull distribution

$$FITS \leq 10^9 \frac{D\,[\,R(t_1) - R(t_1 + t_{10})]}{D \bullet R(t_1 + t_{10}) \bullet (t_{10})}$$

$$= \frac{10^9\,[\,R(t_1) - R\,(t_1+t_{10})]}{R(t_1+ t_{10}) \bullet (t_{10})} \qquad (13)$$

The above equation applies only at the stress temperature. In order to apply the equation to the desired use temperature we factor in the acceleration factors, F_a, from the Arrhenius relationship as it relates to time in the reliability function. Therefore in equation (12) above we replace $R(t_1 + t_{10})$ by $R(t_1 + t_{10}/Fa)$. Note that the device lifetime t_{10} is still 10 years but the reliability function must have the acceleration factor considered for derating to use temperature. Using composite Crystal data through the second quarter of 1993, yields a failure rate at 25 °C of 8.7 FITS.

This failure rate is a more accurate measure of Crystal reliability than that provided by the constant failure rate model of equation (5).

Reliability evaluations involve only samples of an entire population of devices. Therefore a confidence level, (CL), should be placed on the average failure rate. At any time a sample is stressed from a population there exists a finite chance of failures. If many separate samples were stressed from the same population and failure rates plotted, a normal distribution of failure rates would occur. Therefore, valid statistical methods for a normal distribution should be used to determine the desired CL. Confidence levels for reliability analysis are expressed in upper confidence levels (UCL), typically at 60% or 90% depending on the criticality of the device's application. The total sample size stressed is critical in defining the UCL. Therefore rather large sample sizes must be stressed to more accurately demonstrate the true failure rate. A larger spread will exist between the 60% and 90% UCL distribution for smaller sample sizes due to the greater probability that the sample stressed was not representative of the entire population.

Environmental stresses, such as autoclave, temperature cycling, thermal shock, storage life and 85°C/85%R.H., usually have their actual results reported, due to the lack of widely recognized derating models. These stresses are experiments in which a given device will either pass or fail. Test results can be expressed as a simple failure rate - the number of failing devices divided by the total number of devices. However, the true failure rate is usually very small, so often there will be no failures observed. Instead of reporting an observed failure rate of zero, a confidence bound on the true failure rate is determined. Crystal uses a 90% confidence level in a standard formula to determine the test results for environmental stresses.

$$FR = \frac{\chi^2\,(2f+2)}{2n} \qquad (14)$$

The failure rate, FR, is computed by finding an upper bound confidence interval from a standard chi-squared table and dividing it by 2n, where n is the number of parts in the test, and f is the number of failures observed. $\chi^2(2f+2)$ is the right endpoint of the interval starting at zero which spans 90% of the area under the chi-squared curve with $2f+2$ degrees of freedom. This formula results from a Poisson approximation to the Binomial distribution, which is appropriate when the Binomial distribution is heavily skewed towards zero. A chi-squared value arises as an easy way to compute Poisson probabilities. This calculation agrees with the widely accepted lot

6

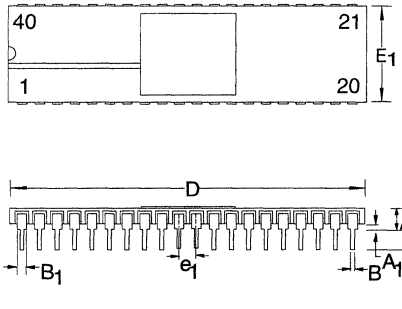
tolerance percent defective, LTPD, plans that are based on 90 % upper confidence.

Of course it is not satisfactory to have accurate methods on reporting failure rates without having programs and methods in place to continuously improve the reliability of the product. Crystal uses methodologies in every level of the company to provide the highest possible quality and reliability standards of its products.

In summary Crystal Semiconductor uses conservative models that are accepted throughout the semiconductor industry to determine the reliability of its devices and has active programs in place to continuously improve the quality and reliability of its devices.

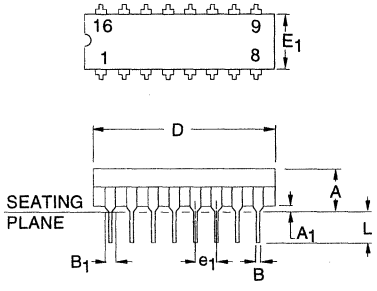
For further information on a summary of Crystal's methods of insuring high quality and reliability standards see the Quality and Reliability information in section 1 of this data book, or contact Crystal's Reliability and Quality Assurance Department at the factory.

MECHANICAL DATA



40 pin
Ceramic
Side-Brazed
DIP

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.18	3.81	4.45	0.125	0.150	0.175
A_1	1.02	1.27	1.52	0.040	0.050	0.060
B	0.38	0.46	0.58	0.015	0.018	0.023
B_1	0.76	1.14	1.52	0.030	0.045	0.060
C	0.20	0.25	0.30	0.008	0.010	0.012
D	50.29	50.80	51.56	1.980	2.000	2.030
E_1	14.75	15.11	15.49	0.580	0.595	0.610
e	15.11	15.49	15.88	0.595	0.610	0.625
e_1	2.41	2.54	2.67	0.095	0.100	0.105
L	3.18	-	4.45	0.125	-	0.175
∝	0°	-	15°	0°	-	15°



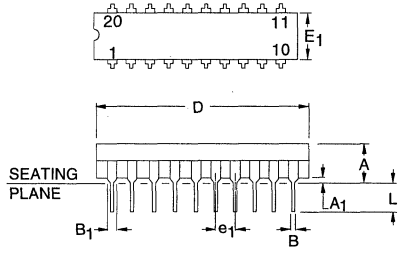
16 pin
CerDIP

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.81	—	5.08	0.150	—	0.200
A_1	0.51	—	1.02	0.020	—	0.040
B	0.38	0.46	0.53	0.015	0.18	0.021
B_1	1.40	—	1.78	0.055	—	0.070
C	0.20	0.25	0.30	0.008	0.010	0.012
D	19.05	19.30	19.94	0.750	0.760	0.785
E_1	6.10	7.24	7.49	0.240	0.285	0.295
e_1	2.41	2.54	2.67	0.095	0.100	0.105
e_A	7.49	7.62	7.75	0.295	0.300	0.305
L	2.92	3.81	4.32	0.115	0.150	0.170
∝	0°	—	15°	0°	—	15°

NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13mm (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER
2. DIMENSION e_A TO CENTER OF LEADS WHEN FORMED PARALLEL.

6

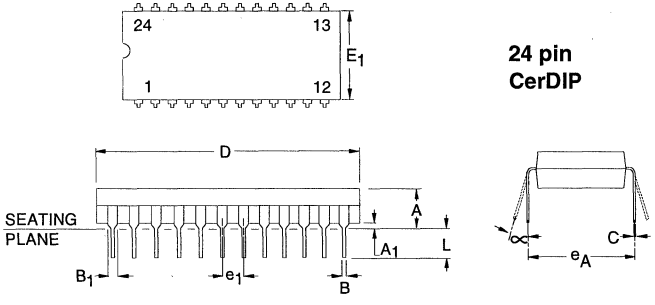


20 pin CerDIP

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	3.81	—	5.08	0.15	—	0.200
A_1	0.51	—	1.02	0.020	—	0.040
B	0.38	0.46	0.53	0.015	0.018	0.021
B_1	1.27	—	1.78	0.050	—	0.070
C	0.20	0.25	0.30	0.008	0.010	0.012
D	23.88	24.26	24.64	0.940	0.955	0.970
E_1	6.60	7.24	7.49	0.260	0.285	0.295
e_1	2.41	2.54	2.67	0.095	0.100	0.105
e_A	7.49	7.62	7.75	0.295	0.300	0.305
L	3.18	3.81	4.32	0.125	0.150	0.170
∝	0°	—	15°	0°	—	15°

NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13mm (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION e_A TO CENTER OF LEADS WHEN FORMED PARALLEL.

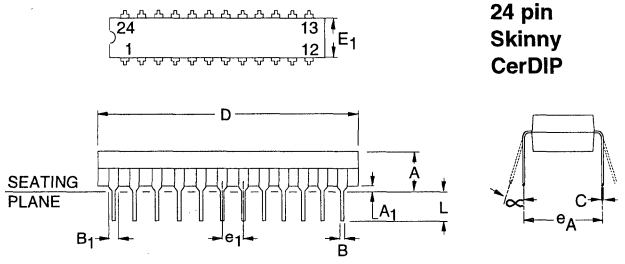


24 pin CerDIP

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	3.81	—	5.08	0.150	—	0.200
A_1	0.51	—	1.02	0.020	—	0.040
B	0.38	0.46	0.53	0.015	0.018	0.021
B_1	1.27	—	1.78	0.050	—	0.070
C	0.20	0.25	0.30	0.008	0.010	0.012
D	31.24	32.0	32.51	1.230	1.260	1.280
E_1	12.95	14.73	15.49	0.510	0.580	0.610
e_1	2.41	2.54	2.67	0.095	0.100	0.105
e_A	15.11	15.24	15.37	0.595	0.600	0.605
L	3.18	3.81	4.32	0.125	0.150	0.170
∝	0°	—	15°	0°	—	15°

NOTES:

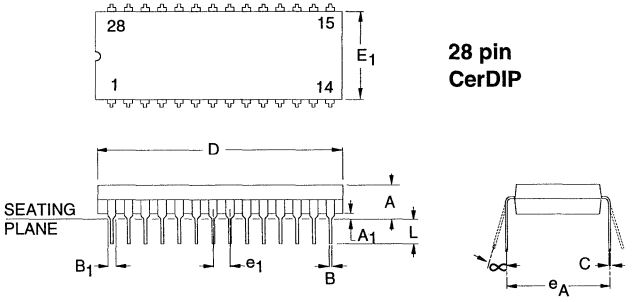
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13mm (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION e_A TO CENTER OF LEADS WHEN FORMED PARALLEL.



24 pin
Skinny
CerDIP

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	3.81	—	5.08	0.150	—	0.200
A_1	0.51	—	1.02	0.020	—	0.040
B	0.38	0.46	0.53	0.015	0.018	0.021
B_1	1.27	—	1.78	0.050	—	0.070
C	0.20	0.25	0.30	0.008	0.010	0.012
D	29.97	32.0	32.51	1.180	1.260	1.280
E_1	5.59	7.11	7.87	0.220	0.280	0.310
e_1	2.41	2.54	2.67	0.095	0.100	0.105
e_A	7.37	7.62	8.13	0.290	0.300	0.320
L	3.18	3.81	4.32	0.125	0.150	0.170
∝	0°	—	15°	0°	—	15°

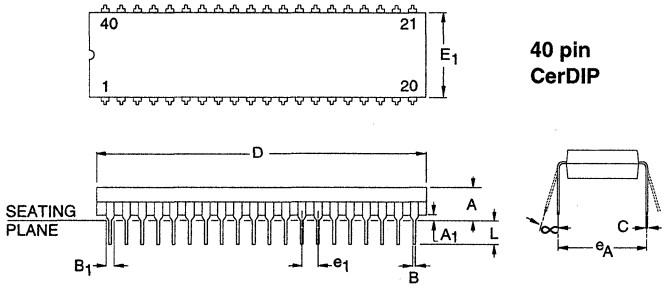
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13mm (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION e_A TO CENTER OF LEADS WHEN FORMED PARALLEL.



28 pin
CerDIP

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	4.06	—	5.84	0.160	—	0.230
A_1	0.51	—	1.27	0.020	—	0.050
B	0.38	0.46	0.56	0.015	0.018	0.022
B_1	1.27	—	1.65	0.050	—	0.065
C	0.20	0.25	0.30	0.008	0.010	0.012
D	36.45	37.08	37.85	1.435	1.460	1.490
E_1	12.70	14.73	15.37	0.500	0.580	0.605
e_1	2.41	2.54	2.67	0.095	0.100	0.105
e_A	15.11	15.24	15.37	0.595	0.600	0.605
L	2.92	3.81	4.06	0.115	0.150	0.160
∝	5°	—	15°	5°	—	15°

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13mm (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION e_A TO CENTER OF LEADS WHEN FORMED PARALLEL.

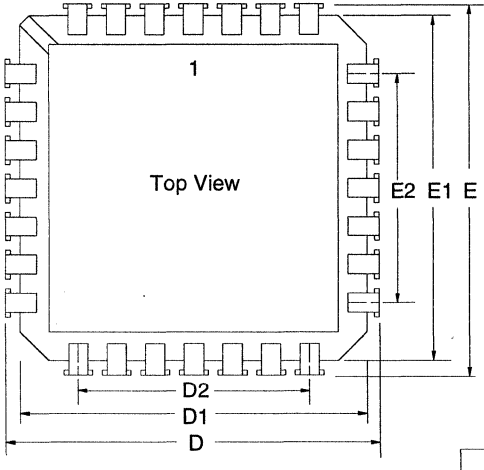


40 pin
CerDIP

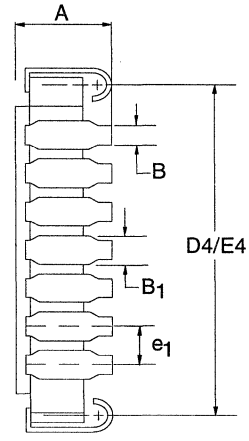
DIM	MILLIMETERS MIN	NOM	MAX	INCHES MIN	NOM	MAX
A	4.06	—	5.84	0.160	—	0.230
A_1	0.51	—	1.27	0.020	—	0.050
B	0.38	0.46	0.56	0.015	0.018	0.022
B_1	1.27	—	1.65	0.050	—	0.065
C	0.20	0.25	0.30	0.008	0.010	0.012
D	50.29	52.32	52.57	1.980	2.060	2.070
E_1	12.70	14.73	15.37	0.500	0.580	0.605
e_1	2.41	2.54	2.67	0.095	0.100	0.105
e_A	15.11	15.24	15.37	0.595	0.600	0.605
L	2.92	3.81	4.06	0.115	0.150	0.160
∝	5°	—	15°	5°	—	15°

NOTES:

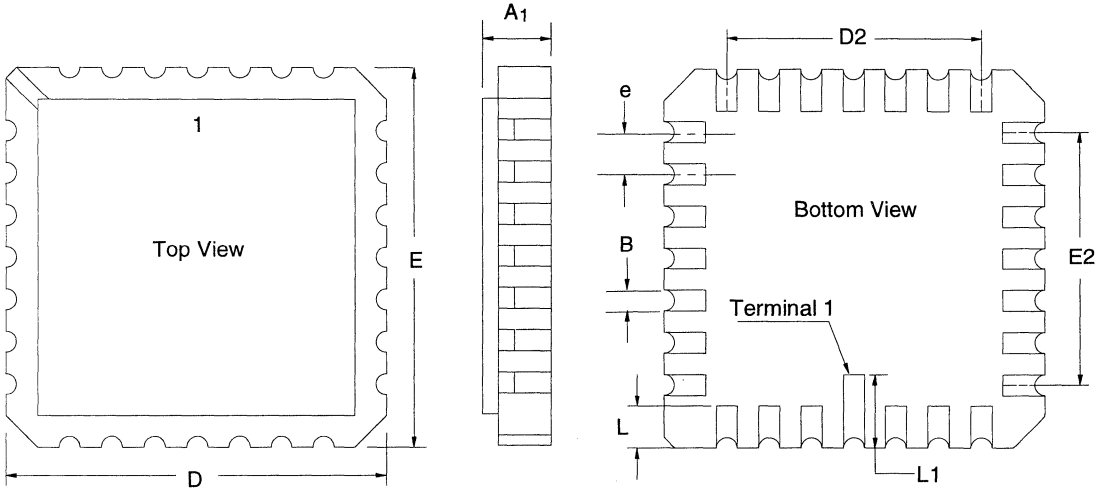
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13mm (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION e_A TO CENTER OF LEADS WHEN FORMED PARALLEL.



28/44 pin
CLCC



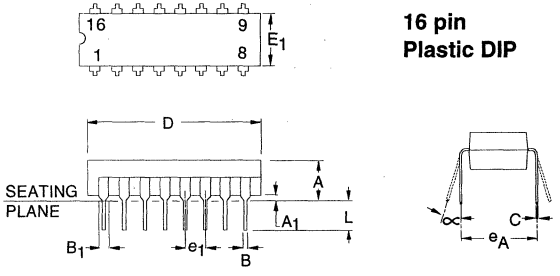
DIM	NO. OF TERMINALS 28 MILLIMETERS MIN	NOM	MAX	28 INCHES MIN	NOM	MAX	44 MILLIMETERS MIN	NOM	MAX	44 INCHES MIN	NOM	MAX
A	2.54	3.05	3.43	0.100	0.120	0.135	2.54	3.05	3.43	0.100	0.120	0.135
B	0.33	0.46	0.58	0.013	0.018	0.023	0.33	0.46	0.58	0.013	0.018	0.023
B_1	0.51	0.64	0.81	0.02	0.025	0.032	0.51	0.64	0.81	0.02	0.025	0.032
D/E	12.19	12.46	12.70	0.480	0.490	0.500	17.27	17.53	17.78	0.680	0.690	0.700
D1/E1	11.18	11.43	11.68	0.440	0.450	0.460	16.26	16.51	16.76	0.640	0.650	0.660
D2/E2	7.49	7.62	7.75	0.295	0.300	0.305	12.57	12.70	12.83	0.495	0.500	0.505
D4/E4	10.80	10.92	11.05	0.425	0.430	0.435	15.88	16.00	16.13	0.625	0.630	0.635
e_1	1.14	1.27	1.40	0.045	0.050	0.055	1.14	1.27	1.40	0.045	0.050	0.055



28/44 pin LCC

	NO. OF TERMINALS											
	28						44					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
A_1	1.57	1.91	2.49	0.062	0.075	0.098	1.57	1.91	2.49	0.062	0.075	0.098
B	0.51	0.64	0.76	0.020	0.025	0.030	0.51	0.64	0.76	0.020	0.025	0.030
D/E	11.25	11.43	11.73	0.443	0.450	0.462	16.33	16.51	16.81	0.643	0.650	0.662
D2/E2	7.49	7.62	7.75	0.295	0.300	0.305	12.57	12.70	12.83	0.495	0.500	0.505
e	1.14	1.27	1.40	0.045	0.050	0.055	1.14	1.27	1.40	0.045	0.050	0.055
L	1.14	1.27	1.40	0.045	0.050	0.055	1.14	1.27	1.40	0.045	0.050	0.055
L1	1.91	2.16	2.41	0.075	0.085	0.095	1.91	2.16	2.41	0.075	0.085	0.095

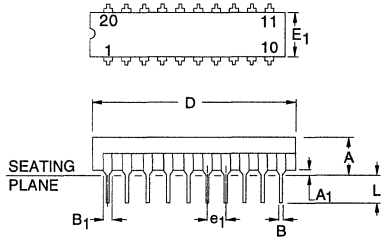
16 pin Plastic DIP



	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	3.94	-	5.08	0.155	-	0.200
A_1	0.51	-	1.02	0.020	-	0.040
B	0.38	0.46	0.53	0.015	0.018	0.021
B_1	0.89	1.27	1.65	0.035	0.050	0.065
C	0.20	0.25	0.38	0.008	0.010	0.015
D	18.93	19.43	19.93	0.745	0.765	0.785
E_1	6.10	6.35	6.60	0.240	0.250	0.260
e_1	2.41	2.54	2.67	0.095	0.100	0.105
e_A	7.62	-	8.25	0.300	-	0.325
L	3.18	-	3.81	0.125	-	0.150
∝	0°	-	15°	0°	-	15°

NOTES:

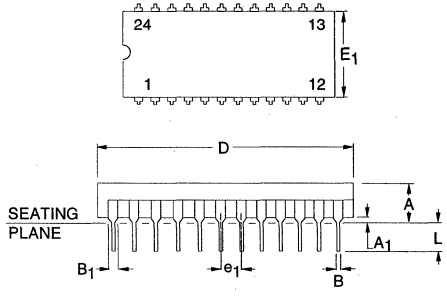
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.13mm (0.005") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION e_A TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION E_1 DOES NOT INCLUDE MOLD FLASH.



20 pin
Plastic DIP

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.94	-	4.57	0.155	-	0.180
A_1	0.51	0.80	1.02	0.020	0.030	0.040
B	0.38	0.46	0.56	0.015	0.018	0.022
B_1	1.27	1.52	1.78	0.050	0.060	0.070
C	0.20	0.25	0.38	0.008	0.010	0.015
D	24.38	25.40	26.42	0.960	1.000	1.040
E_1	6.10	6.35	6.60	0.240	0.250	0.260
e_1	2.41	2.54	2.67	0.095	0.100	0.105
e_A	7.62	7.92	8.25	0.300	0.312	0.325
L	3.18	3.30	3.81	0.125	0.130	0.150
∝	0°	-	15°	0°	-	15°

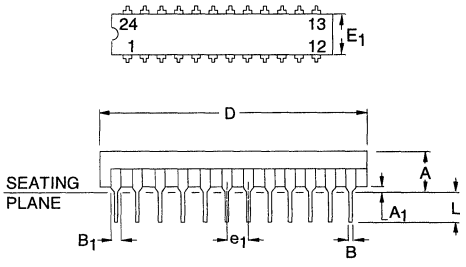
NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25mm (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION e_A TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION E_1 DOES NOT INCLUDE MOLD FLASH.



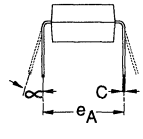
24 pin
Plastic DIP

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.94	4.32	5.08	0.155	0.170	0.200
A_1	0.51	0.76	1.02	0.020	0.030	0.040
B	0.36	0.46	0.56	0.014	0.018	0.022
B_1	1.02	1.27	1.52	0.040	0.050	0.060
C	0.20	0.25	0.38	0.008	0.010	0.015
D	31.37	31.75	32.13	1.235	1.250	1.265
E_1	13.72	13.97	14.22	0.540	0.550	0.560
e_1	2.41	2.54	2.67	0.095	0.100	0.105
e_A	15.24	-	15.87	0.600	-	0.625
L	3.18	-	3.81	0.125	-	0.150
∝	0°	-	15°	0°	-	15°

NOTES:
1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25mm (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION e_A TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION E_1 DOES NOT INCLUDE MOLD FLASH.



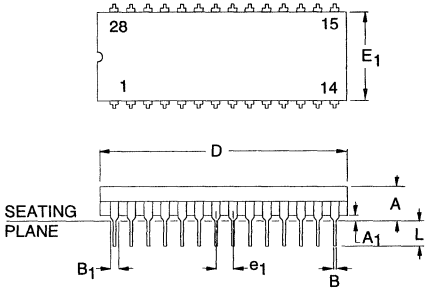
24 pin
Plastic
Skinny DIP



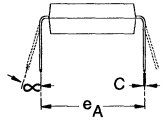
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.94	4.32	4.57	0.155	0.170	0.180
A_1	0.51	0.76	1.02	0.020	0.030	0.040
B	0.36	0.46	0.56	0.014	0.018	0.022
B_1	1.02	1.27	1.65	0.040	0.050	0.065
C	0.20	0.25	0.38	0.008	0.010	0.015
D	31.37	31.75	32.13	1.235	1.250	1.265
E_1	6.10	6.35	6.60	0.240	0.250	0.260
e_1	2.41	2.54	2.67	0.095	0.100	0.105
e_A	7.62	-	8.25	0.300	-	0.325
L	3.18	-	3.81	0.125	-	0.150
∝	0°	-	15°	0°	-	15°

NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25mm (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION e_A TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION E_1 DOES NOT INCLUDE MOLD FLASH.



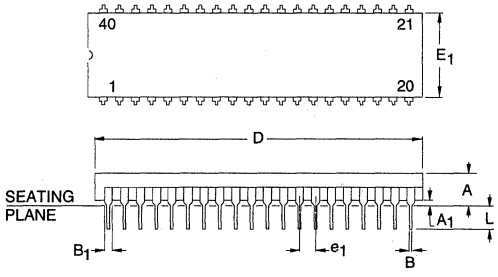
28 pin
Plastic DIP



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.94	4.32	5.08	0.155	0.170	0.200
A_1	0.51	0.76	1.02	0.020	0.030	0.040
B	0.36	0.46	0.56	0.014	0.018	0.022
B_1	1.02	1.27	1.65	0.040	0.050	0.065
C	0.20	0.25	0.38	0.008	0.010	0.015
D	36.45	36.83	37.21	1.435	1.450	1.465
E_1	13.72	13.97	14.22	0.540	0.550	0.560
e_1	2.41	2.54	2.67	0.095	0.100	0.105
e_A	15.24	-	15.87	0.600	-	0.625
L	3.18	-	3.81	0.125	-	0.150
∝	0°	-	15°	0°	-	15°

NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25mm (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION e_A TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION E_1 DOES NOT INCLUDE MOLD FLASH.

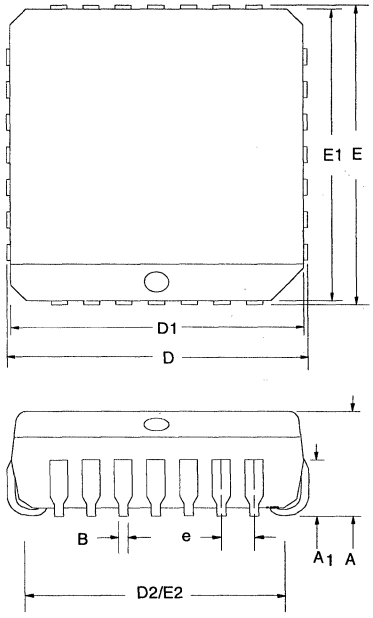


40 pin
Plastic DIP

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.94	4.32	5.08	0.155	0.170	0.200
A_1	0.51	0.76	1.02	0.020	0.030	0.040
B	0.36	0.46	0.56	0.014	0.018	0.022
B_1	1.02	1.27	1.65	0.040	0.050	0.065
C	0.20	0.25	0.38	0.008	0.010	0.015
D	51.69	52.20	52.71	2.035	2.055	2.075
E_1	13.72	13.97	14.22	0.540	0.550	0.560
e_1	2.41	2.54	2.67	0.095	0.100	0.105
e_A	15.24	-	15.87	0.600	-	0.625
L	3.18	-	3.81	0.125	-	0.150
∝	0°	-	15°	0°	-	15°

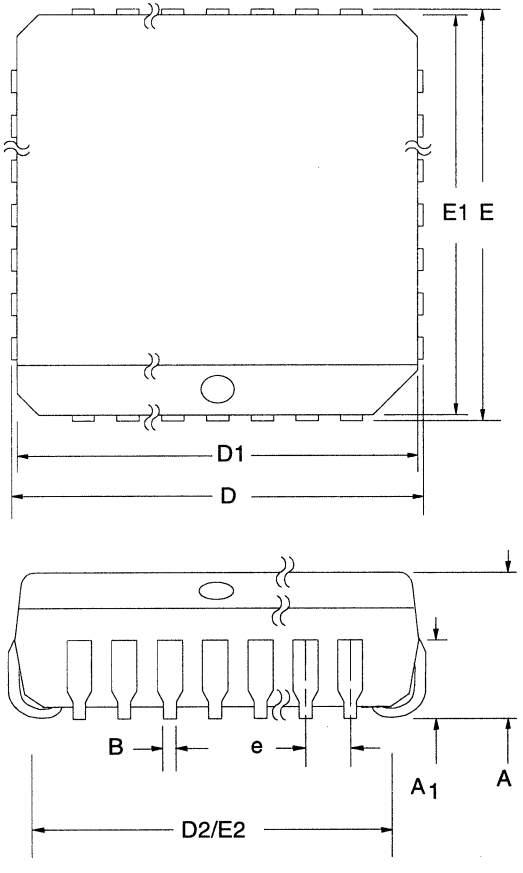
NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25mm (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION e_A TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION E_1 DOES NOT INCLUDE MOLD FLASH.



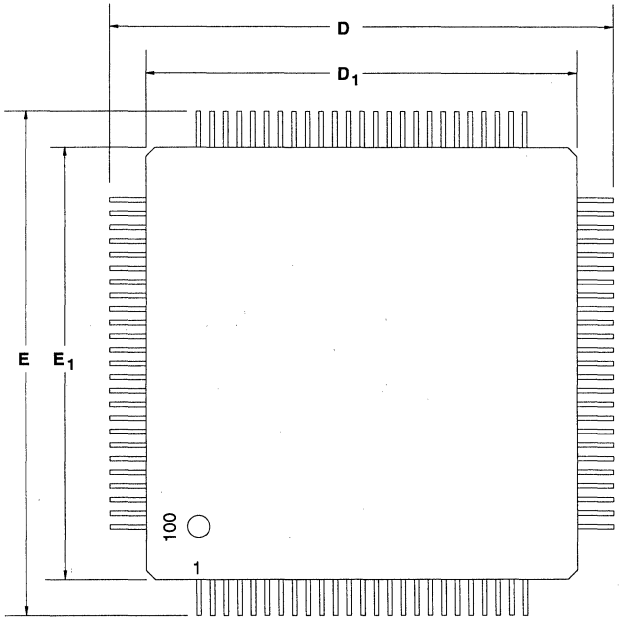
28/44 pin
PLCC

DIM	NO. OF TERMINALS											
	28						44					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
A	4.20	4.45	4.57	0.165	0.175	0.180	4.20	4.45	4.57	0.165	0.175	0.180
A_1	2.29	2.79	3.04	0.090	0.110	0.120	2.29	2.79	3.04	0.090	0.110	0.120
B	0.33	0.41	0.53	0.013	0.016	0.021	0.33	0.41	0.53	0.013	0.016	0.021
D/E	12.32	12.45	12.57	0.485	0.490	0.495	17.40	17.53	17.65	0.685	0.690	0.695
D1/E1	11.43	11.51	11.58	0.450	0.453	0.456	16.51	16.59	16.66	0.650	0.653	0.656
D2/E2	9.91	10.41	10.92	0.390	0.410	0.430	14.99	15.50	16.00	0.590	0.610	0.630
e	1.19	1.27	1.35	0.047	0.050	0.053	1.19	1.27	1.35	0.047	0.050	0.053

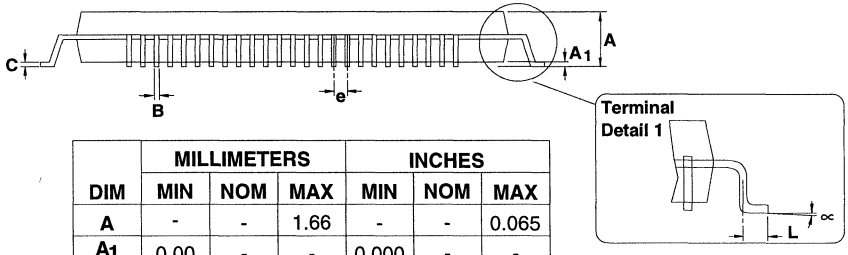


68 pin
PLCC

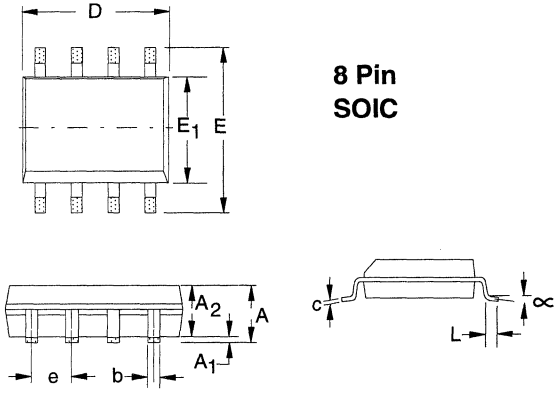
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.20	4.45	5.08	0.165	0.175	0.200
A_1	2.29	2.79	3.30	0.090	0.110	0.130
B	0.38	0.41	0.53	0.013	0.016	0.021
D/E	25.02	25.15	25.27	0.985	0.990	0.995
D1/E1	24.13	24.23	24.33	0.950	0.954	0.958
D2/E2	22.61	23.11	23.62	0.890	0.910	0.930
e	1.14	1.27	1.40	0.045	0.050	0.055



100 pin
TQFP

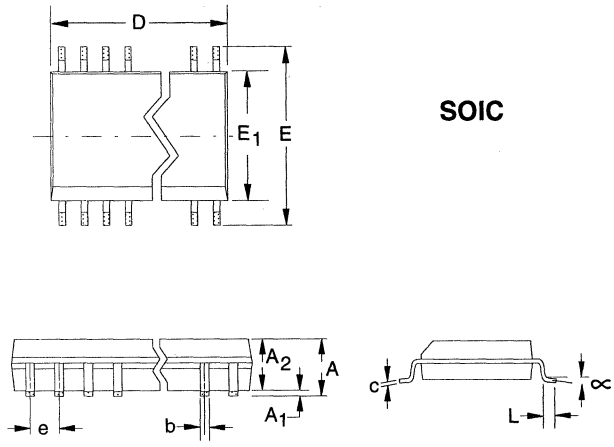


	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.66	-	-	0.065
A_1	0.00	-	-	0.000	-	-
B	0.14	0.20	0.26	0.006	0.008	0.010
C	0.40	0.51	0.60	0.016	0.020	0.024
D	15.70	16.00	16.30	0.618	0.630	0.642
D_1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.70	16.00	16.30	0.618	0.630	0.642
E_1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.077	0.13	0.177	0.003	0.005	0.007
L	0.30	0.51	0.70	0.012	0.020	0.028
∝	0°	-	12°	0°	-	12°



8 Pin SOIC

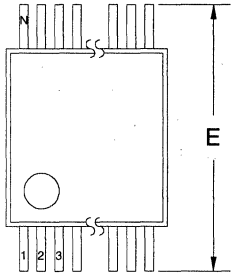
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.78	1.96	2.13	0.070	0.077	0.084
A_1	0	-	0.25	0	-	0.010
A_2	1.78	1.83	1.88	0.070	0.072	0.074
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.23	5.28	5.33	0.206	0.208	0.210
E	7.67	7.87	8.08	0.302	0.310	0.318
E_1	5.18	5.30	5.38	0.204	0.208	0.212
e	1.14	1.27	1.40	0.045	0.050	0.055
L	0.48	-	0.76	0.019	-	0.030
∝	0°	-	8°	0°	-	8°



SOIC

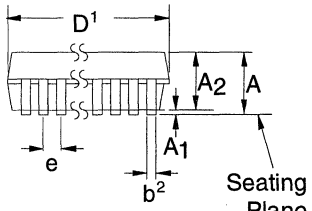
pins	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
16	9.91	10.16	10.41	0.390	0.400	0.410
20	12.45	12.70	12.95	0.490	0.500	0.510
24	14.99	15.24	15.50	0.590	0.600	0.610
28	17.53	17.78	18.03	0.690	0.700	0.710

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.41	2.54	2.67	0.095	0.100	0.105
A_1	0.127	-	0.300	0.005	-	0.012
A_2	2.29	2.41	2.54	0.090	0.095	0.100
b	0.33	0.46	0.51	0.013	0.018	0.020
c	0.203	0.280	0.381	0.008	0.011	0.015
D	see table above					
E	10.11	10.41	10.67	0.398	0.410	0.420
E_1	7.42	7.49	7.57	0.292	0.295	0.298
e	1.14	1.27	1.40	0.040	0.050	0.055
L	0.41	-	0.89	0.016	-	0.035
∝	0°	-	8°	0°	-	8°

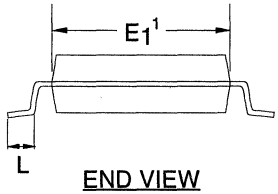


TOP VIEW

SSOP Package Dimensions



SIDE VIEW



END VIEW

NOTES:
1. DIMENSIONS D AND E_1 ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.20mm PER SIDE.
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13mm TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.07mm AT LEAST MATERIAL CONDITION.
3. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25mm FROM LEAD TIPS.

	MILLIMETERS			INCHES			
DIM	MIN	NOM	MAX	MIN	NOM	MAX	Note
A	-	-	2.13	-	-	0.084	
A_1	0.05	0.15	0.25	0.002	0.006	0.010	
A_2	1.62	1.75	1.88	0.064	0.070	0.074	
b	0.22	0.30	0.38	0.009	0.012	0.015	2, 3
D	see other table			see other table			1
E	7.40	7.80	8.20	0.291	0.307	0.323	
E_1	5.00	5.30	5.60	0.197	0.209	0.220	1
e	0.61	0.65	0.69	0.024	0.026	0.027	
L	0.63	0.90	1.03	0.025	0.035	0.040	
N	see other table			see other table			
∝	0°	4°	8°	0°	4°	8°	

	D						
	MILLIMETERS			INCHES			
N	MIN	NOM	MAX	MIN	NOM	MAX	Note
20	6.90	7.20	7.50	0.272	0.283	0.295	1
28	9.90	10.20	10.50	0.390	0.402	0.413	1

STANDARD MILITARY DRAWINGS

Crystal Semiconductor manufactures A/D converters which meet specifications as defined by DESC approved Standard Military Drawings. The following cross reference list is provided to assist in the converter selection process. The SMD (Standard Military Drawing) should be used to determine specifications. Devices are marked with the DESC SMD part number, not with the equivalent Crystal Semiconductor part number. Consequently, orders can only be accepted for the DESC SMD part number.

Standard Military Drawing Cross Refence

Crystal Part Number	DESC SMD Part Number
CS5012-TD12B	5962-8967901QA
CS5012-TE12B	5962-8967901XA
CS5014-SD14B	5962-8967401QA
CS5014-SE14B	5962-8967401XA
CS5014-TD14B	5962-8967402QA
CS5014-TE14B	5962-8967402XA
CS5016-SD16B	5962-8967601QA
CS5016-SE16B	5962-8967601XA
CS5016-TD16B	5962-8967602QA
CS5016-TE16B	5962-8967602XA
CS5412-TC1B	5962-9095701MQA
CS5412-TJ1B	5962-9195701MXA
CS5412-SC1B	5962-9095702MQA
CS5412-SJ1B	5962-9095702MXA
CS5101A-SD8B	5962-9169101MXX
CS5101A-SE8B	5962-9169101M3X
CS5101A-TD8B	5962-9469102MXX
CS5101A-TE8B	5962-9169102M3X
CS5102A-SDB	5962-9169201MXX
CS5102A-SEB	5962-9169201M3X
CS5102A-TDB	5962-9169202MXX
CS5102A-TEB	5962-9169202M3X
CS5336-TCB	5962-9469001MXX

• Notes •

CONTENTS

UNITED STATES

SALES OFFICES

WESTERN AREA

Sales Office and Applications Support:
Crystal Semiconductor Corp.
50 Airport Parkway
San Jose, CA 95110
Ph: 408-437-7743
FAX: 408-437-4943

Crystal Semiconductor Corp.
27281 Las Ramblas, Suite 200
Mission Viejo, CA 92691
Ph: 714-348-8770
FAX: 714-348-9556

CENTRAL AREA

Crystal Semiconductor Corp.
P.O. Box 17847, 78760
4210 S. Industrial Dr.
Austin, TX 78744
Ph: 512-445-7222
FAX: 512-445-7581

EASTERN AREA

Crystal Semiconductor Corp.
5511 Capital Center Dr., Suite 103
Raleigh, NC 27606
Ph: 919-859-5393
FAX: 919-859-5334

Crystal Semiconductor Corp.
Salem Business Center
68 Stiles Rd., unit H
Salem, NH 03079
Ph: 603-894-5544
FAX: 603-894-5533

SALES REPRESENTATIVES

ALABAMA

CP&F, Inc.
2317 Starmount Circle
P.O. Box 1424
Huntsville, AL 35807
Ph: 205-536-1506
FAX: 205-551-0558

ALASKA

Call Crystal Head Office
Ph: 512-445-7222

ARIZONA

Western High Tech Marketing, Inc.
9414 E. San Salvador, Suite 206
Scottsdale, AZ 85258
Ph: 602-860-2702
FAX: 602-860-2712

ARKANSAS

TL Marketing, Inc.
14850 Quorum Dr., Suite 100
Dallas, TX 75240
Ph: 214-490-9300
FAX: 214-960-6075

CALIFORNIA

Earle Associates, Inc.
7585 Ronson Rd., Suite 200
San Diego, CA 92111
Ph: 619-278-5441
FAX: 619-278-5443
Easylink: 62835672

Bager Electronics
17220 Newhope St., Suite 209
Fountain Valley, CA 92708
Ph: 714-957-3367
FAX: 714-546-2654

Bager Electronics
6324 Variel Ave., Suite 314
Woodland Hills, CA 91367
Ph: 818-712-0011
FAX: 818-712-0160

NORCOMP, Inc.
1267 Oakmead Parkway
Sunnyvale, CA 94086
Ph: 408-733-7707
FAX: 408-774-1947

NORCOMP, Inc.
8880 Wagon Way
Granite Bay, CA 95746
Ph: 916-791-7776
FAX: 916-791-2223

COLORADO

PromoTech
2901 S. Colorado Blvd., Suite A
Denver, CO 80222
Ph: 303-692-8484
FAX: 303-692-8416

CONNECTICUT

Alpha-Omega Sales Corp.
325 Main St., Suite 301
North Reading, MA 01864
Ph: 508-664-1118
FAX: 508-664-3212

DELAWARE

Nexus Technology Sales, Inc.
200 Lakeside Dr., Suite 236
Horsham, PA 19044
Ph: 215-675-9600
FAX: 215-675-9604

DISTRICT OF COLUMBIA

New Era Sales, Inc.
890 Airport Park Rd., Suite 103
Glen Burnie, MD 21061-2559
Ph: 410-761-4100
FAX: 410-761-2981

FLORIDA
CP&F Florida, Inc.
7335 Lake Ellenor Dr.
P.O. Box 593229
Orlando, FL 32809-6219
Ph: 407-855-0843
FAX: 407-851-1464

GEORGIA
CP&F Florida, Inc.
2866 Buford Hwy.
Duluth, GA 30136
Ph: 404-497-9404
FAX: 404-497-9412

HAWAII
Call Crystal Head Office
Ph: 512-445-7222

IDAHO
Anderson Associates
270 S. Main St., Suite 108
Bountiful, UT 84010
Ph: 801-292-8991
FAX: 801-298-1503

ILLINOIS
Micro Sales Inc.
901 W. Hawthorn
Itasca, IL 60143
Ph: 708-285-1000
FAX: 708-285-1008

Stan Clothier Co.
3910 Old Hwy. 94 S., Suite 116
St. Charles, MO 63304
Ph: 314-928-8078
FAX: 314-447-5214

INDIANA
TMC Electronics
1526 E. Greyhound Pass
Carmel, IN 46032-1036
Ph: 317-844-8462
FAX: 317-573-5472

TMC Electronics
4630-10 W. Jefferson Blvd.
Ft. Wayne, IN 46804-6800
Ph: 219-432-5553
FAX: 219-432-5555

TMC Electronics
1218 Appletree Ln
Kokomo, IN 46902
Ph: 317-459-5152
FAX: 317-457-3822

IOWA
Stan Clothier Co.
1930 St. Andrews N.E.
Cedar Rapids, IA 52402
Ph: 319-393-1576
FAX: 319-393-7317

KANSAS
Stan Clothier Co.
13000 W. 87th St. Parkway, Suite 105
Lenexa, KS 66215
Ph: 913-492-2124
FAX: 913-492-1855

KENTUCKY
TMC Electronics
100 Trade St., Suite 1A
Lexington, KY 40510-1007
Ph: 606-253-1808
FAX: 606-253-1662

LOUISIANA
TL Marketing, Inc.
14343 Torrey Chase Blvd., Suite 1
Houston, TX 77014
Ph: 713-587-8100
FAX: 713-580-7517

MAINE
Alpha-Omega Sales Corp.
325 Main St., Suite 301
North Reading, MA 01864
Ph: 508-664-1118
FAX: 508-664-3212

MARYLAND
New Era Sales, Inc.
890 Airport Park Rd., Suite 103
Glen Burnie, MD 21061-2559
Ph: 410-761-4100
FAX: 410-761-2981

MASSACHUSETTS
Alpha-Omega Sales Corp.
325 Main St., Suite 301
North Reading, MA 01864
Ph: 508-664-1118
FAX: 508-664-3212

MICHIGAN
J.M.J. & Associates, Inc.
5075 Cascade Rd. S.E.
Grand Rapids, MI 49546
Ph: 616-285-8887
FAX: 616-285-7633

MINNESOTA
The Twist Company
12800 Industrial Park Blvd., Suite 150
Plymouth, MN 55441
Ph: 612-550-0922
FAX: 612-550-0925

MISSISSIPPI
CP&F, Inc.
2317 Starmount Circle
P.O. Box 1424
Huntsville, AL 35807
Ph: 205-536-1506
FAX: 205-551-0558

MISSOURI
Stan Clothier Co.
3910 Old Hwy. 94 S., Suite 116
St. Charles, MO 63304
Ph: 314-928-8078
FAX: 314-447-5214

MONTANA
PromoTech
2901 S. Colorado Blvd., Suite A
Denver, CO 80222
Ph: 303-692-8484
FAX: 303-692-8416

NEBRASKA
Stan Clothier Co.
13000 W. 87th St. Parkway, Suite 105
Lenexa, KS 66215
Ph: 913-492-2124
FAX: 913-492-1855

NEVADA
NORCOMP, Inc.
1267 Oakmead Parkway
Sunnyvale, CA 94086
Ph: 408-733-7707
FAX: 408-774-1947

NEW HAMPSHIRE
Alpha-Omega Sales Corp.
325 Main St., Suite 301
North Reading, MA 01864
Ph: 508-664-1118
FAX: 508-664-3212

NEW JERSEY (NORTH)
Nexus Technology Sales
2460 Lemoine Ave.
Fort Lee, N.J. 07024
Ph: 201-947-0151
FAX: 201-947-0163

NEW JERSEY (SOUTH)
Nexus Technology Sales, Inc.
200 Lakeside Dr., Suite 236
Horsham, PA 19044
Ph: 215-675-9600
FAX: 215-675-9604

NEW YORK
Nexus Technology Sales
2460 Lemoine Ave.
Fort Lee, NJ 07024
Ph: 201-947-0151
FAX: 201-947-0163

Bob Dean, Inc.
P.O. Box 4568
Ithaca, NY 14852-4568
Ph: 607-257-1111
FAX: 607-257-3678

Bob Dean, Inc.
Hollowbrook Park, Suite 1D
15 Myers Corner Rd.
Wappingers Falls, NY 12590
Ph: 914-297-6406
FAX: 914-297-5676

NORTH CAROLINA
CPF Atlantic, Inc.
1 Centerview Dr., Suite 306
Greensboro, NC 27407
Ph: 910-852-4498
FAX: 910-852-4556

OHIO
TMC of Ohio
9200 Montgomery Rd., Suite 11A
Cincinnati, OH 45242
Ph: 513-984-6720
FAX: 513-984-6874

TMC Electronics
One Independence Place
4807 Rockside Rd., Suite 360
Independence, OH 44131
Ph: 216-520-0150
FAX: 216-520-0190

OKLAHOMA
TL Marketing, Inc.
14850 Quorum Dr., Suite 100
Dallas, TX 75240
Ph: 214-490-9300
FAX: 214-960-6075

OREGON
Call Crystal San Jose, CA Office
Ph: 408-437-7743

PENNSYLVANIA
TMC Electronics
One Independence Place
4807 Rockside Rd., Suite 360
Independence, OH 44131
Ph: 216-520-0150
FAX: 216-520-0190

Nexus Technology Sales, Inc.
200 Lakeside Dr., Suite 236
Horsham, PA 19004
Ph: 215-675-9600
FAX: 215-675-9604

RHODE ISLAND
Alpha-Omega Sales Corp.
325 Main St., Suite 301
North Reading, MA 01864
Ph: 508-664-1118
FAX: 508-664-3212

SOUTH CAROLINA
CPF Atlantic, Inc.
1 Centerview Dr., Suite 306
Greensboro, NC 27407
Ph: 919-852-4498
FAX: 919-852-4556

SOUTH DAKOTA
The Twist Co.
12800 Industrial Park Blvd., Suite 150
Plymouth, MN 55441
Ph: 612-550-0922
FAX: 612-550-0925

TENNESSEE (WEST)
CP&F, Inc.
2317 Starmount Circle
P.O. Box 1424
Huntsville, AL 35807
Ph: 205-536-1506
FAX: 205-551-0558

TENNESSEE (EAST)
CP&F, Florida
2866 Buford Hwy
Duluth, GA 30136
Ph: 404-497-9404
FAX: 404-497-9412

TEXAS
TL Marketing, Inc.
8100 Shoal Creek, Suite 250
Austin, TX 78758
Ph: 512-371-7272
FAX: 512-371-0727

TL Marketing, Inc.
14343 Torrey Chase Blvd., Suite 1
Houston, TX 77014
Ph: 713-587-8100
FAX: 713-580-7517

TL Marketing
14850 Quorum Dr., Suite 100
Dallas, TX 75240
Ph: 214-490-9300
FAX: 214-960-6075

UTAH
Anderson Associates
270 S. Main St., Suite 108
Bountiful, UT 84010
Ph: 801-292-8991
FAX: 801-298-1503

VERMONT
Alpha-Omega Sales Corp.
325 Main St., Suite 301
North Reading, MA 01864
Ph: 508-664-1118
FAX: 508-664-3212

VIRGINIA
New Era Sales, Inc.
890 Airport Park Rd., Suite 103
Glen Burnie, MD 21061-2559
Ph: 410-761-4100
FAX: 410-761-2981

WASHINGTON
Call Crystal San Jose, CA Office
Ph: 408-437-7743

WEST VIRGINIA
TMC Electronics
7838 Laurel Ave.
Cincinnati, OH 45243-2609
Ph: 513-271-3860
Fax: 513-271-6321

WISCONSIN (S.E.)
Micro Sales, Inc.
210 Regency Court, Suite L100
Brookfield, WI 53045
Ph: 414-786-1403
FAX: 414-786-1813

WISCONSIN (N.W.)
The Twist Co.
12800 Industrial Park Blvd., Suite 150
Plymouth, MN 55441
Ph: 612-550-0922
FAX: 612-550-0925

WYOMING
PromoTech
2901 S. Colorado Blvd., Suite A
Denver, CO 80222
Ph: 303-692-8484
FAX: 303-692-8416

U. S. DISTRIBUTORS

ALABAMA

Insight Electronics, Inc.
4835 University Square, Suite 19
Huntsville, AL 35816
Ph: 205-830-1222
FAX: 205-830-1225

Nu Horizons Electronics
4835 University Square, Suite 10
Huntsville, AL 35816
Ph: 205-722-9330
FAX: 205-722-9348

ARIZONA

Insight Electronics
Tempe, AZ
1515 W. University Dr., Suite 103
Tempe, AZ 85281
Ph: 602-829-1800
Ph: 602-792-1800 (Tucson)
Ph: 505-823-1800 (New Mexico)
FAX: 602-967-2658

CALIFORNIA

(Los Angeles)
Insight Electronics
4333 Park Terrace Dr., Suite 101
West Lake Village, CA 91361
(San Fernando Valley)
Ph: 818-707-2101
FAX: 818-707-0321

(Orange County)
Insight Electronics, Inc.
Two Venture Plaza, Suite 340
Irvine, CA 92718
Ph: 714-727-3291
FAX: 714-727-1804

Insight Electronics
9980 Huennekens
San Diego, CA 92121
Ph: 619-587-1100
FAX: 619-677-3151

Insight Electronics
1295 Oakmead Parkway
Sunnyvale, CA 94086
Ph: 408-720-9222
FAX: 408-720-8390

Nu Horizons Electronics
2070 Ringwood Ave.
San Jose, CA 95131
Ph: 408-434-0800
FAX: 408-434-0935

COLORADO

Insight Electronics
384 Inverness Dr. S., Suite 105
Englewood, CO 80112
Ph: 303-649-1800
FAX: 303-649-1818

FLORIDA

Nu Horizons Electronics
3421 N.W. 55th St.
Fort Lauderdale, FL 33309
Ph: 305-735-2555
FAX: 305-735-2880

Nu Horizons Electronics
600 S. North Lake Blvd., Suite 270
Altamonte Springs, FL 32701
Ph: 407-831-8008
FAX: 407-831-8862

Insight Electronics
600 S. North Lake Blvd., Suite 250
Altamonte Springs, FL 32701
Ph: 407-834-6310
FAX: 407-834-6461

Insight Electronics
621 N.W. 53rd St., Suite 240
Boca Raton, FL 33487
Ph: 407-995-1486
FAX: 407-995-1487

Insight Electronics
13575 58th St. N., Suite 149
Clearwater, FL 34620
Ph: 813-524-8850
FAX: 813-538-4134

GEORGIA

Nu Horizons Electronics
5555 Oakbrook Parkway, Suite 340
Norcross, GA 30093
Ph: 404-416-8666
FAX: 404-416-9060

Insight Electronics, Inc.
3005 Breckinridge, Bldg 210A
Duluth, GA 30136
Ph: 404-717-8566
FAX: 404-717-8588

ILLINOIS
Insight Electronics, Inc.
1365 Wiley Rd., Suite 142
Schaumburg, IL 60173
Ph: 708-885-9700
FAX: 708-885-9701

MARYLAND
Nu Horizons Electronics
8975 Guilford Rd., Suite 120
Columbia, MD 21046
Ph: 410-995-6330
FAX: 410-995-6332

Insight Electronics, Inc.
6925 Oakland Mills Rd., Suite D
Columbia, MD 21045
Ph: 410-381-3131
FAX: 410-381-3141

MASSACHUSETTS
Nu Horizons Electronics
19 Corporate Place
107 Audubon Rd., Bldg 1
Wakefield, MA 01880
Ph: 617-246-4442
FAX: 617-246-4462

Insight Electronics
55 Cambridge St., Suite 301
Burlington, MA 01803
Ph: 617-270-9400
FAX: 617-270-3279

MINNESOTA
Insight Electronics
5353 Gamble Dr., Suite 330
St. Louis Park, MN 55416
Ph: 612-525-9999
Fax: 612-525-9998

NEW JERSEY
Nu Horizons Electronics
39 U.S. Route 46
Pine Brook, NJ 07058
Ph: 201-882-8300
FAX: 201-882-8398

Nu Horizons Electronics
18000 Horizon Way, Suite 200
Mount Laurel, NJ 08054
Ph: 609-231-0900
FAX: 609-231-9510

Insight Electronics, Inc.
2 Eves Dr., Suite 208
Marlton, NJ 08053
Ph: 609-985-5556
FAX: 609-985-5895

NEW YORK
Nu Horizons Electronics
6000 New Horizons Blvd.
North Amityville, NY 11701
PH: 516-226-6000
FAX: 516-226-5886

Nu Horizons Electronics
333 Metro Park
Rochester, NY 14623
Ph: 716-292-0777
FAX: 716-292-0750

OHIO
Nu Horizons Electronics
6200 Sam Center Rd., Suite A15
Solon, OH 44139
Ph: 216-349-2008
FAX: 216-349-2080

Insight Electronics, Inc.
115 E. Aurora Rd., Suite 101
Northfield, OH 44067
Ph: 216-467-2522
FAX: 216-0467-3412

OREGON
Insight Electronics
8705 S.W. Numbus, Suite 200
Beaverton, OR 97005
Ph: 503-644-3300
FAX: 503-641-4530

TEXAS
(Dallas)
Insight Electronics
1778 N. Plano Rd., Suite 320
Richardson, TX 75081
Ph: 214-783-0800 (Richardson)
Ph: 817-338-0800 (Ft. Worth)
FAX: 214-680-2402

Insight Electronics
10777 Westheimer, Suite 1100
Houston, TX 77042
Ph: 713-260-9614

Insight Electronics
11500 Metric Blvd.
Austin, TX 78758
Ph: 512-719-3090
FAX: 512-719-3091

Nu Horizons Electronics
2081 Hutton Dr., Suite 119
Carrollton, TX 75006
Ph: 214-488-2255
FAX: 214-488-2265

WASHINGTON
Insight Electronics
12002 115th Ave. N.E.
Kirkland, WA 98034
Ph: 206-820-8100
FAX: 206-821-2976

CANADA

REPRESENTATIVES

BRITISH COLUMBIA

MICROWE Electronics Corp.
5330 Wallace Ave.
Delta, BC
Canada, V4M 1A1
Ph: 604-943-5020
FAX: 604-943-8184

ONTARIO

InTELaTECH Inc.
5225 Orbitor Dr., Suite 2
Mississauga, Ontario
Canada, L4W 4Y8
Ph: 905-629-0082
FAX: 905-629-1795

InTELaTECH Inc.
260 Hearst Way, Suite 248
Kanata, Ontario
Canada, K2L 3H1
Ph: 613-599-7330
FAX: 613-599-7329

QUEBEC

InTELaTECH Inc.
6765 Cote De Liesse, Suite 366
St. Laurent, Quebec
Canada, H4T 1A7
Ph: 514-343-4877
FAX: 514-343-4355

EUROPE

SALES OFFICES

European Sales Office and Applications Support:

Crystal Semiconductor (UK) Ltd.
Spectrum Point,
279, Farnborough Rd.,
Farnborough,
Hampshire GU14 7LS,
England
Ph: +44(0)1252372762
FAX: +44(0)1252372763

Crystal Semiconductor
Muhlfelder-Strasse 2
D-82211 Herrsching
Germany
Ph: +49(08152)40088
FAX: +49(08152)40077

EUROPEAN DISTRIBUTORS

AUSTRIA

Eurodis Electronics GmbH
Lamezanstrasse 10
A-1232Wien
Austria
Ph: +43(1)61062-0
(In Austria) (0222)61062-0
FAX: +43(1)61062-151
(In Austria) (0222)61062-151

BELGIUM & LUXEMBOURG

Alcom Electronics NV/SA
Singel 3
2550 Kontich
Belgium
Ph: +32(0345)83033
FAX: +32(0345)83126

DENMARK

Scansupply A/S
Blokken 44
3460 Birkerød
Denmark
Ph: +45(045)825090
FAX: +45(045)825440

Scansupply A/S
Marselisborg Havnevej 36
8000 Århus C.
Denmark
Ph: +45(045)825090
FAX: +45(086)127718

FINLAND
Integrated Electronics OyAB
Turkhaudantie 1
SF-00700 Helsinki
Finland
Ph: +358(0)3513133
FAX: +358(0)3513134

FRANCE
Newtek S. A.
8, Rue De L'Esterel
Silic 583
94663 Rungis Cedex
France
Ph: +33(01468)72200
FAX: +33(014687)8049

Newtek Sud-Est
4, Rue de l'Europe
ZAC Font-Ratel
38640 CLAIX
France
Ph: +33(076)985601
FAX: +33(076)981604

GERMANY
Atlantik Elektronik GmbH
Fraunhoferstrasse, 11A
D-82152 Planegg
Germany
Ph: +49(089)857000-0
FAX: +49(089)8573702
TLX: 841-521-5111

Metronik GmbH
Leonhardsweg 2
D-82008 Unterhaching
Germany
Ph: +49(089)61108-0
FAX: +49(089)61108-161

HOLLAND
Alcom Electronics BV
Essebaan 1
2900 AJ Capelle A/D IJSSEL
Holland
Ph: +31(010)4519533
FAX: +31(010)4586482

IRELAND
Memec Ireland Ltd.
Block H
Lock Quay
Clare St.
Limerick, Ireland
Ph: +353(061)411842
FAX: +353(061)411888

ITALY
Newtek Italia S.P.A.
via Tonoli 1
20145 Milano
Italy
Ph: +39(233)105308
FAX: +39(233)103694

ISRAEL
Telsys
Atidim Industrial Park Bldg 3
Dvora Hanevia St., Neve Sharet,
Tel-Aviv 61431, Israel
Ph: +972(03)492001
TLX: 32392 and 371279
FAX: +972(03)497407

NORWAY
NC ScandComp Norway AS
Nils Hansens vei 3
N-0667 Oslo
Norway
Ph: +47(0)22724045
FAX: +47(0)22724059

PORTUGAL
Amitron Arrow Electronica LDA
QTE Grande Lote 20
Alfragide 2700
Amadora
Portugal
Ph: +351(01)4714806
FAX: +351(01)4710802

RUSSIA
PC Center Techno
126 Pervomayskaya St.
Moscow 105203
Russia
Ph: +7(095)4618775
FAX: +7(095)9651020

SPAIN
Amitron Arrow SA
Albasanz, 75
28037 Madrid
Spain
Ph: +34(1)3043040
FAX: +34(1)3272472

SWEDEN
GBTopcomp Electronics
Alstromergatan 22
P.O. Box 12009
10221 Stockholm
Sweden
Ph: +46(086541)080
FAX: +46(086531)251
TLX: 10135

SWITZERLAND
Memotec AG
Gaswerkstrasse 32
P. O. Box
CH-4901 Langenthal
Switzerland
Ph: +41(063)281122
FAX: +41(063)223506
TLX: 845-982550

UNITED KINGDOM
Sequoia Technology Ltd.
Tekelec House
Back Lane
Spencers Wood
Reading, Berks
United Kingdom RG71PD
Ph: +44(0)1734258000
FAX: +44(0)1734258020

FAR EAST

DISTRIBUTORS

AUSTRALIA

ACD (N.S.W.)
Unit 1, 106 Belmore Rd. Nth.
P. O. Box 402
Riverwood, N. S. W. 2210
Australia
Ph: +61(02)534-6200
TLX: AA121398
FAX: +61(02)534-4910

ACD
Unit 2, 17-19 Melrich Rd.
Bayswater, Victoria, 3153
Australia
Ph: +61(03)762-4244
FAX: +61(03)761-1754

ACD
1048 Beaudesert Rd.
Coopers Plains, Queensland, 4108
Australia
Ph: +61(07)875-1113
FAX: +61(07)275-3662

HONG KONG

CET Ltd.
1108-1112 Metroplaza Tower 2
223 Hing Fong Rd., Kwai Fong
N.T., Hong Kong
Ph: (852)2485-3899
FAX: (852)2485-3802

Cirrus Logic International Ltd.
1203 Park Tower
15 Austin Rd., Tsimshatsui
Kowloon, Hong Kong
Ph: (852)2376-0801
FAX: (852)2375-1202

KOREA

Cirrus Logic, Korea Co., Ltd.
Rm 1302 SangKyung Bldg., 824-21
YeokSam-Dong,
KangNam-Ku,
Seoul, Korea
Ph: +82(02)565-8561
FAX: +82(02)565-8565

Hanaro Corp.
Hana Bldg., 122-30 Chungdam-Dong
Gangnam-Ku,
Seoul, Korea 135-100
Youngdong P. O. Box 1588, Seoul
Korea 135-615
Ph: +82(02)516-1144
FAX: +82(02)516-1151
TLX: K26376 HANARO

MALAYSIA

DCP (M) SDN BHD
6th Floor, Wisma Denko
41, Aboo Sitee Lane
10400 Penang
Malaysia
Ph: +6042281860
FAX: +6042281420

NEW ZEALAND

ACD
P.O. Box 24-500
Royal Oak
Auckland, New Zealand
Ph: +64(09)636-5984
FAX: +64(09)636-5985

TAIWAN

Cirrus Logic International Ltd.
Taiwan Branch
10F, No.214 Tun Hwa North Rd.
Taipei,
Taiwan R.O.C.
Ph: +886(02)718-4533
FAX: +886(02)718-4526

Morrihan International Corp.
8F-5 No. 57 Fu-Hsing N. Rd.,
Taipei,
Taiwan R. O. C.
Ph: +886(02)752-2200
FAX: +886(02)741-4690
TLX: 20422 MORRIHAN
Taichung Branch
Ph: +886(04)224-6666
FAX: +886(02)741-4690

SINGAPORE

Dynamar Computer Products, Pte Ltd.
8 Loyang Dr.
Singapore 1750
Ph: +65-542-1878
FAX: +65-542-7188

THAILAND

Dynamar Computer Systems
2991/19 Visuthanee
1st Floor
Ladprao Rd. SOI 101-103
Klongchan, Bangkapi
Bangkok 10220
Thailand
Ph: +662-376-0132
FAX: +662-376-0133

JAPAN

SALES OFFICES

Sales Office and Applications Support:

Cirrus Logic K.K.
Shinjuku Green Tower, Bldg. 26F
6-14-1 Nishi-Shinjuku,
Shinjuku-ku,
Tokyo 160
Japan
Ph: +81(03)3340-9111
FAX: +81(03)3340-9120

DISTRIBUTORS

Internix, Inc.
Shinjuku Hamada Bldg.,
7-4-7 Nishi-Shinjuku,
Shinjuku-ku,
Tokyo 160
Japan
Ph: +81(03)3369-1105
FAX: +81(03)3363-8486

Marubun Corp.
Marubun Daiya Bldg.,
8-1 Nihonbashi Odenmacho,
Chuo-ku,
Tokyo 103
Japan
Ph: +81(03)3639-9873
FAX: +81(03)3639-3727

A Cirrus Logic Company

Crystal Semiconductor Corporation

P.O. Box 17847
Austin, Texas 78760
Tel: (512) 445-7222
(800) 888-5016
FAX: (512) 445-7581

Cirrus Logic, Inc. develops innovative integrated circuits for user interface and multimedia (graphics, audio and video), mass storage, wired and wireless communications, consumer electronics, data acquisition, and telecommunications.