CIRRUS LOGIC®

CL-GD543X Applications and Errata Book

Revision 1.2

April 1994

365439-003

Publication Change Log

Rev. #	Rev. Date	Changes
1.0	2/9/94	Preliminary Release: Includes AA02-AA05, B5, E1, SW Release Notes, and 5434 Errata for Revisions A and B
1.1	3/25/94	Added AA7, AA8, CAA1, CAA2, renamed AA6 as CAA3
1.2	4/4/94	Added TRM Errata, Added AJ Errata , Updated AA8, Updated AF Errata

CL-GD5434 V1.00 Software Release Errata

Notice

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The following errata have been observed in the v1.00 release of CIR.DRV dated Feb 18, 1994.

1• Word for Windows v6.0 Help

If the help option is used with Word for Windows v6.0, and the Help window is moved on the screen, tl screen is corrupted.

2• Video for Windows v1.1

If Video for Windows v.1.1 is used, Windows will hang the system.

3• CC Mail 2.0

Corrupted fonts appear in some menus.

The following enhancements will be implemented in the next release of drivers.

1• VL Configuration on PCI Systems

Some PCI system BIOSs have been observed to incorrectly report the CL-GD5434 as being on the PC bus when it is configured as a VL VGA in a PCI system. To avoid this in the future, the next release CIR.DRV will not request the PCI frame buffer address if the CL-GD5434 is configured as a VL device.

CIRRUS LOGIC, Inc., 3100 West Warren Avenue, Fremont, CA 94538 Telephone 510.623.8300 FAX 510.252-6070

Mya 5, 1994

Dear Customer,

Thank you for your interest in the Cirrus Logic family of graphics products. Enclosed is the CL-GD5434 information you requested. The production revision A for VL Bus solutions and the production revision C for both VL Bus and PCI Bus systems are now available in production volumes.

The current revision of Driver software is version 1.01A dated May 4, 1994; the current BIOS revision is 1.00A dated March 1, 1994. Any updates will be available from the Cirrus Logic Bulletin Board (510-440-9080). Please contact your Cirrus Logic representative if you have any questions.

Thank you again for your interest in Cirrus Logic.

Very truly yours,

Cirrus Logic, Inc.

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GDK5434-B-DM8-1

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GDK5434-B-DM8-1 Bill of Materials

Part No.	Title	Description
GDK5434-BOM1-01	GDK5434-B-DM8-1 Bill of Materials	Document.
GDB5434-B-DM8-1	PCI Bus Demo Board with CL-GD5434 Chip Installed	PCI Bus Board
GDK5434-LTR1-1	Customer Letter	Document,
GDK5434-DM8-LC1	GDK5434-B-DM8-1 Kit License Agreement	Document
	CL-GD5434-HC-C Errata	Document
	Drivers, Release Release 1.01A, May 4, 1994 Dos Display Drivers & Utilities, Driver disk 1 of 4 Windows 3.1 & WIN/OS2, Driver disk 2 of 4 OS/2 2.1, Driver disk 3 of 4 Window NT, Driver disk 4 of 4	4 Diskettes
	OEM Documentation, OEM disk 1 of 1 Release 1.01A, dated May 4, 1994	1 Diskette

Table of Contents

Revision 1.2

Section **Description**

CIRRUS LOGIC

Section 1
Product Bulletin

CL-GD543X

CIRRUS LOGIC®

CL-GD543X

Preliminary Product Bulletin

FEATURES

- **Pin- and software-compatible VGA graphics accelerator family**
- **Enhanced GUI acceleration**
  - — 64-bit Bit Block Transfer (BitBLT) engine (CL-GD5434)
  - — 32-bit BitBLT engine (CL-GD5430)
- **32-bit direct-connect CPU interface**
  - — PCI™ bus (v2.0 compliant) with burst-cycle support
  - — VESA® VL-Bus™ (v2.0 with 50 MHz)
  - — ISA bus (12.5 MHz) (CL-GD5434 only)
  - — Zero-wait-state write buffer for CPUs up to 33 MHz
- **64-bit DRAM display memory interface**
  - — 1-, 2-, and 4-Mbyte display memory support (CL-GD5434)
  - — 1/2-, 1-, and 2-Mbyte display memory support (CL-GD5430)
- **Resolutions to 1280 x 1024**
  - — Up to 1024 x 768 x 64K colors, non-interlaced
  - — Up to 800 x 600 x 16M colors, non-interlaced
  - — Up to 1280 x 1024 x 64K colors, interlaced
- **Integrated 24-bit DAC**
- **'Green PC' power-saving features:**
  - — VESA® support for Display Power-Management Signalling (DPMS)
  - — Internal DAC with power-down mode
  - — Low-frequency DRAM refresh
  - — Static monitor sync signals
- **100% hardware- and BIOS-compatible with IBM® VGA display standard**

(cont.)

VGA GUI Accelerator

CL-GD5434 — 64-bit GUI Accelerator
CL-GD5430 — 32-bit GUI Accelerator

OVERVIEW

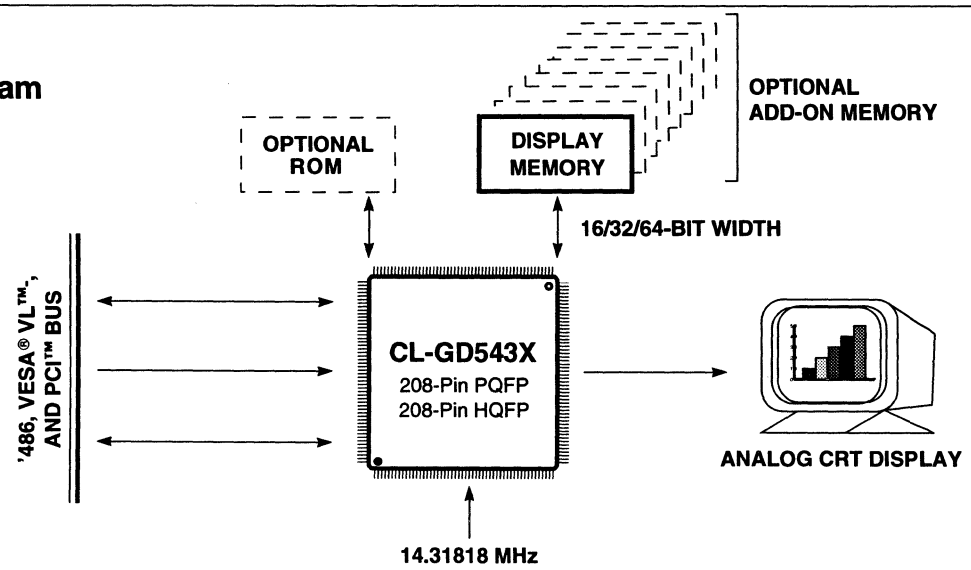
Based on a 64-bit GUI engine, the Alpine Graphics Accelerator Family incorporates a Bit Block Transfer (BitBLT) VGA controller with a 24-bit true-color DAC, dual-clock synthesizer, and direct-connect 32-bit PCI™ and VL-Bus™ interface. Designed to accelerate Microsoft® Windows and Windows NT 3.1, OS/2™ v2.1, and other graphic interfaces, the Alpine family offers performance surpassing current DRAM, and many VRAM-based GUI accelerators.

The software- and pin-compatible Alpine family allows OEMs to meet different price and performance targets with one graphic subsystem design. Built on a 1-Mbyte frame buffer and optimized for PCI and VL-Bus systems, the CL-GD5430 can be quickly upgraded to the higher-performance CL-GD5434. With a 2-Mbyte frame buffer, the CL-GD5434 offers performance beyond current 32-bit standard and interleaved architectures.

By combining a 32-bit external local bus interface with a 64-bit path to the DRAM frame buffer, the Alpine family eliminates the video-memory bottleneck in traditional DRAM architectures, and maximizes system-to-video bandwidth critical for outstanding graphics acceleration.

(cont.)

Functional Block Diagram



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CL-GD543X

Alpine Family VGA GUI Accelerators

FEATURES (cont.)

- **Programmable dual-clock synthesizer**
  - — Pixel clock programmable up to 110 MHz ('GD5434), and up to 86 MHz ('GD5430)
  - — Memory clock programmable up to 50 MHz ('GD5434), and up to 60 MHz ('GD5430)
- **Multimedia-ready**
  - — Video overlay with external video data and 'Color Keying'
  - — Genlock support with external HSYNC and/or VSYNC
  - — Alpha Channel ('GD5434)
  - — VESA® advanced-feature-connector (VAFC) support ('GD5430)
- **64 x 64 hardware cursor**
- **CL-GD5428/'GD5429 register- and software-compatible**
- **Glueless PCI™ bus interface with VGA BIOS ROM support for single 8-bit EPROM**
- **Low-power 5V CMOS, 208-pin PQFP/HQFP package**

OVERVIEW (cont.)

BitBLT support, linear addressing, hardware cursor, color expansion, and memory-mapped I/O are some of the many built-in CL-GD543X features that ensure outstanding GUI performance. The highly integrated 208-pin HQFP package makes the CL-GD543X ideal for both motherboard systems and add-in cards.

The only external support needed is cost-effective DRAM memory and a 14.31818-MHz frequency reference.

Operating at pixel clock rates programmable up to 110 MHz ('GD5434) and 86 MHz ('GD5430), the CL-GD543X chip supports standard and VESA high-resolution extended modes. The internal palette DAC may be configured for the industry-standard VGA modes of 16- or 256-color, or extended to high- and true-color modes of 32K, 64K, or 16.7 million colors. Display resolutions up to 1280 x 1024 are supported.

ADVANTAGES

Unique Features	Benefits
Cost Effectiveness —	
■ Interface to as few as one DRAM, built-in true-color palette DAC and dual-frequency synthesizer	❒ Minimizes chip count, system cost, and board space for cost-effective solution.
■ Interface to x4, x16 DRAMs	❒ Allows design flexibility for use of appropriate type and amount of memory.
High Performance —	
■ Hardware BitBLT for Microsoft® Windows	❒ Accelerates GUIs such as Microsoft® Windows and similar applications.
■ 32-bit PCI™, VESA® VL-Bus™, and local bus interface	❒ Increases system throughput.
■ 64-bit-wide DRAM interface	❒ Eliminates display-memory bottleneck.
■ Independent video and DRAM timing	❒ Optimizes timing for increased performance.
■ Maximizes fast-page mode access to display-memory DRAMs	❒ Improves CPU performance by accessing maximum bandwidth available from DRAM display memory.
■ Host access to DRAMs through advanced write buffers	❒ Provides faster host access for writes to display memory.
■ 32-bit memory-mapped BitBLT control registers	❒ Improves graphics-application performance.
■ 15-, 16-, or 24-bit true-color palette DAC	❒ Provides high-color and true-color display for photo-realistic images. 32K, 64K, or 16.8 million colors on screen at once for life-like images.
Multimedia —	
■ Overlay, color keying, and Genlock	❒ Allows 16-bit-pixel interfacing through the VESA® connector for multimedia applications.
Compatibility —	
■ Compatible with VGA and VESA® standards	❒ Allows compatibility with installed base of systems and software.
■ Drivers supplied at various resolutions for Windows™ 3.1, Windows NT™, AutoCAD®, OS/2™, and other key applications	❒ Provides a 'ready-to-go' solution that minimizes the need for additional driver development.
■ Connects directly to IBM® PS/2™ and multifrequency analog monitors	❒ Drives all PC-industry-standard, high-resolution monitors to ensure compatibility.

CIRRUS LOGIC

SOFTWARE SUPPORT

CL-GD543X VGA Software Drivers

Cirrus Logic provides an extensive — and expanding — range of software drivers to enhance the resolution and performance of many software packages. Note, however, that the CL-GD543X VGA graphics portion of a system *does not* require software drivers to run applications in standard-resolution mode.

Cirrus Logic software drivers for the CL-GD543X include:

Software Drivers	Resolution Supported[a]	No. of Colors
Microsoft® Windows v3.1	640 x 480, 800 x 600, 1024 x 768, 1280 x 1024 640 x 480, 800 x 600, 1024 x 768, 1280 x 1024 640 x 480, 800 x 600, 1024 x 768	256 colors 65,536 colors 16.8 million colors
Microsoft® Windows NT v3.1	640 x 480, 800 x 600, 1024 x 768, 1280 x 1024	16 and 256 colors
OS/2™ V2.1	640 x 480, 800 x 600, 1024 x 768	256 colors
AutoCAD® V11, V12 Autoshade® V2.0 w/ Renderman, 3D Studio V1, V2	640 x 480, 800 x 600, 1024 x 768, 1280 x 1024 640 x 480, 800 x 600, 1024 x 768, 1280 x 1024 640 x 480, 800 x 600, 1024 x 768, 1280 x 1024 640 x 480, 800 x 600, 1024 x 768, 1280 x 1024 640 x 480, 800 x 600, 1024 x 768	16 colors 256 colors 32,768 colors 65,536 colors 16.8 million colors
Lotus® 1-2-3™ v2.X,	132 x 25, 132 x 43 (text) 800 x 600	16 colors 16 colors
Lotus® 1-2-3™ v3.3	800 x 600, 1024 x 768	16 colors
Microsoft® Word v5.X	132 x 25, 132 x 43 (text) 800 x 600, 1024 x 768	16 colors
WordPerfect® v5.1	132 x 25, 132 x 43 (text) 800 x 600, 1024 x 768	16 colors
WordPerfect® v6.0[b]	640 x 480, 800 x 600, 1024 x 768	16 and 256 colors
WordStar® v5.5-7.0	800 x 600, 1024 x 768	16 colors
SCO UNIX™[c]	640 x 480, 800 x 600, 1024 x 768	16 and 256 colors

[a] All resolutions may not run on all monitor types; 640 x 480 drivers will run on PS/2-type monitors. Extended resolutions are dependent upon monitor type and VGA system implementation.

[b] Supported by VESA® driver.

[c] Shipped by Santa Cruz Operations.

BIOS SUPPORT

- **Fully IBM® VGA-compatible BIOS**
- **Relocatable, 32K bytes with VESA® VL-Bus™ and PCI™ Local Bus support**
- **VESA® BIOS Extensions (VBE) support in ROM**
- **Support for Display Power Management Signaling (DPMS) in ROM**
- **VESA® monitor timing-compliant**

UTILITIES

- **Manufacturing test**
- **Windows DOS/NT utilities**
- **Video mode configuration utility — CLMODE**
- **Set resolution in Windows — WINMODE**
- **Configured OEM system integration — OEMSI**

CIRRUS LOGIC

CL-GD543X

Preliminary Product Bulletin

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The Company

Headquartered in Fremont, California, Cirrus Logic, Inc., develops innovative architectures for analog and digital system functions. The Company implements those architectures in proprietary integrated circuits and related software for applications that include user interface and multimedia (graphics, audio, and video), mass storage, communications, and data acquisition.

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355439-003

CIRRUS LOGIC

Section 2
Application Alerts

CL-GD543X

CL-GD543X Application Alert 2
Memory Configurations for CL-GD5430/34

User Interface Group
Cirrus Logic, Inc.

Scope and Applicability

This Application Alert presents information not found in previous documentation for the CL-GD543x. It is intended to be used in conjunction with applicable CL-GD543x literature

Related Documents

– *Alpine VGA Family - CL-GD543x Technical Reference Manual - November 1993*

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Introduction

The purpose of this Application Alert is to summarize the memory configurations for the CL-GD5430/34. It is possible to design a common board that can be populated with 512K (CL-GD5430 only) or up to 4M (CL-GD5434 only).

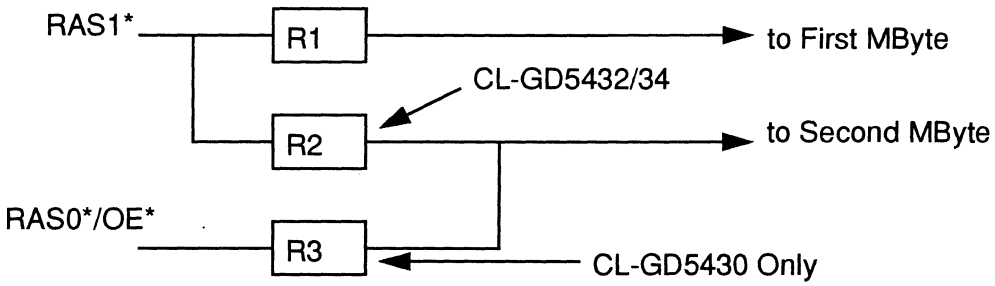
Summary Table

The following table summarizes the various memory configurations defined for the CL-GD5430/34. The column headed "Connection Table" refers to tables in the November 1993 issue of the Alpine TRM.

DRAM Configuration	Number of DRAMs	Total Memory	Connection Table	'30	'34	Ras* Note
256K x 4	4	512 Kbyte	B7-3	✔		
256K x 4	8	1 Mbyte	B7-4	✔	✔	
256k x 4	16	2 Mbyte	B7-5	✔	✔	✔
256k x 16, Dual-CAS*, Symmetric	1	512 Kbyte	B7-6	✔		
256K x 16, Dual-CAS*, Symmetric	2	1 Mbyte	B7-7	✔	✔	
256K x 16, Dual-CAS*, Symmetric	4	2 Mbyte	B7-8	✔	✔	✔
256K x 16, Dual-CAS*, Symmetric	8	4 Mbyte	B7-9		✔	
256K x 16, Dual-WE*, Asymmetric	1	512 Kbyte	B7-10	✔		
256K x 16, Dual-WE*, Asymmetric	2	1 MByte	B7-11	✔	✔	
256K x 16, Dual-WE*, Asymmetric	4	2 MByte	B7-12		✔	

RAS* Connection Note

To ensure the layout can be used with up to 2 MBytes with either the CL-GD5430 or CL-GD5434, the RAS* connections to the 2nd MByte (devices 3 and 4 in Table B7-8) (or devices 9-16 in Table B7-5) should be either RAS1* (CL-GD5434 case) or RAS0*/OE* (CL-GD5430 case). An obvious way to mechanize this is with zero ohm resistors (or damping resistors if they prove necessary) that are optionally populated. See the diagram below.



Notes
R1 is installed for all configurations.
R2 is installed for CL-GD5434 only.
R3 is installed for CL-GD5430 only.

WE* Steering Note

If WE* steering is used, the CL-GD5430 will support up to only 1 MByte of Display Memory since RAS0/OE* is not available to control the 2nd MByte.

CL-GD543X Application Alert 3
Calculated Maximum MCLK for CL-GD5430/34

User Interface Group
Cirrus Logic, Inc.

Scope and Applicability

This Application Alert presents information not found in previous documentation for the CL-GD543x. It is intended to be used in conjunction with applicable CL-GD543x literature

Related Documents

– *Alpine VGA Family - CL-GD543x Technical Reference Manual - November1993*

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Introduction

The purpose of this Application Alert is to document the results of evaluation of the equations described in the CL-GD543X Technical Reference Manual, Appendix B7 (*Memory Configurations and Timing*). The numbers have been compared to 256K x 16 from several vendors. The results of these comparisons are listed in the table below. The devices are ordered alphabetically by vendor. The calculated numbers were rounded to the nearest ns for the purposes of this this comparision.

▼ **Note:** In some cases, the results of the comparison indicates that the memory device supports a Memory Clock (MCLK) greater than 50 Mhz. This is not to be taken as a guarantee that any particular member of the Alpine family is rated to operate with an MCLK greater than 50 MHz.

▼ **Note:** The appearance of any particular device from any vendor is not to be taken as a guarantee that it has been tested with any particular Cirrus Logic device, or as an endorsement from Cirrus Logic.

▼ **Note:** Fast Page Mode cycle time (tPC) and Random Cycle time (tRC) were not considered as limiting parameters since they are calculated, not measured, by the DRAM vendors. The calculations assume very slow signal rise and fall times.

Vendor	Vendor Part Number	Configuration	Speed Grade	Standard RAS Timing		Extended RAS Timing (not CL-GD5434-A)	
				Max MCLK MHz	Limiting Parameter	Max MCLK MHz	Limiting Parameter
Hitachi	HMS14260	Dual CAS	-70	48.3	tRP	55.5	tRAS
Hitachi	HMS14260	Dual CAS	-80	39.4	tRP	48.3	tRAS
Hitachi	HMS41260	Dual CAS	-100	NR	tRP	39.4	tRAS
Hitachi	HMS51470	Dual WE	-70	48.3	tRP	55.5	tRAS
Hitachi	HMS51470	Dual WE	-80	39.4	tRP	48.3	tRAS
Hitachi	HMS51470	Dual WE	-100	NR	tRP	39.4	tRAS
Micron	MT4C16256	Dual WE	-70	48.3	tRP	55.5	tRAS
Micron	MT4C16256	Dual WE	-80	39.4	tRP	48.3	tRAS
Micron	MT4C16256	Dual WE	-100	NR	tRP	39.4	tRAS
Micron	MT4C16257	Dual CAS	-70	48.3	tRP	55.5	tRAS
Micron	MT4C16257	Dual CAS	-80	39.4	tRP	48.3	tRAS
Micron	MT4C16257	Dual CAS	-100	NR	tRP	39.4	tRAS
Mitsubishi	M5M44170A	Dual WE	-60	48.3	tRP	59.1	tRP

Vendor	Vendor Part Number	Configuration	Speed Grade	Standard RAS Timing		Extended RAS Timing (not CL-GD5434-A)	
Mitsubishi	M5M44170A	Dual WE	-70	39.4	tRP	50.1	tRP
Mitsubishi	M5M44170A	Dual WE	-80	NR	tRP	43.0	tRP
Mitsubishi	M5M44170A	Dual WE	-100	NR	tRP	37.6	tRP
Mitsubishi	M5M44260A	Dual CAS	-80	NR	tRP	43.0	tRP
Mitsubishi	M5M44260A	Dual CAS	-100	NR	tRP	37.6	tRP
NEC	uPD42170	Dual WE	-60	48.3	tRP	59.1	tCAC
NEC	uPD42170	Dual WE	-70	48.3	tRP	55.5	tRAS
NEC	uPD42170	Dual WE	-80	39.4	tRP	48.3	tRAS
NEC	uPD424260A	Dual CAS	-60	48.3	tRP	59.1	tCAC
NEC	uPD424260A	Dual CAS	-70	39.4	tRP	50.1	tRP
NEC	uPD424260A	Dual CAS	-80	39.4	tRP	48.3	tRAS
Toshiba	TC51470B	Dual WE	-70	48.3	tRP	55.5	tRAS
Toshiba	TC51470B	Dual WE	-80	39.4	tRP	48.3	tRAS
Toshiba	TC51470B	Dual WE	-100	NR	tRP	39.4	tRAS

Note: "NR" indicates this configuration is not recommended.

CL-GD543X Application Alert 4
Linear Addressing Space for VESA-VL

User Interface Group
Cirrus Logic, Inc.

Scope and Applicability

This Application Alert presents information not found in previous documentation for the CL-GD543x. It is intended to be used in conjunction with applicable CL-GD543x literature

Related Documents

– *Alpine VGA Family - CL-GD543x Technical Reference Manual - June 1993*

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Introduction

The purpose of this Application Alert is to explain how the linear address space is chosen for the Cirrus Logic VESA-VL reference designs. An implementor can choose to copy this method directly, or can use this as an example on which to model a design.

Background

There was never any real problems with memory space address conflicts when using the standard VGA address range at A000:0 - AFFF:F. This stemmed from this range having been assigned on the original IBM PC. Of course, this 64kbyte window is much too small to directly address a large (1-4 Mbyte) display memory and requires a paging mechanism with its attendant overhead.

Linear addressing of display memory avoids the problems associated with this small window by assigning a contiguous address space large enough for all of display memory. However, we have not been so fortunate as to have a well-defined area reserved for this address space. This lack of definition has been exacerbated by designers not decoding the entire address bus, thereby saving pins.

Originally, we placed our linear address space at 128MB. HIMEM was tied to A27 and LOMEM was the decode of A[26:22] all zero. However, the ZEOS platform decoded only to address bit A26, so it can not distinguish between 128MB and 0MB. When our drivers wrote into display memory at 128MB, a write would also take place to location 0. It can be seen that this quickly led to problems.

Next we tried 64MB. HIMEM was tied to A26 and LOMEM was the decode of A[25:22] all zero. However the EFAR platform decodes only up to address bit A25, so they can not distinguish between 64MB and 0MB.

The Current Solution

We are now changing our reference design so that the linear address space can begin at either 64MB or 2048MB. We expect that 64MB will be satisfactory for all platforms other than EFAR and that 2048MB will be satisfactory for them. The choice is made by moving two jumper blocks (or populating two zero ohm resistors). The following table indicates how HIMEM and LOMEM are generated for the two cases. The right-most column indicates how the jumpers in the schematic fragment on the next page are populated.

Please note that only the two choices of 64 MB or 2048 MB are possible with this design. If additional flexibility is required, or if the address space is to be placed at any other location, the design will change.

Address Space	HIMEM	LOMEM	Jumpers
64MB	A26	NOR of A31, A[25:22]	right
2048MB	A31	NOR of A[26:22]	left

Why 2048MB was Selected

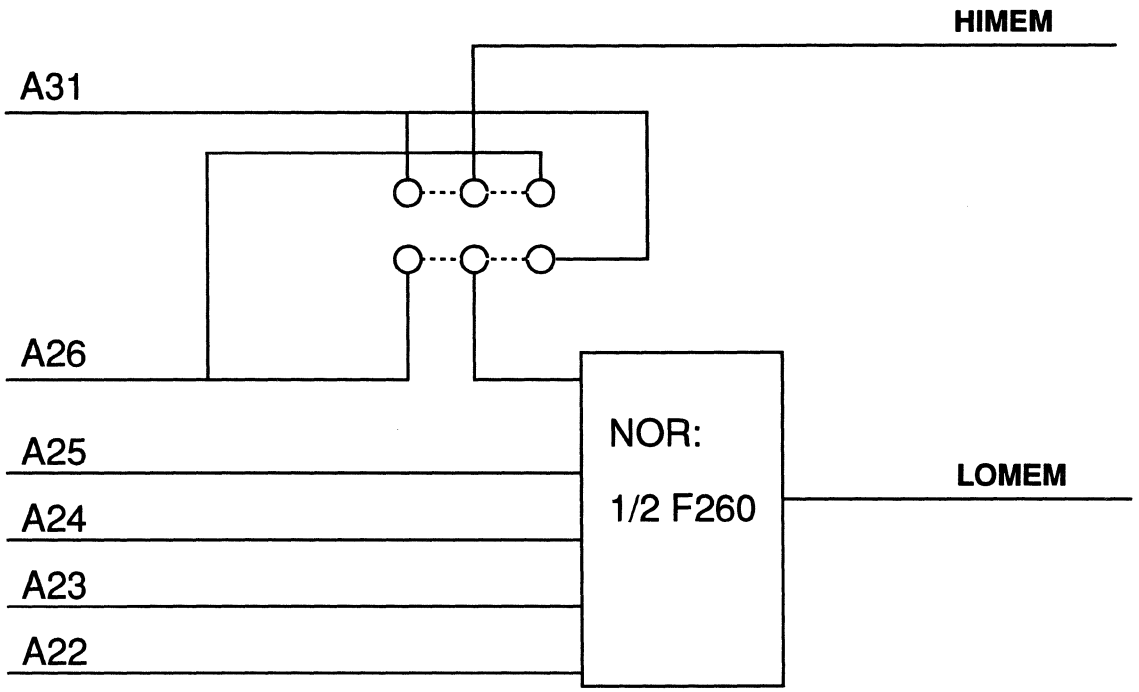
There will soon be motherboards on the market that support both VESA and PCI. We understand that these platforms will allocate memory for PCI devices above 2048MB. This means that we must decode A31 when we are configurated at 64 MB to avoid erroneously responding to accesses intended for PCI devices. Since A31 is decoded in most core logic chip sets, placing the frame buffer at 2048 MB will ensure that the core logic will ignore cycles directed to us.

Software Note

The Windows drivers must know where the linear address space has been placed. This is done with an entry in the SYSTEM.INI file. The entry is Linearaddr = 2048 for the 2048 MB case or Linearaddr = 64 for the 64 MB case. If the address space is moved to some other location, this entry will have to be modified appropriately.

Schematic Fragment

The following schematic fragment shows how this might be implemented. The jumpers are connected as indicated with the dotted lines. The only two cases described in this Ap Alert are both jumpers to the left or both jumpers to the right.



CL-GD543X Application Alert 5
BitBLT Check List for CL-GD5434

User Interface Group
Cirrus Logic, Inc.

Scope and Applicability

This Application Alert presents information not found in previous documentation for the CL-GD543x. It is intended to be used in conjunction with applicable CL-GD543x literature

Related Documents

– *Alpine VGA Family - CL-GD543x Technical Reference Manual - November 1993*

Notice

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Introduction

This application alert is intended for BitBLT programmers who have been working on the CL-GD5426/28 and will be moving on the the CL-GD5434. There are a few differences, mostly resulting from the enhancements available on the '34, that should be taken into consideration. These differences are listed here, in no particular order.

Extension Register GRB

GRB[4] and GRB[1] must be programmed to '0' when executing Screen to Screen BLTs. This is a new restriction. Applications that alternate between Extended Write Modes 4 and 5 and Screen to Screen BLTs will need to pay particular attention to this item.

Mixed I/O

The CL-GD5434 has the capability of accessing the BLT control registers as memory. This speeds the register loading since 4 bytes of data can be transferred per access rather than one. This capability is called Memory Mapped I/O and is described in some detail in the Technical Reference Manual. In general, Memory Mapped I/O should not be mixed with "normal" I/O. An appication should choose one or the other and stick with it.

Pitch Register LSBs

The two LSBs of both pitch registers should be programmed to '0's. This restriction was not previously present.

Delay Prior to Reading Status

If a BitBLT is started while the write buffer is completely filled, the Status register will not report "busy" immediately. Placing the operations that program the BLT registers after any memory writes will insert enough time to guarantee valid status immediately after the BLT is started.

Transparency uses ALL Color Registers

The concept of Color Expand with Transparent is completely re-defined on the CL-GD5434. It is much more nearly analogous to Extended Write Mode 4. This is described in some detail in the TRM. Please observe that the application must load all eight color registers: (GR0,1,10,11,12,13,14,15), even for 8- and 16-bit pixels.

Screen-to-Screen with Color Expand

The source for Screen-to-screen with Color Expand must be on a DWORD boundary. The two LSBs must be '0's.

CL-GD543X Application Alert 7
PCI Configuration Registers 32 Bits Only

User Interface Group
Cirrus Logic, Inc.

Scope and Applicability

This Application Alert presents information not found in previous documentation for the CL-GD543x. It is intended to be used in conjunction with applicable CL-GD543x literature

Related Documents

– *Alpine VGA Family - CL-GD543x Technical Reference Manual - November 1993*

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Introduction

The following issue affects Alpine only when configured for PCI Bus.

Recently a problem was discovered with Microsoft Windows 3.11 EMM386 relating to DWORD I/O cycles. When EMM386 is running it will trap DWORD I/O cycles and will occasionally hang. To work around this, Phoenix, Award, and System Soft BIOS vendors modified their Int 1A routines to never use DWORD I/O.

This uncovered a previously unknown problem in some members of our Alpine family of VGA controllers. If a PCI configuration register is written with a BYTE or WORD I/O cycle, the portion of the register which is not written is cleared to zeroes. The registers effected in this manner are listed in the following table.

List of Registers

Address	Name
04	PCI Command/Status Register
10	PCI Base Address Register
30	PCI Expansion ROM Base Address Register

This applies to the following Cirrus Logic Devices:

List Of Devices

Device
CL-GD5430-1MB-Q-X
CL-GD5434-HC-B

This has been corrected in silicon for the CL-GD5430-1MB-Q-Y and the CL-GD5434-HC-C.

Solution

We have requested that Phoenix, Award, and System Soft modify their POST routine to avoid this problem. We have also contacted AMI and confirmed that there is no problem with their BIOS. We are recommending the following changes.

- When initializing the VGA BIOS Base Address register, a DWORD write to 30h should be used. Once the ROM has been transferred and shadowed, access is disabled using bit 0 of 30h (with a DWORD write).
- The PCI Base Address Register at 10h specifies the Display Memory Base Address. This should always be written as a DWORD.
- The PCI Status register is at offset 6 in the PCI configuration space. The POST routine should check this register for error bits and not clear it if no error bits are set. Since no member of the Alpine family will ever set any error bits, the write to 06h will never be necessary.

CL-GD543X Application Alert 8

PCI Non-Contiguous Byte Writes on CL-GD5434 and CL-GD5430-1MB

User Interface Group
Cirrus Logic, Inc.

Scope and Applicability

This Application Alert presents information not found in previous documentation for the CL-GD543x. It is intended to be used in conjunction with applicable CL-GD543x literature

Related Documents

– *Alpine VGA Family - CL-GD543x Technical Reference Manual - November 1993*

Notice

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Revision History

This is the second version of this document. We have added the 5430-1MB to the list of Cirrus chips which exhibit the problem. A brief description of this item appears in the errata for each chip on which it occurs.

Introduction

The PCI bus has the capability of writing multiple bytes that are not contiguous. For example, a write of byte 0 and byte 2, but not byte 1 can occur. When the CL-GD5434 is the target of such a write, it will fail.

Expansion

Byte merging is where the PCI chipset takes multiple byte writes from the CPU and merges them into one write on a 32-bit boundary. When this occurs, the bytes to be written may not be contiguous (for example, BE1 and BE3 may be active while BE0 and BE2 are not). The Intel **Saturn (82420)** and **Mercury I (82430)** chipsets do not support byte merge. Newer chips set from Intel, currently not in volume production, will support byte merge.

This was first observed when loading Windows NT. The CPU was writing odd bytes to B800, B802, etc. The chipset merged these writes into DWORD operations with non-contiguous bytes. On the third such operation, the CL-GD5434 failed to assert TRDY, hanging the system.

This problem occurs only during planar mode writes; it will not occur in packed-pixel modes. The cause of the problem is well understood.

This problem occurs with the CL-GD5434-HC-AF (production B), the CL-GD5434-HC-AJ (production C), the CL-GD5430-1MB-Q-X, and the CL-GD5430-1MB-Q-Y. This problem will not occur in the CL-GD5430-QC-A.

Solution

The exposure to this item is minimal at this time because there are very few platforms available today based on chip sets which support byte merging. No chip set available from any vendor other than Intel supports byte merging. We have asked the system BIOS vendors to disable the feature for any chip sets which do support it, or at least to make provisions in the CMOS setup to disable it. All BIOS vendors have responded positively to this request.

This will be fixed in a future revision of the CL-GD5434.

CL-GD54XX Combined Application Alert 1
Colored Borders

User Interface Group
Cirrus Logic, Inc.

Scope and Applicability

This Application Alert presents information not found in previous documentation for the CL-GD54XX. It is intended to be used in conjunction with applicable CL-GD54XX literature

Related Documents

- *Alpine VGA Family - CL-GD543x Technical Reference Manual - November 1993*
- *True Color VGA Family- CL-GD542X Technical Reference Manual - January 1994*

Notice

This document describes a potential application of Cirrus Logic integrated circuits. No warranty is given for the suitability of the circuitry or program code described herein for any purpose other than demonstrating functional operation. Cirrus Logic believes this information is accurate and reliable. However, it is subject to change without notice. No responsibility is assumed by Cirrus Logic for the use of this information, nor for infringements of patents or other rights of third parties. This document implies no license under patents or copyrights.

Revision History

This is the initial release of this document.

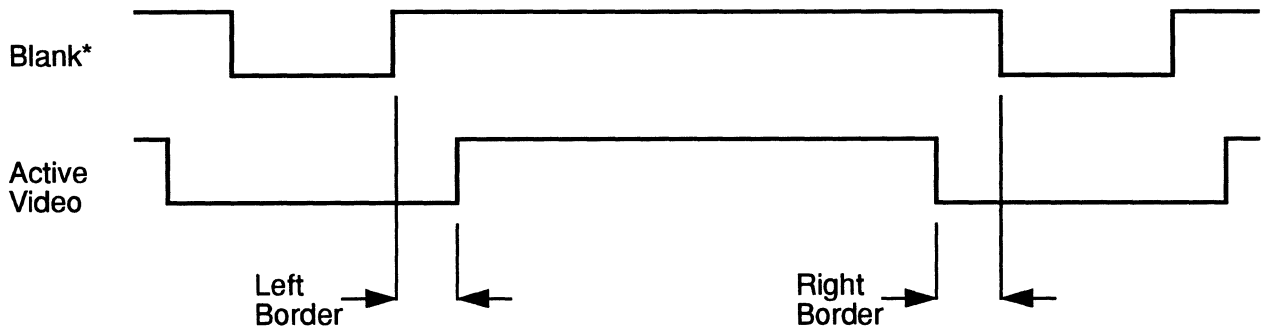
Introduction

It is possible to program the members of the CL-GD542X and CL-GD543X families for a border around the active portion of the screen in standard and extended video modes. The display of such a border is popular in Europe but less so in North America. This is also referred to as overscan.

In the standard VGA the border color is taken from the palette entry which is pointed to by AR11. The Cirrus Logic controllers provide an alternative location for the border color that is protected from normal palette accesses and which does not use a standard palette entry.

Exposition

The following diagram shows the timing for the horizontal sweep. There is a period on the left edge of the



screen after Blank has gone inactive but before the Active Video begins. If the video presented during this period is black, then it is not distinguishable from Blank. If the video is some other color then a colored bar will appear on the left edge of the screen. Similarly, it the right border is programmed a color other than black, a bar will appear on the right edge of the screen.

When this has been extended to the top and bottom, a border will appear completely around the active video. In European standards, this border is large enough to fill the screen to the bezel.

The Cirrus Logic CL-GD542X and CL-GD543X controller chips provide an extended entry in the Palette to contain the color for this border. This entry is referred to as entry 258. It can be accessed at palette entry 02 when SR12[1] is programmed to a '1'. Once the entry is programmed to the desired color, SR12[1] should be programmed to a '0' to enable access to the normal palette entries and SR12[7] should be programmed to a '1' to enable the extended entry for the border.

Extended Video Modes

The VESA specifications for extended video modes specify zero border timing. However, the Cirrus Logic BIOSs program a small border and then suppress it by programming CR1B[5] to a one. The border can be enabled by programming CR1B[5] to a '0'.The border programmed by the BIOS is not guaranteed to

be any particular size (and is certainly not suitable for the European overscan) and will therefore have to be modified by the OEM.

Program

The following program shows how to program the extra palette entry and how to program CR1B[5]. It is written in C++.

```
#include <dos.h>
#include <stdio.h>
#include <stdlib.h>
main(int argc, char **argv)
{
unsigned char red,green,blue;
unsigned int temp, crreg;
setcbrk(1);
if (argc < 4)
          {
          printf ("BORDER.EXE, an overscan programming tool \n");
          printf ("Ver 1.00 3/14/94 YBK/tc \n");
          printf ("Usage: BORDER red green blue \n");
          printf ("red = 0..63 \n");
          printf ("green = 0..63 \n");
          printf ("blue = 0..63 \n");
          exit(1);
          }

red = atoi(argv[1]);
green = atoi(argv[2]);
blue = atoi(argv[3]);


crreg = 0x3b4;                    //assume monochrome mode
temp = inportb(0x3cc);            //read the MISC register
if (temp & 1) crreg= 0x3d4;       //color case

outportb(0x3c4,0x12);             //point to SR12
temp = inportb(0x3c5);
outportb(0x3c5,temp | 2);         /set SR12[1] to enable access to
                                  //to DAC extended entries
outportb(0x3c8,2);                //RAMDAC address 2
outportb(0x3c9,red);              //set color bytes
outportb(0x3c9,green);
outportb(0x3c9,blue);
outportb(0x3c5, temp | 0x80);     //enable overlay

outportb(crreg,0x1b);             //point to cr1b
temp = inportb(crreg + 1);
outportb(crreg+1, temp & 0xdf);   //clear cr1b[5]
}
```

1 Introduction

The Cirrus Logic families of VGA controllers (CL-GD542X, CL-GD543X, and CL-GD545X) comprise highly integrated, mixed signal circuits with high operating frequencies. These chips are designed into video subsystems with very high bandwidth busses. Boards based on these controllers will provide a reliable, compact circuit if designed with care.

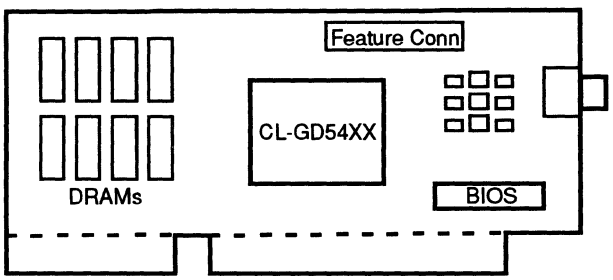
This note distills the experiences gathered by Cirrus Logic in the course of completing our reference designs and in the course of helping our customers solve their problems into a single document.

2 Parts Placement and Adapter Card Considerations

The first consideration is component placement. This section covers the placement of the Cirrus Logic chip. In addition, specific considerations for various Adapter Cards are covered. Subsequent sections will cover how to place the passive devices around the main chip.

2.1 ISA Bus Adapter Card

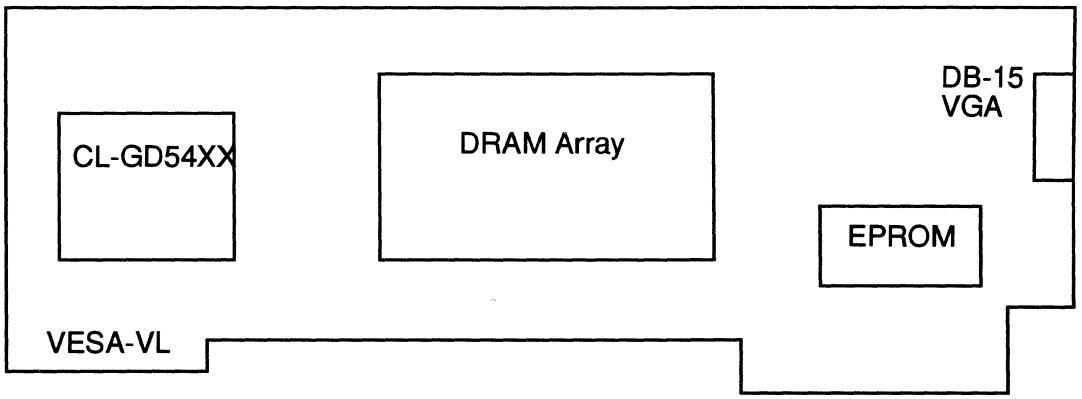
The general parts placement for an ISA adapter should follow the diagram below. The Cirrus Logic chip is positioned close to the ISA interface and relatively close to the VGA feature connector.



The following considerations apply to adapter boards for ISA bus. RESET and IOCHRDY should be isolated from the system data and system address bus lines to avoid coupling noise into them. This can be done by placing them on the other side of a multi-layer board, or by using ground lines as shields. The layout should provide for RC filters for RESET, IOR*, IOW*, MEMR*, and MEMW*. Generally, they will not be required but it is better to make provisions that are unnecessary than the converse. These filters should be close to the Cirrus Logic chip. Finally, it may be necessary to provide termination resistors for SD[7:0]. These should be Thevinin equivalents with 330 ohms to VCC and 470 ohms to ground. A single 10-pin SIP contains the eight terminators required for the eight data lines.

2.2 VESA-VL Bus Adapter Card

Due to the three inch trace maximum imposed by the VESA-VL specification, there is no choice as to where to position the Cirrus Logic controller on a VESA-VL adapter card. It will have to be very near the VESA connector, even though this means placing it far from the DB15 VGA connector. This is shown in the diagram which follows.



The following considerations apply to adapter boards for VESA-VL and PCI bus. The CLK signal is critical and special care should be given to its routing. It should be as short as possible and dressed away from other signals that are apt to induce noise. LDEV# is also critical; it should be routed next.

The RGB traces must be designed to have a characteristic impedance of 75 ohms with no vias or sharp turns. They should be isolated from the DRAM array, either by being routed around the array or on the other side of the board from the traces going to the array.

For information regarding VESA, please contact:

VESA

2150 North First Street, Suite 440

San Jose, CA, 95131-2029

(408) 435-0333

FAX: (408) 435-8225

CL-GD54XX Combined Application Alert 2
Layout Guidelines

User Interface Group
Cirrus Logic, Inc.

Scope and Applicability

This Application Alert presents information not found in previous documentation for the CL-GD54XX. It is intended to be used in conjunction with applicable CL-GD54XX literature

Related Documents

– *Alpine VGA Family Technical Reference Manual- Nov 93*
– *True Color VGA Family Technical Reference Manual - Jan 94*

Notice

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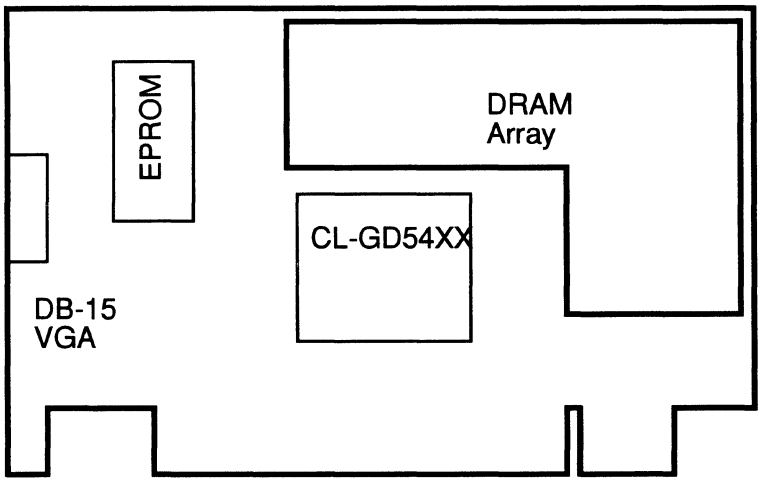
2.3 PCI Bus Adapter Card

The requirements of the PCI specification leave little latitude in the placement of the Cirrus Logic chip. The reference design places the chip near the center of the board with the DRAM array in the upper right portion. The PCI board is much smaller that the VESA-VL board, allowing the chip to be placed in close proximity. This is shown in the diagram which follows.



Questions regarding the PCI specification or membership in the PCI Special Interest Group may be forwarded to:

PCI Special Interest Group

M/S HF3-15A

5200 N.E. Elam Young Parkway

Hillsboro, OR, 97124-6497

(503) 696-2000

2.4 Motherboard

Parts placement is as important in a motherboard design as in any adapter card. The Cirrus Logic controller should simultaneously be close to the CPU and the Core Logic, its DRAM array, and the VGA DB15 connector. At the same time, it should be well away from components on the motherboard which could induce noise, such as the main memory, keyboard controller and other peripherals, and the adapter slots.

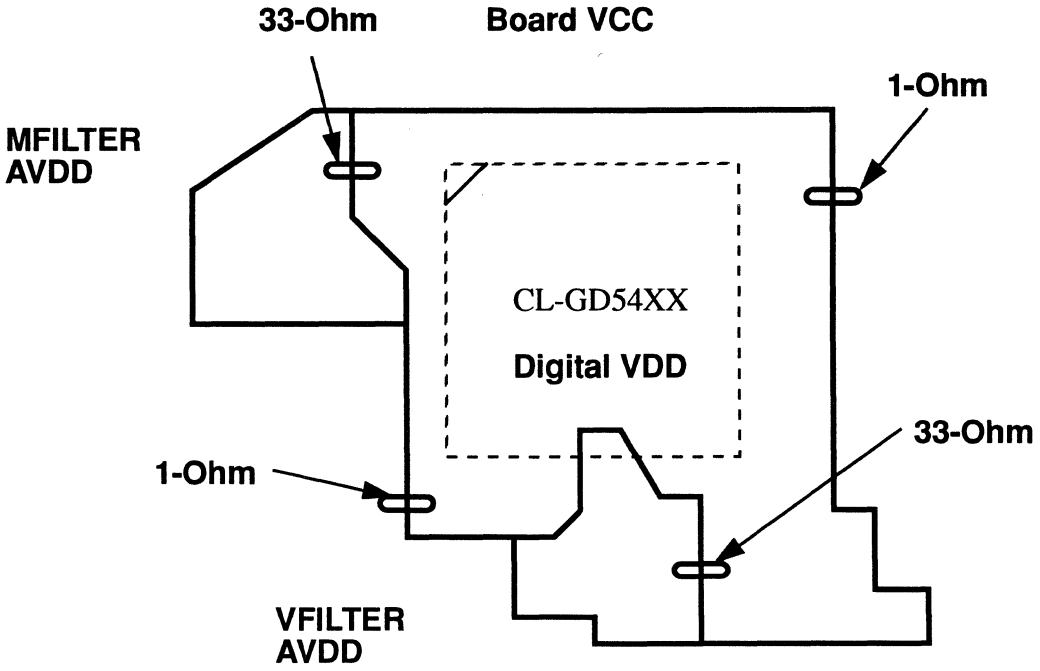
3 Power

Cirrus Logic recommends the use of multi-layer boards for its components, especially when designed into high performance systems. As frequencies continue to get higher, it becomes less and less likely that one can obtain acceptable results with a two-layer board. One plane should be dedicated exclusively to the distribution of power and one plane should be dedicated exclusively to ground.

There should be cuts in the power plane to completely isolate the three power rails distributed to the Cirrus Logic chip from the VCC on the board and from each other. The diagram which follows shows how the cuts are made on a typical board.

It can be seen in the diagram which follows- and in the schematics for the Cirrus Logic Reference designs - that a 1/2 ohm resistor is placed in series between the board VCC and the digital VDD pins of the Cirrus Logic chip (the 1/2 ohm resistor is actually mechanized as two 1 ohm resistors in parallel with each other). This resistor serves as part of an RC filter to isolate the Cirrus chip from noise on the VCC rail, and to provide additional latch-up protection.

Two areas of the power plane must be further isolated. One of these is for AVDD1 (VCLK synthesizer) and one is for AVDD4 (MCLK synthesizer). As shown in the reference designs, these areas are individually further isolated with 33 ohm series resistors that serve as RC filter components.



4 Ground

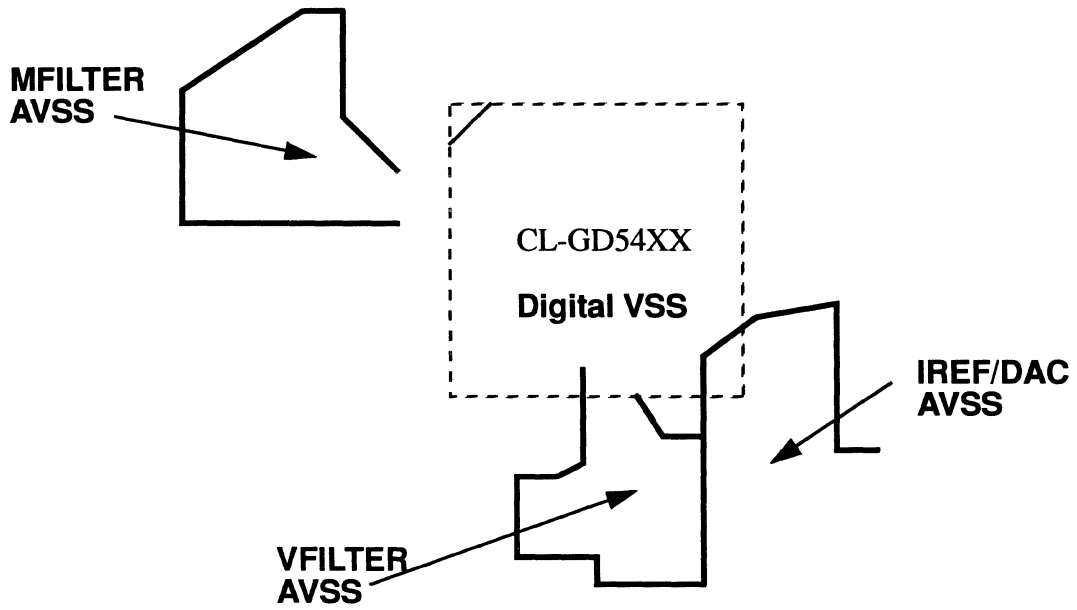
One plane on the board must be dedicated to ground. The ground should have cuts that suppress currents between the various areas (but that do not provide complete isolation). These cuts are shown in the following diagram for a typical reference design.

There is a certain amount of art involved in the exact positioning and size of the cuts in the ground plane and the power plane. Some experimentation may be required to obtain satisfactory results.

The power plane and ground plane cuts should follow each other. It is critical that an isolated ground or power plane not overlay a noisy digital power or ground plane. If such an overlay were to be allowed, the result would be a capacitor composed of the overlay conductors separated by the relatively thin dielectric between the two pieces of epoxy that make up a four-layer board. Noisy busses (such as data or address) should not be allowed to cross any isolated area.

The ground cuts should not interfere in any way with the return currents between the controller and the DRAM array. Any ground differential between the controller and the DRAM array will directly subtract from the TTL margins.

Cirrus Logic can provide reference designs of adapter cards for various chips which yield satisfactory results and pass FCC Class B emission tests.



Designers with prior experience using discrete RAMDACs and clock sources may have found that such care with power distribution and isolation was not necessary, especially at relatively low frequencies. The integrated solution available from Cirrus Logic, operating at high frequencies, has changed this, making these precautions necessary.

5 Decoupling Capacitors

The Cirrus Logic chips operate at high frequencies (over 100 MHz in some cases). Adequate power decoupling is absolutely crucial to a successful design. Each power pin on the chip should have a 0.1 uF capacitor returned to the local ground. These capacitors should be placed as closely to the respective power pins as possible. These capacitors must have excellent high frequency characteristics; Cirrus Logic has found the surface mount ceramic chip capacitors perform adequately.

The high frequency capacitors for AVDD must be on the power pin side of the respective 33 ohm resistors, should be as close to the power pin as possible, and must be returned to the appropriate local ground.

The board design must include adequate bulk bypassing; typically Tantalum capacitors will serve this function. The high frequency characteristics of the bulk bypass capacitors is not as critical as that of the high frequency caps.

6 Synthesizer Filters

The two synthesizer filter pins, MFILTER and VFILTER, must each be connected to a PI RC filter as shown in the reference schematic designs. The filter components, especially the input capacitor and the resistor, must be located as closely to the respective filter pins as possible. The capacitors must be returned to the appropriate AVSS. The traces to the filter pins should be wide (25 mils).

7 IREF Circuitry

The current reference to the DAC (IREF) should be generated using the LM334 circuit shown in the reference designs. The components should be returned to DAC/IREF section of ground plane shown in the previous diagram. A capacitor on the order of 0.1 uF between IREF and AVDD may be necessary to suppress noise in some layouts. Provisions should be made for such a capacitor. During system evaluation the decision can be made as to whether to use the capacitor, and if so, its exact value.

8 RGB Lines

The RGB traces are likely to be fairly long, especially on a VESA-VL adapter card. The rise and fall times on these traces are going to be on the order of 2-4 ns, causing them to behave as transmission lines. This means that the characteristic impedance must be controlled and should be close to the nominal monitor termination value of 75 ohms.

There must be PI LC filters on each of the RGB lines, as shown in the reference designs. The recommended component values are 10 pF for the capacitors. The inductor is a ferrite bead, with 10-20 ohms impedance at 100 MHz.

There is a trade-off involved in the selection of these component values. Obtaining crisp video on the screen requires that the rise and fall times be as short as possible. However, to obtain acceptable emissions testing results, one would like relatively slow rise and fall times. As the pixel rates get higher and higher, there will be less and less margin between these two conflicting requirements. The component values recommended above represent our recommendation as of the time of this writing. The filter components must be placed as closely to the VGA DB15 connector as possible.

A 75 ohm resistor to AVSS is specified for each of the RGB lines. These resistors should be placed as closely to the Cirrus Logic chip as possible.

9 DRAM Array

The DRAMs in Display Memory typically operate as fast as or faster than those in the system memory. The layout of this array should be given as much consideration as that of the system memory. The following general rules apply.

The devices should be placed close to the Cirrus Logic controller. In addition, they should be organized so that each individual device is close to the respective MD pins on the controller. The pin-outs on the controller were carefully optimized to allow this.

The control lines should be treated as the fast, heavily loaded lines they are. Relatively wide traces should be used (8 to 10 mils is typical) and they should be adequately spaced. Placing the traces on 25 mil centers would be ideal. Insofar as it is possible, long parallel runs should be avoided.

Provisions should be made for damping resistors to minimize noise in the array. The damping resistors should be placed at the controller end of the lines.

10 DCLK Line to Feature Connector

Provisions should be made to insert a resistor or inductor in the DCLK line to the Feature Connector. This may prove to be very useful in emissions testing.

CL-GD54XX Combined Application Alert 3
Designing for VESA Display Data Channel (DDC1)

User Interface Group
Cirrus Logic, Inc.

Scope and Applicability

This Application Alert presents information not found in previous documentation for the CL-GD543x. It is intended to be used in conjunction with applicable CL-GD543x literature

Related Documents

– *Alpine VGA Family - CL-GD543x Technical Reference Manual - November 1993*

Notice

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Revision History

This corrects Version 1.0 of this document, which incorrectly stated that ID3 is used for level 1 DDC, and Version 1.1 which incorrectly stated that ID2 is used.

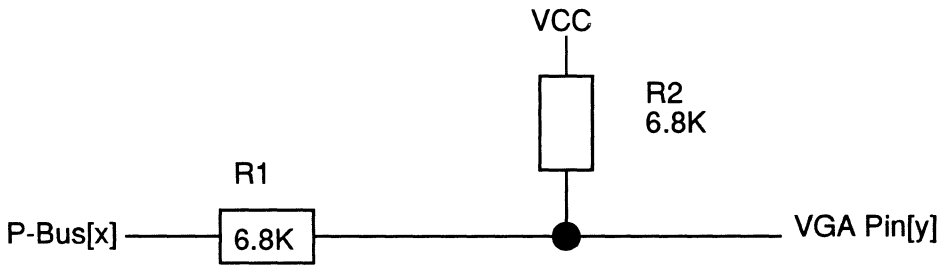
Introduction

The VESA Display Data Channel (DDC) Proposal defines a communication channel between a computer display and the host system. The channel may be used to carry configuration information for optimum use of the display as well as carry additional display control information.

This application alert shows how Cirrus Logic recommends that its CL-GD542X and CL-GD543X chips be configured to support DDC level 1.

Hardware

Since late 1993, all Cirrus Logic reference designs have included (passive) components that allow software to sense TTL levels on the monitor ID pins 15-pin VGA connector. The following diagram indicates how this is mechanized for a typical pin.



If the pin on the VGA connector is open or is being driven to a TTL HIGH, a soft high will appear on the P-Bus pin. If the pin on the VGA connector is grounded or is being driven to a TTL LOW, a soft low will appear on the P-Bus pin. If the overlay control field in CR1A[3:2] is programmed to any value other than 0,0 the P-Bus pins will be inputs and their levels can be sensed in the STAT register (3DA or 3BA). The following table shows how the pins are allocated and how they are sensed.

Mon ID Bit	VGA Pin	P-Bus	Program AR12[5:4] to	Sense on STAT[x]
0	11	P0	00	4
1	12	P1	10	4
2	4	P2	00	5
3	15	P3	10	5

For DDC1, only Mon ID1 needs to be connected. Connecting bits 0 and 2 will allow the implementation to support the old method of monitor ID sensing.

Software Note

For DDC1, the only Monitor ID bit that needs to be sensed is ID1. The following psuedo-code fragment shows how to sense ID1. It may be possible to move the save and restore code to the outside of a loop that recovers the entire byte or string from ID1.

```
read, save AR12
read, save CR1A
AR12[5:4] = 10          ;will read the data on P[1]
CR1A[3:2]= 10           ;set to switch with EVIDEO (EVIDEO remains input)
P1_Val = STAT[4]        ;read stat register; keep bit 4
restore CR1A
restore AR12
```

CIRRUS LOGIC

Section 3
Application Notes

CL-GD543X

Appendix B5

CL-GD5430 Differences

1. Introduction

The purpose of the Appendix is to summarize how the CL-GD5430 is different from the CL-GD5434. This is written for someone who is familiar with the '34 and simply wishes to understand how the '30 differs.

2. Several Video modes/Frequencies not supported

The 5430 supports only 2 MBytes of display memory, and effectively has only a 32-bit memory interface. This restricts the memory modes/refresh frequencies that are supported. See Appendix E1. See App Alert 2 to see how to connect the RAS lines for a compatible 5430/34 board.

3. 5430 does not support 32-bit-pixel modes.

SR7[3:1] must not be programmed to 100. GR30[5:4] must not be programmed to 11. Registers GR12-GR15 do not exist on the 5430.

4. 5430 does not support ISA bus

The CL-GD5430 is a local bus device.

5. Extension Registers Always Enabled

SR6 returns the values 12h or 0fh, depending on the value last written to it. The extension registers are always enabled.

6. SRF[7]

Bank switching is always enabled on the 5430. RAS1* connects to the first MB, RAS* connects to the 2nd MB.

7. CRT FIFO Depth Control: SRF[5]

Programming this bit to a '1' sets the FIFO depth to 20 rather than 32.

8. MCLK

Since we are quoting a maximum MCLK of 60 MHz, the maximum value SR1F[5:0] can be programmed to will increase from 1Ch to 22h. This is certainly subject to our evaluation of the silicon.

9. SR17[7]

The 5430 does not support this bit (Disable DRAM Refresh).

10. Power Management Features

GRE[3] selects Static Clock Mode. MCLK and VCLK are gated off; the chip dissipates only static power. The RAMDAC is powered off. DRAM refresh continues. I/O reads and writes may take place except to the palette. Memory reads and writes and I/O reads and writes to the palette will not hang the system, but will not *product* deterministic results.

Appendix B21 describes Power Management in detail.

11. BLT Destination/Source Start Registers

The 5430 supports only 2 MB. GR2A[5], GR2E[5] are not used.

12. BLT Destination Write Mask: GR2F[2:0]

If this field is programmed to any value other than '0', then n pixels will not be written on the left edge of each scanline for a color-expanded BLT. This is described in detail in Appendix D8.

13. Vertical Preset for Color-Expanded BLT

The three low-order bits of the source address chose the scan line of source data to be used for the first (or only) scanline. This makes it possible to force vertical alignment of the pattern. The source must be aligned.

14. BLT Transparency

For Color Expand with Transparency, the CL-GD5430 does not require that the background color registers be loaded. Also GR11 need not be programmed for 8 bit-per-pixel color expand with transparency.

15. Memory-mapped I/O at Selectable Locations

SR17[6] selects the address space for memory-mapped I/O

16. Overlay/DAC Mode Switching Controls

The internal OVRW* can be chosen for the SWITCH signal without being fed back as EVIDEO*. Refer to CR1D[6]

Choosing EVIDEO* ANDed with OVRW* (CR1A[3:2] = 1,0) functions as originally intended.

Color Key Compare type is always identity (no arithmetic compares) CR1D[5:4]

See Appendix B14 for a complete description of Overlay functions.

17. VAFC Baseline Input

Bit 5 of the Hidden DAC Register is redefined to support VESA VAFC baseline input. It controls Pixel Doubling in 16 bit/pixel display modes.

The VCLK VCO is available on the MCLK pin.

18. Chip ID Updated

The device ID in CR27[7:2] and PCI[0] is changed as indicated in the following table:

Table 1: Device ID

Product	ID
CL-GD5430	101000
CL-GD5434	101010

19. Configuration options changes:

5430 supports MCLK pin source (VCLK VCO on MCLK)

5430 does not support "Disable Internal DAC"

20. CR1C Removed

GENLOCK and Sync Adjust are not present on the 5430

It is actually unknown at this time whether we will have Genlock on the '30.

21. Hidden DAC Register Mode 01xx1010

The palette clock doubling mode is not supported on the 5430.

22. PCI Relocatable I/O

The 5430 supports relocated I/O addresses for PCI only.

Appendix E1

VGA BIOS

External Function Specification

VGA BIOS EXTERNAL FUNCTION SPECIFICATION

1. INTRODUCTION

This document provides a specification for the external software interface of the Cirrus Logic VGA BIOS (Basic Input/Output System).

The Cirrus Logic VGA BIOS is fully compatible with the standard IBM® VGA BIOS and the Interrupt 10h video service functions. This document does not describe the standard Interrupt 10h functions. These functions are described in detail in various other public documents (see the Bibliography in Appendix F1).

All interface extensions to the standard VGA BIOS are fully described in this document.

1.1 Main Features

The Cirrus Logic BIOS is a high-performance firmware product designed to take maximum advantage of the Cirrus Logic VGA controller, especially in the areas of display quality, power management and video performance. The following are some of the major features of the product:

- 100% IBM® VGA-compatible BIOS
- High performance operation
- Modular, proven design
- Adapter or system board implementation (or C000/E000 segments)
- Can be integrated with system BIOS
- Supports switchless configuration
- Can be customized without source code
- VESA®-compatible modes
- VESA®-compatible INT 10h interface

1.2 Enhancements and Revisions since Previous Release

This section describes product enhancements and revisions which resulted in software specification changes since the previous product release.

CL-GD543X BIOS	Enhancement/Revision Description
Version 1.00	Initial Release

1.3 Implementation Type

The Cirrus Logic VGA controller and BIOS can be implemented as an adapter board or placed directly on the motherboard. The following two sections describe specific information

relating to implementation type.

1.3.1 Adapter Implementation

When the video subsystem is implemented as an optional video adapter, the video BIOS will reside at segment C000h for a length of 32K bytes.

The video subsystem is initialized in the standard method. The BIOS will begin with 55h, AAh, and a length indicator. The indicated length will check-sum to a '0', modulo 256. The planar BIOS will make a far call to C000:3 to initialize the video subsystem at power-up.

1.3.2 Planar Implementation

When the video subsystem is implemented as an integral part of the system, the BIOS will reside at segment E000h. The planar BIOS must make a far call to E000:3 to initialize the video subsystem at power-up. This initialization must occur, and must occur prior to initializing any adapter video BIOS. Initialization of optional video adapter ROM BIOS at C000h will be done in the standard manner.

In order for the video subsystem to coexist with an adapter video subsystem, the planar system BIOS must provide CGA and MDA support (INT 42 services). The system BIOS must handle all requirements of CGA and MGA adapters.

For the video subsystem to operate in some environments, a direct BIOS entry is provided to call some BIOS functions without using the interrupt vector table or BIOS data areas in low memory. At offset E000:0034h or C000:0034h is a data word that contains the offset of the VGA BIOS entry point. This word points to the instruction immediately following the CLI clear interrupt instruction. The BIOS preserves the state of the interrupt flag internally, so if interrupts are disabled upon entry through this point, they will remain disabled throughout execution of the BIOS. Note that only certain BIOS functions, such as the save/restore state, should be used unless the interrupt table and BIOS data area are correctly initialized.

1.4 Configuration

1.4.1 INT 15 Support

The system BIOS should implement INT 15h AX=448EH. This is a signal that the video BIOS is ready to accept INT 10 option calls. When this interrupt is received, the system BIOS should perform any option selection required via INT 10h Function 12h, as described in this document. Note that the video BIOS invokes this INT 15 call immediately prior to the initial mode set and displaying the sign-on message.

The INT 15 function call from CLMODE is re-defined as follows:

Input:	AX=	448fhh	
	DL=	bits 7:5	1024 x 768 frequency
		bits 4:2	800 x 600 frequency
		bits 1:0	OEM specific data
	DH=	bits 7:4	Max Resolution
		bits 3:1	1280 x 1024 frequency
		bit 0	640 x 480 frequency

1.4.2 Scratch Pad Definitions:

Cirrus Logic will no longer be publishing the definitions of the Scratch Pad registers since doing so makes modificiation difficult. The information contained in the Scratch Pad regis-

ters can be set or modified using the following BIOS calls.

Table E1–1. Information Contained in Scratch Pad Registers

Fields	Set	Return
Refresh Frequencies	Set Monitor Type	Inquire User Options
Maximum Resolution	Set Monitor Type	Inquire User Options
Memory Size	(not applicable)	Return Installed Memory

2. VIDEO MODES

2.1 Standard VGA Modes

The Cirrus Logic VGA BIOS supports all standard VGA modes. These standard VGA modes are listed in the following table

Table E1–1. IBM Standard VGA Video Modes

Mode No.	VESA® No.	No. of Colors	Char. x Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
0, 1	0, 1	16/256K	40 x 25	9 x 16	360 x 400	Text	14	31.5	70
2, 3	2, 3	16/256K	80 x 25	9 x 16	720 x 400	Text	28	31.5	70
4, 5	4, 5	4/256K	40 x 25	8 x 8	320 x 200	Graphics	12.5	31.5	70
6	6	2/256K	80 x 25	8 x 8	640 x 200	Graphics	25	31.5	70
7	7	Monochrome	80 x 25	9 x 16	720 x 400	Text	28	31.5	70
D	D	16/256K	40 x 25	8 x 8	320 x 200	Graphics	12.5	31.5	70
E	E	16/256K	80 x 25	8 x 14	640 x 200	Graphics	25	31.5	70
F	F	Monochrome	80 x 25	8 x 14	640 x 350	Graphics	25	31.5	70
10	10	16/256K	80 x 25	8 x 14	640 x 350	Graphics	25	31.5	70
11	11	2/256K	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60
11+	11	2/256K	80 x 30	8 x 16	640 x 480	Graphics	31.5	37.5	75
12	12	16/256K	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60
12+	12+	16/256K	80 x 30	8 x 16	640 x 480	Graphics	31.5	37.5	75
13	13	256/256K	40 x 25	8 x 8	320 x 200	Graphics	12.5	31.5	70

NOTE:

1) An 8 x 14 font for the modes with an 8 x 14 font may be provided with a DOS TSR. If the TSR has not been loaded when the mode is set, the 8 x 16 font will be used with the two bottom rows deleted. This causes

truncation of characters with descenders, but does not restrict program operation nor does it make characters particularly difficult to read. For absolute compatibilty with some DOS applications which use the 8 x 14 font, the TSR should be used.

2.2 Extended Video Modes

The CL-GD543X VGA BIOS supports standard VESA® and Extended Modes. These modes are listed in the following table.

Table E1–2. Cirrus Logic Extended Video Modes

Mode No.	VESA® No.	No. of Colors	Char. x Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
14, 55	109	16/256K	132 x 25	8 x 16	1056 x 400	Text	41.5	31.5	70
54	10A	16/256K	132 x 43	8 x 8	1056 x 350	Text	41.5	31.5	70
58, 6A	102	16/256K	100 x 37	8 x 16	800 x 600	Graphics	40	37.8	60
58, 6A	102	16/256K	100 x 37	8 x 16	800 x 600	Graphics	50	48.1	72
58 ,6A	102	16/256K	100 x 37	8 x 16	800 x 600	Graphics	49.5	46.9	75
5C	103	256/256K	100 x 37	8 x 16	800 x 600	Graphics	40	37.9	60
5C	103	256/256K	100 x 37	8 x 16	800 x 600	Graphics	50	48.1	72
5C	103	256/256K	100 x 37	8 x 16	800 x 600	Graphics	49.5	46.9	75
5D†	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	44.9	35.5	87†
5D	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	65	48.3	60
5D	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	75	56	70
5D	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	78.7	60	75
5E	100	256/256K	80 x 25	8 x 16	640 x 400	Graphics	25	31.5	70
5F	101	256/256K	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60
5F	101	256/256K	80 x 30	8 x 16	640 x 480	Graphics	31.5	37.5	75
60†	105	256/256K	128 x 48	8 x 16	1024 x 768	Graphics	44.9	35.5	87†
60	105	256/256K	128 x 48	8 x 16	1024 x 768	Graphics	65	48.3	60
60	105	256/256K	128 x 48	8 x 16	1024 x 768	Graphics	75	56	70
60	105	256/256K	128 x 48	8 x 16	1024 x 768	Graphics	78.7	60	75
64	111	64K	–	–	640 x 480	Graphics	25	31.5	60
64	111	64K	–	–	640 x 480	Graphics	31.5	37.5	75
65	114	64K	–	–	800 x 600	Graphics	40	37.8	60

Table E1–2. Cirrus Logic Extended Video Modes *(cont.)*

Mode No.	VESA® No.	No. of Colors	Char. x Row	Char. Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
65	114	64K	–	–	800 x 600	Graphics	50	48.1	72
65	114	64K	–	–	800 x 600	Graphics	49.5	46.9	75
66	110	32K‡	–	–	640 x 480	Graphics	25	31.5	60
66	110	32K‡	–	–	640 x 480	Graphics	31.5	37.5	75
67	113	32K‡	–	–	800 x 600	Graphics	40	37.8	60
67	113	32K‡	–	–	800 x 600	Graphics	50	48.1	72
67	113	32K‡	–	–	800 x 600	Graphics	49.5	46.9	75
68†	116	32K‡	–	–	1024 x 768	Graphics	44.9	35.5	87†
68	116	32K‡	–	–	1024 x 768	Graphics	65	48.3	60
68	116	32K‡	–	–	1024 x 768	Graphics	75	56	70
68	116	32K‡	–	–	1024 x 768	Graphics	78.7	60	75
69†		32K‡	–	–	1280 x 1024	Graphics	75	48	87†
6C†	106	16/256K	160 x 64	8 x 16	1280 x 1024	Graphics	75	48	87†
6D†	–	256/256K	160 x 64	8 x 16	1280 x 1024	Graphics	75	48	87†
6D	–	256/256K	160 x 64	8 x 16	1280 x 1024	Graphics	108	65	60
71	112	16M	–	–	640 x 480	Graphics	25	31.5	60
72↕	115	16M+A	–	–	800 x 600	Graphics	40	37.8	60
73↕	–	16M+A	–	–	1024 x 768	Graphics	44.9	35.5	87†
74†	117	64K	–	–	1024 x 768	Graphics	44.9	35.5	87†
74	117	64K	–	–	1024 x 768	Graphics	65	48.3	60
74	117	64K	–	–	1024 x 768	Graphics	75	56	70
74	117	64K	–	–	1024 x 768	Graphics	78.7	60	75
75	–	64K	–	–	1280 x 1024	Graphics	75	48	87†
76↕	–	16M+A	–	–	640 x 480	Graphics	25	31.5	60
76↕	–	16M+A	–	–	640 x 480	Graphics	31.5	37.5	75

NOTES:

1) Some modes are not supported by all configurations of all CL-GD543X controllers. Refer to the following table for further information.

2) Some modes are not supported by all monitors. The fastest vertical refresh rate for the monitor type selected will be automatically used.
3) '‡' character indicates 32K Direct-Color/256-color Mixed Mode.
4) '†' character indicates Interlaced Mode.
5) '↕' character indicates 16M colors, but with 32-bit-per-pixel format. 16M+A indicates the same.
6) An 8 x 14 font for mode 55h may be provided with a DOS TSR. If the TSR has not been loaded when the mode is set, the 8 x 16 font will be used with the two bottom rows deleted. This causes truncation of characters with descenders, but does not restrict program operation nor does it make characters particularly difficult to read. For absolute compatibilty with some DOS applications which use the 8 x 14 font, the TSR should be used.

2.3 Extended Video Mode Requirements: CL-GD5430

Many of the extended Video Mode Modes require more Display Memory and memory bandwidth than is available in the smallest possible configuration. The minimum configuration of the CL-GD5430 supports all extended text modes as well as modes 58, 5D, 5E, 5F as all refresh rates. The CL-GD5430 does not support modes 72, 73, or 75.

The following table specifies the minimum MLCK required to support the various extended video modes on the CL-GD5430. MCLKs outside the range 45-60 MHz are not considered. NEM indicates Not Enough Memory; BW indicates insufficient BandWidth.

Table E1–3. Cirrus Logic Extended Video Mode Requirements: CL-GD5430

Mode No.	No. of Colors	Screen Format	Pixel Freq. MHz	Vert. Freq. Hz	5430 512K 16 bits	5430 1MB 32 bits	5430 2MB 32 bits
5C	256	800 x 600	40	60	50 MHz	45 MHz	45 MHz
5C	256	800 x 600	50	72	60 MHz	45 MHz	45 MHz
5C	256	800 x 600	49.5	75	60 MHz	45 MHz	45 MHz
60†	256	1024 x 768	44.9	87†	NEM	45 MHz	45 MHz
60	256	1024 x 768	65	60	NEM	45 MHz	45 MHz
60	256	1024 x 768	75	70	NEM	45 MHz	45 MHz
60	256	1024 x 768	78.7	75	NEM	45 MHz	45 MHz
64	64K	640 x 480	25	60	NEM	45 MHz	45 MHz
64	64K	640 x 480	31.5	75	NEM	45 MHz	45 MHz
65	64K	800 x 600	40	60	NEM	48 MHz	48 MHz
65	64K	800 x 600	50	72	NEM	60 MHz	60 MHz
65	64K	800 x 600	49.5	75	NEM	60 MHz	60 MHz
66	32K‡	640 x 480	25	60	NEM	45 MHz	45 MHz
66	32K‡	640 x 480	31.5	75	NEM	45 MHz	45 MHz

Table E1–3. Cirrus Logic Extended Video Mode Requirements: CL-GD5430 *(cont.)*

Mode No.	No. of Colors	Screen Format	Pixel Freq. MHz	Vert. Freq. Hz	5430 512K 16 bits	5430 1MB 32 bits	5430 2MB 32 bits
67	32K‡	800 x 600	40	60	NEM	48 MHz	48 MHz
67	32K‡	800 x 600	50	72	NEM	60 MHz	60 MHz
67	32K‡	800 x 600	49.5	75	NEM	60 MHz	60 MHz
68†	32K‡	1024 x 768	44.9	87†	NEM	NEM	60 MHz
68	32K‡	1024 x 768	65	60	NEM	NEM	BW
68	32K‡	1024 x 768	75	70	NEM	NEM	BW
68	32K‡	1024 x 768	78.7	75	NEM	NEM	BW
69†	32K‡	1280 x 1024	75	87†	NEM	NEM	NEM
6C†	16	1280 x 1024	75	87†	NEM	45 MHz	45 MHz
6D†	256	1280 x 1024	75	87†	NEM	NEM	48 MHz
6D	256	1280 x 1024	108	60	NEM	NEM	60 MHz
71	16M	640 x 480	25	60	NEM	45 MHz	45 MHz
74†	64K	1024 x 768	44.9	87†	NEM	NEM	55 MHz
74	64K	1024 x 768	65	60	NEM	NEM	BW
74	64K	1024 x 768	75	70	NEM	NEM	BW
74	64K	1024 x 768	78.7	75	NEM	NEM	BW
75	64K	1280 x 1024	75	87†	NEM	NEM	NEM

2.4 Extended Video Mode Requirements: CL-GD5434

Many of the extended Video Mode Modes require more Display Memory and memory bandwidth than is available in the smallest possible configuration. The minimum configuration of the CL-GD5434 supports all extended text modes, as well as modes 58, 5C, 5D, 5E, 5F, 64, 66, and 6C at all refresh rates.

The following table specifies the minimum MLCK required to support the various extended video modes on the CL-GD5434. MCLKs outside the range 45-50 MHz are not considered.

NEM indicates Insufficient Memory; BW indicates insufficient BandWidth.

Table E1–4. Cirrus Logic Extended Video Mode Requirements: CL-GD5434

Mode No.	No. of Colors	Screen Format	Pixel Freq. MHz	Vert. Freq. Hz	5434 1 MB 32 bits	5434 2MB 64 bits	5434 4MB 64 bits
60†	256	1024 x 768	44.9	87†	45 MHz	45 MHz	45 MHz
60	256	1024 x 768	65	60	45 MHz	45 MHz	45 MHz
60	256	1024 x 768	75	70	45 MHz	45 MHz	45 MHz
60	256	1024 x 768	78.7	75	50 MHz	45 MHz	45 MHz
65	64K	800 x 600	40	60	50 MHz	45 MHz	45 MHz
65	64K	800 x 600	50	72	BW	45 MHz	45 MHz
65	64K	800 x 600	49.5	75	BW	45 MHz	45 MHz
67	32K‡	800 x 600	40	60	50 MHz	45 MHz	45 MHz
67	32K‡	800 x 600	50	72	BW	45 MHz	45 MHz
67	32K‡	800 x 600	49.5	75	BW	45 MHz	45 MHz
68†	32K‡	1024 x 768	44.9	87†	NEM	45 MHz	45 MHz
68	32K‡	1024 x 768	65	60	NEM	45 MHz	45 MHz
68	32K‡	1024 x 768	75	70	NEM	45 MHz	45 MHz
68	32K‡	1024 x 768	78.7	75	NEM	45 MHz	45 MHz
69†	32K‡	1280 x 1024	75	87†	NEM	NEM	45 MHz
6D†	256	1280 x 1024	75	87†	NEM	45 MHz	45 MHz
6D	256	1280 x 1024	108	60	NEM	45 MHz	45 MHz
71	16M	640 x 480	25	60	45 MHz	45 MHz	45 MHz
72‡	16M+A	800 x 600	40	60	NEM	50 MHz	48 MHz
73‡	16M+A	1024 x 768	44.9	87†	NEM	NEM	48 MHz
74†	64K	1024 x 768	44.9	87†	NEM	45 MHz	45 MHz
74	64K	1024 x 768	65	60	NEM	45 MHz	45 MHz
74	64K	1024 x 768	75	70	NEM	45 MHz	45 MHz
74	64K	1024 x 768	78.7	75	NEM	45 MHz	45 MHz
75	64K	1280 x 1024	75	87†	NEM	NEM	45 MHz
76‡	16M+A	640 x 480	25	60	NEM	45 MHz	45 MHz
76‡	16M+A	640 x 480	31.5	75	NEM	45 MHz	45 MHz

3. INTERRUPT 10H INTERFACE EXTENSIONS

The Cirrus Logic BIOS supports all standard VGA BIOS Interrupt 10h video service functions. In addition, the BIOS provides extensive support for various features of the Cirrus Logic VGA controller. These functions are available as extended functions under Interrupt 10h.

The standard VGA BIOS Interrupt 10h video service functions are not described in this document. The VESA extensions are covered in section 4 of this appendix.

All extended function calls will preserve the CPU Registers, except those used to pass information from the BIOS.

3.1 Function Summary

The following table provides an overview of the extended functions provided by the Cirrus Logic BIOS.

AH Register	BL Register	Function
12h	80h	Inquire VGA Type
12h	81h	Inquire BIOS Version Number
12h	82h	Inquire Design Revision Code
12h	85h	Return Installed Memory
12h	9Ah	Inquire User Options
12h	9Eh	Set Memory Performance
12h	A0h	Query Video Mode Availability
12h	A1h	Read Monitor Type and ID
12h	A4h	Set Monitor Type

3.2 Inquiry Functions

The inquiry functions are supported for all versions of the video BIOS. These functions allow applications software to determine and use other functions described in the user options. In addition to the Cirrus Logic inquiry functions described here, please see the DPMS inquiry function described in the VESA section.

3.2.1 Inquire VGA Type

This function provides a mechanism for software to determine the type of Cirrus Logic VGA controller, silicon revision number and its corresponding hardware capabilities. BIOS versions that do not support this family of function will preserve the input value in AL Register. The VGA types of particular interest to readers of this manual are in **bold** type.

Input: AH= 12h
BL= 80h

Output: AX= Controller type
0= No extended alternate select support
1= Reserved
2= CL-GD510/520
3= CL-GD610/620
4= CL-GD5320
5= CL-GD6410
6= CL-GD5410
7= CL-GD6420
8= CL-GD6412
10h= CL-GD5401
11h= CL-GD5402
12h= CL-GD5420
13h= CL-GD5422
14h= CL-GD5424
15h= CL-GD5426
16h= CL-GD5420r1
17h= CL-GD5402rl
18h= CL-GD5428
19h= CL-GD5429
20h= CL-GD6205
21h= CL-GD6215
22h= CL-GD6225
23h= CL-GD6235
24h= CL-GD6245
30h= CL-GD5432
31h= CL-GD5434
32h= CL-GD5430
40h= CL-GD6440
52h= CL-GD5452

BL= Silicon revision number
0-7Fh= Silicon revision
80h= Silicon revision number not available

3.2.2 Inquire BIOS Version Number

This function provides a mechanism for software to determine the BIOS version number.

Input: AH= 12h
BL= 81h

Output: AH= Major BIOS version number
AL= Minor BIOS version number

Example: If BIOS version is 1.02, then AH is 01 and AL is 02.

3.2.3 Inquire Cirrus Logic Design Revision Code

This function provides a mechanism for software to determine the revision of Cirrus Logic silicon.

Input: AH= 12h
BL= 82h

Output: AL= Chip revision

3.2.4 Return Installed Memory

The function returns the amount of video memory present in 64K units.

Input: AH= 12h
BL= 85h

Output: AL= Amount of video memory present in 64K units.

3.3 Global Functions

3.3.1 Inquire User Options

This function returns the current status of user options.

Input: AH= 12h
BL= 9Ah

Output: AX= Contains the following options
Bits 1:0= Reserved
Bits 4:2= Monitor Type (Horizontal)
Bits 13:5 Reserved
Bit 14= Vertical montype 640 x 480 frequency (VGA refresh)
Bit 15= Reserved
BX= Reserved
CX= Contains the following options
Bit 0= Reserved
Bits 3:1= 1280 x 1024 vertical frequency
Bits 7:4= Maximum Vertical Resolution
Bits 11:8= 800 x 600 vertical frequency
Bits 15:12= 1024 x 768 vertical frequency
DX= Reserved

3.3.2 Query Video Mode Availability

Input: AH= 12h
AL= Video mode number (0-7fh)
BL= A0h

Output: AH= Bit 0
0= Video mode not supported
1= Video mode supported

DS:SI: Pointer to standard video parameters, or FFFF:FFFF if standard parameters undefined for this mode
ES:DI: Pointer to supplemental video parameters, or FFFF:FFFF if supplemental parameters undefined for this mode

BX= Offset to BIOS sub-routine that will fix up the parameters pointed to by DS:SI. This routine requires ES:DI points to the proper supplemental video parameters.

3.3.3 Read Monitor ID/Type

This function reads the Monitor ID and senses the type of monitor attached.

Input:
AH = 12h
BL = A1h Read monitor ID and type from 15-pin connector

Output:
BH = Monitor ID
09h = IBM 8604/8507 or equivalent
0Ah = IBM 8514 or equivalent
0Bh = IBM 8515 or equivalent
0Dh = IBM 8503 or equivalent
0Eh = IBM 8512/8513 or equivalent
0Fh = No monitor
00..08, 0C = reserved

BL = Monitor gender
00 = Color display
01 = Grayscale display
02 = No display

3.3.4 Set Monitor Type

This function sets the monitor type in terms of vertical timings. The monitor type information is used by the BIOS to determine which frequency to use when selecting an extended mode. It is also used (in conjunction with the amount of display memory available) to determine what extended modes are available. The monitor type can be read back using Function 9A.

To maintain compatablity with previous Cirrus Logic BIOS releases, obsolete frequencies have not been removed from this function. The appearance of any frequency in the description of this BIOS call is no guarantee that any given BIOS will actually support that frequency. In general, the trend is toward supporting higher frequencies and deleting support of lower frequencies.

Note: Calls to the obsolete functions 0A2h (Set Monitor Type - Horizontal) and 0A3h (Set Refresh Type) will be converted into this call.

Input:
AH = 012h
BL = 0A4h
AL[3:0] = Maximum Vertical Resolution
000h = 480 scanlines
001h = 600 scanlines
002h = 768 scanlines
003h = 1024 scanlines
004h - 00Fh = Reserved
AL[4] = 640 x 480 Frequency
0h = 60 Hz

1h = 75 Hz
AL[7:5] = Reserved
BH[3:0] = 800 x 600 Frequency
000h = 56 Hz
001h = 60 Hz
002h = 72 Hz
003h = 75 Hz
004h - 00Fh = Reserved
BH[7:4] = 1024 x 768 Frequency
000h = 87i Hz
001h = 60 Hz
002h = 70 Hz
003h = 72 Hz
004h = 75 Hz
005h - 00Fh = Reserved
CH[3:0] = Reserved
CH[7:4] = 1280 x 1024 Frequency
000h = 87i Hz
001h = 60 Hz
002h = 70 Hz
003h - 00Fh = Reserved
CL = Reserved
DX = Reserved

3.3.5 Set Memory Clock Speed

This function allows the user to set the memory clock. This allows the standard memory clock speed to be overridden. The standard memory clock speed is defined by the OEM using the OEMSI utility.

Input:
AH = 012h
BL = 09Eh
AL = Subfunction
0 = Reserved
1 = Reserved
2 = Program value provided in BH
BH = Value to be programmed into SR1F.

The memory clock can be calculated using the equation:

$$MCLK \cong BH \bullet 1.79MHz$$

where BH is the value provided to the function, and the reference frequency is 14.31818 MHz. If the reference frequency is not 14.3...MHz, the output frequency will scale.

4. VESA® SUPER VGA STANDARD

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Purpose: To standardize a common software interface to Super VGA video adapters to provide simplified software application access to advanced VGA products.

Summary: The standard provides a set of functions that an application program can use to:
a) obtain information about the capabilities and characteristics of a specific Super VGA implementation, and
b) to control the operation of such hardware in terms of video mode initialization and video memory access. The functions are provided as an extension to the VGA BIOS video services, accessed through Interrupt 10h.

4.1 Goals and Objectives

The purpose of the VESA VGA BIOS Extension is to provide a common software interface for developers to design applications successfully on widely disparate architectures. Being a common software interface to Super VGA graphics products, the primary objective is to enable application and system software to adapt to and exploit the wide range of features available in these VGA extensions.

The VESA BIOS Extension attempts to address the following two main issues:
a) Return information about the video environment to the application, and
b) Assist the application in initializing and programming the hardware.

4.1.1 Video Environment Information

The VESA BIOS Extension provides several functions to return information about the video environment. These functions return system-level information as well as video-mode-specific details. Function 00h returns general system-level information, including an OEM identification string. The function also returns a pointer to the supported video modes. Function 01h may be used by the application to obtain information about each supported video mode. Function 03h returns the current video mode.

4.1.2 Programming Support

The VESA BIOS Extension provides several functions to interface to the different Super VGA hardware implementations. The most important of these is Function 02h, Set Super VGA Video Mode. This function isolates the application from the tedious and complicated task of setting up a video mode. Function 05h provides an interface to the underlying memory-mapping hardware. Function 04h enables an application to save and restore a Super VGA state without determining specifics of the particular implementation.

4.1.3 Compatibility

The primary design objective of the VESA BIOS Extension is to preserve maximum compatibility to the standard VGA environment. In no way should the BIOS extensions compromise compatibility or performance. Another related concern is to minimize the changes necessary to an existing VGA BIOS. RAM- as well as ROM-based implementations of the BIOS extension should be possible.

4.2 Standard VGA BIOS

A primary design goal with the VESA BIOS Extension is to minimize the effects on the standard VGA BIOS. Standard VGA BIOS functions should need to be modified as little as possible. This is important since ROM- as well as RAM-based versions of the extension may be implemented.

Two standard VGA BIOS functions are affected by the VESA extension. These are Function 00h (Set Video Mode) and Function 0Fh (Read current video state). VESA-aware applications will not set the video mode using VGA BIOS Function 00h. Nor will such applications use VGA BIOS Function 0Fh. VESA BIOS Functions 02h (Set Super VGA Mode) and 03h (Get Super VGA Mode) will be used instead.

VESA-unaware applications (such as old Pop-up programs and other TSRs, or the CLS command of MS-DOS), might use VGA BIOS Function 0Fh to get the present video mode. Later it may call VGA BIOS Function 00h to restore/re-initialize the old video mode.

To make such applications run properly, VESA recommends that whatever value returned by VGA BIOS Function 0Fh (it is the OEM's responsibility to define this number), it can be used to re-initialize the video mode through VGA BIOS Function 00h. Thus, the BIOS should record the last Super VGA Mode in effect.

It is recommended, but not mandatory, to support output functions (such as TTY-output, scroll, set pixel, etc.) in Super VGA Modes. If the BIOS extension doesn't support such output functions, Bit D2 (Output functions supported) of the ModeAttributes field (returned by VESA BIOS Function 01h) should be cleared.

4.3 Super VGA Mode Numbers

Standard VGA Mode numbers are 7-bits-wide and presently ranges from 00h to 13h. OEMs have defined extended video modes in the range 14h to 7Fh. Values in the range 80h to FFh cannot be used, since VGA BIOS Function 00h (Set Video Mode) interprets Bit 7 as a flag to clear/not clear video memory.

Due to the limitations of 7-bit Mode numbers, VESA Video Mode numbers are 15-bits-wide. To initialize a Super VGA Mode, its number is passed in the BX Register to VESA BIOS Function 02h (Set Super VGA Mode).

The format of VESA Mode numbers is as follows:

D0-D8=	Mode number If D8 = 0, this is not a VESA-defined mode If D8 = 1, this is a VESA-defined mode
D9-D14=	Reserved by VESA for future expansion (= 0)
D15=	Reserved (= 0)

4.4 Extended VGA BIOS

Several new BIOS calls have been defined to support Super VGA Modes. For maximum compatibility with the standard VGA BIOS, these calls are grouped under one function number. This number is passed in the AH Register to the INT 10h handler.

The designated Super VGA extended function number is 4Fh. This function number is presently unused in most, if not all, VGA BIOS implementations. A standard VGA BIOS performs no action when function call 4F is made. Super VGA Standard VS911022 defines subfunctions 00H through 08H. Subfunction numbers 09H through 0FFH are reserved for future use.

4.4.1 Status Information

Every function returns status information in the AX Register. The format of the status word is as follows:

AL = 4Fh: Function is supported
AL ! = 4Fh: Function is not supported
AH = 00h: Function call successful
AH = 01h: Function call failed

Software should treat a non-zero value in the AH Register as a general failure condition. In later versions of the VESA BIOS Extension new error codes might be defined.

4.4.2 Function 00h — Return Super VGA information

The purpose of this function is to provide information to the calling program about the general capabilities of the Super VGA environment. The function fills an information block structure at the address specified by the caller. The information block size is 256 bytes.

Input: AH= 4Fh Super VGA support
AL= 00h Return Super VGA information
ES:DI= Pointer to buffer

Output: AX= Status
All other registers are preserved.

The information block has the following structure:

```
VgaInfoBlock struc
    VESASignature   db      'VESA'          ; 4 signature bytes
    VESAVersion     dw      ?               ; VESA version number
    OEMStringPtr    dd      ?               ; Pointer to OEM string
    Capabilities    db      4 dup (?)       ; capabilities of the video environment
    VideoModePtr    dd      ?               ; pointer to supported Super VGA Modes
    TotalMemory     dw      ?               ; Number of 64kb memory blocks on board
    Reserved        db      236 dup (?)     ; Remainder of VgaInfoBlock
VgaInfoBlock ends
```

The VESASignature field contains the characters 'VESA' if this is a valid block.

The VESAVersion is a binary field that specifies what level of the VESA standard the Super VGA BIOS conforms to. The higher byte specifies the major version number. The lower byte specifies the minor version number. The current VESA version number is 1.2. Applications written to use the features of a specific version of the VESA BIOS Extension are guaranteed to work in later versions. The VESA BIOS Extension will be fully upwards compatible.

The OEMStringPtr is a far pointer to a null-terminated OEM-defined string. The string may used to identify the video chip, video board, memory configuration, etc., to hardware-specific display drivers. There are no restrictions on the format of the string.

The Capabilities field describes what general features are supported in the video environment. The bits are defined as follows:

D0= DAC is switchable

0 = DAC is fixed width, with 6-bits per primary color
1 = DAC width is switchable
D1-31 = Reserved

The VideoModePtr points to a list of supported Super VGA (VESA-defined as well as OEM-specific) Mode numbers. Each mode number occupies one word (16 bits). The list of mode numbers is terminated by a -1 (0FFFFh). Please refer to Section 4.3 for a description of VESA Mode numbers. The pointer could point into either ROM or RAM, depending on the specific implementation. Either the list would be a static string stored in ROM, or the list would be generated at run-time in the information block (see above) in RAM. It is the applications responsibility to verify the current availability of any mode returned by this Function through the Return Super VGA Mode information (Function 1) call. Some of the returned modes may not be available due to the video boards current memory and monitor configuration.

The TotalMemory field indicates the amount of memory installed on the VGA board. Its value represents the number of 64K bytes blocks of memory currently installed.

4.4.3 Function 01h — Return Super VGA Mode Information

This function returns information about a specific Super VGA Video Mode that was returned by Function 0. The function fills a mode information block structure at the address specified by the caller. The mode information block size is maximum 256 bytes.

Some information provided by this function is implicitly defined by the VESA Mode number. However, some Super VGA implementations might support other video modes than those defined by VESA. To provide access to these modes, this function also returns various other information about the mode.

Input:	AH=	4Fh	Super VGA support
	AL=	01h	Return Super VGA Mode information
	CX=		Super VGA Video Mode number
	ES:DI=		Pointer to 256 byte buffer
Output:	AX=		Status
	All other registers are preserved.		

The mode information block has the following structure:

```
ModeInfoBlock   struc
; mandatory information

ModeAttributes      dw    ?     ; mode attributes
WinAAttributes      db    ?     ; window A attributes
WinBAttributes      db    ?     ; window B attributes
WinGranularity      dw    ?     ; window granularity
WinSize             dw    ?     ; window size
WinASegment         dw    ?     ; window A start segment
WinBSegment         dw    ?     ; window B start segment
WinFuncPtr          dd    ?     ; pointer to window function
BytesPerScanLine    dw    ?     ; bytes per scanline extended information

XResolution         dw    ?     ; horizontal resolution
```



```
        YResolution             dw      ?       ; vertical resolution
        XCharSize               db      ?       ; character cell width
        YCharSize               db      ?       ; character cell height
        NumberOfPlanes          db      ?       ; number of memory planes
        BitsPerPixel            db      ?       ; bits per pixel
        NumberOfBanks           db      ?       ; number of banks
        MemoryModel             db      ?       ; memory model type
        BankSize                db      ?       ; bank size in kb
        NumberOfImagePages      db      ?       ; Number of Images
        Reserved                db      1       ; reserved for page function

        RedMaskSize             db      ?       ;size of direct color red mask in  bits
        RedFieldPosition        db      ?       ;bit position of lsb of red mask
        GreenMaskSize           db      ?       ;size of direct color green mask in bits
        GreenFieldPosition      db      ?       ;bit position of lsb of green mask
        BlueMaskSize            db      ?       ;size of direct color blue mask in bits
        BlueFieldPosition       db      ?       ;bit position of lsb of blue mask
        RsvdMaskSize            db      ?       ;size of direct color reserved mask in bits
        RsvdFieldPosition       db      ?       ;bit position of lsb of reserved mask
        DirectColorModeInfo     db      ?       ;Direct Color Mode attributes

        Reserved                db      216 dup (?)  ; remainder of ModeInfoBlock
ModeInfoBlock   ends
```

The ModeAttributes field describes certain important characteristics of the video mode. Bit D0 specifies whether this mode can be initialized in the present video configuration. This bit can be used to block access to a video mode if it requires a certain monitor type, and that this monitor is presently not connected. Bit D1 specifies whether extended mode information is available. This information is required in VESA BIOS Extension Ver. 1.2 and later. Bit D2 indicates whether the BIOS have support for output functions such as TTY output, scroll, pixel output, etc., in this mode (it is recommended, but not mandatory, that the BIOS have support for all output functions).

The field is defined as follows:

D0= Mode supported in hardware
- 0= Mode not supported in hardware
- 1= Mode supported in hardware

D1= Extended information available
- 0= Extended Mode information not available
- 1= Extended Mode information available

D2= Output functions supported by BIOS
- 0= Output functions not supported by BIOS
- 1= Output functions supported by BIOS

D3= Monochrome/Color Mode (see note below)
- 0= Monochrome Mode
- 1= Color Mode

D4= Mode type
- 0= Text Mode
- 1= Graphics Mode

D5-D15= Reserved

NOTE: Monochrome modes have their CRTC address at 3B4h. Color modes have their CRTC address at 3D4h. Monochrome modes have attributes in which only Bit 3 (video) and Bit 4 (in-

tensity) of the attribute controller output are significant. Therefore, monochrome text modes have attributes of off, video, high intensity, blink, etc. monochrome graphics modes are two-plane graphics modes and have attributes of off, video, high intensity, and blink. Extended two-color modes that have their CRTC address at 3D4h, are color modes with one bit per pixel and one plane. The standard VGA Modes, 06h and 11h would be classified as color modes, while the standard VGA Modes 07h and 0fh would be classified as monochrome modes.

The BytesPerScanline field specifies how many bytes each logical scanline consists of. The logical scanline could be equal to or larger than the displayed scanline.

The WinAAttributes and WinBAttributes describe the characteristics of the CPU windowing scheme such as whether the windows exist and are read/writable, as follows:

D0= Window supported
- 0= Window is not supported
- 1= Window is supported

D1= Window readable
- 0= Window is not readable
- 1= Window is readable

D2= Window writable
- 0= Window is not writable
- 1= Window is writable

D3-D7= Reserved

If neither window is supported (Bit D0 = 0), then an application can assume that window paging is not supported, and that the display memory buffer resides at the CPU address appropriate for the MemoryModel of the mode.

The WinGranularity specifies the smallest boundary, in kilobytes, on which the window can be placed in the video memory. If WinGranularity equals a '0' then CPU display memory windowing is not supported.

The WinSize specifies the size of the window in kilobytes.

The WinASegment and WinBSegment address specify the segment addresses where the windows are located in the CPU address space.

The WinFuncAddr specifies the address of the CPU video memory windowing function. The windowing function can be invoked either through VESA BIOS Function 05h, or by calling the function directly. A direct call will provide faster access to the Hardware Paging Registers than using INT 10h, and is intended to be used by high-performance applications. If WinFuncPtr is NULL (0000:0000) then CPU display memory windowing is not supported.

The XResolution and YResolution specify the width and height of the video mode. In graphics modes, this resolution is in units of pixels. In text modes this resolution is in units of characters. Note that text mode resolutions, in units of pixels, can be obtained by multiplying XResolution and YResolution by the cell width and height, if the extended information is present.

The XCharSize and YCharSize specify the size of the character cell in pixels.

The NumberOfPlanes field specifies the number of memory planes available to software in

that mode. For standard 16-color VGA graphics, this would be set to a four. For standard Packed-pixel Modes, the field would be set to a '1'.

The BitsPerPixel field specifies the total number of bits that define the color of one pixel. For example, a standard VGA Four-plane 16-color Graphics Mode would have a four in this field and a packed-pixel 256-color Graphics Mode would specify a eight in this field. The number of bits per pixel per plane can normally be derived by dividing the BitsPerPixel field by the NumberOfPlanes field.

The MemoryModel field specifies the general type of memory organization used in this mode. The following models have been defined:

00h=	Text Mode
01h=	CGA graphics
02h=	Hercules graphics
03h=	Four-plane planar
04h=	Packed pixel
05h=	Non-chain4, 256 color
06h=	Direct Color
07h=	YUV
08h-0fh=	Reserved, to be defined by VESA
10h-ffh=	To be defined by OEM

In Version 1.1 and earlier of the VESA Super VGA BIOS Extension, Direct Color 1:5:5:5, 8:8:8, and 8:8:8:8 are defined as Packed Pixel model with 16, 24, and 32 bits per pixel, respectively. In Version 1.2 and later of the VESA Super VGA BIOS Extension, it is recommended that Direct-color Modes use the Direct-color MemoryModel and use the MaskSize and FieldPosition fields of the ModeInfoBlock to describe the pixel format. BitsPerPixel is always defined to be the total size of the pixel, in bits.

The NumberOfBanks is the number of banks in which the scanlines are grouped. The remainder from dividing the scanline number by the number of banks is the bank that contains the scanline and the quotient is the scanline number within the bank. For example, CGA graphics modes have two banks and Hercules® Graphics Mode has four banks. For modes that don't have scanline banks (such as VGA Modes 0Dh-13h), this field should be set to a '1'.

The BankSize field specifies the size of a bank (group of scanlines) in units of 1K byte. For CGA and Hercules graphics modes this is a eight, as each bank is 8192 bytes in length. For modes that don't have scanline banks (such as VGA Modes 0Dh-13h), this field should be set to a '0'.

The NumberOfImagePages field specifies the number of additional complete display images that will fit into the VGA memory, at one time, in this mode. The application may load more than one image into the VGA memory if this field is a non-zero, and flip the display between the images.

The Reserved field has been defined to support a future VESA BIOS extension feature and will always be set to a '1' in this version.

The RedMaskSize, GreenMaskSize, BlueMaskSize, and RsvdMaskSize fields define the size, in bits, of the red, green, and blue components of a Direct-color Pixel. A bit mask can

be constructed from the MaskSize fields using simple shift arithmetic. Example MaskSize values for Direct-color 5:6:5 Mode would be 5, 6, 5, and 0, for the red, green, blue, and reserved fields, respectively. The MaskSize fields should be set to a '0' in modes using a MemoryModel that does not have pixels with component fields.

The RedFieldPosition, GreenFieldPosition, BlueFieldPosition, and RsvdFieldPosition fields define the bit position within the Direct-color Pixel or YUV pixel of the least-significant bit of the respective color component. A color value can be aligned with its pixel field by shifting the value left by the FieldPosition. Example FieldPosition values for Direct-color 5:6:5 Mode would be 11, 5, 0, and 0, for the red, green, blue, and reserved fields, respectively. The FieldPosition fields should be set to a '0' in modes using a MemoryModel that does not have pixels with component fields.

The DirectColorModeInfo field describes important characteristics of Direct-color Modes. Bit D0 specifies whether the color ramp of the DAC is fixed or programmable. If the color ramp is fixed, then it cannot be changed. If the color ramp is programmable, it is assumed that the red, green, and blue lookup tables can be loaded using a standard VGA DAC Color Registers BIOS Call (AX=1012h). Bit D1 specifies whether the Rsvd field of the Direct-color Pixel can be used by the application or is reserved, and thus unusable.

D0= Color ramp is fixed/programmable
- 0= Color ramp is fixed
- 1= Color ramp is programmable

D1= Rsvd field is usable/reserved
- 0= Rsvd field is reserved
- 1= Rsvd field is usable by the application

The MapFuncAddr specifies the address of the mapping function. The mapping function can be invoked either through VESA BIOS Function 06h, or by calling the function directly. A direct call will provide a faster memory mapping than using INT 10h, and is intended to be used by high-performance applications.

NOTE: Version 1.1 and later VESA BIOS extensions will zero-out all unused fields in the Mode Information Block, always returning exactly 256 bytes. This facilitates upward compatibility with future versions of the standard, as any newly-added fields will be designed such that values of zero will indicate nominal defaults or non-implementation of optional features. (For example, a field containing a bit-mask of extended capabilities would reflect the absence of all such capabilities.) Applications that wish to be backwards-compatible to Version 1.0 VESA BIOS extensions should pre-initialize the 256-byte buffer before calling Return Super VGA mode Information.

4.4.4 Function 02h — Set Super VGA Video Mode

This function initializes a video mode. The BX Register contains the video mode number. The format of VESA Mode numbers is described in Section 2. If the mode cannot be set, the BIOS should leave the video environment unchanged and return a failure error code.

Input:

AH=	4Fh	Super VGA support
AL=	02h	Set Super VGA Video Mode
BX=	Video mode	
	D0-D14=	Video mode number
	D15=	Clear memory flag

0= Clear video memory
1= Don't clear video memory

Output: AX= Status
All other registers are preserved.

4.4.5 Function 03h — Return Current Video Mode

This function returns the current video mode in BX Register. The format of VESA Video Mode numbers is described in Section 2 of this document.

Input: AH= 4Fh Super VGA support
AL= 03h Return current video mode

Output: AX= Status
BX= Current video mode number
All other registers are preserved.

NOTE: In a standard VGA BIOS, Function 0Fh (Read current video state) returns the current video mode in the AL Register. In D7 of AL Register, it also returns the status of the Memory Clear Bit (D7 of 40:87). This bit is set if the mode was set without clearing memory. In this Super VGA Function, the Memory Clear Bit will not be returned in BX Register since the purpose of the function is to return the video mode only. If an application must obtain the Memory Clear Bit, it should call VGA BIOS Function Fh.

4.4.6 Function 04h — Save/Restore Super VGA Video State

These functions provide a mechanism to save and restore the Super VGA video state. The functions are a superset of the three subfunctions under standard VGA BIOS Function 1Ch (Save/restore video state). The complete Super VGA video state (except video memory) should be saveable/restorable by setting the requested states mask (in the CX Register) to 000Fh.

Input: AH= 4Fh Super VGA support
AL= 04h Save/Restore Super VGA video state
DL= 00h Return save/restore state buffer size
CX= Requested states
D0= Save/restore video hardware state
D1= Save/restore video BIOS data state
D2= Save/restore video DAC state
D3= Save/restore Super VGA state

Output: AX= Status
BX= Number of 64-byte blocks to hold the state buffer
All other registers are preserved.

Input: AX= 4Fh Super VGA support
AL= 04h Save/Restore Super VGA video state
DL= 01h Save Super VGA video state
CX= Requested states (see above)
ES:BX= Pointer to buffer

Output: AX= Status

All other registers are preserved.

Input:

AH=	4Fh	Super VGA support
AL=	04h	Save/Restore Super VGA video state
DL=	02h	Restore Super VGA video state
CX=		Requested states (see above)
ES:BX=		Pointer to buffer

Output:

AX= Status
All other registers are preserved.

4.4.7 Function 05h — CPU Video Memory Window Control

This function sets or gets the position of the specified window in the video memory. The function allows direct access to the Hardware Paging Registers. To use this function properly, the software should use VESA BIOS Function 01h (Return Super VGA Mode information) to determine the size, location, and granularity of the windows.

Input:

AH=	4Fh	Super VGA support
AL=	05h	Super VGA video memory window control
BH=	00h	Select super VGA video memory window
BL=		Window number
	0=	Window A
	1=	Window B
DX=		Window position in video memory (in window granularity units)

Output:

AX= Status
See note below.

Input:

AH=	4Fh	Super VGA support
AL=	05h	Super VGA video memory window control
BH=	01h	Return super VGA video memory window
BL=		Window number
	0=	Window A
	1=	Window B

Output:

AX=	Status
DX=	Window position in video memory (in window granularity units)

See note below.

NOTE: This function is also directly accessible through a far call from the application. The address of the BIOS function may be obtained by using VESA BIOS Function 01h, return Super VGA Mode information. A field in the ModeInfoBlock contains the address of this function. Note that this function may be different among video modes in a particular BIOS implementation so the function pointer should be obtained after each set mode.

In the far call version, no status information is returned to the application. Also, in the far call version, the AX and DX Registers will be destroyed. Therefore if AX and/or DX Register must be preserved, the application must do so prior to making the far call.

The application must load the input arguments in BH, BL, and DX Registers (for set window),

but does not need to load either AH or AL Register to use the far call version of this function.

4.4.8 Function 06h — Set/Get Logical Scanline Length

This function sets or gets the length of a logical scanline. This function allows an application to set up a logical video memory buffer that is wider than the displayed area. Function 07h then allows the application to set the starting position that is to be displayed.

Input:	AH =	4fh	Super VGA Support
	AL =	06h	Logical Scanline Length
	BL =	00h	Select Scanline Length
	CX =		Desired Width in Pixels
Output:	AX =		Status
	BX =		Bytes Per Scanline
	CX =		Actual Pixels Per Scanline
	DX =		Maximum Number of Scanlines
Input:	AH =	4fh	Super VGA Support
	AL =	06h	Logical Scanline Length
	BL =	01h	Return Scanline Length
Output:	AX =		Status
	BX =		Bytes Per Scanline
	CX =		Actual Pixels Per Scanline
	DX =		Maximum Number of Scanlines

NOTE: The desired width in pixels may not be achievable because of VGA hardware considerations. The next larger value will be selected that will accommodate the desired number of pixels, and the actual number of pixels will be returned in CX Register. BX Register returns a value that, when added to a pointer into video memory, will point to the next scanline. For example, in a Mode 13h this would be 320, but in Mode 12h this would be 80. DX Register returns the number of logical scanlines based upon the new scanline length and the total memory installed and usable in this display mode. This function is also valid in text modes. In text modes, the application should determine the current character cell width through VESA Function 1 (or VGA BIOS Function 1BH), multiply that times the desired number of characters per line, and pass that value in the CX Register.

4.4.9 Function 07h — Set/Get Display Start

This function selects the pixel to be displayed in the upper-left corner of the display from the logical page. This function can be used to pan and scroll around logical screens that are larger than the displayed screen. This function can also be used to rapidly switch between two different displayed screens for double-buffered animation effects.

Input:	AH =	4fh	Super VGA Support
	AL =	07h	Display Start Control
	BH =	00h	Reserved and must be a '0'
	BL =	00h	
	CX =		First Displayed Pixel In Scanline
	DX =		First Displayed Scanline
Output:	AX =	Status	
Input:	AH =	4fh	Super VGA Support
	AL =	07h	Display Start Control
	BL =	01h	Return Display Start

Output:	AX =		Status
	BH =		00h Reserved and will be a '0'
	CX =		First Displayed Pixel In Scanline
	DX =		First Displayed Scanline

NOTE: This function is also valid in text modes. In text modes, the application should find out the current character cell width through VESA Function 1 (or VGA BIOS Function 1BH), multiply that times the desired starting character column, and pass that value in the CX Register. It should also multiply the current character cell height times the desired starting character row, and pass that value in the DX Register.

4.4.10 Function 08h — Set/Get DAC Palette Control

This function queries and selects the operating mode of the DAC Palette. Some DACs are configurable to provide 6 bits, 8 bits, or more of color definition per red, green, and blue primary color. The DAC Palette width is assumed to be reset to standard VGA 6 bits per primary during a standard or VESA Set Super VGA Mode (AX=4F02h) call.

Input:	AH=	4fh	Super VGA Support
	AL=	08h	Set/Get DAC Palette Control
	BL =	00h	Set DAC Palette Width
	BH=		Desired number of bits of color per primary (Standard VGA = 6)
Output:	AX=		Status
	BH=		Current number of bits of color per primary (Standard VGA = 6)
Input:	AH=	4fh	Super VGA Support
	AL=	08h	Set/Get DAC Palette Control
	BL =	01h	Get DAC Palette Width
Output:	AX=		Status
	BH=		Current number of bits of color per primary (Standard VGA = 6)

An application can determine if DAC switching is available by querying Bit D0 of the Capabilities field of the VgaInfoBlock structure returned by VESA Return Super VGA Information (AX=4F00h). The application can then attempt to set the DAC Palette width to the desired value. If the Super VGA is not capable of selecting the requested palette width, then the next lower value that the Super VGA is capable of selecting. The resulting palette width is returned.

4.4.11 Function 10h — Display Power Management Extensions

The following three functions are defined by VESA as a proposal for VBE/PM which is a software interface to DPMS: Report Display Power Management Capabilities, Set Power State, and Get Power State. These functions are included to specify the Cirrus Logic implementation of display power management. For questions regarding VESA, VBE/PM, or DPMS, please refer to the Video Electronics Standards Association. The contact information is at the beginning of this section.

Report VBE/PM Capabilites

Input:	AH=	4fh	Super VGA Support
	AL=	10f	VBE/PM Services

	BL=	00h Report VBE/PM Capabilities
	ES:DI=	Null pointer, must be 0000:0000 in version 1.0
Output:	AX=	Status
	BH=	Power saving state signals support by the controller: 1 = supported, 0 = not supported bit 0 STAND BY bit 1 SUSPEND bit 2 OFF bit 3 REDUCED ON (not supported by DPMS 1.0) bit 4-7 reserved
	BL=	VBE/PM Version number bits 7:4 Major Version number bits 3:0 Minor Version number

Set Display Power State

Input:	AH=	4fh Super VGA Support
	AL=	10h VBE/PM Services
	BL=	01h Set Display Power State
	BH=	Requested Power State 00h ON 01h STAND BY 02h SUSPEND 04h OFF 08h REDUCED ON (not supported by DPMS 1.0)
Output:	AX=	Status
	BH=	Unchanged

Get Display Power State

Input:	AH=	4fh Super VGA Support
	AL=	10h VBE/PM Services
	BL=	02h Get Display Power State
Output:	AX=	Status
	BH=	Display Power State 00h ON 01h STAND BY 02h SUSPEND 04h OFF 08h REDUCED ON (not supported by DPMS 1.0) bits 7:4 are reserved and should be ignored to ensure upward compatability.

5. EXTENDED MODES IN RAM

5.1 Extensions to the Save Area Table

The Cirrus Logic BIOS (standard versions) supports VGA-compatible modes along with a set of extended modes. OEMs may add new modes to the system, or redefine existing modes that are in the VGA ROM by manipulating the BIOS Save Area Table pointed to by 0040:00A8. This table is located in ROM after the system is booted. Any changes must be

made in a RAM copy. The Cirrus Logic BIOS has extended the definition of this table with 'negative' offsets that point to Cirrus Logic-BIOS-defined parameters. The compatible table, along with the defined extensions is listed below.

Offset	Type	Description
-14h	dword	Ptr to next negative offset table in linked list
-10h	word	Set to 04h if offset -14h is valid ptr, set to 00h if this link is the last in RAM. To block all ROM-based modes, set this field to 04h, and offset -14 to 0:0
-0Eh	word	Size of supplemental table
-0Ch	dword	Ptr to extended mode supplemental parameters
-08h	dword	Ptr to extended mode standard parameters
-04h	word	Number of extended video modes
-02h	word	'RV' identifier
00h	dword	Pointer to standard mode standard parameters
04h	dword	Dynamic saver area pointer (palette save area)
08h	dword	Alpha mode auxiliary character generator ptr
0Ch	dword	Graphics mode auxiliary character generator ptr
10h	dword	Secondary save pointer
14h	dword	Reserved and set to a zero
18h	dword	Reserved and set to a zero

5.2 BIOS Processing

The Cirrus Logic BIOS will determine what mode to select by processing a linked list of extended mode supplemental parameters tables, while evaluating several factors such as memory size, monitor type, memory clock, and the chip set that it is running on. Traveling from the top down, the BIOS will service a mode set request once all factors have been satisfied. A mode that has multiple horizontal frequencies must be sequentially ordered from the highest frequency at the top to the lowest on the bottom. This ensures that the BIOS will always set the correct mode for the given monitor type.

Modes can be added to the BIOS by manipulating the structure described above. The BIOS will always search for the RAM-defined links first to satisfy a mode set request. If it cannot find a mode based on the current configuration of the video subsystem, the ROM tables will then be scanned.

If new modes are to be added to the BIOS by defining them in RAM, a TSR need only modify the negative offsets described above (i.e., higher refreshes of previously defined modes, or entirely new mode numbers). If modes are to be redefined, special care must be taken. If a TSR modifies a particular frequency of a mode that has higher frequencies already defined in ROM, all frequencies must be redefined in RAM.

5.3 Extended Mode Supplemental Parameters

The table below describes what the BIOS expects in the supplemental structure discussed above.

Offset	Size	Description
00	byte	Video mode number
01	word	VESA video mode number
03	word	Horizontal resolution
05	word	Vertical resolution
07	byte	Bits per color
08	byte	Character width
09	byte	Character height
0A	byte	VESA memory model (Define in VESA Function 1)
0B	byte	VESA mode attributes (Defined in VESA Function 1)
0C	byte	Refresh Rate Fixup Index
0D	byte	Standard Parameter List Index
0E	byte	Reserved
0F	byte	Bit Pattern for Supported Chips
10	byte	Memory required, in 64K blocks
11	byte	Bit mask of monitors (3:0 Max Vert Res; 4:6 Req Freq; 7 Res)
12	byte	SR07, Extd Sequ Ctrl
13	byte	SR0F, DRAM Ctrl
14	byte	SR0E, VCLK3 numerator
15	byte	SR1E, VCLK3 denominator
16	byte	GR0B, Grfx Extensions
17	byte	CR19, Interlace end
18	byte	CR1A, Misc Ctrl
19	byte	CR1B, Display Ctrl
1A	byte	DACEXT, DAC Hidden Register
1B	byte	SR16: 70 ns Performance Timing
1C	byte	SR16: 60 ns Performance Timing

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CIRRUS LOGIC

Section 4
Software Update

CL-GD543X

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CL-GD543X

Application Alert – Software Update

Display Drivers and Utilities

User Interface Group
Cirrus Logic, Inc.

Scope and Applicability

This application alert presents information regarding utilities and software drivers support for the CL-GD543X family.

Related Documents

– Alpine VGA Family - CL-GD543X TRM – November 1993

Version 1.00 ***March 1994***

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Introduction

This document describes the features of the Display Driver and Utility Software Package for the GD543X VGA controllers, version 1.00. It provides general technical information about the package, which applications are supported and how to customize the installation procedures. The package will enable you to quickly go into production with thoroughly tested and competitive supporting software for the GD543X. It provides camera ready end-user documentation. The software, including an easy to use install program and procedures, is ready for shipment to the end-user.
The software diskettes contain both end-user utility software and display device drivers to take advantage of the extended capabilities of the GD543X.
The software utilities provide the user with a simple way to install, configure and operate the enhanced features of the GD543X.

Release 1.00 notes

- The linear addressing Windows 3.1 drivers used in this release are configured by the installation utility to locate the linear frame buffer at 64MB. The CIRRUS LOGIC VL Bus demo card uses a 64MB address and is compatible with these drivers. Note that ISA Bus designs are limited to 16MB and are not supported by this installation.
- Please note that the 8x14 font is not included in the BIOS so that room for extended modes, additional refresh rates, and VESA functionality could be included. When programs use the BIOS to write 8x14 characters (in mode 55h, for example), the 8x16 font is used with the bottom two scan lines deleted. This results in truncation of characters with descenders such as "y" and "j". Also note that programs which request that the BIOS return a pointer to the 8x14 ROM font, then directly write characters to the screen, will be given a pointer to the 8x16 font. Programs such as DOSSHELL and Norton use this for graphics 25 and 34 line modes. The utility TSRFONT will load a RAM copy of the 8x14 font, and will restore normal operation to programs which use the 8x14 font in the above two methods. The TSRFONT utility is installed from the DOS Drivers & Utilities disk by selecting the GD543X utilities selection. Users who frequently use modes requiring the 8x14 font should place this utility in their AUTOEXEC.BAT file.

Problems fixed since last BETA release

- The CLMode center adjust doesn't work in video modes 58h and higher. The CENTER.COM file looks changed, the date, size and time is indeed different when you reboot, but it still doesn't save any new screen savings. This problem has been fixed.
- In WinMode, when 1280x1024x16 million colors and any other resolution is selected, the 1280x1024 resolution is not grayed out on the 4M board. This problem has been fixed.
- In Windows grayed out text disappears at 256 colors when the background is gray. This problem has been fixed.
- Windows drivers in 256 colors for OS/2 for Windows when used with 4MB of DRAM, several problems are observed with BitBLT and cursor. This problem has been fixed.
- Select a windowed DOS session, set mode 0, 1, 2, 4, 5, or 6. The display is corrupted. This problem has been fixed.
- In Windows, with several open applications, the display gets corrupted after switching among applications (with ALT-TAB or dragging boxes). Examples of such applications are PageMaker 5.0, Microsoft Works v2.0, and WFW v6.0. The problem appears with the CIR.DRV in color depths of 256 or above. This problem has been fixed.

- In Windows, when using mode 6C (1280x1024x16 colors) at 60Hz refresh, two mouse pointers are present. This mode exceeds the capabilities of the GD5434. When mode 6C is selected, an 87 Hz interlaced refresh will be used. Mode 6D (1280x1024x256 colors) should be used when a 60 Hz refresh is desired. WinMode will correctly select the lower refresh rate when mode 6C is selected.
- When running After Dark for Windows v2.0, two modules display "snow". This problem exists with 256 colors only. The modules are "Satori" and "Kaleidoscope". This problem has been fixed.
- OS/2 2.1 - the files on the diskette are packed using different version of the pack/unpack utility. This makes installation impossible. This problem has been fixed.
- AutoCAD v12 does not display a selection for 800x600x16 million colors. In addition, the selections for 1024x768x64k colors and 1280x1024x256 colors do not work correctly. This problem has been fixed.
- AutoCAD is missing 2 modes for 4 MB boards. Missing modes are 1280x1024x64K, and 1280x1024x32K. This problem has been fixed.
- There are generic drivers available for MicroStation. There are no CIRRUS LOGIC drivers available yet.
- In Microsoft Visual C++, the buttons which are supposed to be grayed out (in App. Studio, for example), are coming up green in 16 million color modes. This problem has been fixed.

Utility Issues:

- The SetRES utility has been replaced with a new program called WinMode. WinMode has all the capabilities of SetRES and has added the following functions:
  - Select monitor refresh rates for all resolutions in Windows 3.1.
  - Adjust memory available for font caching.

The main dialog is the same as that in the installation utility. This will make it easier for users to become familiar with its operation.

Known problems in Release 1.00

- While using 800x600x16 million colors in AutoCAD, part of the right screen is missing.
- In AutoCAD release 12, when using the 16 color drawing modes, after erasing a drawing, several dots are not correctly erased from the display. Selecting REGEN will correctly redraw the screen at this point.

Installation Utility

The INSTALL.EXE program on diskette one will copy the user specified files (device drivers or utilities) to the appropriate directory on the user's hard disk. The user may specify any disk drive as the destination. Also, for each display driver or utility, the user may specify the destination directory. The user must then configure the application to use the driver.
The DOS Installation Utility may be modified to add OEM specific files to the installation process. You may choose to delete some files from the CIRRUS LOGIC supplied driver diskettes. If you choose to delete files from the diskettes, you must alter the Installation Utility to not reference the deleted files.
Please see the section 'Modifying the driver and utility package' for more information about changing the installation procedures.
A separate INSTALL.EXE program is included on the Windows 3.1 driver disk, and is used to install the Windows 3.1 drivers and utilities.

Supported Display Drivers

The following environments and/or applications are supported in this package.

Product Name	Supported Resolutions
AutoCAD v11, v12	640x480, 800x600, 1024x768, 1280x1024 - 16 colors
	640x480, 800x600, 1024x768, 1280x1024 - 256 colors
	640x480, 800x600, 1024x768 - 32,768 colors
	640x480, 800x600, 1024x768 - 65,536 colors
	640x480, 800x600, 1024x768 - 16.8 million colors
Autoshade v2	640x480, 800x600, 1024x768, 1280x1024 - 256 colors
	640x480, 800x600, 1024x768 - 32,768 colors
	640x480, 800x600, 1024x768 - 65,536 colors
	640x480, 800x600, 1024x768 - 16.8 million colors
3D Studio v1, v2	640x480, 800x600, 1024x768, 1280x1024 - 256 colors
	640x480, 800x600, 1024x768 - 32,768 colors
	640x480, 800x600, 1024x768 - 65,536 colors
	640x480, 800x600, 1024x768 - 16.8 million colors
MS Windows v3.1	640x480, 800x600, 1024x768, 1280x1024 - 16 colors
	640x480, 800x600, 1024x768, 1280x1024 - 256 colors
	640x480, 800x600, 1024x768, 1280x1024 - 65,536 colors
	640x480, 800x600, 1024x768 - 16.8 million colors
Windows NT	640x480, 800x600, 1024x768, 1280x1024 - 16 colors
	640x480, 800x600, 1024x768, 1280x1024 - 256 colors
Lotus 123 v2.x	132x25 - 16 (text), 132x43 - 16 (text), 800x600 - 16 colors
Lotus 123 v3.x	800x600, 1024x768 - 16 colors
OS/2 v2.1	640x480, 800x600, 1024x768 - 256 colors
WordPerfect v5.1	132x25 - 16 (text), 132x43 - 16 (text), 800x600, 1024x768 - 16 colors
WordStar v5.5-v7.0	800x600, 1024x768 - 16 colors
MS Word v5.X	132x25 - 16 (text), 132x43 - 16 (text), 800x600 - 16 colors

BIOS and Utilities

User Interface Group
Cirrus Logic, Inc.

Scope and Applicability

This application alert presents information regarding utilities and software drivers support for the CL-GD543X family.

Related Documents

– Alpine VGA Family - CL-GD543X TRM – November 1993

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Introduction

This document describes the features of the VGA BIOS and Utility Software Package for the GD543X VGA controller, version 1.00A. This document provides general technical information about the package and the release.

Apart from these release notes, the release package contains the following items:

- External Software Specification (which describes the extended Interrupt 10h function calls)
- OEM System Integration Tool documentation (which allows the OEM to customize the binary image of the BIOS without making source code changes)
- License Agreements
- BIOS Testing Procedures
- Sample Product Deficiency Report forms (used to report software problems)
- Registration form
- Software Diskettes

Problems fixed in v1.00A

The following errata items have been corrected by the 1.00A BIOS release.

- DPMS support - recovery from power savings modes is supported while in direct color modes.
- The PCI data structure class has been corrected at offset 1BD and 1BF. These bytes have been swapped to conform to little-endian support requirements.

Notes for v1.00A

- Please note that the 8x14 font is not included in the BIOS so that room for extended modes, additional refresh rates, and VESA functionality could be included. When programs use the BIOS to write 8x14 characters (in mode 55h, for example), the 8x16 font is used with the bottom two scan lines deleted. This results in truncation of characters with descenders such as "y" and "j". Also note that programs which request that the BIOS return a pointer to the 8x14 ROM font, then directly write characters to the screen, will be given a pointer to the 8x16 font. Programs such as DOSSHELL and Norton use this for graphics 25 and 34 line modes. The utility TSRFONT will load a RAM copy of the 8x14 font, and will restore normal operation to programs which use the 8x14 font in the above two methods. The TSRFONT utility is installed from the DOS Drivers & Utilities disk by selecting the GD543X utilities selection. Users who frequently use modes requiring the 8x14 font should place this utility in their AUTOEXEC.BAT file.

Problems fixed since last release

- Mode 76h with 1MB should not be available.
- Mode 65h and 67h with 72 and 75Hz refresh should not be available with 1MB.
- Mode 6Ch with 60 Hz refresh should not be available as it exceeds the CL-GD5434 specification
- The following procedure will leave lines on the screen - set mode 4, then execute DIR, then execute CLS. This problem has been fixed.
- Setting a monitor type does save the new monitor type in EEPROM. It is necessary to set the monitor type each time the system is restarted. In addition, the monitor type is not saved across a warm boot. This creates a problem with programs such as SVGA (OS/2 installation). This problem has been fixed.

- On a 1Mbyte VESA VL configuration, CLMode reports 256 Kbytes. This problem has been fixed.
- VESA Power Management problem - character corruption in text modes has been observed when switching to ON from SUSPEND or OFF. This problem has been fixed.

Known problems in Release 1.00A

- VPIC - when using 800x600x16 million colors, the picture is displayed in 256 colors.
- White border with mode D. The following procedure will leave a white border on the screen. Set mode D, then execute test program BOX.EXE, then execute DIR. This is a problem with the CL-GD5434. There is no known work-around at this time

License requirement

To distribute the VGA BIOS and utilities to end-users, you must obtain a License for Distribution of Executable Software from CIRRUS LOGIC. Such license is required for each different CIRRUS LOGIC VGA product that you intend to ship CIRRUS LOGIC software with. If you don't have a valid license, you may evaluate the software, but you may not distribute, duplicate or sublicense the software.

Please refer to Section Six of this package, License Agreements, for blank copies of the License Agreement.

Quality Control

The VGA BIOS and Utility Package has been thoroughly tested for bugs and compatibility problems. The CIRRUS LOGIC Software Quality Assurance Group follows a rigorous and extensive testplan to ensure the highest quality level possible.

Should any problems arise with the package, please report those issues to CIRRUS LOGIC on the Problem Description Report forms, available in section seven of this package.

Selecting BIOS type

The VGA BIOS and Utility Package contains three different directories of BIOS binary images. Each directory will contain a VL Bus image which can execute from either C000 or E000 segments, and a PCI Bus image. The BIOS binary are images in the ADAPTER directory are designed to work on an adapter card and do not contain any CGA or MDA (Hercules monochrome) support. The BIOS binary images in the other directories (MB-46E8 and MB-3C3) are functionally equivalent to an IBM motherboard VGA BIOS.

The adapter BIOS supports the standard adapter VGA sleep mechanism at 46E8h. The mother board BIOS is provided in two versions. The first supports the 46E8h (adapter) sleep mechanism. The second uses the 3C3h (motherboard) sleep mechanism.

Each of these BIOS types contain a number of separate images for different applications. These BIOS files are located on the diskette included in this package. See the last page of this document for the appropriate file names.

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Section 5

Collateral Documentation

Collateral Documentation

Revision 1.2

This book is released as of April 5, 1994. The following additional information regarding the CL-GD543X family is available as of this date.

Alpine VGA Family- CL-GD543X Technical Reference Manual: 385439-003: March 1994
Alpine Family VGA GUI Accelerators Databook: (Reprinted from Chapter 3 of the TRM): March 1994
Alpine Family VGA GUI Accelerators Product Bulletin: 355439-003 (Included in Databook): March 1994
BIOS Release Kit: GDB543X-X-B100P, February 1994
Driver Release Kit: GDB543X-X-D100P, February 1994

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Section 6

CL-GD5430 Erratas

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Section 7

CL-GD5432 Erratas

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Section 8

CL-GD5434 Errata

CL-GD5434 Rev AE (Production A) Errata

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The following two errata have been noted on PCI Bus configuration of the CL-GD5434 Rev AE (production A) silicon. These items will be fixed in the next revision (Rev AF) of silicon.

1• PCI Bus: Reads to B800:0 fail when memory is disabled

Memory reads in the range B800:0 through BFFF:F cause the system to hang if memory is disabled and the CL-GD5434AE is configured for PCI bus.

Workaround: Always use the Cirrus Logic, Inc. supplied BIOS as an adapter BIOS or Motherboard BIOS to initialize the CL-GD5434 before any display memory reads are executed.

2• PCI Bus: Memory-mapped I/O

Memory-mapped I/O fails when the CL-GD5434AE is configured for PCI bus and operating in a system where the FRAME# during memory write cycles is two clocks wide.

Workaround: Depending on the width of FRAME#, different drivers must be used.

Table 1. Driver Summary

FRAME# Width	Example Platform	Drivers	Note
1 Clock	INTEL Mercury Pentium	PCI Linear Addressing for Intel Pentium	Burst must be Disabled
2 Clocks	INTEL Saturn '486	PCI Non-Memory Mapped I/O	e.g. 5428 Drivers

The following three errata have been noted in all host bus configurations of the CL-GD5434 Rev AE (production A). These items will not be fixed in Rev AF silicon.

3• BitBLT: Color expand with Extended RAS*

Color expand (without pattern copy) BitBLT operations fail when extended RAS* (7 MCLK)is enabled.

Workaround: Only 6 MCLK RAS* can be used. Verify no pulldown resistor is installed on MD57 (CF9).

4• Hardware Graphics Cursor with Double Clocking Modes

The hardware graphics cursor does not work properly in double clocking modes. This applies to the 1280 x 1024 256-color non-interlaced mode. This mode requires a pixel clock of 110 MHz.

Workaround: The Cirrus Logic Inc. supplied drivers do not use this function in these modes.

5• BitBLT: Pattern Copy without Color Expand in 32 Bit/Pixel Modes

Pattern Copy BitBLT without Color Expand does not function correctly in any 32 bit/pixel mode.

Workaround: The Cirrus Logic, Inc. supplied drivers do not use this function.

The following three errata have been noted in all host bus configurations of the CL-GD5434 Rev AE (Production A). These items represent deviations from the specification but have no impact on performance. They are noted for completeness only.

6• Readback Of Registers written with Memory-mapped I/O

When any of the following registers are written with memory-mapped I/O, they cannot be read back: GR0, GR1, GR10, GR11.

Workaround: The Cirrus Logic, Inc. supplied drivers do not attempt to read these registers if they have been written with memory-mapped I/O.

7• Readback of Registers GR22, GR23

Registers GR22, GR23 cannot be read.

Workaround: The Cirrus Logic, Inc. supplied drivers do not attempt to read these registers.

8• BitBLT: Screen to System

Screen to system BitBLT operations fail when the CL-GD5434AE is configured for VESA or PCI bus.

Workaround: The Cirrus Logic, Inc. supplied drivers do not use Scr-Sys BitBLTs.

Items 4, 5, 6, 7, 8 should be noted by Software Developers.

CL-GD5434 Rev AF (Production B) Errata

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The following errata have been noted on the PCI configuration of the CL-GD5434 Rev AF (Production B).

1• System to Screen BitBLT on PCI at 25 MHz

System to Screen BitBLT on PCI platforms operating at or below 25 MHz fails.

Workaround: The Cirrus Logic Inc. supplied drivers do not use this function.

2• PCI Configuration Registers 32 Bits Only

If a PCI Configuration Register is written with a BYTE or WORD I/O cycle, the portion of the register which is not written is cleared to zero. This effects PCI registers 04h, 10h, and 30h.

Workaround: The third party software vendors have agreed to modify their POST routines to avoid this problem. See Application Alert 7 for details.

3• PCI Non-contiguous bytes

The PCI bus allows DWORD writes to occur in which multiple, non-contiguous bytes are enabled. As an example, BE1 and BE3 may be active, while BE2 is not active. When such a write occurs, the CL-GD5434 AF will fail to return TRDY, hanging the system.

Workaround: Currently available PCI core logic chip sets do not support the byte merge feature. In the future, chip sets which do support the feature will be available. We are advising our customers to disable the feature. See Application Alert 8 for details.

The following three errata have been noted on all host bus configurations of the CL-GD5434 Rev AF (Production B).

4• BitBLT: Color expand with Extended RAS*

Color expand (without pattern copy) BitBLT operations fail when extended RAS* (7 MCLK)is enabled.

Workaround: Only 6 MCLK RAS* can be used. Verify no pulldown resistor is installed on MD57 (CF9).

5• Hardware Graphics Cursor with Double Clocking Modes

The hardware graphics cursor does not work properly in double clocking modes. This applies to the 1280 x 1024 256-color non-interlaced mode. This mode requires a pixel clock of 110 MHz.

Workaround: The Cirrus Logic Inc. supplied drivers do not use this function in these modes.

6• BitBLT: Pattern Copy without Color Expand in 32 Bit/Pixel Modes

Pattern Copy BitBLT without Color Expand does not function correctly in any 32 bit/pixel mode.

Workaround: The Cirrus Logic, Inc. supplied drivers do not use this function.

The following three errata have been noted in all host bus configurations of the CL-GD5434 Rev AF (Production B). These items represent deviations from the specification but have no impact on performance. They are noted for completeness only.

7• Readback Of Registers written with Memory-mapped I/O

When any of the following registers are written with memory-mapped I/O, they cannot be read back: GR0, GR1, GR10, GR11.

Workaround: The Cirrus Logic, Inc. supplied drivers do not attempt to read these registers if they have been written with memory-mapped I/O.

8• Readback of Registers GR22, GR23

Registers GR22, GR23 cannot be read.

Workaround: The Cirrus Logic, Inc. supplied drivers do not attempt to read these registers.

9• BitBLT: Screen to System

Screen to system BitBLT operations fail when the CL-GD5434AF is configured for VESA or PCI bus.

Workaround: The Cirrus Logic, Inc. supplied drivers do not use Scr-Sys BitBLTs.

CL-GD5434 Rev AJ (Production C) Errata

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Summary

The CL-GD5434-HC-AJ (production revision C) is identical to the CL-GD5434-HC-AF (production revision B), except that the byte or word write to PCI configuration registers problem has been fixed. This is documented as Erratum 2 in the April 4, 1994 AF Errata.

The following errata have been noted on the PCI configuration of the CL-GD5434 Rev AJ (Production C).

1• System to Screen BitBLT on PCI at 25 MHz

System to Screen BitBLT on PCI platforms operating at or below 25 MHz fails.

Workaround: The Cirrus Logic Inc. supplied drivers do not use this BLT operation.

2• PCI Non-contiguous bytes

The PCI bus allows DWORD writes to occur in which multiple, non-contiguous bytes are enabled. As an example, BE1 and BE3 may be active, while BE2 is not active. When such a write occurs, the CL-GD5434 AF will fail to return TRDY, hanging the system.

Workaround: Currently available PCI core logic chip sets do not support the byte merge feature. In the future, chip sets which do support the feature will be available. We are advising our customers to disable the feature. See Application Alert 8 for details.

The following three errata have been noted on all host bus configurations of the CL-GD5434 Rev AJ (Production C).

3• BitBLT: Color expand with Extended RAS*

Color expand (without pattern copy) BitBLT operations fail when extended RAS* (7 MCLK)is enabled.

Workaround: Only 6 MCLK RAS* can be used. Verify no pulldown resistor is installed on MD57 (CF9).

4• Hardware Graphics Cursor with Double Clocking Modes

The hardware graphics cursor does not work properly in double clocking modes. This applies to the 1280 x 1024 256-color non-interlaced mode. This mode requires a pixel clock of 110 MHz.

Workaround: The Cirrus Logic Inc. supplied drivers do not use this function in these modes.

5• BitBLT: Pattern Copy without Color Expand in 32 Bit/Pixel Modes

Pattern Copy BitBLT without Color Expand does not function correctly in any 32 bit/pixel mode.

Workaround: The Cirrus Logic, Inc. supplied drivers do not use this function.

The following three errata have been noted in all host bus configurations of the CL-GD5434 Rev AJ (Production C). These items represent deviations from the specification but have no impact on performance. They are noted for completeness only.

6• Readback Of Registers written with Memory-mapped I/O

When any of the following registers are written with memory-mapped I/O, they cannot be read back: GR0, GR1, GR10, GR11.

Workaround: The Cirrus Logic, Inc. supplied drivers do not attempt to read these registers if they have been written with memory-mapped I/O.

7• Readback of Registers GR22, GR23

Registers GR22, GR23 cannot be read.

Workaround: The Cirrus Logic, Inc. supplied drivers do not attempt to read these registers.

8• BitBLT: Screen to System

Screen to system BitBLT operations fail when the CL-GD5434AF is configured for VESA or PCI bus.

Workaround: The Cirrus Logic, Inc. supplied drivers do not use Scr-Sys BitBLTs.

CIRRUS LOGIC

Section 9

Documentation Errata

CL-GD543X Technical Reference Manual: Update to the March 1994 TRM 385439-003

User Interface Group
Cirrus Logic, Inc.

Scope and Applicability

This Application Alert presents information not found in previous documentation for the CL-GD542x. It is intended to be used in conjunction with applicable CL-GD542x literature

Related Documents

– *TrueColor VGA Family - CL-GD543x Technical Reference Manual - March 1994*

April 1994

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Data Book, Page 73 (Reprinted as Chapter 3 of TRM)

The formula for t21 and t22 in Table 7-24 are incorrectly stated. They should be corrected as indicated in the following table..

Symbol	Parameter	Stated Min	Corrected Min	Stated Max	Corrected Max
t21	tDS: Write Data Setup to CAS* Active	1T + 0.5 ns	1T- 2 ns	1T + 5ns	1T + 2 ns
t22	tDH: Write Data Hold from CAS* Active	1T - 8 ns	1T + 1ns	1T - 0.5 ns	-

Chapter 9, page 22

The bit name for bit 0 should be Shadow DAC Writes on VESA-VL Bus.

Chapter 9, page 23

The bit name for bit 0 should be Shadow DAC Writes on VESA-VL Bus.

Chapter 9, page 38

1. The bit name for bit 4 should be System Level Power Management
2. A bit description should be added for bit 4:

4 **System Level Power Management:** If this bit is programmed to a '1', host access to the display memory is disabled (see MISC[1]) and screen refresh is disabled (see SR1[5]). This bit must be programmed to a '1' prior to programming GRE[3] to a '1' and must be programmed to a '0' after programming GRE[3] to a '0'. The MCLK and VCLK VCO's continue to operate at their programmed frequencies, but consume very little power.

Chapter 9, following page 44

Add a new register description: GR18 - also in Table 9-1 and section 6 of data book
GR18: Extended DRAM Controls (CL-GD5430 Only)
I/O Port Address: 3CF
Index: 18

Bit	Description	Reset State
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2	Extended Read Following Write Timing	0
1	Decreased Write Following Read Timing	0
0	Decreased WE Active Delay	0

This register contains bits for DRAM timing controls. This register is reset to '0'. This register should be programmed to '3' at POST time and should remain unchanged thereafter. This register is implemented on the CL-GD5430 only.

Bit	Description
7:3	Reserved
2	**Extended Read Following Write Timing**: If this bit is programmed to '0', there will be a one MCLK delay of a read CAS* that follows a write CAS*. If this bit is programmed to a '1', there will be a two MCLK delay of a read CAS* that follows a write CAS*.
1	**Decreased Write Following Read Timing**: If this bit is programmed to a '0', there will be three MCLK delay of a write CASE* that follows a read CAS*. If this bit is programmed to a '0', there will be a two MCLK delay of a write CAS* that follows a read CAS*.
0	**Decreased WE Active Delay:** If this bit is programmed to a '0', there will a two MCLK delay of WE* following a read cycle. If this bit is programmed to a '1', there will be a one MCLK delay of WE* following a read cycle.

Chapter 10, page 46,47

The 1Ch functions incorrectly state that AH should be programmed to 1Ah. These correct value is 1Ch.

Appendix B8, page 4

Add a sentence to section 6 Using MCLK as VCLK:
See SR1F.

Appendix D8, page 10

Section 6. The fourth sentence begins "If GR30[2] is programmed....". This should be "If GR30[3] is programmed...".