CIRRUS LOGIC

CL-SH250

Data Sheet

FEATURES

- Selectable open-drain or push-pull SCSI drivers
- Fast microcontroller interface—16 MHz 8051, 12 MHz 68HC11, etc.
- NRZ data rates up to 24 Mbits/second
- Selectable 16-bit CRC/32-bit ECC/56-bit ECC polynominal with fast hardware correction circuitry†
- Support of concurrent non-interleaved disk transfer and SCSI bus transfer
- Interrupt or polled microcontroller interface
- Direct buffer memory addressing up to 64K bytes static RAM
- Dual port circular buffer memory control with access priority resolver
- User-modifiable format sequencer with a RAM-based Writable Control Store (WCS – 31 x 4 bytes)
- Microcontroller access to eight external switch settings
- Can be used with ST506/412, ST412HP, ESDI, and SMD disk interfaces
- Support of buffer memory throughput up to 6 Mbytes/second
- SCSI DMA handshake logic that handles asynchronous transfer at rates up to 3 Mbytes/second
- Low-power CMOS technology in a 100-pin QFP

Integrated SCSI Disk Controller

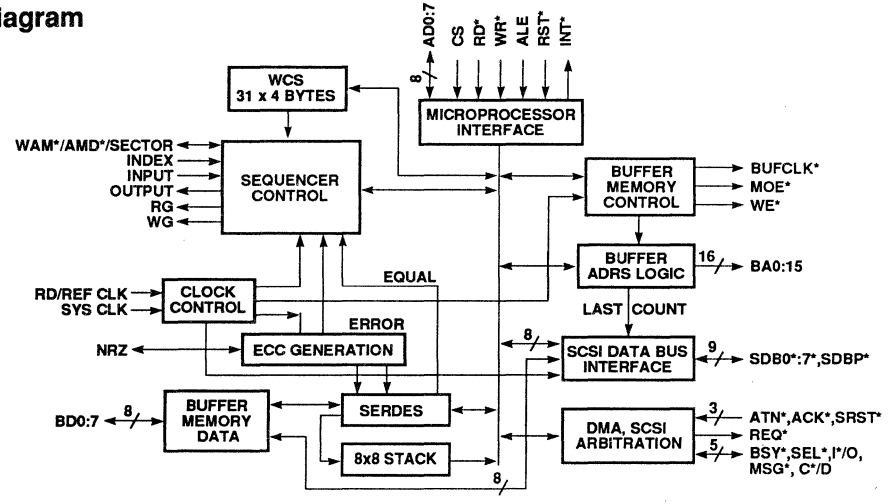
— for low-cost systems —

OVERVIEW

The highly integrated CL–SH250 provides a large portion of the hardware necessary to build a SCSI Winchester disk controller. The controller includes an advanced Winchester disk formatter, a dual-port Buffer Manager, and extensive hardware support (including 48 mA drivers). Also, disk data rates up to 24 Mbits/second are supported.

The CL-SH250 disk formatter consists of a serializer/deserializer, a flexible RAM-based sequencer, and CRC/ECC generation circuitry. Industry-standard 16-bit CCITT-CRC, 32-bit Fire Code, and computer-generated 56-bit ECC polynomials are all supported in hardware. *(cont. next page)*

Functional Block Diagram



† U.S. Patents No.4,293,783 and No.4,979,173

OVERVIEW (cont.)

The ECC circuitry includes hardware correction assist logic to speed the correction process. The CL-SH250 buffer manager will control up to 64K bytes of SRAM buffer memory as a dual port circular buffer.

The CL-SH250 works with a local microcontroller which has a multiplexed address and data bus similar to that provided by the Intel® 8051 family of microcontrollers and the Motorola® 68HC11. It is easily adaptable to other microcontroller I/O techniques and supports both interrupt and polled processor interfaces. Maskable interrupts and status bits include 13 disk and host interface events.

ADVANTAGES

Unique Features	*Benefits*
■ *31 Words of Writable Control Store*	Provides flexibility for the sequencer to perform various disk controller operations.
■ *Computer generated 56-bit ECC polynomial embedded in hardware*	Supports single-burst error correction up to 23 bits. Probability of miscorrection as low as 10^{-14} per bit corrected.
■ *Fire Code 32-bit ECC polynomial embedded in hardware*	Supports single-burst correction up to 11 bits.
■ *ECC circuitry provides logic to speed the correction process*	Provides hardware correction with minimal MPU intervention. Can correct within a single sector time.
■ *Data rate up to 24 Mbits/second*	Can be used in high-performance applications.
■ *Maskable microcontroller interrupt capability*	Relieves the microcontroller from polling and thus enables it to perform other tasks. Provides status information to the microcontroller when interrupts are disabled.
■ *Sector Size Counter*	Reads and writes sectors larger than 512 bytes without microcontroller intervention.
■ *Directly accesses 64K bytes of SRAM*	Requires no external hardware for buffer memory sizes up to 64K bytes.
■ *Provides microcontroller access to eight external switch settings*	Enables the microcontroller to read SCSI ID, SCSI Parity Enable or other switch-settable information.
■ *3 Mbytes/second SCSI transfer rate*	Allows fast data transfer to the host.
■ *Direct I/O path, with REQ/ACK handshake, between the microcontroller and the SCSI bus during disk/buffer memory transfer*	Ensures that the microcontroller is never locked off from the SCSI bus.
■ *Provides on-chip, SCSI-specified, 48 mA open-drain drivers*	Eliminates external transceiver ICs.
■ *Provides programmable, on-chip push-pull drivers for SCSI bus*	Can eliminate termination networks in some cabling configurations.
■ *Pin-out organized for optimum board layout efficiency*	Simplifies board layout, reduces need for multi-layered board.

CIRRUS LOGIC

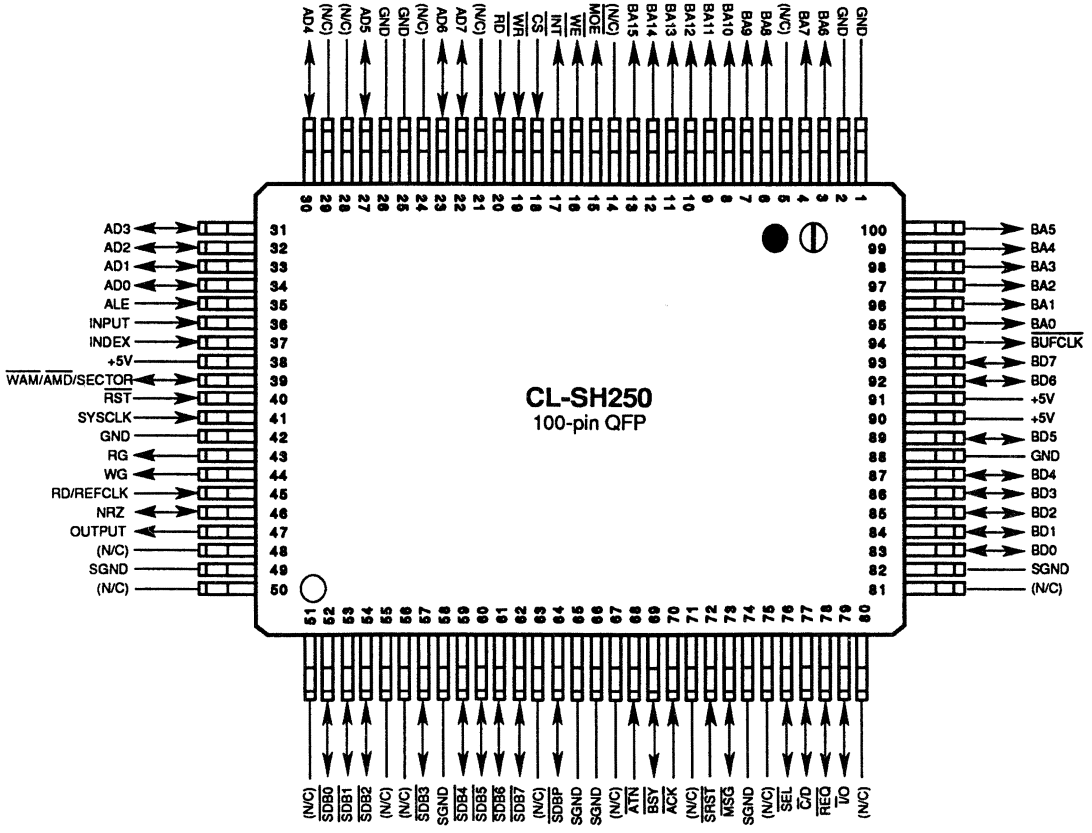
CONTENTS

TABLES

1. PIN INFORMATION

1.1 Pin Diagram for the 100-Pin Quad Flat Pack (QFP)

The CL-SH250 is available only in a 100-pin Quad Flat Pack (QFP). The package's pinouts diagram is shown below. All unused inputs must be tied to their inactive state to VCC or GND, respectively.



1.2 Pin Assignments

The following conventions are used on the pin assignment tables. An asterisk (*) denotes a negative true signal. An (I) indicates an input pin. An (O) indicates an output pin. An input/output pin is indicated by (I/O). Open drain output pins are indicated by (OD). All unused inputs must be tied to their inactive state to VCC or GND, respectively.

BUFFER MEMORY INTERFACE PINS

SYMBOL	PIN NUMBER QFP	TYPE	DESCRIPTION
BD7:0	83-87, 89, 92-93	I/O	**BUFFER MEMORY DATA BUS**: These eight signals are Bits 0-7 of the 8-bit parallel data lines to/from the buffer memory.
BUFCLK*	94	O	**BUFFER CLOCK**: This signal defines buffer memory access cycles. During disk access, this clock is derived from RD/REF CLK (Pin 45). Otherwise, it is derived from the SYSCLK input (Pin 41). The relationship of both these clocks to BUFCLK* is controlled by the contents of the CLOCK/SYNC CONTROL Register (7FH).
BA0:15	95-100, 3-4, 6-13	O	**BUFFER MEMORY ADDRESS LINES**: These 16 signals provide up to 64K of buffer memory addressing capability.
MOE*	15	O	**MEMORY OUTPUT ENABLE**: This signal is asserted low when a buffer memory operation is active.
WE*	16	O	**WRITE ENABLE**: This signal is asserted low when a buffer memory Write operation is active.

1.2 Pin Assignments *(cont.)*

MICROCONTROLLER INTERFACE PINS

SYMBOL	PIN NUMBER QFP	TYPE	DESCRIPTION
INT*	17	O, OD	**LOCAL MICROCONTROLLER INTERRUPT**: This signal is programmable for either push-pull or open-drain output circuitry.
CS	18		**CHIP SELECT**: This signal must be asserted to access the CL–SH250.
WR*	19	I	**WRITE**: When the WR* signal (Pin 19) is asserted low and the CHIP SELECT signal (Pin 18) is asserted high, the data on the Address/Data lines will be written in to the specified register.
RD*	20	I	**READ**: When the RD* signal (Pin 20) is asserted low and the CHIP SELECT signal (Pin 18) is asserted high, the data from the specified register is read on to the Address/Data lines.
AD7:0	22-23, 27, 30-34	I/O	**LOCAL MICROCONTROLLER ADDRESS / DATA**: These are tristate Address/Data lines which interface with a multiplexed microcontroller Address/Data bus.
ALE	35	I	**ADDRESS LATCH ENABLE**: This control signal latches the address on the Address/Data lines on the falling edge of this signal.

1.2 Pin Assignments *(cont.)*

MICROCONTROLLER INTERFACE PINS (cont.)

SYMBOL	PIN NUMBER QFP	TYPE	DESCRIPTION
RST*	40	I	**RESET**: Asserting this signal stops all operations within the chip and deasserts the READ GATE (Pin 43) and the WRITE GATE signals (Pin 44). All I/O signals are set to a high-impedance state--the BUFFER MEMORY DATA BUS (Pins 83-87, 89, 92-93), AD7:0 (Pins 22-23, 27, 30 34), the WAM*/AMD*/SECTOR signal (Pin 39), the NRZ signal (Pin 46), the SCSI DATA BUS (Pins 52-54, 57, 59-62), the SCSI DATA BUS PARITY signal (Pin 64), the SCSI BUSY signal (Pin 69), the SCSI MESSAGE signal (Pin 73), the SCSI SELECT signal (Pin 76), the SCSI COMMAND/DATA signal (Pin 77), the SCSI INPUT/OUTPUT signal (Pin 79), and the SCSI REQUEST signal (Pin 78). When this signal is asserted low, the BUFFER MANAGER RESET bit (Register 59H, Bit 0) and the FORMATTER RESET bit of the ECC CONTROL (Register 71H, Bit 5) are set, and the following bits are reset: the ALTERNATE BRANCH SELECTION MODE ENABLE bit (Register 77H, Bit 6), and Bits 0-6 of the DISK INTERRUPT STATUS Register (41H/61H). Assertion of this signal resets the following registers: the READ ADDRESS POINTER (RAP) Registers (5AH and 5BH), the WRITE ADDRESS POINTER (WAP) Registers (5CH and 5DH), the SHADOW LATCH Register (4DH), the WAM CONTROL Register (7BH), the SYNC PATTERN Register (7CH), and the CLOCK/SYNC CONTROL Register (7FH). When this signal is asserted low, the ECC STATUS Registers (73H-76H) and the SCSI STOP POINTER (Registers 5EH and 5FH) are set.

DISK INTERFACE PINS

SYMBOL	PIN NUMBER QFP	TYPE	DESCRIPTION
INPUT	36	I	**INPUT PIN**: This signal is available to synchronize the Sector Format Sequencer to an external event using a branch input to the Sequencer. The state of this signal is sampled by reading the SEQUENCER INPUT bit (Bit 4) of SCSI INFORMATION PHASE CONTROL (Register 7EH).
INDEX	37	I	**INDEX** : This is input for the INDEX pulse received from the disk drive. The rising (leading) edge of the INDEX pulse sets the INDEX PAST bit (Bit 0) of the OPERATION CONTROL/ STATUS Register (7AH).
WAM* / AMD*/ SECTOR	39	I/O	**WRITE ADDRESS MARK/ADDRESS MARK DETECT/SECTOR**: This pin can be configured to operate in Hard or Soft Sector mode by initializing the HARD/SOFT*SECTOR MODE CONTROL bit (Bit 7) of the FORMATTER/BUFFER MANAGER MODE SELECTION Register (77H). The default is Soft Sector mode. In Soft Sector mode, when the READ GATE signal (Pin 43) is asserted, a low-level input on this bit indicates Address Mark detected. In Hard Sector mode, this is the input for the SECTOR pulse. The rising (leading) edge of the SECTOR pulse sets the SECTOR PAST bit (Register 7AH, Bit 1).
SYSCLK	41	I	**SYSTEM CLOCK**: This is a 2.5 to 24 MHz clock input which is used to generate time slots for buffer memory access when not reading or writing disk data. This is also used for SCSI Arbitration and Reselection time constants.
RG	43	O	**READ GATE**: This signal is asserted when the CL–SH250 is reading NRZ data from the disk interface.
WG	44	O	**WRITE GATE**: This signal is asserted when the CL–SH250 is writing NRZ data to the disk interface.

1.2 Pin Assignments *(cont.)*

DISK INTERFACE PINS (cont.)

SYMBOL	PIN NUMBER QFP	TYPE	DESCRIPTION
RD/REF CLK	45	I	**READ/REFERENCE CLOCK**: This is the primary clock for the chip and must be present at all times including during the Reset operation. It is used in conjunction with the the NRZ signal (Pin 46) to clock data in and out of the chip. Typically, it is sourced from the VFO Oscillator when the READ GATE signal (Pin 43) is asserted; otherwise, it is sourced from the Write Oscillator.
NRZ	46	I/O	**NRZ**: Read data input from the disk when the READ GATE signal (Pin 43) is asserted; write data output to the disk when the WRITE GATE signal (Pin 44) is asserted.
OUTPUT	47	O	**OUTPUT PIN**: This signal is controlled by Bit 2 of the formatter sequencer's CONTROL FIELD (A0H thru BEH) .

SCSI BUS PINS

SYMBOL	PIN NUMBER QFP	TYPE	DESCRIPTION
SDB0*:7*	52-54, 57, 59-62	I/O, OD**	**SCSI DATA BUS:** These eight signals are the parallel data lines to and from the SCSI bus
SDBP*	64	I/O, OD**	**SCSI DATA BUS PARITY**: This signal indicates odd parity on the SCSI data bus.
ATN*	68	I	**SCSI ATTENTION**: This signal indicates the ATTENTION condition on the SCSI bus.
BSY*	69	I/O, OD	**SCSI BUSY**: This signal indicates that the SCSI bus is being used.
ACK*	70	I	**SCSI ACKNOWLEDGE**: When this signal is asserted low, it indicates that a SCSI Initiator has acknowledged the data transfer.
SRST*	72	I	**SCSI RESET**: This signal indicates the Reset condition on the SCSI bus. When this signal is asserted low, the SCSI BUSY signal (Pin 69) and the SCSI SELECT signal (Pin 76) are not actively driven; the ARBITRATION bit (Register 52H, Bit 0), the BUS OUTPUT ENABLE bit (Register 52H, Bit 3), and the ENABLE TARGET bit (Register 53H, Bit 7) will be reset. The SCSI DATA BUS (Pins 52-54, 57, 59-62), the SCSI DATA BUS PARITY (Pin 64), the SCSI INPUT/OUTPUT (Pin 79), the SCSI COMMAND/DATA (Pin 77), the SCSI MESSAGE (Pin 73), and the SCSI REQUEST (Pin 78) signals also go to a high-impedance state. Bit 1 of Register 52H will also be set.
MSG*	73	I/O, OD**	**SCSI MESSAGE**: This signal indicates the SCSI Message phase on the SCSI bus.
SEL*	76	I/O, OD	**SCSI SELECT**: This is a signal used by a SCSI Initiator to select a SCSI Target or by a SCSI Target to reselect a SCSI Initiator.
C*/D	77	I/O, OD**	**SCSI COMMAND/DATA:** This signal indicates whether CONTROL (when low) or DATA (when high) information is on the SCSI data bus signals.
REQ*	78	I/O, OD**	**SCSI REQUEST:** This signal indicates that a request for a REQ/ACK data transfer handshake is on the SCSI bus.

SCSI BUS PINS (cont.)

SYMBOL	PIN NUMBER QFP	TYPE	DESCRIPTION
I*/O	79	I/O, OD**	**SCSI INPUT/OUTPUT:** This signal controls the direction of data movement on the SCSI data bus signals with respect to a SCSI Initiator. Low indicates information input to the SCSI Initiator and high indicates output from the SCSI Initiator. This signal is also used to distinguish between the SCSI Selection and Reselection phases.

OD** The open-drain capability of these signals is programmable (see Register 58H, Bit 3).

POWER AND GROUND PINS

SYMBOL	PIN NUMBER QFP	TYPE	DESCRIPTION
+5V	38, 90-91	N/A	**POWER SUPPLY.**
GND	1-2, 25-26, 42, 88		**GROUND.**
SGND	49, 58, 65-66, 74, 82	N/A	**HIGH CURRENT GROUND.**
N/C	5, 14, 21,24, 28-29, 48, 50, 51, 55-56, 63, 67, 71, 75, 80-81	N/A	**NO CONNECTION.**

2. REGISTER TABLES

2.1 Buffer Manager and SCSI Interface Registers

ADDRESS	TYPE	DESCRIPTION/FUNCTION
40H/60H	R	SCSI INTERRUPT STATUS
42H/62H	R/W	SCSI INTERRUPT ENABLE
52H	R/W	SCSI SELECTION CONTROL
53H	R/W	DMA CONTROL
54H	R/W	BUFFER SIZE
58H	R/W	SCSI MODE CONTROL REGISTER
59H	R/W	BUFFER MANAGER / SCSI RESET CONTROL
5AH, 5BH	R/W	READ ADDRESS POINTER (RAP)
5CH, 5DH	R/W	WRITE ADDRESS POINTER (WAP)
5EH, 5FH	R/W	SCSI STOP POINTER (SCSI-SP)
7EH	R/W	SCSI INFORMATION PHASE CONTROL

2.2 Disk Formatter Registers

ADDRESS	TYPE	DESCRIPTION/FUNCTION
41H/61H	R	DISK INTERRUPT STATUS
43H/63H	R/W	DISK INTERRUPT ENABLE
4DH	R	SHADOW LATCH
4EH	R/W	SECTOR SIZE
71H	R/W	ECC CONTROL
72H	R/W	ECC CORRECTION SHIFT-REGISTER / COUNTER
73H - 76H	R	ECC STATUS
77H	R/W	FORMATTER / BUFFER MANAGER MODE SELECTION
78H 78H	R W	NEXT ACTIVE SEQUENCER ADDRESS BRANCH ADDRESS
79H 79H	R W	SEQUENCER STATUS SEQUENCER START ADDRESS

2. REGISTER TABLES *(cont.)*

2.2 Disk Formatter Registers *(cont.)*

ADDRESS	TYPE	DESCRIPTION/FUNCTION
7AH	R/W	OPERATION CONTROL / STATUS
7BH	R/W	WAM CONTROL
7CH	R/W	SYNC PATTERN
7FH	R	FORMATTER STACK READ
7FH	W	CLOCK/SYNC CONTROL

2.3 External Access Registers

ADDRESS	TYPE	DESCRIPTION/FUNCTION
50H	R/W	SCSI BUS ACCESS
70H	R/W	BUFFER MEMORY ACCESS

2.4 Writable Control Store (WCS)

ADDRESS	TYPE	DESCRIPTION/FUNCTION
80H-9EH	R/W	NEXT ADDRESS FIELD
A0H-BEH	R/W	CONTROL FIELD
C0H-DEH	R/W	COUNT FIELD
E0H-FEH	R/W	DATA FIELD

2.5 Sequencer Registers

ADDRESS	TYPE	DESCRIPTION/FUNCTION
49H-4CH	R/W	CURRENT SEQUENCER WORD

3. FUNCTIONAL DESCRIPTION

The CL-SH250 is designed to be used with a low-cost microcontroller, which allows it to maintain a "loose" synchronization with the real-time disk operation. The CL-SH250 maintains "close" synchronization with the data to and from the disk drive and provides the signals necessary to control this path. Using the CL-SH250 means a lower total part count for the intelligent disk drive design.

The CL-SH250 is divided into four major functional blocks:

- Microcontroller Interface
- Disk Formatter
- Buffer Memory Interface
- SCSI Bus Interface

3.1 Microcontroller Interface

The microcontroller interface is based on an eight-bit multiplexed address and data bus found on popular microcontrollers such as the Intel 8085/8031/8051 and the Motorola 68HC11.

The CL-SH250 decodes addresses from 40H to FFH. In order to prevent erroneous operations, the disk controller board design should reserve the decoding of addresses 40H to FFH for the CL–SH250 only. However, the CL-SH250 does not decode addresses 68H to 6FH. The decoding of addresses 40H-47H and 60H-67H can be totally disabled by resetting the INTERRUPT REGISTER ACCESS ENABLE bit (Register 77H, Bit 1). In that case, the CL-SH250 will not decode addresses 40H-47H and 60H-67H as well.

The CL-SH250 has a programmable interrupt circuit available. There are 13 interrupt sources available from both the Buffer Manager/SCSI Interface Registers and from the Formatter Registers, as shown in Tables 3.1 and 3.2:

Table 3.1 Buffer/SCSI Interrupt Sources

SCSI DMA Done	SCSI Arbitration Detected
SCSI Attention Detected	SCSI Selection Phase Detected
SCSI Parity Error	SCSI Reset Detected

Table 3.2 Formatter Interrupt Sources

Index Past	Sector Past
Input Detected	Data Transfer Detected
ECC Error	Sequencer Output Detected
Sequencer Stopped	

The interrupt capability can be completely disabled (by resetting Register 77H, Bit 3), or the individual interrupt sources can be masked. Four interrupt registers provide the status and mask programmability for the interrupt sources. When the interrupt registers are enabled (Register 77H, Bit 1 is set), the four registers can be mapped to either 40H-43H or 60H-63H by programming the INTERRUPT REGISTER DECODE SELECT bit (Register 77H, Bit 2). Mapping these registers into addresses 40H-43H will disable the CL-SH250 from decoding addresses 60H-67H (they can be used for external system usage). Mapping them into 60H-63H will make addresses 40H-47H available for external system usage. Even when the interrupts are disabled (Register 77H, Bit 3 is reset) if the access to the registers is enabled (Register 77H, Bit 1 is set), the Interrupt Status Registers may be used as a focal point for microcontroller control when the CL-SH250 is being used in a polled mode.

The CL-SH250 provides the microcontroller read access to external switch settings. The microcontroller accesses these switches by reading Register 70H, with the MOE* DISABLE bit (Register 58H, Bit 1) set to a logical 1. The microcontroller-readable switches are connected to the buffer memory data bus. These switches must be installed with relatively high impedance pull-ups and pull-downs so that the resistor impedance does not affect buffer memory performance (it is recommended to use 270 KΩ pull-up and 27 KΩ pull-down and wait 25 µsec after the last buffer memory access for stability).

3.2 Disk Formatter

The basic operation of the Disk Formatter is controlled by the contents of the Sequencer Writable Control Store (WCS). A Sequencer program must be entered into the WCS before the CL-SH250 Disk Formatter can function properly. Under firmware control, the Disk Formatter can be made to sequence through different types of operations, such as: Read ID, Read ID and Read Data, Read ID and Write Data, and Write ID and Write Data.

The Sequencer controls the timing relationships between the disk interface output signals and monitors disk interface input lines to branch to different Sequencer locations. The track layout, such as gap lengths, sector size, and sector data fill character, can be flexibly defined in the WCS. The CL-SH250 Disk Formatter also has other registers that can be used to control the definition of the track format such as the SYNC character and the ADDRESS MARK.

The WCS consists of 124 bytes, organized as 31 words, each four bytes wide. The WCS word can be broken down into DATA, COUNT, NEXT ADDRESS and CONTROL FIELDS.

The DATA FIELD contains data which may be used to initialize the track format, including gap, ID field, and sector data fill characters. This data can also be compared to the NRZ data-in to identify various fields in a sector or to execute sector data compares.

The COUNT FIELD specifies the initial value minus one of the Sequencer Counter for the current word. The Sequencer Counter is decremented once every eight READ/-REFERENCE CLOCK (RD/REF CLK) cycles. When the count reaches zero, the Sequencer will go to the next address.

The next address will be based on the contents of the NEXT ADDRESS FIELD of the WCS word unless a branch condition has been programmed and met during the last byte of the current WCS word.

If a branch condition has been programmed and met, then the next address to be executed is based on the contents of the BRANCH ADDRESS Register (78H). Thus, by programming different branch conditions which are based on external or internal events, the chip can be made to sequence through different operations.

The CONTROL FIELD is used to generate and initiate all synchronous NRZ data handling operations.

The microcontroller's control of the Sequencer revolves around the SEQUENCER START ADDRESS (Register 79H) and the BRANCH ADDRESS (Register 78H). Writing to Register 79H loads the starting address (where the Sequencer is to begin execution), and causes the four bytes at that WCS word to be fetched and written into the Current Sequencer Word Registers (Registers 49H-4CH).

The serial data flow portion of the Disk Formatter consists of a CRC/ECC generator and a serializer/deserializer. Data to be written to the disk enters the CL-SH250 in a byte-wide format. It is serialized and run through a CRC/ECC generator. An NRZ serial bit stream is then shifted out to the disk drive. Note that the NRZ serial bit stream will include serialized constants required for address marks, gaps, and ID fields, as well as the serialized data and ECC generated output.

The CL-SH250 can be programmed (in the WCS COUNT FIELD) for the 16-bit CRC, or one of the ECC polynomials. It can also be fully suppressed to use external ECC circuitry.

The CL-SH250 can be configured for one of two ECC modes. After the RST* signal (pin 40) is asserted, Register 77, bit 5 is reset (to a logic zero) and the 56-bit computer generated polynomial is selected. Also, the ECC circuitry (or linear feedback shift register) is initialized to all logic 1's before use.

When Register 77, bit 5 is set (to a logic 1), the 32-bit Fire Code polynomial is selected. Also, the ECC circuitry is initialized to all logic 0's before use.

The CRC polynomical used is the CCITT-CRC code:

$$x^{16} + x^{12} + x^5 + 1.$$

The CL–SH250 provides the option of using an ECC polynomial by programming the COUNT FIELD of the appropriate WCS word. The forward and reverse 32-bit Fire Code polynomials are derived from the root polynomials

$$(x^{21} + 1) \text{ and } (x^{11} + x^2 + 1)$$

The forward 32-bit polynomial is:

$$x^{32} + x^{23} + x^{21} + x^{11} + x^2 + 1$$

The reverse 32-bit polynomial is:

$$x^{32} + x^{30} + x^{21} + x^{11} + x^9 + 1$$

The forward and reverse 56-bit ECC polynomial is a computer-generated code provided under license from Neal Glover of Data Systems Technology, Broomfield, CO. The forward 56-bit polynomial is:

$$x^{56} + x^{52} + x^{50} + x^{43} + x^{41} + x^{34} + x^{30} + x^{26} + x^{24} + x^8 + 1$$

The reverse 56-bit polynomial is:

$$x^{56} + x^{48} + x^{32} + x^{30} + x^{26} + x^{22} + x^{15} + x^{13} + x^6 + x^4 + 1$$

This polynomial can detect single burst errors up to 56 bits in length, and double-burst errors, where the combination of bursts is less than or equal to 41 bits. This polynomial can also correct single-burst errors up to 23 bits in length.

Data read from the disk enters the CL-SH250 as an NRZ serial bit stream. The input data stream is run through the ECC generator and deserialized into a byte-wide format. The syndrome is saved in the ECC registers and will not be reset until a new Read operation is started.

If an ECC error is detected after a Read Data operation, the microcontroller uses the information stored in Registers 71H - 76H to determine if the error is correctable and to calculate the error pattern and displacement from the beginning of the sector. After this, the error can be corrected in the data bytes in the buffer memory. The CL-SH250 has hardware assist circuitry to speed up the correction process.

During a read process from the device, the CL-SH250 also has the ability to compare the data being received on a byte-by-byte basis with information either from the DATA FIELD of the WCS (such as verifying the ID field) or from the external buffer memory (such as during a data field search operation).

The CL-SH250 also has a circular stack eight bytes deep. By enabling this (setting Bit 4 of the WCS CONTROL FIELD) during the Read operation, information read from the disk drive can be pushed onto the stack to be examined later at a lower speed by the microcontroller (Register 7FH). This capability can be used to pass the ID field to the microcontroller for defect management, seek verification and other disk controller tasks.

3.3 Buffer Memory Interface

Byte-wide data transferred by the CL-SH250 is passed to and from the buffer memory on the buffer memory data bus.

The CL-SH250 is capable of controlling buffer memory sizes up to 64K bytes of static RAM. The chip provides 16 buffer memory address lines (BA0 - BA15) along with a Memory-Output-Enable (MOE*) signal (Pin 15), and a Write-Enable (WE*) signal (Pin 16) for the static buffer memory.

One buffer memory cycle must be initiated for each byte transferred by the serializer/deserializer. The BUFCLK* output (Pin 94) defines the buffer memory access cycles. There must be a minimum of two memory cycles per byte-serialization time (eight RD/REF CLK cycles) to maintain concurrent transfer between the disk and buffer memory, and between the host and buffer memory. Four memory cycles per byte-serialization time allow more host accesses for each disk access of the buffer memory. The CL-SH250 is designed to take advantage of this burst speed for high SCSI throughput. The number of buffer memory access cycles (BUFCLK* cycles) per byte-serialization time is programmed in Register 7FH, Bit 4. If this bit is set, there will be two BUFCLK* cycles per byte-serialization time. This is the Two Window Mode. If this bit is reset, then there will be four BUFCLK* cycles per byte-serialization time. This is the Four Window Mode. If the CL-SH250 is not performing a data transfer operation, then the source of the BUFCLK* output is the SYSTEM CLOCK (SYSCLK) input, which is divided per Register 7FH, Bits 6,7.

The CL-SH250 can support up to 6 MBytes/sec of buffer memory throughput. Applications with a NRZ data rate higher than 12 Mbit/sec must use Two Window mode. The period of the BUFCLK* determines the access time requirement for the buffer memory along with other CL-SH250 specifications. The CL-SH250 samples the data from the RAM at the falling edge of the BUFCLK* signal (Pin 94). Use the Memory-Output-Enable (MOE*) signal as the SRAM output enable (OE*) in order to take advantage of utilizing slower speed SRAM in high-speed applications.

The CL-SH250 handles data transfer in two ways:

(1) synchronously with the disk or

(2) asynchronously with the SCSI host.

Synchronous Disk Transfer

In case of disk transfers, a byte is transferred after every time the Disk Formatter requires service (for a deserialized byte or a byte to serialize). The direction of the transfer is determined by the value of the ROP/WOP* bit (Register 53H, Bit 4). For a Disk Read operation, the ROP/WOP* bit (Register 53H, Bit 4) is set to logical 1, and the NRZ data is deserialized and written to the buffer memory at the location specified by the contents of the WRITE ADDRESS POINTER (WAP) Registers (5CH and 5DH). For a Disk Write operation the ROP/WOP* bit (Register 53H, Bit 4) is reset to logical 0, and the data read from the buffer memory at the location specified by the contents of the READ ADDRESS POINTER (RAP) Registers (5AH and 5BH) is serialized and written to the disk.

Asynchronous SCSI Transfer

In case of transfers between the SCSI bus and buffer memory, data is transferred under DMA control. The direction of transfer is determined by the contents of the SCSI WRITE ENABLE and SCSI READ ENABLE bits (Register 53H, Bits 2 and 3 respectively) along with the ROP/WOP* bit (Register 53H, Bit 4).

For proper operation of the CL-SH250 during read-only operations, the ROP/WOP* bit (Register 53H, Bit 4) must be set to logical 1 when the SCSI READ ENABLE bit (Register 53H, Bit 3) is set. During write-only operations, the ROP/WOP* bit (Register 53H, Bit 4) must be reset to logical 0 when the SCSI WRITE ENABLE bit (Register 53H, Bit 2) is set.

If the SCSI READ ENABLE bit (Register 53H, Bit 3) is set and the ROP/WOP* bit (Register 53H, Bit 4) is set to logical 1, the READ ADDRESS POINTER (RAP) Registers (5AH and 5BH) are used to select the buffer memory location. The data is transferred from the buffer memory to the SCSI bus.

If the SCSI WRITE ENABLE bit (Register 53H, Bit 2) is set to logical 1 and the ROP/WOP* bit (Register 53H, Bit 4) is reset to logical 0, the WRITE ADDRESS POINTER (WAP) Registers (5CH and 5DH) are used to select the buffer memory location where data is transferred from the SCSI bus.

During the SCSI bus data transfer, the top buffer memory address that can be accessed is controlled by the SCSI STOP POINTER (Registers 5EH and 5FH). This SCSI STOP POINTER (Register 5EH and 5FH) is compared with the appropriate Address Pointer (the READ ADDRESS POINTER--RAP (Registers 5AH and 5BH), or the WRITE ADDRESS POINTER--WAP (Registers 5CH and 5DH), masked by the content of Register 54H. When a match occurs, the SCSI DMA DONE bit (Register 53H, Bit 5) is set signifying the completion of the transfer to or from the host.

Microcontroller/Buffer Transfer

Register 70H decode is provided for the microcontroller to gain access to the buffer memory. The buffer memory data bus and the microcontroller data bus are internally bridged accordingly.

The buffer memory address for a Register 70H access is generated based upon the contents of the READ ADDRESS POINTER (RAP) Registers (5AH and 5BH) if the ROP/WOP* bit (Register 53H, Bit 4) is reset to logical 0 (WOP); and on the contents of the WRITE ADDRESS POINTER (WAP) Registers (5CH and 5DH) if the ROP/WOP* bit is set to logical 1 (ROP). The RAP or WAP will not be incremented by Register 70H accesses.

3.4 SCSI Bus Interface

The CL-SH250 provides all the logic to interface to the SCSI bus. Register 50H decode is provided for the microcontroller to access the SCSI data bus directly. The SCSI data bus (SDB0*:7*) and the microcontroller data bus (AD0:7) will be internally bridged accordingly. The microcontroller also has the ability to handshake packets across the SCSI data bus directly, even when the Disk Formatter is accessing the buffer memory.

The microcontroller can:

a) Control the Arbitration/Selection/Reselection process through the SCSI SELECTION CONTROL Register (52H).

b) Control the SCSI Information phase through the SCSI INFORMATION PHASE CONTROL Register (7EH).

c) Control the data handshake by setting SCSI REQUEST and observing SCSI ACKNOWLEDGE in the DMA CONTROL Register (53H).

A read of SCSI BUS ACCESS (Register 50H) will gate the SCSI data on to the microcontroller data bus. A write to Register 50H will latch the data from the microcontroller. The microcontroller data then can be asserted on the SCSI data bus through SCSI SELECTION CONTROL (Register 52H).

The arbitration logic of the CL-SH250 complies with the SCSI Arbitration and Selection phase protocol and timing. Although the logic is designed to arbitrate automatically, the controlling microcontroller is responsible for evaluating the arbitration byte and controlling the Selection/-Reselection process. The timing to the arbitration logic is provided by a prescaled clock which is generated by dividing the SYSCLK according to the value programmed in Register 7FH, Bits 6 and 7. If the period of the internally divided SCSI clock is still too fast, it can be divided by two again by setting Register 58H, Bit 0. This division by two enabled in Register 58H only affects the SCSI clock during the SCSI Arbitration logic. The buffer memory timing on the CL-SH250, when synchronized to the internal SYSCLK, is unaffected by the additional divide by two enabled in Register 58H. Effectively, the period of the SCSI Arbitration clock should be between 200 and 400 nsec.

The CL-SH250 has a SCSI TRISTATE ENABLE mode. With the SCSI TRISTATE ENABLE (Register 58H, Bit 3) reset, the CL-SH250 is backwards compatible with all CL-SH250 revisions. In this mode, the SCSI output drivers (I*/O, C*/D, MSG*, SDB0*:7*, and SDBP*) do not have tristate capability, but the SCSI REQ* (Pin 76) tristate driver is enabled when the local processor has:

1) Set ENABLE TARGET (Register 53H, Bit 7),

2) set BUSY OUT (Register 52H, Bit 7),

3) reset SCSI TRISTATE ENABLE (Register 58H, Bit 3),
4) and the SCSI SEL* signal (Pin 76) is not active.

This enables the SCSI REQ* tristate during the SCSI Information Phases, and disables the SCSI REQ* tristate during the SCSI Bus Free, Arbitration, Selection or Reselection Phases.

When the SCSI TRISTATE ENABLE (Register 58H, Bit 3) is set and ENABLE TARGET (Register 53H, Bit 7) is set, the SCSI output drivers (REQ*, I*/O, C*/D, MSG*, SDB0*:7*, and SDBP*) are enabled. The SDB0*:7*, and SDBP* tristate drivers also require a Bus Output Enable (which may be asserted from Bit 3 of Register 52H, or from one of the internal SCSI state machines).

On power-up, SCSI TRISTATE ENABLE (Register 58H, Bit 3) is reset. The SCSI BUSY* (Pin 69) and SCSI SEL* (Pin 76) signals are always configured as open-drain drivers.

The SCSI TRISTATE ENABLE mode is designed to lower system power consumption by eliminating the need for termination resistor networks in a reduced SCSI environment.

In the SCSI TRISTATE ENABLE mode in an arbitrating SCSI environment the SCSI data bus pull-up drivers are disabled during the arbitration phase (as bus contention would disrupt the arbitration phase). The CL-SH250 still requires external resistor pull-ups to support an arbitrating SCSI environment.

To use the SCSI TRISTATE ENABLE mode in a single-initiator multiple-target non-arbitrating SCSI/SASI environment, the tristate drivers should only be enabled after the CL-SH250 has been selected so that only one target is driving the SCSI bus at any instance.

To use the SCSI tristate enable mode in a single-initiator single-target non-arbitrating SCSI/SASI environment, the tristate drivers can be enabled without constraints.

4. FUNCTIONAL OPERATION

The CL-SH250 performs two basic disk operations, reading NRZ data in and writing NRZ data out. These two operations can be combined easily into the following four major functions:

- Read ID or Sector Identification
- Read ID and Write Data or Sector Write
- Read ID and Read Data or Sector Read
- Write ID and Write Data or Format Sector

These can be further modified to perform the Search Data and Verify Data functions.

Read Operation

One of the fundamental requirements of the Read operation is to synchronize the incoming data on byte boundaries and then either process the data or pass the data through to the buffer memory.

Data synchronization occurs when a specific data stream compares to the sync pattern programmed in the SYNC PATTERN Register (7CH). The number of bits used in synchronization comparison is specified by the contents of the CLOCK/SYNC CONTROL Register (7FH), Bits 0-2. The process begins when the CONTROL FIELD of the Current Sequencer Word activates the READ GATE signal (Pin 43). The serial data passes through a programmable synchronization comparator until a match is found with the contents of the SYNC PATTERN Register (7CH). If the CL-SH250 is in Soft Sector mode, this comparison must be qualified by the assertion low of the WAM*/AMD*/ SECTOR signal (Pin 39) by the time the last NRZ bit of the sync pattern is read into the CL-SH250.

Typically, for soft-sectored formats, the first byte after the synchronization byte is used to differentiate between Sector ID and Data Fields. After synchronization, the Sequencer has the ability to enable the comparison of the incoming data against the DATA FIELD of the WCS and also to capture the incoming data on the stack. The comparison and branch capability of the Sequencer allows the incoming data to be recognized and acted upon. The programmable compare capability can be used to access the correct sector automatically by recognizing the proper Sector ID. If the Sector ID does not match the DATA FIELD of the Current Sequencer Word then the Sequencer can be programmed to stop, and can be restarted by the microcontroller to find the sector again. Note that a delay will often be implemented before the microcontroller restarts this operation. This is done to minimize the danger of false synchronization, particularly during Write splices.

Write Operation

The other disk operation of the CL-SH250 is writing NRZ data. This operation begins when the CONTROL FIELD in the Current Sequencer Word activates WRITE GATE (WG). WRITE GATE (Pin 44) is typically switched on at a specific place in the track layout: during a Write splice after the sector ID ECC (for a write sector data operation), or after INDEX (for a track format operation). Data from the Current Sequencer Word's DATA FIELD or from the buffer memory data bus is passed through the serializer then through the ECC circuitry, and out the NRZ data signal (Pin 46).

4.1 Sector Identification

The Sector Identification function consists of reading the Sector ID field to identify to the microcontroller the current sector address. This function is typically performed with a comparison of the Sector ID field Address Mark, a capture of the Sector ID field in the stack, and finally an ECC/CRC verification of data integrity. Any of the incoming data bytes may be captured in the stack by programming the STACK ENABLE bit (Bit 4) in the WCS CONTROL FIELD. Also, any of the incoming data bytes may be compared against the WCS DATA FIELD by programming both the WCS DATA FIELD and the COMPARE ENABLE bit (Bit 1) in the WCS CONTROL FIELD.

After the Sector Identification function is completed, the microcontroller can then read the SEQUENCER STATUS Register (79H). If there was no ECC error, the microcontroller can then read the stack to identify the current sector address or it may repeat the function.

4.2 Sector Read

The Sector Read function typically consists of two parts. The first is reading and identifying the desired Sector ID field, as previously described in Section 4.1; however, the desired sector address will also be included in the comparison. A branch condition is

often programmed at the end of the Sector Identification function such that if the compared bytes match and there was no ECC error, the Sequencer will automatically execute the second half of the Sector Read function.

After the sector has been positively identified, the second half of the Sector Read function is to transfer the Sector Data field to the buffer memory. Before transferring the Sector Data field, the source of BUFCLK* must be changed from SYSCLK (Pin 41) to RD/REF CLK (Pin 45) for proper synchronization of the data. This change is accomplished by setting COUNT/SWITCH (COUNT FIELD, Bit 5). BUFCLK* source will continue to be synchronized to SYSCLK until the SYNC PATTERN (Register 7CH) is detected. After the read, the microcontroller may then read the SEQUENCER STATUS Register (79H) and determine the completion status of the Sector Read. If the read was successful, then the microcontroller will typically program the CL-SH250 to transfer this sector from the buffer memory to the host. If the read was not successful, the microcontroller may try to correct the data or attempt to re-read this sector.

4.3 Sector Write

The Sector Write function typically consists of two parts. The first is identical with the first part of the Sector Read; reading the Sector ID field. The same Sequencer routine should be used. The only difference is that after a successful Sector ID read, the next address should be the address of the Write Sector routine. This can usually be accomplished by changing the address in the BRANCH ADDRESS Register (78H) after a successful ID read.

After the sector has been positively identified, the second half of the Sector Write function is to transfer the data from the buffer memory to the disk as explained in the Write operation described above. Before transferring the Sector Data Field, the source of BUFCLK* must be changed from SYSCLK (Pin 41) to RD/REF CLK (Pin 45) for proper synchronization of the data. This change is accomplished by setting the COUNT/SWITCH bit (COUNT FIELD, Bit 5). For the Sector Write function, this change occurs immediately upon setting this bit.

4.4 Format Sector

The Format Sector function consists of a Write operation that will write both the Sector ID field and the Sector Data field. This function is normally started with the Sequencer waiting for the INDEX pulse to branch into the Write operation routine. The microcontroller can update the Sector ID field information in the WCS while the Sector Data field is being written on the disk. This allows a full track format with a minimum of microcontroller intervention.

The CL-SH250 allows the Sector Data Field to be generated from the WCS instead of from the buffer memory, through the use of the SUPPRESS TRANSFER bit (Register 7AH, Bit 5).

4.5 Search Data

The Sector Read function can be modified into a Search Data function. When the second half of the Sector Read function is entered, the contents of the buffer memory will be compared, byte-for-byte, with the incoming data from the disk drive. This comparison of the DATA FIELD is enabled by setting the SEARCH OPERATION bit (Bit 4) of the OPERATION CONTROL/STATUS Register (7AH) and the COMPARE ENABLE bit (Bit 1) in the CONTROL FIELD of the WCS word which processes the data transfer.

The result of this comparison is latched into the SEQUENCER STATUS Register (79H, Bits 0 and 1). After the completion of the Data function, reset both the COMPARE ENABLE bit (WCS CONTROL FIELD, Bit 1) in the Formatter Sequencer instruction which processes the data, and the SEARCH OPERATION bit (Register 7AH, Bit 4).

4.6 Verify Sector

By setting the SUPPRESS TRANSFER bit in the OPERATION CONTROL/STATUS Register, (7AH, Bit 5) and performing a Read Sector function, the incoming data will be verified for good ECC but will not be transferred to the buffer memory.

4.7 Extended Data Handling

Variable Sector Size

The CL-SH250 has an eight-bit Sector Data field length counter loadable from the COUNT FIELD of the WCS. The COUNT FIELD is programmable. By setting it to any value from 00H to FFH, any block length up to 256 bytes can be transferred. The value of the COUNT FIELD should be one less than the actual sector length. For sector sizes greater than 256 bytes, several different methods can be used.

The simplest approach is to use as many Sequencer words as required to implement the count for the data field.

The next approach uses the INHIBIT CARRY bit in the OPERATION CONTROL/STATUS Register (7AH, Bit 7). By setting the INHIBIT CARRY bit (Register 7AH, Bit 7) before the count of the WCS word with the DATA TRANSFER bit (CONTROL FIELD, Bit 0) set has expired, the Sequencer will be inhibited from going on to the next WCS word, and another 256 bytes of data will be transferred. The INHIBIT CARRY bit (Register 7AH, Bit 7) will be automatically reset on the next carry of the word with the DATA TRANSFER bit (CONTROL FIELD, Bit 0) set (underflow of the current control word's count field). By testing and setting this bit, additional counts of 256 byte segments may be transferred. For odd-sized data fields, initialize the COUNT FIELD with the remainder and use the modulo-256 counter for the bulk of the counting (i.e., for 532 bytes, start with a count of 13H and set the INHIBIT CARRY bit (Register 7AH, Bit 7) twice).

The final approach uses the COUNT FIELD and the INHIBIT CARRY bit (Register 7AH, Bit 7), as well as the SECTOR SIZE (Register 4EH), to program how many 256 byte counts the INHIBIT CARRY bit (Register 7AH, Bit 7) should suppress. The number initialized in the SECTOR SIZE Register (4EH) should be one less than the number of multiples of 256 byte segments to be transferred, (i.e., for 532 bytes, start with the SECTOR SIZE Register (4EH) initialized to 01H, an initial count of 13H in the WCS COUNT FIELD, and set the INHIBIT CARRY bit (Register 7AH, Bit 7)).

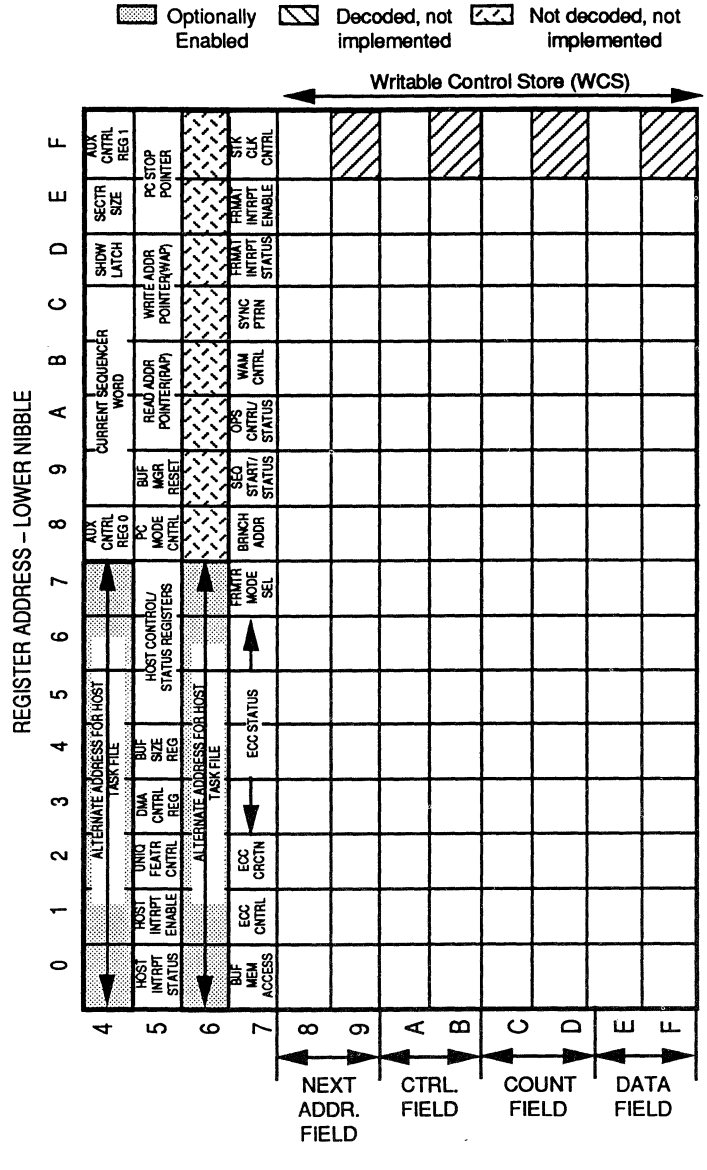
Multi Sector Read/Write Operations

Multi-sector Read or Write operations can be accomplished by two methods. The simplest method is to load the next sector ID to be accessed while the DATA TRANSFER STATUS bit (Register 79H, Bit 6) is set for the present sector, and restarting the Read or Write operation immediately after the end of the present sector.

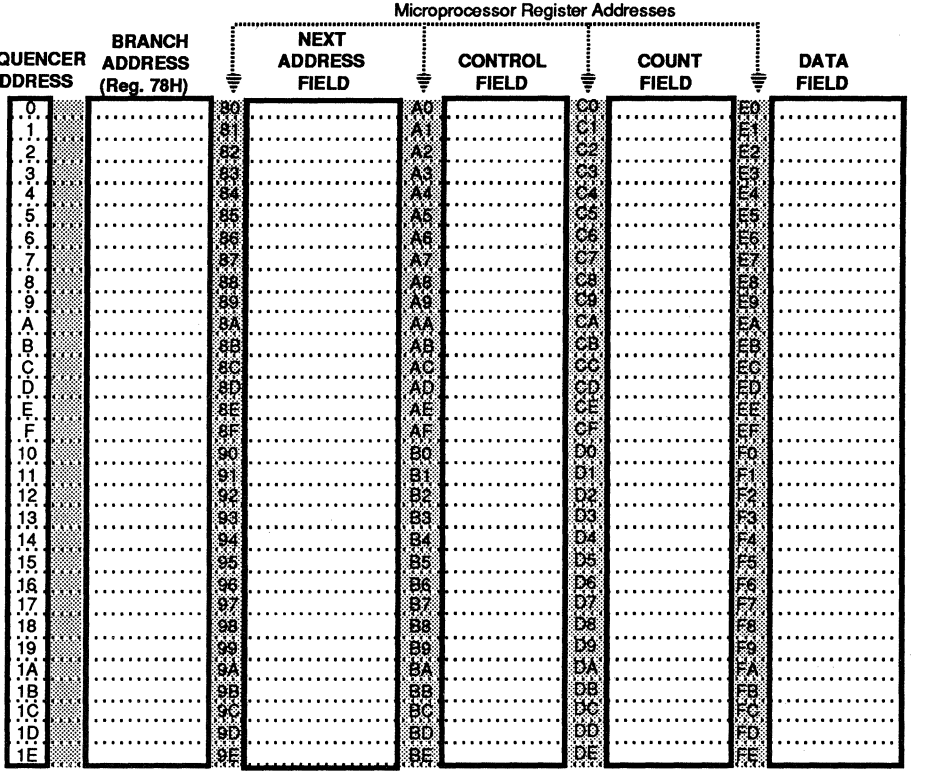
The next approach loads multiple ID field read subroutines and a single read/write data field subroutine into the thirty-one word WCS. The BRANCH ADDRESS (Register 78H) can then be used to jump between the subroutines.

5. REGISTER ADDRESSES

5.1 Memory Map



5.2 WCS Worksheet



If (RG • ECC) = 1
000 = CONTINUE, NEXT ADDRESS USED
001 = STOP ON ECC ERROR
010 = STOP ON COMPARISON NOT EQUAL
011 = STOP ON COMPARISON NOT EQUAL OR ECC ERROR
100 = BRANCH ON GOOD ECC AND COMPARISON EQUAL
101 = BRANCH ON ECC ERROR
110 = BRANCH ON COMPARISON NOT EQUAL
111 = BRANCH ON COMPARISON NOT EQUAL OR ECC ERROR

If (RG • ECC) = 0 AND REGISTER 77H, BIT 6 = 1
000 = CONTINUE, NEXT ADDRESS USED
001 = STOP IF INPUT RISING EDGE DETECTED
010 = STOP IF INDEX OR SECTOR RISING EDGE DETECTED
011 = STOP ON COMPARISON NOT EQUAL
100 = BRANCH ON CARRY
101 = BRANCH ON INPUT RISING EDGE DETECTED
110 = BRANCH ON INDEX OR SECTOR RISING EDGE DETECTED
111 = BRANCH ON COMPARISON NOT EQUAL

IF (RG • ECC) = 0 AND REGISTER 77H, BIT 6 = 0.
110 = BRANCH ON INDEX AND SECTOR RISING EDGE NOT DETECTED

6.0 BUFFER MANAGER AND SCSI INTERFACE REGISTERS

6.1 40H (or 60H) – SCSI Interrupt Status (Read Only)

Bit 0	**SCSI DMA DONE:** When this bit is set, it indicates a completion of the SCSI transfer cycle. This occurs when the SCSI STOP POINTER Registers (5EH and 5FH) are equal to the appropriate Host Address Pointers. During a disk read operation, the Stop Pointer will be equal to the READ ADDRESS POINTER Registers (5AH and 5BH). During a disk write operation, the Stop Pointer will be equal to the WRITE ADDRESS POINTER Registers (5CH and 5DH). This bit is set whenever the SCSI WRITE ENABLE (Bit 2) or the SCSI READ ENABLE are deasserted (Read Only)
Bit 1	**SCSI ARBITRATION DETECTED:** This bit reflects the history of the SCSI Arbitration attempts. When the local circuit starts arbitrating, this bit will be set (even if the attempt is not successful). This latch will be cleared by a microcontroller read of this register.
Bit 2	**SCSI SELECTION PHASE DETECTED:** This bit is set by any SCSI Selection phase on the SCSI bus. This bit will be cleared by a microcontroller read of this register.
Bit 3	**SCSI ATTENTION DETECTED:** This bit gets set when the SCSI ATTENTION signal (Pin 68) is asserted low. This bit is the same as Bit 3 of the SCSI INFORMATION PHASE CONTROL Register (7EH). (The read of this register does not reset this status, reading Register 7EH does).
Bit 4	**SCSI RESET DETECTED:** This bit reflects SCSI RESET (Pin 72) history. This bit is the same as Bit 1 of the SCSI SELECTION CONTROL Register (52H). (A microcontroller read of this register does not reset this status, reading Register 52H does).
Bit 5	**SCSI PARITY ERROR:** When the SCSI SELECT signal (Pin 76) is deasserted, this bit indicates the latched parity status from a DMA transfer read or a local microcontroller read of the SCSI BUS ACCESS Register (50H).
Bit 6	**RESERVED.**
Bit 7	**FORMATTER INTERRUPT ACTIVE:** This bit is the logical-OR of the bits in the DISK INTERRUPT STATUS Register (41H/61H).

6.2 42H (or 62H) – SCSI Interrupt Enable (Read/Write)

Bit 0	**SCSI DMA DONE ENABLE**: When set, this bit will cause the INT* signal (Pin 17) to be asserted low when the SCSI DMA DONE bit (Register 53H, Bit 5) is set.
Bit 1	**SCSI ARBITRATION DETECTED ENABLE**: When set, this bit will cause the INT* signal (Pin 17) to be asserted low when the SCSI ARBITRATION DETECTED bit (Register 40H/60H, Bit 1) is set.
Bit 2	**SCSI SELECTION PHASE DETECTED ENABLE**: When set, this bit will cause the INT* signal (Pin 17) to be asserted low when the SCSI SELECTION PHASE DETECTED bit (Register 40H/60H, Bit 2) is set.
Bit 3	**SCSI ATTENTION DETECTED ENABLE**: When set, this bit will cause the INT* signal (Pin 17) to be asserted low when the SCSI ATTENTION signal (Pin 68) is asserted low.
Bit 4	**SCSI RESET DETECTED ENABLE**: When set, this bit will cause the INT* signal (Pin 17) to be asserted low when the SCSI RESET signal (Pin 72) is asserted low.
Bit 5	**SCSI PARITY ERROR ENABLE**: When set, this bit will cause the INT* signal (Pin 17) to be asserted low when the SCSI PARITY ERROR bit (Register 40H/60H, Bit 5) is set.
Bit 6	**RESERVED.**
Bit 7	**RESERVED.**

6.3 52H – SCSI Selection Control (Read/Write)

This register is used for Arbitration, Reselection, and SCSI Reset status and control.

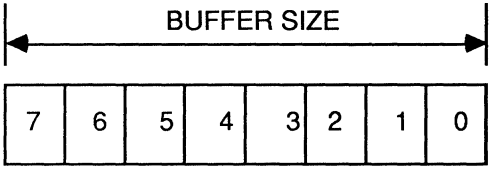
Bit 0	**ARBITRATION**: When this bit is set, the CL-SH250 arbitration logic is enabled to start the arbitration process. The status read from this bit is high when the CL-SH250 is actively arbitrating on the SCSI bus. The read status of this bit is cleared to a low when the SCSI RESET signal (Pin 72) is asserted low, or if the SCSI SELECT signal (Pin 76) was asserted low. The write state of this bit is cleared by a Reset condition or explicitly by writing a 0 to this bit. The SELECT IN bit (Bit 4) and the SELECT OUT bit (Bit 6) have no affect on this bit. The CL-SH250 will remain enabled to retry arbitration as long as this state is not cleared.
Bit 1	**SCSI RESET DETECTED**: This bit reflects SCSI RESET (Pin 72) history. This bit is set when the SCSI RESET signal (Pin 72) is asserted low. The reset event will be latched here, and the latch will be cleared by a microcontroller read of this register. (Read Only)
Bit 2	**SELECTION PHASE ACTIVE**: When the SCSI bus is in the SCSI Selection phase, this bit is set. The SCSI bus is in the SCSI Selection phase when the SCSI SELECT signal (Pin 76) is asserted low, the SCSI BUSY signal (Pin 69) is not asserted, and the SCSI INPUT/OUTPUT signal (Pin 79) is not asserted. (Read Only)
Bit 3	**BUS OUT ENABLE**: When this bit is set, the CL–SH250 will drive the contents of the internal SCSI register on to the SCSI DATA BUS (Pins 52-54, 57, 59-62). If parity is enabled, it will be gated to the SCSI DATA BUS PARITY signal (Pin 64). This bit is reset when the SCSI RESET signal (Pin 72) is asserted low.
Bit 4	**SELECT IN**: This bit reflects the state of the SCSI SELECT signal (Pin 76). (Read Only)
Bit 5	**BUSY IN**: This bit reflects the state of the SCSI BUSY signal (Pin 69). (Read Only)
Bit 6	**SELECT OUT**: When this bit is set, the SCSI SELECT signal (Pin 76) is asserted low if the ENABLE TARGET bit (Register 53H, Bit 7) is set.
Bit 7	**BUSY OUT**: When this bit is set, the SCSI BUSY signal (Pin 69) is asserted low if the ENABLE TARGET bit (Register 53H, Bit 7) is set.

6.4 53H – DMA Control (Read/Write)

This register starts DMA operations and defines data transfer direction for both the host and the disk.

Bit 0	**REQ**: (Request) When this bit is set, the SCSI REQUEST signal (Pin 78) is asserted low. (Note that there is no hardware protection against the microcontroller using this bit during SCSI DMA and subsequent information loss.) Reading this bit reflects the state of the SCSI REQUEST signal.
Bit 1	**SCSI ACKNOWLEDGE STATUS**: This bit indicates the state of the SCSI ACKNOWLEDGE signal (Pin 70). (Read Only)
Bit 2	**SCSI WRITE ENABLE**: Setting this bit will start DMA transfer from the SCSI bus to the buffer memory. In addition, the ROP/WOP* bit (Bit 4) must be reset to a logical 0 when this bit is set.
Bit 3	**SCSI READ ENABLE**: Setting this bit will start DMA transfer from the buffer memory to the SCSI bus. In addition, the ROP/WOP* bit (Bit 4) must be set to a logical 1 when this bit is set.
Bit 4	**ROP/WOP***: Set this bit for a Disk Read operation. This will cause data transfer from the disk to buffer memory. With the SCSI READ ENABLE bit (Bit 3) set, data is transferred from the buffer memory to the SCSI bus. Reset this bit for a Disk Write operation. This will cause data transfer from the buffer memory to the disk. With the SCSI WRITE ENABLE bit (Bit 2) set, data is transferred from the SCSI bus to buffer memory.
Bit 5	**SCSI DMA DONE:** When this bit is set, it indicates a completion of the SCSI transfer cycle. This occurs when the SCSI STOP POINTER Registers (5EH and 5FH) are equal to the appropriate Host Address Pointers. During a disk read operation, the Stop Pointer will be equal to the READ ADDRESS POINTER Registers (5AH and 5BH). During a disk write operation, the Stop Pointer will be equal to the WRITE ADDRESS POINTER Registers (5CH and 5DH). This bit is set whenever the SCSI WRITE ENABLE (Bit 2) or the SCSI READ ENABLE are deasserted (Read Only)
Bit 6	**PARITY ERROR**: This bit indicates a Parity Error on the SCSI data bus. In DMA mode, this bit is set whenever the SCSI ACKNOWLEDGE signal (Pin 70) is asserted low, the SCSI REQUEST signal (Pin 78) goes from asserted low to deasserted high, there is a Parity error on the SCSI DATA BUS (Pins 52-54, 57, 59-62), and parity is enabled (the SCSI PARITY ENABLE bit — Register 58H, Bit 2 — is set). In Programmed I/O (PIO) mode, this bit is set on reading the SCSI BUS ACCESS Register (50H) if there is a SCSI Parity error and if parity is enabled (the SCSI PARITY ENABLE bit is set). This bit is cleared whenever this register is read by the local microcontroller. When the SCSI SELECT signal (Pin 76) is asserted low, this status is switched from the Parity error latch to direct SCSI Parity. This is for checking parity during the SCSI Selection phase.
Bit 7	**ENABLE TARGET**: Set this bit to assert SCSI outputs on SCSI phase and handshake signals. This bit is reset when the SCSI RESET signal (Pin 72) is asserted low.

6.5 54H – Buffer Size (Read/Write)



00H = 256 BYTES
01H = 512 BYTES
03H = 1K BYTES
07H = 2K BYTES
0FH = 4K BYTES
1FH = 8K BYTES
3FH = 16K BYTES
7FH = 32K BYTES
FFH = 64K BYTES

Bits 0-7	This register specifies the size of the physical buffer memory (in bytes). The codes for a given buffer size are in the table above. The upper byte of the SCSI STOP POINTER (Register 5FH) is bit compared with the upper byte of the appropriate Host Address Pointer (the READ ADDRESS POINTER (RAP — Registers 5AH and 5BH), or the WRITE ADDRESS POINTER (WAP — Registers 5CH and 5DH). The result of the bit compare is logically 'ANDed' with the contents of this register. Bit locations that are zero in this register have the bit compare results masked. After the bit compare masking when the SCSI STOP POINTER (Registers 5EH and 5FH) equals the appropriate Host Address Pointer (the READ ADDRESS POINTER (RAP — Registers 5AH and 5BH), or the WRITE ADDRESS POINTER (WAP — Registers 5CH and 5DH), the DMA transfer is terminated and the RAP or WAP will be pointing to one byte higher than the SCSI STOP POINTER. The SCSI DMA DONE bit (Register 40H/60H, Bit 0 and Register 53H, Bit 5) will be set.

6.6 58H – SCSI Mode Control (Read/Write)

Bits [3-1] are reset and Bit 0 is set by either the assertion of the RST* signal (Pin 40) or by setting Register 59, Bit 0.

Bit 0	**SCSI CLOCK PRESCALER ENABLE**: When this bit is set, the SYSCLK division set in Register 7FH is divided by two. This only affects the timing for SCSI Arbitration logic. The period for the SCSI clock timing should be between 200 and 400 ns. The buffer timing on the CL-SH250, when synchronized to the internal SYSCLK, is not affected by this bit.
Bit 1	**MOE* DISABLE**: When this bit is set to logical 1, the MOE* signal (Pin 15) is disabled from being asserted low. This is intended to support switch reads (via Register 70H) on the buffer memory data bus.
Bit 2	**SCSI PARITY ENABLE**: Setting this bit enables the SCSI Parity circuit. The CL–SH250 generates and checks for odd parity. When this bit is set, SCSI Parity will be enabled when the SCSI DATA BUS Out signal (Pins 52-54, 57, 59-62) is asserted low. When the SCSI data bus is enabled, the SCSI Parity will be evaluated and the parity error will be latched (microcontroller-readable at Register 53H, Bit 6) at the rising (trailing) edge of the SCSI REQUEST signal (Pin 78) with the SCSI ACKNOWLEDGE signal (Pin 70) asserted low (and the SCSI INPUT/OUTPUT signal (Pin 79) asserted low). Direct SCSI Parity will be available at Register 53H, Bit 6 whenever the SCSI SELECT signal (Pin 76) is asserted low.
Bit 3	**SCSI TRISTATE ENABLE**: Setting this bit enables the tristate capability of the following signals: SCSI DATA BUS (Pins 52-54, 57, 59-62), SCSI DATA BUS PARITY (Pin 64), SCSI MESSAGE (Pin 73), SCSI COMMAND/DATA (Pin 77), SCSI REQUEST (Pin 78), and SCSI INPUT/OUTPUT (Pin 79).
Bits 4-7	**RESERVED**.

6.7 59H Buffer Manager / SCSI Reset Control (Read/Write)

Any write to Register 59H resets the READ ADDRESS POINTER (RAP) Registers (5AH and 5BH), the WRITE ADDRESS POINTER (WAP) Registers (5CH and 5DH), and sets the SCSI STOP POINTER Registers (5EH and 5FH).

Bit 0	**BUFFER MANAGER RESET**: Setting this bit holds all registers associated with the Buffer Manager and SCSI functions in reset state until this bit is reset. This bit is also set when the RST* signal (Pin 40) is asserted low.
Bits 1-7	**RESERVED**.

6.8 5AH – Read Address Pointer (RAPL) [0:7] (Read/Write)

Registers 5AH and 5BH are the buffer memory address registers for buffer memory read access. (16 bits)

Bits 0-7	These bits are the low-order byte of the buffer memory address for read access. This register is reset when the RST* signal (Pin 40) is asserted low, when the microcontroller writes to the BUFFER MANAGER/SCSI RESET CONTROL Register (59H), or when the BUFFER MANAGER RESET bit (Register 59H, Bit 0) is set.

6.9 5BH – Read Address Pointer (RAPH) [8:15] (Read/Write)

Registers 5AH and 5BH are the buffer memory address registers for buffer memory read access. (16 bits)

Bits 0-7	These bits are the high-order byte of the buffer memory address for read access. This register is reset when the RST* signal (Pin 40) is asserted low, when the microcontroller writes to the BUFFER MANAGER/SCSI RESET CONTROL Register (59H), or when the BUFFER MANAGER RESET bit (Register 59H, Bit 0) is set.

6.10 5CH – Write Address Pointer (WAPL) [0:7] (Read/Write)

Registers 5CH and 5DH are the buffer memory address registers for buffer memory write access. (16 bits)

Bits 0-7	These bits are the low-order byte of the buffer memory address for write access. This register is reset when the RST* signal (Pin 40) is asserted low, when the microcontroller writes to the BUFFER MANAGER/SCSI RESET CONTROL Register (59H), or when the BUFFER MANAGER RESET bit (Register 59H, Bit 0) is set.

6.11 5DH – Write Address Pointer (WAPH) [8:15] (Read/Write)

Registers 5CH and 5DH are the buffer memory address registers for buffer memory write access. (16 bits)

Bits 0-7	These bits are the high-order byte of the buffer memory address for write access. This register is reset when the RST* signal (Pin 40) is asserted low, when the microcontroller writes to the BUFFER MANAGER/SCSI RESET CONTROL Register (59H), or when the BUFFER MANAGER RESET bit (Register 59H, Bit 0) is set.

6.12 5EH – SCSI Stop Pointer (SCSI-SPL) [0:7] (Read/Write)

This pointer is used to detect the end of a SCSI data transfer. The SCSI STOP POINTER (SCSI-SP) (Registers 5EH and 5FH) is compared with the READ or WRITE ADDRESS POINTER (RAP/WAP) (Registers 5AH or 5CH) whose high-order bits are enabled by Register 54H. When they are equal, the SCSI DMA DONE bit (Register 53H, Bit 5) is set, and the DMA Req/Ack cycle is halted. If a new high-order SCSI STOP POINTER is set, a new DMA cycle will begin again if the appropriate SCSI READ ENABLE bit (Register 53H, Bit 3) or the SCSI WRITE ENABLE bit (Register 53H, Bit 2) is still set. Register 5EH and 5FH are set when the SCSI RESET signal (Pin 72) is asserted low (16 bits).

Bits 0-7	These bits are the low-order byte of the SCSI STOP POINTER.

6.13 5FH – SCSI Stop Pointer (SCSI-SPH) [8:15] (Read/Write)

Bits 0-7	These bits are the high-order byte of the SCSI STOP POINTER. If the SCSI READ ENABLE or the SCSI WRITE ENABLE bit (Register 53H, Bit 3 or 2 respectively) is set, writing to this register will restart SCSI transfer.

6.14 7EH – SCSI Information Phase Control (Read/Write)

Bit 0	**SCSI INPUT/OUTPUT***: Writing to this address stores a value which is asserted on the SCSI INPUT/OUTPUT signal (Pin 79) when the ENABLE TARGET bit (Register 53H, Bit 7) is set. Reading this address reads the status of the SCSI INPUT/OUTPUT signal (Pin 79). This bit is a logical inversion of the state of the SCSI bus signal. When this bit is set to logical 1, the SCSI INPUT/OUTPUT signal (Pin 79) is asserted low.
Bit 1	**SCSI COMMAND/DATA***: Writing to this address stores a value which is asserted on the SCSI COMMAND/DATA signal (Pin 77) when the ENABLE TARGET bit (Register 53H, Bit 7) is set. Reading this address reads the status of the SCSI COMMAND/DATA signal (Pin 77). This bit is the logical inversion of the state of the SCSI bus signal. When this bit is set to logical 1, the SCSI COMMAND/DATA signal (Pin 77) is asserted low.
Bit 2	**SCSI MESSAGE**: Writing to this address stores a value which is asserted on the SCSI MESSAGE signal (Pin 73) when the ENABLE TARGET bit (Register 53H, Bit 7) is set. Reading this address reads the status of the SCSI MESSAGE signal (Pin 73).
Bit 3	**SCSI ATTENTION DETECTED**: This bit gets set when the SCSI ATTENTION signal (Pin 68) is asserted low. It will be reset by a microcontroller read of this register.
Bit 4	**SEQUENCER INPUT**: This bit indicates the status of the INPUT signal (Pin 36). If the ALTERNATE BRANCH SELECTION MODE ENABLE bit (Register 77H, Bit 6) is set, then the status of the Current Sequencer Word's CONTROL FIELD, Bit 2, is indirectly read.
Bit 5	**SEQUENCER OUTPUT**: This bit indicates the status of the Current Sequencer Word CONTROL FIELD, Bit 2.
Bit 6	**SCSI ATTENTION**: This bit is the logical inversion of the state of the SCSI ATTENTION signal (Pin 68).
Bit 7	**SCSI RESET**: This bit is the logical inversion of the SCSI RESET signal (Pin 72).

7.0 FORMATTER REGISTERS

7.1 41H (OR 61H) – Disk Interrupt Status (Read Only)

A microcontroller read of this register will reset any bits that were set except Bit 7. Bits 0-6 are also reset when the RST* signal (Pin 40) is asserted low, or when the FORMATTER RESET bit (Register 71H, Bit 5) is set.

Bit 0	**INDEX PAST**: This bit is set by the rising (leading) edge of the INDEX pulse from the disk. This bit is the same as Register 7AH, Bit 0. (A microcontroller read of this register does not reset this status, reading Register 7AH does).
Bit 1	**SECTOR PAST**: This bit is set by the rising (leading) edge of the WAM*/AMD*/SECTOR pulse from the disk. This bit is the same as Register 7AH, Bit 1. (A microcontroller read of this register does not reset this status, reading Register 7AH does).
Bit 2	**INPUT DETECTED**: This bit will be set by the rising (leading) edge of the INPUT signal (Pin 36). This bit will be cleared by a microcontroller read of this register.
Bit 3	**SEQUENCER STOPPED:** This bit indicates that the Sequencer is stopped. The ECC contents have not been reset. The READ GATE signal (Pin 43) and the WRITE GATE signal (Pin 44) are deasserted. This bit is the same as Register 79H, Bit 4.
Bit 4	**ECC ERROR**: This bit will be set after the last ECC data bit is read if there is a non-zero ECC syndrome indicating a data error. This bit is the same as Register 79H, Bit 2.
Bit 5	**DATA TRANSFER DETECTED**: This bit will be set by the rising (leading) edge of the DATA TRANSFER STATUS bit (Register 79H, Bit 6). This bit will be cleared by a microcontroller read of this register.
Bit 6	**SEQUENCER OUTPUT DETECTED**: This bit will be set by the rising (leading) edge of the OUTPUT signal (Pin 47). This bit will be cleared by a microcontroller read of this register.
Bit 7	**SCSI INTERRUPT ACTIVITY**: This bit is the logical-OR of the bits in the SCSI INTERRUPT STATUS Register (40H/60H).

7.2 43H (OR 63H) – Disk Interrupt Enable (Read/Write)

Bit 0	**INDEX ENABLE**: When set, this bit will cause the INT* signal (Pin 17) to be asserted low when the INDEX signal (Pin 37) is asserted.
Bit 1	**SECTOR ENABLE**: When set, this bit will cause the INT* signal (Pin 17) to be asserted low when the SECTOR signal (Pin 39) is asserted.
Bit 2	**INPUT DETECTED ENABLE**: When set, this bit will cause the INT* signal (Pin 17) to be asserted low when the INPUT signal (Pin 36) is asserted.
Bit 3	**SEQUENCER STOPPED ENABLE**: When set, this bit will cause the INT* signal (Pin 17) to be asserted when the SEQUENCER STOPPED bit (Register 79H, Bit 4) is set.
Bit 4	**ECC ERROR ENABLE**: When set, this bit will cause the INT* signal (Pin 17) to be asserted low when the ECC ERROR bit (Register 79H, Bit 2) is set.
Bit 5	**DATA TRANSFER DETECTED ENABLE**: When set, this bit will cause the INT* signal (Pin 17) to be asserted low when the DATA TRANSFER STATUS bit (Register 79H, Bit 6) is set.
Bit 6	**SEQUENCER OUTPUT DETECTED ENABLE**: When set, this bit will cause the INT* signal (Pin 17) to be asserted low when the OUTPUT signal (Pin 47) is asserted.
Bit 7	**RESERVED.**

7.3 4DH – Shadow Latch (Read Only)

Bits 0-7	This is the data latch register for Register 70H read access. When the microcontroller reads Register 70H, the content of the buffer memory data bus will be captured in this register. This register is reset when the RST* signal (Pin 40) is asserted low, or when the FORMATTER RESET bit (Register 71H, Bit 5) is set.

7.4 4EH – Sector Size (Read/Write)

Bits 0-7	Writing to this register sets the number of 256 byte data blocks to be transferred by the Disk Formatter, when the INHIBIT CARRY bit (Register 7AH, Bit 7) is used. The value programmed should be one less than the number of underflows of the Current Sequencer Word [COUNT FIELD] that will be inhibited. If this register is set (or reset) to 00H, the Sequencer will not go to the next WCS word if the INHIBIT CARRY bit (Register 7AH, Bit 7) is set. For a 532-byte Sector Data field, set the COUNT FIELD of the WCS to 13H, set this register to 01H, and set the INHIBIT CARRY bit (Register 7AH, Bit 7). For a 4096-byte Sector Data field, set the COUNT FIELD of the WCS to FFH, set this register to 0EH, and set the INHIBIT CARRY bit (Register 7AH, Bit 7).

7.5 71H - ECC Control (Read/Write)

This is a control register for ECC. Bit 5 (which can be set from the RST* signal (Pin 40) or from the microcontroller) is the Disk Formatter Reset.

Bit 0	**ECC SYNDROME REVERSE /CORRECT CONTROL**: Setting this bit will select the correction operation. Resetting it will select the ECC Syndrome Reversal function. To start any of these functions the ECC SHIFT CONTROL bit (Bit 1) should be set.
Bit 1	**ECC SHIFT CONTROL**: Setting this bit starts the function selected in ECC SYNDROME REVERSE/CORRECT CONTROL (Bit 0). If the ECC SYNDROME REVERSE/CORRECT CONTROL bit (Bit 0) is reset, setting this bit will start shifting data from the ECC CORRECTION SHIFT-REGISTER/COUNTER (Register 72H) in to the ECC circuit. This bit is cleared automatically after the shift is completed. If the ECC SYNDROME REVERSE/CORRECT CONTROL bit (Bit 0) is set, the correction operation is selected and setting this bit will start the correction process. In this case, this bit is cleared if a correctable error is found, or the ECC circuit is shifted 256 bytes. ECC CORRECTION SHIFT REGISTER/COUNTER (Register 72H) is a byte counter and, in case of correctable error, will provide the error offset. Note that all shifts are performed on byte boundries.
Bit 2	**DISABLE ECC FEEDBACK**: When this bit is set, the ECC circuit will function as a shift register.
Bit 3	**CLEAR ECC**: The ECC syndrome will be cleared when this bit is set and no Read or Write operation is in progress. If this bit is set during a Read or Write opeartion, the ECC syndrome will be cleared at the end of that operation.
Bit 4	**ENABLE SECTOR BRANCH**: When set, this bit enables the SECTOR input (Pin 39) as a condition for Sequencer branching along with the INDEX input (Pin 37). Consequently, Sequencer branches may begin at INDEX or SECTOR.
Bit 5	**FORMATTER RESET**: When the RST* signal (Pin 40) is asserted low, this bit is set and a hardware Reset condition is generated. When the microcontroller sets this bit, a software Reset condition is generated. Either Reset condition will stop all operations within the chip, and deassert all output-only pins. In addition, a hardware Reset condition will reset all internal registers. The software Reset condition will reset all registers except 7DH-7FH and will change the NRZ signal (Pin 46), the WAM*/AMD*/SECTOR signal (Pin 39), and AD0-AD7 (Pins 22-23,27,30-34) to a high-impedance state. In either case, the CL–SH250 will remain in the Reset condition as long as this bit is set, and the Reset condition will be removed only when the microcontroller clears this bit.
Bit 6	**RESERVED.**
Bit 7	**ECC POLYNOMIAL DIRECTION**: When reset, this bit selects the forward polynomial. When set, this bit selects the reverse polynomial for the correction process.

7.6 72H – ECC Correction Shift-Register/Counter (Read/Write)

Bits 0-7	When the ECC SYNDROME REVERSAL/CORRECTION CONTROL bit (Register 71H, Bit 0) is set, this is an eight-bit counter. When the ECC SYNDROME REVERSAL/ CORRECTION CONTROL bit is reset, this is a shift register.

7.7 73H – ECC Status [31:24] / ECC Status [7:0] (Read Only)

Bits 0-7	**ECC STATUS BITS [31:24]/[7:0]**: In the 56-bit computer-generated code mode, these are ECC Bits 31:24. In the Fire Code mode, these are ECC Bits 7:0. The status of the bits in this register will only be valid when ECC is not cycling. This register is set when the RST* signal (Pin 40) is asserted low, or when the FORMATTER RESET bit (Register 71H, Bit 5) is set.

7.8 74H – ECC Status [39:32]/ECC Status [15:8] (Read Only)

Bits 0-7	**ECC STATUS BITS [39:32]/[15:8]**: In the 56-bit computer-generated code mode, these are ECC Bits 39:32. In the Fire Code mode, these are ECC Bits 15:8. The status of the bits in this register will only be valid when ECC is not cycling. This register is set when the RST* signal (Pin 40) is asserted low, or when the FORMATTER RESET bit (Register 71H, Bit 5) is set.

7.9 75H – ECC Status [47:40]/ECC Status [23:16] (Read Only)

Bits 0-7	**ECC STATUS BITS [47:40]/[23:16]**: In the 56-bit computer-generated code mode, these are ECC Bits 47:40. In the Fire Code mode, these are ECC Bits 23:16. The status of the bits in this register will only be valid when ECC is not cycling. This register is set when the RST* signal (Pin 40) is asserted low, or when the FORMATTER RESET bit (Register 71H, Bit 5) is set.

7.10 76H – ECC Status [55:48]/ECC Status [31:24] (Read Only)

Bits 0-7	**ECC STATUS BITS [55:48]/[31:24]**: In the 56-bit computer-generated code mode, these are ECC Bits 55:48. In the Fire Code mode, these are ECC Bits 31:24. The status of the bits in this register will only be valid when ECC is not cycling. This register is set when the RST* signal (Pin 40) is asserted low, or when the FORMATTER RESET bit (Register 71H, Bit 5) is set.

7.11 77H – Formatter/Buffer Manager Mode Selection (Read/Write)

This register is reset by the assertion of the RST* signal (Pin 40).

Bit 0 **DISABLE READ REFERENCE FILTER:** When this bit is reset, the Read/Reference Filter is enabled. This provides some protection against ENDEC's which produce glitches when changing clock sources. The maximum Read/Reference clock frequency of the CL-SH250 is limited by this filter. When this bit is set, the Read/Reference Filter is disabled. This increases the maximum Read/Reference Clock frequency for the CL-SH250. See the AC timing characteristics for specifications.

Bit 1 **INTERRUPT REGISTER ACCESS ENABLE:** When set, this bit allows the four interrupt registers to be accessed by the local microcontroller. The interrupt address space is specified by Bit 2. When this bit is reset addresses 40H - 47H and 60H - 6FH are available for external system use.

Bit 2 **INTERRUPT REGISTER DECODE SELECT:** When this bit is set (and Bit 1 is set), the interrupt address space is 40H-43H; however, the CL–SH250 will decode addresses 40H-47H (Addresses 60H - 6FH are available for external system use). When this bit is reset (and Bit 1 is set), the interrupt address space is 60H-63H; however, the CL-SH250 will decode addresses 60H-6FH (Addresses 40H - 47H are available for external system use.).

Interrupt Register Decode Table

Reg. 77H Bit 1	Bit 2	CL–SH250 Decodes:	Available to the MPU
0	x	Neither	Reg. 40H–47H and 60H–67H
1	1	Decodes Reg. 40H-47H	Reg. 60H-67H
1	0	Decodes Reg. 60H–67H	Reg. 40H-47H

Bit 3 **INTERRUPT ENABLE:** When set, this bit enables interrupt capability. The individual sources of interrupt can still be disabled by the Interrupt Mask Registers (Registers 42H/62H and 43H/63H).

Bit 4 **INTERRUPT PIN PULL-UP DISABLE:** When set, this bit disables the pull-up on the INT* signal (Pin 17), leaving an open-drain output. This is intended to support multiple interrupt sources.

Bit 5 **FIRE-CODE MODE:** When this bit is reset, the 56-bit computer generated polynomial is enabled. The ECC circuitry (or linear feedback shift register) is initialized to all logical one's before use. When this bit is set, the 32-bit Fire Code polynomial is enabled. The ECC circuitry is initialized to all logical zero's before use.

Bit 6 **ALTERNATE BRANCH SELECTION MODE ENABLE:** Setting this bit enables an alternate set of branch conditions. This bit is reset when the RST* signal (Pin 40) is asserted low. This bit controls the definition of Bit 3 of the CONTROL FIELD in the Current Sequencer Word. If this bit is reset, Bit 3 in the CONTROL FIELD of the Current Sequencer Word is defined as INVALID NRZ to remain backward compatible with existing firmware. If this bit is set, Bit 3 of the CONTROL FIELD in the Current Sequencer Word is defined as ALTERNATE BRANCH CONDITION ENABLE. In that mode, when Bit 3 of the CONTROL FIELD in the Current Sequencer Word is set, an alternate set of branch conditions is enabled.

7.11 77H – Formatter/Buffer Manager Mode Selection (Read/Write) *(cont.)*

This register is reset by the assertion of the RST* signal (Pin 40).

Bit 7	**HARD/SOFT* SECTOR MODE CONTROL:** When this bit is set to logical 1, the Hard Sector mode is selected. In this mode, the WAM*/AMD*/SECTOR signal (Pin 39) functions as a SECTOR input signal. The SECTOR PAST bit (Register 7AH, Bit 1) and Branch on Sector circuit will be triggered by the rising (leading) edge of the SECTOR signal. When this bit is reset to logical 0, the Soft Sector mode is selected. In this mode, the WAM*/AMD*/SECTOR signal (Pin 39) functions as the WAM*/AMD* I/O signal. The SECTOR PAST bit (Register 7AH, Bit 1) and Branch on Sector circuit will be triggered by the rising (leading) edge of the WAM*/AMD*/SECTOR signal.

7.12 78H – Next Active Sequencer Address (Read Only)

This register specifies the next executable address for the Sequencer.

Bits 0-4	**NEXT ACTIVE SEQUENCER ADDRESS:** Bits 0-4 provide the next WCS address to be executed by the Sequencer. This address could be the contents of the SEQUENCER START ADDRESS (Register 79H), or the BRANCH ADDRESS (Register 78H), or the CURRENT SEQUENCER WORD [NEXT ADDRESS] (Register 49H).
Bits 5-7	**RESERVED.**

7.13 78H – Branch Address (Write Only)

Bits 0-4	The Sequencer will jump to the address specified in Bits 0-4 when a branch condition is programmed and met.
Bits 5-7	**RESERVED.**

7.14 79H – Sequencer Status (Read Only)

Bit 0	**COMPARE EQUAL**: This bit is set when the result of the compare operation is equal. The comparison is done between the Read Data and either the buffer memory data or the WCS DATA FIELD (as determined by the SEARCH OPERATION bit – Register 7AH, Bit 4), on all bytes where comparison was enabled in the COMPARE ENABLE bit (Bit 1) of the WCS CONTROL FIELD. COMPARE EQUAL is not valid until the Sequencer is in the ECC FIELD.
Bit 1	**COMPARE LOW**: This bit is the same as Bit 0 above, but is set when the Read Data is lower.
Bit 2	**ECC ERROR**: This bit will be set after the last ECC data bit is read if there is a non-zero ECC syndrome indicating a data error. This bit is the same as Register 41H/61H, Bit 4.
Bit 3	**CORRECTABLE ERROR FOUND**: This bit indicates that the interactive ECC correction circuit has found a correctable error and has shifted the error burst to a byte boundary. This bit is valid after the ECC SHIFT CONTROL bit (Register 71H, Bit 1) has gone from set to reset.
Bit 4	**SEQUENCER STOPPED**: This bit indicates that the Sequencer is stopped. The ECC contents have not been reset. The READ GATE signal (Pin 43) and the WRITE GATE signal (Pin 44) are deasserted. This bit is the same as Register 41H/61H, Bit 3.
Bit 5	**BRANCH ACTIVE**: This bit is set when a branch condition is met. Reading this register will reset this bit.
Bit 6	**DATA TRANSFER STATUS**: This bit indicates the status of the DATA TRANSFER bit (WCS CONTROL FIELD, Bit 0). This bit is set during data transfer between the buffer memory and the disk.
Bit 7	**AM ACTIVE**: This bit is set when the DATA TRANSFER bit (WCS CONTROL FIELD, Bit 0) is reset and the AM/COUNT bit (WCS COUNT FIELD, Bit 7) is set. It is reset after reading or writing the ECC bytes. The bit is also reset when the Sequencer stops.

7.15 79H – Sequencer Start Address (Write Only)

The Sequencer can be stopped by writing 1FH to this register.

Bits 0-4	**START ADDRESS**: A write to this register will start the Sequencer at the latched address. This register is reset when the RST* signal (Pin 40) is asserted low, or when the FORMATTER RESET bit (Register 71H, Bit 5) is set.
Bits 5-7	**RESERVED**.

7.16 7AH – Operation/Control Status (Read/Write)

Bit 0	**INDEX PAST**: This bit is set by the rising (leading) edge of the INDEX pulse from the disk Reading the register will reset this bit. This bit is the same as Register 41H/61H, Bit 0.
Bit 1	**SECTOR PAST**: This bit is set by the rising (leading) edge of the WAM*/AMD*/SECTOF pulse from the disk. Reading the register will reset this bit. This bit is the same as Registe 41H/61H, Bit 1.
Bit 2	**NRZ DATA IN**: This bit is set when a rising (leading) edge is detected at the NRZ data signal (Pin 46) when the READ GATE signal (Pin 43) is asserted. Reading the registe should reset this bit, but due to the asynchronous relationship between the NRZ signal (Pi 46) and the microcontroller, race conditions may interfere with the reset. It is suggested tha this bit be read until it reports as reset.
Bit 3	**SYNC DETECT**: This bit is set when the CL-SH250 is synchronized to the incoming NRZ data stream after the READ GATE signal (Pin 43) is asserted.
Bit 4	**SEARCH OPERATION**: This bit selects the source of the data for the compare operation When this bit is set, Read Data is compared to buffer memory data. When this bit is reset Read Data is compared to WCS DATA FIELD.
Bit 5	**SUPPRESS TRANSFER**: When this bit is set, serialized or de-serialized data will not be read/written to the buffer memory (disabling the buffer memory access mechanism.) Durinç the Write operation, the NRZ data will be written with the contents of the WCS DATA FIELD During a Read operation, the incoming data will have the ECC verified but no data will be transferred to the buffer memory.
Bit 6	**RESERVED.**
Bit 7	**INHIBIT CARRY**: When this bit is set, the carry/load of the WCS COUNT FIELD for the data transfer will be inhibited. This bit will be automatically reset whenever the Sector Size Counter is zero and there is an underflow from the current COUNT FIELD.

7.17 7BH – WAM Control (Read/Write)

This is the WAM (Write Address Mark) output timing control register.

Bits 0-7	**WRITE ADDRESS MARK CONTROL**: In Soft Sector mode, the WAM*/AMD*/SECTOR signal (Pin 39) will be asserted low for each bit cell time corresponding to the bits set in this register during a Write Address Mark operation. Output at the WAM*/AMD*/SECTOR signal is shifted 3 bits toward LSB at the output. In Hard Sector mode, the signal will not be asserted. This register is reset when the RST* signal (Pin 40) is asserted low.

7.18 7CH – Sync Pattern (Read/Write)

Bits 0-7	**SYNC PATTERN**: This register is to be compared with NRZ read data when the READ GATE signal (Pin 43) and, if in Soft Sector mode, the WAM*/AMD*/SECTOR signal (Pin 39) are asserted. A match between this register and the serial NRZ read data input will set the SYNC DETECT bit (Register 7AH, Bit 3) and will cause the NRZ read data to be gated in to the ECC. Only those bits in this register that are enabled by the CLOCK/SYNC CONTROL Register (7FH) will be used for comparison. In Soft Sector mode, the WAM*/AMD*/SECTOR signal (Pin 39) must also be asserted low for the SYNC DETECT bit (Register 7AH, Bit 3) to be set. This register is reset when the RST* signal (Pin 40) is asserted low.

7.19 7FH – Formatter Stack Read (Read Only)

Bits 0-7	A read of this register reads the last byte that was enabled (by the STACK ENABLE bit, Bit 4 of the WCS CONTROL FIELD) on to the stack. The Address Pointer, in ring fashion, moves around the 8-byte circular stack. As the byte is read, the Address Pointer moves to the previous location. The data during a read is never 'popped' from the stack, it is not lost or removed, a continuous read of eight locations would bring the Address Pointer back around to the original location reading the same data. If 10 bytes in a field were enabled to the stack, the last 8 bytes would be captured as the first two bytes would be overwritten. The first byte read would be the tenth byte enabled on to the stack. In reverse order, all of the last eight bytes could then be read continuously in a circular manner.

7.20 7FH – Clock/Sync Control (Write Only)

This register is reset by the assertion of the RST* signal (Pin 40).

Bits 0-2 **SYNC COMPARE CONTROL**: These bits specify the number of bits to be used in the compare for the sync byte programmed in the SYNC PATTERN Register (7CH).

Bits 2 1 0		Bits 2 1 0	
0 0 0	= Only Bit 7 is compared.	1 0 0	= Only Bits 7:3 are compared.
0 0 1	= Only Bits 7:6 are compared.	1 0 1	= Only Bits 7:2 are compared.
0 1 0	= Only Bits 7:5 are compared.	1 1 0	= Only Bits 7:1 are compared.
0 1 1	= Only Bits 7:4 are compared.	1 1 1	= All Bits are compared.

Bit 3 **RESERVED**.

Bit 4 This bit specifies BUFCLK* frequency during Sequencer data transfer.

0 = 1/2 of RD/REF CLK (Four Window Mode)
1 = 1/4 of RD/REF CLK (Two Window Mode)

Bit 5 **RESERVED**.

Bits 6-7 These bits specify BUFCLK* frequency during non-Sequencer data transfer.

Bits 7 6		Bits 7 6	
0 0	= 1/4 of SYSCLK	1 0	= SYSCLK
0 1	= 1/2 of SYSCLK	1 1	= Not valid

8.0 EXTERNAL ACCESS REGISTER DECODE

8.1 50H – SCSI Bus Access (Read/Write)

Bits 0-7	**SCSI BUS ACCESS**: Register 50H decode allows the microcontroller direct access to the SCSI data bus. This access is available even when the Sequencer is transferring data across the buffer memory data bus. This register stores the data to be written to the SCSI bus when the BUS OUTPUT ENABLE bit (Register 52H, Bit 3) is asserted. A microcontroller read of the SCSI BUS ACCESS Register (50H) reads the information directly from the SCSI data bus.

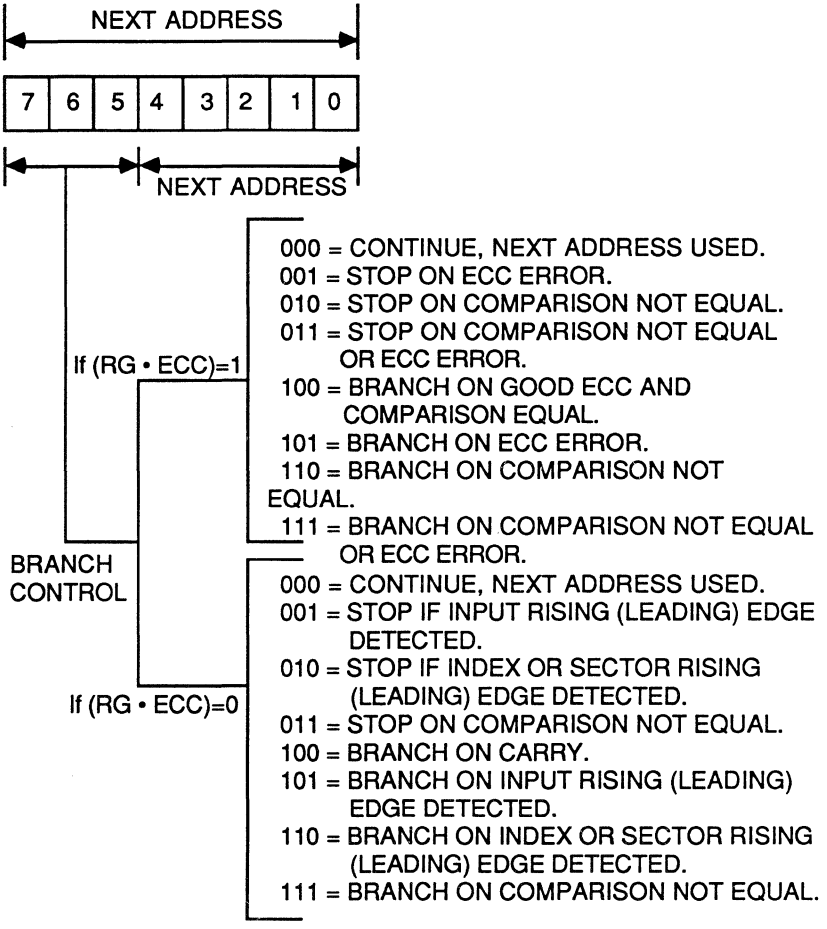
8.2 70H – Buffer Memory Access (Read/Write)

Bits 0-7	**BUFFER MEMORY ACCESS**: Register 70H decode internally bridges the buffer memory data bus and the microcontroller bus (allowing the microcontroller to access the buffer memory) and causes the CL–SH250 to assert the BA0:15 signal (Pins 95-100, 3-4, 6-13), the MOE* signal (Pin 15), and the WE* signal (Pin 16). Read data from the buffer memory will also be latched into the SHADOW LATCH Register (4DH). If the MOE* DISABLE bit (Bit 1) of the SCSI MODE CONTROL Register (58H) is set to logical 1, the MOE* signal (Pin 15) is not asserted so that the microcontroller can read external switch settings on the buffer memory data bus.

9. WRITABLE CONTROL STORE (WCS) FIELDS DESCRIPTIONS

The WCS (addresses 80H-9EH, A0H-BEH, C0H-DEH, and E0H-FEH) may only be written to by the support microcontroller when there is no risk of the contents being accessed by the Sequencer. This is normally true only during long data transfers or when the Sequencer is stopped.

9.1 80H-9EH – Next Address Field (Read/Write)



9.1 80H-9EH – Next Address Field (Read/Write) *(cont.)*

Bits 0-4 **NEXT ADDRESS**: This is the address the Sequencer will go to after the down counter has reached zero and a branch has not been taken. There are 31 possible next-address locations (00H-1EH). Fetching the address 1FH establishes the stopped condition.

Bits 5-7 **BRANCH CONDITION**: All branch conditions are evaluated during the last byte of execution of the Current Sequencer Word.

Branch conditions when both the READ GATE signal (Pin 43) is asserted and the PROCESS ECC bit (Bit 6) of the Current Sequencer Word COUNT FIELD is set:

Bits 7	6	5	
0	0	0	= Continue, next address used.
0	0	1	= Stop on ECC error.
0	1	0	= Stop on comparison not equal
0	1	1	= Stop on comparison not equal or ECC error.
1	0	0	= Branch on good ECC and comparison error.
1	0	1	= Branch on ECC error
1	1	0	= Branch on comparison not equal.
1	1	1	= Branch on comparison not equal or ECC error.

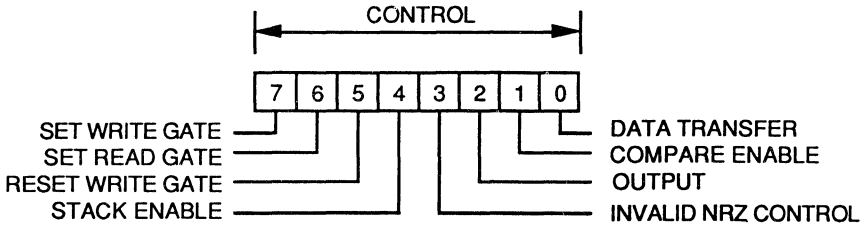
Branch condition when the READ GATE signal (Pin 43) is not asserted or the PROCESS ECC bit (Bit 6) of the Current Sequencer Word COUNT FIELD is reset and the ALTERNATE BRANCH MODE ENABLE bit (Register 77H, Bit 6) is set:

110 = Branch on INDEX and SECTOR rising (leading) edge not detected.

Branch conditions at all other times:

Bits 7	6	5	
0	0	0	= Continue, next address used.
0	0	1	= Stop if INPUT rising (leading) edge detected.
0	1	0	= Stop if INDEX or SECTOR rising (leading) edge detected.
0	1	1	= Stop on comparison not equal.
1	0	0	= Branch on carry.
1	0	1	= Branch on INPUT rising (leading) edge detected.
1	1	0	= Branch on INDEX or SECTOR rising (leading) edge detected.
1	1	1	= Branch on comparison not equal.

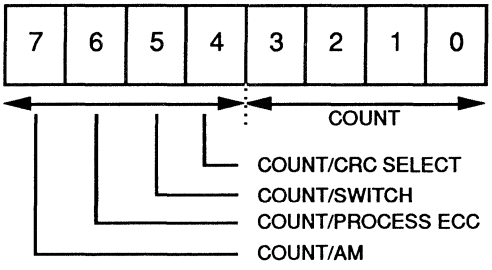
9.2 AOH-BEH - Control Field (READ/WRITE)



Bit 0	**DATA TRANSFER**: When this bit is set, the COUNT FIELD is used as an eight-bit counter. Each byte time that this bit is set, a byte of data will be accessed from the buffer memory if the SUPPRESS TRANSFER bit (Register 7AH, Bit 5) is reset. If the WRITE GATE signal (Pin 44) is asserted, then a byte of data is read from the buffer memory (if the SUPPRESS TRANSFER bit (Register 7AH, Bit 5) is reset) or from the DATA FIELD (if the SUPPRESS TRANSFER bit (Register 7AH, Bit 5) is set), and is serialized and sent to the NRZ pin (Pin 46). If the READ GATE signal (Pin 43) is asserted, then a byte of data is de-serialized from the NRZ pin (Pin 46) and is then written to the buffer memory if the SUPPRESS TRANSFER bit (Register 7AH, Bit 5) is reset. If the SUPPRESS TRANSFER bit (Register 7AH, Bit 5) is set, then no data is written to the buffer memory.
Bit 1	**COMPARE ENABLE**: When this bit is set with the READ GATE signal (Pin 43) asserted, it will allow a comparision between read data and the WCS DATA FIELD, or the buffer memory data (if the SEARCH OPERATION bit is set - Register 7AH, Bit 4).
Bit 2	**OUTPUT**: This bit drives the OUTPUT signal (Pin 47) and is used to synchronize external logic functions to the state of the WCS.
Bit 3	**INVALID NRZ CONTROL**: When this bit is set with the READ GATE signal (Pin 43) asserted, it will block the NRZ data input from being processed.
Bit 4	**STACK ENABLE**: When this bit is set, read data is pushed on the eight-byte recirculating stack.
Bit 5	**RESET WRITE GATE**: This bit is used to deassert the WRITE GATE signal (Pin 44). The WRITE GATE signal (Pin 44) will be deasserted on the last count of the Sequencer word with this bit set. The WRITE GATE signal (Pin 44) is also deasserted when the Sequencer comes to the stopped state.
Bit 6	**SET READ GATE**: The READ GATE signal (Pin 43) will be asserted when the Sequencer word with this bit set is executed. The READ GATE signal (Pin 43) will be deasserted at the end of ECC or when the Sequencer goes to the stopped state. The READ GATE signal (Pin 43) will not be asserted if the WRITE GATE signal (Pin 44) is already asserted.
Bit 7	**SET WRITE GATE**: The WRITE GATE signal (Pin 44) will be asserted when the Sequencer word with this bit set is executed. After this bit is set, WRITE GATE control will be reset by executing a Sequencer word with the RESET WRITE GATE bit (Bit 5) set or when the Sequencer goes to the stopped state. The WRITE GATE signal (Pin 44) will not be asserted if the READ GATE signal (Pin 43) is already asserted.

9.3 C0H-DEH – Count Field (Read/Write)

This is the COUNT FIELD of the WCS word. This sets the initial value of the Sequencer Counter when a new state is entered.



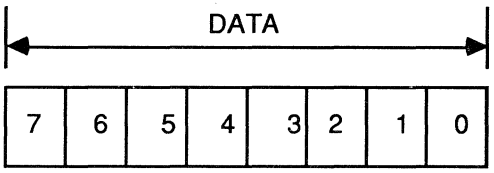
Count Field Functionally

WG On	RG On	Data Transfer	Bit 7	Bit 6	Bit 5	Bit 4	Bits 3-0	Max Count
0	0	0	AM	PROCESS ECC	SWITCH	COUNT	COUNT	32
0	0	1	COUNT	COUNT	COUNT	COUNT	COUNT	256
0	1	0	AM	PROCESS ECC	SWITCH	CRC SELECT	COUNT	16
0	1	1		ILLEGAL				
1	0	0	AM	PROCESS ECC	SWITCH	CRC SELECT	COUNT	16
1	0	1		ILLEGAL				
1	1	0		ILLEGAL				
1	1	1		ILLEGAL				

9.3 C0H-DEH – Count Field (Read/Write) *(cont.)*

Bits 0-3	**COUNT**: These bits are always used for the initial value of the Sequencer byte counter when a new state is entered. When it reaches zero, a new instruction word will be accessed from the Disk Formatter WCS.
Bit 4	**COUNT/CRC SELECT**: In the Current Sequencer Word, when the SET READ GATE and the SET WRITE GATE bits (CONTROL FIELD, Bits 6,7) are reset, or if the DATA TRANSFER bit (CONTROL FIELD, Bit 0) is set, this is a count bit (for a five-bit, or eight-bit count field). (Note that the DATA TRANSFER bit (CONTROL FIELD, Bit 0) set and the SET READ GATE bit (CONTROL FIELD, Bit 6) or the SET WRITE GATE bit (CONTROL FIELD, Bit 7) set is an illegal selection.) If in the Current Sequencer Word either the SET READ GATE (CONTROL FIELD, Bit 6) or the SET WRITE GATE (CONTROL FIELD, Bit 7) bits are set and the DATA TRANSFER bit (CONTROL FIELD, Bit 0) is reset, then the CRC SELECT function is active. With this function active, this bit set initializes the ECC function to the CRC polynomial, and when this bit is cleared, the ECC function is initialized to the 56-bit computer generated polynomial.
Bit 5	**COUNT/SWITCH**: When the DATA TRANSFER bit of the Current Sequencer Word (CONTROL FIELD, Bit 0) is set, this is a count bit (for an eight-bit count field). When the DATA TRANSFER bit is reset, this bit is the SWITCH command. (In SWITCH mode, when this bit is set buffer memory access cycle clock source switches from SYSCLK (Pin 41) to RD/REF CLK (Pin 45)). The source is switched back to SYSCLK at the end of the ECC field.
Bit 6	**COUNT/PROCESS ECC**: When the DATA TRANSFER bit of the Current Sequencer Word (CONTROL FIELD, Bit 0) is set, this is a count bit (for an eight-bit COUNT FIELD). When the DATA TRANSFER bit is reset, this bit treats the incoming NRZ data (if the READ GATE signal (Pin 43) is asserted), or the outgoing NRZ data (if the WRITE GATE signal (Pin 44) is asserted) as an ECC or CRC field.
Bit 7	**COUNT/AM**: When the DATA TRANSFER bit of the Current Sequencer Word (CONTROL FIELD, Bit 0) is set, this is a count bit (for an eight-bit COUNT FIELD). When the DATA TRANSFER bit is reset and the READ GATE signal (Pin 43) is asserted, this bit will set the AM ACTIVE bit (Register 79H, Bit 7). When the DATA TRANSFER bit is reset, and the WRITE GATE signal (Pin 44) is asserted, this bit will set the AM ACTIVE bit and will be used to initialize the CRC/ECC Registers. In the Soft Sector mode (Register 77H, Bit 7 is reset), the WAM* output (Pin 39) will be asserted low as programmed in the WAM CONTROL Register (7BH).

9.4 E0H-FEH – Data Field (Read/Write)



Bits 0-7	**DATA**: This register is the source for all overhead bytes of data used by the device during Write operations. During Read operations, it is one of the operands to the comparison logic. When the DATA TRANSFER bit in the Current Sequencer Word (CONTROL FIELD, Bit 0) is set with the WRITE GATE signal (Pin 44) asserted, the source for write data will be the external buffer memory. When the SUPPRESS TRANSFER bit (Register 7AH, Bit 5) is set with the WRITE GATE signal (Pin 44) asserted, the source for write data will be the content of this register.

10. SEQUENCER REGISTERS DESCRIPTIONS

The WCS word being executed is stored in the Sequencer Registers (Registers 49H-4CH). These registers should only be written by the microcontroller when the Sequencer is stopped. These registers can be read any time.

10.1 49H – Current Sequencer Word - Next Address Field (Read/Write)

This register allows the microcontroller to access the NEXT ADDRESS FIELD of the Current Sequencer Word.

10.2 4AH – Current Sequencer Word - Count Field (Read/Write)

This register allows the microcontroller to access the COUNT FIELD of the Current Sequencer Word.

10.3 4BH – Current Sequencer Word - Control Field (Read/Write)

This register allows the microcontroller to access the CONTROL FIELD of the Current Sequencer Word.

10.4 4CH – Current Sequencer Word - Data Field (Read/Write)

This register allows the microcontroller to access the DATA FIELD of the Current Sequencer Word.

11. ELECTRICAL SPECIFICATION

11.1 Absolute Maximum Ratings

Ambient Temperature Under Bias ..... 0° C to 70° C

Storage Temperature ..... -65° C to 150° C

Voltage On Any Pin With Respect To Ground ..... GND -0.5 to V_{CC} +0.5 Volts

Power Supply Voltage ..... 7 Volts

NOTE: Stress above those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

11.2 DC Characteristics

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{CC}	Power Supply Voltage	4.75	5.25	Vdc	Operating
V_{IL}	Input Low Voltage	-0.5	0.8	Vdc	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5	Vdc	
$V_{OL(1)}$	Output Low Voltage		0.4	Vdc	I_{OL} = 2 mA
$V_{OH(1)}$	Output High Voltage		2.4	Vdc	I_{OH} = – 400µA
$V_{OL(2)}$	Output Low Voltage		0.5	Vdc	I_{OL} = 48mA
I_L	Input Leakage Current	-10	10	µA	0 < V_{IN} <V_{CC}
I_{OZ}	Tri-state Leakage	-10	10	µA	0 < V_{IN} < V_{CC}
I_{CC}	Supply Current		50	mA	Under operating voltage conditions.
C_{IN}	Input Capacitance		10	pF	
C_{OUT}	Output Capacitance		10	pF	

NOTES: (1) All output pins except for SCSI signals.
(2) SCSI outputs.
(3) IOL=4mA for READ GATE (Pin 43) and WRITE GATE (Pin 44).
(4) All unused inputs must be tied to their inactive state to V_{CC} or GND, respectively.

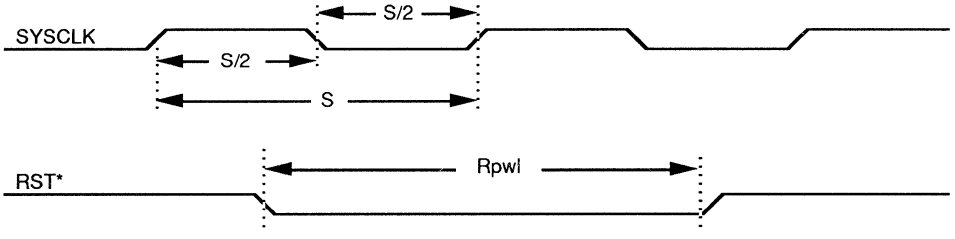
11.3 AC Characteristics

The following timings are operating under the assumption that all non-SCSI outputs will drive one Schottky TTL load in parallel with 50 pF and all inputs are at TTL level. All SCSI outputs will drive a characteristic impedance of 132 ohms and 200 pF. The MIN and MAX timings are conforming to the operating ranges of power supply voltage of 5V ± 5% and ambient temperature of 0° C to 70° C. Clock rise and fall times should be limited to 15% of the clock period.

System Clock Timing Table

SYMBOL	PARAMETER	MIN	MAX	UNITS
S	System Clock Period	41		ns
S/2	System Clock Assert/Deassert	16		ns
Rpwl	RST* low pulse width	100		ns

System Clock Timing:



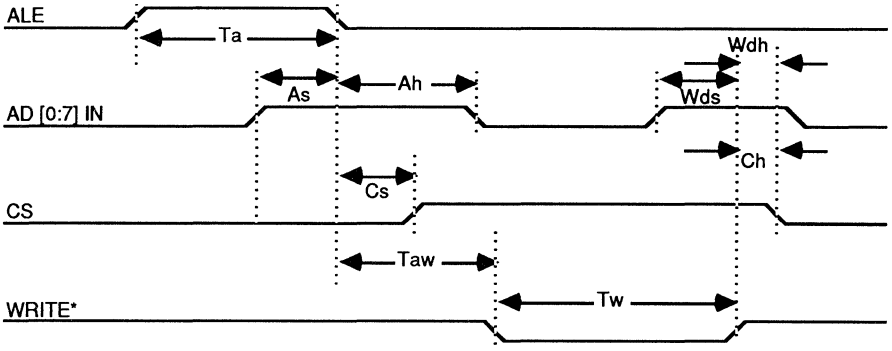
Microcontroller Interface Timing Table

SYMBOL	PARAMETER	MIN	MAX	UNITS
Ta	ALE Width	45		ns
Taw	ALE↓ to WRITE*↓	25		ns
Tar	ALE↓ to READ*↓	25		ns
Tw	WRITE* Width	140		ns
Tr	READ* Width	140		ns
As	Address valid to ALE↓	5		ns
Ah	ALE↓ to Address invalid	20		ns
Cs	ALE↓ to CS valid		5	ns
Ch	READ*↑ or WRITE*↑ to CS↓	0		ns
Wds	Write Data valid to WRITE*↑	55		ns
Wdh	WRITE*↑ to Write Data invalid		10	ns
Tda	READ*↓ to Read Data valid		100	ns
Tdh	READ* ↑ to Read Data invalid	50		ns

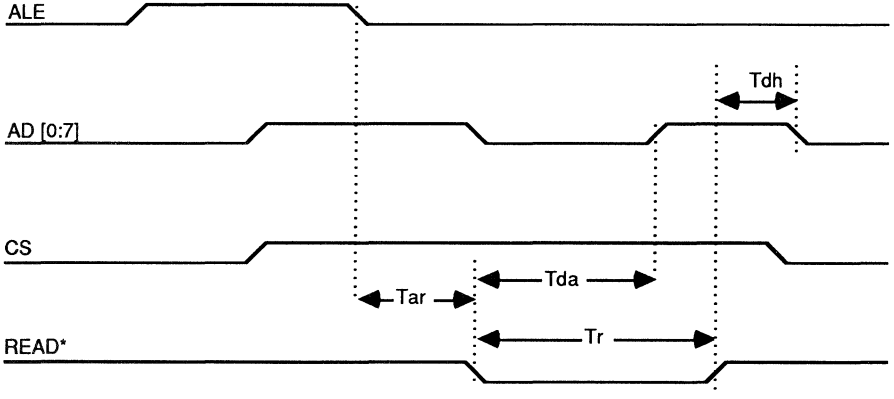
NOTE: ↓ Indicates falling edge. ↑ Indicates rising edge.

MICROCONTROLLER INTERFACE TIMING

Register Write Timing



Register Read Timing

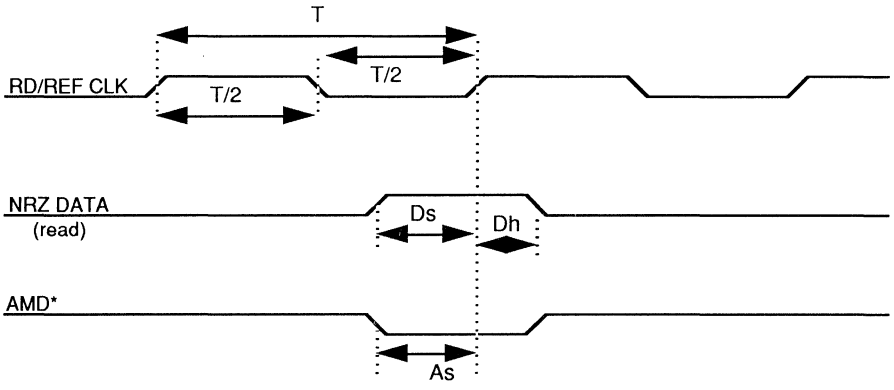


Disk Read/Write Timing Table

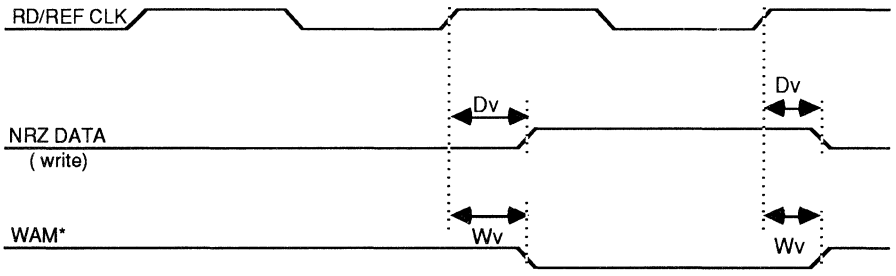
SYMBOL	PARAMETER	Disable Read/ Reference Filters Register 77H Bit 0 Reset MIN	MAX	Disable Read/ Reference Filters Register 77H Bit 0 Set MIN	MAX	UNITS
T	RD/REF CLK Period	62.5		41		ns
T/2	RD/REF CLK Assert-Deassert	23		16		ns
Ds	NRZ valid to RD/REF CLK↑	10		10		ns
Dh	RD/REF CLK↑ to NRZ invalid	5		5		ns
As †	AMD* valid to RD/REF CLK↑	10		10		ns
Dv	RD/REF CLK↑ to NRZ valid	10	25	10	25	ns
Wv †	RD/REF CLK↑ to WAM* valid	10	25	10	25	ns

NOTE: ↑ Indicates rising edge.
† These specifications are only applicable in the Soft Sector mode.

Disk Read Timing



Disk Write Timing



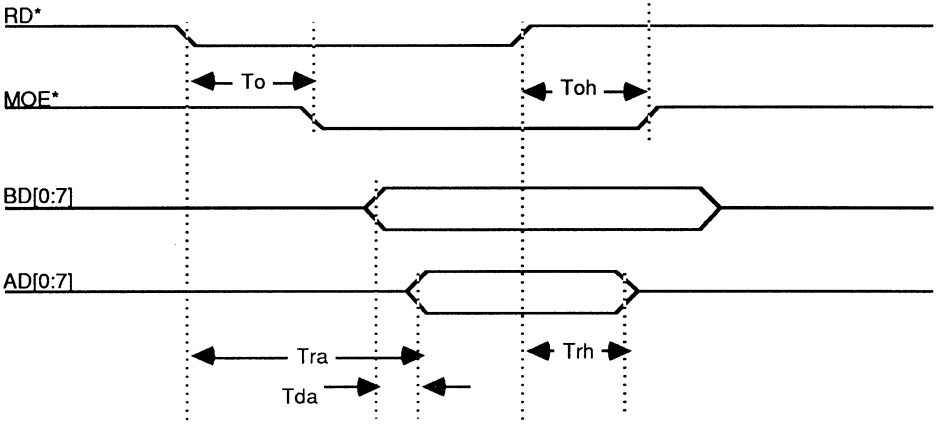
NOTE: NRZ DATA changes after the rising (leading) edge of RD/REF CLK.

Register 70H Timing Table

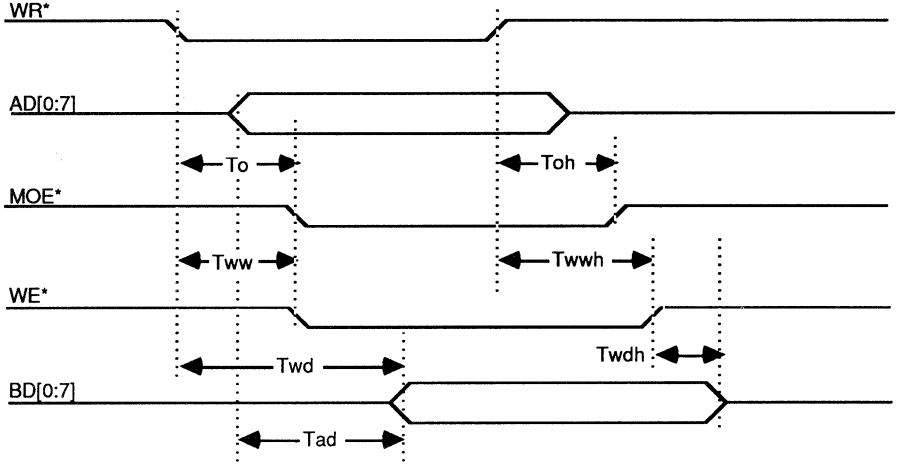
SYMBOL	PARAMETER	MIN	MAX	UNITS
To	RD*↓ or WR*↓ to MOE*↓		40	ns
Tda	BD[0:7] valid to AD[0:7] valid		55	ns
Trh	RD*↑ to ADDRESS/DATA invalid		50	ns
Toh	RD*↑ or WR*↑ to MOE*↑		40	ns
Tww	WR*↓ to WE*↓		40	ns
Tad	AD[0:7] valid to BD[0:7] valid		55	ns
Twwh	WR*↑ to WE*↑		40	ns
Twdh	WE*↑ to BD[0:7] invalid	50		ns

NOTE: ↓ Indicates falling edge. ↑ Indicates rising edge.
Address [0:15] is valid according to ROP/WOP and the contents of the READ ADDRESS POINTER (RAP) Registers (5AH and 5BH) or the WRITE ADDRESS POINTER (WAP) Registers (5CH and 5DH).

Register 70H Read Timing



Register 70H Write Timing



Register 50H Timing Table

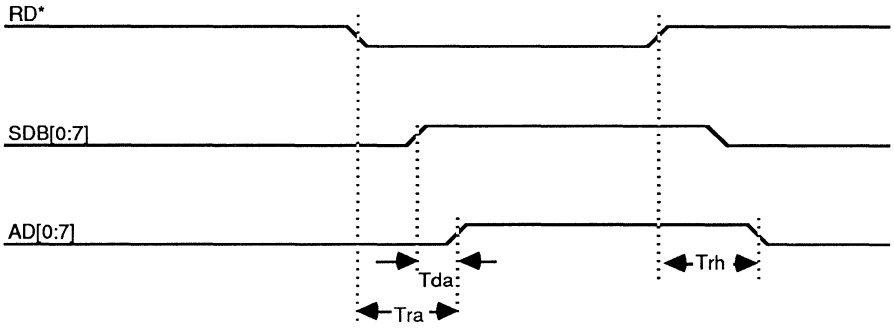
SYMBOL	PARAMETER	MIN	MAX	UNITS
Tra†	RD*↓ to Data Path Established		90	ns
Tda	SDB[0:7] valid to AD[0:7] valid		80	ns
Trh	RD*↑ to ADDRESS/DATA invalid		50	ns
Tad ††	AD[0:7] valid to SDB[0:7] valid		80	ns

NOTES: ↓ Indicates falling edge. ↑ Indicates rising edge.

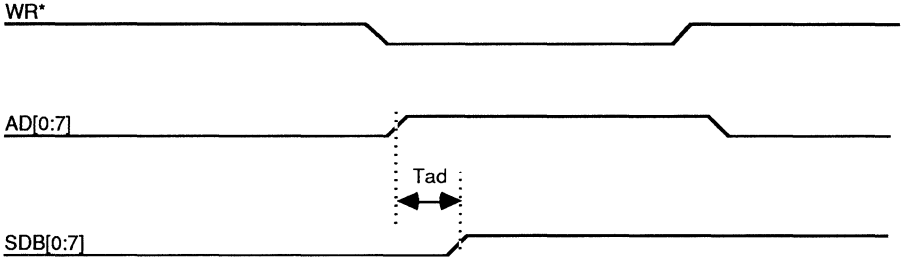
† The Tra specification refers to the delay in creating the SDB[0:7] to D[0:7] path. The given specifications are for reference and assume the SDB[0:7] bus has been stable well before the falling (leading) edge of RD*. If SDB[0:7] is not valid within 5 ns after the falling (leading) edge of RD*, then the Tda specification should be used by the system designer to predict when valid data will be available.

†† The Tad specification refers to the delay in propagating the AD[0:7] to the SDB[0:7] pins. This assumes that the BOE (BUS OUT ENABLE) bit (Register 52H, Bit 3) is set. Note that the data byte written to Register 50H is latched and that no hold or invalid timing is specified.

Register 50H Read Timing



Register 50H Write Timing

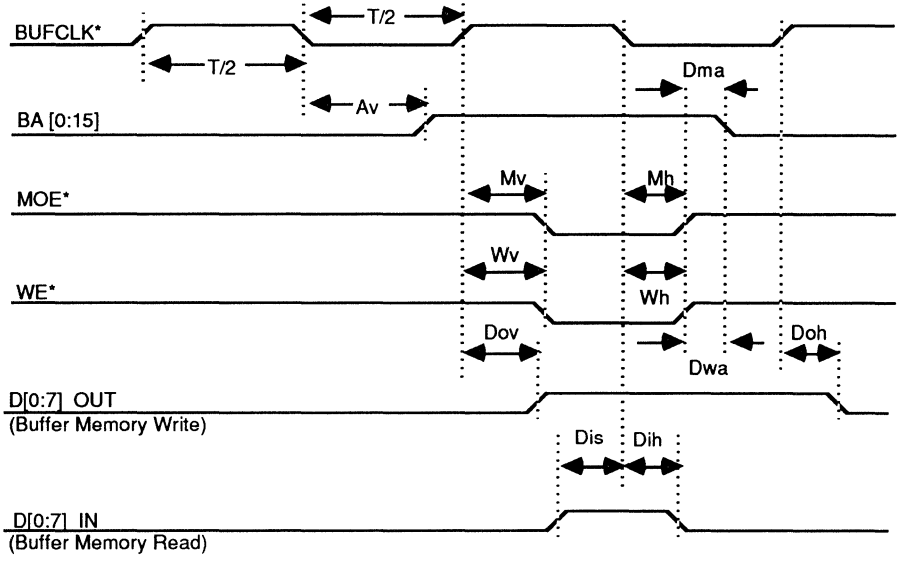


Buffer Memory Read/WriteTiming Table

SYMBOL	PARAMETER	MIN	MAX	UNITS
T	BUFCLK* Period	166		ns
T/2	BUFCLK* Assert/Deassert	80		ns
Av	BUFCLK*↓ to Address valid	50		ns
Dov	BUFCLK*↑ to Data valid		25	ns
Doh	BUFCLK*↑ to Data invalid	0		ns
Dwa	WE*↑ to Address Hold	0	25	ns
Mv	BUFCLK*↑ to MOE*↓	0	20	ns
Mh	BUFCLK*↓ to MOE*↑	0	25	ns
Wv	BUFCLK*↑ to WE*↓	0	20	ns
Wh	BUFCLK*↓ to WE*↑	0	25	ns
Dma	MOE*↓ to Address Hold	0	25	ns
Dis	Data valid to BUFCLK*↓		15	ns
Dih	BUFCLK*↓ to Data invalid		10	ns

NOTE: ↓ Indicates falling edge. ↑ Indicates rising edge.

Buffer Memory Read/WriteTiming



NOTES: (1) When the SCSI WRITE ENABLE or the SCSI READ ENABLE bit (Register 53H, Bits 2,3 respectively) is set, the MOE* signal (Pin 15) will be asserted low each unused BUFCLK* cycle until the falling (leading) edge the SCSI ACKNOWLEDGE signal (ACK* — Pin 70).

(2) When the SCSI WRITE ENABLE bit (Register 53H, Bit 2) is set, the WE* signal (Pin 16) will also be asserted low each unused BUFCLK* cycle until the falling (leading) edge of the SCSI ACKNOWLEDGE signal (ACK* — Pin 70).

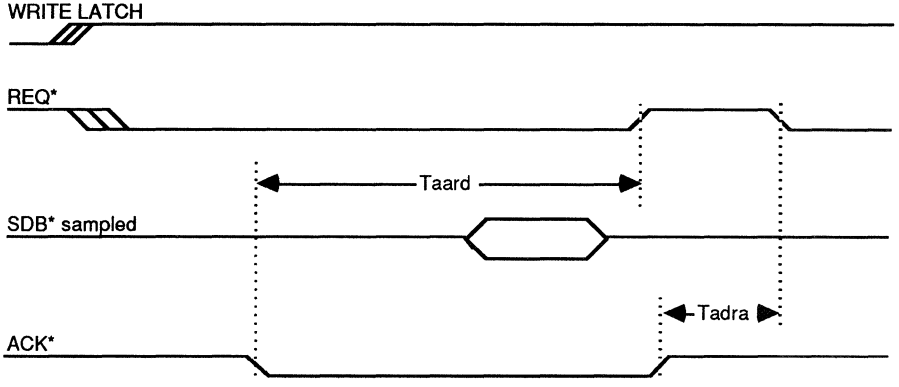
Host-to-Buffer Memory Transfer Timing Table

SYMBOL	PARAMETER	15 MHz MIN	15 MHz MAX	24 MHz MIN	24 MHz MAX	UNITS
Taard	ACK*↓ to REQ*↑		70+(3•T) †		70+(3•T) †	ns
Tadra	ACK*↑ to REQ*↓		75		75	ns

NOTE: ↓ Indicates falling edge. ↑ Indicates rising edge.

† T = BUFCLK* period.

Host-to-Buffer Memory Transfer Timing



NOTE: The MOE* signal (Pin 15) and the WE* signal (Pin 16) will be continuously asserted low every unused BUFCLK* cycle while waiting for the falling (leading) edge of the SCSI ACKNOWLEDGE signal (ACK* — Pin 70).

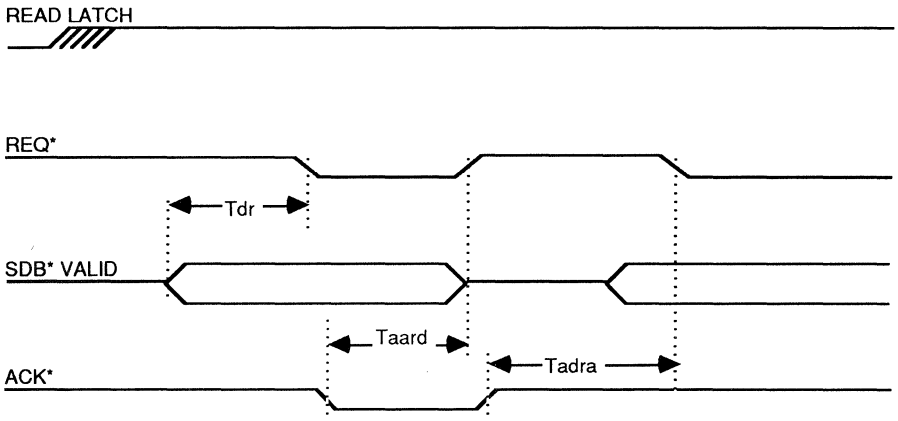
Buffer Memory-to-Host Transfer Timing Table

SYMBOL	PARAMETER	15 MHz MIN	15 MHz MAX	24 MHz MIN	24 MHz MAX	UNITS
Tdr	SDB* Valid to REQ*↓	55		55		ns
Taard	ACK*↓ to REQ*↑		40		40	ns
Tadra	ACK*↑ to REQ*↓		35+(3•T) †		35+(3•T) †	ns

NOTE: ↓ Indicates falling edge. ↑ Indicates rising edge.

† T = BUFCLK* period.

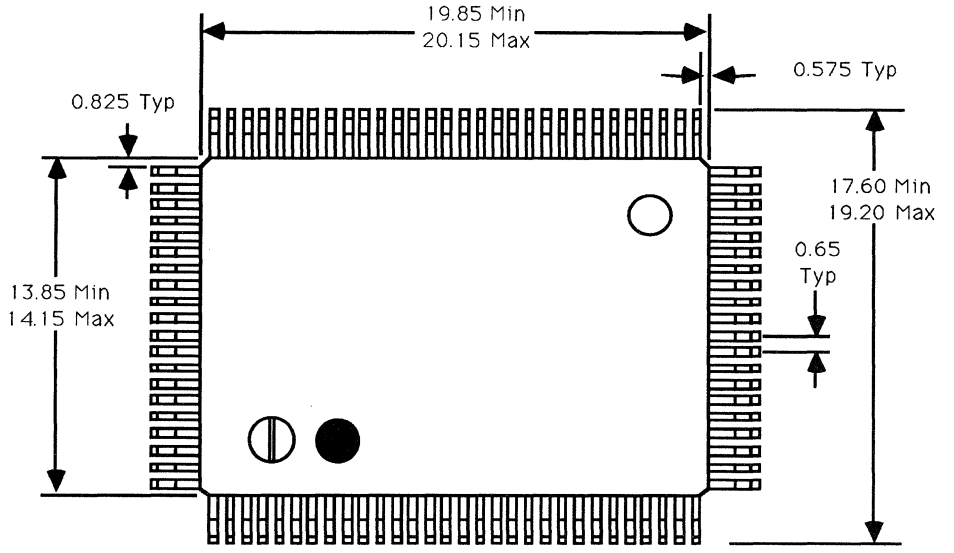
Buffer Memory-to-Host Transfer Timing

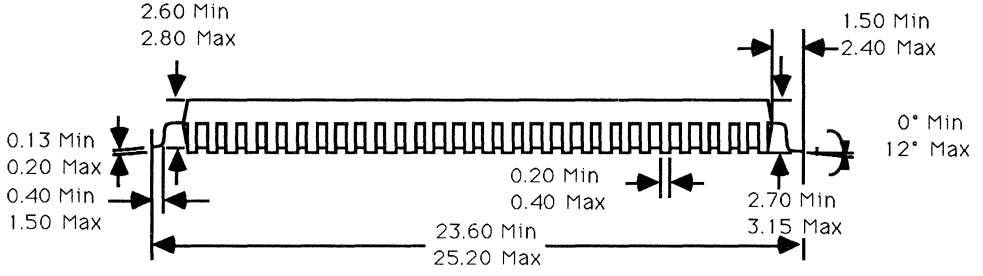


NOTE: The MOE* signal (Pin 15) will be continuously asserted low every unused BUFCLK* cycle while waiting for the falling (leading) edge of the SCSI ACKNOWLEDGE signal (ACK* — Pin 70).

12. SAMPLE PACKAGE

12.1 100-Pin Quad Flat Pack (QFP) Sample Package

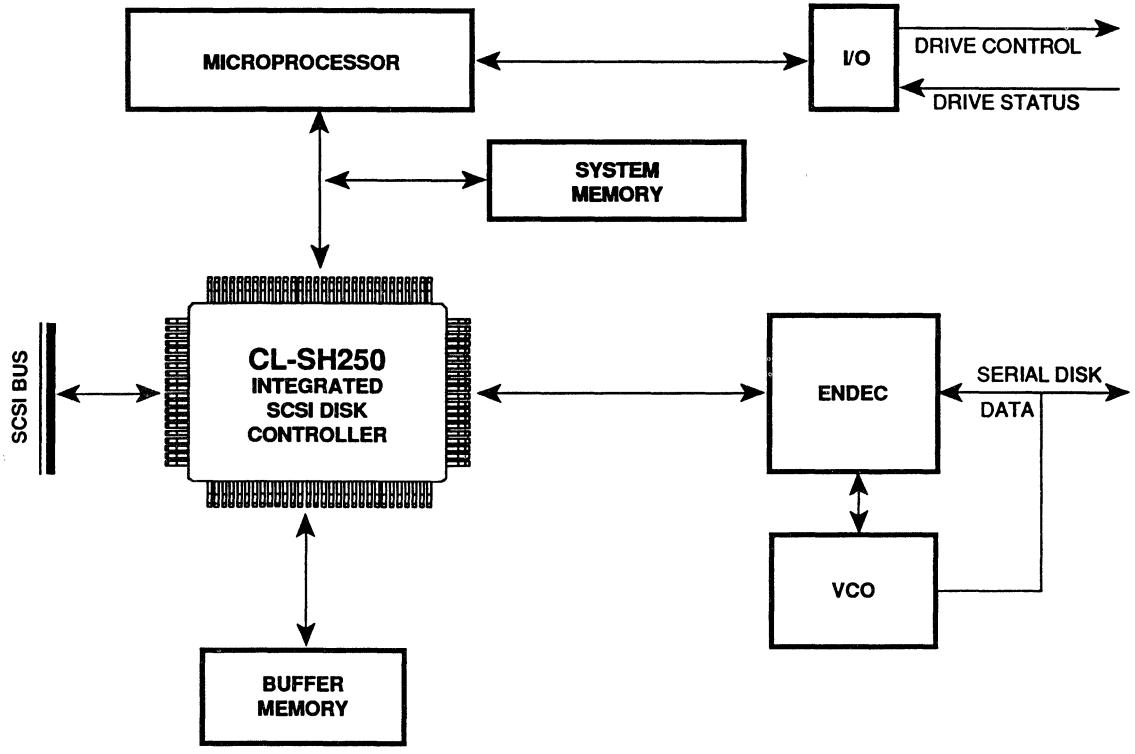




NOTE: Dimensions for the QFP package are in millimeters.

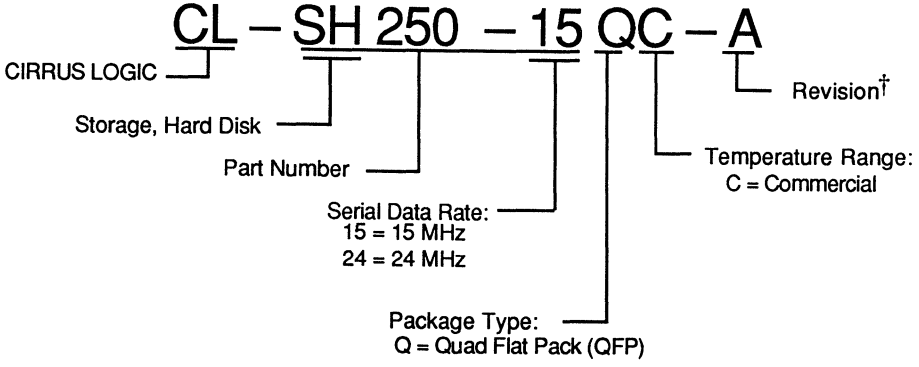
13. TYPICAL APPLICATION

System Block Diagram



14. ORDERING INFORMATION

Cirrus Logic Numbering Guide



† Contact Cirrus Logic for up-to-date information on revisions.

Notes

Notes

Notes

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The Company

Cirrus Logic, Inc., produces high-integration peripheral controller circuits for mass storage, graphics, and data communications. Our products are used in leading-edge personal computers, engineering workstations, and office automation equipment.

The Cirrus Logic formula combines proprietary S/LA™† IC design automation with system design expertise. The S/LA design system is a proven tool for developing high-performance logic circuits in half the time of most semiconductor companies. The results are better VLSI products, on-time, that help you win in the marketplace.

Cirrus Logic's fabless manufacturing strategy, unique in the semiconductor industry, employs a full manufacturing infrastructure to ensure maximum product quality, availability and value for our customers.

Talk to our systems and applications specialists; see how you can benefit from a new kind of semiconductor company.

† U.S. Patent No. 4,293,783

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