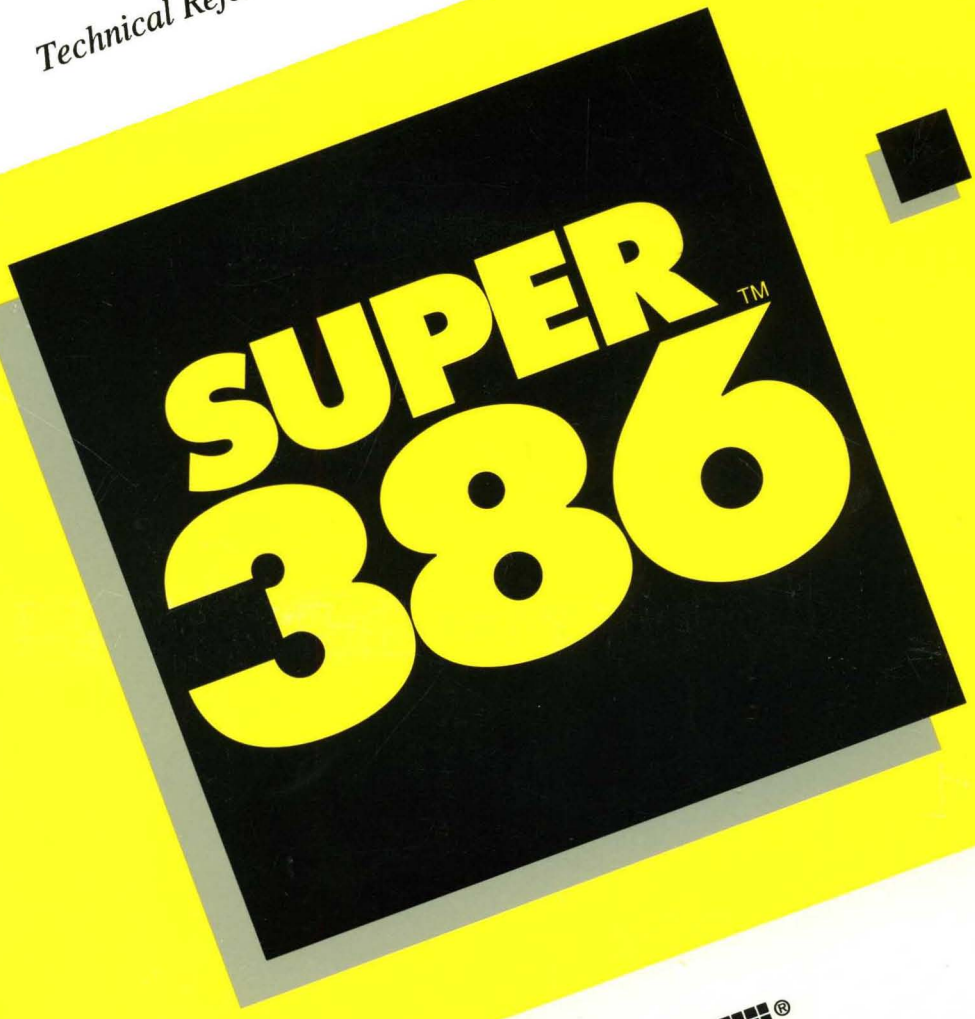
MK82310-PI-Super

Technical Reference Manual



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MK82310-PI-Super

Technical Reference Manual

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Preface

The Super386 PEAK/DM PI board (MK82310-PI-Super) is a design example of a highly integrated motherboard for the medium to high performance PC desktop market. This manual is designed to show a PC OEM or technician how the MK82310-PI-Super system board was designed and how to configure it. Knowledge of basic computer concepts and operation and experience with PC hardware, its terminology and use, is assumed.

This manual explains the features, usage, and installation of the MK82310-PI-Super system motherboard. The manual is divided into three sections: Introduction, Configuration Options, and Designer Notes. The appendices contain the bill of materials and PAL logic equations.

Note: Notes are set off from the text to call special attention to particularly important information. A caution notice, which calls attention to information that could potentially harm the MK82310-PI-Super system board, is also set apart in this manner.

The following acronyms and symbols are used throughout this document:

B	Byte(s), 8-bits
b	Bit(s)
DRAM	Dynamic Random Access Memory
EMC	Extended Math Coprocessor
h	Hexadecimal
k	Kilo or thousand
mA	Milliamperes
M	Mega or million
MHz	MegaHertz
mV	Millivolts

ns	Nanosecond
OEM	Original Equipment Manufacturer
PAL	Program Array Logic
POST	Power-On Self Test
SIMM	Single In-line Memory Module
SRAM	Static Random Access Memory
t(acc)	Address access time for a static memory device
t(oe)	Output enable time

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CHAPTER 1

Introduction

The Super386 PEAK/DM PI board (MK82310-PI-Super) is a design example of a highly integrated motherboard for the medium to high performance PC desktop market. The design is based on the PEAK/DM™ CHIPSet, the Super386™ CPUs, and the SuperMathDX™ coprocessor from Chips and Technologies, Inc. Together, these products offer superior performance in the midrange 386-based computer market. The MK82310-PI-Super board is intended for designers of PC motherboards who are using the PEAK/DM, Super386™ DX, and SuperMathDX components. It also serves as a complete engineering reference for OEMs. All engineering documentation required for production, such as schematics, layout, and Gerber files, are available on floppy diskettes to assure fast turnaround of a proven design at minimum cost.

Inspecting the Board

After unpacking the MK82310-PI-Super system board, carefully inspect the board for any damage that might have occurred during shipping. The types of damage to look for are:

- Shorted pins on the three large flat packs (the 82C351, 82C355, and 82C356)
- Torn signal traces on the PCB
- Bent pins on jumper blocks or Berg connectors.

Examine all socketed components to ensure they are firmly seated. This includes the BIOS ROM, Single In-line Memory Modules (SIMMs), cache and tag memory, CPU, and keyboard controller. If the MK82310-PI-Super board has been damaged during shipment, return the board to the place of purchase.

MK82310-PI-Super Versatility

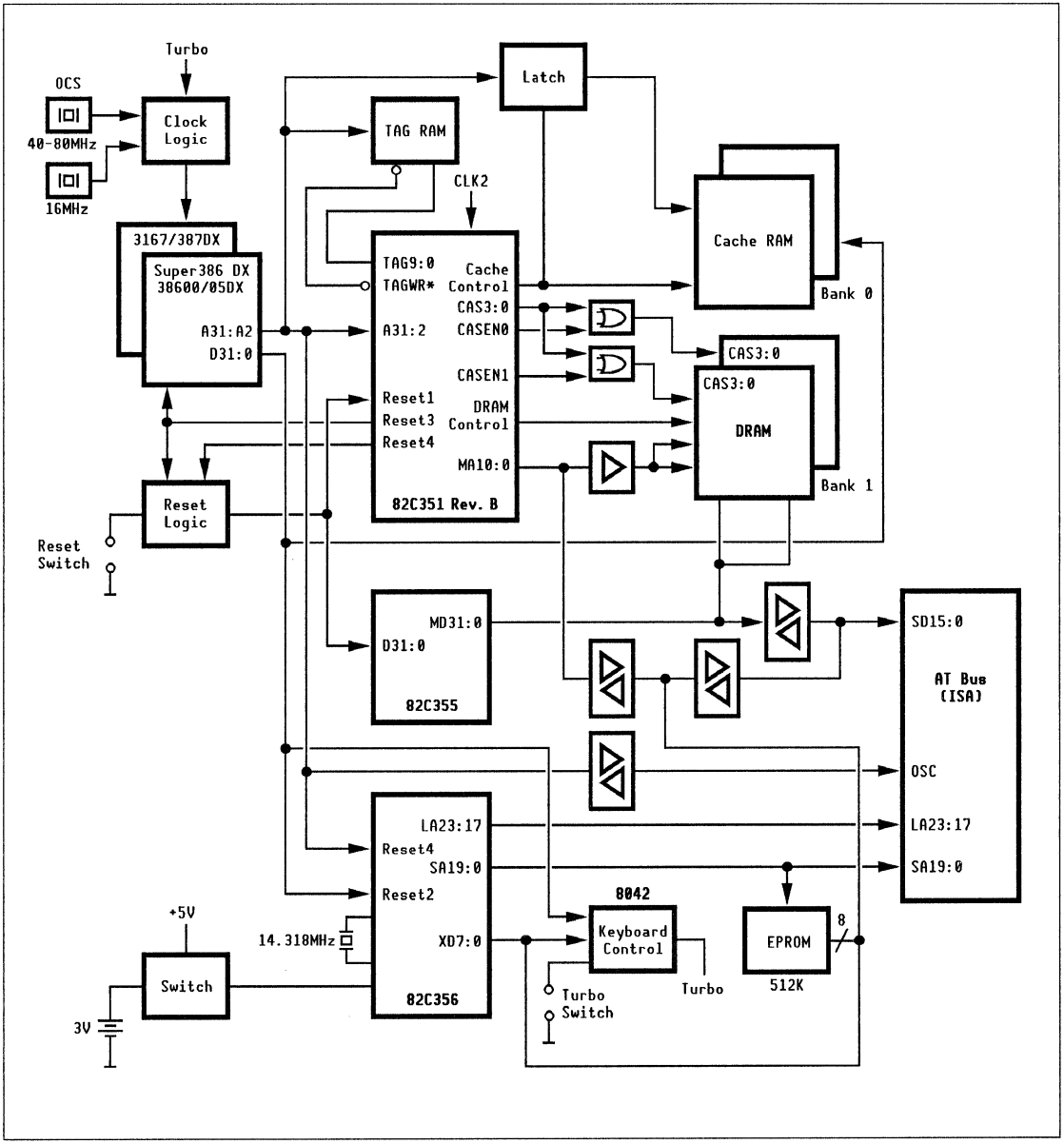
Why would anybody at this point in time be interested in a new 386-based motherboard? There are a number of good reasons, but the most important is economy. The complete PEAK/DM system logic chipset, the Super386 microprocessor, and the SuperMathDX coprocessor are available at a very competitive price. The second reason is economy of scale. One versatile board design can effectively be differentiated by populating the board with various CPUs and memory configurations to cover a broader market segment.

Since the board serves as a platform for more than one design, the volume production of the board can be increased and, at the same time, inventory items can be reduced.

The high performance of the 38600DX CPU and the even higher performance of the 38605DX CPU with on-chip instruction cache can outperform any 386-based competitor on the market and allow expansion into higher performance markets as well. In fact, at the higher frequencies, 33MHz and above, this design compares favorably with an Intel® 486SX based system but costs much less.

The design is based on the field-proven MK82310 motherboard developed for the PEAK/DM CHIPSet, which is in volume production at various OEM sites. Figure 1-1, on the following page, shows the MK82310 PI system block diagram.

Figure 1-1. *MK82310-PI-Super System Block Diagram*



A number of features have been added to the MK82310 board:

- Universal socket to accommodate the 80386DX, 38600DX, or 38605DX CPU
- Pipeline support
- Two-way page interleave DRAM
- Battery for powering the CMOS RAM
- 40MHz maximum operating frequency.

The board contains a 176-pin footprint socket that can be stuffed with any of the following four CPUs: Intel 386DX, Am386™, 386DX, 38600DX, or 38605DX. A 132-pin 386 subset accommodates the 38600DX from CHIPS® as well as the Intel/AMD 386. While performance is significantly improved with the CHIPS CPU, the board is not restricted to only one vendor of this key component. With the Super386 DX CPU, the board can be run at 20MHz to 25MHz in pipeline mode, using slow DRAMs in a cacheless system. Note that pipelining does not work at 33MHz or 40MHz at this time. The Super386 DX and the SuperMathDX coprocessor can operate at speeds up to 40MHz when available.

The 38605DX CPU with on-chip instruction cache (I-cache) improves performance even further. A secondary cache is controlled by the 82C351 integrated cache DRAM controller that supports up to 256k cache RAM and four banks of DRAM. Only two banks of DRAM and up to 128kB of cache are used in this particular design. The DRAM scheme is paged interleaved, which means that DRAM page size is doubled when two banks of identical size are populated.

Operating Modes

Although the CHIPS BIOS will determine the basic hardware setup based on installed memory configuration during the Power-On Self-Test (POST), it is well to understand the operating conditions and modes that optimize performance. The following overview will provide a quick orientation on how to set up the system.

Address Pipeline Mode

Address pipelining is a feature that allows use of slower DRAMs than would otherwise be necessary. In this mode, the CPU address can be changed one CPU clock cycle earlier than in non-pipeline mode. That is, in a 25MHz system, the available time for the DRAM to respond (access data) is increased by 40ns. Therefore, the number of wait states usually required can be reduced.

This feature is supported only in a cacheless configuration (or when the cache is turned off). The operating frequency is limited to 25MHz. Pipelining is selected by jumper W1. No register setup for selecting pipelining is required. However, in order to achieve maximum performance, the user might need to adjust the number of wait states inserted.

Interleave Mode

To use the interleave feature, the second bank of DRAM must be populated with the same memory size used in bank 0. Register 19h, bit 0 must be set to 1 to turn on the CASEN lines. This is done by the BIOS and does not need to be set by the user. In interleave mode, the start address of either bank must be set to 0.

Page Mode

Page mode can be enabled or disabled in all configurations. For maximum performance, page mode should be enabled. Set register 1Ch, bit 4 to 0. Interleaving of memory banks may be selected in addition to page mode when two banks of the same size are populated. If the memory size is not equal in both banks, only page mode without interleaving may be selected. In page mode without interleaving, the start address of the second bank is above that of bank 0. That is, if bank 0 is populated only with 1MB SIMMs (4MB in bank 0), then the starting address of bank 1 is at 4M.

Mixed Memory Mode

One of the unique features of the PEAK/DM CHIPSet is the ability to mix memory in terms of size and speed. A system may be configured with a minimum memory size in one bank, and the second bank can be added later. It is common to upgrade a 1MB system to 5MB. No jumper has to be moved for upgrading DRAMs. The wait states required for the second bank as well as the RAS precharge time can be selected individually. The RAS precharge time is the time the DRAM requires between consecutive access cycles to recover from the charge loss. For interleaving of banks to work properly, both banks have to be the same size; however, the speed of the DRAMs can be different. There is a slight performance difference in comparison with a system that operates in interleaved mode with the same-size memory banks. However, the difference is not noticed with most application programs.

Because of the way block 0 and block 1 of the 82C351 dynamic controller handle address mapping, bank 0 start address is above bank 1. See Table 1-1.

Table 1-1. Bank 0 and Bank 1 Start Addresses in Mixed Memory Mode

Bank 0	Bank 1	Start Address Bank 0	Start Address Bank 1
256k	1M	4M	0
256k	4M	16M	0
1M	4M	0M	4M

External Cache

Cache-based systems run only in non-pipeline mode. Memory regions can be declared as non-cachable, or cache can be turned off altogether. If cache is turned off, the internal I-cache of the 38605DX CPU is still effective.

CPU Selection

The following CPUs are currently offered. Each has specific features that should be considered.

Intel/AMD 80386DX

These CPUs can operate in pipeline or non-pipeline mode (jumper selectable) up to 25MHz. Pipeline mode can be chosen for a low-cost system with slow memory (DRAM) and no cache. In a configuration with cache, the pipelining has to be turned off (W1 open—not jumpered).

CHIPS 38600DX

This CPU operates at the highest performance without pipelining. Up to 128kB of cache can be added to reduce DRAM references, effectively increasing performance.

CHIPS 38605DX

This CPU, with its on-chip cache, is a stuffing option. It can be used in a full cache system with up to 128kB of secondary cache and also without secondary cache.

Coprocessor Selection

The market offers a number of coprocessors that fit into the combined 387/Weitek® 3167 socket. Any of these will operate without modification or jumper settings. Installation of the Weitek coprocessor is detected by U3.

SuperMathDX Coprocessor

The SuperMathDX coprocessor from CHIPS performs better than industry standard coprocessors. This SuperMathDX coprocessor, paired with a Super386 DX CPU (38600DX or 38605DX), is the optimum CHIPS solution in terms of performance, price, and availability.

Clock Speed Selection

The CPU clock speed can range from 20MHz to 40MHz. Some components such as the CPU, cache RAM, cache TAG RAMs, and PEAK/DM need to be selected and tested for the maximum target frequency.

Note: Increasing the operating frequency increases heat dissipation, which has an adverse affect on long-term reliability. Operation beyond the frequency that the components have been screened for is not recommended.

Activating a turbo switch (W3) informs the keyboard controller to switch to the 16MHz oscillator, which effectively puts the CPU in 8MHz operation. The I/O bus (ISA) always operates from this 8MHz clock source. The keyboard controller is interrupt driven, meaning that clock switching follows 82C356 acknowledgement of the interrupt (IRQ 1), and is propagated to the CPU. Note that operating systems other than MS-DOS® might not service this interrupt; therefore, clock switching during operation might not work. In this case, set up the desired frequency in the setup procedure or while operating in MS-DOS.

Please note that the maximum frequency for pipeline mode (cache not populated or cache disabled) is 25MHz. Beyond this, reliable operation cannot be guaranteed.

MK82310-PI-Super Product Specification

Table 1-2 provides an overview of key features.

Table 1-2. *MK82310-PI-Super Product Specification*

Component/Parameter	Type	Feature(s)
CPU	38600DX	
	38605DX	
	Intel i386DX	
CHIPset	PEAK/DM	
	82C351 Rev. B	Cache/DRAM Controller
	82C355	Data Buffer
	82C356	Peripheral Controller
CPU Socket	176-pin PGA	
CPU Speed		8-40 MHz
FPU	387DX, SuperMathDX, W3167	
FPU Socketing	176 PGA	
FPU Speed		8-40 MHz (Starts CPU Clock)
FPU Clock		
I/O Bus Type	ISA	
I/O Bus Speed		8 MHz
I/O Speed Selection		No
Keyboard Connector	5-pin DIN	
#8 Bit Slots		1
#16 Bit Slots		7
DRAM Controller	82C351 Rev B	Paged Interleave
DRAM Size		1MB minimum, 32MB maximum
DRAM Size Variations		1, 4, 5, 8, 16, 17, 20, 32MB
DRAM Type		Page Mode
DRAM Speed, Slowest		80ns @ 40 MHz
DRAM Sockets	8x SIMM 9-Bit	Two banks
Cache Controller	82C251 Rev. B	Direct Mapped,Write Through, Buffered Write

Table 1-2. *MK82310-PI-Super Product Specification (continued)*

Component/Parameter	Type	Feature(s)
Cache RAM Size		32kB Minimum, 128kB Maximum
Cache Size Variations		0, 32k, 64k, 128kB
Cache Speed		15ns @ 40 MHz
Cache RAM Socket	DIP	
Wait-State Support		Yes
BIOS 8/16 bit		8-bit
BIOS Version	CHIPS 2.0.0 or later	
BIOS Shadowing		Yes
Board Form Factor	Baby AT	
Number of Layers		4
Board Material	FR4, 1.6mm	
Trace Width		7 mil
Silk Screen	Dry Etch	
Package Technology	DIP/PGA/SMT	
On-board Battery Type	Varta 3V	
Power Consumption		TBD
Ambient Temperature Range		0-40° C

CHAPTER 2

Configuration Options

The MK82310-PI-Super board, shown in Figure 2-1, uses jumpers and connectors to enable changes to hardware features and system enhancements. However, many of the system's features are implemented as register programmable options in the PEAK/DM CS82310 CHIPSet. Consult the CS82310 data sheet for additional information on the CHIPSet configuration registers and their use. The MK82310-PI-Super system jumpers and connectors support the following options:

- Choice of monitor type (mono or color)
- Choice of cache data RAM and cache tag memory size
- Clearing of battery-backed CMOS memory
- CMOS and RTC backup battery (6 volts)
- Pipeline mode
- Audio speaker (8 ohms)
- Keyboard lock
- Reset switch
- Hardware CPU speed switching (Turbo Switch)
- POWERGOOD generation.

MK82310-PI-Super Hardware Options

To locate the connectors and jumper blocks on the MK82310-PI-Super system board, refer to the system board reference diagrams, Figure 2-1 and Figure 2-2. Designators for the jumper blocks begin with a W, while connectors begin with a J. The power supply connector is labeled P1.

Figure 2-1. *The MK82310-PI-Super Board*

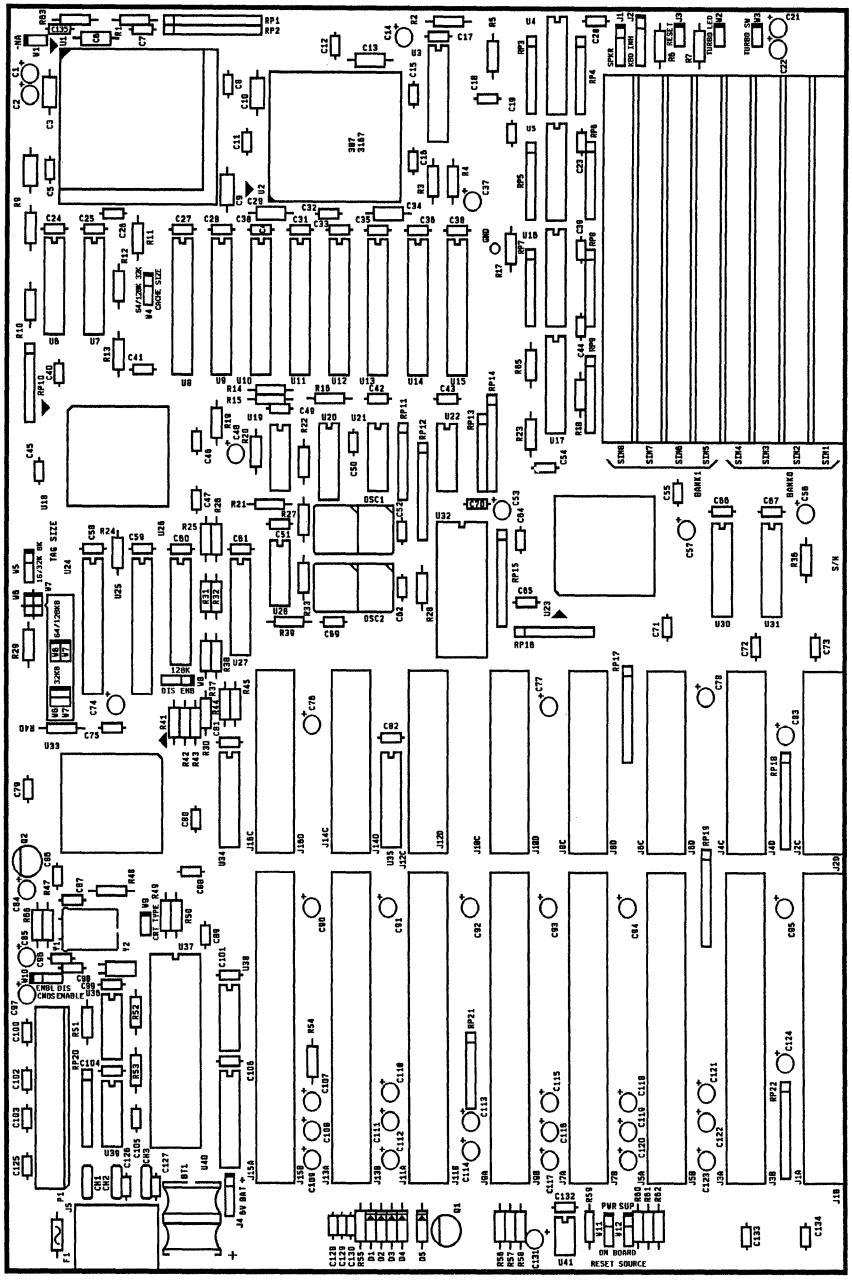


Figure 2-2. *Location of MK82310-PI-Super Connectors and Jumpers*

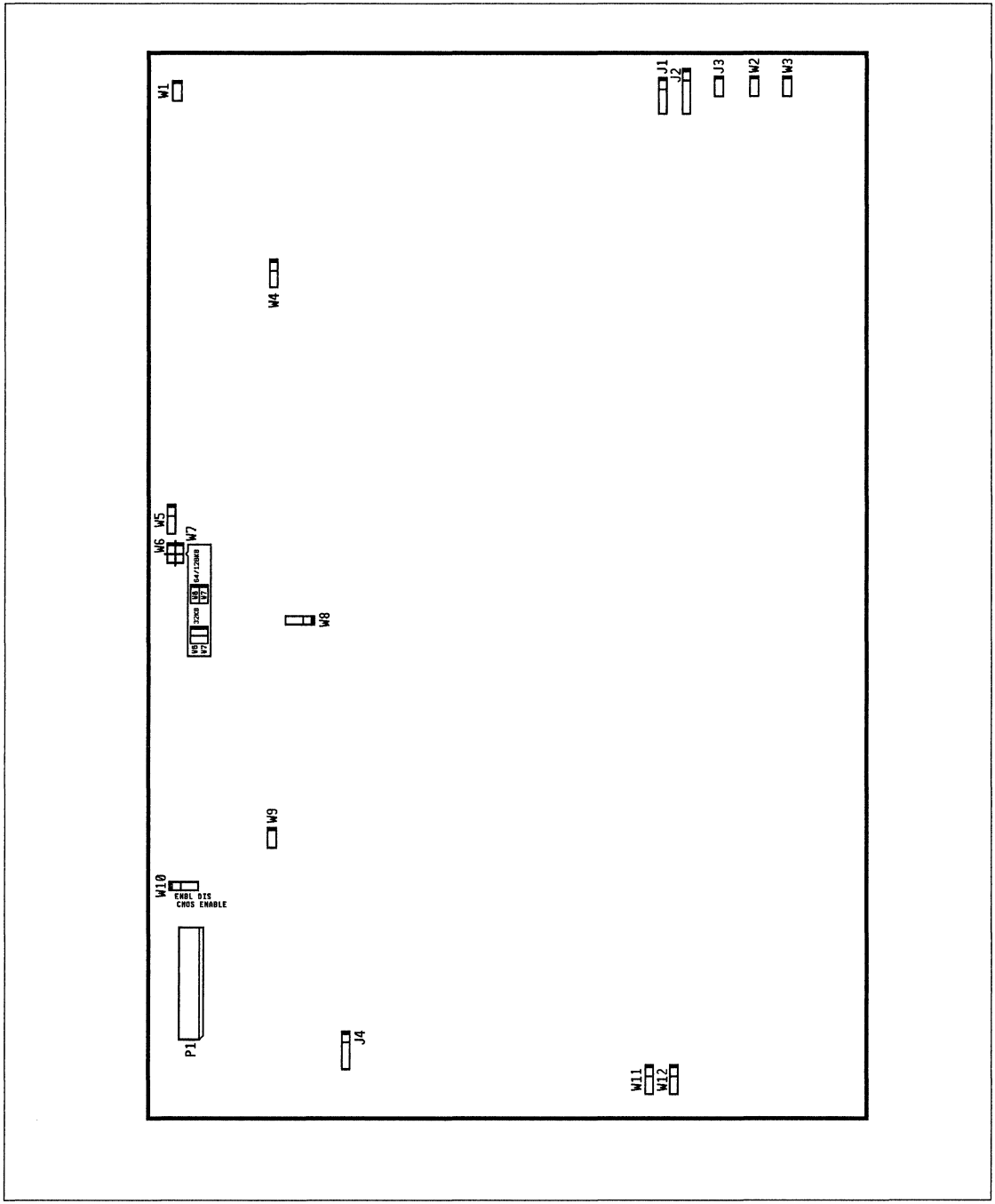


Table 2-1 lists the available jumpers and connectors on the MK82310-PI-Super board.

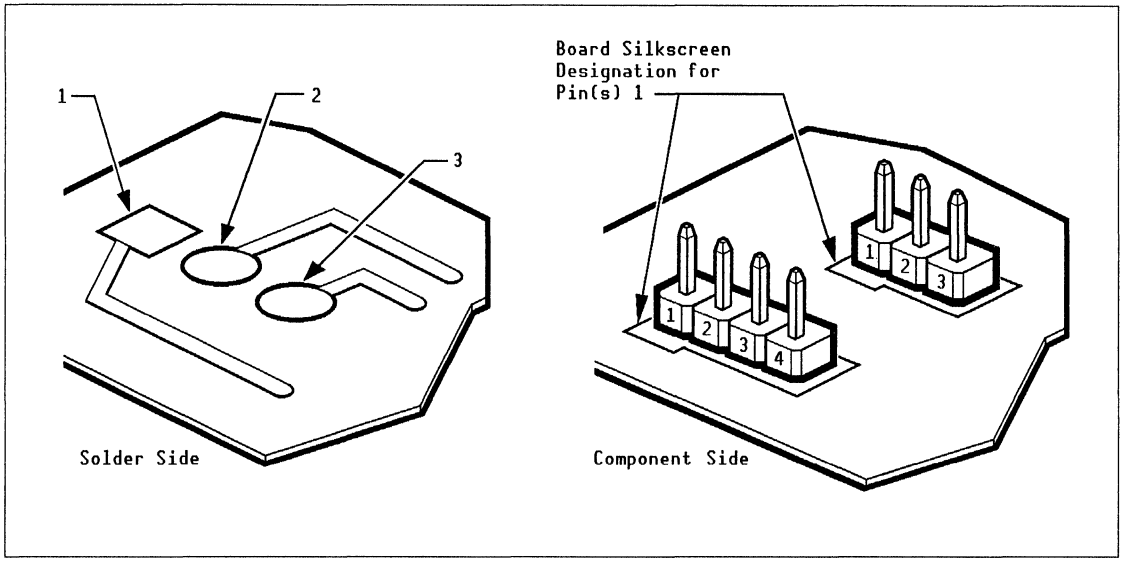
Table 2-1. *MK82310-PI-Super Jumpers and Connectors*

Label	Type	Function
J1	4-pin Berg	External Speaker Connector
J2	5-pin Berg	Security Lock and Power LED
J3	2-pin Berg	Manual System Reset
J4	4-pin Berg	External 6V Battery
J5	5-pin Berg	Keyboard Connector
W1	2-pin Berg	Pipeline
W2	2-pin Berg	CPU Speed LED indicator
W3	2-pin Berg	CPU Speed Control (turbo mode)
W4	3-pin Berg	A15 Cache RAM Enable
W5	3-pin Berg	A15 Tag RAM Enable
W6/W7	2 x 2-pin Berg	Tag 7/9 Address Select
W8	3-pin Berg	Tag 0/8 Address Select
W9	2-pin Berg	CRT Type
W10	3-pin Berg	Battery-backed CMOS Memory Discharge
W11/12	3-pin Berg	RESET1* Signal Source

For the definitions and usage of these jumpers, see the sections "MK82310-PI-Super Connectors" and "MK82310-PI-Super Jumpers."

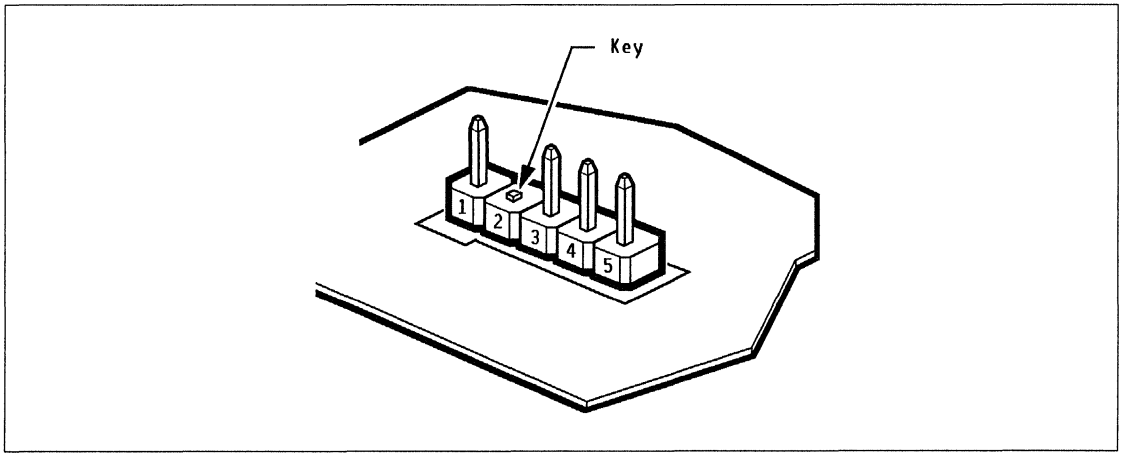
Pin 1 of each jumper block is designated with a square solder pad on the solder side of the PCB and with a white square border on the component side of the PCB, as shown in Figure 2-3.

Figure 2-3. *Jumper Block Pin Assignments*



The MK82310-PI-Super system board also contains Berg connectors that are "keyed." A missing pin is the key or polarity indicator. It is used as a guide to install the system cables correctly. Figure 2-4 shows a 5-pin Berg connector with key.

Figure 2-4. *5-Pin Berg Connector With Key*



Default Settings

The MK82310-PI-Super system has been shipped with the default settings shown in Table 2-2.

Table 2-2. *Default Settings*

Jumper Label	Jumper Pins	Function
W1	Open	Non-pipeline.
W2	Open	No turbo LED is installed.
W3	Open	CPU speed is at maximum (OSC 2).
W4	2-3	A15 is connected to the cache RAM (64kB cache RAM).
W5	1-2	Tag address is selected for 64kB cache mode.
W6/W7	1-2	Tags 7, 9 are connected to tag RAM (64kB cache RAM).
W8	2-3	Tag 0 is selected for 64kB cache modes.
W9	1-2	CRT type CGA/EGA/VGA.
W10	Open	CMOS discharge is disabled.
W11/12	2-3	RESET1* is produced by the TL7705 device.

Note: If the MK82310-PI-Super system fails to operate correctly, return the jumpers to their default settings.

The MK82310-PI-Super board is shipped with 64kB of cache and 16kB (two 8k x 8 SRAMS) of tag RAM installed. Therefore, the maximum amount of local cacheable memory is 8MB. For systems with greater than 8MB of memory, U26 should be populated. U26 allows the MK82310-PI-Super board to have the full 32MB of memory as cacheable memory. Otherwise, only the memory below 8MB will be cached.

The BIOS installed in the MK82310-PI-Super board does not have its default settings programmed for the maximum performance of the system. Maximum performance is determined by the system operating speed, DRAM access time, cache access time, tag access time, and the peripheral cards installed. To achieve the highest performance possible, the system BIOS should be used to set up the CHIPSet configuration registers. The values programmed in the configuration registers are determined by the type of equipment and memory used. Consult the CS82310 data book for suggested register settings.

MK82310-PI-Super Connectors

The locations of the board connectors are shown in Figures 2-1 and 2-2. Connectors J1-J5 are described in the following paragraphs.

J1 External Speaker

J1 is a keyed 4-pin Berg connector. It is used to connect an external speaker. The driver for the Speaker Negative Terminal is a 74F244 buffer.

Caution: The external speaker must have an 8-ohm impedance or the speaker driver may be damaged.

The J1 pin and signal designations are shown in Table 2-3.

Table 2-3. *J1 Pins and Signals*

J1 Pin Number	Signal
1	Speaker Negative Terminal
2	Key (This pin has been removed to indicate polarity.)
3	Ground
4	Vcc (+5 Volts, Speaker Positive Terminal)

J2 Security Lock and Power LED

J2, a keyed 5-pin Berg connector, permits the connection of an AT-style front panel keylock and power LED cable. The power LED current is limited by resistor R7 (220 ohms). The J2 pin and signal designations are shown in Table 2-4.

Table 2-4. J2 Pins and Signals

J2 Pin Number	Signal
1	LED Power (Anode)
2	Key (This pin has been removed to indicate polarity.)
3	Ground
4	Keyboard Inhibit (Security Lock)
5	Ground

J3 Manual System Reset

J3 is a 2-pin Berg connector that is used to reset the system board by driving the RESET1 signal to the 82C351 controller. A single-pole momentary switch should be connected to J3. Pin and signal designations are shown in Table 2-5.

Table 2-5. J3 Pins and Signals

J3 Pin Number	Signal
1	Reset Input
2	Ground

J4 External 6V Battery

J4, a keyed 4-pin Berg connector, is used to supply power to the Real Time Clock and CMOS memory while the system power supply is off. To retain CMOS memory, the time and date, install a 6V lithium/alkaline battery or battery pack. There is a three-diode drop from the battery input to the 82C356. The on-board battery is protected from the external one; no harm will occur if an external battery is connected.

Note: For reliable operation use *only* a 6-volt battery or battery pack.

Pin and signal designations are shown in Table 2-6.

Table 2-6. *J4 Pins and Signals*

J4 Pin Number	Signal
1	Battery Positive Terminal
2	Key (This pin has been removed to indicate polarity.)
3	Ground (Battery Negative Terminal)
4	Ground (Battery Negative Terminal)

J5 Keyboard Connector

J5 is a 5-pin DIN connector for an AT-compatible 84-key or 101-key keyboard. Pin and signal designations are shown in Table 2-7.

Table 2-7. J5 Pins and Signals

J5 Pin Number	Signal
1	Keyboard Clock
2	Keyboard Data
3	This pin is not used.
4	Ground
5	Vcc, +5 Volts

Power Connectors

P1, the system power supply, is designed as a receptacle for the PS8 and PS9 power connectors from an AT-compatible power supply. The required voltages are +5 VDC, -5 VDC, +12 VDC, and -12VDC. Pin functions are listed in Table 2-8. Note that pin 1 is reserved for the POWERGOOD signal from the power supply. This active high signal indicates that the +5 VDC lines are stable. By means of jumpers W12 and W13, POWERGOOD can be used to generate power-up resets.

Table 2-8. P1 Functions

P1 Connector[1]	Number	Function
PS8	1	POWER GOOD
	2	+5 VDC (+/-5%)
	3	+12 VDC (+/-5%)
	4	-12 VDC (+/-5%)
	5	Ground (+/- 300mV)
	6	Ground (+/- 300mV)

1 The IBM AT power supply assigns pins 1-6 to the PS8 connector and pins 7-12 to the PS9 connector.

Table 2-8. P1 Functions (continued)

P1 Connector[1]	Number	Function
PS9	7	Ground (+/- 300mV)
	8	Ground (+/- 300mV)
	9	-5 VDC (+/-5%)
	10	+5 VDC (+/-5%)
	11	+5 VDC (+/-5%)
	12	+5 VDC (+/-5%)

1 The IBM AT power supply assigns pins 1-6 to the PS8 connector and pins 7-12 to the PS9 connector.

Caution: Installing the PS8 and PS9 power connectors backward will short out the power supply or damage the MK82310-PI-Super system board. Only power supplies equipped with an overload protection are recommended.

MK82310-PI-Super Jumpers

The locations of jumpers W1-W12 are shown in Figures 2-1 and 2-2. These jumpers are described in the following sections.

W1, Pipeline

W1 selects pipeline or non-pipeline operation. Pipeline operation can only be selected in a non-cache system. See Table 2-9.

Table 2-9. W1 Connector Pins

W1 Pin Numbers	Function
1-2	Pipeline mode

W2, CPU Speed LED and W3, CPU Speed Control

The MK82310-PI-Super system board is equipped with connectors to support CPU speed switching and an LED indicating CPU speed. Refer to Table 2-10. To alter the speed of the CPU, use a single pole single-throw switch with jumper W3. The CPU speed can also be switched by pressing the key combination <Ctrl><Alt><+> for high speed or <Ctrl><Alt><-> for low speed.

The MK82310-PI-Super board is shipped with a 16MHz canned oscillator at OSC1 and a 66.667MHz canned oscillator at OSC2. OSC1 is intended for the AT state-machine clock. The ATBUS clock is equal to one half the AT state-machine clock. OSC2 is the clock used to drive the CPU at its maximum rated speed. Shorting the two jumper pins on W3 will force the CPU to operate from OSC1. If jumper W3 is open or no switch is connected, the CPU will operate from OSC2 (high speed).

Connector W2 (Table 2-10) is for an optional LED to indicate the speed of the CPU. When the LED is lit, the CPU is operating at the maximum speed. The current of the CPU speed LED is limited by a resistor.

Table 2-10. *W2 and W3 Connector Pins*

Connector	Pin Number	Function
W2	1	Connection for Anode (-) terminal of CPU Speed LED
	2	Vcc (Cathode (+) terminal of CPU Speed LED)
W3	1	Jumpered: CPU operates from OSC1 (16MHz)
	2	Jumpered: CPU operates from OSC1 (16MHz)

W4, A15 Cache RAM Enable

W4 enables A15 of the cache SRAMs. It determines the state of the signal at pin 26 of U8, U10, U12, and U14. When 32kB of cache is installed (four 8k x 8 SRAMs), W4 pins 1 and 2 should be jumpered. See Table 2-11. With a 128kB cache RAM (four 32k x 8 SRAMs), W4 pins 2 and 3 should be jumpered.

Table 2-11. *W4 Connector Pins*

W4 Pin Number	Function
1-2	A15 is not used. A15 to the cache SRAMs is connected to +5V.
2-3	A15 is the chip enable for 64kB cache mode, or an address for 128kB cache mode.

Caution: If W4 is not installed correctly, system malfunctions will occur.

W5, A15 Tag RAM Enable

W5 allows A15 to be connected to pin 26 of socket U24. For 8kB of tag RAM, pins 1 and 2 of jumper W6 should be shorted. This connects pin 26 to +5V and enables an 8k x 8 SRAM by activating CE2 of the memory device. On the other hand, for 16kB or 32kB of tag RAM, pins 2 and 3 should be jumped. For this case, pin 26 of socket U24 is connected to A15 from the local address bus. See Table 2-12.

Table 2-12. *W5 Connector Pins*

W5 Pin Number	Function
1-2	8k x 8 tag SRAM installed.
2-3	16k x 8 or 32k x 8 tag SRAM installed.

Caution: If W5 is not installed correctly, damage may occur either to the tag RAM installed at location U24, U25 or U26 or the 82C351 device.

W6 and W7, Tag 7/9 Address Select

Jumper blocks W6 and W7 form a 2 x 2 jumper block. They reconfigure the tag addresses for an 8k x 8 tag SRAM when 32kB cache is installed. For 32kB cache systems that are programmed for 8-bit wide tag memory, tags 0-6 and tag 9 are used by the internal comparator. If U26 is populated with a 16k x 4 SRAM, then W6 and W7 do not need to be altered; the 82C351 system can be programmed for 10-bit wide tag memory, and tags 0 through 9 can be used by the internal comparator. U26 should be populated for systems with local memory sizes greater than 8MB. For additional information on the use of U26, see the "Cache and Tag Memory" section in Chapter 3.

Note: U26 is not needed for systems with 128kB of cache; it is only required when the DRAM size is beyond 8MB.

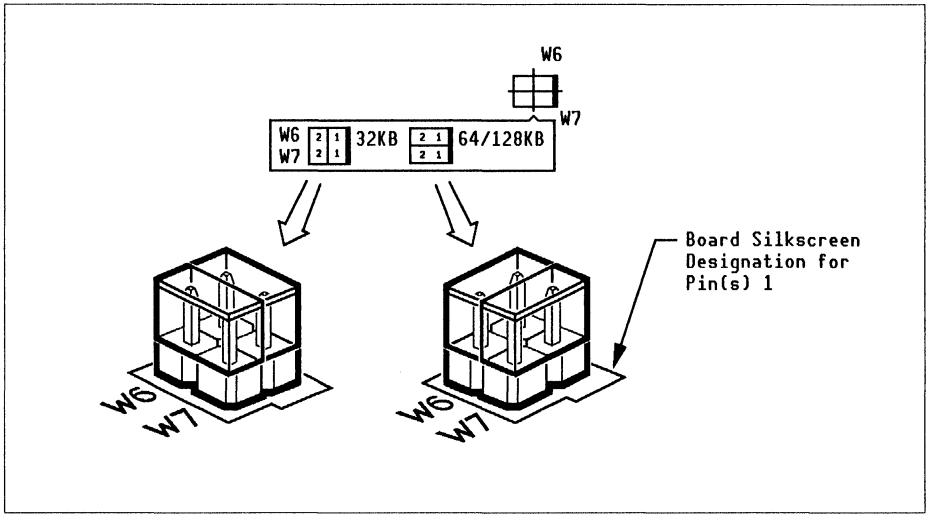
Table 2-13 summarizes the W6 and W7 pin functions.

Table 2-13. *W6 and W7 Pins*

W6, W7 Pin Numbers	Function
W6 1-2, W7 1-2	64kB or 128kB cache mode
W6(1)-W7(1), W6(2)-W7(2)	32kB cache mode with 8-bit wide tag SRAM

See Figure 2-5 for the correct placement of the jumpers.

Figure 2-5. W6 and W7 Jumper Placement



W8, Tag 0/8, Address Select

W8 is used to reconfigure the tag addresses for a 32k x 8 tag SRAM when 128kB of cache is installed. For the 128kB cache mode, tags 1-8 are used by the internal comparator. Only one 32k x 8 tag SRAM is required for 128kB cache mode. The 32kB of tag RAM provides for 32MB of cacheable local memory. See Table 2-14.

Table 2-14. W8 Pins

W8 Pin Numbers	Function
2-3	32kB or 64kB cache modes
1-2	128kB cache mode for 8-bit wide tag memory

Note: For 8-bit wide tag memory, the BIOS must use bits 2 and 1 of register index 21h to configure the address tag width for 8 bits.

W9, CRT Type

W9 is used to indicate the type of primary graphics adapter card installed in the system. W9 drives pin 9 of the keyboard controller, U35. See Table 2-15 for the pin functions.

Table 2-15. W9 Pins

W9 Pin Numbers	Function
1-2	Jumpered: Color graphics adapter card
	Opened: Monochrome video card

W10, Battery Backed CMOS Memory Discharge

W10 is used to clear the system CMOS memory. This memory normally contains the system setup information (i.e., time, date, hard disk, floppy types, and the number of memory wait states). It is usually programmed by a setup program. If you make an error when using the setup program or you wish to erase the setup information, temporarily short pins 2 and 3 to clear the CMOS memory. W10 actually provides Vcc to the 82C356 device, which contains the CMOS memory. Temporarily shorting pins 2 and 3 will ground the 82C356 Vcc inputs.

For normal operation, short pins 1 and 2. *Do not short these pins when the power supply is on.* See Table 2-16.

Table 2-16. W10 Pins

W10 Pin Number	Function
2-3	Clear CMOS RAM
1-2	Normal Operation

W11 and W12, RESET1 Signal Source

Jumpers W12 and W13 are used to select the source of RESET1 to the 82C351 device. RESET1 is active for power-up and power-on system resets. Power-up reset occurs until the power supply has reached the proper voltage levels. Power-on resets are typically driven manually by the system reset switch. On the MK82310-PI-Super board, power-up resets can be generated by the POWERGOOD signal from the power supply or the on-board voltage level detector, TL7705. Power-on resets are generated by the Manual System Reset connector. The Manual System Reset signal is wire ANDed with the power-up reset signal. W11 selects the device that generates the power-up reset signal, and W12 selects the Manual System Reset power-on signal. A detailed schematic of the RESET* circuitry is shown in Figure 2-6.

Figure 2-6. *RESET* Circuitry*

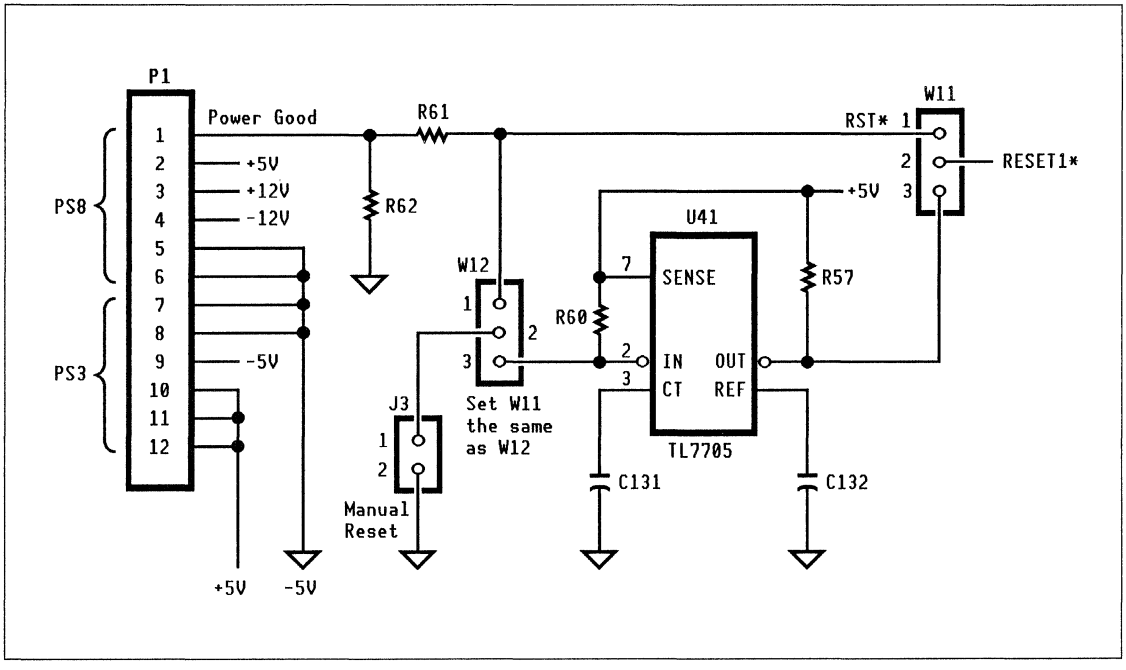


Table 2-17 shows the W11 and W12 pin functions.

Table 2-17. W11 and W12 Pins

Pin Location	Pin Number	Function
W11	1-2	RESET1* is generated by the system power supply POWERGOOD signal.
	2-3	RESET1* is generated by the on-board voltage level detector, TL7705A.
W12	1-2	The Manual System Reset signal is wire ANDed with POWERGOOD.
	2-3	The Manual System Reset signal is wire ANDed with the TL7705A output.

Note: W11 and W12 must be jumpered the same or the manual reset will not operate properly (i.e., W11 pins 1-2 and W12 pins 1-2).

CHAPTER 3

Designer's Notes

The MK82310-PI-Super board contains some logic that is necessary to interface with the 387DX and the Weitek 3167 coprocessors. In this chapter, the required logic is explained and output signals are defined. This chapter also contains recommended configurations, information on cache and tag memory, local memory, and board testing feature.

Recommended Configurations

Table 3-1 shows recommended configurations for the MK82310-PI-Super board.

Table 3-1. Recommended Configurations

	CLK MHz	DRAM trac	SRAM tacc	Index REGs								
				19	1A	1B	1C	11, 13 15, 17	18	20	2A	2F
Interleave Pipeline	25	60	NO	05	00	00	0X	80	00	00	39	00
Interleave Pipeline	25	80	NO	01	66	66	0X	8A	00	00	39	10
Interleave Cache	25	60	35	05	66	66	0X	80	00	00	31	00
Interleave Cache	25	80	35	01	66	66	0X	8A	00	00	31	10
Interleave Cache	33	60	25	01	77	77	4X	8A	00	00	31	10
Interleave Cache	33	80	25	45	F7	77	4X	9C	00	00	31	10
Interleave Cache	40	60	15	45	F7	77	4X	94	00	00	31	10
Interleave Cache	40	80	15	45	F7	F7	4X	9E	00	00	31	10

In Table 3-1 the values for X (index register 1C) are as follows:

X = 0 no interleaving
1 Blocks A, B interleaved
2 Blocks C, D interleaved
3 Blocks A, B and C interleaved individually
4 Blocks A, B, C and D interleaved

Coprocessor Interface PAL

The PEAK/DM CHIPSet requires additional interface logic for the 387DX and Weitek 3167 coprocessors. The 16L8 PAL at location U3 contains all of the logic necessary to interface the 387DX and Weitek 3167 with the exception of the logic functions listed in Table 3-2. These functions are performed by the devices indicated in the table.

Table 3-2. *Logic Devices*

Function	Responsible Device
Port F0 decode	82C356
i387 READY logic	82C351
3167 READY logic	Weitek 3167 directly
3167 bus cycle claiming	AF32* signal from the 3167 to the 82C351

The PAL has the following features:

- Standard speed (25nS) 16L8 PAL.
- Provides the BUSY387* signals: BUSY387*, LATCHED BUSY, and TOGGLE BUSY.
- Provides IRQ13 for both the 387DX and 3167.
- Provides ERROR386* to indicate whether the 387DX coprocessor is present at each CPU reset.
- Provides the 386PEREQ signal.
- Provides autodetection of the 387DX and 3167 coprocessors (no jumpers are required).
- Allows the 387DX and 3167 coprocessors to be installed at the same time (with optional coprocessor board).
- Reduces the number of pullup and pulldown resistors required by gating signals off inside the PAL if the respective coprocessor is not present.

Shown in Table 3-3 are the pin assignments for the interface PAL.

Table 3-3. PAL Pin Assignments

Inputs		Outputs	
Pin Number	**Pin Name**	**Pin Number**	**Pin Name**
1	387PEREQ	11	WTINTR
2	387BUSY*	12	386BUSY*
3	387ERROR*	13	BLOCKBUSY*
4	ADS*	14	387IRQ13
5	INTCLR	15	FLOP
6	RESET4	16	386ERROR*
7	RESET3	17	387PRESENT
8	REFRESH*	18	IRQ13
9	WTPRES*	19	386PEREQ
10	GND	20	PWR

PAL Output Signals

The PAL output signals at pins 12 through 19 are described in the following sections.

Pin 12, 386BUSY*

Signal 386BUSY* serves two functions. First, it indicates that the coprocessor is still excecuting a floating point instruction. Second, if sampled low by the 386DX coprocessor after a reset, it will force the 386DX to perform internal self-tests. This reduces the time it takes the 386DX to exit protected mode via a reset. Normally, when a coprocessor is not present 386BUSY* remains high. If the 387DX is present, 386BUSY* is the OR of the following signals:

- 387DX BUSY
- TOGGLE BUSY
- LATCHED BUSY.

TOGGLE BUSY toggles the busy signal once in a while when the 387DX is not present. This prevents system hangs with certain software packages that search for the presence of the coprocessor in ways that differ from Intel procedures.

LATCHED BUSY is part of what is required by the AT-compatible coprocessor hookup. It holds 386BUSY* active to the 386DX during an error condition, preventing the 386DX from sending a new instruction to the coprocessor before the error status can be read.

Pin 13, BLOCKBUSY*

BLOCKBUSY is low from the beginning of RESET3 until the first ADS*. It is used to prevent 386BUSY* from going active and allowing the 386DX to perform an internal self-test after a reset. This feature allows quick transistions from protected mode when RESET2* is used to reset the processor.

Pins 14 and 15, 387IRQ13

The 387IRQ13 signal is the output of a flipflop whose input is 387BUSY (inverted 387BUSY*) and whose clock is 387ERROR*. The flipflop is cleared when RESET4 is active or INTCLR is high (which occurs during IO writes to port 0F0). The output is held low if 387PRESENT is inactive.

Pin 16, 386ERROR*

386ERROR* is connected to the ERROR* pin on the 386DX coprocessor. This signal indicates either the presence of the 387DX or an error with a floating point operation. The 386DX samples the 386ERROR* pin between a reset and the first ADS* to determine whether a 387DX is present. If 386ERROR* is low, the 387DX assumes that the 387DX is present. 386ERROR* is driven high at all times exept when RESET3 is active until the first ADS*. During this time, if the 387DX is present, then 386ERROR* is driven low.

Pin 17, 387PRESENT

The 387PRESENT signal is used in conjunction with other signals. It is available on pin 17, but is not generally needed outside the PAL. A 387DX coprocessor will drive ERROR* low when it is reset, and will keep it low until it is initialized. If a 387DX is not there, a pullup keeps 387ERROR high.

387PRESENT is a transparent latch with ERROR* as the data input and RESET4 as the gate. When RESET4 (which occurs on a power up reset or RESET button push) is active (high), the latch is transparent. The output pin is inverted from the input, so a 1 indicates that the 387DX is present.

Pin 18, IRQ13

This pin is the OR of the 387DX interrupt and the 3167 interrupt. The 3167 busy signal (387BUSY*) is blocked off if the 3167 is not present. The 387DX interrupt will not occur if the 387DX is not present. (It is gated off in the 387IRQ13 term of this PAL.)

Pin 19, 386PEREQ

The "error" portion of this signal is the AND of the 387IRQ13 and 387BUSY* signals. A 386BUSY* will go high several clock cycles after the interrupt goes high.

If the 387DX is not present, the 386PEREQ signal remains low. This provision eliminates the need for a pull down resistor on this signal. If the 387DX is present, 386PEREQ is the OR of 387PEREQ and a signal that goes active following a 387DX error, after the 387DX becomes non-busy. This is required to clear out an internal flag in the 386DX and is a result of the non-standard coprocessor hookup for AT compatibles.

Cache and Tag Memory

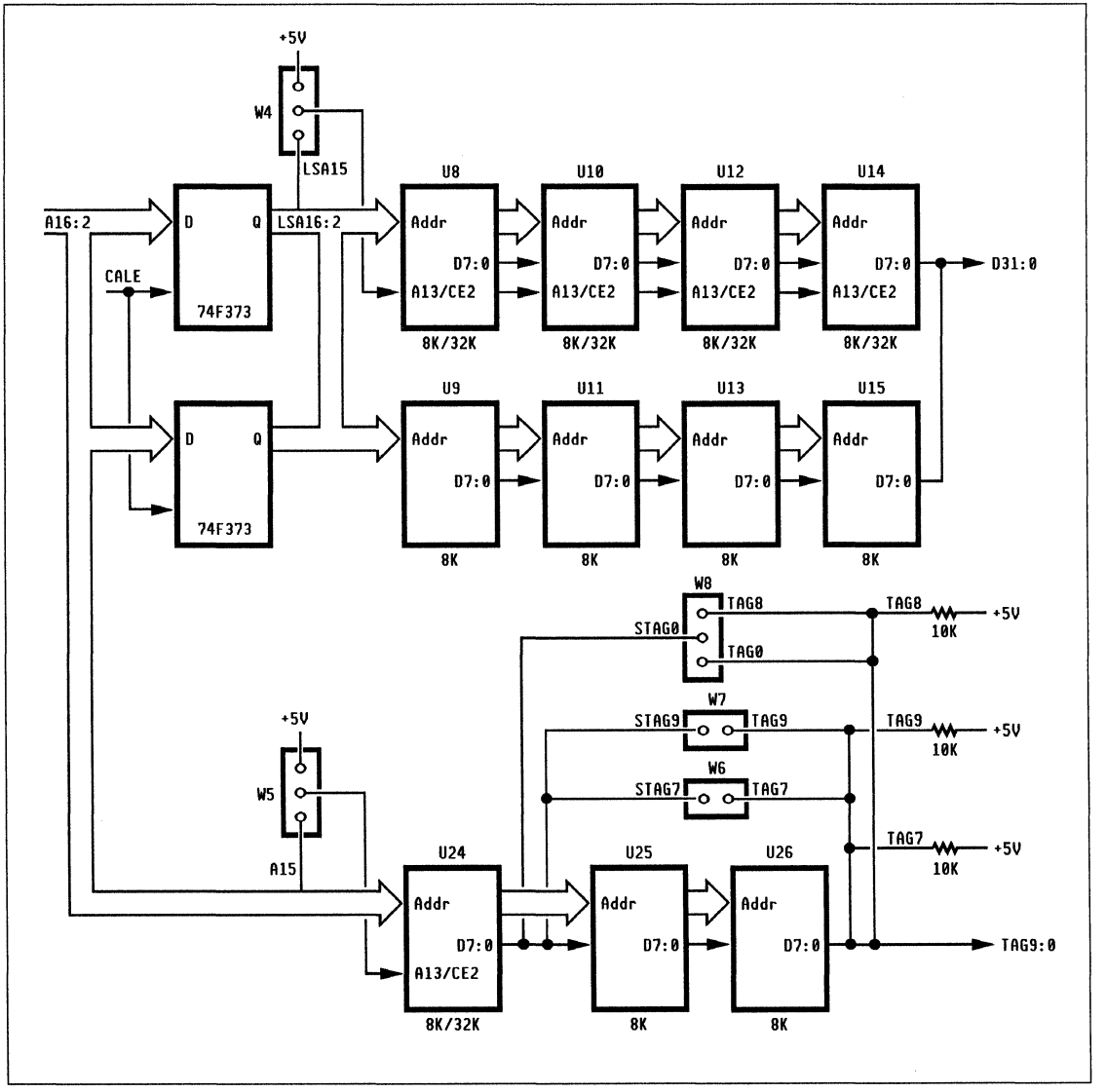
The MK82310-PI-Super system can be configured with 32kB, 64kB or 128kB of cache using off-the-shelf SRAMs. Eight 28-pin sockets are provided for the cache SRAM. Sockets U8, U10, U12 and U14 can accept either 32k x 8 or 8k x 8 SRAMs and are used for 32kB, 64kB or 128kB cache sizes. Sockets U9, U11, U13 and U15 accept only 8k x 8 SRAMs and are used for 64kB of cache memory. Detailed descriptions for implementing 32kB, 64kB, and 128kB of cache memory are given in the following sections of this chapter. Refer to Figure 3-1 for a schematic of the cache and tag SRAM.

PEAK/DM was designed with external tag memory, which is used to determine whether a block of memory resides in the cache memory. PEAK/DM utilizes a cache line size of four bytes with every tag entry pointing to or mapping four bytes of cache memory. Therefore, the tag memory depth is always one fourth the cache memory size. For example, tag memory with a depth of 8k is required for 32kB of cache memory. The width of the tag memory determines the amount of cacheable local memory.

The MK82310-PI-Super system allows for 8-bit, 9-bit, and 10-bit wide tag memory. Socket U24 can accept either 32k x 8 or 8k x 8 SRAMs and is used for 8k, 16k and 32k tag sizes. U25 accepts only an 8k x 8 SRAM and is used for 16k of tag memory. U26 is designed for a 16k x 4 SRAM and is used for the ninth and tenth tag bits. U26 is used for only the 32kB and 64kB cache modes.

When using 8-bit wide tag memory, be sure to use correct tag bits. PEAK/DM uses different combinations of tag bits for each cache size. For 32kB of cache memory, tag bits 0-6 and 9 are required. Tag bits 0-7 are used for 64kB of cache memory. Tag bits 1-8 are used for 128kB of cache memory. Jumpers are provided to configure the tag bits used by the SRAM in socket U24.

Figure 3-1. *Cache and Tag SRAM Schematic*



32kB Cache Configuration

To configure the MK82310-PI-Super board with 32kB of cache memory, you must populate the cache RAM and the tag RAM sockets with the correct speed and size SRAMs. Sockets U8, U10, U12 and U14 are used as the cache data RAM sockets. Populate these sockets must be populated with 8k x 8 DIP SRAMs. U24 and U26 are the tag RAM sockets. U24 with an 8k x 8 DIP SRAM; U26 can be optionally populated with a 16k x 4 DIP SRAM. Population of U26 is required for systems with more than 8MB of local memory and with 32kB or 64kB cache sizes. Sockets U9, U11, U13, U15, and U25 should not be populated. Table 3-4 lists the device requirements for implementing 32kB of cache.

Table 3-4. *32kB Cache Device Requirements*

CPU Speed		Sockets U8, U10, U12, U14	Socket U24	Socket U26 (Optional)
25MHz	Type	8k x 8	8k x 8	16k x 4
	Tacc	35ns	20ns	20ns
	Toe	20ns	N/A	N/A
33MHz	Type	8k x 8	8k x 8	16k x 4
	Tacc	25ns	15ns	15ns
	Toe	15ns	N/A	N/A
40MHz	Type	8k x 8	8k x 8	16k x 4
	Tacc	15ns	15ns	15ns
	Toe	12ns	N/A	N/A

Table 3-5 shows the jumper settings for 32kB cache mode with and without U26.

Table 3-5. *32kB Cache Jumper Requirements*

U26 Unpopulated (Up to 8MB of Memory)		U26 Populated (More than 8MB of Memory)	
Jumper	**Pins**	**Jumper**	**Pins**
W4	1-2	W4	1-2
W5	1-2	W5	1-2
W6	W6(1)-W7(1)[1]	W6	1-2
W7	W7(2)-W6(2)[1]	W7	1-2
W8	2-3	W8	2-3

[1] Refer to W6 and W7 descriptions in Chapter 2.

64kB Cache Configuration

To configure the MK82310-PI-Super system with 64kB of cache memory, you must populate the cache RAM and tag RAM sockets with the correct speed and size SRAMs. Sockets U8, U9, U10, U11, U12, U13, U14 and U15 are the cache RAM sockets. Populate these sockets with 8k x 8 DIP SRAMs. Sockets U24, U25 and U26 are tag RAM sockets. U24 and U25 must be populated with 8k x 8 DIP SRAMs. U26 can be optionally populated with a 16k x 4 DIP SRAM. Population of U26 is required for systems with greater than 16MB of local memory. Table 3-6 lists the device requirements for implementing 64kB of cache.

Table 3-6. 64kB Cache Device Requirements

CPU Speed		Sockets U8—U15	Sockets U24, U25	Socket U26 (Optional)
25MHz	Type	8k x 8	8k x 8	16k x 4
	Tacc	35ns	20ns	20ns
	Toe	20ns	N/A	N/A
33MHz	Type	8k x 8	8k x 8	16k x 4
	Tacc	25ns	15ns	15ns
	Toe	15ns	N/A	N/A
40MHz	Type	8k x 8	8k x 8	16k x 4
	Tacc	15ns	15ns	15ns
	Toe	12ns	N/A	N/A

Table 3-7 shows the jumper settings for 64kB cache mode with and without U26.

Table 3-7. 64kB Cache Jumper Configurations

U26 Unpopulated (Up to 16MB of Memory)		U26 Populated (More than 16MB of Memory)	
Jumper	Pins	Jumper	Pins
W4	2-3	W4	2-3
W5	2-3	W5	2-3
W6	1-2	W6	1-2
W7	1-2	W7	1-2
W8	2-3	W8	2-3

128kB Cache Configuration

To configure the MK82310-PI-Super system with 128kB of cache memory, you must populate the cache RAM and tag RAM sockets with the correct speed and size SRAMs. Sockets U8, U10, U12 and U14, the cache RAM sockets, must be populated with 32k x 8 DIP SRAMs. Socket U24, the tag RAM socket, must be populated with a 32k x 8 DIP SRAM. Sockets U9, U11, U13, U15, U25, and U26 should not be populated. Table 3-8 lists the device requirements for implementing 128kB of cache.

Table 3-8. 128kB Cache Device Requirements

CPU Speed		Sockets U8, U10, U12, U14	Sockets U24
25MHz	Type	32k x 8	32k x 8
	Tacc	35ns	20ns
	Toe	20ns	N/A
33MHz	Type	32k x 8	32k x 8
	Tacc	25ns	15ns
	Toe	15ns	N/A
40MHz	Type	32k x 8	32k x 8
	Tacc	15ns	15ns
	Toe	12ns	N/A

Table 3-9 shows the jumper settings for 128kB cache mode.

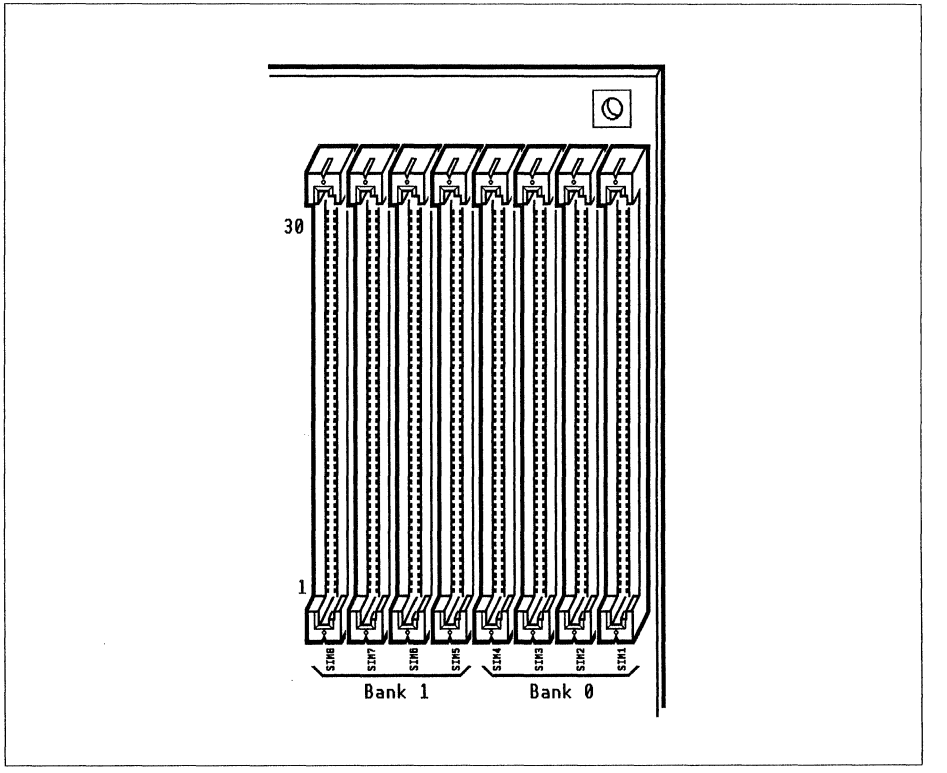
Table 3-9. 128kB Cache Jumper Configurations

Jumpers	Pins	Jumpers	Pins
W4	2-3	W7	1-2
W5	2-3	W8	1-2
W6	1-2		

Local Memory

The PEAK/DM memory controller, 82C351, supports up to four banks of memory in interleave mode. Each bank consists of 36-bit wide memory (32 data bits and 4 parity bits) and has a programmable starting address. This means each bank can contain a different type of memory, and can allow for contiguous memory. The MK82310-PI-Super system is designed with a main memory subsystem that supports 32-bit memory, up to two banks. Eight memory slots are available. Each memory slot is designed to accept a SIMM memory module and is capable of using 256k x 9, 1M x 9, or 4M x 9 DRAM SIMM modules. The two banks of memory allow memory expansion up to 32MB using 4M x 9 DRAM modules. Figure 3-2 shows the SIMM assignments.

Figure 3-2. *SIMM Socket Assignments*



SIMMs 1-4 are configured as bank 0. SIMMs 5-8 are configured as bank 1. The same type of memory must be placed placed in each bank if interleaving of banks is to be used. When only one bank is populated, bank 0 should be used. The MK82310-PI-Super board can be configured for different amounts of memory. Table 3-10 shows the possible memory configurations.

Table 3-10. *Possible Memory Configurations for the MK82310-PI-Super Board*

Bank 0	Bank 1	Memory
256k	Empty	1M
256k	256k	2MB
256k	1M	5MB
256k	4M	17MB
1M	Empty	4MB
1M	1M	8MB
1M	256k	5MB
1M	4M	20MB
4M	Empty	16MB
4M	4M	32MB
4M	256k	17MB
4M	1M	20MB

The access time for the local memory varies, depending on the speed of the CPU and the configuration settings used for the 82C351 controller. Consult the CS82310 data book for recommended register settings.

Mixed memory not only allows two different sizes of DRAMs to be installed, it also allows two different speeds of DRAMs. For example, Bank 0 can contain 256kB 80ns DRAMs and bank 1 can contain 1MB 100ns DRAMs. In this example, accesses to Bank 0 will be faster than to Bank 1. Without mixed memory, accesses to both blocks would be slower due to the 100ns DRAMs.

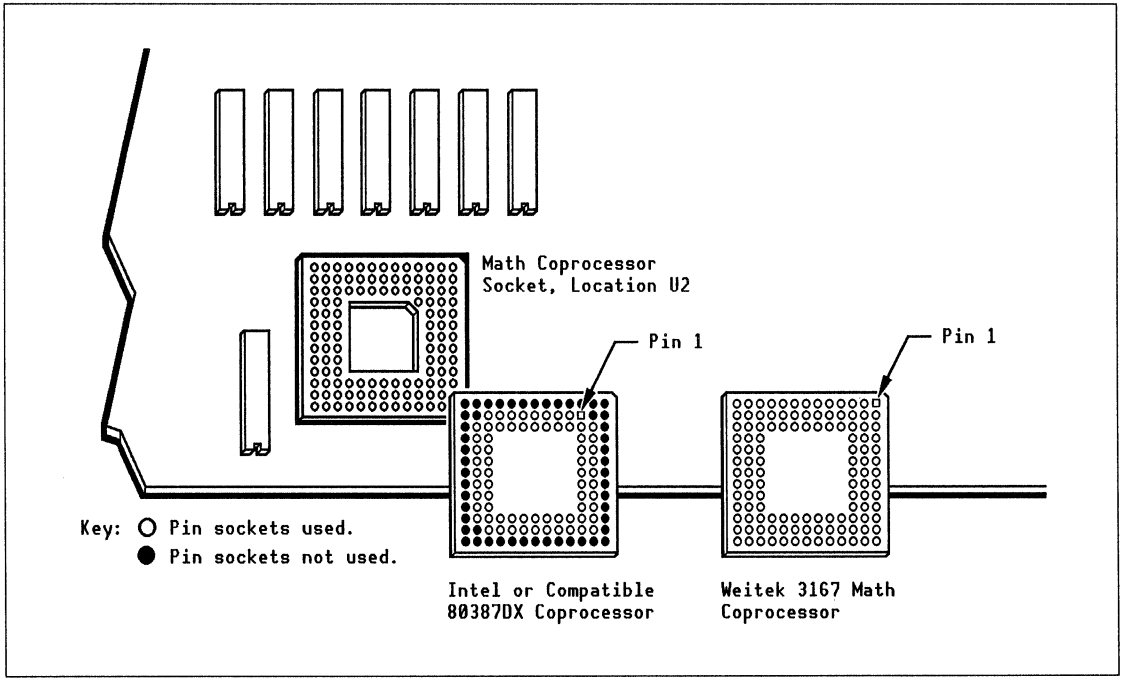
Math Coprocessors

The MK82310-PI-Super system can accept the Intel 80387DX coprocessor, an 80387 DX compatible coprocessor such as the CHIPS SuperMathDX coprocessor, or the Weitek 3167 math coprocessor. Socket U2 is a 121 PGA Extended Math Coprocessor (EMC) socket that can accept any of these coproessors. No jumpers are required when installing a math coprocessor. The system has been designed to detect automatically the presence of either a 387DX or Weitek 3167 coprocessor.

Intel 80387DX or Compatible Coprocessor

An Intel 80387DX or compatible math coprocessor can be installed in the center of the U2 EMC socket. Figure 3-3 shows the location of pin number 1 and the orientation of a 80387DX device. The white circles are the pin sockets for the 80387DX coprocessor. The black circles are unused pin sockets. The white square indicates the location of pin 1.

Figure 3-3. *Intel or Compatible 80387DX and Weitek 3167 Pin Placement*



Weitek 3167

The MK82310-PI-Super system also supports the Weitek 3167 math coprocessor. The 3167 coprocessor plugs directly into the U2 socket. Note that the Weitek 3167 does not support programs using the 80387DX instruction set. No jumpers or switches are required to install the 3167; the MK82310-PI-Super will automatically detect its presence. Figure 3-3 designates pin 1 as a white square pin socket for the Weitek 3167 math coprocessor.

Board Testing Features

The MK82310-PI-Super board has been designed to accommodate "bed of nail testing." When possible, the control signals for TTL logic, which are normally tied to ground or Vcc, have been pulled active using 150-ohm resistors. Enable and input signals for the PEAK/DM devices are pulled active or inactive using 2.2k ohm resistors. Signals that are not used in this design or are not routed on the botton signal layer have a test pad located on the botton of the PCB. The signals requiring a test pad are listed in Table 3-11.

Table 3-11. *Signals Requiring Test Pads*

Reference Number	Signal Name	Reference Number	Signal Name
XTP1	ACEN*	XTP11	AC1
XTP2	AEN16*	XTP12	AC2
XTP3	AEN8*	XTP13	AC3
XTP4	ATEN*	XTP14	BWBUSY
XTP5	DRD*	XTP15	HLDA1
XTP6	INTA*	XTP16	HRQ1
XTP7	LDBEN*	XTP17	LDBDIR
XTP8	*******	XTP18	REFREQ
XTP9	PEN*	XTP19	XA0
XTP10	AC0	XTP20	XA1

All other signals can be accessed using either a via or a pad. All mounting holes are electrically connected to ground.

MK82310-PI-Super Mounting Holes

The PC board provides mounting holes for an XT, AT, and baby AT board. Only certain groups of mounting holes are used for each type of chassis. Figure 3-4, a simple mechanical drawing of the MK82310-PI-Super board, designates the mounting holes used for the XT, AT, and baby AT chassis.

Adapter Board Specifications and Limitations

The main memory is easily accessible. However, the SIMM sockets limit the size of adapter boards in particular AT slots. AT slots 1, 2, and 3 will only accept a maximum two-thirds length adapter card for a fully populated memory system. On the other hand, if only bank 0 is populated, then AT slot 3 can accept a full length adapter card, while AT slots 1 and 2 will only accept adapter cards up to two-thirds length.

Figure 3-5 shows the relationship between the SIMM sockets and the AT adapter I/O slots. Only slots 1, 2 and 3 are limited by the SIMM sockets. Slots 4, 6, and 8 can accept full-length AT or XT adapter boards. Slot 5 can accept a deep style XT adapter board. However, you can modify this slot to accept 16-bit or AT style adapter boards by populating J10 with a 36-pin socket. Due to the location of the single system BIOS ROM, slot 7 can only accept XT style adapter boards.

Figure 3-4. *MK82310-PI-Super Board Mounting Holes*

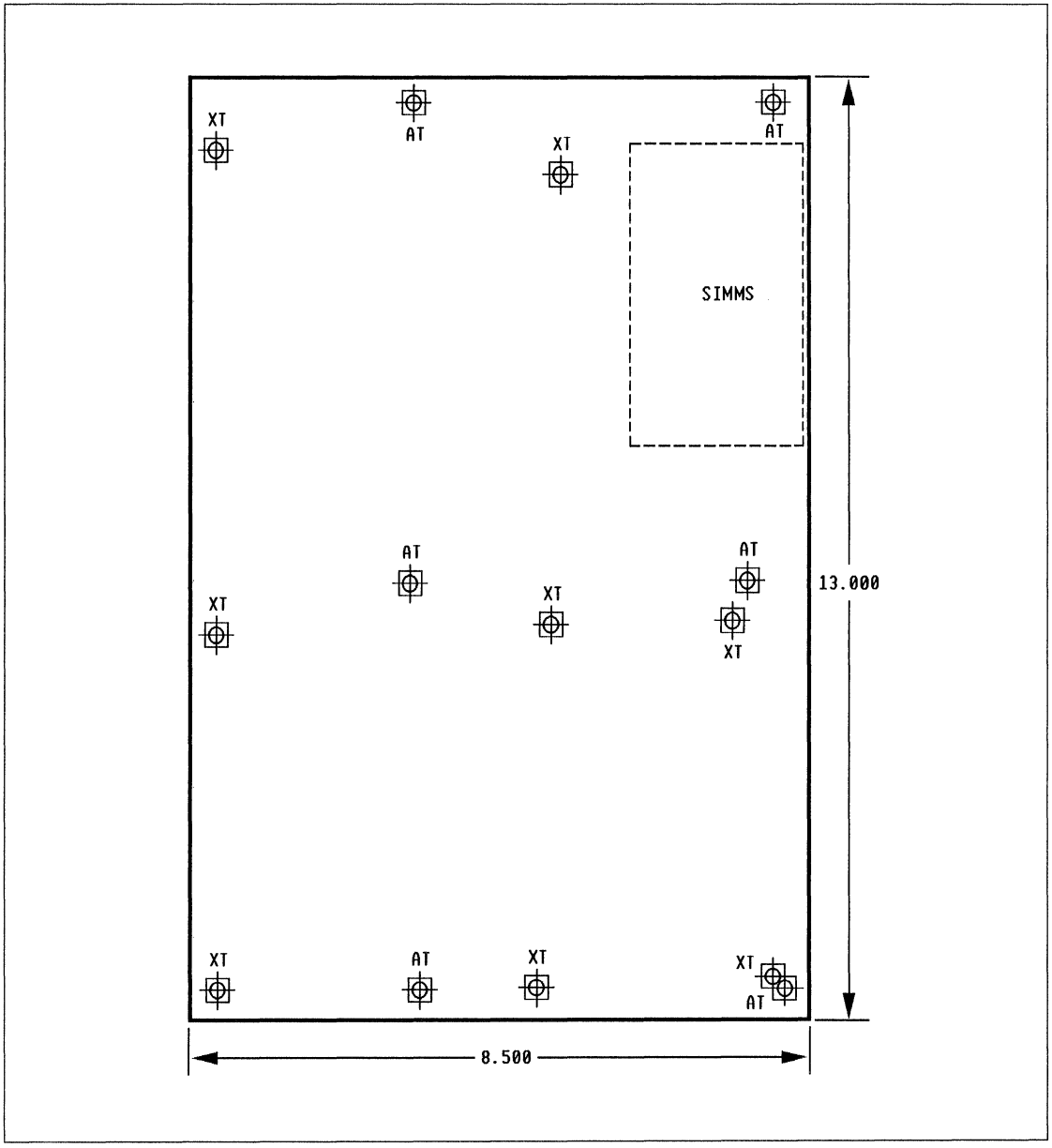
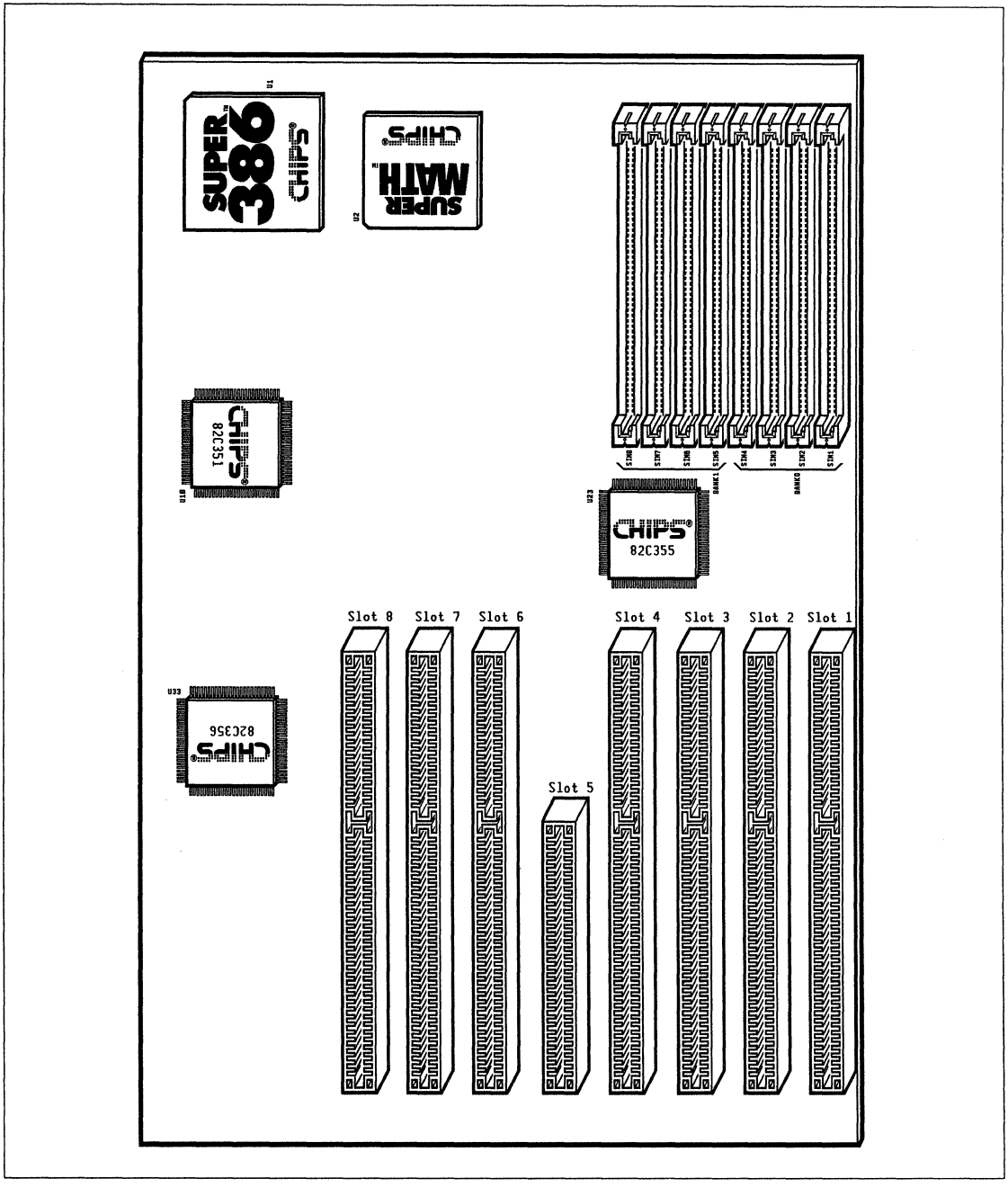


Figure 3-5. Adapter I/O Slot Locations



The only dimensions affected by the placement of the SIMM sockets on the MK82310-PI-Super board are the distance from the 36-pin I/O connector (C1-C18) to the end of the board, the depth of the board from the top of the AT I/O connector, and the depth of the board near the bracket end of the board. The depth of the adapter boards is limited by the devices located under the adapter boards (i.e., ICs, resistors, capacitors, and resistor packs). This distance is limited to 0.5 inch from the top of the I/O connector to the bottom of the adapter board.

Figure 3-6 shows the specific demensions for a full-length AT adapter board.

Figure 3-6. *AT Adapter Board, Full-Length*

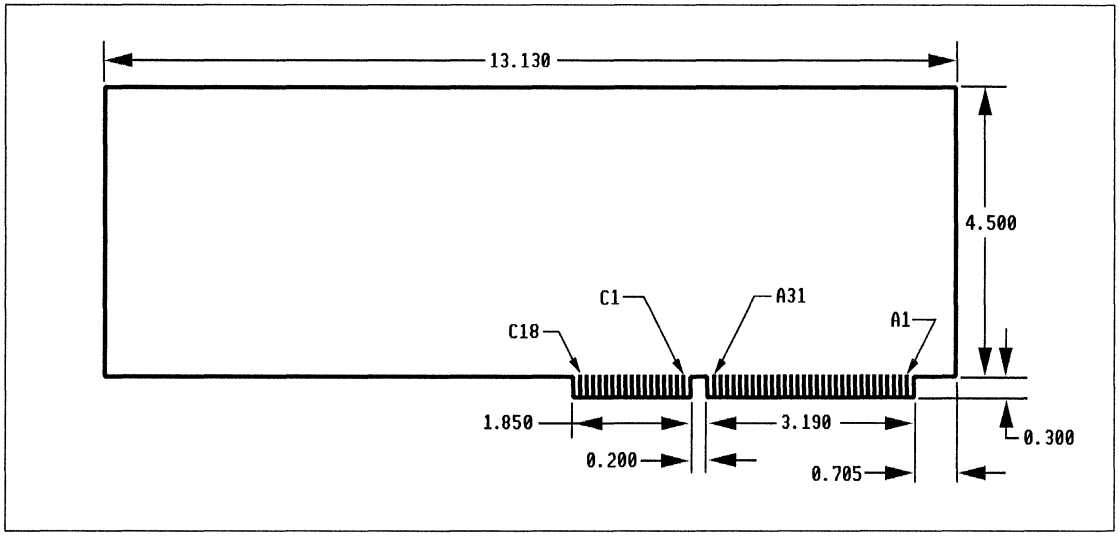
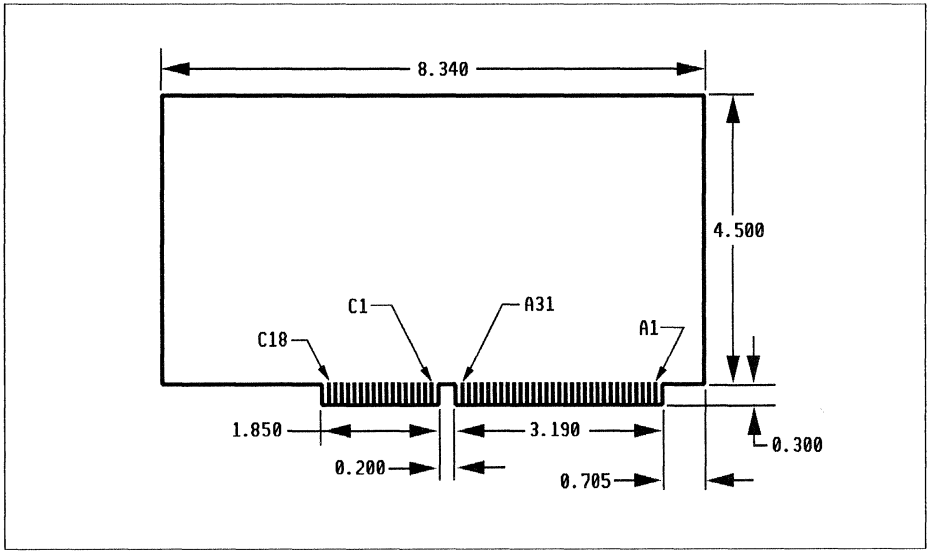


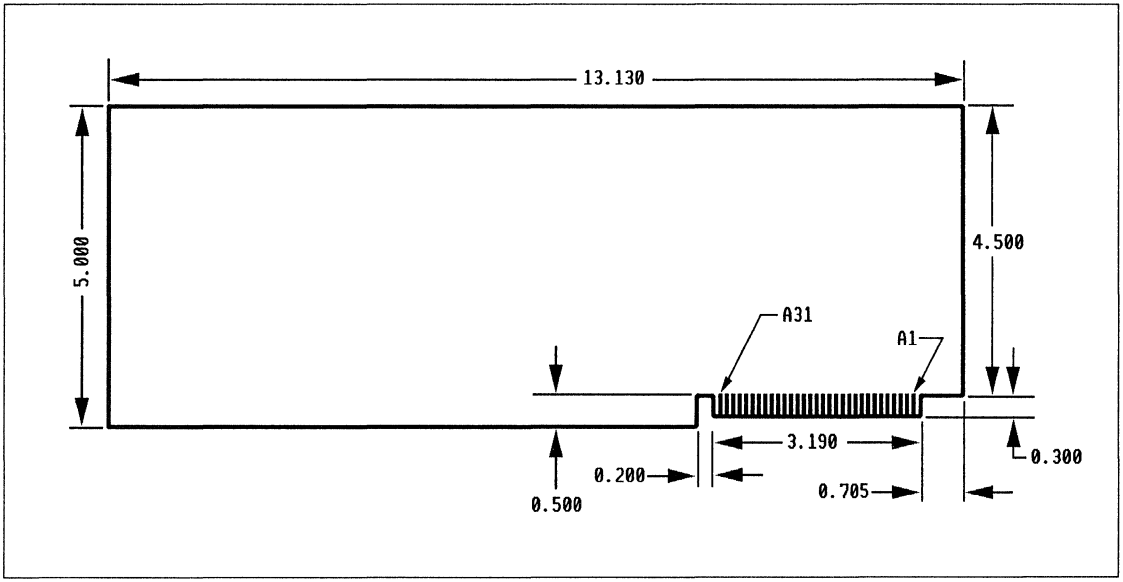
Figure 3-7 shows the maximum length of an AT board in I/O slots 1 and 2.

Figure 3-7. *AT Adapter Board, Two-Thirds Length*



AT slot 5 on the MK82310-PI-Super board accommodates XT adapter boards with PCB depths below the 8-bit I/O connector. XT cards can have depths up to 0.5 inch below the 8-bit I/O connector. Note that AT slot 5 can be optionally populated with an 8-bit or 16-bit I/O connector. The MK82310-PI-Super is shipped with AT slot 5 configured as an 8-bit slot. Figure 3-8 shows the XT deep slot adapter board dimensions.

Figure 3-8. *XT Deep Slot Adapter Board Dimensions*



APPENDIX A

Bill of Materials

Table A-1 provides the quantity, type, and description for each part used in the MK82310-PI-Super board design.

Table A-1. *Product Number Table*

Item	Qnty.	Part	Type	Description	Designator
1	1	Batt		NICAD, 3.6V	BT1
2	1	Cap	100 pf	Mono, +80%/-20%, Axial	C135
3	3	Cap	27 pf	Mono, +80%/-20%, Axial	C87, C96, C98
4	2	Cap	47 pf	Mono, +80%/-20%, Axial	C126, C127
5	1	Cap	4700 pf	Mono, +80%/-20%, Axial	C105
6	2	Cap	0.001µF	Mono, +80%/-20%, Axial	C82, C106
7	73	Cap	0.1 µF	Mono, +80%/-20%, Axial	C5, C7, C8, C11, C12, C15, C16, C17, C18, C19, C20, C23, C24, C25, C26, C27, C28, C30, C31, C32, C33, C35, C36, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C49, C50, C51, C52, C54, C55, C57, C58, C59, C60, C61, C62, C64, C65, C66, C67, C69, C70, C71, C72, C73, C75, C78, C79, C80, C81, C83, C86, C88, C89, C92, C93, C94, C95, C99, C100, C101, C102, C103, C104, C124, C125, C128, C129, C130, C132, C133, C134

Table A-1. *Product Number Table (continued)*

Item	Qnty.	Part	Type	Description	Designator
8	8	Cap	1.0μF	Ceramic, Axial, 5% 50V	C3, C4, C6, C9, C10, C13, C29, C34
9	30	Cap	10 μF	Tant Radial .125 16V	C2, C14, C22, C37, C53, C56, C57, C74, C76, C77, C78, C83, C84, C85, C90, C91, C92, C93, C94, C95, C97, C107, C110, C112, C117, C118, C120, C121, C124, C131
10	11	Cap	22 μF	Tant Radial .125 16V	C48, C108, C109, C111, C113, C114, C115, C116, C119, C122, C123
11	3	Choke	100 pF	EMI Filter, 3 leg cap	CH1, CH2, CH3
12	4	Diode	1 N4148	Signal Diode	D1, D2, D3, D4
13	1	Diode	1 N5818	Schotky Diode	D5
14	1	Ref. Doc		Schematic Drawings	DOC2
15	1	Ref. Doc		Fabrication Drawings	DOC3
16	1	Ref. Doc		Assembly Drawings	DOC1
17	1	Fuse	Fuse	Microfuse	F1
18	1	Conn	5-pin	Keyboard, Shielded DIN	J5
19	1	Conn	CON31	AT 8-bit IO Channel	J9A
20	7	Conn	CON31	Comb. Con 2 x 31 and 2 x 18	J1A, J3A, J5A, J7A, J13A, J11A, J15A
21	1	Header	CON4	.1", Keyed (Spkr)	J1
22	1	Header	CON4	.1", Keyed (Bstt)	J4
23	1	Header	CON5	.1", Unshrouded	J2
24	1	Header	JMP2	.1" (Reset)	J3
25	1	Osc	80MHz	Osc, .01%, 60/40, DIP 14	OSC2
26	1	Osc	16MHz	Osc, .01%, 60/40, DIP 14	OSC1
27	1	Conn	CON12	.156" (AT Pwr Conn)	P1
28	1	Fab	Rev. F	Bare Fab	PCB
29	1	Xsister	2N3904	NPN, TO-92	Q1
30	1	Xsister	2N6732	PNP, TO-92	Q2
31	3	Res	1k	Carbon Film, 1/4W, 5%	R53, R55, R56
32	1	Res	1.2k	Carbon Film, 1/4W, 5%	R66
33	9	Res	10k	Carbon Film, 1/4W, 5%	R1, R23, R28, R32, R37, R38, R42, R45, R58

Table A-1. Product Number Table (continued)

Item	Qnty.	Part	Type	Description	Designator
34	8	Res	2.2k	Carbon Film, 1/4W, 5%	R2, R4, R10, R13, R40, R44, R59, R60
35	4	Res	4.7k	Carbon Film, 1/4W, 5%	R21, R39, R61, R62
36	1	Res	51k	Carbon Film, 1/4W, 5%	R57
37	1	Res	1.2k	Carbon Film, 1/4W, 5%	R47
38	1	Res	2M	Carbon Film, 1/4W, 5%	R51
39	2	Res	10-ohm	Carbon Film, 1/4W, 5%	R41, R43
40	10	Res	150-ohm	Carbon Film, 1/4W, 5%	R5, R9, R12, R17, R29, R30, R31, R36, R52, R54
41	3	Res	220-ohm	Carbon Film, 1/4W, 5%	R6, R7, R63
42	15	Res	33-ohm	Carbon Film, 1/4W, 5%	R11, R14, R18, R19, R20, R22, R24, R25, R26, R27, R33, R48, R49, R50, R65
43	2	Res	54-ohm	Carbon Film, 1/4W, 5%	R15, R16
44	1	Res	680-ohm	Carbon Film, 1/4W, 5%	R3
45	2	Rpack	10k x 7	8-pin SIP x 7	RP16, RP20
46	8	Rpack	10k x 9	10-pin SIP x 9	RP1, RP2, RP12, RP14, RP15, RP17, RP18, RP22
47	1	Rpack	2.2k x 7	8-pin SIP x 7	RP10
48	1	Rpack	330 x 7	8-pin SIP x 7	RP21
49	9	Rpack	33 x 4	8-pin SIP x 7	RP3, RP4, RP5, RP6, RP7, RP8, RP9, RP11, RP13
50	1	Rpack	4.7k x 9	10-pin SIP x 9	RP19
51	4	Shunt	1, 2	.1" Insulated	SH6, SH7, SH9, SH10
52	5	Shunt	2, 3	.1" Insulated	SH4, SH5, SH8, SH11, SH12
53	8	SIMM	SIM227	256k x 9, 60ns, 30P, SIP	SIM1, SIM2, SIM3, SIM4, SIM5, SIM6, SIM7, SIM8
54	1	IC	74ACT02	14-pin DIP	U19
55	1	IC	74ACT04	14-pin DIP	U38
56	1	IC	74ACT74	14-pin DIP	U28
57	1	IC	74175	16-pin DIP	U20
58	5	IC	74F244	20-pin DIP	U4, U5, U16, U17, U35
59	4	IC	74F245	20-pin DIP	U27, U30, U31, U40

Table A-1. Product Number Table (continued)

Item	Qnty.	Part	Type	Description	Designator
60	2	IC	74F32	14-pin DIP	U21, U22
61	3	IC	74F373	20-pin DIP	U6, U7, U34
62	1	IC	74S05	14-pin DIP	U39
63	1	VLSI	80386-40	132-pin PGA	U1
64	1	VLSI	82C351B-40	160-pin QFP	U18
65	1	VLSI	82C355	120-pin QFP	U23
66	1	VLSI	82C356	144-pin QFP	U33
67	10	SRAM	8k x 8	28-pin DIP, 15ns, .3"	U8, U9, U10, U11, U12, U13, U14, U15, U24, U25
68	1	1C	BIOS	512k EPROM	U32
69	1	VLSI	KBD Cntlr	40-pin DIP, .6", Skt	U37
70	1	IC	MC14069	14-pin DIP	U36
71	1	PAL	PAL 16L8B	DIP 20	U3
72	1	SRAM	SRAM 16k x 4	22-pin DIP, 15ns	U26
73	1	IC	TL7705A	8-pin DIP	U41
74	6	Header	JMP2	.1" (Reset)	W1, W2, W3, W6, W7, W9
75	6	Header	JMP3	.1", Unshrouded	W4, W5, W8, W10, W11, W12
76	1	Socket	4-pin	4-pin Osc Skt, 14 FTPR	XOSC2
77	8	Socket	30-pin	Straight SIMM	XSIM1, XSIM2, XSIM3, XSIM4, XSIM5, XSIM6, XSIM7, XSIM8
78	1	Socket	121-pin	PGA	XU2
79	1	Socket	176-pin	PGA	XU1
80	1	Socket	20-pin	DIP .3"	XU3
81	11	Socket	22-pin	DIP .3"	XU26
82	10	Socket	28-pin	DIP .3"	XU8, XU9, XU10, XU10, XU13, XU14, XU15, XU24, XU25
83	1	Socket	28-pin	DIP .6"	XU32
84	1	Socket	40-pin	DIP .6"	XU37
85	1	XTAL	32.768 kHz	MICRO	Y2
86	1	XTAL	14.318 MHz	HC18U	Y1
87	1	Test	MK82310	Test Procedure	

APPENDIX B

PAL Logic Equations

The PAL logic equations are as follows:

```
386PEREQ        = 387BUSY* & 387IRQ13 & 387PRESENT
                        + 387PEREQ & 387PRESENT;

387PRESENT      = -(387ERROR* & RESET4
                        + RESET4* & 387PRESENT*
                        + 387ERROR* & 387PRESENT*);

BLOCKBUSY       = RESET3 + ADS* & BLOCKBUSY;

386BUSY         = 387BUSY & BLOCKBUSY* & 387PRESENT
                        + REFRESH & BLOCKBUSY* & 387PRESENT*
                        + 387IRQ13 & BLOCKBUSY*;

FLOP            = (387BUSY* & 387ERROR*
                        + 387ERROR & FLOP*
                        + 387BUSY* & FLOP*
                        + INTCLR + RESET4);

387IRQ13        = -(FLOP* & 387ERROR
                        + 387ERROR* & 387IRQ13*
                        + 387IRQ13* & FLOP*
                        + INTCLR
                        + RESET4
                        + 387PRESENT*);

IRQ13           = 387IRQ13 + WTINTR & WTPRES;
```

Note: "+" is equivalent to a logical OR, and "&" is equivalent to a logical AND.

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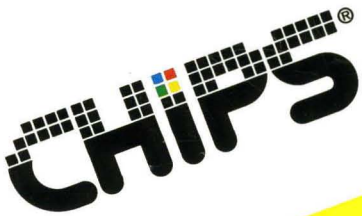

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