Data Book

AT&T

Analog Integrated Circuits

June 1988

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Acknowledgement

Since 1925, the year Bell Laboratories was founded, AT&T has developed some 21,000 patents, or the phenomenal equivalent of a new discovery every day for more than 60 years. It becomes immediately apparent that the single, most unexpendable ingredient contributing to our success is innovation.

In view of this, we welcome the opportunity to fittingly address the efforts and consistent breakthrough accomplishments of our system and design engineers. It is proudly noted, the critical strength of AT&T rests within the human resources of our research partner, Bell Laboratories.

GENERAL

Introduction

AT&T's Reading Works today emerges as one of the world's largest producers of analog integrated circuits, based on our total annual manufacturing volume. Our lofty status and reputation in the electronic industry is the offspring of a continual commitment to analog technology, quality and reliability, and customer satisfaction—in short, a commitment to excellence.

Our heritage is marked by sophisticated accomplishments, progressing steadily from vacuum tubes to microelectronics. But rather than rest on residual success, our solid foundation of achievements tends to stimulate even more discovery—innovation based on experience. Conclusively, along with the variety of inventions outlined in the following pages, you may rightfully expect new developments, diversified applications, proven procedures, and flexible product offerings.

The assortment of analog devices discussed here spans a number of technologies, and gives analog circuit designers an opportunity for selective product evaluation. Wherever possible, the device specifications are certified and supported by significant test and performance data. Devices are further characterized by a low mortality rate and extended service life. The successful application of any component, however, is contingent upon close adherence to the recommended operating procedures, concurrent with maximum device limitations.

Ordering information and technical assistance is available through the AT&T sales force.

Interfacing with AT&T

To place an order, or to inquire about pricing, delivery, or models and availability, contact an AT&T account manager at the nearest regional domestic sales office (listed below), or call 1-800-372-2447.

AT&T Microelectronics

Domestic Regional Sales Office Directory
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1650 W. 82nd St., Suite 700
Bloomington, MN 55431
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(817) 354-9798

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Phoenix, AZ 85008
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AZ, NM, El Paso

500 Park Boulevard
Suite 270
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(312) 250-9777

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16461 Sherman Way - Suite 250
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Portland, OR 97223
(503) 244-3883

WA, OR, ID, MT, AK, BC

AT&T's Analog IC Achievements

As a world-leading manufacturer of linear bipolar and high voltage integrated circuits, we are continually advancing the analog technologies that have brought us to the forefront in the semiconductor market place. During the past two decades, our technologies have evolved methodically in response to the growing complexities of modern communication systems. Today, more than ever, our concentrated research efforts and manufacturing superiority provide a sound basis to serve new developments and diversified applications.

Linear Bipolar Technology Showcase

The succession of milestones in bipolar development is indicative of our ongoing commitment to IC technology and applications:

- 1965—the first bipolar circuits are introduced using 12-volt, standard buried collector (SBC) technology.
- 1968—SBC technology is extended to provide 30-volt capability for catalog op amps.
- 1973—the first complementary bipolar integrated circuits (CBIC) are manufactured, offering 30-volt capability.
- 1977—CBIC/buried injector logic (BIL) is established.
- 1978/79—Silicon tantalum integrated circuits (STIC) and bipolar field-effect transistors (BIFET) are developed.
- 1983—90-volt CBIC is introduced.
- 1986—CBIC-U becomes part of AT&T's high-speed silicon IC family for ultra-high frequency lightwave applications (2.5—4.0 GHz).
- 1987—Semi-custom linear arrays, characterized by the most technological capabilities in the industry, are introduced. Arrays include CBIC-U 12 volt, CBIC-R 33 volt, and CBIC-S 90 volt capability.

It became clear during the early '70s that the potential of analog IC design had outgrown SBC technology. CBIC was then developed by Bell Laboratories at Reading as a natural fit with circuit design efficiency, offering power-miser level shifting, a push-pull output stage with low quiescent power and RFI immunity, symmetric current sources, up/down emitter followers, and fundamental power and speed advantages.

As a result of our CBIC innovations, AT&T today holds prominence in the analog IC arena. CBIC's high-performance circuit design features include vertically-structured NPN and PNP transistors on the same chip.

The true strength of CBIC technology, however, is high speed and low quiescent power. Device designs using CBIC technology can include all of the following attributes:

- BIL—analog and digital functions on the same chip.
- STIC—compact, precision thin-film resistors on the same chip; temperature coefficient of 200 ppm/°C.
- BIFET—precisely controlled pinch-off voltage of 0.7—10 V; resistor values of 25—2000 ohms/sq.; metal nitride oxide silicon (MNOS) capacitors with a value range of 1—1000 pF.

To promote an efficient use of silicon, all of the technologies can be designed with two-level metal interconnections.

Statistics show our average out-going quality (AOQL) products to be better than 250 ppm and our goal is to achieve 50 ppm by 1990. We have demonstrated high reliability of less than 25 FITs.

High-Voltage IC Technology (Dielectric Isolation)

High-voltage ICs (HVIC) designed by AT&T Bell Laboratories exhibit a breakdown voltage in excess of 100 V. Fabricated using a bipolar technology, the high-voltage product line is based on our Gated-Diode Crosspoint (GDX) family of ICs. GDX devices are generally used in highly specialized applications.

AT&T's Analog IC Achievements
(Continued)

In the early 1980s, as HVIC application opportunities expanded to include the areas of telecommunications, display drivers, and motor controllers, GDX technology gave way to yet another new development. MOS/Bipolar technology, including (but not limited to) complementary low-voltage MOS and high-voltage DMOS devices, emerged as BCDMOS technology. Currently, this technology has found applications in devices such as telephone interface circuits and solid-state relays, all requiring bipolar and DMOS architectures.

While GDX and BCDMOS both use dielectric isolation, BCDMOS offers greater flexibility in the variety of devices that can be fabricated with a single chip containing multiple components and technologies. Examples include DMOS transistors, SCRs, vertical NPN and lateral PNP transistors, and capacitors with voltage ratings of at least 300 V.

Today, typical BCDMOS applications include switches or relay replacements with minimal on-resistance, surge handling capability up to 10 amps, and dc current ratings of approximately 200 mA. Most applications require chip sizes of 10—30 mm^2; power dissipation ranges from 1—10 W.

Because of the power requirements necessary to achieve high speed at high voltage, power dissipation is usually a stronger consideration than inherent speed. However, AT&T does offer low-voltage CMOS products that operate at high speeds on the same chip—a data latch, for example. Current CMOS devices in BCDMOS technology can deliver clock rates of 10—50 MHz.

Using a number of special techniques, the limits of our high-voltage devices have been spiraling upward. Individual breakdown voltages have reached 500 V. By stacking devices, breakdown voltages of 1000 V are possible. Using level-shifting or capacitive-coupling of control signals, 500—1000 V input/output isolation can be achieved. And with the optoisolator packaging capabilities at the Reading Works, 2500—3750 V input/output isolation is available.

Although the new technologies are quite versatile, our competitive edge is superiority in manufacturing. In addition to being the world's largest producer of HVICs, AT&T Reading Works is the most experienced in testing and packaging highly reliable parts.

Applications: Telecommunications and Beyond

While linear bipolar and high voltage ICs are used popularly in the communication industry, there are considerable opportunities for allied applications in other fields. In general, AT&T devices provide cost-effective solutions for a significant number of applications required in consumer, industrial and instrumentation products. The listings below are not comprehensive, although they do provide an overview of the types of applications and their associated devices.

Applications	Compatible Devices
Communications	
■ Voice, DTE, Systems	■ Protection devices
■ Local Area Networks	■ Line/battery feeds
■ Modems	■ Analog switches
	■ Line receivers/drivers
	■ Voice-frequency op amps
	■ Compandors
	■ Wide-band op amps
	■ Level expanders
	■ Transceivers
	■ Clock recovery circuits
Consumer Products	
■ Telephones	■ Telephone ICs
■ Home appliances -dishwashers -ovens -lighting	■ Speakerphone devices
	■ MOSFET Gate Arrays
	■ Op amps
	■ Voltage-controlled oscillators
	■ Tone decoders
	■ Voice-signal conditioners
	■ Tone ringers
	■ Solid-State Relays

Applications: Telecommunications and Beyond
(Continued)

Industry

- Test equipment
- Computers and peripherals
- Automotive electronics
- CAD/CAM equipment
- Power equipment
- Aerospace electronics
- Factory automation equipment
- Regulation controllers
- Precision voltage referencers
- Power controllers
- Solid-state relays
- Pulse-width modulators
- Relay drivers
- Op amps
- MOSFET Gate Arrays

Instrumentation

- Process control equipment
- Medical equipment
- Sensors
- Detectors
- Sonar monitors
- Oscillators
- Phase-locked loops
- Analog multipliers
- Comparators
- Sample-and-hold amps
- Micropower op amps
- Relay timers
- Timing circuits

Custom Designs

- Microwave equipment
- 90-volt equipment
- General-purpose high-voltage devices
- High-voltage digital-to-linear interfaces
- P/N channels
- Level translators
- Semi-custom linear arrays
- MOSFET gate arrays

Data Sheet Categories, Commercial Products Linear and High Voltage IC Devices

Description

Data Sheets fall into the following three categories:

1. **ADVANCE:** This Data Sheet is issued as soon as possible after the conceptual characteristics of the device have been established. Electrical characteristics are usually based on computer simulation results. An Advance Data Sheet (sample devices are not necessarily available at this time) is issued prior to the fabrication of initial models.

   CAUTION: The ADVANCE Data Sheet is intended to serve as a product announcement. All aspects such as functionality, specification, packages and pin-outs are subject to change.

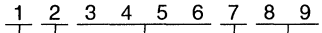
2. **PRELIMINARY:** This Data Sheet is issued as soon as possible after pre-production device models have been fabricated. Typical electrical characteristic curves are obtained from these devices (test specifications are not necessarily finalized at this time).

3. **FINAL:** Data Sheets without a status indicator are classified as Final. These data sheets are issued after a statistically significant amount of product has been manufactured. These Data Sheets contain primary testing characteristics of the device.

Coding: Linear, Digital and High-Voltage IC Devices

AT&T has developed a method for coding linear, digital and high-voltage integrated circuits consistent with general trade practices. The new coding scheme characterizes devices according to functional classification, technology, device identifier, electrical, temperature, family variant, and package type as outlined in Figure 1.

Coding: Linear, Digital and High-Voltage IC Devices (Continued)



Package Configuration—Alpha suffix designators for package variations.①

Omission of characters in positions 8 and 9 identifies the device as being in chip form.

A	=	Wafer②	W	=	16-Pin SONB
B	=	8-Pin DIP	X	=	Special Package
C	=	16-Pin DIP	Y	=	20-Pin SOG
D	=	18-Pin DIP	AA	=	Thinned Wafer
E	=	20-Pin DIP	AB	=	6-Pin Gull Wing
F	=	24-Pin DIP	AC	=	8-Pin Gull Wing
G	=	28-Pin DIP	AD	=	44-Pin Ceramic Chip Carrier
H	=	32-Pin DIP	AE	=	16-Pin SOG
J	=	40-Pin DIP	AF	=	14-Pin SONB
K	=	16-Pin SOJ	AG	=	32-Pin Ceramic Chip Carrier
L	=	20-Pin SOJ	AH	=	28-Pin SOTB
M	=	28-Pin SOJ	AJ	=	28-Pin SOG
N	=	Reserved	AK	=	24-Pin Ceramic Chip Carrier
P	=	44-Pin PLCC	AL	=	28-Pin Ceramic Chip Carrier
R	=	68-Pin PLCC	AM	=	3-Lead Plastic
S	=	8-Pin SONB	AN	=	48-Pin Ceramic Chip Carrier
T	=	6-Pin DIP	AP	=	14-Pin DIP
U	=	Unassigned	AT	=	Tab-Bonded Chip

Electrical, Temperature, or Family Variation—Alpha Suffix Designator

Device Identifier—Alphanumeric Designator

Technology-Alpha Designator to Identify Technology

B	=	CBIC
C	=	CMOS
G	=	Gallium Arsenide
H	=	High Voltage
J	=	MJIM
S	=	SBC

Classification—Alpha Designator to Identify Type of Device

B	=	Building Blocks/Transistor Array IC
D	=	Digital IC
H	=	Hybrid IC
L	=	Linear IC (May contain some digital functions)
U	=	Microwave IC

Figure 1. Coding Scheme

① For specific package dimensions, see individual Data Sheets.
② Devices are shipped in wafer form to the customer who is then responsible for subsequent processing to obtain usable chips.

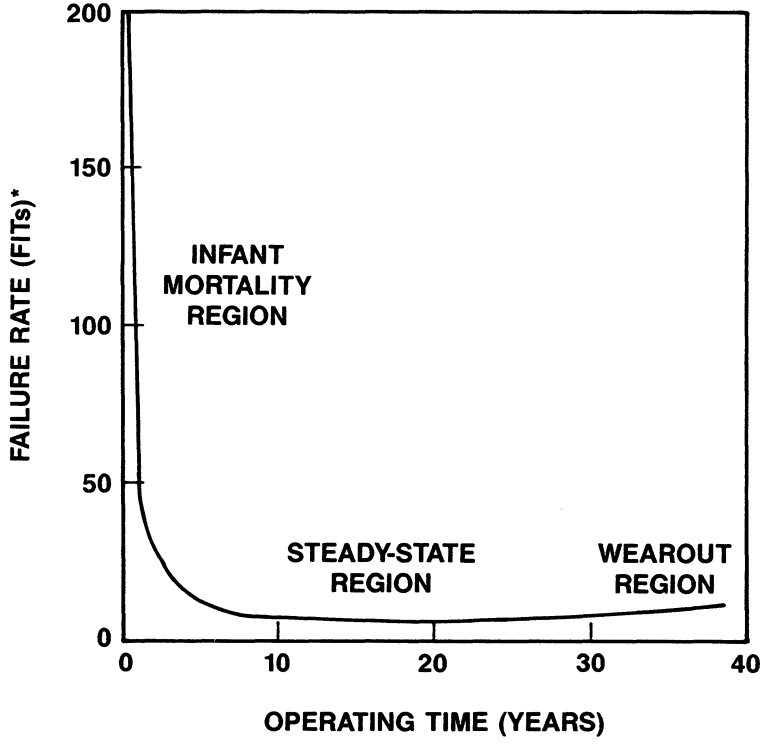
Analog IC Quality and Reliability

At AT&T, quality and reliability are not accidental by-products. Instead, they are established today as strategic business assets in our quest as the world leader in information movement and management. Our primary objective, of course, is to produce precision, error-free integrated circuits—circuits that meet or exceed at any given point in time the required device specifications (quality), and offer continual high performance over an extended service life (reliability).

Our approach to product excellence beings in the design and development stages with the latest quality assurance tools and accelerated life tests, and continues through manufacturing cycles with strict processing and screening methods. AT&T's popular **5ESS™** Switch is a prime example of a linear-supported product with quality designed in from start to finish. With little margin for error, members of our Quality Assurance Center tirelessly documented and reviewed each stage of switch development. Today, the **5ESS** Switch alone can accommodate a staggering 18-million telephone lines. Moreover, the estimated mean time to failure for the typical linear circuit used in the system is 30 years.

It is through these measures, along with time proven field experience, that we can accurately predict the behavior and endurance of any device or group of devices. Most IC populations in normal service can be expected to exhibit high initial failure rates which rapidly decrease in time. However, as devices mature, the failure rate attains a steady or constant state in terms of failures per unit of time and mortality is therefore attributed to normal device exhaustion. Simply stated, product longevity is based on design life intent.

As illustrated in Figure 1, wearout typically occurs very slowly over several decades and is not expected to be important in any reasonable time for ICs manufactured by AT&T.



* FITs = One failure in 10^9 device hours

Figure 1. Typical Failure Rate (Tj = 80°C)

Analog IC Quality and Reliability
(Continued)

- We commonly express reliability numerically in terms of a failure rate per unit of time, such as 0.001%. As we approach the very low failure rates, it is more suitable to define a failure unit (FIT) as one failure in 10^9 device-hours. For example, one failure among 10,000 devices operating for a year is a failure rate of 11 FITs, or 10 FITs = 0.001% per 1000 hours.

In making quantitative estimates of early life failure rates, it is more convenient to use the Weibull distribution model shown in Figure 2. Here, the curve is based on average results for removals from system equipment as well as infant mortality experiments. Since subsequent failure-mode analysis generally shows half the removed devices are in good condition, the curve has been labeled "removal rate," measured in RITs (one removal in 10^9 device hours). System failure rates can be estimated at any point in time by using half the plotted value for each IC and summing failure rates of the individual devices.

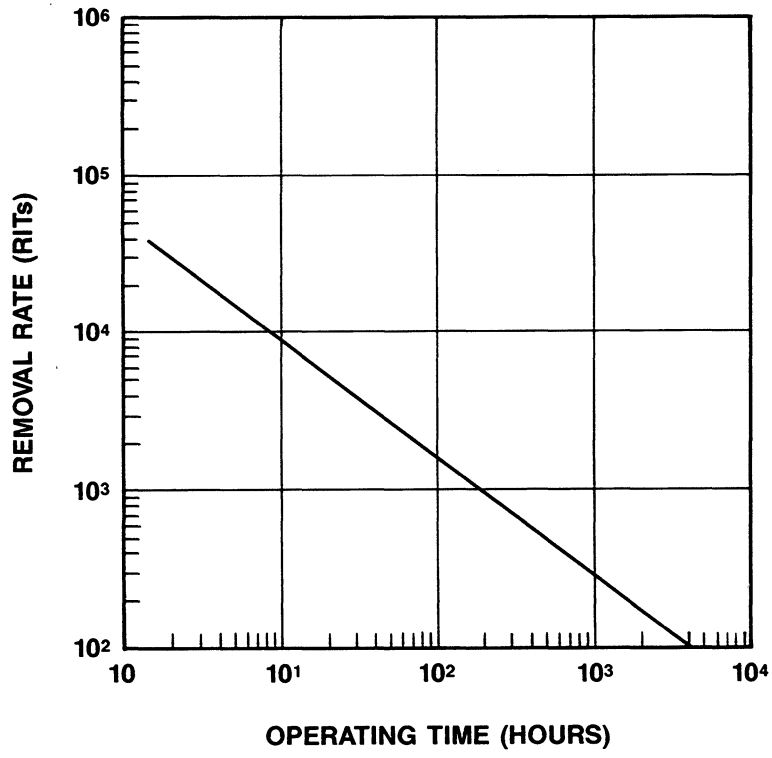


Figure 2. Analog Integrated Circuit Removal Rate (based on experimental data); (Tj = 50°C)

The high incidence of infant mortality, about 0.1%, is the result of defects arising during the manufacturing process. The objective is to reduce the proportion to less than 0.02% by design and manufacturing improvements, and/or 100% in-process screening. To assure a high level of reliability, IC production is continually sampled and tested using the following methods:

- Passivation-layer integrity
- Package terminal pull strength
- Package terminal bending-fatigue resistance
- Package terminal solderability
- Temperature-cycling resistance
- Humidity-temperature resistance

Analog IC Quality and Reliability
(Continued)

- 300°C storage life
- High-temperature operating life

Typical manufacturing faults leading to device removal are poor electrical connections, cracked silicon, and electrical-insulation defects. Some ICs fail because of mobile surface charge, metal migration, and other phenomena causing slow degradation. On the bottom line, the failure rate for a well-made product is projected to be very small (10 FITS maximum) over a typical 10- to 40-year equipment design life.

Nevertheless, in a customer environment, the best devices can be caused to fail if the equipment design allows severe stress levels. Conventional ICs have little voltage margin and exhibit little capacity to absorb energy pulses. On the other hand, failures due to lightning, static-electricity charges, voltage surges, and maintenance errors are almost impossible to predict because of their random nature. Breakdowns due to high humidity or temperature, or temperature cycling, are more predictable. Some of the common types of overstress and their effects on ICs are listed here.

- Lightning—If not properly arrested, lightning will short-circuit most ICs.
- Temperature or power cycling—ICs subjected to many temperature excursions, or to on-off power dissipation changes, may tend to fail because of differing coefficient of expansion among materials or mechanical design features.
- ESD—ICs are particularly vulnerable to electrostatic discharge (ESD), one of the most common causes of irreversible damage.
- Equipment maintenance—Many ICs are destroyed at the system or equipment level under circumstances that can only be traced to inadvertent application of the wrong voltages during testing and diagnostics.
- Electrical pulses and surges—Surges, spikes, and regulator-fault overvoltages can damage ICs or groups of devices. Systems should never exceed the maximum-rated voltage values of component ICs.
- Power sequencing—Semiconductors contain many parasitic junctions and devices which are not apparent in an examination of the circuit schematic. Unusual electrical biasing, in some combinations, may "turn-on" parasitic devices and can cause circuit damage.
- High humidity—ICs exposed to high relative humidity for long periods, while under electrical bias, tend to fail through electrolytic corrosion.
- High Temperature—Technology has practically eliminated surface, contact, and connection degradation as a negative reliability factor. Moreover, elevated operating temperatures actually reduce the probability of failure from electrolytic corrosion. The reliability of linear devices exposed to humid environments is therefore elevated by operating at higher temperatures, even up to the maximum operating limits.

The quality and reliability of AT&T's ICs over the total system life is excellent. Moreover, at AT&T quality is everyone's responsibility and, traditionally, it is the one dominant factor setting AT&T above and apart from the competitive mainstream. As a result, our customers can select with confidence from a wide assortment of the most innovative and persevering devices available in the electronic industry.

For a more detailed discussion, we suggest the "Reliability Information Notebook," published by the Bell Laboratories' Quality Assurance Center. Or, "The Statistical Quality Control Handbook," now in the sixth printing and in use by companies worldwide.

Description

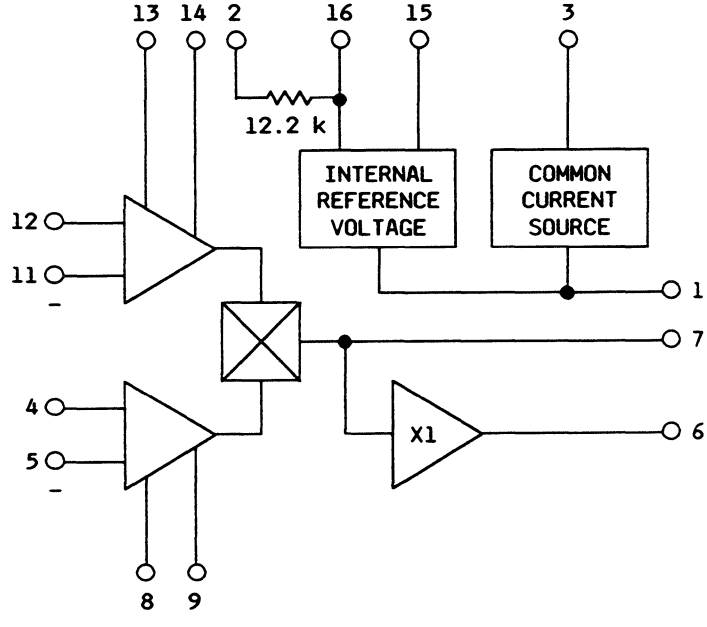
The LS1111AC Analog Multiplier is a full four-quadrant multiplier, meaning that two input voltages of any polarity can be processed. It features adjustable signal gain (within a range of 3700 to 7050), accepts a wide range of power-supply voltages, provides high- and low-impedance outputs, and has a guaranteed gain linearity error magnitude no greater than 9.0%. An on-chip regulator provides a performance trade-off capability between power-supply rejection ratio, temperature coefficient, and absolute multiplier gain accuracy with external resistors.

Applications of Analog Multipliers include: analog computing systems (multiply, divide, square root), frequency doublers, phase detectors, process control equipment, electronic gain controls, and analog modulators/demodulators.

Features

- Full four-quadrant analog signal multiplication
- Accepts wide range of power-supply voltage
- Adjustable signal gain
- 16-pin plastic DIP

Functional Block Diagram



Maximum Ratings (T_A = 25°C)	
Power-Supply Voltage	30 V
Total Power Dissipation	400 mW
Storage Temperature	−40 to +125°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions

Pin	Name/Function	Pin	Name/Function
1	V_S^+	9	Y Gain
2	R_{INT}	10	No Connection①
3	I_{SET}	11	−X Input
4	+Y Input	12	+X Input
5	−Y Input	13	X Gain
6	Low Z Output	14	X Gain
7	High Z Output	15	V_S^+
8	Y Gain	16	V_{INT}

① This lead is not internally connected and may be used as a tie point, provided the ratings of the device are not exceeded.

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic	Test Condition	Min	Typ	Max	Unit
Gain Factor		73		78	dB
Gain Linearity	External Resistor to V_S^+	—		±9.0	%
Input Offset Voltage	X or Y Inputs	—		±5.0	mV
Output Offset Voltage	Measured at Lead 6 with Lead 7 = GND	—		±15	mV
Output Voltage Swing	Lead 6	+13.0 −12.5		—	V
Common-Mode Voltage Range	X or Y Inputs	±12.5		—	V
Internal Reference Voltage	X or Y Inputs	V_S^- +4.6		V_S^- −6.2	V
Input Bias Current	X or Y Inputs	—		7.0	μA
Input Offset Current	X or Y Inputs	—		±1.0	μA
Maximum Output Current	Lead 7, I_{SET} = 250 μA	±350		±450	μA
Maximum Output Current	Lead 6, R_L = 1–0 kΩ	+500 −200		—	μA
Power-Supply Current		3.4		6.3	mA

Test Circuits

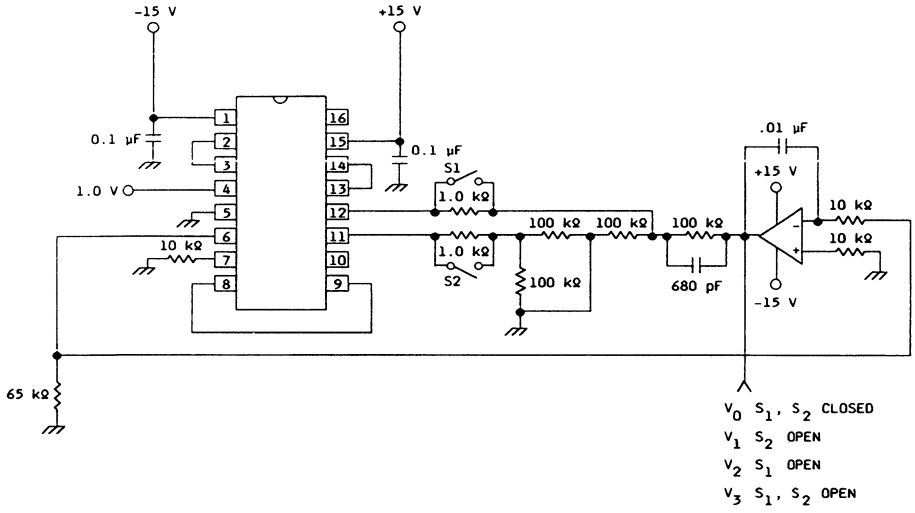
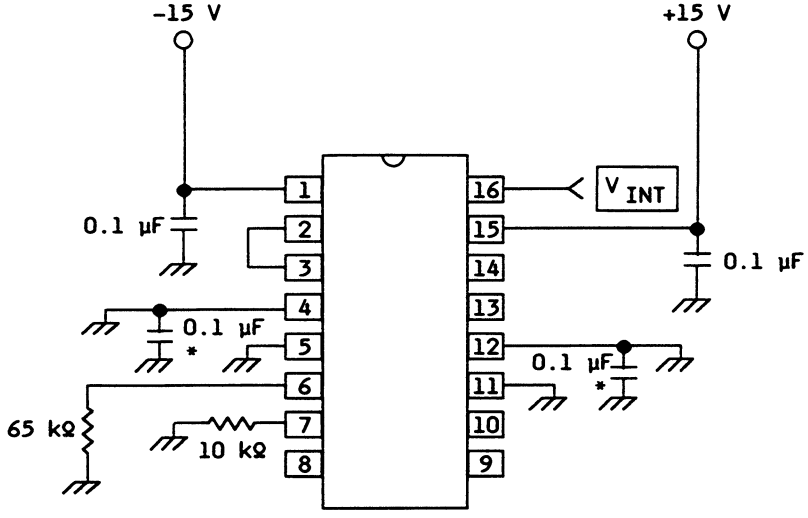


Figure 1. Input Offset Voltage (V_{IO}), Input Bias Current (I_{IB}), and Input Offset Current (I_{IO}) Test Circuit



* CAPACITOR ADDED FOR NOISE SUPPRESSION

Figure 2. Internal Reference Voltage (V_{INT}) Test Circuit

Test Circuits
(Continued)

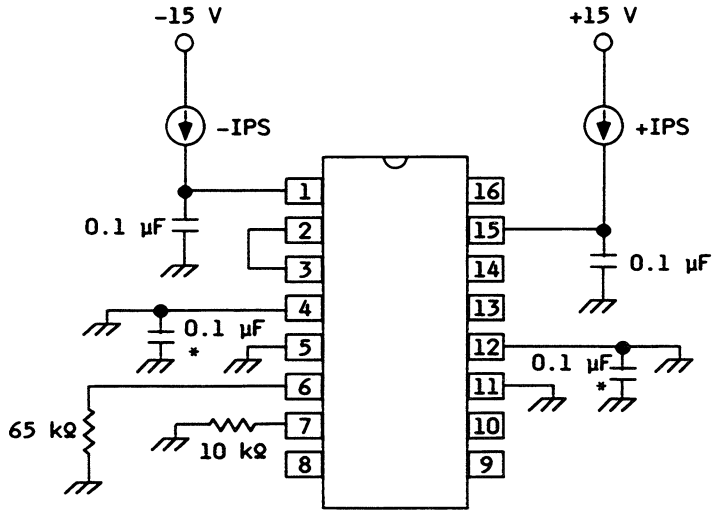


Figure 3. Power-Supply Currents (+ IPS, − IPS) Test Circuit

Application

Figures 1 through 6 show the required connections, external components, and representative performance for general applications. Figures 1, 2, and 3 are shown with ac coupling capacitors on the inputs. For dc-applications, these are omitted.

The external components are chosen according to the following equations and description.

As a four-quadrant analog multiplier, this device is suitable for a variety of applications such as squaring and modulating. External resistors determine the gain and dynamic range, as shown in the expression for the transfer characteristic.

$$V_O = G_F V_X V_Y \frac{R_O}{R_X R_Y} \text{ Volts}$$

where

$$G_F = \frac{1.2}{I_{SET}} \text{ (Ampere)}^{-1②}$$

R_X and R_Y provide individual adjustment of the transfer characteristic from the X and Y inputs, respectively, to allow the user to optimize linearity for large ratios V_X to V_Y. Figure 3 shows the four quadrant gain characteristic and Figure 4 shows a similar two-quadrant characteristic for ac signals. The level of the input voltages should be adjusted in accordance with Figure 5 to maintain linearity and avoid saturation of the inputs. R_O applied to the high-impedance output, fixes the overall gain by providing the current-to-voltage conversion before the signal is fed to a unity-gain buffer that supplies the low-impedance output. $V_{O(sat)}$ varies linearity with R_O. The high-impedance output is also a convenient node for frequency shaping the multipliers transfer characteristic. R_L is chosen to match the application requirements and a value of 65 kΩ is used for the test specification measurements.

Application
(Continued)

The multiplier has 3-dB bandwidth of approximately 2 MHz with $R_X = R_Y = 10\ k\Omega$ and $R_O = 1.0\ k\Omega$. The voltage follower between the high-impedance output and the low-impedance output has approximately 20 MHz of 3-dB bandwidth.

For maximum precision, an external reference current should be applied to lead 3 (I_{SET}). However, several simple means for obtaining I_{SET} may be used (at reduced precision), and these are outlined in the following paragraphs.

By shorting lead 2 (R_{INT}) to lead 3, the internal reference voltage is applied to the internal 12.2 kΩ resistor to generate I_{SET}. This option provides minimum component count and good power-supply rejection ($< 52\ \mu V/V$) of the multiplier gain. However, the gain factor ($G_F = 4400\ A^{-1}$) is subject to considerable variations because of manufacturing tolerances (±25%) and temperature (+0.33%/°C), neglecting the effects of the three gain-setting resistors.

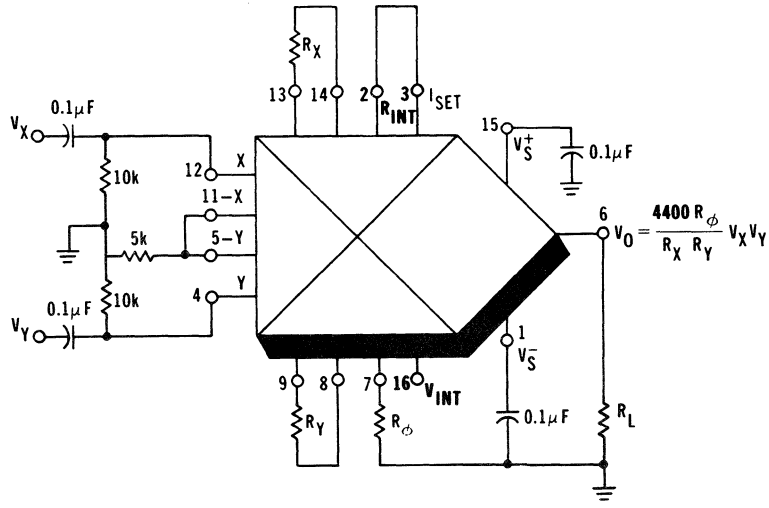


Figure 4. Internal Reference with Internal Resistor

② The theoretical numerator of G_F is 2.0, but experimentally the value 1.2 better describes this device.

Another option is to use the internal reference voltage and an external resistor to generate I_{SET} (see Figure 8). This resistor then determines the overall supply current as well as the gain and should be ≥ 10 kΩ. A resistor value close to 13 kΩ should provide the best operation. This option produces a gain factor

$$G_F = \frac{1.2\ R_{EXT} + 3.4\ k\Omega}{4.1}\ A^{-1}$$

which combines good power-supply rejection (0.03%/%) with improved tolerance (±12%), but without much improvement in temperature coefficient (+.25%/°C), again neglecting contributions of external components.

Application
(Continued)

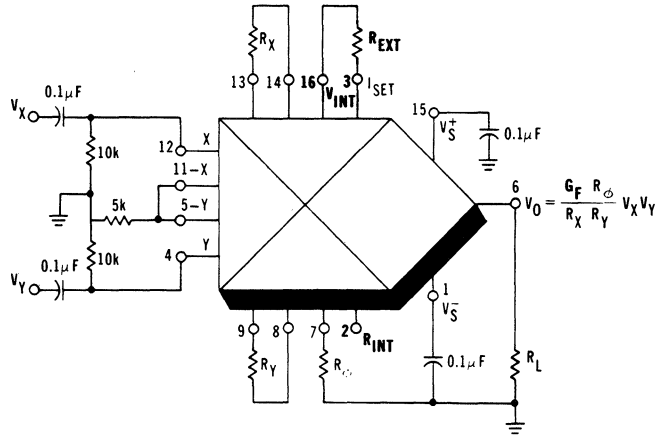


Figure 5. Internal Reference with External Resistor

A third option places an external resistor between V_S^+ and I_{SET}. This option sacrifices power-supply rejection (≈1%/%) to gain considerably in initial tolerance (±3%) and temperature coefficient (−0.012%/°C). Here, the gain factor is given by

$$G_F = \frac{1.2\ R_{EXT} + 3.4\ k\Omega}{V_S^+ - V_S^- - 1.3} \qquad A--$$

The value for R_{EXT} should be chosen so that I_{SET} is ≥ 300 μ A, where

$$I_{SET} = \frac{V_S^+ - V_S^- - 1.3}{R_{EXT} + 2.8\ k\Omega}$$

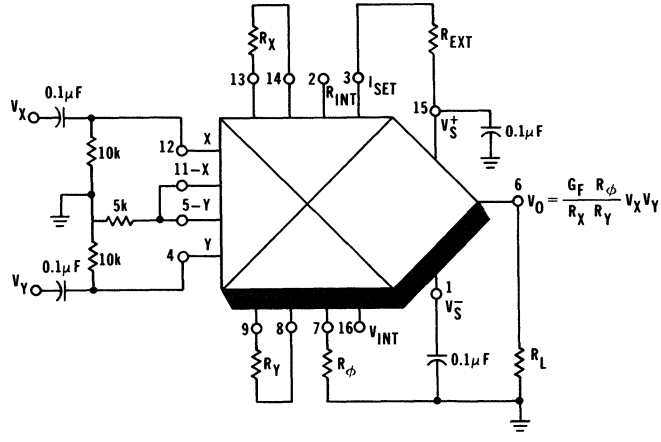
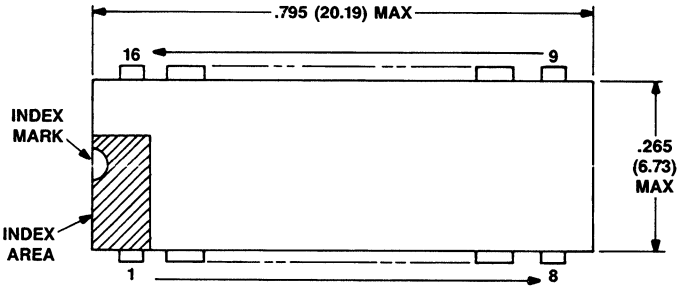
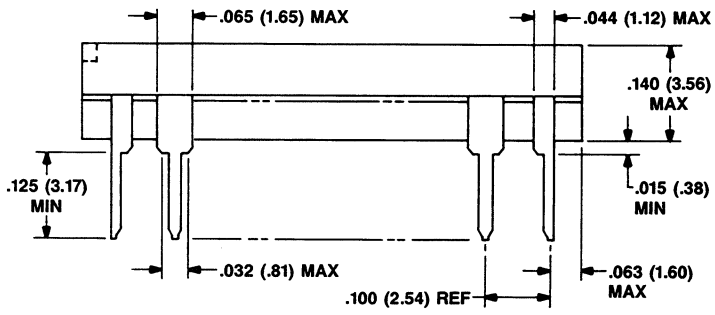


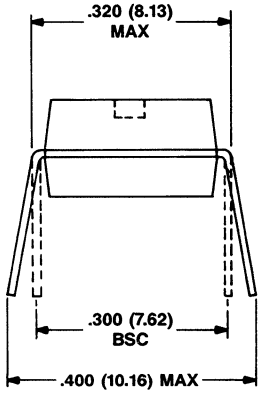
Figure 6. Internal Reference with External Resistor to the Positive Power-Supply

Outline Drawing

(Dimensions in Inches)







Ordering Information

Device	Comcode
LS1111AC	104411889

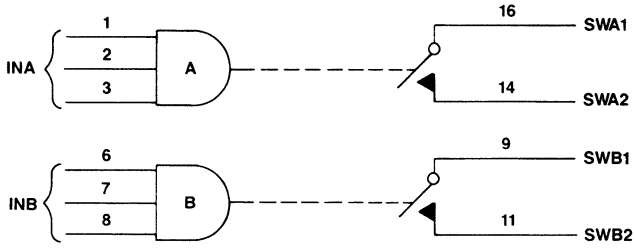
Description

The LB1017AC High-Speed Dual Analog Switch integrated circuit contains two channels in one package. Each channel consists of a driver circuit controller and SPST switch. The drivers interface with TTL-logic input signals for applications such as multiplexing, commutating, and D/A converter applications. These drivers enable a low-level input (0.8 to 2.0 volts) to control the ON/OFF condition of each switch. In the ON-State, each switch will conduct equally well in either direction. In the OFF-State, each switch will block voltages up to ±5 volts. Positive Logic 1 will turn each switch ON and Logic 0 will turn it OFF.

Features

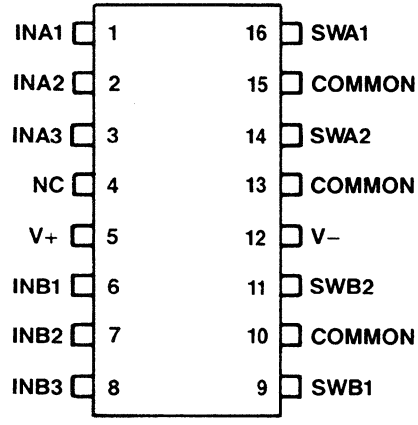
- Low ON resistance (9 to 15 ohms) for signals up to ±4 V and 100 kHz
- Characterized for audio range; capable of handling small-signal analog inputs to the MHz range
- Switching times < 50 ns
- ±4 volt common-mode range
- Low injected charge (< 50 pC)
- High open-switch isolation (–70 dB) at 1.0 kHz
- Low leakage current (< 100 nA) in the OFF-State
- Low crosstalk (–50 dB) between switches
- Low harmonic distortion
- Switches have sink/source current capabilities > 16 mA
- Low feedthrough capacitance (< 0.3 pF)

Functional Diagram



LOGIC	SWITCH
1 1 1	ON
0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0	OFF

Pin Diagram



Maximum Ratings

(T_A = 25°C unless otherwise specified)

Rating	Value	Unit
Ambient Operating Temperature Range	0 to 70	°C
Storage Temperature Range	−40 to +125	°C
Pin Temperature (Soldering, 15 sec)	300	°C
Supply Voltage, V+ to COMMON	+9.5	V
Supply Voltage, V− to COMMON	−9.5	V
Switch Voltages (SWA or SWB to COMMON)	±5.0	V
Input Voltages (INA or INB to COMMON)	±5.5	V

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions

Pin	Symbol	Name/Function
1 2 3 6 7 8	1NA1 1NA2 1NA3 1NB1 1NB2 1NB3	TTL-compatible logic input pins for switching channels A and B, respectively. A channel switch is normally closed if all of its inputs are logic HIGH. A logic LOW on any input pin will open the switch.
4	NC	No connection. This pin should not be used as a tie point for external circuitry.
5	V+	Connection for most positive external power supply.
9 16	SWB1 * SWA1 *	One side of the switch output (designated Side 1) for channels B and A, respectively.
10 13	COMMON	Ground or circuit common (not necessarily physical or system ground). All of these pins should be externally connected to one common point.
11 14	SWB2 * SWA2 *	One side of the switch output (designated Side 2) for channels B and A, respectively.
12	V−	Connection for most negative external power supply.

* Tables and figures relating to SWA1, SWA2, SWB1, and SWB2 describe only one set of switches. They have been designated V_{SW1}, V_{SW2}, for tables and SW1, SW2 for figures.

Characteristics

Switching Characteristics (Each Channel):
T_A = 25°C, V+ = 9 V, V− = −9 V, V_{IN} = Pins 1, 2, 3, 6, 7, and 8 (Functional Diagram)

Characteristics	Min	Typ	Max	Unit
Turn-On Time (Figures 1 and 3)				
V_{IN} (Pins 1, 2, 7, and 8) = 2.4 V				
V_{IN} (Pins 3 and 6) = Pulsed (Note 1)				
R_{LOAD} = 400 ohms				
V_{SET} = −5 V	20	—	50	ns
V_{SET} = +5 V	20	—	50	ns
Turn-On Time (Figures 2 and 3)				
V_{IN} (Pins 1, 2, 7, and 8) = 2.4 V				
V_{IN} (Pins 3 and 6) = Pulsed (Note 1)				
R_{LOAD} = 400 ohms				
V_{SET} = −5 V	10	—	40	ns
V_{SET} = +5 V	10	—	40	ns
Injected Charge (Note 2)				
V_{IN} = 2.4 V				
V_{SW1} = −4.5V	—	±5	±50	pC
V_{SW1} = 0	—	±5	±50	pC
V_{SW1} = +4.5 V	—	±5	±50	pC

Note 1. Positive pulses with 400 ns width and 2.5 volt amplitude are applied with a repetition rate of 60 μs. Rise and fall times of this applied pulse are ≤ 5 ns.

Note 2. Injected charge is defined as the amount of excess charge transferred to a 1000 pF load capacitor (connected to the SW2 side of each channel switch) during the time interval associated with the switch Turn-Off.

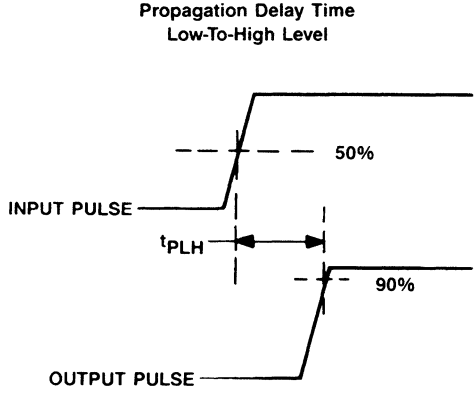


Figure 1. Turn-On Time

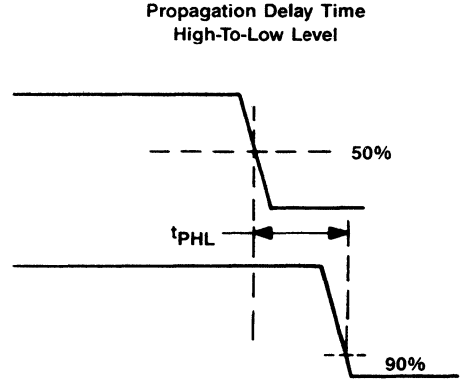


Figure 2. Turn-Off Time

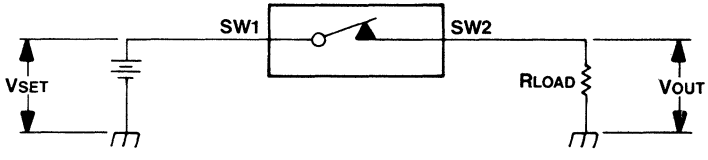


Figure 3. Test Method for Switching Time and Switch Offset Voltage

Electrical Characteristics (Each Channel):

T_A = 25°C, V+ = 9 V, V− = −9 V, V_{IN} = Pins 1, 2, 3, 6, 7 and 8 (Functional Diagram)

Characteristics	Min	Typ	Max	Unit
Switch ON Resistance V_{IN} = 2.4 V, Vsw1 and Vsw2 = 0, f = 1 kHz	9.0	—	15	Ω
Switch Leakage Current, ON Condition				
V_{IN} = 2.4 V, Vsw1 and Vsw2 = 0	—	—	±1.5	mA
V_{IN} = 2.4 V, Vsw1 and Vsw2 = −5 V	—	—	±1.5	mA
V_{IN} = 2.4 V, Vsw1 and Vsw2 = +5 V	—	—	±1.5	mA
Switch Source Current V_{IN} 2.4 V, Vsw1 = 1.5 V, Vsw2 = 0	−16	—	−30	mA
Switch Sink Current V_{IN} = 2.4 V, Vsw1 = −1.5 V, Vsw2 = 0	16	—	30	mA
Logic Input Current HIGH V_{IN} = 5.5 V	—	—	1.0	μA
Logic Input Current LOW V_{IN} = 0.4 V	−0.4	—	−1.2	mA
Switch Leakage Current, OFF Condition				
V_{IN} = 0.8 V, Vsw1 = +4.5 V, Vsw2 = −4.5 V	—	—	±100	nA
V_{IN} = 0.8 V, Vsw1 = −4.5 V, Vsw2 = +4.5 V	—	—	±100	nA
Positive Supply Current Switch in OFF Condition	—	7.7	13	mA
Negative Supply Current Switch in OFF Condition	—	−3.0	−10	mA
Power Supply Rejection Ratio, Positive and Negative	38	—	—	dB
Switch OFF Isolation V_{IN} = 0.4 V (Figure 4)	−70	—	—	dB
Crosstalk Between Switches V_{IN} = 2.4 V (Figure 5)	−50	—	—	dB
Second Harmonic Distortion (Note 3) V_{IN} = 2.4 V, V_{SOURCE} = 250 mVrms at 1 kHz (Figure 6)	—	—	250	μVrms
Third Harmonic Distortion (Note 4) V_{IN} = 2.4 V, V_{SOURCE} = 250 mVrms at 1 kHz (Figure 6)	—	—	140	μVrms
Switch Offset Voltage, No load (Note 5) V_{IN} (Pins 1, 2, 7, and 8) = 2.4 V V_{IN} (Pins 3 and 6) = Pulsed (Note 1)				
V_{SET} = −5 V	—	—	±25	mV
V_{SET} = 0	—	—	±25	mV
V_{SET} = +5 V	—	—	±25	mV
Switch Offset Voltage, 400 Ω load (Note 5) V_{IN} (Pins 1, 2, 7, and 8) = 2.4 V V_{IN} (Pins 3 and 6) = Pulsed (Note 1)				
V_{SET} = −5 V	—	±165	±300	mV
V_{SET} = +5 V	—	±165	±300	mV

Note 3. Second harmonic distortion is defined as the amplitude of a 2 kHz signal at V_{OUT} (V_{SOURCE} = 250 mVrms at 1 kHz).

Note 4. Third harmonic distortion is defined as the amplitude of a 3 kHz signal at V_{OUT} (S_{SOURCE} = 250 mVrms at 1 kHz).

Note 5. The Switch Offset Voltage is defined as the difference in voltage ($\triangle V = V_{SET} - V_{OUT}$) during the last 200 ns of the positive portion of the pulse described in Note 1. See Figure 3 for test method information.

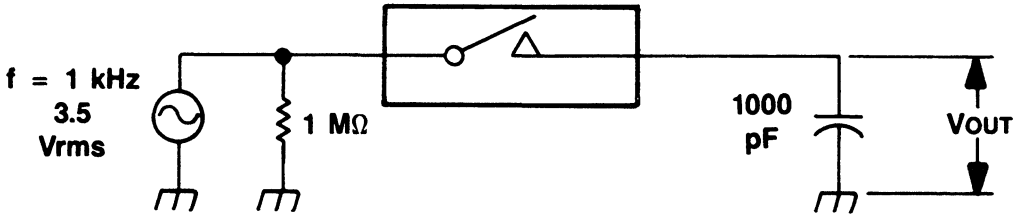


Figure 4. Switch Off Isolation Test Method

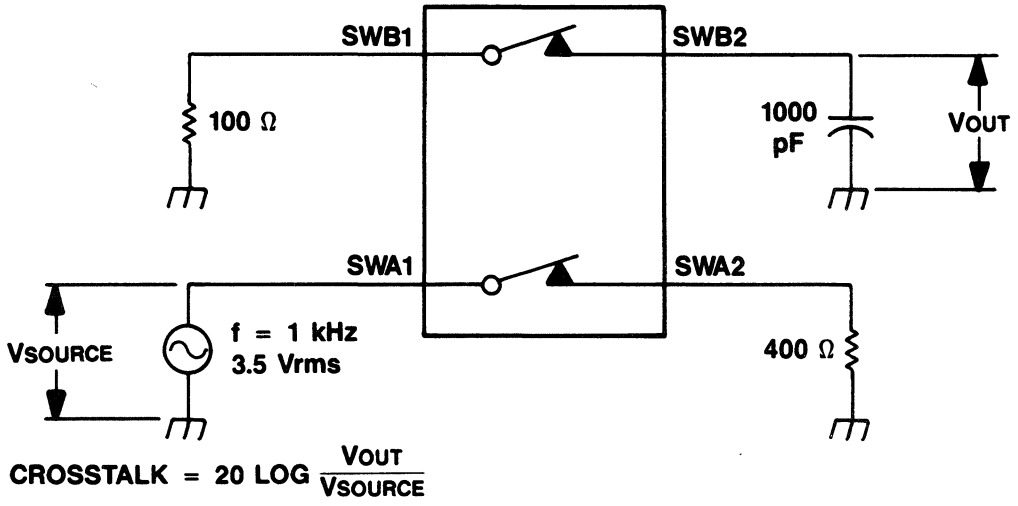


Figure 5. Crosstalk Test Method

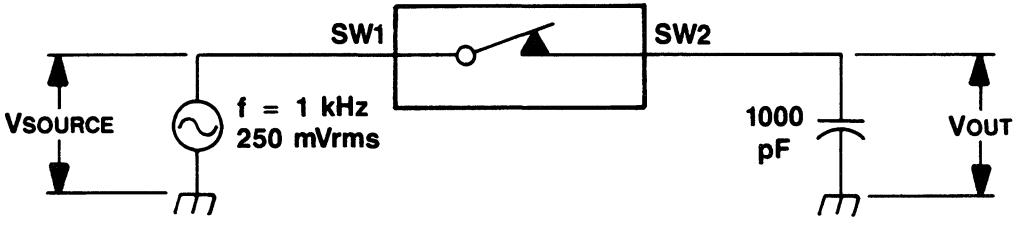


Figure 6. Harmonic Distortion Test Method

Characteristic Curves:

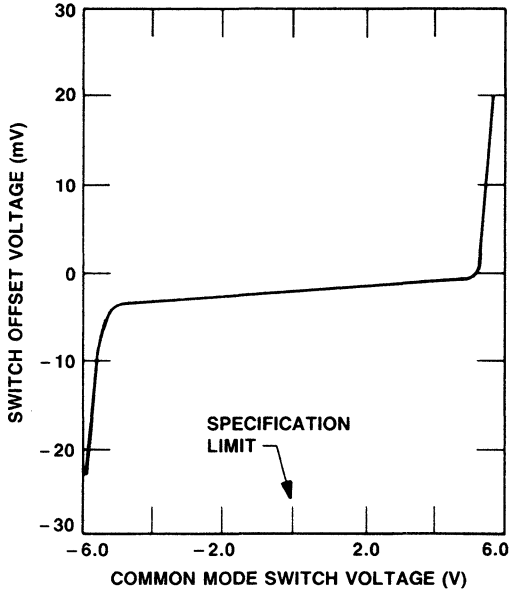


Figure 7. Typical Offset Voltage vs. Common-mode Voltage

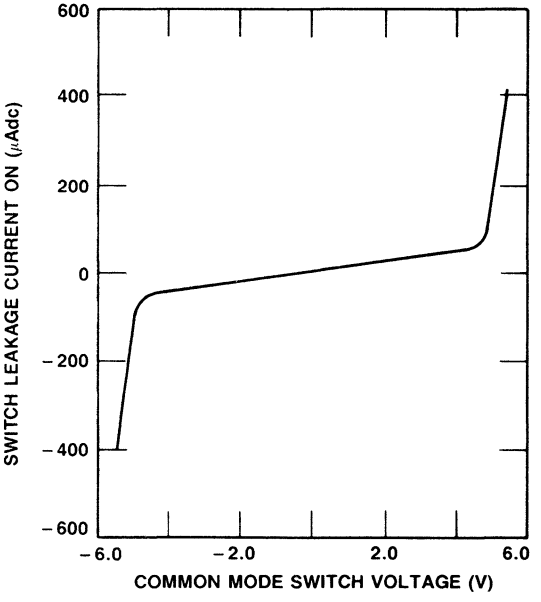


Figure 8. Typical Leakage Current vs. Common-mode Voltage

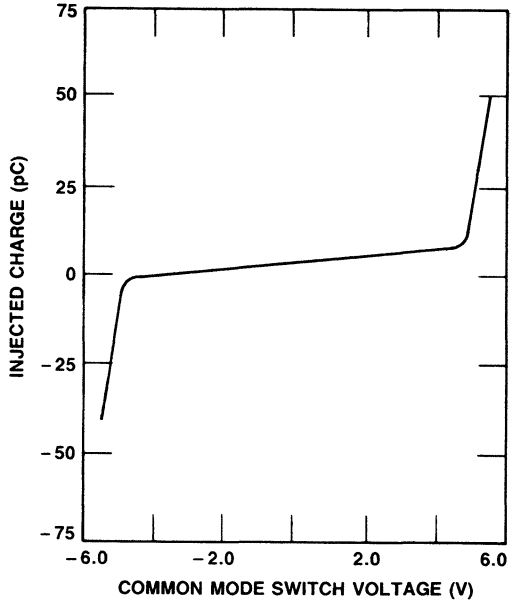


Figure 9. Typical Injected Charge vs. Common-mode Voltage

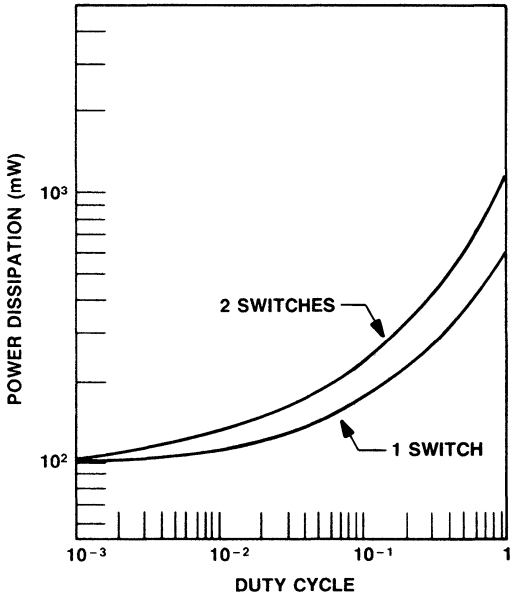


Figure 10. Typical Power Dissipation vs. Duty Cycle

Characteristic Curves

(Continued):

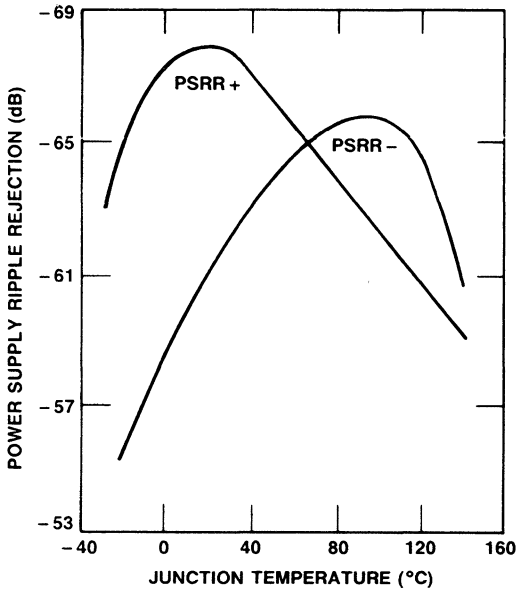


Figure 11. Typical Power Supply Ripple Rejection vs. Temperature

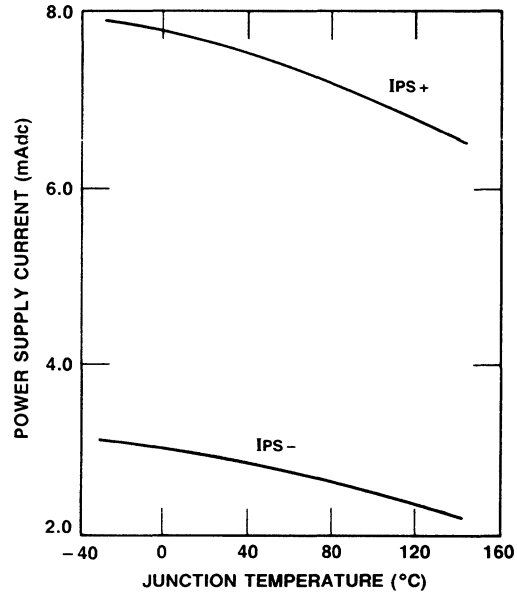


Figure 12. Typical Power Supply Current vs. Temperature

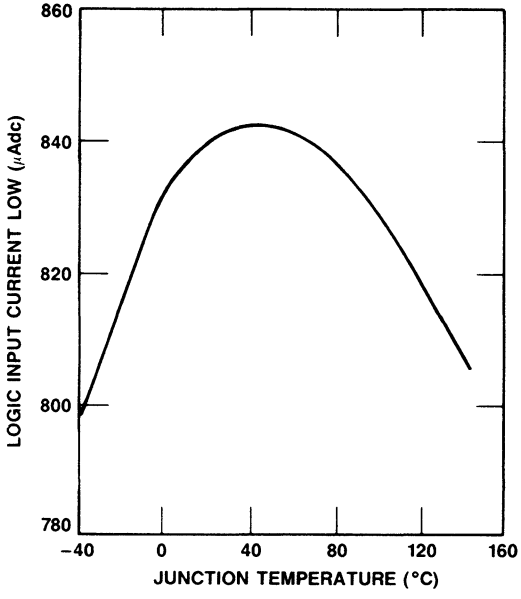


Figure 13. Typical Input Logic Current Low vs. Temperature

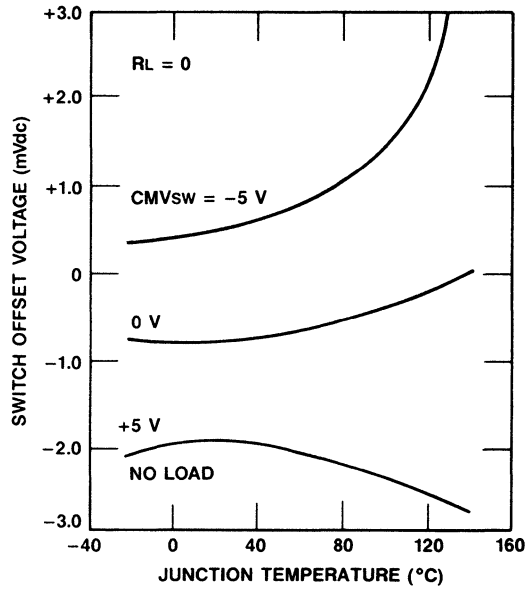


Figure 14. Typical Switch Offset Voltage vs. Temperature

Characteristic Curves
(Continued):

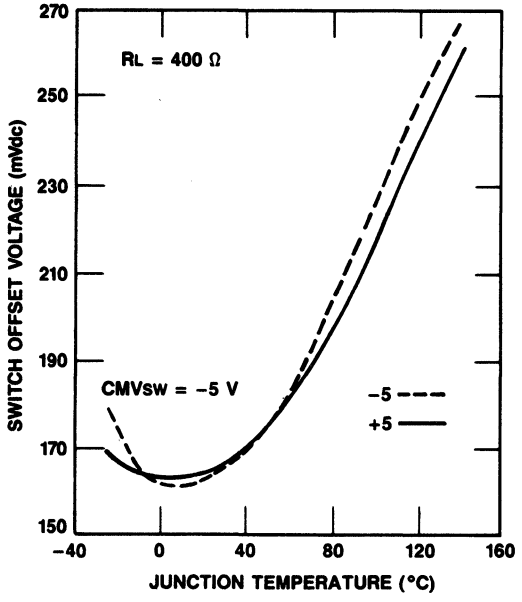


Figure 15. Typical Switch Offset Voltage vs. Temperature

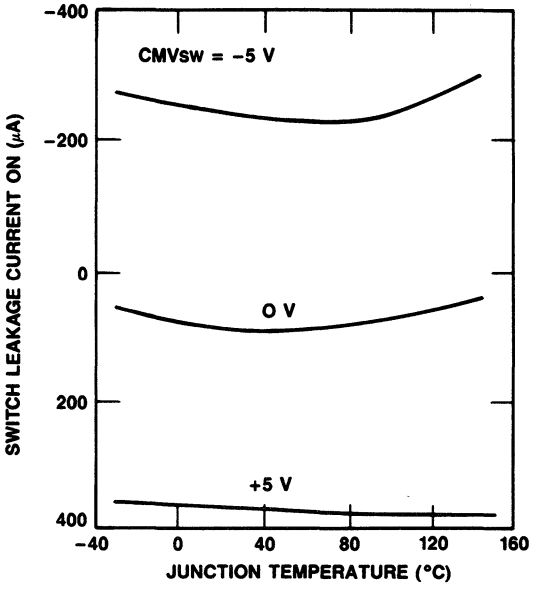


Figure 16. Typical ON Leakage Current vs. Temperature

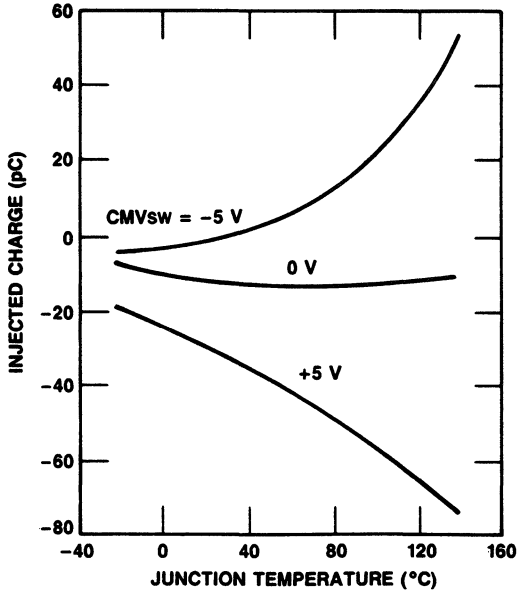


Figure 17. Typical Injected Charge vs. Temperature

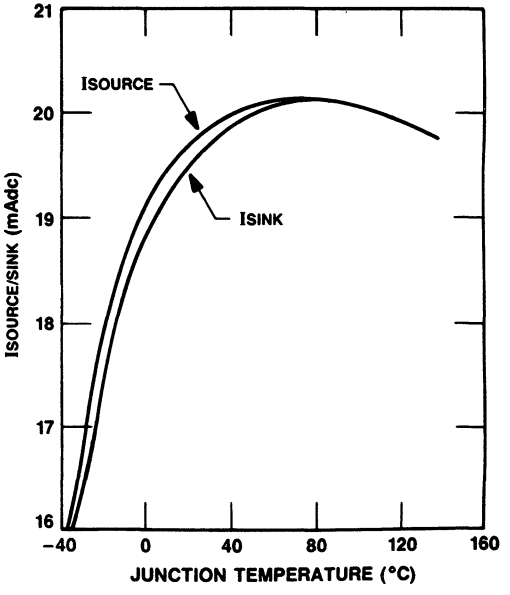


Figure 18. Typical Source and Sink Current vs. Temperature

Characteristic Curves

(Continued):

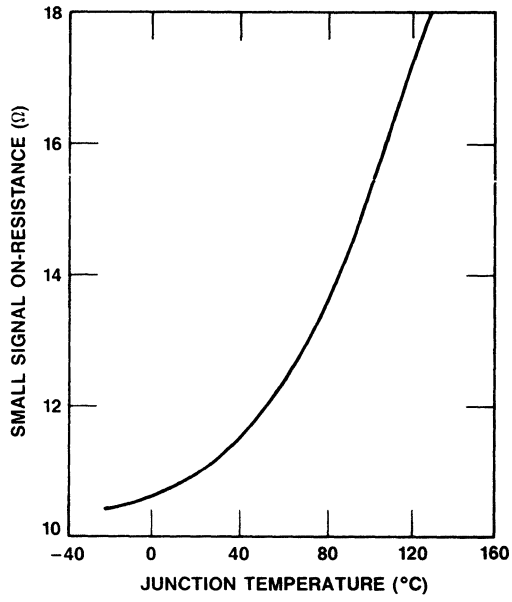


Figure 19. Typical ON Resistance vs. Temperature

Applications

The LB1017AC is a High-Speed Dual Analog Switch with low ON resistances and control inputs which are TTL-compatible.

Figure 20 shows a diagram of the LB1017AC as used in a sampling application. The design of this device incorporates high-speed current amplifiers. It is important that proper high-frequency bypassing of power supplies is used, and that proper grounding designs are incorporated.

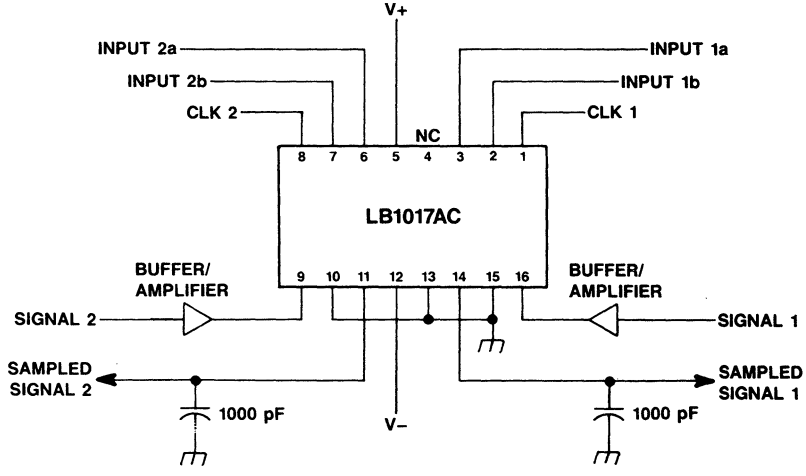
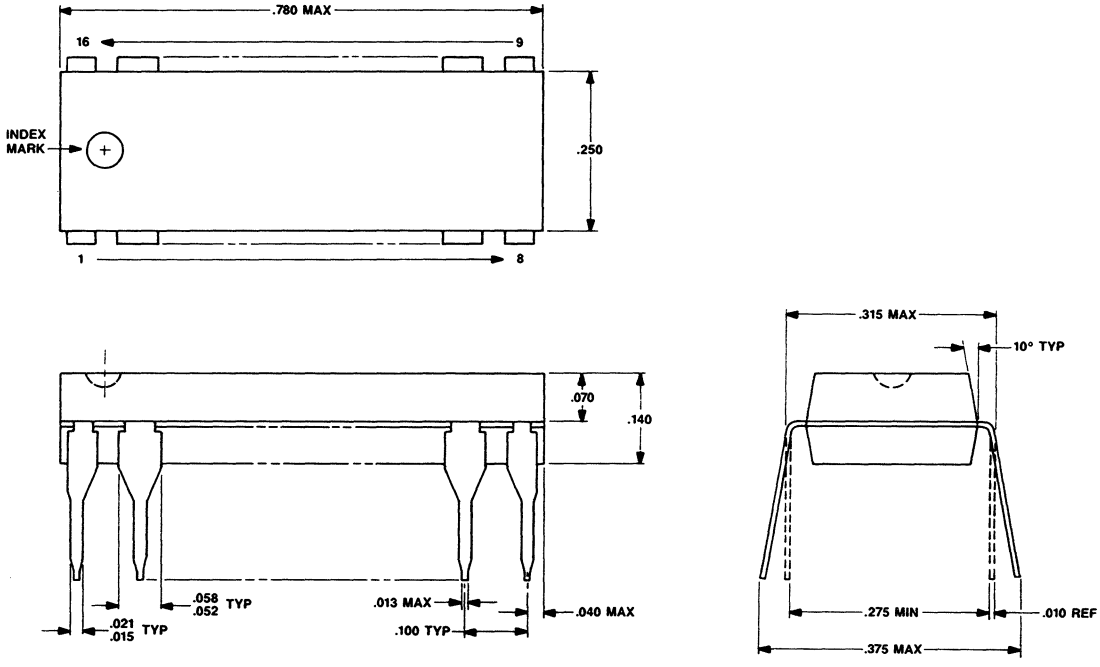


Figure 20. LB1017AC High-Speed Dual Analog Switch Sampling Application

Outline Drawing

(Dimensions in Inches)



Ordering Information:

Device	Comcode
LB1017AC	104208863

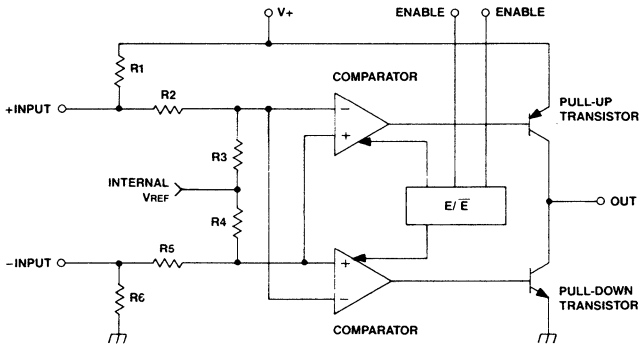
Description

The AM26LS32CC and AM26LS33CC Quad Line Receivers are general-purpose quad line receivers for balanced and unbalanced data transmission. A TTL-compatible ENABLE, $\overline{\text{ENABLE}}$ is common to all four receivers in the device package. The ENABLE, $\overline{\text{ENABLE}}$ allows the output to assume a high-impedance state for output busing.

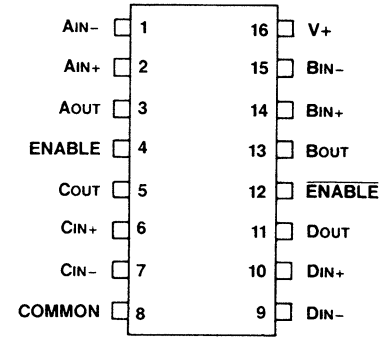
Features

- Requires only a single 5 V (±10%) power supply
- Input sensitivity:
  AM26LS32CC ±200 mV
  AM26LS33CC ±500 mV
- Minimum input hysteresis:
  AM26LS32CC ±15 mV
  AM26LS33CC ± 30 mV
- Internal fail safe forces the output high for an open input condition
- Direct replacement for industry-standard differential Line Receivers
- Meets EIA RS-422A/423A specifications
- Four independent receivers with common strobe TTL-compatible input
- Electrostatic discharge protection on receiver inputs
- Typical propagation delay of 17 ns

Functional Diagram



Pin Diagram



Notes: R1 and R6 are fail-safe resistors.
R2, R3, R4, R5 form an Input Divider.
With the internal reference (V_{REF}), these components set the input characteristics.
One of four identical circuits shown.

Maximum Ratings

Rating	Value	Unit
Supply Voltage (V+)	7.0	V
Control Input Voltage (ENABLE, $\overline{\text{ENABLE}}$)	7.0	V
Input Common Mode Range	±25	V
Input Differential Voltage	±25	V
Operating Temperature	0 to 85	°C
Storage Temperature Range	−40 to +125	°C
Power Dissipation (Package Limitation)	400	mW
Pin Temperature (Soldering, 15 sec)	300	°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions

Pin	Symbol	Name/Function
1	AIN−	Negative Input, Receiver A
2	AIN+	Positive Input, Receiver A
3	AOUT	Output, Receiver A
4	ENABLE	Enable Input
5	COUT	Output, Receiver C
6	CIN+	Positive Input, Receiver C
7	CIN−	Negative Input, Receiver C
8	COMMON	Circuit Common, not necessarily physical or system ground
9	DIN−	Negative Input, Receiver D
10	DIN+	Positive Input, Receiver D
11	DOUT	Output, Receiver D
12	$\overline{\text{ENABLE}}$	$\overline{\text{Enable}}$ Input
13	BOUT	Output, Receiver B
14	BIN+	Positive Input, Receiver B
15	BIN−	Negative Input, Receiver B
16	V+	Supply Voltage, External

Electrical Characteristics

$0 \leq T_A \leq 85°C$, $4.5\ V \leq V+ \leq 5.5\ V$, unless otherwise specified

Characteristic	Conditions	Min	Max	Unit
Differential Input Threshold Voltage (Figure 2)	$I_O = -0.4$ mA, $V_{OH} \geq 2.7$ V AM26LS32CC, $-7.0\ V < V_{CM} < 7.0\ V$	—	0.2	V
	AM26LS33CC, $-15.0\ V < V_{CM} < 15.0\ V$	—	0.5	
	$I_O = 4.0$ mA, $V_{OL} \leq 0.5$ V AM26LS32CC, $-7.0\ V < V_{CM} < 7.0\ V$	—	−0.2	
	AM26LS33CC, $-15.0\ V < V_{CM} < 15.0\ V$	—	−0.5	
Dynamic Input Resistance (Figure 3)	$-15.0\ V < V_{CM} < 15.0\ V$ One input ac ground	6.0	—	kΩ
Input Current (Figure 4)	$V_{IN} = 15.0$ V	—	2.3	mA
	$V_{IN} = -15.0$ V	—	−2.8	
Input Hysteresis Voltage (Figure 2)	$V+ = 5.0$ V, $T_A = 25°C$ AM26LS32CC, $V_{CM} = \pm 7.0$ V	±15	—	mV
	AM26LS33CC, $V_{CM} = \pm 15.0$ V	±30	—	
High-Level Output Voltage (Figure 5)	$V+ = 4.5$ V, $V_{ID} = 1.0$ V, $V_{\overline{EN}} = 0.8$ V, $I_{OH} = -440\ \mu A$	3.6	—	V
Low-Level Output Voltage (Figure 5)	$V+ = 4.5$ V, $V_{ID} = 0.8$ V, $V_{\overline{EN}} = 0.8$ V $I_{OL} = 5.0$ mA	—	0.4	
	$I_{OL} = 10.0$ mA	—	0.45	
Output Short-Circuit Current (Figure 6)	$V+ = 5.5$ V EN = $\overline{EN} = 0.8$ V	−15	−80	mA
Off-State Output Current (High Z) (Figure 7)	$V+ = 5.5$ V, $V_O = 2.4$ V	—	20	μA
	$V+ = 5.5$ V, $V_O = 0.4$ V	—	−20	
Power Supply Current (Figure 8)	$V+ = 5.5$ V All Inputs Grounded, Output Disabled	—	70	mA
Input Low-State Voltage*†		—	0.8	V
Input High-State Voltage*†		1.8	—	
Low-State Current*	V_{IN} 0 V, $V+ = 5.5$ V	—	−0.36	mA
High-State Current*	$V_{IN} = 2.7$ V, $V+ = 5.5$ V	—	20	μA
High-Voltage Current*	$V_{IN} = 5.5$ V, $V+ = 5.5$ V	—	100	μA
Input Clamp Voltage*	$V+ = 4.5$ V, $I_{IN} = -18$ mA	—	1.5	V

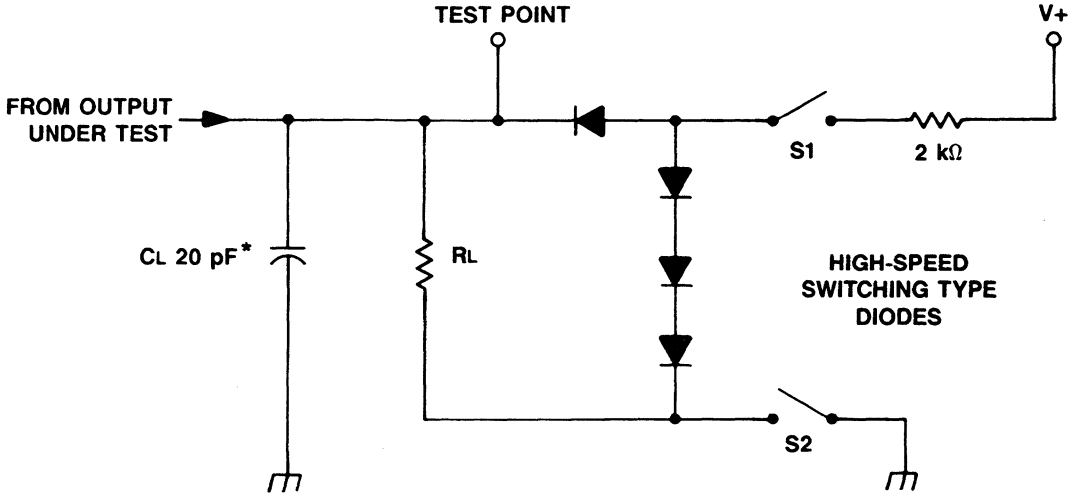
* These specifications refer only to the ENABLE and $\overline{\text{ENABLE}}$ inputs (pins 4 and 12 respectively).
† Indirectly guaranteed; not set up as an individual test.

Timing Characteristics

T_A = 25°C, V+ = 5.0 V, C_L = 20 pF

Characteristic	Conditions		Min	Max	Unit
Propagation Delay Time*	R_L = 5.0 kΩ (Figure 9)	t_{PLH}	—	25	ns
		t_{PHL}	—	25	
	R_L = 1.67 kΩ (Figure 10)	t_{PLZ}	—	30	
		t_{PHZ}	—	27	
	R_L = 5.0 kΩ (Figure 10)	t_{PZL}	—	22	
		t_{PZH}	—	24	

* See Figure 1 for Load Test Circuit, and Figures 11 and 12 for the Timing Diagrams.



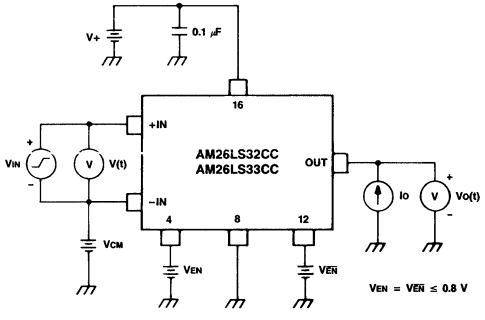
* INCLUDING PROBE & JIG CAPACITANCE

Figure 1. Load Test Circuits for 3-State Outputs

Recommended Operating Conditions

Rating	Value	Unit
Supply Voltage (V+)	4.5 to 5.5	V
Operating Ambient Temperature Range	0 to 85	°C
Input Common Mode Range		
AM26LS32CC	±7.0	V
AM26LS33CC	±15.0	V

Test Circuits



VIN = At+b; b < VCM for VTH
VIN = −At+b; b > VCM for VTH
VThreshold = V(t=t1)
T1 = time @ output transition
Input Hysteresis Voltage = VTLH − VTHL

Figure 2. Differential Input Threshold Voltage

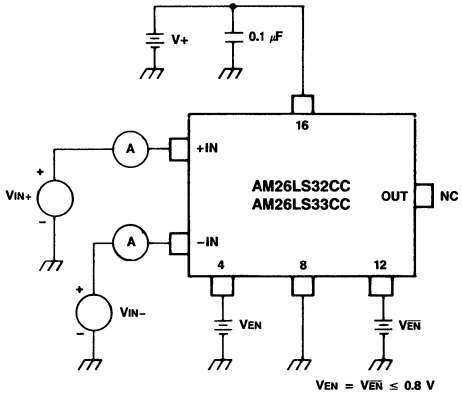


Figure 4. Input Current

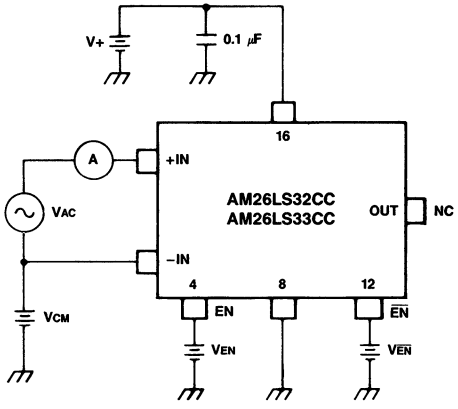


Figure 3. Dynamic Input Resistance

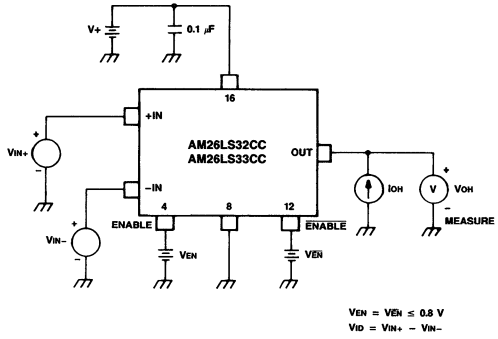


Figure 5. High-Level Output Voltage & Low-Level Output Voltage

TEST CIRCUITS (Continued)

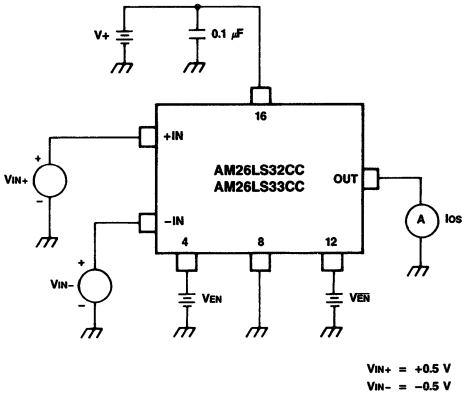


Figure 6. Output Current, Short Circuit

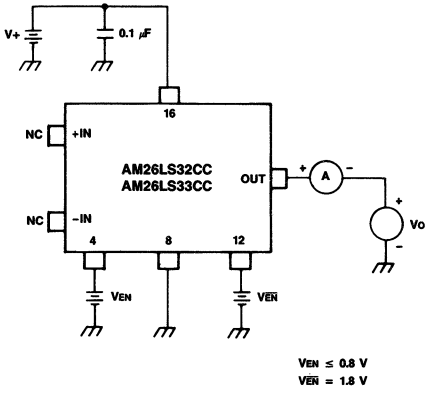


Figure 7. Off-State Output Current (High Z)

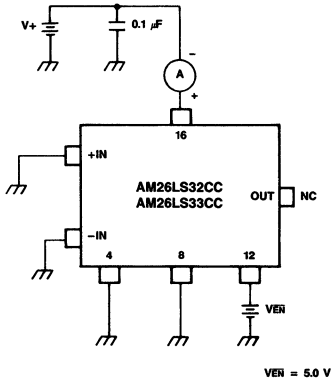


Figure 8. Power Supply Current

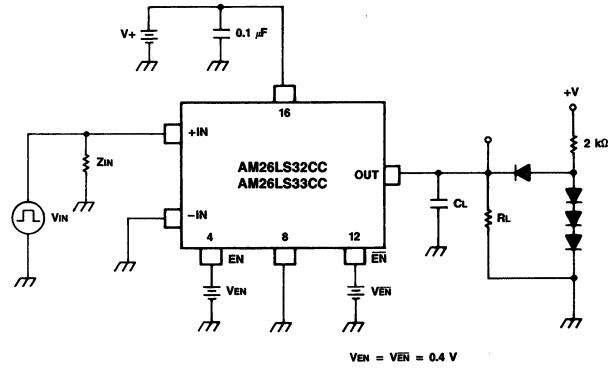


Figure 9. Propagation Delay Times (t_{PLH}, t_{PHL})

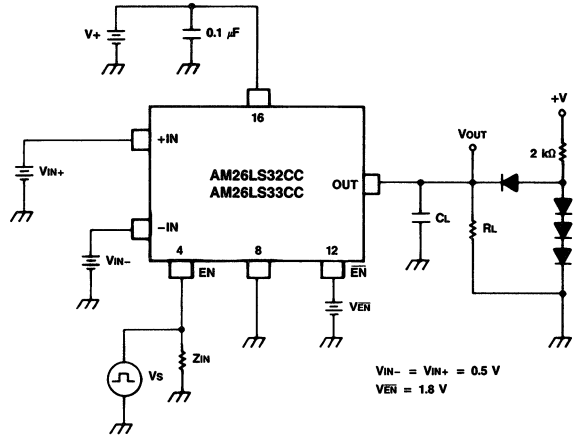


Figure 10. Propagation Delay Times (t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH})

Timing Diagrams

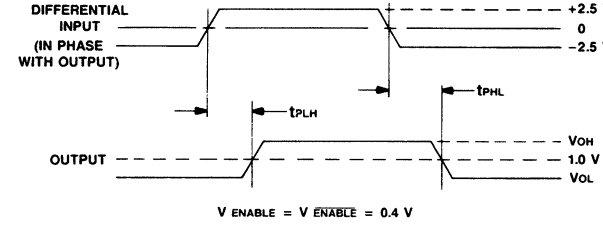
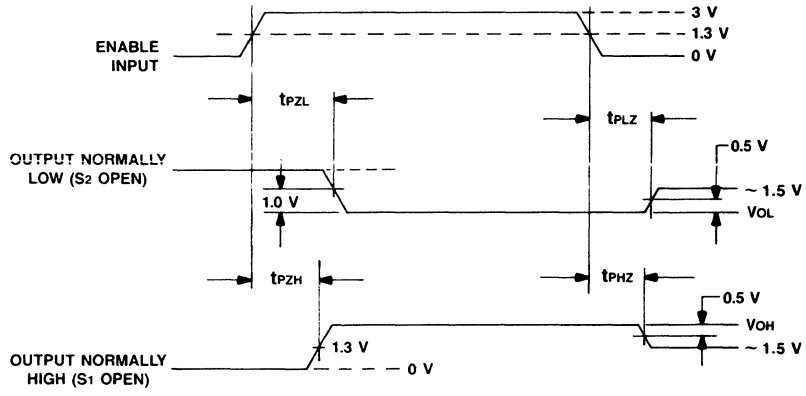


Figure 11. Signal Propagation Delay Time

Timing Diagrams (Continued)



Notes: S_1 and S_2 of Load Circuit are Closed Except as Noted Above, and V $\overline{\text{ENABLE}}$ = 1.8 V
Pulse Generator: Rate ≤ 1.0 MHz, Z_O = 50 Ω, tr ≤ 15 ns, tf ≤ 6 ns

Figure 12. ENABLE, $\overline{\text{ENABLE}}$ Delay Times

Applications

The following Truth Table shows the ENABLE and $\overline{\text{ENABLE}}$ conditions which must be met to provide specific receiver output states.

ENABLE	$\overline{\text{ENABLE}}$	Output
0	0	Enabled
1	0	Enabled
0	1	Disabled
1	1	Enabled

0 = Low State (V_{IN} ≤ 0.8 V)
1 = High State (V_{IN} ≥ 2.0 V)

The following diagram illustrates basic information for application of the AM26LS32CC and AM26LS33CC Quad Line Receiver devices in a two-wire balanced RS-422A system. This particular diagram shows the AM26LS32CC, AM26LS33CC Quad Line Receivers interfacing with the AM26LS31CC Quad Line Driver.

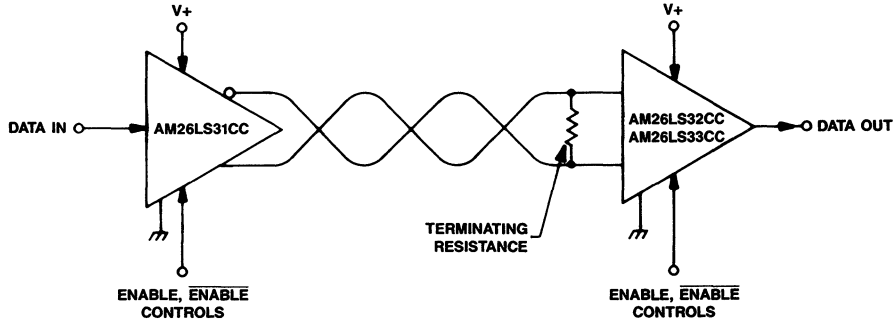
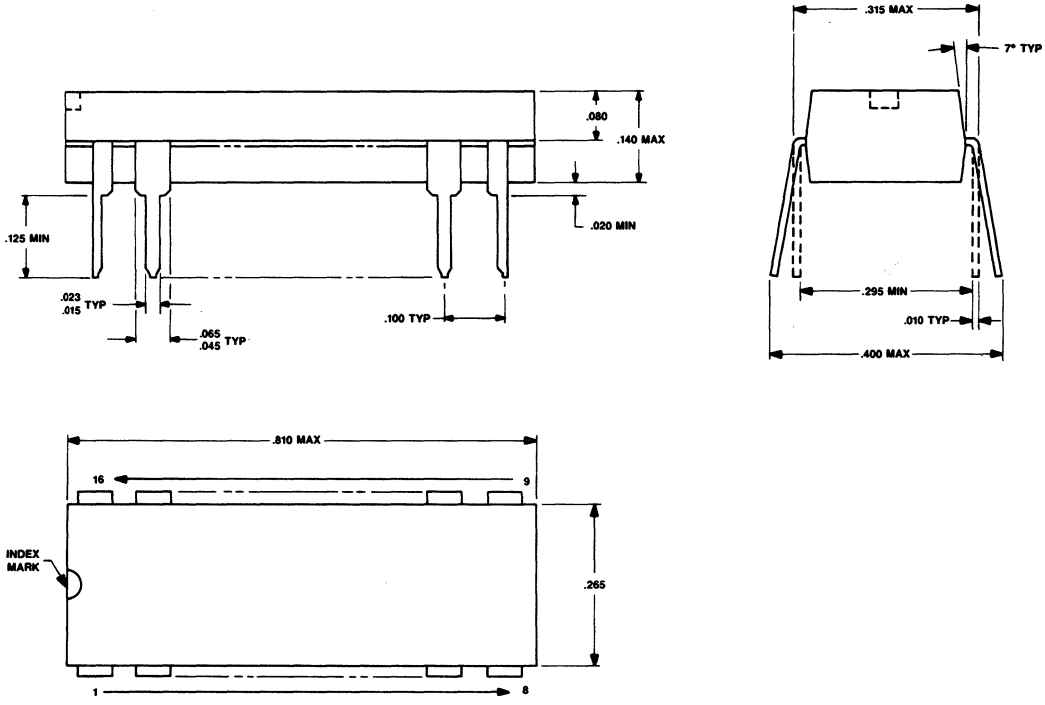


Figure 13. AM26LS32CC, AM26LS33CC Quad Line Receiver Application Diagram

Outline Drawing

(Dimensions in Inches)



Note: Pin numbers are shown for reference only

Ordering Information

Device	Comcode
AM26LS32CC	104438056
AM26LS33CC	104438064

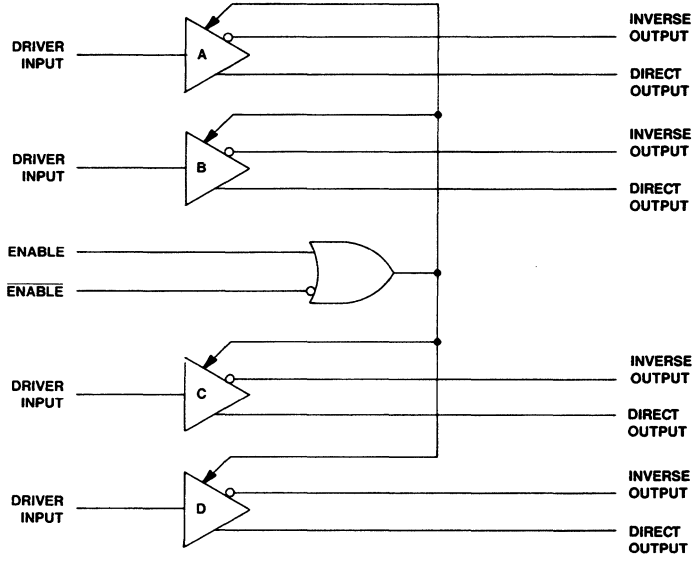
Description

The AM26LS31CC Quad Line Driver is an integrated circuit consisting of four independent line drivers with a common control for both ENABLE, $\overline{\text{ENABLE}}$. It provides high-speed differential drive to transmission lines having an impedance of at least 100 ohms. Each of the four drivers has a complementary tri-state output. The device requires only a 5 volt supply ($\pm$10%) for operation.

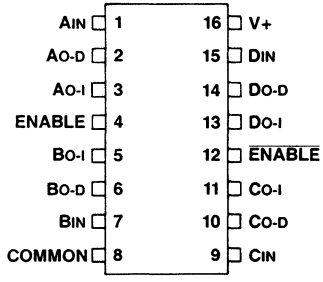
Features

- Propagation delay is less than 20 ns
- Power supply current is reduced to less than 40 mA when device is disabled
- ENABLE, $\overline{\text{ENABLE}}$ to output delay is less than 40 ns
- Direct replacement for industry standard differential Line Drivers
- Meets EIA RS-422A requirements
- TTL-compatible ENABLE, $\overline{\text{ENABLE}}$ inputs
- Output skew (time delay between direct output and inverse output) is typically 2 ns

Functional Diagram



Pin Diagram



Maximum Ratings

Rating	Value	Unit
Power Supply Voltage (V+)	7.0	V
Input Operating Voltages, V+, Driver Inputs, ENABLE, $\overline{\text{ENABLE}}$	5.5	V
Ambient Operating Temperature Range	0 to 70	°C
Storage Temperature Range	−40 to +125	°C
Driver Output Current	±35	mA
Pin Temperature (Soldering, 15 sec)	300	°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions

Pin	Symbol	Name/Function
1	AIN	TTL-Compatible Input, Line Driver A
2	AO-D	Noninverting Line Driver Output, Driver A
3	AO-I	Inverting Line Driver Output, Driver A
4	ENABLE	Logic HIGH Enable, TTL-Compatible Input (see Truth Table for logic programming of this pin)
5	BO-I	Inverting Line Driver Output, Driver B
6	BO-D	Noninverting Line Driver Output, Driver B
7	BIN	TTL-Compatible Input, Line Driver B
8	COMMON	Circuit Common (not necessarily physical or system ground)
9	CIN	TTL-Compatible Input, Line Driver C
10	CO-D	Noninverting Line Driver Output, Driver C
11	CO-I	Inverting Line Driver Output, Driver C
12	$\overline{\text{ENABLE}}$	Logic LOW Enable, TTL-Compatible Input (see Truth Table for logic programming of this pin)
13	DO-I	Inverting Line Driver Output, Driver D
14	DO-D	Noninverting Line Driver Output, Driver D
15	DIN	TTL-Compatible Input, Line Driver D
16	V+	Connection for External Power Supply

Electrical Characteristics

T_A = 25°C, unless otherwise specified

Characteristic	Conditions		Min	Max	Unit
Power Supply Voltage, Operating (Figure 1)			4.5	5.5	V
Output Voltage (Figure 1)	$V+$ = 4.5 V, I_O = 20 mA, V_{IH} = 2.0 V, V_{IL} = 0.8 V	High	2.5	3.5	V
		Low	0.05	0.5	V
Input Clamp Voltage (Figure 2)	$V+$ = 4.5 V, I_{IN} = −18 mA		0	−1.5	V
Power Supply Current, No Load (Figure 3)	$V+$ = 5.5 V, V_{IN} = 0		45	90	mA
Power Supply Current, Disabled (Figure 3)	$V+$ = 5.5 V, V_{IN} = 2.0 V		20	40	mA
Output Current, Disabled (Figure 4)	V_O = 0.5 V or 2.5 V		—	±20	μA
Output Current, Power Off (Figure 5)	V_O = −0.25 or +6.0 V		—	±100	μA
Output Current, Short Circuit (Figure 6)	$V+$ = 5.5 V		—	−150	mA
Input Current, Low (Figure 7)	V_{IN} = 0.4 V		0	−0.36	mA
Input Current, High (Figure 7)	V_{IN} = 2.7 V		—	±20	μA
Input Current, Reverse (Figure 7)	V_{IN} = 7.0 V		0	0.1	mA

Timing Characteristics

Paramter	Min	Max	Unit
Transition Time; t_{THL}, t_{TLH} (Figure 10)	—	20	ns
Propogation Delay Time; t_{PHL}, t_{PLH} (Figure 9)	—	20	ns
V_{O-D} to V_{O-I} Time Difference, t_{skew} (Figure 9)	—	±6.0	ns
Overshoot, $\frac{Vpeak - V+}{V+}$ (Figure 10)	—	10	%
Output Enable Times*			
High Impedance to Output High; t_{ZH}—30ns High Impedance to Output Low; t_{ZL}	—	30	ns
Output $\overline{\text{Enable}}$ Times* Output High to High Impedance; t_{HZ} Output Low to High Impedance; t_{LZ}	— —	40 40	ns ns

* The device is disabled when ENABLE = LOW and $\overline{\text{ENABLE}}$ = HIGH. All other conditions of ENABLE and $\overline{\text{ENABLE}}$ will allow the device to operate (see Truth Table in Applications section, page 9-14).

Test Circuits

Pin Allocation for Test Circuits (See Figures 1 through 8)

Driver	IN	OUT	$\overline{OUT}$
A	Pin 1	Pin 2	Pin 3
B	Pin 7	Pin 6	Pin 5
C	Pin 9	Pin 10	Pin 11
D	Pin 15	Pin 14	Pin 13

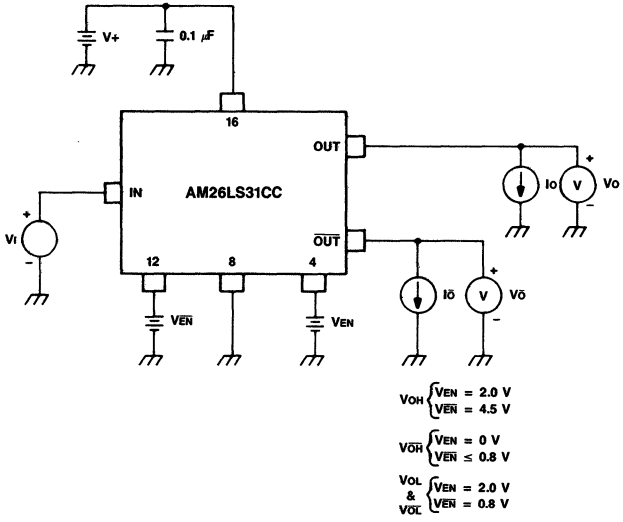


Figure 1. Output Voltages (High, Low)

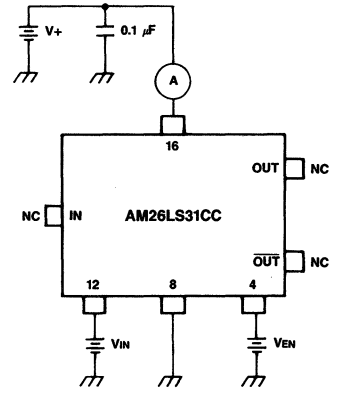


Figure 3. Power Supply Current, No Load & Disabled ($V_{EN} \leq 0.8$ V)

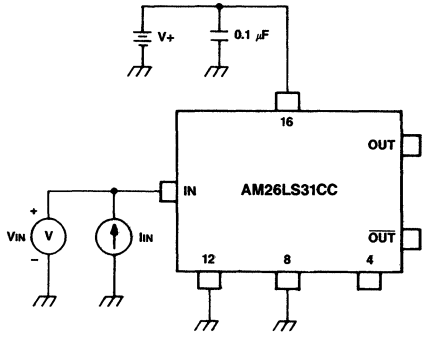


Figure 2. Input Clamp Voltage

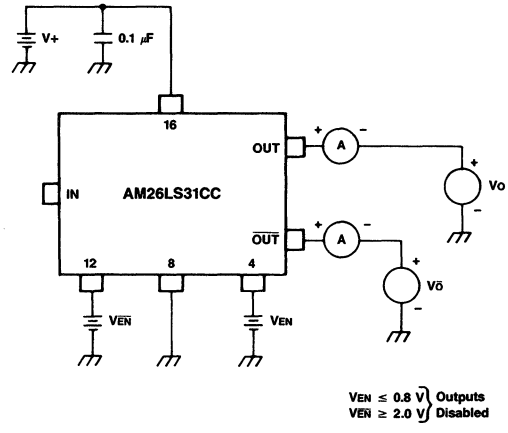


Figure 4. Output Current (Disabled)

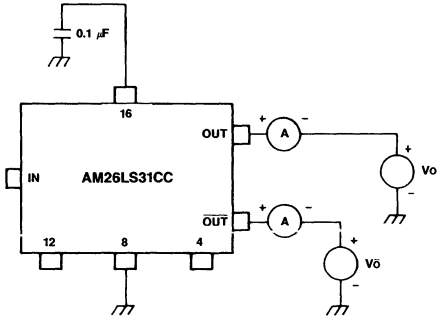


Figure 5. Output Current (Power OFF)

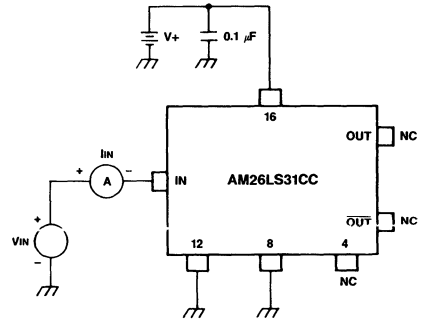


Figure 7. Input Currents (Low, High, Reverse)

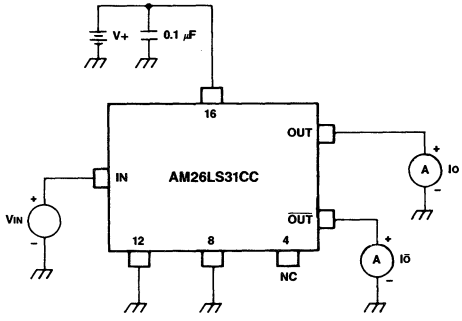


Figure 6. Output Current (Short Circuit)

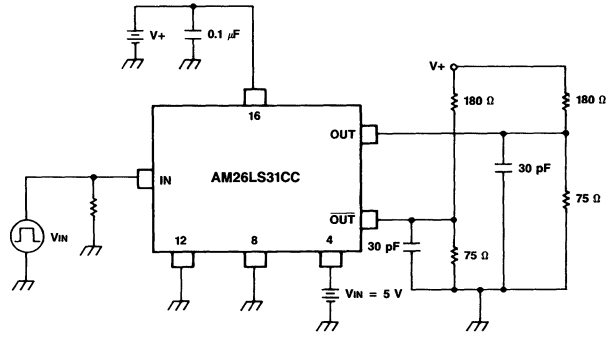
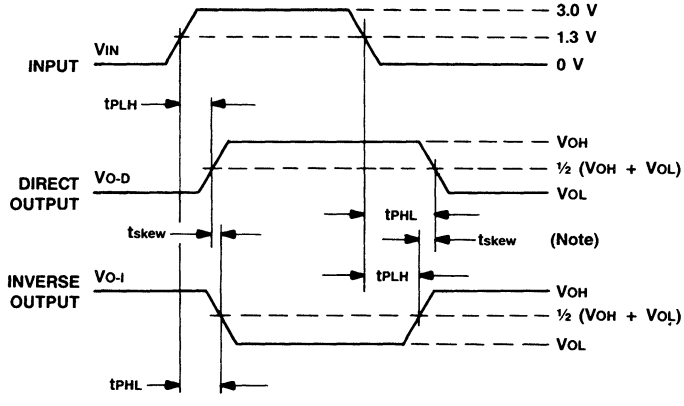
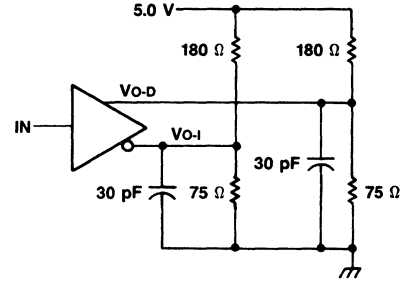


Figure 8. Switching Time

Timing Diagrams

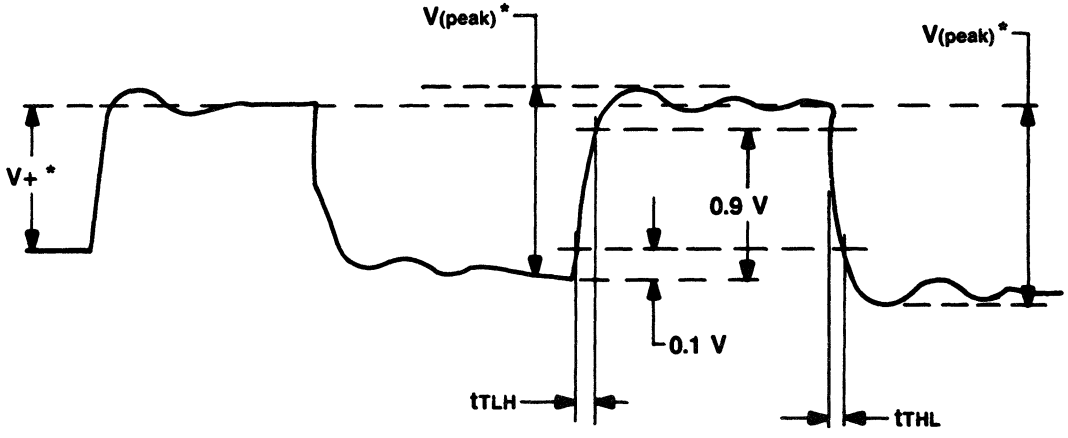




NOTE: t_{skew} IS DEFINED AS THE ABSOLUTE TIME DIFFERENCE BETWEEN THE AVERAGE VOLTAGE OF THE INPUT AND ITS COMPLEMENT. THE AVERAGE VOLTAGE IS ½ (V_{OH} + V_{OL}). EITHER OUTPUT, V_{O-D} OR V_{O-I}, MAY OCCUR FIRST.

Figure 9. Propagation Delay and t_{SKEW} Diagram and Associated Load Schematic

Timing Diagrams (Continued)



* WHERE V+ = STEADY STATE STEP VOLTAGE AND V(peak) = PEAK STEP VOLTAGE

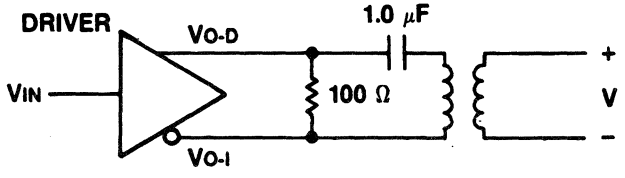


Figure 10. Overshoot Diagram and Associated Load Schematic

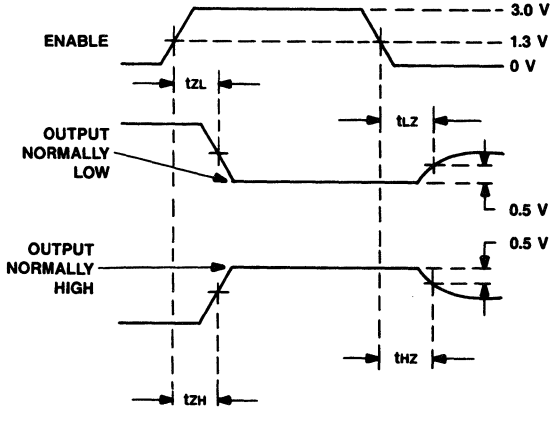


Figure 11. ENABLE and Output Waveforms

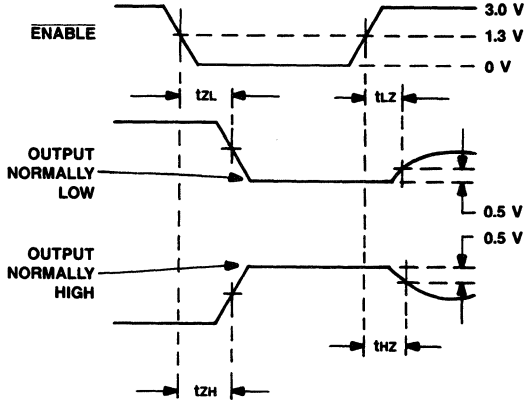


Figure 12. $\overline{\text{ENABLE}}$ and Output Waveforms

Timing Diagrams (Continued)

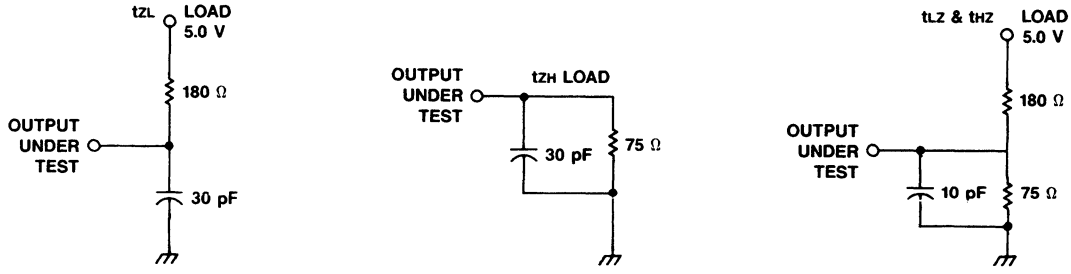


Figure 13. Associated ENABLE, $\overline{\text{ENABLE}}$ Loading Diagrams

Applications

The following Truth Table shows the V+, ENABLE, $\overline{\text{ENABLE}}$, and Data In conditions which must be met to provide specific Driver Output States (both direct and inverse outputs).

The application diagram (Figure 14) illustrates basic information for application of the AM26LS31CC Quad Line Driver device in a two-wire balanced RS-422A system.

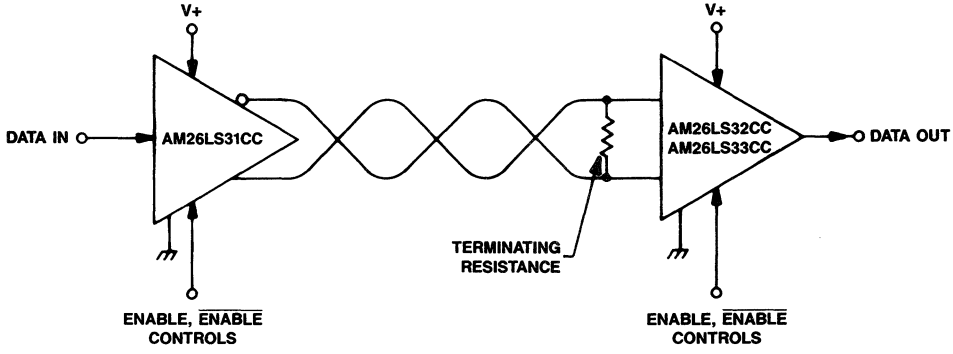


Figure 14. AM26LS31CC Quad Line Driver Application Diagram

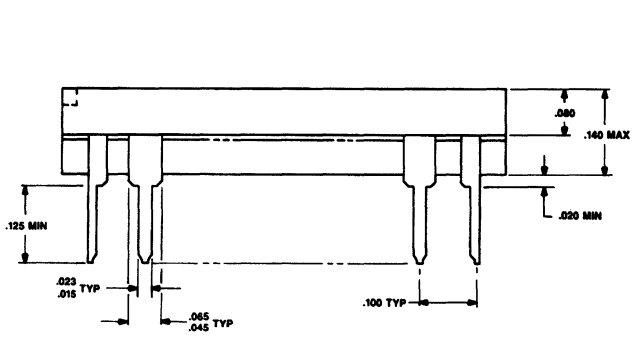
AM26LS31CC Quad Line Driver Truth Table

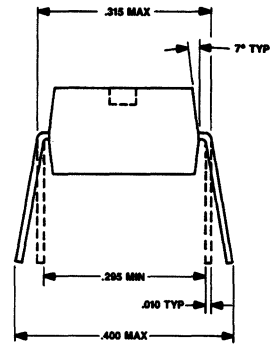
Condition*	Data In*	Direct Output	Inverse Output
ENABLE is High	High	High	Low
ENABLE is High	Low	Low	High
$\overline{\text{ENABLE}}$ is Low	High	High	Low
$\overline{\text{ENABLE}}$ is Low	Low	Low	High
ENABLE is Low $\overline{\text{ENABLE}}$ is Low	Don't Care	High Impedance	 Impedance
V+ is Low (≤ 0.5 V)	Don't Care	High Impedance	High Impedance

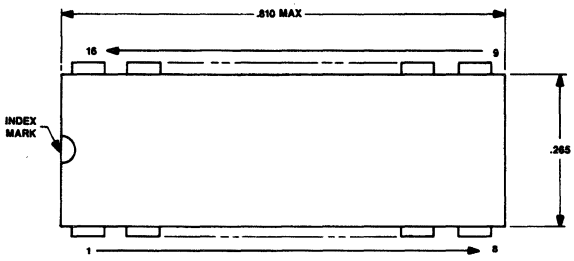
* High and Low levels for ENABLE, $\overline{\text{ENABLE}}$, and Data In are TTL levels ($V_{IH} \geq 2.0$ V, $V_{IL} \leq 0.8$ V).

Outline Drawing

(Dimensions in Inches)







Note: Pin numbers are shown for reference only

Ordering Information

Device	Comcode
AM26LS31CC	104438049

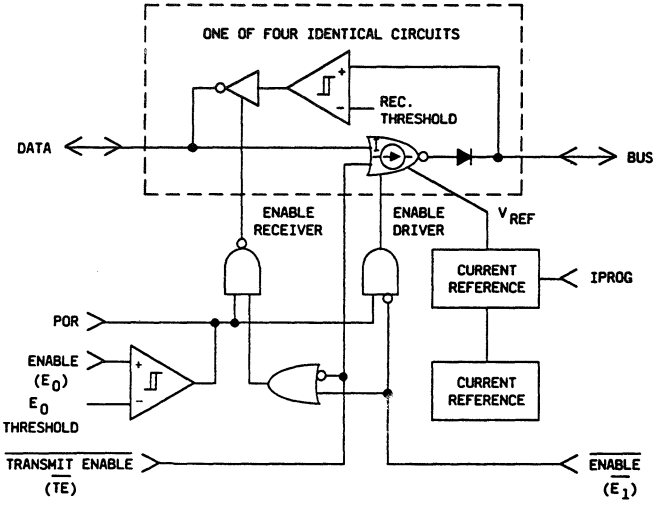
Description

The LB1025AC contains four independent transceivers. Each transceiver will interface circuit board logic with a large, low-impedance backplane party-line bus. It has current-source drive to the party-line bus and maintains a high-impedance load to this bus under all conditions. All receivers have 3-state outputs and their inputs have built-in hysteresis to improve noise control. Fail-safe design ensures that "transmit" is disabled when the enable pins are open.

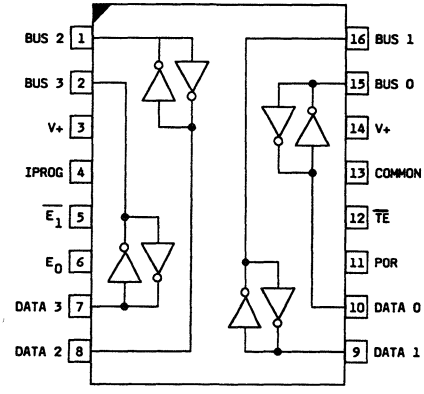
Features

- Four independent transceivers
- Low output capacitance (< 6 pF to bus)
- Simultaneous receive/transmit enabling of all transceivers
- TTL-compatible driver inputs
- 3-state receiver outputs
- Receiver input hysteresis
- Driver output high is 75 mA
- 4.75 V to 5.25 V supply voltage range

Functional Diagram



Pin Diagram



Maximum Ratings (At 25°C)	
Ambient Operating Temperature Range	0 to +70°C
Storage Temperature Range	−40 to +125°C
Pin Soldering Temperature (t = 15 sec.)	300°C
Operating Voltage (all pins)	5.5 V
Power Dissipation	600 mW

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions

(See Pin Diagram)

Pin	Name	Description
10 9 8 7	Data 0 Data 1 Data 2 Data 3	Data inputs/outputs. These pins connect to on-board logic.
15 16 1 2	Bus 0 Bus 1 Bus 2 Bus 3	Bus transmission line inputs/outputs. These pins connect to the "transmission line" backplane, interconnect between circuit boards.
3, 14	V+	External supply voltage (+4.75 V to 5.25 V). The supply voltage pins (3 and 14) are internally connected together.
13	COMMON	Circuit common (not necessarily physical or system ground).
6, 15	E_0 $\overline{E_1}$	Enable (zero) and $\overline{\text{Enable}}$ (one). See table 1 for logic programming of these pins.
12	$\overline{TE}$	Transmit/Receiver control input. See table 1 for logic programming of this pin.
11	POR	Power on reset. A non-inverting buffered signal of the E_0 input may be obtained from this pin.
4	IPROG	This pin should be connected to V+ for all applications.

Electrical Characteristics

(At 25°C)

Characteristic and Conditions				Min	Typical	Max	Unit
Driver Section	Input Voltage		High-Level	2.0	—	—	V
			Low-Level	—	—	0.8	
	Input Current		High-Level	—	−0.03	−40	μA
			Low-Level	—	−0.05	−0.2	mA
	Output Current		High-Level	−67.5	−75	−82.5	
			Low-Level	—	−20	−40	μA
Receiver Section	Input Threshold Voltage		High-to-Low	0.3	0.48	0.6	V
			Low-to-High	0.5	0.76	1.1	
	Hysteresis Voltage			200	270	500	mV
	Output Voltage		High-Level	2.4	4.05	—	V
			Low-Level	—	0.35	0.4	
	Input Current		High-Level	—	−7.0	−40	μA
			Low-Level	—	−20	−40	
	Output Current		Short-Circuit, Low-Level	15	50	150	mA
			Short-Circuit, High-Level	−15	−40	−150	
Logic Section	Input Voltage		$\overline{TE}$ High-Level	2.0	—	—	V
			$\overline{TE}$ Low-Level	—	—	0.8	
			E_0 Low-to-High	2.75	2.96	3.5	
			E_0 High-to-Low	1.75	2.1	2.5	
	Hysteresis Voltage		E_0 Input	0.5	0.85	1.5	
	Input Current	V_{IN} = 3.0 V	$\overline{TE}$ High-Level	—	−0.03	−20	μA
			$\overline{E_1}$ High-Level	—	−0.01	−20	
			E_0 High-Level	—	−0.1	−5.0	
		V_{IN} = 0.4 V	$\overline{TE}$ Low-Level	—	−0.07	−0.4	mA
			$\overline{E_1}$ Low-Level	—	—	−0.4	
		V_{IN} = 0.2 V	E_0 Low-Level	—	−1.4	−4.0	μA
Propagation Delay	Driver	See Figures 1 and 2	Low-to-High	—	9.0	40	ns
			High-to-Low	—	16	40	
	Receiver	See Figures 3 and 4	Low-to-High	—	30	45	
			High-to-Low	—	16	40	
	$\overline{TE}$ to Driver	See Figures 5 and 6	High-to-Low	—	20	50	
	$\overline{TE}$ to Receiver		High-to-Low	—	28	50	
			Low-to-High	—	40	60	
Power Supply	Current (Maximum)			—	380	500	mA
	Current (Quiescent, Idle)			—	65	90	

Test Circuits

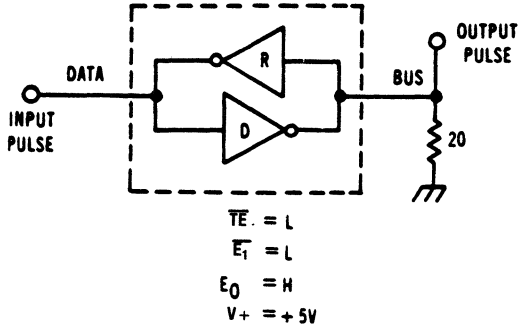


Figure 1. Driver Test Circuit

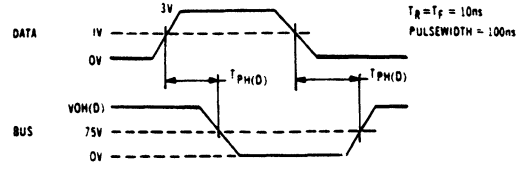


Figure 2. Driver Timing Waveform

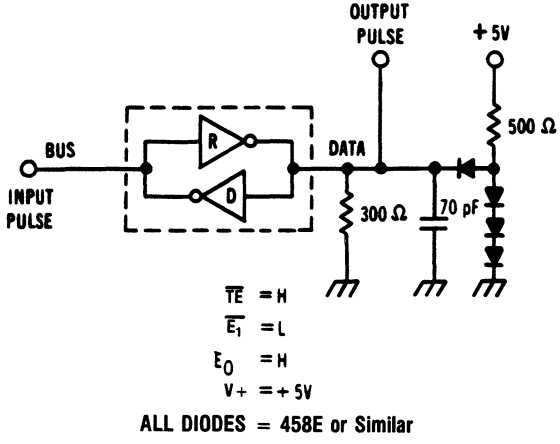


Figure 3. Receiver Test Circuit

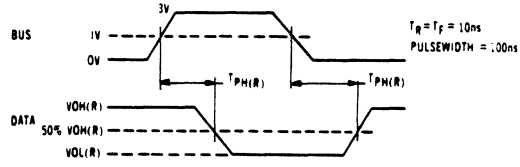


Figure 4. Receiver Timing Waveform

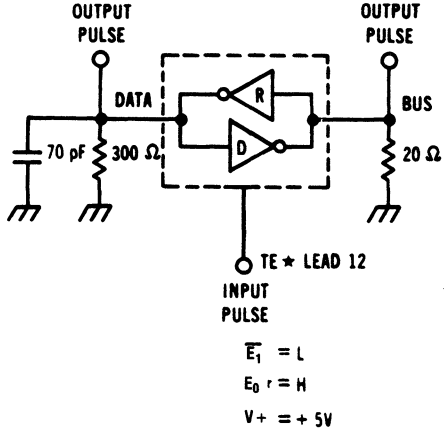


Figure 5. $\overline{TE}$ to Driver and Receiver Test Circuit

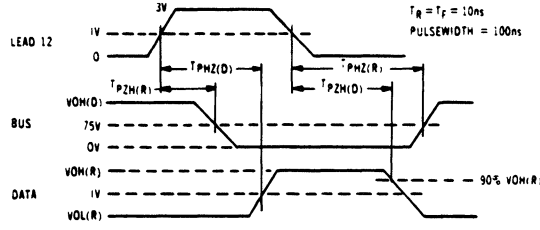


Figure 6. $\overline{TE}$ to Driver and Receiver Timing Waveform

Applications

Table 1 gives the logic information necessary for the operation of the LB1025AC Transceiver.

Figure 7 is a typical application of the Quad Bus Transceiver. This diagram illustrates the device when used as an interface between a 40-ohm party line bus and a computer or peripherals.

Table 1

LB1025AC Truth Table				
$\overline{TE}$	E_0 (NOTE 1)	$\overline{E_1}$	INFORMATION FLOW	OPERATION
0	0	0	Bus ➡ Data	Receiver
1	0	0	Bus ➡ Data	Receiver
0	1	0	Data ➡ Bus	Normal Transmit
1	1	0	Bus ➡ Data	Normal Receive
0	0	1	Bus ➡ Data	Receive
1	0	1	Bus ➡ Data	Receive
0	1	1	Isolate	Disable Device
1	1	1	Isolate	Disable Device

Note 1: E_0 is generally LOW only during the power-on-state. During the power-on-state, the transceiver is **forced** into the "receiver" state until the voltage at E_0 exceeds 3 volts.

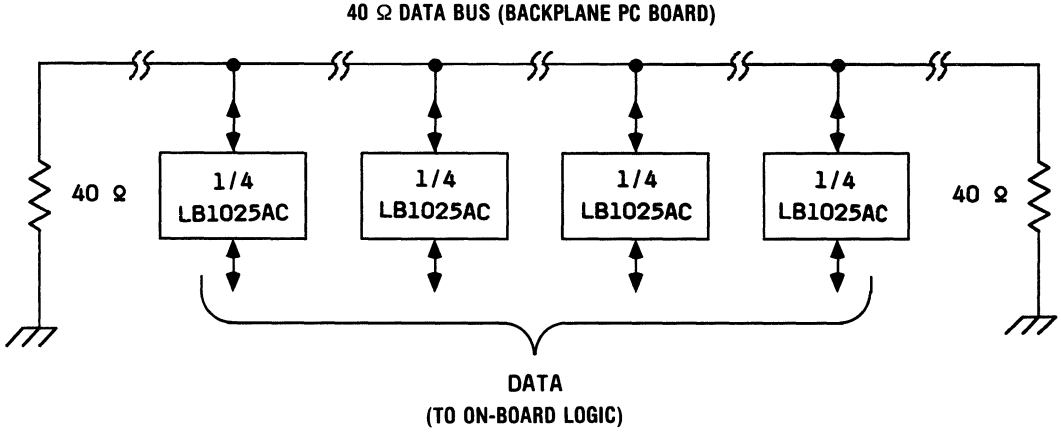
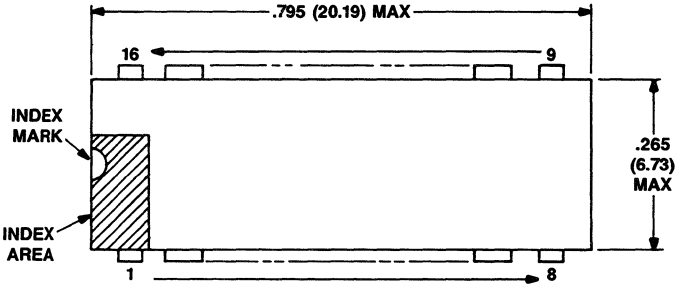
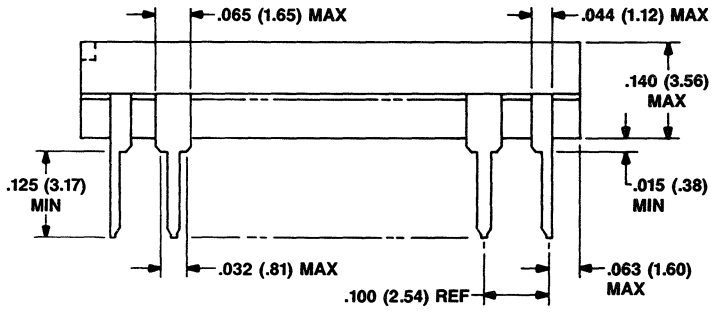


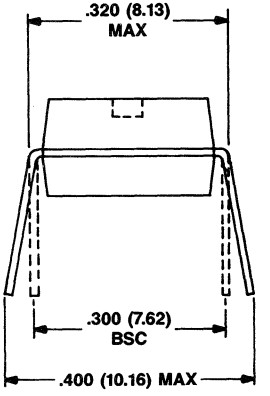
Figure 7. LB1025AC Quad Bus Transceiver Application Diagram

Outline Drawing

(Dimensions in Inches)







Ordering Information

Device	Comcode
LB1025AC	104208962

Description

The LS1128AC Compressor and the LS1129AC Expander or, used together, provide a Compandor function. The LS1128AC/LS1129AC Compandor was developed for (but not limited to) syllabic companding in voice-frequency applications.

The LS1128AC and LS1129AC are matched for low-distortion performance over a frequency range from 0 to 10 kHz. The device features superior thermal stability. The devices will operate from power supplied ranging from ±3.5 volts to ±6.0 volts. External resistors and capacitors are required for proper operation. Both the LS1128AC and LS1129AC are packaged in 16-pin dual-in-line plastic packages.

Compandors have numerous applications including telecommunications, cellular radio, telephone subscriber trunks, dynamic filtering, noise reduction circuits, and high-level limiters.

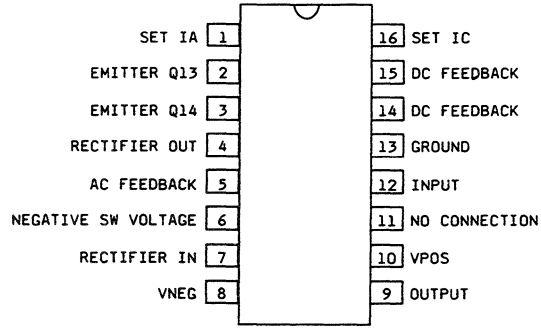
Features

- Low distortion
- Frequency range: 0 to 10 kHz
- Operates with power-supply voltage range ±3.5 to ±6.0 volts

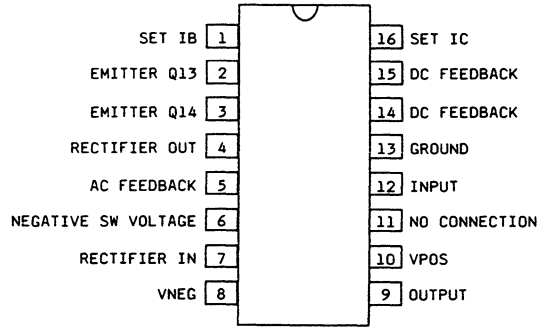
Maximum Ratings (At 25°C unless otherwise specified)	
Input Voltage	±7.5 V
Power Dissipation	200 mW
Storage Temperature Range	−40 to +125°C
Operating Temperature Range	0 to 60°C
Pin Soldering Temperature (t = 15 s max.)	300°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Diagram



LS1128AC PINOUT



LS1129AC PINOUT

Pin Description

Pin	Name/Function	Pin	Name/Function
1	Set I_A (LS1128AC) Set I_B (LS1129AC)	9	Output
2	Emitter Q13	10	V_{POS}
3	Emitter Q14	11	No Connection
4	Rectifier Output	12	Input
5	ac Feedback	13	Ground
6	Negative Switching Voltage	14	dc Feedback
7	Rectifier Input	15	dc Feedback
8	V_{NEG}	16	Set I_C

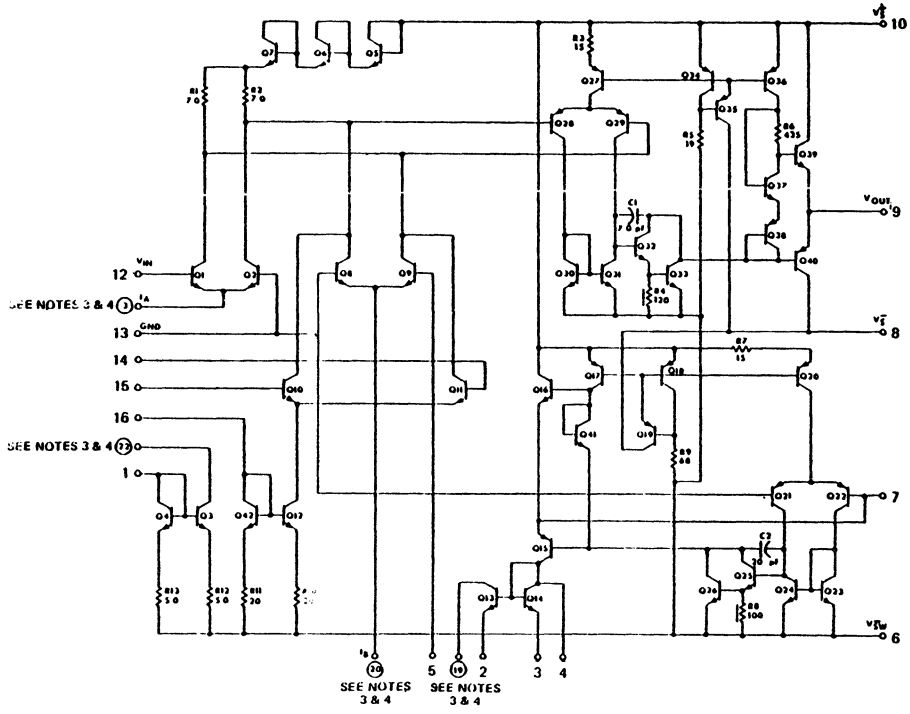
Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Minimum and maximum vales are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic	Test Condition		Min	Max	Unit
LS1128AC					
Output Voltage (f = 1.0 kHz, R_L = 5.0 kΩ)	V_{IN} = 725 mVrms		670	840	mVrms
	V_{IN} = 7.25 mVrms		52	72	
Output Offset Voltage			0	±80	mV
Input Offset Voltage (Rectifier, Lead 7)			0	±5.0	
Output Voltage Swing V_S = ±3.5 V, R_L = kΩ			+2.3 −1.9	—	V
Repeated Current [I_{IN}(Lead 7) = 100 μA]			94	104	μA
Power-Supply Current	V_S = ±6.0 V	Normal	1.4	2.8	mA
			−1.4	−2.8	
		Lead 6 Open, R_L = 2–10Ω	—	−50	μA
Base Current (I_E ≈ 24 μA)			—	0.56	
LS1129AC					
Output Voltage (f = 1.0 kHz)	V_{IN} = 745 mVrms		450	620	mVrms
	V_{IN} = 61.3 mVrms		4.3	6.5	
Output Offset Voltage			0	±80	mV
Input Offset Voltage (Rectifier, Lead 7)			0	±5.0	
Output Voltage Swing (V_S = ±3.5 V)			+2.2 −1.8	—	V
Repeated Current [I_{IN} (Lead 7) = 100 μA]			94	104	μA
Power-Supply Current	V_S = ±6.0 V	Normal	1.4	2.8	mA
			−1.4	−2.8	
		Lead 6 Open	—	−50	μA
Base Current (Q10) (I_E ≈ 24 μA)			—	0.54	

BASIC SCHEMATIC ‡



Notes:

1. All resistance values are in k ohms.
2. R4 & R8 are pinch resistors.
3. For LS1128AC these chip leads are internally connected: 3 to 22, and 19 to 20.
4. For LS1129AC these chip leads are internally connected: 3 to 19, and 20 to 22.
5. For connections, see Lead Identification Table.

Figure 1. Basic Schematic

Test Circuits

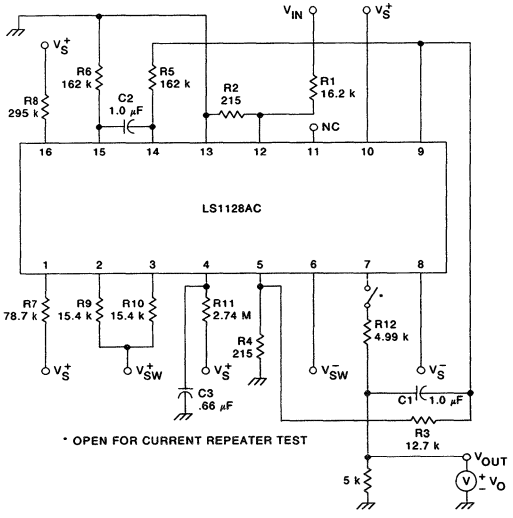


Figure 2A.

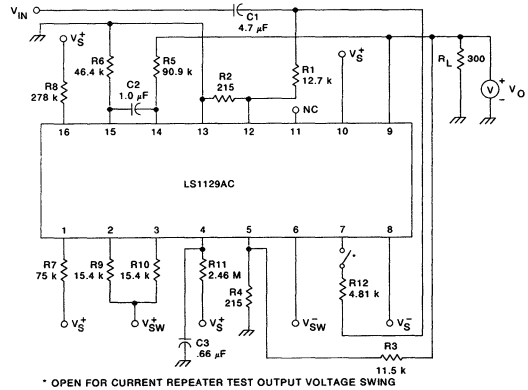


Figure 2B.

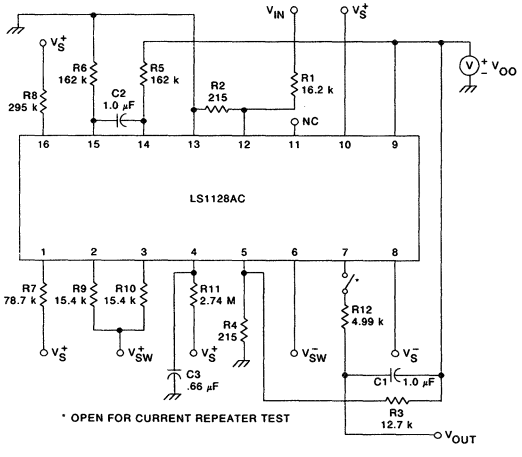


Figure 3A.

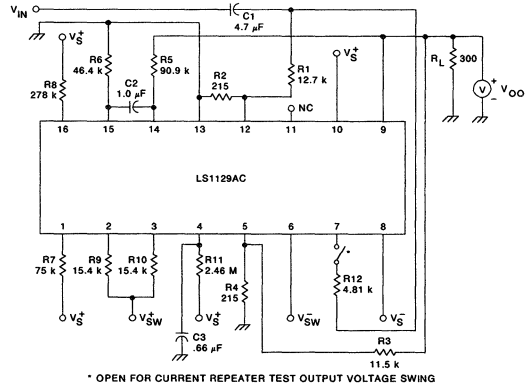


Figure 3B.

Note: All resistance values are in k ohms.

Test Circuits (Continued)

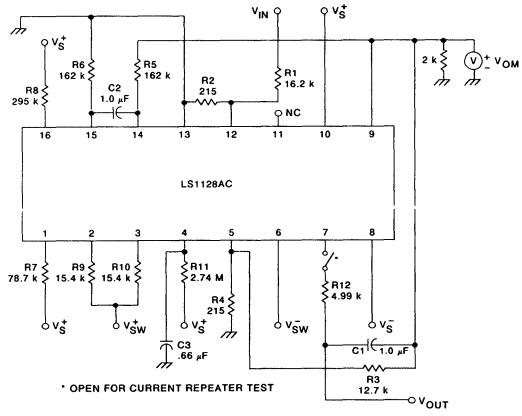


Figure 4A.

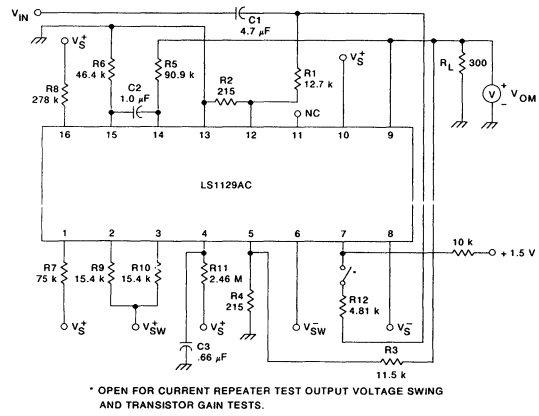


Figure 4B.

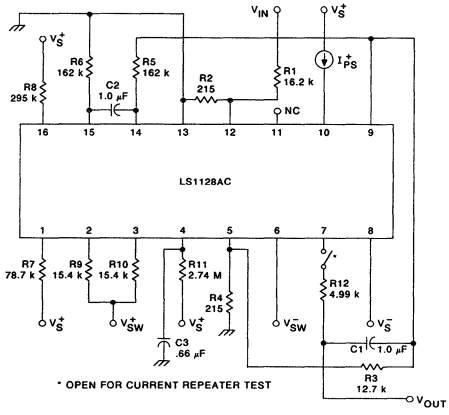


Figure 5A.

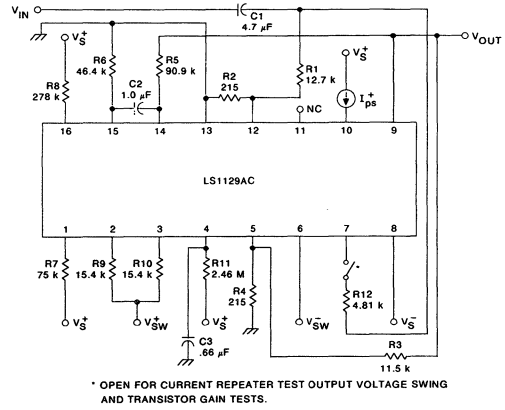


Figure 5B.

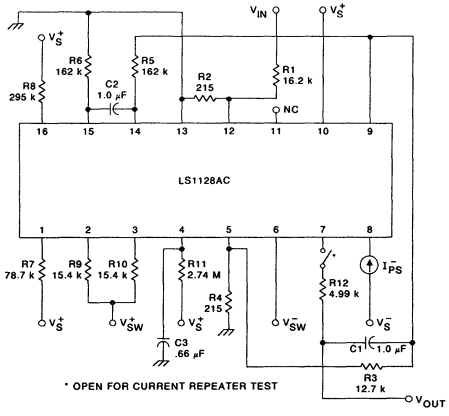


Figure 6A.

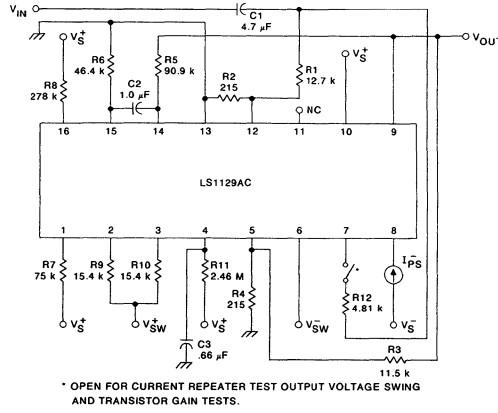


Figure 6B.

Note: All resistance values in k ohms.

Test Circuits (Continued)

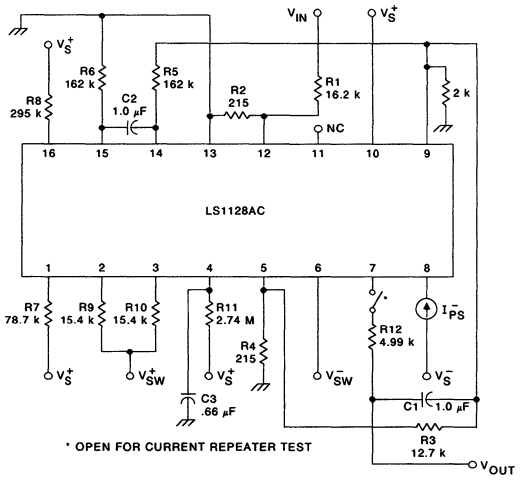


Figure 7A.

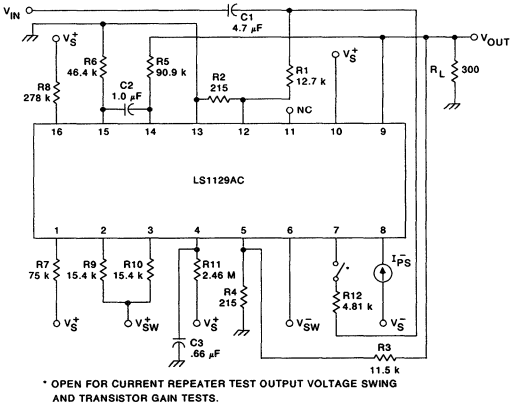
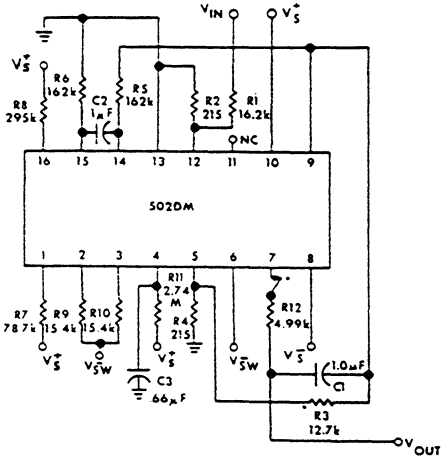


Figure 7B.

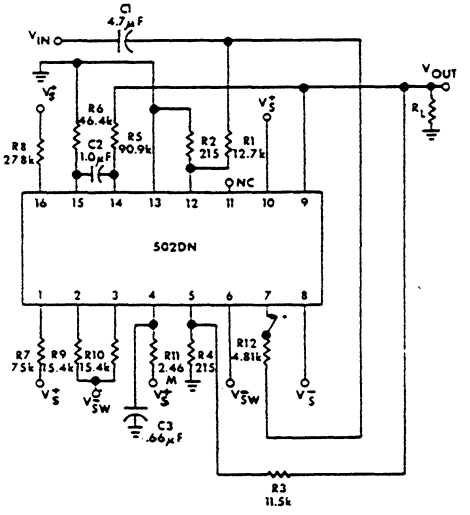
Note: All resistance values are in k ohms.

Typical Applications



*Open for current repeater test.

Figure 8. Typical Compressor Connections



*Open for current repeater, output voltage swing, and transistor gain tests.

Figure 9. Typical Expandor Connections

General Description

The LS1128AC is a compressor and the LS1129AC is an expandor for use in various compandor configurations. They are specifically characterized for (but not limited to) syllabic companding in voice-frequency circuits. The devices will operate from power supplies of ±3.5 volts to ±6.0 volts and require external capacitors and resistors for proper operation.

Characterization

The following series of graphs indicate the dependence of the output voltage on signal level, frequency and temperature over the ranges ordinarily used. They have been obtained by detailed measurements of units using the circuits shown in Figures 1 and 2.

Data are presented in terms of normalized input and output voltages.

Compressor: $Z = V_O/V_O$ (max) where V_O (max) = 1.5 Vrms
$Y = V_{IN}/V_{IN}$ (max) where V_{IN} (max) = 2.14 Vrms

Expandor: $W = V_O/V_O$ (max) where V_O (max) = 1.5 Vrms

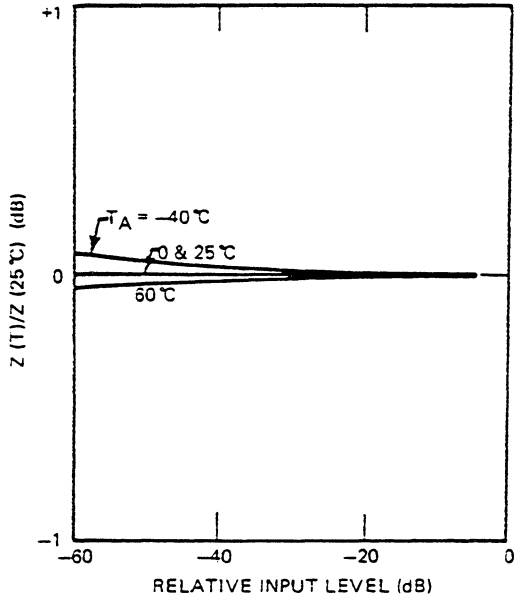


Figure 10. Temperature Stability of the Compressor

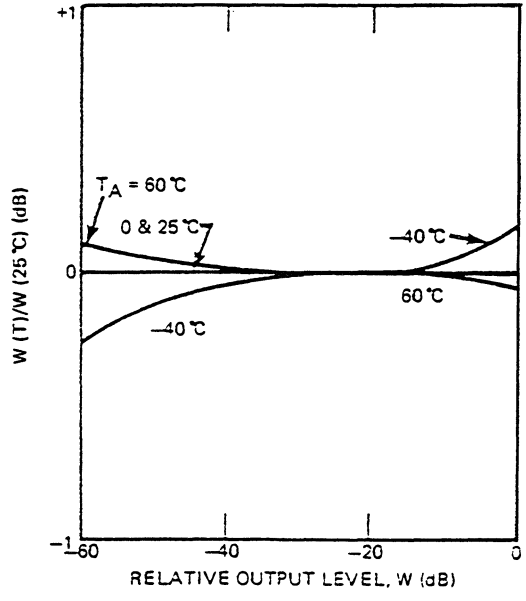


Figure 11. Temperature Stability of the Expandor

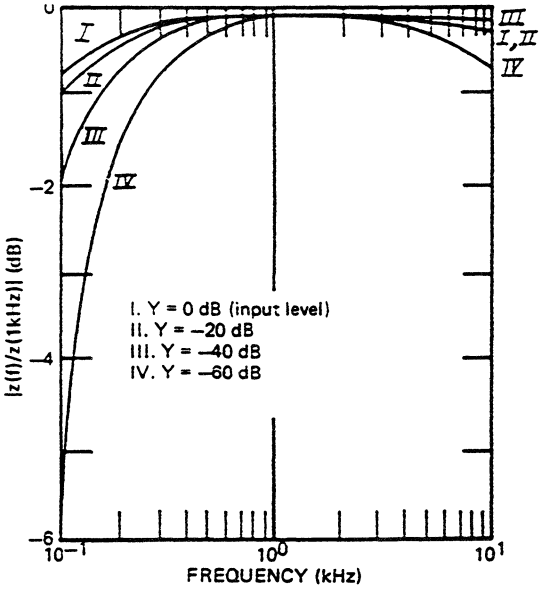


Figure 12. Frequency Response of the Compressor

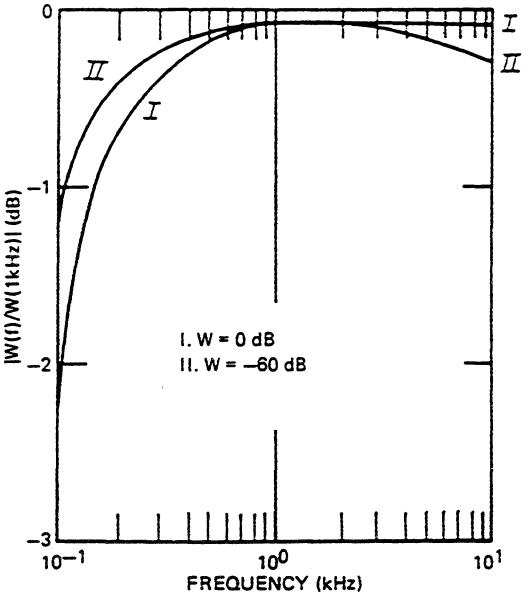


Figure 13. Frequency Response of the Expandor

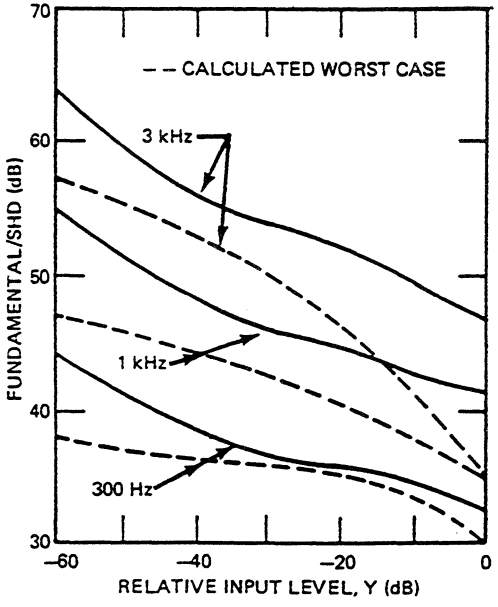


Figure 14. Second Harmonic Distortion of the Compressor

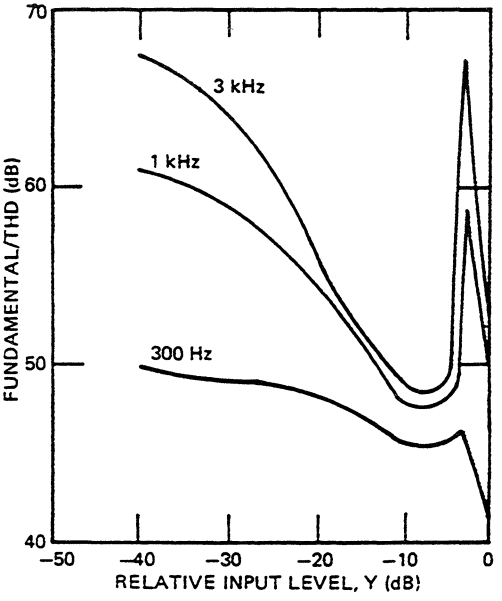


Figure 15. Third Harmonic Distortion of the Compressor

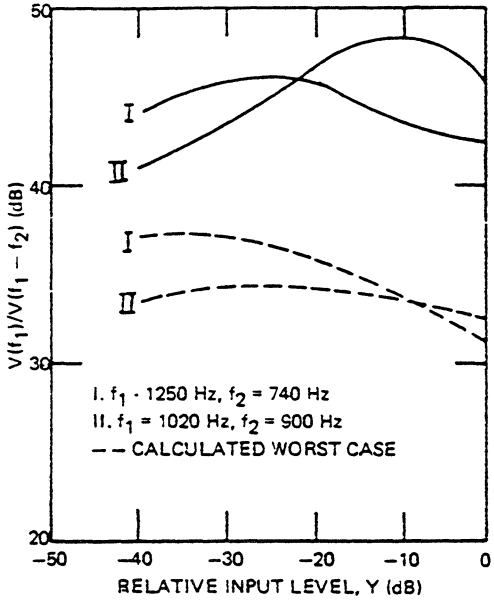


Figure 16. Intermodulation Product (f_1 — f_2) of the Compressor

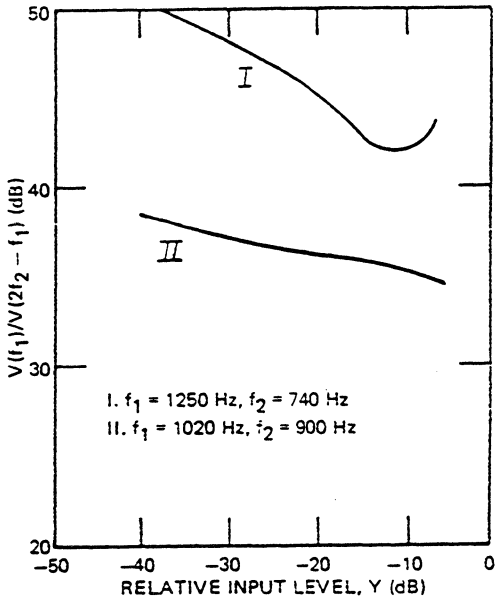


Figure 17. Intermodulation Product ($2f_2$ — f_1) of the Compressor

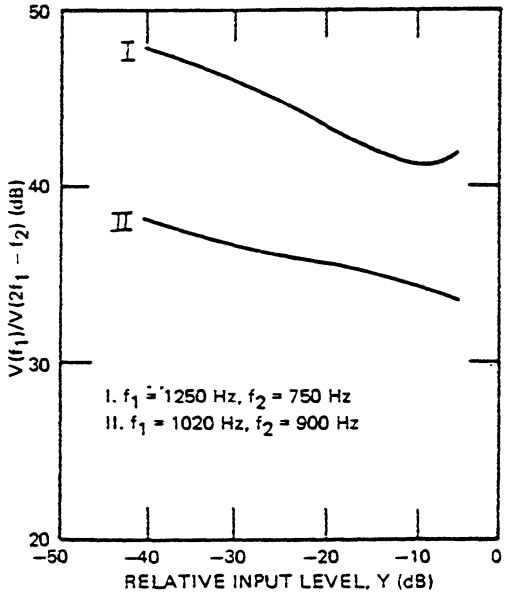
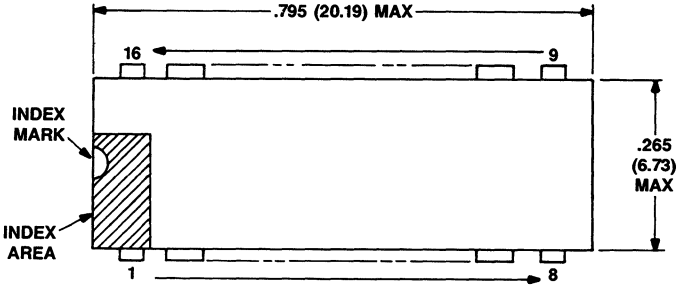
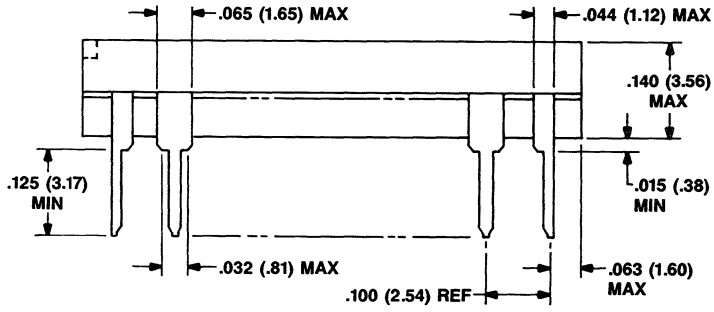


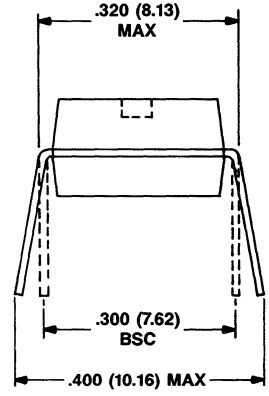
Figure 18. Intermodulation Product ($2f_1$ — f_2) of the Compressor

Outline Drawing

(Dimensions in Inches)







Ordering Information

Device	Comcode
LS1128AC	104413117
LS1129AC	104413133

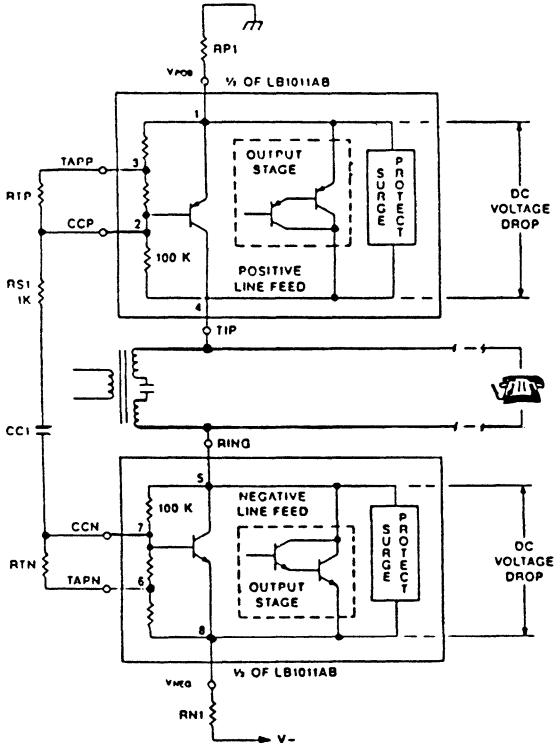
Description

The LB1011AB integrated circuit is a general purpose electronic battery feed circuit which supplies a controlled dc current to the TIP-RING pair of a telephone system. The battery feed circuitry presents a low impedance to dc currents, while presenting a high impedance to ac signals. The LB1011AB is integrated as two complementary chips to supply dc currents of both positive and negative polarities to either balanced or unbalanced lines. In the balanced line application, this device helps suppress undesirable common-mode signals.

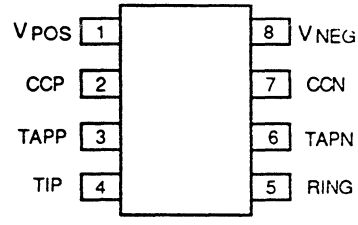
Features

- Basic battery feed function at a low cost
- High ac impedance characteristics for balanced line, differential-mode, voice-band signals
- Full internal lightning surge protection up to 4.0 amps
- dc voltage drops can be adjusted to accommodate different peak signal levels

Functional Diagram



Pin Diagram



Maximum Ratings (TA = 25°C unless otherwise specified)	
Ambient Operating Temperature Range	−20 to +70°C
Storage Temperature Range	−40 to +125°C
Pin Soldering Temperature (t = 15 seconds max.)	300°C
Current Positive Line Feed (VPOS-to TIP)	100 mA
Current, Negative Line Feed (RING-to-VNEG)	100 mA
Voltage, Positive Line Feed (VPOS-to-TIP)	(See testing requirements)
Voltage, Negative Line Feed (RING-to-VNEG)	(See testing requirements)

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions

Pin	Symbol	Name/Function
1	VPOS	This pin connects to the most positive external power supply (in some cases this may be ground) through an external resistor. This external resistor is a factor in determining the amount of current which will be supplied by the Positive Line Feed output.
2 7	CCP CCN	Cross-Coupling, positive and negative respectively. A capacitor between these two pins (for balanced-line configurations) creates a high ac impedance between TIP and RING. Since full TIP-to-RING voltage appears across these pins, it is recommended that a 1 kΩ resistor be placed in series with the cross-coupling capacitor for surge protection purposes. Unbalanced line applications should connect the cross-coupling capacitor to ground so that the common-mode impedance of the output is greatly increased.
3 6	TAPP TAPN	Resistor tap pins. These terminals are used to adjust the dc voltage drops across the Positive Line Feed and the Negative Line Feed respectively. The nominal dc voltage drop is three volts when no resistor is connected between pins 2 and 3, or pins 6 and 7. A short circuit between these same pin combinations will produce a nominal voltage drop of four volts. A resistor between these pin combinations will produce voltage drops varying between three and four volts. A higher dc voltage drop (greater than three volts) may be desirable for higher operating temperatures, or when the peak value of the ac signal exceeds 2.5 volts.
4	TIP	Output of the Positive Line Feed supply.
5	RING	Output of the Negative Line Feed supply.
8	VNEG	This pin connects to the most negative external power supply through an external resistor. This resistor is a factor in determining the amount of current which will be supplied by the Negative Line Feed output.

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Characteristic	Test Condition	Min	Typ	Max	Unit
dc Voltage Drop, Positive Line Feed	Figure 1	2.50	—	3.50	V
dc Voltage Drop, Negative Line Feed	Figure 1	2.50	—	3.50	V
dc Voltage Drop, Positive Line Feed (High-Level Mode)	Figure 1; (Pin 2 connected to Pin 3)	3.75	—	4.85	V
dc Voltage Drop, Negative Line Feed (High-Level Mode)	Figure 1; (Pin 6 connected to Pin 7)	3.60	—	4.00	V
Shunt Impedance	Figure 2	18	—	—	kΩ
Shunt Impedance, (High-Level Mode)	Figure 2; (Pin 2 connected to Pin 3) (Pin 6 connected to Pin 7)	18	—	—	kΩ
Common-Mode (Longitudinal) Rejection	Figure 3	45	—	—	dB
Common-Mode (Longitudinal) Rejection (High-Level Mode)	Figure 3; (Pin 2 connected to Pin 3) (Pin 6 connected to Pin 7)	45	—	—	dB
Distortion	Figure 4	—	—	2.0	%
Distortion (High-Level Mode)	Figure 4 (Pin 2 connected to Pin 3) (Pin 6 connected to Pin 7)	—	—	2.0	%
Base-to-Emitter Voltage, Positive Line Feed	Figure 5; IPOS = 50 mA	1.0	—	2.0	V
Base-to-Emitter Voltage, Positive Line Feed	Figure 5; IPOS = 100 mA				
Base-to-Emitter Voltage Change, Positive Line Feed	Figure 5; ΔV = [V @ 100 mA] minus [V @ 50 mA]	25	—	250	mV
Base-to-Emitter Voltage, Negative Line Feed	Figure 5; INEG = 50 mA	1.0	—	2.0	V
Base-to-Emitter Voltage, Negative Line Feed	Figure 5; INEG = 100 mA				
Base-to-Emitter Voltage Change, Negative Line Feed	Figure 5; ΔV = [V @ 100 mA] minus [V @ 50 mA]	25	—	250	mV

Electrical Characteristics

($T_A = 25°C$ unless otherwise specified)

Characteristic	Test Condition	Min	Typ	Max	Unit
Battery Feed, Total Voltage	Figure 6; Ibf = 50 mA	5.0	—	6.8	V
Battery Feed, Total Voltage	Figure 6; Ibf = 100 mA				
Change in Total Voltage $\triangle V$ = [V @ 100 mA] minus [V @ 50 mA]	Figure 6;	−400	—	+600	V
Battery Feed, Total Voltage (High-Level Mode)	Figure 6; Ibf = 50 mA (Pin 2 connected to Pin 3) (Pin 6 connected to Pin 7)	7.2	—	9.4	V
Battery Feed, Total Voltage (High-Level Mode)	Figure 6; IBM = 100 mA (Pin 2 connected to Pin 3) (Pin 6 connected to Pin 7)				
Change in Total Voltage (High-Level Mode) $\triangle V$ = [V @ 100 mA] minus [V @ 50 mA]	Figure 6; (Pin 2 connected to Pin 3) (Pin 6 connected to Pin 7)	−400	—	+600	V
Line/Supply Voltage Positive Line Feed Negative Line Feed	Figure 7; IT = 200 mA	 — —	 — —	 1.4 1.4	 V V
PNPN Breakdown Voltage Positive Line Feed Negative Line Feed	Figure 7; IT = 35 mA (Pin 2 connected to Pin 1) (Pin 7 connected to Pin 8)	 8.0 8.0	 — —	 10 10	 V V
PNPN Sustain Voltage Positive Line Feed Negative Line Feed	Figure 7; IT = 200 mA (Pin 2 connected to Pin 1) (Pin 7 connected to Pin 8)	 2.0 2.0	 — —	 5.0 5.0	 V V
Line/Cross-Coupling Voltage Positive Line Feed Negative Line Feed	Figure 8	 — —	 — —	 1.4 1.4	 V V
Supply/Cross-Coupling Voltage Positive Line Feed Negative Line Feed	Figure 9	 — —	 — —	 1.4 1.4	 V V

Test Circuits

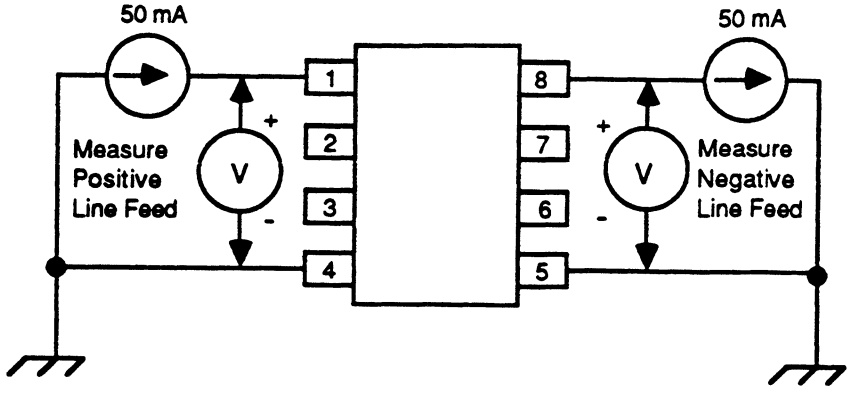
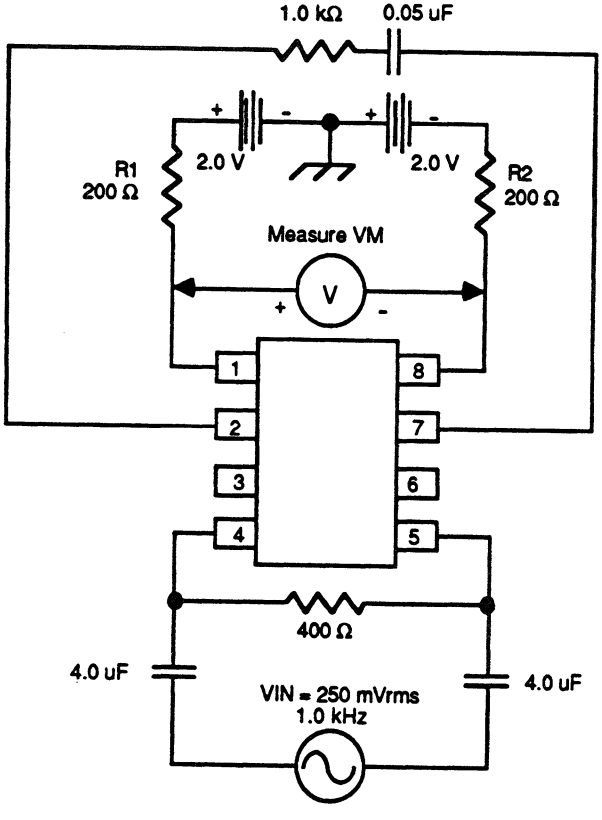


Figure 1. DC Voltage Drop, Test Circuit



R1 and R2 are matched to within 0.1 %.

$$\text{Shunt Impedance (in ohms)} = \frac{100}{\text{VM (in volts)}}$$

Figure 2. Shunt Impedance, Test Circuit

Test Circuits
(Continued)

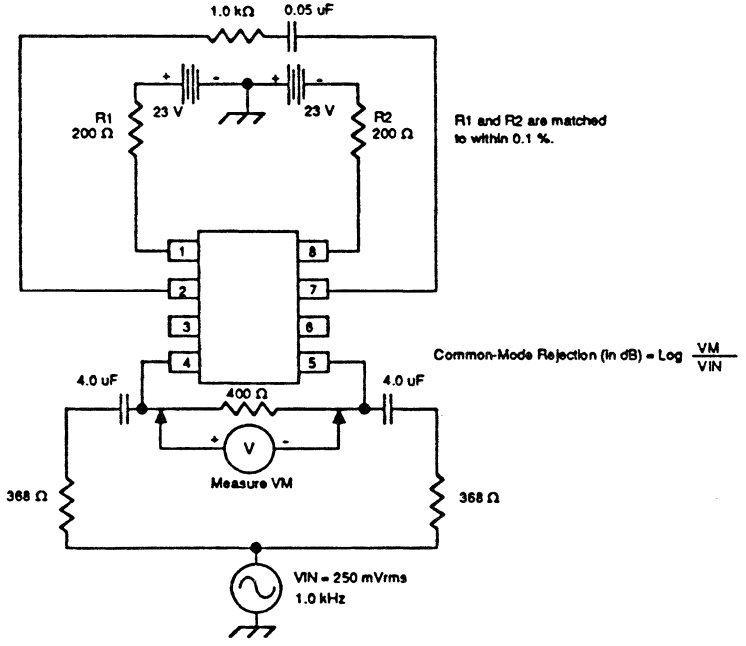


Figure 3. Common-Mode Rejection, Test Circuit

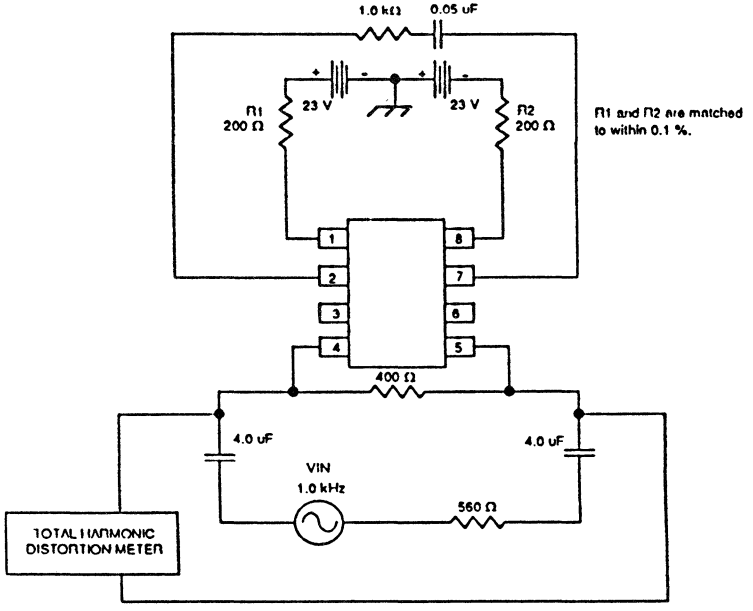


Figure 4. Distortion, Test Circuit

Test Circuits
(Continued)

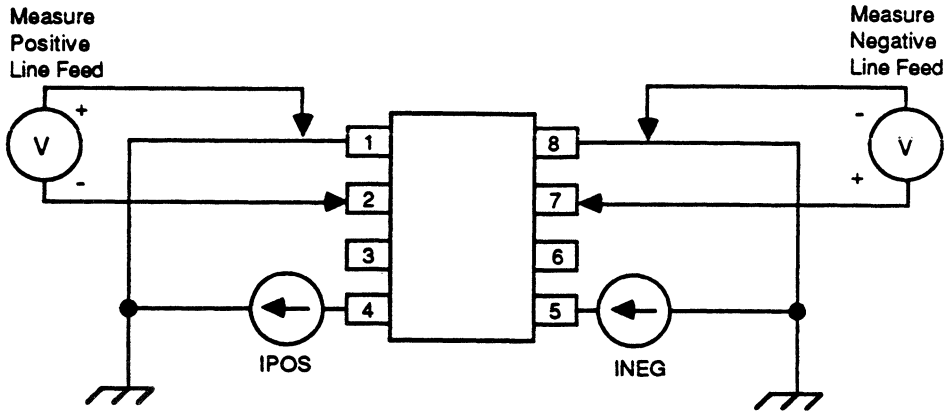


Figure 5. Base-to-Emitter Voltage, Test Circuit

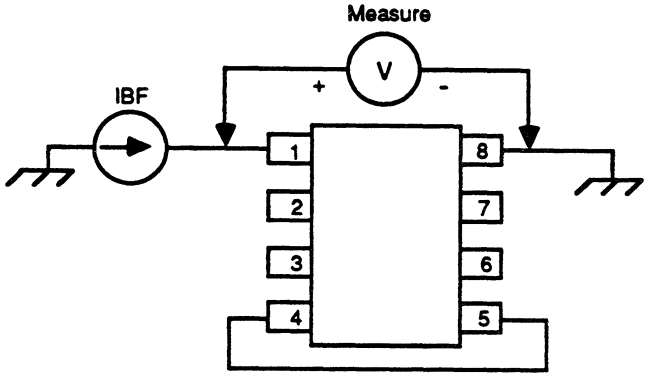


Figure 6. Battery Feed Total Voltage, Test Circuit

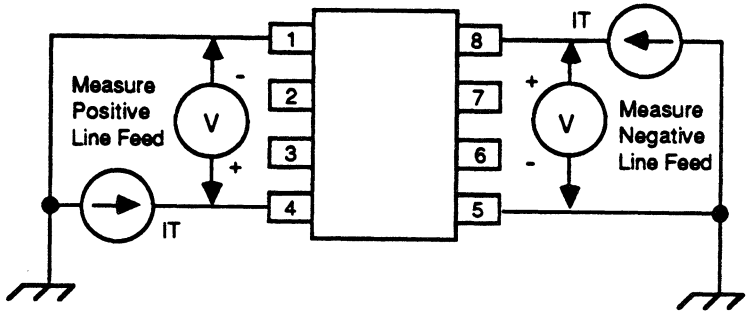


Figure 7. Line/Supply Voltage, Test Circuit

Test Circuits
(Continued)

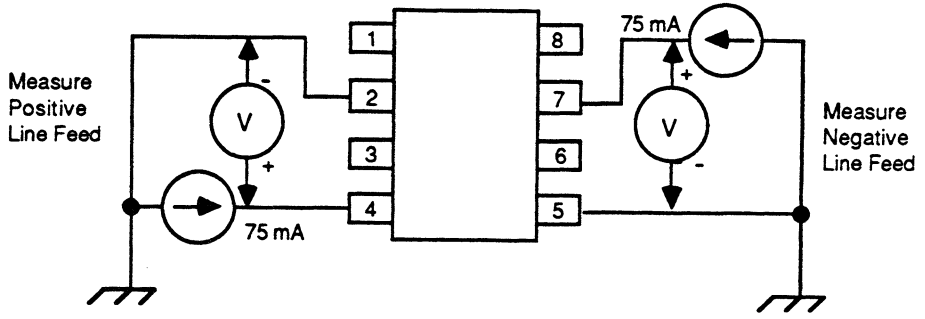


Figure 8. Line/Cross Coupling Voltage, Test Circuit

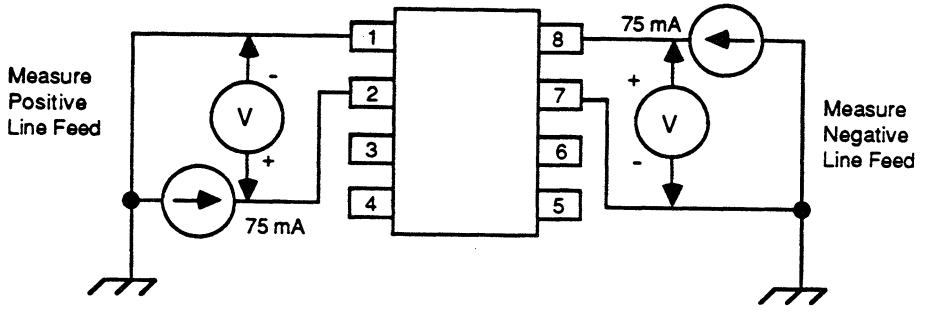


Figure 9. Supply/Cross Coupling Voltage, Test Circuit

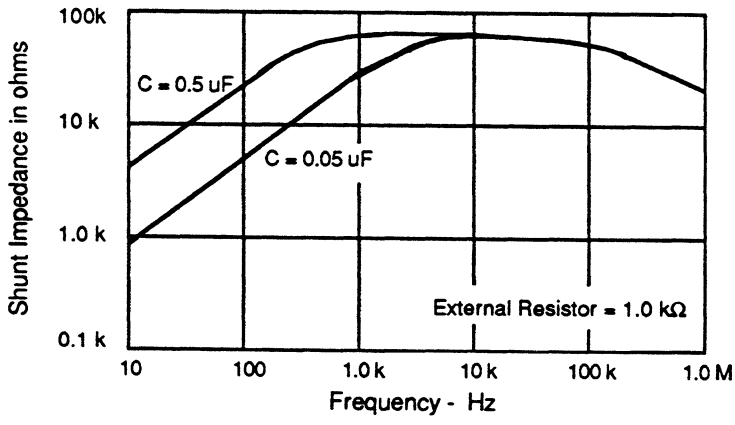


Figure 10. Typical Shunt Impedance vs Frequency

Surge Protection Characteristics

Internal surge protection circuitry (Functional Diagram), in conjunction with external resistors, provides protection against forward voltage surges. Reverse surges are dissipated through large internal diodes bridged across each Line Feed section.

Forward surge protection consists of a PNPN composite device. This PNPN composite device can withstand surges as shown in Figure 11. It has a breakover point (V_{BO}) of approximately 9.0 volts, as shown in Figure 12. After breakover, the output is clamped at less than 2.0 volts as long as the surge source supplies more than 150 mA. When the surge source drops below 150 mA, the PNPN device recovers and normal operations resume.

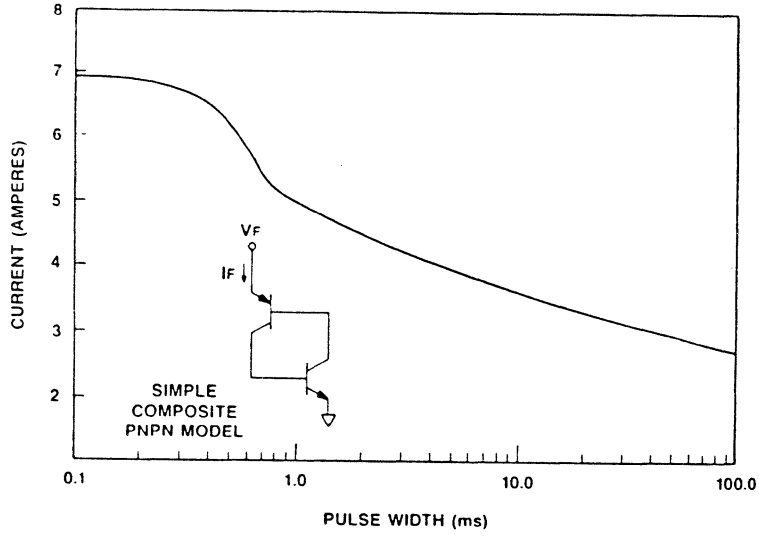


Figure 11. Maximum Applied Forward Surge Limits (PNPN Composite Device)

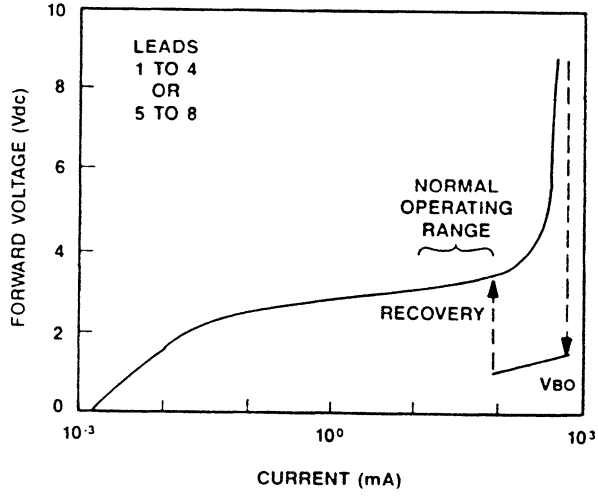


Figure 12. Typical Voltage vs Current (PNPN Composite Device)

Applications

Figure 13 shows the LB1011AB in a balanced configuration. The complementary Positive and Negative Line Feeds are capacitively cross-coupled.

Differential signals on the balanced line (TIP-RING) do not disturb the ac ground at the center of the cross-coupled connection. Therefore, both circuits act as constant current sources that present a high shunt impedance of approximately 50 kΩ.

The cross-coupling does not affect feedback for either dc or common-mode signals. Therefore, for common-mode noise, the two complementary power supplies act as low impedance paths to ground through the resistors connected to V_{POS} and V_{NEG}. Common-mode rejection depends on the degree of matching between resistors RP1 and RP2.

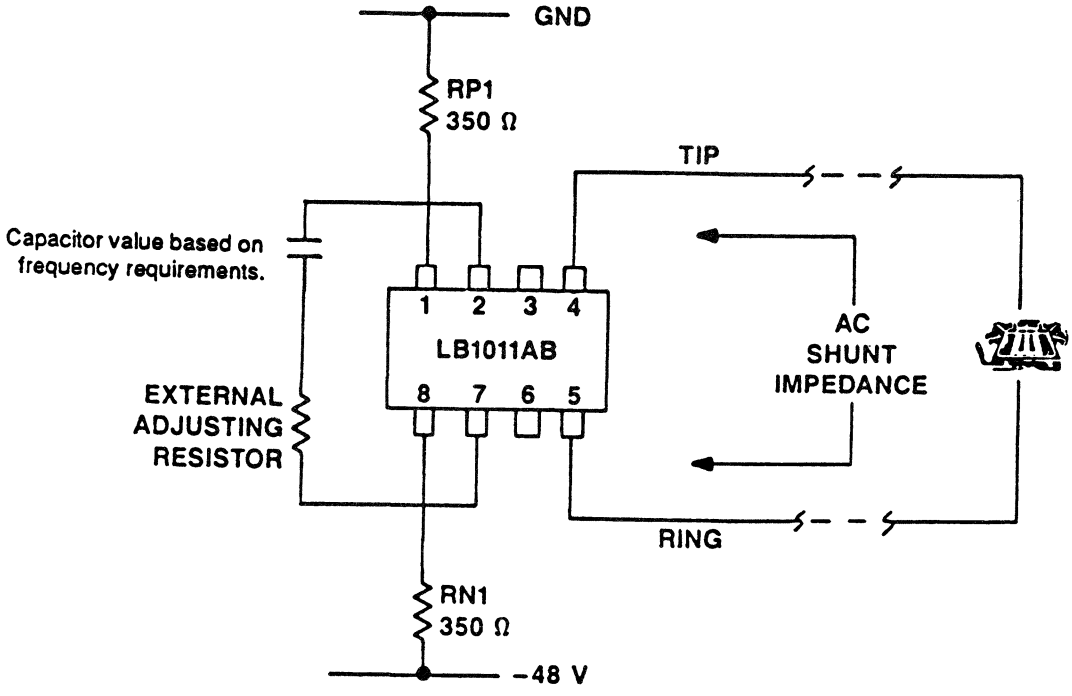


Figure 13. Battery Feed Application (Balanced Configuration)

Applications
(Continued)

Figure 14 illustrates the LB1011AB as a single-ended configuration which exhibits a very low dc impedance and a very high ac impedance.

In some applications (where dc current needs to flow and ac current should be blocked) this LB1011AB configuration can replace an inductor. It does not, however, have the "phase and amplitude versus frequency" characteristics of a true inductor or RL network.

The TAPP connection (Pin 2) permits an external resistor (RTP) to change the dc voltage drop (Functional Diagram). RTP can be selected to raise the voltage from 3.0 volts (normal operating value to as high as 4.0 volts). This voltage may be desirable for high operating temperatures, or if the peak voltage of the ac signal exceeds 2.5 volts.

Since the dc voltage drop is relatively constant, the current supplied to the line is controlled by the supply voltage, the external resistor to the supply, and the resistance which shunts the line. For ac signals, however, the capacitively-coupled ground causes the LB1011AB to operate as a constant-current source with an impedance of approximately 25 kΩ.

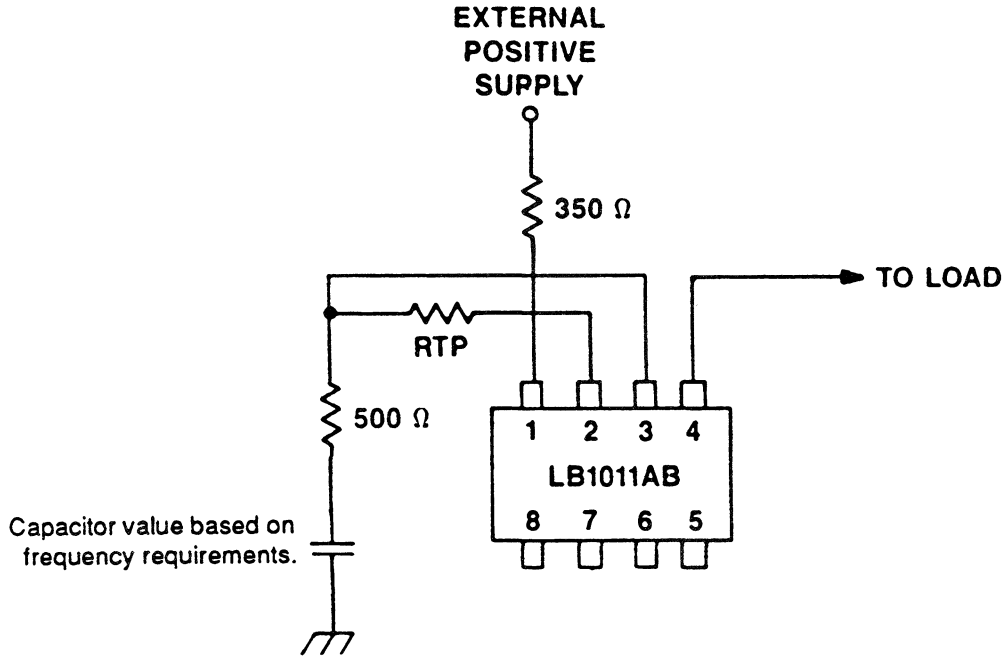
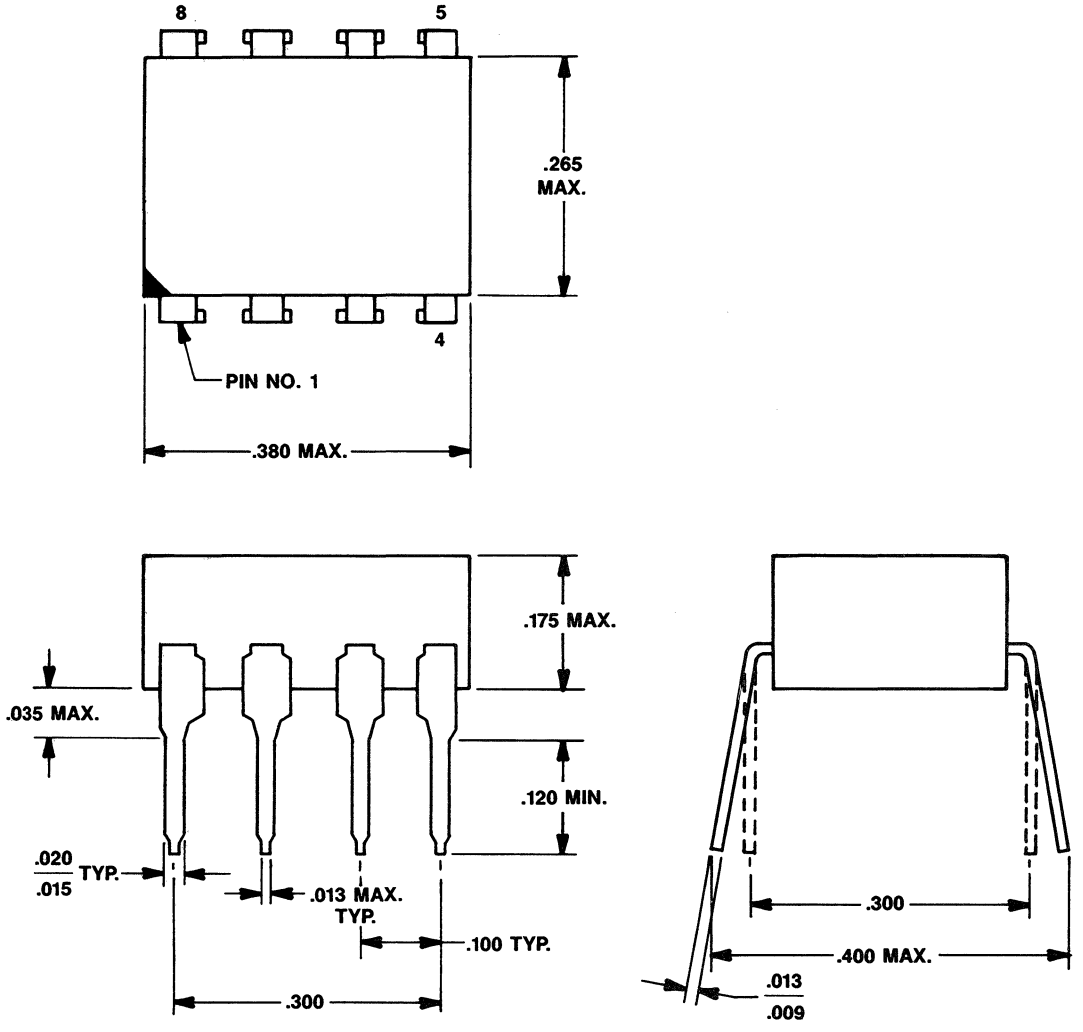


Figure 14. Battery Feed Application (Unbalanced Configuration)

Outline Drawing

(Dimensions in inches)



Ordering Information

Device	Comcode
LB1011AB	104208814

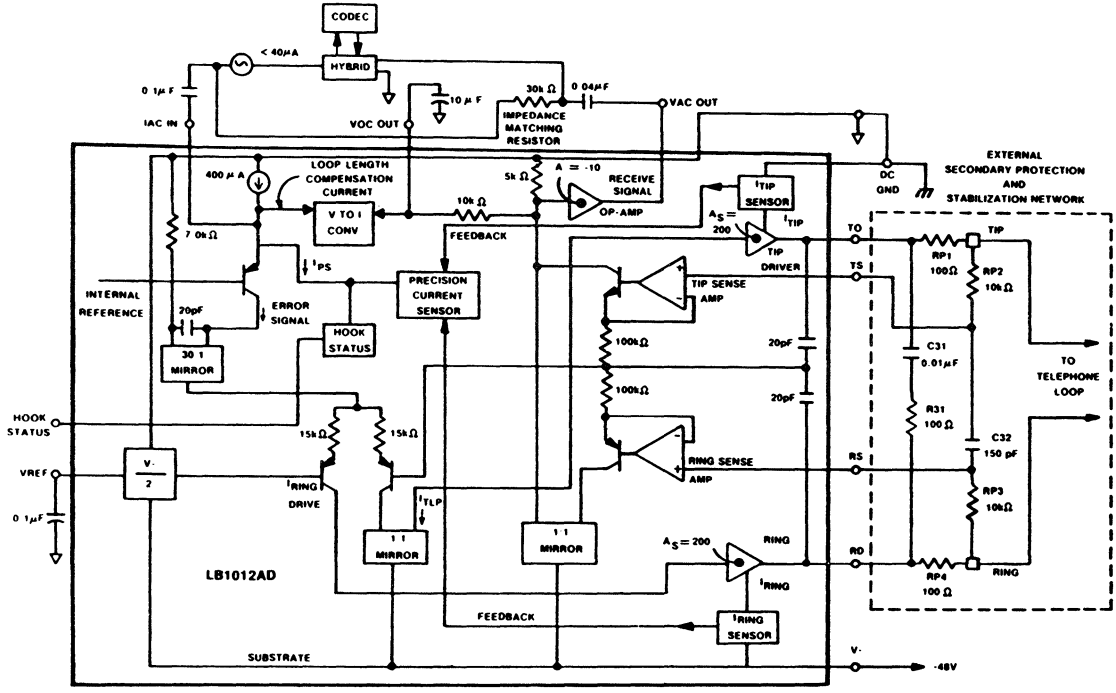
Description

The LB1012AA/AD integrated circuit is an electronic battery-feed circuit which supplies a controlled dc current to the TIP-RING pair of a telephone system. The battery-feed circuitry presents a low impedance to dc current, while presenting a high impedance to ac signals. The LB1012AA/AD contains input and output terminals for voice-frequency signals and a hook-status output signal. The LB1012AA is available in wafer form and the LB1012AD is available in an 18-pin DIP package.

Features

- Drives loop lengths up to 1300 Ω
- Proper line matching can be provided with a 50:1 scaled network: 30 kΩ provide a 600 Ω termination
- Common-mode rejection (longitudinal balance) better than 60 dB (ac)
- TTL-compatible "hook-status" indicator
- Longitudinal balance and amplifier gains are laser trimmed

Functional Diagram



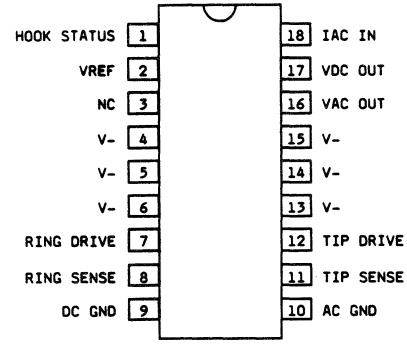
Maximum Ratings (At $T_A = 25°C$ unless otherwise specified)	
Ambient Operating Temperature Range	−20 to +70°C
Storage Temperature Range	−40 to +125°C
Lead Soldering Temperature (15 s. max.) (LB1012AD)	300°C
Power Dissipation (Note 1) (LB1012AD)	2.0 W
Voltage, HOOK STATUS to V−	60 V
Voltage, GND to V−	60 V
Voltage (HOOK STATUS to GND)	5.5 V
Current (TIP DRIVE)	50 mA

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may affect device reliability.

Note 1:
Care in mounting and proper environmental conditions are required to keep the operating temperature acceptably low. The package of this device has a thermal resistance of approximately 12°C/W to its mounting plane. The remainder of its environment (thermal resistance of wiring board mounting plane to ambient) should not exceed an additional 30°C/W. Forced air circulation over the IC or high-thermal-conductivity wiring boards may be needed.

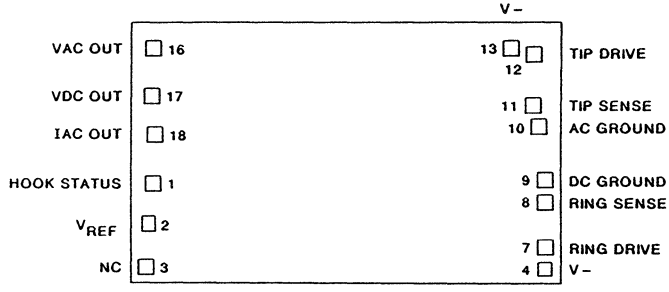
Thermal impedance between the package and the connecting mounting path may be minimized by connecting the V− pins to as large a thermally conductive land area as is practical to place on the mounting board. See the V− pin description for additional information.

Pin Diagram



LB1012AD

Pad Diagram

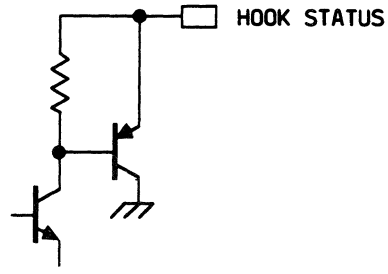


LB1012AA

Recommended Operating Conditions	
Voltage Range (GND to V−)	−42 to −53 V (Note 2)
Voltage (HOOK STATUS to GND)	+5.0 V

Note 2:
These conditions assume continuous operation with the HOOK STATUS operating at 5.0 volts. Momentary excursions ($t \leq 100$ ms) to −55 volts are permissible.

Pin Descriptions

Pin	Symbol	Name/Function
1	HOOK STATUS	HOOK STATUS output, TTL compatible (See Figure 1). This circuit function performs very much like an open collector NPN. When the phone is ON-HOOK, the drive current is zero and the output is essentially an open circuit. A 50 kΩ pull-up resistor to +5 volts will raise the output voltage to 5 volts (indicating a logic HIGH). When the phone is OFF-HOOK, and with loop currents greater than 16 mA the HOOK STATUS voltage will be ≤ 200 mV, indicating a logic low. The drive current is approximately 100 μA and the output is pulled down until the collector-base junction of the PNP is sufficiently forward biased to remove the excess bias current. The HOOK STATUS output will sink at least 1 mA of current for all operating conditions. The criteria for OFF-HOOK detection is that the sum of TIP and RING current must exceed a nominal 30 mA (20 mA to 36 mA). However, HOOK STATUS is disabled during ringing when the RING current is approximately zero.  **Figure 1. Simplied HOOK STATUS Output Circuit**
2	VREF	This pin connects to an internal reference voltage (approximately ½ of the V− voltage). A bypass capacitor should be connected from this pin to the signal ground pin to maximize power-supply rejection characteristics.
3	NC	No connection. This pin should **not** be used as an external tie point.
4 5 6	V− V− V−	The most negative external supply voltage is connected to these pins. Pins 4, 5 and 6 are physically connected together with a large metal area internal to the package. This statement is also true for pins 13, 14 and 15. All of these pins should be connected to the external V− supply and to a large plated area on the printed circuit board for heat dissipation.
7	RING DRIVE	Output of the RING DRIVE (RD) amplifier. A protective resistor should go between this pin and the RING side of the active load (Functional Diagram).
8	RING SENSE	Input to the RING SENSE (RS) amplifier. This pin should be connected through a resistor to the RING side of the active load (Functional Diagram). The separation of the RING DRIVE and the RING SENSE allows the use of a low-cost protective RC network (RP1-RP4 in Functional Diagram).
9	DC GND	High-current dc ground. This is the main source of TIP dc current. This pin connects directly to system ground and is the most positive power supply connection (note that HOOK STATUS is +5.0 volts with respect to pin 9).

Pin Descriptions (Continued)

Pin	Symbol	Name/Function
10	AC GND	AC (signal ground). All signal bypass capacitors and the Hybrid/CODEC ground should be connected directly to this pin. This AC GND pin should be connected directly to the DC GND pin.
11	TIP SENSE	Input to TIP SENSE (TS) amplifier. This pin should be connected through a resistor to the TIP side of the active load (Functional Diagram). The separation of TIP DRIVE and TIP SENSE allows the use of a low-cost protective RC network (RP1-RP4 in Functional Diagram).
12	TIP DRIVE	Output of the TIP DRIVE (DR) amplifier. A protective resistor should go between this and the TIP side of the active load (Functional Diagram).
13 14 15	V− V− V−	See description for pins 4 through 6.
16	VAC OUT	Low impedance output of an op-amp (Functional Diagram). A differential TIP-RING signal input is converted to a single-ended output and is referenced to ground. This ac signal is −0.5 times the ac voltage from TIP-TO-RING. The dc bias on this pin is −3 volts. This pin requires a dc blocking capacitor.
17	VDC OUT	This pin is an output from a loop length compensation path. A by-pass capacitor must be connected from this pin to signal ground so that a "dc only" signal is present in the loop-length compensation path. The voltage on this pin is directly proportional to the loop length (approximately −0.05 of the dc voltage from Tip-to-Ring). This pin could be used to control optional loop-length functions.
18	IAC IN	This is the input for the TIP-RING drive currents. It has very low ac input impedance. The TIP-RING output currents are 100 times this input current. It requires a dc blocking capacitor. The dc bias on this pin is −1.35 volts. The maximum ac signal input is 40 μAmps. This produces a signal level of approximately +7 dBm in a 600 Ω loop, without causing signal clipping.

Electrical Characteristics ($V- = -53V$ and $T_A = 25°C$ unless otherwise specified)

The characteristics shown below are expressed in circuit functional terms. They are insured as the result of production testing measurements shown in the test description table which follows this table.

Characteristics and Conditions	Min	Max	Unit
Power Supply Current, OFF-HOOK (V− = −53 to −60 V), (Loop = 275Ω)	43	49.5	mA
Power Supply Current, ON-HOOK (V− = −48 V), (Loop = Open Circuit)	0.2	3.5	mA
Ringing Current Capability, RING Lead Open	100	—	mA
TIP Current for Power Gate Threshold	3.0	8.0	mA
Loop Current for Hook Status Threshold (Loop = 500 Ω)	11	16	mA
Loop Current: 150 Ω 500 Ω 800 Ω 1300 Ω	38.3 38.5 30.5 19.0	41.3 41.5 34.5 23.0	mA mA mA mA
Transmit Loop Current Gain, Iac IN to TIP-RING	95.5	101	—
Receive Voltage Gain, TIP-RING to VAC OUT	0.476	0.506	—
Longitudinal Balance (ac) (Common-Mode Current < 10 mA)	60	—	dB

Electrical Characteristics
(Continued)

Characteristics and Conditions	Min	Max	Unit
Power-Supply Rejection: (Loop = 400 Ω)	52	—	dB
Noise Voltage, TIP/RING: (Loop = 500 Ω)	—	8.0	dBrnc
IAC IN, Input Resistance	—	100	Ω
VAC OUT, Output Resistance: (2.0 kΩ between VAC OUT & GND)	—	50	Ω
Longitudinal Resistance	50	100	Ω
TIP-TO-RING Shunt Resistance: (△Loop = 150 Ω − 400 Ω)	30	—	KΩ
Input Current Capability of "IAC IN" without Clipping	—	100	μAp-p
Output Voltage Capability of "VAC OUT" without Clipping	—	2.0	Vp-p

Test Descriptions
(At V− = − 53 V and T_A = 25°C unless otherwise specified)

Characteristic	Test Condition	Min	Max	Unit
TIP-RING Voltage Balance, △V(B-G)	Figure 3; Measure V(B,G) @ R(Load) = 400 Ω and R(Load = 275 Ω. Let △V(B,G) = the difference of these two measurements	—	±75	mV
Power-Supply Current	Figure 4; R(Loop) = 275 Ω, Measure V− Current	−43	−49.5	mA
Power-Supply Current, Maximum Voltage	Figure 4; R(Loop) = 275 Ω Measure V− Current, V− = − 60 V	−43	−49.5	mA
ON-HOOK Power-Supply Current	Figure 2; Measure V− Current	−0.2	−3.5	mA
$\frac{V_{TIP} + V_{RING}}{2}$	Figure 3; R(Loop) = 400 Ω Measure V(B,G)	−26.2	−28.3	V
Common-Mode Voltage	Figure 3; R(Loop) = 400 Ω, Measure VCM	−26.2	−28.3	V
Longitudinal Loop Error	Figure 3; [V(B,G)] − [VCM]	−	±1.0	V
Input Voltage	Figure 5; Measure V(A,GND) Open V− Power-Supply Lead	390	470	mV
Bandgap Voltage	Figure 6; Measure V(A, System GND), V(CM) = 26.5 V	−1.20	−1.48	V
TIP-RING Voltage	Figure 6; Measure V(T-R) R(Load) = 150 Ω, V(CM) = 26.5 V	5.75	6.20	V
VAC OUT, dc Level	Figure 6; Measure V(16, System GND); V(CM) = −26.5 V R(Load) = 150 Ω R(Load) = 500 Ω	 −2.0 −2.0	 −4.0 −4.0	 V V
△VAC OUT, dc Level	150 Ω meas. − 500 Ω meas.	−	±0.4	V
VAC OUT Voltage, Power Gate OFF Power Gate ON	Figure 7; Measure V(AC) I(TIP) = 3 mA I(TIP) = 8 mA	 − −2.0	 −1.0 −5.0	 V V
HOOK STATUS, OFF Voltage ON Voltage	Figure 8; Measure V(HS) Set I(ADJ) so that I(L) = 11 mA Set I(ADJ) so that I(L) = 16 mA	 4.0 −	 5.0 ±0.2	 V V

Test Descriptions (Continued)

Characteristic	Test Condition	Min	Max	Unit
Current Gain, IAC IN to I(Loop)	Figure 9; Measure V(T-R) @ I(A) = +50 μA and @ I(A) = −50 μA. Gain = $\frac{\triangle V(T\text{-}R)/500\ \Omega}{100\ \mu A}$	95.5	101	dB
Voltage Gain, V(T-R) to V(AC)	Figure 9; Measure V(T-R) and V(AC) @ I(A) = −50 μA and I(A) = +50 μA. Gain = △V(AC)/△V(T-R)	0.476	0.505	—
Longitudinal Balance (dc), △V(TIP-to-RING)	Figure 9; Measure V(T-R) @ I(D) = +10 mA, I(D) = −10 mA	—	±25	mV
Loop Current	Figure 4; Measure I(Loop) R(Loop) = 500 Ω R(Loop) = 800 Ω R(Loop) = 1300 Ω	 38.5 30.5 19.0	 41.4 34.5 23.0	 mA mA mA
IAC Input Resistance, △V(IAC)	Figure 10; Measure V(IAC) @ I(A) = −50 μA, I(A) = +50 μA	—	±10	mV
TIP-RING Current Capability	Figure 11; Measure V(T-G) I(TIP) = 100 mA for 0.5 s.	−12.0	−15.0	V
TIP-RING Voltage, Loop-Shunt Impedance) △V(T-G)	Figure 12; Measure V(T-G) @ R(LOAD) = 150 Ω and @ R(LOAD) = 400 Ω	—	±20	mV
AC OUT Source Impedance	Figure 13; Measure V(VAC) @ R(VAC) = open and @ R(VAC) = 2000 Ω Impedance = $\frac{2000\ [V(open) - V(2000\ \Omega)]}{V(2000\ \Omega)}$	—	50	Ω
Power-Supply Rejection, △V(T-G)	Figure 6; Measure V(T-G) @ V− = −53 V, V(CM) = −26.5 V and @ V− = −45 V, V(CM) = 22.5 V R(LOAD) = 400 Ω	—	±20	mV
Longitudinal Resistance, △V(T-G)	Figure 14; Measure V(T-G) @ I(D) = +10 mA, I(D) = −10 mA	—	±20	mV
Noise, Short Loop Long Loop	Figure 15; Measure V(NOISE) R(Loop) = 500 Ω R(Loop) = 1000 Ω	 — —	 8.0 25.0	 dBrnc dBrnc

Test Circuits

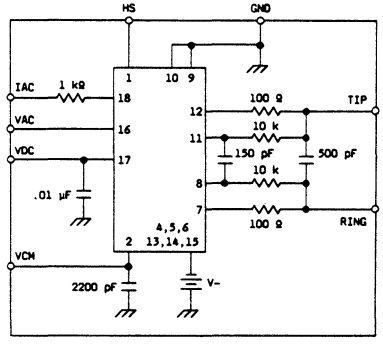


Figure 2. Basic Test Circuit

Test Circuits
(Continued)

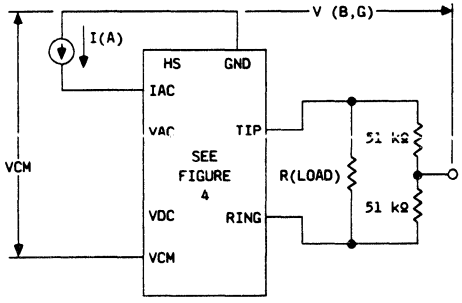


Figure 3. Test Circuit

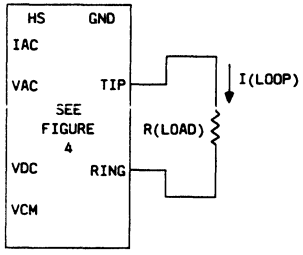


Figure 4. Test Circuit

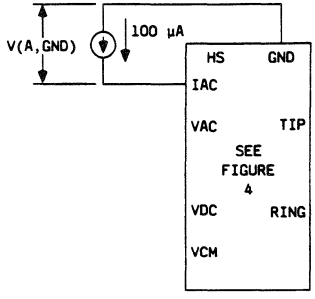


Figure 5. Test Circuit

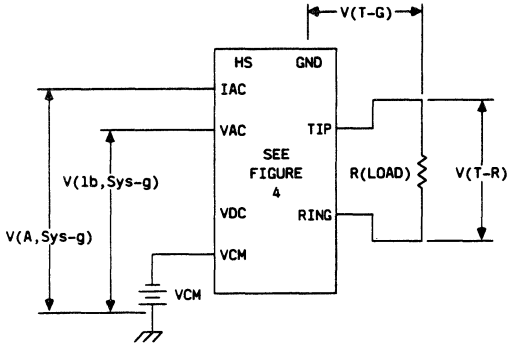


Figure 6. Test Circuit

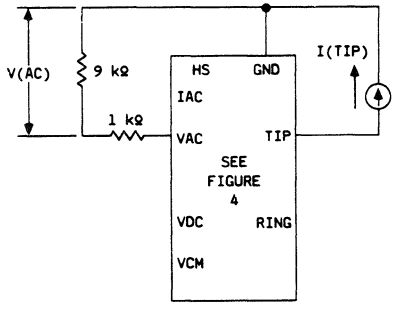


Figure 7. Test Circuit

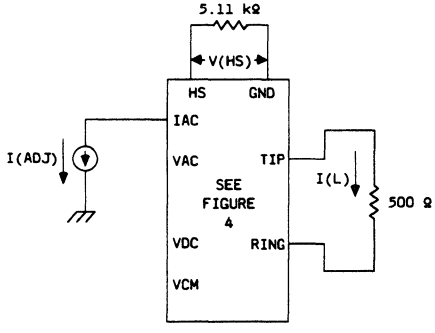


Figure 8. Test Circuit

Test Circuits
(Continued)

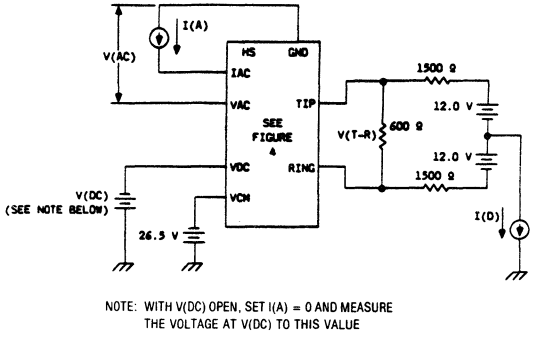


Figure 9. Test Circuit

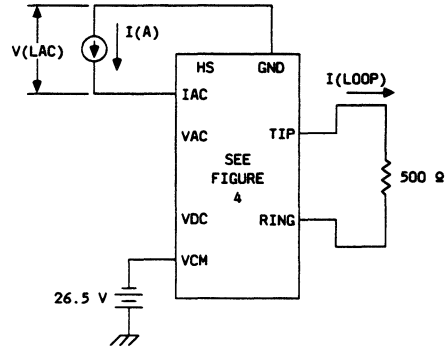


Figure 10. Test Circuit

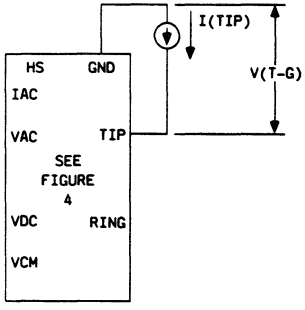


Figure 11. Test Circuit

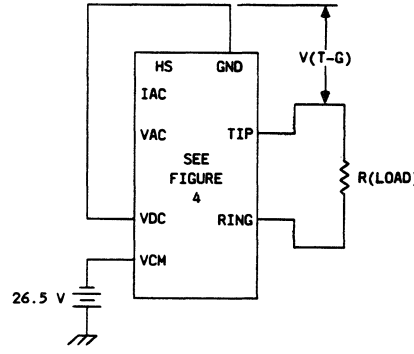


Figure 12. Test Circuit

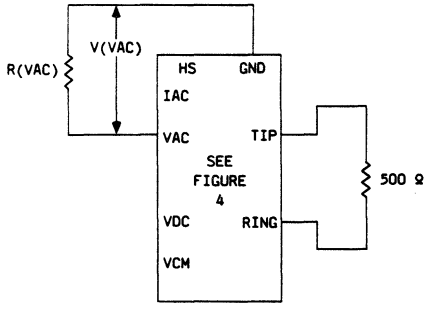


Figure 13. Test Circuit

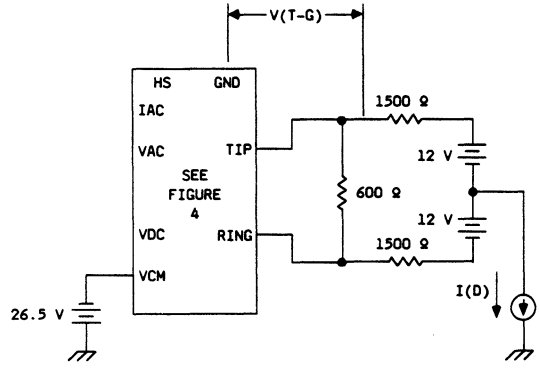


Figure 14. Test Circuit

Test Circuits (Continued)

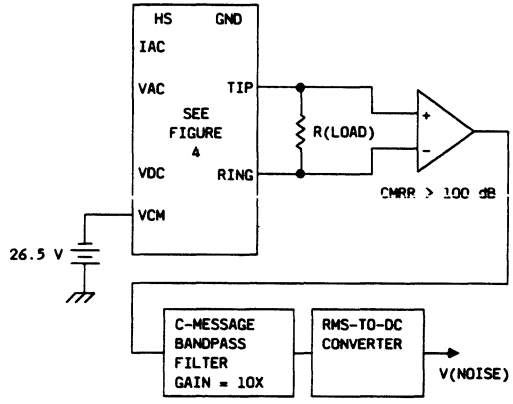


Figure 15. Test Circuit

Characteristics

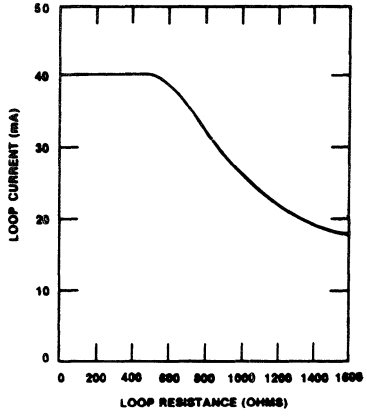


Figure 16.
Typical Loop Current vs Loop Resistance

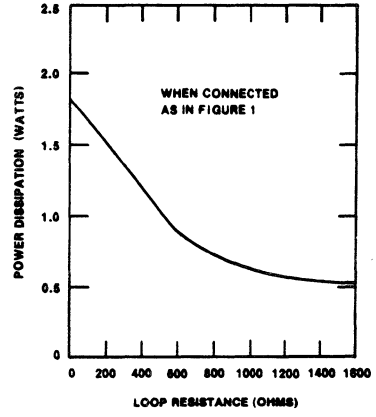


Figure 17.
Typical Power Dissipation vs Loop Resistance

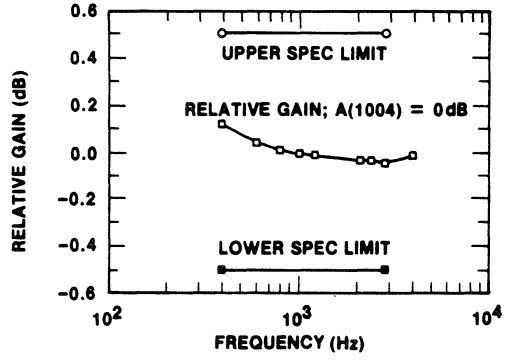


Figure 18(a). LB1012AA/AD Typical Gain vs Frequency Response

Characteristic Curves
(Continued)

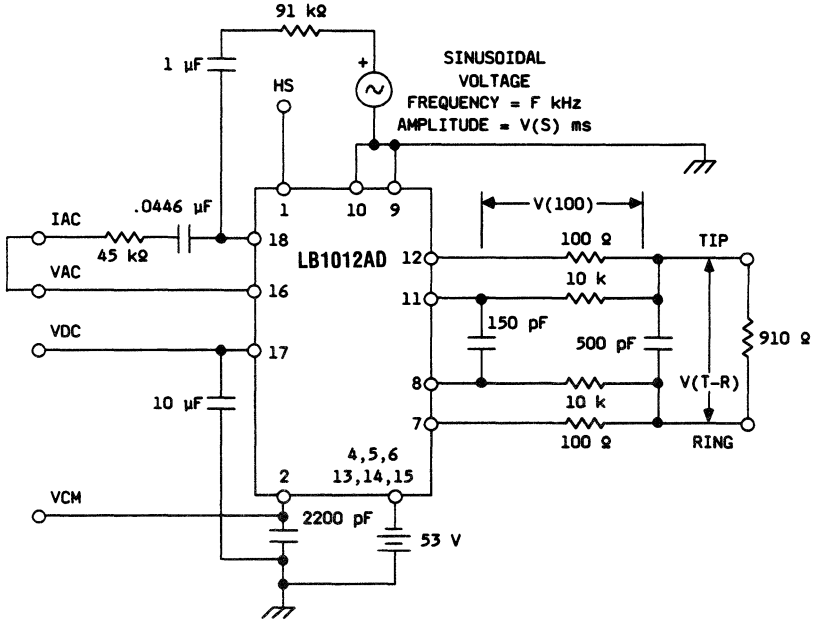


Figure 18(b). Frequency Response Test Circuit

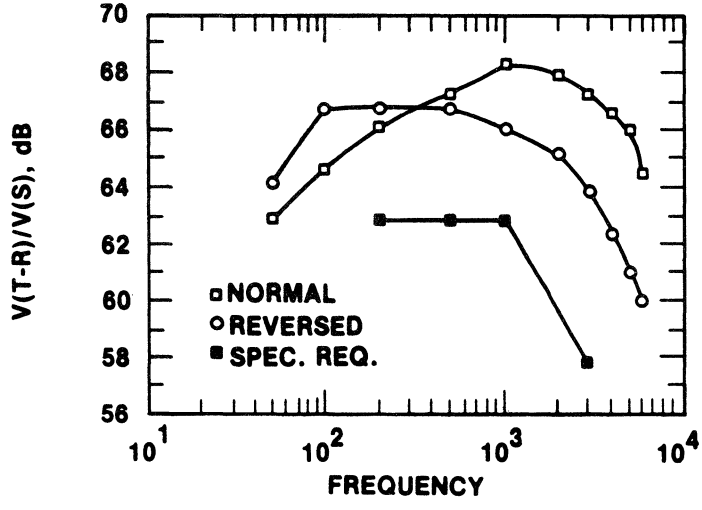


Figure 19(a). LB1012AA/AD Typical Longitudinal Balance vs Frequency

Characteristic Curves
(Continued)

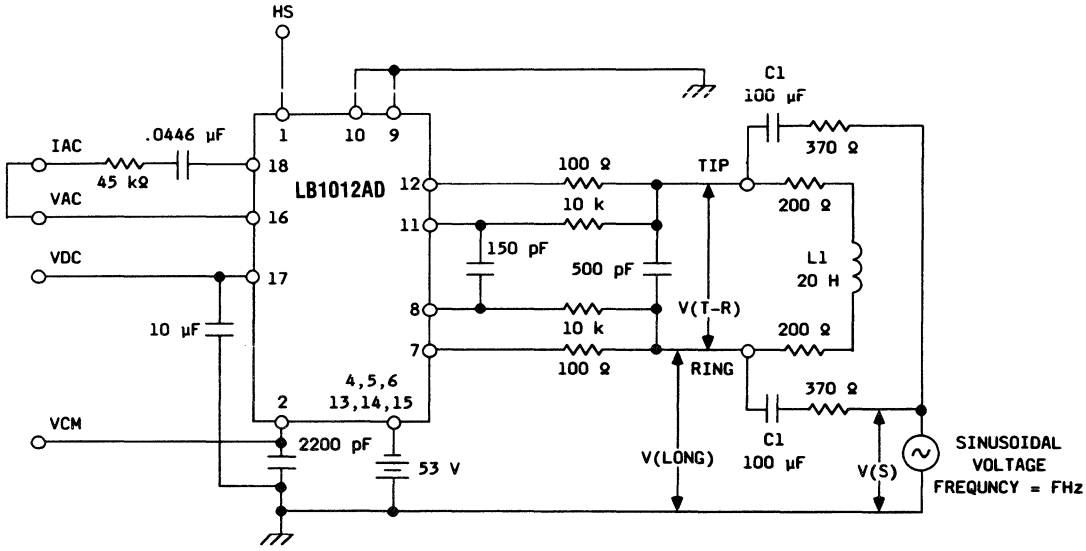


Figure 19(b). Longitudinal Balance Test Circuit

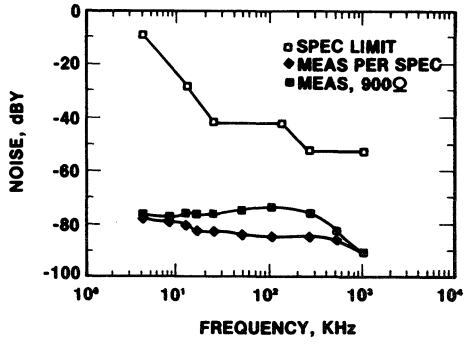


Figure 20(a). Typical. Metallic Out-of-Band Noise

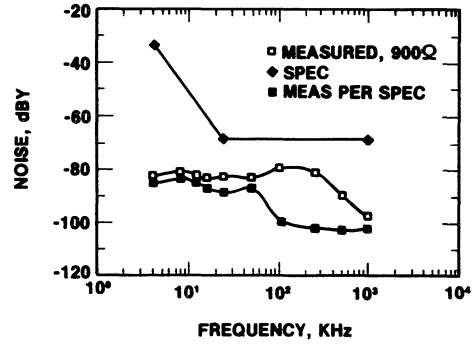


Figure 20(b). Typical Longitudinal Out-of-Band Noise

Characteristic Curves
(Continued)

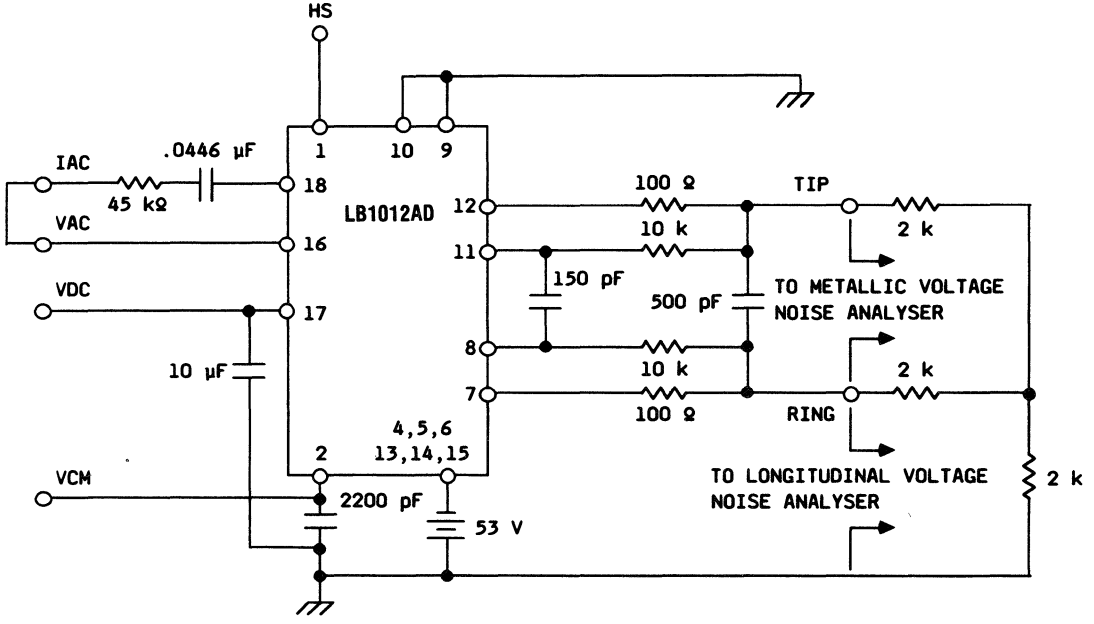


Figure 20(c). LB1012AD Noise Test Circuit

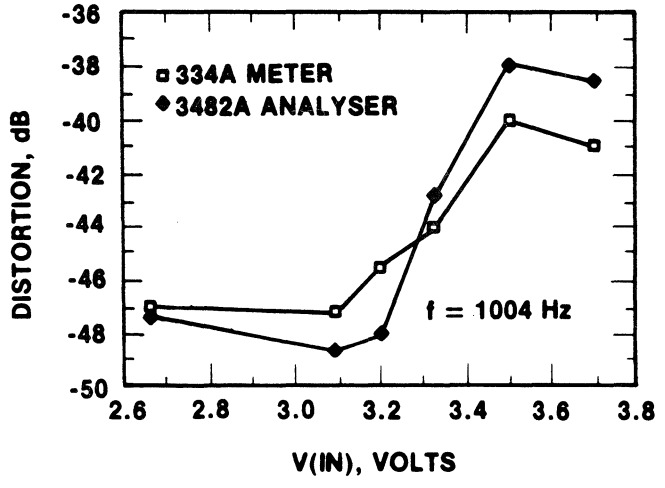


Figure 21(a). Typical Distortion vs Input Characteristics

Characteristic Curves

(Continued)

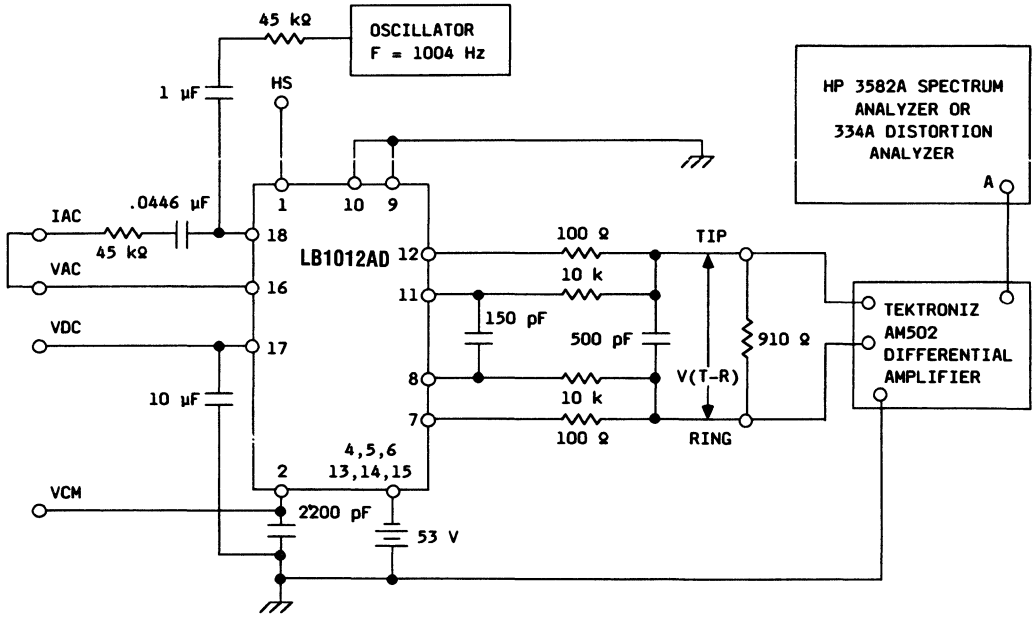


Figure 21(b). LB1012AD Distortion Test Circuit

Table 1

Temperature coefficients of LB1012AD Battery Feed Circuit measured at low temperature (−25°C) and high temperature (+100°C). Supply voltage range: −43 to −60 V

Test	Specification			Variation: % of Spec Range/°C	
Name	Min	Max	Units	−25°C to +25°C	+25°C to +100°C
Offhook Supply Current	43	49.5	mA	−.04%	−.03%
Onhook Supply Current	−0.2	−3.5	mA	−.13%	−.12%
Longitudinal Loop Error	—	±1	V	+.02%	<.001%
IAC to T-R Current Gain	95.5	101	—	−.14%	−.21%
T-R to VAC Gain	−.476	−.505	—	−.21%	−.18%
Long to Met Balance	—	±25	mV	<.001%	<.001%
500 Ω Loop Current	38.5	41.5	mA	−.1%	−.3%
800 Ω Loop Current	30.5	34.5	mA	−.02%	−.13%
1300 Ω Loop Current	19	23	mA	<.001%	−.07%
Power Supply Rejection	—	±25	mV	<.001%	<.001%
Long. Res., △I = 20 mA	1.0	2.0	V	−.32%	.37%

Functional Description

(Functional Diagram and Figure 22)

The LB1012AD Battery Feed device supplies a controlled dc current from its own external V− power supply to a customer loop Tip-Ring pair (40 mA on loops up to approximately 600 ohms, decreasing to approximately 21 mA for 1300-ohm loops). Two precisely trimmed audio interface ports are provided: IAC IN with a current gain of 100 to the Tip-Ring pair and the TIP SENSE to RING SENSE input with a voltage gain of −0.50 to VAC OUT.

These gains make it possible to control loop termination with impedances scaled 50:1 (30 k ohms connected between VAC OUT and IAC IN look like 600 ohms across TIP-to-RING, Figure 22). A common-mode cancellation feature provides 75-ohm loading for common-mode TIP-RING current with peak values less than loop current.

The LB1012AD features very good "common-mode to differential" signal rejection (and vice-versa), high TIP-to-RING termination impedance, and very good power-supply noise rejection. Internal thermal-shutdown circuitry protects against overload currents. Lightning-surge protection is achieved with external diodes and resistors (see Applications). The power gating circuitry is designed to minimize on-hook current drain. When Tip current falls below a nominal value of 5.0 mA (3.0 mA to 8.0 mA), the circuit goes into the "power down" mode. The signal path is broken in this "power down" mode, and only a dc current is supplied by Tip and Ring for off-hook sensing. The TIP DRIVE output provides ringing current capability for those times when the RING DRIVE output is open-circuited. Both TIP DRIVE and RING DRIVE are clamped to their respective power supplies while the telephone set is on-hook.

The LB1012AD is designed for use with supply voltages of +5.0 V, ground, and a negative voltage supply (V−). The device is tested at V− values of both −42 V and −60 V, but can work at voltages as small as −30 V (if loop resistance is low enough to prevent signal clipping).

Applications

Each LB1012AA/AD Battery Feed integrated circuit feeds an individual customer loop. It moderates the flow of dc current from its external V− power supply to the loop system. Simultaneous to supplying the dc current, it serves as a signal path between the hybrid (input/output in the Central Office) and the customer loop system (input/output to a telephone set). The LB1012AA/AD must respond to ringing signals and to off-hook conditions. Morever, since the battery-feed circuit must work in a potentially harsh environment (due to power line crossing and lightning surges), there must be some protective provisions for the possibility of overvoltage.

Figure 22 shows a method for correctly connecting the LB1012AD device to the TIP and RING connections of a telephone loop system. Careful grounding procedures will assure good common-mode and power-supply noise rejection characteristics. The AC GND pin should be connected directly to the DC GND pin, and all bypass capacitors should be connected directly to the signal ground (AC GND).

The RC network (RS1 and RS2) should be placed between TIP DRIVE and RING DRIVE, and a capacitor (CS2) should be placed between TIP SENSE and RING SENSE. This assures stable operation under widely varying conditions.

An external network of four resistors (RP1-RP4) and four surge-protection diodes (D1-D4) are required to protect the LB1012AD device against electrical transients, including lightning surges. The four diodes connected between TIP, RING, system ground, and V− must be able to withstand secondary lightning surges (15 amps peak, 10 μs risetime, 1000 μs decay to half-peak amplitude).

For a detailed explanation of the resistor on the HOOK STATUS pin and the capacitors on IAC IN, VAC OUT, VDC OUT, and VREF, refer to the respective PIN or pad description section.

Applications
(Continued)

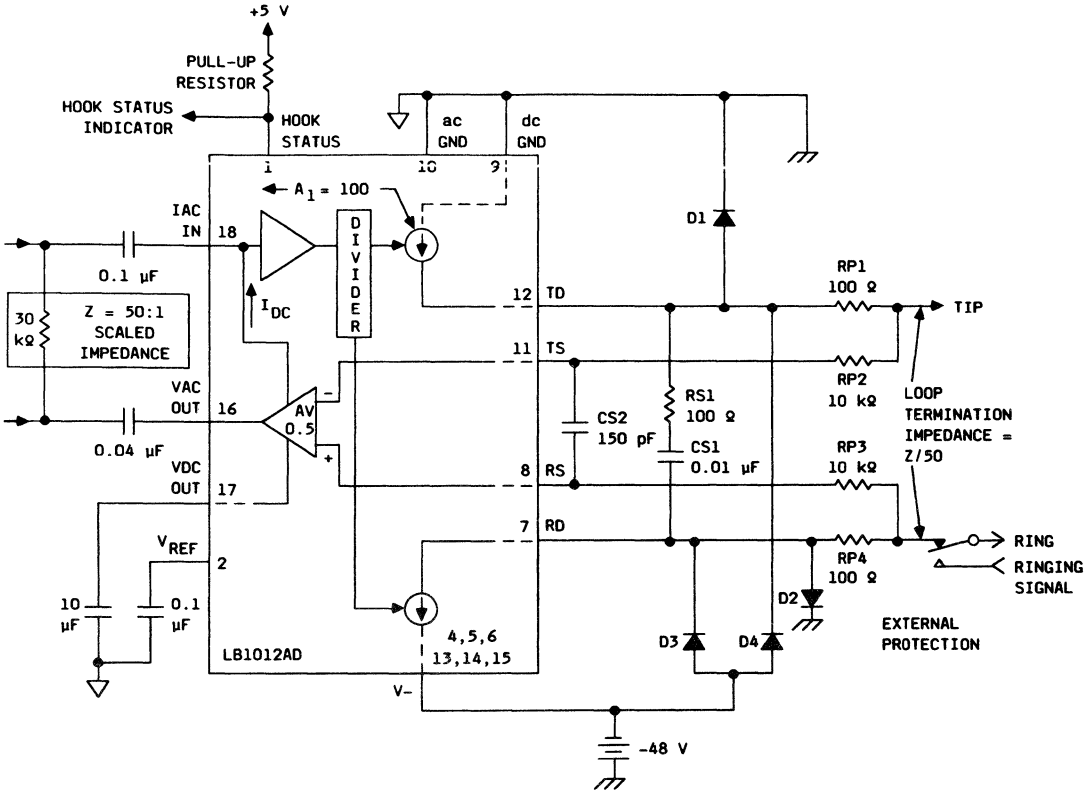
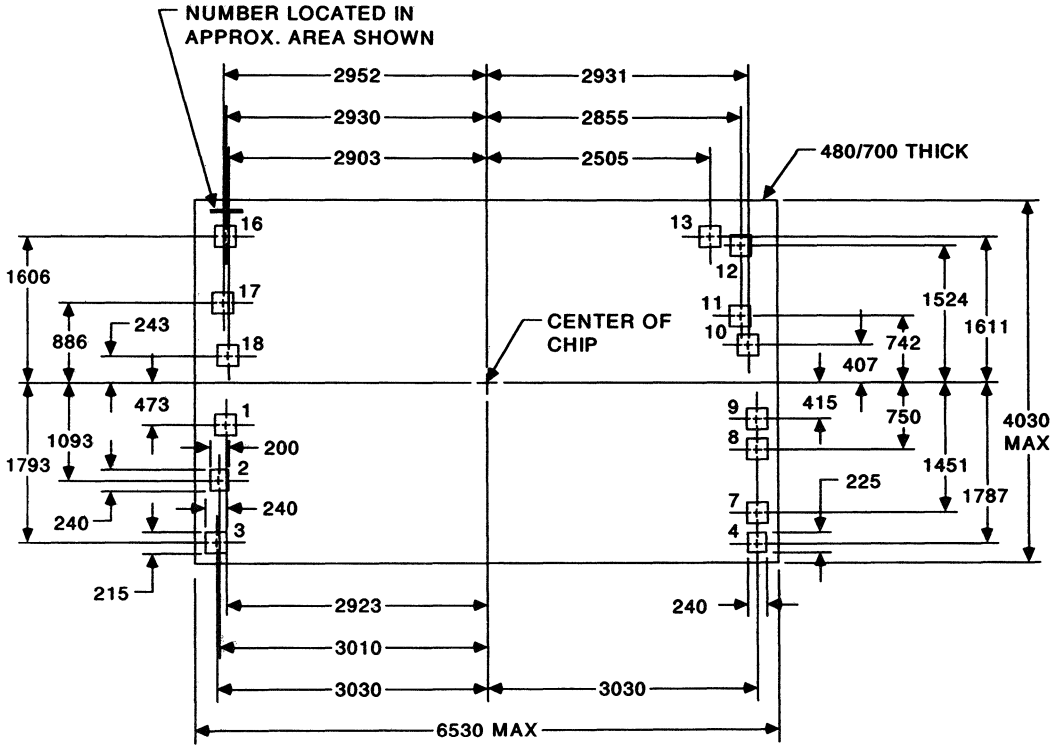


Figure 22. LB1012AD Battery Feed Application Diagram

Outline Drawings

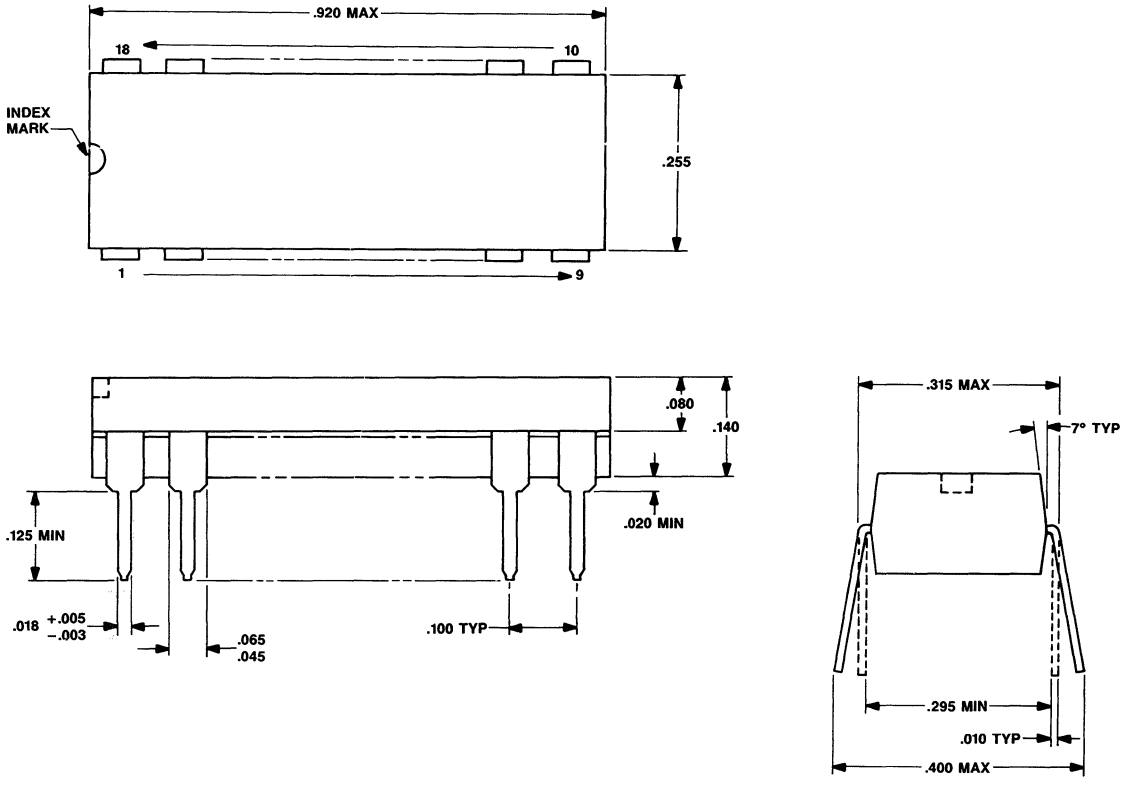
LB1012AA

(Dimensions in Microns)



Note: Bonding pad numbers are for reference only. Bonding pads are 240 microns square, except where dimensioned otherwise.

Outline Drawing
LB1012AD
(Dimensions in Inches)



Note: Pin numbers are for reference only

Ordering Information

Device	Comcode
LB1012AA	104381033
LB1012AD	104208822

HIGH-GAIN COMPARATOR LS1112AC

Description

The LS1112AC device is a high-gain, flexible comparator featuring an output voltage gain of 100k. The circuit is equivalent to an operational amplifier with a TTL output stage and a differential input, and therefore is compatible with TTL, DTL, and RTL logics.

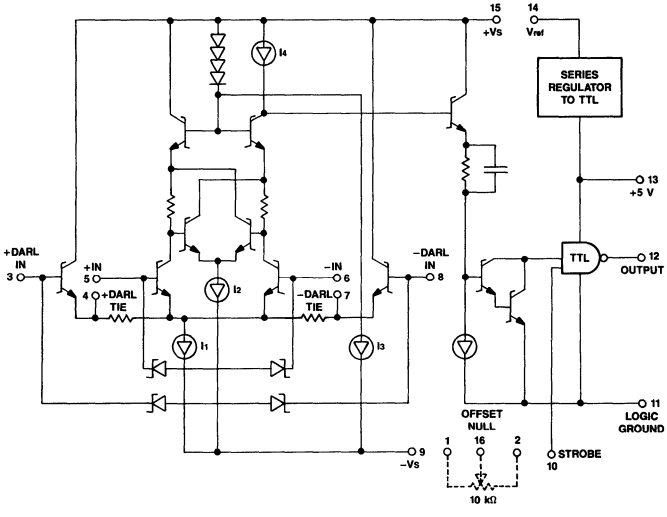
The device offers a number of user options, including Darlington inputs, offset nulling, strobing, and an internal series regulator for the TTL output stage. Applications include peak and zero-crossing detectors, switching power amplifiers, A/D converters, clock generators, multivibrators, logic interface, logic gates, line receivers, and hysteresis elements.

The high-gain comparator is designed for operation using a positive power supply range of 5.0 to 15 V and a negative power supply range of 0 to − 15 V. For positive voltages less than 9 V, + 5.0 V must be supplied for the TTL output. The LS1112AC High-Gain Comparator is packaged in a 16-pin plastic DIP.

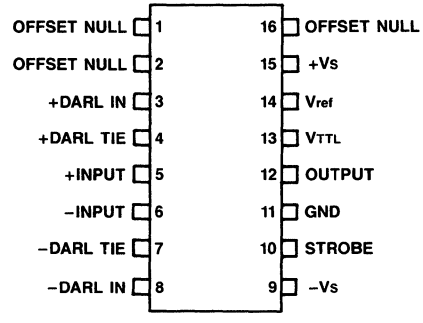
Features

- Multiple applications
- TTL, DTL, RTL logic compatible
- Single power supply operation available
- 100 ns switching
- Typical output voltage gain of 100 k
- 10 mV input threshold without offset null
- Strobed output

Functional Diagram



Pin Diagram



Maximum Ratings

Parameter	Rating	Unit
Supply Voltage:		
Pins 15, 9	30	Vdc
Pins 14, 11	15	Vdc
Pins 13, 11	7.0	Vdc
Input Current: Pins 3, 5, 6, 8	10	mA dc
Power Dissipation	400	mW
Storage Temperature Range	−65 to +175	°C
Operating Temperature Range	0 to +60	°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions

Pin	Name/Function	Pin	Name/Function
1	OFFSET NULL	9	−Vs
2	OFFSET NULL	10	STROBE
3	+ DARLINGTON INPUT	11	GND
4	+ DARLINGTON TIE	12	OUTPUT
5	+ INPUT	13	V_{TTL}
6	− INPUT	14	V_{ref}
7	− DARLINGTON TIE	15	+Vs
8	− DARLINGTON INPUT	16	OFFSET NULL

Electrical Characteristics*

(T_A = 25°C, V_S = ±15 V unless otherwise specified)

Characteristic and Conditions		Symbol	Min	Max	Unit
Positive Supply Current**		$I_{(15)}$	5.0	10	mA
Negative Supply Current**		$I_{(9)}$	−3.5	−7.0	
Logic Supply Current**	$V_{(14,11)}$ = 15 V	$I_{(14)}$	2.5	5.5	
	$V_{(13,11)}$ = 5.5 V	$I_{(13)}$	1.5	3.5	
Strobe input Current	$V_{(10,11)}$ = 0	$I_{(10)}$	−0.6	−1.8	
Stobe Leakage Current	$V_{(10,11)}$ = 2.4 V		−2.0	20	μA
Output Voltage High	$V_{(10,11)}$ = 2.4 V, $I_{(12)}$ = −0.2 mA†	V_{OH}	3.0	5.3	V
	$V_{(10,11)}$ = 0.8 V, $I_{(12)}$ = −4.0 mA††		2.5	5.0	
Output Voltage Low	$V_{(10,11)}$ = 1.8 V, $I_{(12)}$ = −7.0 mA**	V_{OL}	100	370	mV
Input Bias Current	Common-Mode Voltage = 0	I_{IB}	—	40	μA
Input Offset Current		I_{IO}	—	±4.0	
Input Offset Voltage (Nullable)		V_{IO}	—	±4.5	mV
Common-Mode Voltage Range	ΔV_{IO} = 2.0 mV, V_S = ±13.2 V	+CMVR	8.7	—	V
		−CMVR	−8.0	—	
Input Bias Current	Darlington Input − Common-Mode Voltage = 0	I_{IB}	—	−2.5	μA
Input Offset Current		I_{IO}	—	±0.25	
Input Offset Voltage		V_{IO}	—	±7.5	mV
Common-Mode Voltage Range	Darlington Input ΔV_{IO} = 2.0 mV, V_S = ±13.2 V	CMVR	−7.3	9.4	V
Voltage Gain		A_V	10k	—	V/V
Typical Propagation Delay Time	$V_{(13,11)}$ = 5.0 V, V_S = ±12 V	t_{PLH}	110	—	ns
		t_{PHL}	95	—	
Typical Differential Input Voltage For Switching††		V_{ID}	≤10	—	mV

* Threshold voltage should be set at 1.4 V when using supply voltages of 5.0 V and 0 V.
** $V_{(5,6)}$ = −100 mV.
† $V_{(5,6)}$ = 100 mV.
†† Includes Input Offset Voltage (Nullable) effects.

Timing Characteristics

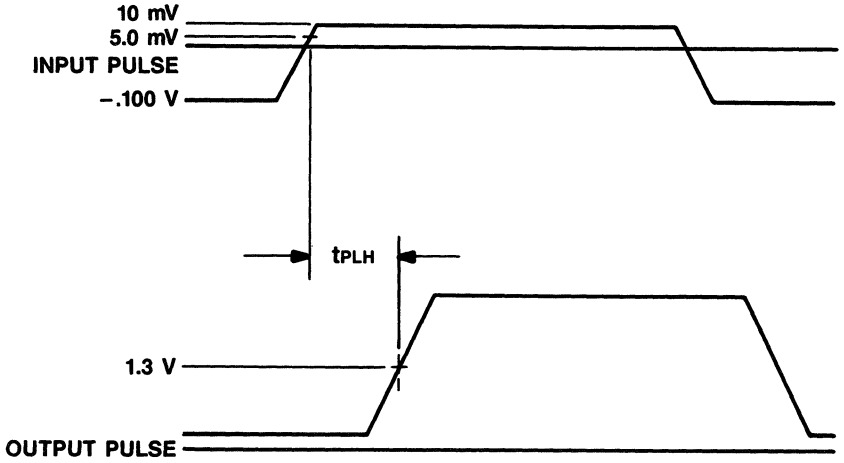


Figure 1. Positive Input and Output Waveforms

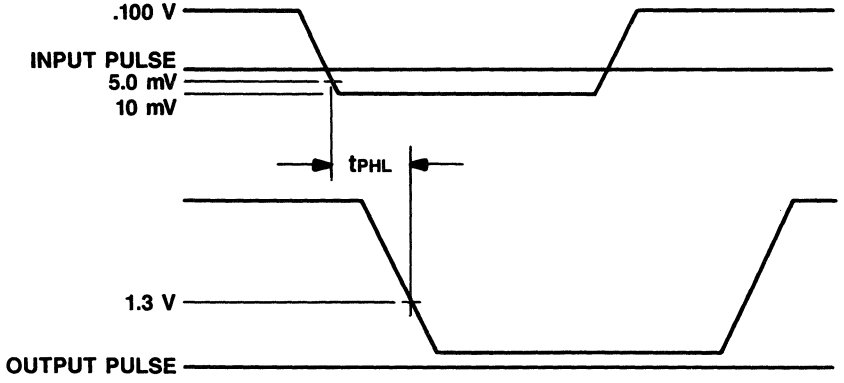


Figure 2. Negative Input and Output Waveforms

Test Circuits

Resistor values selected for use in all test circuits are characterized by a nominal ± 1% tolerance; capacitors ± 10%.

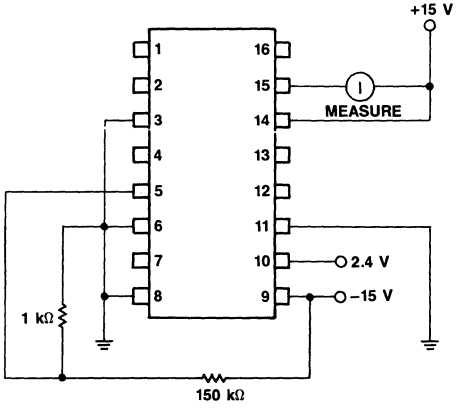


Figure 3. Positive Supply Current (I_{15})

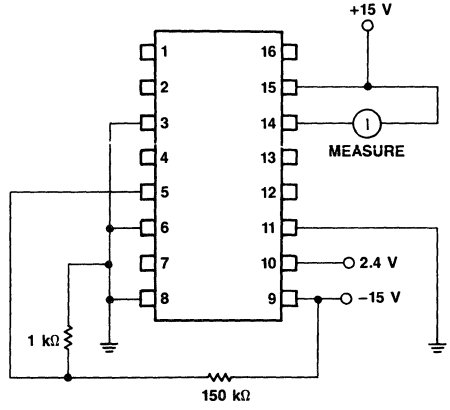


Figure 4. Logic Supply Current (I_{14})

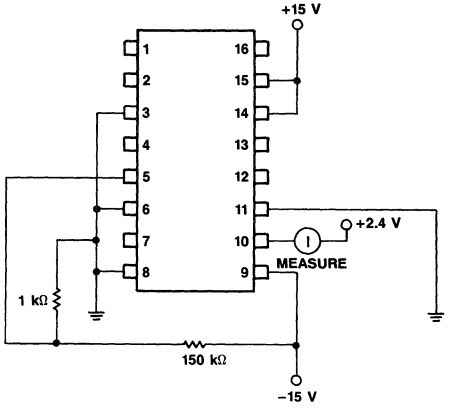


Figure 5. Strobe Leakage Current (I_{10})

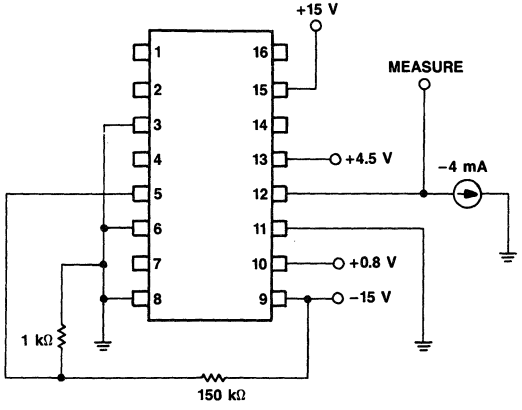


Figure 6. High-Voltage Output (V_{OH}), ($I_{12} = -4$ mA)

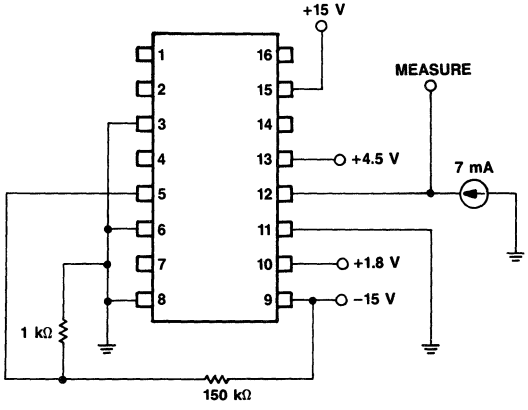


Figure 7. Low-Voltage Output (V_{OL}), ($I_{12} = -7$ mA)

Characteristic Curves

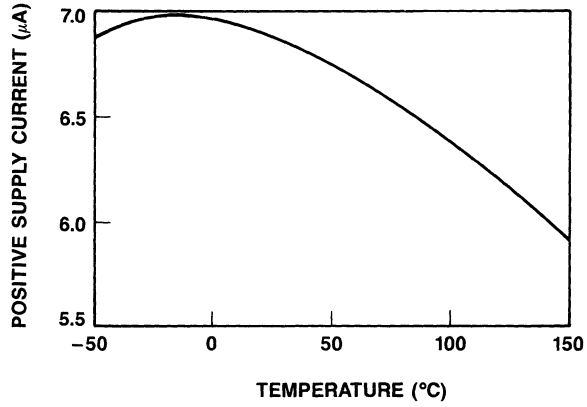


Figure 8. Typical Positive Supply Current vs. Temperature

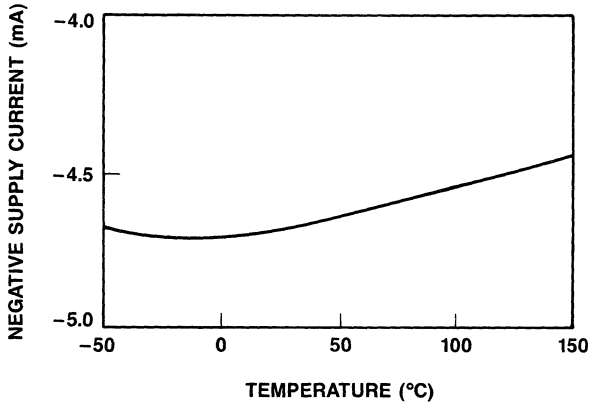


Figure 9. Typical Negative Supply Current vs. Temperature

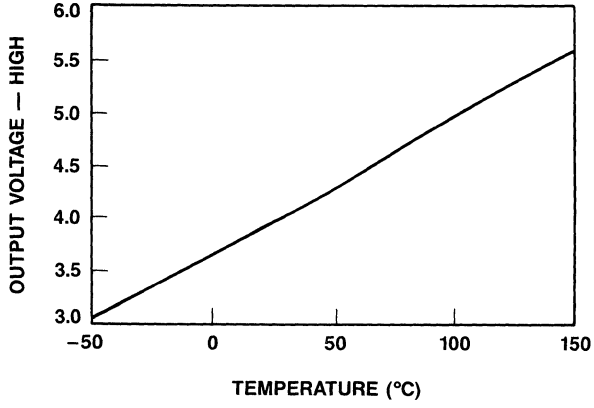


Figure 10. Typical High-Level Output Voltage vs. Temperature

Characteristic Curves
(Continued)

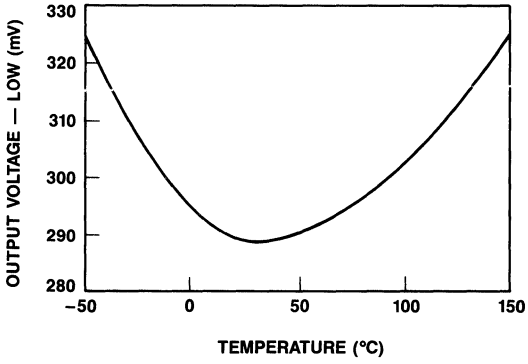


Figure 11. Typical Low-Level Output Voltage vs. Temperature

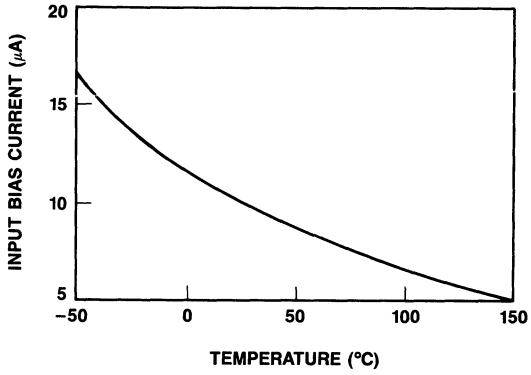


Figure 12. Typical Input Bias Current vs. Temperature

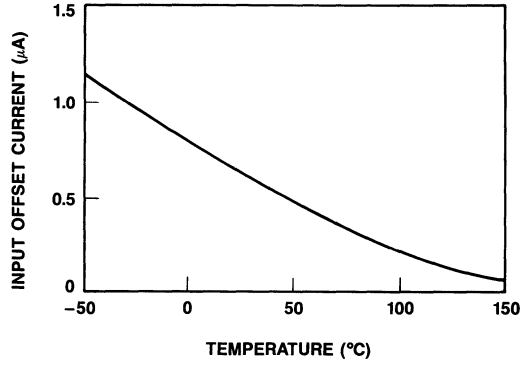


Figure 13. Typical Input Offset Current vs. Temperature

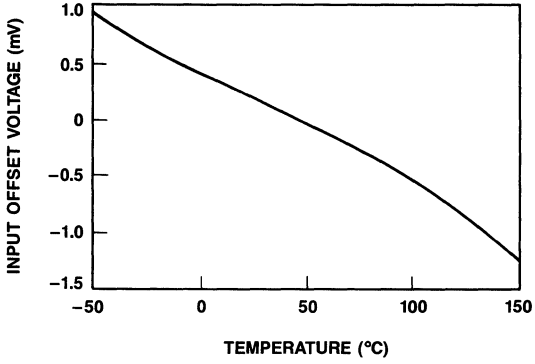


Figure 14. Typical Input Offset Voltage vs. Temperature

Characteristic Curves
(Continued)

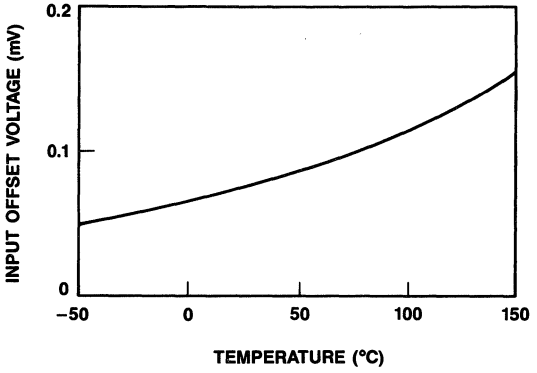


Figure 15. Typical Common-Mode Voltage Range vs. Temperature

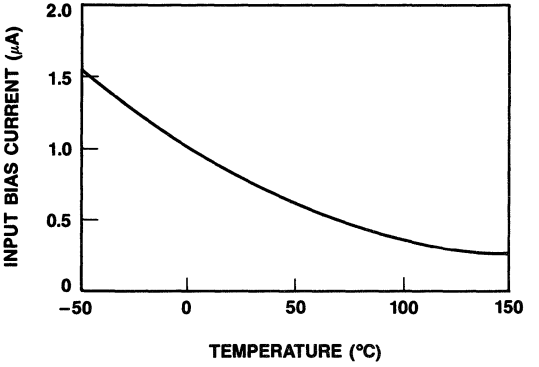


Figure 16. Typical Darlington Input Bias Current vs. Temperature

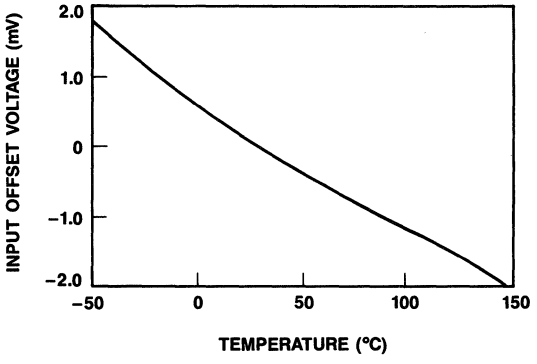


Figure 17. Typical Darlington Input Offset Voltage vs. Temperature

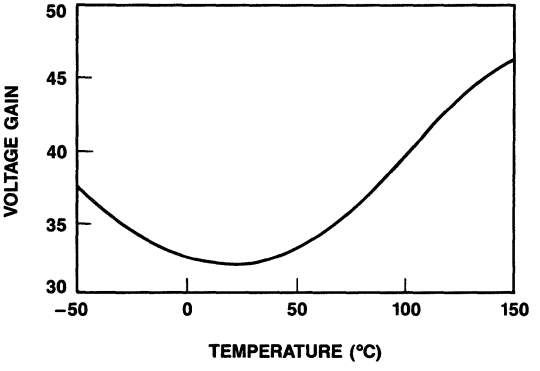


Figure 18. Typical Voltage Gain vs. Temperature

Applications

The following diagrams show the connections for the various options available with the LS1112AC High-Gain Comparator.

- Figure 19 shows the required connections for the logic circuit operation.
- As shown in Figure 20, Darlington inputs are used by connecting lead 4 to 5 and lead 6 to 7, using leads 3 and 8 as the positive and negative inputs, respectively. This connection provides higher input impedance at the expense of additional input offset voltage.
- Figure 21 illustrates the use of internal logic reference. Lead 13 is not connected using this option. Positive supply voltages greater than 7.5 V are required.
- Offset nulling is illustrated in Figure 22. A 10 k ohm potentiometer is connected between leads 1 and 2 with the wiper arm connected to lead 16.

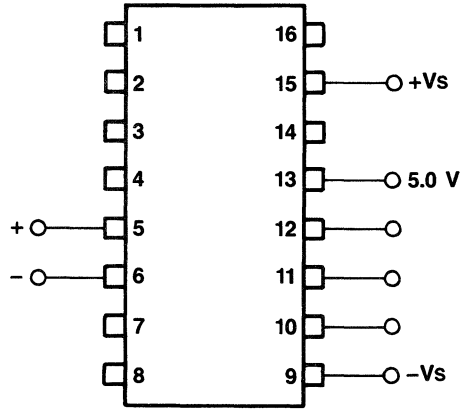


Figure 19. Logic Circuit Operation

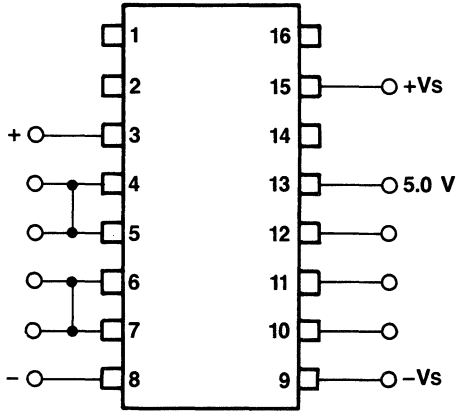


Figure 20. Darlington Inputs

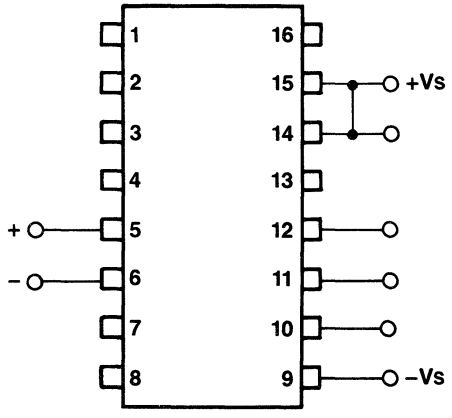


Figure 21. Internal Logic Reference

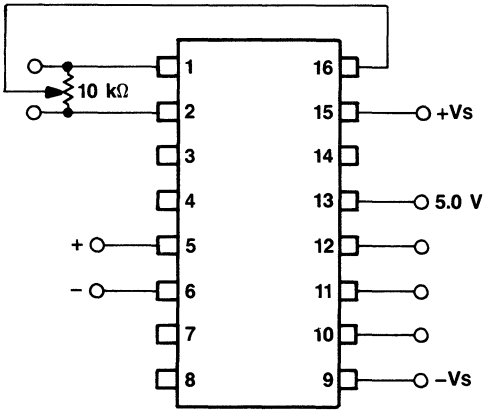
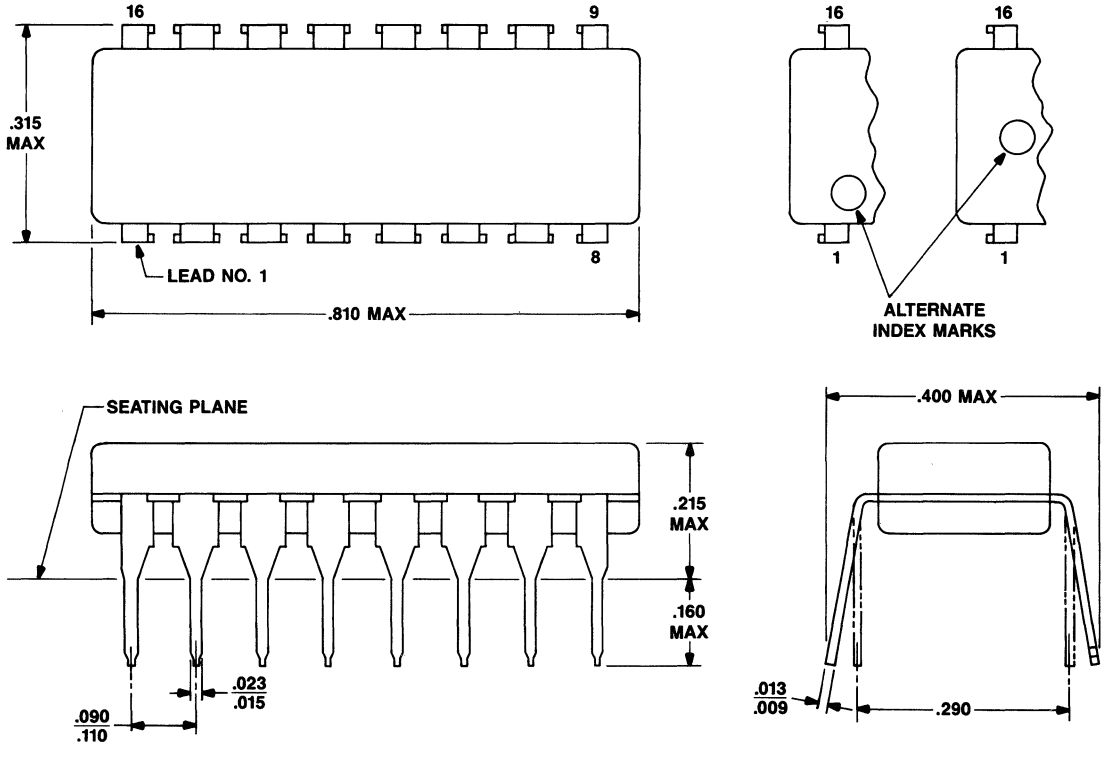


Figure 22. Offset Nulling

Outline Drawing

(Dimensions in Inches)



Ordering Information

Device	Comcode
LS1112AC	104411905

Description

The LS1113AC Time-Delay Comparator is a general-purpose timing circuit consisting of a comparator, constant-current source, threshold voltage generator, a detector comparator with a logic-level output, and three logic gates. Functionally, it serves as a single-shot adjustable delay comparator.

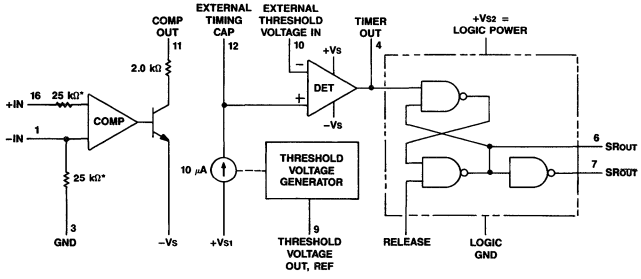
When used with the appropriate external components, the device is suitable in numerous general-purpose time-delay applications including peak- and zero-crossing detectors, switching power amplifiers, A/D converters, clock generators, multivibrators, logic interfaces, line receivers, and hysteresis elements.

The LS1113AC Time-Delay Comparator is available in a 16-pin plastic DIP.

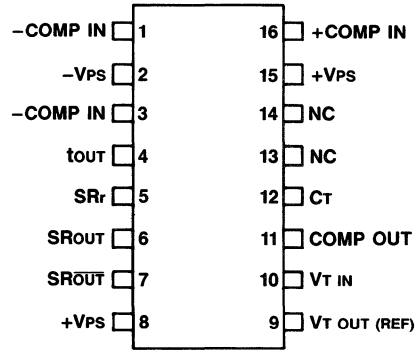
Features

- Complex timing functions single package
- Low power dissipation (100 mW, max.)
- Pre-trimmed, low input offset voltage comparator
- Operates from a ± 15 V power supply
- TTL-compatible logic output

Functional Diagram



Pin Diagram



Maximum Ratings*

Parameter	Rating	Unit
Supply Current (I_8, I_{15}, $-I_2$)	5.0	mA
Supply Voltage (V_{15}, V_3)	15	Vdc
Supply Voltage (V_2, V_3)	−15	Vdc
Power Dissipation**	100	mW
Operating Temperature Range	0 to 60	°C
Storage Temperature Range	−40 to +125	°C

* Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

** Derate at 1.0 mW/°C for temperature within the range of 25 to 125°C.

Pin Descriptions

Pin	Symbol	Name/Function
1	−COMP IN	Negative comparator input
2	$-V_{PS}$	Negative power supply
3	−COMP IN	Negative comparator input (through 25 kΩ)
4	t_{OUT}	Timer output
5	SR Reset	SR set/reset flip-flop
6	SR_{OUT}	Flip-flop output
7	$SR_{\overline{OUT}}$	Inverted flip-flop output
8	$+V_{PS}$	Positive power supply
9	V_T out (REF)	Threshold voltage output
10	$V_{T\ IN}$	External threshold voltage input
11	COMP OUT	Comparator output
12	C_T	External capacitor
13	NC	No connection
14	NC	No connection
15	$+V_{PS}$	Positive power supply
16	+COMP IN	Positive comparator input

Electrical Characteristics

(T_A = 25°C) ①

Characteristic and Conditions		Symbol	Min	Max	Unit
Comparator Section					
Positive Supply Current		$+I_{PS}$	—	3.0	mA
Negative Supply Current		$-I_{PS}$	—	−3.0	
Input Offset Voltage		V_{IO}	−3.5	+3.5	mV
Input Sensitivity②		Vin	10	—	
Charging Current③		$I_C(Q_{12})$	9.0	11.3	μA
Logic Section					
Logic Supply Current ④		I_{PSL}	—	4.0	mA
Output Voltages (Leads 9 & 10)	V_{IH} = 1.9 V, I_{OL} = 4.1 mA	V_{OL}	—	0.250	V
	V_{IL} = 1.1 V, I_{OH} = 20 μA	V_{OH}	5.35	—	
Input Forward Current	$V_{(5)}$ = 0⑤	I_{IL}	0.14	0.28	mA
	$V_{(4)}$ = 0⑥		0.48	0.89	
Input Leakage	$V_{I(5)}$ = 5.5 V⑦	I_{IH}	—	0.10	μA
Output Leakage (Lead 6)		I_{OH}	—	20	
Output Leakage (Lead 7)			—	7.0	
Output Leakage (Lead 4)			—	7.0	

Notes: ① These characteristics are guaranteed by appropriate specification limits at the following conditions: $+V_{S1}$ (lead 15) = +6.2 V. $-V_S$(lead 2) = −6.2 V. (Ground is lead 3.) Lead 10 shorted to lead 4 and lead 12 shorted to lead 11 except for $V_C(Q_{12})$ measurement.

② When the voltage on lead 16 exceeds the voltage on lead 2 by 10 mV (or more), lead 4 must be within 100 mV of $+V_{S2}$.

③ I_C of Q_{12} is trimmed to a value between 9.0 μA and 11.3 μA in accordance with the following equation:

$$I_C = \frac{+V_S + V_{CE(Q11)} - V_{REF}}{730\ k\Omega}$$

④ $+V_{S2}$ (lead 8) = +5.5 V.

⑤ Q29 is "OFF" so that only the input to Q30, which is attached to lead 5, is "LOW".

⑥ A large portion of this current is through R18.

⑦ Lead 5 is grounded to set logic and then taken to +5.5 V for leakage test.

Test Circuits

Resistor values selected for all test circuits are characterized by a nominal ±1% tolerance; capacitors, ±10%.

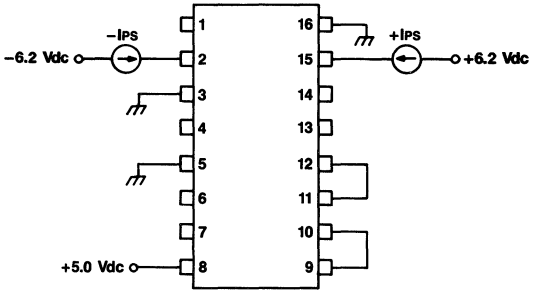


Figure 1. Positive/Negative Power Supply Current, Comparator Section

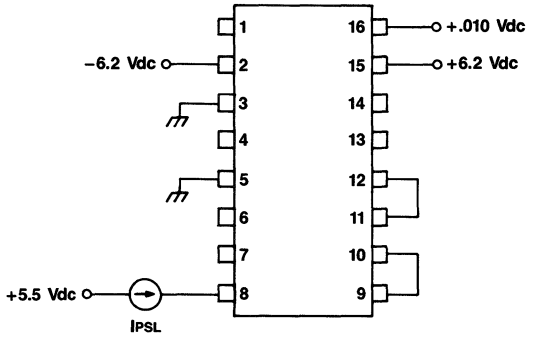


Figure 2. VIN Comparator Section

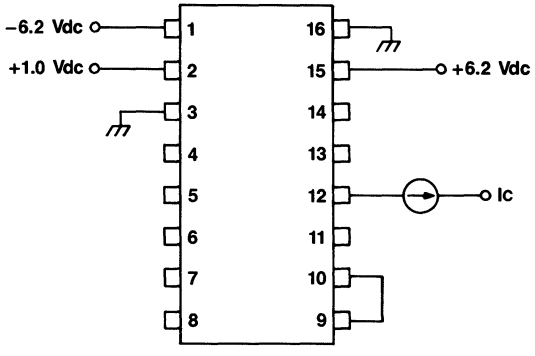


Figure 3. Charging Current

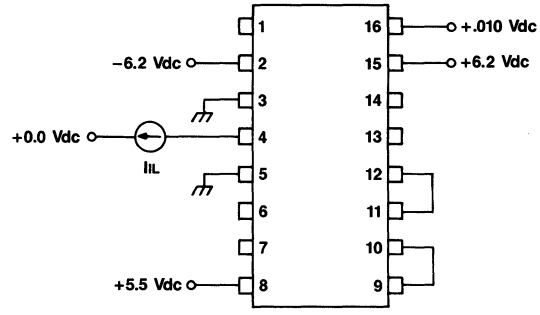


Figure 4. Logic Supply Current (IPSL)

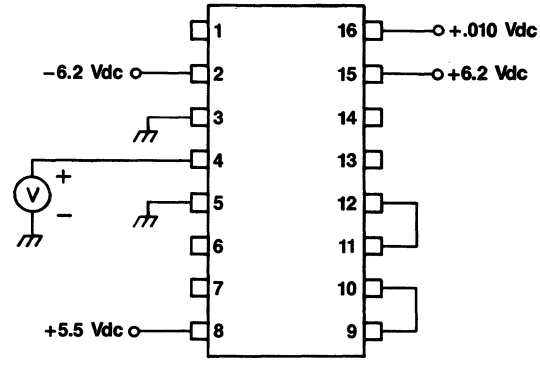


Figure 5. Input Forward Current, V(s) = 0

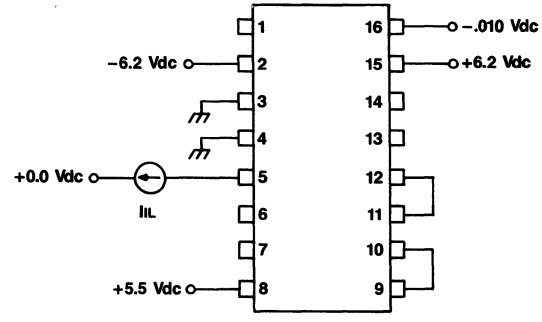


Figure 6. Input Forward Current, V(4) = 0

Test Circuits (Continued)

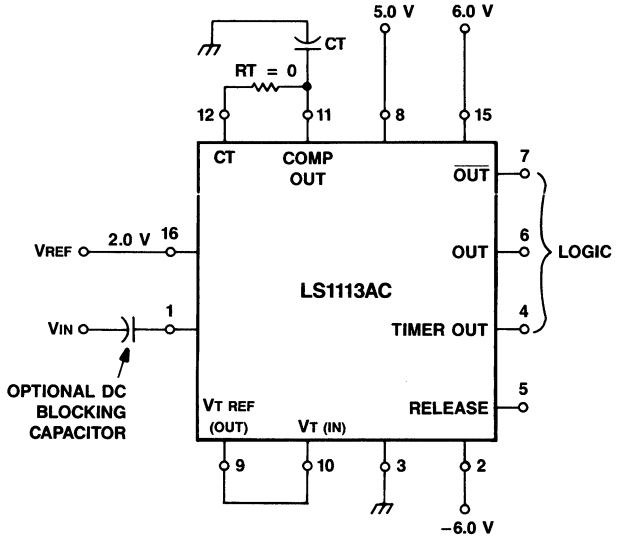
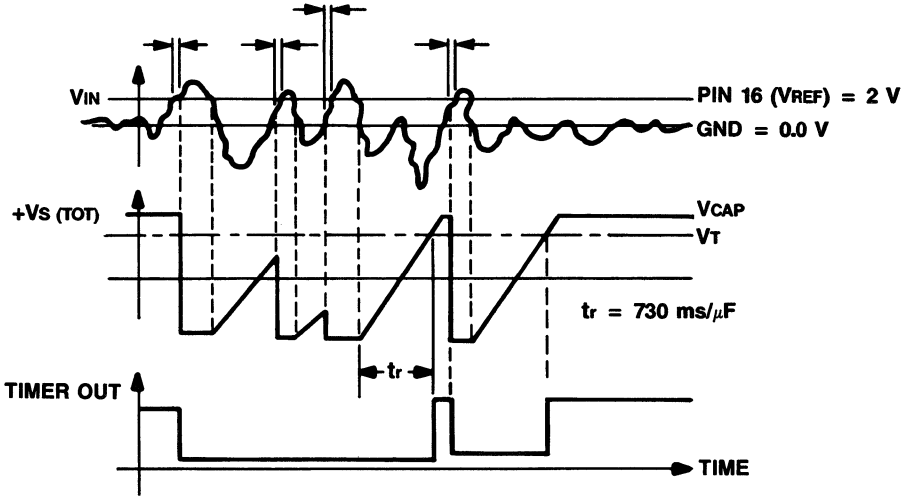


Figure 7. Typical Connections

Timing Characteristics



Truth Table			
R (t_N)	To (t_N)	OUT (t_{N-1})	OUT (t_N)
0	—	—	1
1	0	—	0
1	1	0	0
1	1	1	1

Figure 8. Timing Diagram and Truth Table

Circuit Overview

Figure 8 shows a typical connection with its timing diagrams and truth table. In this case, the external timing capacitor (C_T) is connected from leads 11 and 12 to ground ($-V_{S1}$ and $+V_{S1}$ can also be used). The internally generated threshold voltage (V_T), lead 9 is applied to the detector threshold input [$T_{(IN)}$] lead 10.

When the signal on $-$IN exceeds that on $+$IN, the comparator output goes low, discharging the capacitor via the 2.0 kΩ current-limiting resistor from $+V_{S1} - 0.2$ V to $-V_S + 0.6$ V. After the capacitor voltage drops below the detector threshold ($\approx -V_S + 8.0$ V), the detector output accesses to the low state.

The access time is (2.0 μs $+$1.0 ms/μF) $\pm$40% for $\pm$6.0 V power supplies.

When the signal on $-$IN drops below that on $+$IN, the comparator open-collector output releases, charging the capacitor via the 10 μA current source. After the capacitor voltage exceeds the detector threshold input, the output of the detector releases to the high state. The release time is $\approx$ 730 ms/μF.

The circuit is trimmed during manufacturing to ensure that the comparator input offset is within $\pm$3.5 mV and the release time of an appropriate external capacitor is 730 ms/μF $\pm$5.0 percent when the V_T is used as the $V_{T(IN)}$ (leads 9 and 10 connected).*

Additional error terms will, of course, result from capacitor tolerance and leakage. In evaluating leakage errors, users should note that the charging current is approximately 10 μA and the voltage in the capacitor during timing swings is set for $-V_S$ to $-V_S + 8$ V.

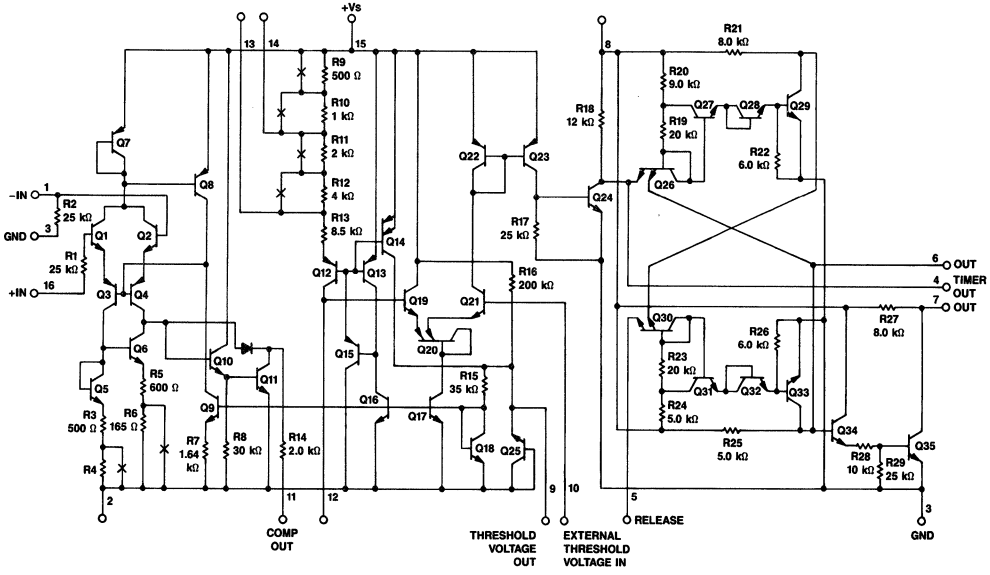
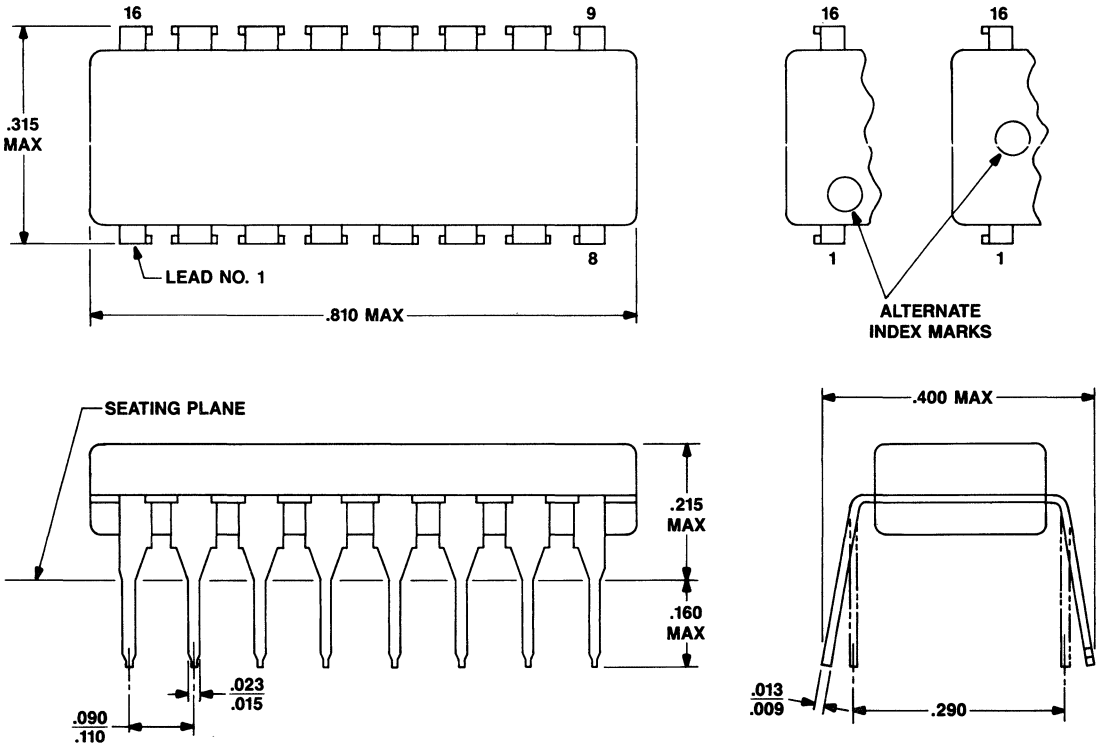


Figure 9. Basic Schematic

Schematic, as shown, does not include parasitic components and is subject to change. However, the design intent of the device is guaranteed by the electrical characteristics.

Outline Drawing

(Dimensions in Inches)



Ordering Information

Device	Comcode
LS1113AC	104411921

Description

This LS1114AC Quad Comparator is a general-purpose device certified for operation over a power supply range of +4 to +33 V and functions with single or dual power supplies. It consists of four identical comparator segments and features an open collector output, common-mode voltage range below the negative supply, input protection, and a shutdown option.

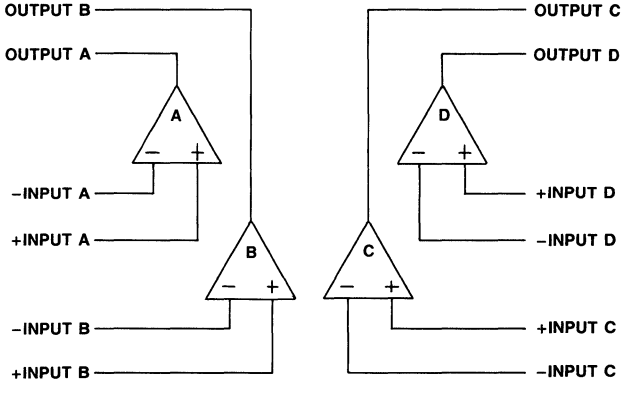
The optional shutdown function will disable the entire device to a current of less than 200 μA while allowing all outputs to go high. Disabling is accomplished by connecting 80 μA into the disable lead, pin 8. Input protection is provided; however, the input current must be limited to ±16 mA.

The LS1114AC Quad Comparator is available in a 16-pin plastic DIP.

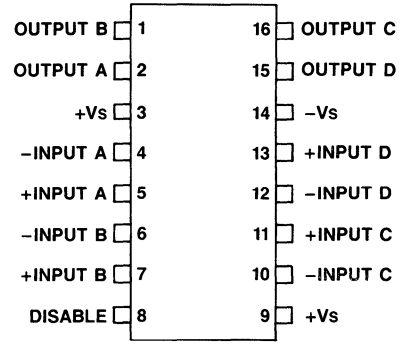
Features

- General-purpose applications
- Low standby power supply current (≤ 700 μA with ±15 V supply)
- Overload protection
- Power supply range, +4 to +33 V
- Single or dual power supply
- Optional shutdown function
- Input current protection to ±16 mA
- Low output saturation voltage (≤ 400 mV @ 4.5 mA)

Functional Diagram



Pin Diagram



Maximum Ratings*

Parameter	Pins	Rating	Unit
Input Voltages**	V(4, 14), V(5, 14), V(6, 14) V(7, 14), V(10, 14), V(11, 14) V(12, 14), V(13, 14)	−0.5 and (+Vs −Vs) +0.5	V
Differential Input Voltages	V(4, 5), V(6, 7), V(10, 11) V(12, 13)	±33	V
Output Voltages	I(1, 14), I(2, 14), I(15, 14), I(16, 14)	34	Vdc
Power Supply Voltages	V (3, 14) V(9, 14)	33	V
Input Currents	I4, I5, I6, I7, I10, I11, I12, I13	±16	mA
Power Dissipation	—	400	mW
Storage Temperature Range	—	−40 to +125	°C
Operating Temperature Range	—	0 to 60	°C

Notes:

* Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

** Input voltages greater than 0.5 volt above the positive supply or greater than 0.5 volt below the negative supply are permitted, provided that input currents do not exceed 16 mA. Correct output condition and high input impedence cannot, however, be assured for input voltages outside of the common mode range.

Pin Descriptions

Pin	Symbol	Name/Function
1	Output B	Output, Comparator B
2	Output A	Output, Comparator A
3	+Vs	Positive voltage supply
4	−Input A	Negative input, Comparator A
5	+Input A	Positive input, Comparator A
6	−Input B	Negative input, Comparator B
7	+Input B	Positive input, Comparator B
8	Dis	Disable
9	+Vs	Positive voltage supply
10	−Input C	Negative input, Comparator C
11	+Input C	Positive input, Comparator C
12	−Input D	Negative input, Comparator D
13	+Input D	Positive input, Comparator D
14	−Vs	Negative voltage supply
15	Output D	Output, Comparator D
16	Output C	Output, Comparator C

Electrical Characteristics*

(T_A = 25°C)

Characteristic and Conditions			Symbol	Min	Max	Unit
Input Offset Voltage		V_S = ±2.0 V and V_S = ±16.5 V	V_{IO}	—	±5.0	mV
Input Bias Current			I_{IB}	0	−500	nA
Input Offset Current			I_{IO}	—	±150	
Output Voltage (I_O = 3.5 mA)			V_{OI}	—	400**	mV
Output Leakage Current			I_{OH}	—	1.0	μA
Power Supply Current			+I_{PS}	0.1	1.8	mA
Power Supply Current (Disable)		V_S = ±16.5 V	+I_{PS}	0.2	700	μA
		V_S = ±2.0 V	+I_{PS}	0.2	250	
Comparator Voltage Gain		V_S = ±15 V, R_L = 1.0 kΩ	A_V	1,000	—	—
Common-Mode Voltage Range		V_S = ±2.0 V	+CMVR	0.4	—	V
			−CMVR	−2.2	—	
		+V_S = +33 V, −V_S = 0 V	+CMVR	31	—	
			−CMVR	0	—	
Propagation Delay Time†	10 mV Overdrive	V_S = ±5.0 V, R_L = 10 kΩ, C_L = 50 pF	t_{PLH}	—	3.0	μs
			t_{PHL}	—	3.0	
	100 mV Overdrive		t_{PLH}	—	1.5	
			t_{PHL}	—	1.5	
Transmission Time			+t_{THL} t_{TLH}	—	430	ns

* The minimum and/or maximum limits, specified for the characteristics, are based on the absolute system. The algebraic sign, implied or specifically noted, applies to the direction or polarity of the characteristic.

** Output Voltage (V_O) measured with respect to −V_S.

† Measurements are made with 100 mV underdrive as initial condition.

Operating Recommendations

Meeting at least one of the following precautions will guarantee proper operation of the LS1114AC Quad Comparator.

- Power-up the negative supply before the positive supply.
- Tie the disable pin to the positive supply during power-up.
- Inputs to ground must have a minimum of 3 K ohms series resistance. In addition, unused input pairs should be connected with one of the following circuits:
  — all unused input pairs floating,
  — all negative inputs with 10 K ohm series resistance to ground and all positive inputs with 3 K ohm series resistance to ground.

Test Circuits

General Notes:

Resistor values selected for use in all test circuits are characterized by a nominal ±1% tolerance; capacitors, ±10%.

Test circuits illustrate comparator A only. Equivalent tests are also done on comparators B, C, and D.

Unless otherwise specified, comparators not being tested will be returned to ground through 1 kΩ on the noninverting side and 10 kΩ on the inverting side. The outputs will remain open.

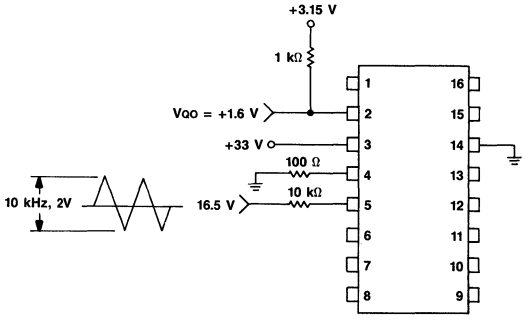


Figure 1. Input Offset Voltage; Input Bias Current; Input Offset Current (+Vs = 33 V and −Vs = 0 V)

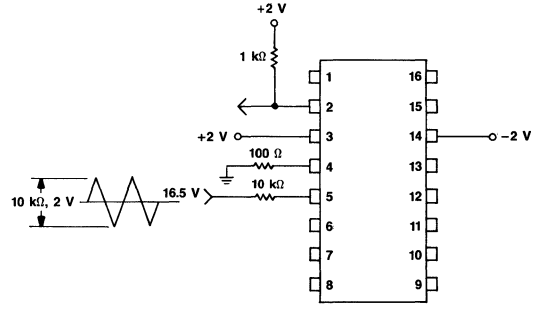


Figure 2. Input Offset Voltage; Input Bias Current; Input Offset Current (+Vs = 2 V and −Vs = −2 V)

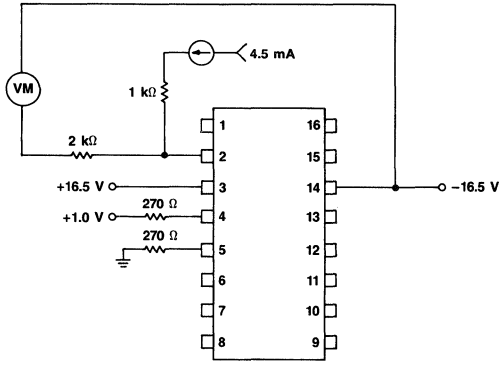


Figure 3. Low-Level Output Voltage (+Vs = +16.5 V and −Vs = −16.5 V)

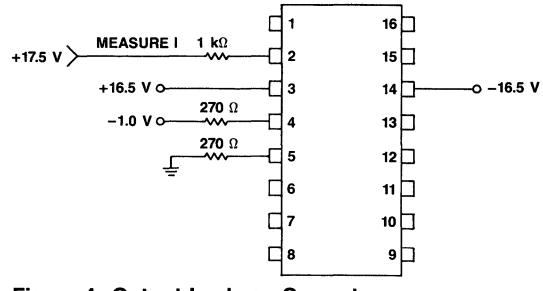


Figure 4. Output Leakage Current (+Vs = +16.5 V and −Vs = −16.5 V)

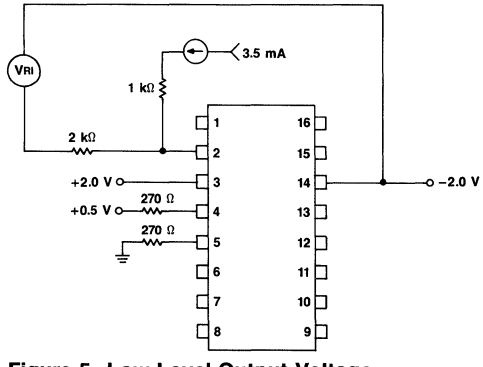


Figure 5. Low-Level Output Voltage (+Vs = +2 V and −Vs = −2 V)

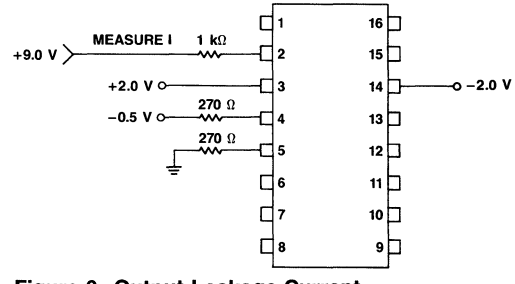


Figure 6. Output Leakage Current (+Vs = +2 V and −Vs = −2 V)

Test Circuits (Continued)

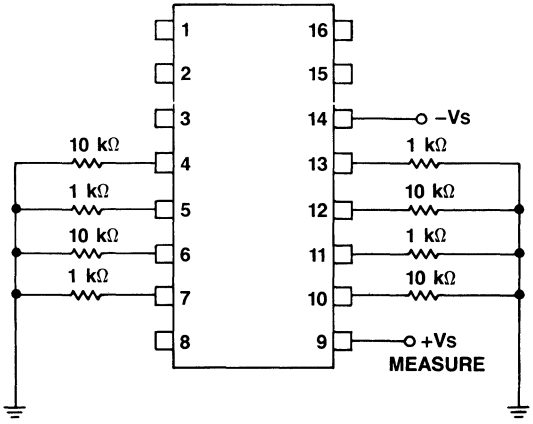


Figure 7. Power Supply Current

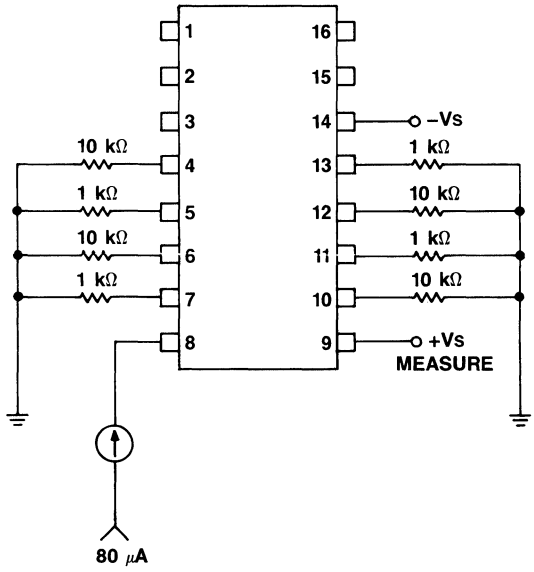


Figure 8. Power Supply Current (Disabled)

Characteristic Curves

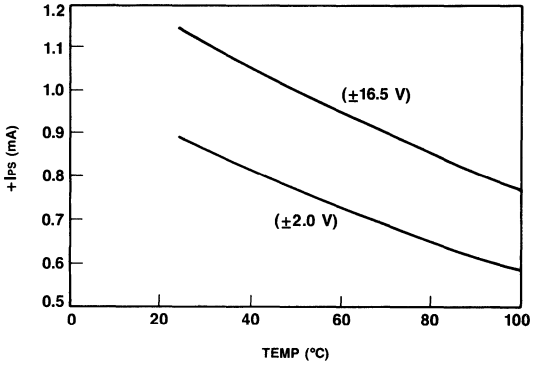


Figure 9. Temperature vs. Power Supply Current at Various Supply Voltages

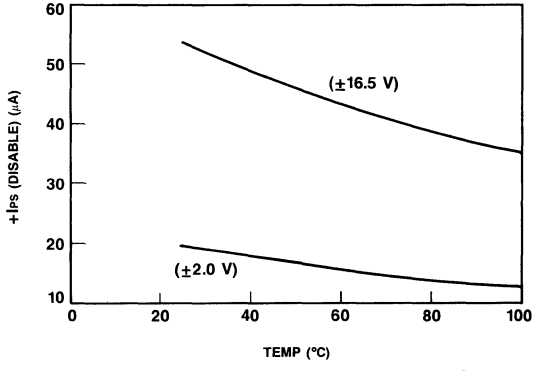


Figure 10. Temperature vs. Power Supply Current (Disabled) at Various Supply Voltages

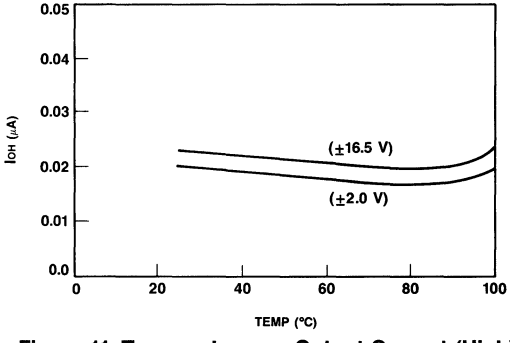


Figure 11. Temperature vs. Output Current (High) at Various Supply Voltages

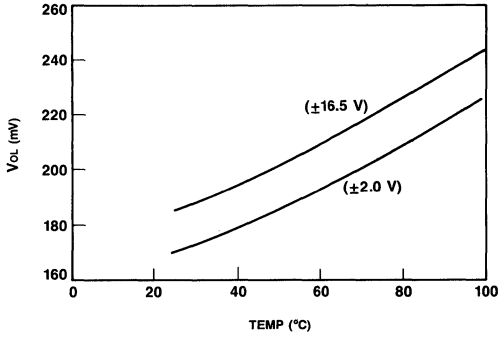


Figure 12. Temperature vs. Output Voltage (Low) at Various Supply Voltages

Characteristic Curves (Continued)

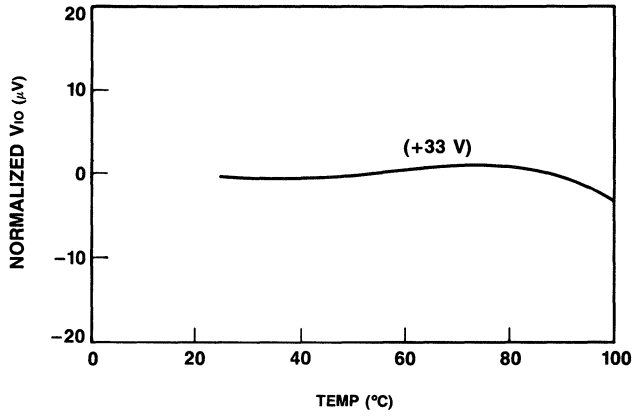


Figure 13. Temperature vs. Input Offset Voltage (Normalized) at Various Supply Voltages

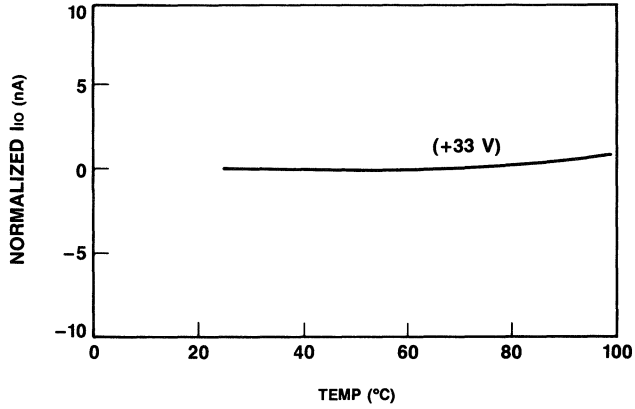


Figure 14. Temperature vs. Input Offset Current (Normalized) at Various Supply Voltages

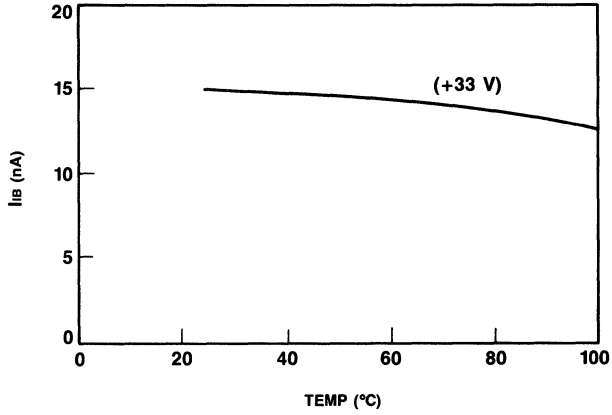
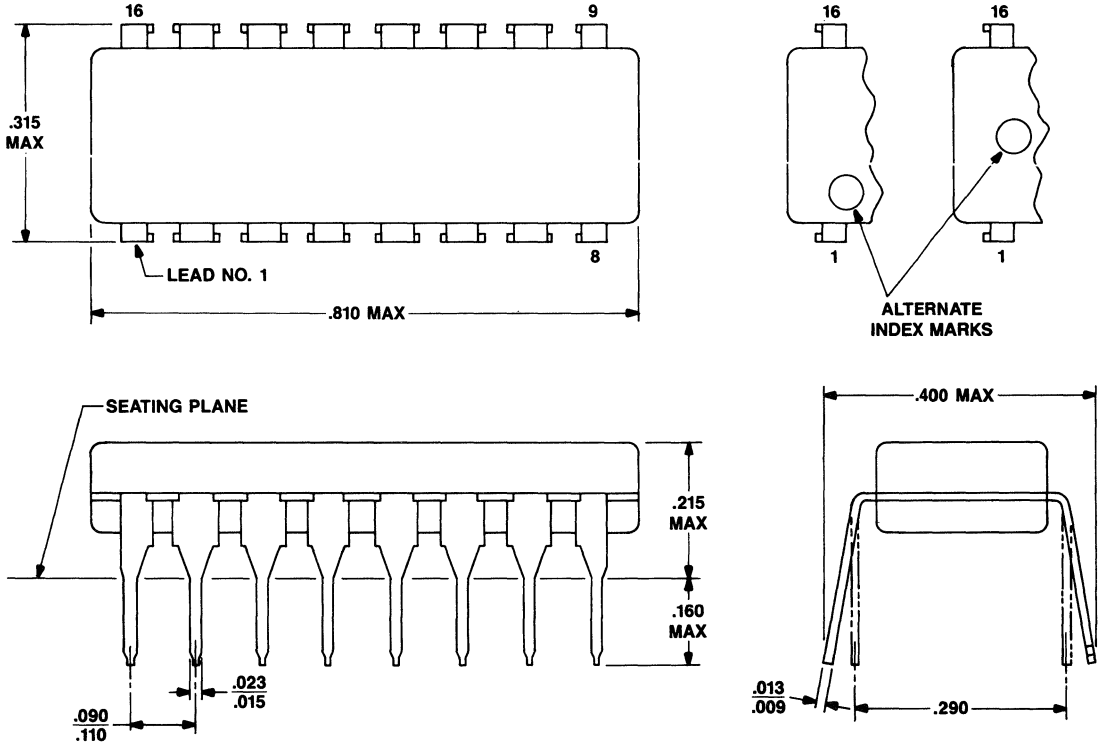


Figure 15. Temperature vs. Input Bias Current at Various Supply Voltages

Outline Drawing

(Dimensions in inches)



Ordering Information

Device	Comcode
LS1114AC	104411947

Description

The LS1115AC integrated circuit is a high-gain, high-impedance device consisting of a three-input, emitter-coupled comparator; a two-input second-stage comparator, and an output amplifier. An approximate gain of 100 dB can be achieved by using the chip in a comparator/amplifier combination.

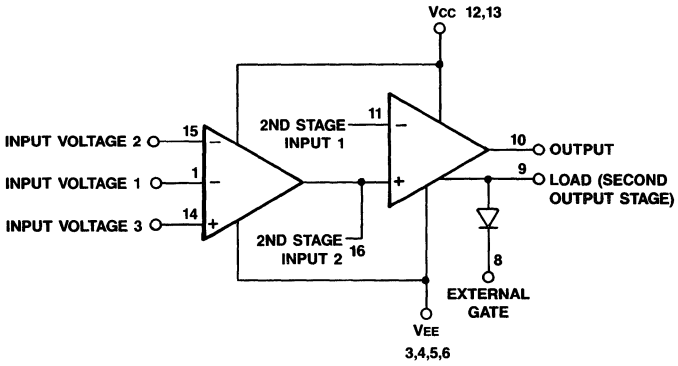
The device accepts three inputs and provides an "OR" function with the two inverting inputs. The second comparator includes complementary open-collector outputs and an internal diode-clamped output.

The comparator is recommended for a number of general-purpose applications such as peak- and zero-crossing detectors, switching-power amplifiers, A/D converters, clock generators, multivibrators, logic interfaces, logic gates, line receivers, and hysteresis elements. The LS1115AC Three-Input Comparator is available in a 16-pin plastic DIP.

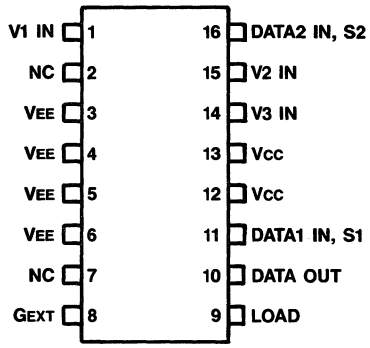
Features

- High-output voltage gain, 100 dB
- Two high-impedance input comparators
- Specialized logic functions
- Complementary open-collector outputs
- Internal diode-clamped output option

Functional Diagram



Pin Diagram



Maximum Ratings

Parameter	Rating	Unit
Positive Power Supply (V_{CC})	8.0 ±5%	Vdc
Negative Power Supply (V_{EE})	−4.3 ±5%	Vdc
Power Dissipation	210	mW
Storage Temperature Range	−40 to +125	°C
Operating Temperature Range	0 to 60	°C

* Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions

Pin Number	Name/Function	Pin Number	Name/Function
1	Input Voltage 1	9	Load
2	No Connection	10	Output
3	V_{EE}	11	2nd Stage Input 1
4	V_{EE}	12	V_{CC}
5	V_{EE}	13	V_{CC}
6	V_{EE}	14	Input Voltage 3
7	No Connection	15	Input Voltage 2
8	External Gate	16	2nd Stage Input 2

Electrical Characteristics

(T_A = 25°C)

Characteristics and Conditions			Symbol	Min	Max	Units
First Stage						
Single-Ended Voltage Gain	V_{16} = 4.6 Vdc	V_{14} = 4.0 Vdc, $\triangle V_{15}$ < − 200 mVdc	A_{V1}*	27.95	—	dB
	V_{16} = 3.5 Vdc					
	V_{16} = 4.6 Vdc	V_{14} = 4.0 Vdc, $\triangle V_1$ < − 200 mVdc	A_{V2}**			
	V_{16} = 3.5 Vdc					
Input Offset Voltage	V_{16} = 4.0 Vdc		V_{IO}	—	±20	mVdc
Common-Mode Input Current	$V_1 = V_{14} = V_{15}$ = 4.0 Vdc		CMI_{IN}	—	1.0	μAdc
Second Stage						
Output Voltage	V_{11} = 3.50 Vdc	V_{16} = 3.45 Vdc	V_{OUT}	—	0.50	Vdc
		V_{16} = 3.55 Vdc		7.70	—	
	V_{11} = 4.60 Vdc	V_{16} = 4.55 Vdc		—	0.50	
		V_{16} = 4.65 Vdc		7.70	—	
Input Bias Current	V_{11} = 3.50 Vdc, V_{16} = 4.60 Vdc		I_{IB}	—	1.0	μAdc
	V_{11} = 4.60 Vdc, V_{16} = 3.50 Vdc			—	50	
Supply Current	$V_{12} = V_{13}$ = 8.0 Vdc		I_S	—	18	mAdc
	$V_3 = V_4 = V_5 = V_6$ = −4.3 Vdc					

* $\triangle V_{16}/\triangle V_1$

** $\triangle V_{16}/\triangle V_{15}$

Test Circuits

Resistor values selected for used in all test circuits are characterized by a nominal ± 1% tolerance; capacitors, ± 10%.

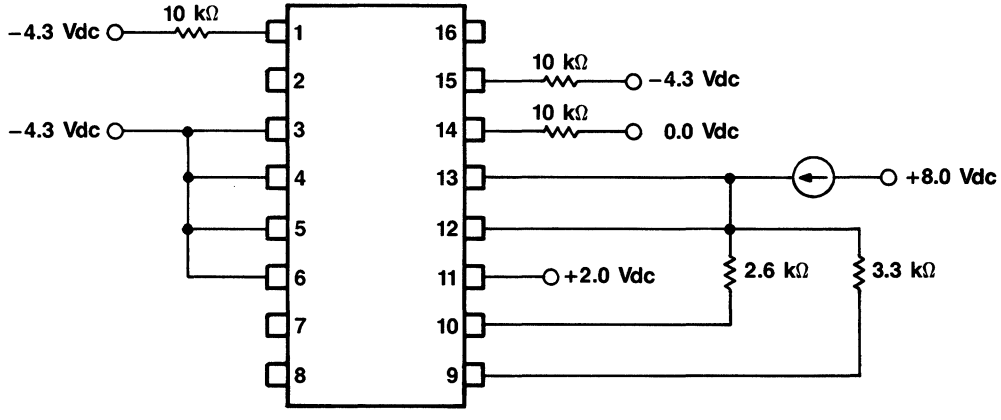


Figure 1. Current Supply (Is)

Test Circuits
(Continued)

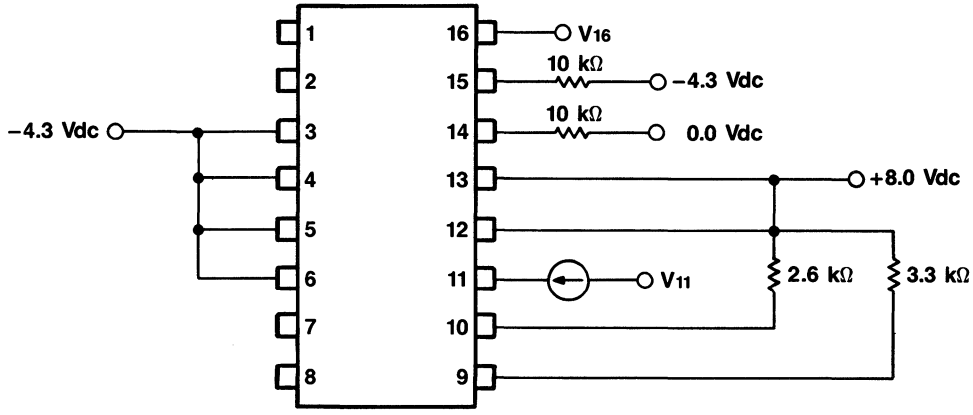


Figure 2. Input Bias Currents (I_{IB})

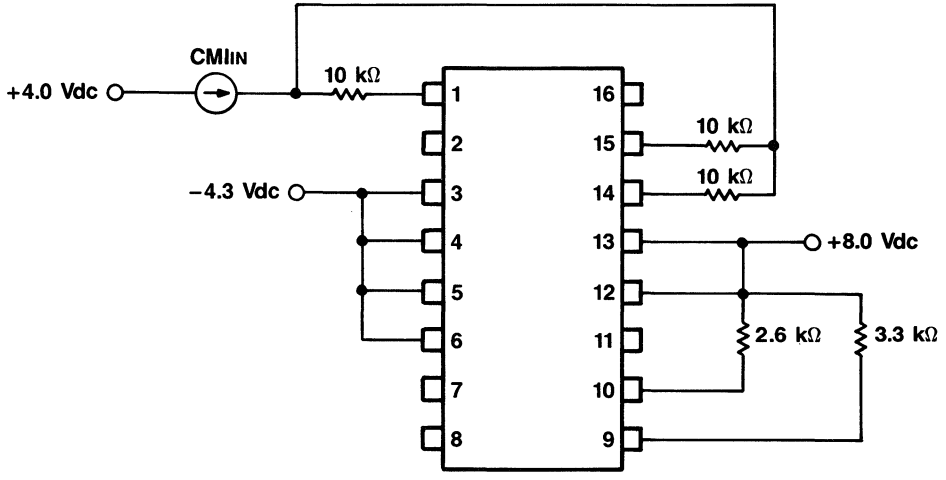


Figure 3. Common Mode Input Current (CMI_{IN})

Test Circuits
(Continued)

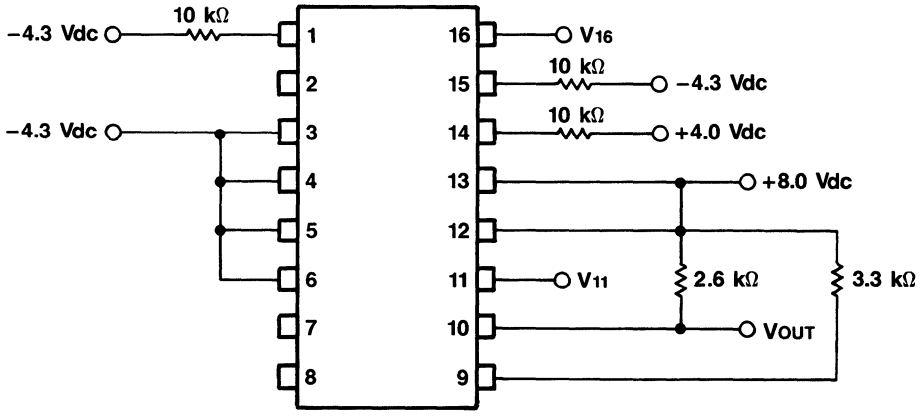


Figure 4. Output Voltage (V_{OUT})

Characteristic Curves

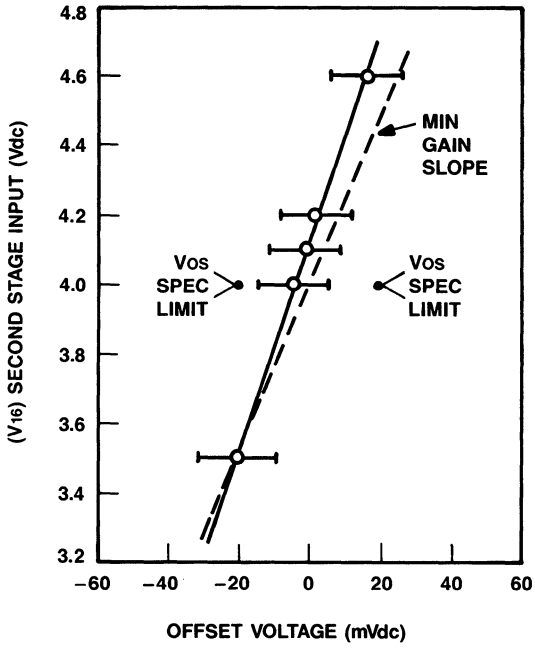


Figure 5. Average Offset Voltage

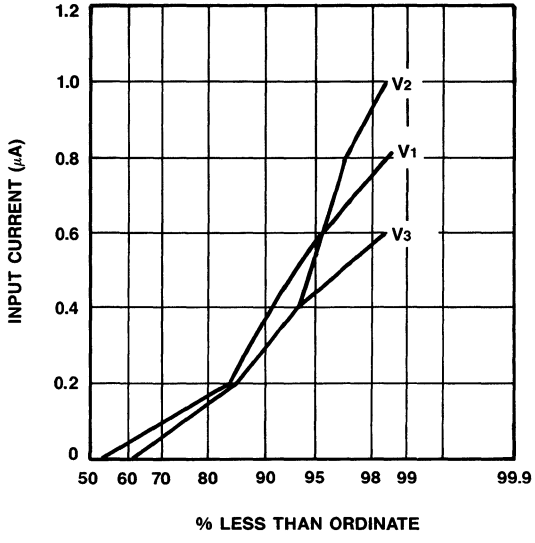


Figure 6. Typical Input Current Distributions

User Information

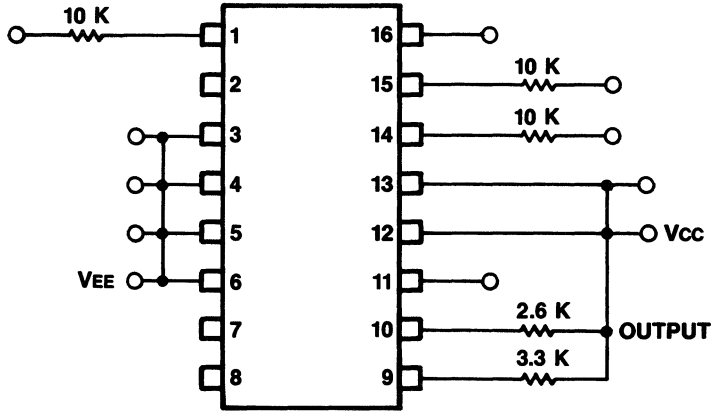


Figure 7. Connection Diagram

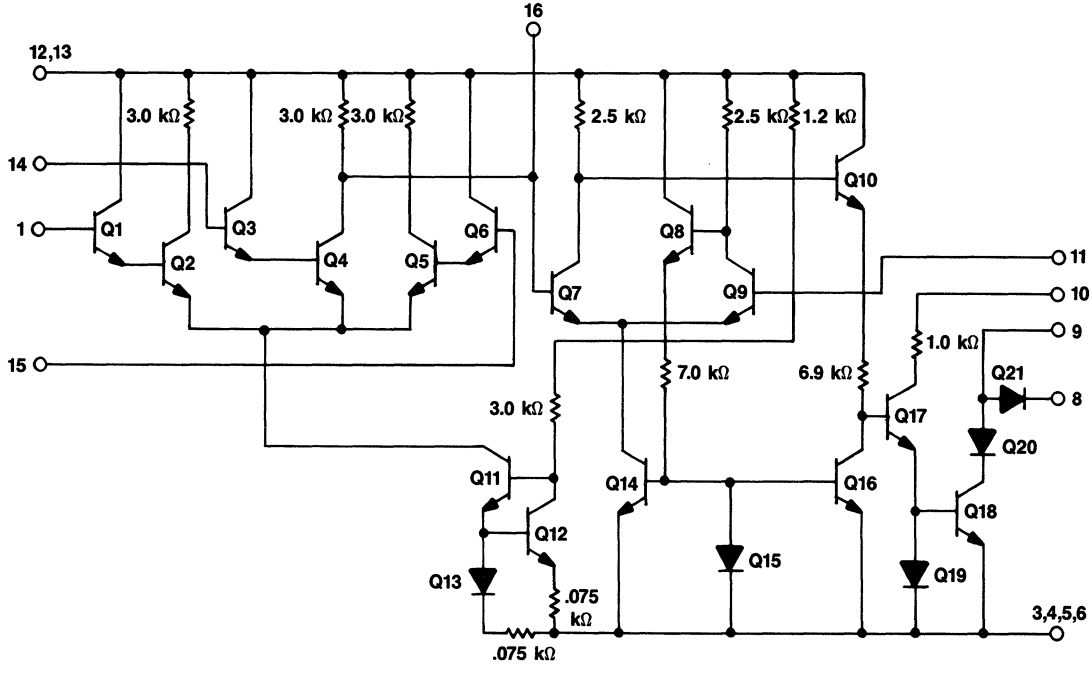
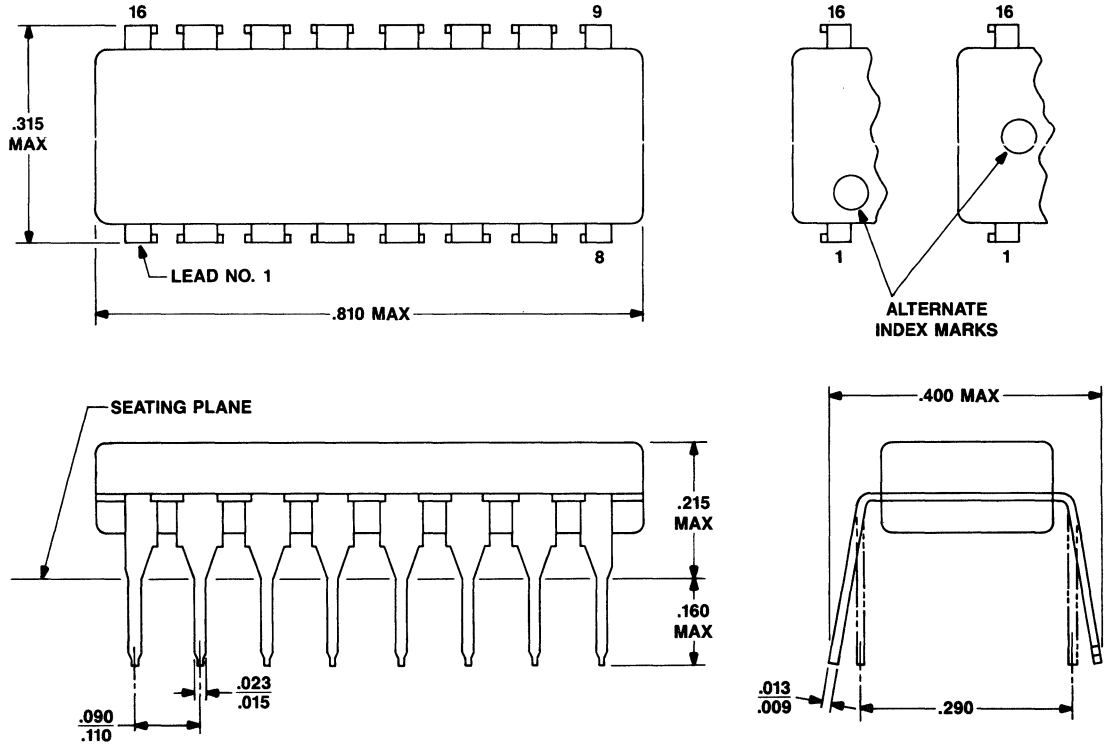


Figure 8. Basic Schematic

Outline Drawing

(Dimensions in Inches)



Ordering Information

Device	Comcode
LS1115AC	104411962

DUAL SAMPLE-AND-HOLD AMPLIFIERS LB1127AAK

ADVANCE

Description

The LB1127AAK is a silicon integrated circuit consisting of two separate sample-and-hold circuits, with differential inputs, combined in one 24-pin, hermetically-sealed, leadless ceramic chip carrier. It consists of FET input amplifiers in series with switched, high performance operational amplifiers. Internal holding capacitors are connected to the switch output (Functional Diagram), but provisions have been made so that external capacitors may be connected in parallel. This provides for application flexibility. This device is ideal for data systems where fast acquisition time, low sample-to-hold offset and low droop rate are critical.

The LB1127AAK (in addition to being a dual device) has an advantage over comparable devices in that offset voltage drift is guaranteed by production testing to be less than 20 μV/°C.

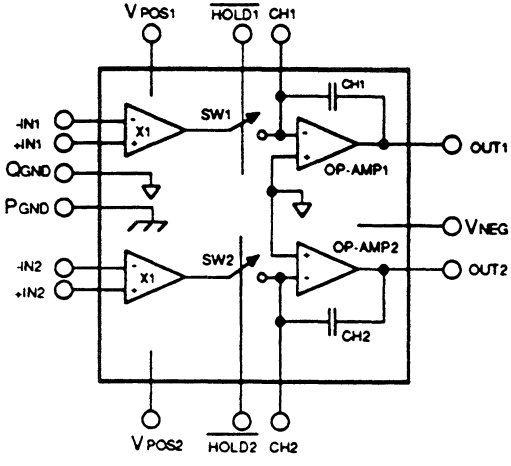
Features

- Fast acquisition time (10 V step to $\pm$0.01%) $\leq$ 3 us
- Low droop rate (CH = 100 pF) $\leq$ 1.0 mV/ms
- Sample-hold offset step $\leq$ 3 mV
- Low aperature jitter $\approx$ 0.5 ns
- TTL-compatible control inputs
- 100 pF internal hold capacitor. External capacitance can be added to reduce droop rate when long hold times and high accuracy are required.

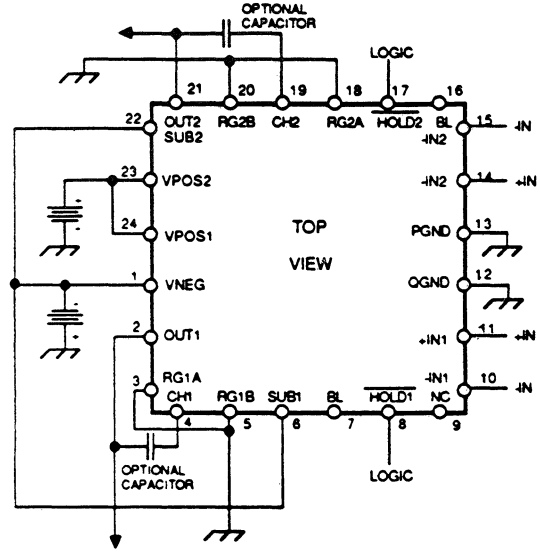
Applications

- Data Acquisition Systems
- Peak Detection
- Data Distribution Systems
- Analog Delay and Storage
- A/D Conversion Systems

Functional Diagram



Pin Diagram



Maximum Ratings

(At T_A 25°C unless otherwise specified)

Ambient Operating Temperature Range	15 to 75°C
Storage Temperature Range	−40 to +125°C
Pin Soldering Temperature (t = 15 sec max.)	300°C
Supply Voltage (V_{POS} to V_{NEG})	30 V
Short Circuit Output Current	40 mA
Logic Input Voltage (Pins 7 and 17)	V_{POS}, V_{NEG}
Differential Input Voltage	±8V

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Table 1. Operating Characteristics

Parameter	Min	Max	Unit
Operating Supply Voltage (V_{POS}, V_{NEG})	+5, −12	±16.5	V
Output Current (Source or Sink)	—	15	mA

Table 2. Logic Input Levels

Parameter	Min	Max	Unit
HOLD1 (Pin 8) and HODL2 (Pin 17)			
High Input Voltage	2.0	—	V
Low Input Voltage	—	0.8	V

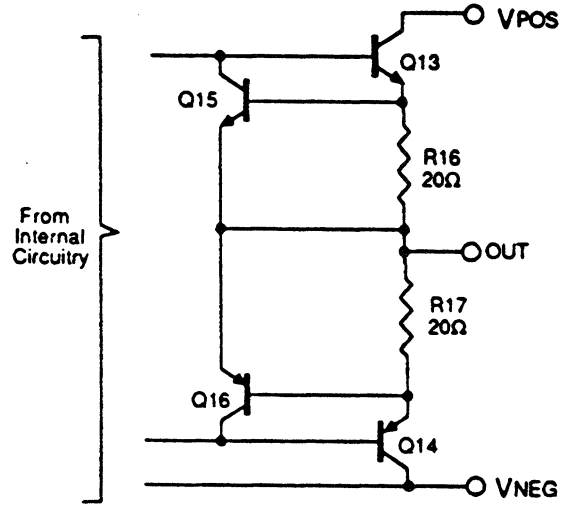


Figure 1. Sample-And-Hold Op-Amp Outputs (Simplified)

Pin Descriptions

Pin	Symbol	Name/Function
1	V_{NEG}	The most negative supply voltage to the device, serving both amplifiers.
2 21	OUT1 OUT2	Output for amplifiers 1 and 2 respectively. See Figure 1 for simplified output diagram.
3 4 5	RG1A CH1 RG1	Pin 4 is provided so that an external capacitor may be placed in parallel with an internal hold capacitor CH1 (Functional Diagram). An external capacitor may be connected between Pin 4 and OUT1 (Pin 2) to reduce droop when long hold times and accuracy are required. Pins 3 and 5 provide ring guards (they should always be connected to ground) for the output circuitry of Amplifier 1. The ring guard circuitry minimizes output drift during hold-mode operation.
6 22	SUB1 BUS2	Substrate for the device. These pins should always be connected to V_{NEG} (Pin 1), the most negative voltage on the device.
8 17	$\overline{HOLD1}$ $\overline{HOLD2}$	TTL compatible (see Table 2) inputs for amplifiers 1 and 2 respectively. A logic low signal will put the respective amplifier in the hold-mode.
9	NC	No connection. External circuitry should **not** be connected to this pin.
10 11 14 15	−IN1 +IN1 +IN2 −IN2	Inverting and noninverting inputs to amplifiers 1 and 2 respectively. These pins connect to FET input, unity gain amplifiers.
12	Q_{GND}	Quiet Ground. This is the ground for low-current circuitry. It should be connected directly to system ground. Care should be used to make certain that P_{GND} is not connected between this pin and system ground.
13	P_{GND}	Power Ground. This is the high-current ground for the output stage. It should be connected directly to the system ground.
16 7	BL	Blank. External circuitry may be connected to this pin if the voltage does not exceed 25 volts.
18 18 20	RG2A CH2 RG2B	The description is the same as for Pins 3, 4, and 5, respectively, except that it applies to amplifier 2.
23 24	V_{POS2} V_{POS1}	Positive supply voltage for amplifiers 2 and 1 respectively.

Testing Requirements

(At T_A = 25°C unless otherwise specified)

These requirements are for each separate amplifier section. Referenced Test Figures are illustrated for amplifier section 1 only.

Characteristic	Test Condition	Min	Typ	Max	Unit
Acquisition Time	Figure 2; VIN1 = 5.0 V	—	—	3.0	μs
Droop Rate	Figure 2	—	—	±1.0	mV/ms
Pedestal Error Voltage	Figure 2; VIN1 = 0	—	—	±3.0	mV
Feedthrough Voltage	Figure 2; VHOLD1 = 0 VIN1 = 10 kHz	—	—	1.6	mVrms
Open Loop Voltage Gain	Figure 3	200	—	—	kV/V
Common-Mode Rejection	Figure 4	80	—	—	dB
Full-Power Bandwidth	Figure 5; −3 dB point	100	—	—	kHz
Slew Rate (△VOUT/△ts)	Figure 6; △ts1 △ts2	 4.0 4.0	 8.0 8.0	 — —	 V/μs V/μs
Output Resistance	Figure 7	—	—	0.05	ohms
Input Offset Voltage	Figure 8	—	—	±3.0	V
Input Offset Voltage Change, Temperature	Figure 8; △V (75°C-25°C)	—	—	1.0	mV
Input Bias Current	Figure 9	—	—	±2.0	nA
Logic Input Current	Figure 10	—	—	±5.0	μA
Positive Power Supply Current, Quiescent	Figure 11 IPOS1 IPOS2	 — —	 — —	 6.0 6.0	 mA mA
Negative Power Supply Current, Quiescent	Figure 11	—	—	12.0	mA
Power Supply Rejection Ratio	Figure 12	75	—	—	dB
Crosstalk	Figure 13	—	—	80	dB

Test Circuits

(See Note 1)

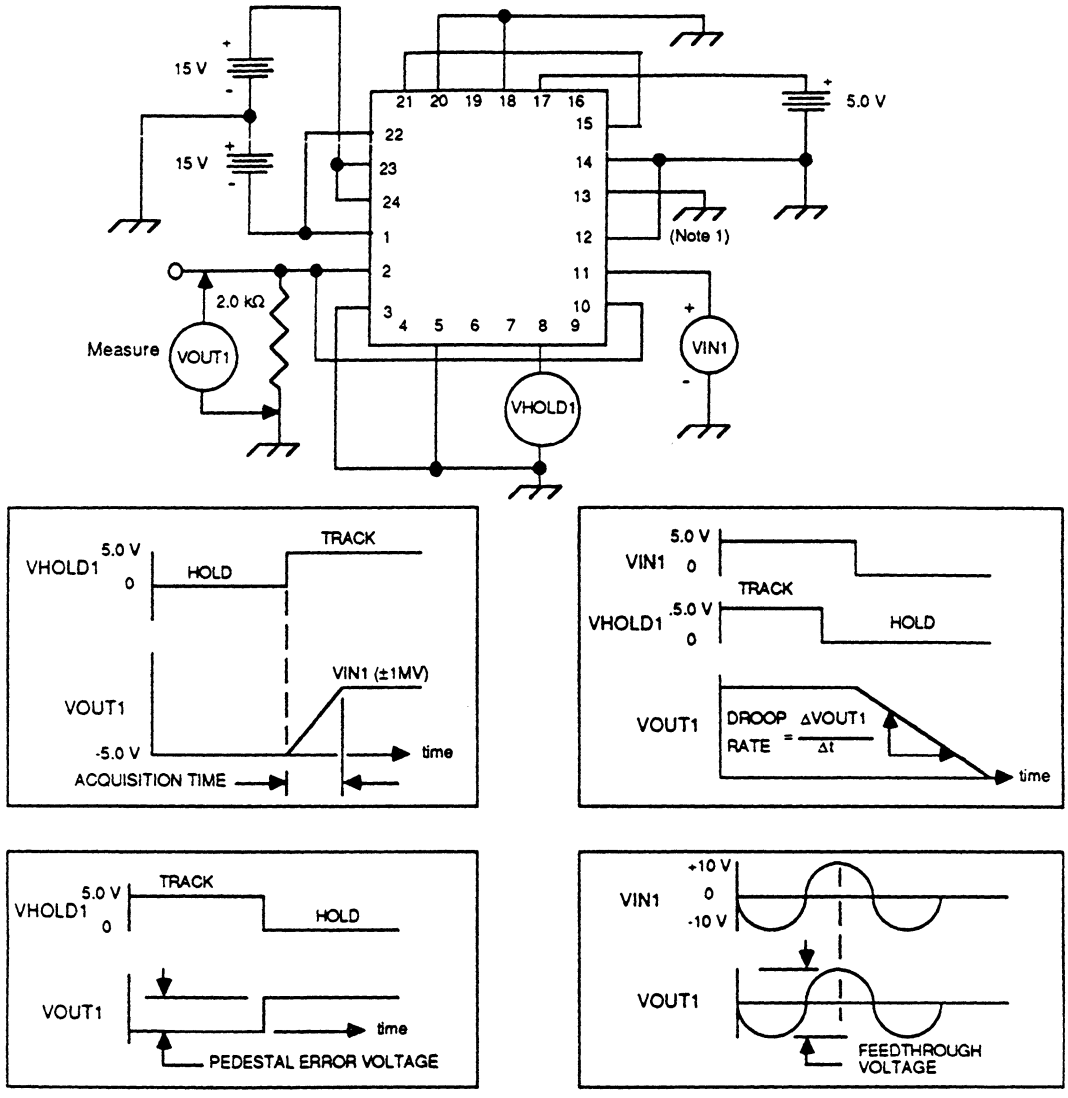


Figure 2. Test Circuit

Note 1: All power supply rails should be by-passed with capacitors of 0.1 μF or greater. These capacitors should be connected as close as possible to the appropriate device pin.

Pin 13 is a high-current ground termination. Care should be used to make certain that Pin 13 connects directly to ground, and does not connect to a tie-point between any other device pin and ground.

Test Circuits
(Continued)

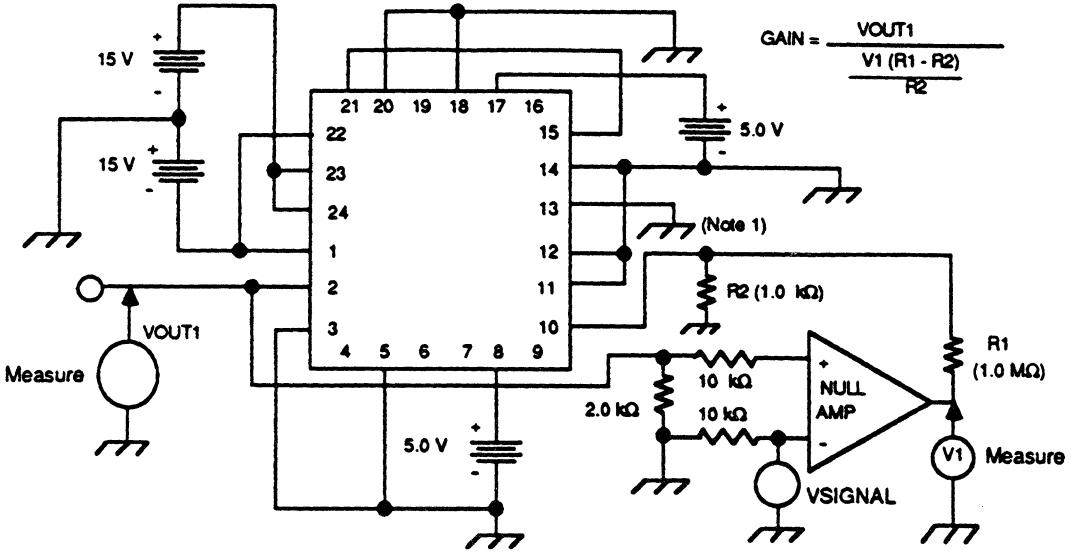


Figure 3. Open Loop Gain Test Circuit

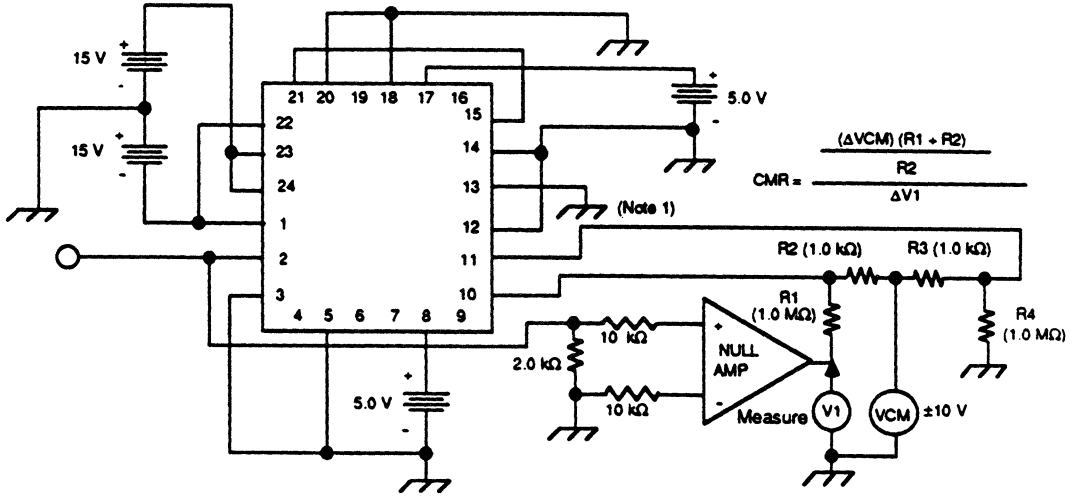


Figure 4. Common Mode Rejection Test Circuit

Test Circuits
(Continued)

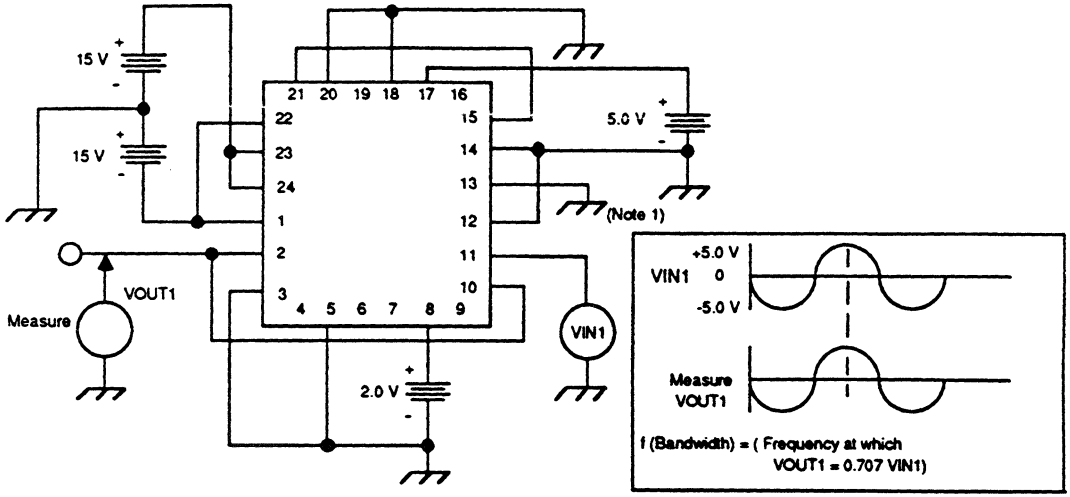


Figure 5. Full-Power Bandwidth Test Circuit

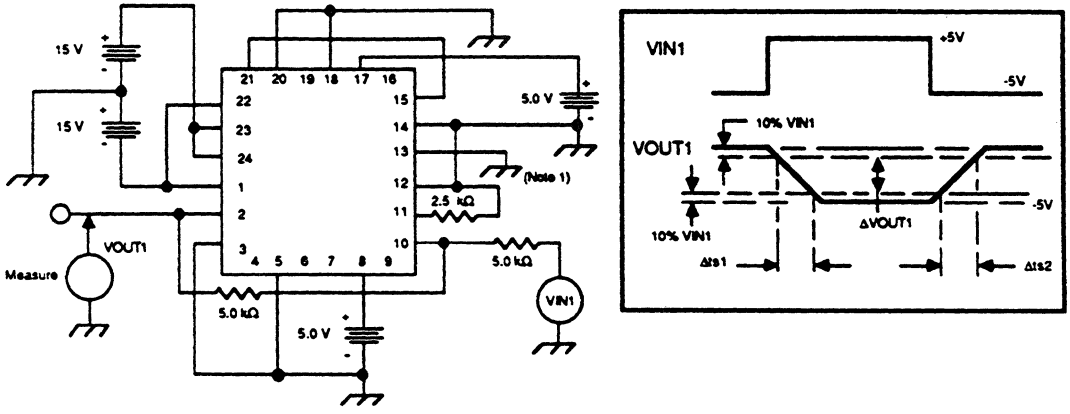


Figure 6. Slew Rate Test Circuit

Test Circuits (Continued)

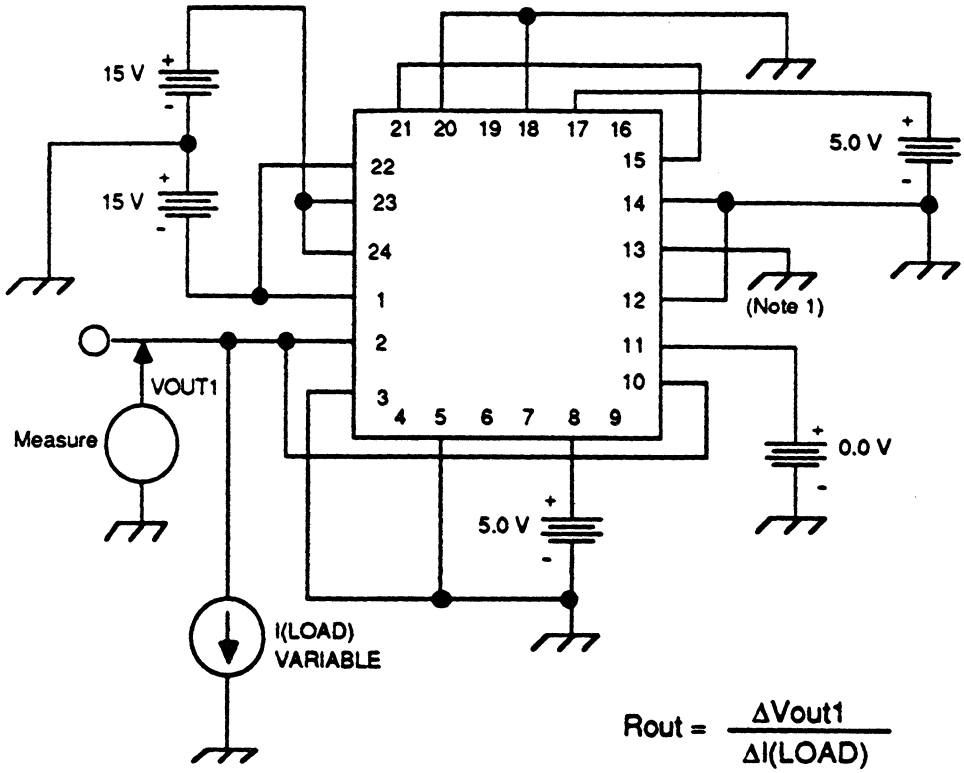


Figure 7. Output Resistance Test Circuit

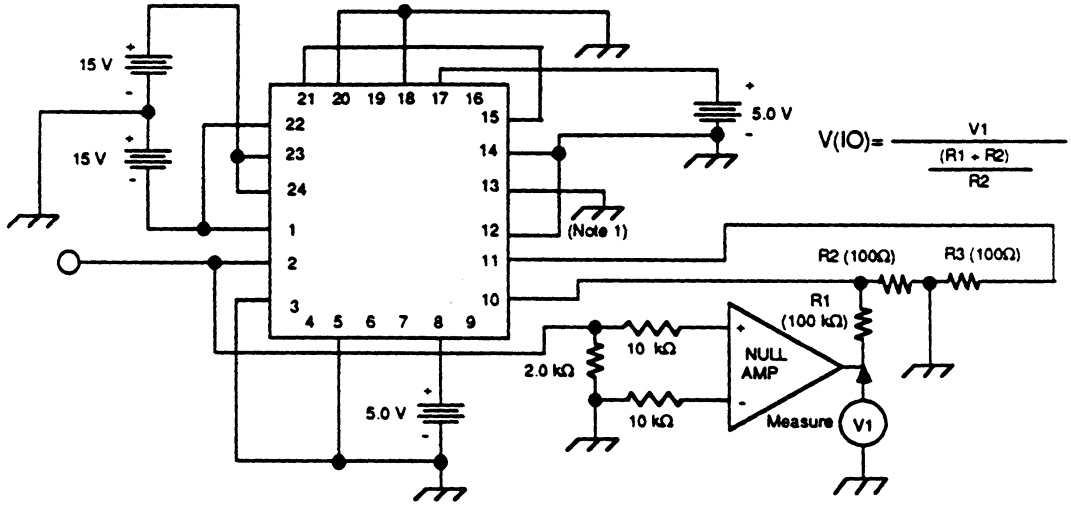
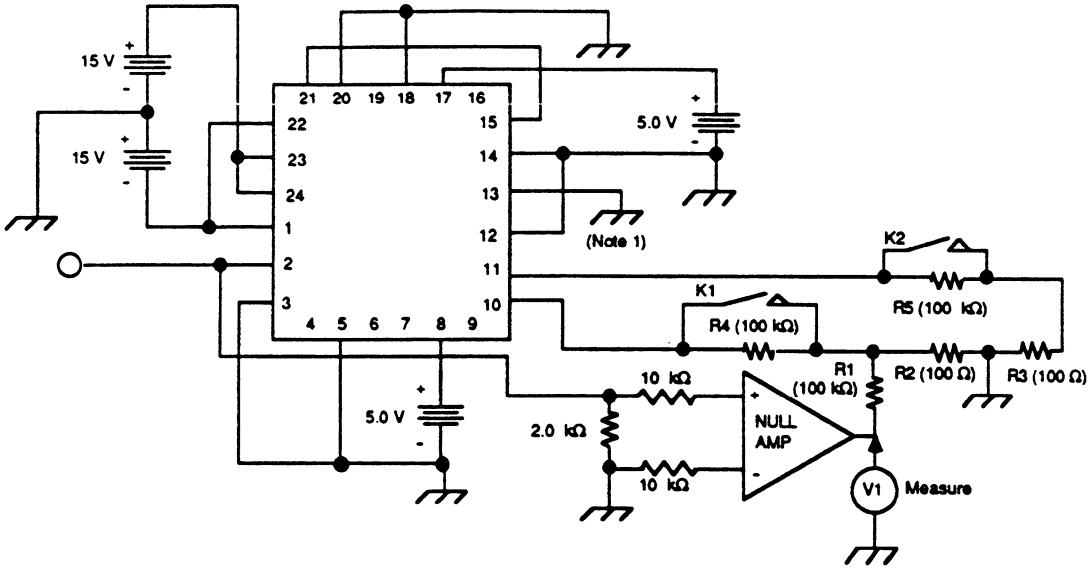


Figure 8. Input Offset Voltage Test Circuit

Test Circuits
(Continued)



Test Condition	V1 Measurement
K1 and K2 Closed	VCASE1
K1 Open, K2 Closed	VCASE2
K1 Closed, K2 Open	VCASE3

$$IB(-) = \frac{VCASE1 - VCASE2}{R4\left[\frac{R2 - R1}{R1}\right]}$$

INPUT BIAS CURRENT (IB)

$$IB = \frac{IB(-) + IB(+)}{2}$$

$$IB(+) = \frac{VCASE1 - VCASE3}{R5\left[\frac{R2 - R1}{R1}\right]}$$

Figure 9. Input Bias Current Test Circuit

Test Circuits (Continued)

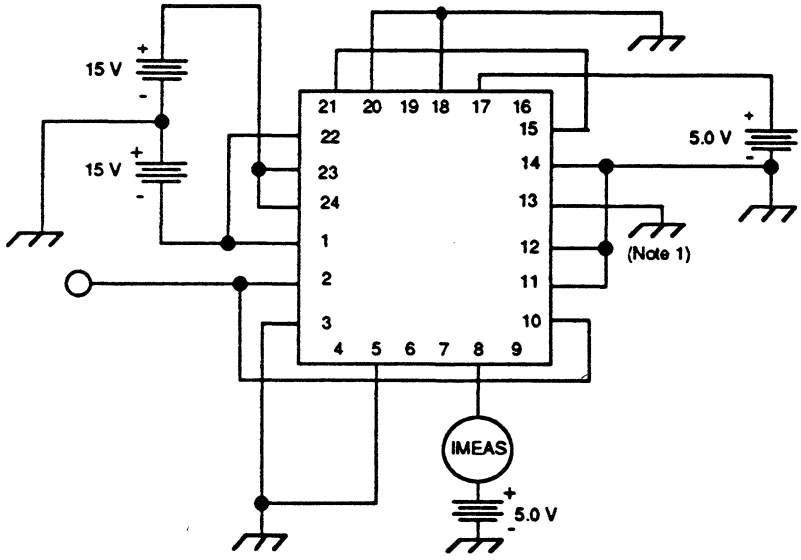


Figure 10. Logic Input Current Test Circuit

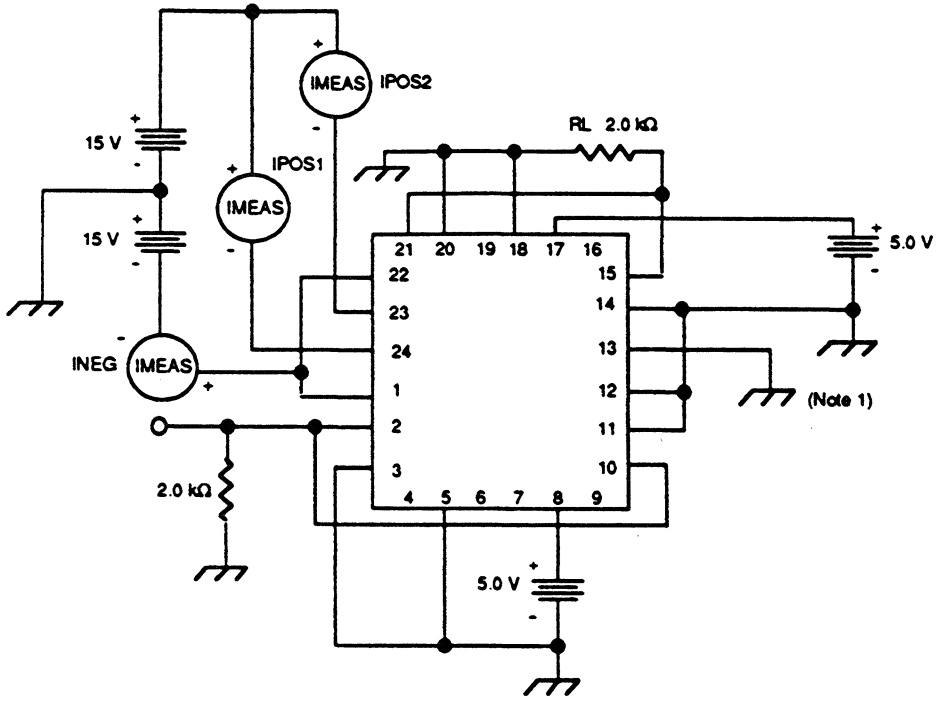


Figure 11. Power Supply Current Test Circuit

Test Circuits
(Continued)

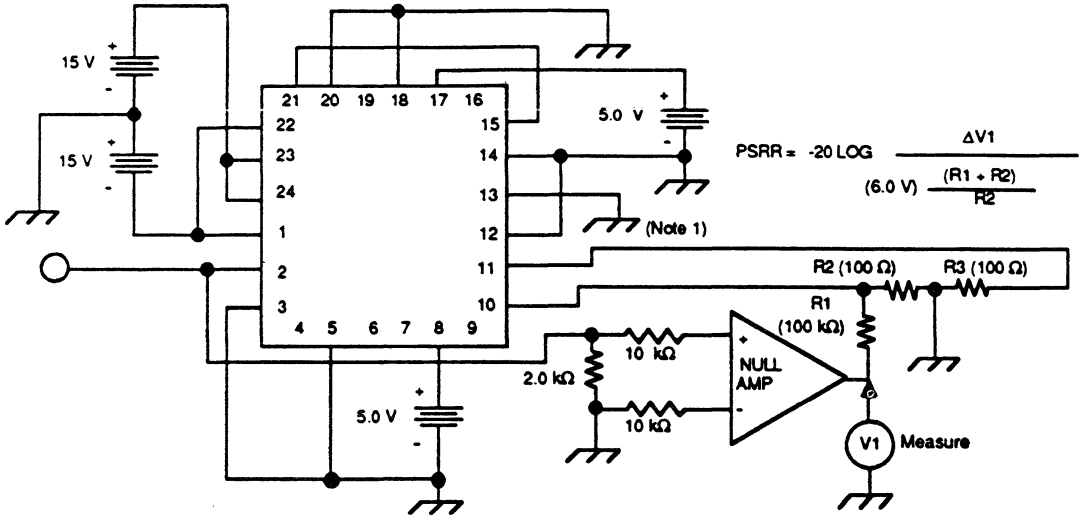


Figure 12. Power Supply Rejection Ratio Test Circuit

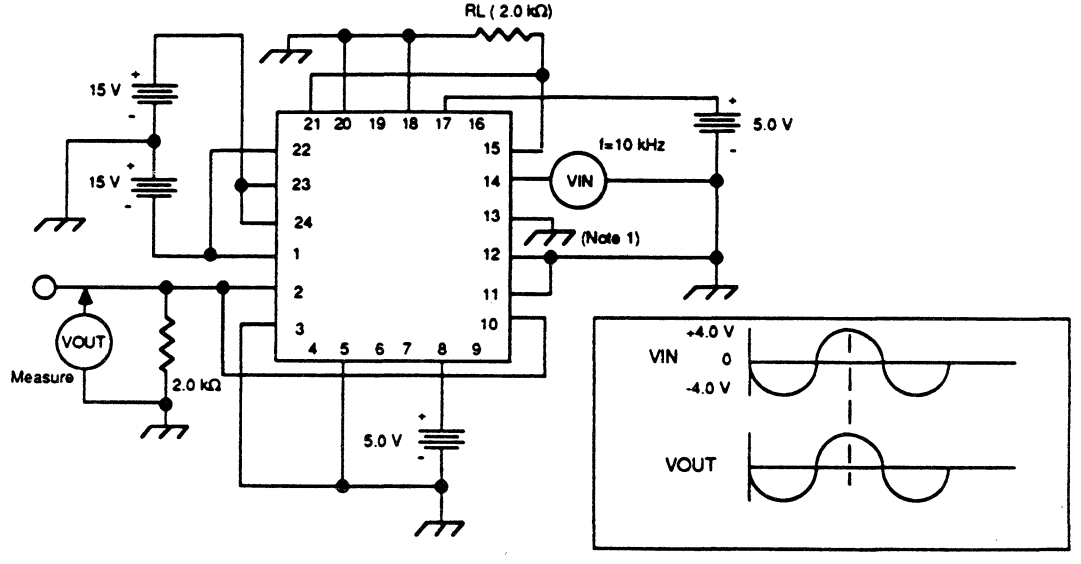


Figure 13. Crosstalk Test Circuit

Functional Operation

Sample-and-hold circuits are devices which store analog information and reduce the aperture time (Figure 15) of an A/D converter. These devices are simply voltage-memory devices in which an input voltage is acquired and then stored on a high-quality capacitor.

There are two modes of operation for a sample-and-hold device:

1. Sample (or Tracking) mode - SW1 is closed.
2. Hold mode - SW1 is open.

Sample-and-hold devices are usually operated in one of two basic methods. Devices can continuously track the input signal and be switched into the hold mode only at certain specified times, thereby spending most of the time in the tracking mode. This is an example of sample-and-holds employed as a deglitcher at the output of a D/A converter.

Conversely, devices can stay in the hold mode most of the time and go to the sample mode just to acquire a new input signal level. This is the case for sample-and-hold devices used in a data acquisition system following a multiplexer.

Figure 14 shows the basic functions of the LB1127AAK device. It consists of a high-performance operational amplifier (A1) in series with a low-leakage analog switch (SW1) and a high-impedance input unity gain amplifier (A2).

An internal holding capacitor (CH-int) is connected to the switch output. Also, provisions have been made so that an external holding capacitor (CH-ext) may be connected in parallel to the internal holding capacitor. The addition of external capacitance will reduce the droop rate when long hold times and high accuracy are required.

When the low-leakage switch is closed, the device operates as an operational amplifier, and any of the standard op-amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

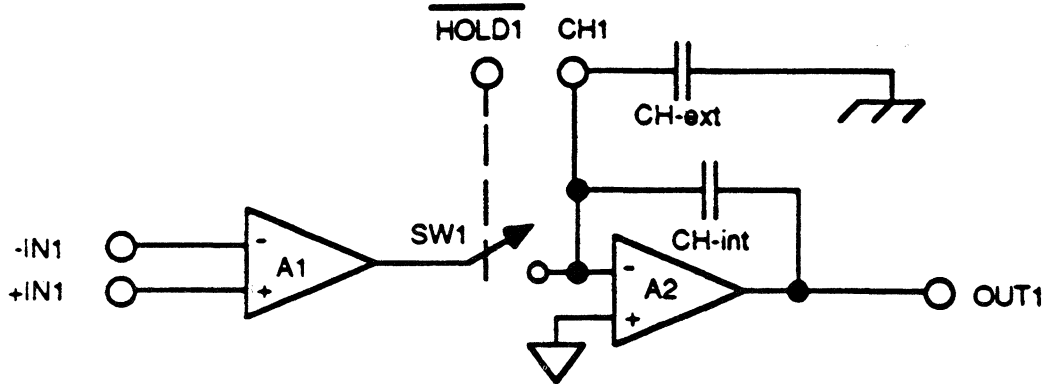


Figure 14. Simplified Functional Operation

Definition of Terms

Acquisition Time (Figure 2) is probably the most important parameter in characterizing sample-and-hold performance. The definition is similar to that for settling time for an amplifier. It is the time required, after the sample command is given, for the output of the device to reach its final value (within ±0.01%). Included are switch-delay time, the slewing interval and settling time.

Several hold-mode specifications are also important. Hold-mode droop **(Droop Rate)** is the output voltage charge per unit time when the switch (SW1) is opened. This droop is caused by the leakage currents of the hold capacitors and switch, and the output amplifier bias current. Hold-mode feedthrough **(Feedthrough Voltage)** is the amount of input signal transferred to the output when the switch is open. It is measured (Figure 2) with a sinusoidal input signal and is caused by capacitive coupling.

The most critical phase of sample-hold operation is the transition from the sample-mode to the hold-mode. Sample-to-hold offset error **(Pedestal Error Voltage)** is the change in output voltage from the sample-mode to the hold-mode, with a constant input voltage (Figure 2). It is caused by the switch transferring charge onto the hold capacitor as it turns off.

Aperture Delay is the time elapsed from the hold command to when the switch (SW1) actually opens. **Aperture jitter** (or aperture uncertainty) is the time variation, from device to device, of the aperture delay.

Sample-and-hold circuits are simple in concept, but are difficult to fully understand and apply. Their operation is full of subtleties and subjective interpretations. Therefore, they must be carefully selected and tested in given applications.

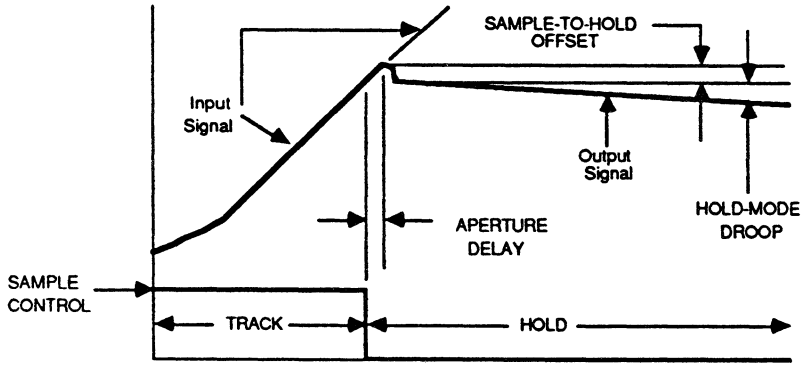
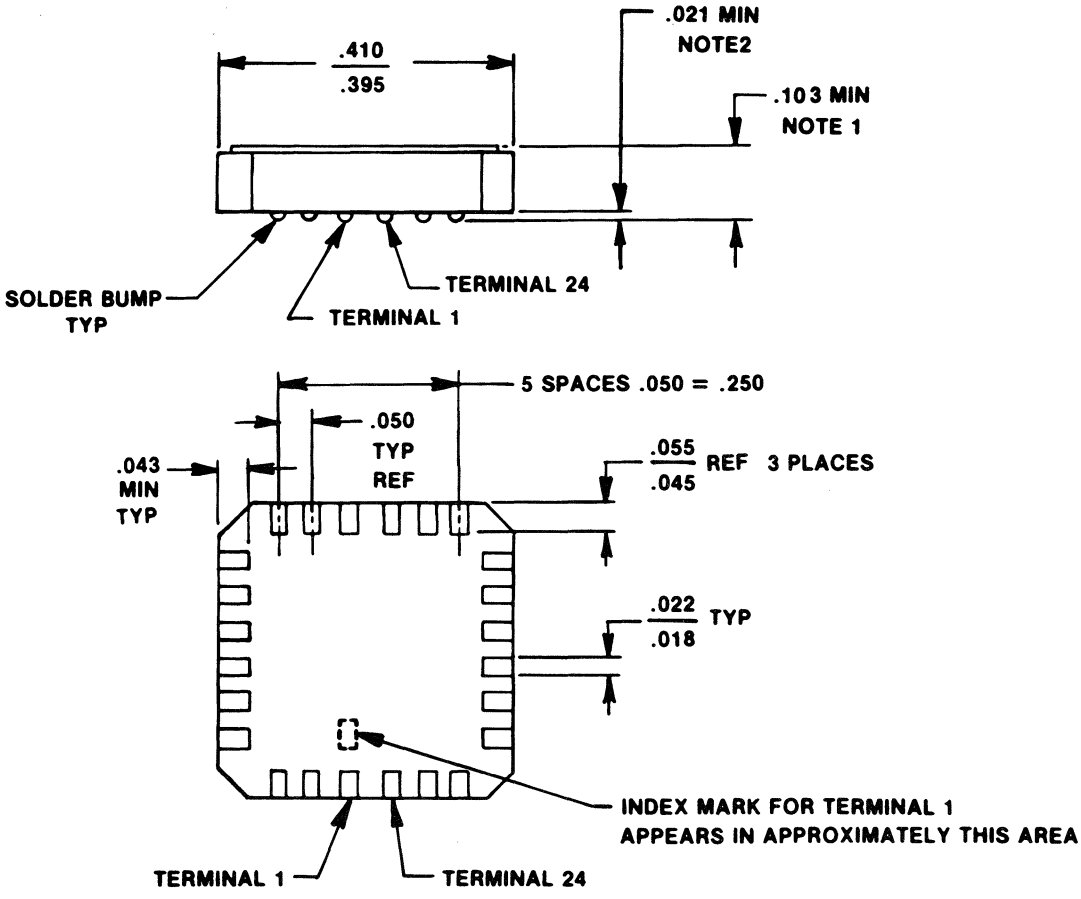


Figure 15. Several Sample-Hold Characteristics

Outline Drawing

(Dimensions in Inches)



Ordering Information

Device	Comcode
LB1127AAK	104412622

Description

The LS1119AC device is a general purpose phase-locked loop (PLL) characterized by a wide frequency range and low power consumption. It is suitable for applications in thermally unstable environments. The PLL is designed to operate in the 10 Hz to 10 MHz frequency range. At a frequency of 100 kHz, it exhibits excellent thermal stability of less than ±50 ppm/°C.

The PLL circuit consists of a voltage-controlled oscillator (VCO) and phase comparator (PC), each functionally isolated from the other. The VCO output is TTL-compatible (open collector).

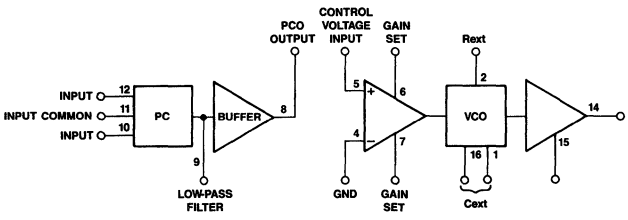
The device operates with bipolar power supplies over a range of ±5.0 to ±15 V. The supply voltages need not be symmetrical. The supply current drain is controlled by an external resistor (Rf); typical current drain is less than 8.0 mA with a resistance value of 2.5 k ohm.

In application, the circuit is used for frequency synthesis, signal conditioning, clock extraction, and FM demodulation. It is available in a 16-pin plastic DIP.

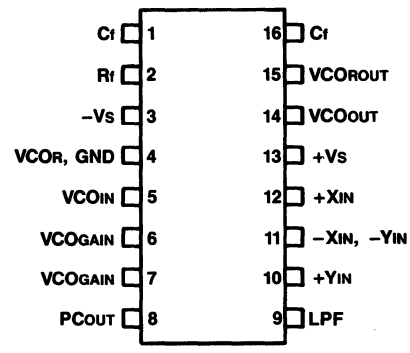
Features

- Wide frequency range
- Applications in thermally unstable environments
- Low power consumption
- TTL-compatible
- 10 Hz to 10 MHz operation
- Low temperature coefficient (±50 ppm/°C)
- Typical supply current < 8 mA

Functional Diagram



Pin Diagram



Maximum Ratings*

Rating	Value	Unit
Power Supply Voltage (V+) (V−)	30	V
Power Supply Current (+I_{PS})	9.0	mA
Storage Temperature Range (T_{stg})	−40 to +125	°C
Ambient Operating Temperature Range	0 to +60	°C
Power Dissipation**	400	mW

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

* The ratings specified are limiting values under all variations of circuit and environmental conditions beyond which the serviceability of the device may be impaired from the viewpoint of life and satisfactory performance. Ratings, as such, do not constitute a set of operating conditions and all values may not, therefore, be attained simultaneously.

** Derate at 4.0 mW/°C for temperature within the range of +25°C to +125°C.

Pin Descriptions

Pin Number	Name/Function	Pin Number	Name/Function
1	Timing Capacitor	9	Low-Pass Filter
2	Timing Resistor	10	+Y Input
3	−Vs	11	−X and −Y Inputs
4	VCO Reference	12	+X Input
5	VCO Input	13	+Vs
6	VCO Gain	14	VCO Output
7	VCO Gain	15	VCO Output Reference
8	PC Output	16	Timing Capacitor

Electrical Characteristics

(T_A = 25°C)

Characteristics and Conditions*		Symbol	Min	Max	Unit
Phase Comparator					
Input Offset Voltage		V_{IO}	—	±5.0	mV
Input Bias Current		I_{IB}	—	4.5	μA
Input Offset Current		I_{IO}	—	±1.0	μA
Maximum Output Current	Lead 9 (Test Circuit 3)	I_{OM}	±350	±450	μA
Common-Mode Voltage Range	X Input	CMVR	−13.2 +12.7	—	V
	Y Input		−13.2 +13.2	—	V
Voltage Follower					
Output Offset Voltage		V_{OO}	—	±15.0	mV
Maximum Output Voltage Swing (Test Circuit #4)		V_{om}	±13.5 −13.0	—	V
Voltage-Controlled Oscillator					
Free-Running Frequency (Test Circuit 2)		f_{FR}	0.95fo	1.05fo	Hz
VCO Sensitivity	R_G = 10 kΩ between Leads 6 and 7	S_{VCO}	60	84	%/V
Power Supply Rejection Ratio	△Vs = 10 V	PSRR	—	±0.1	%/V
Common-Mode Voltage Range		CMVR	−13.2 +12.5	—	V
Low-Level Output Voltage	Io = −5.0 mA	V_{OL}(14.15)	0.2	1.0	V
VCO Range		△f_{FR}	±40.0	±62	%
General					
Output Voltage Reference Range		V_{ORR}	−11.5 +12.5	—	V
Power Supply Current (Test Circuit 1)		+I_{PS}	5.0	9.0	mA

*Characteristics are certified by appropriate manufacturing test limits. Vs = ±15 V, Rf = 2.5 kΩ, Cf = 0.2 μF unless otherwise specified.

Test Circuits

Resistor values selected for use in all test circuits are characterized by a nominal ±1% tolerance; capacitors ±10%.

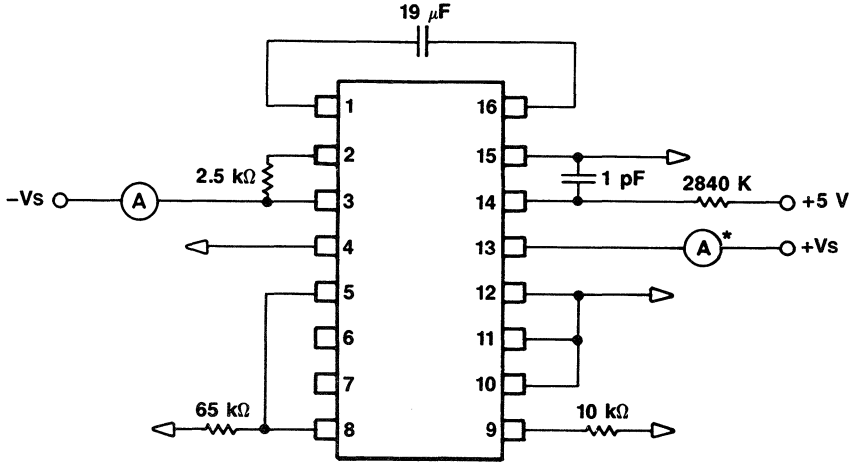
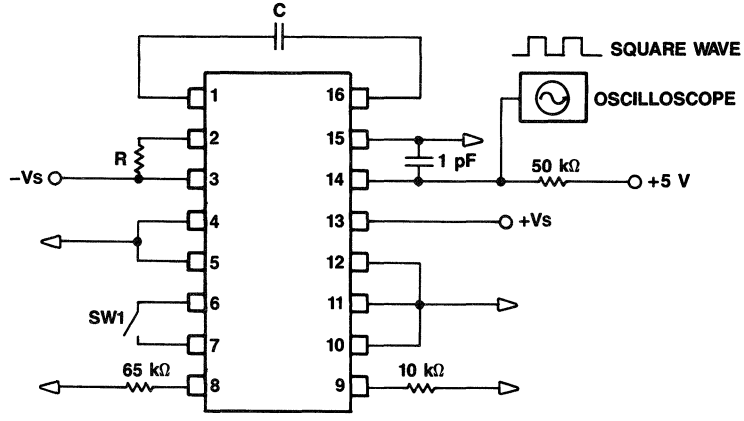


Figure 1. Power Supply Current (±IPS)



Notes: 1. $f_{RF} = \frac{1}{2RC}$ (e.g., R = 2.5 kΩ, C = 0.2 μF, f_{FR} = 1 kHz)

2. VCO—Power Supply Rejection Ratio (PSRR):
   Gvs = ±15 Volts, Close K1; Output Frequency = FO
   Gvs = ±10 Volts, Close K1; Output Frequency = F1

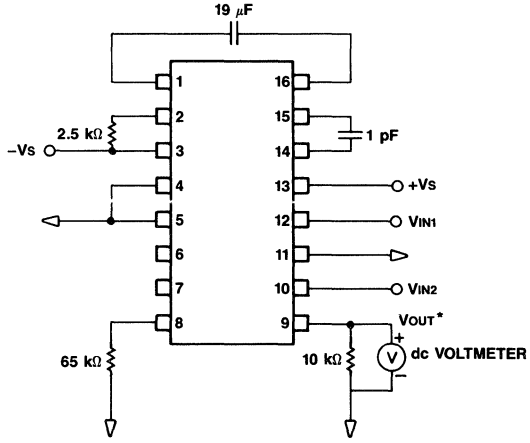
3. $PSRR = \left| \frac{F1\text{-}F0}{FO} \right|_{\Delta V \text{ supply}}$

   △V supply = 10 volts
   R = 2.5 kΩ
   C = 0.2 μF

4. Units = $\frac{\%}{V}$

Figure 2. VCO Free Running Frequency (Notes 1-4)

Test Circuits (Continued)

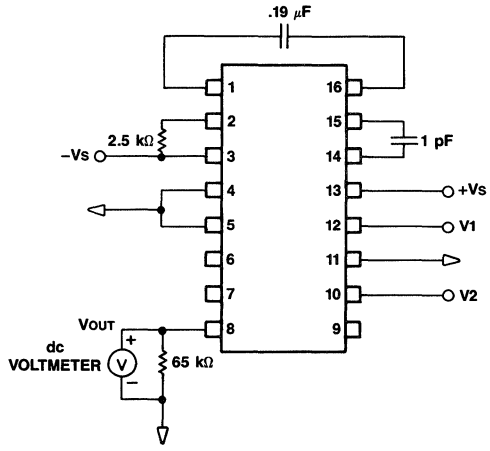


Measure VOUT under the following conditions

VIN1	VIN2
+.5V	+.5V
−.5V	−.5V
+.5V	−.5V
−.5V	+.5V

$$I_{MAX} = \frac{Vout}{10\ k\Omega}$$

Figure 3. Phase Comparator: Maximum Output Current



1. Negative voltage swing
   V1 = +.5 volts
   V2 = −.5 volts
   Vout = − Vos

2. Positive voltage swing
   V1 = +.5 volts
   V2 = +.5 volts
   Vout = +Vos

Figure 4. Voltage Follower — Maximum Voltage Swing (±Vos)

Applications

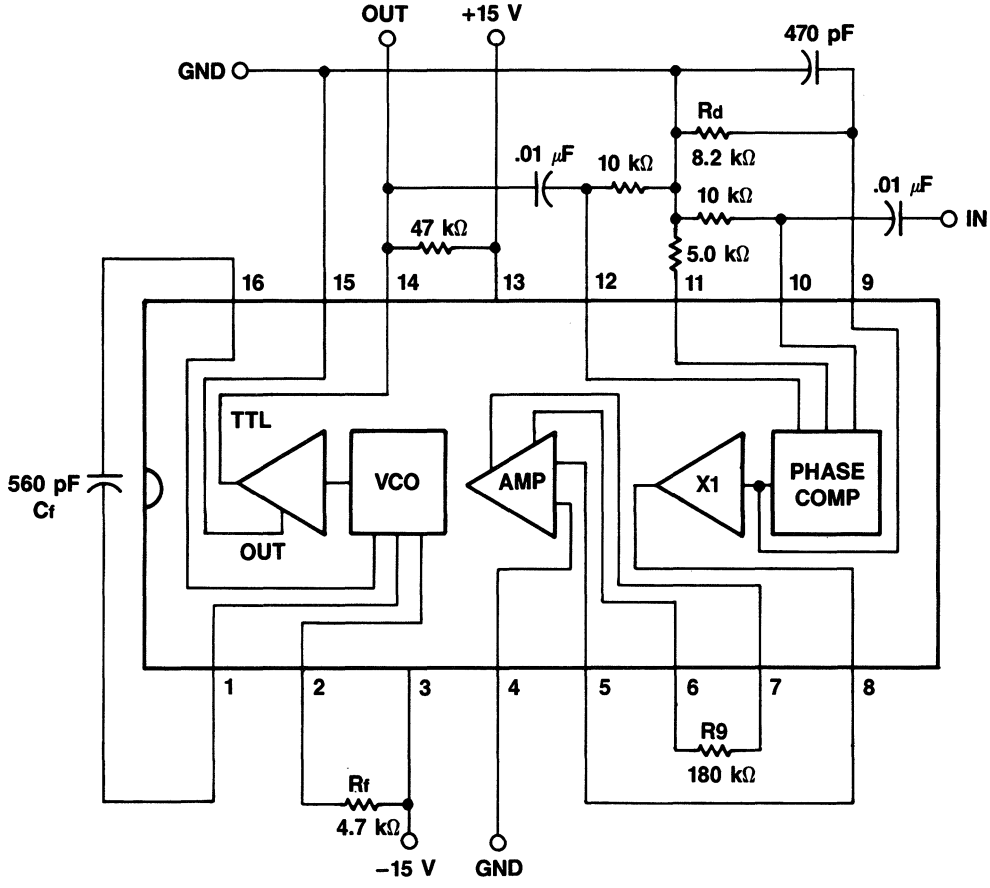


Figure 5. 200 kHz Synchronizer Application

Figure 5 shows connections and external components for a synchronizer application of this device. The external components are chosen according to the following equations and descriptions:

Voltage-Controlled Oscillator (VCO)

The free-running frequency (f_{FR}) of the VCO is determined by the timing resistor (R_t) and the timing capacitor (C_t).

$$f_{FR} \cong f_o = \left(\frac{1}{2R_tC_t} \right) \text{Hz}$$

Applications (Continued)

The oscillator follows this relation very closely at frequencies well below its upper limit, typically within ±3 percent for $R_f = 2500\ \Omega$. R_f also sets up the bias currents for the entire device. At full bias current, typically 7.5 mA for $R_f = 2500\ \Omega$ temperature stability and high-frequency performance are optimized. Higher values of R_f, up to 25 kΩ, may be used to reduce the power consumption but at the expense of a slight degradation in performance.

The VCO sweep gain (G_{SW}), defined as the percent change in frequency per volt of input, can be controlled by the gain resistor (R_G).

$$G_{SW} \cong 268 \left[\frac{R_f}{R_G} \right] \%\triangle f/V$$

This expression is only accurate for sweep gains $< 500\%\ \triangle f/V$, since actual performance asymptotically approaches $800\%\triangle f/V$ as R_G approaches zero.

VCO gain (K_o), defined as the change in frequency per volt of input:

$$K_o \cong \frac{1.34}{R_G C_f} \text{ Hz/V}$$

In normal operation, the VCO can be swept ±50 percent about f_{FR}.

The output of the VCO is an open collector compatible with TTL logic. For improved performance a 47 kΩ pull-up resistor may be used between the VCO OUT pin and the positive voltage.

The VCO output is externally ac coupled to the PC input. The level of the input to the PC should be kept below ~2.5 volts peak to peak. This may require an attenuation of the VCO output voltage (in Figure 3, achieved by the 47 kΩ pull-up resistor, in conjunction with the 10 kΩ resistor, from X to ground). The VCO frequency can be phase-locked with a low-level, but highly stable, reference signal which may have a low S/N ratio. The VCO output reproduces the reference signal frequency with the same accuracy, but at much higher power level. This output is referenced to ground, but can be referenced anywhere between −11.5 and 12.5 volts (V_s^- +3.5 Vdc, V_s^+ −2.5 Vdc).

Phase Comparator (PC)

The X and Y inputs share a common reference, which in most applications is returned to ground. The optional 5 kΩ resistor from this lead to ground equalizes voltage drops caused by input bias currents.

The PC current output is converted to a voltage by external resistance (R_d) from the low-pass filter (LPF) lead to ground. The gain of the PC, a function of this resistor is:

$$K_d \cong 0.51 \left[\frac{R_d}{R_f} \right] \text{ volts per radian}$$

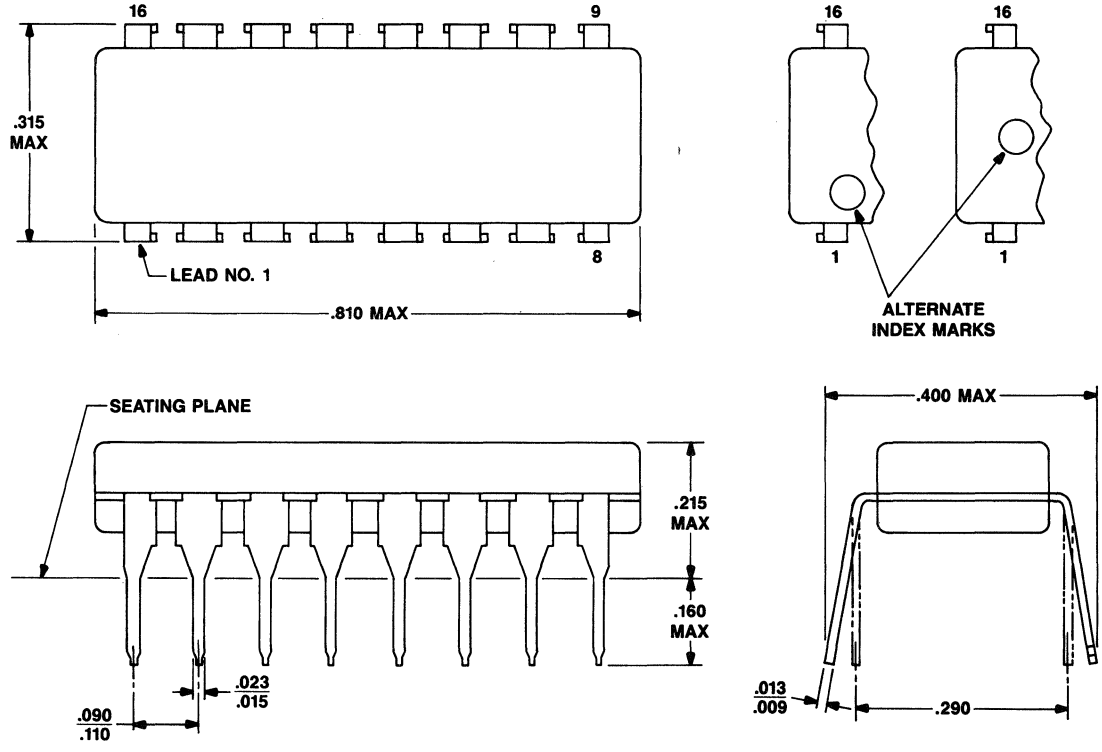
The signal appearing at the LPF lead enters a unity-gain voltage follower. The low output impedance of the follower greatly enhances the usefulness of the PC output and simplifies system interfacing, especially for additional signal processing between the PC and the VCO.

Filters

In most PLL applications, an LPF is needed between the phase comparator output and the VCO input. The characteristics of this filter and the loop gain of the PLL determine the lock range and capture range. Typically, the filter consists of a capacitor in series with a resistor, both in parallel with PC gain resistor. Alternatively, the low-pass filter, either active or passive, can be inserted between the PC and the VCO. It is generally desirable, however, to perform some of the filtering action directly at the LPF lead to keep the ripple voltage swings at that point within the allowable voltage range.

Outline Drawing

(Dimensions in Inches)



Ordering Information

Device	Comcode
LS1119AC	104412002

Description

The LS1120AC is a phase-locked loop (PLL) intended for use as a tone decoder. The circuit contains a phase comparator (PC), a window detector, a current-controlled oscillator (CCO), a quadrature phase comparator, an internal voltage regulator, ON and OFF timers, and a TTL-compatible output.

This circuit is designed for use with power supplies from 9.0 to 30 volts. The free-running frequency (f_{FR}), determined by an external resistor (R_f) and capacitor (C_f), can range up to 1.0 MHz. The ON timer, which requires an external capacitor (C_{ON}), produces a delay between capture of an incoming signal and the actual indication, at the output, that capture has been achieved. Similarly, the OFF timer, which also uses an external capacitor (C_{OFF}), creates a delay between loss of capture and output indication.

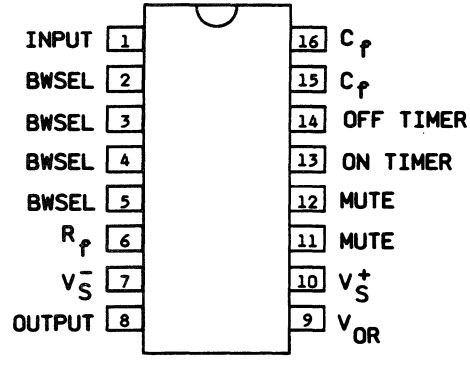
Features

- Fast capture time (< 10 cycles)
- Adjustable bandwidth
- Variable on and off delays
- Operation over frequency range to 1.0 MHz
- TTL-compatible output
- Operates from 9.0- to 30-volt power supply
- Excellent temperature coefficient is typically < 100 ppm/°C for frequencies < 10 kHz
- 16-pin plastic DIP

Applications

- Touch-tone decoding
- Wireless communications system controls
- Precision oscillator
- Ultrasonic detection
- Frequency monitor
- Pulse generator

Pin Diagram



Maximum Ratings (At T_A = 25°C unless otherwise specified)	
Power-Supply Voltage	30 V
Power-Supply Current	12 mA
Power Dissipation	400 mW
Storage Temperature	−40 to +125°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Description

(See Pin Diagram)

Pin	Symbol	Name/Function
1	INPUT	
2 3 4 5	BWSEL BWSEL BWSEL BWSEL	These pins are used to select the bandwidth temperature stabilization across the low-pass filter resistor (BWSEL = Bandwidth Select).
6	R_f	This pin is used for the external frequency component of the CCO.
7	V_S^-	The most negative supply voltage pin.
8	OUTPUT	
9	V_{OR}	Output reference voltage
10	V_S^+	The most positive supply voltage pin.
11 12	MUTE MUTE	These pins allow retrofit into second order tone-decoder phase-locked loops.
13 14	ON Timer OFF Timer	These pins are used to establish the external timing of the timer output driver.
15 16	C_f C_f	These pins are used for the external frequency component of the CCO.

Electrical Characteristics

(T_A = 25°C)

Parameter and Conditions			Symbol	Min	Max	Unit
Maximum Bandwidth			BW_{MAX}	±5.0%	±10%	
Output Voltage		High	V_{OH}	V_{OR}–0.5	—	V
		Low (I_O = 10 mA)	V_{OL}	—	0.4	
Free-Running Frequency			f_{FR}	0.975 f_O	1.025 f_O	Hz
Supply Current	V_{OH}	$V_{(10,7)}$ = $V_{(9,7)}$ = 12 V	I_{PS}	1.4	2.6	mA
		$V_{(10,7)}$ = $V_{(9,7)}$ = 30 V		2.0	4.0	
	V_{OL}	$V_{(10,7)}$ = $V_{(9,7)}$ = 12 V		2.5	7.0	
		$V_{(10,7)}$ = 30 V		1.5	12	
ON Timer Current		In Band	I_{ON}	−6.0	−16	μA
		Muted		27	47	
		No Signal		10	18	
OFF Timer Current		In Band	I_{OFF}	−50	−84	
		Muted		24	42	

Applications

The Pin Diagram shows a functional representation of the LS1120AC Phase-Locked Loop/Tone Decoder. The external components should be chosen according to the following equations and descriptions.

The free-running frequency of the CCO, established by external components, is given to within ±3.0 percent by $f_o = 1/(12\ R_f C_f)$. Performance is optimized by R_f values between 1.4 kΩ and 2.6 kΩ. The CCO design ensures low temperature drift (< 100 ppm/°C typically), assuming no contribution from the external timing elements. The on-chip voltage regulator maintains this level of performance over the full 9.0- to 30-volt power-supply range (typical CCO stability < 150 ppm/V).

Fast capture (within 10 cycles of incoming tone) is achieved by a first-order locking loop rather than the more conventional second-order loop (with the filter components connected to ground).

The window detector monitors the filtered error voltage appearing across the low-pass filter resistor (R_{LPF}) and inhibits the output if the error is large enough to signify an out-of-band input signal. Bandwidth is thus established to a first order by the value of R_{LPF} and to a second order by that of the low-pass filter capacitor (C_{LPF}).

The MUTE line, which carries the inhibit signal to the output circuitry in the case of an out-of-band input, must be connected externally by shorting the adjacent "MUTE" leads together. However, by leaving these leads open, and by adding a parallel RC filter from the PC output (lead 4) to ground, the device can be degenerated to a standard second-order loop tone decoder. This allows the achievement of a narrower bandwidth at the expense of longer capture time. Also, it allows the LS1120AC to retrofit into applications that use commercial second-order tone decoder phase-locked loops.

Bandwidth temperature stabilization is achieved by keeping R_{LPF} on the chip, with taps to permit users to select among bandwidth of ±2.0% (25 kΩ), ±4.0% (13 kΩ), ±6.0% (9.0 kΩ), and ±8.5% (< 4.0 kΩ). Leads 2, 3, 4 and 5 are used to select bandwidth.

With the LS1120AC, intermediate bandwidth values are obtained, as shown in Figure 1 by shunting R_{LPF} with an external resistor. Figure 1 also illustrates the discrepancy between the average of the upper- and lower-band edges and the free-running center frequency. This discrepancy, a function of R_{LPF}, must be compensated for to yield a symmetrical bandwidth. For example, in order to achieve a ±3.0% bandwidth centered at 1.0 kHz, R_f should be trimmed to get a free-running frequency (monitored with an ac-coupled low-capacitance probe at C_f) of 1.005 kHz. As with most PLLs, the loop dynamics of the capture process are difficult to define, but good performance is generally achieved with a low-pass filter capacitor selected so that $C_{LPF} \cong 3\ C_f$.

The quadrature PC enables the tone decoder to distinguish between a "no signal" case and a "centered signal" case, both of which provide zero error signal into the CCO. The quadrature PC multiplies the input with the CCO signal; thus, when an in-band signal is present, the ON timer is enabled and C_{ON} begins charging up. If the signal is lost or shifts out of band, C_{ON} is discharged. When the voltage on C_{ON} exceeds a fixed threshold, C_{OFF} quickly charges past the output threshold to produce a detection signal at the output ("low" state). When the signal is lost, C_{ON} quickly drops below its threshold which causes C_{OFF} to discharge until it crosses the output threshold, resulting in a switch to the no-signal state (output "high"). The equations for the delay times between the loop lock or release and the appropriate output transistions are:

$$T_{ON} = 187\ R_f\ (C_{ON} + C_{OFF}/36)$$
$$T_{OFF} = 57\ R_f\ (C_{OFF} + C_{ON}/2.2)$$

T_{ON} is the delay after loop capture, which itself may take up to 10 cycles of incoming tone.

For $C_{ON} = C$, $T_{ON}/C = 160\ ms/\mu F$.

Since the decoder input is self-biased at $+3\ V_{BE}$, a coupling capacitor, C_c, is generally required. As the input impedance of approximately 20 kΩ is used, a value of $C_c = C_f$ will pass any valid signal with less than 2.0-dB loss ensuring detection for input levels between 100 millivolts and 3.0 volts peak.

Applications
(Continued)

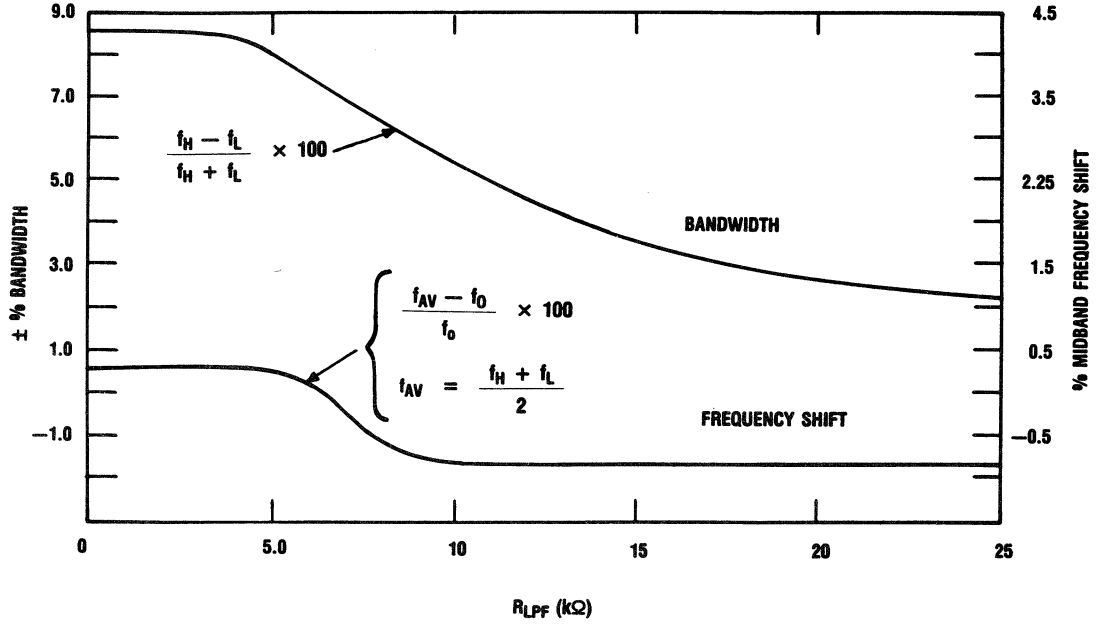


Figure 1. Bandwidth and Midband Frequency Shift vs R_{LPF}

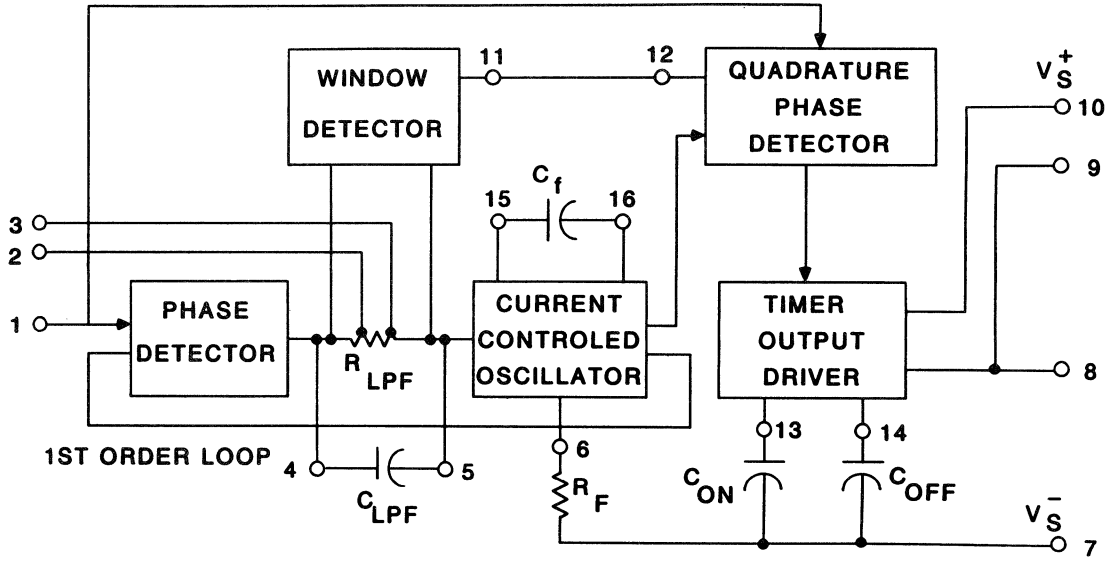
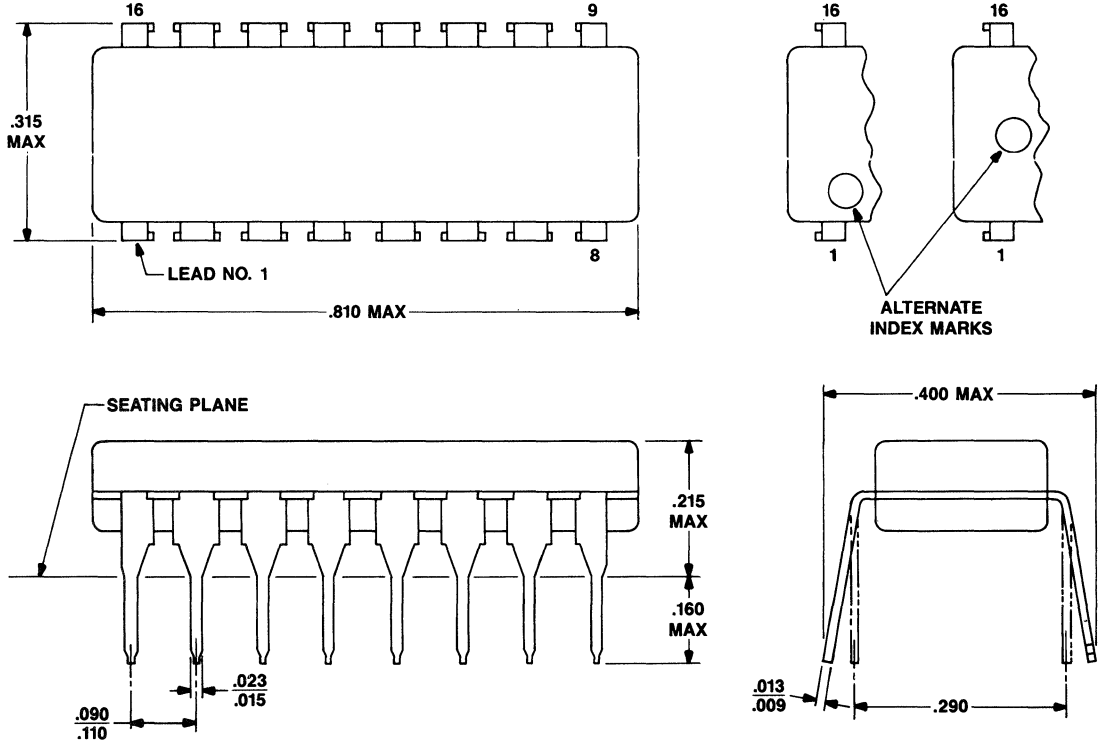


Figure 2. Functional Schematic

Outline Drawing

(Dimensions in Inches)



Ordering Information

Device	Comcode
LS1120AC	104412028

VOLTAGE-CONTROLLED OSCILLATOR — LB1121AC

PRELIMINARY

Description

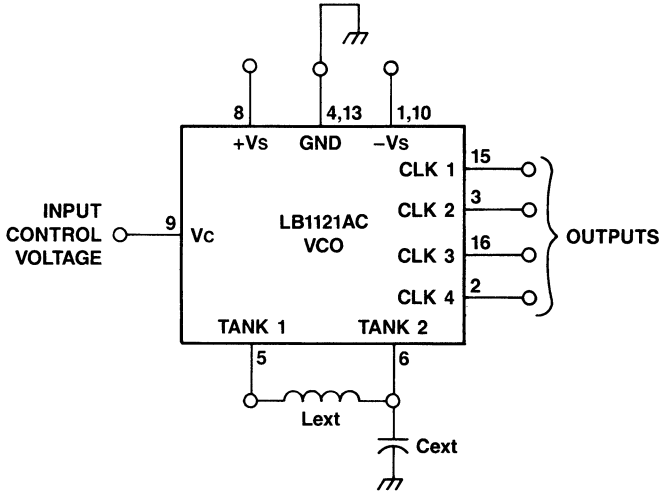
The LB1121AC is a general-purpose voltage-controlled oscillator (VCO) with operating capabilities as high as 70 MHz. It is designed for use in voltage-to-frequency conversion applications, including function generation and signal conditioning.

The device is characterized by superior thermal stability and features four ECL-compatible outputs with relative phases of 0, 90, 180, and 270 degrees. An applied input voltage within the range of ±1.0 V controls the VCO operating frequencies. Two power-supply voltages, + 5.0 and − 5.2 V, are required for operation. The VCO is available in a 16-pin, plastic DIP.

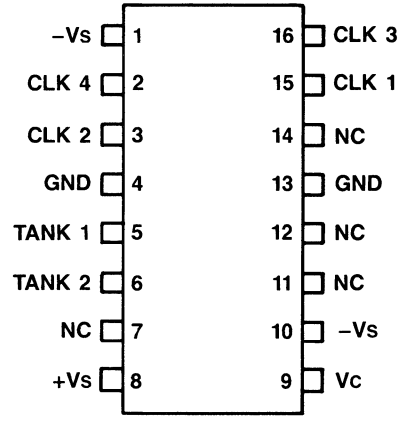
Features

- High frequency operation
- Multiple clock frequency applications (general-purpose VCO)
- Optional phase-shift selection
- Tight VCO control voltage
- Temperature stability
- Operation to 70 MHz
- Four ECL-compatible outputs
- VCO input range, ±1 V

Functional Diagram



Pin Diagram



Maximum Ratings

(T_A = 25°C unless otherwise specified)

Parameter	Rating	Unit
Positive Power Supply Voltage	5.5	V
Negative Power Supply Voltage	−5.7	V
Power Dissipation	670	mW
Storage Temperature	−40 to +125	°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions

Pin	Symbol	Name/Function
1	−Vs	−5.2 V negative supply
2	CLK 4	Clock output, 270° relative phase
3	CLK 2	Clock output, 90° relative phase
4	GND	Ground connection
5	TANK 1	External tank circuit inductor connection
6	TANK 2	External tank circuit inductor-capacitor connection
7	NC	No connection
8	+Vs	+5.0 V positive supply
9	Vc	Control voltage input
10	−Vs	−5.2 V negative supply
11	NC	No connection
12	NC	No connection
13	GND	Ground connection
14	NC	No connection
15	CLK 1	Clock output, 0° relative phase
16	CLK 3	Clock output, 180° relative phase

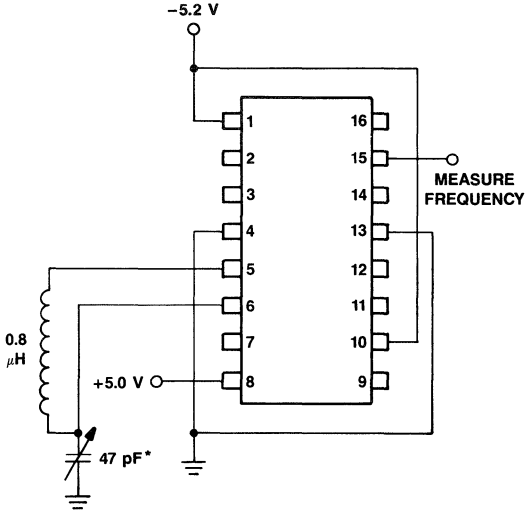
Electrical Characteristics (T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic and Conditions	Symbol	Min	Typ	Max	Unit
Positive Power Supply Current = 5.0 V	$+V_{PS}$	15	19	24	mA
Negative Power Supply Current = −5.2 V	$-V_{PS}$	40	46	54	
Free Running Frequency	f_{FR}	—	20.9	—	MHz
Frequency w/Input Voltage = 0	f_{VIN}	—	20	—	
Frequency Deviation w/Input Voltage = 1.0 V	fd	0.6	0.9	1.2	MHz/V
Frequency Deviation w/Input Voltage = −1.0 V	fd	−0.6	−1.1	−1.2	
Output Clock Level (High) w/Input = 0	CLK_{OH}	−0.7	−0.8	−1.0	V
Output Clock Level (Low) w/Input = 0	CLK_{OL}	−1.3	−1.8	−2.5	
Clock Amplitude	—	0.5	1.0	1.75	
Clock Duty Cycle w/Input = 0	—	35	50	65	%
VCO Input Bias Current w/Input = 0 V	I_{IB}	—	1.2	—	μA
VCO Input Bias Current w/Input = 1.0 V	I_{IB}	0.3	−0.2	−1.0	
VCO Input Bias Current w/Input = −1.0 V	I_{IB}	0.3	−2.4	−15	
Power Supply Rejection	PRR	—	—	0.07	%△P/V

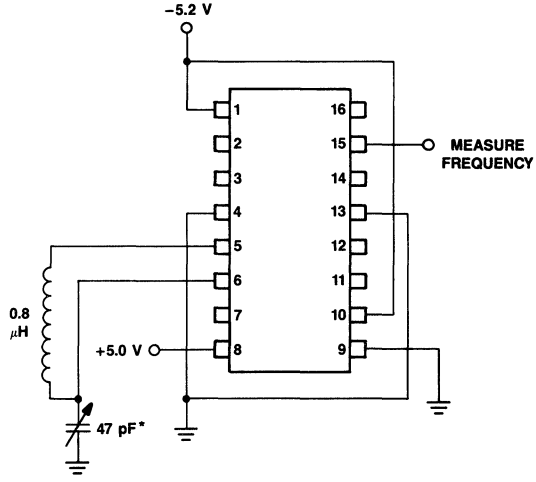
Test Circuits (All unconnected pins are floating.)

Resistor values selected for use in all test circuits are characterized by a nominal ±1% tolerance; capacitors, ±10%.



* Capacitor should be adjusted so the resonant frequency of the tank circuit (including lead length, etc.) is nominally 20 MHz.

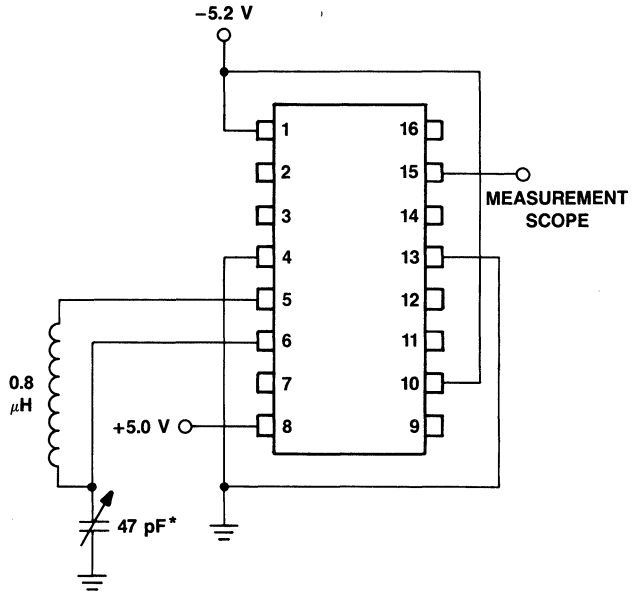
Figure 1. Free-Running Frequency

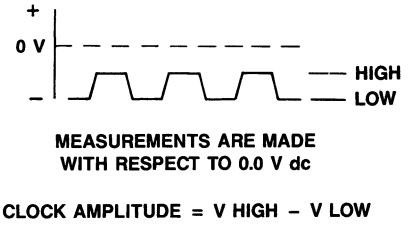


* Capacitor should be adjusted so the resonant frequency of the tank circuit (including lead length, etc.) is nominally 20 MHz.

Figure 2. Frequency with Vin = 0.0 V

Test Circuits (Continued)





* Capacitor should be adjusted so the resonant frequency of the tank circuit (including lead length, etc.) is nominally 20 MHz.

Figure 3. Clock Level High and Low; Clock Amplitude

Characteristic Curves

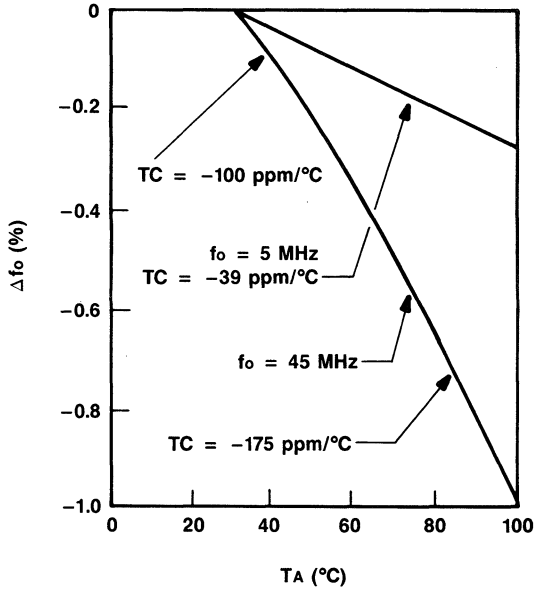
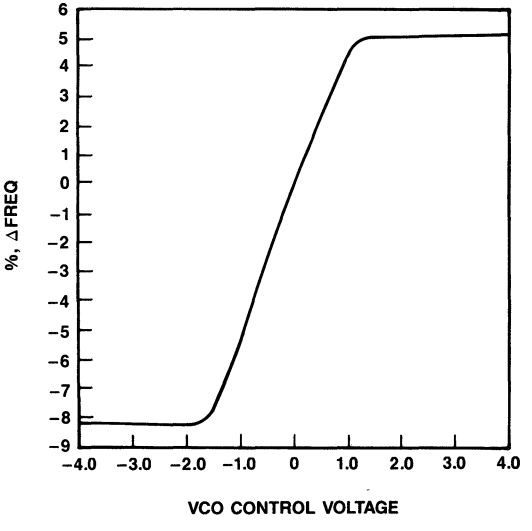


Figure 4. Typical Temperature Coefficient



* To eliminate variations, devices are tested and tightly controlled using a control voltage of ±1 V.

Figure 5. VCO Control Voltage* vs. Percent Change in Frequency

Application

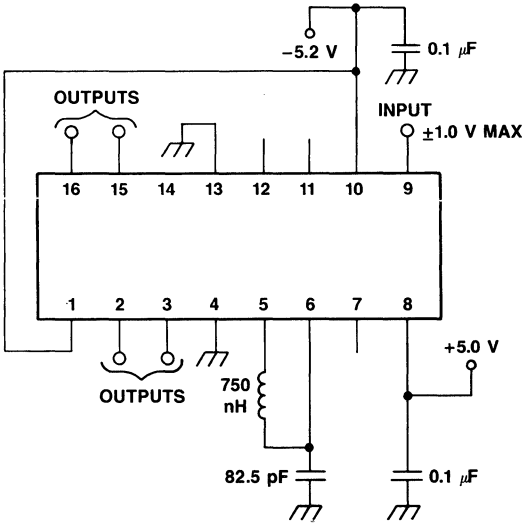
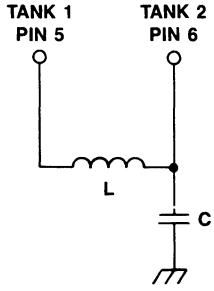


Figure 6. Typical VCO Configuration for Operation at 20 MHz



$$Q = 10 = \frac{1}{R}\sqrt{\frac{L}{C}}$$

WHERE R = 10 Ω ON CHIP

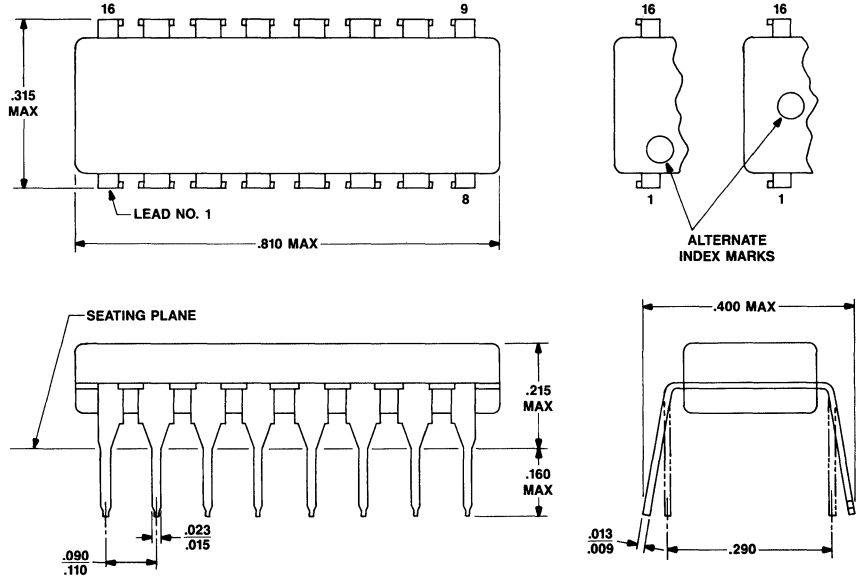
$$f = \frac{1}{2\pi\sqrt{LC}}$$

f	L	C
50 MHz	300 nH	30 pF
20 MHz	800 nH	80 pF
5 MHz	3 μH	300 pF

Figure 7. External Connections for Oscillator

Outline Drawing

(Dimensions in Inches)



Ordering Information

Device	Comcode
LB1121AC	104411772

Description

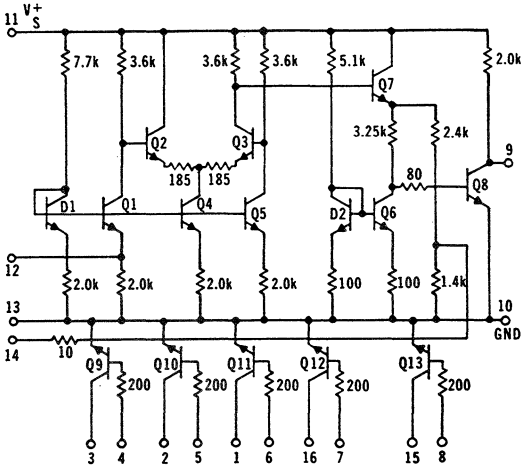
The LS1122AC Oscillator, when used with an external crystal, functions as a general-purpose oscillator at frequencies up to 2 MHz.

This device will provide a symmetcial (typically ±10%) square wave output suitable for driving integrated logic circuits. Five on-chip transistors are provided which can be used as Logic buffers or to boost drive currents.

Features

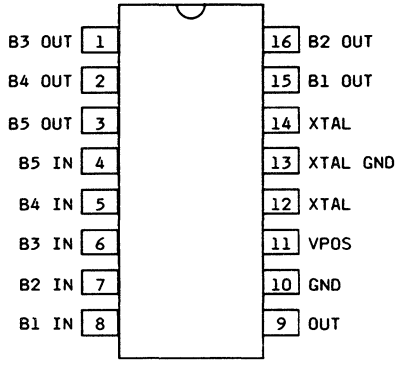
- TTL-compatible
- Symmetrical square wave output
- 16-pin plastic DIP

Functional Diagram



Note: All resistance values are in ohms.

Pin Diagram



Maximum Ratings (At T_A = 25°C unless otherwise specified)	
Power-Supply Voltage	10 V
Power Dissipation	180 mW
Storage Temperature Range	−40 to +125°C
Operating Temperature Range	0 to 60°C
Pin Soldering Temperature (t = 15 s)	300°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Description

Pin	Symbol	Name/Function
1	B3OUT	Output Buffer 3
2	B4OUT	Output Buffer 4
3	B5OUT	Output Buffer 5
4	B5IN	Input Buffer 5
5	B4IN	Input Buffer 4
6	B3IN	Input Buffer 3
7	B2IN	Input Buffer 2
8	B1IN	Input Buffer 1
9	OUT	Oscillator Output
10	GND	Ground
11	VPOS	The most positive supply-voltage is connected to this pin.
12	XTAL	Crystal
13	XTAL GND	Crystal Ground
14	XTAL	Crystal
15	B1OUT	Output Buffer 1
16	B2OUT	Output Buffer 2

Electrical Characteristics (T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic and Test Condition		Min	Typ	Max	Unit
Cutoff Voltage (Figure 1)		7.8	—	—	V
Saturation Voltage (Figure 1)		0.05	—	0.40	
Amplifier Output Resistance ($V_{11, 10}$ = 8.0 V)		0.8	—	1.2	kΩ
Amplifier Transimpedance ($V_{11, 10}$ = 4.5 V)		3.0	—	9.0	
Output Load Resistance		1.5	—	—	
For All Five Buffer Transistors					
Breakdown Voltage (Figure 2)		10	—	—	V
Saturation Voltage	(Figure 3)	0.05	—	0.35	
	(Figure 4)	0.6	—	1.0	
Leakage Current	(Figure 5)	—		1.0	μA

Test Circuits

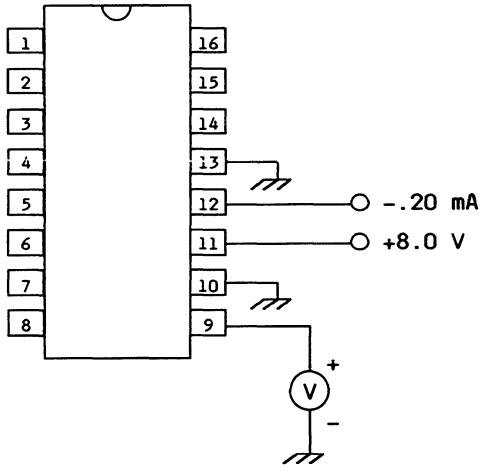


Figure 1. Cutoff Voltage and Collector-Emitter Saturation Voltage Test Circuit

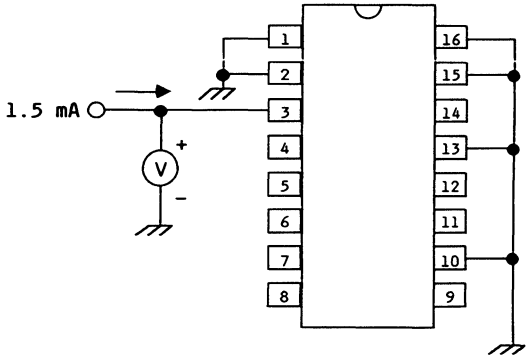


Figure 2. Breakdown Voltage (V_{BEO}) Test Circuit

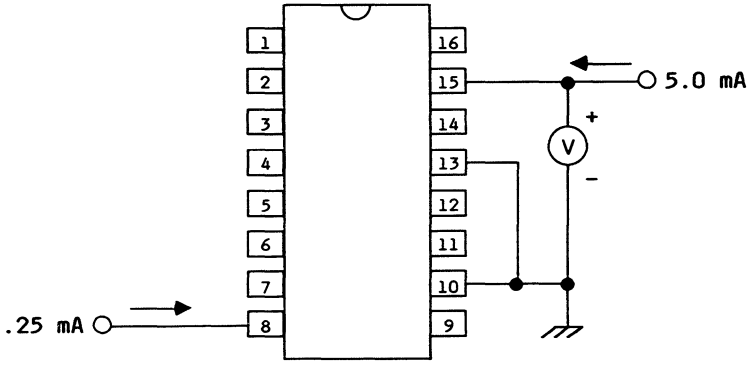


Figure 3. Saturation Voltage (V_{CE}) Test Circuit

Test Circuits
(Continued)

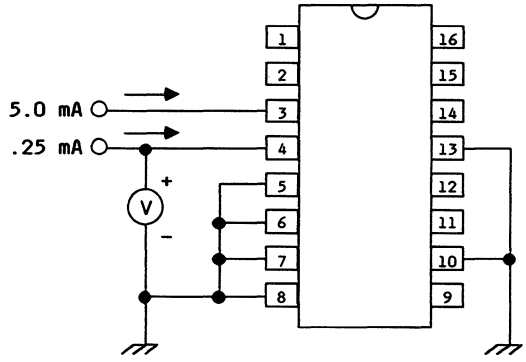


Figure 4. Saturation Voltage (V_{BE}) Test Circuit

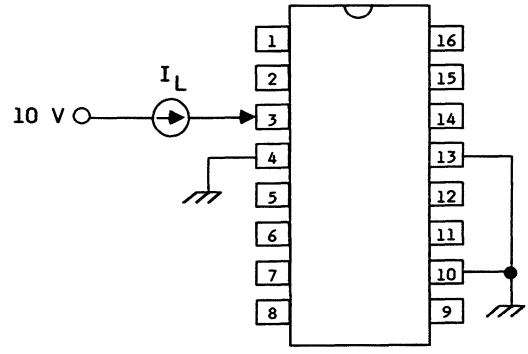


Figure 5. Leakage Current Test Circuit

General Description

The oscillator frequency is stable within ±20 ppm for supply voltages between 4.0 and 10 volts and temperature variations from 0 to +65°C as shown in Figure 6. The integrated amplifier can be used with any frequency crystal up to about 2.0 MHz without external resistors or capacitors, or an external resistor, capacitor, and inductor can be used to form an L-C oscillator over the same frequency band. The crystal current provided by the amplifier is about 0.35 mA (rms). The output current capability may be increased to over 200 mAp-p by connecting the output of the oscillator to one buffer transistor and using its output to drive the other four transistors in parallel.

Crystal Selection

Crystal units may have unwanted modes of oscillation; therefore, selection of a crystal for use with the LS1122AC is not trivial. Within the bandwidth of the amplifier (LS1122AC) the crystal will oscillate at the series resonant frequency of lowest equivalent resistance.

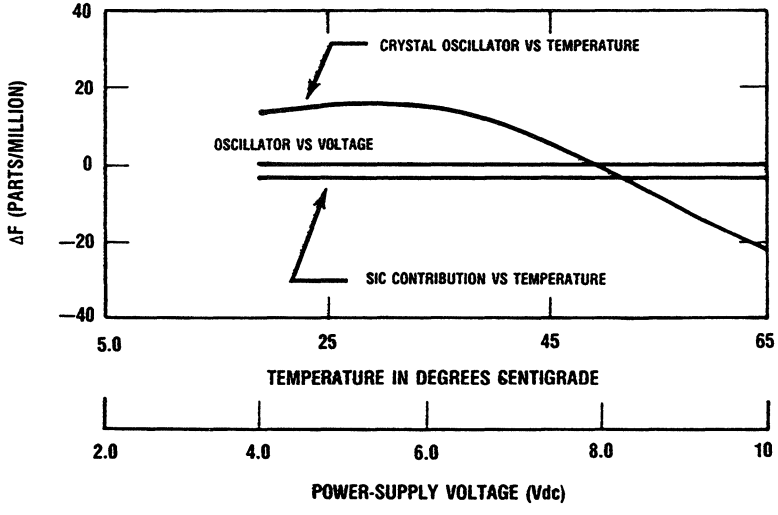


Figure 6. Frequency Deviation from Nominal 512 kHz

Options

Figure 7 shows the required connections to cause the LS1122AC to oscillate at frequencies up to about 2.0 MHz. The amplifier circuit transimpedance vs frequency is shown in Figure 8. This transimpedance [output voltage (lead 14) divided by input current (lead 12)] is referred to 1000 ohms. The typical value at 500 kHz is 4500 ohms.

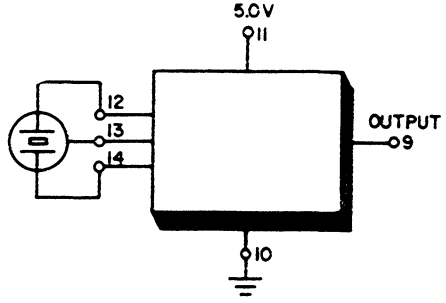


Figure 7. Low Frequency

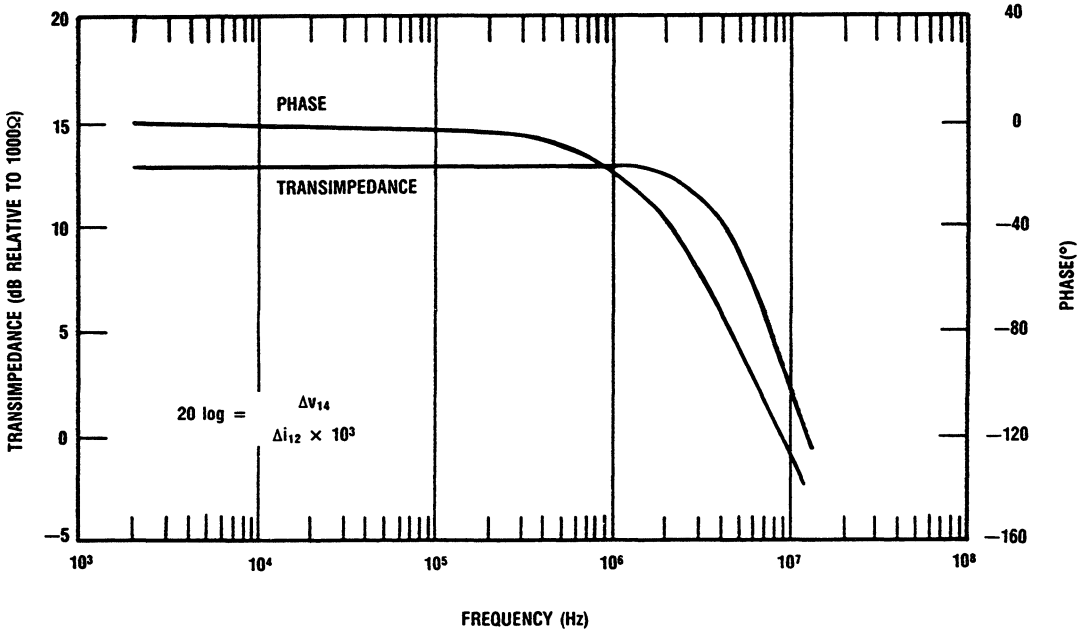
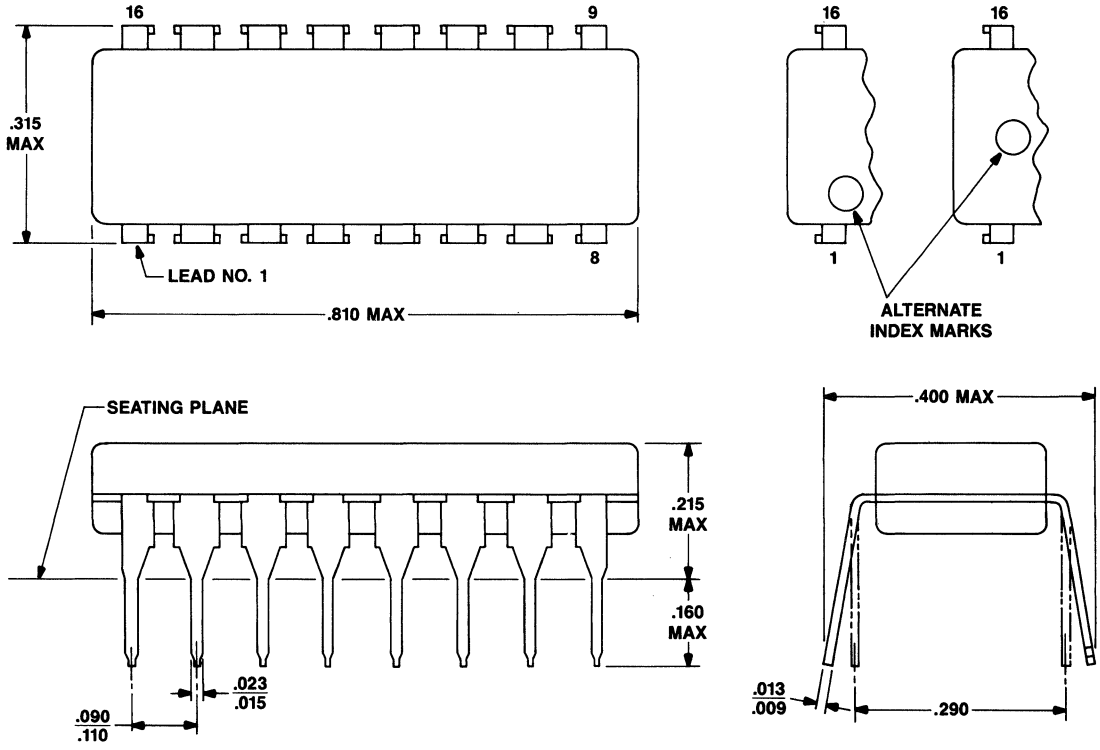


Figure 8. Typical Transimpedance and Phase vs Frequency

Outline Drawing

(Dimensions in Inches)



Ordering Information

Device	Comcode
LS1122AC	104412044

Description

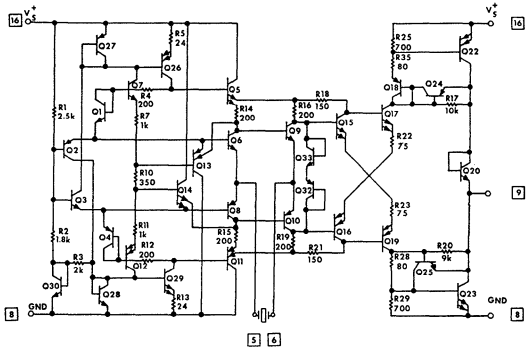
The LB1123AC Crystal Oscillator is a general-purpose oscillator which provides a TTL-compatible square wave output over a frequency range of 1.0 to 22 MHz. The LB1123AC accepts supply voltages over a range from +4.5 volts to +5.5 volts. It features typical transition (rise and fall) times of less than 10 ns and a symmetric duty cycle, typically ranging from 42% to 58%. The output voltage ranges from 2.4 volts to 4.85 volts.

The LB1123AC Crystal Oscillator requires an external crystal with series resonance less than 30 ohms. The LB1123AC is packaged in a 16-pin plastic DIP.

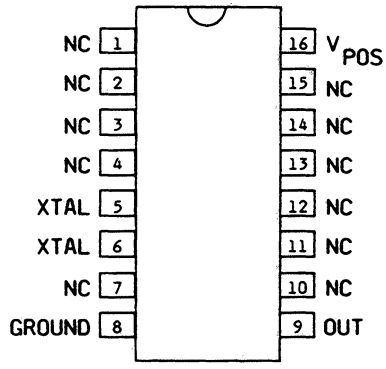
Features

- TTL-compatible square wave output
- Frequency range: 1.0 to 22 MHz
- Symmetrical duty cycle
- Quick transition times: < 10 ns

Functional Diagram



Pin Diagram



Notes:
1. All resistance values are in ohms.
2. For connections, see Lead Identification Table

Maximum Ratings (At T_A = 25°C unless otherwise specified)	
Power-Supply Voltage	7.0 V
Power Dissipation	180 mW
Storage Temperature Range	−40 to +125°C
Operating Temperature Range	0 to 60°C
Pin Soldering Temperature (t = 15 s)	300°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions

Pin	Name/Function	Pin	Name/Function
1	No Connection①	9	Output
2	No Connection①	10	No Connection①
3	No Connection①	11	No Connection①
4	No Connection①	12	No Connection①
5	Crystal	13	No Connection②
6	Crystal	14	No Connection①
7	No Connection①	15	No Connection①
8	Ground	16	V_{POS}

① This lead is not internally connected and may be used as a tie point provided the ratings of the device are not exceeded.
② No connections should be made to this lead.

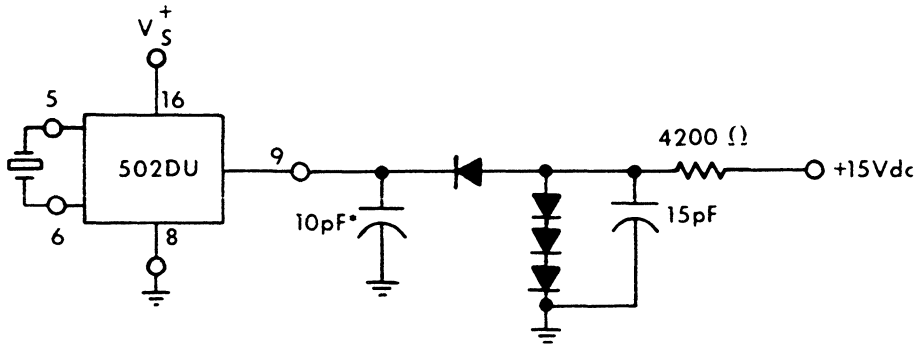
Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic		Test Condition	Min	Max	Unit
Power-Supply Current		V_{POS} = 7.0 V	5.0	17	mA
		V_{POS} = 5.5 V	4.0	14	
Output Voltage		V_{POS} = 4.5 V	100	360	mV
		V_{POS} = 5.5 V	2.6	5.2	V
		V_{POS} = 4.5 V	2.6	4.2	
Transition Time	Low to High	f = 5.0 MHz	—	12	ns
	High to Low		—	12	
Duty Cycle			45	55	%
Transition Time	Low to High	f = 12 MHz	—	10	ns
	High to Low		—	10	
Duty Cycle			42	58	%
Output Voltage High			2.4	4.7	$V_{(peak)}$

Test Circuit



*Includes probe, trigger circuit, and fixture capacitance. All diodes shall be 458E or equivalent.

Figure 1. Switching Time Test Circuit

General Description and Characteristics

This device is intended for use with an external crystal unit, especially for applications where fine adjustment of the crystal frequency is required.

The SIC is tested with a simulated five-gate medium-power TTL load at 5.0 and 12 MHz. Capacitive loading at the output will degrade the rise time. For frequencies above 12 MHz, the output loading shall be no more than two equivalent medium-power TTL gates.

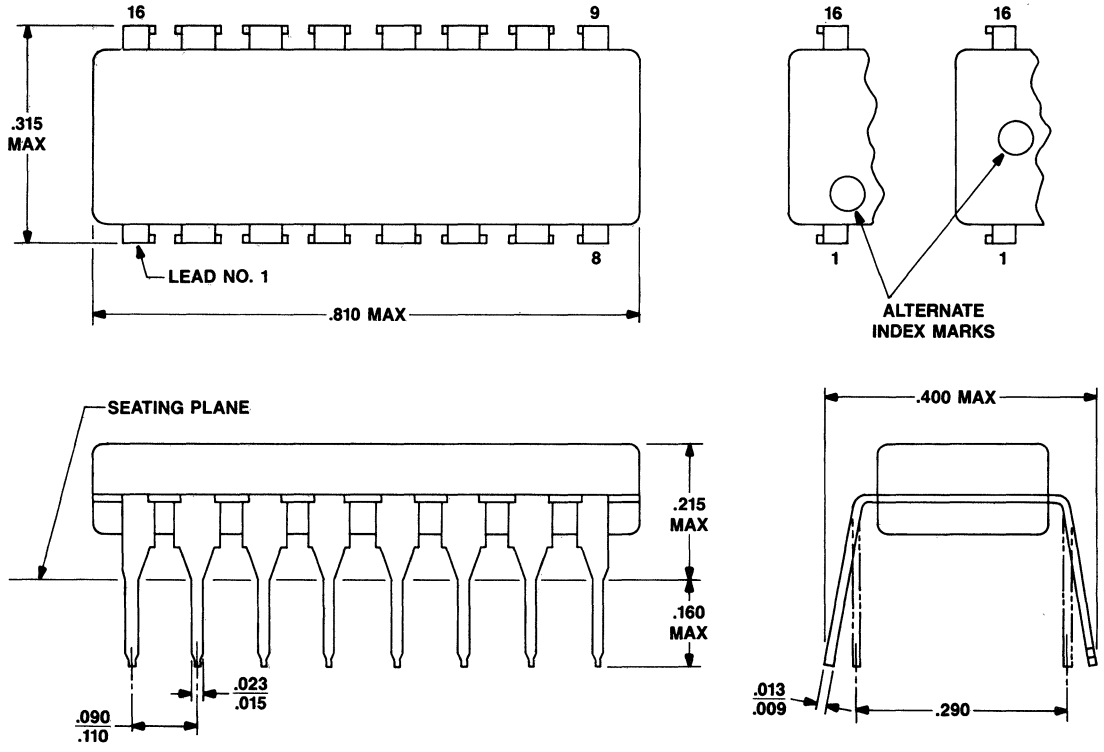
The duty cycle and transition times for the device are guaranteed over the power-supply voltage range of 4.5 to 5.5 V. Because of the high-frequency signals and high-peak currents in the LB1123AC, a bypass capacitor should be located close to the positive supply lead. In addition, the crystal should be located close to the crystal input leads.

Crystal Selection

Crystal units may have unwanted modes of oscillation; therefore, selection of a crystal for use with the LB1123AC is not trivial. Within the bandwidth of the amplifier (LB1123AC) the crystal will oscillate at the series resonant frequency of lowest equivalent resistance.

Outline Drawing

(Dimensions in Inches)



Ordering Information

Device	Comcode
LB1123AC	104411798

Description

The LB1125AF is a general-purpose phase-locked loop (PLL) designed for a variety of applications, including synchronization, synthesis, signal reconditioning, and stereo decoding. The key elements of the device are a phase comparator and voltage-controlled oscillator (VCO). It also incorporates a frequency-difference detector and a quadrature phase detector (QPD).

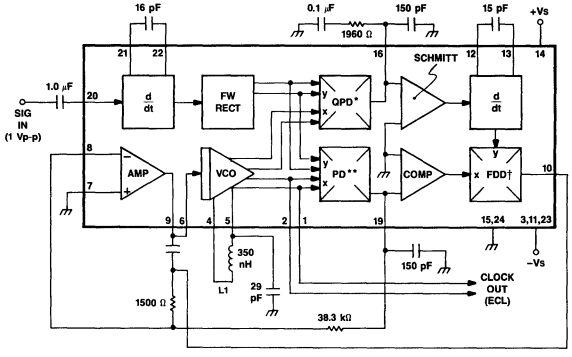
The frequency-difference detector exhibits a wide capture range (> ± 5%) while operating at the narrow bandwidths required for precise timing recovery. In addition, the circuitry is immune to random noise and features a differentiator/rectifier for use with unipolar NRZ (non-return to zero) data. The QPD is used with an external comparator to provide lock detection.

The LB1125AF PLL is a high-speed circuit capable of operating at frequencies as high as 50 MHz. The device requires power supply voltages of +5.0 and −5.2 V. It is suitable for applications with frequency differences of as much as 8%. Also, the device provides four balanced or single-ended ECL-compatible outputs with relative phases at 0, 90, 180, and 270 degrees. The VCO accuracy is within 1% for a ±4% sweep range. The LB1125AF is packaged in a 24-pin plastic DIP.

Features

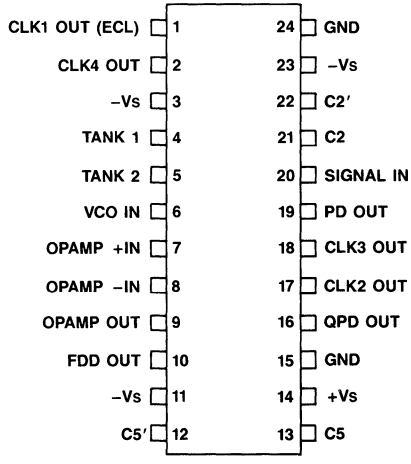
- High-frequency operation
- Precise timing recovery
- Reliable lock detection
- Noise immunity
- Operation to 50 MHz
- Unique frequency detector
- Four balanced or single-ended ECL-compatible clock outputs
- Quadrature phase detector output provides lock detection capability

Functional Diagram



* Quadrature Phase Detector
** Phase Detector
† Frequency Difference Detector

Pin Diagram



Maximum Ratings

Parameter	Rating	Unit
Positive Power Supply Voltage	5.5 V	V
Negative Power Supply Voltage	−5.7 V	V
Power Dissipation	500	mW
Operating Temperature Range	0 to 60	°C
Storage Temperature Range	−40 to +125	°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions

Pin	Symbol	Name/Function
1	CLK1 OUT	VCO output, 0° relative phase
2	CLK4 OUT	VCO output, 180° relative phase
3	−Vs	Negative supply, −5.2 V
4	TANK1	External tank circuit inductor connection
5	TANK2	External tank circuit inductor-capacitor connection
6	VCO IN	VCO control voltage input
7	OPAMP +IN	Internal op amp noninverting input
8	OPAMP −IN	Internal op amp inverting input
9	OPAMP OUT	Internal op amp output
10	FDD OUT	Frequency-difference detector output
11	−Vs	Negative supply, −5.2 V
12	C5′	Differentiation capacitor, connection 2
13	C5	Differentiation capacitor, connection 1
14	+Vs	Positive supply, +5.0 V
15	GND	Ground
16	QPD OUT	Quadrature phase detector output
17	CLK2 OUT	VCO output, 90° relative phase
18	CLK3 OUT	VCO output, 270° relative phase
19	PD OUT	Phase detector output
20	SIGNAL IN	Signal input
21	C2	Differentiation capacitor, connection 1
22	C2′	Differentiation capacitor, connection 2
23	−Vs	Negative supply, −5.2 V
24	GND	Ground

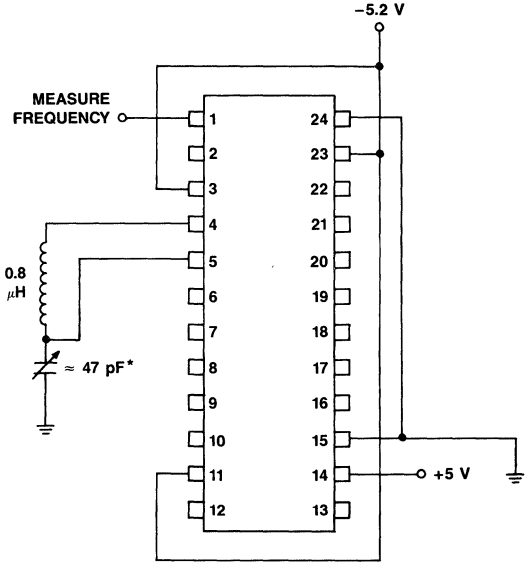
Electrical Characteristics (T_A = 25°C with $+V_S$ = 5.0 V and $-V_S$ = −5.2 V)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic and Conditions	Symbol	Min	Typ	Max	Unit
Operating Frequency	fo	—	—	50	MHz
Center Frequency Tolerance	f_{CT}	—	±0.5	±1.0	%
VCO Sweep Range	VCO_R	±4.5	±5.0	—	%
VCO Gain	VCO_G	4.8	5.4	6.0	%/V
PD Gain (100% Transition Density)	PD_G	0.8	1.0	1.2	V/pad
PD Offset	PD_{OFF}	—	±25	±50	mV
FDD Gain (100% Transition Density)	FDD_G	0.13	0.17	0.21	V/%
NRZ Data Input Level	Data IN	0.8	1.0	1.25	Vp-p
Positive Supply Voltage	$+V_S$	4.0	5.0	6.0	V
Negative Supply Voltage	$-V_S$	−4.9	−5.2	−5.5	V
Positive Supply Current	$+I_S$	15	19	30	mA
Negative Supply Current	$-I_S$	−50	−67	−85	mA
Free-Running Frequency	f_{FR}	19	20.9	24	MHz
Frequency with Input Voltage = 0.0 V	F_{VIN}	18	20	22	MHz

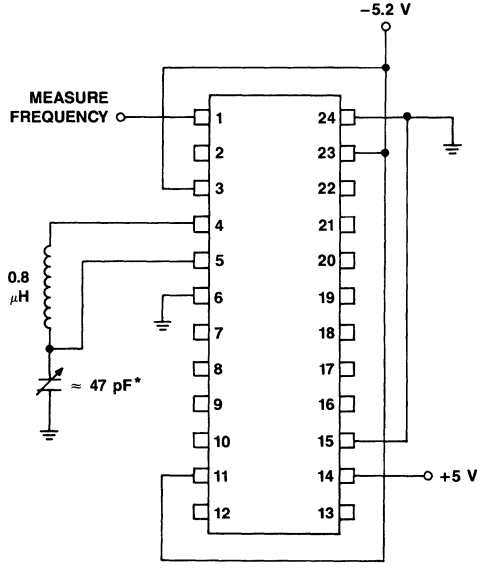
Test Circuits

Resistor values selected for use in all test circuits are characterized by a nominal ±1% tolerance; capacitors, ±10%.



* Capacitor should be adjusted so the resonant frequency of the tank circuit (including Lead length, etc.) is nominally 20 MHz.

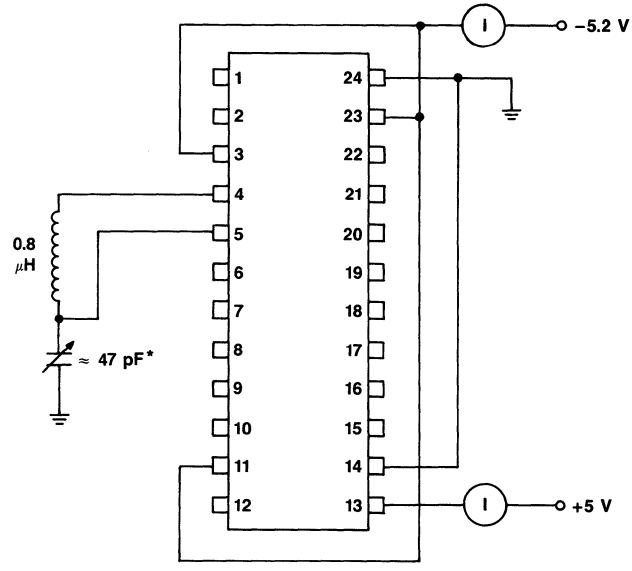
Figure 1. VCO Free-Running Frequency



* Capacitor should be adjusted so the resonant frequency of the tank circuit (including Lead length, etc.) is nominally 20 MHz.

Figure 2. VCO Clock Frequency with Input Voltage = 0.0 V

Test Circuits (Continued)



* Capacitor should be adjusted so the resonant frequency of the tank circuit (including lead length, etc.) is nominally 20 MHz.

Figure 3. ± Power Supply Currents

Characteristic Curves

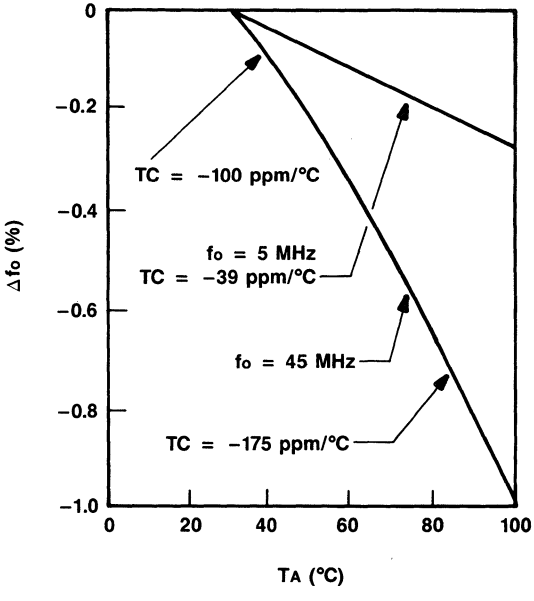


Figure 4. Typical Temperature Coefficient

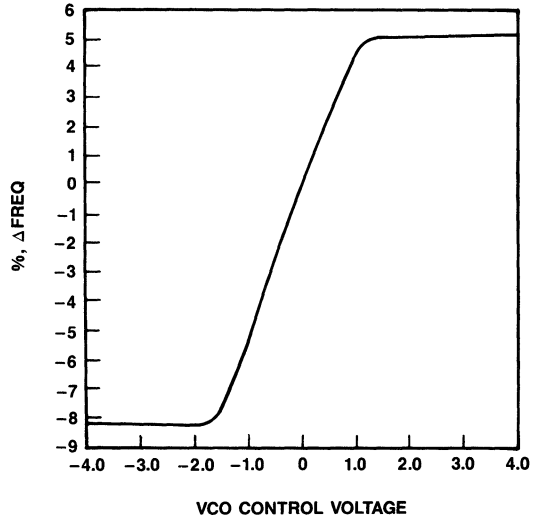


Figure 5. VCO Control Voltage* vs. Percent Change in Frequency

* To eliminate variations, devices are tested and tightly controlled using a control voltage of ±1 V.

Application

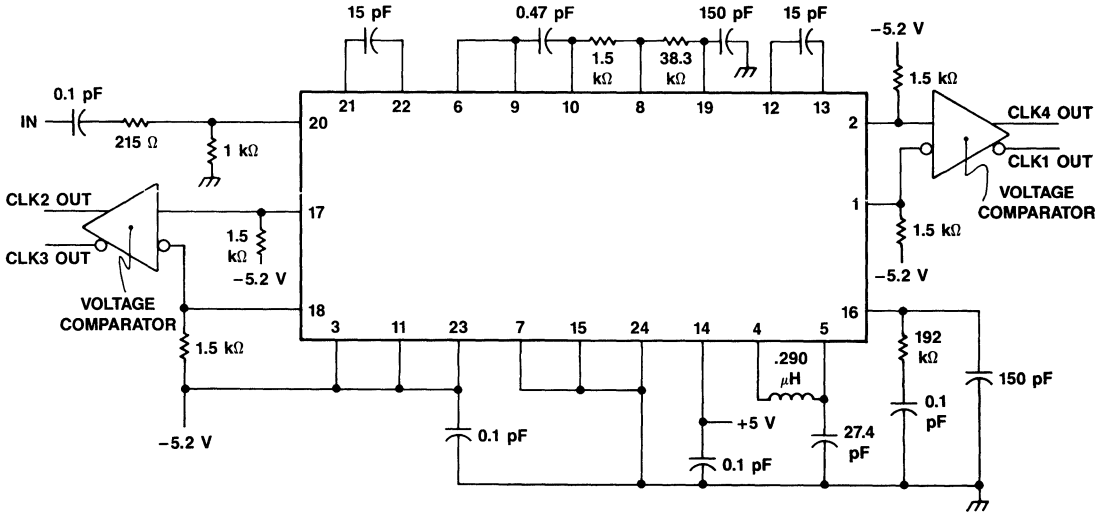
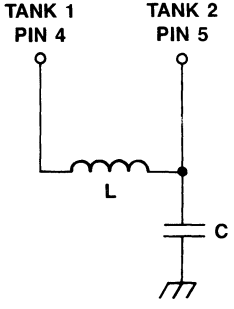


Figure 6. Sample Application Timing Recovery* in a Synchronous Digital Communication System Operating at 50 MHz

* In this application, the LB1125AF accepts data in a unipolar, non-return to zero (NRZ) format. Using the timing information contained in the data signal transitions, the circuit synchronizes the VCO to the data signal. The stable sinusoidal digital output is "squared-up" by an external comparator to provide a stable digital output at the baud frequency: a recovered clock. The recovered clock becomes a timing reference for regenerating data in the communications system.



$$Q = 10 = \frac{1}{R}\sqrt{\frac{L}{C}}$$

WHERE R = 10 Ω ON CHIP

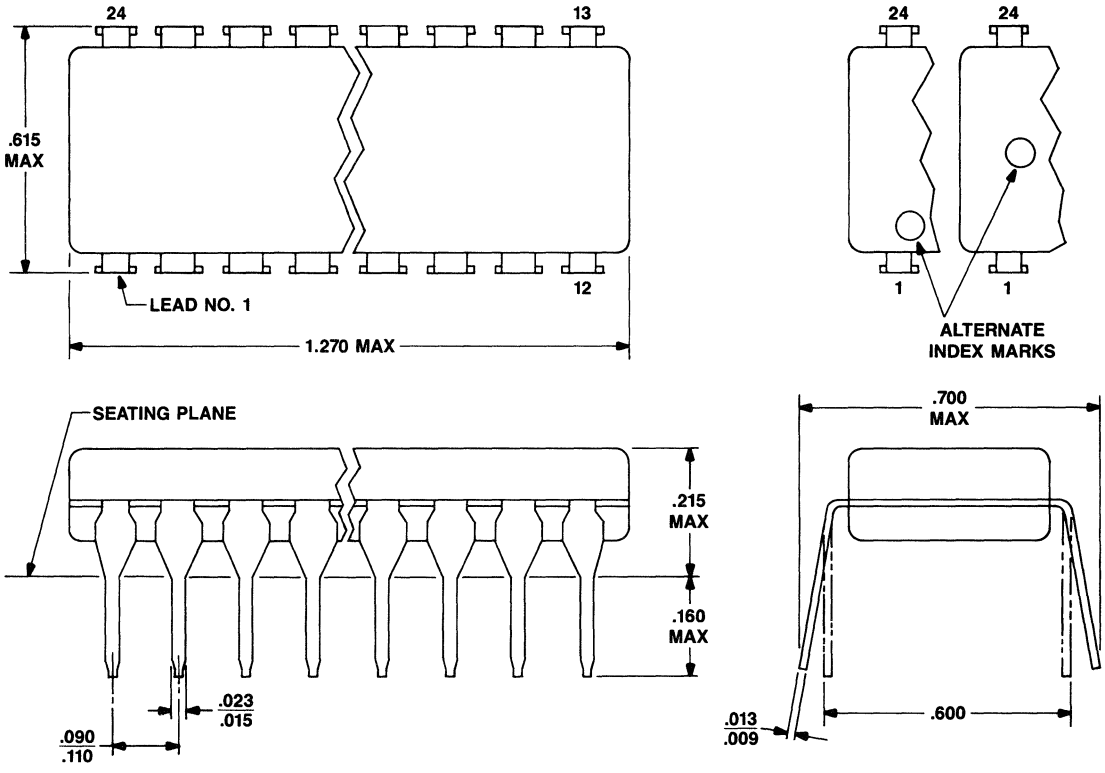
$$f = \frac{1}{2\pi\sqrt{LC}}$$

f	L	C
50 MHz	300 nH	30 pF
20 MHz	800 nH	80 pF
5 MHz	3 μH	300 pF

Figure 7. External Connections for Oscillation

Outline Drawing

(Dimensions in Inches)



Ordering Information

Device	Comcode
LB1125AF	104411814

PRELIMINARY

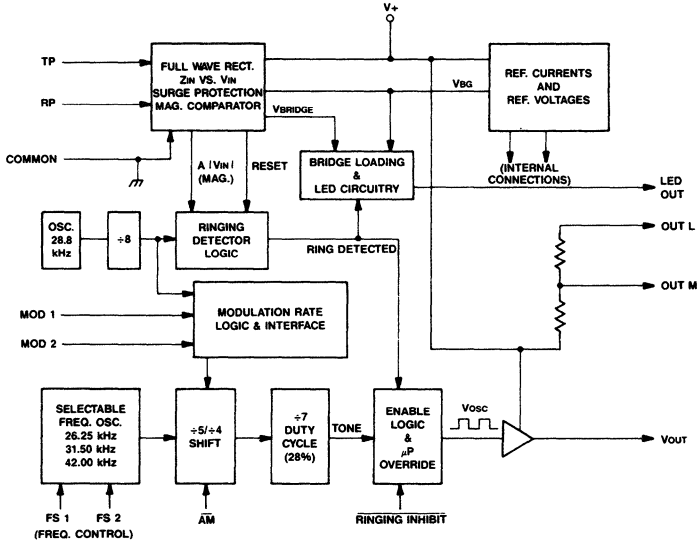
Description

The LB1004AC is a Full Feature Tone Ringer/Ringing Detector integrated circuit which simultaneously provides a ringer-output tone and a "ringing-detected" output signal. The tone ringer portion of the device provides switch-selectable output frequencies of 750, 900, 940, and 1200 Hz at independently selectable modulation rates of 7.5, 10, 15, and 20 Hz. Amplitude or frequency modulation may also be independently selected. These TTL/CMOS logic or switch selectable features, controlling both the type of sound and its duration, provide distinctive ringing capabilities which are useful for a multiphone office environment. The ringer can be prevented from providing a tone output with a "$\overline{\text{Ringing Inhibit}}$" function. These functions can be controlled by a microprocessor, allowing various alerting tasks to be performed by appropriate programming. The ringing detector portion of the device provides an output (LED OUT) which can interface with a microprocessor or an opto-isolator (see Applications).

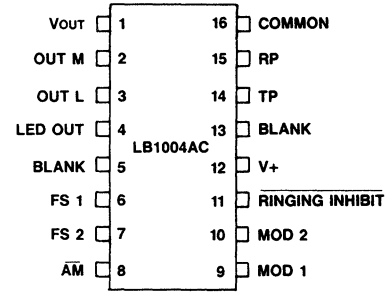
Features

- Complete telephone bell replacement with distinctive ringing capability
- Tight output frequency control (±3%) for maximum acoustic output
- External components: only two capacitors and one resistor required
- Independently selectable AM or FM modulation
- On-chip volume control resistors provided
- Immune to rotary dial pulsing (bell tap)
- Meets both type A and B ringing requirements (40 Vrms ≤ V_{IN} ≤ 150 Vrms, 15 Hz ≤ f_{IN} ≤ 68 Hz) as specified by EIA RS-470 and FCC Part 68
- Meets input impedance criteria specified by EIA RS-470
- Logic- or switch-selectable output frequency and modulation rate options
- Internal polarity guard and 1500 V lightning surge protection provided
- Ringer equivalency: 1.0 B when configured as shown in Figures 1 & 2

Functional Diagram



Pin Diagram



Maximum Ratings

Rating	Value	Unit
Operating Voltage (V+ to Common)	30	V
Operating Voltage (TP-RP)	±30	V
Operating Current (TP-RP)	±100	mA
Output Current (V_{OUT}-Common)	±30	mA
Ambient Operating Temperature Range	−20 to +75	°C
Storage Temperature Range	−40 to +125	°C
Pin Temperature (Soldering, 15 sec)	300	°C
Power Dissipation (Package Limitation)	500	mW

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Characteristic/Conditions	Min	Typ	Max	Unit
Power Supply Current (V+ = 28V)	—	0.76	1.9	mA
Power Supply Current (V+ = 15V)	—	0.73	1.5	
TP Current, No Load (TP-RP = 8.0 V)[1]	—	0.90	1.2	
RP Current, No Load (RP-TP = +8.0 V)[1]	—	−0.90	−1.2	
TP Current, No Load (RP-TP = 20V)[1]	—	0.98	1.55	
RP Current, No Load (TP-RP = −20 V)[1]	—	−1.0	−1.55	
Input Threshold Voltage, TP-RP (V+ = 8.0 V)[2]	6.0	7.0	8.0	V
Input Threshold Voltage, TP-RP (V+ = 25 V)[2]	6.0	7.0	8.0	
I_{TP} (V_{TP-RP} = 4.0 V); I_{RP}(V_{RP-TP} = 4.0 V)	—	15	30	μA
Clamp Voltage (I_{TP} = 25 mA)[3]	22.5	25.7	30	V
Clamp Voltage (I_{RP} = −25 mA)[3]	−22.5	−25.7	−30	
Clamp Voltage (I_{TP} = 100 mA)[3]	—	3.8	5.5	
Clamp Voltage (I_{RP} = −100 mA)[3]	—	−3.8	−5.5	
LED Current Off (Ringing not detected state)	—	0.43	±10	μA
LED Current On (Ringing detected state)	310	375	500	
Frequency (I_{TP} = 15 V)[4]	1164	1200	1236	Hz
Modulation Rate (V+ = 15 V)[4]	16	20	24	
Frequency (I_{TP} = 10 mA)[5]	1154	1225	1246	
Modulation Rate (I_{TP} = 10 mA)[5]	16	20	24	

Pin Description Key

Pin	Symbol	Name/Function
1	VOUT	Tone ringer output which drives the alerter
2	OUT M	Control option for medium volume output
3	OUT L	Control option for low volume output
4	LED OUT	Sinks current when ringing is detected
5	Blank	This pin may be used as a tie point for external components. Voltage applied to this pin should not exceed 30 volts.
6	FS 1	Frequency Select pin (see Table 2)
7	FS 2	Frequency Select pin (see Table 2)
8	$\overline{AM}$	Selects either AM or FM modulation of output ringer tone (see Table 1)
9	MOD 1	Modulation Rate Select pin (see Table 2)
10	MOD 2	Modulation Rate Select pin (see Table 2)
11	$\overline{\text{Ringing Inhibit}}$	The Ringer Inhibit function is a TTL/CMOS-compatible input for logic control of the Tone Ringer output (see Table 1)
12	V+	Internal supply voltage. This voltage is usually derived from the AC signal which is present on the Tip-Ring pair. This pin must have a 10 μF capacitor to common for energy storage and "smoothing" purposes. For "stand alone applications," an external voltage may be used to bias this pin.
13	Blank	This pin may be used as a tie point for external components. Voltage applied to this pin should not exceed 30 volts.
14 15	TP RP	Tip Prime (TP) and Ring Prime (RP) are the inputs to this device. AC ringing signals from the telephone line energize the detector circuit.
16	Common	Circuit Common (not necessarily physical or system ground)

Table 1. Tone Output Status (see Notes 6 and 7)

$\overline{\text{Ringing Inhibit}}$	$\overline{AM}$	Tone Output State
Open	Open	Frequency Shift Modulation (at modulation rate)
Low	Don't Care	No output tone
Open	Low	Amplitude Modulation (at modulation rate)

Table 2. Tone Selection (see Notes 6 and 7)

Frequency Select Pins			Modulation Rate Select Pins		
FS 1	FS2	Tone Output Frequency	MOD 1	MOD 2	Tone Output Modulation Rate
Open	Open	1200 Hz	Open	Open	20 Hz
Open	Low	960 Hz	Open	Low	15 Hz
Low	Open	900 Hz	Low	Open	10 Hz
Low	Low	750 Hz	Low	Low	7.5 Hz

Notes:

1. The specified current is measured with a 10 μF, 30 volt capacitor between V+ and Common, the proper voltage across TP and RP, and after ringing has been detected (30 to 40 ms).
2. With the proper voltage applied to V+, the threshold voltage is defined as the TP-RP voltage at which the device detects a ringing signal, as seen at the LED OUT pin or the alerter output (V_{OUT}-Common).
3. The potential between TP and RP is measured with the specified current at TP.
4. The output frequency and modulation rate between V_{OUT} and Common are measured with the specified voltage at V+ and the same potential at TP and RP. These measurements are obtained after ringing has been detected (30 to 40 ms).
5. The output frequency and modulation rate are measured with the specified current at TP and after ringing has been detected (30 to 40 ms).
6. Low denotes a connection (switch, wire path, or a transistor) between the appropriate pin and Common (pin 16). Pins 6, 7, 8, 9, 10 are TTL/CMOS-compatible inputs, with internal pull-up provided.
7. Frequency shift modulation generates frequencies f_O and 5/4 f_O. Amplitude modulation generates f_O and 2 f_O turned on and off at the modulation rate.

Applications

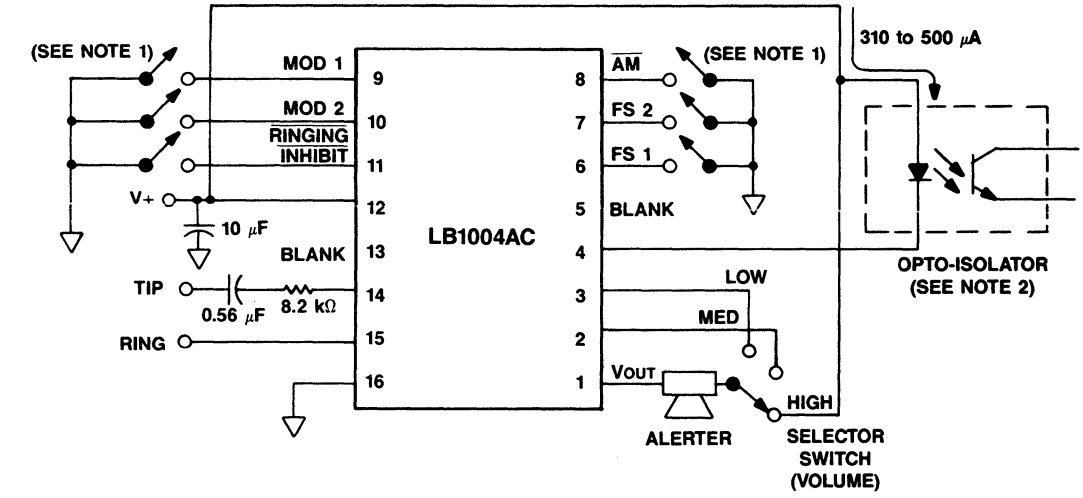
The LB1004AC requires only two capacitors, one resistor, and an output transducer to provide tone ringing functions from any standard Tip-Ring telephone pair. These devices operate over widely varying ringing waveforms (15 to 68 Hz at 40 to 150 Vrms).

A tone ringer derives its power by rectifying the ac ringing signal from the Tip-Ring pair of a telephone loop. It uses this power to activate a tone generator, and then transfers most of this power to an alerter after ringing is detected. Thus, there is essentially no loading under non-ringing conditions. Selectable on-chip resistors allow the volume of the alerter output to the adjusted (see application section).

The ringing detector portion of this device has one output (LED OUT). This output will sink current when ringing is detected, and can be connected to either an opto-isolator device or to a logic interface with a microprocessor (see Figures 1 and 2).

This device does not have to depend upon power derived from the Tip-Ring inputs to become operational. Connecting an external voltage source to V+ will also allow the device to operate in what is described as "stand alone applications."

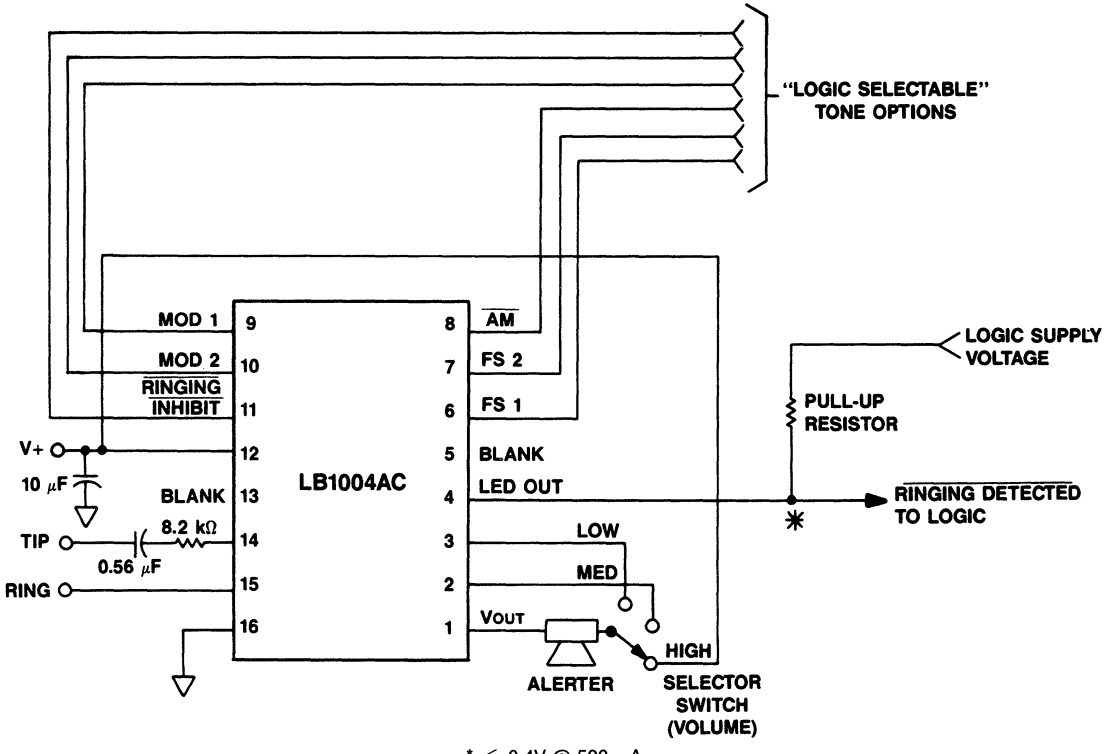
Applications (Continued)



Notes:

1. Pins 6, 7, 8, 9, 10 & 11 are switch or strap selectable
2. AT&T 4U, GI MCT210Q4898 or similar devices

Figure 1. Typical Application For Opto-Isolator Drive

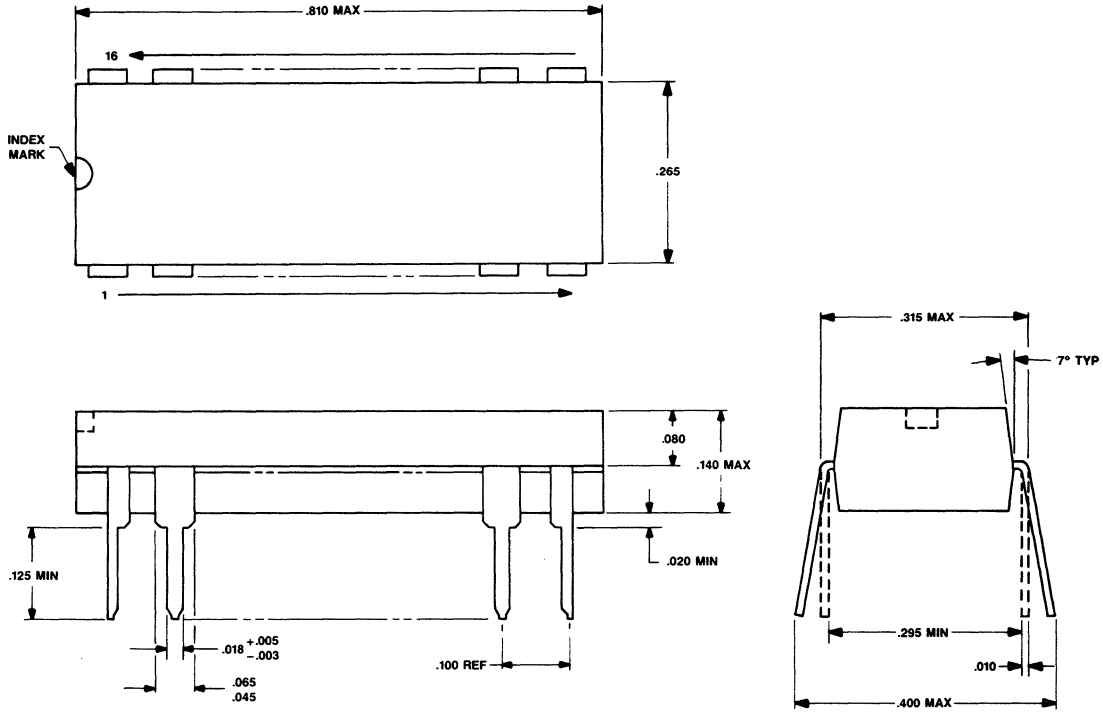


* ≤ 0.4V @ 500 μA

Figure 2. Typical Application for Interface Direct to Logic

Outline Drawing

(Dimensions in Inches)



Note: Pin numbers are shown for reference only

Ordering Information

Device	Comcode
LB1004AC	104208731

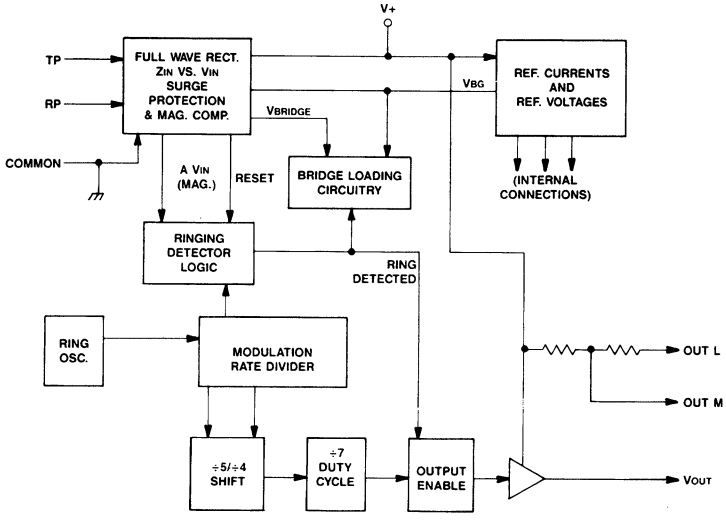
Description

The LB1005-TYPE General-Purpose Telephone Tone Ringer provides the telephone alerter function. The output tone warbles between the base frequency and 1.25 times the base frequency at a 15 or 20 Hz modulation rate (see Table 1 under Applications for specific tone options). These devices meet all known standard criteria for telephone alerters. Piezoelectric transducers can be driven directly.

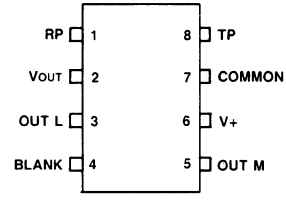
Features

- Tight output frequency control (±3%) for maximum acoustic output
- An internal polarity guard provides 2000 V lightning surge protection when connected as shown in the Application Diagram
- Meets both type A and B ringing requirements (40 Vrms ≤ V_{IN} ≤ 150 Vrms, 15 Hz ≤ f_{IN} ≤ 68 Hz) as specified by EIA RS-470 and FCC Part 68
- Provides essentially no loading under non-ringing conditions
- External components required are two capacitors, one resistor and an alerter
- Meets input impedance criteria specified by EIA RS-470
- Immune to rotary dial pulsing (bell tap)
- Ringer equivalency: 0.8 B when configured as shown in the Application Diagram
- On-chip volume control resistors are provided
- Class II ESD Rating

Functional Diagram



Pin Diagram



Maximum Ratings

Rating	Value	Unit
Operating Voltage (V+ to RP)	30	V
Operating Voltage (VOUT to RP)	30	V
Operating Current (TP or RP)	±100	mA
Output Current (VOUT)	±30	mA
Non-Recurrent Peak Surge Current, TP or RP (t ≤ 1 ms)	±500	mA
Ambient Operating Temperature Range	−20 to +75	°C
Storage Temperature Range	−40 to +125	°C
Pin Temperature (Soldering 15 sec)	300	°C
Power Dissipation (Package Limitations)	500	mW

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Characteristics

Pin Description Key

Pin	Symbol	Name/Function
1 8	RP TP	Tip Prime (TP) and Ring Prine (RP) are the inputs to the device. AC ringing signals from the telephone line energize the detector circuit. (Caution: Except for "Stand-Alone Applications" (see Applications), operation of Tip or Ring from a dc source is not recommended.)
2	VOUT	Tone ringer output which drives the alerter.
3	OUT L	Control option for low volume output.
4	Blank	This pin may be used as a tie point for external components. Voltage applied to this pin should not exceed 30 volts.
5	OUT M	Control option for medium volume output.
6	V+	Internal supply voltage. This voltage is usually derived from the ac signal which is present on the Tip-Ring pair. This must have a 10μF capacitor to common for energy storage and "smoothing" purposes. For "stand alone applications," an external voltage may be used to bias this pin. (Caution: In "Stand-Alone Applications" neither Tip nor Ring may swing more than one volt above V+ or 0.5 volts below chip common.)
7	Common	Circuit common (not necessarily physical or system ground). (Caution: This pin cannot be tied to hard (physical or system) ground if either Tip or Ring swings more than 0.5 volts below ground.

Electrcial Characteristics

(At 25°C unless otherwise specified)

Characteristic	Test Condition	Min	Typ	Max	Unit
Power Supply Current	V+ = 28 V (See Fig. 1)	200	455	900	μA
Power Supply Current	V+ = 15 V (See Fig. 1)	200	450	800	μA
TP Current, No Load	V_{TP-RP} = 20 V (See Fig. 2)	250	585	850	μA
RP Current, No Load	V_{TP-RP} = −20 V (See Fig. 2)	−250	−585	−850	μA
Input Threshold Voltage	V+ = 10 V (See Fig. 3)	6.0	7.4	8.0	V
TP Current, Low Voltage	V_{TP-RP} = 4.5 V (See Fig. 4)	—	32	65	μA
RP Current, Low Voltage	V_{TP-RP} = −4.5 V (See Fig. 4)	—	−32	−65	μA
Clamp Voltage	I_{TP} = 20 mA (See Fig. 5)	22.5	25.8	33.0	V
Clamp Voltage	I_{TP} = −20 mA (See Fig. 5)	−22.5	−25.8	−33.0	V
Clamp Voltage	I_{TP} = 100 mA (See Fig. 5)	—	3.6	5.5	V
Clamp Voltage	I_{TP} = −100 mA (See Fig. 5)	—	−3.6	−5.5	V
Low Frequency Output (F1)	(See Figure 6)				
LB1005AB		1746	1800	1854	Hz
LB1005BB		1164	1200	1236	Hz
LB1005CB		873	900	927	Hz
High Frequency Output (1.25 x F1)	(See Figure 6)				
LB1005AB		2160	2250	2340	Hz
LB1005BB		1440	1500	1560	Hz
LB1005CB		1080	1125	1170	Hz
Modulation Rate	(See Figure 6)				
LB1005AB & LB1005BB		16	20	24	Hz
LB1005CB		12	15	18	Hz

Test Circuits

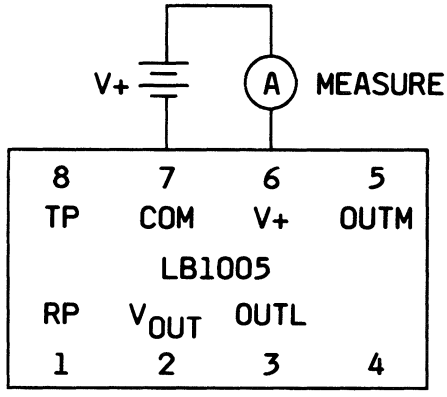


Figure 1. Test Circuit (Power Supply Current)

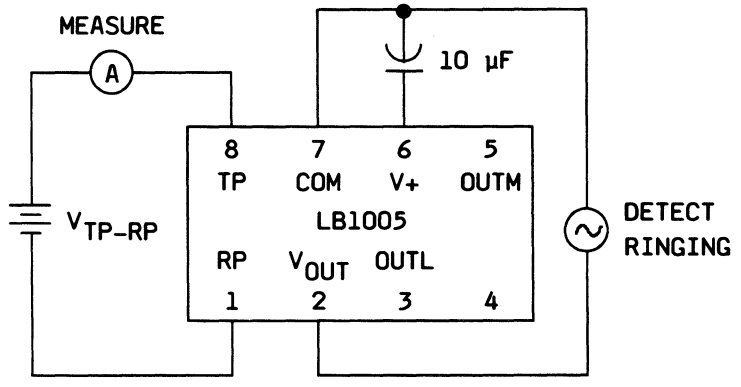


Figure 2. Test Circuit (TP and RP Currents, No Load)

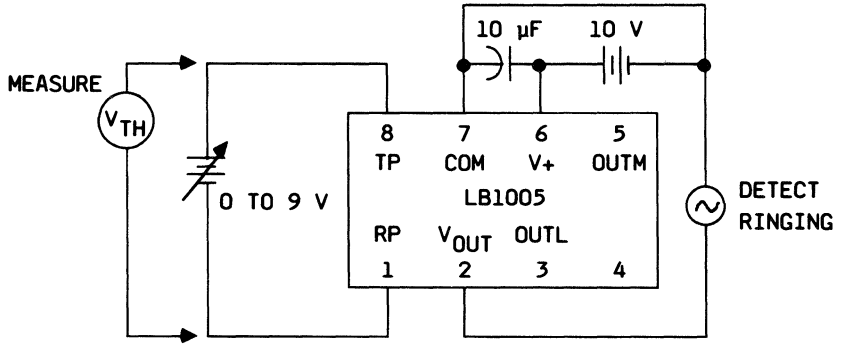


Figure 3. Test Circuit (Input Threshold Voltage)

Test Circuits
(Continued)

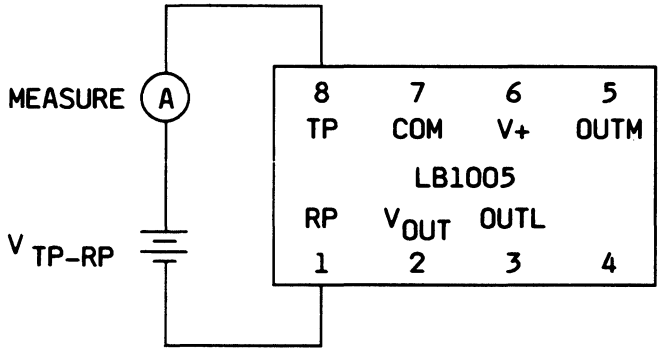


Figure 4. Test Circuit (TP and RP Current, Low Voltage)

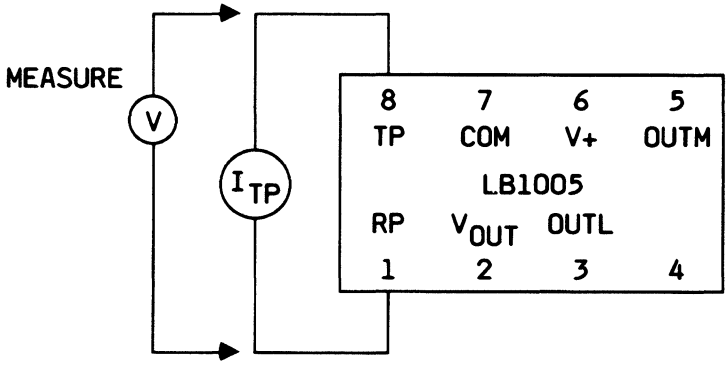


Figure 5. Test Circuit (Clamp Voltage)

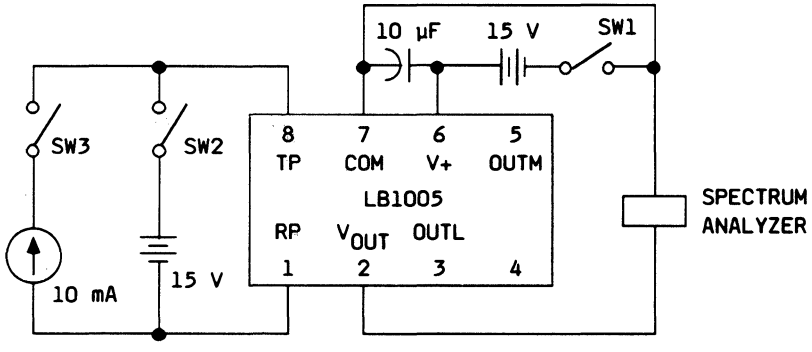


Figure 6. Test Circuit (Output Frequency and Modulation Rate)

Test Circuits
(Continued)

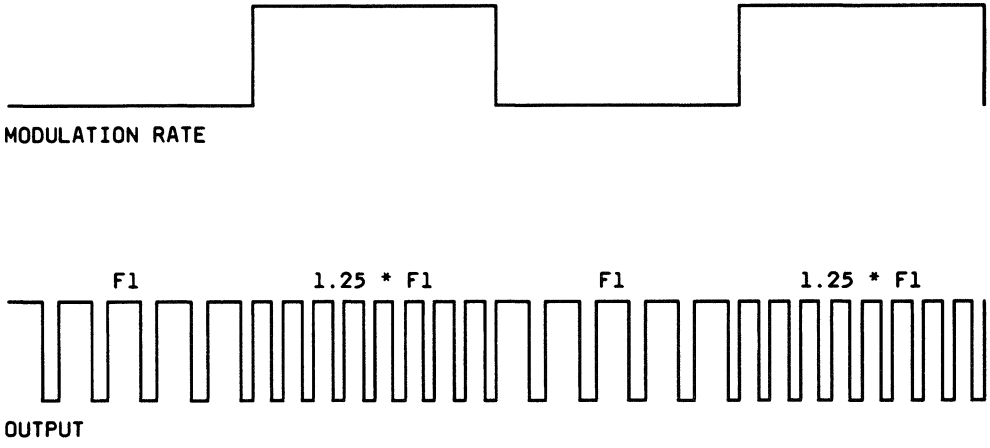


Figure 7. Tone Ringer Output Waveform (Approximately)

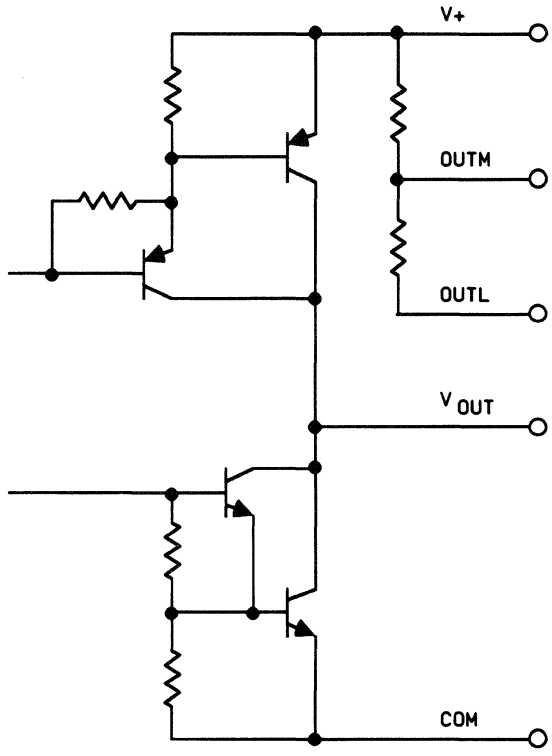


Figure 8. Simplified Tone Ringer Output Diagram

Applications

The LB1005-TYPE device requires only two capacitors, one resistor, and an alerter to provide tone ringing functions from any standard Tip-Ring telephone pair. The device operates over widely varying ringing waveforms (15 to 68 Hz at 40 to 150 Vrms.) The LB1005-TYPE derives its power by rectifying the ac ringing signal from the Tip-Ring pair of a telephone loop. It uses this power to activate a tone generator, and then transfers most of this power to an alerter after the ringing has been detected. There is essentially no loading under non-ringing conditions. Selectable on-chip resistors allow the volume of the alerter output to be adjusted (see Typical Application diagram). These devices do not have to depend upon power derived from the Tip-Ring inputs to become operational. Connecting an external voltage source to V+ will also allow the devices to operate in what is described as "stand alone applications." The tone generator circuitry includes an oscillator and frequency divider which produce specified tones and the tone modulation rate. The output warble frequency ranges and modulation rates are shown in Table 1. This device is not intended to drive electromagnetic (EMR) type alterers directly without a coupling capacitor. In such applications, a suitable capacitor in the range of 0.01 to 1.0 μf should be inserted in series with the alterer.

Table 1. Tone Generation (Design Values)

Device Number	Output Warble Frequency Range	Modulation Rate	Output Duty Cycle
LB1005AB	1800/2250 Hz	20 Hz	28%
LB1005BB	1200/1500 Hz	20 Hz	50%
LB1005CB	900/1125 Hz	15 Hz	50%

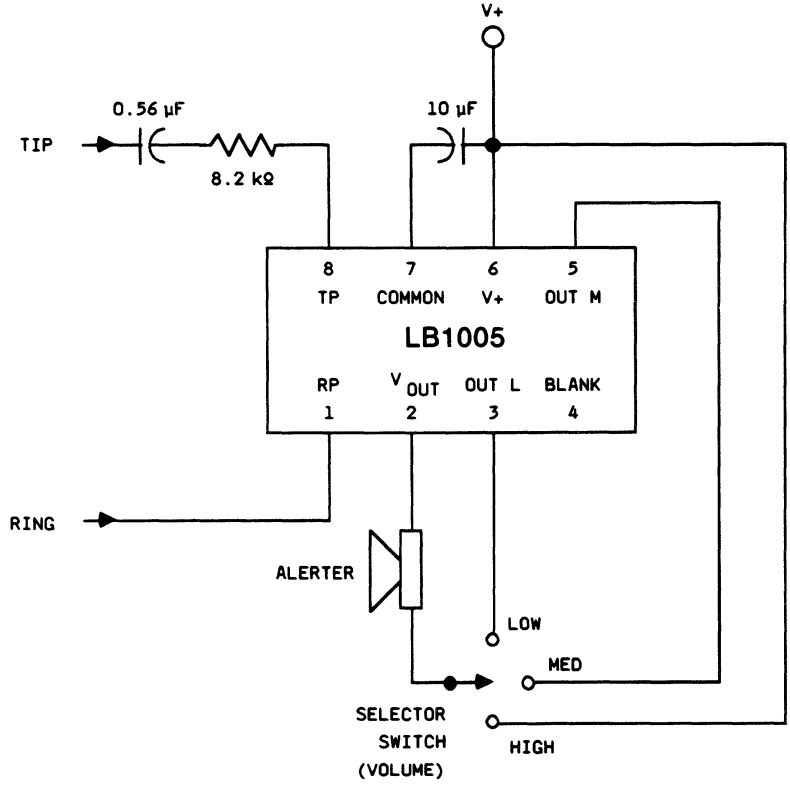
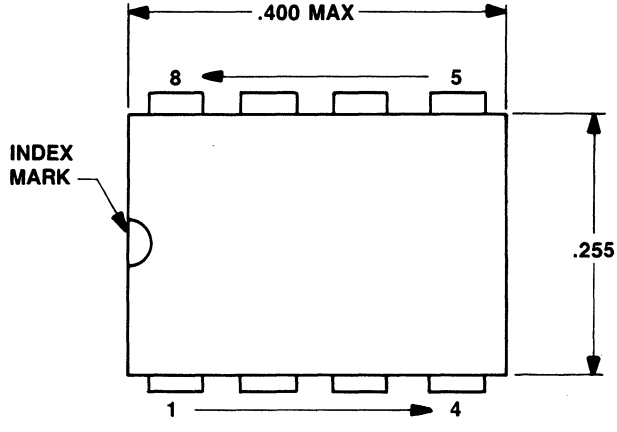
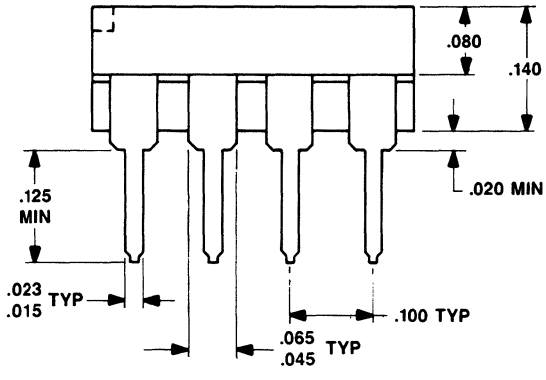


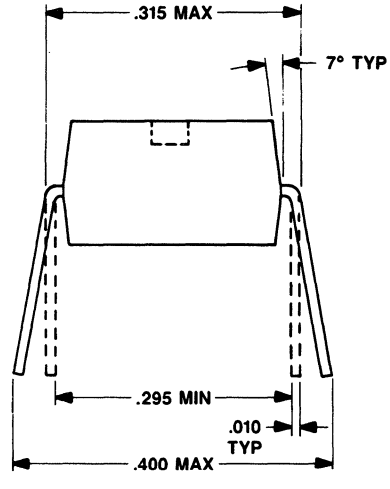
Figure 9. LB1005 Typical Application

Outline Drawing

(Dimensions in Inches)







Ordering Information

Device	Comcode
LB1005AB	104208749
LB1005BB	104208756
LB1005CB	104393293

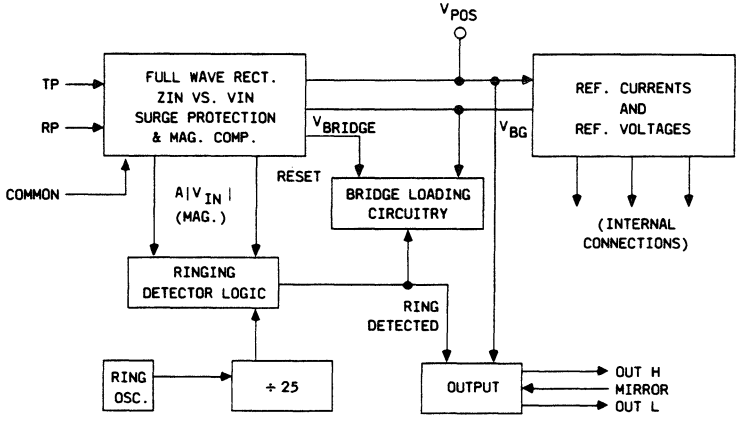
Description

The LB1006AB Telephone Ringing Detector integrated circuit provides ringing detection functions from the Tip-Ring pair of a telephone loop. This device provides approximately 1 mA output current for two types of output drivers. The output can be connected to either an opto-isolator device or to a logic interface with a microprocessor.

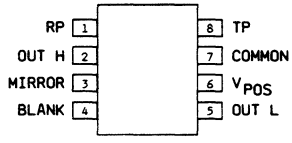
Features

- Internal polarity guard provides 1500 V secondary lightning-surge protection (15 A peak, 10 μs rise time, 1000 μs decay to half-peak amplitude), when connected as shown in Figures 13 and 14
- Operates on less than 1.0 mA from telephone loop
- Immune to rotary dial pulsing (bell tap)
- Meets both type A and B ringing requirements (40 Vrms $\leq V_{IN} \leq$ 150 Vrms, 15 Hz $\leq f_{IN} \leq$ 68 Hz) as specified by EIA RS-470 and FCC Part 68
- High-input standby impedance (typically > 100 k ohms)
- Ringer equivalency; 0.8 B when configured as shown in Figures 13 and 14

Functional Diagram



Pin Diagram



Maximum Ratings (At 25°C unless otherwise specified)	
Operating Voltage (V_{POS} to COMMON)	30 V
Operating Voltage (TP to RP)	±30 V
Operating Voltage (OUT H to COMMON)	30 V
Operating Voltage (OUT L to COMMON)	30 V
Operating Current (TP to RP)	±100 mA
Non-Recurrent Peak Surge Current, t ≤ 1 ms (TP to RP)	±500 mA
Ambient Operating Temperature Range	−40 to +75°C
Storage Temperature Range	−40 to +125°C
Pin Soldering Temperature (t = 15 s max.)	300°C
Power Dissipation	500 mW

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may affect device reliability.

Pin Description

Pin	Symbol	Name/Function
1	RP	RING Prime. AC input signal from the RING side of the telephone loop.
2	OUT H	This output sources current when ringing is detected (Figure 12).
3	MIRROR	Current from OUT H will activate OUT L when connected as shown in Figure 12.
4	BLANK	This pin may be used as a tie point for external components. Voltage applied to this pin should not exceed 30 volts.
5	OUT L	This output sinks current when ringing is detected (Figure 12).
6	V_{POS}	Internal supply voltage. This voltage is usually derived from the ac signal which is present on the TIP-RING pair. This pin must have a 10 μF capacitor to COMMON for energy storage and "smoothing" purposes. For "stand-alone applications", an external voltage supply may be used to bias this pin.
7	COMMON	Substrate of the LB1006AB device. **Caution:** Extra care must be taken when the LB1006AB is used with systems referenced to earth ground (see further discussions under the APPLICATION section).
8	TP	TIP Prime. AC input signal from the TIP side of the telephone loop.

Test Description

(At 25°C unless otherwise specified)

Characteristic	Test Condition	Min	Typ	Max	Unit
Power-Supply Current	Figure 1; V_S = 28 V	200	365	900	μA
Power-Supply Current	Figure 1; V_S = 15 V	200	360	800	μA
TP Current	Figure 2	—	30	65	μA
RP Current	Figure 3	—	30	65	μA
OUT L Current	Figure 4	750	—	1400	μA
OUT H Current	Figure 5	540	900	1040	μA
Mirror Current	Figure 6	750	1245	1400	μA
TP Current, No Load	Figure 7	0.25	1.4	1.8	mA
RP Current, No Load	Figure 8	0.25	1.4	1.8	mA
Input Threshold Voltage	Figure 9	6.0	7.2	8.0	V
Clamp Voltage	Figure 10; I_{TP} = 20 mA Figure 10; I_{TP} = 100 mA	22.5 —	25.5 3.60	30.0 5.50	V V
Clamp Voltage	Figure 11; I_{RP} = 20 mA Figure 11; I_{RP} = 100 mA	22.5 —	25.5 3.60	30.0 5.50	V V

Test Circuits

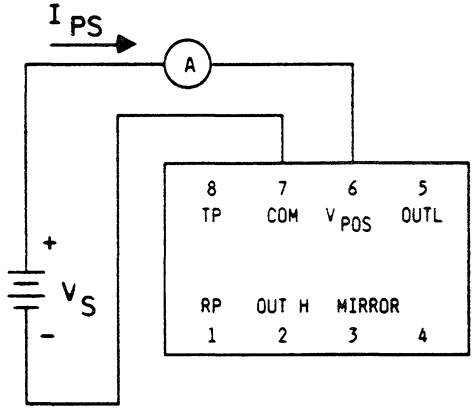


Figure 1. Power-Supply Currents

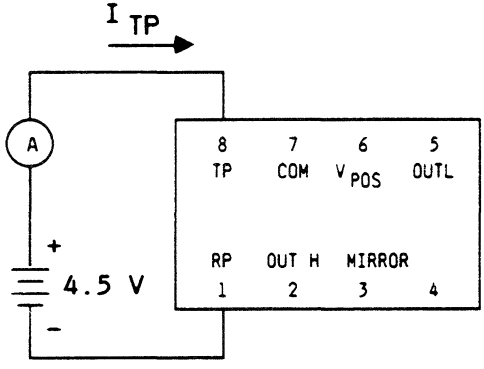


Figure 2. TP Current

Test Circuits
(Continued)

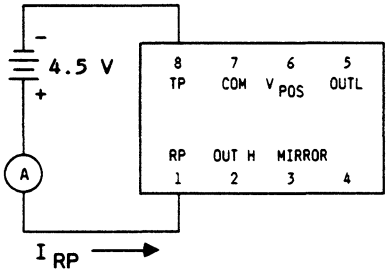


Figure 3. RP Current

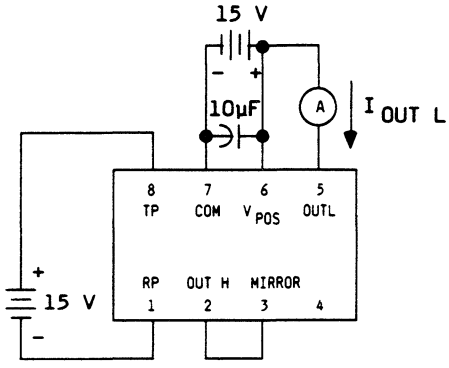


Figure 4. OUT L Current

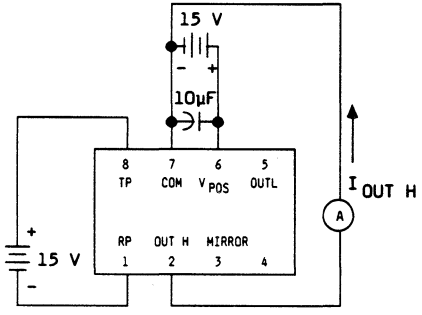


Figure 5. OUT H Current

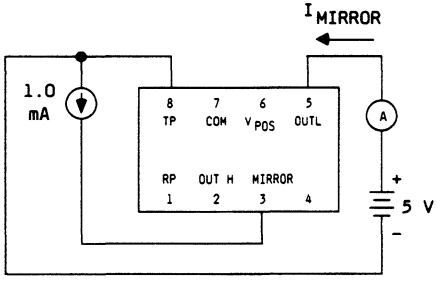


Figure 6. MIRROR Current

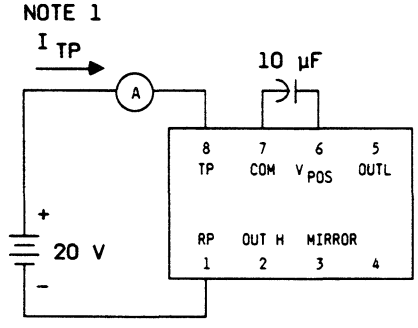


Figure 7. TP Current, No Load

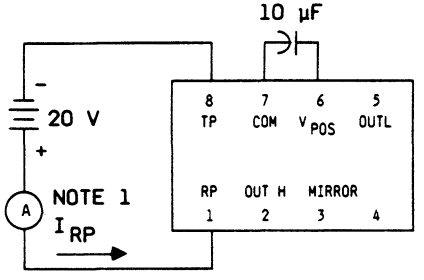
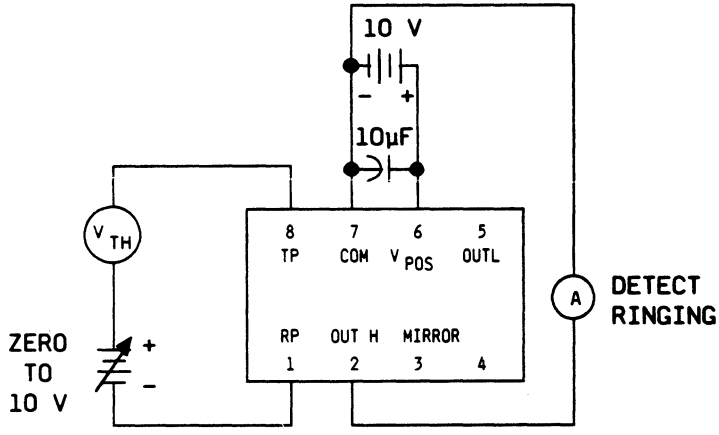


Figure 8. RP Current, No Load

Note 1: Current is measured between 30 ms and 40 ms after ringing has been detected ("OUT H" sources current when ringing has been detected).

Test Circuits
(Continued)



Threshold voltage is the voltage between TP and RP when ringing has been detected ("OUT H" sources current when ringing has been detected). This voltage is increased in the positive direction until the ringing condition occurs.

Figure 9. Input Threshold Voltage

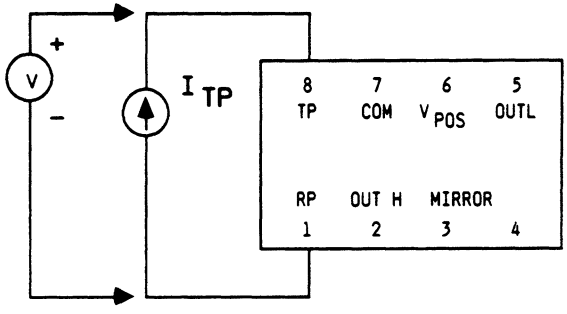


Figure 10. Clamp Voltage (I_{TP})

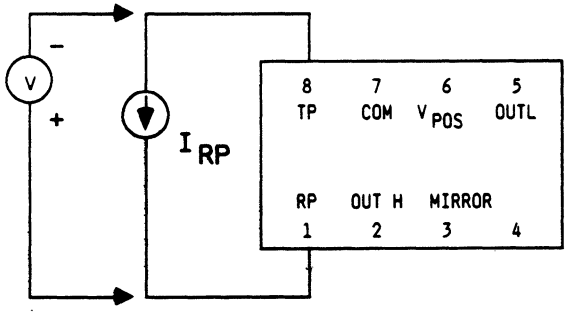


Figure 11. Clamp Voltage (I_{RP})

Applications

The LB1006AB detector derives its power by rectifying the ac ringing signal from the Tip-Ring pair of a telephone loop. It operates over widely varying ringing waveforms (15 to 68 Hz at 40 to 150 V_{RMS}). It uses this derived power to activate ringing-detector logic, and then transfers most of this power to an output current driver. There is essentially no loading under non-ringing conditions.

Caution:
Relatively high voltages (see above paragraph) can be present at the inputs (TP and RP) with respect to earth ground. Therefore, care must be taken when interfacing to an LB1006AB load which is referenced to earth ground. In these situations, use of an opto-isolator is recommended to prevent low-impedance paths from the Tip-Ring to earth ground. In summary, an opto-isolator (or similar functional type of device) is recommended when the load on the LB1006AB is referenced to earth ground.

This device has two outputs, OUT H and OUT L. The OUT H pin is used to source output current when ringing is detected. The OUT L output becomes functional when the OUT H pin is connected to the MIRROR input. The OUT L pin will sink current when ringing is detected (see Figure 12). This device does not have to depend upon power derived from the Tip-Ring inputs to become operational. Connecting an external voltage source to V_{POS} will also allow the device to operate in what is described as "stand-alone operation".

Application for the two types of outputs (source or sink current) are shown in Figures 13 and 14. Figure 13 shows an application where the output is configured to source an opto-isolator. Figure 14 shows an application where the output is configured to sink current for logic operation.

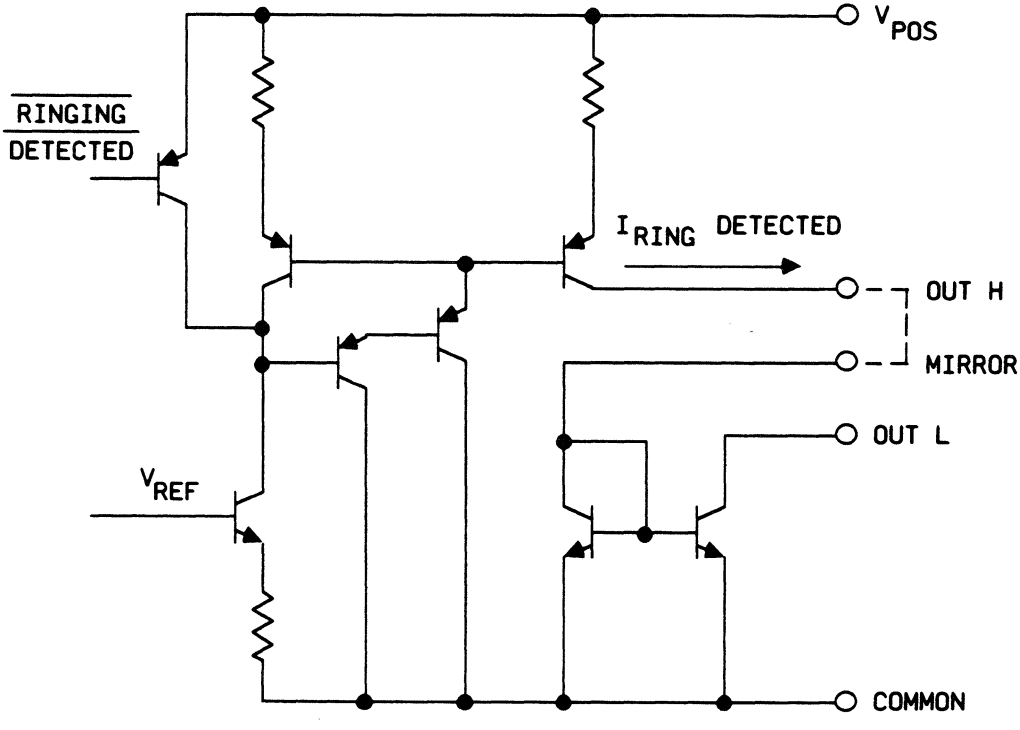
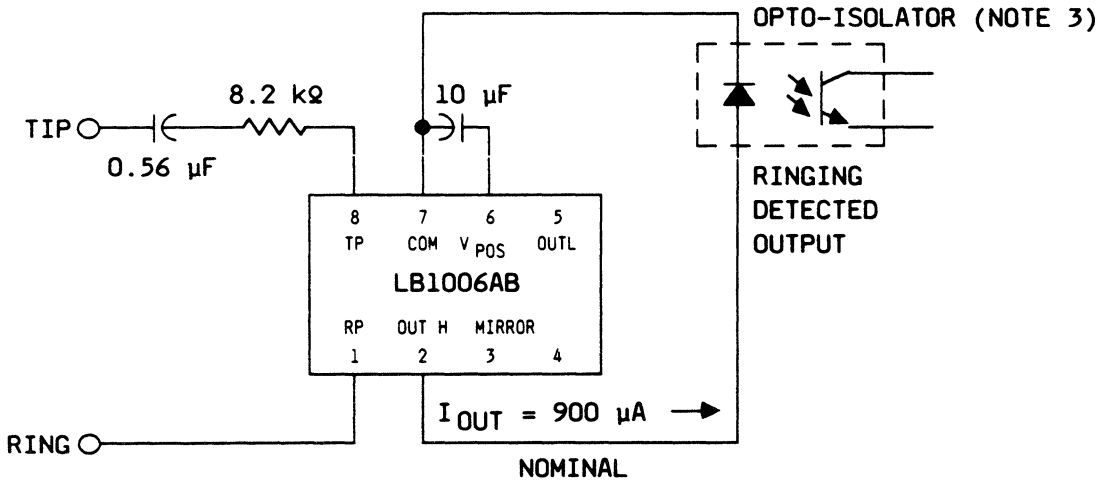


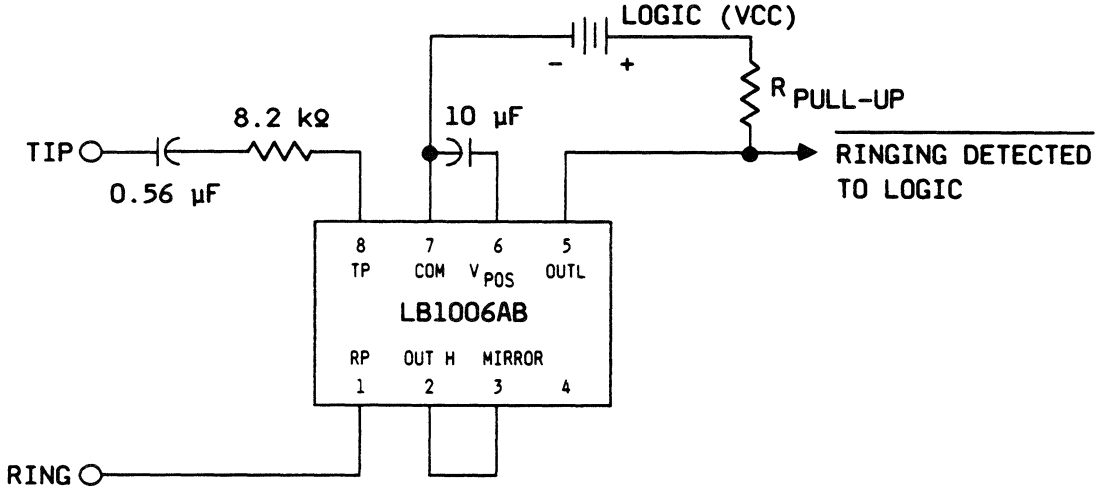
Figure 12. Simplified Output Diagram

Applications
(Continued)



Note 3: AT&T 4U GI MCT210Q4898 or similar devices

Figure 13. Typical Application for Opto-Isolator Drive

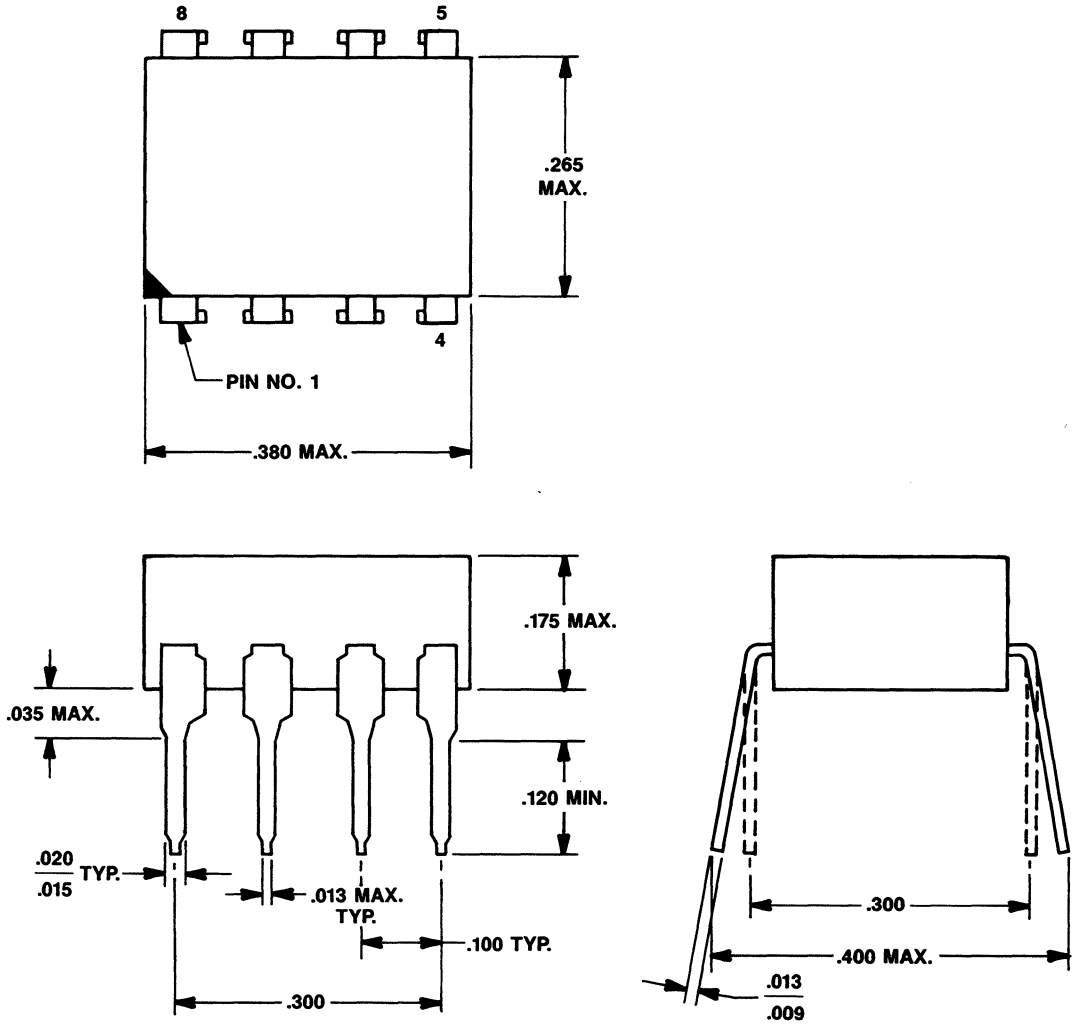


CAUTION: Care must be taken when interfacing to a load which is referenced to earth ground (see APPLICATIONS text for further details).

Figure 14. Typical Application for Interface Direct to Logic

Outline Drawing

(Dimensions in Inches)



Ordering Information

Device	Comcode
LB1006AB	104208764

PRELIMINARY

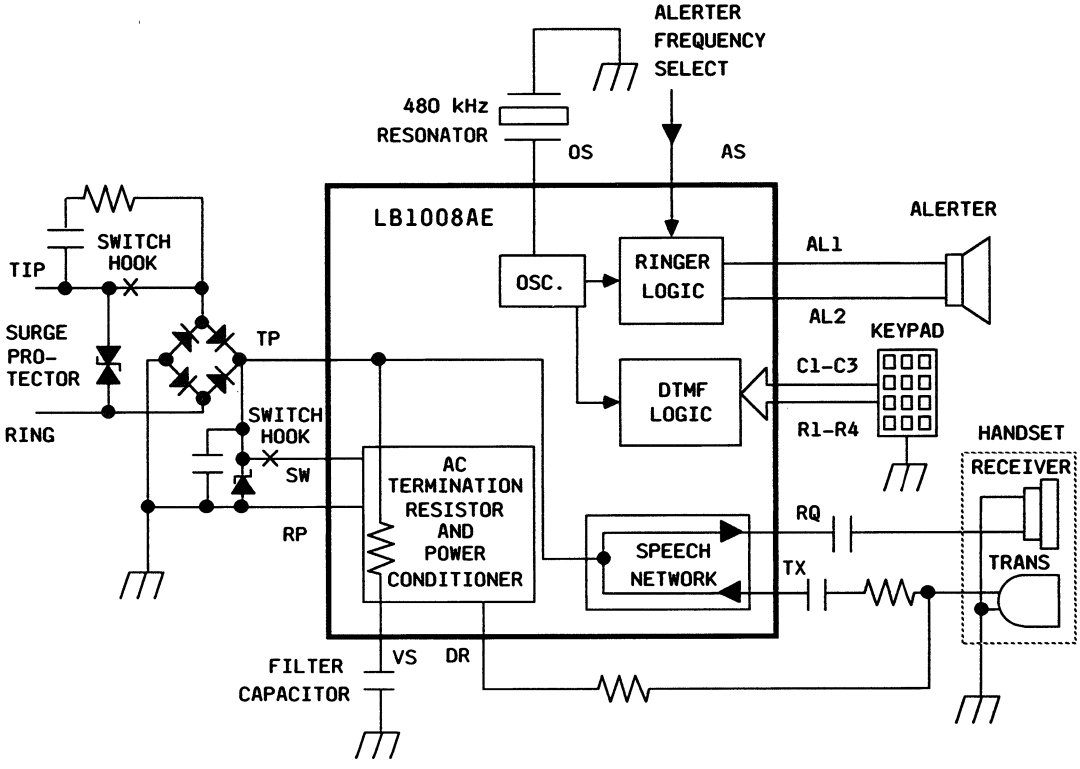
Description

The LB1008AE integrated circuit requires only a few external components (see Figure 19) to provide all of the touch-tone electronic functions. This integrated circuit furnishes ac and dc loop termination for both switchhook states, transmits and receives voice signals to the central office, provides dual-tone multi-frequency (DTMF) signals to the central office, and properly distinguishes between spurious noise and genuine ringing signals, providing a distinctive audible alerter output.

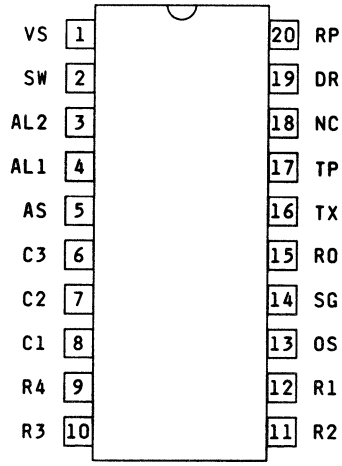
Features

- An alerter option function of 1200/1500, or 1800/2250 Hz
- Capable of speech transmission down to 3.0 mA loop current
- Compatible with electret and carbon microphones
- Signal ground pin eliminates external capacitor for dial-in-handset designs
- 700 ohm line matching impedance, 600 ohm receiver impedance
- Provides a power port for driving an LED

Functional Diagram



Pin Diagram



Maximum Ratings (At 25°C unless otherwise specified)	
Ambient Operating Temperature Range	0 to +60°C
Storage Temperature Range	−40 to +125°C
Pin Soldering Temperature (t = 15 s max.)	300°C
Voltage (TP)	20 V
Current (TP)	120 mA

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Characteristics

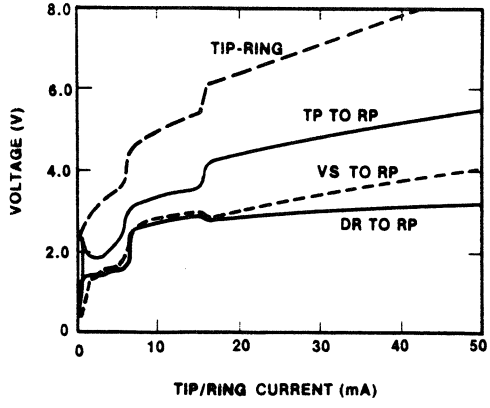


Figure 1. Typical V-1 Characteristics (Dial Mode)

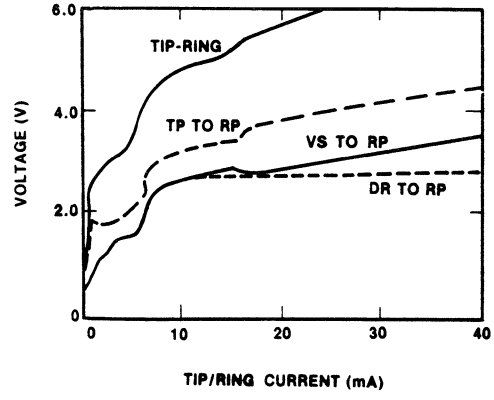


Figure 2. Typical V-1 Characteristics (Speech Mode)

Pin Description (See Functional Diagram)

Pin	Symbol	Name/Function
1	VS	The most positive dc voltage (filtered) on the device. This voltage is derived from the TIP-RING inputs. It is used to supply internal circuits.
2	SW	Turns on transmit/receive circuitry when connected through switchhook contact to the TP pin.
3 4	AL2 AL1	Output terminals for driving an alerter. The ringer logic distinguishes between genuine ringing and noise signals present on the telephone loop, and provides a distinctive audible output. The alerter can be driven differentially or single-ended. If the alerter is driven single-ended to RP, the second output can be used to drive a visible indicator to RP. Volume can be adjusted by placing a resistor in series with AL1 or AL2.
5	AS	Logic input used to determine alerter frequency. This pin can be programmed via a microprocessor or mechanically set to provide an output frequency of 1200 Hz shifted to 1500 Hz (AS pin set to logic low or left open) or 1800 Hz shifted to 2250 Hz (AS pin set to logic high or pulled up to VS through a 100 kΩ resistor).
6 7 8	C3 C2 C1	Keypad inputs for columns 3 through 1 respectively. High-frequency touch-tone signals are controlled by these inputs. These inputs are disabled when the telephone goes on-hook. Single tones are generated when two rows or two columns are activated. Diagonals result in no tones. A high-frequency and allow frequency tone can be generated by connecting the appropriate column to the desired row pin by the way of the keypad crosspoint switch. An alternate method for generating a single high-frequency tone is to connect the appropriate column to VS through a 50 kΩ resistor.
9 10 11 12	R4 R3 R2 R1	Keypad inputs for rows 4 through 1 respectively. Low-frequency single tones are generated when two rows or two columns are activated. Diagonal selection results in no tones. A high-frequency and a low-frequency tone can be generated by connecting the appropriate row to the desired column pin by the way of the keypad crosspoint switch. An alternate method for generating a single low-frequency is to connect the appropriate row pin to RP through a 50 kΩ resistor.
13	OS	Resonator connection. A 480 kHz ceramic resonator is placed between this pin and RP. This resonator is used to provide the precise frequency required to generate the DTMF tones.
14	SG	Signal ground for use with the receiver output (RO) drive. The receiver can be placed between this pin and RO *without* a decoupling capacitor.
15	RO	Receiver output. Optimum receiver impedance is 600 Ω. The circuit will provide 2.0 dB less power to a 150 Ω receiver. A receiver can be placed between RO and RP or between RO and SG. If the receiver is connected between RO and RP, a decoupling capacitor must be used.
16	TX	Input from the handset transmitter which must be coupled through a capacitor.
17	TP	TIP-Prime is the device terminal which connects to the positive output of the polarity guard bridge (Functional Diagram).
18	NC	No connection. This pin should not be used as a tie point for external circuitry.
19	DR	A low impedance regulated output port. Currents (in the full feature mode) will provide a minimum of 800 μA for a maximum of 3.3 volts. Excess set current not used by internal circuits will appear on DR to power external circuits. Current not used by external circuits will be passed to RP via an external PNP transistor.
20	RP	RING-Prime is the device terminal which connects to the negative output of the polarity guard bridge. It is also the logic common (ground) point.

Testing Requirements

(At 25°C unless otherwise specified)

Characteristic	Test Condition	Min	Typ	Max	Unit
VS Current	Figure 3; Ring Detect	800	—	958	μA
Voltage (TP-to-RP)	Figure 4; Ring Detect	5.8	—	6.6	V
TP Current	Figure 5; Ring Detect	1.20	—	2.00	mA
Voltage (TP-to-RP), Speech	Figure 6				
	ITP Force = 8 mA	3.10	—	3.45	V
	ITP Force = 20 mA	3.70	—	4.50	V
	ITP Force = 90 mA	5.35	—	7.00	V
Voltage (VS-to-RP), Speech	Figure 7				
	ITP Force = 8.0 mA	2.50	—	2.78	V
	ITP Force = 20 mA	2.75	—	3.20	V
	ITP Force = 90 mA	5.00	—	6.10	V
Voltage (TP-to-RP), Dial	Figure 8				
	ITP Force = 20 mA	4.00	—	4.80	V
Dump Current, Dial	Figure 10				
	ITP Force = 20 mA	8.30	—	11.2	mA
	ITP Force = 90 mA	70.5	—	77.5	mA
Dump Current, Speech	Figure 13				
	ITP Force = 20 mA	9.30	—	12.1	mA
	ITP Force = 90 mA	71.5	—	78.5	mA
Upper Switch-Point, Speech	Figure 12	13.0	—	19.5	mA
Lower Switch-Point, Speech	Figure 13	10.0	—	17.0	mA
Hysteresis, Speech	Figure 12 test value				
	minus Figure 13 test value	2.0	—	—	mA
Lower Switch-Point, Dial	Figure 14	11.0	—	18.0	mA
Hysteresis, Dial	Figure 12 test value				
	minus Figure 14 test value	1.25	—	—	mA
Impedance, Speech	Figure 15	650	—	945	ohms
Transmit Gain	Figure 16				
	20 mA, RTX = 0 Ω	3.4	4.4	5.5	—
	90 mA, RTX = 0 Ω	2.9	4.0	5.5	—
Receive Gain	Figure 17				
	20 mA, RPO = 600 Ω	0.13	0.21	0.29	—
	90 mA, RPO = 600 Ω	0.09	0.21	0.45	—
Sidetone Gain	Figure 18				
	20 mA	0.6	0.8	1.1	—
	90 mA	0.4	0.8	1.3	—

Test Circuits

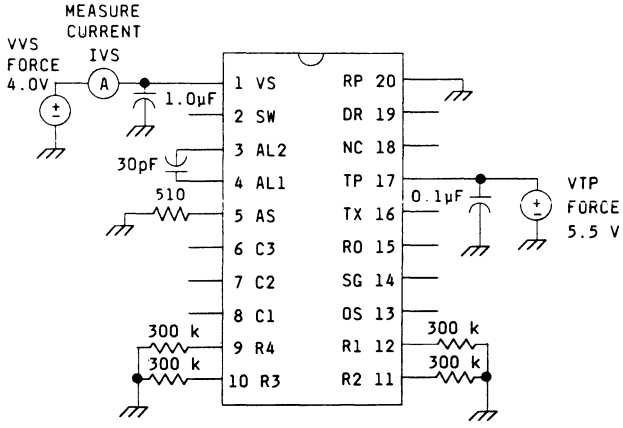
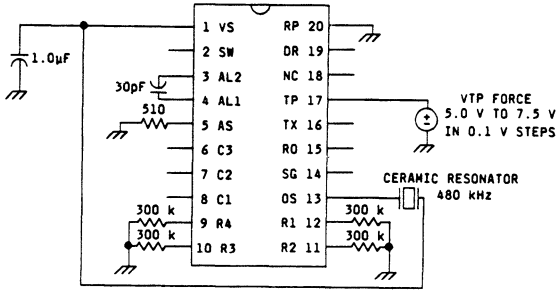
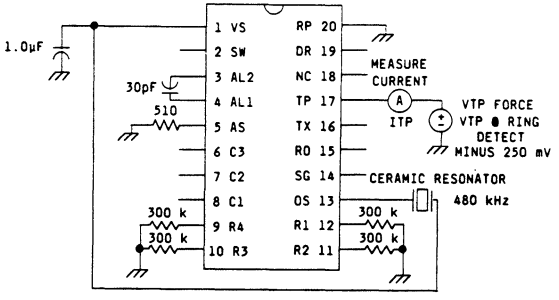


Figure 3. VS Current (Ring Detect)



The voltage on TP is ramped until the signal on either AL1 or AL2 (with respect to RP) exceeds 1.0 volts. Ring Detect is defined as the condition where voltage exceeds 1.0 volts on AL1 or AL2.

Figure 4. Voltage, TP-to-RP (Ring Detect)



ITP (for this test) is defined as the current in Pin 17 just prior to Ring Detect. Lower the voltage applied to pin 17 to a value which is 250 mV less than the TP Ring Detect voltage value (which was measured in Figure 4).

Figure 5. TP Current (Ring Detect)

Test Circuits
(Continued)

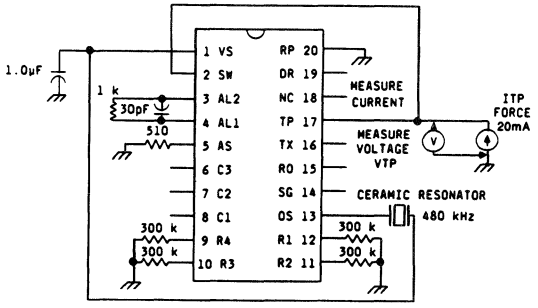


Figure 6. Voltage (TP-to-RP), Speech

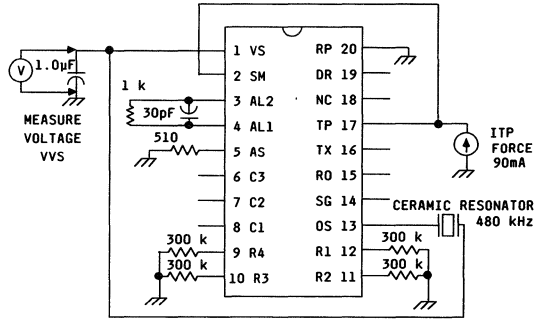


Figure 7. Voltage (VS-to-RP), Speech

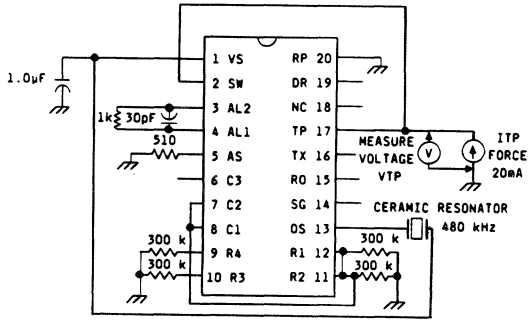


Figure 8. Voltage (TP-to-RP), Dial

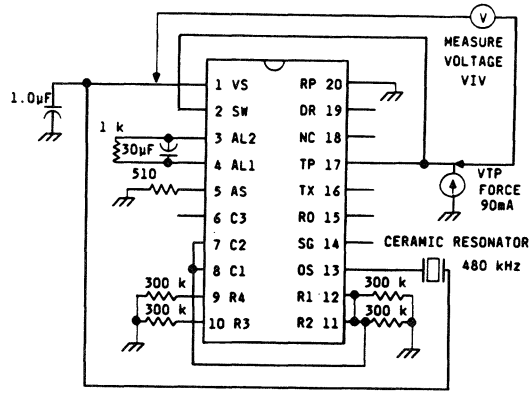


Figure 9. Voltage (TP-to-VS), Dial

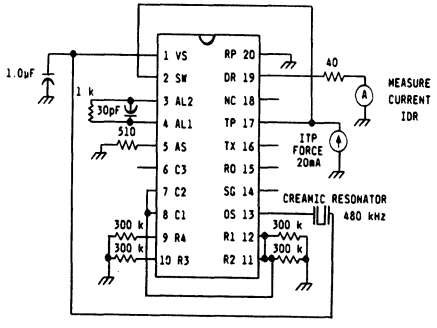


Figure 10. Dump Current, Dial

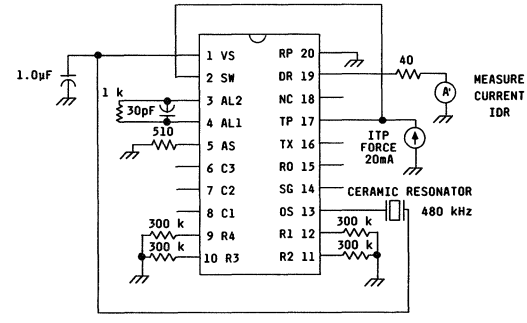


Figure 11. Dump Current, Speech

Test Circuits
(Continued)

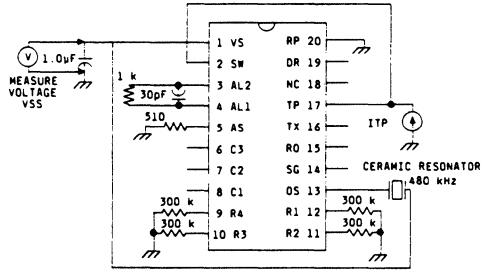
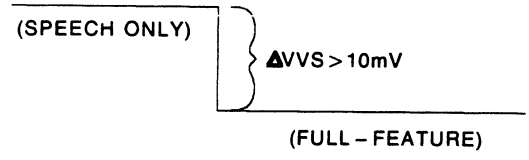


Figure 12. Upper Switch-Point, Speech

ITP is ramped up from 13 mA (in the range from 13 mA to 20.5 mA in 50 μA steps) until the *transition* from "speech only" to full-feature occurs. *Transition* occurs when the measured voltage (VVS) decreases as a step function ($\triangle$VVS > 10 mV).



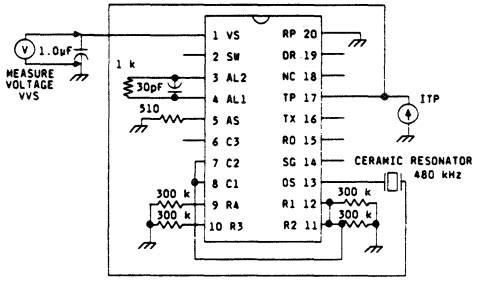
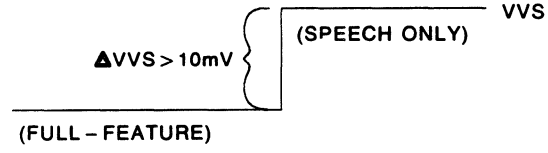


Figure 13. Lower Switch-Point, Speech

ITP is ramped down (starting at the value of current for which *transition* occured in the Figure 12 test, plus an additional 100 μA). As the current is ramped down in 50 μA steps, a *transition* will occur from "full-feature" to "speech-only". *Transition* occurs when the measured voltage (VVS) increases as a step function ($\triangle$VVS > 10 mV).



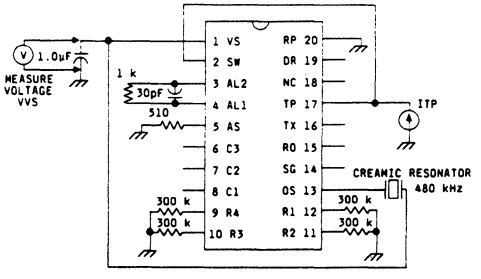
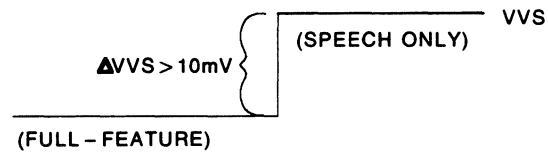


Figure 14. Lower Switch-Point, Dial

ITP is ramped down (starting at the value of current for which *transition* occured in the Figure 12 test, plus an additional 100 μA). As the current is ramped down in 50 μA steps, a *transition* will occur from "full-feature" to "speech-only". *Transition* occurs when the measured voltage (VVS) increases as a step function ($\triangle$VVS > 10 mV).



Test Circuits
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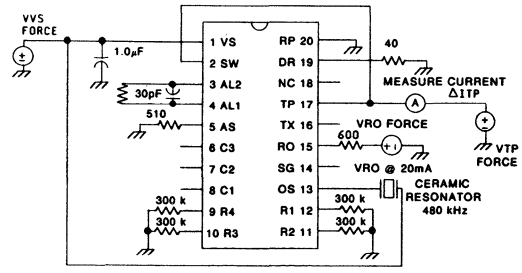


Figure 15. Impedance, Speech

VVS FORCE VALUE: Same as the voltage measured on Pin 1 when the current sourced into TP (Pin 17) is 20 mA.

VRO FORCE VALUE: Same as the voltage measured on Pin 15 when the current sourced into TP (Pin 17) is 20 mA and TX (Pin 16) opens.

VTP FORCE VALUE: Same as the voltage measured on Pin 17 when 20 mA is sourced into Pin 17.

SET IMPEDANCE: A 1.0 Vdc step (△VTP) is added to the VTP Force Value.
Set Impedance (AIN) = △VTP/△ITP.

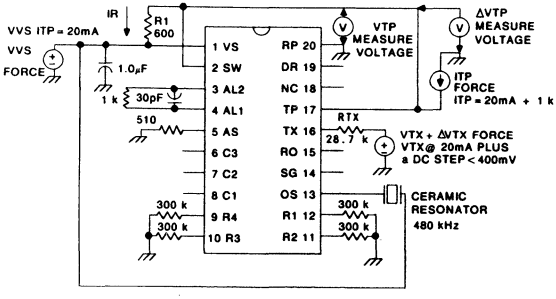


Figure 16. Transmit Gain

DETERMINE THE VALUE OF IR: Force 20 mA into TP (Pin 17) with TX (Pin 16) open and R1 disconnected. Measure VVS voltage (Pin 1) and VTP voltage (Pin 17). The, IR (in mA) = [(VTP − VVS)/600] times 1000.

DETERMINE VTS: Force 20 mA into TP (Pin 17) with TX (Pin 16) open and R1 disconnected. Measure VTX voltage (Pin 16).

TRANSMIT GAIN: Gain = (△VTP/△VTX)(−1): where △VTX is chosen to be a value ≤ 400 mVdc and △VTP is the difference when measuring VTP for determining the value of IR, and measuring VTP with connections shown in Figure 16.

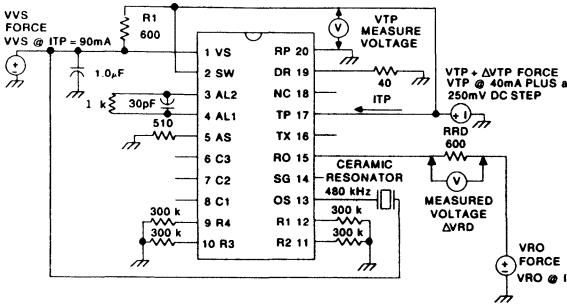
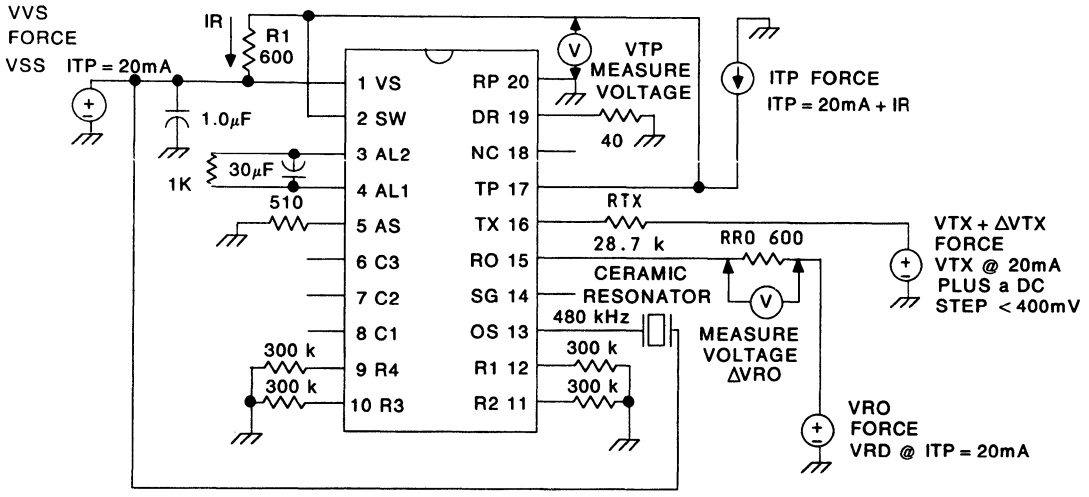


Figure 17. Receive Gain

DETERMINE THE VRO, VTP AND VVS "FORCE" VALUES: Force 90 mA into Tp (Pin 17) with R1 disconnected. Measure voltages on Pins 15, 17 and 1 respectively.

RECEIVE GAIN: Connect R1 and apply VRO Force, VVS Force and VTP Force plus △VTP (where △VTP is 250 mVdc referenced to VTP Force). Gain = (△VRO/△VTP)(−1); where △VRO is the difference when measuring VRO for determining VRO Force, and measuring VRO with the connections shown in Figure 17.

Test Circuits
(Continued)



DETERMINE THE VALUE OF IR AND RECORD VRO VOLTAGE: Force 20 mA into RP (Pin 17) with TX (Pin 16) open and R1 disconnected. Measure VVS voltage (Pin 1), VTP voltage (Pin 17) and VRO voltage (Figure 18). Then, IR (mA) = [(VTP − VSS)/600] times 1000.

DETERMINE VTX FORCE VOLTAGE: Force 20 mA into TP (Pin 17) with TX (Pin 16) open and R1 disconnected. Measure VTX voltage (Pin 16).

SIDETONE GAIN: Gain (△VRO/△VTX); where △VTX is chosen to be a value ≤ 400 mVdc and △VRO is the difference when measuring VRO for determining the value of IR, and measuring VRO with the connections shown in Figure 18.

Figure 18. Sidetone Gain

Functional Descriptions

Ringing Alerter

The ringing detector determines the presence of a true incoming signal by incrementing an up/down counter, depending upon the instantaneous magnitude of the incoming signal. It also provides an on-hook Type B ringer equivalency. Alerter outputs AL1 and AL2 can be used to drive an external piezoelectric transducer. The load can also be applied from AL1 to RP for single-ended drive or between AL2 and AL2 for differential push-pull drive (larger amplitude). The volume can be reduced by placing resistors in series with the load. The alerting signal is a square wave alternating between 1300 2250 Hz with AS high (or 1200/1500 Hz with AS low) at a 20 Hz repetition rate.

Polarity Guard

An external bridge rectifier ensures proper voltage polarity on the device, with a minimum voltage drop across the bridge rectifier.

Functional Descriptions
(Continued)

Oscillator

An external 480 kHz ceramic resonator, in conjunction with an internal oscillator control circuit, is used to provide timing functions for logic circuits. Panasonic EFO-A480K01, Murata CSB480E or similar type ceramic resonators can be used.

Power Conditioner

This set of circuits provides accurate temperature compensated current and voltage references for the other circuit blocks. It also sets the loop loading and digital reset states for the various types of operation, i.e., on-hook, off-hook, and multiple telephone sets. For loop currents greater than 5.0 mA, the DR port can be used to power an electret preamplifier or an external LED.

Speech Network

This analog circuit block provides proper transmission levels in both directions. Since the local talker's signal is larger than (on the average) the received signal at the telephone set terminals, an out-of-phase portion of the transmitted signal is also sent to the receiver via the normal sidetone path (sidetone is that portion of the speaker's voice which is purposely fed back to the receiver to prevent the phone from sounding too "dead"). The DTMF D/A converter is placed in the transmit path during dialing, while the receive-gain path is simultaneously attenuated.

Tone Generation Table

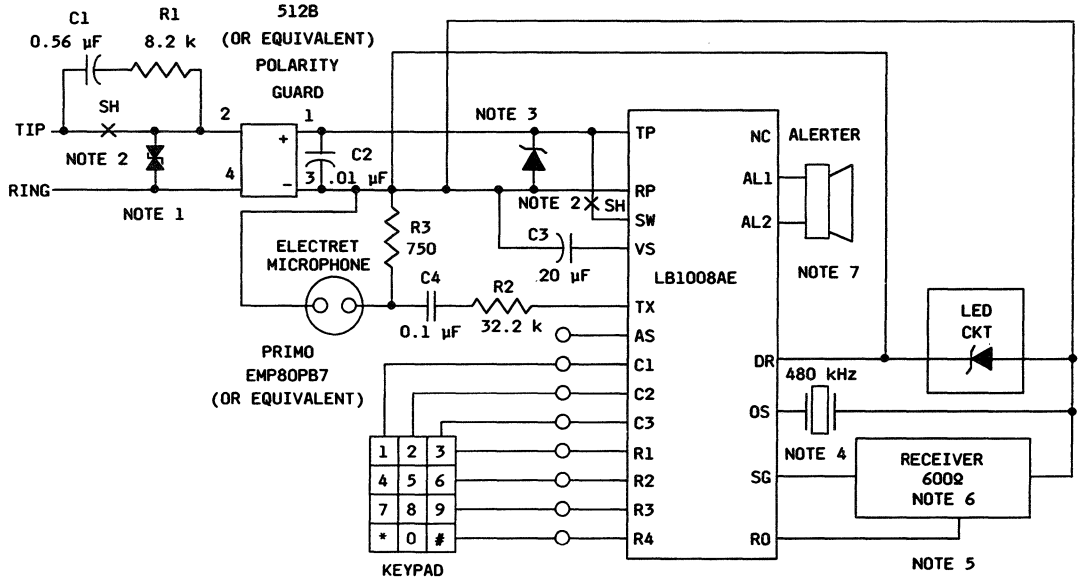
Pin Name	Keypad Input	Tones (Design Value)
R1	Row 1	697 Hz
R2	Row 2	770 Hz
R3	Row 3	852 Hz
R4	Row 4	941 Hz
C1	Column 1	1209 Hz
C2	Column 2	1336 Hz
C3	Column 3	1477 Hz

Applications

External Components

Only two switchhook contacts are required with this device. In going off-hook, the contact connected to the SW pin should open simultaneously with, or before, the other switchhook contact. As shown in the functional diagram, the LB1008AE needs only five capacitors (only four capacitors if a 5-wire interface is used as shown in Figure 19 and 20), three resistors, a ceramic resonator, a surge protection diode and a polarity guard to provide all of the basic touch-tone electronic functions. An alerter, a telephone handset (containing the transmitter and receiver) and a keypad are also illustrated.

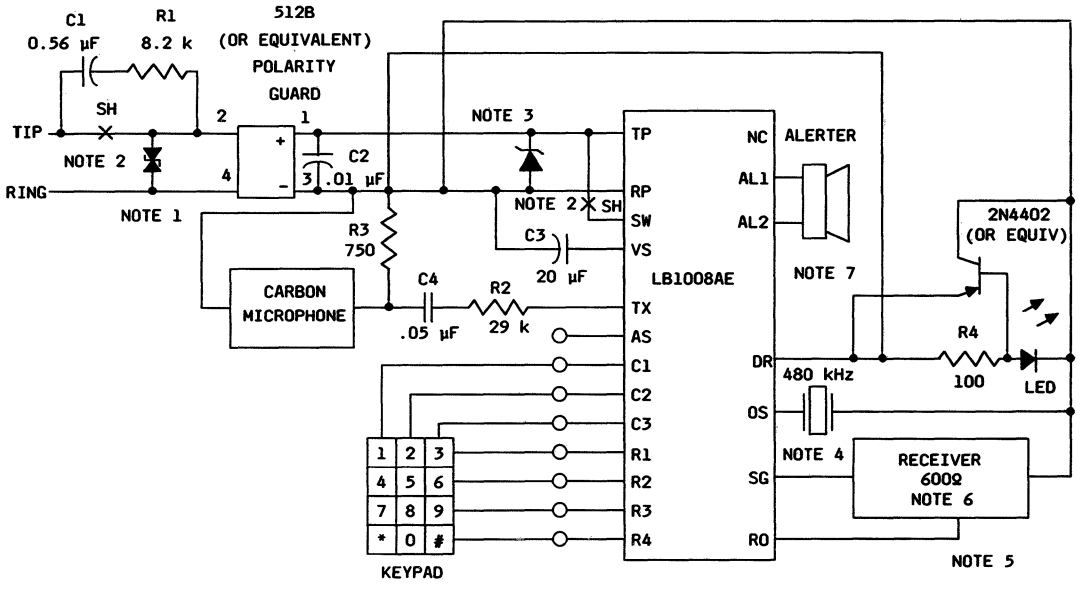
The application diagrams (see Figures 19 and 20) contain detailed parts and connection information. The LB1008AE can be used with a telephone handset which uses an electret or carbon microphone as a transmitter.



Notes on page 9-34.

Figure 19. Typical Electret Microphone Application Diagram, LB1008AE (5-Wire Handset Interface)

Applications
(Continued)



Notes Below

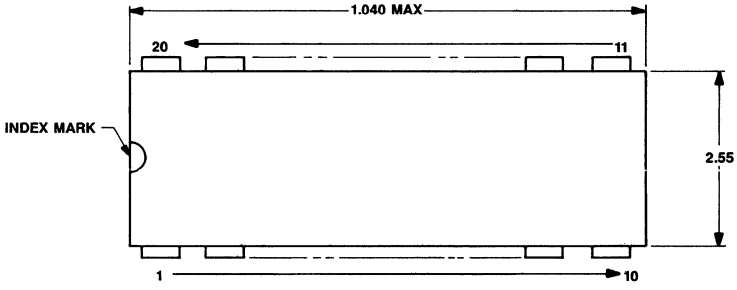
Figure 20. Typical Carbon Microphone Application Diagram, LB1008AE (5-Wire Handset Interface)

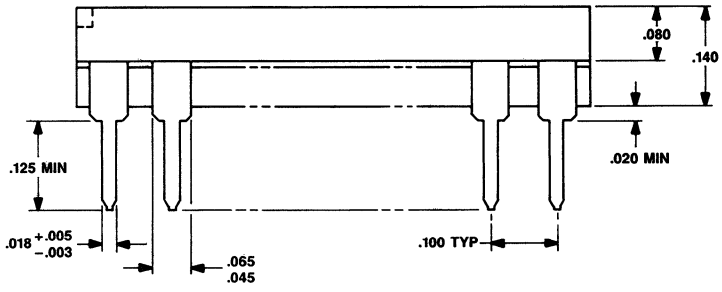
Notes (Figures 19 and 20):

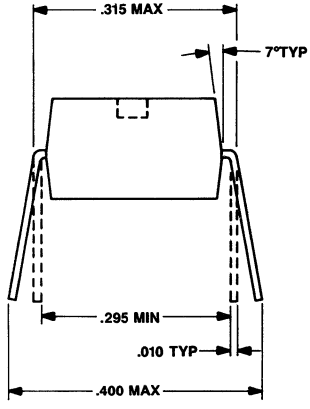
1. This surge protector must protect the particular polarity guard being used. The peak inverse voltage rating of the polarity guard must never be exceeded. The surge protector may be an AT&T 813BA, 75 volts, 1 watt device (or equivalent) when used with an AT&T 512B polarity guard.
2. SH denotes switchhook.
3. TP to RP voltage should not exceed 18 volts nominally. An 0.75-watt (minimum), 18-volt (5%) regulator diode should be connected as shown.
4. Panasonic EFO-A480K01, Murata CSB480E or similar device.
5. See Functional Diagram for a 4-wire Handset Interface.
6. See PIN DESCRIPTION (Pin 15) for 150 ohm receivers.
   Use AT&T MR-3 (600Ω Receiver with varistor; COMCODE 103670037) or similar device.
   Use AT&T MR-3N (600Ω Receiver without varistor; COMCODE 104041272) or similar device.
7. Several types of alerters manufactured by Murata (or equivalent) may be used with the LB1008AE device. The AT&T COMCODE ordering numbers for these Murata devices are as follows:
   1800 Hz - COMCODE 845403989
   1800 Hz - COMCODE 845484476
   1800 Hz - COMCODE 845775147

Outline Drawing

(Dimensions in Inches)







Note: Pin numbers are for reference only.

Ordering Information

Device	Comcode
LB1008AE	104208780

MICROPROCESSOR-CONTROLLED, SINGLE-CHIP-TELEPHONE IC

LB1009-TYPE

PRELIMINARY

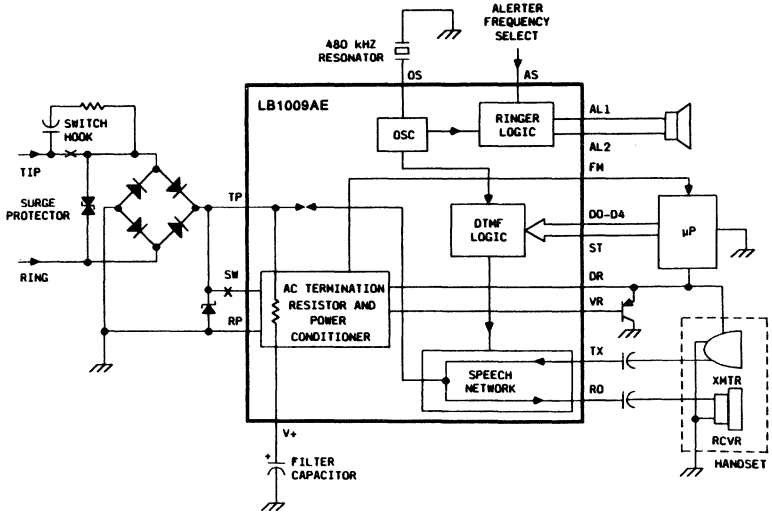
Description

The LB1009 requires only a few external components (see Figure 10) to provide all of the touch-tone electronic functions. This integrated circuit furnishes ac and dc loop termination for both switchhook states, transmits and receives voice signals to the central office, provides dual-tone multi-frequency (DTMF) signals to the central office, and properly distinguishes between spurious noise and genuine ringing signals, providing a distinctive audible alerter output. The LB1009 is offered as the LB1099AE with a 600 ohm receiver output impedance and the LB1009BE with a receiver output impedance of zero ohms.

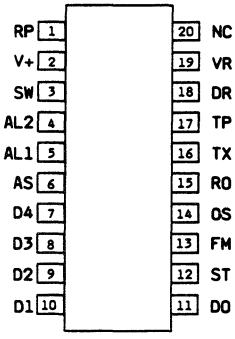
Features

- An alerter select option of 1200/1500 Hz or 1800/2250 Hz
- Capable of speech transmission down to 3 mA loop current
- Compatible with electret microphones
- Provides a power port (DR) for driving a microprocessor or LED
- A feature-mode function indicates power port status
- Requires only a 2-contact switchhook

Functional Diagram



Pin Diagram



Maximum Ratings (At 25°C unless otherwise specified)	
Ambient Operating Temperature Range	0 to 60°C
Storage Temperature Range	−40 to +125°C
Pin Soldering Temperature (t = 15 s max.)	300°C
Voltage (TP)	20 V
Current (TP)	120 mA
Power Dissipation	500 mW

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Characteristics

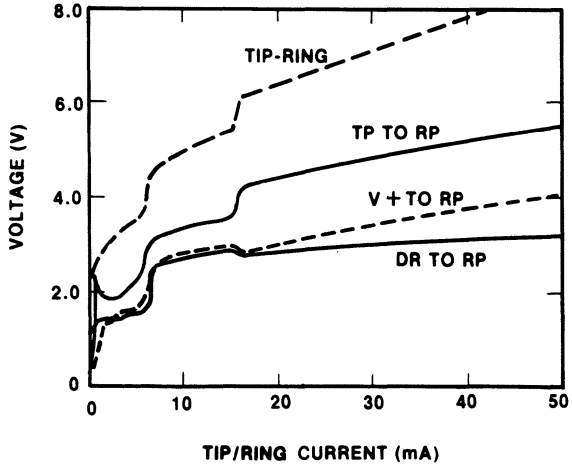


Figure 1. Typical V-I Characteristics (Dial Mode)

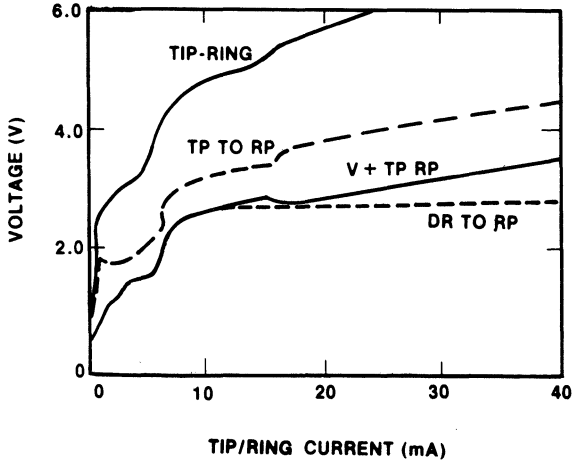


Figure 2. Typical V-I Characteristics (Speech Mode)

Pin Description Key

Pin	Symbol	Name/Function
1	RP	The RING-Prime terminal is the more negative input connected to the Tip-Ring on the negative side of the polarity guard bridge. It is also the logic common (ground) point.
2	V+	The most positive dc voltage (filtered) on the device. This voltage is derived from the Tip-Ring inputs. It is used to supply internal circuits.
3	SW	Turns on transmit/receive circuitry when connected through switchhook contact to TP.
4 5	AL2 AL1	Output terminals for driving an alerter. The ringer logic distinguishes between genuine ringing and other noise signals present on the telephone loop, and provides a distinctive audible output. The alerter can be driven differentially or single ended. If the alerter is driven single ended to RP, the second output can be used to drive a visible indicator to RP. Volume can be adjusted by placing a resistor in series with terminals AL1 or AL2.
6	AS	Logic input used to determine alerter frequency. This pin can be programmed via a microprocessor or mechanically set to provide an output frequency of 1200 Hz shifted to 1500 Hz (AS pin set to logic low or left open), or 1800 Hz frequency shifted to 2250 Hz (AS pin set to logic high or pulled up to V+ through a 100 kΩ resistor).
7 8 9 10 11	D4 D3 D2 D1 D0	DTMF signals are controlled by these inputs via a microprocessor. These inputs are disabled when the telephone goes on-hook and in the low power mode (FM open). These inputs are CMOS and TTL compatible. See Figure 9.
12	ST	Data strobe from microprocessor. It loads the DTMF inputs on a rising edge pulse.
13	FM	Feature Mode is an open collector output which shorts to RP when the telephone goes off-hook. Long loops (with two telephones off-hook) can result in a "speech-only, low power" mode of operation. FM will "open circuit" under these conditions.
14	OS	Resonator connection. This logic is designed to operate with some 480 kHz ceramic resonators. The resonator frequency is divided down to perform various synchronous clock tasks.
15	RO	LB1009AE receiver output. Optimum receiver impedance is 600 ohms. The circuit will provide 2 db less power to a 150-ohm receiver. LB1009BE receiver output. Receiver output impedance is 0 Ω. Desired receiver matching impedance should be added in series with the receiver.
16	TX	Input from transmitter, capacitively coupled.
17	TP	The TIP-Prime terminal is the more positive input to the Power Conditioner and Speech Network. It connects to Tip-Ring on the positive side of the polarity guard bridge.
18	DR	A low impedance regulated port for powering a microprocessor and transmitter. Currents (in the full feature mode) will provide a minimum of 800 μA for a maximum of 3.3 volts. Excess set current not used by internal circuits will appear on DR to power external circuits. Current not used by external circuits will be passed on to RP via an external PNP transistor.
19	VR	This voltage is a reference when the set is off-hook. When connected to DR via a PNP transistor (see Figure 2), a regulated voltage is produced on DR.
20	NC	No connection. This pin should not be used as a tie point for external circuitry.

Electrical Characteristics

(At 25°C unless otherwise specified)

Characteristic	Test Condition	Min	Typ	Max	Unit
Off-Hook DC Tests					
TP Voltage (Figure 3)	I_{TP} = 8 mA, Speech	—	3.50	—	V
	I_{TP} = 20 mA, Speech	3.80	—	4.40	V
	I_{TP} = 90 mA, Speech	5.40	—	6.80	V
	I_{TP} = 20 mA, Dialing	3.90	—	4.50	V
V+ Voltage (Figure 3)	I_{TP} = 8 mA, Speech	—	2.50	—	V
	I_{TP} = 20 mA, Speech	2.80	—	3.20	V
	I_{TP} = 90 mA, Speech	—	5.50	—	V
Voltage (TP-V+)	I_{TP} = 20 mA, Dialing (Figure 3)	1.10	—	—	V
Driver Current (Figure 3)	I_{TP} = 20 mA, Dialing	7.50	—	10.50	mA
TP Current, Speech (Figure 3)	Upper Switch Point, Speech	15.00	—	19.70	mA
	Lower Switch Point, Speech	12.00	—	16.00	mA
TP Hysteresis Current, Speech (Figure 3)	Upper Switch Point, Speech minus Lower Switch Point, Speech	4.30	—	—	mA
TP Current, Dialing (Figure 3)	Lower Switch Point, Dialing	13.00	—	18.00	mA
TP Hysteresis Current, Dialing (Figure 3)	Upper Switch Point, Speech minus Lower Switch Point, Dialing	1.25	—	—	mA
Receiver Output Offset Voltage Referenced to One-Half of V+ (Figure 3)	I_{TP} = 20 mA, Speech	−200	—	200	mV
	I_{TP} = 20 mA, Dialing	−300	—	350	mV
Off-Hook AC Tests					
Transmit Gain (vTP/vTX, Figure 4) @ 1 kHz	I_{TP} = 8 mA, vTX = 50 mVrms	—	4.00	—	—
	I_{TP} = 20 mA, vTX = 100 mVrms	—	3.80	—	—
	I_{TP} = 90 mA, vTX = 100 mVrms	—	2.50	—	—
Receive Gain (vRO/vTP, Figure 5) @ 1 kHz	I_{TP} = 20 mA, vTP = 500 mVrms	—	0.21	—	—
	I_{TP} = 90 mA, vTP = 500 mVrms	—	0.21	—	—
Transmit Impedance (vTX/iTX, Figure 4)	I_{TP} = 20 mA, vTX = 100 mVrms	—	30K	—	Ω
Receiver Output Impedance (vRO/iRO, Figure 6) (LB1009AE)	I_{TP} = 20 mA, vRO = 100 mVrms	—	600	—	Ω
TP Impedance (vTP/iTP, Figure 5)	I_{TP} = 20 mA, vTP = 500 mVrms	650	700	945	Ω
	I_{TP} = 90 mA, vTP = 500 mVrms	550	—	850	Ω
SDT Gain (V_{RCG}/vTX, Figure 4) @ 1 kHz	I_{TP} = 8 mA, vTX = 100 mVrms	—	0.32	—	—
	I_{TP} = 20 mA, vTX = 100 mVrms	—	0.62	—	—
	I_{TP} = 90 mA, vTX = 100 mVrms	—	0.70	—	—
vTP, Low Group Out (Figure 4), L1-L4	I_{TP} = 20 mA See Note 1	0.291	0.425	—	Vrms
vTP, High Group Out (Figure 4), H1-H3	I_{TP} = 20 mA See Note 1	0.367	0.532	—	Vrms

Electrical Characteristics (Continued)

(At 25°C unless otherwise specified)

Characteristic	Test Condition	Min.	Typ	Max	Unit
Off-Hook AC Tests (Continued)					
VTP, Total DTMF, both High and Low Groups (Figure 4)	I_{TP} = 20 mA, Dialing See Note 1	—	0.679	0.869	Vrms
Transmit gain, vTP/vTX (Figure 4) @ 1 kHz	I_{TP} = 20 mA, Dialing, No Tone vTX = 100 mVrms Apply "Dial No-Tone" Vector	—	0.010	—	—
On-Hook DC Tests					
TP Current (Figure 7)	V_{TP} = 3 V	—	—	35.0	μA
TP Voltage, Threshold of Detection (Figure 7)	Ringing Detected	6.2	—	7.0	V
TP Current (Figure 7)	V_{TP} = 10 V V_{TP} = 20 V	1.5 1.5	— —	2.0 2.5	mA mA
On-Hook AC Tests					
Alerter Voltage vAL2-vAL1 (Figure 8)	V_{TP} = 10V V_{TP} = 20 V	5.0 15.0	— —	7.0 17.0	V_{PP} V_{PP}

Test Circuits

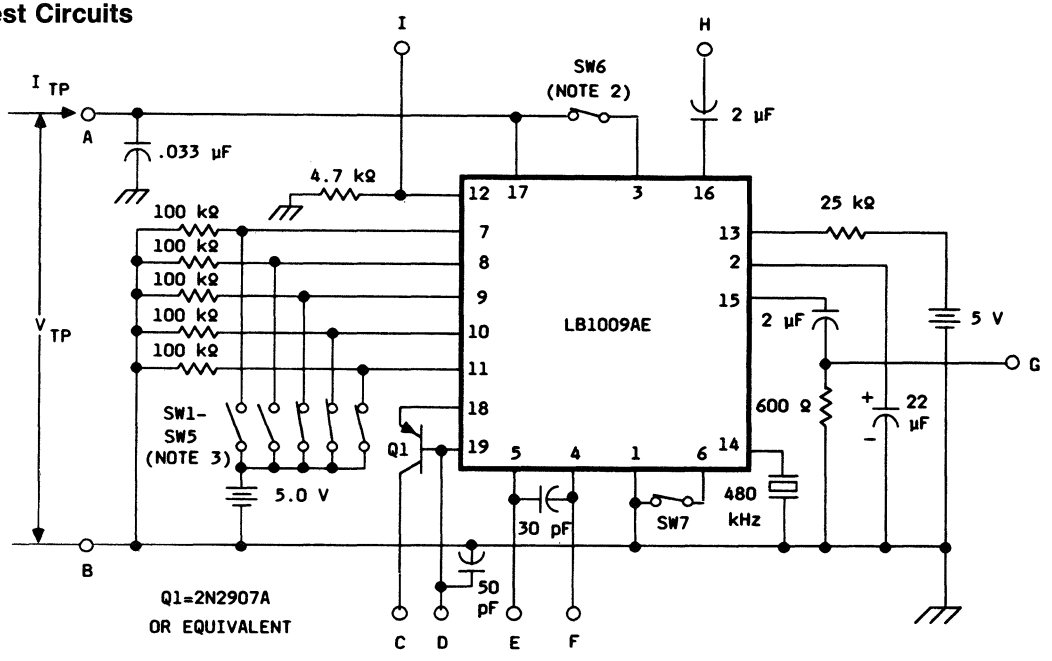


Figure 3a. OFF Hook dc Test Circuit

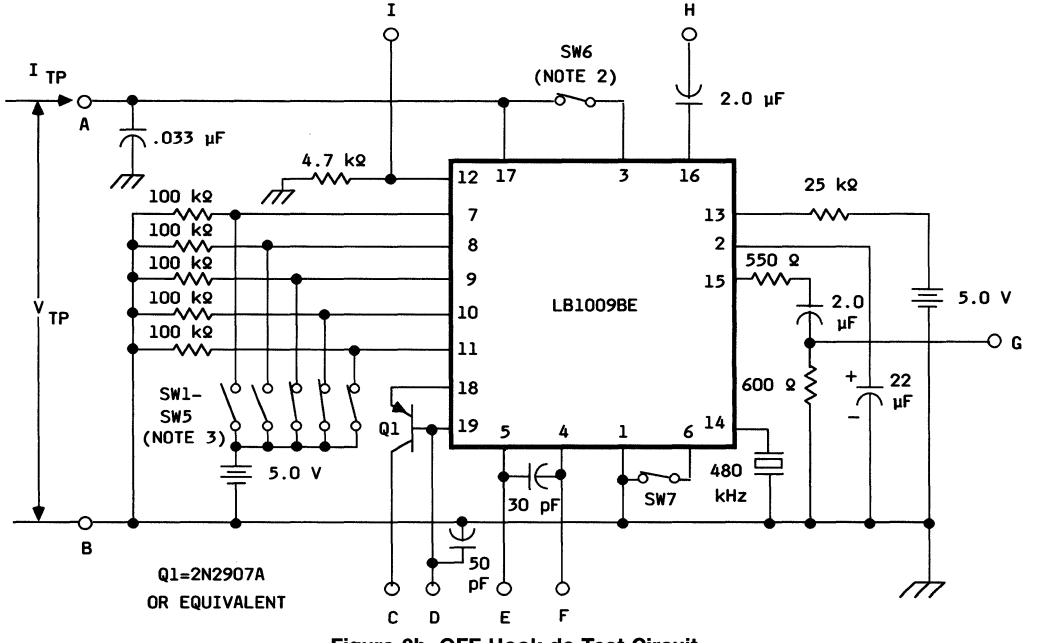


Figure 3b. OFF Hook dc Test Circuit

Notes:

1. The DTMF levels are measured with a true RMS meter capable of measuring up to 100 kHz. The measurements reflect the fundamental and harmonics of the tone.
2. SW6 is closed for on-hook tests and open for off-hook tests.
3. Switches are shown in the speech position.

Test Circuits
(Continued)

When using test Figure 4 thru 8, reference Figures 3a and 3b.

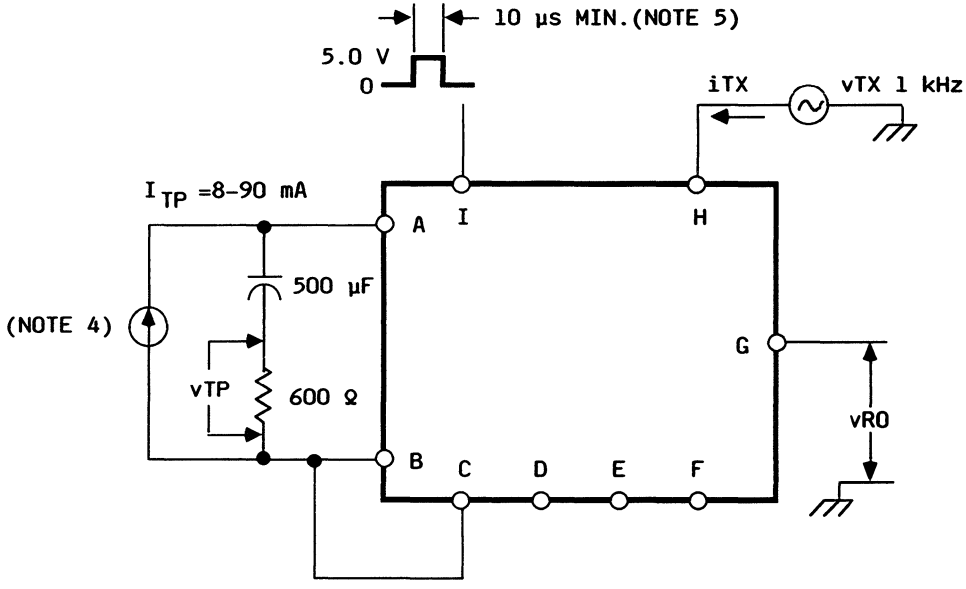


Figure 4. OFF Hook ac Test Circuit 1

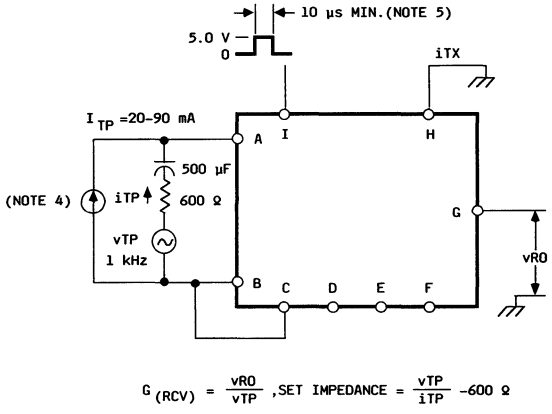


Figure 5. OFF Hook ac Test Circuit 2

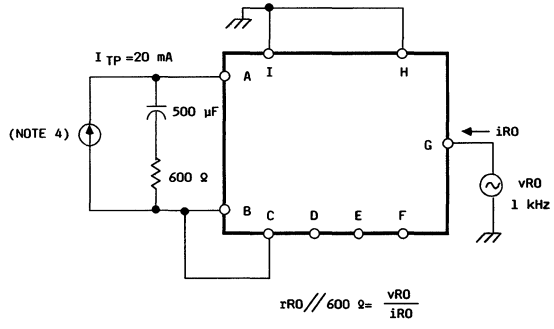


Figure 6. OFF Hook ac Test Circuit 3

Notes:
4. A current source with an ac impedance of 90 kΩ or greater at 1 kHz is required.
5. When changing digital vectors, a strobe is needed to latch the data into the port.

Test Circuits (Continued)

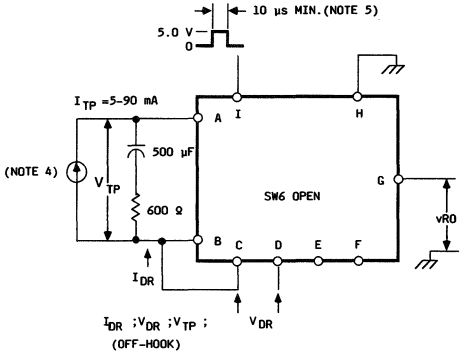


Figure 7. ON Hook dc Test Circuit

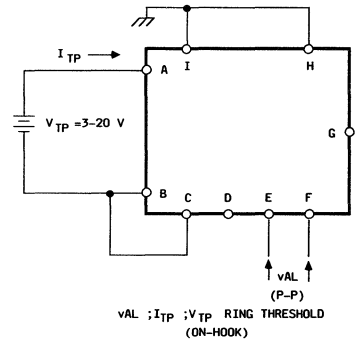


Figure 8. ON Hook ac Test Circuit

Functional Descriptions (See Functional Diagram)

DTMF Generation Logic

This circuit connects to a microprocessor. The logic circuitry decodes the microprocessor input states to generate accurately timed digital control signals for a D/A converter.

Ringing Logic

This circuit determines the presence of a true incoming ringing signal by up or down counting, depending upon the instantaneous magnitude of an incoming signal. After a positive decision, the logic provides suitable timed inputs to an external alerter device. Volume can be controlled by placing resistors in series with pins AL1 or AL2. See "AS" pin description for alerter frequency-selected capability.

Polarity Guard

An external bridge rectifier ensures proper voltage polarity on the device, with a minimum voltage drop across the bridge rectifier.

Oscillator

An external 480 kHz ceramic resonator, in conjunction with an internal oscillator control circuit, is used to provide timing functions for logic circuits. Panasonic EFO-A480K01, Murata CSB480E or similar type ceramic resonators can be used.

Power Conditioner

This set of circuits provides accurate temperature-compensated current and voltage references for the other circuit blocks. It also sets the loop loading and digital reset states for the various types of operation, i.e., on-hook, off-hook, and multiple telephone sets.

Speech Network

This analog circuit block provides proper transmission levels in both directions. Since the local talker's signal is larger than (on the average) the received signal at the telephone set terminals, an out-of-phase portion of the transmitted signal is also sent to the receiver. This portion is designed to provide a level in the talker's ear (the "sidetone") between "too hot" and "dead". The DTMF D/A converter is placed in the transmit path during dialing, while the receive-gain path is simultaneously attenuated. Trasmit mute is provided independently of receive mute and is under control of the microprocessor. Transmit mute is not functional in the speech-only mode (telephone set current is below approximately 16 mA). When transmit mute is functional, it provides a minimum of 40 dB attenuation.

Driver (DR) and Voltage Regulator (VR) Ports

See Pin Description Key.

Applications

External Components

Only two switchhook contacts are required with this device. In going off-hook, the contact connected to the SW pin should open simultaneously with, or before, the other switchhook contact. As shown in the functional diagram, the LB1009 needs only four capacitors, two resistors, a ceramic resonator, a transistor, a surge protection diode and a polarity guard to provide all of the basic touch-tone electronic functions. An alerter, a telephone handset (containing the transmitter and receiver) and a microprocessor are also illustrated.

The application diagram (see Figure 10) contains detailed information. The LB1009 can be used in a 4-wire handset application.

DTMF Signal Inputs					Mode of Operation	Tones (Design Value)	
D4	D3	D2	D1	D0			
1	0	0	0	*	Dial	L1 (697 Hz)	Single Tones
1	0	1	0	*	Dial	L2 (770 Hz)	
1	1	0	1	0	Dial	L3 (825 Hz)	
1	1	1	1	0	Dial	L4 (941 Hz)	
1	1	*	0	0	Dial	H1 (1209 Hz)	
1	1	*	0	1	Dial	H2 (1336 Hz)	
1	0	*	1	0	Dial	H3 (1477 Hz)	
0	0	0	0	0	Dial	H1, L1 [1]	DTMF Tones
0	0	0	0	1	Dial	H2, L1 [2]	
0	0	0	1	0	Dial	H3, L1 [3]	
0	0	1	0	0	Dial	H1, L2 [4]	
0	0	1	0	1	Dial	H2, L2 [5]	
0	0	1	1	0	Dial	H3, L2 [6]	
0	1	0	0	0	Dial	H1, L3 [7]	
0	1	0	0	1	Dial	H2, L3 [8]	
0	1	0	1	0	Dial	H3, L3 [9]	
0	1	1	0	0	Dial	H1, L4 [*]	
0	1	1	0	1	Dial	H2, L4 [0]	
0	1	1	1	0	Dial	H3, L4 [#]	
*	0	0	1	1	Speech, Transmit Mute		Special Functions
*	0	1	1	1	Speech (Note 6)		
*	1	0	1	1	Dial, No Tone (Note 7)		

* = Don't Care

Figure 9. Microprocessor Control Logic Table

Notes:
6. The device power-up in the speech mode.
7. The device enters dial mode, but generates no tones.

Applications
(Continued)

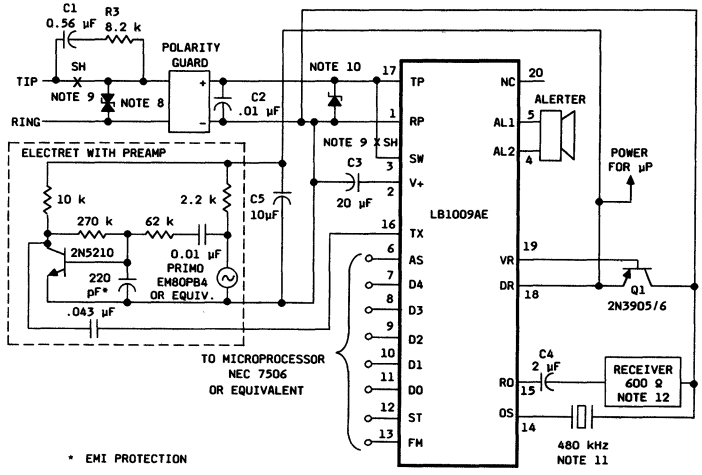


Figure 10a. Typical Application Diagram

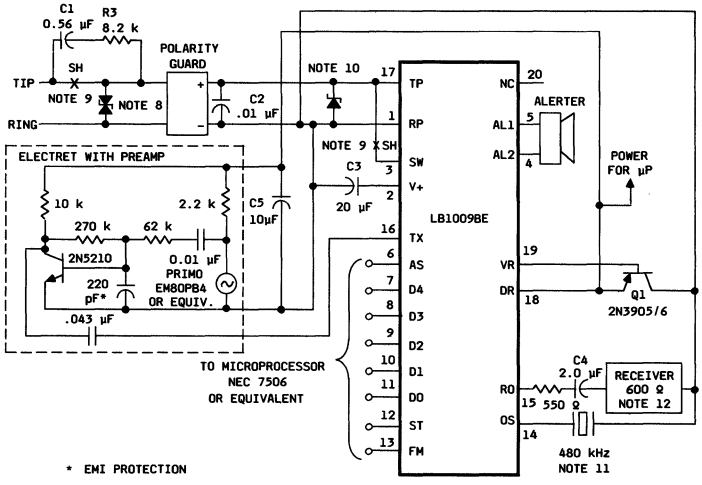


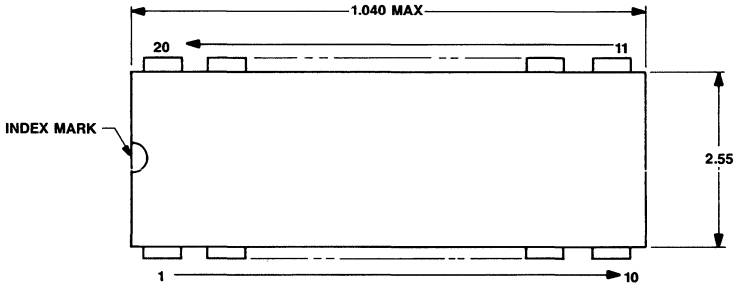
Figure 10b. Typical Application Diagram

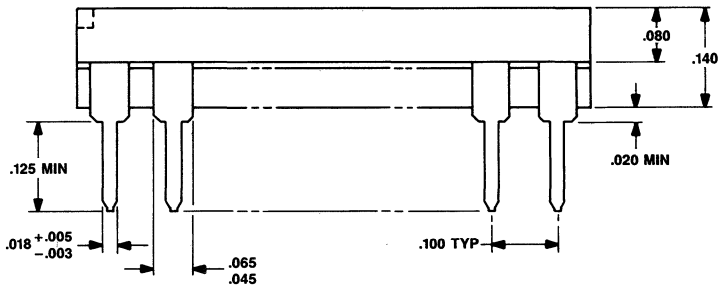
Notes:

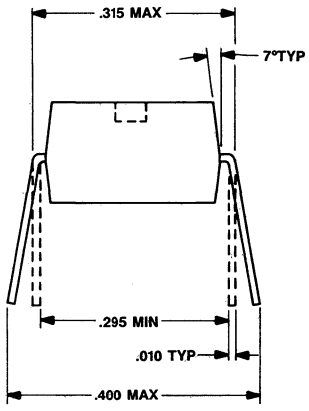
8. This surge protector must protect the particular polarity guard being used. The peak-inverse voltage rating of the polarity guard must never be exceeded.
9. SH denotes switchhook.
10. TP to RP voltage should not exceed 18 volts nominally. An 0.75-watt (minimum), 18-volt (±5%) regulator diode should be connected as shown.
11. Panasonic EFO-A480K01. Murata CSB480E or similar device.
12. See PIN DESCRIPTION (Pin 15) for 150 Ω receivers.
    Use AT&T MR-3 (600Ω Receiver with varistor; COMCODE 103670337) or similar device.
    Use AT&T MR-3N (600 Ω Receiver without varistor; COMCODE 104041272) or similar device.

Outline Drawing

(Dimensions in Inches)







Note: Pin numbers are for reference only.

Ordering Information

Device	Comcode
LB1009AE	104208798
LB1009BE	104405089

Description

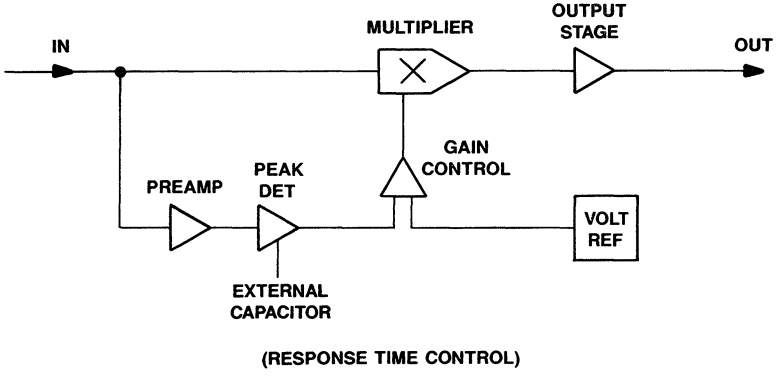
The LB1026AA/AB is a voice frequency level expander used to condition amplified signals from electret-type microphones in telephone handsets. The function of this device is to attenuate low-level signals that typically originate from background noise, and pass normal amplitude speech signals at unity gain. With this device the quality of conversation is enhanced for both the speaker, by way of receiver sidetones, and the listener, by reducing background sounds that might be heard during the speaker's silence. This device is particularly suited for office and industrial telephone applications where the suppression of undesirable background noise during lulls in conversation is desired.

A 1.0 μF response-time control capacitor must be provided by the user if the specified attack and decay times are to be obtained. The LB1026AA is supplied in wafer form to the customer, who is responsible for the subsequent processing to obtain a usable device. Each chip has six pads for wire bond attachment (Figure 4).

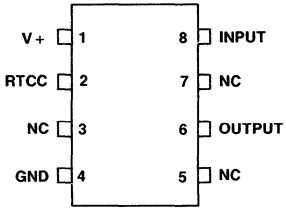
Features

- Reduces transmitted background noise during pauses in conversation
- Provides unity-gain transmission of normal amplitude voice signals
- Operates from 2- to 15-volt power supply
- Available in wafer form (LB1026AA) and 8-pin plastic DIP (LB1026AB)

Functional Diagram



Pin Diagram



Maximum Ratings*

(T_A = 25°C unless otherwise specified)

Rating	Value	Unit
Operating Voltage (V+ to Ground)	25	V
Temperature Storage Range	−40 to +125	°C
Pin Temperature (Soldering, 15 s)	300	°C
Ambient Operating Temperature Range	0 to 50	°C

* Stresses in excess of those listed in the Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition in excess of those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating condtions for extended periods may affect device reliability.

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

The test circuit shown in Figure 1 applies for all tests.

Parameter	Min	Typ	Max	Unit
Power Supply Voltage	2.0	—	15	V
Power Supply Current at 15 V	—	—	1.0	mA
Power Supply Current at 3.0 V	—	—	700	μA
Output Voltage, R_L = 6k ohms**	—	—	1.0	V_{PP}
Maximum Input Gain Ratio (Input = 353 mVrms, pin 8)	0.94	—	1.15	—
High-Level Gain Ratio (Input ≥ 50 mVrms)	0.94	—	1.1	—
Mid-Level Gain Ratio (Input = 12.5 mVrms)	0.38	—	0.6	—
Low-Level Gain Ratio (input = 1.0 mVrms)	0.19	—	0.28	—
Attack Time†	10.5	—	17.5	ms
Decay Time††	105	—	175	ms
Input Resistance	—	25	—	kΩ

** With less than 3% THD.

† Attack time is defined as the time required for the output voltage (Vo) to settle within 90 to 100% of the steady-state output voltage after the input voltage (Vi) is changed in less than 1.0 ms. from 3.16 mVrms to 31.6 mVrms.

†† Decay time is defined as the time required for the output voltage (Vo) to settle within 100 to 110% of the steady-state output voltage after the input voltage (Vi) is changed in less than 1.0 ms from 31.6 mVrms to 3.16 mVrms.

Test Circuit

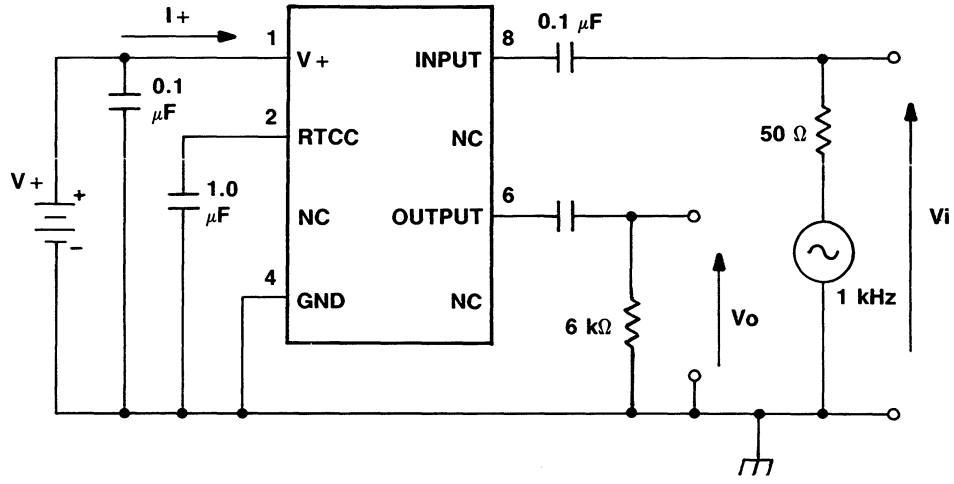


Figure 1. LB1026AB Test Circuit

Pin Description Key

Pin	Symbol	Name/Function
1	V+	Connection for the power supply voltage
2	RTCC	Response Time Control Capacitor
3	NC	No Connection. This pin should not be used as a tie point.
4	GND	Circuit common. Not necessarily physical or system ground.
5	NC	No connection. This pin should not be used as a tie point.
6	OUTPUT	Device output. This connects to subsequent telephone speech network circuitry.
7	NC	No connection. This pin should not be used as a tie point.
8	INPUT	Input signal

Application

The following information summarizes the basic operation of a voice frequency level expander in electret-type microphone applications.

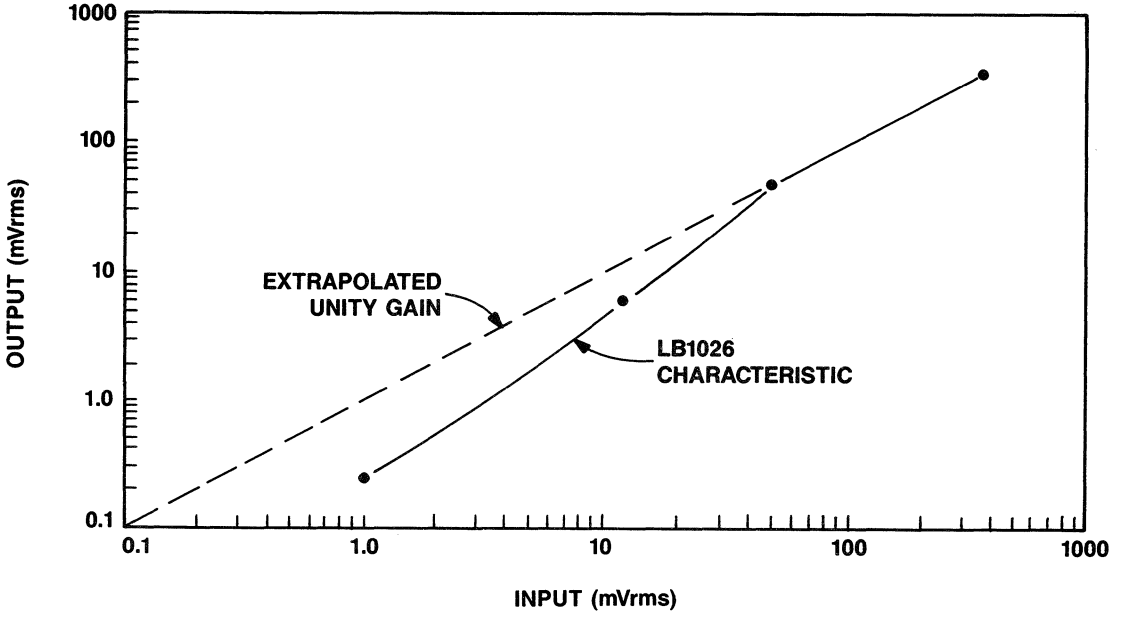


Figure 2. Typical Expander Characteristics

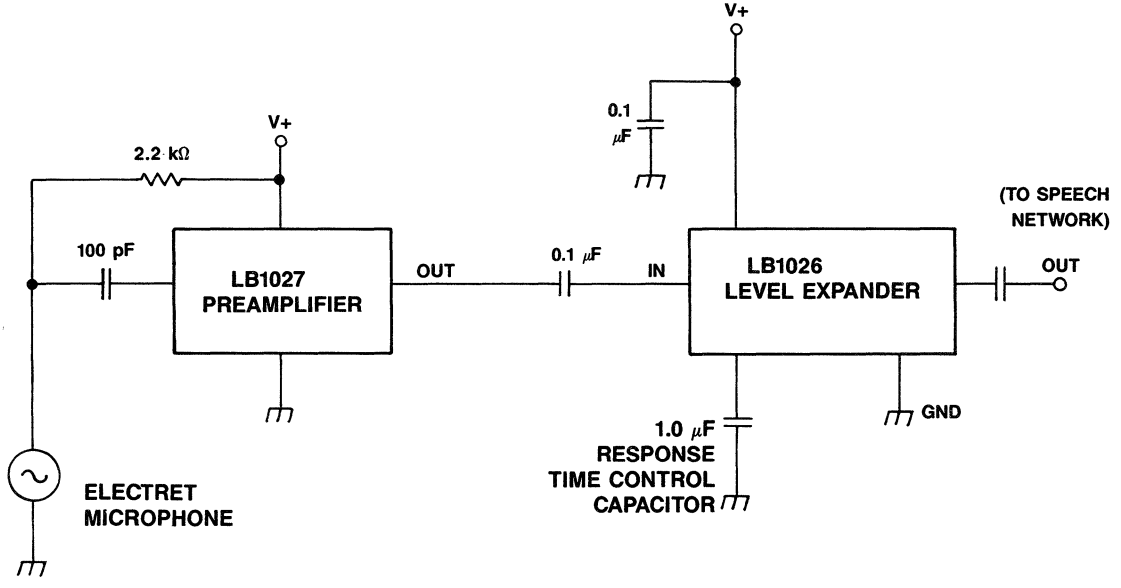
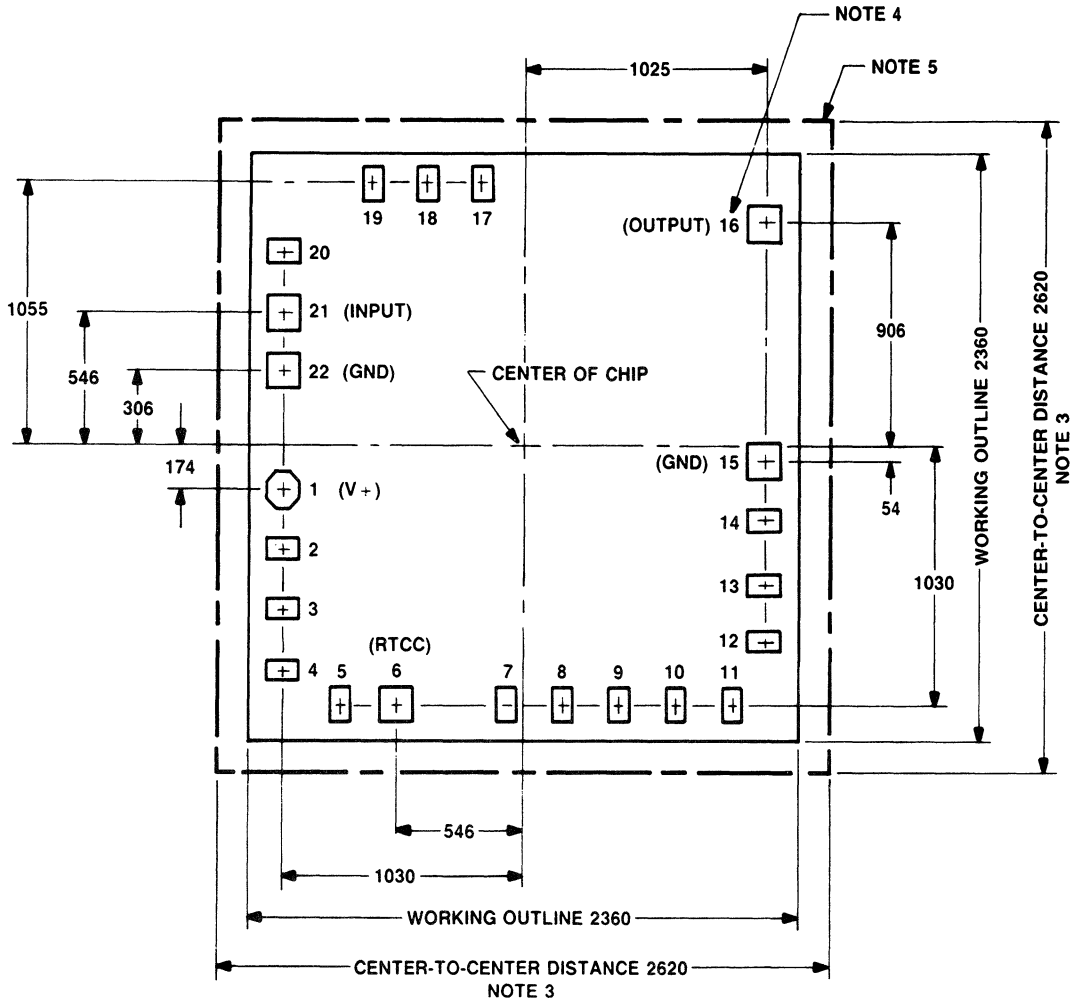


Figure 3. LB1026AA/AB Level Expander Application Diagram

Outline Drawings

(Notes 1, 2)



Notes:

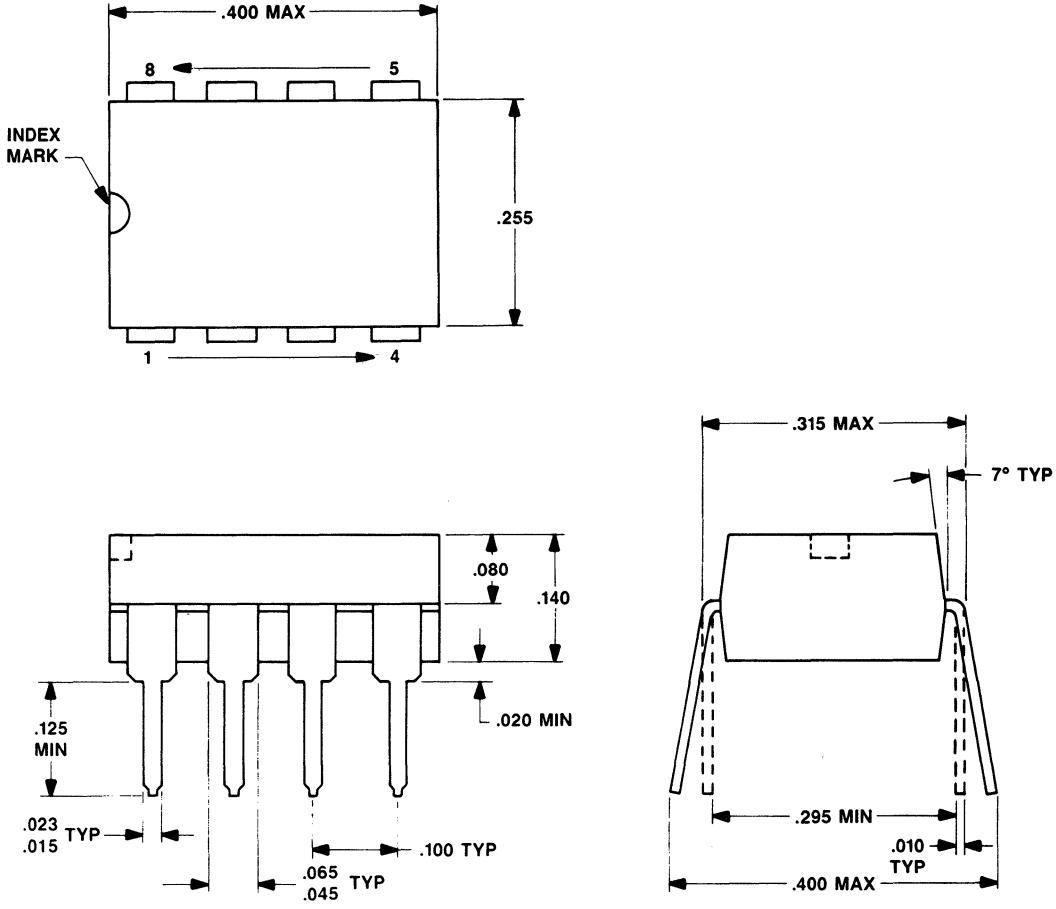
1. All dimensions are shown for reference only.
2. Bonding pads 1, 6, 15, 16, 21, and 22 are 140 x 140 microns. Bonding pad #1 is a reference point and can be identified by its octagon shape; e.g. 2, 3, 4, etc. are located by counting CCW from bonding pad #1. Refer to Figure 4 for description and dimension locations. All other pad numbers are used by AT&T during wafer fabrication to trim the circuit. They are not to be used as bonding pads. The dimensions of the pads are 80 x 140 microns.
3. The actual chip size equals the center-to-center dimension less the saw kerf width, typically 50 to 70 microns.
4. Chip pad numbers are for reference only and do not appear on the chip. The complete metallization pattern is not shown.
5. The thickness may vary as determined by the wafer diameter used in fabrication. However, the thickness dimension shall be in the range of 480 microns (0.0188 inch) minimum and 700 microns (.0275 inch) maximum.

Figure 4. LB1026AA Wafer Drawing (Dimensions in Microns)

Outline Drawing

(Dimensions in Inches)

8-Pin Plastic DIP (LB1026AB)



Note: Pin numbers are shown for reference only

Ordering Information

Device	Comcode
LB1026AA	104208970
LB1026AB	104208988

ELECTRET PREAMPLIFIER

LB1027AA/AB

PRELIMINARY

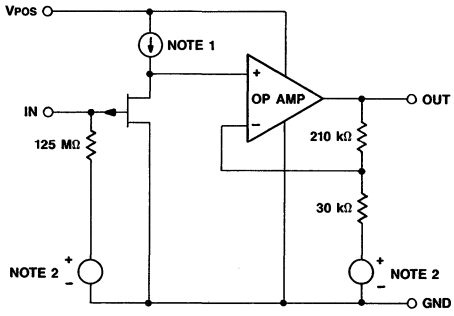
Description

The LB1027AA/AB Electret Preamplifier has been specifically designed for electret microphone (voice frequency) applications. It operates from a supply voltage of 15 volts down to 1.6 volts with no performance degradation. The Electret Preamplifier is supplied in wafer form (LB1027AA) which requires subsequent processing, or in an 8-pin plastic DIP (LB1027AB).

Features

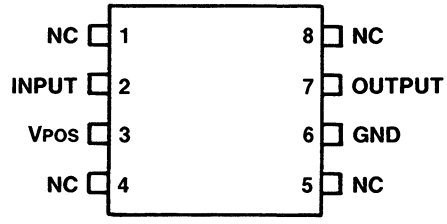
- Input impedance of 125 M Ω (in parallel with 2.5 pF)
- Low power drain (< 327 μA at 4 V)
- AC voltage gain of 18 dB
- 600 mV peak-to-peak output voltage swing
- Typical output resistance of 50 Ω

Functional Diagram



NOTES:
1. INTERNAL CURRENT SOURCE.
2. EFFECTIVE INTERNAL VOLTAGE SOURCE.

Pin Diagram



Maximum Ratings (at 25°C unless otherwise specified)	
Ambient Operating Temperature Range	−20 to +70°C
Storage Temperature Range	−40 to +125°C
Power Dissipation	100 mW
Voltage (V+ to GND)	18 V
Input Current	±10 μA
Output Current	±1 mA
Pin Temperature (Soldering, 15 s)	300°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Characteristics

Pad/Pin Descriptions

Symbol	LB1027AA	LB1027AB	Description
VPOS	2	3	Positive-Supply Voltage
GND	4	1	Ground
IN	3	2	Input (See Source Requirements below)
OUT	1	4	Output (See Load Requirements below)
BLANK		1, 4, 5, 8	Not internally connected—May be used as tie points provided the ratings are not exceeded.

Source Requirements (See Figure 1)

The LB1027 is optimized (for PSSR) where Cs = 12 pF, but will work with any value consistent with its input impedance. The low-frequency roll-off point is determined by Cs. Direct current into the input should be ± pA. The LB1027 is designed for ac input signals less than 20 mV peak-to-peak (low-frequency response may degrade with larger input peaks). Signals greater than 70 mV peak-to-peak may be asymmetrically clipped.

Load Requirements (See Figure 1)

CL can be any value consistent with the desired output low-frequency roll-off characteristic. Values of Cs, RL, maximum signal frequency and output voltage swing must be chosen so as not to exceed the LB1027 output drive current capability (+ 80 μA, −250 μA).

The LB1027 will output a 600 mV p-p signal to > 4 kHz without clipping or slew-rate limiting (when RL = 10k and CSTRAY ≤ 5000 pF). it is recommended that CSTRAY not exceed 5000 pF in any event.

Electrical Specification (TA = 25°C unless otherwise specified)

Characteristic	Min	Typ	Max	Unit
Power-Supply Current				
V+ = 1.5 V	160	—	300	
V+ = 4.0 V	160	230	327	μA
V+ = 15 V	160	—	350	
Operating Supply Voltages				
Maximum	—	15	—	V
Minimum	—	1.1	—	
DC Output Currents				
Positive Drive; VIN = 1.5 V, V+ = 4.0 V	80	110	—	μA
Negative Drive; VIN = 0.9 V, V+ = 4.0 V	−250	−430	—	

Characteristics
(Continued)

Characteristic/Test Condition	Min	Typ	Max	Unit
dc Quiescent Output Voltage				
V+ = 1.6 V	0.32	0.40	0.9	
V+ = 4.0 V	0.35	0.55	1.05	V
V+ = 15V	0.35	0.80	1.20	
DC Output Voltages				
Positive Swing; V_{IN} = 1.5 V, V+ = 4.0 V	1.5	0.6	—	V
Negative Swing; V_{IN} = 0.9 V, V+ = 4.0V	—	0.6	0.1	
ac Voltage Gain f = 1.0 kHz, C_{IN} = 1000 pF, V_{IN} = 14 mVrms **Note:** Circuit frequency response is flat to within ± 0.5 dB (DC to 10 kHz)	16.8	18.0	19.3	dB
Input Impedance				
Resistive	—	125	—	MΩ
Capacitive (capacitive source = 12 pF)	—	2.5	—	pF
Capacitive Driving Ability	—	0.01	—	μF
Output Resistance	—	50	—	Ω
Low Frequency Response (−3 dB point) Capacitive Source = 12 pF	—	80	—	Hz

Applications

The following simplified diagram summarizes the requirements for optimized operation of the LB1027 electret preamplifier.

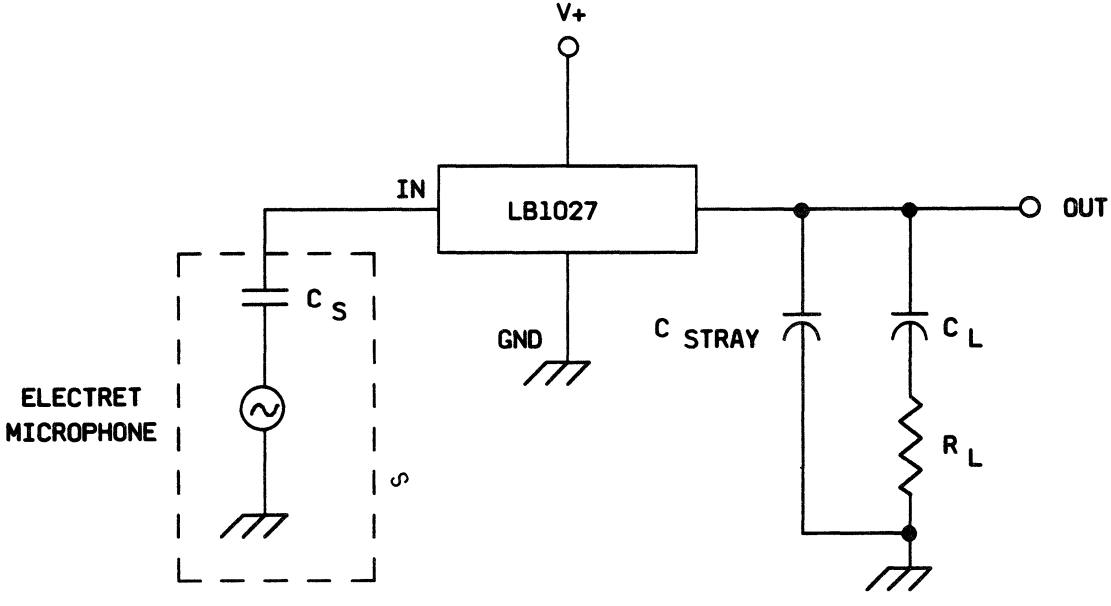
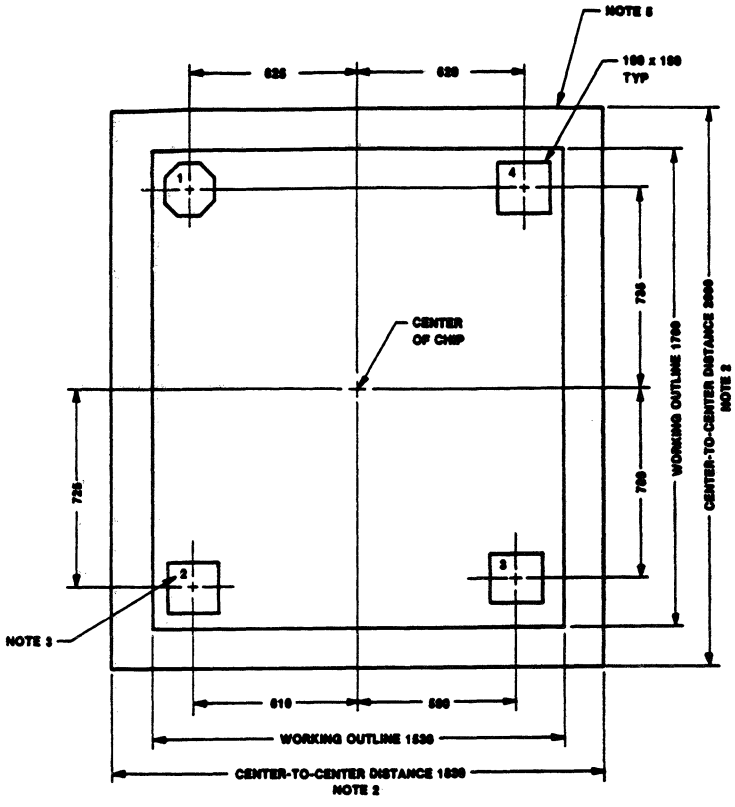


Figure 1. LB1027 Electret Preamplifier Application Diagram

Outline Drawing

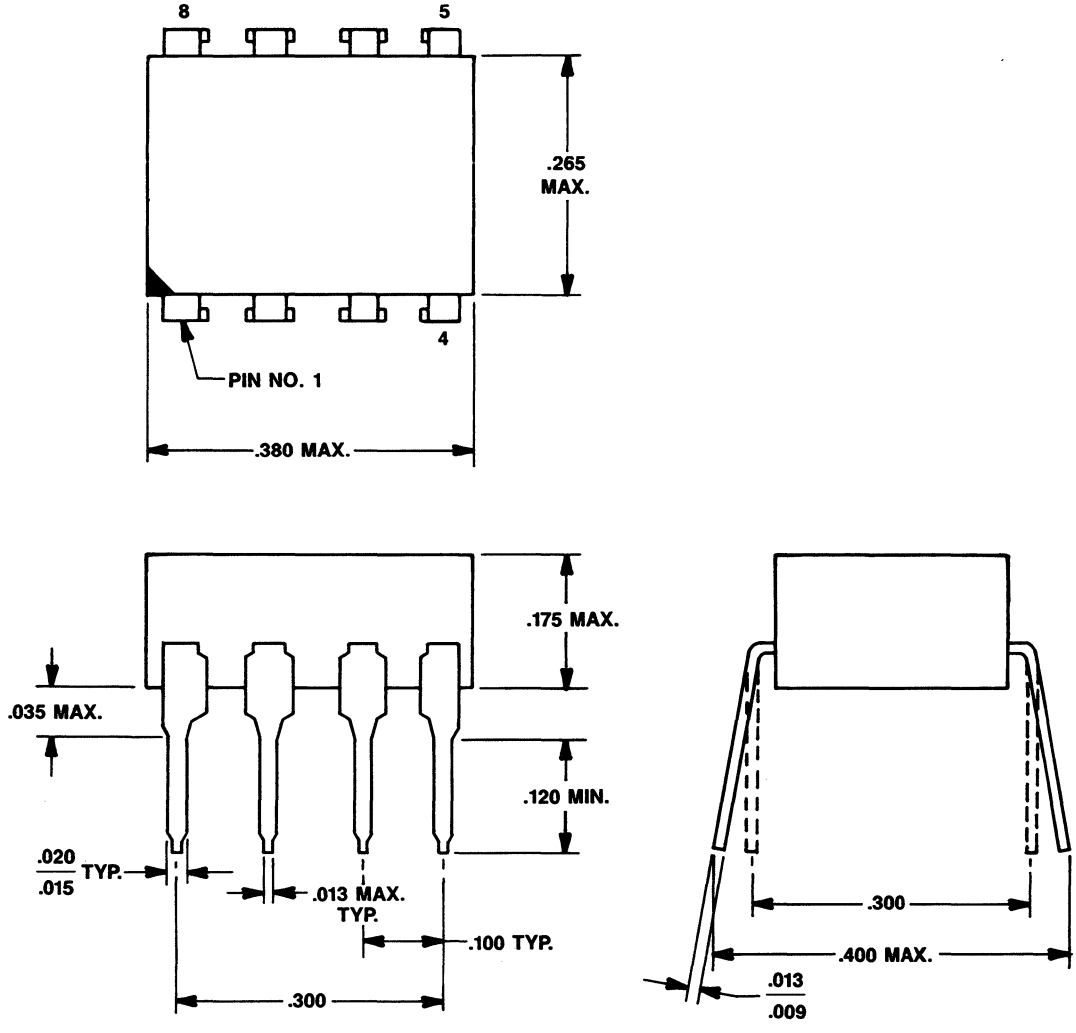


NOTES:

1. ALL DIMENSIONS ARE REFERENCE DIMENSIONS AND ARE SHOWN IN MICROMETERS.
2. THE ACTUAL CHIP SIZE EQUALS THE CENTER-TO-CENTER DIMENSION LESS THE SAW KERF WIDTH. TYPICALLY 50 TO 70 MICROMETERS.
3. CHIP PAD NUMBERS ARE FOR REFERENCE ONLY AND DO NOT APPEAR ON THE CHIP.
4. THE COMPLETE METALLIZATION PATTERN IS NOT SHOWN.
5. THE THICKNESS MAY VARY AS DETERMINED BY THE WAFER DIAMETER USED IN FABRICATION. HOWEVER, THE THICKNESS DIMENSION WILL BE IN THE RANGE OF 480 MICROMETERS (.0189 INCHES) MINIMUM AND 700 MICROMETERS (.0275 INCH) MAXIMUM.

Outline Drawing

(Dimensions in Inches)



Ordering Information

Device	Comcode
LB1027AA	104208996
LB1027AB	104413760

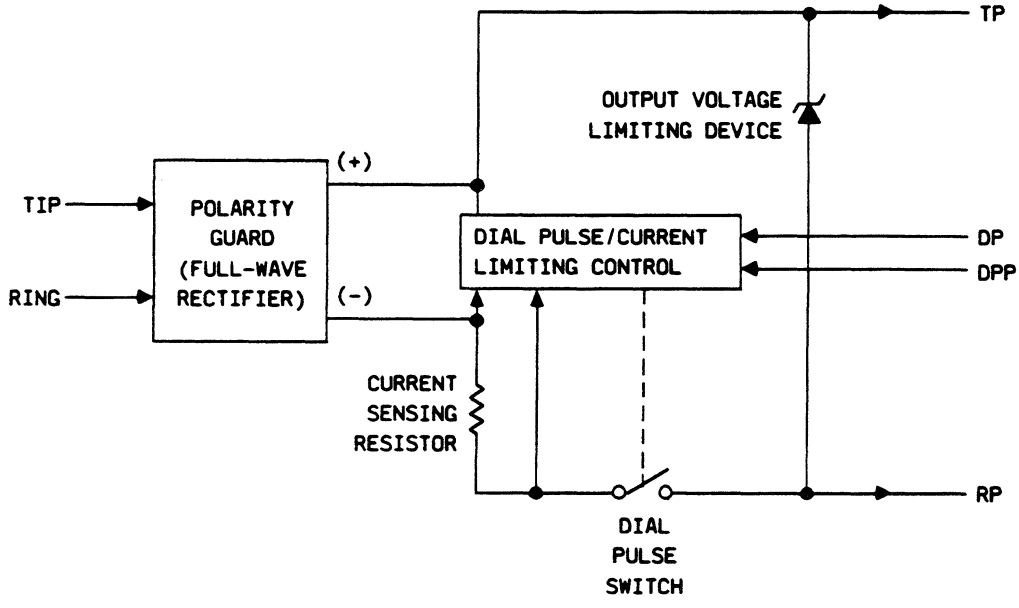
Description

The LH1028BB Telephone Interface Circuit (TIC) is a product fabrication of monolithic high-voltage BCDMOS technology and dielectric isolation. This integrated circuit performs the following basic functions: high-voltage dial-pulse switching, protection against reversal of TIP-RING polarity from the Central Office, and overvoltage/overcurrent protection of telephone circuits.

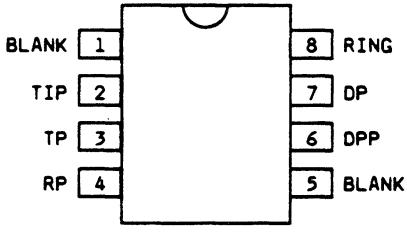
Features

- Withstands telephone loop voltages to 155 volts
- Operates at low TIP-RING voltages (typically as low as 2.7 volts)
- Minimal internal voltage drop across polarity guard
- Monolithic solid-state construction allows for greater reliability and physical area conservation

Functional Diagram



Pin Diagram



Maximum Ratings (At 25°C unless otherwise specified)	
Ambient Operating Temperature Range	0 to 50°C
Storage Temperature Range	−40 to +125°C
Pin Soldering Temperature (t = 15 s max.)	300°C
Voltage, (TIP-RING)	155 V
Power Dissipation (Package Limitation)	750 mW

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may affect device reliability.

Pin Description

Pin	Symbol	Name/Function
1 5	BLANK	These pins may be used as a tie point for external components. Voltages applied to these pins should not exceed 155 volts.
2	TIP	Input from TIP terminal of central office.
3	TP	TIP Prime. Positive output of the polarity guard (see Functional Diagram).
4	RP	RING Prime. Negative output of the polarity guard (see Functional Diagram).
6	DPP	Dial-pulse control voltage is applied between Dial Pulse (DP) and Dial-Pulse Prime (DPP) pins. See APPLICATIONS for a functional description of this control voltage.
7	DP	Dial-pulse. Control pin for internal dial-pulse switching.
8	RING	Input from RING terminal of central office.

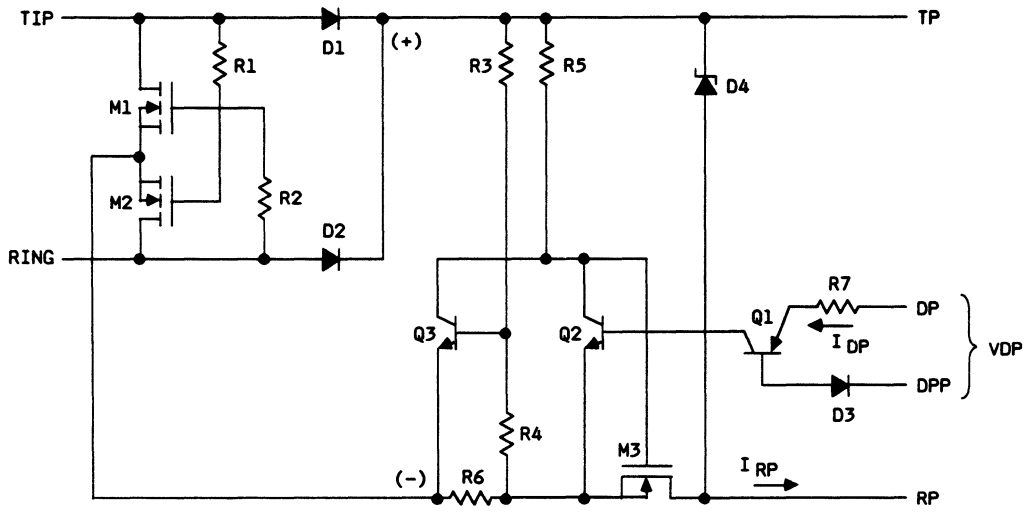


Figure 1. Simplified Schematic Illustrating Symbology of Characteristics

Testing Description (At 25°C unless otherwise specified)

CHARACTERISTIC	TEST CONDITION	MIN	MAX	UNIT
Breakdown Voltage (TIP-RING)	Figure 2; V_{DP} = 2.0 V, R_L = 1000Ω, Increase V_{T-R} until I_{T-R} = 3.0 mA	155	—	V
Off-State Leakage	Figure 2; V_{DP} = 2.0 V, R_L = 200 Ω, V_{T-R} = 78.8 V, Measure I_{T-R}	—	1.0	mA
Current Limiting	Figure 2; V_{DP} = 0.65 V, R_L = 40 Ω, V_{T-R} = 12 V, Measure I_{T-R}	155	—	mA
TIP-RING Operating Voltage	Figure 3; V_{DP} = 0.65 V, R_L = 400 Ω, I_{T-R} = 4.0 mA, Measure V_{T-R}	—	2.9	V
On-State Voltage	Figure 3; V_{DP} = 0.65, R_L = 200 Ω, I_{T-R} = 20 mA, Measure V_{T-R} minus V_{OUT}	—	1.3	V
Dial-Pulse Control Voltage (Note 1)	Figure 4, I_{DP} = 5.0 μA, R_L = 200Ω, V_{T-R} = 78.8 V, I_{T-R} < 1,0 mA, Measure V_{DP}	—	2.0	V
Dial-Pulse Input Current	Figure 4, V_{DP} = 2.0 V, R_L = 200 Ω V_{T-R} = 78.8 V, I_{T-R} < 1.0 mA, Measure I_{DP}	—	25.0	μA
Output Voltage	Figure 5, V_{T-R} = 140 V_{peak}, Measure V_{OUT}	—	29.0	V_{peak}
Turn-On Time	Figure 6, R_L = R1 = 200Ω, V_{TP} = 78.8 V, V_{DP} = 2.0 V initially. Turn-On Time is the time for the voltage across R1 (V_{R1}) to reach 57.5 after V_{DP} is switched to zero.	—	500	μs
Turn-Off Time	Figure 6, R_L = R1 = 200Ω, V_{TP} = 78.8 V, V_{DP} = zero initially. Turn-Off Time is the time for the voltage across R1 (V_{R1}) to decrease to 6.4 V after V_{DP} is switched to 2.0 V.	—	500	μs

Testing Circuits

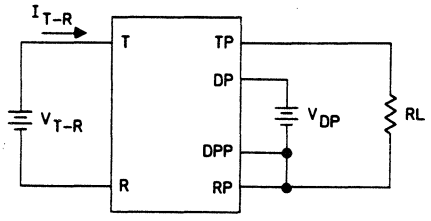


Figure 2. Test Circuit

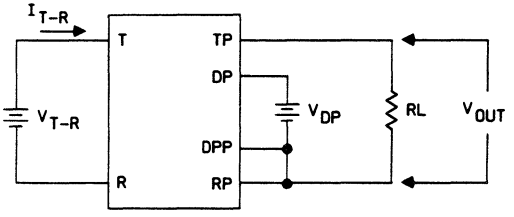


Figure 3. Test Circuit

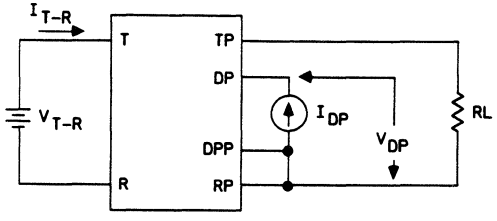


Figure 4. Test Circuit

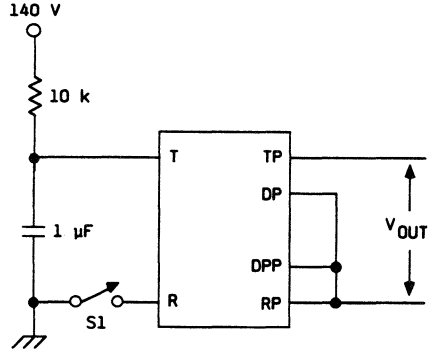
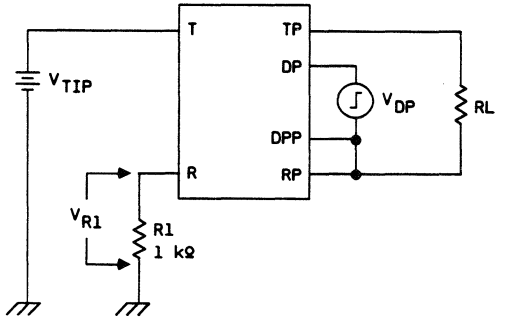
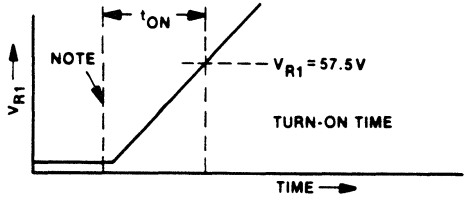
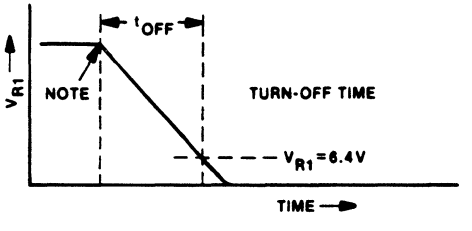


Figure 5. Test Circuit





NOTE: Time at which DP is shorted to DPP.



NOTE: Time at which VDP = 2.0 V

Figure 6. Switching Time Test Circuit

Applications

Figure 7 is a block diagram representing a telephone set application using the LH1028BB Telephone Interface Circuit (TIC). The incoming signal first passes through a switchhook before being connected to the TIC input terminals pin 2 (TIP) and pin 8 (RING). A metal-oxide varistor (MOV) or similar device shunts the input terminals of the TIC and limits the voltage across these terminals to less than 155 volts. This protection is needed to prevent the TIC input from exceeding its maximum voltage rating.

The output terminals of the TIC are TIP Prime (TP) and RING Prime (TP). TP is the positive output side of the polarity guard (full-wave rectifier). The RP terminal is connected to the negative side of the polarity guard by an internal dial pulse switch (M3, Figure 1) which is opened by applying a voltage between the control terminal Dial Pulse (DP) and Dial Pulse Prime (DPP).

The Set Electronics are attached to output pin 3 (TP) and pin 4 (RP). All of the audio functions, touch-tone dialing, dc characteristics control, logic and memory (if required) are contained in this external circuitry. If these circuits normally obtain their operating power from the telephone line through the TIC, they must have a temporary source of power to keep them working during the dial-pulse switch opening. This can usually be achieved using the charge provided by a storage capacitor. The operation of the LH1028BB TIC's primary functions, i.e., polarity guard, dial-pulse switching, and overload protection are described in more detail in an Application Note.

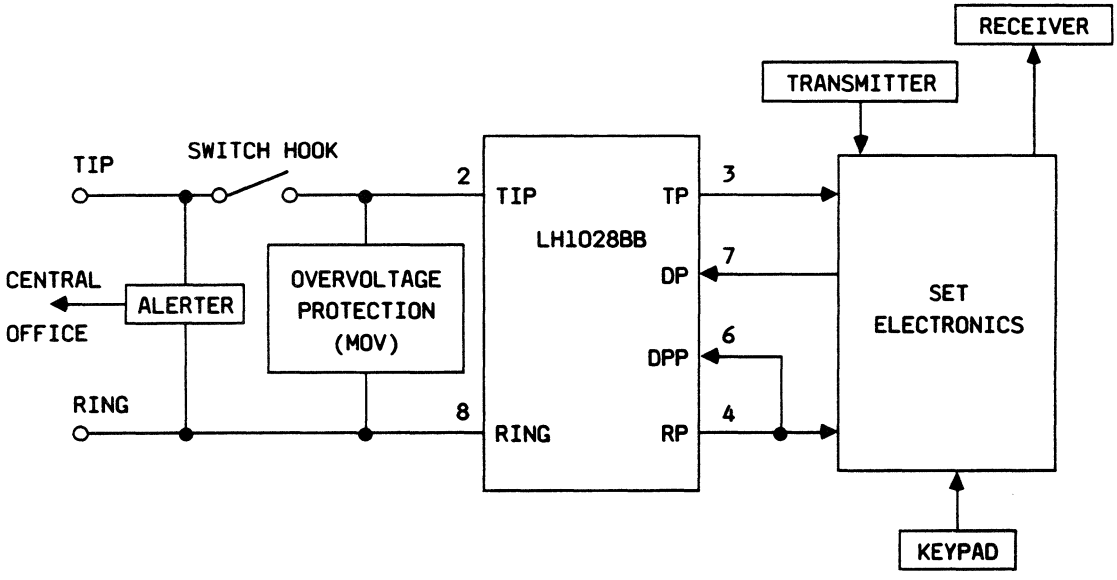


Figure 7. Typical Telephone Set Configuration

Characteristics

The dc characteristics of the LH1028BB TIC are shown in Figure 8. The RP, DP and DPP terminals are shorted and a 40 Ω load is between TP and RP. Also shown in Figure 10 is a load curve representing the central office battery and loop resistance. Note that the loop load intersects the TIC characteristics in a region where the drain current of M3 (Figure 3) is limited only by the 40 Ω load and not by the current limiting feedback current in the device. If the characteristic of the LH1028BB TIC current limiting circuit had a slope such that it intersected the loop load curve, it would be possible for the TIC to "latch up" in this higher voltage state and fail to operate properly. For this reason, the current limiting curve of the TIC has been designed to always be above, and almost parallel to, the worst case loop load curve.

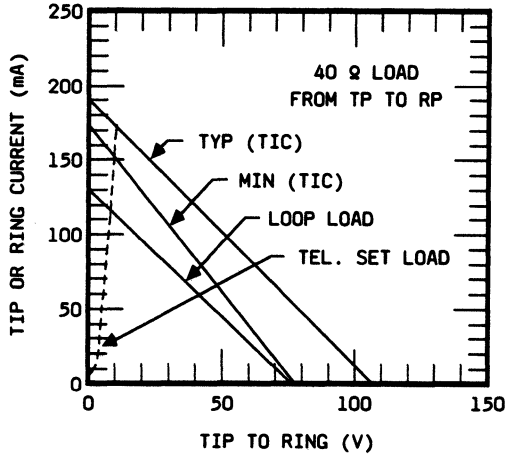
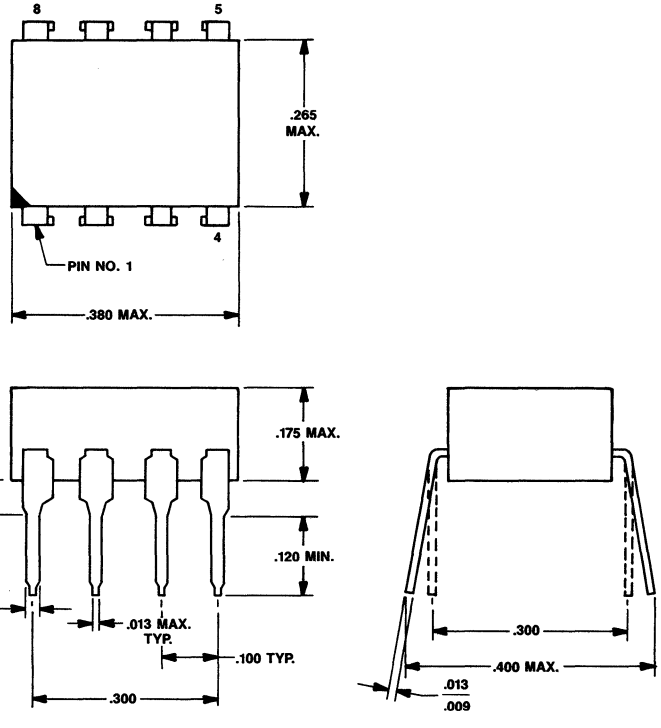


Figure 8. Current-Voltage Relationships

Outline Drawings (Dimensions in Inches)



Ordering Information

Device	Comcode
LH1028BB	104384474

LOOP TERMINATION SWITCH WITH SURGE PROTECTION LB1060AB

PRELIMINARY

Description

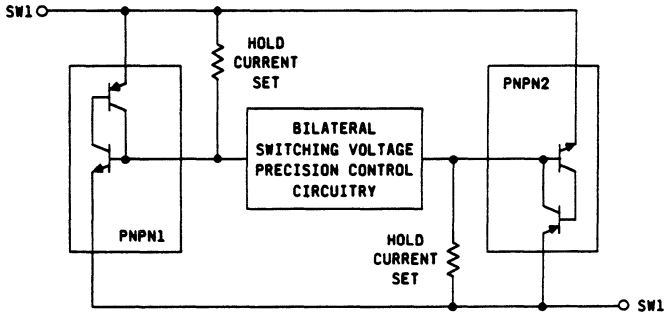
The LB1060AB Loop Termination Switch is an application specific integrated circuit for use in telecommunications loop test equipment. It consists of two (dual) isolated, polarity-insensitive (bilateral) voltage/current-controlled switches. Each independent switch has only two terminals. A switch will normally be open until the voltage across these two terminals rises to a nominal 17.3 volts, at which point it will close (customers desiring a different activating voltage should inquire about factory trimmed options). The switch will remain closed until the current flowing through the switch drops to a nominal 3.0 mA. Each switch has PNPN protector devices to guard against lightning surges.

Features

- Survives ±10-amp lighting surges
- The switch will survive or fail shorted when subjected to lightning surge currents between ±10 amps and ± 30 amps
- Temperature coefficient of switching voltage is typically ±0.5 mV/°C

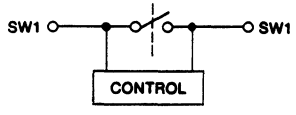
Functional Diagrams

The LB1060AB consists of two identical switches. Only one switch section is shown here.

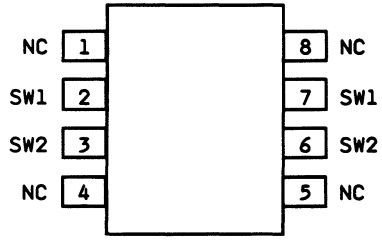


OPERATION	ACTION
$V_{SW1} > V_{BO}$	SW1 Closes
$V_{SW2} > V_{BO}$	SW2 Closes
$I_{SW1} < I_{HOLD}$	SW1 Opens
$I_{SW2} < I_{HOLD}$	SW2 Opens

NOTE:
Nominal V_{BO} = 17.3 V (±0.5 mV/°C)
Nominal I_{HOLD} = 3 mA



Pin Diagram



Maximum Ratings (At 25°C unless otherwise specified)	
Ambient Operating Temperature Range	−40 to +65°C
Storage Temperature Range	−40 to +125°C
Pin Soldering Temperature (t = 15 sec max.)	300°C
Operating Voltage, Positive or Negative (S1-to-S1, or S2-to-S2)	18.6 V
DC Operating Current, t ≤ 1 sec Each Switch	1.0 A
Power Dissipation (Package Limitation)	400 mW

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions

Pin	Symbol	Name/Function
1 4 5 8	NC	No connection. These pins are connected for internal circuitry. They should **not** be used as tie-points for any external circuitry.
2 7	SW1	Each pin represents one side of a switch (see Functional Diagrams) designated as Switch 1. Voltages or currents *may be applied between these pins without regard to polarity.*
3 6	SW2	Each pin represents one side of a switch designated as Switch 2. Voltages or currents *may be applied between these pins without regard to polarity.*

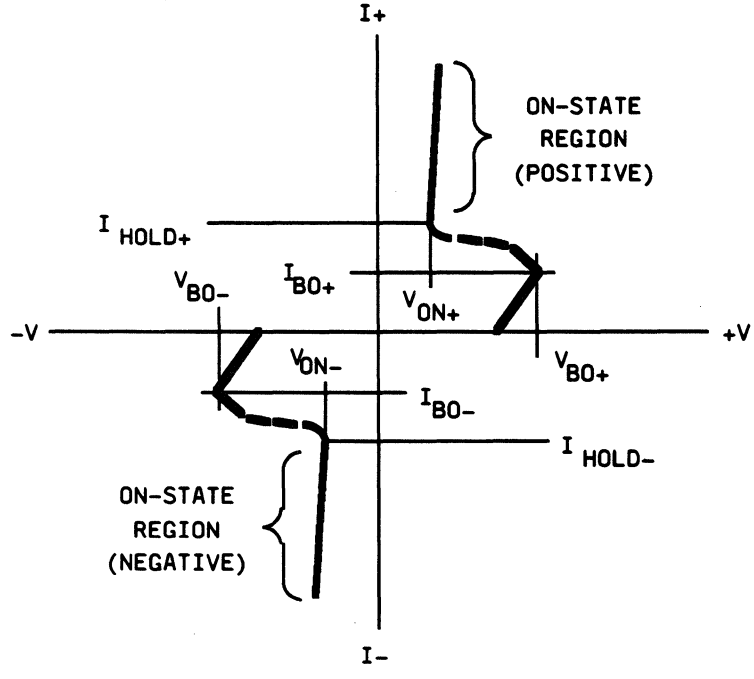


Figure 1. Symbology for Test Characteristics (Not to Scale)

Electrical Characteristics

(At 25°C unless otherwise specified)

These tests apply to both SW1 and SW2. Positive and negative descriptive terms (positive or negative signs for limit values) are for reference purposes only. These devices are bilateral in operation.

Characteristic	Test Condition	Min	Typ	Max	Unit
Breakover Voltage, Positive ($V_{BO}+$); Switch Closes	See Figure 2	16.55	17.3	18.05	V
Breakover Voltage, Negative ($V_{BO}-$); Switch Closes	See Figure 2	−16.55	−17.3	−18.05	V
Breakover Current, Positive ($I_{BO}+$)	See Figure 2	30	60	125	μA
Breakover Current, Negative ($I_{BO}-$)	See Figure 2	−30	−60	−125	μA
Leakage Current, Positive	See Figure 3	—	—	5.0	μA
Leakage Current, Negative	See Figure 3	—	—	−5.0	μA
Hold Current, Positive ($I_{HOLD}+$), Switch Opens	See Figure 2	1.3	3.0	7.4	mA
Hold Current, Negative, ($I_{HOLD}-$), Switch Opens	See Figure 2	−1.3	−3.0	−7.4	mA
On Voltage, Positive ($V_{ON}+$)	See Figure 4; I = 20 mA	—	—	950	mV
On Voltage, Negative ($V_{ON}-$)	See Figure 4; I = −20 mA	—	—	−950	mV
Forward Voltage, Positive	See Figure 4; I = 1 A, t ≥ ms	—	—	2.0	V
Forward Voltage, Negative	See Figure 4; I = −1 A, t ≤ ms	—	—	−2.0	V

Test Circuits

(Tests shown are defined as positive tests for Switch 1, pins 2 and 7; reverse the connections to pins 2 and 7 for negative tests; use pins 3 and 6 for Switch 2 tests.)

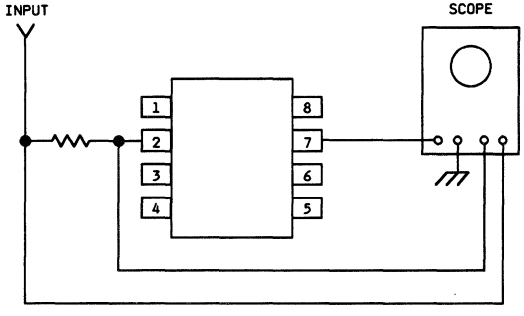


Figure 2. Hold Current and Breakover Voltage Tests

Breakover Voltage (V_{BO})

A ramped bias current of 1% duty cycle is applied to the input. Breakover voltage is **measured** as the peak magnitude of voltage which occurs as the bias current is increased in magnitude (from 0 to 150 μA, in 1 μA steps). This forces the device into the low impedance "on-state" region of its characteristic (see Figure 1).

Breakover Current (I_{BO})

Breakover current is that value of current which must be applied for the breakover voltage peak to occur.

Hold Current (I_{HOLD})

A ramped bias current of 1% duty cycle is applied to the input. Hold current is measured as the minimum current for which the device will stay in the on-state region or the "switch-closed condition" (see Figure 1), as the bias current is decreased from 10 mA to 1 mA.

Test Circuits
(Continued)

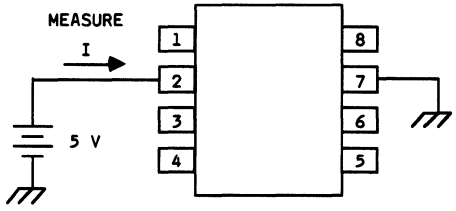


Figure 3. Leakage Tests

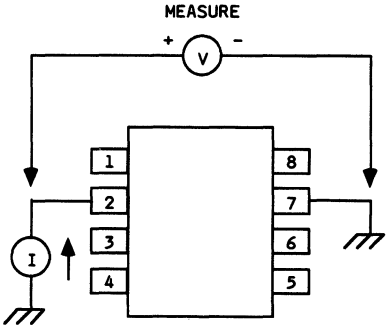


Figure 4. On/Forward Voltage Tests

Electrical Characteristics

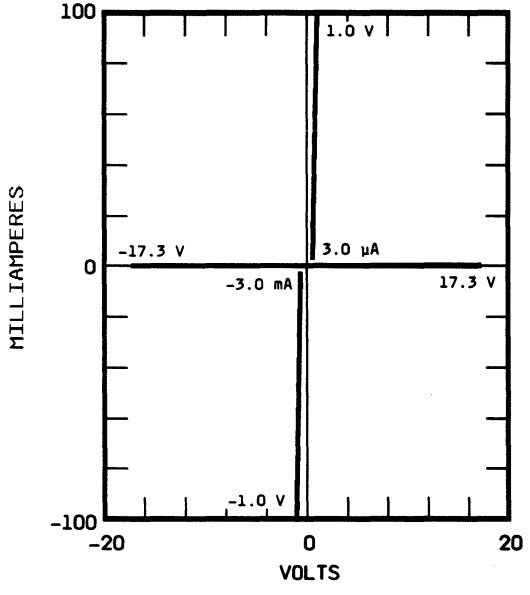


Figure 5. High Current Characteristics

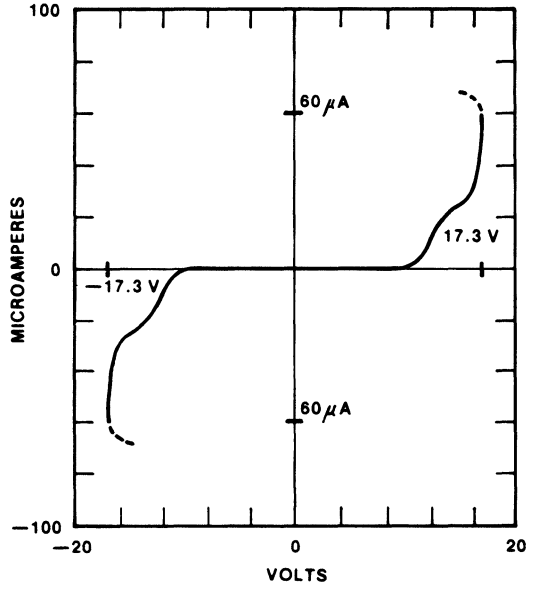


Figure 6. Low Current Characteristics

Applications

The following diagram illustrates the use of an LB1060AB device in telephone loop testing applications. The LB1060AB, when designed into a maintenance termination unit (MTU), is located on the customer premises at the demarcation point between the network and the customer's equipment wiring. An MTU is used in conjunction with a test system located in the Central Office. The purpose is to identify the location of resistive or open circuit faults, either on the customer premise or in the network. The responsibility for the repair can then be determined. The circuit test is performed by the Central Office, which controls the switching action of the LB1060AB by applying the appropriate voltages to the loop.

This device could also be used in an application as a surge protector where the LB1060AB is placed in parallel with a circuit being protected. For this application, LB1060AB devices could be connected in series to boost the maximum voltage across the circuit being protected.

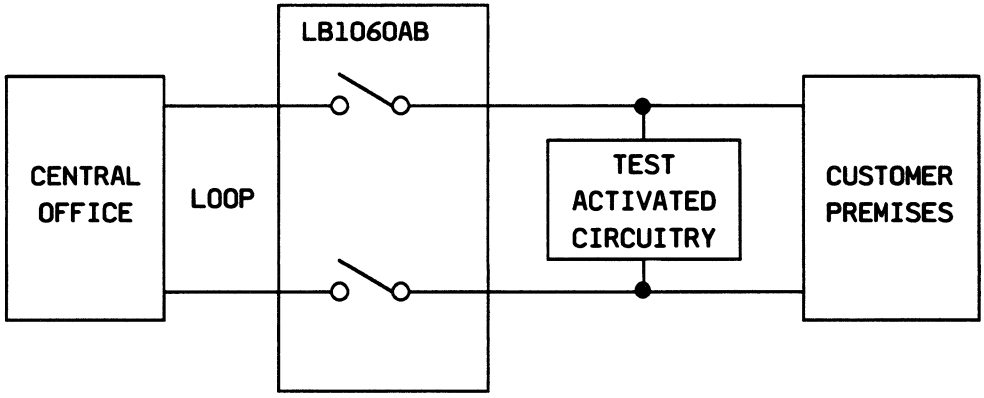


Figure 7. Block Diagram of LB1060AB Device

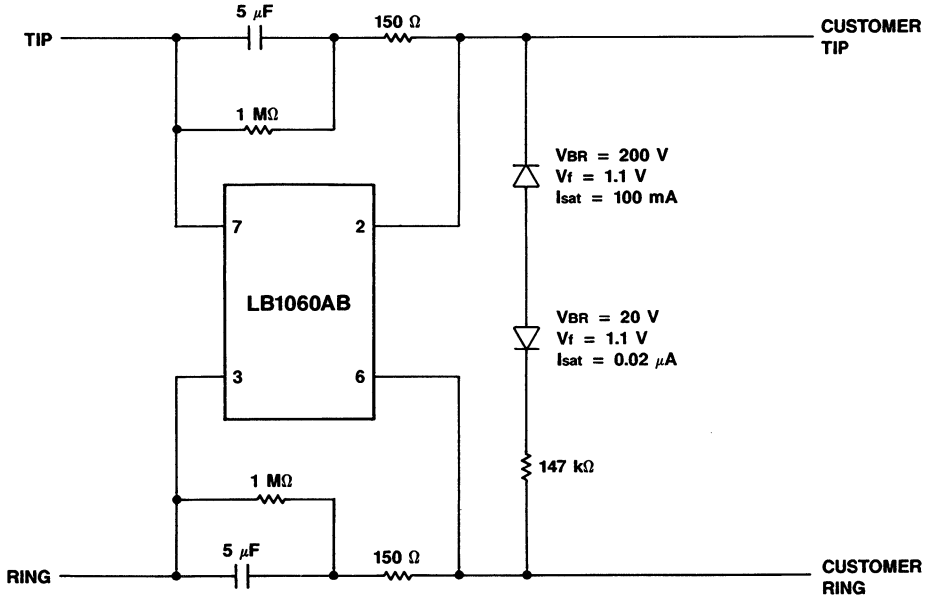
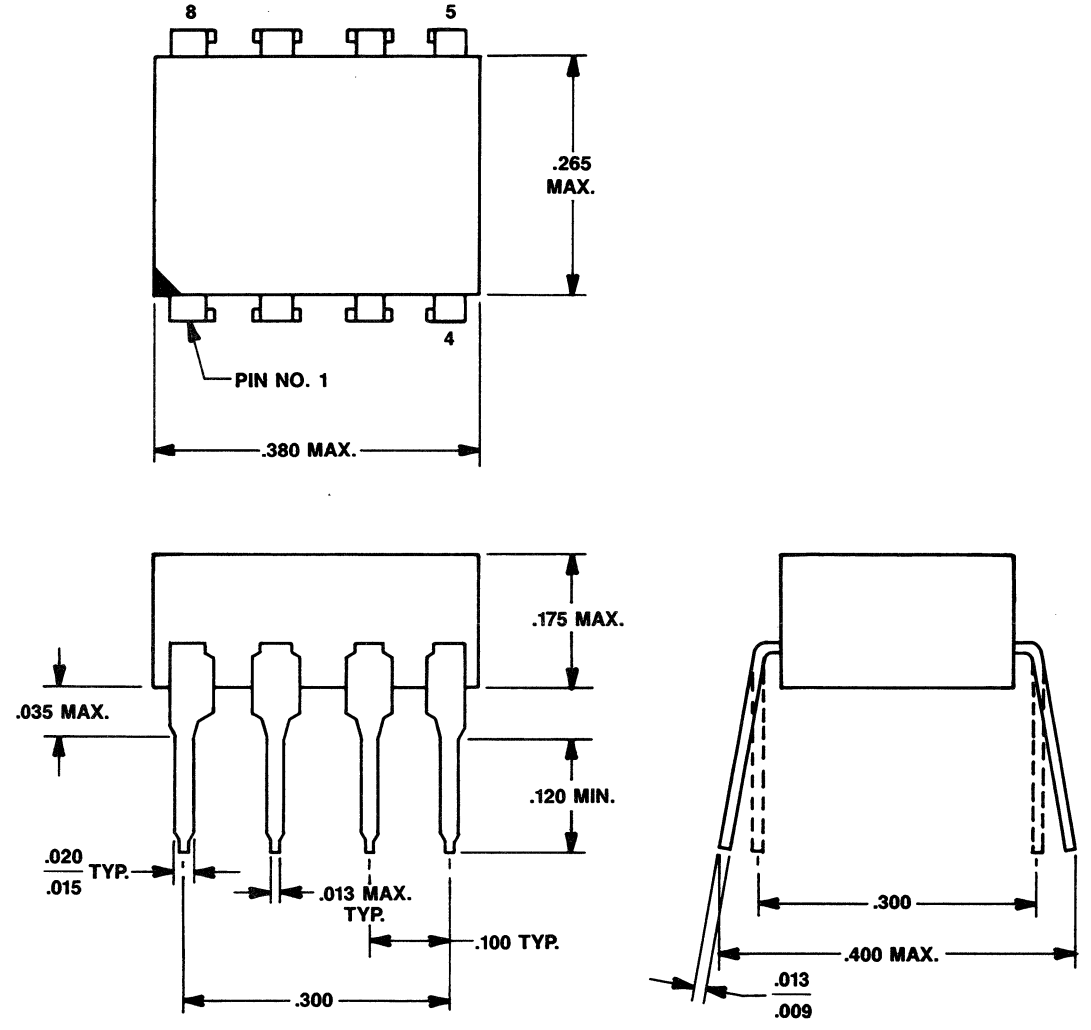


Figure 8. Typical Application Diagram for LB1060AB in Maintenance Termination Unit (MTU)

Outline Drawing

(Dimensions in Inches)



Ordering Information

Device	Comcode
LB1060AB	104382064

PRELIMINARY

Description

The LB1068AC/AW is intended for use as a conditioner of voice signals in telephone handset and speech applications. This device provides the following five functions:

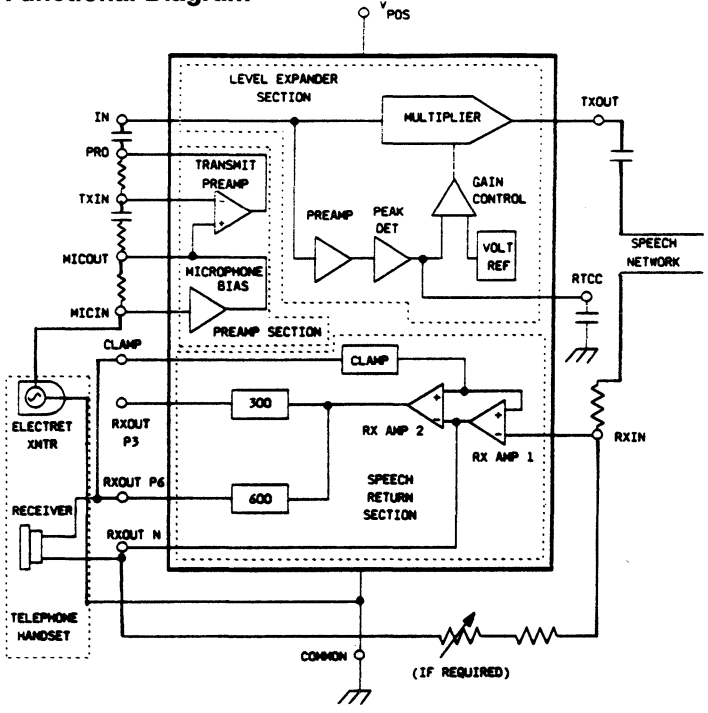
1. High PSRR electret microphone biasing—low noise output in the presence of power-supply modulation.
2. Microphone preamplification with adjustable gain—provides flexibility for different microphones and acoustic applications.
3. Gain expansion of the microphone signal—reduces the effects of background noise during periods when the talker is silent.
4. Adjustable gain receiver amplification with a choice of 300 Ω or 600 Ω output impedance; active receiver duty for noisy environments or hearing-impaired applications.
5. Receiver clamping—limits high transient signals from overdriving the receiver.

The Universal Voice-Signal Conditioner is available in a 16-pin plastic DIP (LB1068AC) and as a 16-lead surface mount (LB1068AW).

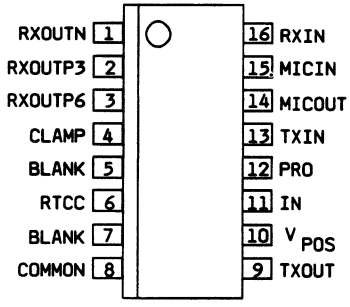
Features

- Supply-voltage range from 2.6 to 10 V (suitable for line-powered applications)
- High PSRR electret microphone biasing (typically > 50 dB)
- User selectable microphone and receiver gain
- Usable with other types of microphones (ceramic, dynamic, etc.)
- Internally supplied signal ground
- Built-in receiver equalizing resistors for 300-ohm or 600-ohm applications
- Both 16-pin DIP and 16-lead surface mount available

Functional Diagram



Pin Diagram



Maximum Ratings (At 25°C unless otherwise specified)	
Ambient Operating Temperature Range	−20 to +55°C
Storage Temperature Range	−40 to +125°C
Pin Soldering Temperature (t = 15 s max.)	300°C
Supply Voltage Surge (V_{POS} to COMMON)	25V

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Recommended Operating Voltage Range (T_A = −20°C to +55°C)	
Minimum Supply Voltage (V_{POS})	2.6 Volts
Maximum Supply Voltage (V_{POS})	10 Volts

Pin Description

(See Functional Diagram)

Pin	Symbol	Name/Function
1 2 3	RXOUTN RXOUTP3 RXOUTP6	Amplifier outputs for connection to a handset speech receiver. RXOUTN is a common output terminal and is used in conjunction with either RXOUTP3 for 300 Ω receivers, or RXOUTP6 for 600 Ω receivers.
4	CLAMP	The CLAMP terminal is used as a click reducer in telephone applications. It should be connected to either RXOUTP3 or RXOUTP6, whichever terminal is being used.
5 7	BLANK BLANK	These pins may be used as tie-points for external components. Maximum voltage should not exceed 15 volts.
6	RTCC	Response Time Control Capacitor (RTCC). A 1 μF capacitor on this pin is necessary to set the **attack** and **release** times of the expander's AGC circuit. The nominal attack and release times with a 1 μF capacitor are 14 milliseconds and 140 milliseconds respectively. The expansion function may be defeated by connecting a 10 kΩ resistor from this lead to V_{POS} (in addition to the RTCC capacitor connection to ground).
8	COMMON	Circuit common (not necessarily system or physical ground).
9	TXOUT	Output of the Expander function of the device. The "Expander" conditioned signal is transmitted to a speech network.
10	V_{POS}	External supply-voltage connection (2.6 to 10 volts operating range).
11	IN	Input to the Expander function of the device.
12 13 14 15	PRO TXIN MICOUT MICIN	Preamp Output, Transmit Input, Microphone Output and Microphone Input respectively. There is a wide choice of electret microphones available to designers of voice signal systems. These terminals are made available externally so that discrete components may be added to properly condition the electret output signal. (See the APPLICATIONS section for a more complete discussion.)
16	RXIN	Input for receiver amplifier. This lead should be connected to the speech network.

Electrical Characteristics

(At 25°C unless otherwise specified)

Characteristic	Test Condition	Min	Typ	Max	Unit
General Characteristics					
Supply Current, Surge	Figure 1; Measure I V_{POS} = 25 V; t = ms V_{IN} = 0	—	—	10.0	mA
Quiescent Supply Current	Figure 1; Measure I				
	V_{POS} = 10 V, V_{IN} = 0	—	—	2.0	mA
	V_{POS} = 2.28 V, V_{IN} = 0	—	—	1.7	mA
Supply Current @ Maximum Output (Receiver Amp.)	Figure 1; Measure I V_{POS} = 3.35V, V_{IN} = 225 mVrms	—	—	4.0	mA
Gain Expander					
Speech Response Time:	See Note 1				
Attack Time	V_{POS} = 3.5 V	—	14	—	ms
Release Time	V_{POS} = 3.5 V	—	140	—	ms
(See EXPANDER OPERATION discussion for further information)					
Expander, Input Gain Ratio; $\frac{V_{OUT}}{V_{IN}}$	Figure 4; V_{POS} = 3.5V, Measure V_{OUT};				
Maximum	V_{IN} = 353 mVrms	0.94	—	1.15	—
High	V_{IN} = 50 mVrms	0.94	—	1.10	—
Mid	V_{IN} = 12.5 mVrms	0.38	—	0.60	—
Low	V_{IN} = 10. mVrms	0.19	—	0.28	—
Electret Microphone Bias and Transmit Preamp					
Microphone Bias Current	Figure 3; V_{POS} = 3.5 V Measure I	420	—	560	μA
Microphone Bias Output Voltage Swing	Figure 4; V_{POS} = 3.5V, Measure V_{OUT} V_{IN} = 50 mVrms	—	—	50	mVrms
Pre-Amp Output Voltage Swing	Figure 5; V_{POS} = 3.5V Measure V_{OUT} V_{IN} = 50 mVrms	—	—	353	mVrms
Pre-Amp Closed Loop Gain; 20 log $\frac{V_{OUT}}{V_{IN}}$	Figure 5; V_{POS} = 3.5V Measure V_{OUT} V_{IN} = 12.5 mVrms	—	—	29	dB

Note 1: Speech Response Time is shown here as an electrical characteristic and is expressed in circuit functional terms. It is assured as a result of production testing.

Electrical Characteristics (Continued)

(At 25°C unless otherwise specified)

Characteristic	Test Condition	Min	Typ	Max	Unit
Speech Return Section					
Receive Amp Output Voltage Swing	Figure 6; V_{POS} = 3.5 V V_{IN} = 225 mVrms Rf = 600 Ω; Measure V_{OUT}	—	—	225	mVrms
Receive Amp Closed Loop Gain 20 Log $\frac{V_{OUT}}{V_{IN}}$	Figure 6; V_{POS} = 3.5 V V_{IN} = 1.0 mVrms Rf = 18.9 K; Measure V_{OUT}	—	—	30	dB
Clamp Voltage Positive Negative	Figure 7; V_{POS} = 3.5 V IS = +2.0 mA IS = −2.0 mA Measure V_{CLAMP}	 0.6 −0.6	 — —	 0.9 −0.9	 V V

Test Circuits

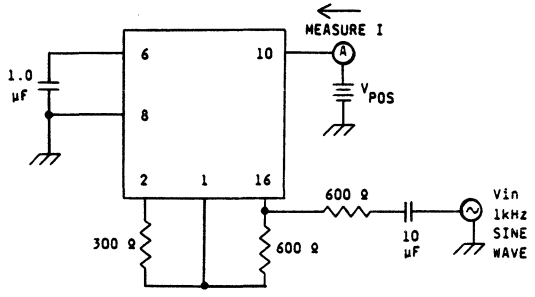


Figure 1. Supply Currents

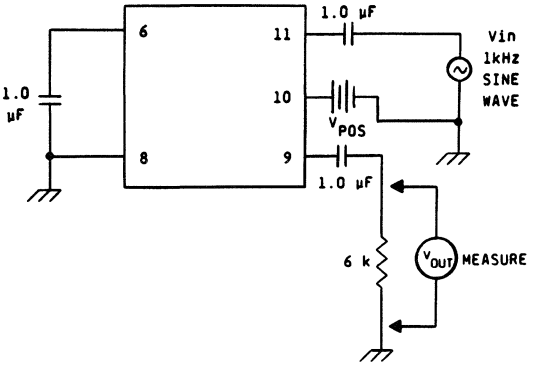


Figure 2. Expander, Input Gain Ratio

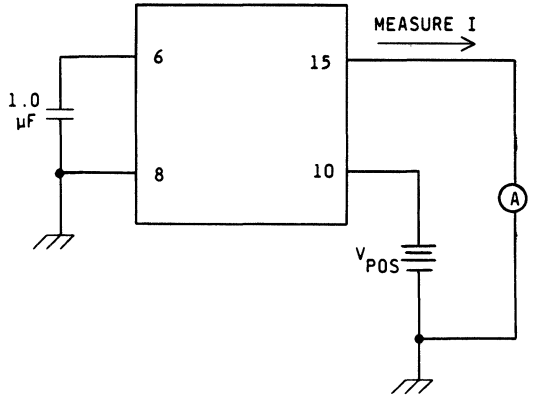


Figure 3. Microphone Bias Current

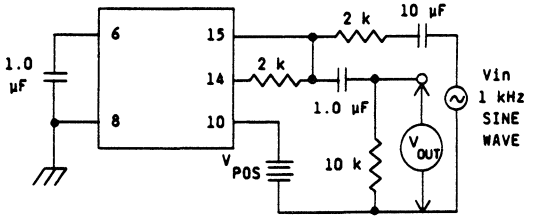


Figure 4. Microphone Bias Output Voltage Swing

Test Circuits (Continued)

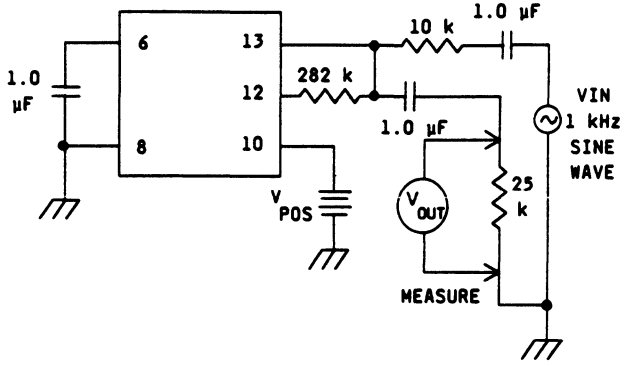


Figure 5. Pre-Amp Output and Gain

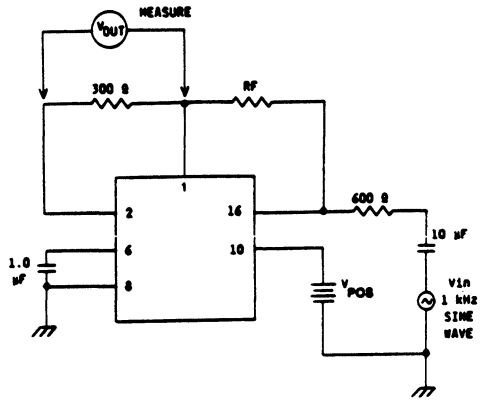


Figure 6. Receive Amplifier, Output and Gain

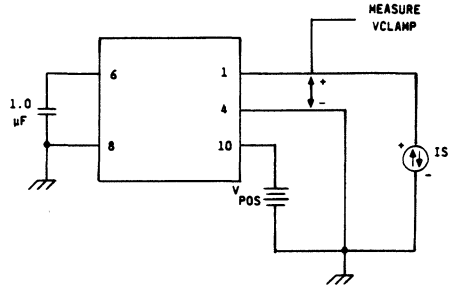


Figure 7. Clamp Voltage

Expander Input and Output Diagrams (See Functional Diagram)

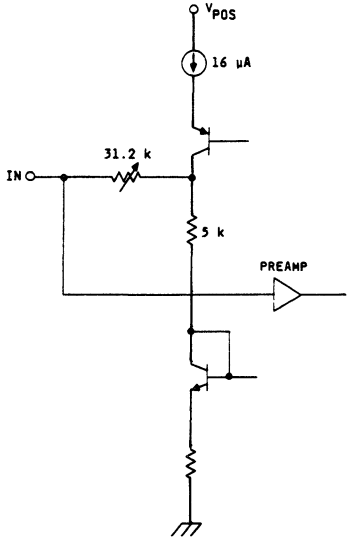


Figure 8. Expander Input

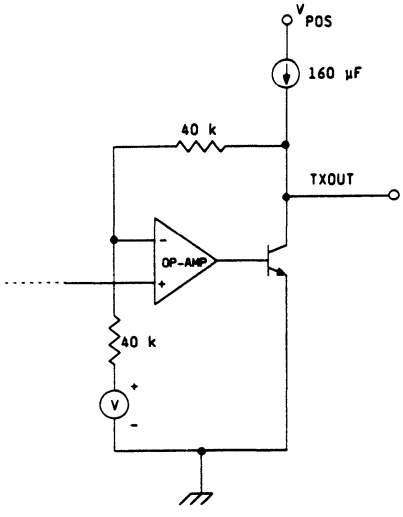


Figure 9. Expander Output

Expander Operation

Figure 10 summarizes the basic characteristics of a voice frequency level expander. This level expander circuit is used to suppress low-level background noise in handsets equipped with electret microphones. In a noisy environment, the users may hear an objectionable high reproduction of background noise in their receiver via the normal sidetone path (sidetone is that portion of the speaker's voice which is purposely fed back to the receiver to prevent the phone from sounding "dead". It also aids the speakers to adjust their voice to a desirable level).

High levels of background noise pickup are due to two factors:

1. More recent handset designs (as compared to earlier designs) have less microphone directivity and more gain, allowing the mouth-to-microphone distance to be greater.

2. Electret microphones do not have the built-in, non-linear sensitivity inherent in carbon microphones.

The level expander cures these background noise problems by introducing attenuation into the voice path for signals below approximately 353 mVrms, and removing this attenuation when the user is speaking. The level expander's response to the beginning of a sentence (attack time) is rapid, while the decay time back to the "idle state" (release time) is slow so that it may allow for short breaks between syllables or words. Thus the sharpness or clarity of the electret is preserved by restricting any distortion to a short-time interval.

Attack time is technically defined as the time required for the output voltage to increase to within 90% of the value shown in Figure 10, after the input voltage is instantaneously changed from 3.16 mVrms to 31.6 mVrms. Decay time is technically defined as the time required for the output voltage to decrease to within 90% of the value shown in Figure 10, after the input voltage is instaneously changed from 31.6 mVrms to 3.16 mVrms. For this specific response, a 1.0 μF capacitor must be connected from Pin 6 to COMMON, in addition to the normal input, output and supply connection. These response times are not directly measured, but are guaranteed by design and charge/discharge current tests.

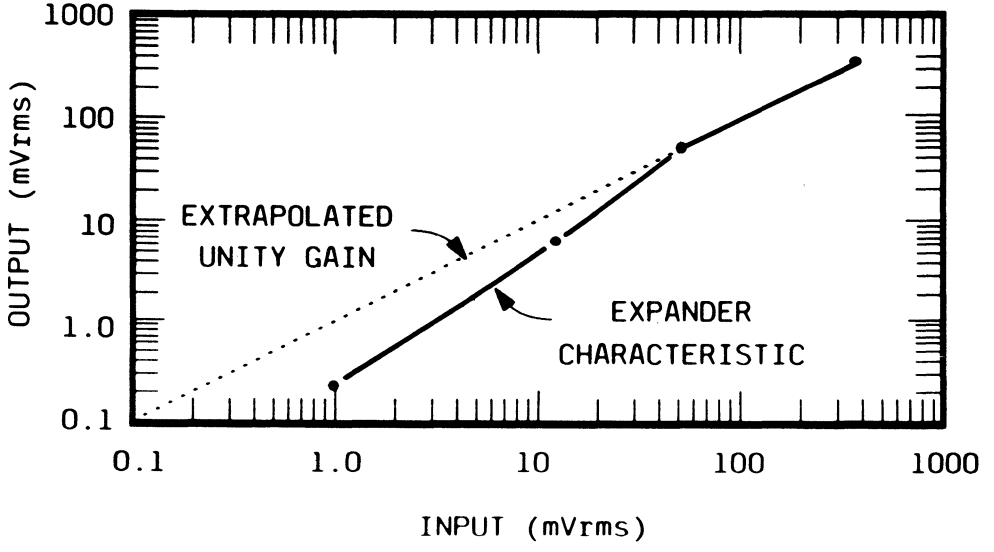


Figure 10. Typical Expander Characteristics

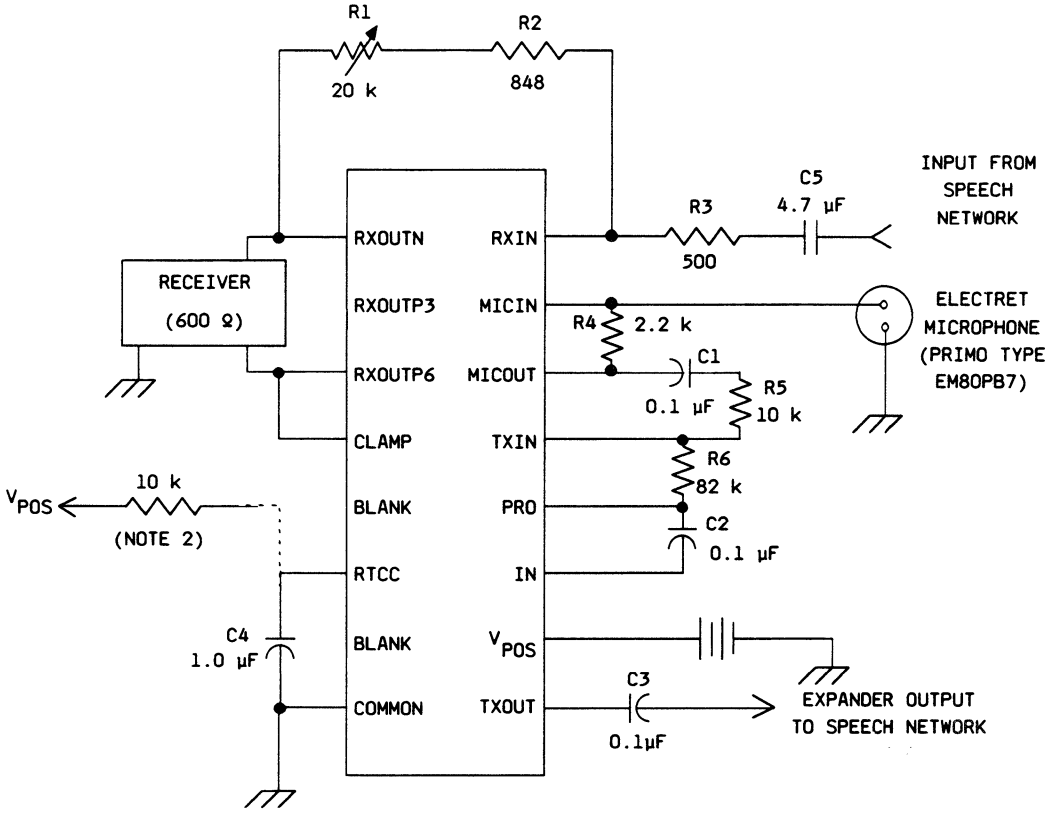
Applications

Figure 11 is an application diagram showing the LB1068AC/AW connected as a voice-signal conditioner for a telephone handset application (also see Functional Diagram). The telephone handset contains a Primo electret microphone (as the speech transmitter) and a 600 Ω receiver. The expander function of the LB1068AC/AW can be disabled if it is not desired (see Note 2).

External resistors R1, R2 and R3 form a receiver gain network. Resistor R1 acts as a volume control to adjust the gain of incoming signals from the speech network. This is useful for those applications where hearing-impaired aids must be considered.

Several types of commercial electret microphones are available. External resistor R4 is used to match the impedance of a particular electret microphone to the LB1068AC/AW.

External resistors R5 and R6 form a transmit gain network. They adjust the gain of the signal which is output from the electret microphone.



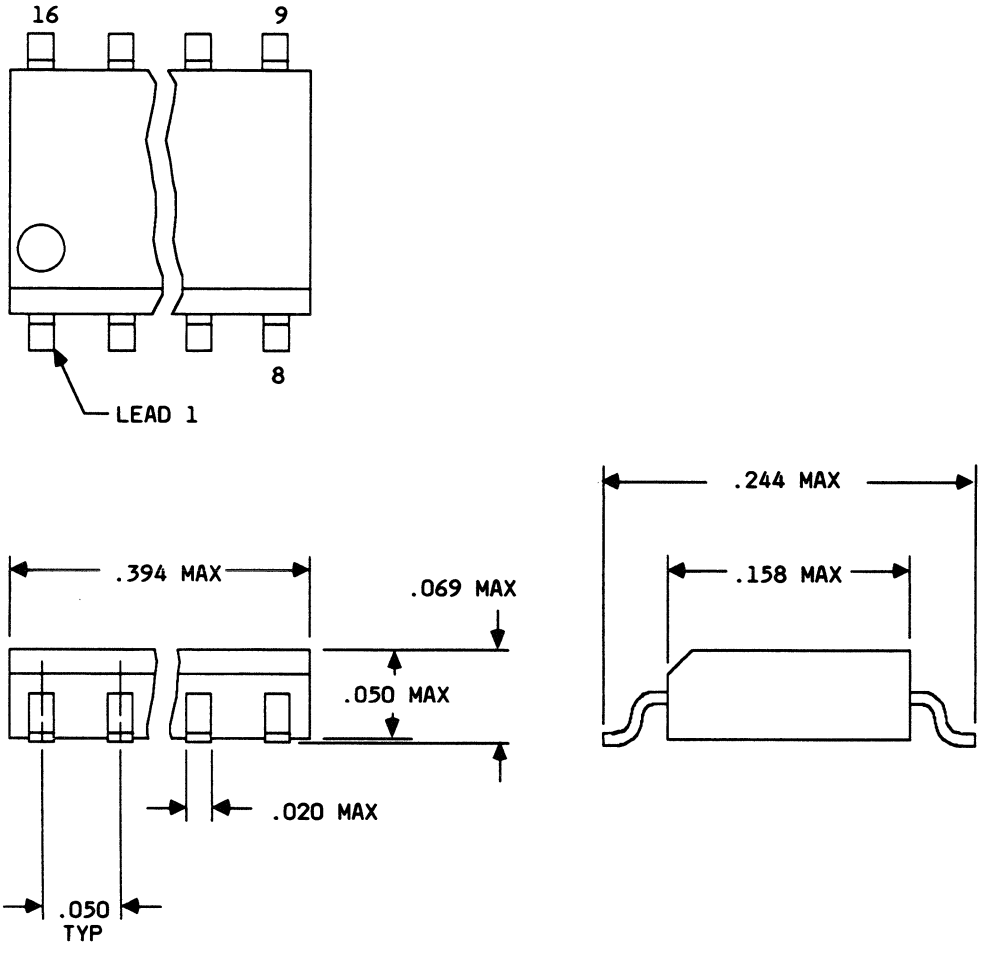
Note 2: The RTCC pin may be connected to V_{POS} through a 10 kΩ resistor to eliminate the expander function.

Figure 11. LB1068 Application Diagram

Outline Drawing

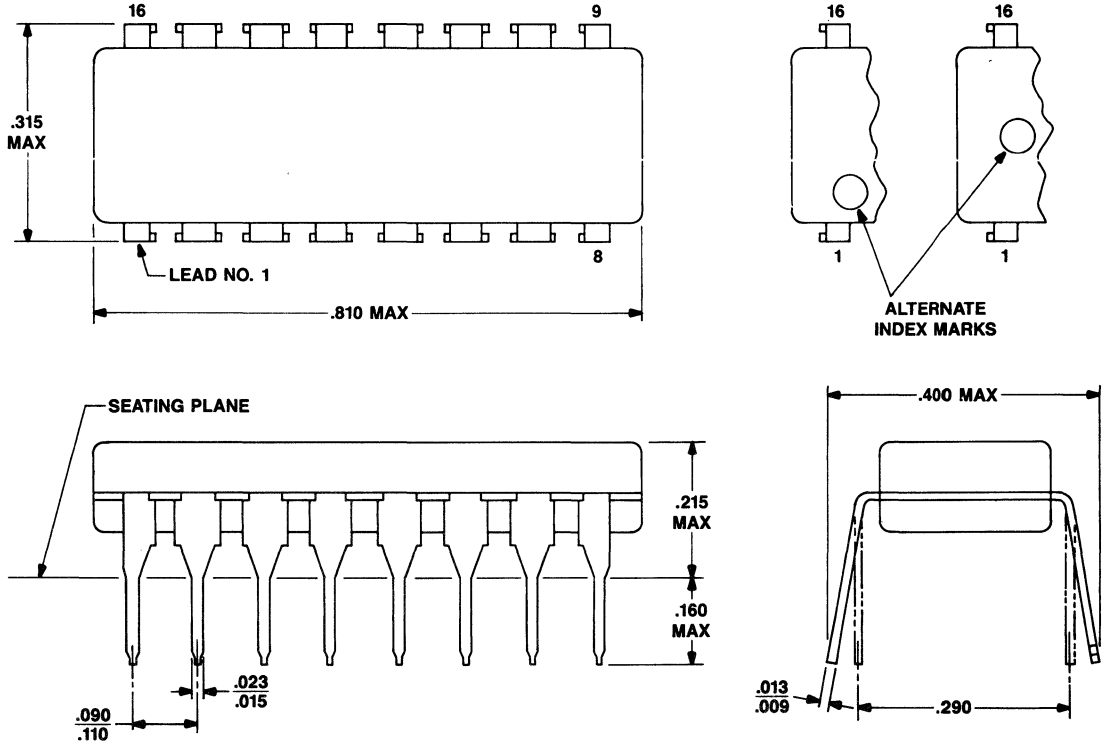
(Dimensions in Inches)

16-Pin SOIC



Outline Drawing

(Dimensions in Inches)
(Continued)



Ordering Information

Device	Comcode
LB1068AW	104386552
LB1068AC	104430848

QUAD TONE DETECTOR

LS1130AC

PRELIMINARY

Description

The LS1130AC is a quad tone detector used in the receiver of the Key Telephone Systems. The circuit compares the peak amplitude of the signaling frequencies to a fixed reference. When a peak input is above the reference the corresponding output goes low to control the associated TTL logic. Each of the four outputs drive a different number of gates dictated by the different load resistors.

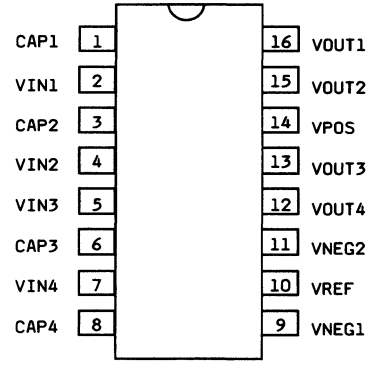
Features

- TTL-compatible

Maximum Ratings (At T_A = 25°C unless otherwise specified)	
Supply Voltage 1	−6.5 V
Supply Voltage 2	−13 V
Power Dissipation	200 mW
Storage Temperature Range	−40 to +125°C
Operating Temperature Range	0 to 60°C
Pin Soldering Temperature (t = 15 s)	300°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Diagram



Pin Description

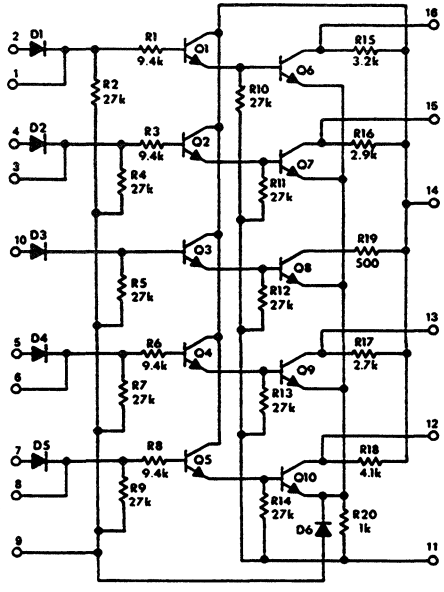
Pin	Name/Function	Pin	Name/Function
1	Capacitor 1	9	V_{NEG1}
2	Input Voltage 1	10	Reference Voltage
3	Capacitor 2	11	V_{NEG2}
4	Input Voltage 2	12	Output Voltage 4
5	Input Voltage 3	13	Output Voltage 3
6	Capacitor 3	14	V_{POS}
7	Input Voltage 4	15	Output Voltage 2
8	Capacitor 4	16	Output Voltage 1

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for informational purposes only and are not part of the testing requirements.

Characteristic	Test Condition	Min	Max	Unit
Power-Supply Current	Figure 2	4.2	6.6	mA
	Figure 3	−4.2	−6.6	
Input Current	Figure 4	—	125	μA
Output Voltage	Figure 5	—	−3.2	V
		−4.5	—	



Note: All resistance values are in ohms.

Figure 1. Basic Schematic

Test Circuits

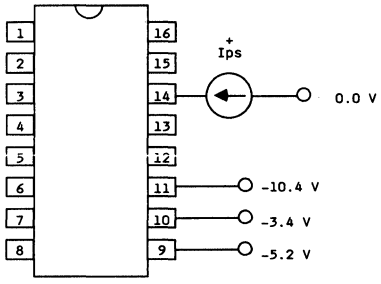


Figure 2. Power-Supply Current (+ IPS) Test Circuit

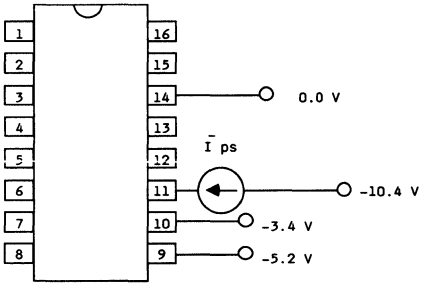
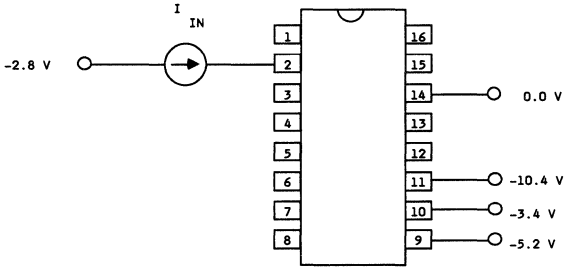
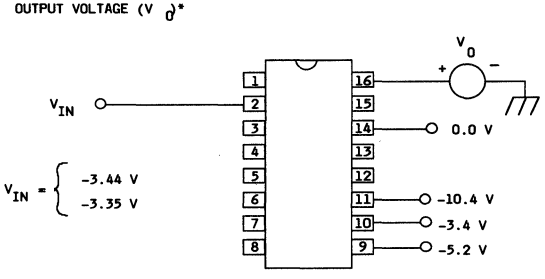


Figure 3. Power-Supply Current (− IPS) Test Circuit



*-REPEAT FOR INPUTS 2-4(LEADS 4,5,&7)

Figure 4. Input Current (IIN) Test Circuit

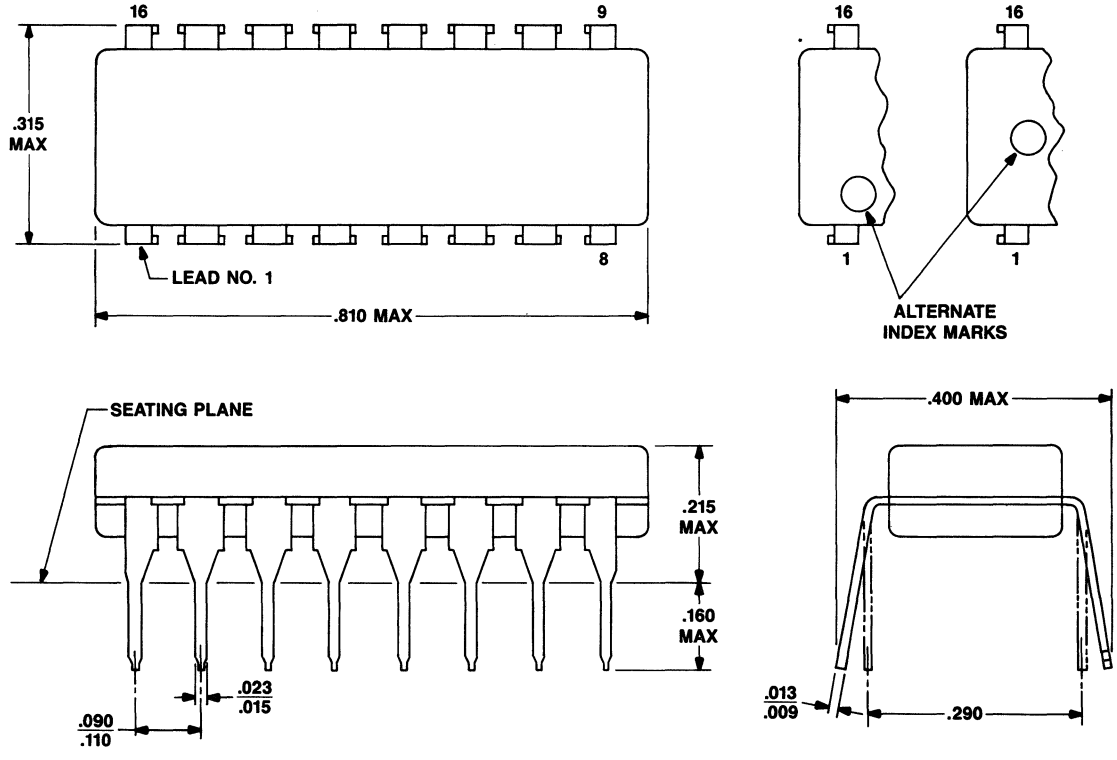


*REPEAT FOR INPUTS/OUTPUTS 2-4, CONNECT
A 0.1μfd CAPACITOR FROM EACH OF THE LEADS 1,3,6,8,
AND 10 TO GROUND

Figure 5. Output Voltage (VO) Test Circuit

Outline Drawing

(Dimensions in Inches)



Ordering Information

Device	Comcode
LS1130AC	104413158

VOICE PATH SWITCH
POWER CONDITIONER/AMPLIFIER

LB1020AF
LB1021AD

Description

The LB1020AF performs the switching function needed for Speakerphone operation by accepting transmit and receive signals as input, and providing transmit and receive variolosser control signals as output. Timing of these switching functions is selectable using external RC combinations. The LB1020AF also provides a noise guard feature which permits steady background noise to be ignored in making the transmit/receive switching decision. It is normally used in conjunction with the LB1021AD to which it provides variolosser control currents.

The LB1021AD provides the linear amplification for a full-feature Speakerphone system, including switchable, controllable gain for the transmit and receive voice paths, speaker and line drive capabilities, and switchguard/talkdown gain. It provides a stable, low-noise signal reference from a single 12-volt supply needed to power the circuit. It is normally used in conjunction with the LB1020AF.

Features

- 70 mA speaker driver capability
- High-gain receive preamplifier accommodates variety of microphones
- 40 dB typical receive path gain
- Quiet, on/off volume control
- Receive in default
- Switching unaffected by constant background noise
- Slow attack/quick decay noise guard does not interfere with forced switching
- All switching time constants independently controllable
- Holdover timing independent of forced switching time constants

Note: Request the "FULL-FEATURE SPEAKERPHONE" Application Note by H.J. Lory, Bell Laboratories for a complete discussion of Speakerphone operation.

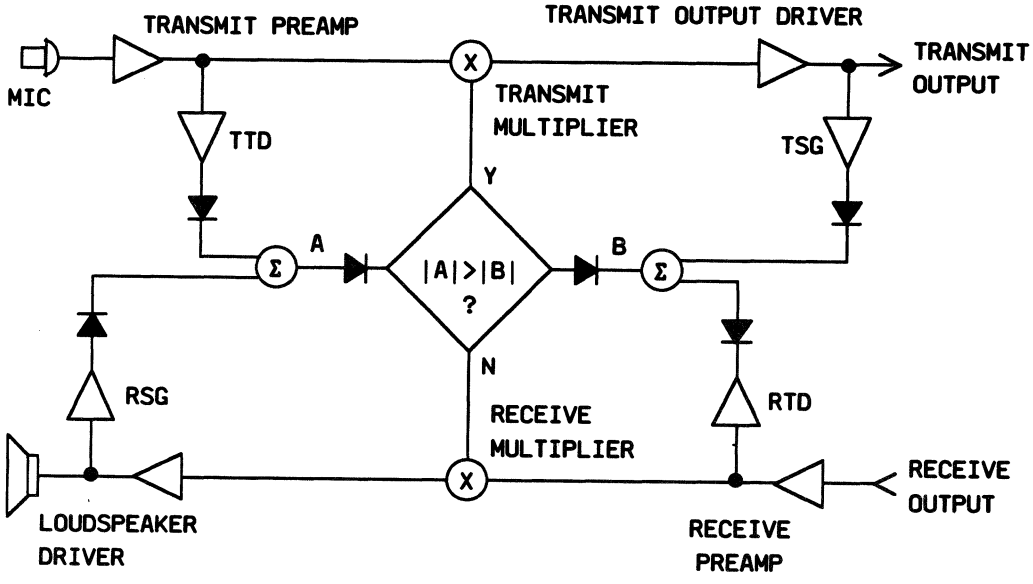


Figure 1. Simplified Speakerphone Circuit

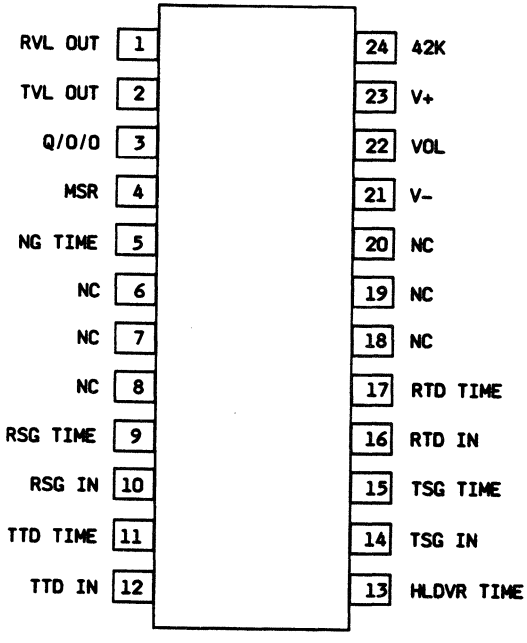


Figure 2. LB1020AF 24-Pin Plastic DIP

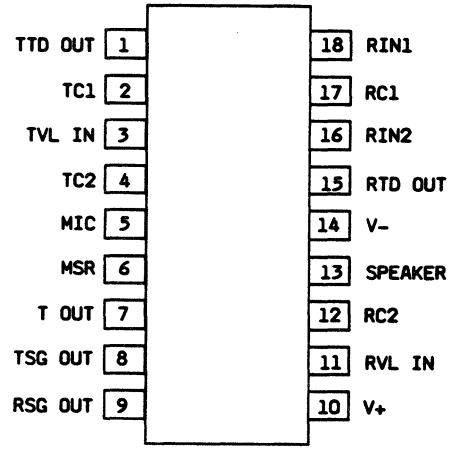


Figure 3. LB1021AD 18-Pin Plastic DIP

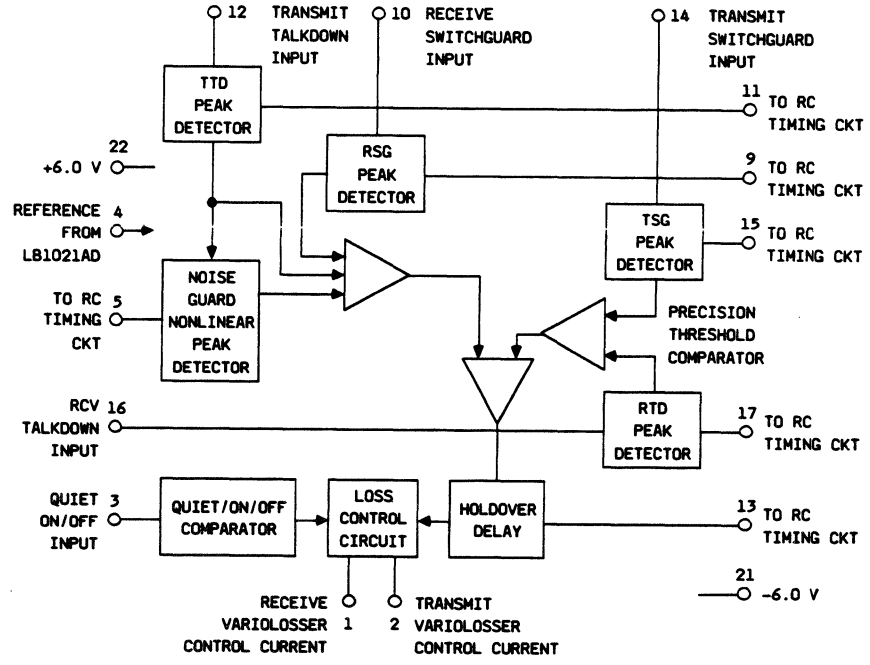


Figure 4. LB1020AF Voice Path Switch Block Diagram

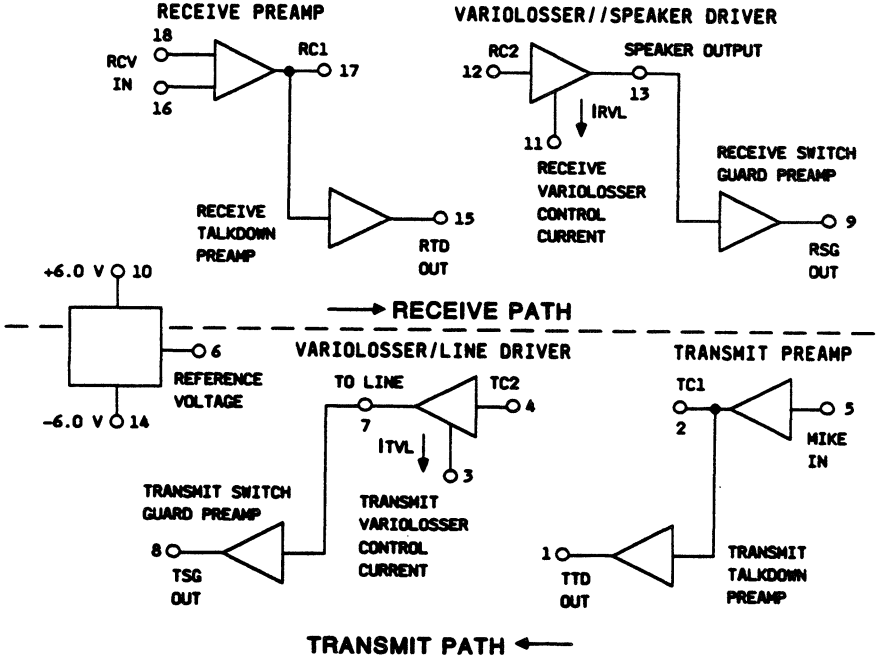


Figure 5. LB1021AD Power Conditioner—Amplifier Block Diagram

Maximum Ratings
(At 25°C unless otherwise specified)

Ambient Operating Temperature Range	0 to 70°C
Storage Temperature Range	−40 to +125°C
Pin Soldering Temperature (t = 15 s max.)	300°C
Voltage (V+)	+15 V
Voltage (V−)	−15 V

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of the Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

V+ Voltage	+6 V
V− Voltage	−6 V

Electrical Characteristics

(T_A = 25°C)

LB1020AF Test Specifications

Test #	Test Name	Fig. #	Test Conditions Unless otherwise stated, V+ = +6V, V− = −6V	Symbol	Specification Min	Specification Max	Unit
1	Power-Supply Currents	6	Measure current in positive and negative supply leads	I(PS)	3.0	9.0	mA
2	Holdover Voltage, Idle	6	—	V(13,4)	2.6	3.4	V
3	Holdover Voltage, High	7	V(TTD) = +2V	V(13,4)	4.3	—	V
4	Holdover Voltage, Low	8	V(RTD) = −2 V	V(13,4)	0	1.6	V
5	Receive Variolosser Current Out, RCV Max Volume	9	V(VOL) = V(RTD) = −1.0 V, V(QT) = 0	I(RVL)	−6.5	+6.5	μA
6	Receive Variolosser Current Out, RCV Min Volume	9	V(VOL) = −4 V, V(RTD) = −1.0 V, V(QT) = 0	I(RVL)	93	107	μA
7	Transmit Variolosser Current Out, RCV Min Volume	9	V(VOL) = −4 V, V(RTD) = −1.0 V, V(QT) = 0	I(TVL)	−6.0	+10	μA
8	Transmit Variolosser Current Out, RCV Max Volume	9	V(VOL) = V(RTD) = −1.0 V, V(QT) = 0	I(TVL)	92	121	μA
9	Receive Variolosser Current Out, Transmit Max Volume	10	V(VOL) = V(RTD) = +1.0 V, V(QT) = 0	I(RVL)	92	108	μA
10	Transmit Variolosser Current Out, Transmit Max Volume	10	V(VOL) = V(RTD) = +1.0 V, V(QT) = 0	I(RVL)	−2.0	+6.0	μA

Electrical Characteristics

(T_A = 25°C)

LB1020AF Test Specifications

Test #	Test Name	Fig. #	Test Conditions Unless otherwise stated, V+ = +6V, V− = −6V	Symbol	Specification Min	 Max	Unit
11	Receive Output Variolosser Current, Trasmit Min Volume	11	V(VOL) = −4V, V(RTD) = 0, V(TTD) = +1 V, V(QT) = 0	I(RVL)	93	108	μA
12	Transmit Output Variolosser Current, Trasmit Min Volume	11	V(VOL) = −4V, V(RTD) = 0, V(TTD) = +1 V, V(QT) = 0	I(TVL)	−2.2	+6	μA
13	RCV Variolosser Output Current Quiet/ON/OFF = OFF	12	V(QT) = −4 V	I(RVL)	150	650	μA
14	Trans. Variolosser Output Current, Quiet/ON/OFF = OFF	12	V(QT) = −4 V	I(TVL)	150	650	μA
15	RCV Variolosser Output Current RCV Quiet	12	V(QT) = +4 V	I(RVL)	−6.0	+6.0	μA
16	Trans Variolosser Output Current, RCV Quiet	12	V(QT) = +4 V	I(TVL)	150	650	μA
17	Receive-Volume Interaction Current	13	V(HLDVR) = +5.5 V	I(RVL)	−93	+108	μA
18	Transmit-Volume Interaction Current	13	V(HLDVR) = 0	I(TVL)	−6.0	10	μA
19	Noise Guard Timing Offset	6	—	V(5,4)	0	620	mV
20	Transmit State Quiescent Current	14	V(QT) = +4V, V(TTD) = +1 V, V(RTD) = 0	I(RVL)	−6.0	+6.0	μA
21	Transmit Talkdwon Current Transmit Quieting	14	V(QT) = +4V, V(TTD) = +1 V, V(RTD) = 0	I(TVL)	150	620	μA
22	Receive Talkdown Current Transmit Off	14	V(QT) = −4V, V(TTD) = 0, V(RTD) = −2 V	I(RVL)	150	620	μA
23	Transmit Talkdown Current Transmit OFF	14	V(QT) = −4V, V(TTD) = +2 V, V(RTD) = 0	I(TVL)	150	620	μA
24	Noise Guard Action Leakage	15	—	I(13)	−1.3	+1.3	μA
25	Transmit Talkdown Voice Switch Threshold	16	I(HLDVR) = −24 μA, V(RSG) = 0, V(TSG) = 0	VTH(13,4)	27.5	40	mV
26	Transmit Talkdown Voice Switch Threshold, RSG Signal	16	I(HLDVR) = −200μA, V(RSG) = −1V, V(TSG) = 0	VTH(12,4)	946	1121	mV
27	Transmit Talkdown Voice Switch Threshold, RSG Signal	16	I(HLDVR) = +65 μA, V(RSG) = 0, V(TSG) = 0	VTH(16,4)	−27.5	−42.5	mV
28	Receive Talkdown Switch Threshold, TSG Signal	16	I(HLDVR) = +65μA, V(RSG) = 0, V(TSG) = +1V	VTH(16,4)	−1375	−1633	mV
29	Receive Switch Guard Input Leakage	17	V(RSG) = V(TTD) = V(RTD) = V(TSG) = 0, S1 closed, S2-5 open	I(10)	−1.5	+1.5	μA
30	Transmit Talkdown Input Leakage	17	V(RSG) = V(TTD) = V(RTD) = V(TSG) = 0, S2 closed, S1,3,4,5 open	I(12)	−1.5	+1.5	μA

Electrical Characteristics
(Continued)

LB1020AF Test Specifications

Test #	Test Name	Fig #	Test Conditions Unless otherwise stated, V+ = +6V, V− = −6 V Switches S1-6 open, V(RSG) = V(TTD) = V(TSG) = V(RTD) = 0	Symbol	Specification Min	Specification Max	Unit
31	Transmit Switch Guard Input Leakage	17	Clsoe S3	I(14)	−1.5	+1.5	μA
32	Receive Talkdown Input Leakage	17	Close S4	I(16)	−1.5	+1.5	μA
33	Receive Talkdown Timing Leakage Current	17	Close S4 and S5. V(RTD) = +1.0 V	I(16)	−1.5	+1.5	μA
34	Receive Talkdown Timing Discharge Current	17	Close S4 and S5. V(RTD) = −1.0 V	I(16)	440	—	μA
35	Transmit Switch Guard Time Leakage Current	17	Close S3 and S6. V(TSG) = −1.0 V	I(15)	−1.5	+1.5	μA
36	Transmit Switch Guard Time Discharge Current	17	Close S3 and S6. V(TSG) = +1.0 V	I(15)	—	−440	μA
37	Transmit Talkdown Time Leakage Current	17	Close S2 and S7. V(TTD) = −1.0 V	I(11)	−1.5	+1.5	μA
38	Transmit Talkdown Time Discharge Current	17	Close S2 and S7. V(TTD) = +1.0 V	I(11)	—	−440	μA
39	Receive Switch Guard Time Leakage Current	17	Close S1 and S8. V(RSG) = +1.0 V	I(9)	−1.5	+1.5	μA
40	Receive Switch Guard Time Discharge Current	17	Close S1 and S8. V(RSG) = −1.0 V	I(9)	440	—	μA
41	Volume Control Leakage Current	18	S1,2,3,4 open. S5, S6 closed. V(VOL) = −4 V, V(TTD) = 0, V(QOO) = 0, V(HLDVR) = 0	I(22)	−1.5	+1.5	μA
42	Holdover Timing Leakage Current	18	S1,2,3,4,5 open. S6 closed. V(VOL) = 0, V(TTD) = 0, V(QOO) = 0, V(HLDVR) = +4.0 V	I(13)	−1.5	+1.5	μA
43	Noise Guard Timing Leakage Current	18	S1,4,5,6 open. S2, S3 closed. V(VOL) = 0, V(TTD) = +1 V, V(QOO) = 0, V(HLDVR) = 0	I(5)	4.5	21	μA
44	Noise Guard Drive Leakage Current	18	S1,4,5,6 open. S2, S3 closed. V(VOL) = 0, V(TTD) = −3 V, V(QOO) = 0, V(HLDVR) = 0	I(5)	—	350	μA
45	Q/O/O High Leakage Current	18	S1,2,3,4,6 open. S5 closed. V(VOL) = 0, V(TTD) = 0, V(QOO) = +4.0 V, V(HLDVR) = 0	I(3)	−12	+12	μA
45	Q/O/O Low Leakage Current	18	S1,2,3,4,6 open. S5 closed. V(VOL) = 0, V(TTD) = 0, V(QOO) = −4.0 V, V(HLDVR) = 0	I(3)	−12	+12	μA
47	Receive Talkdown Threshold	19	VTH(16,4) is the voltage between pins 16 and 4 at which V(13,14) makes the transition from > 1.2 V to < 1.2 V	VTH(16,14)	−24	−46	mV
48	Holdover Timing Threshold Voltage	20	VTH(13,4) is the voltage between the pins 13 and 4 at which I(RVL) lies between 10 and 90 μA	VTH(13,4)	.915	1.16	V

Test Circuits

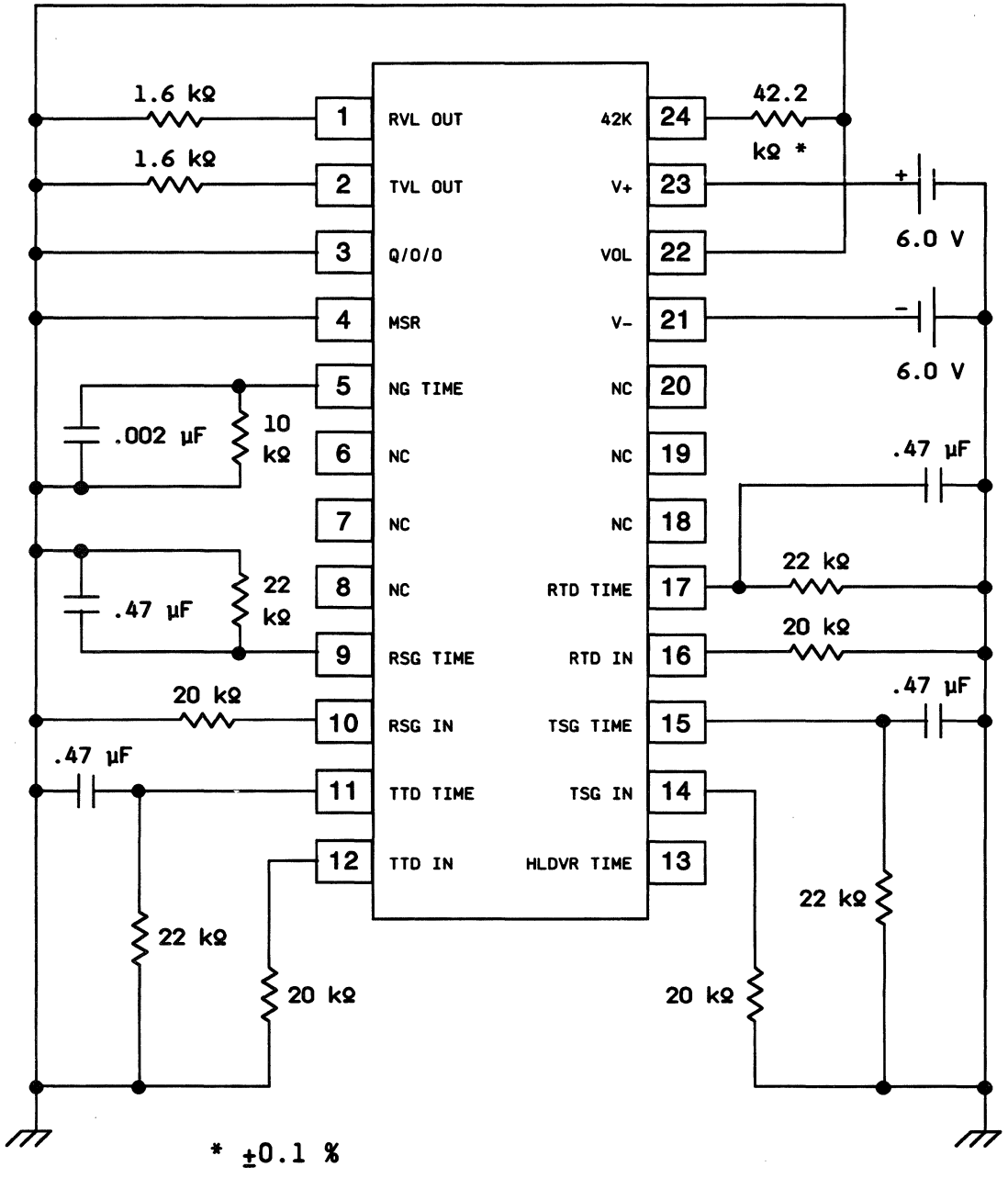


Figure 6. LB1020AF Default Test Circuit

Test Circuits
(Continued)

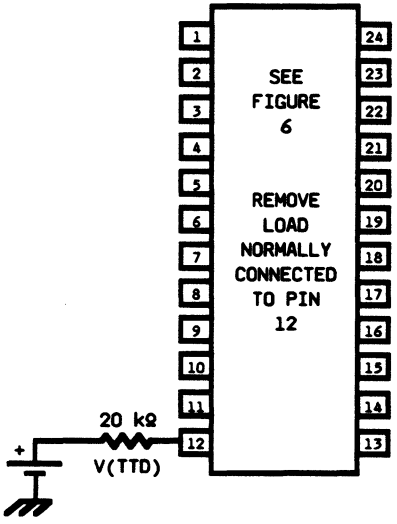


Figure 7. LB1020AF Test Circuit

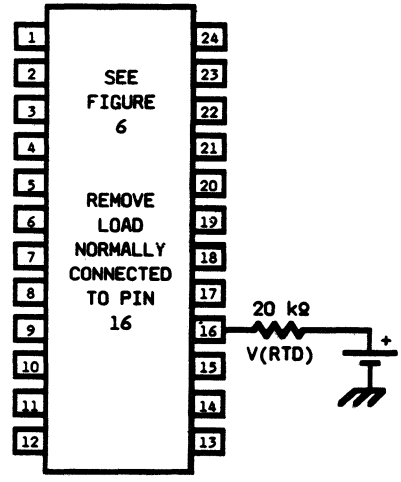


Figure 8. LB1020AF Test Circuit

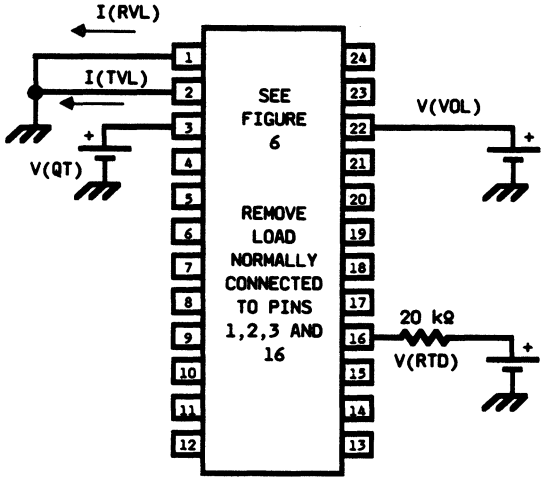


Figure 9. LB1020AF Test Circuit

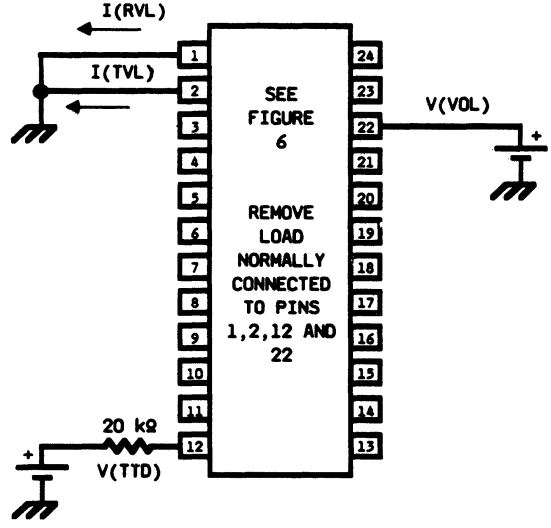


Figure 10. LB1020AF Test Circuit

Test Circuits
(Continued)

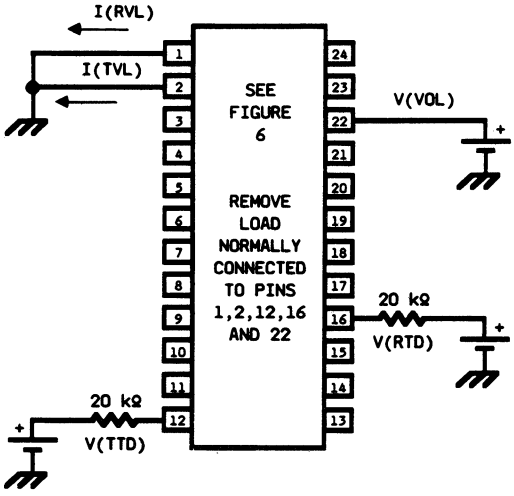


Figure 11. LB1020AF Test Circuit

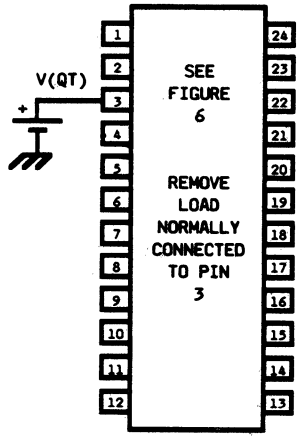


Figure 12. LB1020AF Test Circuit

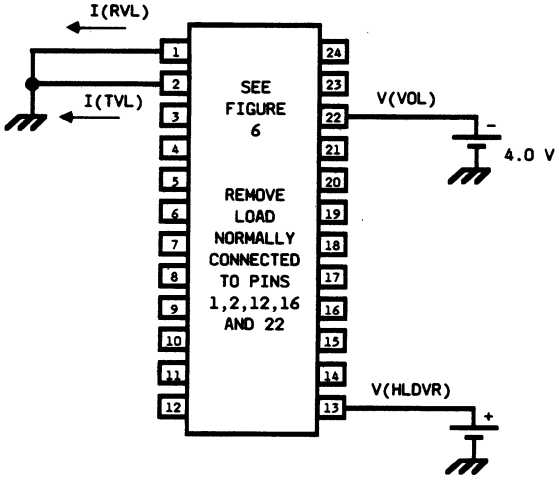


Figure 13. LB1020AF Test Circuit

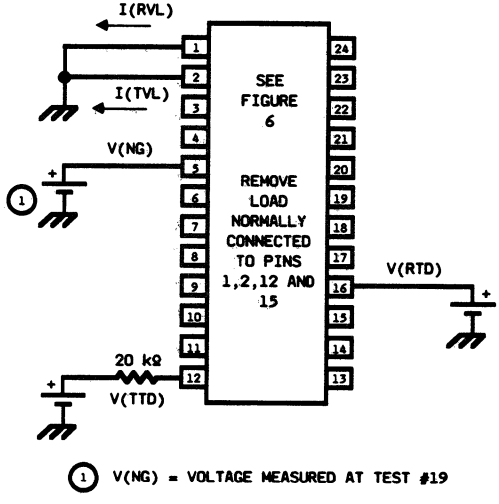


Figure 14. LB1020AF Test Circuit

Test Circuits
(Continued)

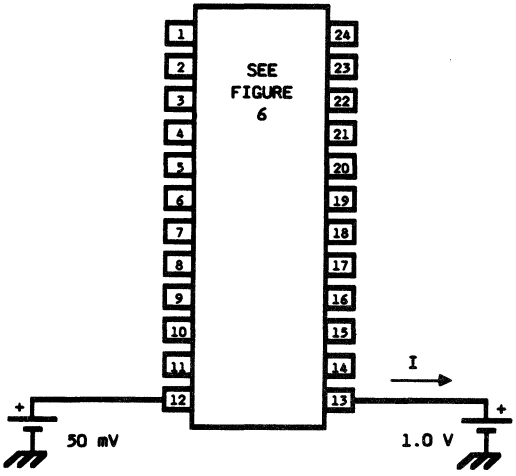


Figure 15. LB1020AF Test Circuit

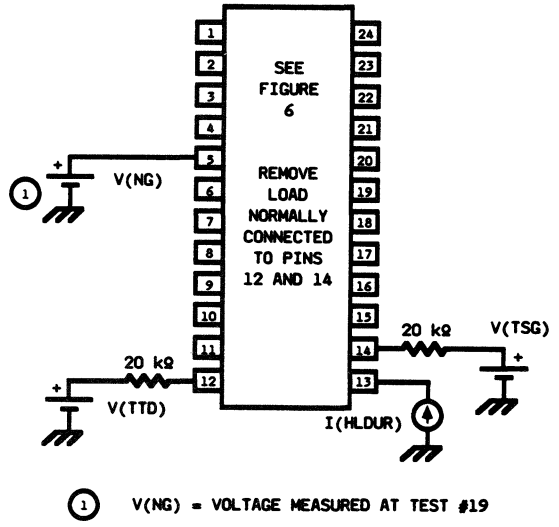


Figure 16. LB1020AF Test Circuit

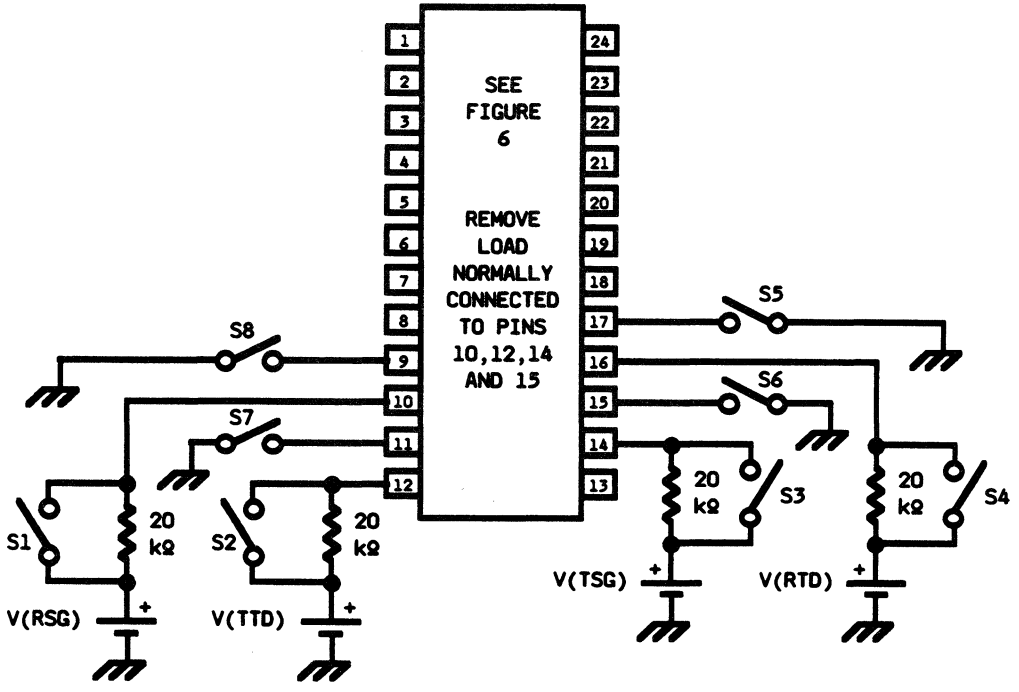


Figure 17. LB1020AF Test Circuit

Test Circuits
(Continued)

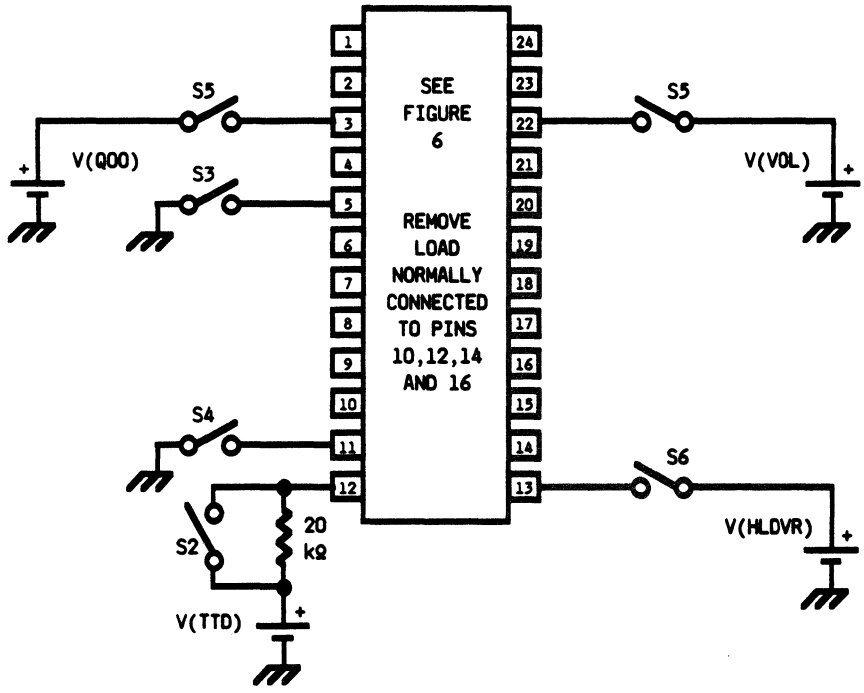
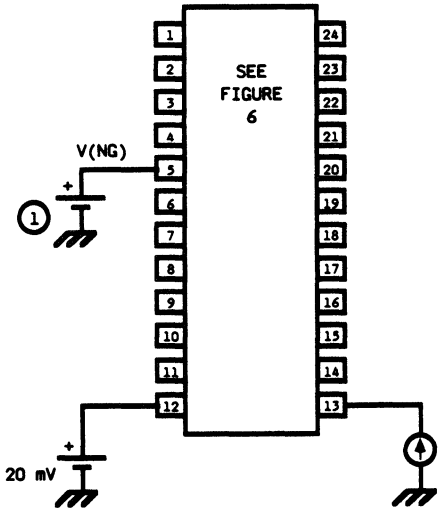
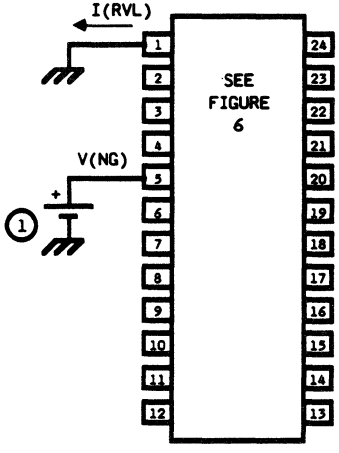


Figure 18. LB1020AF Test Circuit



(1) V(NG) = VOLTAGE MEASURED AT TEST #19

Figure 19. LB1020AF Test Circuit



(1) V(NG) = VOLTAGE MEASURED AT TEST #19

Figure 20. LB1020AF Test Circuit

Electrical Characteristics

(T_A = 25°C)

LB1021AD Test Specifications

Test #	Test Name	Fig. #	Test Conditions Unless otherwise stated, V+ = +6V, V− = −6V	Symbol	Specification Min	 Max	Unit
1	Power-Supply Current	21	Measure current into VS+ lead	IPS	8	34	mA
2	Mid-Supply Reference Voltage	21	$VREF = V(6) - \frac{V(10) - V(14)}{2}$	VREF	−120	+120	mV
3	Speaker Offest Voltage	22	Ramp current out of lead 11 from 0 to 100 μA. Measure positive and negative excursions of V(13,6)	V(13,6)	−190	+190	mV
4	Receive Switch Offset Voltage	22	Calulate difference between maximum and minimum value of V(13,6) during current ramp of test 3	△V(13,6)	—	230	mV p-p
5	Receive Switch Guard Offset	22	Ramp current out of lead 11 from 0 to 100 μA. Measure positive and negative excursions of V(9,6)	V(9,6)	−0.55	+1.2	V
6	Receive Talkdown Offset	21	—	V(15,6)	−0.55	+0.55	V
7	Receive Preamp Offset Current	23	—	I(RPRE)	−77	+77	μA
8	Mid-Supply Current Source and Sink Capability	24	V + = +5.5 V, V− = −5.5, Vary I(MSR) from −10 mA to +10 mA. Measure V(6) referenced to power-supply ground.	V±(MS)	−660	+660	mV
10	Receive Preamp Swing, Low	25	V(RIN1) = +400 mV, V(RC1) = +2.0 V, remove normal load from 17.	IOS(RPA)	—	−450	μA
11	Receive Preamp Swing, High	25	V(RIN1) = −400 mV, V(RC1) = −2.0 V, remove normal load from 17.	IOS(RPA)	+450	—	μA
12	RTD Swing, High	26	V(RIN1) = −200 mV	VOS(RTD)	+2.7	—	V
13	RTD Swing, Low	26	V(RIN1) = +200 mV	VOS(RTD)	—	−2.5	V
14	RSG Swing, High	27	I(RC2) = +200 mA	VGS (RSG)	+3.6	—	V
15	RSG Swing, Low	27	I(RC2) = −200 mA	VOS(RSG)	—	−3.6	V
16	Speaker Swing, Positive	28	I(RC2) = −500 μA, I13 = +100 mA	VOS(SPR)	+3.2	—	V
17	Speaker Swing, Negative	28	I(RC2) = +500 μA, I13 = −100 mA	VOS(SPR)	—	−3.2	V
18	Receive Preamp Common Mode Rejection	29	$ARCM(RP) = \frac{V(RC1)}{V(RIN1)}$	ARCM(RP)	—	1.75	—
19	Receive Path Transimpedance, High	30	IAC(RC2) = 10 μA rms, I(RVLIN) = 0, Z01 = V(SPKA)/I(RVLIN)	Z01	54.1	93.3	kΩ
20	Receive Path Transimpedance, Low	30	IAC(RC2) = 180 μA rms, I(RVLIN) = 100 μA, Z01 = V(SPKA)/I(RVLIN)	Z01	94.4	428	Ω
21	Receive Variolosser Range	30	AV = Z01 (Test 20)/Z01(Test 21)	AV	46	54	dB
22	Receive Switch Guard Impedance	30	I(RVLIN) = 0, IAC(RC2) = 4 μA rms, Z01(RSG) = C(RSGout)/IAC(RC2)	Z01(RSG)	400	665	kΩ
23	Receive Talkdown Current Gain	31	I(RVLIN) = 0, IAC(RC1) = 10 μA AI(RTD) = V(RTDOUT)/20.5 kΩ/10 μA	AI(RTD)	10	14	dB
24	Receive Preamp Current Gain	31	I(RVLIN) = 0, IAC(RIN1) = 30 μA, AI(PRE) = V(RC1)/1 kΩ/30 μA	AI(PRE)	7.7	16	dB

Electrical Characteristics
(Continued)

LB1021AD Test Specifications

Test #	Test Name	Fig. #	Test Conditions Unless otherwise stated, V+ = +6V, V− = −6V	Symbol	Specification Min	Specification Max	Unit
25	Overall Receive Path Gain	32	VAC(RIN1) = 20 mV, AT(RP) = V(SPKR/VAC(RIN1)	AT(RP)	38	47	dB
26	Transmit Output Offset	23	Vary I(TVL) from 0 to 100 μA while observing maximum and minimum values of V(TOUT)	V(TOUT)	−88	+88	mV
27	Transmit Switch Offset	33	In test 26, V(TOUT)(RANGE) = V(TOUT)(MAX) − V(TOUT)(MIN)	V(TOUT) (RANGE)	—	88	mV
28	Transmit Switch Guard Offset	33	Vary I(TVL) from 0 to 100 μA while observing minimum and maximum values of V(TSG)	V(TSG)	−550	+280	mV
29	Transmit Talkdown Offset	21	—	V(1,6)	−550	+550	mV
30	Transmit Talkdown Offset Current	34	S1 open, V(TC1) = 0	I(TGI)	−77	+77	μA
31	Transmit Preamp Swing, Negative	34	S1 closed. V(TC1) = +2 V, V(MK) = +0.3 V	I(TCI)	—	−360	μA
32	Transmit Preamp Swing, Positive	34	S1 closed. V(TC1) = −2 V, V(MK) = −0.12 V	I(TCI)	+450	—	μA
33	Transmit Talkdown Swing Positive	35	I(TTD) = −50 μA, V(MK) = +0.12 V	V(TTD)	3.2	—	V
34	Transmit Talkdown Swing Negative	35	I(TTD) = −50 μA, V(MK) = +0.12 V	V(TTD)	—	1.1	V
35	Transmit Switch Guard Output, Positive	36	I(TC2) = +300 μA dc, S1 closed. I(TVLIN) = 0	V(TSG)	3.2	—	V
36	Transmit Switch Guard Output, Negative	36	I(TC2) = −300 μA dc, S1 closed. I(TVLIN) = 0	V(TSG)	—	−3.2	V
37	Transmit Voltage Swing, Positive	36	S1 open, I(TC2) = −800 μA dc. I(TVLIN) = 0	V(TRAN)	2.7	—	V
38	Transmit Voltage Swing, Negative	36	S1 open, I(TVLIN) = 0, I(TC2) = +800 μA dc.	V(TRAN)dc	—	−2.7	V
39	Transmit Path Transimpedance Max	36	S1 open, 1(TVLIN) = 0, I(TC2) = 180 μA rms, Z(TRAN) = V(TRAN)/I(TC2)	Z(TRAN)	11.1	22	kΩ
40	Transmit Path Transimpedance Min	36	S1 open, 1(TVLIN) = 100 μA, I(TC2) = 180 μA rms, Z(TRAN) = V(TRAN)/I(TC2)	Z(TRAN)	25	88	Ω
41	Transmit Loss Range	36	ZV(TRAN) = ZTRAM(test 39)/ZTRAN(test 40)	AV(TRAN)	46	57	dB
42	Transmit Talkdown Voltage Gain	37	I(TVLIN) = 0, V(MIC) = 20 mV rms, ATTD = V(TTD)/V(MIC)	A(TTD)	32.7	38.4	dB
43	Transmit Preamp, Transconductance	38	I(TVLIN) = 0, V(MIC) = 20 mV rms, G(TPRE) = V(TC1)/10 kΩ/V(MIC)	G(TRPE)	3.0	8.3	mS
44	Transmit Voltage Gain	37	I(TVLIN) = 0, V(MIC) = 20 mV rms, AV(TPAN) = V(TRAN)/V(MIC)	AV(TRAN)	22.5	34	dB

Electrical Characteristics
(Continued)

LB1021AD Test Specifications							
Test #	Test Name	Fig. #	Test Conditions Unless otherwise stated, V+ = +6V, V− = −6V	Symbol	Specification Min	 Max	Unit
45	MIC-RSG Crosstalk, High Gain	37	I(TVLIN) = 100 μA, V(MIC) = 120 mV rms, ACT = V(RSG)/V(MIC)	ACT	—	3.0	dB
46	MIC-RSG Crosstalk, Low Gain	37	I(TVLIN) = 0, V(MIC) = 120 mV rms, ACT = V(RSG)/V(MIC)	ACT	—	3.0	dB
47	RIN-TSG Crosstalk	39	ACT = V(TSG)/20 mV	ACT	—	10	dB
48	Noise Output	40	Bandwidth Limited to 15 kHz	V(NOISE)	—	10	mV rms

Test Circuits

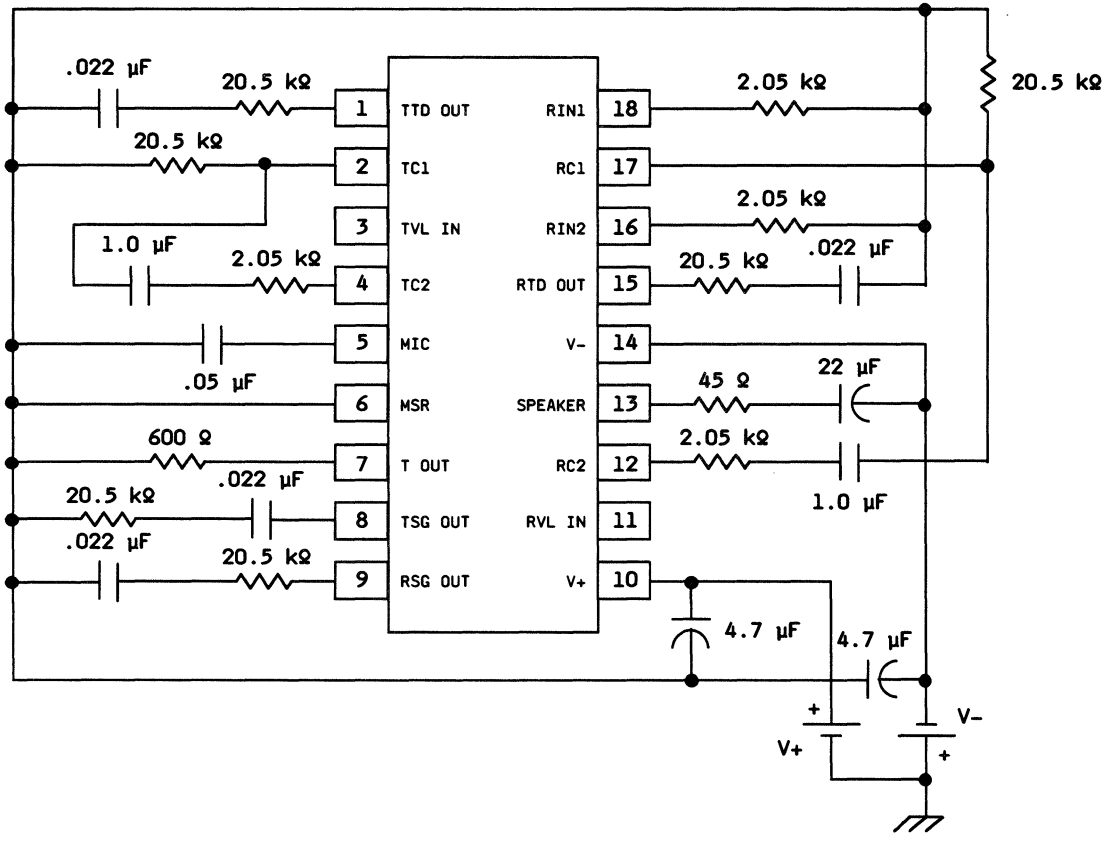


Figure 21. LB1021AD Test Circuit

Test Circuits
(Continued)

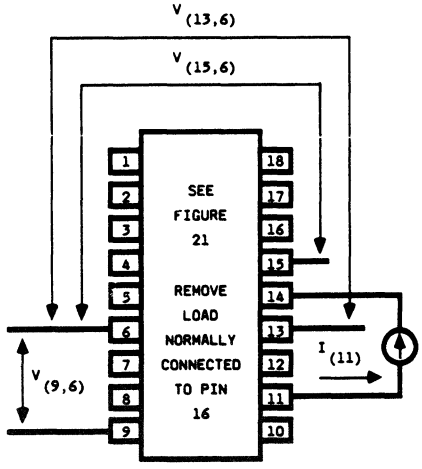


Figure 22. LB1021AD Test Circuit

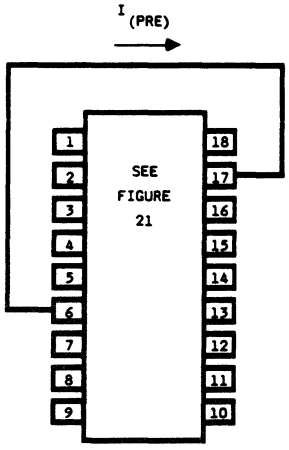


Figure 23. LB1021AD Test Circuit

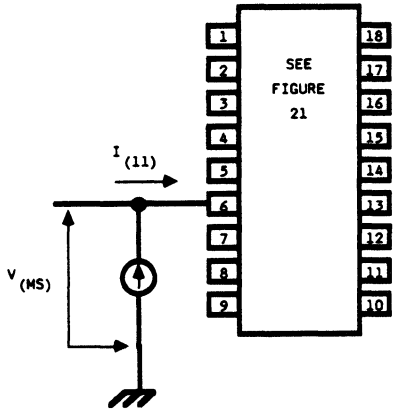


Figure 24. LB1021AD Test Circuit

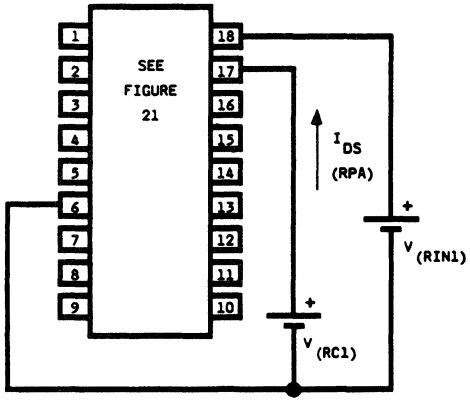


Figure 25. LB1021AD Test Circuit

Test Circuits
(Continued)

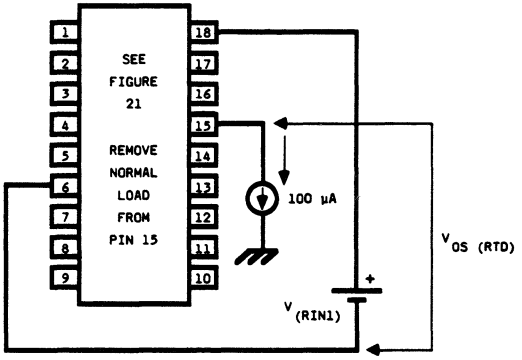


Figure 26. LB1021AD Test Circuit

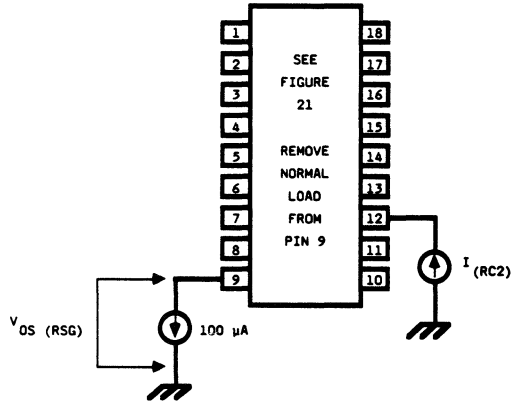


Figure 27. LB1021AD Test Circuit

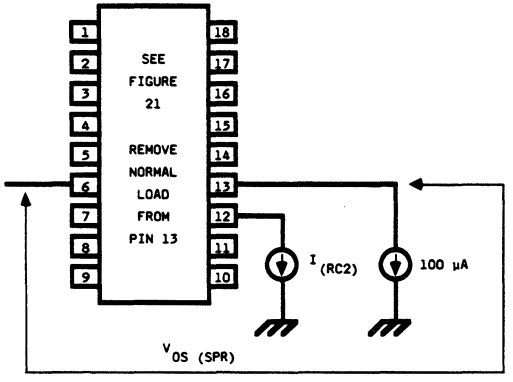


Figure 28. LB1021AD Test Circuit

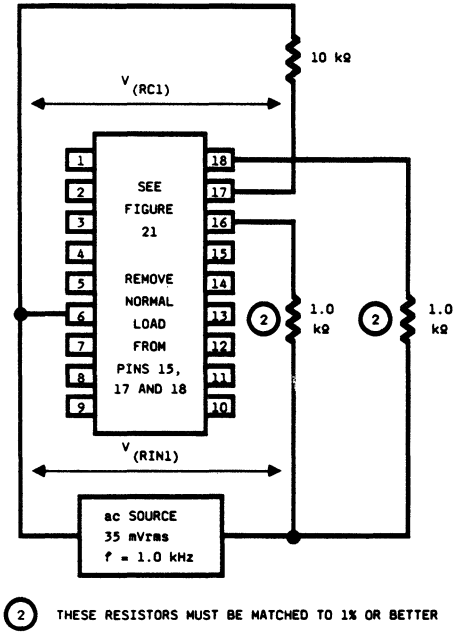


Figure 29. LB1021AD Test Circuit

Test Circuits
(Continued)

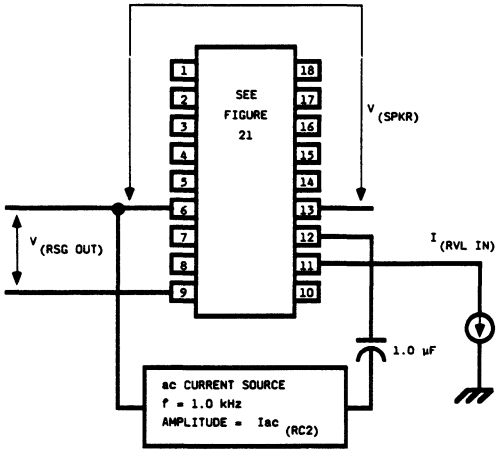


Figure 30. LB1021AD Test Circuit

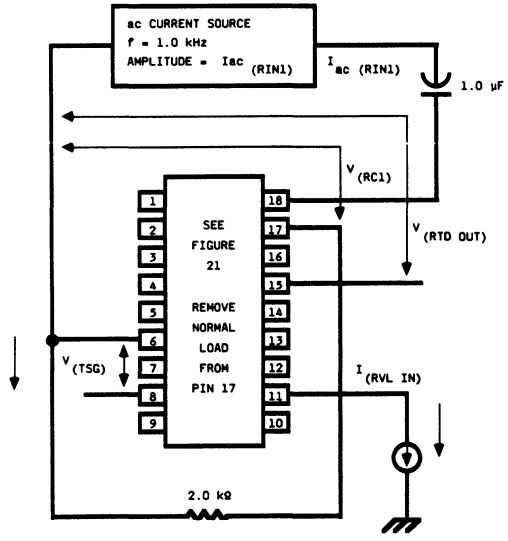


Figure 31. LB1021AD Test Circuit

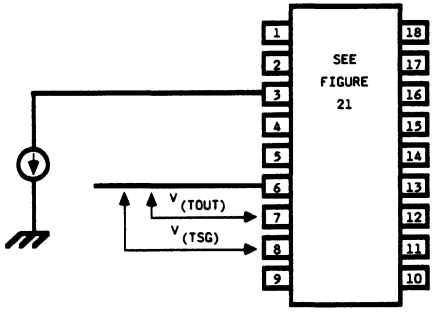


Figure 32. LB1021AD Test Circuit

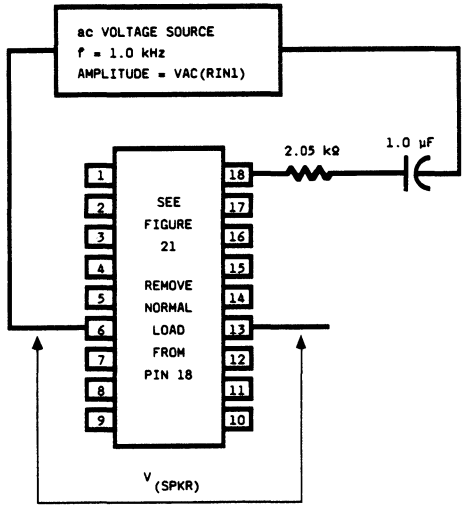


Figure 33. LB1021AD Test Circuit

Test Circuits
(Continued)

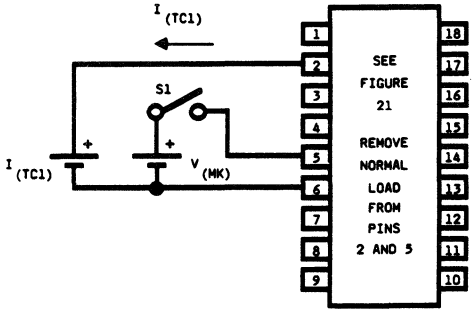


Figure 34. LB1021AD Test Circuit

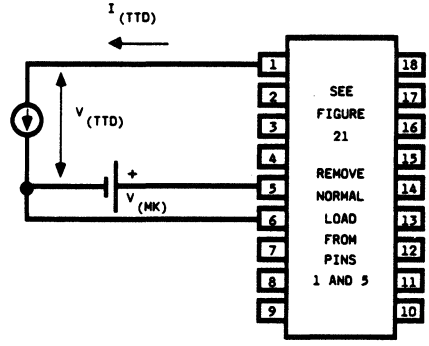


Figure 35. LB1021AD Test Circuit

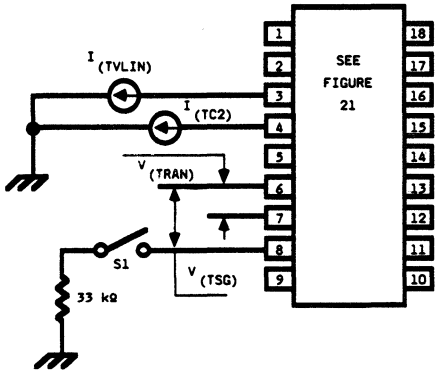


Figure 36. LB1021AD Test Circuit

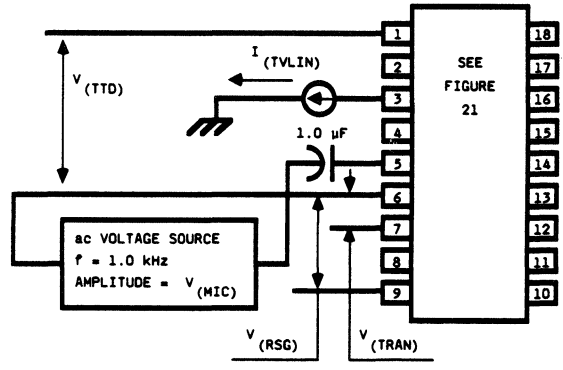


Figure 37. LB1021AD Test Circuit

Test Circuits
(Continued)

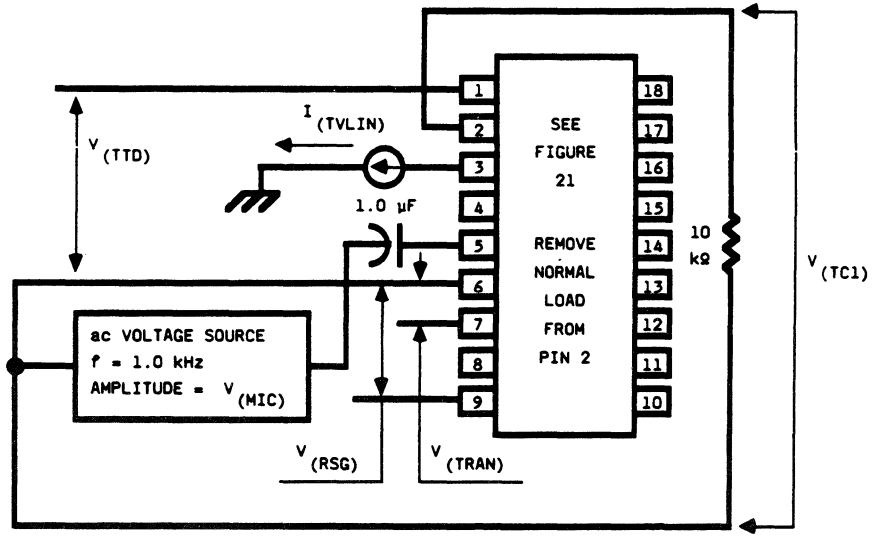


Figure 38. LB1021AD Test Circuit

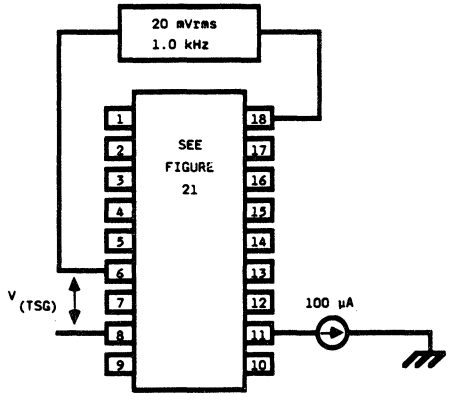


Figure 39. LB1021AD Test Circuit

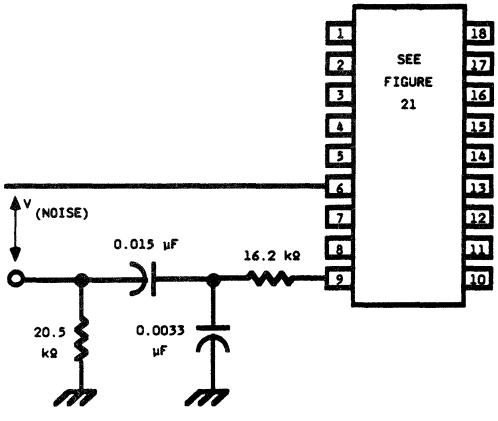


Figure 40. LB1021AD Test Circuit

Pin Description Key

(LB1020AF)

Pin	Symbol	Name/Function
1	RVL OUT	Control current which regulates the attenuation of the Receive Variolosser on the LB1021AD device. In transmit, the control current is nominally 100 μA. In receive, the value is between zero and 100 μA, depending on the volume control range.
2	TVL OUT	Control current which regulates the attenuation of the Transmit Variolosser. In transmit, it is close to zero; in receive, it is nominally 100 μA.
3	Q/O/O	Quiet-On-Off; Quiet is $>$ 2 volts, Off is $<$ $-$2 volts, On is nominally zero volts.
4	MSR	Midsupply Reference input for the reference voltage received from the LB1021AD.
5	NG TIME	Noise Guard Timing node to which a capacitor (usually of a large value) is externally connected and sets the time over which the noise guard signal is averaged.
6, 7, 8	NC	No connection. These pins should not be used as tie points for external components.
9	RG TIME	Receive Switch Guard Timing node, to which the RC circuit is connected. The RC circuit time constant determines the response of the noise guard peak catcher in decaying when the noise guard signal decreases.
10	RSG IN	Input to the receive switch guard peak detector from LB1021AD through an RC voltage divider. The ratio of this divider sets the relative weight of this signal.
11	TTD TIME	Transmit Talkdown Timing. The RC circuit at this point sets the time constant of the peak detector for the Transmit Talkdown signal.
12	TTD IN	This is the input to the Transmit Talkdown Detector.
13	HLDVR TIME	Holdover Timing node. The RC pair at this point sets the timing of the transition back to the receive state when an idle condition is preceded by transmit. It has little effect on the timing of the forced receive transition.
14	TSG IN	"Transmit Guard Switch In" is the input to the transmit switch guard peak detector.
15	TSG TIME	The RC pair at this point sets the dynamics of the Transmit Switch Guard peak detector.
16	RTD IN	Input to Receive Talkdown peak detector.
17	RTD TIME	Sets the time constant associated with the Receive Talkdown peak detector.
18, 19, 20	NC	No connection. These pins should not be used as tie points for external components.
21	V$-$	Negative power-supply connection.
22	VOL	Volume control input varies from $-$4 volts (minimum volume) to zero volts (maximum volume).
23	V+	Positive power-supply connection.
24	42 K	Connection from Midsupply Reference (MSR through a 42.2 k ohm, 1% resisitor).

Pin Description Key

(LB1021AD)

Pin	Symbol	Name/Function
1	TTD OUT	Output of the Transmit Talkdown amplifier. This voltage is proportional to the output of the microphone.
2	TC1	Current output of the transmit preamplifier which drives the transmit variolosser. There are two outputs of both the transmit preamplifiers (Figure 5); one to drive the variolosser, the other to drive the talkdown circuits.
3	TVL IN	Transmit variolosser control current input.
4	TC2	Transmit variolosser signal current input which is connected to pin 2 (TC1) via an RC circuit.
5	MIC	Microphone Input. There is sufficient gain to handle low-level microphones. Higher output microphone types may need a resistive pad. The return path to the microphone is the midsupply reference.
6	MSR	Midsupply Reference Output. A voltage midway between the positive and negative supply, used for signal reference.
7	T OUT	Transmit Output, which drives the line in the transmit mode.
8	TSG OUT	Transmit Switch Guard Output. This voltage drives the transmit switch guard peak detector and is proportional to the transmitted signal.
9	RSG OUT	Receive Switch Guard Output is proportional to the voltage which drives the speaker and it is an input to the RSG peak detector.
10	V+	Positive power-supply input.
11	RVL IN	Receive variolosser control current input. The source originates in the LB1020AF device.
12	RC2	The signal current input to the receive variolosser.
13	SPEAKER	Output to a speaker via a connection through a capacitor.
14	V-	Negative power-supply connection. The return path from the speaker is connected to this pin also.
15	RTD OUT	Receive Talkdown Output, proportional to the receive input signal.
16	RIN2	This is one of the two input connections from a microphone through a resistor. When the receive signal source is single-ended, this pin is tied to a mid-supply reference.
17	RC1	The output of the receive amplifier which drives the variolosser.
18	RIN1	Input from receive hybrid through a resistor.

Applications

Figures 1, 4 and 5 are simplified circuits and block diagrams (with pinout information where appropriate) of a complete Speakerphone IC Device Set. A complete discussion of these functions is given in the APPLICATION NOTE which is referenced on the front page of this data sheet.

One of the outstanding features of this Speakerphone Set is the possibility to set most electrical and working components by means of external components. Figure 41 shows a circuit which provides values for components in a general basic application.

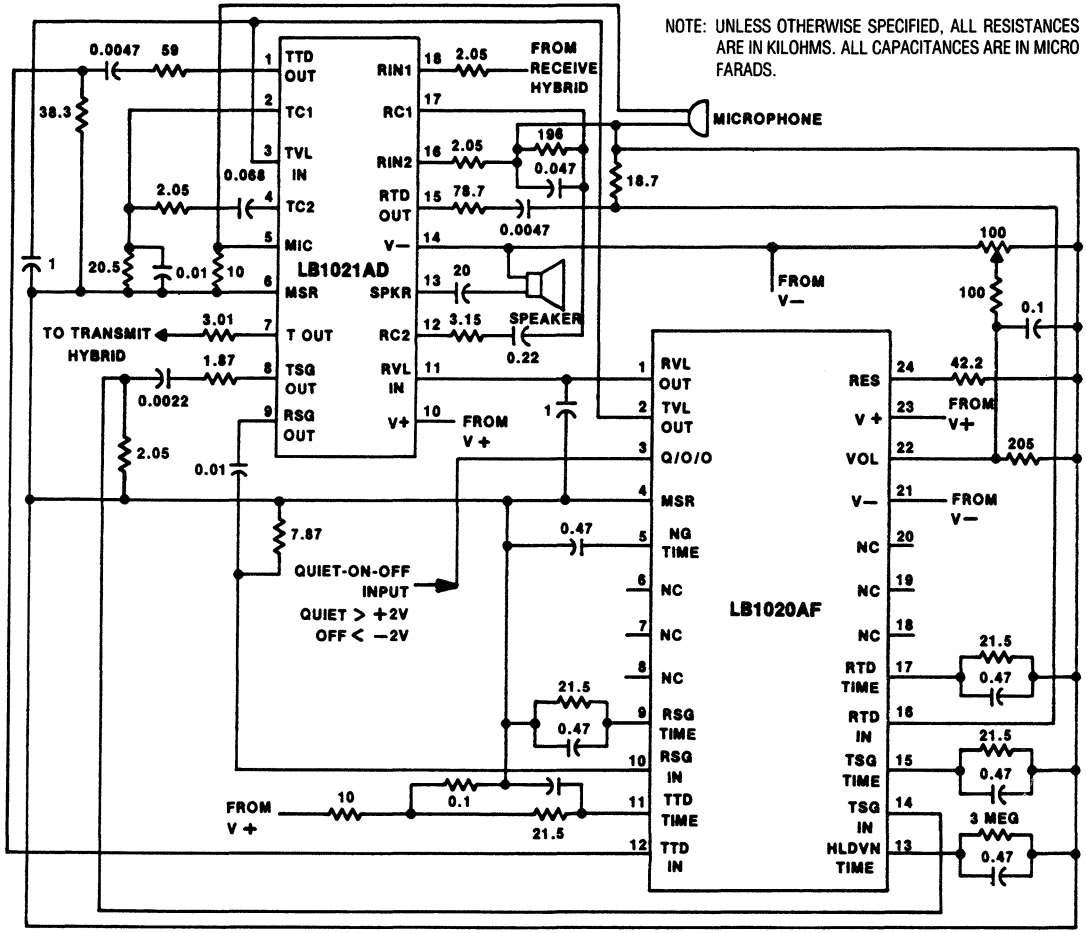


Figure 41. Typical Speakerphone Basic Application

Applications
(Continued)

Specific applications are shown in the following two circuits. Figure 42 is a typical line-coupled application, while Figure 43 is a typical telephone-coupled application. Both of these applications use a 50-ohm speaker, an electret PRIMO microphone and a 12-volt power-supply. Both applications use a standard telephone set that performs dial and alerting functions.

Detailed circuit performance characteristics for the circuits shown in Figures 42 and 43 will be provided in an Application Note.

The line-coupled application uses a transformer (T1) to perform the two- to four-wire conversion, and to match the line with a proper DC and AC impedance. The line is switched to the transformer or to the standard telelphone set by means of a switch (SW3). To dial or to detect the ringing signal, a telelphone set must be connected to the line. The Speakerphone can be activated only after dialing or ringing detection is completed.

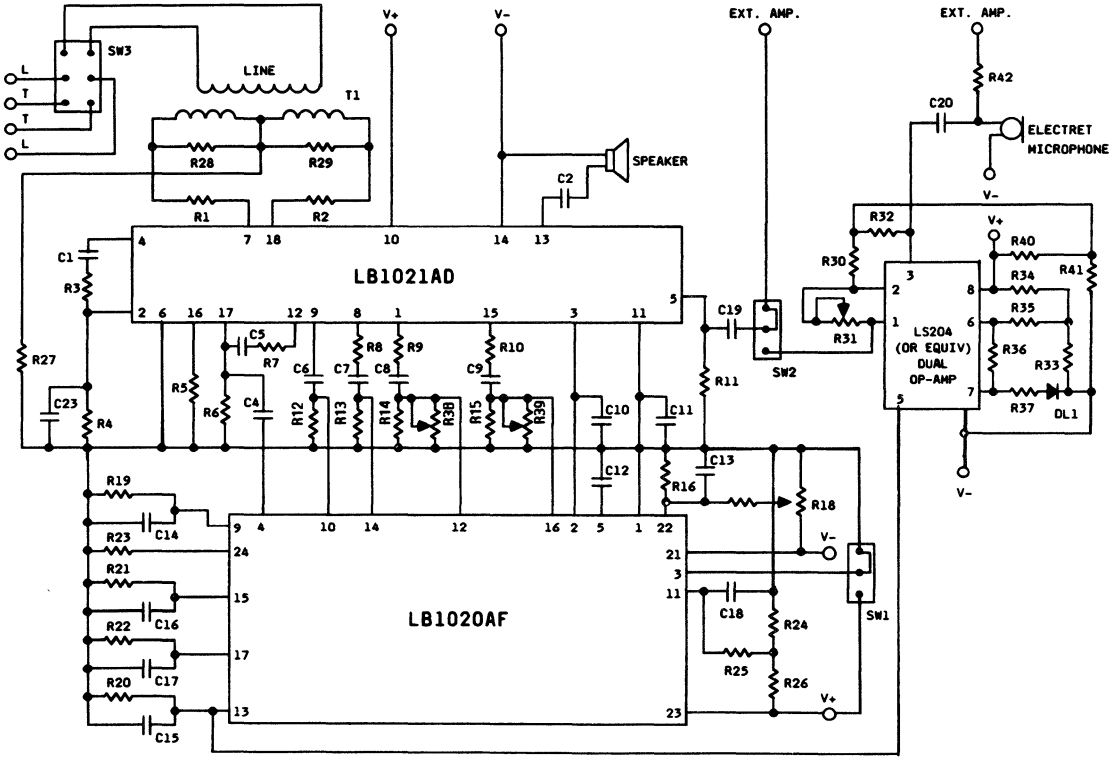


Figure 42. Typical Speakerphone Line-Coupled Application

Applications
(Continued)

Figure 42 Parts List (Line-Coupled Application)

R1	=	10 ohm	R37	=	2.4 k ohm
R2	=	2 k ohm	R38	=	100 k ohm
R3	=	2 k ohm	R39	=	47 k ohm
R4	=	2 k ohm	R40	=	1 k ohm
R5	=	2 k ohm	R41	=	1 k ohm
R6	=	200 k ohm	R42	=	2 k ohm
R7	=	3 k ohm			
R8	=	1.8 k ohm	C1	=	68 nF
R9	=	56 k ohm	C2	=	20 μF
R10	=	75 k ohm	C3	=	10 nF
R11	=	10 k ohm	C4	=	47 nF
R12	=	7.5 k ohm	C5	=	220 nF
R13	=	2 k ohm	C6	=	10 nF
R14	=	39 k ohm	C7	=	2.2 nF
R15	=	18 k ohm	C8	=	4.7 nF
R16	=	200 k ohm	C9	=	4.7 nF
R17	=	100 k ohm	C10	=	1 μF
R18	=	100 k ohm	C11	=	1 μF
R19	=	22 k ohm	C12	=	47 μF
R20	=	3 M ohm	C13	=	100 nF
R21	=	22 k ohm	C14	=	470 nF
R22	=	22 k ohm	C15	=	470 nF
R23	=	43 k ohm	C16	=	470 nF
R24	=	100 ohm	C17	=	470 nF
R25	=	22 k ohm	C18	=	470 nF
R26	=	10 k ohm	C19	=	100 nF
R27	=	130 ohm	C20	=	100 nF
R28	=	10 k ohm			
R29	=	10 k ohm	DL1	=	LED
R30	=	10 k ohm			
R31	=	470 k ohm	T1	=	Hybrid Transformer
R32	=	100 k ohm			
R33	=	8.2 k ohm	SW1	=	Switch 1 way 2 position
R34	=	3.9 k ohm	SW2	=	Switch 1 way 2 position
R35	=	1 k ohm	SW3	=	Switch 2 way 2 position
R36	=	100 k ohm			

Applications
(Continued)

The telephone-coupled application uses the internal speech circuit of the standard telelphone set to perform the two- to four-wire conversion and to obtain a proper line impedance match. The terminations of the handset are switched either to the handset itself or to the speakerphone by means of switches SW2 and SW3. A common reference level for all signals is important. This reference level can be obtained with a floating power supply whose negative connection is connected to the negative termination of the line.

Note: This circuit is designed to operate with a telephone set which uses either an SGS **LS656** or **LS156** (or equivalent) speech circuit.

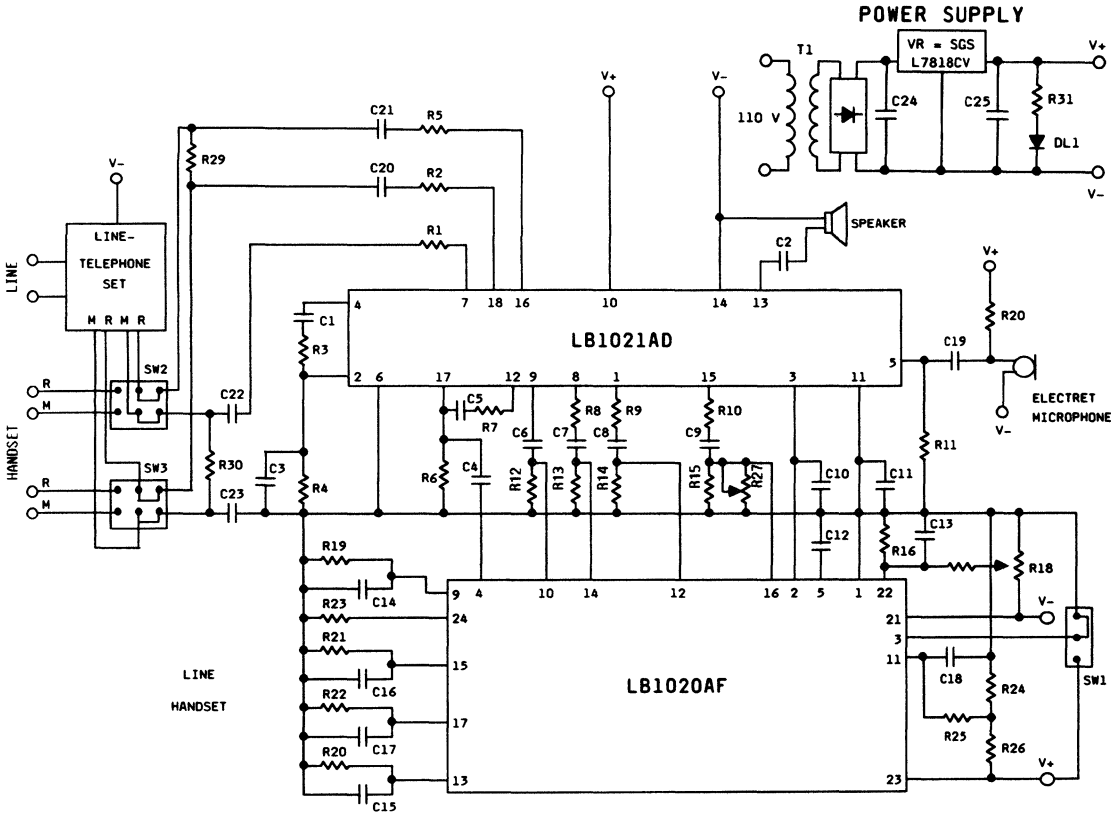


Figure 43. Typical Speakerphone Telephone-Coupled Application

Applications
(Continued)

Parts List for Figure 43 (Telephone-Coupled Application)

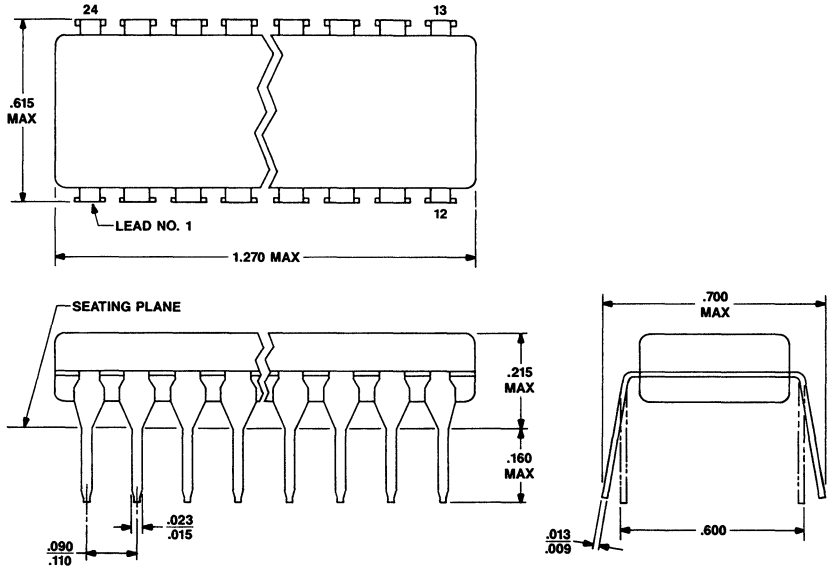
R1	=	3 k ohm	C1	=	68 nF
R2	=	2 k ohm (8.2 k ohm)	C2	=	20 μF
R3	=	2 k ohm	C3	=	10 nF
R4	=	2 k ohm	C4	=	47 nF
R5	=	2 k ohm (8.2 k ohm)	C5	=	220 nF
R6	=	200 k ohm	C6	=	10 nF
R7	=	3 k ohm	C7	=	220 nF
R8	=	1.8 k ohm	C8	=	33 nF
R9	=	8.2 k ohm	C9	=	4.7 nF
R10	=	75 k ohm	C10	=	1 μF
R11	=	10 k ohm	C11	=	1 μF
R12	=	3.9 k ohm	C12	=	47 μF
R13	=	2 k ohm	C13	=	100 nF
R14	=	39 k ohm	C14	=	470 nF
R15	=	10 k ohm	C15	=	470 nF
R16	=	200 k ohm	C16	=	470 nF
R17	=	100 k ohm	C17	=	470 nF
R18	=	100 k ohm	C18	=	470 nF
R19	=	22 k ohm	C19	=	100 nF
R20	=	3 M ohm	C20	=	1 μF
R21	=	22 k ohm	C21	=	1 μF
R22	=	22 k ohm	C22	=	22 μF
R23	=	43 k ohm	C23	=	22 μF
R24	=	100 ohm	C24	=	2200 μF
R25	=	22 k ohm	C25	=	100 nF
R26	=	10 k ohm			
R27	=	10 k ohm	DL1	=	LED
R28	=	2 k ohm			
R29	=	200 ohm (4.7 k ohm)	T1	=	220 to 12 Volt Transformer
R30	=	— (220 ohm)			
R31	=	4.3 k ohm			

SW1 = Switch 1 way 2 position
SW2 = Switch 2 way 2 position
SW3 = Switch 2 way 2 position

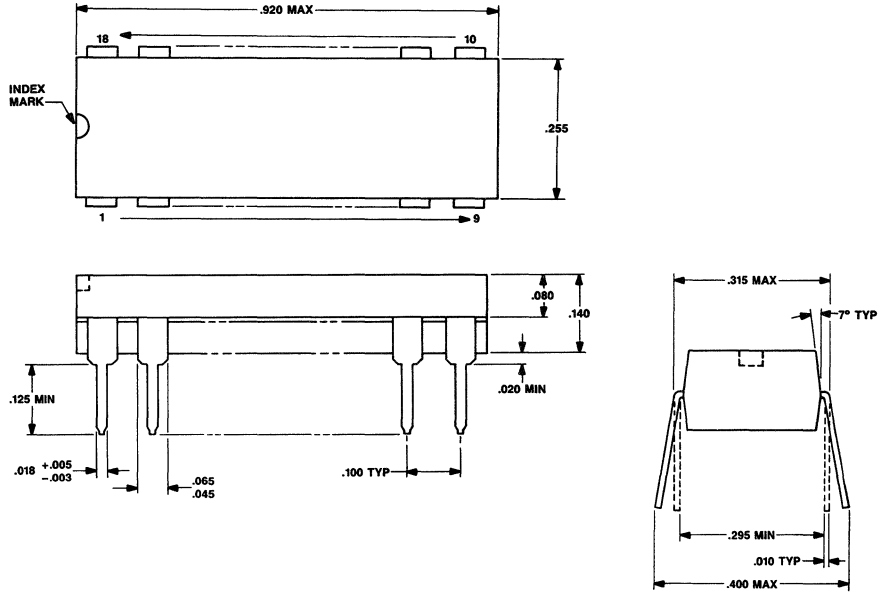
The values in brackets concern the components that must be changed for the application with the LS156.

Outline Drawings (Dimensions in Inches)

LB1020AF



LB1021AD



Ordering Information

Device	Comcode
LB1020AF	104208897
LB1021AD	104208905

HIGH-VOLTAGE DUAL OP-AMP

LB1013AD

PRELIMINARY

Description

The LB1013AAD High-Voltage Dual Op-amp integrated circuit operates off a single power-supply from 5 to 85 volts, or a dual power-supply from ±2.5 to ±42.5 volts. The amplifiers are internally compensated and are designed to operate in the audio band. This device is powered up with a current supplied to the IBIAS pin (typically 40 to 80 μA). External circuitry is required to provide short-circuit protection.

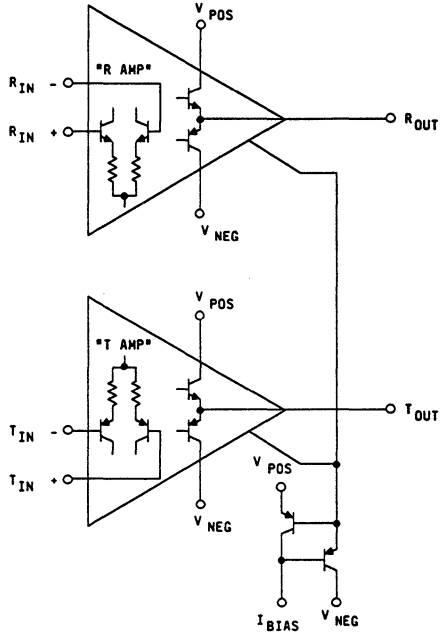
Features

- Typical ft = 1 MHz
- Open Loop Gain; 50 dB @ 3 kHz
- Provides output currents ±40 to ±80 mA (depending upon the IBIAS value)
- Operating temperature range (−25 to +100°C)

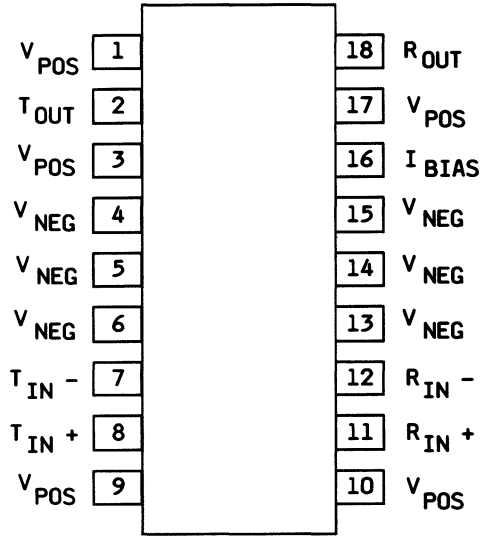
Applications

- Transconductance amplifiers for telephone line driving
- Voltage followers
- Audio amplifiers
- General-purpose circuits requiring high-voltage, high-power op-amps

Functional Diagram



Pin Diagram



Maximum Ratings (At 25°C unless otherwise specified)	
Ambient Operating Temperature Range	−25 to +100°C
Storage Temperature Range	−40 to +125°C
Pin Soldering Temperature (t = 15 s max.)	300°C
Power Dissipation (see note under Outline Drawing)	2 W
Voltage (V_{POS} to V_{NEG})	85 V

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may affect device reliability.

Pin Description

Pin	Symbol	Name/Function
1,3,9, 10,17	V_{POS}	The more positive supply voltage is connected to the five pins designated as V_{POS}. Either V_{POS} or V_{NEG} can be connected to ground.
2 18	T_{OUT} R_{OUT}	These pins are the op-amp outputs for the "T" amplifier and the "R" amplifier, respectively.
4,5,6 13,14,15	V_{NEG}	The more negative supply voltage is connected to the six pins designated as V_{NEG}. Either V_{NEG} or V_{POS} can be connected to ground.
7 8	$T_{IN}+$ $T_{IN}+$	These pins are the inverting and the noninverting inputs, respectively, for the "T" amplifier.
11 12	$R_{IN}+$ $R_{IN}-$	These pins are the noninverting and the inverting pins, respectively, for the "R" amplifier.
16	I_{BIAS}	A current source (or a suitable value resistor to V_{NEG}) can be connected to this pin. A negative current flow must be present before the LB1013AD becomes operational.

Typical Device Characteristics

(T_A = 25°C)

Characteristic	I_{BIAS} V_{POS} = 40 μA	I_{BIAS} = 80 μA
Slew Rate	2 V/μs	4 V/μs
Output Current	±40 mA	±80 mA
Power-Supply Rejection Ratio	45 dB	45 dB

Electrical Characteristics

(T_A = 25°C, V_{POS} = 25 V, V_{NEG} = −25 V, I_{BIAS} connects through 1.25 MΩ to V_{NEG}, unless otherwise specified)

Characteristic	Test Condition	Min	Max	Unit
Open-Loop Gain	f = 100 Hz f = 1 Hz	75 55	— —	dB dB
Input Offset Voltage	—	—	±5.0	mV
Input Bias Current	Inverting and Noninverting Pins	—	±1.0	μA
Input Offset Current	—	—	±1.0	μA
Common-Mode Rejection Ratio	V_{NEG} = −30 V, VCM = X ± Y	80	—	dB
Output Voltage Swing, "R" Amplifier	V_{HIGH} V_{LOW} V_{POS} = 38 V, V_{NEG} = −38 V Noninv. Input = Gnd ΔV (Inv. Input = ±0.5 V) I_{BIAS} = 40 μA, R_L = 1 kohm	+36.8 −34.6	— —	V V
Output Voltage Swing, "T" Amplifier	V_{HIGH} V_{LOW}	+36.0 −34.6	— —	V V
Power-Supply Currents (Amplifiers Activated Under No-Load Conditions)	V_{POS} = 42.5 V, V_{NEG} = −42.5 V See Figure 1 I_{VPOS} I_{VNEG}	— —	1.1 −1.1	mA mA
Power-Supply Leakage Current (Amplifiers Off)	V_{POS} = 25V, V_{NEG} = −35 V I_{BIAS} = Open; See Figure 1 I_{VPOS} I_{VNEG}	— —	±10 ±10	μA μA
Output Leakage Currents (Amplifiers Off)	V_{POS} = 35 V, V_{NEG} = −35 V I_{BIAS} = Open; See Figure 2 V_{LOAD} = 30 V V_{LOAD} = −30 V	— —	±10 ±10	μA μA
T_{OUT} to V_{POS} Fault Current	V_{LOAD} = 35 V, t = 100 ms, See Figure 3	41	47	mA
T_{OUT} to V_{NEG} Fault Current	V_{LOAD} = −35 V, t = 100 ms, See Figure 3	−41	−47	mA
R_{OUT} to V_{POS} Fault Current	V_{LOAD} = 35 V, t = 100 ms, See Figure 3	41	47	mA
R_{OUT} to V_{NEG} Fault Current	V_{LOAD} = −35 V, t = 100 ms, See Figure 3	−41	−47	mA

Simplified Test Circuits

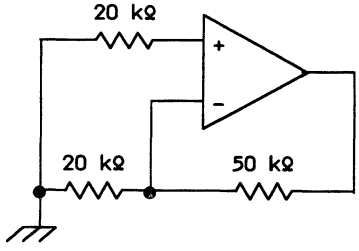


Figure 1. Power-Supply Current, (Connect both op-amps as shown above)

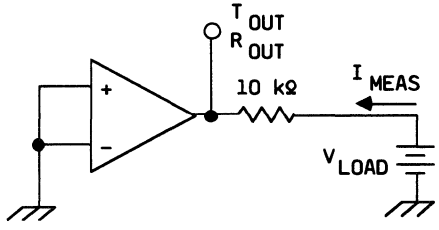


Figure 2. Output Leakage Current, (The current through V_{LOAD} is the leakage current)

Simplified Test Circuits (Continued)

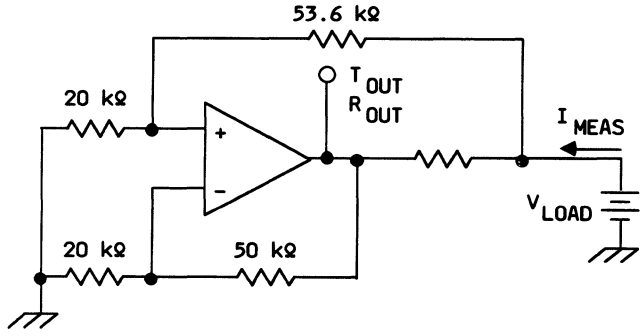
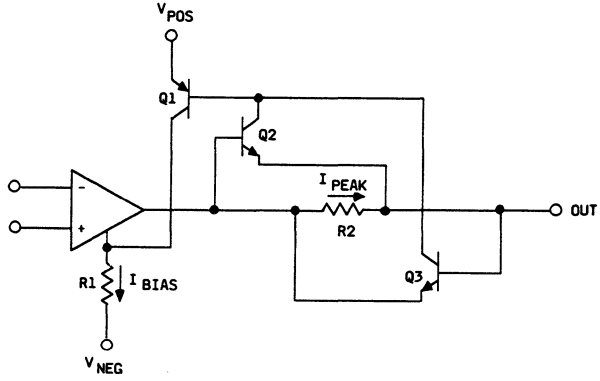


Figure 3. Fault Current

Short-Circuit Protection



NOTES:
1. Q1, Q2, Q3; $V_{(BR)CEO}$ >90 V
2. R1 = $\frac{V_{POS} - V_{NEG} - 1.2\ V}{I_{BIAS}}$
3. R2 = $\frac{0.6\ V}{I_{PEAK}}$

Figure 4. External Circuitry for Short-Circuit Protection

Typical Characteristics

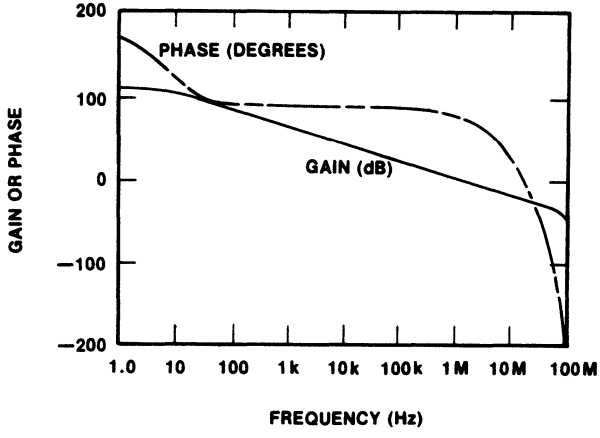


Figure 5. Gain/Frequency Response Curve

Applications

The simplified schematic shown below illustrates an application as a transconductance amplifier for telephone line drive applications. Other applications include high voltage/power voltage followers, audio amplifiers and circuits where high-voltage, high-power op-amp capability are required.

The equations relating to the circuit shown below are as follows:

$$\text{For R1 \& R2} > > \text{R3}$$

$$I_T = \frac{V_C - V_D}{R1} \times \frac{R2}{R3}$$

$$I_R = -\frac{(V_C + V_D)}{R1} \times \frac{R2}{R3}$$

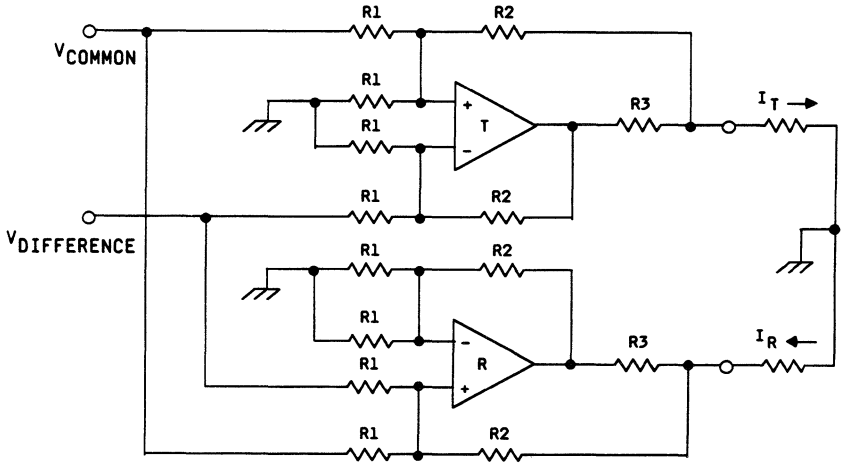


Figure 6. Simplified Line Feed Operation (Power-Supply Connections Not Shown)

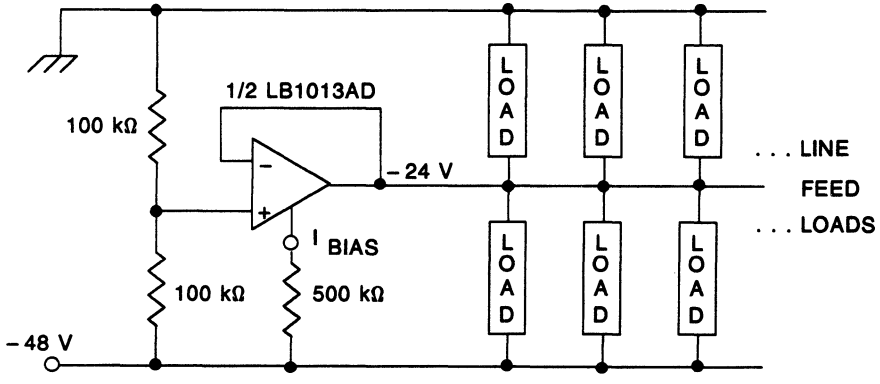
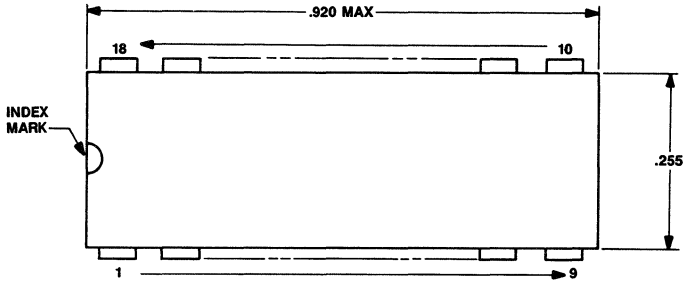
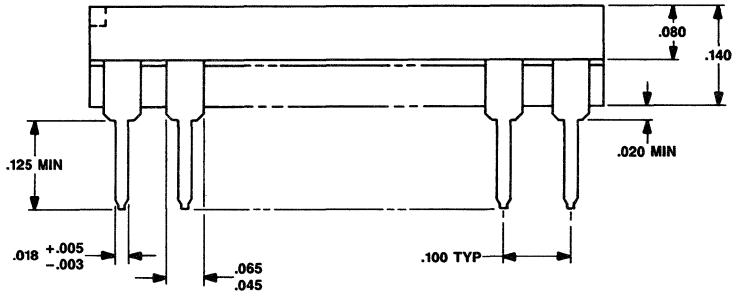


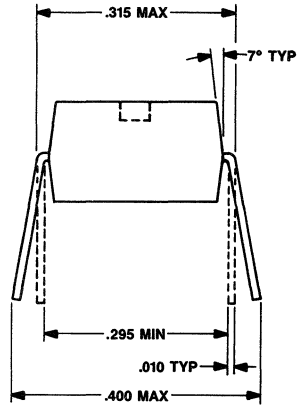
Figure 7. Typical Voltage Follower

Outline Drawing

(Dimensions in Inches)







Ordering Information

Device	Comcode
LB1013AD	104208848

Description

The LB1029BB/BC are dual general-purpose wideband op-amps with internal compensation. This dual general-purpose op-amp is available in an 8-pin plastic DIP (LB1029BB) and in a 16-pin plastic DIP (LB1029BC).

The LB1029BB/BC provides approximately 20 dB improvement in RFI immunity (up to 100 MHz) as compared to standard voice-frequency amplifiers. They also feature high-output capability ($\geq \pm$ 15 mA), short-circuit protection, static-discharge protection, offset-voltage-null capability, $f_T \geq 3.5$ MHz, and large common-mode-voltage range. These devices will operate over a power-supply range of ± 5.0 to ± 15 volts.

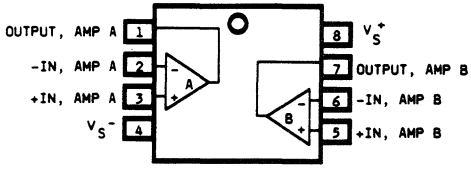
The LB1029BC has the additional capability of an external offset null adjustment for each amplifier.

Features

- Guaranteed minimum unity-gain frequency of 3.5 MHz with internal compensation
- 1.3 V/μs typical slew rate
- Large common-mode voltage range
- 15 mA minimum output current capability
- Offset voltage null capability (LB1029BC)
- Short circuit current limited
- Static discharge protection
- Supply voltage range: ± 5.0 to ± 15 volts
- Differential-mode voltage range: ± 6.0 volts
- 16 pin plastic DIP; 400 mW

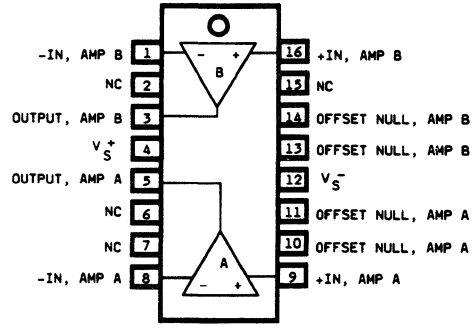
Pin Diagrams

LB1029BB



Power-supply connections are common for two amplifiers.

LB1029BC



Power-supply connections are common for two amplifiers. If offset null is not desired for either amplifier, leads 10, 11, 13, and 14 must be connected to lead 12.

Maximum Ratings (At 25°C unless otherwise specified)	
Supply Voltage Range (V_S^- and V_S^+)	30 V
Differential Mode Input Voltage (−IN to +IN)	±6.0 V
Power Dissipation	500 mW
Storage Temperature Range	−40 to +125°C
Ambient Operating Temperature Range	0 to +60°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may affect device reliability.

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic and Test Condition	Symbol	Min	Typ①	Max	Unit
Test Condition Supply Voltage	V_S	±15	±15	±15	V
Extrapolated Unity Gain Frequency ($C_C = C_{INT}$)④	f_T	3.5	5.0	12	MHz
Open-Loop Voltage Gain (R_L = 10 kΩ, f = 100 Hz, C_C = C_{INT}) (Figure 1)	A_{VOL}	88	96	—	dB
Input Offset Voltage (Figure 2)	$\lvert V_{IO}\rvert$	—	1.0	4.5	mV
Input Bias Current (Figure 3)	I_{IB}	—	−120	−400	nA
Input Offset Current② (Figure 3)	$\lvert I_{IP}\rvert$	—	10	80	
Output Voltage Swing (R_L = 10 kΩ) (Figure 4)	V_{OM}	+13.6 −13.0	—	—	V(peak)
Output Current Drive (R_L = 100 Ω)	I_O	+15 −15	+32 −32	+60 −125	mA
Common-Mode Voltage Range ($\triangle V_{IO}$ = 2.0 mV)	CMVR	+13.8 −13.8	—	—	V
Common-Mode Rejection Ratio (Figure 5)	CMRR	86	100	—	dB
Power-Supply Rejection Ratio (Figure 6)	$\lvert PSRR(\pm)\rvert$	86	105	—	
Power-Supply Current③ (Figure 7)	I_{PS}	—	2.2	3.0	mA
Slew Rate (Typical) (Figures 8 and 9)	SR	—	+1.3 −1.3	—	V/μs
Temperature Coefficient of Input Offset Voltage (−20°C to +80°C)④	TCV_{IO}	—	8.0	—	μV/°C
Differential Input Breakdown Voltage	$V_{(BR)}$	±6.0	±8.5	—	V

① Individual devices may differ significantly from the typical values shown.
② This current may degrade if the differential input voltage exceeds ±6.0 V.
③ Total current for both amplifiers.
④ This condition is not tested in production devices.

Test Circuits

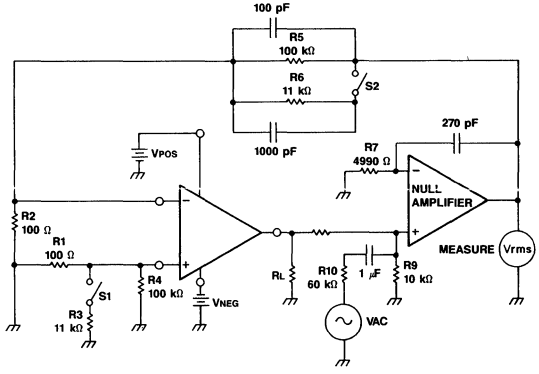


Figure 1. Open Loop Gain Test Circuit

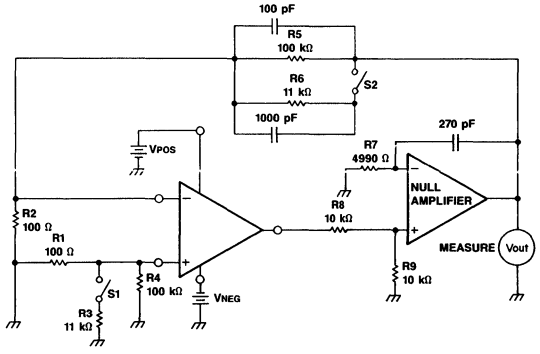


Figure 2. Input Offset Voltage (V_{IO}), Input Bias Current (I_{IB}), and Input Offset Current (I_{IO}) Test Circuit

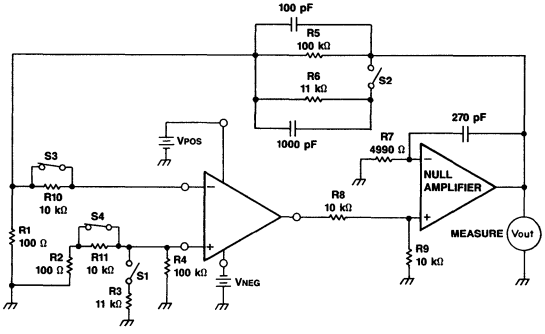


Figure 3. Input Bias and Input Offset Current Test Circuit

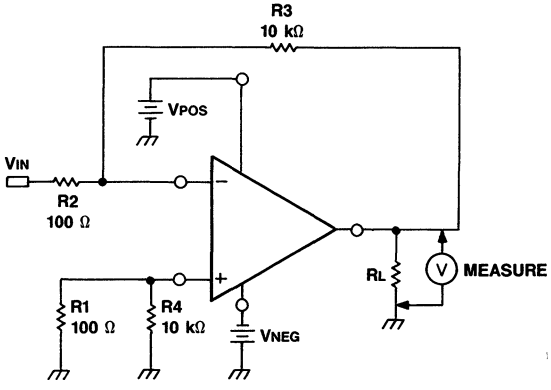


Figure 4. Output Voltage Swing Test Circuit

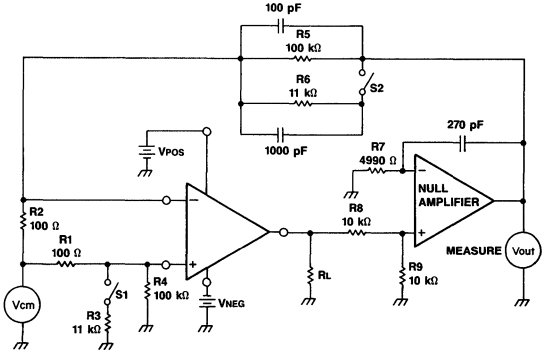


Figure 5. Common Mode Voltage Range and Common-Mode Rejection Ratio Test Circuit

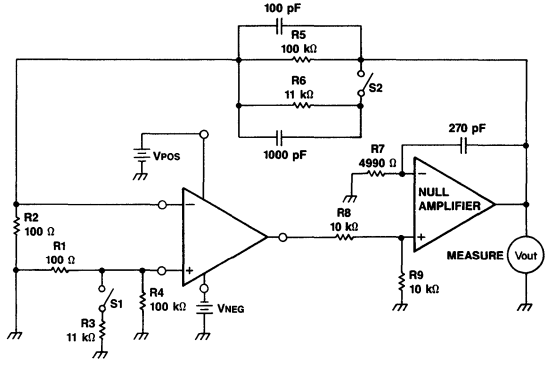


Figure 6. Power Supply Rejection Ratio Test Circuit

Test Circuits
(Continued)

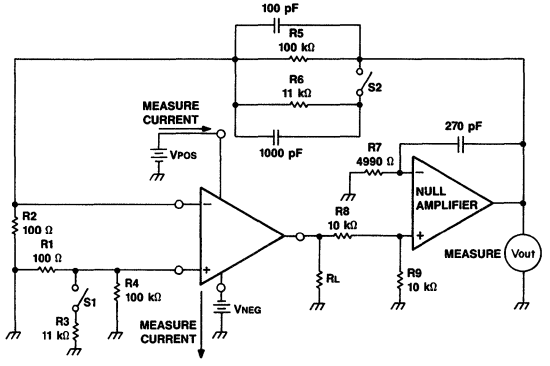


Figure 7. Power Supply Quiescent Current Test Circuit

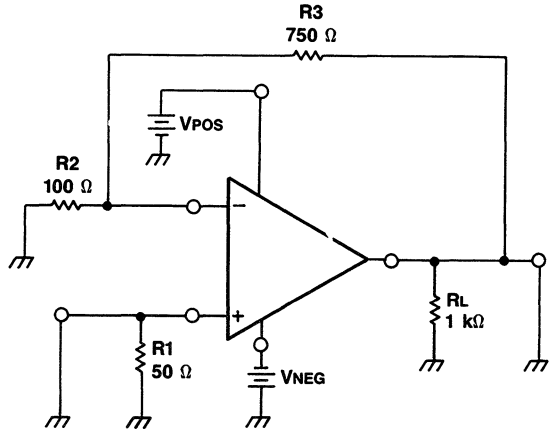


Figure 8. Slew Rate Test Circuit

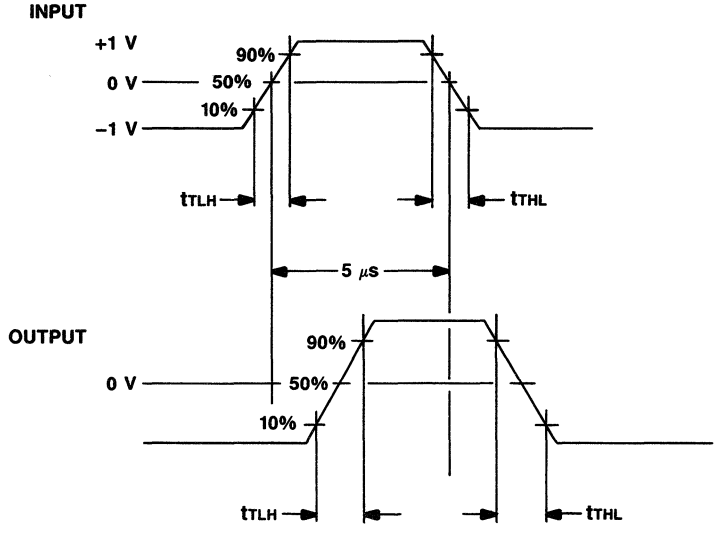


Figure 9. Slew Rate Test Circuit

Connector Options

These amplifiers are internally compensated and thus offer no compensation options.

The LB1029BC has offset null capability. This may be accomplished by placing a 2 kΩ potentiometer between the two offset null leads (leads 10 and 11 for amplifier A and leads 13 and 14 for amplifier B) with the wiper arm connected to the negative supply (lead 12). If offset null is not desired for either amplifier, leads 10, 11, 13 and 14 must be connected to lead 12.

Frequency Characteristics

At the unity gain crossover frequency, the typical phase margin is 70°. With internal compensation the normal 6 dB/octave roll-off is obtained. With this compensation, the amplifier configured as a unity gain amplifier will show little high-frequency peaking, and the step response will exhibit negligible overshoot or ringing.

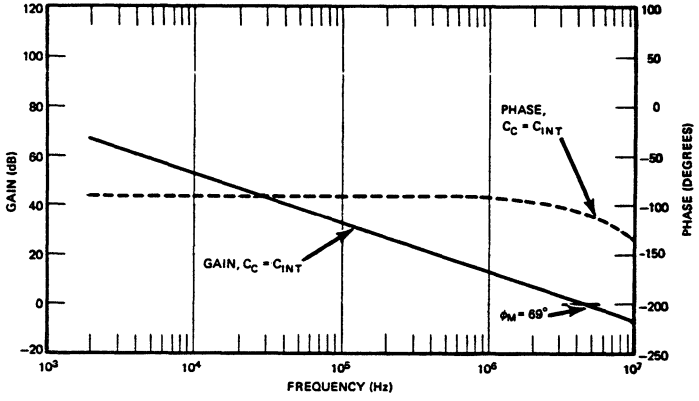
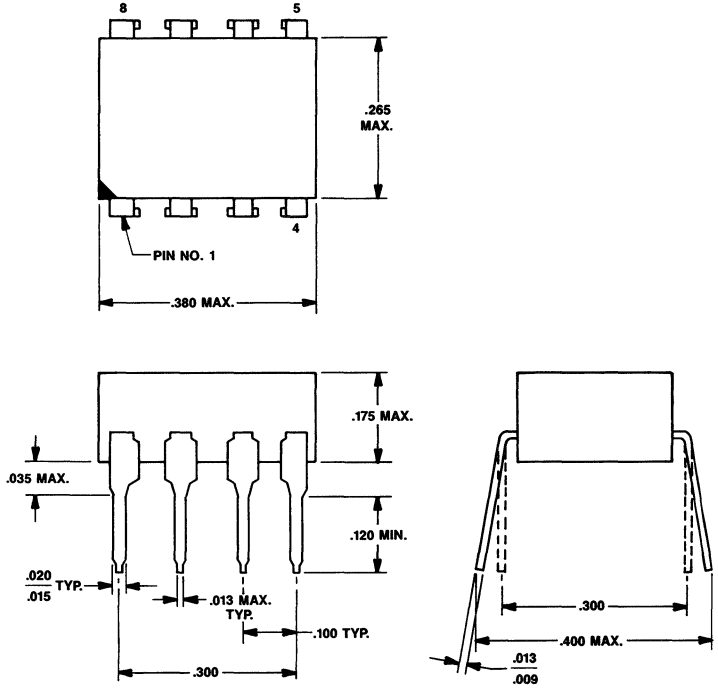


Figure 10. Gain and Phase vs. Frequency

Outline Drawings (Dimensions in Inches)

LB1029BB

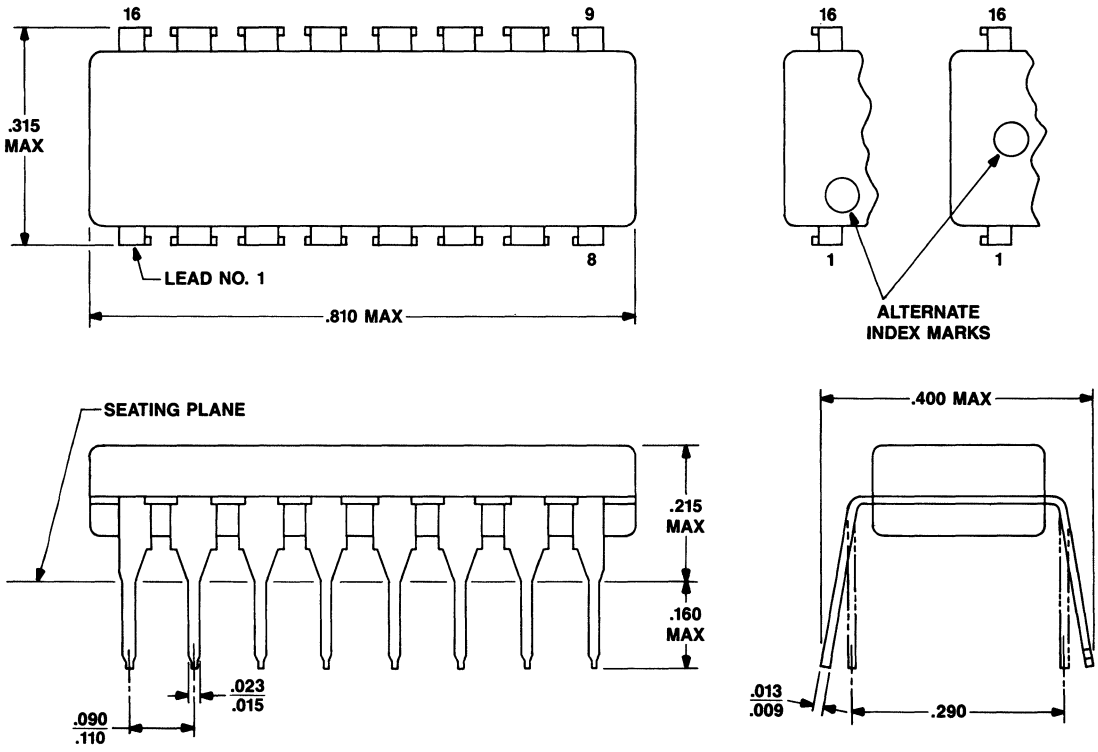


Note 1: Pin numbers are shown for reference only.

Outline Drawings (Continued)

(Dimensions in Inches)

LB1029BC



Note 1: Pin numbers are shown for reference only.

Ordering Information

Device	Comcode
LB1029BB	104368006
LB1029BC	104368014

Description

The LB1029CC is a dual operational amplifier with internal compensation for use in general-purpose applications where high slew rate is desired.

This device will provide a slew rate of 15 Vrms and approximately 50 dB improvement in RFI immunity (up to 100 MHz) as compared to standard voice-frequency amplifiers. It also features high-output current capability ($\geq \pm$ 15 mA), short-circuit protection, static-discharge protection, offset-voltage null capability, $f_T \geq$ 5.0 MHz, and a large common-mode voltage range. This integrated circuit will operate over the power-supply voltage range of $\pm$5.0 to $\pm$15 volts.

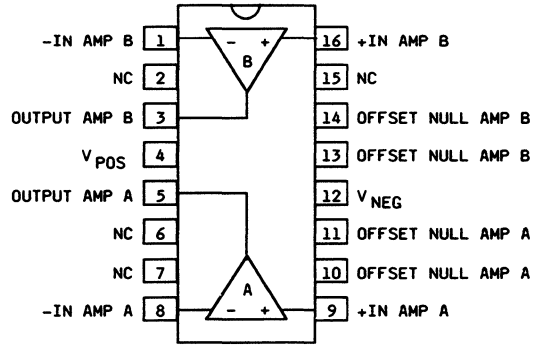
Features

- Minimum slew rate $\pm$ 15 V/μs guaranteed
- Unity gain frequency minimimum of 5.0 MHz
- Large common-mode voltage range
- 15 mA minimum output current capability
- Offset voltage null capability
- Short circuit current limited
- Offset voltage null capability
- RFI immunity typically 50 dB greater than LS1039BC
- 16-pin plastic DIP

Maximum Ratings (At 25°C unless otherwise specified)	
Voltage between V_S^+ and V_S^-	30 V
Voltage Between $-$IN and $+$IN of each Amplifier	$\pm$6.0 V
Power Dissipation	500 mW
Storage Temperature	$-$40 to $+$135°C
Operating Temperature	0 to $+$60°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Diagram



Pin Descriptions

Pin	Name/Function	Pin	Name/Function
1	Negative Input Amp B	9	Positive Input Amp A
2	No Connection①	10	Offset Null Amp A
3	Output Amp B	11	Offset Null Amp A
4	V_S^+	12	V_S^-
5	Output Amp A	13	Offset Null Amp B
6	No Connection①	14	Offset Null Amp B
7	No Connection①	15	No Connection①
8	Negative Input Amp A	16	Positive Input Amp B

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Parameter and Conditions	Min	Typ②	Max	Unit
Extrapolated Unity Gain Frequency⑤ (C_C = C_{INT})	5.0	8.0	12	MHz
Open-Loop Voltage Gain (Figure 1)	88	100	—	dB
Input Offset Voltage (Figure 2)	—	1.7	4.5	mV
Input Bias Current (Figure 3)	—	−0.7	−3.5	μA
Input Offset Current③ (Figure 3)		60	700	nA
Output Voltage Swing (Figure 4)	+12.5 −12.5	—	—	V_{peak}
Output Current Drive (R_L = 100 kΩ)⑤	+15 −15	+32 −32	+120 −120	mA
Common-Mode Voltage Range ($\triangle V_{IO}$ = 2.0 mV)	±13.4	—	—	V
Common-Mode Rejection Ratio (Figure 5)	86	100	—	dB
Power-Supply Rejection Ratio (Figure 6)	86	105	—	
Power-Supply Current④ (Figure 7)	—	4.5	6.1	mA
Slew Rate (Figures 8 and 9)	+15 −15	+21 −39	—	V/μs
Temperature Coefficient of Input Offset Voltage (−20°C to +80°C)⑤	—	12	—	μV/°C
Noise Voltage-C-Message Weighting ⑤	—	115	—	dBV
Differential Input Breakdown Voltage ⑤	±6.0	±8.5	—	V

① This lead is not internally connected and may be used as a tie point provided the maximum ratings of the device are not exceeded.
② Individual devices may differ significantly from the typical values shown.
③ This current may degrade if the differential input voltage exceeds ±6 V.
④ Total current for both amplifiers.
⑤ This condition is not tested in production devices.

Test Circuits

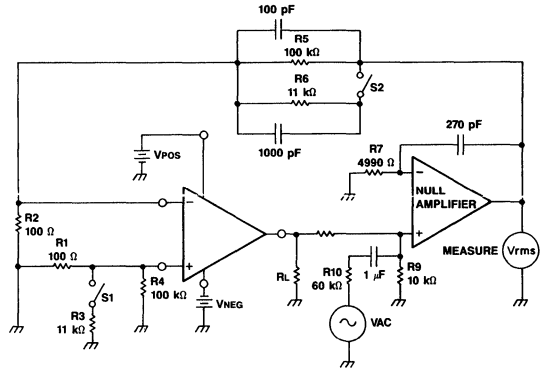


Figure 1. Open Loop Gain Test Circuit

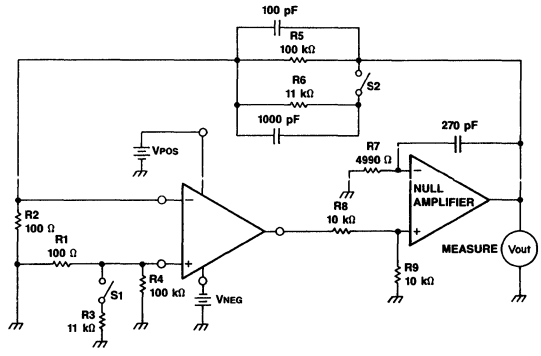


Figure 2. Input Offset Voltage (V_{IO}), Input Bias Current (I_{IB}), and Input Offset Current (I_{IO}) Test Circuit

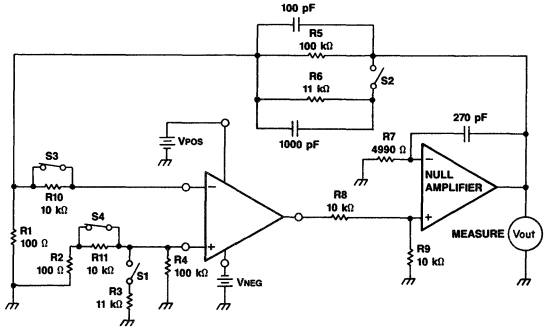


Figure 3. Input Bias and Input Offset Current Test Circuit

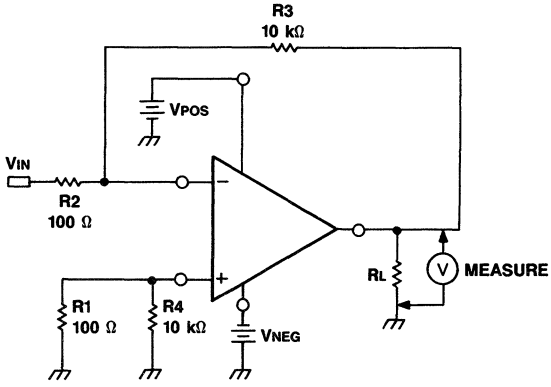


Figure 4. Output Voltage Swing Test Circuit

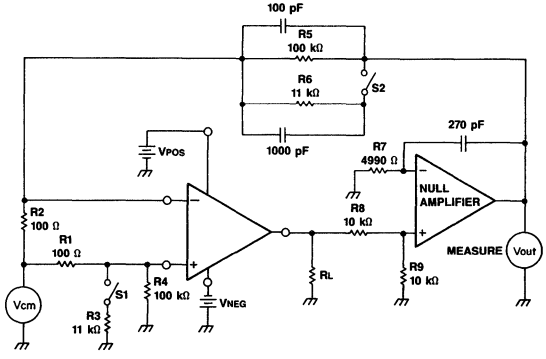


Figure 5. Common Mode Voltage Range and Common-Mode Rejection Ratio Test Circuit

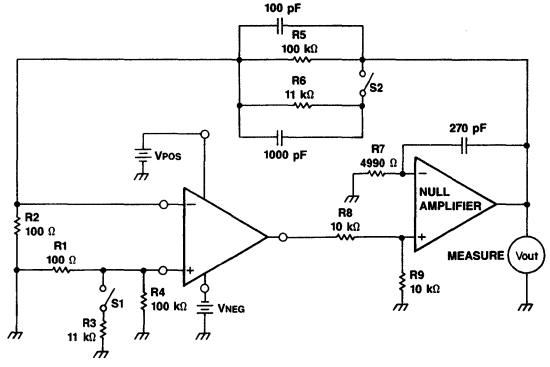


Figure 6. Power Supply Rejection Ratio Test Circuit

Test Circuits
(Continued)

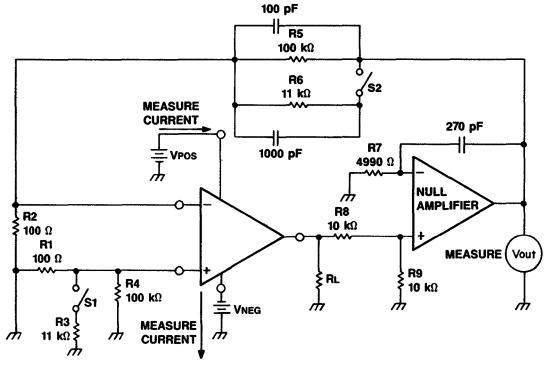


Figure 7. Power Supply Quiescent Current Test Circuit

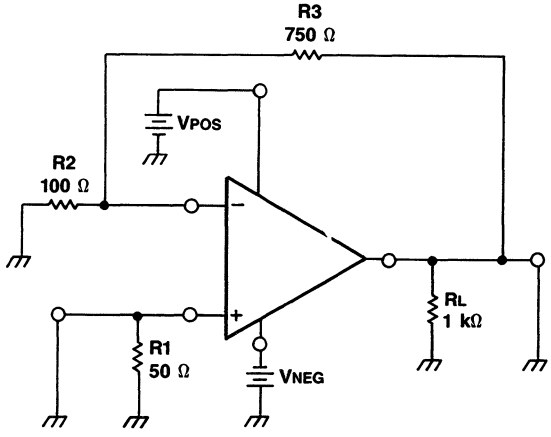


Figure 8. Slew Rate Test Circuit

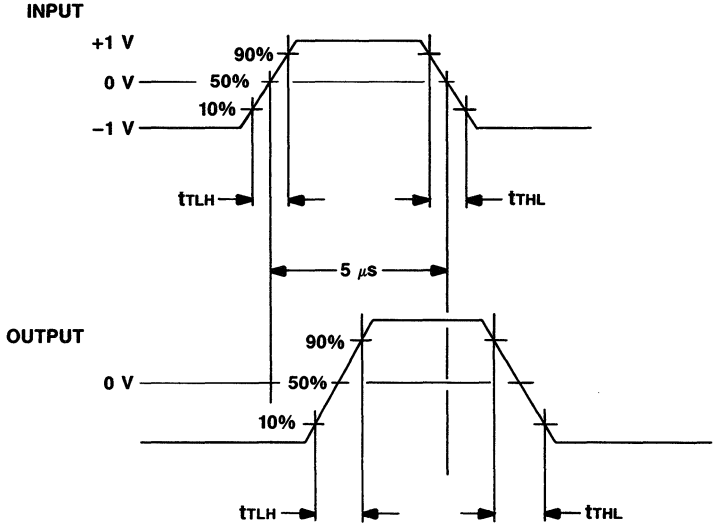


Figure 9. Slew Rate Test Circuit

Connection Options

This amplifier is internally compensated and thus offers no compensation options.

Offset null may be accomplished on the LB1029CC only by placing a 2 kΩ potentiometer between the two offset null leads (leads 10 and 11 for amplifier A and leads 13 and 14 for amplifier B) with the wiper arm connected to the negative supply (lead 12). If offset null is not desired for either amplifier, leads 10, 11, 13 and 14 must be connected to lead 12.

Frequency Characteristics

At the unity gain crossover frequency, the typical phase margin is 69°. With internal compensation the normal 6 dB/octave roll-off is obtained. With this compensation, the amplifier configured as a unity gain amplifier will show little high-frequency peaking, and the step response will exhibit negligible overshoot or ringing.

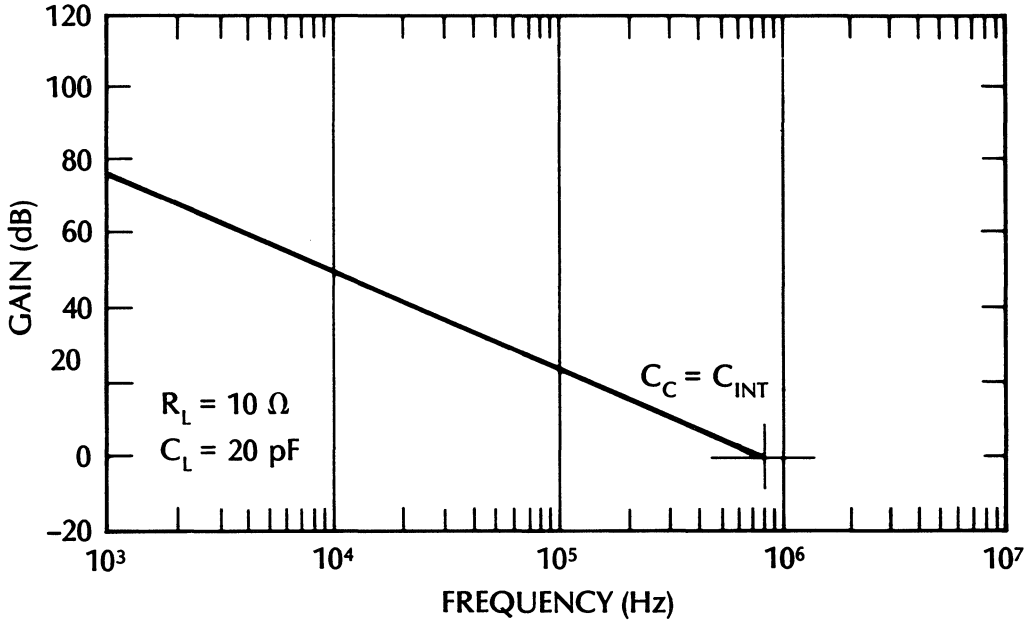
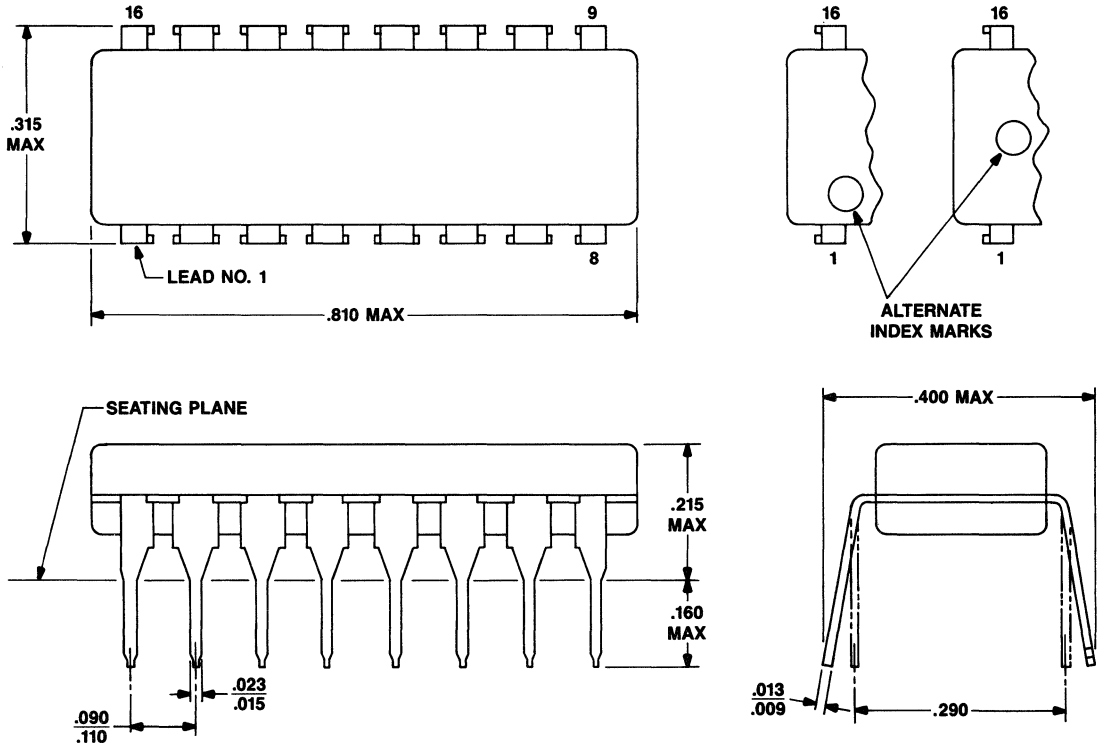


Figure 10. Gain and Phase vs. Frequency

Outline Drawing

(Dimensions in Inches)



Note 1: Pin Numbers are shown for reference only.

Ordering Information

Device	Comcode
LB1029CC	104368022

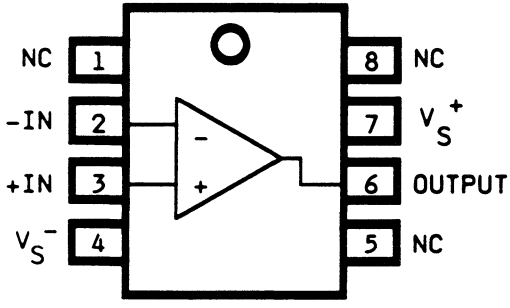
Description

The LB1030AB functions as a voice-frequency operational amplifier and is intended for general purpose use where internal "T" compensation is desired. This device features good output current capability, short circuit protection, static discharge protection, and large common-mode voltage range. The differential voltage range is limited to ±6.0 volts. The LB1030AB will operate over the power-supply range of ±5.0 to ±15 volts.

Features

- Minimum unit-gain frequency of 3 MHz
- Internal "T" compensation
- 0.5 V/μs typical slew rate
- Large common-mode voltage range
- 12 mA minimum output current capability
- Short circuit current limited
- Static discharge protection
- Supply range voltage: ±5 to ±15 volts
- Differential-mode voltage range: ±6 volts
- 8-pin plastic DIP

Pin Diagram



Maximum Ratings (At 25°C unless otherwise specified)	
Supply Voltage Range	30 V
Differential Mode Input Voltage (−IN to +IN)	±6.0 V
Power Dissipation	400 mW
Storage Temperature Range	−40 to +125°C
Ambient Operating Temperature Range	0 to +60°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic and Test Condition	Symbol	Min	Typ①	Max	Unit
Test Condition Supply Voltage	V_S	±15	±15	±15	V
Extrapolated Unity Gain Frequency② (f = 1.0 kHz, $C_C = C_{INT}$)	f_T	3.0	4.5	7.0	MHz
Open-Loop Voltage Gain (Figure 1) (f = 100 Hz, C_C = 0)	A_{VOL}	70	73	77	dB
Input Offset Voltage (Figure 2)	$\|V_{IO}\|$	—	0.5	3.0	mV
Input Bias Current (Figure 3)	i_{IB}	—	75	250	nA
Input Offset Current (Figure 3)	$\|I_{IO}\|$	—	5.0	50	nA
Output Voltage Swing (R_L = 10 kΩ)(Figure 4)	V_{OM}	+13.0 −13.8	+13.5 −14.2	—	V(peak)
Output Current Drive (R_L = 200 Ω)②	I_O	+12 −12	+31 −27	+40 −40	mA
Common-Mode Voltage Range ($\triangle V_{IO}$ = 2.0 mV)	CMVR	+12.5 −14.0	+14.1 −14.5	—	V
Common-Mode Rejection Ratio (Figure 5)	CMRR	86	105	—	dB
Power-Supply Rejection Ratio (V_S = ±5 to ±15 V) (Figure 6)	$\|PSRR(\pm)\|$	—	3.0	50	μV/V
Power-Supply Current③ (Figure 7)	I_{PS}	0.6	1.0	1.5	mA
Differential Input Breakdown Voltage②	$V_{(BR)II}$	±6.0	±8.5	—	V
Slew Rate ($C_C = C_{INT}$)② (Figures 8 and 9)	SR	—	0.5	—	V/μs

① Individual devices may differ significantly from the typical values shown.
② This condition is not tested in production devices.

Test Circuits

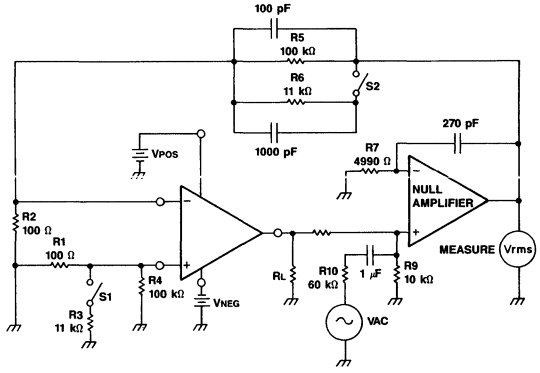


Figure 1. Open Loop Gain Test Circuit

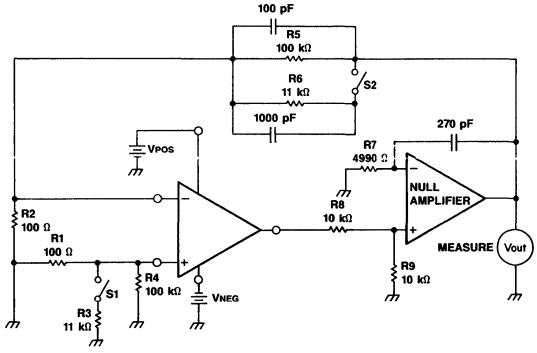


Figure 2. Input Offset Voltage (V_{IO}), Input Bias Current (I_{IB}), and Input Offset Current (I_{IO}) Test Circuit

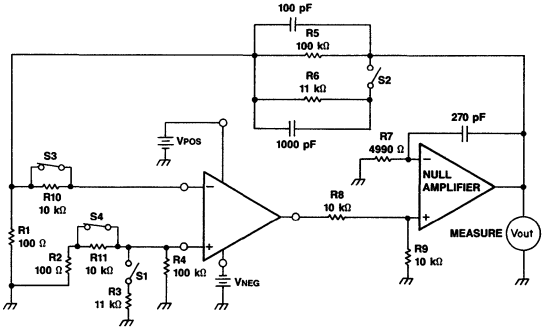


Figure 3. Input Bias and Input Offset Current Test Circuit

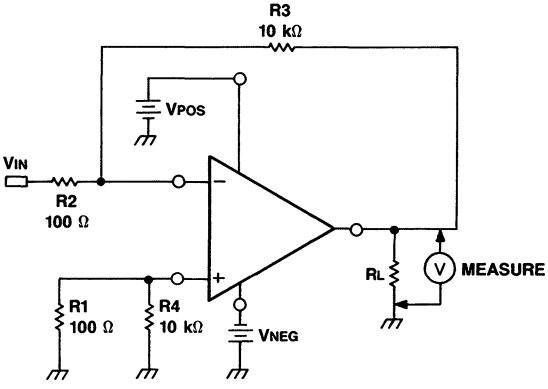


Figure 4. Output Voltage Swing Test Circuit

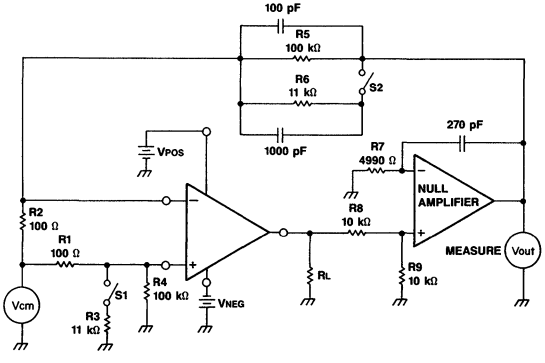


Figure 5. Common Mode Voltage Range and Common-Mode Rejection Ratio Test Circuit

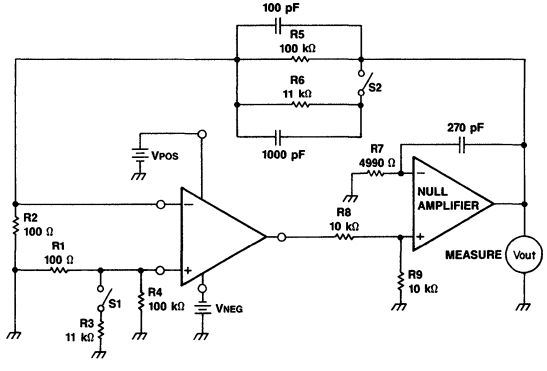


Figure 6. Power Supply Rejection Ratio Test Circuit

Test Circuits (Continued)

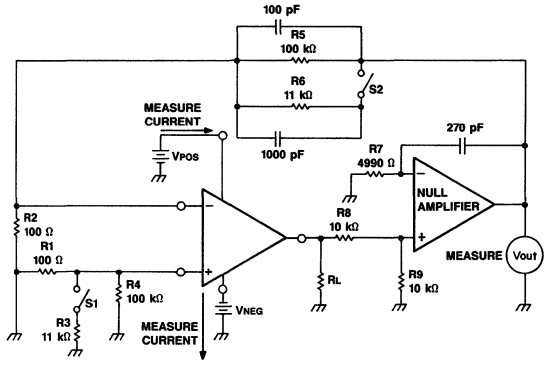


Figure 7. Power Supply Quiescent Current Test Circuit

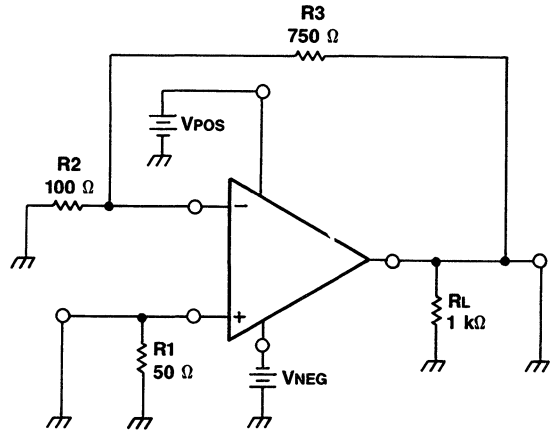


Figure 8. Slew Rate Test Circuit

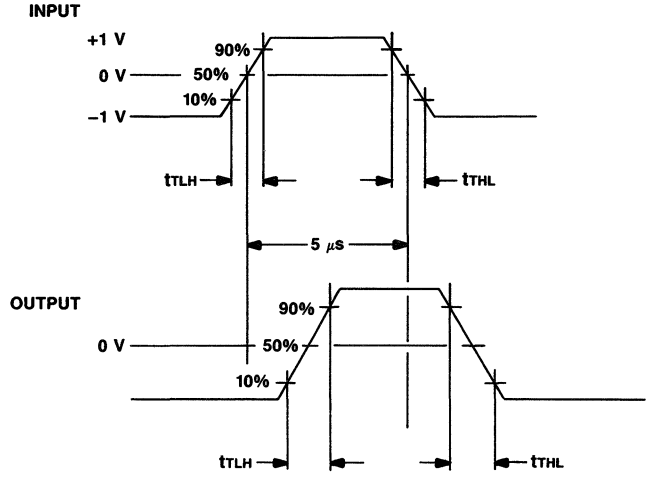


Figure 9. Slew Rate Test Circuit

Connection Options

This amplifier is internally compensated and offers no compensation options. It is designed for use with internal "T" compensation and provides high gain over the voice frequency bandwidth.

A "T" compensated amplifier will exhibit considerable peaking for closed loop gains greater than 20 dB. Typical open-loop gain and phase relationships are shown in the Frequency Characteristics section.

Capacitive loading (C_L) coupled with the high-frequency output resistance (R_O) of the amplifier will add a pole to the open-loop response at $f = \frac{1}{2}\pi R_O C_O$. For "T" compensated amplifiers, this added pole can cause oscillation for C_L greater than 200 pF. Isolating the capacitor from the output of the amplifier and the feedback loop with about 50 ohms will insure stability.

Frequency Characteristics

The internal "T" compensation can achieve high open-loop gain over the voice-frequency bandwidth. Double-pole, single-zero roll-off is obtained as shown. At unity gain, the phase margin is about 50 degrees, and a slight amount of high-frequency (5.0 MHz) peaking may occur. Closed-loop gains near 20 dB will experience peaking since the closed-loop gain intersects the open-loop response near or on the 12 dB/octave slope. For closed-loop gains above 20 dB, the peaking will exceed 3.0 dB. Furthermore, the double-pole, single-zero roll-off may introduce potentially undesirable features in the step response. However, "T" compensation does have the advantage of greater than 70 dB of open-loop gain over the voice-frequency bandwidth.

The power-supply rejection and common-mode rejection are expected to have frequency dependence similar to the open-loop gain. Thus, at 10 kHz, a "T" compensated amplifier will have better power-supply rejection and common-mode rejection than a feedback-compensated amplifier. At dc or very low frequency, there will be no significant difference.

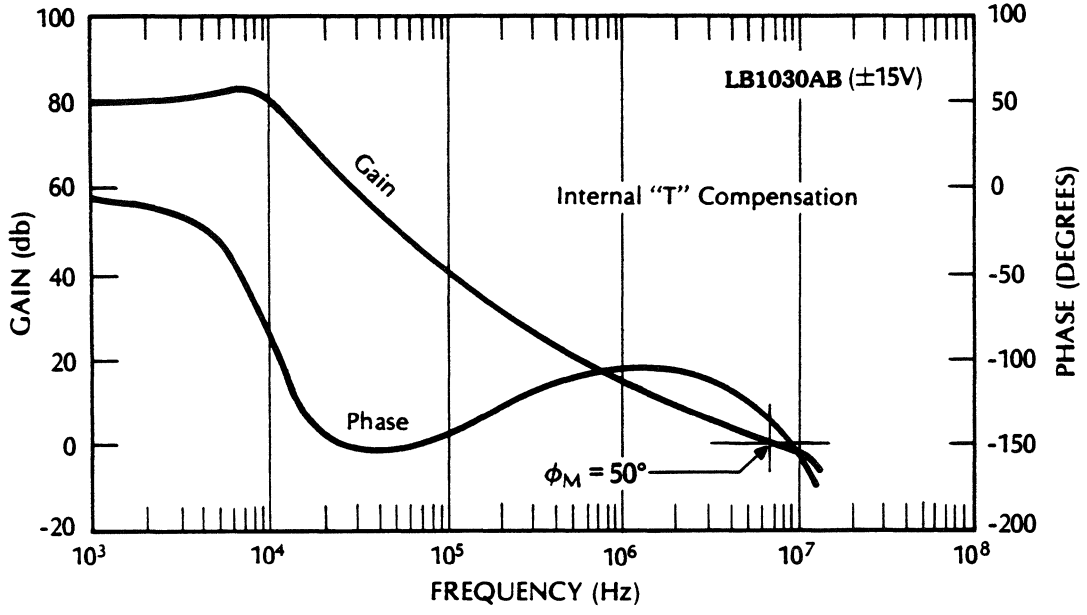
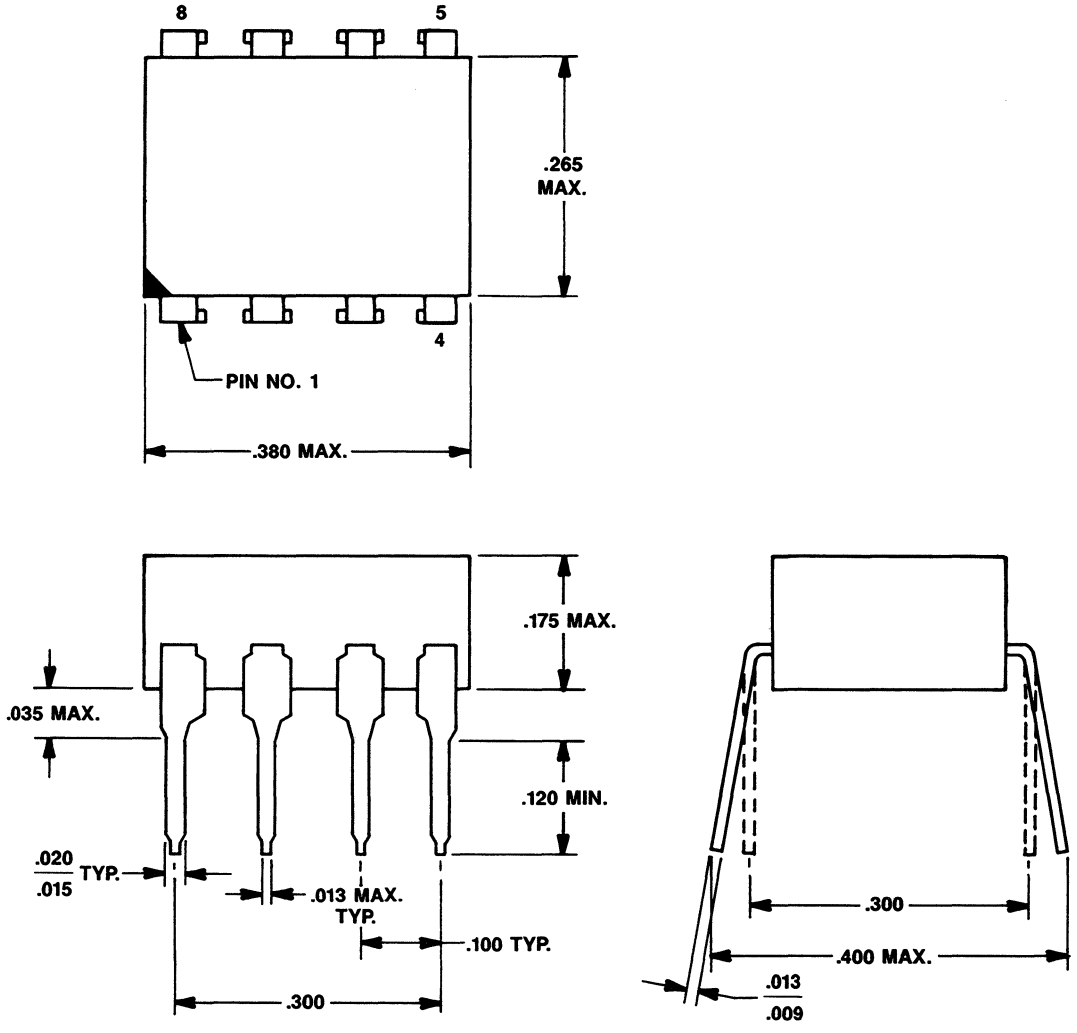


Figure 10. Typical Gain and Phase vs. Frequency

Outline Drawing

(Dimensions in Inches)



Note 1: Pin numbers are shown for reference only.

Ordering Information

Device	Comcode
LB1030AB	104368030

Description

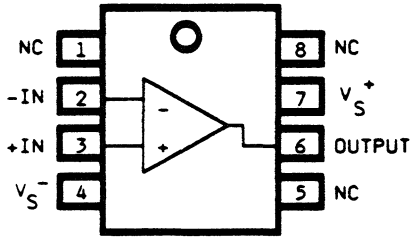
The LB1031AB/AC functions as a voice-frequency operational amplifier and is intended for general-purpose use where internal compensation is desired. This device features good output current capability, short circuit protection, static discharge protection, and large common-mode voltage range. The differential voltage range is limited to ±6.0 volts. This
device will operate over the power-supply range of ±5.0 to ±15 volts. The LB1031AC features an offset null adjustment.

Features

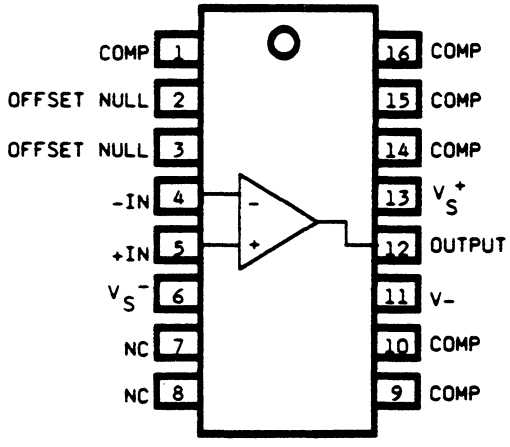
- Guaranteed minimum unity-gain frequency of 4.0 MHz
- 5.0 V/μs typical slew rate
- Large common-mode voltage range
- 12 mA minimum output current capability
- Offset voltage null capability (LB1031AC)
- Short circuit current limited
- Internal "T" compensation (LB1031AB)
- Optional internal "T" or feedback compensation (LB1031AC)
- Static discharge protection
- Supply range voltage: ±5.0 to ±15 volts
- Differential-mode voltage range: ±6.0 volts
- 8- or 16-pin plastic DIP

Pin Diagrams

LB1031AB



LB1031AC



Maximum Ratings (At 25°C unless otherwise specified)	
Supply Voltage Range (V_S^+ and V_S^-)	30 V
Differential Mode Input Voltage (+IN to −IN)	±6.0 V
Power Dissipation	400 mW
Storage Temperature Range	−40 to +125°C
Ambient Operating Temperature Range	0 to +60°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic and Test Condition	Symbol	Min	Typ①	Max	Unit
Test Condition Supply Voltage	V_S	±15	±15	±15	V
Extrapolated Unity Gain Frequency② (f = 1.0 kHz, C_C = C_{INT})	f_T	4.0	5.6	9.0	MHz
Open-Loop Voltage Gain (Figure 1) (f = 100 Hz, C_C = 0)	A_{VOL}	72	75	79	dB
Input Offset Voltage (Figure 2)	$\lvert V_{IO}\rvert$	—	0.5	4.5	mV
Input Bias Current (Figure 3)	I_{IB}	—	800	3500	nA
Input Offset Current (Figure 3)	$\lvert I_{IO}\rvert$	—	40	700	nA
Output Voltage Swing (R_L = 10 kΩ) (Figure 4)	V_{OM}	+13.0 −13.8	+13.5 −14.2	—	V(peak)
Output Current Drive (R_L = 200 Ω)②	I_O	+12 −12	+31 −27	+40 −40	mA
Common-Mode Voltage Range (△ = 2.0 mV)	CMVR	+12.5 −14.0	+14.1 −14.5	—	V
Common-Mode Rejection Ratio (Figure 5)	CMRR	86	105	—	dB
Power-Supply Rejection Ratio (±5 to ±15 V)(Figure 6)	$\lvert PSRR(\pm)\rvert$	—	3.0	50	μV/V
Power-Supply Current (Figure 7)	I_{PS}	0.8	1.1	1.7	mA
Differential Input Breakdown Voltage	$V_{(BR)II}$	±6.0	±8.5	—	V
Slew Rate (C_C = C_{INT})② (Figures 8 and 9)	SR	—	5.0	—	V/μs

① Individual devices may differ significantly from the typical values shown.
② This condition is not tested in production devices.

Test Circuits

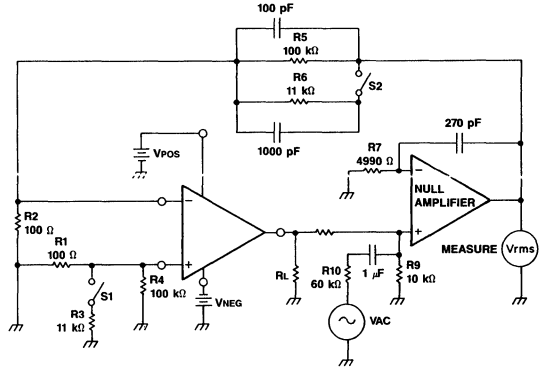


Figure 1. Open Loop Gain Test Circuit

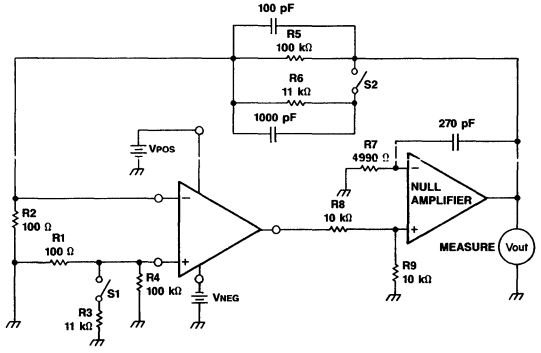


Figure 2. Input Offset Voltage (V_{IO}), Input Bias Current (I_{IB}), and Input Offset Current (I_{IO}) Test Circuit

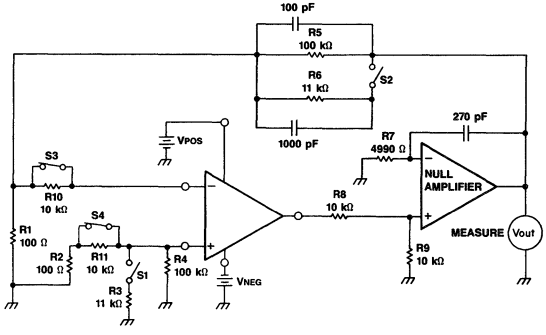


Figure 3. Input Bias and Input Offset Current Test Circuit

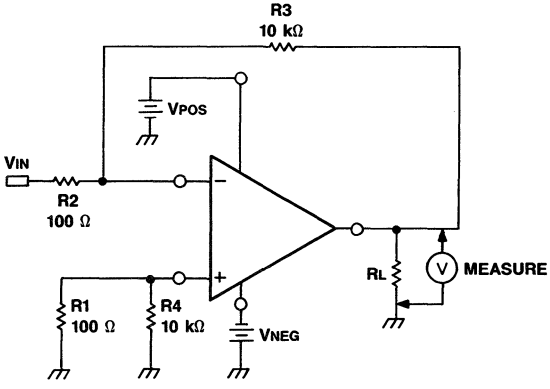


Figure 4. Output Voltage Swing Test Circuit

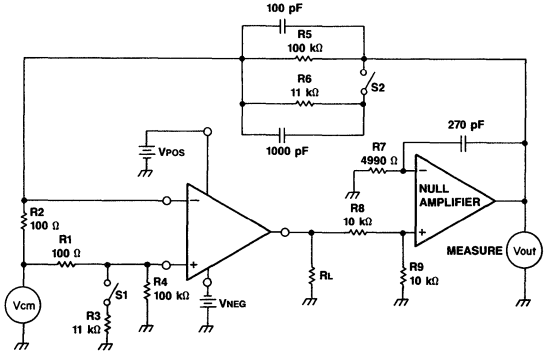


Figure 5. Common Mode Voltage Range and Common-Mode Rejection Ratio Test Circuit

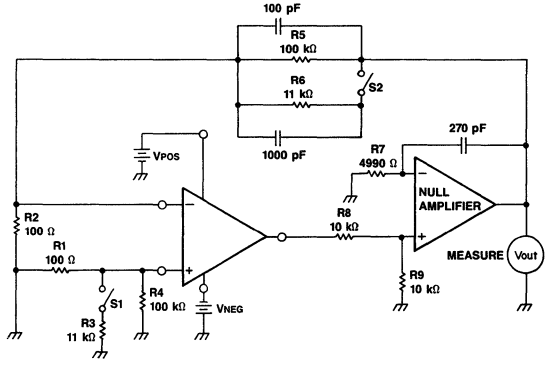


Figure 6. Power Supply Rejection Ratio Test Circuit

Test Circuits
(Continued)

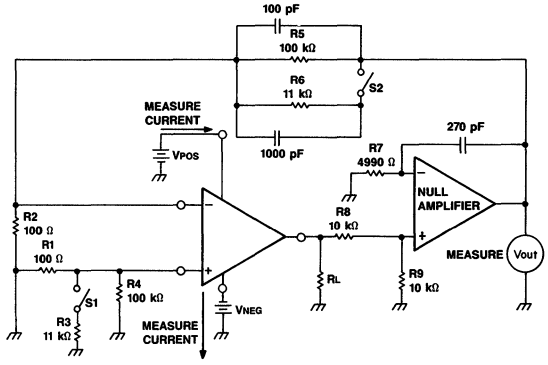


Figure 7. Power Supply Quiescent Current Test Circuit

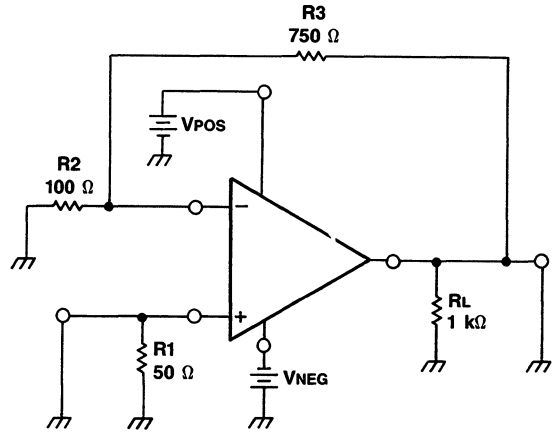


Figure 8. Slew Rate Test Circuit

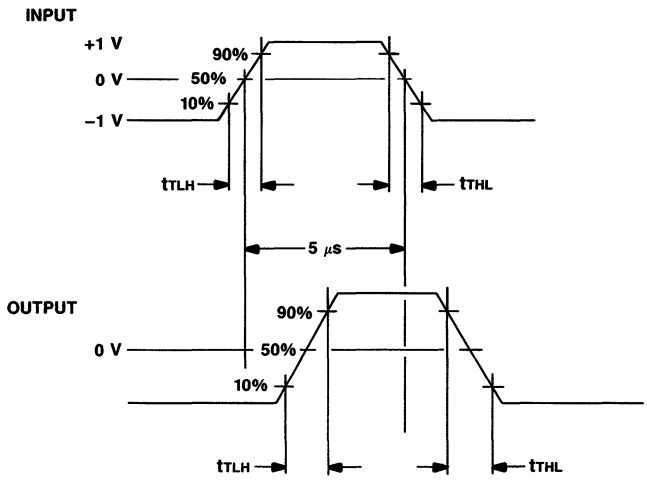


Figure 9. Slew Rate Test Circuit

Connector Options

These amplifiers are internally compensated and thus offer no compensation options.

The LB1029BC has offset null capability. This may be accomplished by placing a 2 kΩ potentiometer between the two offset null leads (leads 10 and 11 for amplifier A and leads 13 and 14 for amplifier B) with the wiper arm connected to the negative supply (lead 12). If offset null is not desired for either amplifier, leads 10, 11, 13 and 14 must be connected to lead 12.

LB1031AB Connection Options

This amplifier is internally compensated and offers no compensation options. It is designed for use with internal "T" compensation and provides high gain over the voice frequency bandwidth.

A "T" compensated amplifier will exhibit considerable peaking for closed loop gains greater than 20 dB. Typical open-loop gain and phase relationships are shown in the Frequency Characteristics section.

Capacitive loading (C_L), coupled with the high-frequency output resistance (R_O) of the amplifier, will add a pole to the open-loop response at $f = \frac{1}{2\pi R_O C_L}$. For a "T" compensated amplifier, this added pole can cause oscillation for C_L greater than 200 pF. Isolating the capacitor from the output of the amplifier and the feedback loop with about 50 ohms will insure stability.

LB1031AC Connection Options

The diagrams show various connection options. Combinations of the options are, of course, possible.

Figure 10 shows connections for the basic circuit operation with internal "T" compensation and no offset null. Offset null may be accomplished by placing a 200 ohm potentiometer between leads 2 and 3 with the wiper arm connected to the positive supply (Figure 12).

Three internal and one external compensation options are shown. This amplifier is designed for use with "T" compensation to provide high gain over the voice frequency bandwidth. A "T" compensated amplifier will exhibit considerable peaking for closed-loop gains greater than 20 dB.

Internal feedback compensation (Figure 11) provides 6 dB/octave roll-off with reduced bandwidth ($f_T \geq 2$ MHz) and increased phase margin. Increased bandwidth ($f_T \geq 4$ MHz) is obtained with an external resistor (Figure 12) or with external compensation (Figure 13).

Capacitive loading (C_L), coupled with the high-frequency output resistance (R_O) of the amplifier, will add a pole to the open-loop response at $f = \frac{1}{2\pi R_O C_L}$. For "T" compensated amplifiers, this added pole can cause oscillation for C_L greater than 200 pF. Isolating the capacitor from the output of the amplifier and the feedback loop with about 50 ohms will insure stability. The internal feedback compensation, with its improved phase margin and lower bandwidth, may also be used to insure stability with capacitive loading.

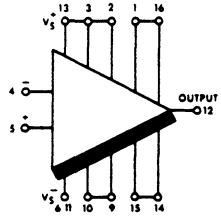


Figure 10. 1031AC No Offset Null Internal "T" Compensation

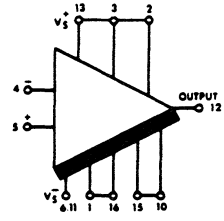


Figure 11. 1031AC No Offset Null Internal Feedback Compensation

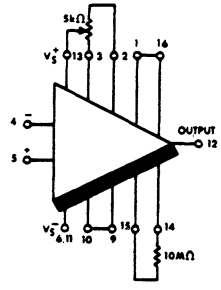


Figure 12. 1031AC Offset Null Feedback Compensation

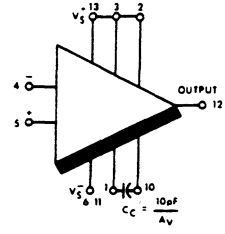


Figure 13. 1031AC No Offset Null External Compensation

Frequency Characteristics

With internal feedback compensation, the normal 6.0 dB/octave roll-off is obtained (Figure 14, Curve I). With this compensation, a unity gain amplifier will show no high-frequency peaking and the step response will exhibit no overshoot or ringing. However, open-loop gain at the upper edge of the voiceband (3.5 kHz) is only about 55 dB. For some applications, at least 70 dB open-loop gain at 3.5 kHz is desired.

The internal "T" compensation can achieve high open-loop gain over the voice-frequency bandwidth. Double-pole, single-zero roll-off is obtained as shown. At unity gain, the phase margin (Figure 14) is about 50 degrees, and a slight amount of high-frequency (5.0 MHz) peaking may occur. Closed-loop gains near 30 dB will experience peaking since the closed-loop gain intersects the open-loop response near or on the 12 dB/octave slope. For closed-loop gains above 20 dB, the peaking will exceed 3.0 dB. Furthermore, the double-pole, single-zero roll-off may introduce potentially undesirable features in the step response. However, "T" compensation does have the advantage of greater than 70 dB of open-loop gain over the voice-frequency bandwidth.

The power-supply rejection and common-mode rejection are expected to have frequency dependence similar to the open-loop gain. Thus, a 10 kHz, "T" compensated amplifier will have better power-supply rejection and common-mode rejection than a feedback compensated amplifier. At dc or very low frequency, there will be no significant difference.

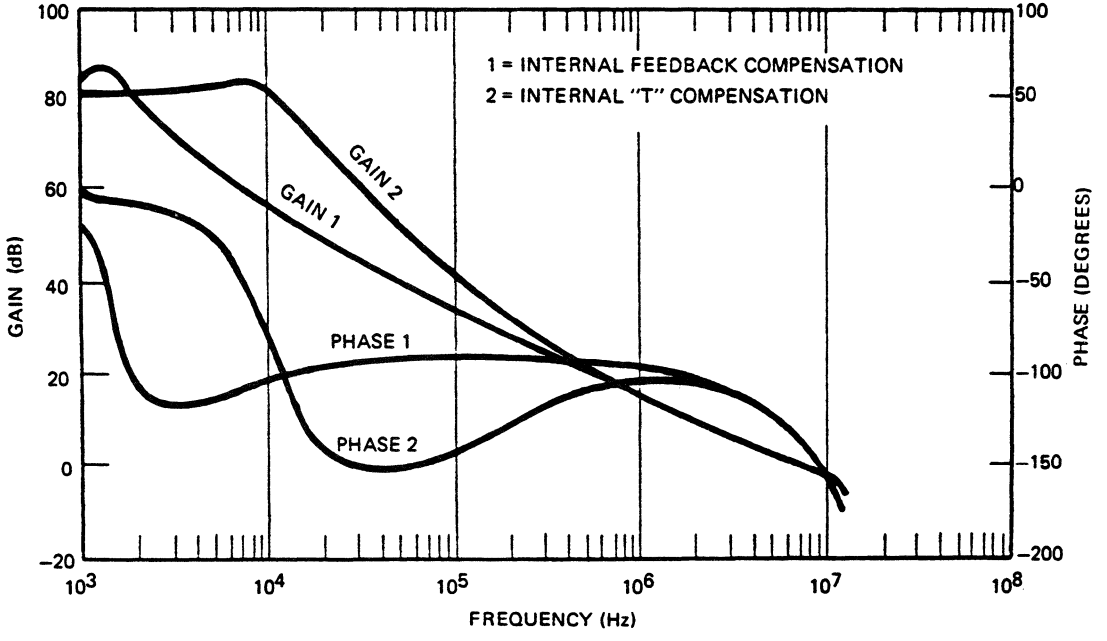
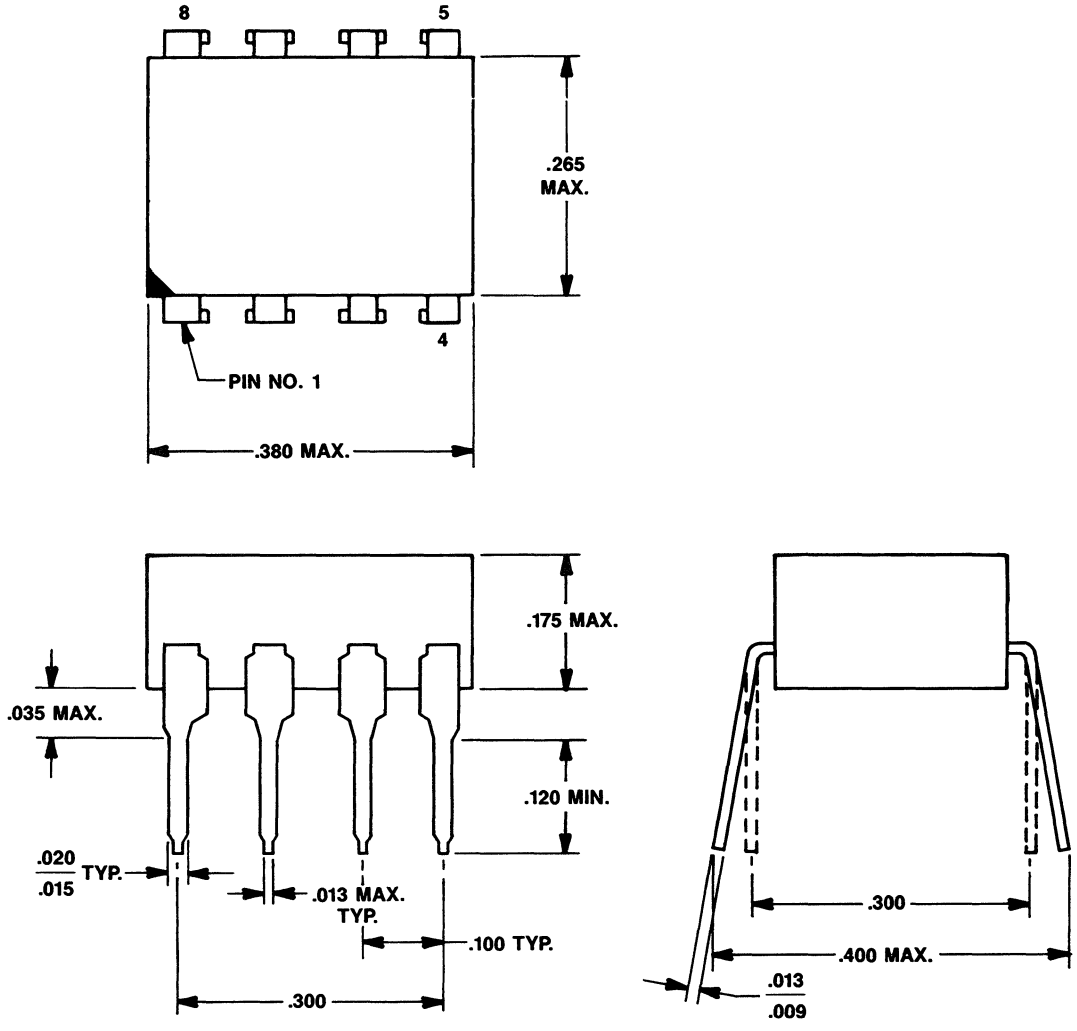


Figure 14. Gain and Phase vs. Frequency

Outline Drawings

(Dimensions in Inches)

LB1031AB

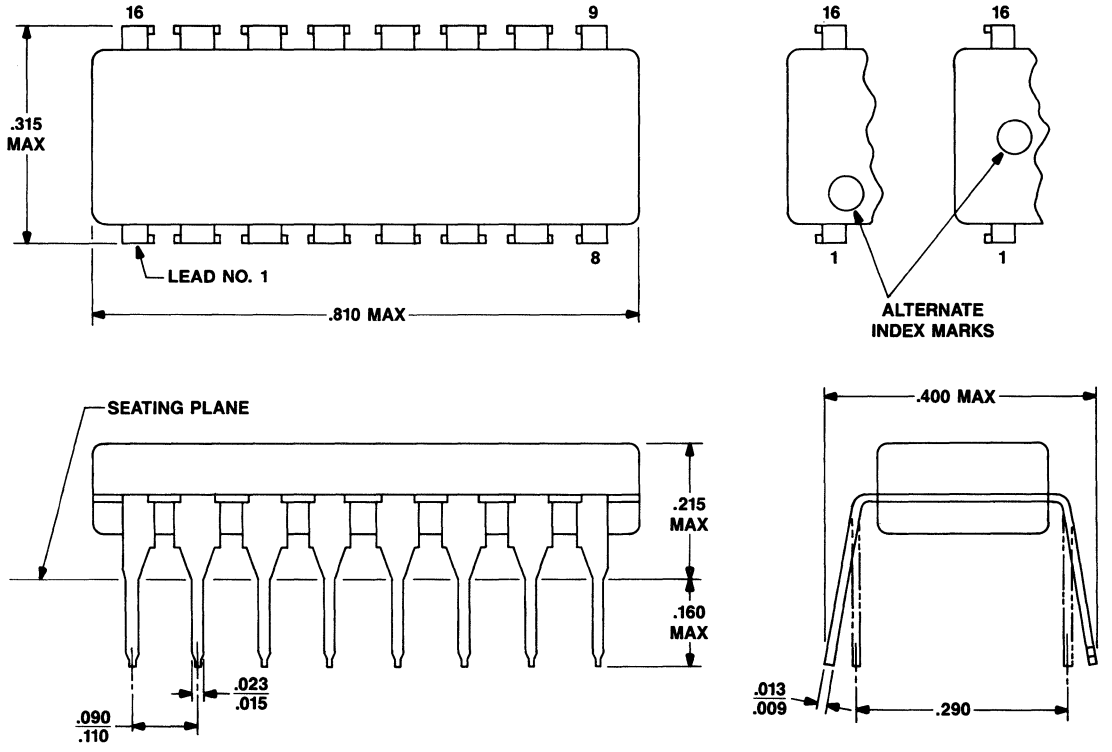


Note 1: Pin numbers are shown for reference only.

Outline Drawings (Continued)

(Dimensions in Inches)

LB1031AC



Note 1: Pin numbers are shown for reference only.

Ordering Information

Device	Comcode
LB1031AB	104368055
LB1031AC	104368063

GENERAL-PURPOSE PROGRAMMABLE MEDIUM POWER OUTPUT OP-AMP

LB1032AC

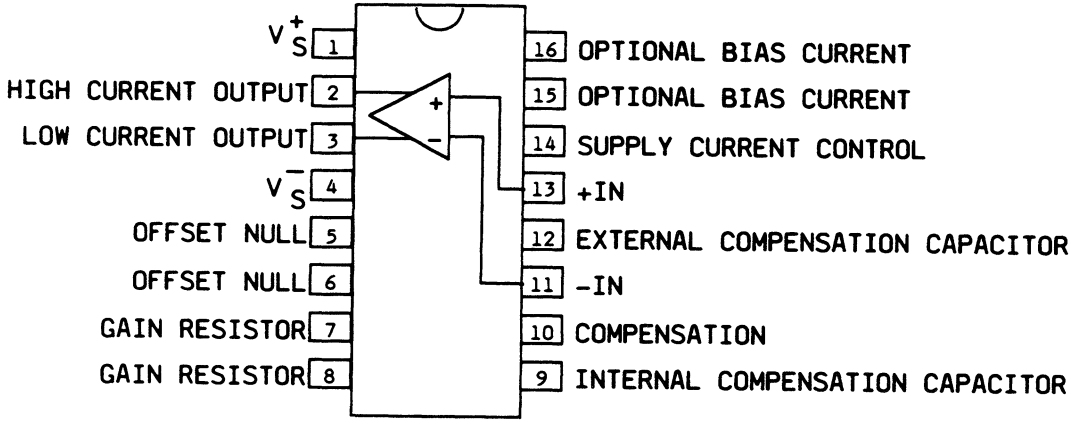
Description

The LB1032AC is a programmable internally compensated medium-power operational amplifier. Maximum supply voltage is ±7.0 V and output current is ±77 mA into a 45 Ω load. Optional bias control, external compensation, offset nulling, and a low-current, higher frequency output are also provided.

Features

- 80 mA minimum output current capability
- Guaranteed minimum unity-gain frequency of 2.5 MHz
- Offset voltage null capability
- 1.5 V/μs typical slew rate
- Optional internal or external compensation
- Supply voltage range: ±3.0 to ±7.0 volts
- Differential-mode voltage range: ±6.5 volts
- 16-pin plastic DIP

Pin Diagram



Maximum Ratings (At 25°C unless otherwise specified)	
Ambient Operating Temperature Range	0 to +60°C
Storage Temperature Range	−40 to +125°C
Supply Voltage Range (V_S^+ to V_S^-)	14 V
Differential Mode Input Voltage (+IN to −IN)	±6.5 V
Total Power Dissipation	500 mW

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Electrical Characteristics (T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic and Test Condition			Symbol	Min①	Typ②	Max①	Unit
Open Loop Voltage Gain (Figure 1) (F = 100 Hz, R_L = 10 kΩ, C_C = 0) (F = 1000 Hz, R_L = 10 kΩ, C_C = C_{INT})			A_{VOL}	87 69	95 72	— 80	dB
Closed Loop Voltage Gain③ (R_L = 45 Ω)			A_{VCL}	2.5	2.8	3.5	dB
Input Offset Voltage (Figure 2) (R_L = 10 kΩ, V_S = 3.0 V) (R_L = 10 kΩ, V_S = ±7.0 V)			$\lvert V_{IO}\rvert$	—	0.9	10	mV
Input Bias Current (Figure 3) (R_L = 10 kΩ, V_S = ±7.0 V)			I_{IB}	0	0.4	1.5	μA
Input Offset Current (Figure 3) (R_L = 10 kΩ, V_S = ±7.0 V)			$\lvert I_{IO}\rvert$	—	35	500	nA
Output Voltage Swing (Figure 4)	Low Current Output	R_L = 10 kΩ	V_{OM}	+4.5 −4.4	+4.8 −4.8	—	V(peak)
		R_L = 180 Ω		+3.7 −3.7	+4.1 −4.1	—	
	High Current Output	R_L = 10 kΩ		+4.4 −4.3	+4.7 −4.6	—	
		R_L = 45 Ω		+3.5 −3.5	+3.7 −3.7	—	
Common-Mode Voltage Range (△V_{IO} = 2.0 mV, V_S = ±7.0 V, R_L = 10 kΩ)			CMVR	+5.5 −5.5	—	—	V
Power-Supply Rejection Ratio (V_S = ±3 to ±7.0 V)(Figure 5)			$\lvert PSRR(\pm)\rvert$	—	30	200	μV/V
Power-Supply Current (V_S = ±7.0 V, R_L = 10 kΩ)(Figure 7)			I_{PS}	—	+3.2 −2.6	+5.3 −5.3	mA

① Max/Min values are guaranteed specification limits at worst case supply conditions.
② Typical values are characteristics at optimum power-supply voltage conditions. Individual devices may differ significantly from the typical values shown.
③ Lead 7 = ground; lead 13 = +IN; lead 2 connected to lead 8.
④ This condition is not tested in production devices.

Test Circuits

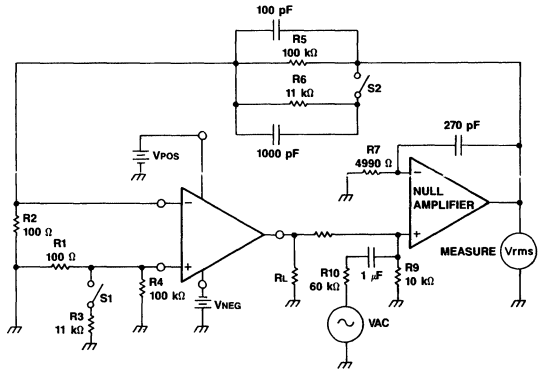


Figure 1. Open Loop Gain Test Circuit

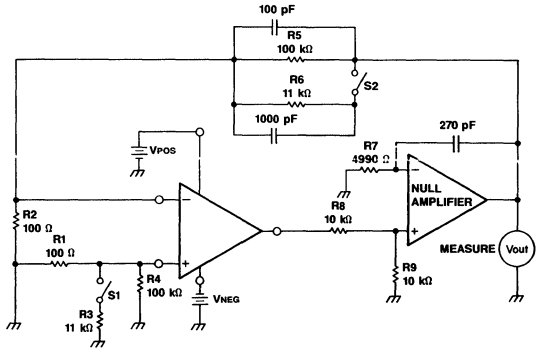


Figure 2. Input Offset Voltage (V_{IO}), Input Bias Current (I_{IB}), and Input Offset Current (I_{IO}) Test Circuit

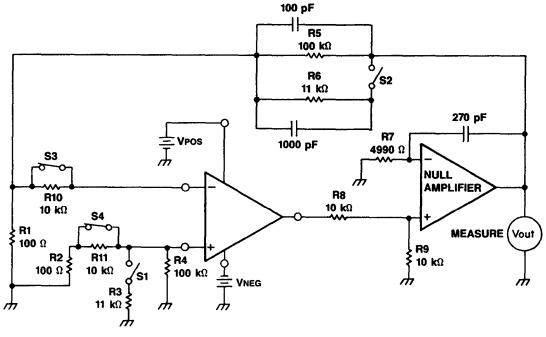


Figure 3. Input Bias and Input Offset Current Test Circuit

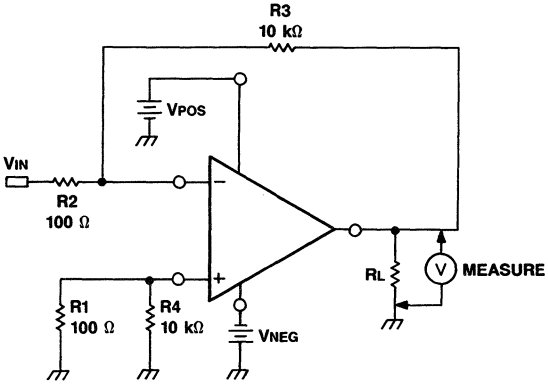


Figure 4. Output Voltage Swing Test Circuit

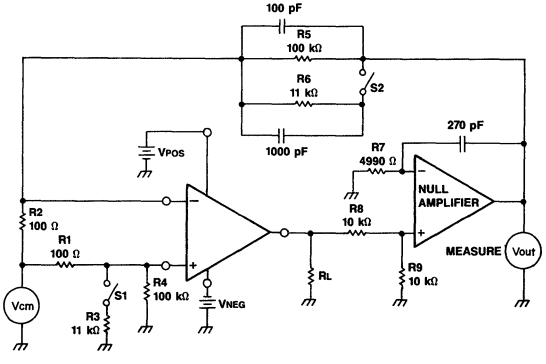


Figure 5. Common Mode Voltage Range and Common-Mode Rejection Ratio Test Circuit

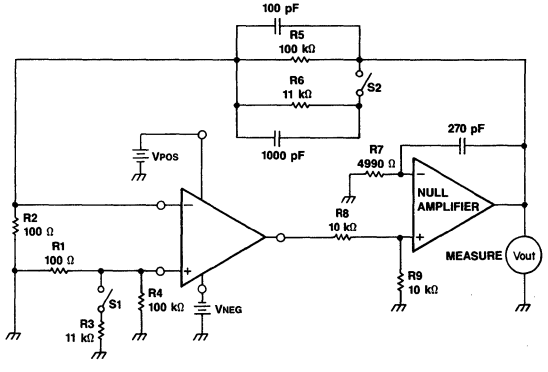


Figure 6. Power Supply Rejection Ratio Test Circuit

Test Circuits
(Continued)

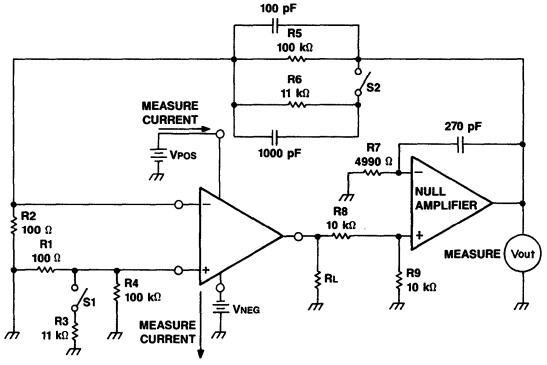


Figure 7. Power Supply Quiescent Current Test Circuit

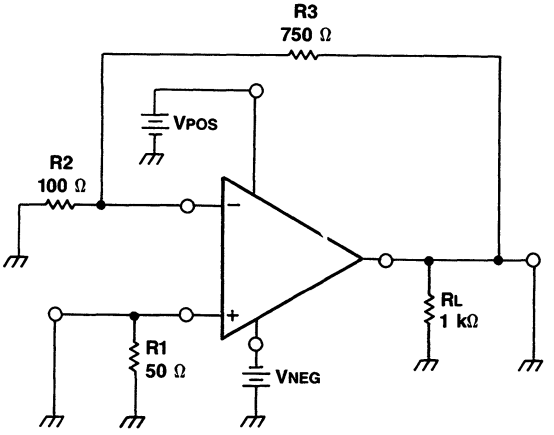


Figure 8. Slew Rate Test Circuit

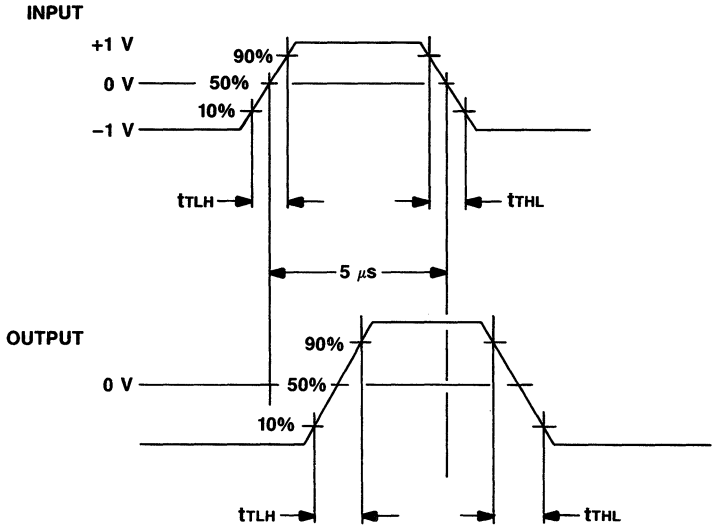


Figure 9. Slew Rate Test Circuit

Connection Options

The diagrams show connections for the various options.

Figure 10 shows the required connections for basic circuit operation with internal compensation and no offset null of the low-output current option, while Figure 11 shows the connections for the same options for high-output current.

Figures 12 and 13 show the connections with offset null and external compensation for the low-output current and high-output current, respectively. Offset null can be accomplished by placing a 200 ohm potentiometer between leads 5 and 6 with the wiper arm connected to the negative supply (lead 4).

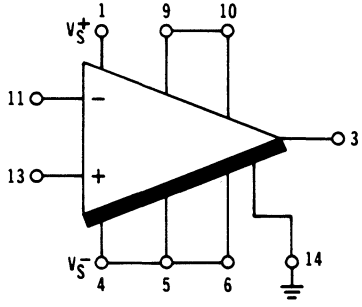


Figure 10. Low Current Output
No Offset Null Internal Compensation

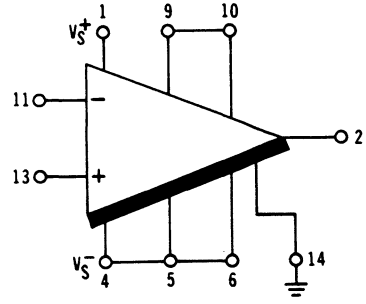


Figure 11. High Current Output
No Offset Null Internal Compensation

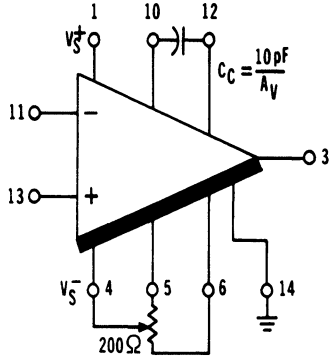


Figure 12. Low Current Output
Offset Null External Compensation

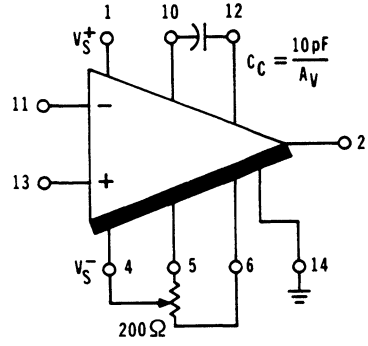


Figure 13. High Current Output
Offset Null External Compensation

Optional Bias Current Feature

This device features an optional supply current bias adjustment capability (leads 14, 15, 16). With this option there are several methods by which correct adjustment of the supply current may be obtained. Three are illustrated here:

Option 1:
If a noise-free dc ground is available, simply connect lead 14 (Supply Current Control) to ground to assure the correct bias.

Option 2:
If a noise-free dc ground is not available, tie lead 14 to lead 4 (Negative Supply Voltage) with an external 12 k resistor to assure the correct bias.

Option 3:
If a noise-free dc ground is not available, another option would be to tie lead 16 (Optional Bias Current) to lead 4 with an external 24 k resistor to assure the correct bias.

Supply Current/Unity-Gain Bandwidth Characteristic

With this device feature it is possible to establish a trade-off between supply current and unity-gain bandwidth. This characteristic is illustrated in Figure 14.

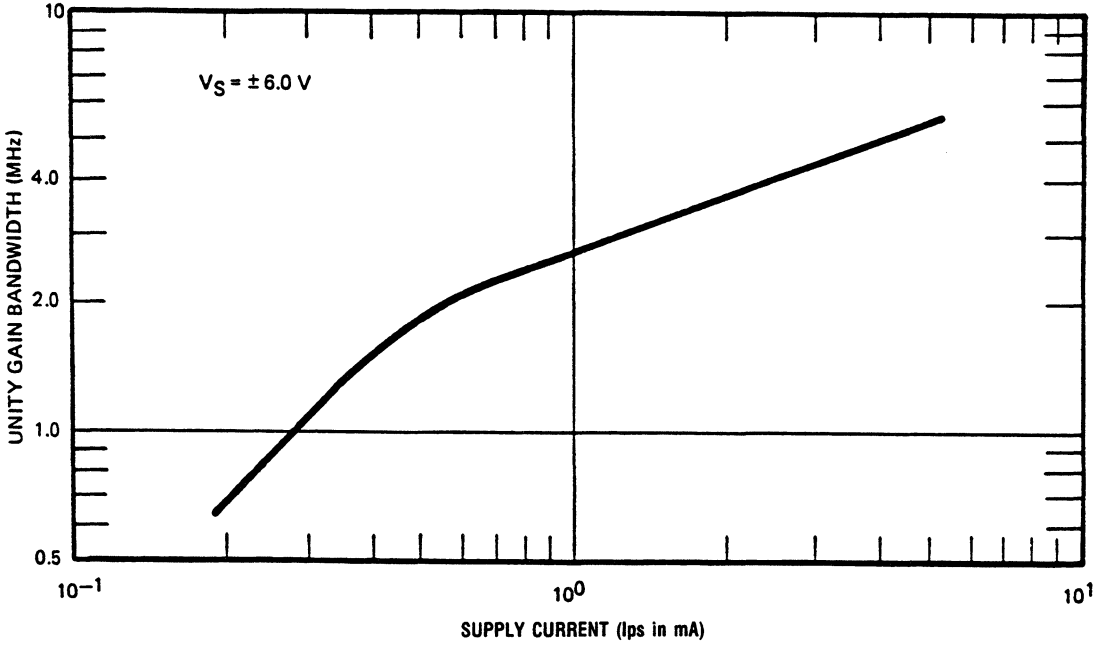


Figure 14. Supply Current/Unity Bandwidth Characteristic

Frequency Characteristics

The open-loop phase and gain curves (Cc = 0) show that for 40 dB closed-loop gain, the phase margin is approximately 60°.

With the 10 pF external compensation, the normal 6 dB/octave roll-off is obtained for both the high- and low-output current options. With this compensation, the amplifier will show little high-frequency peaking, and the step response will exhibit negligible overshooting or ringing.

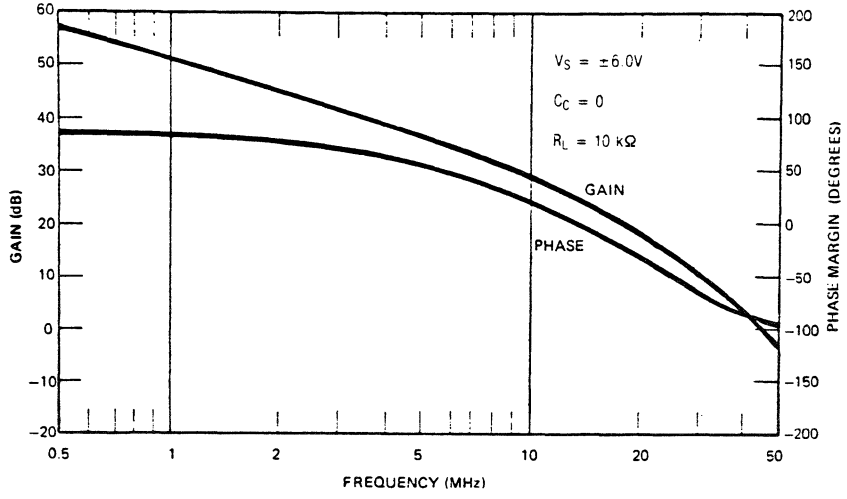


Figure 15. Open-Loop Gain and Phase vs. Frequency

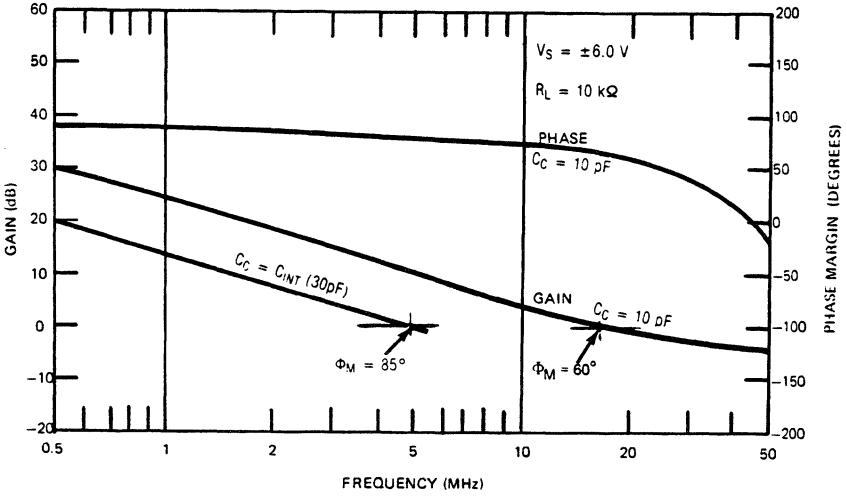
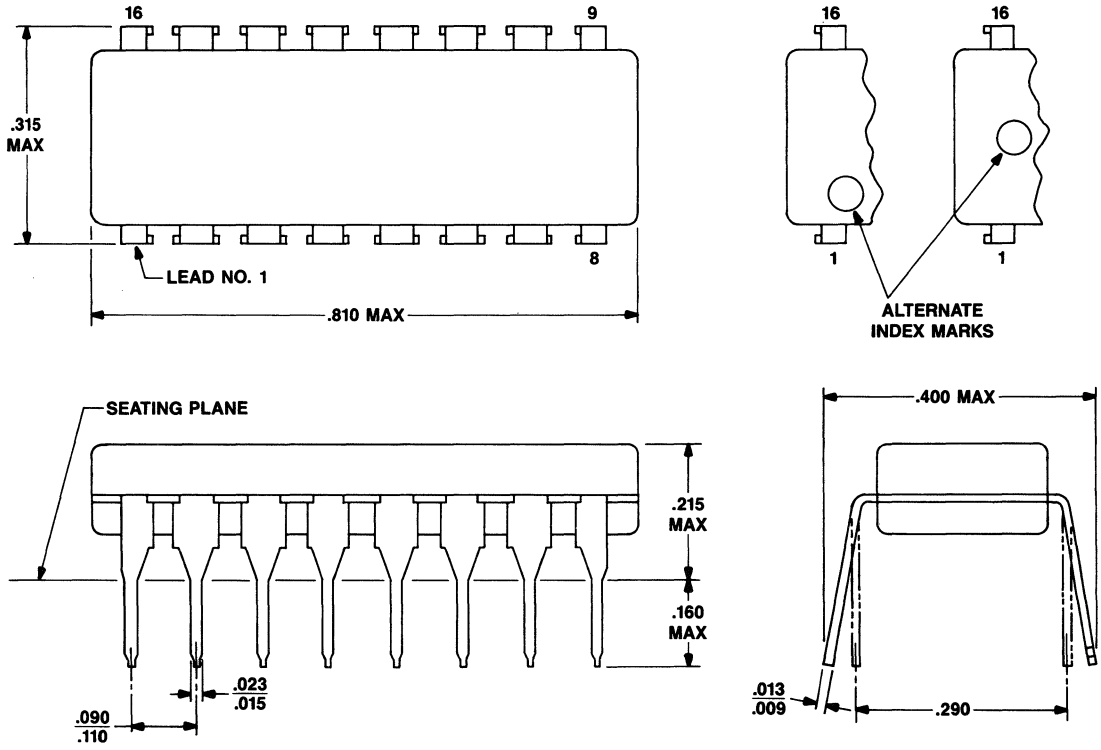


Figure 16. Open-Loop Gain and Phase vs. Frequency

Outline Drawing

(Dimensions in Inches)



Note 1: Pin numbers are shown for reference only.

Ordering Information

Device	Comcode
LB1032AC	104368071

PROGRAMMABLE MEDIUM POWER OUTPUT OP-AMP LB1032BC

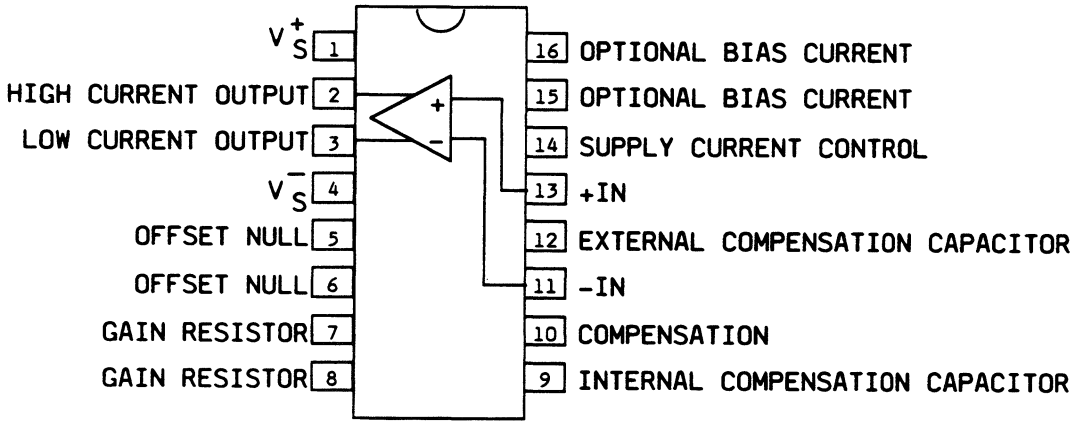
Description

The LB1032BC is a programmable internally compensated medium-power operational amplifier. Maximum supply voltage is ±9.0 V and output current is ±140 mA into a 45 ohm load. Optional bias control, external compensation, offset nulling, and a low-current, higher frequency output also provided.

Features

- 140 mA minimum output current capability
- Guaranteed minimum unity-gain frequency of 2.5 MHz
- Offset voltage null capability
- 1.5 V/μs typical slew rate
- Optional internal or external compensation
- Supply voltage range: ±3.0 to ±9.0 volts
- Differential-mode voltage range: ±6.5 volts
- 16-pin plastic DIP

Pin Diagram



Maximum Ratings (At 25°C unless otherwise specified)	
Ambient Operating Temperature Range	0 to +60°C
Storage Temperature Range	−40 to +125°C
Supply Voltage Range (V_S^+ to V_S^-)	18 V
Differential Mode Input Voltage (+IN to −IN)	±6.5 V
Total Power Dissipation	500 mW

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Electrical Characteristics (T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic and Test Condition			Symbol	Min①	Typ②	Max①	Unit
Open Loop Voltage Gain (Figure 2) (f = 100 Hz, R_L = 10 kΩ, C_C = 0, V_S = ±8.5 V) (f = 1000 Hz, R_L = 10 kΩ, C_C = C_{INT}, V_S = ±8.5V) (f = 100 Hz, R_L = 45 Ω, V_S = ±8.5 V, V_O = 4.25 V_{RMS})			A_{VOL}	88 68 80	97 73 87	— 80 —	dB
Closed Loop Voltage Gain③ (R_L = 45 Ω. V_S = ±8.5 V)			A_{VCL}	2.5	2.8	3.5	dB
Input Offset Voltage (Figure 3) (R_L = 10 kΩ, V_S = 3.0 V) (R_L = 10 kΩ, V_S = ±9.0 V)			$\lvert V_{IO}\rvert$	—	0.9	5.0	mV
Input Bias Current (Figure 4) (R_L = 10 kΩ, V_S = ±8.5 V)			I_{IB}	0	0.42	1.8	μA
Input Offset Current (Figure 4) R_L = 10 kΩ, V_S = ±8.5 V)			$\lvert I_{IO}\rvert$	—	30	400	nA
Output Voltage Swing (Figure 5)	Low Current Output (V_S = ±8.5 V)	R_L = 10 kΩ	V_{OM}	+7.5 −7.5	+7.7 −7.7	—	V(peak)
		R_L = 180 Ω		+6.3 −6.3	+6.7 −6.7	—	
	High Current Output (V_S = ±8.5 V)	R_L = 10 kΩ		+7.4 −7.4	+7.7 −7.6	—	
		R_L = 45 Ω		+6.5 −6.3	+6.6 −6.5	—	
Common-Mode Voltage Range ($\triangle V_{IO}$ = 2.0 mV, V_S = ±9.0 V, R_L = 10 kΩ)			CMVR	+7.5 −7.5	—	—	V
Power-Supply Rejection Ratio (V_S = ±3 to ±9.0 V)(Figure 6)			$\lvert PSRR(\pm)\rvert$	—	30	200	μV/V
Power-Supply Current (V_S = ±9.0 V, R_L = 10 kΩ) (Figure 8)			I_{PS}	—	+4.4 −3.7	+7.0 −7.0	mA
Differential Input Breakdown Voltage (V_S = ±9.0 V, @ 10 μA dc)			$V_{(BR)II}$	+6.5 −6.5	+7.7 −7.9	—	V

① Max/Min values are guaranteed specification limits at worst case supply conditions.
② Typical values are characteristics at optimum power-supply voltage conditions. Individual devices may differ significantly from the typical values shown.
③ Lead 7 = ground; lead 13 = +IN; lead 2 connected to lead 8.
④ This condition is not tested in production devices.

Test Circuits

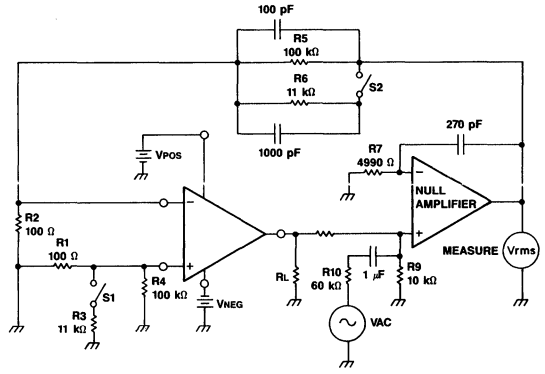


Figure 1. Open Loop Gain Test Circuit

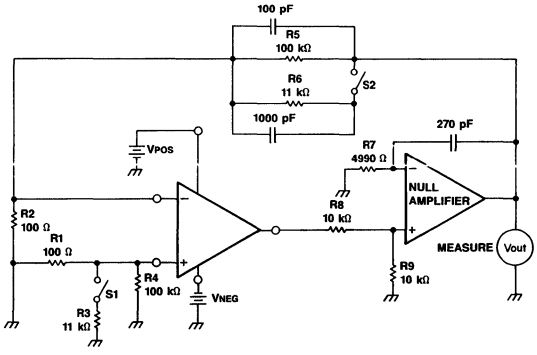


Figure 2. Input Offset Voltage (V_{IO}), Input Bias Current (I_{IB}), and Input Offset Current (I_{IO}) Test Circuit

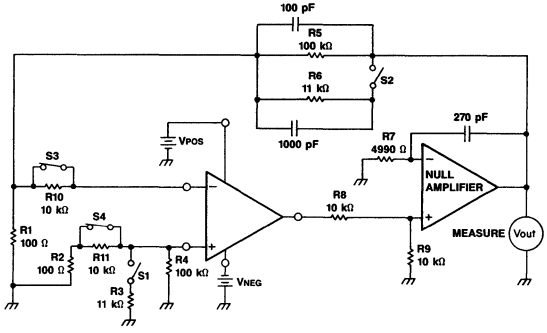


Figure 3. Input Bias and Input Offset Current Test Circuit

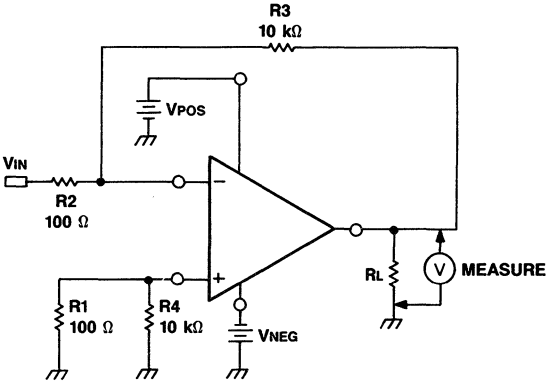


Figure 4. Output Voltage Swing Test Circuit

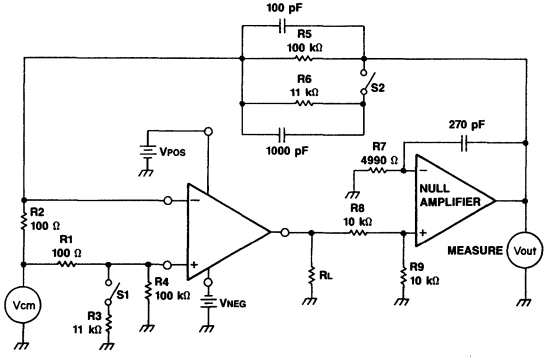


Figure 5. Common Mode Voltage Range and Common-Mode Rejection Ratio Test Circuit

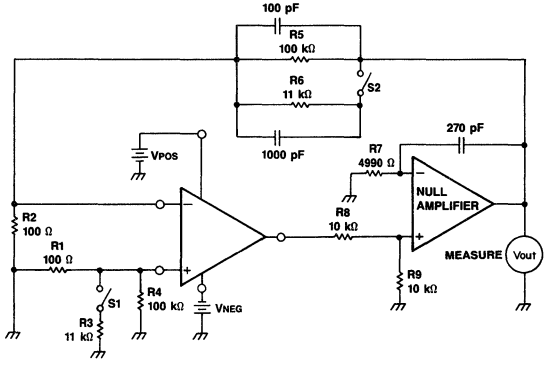


Figure 6. Power Supply Rejection Ratio Test Circuit

Test Circuits
(Continued)

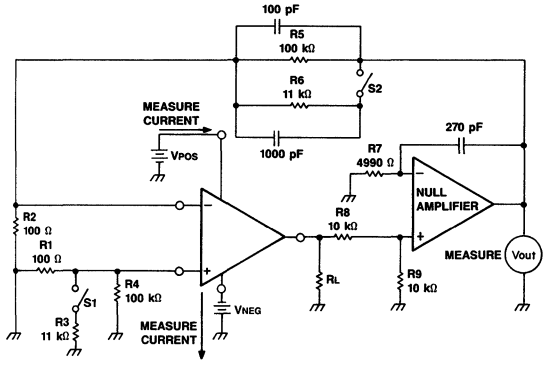


Figure 7. Power Supply Quiescent Current Test Circuit

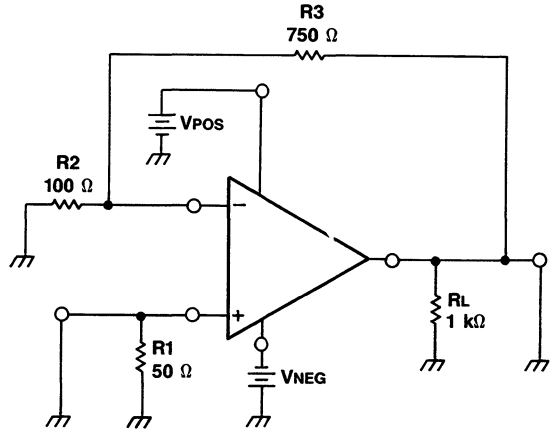


Figure 8. Slew Rate Test Circuit

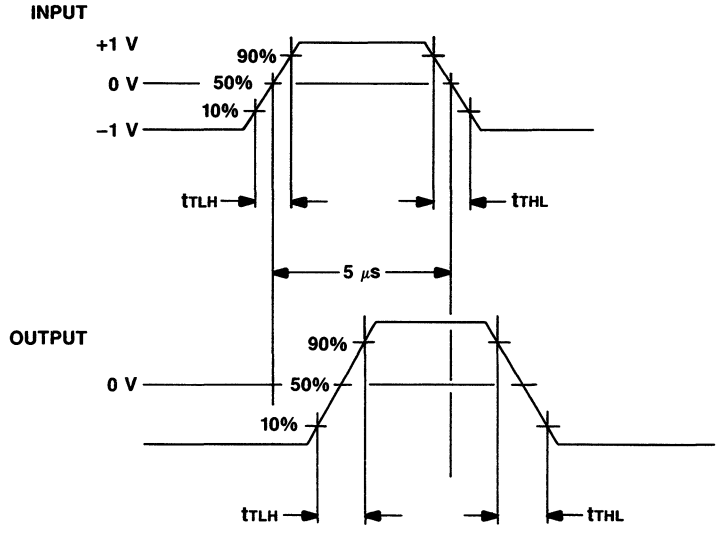


Figure 9. Slew Rate Test Circuit

Connection Options

The diagrams show connections for the various options.

Figure 11 shows the required connections for basic circuit operation with internal compensation and no offset null of the low-output current option, while Figure 12 shows the connections for the same options for high-output current.

Figures 13 and 14 show the connections with offset null and external compensation for the low-output current and high-output current, respectively. Offset null can be accomplished by placing a 200 ohm potentiometer between leads 5 and 6 with the wiper arm connected to the negative supply (lead 4).

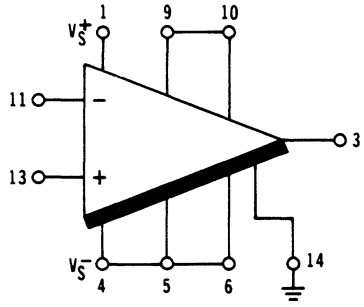


Figure 11. Low Current Output
No Offset Null Internal Compensation

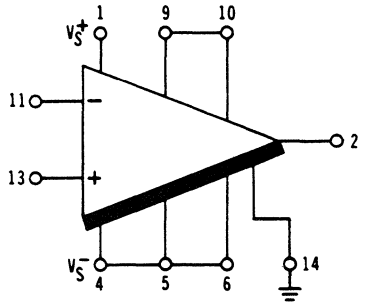


Figure 12. High Current Output
No Offset Null Internal Compensation

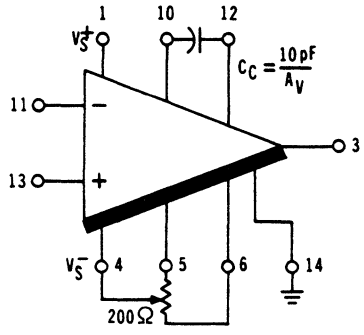


Figure 13. Low Current Output
Offset Null External Compensation

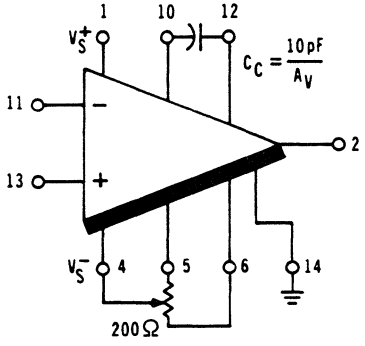


Figure 14. High Current Output
Offset Null External Compensation

Optional Bias Current Feature

This device features an optional supply current bias adjustment capability (leads 14, 15, 16). With this option there are several methods by which correct adjustment of the supply current may be obtained. Three are illustrated here:

Option 1:
If a noise-free dc ground is available, simply connect lead 14 (Supply Current Control) to ground to assure the correct bias.

Option 2:
If a noise-free dc ground is not available, tie lead 14 to lead 4 (Negative Supply Voltage) with an external 12 k resistor to assure the correct bias.

Option 3:
If a noise-free dc ground is not available, another option would be to tie lead 16 (Optional Bias Current) to lead 4 with an external 24 k resistor to assure the correct bias.

Supply Current/Unity-Gain Bandwidth Characteristic

With this device feature it is possible to establish a trade-off between supply current and unity-gain bandwidth. This characteristic is illustrated in Figure 15.

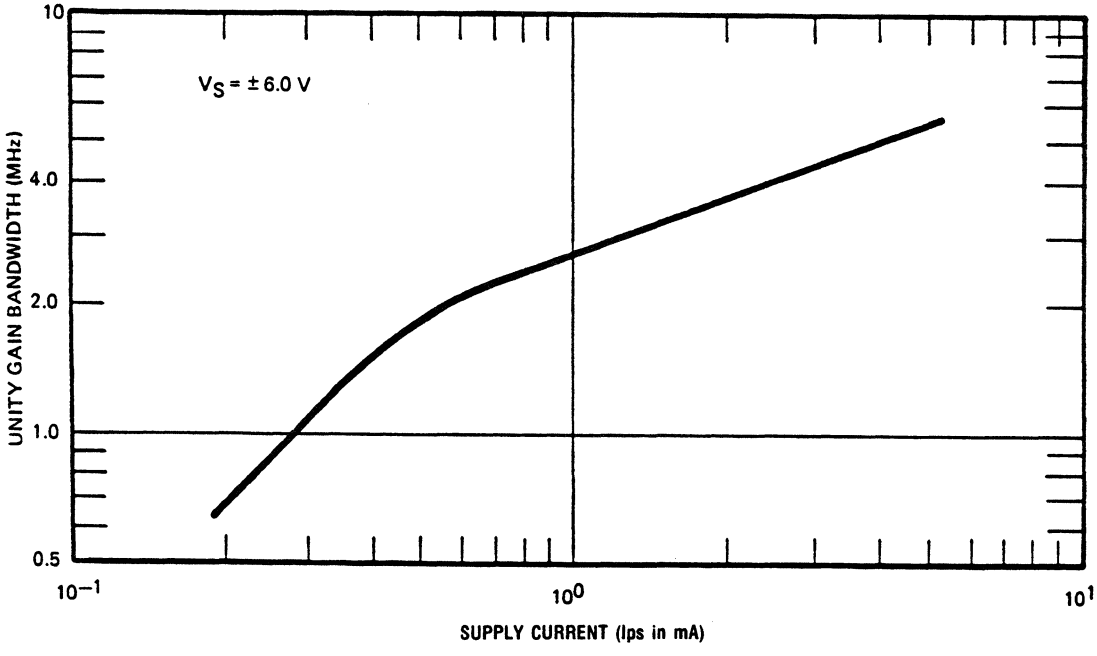


Figure 15. Supply Current/Unity Bandwidth Characteristic

Frequency Characteristics

The open-loop phase and gain curves (Cc = 0) show that for 40 dB closed-loop gain, the phase margin is approximately 60°.

With the 10 pF external compensation, the normal 6 dB/octave roll-off is obtained for both the high- and low-output current options. With this compensation, the amplifier will show little high-frequency peaking, and the step response will exhibit negligible overshooting or ringing.

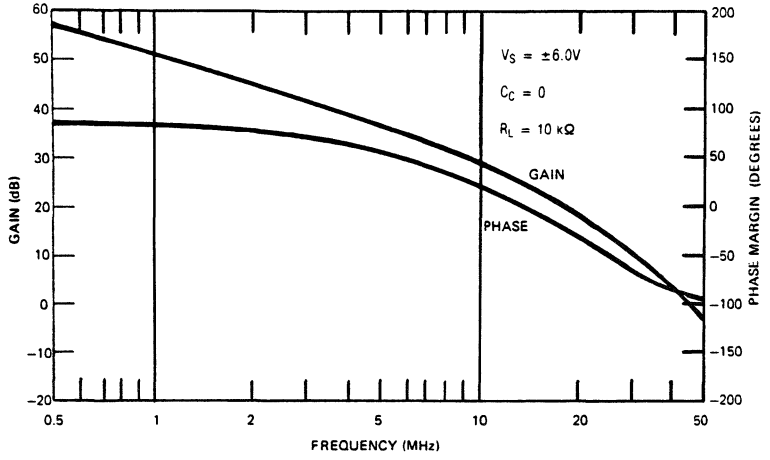


Figure 16. Open-Loop Gain and Phase vs. Frequency

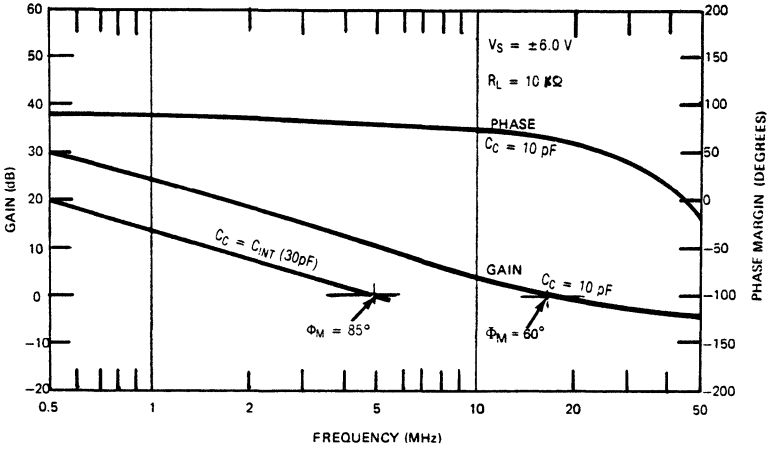
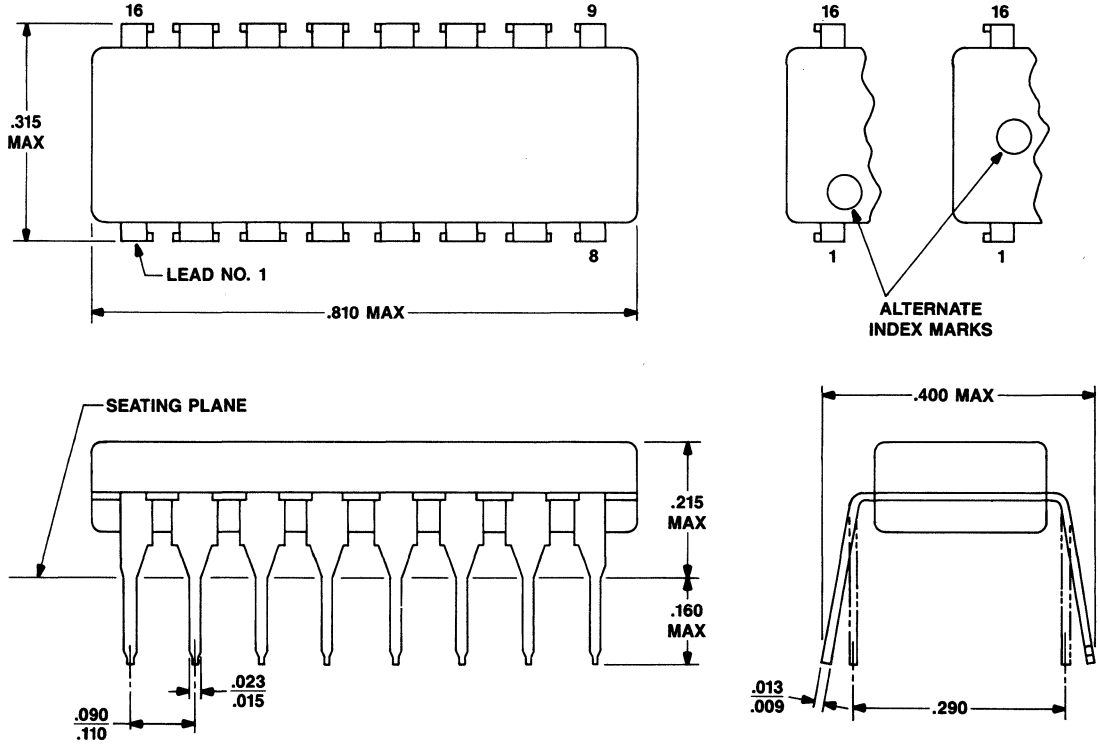


Figure 17. Open-Loop Gain and Phase vs. Frequency

Outline Drawing

(Dimensions in Inches)



Note 1: Pin numbers are shown for reference only.

Ordering Information

Device	Comcode
LB1032BC	104368089

Description

The LB1034AC is a bias programmable wideband, high-output current operational amplifier. It features low-quiescent current, high-output voltage swing, and a high gain-bandwidth product. Power-supply voltages of ±2.0 to ±15 volts are usable. Internal "T" and feedback compensation are available for closed-loop gains exceeding 20 dB.

This device can also be used as a micropower operational amplifier, with power-supply currents as low as 5.0 μA, and greatly reduced input bias and offset currents. The gain-bandwidth product of the amplifier (f_T) is adjustable with bias current.

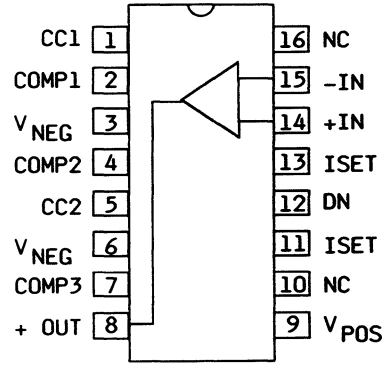
Features

- Capable of sinking or sourcing a minimum 150 mA output current
- 2.1 mA maximum quiescent-supply current
- Static discharge protection
- Internal "T" compensation
- 80 dB open-loop gain to 100 kHz
- Wideband performance optimized for closed-loop gains > 20 dB
- Bias programmable for wide adjustment of bandwidth and supply current
- Typical minimum unity-gain frequency of 1.0 MHz
- Operation to +85°C

Maximum Ratings (At T_A = 25°C)	
Supply-Voltage Range	±2.0 to ±15 V
Differential-Mode Voltage Range	±6.0 V
Bias Resistor Voltage	15 V
Power Dissipation	600 mW
Storage Temperature Range	−40 to +125°C
Ambient Operating Temperature Range	0 to +85°C
Pin Soldering Temperature (t = 15 s max.)	300°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Diagram



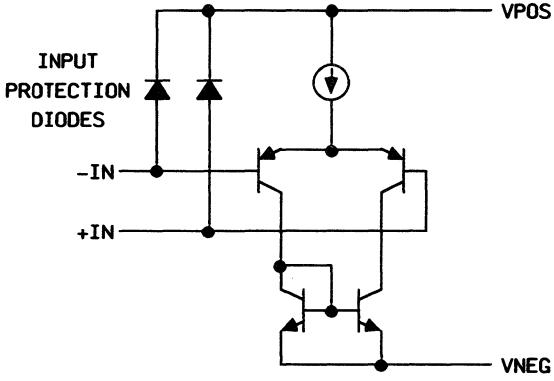


Figure 1. Simplified Input Diagram

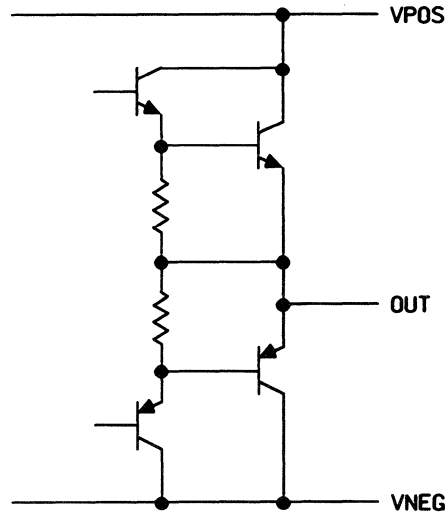


Figure 2. Simplified Output Diagram

Note: The input leads are ESD-protected to the negative supply by parasitic diodes.

Pin Description

Pin	Symbol	Name/Function
1	CCI	Feedback Compensation Capacitor—Internal
2	COMP1	Feedback Compensation Capacitor—External
3	VNEG	The most negative supply-voltage is connected to this pin.
4	COMP2	Feedback Compensation Capacitor—External
5	CC2	Feedback Compensation Capacitor—Internal
6	VNEG	The most negative supply-voltage is connected to this pin.
7	COMP3	"T" Compensation—Internal
8	OUT	Op-Amp Output
9	VPOS	The most positive supply-voltage is connected to this pin.
10	NC	No connection. This lead may be used for a tie point.
11	ISET	Internal Bias Current (Through Internal Resistor IBR)
12	DN	Decoupling Node
13	ISET	External Bias Current (Through External Resistor EBR)
14	+ IN	Op-Amp Input (Non-Inverting)
15	− IN	Op-Amp Input (Inverting)
16	NC	No Connection. This lead must not be used as a tie point.

Connection Options

Figures 3, 4, and 5 show the connections for various options available with the LB1034AC in normal operation. Combinations of the options are, of course, possible.

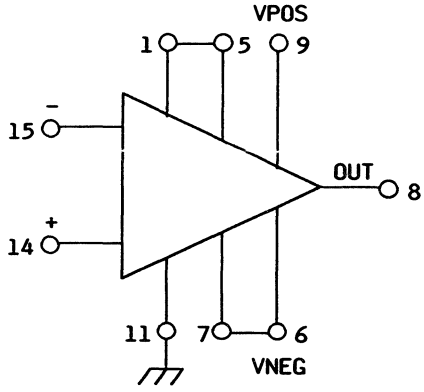


Figure 3. Internal Bias Setting Internal "T" Compensation

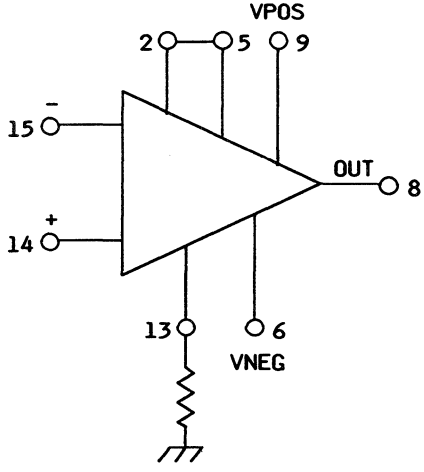


Figure 4. External Bias Setting Internal Feedback Compensation

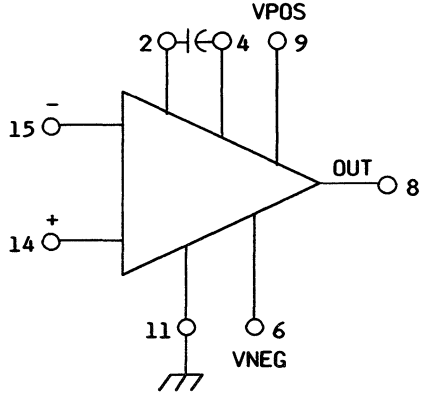


Figure 5. Internal Bias Setting External Feedback Compensation

Type of Compensation	Connect
Feedback, C_C = 4.5 pF	1 to 5
Feedback, C_C = 9.0 pF	2 to 5
Feedback, C_C = 18 pF	2 to 5 and 1 to 4
Feedback, C_C = External	Capacitor between 2 and 4
T, Internal (9 + 9) pF	1 to 5 and 7 to 6*
T, External Components	Input C to 2
	Output C to 4
	Resistor to 6

*Add 200 kΩ resistor between leads 1, 5, and 9 if needed to prevent high-frequency ringing.

Feedback Compensation

When using the LB1034AC with capacitive feedback compensation, the amplifier gain exhibits a single-pole (1/f) frequency response. The gain-bandwidth product (f_T) obtained depends on I_{SET} and C_C measured in pF,

$$f_T = \left[\frac{1000}{(C_C + 0.8)}\right] \left[\frac{I_{SET}}{250\ \mu A}\right] \text{MHz}$$

The amplifier must be compensated so that its feedback loop gain is reduced below unity at a frequency not higher than

$$f_L = 15 \left[\frac{I_{SET}}{250\ \mu A}\right] \text{MHz}$$

Conservative designs may have loop gain crossover at a frequency which is lower than f_L by a factor of 2 to 5 or more.

For a given closed-loop voltage gain A_V, a suggested minimum C_C to assure stability is

$$C_C = (90/A_V)\ \text{pF}.$$

To improve phase margins, a small resistor R_C may be added in series with C_C. If used, R_C may be chosen approximately equal to the reactance of C_C at 3 times the loop gain crossover frequency f_T/A_V. Hence,

$$R_C = 53\ A_V(1 + 0.8/C_C)(250\ \mu A/I_{SET})\ \Omega, \text{ with } (C_C \text{ in pF}).$$

Operation with $C_C < 1.0$ pF is not recommended in any case, as phase margins may be unacceptably low. Thus for example, with I_{SET} = 250 μA and A_V = 1, C_C = 90 pF and R_C = 54 ohms provide f_T = 11 MHz. This compensation provides a useful wideband unity-gain buffer amplifier.

In general, the slew rate obtainable with capacitive feedback compensation is approximately

$$\text{Slew Rate } (V/\mu s) \cong 2\ I_{SET}(\mu A)/C_C(pF).$$

Electrical Characteristics⑤

(T_A = 25°C unless otherwise specified)

Parameter and Conditions			Symbol	Min	Typ⑥	Max	Units
Test Condition Supply Voltage			V_S	±15	±12	±15	V
Open-Loop Voltage Gain (C_C = C_{INT} "T"	f = 10 kHz	Figure 6	A_{VOL}	80	—	—	dB
	f = 150 kHz			68.9	—	79	
Input Offset Voltage		Figure 7	$\|V_{IO}\|$	—	1.0	4.5	mV
Input Bias Current		Figure 7	I_{IB}	—	3.0	6.0	μA
Input Offset Current⑦		Figure 7	$\|I_{IO}\|$	—	0.2	1.0	μA
Output Voltage Swing (R_L = 2 kΩ)			V_{OM}	+9.7 −9.7	+10.0 −10.5	—	V(peak)
Common-Mode Voltage Range (△V_{IO} = ±2.0 mV)			CMVR	+10.0 −11.5	—	—	V
Common-Mode Rejection Ratio f = dc			CMRR	75	95	—	dB
Power-Supply Rejection Ratio		Figure 7	$\|PSRR(\pm)\|$	—	20	40	μV/V
Power-Supply Current	Positive	Figure 8	I_{ps}^{+}	1.65	1.8	2.10	mA
	Negative		I_{ps}^{-}	1.40	—	1.85	
Output Current Drive	R_L = 30 Ω		I_O	±150	±220	—	mA(peak)

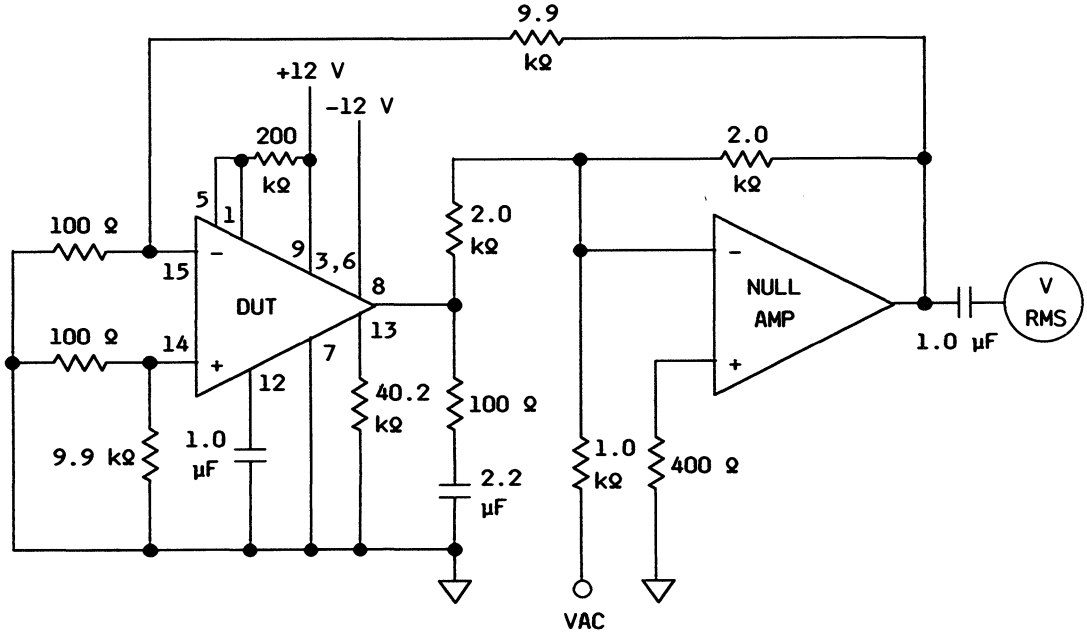


Figure 6. Open-Loop Voltage Gain Test Circuit

⑤ Lead 3 is connected through a 40.2-kohms bias resistor to ground for all tests.
⑥ Typical values are characteristics at optimum power-supply voltage conditions.
⑦ This current may degrade if the differential mode input voltage exceeds ±6 V.

Characteristics (Continued)

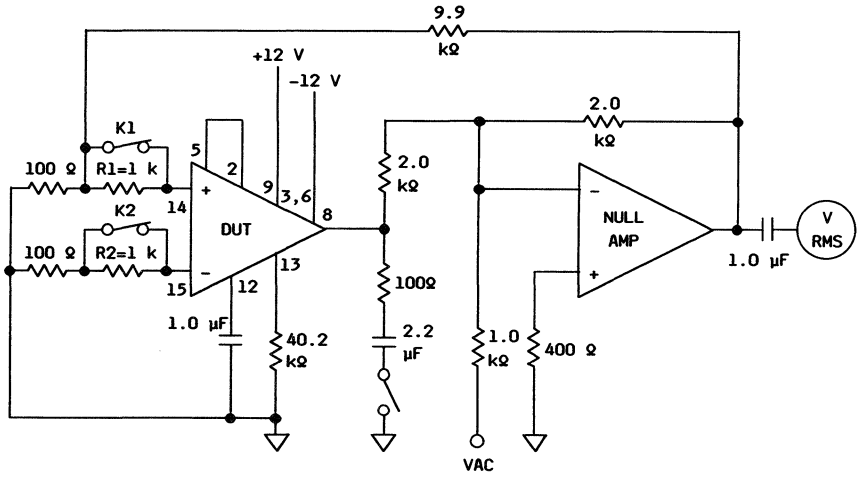


Figure 7. Input Offset Voltage (V_{IO}), Input Bias Current (I_{IB}), Input Offset Current (I_{IO}) and Power-Supply Rejection Ratio (PSRR) Test Circuit

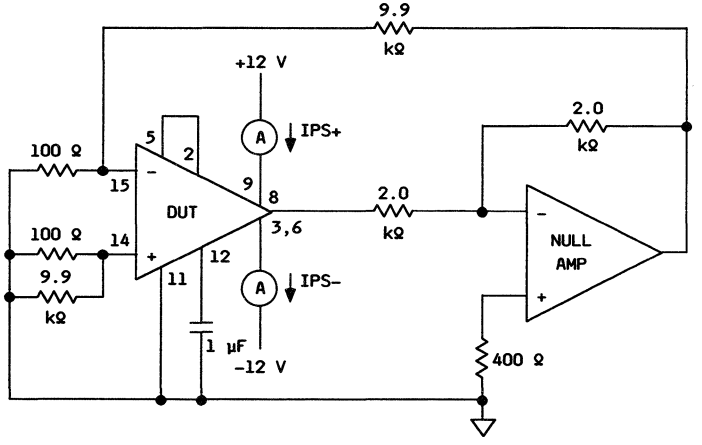


Figure 8. Power-Supply Current Test Circuit

dc Biasing

A dc bias current, I_{SET}, must be drawn from either lead 11 or lead 13 to permit amplifier operation. This may be done as follows:

Option 1. If $V_S = \pm 12$ V, grounding lead 11 permits normal operation.

Option 2. If $V_S = \pm 6.0$ V, connecting lead 6 to lead 11 permits normal operation.

Option 3. To set bias levels externally, a resistor, R, is connected from lead 13 to a lower fixed potential, V_R. Usually V_R is connected to ground or V_{NEG}. For normal operation, R, is selected so that

$$I_{SET} = \frac{(V_{POS} - V_R - 1.3)}{(R + 1.5\ k\Omega)} = 0.250\ mA.$$

Option 4. Micropower application.

Micropower operation can be achieved by using larger values of R in the bias circuit of Figure 4. The resulting quiescent power-supply current is approximately

$$I_{ps}^{+} \approx 7.5\ I_{SET}, \text{ where } I_{SET} = \frac{(V_{POS} - V_R - 1.3)}{(R + 1.5\ k\Omega}$$

I_{ps}^{+} values as low as 5.0 μA have been achieved this way. The available output current (I_O), input bias current (I_{IB}), input offset current (I_{IO}), and open-loop voltage gain (A_{VOL}) will be decreased as bias current is lowered.

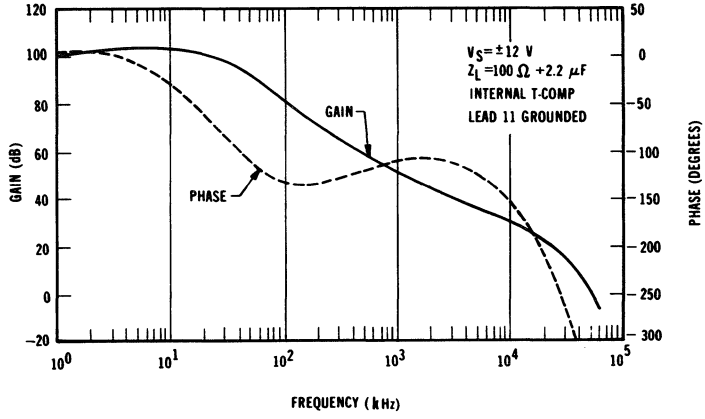


Figure 9. Open-Loop Gain and Phase vs. Frequency

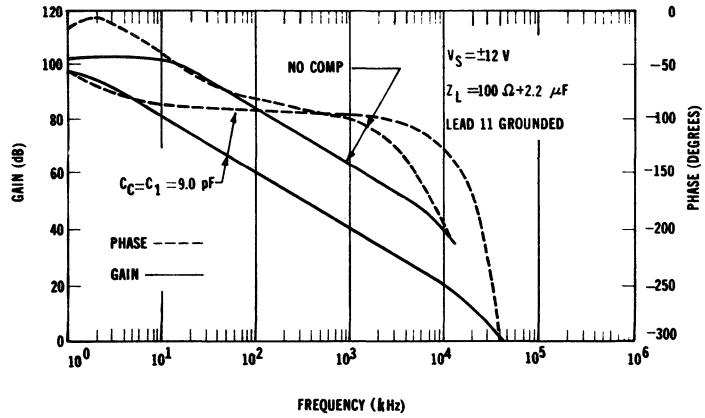


Figure 10. Open-Loop Gain and Phase vs. Frequency

Characteristics
(Continued)

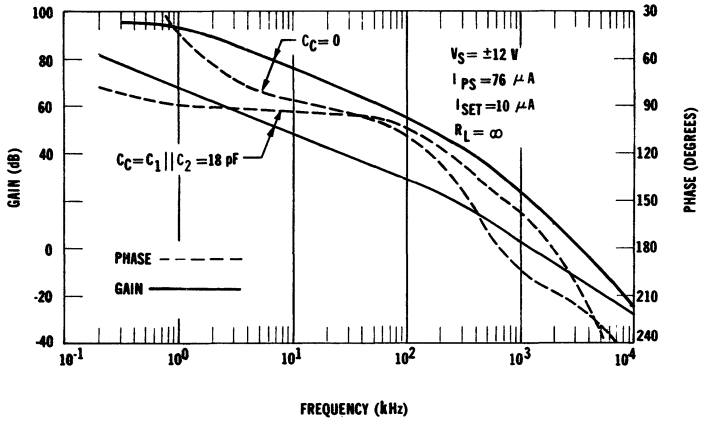


Figure 11. Open-Loop Gain and Phase vs. Frequency

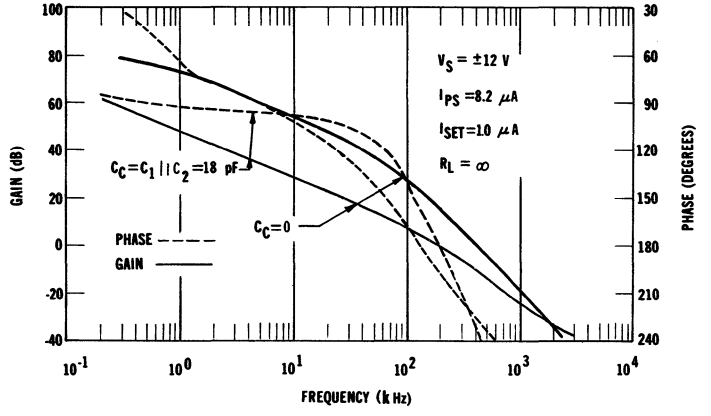


Figure 12. Open-Loop Gain and Phase vs. Frequency

Frequency Characteristics

The open-loop phase and gain curves using internal feedback compensation (C_C = 9.0 pF) show that closed-loop gains down to about 20 dB are usable. With this compensation, the normal 6.0 dB/octave roll-off is obtained. The amplifier thus configured will show little high-frequency peaking, and the stop response will exhibit negligible overshoot or ringing. Lower closed-loop gains can be used by increasing C_C. The minimum usable gain varies inversely with C_C.

The internal "T" compensation can achieve 80 dB open-loop gain up to 100 kHz. Double-pole, single-zero roll-off is obtained as shown. This compensation is designed primarily for closed-loop gains above 30 dB, with $I_{SET} \approx 250\ \mu A$. It may not give optimum step response.

The power-supply rejection and common-mode rejection ratios should have frequency dependence similar to the open-loop gain. Thus at 10—100 kHz, a T-compensated LB1034AC will have better power-supply and common-mode rejection than a feedback-compensated amplifier. At dc or very low frequencies, there will be no significant difference.

Special Applications

Dynamic Control of ISET

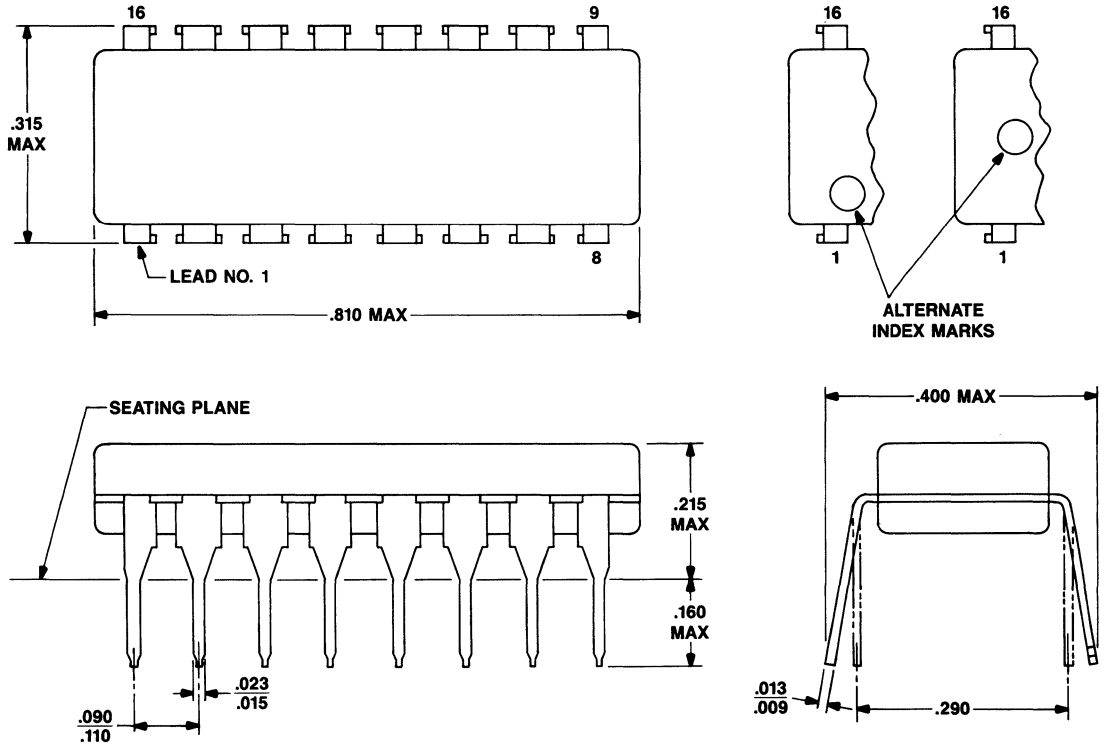
Biasing the LB1034AC by connecting lead 13 to an external variable current sink permits switching the amplifier on and off; or controlling its effective bandwidth, at a constant closed-loop gain.

High-Temperature Operation

Using high ISET (about 1 mA) and low supply voltage enables short-term operation at derated temperatures (to 150°C), with reduced performance.

Outline Drawing

(Dimensions in Inches)



Ordering Information

Device	Comcode
LB1034AC	104368105

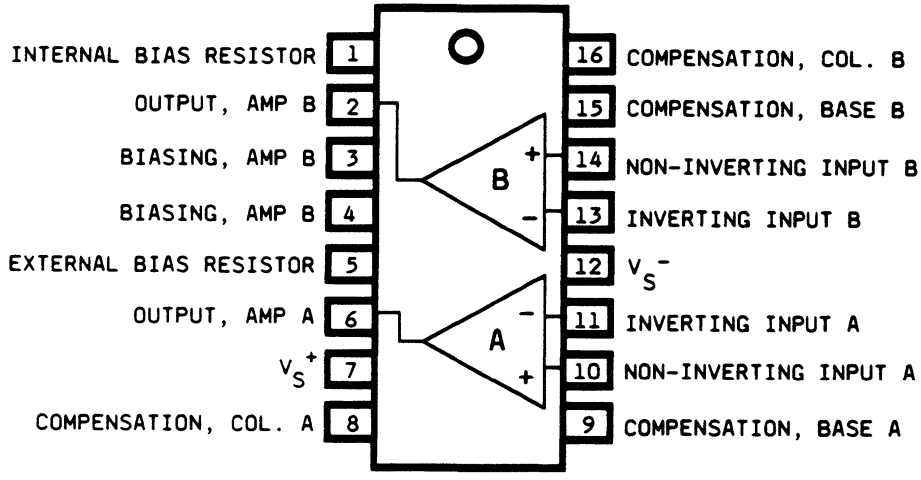
Description

The LB1035AC is a dual micro-power operational amplifier intended for applications requiring minimum quiescent power dissipation. It is bias-programable, permitting simultaneous adjustment of supply current (I_{PS}) and gain-bandwidth product (f_T) over about three orders of magnitude. A nominal $I_{PS} \cong 100\ \mu A$ per amplifier provides $\cong$ 1.5 MHz internally compensated for closed-loop gains down to unity.

Features

- 130 μA per amplifier maximum supply current at $\pm$6.2 V power supplies
- Low-voltage operation
- Internal compensation
- Guaranteed minimum unity-gain frequency of 750 kHz
- 0.53 V/μs typical slew rate
- Bias programmable for adjustment of bandwidth and supply current
- Static discharge protection
- Supply voltage range: $\pm$1.0 to $\pm$10 volts
- Differential-mode voltage range: $\pm$6.0 volts
- 16-pin plastic DIP

Pin Diagram



Maximum Ratings (At 25°C unless otherwise specified)	
Ambient Operating Temperature Range	0 to +60°C
Storage Temperature Range	−40 to +125°C
Power Dissipation	500 mW
Supply-Voltage Range (V+ to V−)	30 V
Supply-Voltage Difference Internal Bias Resistor (Pin 1) to V+ (Pin 7)	15 V
Supply-Voltage Difference Non-Inverting Input A (Pin 10) to Inverting Input (Pin 11)	±6.0 V
Supply-Voltage Difference Inverting Input (Pin 13) to Non-Inverting Input B (Pin 14)	±6.0 V
Output Current (Each Amplifier, Pin 2 and Pin 6)	±2.0 mA

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

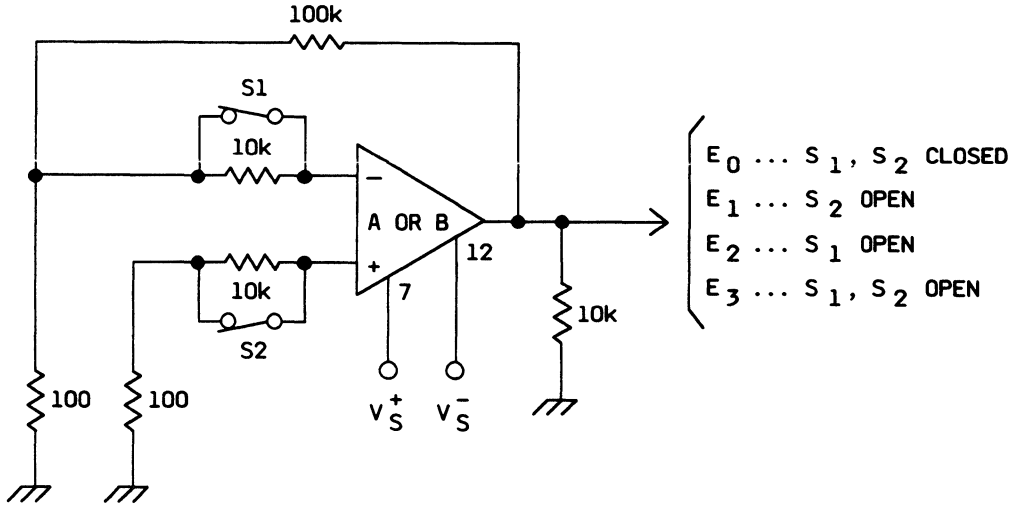
Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic and Test Condition		Symbol	Min	Typ②	Max	Unit
Test Condition Supply Voltage		V_S	±6.2	±6.2	±6.2	V
Extrapolated Unity Gain Frequency (R_L = 10 kΩ, f = 1.0 kHz, C_C = C_{INT}		f_T	750	1500	3000	kHz
Open-Loop Voltage Gain (R_L = 10 kΩ)		A_{VOL}	—	108	—	dB
Input Offset Voltage (Figure 1)		$\lvert V_{IO}\rvert$	—	1.0	4.5	mV
Input Bias Current (Figure 1)		I_{IB}	—	40	100	nA
Input Offset Current③ (Figure 1)		$\lvert I_{IO}\rvert$	—	5	30	nA
Output Voltage Swing, (R_L = 10 kΩ)(Figure 2)		V_{OM}	+5.0 −5.0	+5.35 −5.35	—	V
Common-Mode Voltage Range		CMVR	+5.0 −5.0	+5.4 −5.4	—	V
Common-Mode Rejection Ratio		CMRR	80	100	—	dB
Power-Supply Rejection Ratio (Figure 3)		$\lvert PSRR(\pm)\rvert$	74	104	—	dB
Power-Supply Current	Both Amplifiers (Figure 4)	I_{PS}^{+}	100	200	260	μA
	Amp A Only		55	105	140	μA
Slew Rate (Typical)		SR	—	0.53	—	V/μs
Temperature Coefficient of Input Offset Voltage		$\lvert TCV_{IO}\rvert$	—	10	—	μV/°C
Output Current Drive (R_L = 100 Ω)		I_O	+2.0 −2.0	+20.0 −3.0	—	mA
Stability Test (R_L = 100 kΩ) (Figure 4)		$\lvert V_{OG}\rvert$	—	—	10	mVrms

Test Circuits



$$V_{IO} = \frac{E_0}{1000}$$

$$I_{IB-} = \frac{E_0 - E_2}{(1000)(10{,}000)}$$

$$I_{IB} = \frac{|I_{IB+}| + |I_{IB-}|}{2}$$

$$I_{IB+} = \frac{E_0 - E_1}{(1000)(10{,}000)}$$

$$I_{IO} = \frac{E_0 - E_3}{(1000)(10{,}000)}$$

Figure 1. Test Circuit, Input Offset Voltage

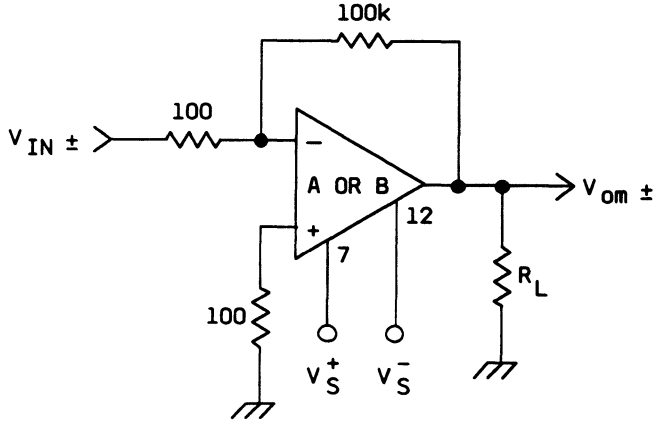
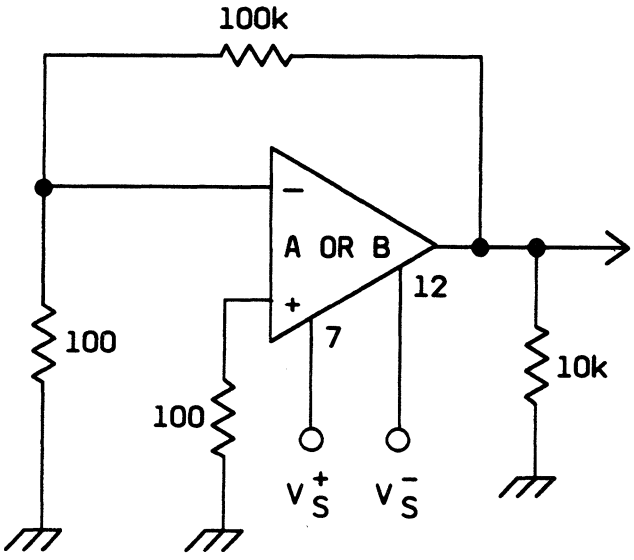


Figure 2. Test Circuit, Output Voltage Swing④

④ Unless otherwise noted: Lead 1 ground, Leads 3 and 4 shorted together.
Lead 7 connected to +6.2 V and Lead 12 connected to −6.2 V.

Test Circuits
(Continued)



E_O @ V_S^+/V_S^- at initial level
E_I @ V_S^+/V_S^- at increased level

$$PSRR(\pm) = \frac{E_I - E_O}{(1000)(\Delta V_S^+ + \Delta V_S^-)}$$

Figure 3. Test Circuit, Power-Supply Rejection Ratio④

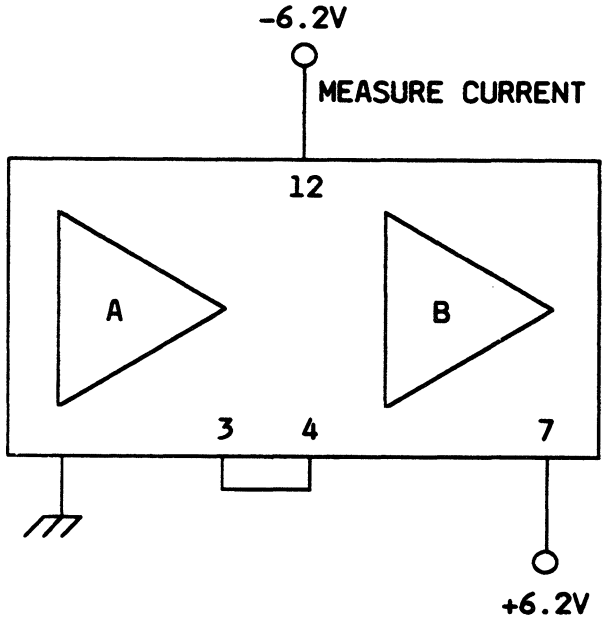


Figure 4. Test Circuit, Power-Supply Current④

Test Circuits
(Continued)

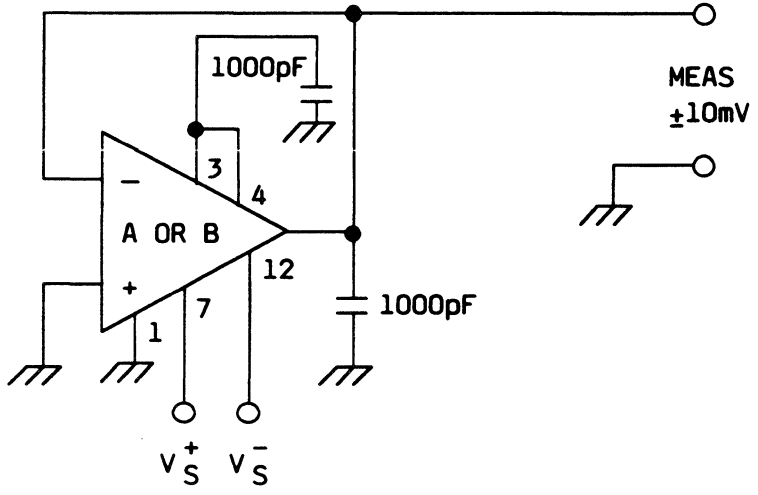


Figure 6. Test Circuit, Open Loop Voltage Gain Test Circuit

Connection Options

Figures 7 and 8 show the connections for various options available with this device in normal operation. Combinations of the options are, of course, possible.

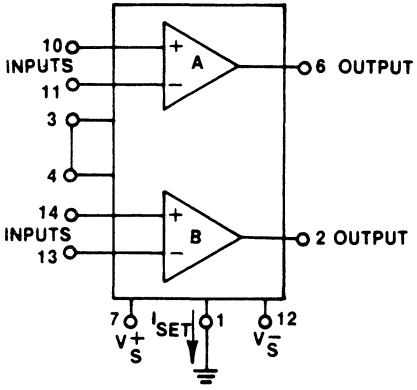


Figure 7. Both Amplifiers Operating, Internal Bias Resistor, Internal Frequency Compensation

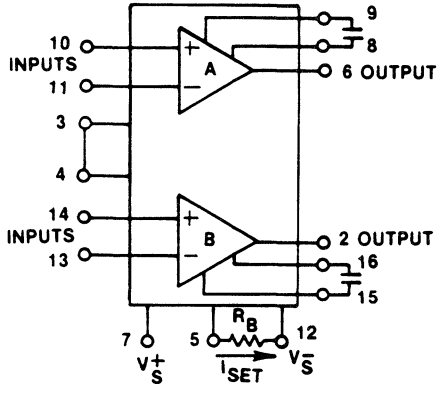


Figure 8. Both Amplifiers Operating, External Bias Resistor, External Frequency Compensation

Connection Options
(Continued)

For general-purpose use, this device may be connected as shown in Figure 7. With ±6.0 volt supplies, this gives $f_T \cong 1.5$ MHz in each amplifier, using the internal-bias resistor and internal frequency-compensation capacitors. With ±3.0 volt supplies, connect lead 1 to V_S^- (Lead 12) instead of to ground, for similar bandwidth.

Figure 8 illustrates the use of external capacitance for improved stability, and the use of an external bias resistor, R_B.

This device may also be used as a single op-amp, with amplifier B rendered inoperative to reduce supply current. To do so, connect lead 3 to lead 7, and make no connection to lead 4. All input, output, and compensation leads to amplifier B may then be left unconnected.

dc Biasing

A dc bias current, I_{SET}, must be drawn from either lead 5 or lead 1 to permit amplifier operation. This is most easily done in one of two ways:

1. Connect a bias resistor, R_B, from lead 5 to some fixed voltage, V_R, which is at least 2.0 V more negative than lead 7. Commonly V_R is ground or V_S^-. Then I_{SET} is determined by the equation

$$I_{SET} \cong \frac{(V_S^- - V_R - 1.3\ V)}{(R_B + 12\ k\Omega)}$$

2. Connect lead 1 directly to V_R as described above. I_{SET} is then calculated by the equation given above, using a value $R_B = 300\ k\Omega$.

For nominal operation ($f_T = 1.5$ MHz internal $C_C = 15$ pF, choosing $V^+ = 6.2$ volts and $V_R = 0$, with $R_B \cong 300\ k\Omega$, gives $I_{SET} = 16\ \mu A$.

I_{SET} can also be established by an external circuit sink. This would allow switching the amplifier on and off, permitting dynamic control of gain-bandwidth, etc.

The total quiescent supply current, $I_{P_S^+}$, in lead 7 ≅ 12 I_{SET} with both amplifiers operating, and ≅ I_{SET} with only amplifier A operating.

Relationship Between Gain-Bandwidth Product, dc Bias Current, and Compensation Capacitance

Gain-bandwidth product, f_T, input bias current, I_{IB}, input offset current, I_{IO}, and the available output currents, I_O, are also roughly proportional to I_{SET}. For any I_{SET}, I_O is further limited by output transistor capabilities to about + 15 mA.

An approximate expression for gain-bandwidth product, using a compensation capacitor, C_C, either external or on-chip, is

$$f_T \cong 1.5\ \text{MHz} \left[\frac{I_{SET}}{16\ \mu A}\right] \left[\frac{15\ pF}{C_C}\right]$$

$C_C = 15$ pF is supplied on chip. I_{SET} values from 0.1 to 200 μA have been used. The lowest I_{SET} value permits operation with $I_{P_S^+}$ below 1.0 μA/amplifier. The highest I_{SET} value permits operation with $I_{P_S^+}$ below 1.0 μA/amplifier. The highest I_{SET} value permits $f_T \cong 15$ MHz, subject to the limitations following.

Limits On Loop-Gain Crossover Frequency With Internal Compensation

The LB1035AC is optimized for operation at a nominal $f_T \cong 1.5$ MHz. The internal compensation present to improve stablility margins in the nominal case, limits the maximum usable loop-gain crossover frequency with 1.5 MHz, unless external compensation is used. values of f_T above 1.5 MHz may be used if the closed-loop voltage gain, A_{VCL}, is greater than unity. The maximum usable f_T is

$$f_T\ (\text{maximum}) \cong 1.5\ \text{MHz}\ A_{VCL}$$

Compensation With External Capacitance

The use of external compensating capacitance, as shown in Figure 8, also removes the restriction on maximum loop-gain crossover frequency mentioned above. Bandwidths above 10 MHz with unity-gain stability have been obtained in this way.

External compensation capacitance is also useful in limiting bandwidth in noise-sensitive applications, or for improving stability margins when driving large capacitive loads (> 50 pF).

Frequency Characteristics

The open-loop-phase and gain curves ($C_C = C_{INT}$) show that for 40 dB closed-loop gain, the phase margin is approximately 90°.

With the internal feedback compensation, the normal 6 dB/octave roll-off is obtained. With this compensation, the amplifier configured as a unity gain amplifier will show little high-frequency peaking, and the step response will exhibit negligible overshoot or ringing.

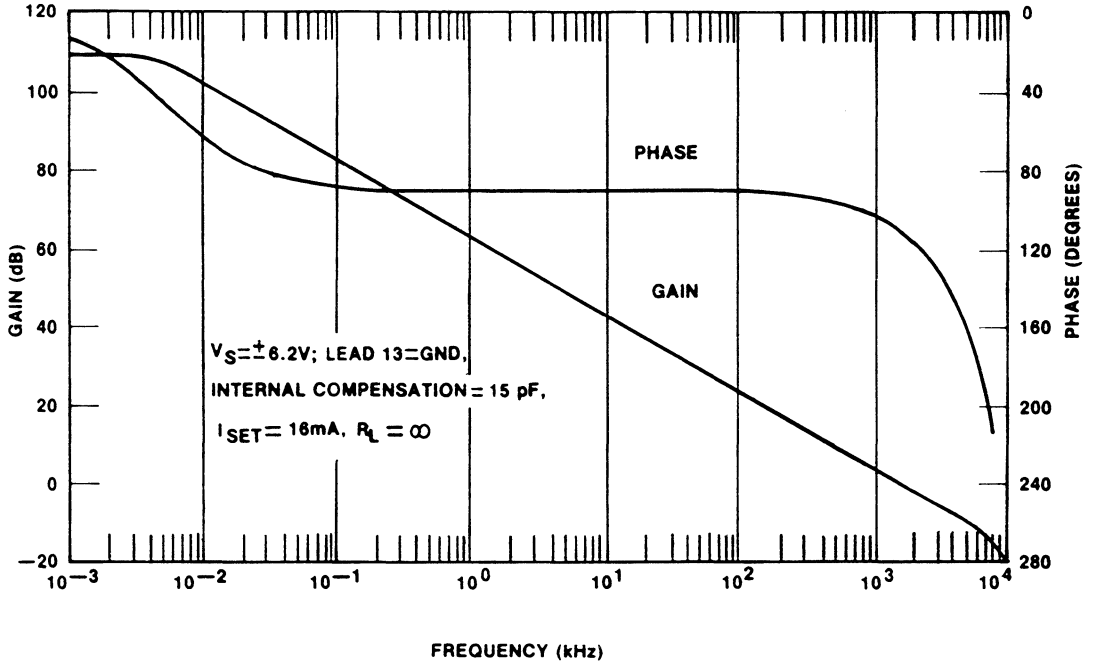
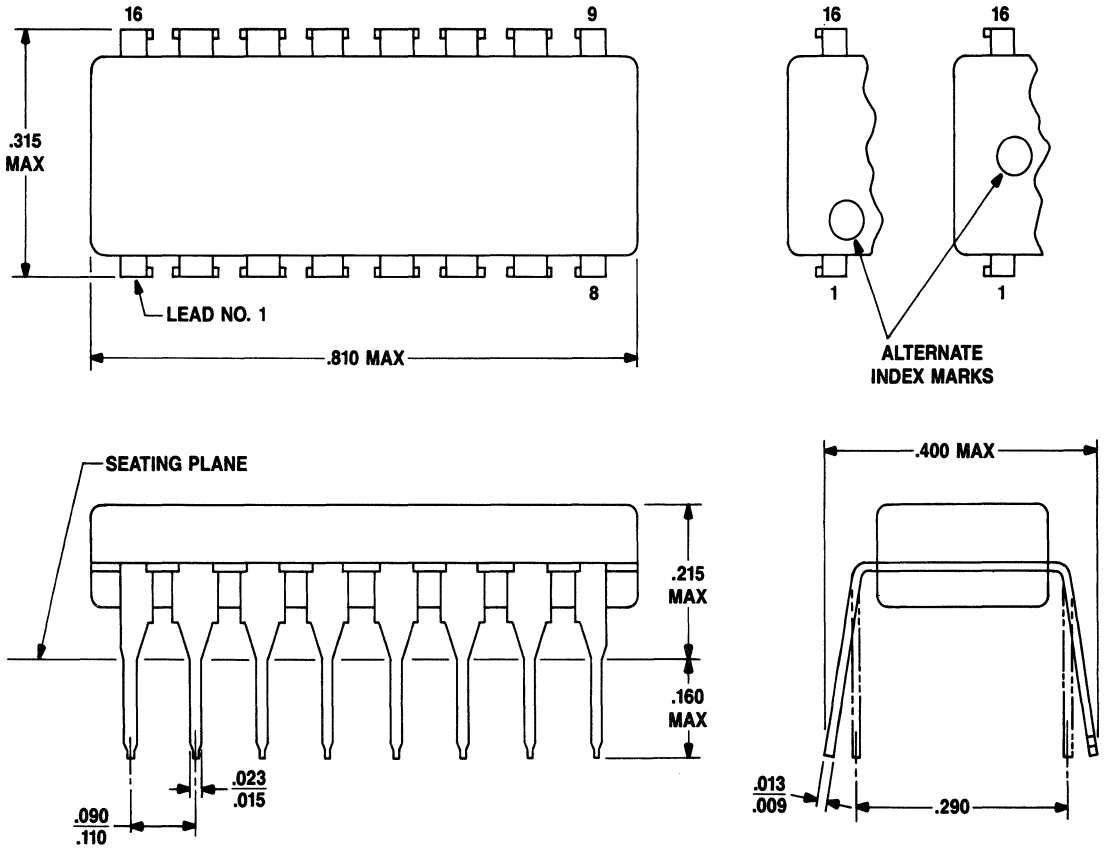


Figure 9. Typical Open-Loop Gain and Phase vs Frequency

Outline Drawing

(Dimensions in Inches)



Note 1: Pin numbers are shown for reference only.

Ordering Information

Device	Comcode
LB1035AC	104368113

DUAL GENERAL-PURPOSE VOICE-FREQUENCY OP-AMP LS1039BC

ADVANCE

Description

The LS1039BC is a dual voice-frequency operational amplifier for use in general-purpose applications where internal compensation is desired.

This device will provide good output current capability, short-circuit protection, offset voltage null capability, and large common-mode and differential voltage ranges. This integrated circuit will operate over the power-supply voltage range of ±8.0 to ±15 volts.

Features

- Extrapolated unity gain of 750 kHz
- Will not change polarity if input does not exceed V_{POS}
- Large common-mode voltage range
- Offset voltage null capability
- Short-circuit current limited
- 16-pin plastic DIP

Maximum Ratings (At 25°C unless otherwise specified)	
Supply Voltage Range (V− to V+)	30 V
Power Dissipation	600 mW
Storage Temperature Range	−40 to +125°C
Ambient Operating Temperature Range	0 to 100°C
Pin Soldering Temperature (t = 15 s max.)	300°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions

Pin	Name/Function	Pin	Name/Function
1	Negative Input Amp B	9	Positive Input Amp A
2	No Connection①	10	Offset Null Amp A
3	Output Amp B	11	Offset Null Amp A
4	V_{POS}	12	V_{NEG}
5	Output Amp A	13	Offset Null Amp B
6	No Connection①	14	Offset Null Amp B
7	No Connection①	15	No Connection①
8	Negative Input Amp A	16	Positive Input Amp B

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

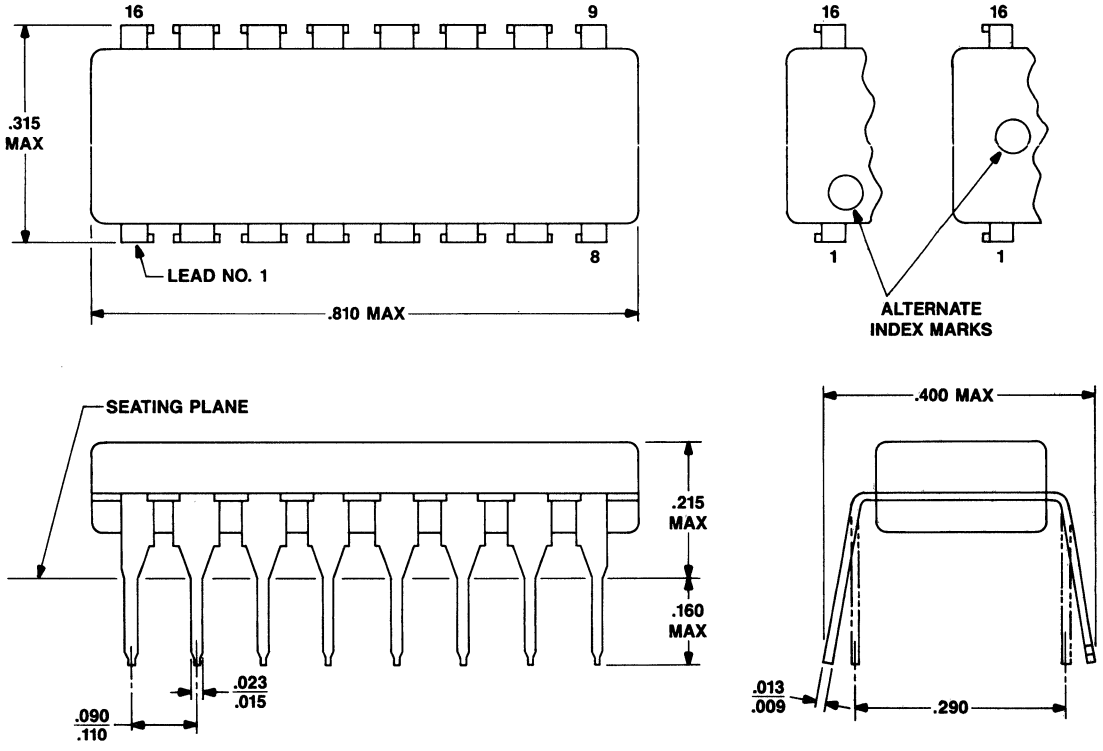
Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic and Test Condition	Min	Typ	Max	Unit
Open-Loop Voltage Gain f = 100 Hz	—	7500	17,000	
Input Offset Voltage	—	1.2	±4.5	mV
Input Bias Current	—	110	400	nA
Input Offset Current		8.0	±80	nA
Output Voltage Swing	±13.6 −13.0	11.2 −10.9	—	V(peak)
Common-Mode Voltage Range ($\triangle V_{IO}$ = 2.0 mV)	+14.0 −12.5	+12 −10	—	V
Common-Mode Rejection Ratio②	77	100	—	dB
Power-Supply Rejection Ratio	—	23	75	μV
Power-Supply Current	—	2.3	5.6	mA
Extrapolated Unity Gain Frequency (C_C = C_{INT})②	—	750	—	kHz
Output Current Drive (R_L = 100 Ω)	+15 −15	+20 −26	+60 −60	mA
Differential Mode Voltage Range②	—	24	—	V
Slew Rate (C_C = C_{INT} ≈ 25 pF)②	—	0.5	—	V/μs

① This lead is not internally connected and may be used as a tie point provided the maximum ratings of the device are not exceeded.
② This condition is not tested in production devices.

Outline Drawing

(Dimensions in Inches)



Note 1: Pin numbers are shown for reference only.

Ordering Information

Device	Comcode
LS1039BC	104368279

ADVANCE

Description

The LS1042AC/BC ICs are characterized as quad voice-frequency operational amplifiers with internal compensation. Each code (LS1042AC and LS1042BC) is a single wire-bonded chip comprised of four independent op-amps and a common substrate. These devices feature short-circuit protection and large common-mode and differential voltage ranges. The LS1042AC is specified for operation over the power-supply range of ±5.0 to ±9.0 volts, while the LS1042BC is specified for operation over the power-supply range of ±8.0 to ±15 volts.

Features

- Typical slew rate .5 V/μs guaranteed
- Unity-gain frequency minimum of 450 kHz
- Large common-mode voltage range
- 15 mA minimum output current capability
- Short-circuit current limited
- 16-pin plastic DIP

Maximum Ratings①
(At T_A = 25°C unless otherwise specified)

Supply-Voltage Amplifiers 1A, 1B, 2A, 2B	
(LS1042AC)	18V
(LS1042BC)	30 V
Total Power Dissipation	400 mW
Storage Temperature	−40 to +125°C
Operating Temperature Range	0 to +100°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

① The ratings specified are limiting values beyond which the serviceability of the device may be impaired from the viewpoint of life and satisfactory performance. Ratings, as such, do not constitute a set of operating conditions and all values may not, therefore, be attained simultaneously.

Pin Description

Pin	Name/Function	Pin	Name/Function
1	Negative Input, Amplifier 1B	9	Positive Input, Amplifier 2A
2	Output, Amplifier 1B	10	V_{NEG}, Amplifiers 2A, 2B
3	V_{POS1}, Amplifiers 1A, 1B	11	Positive Input, Amplifier 2B
4	Output, Amplifier 1A	12	Negative Input, Amplifier 2B
5	Output, Amplifier 2B	13	Negative Input, Amplifier 1A
6	V_{POS2}, Amplifiers 2A, 2B	14	Positive Input, Amplifier 1A
7	Output, Amplifier 2A	15	V_{NEG1}, Amplifiers 1A, 1B
8	Negative Input, Amplifier 2A	16	Positive Input, Amplifier B

Electrical Characteristics

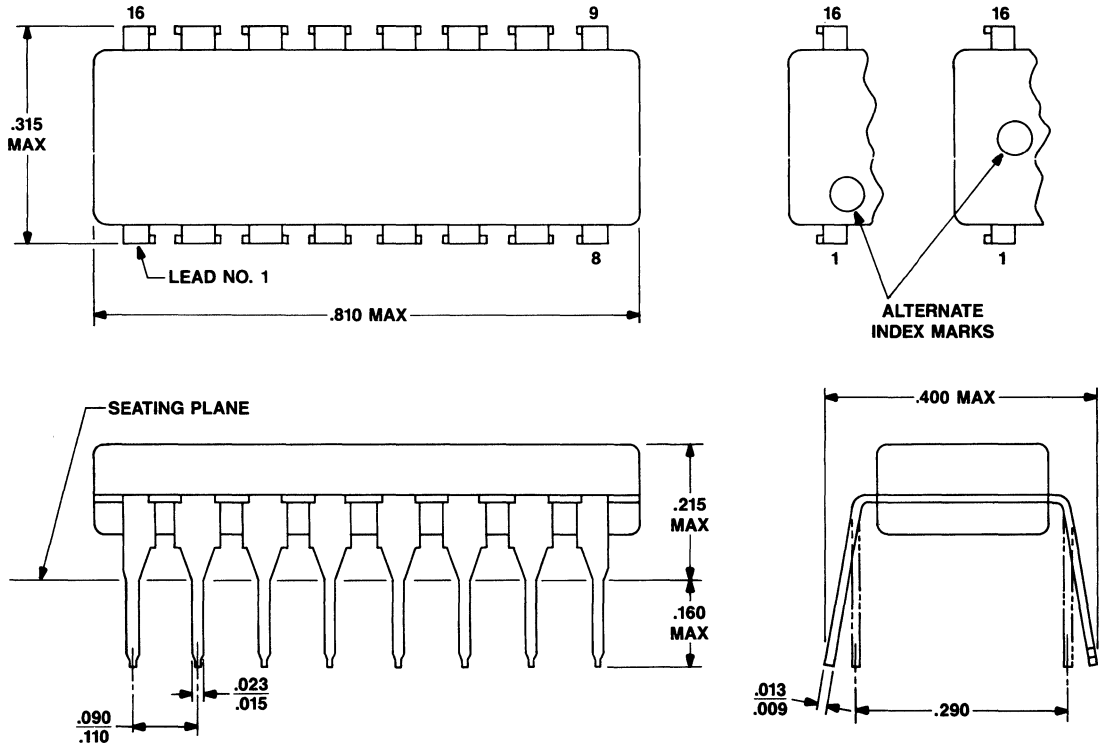
(T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic and Test Condition		Min	Typ	Max	Unit
Open-Loop Voltage Gain (R_L = 10 kΩ, f = 100 Hz, C_C = C_{INT})		4,500	—	17,000	—
Input Offset Voltage		—	—	±4.5	mV
Input Bias Current		—	—	400	nA
Input Offset Current		—	—	±80	nA
Output Voltage Swing (R_L = 10 kΩ)	(LS1042AC)	+7.6	—	—	V(PEAK)
	(LS1042AC)	−7.0	—	—	V(PEAK)
	(LS1042BC)	+13.6	—	—	V(PEAK)
	(LS1042BC)	−13.0	—	—	V(PEAK)
Output Current Drive (R_L = 100 Ω)		±15	—	±60	mA
Common-Mode Voltage Range ($\triangle V_{IO}$ = 2.0 mV)	(LS1042AC)	+8.0	—	—	V
	(LS1042AC)	−6.5	—	—	V
	(LS1042BC)	+14.0	—	—	V
	(LS1042BC)	−12.5	—	—	V
Common-Mode Rejection Ratio	(LS1042AC)	72	—	—	dB
	(LS1042BC)	77	—	—	dB
Power-Supply Rejection Ratio	(LS1042AC)	—	—	±125	μV
	(LS1042BC)	—	—	±75	μV
Power-Supply Current	(LS1042AC)	—	—	14	mA
	(LS1042BC)	—	—	11.2	mA
Slew Rate (C_C = C_{INT} ≈ 25 pF)		—	0.5	—	V/μs

Outline Drawing

(Dimensions in Inches)



Note 1: Pin numbers are shown for reference only.

Ordering Information

Device	Comcode
LS1042AC	104368345
LS1042BC	104368352

PRELIMINARY

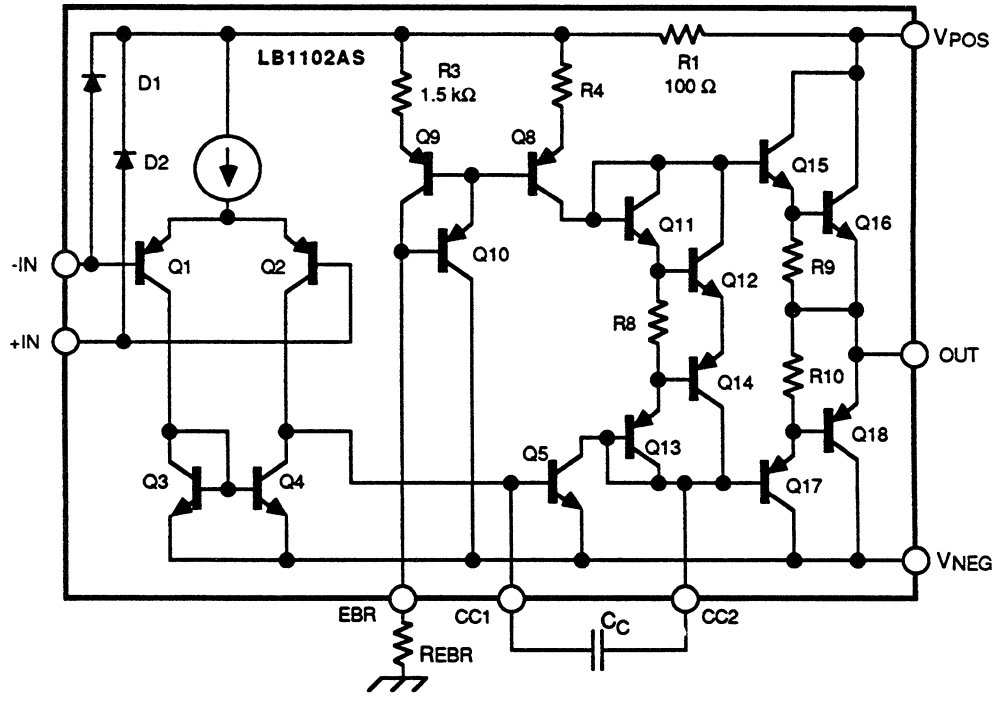
Description

The LB1102AB/AS Operational Amplifier combines the line driving capability of a high output current with a high gain-bandwidth product. The device features low quiescent current with operation over a power-supply voltage range of ±3.0 to ±15 volts. It also has the added advantage of having an input stage programmed with an external resistor. The user is able to obtain optimum performance for each individual application with this feature. Applications include servo amplifiers and drivers, high input impedance audio amplifier dc-to-dc converters, precision power comparators and motor speed controls. This device is available as an LB1102AB in an 8-pin DIP package and as an LB1102AS in an 8-pin surface-mount package.

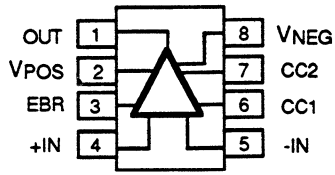
Features

- Typical unity gain frequency of 30 MHz (open loop, compensated)
- Electronic shutdown capability
- Internal static discharge protection
- Wideband performance optimized for closed-loop gains > 20 dB up to 15 MHz
- Externally programmable input stage
- Capable of sinking or sourcing an output current to ±150 mA (peak)

Functional Diagram



Pin Diagram



Surface Mount

Maximum Ratings

(TA = 25°C unless otherwise specified)

Ambient Operating Temperature Range	0 to +85°C
Storage Temperature Range	−40 to +125°C
Pin Soldering Temperature (t = 15 sec max.)	300°C
Differential Mode Input Voltage	±6 V
Supply Voltage Range (VPOS-to-VNEG)	30 V
Output Current	±150 mA(peak)
Maximum Power Dissipation	400 mW

Stresses in excess of those listed under "MAXIMUM RATINGS" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Description

Pin	Symbol	Name/Function
1	OUT	Output capable of sinking or sourcing peak currents to ±150 mA (peak). See output on Functional Diagram schematic.
2	VPOS	The more positive supply voltage is connected to this pin.
3	EBR	External Bias Resistor and shutdown control. Biasing this lead to a voltage approaching VPOS will cause the device to shutdown. Varying the current in this lead permits control of the effective bandwidth capability of the device, at a constant closed loop gain. A dc bias current must be drawn from Pin 3 for the LB1102A-Type to operate. A resistor (REBR) is connected from this pin to a lower fixed reference potential, VREF; VREF is usually the Ground or VNEG potential. Normal operation for the current through REBR (hereafter described as ISET) is: $I_{SET}\ (normal) = \frac{(V_{POS} - V_{REF} - 1.3)}{(R_{EBR} + 1.5\ k\Omega)} = 250\ \mu A$
4 5	+IN −IN	Non-inverting and inverting inputs respectively (see Figure 1). The voltage difference between these pins should not exceed 6.0 volts.
6 7	CC1 CC2	Pins for connecting an external capacitor (CC) to provide feedback compensation. CC < 1.0 pF is not recommended (see Feedback Compensation discussion).
8	VNEG	The more negative supply voltage is connected to this pin.

Table 1—Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Positive Supply Voltage (V_{POS} - to - Ground)	3.0	12	15	V
Negative Supply Voltage (V_{NEG} - to - Ground)	−3.0	−12	−15	V
Output Current (Source or Sink)	—	—	150	mA (peak)
Differential Mode Input Voltage	—	—	±6.0	V

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic	Test Condition	Min	Typ	Max	Unit
V_{POS} Supply, Quiescent Current (Figure 1)	V_{POS} = 12 V; V_{NEG} = 12 V R_{EBR} = 40.2 kΩ (±1.0%)	1.65	1.80	2.10	mA
	V_{POS} = 15 V; V_{NEG} = 15 V R_{EBR} = 51.9 kΩ (±1.0%)	1.65	—	2.25	mA
V_{NEG} Supply, Quiescent Current (Figure 1)	V_{POS} = 12 V; V_{NEG} = 12 V R_{EBR} = 40.2 kΩ (±1.0%)	−1.40	—	−1.85	mA
	V_{POS} = 15 V; V_{NEG} = 15 V R_{EBR} = 51.9 kΩ (±1.0%)	−1.40	—	−2.00	mA
Power Supply, Leakage Current (Figure 2)	V_{POS} = 15 V; V_{NEG} = 15 V R_{EBR} = 40.2 kΩ (±1.0%)	—	—	±20	μA
Open Loop Voltage Gain (A_{VOL}) (Figure 3)	V_{POS} = 12 V; V_{NEG} = 12 V f = 150 kHz C_C = 9.0 pF	52	—	62	dB
Output Voltage Swing (Figure 4)	R_L = 2.0 kΩ V_{POS} = 12 V; V_{NEG} = 12 V				
V_{OH}	V_{IN} = −100 mV	9.70	10.0	—	V
V_{OL}	V_{IN} = +100 mV	−9.70	−10.5	—	V

Electrical Characteristics
(Continued)

Characteristic	Test Condition	Min	Typ	Max	Unit
Output Voltage Swing, Current Limiting (see Note 1)	Figure 4; R_L = 30 Ω V_{POS} = 10 V; V_{NEG} = 10 V				
V_{OH}	V_{IN} = 100 mV	4.50	6.60	—	V
V_{OL}	V_{IN} = +100 mV	−4.50	−6.60	—	V
Power Supply Rejection Ratio	Figure 5	88	94	—	dB
Input Offset Voltage (V_{IO})	Figure 6	—	±1.0	±4.5	mV
Input Bias Current (I_{IB})	Figure 7	—	3.0	6.0	μA
Input Offset Current (I_{IO})	Figure 7	—	±0.2	±1.0	μA
Common-Mode Voltage Range	Figure 8; Vcm = ±2.0 mV				
Positive		10.0	—	—	V
Negative		11.5	—	—	V
Common-Mode Rejection Ratio	Figure 8; Vcm = ±2.0 mV	74	94	—	dB

Test Circuits
(See Note 1)

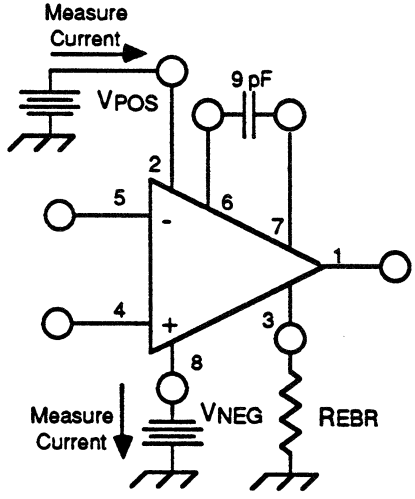


Figure 1. Power Supply Quiescent Current

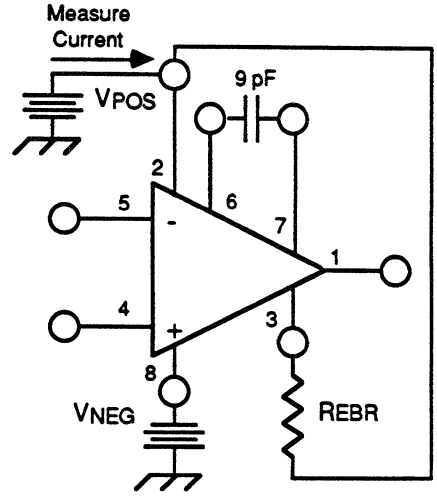
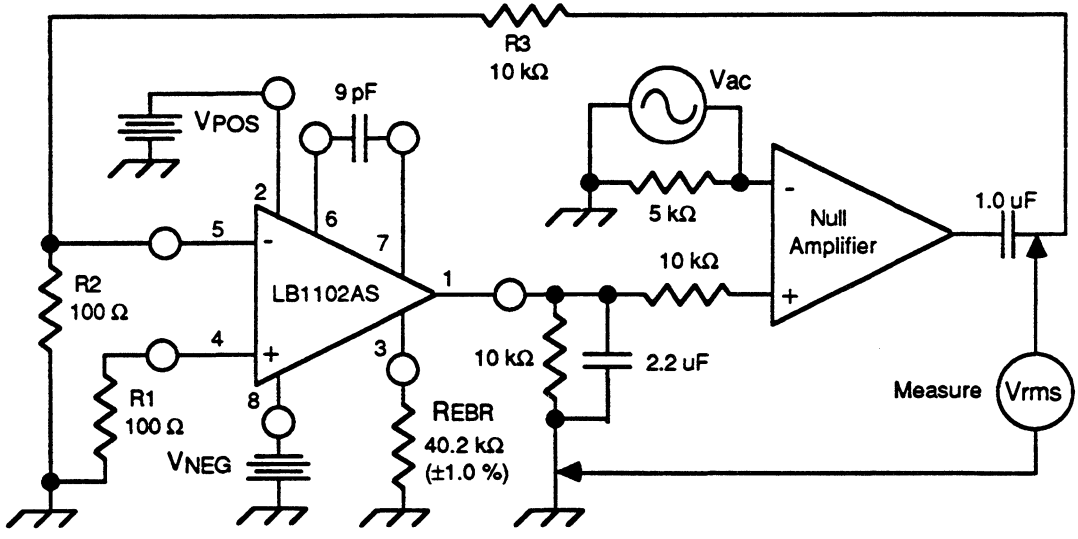


Figure 2. Power Supply Leakage Current

Note 1: All power supply rails should be bypassed with capacitors of 0.1 μF or greater. These capacitors should be connected as close as possible to the appropriate pin.

Test Circuits (Continued)
(Note 1)



$$\text{GAIN (dB)} = 20\,[\text{Lo}\,(K\frac{\text{Vrms}}{\text{Vac}})]; \text{ where } K = \frac{R2 + R3}{R2}$$

Figure 3. Open Loop Voltage Gain Test Circuit

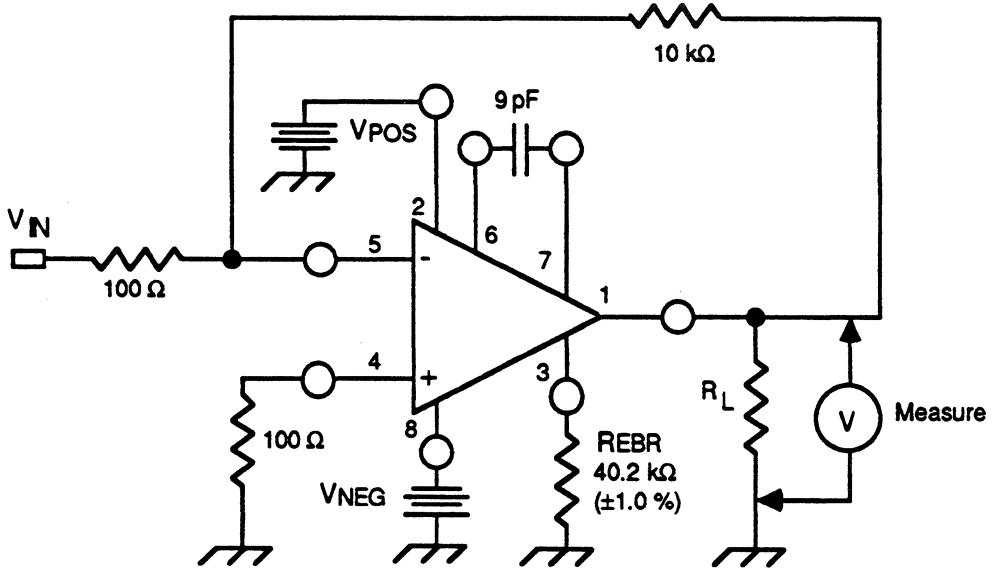
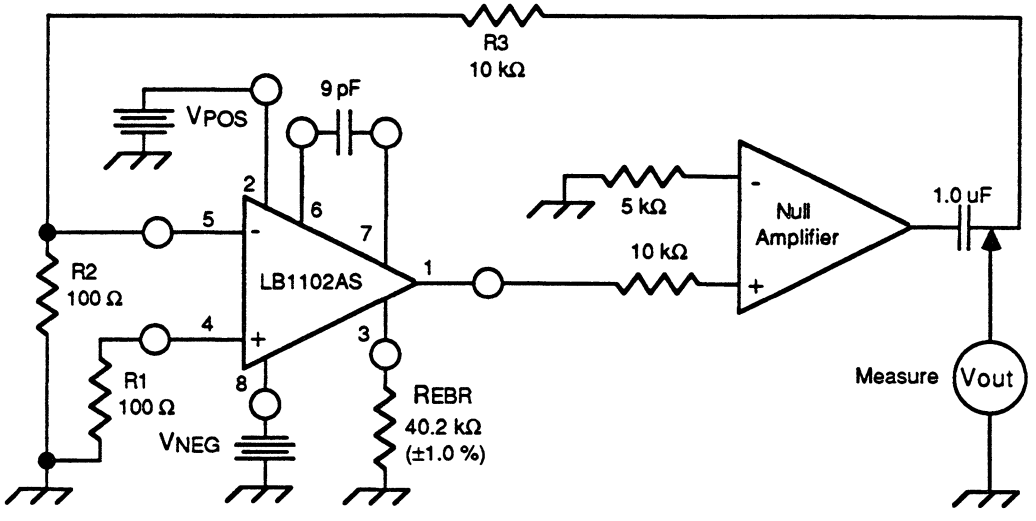


Figure 4. Output Voltage Swing Test Circuit

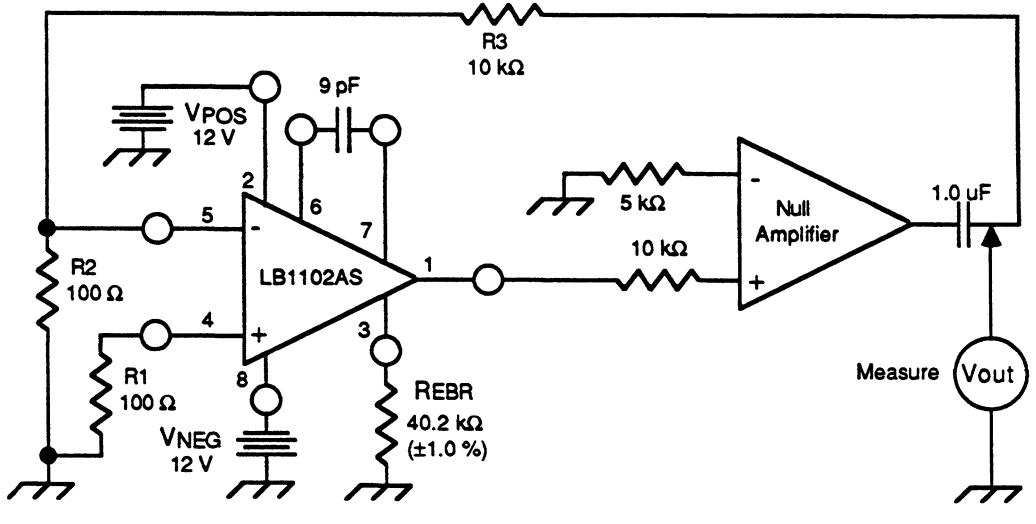
Test Circuits (Continued)
(Note 1)



PSRR (dB) $= 20\,[\text{Log}\frac{\triangle\text{Vout}}{\text{K}(\triangle\text{Vsupply})}]$; where $\text{K} = \frac{\text{R2} + \text{R3}}{\text{R2}}$;

△Vsupply = 5.0 volts (Positive and Negative power supplies are simultaneously varied from 12 volts to 7.0 volts.

Figure 5. Power Supply Rejection Ratio

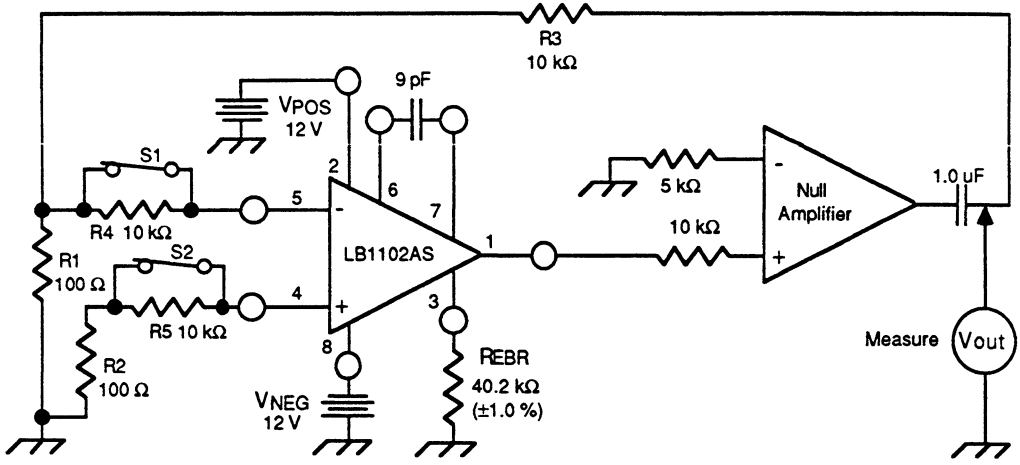


Input Offset Voltage $= \frac{\text{Vout}}{\text{K}}$; where $\text{K} = \frac{\text{R2} + \text{R3}}{\text{R2}}$;

Figure 6. Input Offset Voltage

Test Circuits(Continued)

(Note 1)



Input Bias Current Measurement

Step 1: Measure Vout with S1 and S2 closed (V1).
Step 2: Measure Vout with S1 open and S2 closed (V2)

$\triangle V3 = V1 - V2$

$IB1 = \triangle V3/(K)\ (R4)$

Step 3: Measure Vout with S2 open and S1 closed (V4).

$\triangle V5 = V1 - V4$

$IB2 = \triangle V5/(K)\ (R5)$

$$\text{Input Bias Current} = \frac{IB1 + IB2}{2}$$

$$\text{where } K = \frac{R2 + R3}{R2}$$

Input Offset Current Measurement

Step 1: Measure Vout with S1 and S2 closed (V6).
Step 2: Measure Vout with S1 and S2 open (V7).

$\triangle V8 = V6 - V7$

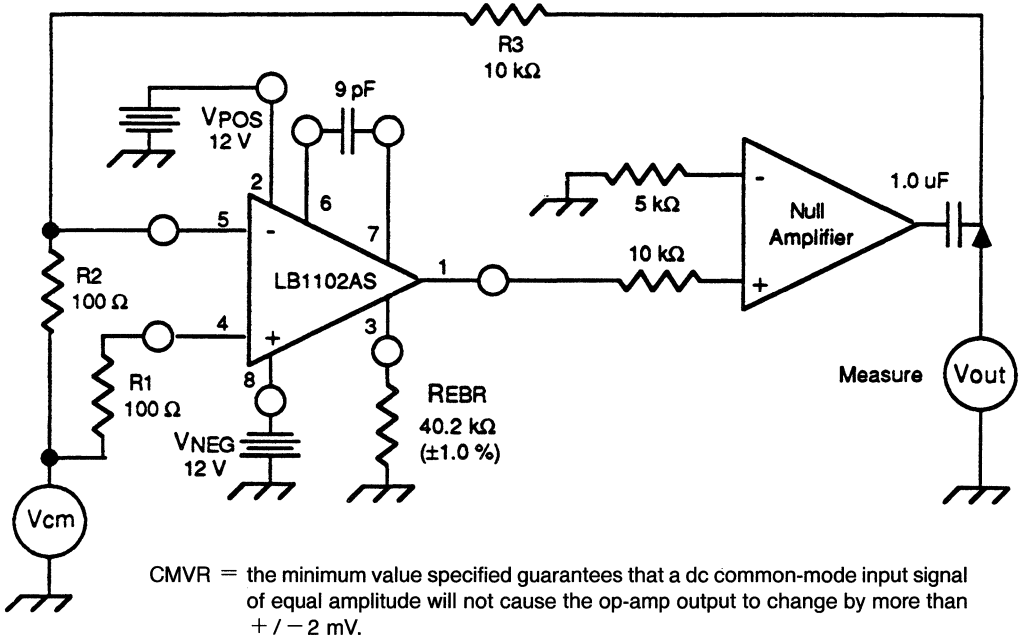
$$\text{Input Offset Current} = \frac{\triangle V8}{(K)\ (R4)} \text{ ; where R4 = R5}$$

$$\text{where } K = \frac{DR2 + R3}{R2}$$

Figure 7. Input Bias And Input Offset Current

Test Circuits (Continued)

(Note 1)



CMVR = the minimum value specified guarantees that a dc common-mode input signal of equal amplitude will not cause the op-amp output to change by more than +/−2 mV.

$$\text{Common-Mode Rejection Ratio (dB)} = 20\,[\text{Log}\,\frac{\triangle V_{CM}}{\triangle \text{ out}}$$

Figure 8. Common-Mode Voltage Range and Common-Mode Rejection Ratio Test Circuit

Typical Electrical Characteristics

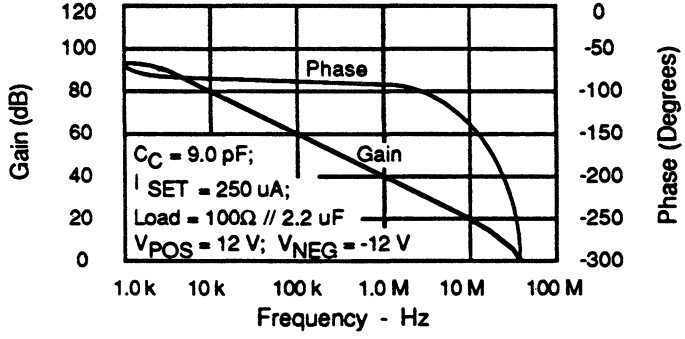


Figure 9. Open Loop Gain and Phase vs Frequency

Typical Electrical Characteristics
(Continued)

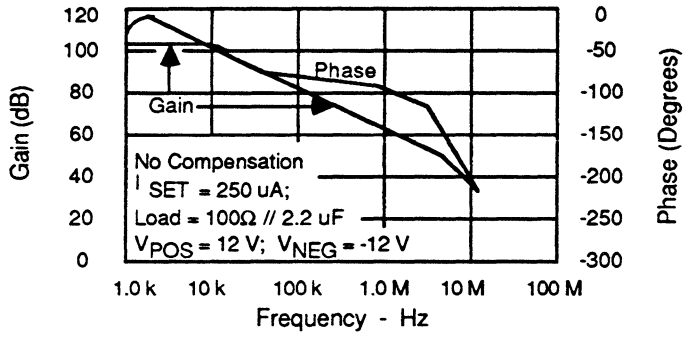


Figure 10. Open Loop Gain and Phase vs Frequency

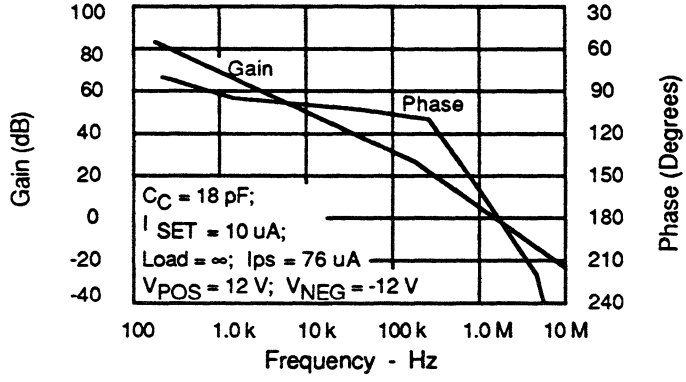


Figure 11. Open Loop Gain and Phase vs Frequency

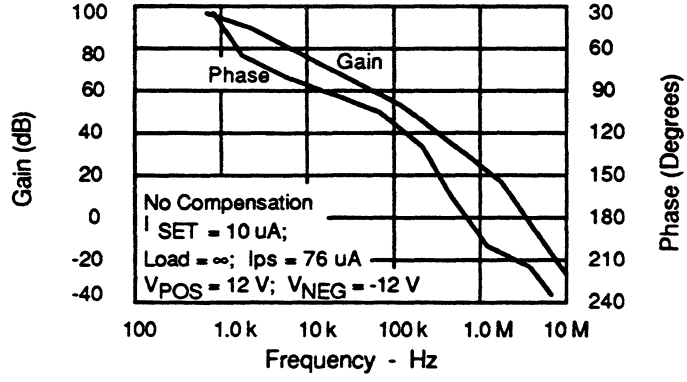


Figure 12. Open Loop Gain and Phase vs Frequency

Feedback Compensation

The amplifier gain of the LB1102AB/AS exhibits a single-pole (1/f) frequency response when capacitive feedback compensation is used. The unity gain bandwidth product (f_t) depends on I_{SET} and C_C (measured in pF):

$$f_t(\text{in MHz}) = \left[\frac{1000}{(C_C + 0.8)}\right]\left[\frac{I_{SET}}{250\ \mu A}\right]$$

The amplifier must be compensated so that its feedback loop gain is reduced below unity at a frequency limit (f_L) not higher than

$$f_L(\text{in MHz}) = 15\left(\frac{I_{SET}}{250\ \mu A}\right)$$

Conservative designs will have loop gain crossover at a frequency which is lower than f_L by a factor of two or greater.

For a given closed loop gain (A_V), a suggested minimum C_C to assure stability is:

$$C_C(\text{in pF}) = 90/A_V$$

Phase margins may be improved by adding a small value of resistance (R_C) in series with C_C (operation with $C_C < 1.0$ pF is not recommended as phase margins may be unacceptably low). R_C may be chosen so that it is approximately equal to the reactance of C_C (at a point which is three times the loop gain crossover frequency f_t/A_V). Therefore, at a desired bandwidth of 11 MHz and unity gain:

$$R_C = \frac{1}{(2\pi)\ (3\ f_t)\ (C_C)} = 54\Omega$$

Using all of the above equations, calculations can be made to show that the LB1102AB/AS is capable of providing a useful wideband, unity gain, buffer amplifier at the following conditions:

$I_{SET} = 250\ \mu A$, $C_C = 90$ pF, $R_C = 54\ \Omega$ and $f_t = 11$ Mhz

In general, the following application conditions lead to lower stability margins:

Large capacitive loads (C_L): where C_L (in pF) > [5.0 I_{SET} (in μA)] [A_V/f_t (in MHz)]

High Source Resistances (R_S) in ohms: where R_S > 15,000 [A_V/f_t (in MHz)]

Low Power-Supply Voltages: where $V_{POS} < 3.0$ V; $V_{NEG} < -3.0$ V

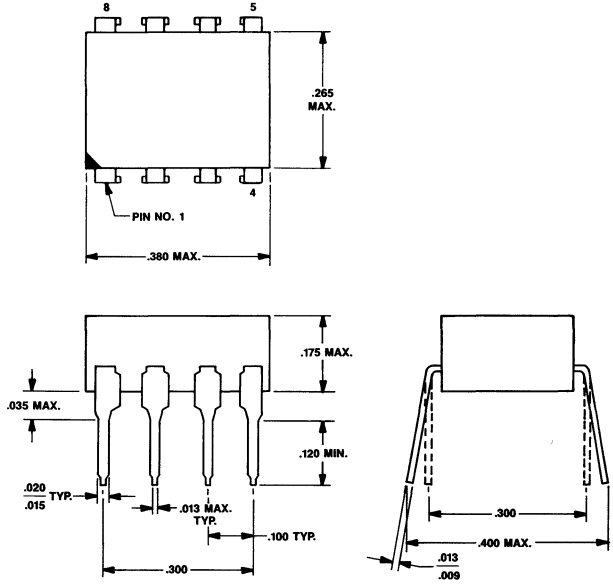
A large compensation capacitor (C_C) may be needed in order to assure stability when the above application conditions are encountered.

Slew rates for LB1102AB/AS devices with capacitive feedback compensation are approximately as follows:

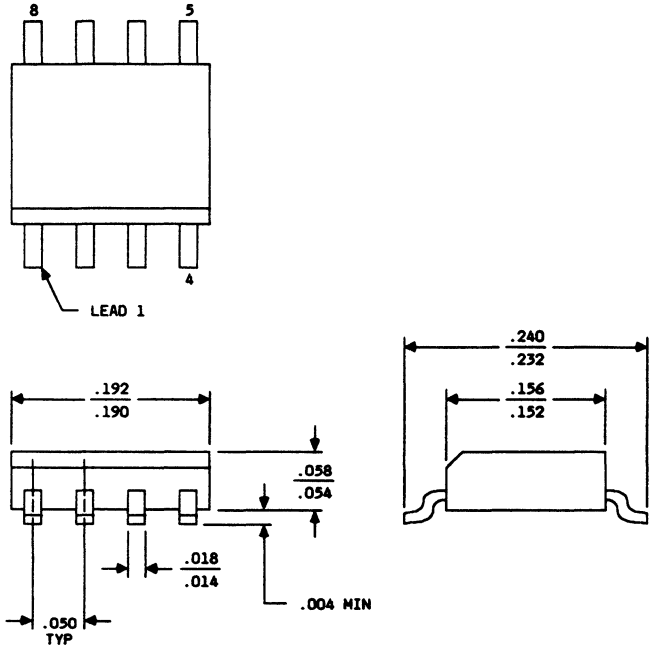
$$\text{Slew Rate } (V/\mu s) = \frac{2\ I_{SET}\ (\text{in } \mu A)}{C_C\ (\text{in pF})}$$

Outline Drawings (Dimensions in Inches)

8-Pin DIP



8-Pin SONB



Ordering Information

Device	Comcode
LB1102AB	104434105
LB1102AS	104407382

ADVANCE

Description

The LB1108AD is an internally compensated, high-voltage dual operational amplifier. It is similar in performance to the LB1013AD, except that it has internal current limiting and thermal shut-down features. Provisions are provided to accommodate separate positive supply voltages for the input stages (V_{S1}) and the output stages (V_{S2}). This connection configuration allows for higher common-mode input voltage swing and provides higher output currents for telephone line applications.

Each amplifier output can sink or source up to 60 mA, and will operate in the temperature range of $-40°C$ to $+85°C$. The output voltage swing is typically 2.0 volts from the power-supply voltage.

An optional powerdown feature is available for applications requiring minimum standby power.

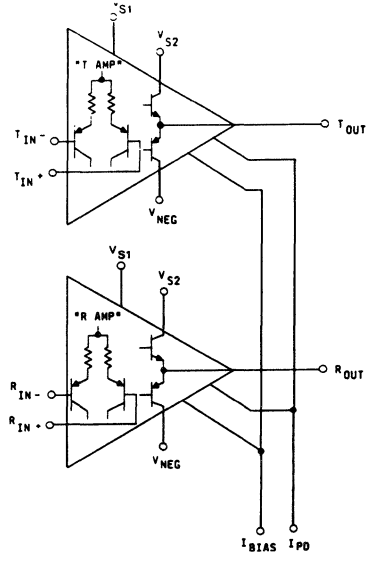
Features

- Audio band operation: typically F_T = 3.0 MHz; Gain = 70 dB @ 1.0 kHz
- Single-supply operation; 5.0 to 85 V; Dual-supply operation; ±2.5 to ±42.5 V
- Output voltage swing to within 2.0 volts of supply voltage rails
- Internal circuitry provides output overload protection @ 70 mA
- Thermal shut-down protection on-chip temperature range of 150°C to 160°C

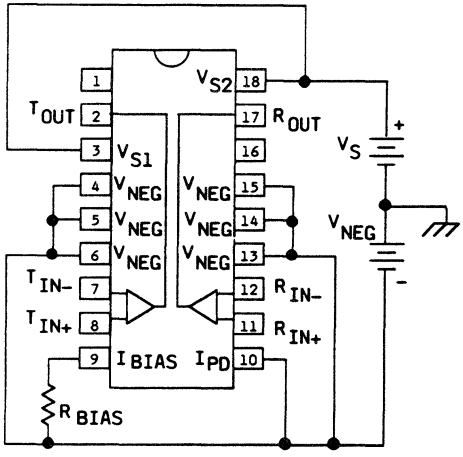
Applications

- Telephone line feed
- Power supplies
- Voltage followers
- Industrial control systems
- High-voltage regulators
- Audio amplifiers
- Resolve excitation
- Signal conditioning
- General-purpose, high-voltage circuits

Functional Diagram



Pin Diagram



Maximum Ratings (At 25°C unless otherwise specified)	
Ambient Operating Temperature Range	−40 to +85°C
Storage Temperature Range	−40 to +150°C
Pin Soldering Temperature (t = 15 s max.)	300°C
Voltage (Vs to VNEG)	85 V
Current (Each Amplifier Output)	70 mA
Maximum Power Dissipation	2 W

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Thermal Data

(Power DIP and SOJ to be determined)

Pin Description

(**Caution:** Final version pinouts may change)

Pin	Symbol	Name/Function
1,16	NC	No connection (do not use as an external tie point).
2 17	TOUT ROUT	These pins are the op-amp outputs for the "T" Amplifier and the "R" Amplifier respectively.
3	VS1	The most positive supply-voltage is connected to this pin. This is the supply for the input stage and can be more positive than VS2 to allow higher common-mode voltages.
4,5,6, 13,14,15	VNEG	The more negative supply-voltage is connected to these pins. These pins are internally connected together. Maximum thermal conductivity may be obtained by providing external connections to each of these pins from the VNEG power-supply.
7 8 12 11	TIN − TIN + RIN − RIN +	These pins are the inverting and noninverting inputs, respectively, for both the "T" Amplifier and the "R" Amplifier.
9	IBIAS	Bias current of 40 μA must be pulled from this pin to activate the amplifiers. The amplifiers will be in an undetermined state if this pin is left open.
10	IPD	User controlled shutdown (power down) pin. A current of 40 μA should be pulled out of this pin to deactivate the amplifiers. The amplifier outputs will float when shutdown is accomplished via this pin. If this feature is not desired, the IPD pin can be connected to VS1.
18	VS2	This is the positive supply for the output stage. This pin may be connected to a lower voltage than VS1 (such as ground in telephone line feed applications), where higher line currents are required.

Electrical Characteristics

(Unless otherwise specified, T_A = 25°C, V_{S1} = 41.5 V, V_{S2} = 41.5 V, V_{NEG} = 41.5 V, I_{PD} = connected to V_{S1}, I_{BIAS} = −40 μA; Tests apply individually to both the "T" Amplifier and the "R" Amplifier except where otherwise indicated)

Characteristic and Conditions	Test Condition	Min	Max	Unit
Output Voltage Swing, Positive	V_{IN} = −0.5 V, See Figure 1	39.5	—	V
Output Voltage Swing, Negative	V_{IN} = +0.5 V, See Figure 1	−39.5	—	V
Output Voltage Swing, Positive (Current Limiting)	V_{S1} = V_{S2} = 5.0 V V_{NEG} = −5 V V_{IN} = −0.5 V See Figure 1	0.7	2.0	V
Output Voltage Swing, Negative (Current Limiting)	V_{S1} = V_{S2} = 5.0 V V_{NEG} = −5.0 V V_{IN} = +0.5 V See Figure 1	−0.7	−2.0	V
Power-Supply Current (Amplifiers On)	V_{IN} = +0.5 V, Measure I_{VS} V_{IN} = −0.5 V, Measure I_{VNEG} See Figure 2	— —	2.5 −2.5	mA mA
Power-Supply Current (Shutdown)	I_{PD} = −40 μA Measure I_{VS} Measure I_{VNEG} See Figure 2	 128 −128	 500 −500	 μA μA
Output Source Current	V_{LOAD} = −35 V V_{IN} = +0.5 V, See Figure 3	60	—	V
Output Sinke Current	V_{LOAD} = +35 V V_{IN} = −0.5 V, See Figure 3	60	—	V
Output Leakage Current	I_{PD} = −40 μA, See Figure 4 V_{LOAD} = +35 V V_{LOAD} = −35 V	 — —	 ±10 ±10	 μA μA
Open-Loop Voltage Gain	f = 100 Hz f = 1 kHz	10000 2000	— 5500	— —
Input Offset Voltage	—	—	±15	mV
Input Bias Current	—	—	±4.0	μA
Input Offset Current	—	—	±0.8	μA
Power-Supply Rejection Ratio	—	—	100	μV/V
Common-Mode Rejection Ratio	—	80	—	dB

Simplified Test Circuits

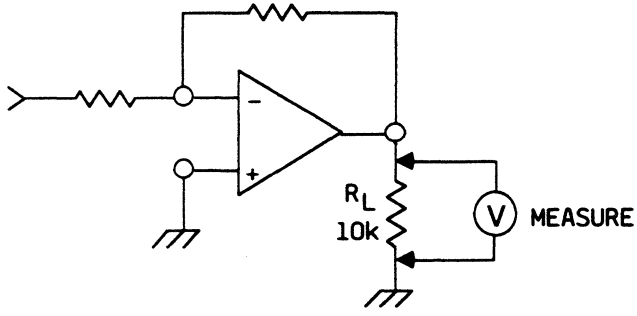


Figure 1. Test Circuit, Output Voltage Swing

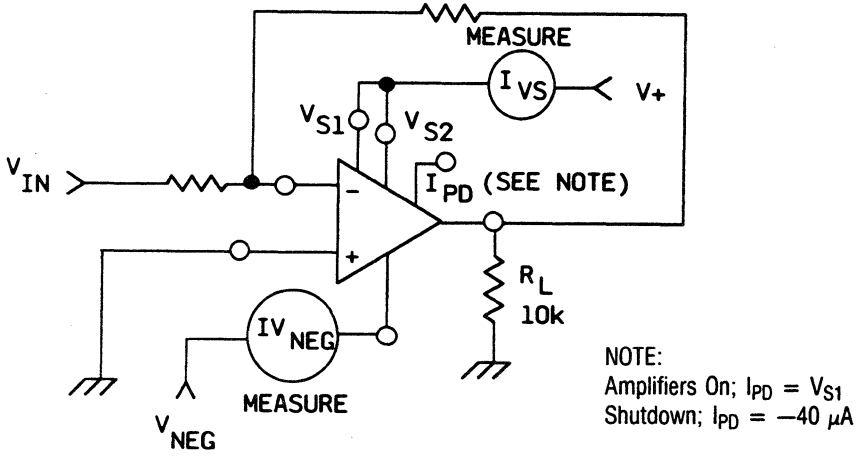


Figure 2. Test Circuit, Power-Supply Current

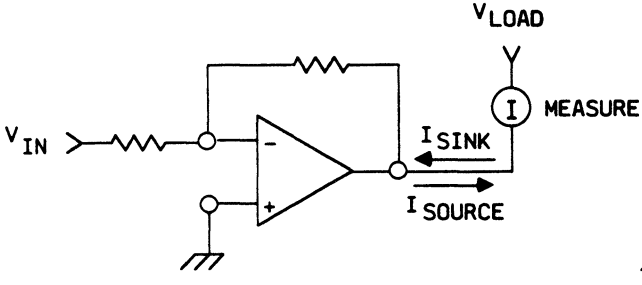


Figure 3. Test Circuit, Output Current

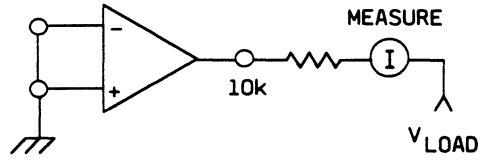


Figure 4. Test Circuit, Output Leakage Current

Characteristics

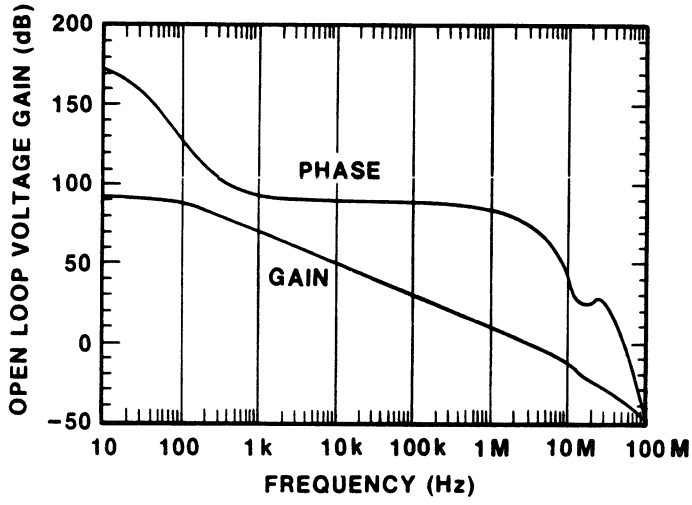


Figure 5. LB1108AD Open-Loop Frequency and Phase Response

Applications

Pin Diagram (page 1) shows a simple connection. Vs and V_{NEG} can be provided either by dual or single power supplies. The common-mode input voltage range of this configuration does not include either Vs and V_{NEG}. R_{BIAS} is selected to meet the requirements.

$$R_{BIAS} \text{ (in megohms)} \geq (V_S - V_{NEG})/40$$

Figure 6 shows connections with Vs1 connected to 5.0 volts, Vs2 returned to ground and V_{NEG} connected to the negative supply. This configuration permits an input common-mode range which includes ground.

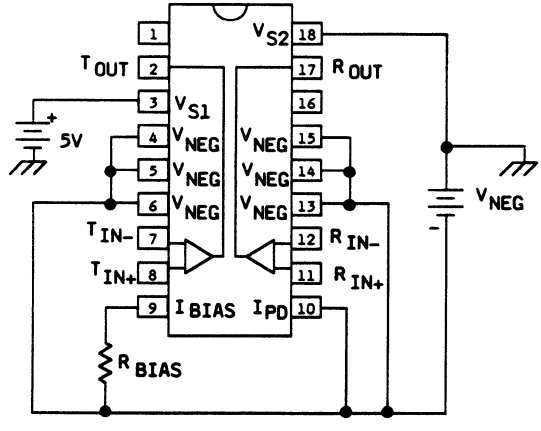


Figure 6. LB1108AD Op-Amp (Ground Return Connections)

Applications
(Continued)

Figure 7 shows connections to achieve a transconductance configuration for telephone line drive applications.

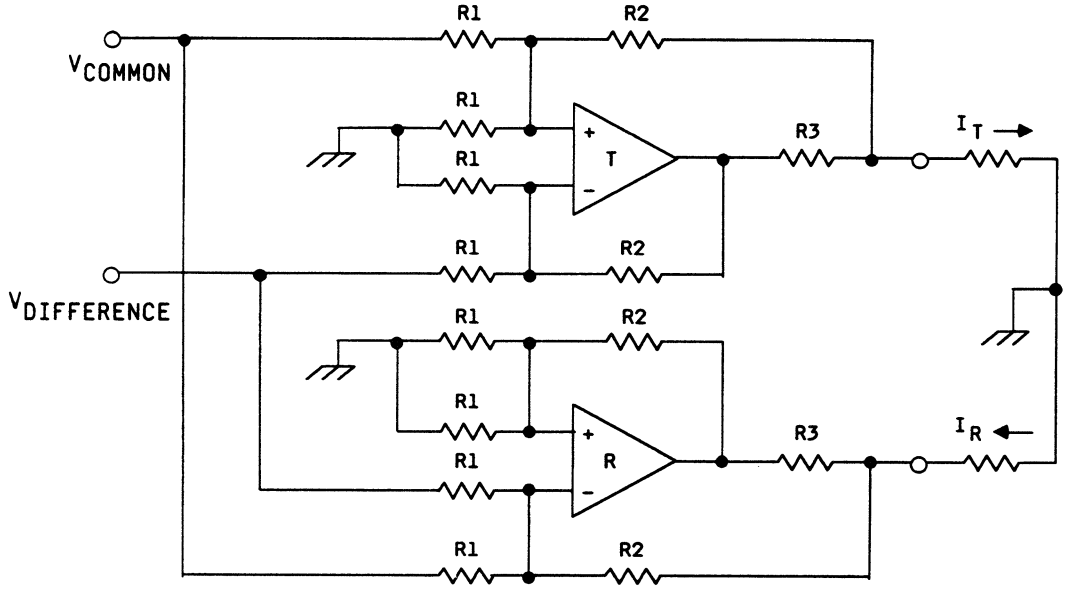


Figure 7. Simplified Line Feed Operation (Power-Supply Connections Not Shown)

Ordering Information

Device	Comcode
LB1108AD	104411145

REGULATION CONTROL CIRCUIT LBR FAMILY

Description

The Regulation Control Circuit LBR Family consists of integrated circuits which provide three useful power supply function (see Applications) in the same package: a voltage regulator, a precision 1.25 V reference, and a high-speed comparator. Each device accepts an unregulated dc supply voltage ranging from 4 V to 26 V and provides two fixed outputs: a 1.25 V reference voltage, common to each device code in this family; and a customer specified regulation voltage, ranging from 2 V to 24 V, fixed at time of manufacture. Refer to Ordering Information (last page) for a detailed coding description.

These devices are available in 16-pin packages (Functional Diagram) which allow a designer to customize several circuit configurations. These devices are also available in 8-pin packages (Functional Diagram) with a fixed configuration.

Features

Voltage Regulator

- Fixed values between 2 V and 24 V (±1%)
- Less than 1% change over combined temperature and supply voltage ranges:
  $-40°C \leq T_A \leq +100°C$
  $4\ V \leq V+ \leq 26\ V$

High-Speed Comparator

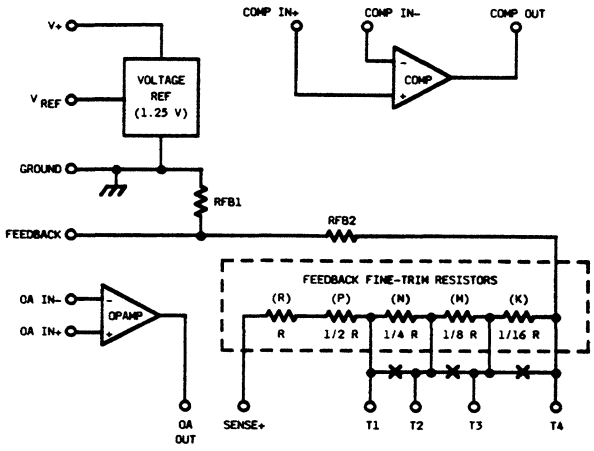
- Referenced to 1.25 V
- Propagation delay < 150 ns
- Input offset < 5 mV (−40 to +100°C)
- Output loading to 10 mA maximum

Precision Low-Voltage Reference

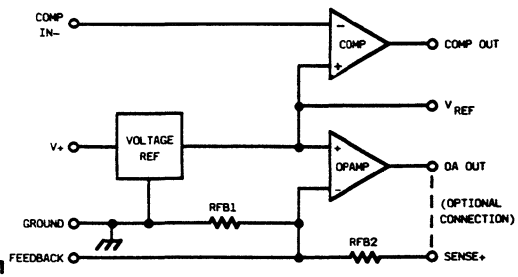
- 1.25 V (±1%) from 4- to 26-Volt Supply
- Temperature coefficient
  < 50 ppm/°C (−40 to +100°C)
- 4-Volt minimum V+ operation
  (−40 to +100°C)
- Capacitive operation to 100 pF maximum
- Current loading to ≤ 10 mA
- Excellent power supply rejection ratio (PSRR) 70 dB @ dc; 40 dB @ 1 MHz
- Fast transient start-up time

Functional Diagrams

16-Pin Package



8-Pin Package



Pin Diagrams (See Notes 1 & 2 on page 5.)

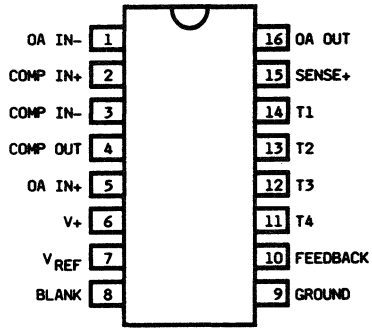


Figure 1. 16-Pin Surface Mount (SOJ)

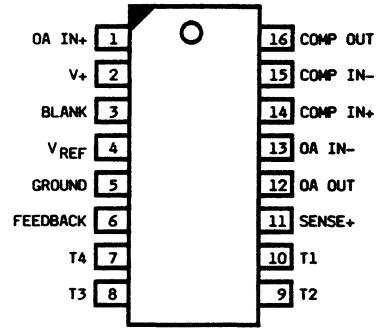


Figure 2. 16-Pin Plastic DIP

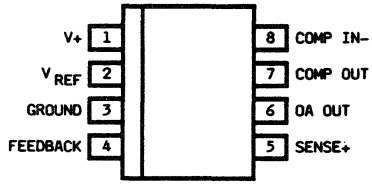


Figure 3. 8-Pin Surface Mount (SOIC)

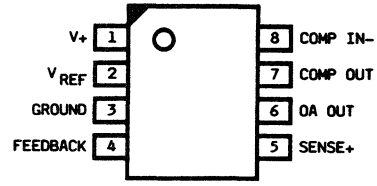


Figure 4. 8-Pin Plastic DIP

Pin Descriptions (See Notes 1 & 2 on page 5.)

Pin No.	Name	Description
6	V+	Supply Voltage (4- to 26-volt)
8	BLANK	This pin may be used as a tie-point for external components. Maximum Voltage = 30 V
9	GROUND	Circuit common (not necessarily system or physical ground).
7	VREF	1.25 V Reference Output
3	COMP IN –	Inverting Comparator Input
2	COMP IN +	Non-Inverting Comparator Input. Connected to VREF on 8-Pin Packages.
4	COMP OUT	Comparator Output, Open Collector. Requires pull-up resistor.
1	OA IN –	Inverting Op-Amp Input. Connected to FEEDBACK on 8-Pin Packages.
5	OA IN +	Non-Inverting Op-Amp Input. Connected to VREF on 8-Pin Packages.
16	OA OUT	Op-Amp Output.
10	FEEDBACK	Connection to feedback resistors. Connected to OA IN – on 8-Pin Packages.
15	SENSE +	Positive Sense Node. Normally connected to OA OUT in regulator applications.
14 13 12 11	T1 T2 T3 T4 (See Functional Diagram)	These trim links are normally factory trimmed as required to provide the desired voltage regulator output. However, some applications may require additional fine-tuned trimming to account for offset voltages in customer systems. Devices can be ordered which are trimmed to a value within several millivolts of a customer's desired value. The customer is then responsible for final trimming. (This option not available in 8-Pin Packages.)

Maximum Ratings (At 25°C unless otherwise specified)	
Power-Supply Voltage (V+)	30 V
Ambient Operating Temperature Range	−40 to +100°C
Storage Temperature	−55 to +125°C
Pin Soldering Temperature (t = 15 s max.)	300°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Characteristic and Conditions	Min	Typ	Max	Unit
Total Circuit				
Power-Supply Voltage Range (V+)	3.5	—	26	V
Standby Current Drain (V+ = 29 V) (Note 3) T_A = 25°C T_A = 100°C	 — —	 3.7 4.0	 4.5 —	 mA mA
Line Impedance (4 V ≤ V + ≤ 26 V)	—	230	—	kΩ
Voltage Regulator				
Available V_{SENSE} Range (Note 4)	2	—	24	V
V+ minus V_{SENSE} (Note 5)	1.4	—	24	V
V_{SENSE} Set Point	−1	±0.3	+1	%
V_{SENSE} Load Regulation (0 mA ≤ I_{SENSE} ≤ 10 mA) (Note 5) T_A = 25°C −40°C ≤ T_A ≤ 100°C	 — —	 ±0.05 ±0.15	 ±0.2 —	 % %
Temperature Coefficient of V_{SENSE} Over V+ Range (−40°C ≤ T_A ≤ +100°C; 4V ≤ V+ ≤ 26 V)	—	±.002	—	%/°C
Precision Low-Voltage Reference				
V_{REF}, Set Point V+ = 4 V to 26 V	1.238	1.250 (±.005)	1.262	V
I_{REF} Operating Current	—	—	10	mA
V_{REF} Voltage Change (−40°C ≤ T_A ≤ +100°C; I_{REF} = 10 mA)	— —	±.0035 or ±35	±.005 ±50	%/°C ppm/°C
V_{REF} Line Regulation (Note 6) 4 V ≤ V+ ≤ 26 V; I_{REF} = 10 mA)	—	3	6	mV
V_{REF} Load Regulation (0 ≤ I_{REF} ≤ 10 mA)	—	3	8	mV
V_{REF} Temperature Regulation (−40°C ≤ T_A ≤ +100°C; I_{REF} = 10 mA)	—	3	—	mV

Electrical Characteristics
(Continued)

Characteristic and Conditions	Min	Typ	Max	Unit
Precision Low-Voltage Reference (Continued)				
Supply Voltage (V+) Start-Up (Note 7) ($-40°C \leq T_A + 100°C$; I_{REF} = 10 mA)	4	—	—	V
Power-Supply Rejection Ratio (Load Capacitance = 100 pF) dc 1 MHz	— —	70 40	— —	dB dB
Transient start-Up Time (Load Capacitance = 100 pF) I_{REF} = 1 mA I_{REF} = 5 mA I_{REF} = 10 mA	— — —	2 15 150	— — —	μs μs μs
V_{REF} RMS Noise Voltage (10 Hz ≤ f ≤ 10 kHz)	—	5	—	μVrms
High-Speed Comparator				
Input Offset Voltage ($-40°C \leq T_A \leq +100°C$)	—	±1	±5	mV
Input Bias Current	—	300	900	nA
Output Sink Current	—	—	10	mA
Output Saturation Voltage (Output Sink Current = 10 mA) (V_{IN} + = 250 mV overdrive), T_A = 25°C $-40°C \leq T_A + 100°C$ (Output Sink Current = 5 mA) (V_{IN} + = 250 mV overdrive), T_A = 25°C $-40°C \leq T_A \leq +100°C$	 — — — —	 235 <350 130 <150	 500 — 400 —	 mV mV mV mV
Transient Response Times (Logic Low = 0 V; Logic High = 2.5 V, Output Reference = 1.4 V) Propagation Dely (Low-to-High) Propagation Delay (High-to-Low) Rise Time (10% to 90%) Fall Time (90% to 10%)	 — — — —	 105 25 20 50	 — — — —	 ns ns ns ns
Output Leakage Current	—	1	10	μA
Differential Input Voltage	—	—	±6	V
Operational Amplifier				
Input Offset Voltage	—	±1.0	±5.0	mV
Output Voltage Swing (R_L = 2kΩ) $V_{IN}-$ = 0.5 V, V_{HIGH} $V_{IN}-$ = 1.5 V, V_{LOW}	 (V+)−1.5 —	 (V+)−0.8 +1.6	 — +1.65	 V V
Input Bias Current	—	550	—	nA
Output Source Current ($V_{IN}-$ = 0 V; R_L = 100Ω)	—	31	—	mA

Electrical Characteristics
(Continued)

Characteristic and Conditions	Min	Typ	Max	Unit
Operational Amplifier				
Output Sink Current (V_{IN-} = 2.25 V; R_L = 100Ω; $V_{OUT} \leq$ 1.65 V)	—	35	—	mA
Common-Mode Voltage Range				
High (Note 8)	—	(V+) − 2.5	—	V
Low	—	GND	—	V
Power-Supply Rejection Ratio (DC)	—	100	—	dB
Unity Gain Frequency ($C_C = C_{int}$)	—	3.0	—	MHz
Slew Rate (Gain = 10 to 100; $C_C = C_{int}$)	—	11	—	V/μs

Notes:

1. When certain pins are not being used, they should be connected as follows for the 8-Pin devices:
   a. COMP IN − to GND (when comparator is not used)
   b. OA OUT to FEEDBACK (when Op-Amp is not used)
   c. SENSE + should float (when Op-Amp is not used)
2. When certain pins are not used, they should be connected as follows for the 16-Pin devices:
   a. When the comparator is not used, connect COMP IN + to V_{REF} and COMP IN − to GND.
   b. When the Op-Amp is not used, connect OA OUT to OA IN − and OA IN + to V_{REF}.
3. This characteristic excludes the current flowing in the feedback resistors. Feedback current must be calculated for each voltage regulator value.
4. Specific available V_{SENSE} output levels are listed with Ordering Information on the last page.
5. OA OUT is connected to SENSE +.
6. OA OUT is disconnected from SENSE +.
7. This is the minimum supply voltage which is required to assure that V_{REF} has stabilized at any specific temperature within the specified temperature range.
8. Supply voltage (V +) minus a nominal 2.5 V yields high CMVR.

Characteristic Curves

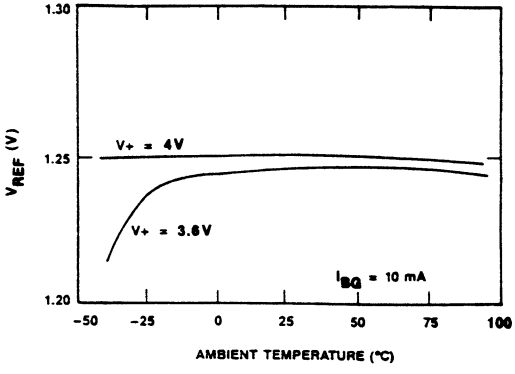


Figure 5. Precision Low-Voltage Reference Start-Up Characteristics

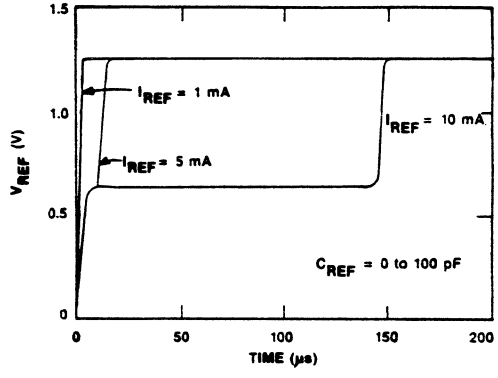


Figure 6. Precision Low-Voltage Reference Transient Start-Up Time

Characteristic Curves
(Continued)

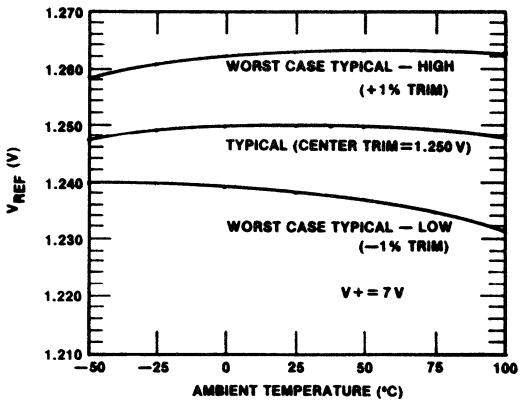


Figure 7. Precision Low-Voltage Reference Temperature Characteristics

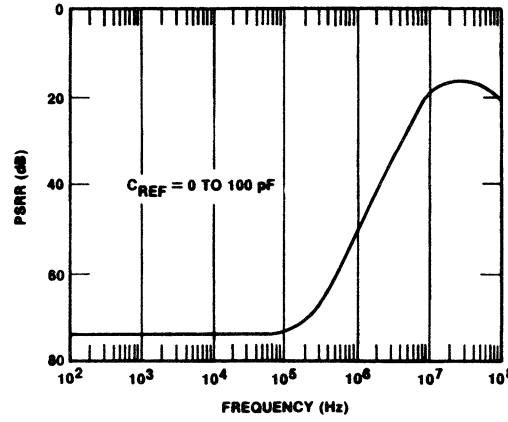


Figure 8. Precision Low-Voltage Reference Power Supply Rejection Ratio Frequency Characteristics

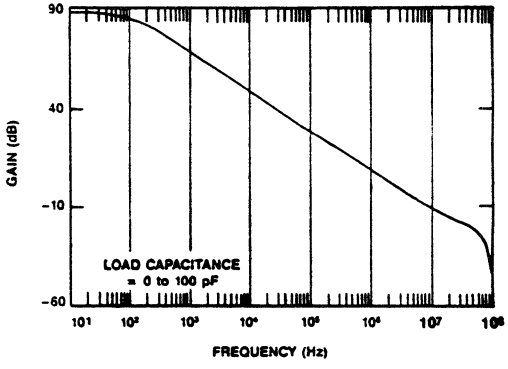


Figure 9. Op-Amp Open Loop Gain

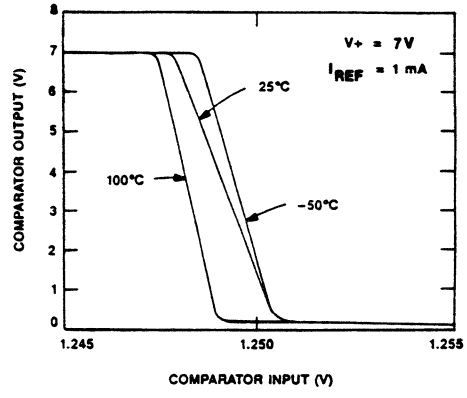


Figure 10. Typical Comparator DC Transfer Characteristics vs Temperature

Characteristic Curves
(Continued)

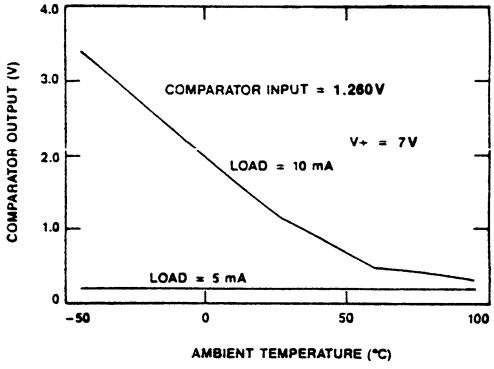


Figure 11. Typical Temperature Characteristics Comparator Output Voltage vs Comparator Input Overdrive of 10 mV

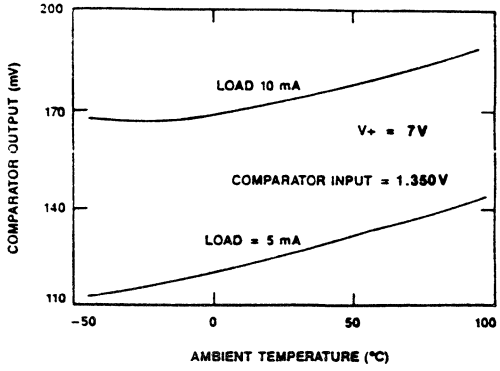


Figure 12. Typical Temperature Characteristics Comparator-Output Voltage vs Comparator Input Overdrive of 100 mV

Applications

The regulation control devices are used in power-supply applications where the simultaneous use of all three functions (voltage regulator, high-speed comparator, precision low-voltage reference) is a common practice.

Figure 13 shows an application which uses all three functions:

The regulator output (Pins 5 and 6 are connected) can be used in dc-dc Converter applications (see Figure 14), current regulation circuits, precision current limiting, etc.

The comparator (Pins 7 and 8) is configured as an alarm indicator circuit. The alarm indicator can be configured as either a visual indicator (LED), a logic output, or both.

The 1.25 V reference output (Pin 2) has many potential applications. Figure 13 shows one application where a programmable shutdown circuit is formed in conjunction with resistors R1 through R4, and an external comparator. The shutdown output controls a circuit which can shut down line voltages which exceed predetermined values.

Applications
(Continued)

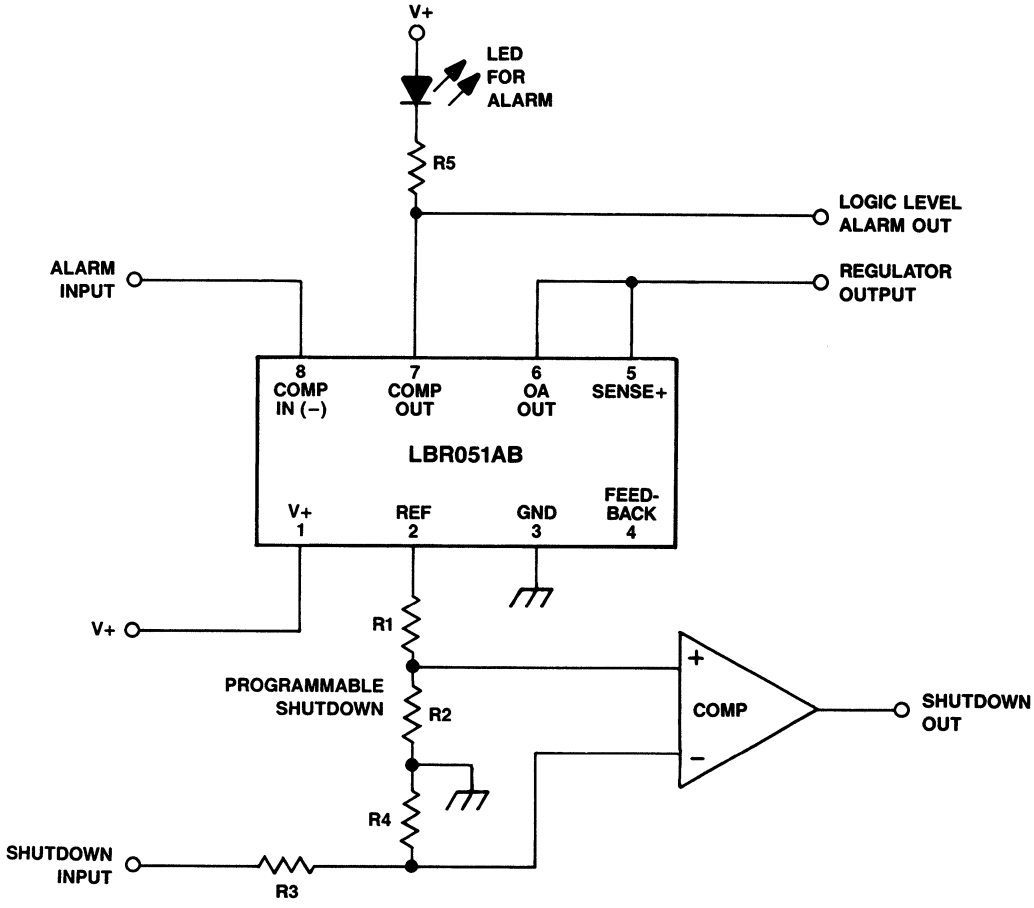
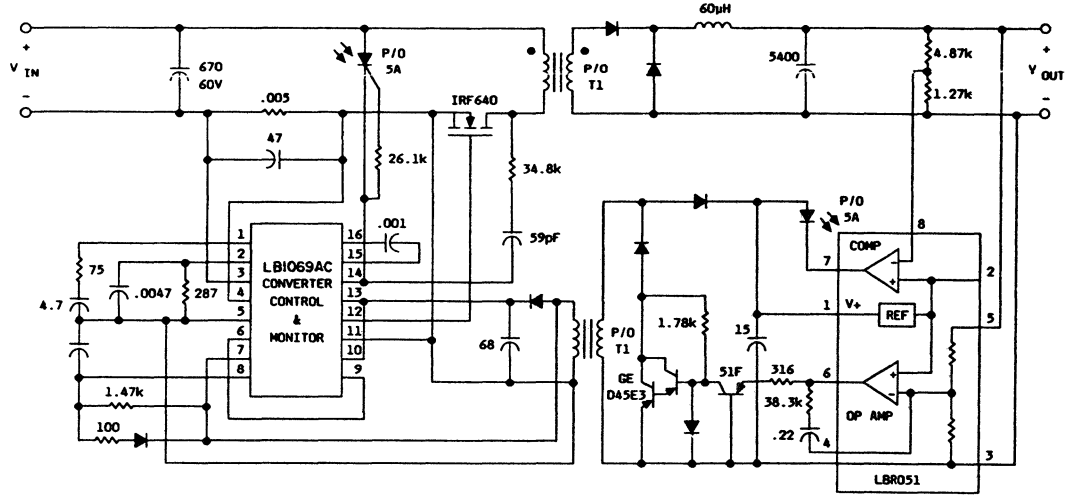


Figure 13. Regulation Control General Application Diagram

Applications
(Continued)

Figure 14 shows the LBR051, a 5.1 volt regulation control device, as it is used in a dc-dc Converter application. This application is a 48 V to 5 V, 20 amp converter, and features high-voltage shutdown and current limiting.



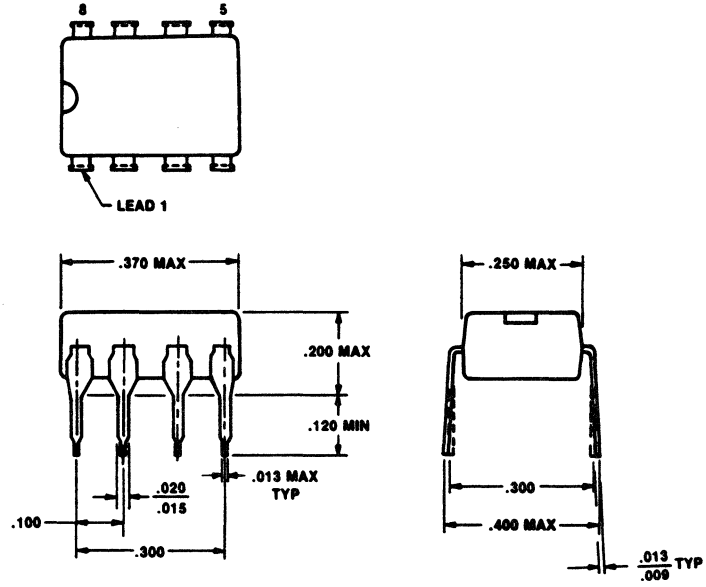
Note: Unless otherwise specified, resistor values are in ohms and capacitor values are in microfarads.

Figure 14. DC-DC Converter Application

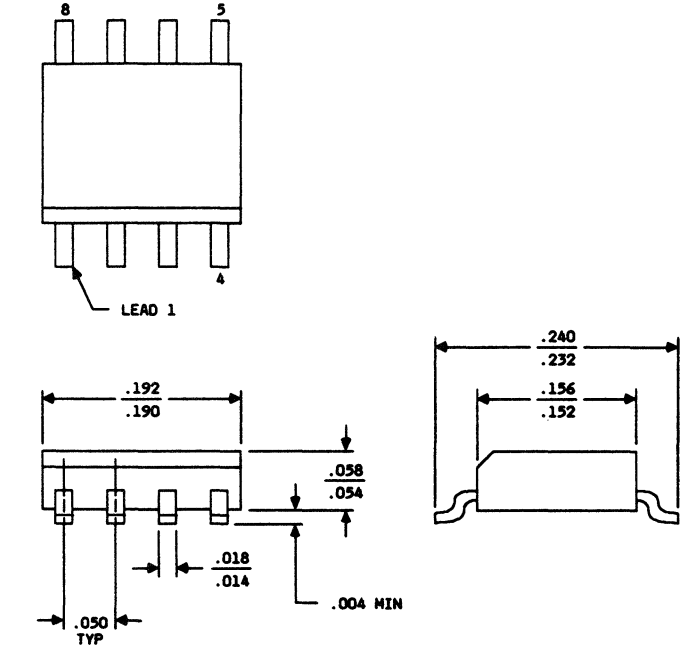
Outline Drawings

(Dimensions in Inches)

8-Pin DIP



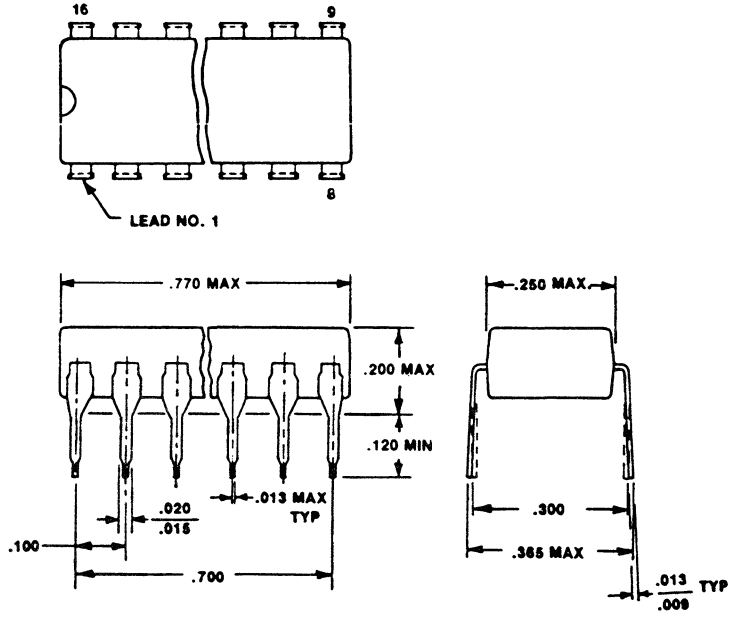
8-Pin



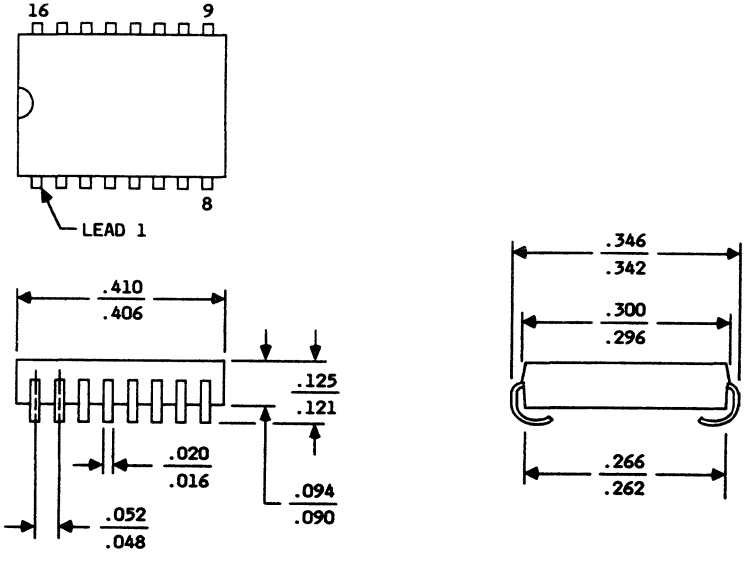
Outline Drawings

(Dimensions in Inches)

16-Pin DIP

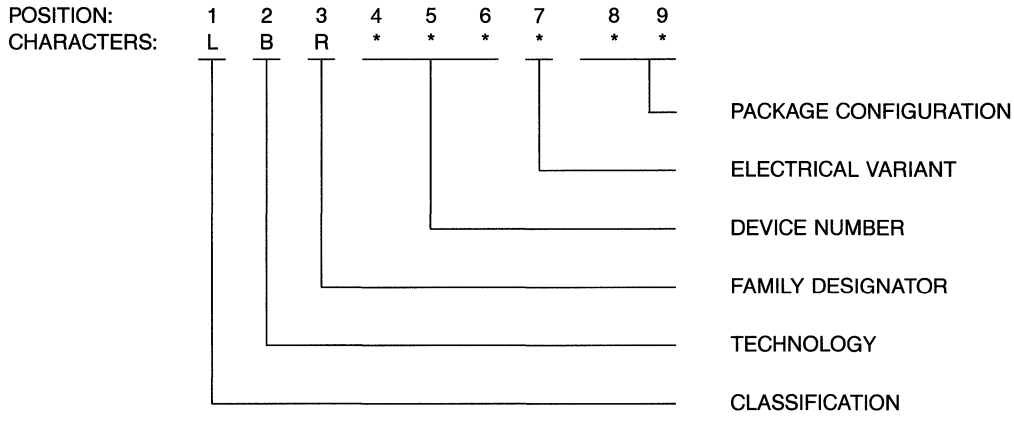


16-Pin SOJ



Ordering Information

The Regulation Control Circuit Family is coded as follows:



Classification (Position 1): L = Linear

Technology (Position 2): B = Complementary Bipolar Integrated Circuit (CBIC)

Family Designator (Position 3): Regulation Control Circuit Family

Device Number (Positions 4, 5, 6): The device number is also the voltage value of the regulator function for this device. A decimal point shall be understood to exist between positions 5 and 6.

Example: 022 = 2.2 V
220 = 22.0 V

Electrical Variants (Position 7): A = ±1% Regulator Voltage①
B = ±1.5% Regulator Voltage
C = ±2% Regulator Voltage
D = ±0.5% Regulator Voltage

Package Configuration (Positions 8, 9):

A = Wafer (8-Pad Chip) Unthinned
AA = Wafer (8-Pad Chip) Thinned
B = 8-Pin DIP
C = 16-Pin DIP
K = 16-Pin SOJ (Surface Mount)
S = 8-Pin SOIC (Surface Mount)
X = Wafer (16-Pad Chip) Unthinned
XA = Wafer (16-Pad Chip) Thinned

①Regulator voltage output is SENSE+ connected to OA OUT.

Description

The LB1019AB integrated circuit is used to switch the unregulated negative 48-volt power-supply to telephone station sets or other loads. It is digitally controlled and has a normal output current drive capability of 300 mA. It can drive instantaneous currents higher than 300 mA and has a built-in thermal shutdown to provide protection in the event of a fault condition.

This device provides logic output states for three different load conditions:

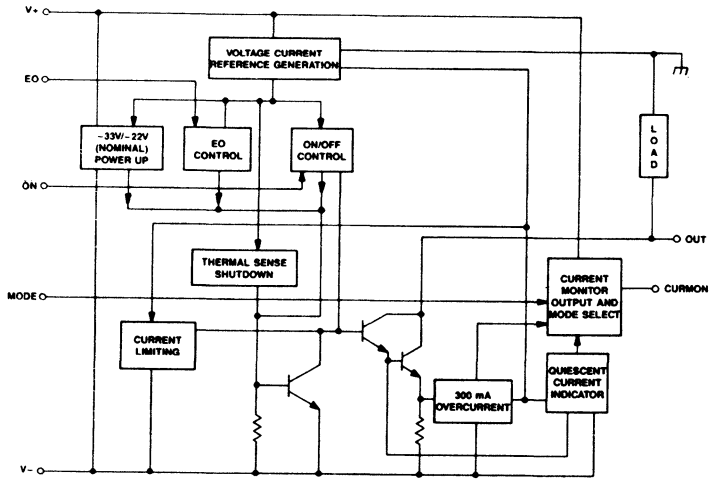
Load currents less than 3 mA—open circuit condition
Load currents greater than 3 mA and less than 300 mA—normal load condition
Load currents greater than 300 mA—overload condition.

The Power Controller will interrupt current to the load if the V− supply voltage is more positive than a nominal −30 volts. This prevents hazardous high current conditions from occurring in a switching regulator located in some telephone station sets. Conversely, current will not be applied to the load unless the V− power-supply is more negative than a nominal −33 volts.

Features

- Digital-controlled power switch
- Controls −48-volt power to telephone sets or other loads
- Power can be turned on and off using on (bar) input
- Current limiting during a fault (overload)
- Thermal shutdown during extended fault conditions
- EO input allows smooth power-up sequence
- Indicates quiescent current flow to confirm circuit continuity
- Indicated overcurrent condition when the load current exceeds 300 mA (typically)
- Inquire about availability of devices with overcurrent threshold settings of 200 mA, 400 mA and 600 mA (±15%)

Functional Diagram



Maximum Ratings (At 25°C unless otherwise specified)	
Ambient Operating Temperature Range	−20 to +70°C
Storage Temperature Range	−40 to +125°C
Pin Soldering Temperature (t = 15 s max.)	300°C
Power, Instantaneous (t 2 μs)	50 W
Operating Voltage (V+ to GND)	+5.5 V
Operating Voltage (V− to GND)	−54 V

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions

(See Functional Diagram and Table 1)

Pin	Symbol	Name/Function
1	V−	Connection for "most negative" external power supply.
2	OUT	The OUTPUT pin supplies a "controlled" voltage to a telephone set or other types of loads.
3	GND	Ground or circuit common (not necessarily physical or system ground).
4	CURMON	Current Monitor. CURMON is a TTL-compatible output signal. It indicates whether the output load current is either less than or greater than a predetermined threshold reference level.
5	MODE	MODE is an LSTTL-compatible input signal (Table 1). A logic HIGH sets the CURMON threshold reference level to a typical value of 300 mA. A logic LOW sets the CURMON threshold level to a typical value of 3 mA (Table 2).
6	V+	Connection for the "most positive" external power-supply.
7	EO	EO is a high-impedance input used to force the chip to ignore all other inputs and hold the −48-volt output off until the voltage on EO exceeds 3.0 volts. This input can be used to eliminate logic power-up "sanity" problems by use of an external RC network, as shown in the Applications Diagram (Figure 10). This input has substantial hysteresis (1.0 ± 0.5 volts) to prevent noise problems since the voltage may ramp up slowly. A diode is included on the chip between EO and +5.0 volts to insure quick discharge of the capacitor upon power-down. The leakage current into or out of EO is tested to be less than 5.0 μA under usage conditions.
8	ON	This pin is an LSTTL-compatible input. When held LOW, it turns on the power to the −48-volt load as long as EO is HIGH and LB1019AB is not in a thermal overload condition.

Characteristics

Table 1—TTL-Compatible Input/Output Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{IL}	Single LSTTL Input: (ON & MODE)	V_{IN} = 0.4 V, V+ = 5.0 V	—	—	−40	μA
I_{IH}		V_{IN} = 2.7 V, V+ = 5.0 V	—	—	20	
V_{OL}	TTL Output: (CURMON)	I_{OL} = 1 mA, V+ = 4.5 V	—	—	0.45	V
V_{OH}		I_{OH} = −250 μA, V+ = 4.5 V	2.4 V	—	—	
V_I	Input Clamp Diode (See EO Pin Description)	I_I = −10 mA, V+ = 4.5 V	—	—	1.5	—

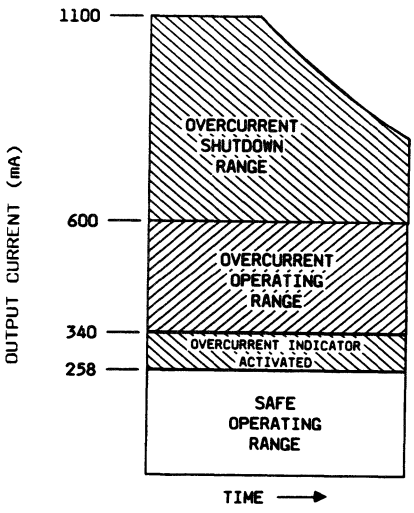


Figure 1 is an output diagram of a typical LB1019AB at room temperature as a function of load current.

For load currents of less than 258 mA, the device is fully on with a voltage drop of less than 2 volts.

Somewhere between 258 mA and 340 mA, the Power Controller will detect current overload and report this condition on the CURMON lead. The Power Controller will remain in the ON state.

For currents less than 600 mA, the power in a typical controller will not be high enough to heat the device to the thermal overload state. For most LB1019AB devices, the Power Controller will remain in the fully ON state.

Somewhere between load currents of 600 mA to 1100 mA, and as a function of time, the device will go into thermal shutdown. At this time, the output current will go to zero until the device has cooled to a temperature less than the thermal overload threshold.

Figure 1. Output Characteristics at 25°C

Characteristics
(Continued)

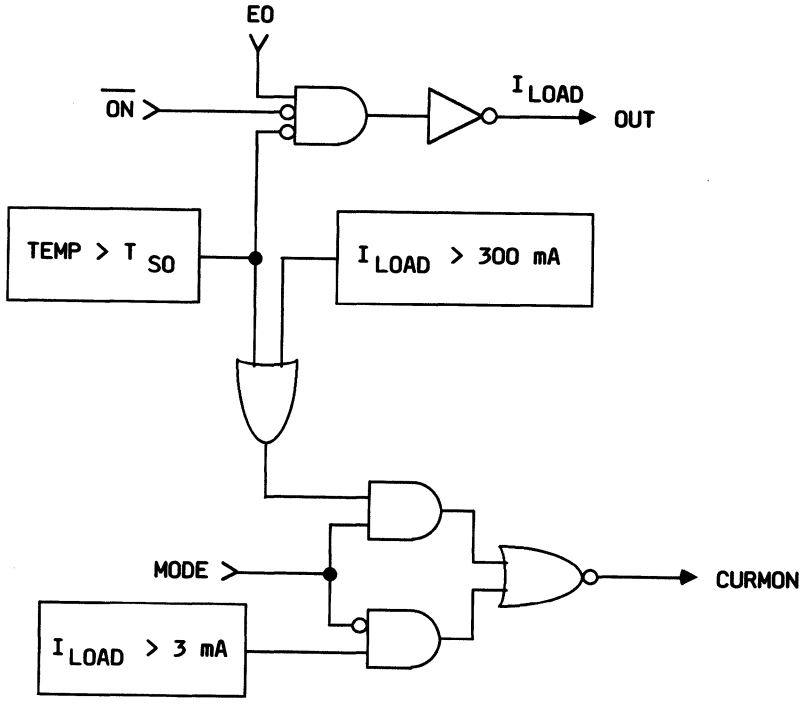


Figure 2. Logic Diagram

Table 2. Output Status Logic Table

EO	$\overline{ON}$	Thermal Shutdown	OUT
0	X	X	OFF
X	X	1	OFF
1	1	0	OFF
1	0	0	ON

Table 3. Current Monitor Status Logic Table

MODE	I_{LOAD} > 3 mA	I_{LOAD} > 300 mA	Thermal Shutdown	CURMON
0	0	X	X	1
0	1	X	X	0
1	X	0	0	1
1	X	X	1	0
1	X	1	0	0

Electrical Characteristics

(T_A = 25°C, V+ = 5.0 volts, V− = −48 volts; unless otherwise specified)

Characteristic	Test Condition	Min	Typ	Max	Unit
Power-Supply Current (V+)	V+ = 5.5 V See Figure 3	—	—	4.4	mA
Power-Supply Current (V−)	V− = −54 V See Figure 3	—	—	2.8	mA
Power-Supply Current (V−)	V+ = open, V− = −54 V See Figure 4	—	—	3.0	mA
V− Turn-On Threshold	See Figure 5	−29.3	−33.0	−37.0	V
V− Turn-Off Threshold	See Figure 5	−26.0	−30.0	−35.2	V
V− Hysteresis	V− Turn-Off Minus V− Turn-On	1.8	—	5.2	V
Output Voltage	I_{OUT} = 300 mA See Figure 6	—	—	2.0	V
EO Turn-On Threshold	See Figure 7	2.5	3.0	3.5	V
EO Turn-Off Threshold	See Figure 7	1.5	2.0	2.5	V
EO Hysteresis	EO Turn-On Minus EO Turn-Off	0.5	—	1.5	V
Low Output Current Threshold	See Figure 8	1.5	3.0	7.0	mA
High Output Current Threshold	See Figure 8	258	300	340	mA
Output Current Limit	See Figure 9	0.6	0.8	1.1	A

Test Circuits

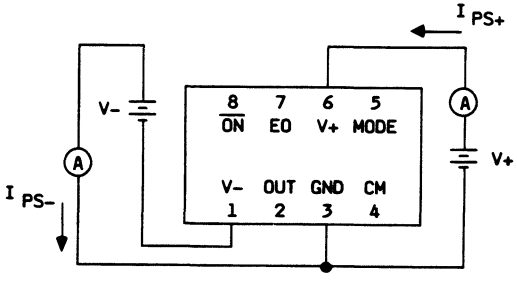


Figure 3. Power-Supply Current

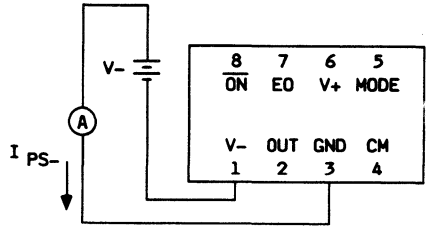


Figure 4. Power-Supply Current

Test Circuits (Continued)

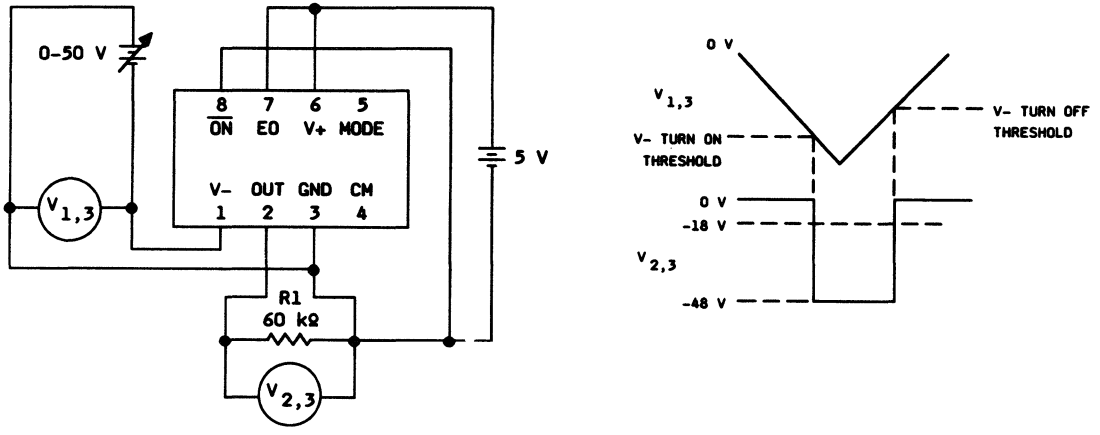


Figure 5. V-Threshold Tests

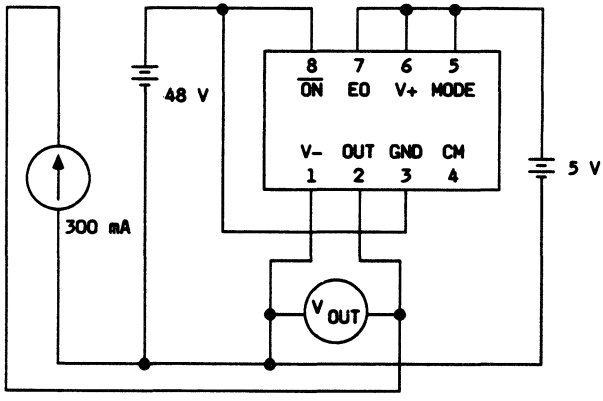


Figure 6. Output Voltage Test

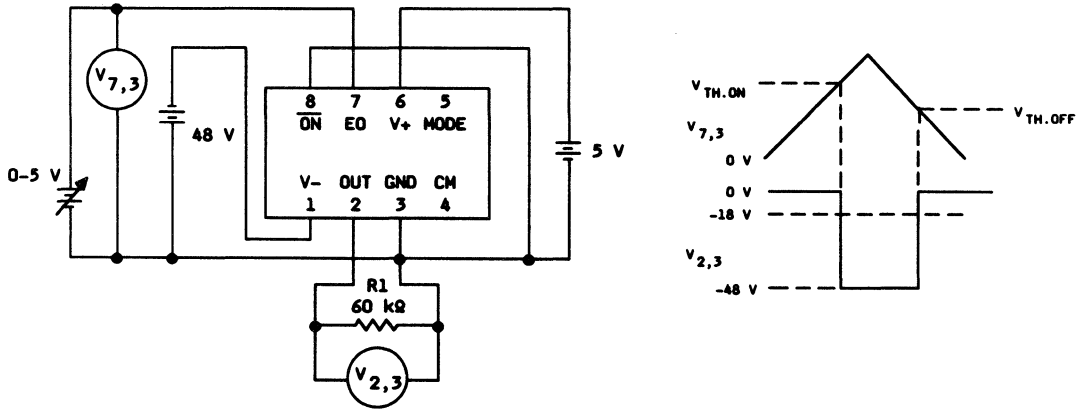


Figure 7. EO Threshold Tests

Test Circuits
(Continued)

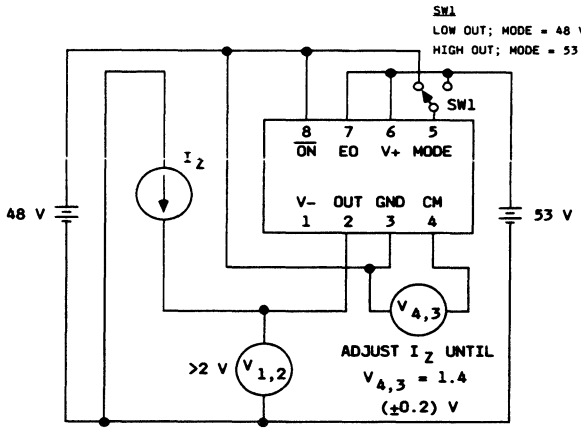


Figure 8. Output Current Threshold Test

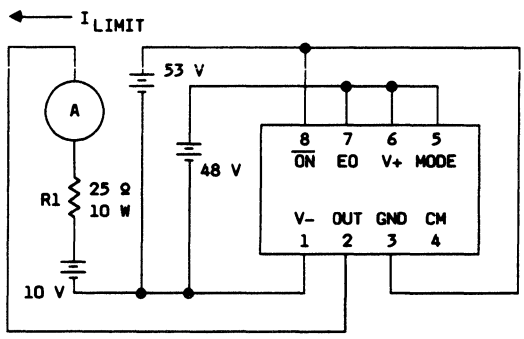


Figure 9. Output Current Limit Test

Applications

Figure 10 is a typical application of the Power Controller used to provide −48 volts to a load. The load is connected between ground and the output of the Power Controller. The −48-volt supply is connected to the V− terminal.

A positive supply of 5 volts is connected to the V+ terminal. A series RC network to ground provides a power-up delay when the 5 volts is initially applied. This circuit will not allow the output to be activated until the voltage at pin EO reaches 3 volts. The EO input is a high impedance and can be connected in parallel with other Power Controller EO inputs.

The ON(BAR) input is used to control the state of the Power Controller output. The output of the LB1019AB will not turn on if the V− supply is more positive than a nominal −33 volts, or the circuit is still hot as a result of thermal overload. Power will be removed from the load when V− is more positive than a nominal −30 volts, or when the circuit temperature exceeds the thermal overload threshold.

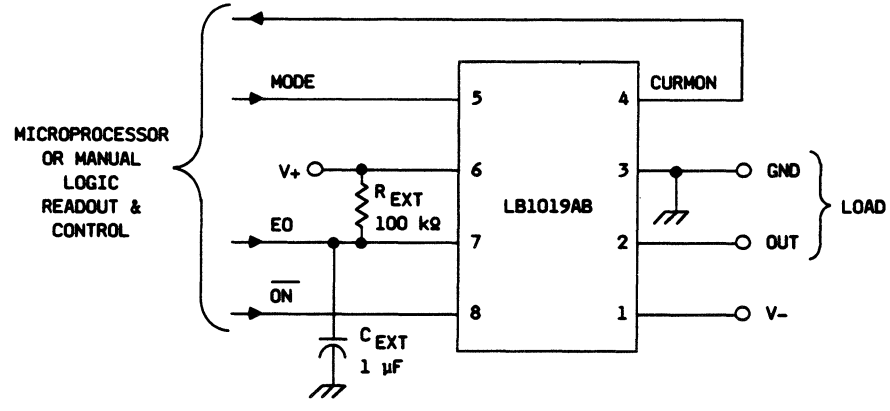


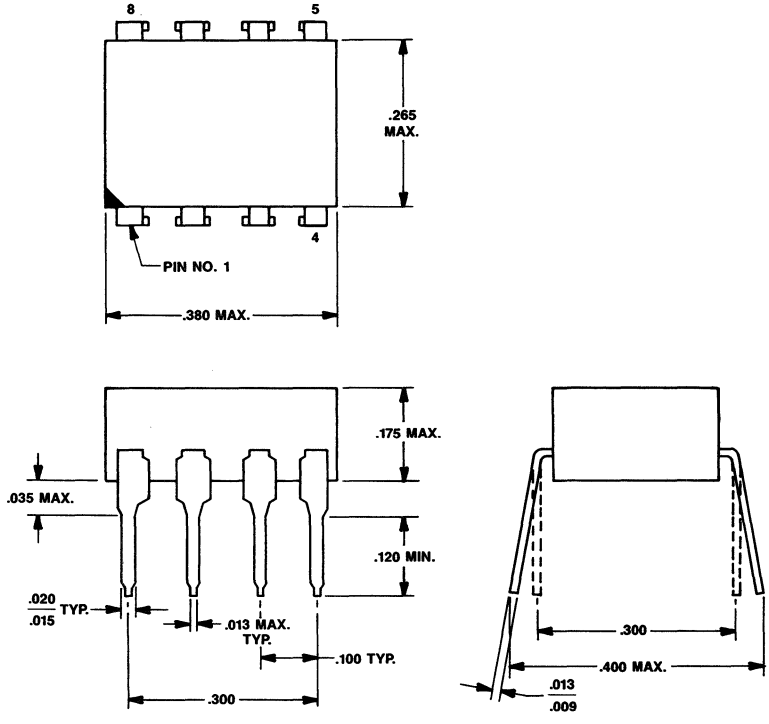
Figure 10. Typical Application Diagram for LB1019AB

Applications
(Continued)

Table 4. Device Operation Summary

EO (In)	$\overline{ON}$ (In)	MODE (In)	CURMON (Out)	DEVICE STATE
0	X	X	1	Disabled, output turned OFF
1	1	X	1	Output OFF, device not in thermal shutdown
1	1	1	0	Output OFF, device in thermal shutdown from previous overload
1	0	0	1	Output ON, connection from controller output to the load is open
1	0	0	0	Output ON, load is connected to the controller output
1	0	1	1	Output ON, current less than overload threshold
1	0	1	0	Output ON, current greater than overload threshold, device may be in danger of going into thermal shutdown, or is in thermal shutdown

Outline Drawing
(Dimensions in Inches)



Ordering Information

Device	Comcode
LB1019AB	104208889

ADVANCE

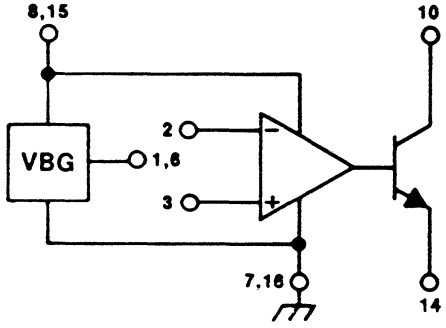
Description

The LB1047AS Voltage Controller contains a bandgap voltage reference and an op-amp with an emitter-follower output stage. The circuit performs the secondary side control functions for a switching power-supply. It drives a light-emitting diode which in turn drives a phototransistor that provides isolation from the input to the output of a power-supply.

Features

- Op-amp with an emitter-follower output stage
- 200 ppm/°C bandgap reference
- Flexible circuitry: part of or all of the device may be used in other applications
- 8-pin small outline narrow body package

Functional Diagram



Maximum Ratings (At $T_A = 25°C$ unless otherwise specified)	
Voltage	18 V
Power Dissipation	550 mW
Storage Temperature	−40 to +125°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Description

Lead	Function
1	Positive Amp Output
2	No Connection
3	Negative Amp Output
4	Ground
5	Inverting Input
6	Non-Inverting Input
7	Bandgap Output
8	Positive Rail

Electrical Characteristics

(At $T_A = 25°C$ unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic and Test Condition	Min.	Typ.	Max.	Unit
Sourcing or Sinking Current @ 5.0 V	6.0	—	—	mA
Power-Supply Current @ 5.0 V	0.8	—	2.5	mA
Bandgap Voltage	1.18	—	1.3	V
Input Bias Current, Negative	—	—	±1.0	μA
Input Bias Current, Positive	—	—	±1.0	μA

Applications

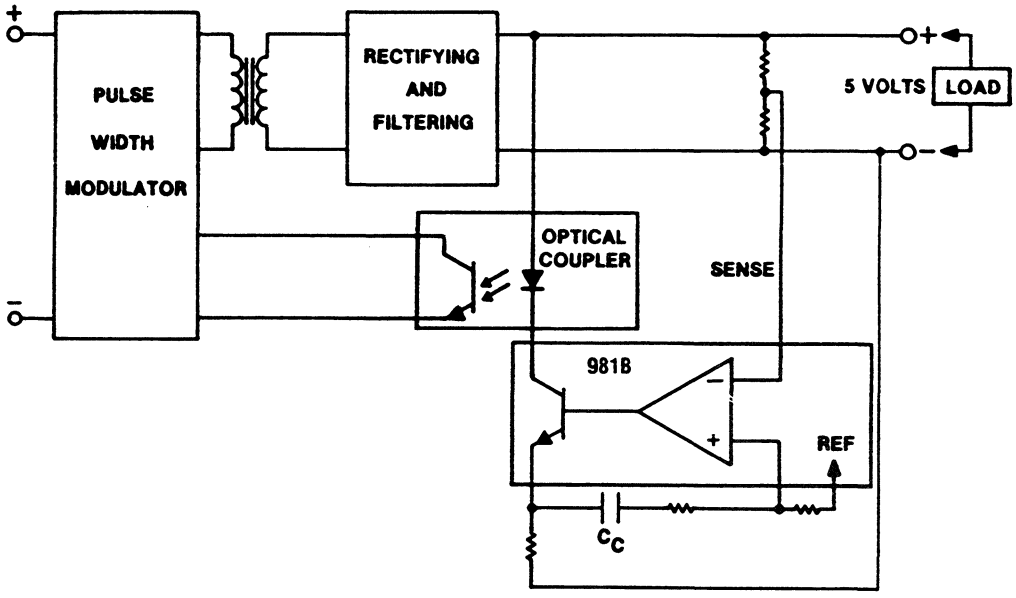
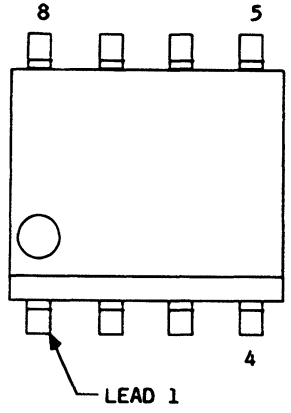
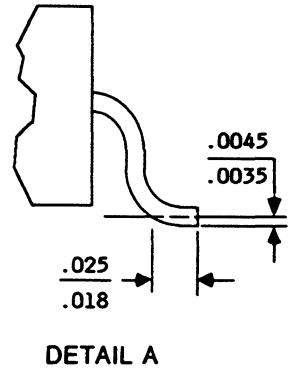


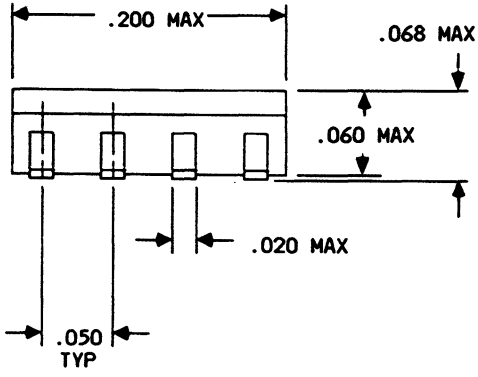
Figure 1. Typical Application

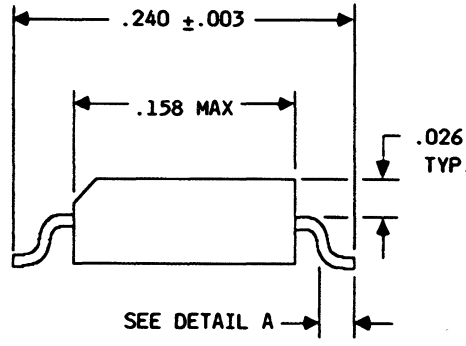
Outine Drawing

(Dimensions in Inches)









Ordering Information

Device	Comcode
LB1047AS	104371380

PRELIMINARY

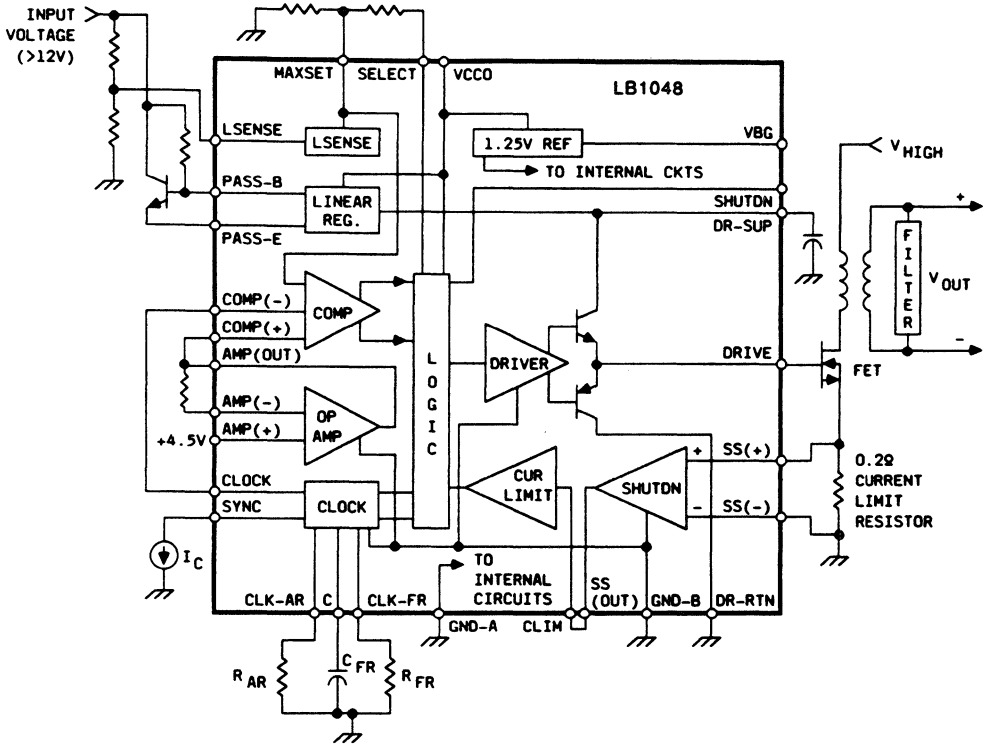
Description

The LB1048AG/AAJ Pulse-Width Modulator is a silicon integrated circuit offering a single-ended output which can either sink or source currents up to 200 mA. This device is suitable for performing the basic pulse width modulation function in switching power supplies. The logic section provides noise immunity by having an edge-triggered input which allows only one transition per clock cycle. This device includes a 1.25 volts temperature-compensated reference capable of supplying up to 1 mA to external circuitry. It also features circuitry for current limiting, maximum duty-cycle limiting, shut-down and adaptive start-up. An internal triangular wave shape oscillator (providing equal rise and fall times) is controlled by external components. This Pulse-Width Modulator is available in a 28-pin DIP (LB1048AG) and in a 28-pin surface mount package (LB1048AAJ).

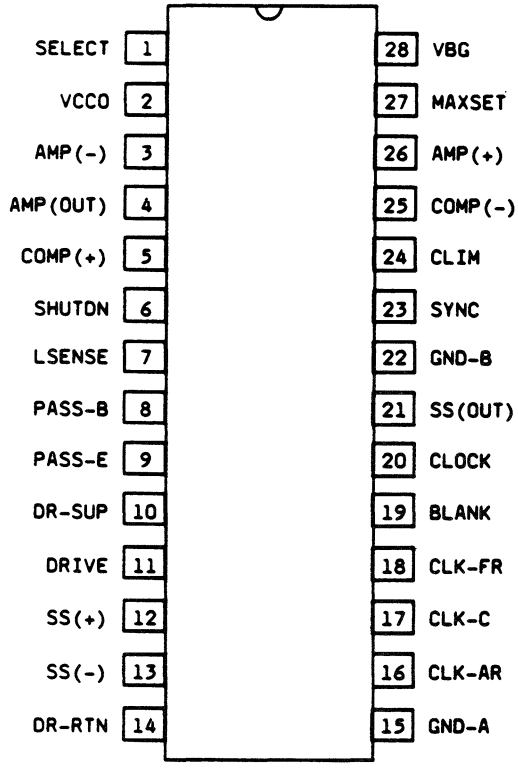
Features

- Single source/sink output: ±200 mA
- Frequency adjustable to 500 KHz
- Noise-immunity logic
- External oscillator synchronization
- Adaptive start-up and shutdown control
- Double pulse suppression
- Current limit control of external FET
- Quiescent current less than 7.0 mA
- Maximum duty cycle control
- FET driver

Functional Diagram



Pin Diagram



Maximum Ratings (At 25°C unless otherwise specified)	
Ambient Operating Temperature Range	−25 to +100°C
Storage Temperature Range	−40 to +125°C
Driver Output Current, Source or Sink	500 mA

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Recommended Operating Conditions

Parameter	Min	Max	Unit
Reference Load Current (Pin 28)	—	1.0	mA
Clock Frequency Range (See Applications)	0.1	500	kHz

Pin Descriptions (See Functional Diagram)

Pin	Symbol	Name/Function
1	SELECT	SELECT is a TTL-compatible pin. A logic low on this pin will disable the current limiting function of the output DRIVE terminal (pin 11).
2	VCCO	This pin provides a regulated output voltage of 9.0 (±0.5) volts.
3 4 26	AMP(−) AMP(OUT) AMP(+)	Inverting input, output and non-inverting input respectively to the operational amplifier. The function of the operational amplifier is to provide a dc signal for comparison with the clock.
5 25	COMP(+) COMP(−)	Non-inverting and inverting inputs respectively to a 3-input comparator (also see MAXSET, pin 27 description). The comparator controls the duty cycle of the FET by comparing the operational signal to the clock signal.
6	SHUTDN	This input pin is intended for shutdown of the FET driver and is TTL compatible. A logic high shuts the FET driver off.
7	LSENSE	Line sense monitors the line voltage to provide adaptive start-up.
8 9	PASS-B PASS-E	Connection to the base and emitter respectively, of an external NPN transistor. These terminals provide dc power for the LB1048AAJ and LB1048AG.
10	DR-SUP	This pin should be tied to a capacitor to provide the current surge needed (up to 200 mA) to switch the FET.
11	DRIVE	Output of a driver which is capable of sourcing or sinking in excess of 200 mA. This driver can turn-on or turn-off a 1000 pF gate FET in less than 50 ns.
12 13 21	SS(+) SS(−) SS(OUT)	Positive input, negative input and output respectively for the current limit circuitry. The current limit circuit's function is to turn off the FET if the current limit value is exceeded. This value is controlled by the user when specifying the current limit resistor (see Functional Diagram).
14	DR-RTN	Return (common) for the high-current ouput stage of the Driver circuit. This pin should be connected separately to a low-ohmic ground because of its high noise content.
15	GND-A	Quiet ground for all of the device circuitry except for the circuits described under the descriptions for pins 14 and 22.
16 17 18	CLK-AR CLK-C CLK-FR	Clock connections to an external amplitude adjusting resistor, an external frequency adjusting capacitor and an external frequency adjusting resistor. The clock provides a triangular waveshape with a frequency of 1/[2 RC] and an amplitude of from 3 to 6 volts (see note 3 under applications).
19	BLANK	This pin **may** be used as a tie point for external components. Maximum allowable voltage on this pin is 10 volts.
20 22	CLOCK GND-B	This output provides a triangular clock waveform which is used by the comparator (also see Pin 25 description). Quiet ground for the designated circuitry as shown in the Functional Diagram.
23	SYNC	Clock Sync. This function synchronizes the LB1048AAJ and LB1048AG clock to some external reference clock.
24	CLIM	Current Limit. The current limit (CLIM) turns off and keeps off the FET under excess current conditions.
27	MAXSET	Limits the duty cycle of the FET driver (See Figure 10). Resistors R1 and R2 set the maximum voltage of the error signal in the compensator.
28	VBG	Output of a 1.25 volt, temperature-compensated reference circuit. This circuit provides references for internal operation of this modulator device. In addition, this output pin has been supplied for the convenience of the user in external applications. The load on this pin should be limited to < 1 mA source.

Electrical Characteristics

(At 25°C and 100°C)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic	Test Condition	Min	Typ	Max	Unit
DC Operating Current	Figure 1; Measure I_{DC}	5.0	6.5	7.0	mA
Sync Current, Differential	Figure 2; Measure Is-I_{DC}	1.0	1.5	2.0	mA
Reference Voltage (VCCO)	Figure 3; Measure Pin 2 (VCCO)	8.5	9.0	9.5	V
Reference Voltage (VBG)	Figure 3; Measure Pin 28 (VBG) opened	1.18	1.25	1.30	V
SS Amplifier, Null	Figure 4; Measure Pin 21 (SSOUT) Pin 12 Connected to Pin 22 (Gnd)	−100	+10	100	mV
SS Amplifier, DC Gain SSOUT/SST	Figure 4; Measure Pin 21 (SSOUT) Pin 12 = 0.1 V	2.1	2.2	2.5	V
SS Amplifier, DC Gain with Current Limiting Load SSOUT/SST	Figure 4; Measure Pin 21(SSOUT) Pin 12 = 0.2 V (SST) Pin 24 connected to Pin 21 (SSOUT)	1.08	1.1	1.32	V
SS Amplifier, AC Gain	Figure 4; Measure Pin 21 (SSOUT)①	21	22	25	—
SS Amplifier, Positive Output Voltage Swing	Figure 4; Measure Pin 21 (SSOUT) Pin 12 = 0.7 V	7.0	8.2	10.0	V
Operational Amplifier, Output Voltage Swing (High)	Figure 5: Measure Pin 4 (AMP OUT) Pin 3 (AMP−) = 1.00 V Pin 26 (AMP+) = 1.25 V	6.5	8.0	8.5	V
Operational Amplifier, Output Voltage Swing (Low)	Figure 5; Measure Pin 4 (AMP OUT) Pin 3 (AMP−) = 1.25 V Pin 26 (AMP+) = 1.00 V	1.2	1.5	2.0	V
Driver Supply Voltage	Figure 6; Measure Pin 10 (DR-SUP)	10.0	10.7	11.0	V
Driver Voltage (High)	Figure 6; Measure Pin 11 (DRIVE) Pin 11 = 35 Ω, 2W Resistor to Gnd	7.0	8.8	9.4	V
Driver Current, Sink	Figure 6②	200	235	500	mA
Clock-C, Source Current	Figure 7; Pin 18 (CLK-FR) = +7.0 V	80	100	120	μA
Clock-C, Sink Current	Figure 7; Pin 18 (CLK-FR) = +2.0 V	80	100	120	μA
Clock-C Ratio (Sink I/Source I)	Figure 7	0.96	1.00	1.04	—
Maxset Voltage (High)	Figure 8; Pin 7 = 5.0 V	4.0	4.5	5.0	V
Maxset Voltage (Low)	Figure 8; Pin 7 = 1.0 V	−2.0	+1.0	+2.0	V
Operational Amplifier, Open-Loop Voltage Gain @ 10 kHz	V_{IN} = 100 mVrms V_{CM} = 1.25 V (Standard Op-Amp Test)	37	57	65	dB
Operational Amplifier, Input-Offset	V_{CM} = 1.25 V (Standard Op-Amp Test)	−6.0	—	+1.0	mV

① The input signal on pin 12 shall be a 10 kHz (sinewave) with an amplitude of 100 mVrms (±5%) and a dc offset of +150 mVDC. The output (pin 21) shall be measured with a high impedance (≥ 1 megohm) rms to dc converter.

② Disconnect Pin 11 (DRIVE) connections as shown and connect a +2.0 volt power-supply to this pin. Measure the power-supply current.

Simplified Test Circuits

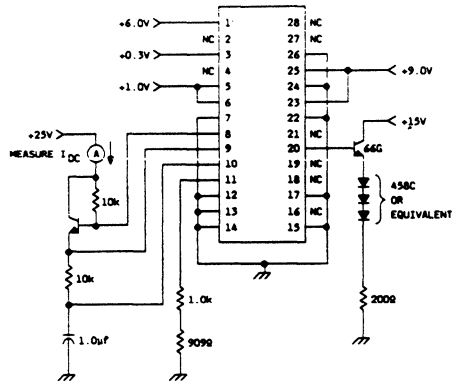


Figure 1. Test Circuit

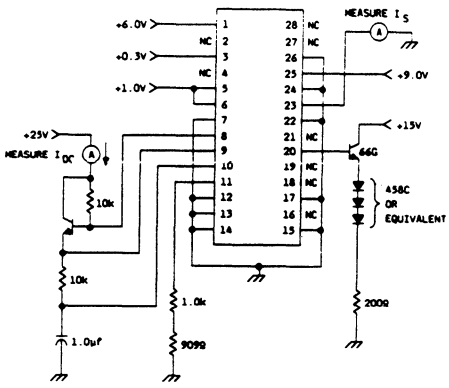


Figure 2. Test Circuit

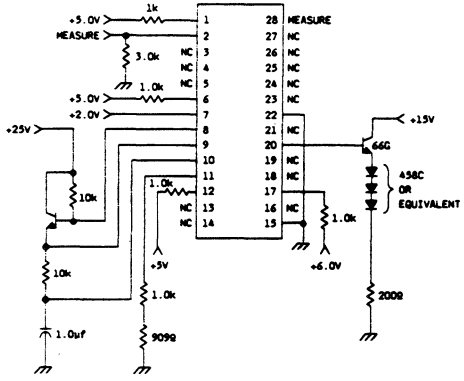


Figure 3. Test Circuit

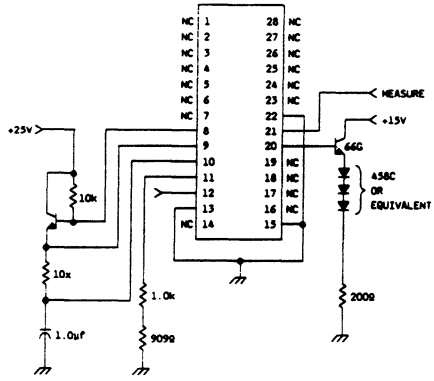


Figure 4. Test Circuit

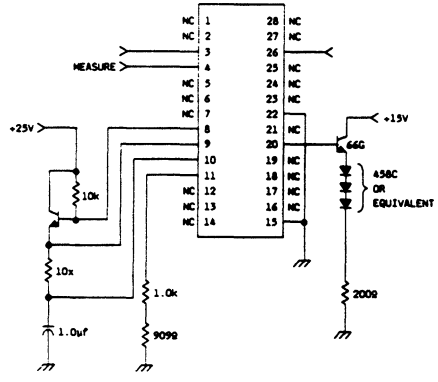


Figure 5. Test Circuit

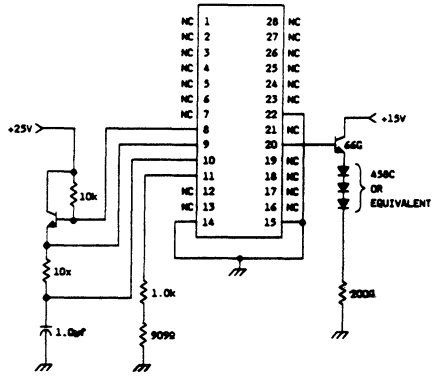


Figure 6. Test Circuit

Simplified Test Circuits
(Continued)

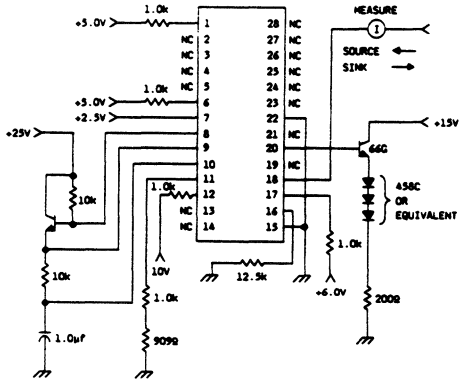


Figure 7. Test Circuit

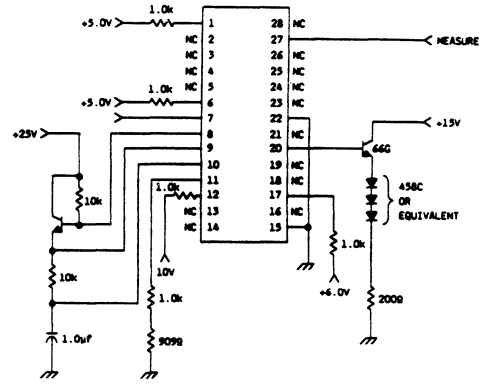


Figure 8. Test Circuit

Applications

The LB1048AG/AAJ integrated circuit performs the primary functions for the pulse-width modulated switching power-supply as shown in Figure 9. Since the LB1048AG/AAJ are 18-volt device, it cannot operate directly off of the 48-volt line voltage. An external high-voltage transistor (Q1) interfaces with the line voltage and the LB1048 linear regulator in such a manner that a 9-volt operating supply is generated (VCCO, Pin 2).

The pulse-width modulated power-supply works on the principle that the amount of power delivered to the load increases with an increase in the duty cycle of the transformer primary Field Effect Transistor (FET) switch. This is accomplished with the comparator by comparing a feedback signal from the output of the power-supply with a 100 KHz triangular wave of 3 to 6 volts amplitude. The comparator also has the capability of limiting the maximum duty cycle and can be used to keep the FET switch off during start-up conditions.

The output of the comparator is a treed Emitter Coupled Logic (ECL) signal which feeds into the logic. The logic section provides noise immunity by having an edge-triggered input which only permits one transition per clock cycle. It also performs the on/off function and shuts down the FET switch when the current in the transformer primary exceeds a set maximum value.

The current limit signal is obtained by sampling the voltage across a current limiting resistor (usually only a few tenths of an ohm) and amplifying it by a factor of six. This amplified signal is then compared to an internally generated reference voltage (VBG) of 1.25 volts. The output of the comparator is an ECL signal that feeds into the logic section.

The output of the logic feeds the Driver amplifier which controls an external FET switch. The Driver is capable of sourcing or sinking in excess of 200 mA, which can turn on/off a 1000 pF gate FET in less than 50 ns.

Applications
(Continued)

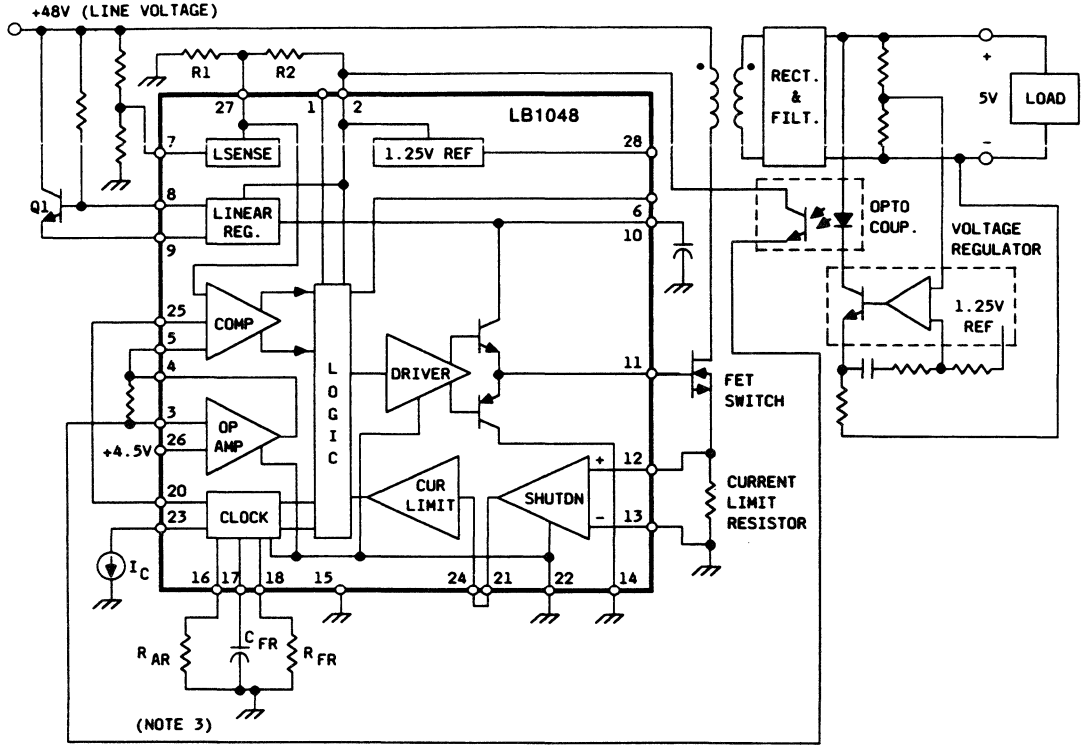


Figure 9. Application Diagram

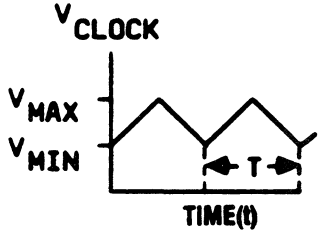


Figure 10. Clock Diagram

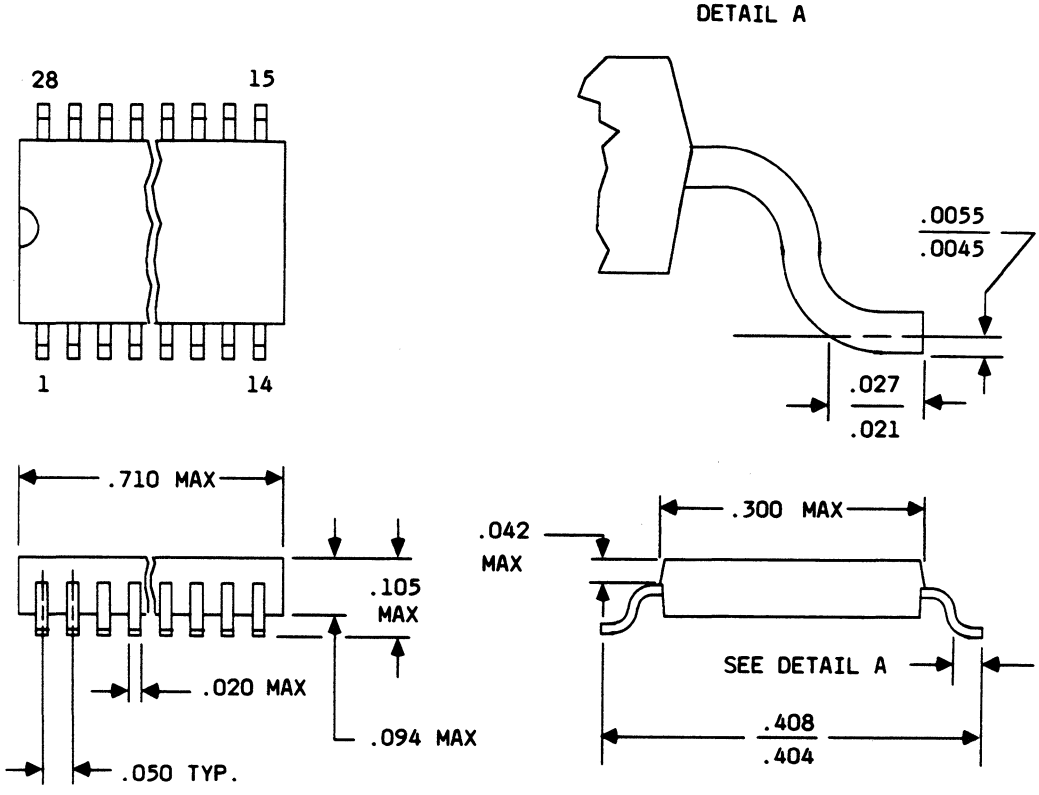
Note 3: C_{FR}, R_{AR} accurately set the clock frequency as well as the maximum and minimum voltages. V_{MAX} is set to 6 volts for normal operation.

$$R_{AR} = \frac{VBG}{I_{RAR}} \qquad R_{FR} = \frac{V_{MAX}}{2}\,\frac{R_{AR}}{VBG} \qquad C_{FR} = \frac{T}{2\,R_{FR}} \qquad V_{MIN} = \frac{V_{MAX}}{2}$$

Typical Values: $I_{RAR} = 100\ \mu A$, $VBG \approx 1.25$ V

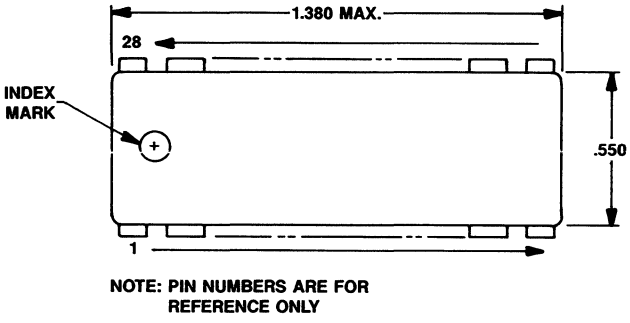
LB1048AAJ Outline Drawing

(Dimensions in Inches)

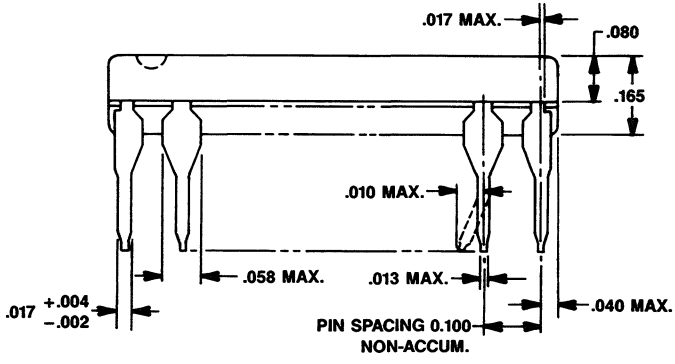


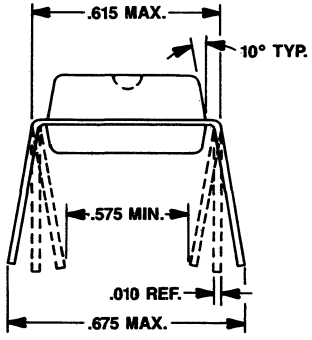
LB1048AG Outline Drawing

(Dimensions in Inches)



NOTE: PIN NUMBERS ARE FOR REFERENCE ONLY





Ordering Information

Device	Comcode
LB1048AAJ	104411558
LB1048AG	104411541

Description

The LB1073AB Regulation Control Circuit provides three main functions in the same package; a precision 1.25 V reference, a high-speed comparator, and an operational amplifier with the non-inverting input referenced to the 1.25 V reference. The device operates over the supply-voltage range of 4 V to 26 V. The LB1073AB device is similar to the LBR Regulation Control Family except that the feedback resistors must be supplied by the end user.

Features

Op-Amp

- Input offset < 5 mV (-40 to 100°C)
- Unity gain frequency 3.0 mHz
- Typical Slew rate 11 V/μs
- Referenced to 1.25 V

High-Speed Comparator

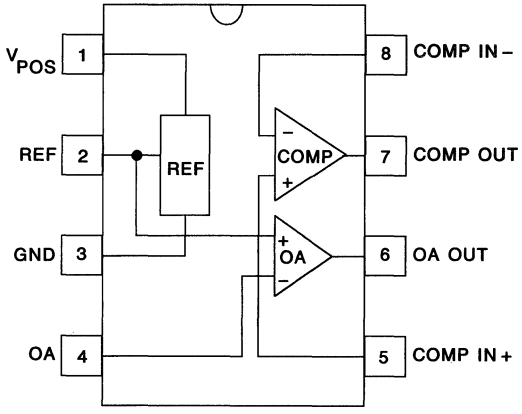
- Propagation delay < 150 ns
- Input offset < 5 mV (-40 to $+100$°C)
- Output loading to 10 mA maximum

Precision Low-Voltage Reference

- 1.25 V ($\pm$1%) from 4- to 26-volt supply
- Temperature coefficient < 50 ppm/°C (-40 to $+100$°C)
- 4-volt minimum V+ operation (-40 to $+100$°C)
- Capacitive Loading to 100 pF maximum
- Current loading to ≤ 10 mA
- Excellent power-supply rejection ratio (PSRR) 70 dB @ dc; 40 dB @ 1 MHz
- Fast transient start-up time

Pin Diagrams

8-Pin Dip



Maximum Ratings (At 25°C unless otherwise specified)	
Power-Supply Voltage (V+)	30 V
Ambient Operating Temperature Range	−40 to +100°C
Storage Temperature	−55 to +125°C
Pin Soldering Temperature (t = 15 s max.)	300°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Description

(See Pin Diagram)

Pin	Symbol	Name/Function
1	V_{POS}	Supply Voltage (4 to 26V)
3	GROUND	Circuit Common (not necessarily system or physical ground)
2	VREF	1.25 V Reference Output
8	COMP IN−	Inverting Comparator Input
5	COMP IN +	Non-Inverting Comparator Input
7	COMP OUT	Comparator Output, Open Collector, Requires Pull-Up Resistor
4	OA IN−	Inverting Op-Amp Input
	OA IN+	Non-Inverting Op-Amp Input. Connected to V_{REF}
6	OA OUT	Op-Amp Output

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Parameter and Conditions	Min.	Typ.	Max.	Unit
Total Circuit				
Power-Supply Voltage Range (V+)	3.5	—	26	V
Standby Current Drain (V+ = 29 V) (Note 3)				
T_A = 25°C	—	3.7	4.5	mA
T_A = 100°C	—	4.0	—	mA
Line Impedance (4 V ≤ V + ≤ 26 V)	—	230	—	kΩ

Electrical Characteristics
(Continued)

Parameter and Conditions	Min	Typ	Max	Unit
Precision Low-Voltage Reference				
V_{REF}, Set Point $V+ = 4$ V to 26 V	1.238	1.250 ($\pm$.005)	1.262	V
I_{REF} Source Current	—	—	10	mA
V_{REF} Voltage Change ($-40°C \leq T_A \leq +100°C$; $I_{REF} = 10$ mA)	— or —	$\pm$.0035 $\pm$35	$\pm$.005 $\pm$50	%/°C ppm/°C
V_{REF} Line Regulation (Note 3) ($4V \leq V+ \leq 26$ V; $I_{REF} = 10$ mA)	—	3	6	mV
V_{REF} Load Regulation ($0 \leq I_{REF} \leq 10$ mA)	—	3	8	mV
V_{REF} Temperature Regulation ($-40°C \leq T_A \leq +100°C$; $I_{REF} = 10$ mA)	—	3	—	mV
Supply Voltage ($V+$) Start-Up (Note 4) ($-40°C \leq T_A \leq +100°C$; $I_{REF} = 10$ mA)	4	—	—	V
Power-Supply Rejection Ratio (Load Capacitance = 100 pF) dc 1 MHz	 — —	 70 40	 — —	 dB dB
Transient Start-Up Time (Load Capacitance = 100 pF) $I_{REF} = 1$ mA $I_{REF} = 5$ mA $I_{REF} = 10$ mA	 — — —	 2 15 150	 — — —	 μs μs μs
V_{REF} RMS Noise Voltage (10 Hz $\leq$ f $\leq$ 10 kHz)	—	5	—	μVrms
High-Speed Comparator				
Input Offset Voltage ($-40°C \leq T_A \leq +100°C$)	—	$\pm$1	$\pm$5	mV
Input Bias Current	—	300	900	nA
Output Sink Current	—	—	10	mA
Output Saturation Voltage (Output Sink Current = 10 mA) ($V_{IN}+ = 250$ mV Overdrive, $T_A = 25°C$ $-40°C \leq T_A \leq +100°C$ (Output Sink Current = 5 mA) ($V_{IN}+ = 250$ mV Overdrive, $T_A = 25°C$ $-40°C \leq T_A \leq +100°C$	 — — — —	 235 < 350 130 < 150	 500 — 400 —	 mV mV mV mV
Transient Response Times (Logic Low = 0 V; Logic High = 2.5 V; Output Reference = 1.4 V) Propagation Delay (Low-to-High) Propagation Delay (High-to-Low) Rise Time (10% to 90%) Fall Time (90% to 10%)	 — — — —	 105 25 20 50	 — — — —	 ns ns ns ns
Output Leakage Current	—	1	10	μA
Differential Input Voltage	—	—	$\pm$6	V

Electrical Characteristics
(Continued)

Parameter and Conditions	Min.	Typ.	Max.	Unit
Optional Amplifier				
Input Offset Voltage	—	±1.0	±±5.0	mV
Output Voltage Swing (R_L = 2 kΩ) $V_{IN}-$ = 0.5 V, V_{HIGH} $V_{IN}-$ = 1.5 V, V_{LOW}	 (V+) − 1.5 —	 (V+) − 0.8 +1.6	 — +1.65	 V V
Input Bias Current	—	550	—	nA
Output Source Current ($V_{IN}-$ = 0 V; R_L = 100 Ω)	—	31	—	mA
Output Sink Current ($V_{IN}-$ = 2.25 V; R_L = 100Ω; V_{OUT} ≤ 1.65 V)	—	35	—	mA
Common-Mode Voltage Range High (Note 5) Low	 — —	 (V+) −2.5 GND	 — —	 V V
Power-Supply Rejection Ratio (DC)	—	100	—	dB
Unity Gain Frequency (C_C = C_{int})	—	3.0	—	MHz
Slew Rate (Gain = 10 to 100; C_C C_{int})	—	11	—	V/μs

Notes:
1. When certain pins are not being used, they should be connected as follows for the 8-Pin devices:
   a. COMP IN − to GND (when Comparator is not used)
   b. OA OUT to OA IN − (when Op-Amp is not used)
2. This characteristic excludes the current flowing in the feedback resistors. Feedback current must be calculated for each voltage regulator value.
3. OA OUT is connected to OA IN −
4. This is the minimum supply voltage which is required to assure that V_{REF} has stabilized at any specific temperature within the specified temperature range.
5. Supply voltage (V+) minus a nominal 2.5 V yields high CMVR.

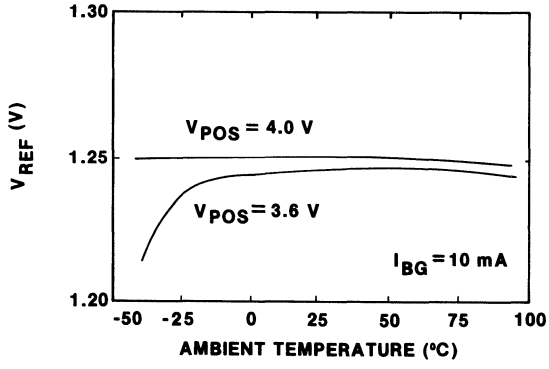


Figure 1. Precision Low-Voltage Reference Start-Up Characteristics

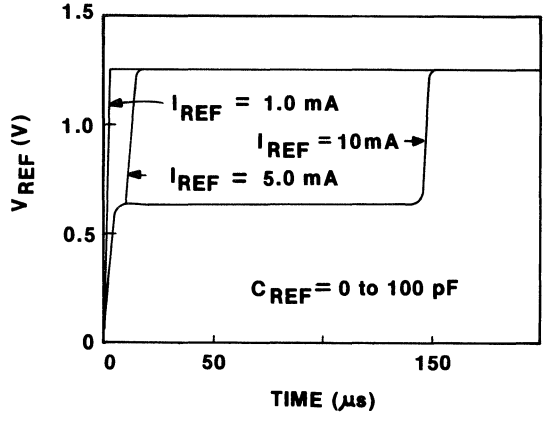


Figure 2. Precision Low-Voltage Reference Transient Start-Up Time

Characteristics
(Continued)

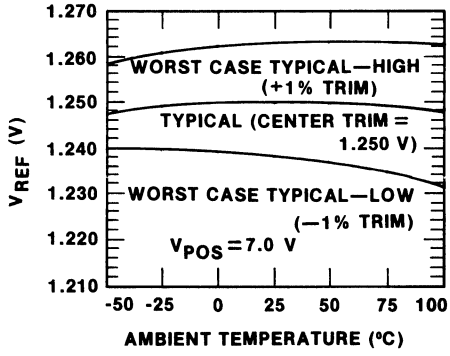


Figure 3. Precision Low-Voltage Reference Temperature Characteristics

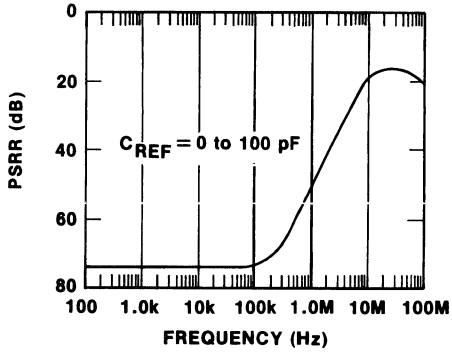


Figure 4. Precision Low-Voltage Reference Power-Supply Rejection Ratio Frequency Characteristics

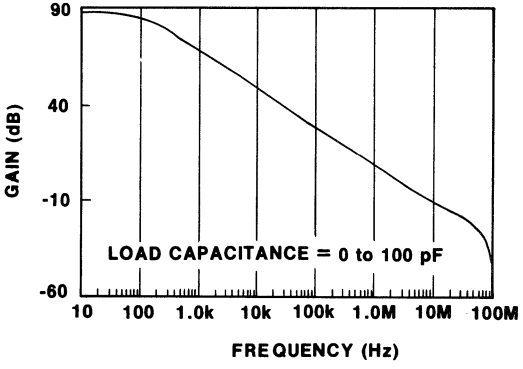


Figure 5. Op-Amp Open-Loop Gain

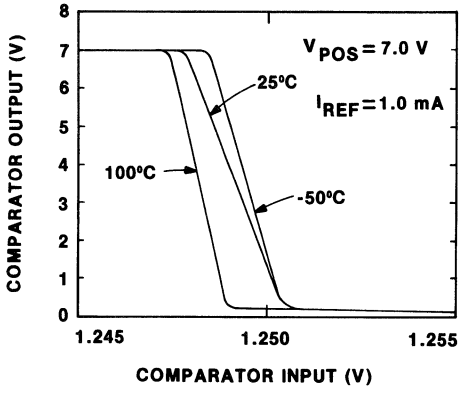


Figure 6. Typical Comparator DC Transfer Characteristics vs Temperature

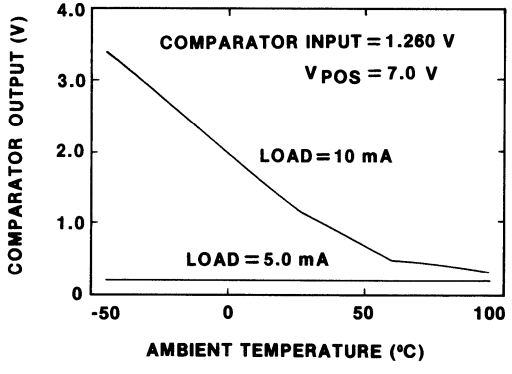


Figure 7. Typical Temperature Characteristics Comparator Output Voltage vs. Comparator Input Overdrive of 10 mV

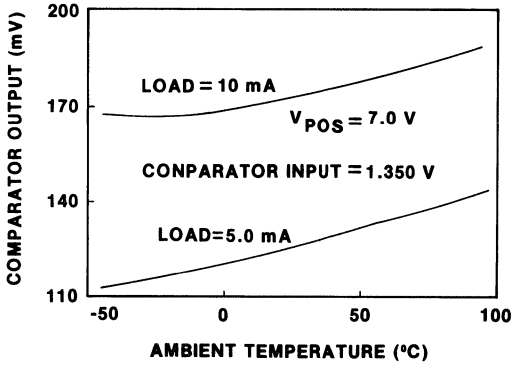


Figure 8. Typical Temperature Characteristics Comparator Output Voltage vs Comparator Input Overdrive of 100 mV

Figure 9 shows the LB1073AB as it is used in a dc-dc converter application. This application is a 48 V to 5 V, 20A converter, and features high-voltage shutdown and current limiting.

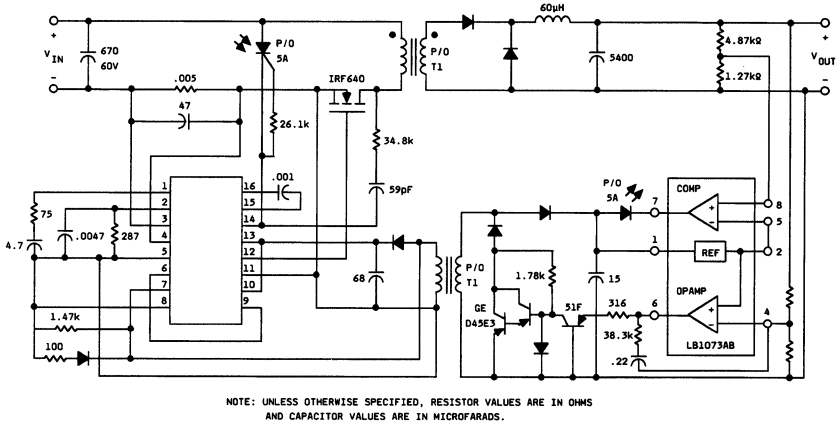
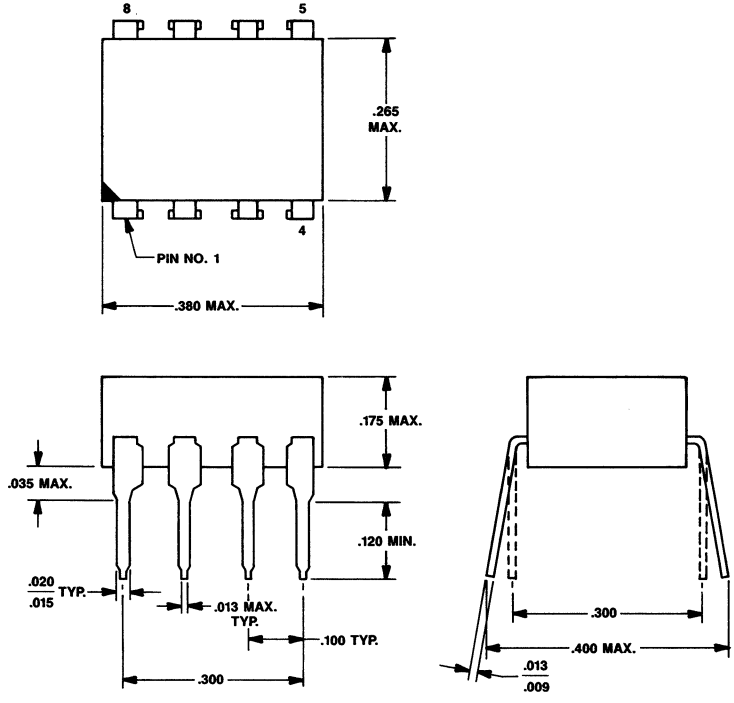


Figure 9. dc-dc Converter Application

Outline Drawing (Dimensions in Inches)



Note 1: Pin numbers are shown for reference only.

Ordering Information

Device	Comcode
LB1073AB	104387634

PRELIMINARY

Description

The LB1081-Type Voltage References represent a family of low-power control devices, each designed to provide a specific output within the range of 4 to 8 volts.

Offering multipurpose applications, all circuits are characterized by low noise, medium current, and a predetermined output voltage. As a special design consideration, the reference voltage is set during manufacture by applying a voltage waveform to fusible, on-chip resistors.

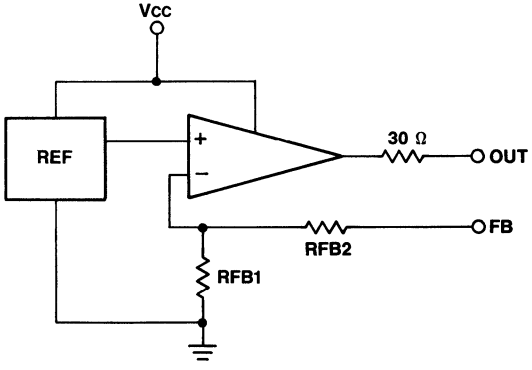
When used with the appropriate external components, the devices function as negative voltage regulators and high-output voltage regulators, and are suitable in environments requiring high current with low-impedance capabilities. Additionally, they are ideal for use in instrumentation equipment, measurement devices, and monitoring systems.

The nominal output current is 5 mA; the temperature coefficient for the LB1081AC through LB1081EC is 0.0075%/°C, and 0.0045%/°C for the LB1081FC. Output current limiting is set at approximately 30 mA to provide short-circuit protection. The LB1081 Voltage Reference family is available in a 16-pin plastic DIPs.

Features

- Five pre-set output options:
  - * LB1081AC—4 V
  - * LB1081BC—5 V
  - * LB1081CC—6 V
  - * LB1081DC—7 V
  - * LB1081EC and LB1081FC—8 V
- Factory programmable reference voltages
- Negative-voltage and high-voltage capabilities
- Medium-current and high-current capabilities
- Output current limiting, 30 mA
- Low temperature coefficient: LB1081AC-EC, 0.0075%/°C; LB1081FC, 0.0045%/°C

Functional Diagram



Note: The value of RFB2 and corresponding codes are shown in the table.

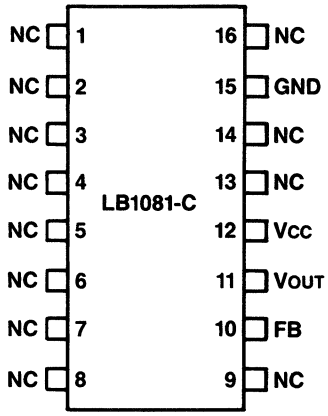
Code	RFB2*	TC VOUT**
LB1081AC	5.5 kΩ	±.0075%/°C
LB1081BC	7.5 kΩ	±.0075%/°C
LB1081CC	9.5 kΩ	±.0075%/°C
LB1081DC	11.5 kΩ	±.0075%/°C
LB1081EC	13.5 kΩ	±.0075%/°C
LB1081FC†	13.5 kΩ	±.0045%/°C

* RFB1 = 2.48 k ohms and may be trimmed via meltback path to achieve precision output voltage.

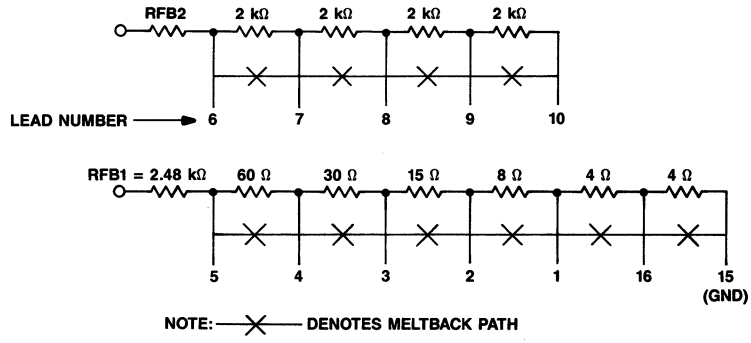
** TC VOUT denotes temperature coefficient of output voltage.

† The LB1081EC and LB1081FC are electrically similar except for the noted difference in TC VOUT.

Pin Diagram



Package Connection Diagram



Maximum Ratings*

(T_A = 25°C unless otherwise specified)

Rating	Value	Unit
Power Supply Current (I_{LOAD})	30	mA
Power Supply Voltage (+Vs	15	V
Power Dissipation (P_{DISS})**	350	mW
Storage Temperature Range (T_{STG})	−40 to +125	°C
Operating Temperature Range	0 to 85	°C

* Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

** Derate at 3.5 mW/°C for temperature within the range of 25 to +125°C.

Pin Descriptions

Pin	Name/Function	Pin	Name/Function
1	Meltback NC†	9	Meltback NC†
2	Meltback NC†	10	$V_{FEEDBACK}$
3	Meltback NC†	11	Output (V_O)
4	Meltback NC†	12	Power Supply Voltage (+Vs)
5	Meltback NC†	13	Open
6	Meltback NC†	14	Open
7	Meltback NC†	15	Ground
8	Meltback NC†	16	Meltback NC†

† No connection, terminal should not be used as a tie point.

Electrical Characteristics*

(T_A = 25°C)

Characteristic and Conditions		Symbol	Min	Max	Unit
Power Supply Voltage		+Vs	10**	15	V
Output Voltage	LB1081AC	Vo(11,15)	3.988	4.012	V
	LB1081BC		4.985	5.015	
	LB1081CC		5.982	6.018	
	LB1081DC		6.979	7.021	
	LB1081EC, FC		7.976	8.024	
Line Regulation (Figure 1)	+Vs = 10** to 15 V	ΔVo	—	25	mV
Load Regulation (Figure 2.)	I_{LOAD} = 1.0 mA to 11 mA		—	10	
Output Noise Voltage	I_{LOAD} = 5.0 mA, C_L = 5.0 μF, C_{REF} = 1.0 μF	NVo	—	100	μV
Power Supply Current	+Vs = 12.4 V	+Ips	—	2.5	mA
Output Current		Io	—	10	
Short-Circuit Output Current		Isco	—	30	
Output Impedance	I_{LOAD} = 5.0 mA, C_L = 5.0 μF	Zout	—	1.5	Ω
Temperature Coefficient of Output Voltage†		TCVo	—	0.6	%/°C

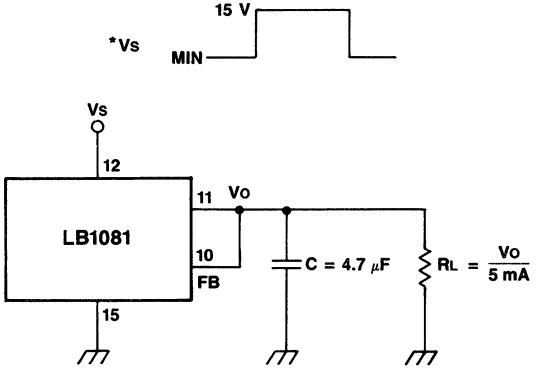
* These characteristics are assured by appropriate manufacturing specification limits.

** Or a minimum of 3 V above the output voltage, whichever is greater.

† The output voltage is measured at 25°C and 85°C and the curve is assumed to be linear. The maximum change will be as specified.

Test Circuits

Resistor values selected for all test circuits are characterized by a nominal ± 1% tolerance; capacitors, ± 10%.



*Vs MIN = Vout + 3 V or + 10 V, whichever is greater

Figure 1. Line Regulation (ΔVo < 25 mV)

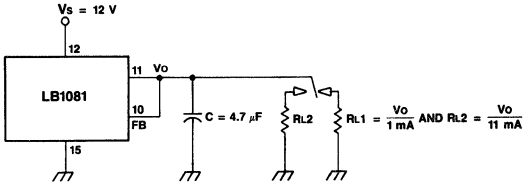


Figure 2. Load Regulation

($\Delta Vo < \frac{Vo}{11\ mA}$)

Characteristic Curves

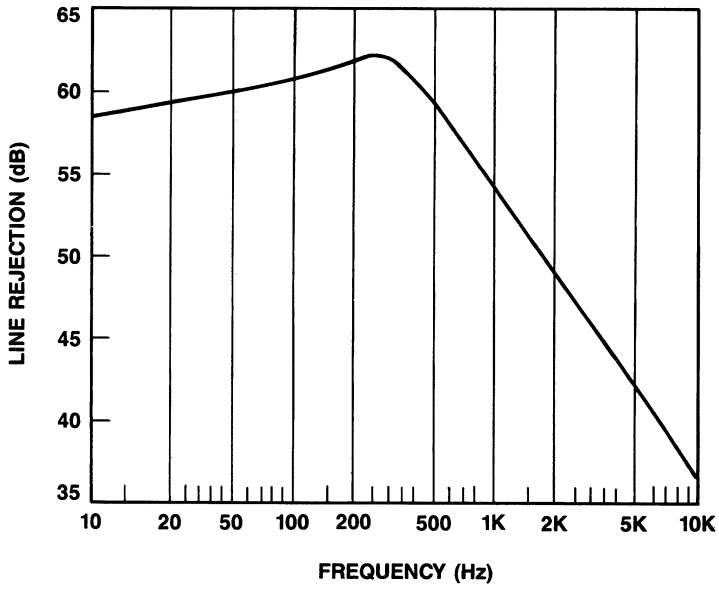


Figure 3. Typical Line Rejection vs. Frequency

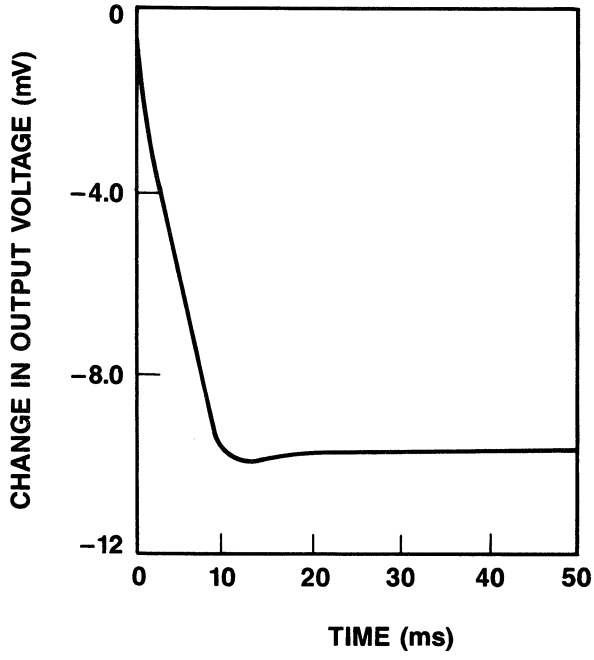


Figure 4. Typical Output Step Response

Characteristic Curves
(Continued)

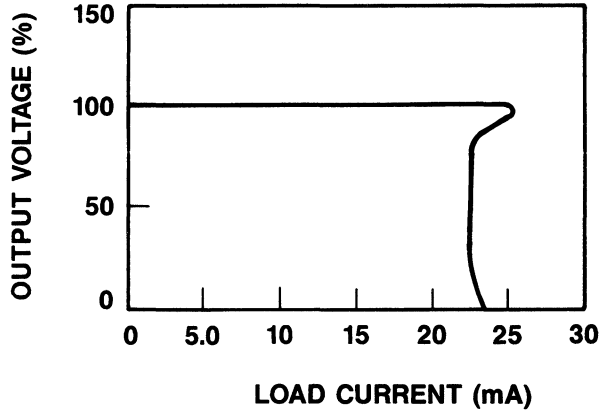


Figure 5. Typical Output Voltage vs. Load Current

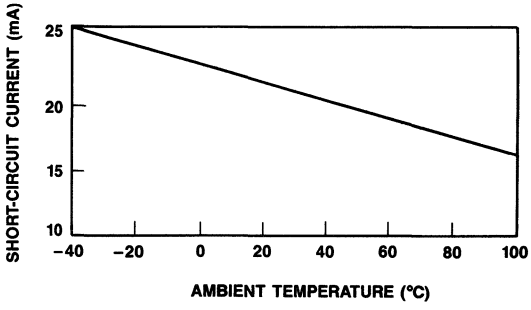


Figure 6. Typical Short-Circuit Current vs. Temperature

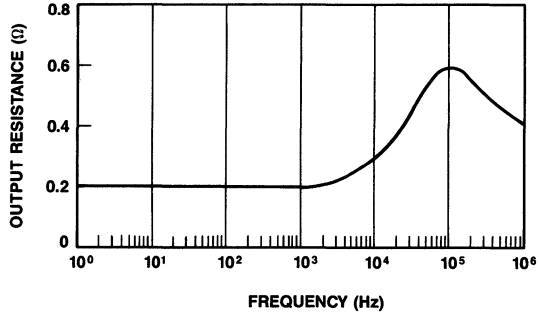


Figure 7. Typical Output Resistance vs. Frequency

Applications

The diagrams below show the connections necessary for the various options available with the LB1081CC. Similar combinations and options are available with the other devices in this series.

Figure 8 shows that with the addition of a discrete transistor, high current with low-output impedance capability is provided.

The basic circuit connections which provide low noise, medium current, and regulated output voltage at the value determined are shown in Figure 9.

Appropriate additions, as shown in Figure 10, allow the basic device to be used as a negative voltage regulator. Figure 11 shows the circuit as designed for use as a high-voltage regulator.

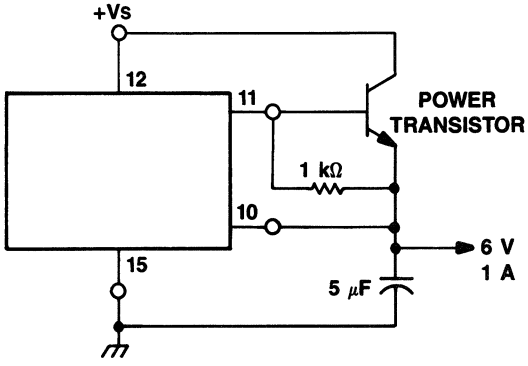


Figure 8. High-Current Application

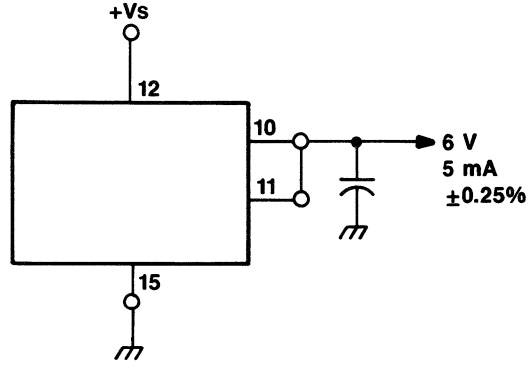


Figure 9. Medium-Current Application

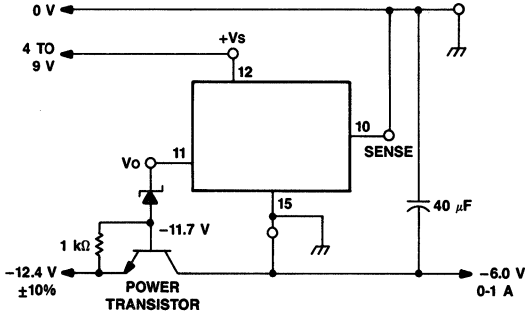


Figure 10. Negative 6.0 V Application Using the LB1081CC 6 V Reference

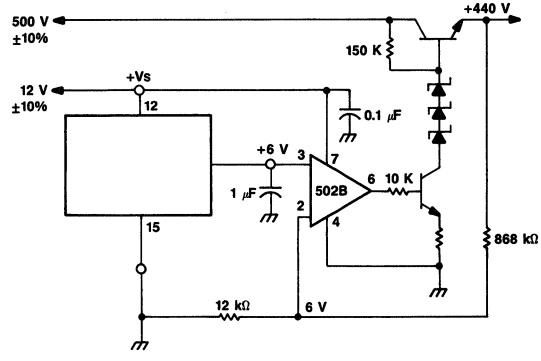
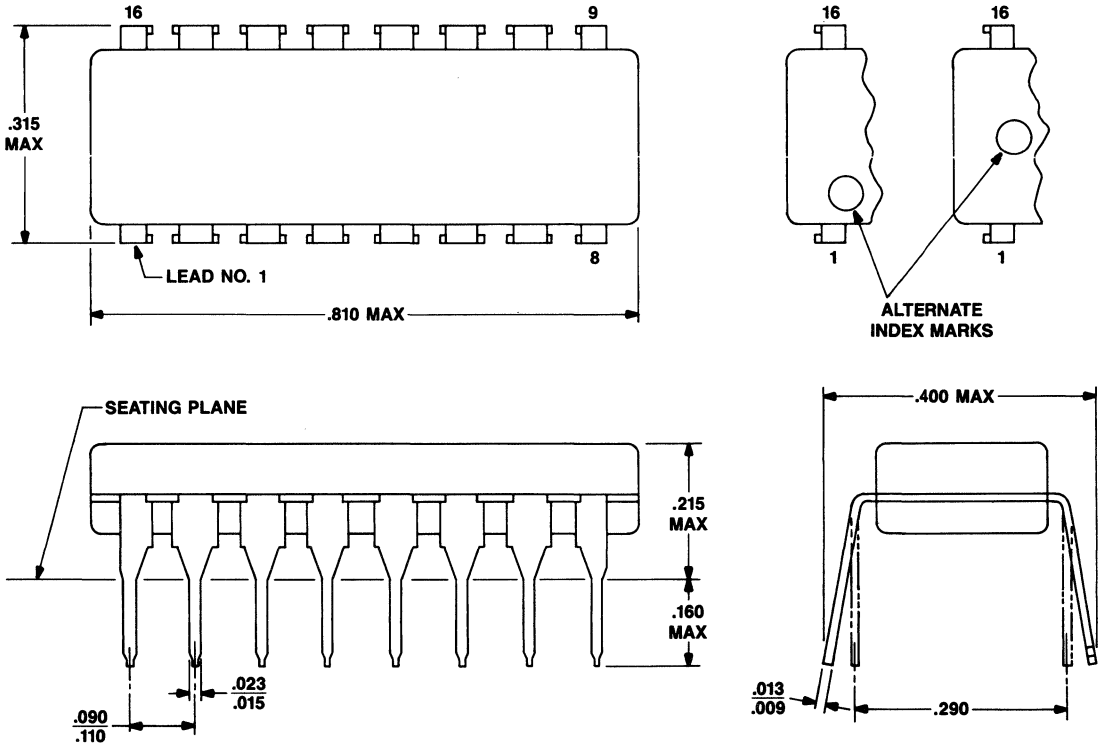


Figure 11. High-Voltage Application Using the LB1081CC 6 V Reference

Outline Drawing

(Dimensions in Inches)



Ordering Information

Device	Comcode
LB1081AC	104394416
LB1081BC	104394424
LB1081CC	104394432
LB1081DC	104394440
LB1081EC	104304457
LB1081FC	104412606

Description

The LB1117AC integrated circuit is a Pulse-Width Modulator (PWM) designed for use in dc-to-dc converters and in switching regulators requiring a single-power switching transistor. Essentially, it provides the control functions necessary for constant frequency, pulse-width modulated switching power supplies. The circuit consists of a band-gap voltage reference, operational amplifier, sense amplifier, ramp generator, complementary output comparator, a power transistor for the PWM function, and a differential amplifier for the voltage regulation and current limiting functions.

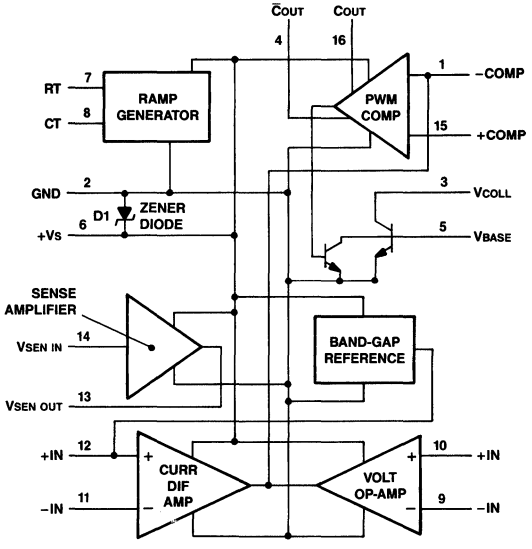
Additionally, the device features a 7.0 V, 100 mW Zener that may be used with an external resistor to function as a shunt voltage regulator for the control circuit. The sense amplifier amplifies signals at the negative rail, providing dc current sensing capabilities. Clock synchronization and minimum duty cycle options are also available.

The PWM is suitable for a wide range of applications, including switching regulators, switching power supplies, power converters, and motor speed controllers. It operates with a typical 5.0 supply voltage and, when utilizing the internal Zener, the circuit will operate with much higher input voltages. The device is characterized by a low supply current drain which relaxes power requirements on an external shunt regulator resistor, thereby allowing high-input voltage applications. The LB1117AC Pulse-Width Modulator is available in a 16-pin plastic DIP.

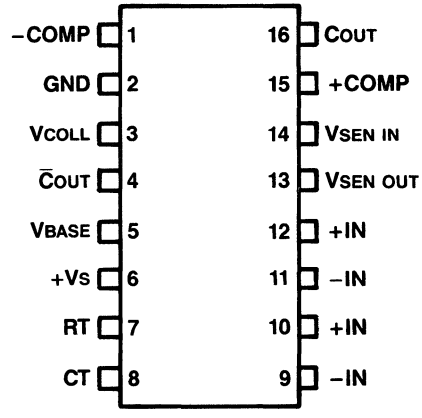
Features

- 7.0 V, 100 mW Zener
- Supply current less than 5.0 mA with 5.0 supply voltage
- Current limit sensing
- On-chip Zener allows operation from 13.0 mA current source (series resistor and high voltage supply)
- On-chip output power transistor capable of sinking a current to 100 mA
- Ramp generation frequency, 200 kHz at 7.5 V

Functional Diagram



Pin Diagram



Maximum Ratings

Rating	Value	Unit
Positive Power Supply Voltage/Current	8/25	V/mA
Positive Voltage for On-Chip Output Power Transistor	30	V
Power Dissipation	600	mW
Storage Temperature Range	−40 to +125	°C
Ambient Operating Temperature Range	0 to 60	°C

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions

Pin	Symbol	Name/Function
1	−COMP	Negative Comparator Input; Output of Voltage op amp and Current Diff. Amp
2	GND	Ground
3	V_{coll}	Collector for On-chip Output Power Transistor
4	$\overline{C}_{OUT}$	Inverted Comparator Output
5	V_{base}	Base of On-chip Output Power Transistor
6	V_S	Power Supply Input
7	R_T	Timing Resistor Connected to Pin 7 and Ground
8	C_T	Timing Capacitor Connected to Pin 8, Ground, and Ramp Generator Output
9	−IN	Negative Voltage Op Amp Input
10	+IN	Positive Voltage Op Amp Input
11	−IN	Negative Current Diff Amp Input
12	+IN	Positive Current Diff Amp Input
13	VSENOUT	Sense Amplifier Output
14	VSENIN	Sense Amplifier Input
15	+COMP	Positive Comparator Input
16	COUT	Non Inverted Comparator Output

Electrical Characteristics

(T_A = 25°C, V_S = 7.5 V, R_T = 34.8 kΩ, unless otherwise specified)

Characteristics	Conditions		Min	Max	Unit
Reference Section:					
Output Voltage	R_L = ∞; Is = 34.7 mA (Fig. 2)		1.18	1.32	V
Power Supply Rejection Ratio	△Vs = −3.0V; R_L = ∞		54	—	dB
Load Regulation	R_L = 1.25 KΩ; Is = 13.7 mA		—	6.0	mV
Bandgap Temperature Coefficient	0°C ≤ t_A ≤ 100°C		—	.012	%/°C
Ramp Generator Section:					
Frequency	C_T = 2610 pF		—	200	kHz
Line Regulation	△Vs = −1.0 V		—	500	Hz
High Ramp Voltage			3.75	5.25	V
Low Ramp Voltage			2.15	2.60	
Current Source			100	170	μA
Voltage Amplifier Section:					
Input Offset Voltage	Vs = 12 V, R_O = 30 kΩ		—	7.0	mV
Input Bias Current			—	−2.5	μA
Input Offset Current			—	0.5	
Power Supply Rejection Ratio			54	—	dB
Open-Loop Gain			66	92	
Common-Mode Voltage Range			0.75	10.5	V
Output Voltage Swing		HIGH	5.8	—	
		LOW	—	0.1	
Comparator Section:					
Input Bias Current			—	5.0	μA
Common-Mode Voltage Range			1.5	V_{CC} − 1	V
Output Voltage Swing	Is = 15.7 mA; R_L = 1.0 K	HIGH	5.5	—	
		LOW	—	0.1	
Current Amplifier Section:					
Input Bias Current			—	−2.5	μA
Output Voltage Low	R_L = 30 kΩ; Is = 12.5 mA		—	0.3	V
Sense Amplifier Section:					
Output Voltage	V_{SEN} = 0 V; Is = 12.5 mA (Fig. 3)		0.0	0.57	V
	V_{SEN} = 0.2 V; Is = 12.5 mA		1.10	1.38	
Voltage Gain	△V_{SENIN} = 0.05 V; Is = 12.5 mA		18	20	dB
Output Transistor Section:					
Breakdown Voltage	I_C = 1.0 mA		30	—	V
Saturation Voltage	I_B = 10 mA; I_C = 100 mA		—	0.55	
Static Current Forward Transfer Ratio	V_{CE} = 1.0 V; IC = 50 mA		25	—	—

Electrical Characteristics (Continued)

(T_A = 25°C, V_S = 7.5 V, R_T = 34.8 kΩ, unless otherwise specified)

Characteristics	Conditions	Min	Max	Unit
Miscellaneous				
Zener Voltage	I_Z = 1.0 mA	6.25	7.15	V
	I_Z = 13.7 mA (Fig. 1)	6.5	7.5	
Supply Current	V_S = 5.0 V, $V_{SEN\ IN}$ = 0 V	2.0	—	mA
	$V_{SEN\ IN}$ = 200 mV; V_S = 5.0 V	—	4.5	

Test Circuits

Resistor values selected for use in all test circuits are characterized by a nominal ± 1% tolerance; capacitors, ± 10%.

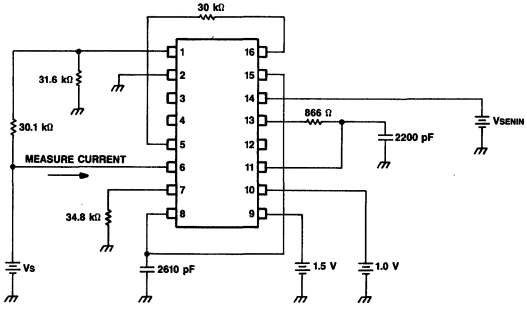


Figure 1. Power Supply Current Test Circuit

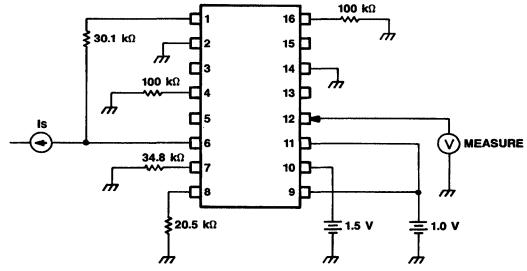


Figure 2. Bandgap Output Voltage Test Circuit

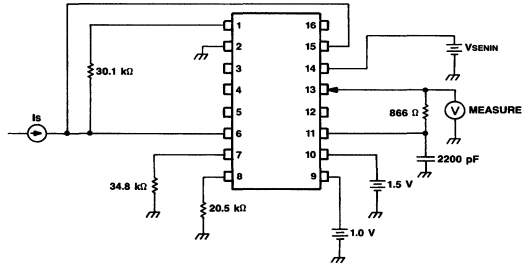


Figure 3. Sense Amplifier Output Voltage Test Circuit

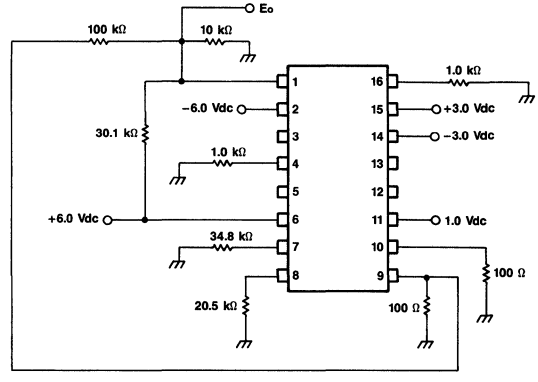


Figure 4. Input Offset Voltage Test Circuit

$$\left(V_{IO} = \frac{E_O}{1000}\right)$$

Test Circuits (Continued)

Ramp Generator Frequency:

$$\left.\begin{array}{l}\dfrac{V_S - 1.8}{500\ \mu A} \leq R_T \leq \dfrac{V_S - 1.8}{135\ \mu A}\end{array}\right\} \text{Limits on } R_T;$$

$$\left.\begin{array}{l}C_T \leq 3000\,\dfrac{(.177\ V_S - .219)}{(.664\ V_S - 1)}\ pF\end{array}\right\} \text{Limits on } C_T;$$

$$T = \frac{1}{\text{Ramp Frequency}}\ ;\ T = \frac{R_T C_T}{(V_S - 1.8)}\,(.487\ V_S - .781)$$

$\dfrac{T}{R_T C_T}$ plotted in Figure 6.

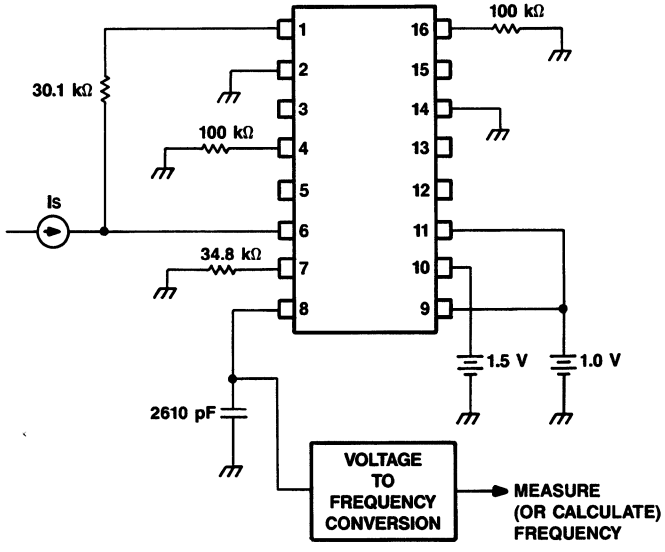


Figure 5. Ramp Generator Frequency Test Circuit

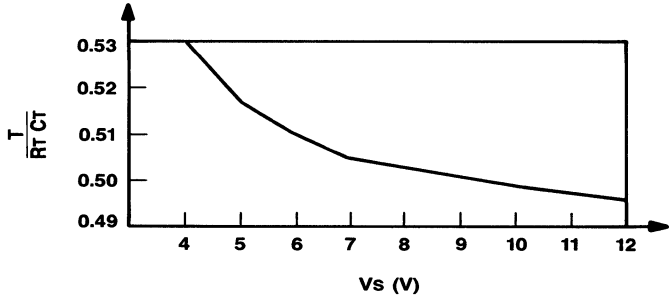
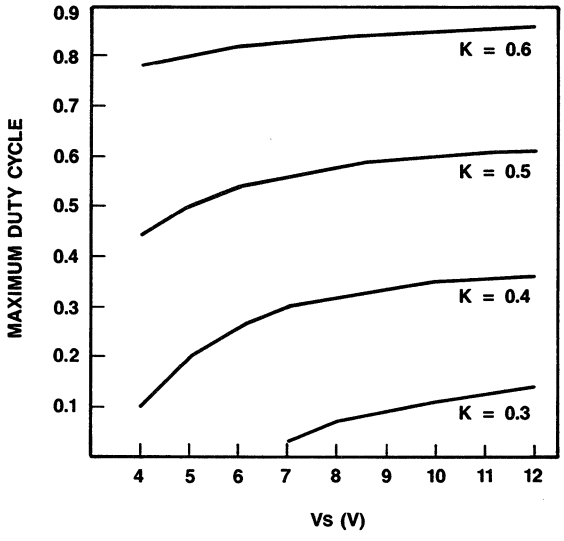
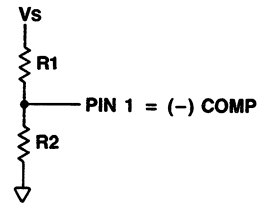


Figure 6. Ratio of Ramp Generator Period (T) to R_T C_T Time Constant vs. Supply Voltage

Characteristic Curves





*Minimum Duty Cycle Resistor Ratio

Minimum Duty Cycle:

$$x = \frac{(K - .177)\,Vs - .781}{.487\,Vs - .781}$$

Duty Cycle Divider Ratios ($K = \frac{R2}{R1 + R2}$)

Figure 7. Maximum Duty Cycle as a Function of Supply Voltage for Various

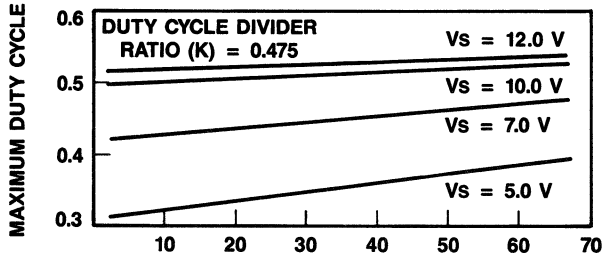


Figure 8. Maximum Duty Cycle as a Function of Temperature for Various Supply Voltages

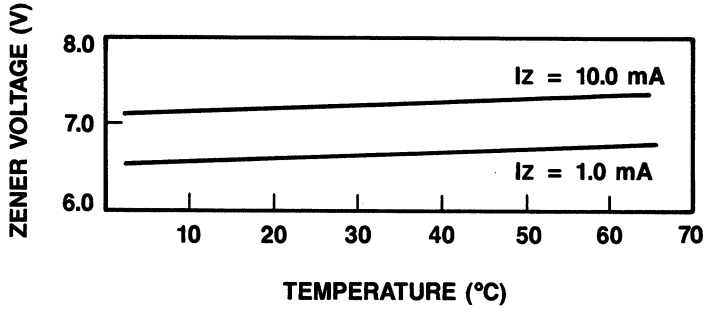
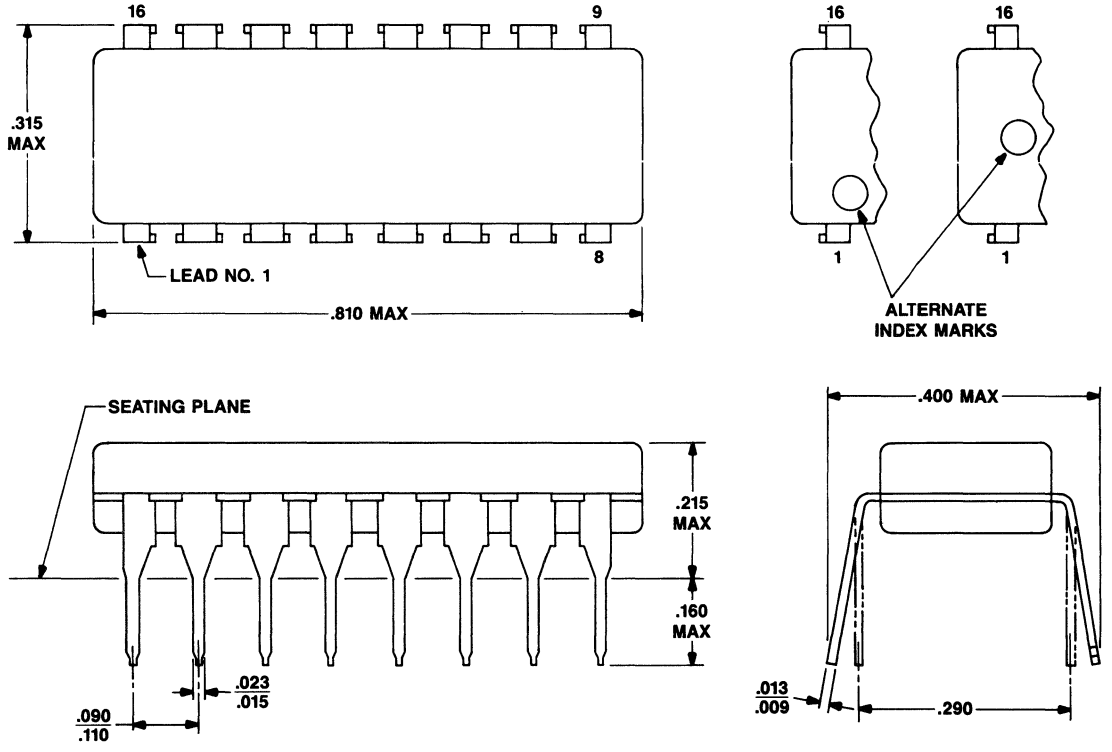


Figure 9. Zener Voltage vs. Temperature at 1 mA and 10 mA

Outline Drawing

(Dimensions in Inches)



Ordering Information

Device	Comcode
LB1117AC	104411756

Description

The LB1132AC Switched-Mode Pulse-Width Modulator (PWM) features a single-ended output which can either sink or source currents up to 200 mA. Consisting of eight functional blocks, the device is suitable for performing the basic pulse-width modulation function in switching power supplies.

Functionally, the PWM includes a 1.25 V temperature-compensated reference capable of supplying up to 1 mA to external circuitry. It also features supervisory circuitry for current limiting, maximum duty-cycle limiting, shutdown and adaptive startup. An internal triangular wave-shape oscillator (providing equal rise and fall times) is controlled by external components. The output from the comparator is an ECL tree-configured signal feeding into the logic block. Additionally, the logic section provides noise immunity using an edge-triggered input which allows only one transition per clock cycle.

The LB1132AC is characterized chiefly by high speed and a powerful FET driver. It is capable of operating at a clock frequency of 500 kHz, and can turn on or off a 1000 pF external gate FET in less than 50 ns. Offering superior thermal stability, the PWM incorporates a bandgap voltage reference with a temperature coefficient of less than 100 ppm/°C.

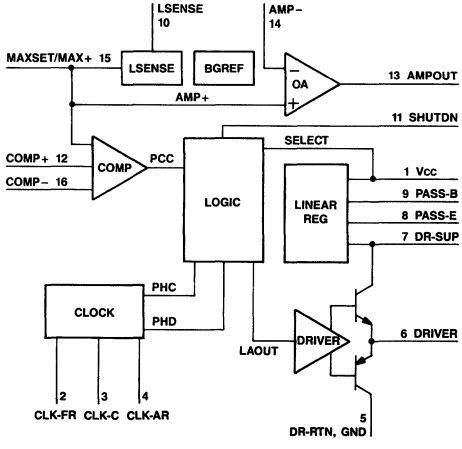
The PWM cannot operate directly from a 48 V battery, thus it generates a 9 V external supply using an internal linear regulator to control an off-chip, discrete, high-voltage bipolar transistor. To control the amount of power delivered to a power supply load, the PWM adjusts the "on-time" of the primary transformer FET switch. "On-time" is regulated by comparing a feedback signal from the power supply output (load) with a slope-compensated pulse; the pulse is proportional to the primary transformer current. Also, the comparator limits the maximum duration of FET switch "on-time," and keeps the FET switch off during startup conditions.

The LB1132AC Switched-Mode Pulse-Width Modulator is available in a 16-pin plastic DIP.

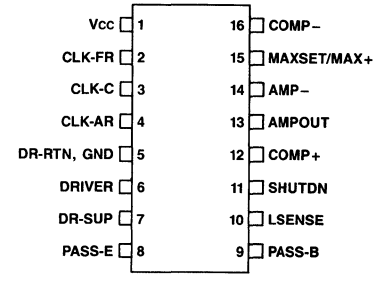
Features

- High clock frequency
- Manual power-down override
- Prevents start-up damage
- Noise immunity logic
- Eliminates excessive "on" time
- Excellent thermal stability
- Low power consumption
- Adaptive startup and shutdown control
- 500 kHz clock frequency (adjustable)
- Powerful FET driver
- Shutdown lead
- Double-pulse suppression
- Maximum duty cycle control
- Vcc temperature coefficient, 200 ppm/°C
- Quiescent current less than 7.0 mA
- Single source/sink output: ±200 mA
- External oscillator synchronization

Functional Diagram



Pin Diagram



Maximum Ratings*

Parameter	Rating	Unit
Power Supply Voltage	**	V
Power Dissipation (25°C)	550	mW
Storage Temperature Range	−40 to +125	°C
Operating Temperature Range	−25 to +85	°C

* Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

** A 9 V power supply is generated internally through a pass transistor (V_{CC} at pin 1). The requirements on the external pass transisitor collector emitter breakdown voltage (BV_{CEO}) range is the line voltage minus 9 V. The line voltage must be greater than 12 V.

Pin Descriptions

Pin	Symbol	Name/Function
1	Vcc	Provides a regulated output voltage of 9.0 (± 0.5) V.
2 3 4	CLK-FR CLK-C CLK-AR	Clock connection to an external amplitude-adjusting resistor, and an external frequency-adjusting resistor. The clock provides a triangular waveshape with a frequency of 1/2 (RC), and an amplitude of 3 to 6 V.
5	DR-RTN, GND	Return (common) for the high-current output stage of the driver circuit. Pin 5 should be connected to a low-ohmic ground because of its high noise content.
6	DRIVER	The output of the driver is capable of sourcing or sinking in excess of 200 mA. The driver can turn on or turn off a 100 pF gate FET in less than 50 ns.
7	DR-SUP	Provides the current surge needed (as high as 200 mA) to switch the FET. This pin must be tied to a capacitor to ground.
8 9	PASS-B PASS-E	Connections to the base and emitter, respectively, of an external NPN transistor. Pass-E terminal provides dc power for the LB1132AC.
10	LSENSE	Line sense monitors the line voltage to provide adaptive start-up.
11	SHUTDN	Input pin intended for emergency shutdown of the FET driver and is TTL-compatible. A logic high shuts off the FET driver.
12 16	COMP+ COMP−	Noninverting and inverting inputs, respectively, to a 3-input comparator. The comparator controls the duty cycle of the FET by comparing the operational signal to the clock signal.
14 13	AMP− AMPOUT	Inverting input and output, respectively, to the operational amplifer. Functionally, the operational amplifier provides a dc signal for comparison with the clock.
15	MAXSET/ MAX+	Limits the duty cycle of the FET driver and is connected to the positive lead of the operational amplifier.

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic and Conditions	Symbol	Min	Typ	Max	Unit
Quiescent dc Operating Current	I_{DC}	4.0	6.5	7.0	mA
Vcc with 3 kΩ load	V_{CC}	8.5	9.0	9.5	V
Op-Amp Output Low	Op-Amp$_{OL}$	1.2	1.5	2.0	V
Op-Amp Output High	Op-Amp$_{OH}$	6.5	8.0	8.5	V
Op-Amp ac Gain @ 10 kHz	Op-Amp$_G$	37	57	60	dB
Op-Amp Offset Voltage	Op-Amp$_V$	−6.0	−1.4	+1.0	mV
Clock-C Current Source with 12.5 k @ RFR	$I_{ICKL\ SOURCE}$	80	100	120	μA
Clock-C Current Sink with 12.5 k @ RFR	$I_{CLK\ SINK}$	80	100	120	μA
Source and Sink Current Ratio		.96	1.0	1.04	—
Voltage LSENSE High	$V_{LSENSE\ H}$	4.0	4.5	5.0	V
Voltage LSENSE Low	$V_{LSENSE\ L}$	−2.0	1.0	2.0	V
Drive Supply Voltage	V_{DS}	10.0	10.7	11.0	V
Driver Voltage High with 35 Ω Load	$V_{DS\ H}$	7.0	8.8	9.4	V
Driver Current Sink @ 2 V	$I_{DR\ SINK}$	200	235	500	mA

Test Requirements

(At 25°C unless otherwise specified)

Characteristic	Conditions	Min	Typ	Max	Unit
dc Operating Current	Figure 1; Measure I_{DC}	4.0	6.5	7.0	mA
Reference Voltage (V_{CCO})	Figure 2; Measure Pin 1 (V_{CC})	8.5	9.0	9.5	V
Operational Amplifier, Output Voltage Swing (High)	Figure 3; Measure Pin 13 (AMPOUT) Pin 14 = 1.00 V (AMP− Pin 15 = 1.25 V (MAXSET/MAX+)	6.5	8.0	8.5	V
Operational Amplifier, Output Voltage Swing (Low)	Figure 3; Measure Pin 13 (AMPOUT) Pin 14 = 1.25 V (AMP−) Pin 15 = 1.00 V (MAXSET/MAX+)	1.2	1.5	2.0	V
Driver Supply Voltage	Figure 4; Measure Pin 7 (DR-SUP)	10.0	10.7	11.0	V
Driver Voltage (High)	Figure 4; Measure Pin 6 (DRIVER) Pin 11 = 35 Ω, 2 W Resistor to GND.	7.0	8.8	9.4	V
Driver Current, Sink	Figure 4*	200	235	500	mA
Clock-C, Source Current	Figure 5; Pin 2 = +7.0 V (CLK-C)	80	100	120	μA
Clock-C, Sink Current	Figure 5; Pin 2 = +2.0 V (CLK-C)	80	100	120	μA
Clock-C Ratio (Sink I/Source I)	Figure 5	0.96	1.00	1.04	—

* Shutdown must be kept high during this test.

Electrical Requirements

(At 25°C unless otherwise specified)

The characteristics shown below are certified through production (ac with feedback loop) op-amp tests.

Characteristic	Test Condition	Min	Typ	Max	Unit
Operational Amplifier, Open-Loop Voltage Gain @ 10 kHz	Figure 6; V_{IN} = 100 mVrms V_{CM} = 1.25 V	37	57	65	dB
Operational Amplifier, Input-Offset	Figure 6; V_{IN} = 0 V_{CM} = 1.25 V	—	—	+1.0 −6.0	mV

Test Circuits

Resistor values selected for use in all test circuits are characterized by a nominal ±1% tolerance; capacitors, ±10%.

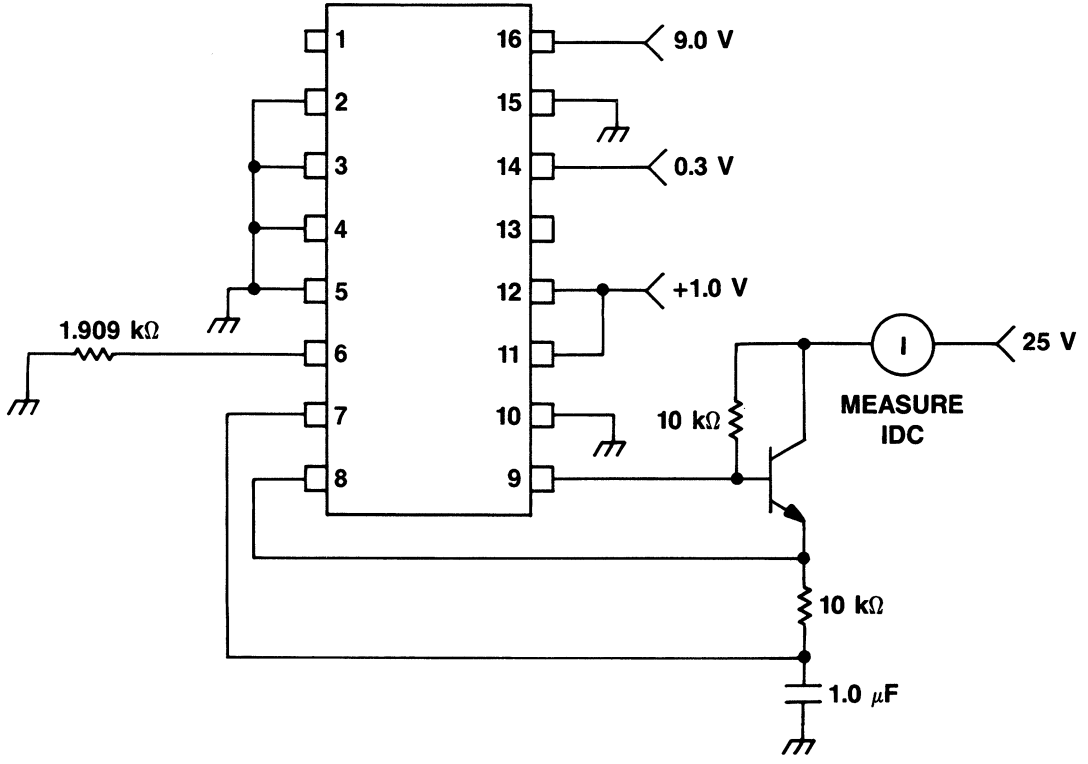


Figure 1. dc Operating Current

Test Circuits (Continued)

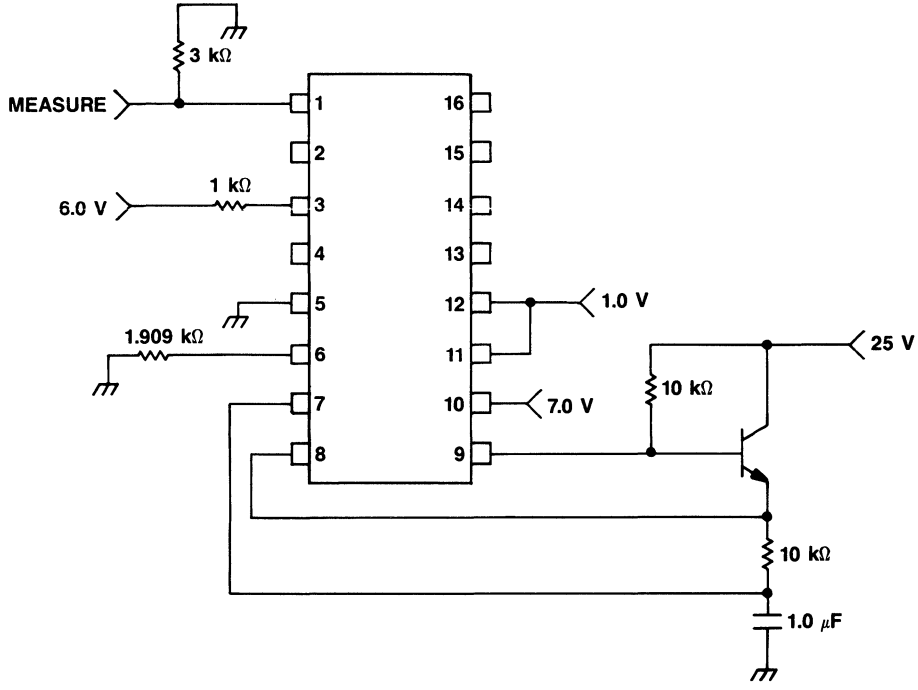


Figure 2. Reference Voltage

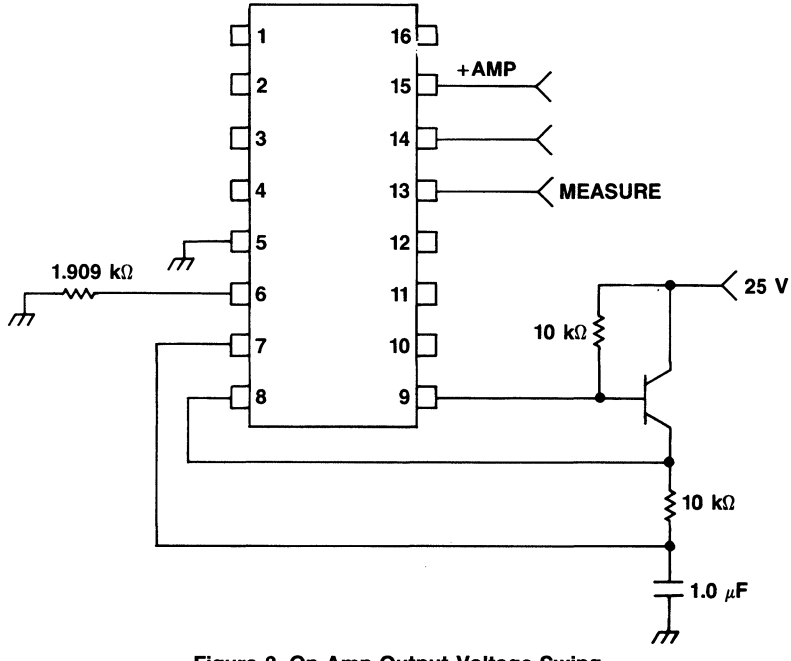


Figure 3. Op Amp Output Voltage Swing

Test Circuits (Continued)

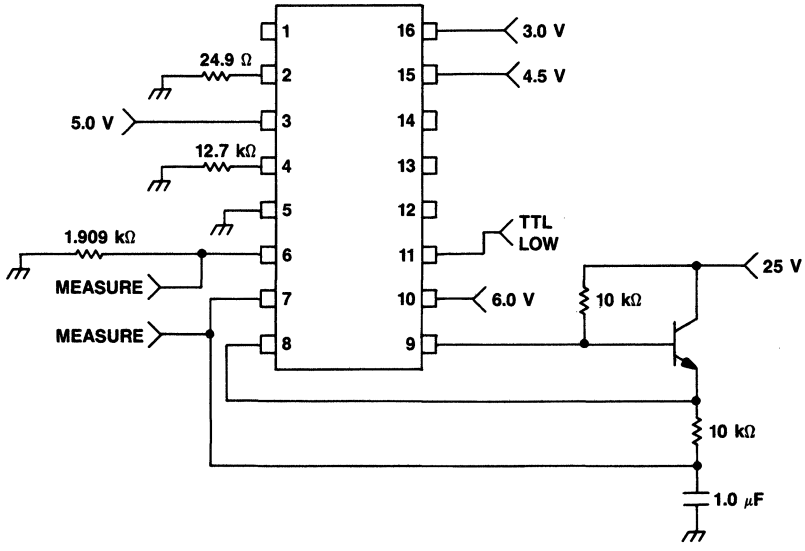


Figure 4A. Driver Output Test

Note: Shutdown must be kept high during driver current (sink) test.

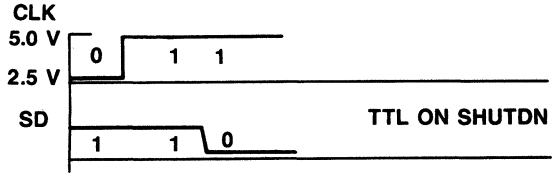


Figure 4B. Driver "ON" Sequence

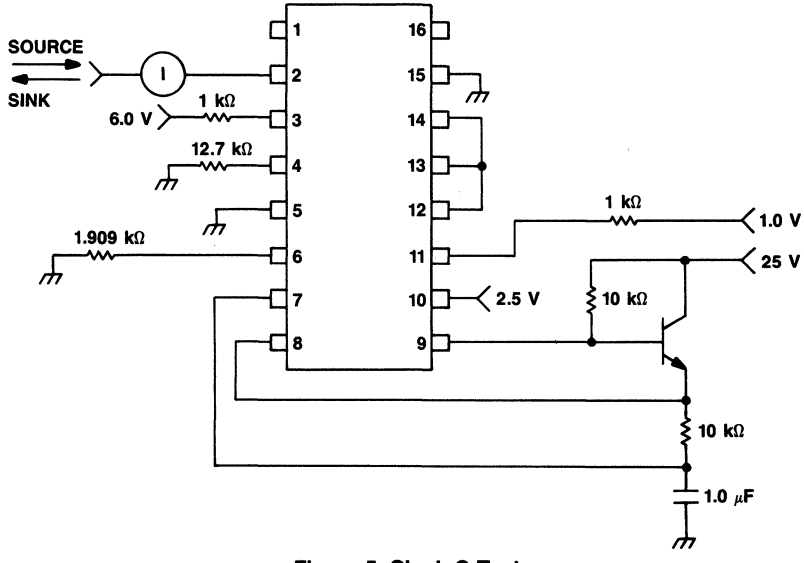


Figure 5. Clock-C Test

Test Circuits (Continued)

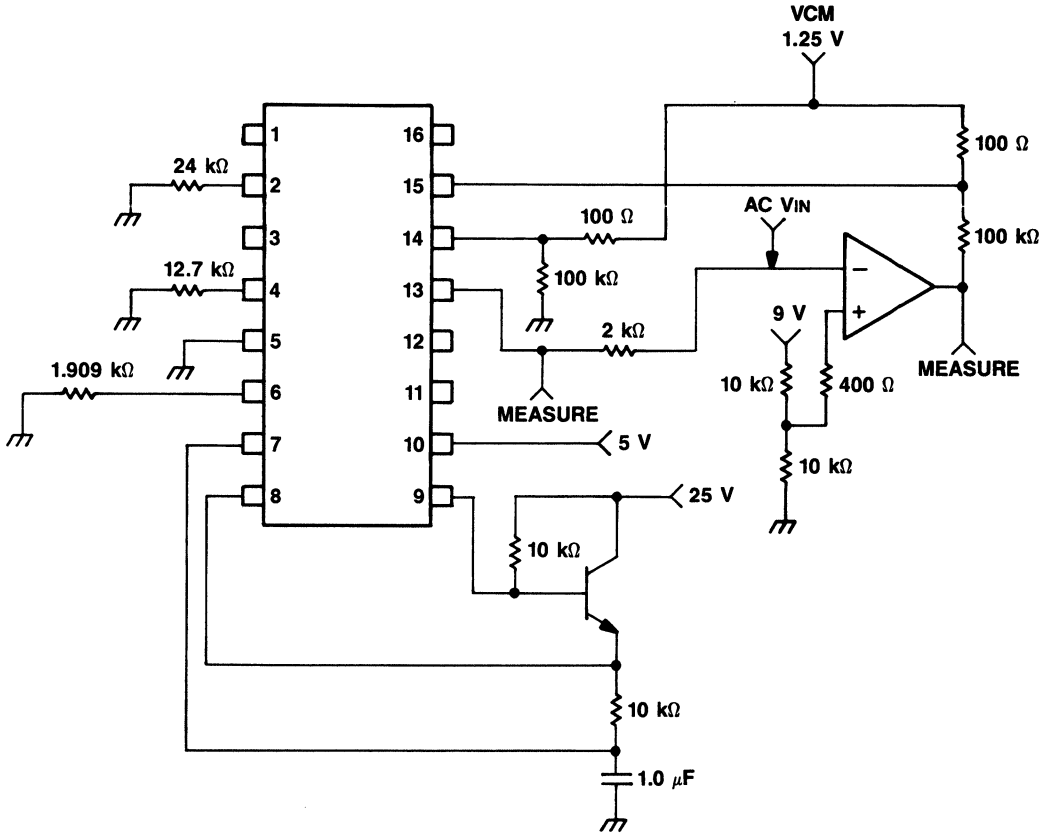


Figure 6. Open Loop Voltage Gain @ 10 kHz

Characteristic Curve

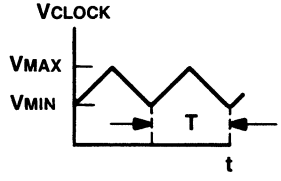


Figure 7. Voltage vs. Time

C_{FR}, R_{FR} and R_{AR} accurately set the clock frequently as well as the maximum and minimum voltages. V_{MAX} is set to 6 volts for normal operation.

$$R_{AR} = \frac{VBG}{I_{RAR}} \qquad R_{FR} = \frac{V_{MAX}}{2} \frac{R_{AR}}{VBG} \qquad C_{FR} = \frac{1}{2f\,R_{FR}} \qquad V_{MIN} = \frac{V_{MAX}}{2}$$

Typical Values: $I_{RAR} = 100\ \mu A$, $VBG \approx 1.25$ V

Application

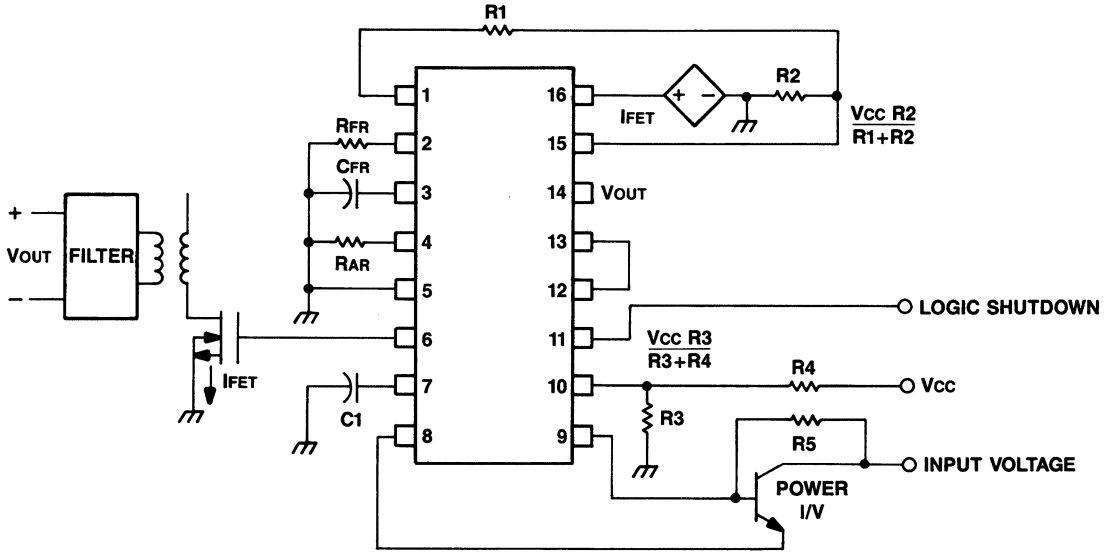
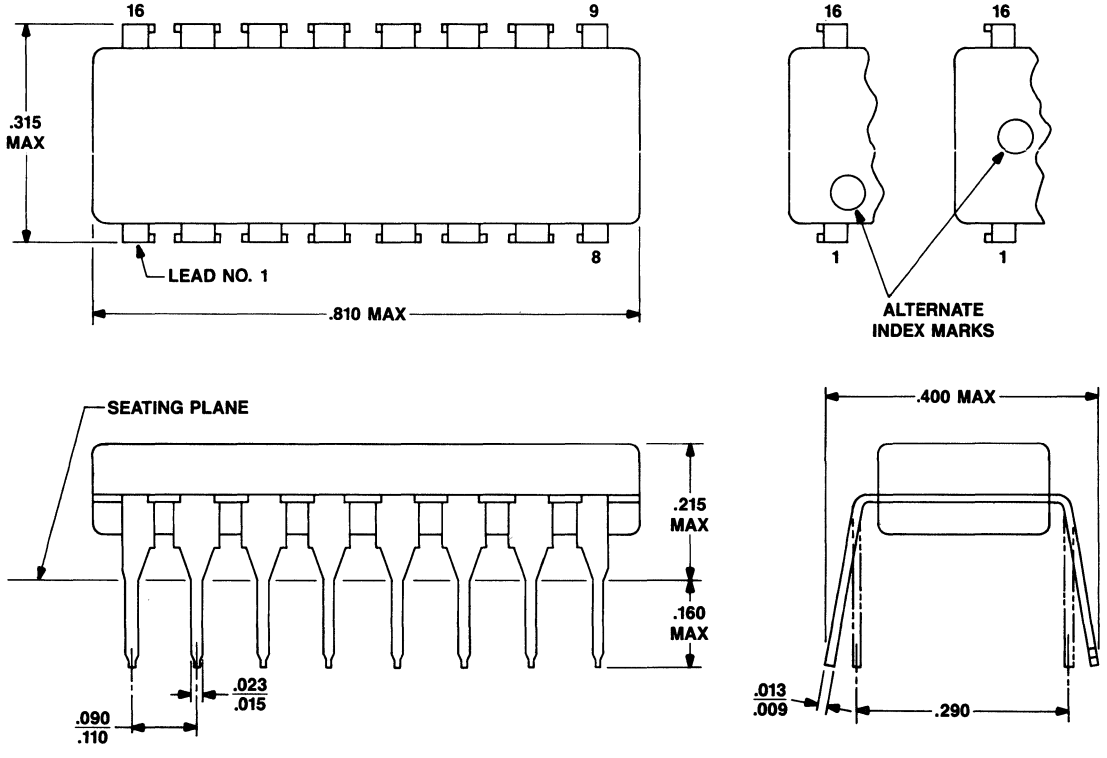


Figure 8. LB1132AC Switched-Mode PWM Application Diagram

Outline Drawing

(Dimensions in Inches)



Ordering Information

Device	Comcode
LB1132AC	104413802

PRELIMINARY

Description

The LH1056-Type Multipurpose Solid-State Relays (MSR) are low-cost, bi-directional, SPST switches which can replace mechanical relays in many applications. Output is rated at 350 volts and can handle loads up to 100 mA. The MSR is UL approved for 1500 Vrms of input/output isolation and is available in a 6-pin plastic DIP. The MSR device will switch both ac and dc loads, but is primarily intended for audio frequency or dc applications.

The circuit consists of one GaAlAs LED to optically couple the control signal to a dielectrically isolated high-voltage integrated circuit. The typical ON-Resistance is 30 ohms at 25 mA (LH1056AT), 27 ohms at 25 mA (LH1056CT), and is exceptionally linear up to 50 mA. Beyond 50 mA, the incremental resistance becomes even less, thereby minimizing internal power dissipation. The MSR also has internal current limiting which clamps the load current to 150 mA to insure that the device survives during power surges. The MSR will survive FCC lightning test number 68-302 when it is properly protected.

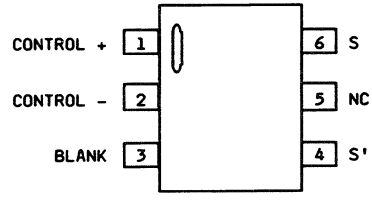
Features

- Low On-resistance
- Clean, bounce-free switching
- 1500 Vrms input/output isolation (optically coupled)
- dv/dt typically better than 500 V/μs
- High-surge capability
- Low power consumption
- Noise-free operation
- No electromagnetic interference
- High voltage monolithic IC fabricated in a dielectric isolation process

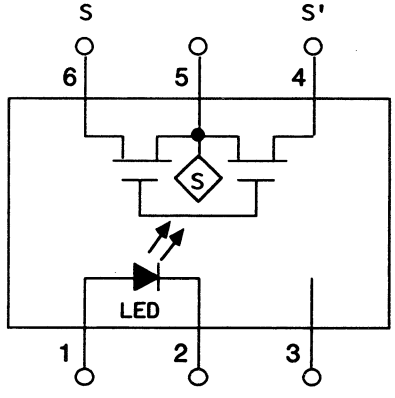
Applications

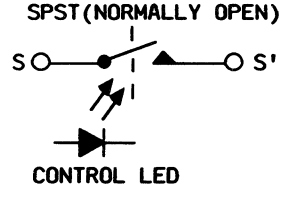
- Telephone switchhook
- High-voltage testers
- Industrial controls
- Triac driver
- Isolation switching

Pin Diagram



Functional Diagram





EQUIVALENT RELAY DIAGRAM

Maximum Ratings

(At 25°C unless otherwise specified)

Rating	Value	Unit
Ambient Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−40 to +100	°C
Pin Soldering Temperature (t = 15 sec max.)	300	°C
Input/Output Voltage Isolation	1500	Vrms
LED Input Ratings		
Continuous Forward Current	20	mA
Reverse Voltage	10	V
Output Operation		
Operating Voltage	350	V
DC or Peak Load Current	100	mA

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions

(Also see Functional and Pin Diagrams)

Pin	Symbol	Name/Function
1 2	Control + Control −	These pins are the positive and negative inputs respectively to the input control LED. An appropriate amount of current through the LED will close the circuit path between S and S'.
6 4	S S'	These pins are the outputs. The pin designated as S represents one side of a relay pole. The pin designated as S' (S Prime) is the complementary side of a relay pole. This relay pole is normally open unless sufficient control current is flowing.
3	Blank	This pin may be used as a tie-point for external components. Voltage on this pin should not exceed 300 volts.
5	NC	This pin is connected to internal circuitry. It should **not** be used as a tie-point for external circuitry.

Characteristics

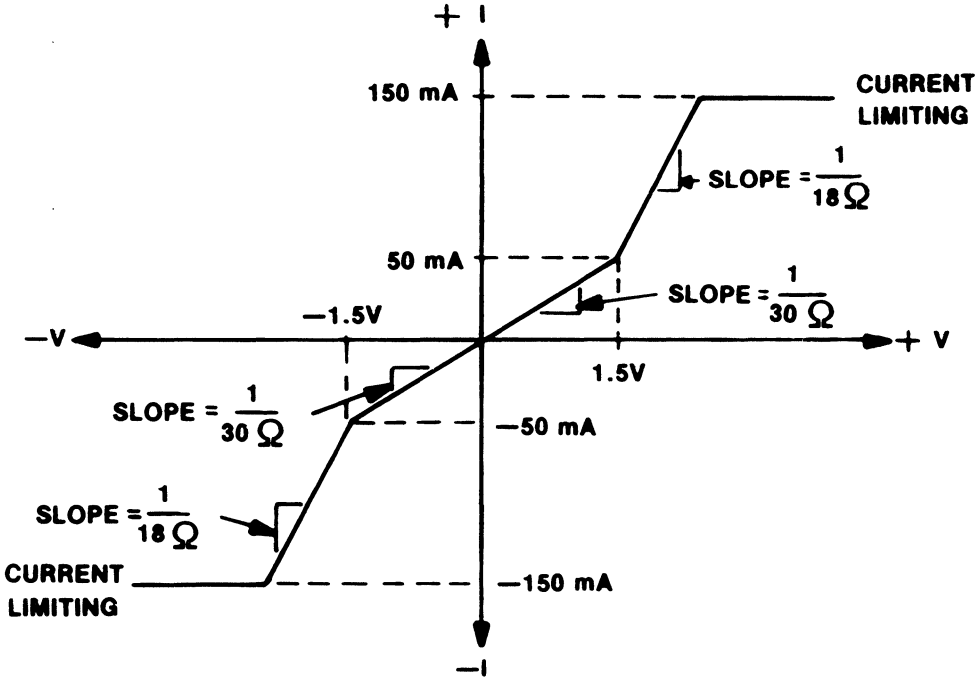


Figure 1. Typical ON Characteristics

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic and Test Condition		Min	Typ	Max	Unit
*LED Forward Current for Turn-On (LH1056AT)	I_{LOAD} = 100 mA, 25°C	—	1.5	2.5	mA
	I_{LOAD} = 80 mA, 70°C	—	2.5	5.0	
LED ON Voltage @ 10 mA		1.15	1.30	1.45	V
ON Resistance @ 25 mA	(LH1056AT)	20	30	50	Ω
	(LH1056CT)	15	27	30	Ω
Breakdown Voltage @ 50 μA		350	380	—	V
Output Off-State Leakage Current	100 V, I_{LED} = 0 μA	—	1.0	200	nA
	100 V, I_{LED} = 200 μA	—	0.1	2.0	μA
	300 V, I_{LED} = 200 μA	—	0.1	5.0	μA
Turn-On Time	See Figure 6	—	1.0	2.0	ms
Turn-Off Time		—	0.5	2.0	
Feedthrough Capacitance, Pin 4 to 6 (4 V p-p, 1 kHz)		—	24	—	pF

* Supply a minimum of 6 mA LED current to insure proper operation over the full operating temperature range.

Test Circuits

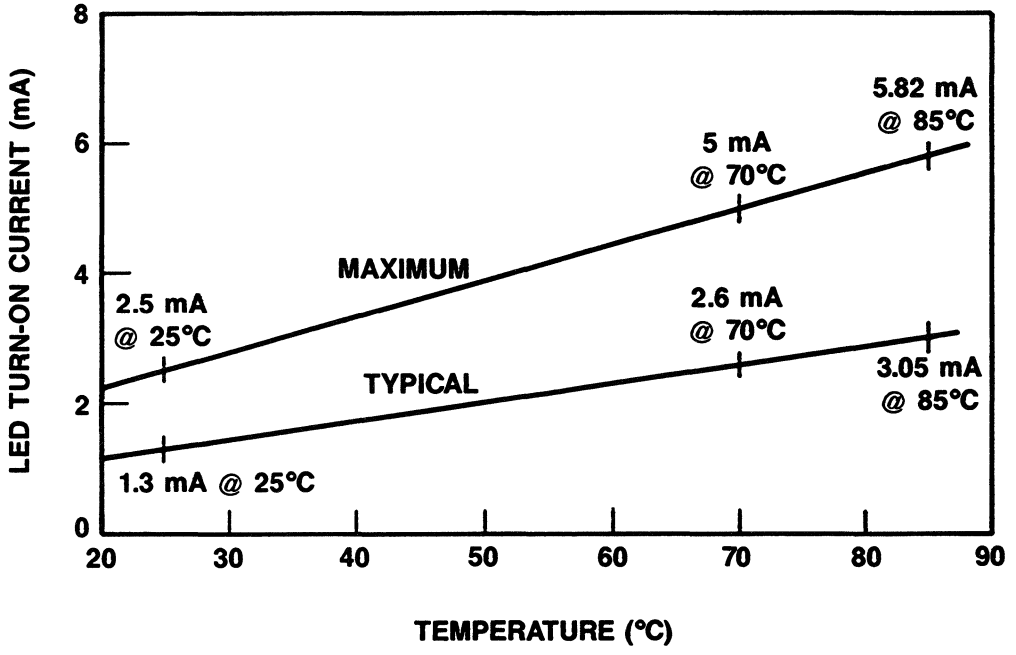


Figure 2. LED Turn-On Current vs. Temperature (°C)

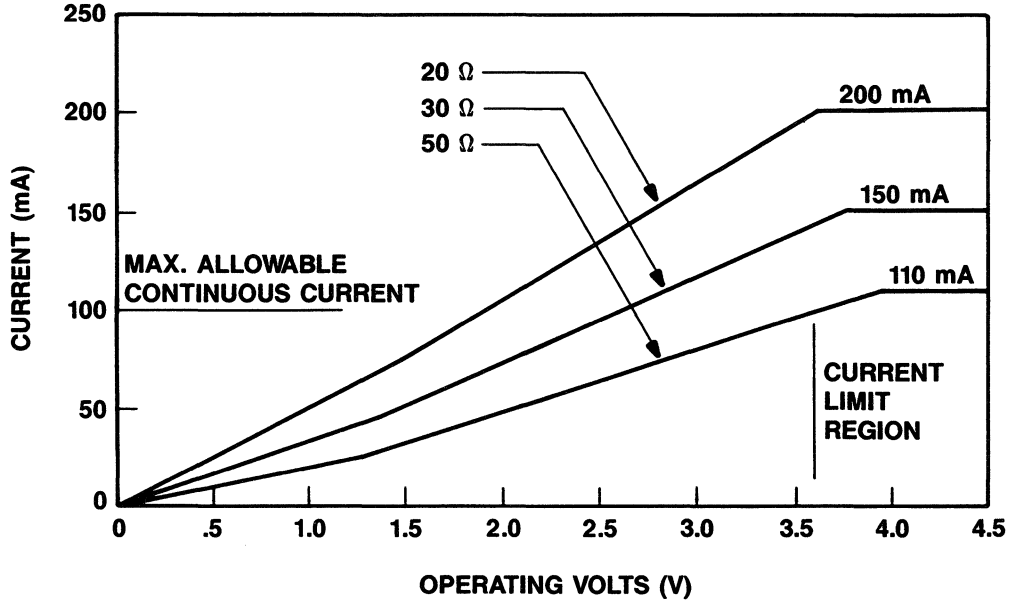


Figure 3. Output I/V Characteristics for Various R_{ON} @ 25°C

Test Circuits
(Continued)

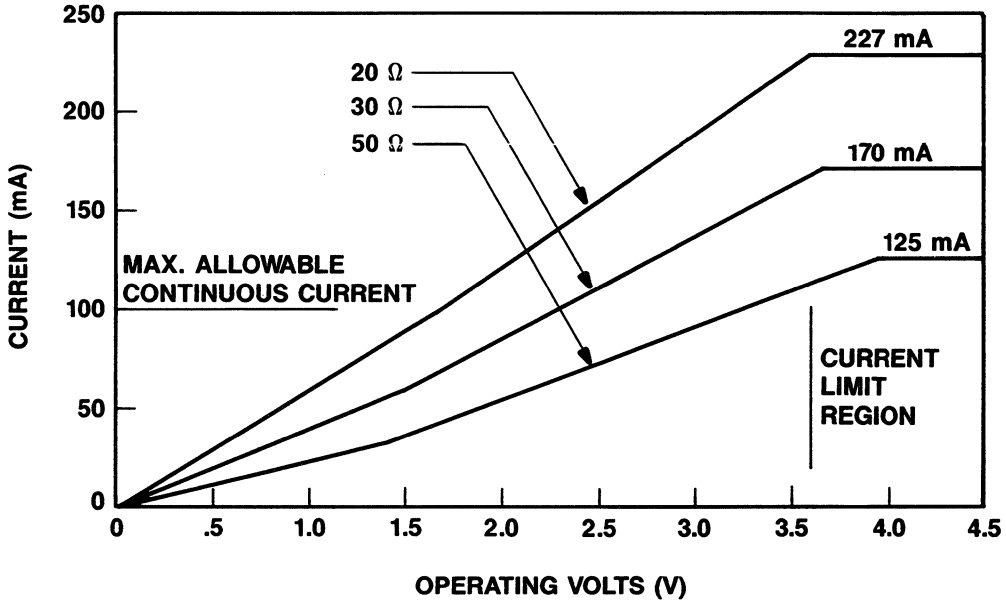


Figure 4. Output I/V Characteristics for Various R_{ON} @ 0°C

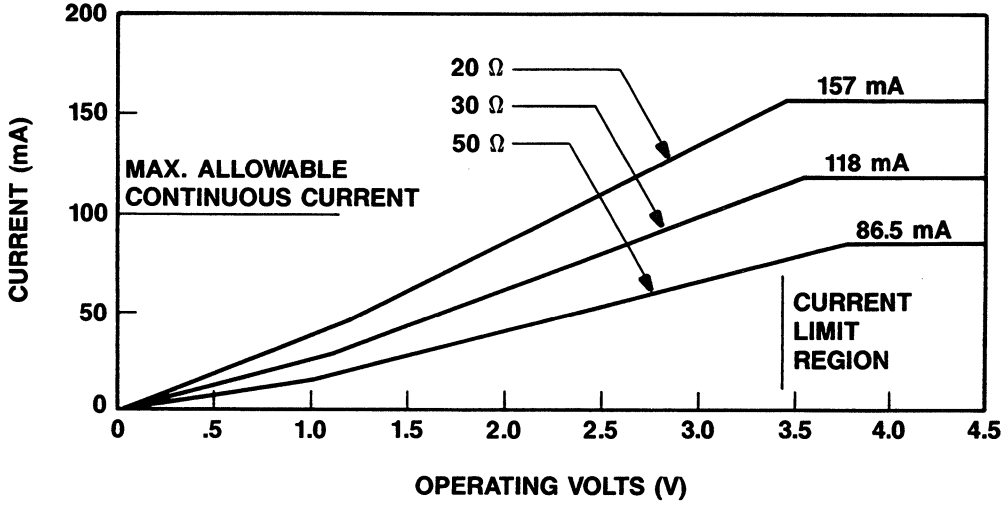


Figure 5. Output I/V Characteristics for Various R_{ON} @ 70°C

Test Circuits
(Continued)

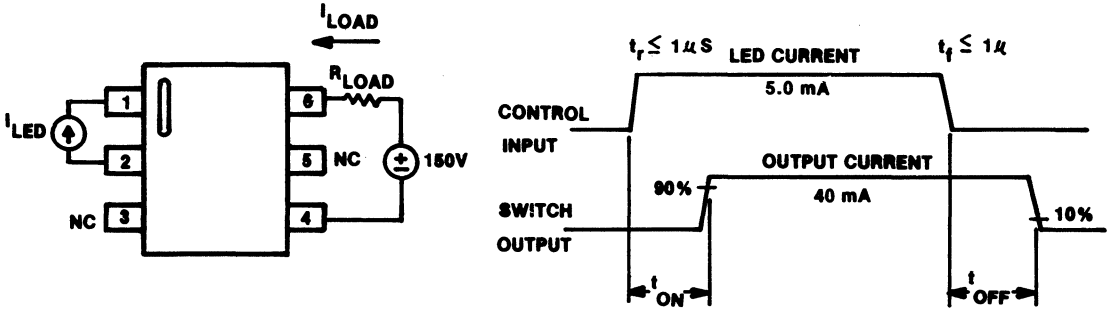
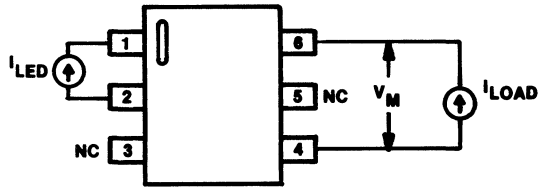
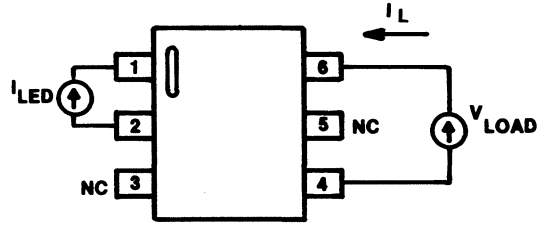


Figure 6. tON/tOFF Test Circuit and Waveform



ILED	ILOAD	Measure	Parameter
5.0 mA	±25 mA	±VM	ON Resistance, RON = $\frac{V_M}{25\ mA}$
5.0 mA	±100 mA	±VM	ON Voltage, VON = VM
0	±50 μA	±VM	Breakdown Voltage, V(BR) = VM

Figure 7. Test Circuit for RON, ON Voltage and Breakdown Voltage



ILED	VLOAD	Measure	Parameter
200 μA	±300 V	IL	Leakage, ILKG = IL
0, 200 μA	±100 V	IL	
5.0 mA	±5.0 V	IL	Limit Current ILIM = IL

Figure 8. Test Circuit for Leakage and Limit Current

Applications

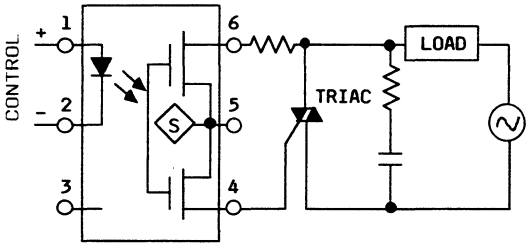


Figure 9. Triac Predriver

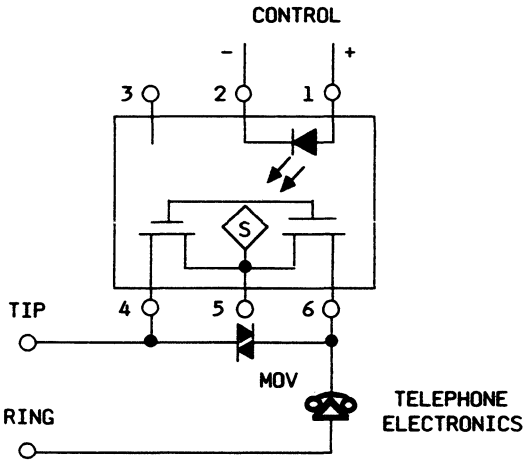
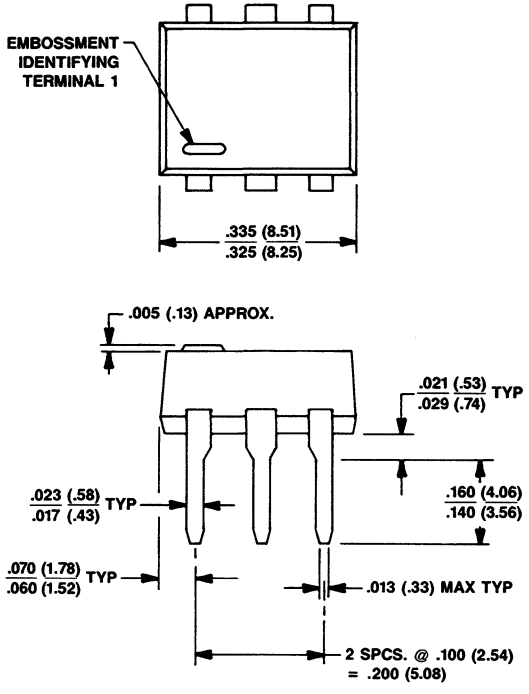


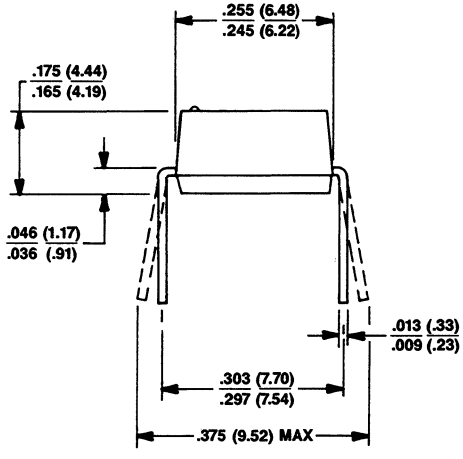
Figure 10. Telephone Switchhook

Outline Drawings

6-Pin Plastic DIP

(Dimensions in Inches)





Ordering Information

Device	Comcode
LH1056AT	104375217
LH1056CT	104437561

PRELIMINARY

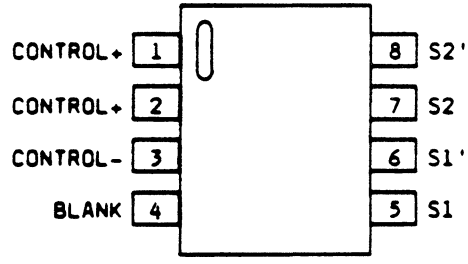
Descripton

The LH1061AB Multi-Purpose Solid-State Relay (MSR) is a low-cost, bi-directional, double-pole, single-throw (DPST) switch which can replace mechanical relays in many applications. Its output is rated at 200 volts per pole and can handle loads up to 200 mA. The LH1061AB MSR is packaged in an 8-pin plastic DIP. It provides up to 1500 Vrms of input/output isolation. The device will switch both ac and dc loads, but is primarily intended for audio frequency or dc applications. This device consists of a single LED to optically couple the control signal to a dielectrically isolated high-voltage integrated circuit. The typical ON-Resistance is 12 ohms per pole at 50 mA, and is exceptionally linear to 100 mA. Beyond 100 mA, the incremental ON-resistance becomes even less, thereby minimizing internal power dissipation. The LH1061AB MSR also has internal current limiting which clamps the load current to 250 mA to insure that the device survives during power surges.

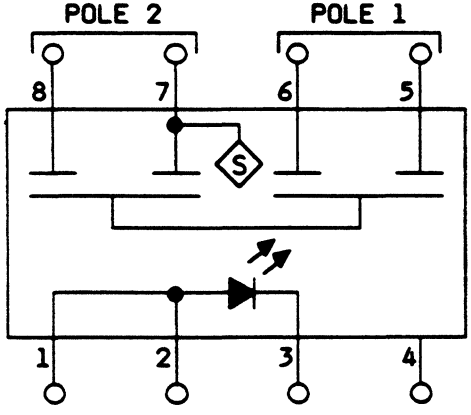
Features

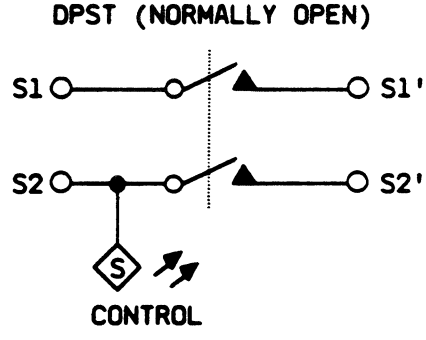
- Low ON-Resistance
- Clean, bounce-free switching
- 1500 V input/output isolation (optically coupled)
- dv/dt typically better than 500 V/μs
- High-surge capability
- Low power consumption
- Noise-free operation
- No electromagnetic interference
- High-voltage monolithic IC fabricated in a dielectric isolation process

Pin Diagram



Functional Diagram





Maximum Ratings

(At 25°C unless otherwise specified)

Rating	Value	Unit
Ambient Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−40 to 100	°C
Pin Temperature (Soldering Time =. 15 s)	300	°C
Input/Output Voltage Isolation	1500	Vrms
LED Input Ratings Continuous Forward Current Reverse Voltage	 20 10	 mA V
Output Operation Operating Voltage DC or Peak Load Current (Each pole, two poles operating simultaneously)	 200 200	 V mA

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions

(Also See Functional and Pin Diagrams)

Pin	Symbol	Name/Function
1 2 3	Control + Control + Control −	These pins are the positive and negative inputs respectively to the input control LED. An appropriate amount of current through the LED will close the circuit path between S and S'.
5, 6 7, 8	S1, S1' S2, S2'	These pins are the outputs. The pin designated as S represents one side of a relay pole. The pin designated as S' (S Prime) is the complementary side of a relay pole. S2 is electrically connected to the device substrate. To achieve maximum dv/dt sensitivity, connect S2 to the lowest circuit potential.
4	Blank	This pin may be used as a tie-point for external components. Voltage on this pin should not exceed 300 volts.

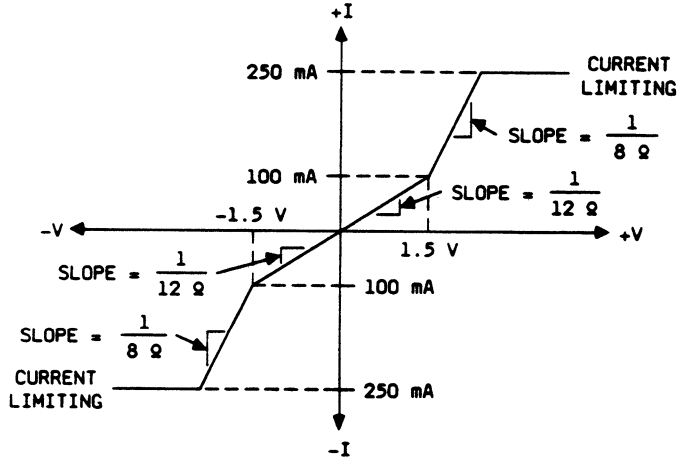


Figure 1. LH1061AB Typical ON Characteristics

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic and Test Condition		Min.	Typ.	Max.	Unit
LED Forward Current for Turn-On*	I_{LOAD} = 200 mA, 25°C	—	1.5	2.5	mA
	I_{LOAD} = 160 mA, 70°C	—	2.5	5.0	mA
LED ON Voltage @ 10 mA		1.15	1.30	1.45	V
ON Resistance @ 50 mA (Figure 2)		8	12	15	Ω
ON Voltage @ 200 mA (Figure 2)		—	2.0	2.5	V
Output Off-State Leakage Current (Figure 3)	100 V, I_{LED} = 0 μA	—	1.0	—	nA
	100 V, I_{LED} = 200 μA	—	0.1	2.0	μA
Breakdown Voltage @ 50 μA (Figure 2)		200	230	—	V
Turn-On Time	I_{LED} = 5 mA, I_{LOAD} = 40 mA/Pole	—	2.0	—	ms
Turn-Off Time		—	1.0	—	
Feedthrough Capacitance, Pin 4 to 6 (4 V p-p, 1 kHz)		—	35	—	pF
Pole to Pole Capacitance (4 V p-p, 1 kHz)		—	20	—	pF

* Supply a minimum of 6 mA LED current to insure proper operation over the full operating temperature range.

Test Circuits

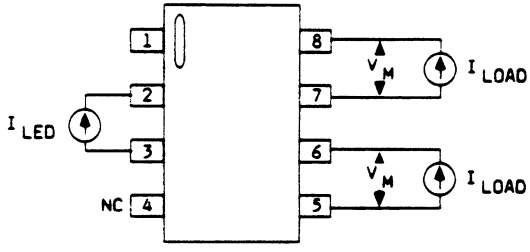


Figure 2. Test Circuit for R_{ON}, ON Voltage and Breakdown Voltage

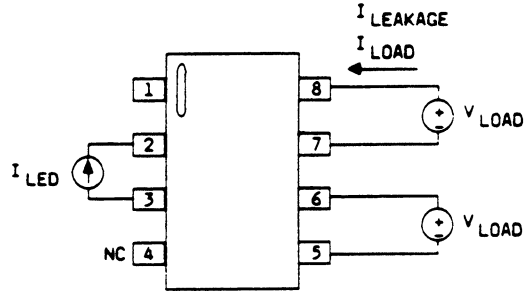


Figure 3. Test Circuit for Leakage and Limit Current

Test Circuits
(Continued)

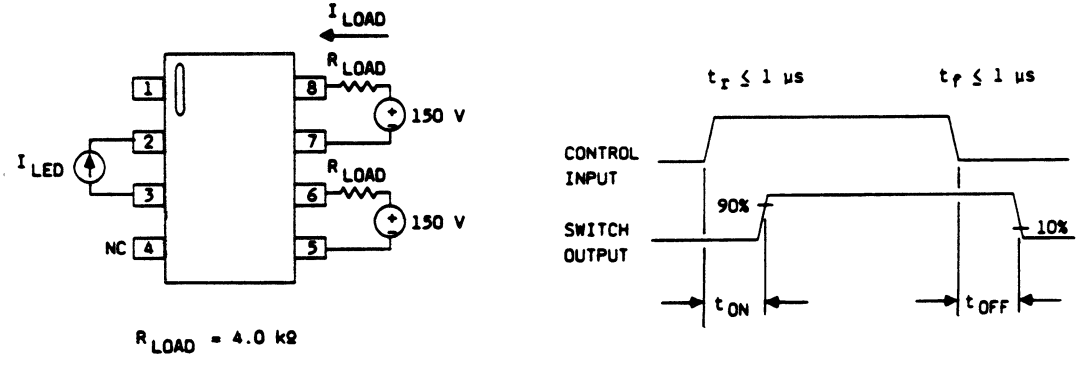


Figure 4. t_{ON}/t_{OFF} Test Circuit and Waveform

Applications

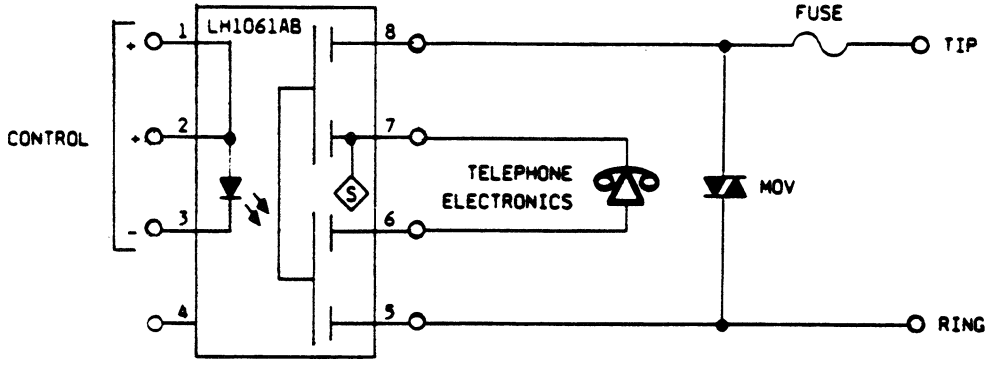
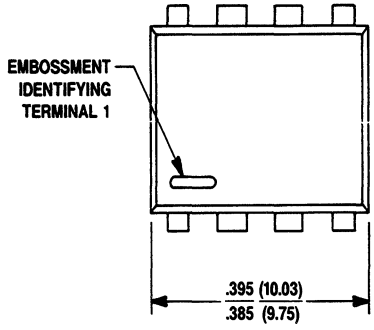


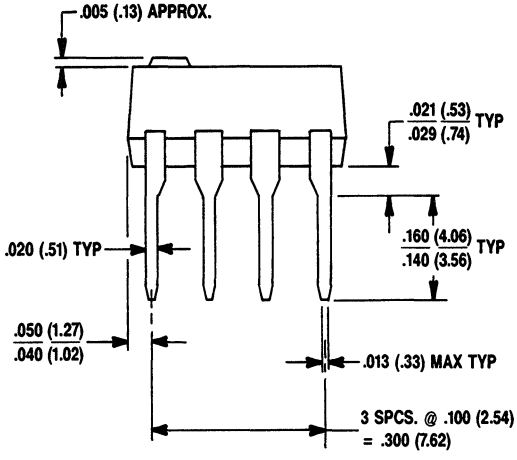
Figure 5. Balanced Switchhook Application

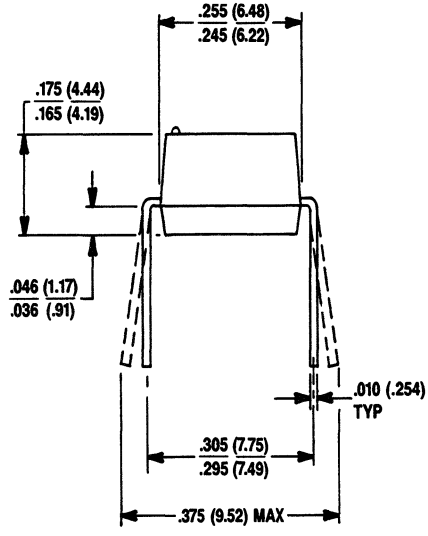
Outline Drawings

8-Pin Plastic DIP

(Dimensions in Inches)







Ordering Information

Device	Comcode
LH1061AB	104384482

Description

The LH1085AT Multipurpose Solid-State Relay (MSR) is a low-cost, bidirectional, SPST switch which can replace mechanical relays in many applications. The output is rated for 350 volts and is similar to the LH1056-Type MSR except that the typical value of the internal current limiting has been increased from 150 to 300 mA. The LH1085AT MSR provides 1500 Vrms of input-to-output isolation and is available in a 6-pin plastic DIP. It can switch both ac and dc loads but is primarily intended for audio frequency applications.

This device uses a GaAlAs LED to optically couple the control signal to a dielectrically isolated high-voltage integrated circuit. The typical ON-Resistance is 30 ohms at 25 mA and is extremely linear up to 50 mA. Beyond 50 mA the incremental resistance becomes even less, thereby minimizing internal power dissipation. The LH1085AT MSR is rated for dc load (operating) currents up to 150 mA and peak currents up to 225 mA. Internal current limiting protects the device in many applications; however the LH1056-Type MSR is recommended for applications where operating currents are below 100 mA.

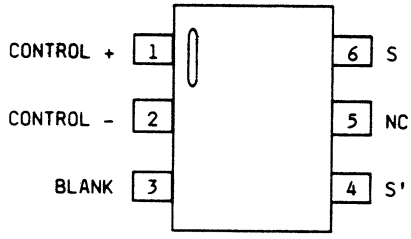
Features

- Low ON-Resistance
- Clean, bounce-free switching
- 1500 Vrms input/output isolation (optically coupled)
- dv/dt typically better than 500 V/μs
- High-surge capability
- Low power consumption
- Noise-free operation
- No electromagnetic interference
- High-voltage monolithic IC fabricated in a dielectric isolation process

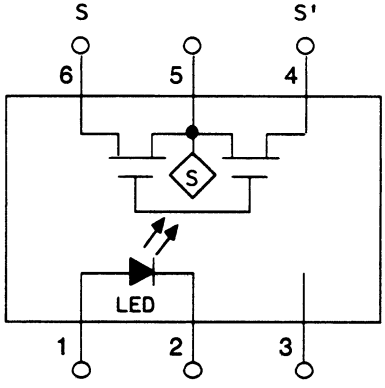
Applications

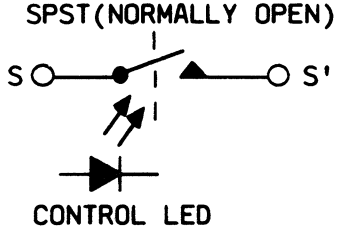
- Telephone switchhook
- High-voltage testers
- Industrial controls
- Triac driver
- Isolation switching

Pin Diagram



Functional Diagram





Maximum Ratings

(At 25°C unless otherwise specified)

Rating	Value	Unit
Ambient Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−40 to 100	°C
Pin Soldering Temperature (t = 15 sec max.)	300	°C
Input/Output Voltage Isolation	1500	Vrms
LED Input Ratings		
Continuous Forward Current	20	mA
Reverse Voltage	10	V
Output Operation		
Operating Voltage	350	V
Peak Load Current (t ≤ 10 milliseconds)	225	mA
DC or RMS Load Current	150	mA

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions

(Also See Functional and Pin Diagrams)

Pin	Name	Description
1 2	Control + Control −	These pins are the positive and negative inputs to the input control LED. An appropriate amount of current through the LED will close the circuit path between S and S'.
6 4	S S′	These pins are the outputs. The pin designated as S represents one side of a relay pole. The pin designated as S' (S Prime) is the complementary side of a relay pole. This relay pole is normally open unless sufficient control current is flowing.
3	Blank	This pin may be used as a tie-point for external components. Voltage on this pin should not exceed 300 volts.
5	NC	This pin is connected to internal circuitry. It should **not** be used as a tie-point for external circuitry.

Characteristics

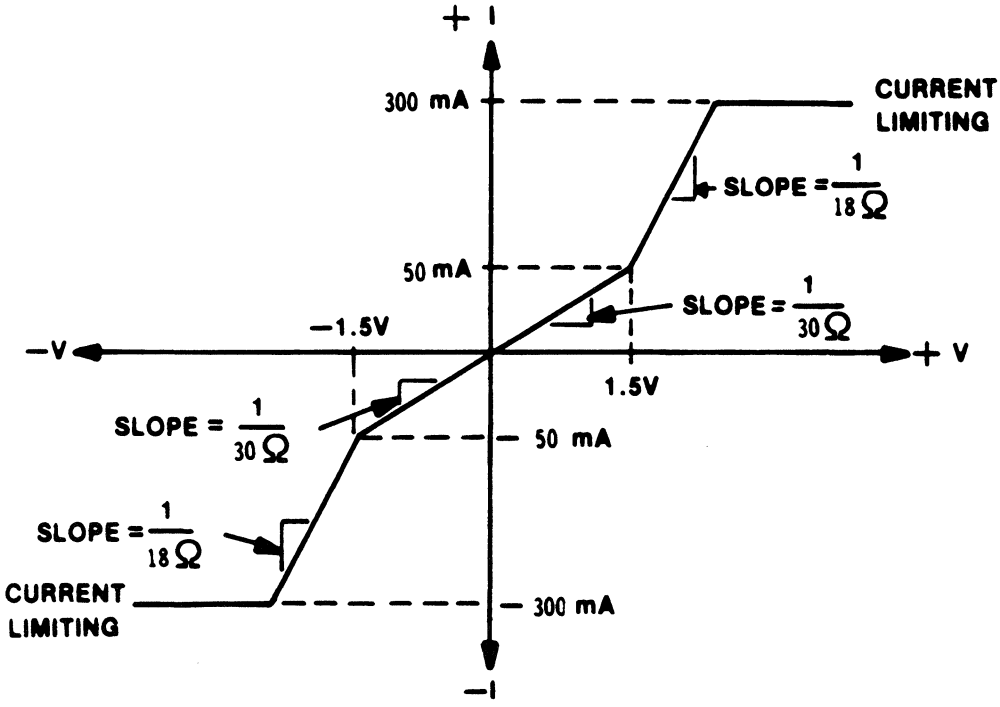


Figure 1. Typical ON Characteristics

Electrical Characteristics

(T_A = 25°C, unless otherwise specified)

Characteristics		Min	Typ	Max	Unit
LED Forward Current for Turn-On *	I_{LOAD} = 150 mA, 25°C	—	1.5	2.5	mA
	I_{LOAD} = 120 mA, 70°C	—	2.5	5.0	
LED ON Voltage @ 10 mA		1.15	1.30	1.45	V
ON Resistance @ 25 mA		20	30	50	Ω
Breakdown Voltage @ 50 μA		350	380	—	V
Output Off-State Leakage Current	100 V, I_{LED} = 0 mA	—	1.0	—	nA
	100 V, I_{LED} = 200 mA	—	0.1	2.0	μA
	300 V, I_{LED} = 200 mA	—	0.1	5.0	μA
Turn-On Time	See Figure 2	—	1.0	—	ms
Turn-Off Time		—	0.5	—	
Feedthrough Capacitance, Pin 4 to 6 (4 V p-p, 1 kHz)		—	30	—	pF

* Supply a minimum of 6 mA LED current to insure proper operation over the fully operating temperature range.

Test Circuits

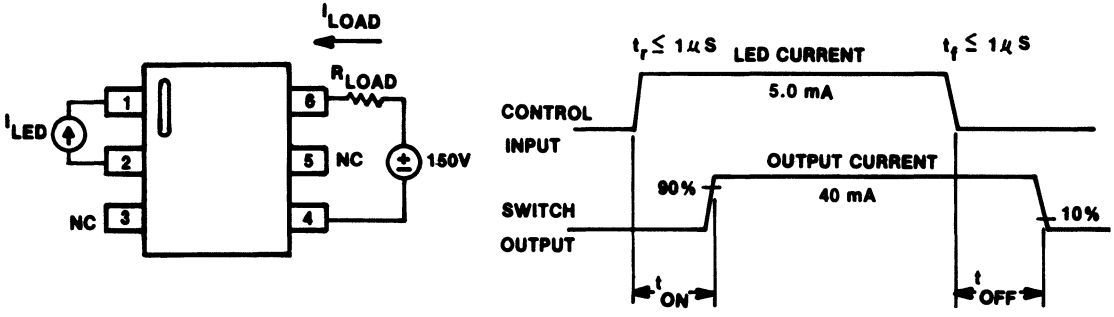
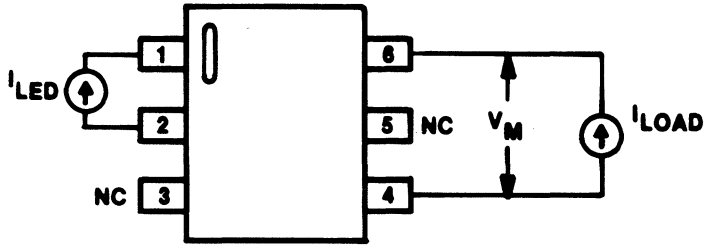
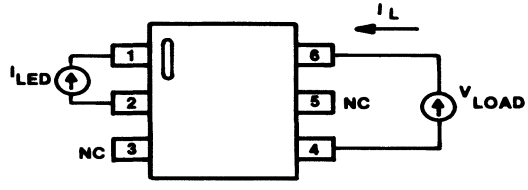


Figure 2. t_{ON}/t_{OFF} Test Circuit and Waveform



I_{LED}	I_{LOAD}	Measure	Parameter
5.0 mA	±25 mA	±V_M	ON Resistance, $R_{ON} = \frac{V_M}{25\ mA}$
5.0 mA	±100 mA	±V_M	ON Voltage, $V_{ON} = V_M$
0	±50 μA	±V_M	Breakdown Voltage, $V_{(BR)} = V_M$

Figure 3. Test Circuit for R_{ON}, ON Voltage and Breakdown Voltage



I_{LED}	V_{LOAD}	Measure	Parameter
200 μA	±300 V	I_L	Leakage, $I_{LKG} = I_L$
0, 200 μA	±100 V	I_L	
5.0 mA	±5.0 V	I_L	Limit Current $I_{LIM} = I_L$

Figure 4. Test Circuit for Leakage and Limit Current

Applications

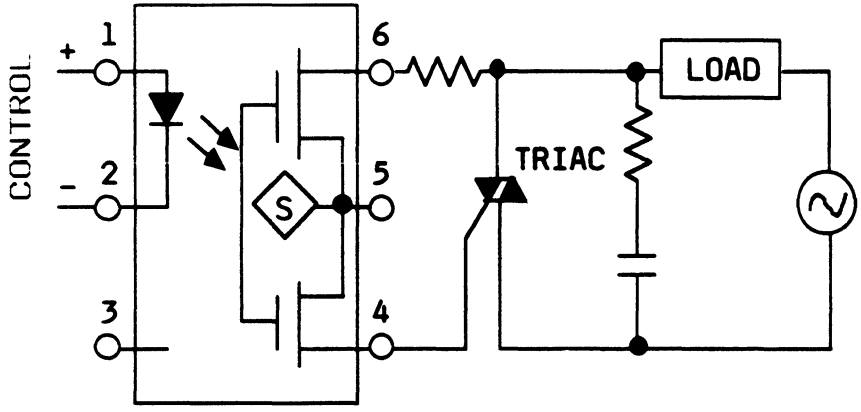


Figure 5. Triac Predriver

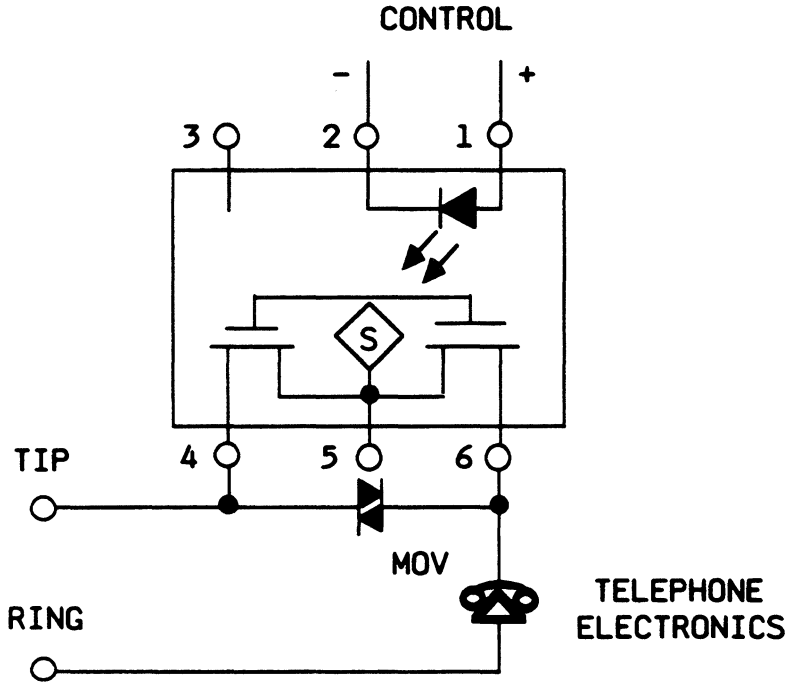
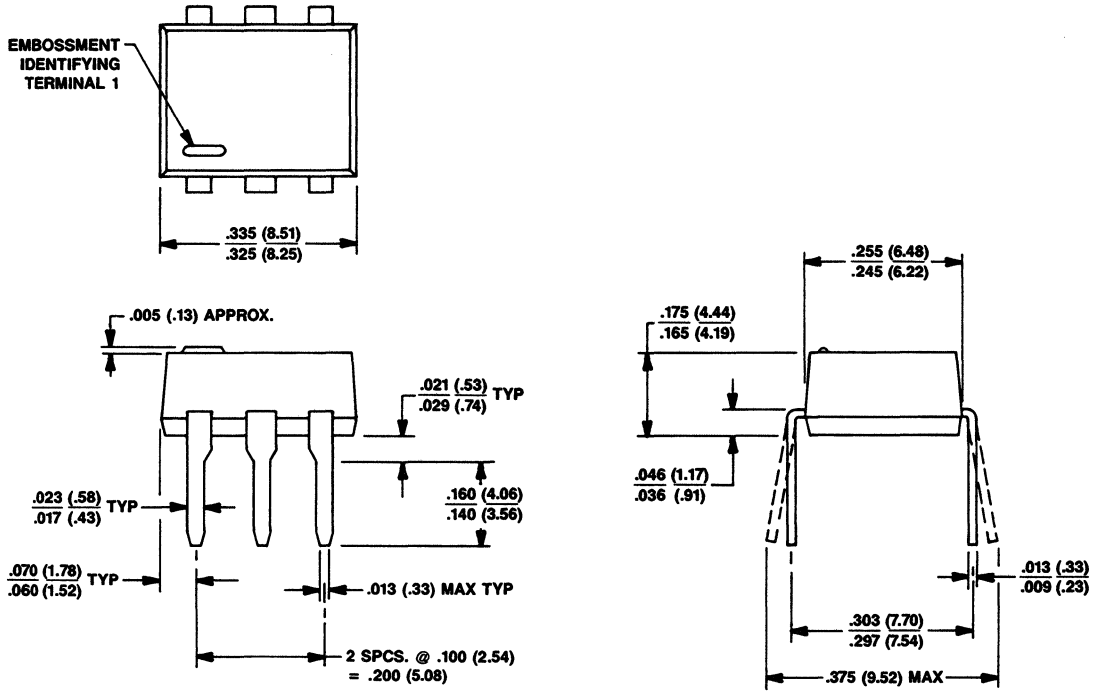


Figure 6. Telephone Switchhook

Outline Drawing

Dimensions in Inches
(mm)



Ordering Information

Device	Comcode
LH1085AT	104395520

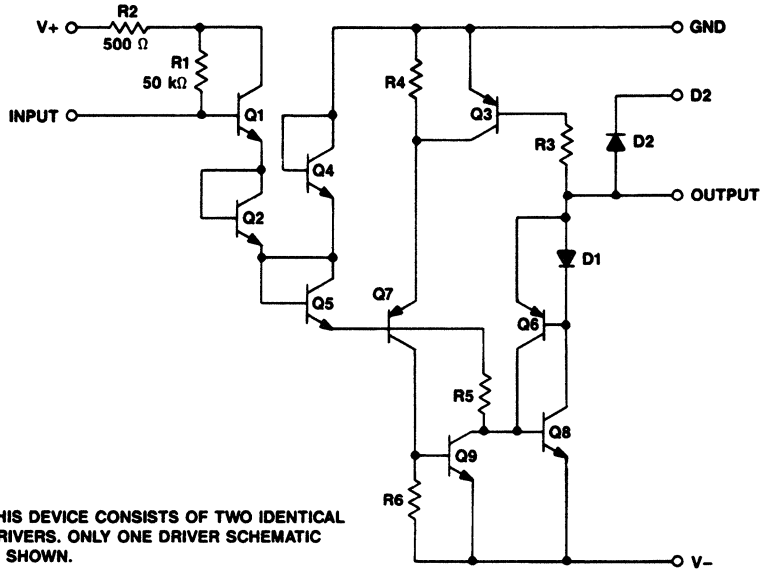
Description

The LS1014AB integrated circuit consists of two independent relay drivers and is intended for use in high-voltage relay applications. Each driver is controlled by TTL logic. A logic 1 on the input activates a relay. The device is available in an 8-pin plastic DIP.

Features

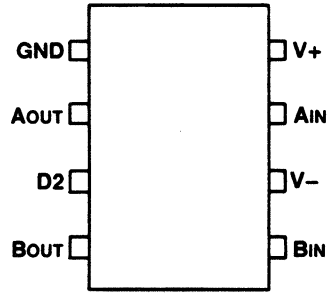
- Flyback protection diode at each output for optional connection
- Each output can handle any load from 2 to 30 mA
- 60-volt operation (nominal −48 volt with +5 volt logic)
- Input logic levels TTL-compatible

Functional Diagram



THIS DEVICE CONSISTS OF TWO IDENTICAL DRIVERS. ONLY ONE DRIVER SCHEMATIC IS SHOWN.

Pin Diagram



Maximum Ratings

(T_A = 25°C unless otherwise specified)

Parameter	Value	Unit
Ambient Operating Temperature Range	0 to 70	°C
Storage Temperature Range	−40 to +125	°C
Pin Temperature (Soldering, 15 sec)	300	°C
Voltage (V+ to V−)	70	V
Voltage (V+ to GND)	6.25	V
Current (Each Driver Output)	−30	mA

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Description Key

Pin	Symbol	Name/Function
1	GND	Circuit common (not necessarily system or physical ground).
2	AOUT	Output for section A of this dual device.
3	D2	Cathode side of an internal surge protection diode (Functional Diagram). See the Applications section for further information.
4	BOUT	Output for section B of this dual device
5	BIN	TTL-compatible input for section B of this dual device.
6	V−	This pin connects to the most negative external power supply.
7	AIN	TTL-compatible input for section A of this dual device.
8	V+	This pin connects to a +5 volt external power supply. The logic portion of this device operates from the +5 volt supply.

Characteristics

Electrical Characteristics

(TA = 25°C unless otherwise specified)

Characteristic/Test Condition		Min	Max	Unit
Power Supply, Current On	(Figure 1)	0.1	2.4	mA
Power Supply, Current Off	(Figure 2)	0.1	1.6	mA
Output Leakage Current	(Figure 3)	—	1.0	μA
Logic Supply, Current On	(Figure 4)	100	1000	μA
Logic Supply, Current Off	(Figure 5)	10	500	μA
Logic Input, Current On	(Figure 6)	−4.0	−75	μA
Logic Input, Current Off	(Figure 7)	−5.0	−250	μA
Output Voltage, High	(Figure 8)	0.6	1.6	V
Output Voltage, Low	(Figure 9)	—	10	mV
Input Switching Voltage, On	—	1.8	—	V
Input Switching Voltage, Off	—	—	0.8	V

Test Circuits

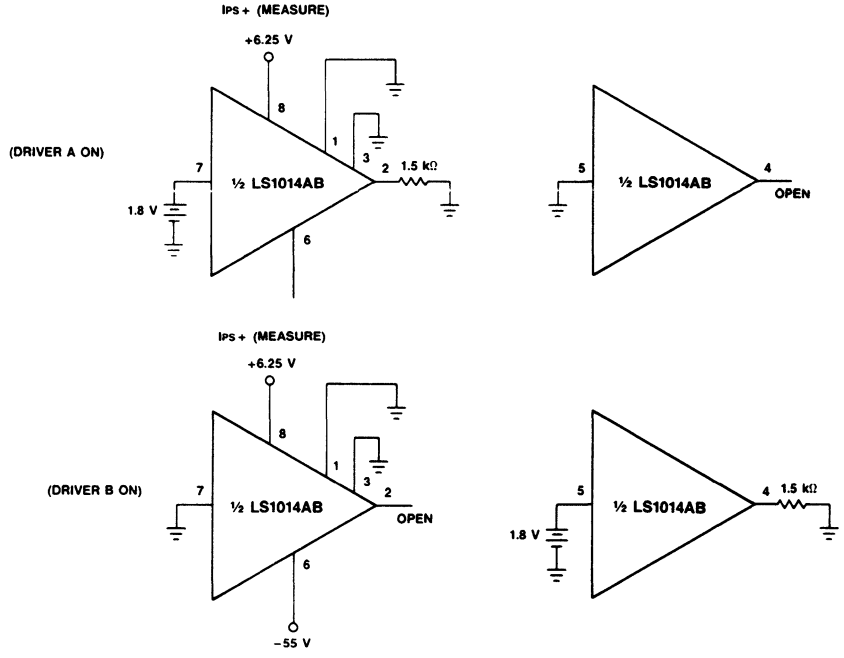


Figure 1. Power Supply, Current On.

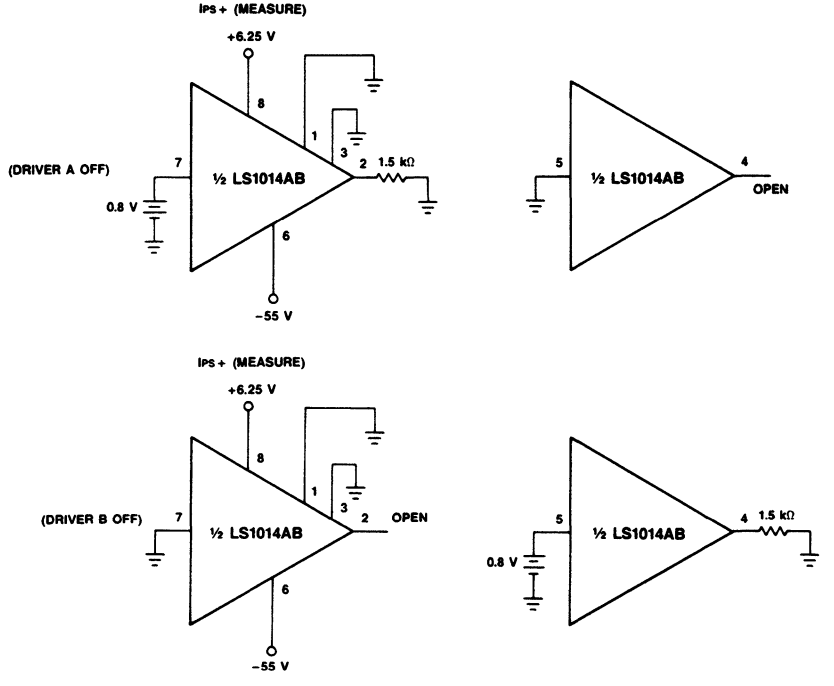


Figure 2. Power Supply, Current Off

Test Circuits
(Continued)

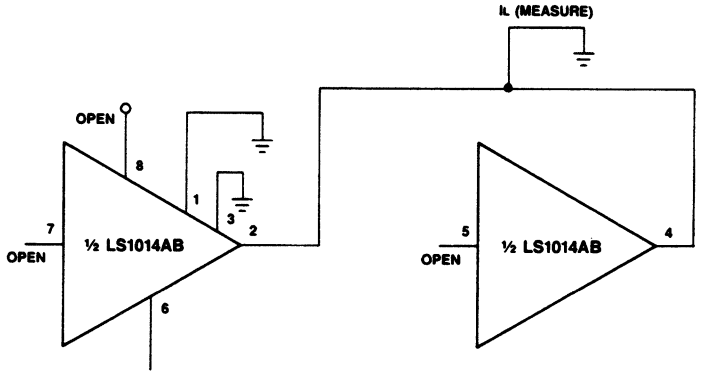


Figure 3. Output Leakage Current

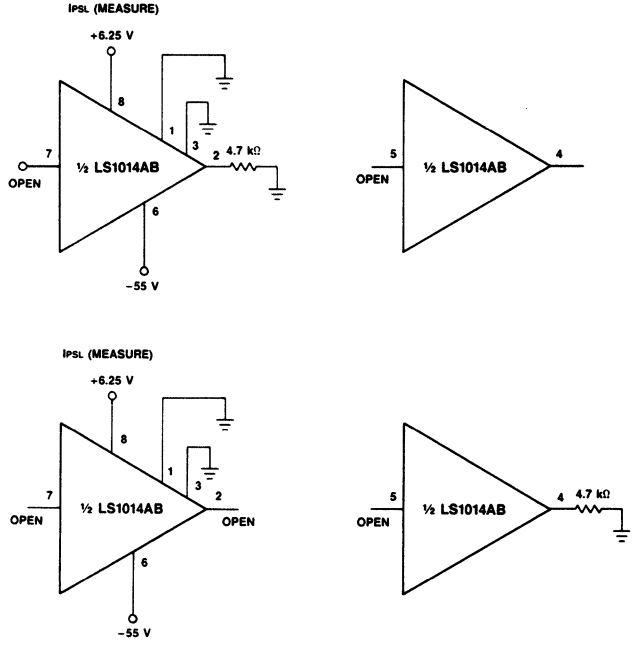


Figure 4. Logic Supply, Current On

Test Circuits
(Continued)

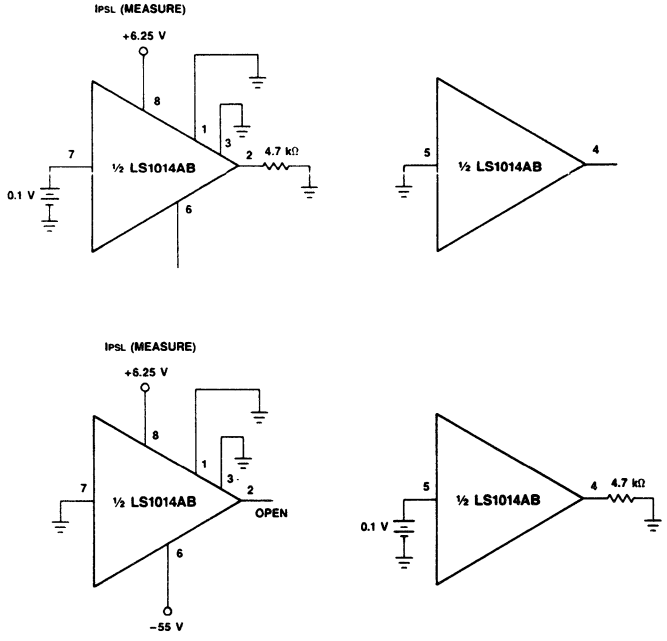


Figure 5. Logic Supply, Current Off

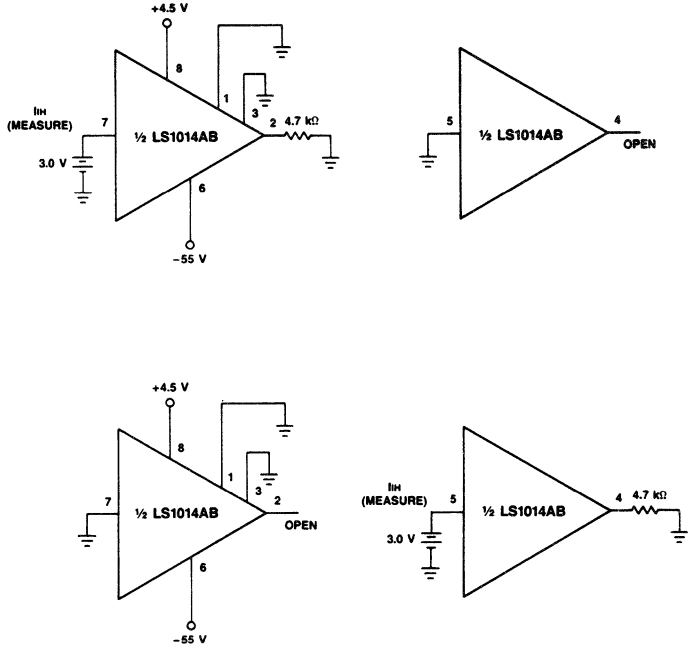


Figure 6. Logic Input Current, On

Test Circuits
(Continued)

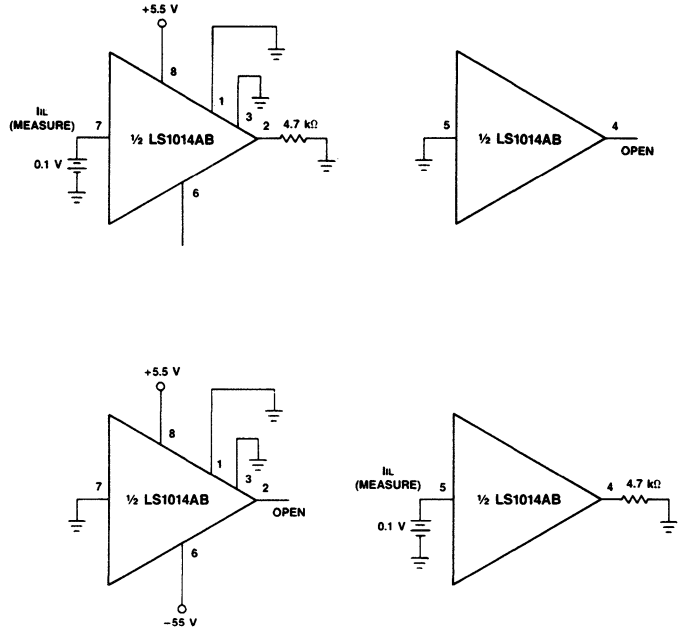


Figure 7. Logic Input Current, Off

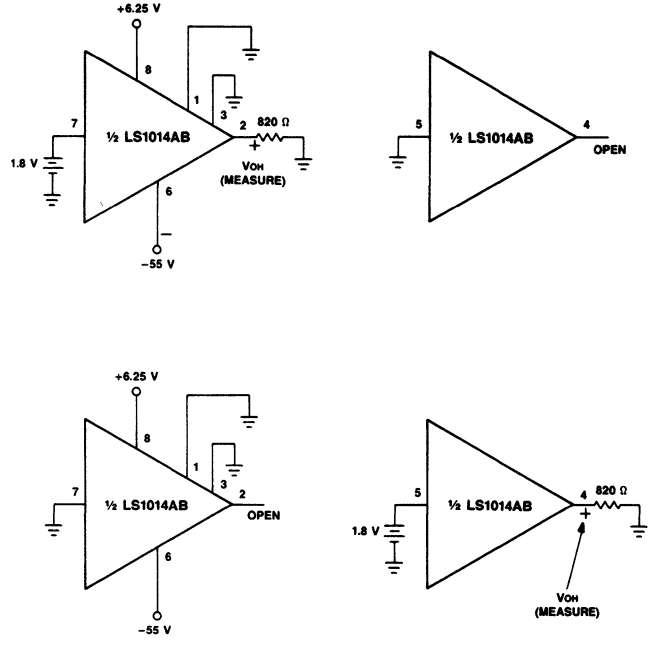


Figure 8. Output Voltage, High

Test Circuits
(Continued)

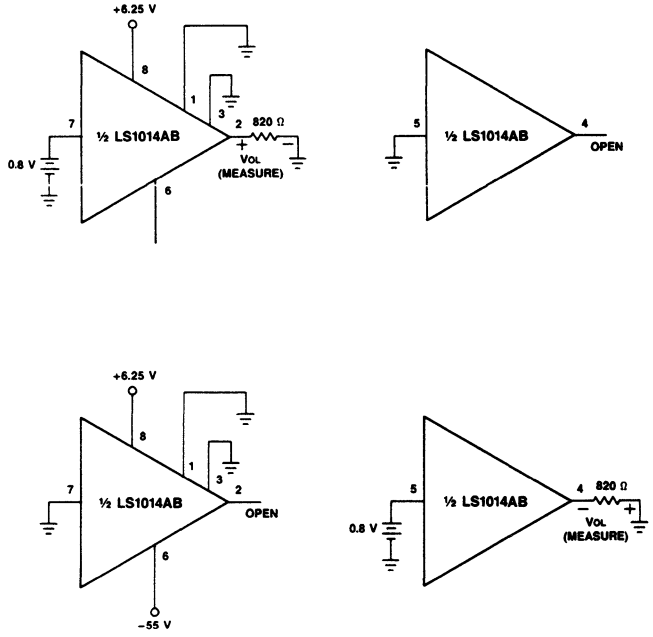


Figure 9. Output Voltage, Low

Characteristic Curves

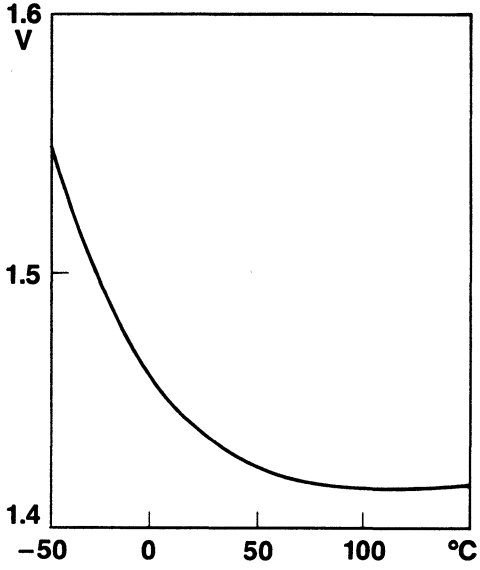


Figure 10. Output Voltage vs. Temperature

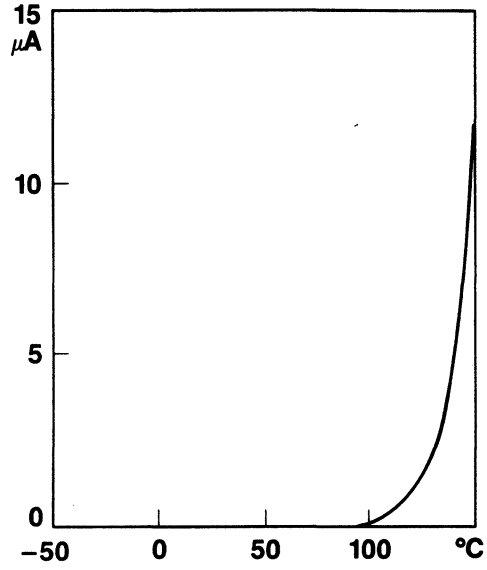


Figure 11. Output Leakage Current vs. Temperature

Characteristic Curves (Continued)

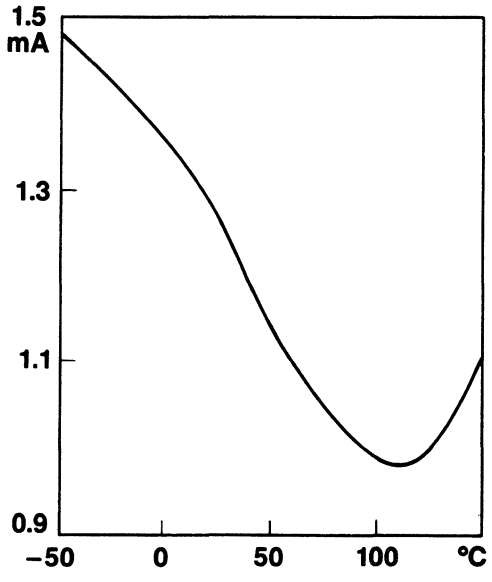


Figure 12. Supply Current vs. Temperature

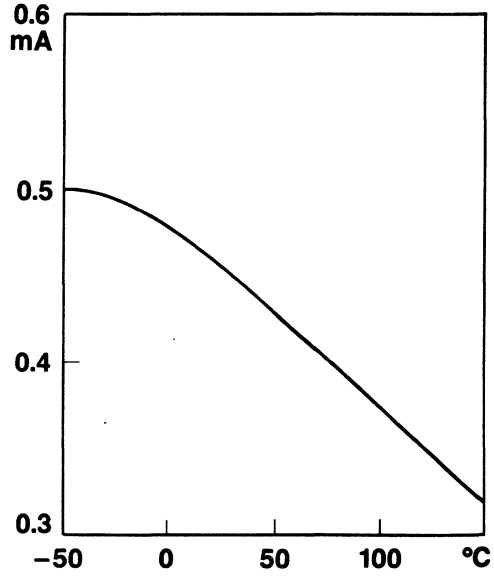
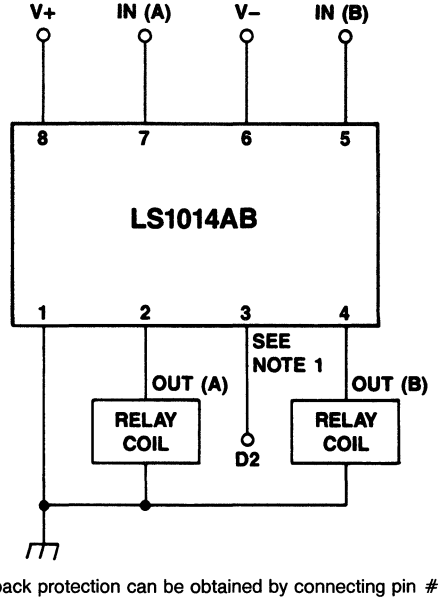


Figure 13. Logic Supply Current vs. Temperature

Applications

Figure 14 illustrates the relay-to-ground method of driving a relay using the LS1014AB device. A surge protection diode can be placed across the relay coils by connecting pin 3 to ground. (See Functional Diagram for the internal surge protection diode connections.)

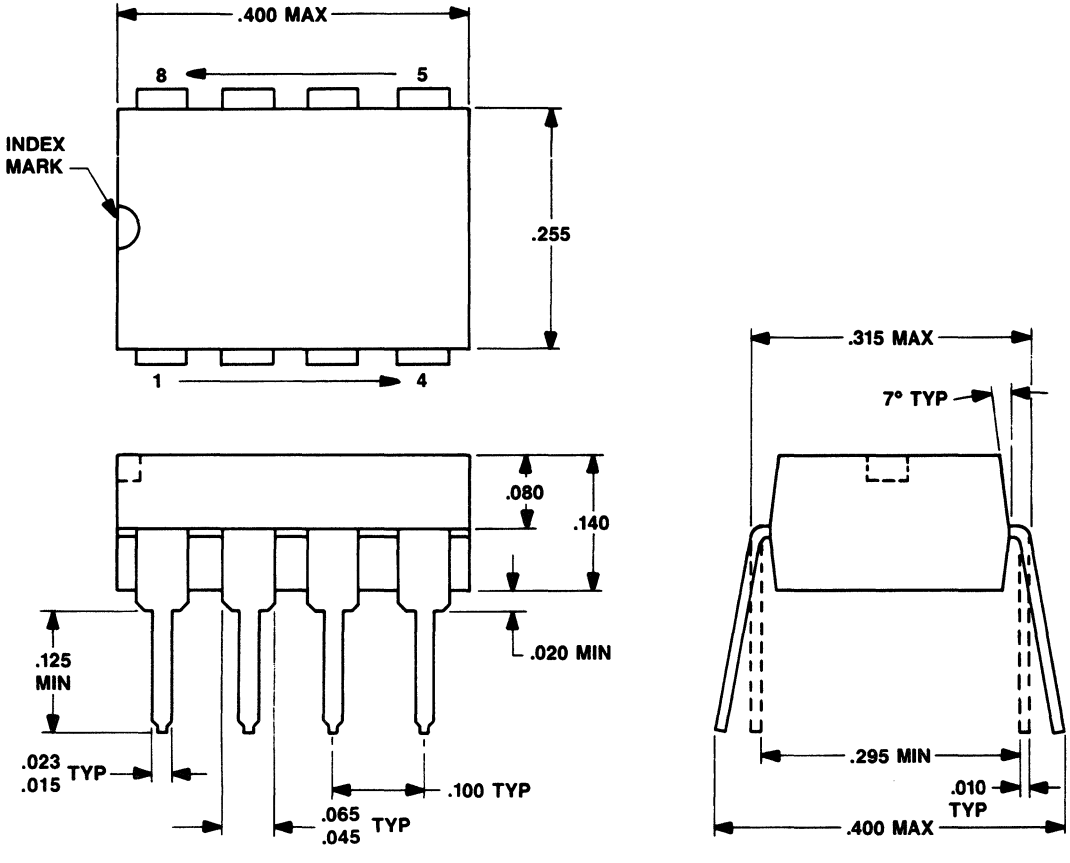


Note 1: Flyback protection can be obtained by connecting pin #3 to ground.

Figure 14. LS1014AB Relay-to-Ground Application Diagram

Outline Drawing

(Dimensions in Inches)



Note: Pin numbers are shown for reference only

Ordering Information

Device	Comcode
LS1014AB	104208855

QUAD NEGATIVE-VOLTAGE RELAY DRIVER

LS1098AAF

PRELIMINARY

Description

THE LS1098AAF integrated circuit consists of four independent 60-volt relay drivers designed to operate over wide ranges of supply voltage, common-mode voltage, and ambient temperature, with 50 mA source capability. These drivers are intended for switching the ground side of loads which are directly connected to a negative supply, such as in telephone relay systems.

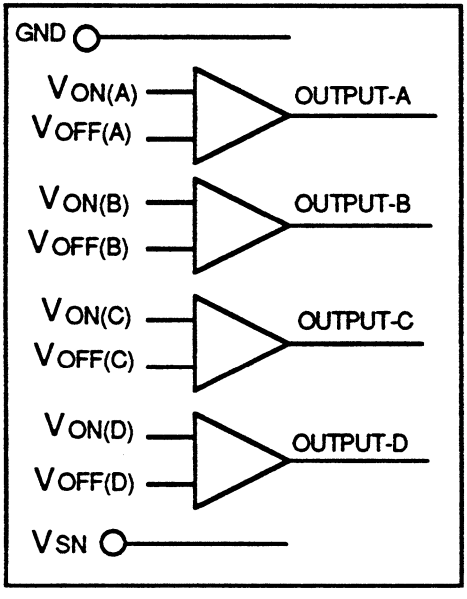
Noise and IR drop between logic ground and negative supply ground are problems which must always be considered in telephone relay systems. Therefore, these relay drivers are designed to operate with a high common-mode range.

These drivers are compatible with TTL, LS, and CMOS logic, since the differential input current requirements are low. Differential inputs permit either inverting or noninverting operation. The driver outputs incorporate transient suppression clamp networks which eliminate the need for external suppression circuitry when used in applications for switching inductive loads. A fail-safe feature is incorporated to insure that, if the VON input or both inputs (VON and VOFF) are open, the driver will be off. The LS1098AAF Quad Negative-Voltage Relay driver is available in a 14-pin SONB package.

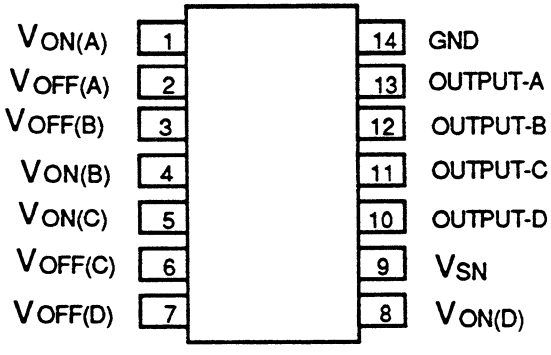
Features

- 50 mA source capability (each driver)
- Low propagation delays ($\leq 10\ \mu s$)
- TTL, LS or CMOS compatible Inputs
- Fail-safe disconnect protection
- High input common-mode voltage range (± 20 V)
- Negative supply operating voltage (-10 V to -60 V)
- Built-in output clamp diodes

Functional Diagram



Pin Diagram



(Surface Mount)

Maximum Ratings (T_A = 25°C unless otherwise specified)	
Storage Temperature Range	−40 to +125°C
Pin Soldering Temperature (t = 15 sec max.)	300°C
Supply Voltage V_{SN} tp GND, and Any Pin)	−70 V
Positive Input Voltage (Input to GND)	20 V
Differential Input (V_{ON} to V_{OFF})	±20 V
Output Current (Each Driver)	50mA

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Description

Pin	Symbol	Name/Function
1 4 5 8	$V_{ON(A)}$ $V_{ON(B)}$ $V_{ON(C)}$ $V_{ON(D)}$	Driver **logic ON** inputs for sections A, B, C and D respectively. These inputs are TTL, LS and CMOS compatible. Figure 1 shows a simplified diagram of the input circuit.
2 3 6 7	$V_{OFF(A)}$ $V_{OFF(B)}$ $V_{OFF(C)}$ $V_{OFF(D)}$	Driver **logic OFF** inputs for sections A, B, C and D respectively. These inputs are TTL, LS and CMOS compatible. Figure 1 shows a simplified diagram of the input circuit.
9	V_{SN}	Connection for "most negative" external power supply.
10 11 12 13	OUTPUT-D OUTPUT-C OUTPUT-B OUTPUT-A	Driver outputs for sections D,C, B and A respectively. Figure 2 shows a simplified diagram of the output circuit.
14	GND	Ground or circuit common (not necessarily physical or system ground).

Table 1. Recommended Operating Condition

Pin 14 is connected to system ground. The supply voltage (Pin 9) is negative with respect to Pin 14.

Conditions	Min	Max	Units
V_{SN} Supply Voltage	−10	−60	V
Input Voltage (Input to GND)	−20	20	V
Logic ON voltage (V_{ON} referenced to V_{OFF})	2	20	V
Logic OFF Voltage (V_{ON} referenced to V_{OFF})	−20	0.8	V
Temperature Range	0	85	°C

Simplified Input/Output Diagrams

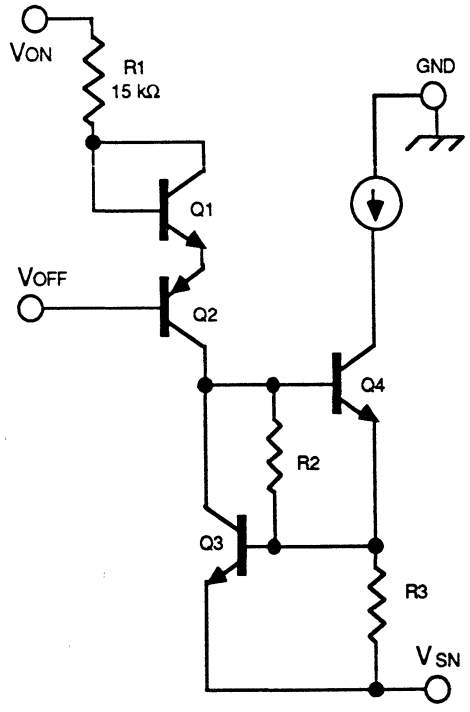


Figure 1. LS1098AAF Simplified Input Diagram

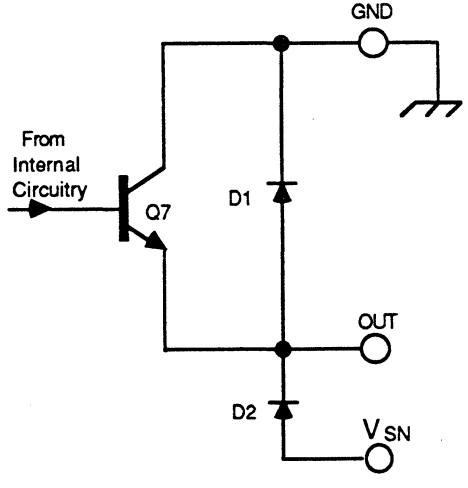


Figure 2. LS1098AAF Simplified Output Diagram

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements. Also see Note 1.

Characteristic	Test Condition	Min	Typ	Max	Unit
Supply Current	Figure 3;				
Drivers ON	V_{ON} = 2.0 V	—	1.4	4.4	mA
Drivers OFF	V_{ON} = 0.8 V	—	0.01	100	μA
Fail-Safe Output Leakage Current	Figure 4	—	0.01	100	μA
Output-Off Leakge Current	Figure 5; V_{ON} = 0.8 V	—	0.01	100	μA
Output-On Voltage	Figure 6; V_{ON} = 2.0 V	0.6	1.5	2.1	V
V_{ON} Input Current	Figure 7;				
	V_{ON} = 0.4 V, V_{OFF} = 0	—	0.01	50	μA
	V_{ON} = 2.0 V, V_{OFF} = 0	—	57	100	μA
	V_{ON} = 7.0 V, V_{OFF} = 0	—	436	1000	μA
	V_{ON} = 22 V, V_{OFF} = 0	—	0.01	100	μA
V_{OFF} Input Current	Figure 8;				
	V_{OFF} = 0 V; V_{ON} = 7 V	—	10.5	100	μA
Forward Voltage,					
Output Diode D1	Figure 9	0.40	0.66	1.20	V
Output Diode D2	Figure 10	0.40	0.57	1.20	V
Reverse Leakage Current,					
Output Diode D1	Figure 11	—	1.80	10	μA
Output Diode D2	Figure 12	—	0.11	10	μA
Propagation Delay, Driver On	—	—	1.0	—	μs
Driver Off	—	—	1.0	—	μs

Note 1: The test circuit and the testing requirements are shown only for Driver number 1 (except supply current). The test circuits (appropriately modified) and testing requirements apply to each individual Driver.

Test Circuits

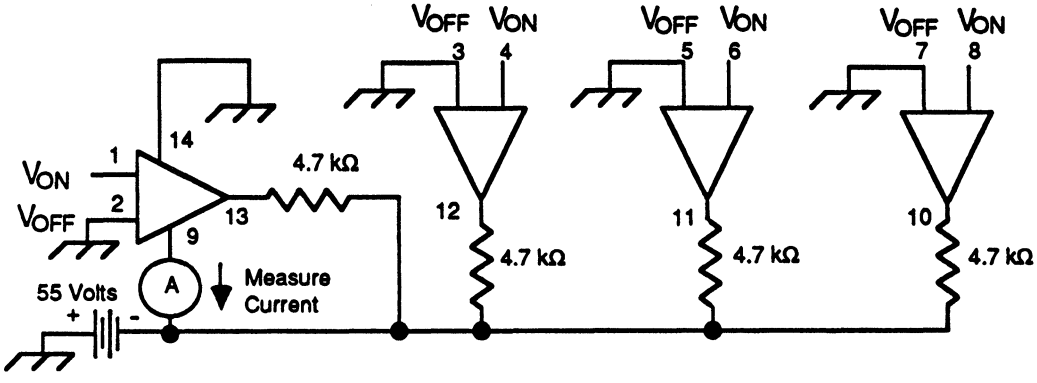


Figure 3. Supply Current Test Circuit

Test Circuits
(Continued)

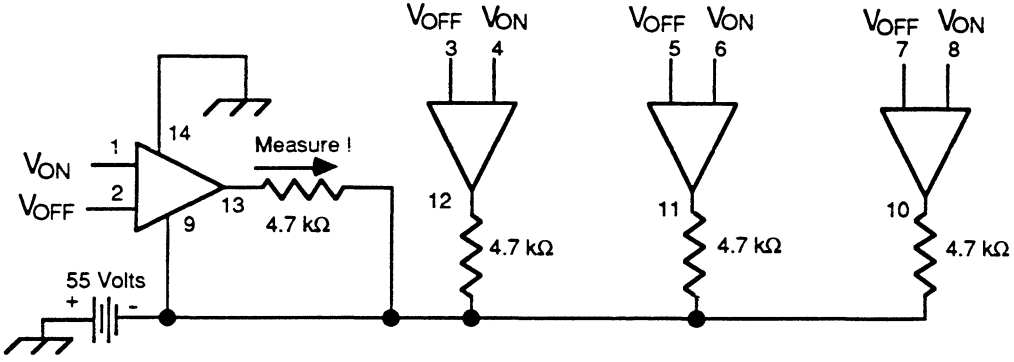


Figure 4. Fail-Safe Output Leakage Current Test Circuit

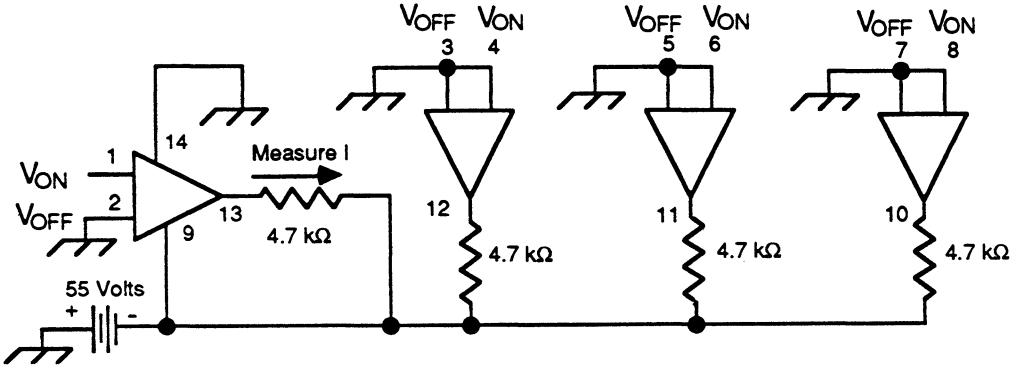


Figure 5. Fail-Safe Output Leakage Current Test Circuit

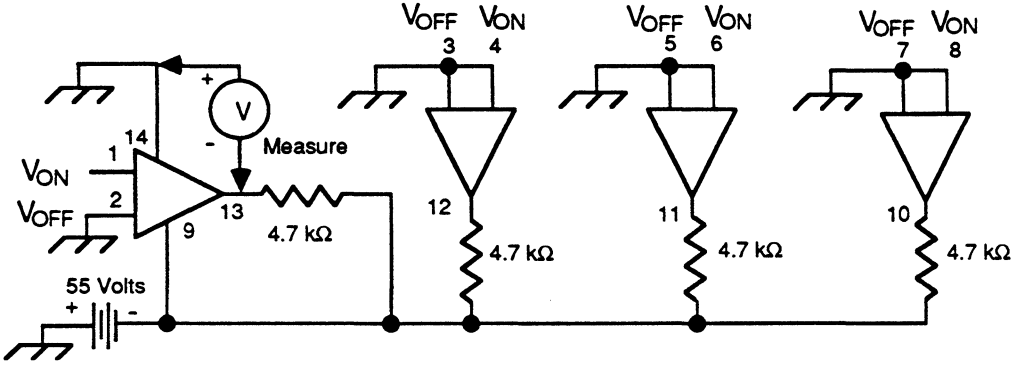


Figure 6. Output-On Voltage Test Circuit

Test Circuits
(Continued)

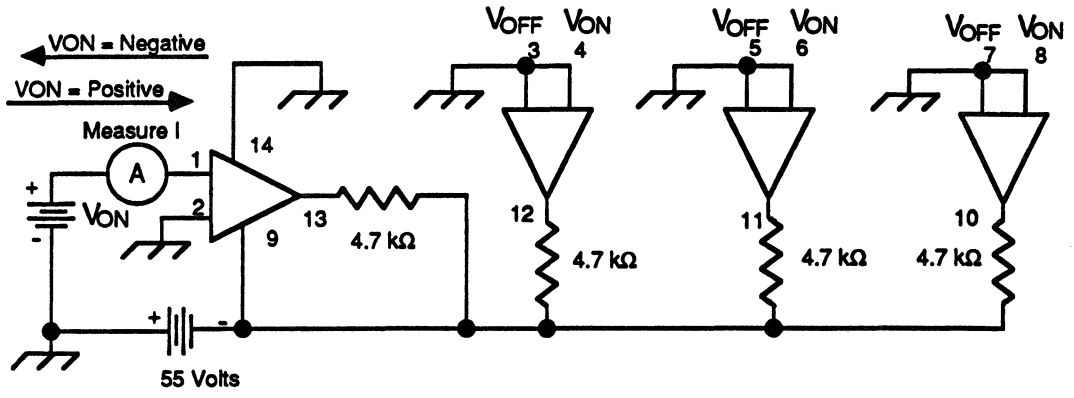


Figure 7. VON Input Current Test Circuit

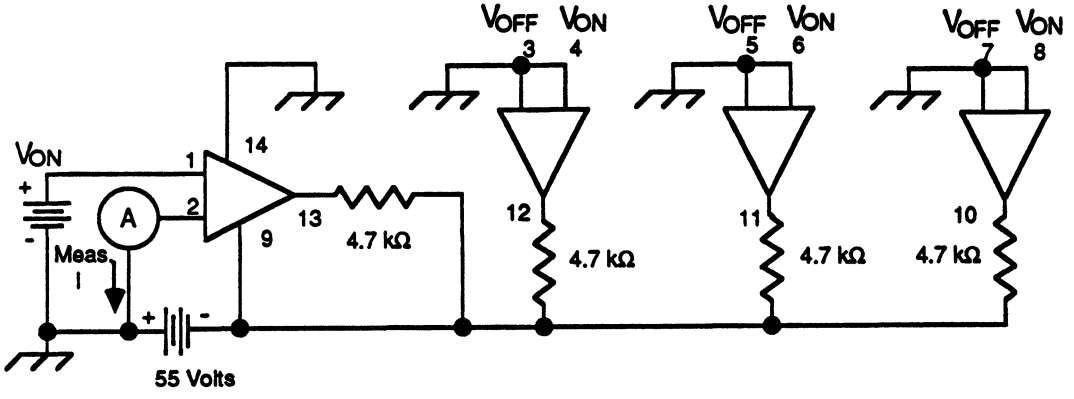


Figure 8. VOFF Input Current Test Circuit

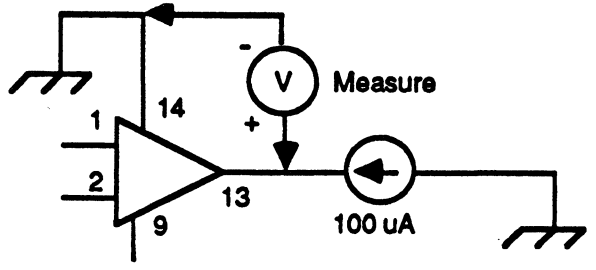


Figure 9. Forward Voltage, Output Diode D1 Test Circuit

Test Circuits
(Continued)

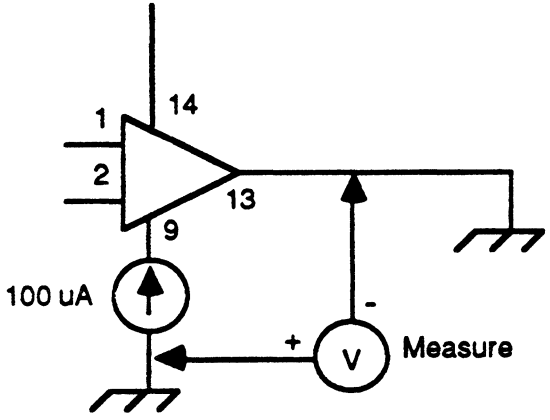


Figure 10. Forward Voltage, Output Diode D2 Test Circuit

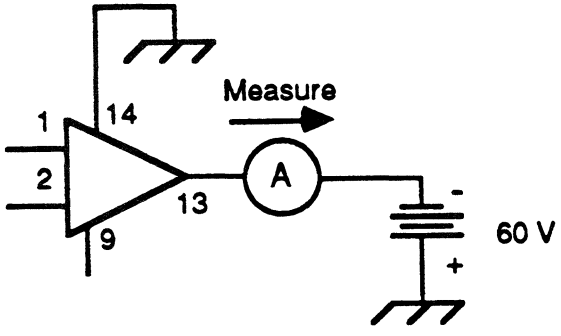


Figure 11. Reverse Leakage Current, Output Diode D1 Test Circuit

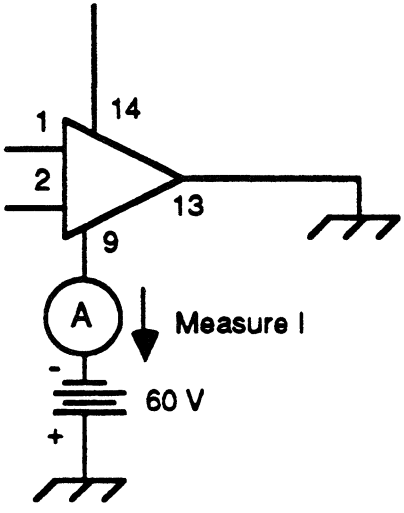


Figure 12. Reverse Leakage Current, Output Diode D2 Test Circuit

Electrical Characteristics

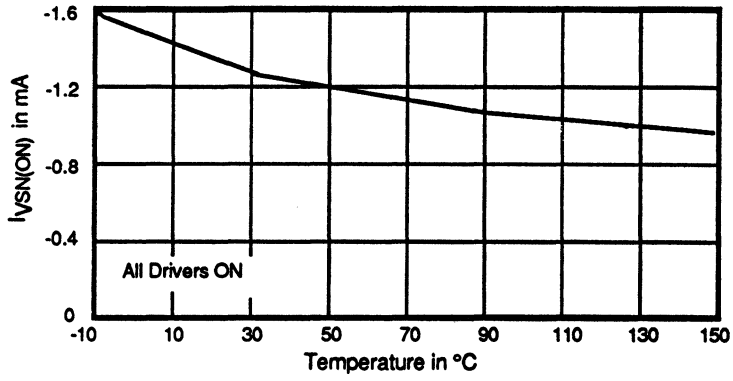


Figure 13. Typical Supply Current ($I_{VSN(ON)}$) vs Temperature

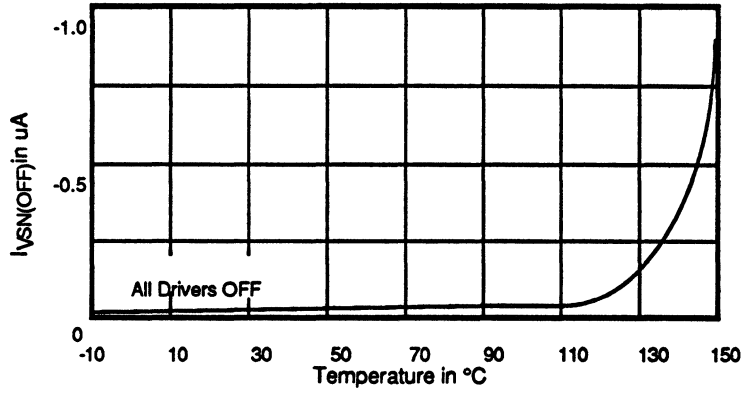


Figure 14. Typical Supply Current ($I_{VSN(OFF)}$) vs Temperature

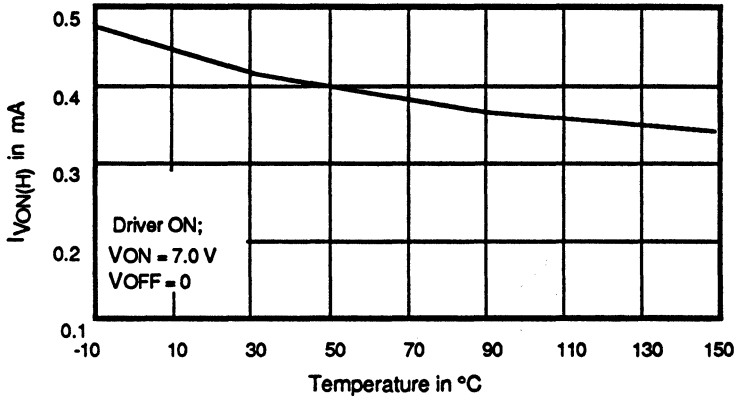


Figure 15. Typical Driver V_{ON} Input Current ($I_{VON(H)}$) vs Temperature

Electrical Characteristics (Continued)

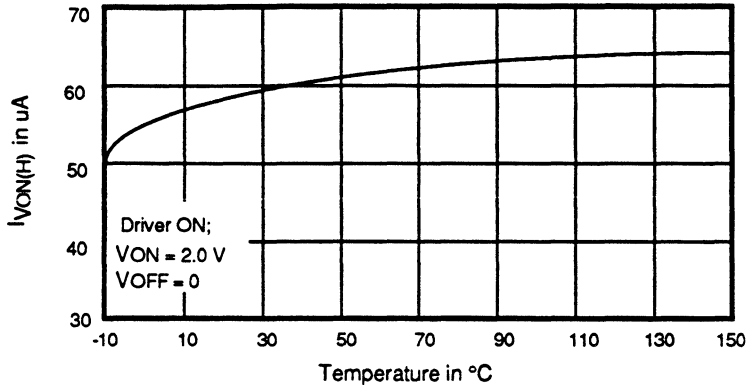


Figure 16. Typical Driver VON Input Current ($I_{VON(H)}$) vs Temperature

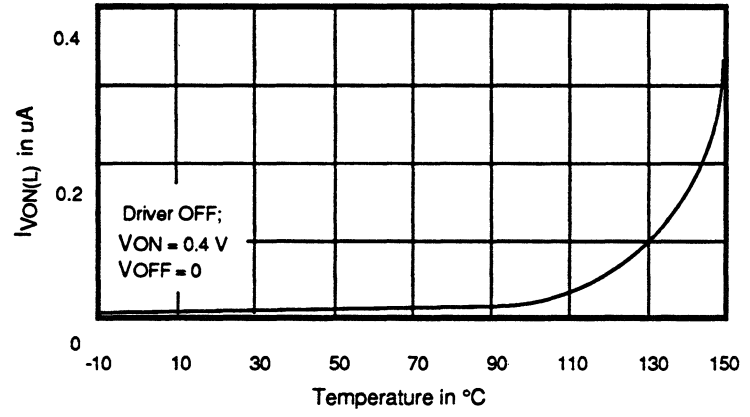


Figure 17. Typical Driver VON Input Current ($I_{VON(L)}$) vs Temperature

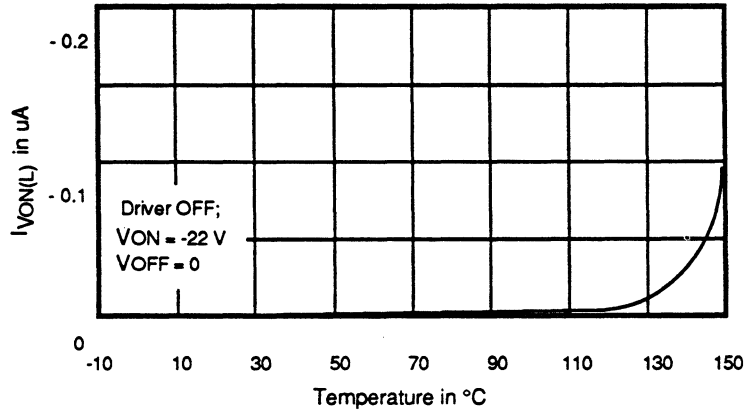


Figure 18. Typical Driver VON Input Current ($I_{VON(L)}$) vs Temperature

Electrical Characteristics (Continued)

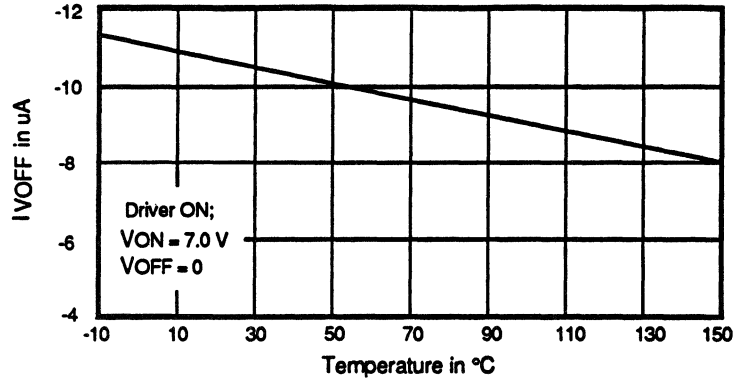


Figure 19. Typical Driver Input Current (I_{VOFF}) vs Temperature

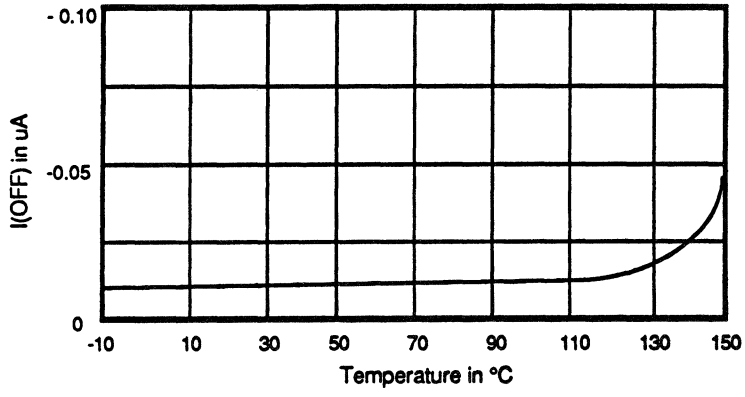


Figure 20. Typical Driver Output-Off Current (I(OFF)) vs Temperature

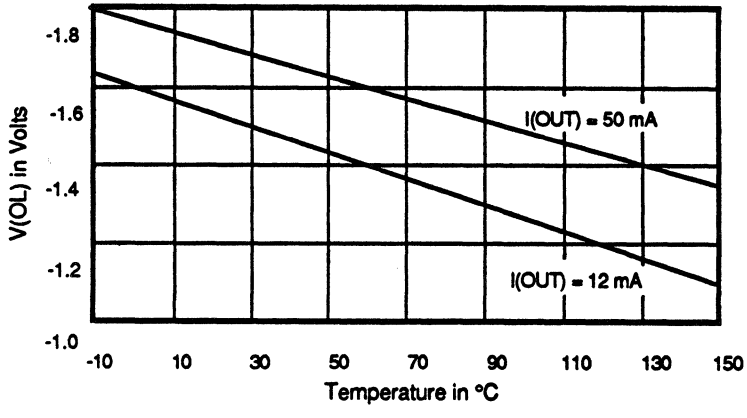


Figure 21. Typical Driver Output ON Voltage (V(OL)) vs Temperature

Applications

The LS1098AAF quad relay drivers are designed to operate with a high common-mode range (± 20 volts referenced to negative supply ground). Each driver has a common-mode range separate from the other drivers in the package, which permits input signals from more than one source in the system.

These drivers are intended for switching the ground side of loads which are directly connected to a negative supply, such as in a telephone relay system (Figure 22 illustrates a typical application).

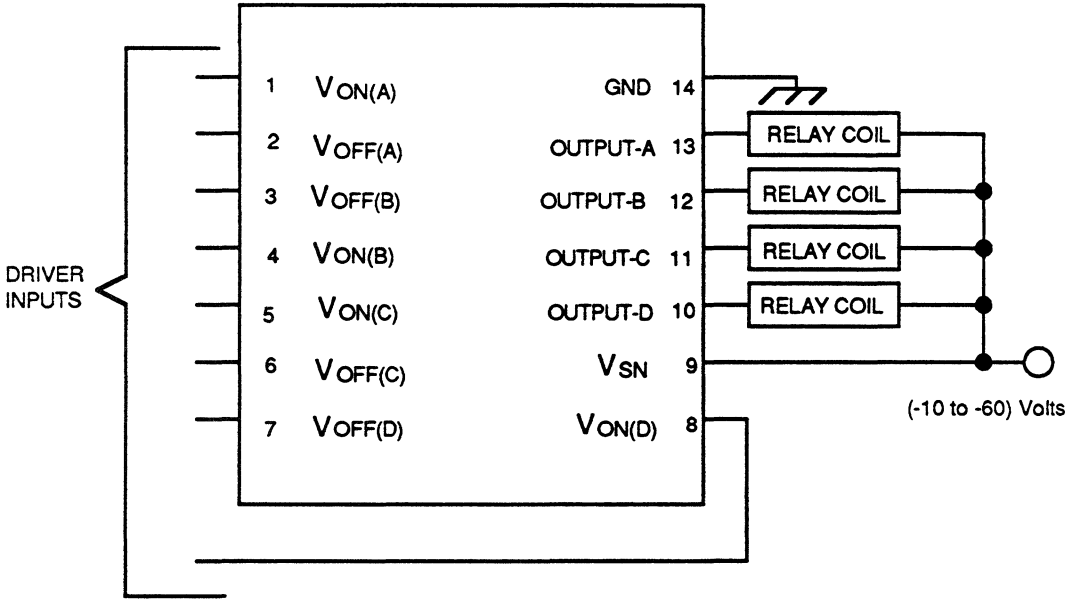
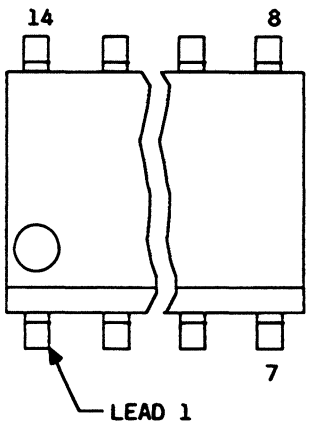
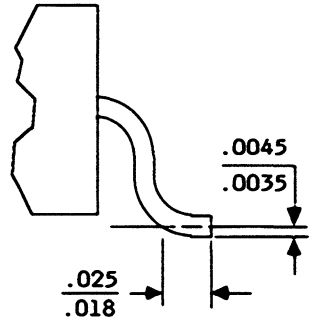


Figure 22.

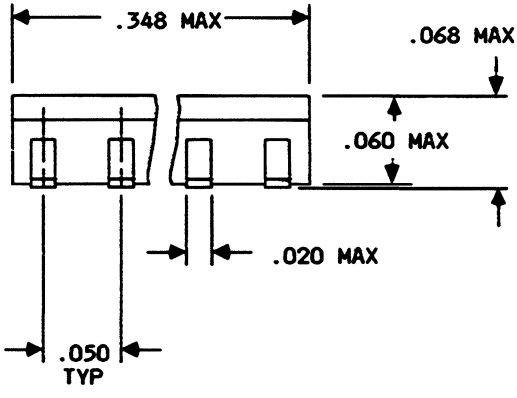
Outline Drawing

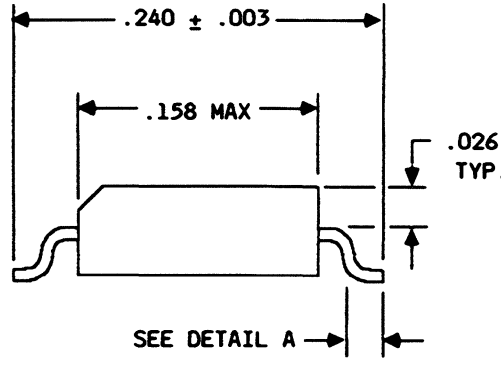
(Dimensions in Inches)





DETAIL A





Ordering Information

Device	Comcode
LS1098AAF	104405964

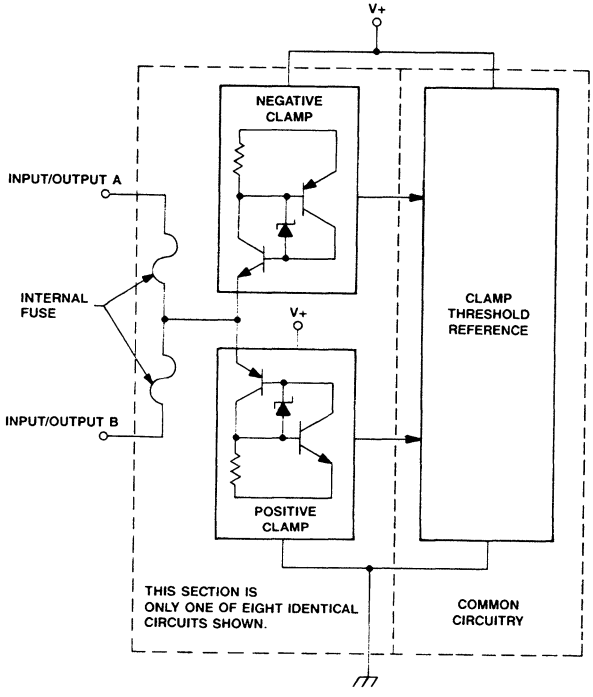
Description

The LB1010AD integrated circuit is a bidirectional over-voltage/over-current limiting device that protects up to eight digital lines. This circuit contains 16 on-chip fuses, 8 bidirectional voltage clamps, and a clamp threshold reference that tracks the power supply. During operation, transient on-line surges (within specified limits) are clamped to a safe level. However, if an extraordinarily high-current fault is present on an input (on the order of 1 amp), an on-chip fusing component will open, protecting the electronic circuits that are connected to the complementary output.

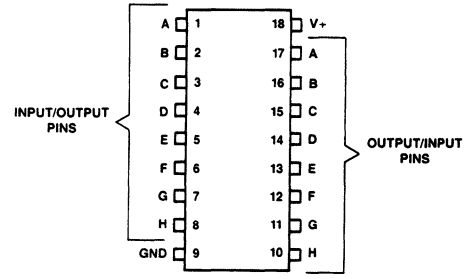
Features

- Bidirectional clamping
- Clamp threshold tracks supply voltage to 7.0 volts
- Protects 8 lines
- Input standoff voltage up to 65 volts (after on-chip fuse opens)
- Available in an 18-pin plastic DIP

Functional Diagram



Pin Diagram



COMPLEMENTARY INPUT/OUTPUT LEADS MAY BE INTERCHANGED FOR BIDIRECTIONAL OPERATION.

Maximum Ratings (T_A = 25°C unless otherwise specified)

Rating	Value	Unit
Ambient Operating Temperature Range	0 to 70	°C
Storage Temperature Range	−40 to +125	°C
Pin Temperature (soldering, 15 sec)	300	°C
Input Standoff Voltage (after on-chip fuse opens)*	65	V
Input Current Continuous, (each I/O and O/I pin)	±15	mA
Input Current 50% duty cycle (each I/O and O/I pin)	±50	mA
Voltage (V+ to GND)	7.0	V

* Rating applies from each I/O pin to its complementary O/I pin and vice versa.

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this data sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Pin Descriptions (see Pin Diagram)

Pin	Symbol	Name/Function
1 – 8	Input/Output (A – H)	Input/Output (I/O) pins A through H, respectively. The LB1010AD device consists of eight independent protector sections (Functional Diagram) designated by the letters A through H. Each protector section has two leads that may be used either as an input terminal or as an output terminal.
9	GND	Circuit common. This pin should be connected to system ground.
10 – 17	Output/Input (H – A)	Input/Output (O/I) pins H through A, respectively. For reference purposes, pins 1 through 8 are designated as I/O pins, while complementary pins 10 through 17 are designated as O/I pins. Unused I/O and O/I pins may float when not being used.
18	V+	External positive supply voltage pin range is 2.5 to 7.0 volts.

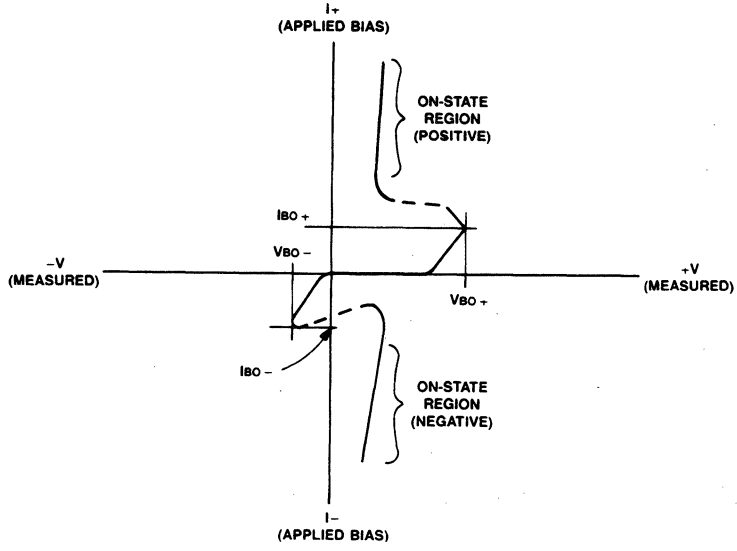


Figure 1. Symbology For Test Characteristics

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Characteristics	Min	Typ	Max	Unit
Power Supply Current V+ = 7.0 V	6.0	—	22	mA
Leakage Current (Note 1) V+ = 3.0 V, Pin Voltage = 0 V V+ = 3.0 V, Pin Voltage = 2.7 V	 — —	 — —	 ±1.0 ±10	 mA μA
Through Package Resistance (Each I/O pin to complementary O/I pin) I/O pin = 10 mA, O/I pin = GND	1.0	2.5	5.0	Ω
Positive Breakover Voltage ($V_{BO}+$)(Note 1) Bias Current Ramp (1% duty cycle)(Note 2) Measure voltage on pin complementary to the applied bias pin V+ = 3.0 V V+ = 5.0 V	 3.2 5.3	 — —	 4.8 6.6	 V V
Negative Breakover Voltage ($V_{BO}-$) (Note 1) V+ = 3.0 V−0.3	−0.3	—	−2.5	V
Positive On-State Voltage ($V_{ON}+$) (Note 1) Bias current (1% duty cycle) = 500 mA, V+ = 3.0 V Measure voltage on pin complementary to applied bias pin	1.0	—	2.0	V
Negative On-State Voltage ($V_{ON}-$) (Note 2) Bias current (1% duty cycle) = −500 mA, V+ = 3.0 V	0.5	—	2.0	V
Positive Breakover Current ($I_{BO}+$) (Note 1) Bias current (1% duty cycle) (Note 3) Measurements on pin to which bias is applied, V+ = 3.0 V	100	—	200	mA
Negative Breakover Current ($I_{BO}-$) (Note 1)	−100	—	−250	mA
Positive Release Current ($I_{REL}+$) (Note 1) Bias current (1% duty cycle) (Note 4) Measure voltage on pin to which bias is applied, V+ = 3.0 V	100	—	350	mA
Negative Release Current ($I_{REL}-$) (Note 1)	−75	—	−300	mA

Notes:

1. This test applies to each I/O and O/I pin.
2. A ramped bias current (1% duty cycle) is applied to the appropriate I/O or O/I pin. Breakover voltage is measured as the peak magnitude of voltage which occurs as the bias current is increased in magnitude from zero to a value which forces the device into the low impedance on-state region of its characteristic (Figure 1). Polarity designations should be observed with respect to GND.
3. Breakover current is that value of current applied to the specified pin at which the breakover voltage peak occurs (Figure 1).
4. Force the device into a low impedance on-state condition. Reduce the current (as specified in the following sentences) and measure the voltage on the pin to which the bias is applied (Figure 2).
   The Positive Release Current is recorded when the voltage on the specified pin equals V+.
   The Negative Release Current is recorded when the voltage on the specified pin equals zero.

Characteristics

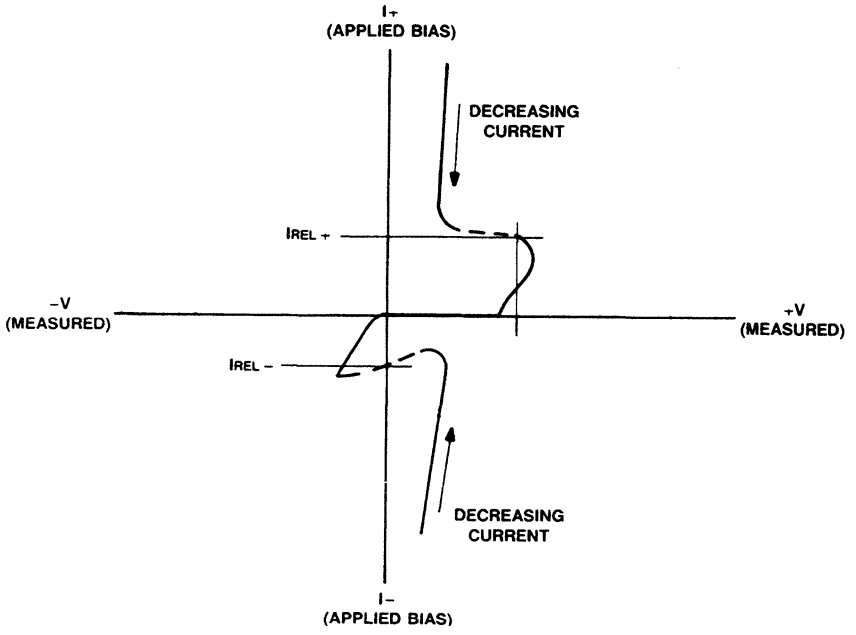


Figure 2. Release Current Characteristics

Characteristics and Conditions	Typical	Unit
Line Capacitance (V+ = 5.0 V, V_{IN} = 0.3 to 4.7 V)	12.0	pF
Positive ON-State Resistance (Figure 1)	0.7	Ω
Negative ON-State Resistance (Figure 1)	0.8	
Fusing Time (Isurge = 1.0A)	6.0	μs

Characteristics
(Continued)

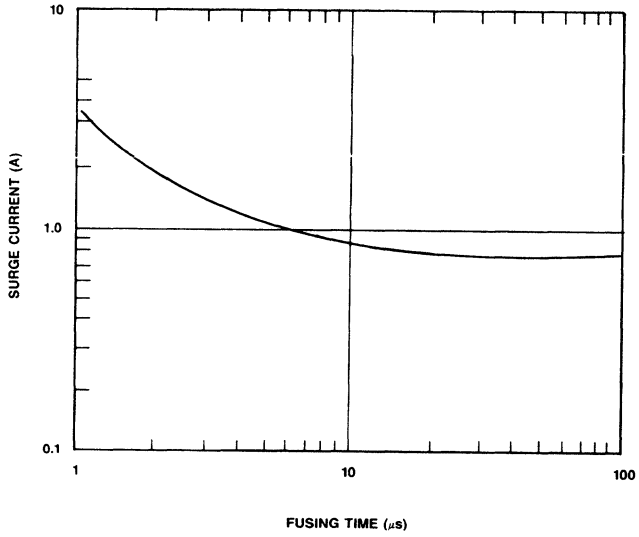


Figure 3. Typical Fusing Characteristics

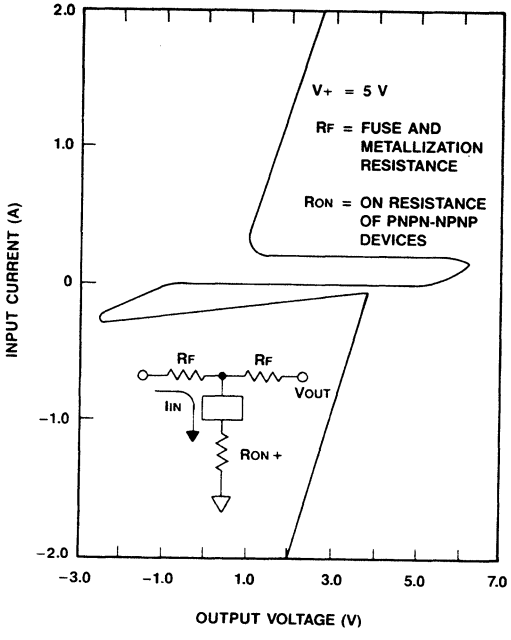


Figure 4. Typical Operating Characteristic

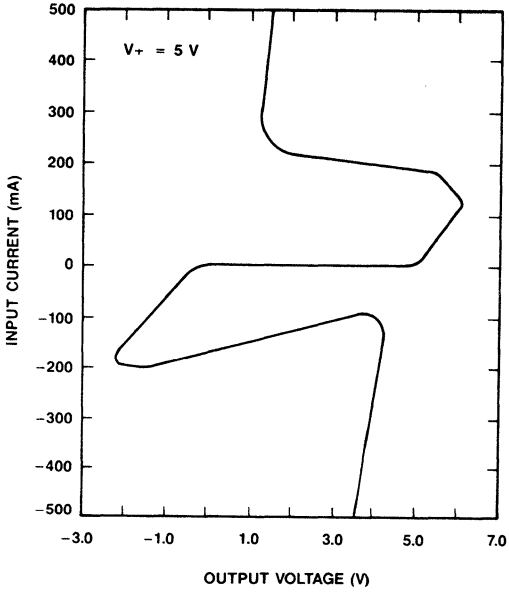


Figure 5. Typical Operating Characteristic

Applications

Figure 6 illustrates connections for line protection applications. No additional circuitry is needed with the LB1010AD device other than a 0.1 μF by-pass capacitor as close as possible between V + and GND.

The clamp threshold reference circuit (Functional Diagram) tracks the external V + supply. The positive/negative clamps will begin to clamp the digital data lines at a voltage which will be only slightly above the voltage of the external V + power supply (Figure 5). Since the threshold voltage is a function of the external V + power supply, the LB1010AD Octal Line Protector can be used with a variety of logic families up to 7 volts.

If the resulting current exceeds the conditions shown under Fusing Characteristics in Figure 3, the associated on-chip fuse will open permanently, disconnecting the affected Digital Data Line until a new LB1010AD device is installed. The maximum voltage which may be applied to an open input line is 65 volts.

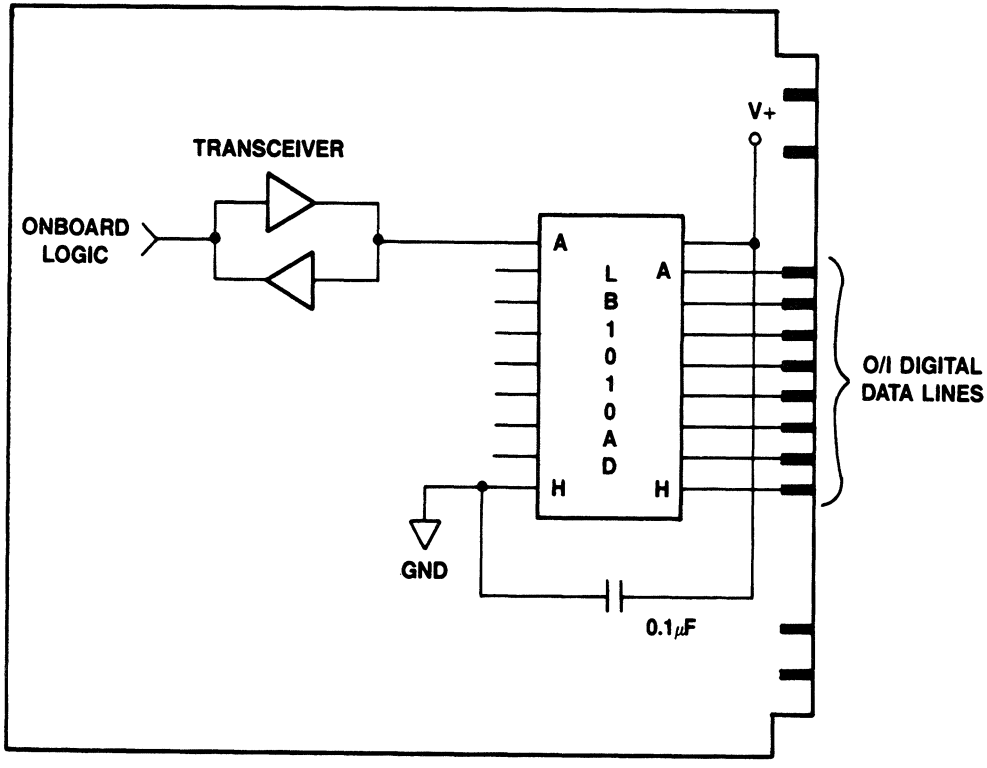
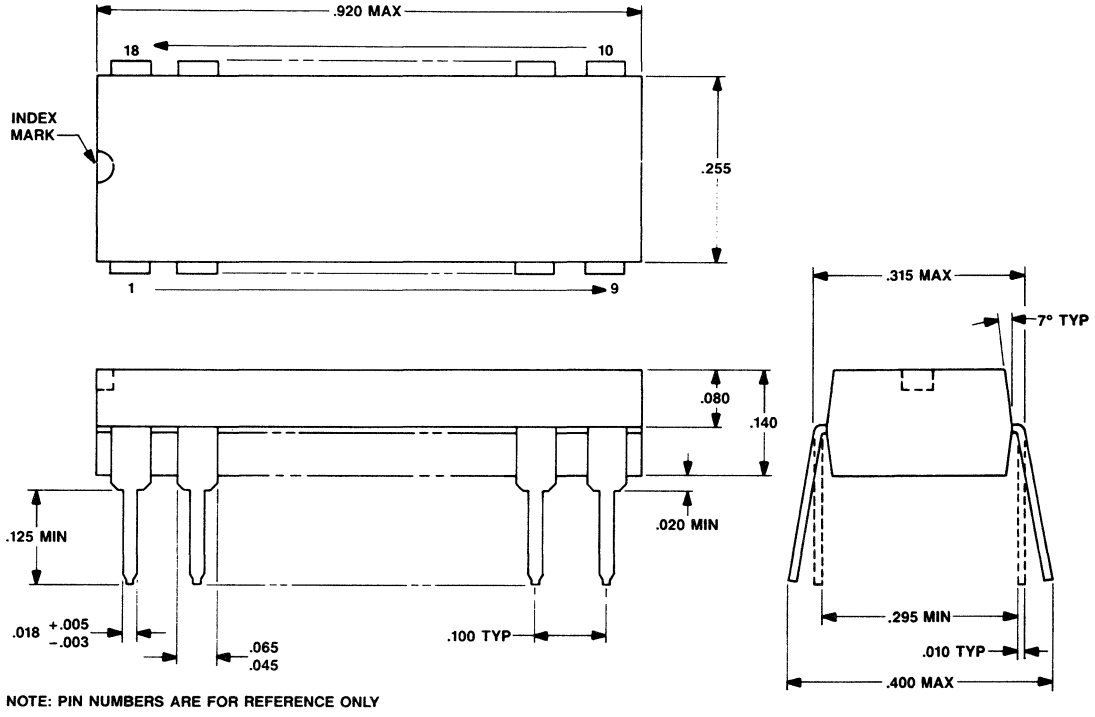


Figure 6. Octal Line Protector Application

Outline Drawing

(Dimensions in Inches)



NOTE: PIN NUMBERS ARE FOR REFERENCE ONLY

Ordering Information

Device	Comcode
LB1010AD	104208806

PRELIMINARY

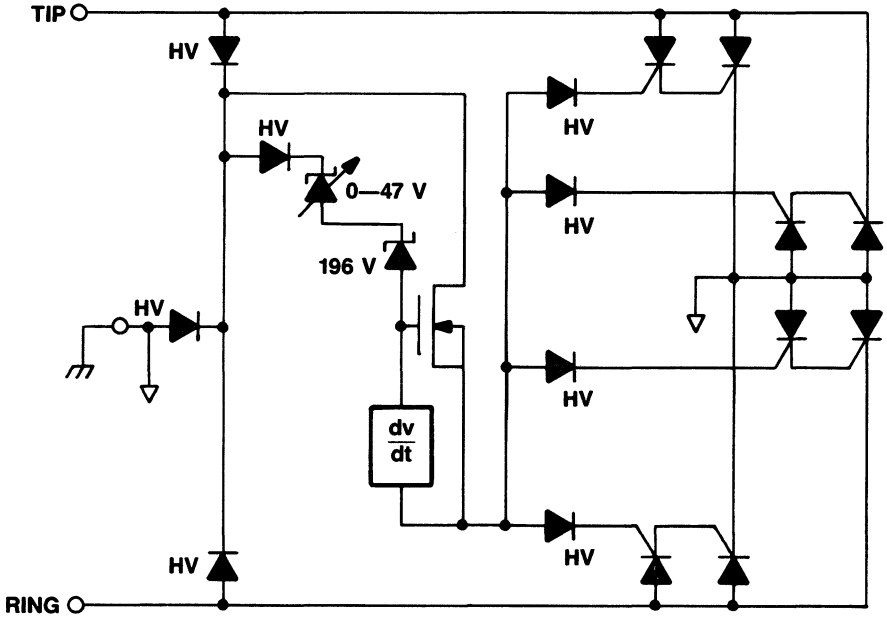
Description

The LH1150-Type Integrated Secondary Protectors (ISP) are a family of two-wire bidirectional overvoltage protection devices used for secondary protection of electronic switch line units. Each circuit contains four thyristor devices with associated threshold sensing. The device is fabricated in a high-voltage dielectrically isolated BCDMOS process and is packaged in a three lead ruggedized plastic package. In many applications the LH1150-Type ISP devices are interchangeable with Texas Instruments voltage suppressor part TISP229A and TECCOR Electronics surge protector part P101.

Features

- Bidirectional overvoltage protection
- Crowbars surge waves and power cross faults
- Internal voltage trim capability to meet threshold voltage requirements
- Symmetrical pinout
- No Heat sink required

Functional Diagram



Electrical Characteristics

Characteristic/Conditions	Min	Typ	Max	Unit
Offstate Current (I_D)				
V_D = +/− 160 V	—	—	1.0	μA
V_D = +/− 210 V	—	—	5.0	mA
V_D = +/− 224 V *	—	—	10.0	mA
Breakover Voltage (V_{BO}) @ I_{BO}	—	230	—	V
Breakover Current (I_{BO}) 20 Hz Sine Wave	—	50	—	mA
Holding Current (I_H) R_S = 300 Ω (T-R, R-T)				
LH1150AAM	110	150	—	mA
LH1150BAM	155	220	—	mA
LH1150CAM	165	220	—	mA
Peak Voltage (power cross) (T-G, R-G) V_S = 600 Vrms R_S = 700 Ω t = 1.0 s	—	—	255**	V
Peak Voltage (lightning strike) (T-G, R-G) Vsurge = 1000 Vpeak 10/1000 μs R_S = 110 Ω	—	—	255**	V

* This parameter is guaranteed only for the LH1150CAM device.

** Peak voltage will increase by a factor of approximately 0.2 V/°C as ambient temperature rises.

R_S is the resistance in series with the ISP device during characteristics specified.

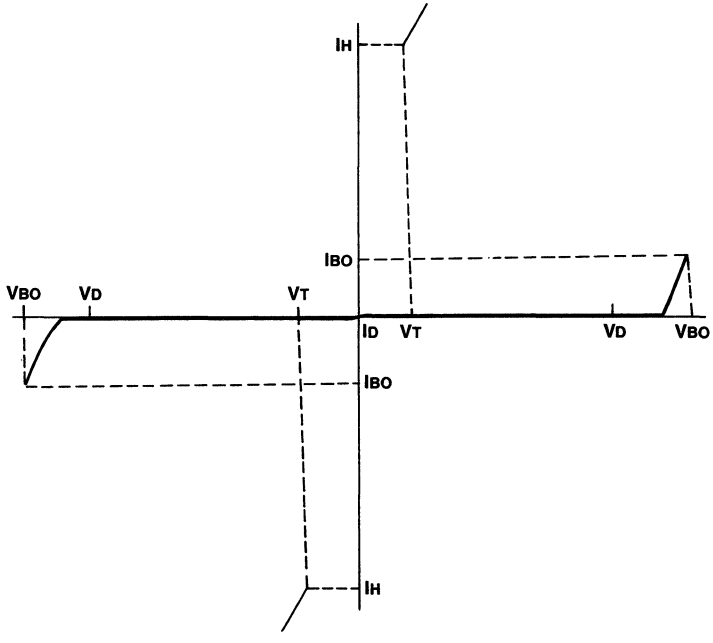


Figure 1. Typical Electrical Characteristics

Applications

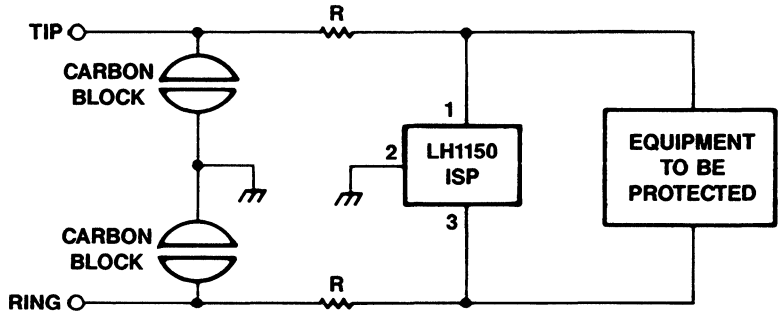


Figure 2. Application Diagram

Characteristic Curves

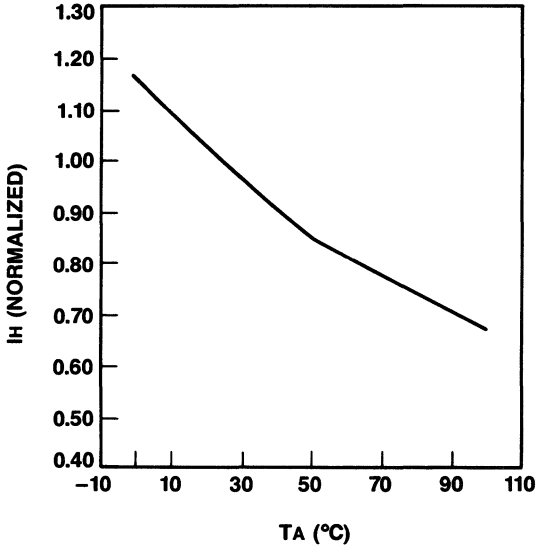


Figure 3. Holding Current vs Temperature

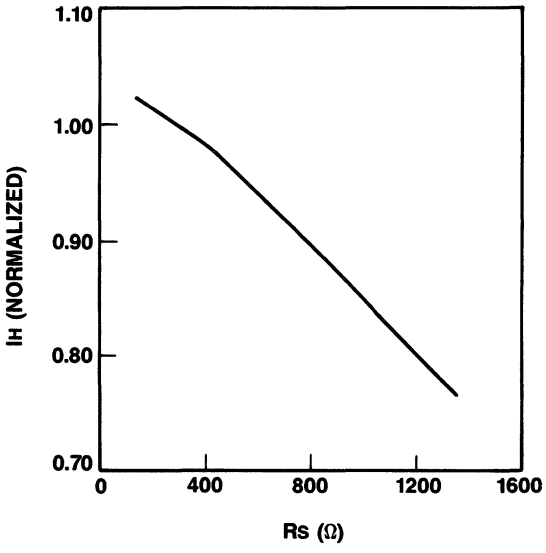
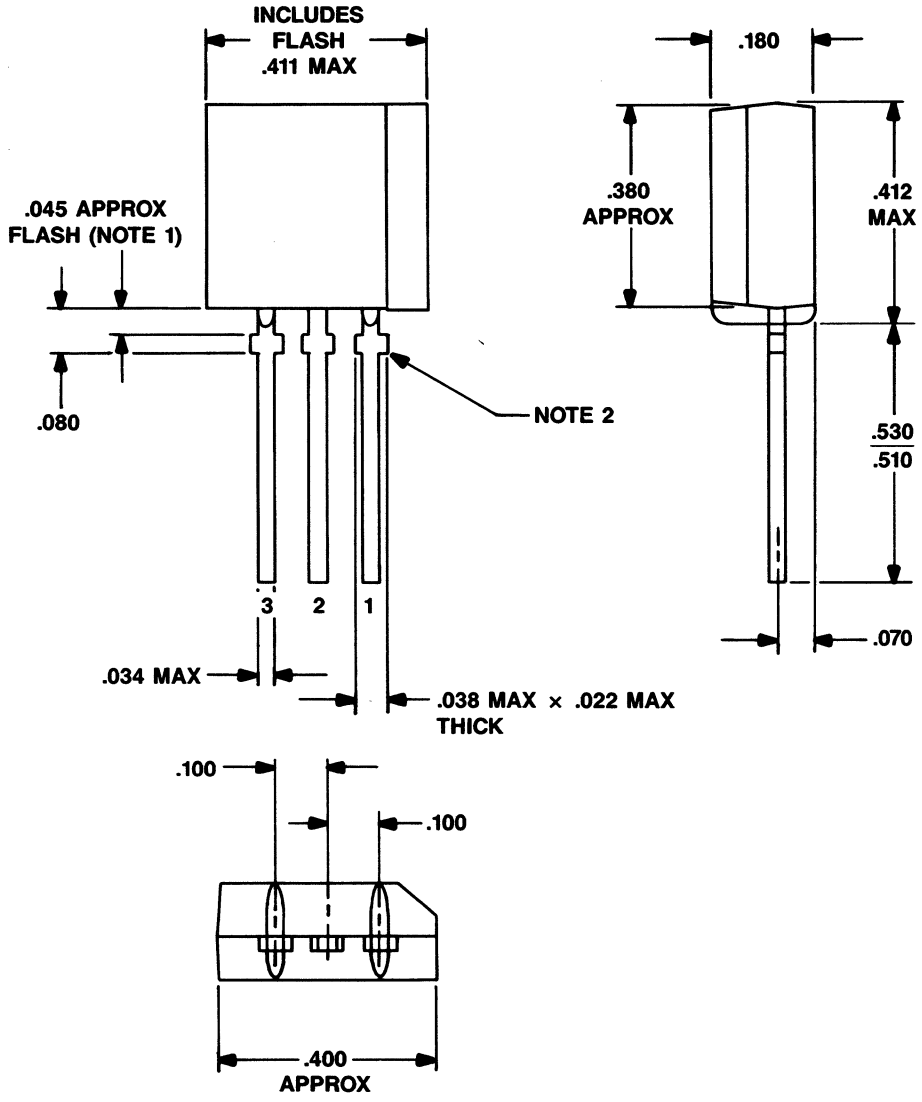


Figure 4. Holding Current vs Series Resistance

Outline Drawing

(Dimensions in Inches)



Note 1. Flash permissable in this area along with lead length not to exceed the .038″ max. wide X .022″ max thickness of the leads.

Note 2. Burrs in trim are not to exceed overall lead thickness of .023″.

Ordering Information

Device	Comcode
LH1150AAM	104435607
LH1150BAM	104435615
LH1150CAM	104435623

OCTAL HIGH-VOLTAGE N-CHANNEL MOSFET ARRAY AN0130NA

PRELIMINARY

Monolithic N-Channel Enhancement-Mode

Description

The AN0130NA Octal High-Voltage N-Channel MOSFET Array contains eight N-Channel DMOS drivers configured common-source, open drains, and ESD protected gates. The device interfaces MOS logic level inputs to outputs capable of withstanding 300 volts and sinking 30 mA. The devices are fabricated in AT&T's proprietary BCDMOS technology with dielectric isolation. This process offers unprecedented freedom from latchup and parasitic device interaction.

Features

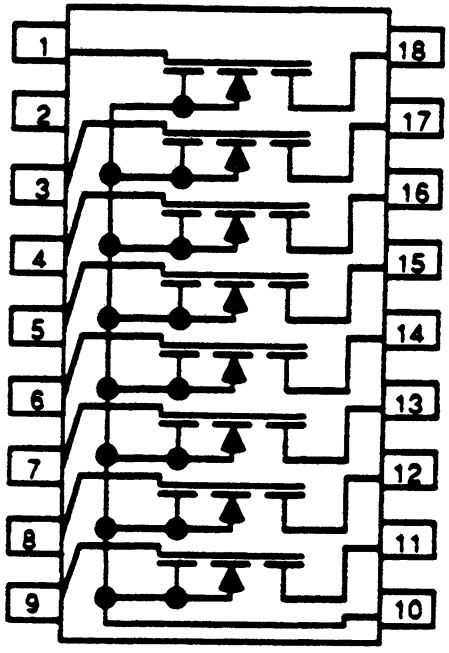
- On-chip ESD protection
- Operating voltage up to 300 volts
- Processed with BCDMOS technology
- Gate CMOS Logic compatible

Applications

- Test systems
- Industrial controls
- Telecommunications
- Electrostatic array drivers
- Electroluminescent panel drivers
- General multi-channel driver array

BV_{DS}	$R_{DS}(ON)$	$I_D(ON)$
300 V	300 Ω	25 mA

Functional and Pin Diagram



Maximum Ratings (At 25°C unless otherwise specified)	
Ambient Operating Temperature Range	−40 to +85°C
Storage Temperature Range	−55 to +150°C
Pin Soldering Temperature (t = 15 sec max.)	300°C
Drain Current, DC	30 mA
Drain Current, Pulsed (tp = 200 μs; duty cycle = 2%)	75 mA
Gate-to-Source Voltage	±15 V
Drain-to-Source Voltage	300 V
Power Dissipation	1500 mW

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic	Test Condition	Min	Typ	Max	Unit
Drain-to-Source Breakdown Voltage, BV_{DS}	I_D = 1 μA; V_{GS} = 0	300	350	—	V
Gate Threshold Voltage, $V_{GS(th)}$	V_{GS} = V_{DS}; I_D = 1.0 mA	1.5	3.0	4.0	V
Gate Leakage Current, I_G	V_{GS} = ±15 V; V_{DS} = 0	—	60×10^{-12}	10×10^{-9}	A
Drain Current, I_D	V_{GS} = 0; V_{DS} = 300 V	—	250×10^{-12}	3×10^{-9}	A
Saturation Current	V_{DS} = 25 V; V_{GS} = 10 V	25	57	—	mA
Static Drain-to-Source ON-State resistance $R_{DS(ON)}$	V_{GS} = 10 V; I_D = 10 mA	—	175	300	Ω

Characteristic	Test Condition	Typ	Unit
Change in Gate Threshold Voltage With Temperature	V_{GS} = V_{DS}; I_D = 1.0 mA T_A = (−25 to +85)°C T_{REF} = 25°C	−1.1	mV/°C
Change in $R_{DS(ON)}$ With Temperature	V_{GS} = 10 V; I_D = 10 mA T_A = (−25 to +85)°C T_{REF} = 25°C	0.8	%/°C
Switching Times	Functional Diagram; $V_{GS(ON)}$ = 10 V V_{DS} = 25 V; I_D = 10 mA		
Turn-ON Delay Time; td(ON)		28	ns
Rise Time; tr		80	ns
Turn-OFF Delay Time; td(OFF)		70	ns
Fall Time; tf		300	ns

Test Circuits

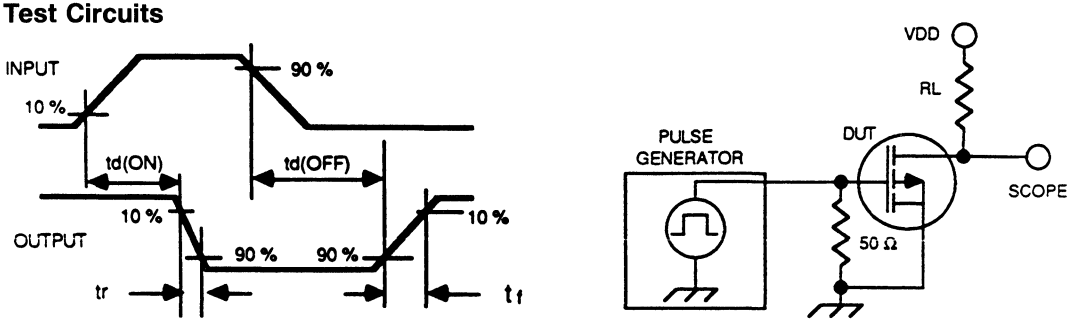
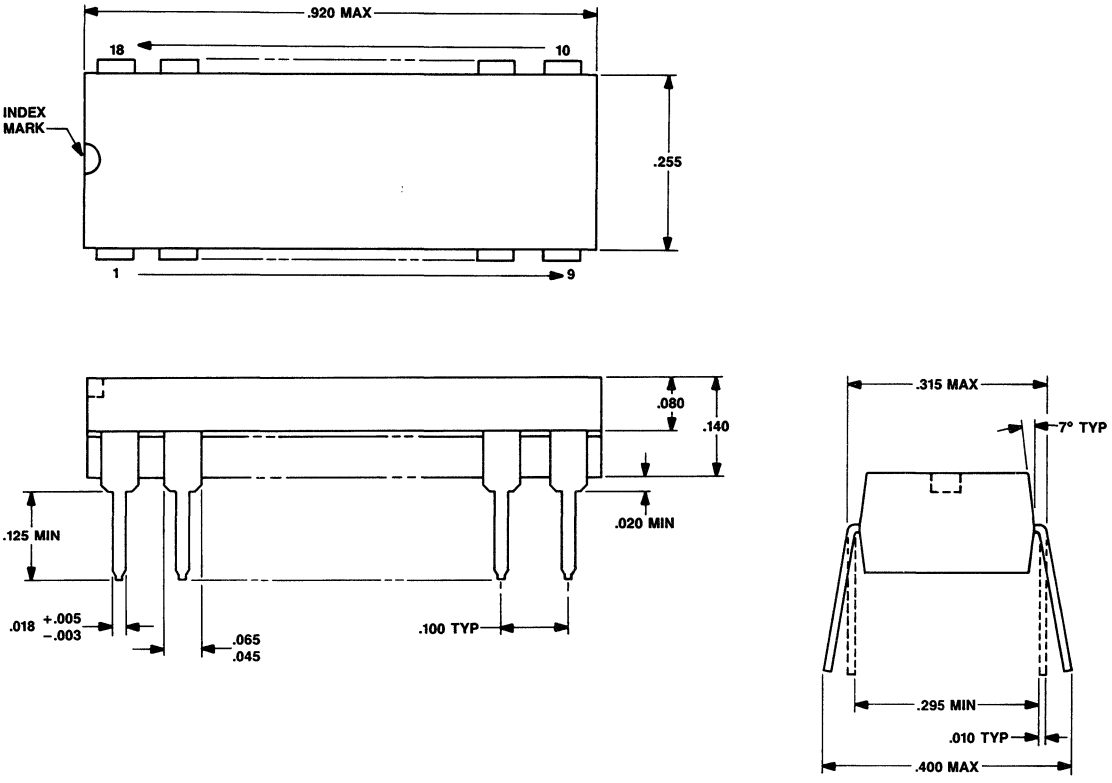


Figure 1. Switching Waveforms and Simplified Test Circuit

Outline Drawing (Dimensions in inches)



Note: Pin numbers are for reference only.

Ordering Information

Device	Comcode
AN0130NA	104432554

OCTAL HIGH-VOLTAGE N-CHANNEL MOSFET ARRAY AN0132NAR

ADVANCE

Monolithic N-Channel Enhancement-Mode

Description

The AN0132NAR Octal High-Voltage N-Channel MOSFET Array contains eight independent N-Channel DMOS drivers configured with common-sources, open drains and ESD protected gates. The AN0132NAR, because of its robust design and construction, is capable of discharging capacitive loads up to 1 μF. The device interfaces MOS logic level inputs to outputs capable of withstanding 320 volts and sinking 30 mA. The devices are fabricated in AT&T's proprietary BCDMOS technology with dielectric isolation. This process offers unprecedented freedom from latchup and parasitic device interaction.

Features

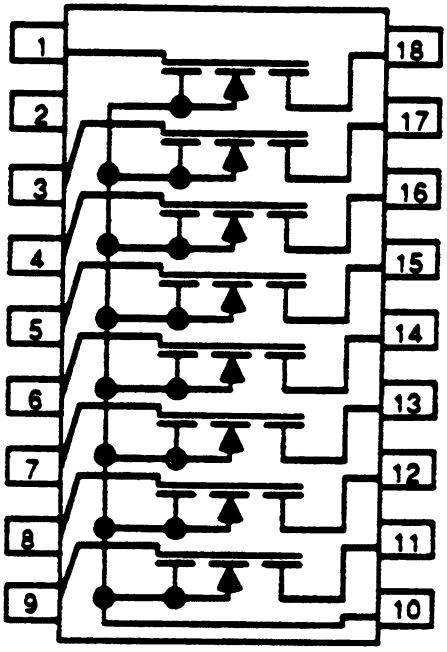
- On-chip ESD protection
- Operating voltage up to 320 volts
- Processed with BCDMOS technology
- Gate CMOS Logic Compatible

Applications

- Test systems
- Industrial controls
- Telecommunications
- Electrostatic array drivers
- Electroluminescent panel drivers
- General multi-channel driver array

BV_{DS}	$R_{DS(ON)}$	$I_{D(ON)}$
320 V	300 Ω	25 mA

Functional and Pin Diagram



Maximum Ratings (At 25°C unless otherwise specified)	
Ambient Operating Temperature Range	−40 to +85°C
Storage Temperature Range	−55 to +150°C
Pin Soldering Temperature (t = 15 sec max.)	300°C
Drain Current, DC	30 mA
Drain Current, Pulsed (tp = 200 μs; duty cycle = 2%)	75 mA
Gate-to-Source Voltage	±15 V
Drain-to-Source Voltage	300 V
Power Dissipation	1500 mW

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic	Test Condition	Min	Typ	Max	Unit
Drain-to-Source Breakdown Voltage, BV_{DS}	I_D = 1 μA; V_{GS} = 0	320	380	—	V
Gate Threshold Voltage, $V_{GS(th)}$	V_{GS} = V_{DS}; I_D = 1.0 mA	1.5	3.0	4.0	V
Gate Leakage Current, I_G	V_{GS} = ±15 V; V_{DS} = 0	—	60×10^{-12}	10×10^{-9}	A
Drain Current, I_D	V_{GS} = 0; V_{DS} = 320 V	—	250×10^{-12}	1×10^{-9}	A
Saturation Current	V_{DS} = 25 V; V_{GS} = 10 V	25	57	—	mA
Static Drain-to-Source ON-State resistance $R_{DS(ON)}$	V_{GS} = 10 V; I_D = 10 mA	—	175	300	Ω

Characteristic	Test Condition	Typ	Unit
Change in Gate Threshold Voltage With Temperature	V_{GS} = V_{DS}; I_D = 1.0 mA T_A = (−25 to +85)°C T_{REF} = 25°C	−1.1	mV/°C
Change in $R_{DS(ON)}$ With Temperature	V_{GS} = 10 V; I_D = 10 mA T_A = (−25 to +85)°C T_{REF} = 25°C	0.8	%/°C
Switching Times	Functional Diagram; $V_{GS(ON)}$ = 10 V V_{DS} = 25 V; I_D = 10 mA		
Turn-ON Delay Time; td(ON)		28	ns
Rise Time; tr		80	ns
Turn-OFF Delay Time; td(OFF)		70	ns
Fall Time; tf		300	ns

Test Circuits

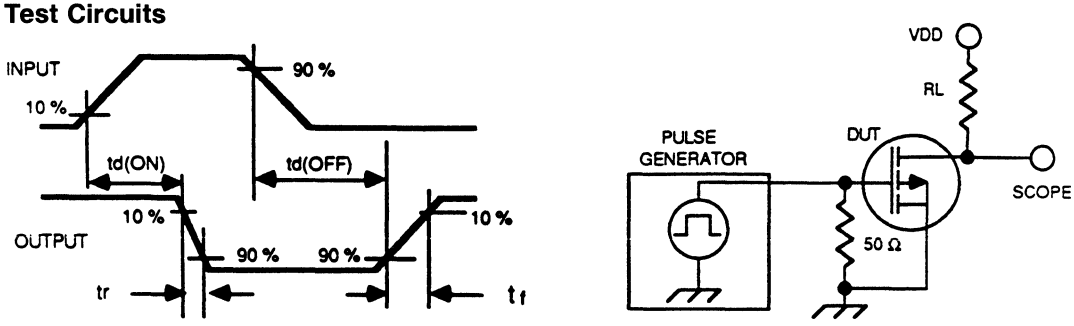
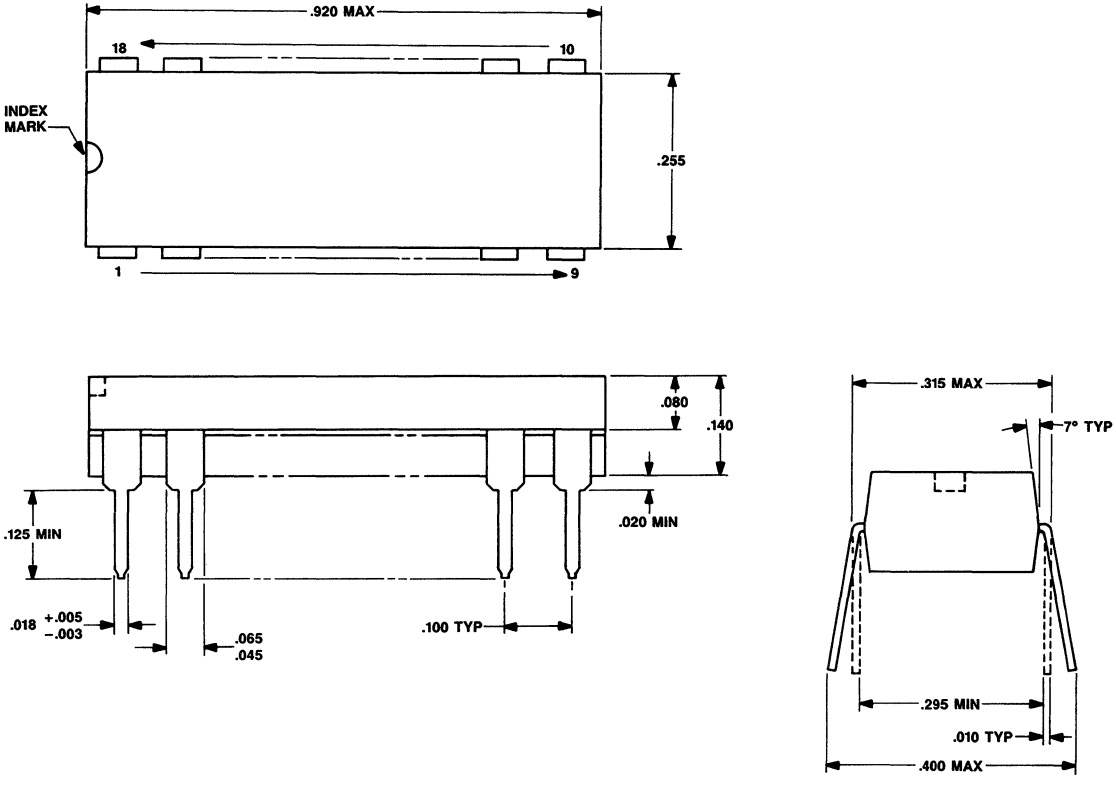


Figure 1. Switching Waveforms and Simplified Test Circuit

Outline Drawing (Dimensions in inches)



Ordering Information

Device	Comcode
AN0132NAR	104439898

OCTAL HIGH-VOLTAGE P-CHANNEL MOSFET ARRAY AP0130NA

PRELIMINARY

Monolithic P-Channel Enhancement-Mode

Description

The AP0130NA Octal High-Voltage P-Channel MOSFET Array contains eight P-Channel DMOS drivers configured common-source, open drains, and ESD protected gates. The device interfaces MOS logic level inputs to outputs capable of withstanding 300 volts and sinking 15 mA. The devices are fabricated in AT&T's proprietary BCDMOS technology with dielectric isolation. This process offers unprecedented freedom from latchup and parasitic device interaction.

Features

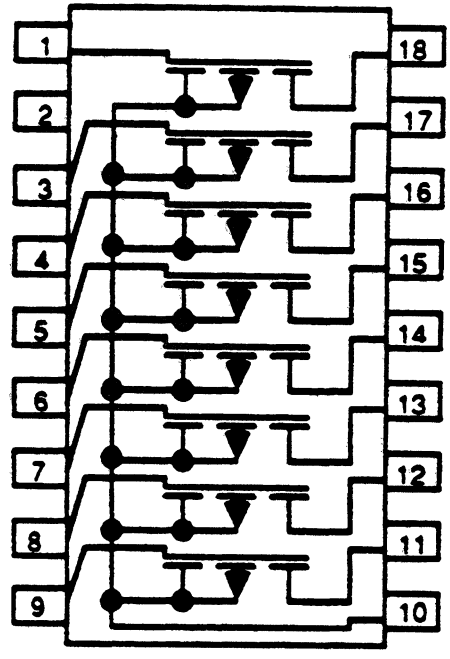
- On-chip ESD protection
- Operating voltage up to 300 volts
- Processed with BCDMOS technology
- Gate CMOS Logic compatible

Applications

- Test systems
- Industrial controls
- Telecommunications
- Electrostatic array drivers
- Electroluminescent panel drivers
- General multi-channel driver array

BV_{DS}	$R_{DS(ON)}$	$I_{D(ON)}$
−300	600 Ω	−15 mA

Functional and Pin Diagram



Maximum Ratings (At 25°C unless otherwise specified)	
Ambient Operating Temperature Range	−40 to +85°C
Storage Temperature Range	−55 to +150°C
Pin Soldering Temperature (t = 15 sec max.)	300°C
Drain Current, dc	−15 mA
Drain Current, Pulsed (tP = 200 μs; duty cycle = 2%)	−40 mA
Gate-to-Source Voltage	±20 V
Drain-to-Source Voltage	−300
Power Dissipation	1500 mW

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic	Test Condition	Min	Typ	Max	Unit
Drain-to-Source Breakdown Voltage, BV_{DS}	I_D −1 μA; V_{GS} = 0	−300	−380	—	V
Gate Threshold Voltage, $V_{GS(th)}$	V_{GS} = V_{DS}; I_D = 1.0 mA	−0.75	−2.10	−3.0	V
Gate Leakage Current, I_G	V_{GS} =15 V; V_{DS} = 0	—	-40×10^{-12}	-10×10^{-9}	A
Drain Current, I_D	V_{GS} = 0; V_{DS} = 300 V	—	$-.5\times10^{-9}$	-3×10^{-9}	A
Saturation Current	V_{DS} = −25 V; V_{GS} = −10 V	−15	−40	—	mA
Static Drain-to-Source ON-State Resistance, $R_{DS(ON)}$	V_{GS} = −10 V; I_D = −10 mA	—	450	600	Ω

Characteristic	Test Condition	Typ	Unit
Change in Gate Threshold Voltage With Temperature	V_{GS} = V_{DS}; I_D = 1.0 mA T_A = −25 to +85°C T_{REF} = 25°C	−1.4	mV/°C
Change in $R_{DS(ON)}$ With Temperature	V_{GS} = 10 V; I_D = 10 mA T_A = −25 to +85°C T_{REF} = 25°C	0.8	%/°C
Switching Times	Functional Diagram; $V_{GS(ON)}$ = 10 V V_{DS} = 25 V; I_D = 10 mA		
Turn-ON Delay Time; td(ON)		60	ns
Rise Time; tr		240	ns
Turn-OFF Delay Time; td(OFF)		140	ns
Fall Time; tf		900	ns

Test Circuit

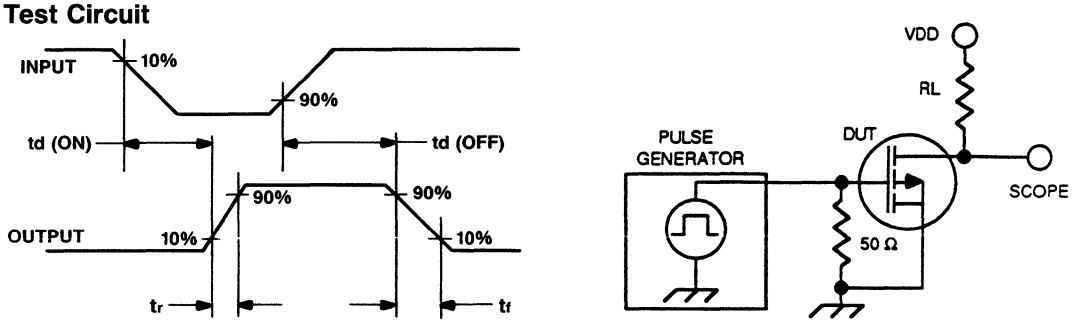
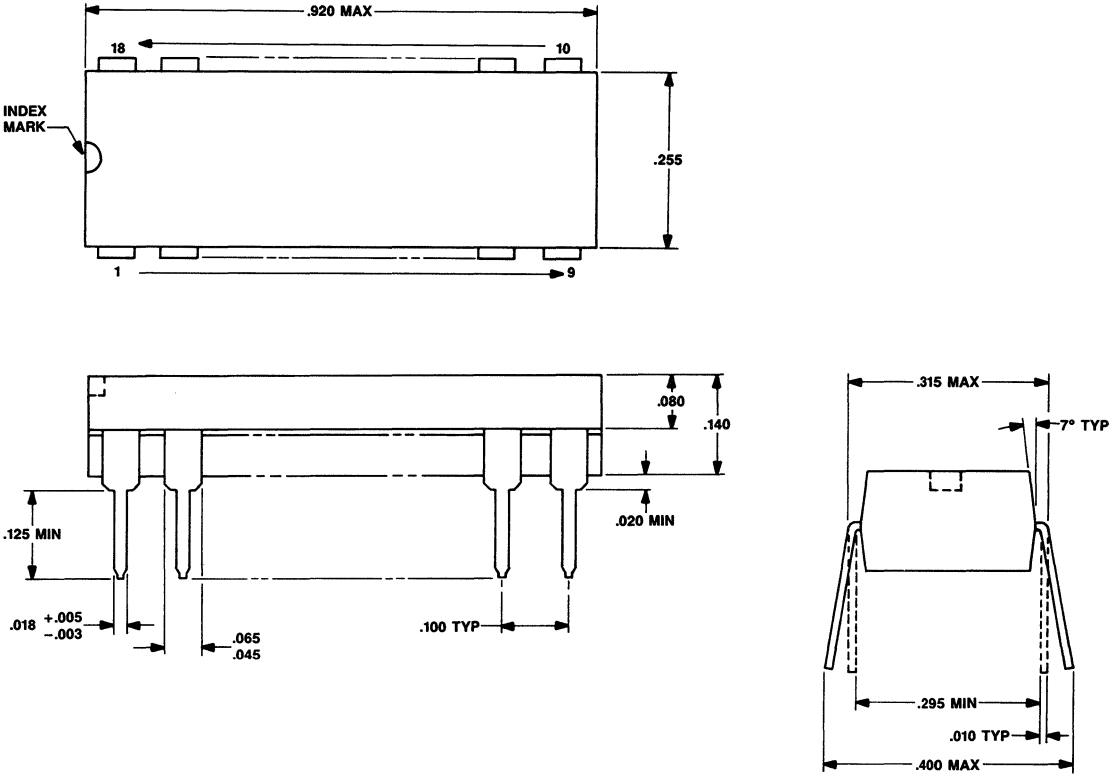


Figure 1. Switching Waveforms and Simplified Test Circuit

Outline Drawing (Dimensions in inches)



Ordering Information

Device	Comcode
AP0130NA	104432562

QUAD HIGH-VOLTAGE N-CHANNEL MOSFET ARRAY LH1162AAP

ADVANCE

Monolithic N-Channel Enhancement-Mode

Description

The LH1162AAP Quad High-Voltage N-Channel MOSFET Array contains four independent N-Channel DMOS drivers with ESD protected gates. The device interfaces MOS logic level inputs to outputs capable of withstanding 350 volts and sinking 30 mA.

The devices are fabricated in AT&T's proprietary BCDMOS technology with dielectric isolation. This process offers unprecedented freedom from latchup and parasitic device interaction.

Features

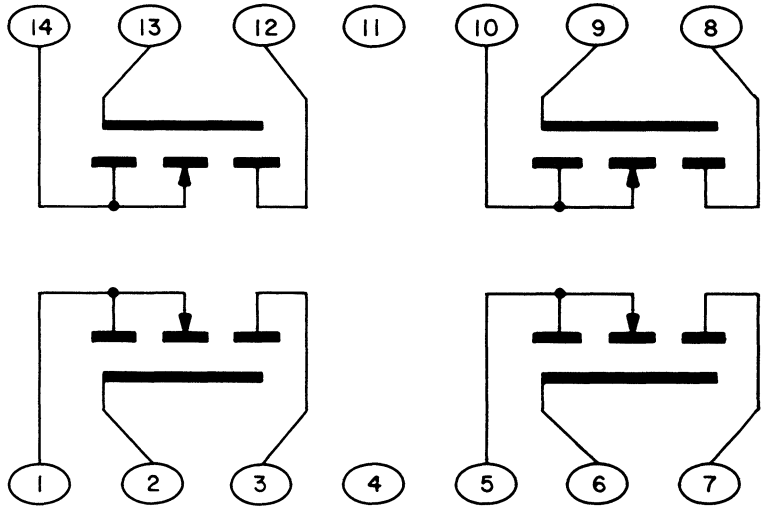
- On-chip ESD protection
- Operating voltage up to 350 volts
- Processed with BCDMOS technology
- Gate CMOS Logic Compatible

BV_{DS}	$R_{DS(ON)}$	$I_{D(ON)}$
350 V	380 Ω	25 mA

Applications

- Test systems
- Industrial controls
- Telecommunications
- Electrostatic array drivers
- Electroluminescent panel drivers
- General multi-channel driver array

Functional Diagram



Maximum Ratings (At 25°C unless otherwise specified)	
Ambient Operating Temperature Range	−40 to +85°C
Storage Temperature Range	−55 to +150°C
Pin Soldering Temperature (t = 15 sec max.)	300°C
Drain Current, DC	30 mA
Drain Current, Pulsed (tp = 200 μs; duty cycle = 2%)	75 mA
Gate-to-Source Voltage	±15 V
Drain-to-Source Voltage	350 V
Power Dissipation	750 mW

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Minimum and maximum values are testing requirements. Typical values are characteristics of the device and are the result of engineering evaluations. Typical values are for information purposes only and are not part of the testing requirements.

Characteristic	Test Condition	Min	Typ	Max	Unit
Drain-to-Source Breakdown Voltage, BV_{DS}	I_D = 1 μA; V_{GS} = 0	350	380	—	V
Gate Threshold Voltage, $V_{GS(th)}$	V_{GS} = V_{DS}; I_D = 1.0 mA	1.5	3.0	4.0	V
Gate Leakage Current, I_G	V_{GS} = ±15 V; V_{DS} = 0	—	60×10^{-12}	10×10^{-9}	A
Drain Current, I_D	V_{GS} = 0	—	250×10^{-12}	1×10^{-9}	A
Saturation Current	V_{DS} = 25 V; V_{GS} = 10 V	25	57	—	mA
Static Drain-to-Source ON-State resistance $R_{DS(ON)}$	V_{GS} = 12 V; I_D = 1.0 mA	—	175	380	Ω

Characteristic	Test Condition	Typ	Unit
Change in Gate Threshold Voltage With Temperature	V_{GS} = V_{DS}; I_D = 1.0 mA T_A = (−25 to +85)°C T_{REF} = 25°C	−1.1	mV/°C
Change in $R_{DS(ON)}$ With Temperature	V_{GS} = 10 V; I_D = 10 mA T_A = (−25 to +85)°C T_{REF} = 25°C	0.8	%/°C
Switching Times	Functional Diagram; $V_{GS(ON)}$ = 10 V V_{DS} = 25 V; I_D = 10 mA		
Turn-ON Delay Time; td(ON)		28	ns
Rise Time; tr		80	ns
Turn-OFF Delay Time; td(OFF)		70	ns
Fall Time; tf		300	ns

Test Circuits

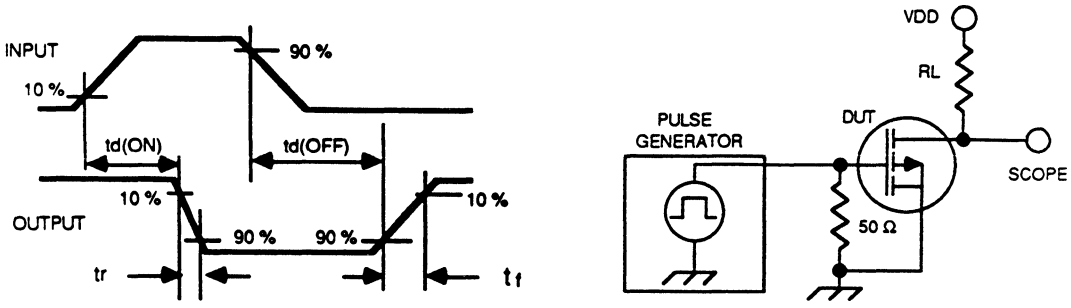


Figure 1. Switching Waveforms and Simplified Test Circuit

Ordering Information

Device	Comcode
LH1162AAP	105461677

8-CHANNEL LOGIC TO HIGH-VOLTAGE LEVEL TRANSLATOR

HT0130P

PRELIMINARY

Description

The HT0130P Level Translator converts V_{DD} referenced logic inputs to V_{PP} referenced outputs ranging from −3 to +300 volts. The HT0130P device can be used to drive the AT&T AP0130NA P-Channel MOSFET array. The device features low power supply drain current under quiescent conditions and provides on-chip ESD protection of inputs. These are features not always present in similar types of arrays currently available from the commercial industry.

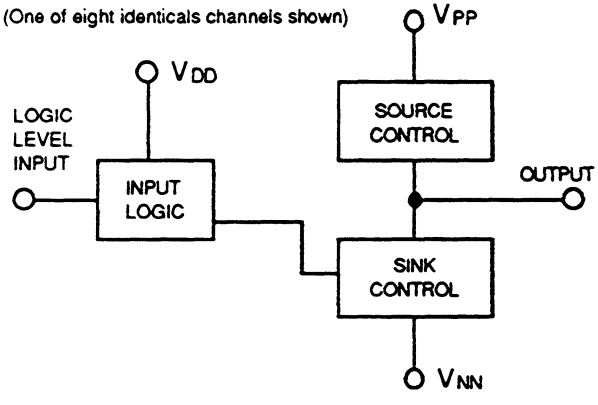
Features

- On-chip ESD protection
- Operating voltage up to 300 V
- Processed with BCDMOS Technology
- Provides logic to high-voltage translation for controlling P-Channel MOS gates
- Accommodates 5 to 5 volts logic inputs
- Accommodates output voltage swings below ground
- Eliminates need for floating logic

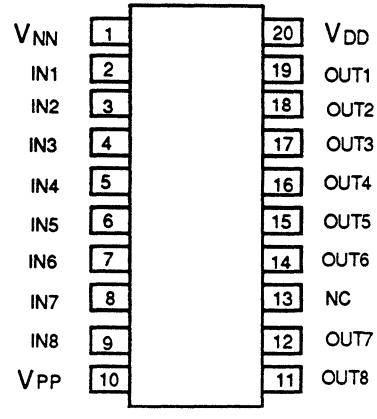
Applications

- Test Systems
- P-Channel MOSFET Control
- Industrial Controls
- Printers/Plotters

Functional Diagram



Pin Diagram



Maximum Ratings (T_A = 25°C unless otherwise specified)	
Ambient Operating Temperature Range	−40 to +85°C
Storage Temperature Range	−55 to +150°C
Pin Soldering Temperature (t = 15 s max.)	300 °C
Output Current per Channel, DC	10 mA
Logic Supply Voltage; (V_{DD})	16 V
Supply Voltage; (V_{PP})	300 V
Negative Supply Voltage (V_{NN})	−16 V

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may adversely affect device reliability.

Recommended Operating Conditions

(T_A = 25°C unless otherwise specified)

Characteristic	Min	Max	Unit
Logic Supply Voltage, V_{DD}	4.5	15	V
Positive High-Voltage Supply, V_{PP}	(V_{NN} + 12)	300	V
Negative Supply Voltage, V_{NN}	−15	0	V
High-Level Input Voltage	(V_{DD} − 1.2)	V_{DD}	V
Low-Level Input Voltage	0	(V_{DD} − 4.2)	V
V_{DD} to V_{NN} Voltage	4.5	25	V

Electrical Characteristics

(T_A = 25°C unless otherwise specified)

Characteristic	Test Condition	Min	Typ	Max	Unit
V_{DD} Supply Current	All Channels Off One Channel On, No Load	— —	— —	1.0 1.0	μA mA
V_{PP} Supply Current	All Channels Off One Channel On, No Load	— —	— —	1.0 0.5	μA mA
V_{NN} Supply Current	All Channels Off One Channel On, No Load	— —	— —	1.0 1.0	μA mA
I_{SOURCE}	V_{DD} = 10 V, V_{NN} = 0 V, V_{IN} = 0 V, Capacitive Load	—	75	—	μA
I_{SINK}	V_{DD} = 10 V, V_{NN} = 0 V, V_{IN} = 10 V, Capacitive Load	—	50	—	μA
V_{ON}		V_{PP} − 17	V_{PP} − 14	V_{PP} − 12.5	V
V_{OFF}		V_{PP} − 0.5	—	—	V
Turn-On Time, Each Channel	Figure 1; V_{DD} = 10 V, V_{NN} = 0	—	5.0	—	μs
Turn-off Time, Each Channel	Figure 1; V_{DD} = 10 V, V_{NN} = 0	—	3.0	—	μs

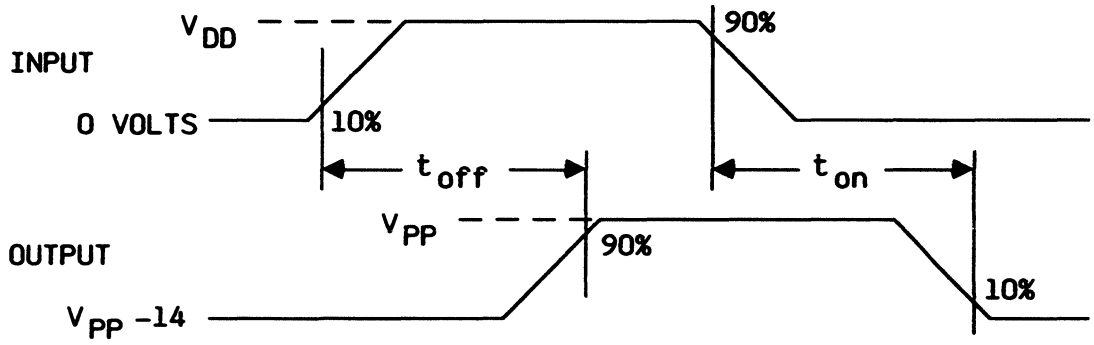


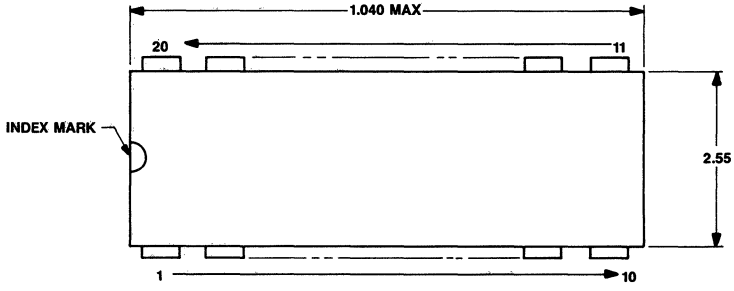
Figure 1. Switching Waveforms

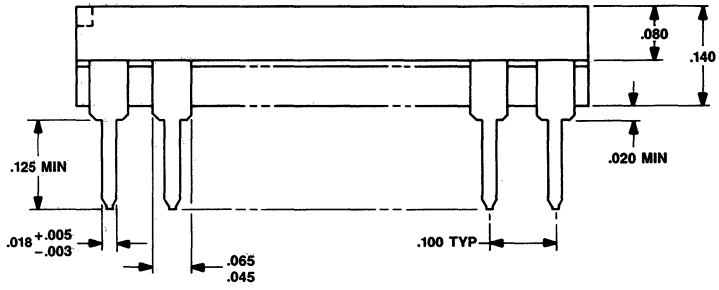
Functional Operation

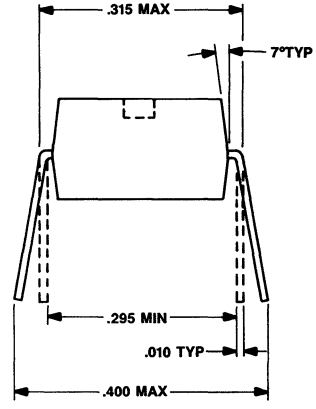
The output will switch from V_{PP} to V_{ON} when the appropriate input is switched from a high-to-low level. The output can swing below ground by connecting the V_{NN} supply to a negative voltage as low as −15 V and using the appropriate V_{PP} supply voltage. In this situation the logic inputs are still referenced to V_{DD}.

Outline Drawing

(Dimensions in Inches)







Ordering Information

Device	Comcode
HT0130P	104432588

Description

The ALA201/202 UHF Linear Arrays are semi-custom integrated circuits consisting of vertical NPN and PNP transistors, capacitors, and ion-implanted resistors. Designed on a regular grid system, the array provides easy interconnector for the designer. The ALA201/202 UHF Linear Arrays are fabricated in a complementary bipolar integrated circuit (CBIC) process that offers the advantages of similar NPN and PNP transistor characteristics at very high speeds. Typical f_T of 4.5 GHz for the NPN and 3.75 GHz for the PNP transistors (V_{CE} = 6 volts and I_C = 3 mA) with high current drive capability (9 mA for the NPN and PNP 1X transistors) is unique to these linear arrays.

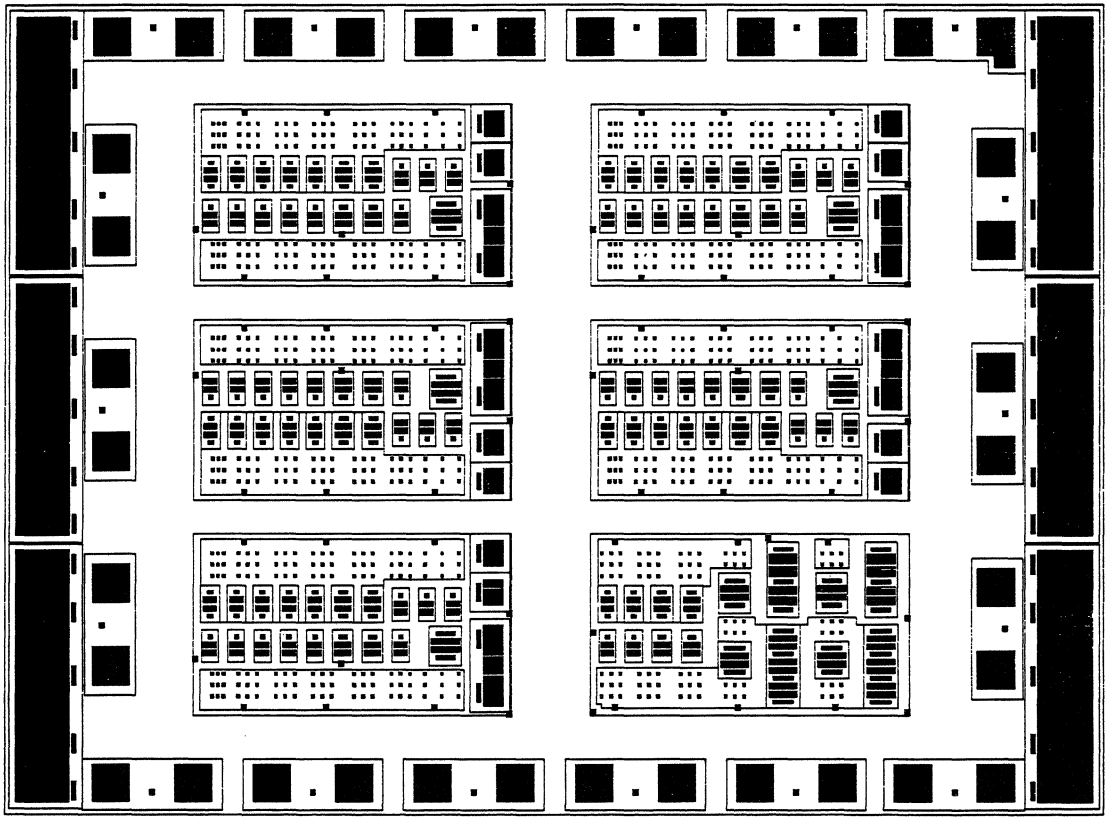
Dual-layer metal and thick metal are typically used for most applications; however, singie-layer metal may be used upon special request. The bottom and top metal layers have a low sheet resistance of about 0.03 ohm/sq. and a current capacity of 2 mA/micron of metal width. The standard 6 μm bottom and 10 μm top metal linewidths are capable of carrying a maximum of 12 mA and 20 mA dc current, respectively. For cases where high-current must be carried, a thicker gold layer called "thick metal" is available with a sheet resistance of about 0.004 ohms/sq. and a current capacity of 14 mA/micron of metal width. The ALA201 device is divided into 6 modules consisting of 5 standard and 1 power module. The ALA202 device is divided into 12 modules consisting of 9 standard, 2 power, and 1 input module. All modules are symmetrically located within the array for ease of layout. Because the modules are on a regular grid system, the user interconnects components by drawing lines on a clearly defined grid marked on a layout sheet.

For more detailed information regarding ordering procedures, design kits, and packaging for the ALA201/202 UHF Linear Arrays, refer to the Semi-Custom Linear Array brochure.

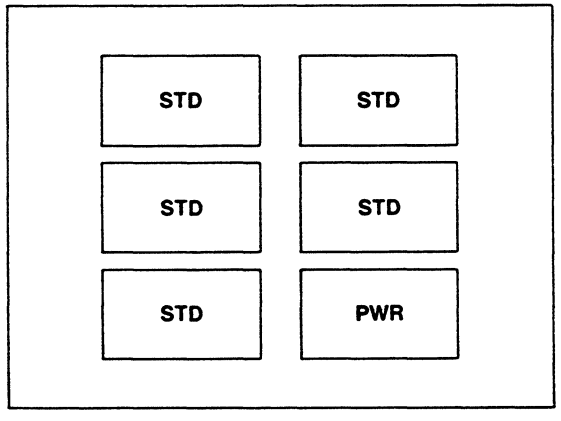
Features

- Quick design turnaround
- Custom circuitry at low cost
- High performance
- High probability of success
- High reliability

Figure 1. ALA201 UHF Linear Array

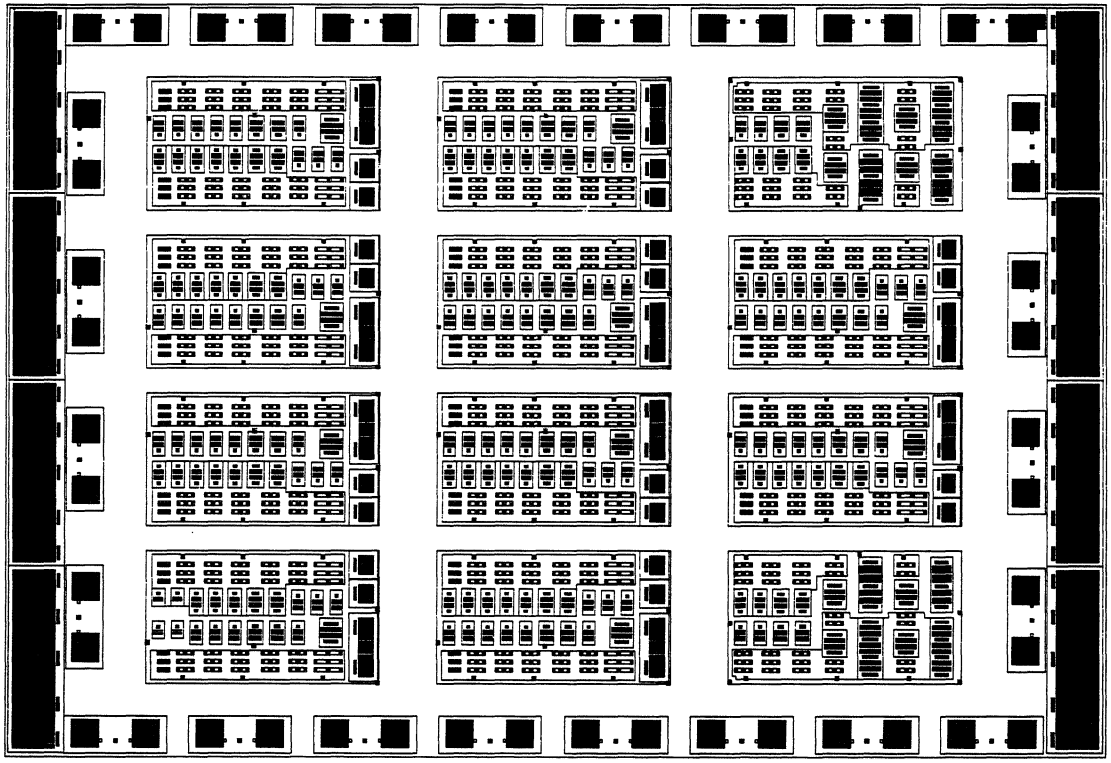


(a) Module Layout

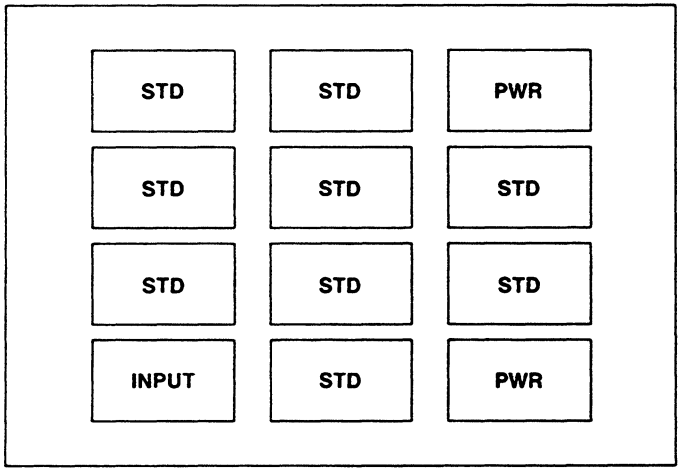


(b) Location of Tiles on Chip

Figure 2. ALA202 UHF Linear Array



(a) Module Layout



(b) Location of Tiles on Chip

Electrical Characteristics

(T_A = 250°c unless otherwise specified)

NPN dc Parameters

Symbol	Measurement/Condition	Min	Typ	Max	Unit
h_{FE}*	I_C = 1 mA, V_{CE} = 2 V	80	110	—	—
f_T	I_C = 1 mA, V_{CE} = 2 V	—	3.5	—	GHz
V_A (early voltage)	I_C = 1 mA, V_{CE} = 2, 4 V	20	40	—	V
V_{CE} (sat)	I_C = 1 mA, I_B = 100 μA	—	.13	.35	V
V_{BE}**	I_E = 1 mA, V_{CE} = 2 V	.700	.775	.900	V
BV_{CEX}	I_C = 100 μA, I_B = .1 nA	12	18	—	V
I_{EBO}	V_{EB} = 2 V	—	.02	1	μA
BV_{CSO} (collector substrate breakdown)	I_C = 1 μA	20	60	—	V
I_{CES}	V_{CE} = 5 V	—	1	—	nA
I_{CBO}	V_{CB} = 10 V, I_E = 0	—	1	—	nA
BV_{EBO}	I_E = 10 μA	4.7	5.3	5.9	V

PNP dc Parameters

Symbol	Measurement/Condition	Min	Typ	Max	Unit
h_{FE}*	I_C = 1 mA, V_{CE} = 2 V	25	40	—	—
f_T	I_C = 1 mA, V_{CE} = 2 V	—	2.5	—	GHz
V_A (early voltage)	I_C = 1 mA, V_{CE} = 2, 4 V	8	11	—	V
V_{CE} (sat)	I_C = 1 mA, I_B = 100 μA	—	.13	.35	V
V_{BE}**	I_E = 1 mA, V_{CE} = 2 V	.700	.780	.900	V
BV_{CEX}	I_C = 100 μA, I_B = .1 nA	11	14	—	V
I_{EBO}	V_{EB} = 2 V	—	.01	1	μA
BV_{CSO} (collector substrate breakdown	I_C = 1 μA	20	40	—	V
I_{CES}	V_{CE} = 5 V	—	1	—	nA
I_{CBO}	V_{CB} = 10 V, I_E = 0	—	1	—	nA
BV_{EBO}	I_E = 10 μA	5.0	5.4	6.7	V

* h_{FE} matching of adjacent transistors of the same type is within ±5%.

** V_{BE} matching of adjacent transistors of the same type is within ±1.5 mV.

Resistor Data (ALA201)

(T_A = 25°C)

Value (Ω)	Tol (%)	Type	TCR PPM/°C	Total
50	±20	BI*	+1300	40
100	±20	BI*	+1300	240
200	±20	BI*	+1300	40
1000	±20	BI**	+1100	20
2000	±20	BI**	+1100	120
4000	±20	BI**	+1100	20

Capacitor Data (ALA201)

Type	Cap (pF)	Tol (%)	Total
Programmable	0.75 to 3.35	±20	5
Fixed	1.0	±20	10
Programmable	1.0 to 32	±20	6

Component Totals (ALA201)

Component	Type	Total	Standard	Power
Transistors				
NPN	1X	47	9	2
NPN	2X	12	2	2
NPN	5X	7	1	2
NPN	15X	2	—	2
PNP	1X	27	5	2
PNP	2X	12	2	2
PNP	5X	2	—	2
PNP	15X	2	—	2
Resistors*	50 Ω	40	8	—
	100 Ω	240	40	40
	200 Ω	40	8	—
Resistors**	1000 Ω	20	4	—
	2000 Ω	120	20	20
	4000 Ω	20	4	—
Capacitors	0.75 to 3.35 pF	5	1	—
	1.0 pF	10	2	—
	1.0 to 32 pF†	6	—	—
Bonding Pads	—	36	—	—

* Denotes a 50 ohm/sq. implanted boron resistor.
** Denotes a 1080 ohm/sq. implanted boron resistor.
† These capacitors are located on the border of the overall die.

Note: Matching of adjacent resistors of similar type is within ±1%.

Resistor Data (ALA202)

(T_A = 25°C)

Value (Ω)	Tol (%)	Type	TCR PPM/°C	Total
50	±20	BI*	+1300	80
100	±20	BI*	+1300	480
200	±20	BI*	+1300	80
1000	±20	BI**	+1100	40
2000	±20	BI**	+1100	240
4000	±20	BI**	+1100	40

Capacitor Data (ALA202)

Type	Cap (pF)	Tol (%)	Total
Programmable	0.75 to 3.35	±20	10
Fixed	1.0	±20	20
Programmable	1.0 to 32	±20	8

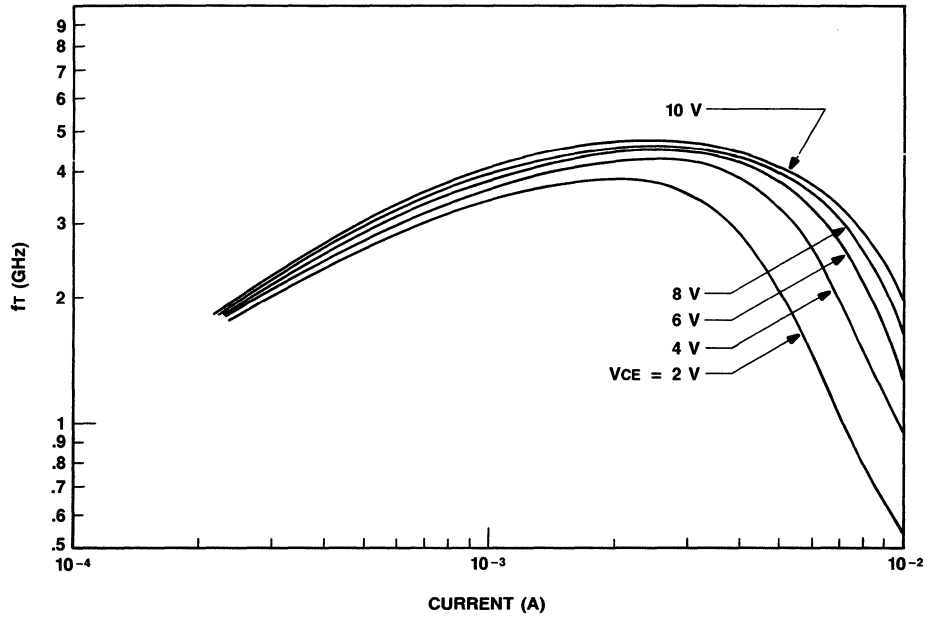
Component Totals (ALA202)

Component	Type	Total	Standard	Input	Power
Transistors					
NPN	1/3X	2	—	2	—
NPN	1X	92	9	7	2
NPN	2X	24	2	2	2
NPN	5X	14	1	1	2
NPN	15X	4	—	—	2
PNP	1/3X	2	—	2	—
PNP	1X	52	5	3	2
PNP	2X	24	2	2	2
PNP	5X	4	—	—	2
PNP	15X	4	—	—	2
Resistors*	50 Ω	80	8	8	—
	100 Ω	480	40	40	40
	200 Ω	80	8	8	—
Resistors**	1000 Ω	40	4	4	—
	2000 Ω	240	20	20	20
	4000 Ω	40	4	4	—
Capacitors	0.75 to 3.35 pF	10	1	1	—
	1.0 pF	20	2	2	—
	1.0 to 32 pF†	8	—	—	—
Bonding Pads	—	48	—	—	—

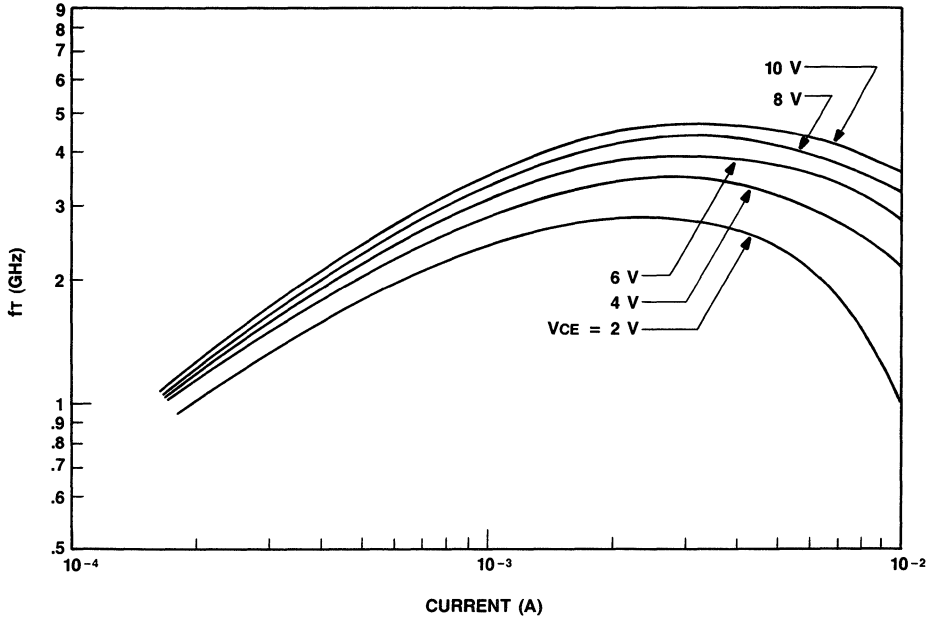
* Denotes a 50 ohm/sq. implanted boron resistor.
** Denotes a 1080 ohm/sq. implanted boron resistor.
† These capacitors are located on the border of the overall die.

Note: Matching of adjacent resistors of similar type is within ±1%.

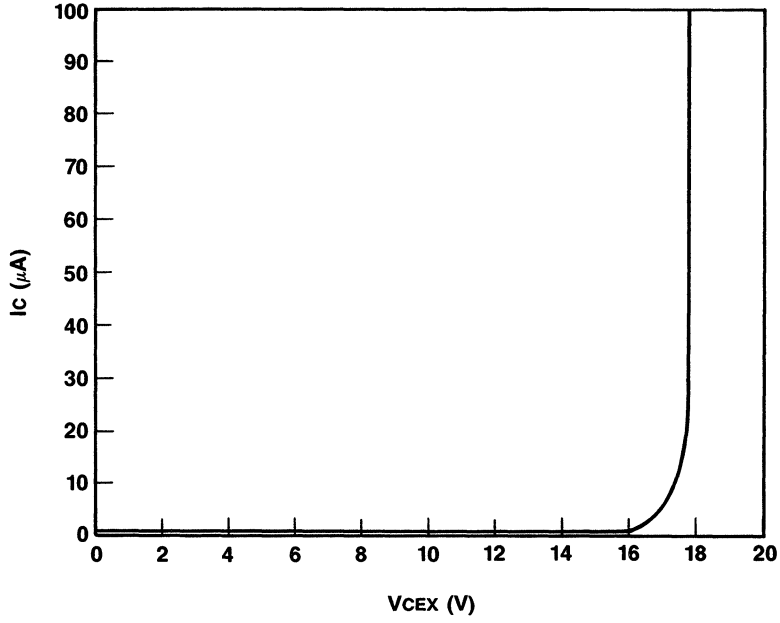
Frequency vs. Current (Typical NPN 1X)



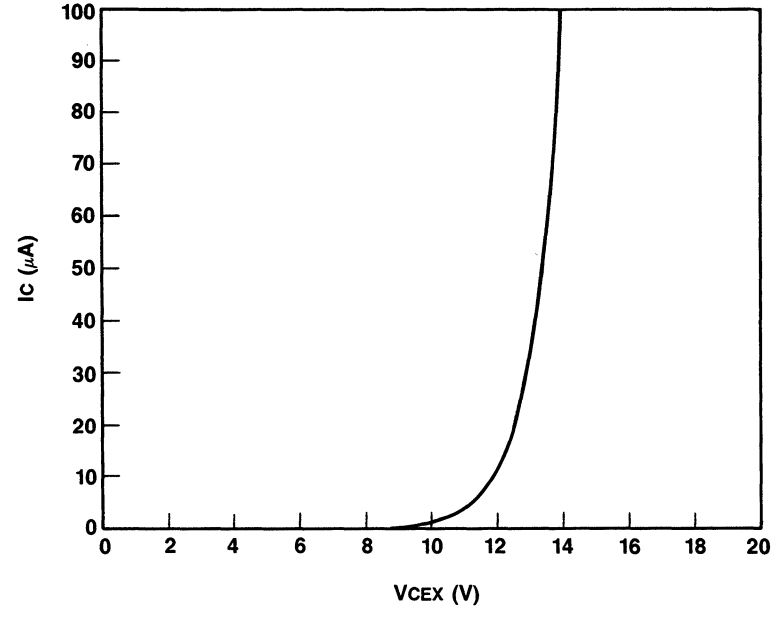
Frequency vs. Current (Typical PNP 1X)



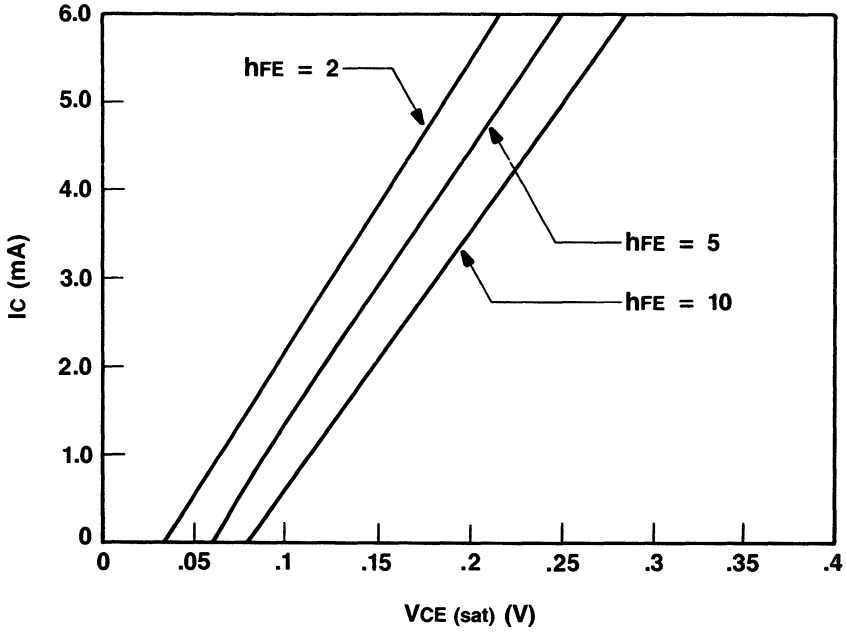
Current vs. Breakdown Voltage (NPN 1X)



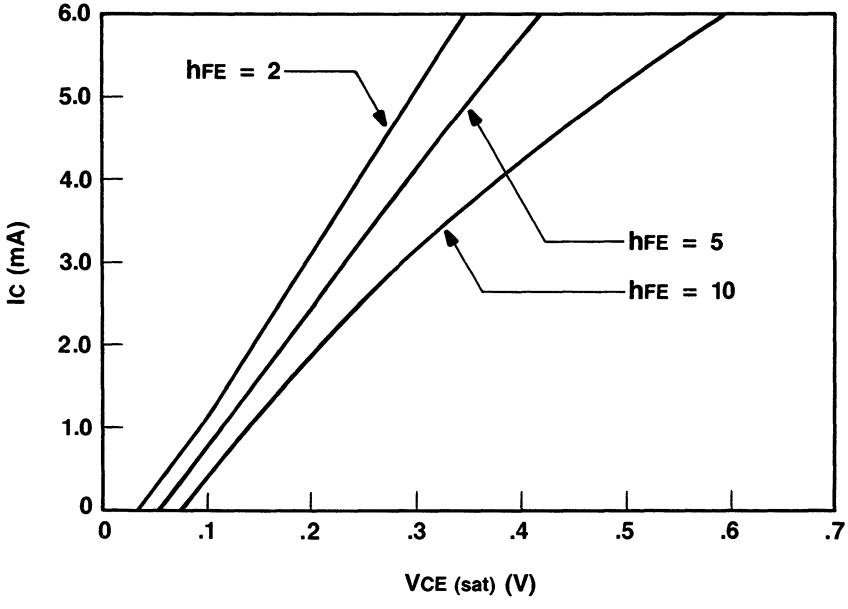
Current vs. Breakdown Voltage (PNP 1X)



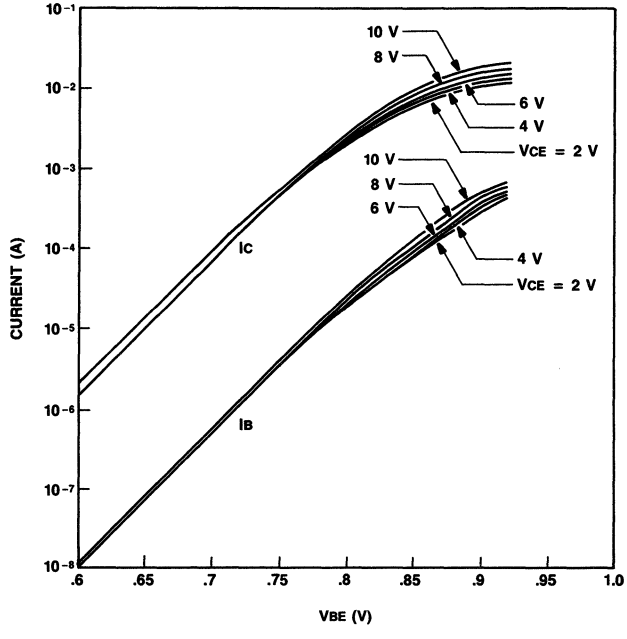
Current vs. Saturation Voltage (NPN)



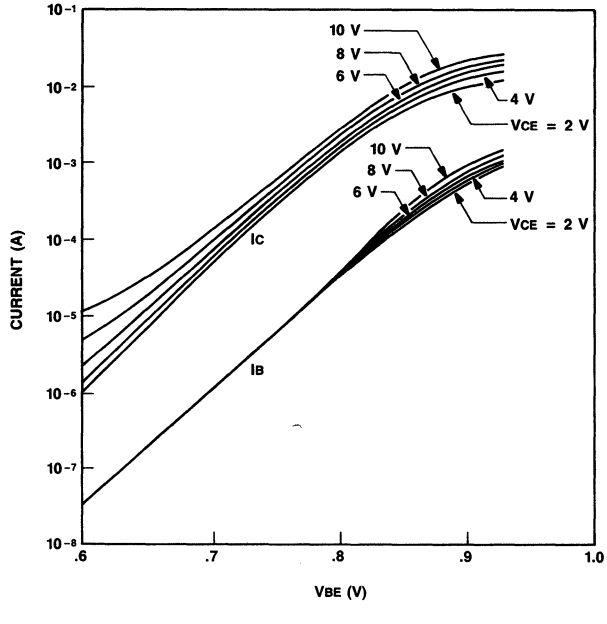
Current vs. Saturation Voltage (PNP)



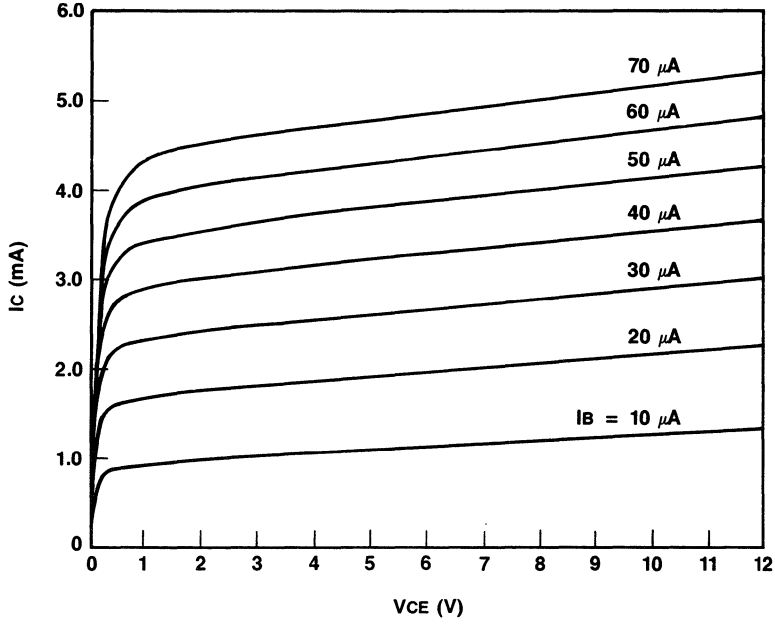
Current vs. Voltage Characteristics (NPN 1X)



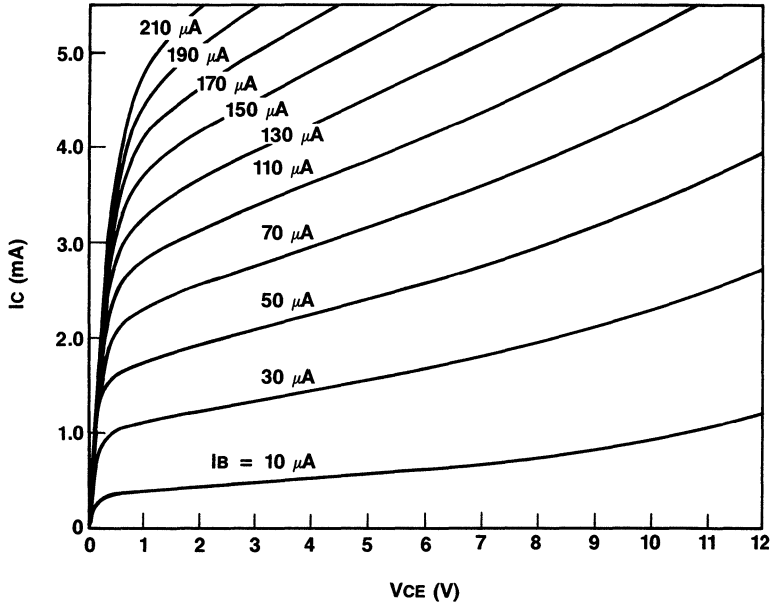
Current vs. Voltage Characteristics (PNP 1X)



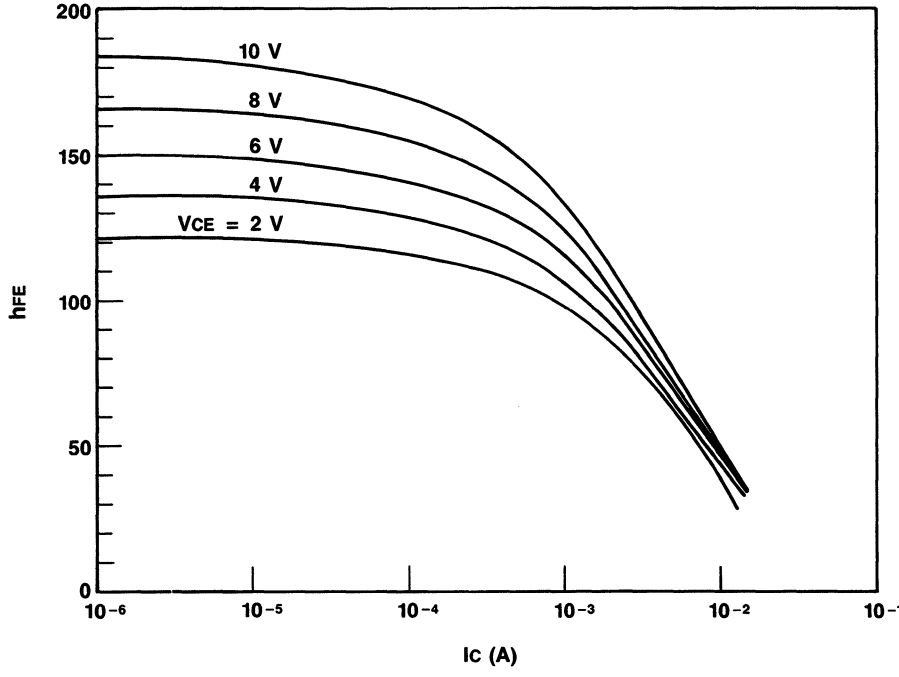
Output Voltage Characteristics (NPN 1X)



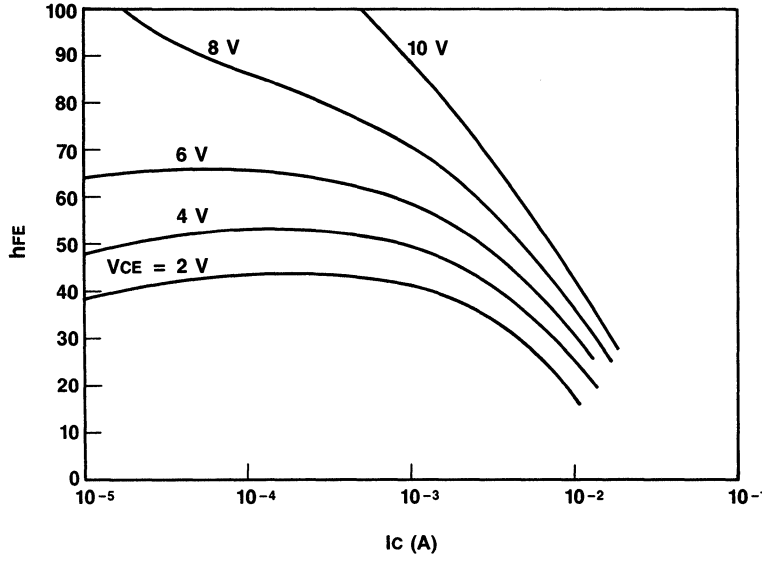
Output Voltage Characteristics (PNP 1X)



Current Gain Characteristics (NPN 1X)



Current Gain Characteristics (PNP 1X)



Description

The ALA300/301 Linear Arrays provide design engineers the means to obtain 90 volt semi-custom integrated circuits. The single-module array (ALA300) consists of 13 vertical NPN and 15 vertical PNP transistors, three 6 pF capacitors, and 1k diffused and 10k ion-implanted resistor banks. The quad-module array (ALA301) is identical to the single-module array (ALA300), but has four times the number of components.

These linear arrays are fabricated using the complementary bipolar integrated circuit (CBIC) process that offers the advantages of vertical NPN and PNP transistors. CBIC technology offers the advantage of designing high-performance circuits with less design complexity. A minimum collector-to-emitter reverse breakdown voltage of 90 volts is guaranteed for both transistors. Typical peak f_T of 350 MHz for NPN and 300 MHz for PNP transistors and 5 mA current drive capability for the minimum area transistors are unique for these linear arrays.

Two-level metal is used for interconnections. Upon request, a thick-metal interconnect is also available to provide higher current capacity. The top and bottom metal layers have a low sheet resistance of < 0.03 ohms/sq. and < 1.0 ohms/sq. with a current capacity of 2.0 mA/micron and 60 μA/micron of metal width, respectively. The thicker metal interconnect has a sheet resistance of < 0.003 ohms/sq. and a current capacity of 20 mA/micron of metal width.

For more detailed information regarding ordering procedures, design kits, and packaging of the ALA300/301 devices, refer to the Semi-Custom Linear Array brochure.

Features

- High-frequency performance, typical f_T of 350 MHz for NPN and 300 MHz for PNP transistors
- 90 volt capability
- Low development costs
- Quick design turn-around, typically six to eight weeks from design approval
- Complementary vertical NPN and PNP transistors
- 2-level metal interconnect
- 1k and 10k resistor banks
- All I/O ESD protected
- Available in chip form and a variety of standard packages

Figure 1. ALA300 High-Voltage Linear Array

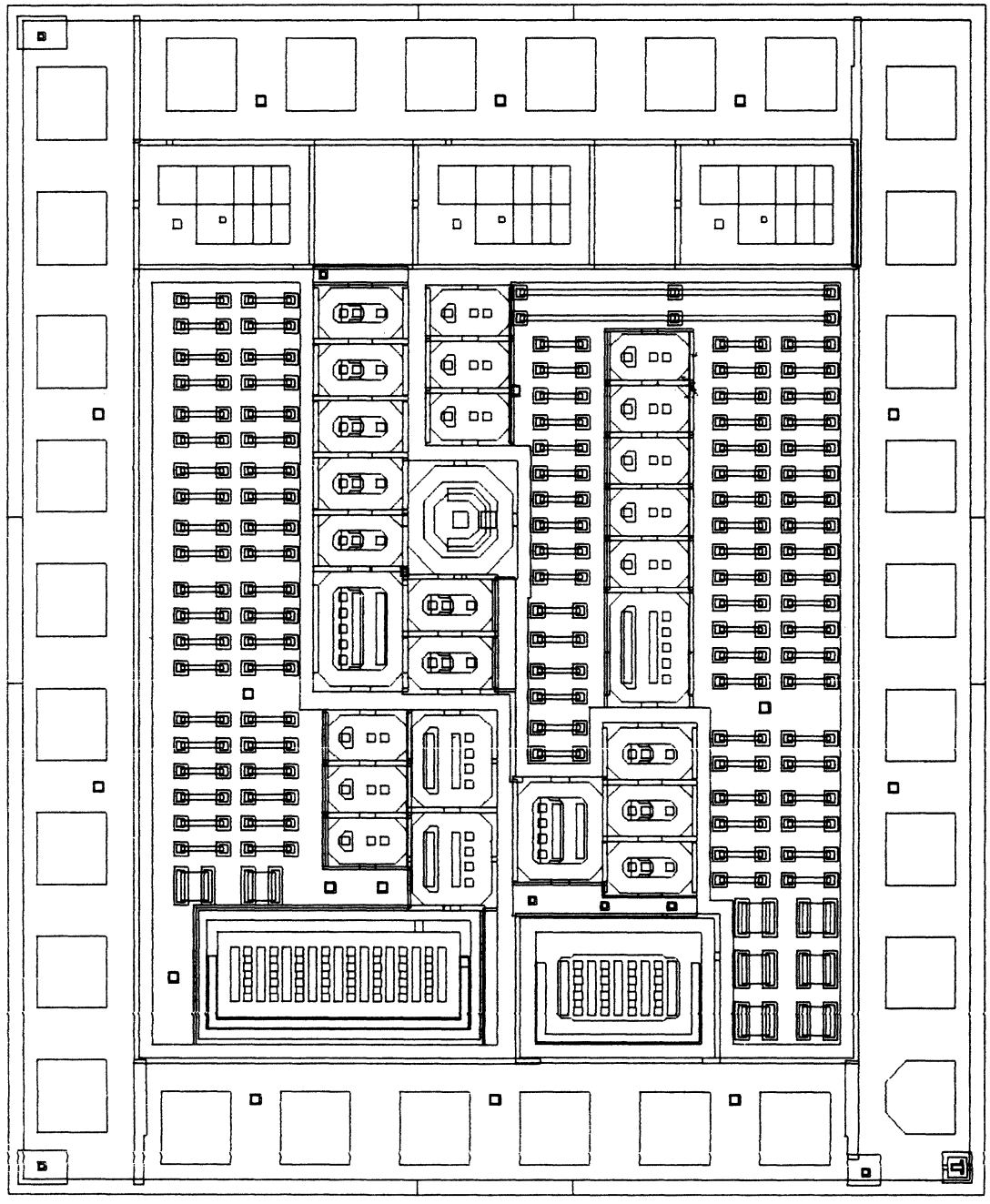


Figure 2. ALA301 High-Voltage Linear Array

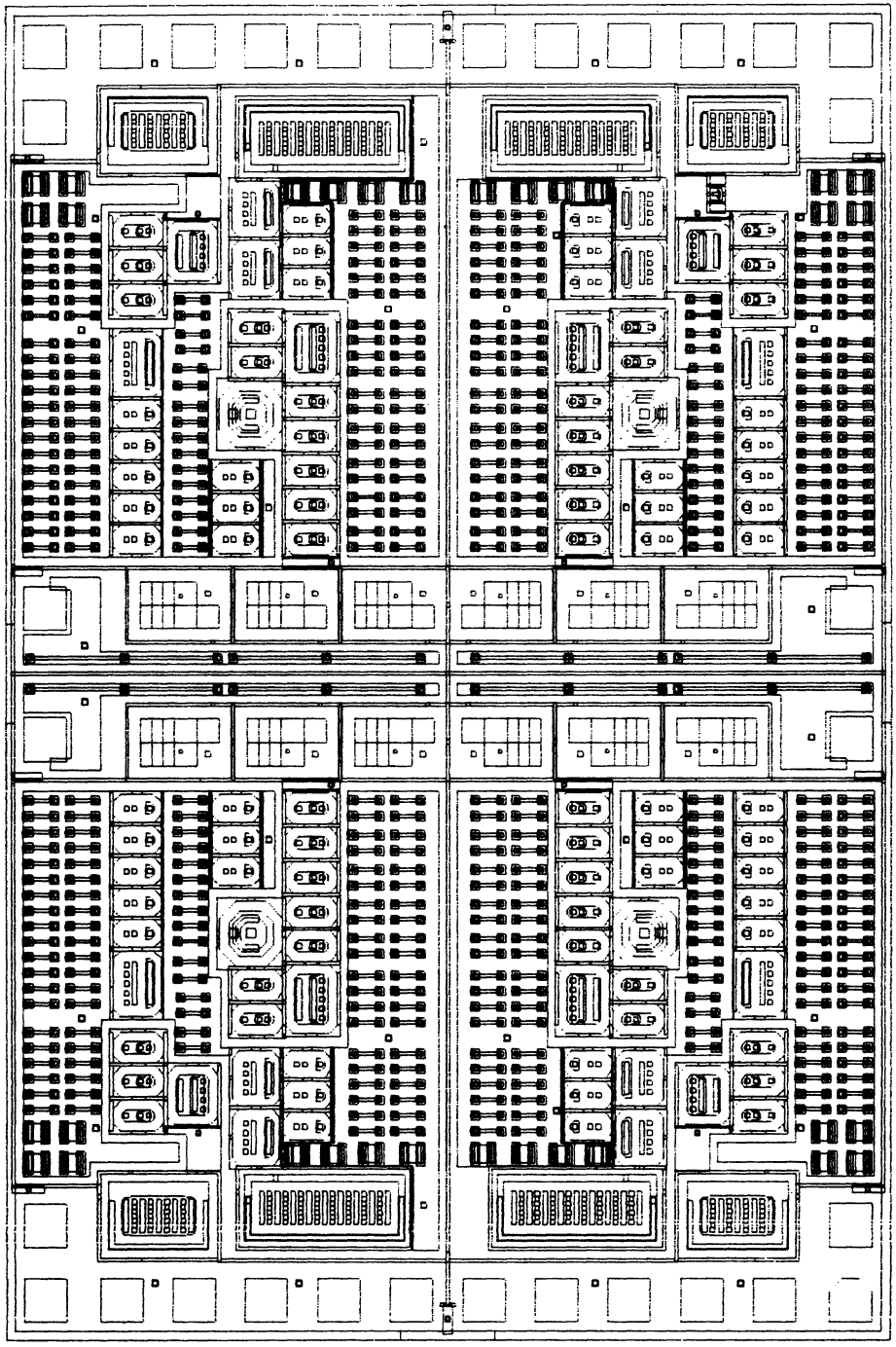
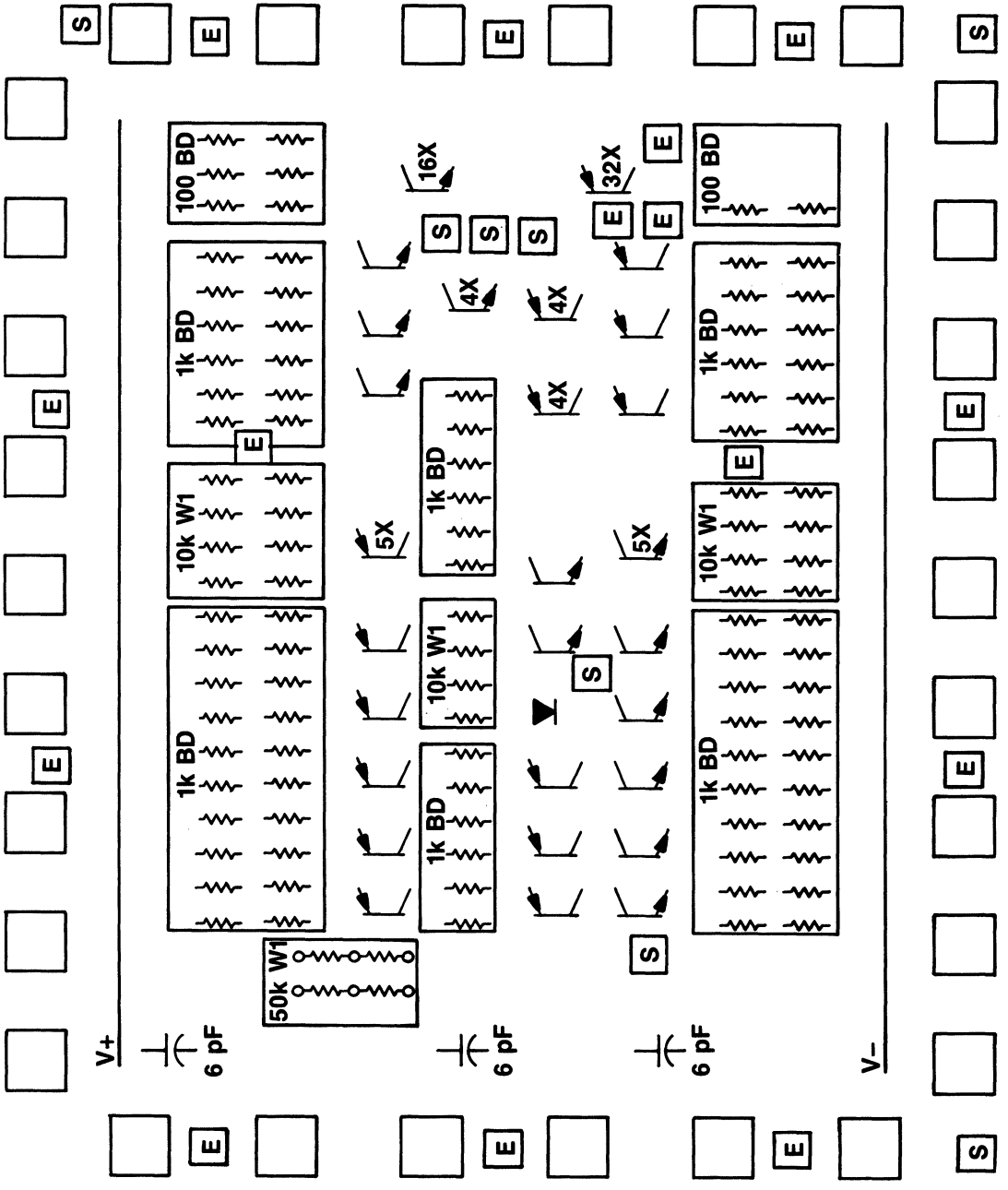


Figure 3. Schematic of ALA300 Components



Electrical Characteristics

NPN

(T_A = 25°C unless otherwise specified)

Symbol	Measurement Condition	Min	Typ	Max	Unit
h_{FE}	I_C = 1 mA, V_{CE} = 3 V	50	110	—	—
f_T	I_C = 500 μA, V_{CE} = 10 V	—	350	—	MHz
V_A (early voltage)	I_C = 100 μA, V_{CE} = +5 V	40	100	—	V
V_{CE} (sat)	I_C = 1 mA, I_B = 500 μA	—	100	150	mV
V_{BE}	I_E = 1 mA, V_{CE} = 3 V	750	830	900	mV
BV_{CEO}	I_C = 1 mA	90	110	—	V
BV_{EBO}	I_E = 10 μA	7.5	8.0	9.5	V
BV (collector substrate breakdown)	I_C = 1 mA	190	200	—	V
I_{CEO}	V_{CE} = 80 V, I_B = 0	—	50	150	nA
I_{CBO}	V_{CB} = 80 V, I_E = 0	—	2	3	nA

PNP

(T_A = 25°C unless otherwise specified)

Symbol	Measurement Condition	Min	Typ	Max	Unit
h_{FE}	I_C = 1 mA, V_{CE} = 3 V	40	80	—	—
f_T	I_C = 500 μA, V_{CE} = 10 V	—	300	—	MHz
V_A (early voltage)	I_{CB} = 100 μA, V_{CE} = −5 V	40	125	—	V
V_{CE} (sat)	I_C = −1 mA, I_B = −500 μA	—	200	300	mV
V_{BE}	I_E = 1 mA, V_{CE} = −3 V	750	830	900	mV
BV_{CEO}	I_C = −1 mA	90	115	—	V
BV_{EBO}	I_E = −10 μA	8.0	8.5	9.2	V
BV (collector substrate breakdown)	I_C = −1 mA	90	100	250	V
I_{CEO}	V_{CE} = −80 V, I_B = 0	—	100	250	nA
I_{CBO}	V_{CB} = −80 V, I_E = 0	—	2	4	nA

Resistor Data

(T_A = 25°C unless otherwise specified)

Value (Ω)	TOL (%)	Type *	TCR PPM/°C	ALA300	ALA301
100	±20	BD	1670	8	32
1k	±20	BD	1670	76	304
10k	±20	W1	1610	20	80
50k	±20	W1	1610	4	16

* BD denotes a 200 Ω/sq. diffused boron resistor
W1 denotes a 2000 Ω/sq. implanted boron resistor

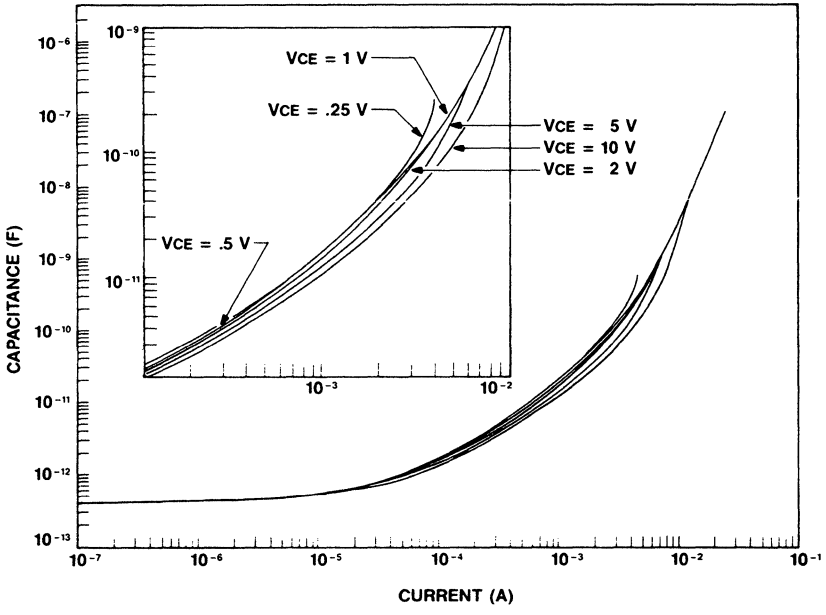
Capacitor Data

Value (pF)	TOL (%)	Type	ALA300	ALA301
6	±30	Fixed MOS	3	12

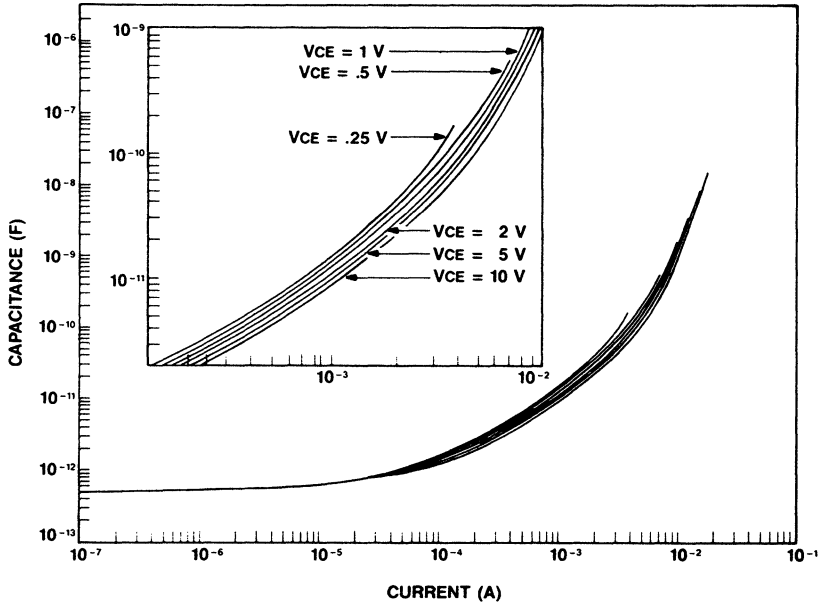
Component Totals

Component Type	ALA300	ALA301
NPN	13	52
PNP	15	60
Resistors	108	432
Capacitors	3	12
Diodes	1	4
Bonding Pads	30	32

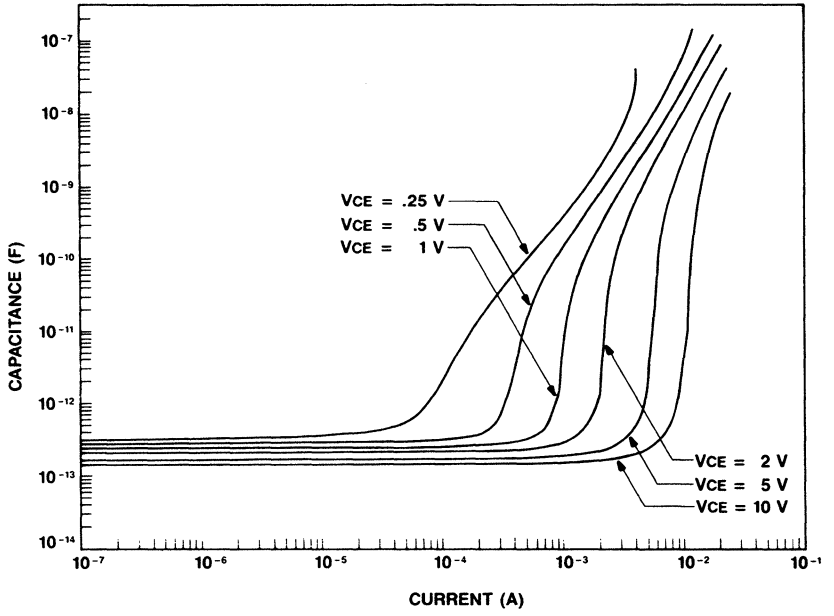
Base-Emitter Capacitance (NPN)



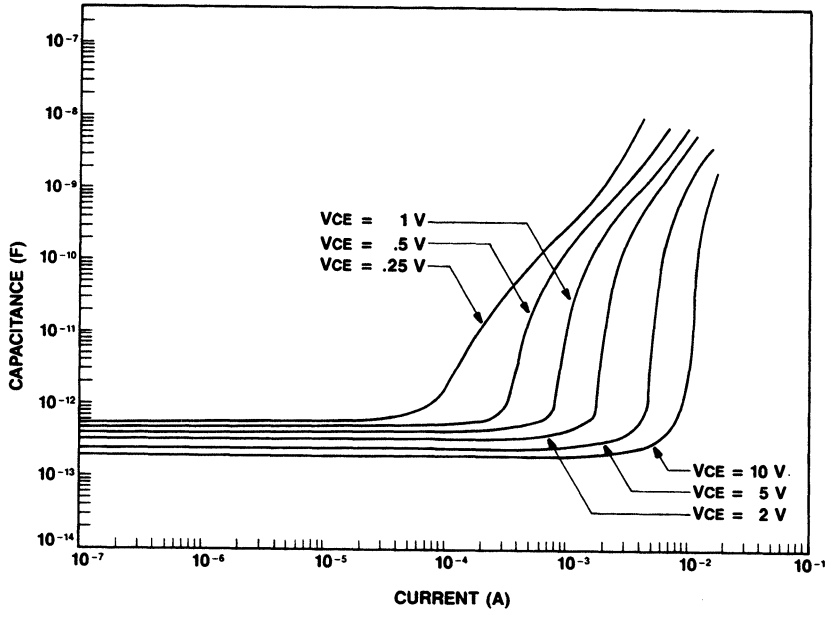
Base-Emitter Capacitance (PNP)



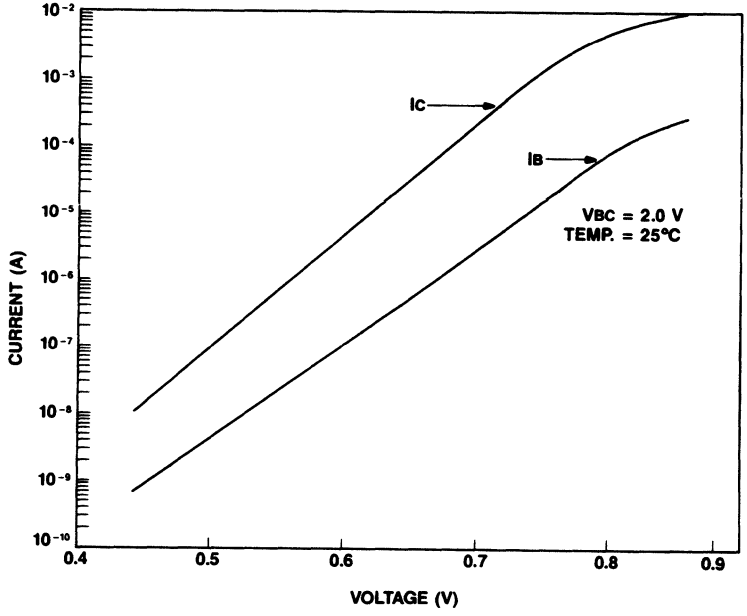
Collector-Base Capacitance (NPN)



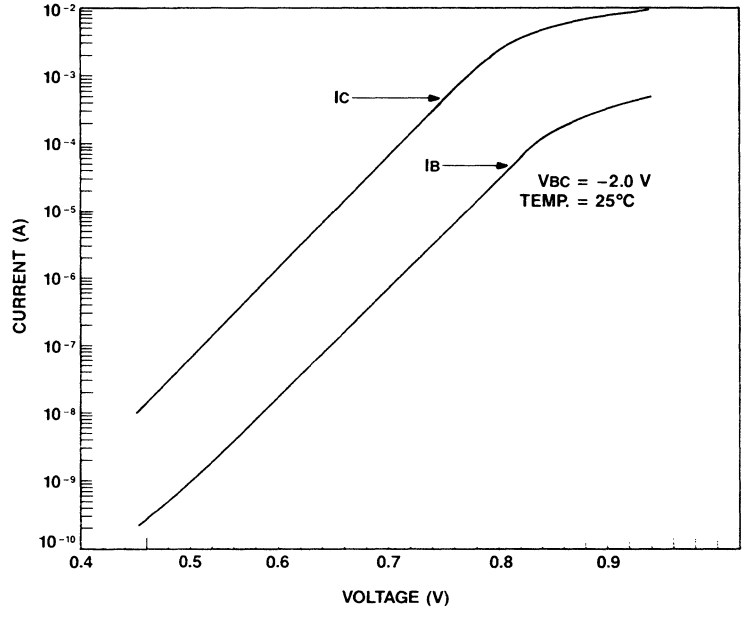
Collector-Base Capacitance (PNP)



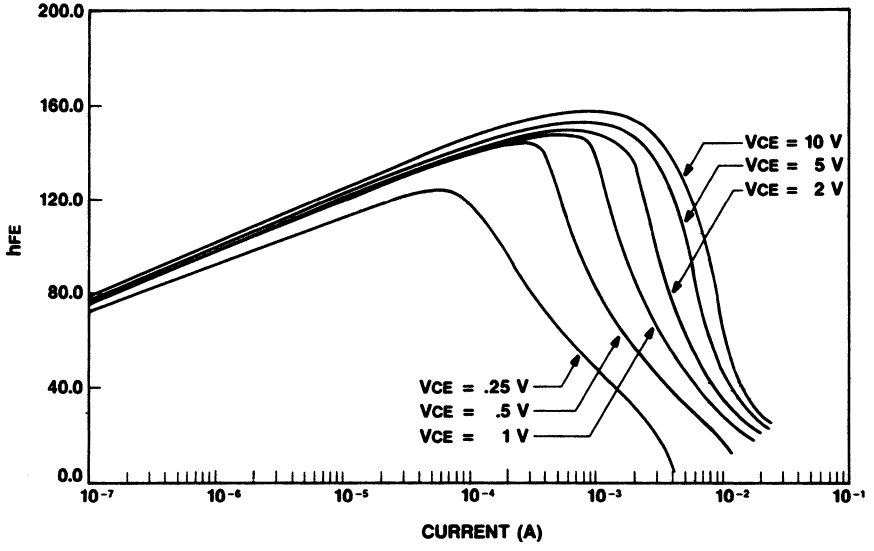
Current-Voltage Characteristics (NPN)



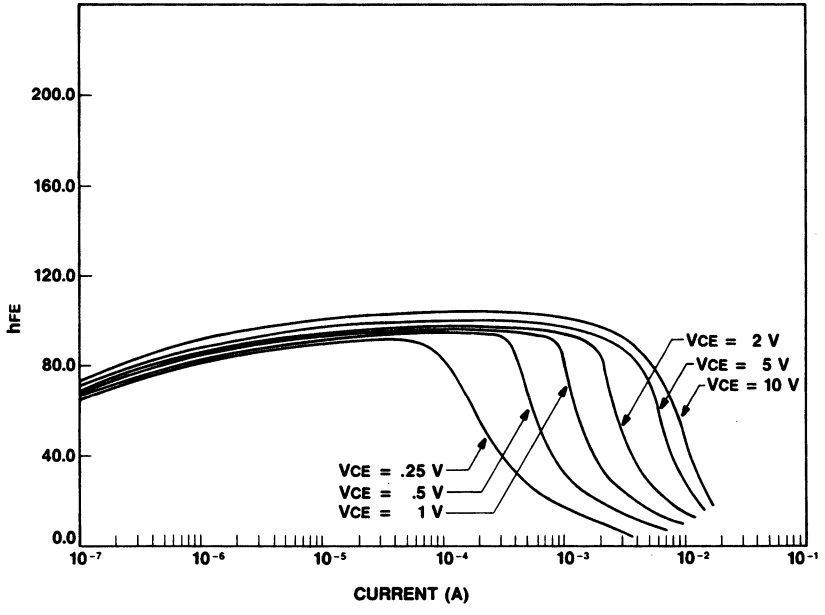
Current-Voltage Characteristics (PNP)



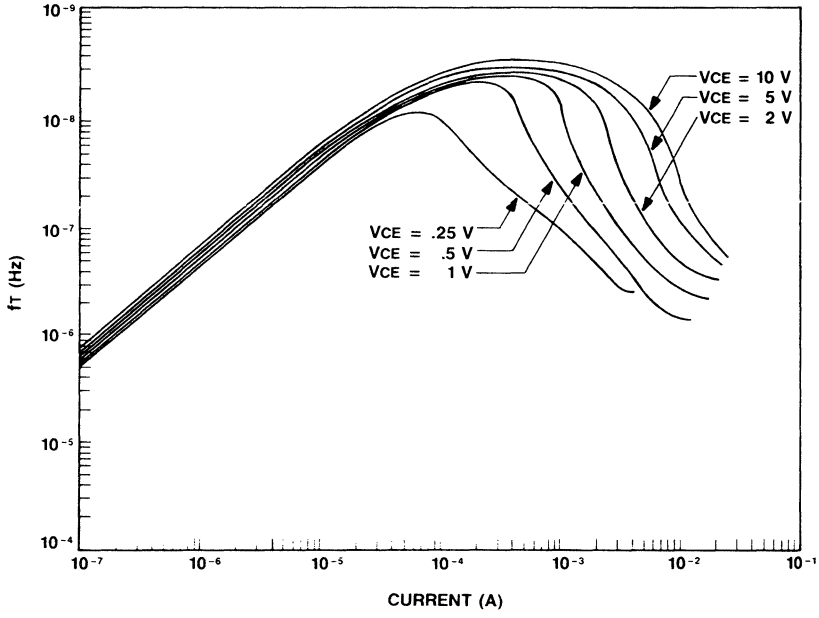
Current Gain (NPN)



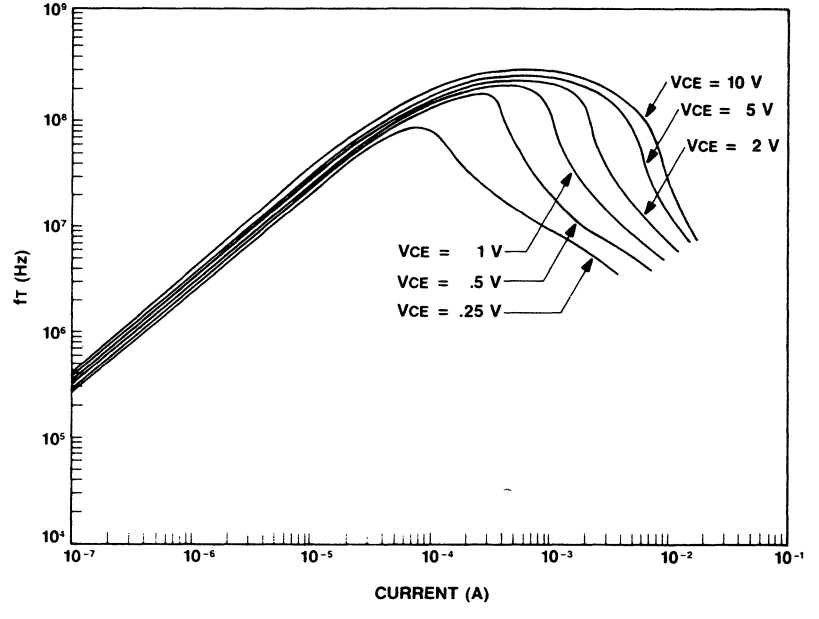
Current Gain (PNP)



Unity Gain Frequency (NPN)



Unity Gain Frequency (PNP)



Description

The ALA400/401 Linear Array Family is fabricated using the complementary bipolar integrated circuit (CBIC) process that offers the advantages of vertical NPN and vertical PNP transistors. CBIC technology offers the advantage of designing high-performance circuits with less design complexity. A minimum collector-to-emitter reverse break-down voltage of 33 volts is guaranteed for both transistors.

Typical peak f_T of 350 MHz for NPN and 300 MHz for PNP transistors and 2 mA current drive capability for the 1 X transistors are unique for these linear arrays. Current drive capability for the other on-chip transistors is linear, e.g., 2 X = 4 mA, 3 X = 6 mA, etc. Pinch-off voltage for JFETs is 1 to 2 volts. I_{DSS} is about 1.0 mA.

The ALA400 Linear Array is divided into 16 modules, consisting of 12 standard, 2 power, and 2 JFET modules. The ALA401 Linear Array is divided into 9 modules, consisting of 7 standard and 2 power modules. All modules are symmetrically located within the array for ease of design layout. Because the modules are on a regular grid system, the user interconnects components by drawing lines on a clearly defined grid, marked on a layout sheet.

Two-level metal is used for interconnections. Upon request, a thick-metal interconnect is also available to provide higher current capacity. The top metal layer has a low sheet resistance of $< 0.03\ \Omega$/sq. and a current capacity of 2.0 mA/micron metal width. The bottom metal layer has a sheet resistance of $< 1.0\ \Omega$/sq. and a current capacity of 200 μA/micron of metal width. The thicker metal interconnect has a sheet resistance of $< 0.003\ \Omega$/sq. and a current capacity of 20 mA/micron of metal width.

For more detailed information regarding ordering procedures, design kits, and packaging of the ALA400/401 devices, refer to the Semi-Custom Linear Array brochure.

Benefits

- High-frequency performance, typical f_T of 350 MHz for NPN and 300 MHz for PNP transistors
- 33 volt capability
- Low development costs
- Quick design turnaround, typically six to eight weeks from design approval

Features

- Complementary vertical NPN and PNP transistors
- Two-level metal interconnect
- All I/O ESD protected

Figure 1. ALA400 Module Layout

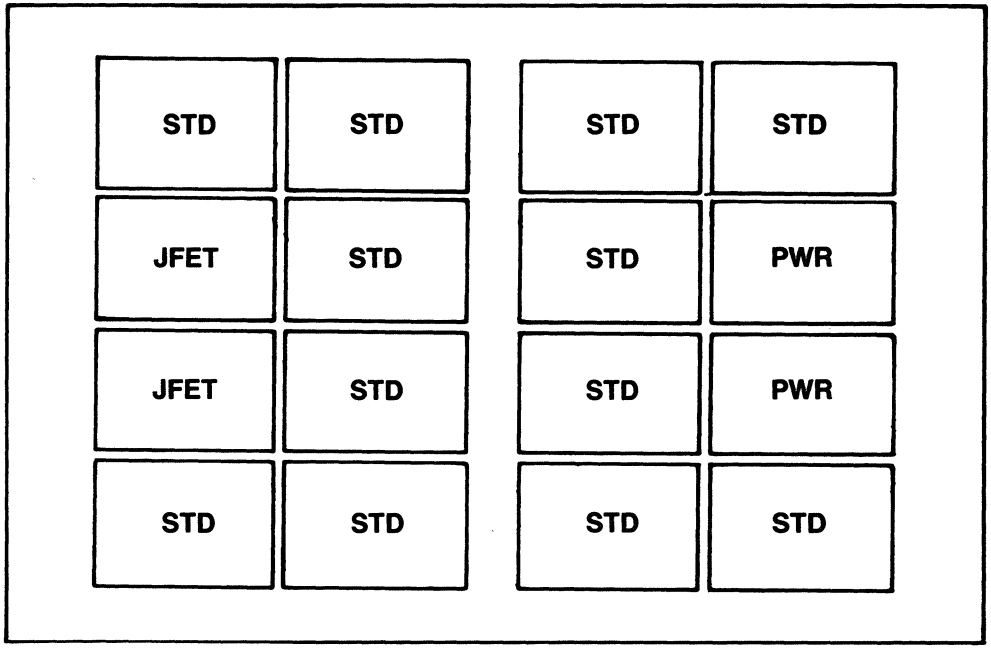
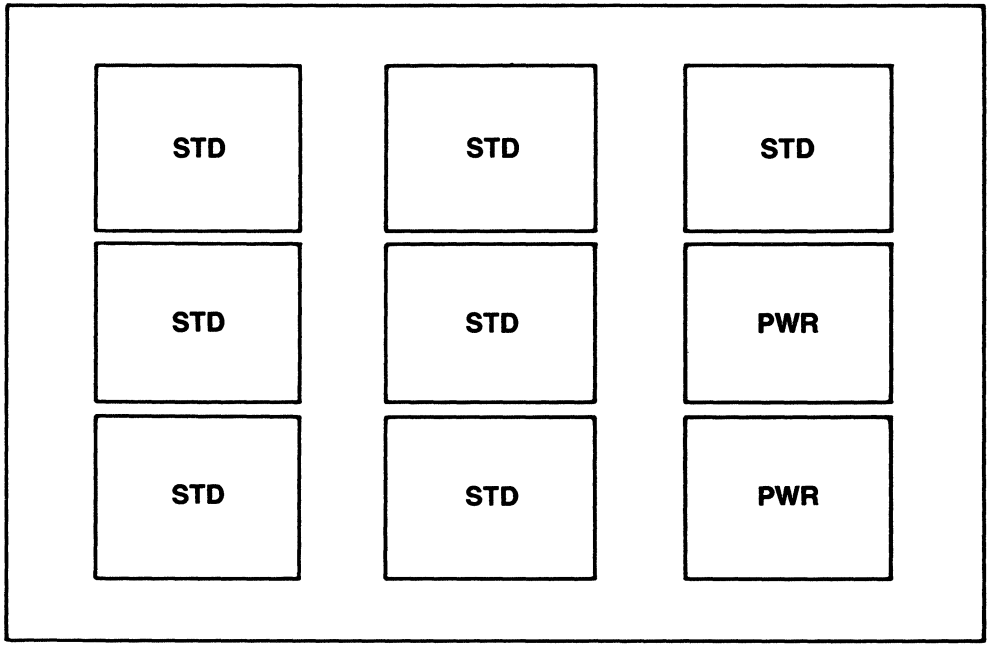


Figure 2. ALA401 Module Layout



Electrical Characteristics

T_A = 25°C

NPN1X Transistor

Symbol	Measurement Condition	Min	Typ	Max	Unit
h_{FE}*	I_C = 1 mA, V_{CE} = 2.5 V	40	85	250	—
I_C	80% of peak h_{FE}	—	2	—	mA
BV_{CEO}	I_C = 1 mA	33	38	—	V
BV_{CBO}	I_C = 10 μA	33	50	—	V
BV_{EBO}	I_C = 10 μA	7.7	8.2	8.7	V
V_{BE}**	I_E = 100 μA	—	743	—	mV
R_{sat}	h_{FE} = 2	—	37	—	Ω
V_{CE} (sat)	I_C = 1 mA, h_{FE} = 2	—	70	150	mV
V_A (early voltage)	I_C = 500 μA	60	225	—	V
f_T	V_{CE} = 10 V	—	350	—	MHz

PNP1X Transistor

Symbol	Measurement Condition	Min	Typ	Max	Unit
h_{FE}*	I_C = 1 mA, V_{CE} = 2.5 V	40	110	250	—
I_C	80% of peak h_{FE}	—	.800	—	mA
BV_{CEO}	I_C = 1 mA	33	47	—	V
BV_{CBO}	I_C = 10 μA	33	48	—	V
BV_{EBO}	I_C = 10 μA	7.7	8.2	8.7	V
V_{BE}**	I_E = 100 μA	—	748	—	mV
R_{sat}	h_{FE} = 2	—	127	—	Ω
V_{CE} (sat)	I_C = 1 mA, h_{FE} = 2	—	140	250	mV
V_A (early voltage)	I_C = 500 μA	45	60	—	V
f_T	V_{CE} = 10 V	—	300	—	MHz

* h_{FE} match of same type adjacent transistors is within 5%.

** V_{BE} match of same type adjacent NPN transistor is within +/− 1.0 mV.

** V_{BE} match of same type adjacent PNP transistor is within 1.2 mV.

Resistor Data (ALA400)

(T_A = 25°C)

Value (Ω)	Tol (%)	Type	TCR PPM/°C	Total
500	20	BI*	1900	104
1k	20	BI*	1900	168
5k	20	BI**	3000	216
10k	20	BI**	3000	168

Capacitor Data (ALA400)

Type	Cap (pF)	Tol (%)	Total
Programmable	1.0 to 5.0	±30	14

Component Totals (ALA400)

Component	Type	Total	Standard	JFET	Power
NPN	1 X	70	5	5	—
NPN	2 X	12	1	—	—
NPN	3 X	14	1	—	2
NPN	38 X	4	—	—	2
PNP	1 X	70	5	5	—
PNP	2 X	12	1	—	—
PNP	3 X	14	1	—	2
PNP	63 X	4	—	—	2
Resistors*	500 Ω 1 kΩ	104 168	8 12	4 12	— —
Resistors**	5 kΩ 10 kΩ	216 168	16 12	8 12	4 —
Capacitors	—	14	1	1	—
JFETs	—	4	—	2	—
Bonding Pads	—	44	—	—	—

* Denotes a 200 ohm/sq. implanted boron resistor.
** Denotes a 2000 ohm/sq. implanted boron resistor.

Resistor Data (ALA401)

(T_A = 25°C)

Value (Ω)	Tol (%)	Type	TCR PPM/°C	Total
100	20	BI*	1900	42
500	20	BI*	1900	72
1k	20	BI**	1900	64
5k	20	BI**	3000	132
10k	20	BI**	3000	100

Capacitor Data (ALA401)

Type	Cap (pF)	Tol (%)	Total
Programmable	1.0 to 7.0	±30	7

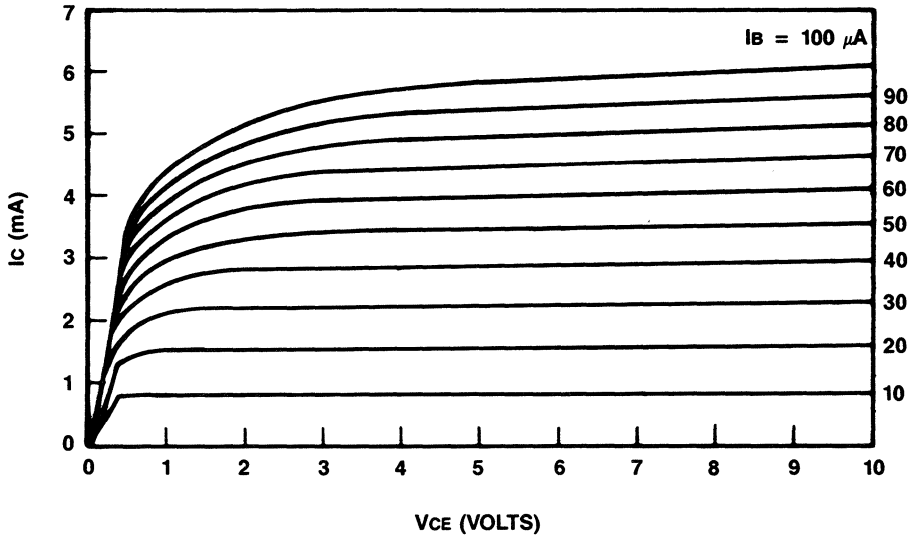
Component Totals (ALA401)

Component	Type	Total	Standard	Power
NPN	1 X	50	5	4
NPN	3 X	16	2	1
NPN	38 X	2	—	1
PNP	1 X	50	5	4
PNP	3 X	16	2	1
PNP	63 X	2	—	1
Resistors*	100 Ω 500 Ω 1 kΩ	42 72 64	6 8 8	— 8 4
Resistors**	5 kΩ 10 kΩ	132 100	16 12	10 8
Capacitors	—	7	1	—
Bonding Pads	—	38	—	—

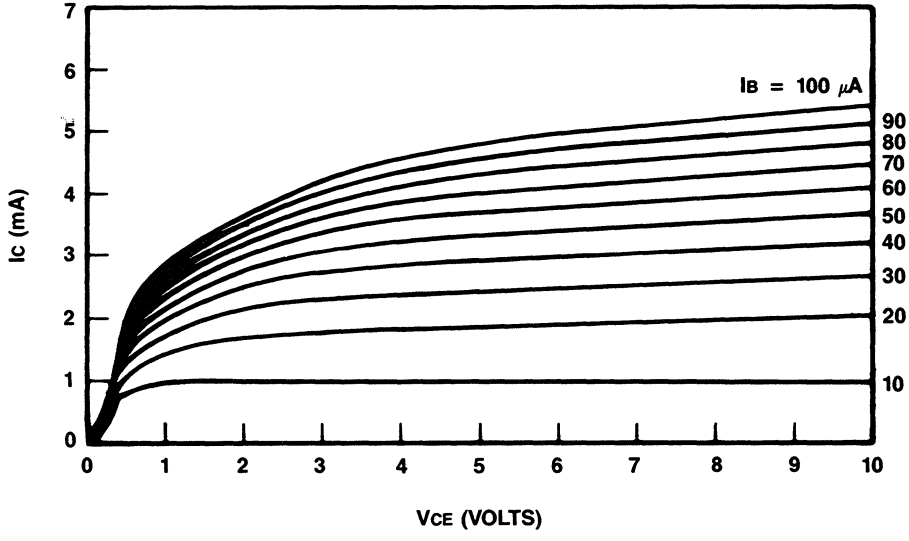
* Denotes a 200 ohm/sq. implanted boron resistor.

** Denotes a 2000 ohm/sq. implanted boron resistor.

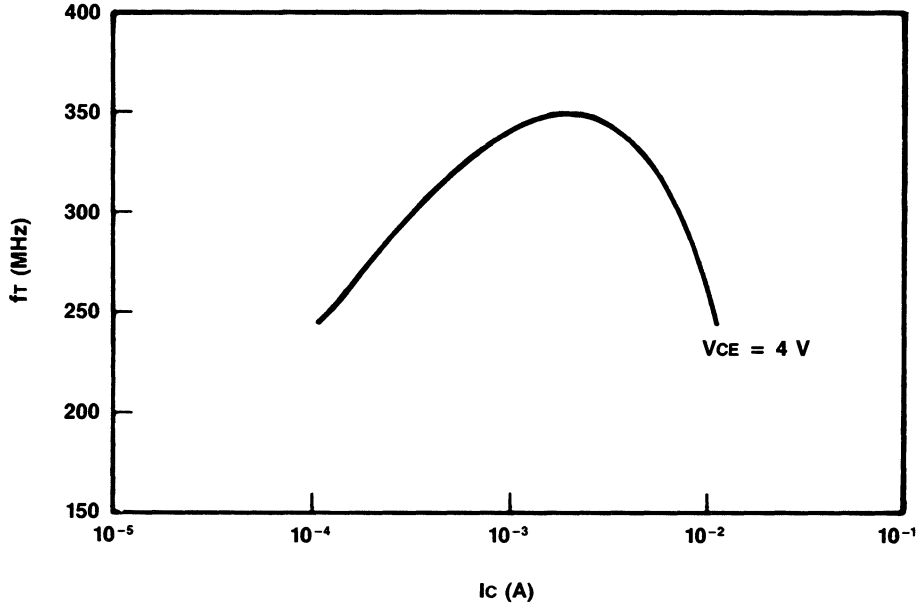
Output Characteristics (NPN)



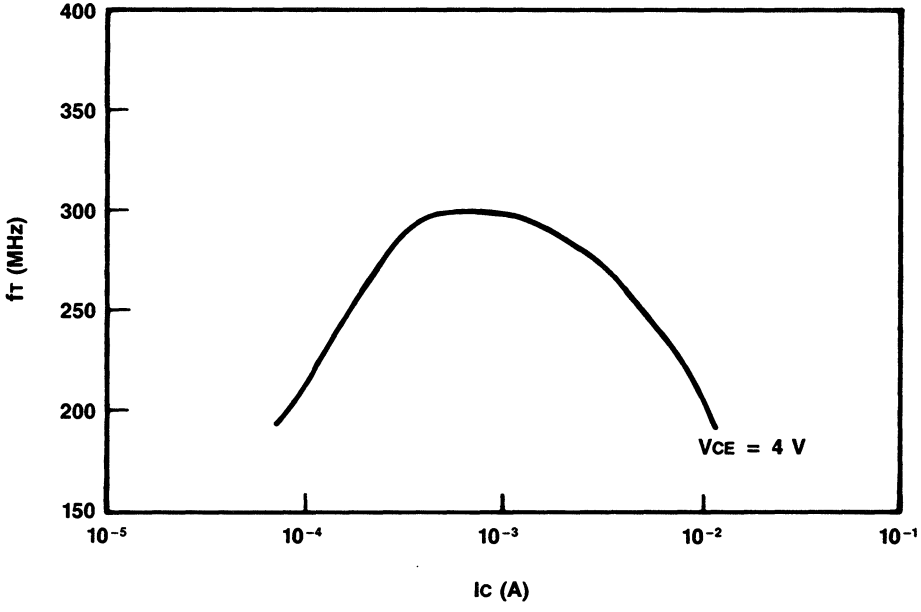
Output Characteristics (PNP)



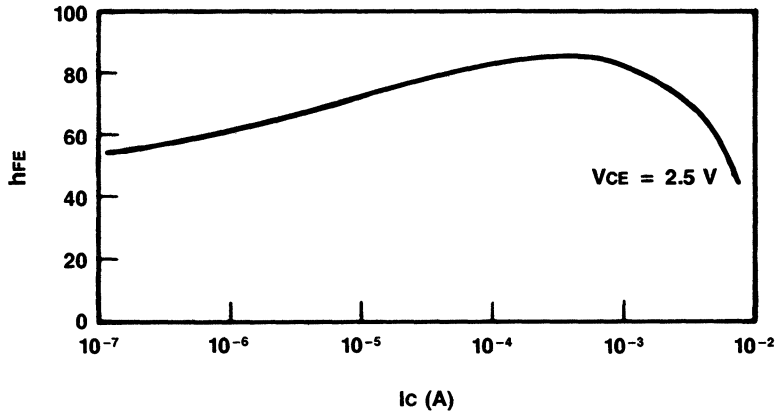
Common-Emitter Cutoff Frequency Characteristics (NPN)



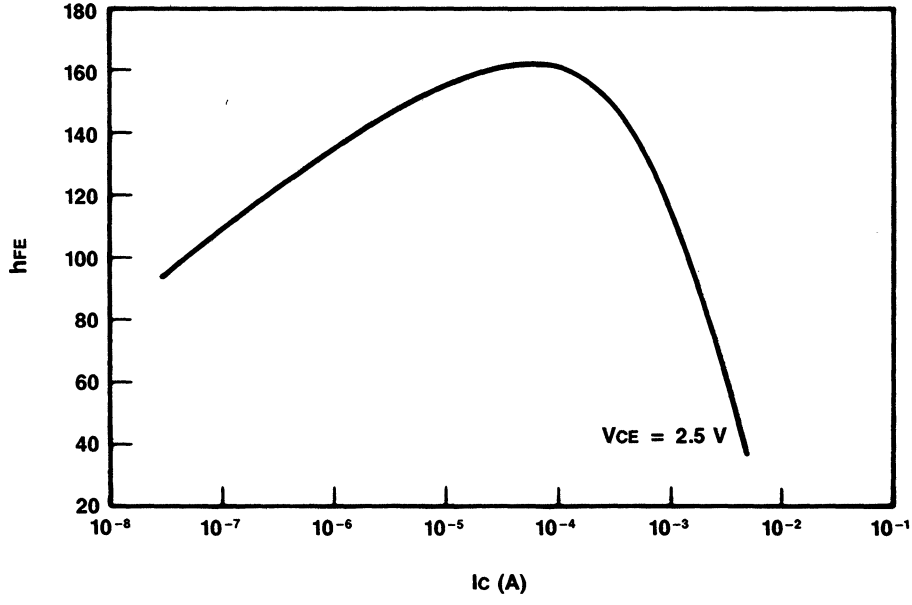
Common-Emitter Cutoff Frequency Characteristics (PNP)



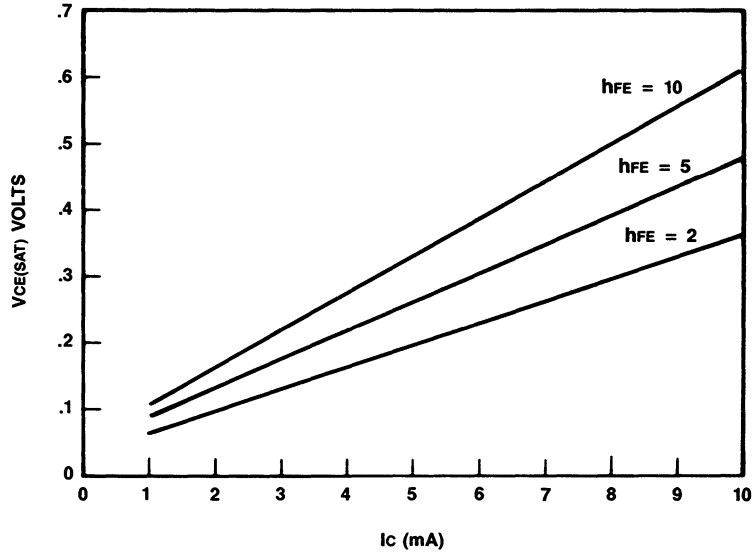
Common-Emitter Current Gain (NPN)



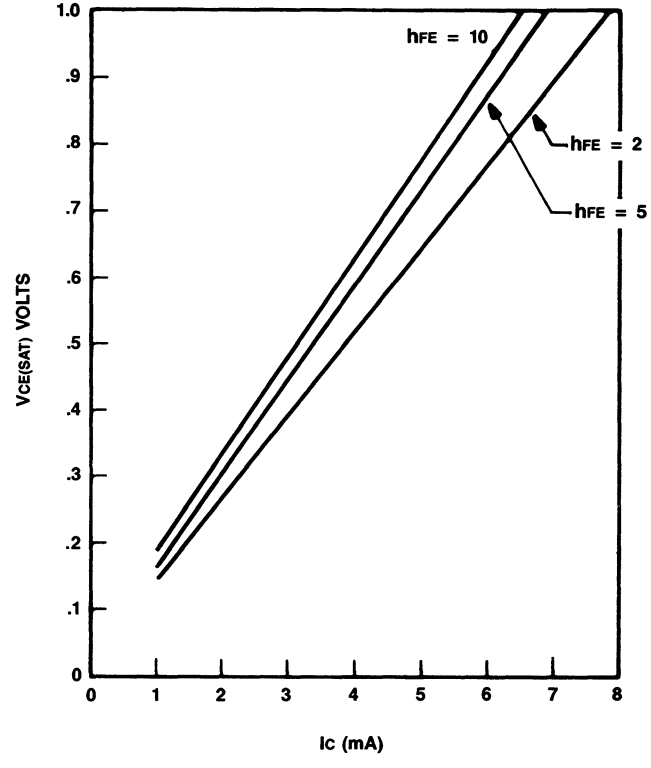
Common-Emitter Current Gain (PNP)



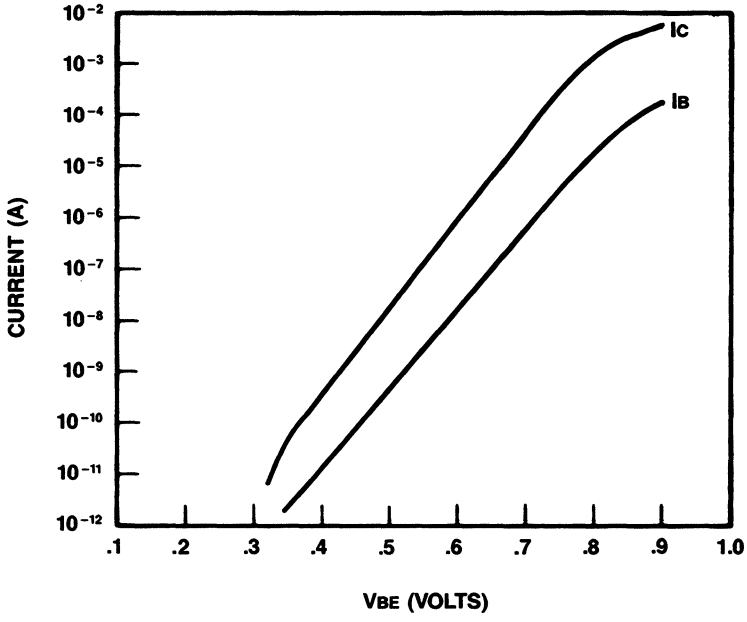
V_{CE} Saturation Characteristic (NPN)



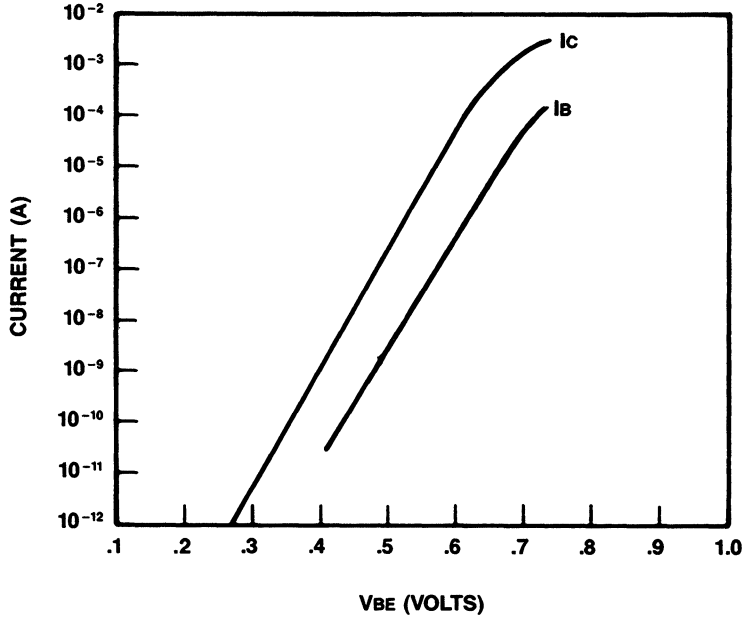
V_{CE} Saturation Characteristic (PNP)



Current-Voltage Characteristic (NPN)



Current-Voltage Characteristic (PNP)



AT&T'S CUSTOM DESIGN CAPABILITIES: BCDMOS AND CBIC

Using our latest technologies, custom designed integrated circuits can be created to meet the criteria of your most complex applications. As opposed to off-the-shelf devices, AT&T custom circuits offer several inherent advantages, including cost efficiency, higher levels of functionality, reduced circuit board requirements, simplicity of functional implementation, protection of proprietary circuits, and improved reliability. Moreover, in many cases, custom devices can provide unique capabilities that are not possible with general trade components.

The custom development methodology, as orchestrated by our design engineers, is a structured series of steps aimed at producing the best device within the expected time frame. Of course, there are a number of practical factors to be considered from the standpoint of function, complexity, production, cost, and application. But once custom design is imminent, selecting the most suitable technology becomes a critical decision.

BCDMOS (bipolar, CMOS, DMOS and IGBT combined), and CBIC-R, S, U (complementary bipolar) technologies, developed by Bell Laboratories at Reading, are available for a wide variety of custom-designed devices. Typical development time depends on complexity and performance requirements. But by using an extensive arsenal of computer-aided design tools for design capture, simulation, analysis and testing, there is a very high probability the circuitry will meet your specifications on the first design iteration.

A limited description of the technologies, including common characteristics and typical applications, is contained in the following overview.

BCDMOS

Although it's a relatively new technology, BCDMOS is considered versatile, affordable, and practical. It is distinguished by 400 volt switching devices and full analog/digital circuit capabilities. Additionally, using a dielectric isolation process allows complex functions to be fabricated on the same chip without the problems of parasitic device interaction and latch-up. The growing market for power and high-voltage ICs has already accelerated the popularity of BCDMOS processing, particularly since it supports the integration of a wide variety of silicon devices in a cost-effective, producible fashion.

Features

- NPN, PNP, DMOS, IGBT, and CMOS transistors on the same chip
- Free from latch-up and active parasitic elements
- Breakdown voltage of 400 volts with a 1000 volt maximum isolation between components

BCDMOS device structures including DMOS, IGBT, NPN, PNP and CMOS transistors, and a blocking diode are illustrated in Figure 1, with parametric data listed in Table 1. The DMOS device is fabricated in a standard, double-diffused process with a deep P + plug to prevent secondary breakdown. To create CMOS transistors, a special two-poly process was developed, offering 20 kΩ/sq. poly resistors. HVPMOS uses a simple, lightly-doped extended drain structure to support high voltage. BCDMOS also may be used in the fabrication of JFETs and photodiodes.

Table 1. Typical Parameters and Applications for BCDMOS 250 Volt Process

Field-Effect Devices			
Device	**BV_{TYP}**	**V_{TH}**	**Applications**
HVDMOS	290 V	2.4 V	Switching Driver
HVPMOS	300 V	−1.25 V	
LVNMOS	28 V	1.25 V	Logic, Analog
LVPMOS	32V	−1.25 V	
PJFET	60 V	1.6 V	Analog
D^2MOS	290 V	2.4 V	Switching Protection

Bipolar Junction Devices			
Device	**BV_{TYP}**	β	**Applications**
NPN	50 V_{CEO} 210 V_{CBO}	100	Analog, Level Shift, Pre-Drive
PNP	190 V_{CEO} 280 V_{CBO}	70	
SCR	275 V	—	Crowbar Switching
GTO	275 V	—	dc Current Break

Resistors		
Type	**Sheet RHO**	**TC**
Poly	20 kΩ/sq.	−4800 ppm
P_{BODY}	470 Ω/sq.	4800 ppm
N_{SOURCE}	27 Ω/sq.	1500 ppm

Miscellaneous

- 350 V blocking diodes
- 26 V, 13 V, and 7 V Zeners
- Photodiodes
- Dielectric capacitors, BV > 500 V
- Thinox capacitors, 35 nF/cm^2

CUSTOM DESIGN CAPABILITIES

CBIC

CBIC technology is a continuously evolving bipolar process used in analog devices. Developed by Reading Bell Laboratories in the early 1970s, it has allowed AT&T to forge the leading edge in IC design. The technology includes CBIC-U (12 volt), CBIC-R (33 volt), and CBIC-S (90 volt).

Features

- High-frequency output stage with high-swing tracking
- Symmetric current sources
- Precision, low-power level shifting
- High slew rate with low quiescent power
- High-speed PNPN latch circuits

Table 2. Transistor Characteristics

(At 25°C)

	CBIC-R		CBIC-U		CBIC-S	
	NPN	PNP	NPN	PNP	NPN	PNP
f_T (MHz)	350	300	4000	2500	350	300
h_{FE}	95	110	150	55	110	80
V_A	180	50	30	14	150	125
V_{CE} (mV)	100	175	165	350	100	175
V_{BE} (mV)	745	750	775	780	750	750
BV_{CEO} (V)	38	47	20	13	110	115
BV_{EBO} (V)	8.2	8.2	5.0	5.5	8.00	8.85
I_{CEO} (nA)	1	5	1.0	1.0	250	70
I_{CBO} (nA)	2	3	1.0	1.0	2	3

Typical Custom Applications

- CBIC-U, 12 V, 2.5 to 4 GHz
  - Broadband amplifiers
  - Phase-locked loops
  - Clock recovery circuits
  - Transceivers
- CBIC-R, 33 V, 350/300 MHz
  - High-frequency op amps
  - General-purpose data converters
  - Sample and hold circuits
  - Referencers
  - Ringers
  - Touch-tone generators
  - Adaptive filters (speakerphones)
- CBIC-S, 90 V, 350/300 MHz
  - Op amps
  - Thermal shutdown controllers (smart power)
  - Loop interfaces
  - Battery feeds

PACKAGING INFORMATION

The packaging technologies represented here are supported by sophisticated CAD and CAM systems and the latest assembly and testing procedures, resulting in an extremely reliable yet cost-effective package. Since electrical characteristics of packages affect device performance, AT&T packages are designed for reduced parasitics and minimal losses.

For convenient reference, all packages used in the catalog devices are illustrated below in the form of outline drawings. Included are the handling and installation criteria necessary to use the device properly while avoiding damage or compromising component life expectancy.

Three styles of packages are used for the catalog devices: the traditional through-hole, dual in-line package (DIP); the plastic leaded chip carrier (PLCC), and the surface-mount, small-outline (SO) package. (Inquiries concerning optional or custom packaging may be directed to your AT&T Account Manager.)

DIPs

Of all the through-hole packages, DIPs are the most commonly used. They feature two rows of in-line leads with a standard 100-mil pitch. Automated wire-bonding, postmolded plastic construction and high degree of thermal resistance are inherent in the design. (See packages B, C, D, E, F, and T.)

PLCCs

Chip carriers provide an effective method for surface mounting electronic components. The PLCC uses a "J-bent" lead design and features leads on all four sides of the package to improve space efficiency over DIPs. (See package P.)

SO-Type Packages

The SO is essentially a miniaturized surface-mount plastic DIP. They incorporate all the features of a standard plastic DIP, but with additional size reduction benefits for high-density circuit packs. Four different SO packages are available:

- SOJ-small outline with J-bent leads (package K)
- SOG-small outline "gull-wing" (package AB)
- SONB-small outline narrow body; a smaller version of the surface mount gull-wing (package AF, W, S)
- SOTB-small outline terminal butt-weld; short, conventional leads (package AH)

Handling and Installation Considerations

All devices are subject to damage as the result of electrostatic discharge. Proper precautions should be taken to eliminate exposure to electrostatic charge during handling and installation.

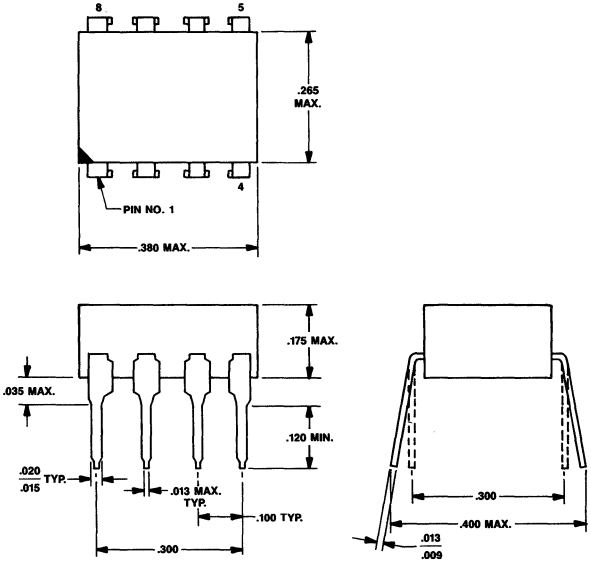
- DO NOT BEND THE LEADS ON SURFACE-MOUNT PACKAGES. One notable physical difference between DIPs and SO/PLCCs becomes apparent during installation. Because of the copper mainframe construction used in surface-mount styles, these packages should be board-mounted using solder or conductive adhesives. The leads are both softer and smaller than DIP leads and therefore are mot susceptible to damage when handling and mounting.
- Leads may be subjected to a maximum tensile force of one pound in any direction during mounting.
- DIP leads *only* may be bent to facilitate mounting or connecting the device into equipment. When inserted into circuit boards, the leads may be bent manually on the opposite side of the board using a crimping tool.
- For all packages, certain precautions should be taken when using solder during installation. When soldering from a constant temperature solder bath, temperatures as high as 300°C may be employed for a maximum of 15 seconds. For installation with a soldering iron, the temperature of the tip of the soldering iron should not be hotter than 500°C, and soldering time for each lead should not exceed 5 seconds. If soldering temperatures and/or soldering times exceed the recommended maxima, a suitable heat sink should be used to protect the device from thermal damage.

Package styles illustrated in the following outline drawings include:

— DIPs: B, C, D, E, F, T
— PLCC: P
— SOJ: K
— SOG: AB
— SONB: AF, W, S
— SOTB: AH

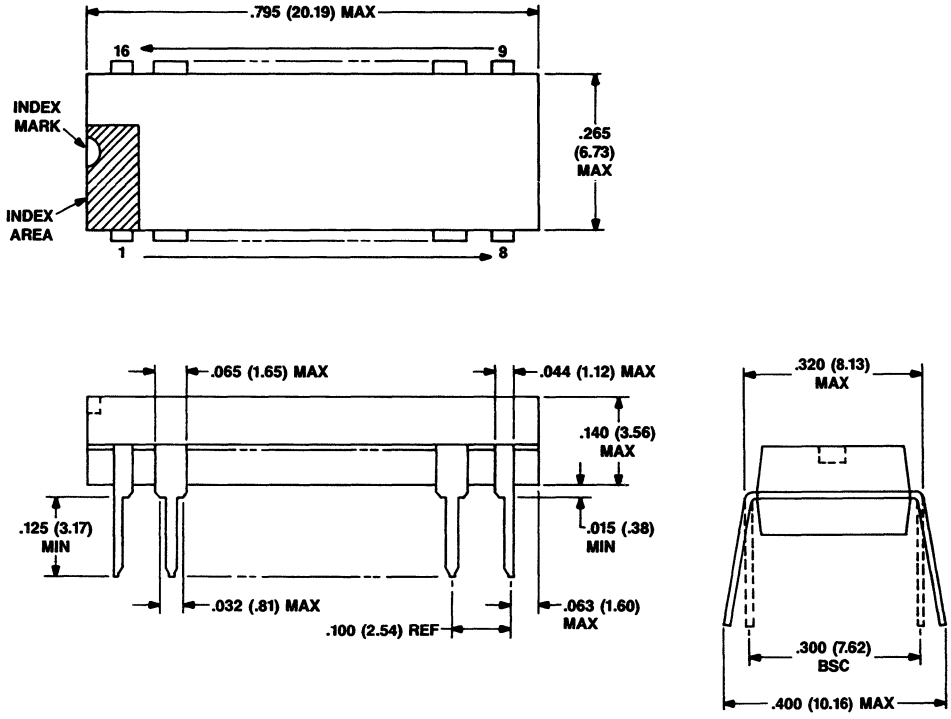
Outline Drawings

Package B—Standard 8-pin DIP (Dimensions in Inches)

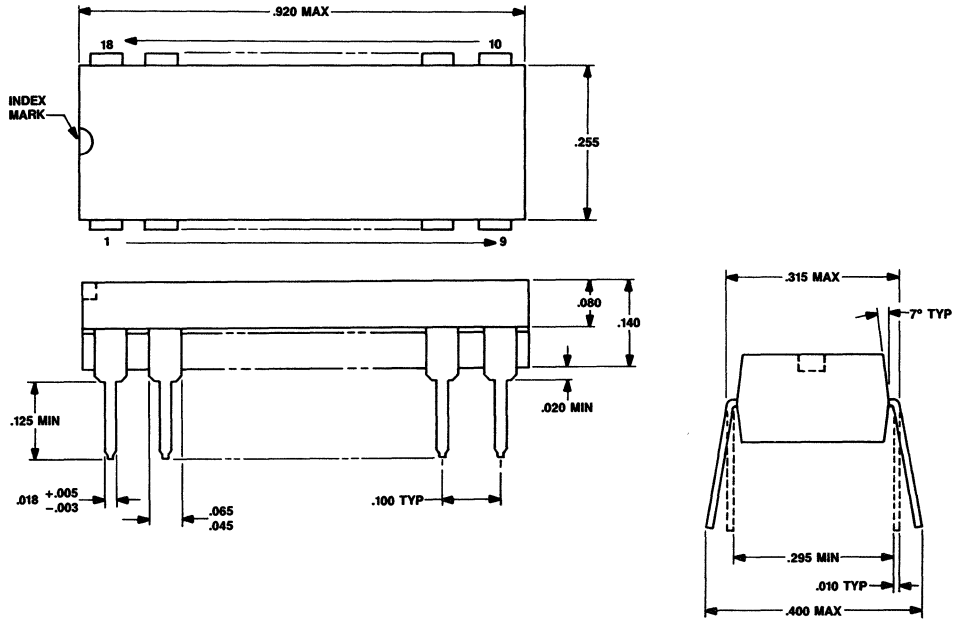


Outline Drawings (Continued)

Package C—Standard 16-pin DIP (Dimensions in Inches)

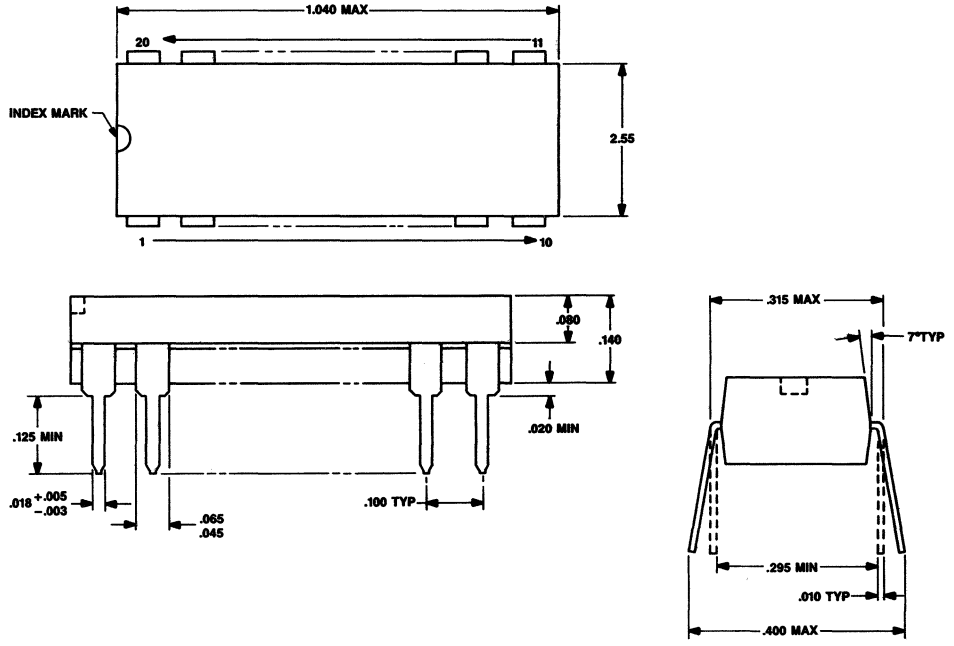


Package D—Standard 18-pin DIP (Dimensions in Inches)

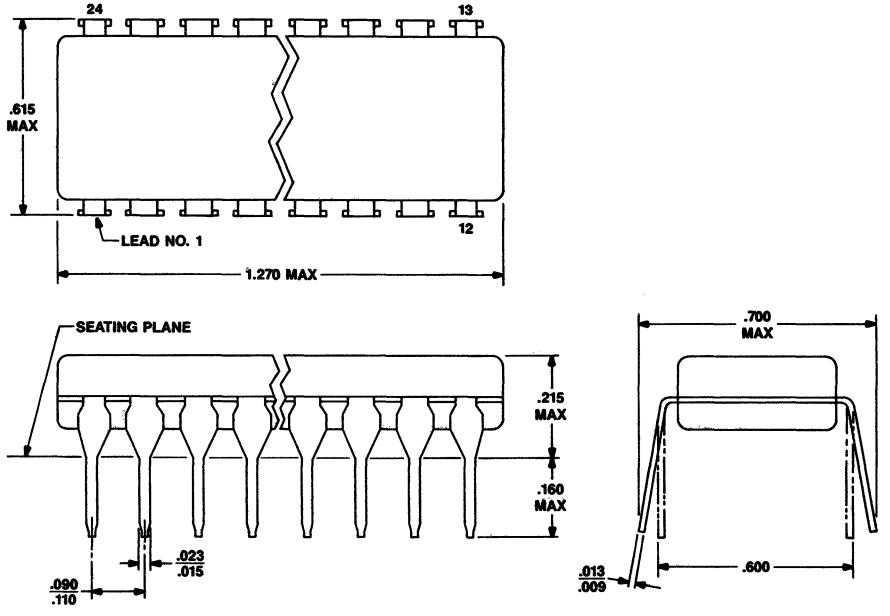


Outline Drawings
(Continued)

Package E—Standard 20-pin DIP (Dimensions in Inches)

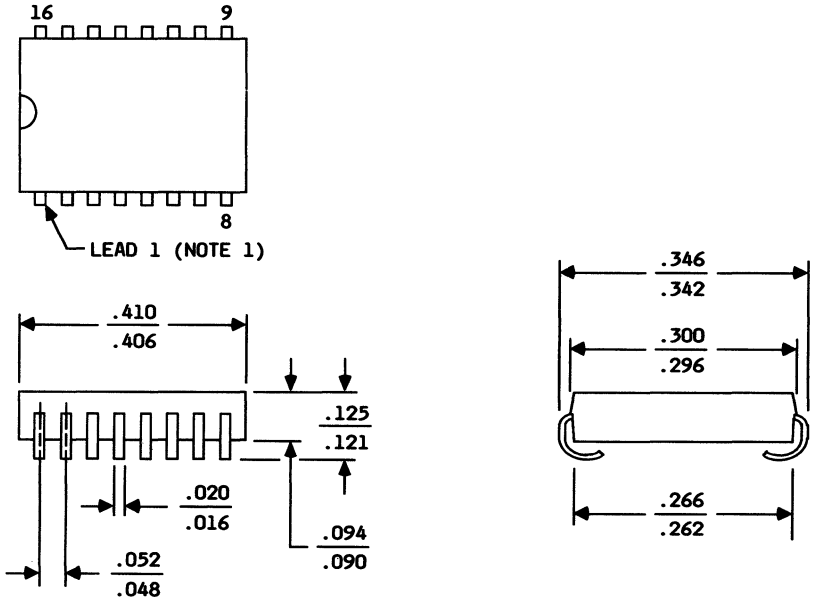


Package F—Standard 24-pin DIP (Dimensions in Inches)

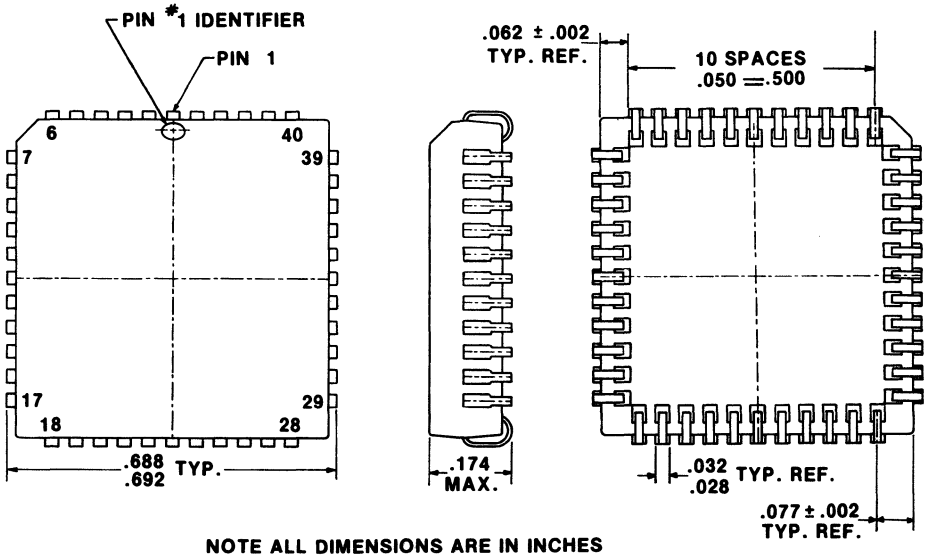


Outline Drawings
(Continued)

Package K—16-pin SOJ
(Dimensions in Inches)



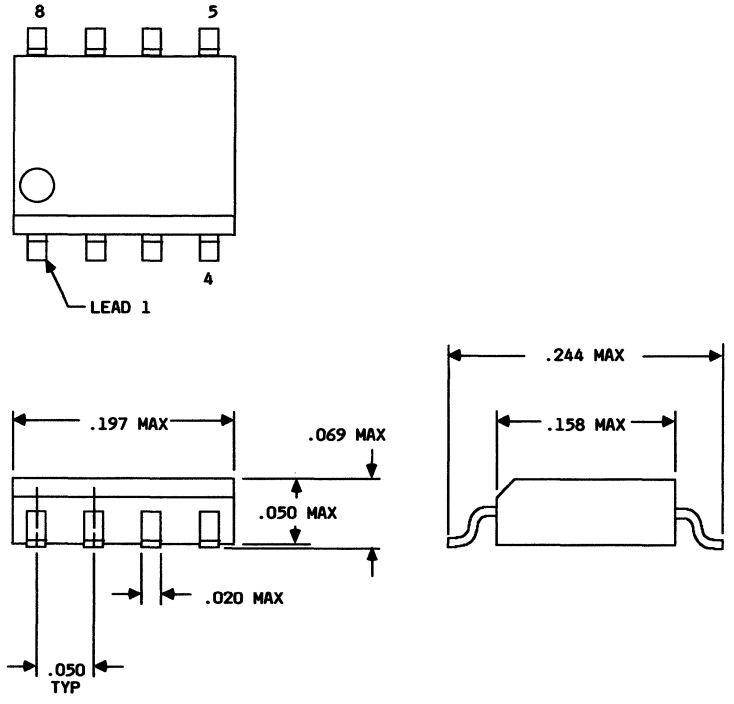
Package P—44-pin DIP
(Dimensions in Inches)



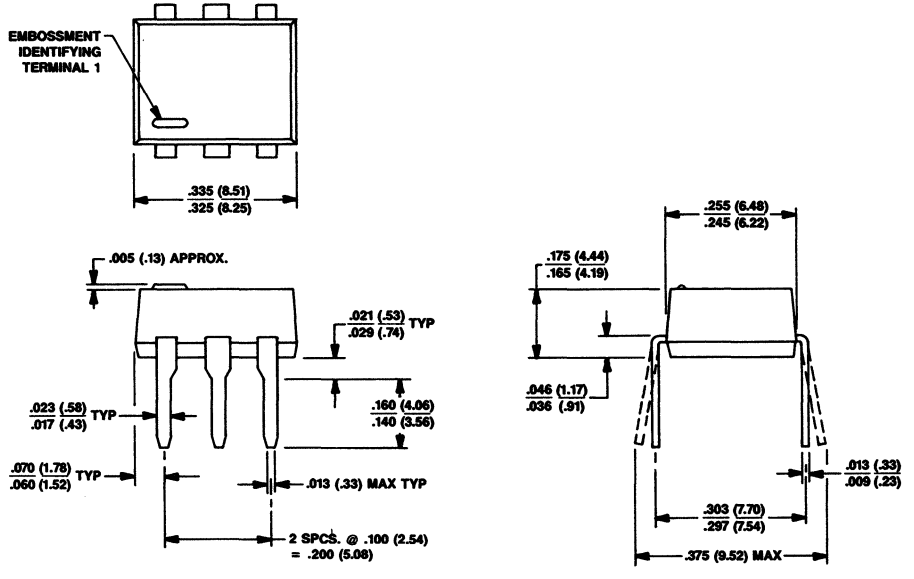
NOTE ALL DIMENSIONS ARE IN INCHES

Outline Drawings (Continued)

Package S—8-pin SONB (Dimensions in Inches)

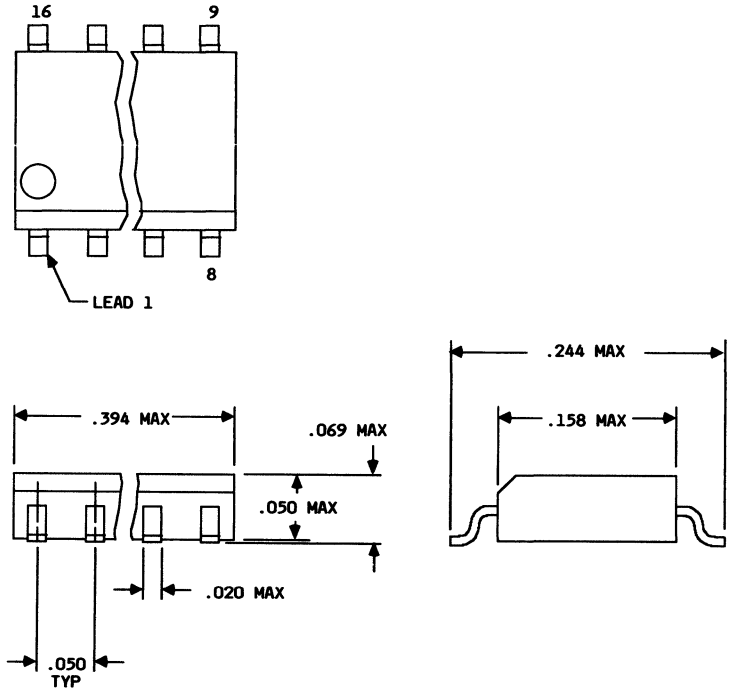


Package T—Standard 6-pin DIP (Dimensions in Inches)

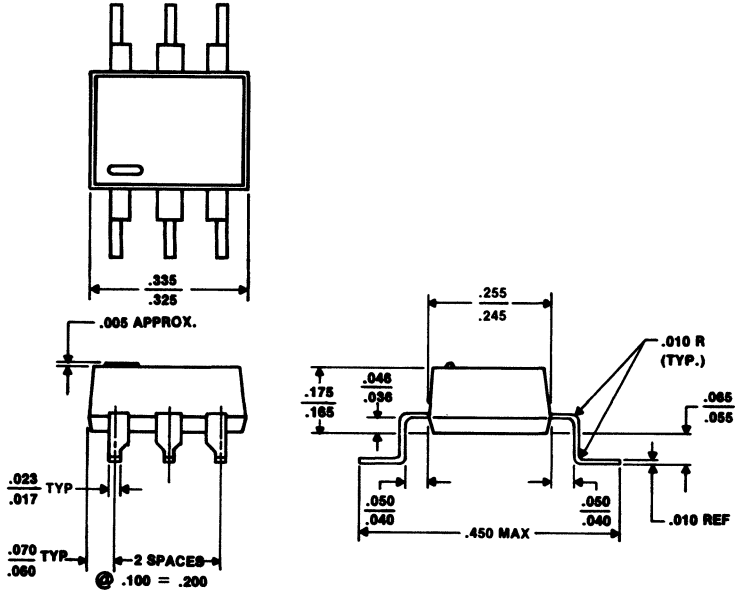


Outline Drawings (Continued)

Package W—16-pin SONB (Dimensions in Inches)

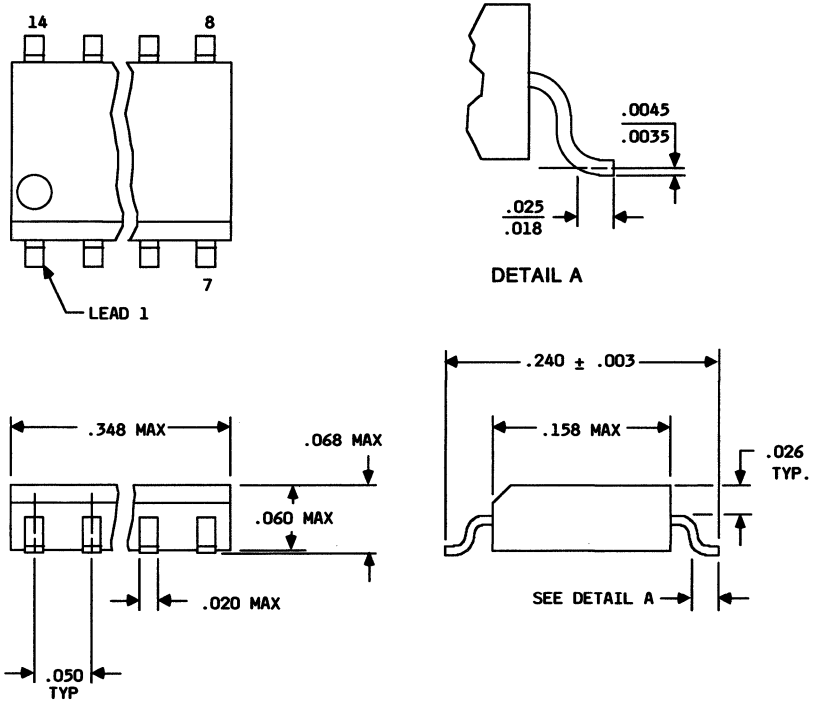


Package AB—6-pin SOG (Dimensions in Inches)

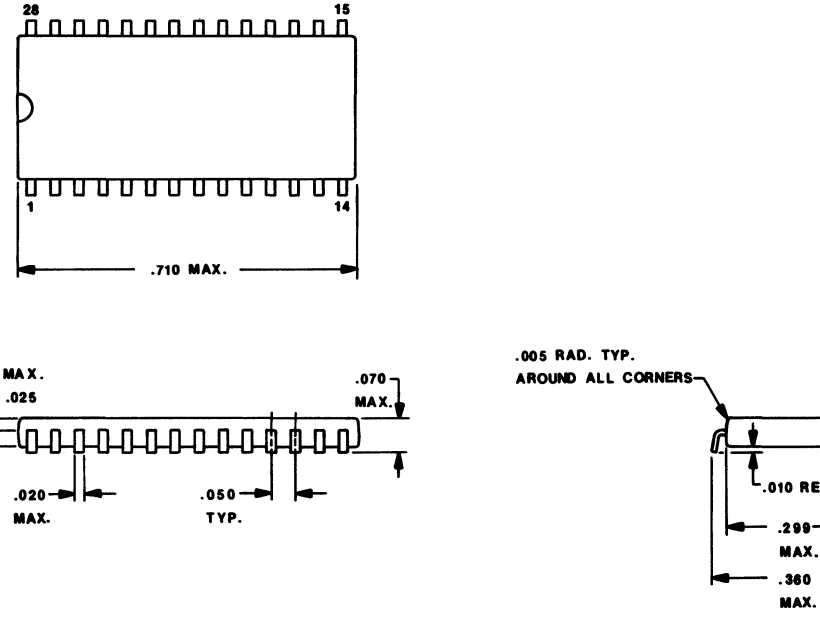


Outline Drawings (Continued)

Package AF—14-pin SONB (Dimensions in Inches)



Package AH—28-pin SOTB (Dimensions in Inches)



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