IOMD21 ASIC
Functional Specification

Distribution:	COMPANY CONFIDENTIAL
Title:	IOMD21 ASIC Functional Specification
Drawing Number:	0297,037/FS
Issue:	1
Author(s):	P.Watkinson / P.Pedder
Date:	19/05/94
Change Number:	AMR 4060
Last Issue:	N/A

Contents:

1: Introduction. 2
2: DRAM initialization during reset. 2
3: Video request modification. 2
4: I/O DMA. 2
5: Bd bus clash. 2
6: JTAG 2
7: Package and pinout 3

1: Introduction.

Apart from the minor changes listed below, the IOMD 21 has the same functionality and pin-out as the IOMD 20 (See IOMD Functional Specification 0297,030/FS)

2: DRAM initialization during reset.

To ensure the DRAM and VRAM is initialized (eg not in test mode), during reset IOMD 21 performs ras only refresh cycles by pulsing the 5 ras lines low for 125ns every 256us. The ARM address bus cycles during reset. IOMD passes the addresses through to the DRAM such that Ra<1> changes every 256us. IOMD 21 strobes the ras shortly after Ra<1> goes low. This ensures the address bus is stable during the ras strobe. One period of ref8m is used to time the width of the strobe pulse.

3: Video request modification.

In high data rate screen modes, VIDC20A re-asserts vidrq more quickly than VIDC 20. If the vidrq inactive time is to short, the IOMD20 arbitration logic does not see vidrq in-active, and so does not perform a pending sound request (or write to VIDC). This can result in the main bus state machine being stalled which prevents VRAM transfer cycles, and so lead to screen break up.

The modification prevents Vidrq being re-applied for up to one rclk low period, and thus allows a pending sound request (or VIDC write).

4: I/O DMA.

Relaxed set-up time for I/O DMA memory read data to ensure IOMD does not read incorrect data from a heavily loaded memory system.

5: Bd bus clash.

IOMD 21 delays turning on its Bd bus drivers by 32ns so that a bus clash with an external buffer using the Lrnw signal is avoided.

6: JTAG

The JTAG version number has been incremented to 3 (both for the boundary scan and for reading the internal VERSION register).

7: Package and pinout

IOMD21 is packaged in a 208 pin SQFP package, with a 0.5mm pin pitch. Pin 1 is at the top left corner, and pin numbering proceeds anti-clockwise, as shown in the diagram 9.1 below.

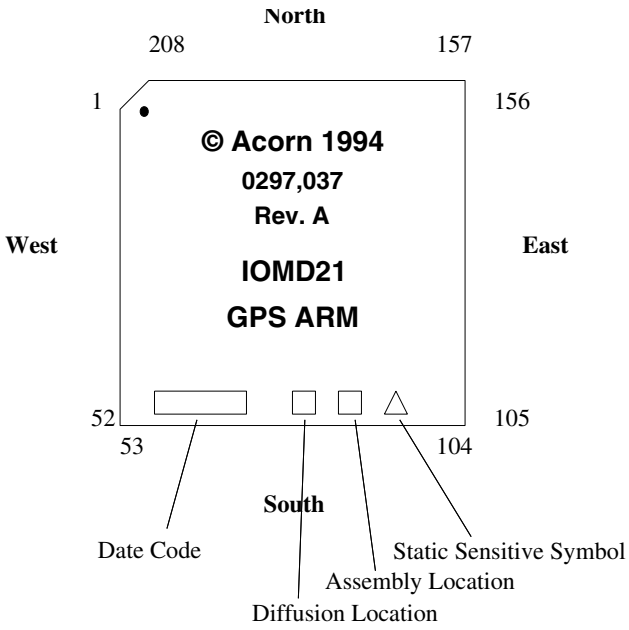

Figure 1.1 Pin location diagram for 208 SQFP package

The Packaging must have the following markings -

1. Part Number in the following format - 0297,037
2. A Revision Level - located under part number
3. Name of device - IOMD21
4. Manufacturers name or Logo
5. Acorn name or logo with copyright symbol and year
6. Pin 1 identification such as a dot
7. Date Code

The Revision Level is the control on the device and reflects the build standard.

If any changes are made to the build standard of the device , then the Revision Level must be updated and Acorn must be informed of, and agree to, any alterations.

The Revision level of the device is 'A'.

The Manufacturer can add any further information such as Assembly Location etc, as long as the markings remain of a suitable size and are legible.