MACH® 3 and 4 Family Data Book

2nd Generation High Density EE CMOS Programmable Logic

Fall 1994

Advanced Micro Devices

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MACH® 3 and 4 Family Data Book

Second Generation
High-Density EE CMOS
Programmable Logic

Fall 1994

ADVANCED MICRO DEVICES

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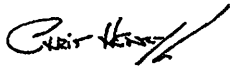
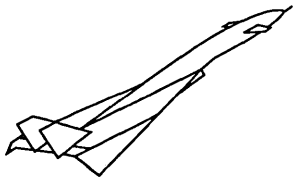
First introduced in Fall 1990, MACH® (Macro Array CMOS High-density) devices have set the industry standard for 15-nanosecond predictable worst-case pin-to-pin delays for devices ranging from 900 to 3600 gates. For the first time, higher-density EE CMOS PAL®-like devices with truly predictable speeds were widely available. FPGA and high-density customers responded enthusiastically, resulting in thousands of designs wins and over one million MACH devices shipped.

Based on your feedback, we are introducing the second generation of MACH devices – the MACH 3 and 4 families. Like the first generation MACH 1 and 2 devices, these new MACH devices have been the same, truly predictable pin-to-pin delays, but offer greater densities, increased flexibility, and higher-pin count packages. MACH 3 and 4 family devices feature synchronous or asynchronous operation, gate densities from 3500 to 10,000 gates, and 84 to 208 pins in PLCC and PQFP packages.

In just a few short years, AMD has become a major force in CMOS PLDs, building on our #1 spot in bipolar to become the industry leader in CMOS as well. Given the benefits of our advanced 0.65 micron double metal EE CMOS technology, we promise to continue providing the fastest and most innovative programmable logic devices, making it even easier to get new products to market quickly.



Chris Henry
Director of Marketing
Programmable Logic



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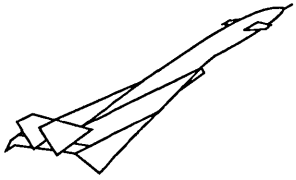

FINAL

MACH 3 and 4 Device Families

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High-performance, high-density electrically-erasable CMOS PLD families**
- **Predictable design-independent 15- and 20-ns speeds**
- **High density, pin count**
  - — 3500–10,000 PLD Gates
  - — 84–208 Pins
  - — 96–384 Registers
- **Input and output switch matrices increase ability to hold a fixed pinout**
- **JTAG, 5-V in-circuit programmability on devices with more than 84 pins**
- **Synchronous and asynchronous modes available for each macrocell**
  - — Clock generator in each PAL block for programmable clocks, edges in either mode
  - — Individual clock, initialization product terms in asynchronous mode
- **Central, input, and output switch matrices**
  - — 100% Routability
- **Up to 20 product terms per function**
- **96–256 configurable macrocells**
  - — D/T/J-K/S-R Registers, latches
  - — Synchronous or asynchronous mode
  - — Programmable polarity
  - — Reset/preset swapping
- **XOR gate available**
- **Registered/latched inputs on MACH 4 series**
- **Extensive third-party software and programmer support through FusionPLD℠ partners**

PRODUCT SELECTOR GUIDE

Device	Pins	Macrocells	PLD Gates	Max Inputs	Max Outputs	Max Flip-Flops	JTAG/ 5 V Prog	Speed
MACH 3 Family								
MACH355	144	96	3500	102	96	96	Y	15, 20
MACH 4 Family								
MACH435	84	128	5000	70	64	192	N	15, 20, Q-25
MACH445	100	128	5000	70	64	192	Y	10, 12, 15, 50
MACH446	100	128	5000	70	64	192	Y	10, 12, 15, 20
MACH465	208	256	10,000	146	128	384	Y	15, 20

GENERAL DESCRIPTION

The MACH® (Macro Array CMOS High-speed/density) family provides a new way to implement large logic designs in a programmable logic device. AMD has combined an innovative architecture with advanced electrically-erasable CMOS technology to offer a device with many times the logic capability of the industry's most popular existing PAL® device solutions at comparable speed and cost.

The second-generation MACH devices provide approximately three times the density and register count, and two times the amount of I/O of the original MACH 1 and 2 families. By increasing the pin count, adding functionality, and improving routing, the MACH 3 and 4 families build upon the strength of the MACH architecture without sacrificing predictable timing.

Their unique architecture makes these devices ideal for replacing large amounts of TTL, PAL-device, glue, and gate-array logic. They are the first devices to provide such increased functionality with completely predictable, deterministic speed.

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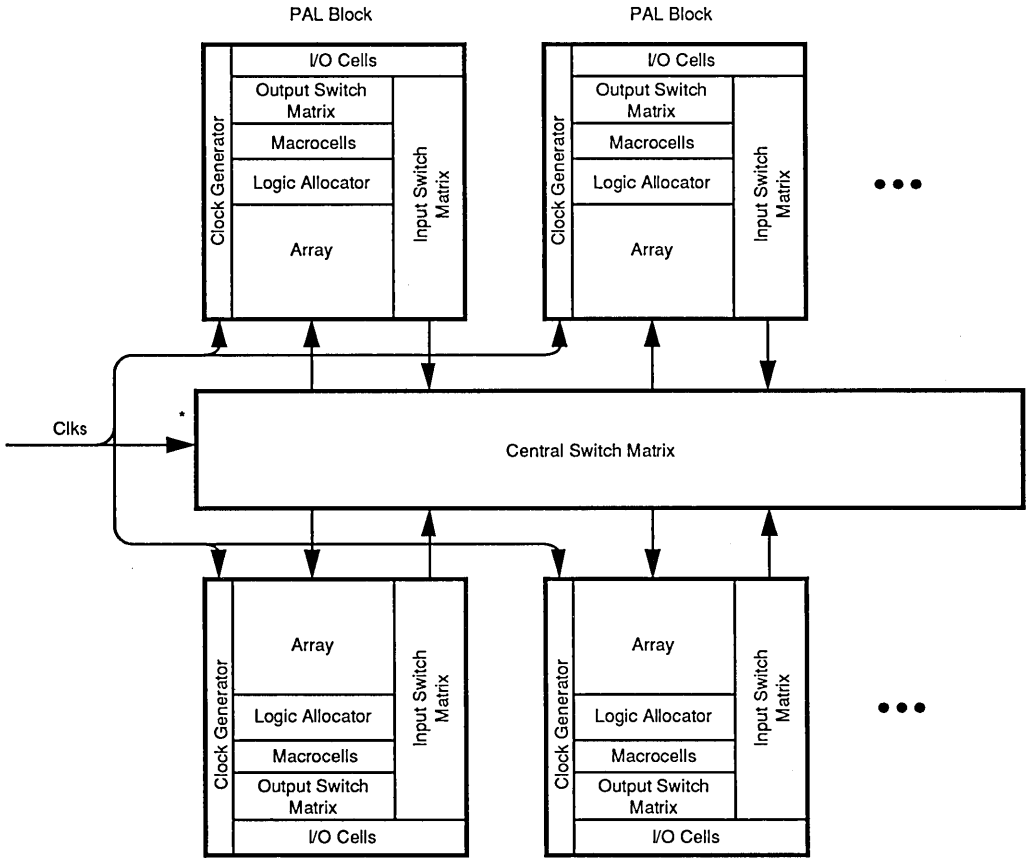
The MACH devices consist of PAL blocks interconnected by a programmable central switch matrix (Figure 1). Designs that consist of several interconnected functional modules can be efficiently implemented by placing the modules into PAL blocks. Designs that are not as modular can also be readily implemented since the central switch matrix provides a very high level of connectivity between PAL blocks.

The use of input and output switch matrices allows logic to be implemented independent of pin connections. This allows greater flexibility when making initial pin assignments for PCB layout, or when trying to maintain the pinout through design changes. The internal arrangement of resources is managed automatically by the design software, so that the designer does not have to be concerned with the logic implementation details.

AMD's FusionPLD program allows MACH device designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide timely, accurate, quality support. This ensures that a designer does not have to buy a complete new set of tools for each new device, but rather can use the tools with which he or she is already familiar. The MACH devices can programmed on conventional PAL device programmers. Devices with pin counts greater than 84 have an additional 5-V programming algorithm option that can be implemented with the devices soldered onto the board.

MACH devices are manufactured using AMD's state-of-the-art advanced CMOS electrically-erasable process for high performance and logic density. CMOS EE technology provides 100% testability, reducing both prototype development costs and production costs.



*The MACH465 has dedicated clock inputs.

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Figure 1. MACH 3 and 4 Block Diagram

Design Methodology

Design tools for all MACH devices are widely available both from AMD and from third-party software vendors. AMD provides MACHXL® software as a low-cost baseline tool set and works with third-party vendors to ensure broad MACH device support. MACHXL software is based on the popular PALASM® 4 software package, with support dedicated to the higher-density MACH 3 and 4 devices. PAL devices, MACH 1 devices, and MACH 2 devices are supported by PALASM 4 software; MACH 3 and 4 devices are supported by MACHXL software. This allows designers to do MACH device designs using the same methodology that they would use to do any PLD or FPGA designs, whether with MACHXL software or any of the other popular PAL device or FPGA design packages.

Design entry can be the same as that used for PAL, MACH 1, and MACH 2 devices. The basic logic processing steps are the same steps that are needed to process and minimize logic for any PAL device. Simulation is available for verifying the correct behavior of the device. Functional (unit-delay) simulation of MACH devices is supported in all approved software packages, and other options for simulating the timing and board-level behavior of the MACH devices are available. The end result is a JEDEC file that can be downloaded to a programmer for device configuration.

MACH device design methodology differs somewhat from that of a PAL device due to the automatic design fitting procedure that the software performs. Designs written by logic designers—whether by schematic capture, state machine equations, Boolean equations, or behavioral languages—are partitioned and placed into the PAL blocks of the MACH device. While this procedure is handled automatically by the software, the software can also accept manual direction based upon the user's working knowledge of the design. The overall device utilization provided by the fitter will vary from design to design, but in general significantly higher utilization can be expected from the MACH 3 and 4 families than from the MACH 1 and 2 devices due to the additional routing resources. In addition, MACH 3 and 4 device designs with higher utilization are more likely to retain the same pinout when design changes are made since the output switch matrix allows a pin to be driven by any of a number of macrocells.

AMD recommends allowing the software to decide the best fit and pin placement automatically for the first design iteration. This will provide the best chance of fitting. With this approach, large designs can be implemented incrementally, starting with low device utilization and building up by adding logic until the device is full. This generally means that designs are done without any specific pinout assignments, with the final pinout decided by the software. It is possible to "pre-place" signals, and, given the plentiful routing resources, pre-placement is very likely to be successful on the MACH 3 and 4 families. However, the most successful design fit can still be achieved by allowing the software as much fitting flexibility as possible.

The design is partitioned and placed into the MACH device by the software so as not to affect the performance of the design. With designs that do not fit it is possible to make some performance tradeoffs to aid in fitting (for example, by optimizing the flip-flop type or passing through the device more than once), but those tradeoffs must be specifically requested, and any additional delays are entirely predictable.

Once an initial design fits, there may be subsequent changes to the design. This is important if board layout has already started based on the original pinout. A major role of the input and output switch matrices is to allow such changes without impacting the original pinout. Certain design changes may make it impossible to maintain the original pinout, but designs can easily target 80% utilization without seriously jeopardizing the ability to make design changes and maintain pinout.

SECOND GENERATION MACH DEVICES

The MACH 3 and MACH 4 families consist of several members differentiated primarily by pin count and number of macrocells. The MACH 3 family has one macrocell per I/O pin; the MACH 4 family has two macrocells per I/O pin. In addition, the MACH 4 family has input registers. The MACH 4 register count is therefore three times the I/O pin count.

The devices range in pin count from 84 to 208; in number of macrocells from 96 to 256; and in number of registers from 96 to 384. All devices above 84 pins are provided in space-saving PQFP packages, with JTAG and 5-V in-circuit programmability. The 84-pin MACH435 comes in a PLCC package, without JTAG or 5-V programming, for pin-compatibility with the MACH130 and MACH230. Its architecture is available with JTAG and 5-V programmability in the 100-pin MACH445.

Functional Description

The fundamental architecture of the MACH devices consists of multiple optimized PAL blocks interconnected by a central switch matrix. The central switch matrix allows communication between PAL blocks, and routes inputs to the PAL blocks. Together, the PAL blocks and central switch matrix allow the logic designer to create large designs in a single device instead of multiple devices.

Most pins are I/O pins that can be used as inputs, output, or bidirectional pins. There are some dedicated input pins, but all macrocells have internal feedback, allowing the pin to be used as an input if the macrocell signal is not needed externally.

The key to being able to make effective use of these devices lies in the interconnect schemes. Because of the programmable interconnections, the product term arrays have been decoupled from the central switch matrix; the macrocells have been decoupled from the product terms through the logic allocator; and the I/O pins have been decoupled from the macrocells due to the output switch matrix. In addition, more input routing options are provided by the input switch matrix. These resources provide the flexibility needed to place and route designs efficiently.

In a MACH device, all signals incur the same delays, regardless of routing. Performance is design-independent, and is known before the design is begun.

The PAL Blocks

The PAL blocks resemble independent PAL devices on the chip. This provides for logic functions that need the complete interconnect that a PAL device provides. PAL blocks communicate with each other through the central switch matrix.

Each PAL block consists of:

- a product-term array
- a logic allocator
- macrocells
- an output switch matrix
- I/O cells
- an input switch matrix
- a clock generator

The logic allocator distributes the product terms to the macrocells, as required by each individual design. The macrocell configures the signal largely by determining the storage characteristics. Macrocell signals are routed to I/O cells and the I/O pins by the output switch matrix. The I/O cells on MACH 4 devices also allow for registered or latched inputs. The input switch matrix optimizes the routing of input signals into the central switch matrix.

The clock generator uses the four global clock inputs to generate a set of four clock signals available throughout the PAL block. Various combinations of clock signals in both true and complement form can be generated.

Each PAL block also contains an asynchronous reset product term and an asynchronous preset product term to be used for synchronous-mode macrocells. This allows synchronous flip-flops within a single PAL block to be initialized as a bank. Macrocells implemented in asynchronous mode are not affected by the PAL-block initialization.

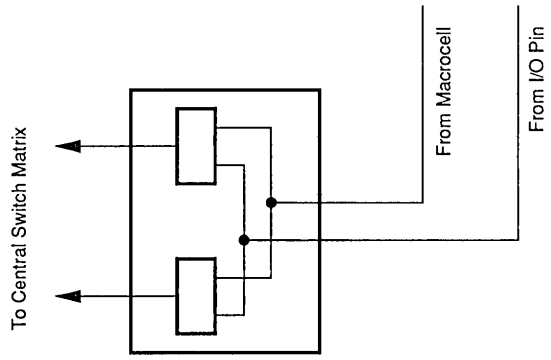
The Central Switch Matrix

The central switch matrix takes all dedicated inputs and signals from the input switch matrices and routes them as needed to the PAL blocks. Feedback signals that only return to the same PAL block still must go through the central switch matrix. This mechanism ensures that PAL blocks in MACH devices communicate with each other with consistent, predictable delays.

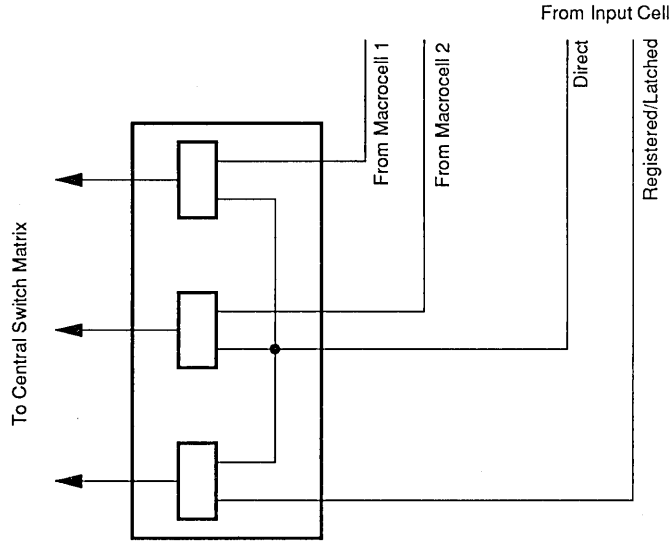
The central switch matrix makes a MACH device more than just several PAL devices on a single chip. It allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into PAL blocks through the central switch matrix so that the designer does not have to be concerned with the internal architecture of the device.

The Input Switch Matrix

The input switch matrix (Figure 2) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.



a. MACH 3; one per macrocell



b. MACH 4; one for every two macrocells

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Figure 2. Input Switch Matrix

PAL Block Clock Generation

Each MACH 3 and 4 device has four clock pins that can also be used as inputs. These pins drive a clock generator in each PAL block (Figure 3). The clock generator provides four clock signals that can be used anywhere in the PAL block. These four PAL block clock signals can consist of a large number of combinations of the true and complement edges of the global clock signals; Table 1 lists the possible combinations.

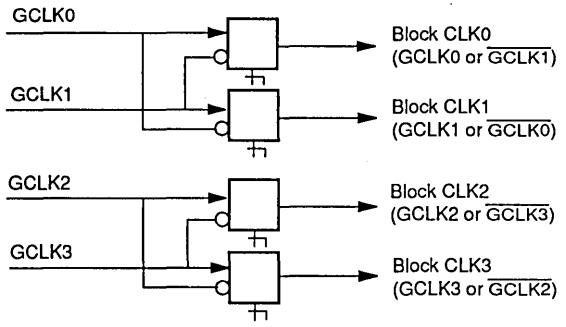


Figure 3. PAL Block Clock Generator

Table 1. PAL Block Clock Combinations

Block CLK0	Block CLK1	Block CLK2	Block CLK3
GCLK0	GCLK1	X	X
$\overline{\text{GCLK1}}$	GCLK1	X	X
GCLK0	$\overline{\text{GCLK0}}$	X	X
$\overline{\text{GCLK1}}$	$\overline{\text{GCLK0}}$	X	X
X	X	GCLK2	GCLK3
X	X	$\overline{\text{GCLK3}}$	GCLK3
X	X	GCLK2	$\overline{\text{GCLK2}}$
X	X	$\overline{\text{GCLK3}}$	$\overline{\text{GCLK2}}$

This feature provides high flexibility for partitioning state machines and dual-phase clocks. It also allows latches to be driven with either polarity of latch enable, and in a master-slave configuration.

Synchronous and Asynchronous Operation

The MACH 3 and 4 families can perform synchronous or asynchronous logic. Each individual cell can be programmed as synchronous or asynchronous, allowing unlimited "mixing and matching" of the two logic styles. The selection of synchronous or asynchronous mode affects the logic allocator and the macrocell, since product terms used for logic in the synchronous mode are used for control functions in the asynchronous mode.

The Product Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the central switch matrix (Table 2), and are provided in both true and complement forms for efficient logic implementation.

Table 2. PAL Block Inputs

Device	Number of Inputs to PAL Block
MACH355	33
MACH435	33
MACH445	33
MACH446	33
MACH465	34

Because the number of product terms available for a given logic function is not fixed, the full sum of products is not realized in the array. The product terms drive the logic allocator, which allocates the appropriate number of product terms to generate the function.

The Logic Allocator

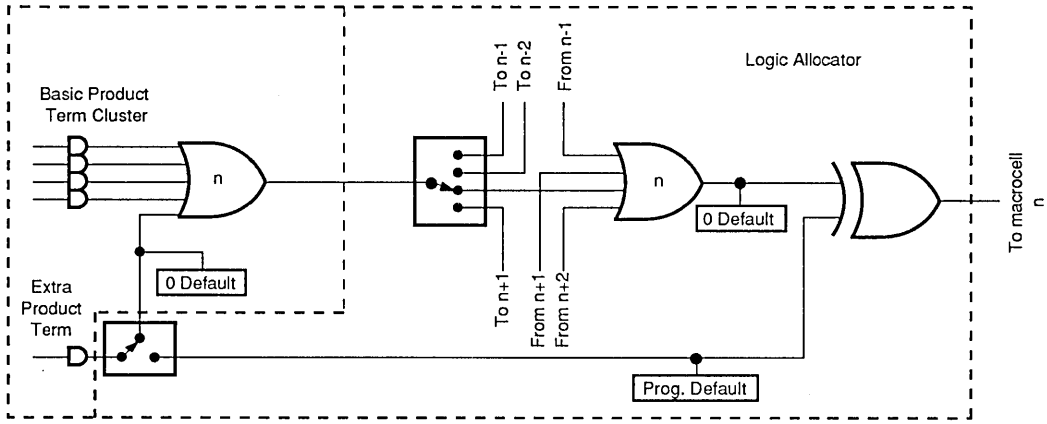
Within the logic allocator, product terms are allocated to macrocells in "product term clusters." The availability and distribution of product term clusters are automatically considered by the software as it places and routes functions within a PAL block. The size of a product term cluster has been optimized to provide high utilization of product terms, making complex functions using many

product terms possible. Yet when few product terms are used, there will be a minimal number of unused—or wasted—product terms left over.

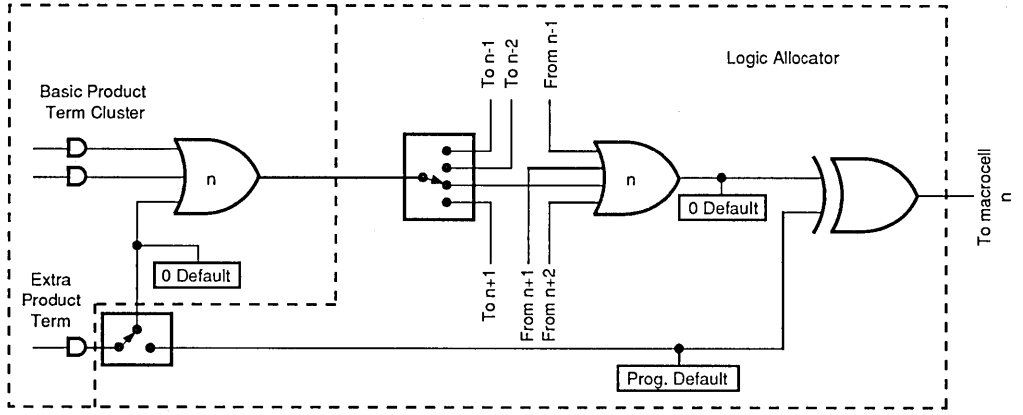
The logic allocator has two fundamental modes, depending on whether the macrocell is synchronous or asynchronous. The synchronous mode (Figure 4a) has a basic product term cluster of four product terms; the asynchronous mode (Figure 4b) has a basic cluster of two product terms. Note that if the product term cluster is routed to a different macrocell, the allocator configuration is not determined by the mode of the macrocell actually being driven. The configuration is always set by the mode of the macrocell that the cluster will drive if not routed away, regardless of the actual routing.

In addition, there is an extra product term that can either join the basic cluster to give an extended cluster, or drive the second input of an exclusive-OR gate in the signal path. If included with the basic cluster, this provides for up to 20 product terms on a synchronous function that uses four extended 5-product-term clusters. A similar asynchronous function can have up to 18 product terms.

When the extra product term is used to extend the cluster, the value of the second XOR input can be programmed as a 0 or a 1, giving polarity control. The possible configurations of the logic allocator are shown in Figures 5 and 6.



a. Synchronous Mode



b. Asynchronous Mode

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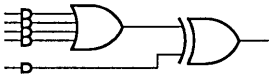
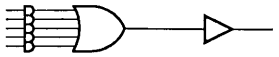
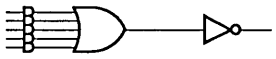
Figure 4. Logic Allocator. Configuration of cluster "n" set by mode of macrocell "n".



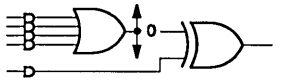
a. Basic cluster with XOR



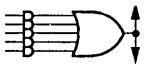
b. Extended cluster, active high



c. Extended cluster, active low



d. Basic cluster routed away; single-product-term, active high



e. Extended cluster routed away

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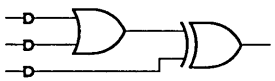
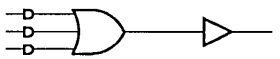
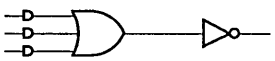
Figure 5. Logic Allocator Configurations: Synchronous Mode



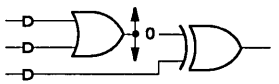
a. Basic cluster with XOR



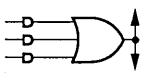
b. Extended cluster, active high



c. Extended cluster, active low



d. Basic cluster routed away; single-product-term, active high



e. Extended cluster routed away

17466C-6

Figure 6. Logic Allocator Configurations: Asynchronous Mode

Note that the configuration of the logic allocator has absolutely no impact on the speed of the signal. All configurations have the same delay. This means that designers do not have to decide between optimizing resources or speed; both can be optimized.

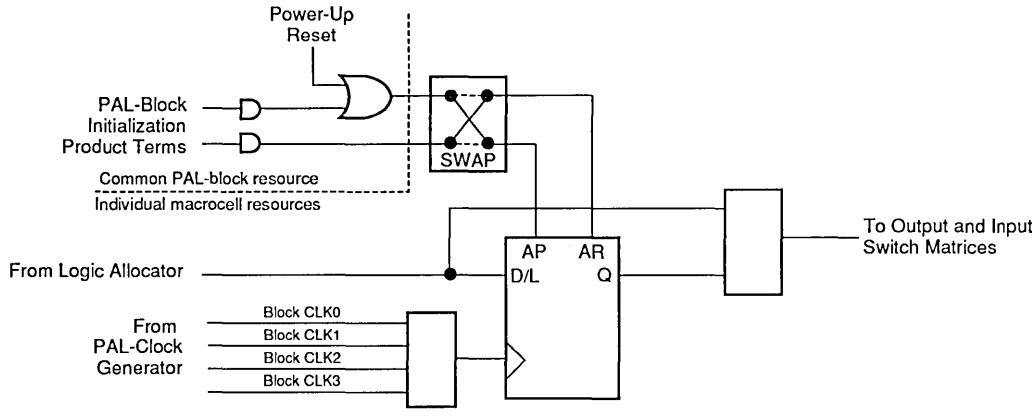
If not used in the cluster, the extra product term can act in conjunction with the basic cluster to provide XOR logic for such functions as data comparison, or it can work with the D-type flip-flop to provide for T, J-K, and S-R register operation. In addition, if the basic cluster is

routed to another macrocell, the extra product term is still available for logic. In this case, the first XOR input will be a logic 0. This circuit has the flexibility to route product terms elsewhere without giving up the use of the macrocell.

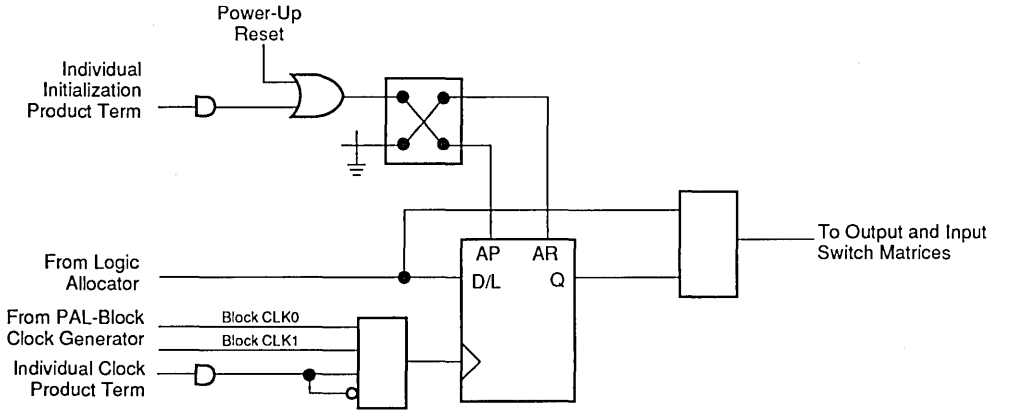
Product term clusters do not "wrap" around a PAL block. This means that the macrocells at the ends of the block have fewer product terms available. Refer to the individual product data sheets for details.

The Macrocell

The macrocell consists of a storage element, routing resources, a clock multiplexer, and initialization control. The macrocell has two fundamental modes: synchronous and asynchronous (Figure 7). The mode chosen only affects clocking and initialization in the macrocell.



a. Synchronous Mode



b. Asynchronous Mode

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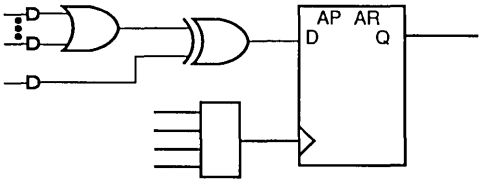
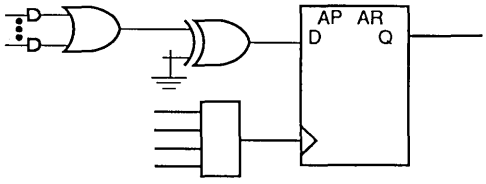
Figure 7. Macrocell

In either mode, a combinatorial path can be used. For combinatorial logic, the synchronous mode will generally be used, since it provides more product terms in the allocator.

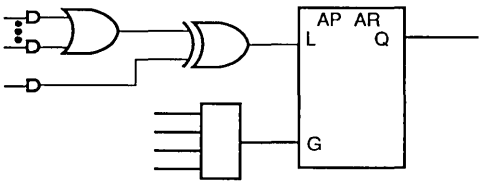
The flip-flop can be configured as a D-type, T-type, J-K, or S-R register or latch. The primary flip-flop configurations are shown in Figure 8, although others are possible. Flip-flop functionality is defined in Table 3. Note that a J-K latch is unadvisable, as it will cause oscillation if both J and K inputs are HIGH.



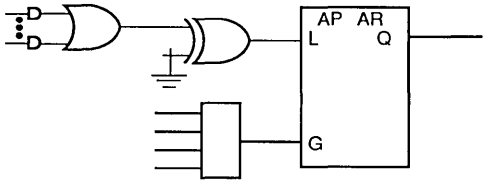
a. D-type with XOR



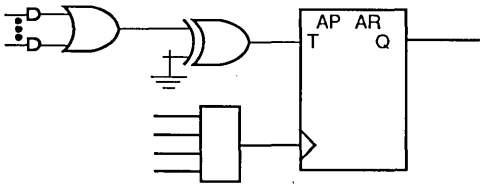
b. D-type with programmable D polarity



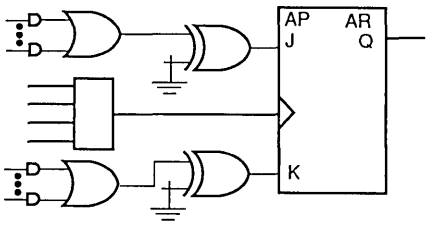
c. Latch with XOR



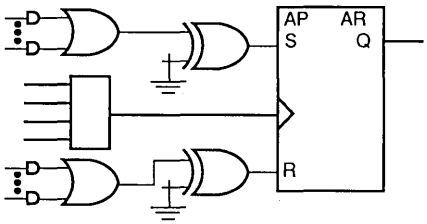
d. Latch with programmable polarity



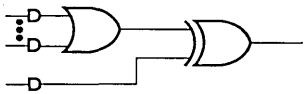
e. T-type with programmable T polarity



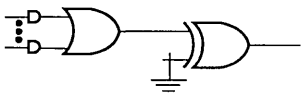
f. J-K with programmable J and K polarity



g. S-R with programmable S and R polarity



h. Combinatorial with XOR



i. Combinatorial with programmable polarity

17466C-8

Figure 8. Primary Macrocell Configurations

Table 3. Register/Latch Operation

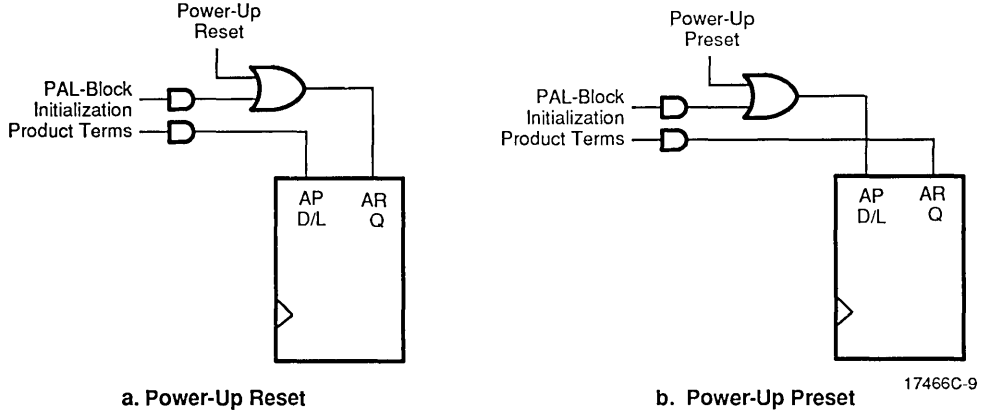
Configuration	Input(s)	CLK/LE*	Q+
D-type Register	D=X	0, 1, ↓(↑)	Q
	D=0	↑(↓)	0
	D=1	↑(↓)	1
T-type Register	T=X	0, 1, ↓(↑)	Q
	T=0	↑(↓)	Q
	T=1	↑(↓)	$\overline{Q}$
J-K Register	J=K=X	0, 1, ↓(↑)	Q
	J=0, K=0	↑(↓)	Q
	J=0, K=1	↑(↓)	0
	J=1, K=0	↑(↓)	1
	J=1, K=1	↑(↓)	$\overline{Q}$
S-R Register	S=R=X	0, 1, ↓(↑)	Q
	S=0, R=0	↑(↓)	Q
	S=0, R=1	↑(↓)	0
	S=1, R=0	↑(↓)	1
	S=1, R=1	↑(↓)	Undefined
D-type Latch	D=X	1(0)	Q
	D=0	0(1)	0
	D=1	0(1)	1

**Polarity of CLK/LE can be programmed.*

Although the macrocell shows only one input to the register, the XOR gate in the logic allocator allows the D-type register to emulate T, J-K, and S-R behavior. In this case, the available product terms are divided between J and K (or S and R). When configured as J-K, S-R, or T-type, the extra product term must be used on the XOR gate input for flip-flop emulation. In any register type, the polarity of the inputs can be programmed.

The clock input to the flip-flop can select any of the four PAL block clocks in synchronous mode, with the additional choice of either polarity of an individual product term clock in the asynchronous mode.

The initialization circuit depends on the mode. In synchronous mode (Figure 9), asynchronous reset and preset are provided, each driven by a product term common to the entire PAL block.



a. Power-Up Reset

b. Power-Up Preset

Figure 9. Synchronous Mode Initialization Configurations

A subtle difference between MACH 1 and 2 devices and the MACH 3 and 4 devices is that the original devices have programmable output polarity; that is, the polarity control comes after the flip-flop. In the new MACH 3 and 4 architecture, the flip-flop input polarity is programmable. For designs that can be implemented on both the older and newer devices, this makes no difference except that in the older architecture, reset and preset values are affected by polarity; in the new architecture they are not. A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility and design compatibility between the old and new architectures.

In asynchronous mode (Figure 10), a single individual product term is provided for initialization. It can be selected to control reset or preset.

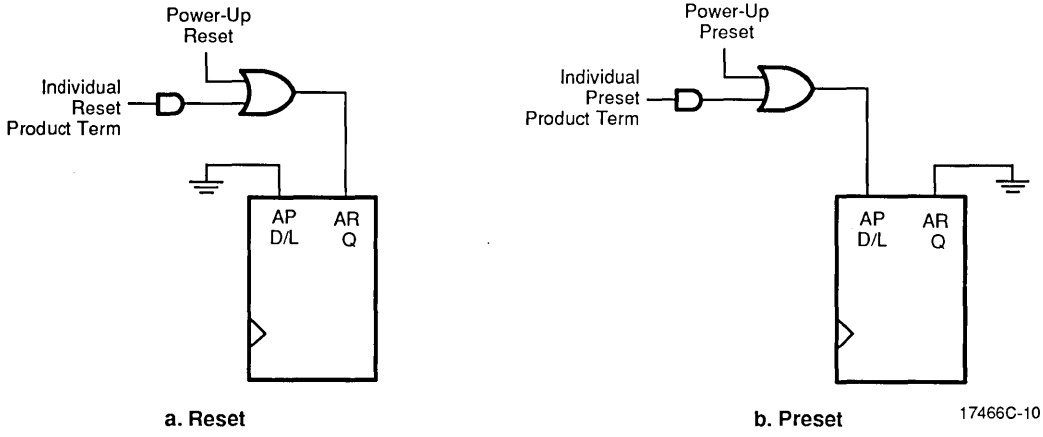


Figure 10. Asynchronous Mode Initialization Configurations

Note that the reset/preset swapping selection feature affects power-up reset as well. The initialization functionality of the flip-flops is illustrated in Table 4.

The macrocell sends its data to the output switch matrix and the input switch matrix. The output switch matrix can route this data to an output if so desired. The input switch matrix can send the signal back to the central switch matrix as feedback.

Table 4. Asynchronous Reset/Preset Operation

AR	AP	CLK/LE*	Q+
0	0	X	See Table 3
0	1	X	1
1	0	X	0
1	1	X	0

**Transparent latch is unaffected by AR, AP.*

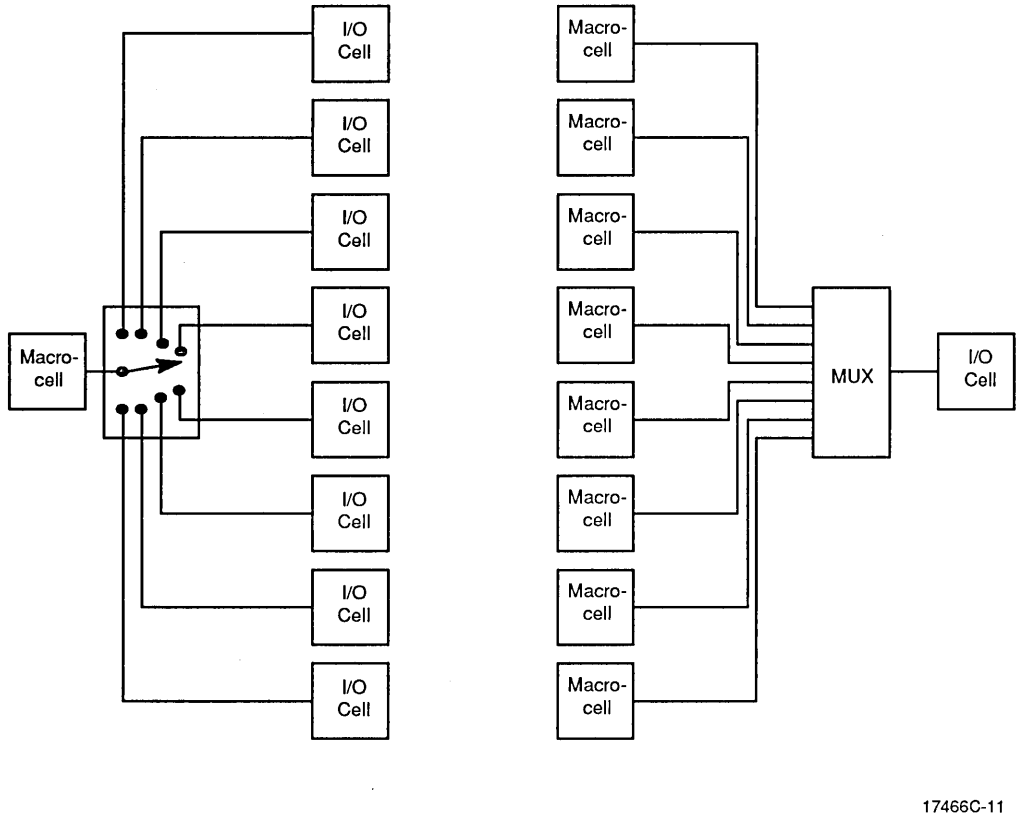
The Output Switch Matrix

The output switch matrix allows macrocells to be connected to any of several I/O cells within a PAL block. This provides high flexibility in determining pinout, and allows design changes that will not affect pinout.

On MACH 3 devices, each PAL block has the same number of macrocells as I/O cells. The output switch matrix allows the design to scramble macrocells and I/O pins within the PAL block according to Figure 11. Each I/O cell can choose from eight macrocells; each macrocell has a choice of eight I/O cells.

In MACH 4 devices, each PAL block has twice as many macrocells as I/O cells. The MACH 4 output switch matrix allows for half of the macrocells to drive I/O cells within a PAL block, in combinations according to Figure 12. Each I/O cell can choose from eight macrocells; each macrocell has a choice of four I/O cells.

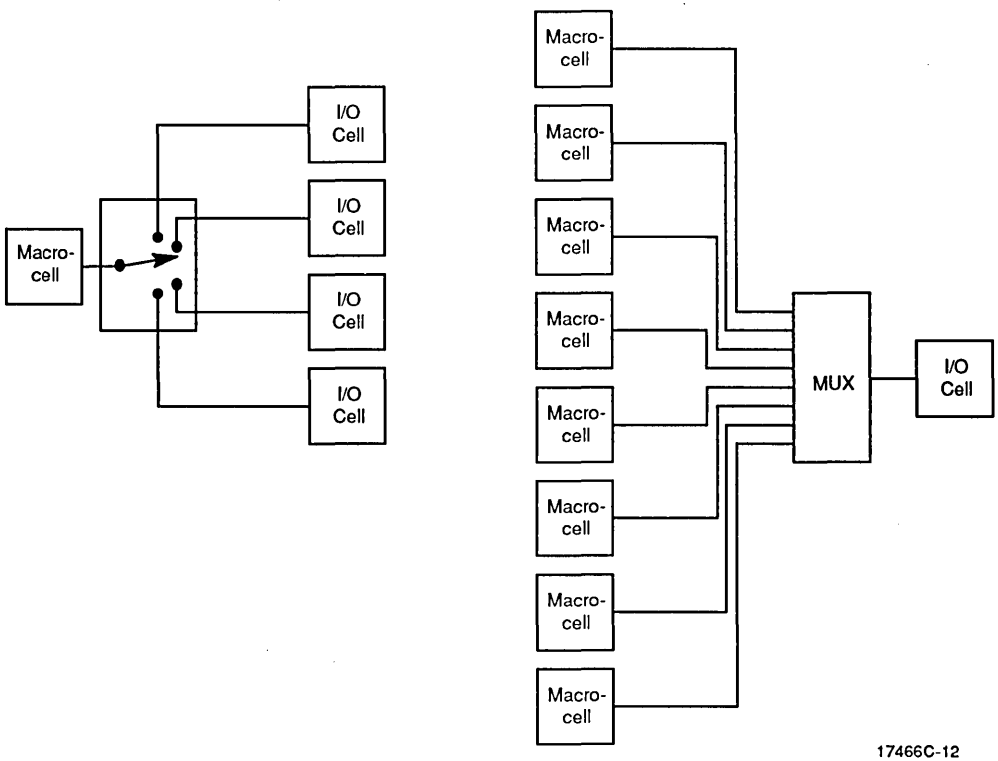
Specific combinations allowed for each device are tabulated in the individual product data sheets. No macrocell may drive more than one I/O cell.



a. Macrocell drives one of 8 I/Os

b. I/O can choose one of 8 macrocells

Figure 11. MACH 3 Output Switch Matrix



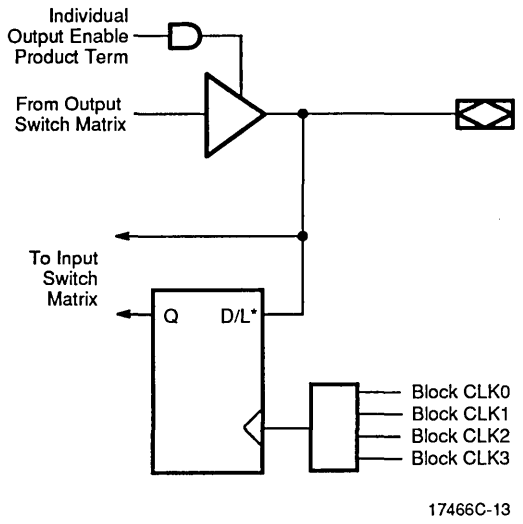
a. Macrocell drives one of 4 I/Os

b. I/O can choose one of 8 macrocells

Figure 12. MACH 4 Output Switch Matrix

The I/O Cell

The I/O cell (Figure 13) simply consists of programmable output enable, a feedback path, and for MACH 4 devices, a flip-flop. An individual output enable product term is provided for each I/O cell. The feedback signal drives the input switch matrix.



**Flip-flop available on MACH 4 devices only.*

Figure 13. I/O Cell

The MACH 4 I/O cell contains a flip-flop, which provides the capability for storing the input in a D-type register or latch. The clock can be any of the PAL block clocks. Both the direct and registered versions of the input are sent to the input switch matrix. This allows for such functions as "time-domain-multiplexed" data comparison, where the first data value is stored, and then the second data value is put on the I/O pin and compared with the previous stored value.

Note that the flip-flop used in the MACH 4 I/O cell is independent of the flip-flops in the macrocells. It powers up to a logic low.

JTAG Testability Circuit

All MACH 3 and 4 devices with greater than 84 leads have JTAG testability circuits built in. This allows functional testing of the device through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

The only device without JTAG is the MACH435, which is pin-compatible with the 84-pin MACH130 and MACH230. This device has preload and observability functions. All registers on the MACH435 can be preloaded to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

In addition to the control offered by preload, testing requires observability of the internal state of the device following a sequence of vectors. The MACH435 offers an observability feature that allows the user to send hidden buried register values to observable output pins.

5-V, In-Circuit Programmability and Erasability

Because high-pin-count PQFPs have leads that are subject to damage, 5-V, in-circuit programmability and erasability have been provided. This allows the devices to be soldered on the board prior to programming. Once on the board, the device leads are immobile, and can be programmed without damage. Because there are no "supervoltages" (voltages above the standard TTL range), devices that share lines on the board will not be damaged by high voltages. Programming is enabled by a dedicated pin; this pin is pulled high during normal operation.

Power-Up Reset/Preset

All flip-flops power up to a known state for predictable system initialization. The power-up value can be programmed through the initialization swapping selection feature. The V_{CC} rise must be monotonic and clock must be inactive until the reset delay time, 10 µs maximum, has elapsed.

Security Bit

A security bit is provided on the MACH devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. Preload and the JTAG circuitry can be used independently of the security bit, since a separate security bit is provided to disable these features. The bits can only be erased in conjunction with the array during an erase cycle.

Quality and Testability

The MACH devices offer a very high level of built-in quality. The fact that the device is erasable allows direct verification of all AC and DC parameters. In addition, this verifies complete programmability and functionality

of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The MACH devices are fabricated with AMD's advanced electrically-erasable floating-gate 0.65-µm CMOS technology. This provides the devices with performance and power consumption that are unmatched in the industry. The floating gate cells rely on Fowler-Nordheim tunneling to charge the gate, and have long proven their endurance and reliability. 20-year data retention is provided over operating conditions when devices are programmed on approved programmers.

The substrate of these devices is grounded, providing for a more efficient circuit. In addition, this provides substrate clamp diodes at all inputs, making them more immune to noisy input signals. All of the MACH 3 and MACH 4 devices have pull-up resistors on all inputs and I/O pins. While it is good design practice to tie unused pins high, the pull-up resistors allow unused pins to float safely.

MACH355-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 144 Pins in PQFP
- JTAG, 5-V, in-circuit programmable
- IEEE 1149.1 JTAG testing capability
- 96 Macrocells
- 15 ns t_{PD}
- 50 MHz f_{MAX} external
- 102 Inputs with pull-up resistors
- 96 Outputs
- 96 Flip-flops
- Up to 20 product terms per function, with XOR
- Flexible clocking
  - — Four global clock pins with selectable edges
  - — Asynchronous mode available for each macrocell
- 6 "PAL33V16" blocks
- Input and output switch matrices for high routability
- Fixed, predictable, deterministic delays

GENERAL DESCRIPTION

The MACH355 is a member of AMD's high-performance EE CMOS MACH 3 family. This device has approximately nine times the macrocell capability of the popular PAL22V10, with significant density and functional features that the PAL22V10 does not provide.

The MACH355 consists of six PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The MACH355 has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

Up to 20 product terms per function can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

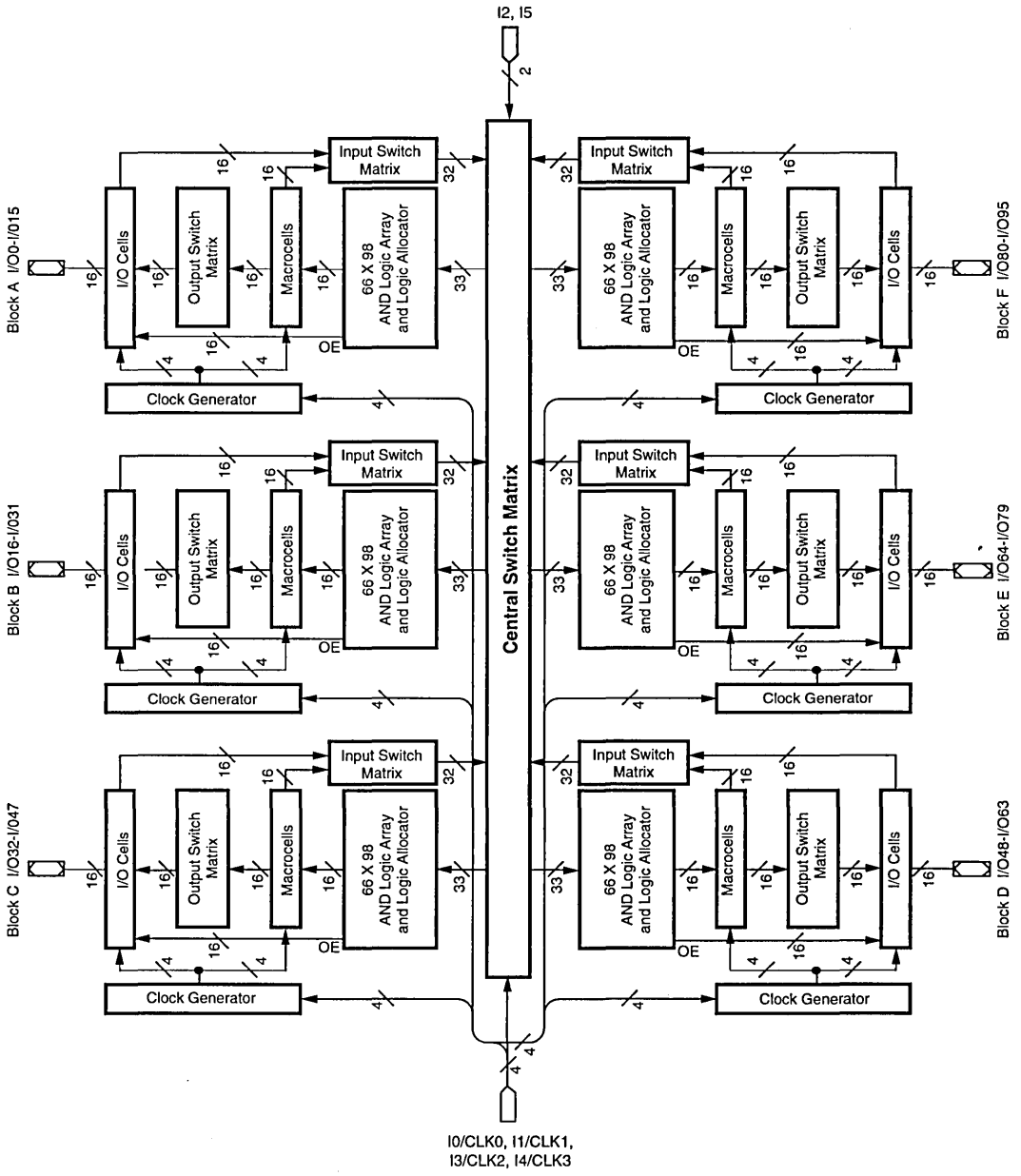
The MACH355 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer or by the software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

Publication# 17467 Rev. C Amendment/0
Issue Date: August 1994

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

BLOCK DIAGRAM



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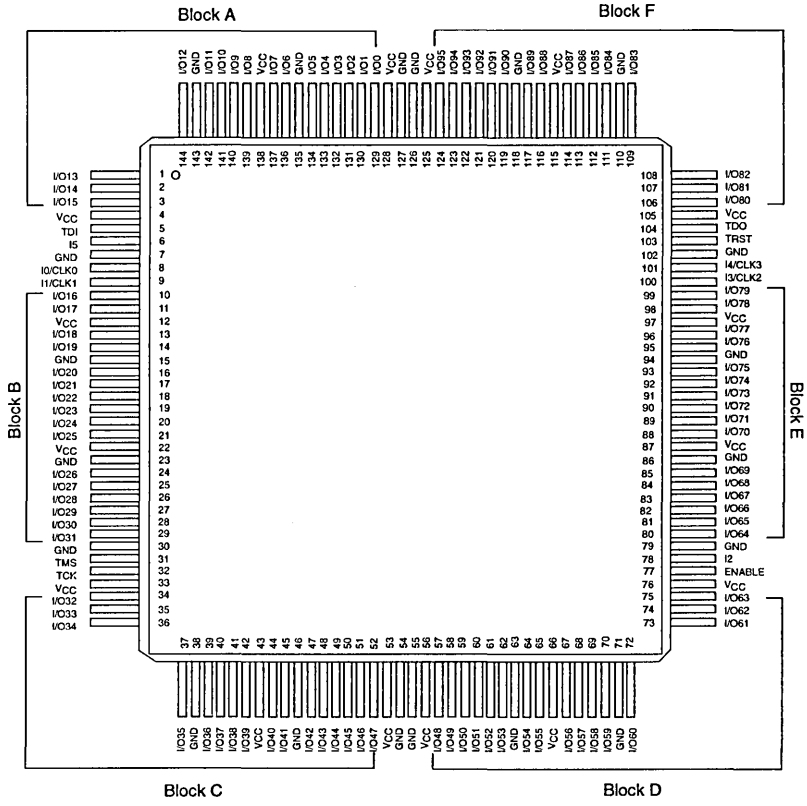
CONNECTION DIAGRAM

Top View

PQFP



17467C-2

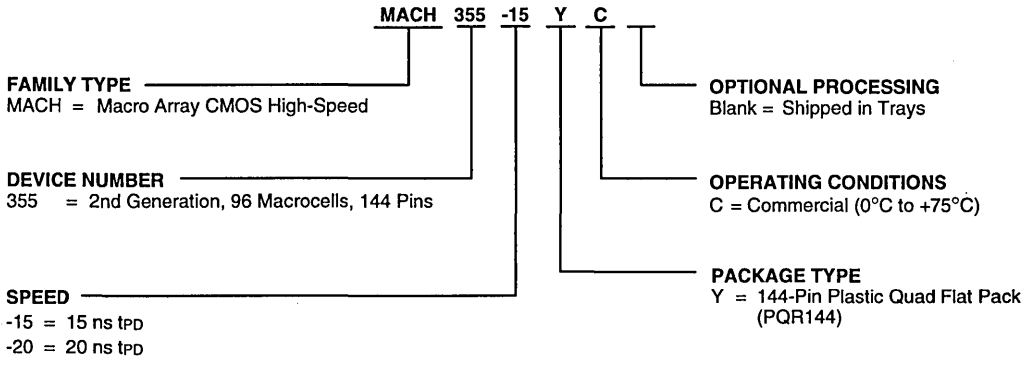
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH355-15	YC
MACH355-20	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH355 consists of six PAL blocks connected by a central switch matrix. There are 96 I/O pins and 6 dedicated input pins feeding the central switch matrix. These signals are distributed to the eight PAL blocks for efficient design implementation. There are 4 global clock pins that can also be used as dedicated inputs.

All inputs and I/O pins have built-in pull-up resistors. While it is always good design practice to tie unused pins high, the pull-up resistors provide design security and stability in the event that unused pins are left disconnected.

The PAL Blocks

Each PAL block in the MACH355 (Figure 14) contains a clock generator, a 98-product-term logic array, a logic allocator, 16 macrocells, an output switch matrix, 16 I/O cells, and an input switch matrix. The central switch matrix feeds each PAL block with 33 inputs. This makes the PAL block look effectively like an independent "PAL33V16".

In addition to the logic product terms, individual output enable product terms and two PAL block initialization product term are provided. Each I/O pin can be individually enabled. All flip-flops that are in the synchronous mode within a PAL block are initialized together by either of the PAL block initialization product terms.

The Central Switch Matrix and Input Switch Matrix

The MACH355 central switch matrix is fed by the input switch matrices in each PAL block. Each PAL block provides 16 internal feedback signals and 16 I/O pin signals to the input switch matrix. Of these 32 signals, 24 decoded signals are provided to the central switch matrix by the input switch matrix. The central switch matrix distributes these signals back to the PAL blocks in a very efficient manner that provides for high performance. The design software automatically configures the input and central switch matrices when fitting a design into the device.

The Clock Generator

Each PAL block has a clock generator that can generate four clock signals for use throughout the PAL block. These four signals are available to all macrocells and I/O cells in the PAL block, whether in synchronous or asynchronous mode. The clock generator chooses the four signals from the eight possible signals given by the true and complement versions of the four global clock pin signals.

The Product-Term Array

The MACH355 product-term array consists of 80 product terms for logic use, 16 product terms for output enable use, and two product terms for global PAL block initialization. Each macrocell has a nominal allocation of 5 product terms for logic, although the logic allocator allows for logic redistribution. Each I/O pin has its own individual output enable term. The initialization product terms provide asynchronous reset or preset to synchronous-mode macrocells in the PAL block.

The Logic Allocator

The logic allocator in the MACH355 takes the 80 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 20 product terms if in synchronous mode, or 18 product terms if in asynchronous mode. When product terms are routed away from a macrocell, it is possible to route all 5 product terms away, which precludes the use of the macrocell for logic generation; or it is possible to route only 4 product terms away, leaving one for simple function generation. The design software automatically configures the logic allocator when fitting the design into the device.

The logic allocator also provides an exclusive-OR gate. This gate allows generation of combinatorial exclusive-OR logic, such as comparison or addition. It allows registered exclusive-OR functions, such as CRC generation, to be implemented more efficiently. It also makes in possible to emulate all flip-flop types with a D-type flip-flop. Register type emulation is automatically handled by the design software.

Table 5 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 14 for cluster and macrocell numbers.

Table 5. Logic Allocation

Macrocell	Available Clusters
M0	C0, C1, C2
M1	C0, C1, C2, C3
M2	C1, C2, C3, C4
M3	C2, C3, C4, C5
M4	C3, C4, C5, C6
M5	C4, C5, C6, C7
M6	C5, C6, C7, C8
M7	C6, C7, C8, C9
M8	C7, C8, C9, C10
M9	C8, C9, C10, C11
M10	C9, C10, C11, C12
M11	C10, C11, C12, C13
M12	C11, C12, C13, C14
M13	C12, C13, C14, C15
M14	C13, C14, C15
M15	C14, C15

The Macrocell and Output Switch Matrix

The MACH355 has 16 macrocells, half of which can drive I/O pins; this selection is made by the output switch matrix. Each macrocell can drive one of four I/O cells. The allowed combinations are shown in Table 6. Please refer to Figure 14 for macrocell and I/O pin numbers.

Table 6. Output Switch Matrix Combinations

Macrocell	Routable to I/O Pins
M0, M1 M2, M3 M4, M5 M6, M7	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7
M8, M9 M10, M11 M12, M13 M14, M15	I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15
I/O Pin	**Available Macrocells**
I/O0	M0, M1, M2, M3, M4, M5, M6, M7
I/O1	M1, M2, M3, M4, M5, M6, M7, M0
I/O2	M2, M3, M4, M5, M6, M7, M0, M1
I/O3	M3, M4, M5, M6, M7, M0, M1, M2
I/O4	M4, M5, M6, M7 M0, M1, M2, M3
I/O5	M5, M6, M7, M0, M1, M2, M3, M4
I/O6	M6, M7, M0, M1, M2, M3, M4, M5
I/O7	M7, M0, M1, M2, M3, M4, M5, M6
I/O8	M8, M9, M10, M11, M12, M13, M14, M15
I/O9	M9, M10, M11, M12, M13, M14, M15, M8
I/O10	M10, M11, M12, M13, M14, M15, M8, M9
I/O11	M11, M12, M13, M14, M15, M8, M9, M10
I/O12	M12, M13, M14, M15, M8, M9, M10, M11
I/O13	M13, M14, M15, M8, M9, M10, M11, M12
I/O14	M14, M15, M8, M9, M10, M11, M12, M13
I/O15	M15, M8, M9, M10, M11, M12, M13, M14

The macrocells can be configured as registered, latched, or combinatorial. In combination with the logic allocator, the registered configuration can be any of the standard flip-flop types. The macrocell provides internal feedback whether configured with or without the flip-flop, and whether or not the macrocell drives an I/O cell.

The flip-flop clock depends on the mode selected for the macrocell. In synchronous mode, any of the PAL block clocks generated by the Clock Generator can be used. In asynchronous mode, the additional choice of either edge of an individual product-term clock is available.

Initialization can be handled as part of a bank of macrocells via the PAL block initialization terms if in synchronous mode, or individually if in asynchronous mode. In synchronous mode, one of the PAL block product terms is available each for preset and reset. The swap function determines which product term drives which function. This allows initialization polarity compatibility with the MACH 1 and 2 series. In asynchronous mode, one product term can be used either to drive reset or preset.

The I/O Cell

The I/O cell in the MACH355 consists of a three-state buffer and an input flip-flop. The I/O cell is driven by one of the macrocells, as selected by the output switch matrix. Each I/O cell can take its input from one of eight macrocells. The three-state buffer is controlled by an individual product term. The direct I/O signal is available to the input switch matrix, and can be used if desired.

JTAG Testing

JTAG is the commonly used acronym for the IEEE Standard 1149.1–1990. The JTAG standard defines input and output pins, logic control functions, and instructions. AMD has incorporated this standard into the MACH355 device.

The JTAG standard was developed as a means of providing both board-level and device-level testing. Details on this feature can be found in the application note titled, *Introduction to JTAG and Five-Volt Programming with MACH 3 and 4 Devices,* at the end of this Data Book.

Five-Volt Programming

Another benefit from the JTAG circuitry that AMD has derived is the ability to use the JTAG port for five-volt programming. This allows the device to be soldered to the board before programming. Once the device is attached, the delicate Plastic Quad Flat Pack, or PQFP, leads are protected from programming and testing operations that could potentially damage them. Programming and verification of the device is done serially which is ideal for on-board programming since it only requires the use of the Test Access Port, along with the additional ENABLE* pin.

Details on this feature can also be found in the *Introduction to JTAG and Five-Volt Programming with MACH 3 and 4 Devices* application note, at the end of this Data Book.

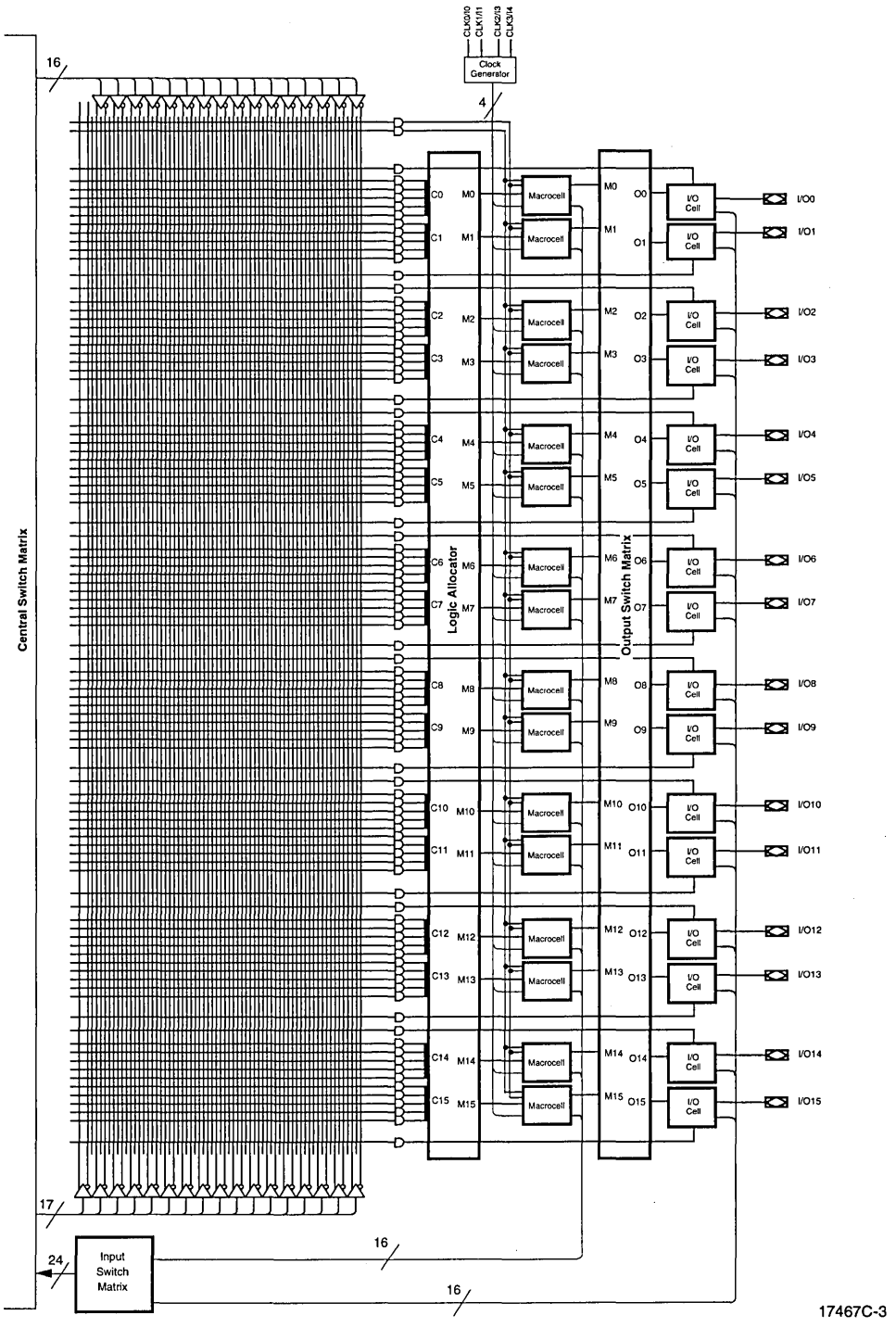


Figure 14. MACH355 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} +0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} +0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +75°C) ..... 200 mA

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	PRELIMINARY Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f =25 MHz, T_A = 25°C (Note 5)		225		mA

CAPACITANCE (Note 6)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset. An actual I_{CC} value can be calculated by using the "Typical Dynamic I_{CC} Characteristics" Chart towards the end of this data sheet.*
6. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				PRELIMINARY -15 Min	-15 Max	-20 Min	-20 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 2)				3	15	3	20	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	8		10		ns
				T-type	9		11		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				8		10		ns
t_{COA}	Product Term Clock to Output (Note 2)				4	18	4	22	ns
t_{WLA}	Product Term, Clock Width			LOW	9		12		ns
t_{WHA}				HIGH	9		12		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 3)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	38.5		31.2		MHz
				T-type	37		30.3		MHz
		Internal Feedback (f_{CNTA})		D-type	47.6		37		MHz
				T-type	45.4		35.7		MHz
		No Feedback (Note 4)	$1/(t_{WLA} + t_{WHA})$		55.6		41.7		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	10		13		ns
				T-type	11		14		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		ns
t_{COS}	Global Clock to Output (Note 2)				2	10	2	12	ns
t_{WLS}	Global Clock Width			LOW	6		8		ns
t_{WHS}				HIGH	6		8		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 3)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	50		40		MHz
				T-type	47.6		38.5		MHz
		Internal Feedback (f_{CNTS})		D-type	66.6		50		MHz
				T-type	62.5		47.6		MHz
		No Feedback (Note 4)	$1/(t_{WLS} + t_{WHS})$		83.3		62.5		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				8		10		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				8		10		ns
t_{GOA}	Product Term Gate to Output (Note 2)					19		22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				9		12		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate				10		13		ns
t_{HLS}	Latch Data Hold Time Using Global Gate				0		0		ns
t_{GOS}	Gate to Output (Note 2)					11		12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				6		8		ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

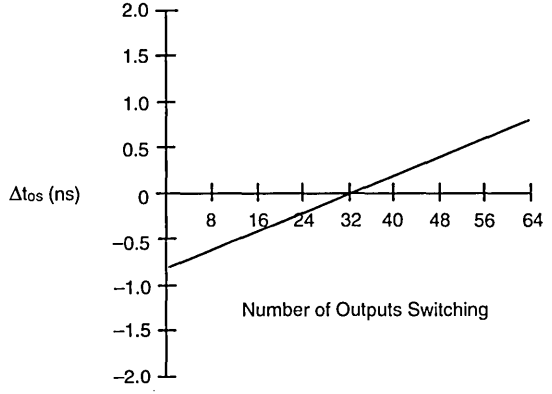
Parameter Symbol	Parameter Description	PRELIMINARY -15 Min	-15 Max	-20 Min	-20 Max	Unit
t_{AR}	Asynchronous Reset to Registered or Latched Output		20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 3)	15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)	15		20		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output		20		25	ns
t_{APW}	Asynchronous Preset Width (Note 3)	15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 3)	15		20		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 2)	2	15	2	20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 2)	2	15	2	20	ns

Notes:

1. *See Switching Test Circuit at the end of this Data Book for test conditions.*
2. *Parameters measured with 32 outputs switching.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

TYPICAL SWITCHING CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C. These parameters are not tested.



17467C-4

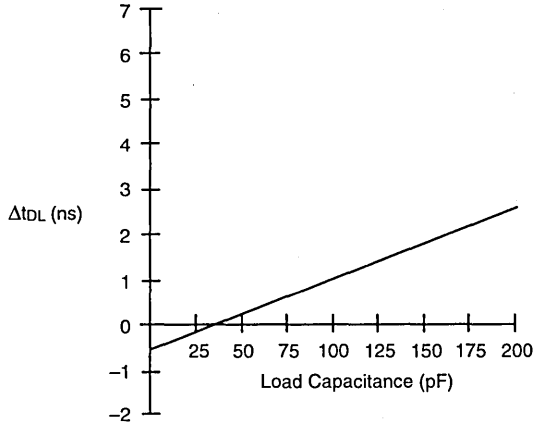
Derating for Number of Outputs Switching

Notes:

Applies to t_{PD}, t_{CO}. Calculate as:

$t_{derated} = t_{32O/P} + \Delta t_{OS}$

Datasheet numbers ($t_{32O/P}$) are specified at 32 outputs switching



17467C-5

Capacitive Load Derating

Notes:

Applies to all AC specifications and rise and fall times. Calculate as:

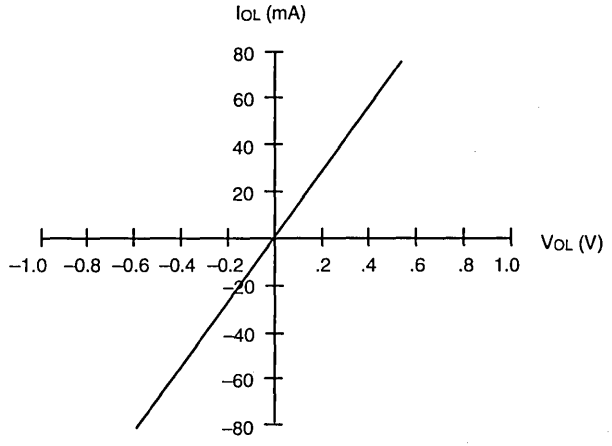
$t_{derated} = t_{35pF} + \Delta t_{DL}$

Datasheet numbers (t_{35pF}) are specified with 35 pF.

For typical rise and fall rates, use 1V/ns at 35 pF.

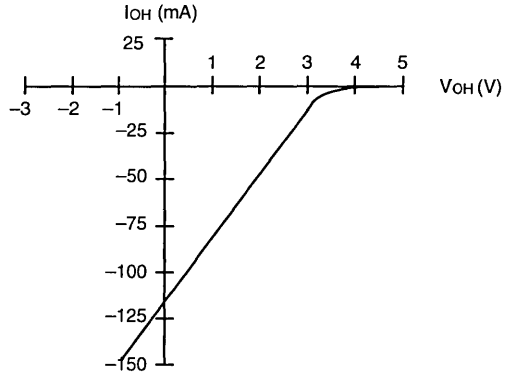
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



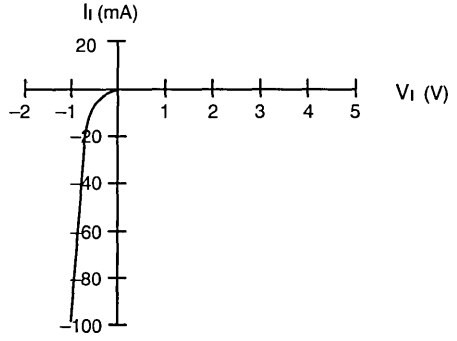
17467C-6

Output, LOW



17467C-7

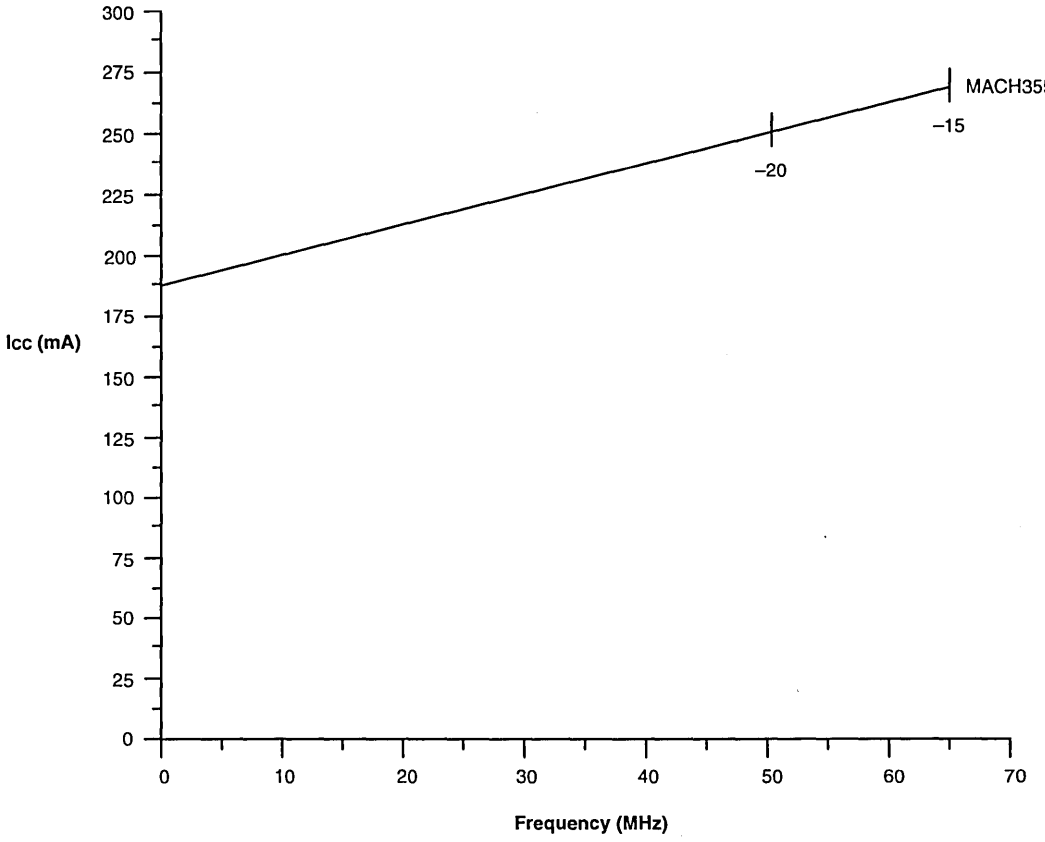
Output, HIGH



17467C-8

Input

TYPICAL I_{CC} CHARACTERISTICS
V_{CC} = 5 V, T_A = 25°C



The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Actual I_{CC} values vary with the selected pattern. An actual I_{CC} value can be calculated using the "Typical Dynamic I_{CC} Characteristics" chart towards the end of this datasheet.

Maximum frequency shown uses internal feedback and a D-type register.

TYPICAL DYNAMIC I_{CC} CHARACTERISTICS

These parameters are not tested. Please refer to the General Information section for a discussion on the usage of these parameters.

Parameter Symbol	Parameter Description	Typ	Units
i_{CCO}	Base static I_{CC}	190	mA
i_I	Incremental input current	32	µA/MHz
i_B	Incremental current per PAL block	30	µA/MHz
i_O	Incremental output current	110	µA/MHz
i_V	Voltage dependence	38	%/V
i_T	Temperature dependence	–0.13	%/°C

TYPICAL DATA DESIGN GUIDELINES

The following parameters are provided in response to questions from designers. They are intended only as design guidelines, and should be used with care. They are not guaranteed or tested.

Parameter Description	Typ	Units
Edge Rates (Note 1)		
Rise rate	1	V/ns
Fall rate	1	V/ns
Skew (Note 2)		
Global clock-to-output skew, same clock polarity and same output polarity	1	ns
Global clock-to-output skew, same clock polarity only	2	ns
Global clock-to-output skew, same output polarity only	2	ns
Global clock-to-output skew, different clock polarity and different output polarity	3	ns
Internal Delay Savings (Note 3)		
Propagation delay savings	2	ns
Clock-to-output delay savings	3	ns
Ground Bounce (Note 4)		
Ground bounce noise level on low output	0.5	V

Notes:

1. *Rise and fall rates are for unloaded outputs.*
2. *Skew values assume equal output loading.*
3. *Internal delay savings gives the typical amount of delay saved by not going through an output buffer.*
4. *The ground bounce noise level should be added to the static V_{OL} under normal load conditions as applied to a silent low output when all other I/O pins are switching from high to low.*

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PQFP	Unit
θ_{jc}	Thermal impedance, junction to case		7	°C/W
θ_{ja}	Thermal impedance, junction to ambient		25	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	21	°C/W
		400 lfpm air	18	°C/W
		600 lfpm air	16	°C/W
		800 lfpm air	15	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

MACH435-15/20, Q-25

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 84 Pins in PLCC
- 128 Macrocells
- 15 ns t_{PD}
- 50 MHz f_{MAX} external
- 70 Inputs with pull-up resistors
- 64 Outputs
- 192 Flip-flops
  - — 128 Macrocell flip-flops
  - — 64 Input flip-flops
- Up to 20 product terms per function, with XOR
- Flexible clocking
  - — Four global clock pins with selectable edges
  - — Asynchronous mode available for each macrocell
- 8 "PAL33V16" blocks
- Input and output switch matrices for high routability
- Fixed, predictable, deterministic delays
- Pin compatible with MACH130, MACH230

GENERAL DESCRIPTION

The MACH435 is a member of AMD's high-performance EE CMOS MACH 4 family. This device has approximately twelve times the macrocell capability of the popular PAL22V10, with significant density and functional features that the PAL22V10 does not provide.

The MACH435 consists of eight PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The MACH435 has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

Up to 20 product terms per function can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

The MACH435 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer or by the software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

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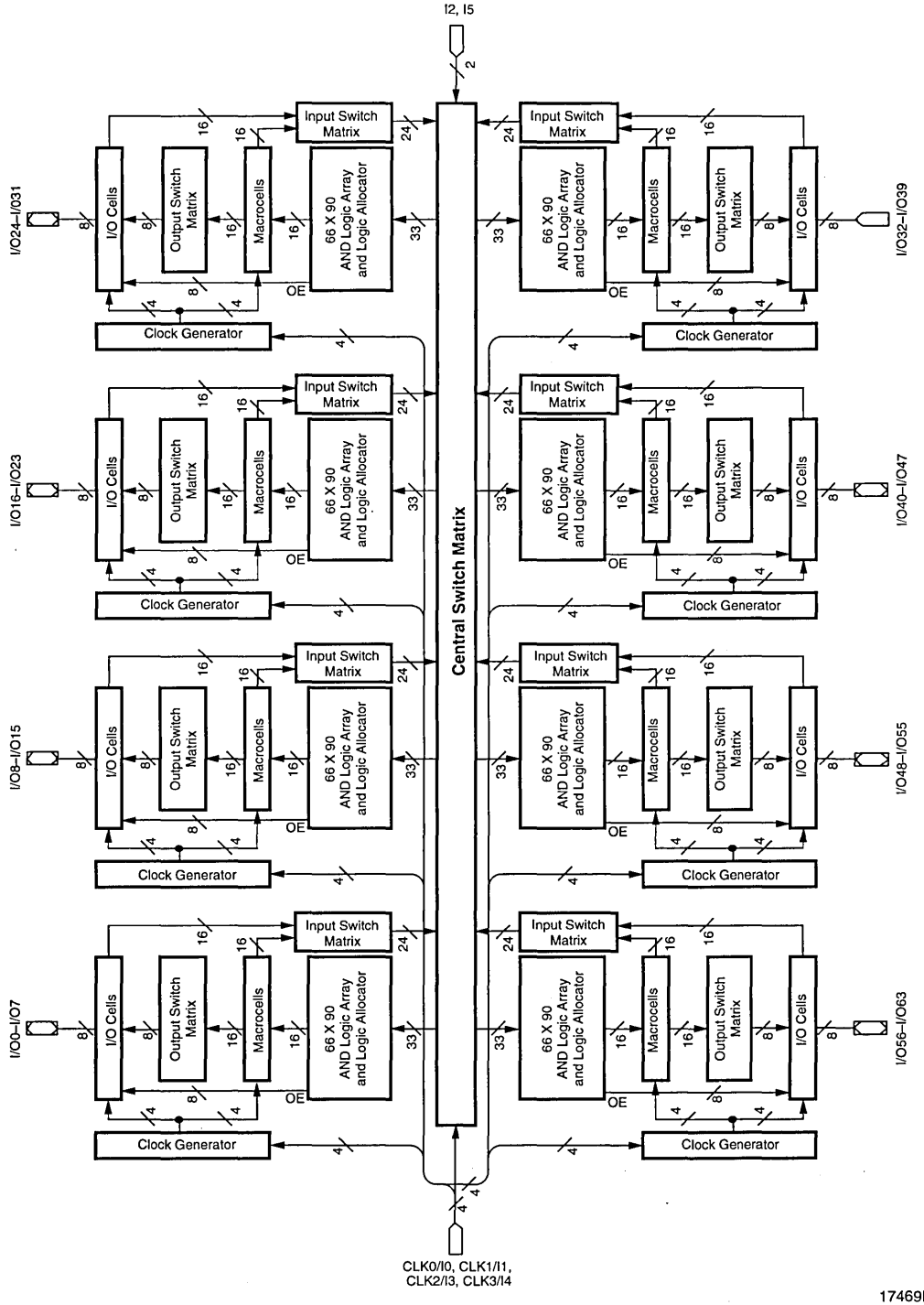
Issue Date: August 1994

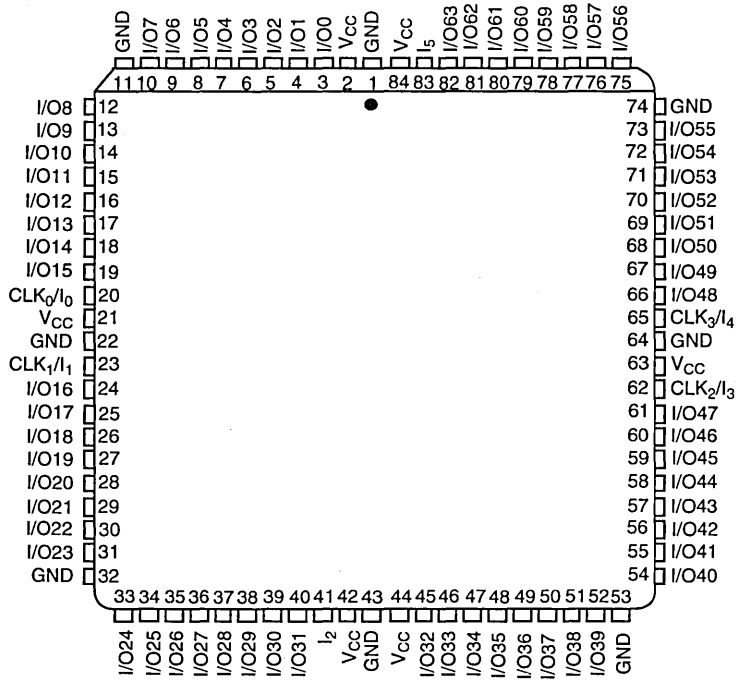
BLOCK DIAGRAM



17469D-1

CONNECTION DIAGRAM
Top View

PLCC



17469D-2

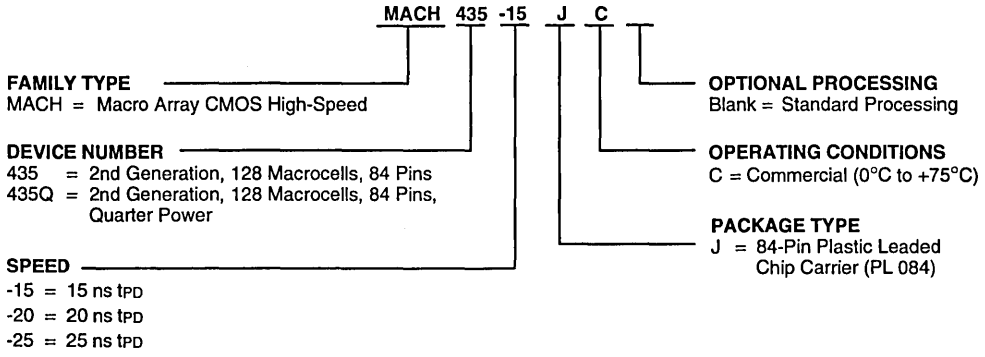
Note:
Pin-compatible with MACH130, MACH230

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION
Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH435-15	JC
MACH435-20	
MACH435Q-25	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH435 consists of eight PAL blocks connected by a central switch matrix. There are 64 I/O pins and 6 dedicated input pins feeding the central switch matrix. These signals are distributed to the eight PAL blocks for efficient design implementation. There are 4 global clock pins that can also be used as dedicated inputs.

All inputs and I/O pins have built-in pull-up resistors. While it is always good design practice to tie unused pins high, the pull-up resistors provide design security and stability in the event that unused pins are left disconnected.

The PAL Blocks

Each PAL block in the MACH435 (Figure 15) contains a clock generator, a 90-product-term logic array, a logic allocator, 16 macrocells, an output switch matrix, 8 I/O cells, and an input switch matrix. The central switch matrix feeds each PAL block with 33 inputs. This makes the PAL block look effectively like an independent "PAL33V16" with 8 to 16 buried macrocells.

In addition to the logic product terms, individual output enable product terms and two PAL block initialization product term are provided. Each I/O pin can be individually enabled. All flip-flops that are in the synchronous mode within a PAL block are initialized together by either of the PAL block initialization product terms.

The Central Switch Matrix and Input Switch Matrix

The MACH435 central switch matrix is fed by the input switch matrices in each PAL block. Each PAL block provides 16 internal feedback signals, 8 registered input signals, and 8 I/O pin signals to the input switch matrix. Of these 32 signals, 24 decoded signals are provided to the central switch matrix by the input switch matrix. The central switch matrix distributes these signals back to the PAL blocks in a very efficient manner that provides for high performance. The design software automatically configures the input and central switch matrices when fitting a design into the device.

The Clock Generator

Each PAL block has a clock generator that can generate four clock signals for use throughout the PAL block. These four signals are available to all macrocells and I/O cells in the PAL block, whether in synchronous or asynchronous mode. The clock generator chooses the four signals from the eight possible signals given by the true and complement versions of the four global clock pin signals.

The Product-Term Array

The MACH435 product-term array consists of 80 product terms for logic use, eight product terms for output enable use, and two product terms for global PAL block initialization. Each macrocell has a nominal allocation of 5 product terms for logic, although the logic allocator allows for logic redistribution. Each I/O pin has its own individual output enable term. The initialization product terms provide asynchronous reset or preset to synchronous-mode macrocells in the PAL block.

The Logic Allocator

The logic allocator in the MACH435 takes the 80 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 20 product terms if in synchronous mode, or 18 product terms if in asynchronous mode. When product terms are routed away from a macrocell, it is possible to route all 5 product terms away, which precludes the use of the macrocell for logic generation; or it is possible to route only 4 product terms away, leaving one for simple function generation. The design software automatically configures the logic allocator when fitting the design into the device.

The logic allocator also provides an exclusive-OR gate. This gate allows generation of combinatorial exclusive-OR logic, such as comparison or addition. It allows registered exclusive-OR functions, such as CRC generation, to be implemented more efficiently. It also makes in possible to emulate all flip-flop types with a D-type flip-flop. Register type emulation is automatically handled by the design software.

Table 7 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 15 for cluster and macrocell numbers.

Table 7. Logic Allocation

Macrocell	Available Clusters
M0	C0, C1, C2
M1	C0, C1, C2, C3
M2	C1, C2, C3, C4
M3	C2, C3, C4, C5
M4	C3, C4, C5, C6
M5	C4, C5, C6, C7
M6	C5, C6, C7, C8
M7	C6, C7, C8, C9
M8	C7, C8, C9, C10
M9	C8, C9, C10, C11
M10	C9, C10, C11, C12
M11	C10, C11, C12, C13
M12	C11, C12, C13, C14
M13	C12, C13, C14, C15
M14	C13, C14, C15
M15	C14, C15

The Macrocell and Output Switch Matrix

The MACH435 has 16 macrocells, half of which can drive I/O pins; this selection is made by the output switch matrix. Each macrocell can drive one of four I/O cells. The allowed combinations are shown in Table 8. Please refer to Figure 15 for macrocell and I/O pin numbers.

Table 8. Output Switch Matrix Combinations

Macrocell	Routable to I/O Pins
M0, M1	I/O5, I/O6, I/O7, I/O0
M2, M3	I/O6, I/O7, I/O0, I/O1
M4, M5	I/O7, I/O0, I/O1, I/O2
M6, M7	I/O0, I/O1, I/O2, I/O3
M8, M9	I/O1, I/O2, I/O3, I/O4
M10, M11	I/O2, I/O3, I/O4, I/O5
M12, M13	I/O3, I/O4, I/O5, I/O6
M14, M15	I/O4, I/O5, I/O6, I/O7
I/O Pin	**Available Macrocells**
I/O0	M0, M1, M2, M3, M4, M5, M6, M7
I/O1	M2, M3, M4, M5, M6, M7, M8, M9
I/O2	M4, M5, M6, M7, M8, M9, M10, M11
I/O3	M6, M7, M8, M9, M10, M11, M12, M13
I/O4	M8, M9, M10, M11, M12, M13, M14, M15
I/O5	M10, M11, M12, M13, M14, M15, M0, M1
I/O6	M12, M13, M14, M15, M0, M1, M2, M3
I/O7	M14, M15, M0, M1, M2, M3, M4, M5

The macrocells can be configured as registered, latched, or combinatorial. In combination with the logic allocator, the registered configuration can be any of the standard flip-flop types. The macrocell provides internal feedback whether configured with or without the flip-flop, and whether or not the macrocell drives an I/O cell.

The flip-flop clock depends on the mode selected for the macrocell. In synchronous mode, any of the PAL block clocks generated by the Clock Generator can be used. In asynchronous mode, the additional choice of either edge of an individual product-term clock is available.

Initialization can be handled as part of a bank of macrocells via the PAL block initialization terms if in synchronous mode, or individually if in asynchronous mode. In synchronous mode, one of the PAL block product terms is available each for preset and reset. The swap function determines which product term drives which function. This allows initialization polarity compatibility with the MACH 1 and 2 series. In asynchronous mode, one product term can be used either to drive reset or preset.

The I/O Cell

The I/O cell in the MACH435 consists of a three-state buffer and an input flip-flop. The I/O cell is driven by one of the macrocells, as selected by the output switch matrix. Each I/O cell can take its input from one of eight macrocells. The three-state buffer is controlled by an individual product term. The input flip-flop can be configured as a register or latch. Both the direct I/O signal and the registered/latched signal are available to the input switch matrix, and can be used simultaneously if desired.

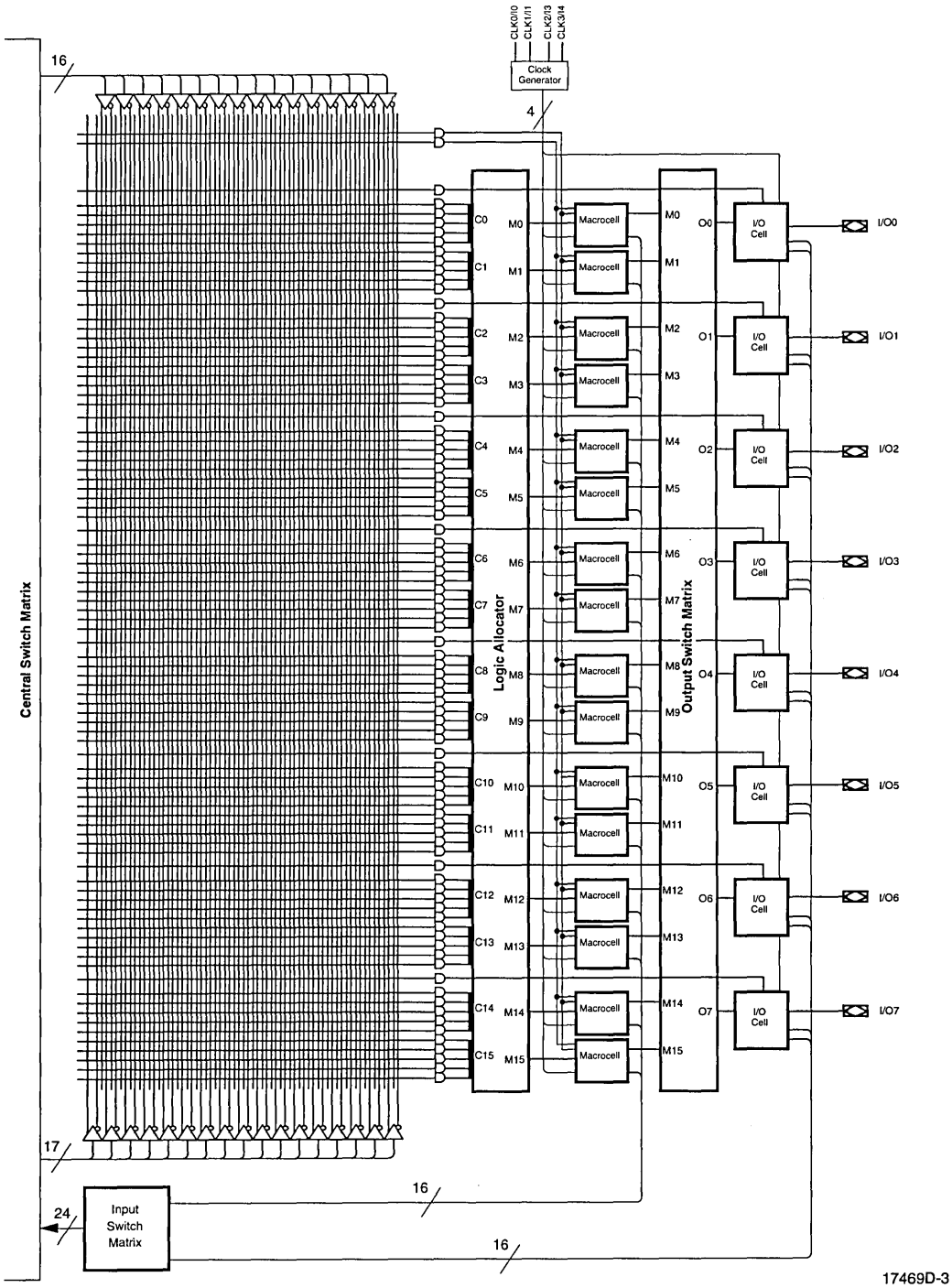


Figure 15. MACH435 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} +0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} +0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +75°C) ..... 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f =25 MHz, T_A = 25°C (Note 5)		255		mA

CAPACITANCE (Note 6)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL Block and capable of being loaded, enabled, and reset. An actual I_{CC} value can be calculated by using the "Typical Dynamic I_{CC} Characteristics" Chart towards the end of this data sheet.*
6. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				-15		-20		Unit
					Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 2)				3	15	3	20	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	8		10		ns
				T-type	9		11		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				8		10		ns
t_{COA}	Product Term Clock to Output (Note 2)				4	18	4	22	ns
t_{WLA}	Product Term, Clock Width			LOW	9		12		ns
t_{WHA}				HIGH	9		12		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 3)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	38.5		31.2		MHz
				T-type	37		30.3		MHz
		Internal Feedback (f_{CNTA})		D-type	47.6		37		MHz
				T-type	45.4		35.7		MHz
		No Feedback (Note 4)	$1/(t_{WLA} + t_{WHA})$		55.6		41.7		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	10		13		ns
				T-type	11		14		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		ns
t_{COS}	Global Clock to Output (Note 2)				2	10	2	12	ns
t_{WLS}	Global Clock Width			LOW	6		8		ns
t_{WHS}				HIGH	6		8		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 3)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	50		40		MHz
				T-type	47.6		38.5		MHz
		Internal Feedback (f_{CNTS})		D-type	66.6		50		MHz
				T-type	62.5		47.6		MHz
		No Feedback (Note 4)	$1/(t_{WLS} + t_{WHS})$		83.3		62.5		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				8		10		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				8		10		ns
t_{GOA}	Product Term Gate to Output (Note 2)					19		22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				9		12		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate				10		13		ns
t_{HLS}	Latch Data Hold Time Using Global Gate				0		0		ns
t_{GOS}	Gate to Output (Note 2)					11		12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				6		8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					17		22	ns
t_{SIR}	Input Register Setup Time				2		2		ns
t_{HIR}	Input Register Hold Time				4		5		ns
t_{ICO}	Input Register Clock to Combinatorial Output					20		25	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

Parameter Symbol	Parameter Description		-15		-20		Unit
			Min	Max	Min	Max	
t_{ICS}	Input Register Clock to Output Register Setup	D-type	15		20		ns
		T-type	16		21		ns
t_{WICL}	Input Register Clock Width	LOW	6		8		ns
t_{WICH}		HIGH	6		8		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	83.3		62.5		MHz
t_{SIL}	Input Latch Setup Time		2		2		ns
t_{HIL}	Input Latch Hold Time		4		5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output			20		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			22		27	ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Latch Gate		10		12		ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		14		19		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Global Output Latch Gate		12		16		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		16		21		ns
t_{WIGL}	Input Latch Gate Width LOW		6		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			19		24	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 3)		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)		15		20		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			20		25	ns
t_{APW}	Asynchronous Preset Width (Note 3)		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 3)		15		20		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 2)		2	15	2	20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 2)		2	15	2	20	ns

Notes:

1. *See Switching Test Circuit at the end of this Data Book for test conditions.*
2. *Parameters measured with 32 outputs switching.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} +0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} +0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +75°C) ..... 200 mA

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f=25 MHz, T_A = 25°C, (Note 5)		115		mA

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL Block and capable of being loaded, erased, and reset. An actual I_{CC} value can be calculated by using the "Typical Dynamic I_{CC} Characteristics" Chart towards the end of the this data sheet.*
6. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				-25 Min	-25 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 2)				3	25	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	18		ns
				T-type	19		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				18		ns
t_{COA}	Product Term Clock to Output (Note 2)				4	28	ns
t_{WLA}	Product Term, Clock Width			LOW	19		ns
t_{WHA}				HIGH	19		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 3)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	21.7		MHz
				T-type	21.3		MHz
		Internal Feedback (f_{CNTA})		D-type	24.4		MHz
				T-type	23.8		MHz
		No Feedback (Note 4)	$1/(t_{WLA} + t_{WHA})$		26.3		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	20		ns
				T-type	21		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		ns
t_{COS}	Global Clock to Output (Note 2)				2	12	ns
t_{WLS}	Global Clock Width			LOW	8		ns
t_{WHS}				HIGH	8		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 3)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	31.3		MHz
				T-type	30.3		MHz
		Internal Feedback (f_{CNTS})		D-type	37		MHz
				T-type	35.7		MHz
		No Feedback (Note 4)	$1/(t_{SS} + t_{HS})$		50		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				18		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				18		ns
t_{GOA}	Product Term Gate to Output (Note 2)					29	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				19		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate				20		ns
t_{HLS}	Latch Data Hold Time Using Global Gate				0		ns
t_{GOS}	Gate to Output (Note 2)					21	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				8		ns
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input or Output Latch					27	ns
t_{SIR}	Input Register Setup Time				5		ns
t_{HIR}	Input Register Hold Time				5		ns
t_{ICO}	Input Register Clock to Combinatorial Output					30	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

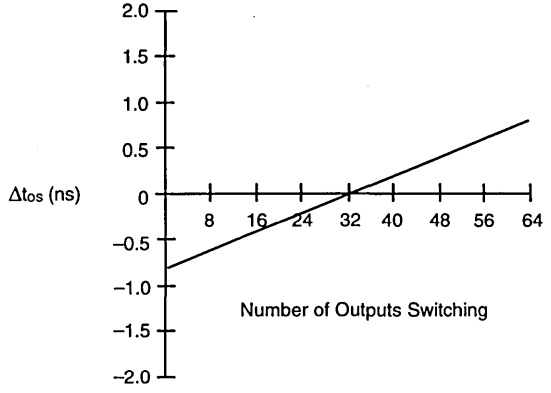
Parameter Symbol	Parameter Description		-25 Min	-25 Max	Unit
t_{ICS}	Input Register Clock to Output Register Setup	D-type	25		ns
		T-type	26		ns
t_{WICL}	Input Register Clock Width	LOW	8		ns
t_{WICH}		HIGH	8		ns
f_{MAXIR}	Maximum Input Register Frequency | $1/(t_{WICL} + t_{WICH})$		62.5		MHz
t_{SIL}	Input Latch Setup Time		5		ns
t_{HIL}	Input Latch Hold Time		5		ns
t_{IGO}	Input Latch Gate to Combinatorial Output			30	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			32	ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Latch Gate		20		ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		24		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Global Output Latch Gate		22		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		26		ns
t_{WIGL}	Input Latch Gate Width LOW or HIGH		8		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			29	ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			30	ns
t_{ARW}	Asynchronous Reset Width (Note 3)		25		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)		25		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			30	ns
t_{APW}	Asynchronous Preset Width (Note 3)		25		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 3)		25		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 2)		2	25	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 2)		2	25	ns

Notes:

1. *See Switching Test Circuit at the end of this Data Book for test conditions.*
2. *Parameters measured with 32 outputs switching.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

TYPICAL SWITCHING CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C. These parameters are not tested.



17469D-4

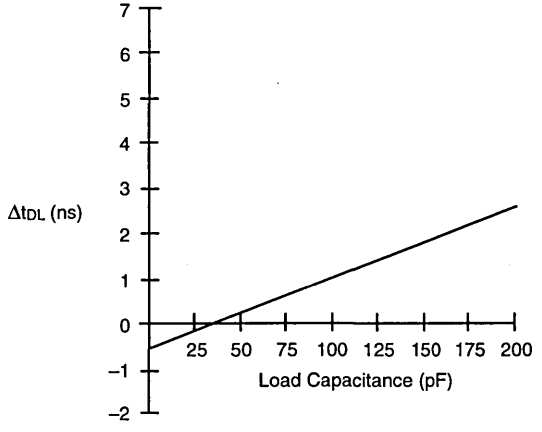
Derating for Number of Outputs Switching

Notes:

Applies to t_{PD}, t_{CO}. Calculate as:

$t_{derated} = t_{32O/P} + \Delta t_{OS}$

Datasheet numbers ($t_{32O/P}$) are specified at 32 outputs switching



17469D-5

Capacitive Load Derating

Notes:

Applies to all AC specifications and rise and fall times. Calculate as:

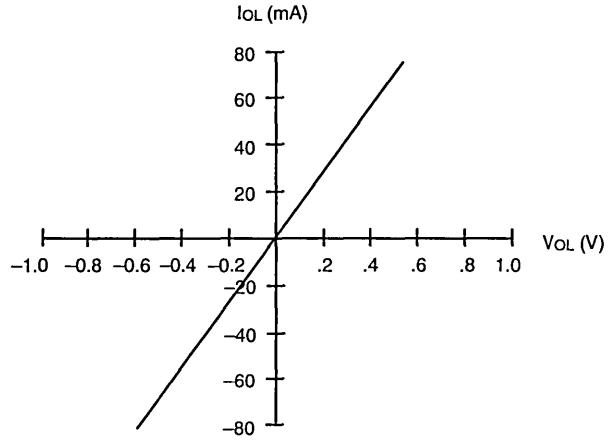
$t_{derated} = t_{35pF} + \Delta t_{DL}$

Datasheet numbers (t_{35pF}) are specified with 35 pF.

For typical rise and fall rates, use 1V/ns at 35 pF.

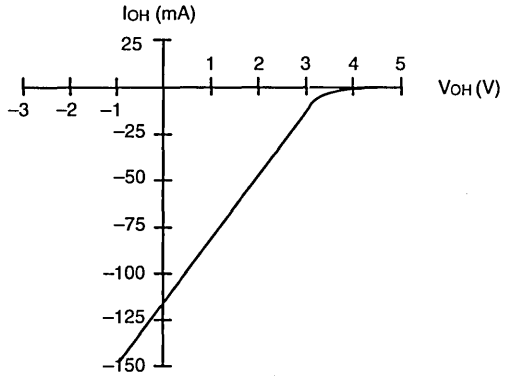
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



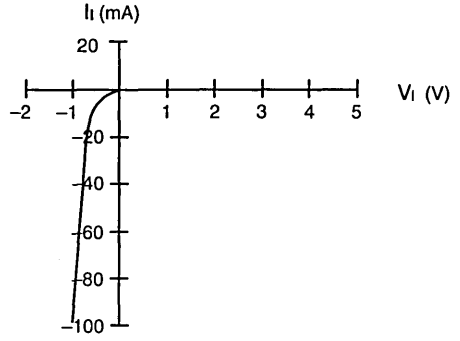
17469D-6

Output, LOW



17469D-7

Output, HIGH

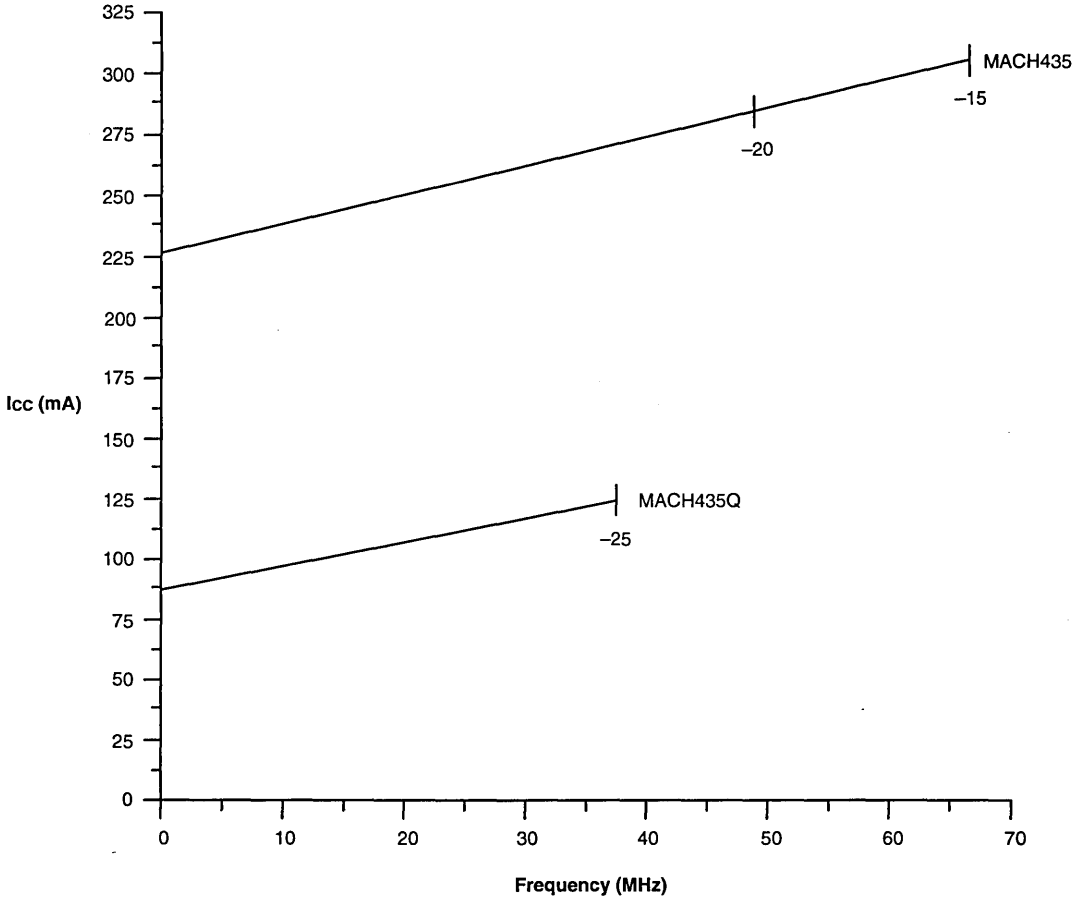


17469D-8

Input

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C



The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Actual I_{CC} values vary with the selected pattern. An actual I_{CC} value can be calculated using the "Typical Dynamic I_{CC} Characteristics" chart towards the end of this datasheet.

Maximum frequency shown uses internal feedback and a D-type register.

TYPICAL DYNAMIC I_{CC} CHARACTERISTICS

These parameters are not tested. Please refer to the General Information section for a discussion on the usage of these parameters.

Parameter Symbol	Parameter Description		Typ	Unit
I_{CCO}	Base static I_{CC}		255	mA
		Q	90	
i_I	Incremental input current		32	µA/MHz
i_B	Incremental current per PAL block		30	µA/MHz
i_O	Incremental output current		110	µA/MHz
i_V	Voltage dependence		38	%/V
i_T	Temperature dependence		–0.13	%/°C

TYPICAL DATA DESIGN GUIDELINES

The following parameters are provided in response to questions from designers. They are intended only as design guidelines, and should be used with care. They are not guaranteed or tested.

Parameter Description	Typ	Unit
Edge Rates (Note 1)		
Rise rate	1	V/ns
Fall rate	1	V/ns
Skew (Note 2)		
Global clock-to-output skew, same clock polarity and same output polarity	1	ns
Global clock-to-output skew, same clock polarity only	2	ns
Global clock-to-output skew, same output polarity only	2	ns
Global clock-to-output skew, different clock polarity and different output polarity	3	ns
Internal Delay Savings (Note 3)		
Propagation delay savings	2	ns
Clock-to-output delay savings	3	ns
Ground Bounce (Note 4)		
Ground bounce noise level on low output	0.5	V

Notes:

1. *Rise and fall rates are for unloaded outputs.*
2. *Skew values assume equal output loading.*
3. *Internal delay savings gives the typical amount of delay saved by not going through an output buffer.*
4. *The ground bounce noise level should be added to the static V_{OL} under normal load conditions as applied to a silent low output when all other I/O pins are switching from high to low.*

TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PLCC	Unit
θ_{jc}	Thermal impedance, junction to case		5	°C/W
θ_{ja}	Thermal impedance, junction to ambient		20	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	17	°C/W
		400 lfpm air	14	°C/W
		600 lfpm air	12	°C/W
		800 lfpm air	10	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

MACH445-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **100-pin version of the MACH435 in PQFP**
- **5 V, in-circuit programmable**
- **JTAG, IEEE 1149.1 JTAG testing capability**
- **128 macrocells**
- **15 ns t_{PD}**
- **50 MHz f_{MAX} external**
- **70 inputs with pull-up resistors**
- **64 outputs**
- **192 flip-flops**
  - — 128 macrocell flip-flops
  - — 64 input flip-flops
- **Up to 20 product terms per function, with XOR**
- **Flexible clocking**
  - — Four global clock pins with selectable edges
  - — Asynchronous mode available for each macrocell
- **8 "PAL33V16" blocks**
- **Input and output switch matrices for high routability**
- **Fixed, predictable, deterministic delays**
- **JEDEC-file compatible with MACH435**
- **Zero-hold-time input register option**

GENERAL DESCRIPTION

The MACH445 is a member of AMD's high-performance EE CMOS MACH 4 family. This device has approximately twelve times the macrocell capability of the popular PAL22V10, with significant density and functional features that the PAL22V10 does not provide. It is architecturally identical to the MACH435, with the addition of JTAG and 5-V programmability capabilities.

The MACH445 consists of eight PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The MACH445 has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

Up to 20 product terms per function can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

The MACH445 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer or by the software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

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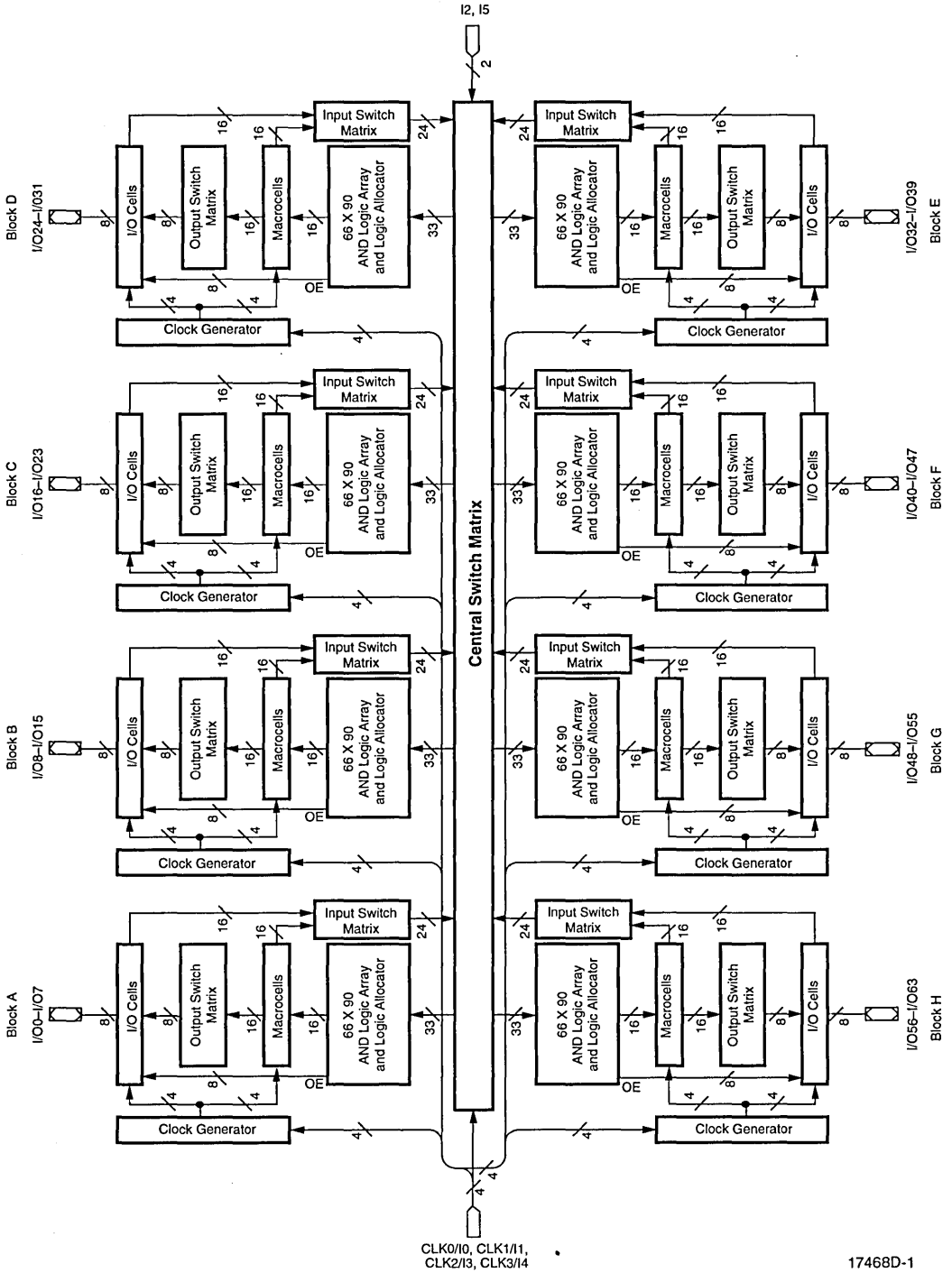
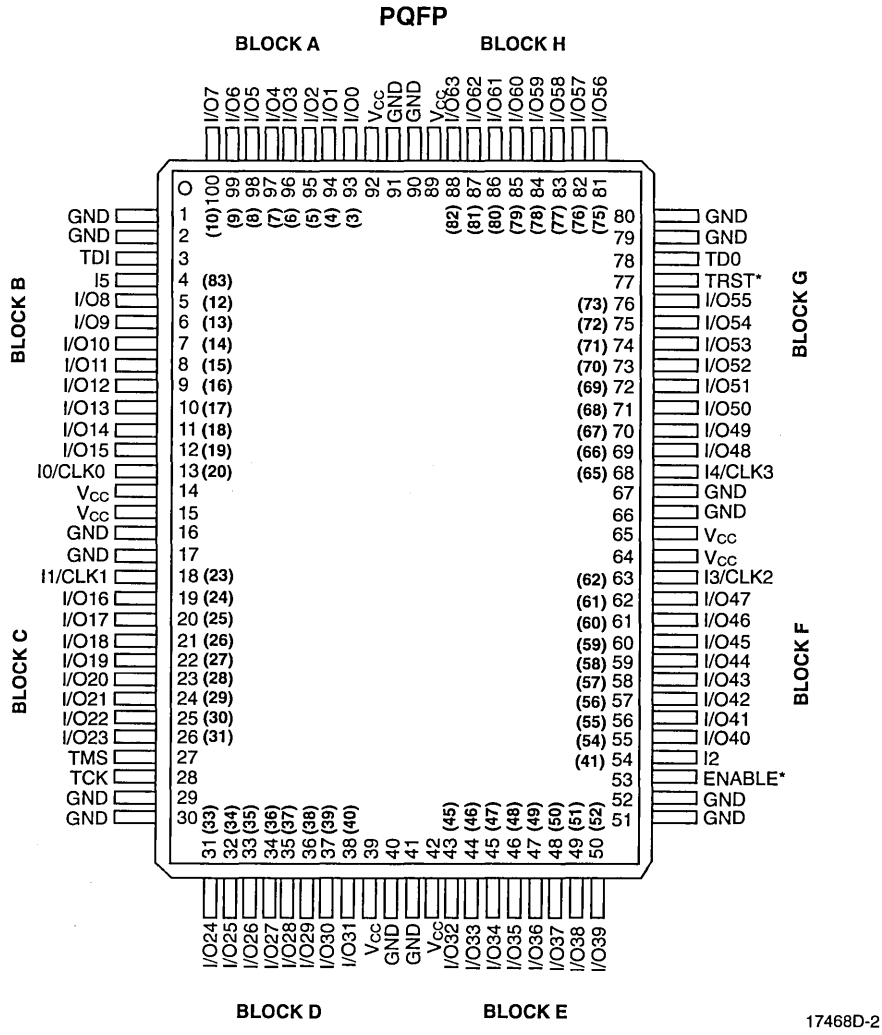
BLOCK DIAGRAM



CONNECTION DIAGRAM MACH445 (MACH435)
Top View



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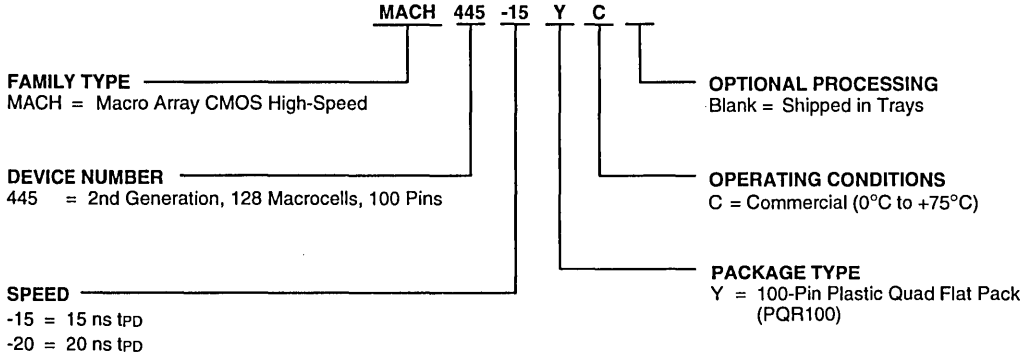
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH445-15	YC
MACH445-20	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH445 consists of eight PAL blocks connected by a central switch matrix. There are 64 I/O pins and 6 dedicated input pins feeding the central switch matrix. These signals are distributed to the eight PAL blocks for efficient design implementation. There are 4 global clock pins that can also be used as dedicated inputs.

All inputs and I/O pins have built-in pull-up resistors. While it is always good design practice to tie unused pins high, the pull-up resistors provide design security and stability in the event that unused pins are left disconnected.

The PAL Blocks

Each PAL block in the MACH445 (Figure 16) contains a clock generator, a 90-product-term logic array, a logic allocator, 16 macrocells, an output switch matrix, 8 I/O cells, and an input switch matrix. The central switch matrix feeds each PAL block with 33 inputs. This makes the PAL block look effectively like an independent "PAL33V16" with 8 to 16 buried macrocells.

In addition to the logic product terms, individual output enable product terms and two PAL block initialization product term are provided. Each I/O pin can be individually enabled. All flip-flops that are in the synchronous mode within a PAL block are initialized together by either of the PAL block initialization product terms.

The Central Switch Matrix and Input Switch Matrix

The MACH445 central switch matrix is fed by the input switch matrices in each PAL block. Each PAL block provides 16 internal feedback signals, 8 registered input signals, and 8 I/O pin signals to the input switch matrix. Of these 32 signals, 24 decoded signals are provided to the central switch matrix by the input switch matrix. The central switch matrix distributes these signals back to the PAL blocks in a very efficient manner that provides for high performance. The design software automatically configures the input and central switch matrices when fitting a design into the device.

The Clock Generator

Each PAL block has a clock generator that can generate four clock signals for use throughout the PAL block. These four signals are available to all macrocells and I/O cells in the PAL block, whether in synchronous or asynchronous mode. The clock generator chooses the four signals from the eight possible signals given by the true and complement versions of the four global clock pin signals.

The Product-Term Array

The MACH445 product-term array consists of 80 product terms for logic use, eight product terms for output enable use, and two product terms for global PAL block initialization. Each macrocell has a nominal allocation of 5 product terms for logic, although the logic allocator allows for logic redistribution. Each I/O pin has its own individual output enable term. The initialization product terms provide asynchronous reset or preset to synchronous-mode macrocells in the PAL block.

The Logic Allocator

The logic allocator in the MACH445 takes the 80 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 20 product terms if in synchronous mode, or 18 product terms if in asynchronous mode. When product terms are routed away from a macrocell, it is possible to route all 5 product terms away, which precludes the use of the macrocell for logic generation; or it is possible to route only 4 product terms away, leaving one for simple function generation. The design software automatically configures the logic allocator when fitting the design into the device.

The logic allocator also provides an exclusive-OR gate. This gate allows generation of combinatorial exclusive-OR logic, such as comparison or addition. It allows registered exclusive-OR functions, such as CRC generation, to be implemented more efficiently. It also makes in possible to emulate all flip-flop types with a D-type flip-flop. Register type emulation is automatically handled by the design software.

Table 9 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 16 for cluster and macrocell numbers.

Table 9. Logic Allocation

Macrocell	Available Clusters
M0	C0, C1, C2
M1	C0, C1, C2, C3
M2	C1, C2, C3, C4
M3	C2, C3, C4, C5
M4	C3, C4, C5, C6
M5	C4, C5, C6, C7
M6	C5, C6, C7, C8
M7	C6, C7, C8, C9
M8	C7, C8, C9, C10
M9	C8, C9, C10, C11
M10	C9, C10, C11, C12
M11	C10, C11, C12, C13
M12	C11, C12, C13, C14
M13	C12, C13, C14, C15
M14	C13, C14, C15
M15	C14, C15

The Macrocell and Output Switch Matrix

The MACH445 has 16 macrocells, half of which can drive I/O pins; this selection is made by the output switch matrix. Each macrocell can drive one of four I/O cells. The allowed combinations are shown in Table 10. Please refer to Figure 16 for macrocell and I/O pin numbers.

Table 10. Output Switch Matrix Combinations

Macrocell	Routable to I/O Pins
M0, M1	I/O5, I/O6, I/O7, I/O0
M2, M3	I/O6, I/O7, I/O0, I/O1
M4, M5	I/O7, I/O0, I/O1, I/O2
M6, M7	I/O0, I/O1, I/O2, I/O3
M8, M9	I/O1, I/O2, I/O3, I/O4
M10, M11	I/O2, I/O3, I/O4, I/O5
M12, M13	I/O3, I/O4, I/O5, I/O6
M14, M15	I/O4, I/O5, I/O6, I/O7
I/O Pin	**Available Macrocells**
I/O0	M0, M1, M2, M3, M4, M5, M6, M7
I/O1	M2, M3, M4, M5, M6, M7, M8, M9
I/O2	M4, M5, M6, M7, M8, M9, M10, M11
I/O3	M6, M7, M8, M9, M10, M11, M12, M13
I/O4	M8, M9, M10, M11, M12, M13, M14, M15
I/O5	M10, M11, M12, M13, M14, M15, M0, M1
I/O6	M12, M13, M14, M15, M0, M1, M2, M3
I/O7	M14, M15, M0, M1, M2, M3, M4, M5

The macrocells can be configured as registered, latched, or combinatorial. In combination with the logic allocator, the registered configuration can be any of the standard flip-flop types. The macrocell provides internal feedback whether configured with or without the flip-flop, and whether or not the macrocell drives an I/O cell.

The flip-flop clock depends on the mode selected for the macrocell. In synchronous mode, any of the PAL block clocks generated by the Clock Generator can be used. In asynchronous mode, the additional choice of either edge of an individual product-term clock is available.

Initialization can be handled as part of a bank of macrocells via the PAL block initialization terms if in synchronous mode, or individually if in asynchronous mode. In synchronous mode, one of the PAL block product terms is available each for preset and reset. The swap function determines which product term drives which function. This allows initialization polarity compatibility with the MACH 1 and 2 series. In asynchronous mode, one product term can be used either to drive reset or preset.

The I/O Cell

The I/O cell in the MACH445 consists of a three-state buffer and an input flip-flop. The I/O cell is driven by one of the macrocells, as selected by the output switch matrix. Each I/O cell can take its input from one of eight macrocells. The three-state buffer is controlled by an individual product term. The input flip-flop can be configured as a register or latch. Both the direct I/O signal and the registered/latched signal are available to the input switch matrix, and can be used simultaneously if desired.

JTAG Testing

JTAG is the commonly used acronym for the IEEE Standard 1149.1–1990. The JTAG standard defines input and output pins, logic control functions, and instructions. AMD has incorporated this standard into the MACH445 device.

The JTAG standard was developed as a means of providing both board-level and device-level testing. Details on this feature can be found in the application note titled, *Introduction to JTAG and Five-Volt Programming with MACH 3 and 4 Devices* at the end of this databook.

Five-Volt Programming

Another benefit from the JTAG circuitry that AMD has derived is the ability to use the JTAG port for five-volt programming. This allows the device to be soldered to the board before programming. Once the device is attached, the delicate Plastic Quad Flat Pack, or PQFP, leads are protected from programming and testing operations that could potentially damage them. Programming and verification of the device is done serially which is ideal for on-board programming since it only requires the use of the Test Access Port, along with the additional ENABLE* pin.

Details on this feature can also be found in the *Introduction to JTAG and Five-Volt Programming with MACH 3 and 4 Devices* application note at the end of this databook.

Zero-Hold-Time Input Register

The MACH445 device has a zero-hold time (ZHT) fuse. This fuse controls the time delay associated with loading data into all I/O cell registers and latches in the MACH445 device.

When programmed, the ZHT fuse increases the data path setup delays to input storage elements, matching equivalent delays in the clock path. When the fuse is erased, the setup time to the input storage element is minimized and the device timing is compatible with the MACH435 device.

This feature facilitates doing worst-case designs for which data is loaded from sources which have low (or zero) minimum output propagation delays from clock edges. See the *MACHXL™ Software User's Guide* for more details.

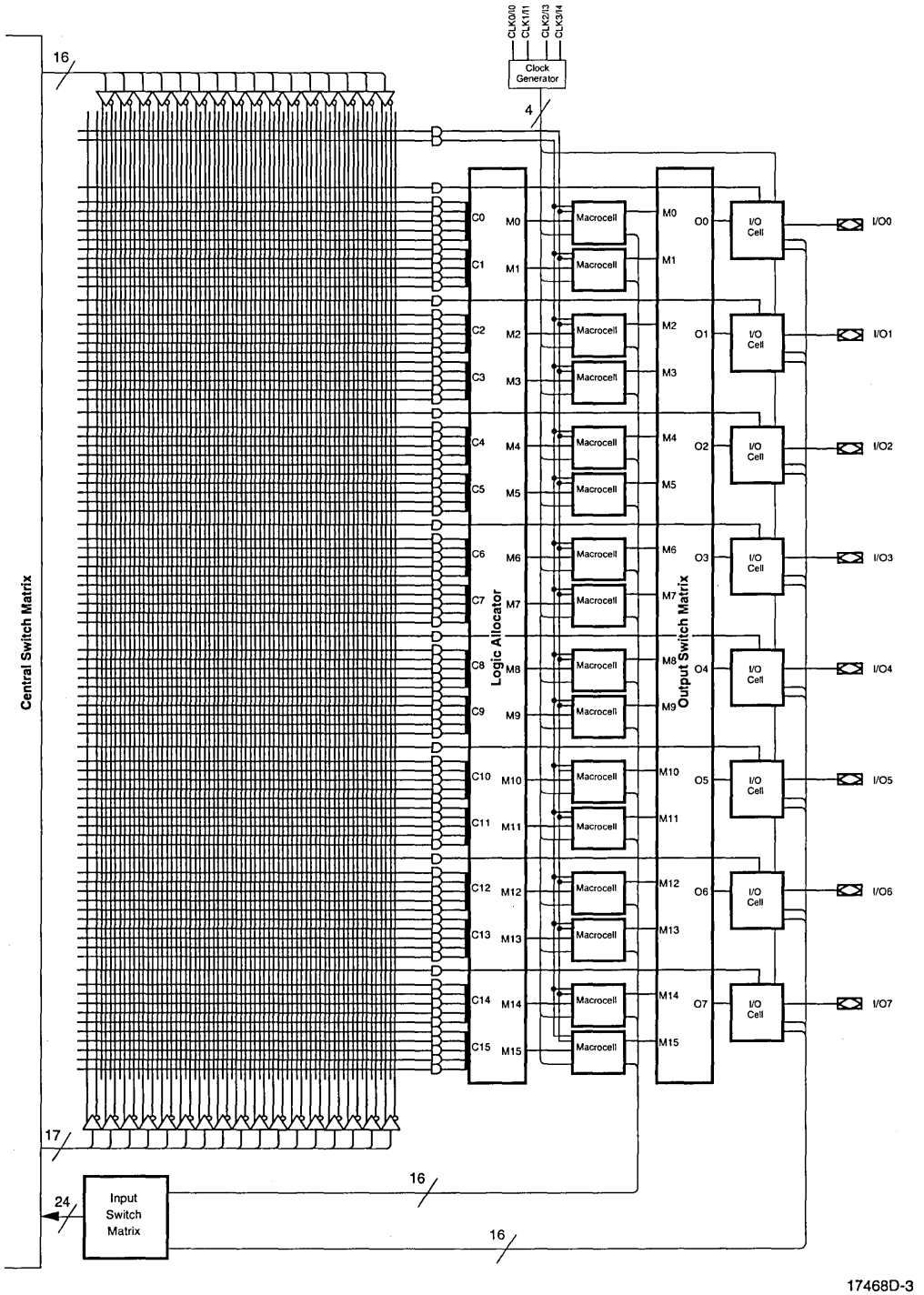


Figure 16. MACH445 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature
with Power Applied ..... –55°C to +125°C

Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} +0.5 V

DC Output or
I/O Pin Voltage ..... –0.5 V to V_{CC} +0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current
(T_A = 0°C to +75°C) ..... 200 mA

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating
in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with
Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)		–30	–160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f =25 MHz T_A = 25°C (Note 5)		255		mA

CAPACITANCE (Note 6)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset. An actual I_{CC} value can be calculated by using the "Typical Dynamic I_{CC} Characteristics" Chart towards the end of this data sheet.*
6. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				-15		-20		Unit
					Min	Max	Min	Max	
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 2)				3	15	3	20	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	8		10		ns
				T-type	9		11		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				8		10		ns
t_{COA}	Product Term Clock to Output (Note 2)				4	18	4	22	ns
t_{WLA}	Product Term, Clock Width			LOW	9		12		ns
t_{WHA}				HIGH	9		12		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 3)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	38.5		31.2		MHz
				T-type	37		30.3		MHz
		Internal Feedback (f_{CNTA})		D-type	47.6		37		MHz
				T-type	45.4		35.7		MHz
		No Feedback (Note 4)	$1/(t_{WLA} + t_{WHA})$		55.6		41.7		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	10		13		ns
				T-type	11		14		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		ns
t_{COS}	Global Clock to Output (Note 2)				2	10	2	12	ns
t_{WLS}	Global Clock Width			LOW	6		8		ns
t_{WHS}				HIGH	6		8		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 3)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	50		40		MHz
				T-type	47.6		38.5		MHz
		Internal Feedback (f_{CNTS})		D-type	66.6		50		MHz
				T-type	62.5		47.6		MHz
		No Feedback (Note 4)	$1/(t_{WLS} + t_{WHS})$		83.3		62.5		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				8		10		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				8		10		ns
t_{GOA}	Product Term Gate to Output (Note 2)					19		22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				9		12		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate				10		13		ns
t_{HLS}	Latch Data Hold Time Using Global Gate				0		0		ns
t_{GOS}	Gate to Output (Note 2)					11		12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				6		8		ns
t_{ICO}	Input Register Clock to Combinatorial Output					20		25	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

Parameter Symbol	Parameter Description		-15		-20		Unit
			Min	Max	Min	Max	
t_{ICS}	Input Register Clock to Output Register Setup	D-type	15		20		ns
		T-type	16		21		ns
t_{WICL}	Input Register Clock Width	LOW	6		8		ns
t_{WICH}		HIGH	6		8		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	83.3		62.5		MHz
t_{IGO}	Input Latch Gate to Combinatorial Output			20		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			22		27	ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		14		19		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		16		21		ns
t_{WIGL}	Input Latch Gate Width LOW		6		8		ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 3)		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)		15		20		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			20		25	ns
t_{APW}	Asynchronous Preset Width (Note 3)		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 3)		15		20		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 2)		2	15	2	20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 2)		2	15	2	20	ns
Input Register with Standard-Hold-Time Option							
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch			17		22	ns
t_{SIR}	Input Register Setup Time		2		2		ns
t_{HIR}	Input Register Hold Time		4		5		ns
t_{SIL}	Input Latch Setup Time		2		2		ns
t_{HIL}	Input Latch Hold Time		4		5		ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate		10		12		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate		12		16		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			19		24	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

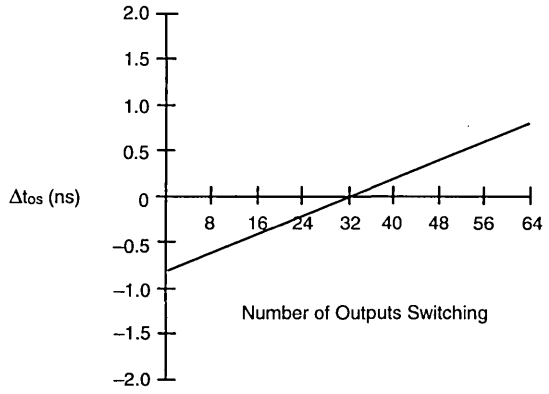
Parameter Symbol	Parameter Description	-15		-20		Unit
		Min	Max	Min	Max	
Input Register with Zero-Hold-Time Option						
t_{PDL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input Latch		23		30	ns
t_{SIR}^{I}	Input Register Setup Time	6		8		ns
t_{HIR}^{I}	Input Register Hold Time	0		0		ns
t_{SIL}^{I}	Input Latch Setup Time	6		8		ns
t_{HIL}^{I}	Input Latch Hold Time	0		0		ns
t_{SLLA}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	16		20		ns
t_{SLLS}^{I}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	18		24		ns
t_{PDLL}^{I}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		25		32	ns

Notes:

1. *See Switching Test Circuit at the end of this Data Book for test conditions.*
2. *Parameters measured with 32 outputs switching.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

TYPICAL SWITCHING CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C. These parameters are not tested.



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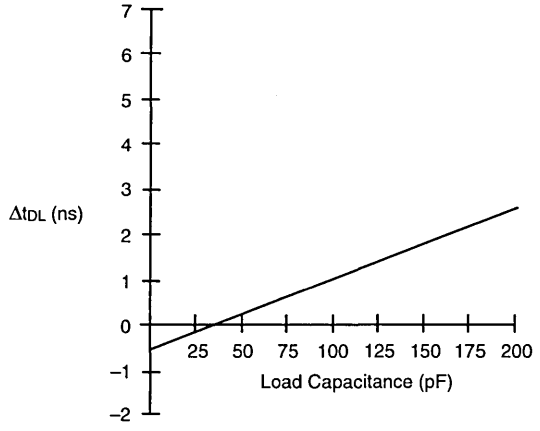
Derating for Number of Outputs Switching

Notes:

Applies to t_{PD}, t_{CO}. Calculate as:

$t_{derated} = t_{32O/P} + \Delta t_{OS}$

Datasheet numbers ($t_{32O/P}$) are specified at 32 outputs switching



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Capacitive Load Derating

Notes:

Applies to all AC specifications and rise and fall times. Calculate as:

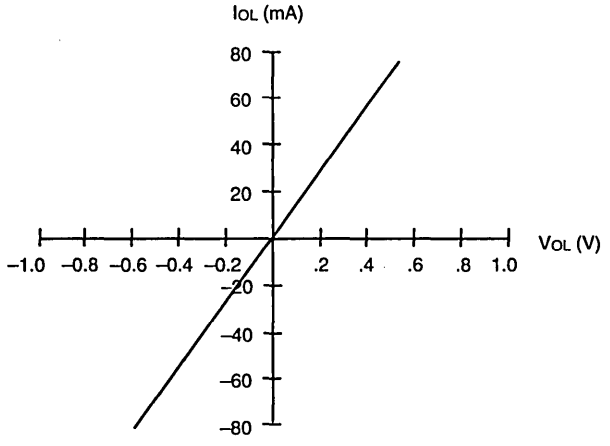
$t_{derated} = t_{35pF} + \Delta t_{DL}$

Datasheet numbers (t_{35pF}) are specified with 35 pF.

For typical rise and fall rates, use 1V/ns at 35 pF.

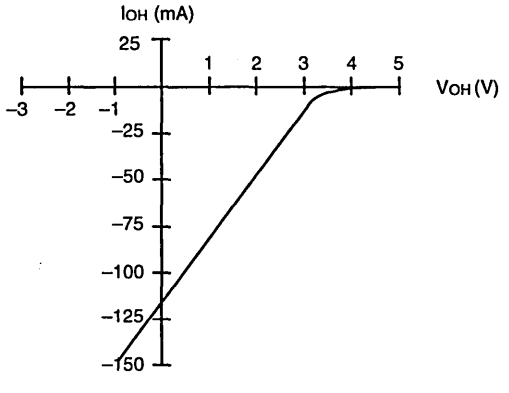
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



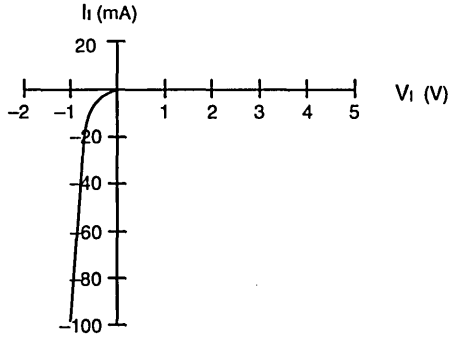
Output, LOW

17468D-6



Output, HIGH

17468D-7

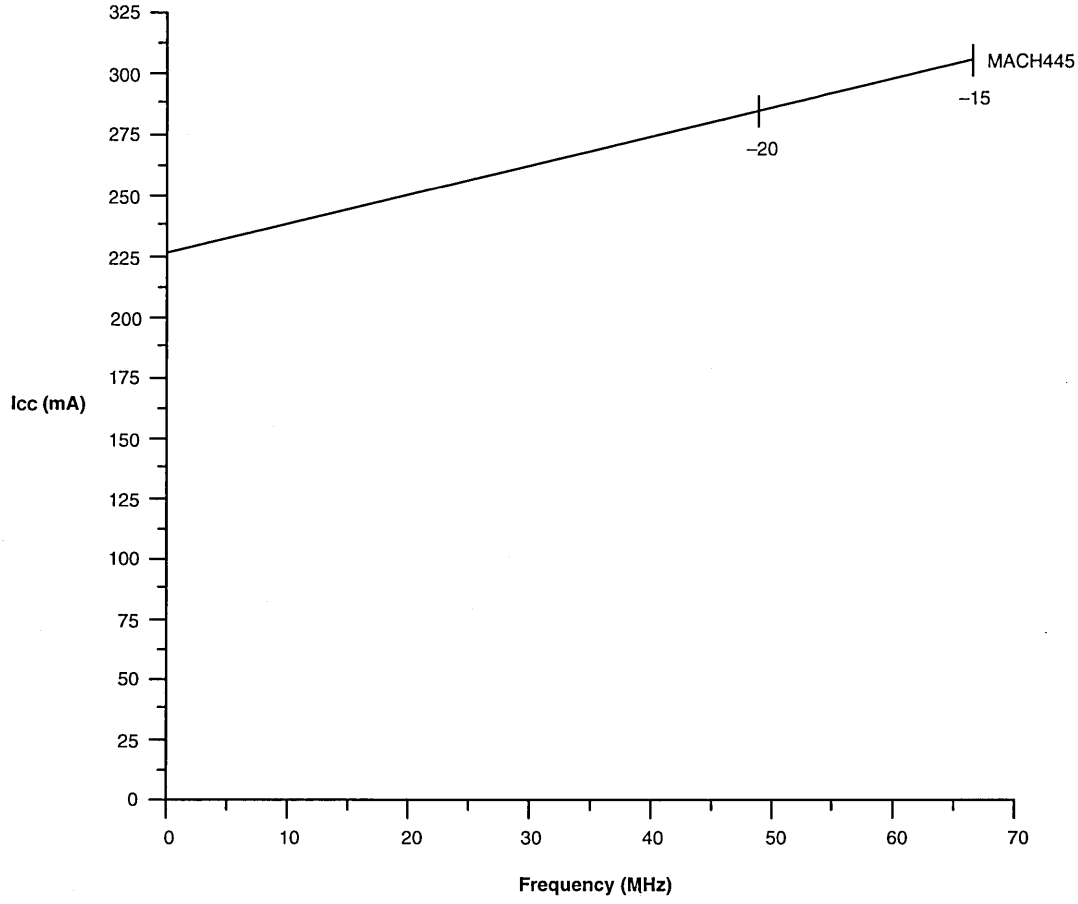


Input

17468D-8

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C



The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Actual I_{CC} values vary with the selected pattern. An actual I_{CC} value can be calculated using the "Typical Dynamic I_{CC} Characteristics" chart towards the end of this datasheet.

Maximum frequency shown uses internal feedback and a D-type register.

TYPICAL DYNAMIC I_{CC} CHARACTERISTICS

These parameters are not tested. Please refer to the General Information section for a discussion on the usage of these parameters.

Parameter Symbol	Parameter Description	Typ	Unit
I_{CCO}	Base static I_{CC}	225	mA
i_I	Incremental input current	32	µA/MHz
i_B	Incremental current per PAL block	30	µA/MHz
i_O	Incremental output current	110	µA/MHz
i_V	Voltage dependence	38	%/V
i_T	Temperature dependence	–0.13	%/°C

TYPICAL DATA DESIGN GUIDELINES

The following parameters are provided in response to questions from designers. They are intended only as design guidelines, and should be used with care. They are not guaranteed or tested.

Parameter Description	Typ	Unit
Edge Rates (Note 1)		
Rise rate	1	V/ns
Fall rate	1	V/ns
Skew (Note 2)		
Global clock-to-output skew, same clock polarity and same output polarity	1	ns
Global clock-to-output skew, same clock polarity only	2	ns
Global clock-to-output skew, same output polarity only	2	ns
Global clock-to-output skew, different clock polarity and different output polarity	3	ns
Internal Delay Savings (Note 3)		
Propagation delay savings	2	ns
Clock-to-output delay savings	3	ns
Ground Bounce (Note 4)		
Ground bounce noise level on low output	0.5	V

Notes:

1. *Rise and fall rates are for unloaded outputs.*
2. *Skew values assume equal output loading.*
3. *Internal delay savings gives the typical amount of delay saved by not going through an output buffer.*
4. *The ground bounce noise level should be added to the static V_{OL} under normal load conditions as applied to a silent low output when all other I/O pins are switching from high to low.*

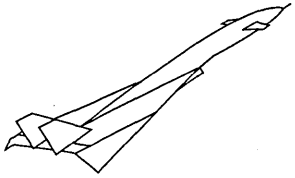
TYPICAL THERMAL CHARACTERISTICS

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PQFP	Unit
θ_{jc}	Thermal impedance, junction to case		5	°C/W
θ_{ja}	Thermal impedance, junction to ambient		38	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	32	°C/W
		400 lfpm air	28	°C/W
		600 lfpm air	26	°C/W
		800 lfpm air	24	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.



MACH446-10/12/15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **100-pin version of the MACH435 in PQFP**
- **5 V, in-circuit programmable**
- **JTAG, IEEE 1149.1 JTAG testing capability**
- **128 macrocells**
- **15 ns t_{PD}**
- **50 MHz f_{MAX} external**
- **70 Bus-Friendly™ inputs**
- **64 outputs**
- **192 flip-flops**
  - — 128 macrocell flip-flops
  - — 64 input flip-flops
- **Up to 20 product terms per function, with XOR**
- **Flexible clocking**
  - — Four global clock pins with selectable edges
  - — Asynchronous mode available for each macrocell
- **8 "PAL33V16" blocks**
- **Input and output switch matrices for high routability**
- **Fixed, predictable, deterministic delays**
- **JEDEC-file compatible with MACH435**
- **Zero-hold-time input register option**
- **Programmable power-down mode**

GENERAL DESCRIPTION

The MACH446 is a member of AMD's high-performance EE CMOS MACH 4 family. This device has approximately twelve times the macrocell capability of the popular PAL22V10, with significant density and functional features that the PAL22V10 does not provide. It is architecturally identical to the MACH445, with the addition of bus-friendly inputs and programmable power-down mode.

The MACH446 consists of eight PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The MACH446 has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

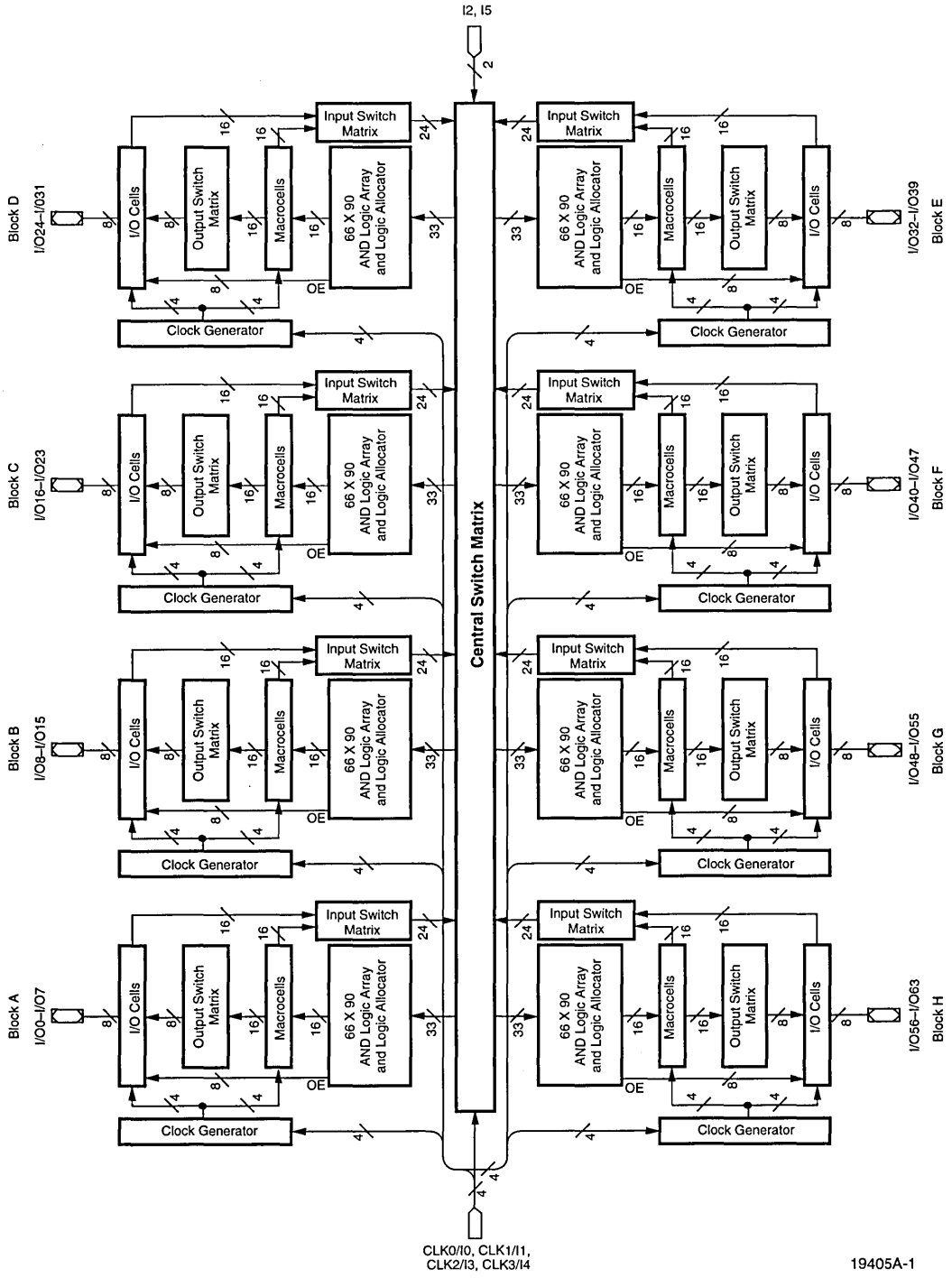
Up to 20 product terms per function can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

The MACH446 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer or by the software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

Publication# 19405 Rev. A Amendment/0
Issue Date: August 1994

BLOCK DIAGRAM



PRELIMINARY

COM'L: -15/20

MACH465-15/20

High-Density EE CMOS Programmable Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- 208 pins in PQFP
- JTAG, 5-V, in-circuit programmable
- IEEE 1149.1 JTAG testing capability
- 256 macrocells
- 15 ns t_{PD}
- 50 MHz f_{MAX} external
- 146 inputs with pull-up resistors
- 128 Outputs
- 384 flip-flops
  - — 256 Macrocell flip-flops
  - — 128 Input flip-flops
- Up to 20 product terms per function, with XOR
- Flexible clocking
  - — Four global clock pins with selectable edges
  - — Asynchronous mode available for each macrocell
- 16 "PAL34V16" blocks
- Input and output switch matrices for high routability
- Fixed, predictable, deterministic delays
- Zero-hold-time input register option

GENERAL DESCRIPTION

The MACH465 is a member of AMD's high-performance EE CMOS MACH 4 family. This device has approximately 25 times the macrocell capability of the popular PAL22V10, with significant density and functional features that the PAL22V10 does not provide.

The MACH465 consists of 16 PAL blocks interconnected by a programmable central switch matrix. The central switch matrix connects the PAL blocks to each other and to all input pins, providing a high degree of connectivity between the fully-connected PAL blocks. This allows designs to be placed and routed efficiently. Routability is further enhanced by an input switch matrix and an output switch matrix. The input switch matrix provides input signals with alternative paths into the central switch matrix; the output switch matrix provides flexibility in assigning macrocells to I/O pins.

The MACH465 has macrocells that can be configured as synchronous or asynchronous. This allows designers to implement both synchronous and asynchronous logic together on the same device. The two types of design can be mixed in any proportion, since the selection on each macrocell affects only that macrocell.

Up to 20 product terms per function can be assigned. It is possible to allocate some product terms away from a macrocell without losing the use of that macrocell for logic generation.

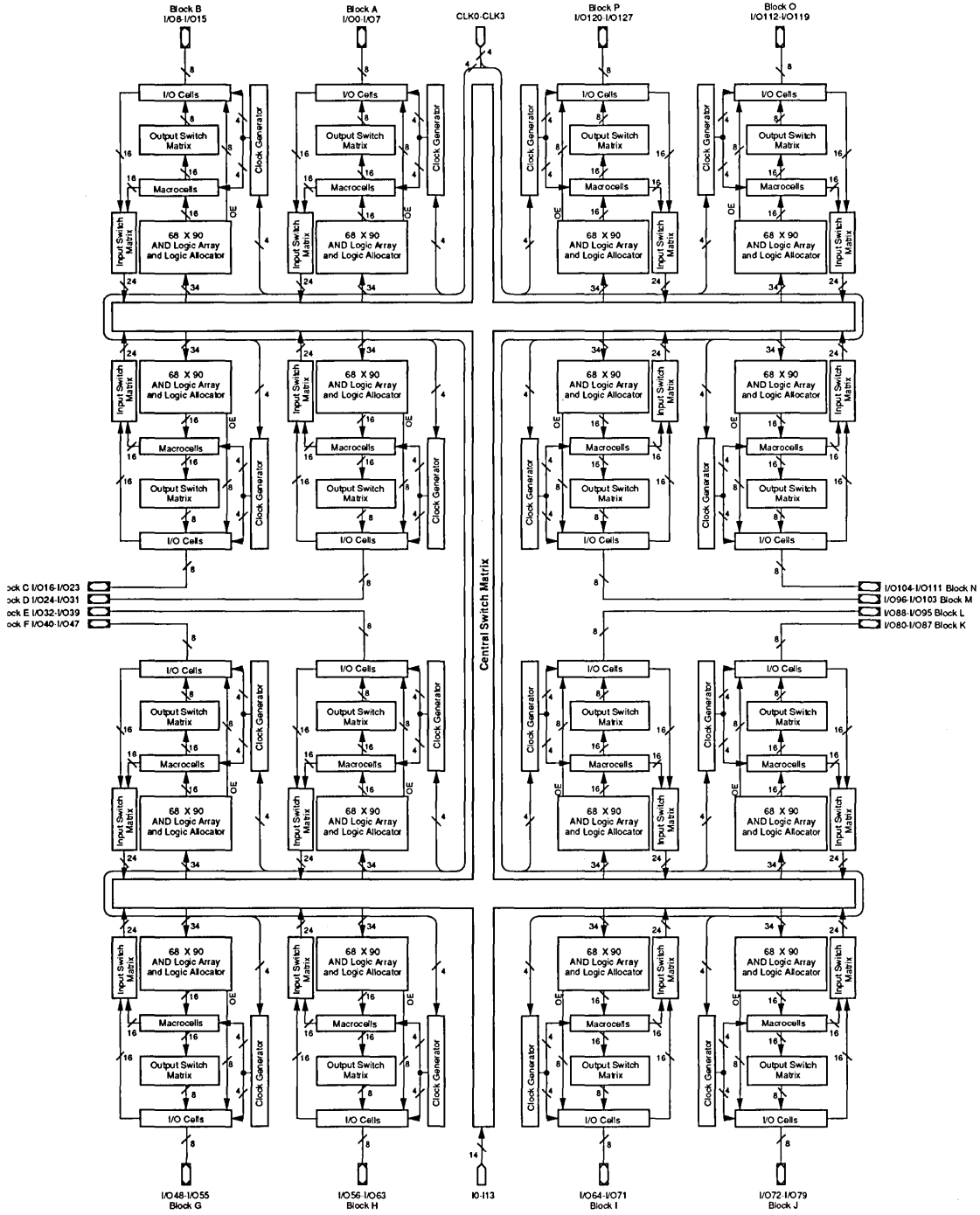
The MACH465 macrocell provides either registered or combinatorial outputs with programmable polarity. If a registered configuration is chosen, the register can be configured as D-type, T-type, J-K, or S-R to help reduce the number of product terms used. The flip-flop can also be configured as a latch. The register type decision can be made by the designer or by the software.

All macrocells can be connected to an I/O cell through the output switch matrix. The output switch matrix makes it possible to make significant design changes while minimizing the risk of pinout changes.

Publication# 17470 Rev. C Amendment/0
Issue Date: August 1994

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

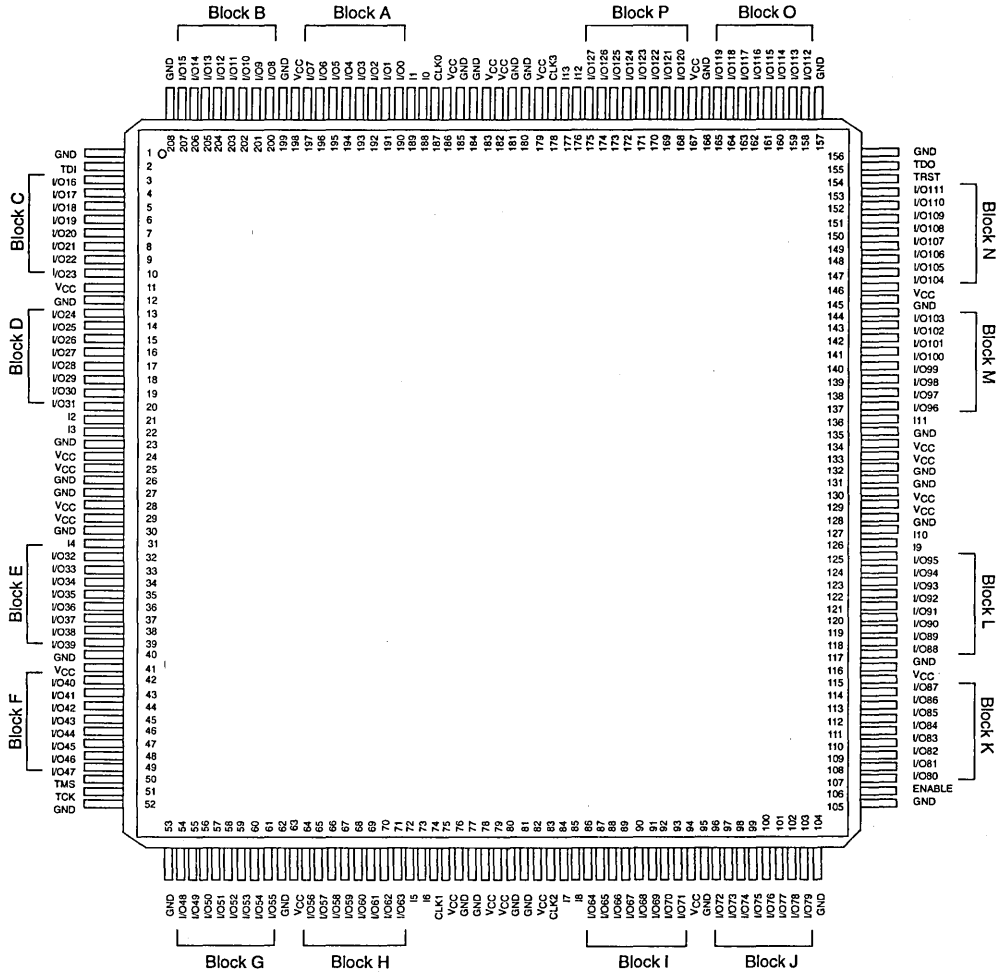
BLOCK DIAGRAM



17470C-1

CONNECTION DIAGRAM
Top View

PQFP



17470C-2

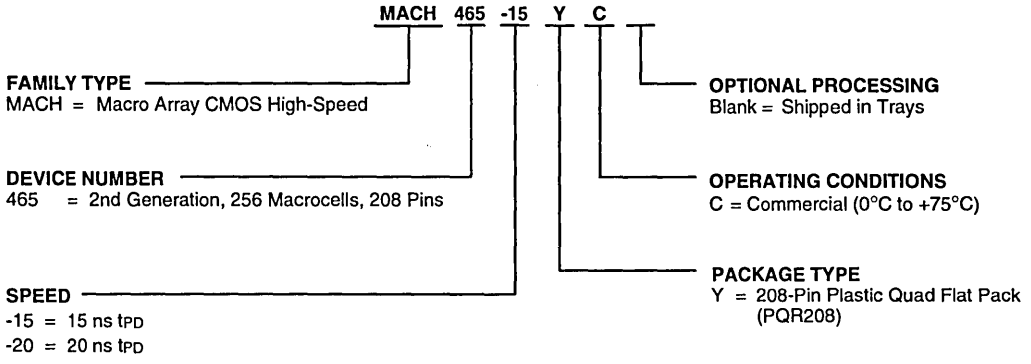
PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage

ORDERING INFORMATION

Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
MACH465-15	YC
MACH465-20	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The MACH465 consists of sixteen PAL blocks connected by a central switch matrix. There are 128 I/O pins and 14 dedicated input pins feeding the central switch matrix. These signals are distributed to the sixteen PAL blocks for efficient design implementation. There are also 4 global clock pins.

All inputs and I/O pins have built-in pull-up resistors. While it is always good design practice to tie unused pins high, the pull-up resistors provide design security and stability in the event that unused pins are left disconnected.

The PAL Blocks

Each PAL block in the MACH465 (Figure 17) contains a clock generator, a 90-product-term logic array, a logic allocator, 16 macrocells, an output switch matrix, 8 I/O cells, and an input switch matrix. The central switch matrix feeds each PAL block with 34 inputs. This makes the PAL block look effectively like an independent "PAL34V16".

In addition to the logic product terms, individual output enable product terms and two PAL block initialization product term are provided. Each I/O pin can be individually enabled. All flip-flops that are in the synchronous mode within a PAL block are initialized together by either of the PAL block initialization product terms.

The Central Switch Matrix and Input Switch Matrix

The MACH465 central switch matrix is fed by the input switch matrices in each PAL block. Each PAL block provides 16 internal feedback signals, 8 registered input signals, and 8 I/O pin signals to the input switch matrix. Of these 32 signals, 24 decoded signals are provided to the central switch matrix by the input switch matrix. The central switch matrix distributes these signals back to the PAL blocks in a very efficient manner that provides for high performance. The design software automatically configures the input and central switch matrices when fitting a design into the device.

The Clock Generator

Each PAL block has a clock generator that can generate four clock signals for use throughout the PAL block. These four signals are available to all macrocells and I/O cells in the PAL block, whether in synchronous or asynchronous mode. The clock generator chooses the four signals from the eight possible signals given by the true and complement versions of the four global clock pin signals.

The Product-Term Array

The MACH465 product-term array consists of 80 product terms for logic use, eight product terms for output enable use, and two product terms for global PAL block initialization. Each macrocell has a nominal allocation of 5 product terms for logic, although the logic allocator allows for logic redistribution. Each I/O pin has its own individual output enable term. The initialization product terms provide asynchronous reset or preset to synchronous-mode macrocells in the PAL block.

The Logic Allocator

The logic allocator in the MACH465 takes the 80 logic product terms and allocates them to the 16 macrocells as needed. Each macrocell can be driven by up to 20 product terms if in synchronous mode, or 18 product terms if in asynchronous mode. When product terms are routed away from a macrocell, it is possible to route all 5 product terms away, which precludes the use of the macrocell for logic generation; or it is possible to route only 4 product terms away, leaving one for simple function generation. The design software automatically configures the logic allocator when fitting the design into the device.

The logic allocator also provides an exclusive-OR gate. This gate allows generation of combinatorial exclusive-OR logic, such as comparison or addition. It allows registered exclusive-OR functions, such as CRC generation, to be implemented more efficiently. It also makes in possible to emulate all flip-flop types with a D-type flip-flop. Register type emulation is automatically handled by the design software.

Table 11 illustrates which product term clusters are available to each macrocell within a PAL block. Refer to Figure 17 for cluster and macrocell numbers.

Table 11. Logic Allocation

Macrocell	Available Clusters
M0	C0, C1, C2
M1	C0, C1, C2, C3
M2	C1, C2, C3, C4
M3	C2, C3, C4, C5
M4	C3, C4, C5, C6
M5	C4, C5, C6, C7
M6	C5, C6, C7, C8
M7	C6, C7, C8, C9
M8	C7, C8, C9, C10
M9	C8, C9, C10, C11
M10	C9, C10, C11, C12
M11	C10, C11, C12, C13
M12	C11, C12, C13, C14
M13	C12, C13, C14, C15
M14	C13, C14, C15
M15	C14, C15

The Macrocell and Output Switch Matrix

The MACH465 has 16 macrocells, half of which can drive I/O pins; this selection is made by the output switch matrix. Each macrocell can drive one of four I/O cells. The allowed combinations are shown in Table 12. Please refer to Figure 17 for macrocell and I/O pin numbers.

Table 12. Output Switch Matrix Combinations

Macrocell	Routable to I/O Pins
M0, M1	I/O5, I/O6, I/O7, I/O0
M2, M3	I/O6, I/O7, I/O0, I/O1
M4, M5	I/O7, I/O0, I/O1, I/O2
M6, M7	I/O0, I/O1, I/O2, I/O3
M8, M9	I/O1, I/O2, I/O3, I/O4
M10, M11	I/O2, I/O3, I/O4, I/O5
M12, M13	I/O3, I/O4, I/O5, I/O6
M14, M15	I/O4, I/O5, I/O6, I/O7
I/O Pin	**Available Macrocells**
I/O0	M0, M1, M2, M3, M4, M5, M6, M7
I/O1	M2, M3, M4, M5, M6, M7, M8, M9
I/O2	M4, M5, M6, M7, M8, M9, M10, M11
I/O3	M6, M7, M8, M9, M10, M11, M12, M13
I/O4	M8, M9, M10, M11, M12, M13, M14, M15
I/O5	M10, M11, M12, M13, M14, M15, M0, M1
I/O6	M12, M13, M14, M15, M0, M1, M2, M3
I/O7	M14, M15, M0, M1, M2, M3, M4, M5

The macrocells can be configured as registered, latched, or combinatorial. In combination with the logic allocator, the registered configuration can be any of the standard flip-flop types. The macrocell provides internal feedback whether configured with or without the flip-flop, and whether or not the macrocell drives an I/O cell.

The flip-flop clock depends on the mode selected for the macrocell. In synchronous mode, any of the PAL block clocks generated by the Clock Generator can be used. In asynchronous mode, the additional choice of either edge of an individual product-term clock is available.

Initialization can be handled as part of a bank of macrocells via the PAL block initialization terms if in synchronous mode, or individually if in asynchronous mode. In synchronous mode, one of the PAL block product terms is available each for preset and reset. The swap function determines which product term drives which function. This allows initialization polarity compatibility with the MACH 1 and 2 series. In asynchronous mode, one product term can be used either to drive reset or preset.

The I/O Cell

The I/O cell in the MACH465 consists of a three-state buffer and an input flip-flop. The I/O cell is driven by one of the macrocells, as selected by the output switch matrix. Each I/O cell can take its input from one of eight macrocells. The three-state buffer is controlled by an individual product term. The direct I/O signal is available to the input switch matrix, and can be used if desired.

JTAG Testing

JTAG is the commonly used acronym for the IEEE Standard 1149.1–1990. The JTAG standard defines and output pins, logic control functions, and instructions. AMD has incorporated this standard into the MACH465 device.

The JTAG standard was developed as a means of providing both board-level and device-level testing. Details on this feature can be found in the application note titled, *Introduction to JTAG and Five-Volt Programming with MACH 3 and 4 Devices*, at the end of this Data Book.

Five-Volt Programming

Another benefit from the JTAG circuitry that AMD has derived is the ability to use the JTAG port for five-volt programming. This allows the device to be soldered to the board before programming. Once the device is attached, the delicate Plastic Quad Flat Pack, or PQFP, leads are protected from programming and testing operations that could potentially damage them. Programming and verification of the device is done serially which is ideal for on-board programming since it only requires the use of the Test Access Port, along with the additional ENABLE* pin.

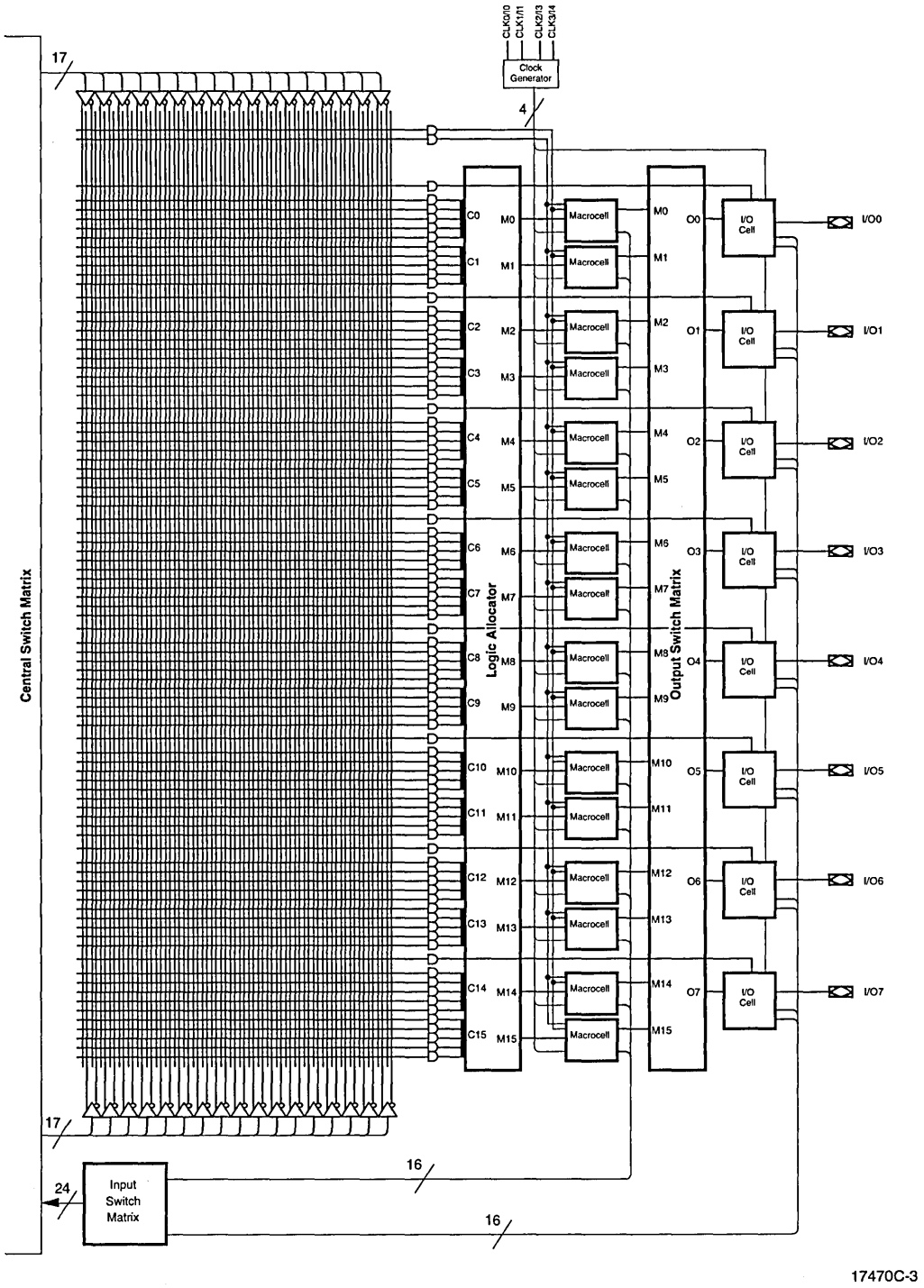
Details on this feature can also be found in the *Introduction to JTAG and Five-Volt Programming with MACH 3 and 4 Devices* application note, at the end of this Data Book.

Zero-Hold-Time Input Register

The MACH465 device has a zero-hold time (ZHT) fuse. This fuse controls the time delay associated with loading data into all I/O cell registers and latches in the MACH465 device.

When programmed, the ZHT fuse increases the data path setup delays to input storage elements, matching equivalent delays in the clock path. When the fuse is erased, the setup time to the input storage element is minimized.

This feature facilitates doing worst-case designs for which data is loaded from sources which have low (or zero) minimum output propagation delays from clock edges. See the *MACHXL™ Software User's Guide* for more details.



17470C-3

Figure 17. MACH465 PAL Block

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C
Ambient Temperature
with Power Applied ..... –55°C to +125°C
Supply Voltage with
Respect to Ground ..... –0.5 V to +7.0 V
DC Input Voltage ..... –0.5 V to V_{CC} +0.5 V
DC Output or
I/O Pin Voltage ..... –0.5 V to V_{CC} +0.5 V
Static Discharge Voltage ..... 2001 V
Latchup Current
(T_A = 0°C to +75°C) ..... 200 mA

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating
in Free Air ..... 0°C to +75°C
Supply Voltage (V_{CC}) with
Respect to Ground ..... +4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	PRELIMINARY Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			–100	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = 5.0 V, f =25 MHz T_A = 25°C (Note 5)				mA

CAPACITANCE (Note 6)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C,	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V	f = 1 MHz	8	pF

Notes:

1. *Total I_{OL} for one PAL block should not exceed 128 mA.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*
5. *Measured with a 16-bit up/down counter pattern. This pattern is programmed in each PAL block and capable of being loaded, enabled, and reset. An actual I_{CC} value can be calculated by using the "Typical Dynamic I_{CC} Characteristics" Chart towards the end of this data sheet.*
6. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description				PRELIMINARY -15 Min	-15 Max	-20 Min	-20 Max	Unit
t_{PD}	Input, I/O, or Feedback to Combinatorial Output (Note 2)				3	15	3	20	ns
t_{SA}	Setup Time from Input, I/O, or Feedback to Product Term Clock			D-type	8		10		ns
				T-type	9		11		ns
t_{HA}	Register Data Hold Time Using Product Term Clock				8		10		ns
t_{COA}	Product Term Clock to Output (Note 2)				4	18	4	22	ns
t_{WLA}	Product Term, Clock Width			LOW	9		12		ns
t_{WHA}				HIGH	9		12		ns
f_{MAXA}	Maximum Frequency Using Product Term Clock (Note 3)	External Feedback	$1/(t_{SA} + t_{COA})$	D-type	38.5		31.2		MHz
				T-type	37		30.3		MHz
		Internal Feedback (f_{CNTA})		D-type	47.6		37		MHz
				T-type	45.4		35.7		MHz
		No Feedback (Note 4)	$1/(t_{WLA} + t_{WHA})$		55.6		41.7		MHz
t_{SS}	Setup Time from Input, I/O, or Feedback to Global Clock			D-type	10		13		ns
				T-type	11		14		ns
t_{HS}	Register Data Hold Time Using Global Clock				0		0		ns
t_{COS}	Global Clock to Output (Note 2)				2	10	2	12	ns
t_{WLS}	Global Clock Width			LOW	6		8		ns
t_{WHS}				HIGH	6		8		ns
f_{MAXS}	Maximum Frequency Using Global Clock (Note 3)	External Feedback	$1/(t_{SS} + t_{COS})$	D-type	50		40		MHz
				T-type	47.6		38.5		MHz
		Internal Feedback (f_{CNTS})		D-type	66.6		50		MHz
				T-type	62.5		47.6		MHz
		No Feedback (Note 4)	$1/(t_{WLS} + t_{WHS})$		83.3		62.5		MHz
t_{SLA}	Setup Time from Input, I/O, or Feedback to Product Term Clock				8		10		ns
t_{HLA}	Latch Data Hold Time Using Product Term Clock				8		10		ns
t_{GOA}	Product Term Gate to Output (Note 2)					19		22	ns
t_{GWA}	Product Term Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				9		12		ns
t_{SLS}	Setup Time from Input, I/O, or Feedback to Global Gate				10		13		ns
t_{HLS}	Latch Data Hold Time Using Global Gate				0		0		ns
t_{GOS}	Gate to Output (Note 2)					11		12	ns
t_{GWS}	Global Gate Width LOW (for LOW transparent) or HIGH (for HIGH transparent)				6		8		ns
t_{ICO}	Input Register Clock to Combinatorial Output					20		25	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

Parameter Symbol	Parameter Description		PRELIMINARY -15 Min	-15 Max	-20 Min	-20 Max	Unit
t_{ICS}	Input Register Clock to Output Register Setup	D-type	15		20		ns
		T-type	16		21		ns
t_{WICL}	Input Register Clock Width	LOW	6		8		ns
t_{WICH}		HIGH	6		8		ns
f_{MAXIR}	Maximum Input Register Frequency	$1/(t_{WICL} + t_{WICH})$	83.3		62.5		MHz
t_{IGO}	Input Latch Gate to Combinatorial Output			20		25	ns
t_{IGOL}	Input Latch Gate to Output Through Transparent Output Latch			22		27	ns
t_{IGSA}	Input Latch Gate to Output Latch Setup Using Product Term Output Latch Gate		14		19		ns
t_{IGSS}	Input Latch Gate to Output Latch Setup Using Global Output Latch Gate		16		21		ns
t_{WIGL}	Input Latch Gate Width LOW		6		8		ns
t_{AR}	Asynchronous Reset to Registered or Latched Output			20		25	ns
t_{ARW}	Asynchronous Reset Width (Note 3)		15		20		ns
t_{ARR}	Asynchronous Reset Recovery Time (Note 3)		15		20		ns
t_{AP}	Asynchronous Preset to Registered or Latched Output			20		25	ns
t_{APW}	Asynchronous Preset Width (Note 3)		15		20		ns
t_{APR}	Asynchronous Preset Recovery Time (Note 3)		15		20		ns
t_{EA}	Input, I/O, or Feedback to Output Enable (Note 2)		2	15	2	20	ns
t_{ER}	Input, I/O, or Feedback to Output Disable (Note 2)		2	15	2	20	ns
Input Register with Standard-Hold-Time Option							
t_{PDL}	Input, I/O, or Feedback to Output Through Transparent Input Latch			17		22	ns
t_{SIR}	Input Register Setup Time		2		2		ns
t_{HIR}	Input Register Hold Time		4		5		ns
t_{SIL}	Input Latch Setup Time		2		2		ns
t_{HIL}	Input Latch Hold Time		4		5		ns
t_{SLLA}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate		10		12		ns
t_{SLLS}	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate		12		16		ns
t_{PDLL}	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches			19		24	ns

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1) (continued)

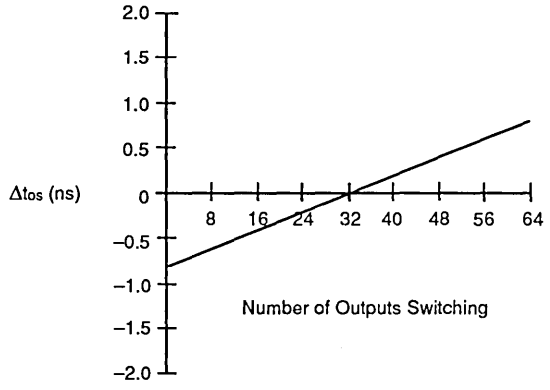
Parameter Symbol	Parameter Description	PRELIMINARY -15 Min	-15 Max	-20 Min	-20 Max	Unit
Input Register with Zero-Hold-Time Option						
t_{PDL}[4]	Input, I/O, or Feedback to Output Through Transparent Input Latch		23		30	ns
t_{SIR}[4]	Input Register Setup Time	6		8		ns
t_{HIR}[4]	Input Register Hold Time	0		0		ns
t_{SIL}[4]	Input Latch Setup Time	6		8		ns
t_{HIL}[4]	Input Latch Hold Time	0		0		ns
t_{SLLA}[4]	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Product Term Output Gate	16		20		ns
t_{SLLS}[4]	Setup Time from Input, I/O, or Feedback Through Transparent Input Latch to Output Gate	18		24		ns
t_{PDLL}[4]	Input, I/O, or Feedback to Output Through Transparent Input and Output Latches		25		32	ns

Notes:

1. *See Switching Test Circuit at the end of this Data Book for test conditions.*
2. *Parameters measured with 32 outputs switching.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

TYPICAL SWITCHING CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C. These parameters are not tested.



17470C-4

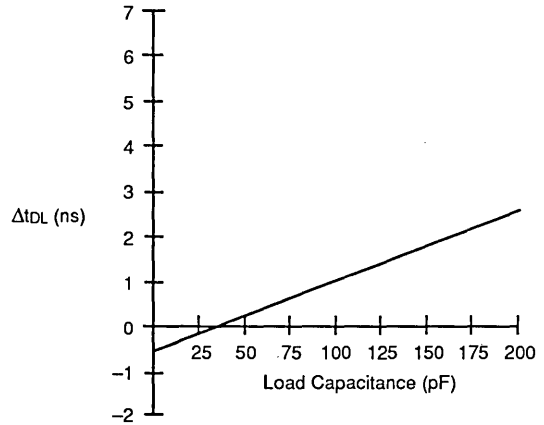
Derating for Number of Outputs Switching

Notes:

Applies to t_{PD}, t_{CO}. Calculate as:

$t_{derated} = t_{32\ O/P} + \Delta t_{OS}$

Datasheet numbers ($t_{32\ O/P}$) are specified at 32 outputs switching



17470C-5

Capacitive Load Derating

Notes:

Applies to all AC specifications and rise and fall times. Calculate as:

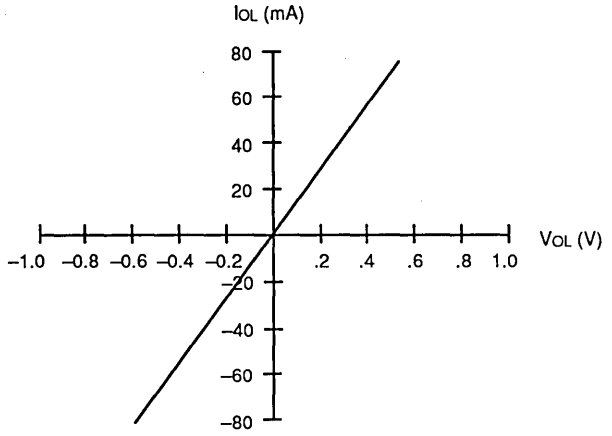
$t_{derated} = t_{35\ pF} + \Delta t_{DL}$

Datasheet numbers ($t_{35\ pF}$) are specified with 35 pF.

For typical rise and fall rates, use 1V/ns at 35 pF.

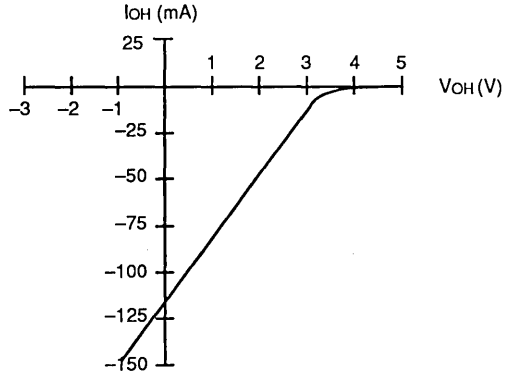
TYPICAL CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS

V_{CC} = 5.0 V, T_A = 25°C



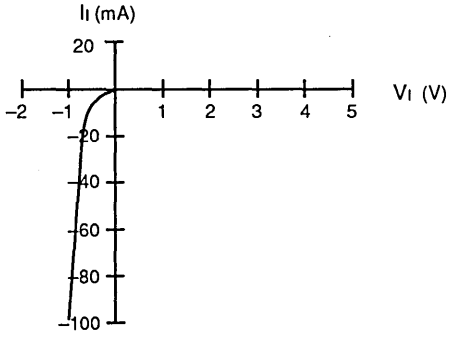
Output, LOW

17470C-6



17470C-7

Output, HIGH

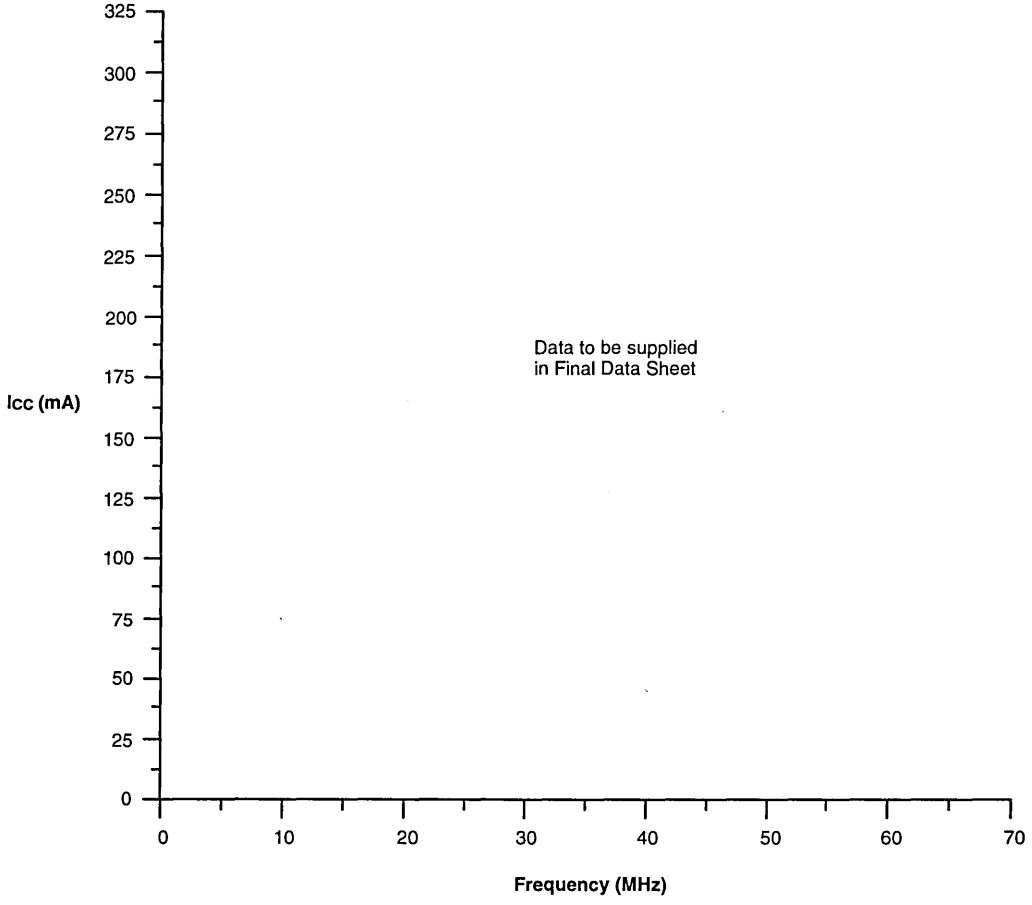


17470C-8

Input

TYPICAL I_{CC} CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C



The selected "typical" pattern is a 16-bit up/down counter. This pattern is programmed in each PAL block and is capable of being loaded, enabled, and reset.

Actual I_{CC} values vary with the selected pattern. An actual I_{CC} value can be calculated using the "Typical Dynamic I_{CC} Characteristics" chart towards the end of this datasheet.

Maximum frequency shown uses internal feedback and a D-type register.

TYPICAL DYNAMIC I_{CC} CHARACTERISTICS

These parameters are not tested. Please refer to the General Information section in the latest MACH 3 and 4 Data Book for a discussion on the usage of these parameters.

Parameter Symbol	Parameter Description	Typ	Units
i_{CC0}	Base static I_{CC}	TBD	mA
i_I	Incremental input current	32	µA/MHz
i_B	Incremental current per PAL block	30	µA/MHz
i_O	Incremental output current	110	µA/MHz
i_V	Voltage dependence	38	%/V
i_T	Temperature dependence	–0.13	%/°C

TYPICAL DATA DESIGN GUIDELINES

The following parameters are provided in response to questions from designers. They are intended only as design guidelines, and should be used with care. They are not guaranteed or tested.

Parameter Description	Typ	Units
Edge Rates (Note 1)		
Rise rate	1	V/ns
Fall rate	1	V/ns
Skew (Note 2)		
Global clock-to-output skew, same clock polarity and same output polarity	1	ns
Global clock-to-output skew, same clock polarity only	2	ns
Global clock-to-output skew, same output polarity only	2	ns
Global clock-to-output skew, different clock polarity and different output polarity	3	ns
Internal Delay Savings (Note 3)		
Propagation delay savings	2	ns
Clock-to-output delay savings	3	ns
Ground Bounce (Note 4)		
Ground bounce noise level on low output	0.5	V

Notes:

1. *Rise and fall rates are for unloaded outputs.*
2. *Skew values assume equal output loading.*
3. *Internal delay savings gives the typical amount of delay saved by not going through an output buffer.*
4. *The ground bounce noise level should be added to the static V_{OL} under normal load conditions as applied to a silent low output when all other I/O pins are switching from high to low.*

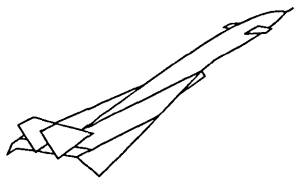
TYPICAL THERMAL GUIDELINES

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ PQFP	Unit
θ_{jc}	Thermal impedance, junction to case		TBD	°C/W
θ_{ja}	Thermal impedance, junction to ambient		TBD	°C/W
θ_{jma}	Thermal impedance, junction to ambient with air flow	200 lfpm air	TBD	°C/W
		400 lfpm air	TBD	°C/W
		600 lfpm air	TBD	°C/W
		800 lfpm air	TBD	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.



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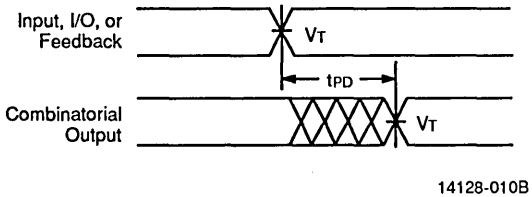
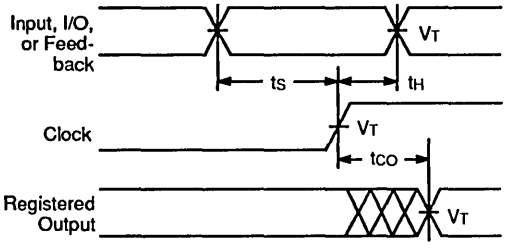
SWITCHING WAVEFORMS



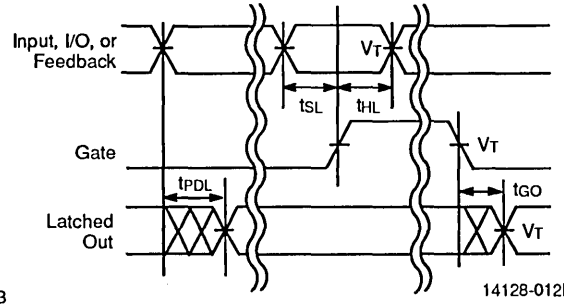
14128-010B

Combinatorial Output



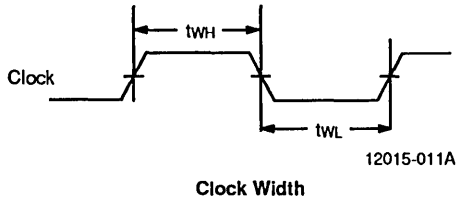
14128-011B

Registered Output



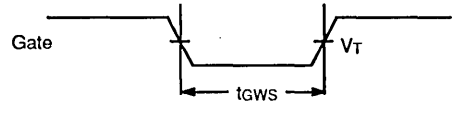
14128-012B

Latched Output



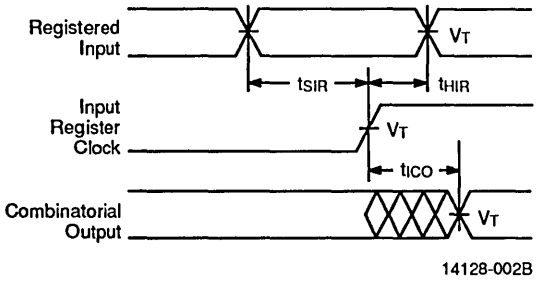
12015-011A

Clock Width



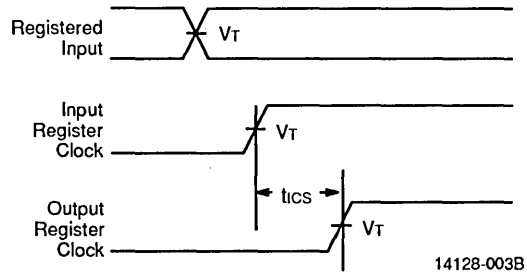
14128-014A

Gate Width



14128-002B

Registered Input



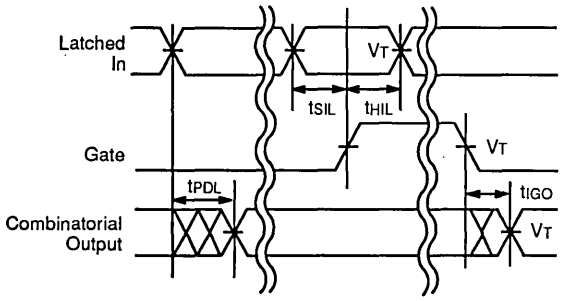
14128-003B

Input Register to Output Register Setup

Notes:

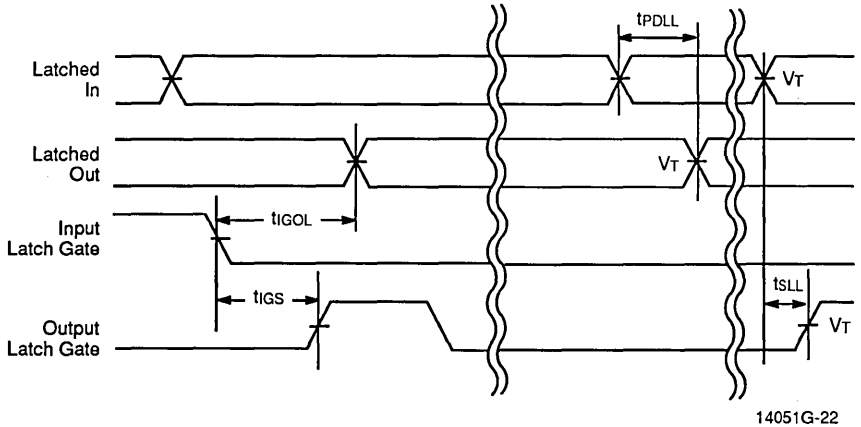
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



14051G-21

Latched Input



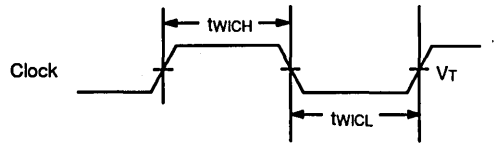
14051G-22

Latched Input and Output

Notes:

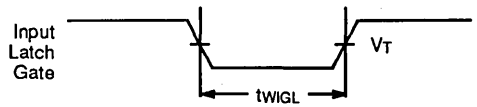
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

SWITCHING WAVEFORMS



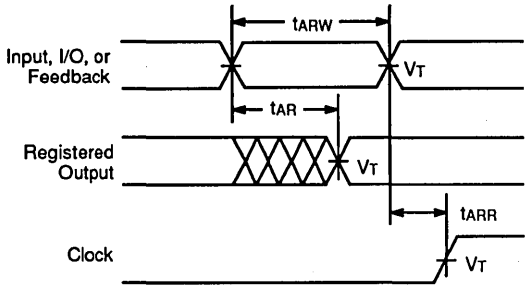
14128-003B

Input Register Clock Width



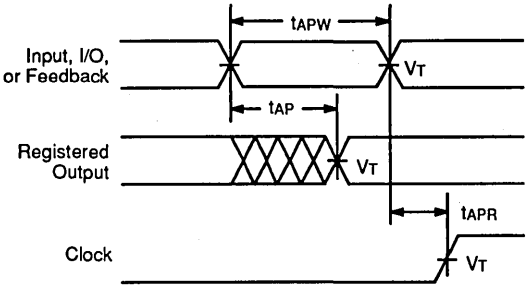
14128-018A

Input Latch Gate Width



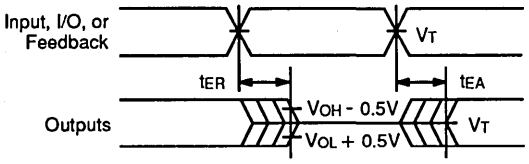
14128-005B

Asynchronous Reset



14128-006B

Asynchronous Preset



14128-019A

Output Disable/Enable

Notes:

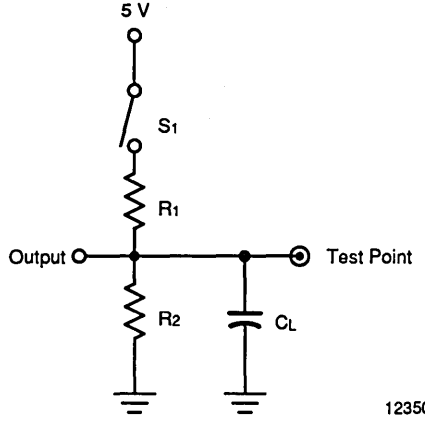
1. *V_T = 1.5 V.*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns–4 ns typical.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT



12350-019A

Specification	S_1	C_L	Commercial R_1	Commercial R_2	Measured Output Value
t_{PD}, t_{CO}	Closed	35 pF	300 Ω	390 Ω	1.5 V
t_{EA}	Z → H: Open Z → L: Closed				1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} − 0.5 V L → Z: V_{OL} + 0.5 V

f_{MAX} PARAMETERS

The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because the flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

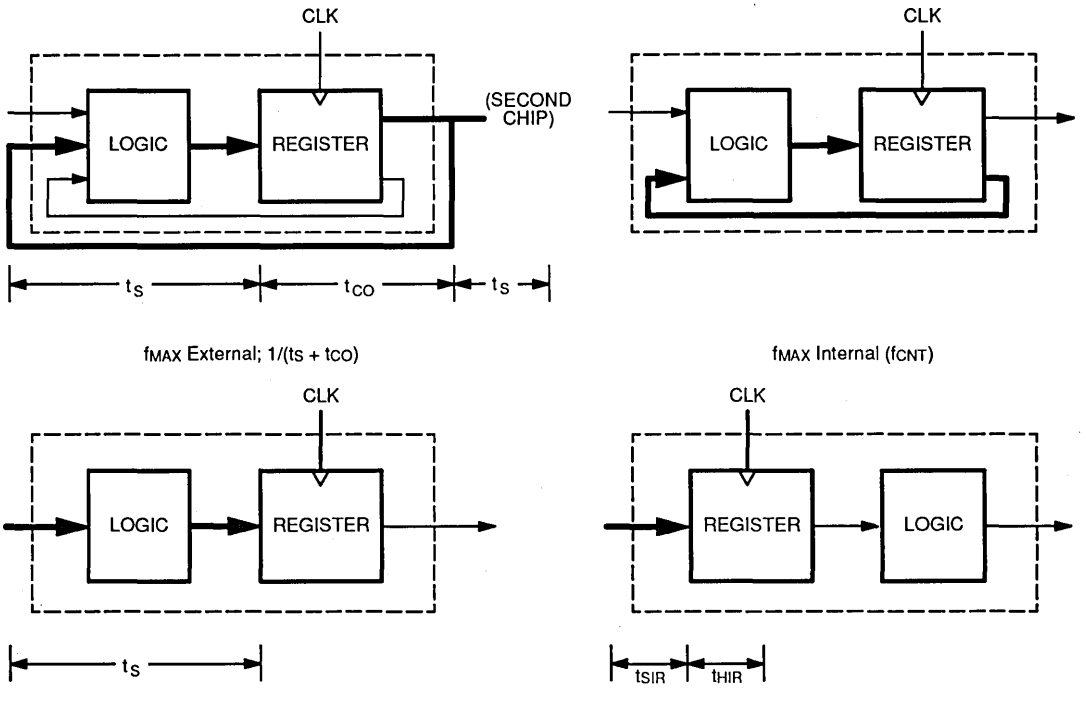
The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external."

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs. This f_{MAX} is designated "f_{MAX} internal". A simple internal counter is a good example of this type of design; therefore, this parameter is sometimes called "f_{CNT}."

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, a lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period determines the period for the third f_{MAX}, designated "f_{MAX} no feedback."

For devices with input registers, one additional f_{MAX} parameter is specified: f_{MAXIR}. Because this involves no feedback, it is calculated the same way as f_{MAX} no feedback. The minimum period will be limited either by the sum of the setup and hold times ($t_{SIR} + t_{HIR}$) or the sum of the clock widths ($t_{WICL} + t_{WICH}$). The clock widths are normally the limiting parameters, so that f_{MAXIR} is specified as $1/(t_{WICL} + t_{WICH})$. Note that if both input and output registers are use in the same path, the overall frequency will be limited by t_{ICS}.

All frequencies except f_{MAX} internal are calculated from other measured AC parameters. f_{MAX} internal is measured directly.



12350-023B

APPROXIMATING ACTUAL APPLICATION SUPPLY CURRENT

Introduction

The approach shown below will allow you to estimate the current consumption for your application. It does require some work, but the variation in current between applications can be significant, and any simple attempts at defining consumption for a "typical" application will be meaningless.

Parameters and Formulas

Dynamic operation is also important, especially on large devices like this that have many signals. However, using simple Icc vs Frequency curves is difficult, since there is great variation in behavior between a few outputs switching and all outputs switching. In addition, real-life devices have outputs that switch at different frequencies, making it difficult to assess an actual frequency for the device as a whole. Breaking the current down into its components gives a much more accurate result than trying to define a "typical" pattern.

The following formula gives you a way to approximate the actual supply current that your application will require. It is not necessary to go through all of the calculations if you do not desire to. Each component is independent, and only those components you are concerned with need be calculated.

Note that the concept of frequency used below is a little different from that normally discussed with PLDs: it generally does not refer to the clock frequency. The frequency of each individual signal must be considered, since in most designs, the different signals operate at widely differing frequencies. In many cases, a signal is not even periodic. In that case, an approximation as to the "average" frequency should be made.

There are six new parameters that are used in this formula. Values for the parameters for each product are given at the end of each individual data sheet. Note that they are typical numbers, and are not tested. The new parameters are:

- I_{CCO} The base static Icc at 25°C and 5.0 V Vcc, in mA.
- i_I The incremental current for a single input switching, but not driving logic, in µA/MHz.
- i_B The incremental current for each PAL block that an input or feedback signal drives, in µA/MHz.
- i_O The incremental current for a single output switching an unloaded output, but not driving feedback logic, in µA/MHz.
- i_V The current change due to changes in Vcc, in %/V.
- i_T The change in current due to changes in temperature, in %/°C.

The following components of the total current are considered:

- The basic DC current, I_{CCO}
- The AC components for the inputs
- The AC components for the outputs
- Vcc derating
- Temperature derating
- The output load

Calculating the AC Components

The AC components are a result of inputs and outputs switching.

Contribution of Inputs

The incremental current due to a switching input or buried feedback signal *x* can be calculated as:

$$i_{IX} = (i_I + N_{BX}\, i_B)\, f_{IX}$$

where

i_{IX} is the total incremental current for input *x*

N_{BX} is the number of PAL blocks that input *x* drives

f_{IX} is the average frequency of input *x* (not the clock frequency)

The number of blocks driven by an input, also known as the block fanout, can be determined from the MACH Report generated by the MACH Fitter after the design has been successfully fit. The fanout for each individual input is in the "Blocks" column on the far right of the "Signals—Tabular Information" table. Each block that the input drives is listed here. Note that with some devices you may see blocks in this list that you would not expect from the logic equations and signal placement. This is a normal part of the fitting process, and does not affect the logic in any way, but should be accounted for in the current calculation.

The current is calculated for each switching input and buried feedback signal; the results for each input should be summed to give the total incremental current due to switching inputs:

$$i_{IT} = \sum_{x}^{inputs\ \&\ buried} i_{IX}$$

A short-cut calculation is also possible if you can determine an "average" frequency that you can apply to all inputs, and if you can tolerate less accuracy than that given by the calculation above. Given such a single average frequency f_A, you can estimate the input contribution to current with the calculation

$$i_{IT} = (N_I i_I + N_{TBF} i_B)\, f_A$$

where

N_I is the number of inputs used

N_{TBF} is the total block fanout

The total block fanout is listed in the MACH Report that the AMD Fitter generates, just before the "Signals—Tabular Information" table. It is simply the sum of all the fanouts of the individual inputs.

An example of the part of the report that gives fanout information is shown below.

In this example, N_{TFB} is 40 for the short-cut calculation. If input contributions are to be considered individually, then N_B for inputs COUNT and LOAD is 2, since both inputs drive blocks A and B. So out of the total fanout of 40, COUNT and LOAD account for 4.

Contribution of Outputs

The incremental current for an output y is calculated as

$$i_{oy} = i_o f_{oy}$$

where

i_{oy} is the incremental current for output y

f_{oy} is the average frequency at which output y is switching (not the clock frequency)

This is calculated for each switching output; the results for each output should be summed to give the total incremental current due to switching outputs:

$$i_{oT} = \sum_{y}^{outputs} i_{oy}$$

The total AC current under nominal conditions (5.0 V V_{CC}, 25°C, 35-pF load) is then

$$I_{CCN} = I_{CCO} + i_{IT} + i_{oT}$$

Derating for V_{CC}

The current will change with applied V_{CC}. To estimate the current at a given applied V_{CC} (V_a), calculate the following:

$$I_{CCV} = I_{CCN} [1 + i_V (V_a - 5.0\ V)]$$

where

I_{CCV} is the total dynamic current derated only for V_{CC}

```
.
.
.
Wiring Completion:  100% -> (  0 nc)

|>  INFORMATION F058 - Total Block Fanout (All Signals) *: 40          <---

***Signals - Tabular Information

   Signal     #     P/N #    (Loc)      Type      Logic   # PT   Blocks
    CLK1      1       35     I  5    clock pin      .       .      ...
    COUNT     2       13     I  2      input        .       .      .AB    <---
    LOAD      3       10     I  0      input        .       .      .AB    <---
.
.
.
```

Derating for Temperature

To estimate the current at an applied temperature T_a, calculate the following:

$$I_{CCT} = I_{CCN}\ [1 + i_T\ (T_a - 25°C)\ ]$$

or

$$I_{CCVT} = I_{CCV}\ [1 + i_T\ (T_a - 25°C)\ ]$$

where

I_{CCT} is the total current derated only for temperature

I_{CCVT} is the total current derated for both V_{CC} and temperature

Note that i_T will be a negative number, since current increases as temperature decreases.

Calculating the Load Current

A load may have both capacitive and resistive portions, both of which draw current.

Capacitive Load Contribution

The dynamic current of a purely capacitive output load on an output *w* can be calculated as:

$$i_{CLw} = C_{Lw} V_{sw} f_{0w}$$

where

i_{CLw} is the incremental current due to the capacitive load on output *w*

C_{Lw} is the amount of capacitance on output *w*

V_{sw} is the voltage swing of output *w*

f_{0w} is the average frequency at which output *w* is switching (not the clock frequency)

Resistive Load Contribution

If there is a resistive component to the load, then there will be a current component that can be calculated as follows for an output *w* with a single resistor:

$$i_{RLw} = K_{DCw} \frac{V_o}{R_w}$$

where

i_{RLw} is the current due to the resistive load on output *w*

K_{Dcw} is the average duty cycle for output *w* being HIGH in the case of a resistor to ground, or LOW in the case of a resistor to V_{CC}

V_o is V_{OH} in the case of a resistor to ground, or V_{OL} in the case of a resistor to V_{CC}

R_w is the value of the terminating resistor on output *w*

If there is a resistor network with Thévenin equivalent resistance R_{eq} and voltage V_{eq}, then the current can be calculated as:

$$i_{RLw} = \frac{K_{DCH}\ (V_{OH} - V_{eq})\ +\ (1 - K_{DCH})\ (V_{eq} - V_{OL})}{R_{eq}}$$

where

K_{DCH} is the average duty cycle for output *w* being HIGH

The total current due to the load is then

$$i_{LT} = \sum_{w}^{outputs} i_{CLw} + i_{RLw}$$

Load currents can be derated for temperature, but the behavior of the load with temperature may not be available.

Summary

To get the best approximation of supply current, two fundamental components must be added: current drawn by the chip, and current drawn by the load. The former is a combination of static current and dynamic current from inputs and outputs switching. The latter is a function of the voltage swing and the kind of load. The sum of the two should give a reasonable idea of the actual supply current requirements for your application.

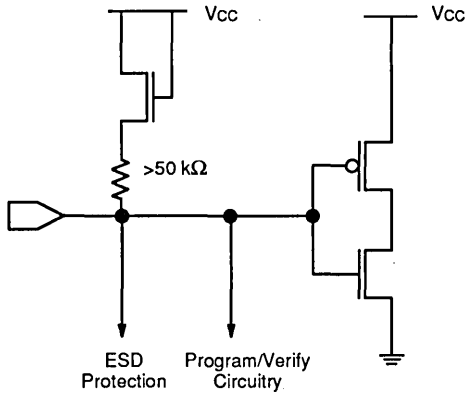
ENDURANCE CHARACTERISTICS

The MACH 3 and MACH 4 families are manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed, a feature which allows 100% testing at the factory.

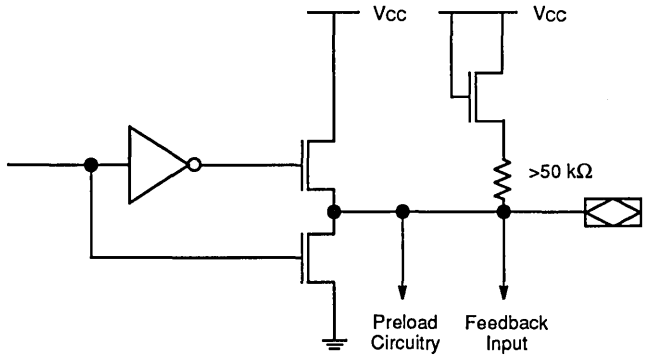
Endurance Characteristics

Parameter Symbol	Parameter Description	Min	Units	Test Conditions
t_{DR}	Min Pattern Data Retention Time	10	Years	Max Storage Temperature
		20	Years	Max Operating Temperature
N	Min Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS



Input



Output

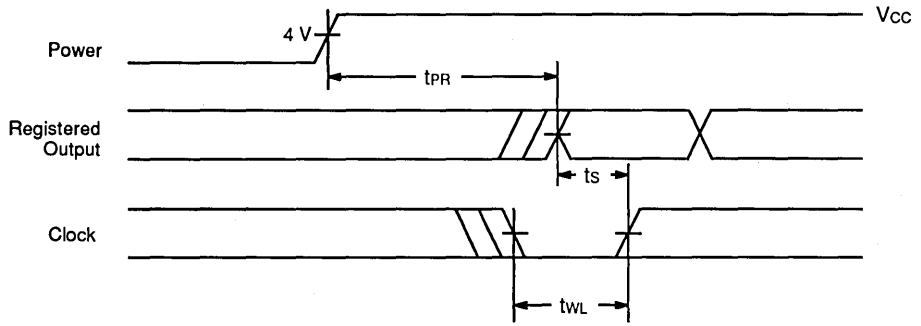
12197-013A

POWER-UP RESET

The MACH devices have been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will depend on the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Max	Unit
t_{PR}	Power-Up Reset Time	10	µs
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Reset Waveform

DEVELOPMENT SYSTEMS (subject to change)

For more information on the products listed below, please consult the AMD FusionPLD catalog.

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEMS	
Advanced Micro Devices, Inc. P.O. Box 3453, MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	MACHXL® Software	MACH355: V1.3 MACH435: V1.3 MACH445: V1.3 MACH465: V1.3
Advanced Micro Devices, Inc. P.O. Box 3453, MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	Design Center/AMD Software	MACH355: V6.1 MACH435: V6.0 MACH445: V6.1 MACH465: V6.1
Advanced Micro Devices, Inc. P.O. Box 3453, MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	AMD-ABEL Software Data I/O MACH Fitters	MACH355: In Development MACH435: V5.0 MACH445: In Development MACH465: In Development
Advanced Micro Devices, Inc. P.O. Box 3453, MS 1028 Sunnyvale, CA 94088-3543 (800) 222-9323 or (408) 732-2400	PROdeveloper/AMD Software PROsynthesis/AMD Software	MACH355: In Development MACH435: In Development MACH445: In Development MACH465: In Development
Cadence Design Systems 555 River Oaks Pkwy San Jose, CA 95134 (408) 943-1234	ComposerPIC™ Designer (Requires MACH Fitter) Verilog, LeapFrog, RapidSim Simulators (Models also available from Logic Modeling)	MACH355: Now MACH435: V3.2 MACH445: V3.3 MACH465: V3.3
Capilano Computing 960 Quayside Dr., Suite 406 New Westminster, B.C. Canada V3M 6G2 (800) 444-9064 or (604) 552-6200	MacABEL™ Software (Requires SmartPart MACH Fitter)	MACH355: Future MACH435: V5.0 MACH445: Future MACH465: Future
CINA, Inc. P.O. Box 4872 Mountain View, CA 94040 (415) 940-1723	SmartCAT Circuit Analyzer	MACH355: Future MACH435: V2.0 MACH445: Future MACH465: Future
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	ABEL™-5 Software (Requires MACH Fitter) Synario™ Software	MACH355: Future MACH435: Now MACH445: In Development MACH465: In Development
iNt GmbH Busenstrasse 6 D-8033 Martinsried, Munich, Germany (89) 857-6667	PLDSim 90	MACH355: Future MACH435: V2.60 MACH445: Future MACH465: Future
ISDATA GmbH Daimlerstr. 51 D7500 Karlsruhe 21 Germany Germany: 0721/75 10 87 U.S.: (510) 531-8553	LOG/iC™ Software (Requires MACH Fitter)	MACH355: In Development MACH435: Now MACH445: In Development MACH465: In Development
Logic Modeling 19500 NW Gibbs Dr. P.O. Box 310 Beaverton, OR 97075 (503) 690–6900	SmartModel® Library	MACH355: Future MACH435: Now MACH445: Now MACH465: In Development
Logical Devices, Inc. 692 S. Military Trail Deerfield Beach, FL 33442 (800) 331-7766 or (305) 428-6868	CUPL™ Software	MACH355: In Development MACH435: V4.4 MACH445: In Development MACH465: In Development

DEVELOPMENT SYSTEMS (subject to change) (continued)

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEMS	
Mentor Graphics Corp. 8005 S.W. Boeckman Rd. Wilsonville, OR 97070-7777 (800) 547-3000 or (503) 685-7000	PLDSynthesis™ (Requires MACH Fitter) QuickSim Simulator (Models also available from Logic Modeling)	MACH355: Now MACH435: V8.2-5 MACH445: Now MACH465: Now
MicroSim Corp. 20 Fairbanks Irvine, CA 92718 (714) 770-3022	Design Center Software (Requires MACH Fitter)	MACH355: V6.1 MACH435: V6.0 MACH445: V6.1 MACH465: V6.1
MINC Incorporated 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (800) 755-FPGA or (719) 590-1155	PLDesigner™-XL Software (Requires MACH Fitter)	MACH355: Now MACH435: V3.3 MACH445: V3.3 MACH465: V3.3
OrCAD 3175 N.W. Aloclek Dr. Hillsboro, OR 97124 (503) 690-9881	Programmable Logic Design Tools 386+ Schematic Design Tool 386+ Digital Simulation Tools	MACH355: Future MACH435: In Development MACH445: Future MACH465: Future
SUSIE–CAD 10000 Nevada Highway, Suite 201 Boulder City, NV 89005 (702) 293-2271	SUSIE™ Simulator	MACH355: In Development MACH435: V1.4 MACH445: In Development MACH465: In Development
Teradyne EDA 321 Harrison Ave. Boston, MA 02118 (800) 777-2432 or (617) 422-2793	MultiSIM Interactive Simulator LASAR	MACH355: Future MACH435: In Development MACH445: Future MACH465: Future
Viewlogic Systems, Inc. 293 Boston Post Road West Marlboro, MA 01752 (800) 442-4660 or (508) 480-0881	ViewPLD or PROPLD (Requires PROSim Simulator MACH Fitter) ViewSim Simulator (Models for ViewSim also available from Logic Modeling)	MACH355: In Development MACH435: Now MACH445: In Development MACH465: In Development
MANUFACTURER	**TEST GENERATION SYSTEM**	
Acugen Software, Inc. 427-3 Amherst St., Suite 391 Nashua, NH 03063 (603) 891-1995	ATGEN™ Test Generation Software	MACH355: Future MACH435: In Development MACH445: Future MACH465: Future
iNt GmbH Busenstrasse 6 D-8033 Martinsried, Munich, Germany (87) 857-6667	PLDCheck 90	MACH355: Future MACH435: V2.60 MACH445: Future MACH465: Future

Advanced Micro Devices is not responsible for any information relating to the products of third parties. The inclusion of such information is not a representation nor an endorsement by AMD of these products.

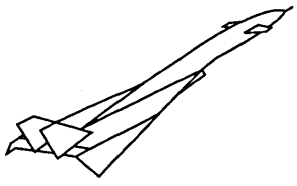
APPROVED PROGRAMMERS (subject to change)

For more information on the products listed below, please consult the AMD FusionPLD catalog.

MANUFACTURER	PROGRAMMER CONFIGURATION
Advin Systems, Inc. 1050-L East Duane Ave. Sunnyvale, CA 94086 (408) 243-7000	Pilot U84 MACH435: V10.75
BP Microsystems 100 N. Post Oak Rd. Houston, TX 77055–7237 (800) 225-2102 or (713) 688-4600	BP1200 MACH435: V2.21C MACH445: V2.34C
Data I/O Corporation 10525 Willows Road N.E. P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	UniSite™ MACH435: V4.4 MACH445: V4.6 Model 3900 MACH435: V2.2 AutoSite MACH435: V2.2
Logical Devices Inc./Digelec 692 S. Military Trail Deerfield Beach, FL 33442 (800) 331-7766 or (305) 428-6868	ALLPRO™–88 MACH435: V2.3 with Adapter only
SMS North America, Inc. 16522 NE 135th Place Redmond, WA 98052 (800) 722-4122 or SMS Im Grund 15 D-7988 Vangen Im Allgau, Germany 07522-5018	Sprint/Expert MACH435: V 1/93
Stag Microsystems Inc. 1600 Wyatt Dr. Suite 3 Santa Clara, CA 95054 (408) 988-1118 or Stag House Martinfield, Welwyn Garden City Herfordshire UK AL7 1JT 707-332148	Stag Quazar MACH435: V10.75
System General 510 S. Park Victoria Dr. Milpitas, CA 95035 (408) 263-6667 or 3F, No. 1, Alley 8, Lane 45 Bao Shing Rd., Shin Diau Taipei, Taiwan 2-917-3005	Turpro-1 MACH435: V1.68G

PROGRAMMER SOCKET ADAPTERS (subject to change)

MANUFACTURER	PART NUMBER
EDI Corporation P.O. Box 366 Patterson, CA 95363 (209) 892–3270	Contact Manufacturer
Emulation Technology 2344 Walsh Ave., Bldg. F Santa Clara, CA 95051 (408) 982–0660	MACH435: (84-Pin to 28-Pin) PLCC: AS-84-28-01P-6
Logical Systems Corp. P.O. Box 6184 Syracuse, NY 13217-6184 (315) 478-0722	MACH435: (84-Pin to 28-Pin) PLCC: PA MACH 84
Procon Technologies, Inc. 1333 Lawrence Expwy, Suite 207 Santa Clara, CA 95051 (408) 246-4456	MACH435: (84-Pin to 28-Pin) PLCC: 325-084-1221-028A



Design Tool Support for MACH 3 and 4 Devices

Advanced Micro Devices

Customers have described the ideal programmable logic design environment as one that supports several different design entry methods, has an easy to use interface, tightly integrates schematic entry and timing simulation, and offers state of the art technology such as multiple device partitioning across different types of programmable logic devices. Others feel that the ideal programmable design environment should interface tightly to PCB layout and mixed digital and analog simulation tools, and be architecture independent, while still other customers feel the ideal design tool should support devices from many different programmable logic vendors.

The trouble is that everyone's picture of the ideal programmable logic design environment is different. That's why AMD offers its customers a choice of software and programming tools for designing with MACH devices. With MACH devices, customers have a choice of design environments:

- **Support for universal design tools** customers already own: MACH device fitters and libraries are available from Cadence, Data I/O, Logical Devices, Logic Modeling, Mentor, MicroSim, Minc, OrCAD, SUSIE-CAD, Synopsys, and Viewlogic for PC-based and workstation environments. These add-on MACH device Fitters and libraries are available at little or no additional cost from the design tool vendor.

  In addition, add-on MACH device Fitters for Data I/O's ABEL software are also available from AMD and its distributors.

- **AMD-only versions of popular third-party design tools**: Through AMD and its resellers, customers can purchase AMD-only versions of popular Data I/O, MicroSim, and Viewlogic. These systems offer complete start-to-finish third-party support for MACH in a single integrated environment. These AMD-only versions also allow customers who are considering upgrading their design tools a chance to get started with higher-end tools at a lower cost. Later on, the customer can upgrade to a full universal version of these tools through the tool vendor at a reduced cost.

- **AMD-developed MACHXL software** for very low-cost, text-based design environments.

Each of these scenarios are discussed in the sections that follow.

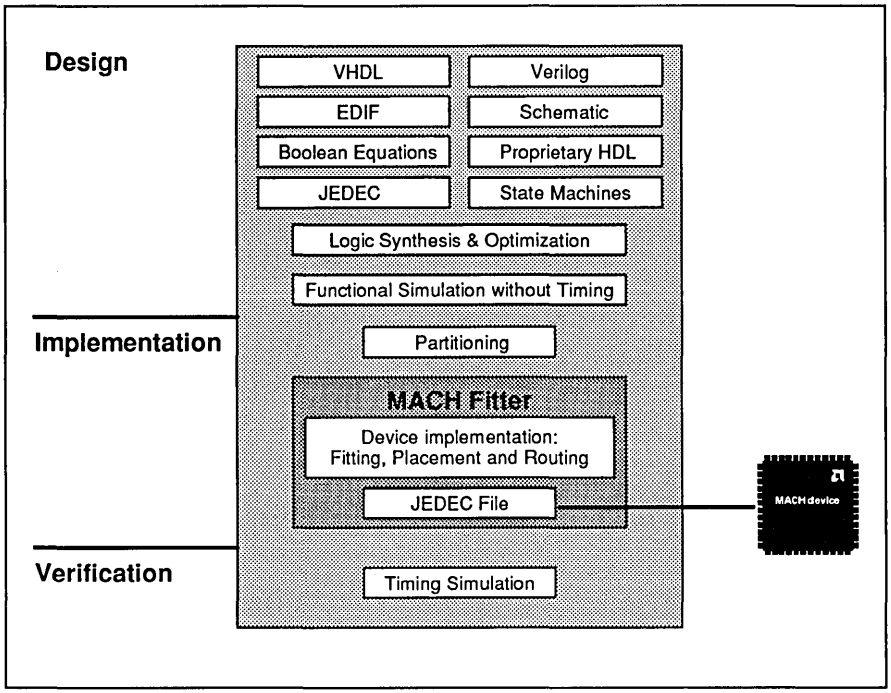
Support for Universal Design Environments

AMD's MACH devices are supported by AMD FusionPLD[SM] partners, a select group of leading third-party design tool vendors with proven track records. Actual development work with these vendors begins far in advance of AMD's introduction of new devices. Each FusionPLD partner adheres to AMD's strict quality and certification requirements. The end result is timely support of new AMD MACH devices on a large number of platforms.

Support for MACH devices is at no or little additional cost for customers currently using Cadence, Data I/O, Logical Devices, Mentor, MicroSim, Minc, OrCAD, SUSIE-CAD, Synopsys, and Viewlogic tools to design with AMD PAL devices. Most AMD PAL customers find that an add-on Fitter and MACH device libraries is all that is required to get started designing with AMD MACH devices.

Designing with MACH devices is almost as easy as designing with AMD PAL devices. Customers begin their design using traditional design entry methods—Boolean equations, schematic capture, state machine syntax, VHDL, Verilog, or a design tool's HDL—and move through logic synthesis before functionally simulating their design to verify the logic. Once a designer completes the design phase, they move on to the implementation phase where the design tool's logic compiler will partition the logic. An add-on MACH Fitter available from the third-party tool vendor performs the placement and routing steps completely within the native third-party design tool environment.

Publication# 17573 Rev. C Amendment /0
Issue Date: August 1994



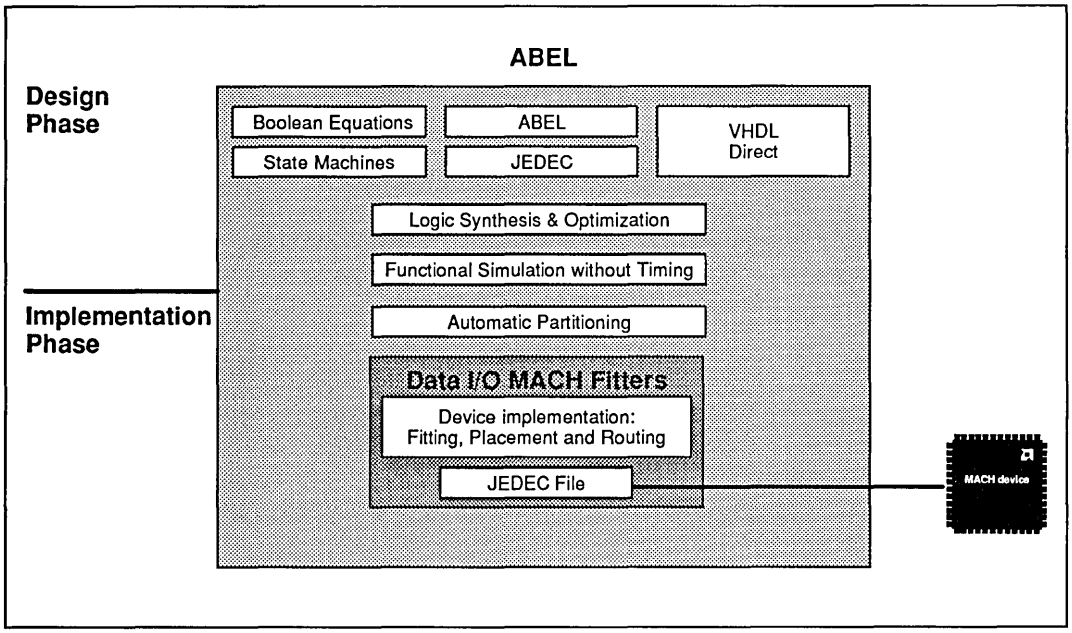
General MACH design flow for third-party design environments

Once the design has been implemented in a MACH device, the designer can verify its operation with the design tool's timing simulator and waveform analysis tools.

Note that Cadence, Mentor, MicroSim, Synopsys and Viewlogic customers who have not used these tools for PAL device designs before may also need to acquire a logic compiler for logic synthesis and minimization. These customers should verify that they have the appropriate programmable logic compiler either by running a PAL device through their system or by contacting their design tool account representative:

- Cadence: PIC-Designer software
- Mentor: PLD Synthesis II software
- MicroSim: PLSyn software
- Synopsys: Minc PLDesigner-XL software
- Viewlogic PRO Series: PROPLD software
- Viewlogic WorkView or PowerView: ViewPLD software

MACH device Fitters for these environments can be obtained directly from the third party tool vendor.



Data I/O MACH Fitters

Devices Supported	MACH110, 120, 130, 210, 215, 220, 230, and 435 devices
Design Entry	ABEL-5 for PC-DOS required
AMD Ordering Part Number	PLDSW/AMDABELB1322

Add-on MACH Fitters for Data I/O ABEL software version 5.0 or above are available from AMD and its distributors as well as Data I/O. MACH Fitters for ABEL software integrate tightly into the customer's existing ABEL-5 design environment, providing a transparent link between ABEL design descriptions and MACH-specific device Fitters. Everything a customer needs to design with MACH devices is right there in the Data I/O environment. Customers develop their designs using ABEL syntax, then compile and functionally simulate the design before choosing the SmartPart MACH Fitter from the menu. The MACH Fitter will automatically place and route the device and create the JEDEC file.

Recommended System Configuration

- ABEL-5 for PC-DOS already installed
- 640 Kbyte conventional memory, 2-4 Mbyte extended memory
- 4 Mbyte additional disk space

AMD-only Versions of Third-Party Tools

AMD and its distributors resell AMD-only versions of popular third-party design tools from MicroSim, Data I/O, and Viewlogic. These resale arrangements allow AMD to offer its customers state-of-the-art desktop-based design tools at affordable prices. All these third-party tools are AMD-certified, so designers can be confident of their resulting pinouts and JEDEC files. Most also include one year of free device updates for new MACH devices and maintenance. All these AMD-only third-party design tools can also be upgraded to full universal versions supporting other device manufacturers through the third-party tool vendor at a substantial discount.

Each of these AMD-only third-party software products— MicroSim's Design Center/AMD, Data I/O's AMD-ABEL, and Viewlogic's PROdeveloper/AMD—are discussed below.

Design Center/AMD tools are developed by MicroSim, the creator of PSpice. Design Center/AMD software offers customers device-independent high-performance logic synthesis carefully integrated with interactive schematic capture and min-max timing simulation. The Design Center/AMD system is available in two versions—a Standard version without timing simulation and a graphical editor for inputting test vectors, and an Advanced version with timing simulation and the graphical stimulus editor. An Evaluation version, supporting only the MACH210 device permits customers to evaluate the Design Center/AMD software and the MACH device architecture.

Design Center/AMD Software

Devices Supported	Standard All PAL and MACH devices	Advanced All PAL and MACH devices	Evaluation MACH210 only
Design Entry			
Schematic capture	X	X	X
Symbol editor	X	X	X
Boolean equations	X	X	X
State machines	X	X	X
Hierarchical design	X	X	X
Mixed schematic and language	X	X	X
Design Processing			
Design rule checks	X	X	X
Logic synthesis and fitting	X	X	X
User-defined device selection criteria and automated device selection	X	X	X
Single device partitioning	X	X	X
Multiple Device Partitioning	option	option	N/A
JEDEC generation	X	X	X
Backannotation of pinouts	X	X	X
Design Verification			
Functional simulation	X	X	X
Timing simulation	N/A	X	X
Waveform viewer	X	X	X
Waveform editing	text	graphical & text	graphical & text
Interactive cross probing from schematic	X	X	X
AMD Ordering Part Number			
Without Multiple Device Partitioning	PLDSW/DCSTDB1322	PLDSW/DCADVB1322	PLDSW/DCEVALB1322
With Multiple Device Partitioning	PLDSW/DCSTDMB1322	PLDSW/DCADVMB1322	N/A

Recommended System Configuration

- 386- or 486-based PC
- 8 Mbyte memory
- 20 Mbyte disk space
- MS-DOS 3.0 or later
- Microsoft Windows 3.1 or later (386 enhanced mode)
- 1.44 Mbyte 3.5" floppy disk drive

Multiple-device partitioning, an option to Design Center/AMD Standard and Advanced products, can be used to partition large designs across different types of programmable logic devices and retarget existing designs. If a design does not fit into a single device, such as a MACH435, this add-on option will split the design and implement it in more than one device, such as a MACH435 and a PALCE22V10. Because the customer controls the device selection constraints and priorities such as frequency, the type of device, maximum propagation delay, power, temperature, technology, the number of pins and the number of devices, the resulting implementation is always under their control. Design Center/AMD software will present the ten top solutions meeting the customer's constraints and priorities before generating JEDEC files for the solution the customer chooses.

AMD-ABEL software, based on Data I/O's popular ABEL-5 software, supports both AMD PAL and MACH devices and includes MACH device Fitters. AMD-ABEL is ideal for customers who are just beginning to work with AMD MACH devices or who are looking to upgrade their existing tools. It includes everything needed to get new customers designing with AMD PAL or MACH devices in a familiar PC-based environment.

	AMD-ABEL
Devices Supported	All PAL and MACH110, 120, 130, 210, 215, 220, 230, and 435 devices
Design Entry	
Boolean equations	X
State machines	X
VHDL	available from Data I/O
Design Processing	
Design rule checks	X
Logic synthesis and fitting	X
User-defined device selection criteria and automated device selection	X
Single device partitioning	X
JEDEC generation	X
Back annotation of pinouts	X
Design Verification	
Functional simulation	X
Waveform viewer	X
Waveform editing	text
AMD Ordering Part Number	PLDSW/AMDABELB1322

Recommended System Configuration

- 386- or 486-based PC
- 640 Kbyte conventional memory, 2-4 Mbyte extended memory
- 20 Mbyte disk space
- MS-DOS 5.0 or higher
- 1.44 Mbyte 3.5" floppy disk drive
- Parallel port for key
- Mouse optional
- Note: AMD-ABEL is not a Windows program, but may be used from a DOS application window.

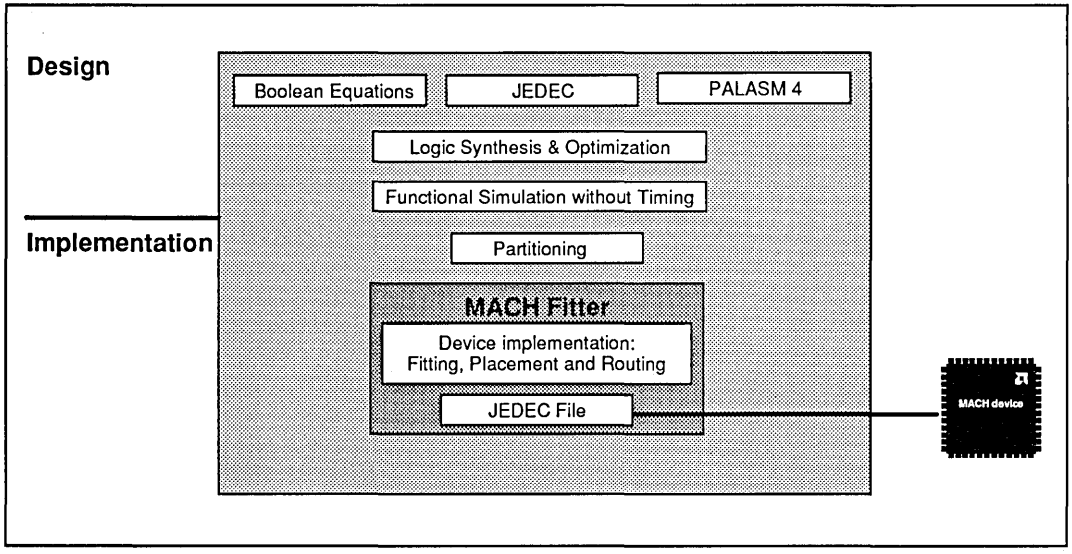
For customers who already have ABEL-5 software, the Data I/O MACH Fitters are also available separately from AMD and its distributors. See the previous section for more information.

Viewlogic's PROdeveloper/AMD software supports AMD PAL and MACH devices. Based on Viewlogic's desktop PRO Series software, PRODeveloper/AMD includes schematic and Boolean equation design entry, logic synthesis, functional and timing simulation, MACH Fitters, and waveform analysis. PROsynthesis/AMD, a VHDL design entry and simulation add-on for PRODeveloper/AMD, generates optimized MACH designs from behavioral, register transfer level, and structural VHDL descriptions. More information will be available on both products in late 1994.

AMD-Developed MACHXL Software

AMD's MACHXL software is a menu-driven entry-level tool for designing with AMD MACH devices. Based on AMD's PALASM 4 software, MACHXL software fully supports the density and flexibility of MACH devices in a low-cost, PC-based design environment.

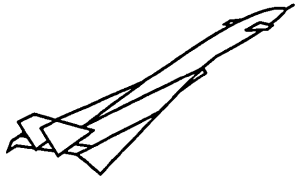
The MACHXL software design flow is shown below:



New designs begin with Boolean equation entry, by importing a PALASM 4 file, or by disassembling a JEDEC file. Customers have control over logic synthesis and optimization, and can functionally simulate before implementing their design.

	MACHXL
Devices Supported	All MACH 3 and 4 devices. MACH 1 and 2 device support late 1994.
Design Entry	
Boolean equations	X
PALASM 4 design files	X
Design Processing	
Design rule checks	X
Logic synthesis and fitting	X
Single device partitioning	X
JEDEC generation	X
Back annotation of pinouts	X
Design Verification	
Functional simulation	X
Waveform viewer	X
Waveform editing	text
AMD Ordering Part Number	AMPLDSW/MXLB1322

For a more complete description, see the MACHXL software manual or an AMD sales person.



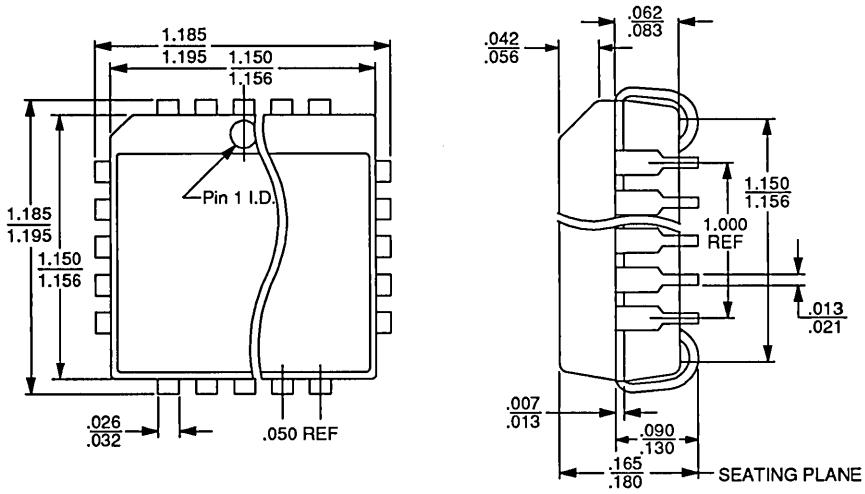
PHYSICAL DIMENSIONS*

PL 084 84-Pin Plastic Leaded Chip Carriers 114
PQR100 100-Pin Plastic Quad Flat Pack 115
PQR144 144-Pin Plastic Quad Flat Pack 116
PQR208 208-Pin Plastic Quad Flat Pack 117

PHYSICAL DIMENSIONS*

PL 084

84-Pin Plastic Leaded Chip Carrier (measured in inches)

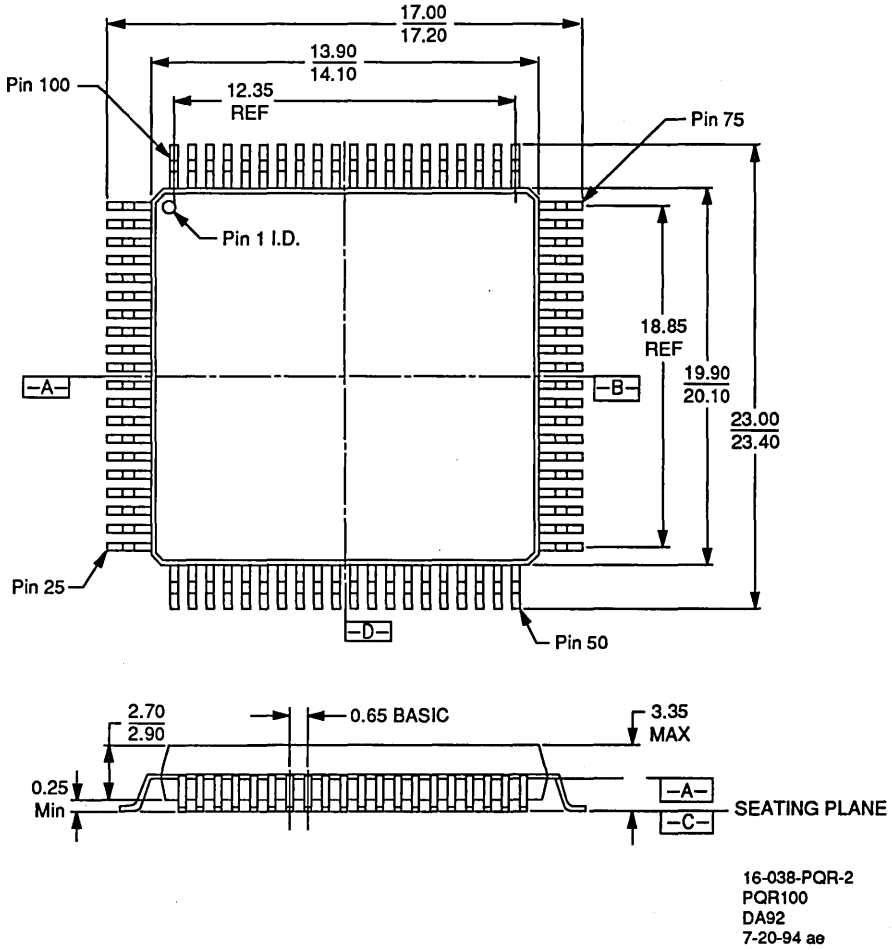


For reference only. BSC is an ANSI standard for Basic Space Centering.

PHYSICAL DIMENSIONS*

PQR100

100-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)

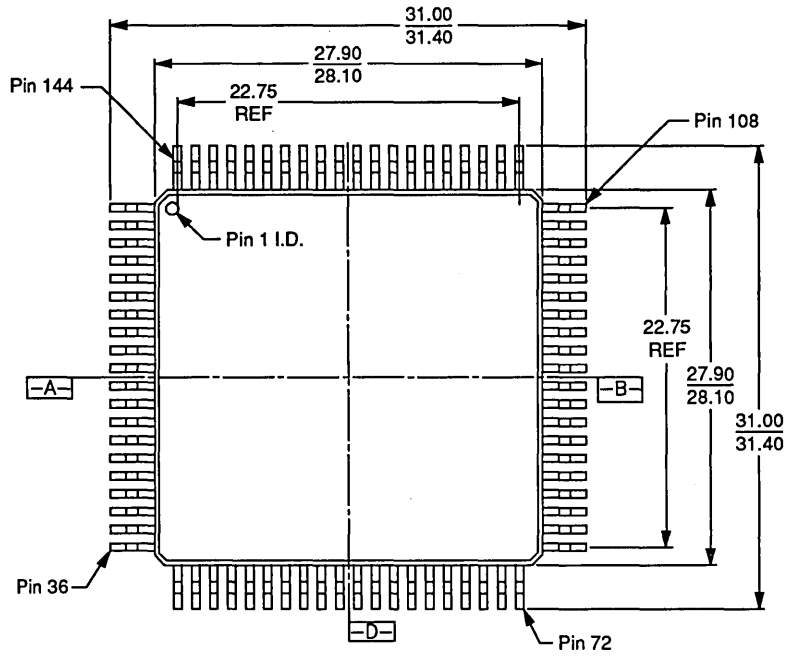


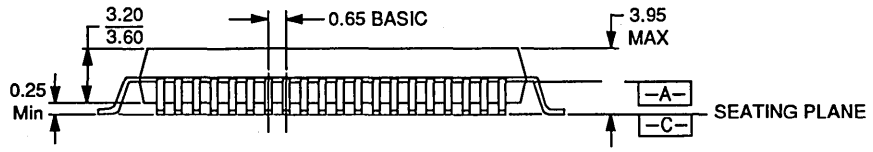
**For reference only. BSC is an ANSI standard for Basic Space Centering.*

PHYSICAL DIMENSIONS*

PQR144

144-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)





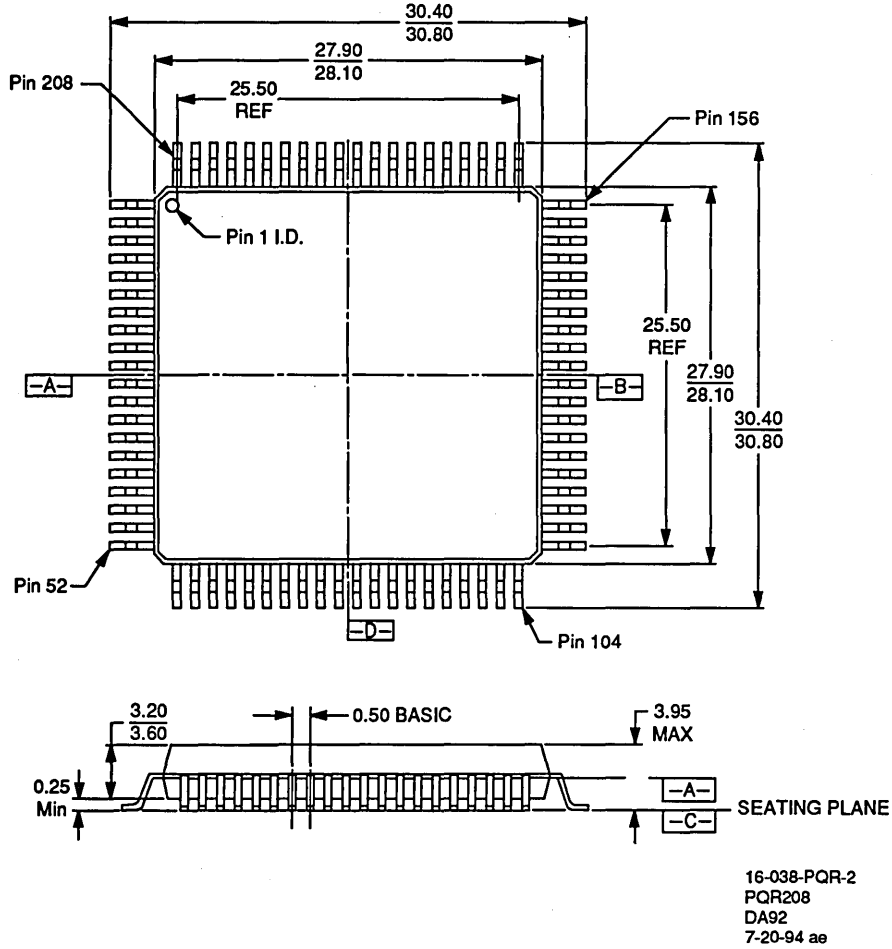
16-038-PQR-2
PQR144
DA92
7-20-94 ae

For reference only. BSC is an ANSI standard for Basic Space Centering.

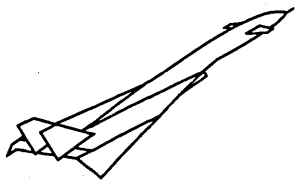
PHYSICAL DIMENSIONS*

PQR208

208-Pin Plastic Quad Flat Pack; Trimmed and Formed (measured in millimeters)



**For reference only. BSC is an ANSI standard for Basic Space Centering.*



Introduction to JTAG and Five-Volt Programming with MACH® 3 and 4 Devices

Advanced Micro Devices

Application Note

Certain members of the second-generation, high-performance, high-density, MACH devices contain features that require a formal introduction: JTAG testing capabilities and five-volt programming. Any MACH device with more than 84 pins will contain the JTAG and programming enhancements. These devices presently include the MACH445, the MACH355, and the MACH465.

The purpose of this application note is to provide the user with the basic knowledge required to understand the topics of JTAG and five-volt, on-board programming. A listing of AMD and third-party support tools is also included. Descriptions of the associated AMD MACHXL™ programming software files are found in the AMD MACHPRO™ software manual. An additional application note containing advanced system-level reconfiguration techniques is available for more exotic applications.

A BRIEF HISTORY OF JTAG

JTAG is the commonly used acronym for the IEEE Standard 1149.1-1990. The concept for this standard was proposed by a group of European companies known as the Joint European Test Action Group, or JETAG, in 1985. A year later, this group was expanded to include companies from North America and the name was changed to Joint Test Action Group, or JTAG. This group developed a standard so that circuit connectivity could be checked using a boundary-scan register approach. This standard was adopted by the Institute of Electrical and Electronics Engineers, or IEEE, in 1990. An amendment, Supplement "A", was passed in 1993 and included corrections, clarifications, and additions to the original standard.

Before the standard for boundary scan was developed, many companies were implementing their own serial or parallel scan testing methods. The JTAG standard was developed as a means of providing both board-level and device-level testing. The JTAG standard defines input and output pins, logic control functions, and instructions. To use JTAG for testing, all that is required is a four- or five-wire interface to accommodate a serial data stream and the software to drive that interface. JTAG allows access and control of each node of each JTAG-compatible integrated circuit, or IC, in order to test board connections as well as board functionality.

There are a number of benefits associated with the JTAG approach. As IC manufacturers reduce the size and increase the complexity of their devices, testing becomes more difficult with conventional methods. Printed Circuit Board, or PCB, traces have decreased in width by a factor of ten and IC package pin sizes have decreased by a factor of eight, increasing the probability of damage to the leads during conventional testing with bulky test probes. The internal array of Boundary-Scan Cells, or BSCs, become a virtual "bed-of-nails" multi-point test set-up which makes it possible to test PCB connections and circuit logic functionality independently. The structured approach of JTAG enables the research and development testing to be easily transferred to manufacturing on conventional bed-of-nails testers.

JTAG Boundary – Scan Architecture

Figure 1 illustrates an example of a device containing JTAG circuitry. The core logic remains intact, but a separate boundary scan control circuit is added to perform the JTAG functions. The five JTAG pins are used to access the state machine, instruction register, and data registers. These five pins are known as the Test Access Port, or TAP. The TMS and TCK pins drive the state-machine-based TAP controller. A boundary-scan cell is paired with every important node in the device. These nodes include all inputs, all outputs, and enable control lines. The ENABLE* pin is a dedicated non-JTAG programming pin that is utilized by AMD to program a MACH device.

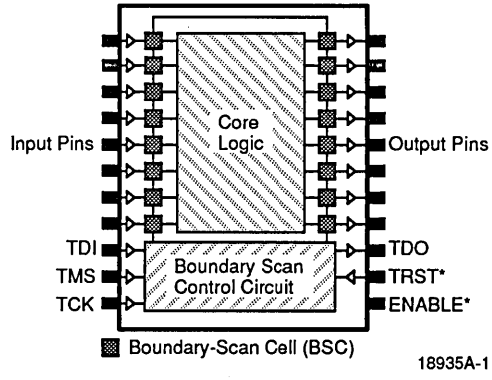


Figure 1. Boundary-Scan Architecture

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Issue Date: **March 1994**

The five JTAG pins and associated functions are defined in Table 1. The ENABLE* programming pin is included in the definitions, but is not considered part of the JTAG TAP. Details on programming appear later in this application note. The TRST* and ENABLE* pins are active LOW inputs as denoted by the asterisk.

Table 1. TAP Pin Descriptions

TCK (Test Clock)	This pin controls the state machine and data transfer operations
TMS (Test Mode Select)	Selects the boundary scan test mode, which controls the state machine test operations
TDI (Test Data Input)	Receives serial instruction codes and data on the rising edge of the TCK signal
TDO (Test Data Output)	Shifts serial output data on the falling edge of the TCK signal
TRST* (Test Reset)	Optional JTAG pin used to reset the state machine
ENABLE* (Program)	Non-JTAG pin used for programming MACH devices

JTAG TAP Controller

All implementations of JTAG are required to contain three key elements for the TAP controller. These elements include the state machine, the instruction register and the data registers. The synchronous finite state machine controls the function of the various JTAG registers. The state machine determines whether the device is in reset mode, receiving an instruction, receiving data, or idling. The state machine, as illustrated in Figure 2, is completely controlled by the TCK, TMS, and TRST* pins. The value of TMS on the edge of TCK is located next to each transition in Figure 2.

The TAP controller shifts and updates the individual JTAG registers. The data enters on the TDI pin and exits through the TDO pin. After the data is shifted into place, the TAP controller updates the register to make the data current. As stated earlier, there are boundary-scan cells on all of the inputs into the core logic and on all of the outputs from the core logic. The TAP controller manipulates both the input and the output BSCs. This allows the capability to drive inputs and capture outputs or vice versa. The pause states are included so that the shifting of data can be temporarily stopped.

When power is applied to the device, the TAP controller is forced into the Test Logic Reset state and the IDCODE register is initialized. Note that from any state position in the state machine, five consecutive ones on the TMS pin will reset the logic without the use of the optional TRST* pin. If standard four-pin JTAG is desired, tie the TRST* pin high. To disable the JTAG circuitry entirely, tie the TRST* pin low.

The second required element is an instruction register, or IR, which holds the instruction word. The instruction word length in a MACH device is six bits. The instruction decoder interprets the instruction word held in the IR. The instruction in the instruction register dictates which JTAG register acts as the data register being shifted and updated.

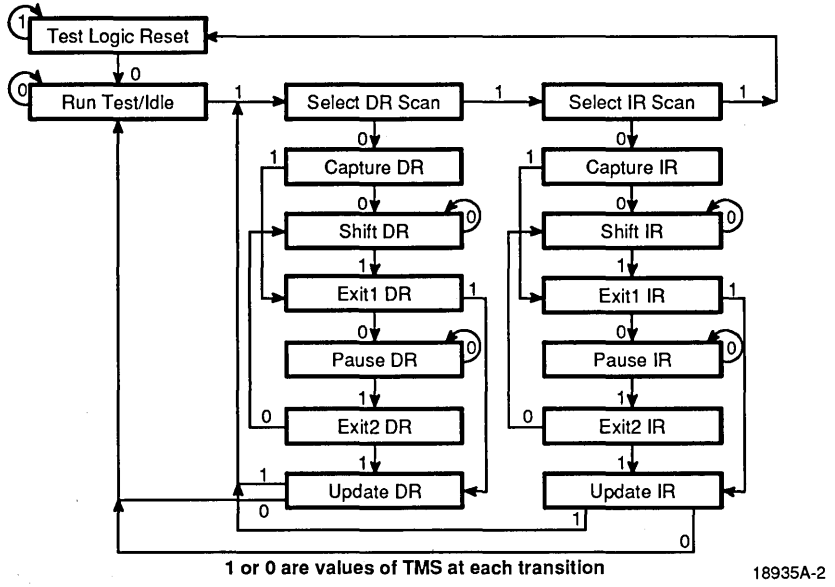


Figure 2. TAP Controller State Machine

The third element is the data registers, or DR, which could be the boundary-scan register, the IDCODE register, the USERCODE register, the row register, the column register, or the bypass register, depending on the individual instruction.

The registers illustrated in Figure 3 are part of the JTAG circuitry, with the exception of the row and column registers. The MACH device instruction register, as defined earlier, holds the six-bit instruction words. The Boundary-Scan Register is a term for the sum of all of the BSCs, so the size of this register varies with the size of the device. The IDCODE register is an optional register that contains a 32-bit word with three components: the manufacturer identification, the device identification, and the revision number. The USERCODE register is a user-specified, 32-bit word. The bypass register is a single shift register stage which provides a serial path between the TDI and TDO pins.

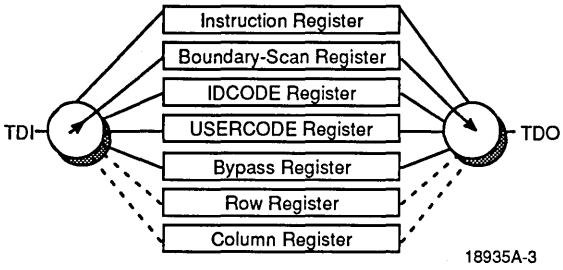


Figure 3. JTAG Instruction and Data Registers

The row and column registers implemented by AMD are not actually part of the JTAG standard but have been included here for educational purposes. The row register contains the row address when programming or verifying the device. The column register contains the column data during programming or verification.

JTAG Testing Procedure

The actual JTAG testing procedure will not be addressed in this application note. The purpose of this note is to introduce the concept of JTAG and the various components that comprise the feature. AMD does not directly support JTAG testing, however, there are a number of third-party vendors that specialize in JTAG testing hardware and software packages. These vendors include bed-of-nails manufactures such as GenRad and Teradyne, as well as exclusive JTAG testers manufactured by Texas Instruments and Corelis. A listing of presently available JTAG support contacts is provided at the end of this document.

FIVE-VOLT PROGRAMMING

Another benefit from the JTAG circuitry that AMD has derived is the ability to use the JTAG TAP for five-volt programming. This allows the device to be soldered to the board before programming. Once the device is attached, the delicate Plastic Quad Flat Pack, or PQFP, leads are protected from programming and testing operations that could potentially damage them. Programming and verification of the device is done serially which is ideal for on-board programming since it only requires the use of the TAP, along with the additional ENABLE* pin.

The ENABLE* pin is used for extra programming security. If desired, the ENABLE* pin can be connected to ground, and the device programmed with only the TAP. If TRST* is not used in the system, it too, can be removed by connecting it to V_{CC}.

Programming is the process where MACH devices are loaded with a pattern defined in a JEDEC file obtained from MACHXL software or third-party software. Programming the MACH device after it has been placed on a circuit board is a relatively simple task. Programming is accomplished by initially placing the device into programming mode, using the MACHPRO programming software provided by AMD through MACHXL or third-party software. The device is initially bulk erased and the JEDEC file is then loaded. After the data is transferred into the device, the PROGRAM instruction is loaded and the ENABLE* pin is pulsed to complete the programming sequence. Further programming details can be found in the additional advanced application note.

On-Board Programming Options

Since the MACHPRO software performs these steps automatically, the following programming options are published for educational purposes.

The configuration file, which is also known as the chain file, defines the MACH device scan path. The file contains the information concerning which JEDEC file is to be placed into which device, the state which the outputs should be placed, and whether the security fuses should be programmed. The configuration file is discussed in detail in the MACHPRO software manual.

The state of the I/Os during programming can be controlled by preloading the boundary-scan cells at the I/Os into a known state or by disabling the Output Enable for each I/O giving the I/Os a high-impedance output. This preload value is obtained from the configuration file.

There are two optional security bits for the MACH devices. The first one is the program and verify security bit. Once this bit has been programmed, all of the programming and verification options are disabled until the device is erased. Programming the second bit also prohibits the option to preload and observe the macrocell registers of the device. This allows the user to protect proprietary patterns and designs.

Program verification of a MACH device involves reading back the programmed pattern and comparing it with the original JEDEC file. The AMD method of program verification performed on the MACH devices permits the verification of only one device at a time.

Accidental Programming or Erasure Protection

It is virtually impossible to program or erase a MACH device inadvertently. The following conditions must be met before programming actually takes place:

- The device must be in the password-protected program mode
- The programming or bulk erase instruction must be in the instruction register
- The ENABLE* pin must be low

If the above conditions are not met, the programming circuitry cannot be activated. Even if the device is in program mode with a programming instruction in the register, an internal pull-up resistor on the ENABLE* pin prevents any accidental pulses from occurring.

To ensure that the AMD ten year device data retention guarantee applies, the following programming conditions should be observed:

- 100 program/erase cycle limit should not be exceeded
- Programming should not be done above 35°C ambient

These devices cannot be reprogrammed instantaneously or "on the fly" if the ambient temperature is too high. The system ambient temperature should be cooled until at least 35°C ambient before in-system programming is initiated.

Programming Multiple MACH Devices

There will often be more than one JTAG-compatible MACH device in a circuit and these devices will be connected to form a scan path. The simplest scan path is when all JTAG-compatible devices have their TMS, TCK and TRST* pins connected in parallel. The TDI and TDO pins are connected serially, where the TDO of one device is connected to the TDI of the next device. The ENABLE* pins may be connected in parallel or remain separate for individual MACH device programming access. More complex scan paths could involve multiple TDI and TDO paths or multiple TMS paths. Multiple device programming does not imply multiple device verification since verification is performed one device at a time. The user specifies which devices in the scan path to program, and the MACHPRO software will program them.

Figure 4 illustrates a map of the scan path which contains each device and its position in the chain. Any device in a scan path which has not been selected for programming must be bypassed for the entire programming and program verification cycle. This is done by loading the appropriate instruction into the device any time new instructions are loaded. Additionally, the bypass register must be taken into account any time data is being shifted through the path.

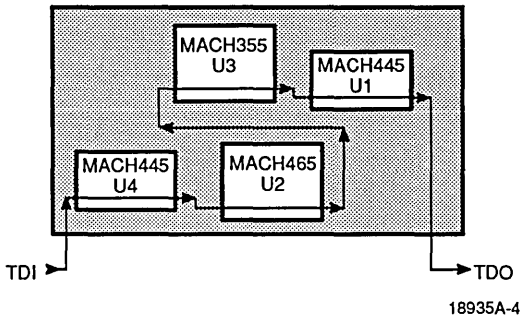


Figure 4. JTAG Scan-Path Map

The order in which program and program verification is completed is from the first device in the scan path to the last device in the chain.

Programming Hardware

The hardware interface for supporting both the JTAG and five-volt programming features requires six pins for the TAP and ENABLE* pins. Additional pins to accommodate power and ground, as well as specialized functions such as in-circuit reconfigurability and multiple scan path configurations, may be desirable.

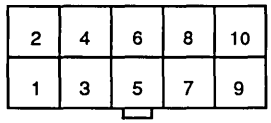
A parallel printer port of any IBM-compatible Personal Computer, or PC, is sufficient to interface with the target board containing the MACH devices. AMD supplies a cable that could be used to adequately program and test the MACH devices.

Some PC systems have software keys connected to the parallel port. Please remove these keys before using the supplied software.

The AMD cable contains the five required interface signals, plus the ENABLE* signal for programming and a ZCTL signal for advanced in-circuit configuration applications. If in-circuit reconfigurability is not required, ZCTL should be tied to ground. There is also a V_{CC} pin and two ground connections for signal integrity.

The target board cable connector is a 10 (5x2) pin female connector. The connector chosen by AMD is manufactured by Dupont and their connector number is 71602-010. The suggested target board male connector is Dupont number 71918-110 which is a 10-pin header with latches that allow for a quick disconnect. Figure 5

illustrates the cable header connector pinout locations. There is a locator key opposite of pin 5 for safety purposes.



Pin 1 - TCK Pin 2 - ZCTL
Pin 3 - TMS Pin 4 - GND
Pin 5 - TDI Pin 6 - V_{CC}
Pin 7 - TDO Pin 8 - GND
Pin 9 - TRST* Pin 10 - ENABLE*

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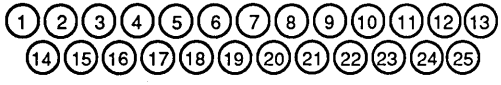
Figure 5. Board Header Cable Connector Pin Locations

The pin locations of the board header were chosen to minimize crosstalk between the wires in the ribbon cable. This header-pin configuration is supported by AMD, but individual applications may require an alternate header-pin arrangement. The AMD cable is six feet in length. If the distance from the user's computer to the target application is more than six feet, proper cable design rules should be followed in order to reliably program the MACH devices.

The connector for the computer end of the cable is a standard DB-25 male connector. The connections are illustrated in Figure 6.



Pin 1 - TRST* (STROBEB) Pin 2 - TCK (D0)
Pin 3 - TDI (D1) Pin 4 - TMS (D2)
Pin 11 - TDO (PRINTER_BUSY) Pin 12 - V_{CC} (PE)
Pin 17 - ENABLE* (ACT_SELB) Pin 23 - GND
Pin 24 - GND Pin 25 - ZCTL (GND)

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Figure 6. Computer Port Cable Connector Pin Locations

A third-party programmer could also provide programming support for the MACH devices. The programmer also uses the AMD cable which plugs into a 28-pin socket on the programmer instead of the PC parallel port. An assortment of programmer manufacturers are listed at the end of this document.

There are a number of additional programming scenarios that could also be considered. Programming practices used while protyping could vary significantly from final production methods. A number of bed-of-nails tester vendors, including GenRad and Teradyne, support MACH device programming. Contact individual vendors listed at the end of this application note for more information.

Software Support Tools

AMD's MACHXL software includes support for programming MACH devices. This software is an easy to use tool that supports the design entry, fitting, and simulation of MACH device applications. Once the design has been completed, it may be downloaded to the MACH device through the programming operation.

The five-volt programming software in MACHXL software supports multiple MACH devices and allows the user to combine AMD MACH devices with other JTAG devices in a chain. A listing of third-party software support appears at the end of this note. The FusionPLDSM Catalog contains a complete list of available third-party software support.

Programming Procedure Overview

This section provides an overview of a typical programming procedure using the MACHPRO software. This assumes that the MACH devices are already placed on the board and are linked in a serial chain with the other JTAG devices. Additional details of the programming process are available in the MACHXL software documentation as well as in the advanced application note.

Initially, the JEDEC files for the MACH devices to be programmed are generated using MACHXL or other third-party tools. Next, a serial chain description file, listing the JTAG devices in the chain and the actions to be performed on each device, is written. Then, the target board is connected to a power supply and the JTAG programming cable is attached to both the PC parallel port and the board. Finally, after the target board supply is switched on, the MACHPRO software with the associated chain file is used to program the MACH devices.

Please refer to the MACHPRO software manual for more information on writing a chain description file.

Boundary Scan Description Language File

The Boundary Scan Description Language, or BSDL, file describes the pinout of an IC. The file also describes the instruction codes and layout of the boundary-scan cells. The file does not describe the JTAG scan path. The MACHXL software creates the BSDL file from the JEDEC file.

The BSDL file declares TAP pin locations, instruction codes, register length/structure, device ID code, and whether there is a TRST* pin. To test a JTAG board, a

collection of all of the BSDL files for the JTAG ICs is required along with a netlist describing how these ICs are connected.

Additional information on BSDL files may be obtained from the Suggested Reading section.

SUGGESTED READING

IEEE Standard 1149.1-1990

IEEE Standard 1149.1-1990 Supplement A

The Boundary-Scan Handbook by Kenneth Parker

Meeting the Challenge of Boundary Scan by GenRad

Preliminary JTAG and/or Programming Support for MACH Devices

Manufacturer	Bed-of-Nails Tester Tools
GenRad 300 Baker Avenue Concord, MA 01742 508-369-4400	Model 2272
Teradyne 179 Lincoln Street Boston, MA 617-422-3567	Victory Software
Hewlett Packard Loveland, CO 80539	3070 Series

Manufacturer	JTAG Analyzer
Corelis 12607 Hidden Creek Way Suite H Cerritos, CA 90701 310-926-6727	SCANIO/280 SCANTEST Software
Texas Instruments P.O. Box 869305 Plano, TX 75086 214-575-6396	Asset

Manufacturer	Software Development System
Advanced Micro Devices P.O. Box 3453 Sunnyvale. CA 94086 (800) 222-9323	MACHXL
Data I/O 10525 Willows Road N.E P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	ABEL5
MINC Incorporated 6755 Earl Drive, Suite 200 Colorado Springs, CO 80918 (719) 590-1155	PLDesigner

Manufacturer	Programmer Support
BP Microsystems 1000 N. Post Rd. Houston, TX 77055-7237 (800) 225-2102 or (713)688-4600	BP1200
Data I/O 10525 Wiilows Road N.E P.O. Box 97046 Redmond, WA 98073-9746 (800) 332-8246 or (206) 881-6444	UniSite Model 3900 AutoSite
System General 510 S. Park Victoria Dr. Milpitas, CA 95035 (408) 263-6667	Turpro-1

Advanced In-circuit Programming Guidelines for MACH® 3 and 4 Devices

Application Note
by Kenneth Cuy, Applications Engineer, Programmable Logic Division and David Stoenner, Member of the Technical Staff, Field Applications

Advanced Micro Devices

INTRODUCTION

This application note serves as a guideline for using the JTAG interface on selected MACH 3 and 4 devices to perform in-circuit programming via a microcontroller. Although this application note will concentrate on an in-circuit programming example with an AMD Am29240™ RISC microcontroller, the information contained within can be extended to other such applications.

An additional application note entitled *Introduction to JTAG and Five-Volt Programming with MACH 3 and 4 Devices* is available to provide the basic knowledge required to understand the topics of JTAG and five-volt, on-board programming.

System Configuration

The parallel port of a standard PC was chosen as the initial tool to interface with the JTAG port for programming control. The ubiquitous availability of PCs provide a universal development environment for the MACH 3 and 4 devices that support JTAG.

The standard parallel port on a PC is composed of two register addresses in the I/O space of the PC. The two ports are the data port and the control port. The control port consists of two signals; Control which writes to the address and Status which reads to the address.

The six JTAG lines were placed on the parallel port in the following manner. TMS, TCLK and TDI are positive true, output only lines and thus were chosen to be put on the data port. As a convenience for the programmer, the data port is a positive true interface. TRST* and ENABLE* are negative true, output only lines and thus were chosen to be put on the control port. Besides being a negative true interface, the control port is always reset to a known value on power-up. TRST* and ENABLE* were selected to be Strobe and Printer Initiate signals respectively.

The only input needed is for TDO, which was selected as input on the Status Register bit D7, the Printer Busy bit.

The interfacing PAL® device, that is used for in-circuit programming, was developed to mimic the parallel port, except that only the bits needed were implemented. This allows the entire control to be put in one PAL device for simplicity, cost, and board space considerations. The example design uses a PALCE22V10 to implement the in-circuit programmability interface for the 29240 microprocessor. The design file for the 22V10 is included in Appendix A.

Interfacing PAL Device

The PALCE22V10 contained in the file JTAG.V10 has been designed to look like a standard microprocessor peripheral using a Chip Select ($\overline{CS}$), I/O Read ($\overline{RD}$), I/O Write ($\overline{WR}$) and A0. The 22V10 is composed of two sections, one to support the data port and the other to support the control and status port. The A1 bit is used in the Am29240. A higher order chip select (PIACS0) is provided with A23–A0. This allows the chip select to occupy 16 megabytes of address space. A1 is used in the equations so the MACH device can be accessed independent of the JTAG controller.

In the Am29240, the two registers (normally byte oriented) are configured on word (32 bit) boundaries for both the Am29240 hardware and the C software. Therefore, the A0 bit in the JTAG.V10 design is connected to the Am29240 address bit A2, and A1 in the 22V10 is connected to A3 of the Am29240.

The PALCE22V10 has only one clock input (pin 1) which can be used to clock any of the macrocells within the PALCE22V10. However, two registers in the design require different clocks. To solve this problem, the clock pin is used to clock the data register and the control register is implemented as transparent latches arranged in a master/slave configuration. The equation WR_CLK is used to generate the clock for the data register and is externally looped back to pin 1. The equation for WR_CLK is simply the chip select ANDED with I/O write at the correct address. D0, D1 and D2 are then registered into TDI, TCLK and TMS respectively. This is the same bit order that is used in the PC printer port configuration. These outputs are controlled by the term TRI_DISABLE which in turn is controlled by the parallel port cable. If the cable is plugged in then the outputs of the PALCE22V10 are disabled to prevent output contention. This arrangement can even be used in a manufacturing system for both development as well as in field updates.

The TRST* signal is generated from a reset input as well as the master latch called TRST_LAT. The input pin RESET will not only reset all the registers and latches but will also enable TRST* on the interface to reset the JTAG state machine in the selected MACH 3 or 4 device. In the design file, the latch equations are surrounded by MINIMIZE_OFF and MINIMIZE_ON. This is done because of the cross terms in the latch equations

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that are necessary to hold the output stable as the latch enable term goes false.

The slave latches are controlled only by chip select (CS) so any activity with the interfacing PAL device will hold TRST* and ENABLE* stable.

The remainder of the PALCE22V10 design is very straight forward in its implementation and can be followed in the design file.

System Dependent Source Code

The software written for the Am29240 interface consists of a group of low level drivers written in pseudo ANSI C for the 29K™ family and is included in Appendix B. These drivers are the only ones that change from system to system. If a different interface was chosen for the JTAG port, these drivers are all that is needed to be rewritten for the target system. These drivers are written so that they can directly interface to the C compiler for the 29K family and adhere to the 29K calling convention.

Please contact your local sales office for details on a supplement entitled *MACHPRO™ Downloading Software: C Source Code* which contains the C source code for AMD's MACHPRO programming software. MACHPRO uses the JTAG circuitry on selected MACH devices to program and verify the devices via the PC parallel port. The required drivers listed below need to be integrated with the existing MACHPRO software so that programming may now be performed via a microcontroller.

Required Drivers

Listed below are all of the low level drivers necessary to implement in-circuit programming with the selected JTAG compatible MACH devices. An effort was made to keep the drivers simple and easy to embed for the user.

- _JTAG_reset_interface()

  This routine is called at the beginning of the main program and establishes the JTAG interface to a known state.

  This state is:

ENABLE*	FALSE (Logic High)
TRST*	FALSE (Logic High)
TMS	FALSE (Logic Low)
TCLK	TRUE (Logic High)
TDI	FALSE (Logic Low)

- _JTAG_reset()

  This routine will pulse the TRST* pin for a reset pulse

- _JTAG_pgm_pulse(pulse_width)

  This routine will pulse the ENABLE* pin for the duration of the input variable pulse_width in milliseconds. For the 29K there is a system call to the Host Interface (HIF) that will return a clock with a resolution of 1 millisecond. So this routine will set the ENABLE* pin true and then call the clock routine once to establish a starting time and then it will loop calling the clock routine again until the correct time has elapsed. It will then set the ENABLE* pin false and return.

- _JTAG_pgm_set(value)

  This routine will set the ENABLE* pin to the value specified in the D3 bit position of the input variable.

- _JTAG_shift(TDI_value, TMS_value)

  This routine will shift out one bit on to the TDI line and at the end will read the TDO input and return this value. The routine will first set TCLK low, TDI to the value specified in the TDI_value variable and TMS to the value specified in the TMS_value variable. Then the TCLK pin will be set high and then set low and the D7 bit will be read and right justified in the return register.

- _setup()

  This routine simply sets up the PIA port of the Am29240 for 3 clock cycle wait state operation. This is also compatible with the Am29200™.

REFERENCES

Introduction to JTAG and Five-Volt Programming with MACH 3 and 4 Devices

MACH 3 and 4 Family Data Book

MACHPRO™ Programming Software Manual

Am29240™, Am29245™, and Am29243™ RISC Microcontrollers User's Manual and Data Sheet

IEEE Standard 1149.1–1990

IEEE Standard 1149.1–1990 Supplement A

APPENDIX A

PALASM® Design Files

```
;PALASM Design Description

;---------------------------------- Declaration Segment ------------

TITLE     JTAG CONTROL PAL FOR MACH 3XX AND MACH4XX PAL FAMILY
PATTERN   JTAG.V10
REVISION A
AUTHOR    DAVID STOENNER
COMPANY   ADVANCED MICRO DEVICES

DATE      06/21/93

CHIP   _jtag   PAL22V10

;---------------------------------- PIN Declarations ---------------

PIN   1          CLK                                                ;
PIN   2          /CS                                                ;
PIN   3          /RD                                                ;
PIN   4          /WR                                                ;
PIN   5          A0                                                 ;
PIN   6          A1                                                 ;
PIN   7          D0                                                 ;
PIN   8          D1                                                 ;
PIN   9          D2                                                 ;
PIN   10         D3                                                 ;
PIN   11         /RESET                                             ;
PIN   12         GND                                                ;
PIN   13         /TRI_DISABLE                                       ;
PIN   14         D7                                                 ;
PIN   15         /PRM_EN                                            ;
PIN   16         TRST_LAT                                           ;
PIN   17         PRM_EN_LAT                                         ;
PIN   18         /TRST                                              ;
PIN   19         TDO                                                ;
PIN   20         TDI                                                ;
PIN   21         TMS                                                ;
PIN   22         TCLK                                               ;
PIN   23         /WR_CLK                                            ;
PIN   24         VCC                                                ;
NODE  1          GLOBAL                                             ;

;---------------------------------- Boolean Equation Segment ------

EQUATIONS

GLOBAL.RSTF = RESET

MINIMIZE_OFF
```

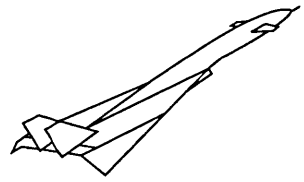
```
TRST =   RESET
       + TRST_LAT*/CS*/RESET
       + TRST*TRST_LAT*/RESET
       + TRST*CS*/RESET

PRM_EN =    PRM_EN_LAT*/CS*/RESET
          + PRM_EN*PRM_EN_LAT
          + PRM_EN*CS*/RESET

TRST_LAT =   CS*WR*A0*D0*/A1*/RESET
           + TRST_LAT*/(CS*WR*A0*/A1)*/RESET
           + TRST_LAT*D0*/RESET

PRM_EN_LAT =   CS*WR*A0*/A1*D3*/RESET
             + PRM_EN_LAT*/(CS*WR*A0*/A1)*/RESET
             + PRM_EN_LAT*D3*/RESET

MINIMIZE_ON

WR_CLK = CS*WR*/A0*/A1*/RESET

; NOTE PIN 23 ( WR_CLK ) IS EXTERNALLY CONNECTED TO PIN 1 ( CLK ) FOR

; THE CLOCKED REGISTER.

TDI := D0

TCLK := D1

TMS := D2

D7 = TDO

D7.TRST = CS*RD*/A1*A0*/RESET

TRST.TRST = /TRI_DISABLE*/RESET

TDI.TRST = /TRI_DISABLE*/RESET

TCLK.TRST = /TRI_DISABLE*/RESET

PRM_EN.TRST = /TRI_DISABLE*/RESET

;---------------------------------------------------------------------
```

Low Level Drivers

```
    pragma On(Pointers_compatible_with_ints);

    volatile int *Data_Reg ;
    volatile int *Command_Reg ;
    volatile int *Status_Reg ;
    volatile int *PIA_Control;

#define     TRST        0x1
#define     PGM_EN      0x8
#define     TDI         0x1
#define     TCLK        0x2
#define     TMS         0x4

extern clock();

void JTAG_reset_interface()

/* We will give the interface a reset pulse and then do 5 TCLK with TMS
   = 1 which will reset the state machine to reset if the reset pulse
   did not work. It will then leave the interface with the command
   register = 0 and the data register = tclk = 0 tdi = 0 and tms = 1. */

{

    *Command_Reg = TRST;
    *Command_Reg = 0;
    *Data_Reg = TMS;
    *Data_Reg = TMS | TCLK;
    *Data_Reg = TMS;
    *Data_Reg = TMS | TCLK;
    *Data_Reg = TMS;
    *Data_Reg = TMS | TCLK;
    *Data_Reg = TMS;
    *Data_Reg = TMS | TCLK;
    *Data_Reg = TMS;
    *Data_Reg = TMS | TCLK;
    *Data_Reg = TMS;

    return;

}

void JTAG_reset()

{

    *Command_Reg = TRST;
    *Command_Reg = 0;

    return;

}

void JTAG_pgm_pulse(w)
```

```
    int w;
{
    int start;

/* Now that the program enable is on we will start the timeout in
   milliseconds for the pulse width.  A system call to clock ( HIF
   service call 273 ) will return the time in milliseconds in gr96, so
   we will just do a compare to the pulse width value and loop till the
   time has passed. */

    start = clock();
    *Command_Reg = PGM_EN;

/* now do another system clock call and start the timeout loop */

    while(clock()-start < w){;}
    *Command_Reg=0;

   return;

}

void JTAG_pgm_set(in)

int in;

{

    *Command_Reg = (in & 0x1)<<3;

    return;

}

int JTAG_shift(tdi,tms)

    int tms,tdi;

{

    int temp;
    temp = ( tms & 1 ) << 2 | ( tdi & 1 );
    *Data_Reg = temp;
    *Data_Reg = temp | TCLK;
    *Data_Reg = temp;
    return(( *Status_Reg & 0x80 ) >> 7 );

}

void setup()

/* This routine sets up the PIA controller on the 292XX microcontroller
   to the needed values. For any race conditions we will set the IO
   extend bit and make the interface 3 wait states so that both the
   29200 and 29240 behave identical. This port is at 0x80000020. We will
   only affect PIACS0 so we will leave the other set up as is. */
{

    Data_Reg = 0x90000000;
    Command_Reg = 0x90000004;
    Status_Reg = 0x90000004;
    PIA_Control = 0x80000020;
    *PIA_Control = ( *PIA_Control & 0x00ffffff ) | 0x83<<24;

    return;
}
```

NOTES



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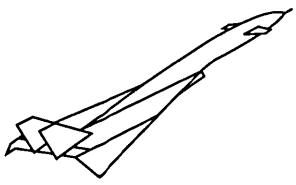

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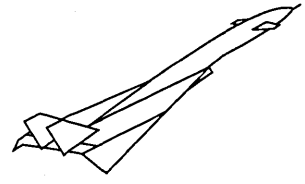

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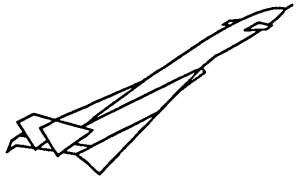

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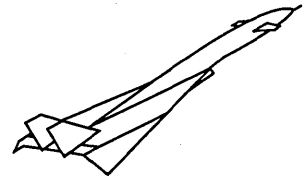
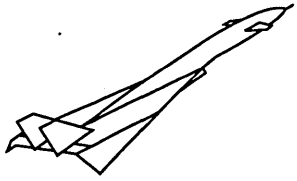


NOTES



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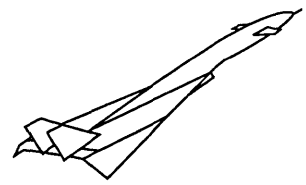

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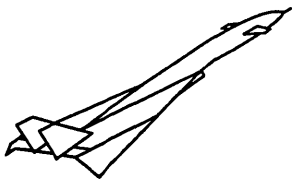

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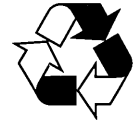

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